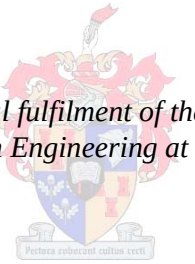
Digital Control of Line-Interactive UPS

by

JF van Papendorp



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Declaration

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Abstract

The digital control of UPS systems has been difficult in the past due to a lack of DSP technology. It was for this reason not possible to establishing the necessary control to regulate the voltages and currents of the UPS systems. Recent advances in DSP technology have however provided the means of establishing central control of the UPS system as well as incorporating more complex closed-loop control algorithms by utilising a single floating-point DSP.

Closed-loop control strategies are investigated and the central control of a line-interactive UPS is established in this study. Both the status of the physical system as well as various system parameters are controlled. The system both regulates and charges the storage batteries when the main utility supply is maintained. In the event that the utility fails, the converter instantaneously changes power flow towards the load with the aim of maintaining an uninterrupted voltage supply.

Several closed-loop deadbeat based control strategies are investigated for the regulation of the inductor current. A solution for the regulation of the DC-link is also developed and implemented. Furthermore, an intensive study is done on the regulation of the voltage supplied to the load in the event that the utility supply fails. The investigation is initially approached by considering classical control theory. Although these control strategies provided sufficient results, a predictive strategy that is based on the physical conditions of the switching converter is finally investigated to establish closed loop control of the output voltage. This resulted in a high-bandwidth voltage controller capable of maintaining control under a wide-array of load conditions.

Opsomming

Die digitale beheer van UPS stelsels was moeilik in the verlede as gevolg van ‘n gebrek aan DSP tegnologie. Dit was vir hierdie rede nie moontlik om beheer te kon bewerkstelling ten einde die spannings and strome in the UPS stelsels te kon reguleer nie. Onlangse vordering in DSP tegnologie het egter dit moontlik gemaak om sentrale beheer van die UPS stelsel te bewerkstellig sowel as om meer komplekse geslote lus beheer algoritmes te inkorporeer met behulp van ‘n enkele DSP.

Geslote lus beheer strategiëe word ondersoek en die sentrale beheer van die line-interaktiewe UPS word bewerkstellig in hierdie studie. Beide die huidige toestand van die fisiese stelsel sowel as die verskeie parameters word beheer. Die stelsel beide laai en reguleer die batterye terwyl die hooftoevoer onderhou word. In die geval dat die hooftoevoer faal, word die omsetter se rigting van drywingsvloei verander om die las te voorsien van ‘n ononderbroke spannings toevoer.

Verskeie geslote-lus “deadbeat” beheer strategiëe word ondersoek vir die regulasie van die induktor stroom. ‘n Oplossing vir die regulasie van die GS-koppervlak word ook ontwikkel en geïmplementeer. Verder word ‘n intensiewe studie gedoen op regulasie van die spanning wat aan die las gevoer word in die geval dat die hooftoevoer faal. Hierdie ondersoek word aanvanklik benader deur klassieke beheer teorie te bestudeer. Alhoewel hierdie beheer strategiëe voldoene resultate gebied het, was ‘n voorspel beheerstrategie gebaseer op die fisiese toestand van die omsetter finaal ondersoek. Die resultaat is ‘n hoë-bandwydte spannings beheerder wat daartoe instaat is om beheer te handhaaf onder ‘n verskeidenheid van lastoestande.

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Nomenclatures

AC	Alternating Current
ADC	Analog to Digital Converter
ALU	Arithmetic Logic Unit
APF	Active Power Filter
CMRR	Common-Mode Rejection Ratio
CPLD	Complex Programmable Logic Device
DC	Direct Current
DEPWM	Double-Edge PWM
DQ	Direct-Quadrature
DSC	Digital Signal Controller
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
ENOB	Effective Number of Bits
FSR	Full-Scale Range
GBP	Gain-Bandwidth Product
HMI	Human Machine Interface
IGBT	Isolated Gate Bipolar Transistor
LEPWM	Leading-Edge PWM
LSB	Least Significant Bit
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
MSB	Most Significant Bit
PCB	Printed Circuit Board
PCC	Point of Common Coupling
PI	Proportional Integral
PM	Phase Margin
PWM	Pulsewidth Modulation
RMS	Root Mean Squared
RTC	Real-Time Clock
SAR	Successive Approximation Register
SD	Secure-Digital
SEPWM	Single-Edge PWM
SHA	Sample-and-Hold Amplifier
SINAD	Signal-to-Noise Ratio + Distortion
SMPS	Switch-Mode Power Supply
SNR	Signal-to-Noise Ratio
SNR	Signal to Noise Ratio
SVM	Space Vector Modulation
SVPWM	Space Vector Pulsewidth Modulation

TEPWM	Trailing-Edge PWM
THD	Total Harmonic Distortion
THD+N	Total Harmonic Distortion and Noise
UPS	Uninterruptible Power Supply
VSI	Voltage-Source Inverter

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1 INTRODUCTION

1.1 Improving the Quality of the Electricity Supply

An inherent part of any country's infrastructure is its electricity supply network. The electricity supplied by the national power utility must comply with numerous requirements. These requirements have been developed over the years and been set out in regulations that specify with which degree of quality the electricity supplied by the utility must comply. Some of these deviations, as discussed by [1] and [2], include over- and under-voltages for a few or more supply cycles, voltage spikes, harmonic distortions, frequency fluctuations and electromagnetic interferences (EMI).

There exist several solutions of mitigating the abovementioned voltage deviation with each having its respective advantages. A tap changer proposed by [3] and an electronic voltage regulator proposed by [4] can be used to compensate for over-and under-voltages. Furthermore, a multilevel converter such as the solid-state transformer as proposed by [5] and [6] assists in the mitigation of transient pollutants like harmonic distortions, voltage spikes, etc. None of these proposals, however, are able to ensure a continued supply of power to the end-user upon the occurrence of a power outage. The uninterruptible power system (UPS) is used to address this shortcoming.

With electrical loads becoming increasingly more technologically sophisticated, there is a growing need for a high quality supply of power from the supply grid. With an ever expanding grid, the risk on components such as transmission equipment is also increasing resulting in the further deterioration of the supply power quality. Traditional power quality mitigation devices like the simple UPS and the active power filter have been used to address power outages, supply harmonics and power factor problems, to name a few. In the following section the low conversion efficiency and unacceptable harmonics [7] generated by certain UPS topologies will pointed out.

It will be shown that the line-interactive UPS does not have these disadvantages if it is appropriately controlled by a good control scheme. The line-interactive UPS is a multi-functional, high-efficiency bi-directional; shunt connected, power quality compensator with a static switching converter [7]. Depending on the digital control scheme, the line-interactive UPS is capable of both active filtering, voltage regulation and dip compensation. Additionally, it is capable of supplying uninterrupted power to the load when the supply voltage deviates outside an allowable limit.

1.2 The Uninterruptible Power System (UPS)

One of the most important qualities that an electrical utility must have is that it has to be able to supply electrical power that will satisfy the demands of all the end-users of the national grid. It is, however, not always possible to guarantee a constant supply of power to all end-devices.

Numerous solutions have been proposed and developed to ensure constant power supply to an end-user. Some of these include the integration of renewable energy sources like solar photovoltaic power systems or small-scale wind generators in the electrical infrastructure of the end-user. Another popular solution is the installation of a backup generator at the end-user that utilises fossil fuels like gas or diesel. The generator will supply the required power upon the occurrence of a power outage. The problem with this setup is that the generator requires a finite amount of time to initialise before being capable of supplying the power demanded by the end-user. It is during this start up time that the end-devices will be without electrical power. The inclusion of an uninterruptible power system (UPS) at the point of common coupling (PCC)[1] will increase the guarantee that the end-user is provided with a constant supply of power.

In addition to acting as precaution against power outages, a UPS is also capable of mitigating various types of faults and voltage deviations. Depending on the topology of the UPS, as discussed in section 1.3, the UPS is capable of mitigating some or all of the deviations mentioned in section 1.1. Notwithstanding common misconceptions, it is not always required that the UPS instantly provide electrical power once an outage occurs, since the IEC 61000-4 standard [8] specifies a "ride-through" duration that certain types of end-devices have to adhere to.

The manner in which the system controlling the UPS operates, greatly affects the degree to which the UPS is capable of diminishing voltage deviations. The control of the output is generally based on three types of control systems, one being, the closed-loop or feedback controller where the signal supplied by the system is measured and fed back to the controller to diminish any errors made in the waveform. Conversely, the second control system is open-loop control where the controller is unaware of the condition of the signal it outputs. Additionally, the open-loop control system can be augmented by including a path to respond to a disturbance in the system. Such a system is called a feed-forward system. The voltage output quality is generally superior if closed-loop control strategies are employed rather than simply operating the UPS in an open-loop manner. Sudden changes in load conditions can more successfully be dealt with if closed-loop control topologies are used, where the use of open-loop controllers does not necessarily ensure voltage stability under changing load conditions. Nevertheless, high power UPS systems are capable of supplying stable and relatively high quality electrical power to the end-user. It is nonetheless undeniable that the

[1] The PCC is defined by [54] as the interface between a source and load in an electrical system.

voltage quality will be affected by the load conditions, since the UPS is incapable of correcting errors in the voltage waveform supplied to the user. On the other hand, closed-loop controllers are capable of removing these voltage errors.

It has been established that the utilisation of a closed-loop control topology will ensure diminished deviations in the voltage supplied by a UPS. It is, on the other hand, extremely difficult for the controller to eliminate these voltage deviations totally. This incapability consequently affects the voltage quality provided by the UPS. Poor quality in the power supplied by the UPS to any end-device can greatly reduce the lifetime of sensitive devices and even cause permanent damage or failure. It is therefore of the utmost importance that the UPS be able to provide power of sufficient high quality to the end-devices under any conditions. It is thus important to investigate the performance of closed-loop strategies in UPS applications.

1.3 UPS Topologies

According to Sölter [2] and the IEC 62040-3 regulation [9] there are generally three categories of UPS systems:

- Passive-Standby Off-line UPS
- Double-Conversion On-line UPS
- Line-Interactive UPS

The IEC 62040-3 standard [9] has specified that a UPS must provide the load with isolation from as many of the disturbances and faults discussed in section 1.1 as possible. The extent to which the UPS is able to mitigate these disturbances partly depends upon its topology. The different topological classifications will be discussed in the following sections.

When the primary utility is maintained, the UPS system operates in Normal-Mode, whereby it will charge its storage medium. If the primary utility however fails, the system will go into UPS-Mode. During this mode the energy from the storage medium will be converted to provide the load with an uninterrupted supply of power.

1.3.1 Passive-Standby Offline UPS

According to Karve [10] the accepted passive-standby offline topology as defined by the IEC 62040-3 standard is illustrated in Figure 1-1.

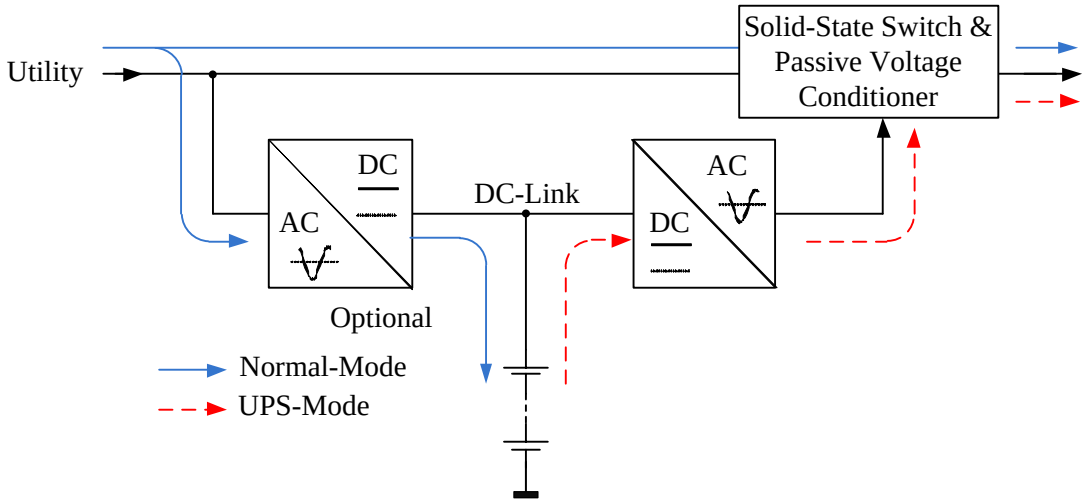

Figure 1-1: Passive-Standby Topology

This topology has the clear advantage of being a relatively simple design. It utilises either an electronic or electromechanical switch to transfer the supply of power to the load from either the UPS or the utility supply. It is however common that these switches are solid-state switches to ensure quick transition between supply sources. In the event that the utility supply goes outside the specified tolerance range or fails outright, the UPS switch will transfer the supply of power to the inverter. This transition from utility supply to inverter supply has a relatively long duration (usually 10 ms or longer). This might result in the load experiencing a brief loss of power. The long transition is acceptable with certain end-devices that must comply with the IEC 61000 standard that specifies a “ride-through” duration upon the occurrence of brief power failures, but this situation is in general unacceptable for most end-devices. The simplicity of the design is also the great disadvantage of the topology, since it is incapable of effectively mitigating voltage deviations. It is unable to provide isolation for voltage fluctuations that occur on the utility supply.

This topology is a result of a compromise between isolation from voltage disturbances and cost, and is the worst topology to be used for protection from voltage disturbance and faults.

1.3.2 Double-Conversion On-line UPS

The double-conversion on-line UPS topology employs, as its name implies, two converters. If the graphical representation of this topology in Figure 1-2 is considered, it is clear that a cascaded combination of the two converters is used. This combination provides a highly advantageous condition for the load, where the voltage supplied to the load is decoupled from the voltage supplied by the utility. In other words, any voltage disturbances and/or fault that occur on the utility will not affect the voltage supplied to the load.

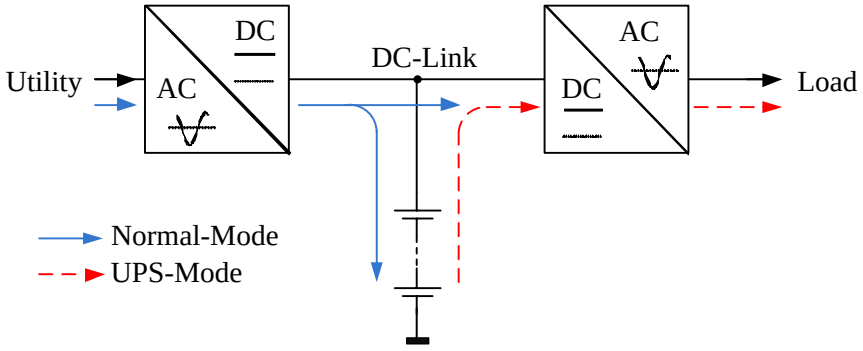

Figure 1-2: Double-Conversion On-Line UPS Topology

The advantage of having a decoupled load supply is due to the organisation of the two converters. The AC-DC converter provides a controlled DC-link to be used by the load-side DC-AC inverter. This converter also ensures that the current drawn from the utility is similarly decoupled from the current drawn by the load [11]. In other words, if a pulsating current is drawn from the UPS, the utility-side AC-DC converter ensures that a smooth sinusoidal current waveform is drawn from the utility. Furthermore, the controlled DC-link combined with the stabilising characteristics of the bus capacitors, ensures the effective elimination of any irregularities that occur on the utility voltage.

Unlike the line-interactive UPS (discussed in the following section), the double-conversion on-line UPS is able to operate under conditions with lower-than-nominal utility supply voltage. This means that if a long duration under-voltage situation occurs on the utility supply, the load voltage will be unaffected since power will be drawn from the storage batteries. Another great advantage that this topology provides above a line-interactive UPS topology, is that the load-side converter can be configured to comply with customisable UPS specifications and can even supply voltage at a different frequency than the utility supply. This is definitely not possible with a line-interactive UPS topology. The double-conversion on-line UPS topology however has a few disadvantages.

One of the main disadvantages associated with this converter is that the two converters will operate continuously over the full power rating spread of the UPS. This corresponds with an increase in the converters' temperatures and subsequently a reduced efficiency and expected operating lifetime. The utilisation of two converters in series also increases the complexity of the UPS and moreover implies reduced overall reliability. This increased complexity in the power path increases the probability of failure and a subsequent power loss experienced by the load.

A UPS utilising this topology commonly contains a solid-state bypass switch that is used in the case of extended overload conditions, as pointed out by [11]. It is during the transition to the bypass mode that the power supply to the load will be lost for a few milliseconds. It is important to point out that this is not the case with a line-interactive UPS. Transfer from normal-mode to UPS-mode in a line-interactive UPS does

not correspond with a short duration loss of power to the load. Constant power supply is ensured as long as the UPS load conditions comply with the specifications set out by the IEC 62040-3 regulation [9], [11].

This topology is still commonly used in applications with larger than 10 kVA power ratings [12], notwithstanding the disadvantages associated with this topology. All things considered, this topology provides a means of effectively mitigating most or even all of the voltage disturbances and faults identified in section 1.1.

1.3.3 Line-Interactive UPS

A line-interactive UPS regulates the AC power delivered by the electrical utility to a load and generally consists of one converter. Figure 1-3 depicts the general topology of the line-interactive UPS.

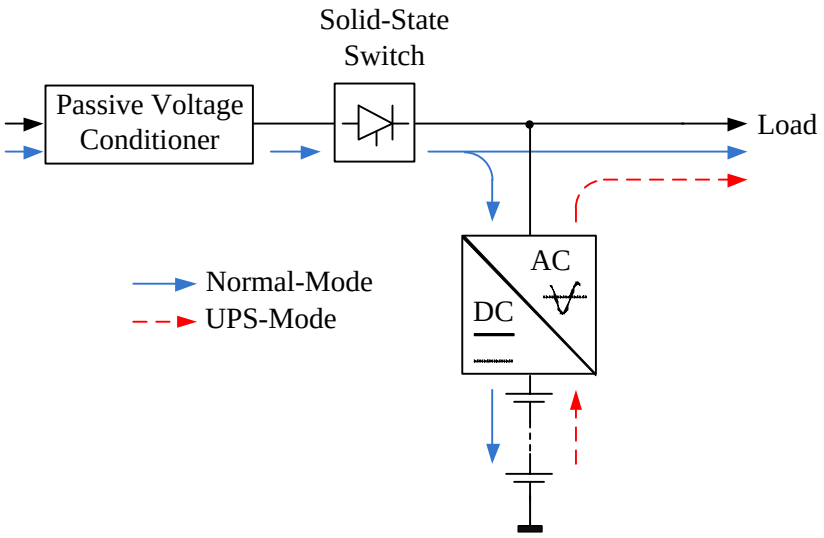

Figure 1-3: Line-Interactive Topology

The line-interactive UPS is incapable of actively suppressing voltage fluctuations and disturbances as successfully as the double-conversion on-line UPS. The voltage conditioner module usually consists of passive components such as surge arrestors or voltage suppressors to mitigate any sporadic voltage disturbances. It is evident that the inverter is permanently connected to the load. This ensures quick to nearly instantaneous restoration of power to the load upon the occurrence of a power outage by the utility. When the power supply is sustained by the utility, the inverter operates as an AC-DC converter, actively rectifying the AC power to charge the storage batteries. Operating the converter in this manner ensures that smooth sinusoidal current is drawn from the utility. The power flow during this mode of operation is usually 10% of the maximum capability of the converter [11]. This ensures the converter temperature is kept low enough for long duration operation. According to [11] a subtle but important aspect of a line-interactive UPS is that while it conditions the voltage supplied to the load, it does not alter the wave shape of the current drawn by the load. This topology also ensures the continuous regulation of the voltage supplied to the load. When an over- or under-voltage condition is experienced by the load, the UPS is able to change the flow of power to

the load from the batteries via the inverter. In conjunction with the power supplied by the utility, this eliminates single-point failure and thus guarantees two independent power paths [12].

In conclusion, the line-interactive UPS topology provides sustained power to load upon the event that the utility supply fails. The sustained power is ensured by utilising only one converter which implies a reduced cost and complexity when compared with the double-conversion UPS topology.

1.4 Problem Statement

The ultimate goal of the closed-loop controller in UPS applications is to control the transient behaviour of the output signal effectively. The aim is to achieve sinusoidal output transient behaviour. The controller might be unable to achieve this sinusoidal waveform effectively, due to discrepancy between the actual condition of the system and how the controller perceives the system to be.

One, among many, of these discrepancies may be the incorrect or inaccurate modelling of the system. Inaccurate modelling can make the difference between the control of a single three-phase system and the control of three independent single-phase systems. These systems have their similarities, but there are definitive behavioural differences. For example, the model for a single three-phase system will be different than three single-phase systems, because the three phases are dependent on each other in a single three-phase system. This is however not always the case with three single-phase system. It is possible to independently operated the three phases. There are cases in the single three-phase system when the three phases can be operated independently from each other and will be further discussed in section 3.2 where the Park transform can provide a means on independent operation for balanced systems.

Inaccurate circuitry used for the measurement of the voltages and currents can also degrade the controller's performance. Additionally, the performance of the analogue-to-digital (ADC) can also greatly affect the controller performance, since this produces the digital representation of the analogue signal used by the controller. An error made in either of these systems will result in incorrect signals being fed back to the controller and consequently resulting in an inaccurately controlled system. This is the case for all digitally implemented closed-loop control systems.

The above-mentioned discrepancies have to be kept in mind when a digital closed-loop control system is designed. To achieve the best possible controller performance, these systems have to be analysed in an attempt to reduce the negative effect they have on the system as a whole. Additionally, the design and implementation of a closed-loop control strategy that will be capable of providing sufficient performance under all load conditions, needs to be investigated.

1.5 Thesis Objective

The objective of this thesis is to investigate the digital control of a line-interactive UPS. Firstly, the sources that cause degradation of the controller performance are identified. Due to the quantifiable effect that the data acquisition system has on the controller and its performance, it is deemed necessary to make an in-depth analysis of each respective degrading component. The manners in which voltages and currents can be acquired are examined and the best options for line-interactive UPS applications being identified. Additionally, the candidates for the electronic measurement of the voltages and currents are identified. Their advantages and disadvantages will be discussed resulting in the optimal choice of measurement circuit for the applicable UPS topology. The influences of environmental conditions like EMI, ground loops and other sources of noise are identified, discussed and recommendations are made on how to minimise the susceptibility to these noise sources. Furthermore, numerous analogue-to-digital methods are considered with the aim of concluding which method will result in the best performance of the controller. Likewise, the various switching schemes are examined and an optimal combination of ADC and switching scheme is chosen.

Secondly, an investigation is done on digital control strategies. The emphasis of this thesis is on the regulation of the voltage produced by the line-interactive UPS. Ohmic law states that the current through a load is directly proportional to the potential difference across the terminals of that load. Consequently, current control strategies are also further examined to achieve higher voltage regulation performance.

1.6 Structure of this Thesis

In this chapter the main contributors that corrupt the quality of the voltage supplied by a national utility, was mentioned. A few methods were mentioned that are used to mitigate some of these voltage pollutants. The UPS was introduced as a means of providing uninterrupted voltage supply to a load in the case of the utility supply failing. In this chapter the predominant topologies used in UPS systems, were listed and their classification according to the international IEC 62040-3 regulation [9] was discussed. The problem statement was given and it was identified that the focus of this thesis is on the control of the voltage supplied by the UPS. It was also mentioned that a digital controller is required to achieve sufficient control of voltage.

In chapter 2 the development and design of the analogue circuits and electronics that are used to enable the implementation of the control strategies incorporated into the digital controller, is discussed. The control hardware requires numerous voltages. Common sources of noise and the compromises the system's noise immunity are identified. A power supply structure is subsequently developed that is the least susceptible to environmental noise and electromagnetically induced disturbances. A study is made of different measurement topologies where each topology's advantages and disadvantages are discussed. The most

popular ADC architectures are furthermore also discussed in chapter 2, since the ADC can greatly influence the accuracy of the digital controller.

The switching converter in the line-interactive UPS functions both as an AC-DC converter and a DC-AC converter. In chapter 3 a dead-time compensation scheme that are common to both the AC-DC and DC-AC converters are discussed. The discussed theory includes the discussion and derivation of the Park and Clarke transformations. In the subsequent chapters 4 and 5 uses all the material discussed in chapter 3 and the dead-time compensation scheme are employed along with all the control schemes derived in these chapters. A literature study on the different control topologies and types is also supplied.

In chapter 4 a closed-loop control scheme to control the inductor current when the line-interactive UPS operates in standby mode is provided. It is during this mode that the utility supplies power to the load and the UPS charges its storage batteries. A regulation algorithm is also derived to regulate the DC-link during this mode of operation.

When the utility supply fails the UPS system supplies power to the load from the storage batteries. In chapter 5 a model of the UPS system that is used in the subsequent design of the current- and voltage controllers, is derived. Two closed-loop current controllers for regulating the inductor current during this mode of operation are discussed and several voltage control algorithms are also developed and further discussed. The necessary literature study required for the derivation of the controllers is incorporated in this chapter. Simulations are done and the results are analysed to gauge the controllers' capability.

In chapter 6 an experimental investigation into the performance of the voltage controllers developed in chapter 5, is provided. Each voltage controller's performance is evaluated and compared with the requirements set out by the national NRS 048 regulation [13].

CHAPTER 2

DEVELOPMENT OF THE CONTROL HARDWARE

2 DEVELOPMENT OF THE CONTROL HARDWARE

2.1 Introduction

To be capable of digitally controlling a line-interactive UPS, a central controller is required. The controller must be able to sense the current operating status of the UPS system and also provide closed-loop control of both the currents and voltages in the unit. The control schemes described in the subsequent chapters can then be implemented in the digital system.

In this chapter the development of the digital central controller of the UPS system is discussed. At the core of the controller is a digital signal processor (DSP). A very important attribute of the DSP is its floating-point arithmetic-logic-unit (ALU). The floating-point ALU opens the door to the implementation of several control schemes that were not possible with fixed-point ALUs. A floating-point ALU is capable of computing several complex calculations at a much faster rate than a fixed-point ALU. Calculations are done synchronously on the DSP. It is therefore important that all calculations need to be executed before the next calculation cycle commences. The advantage gained from having a floating-point ALU at your disposal is that more complex calculation can now be implemented without the concern that their execution will overrun to the next calculation cycle.

A study is also done on the several means of improving the digital control capability of the system. It was found that the means by which the digital system acquires the analogue signals of a UPS system can be a source of numerous anomalies and disturbances.

These sources of disturbances range from the circuitry used for the measurement and conditioning of analogue signals to the digitisation of these signals. A study on most of the methods whereby the quality and performance of the digital controller can be improved is also provided.

The DSP will not only be used for the closed-loop control of the system's voltages and currents but will also be capable of controlling the system as a whole. The various components that make up the controller will be discussed and it will be explained how each contributes to achieving control of the system. Additionally, the DSP provides a means of communicating with a human-machine-interface (HMI) through a simple RS232 protocol and is even be able to log all relevant data on a non-volatile memory unit such as a Secure-Digital (SD)-card.

2.2 Analogue-to-Digital Converter

It is evident that to achieve effective and accurate control of the UPS voltages and currents, it is imperative to have a very accurate measurement of a signal at the exact time instant that the controller requires that signal. In the case where a controller is digitally-based the analogue-to-digital converter (ADC) is required to reproduce a digital representation of the analogue measurement. However, due to real-world irregularities and the fact that every operation has a finite duration, it is not possible to acquire this digital representation instantaneously.

The functionality and operation of the ADC process therefore needs to be investigated to determine the best ADC solution that will ensure optimal performance of the digital central controller. Figure 2-1 depicts typical closed-loop control topology and shows that the emphasis of this section is on the discretisation of the analogue signals of a system.

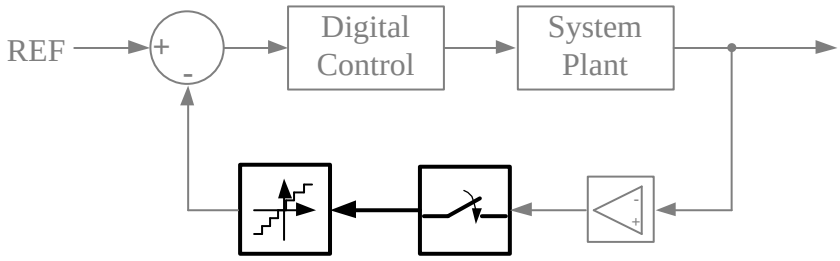

Figure 2-1: Focus on Discretisation of Analogue Signals

As the name implies, an ADC is a component which serves the function of converting an analogue signal to a numerically equivalent digital value. There are different techniques according to which this conversion is done, each having its respective advantages and drawbacks. For example, a certain technique will provide a high sampling rate but at the expense of accuracy. It is therefore important at least to possess a basic understanding of the ADC and the operation of the different conversion techniques to determine how to obtain a digital representation of the analogue signals in the UPS system.

2.2.1 Basic Operation

The greater majority of ADCs are based on the same generic structure. This structure can be considered in Figure 2-2, where the analogue signal is acquired by means of a sampling circuit, which is subsequently used by a comparator optimised for ADC purposes to obtain a digital equivalent of the sampled analogue signal. Thereafter, the data is processed depending upon the type of architecture on which the ADC is based. As can be seen, there is a logical flow between these processes. These processes will forthwith discussed briefly.

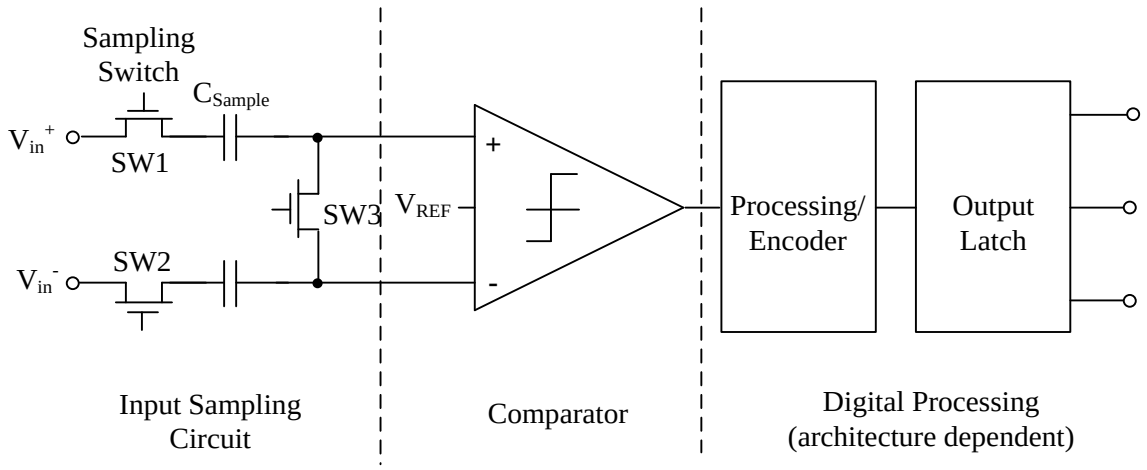

Figure 2-2: Generic ADC Structure

Input Sampling Circuit

This portion of the ADC, in conjunction with the accompanying comparator, in essence serves as the sample-and-hold amplifier (SHA) of the ADC. The structure of the input sampling circuit varies in complexity depending on the architecture in which it is utilised. For example, an additional resistor may be included in series with the sampling capacitor C_{sample} to control the rate at which this capacitor is charged. It is important to note that the source of the analogue signal must be able to charge this capacitor to a settling level accurate to the bit-resolution of the ADC, e.g. for an ADC with a 12-bit resolution and an analogue input range of 5 V, this capacitor must be charged to an accuracy settling level of 1.22 mV. This level is obtained by using equation (2.1):

$$V_{LSB} = \frac{V_{FSB}}{s^N} \tag{2.1}$$

with V_{LSB} being the equivalent voltage of the Least-Significant-Bit, V_{FSB} being the analogue full-scale voltage range of the ADC and N indicating the bit-resolution of the ADC. It is also common in the design of modern ADCs to include additional functionality to the ADC. For instance, it is highly desirable to reduce the effects of noise in the resulting digital value produced by the ADC. Noise will have a tremendously adverse effect on the input sampling circuit and it is desirable to include additional noise filters in the circuit.

The input sampling circuit has two functional modes: sample-mode and hold-mode. The sample-mode is the acquisition phase where the analogue signal is obtained. During this mode, the solid-state based switches SW1, SW2 and SW3 are closed, resulting in the series connecting and consequent charging of the sampling capacitors. During the hold-mode, the conversion phase is initiated where all the switches are open and the comparator measures the differential voltage at its input. This differential voltage is held stable by the sampling capacitors for the duration of the conversion phase. A general design habit is to place an additional capacitor on the input of the ADC to facilitate the sampling of the analogue signals and improve the dynamic performance of the ADC.

As distinguished by [14], the structure of the input sampling circuit is categorised as having either a single-ended, pseudo-differential or fully-differential structure. Sections 2.3.1 to 2.3.3 provide a brief discussion of these different structures.

Comparator

The analogue-to-digital conversion process is not possible without the aid of a comparator. It is here that the analogue signal is converted to a digital format. This makes the comparator an integral part of the ADC and closer attention to its operation in the analogue-to-digital conversion process is therefore merited.

The basic function of a comparator is to produce a logic output signal based on its differential input. In ADC applications, the comparator compares this differential input with a reference voltage, which can be generated internally or provided by an external reference circuit. A common problem experienced with the comparator is that the output tends to oscillate when the differential input magnitude is very close to the reference voltage. The comparator is subsequently unable to produce a definitive logic output state. According to Kester in [15] the comparator is then in a so-called “metastable” state. This oscillation will eventually settle, but will result in the corruption of the converted value for that instant in time.

These oscillations cause errors that are known as “sparkle codes” and account - to a small extent - for the quantisation errors experienced with ADCs in general. The comparator is designed with a small hysteresis band at the threshold between logic states to prevent instability in the transition region and to counteract this oscillatory operation. Comparators used in ADC applications additionally utilise a built-in latch at the input of the comparator which improves their performance as sampling devices.

The latch at the input of the comparator locks the output in the logic state it was in at the instant it was enabled, allowing the sampling of very short duration analogue signals, and holds the signals for further processing. Due to the fact that the latching occurs on the input signal of the comparator, this ensures miniscule sampling delay. Since the output of the comparator is determined by not only the differential signal provided by the input sampling circuit but also on the reference voltage, it is evident that this reference voltage must be as accurate and devoid of noise as much as possible. Any disturbances on either the differential input or the reference voltage will result in the irrecoverable corruption of the signal used in the digital processing portion of the ADC.

Digital Processing

The analogue signal that was sampled by the input sampling circuit and thereafter discretised by the comparator needs to be interpreted and processed into a usable digital format such as a binary code or twos complement code. This is done in the digital processing portion of the ADC and directly determines the major characteristics of the ADC. Characteristics such as the sampling rate, throughput rate, accuracy,

latency and even power consumption. Due to the vast different techniques of digital processing, the ADC family has been divided into different architectures. In other words, the architecture of an ADC determines the manner in which the data is processed. The architecture of an ADC not only determines the digital processing technique, but also branches out to the other portions of the ADC structure. The structure of the input sampling circuit can differ from one architecture to another. Furthermore, the architecture even determines whether only one comparator is used in an ADC or numerous comparators are utilised to facilitate parallel processing.

There are numerous ADC architectures. The following architectures will be considered in this study:

- Direct Conversion or Flash
- Pipelined Sub-Ranging
- SAR

The motivation for only considering these architectures is the fact that these are the most commonly used in power electronic applications. Most other architectures are either based on one of the above-mentioned or are hybrids between the above architectures.

2.2.2 ADC Architectures

To change the technique an analogue signal is converted, the manner in which the different sub-components are arranged and how they interact with each other need to be changed physically. These differently organised layouts are called ADC architectures. These architectures are further investigated in the subsequent sub-sections.

2.2.2.1 Direct Conversion/ Flash

This architecture is commonly known as the flash architecture but is also called the parallel [16] or the direct conversion architecture [17], because this architecture directly converts the analogue signal to a digital value. It does not utilise complex manipulations and techniques to convert the analogue signal. This architecture is based on the cascaded arrangement of a vast number of comparators that are optimised for ADC applications as discussed in section 2.2.1.

As seen in Figure 2-3, these comparators are used for the analysis of a certain portion of the analogue signal. For an N-bit converter there are $(2^N - 1)$ comparators and a resistive-divider string consisting of 2^N resistors provides the reference voltage for each comparators.

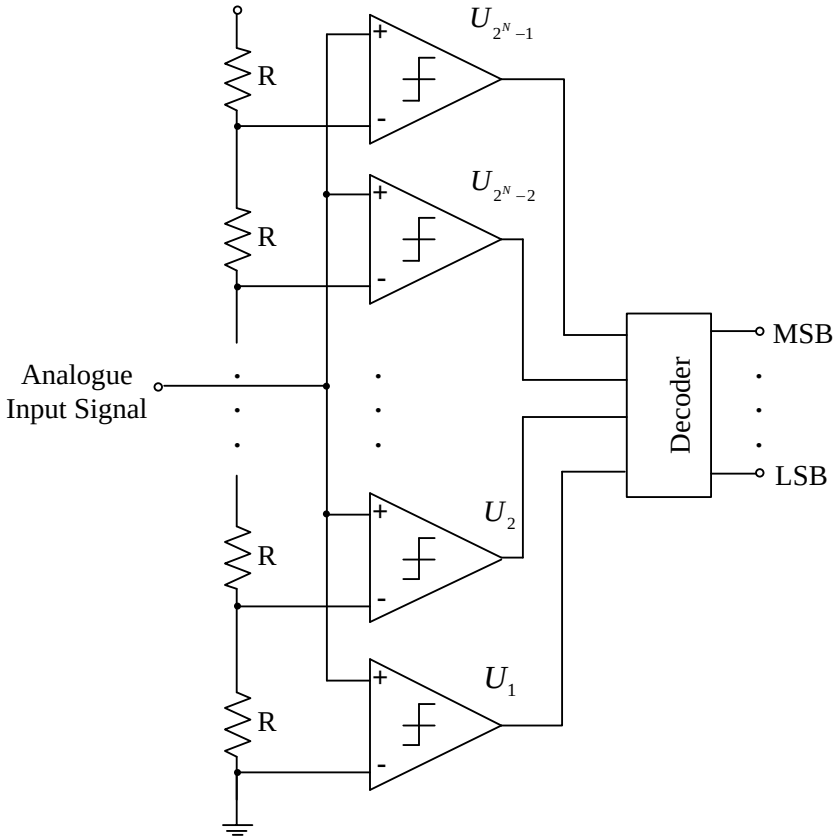

Figure 2-3: Flash Architecture Structure

The reference voltage for each comparator is 1 LSB (determine with equation (2.1)) greater than the reference voltage of the comparator immediately below it. The comparators, subsequently produce output codes which are processed and latched out as a binary numeral. Due to the high parallelism provided by the flash architecture, it is capable of extremely high sampling rates. With an increase in sampling rate, the power dissipation likewise increases. It is discernable that with an increase in bit resolution the number of comparators and resistors greatly increase. This results in an increase of die real-estate and also much higher power usage. It is due to these rapid increases that flash architectures based ADC are constrained to applications requiring relatively low bit resolution but that still necessitate high sampling rates.

However, the flash architecture is still the fastest ADC architecture on the market, capable of achieving sampling rates in the Giga-samples per second range [15]. It is thanks to this great speed that the flash-architecture serves as the stepping-stone for the development of the modern pipelined sub-ranging architecture.

2.2.2.2 Pipelined Sub-Ranging

Also known as sub-ranging quantisers [17], the pipelined architecture takes over where the flash architecture is unable to deliver. This architecture has the same advantage as the flash architecture in that it is capable of very high sampling rates, but does not have the drawbacks associated with the flash architecture. Admittedly,

the flash architecture provides extremely high sampling rates but it comes at the price of low resolution and high power consumption. The pipelined architecture does not have these drawbacks. On the contrary, ADCs based on the pipelined architecture are capable of high bit resolutions (12-bit to even 24-bit) along with similarly flash-equivalently high sampling rates (100 MSPS and more) at relatively low to moderate power dissipation (≈400 mW). Note that there is an inversely proportional relationship, albeit a weak relationship, between the resolution and the sampling rate of a pipeline-based ADC. In other words, with a drastic increase in resolution accuracy, the sampling rate capability of the ADC will slightly decrease. Still, how this architecture achieves all of these phenomenal advantages is based on its unique approach to parallel processing of the analogue signal.

The term pipeline is coined by [18] as the ability of one stage to process data from the previous stage during any given phase of the sampling clock cycle. The alias of this architecture, sub-ranging, more clearly defines this architecture as dividing the input signal into a number of smaller ranges (sub-ranges) which are, in turn, further subdivided [18]. In other words, the design is based on dividing the sampling of the analogue signal across multiple stages with each stage employing a flash ADC to convert a certain bit-range part of the input signal. This is shown in Figure 2-4, where, for illustrative purposes, a pipelined structure for a 12-bit ADC is employed. As seen in this figure, the conversion process starts with the input signal being converted in Stage 1.

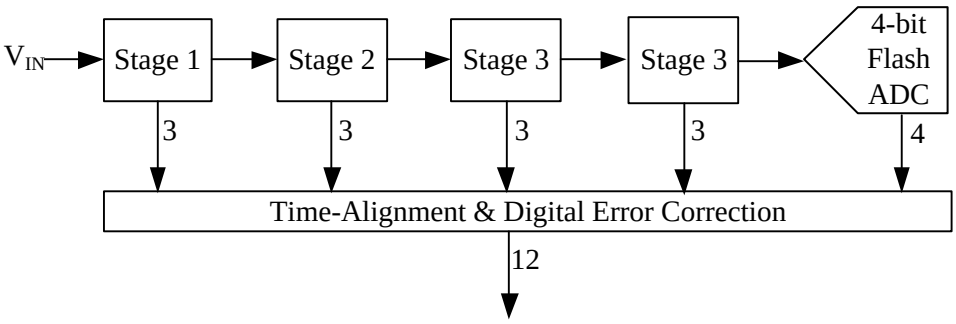

Figure 2-4: Pipeline Architecture Overview

A single stage is depicted in Figure 2-5 and shows how a pipelined architecture utilises the flash ADCs consequently ensuring high sample- and throughput-rates in a 12-bit ADC. Every stage samples the analogue signal accurate to, say, 3-bit accuracy which is converted with a digital-to-analogue converter (DAC) back to an analogue signal which is accurate to 12-bit resolution. This is subtracted for the original sample with the purpose of determining the error made during the conversion process. This error is subsequently gained by a factor of, in this case, 4 and sent to the following stage where the same process will be executed. It is important to note that the different stage can be different bit-resolution ADC. This process is repeated depending on the design choices of the manufacturer, until finally at the last stage the residue from the preceding stages are converted by an ADC with a slightly higher resolution accuracy.

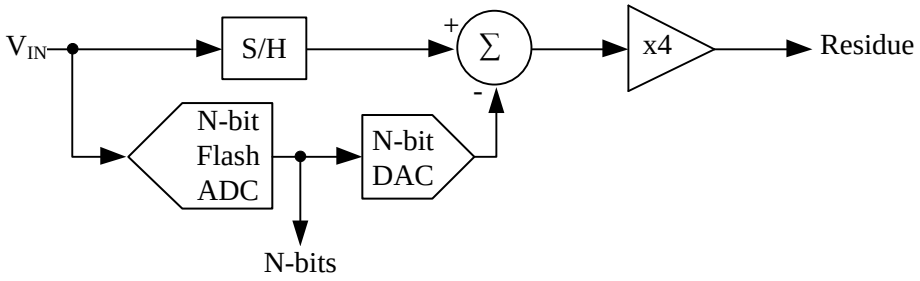

Figure 2-5: Single-Stage Pipeline Diagram

The capability of the pipelined architecture to achieve parallel conversion of numerous samples is thanks to the property of each stage to commence with the next available sample immediately once it has completed quantisation of the sample it has currently been busy with. This parallelism yields high sampling rates and great throughput rates in the pipelined architecture [19].

To produce a digital output which is accurate to the bit-resolution of the specific ADC it is necessary to time-align the converted results from each respective stage. This is achieved by using a sample-and-hold to store the data from each stage in shift registers. In conjunction to the time-alignment between the different stages, the output from a preceding stage is also adjusted to ensure optimal alignment for utilisation of the succeeding stage. This is achieved by amplifying the residue signal (see Figure 2-5) produced by the preceding stage. The aim of this amplification is to ensure that the analogue signal produced by the DAC from the preceding stage occupies the full-scale of the analogue input range for the following stage. Finally, a digital error correction algorithm is employed to correct for errors due to misalignment between the stages [19]. Such a misalignment is depicted in Figure 2-6 in the case when a ramp analogue signal is input to the ADC. This misalignment occasionally occurs when the residue signal is larger than expected, resulting in the analogue signal input to the following stage being larger than the maximum analogue range of that stage. The ADC is subsequently unable to produce a digitally equivalent value, which gives rise to the missing codes shown in Figure 2-6.

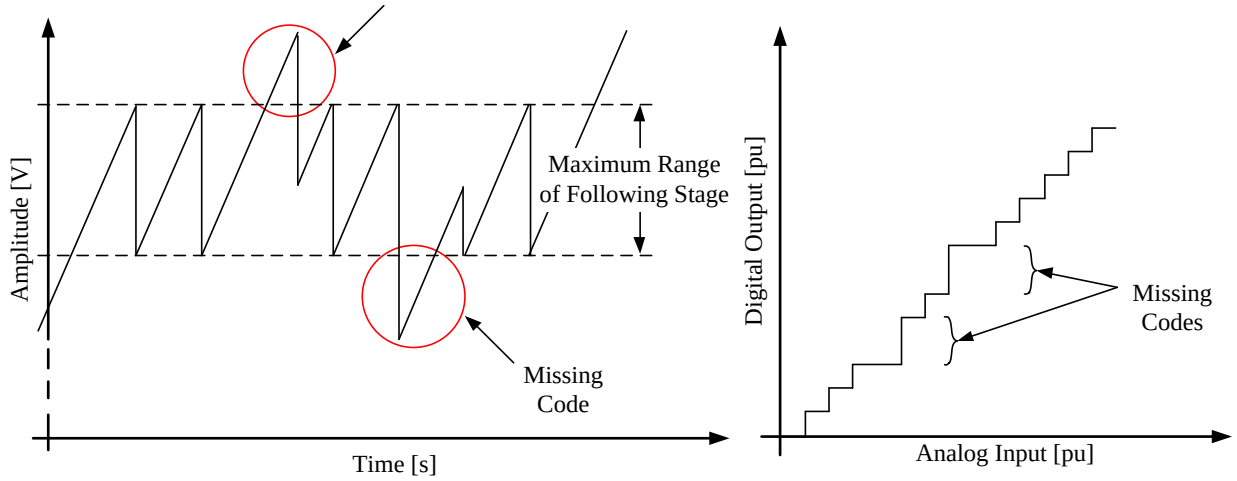

Figure 2-6: Illustrating Inter-Stage Misalignment

Any errors made due to the abovementioned misalignment are however corrected with a digital error correction algorithm by adding extra quantisation levels in the region where the residue signal has exceeded the maximum analogue range.

This necessity to ensure optimal alignment in time and alignment of the signal amplitudes gives rise to the delay in the production of the final digital output. This delay is known as latency (or pipeline delay) and is one of the main characteristics for which this architecture is notorious. Figure 2-7 illustrates this latency making it clear that the digital output of the ADC is time delayed with respect to the analogue signal it is sampling. The sample-and-hold used between stages to achieve time-alignment of the respective digital results operates on the sampling clock of the ADC. The latency thus is a function of the number of stages employed in the ADC and the cycle duration of the sampling clock. Consequently, the latency is always defined as an integer multiple (which is determined by the number of stages) of the sample clock duration. It is therefore clear to see that the latency can be reduced by either reducing the number of stages employed in the ADC or by greatly increasing the sampling clock rate.

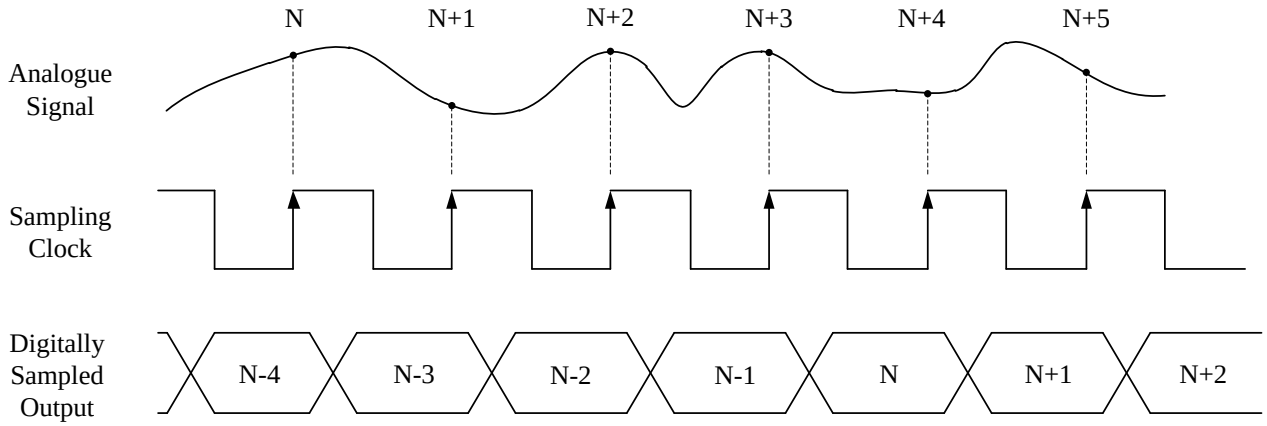

Figure 2-7: Illustrating Pipelined Latency

As discussed at the beginning of this section, the goal is to reduce the conversion duration of the ADC and conclusively it is clear that the pipelined architecture is able to produce the required high sampling rate. This architecture is nonetheless too fast for the current DSP currently being used. There is also not a way of effectively synchronising the measured values with the rest of the system. If the DSP is used to drive the ADC, the current DSP technology limits the capability of the DSP to produce a sampling clock that operates at such high frequencies.

Synchronisation between the DSP and the ADC is therefore very difficult and even impossible. DSP technology only recently progressed to the point where synchronisation at moderately high frequencies can become possible, but the DSP used in this project does not have that capability.

The utilisation of an ADC with such high sampling rates is generally unnecessary in typical power electronic applications. The switching frequency of the converter is usually at a low frequency (in the range of a few kilohertz) relative to the sampling frequency of pipelined ADCs. Sampling at such high frequencies would only seem viable if oversampling of the signals need to be employed.

2.2.2.3 Successive Approximation Register (SAR)

This architecture employs a conversion technique which is also known as the bit-weighing conversion technique. The general structure of the SAR architecture can be seen in Figure 2-8 and it can be seen that it employs only a single comparator.

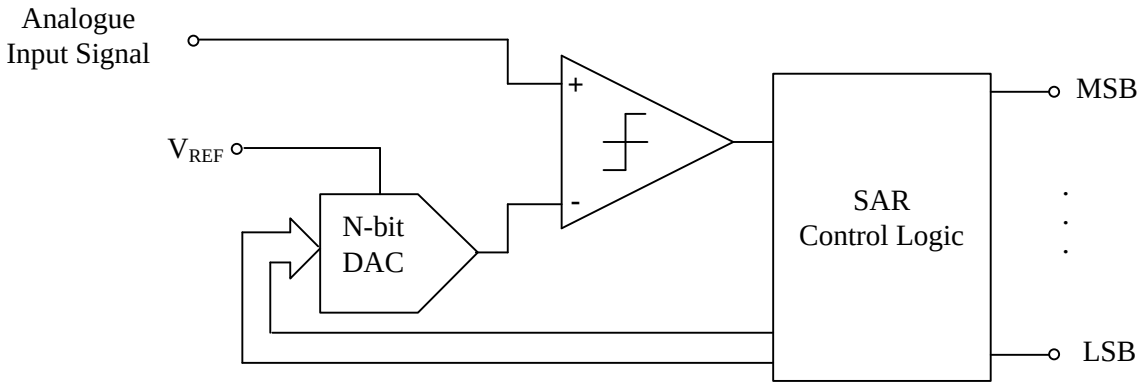

Figure 2-8: Basic SAR Structure

Employing only a single comparator greatly reduces the overall complexity and component count of ADCs based on this architecture. Another advantage is that there is very low power dissipation and that only a small amount of real-estate is used on the die. The method of conversion employs a binary search algorithm by comparing the analogue signal with a signal produced by an N-bit DAC [17]. The signal produced by the DAC is determined by the reference voltage, V_{REF}, and the commands received from the SAR control logic. It is common practice to use a capacitive-DAC [20] because it has an inherent track-and-hold functionality. As explained by [20], [21] and [22], the capacitive DAC employs an array of N capacitors, with each capacitor having a binary weighted, ie $C, \frac{C}{2}, \ldots, \frac{C}{2^N - 1}$ capacitance values with N being the bit resolution of the ADC. The use of capacitors enables the utilisation of charge redistribution in the conversion process and has the added advantage of providing more precise matching of the component values.

The conversion process is illustrated in Figure 2-10, which shows a typical capacitive DAC utilising a capacitor array to apply the principle of charge redistribution. When the analogue signal is acquired, the inverting input terminal of the comparator is connected to ground and all N capacitors are connected to the analogue input signal. After this acquisition phase, the inverting input is disconnected from ground and all the capacitors are disconnected from the analogue input. This effectively captures a charge in the capacitor

array which is proportional to the analogue input, V_{IN}. Thereafter, the capacitor array is connected to ground, resulting in the non-inverting input of the comparator being biased at $-V_{IN}$. The binary search algorithm commences by disconnecting the capacitor that represents the MSB, from ground and connecting it to V_{REF}, leading to the non-inverting input being driven positive by a voltage of $\frac{V_{REF}}{2}$. In other words, if $V_{IN} = -0.6V_{REF}$, then the connection of the MSB capacitor will drive the non-inverting input of the comparator to $(-0.6V_{REF} + 0.5V_{REF}) = -0.1V_{REF}$. This voltage is subsequently compared with the inverting input of the comparator (which is connected to ground) and produces a logic high, thus implying that the MSB represents a value that is larger than $\frac{V_{REF}}{2}$. This process is repeated, this time disconnecting the second largest capacitor in the array, which has a binary weight as previously mentioned, i.e half the capacitance of the largest capacitor. A similar comparison is done which determines the logic value of the second-most-significant-bit (MSB – 1). This continues until logic values for all the bits have been determined, after which the ADC is ready to compensate with the conversion of another analogue signal.

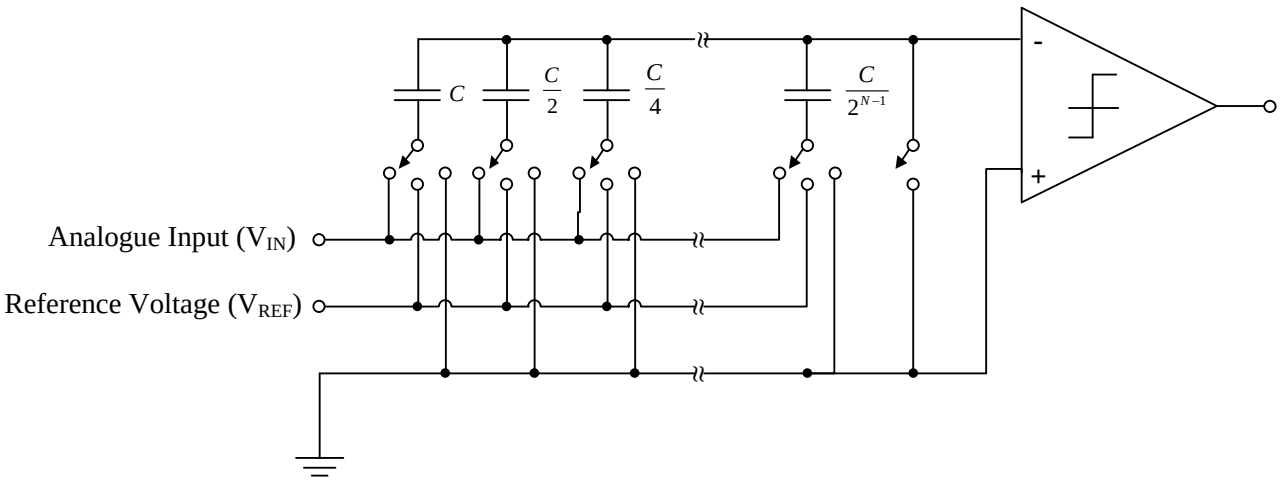

Figure 2-9: Capacitive DAC based on Charge Redistribution

An example of a conversion process can be seen in Figure 2-10 which shows how the DAC output voltage approximates the sampled analogue input signal by successively comparing the weight of each bit with the reference voltage.

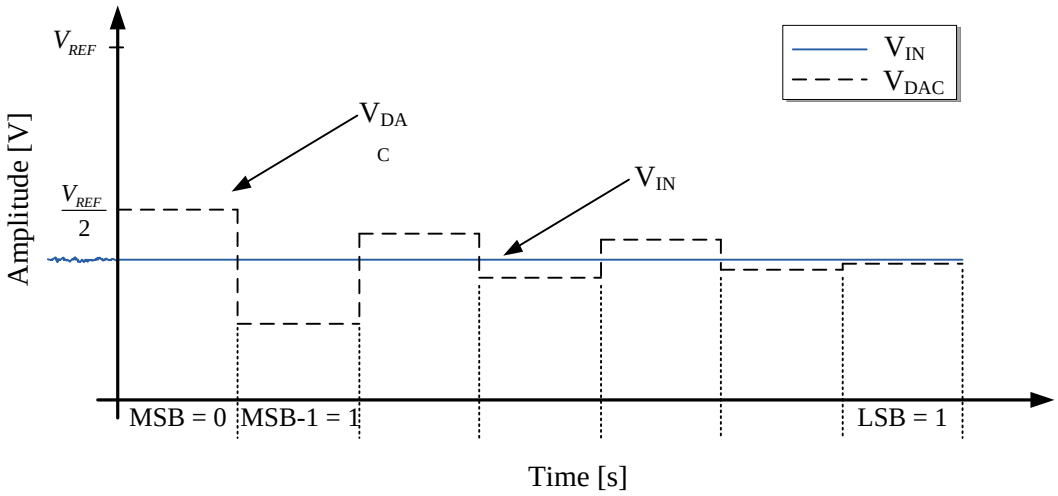

Figure 2-10: SAR Operation

Each comparison operation has a duration of one sample clock cycle. Therefore, the conversion time is directly proportional to the bit-resolution of the ADC and the sampling clock cycle duration, i.e at least 12 clock cycles are required to convert an analogue signal to a digital equivalent, accurate to 12-bits.

Establishing closed-loop control requires that the output telemetry be fed back to the central controller. This implies that the measurements fed back to the controller need to be synchronised with the reference signal. It is therefore required to control the instant when an analogue signal is converted to its equivalent digital code. This instant can be controlled in the SAR-based ADC, meaning that the data produced by the ADC can be synchronised with the central controller, whereas the pipeline-based ADC continuously converts the analogue signal and additional means are required to synchronise the controller with the data. ADCs based on the SAR architecture are the most popular general-purpose ADCs for data acquisition in low-to-medium frequency time domain applications.

2.3 Data Acquisition Solutions

The voltages and currents in common UPS systems usually have large amplitudes. It is thus not possible to connect these signals to an ADC directly, since it will most obviously permanently damage the ADC. For this reason it is required to recondition the high amplitude signals so that they can be compatible with the analogue input specifications of the ADC. It is therefore necessary to investigate the different measurement and signal conditioning schemes. Figure 2-11 depicts a typical closed-loop control topology and points out where the emphasis of this section lies.

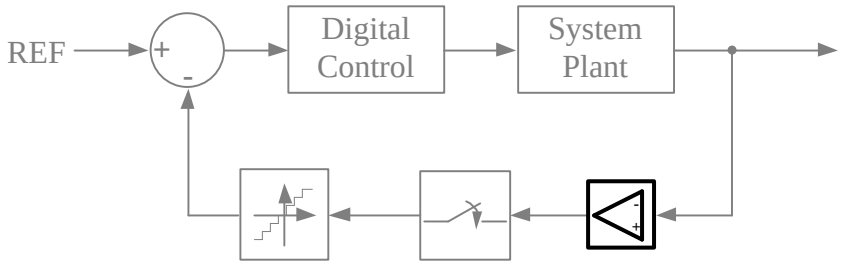

Figure 2-11: Focus on Signal Measurement and Conditioning

There are predominantly three measurement structures. These are the single-ended, fully-differential and pseudo-differential structures.

2.3.1 Single-Ended

This is the most elementary structure, yet it is sufficient for most applications where noise susceptibility is not of strong concern. External signal conditioning circuits need to be used if this noise becomes a concern. A single-ended input structure does not provide any of the advantages of the other input structures such as increased CMRR and immunity to DC offsets.

In general, the input sampling circuit is identified as the portion of the ADC that is the most sensitive to noise and can thus greatly affect the accuracy of the ADC. As emphasised by [15], the input sampling circuit specifically enhances the dynamic performance of the comparator. It is therefore imperative to ensure that the input sampling structure operates under the best conditions to provide the most accurate, least noise-polluted signal to the comparator.

2.3.2 Fully-Differential

The fully-differential structure provides the best noise immunity properties, thus resulting in a higher signal-to-noise ratio (SNR) and also improves the common-mode rejection-ratio (CMRR) of the ADC. A dynamic analogue input range is an additional association with a fully-differential input structure. This is thanks to the two signals that comprise a differential signal pair being 180° out of phase with respect to each other, resulting in the effectual doubling of the analogue amplitude of the differential signal. Finally, the use of a fully-differential input structure means that a signal that is galvanically isolated can be applied to the ADC without the accompanying concern of whether the input signal is within the analogue input range of the ADC.

2.3.3 Pseudo-Differential

A typical application of pseudo-differential signals is for circuits that are biased at an arbitrary DC level with respect to the ADC reference ground. This type of input structure, similar to fully-differential structures,

separate the signal grounds by cancelling DC common-mode voltages, but does not provide increased CMRR.

2.4 Pulsewidth Modulation Schemes

Figure 2-12 shows that the emphasis of this section is on a typical closed-loop control strategy. Switching converters requires a means of translating the digitally-based reference signal to a realisable analogue signal on the output of the converter. Pulsewidth Modulation (PWM) is a well-established modulation scheme for the control of switching converters. The digital signal produced by the digital controller is modulated with the objective of reproducing the signal in the analogue domain. Black [23] defines PWM as the modulation of a pulse carrier in which the value of each instantaneous sample of a continuously varying modulating wave is caused to produce a pulse of proportional duration.

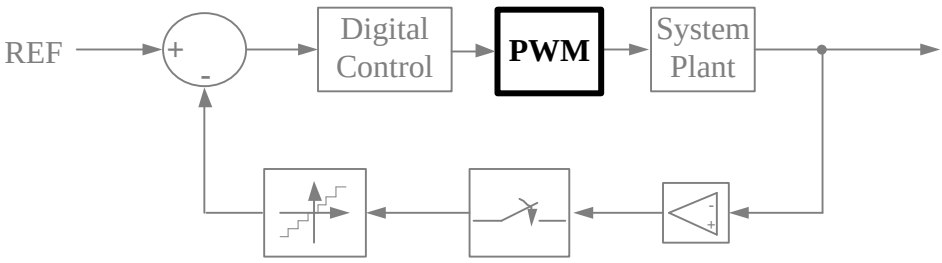

Figure 2-12: Focus on PWM Scheme

There are predominantly two categories in which modulation schemes in switching converters can be placed. The first is synchronised sinusoidal modulation which occurs when the switching frequency is an integer multiple of the fundamental output frequency. The effect is a definable placement of the fundamental message signal and the PWM carrier in the frequency spectrum. The second is when the switching frequency and fundamental frequency are independent of each other. The modulation scheme is called free-running sinusoidal modulation [24]. The frequency spectrum produced by the free-running sinusoidal modulation of a signal is much polluted. The switching frequency changes over a considerably large range which produces large frequency component within the whole range by which the frequency can change. The synchronised sinusoidal modulation scheme has the advantage of producing a less populated frequency spectrum. Unlike the synchronised sinusoidal modulation scheme however the free-running modulation scheme is capable of quickly mitigating tracking error at the expense of higher total-harmonic-distortion (THD).

Apart from the synchronised and free-running modulation schemes, PWM are characterised as being either symmetrical or asymmetrically based. The classification is determined by the wave type of the modulation carrier. PWM can be implemented by digital means and is called digital PWM (DPWM) or by analogue means which is called natural (or analogue) PWM (NPWM). The DPWM implementation has certain drawbacks when compared to NPWM, since the message signal stays constant of the switching cycle, but is

not of great concern in this study. The manner in which PWM is generated is not the focus in this section but rather the different schemes that are employed.

Figure 2-13 shows three modulation schemes that are predominantly used and also shows the generation thereof. It the modulation carrier is a saw tooth waveform with the fixed-edge being either leading or trailing the sloped edge, the modulation scheme is called Leading-edge PWM (LEPWM) or Trailing-Edge PWM (TEPWM) respectively. Modulation schemes using a saw tooth waveform and thus utilising only a single modulated edge are classified as Single-Edge PWM (SEPWM). On the other hand, if the modulation carrier is a triangular waveform, the scheme is called Double-Edge PWM (DEPWM).

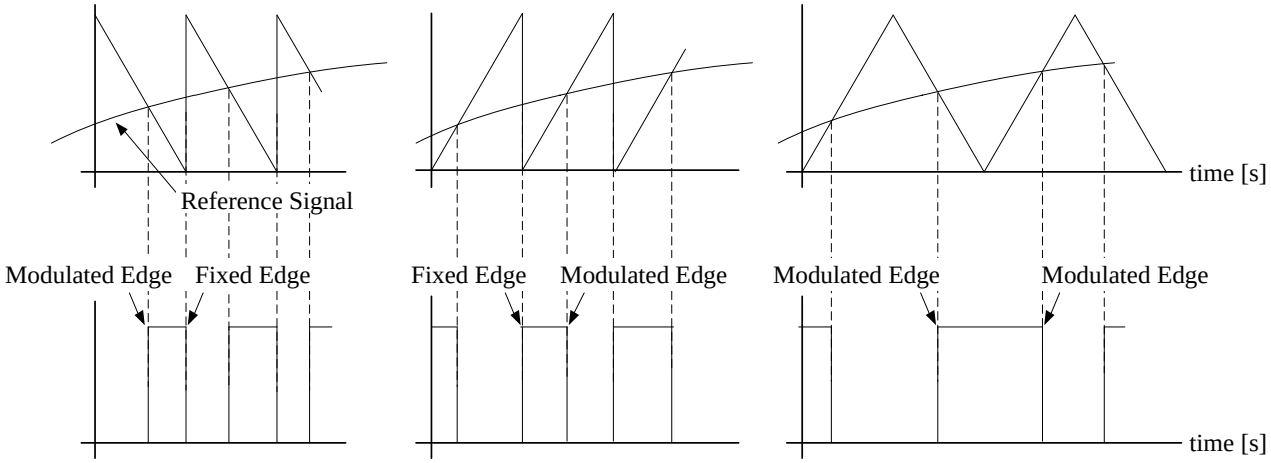

Figure 2-13: Generation of (a) LEPWM (b) TEPWM (c) DEPWM

Koeslag [25] did an analysis of the spectral characteristics of a signal that is modulated with LEPWM, TEPWM and DEPWM. It was found that TEPWM and LEPWM produce exactly the same magnitude spectra. More interesting is that DEPWM implementations produced fewer harmonics than SEPWM implementations. All even sideband harmonics around even multiples of the carrier frequency are eliminated. The odd sideband harmonics around odd multiples of the carrier frequency are also eliminated. Figure 2-14 shows the magnitude spectra of a 50 Hz signal that is modulated using a 5 kHz carrier with a unity modulation index. Figure 2-14 (a) shows the magnitude spectrum when DEPWM is used for the modulation of the signal, whereas Figure 2-14 (b) shows the spectrum of when SEPWM is used. Since [25] established that both LEPWM and TEPWM produce the same magnitude spectrum, it can be concluded that DEPWM produces a seemingly better magnitude spectrum that SEPWM. Figure 2-14 (a) shows a great deal less harmonic content than Figure 2-14 (b). It is important to point out that the magnitude spectra of both DEPWM and SEPWM signals at the fundamental frequency of 50 Hz is exactly the same. No sidebands are generated by either DEPWM or SEPWM. The purpose of showing the magnitude spectra over a frequency range of 2 kHz to 60 kHz is to depict the difference between the double-edge and single-edge modulated magnitude spectra across the higher frequencies.

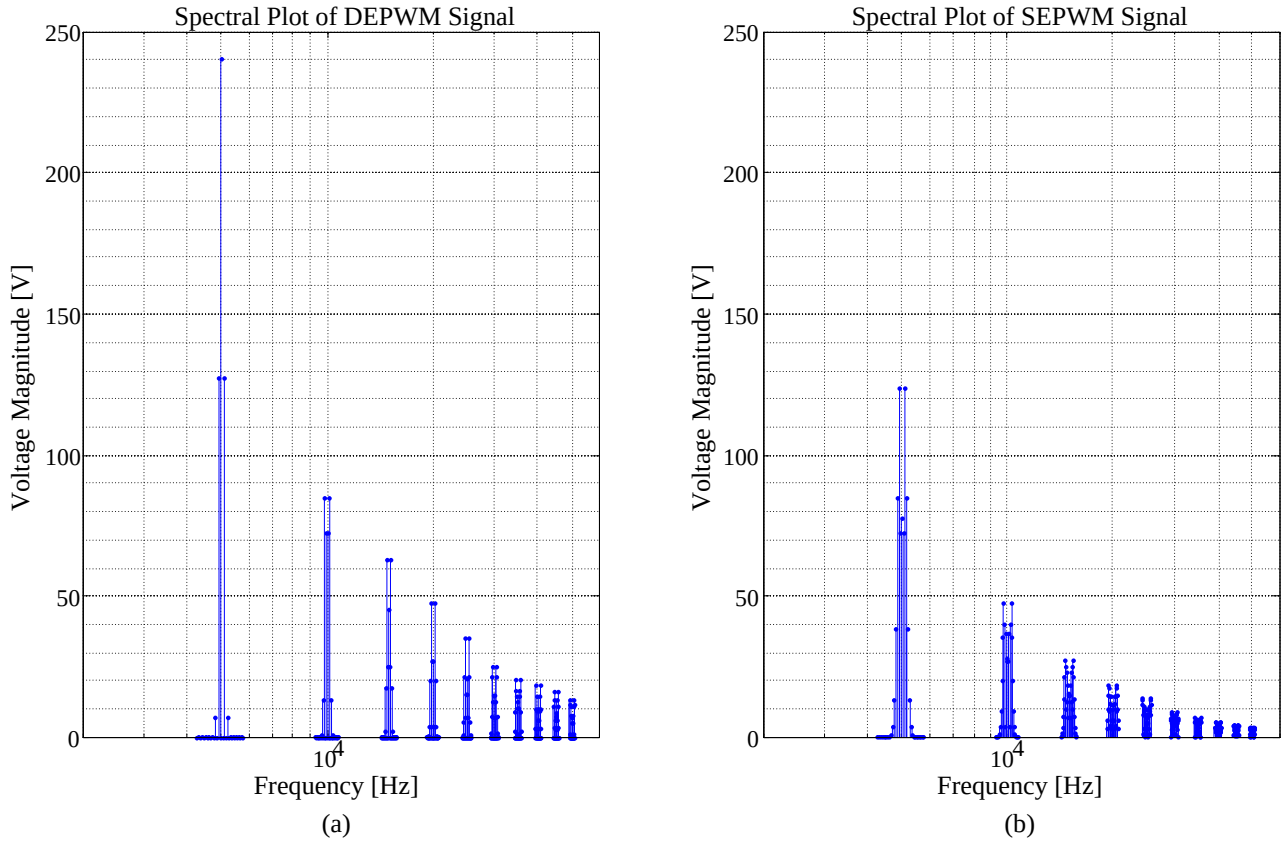

Figure 2-14: Magnitude Spectrum of Pulsewidth Modulated Signal

The greatly improved THD obtained from simply using DEPWM above SEPWM provides one of the motivations to use DEPWM in the line-interactive UPS. Another more fundamentally important advantage provided by the utilisation of DEPWM is that it provides a means of obtaining an average measurement of the system's voltages and currents.

Since the switching converter is at the lowest level controlled by the PWM, every electrical signal has a characteristic ripple that is proportional to the frequency of the modulation carrier. Shannon's theorem states that for an analogue signal $x(t)$ with a maximum frequency of F_{MAX} the sampling rate f_C at which that signal is sampled needs to be $f_C > 2F_{MAX}$ to ensure that the signal can be exactly recovered [26]. The minimum value of f_C is known as the Nyquist frequency. To be able to realise the signals in the system exactly, the Nyquist frequency needs to be twice the switching frequency to satisfy Shannon's theorem. In typical switching converters, the sampling frequency will be set to either the switching frequency or twice the switching frequency. This will however violate Shannon's Theorem. If however the sampling and switching frequencies are synchronised, this will result in the automatic reconstruction of the average value of the sampled signal. This is in fact exactly what is required, since the high-frequency ripple deviates around the average of that signal. It is this average signal that is controlled.

DEPWM produces a switching signal that is symmetrical around the peak of the modulation carrier. If the sampling rate is thus synchronised at the switching frequency such that the point of sampling coincides with the peak of the carrier, this will result in the effective sampling of the average of that signal at the beginning of that sampling period. This process is illustrated in Figure 2-15. The output inductor current is a typical signal that contains a definable ripple component that is proportional to the switching frequency of the system.

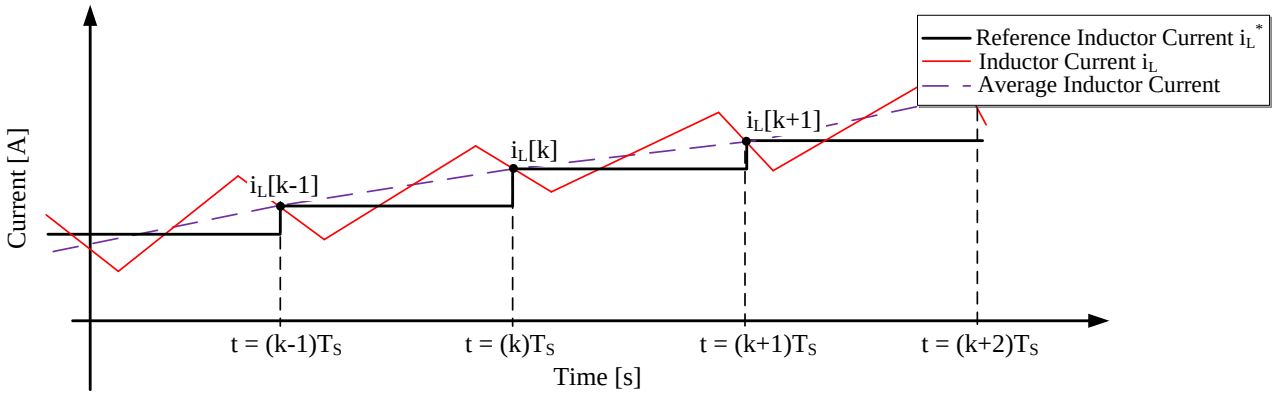

Figure 2-15: Synchronised Sampling of Switched Signal

Sampling the inductor current at the peak of the carrier will measure the average value of the inductor current during that switching period. It is shown that this average inductor current is exactly reconstructed and that the ripple component is disregarded.

In conclusion, DEPWM provides good THD in comparison with SEPWM. Its symmetrical characteristic provides the means of sampling the system signal to obtain an accurate representation of the average equivalent.

2.5 Overview of the Line-Interactive UPS

In section 1.3.3 it was shown that the line-interactive UPS topology contains a solid-state switch that connects the switching converter to and from the main utility. To realise this, two thyristors are connected in anti-parallel on each phase. Figure 2-16 gives a graphical overview of the line-interactive UPS system and how the digital controller is connected to establish full control of the UPS system.

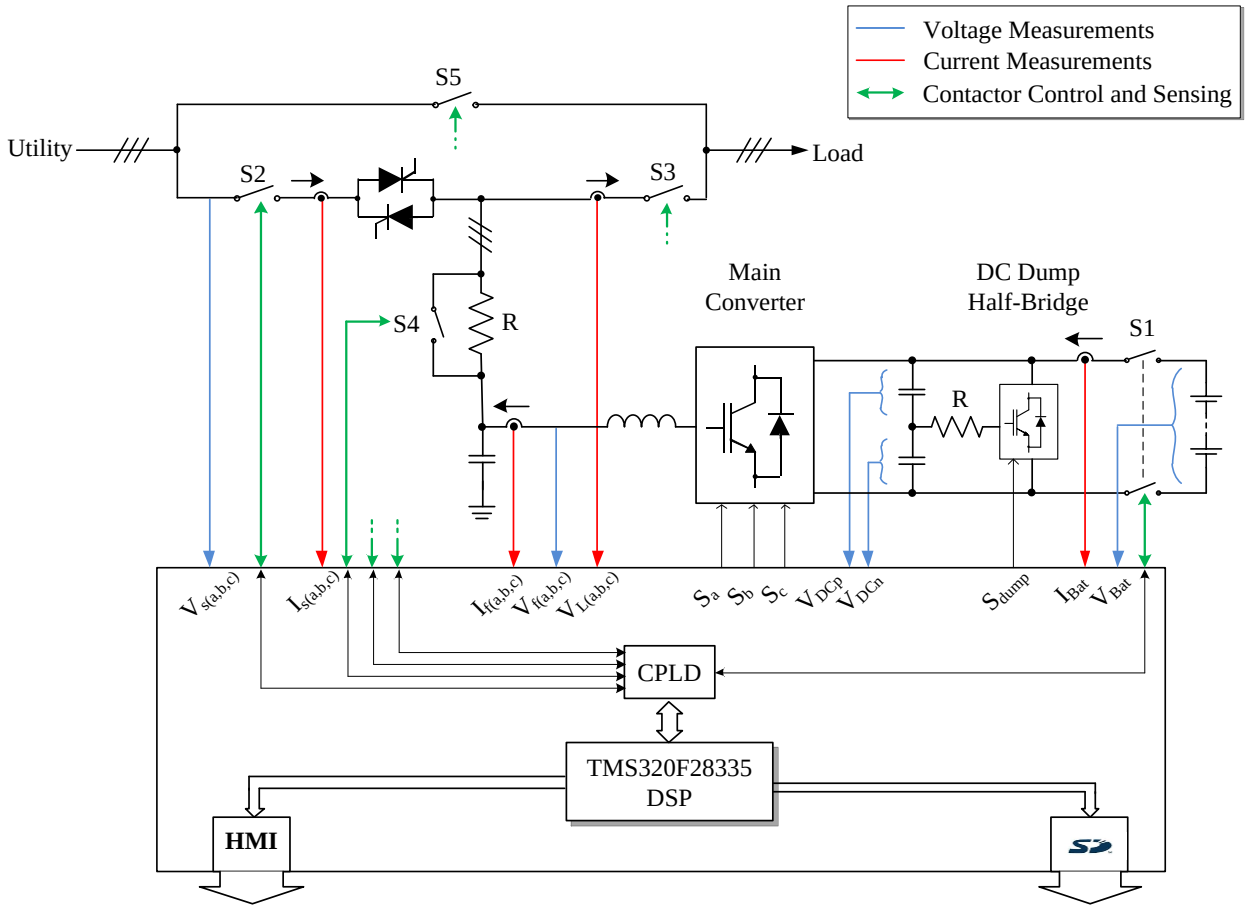

Figure 2-16: Line-Interactive UPS System Overview

It can be seen that the DSP is at the centre of the system, since all signal paths either originate or lead to the DSP. All contactors' and circuit breakers' status are sensed and controlled by the DSP via a complex programmable logic device (CPLD). The DSP directly controls the main converter to establish the control schemes that will be discussed in chapters 4 – 6. Additionally, the DSP controls a half-bridge converter leg that is used to dump the voltage on the DC-link in the case of an emergency. All voltage and current signals are measured and conditioned to be compatible with ADCs that are either internal to the DSP or externally implemented on the central controller.

The switching converter has dual functionality. During initial start-up of the line-interactive UPS, the converter is used to actively rectify the AC supply to match the DC-link's capacitor voltage and the battery voltage to ensure clean connection of the batteries. During normal operation, the converter is used to ensure power flow from the electric utility to keep the battery storage bank fully charged. When the utility supply fails the line-interactive UPS immediately starts converting power from the storage batteries to ensure uninterrupted power supply to the load.

2.6 Power Supply Consideration

The consideration of the power supply for the electronics of the system included whether or not to utilise isolated power. To comprehend the motivation for the use of any specific power supply topology fully, it is required to consider a few sources of problems that can greatly deteriorate the robustness and quality of the power supply.

2.6.1 Ground Loops

A ground loop refers to a - generally undesired – signal path where current in a conductor connecting two points that are supposed to be at the same potential, which is usual ground. Long signal paths often imply an increase in the impedance of the connector, since the Ohmic value of the conductor is directly proportional to the length of the conductor. This non-zero impedance results in the potential difference between the two points of the connector not equalling zero, resulting in the flow of a current through that conductor. All signals in a system are with respect to its respective grounding potential, which means that the current flowing in that signal returns to its source through the conductor at ground potential. In large systems the source may be a relatively large distance away, again implying a long path for the returning signal to follow. These long paths increase the susceptibility to environmental noise as depicted in Figure 2-17:

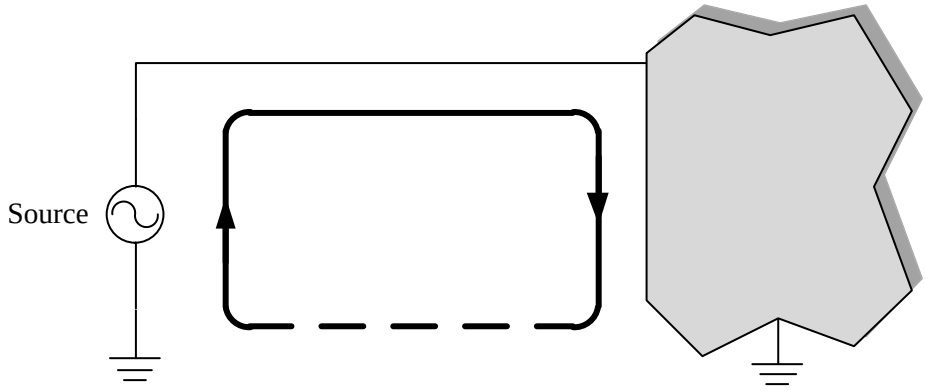

Figure 2-17: A Common Ground Loop

The system designer can however greatly reduce this induction of noise by utilising the basics of circuit theory*: A current can only flow if there is a complete path for it to follow*. Ampere's Integral law is formalised as Maxwell's 2nd integral law:

$$\oint \vec{\mathbf{H}}.d\vec{\mathbf{s}} = \int_S \vec{\mathbf{J}}.d\vec{\mathbf{a}} + \frac{d}{dt}\int_S \varepsilon_0 \vec{\mathbf{E}}.d\vec{\mathbf{a}} \qquad (2.2)$$

where $\vec{\mathbf{H}}$ is the magnetic field intensity around a closed contour, $\vec{\mathbf{J}}.d\vec{\mathbf{a}}$ is the current passing through the surface and $\varepsilon_0\vec{\mathbf{E}}$ is the flux density through the surface with ε_0 being the permittivity of free space. Haus and Melcher [27] define Maxwell's 2nd integral law as:

> *The circulation of the magnetic field intensity around a closed contour is equal to the sum of net current passing through the surface spanning the contour and net displacement flux density through the surface*.

If the designer is therefore able to inhibit the flow of current of a signal through the ground path, then no noise can be induced in that conductor and this results in the reduction of EMI in the system. A typical application that is implemented to prevent a ground loop between a power source and a load is to use a supply with respect to a ground potential that is not physically connected to the ground potential of the load. This is one of the governing properties that separate the isolated- from the non-isolated power supply system, since an isolated power supply provides a supply solution where the return path to the source is physically disconnected.

2.6.2 Common-Mode Noise

In circuit theory, signals can be classified as being either single-ended or differential signals. A single-ended signal is transmitted by sending the signal on a single path which is with respect to a common ground. Common-mode (CM) noise is interference that appears on both the signal lead and the return lead. The signal attributes and behaviour of common-mode noise are thus identical on both the signal path and its return path. Conclusively, a single-ended signalling path can be highly susceptible to CM noise. However, various component options exist to greatly reduce CM noise:

CM-Filter: CM-noise induces an identical signal and consequently similar current flow in both paths. The primary- and secondary- windings of the transformer can be placed on a signal pair as shown in Figure 2-18. Consequently, CM-noise in one signal lead will induce a magnetic field that will counteract a magnetic field that is identically induced by the other lead. This will result in the currents that induced the magnetic fields in the respective signal leads, being reduced and subsequently inhibiting the CM-noise on both signal paths.

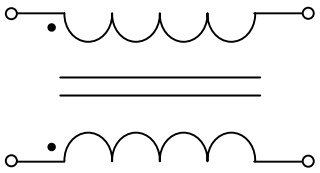

Figure 2-18: CM-Filter Equivalent Circuit

Ferrite bead: A ferrite bead is a component that is often used to reduce high-frequency noise on a power supply path. The ferrite bead has the property that it is purely inductive at relatively low frequency but when high-frequency (in the range of MHz) current flows through the bead its Ohmic value drastically increases, resulting in the attenuation of the current strength of the corresponding high-frequency signals. Its Ohmic

reactance is non-linear with respect to frequency. This effectively eliminates many high-frequency signals from the signal path.

2.6.3 Differential-Mode Noise

A signal is transmitted differentially by means of complementary signals sent on two separate paths. The differential equivalent signal is interpreted at the destination as the difference between these two signals. Therefore, any deviation of a signal with respect to ground is ignored. Differential-mode (DM) noise is more difficult to quantify, since DM noise occurs when the noise on the signal path is 180° out of phase with the signal on the return path. The magnetic fluxes induced by DM noise on the respective leads thus counteract each other which consequently implies that no impedance is produced on the leads. This means that DM noise cannot be suppressed by a CM filter. Impedance therefore needs to be included to suppress the DM noise. For this reason, an inductor is typically included on the signal path. To dissipate the DM-noise a low impedance path is required. A capacitor can thus be connected between the differential signal pairs which will effectively suppress some of the DM-noise. Figure 2-19 shows this typical means of successfully suppressing DM noise. If a source is differentially supplying power to a load, then including an inductor in series with the line will suppress the DM noise.

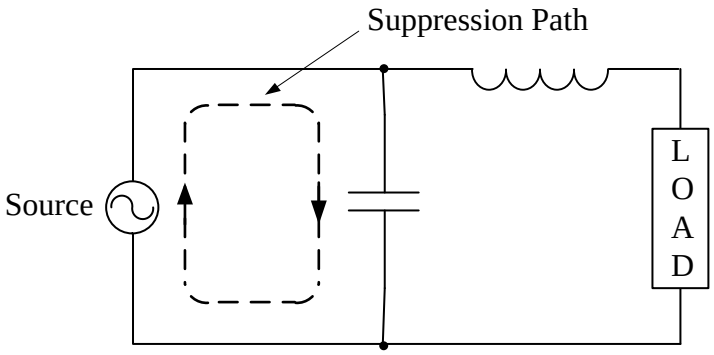

Figure 2-19: Suppressing Differential-Mode Noise

It should be noted however that the inductor-capacitor combination will affect the transfer characteristics of the line, which may further complicate the design of future control strategies.

2.6.4 Choosing a Power Supply Solution

A non-isolated supply implies a single ground level and all potential levels being with respect to this ground level. The modules driving a power switch, like an IGBT, are typically placed in close proximity to the IGBT, implying grounding leads to each module. These leads can quickly become very long and as a consequence increase the system's susceptibility to environmental noise. The switching converter generates high $\frac{di}{dt}$ and $\frac{dV}{dt}$ signals, which results in the generation of strong electromagnetic interference (EMI) in the proximity of the driver modules. The long grounding leads between the controller and the driver modules

provide an undesired path for the propagation of EMI. EMI will negate the performance of the whole system due to the afore-mentioned close proximity of the grounding lead between the main controller and the driver modules. Employing an isolated power supply setup to power the driver modules will greatly increase the system's immunity to EMI induced noise, since these driver modules are typically galvanically isolated from the rest of the system. An isolated power supply solution will thus increase the power supply rejection ratio for the electronics and consequently improve power quality and signal integrity.

To reduce the noise susceptibility of the power supply system, an isolated power supply solution is hence proposed. Switch-mode power supplies (SMPS) often include galvanic isolation between their power source and their output. For this reason, SPMSs are used to establish the various potential levels required by the system, due to their isolating property. As has been mentioned above, the power switch driver modules are placed in close proximity to the switch. To prevent large ground loops, these modules will be independently powered by a single DC-DC converter. The controller likewise requires various potential levels. To establish an isolated supply system in addition to satisfying the numerous power requirements, the topology in Figure 2-20 is proposed.

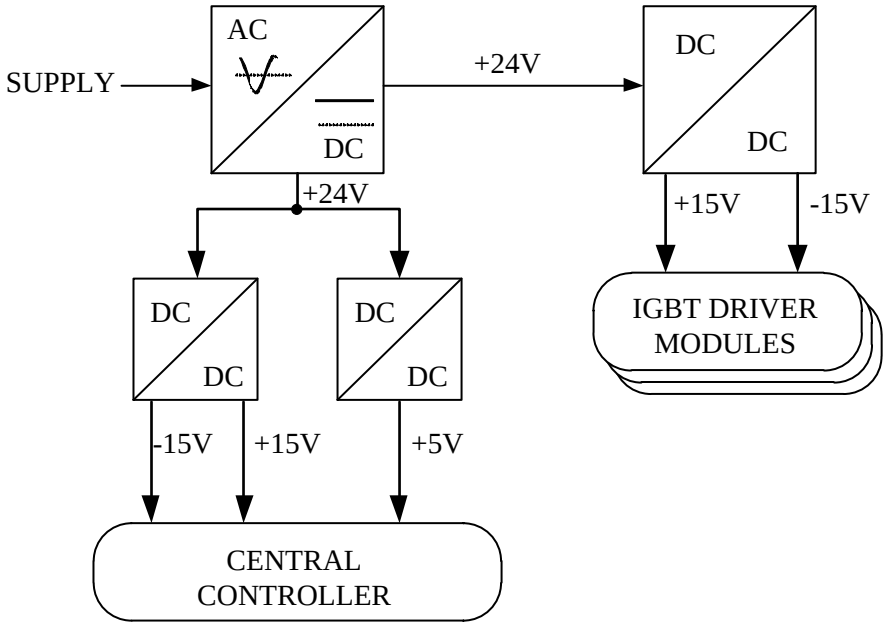

Figure 2-20: Power Supply Overview

The AC supply is converted by an isolated AC-DC SMPS to produce +24 V, which is subsequently used to generate ±15 V by a DC-DC converter for the IGBT driver modules. The same +24 V is used by two other independent DC-DC converters to generate ±15 V and +5 V for the analogue and digital electronics of the central controller. This system provides the required flexibility to achieve the required isolation. The potential levels used on the controller are shown in Figure 2-21. Isolated power is input to the controller and further regulated to +3.3 V to power the analogue and digital electronics on the controller.

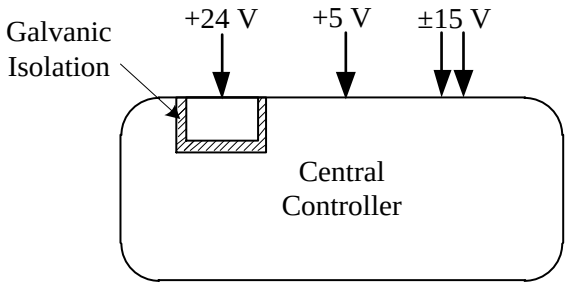

Figure 2-21: Central Controller Power Supply Overview

As indicated in Figure 2-21, the +24 V supply is isolated from the rest of the power on the central controller. This potential is used in the sensing of the contactors and circuit breakers in the line-interactive UPS. It once more entails long leads between the individual contactors and the central controller and thus again increases noise susceptibility. The connection path length needs to be minimised to ensure reduced environmentally induced noise on the lead. Utilising the isolated supply thereby ensures that no complete signal paths to the grounding potential of the central controller exist. The isolation therefore prevents any noise induced on the leads to be injected into the rest of the power supply system. The design of a solution to achieve this isolation is further discussed in the next section.

2.7 Online Monitoring of Small-Signal Power Supply Voltages

Practical experience indicated that the probability of IGBT failure increases when the IGBT driver modules' supply voltage varies from a nominal value. Measurements of these small-signal power supply potentials are therefore included to enable online monitoring by the central controller and consequently providing additional protection for the system. All the voltages that are used to supply both the analogue and digital electronics of the system are therefore measured. This telemetry is processed by the CPLD and relayed to the DSP. The DSP in turn determines whether any voltage potential varies from the nominal by a predetermined limit and consequently executes the necessary procedure to safely shut down the UPS system.

2.7.1 Measurement of Power Supply Voltages

The voltages are measured and conditioned by simple operational amplifier circuits. The signals are conditioned to be compatible with a multi-channel ADC. Figure 2-22 provides a topological overview of the strategy employed to measure the small-signal supply voltages.

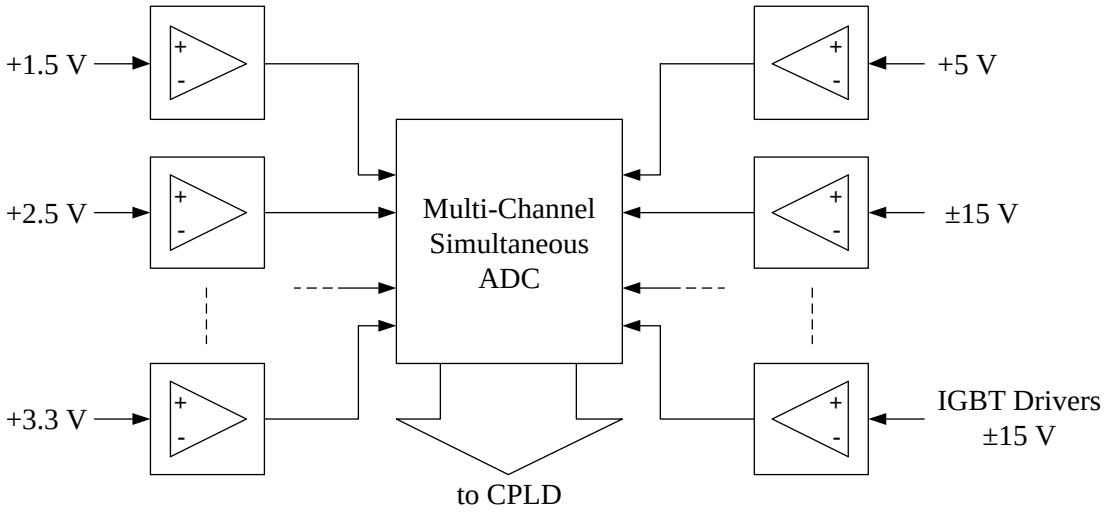

Figure 2-22: Voltage Measurement

The multi-channel ADC is an AD7266 from Analog Devices™ [28]. It consists of two identical SAR ADCs and is capable of simultaneously converting two analogue signals at a sampling rate of 2 MSPS. The digital data produced by the ADC is subsequently relayed to the CPLD, where it is further processed.

2.7.2 Embedded Acquisition of Measured Voltages

The converted data produced by the multi-channel ADC is input to the CPLD, where embedded hardware has been developed to process the data into information that can be used by the DSP. The motivation for processing the data by the CPLD rather than by the DSP is to alleviate some of the unnecessary calculation overhead on the DSP. If this is done the DSP has more time at its disposal to execute the more important time-critical control calculations. Figure 2-23 shows the embedded hardware that is implemented on the CPLD. The data conversion block simply processes the serial data steams received from the ADC and converts them to 12-bit numbers. The data conversion block also provides the necessary $\overline{CS}$, clock and multiplexing signals required by the ADC for conversion. The data conversion block is controlled by the conversion control block which determines the multiplexing signal for the ADC which corresponds with the appropriate small-signal supply voltage.

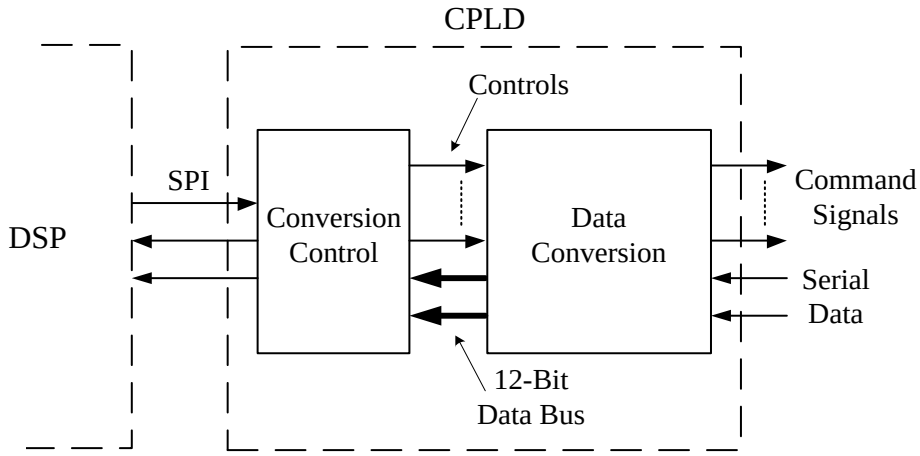

Figure 2-23: Embedded Design of Voltage Acquisition

The processed data is subsequently transferred from the CPLD to the DSP via a simple SPI protocol. The DSP therefore only determines whether these supply voltages are within tolerable limits. If any of the voltages deviate outside the allowable limit, the central controller shuts down the line-interactive UPS and logs the error.

2.8 System Status Sensing and Control

Figure 2-16 shows that numerous contactors and circuit breakers exist in the UPS system. The objective is to control the real-time status of these switches and additionally be aware of its real-time status. In the following subsections therefore the respective control and sensing of these contactors and circuit breakers will be discussed.

2.8.1 Real-Time Sensing

To determine whether a contactor or circuit breaker is either opened or closed, a sensing strategy is required to ascertain its real-time status. For this reason there are auxiliary switches that are mechanically connected to each contactor and circuit breaker. In other words, if the contactor opens, the auxiliary switch will similarly change its state. It was seen in the previous section that an isolated power supply solution is utilised to sense the status of these switches. As shown in Figure 2-24, the isolated + 24 V supply is directly connected to the auxiliary switch of a contactor/circuit breaker. The series resistor R_S is simply included for limiting the current drawn by the primary LED of the optocoupler and the capacitor C_p and serves the purpose of filtering high-frequency EMI induced transients on the sensed signal. Due to the high $\frac{dV}{dt}$ and $\frac{di}{dt}$ signal produced by the switching converter, this small-signal circuit operates in a high-noise environment. The optocoupler produces a binary output signal and will sporadically change state due to the

high noise level of the system. A Schmitt trigger was therefore included for this purpose and will reduce unnecessary state changes by inducing a hysteresis band around the threshold between a logic high and logic low.

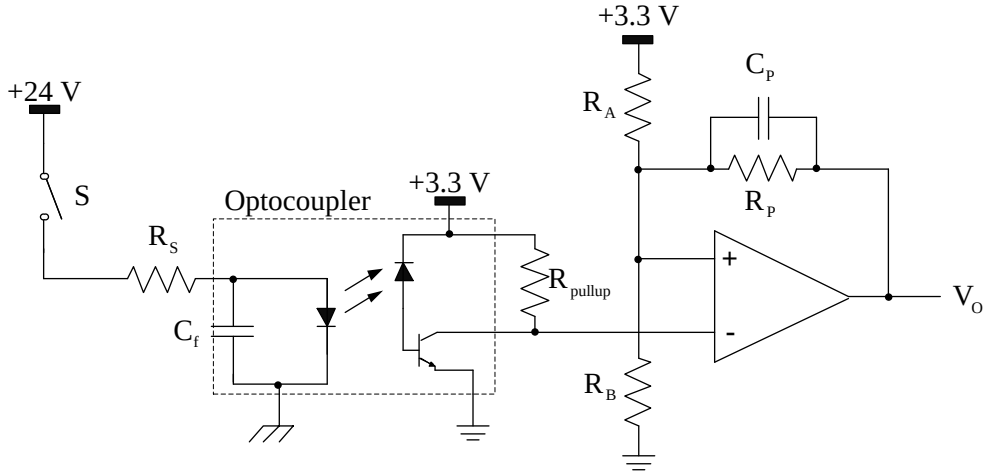

Figure 2-24: Sensing Circuit with Incorporated Schmitt Trigger

Resistor R_{pullup} provides a definable high state voltage for the open-collector output of the optocoupler. Resistors R_A and R_B establishes a threshold of approximately 1.6 V and resistor R_p determines the amount of hysteresis around that 1.6 V threshold and the parallel connected capacitor provides enhanced switching speed between the output states of the Schmitt trigger. Appendix B discusses the calculations to determine resistor R_p to establish a hysteresis of V_{hys}.

2.8.2 Switch Control

With the objective of controlling the various contactors and circuit breakers in the line-interactive UPS, the circuit in Figure 2-25 is used. The contactors are driven via a relay which is controlled by this circuit. A logic signal u_C is applied to a MOSFET driver which in turn drives a MOSFET. There exists a capacitive miller plateau at the gate of a MOSFET. A MOSFET driver is thus utilised because it can provide large peak currents to the capacitive gate of the MOSFET [29]. This ensures quick transition of the MOSFET between fully on or fully off state.

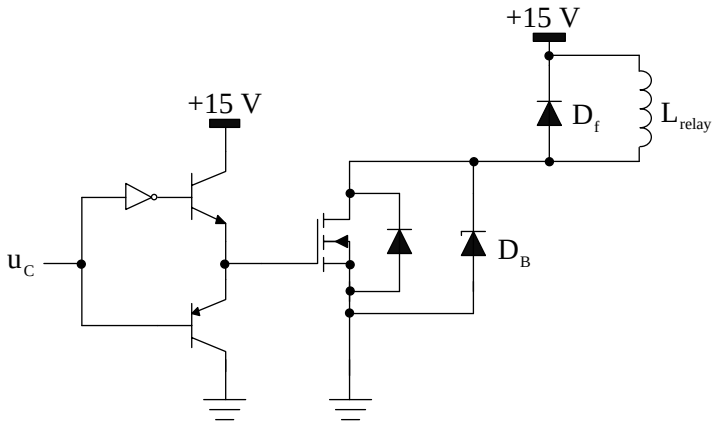

Figure 2-25: Switch Control Circuit

The MOSFET is a MTP27N10E power MOSFET that is capable of withstanding high energy avalanche and commutation modes [30]. It is thus capable of conducting the large initial current when the relay's magnetising coil is engaged, as well as withstanding the relatively large back-EMF that occurs when the magnetising coil is disengaged. The free-wheeling diode D_f is for this reason included across the relay's magnetising coil to provide a path for the inductor current to dissipate. The ceramic transient voltage suppressor (CTVS) D_B is included for protection of the MOSFET by preventing voltage breakthrough of the MOSFET's drain-source threshold.

2.9 Digital Signal Controller

To establish central control on the UPS system, the controller is digitally operated by a digital signal controller. This controller is briefly discussed in the following sections.

2.9.1 The Delfino 32-bit Floating-Point Processor

The TMS320F28335 MCU from Texas Instruments is at the core of the controller of the system. It has a 32-bit floating-point ALU and is capable of executing numerous complex floating-point calculations at a fraction of the time it would have taken for a fixed-point ALU. The floating-point ALU complies with the IEEE Standard for Floating-Point Arithmetic (IEEE 754). The TMS320F28335 has several integrated peripherals features; features such as high-resolution enhanced PWM, integrated multi-channel high-speed ADC units and several communication peripherals such as serial-peripheral-interface (SPI), serial-communication-interface (SCI) and inter-integrated-Circuit (I^2C) to name a few.

All of these interfaces are united on the central controller. Figure 2-26 diagrammatically depicts all functional blocks on the central controller.

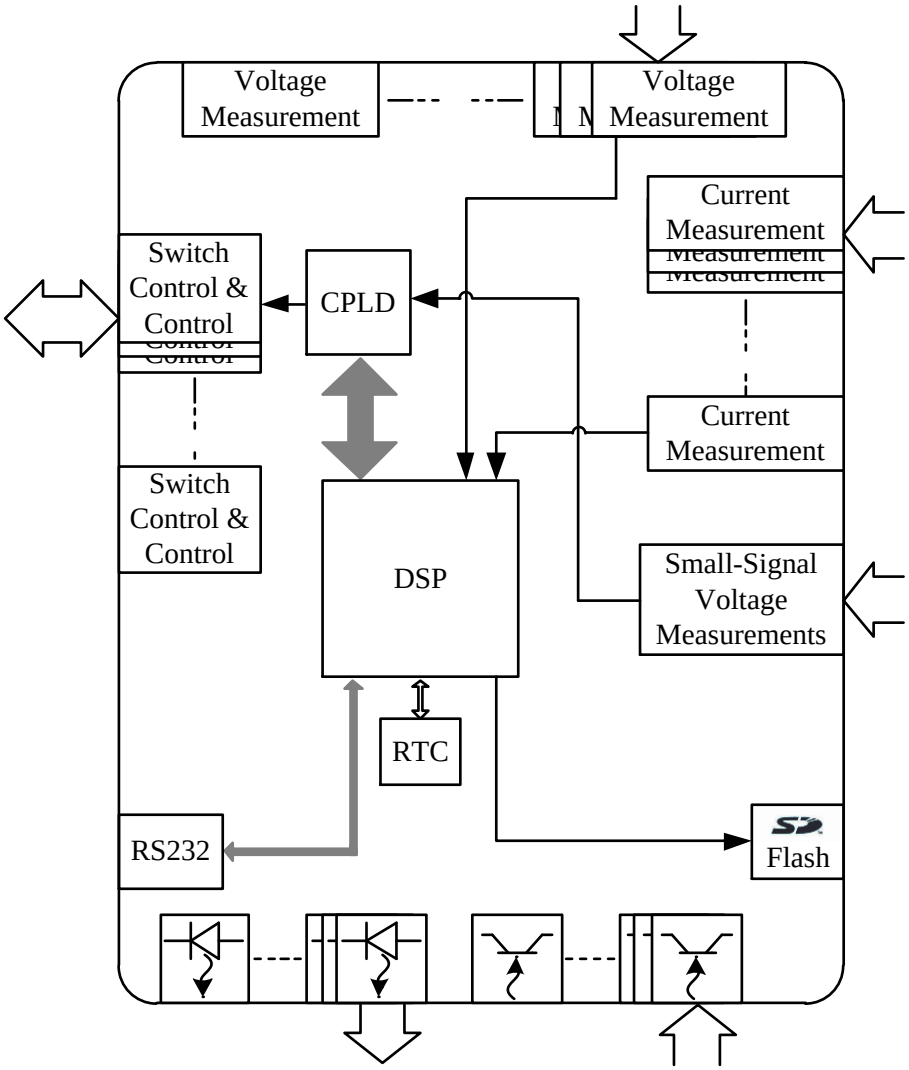

Figure 2-26: Controller Block Diagram

2.9.2 Measurement Conversion

The controller updates the PWM signal once every switching cycle. The switching frequency on the system used in this project is 5 kHz, thus implying a 200 μs switching period. To establish closed-loop control, the output parameters need to be fed back to the controller. The analogue signals therefore need to be converted to equivalent digital codes. The controller needs to acquire the required measurement and execute the required calculations within the switching period. The conversion time needs to be as short in duration as possible not to occupy too much of the time in the switching cycle. The format of this digital data is directly dependent on the architecture of the analogue-to-digital converter (ADC). Various architectures have been investigated, as briefly discussed.

To reduce the amount of available calculation time and consequently the capabilities of the DSP controller, the conversion time needs to be as short as possible. A fast conversion time signifies a fast sampling rate. Therefore, the goal is to use an ADC with a high sampling rate.

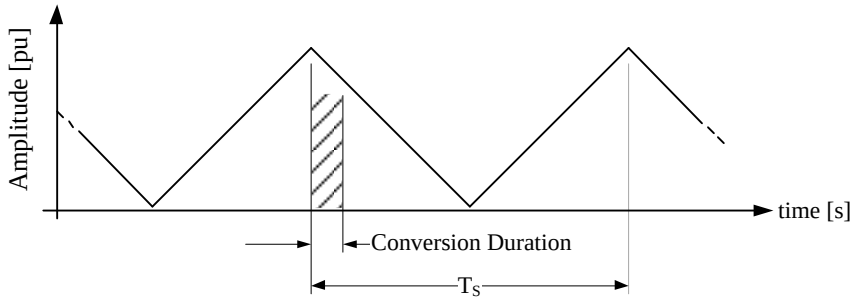

Figure 2-27: Conversion Duration Timing Diagram

2.10 Parameter Measurement and Signal Conditioning

It is important that the measurement circuit has the ability to give an accurate representation of the system's current or voltage values. As discussed in [31], some of the more typical measurements are the DC-link voltage (V_{DC}), load voltage (V_L), output currents like the inductor current (I_L) and load current (I_O). To a large extent, power measurement equipment is designed under the assumption that a sinusoidal parameter is measured. This, however, is not the case for switching converters due to their non-linear characteristics. The performance requirement of the measurement circuits is therefore much more demanding. Circuit specifications such as Gain-Bandwidth Product (GBW), Total Harmonic Distortion + Noise (THD+N), Signal to Noise Ratio (SNR), Common-Mode Rejection Ratio (CMMR), amplitude error and phase error need to be considered when such systems are designed:

i. GBW: The non-linear behaviour of switching converters produce output voltage and current signals containing multiple frequency components, some of which include:
   - The desired fundamental output signal;
   - The ripple components caused by the switching behaviour of the converters; and
   - Feedback components caused by non-linear loads.

   These additional high-frequency components are used in certain control algorithms, such as ripple compensation. This consequently places increased emphasis on the GBW of the measurement circuit to produce the high frequency components accurately without a drop in gain.

ii. THD+N: Even though the measurement of certain signal components are essential, care should be taken to prevent the injection of additional harmonic components on printed-circuit board level. Long measurement paths are susceptible to the induction of environmental noise. Digital clocks used by the microcontroller can also cause clock feed-through. It is important to draw attention to the fact that the THD+N of both the system parameter and the measurement result should be similar. Any loss in frequency information may result in the degradation of the controller performance capability.

iii. SNR: Common-mode instability and environmental noise can degrade the signal integrity of measurement signals. Unmistakably, the introduction of additional noise is undesired.

iv. CMRR: A high CMRR will guarantee that any signal introduced to the system that is common to the measurement circuit's input and its point of reference will be discarded. An insufficient CMRR

degrades circuit precision by effectively introducing a voltage offset as a function of a DC level at the input [32]. However, this is rarely the case in power electronic applications where line voltage signals are used. It is also recommended in [32], that a completely differential signal-chain be used to achieve the benefits of differential signals, such as even-order harmonic cancellation and increased analogue dynamic range.

v. Amplitude Error: Koeslag identified in [25] that switching devices such as MOSFETs have series non-linear impedance. MOSFETs are commonly used in – for example – half-bridge topologies. In such a situation, if the current through the MOSFET increases, a corresponding error in the output voltage will occur. This is a clear example of an error that is made in the amplitude of a signal. As a result, output amplitude of the half-bridge varies, which effectively corrupts the system parameters.

vi. Phase Error: Phase error can easily creep into a measurement circuit if some of the discrete components contain parasitic capacitance. The parasitic capacitance will influence the transfer function of the circuit and induce a small phase on the output. If the measurement result contains a phase error with respect to the measured parameter, the resulting digital code used by the controller will cause an inaccurate response. This could degrade the performance of the power electronic system.

The voltage and current measurements are fed back to the digital controller for the implementation of closed-loop control schemes. It is important however to condition these measured signals to exploit the whole analogue input voltage range of the ADC fully. Quantisation of the signal is necessary to digitise the analogue signal to a digital equivalent. It can however undermine the stability of the digitally implemented control systems. Exploitation of the whole ADC input range will optimise the effective-number-of-bits (ENOBs) used for the digital representation of the analogue signal. The ENOB of a signal is defined as:

$$\mathrm{ENOB} = \mathrm{n} - \mathrm{floor}\left(\log_2 \frac{\mathrm{FSR}}{\mathrm{A_{PP}}} \right) \tag{2.3}$$

with n being the bit resolution capability of the ADC, FSR being the Full Scale Range of the ADC and A_{PP} being the peak-to-peak amplitude of the signal being measured [31]. The goal is to implement a controller capable of achieving a as close to zero tracking error as possible. To achieve this, the measurement hardware has to take accurate measurements. Due to the high-noise environment of switching converters, the measurement circuit requires increased noise immunity. In the following sections the voltage and current measurements will discussed.

2.10.1 Voltage Measurement

It is highly recommended to employ the high CMRR benefit for measuring the voltage differentially. This has the added benefit that the measured voltage need not be measured with respect to the ground of the measurement circuit. Additionally, the differential measurement enables the system ground of the controller

to be referenced to any point within the DC bus's upper or lower limits [33]. Even if the system ground of the controller is isolated from the high voltage power electronic system, a large DC level can be observed due to ground differences. Consider the circuit proposed by [32] in Figure 2-28, which depicts a high voltage differential amplifier measurement solution.

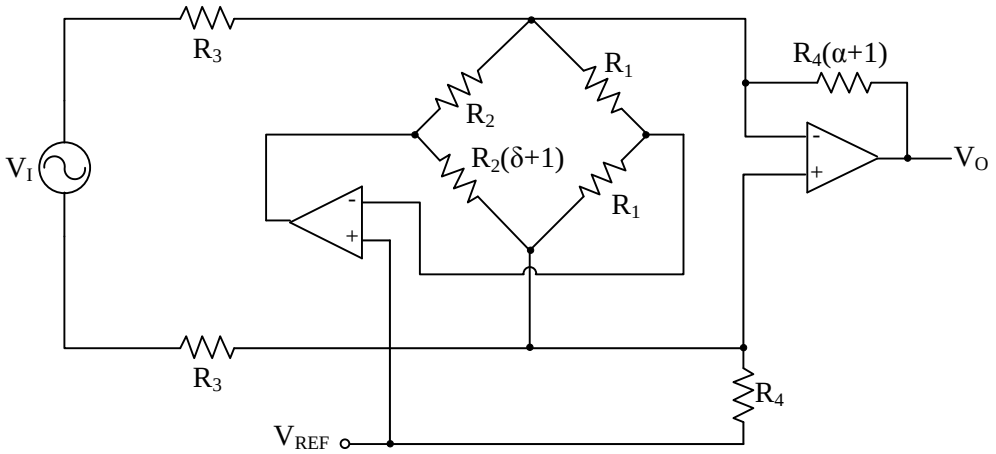

Figure 2-28: Voltage Measurement

The circuit's high CMRR capability makes it a great option when high common-mode signals are experienced in the system. The transfer function for this circuit is given in equation (2.4), where V_{CM} is the common-mode noise component of the input signal and V_{diff} the differential component.

$$V_O = \frac{-1}{R_3}\left\{\frac{(\delta+1)\left[R_1R_2R_4\frac{\alpha+1}{\delta+2}+R_2R_3R_4\frac{\alpha+1}{2}\right]}{R_1R_3R_4+\left(R_2R_3R_4+R_1R_2R_4+R_1R_2R_3-\frac{R_2R_3}{2}\right)(\delta+1)-R_1R_3\frac{1}{\delta+2}}\right\}V_{CM} + \frac{-R_4(\alpha+1)}{R_3}V_{diff} \quad (2.4)$$

The derivation of the transfer function can be found in Appendix A. The output voltage is then level shifted by V_{REF} to ensure compatibility with an ADC. Analysis of V_{CM}'s term shows that it is an extremely small value which corresponds with this circuit's characteristically high CMRR. The Wheatstone bridge has a high sensitivity and facilitates the active filtering of these common-mode components.The common-mode element on the input is furthermore removed using an active filter utilising a Wheatstone bridge topology. This topology ensures a very sensitive means of detecting and actively mitigating any common-mode signals.

Varying R_1 will have no effect, due to the symmetric design of the circuit. Its purpose is to determine the severity by which common-mode noise is removed. The circuit characteristics, however, will indeed be changed by the changing of the value of R_2. This is due to the fact that R_2 contributes to the loading of the resistor network at the input and directly affects the voltage division of that network. The high voltage signal is decreased by means of a voltage divider resistor network. Increasing R_B will decrease the factor by which

the high voltage signal is attenuated. Care must therefore be taken not to excessively exceed R_2, since this will result in the signals input to the op amp extending beyond the amplifier's input range. Similarly, changing R_3 will affect the magnitude of the signal that will be measured by the circuit. The main goal is to ensure optimal utilisation of the analogue input range of the ADC. In the appendix the design and subsequent calculation of the biasing resistors of the voltage measurement circuit is discussed.

2.10.2 Current Measurement

In conjunction with the output voltage telemetry, additional current measurements need to be made to achieve closed-loop control of the output current. There are numerous options for measuring current. Some of the more common methods for measuring current are:

- Shunt Resistor
- Current Transformer
- Current Transducer

Shunt Resistor: A current shunt circuit measures the small differential voltage across a resistive shunt. The voltage difference across the shunt is proportional to the current through the shunt. The obvious advantage of this option is that it is a cheap and simple solution. The disadvantage however lies in the problem created by the common-mode component of the circuit being measured. Ideally, the differential voltage across the resistive shunt corresponds directly to the current through the shunt. The problem is that there will almost always be a common-mode component on the current in the circuit. The switching of the converter in fact causes large common-mode voltages and high slew rates which can result in a highly corrupted measurement. This common-mode current will consequently also induce a voltage on the shunt which effectively leads to the distortion of the measurement, since the differential voltage needs to be an accurate representation of the differential current in the circuit. This makes it extremely difficult to measure current telemetry accurately and it is for this reason that this option for current measurement is seldom used.

Ackermann also discussed in [34] that the typical limiting factor of resistive shunts is the self-heating of the shunts due to I^2R losses. Temperature related errors however are not the primary contributors to overall errors. Other subtle errors such as current feed-point sensitivity, field coupling to the shunt, proximity of ferromagnetic materials and many others often dominate.

Current Transformer (CT): The current transformer provides various advantages in current measurement. It provides sufficient galvanic isolation between the high-current circuit and the measurement circuit and it additionally gives an extremely good representation of the AC current in the primary circuit. This advantage reminds of the disadvantage that a CT can only measure AC currents. A transformer is also very expensive due to the large amount of copper being used in the component. It furthermore has a limited spectrum of frequencies depending on the core material of the transformer [35].

Hall-Effect Transducer: The transducer utilises hall-effect technology in conjunction with closed-loop application-specific integrated circuits to obtain a scaled representation of the primary current measurement with relatively low offset drift. The disadvantage of using current transducers however is their high cost. This option fortunately enables the measurement of the DC components in currents while also providing excellent galvanic isolation which normally is in the order of thousands of volts. This component, nonetheless, has a limited measurement bandwidth, but with a range of 100-200 kHz [36], which is more than sufficient for most, if not all, power-electronic applications. Nevertheless, as pointed out in [37], the hall-effect sensor has a minor design problem in that it has a large gain at high frequencies, which results in a highly distorted feedback signal in its closed loop circuitry.

Due to the great advantages provided by a Hall-Effect transducer, the circuit depicted in Figure 2-29 was designed for the measurement of the currents in the system. The LA 305-S [36] current transducer was used and can be approximated as a current source where the current output by the transducer is a scaled representation of the actual measured current.

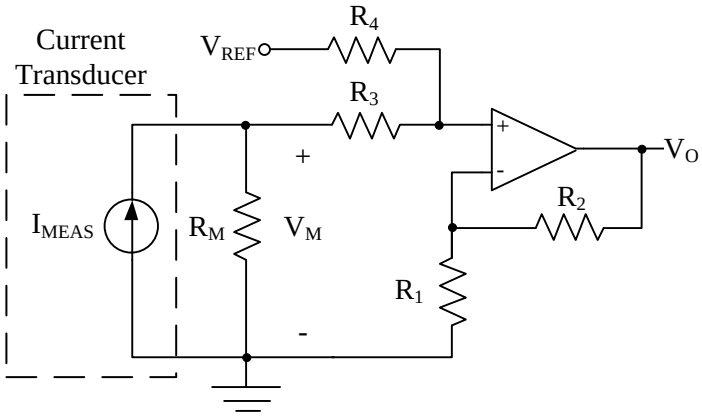

Figure 2-29: Current Measurement

The current I_{MEAS} subsequently flows through the measurement resistor R_M which induces a voltage V_M. The transfer function of this circuit is given by equation (2.5).

$$V_O = \left(1+\frac{R_2}{R_1}\right)\left(\frac{R_4}{R_3+R_4}V_M + \frac{R_3}{R_3+R_4}V_{ref}\right) \tag{2.5}$$

2.11 Optical Communication Interface

The digital controller communicates with the IGBT driver modules via an optical interface. The advantage obtained from utilising an optical interface is that it provides physical isolation between the high-power IGBT circuitry and the sensitive digital controller.

2.11.1 Optical Transmission

The initial state of all the IO (input/output) pins of the DSP is logic high. These IO pins are used to send commands to the optical transmitter. A logic high signal indicates that the respective IGBT must switch on and conversely a logic low implies that he IGBT must switch off. If all the IO pins are however high at start-up of the DSP, it means that all IGBTs will also be switched on. This will result in cross-conduction between the DC voltage rails of the converter. To prevent this from happening, the circuit depicted in Figure 2-30 is proposed.

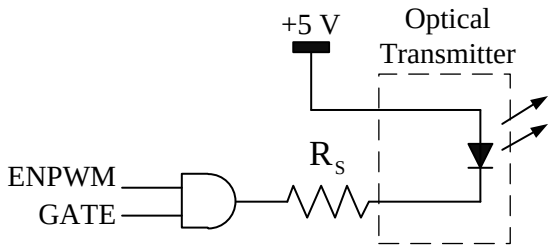

Figure 2-30: Optical Transmitter Circuit

In the event that both the ENPWM and the GATE command signals are logic high, the logic AND element will drive the terminal of resistor R_S high. The result is that the LED of the optical transmitter is not forward biased and therefore not turned on. The IGBT will thus not switch on when all the IO pins of the DSP are simultaneously high.

2.11.2 Optical Receiving

The IGBT driver modules are designed to return an error signal upon failure of the IGBT or if the IGBTs temperature is higher than a predetermined threshold. These error signals are transmitted optically to the digital controller. The error signals operate on an active low principle. In other words, the IGBT driver modules continuously send a signal if there is no error. Upon the occurrence of an error the IGBT driver module will cease sending a signal to the controller and the appropriate shutdown sequence will be initiated.

The circuit in Figure 2-31 shows an optical receiver connected to a CPLD. The optical signals from all the IGBT driver modules are connected in an identical manner to the CPLD. An embedded NOR gate on the CPLD multiplexes these error signals to a single signal and relays it to the DSP. The DSP is configured in such a way that it will subsequently initiate a shutdown sequence if it receives this error signal.

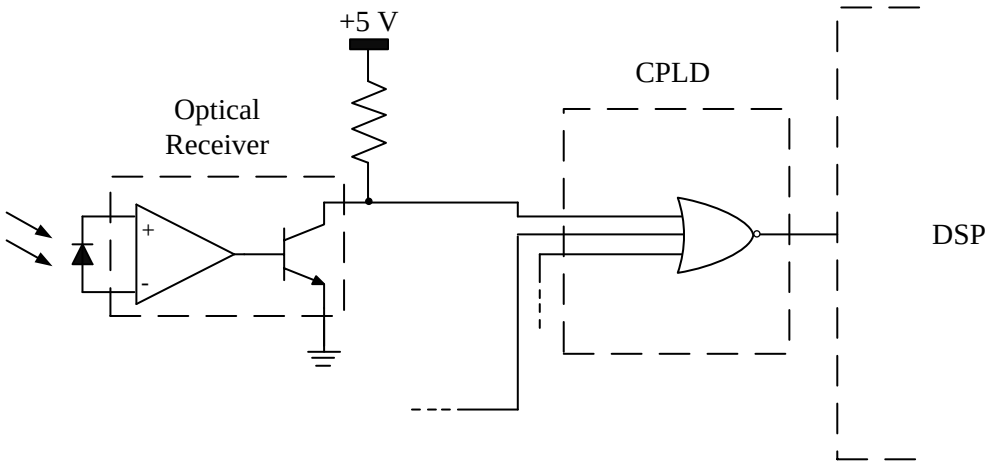

Figure 2-31: Optical Receiver Circuit

Utilising the optical interface between the IGBT driver modules and the digital controller provides the necessary physical isolation of the controller. In so doing, it ensures the safety of the controller in the case of an IGBT failing drastically.

2.12 Conclusion

This chapter identified that the analogue circuit used to measure the system's voltages and currents can influence the performance of the closed-loop controller. It was also found that the ADC architecture used to discretise the analogue signals can similarly affect the control performance. A study was done on some of the ADC architectures that are commonly used in power electronic applications.

Furthermore, the sensing circuits used by the digital controller were discussed. The design and implementation of these sensing circuits provided the additional advantage of minimising the ground loop in the system. Finally the optical interface between the controller and the IGBT driver modules and how it was implemented in the system, was briefly discussed. All of the abovementioned circuits and methods were used in the development of the central controller which is depicted in Figure 2-32. The figure provides a depiction of the implemented digital controller and shows how the physical system corresponds with the block diagram in Figure 2-26.

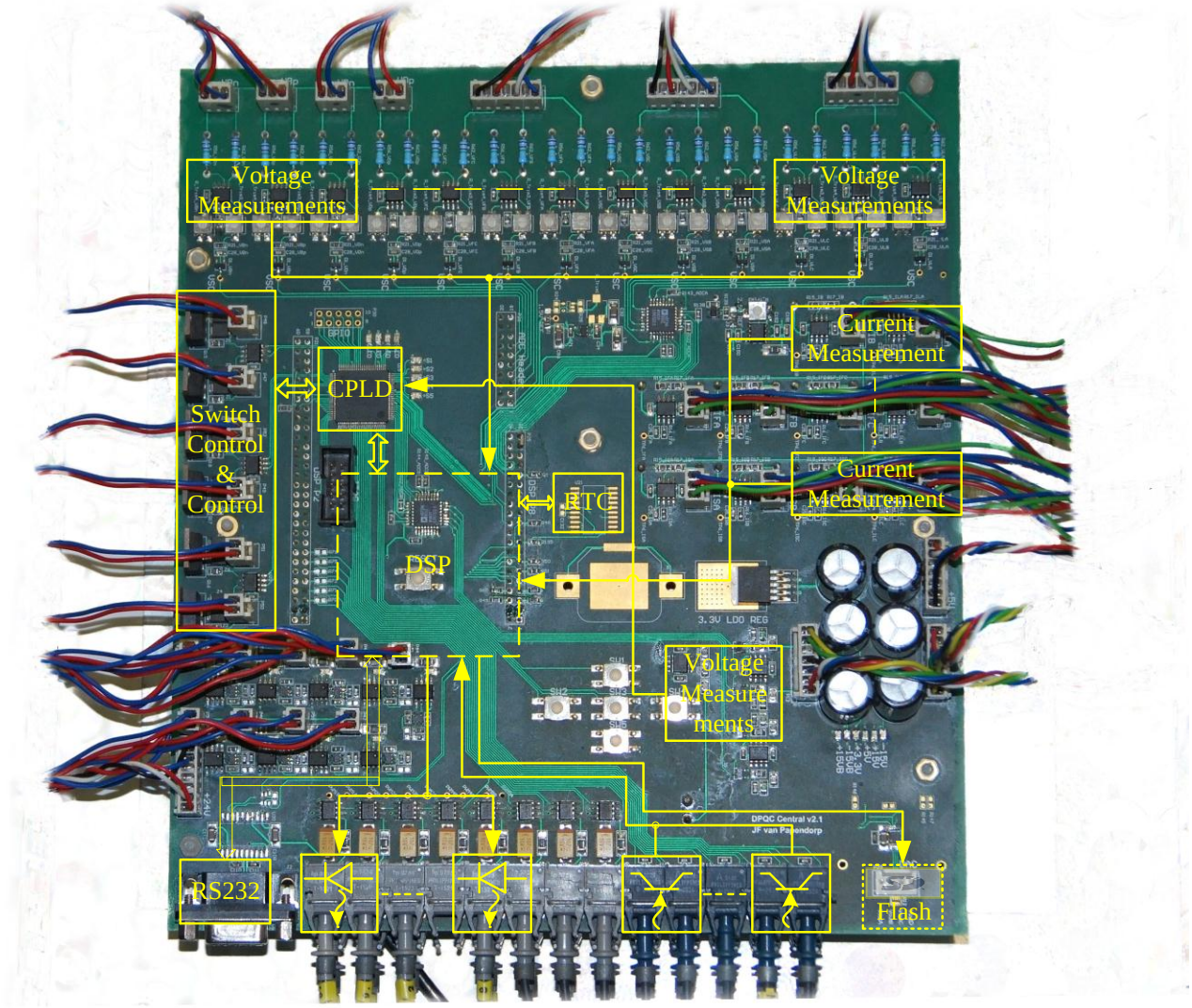

Figure 2-32: Photograph of Digital Central Controller

CHAPTER 3

THE THREE-PHASE SWITCHING CONVERTER

3 THE THREE-PHASE SWITCHING CONVERTER

3.1 Introduction

In this chapter the literature along with any background information required to establish effective controlled switching of the line-interactive UPS regardless of the mode it is operating in, is discussed. Whether it is charging the DC-link, regulating it or supplying power to the load, there remain similarities in the UPS. The manner in which the converter is switched for instance always utilises Space-Vector-Pulsewidth-Modulation (SVPWM). This modulation scheme is discussed in this chapter along with the inherent advantages associated with its implementation.

Due to practical irregularities, the IGBT switches are not capable of instantly latching to the active or inactive states. It is therefore common practice to implement a dead time between the switching of the respective high-side and low-side IGBTs. This dead time leads to corruption of the output signal, which serves as the motivation to develop a dead time compensation scheme to counteract this corrupting property caused by the inclusion of dead time.

3.2 The Clarke Transformation

The Clarke transform, better known as the alpha-beta (αβ) transform, is a mathematical transformation whereby a three-phase system model is converted to a two-dimensional model. At first glance, this transformation immediately reduces the calculation of control equation by 33%. Under normal circumstances, the reference voltage for each of the three phases has to be calculated. The Clarke transform, however, provides a means of calculating only two reference voltages and still ensuring effective control of all three leg-voltages. For the sake of this discussion, assume an inverter topology as shown in Figure 3-1 and that it connects to a three-phase balanced load. With a balanced load being assumed, the voltage V_{GN} is found to be:

$$V_{GN} = \frac{V_{ag} + V_{bg} + V_{cg}}{3} \tag{3.1}$$

and the balanced output voltages are described by equation (3.2):

$$\begin{aligned} V_a(t) &= V_M \sin(\omega t) \\ V_b(t) &= V_M \sin(\omega t - 120°) \\ V_c(t) &= V_M \sin(\omega t + 120°) \end{aligned} \tag{3.2}$$

with ω being the angular velocity of the sinusoidal signals which is directly proportional to the output frequency according to $\omega = 2\pi f$.

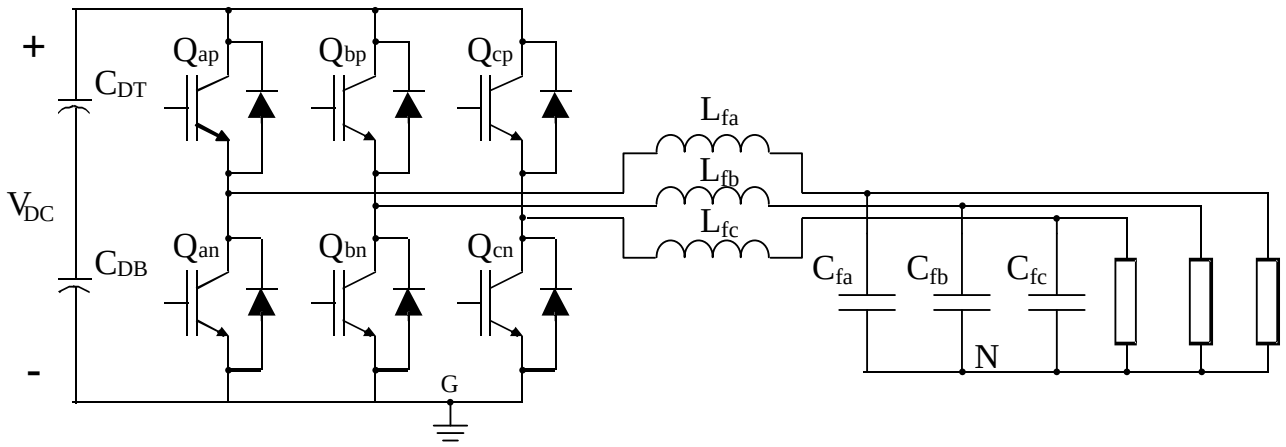

Figure 3-1: Three-Phase Inverter Topology

A balanced three-phase system can produce only two independent output voltages, since if V_{AB} and V_{BC} are known, then V_{CA} is implicitly defined. The eight (2^3) possible switching states of the three-phase inverter are listed in Table 3-1 with the corresponding voltages V_{xG} and V_{xN} for each phase. The vectors that represent the leg-voltages, V_{xG}, agree with a three-degrees-of-freedom (DOF) system.

Table 3-1: Three-Phase Inverter Switching States

Q_{Ax}	Q_{Bx}	Q_{Cx}	V_{AG}	V_{BG}	V_{CG}	V_{GN}	V_{AN}	V_{BN}	V_{CN}	Switching States
0	0	0	0	0	0	0	0	0	0	U_0
0	0	1	0	0	V_{DC}	$V_{DC}/3$	$-V_{DC}/3$	$-V_{DC}/3$	$2V_{DC}/3$	U_1
0	1	0	0	V_{DC}	0	$V_{DC}/3$	$-V_{DC}/3$	$2V_{DC}/3$	$-V_{DC}/3$	U_2
0	1	1	0	V_{DC}	V_{DC}	$2V_{DC}/3$	$-2V_{DC}/3$	$V_{DC}/3$	$V_{DC}/3$	U_3
1	0	0	V_{DC}	0	0	$V_{DC}/3$	$2V_{DC}/3$	$-V_{DC}/3$	$-V_{DC}/3$	U_4
1	0	1	V_{DC}	0	V_{DC}	$2V_{DC}/3$	$V_{DC}/3$	$-2V_{DC}/3$	$V_{DC}/3$	U_5
1	1	0	V_{DC}	V_{DC}	0	$2V_{DC}/3$	$V_{DC}/3$	$V_{DC}/3$	$-2V_{DC}/3$	U_6
1	1	1	V_{DC}	V_{DC}	V_{DC}	V_{DC}	0	0	0	U_7

The three inverter leg-voltages (V_{ag}, V_{bg}, V_{cg}) can subsequently be depicted by three orthogonal axes in the 3-DOF system of the leg-voltages. Ryan et al. [38] shows that the output voltages (V_{an}, V_{bn}, V_{cn}) can be constructed by projecting the 3-DOF leg-voltages onto a 2-DOF plane as depicted in Figure 3-2.

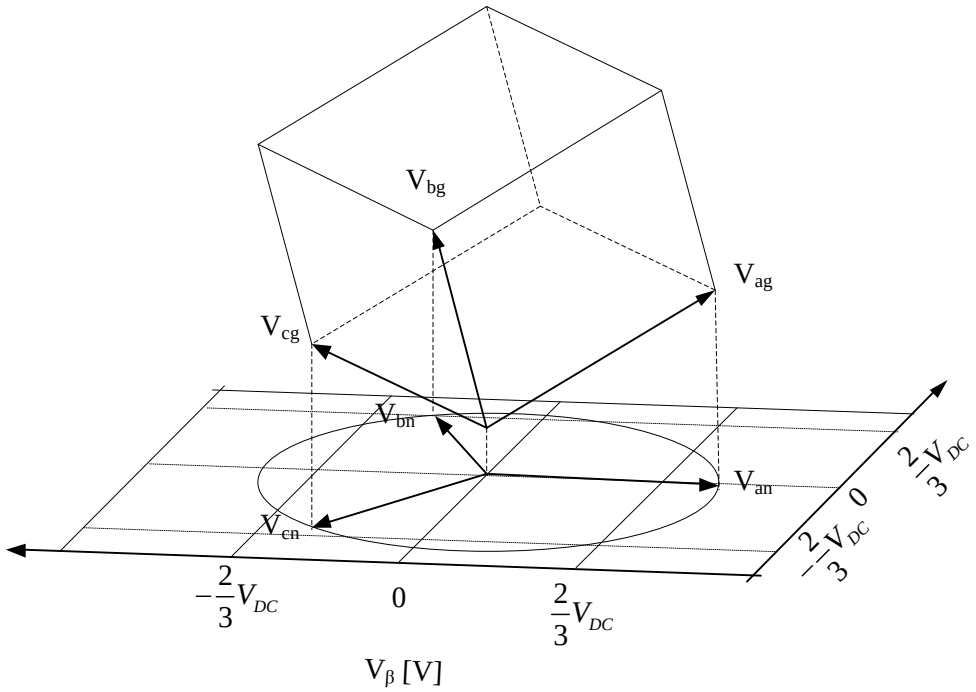

Figure 3-2: Three-Phase System Projection onto αβ-Plane

Consider this newly constructed 2-DOF plane onto which the output voltages are projected in Figure 3-3.

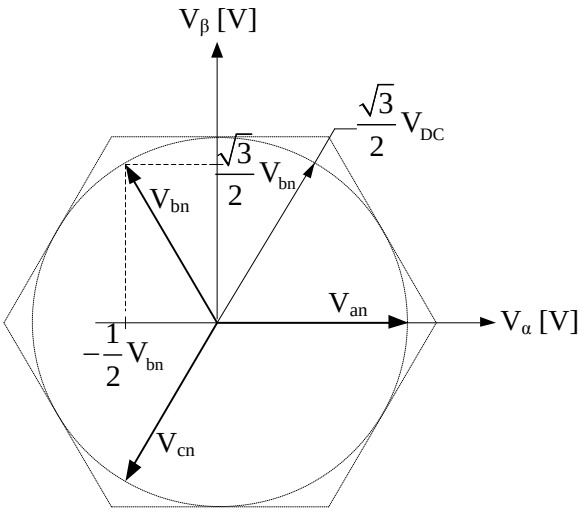

Figure 3-3: Projecting ABC-Vectors onto αβ-Plane

The output voltages (V_{an}, V_{bn}, V_{cn}) can therefore be projected onto the α- and β-axes of this 2-DOF plane resulting in a rotational vector with a constant amplitude (as shown in Figure 3-4). This plane is commonly known as the stationary reference frame. Note that the switching states U_0 and U_7 correspond with the so-called zero vectors, since zero output voltages are induced during these states. Notice that the limit of the amplitude of this vector is indicated by the inscribed circle being equal to $\frac{\sqrt{3}}{2}V_{DC}$. If the vector happens to

become larger than this indicated limit, the output voltages will be distorted resulting in a situation called inverter saturation [31].

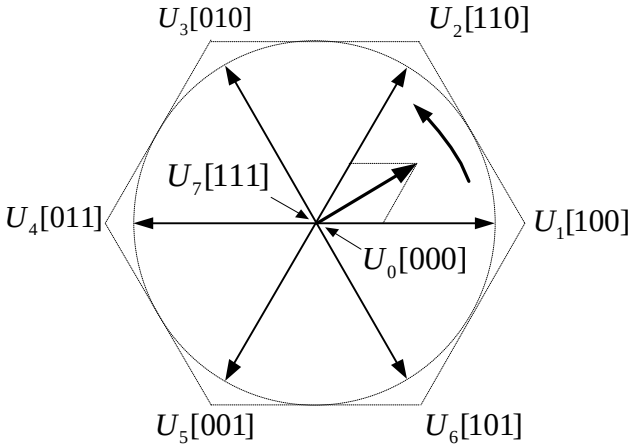

Figure 3-4: Construction of the Rotational αβ-Reference Vector

It is worth mentioning that the vector $\overrightarrow{\mathbf{V}^*_{\alpha\beta}}$ rotates at the angular velocity indicated by the sinusoidal output voltages in equation (3.2) through a full 360° in an anti-clockwise direction for a positive sequence of the output voltages. Conversely, a clockwise rotation will be observed when the output voltages have a negative sequence. Constructing the α- and β-vectors is accomplished by the use of the Clarke transformation matrix given in equation (3.3):

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_\gamma \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \tag{3.3}$$

The γ-vector is included for the sake of completeness, however, in balanced systems $V_{an} + V_{bn} + V_{cn} = 0$ results in $V_\gamma = 0$ and the 3-by-3 matrix in (3.3) simplifying to a 2-by-3 matrix:

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \tag{3.4}$$

Reconstruction of the ABC voltages simply implies using the inverse of the transformation matrix in equation (3.3), as indicated in equation (3.5) and is called the inverse Clarke transform.

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} V_{\alpha} \\ V_{\beta} \\ V_{\gamma} \end{bmatrix} \tag{3.5}$$

Keeping in mind that the $\overrightarrow{\mathbf{V}^*_{\alpha\beta}}$ reference vector has a maximum amplitude of $\frac{\sqrt{3}}{2}V_{DC}$, the maximum realisable sinusoidal output voltage by utilisation of the space-vector-modulation (SVM) scheme would be:

$$\begin{aligned} V_{xnMAX} &= \sqrt{\frac{2}{3}}\left(\frac{\sqrt{3}}{2}V_{DC}\right) \\ &\cong 1.15\frac{V_{DC}}{2} \end{aligned} \tag{3.6}$$

Notice that the application of space-vector modulation (SVM) increases the possible sinusoidal output voltage by approximately 15% with respect to what could be expected when considering the converter in Figure 3-1.

Furthermore, when analysing the transformation matrix in equation (3.3), it is observable that the row and column vectors of the Clarke transform are orthonormal to each other, since according to [39] the dot products of the unity vectors equal zero. The orthonormal characteristic of the vectors proves that the α- and β-vectors are independent of each other. This is an important advantage provided by the SVM scheme, since a controller can consequently be capable of independently controlling $V_{\alpha}(t)$ and $V_{\beta}(t)$, without the possible coupling of the two voltages.

The reference vector $\overrightarrow{\mathbf{V}^*_{\alpha\beta}}$ can be realised by the combination of the 8 switching states. Supposing the vector is in sector I as shown in Figure 3-5, it is possible to realise this vector by the combination of the U_1 and U_7 vectors. This modulation scheme is more commonly known as Space-Vector-Pulse-Width-Modulation (SVPWM) and provides a great advantage for the control of a switching converter.

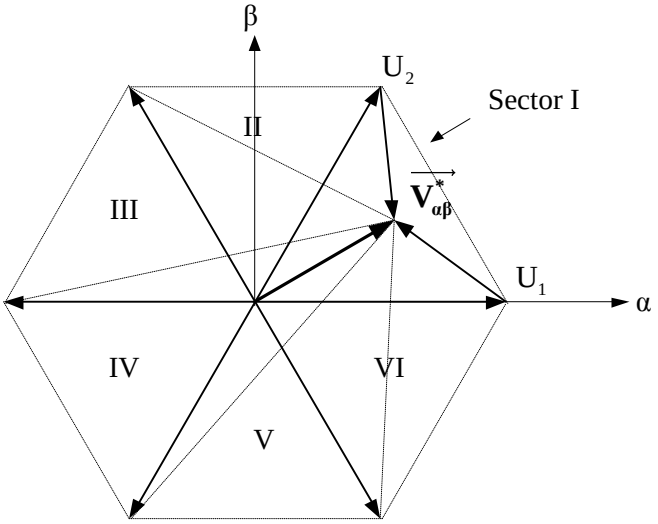

Figure 3-5: Constructing the αβ-Reference

The advantage obtained by the utilisation of the SVPWM scheme is grounded in the fact that the DC-link voltage V_{DC} is used to calculate the duty cycles for the three phase legs. This is proved by the fact that the amplitudes of the switching vectors U_0 through U_7 are directly influenced by the DC-link voltage. Therefore, any deviation in the DC-link voltage will forthwith influence the construction of the vectors required to realise the $\overrightarrow{\mathbf{V}^*_{\alpha\beta}}$ vector. For example, if the DC-link voltage would slightly increase momentarily, the calculated duty cycles will be slightly less than what is expected (under normal DC-link voltage conditions) to accurately realise the $\overrightarrow{\mathbf{V}^*_{\alpha\beta}}$ vector. This emphasises the fact that the calculation of the duty cycles will compensate for DC-link deviations to realise an accurate $\overrightarrow{\mathbf{V}^*_{\alpha\beta}}$ vector and consequently provide the crucial decoupling of the DC-link voltage which will greatly improve the dynamic stiffness and general performance of the digital control strategies implemented in the converter.

3.3 Park's Transformation

The stationary reference frame produced by the Clarke transformation provides numerous advantages such as independence of the $\alpha-$ and $\beta-$voltages and an increased output voltage range when compared with normal carrier-based PWM. Instead of mapping the three-phase voltages to this stationary reference frame it is possible to map them to a rotating reference frame. Park's transform, also known as the Direct-Quadrature-Zero (DQ0) transform, maps the three-phase voltages onto a two-axis synchronous rotating reference frame [31] rotating at a coordinate angle θ defined as:

$$\theta = \int_0^t \omega dt + \theta_0 \tag{3.7}$$

where ω is the frequency of the output voltage. When ω is constant the rotation coordinate angle becomes $\theta = \omega t$. Employment of this transformation results in the three phase voltages being mapped to a dynamic coordinate system which is accomplished by utilising equation (3.8):

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\omega t) & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \\ -\sin(\omega t) & -\sin\left(\omega t - \frac{2\pi}{3}\right) & -\sin\left(\omega t + \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \tag{3.8}$$

The homopolar component V_0 is included for the sake of completeness, but will be zero in the case of balanced symmetrical systems. The $\alpha\beta$ reference frame is a static coordinate system but the Park transform, however, makes it possible to rotate around this stationary reference frame at the angular velocity ω. It is common in UPS applications that the output frequency remains constant. Consequently, the rotating coordinate system produced by the Park transform rotates at the angular velocity ω around the $\alpha\beta$ coordinate system. Due to the stationary reference frame being a static coordinate system, the direct-quadrature (DQ) dynamic coordinate system can be transformed directly from the stationary reference frame by using the following simple equation:

$$\mathbf{V}_{dq} = \mathbf{T}_{dq} \mathbf{V}_{\alpha\beta 0}$$

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta & 0 \\ -\sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \\ V_0 \end{bmatrix} \tag{3.9}$$

with $\theta = \omega t$ .Notice that the transformation matrix $\boldsymbol{T}_{dq}$ forms an orthogonal matrix since $\mathbf{T}_{dq}^{-1} = \mathbf{T}_{dq}^{T}$, which again signifies independence between the direct- and quadrature voltages V_d and V_q. The inverse dq transformation is therefore obtained:

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_0 \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta & 0 \\ \sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} \tag{3.10}$$

It is clear that the angular velocity at which the DQ reference frame rotates is equal to the fundamental frequency of the three-phase system. The immediate advantage offered by using the Park transform is provided by this synchronisation which ensures that the voltage vector remains stationary in the rotating reference. Subsequently, the quasi DC characteristics of the stationary voltage vectors result in lower bandwidth requirements of the system's controller, which irrefutably improves the performance and effectiveness of PI controllers.

The performance of classical control strategies such as PI controllers are affected by non-negligible tracking errors of the controller's output signal with respect to the reference signal. If the Park transform is utilised, it

efficaciously results in the control of a constant signal which subsequently makes it theoretically possible to achieve zero tracking error, thanks to the integral characteristics of the PI controller. The relationship between the phase voltages, the stationary reference frame and the rotational reference frame is shown in Figure 3-6. It shows that the DQ reference frame rotates at the same angular velocity as the voltage vector and that the vector in the DQ reference frame is effectually equal to the vector in the $\alpha\beta$ reference frame. A mentionable difference between vectors $\overrightarrow{\mathbf{V}^*_{\alpha\beta}}$ and $\overrightarrow{\mathbf{V}^*_{dq}}$ is the respective coordinate systems in which they operate.

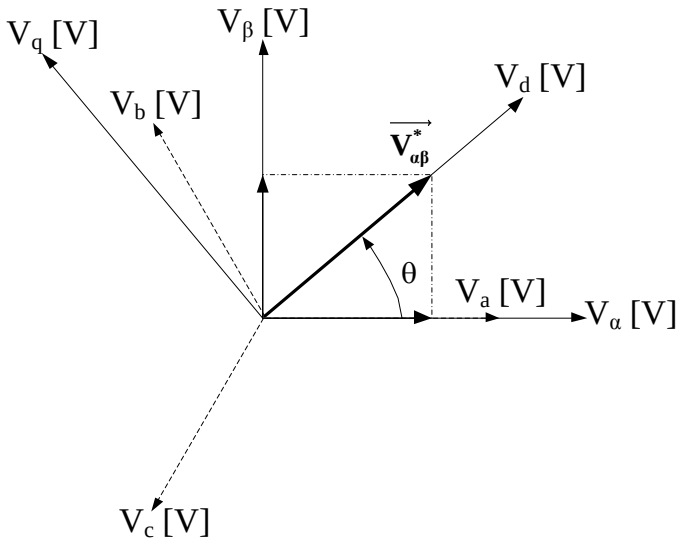

Figure 3-6: Rotational Reference Frame

To ensure synchronisation of the rotational reference frame with the vector $\overrightarrow{\mathbf{V}^*_{dq}}$, it is evident that the d-axis remains collinear with the $\overrightarrow{\mathbf{V}^*_{dq}}$ vector. In other words, it has the same angle and angular velocity. When the rotational reference frame is utilised in the control of the converter it is for this reason desirable to ensure that the d-component of $\overrightarrow{\mathbf{V}^*_{dq}}$ equals the magnitude of the reference signal and simultaneously also drives the q-component of $\overrightarrow{\mathbf{V}^*_{dq}}$ to zero.

It is important to point out that the matrix elements of the Park transformation $\mathbf{T}_{dq}$ are time variant. The implication of using the Park transform of the three phase system is that the system's dynamics can, to a large extent, be affected by this time variant characteristic of $\mathbf{T}_{dq}$ [31]. A controller that is subsequently designed in the DQ coordinate system is therefore equivalent to a stationary frame controller that does not exert the same frequency response of a similarly designed controller based on the $\alpha\beta$ reference frame.

3.4 Dead Time Compensation

Switching devices such as IGBTs and MOSFETs are connected in series to constitute a phase leg in a converter. These practical switching devices have inherent non-zero turn-on and turn-off times. The consequence of these non-zero transition times is that an immediate change of the switch's state is not possible. Figure 3-7 shows the complementary switching signal g_t^* and g_b^* for the respective top and bottom IGBT in a commonly used converter leg.

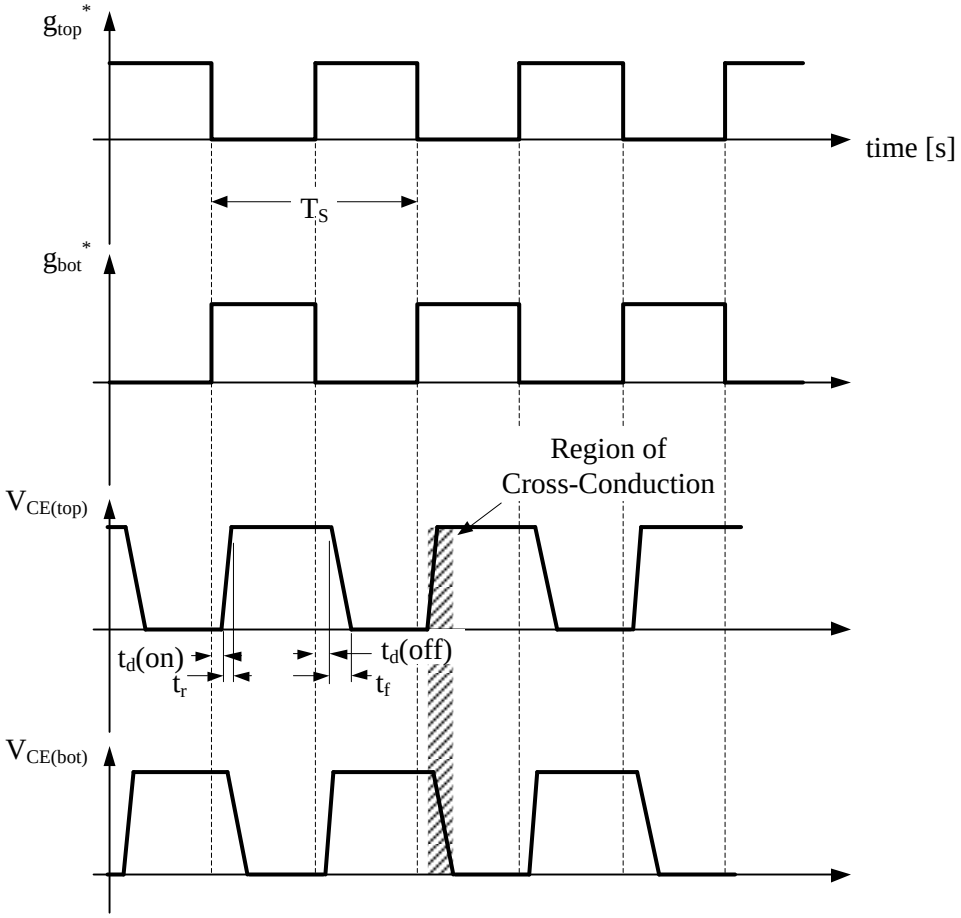

Figure 3-7: Ideal Switching versus Actual Transition of Power Switch

It can be seen that the corresponding states of the actual top and bottom IGBT contain additional turn-on, turn-off and rise- and fall-times due to the physical characteristics of the IGBT. Other gate driven switching devices will also exhibit - to a certain extent - similar transitional behaviour.

Neglecting these non-zero transition times will result in cross-conduction between the voltage rails (pointed out in Figure 3-7) and an obvious shoot-through of high magnitude currents when both switching devices are on [1] [25]. It is common practice to include a time delay when an IGBT is turned on with the aim of preventing this situation from occurring. The time that is required to prevent the simultaneous conduction of both switches, is known as the blanking time.

3.4.1 Principle of Operation

The effect of the blanking time is best described by considering a singular phase leg, such as the one shown in Figure 3-8. Through inspection of Figure 3-8 it is evident that when both switches Q_{top} and Q_{bottom} are turned off the polarity of the output voltage is dependent on the direction of the output current. In other words, the converter output voltage is dependent on the direction of the output current during the blanking time.

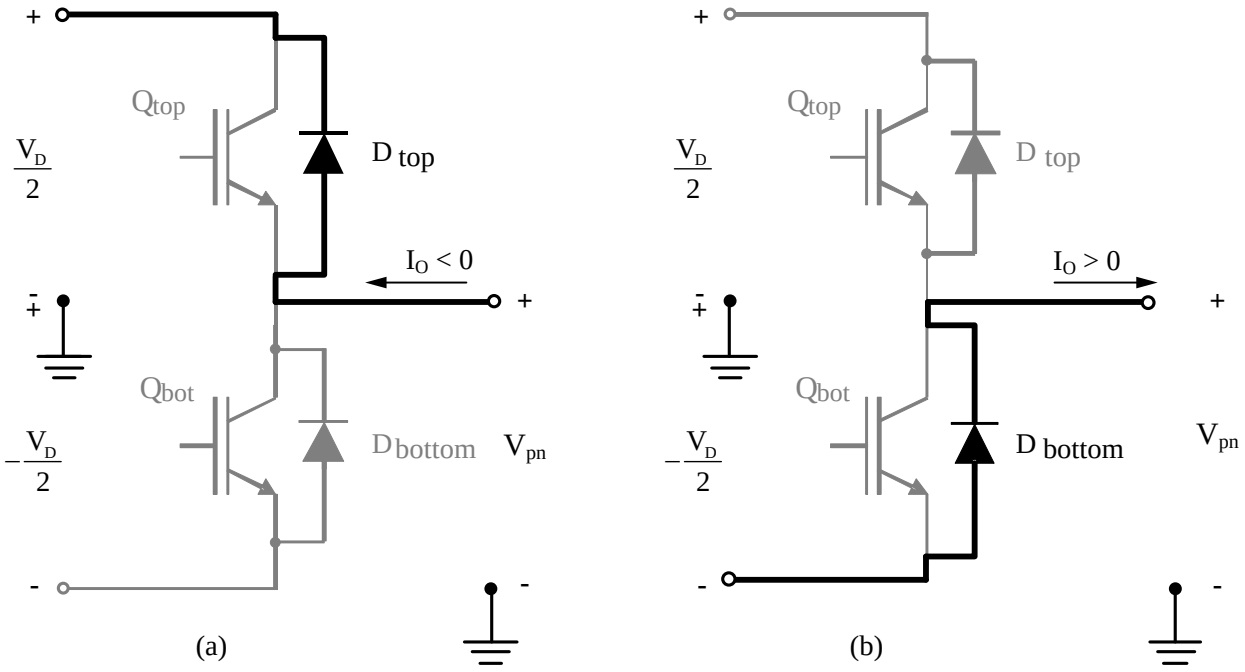

Figure 3-8: Current Flow during Dead Time when Output Current is (a) Negative and (b) Positive

The current I_O flowing out of the converter is defined as positive. Figure 3-8 shows that when the output current is negative the top diode will be on. Subsequently, the converter output voltage will equal $\frac{V_d}{2}$. Similarly, when the output current is positive D_{bottom} will be on and the output voltage will be $-\frac{V_d}{2}$.

Assume that the rise and fall times are negligible in comparison with the turn-on and turn-off times. Figure 3-9 shows the output voltage of a phase leg over two switching cycles. The reference gating signals for the top and bottom switch are respectively indicated as g^*_{top} and g^*_{bottom}. The actual gating signals are subsequently defined as g_{top} and g_{bottom}. It is obvious that during normal switching operation either D_{top} or Q_{bottom} will be conducting when the output current is negative. As a resultant the output voltage will either equal $\frac{V_d}{2}$ or $-\frac{V_d}{2}$. In a similar manner when the output current is positive either D_{bottom} or Q_{top} will be conducting, resulting in the output voltage equalling $\frac{V_d}{2}$ or $-\frac{V_d}{2}$ respectively.

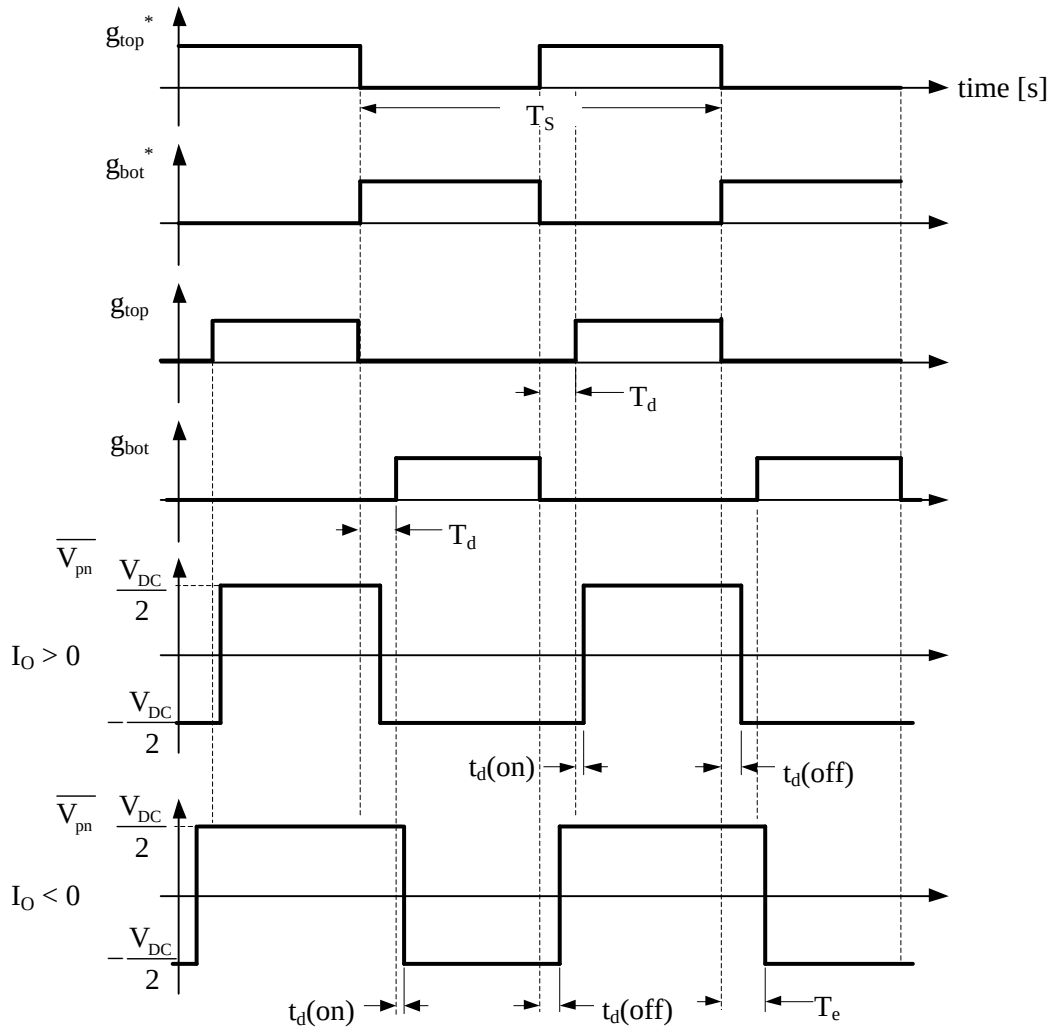

Figure 3-9: Illustrating Output Voltage Corruption due to Blanking Time

Notice that in the case where the output current is positive the average output voltage is less than the reference voltage command. This is due to the top IGBT being on for a duration that is shorter than what is required. Conversely, when the output current is negative the top IGBT will be on for longer than what is commanded. Consequently, the average output voltage is larger than the reference voltage.

The corruption of the output voltage that results from the differences between the actual output voltage and the reference is depicted in Figure 3-10. Examination of Figure 3-10 (a) shows that the actual output voltage is severely corrupted at the points where the output current changes polarity. Additionally, note the phase distortion of the actual output voltage with respect to the ideal reference voltage. Figure 3-10 (b) further clarifies the deviation experienced in the output voltage when directly compared to the reference voltage.

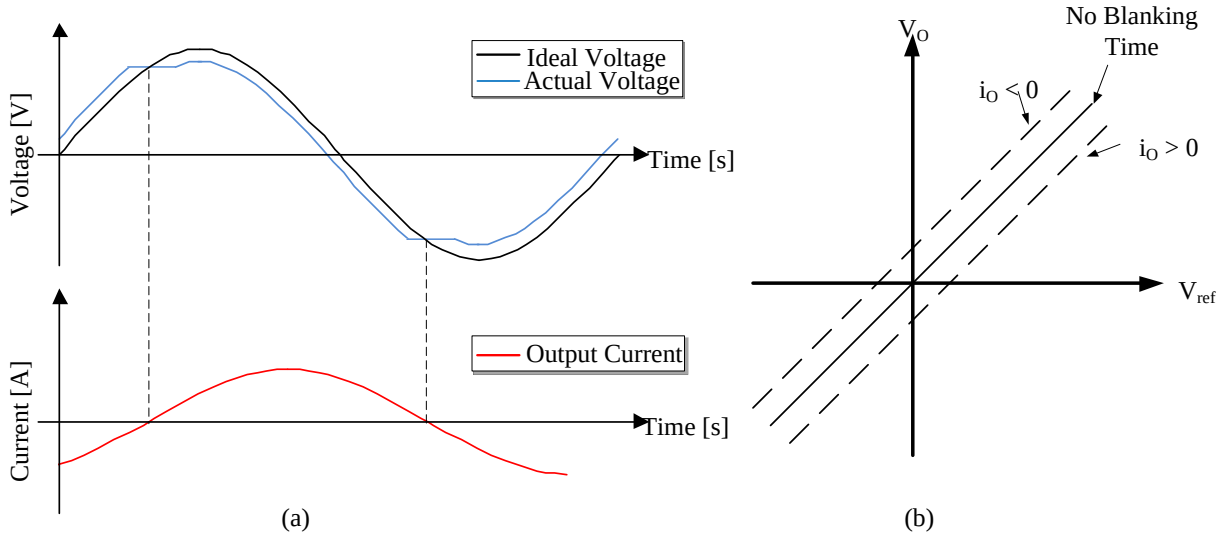

Figure 3-10: Corruption of Output Voltage due to Dead Time (a) in Time Domain and (b) versus the Input Reference Voltage

It is therefore firmly established that a distinct error is made due to the blanking time ($T_{blanking}$) and the turn-on ($T_{d(on)}$) and turn-off ($T_{d(off)}$) times. In general, the duration of dead time that results in the error that is made due to these times is defined as:

$$T_e = T_{blanking} + T_{d(on)} - T_{d(off)} \tag{3.11}$$

Upon further inspection of Figure 3-9, the duration that the top IGBT is active, equals

$$t_p^+ = t_p^* - T_e \qquad \text{when } I_O > 0$$
$$t_p^+ = t_p^* + T_e \qquad \text{when } I_O < 0$$

Generally speaking, the duration that the top IGBT of phase leg *p* is active can be defined by equation (3.12) in terms of the polarity of the output current for the phase leg *p*:

$$t_p^+ = t_p^* - \text{sgn}(i_p) T_e \qquad p = a, b, c, ..., n \tag{3.12}$$

The average output voltage is consequently expressed as:

$$\begin{aligned} \overline{v_{pn}} &= \frac{V_d}{2}\frac{t_p^+}{T_S} + \frac{-V_d}{2}\left(1 - \frac{t_p^+}{T_S}\right) \\ &= V_d\left(\frac{t_p^+}{T_S} - \frac{1}{2}\right) \end{aligned} \tag{3.13}$$

Oh et al [40] proposed a compensation method to reduce the corrupting effect of blanking time on the output. De Wit [41] adapted this proposal with the objective of implementation in a line-interactive UPS. Analysis on the dead time is divided into three modes. The division of these modes is clarified in Figure 3-11 which shows the per-unit reference duty cycle over one full period of the fundamental signal.

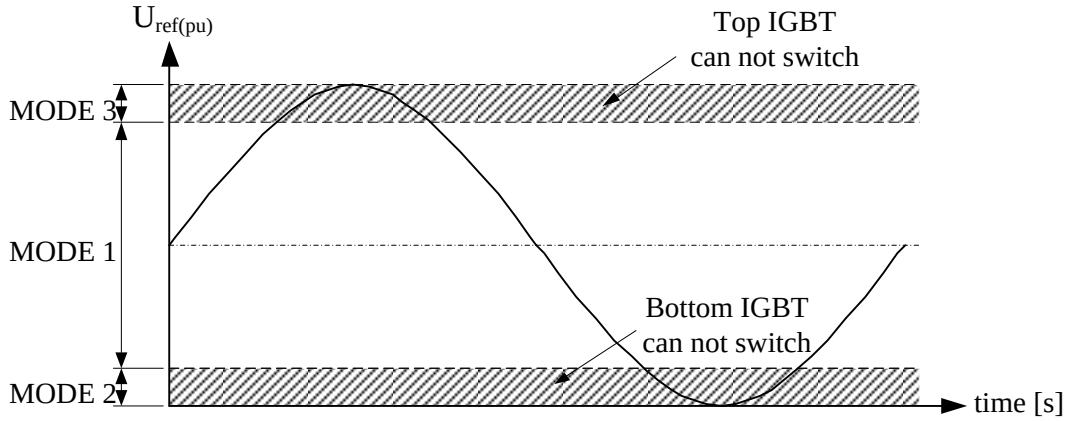

Figure 3-11: Mode Definitions used in Dead Time Compensation

The first mode of operation is when the reference duty cycle is long enough to ensure that a gating pulse will be observed by the IGBT. The second mode represents the case where the reference command is so small that it results in a gating pulse that is narrower than the dead time. The result is that a gating signal is not observed by the top IGBT. Finally, the third mode of operation is when the reference command is so large that the consequential complementary gating pulse of the bottom IGBT is narrower than the dead time. Consequently, the bottom IGBT is unable to observe a gating signal. Neither Oh et al nor De Wit was able to identify this third mode that caused voltage corruption. Consequently, their proposed dead time compensation method was improved upon in collaboration with Welgemoed [42].

MODE 1

It is only necessary to compensate for the errors that result from dead time in this mode of operation. Suppose $I_a > 0$, $I_b > 0$ and $I_c < 0$. The time the top IGBT of each phase will be on is expressed as follows:

$$\begin{aligned} t_a^+ &= t_a^* - T_e \\ t_b^+ &= t_b^* - T_e \\ t_c^+ &= t_c^* + T_e \end{aligned} \tag{3.14}$$

Subsequently, the average output voltages of the three phases can be defined according to equation (3.15):

$$\begin{aligned} \overline{v_{an}} &= V_d \left(\frac{t_a^* - T_e}{T_S} - \frac{1}{2} \right) \\ \overline{v_{bn}} &= V_d \left(\frac{t_b^* - T_e}{T_S} - \frac{1}{2} \right) \\ \overline{v_{cn}} &= V_d \left(\frac{t_c^* + T_e}{T_S} - \frac{1}{2} \right) \end{aligned} \tag{3.15}$$

Consequently, the line-to-line voltages are found to be:

$$\begin{aligned}
\overline{v_{ab}} &= V_d\left(\frac{t_a^* - t_b^*}{T_S}\right) = \overline{v_{ab}^*} \\
\overline{v_{bc}} &= V_d\left(\frac{t_b^* - t_c^* - 2T_e}{T_S}\right) = \overline{v_{bc}^*} - V_d\left(\frac{2T_e}{T_S}\right) \\
\overline{v_{ca}} &= V_d\left(\frac{t_c^* - t_a^*}{T_S}\right) = \overline{v_{ca}^*} + V_d\left(\frac{2T_e}{T_S}\right)
\end{aligned} \tag{3.16}$$

A general observation of the average line-to-line voltages is that no dead time distortion is observed between phases with the same output current polarity. Furthermore, the distortion can be mitigated by adding a compensation term to the reference signal. Consequently, the duration that the top IGBTs of the respective phases are on is expressed as:

$$\begin{aligned}
t_a^{comp} &= t_a^* + T_e \\
t_b^{comp} &= t_b^* + T_e \\
t_c^{comp} &= t_c^* - T_e
\end{aligned} \tag{3.17}$$

In general, the compensation term in MODE1 for phase p is given by equation (3.18):

$$t_p^{comp} = t_p^* + \mathrm{sgn}\left(I_p\right)T_e \tag{3.18}$$

where I_p is the output current for phase p.

MODE 2

Next consider the situation where the reference command is so small that the gating signal will be shorter than the dead time. Suppose that $I_a > 0$, $I_b > 0$ and $I_c < 0$ and that the gating signal for the top IGBT of phase A is a very narrow pulse. Consequently, the durations that the respective top IGBTs are conducting are found to be:

$$\begin{aligned}
t_a^+ &= 0 \\
t_b^+ &= t_b^* - T_e \\
t_c^+ &= t_c^* + T_e
\end{aligned} \tag{3.19}$$

The subsequent line voltages are therefore expressed:

$$\begin{aligned}
\overline{v_{ab}} &= \overline{v_{ab}^*} - V_d\left(\frac{t_a^* - T_e}{T_S}\right) \\
\overline{v_{bc}} &= \overline{v_{bc}^*} - V_d\left(\frac{2T_e}{T_S}\right) \\
\overline{v_{ca}} &= \overline{v_{ca}^*} + V_d\left(\frac{t_a^* + T_e}{T_S}\right)
\end{aligned} \tag{3.20}$$

To compensate for these errors in the line voltages, the compensation durations are given as:

$$\begin{aligned}
t_b^{comp} &= t_b^* - \left(t_a^* - T_e\right) \\
t_c^{comp} &= t_c^* - \left(t_a^* + T_e\right)
\end{aligned} \tag{3.21}$$

In this case the reference duty cycle for phase A is shorter than the dead time and consequently results in no gating signal driving the top IGBT. The compensation terms found in equation (3.21) not only correct the line voltage errors of their respective phases, but also correct the voltage error on phase A.

Consider a similar situation where the output currents are again $I_a > 0$, $I_b > 0$ and $I_c < 0$, but that the gating signal for the top IGBT of phase C is now a very narrow pulse. Under these conditions, the duration that the top IGBTs are conduction is given as:

$$\begin{aligned} t_a^+ &= t_a^* - T_e \\ t_b^+ &= t_b^* - T_e \\ t_c^+ &= 2T_e \end{aligned} \tag{3.22}$$

The subsequent line voltages are now found to be:

$$\begin{aligned} \overline{v_{ab}} &= \overline{v_{ab}^*} \\ \overline{v_{bc}} &= \overline{v_{bc}^*} + V_d\left(\frac{t_c^* - 3T_e}{T_S}\right) \\ \overline{v_{ca}} &= \overline{v_{ca}^*} - V_d\left(\frac{t_c^* - 3T_e}{T_S}\right) \end{aligned} \tag{3.23}$$

The amount of time required to compensate for the line voltage errors is subsequently given as:

$$\begin{aligned} t_a^{comp} &= t_a^* - \left(t_c^* - 3T_e\right) \\ t_b^{comp} &= t_b^* - \left(t_c^* - 3T_e\right) \end{aligned} \tag{3.24}$$

In general, when the gating signal is a narrow pulse in a phase *p* where $I_p > 0$, then the amount of time required in the other phases to compensate for the dead time is given as:

$$t_p^{comp} = \begin{cases} t_p^* - \left(t_{narrow}^* - T_e\right) & \text{when } I_p > 0 \\ t_p^* - \left(t_{narrow}^* + T_e\right) & \text{when } I_p < 0 \end{cases} \tag{3.25}$$

where t_{narrow}^* refers to the duration of the gating signal on the phase where the narrow pulse occurs. Likewise, if there is a narrow pulse in the phase where $I_p < 0$, then:

$$t_p^{comp} = \begin{cases} t_p^* - \left(t_{narrow}^* - 3T_e\right) & \text{when } I_p > 0 \\ t_p^* - \left(t_{narrow}^* - T_e\right) & \text{when } I_p < 0 \end{cases} \tag{3.26}$$

MODE 3

In this mode of operation the duty cycle is very large. The result is that the gating signal of the bottom IGBT is a narrow pulse which is shorter than the dead time. Consequently, no gating signal is observed on the bottom IGBT.

Suppose the output current conditions are that $I_a > 0$, $I_b > 0$ and $I_c < 0$ and that a narrow pulse exists in the gating signal to the bottom IGBT of phase A. The durations that the top IGBTs are on can be expressed as:

$$\begin{aligned} t_a^+ &= T_S - 2T_e \\ t_b^+ &= t_b^* - T_e \\ t_c^+ &= t_c^* + T_e \end{aligned} \tag{3.27}$$

The subsequent line voltages are:

$$\begin{aligned} \overline{v_{ab}} &= \overline{v_{ab}^*} - V_d\left(\frac{t_a^* - T_S + T_e}{T_S}\right) \\ \overline{v_{bc}} &= \overline{v_{bc}^*} - V_d\left(\frac{2T_e}{T_S}\right) \\ \overline{v_{ca}} &= \overline{v_{ca}^*} + V_d\left(\frac{t_a^* - T_S + 3T_e}{T_S}\right) \end{aligned} \tag{3.28}$$

The amount of time required to compensate for the line voltage errors are subsequently given as:

$$\begin{aligned} t_b^{comp} &= t_b^* - \left(t_a^* - T_S + T_e\right) \\ t_c^{comp} &= t_c^* - \left(t_a^* - T_S + 3T_e\right) \end{aligned} \tag{3.29}$$

Suppose now that $I_a < 0$, $I_b > 0$ and $I_c < 0$ and again that a narrow pulse now exists in the gating signal to the bottom IGBT of phase A. The durations that the top IGBTs are on can similarly be determined:

$$\begin{aligned} t_a^+ &= T_S \\ t_b^+ &= t_b^* - T_e \\ t_c^+ &= t_c^* + T_e \end{aligned} \tag{3.30}$$

The corresponding line voltages in this mode of operation are found to be:

$$\begin{aligned} \overline{v_{ab}} &= \overline{v_{ab}^*} - V_d\left(\frac{t_a^* - T_e - T_S}{T_S}\right) \\ \overline{v_{bc}} &= \overline{v_{bc}^*} - V_d\left(\frac{2T_e}{T_S}\right) \\ \overline{v_{ca}} &= \overline{v_{ca}^*} + V_d\left(\frac{t_a^* + T_e - T_S}{T_S}\right) \end{aligned} \tag{3.31}$$

Consequently, the required compensation terms to correct the errors in the line voltages are defined as:

$$\begin{aligned} t_b^{comp} &= t_b^* - \left(t_a^* - T_e - T_S\right) \\ t_c^{comp} &= t_c^* - \left(t_a^* + T_e - T_S\right) \end{aligned} \tag{3.32}$$

In general, when the gating signal is a narrow pulse in a phase *p* where $I_p > 0$, then the amount of time required in the other phases to compensate for the dead time is given as:

$$t_p^{comp} = \begin{cases} t_p^* - \left(t_{narrow}^* - T_S + T_e\right) & \text{when } I_p > 0 \\ t_p^* - \left(t_{narrow}^* - T_S + 3T_e\right) & \text{when } I_p < 0 \end{cases} \tag{3.33}$$

Likewise, when the gating signal is a narrow pulse in a phase *p* where $I_p < 0$, then the compensated amount of time required in the other phases is found to be:

$$t_p^{comp} = \begin{cases} t_p^* - \left(t_{narrow}^* - T_e - T_S \right) & \text{when } I_p > 0 \\ t_p^* - \left(t_{narrow}^* + T_e - T_S \right) & \text{when } I_p < 0 \end{cases} \tag{3.34}$$

The above dead time compensation method is capable of mitigating the error made in the output voltage due to the blanking time. It is however important to take note that the amount of time that is compensated is dependent on the magnitude of the current through the IGBT. It is a well-known fact that the transitional times ($t_{d(on)}$, $t_{d(off)}$, t_r and t_f) can greatly deviate with the current through the IGBT. In fact, this variable characteristic of the transition times is well documented in the datasheet of every IGBT, MOSFET and other switching devices. For this reason, it is recommended to define a dead time T_e value for currents across the whole current spectrum to which the IGBT is capable.

Although the proposed dead time compensation method is capable of mitigating errors made due to the blanking time, it is important also to focus on the detrimental effects the blanking time has on the output voltage at the point of zero-crossing. The output distortion occurs due to the non-linear phenomenon that occurs on the average inductor current when it crosses through zero. The non-linear effect is caused by the blanking time and is highly dependent on the polarity of the average inductor current. A joint collaboration between Hobbs and Koeslag in [43] proposed an analytical characterisation of the blanking time at the zero-crossing region of the inductor current. A method was developed to counteract the detrimental effects the blanking time has at these zero-crossing regions and is herewith implemented to further augment the dead time compensation method proposed thus far.

Hobbs identified three regions in the inductor current for the analytical characterisation of the dead time. These regions are identified in Figure 3-12 and are defined as Region A, B and C. Region A and C are synonymous with the current being distinctly positive or negative. In these regions the output voltage is either larger or smaller than required by the voltage indicated by the reference signal. These regions of operation will not be further discussed since the error is already being compensated by the method proposed by Oh et al [40].

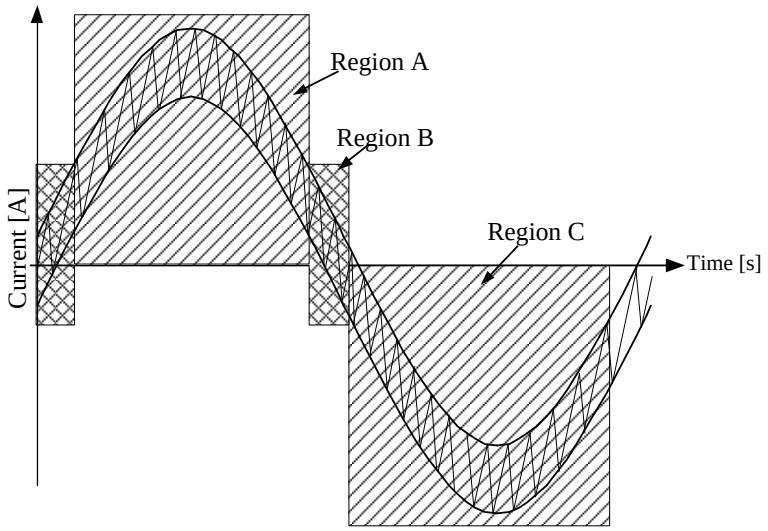

Figure 3-12: Defining Inductor Current Regions

The region of interest is region B where the inductor current changes polarity. It is during the period that the current is in this region that the blanking time is implemented and therefore means that neither the top nor bottom IGBT is conducting. It can thus be deducted that only the anti-parallel connected freewheeling diodes provide a conduction path for the inductor current. Hobbs et al [43] identified that these diodes have a reverse recovery time where the excess charge carriers need to be swept out of the biasing area in the diode such that it can switch off completely. Figure 3-13 shows how the converter output voltage is distorted during the blanking time. The finite reverse recovery time of the power diodes causes the inductor current to oscillate around zero to sweep out the excess charge carriers from the biasing threshold of the diode. The subsequent result is the corruption of the converter voltage.

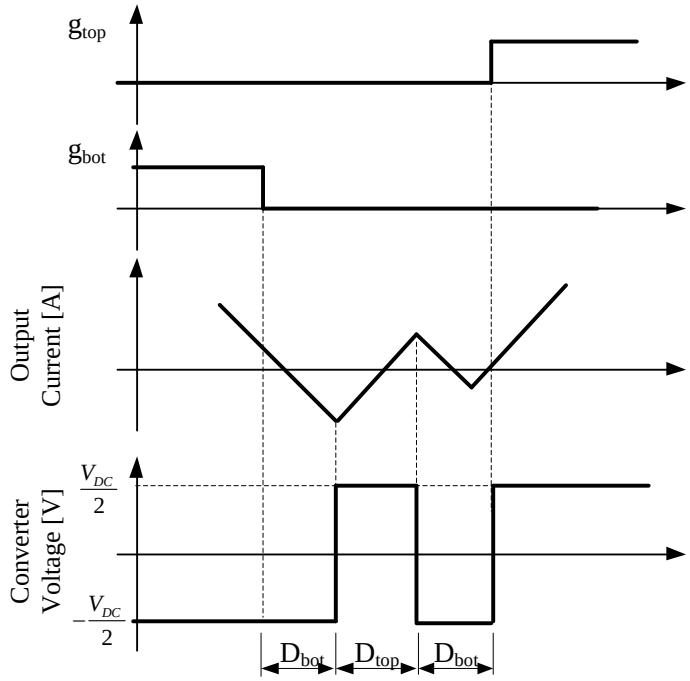

Figure 3-13: Waveform Distortion during Region B

The objective is to minimise the degree to which the output voltage is corrupted by the reverse recovery of the diodes during the blanking time. To achieve this it is required to drive the inductor current to zero at the point of zero crossing. While so doing the current through the diode will be zero and the diode will not go into reverse recovery since all the charge carriers are already zero.

The compensation method proposed by Oh et al effectively results in the adding or subtracting of a certain amount of voltage to the reference voltage depending on the direction of the output current. In an attempt to drive the output current to zero at the point of zero-crossing the reference voltage is multiplied by a linear slope which is dependent on the polarity of the output current. The reference voltage that results from these compensations is shown in Figure 3-14. A hysteresis band is defined around zero where the linear slope is implemented. The hysteresis band ensures that the linear slope produces a gradual decay of the output voltage towards zero. Consequently, a minimal distortion of the average inductor current is ensured for the duration of the blanking time.

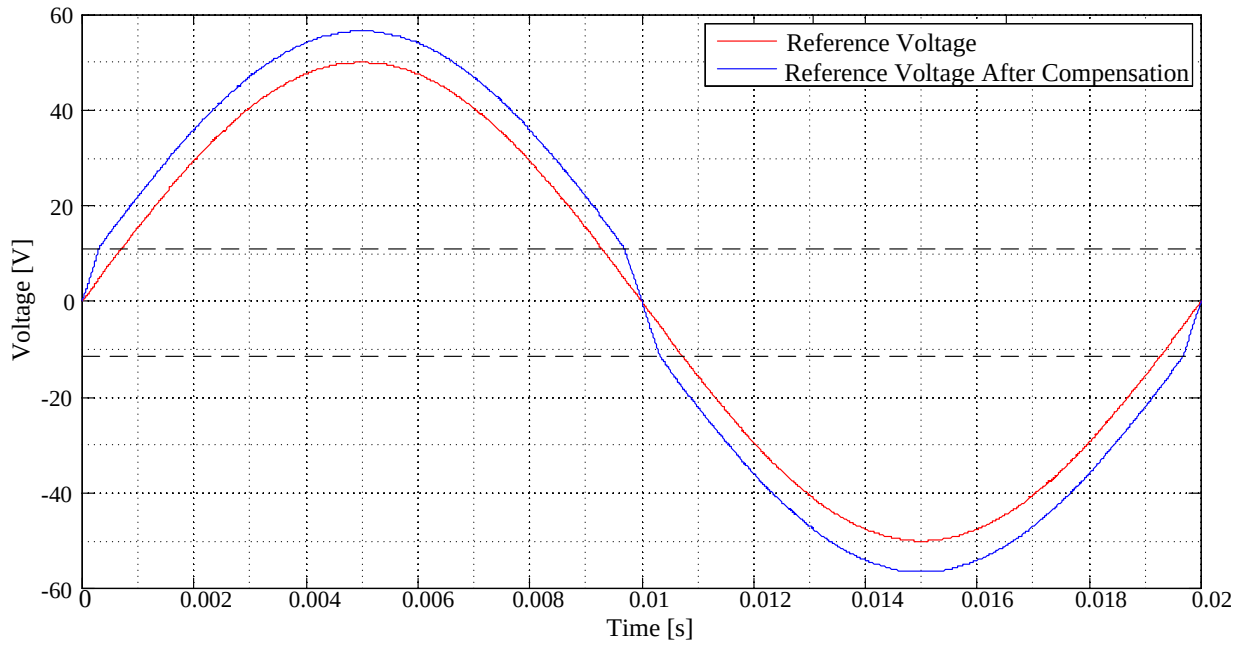

Figure 3-14: Resulting Modified Output Voltage due to Dead Time Compensation

Implementation of the above-mentioned dead time compensation methods will ensure that the actual output voltage is able to track the initial reference voltage more accurately. Since blanking time distorts the output voltage, this results in the degradation of the THD of the voltage produced by a switching converter. The elimination of the effects of blanking time on the output voltage provides the further advantage of greatly improving the THD of the output voltage.

3.4.2 Simulated Performance

To demonstrate the advantages provided by the dead time compensator, a simulation was conducted to gauge its performance. The system shown in Figure 3-15 is a three-phase VSI model driving a symmetrical balanced load. The system is open-loop controlled and employs SVM to provide 200 A line-to-line current to the load. It has a switching frequency of f_S = 5 kHz and blanking time of 5 µs.

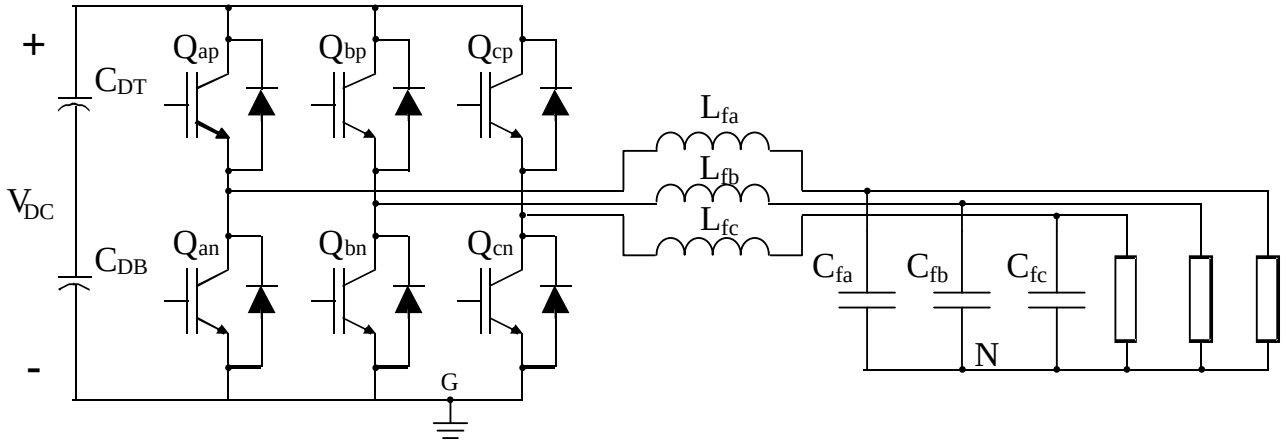

Figure 3-15: Three-Phase VSI Simulation Model

The system was initially simulated without any dead time compensation. Thereafter, the system was again simulated with exactly the same system parameters but with the proposed dead time compensation method included. Figure 3-16 shows the alpha converter reference- and output voltages along with the corresponding output alpha current.

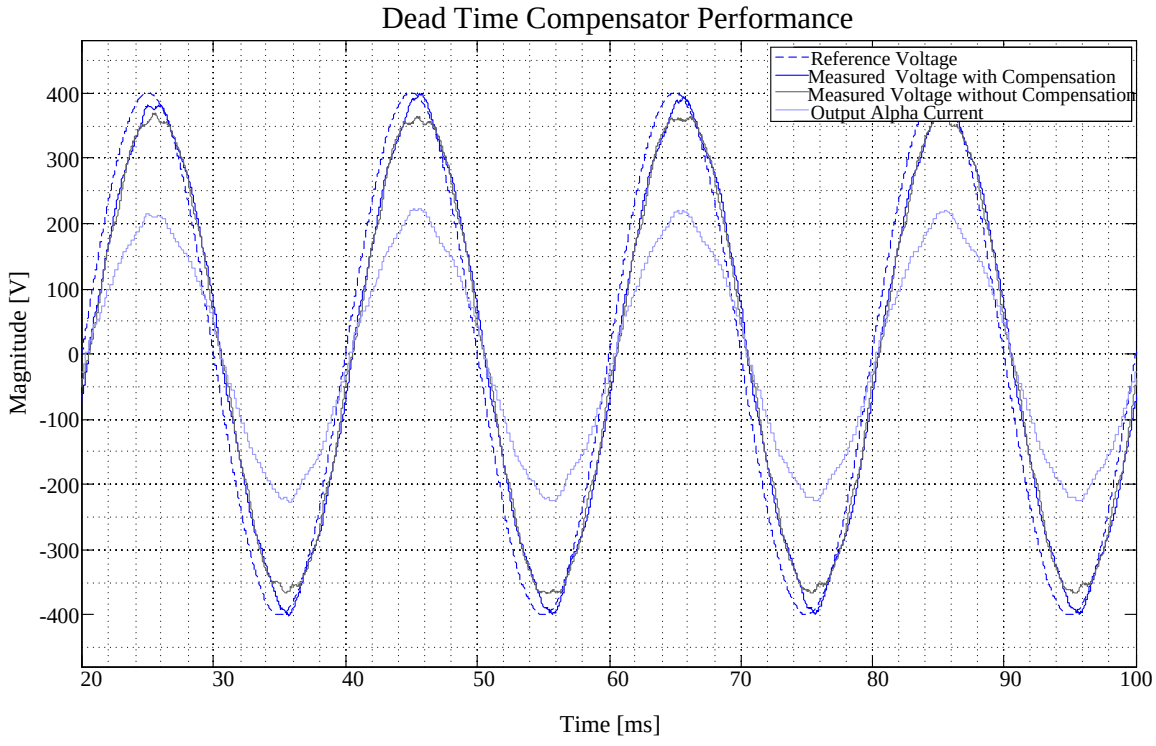

Figure 3-16: Simulation of Dead Time Compensator Performance

The tracking errors of the measured output voltage with respect to the reference voltage are a result of no closed-loop controller being active to remove the said errors. Apart from these tracking errors on the output voltage, it can be seen that the output voltage from the system that employs the dead time compensator provides a more accurate transient response. The voltage magnitude more accurately follows the reference voltage. On the other hand, the system that does not compensate for the dead time between the top and bottom IGBTs produces an output voltage magnitude that is considerably less than the reference voltage. This is completely understandable when considering that dead time effectively reduces that average voltage.

In conclusion it can be said with great certainty that the proposed compensation method is very effective at compensating for the errors that are caused by dead time in a converter.

3.5 Conclusion

In this chapter the derivation of the Clarke transform was discussed. The advantages provided by this transform and how it simplifies the control of three-phase converters, was discussed. Thereafter, the Park transform was similarly discussed. How to obtain the direct and quadrature voltage by directly transforming the three phase voltages from phase A, B and C was also shown. A transform was also given to obtain the direct and quadrature voltages from the alpha- and beta equivalent voltage of the three-phase converter.

The detrimental effect of dead time was discussed and it was shown how its implementation can greatly corrupt the voltage produced by a converter phase leg. This served as a motivation to derive a means of compensation to counteract these detrimental corrupting effects. Literature was reviewed and a pulse-based dead time compensation method was derived based on this literature. The method proposed in the literature did not fully compensate for dead time corruption under all possible situations. The proposed method was therefore improved.

Furthermore, an average-based dead time compensation method was also included to operate in conjunction with the pulse-based compensator. This compensation technique was analysed and implemented.
A simulation was done to illustrate the effectiveness of the proposed dead time compensator and the advantages it provides in the switching converter.

CHAPTER 4

CONTROL OF THE ACTIVE RECTIFIER

4 CONTROL OF THE ACTIVE RECTIFIER

4.1 Introduction

The line-interactive UPS is a complex system which operates in different modes as discussed in section 1.3.3. For instance, when the UPS is initialised the DC-link needs to be charged with the aim of matching with the voltage of the storage batteries. Thereafter, this DC-link needs to be continuously regulated under all conditions that the UPS might experience. Figure 4-1 shows the line-interactive UPS with the purpose of indicating the focus of this chapter.

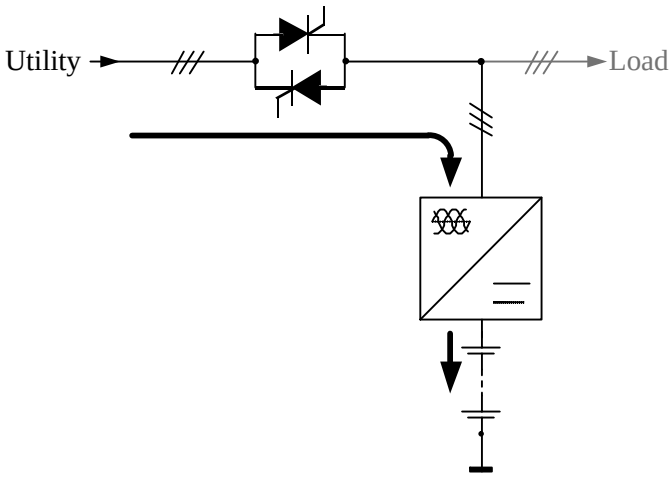

Figure 4-1: Active Rectifier of the Line-Interactive UPS

The three-phase converter functions as an active rectifier that boost converts the three-phase AC voltages to a DC voltage. The control of the line-interactive UPS when it operates as an active rectifier (or AC-DC converter), is discussed in this chapter.

4.2 Proposed Control Strategy

A double-loop control strategy is proposed with the current controller being the inner loop and the voltage controller completing the outer loop. The current controller is designed with a considerably higher bandwidth than the voltage controller. In fact, a predictive current controller is proposed which has the maximum capable bandwidth that is implementable in the converter. A single-line diagram of the active rectifier is shown in Figure 4-2 along with an elementary equivalent of the proposed double-loop control strategy.

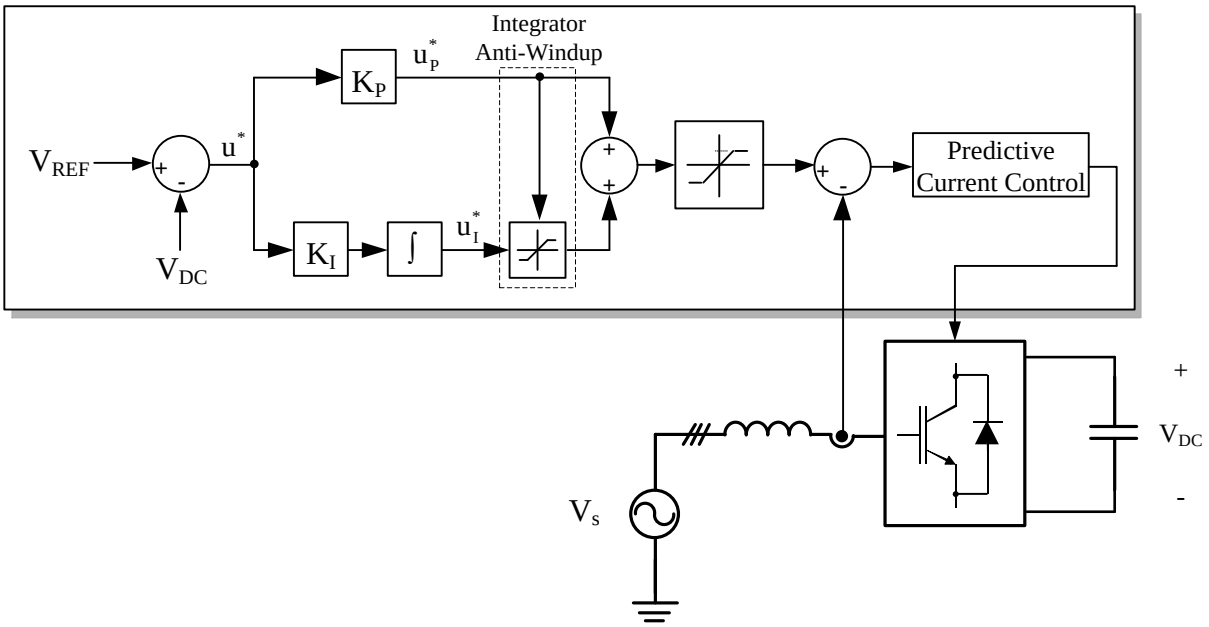

Figure 4-2: Proposed Control of the Active Rectifier

The voltage controller that is proposed is a simple proportional-integral (PI) controller that regulates the DC-link voltage, V_{DC}, of the converter. This PI controller is designed with a definably lower bandwidth with respect to the current controller which effectively results in the decoupling of the inductor current from the voltage controller. This decoupling will be discussed and proven in section 4.4.

4.3 Predictive Current Controller: A Direct Approach

4.3.1 Principle of Operation

Bester [44] proposed a strategy for the control of the inductor current of a full-bridge converter. This strategy is realised by calculating the duty cycle that is required to ensure that the average inductor current equals the reference signal at the end of the next switching period. A one cycle prediction is thus proposed. This control scheme has subsequently been adapted by [45] for implementation in a half-bridge converter. Consider the single-phase active rectifier depicted in Figure 4-3 with the inductor current defined as shown. The motivation for using a single-phase topology is based on the simplicity it provides to support the argumentation and derivation of the proposed controller.

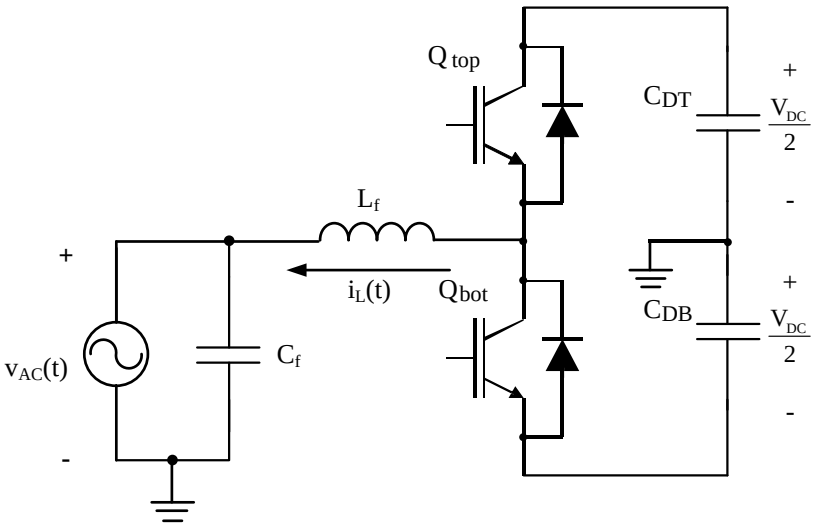

Figure 4-3: Typical Single-Phase Active Rectifier

Although the converter has four possible switching states, it is only possible to implement a bipolar switching scheme with a half-bridge topology, since it is not possible to realise the so-called zero states. This is a valid generalisation in this case since the three-phase converter that is used in the line-interactive UPS similarly utilises a bipolar switching scheme. The two equivalent converter circuits are subsequently exhibited in Figure 4-4. Note that during a particular state, the other half of the converter is effectively removed due to the centre-point of the capacitor bridge being tied to ground.

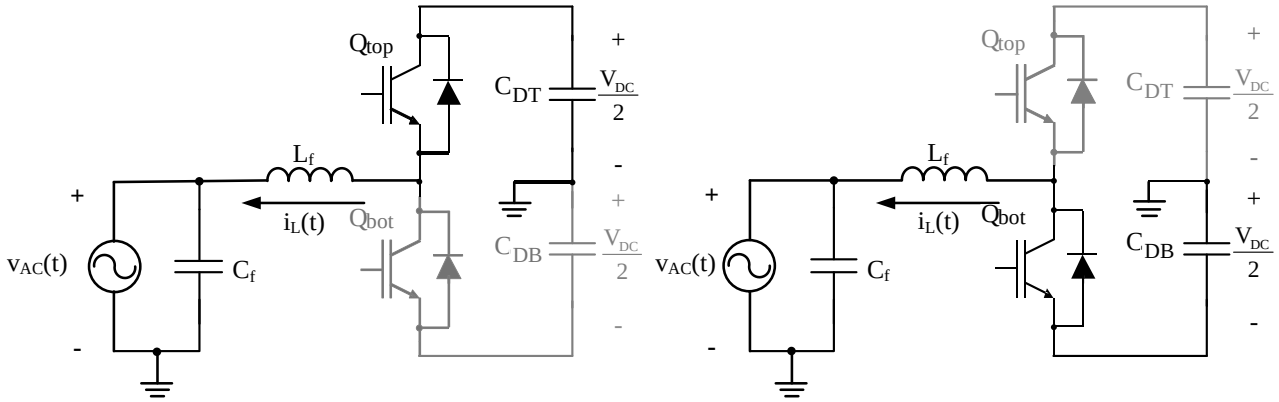

Figure 4-4: Switching States of the Active Rectifier with (a) High-Side Active and (b) Low-Side Active

In the cases when the top IGBT, Q_{top}, is conducting, the differential equation of the system is described by equation (4.1):

$$L\frac{di_L(t)}{dt} = \frac{V_{DC}}{2} - v_{AC}(t) \tag{4.1}$$

Similarly, during conduction of the bottom IGBT, Q_{bot}, the differential equation of the system is:

$$L\frac{di_L(t)}{dt} = -\frac{V_{DC}}{2} - v_{AC}(t) \tag{4.2}$$

Considering that Q_{top} is conducts for a duration $d(t)T_S$ with $d(t)$ being the duty cycle signal at the specific instant t, the inductor current is as shown in Figure 4-5:

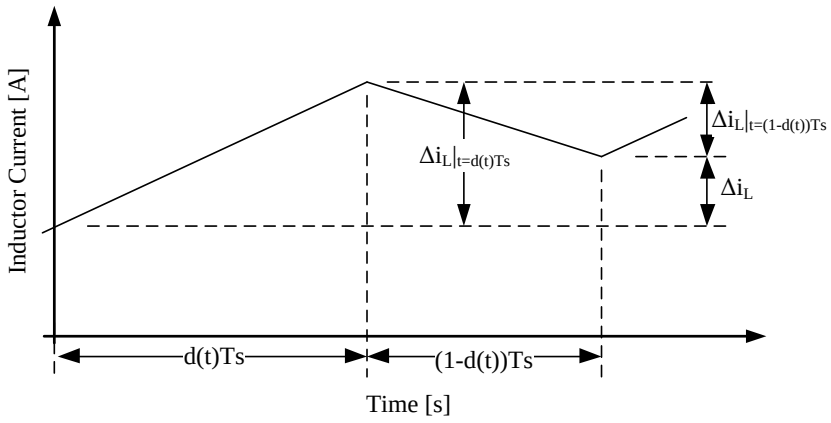

Figure 4-5: Inductor Current for One Switching Period

The change in inductor current over one switching period is thus the sum of the change in current due to Q_{top} conducting and thereafter the conduction of Q_{bot}.

$$\Delta i_L = \Delta i_L\big|_{t=d(t)Ts} + \Delta_L\big|_{t=(1-d(t))Ts} \tag{4.3}$$

Assume for the sake of this discussion that zero dead time is included and has a negligible effect. Superposition of equations (4.1) and (4.2) according to equation (4.3), and approximating $\frac{di_L(t)}{dt}$ as $\frac{\Delta i_L}{T_S}$, results in the duty cycle being defined as:

$$d(t) = \frac{L}{V_{DC}}\frac{\Delta i_L(t)}{T_S} + \frac{1}{2} + \frac{v_{AC}(t)}{V_{DC}} \tag{4.4}$$

The duty cycle in the switching converter is defined as the ratio in the duration that the top IGBT is in an active state with respect to the period of the switching frequency. Therefore, the duty cycle is a per-unit signal ranging from 0 to 1. Consequently, the duty cycle can be expressed in terms of the converter voltage $v_C(t)$, and the DC-link voltage, $\frac{V_{DC}}{2}$, for a half-bridge topology:

$$d(t) = \frac{v_c(t)}{v_{DC}(t)} + \frac{1}{2} \tag{4.5}$$

Consequently, substituting (4.5) into (4.4), the control law can be expressed for the converter voltage as follows:

$$v_C(t) = L\frac{\Delta i_L(t)}{T_S} + v_{AC}(t) \tag{4.6}$$

As discussed in section 2.4, the average of the inductor current can be obtained by sampling the measurement at the time the carrier signal is at its peak due to the symmetrical properties of DEPWM. This is indicated in Figure 4-6 at time $t = kT_S$ where k specifies the integer multiple of the sampling time T_S used

in the digital controller. The inductor current at this point in time is indicated as $i_L[k]$ and similarly $i_L[k-1]$ for the previous sample of the inductor current at $t=(k-1)T_S$.

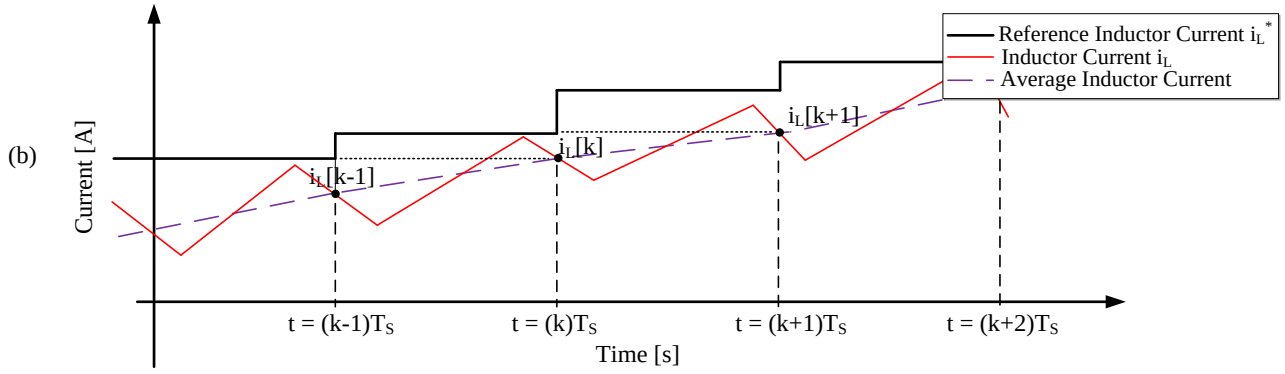

Figure 4-6: Inductor Current Signals

Since the digital controller uses these sampled values of the inductor current, the difference in inductor current $\Delta i_L(t)$ in equation (4.6) can be considered as the difference between $i_L[k]$ and $i_L[k-1]$ over the time period T_S. Subsequently, a discrete equivalent of equation (4.6) is expressed as follows:

$$v_c[k] = L\frac{i_L^*[k]-i_L[k-1]}{Ts} + v_{AC}[k] \tag{4.7}$$

Advancing the equation one switching period:

$$v_c[k+1] = L\frac{i_L^*[k+1]-i_L[k]}{Ts} + v_{AC}[k+1] \tag{4.8}$$

With the objective of expanding this control law to a three-phase system, section 3.2 pointed out that a system can effectively be controlled by applying the same control law to both the alpha- and beta-voltage vectors and still ensure independent behaviour. Therefore, the following is true:

$$\begin{aligned} v_\alpha[k+1] &= L\frac{i_L^{\alpha*}[k+1]-i_L^{\alpha}[k]}{Ts} + v_{AC}^{\alpha}[k+1] \\ v_\beta[k+1] &= L\frac{i_L^{\beta*}[k+1]-i_L^{\beta}[k]}{Ts} + v_{AC}^{\beta}[k+1] \end{aligned} \tag{4.9}$$

with the alpha- and beta-reference commands for the inductor current illustrated by $i_L^{\alpha*}[k+1]$ and $i_L^{\beta*}[k+1]$ respectively. Note that the value of the voltage $V_{AC}(t)$ at the time instant $t=(k+1)T_S$ is required to determine the converter voltages. These values are yet to be determined since the converter is a causal system and implies a subsequent prediction of this voltage. This is achieved when the converter utilises SVPWM. The signal $V_{AC}^{\beta}[k]$ and $V_{AC}^{\beta}[k]$ respectively represent the alpha- and beta- component of the space vector in the stationary reference frame (as indicated in section 3.2). If the sampling frequency is for example 5 kHz, and the reference frequency is 50 Hz, there will be 100 samples in a full period of the reference signal. As explained in section 3.2, the vector $\overrightarrow{\mathbf{V}_{AC}^{\alpha\beta}}$ in Figure 4-7 rotates through a full 360° of the stationary

reference frame for every full period cycle of the reference signal. Therefore, the vector rotates in increments of 3.6°. The space vector $\overrightarrow{\mathbf{V}_{AC}^{\alpha\beta}}[k+1]$ can subsequently be determined with simple trigonometry. This is illustrated in Figure 4-7:

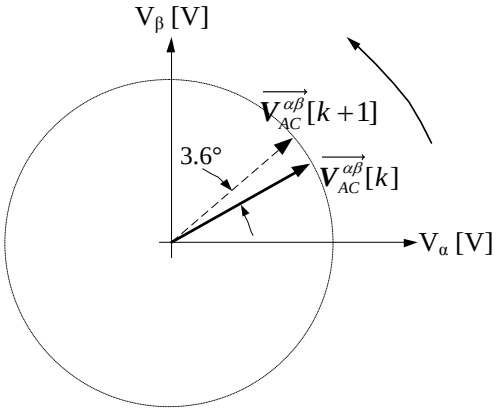

Figure 4-7: Advancing the Space Vector

The values $V_{AC}^{\alpha}[k+1]$ and $V_{AC}^{\beta}[k+1]$ can accordingly be expressed in term of $V_{AC}^{\alpha}[k]$ and $V_{AC}^{\beta}[k]$ as follows:

$$\begin{aligned} V_{AC}^{\alpha}[k+1] &= \cos(3.6°)V_{AC}^{\alpha}[k] - \sin(3.6°)V_{AC}^{\beta}[k] \\ V_{AC}^{\beta}[k+1] &= \sin(3.6°)V_{AC}^{\alpha}[k] + \cos(3.6°)V_{AC}^{\beta}[k] \end{aligned} \tag{4.10}$$

As pointed out in section 3.2, the implementation of SVPWM provides the crucial advantage of decoupling the DC-link voltage. Additionally, the DC-link capacitors, C_{DT} and C_{DB}, will decouple high frequency load currents, which, when considered in conjunction with the SVPWM that ensures DC-link decoupling at the lower frequencies, provides complete V_{DC} decoupling.

4.3.2 Simulated Performance

A simulation of the proposed controller was done in Simplorer®. A three-phase Active Rectifier is shown in Figure 4-8 and was simulated to illustrate the line-interactive UPS operating as an Active Rectifier with the current being controlled according to the control law explained above.

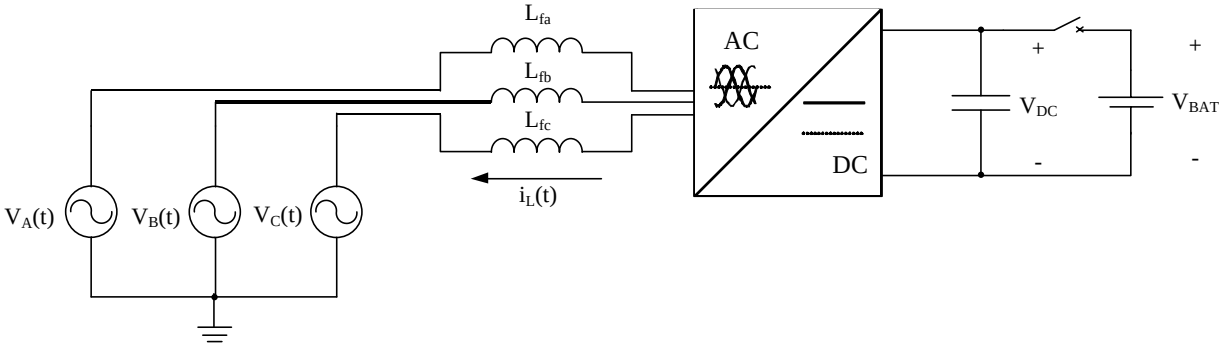

Figure 4-8: Active Rectifier Simulation Model

This three-phase converter was implemented utilising SVPWM in addition to the dead time compensation strategy developed in section 3.4. The converter system's parameters are selected to be exactly as implemented in the practical line-interactive UPS system and are found in Table 4-1:

Table 4-1: AC-DC Simulation Parameters

Simulated System Parameters	
Parameter	**Value**
V_{DC}	800 V
L	400 µH
C	200 µF
f_S	5 kHz
Dead Time	5 µs

The converter was excited by a 100 A reference space vector rotating at 50 Hz, implying reference commands of:

$$\begin{aligned} i_L^{\alpha^*}(t) &= 100\sin(2\pi 50t) \\ i_L^{\beta^*}(t) &= 100\cos(2\pi 50t) \end{aligned} \tag{4.11}$$

Figure 4-9 shows the result of the simulation containing the reference signals in addition to the average alpha- and beta components of the converter's inductor current.

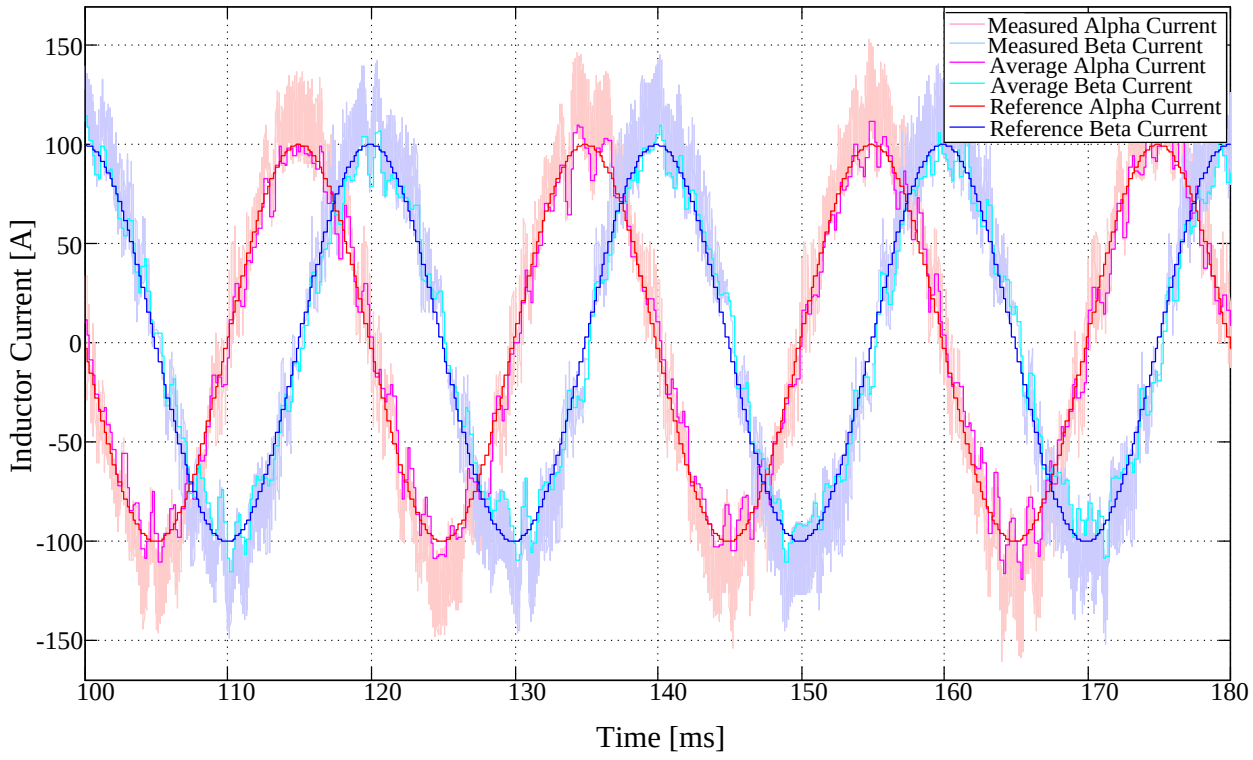

Figure 4-9: Predictive Current Controller #1 Simulation Results

It is observable that the reference tracking capability of the controller performs sufficiently, in that it is able to effectively control the average inductor current. Since the current drawn from the supply by the Active Rectifier has a constant magnitude, the DC-link voltage will increase uncontrollably. It is therefore important to point out that with the ever increasing DC-link voltage; the performance of the controller remains unaffected. This confirms that SVPWM ensured V_{DC} decoupling. The inductor current ripple, however, increases with an increase in V_{DC} but this is understandable since the ripple of the inductor current $\frac{di_L(t)}{dt}$ is proportional to the voltage potential over the inductor which in turn is dependent on the voltage of the capacitor of the DC-link.

4.4 DC-Link Voltage Regulation Strategy

4.4.1 Principle of Operation

It has been established in the previous section that the current controller effectively controls the current drawn by the converter. When considering an overview of the Active Rectifier in
Figure 4-10 and accepting the direction of the inductor current out of the converter as positive, the real power transferred through the converter can be expressed as the dot product of the supply voltage and the current through the converter [46]:

$$\begin{aligned} \mathbf{P} &= \mathbf{V}.\mathbf{I} \\ &= V_{RMS} I_{RMS} \cos\theta \end{aligned} \tag{4.12}$$

with **V** and **I** being the respective supply voltage and inductor current vectors.

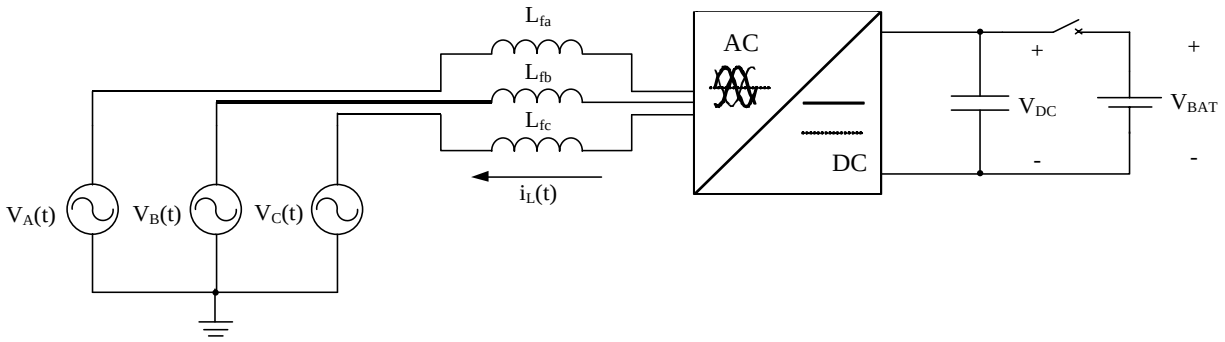

Figure 4-10: Overview of Active Rectifier

Since the current out of the converter is considered as positive, this implies that to transfer real power from the supply to the capacitor of the DC-link, the current out of the converter must be 180° out of phase with respect to the supply voltage.

A controller capable of regulating the current through the inductors has been proposed and developed in the previous section. The current, however, needs to be controlled to ensure effective regulation of the DC-link. The magnitude of the current drawn from the supply needs to be controlled depending on the amount of

power transferred and the magnitude of the DC-link voltage. Failure to do so might result in over-voltage of the DC-link which will permanently damage the capacitor and possibly the IGBTs. This is achieved by utilising the multi-loop control strategy in Figure 4-11 with the current controller implemented in the inner loop and the DC-link voltage controller completing the outer loop:

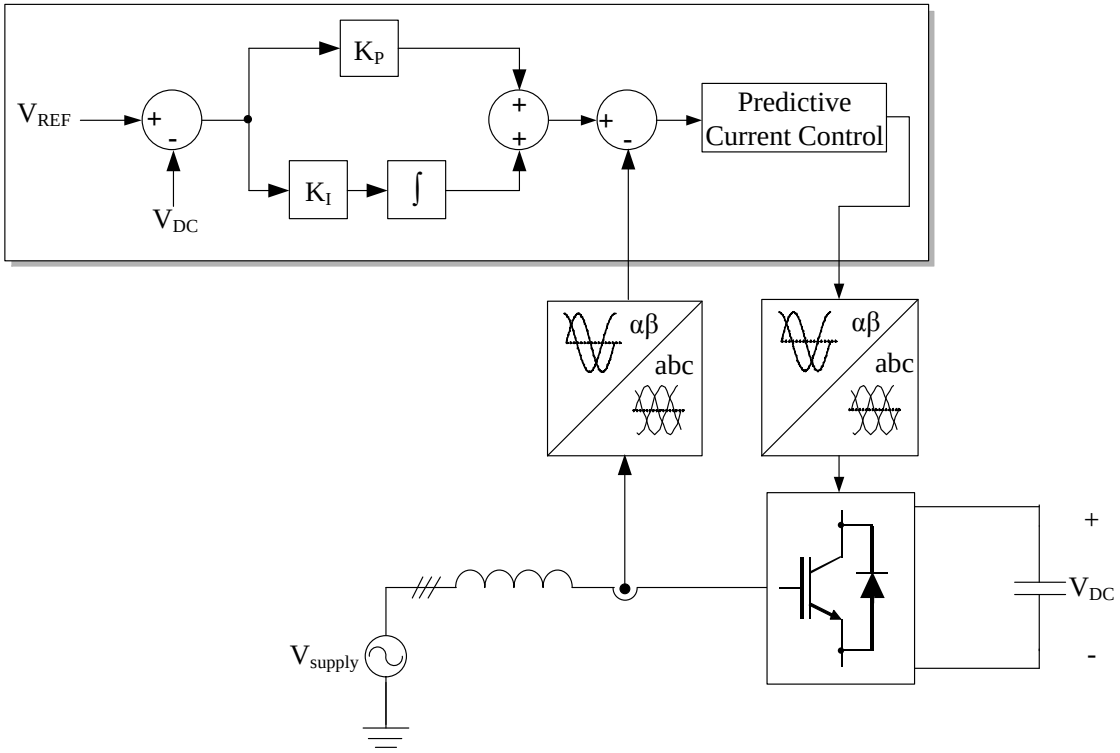

Figure 4-11: Proposed Multi-loop Control Strategy

In short, it is desired to control the DC-link voltage by controlling the magnitude of the current drawn from the supply and simultaneously ensuring a 180° difference between the current with respect to the voltage of the supply.

With the objective of regulating the DC-link voltage, V_{DC}, a simple PI-controller is proposed. The motivation for this is based on the fact that regulation of the DC-link voltage does not necessitate a high bandwidth controller due to the low system bandwidth caused by the large array of capacitors used for the DC-link. To design the PI-controller, a system model needs to be determined. Consider a simplified model of the Active Rectifier in Figure 4-12:

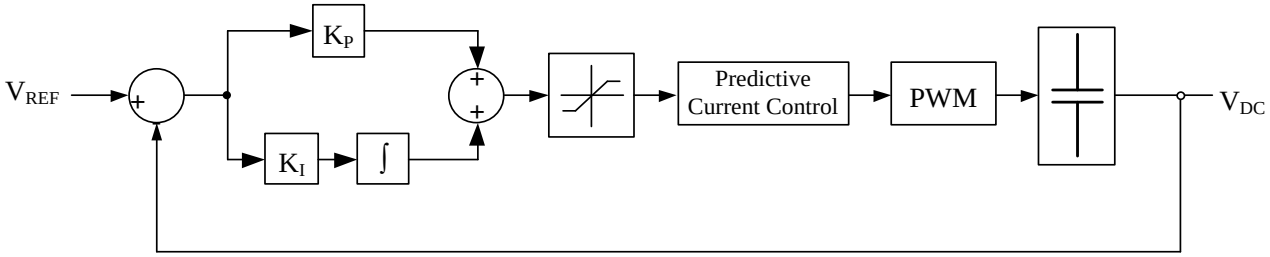

Figure 4-12: Proposed DC-Link Voltage Controller and System Model Representation

Only the capacitor of the DC-link is considered for the model of the plant. The reason for this is that a controller capable of controlling the capacitor voltage will similarly be capable of regulating the voltage with the battery connected. Connection of the battery will further decrease the natural bandwidth of the system thereby ensuring more stable control characteristics such as lower maximum overshoot. There might be a concern that the connection of the battery will result in reduced stability due to a sudden change of the system model and the increased current drawn from the system, but it will be shown that the system is still stable under these conditions.

As pointed out in Figure 4-12, the design of the voltage controller necessitates knowledge of the dynamic characteristics of the current controller. Since the predictive current controller operates at the sampling rate, the inductor is effectively decoupled from the system due to the high frequency behaviour of the system caused by the corresponding high frequency current controller. Additionally, the impedance of the inductor is almost negligible at the low operating frequency of the voltage controller. Consequently, the inductor is not taken into consideration during the design of the voltage controller. The limiter in Figure 4-12 is utilised in the practical implementation to limit the amount of current drawn from the supply.

Since the predictive current controller is capable of effectively regulating the inductor current by inducing a reference command with the aim of removing the tracking error by the end of the next switching period, it is clear that the system's inductor current is delayed by a single switching period. It is, therefore, affordable to estimate the predictive controller as a unity gain with a single sample delay. From classical control theory, a single sample delay can be represented by the non-rational function $e^{-T_S s}$. Franklin provides in [47] a rationalisation of $e^{-T_S s}$ by proposing a Padé approximation. This results in a unit delay to be represented as:

$$\text{Unit Delay} = e^{-T_s} \simeq \frac{1-\frac{T_S s}{2}}{1+\frac{T_S s}{2}} \tag{4.13}$$

Following the above argumentation and assuming that the PWM has a miniscule effect in comparison to the effect of the current controller, the system depicted in Figure 4-12 equates to the following:

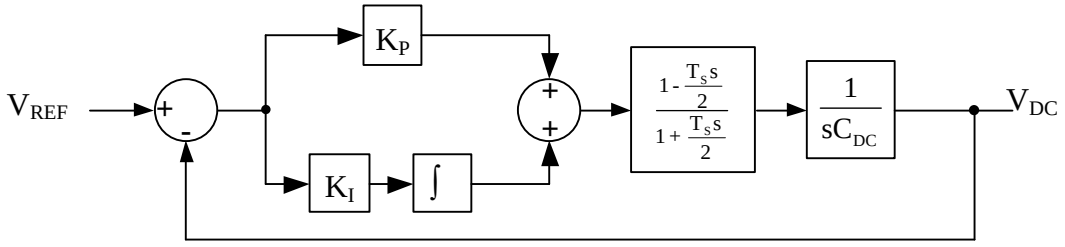

Figure 4-13: Simplified Control Scheme utilised in DC-link Voltage Regulator

The open-loop transfer function of the system in Figure 4-13 is consequently expressed as:

$$G_{OL}(s) = \left(K_P + \frac{K_I}{s}\right)\left(\frac{1-\frac{T_S s}{2}}{1+\frac{T_S s}{2}}\right)\left(\frac{1}{sC_{DC}}\right) \tag{4.14}$$

To guarantee stability, the system needs to ensure that $G(j\omega_{CL})=-1$ where ω_{CL} represents the maximum angular velocity of the proposed closed-loop system. Applying the standard gain- and phase-margin conditions, equations (4.15) and (4.16) are respectively derived:

$$\frac{\sqrt{\omega_{CL}^2 K_P^2 + K_I^2}}{\omega_{CL} C_{DC}} = 1 \tag{4.15}$$

$$\frac{\omega_{CL} K_P}{K_I} = \tan\left(\arctan\left(\frac{\omega_{CL} T_S}{2}\right) + PM\right) \tag{4.16}$$

where PM represents the desired phase-margin of the controller. With the aim of regulating a DC voltage, it is understandable that the bandwidth of the voltage controller needs be substantially less than the large bandwidth of the current controller. Choosing a bandwidth of $\omega_{CL} \simeq 31.42$ rad/s and a phase margin of 50°, the simultaneous solution of equations (4.15) and (4.16) results in:

$$K_P = 0.77$$
$$K_I = 20.04 \ (\text{rads}^{-1})$$

Note that these gains do not represent the discrete gains which are implemented in the digital controller, but are found to be:

$$K_{P\_DIG} = 0.77$$
$$K_{I\_DIG} = 4\text{x}10^{-3}$$

To determine whether the model which was derived in the above discussion is an accurate approximation of the actual system, this closed-loop system was simulated in Matlab®. A step response of the closed-loop system is shown in Figure 4-14 and shows a maximum overshoot of 26.7 %.

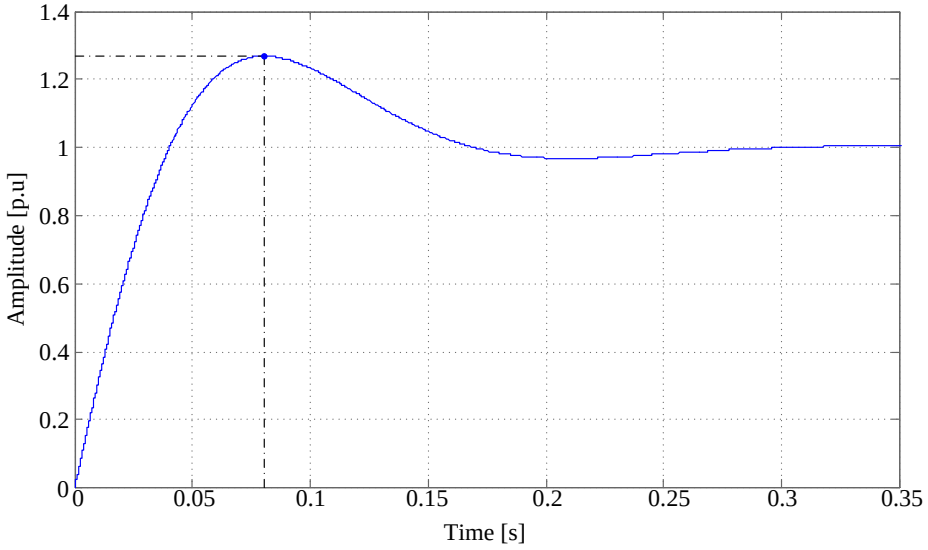

Figure 4-14: Matlab Step Response of Voltage Control System

The settling time according to the 2% criterion in this step response is approximately t_s = 0.25 s. Therefore, the dampening factor ζ of the system can be determined:

$$\zeta = \sqrt{\frac{(\ln M_p)^2}{\pi^2 + (\ln M_p)^2}} \simeq 0.38 \tag{4.17}$$

Consequently, utilising classical control theory the bandwidth of the system is determined from this dampening factor and the settling time:

$$\omega_n \simeq \frac{3}{\zeta t_s} = 31.2 \text{ rad/s} \tag{4.18}$$

The natural frequency is thus $\omega_n \simeq 31.2$ rad/s. When compared with the design choice of making the bandwidth of the system 31.42 rad/s, it be concluded that the controller performs according to the desired design specifications.

4.4.2 Integrator Windup

With the objective of removing the steady-state tracking error, an integrator will feed a large command signal to the system plant. Due to practical limitations the plant is often unable to realise the command it received from the integrator. When considering the Active Rectifier, an example of such a limitation is when the integrator provides a large command for the current controller which subsequently corresponds with a large current drawn by the converter. The system will subsequently be driven into saturation, due to inherent limitations such as inverter saturation because of SVPWM implementation or just simply because the required current is larger than what the IGBT modules are capable of realising. This phenomenon of the integrator to producing an ever-increasing command which results in converter saturation is known as *integrator windup*.

To prevent the occurrence of integrator windup, an integrator *anti*-windup scheme as recommended in [31] is proposed and depicted in Figure 4-15. The motivation for using this anti-windup scheme is that it is easily implementable, effective at achieving the required results and is computationally non-taxing for controllers such as, for instance, DSPs.

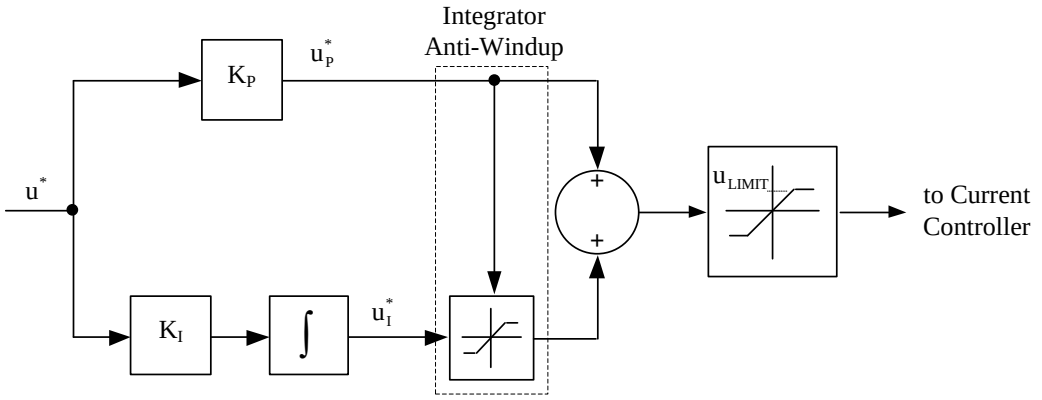

Figure 4-15: Proposed Integrator Anti-Windup Scheme

The proposed integrator anti-windup scheme functions by utilising the reference command produced by the proportional controller, u_P^*, in conjunction with the limit of the overall controller, u_{LIMIT}, to determine a dynamic limit, u_{INT_LIMIT}, according to equation (4.19):

$$u_{INT\_LIMIT} = u_{LIMIT} - u_P^* \tag{4.19}$$

This anti-windup scheme provides an effective means of controlling the current command produces by the voltage controller without causing unnecessary controller saturation and non-linear command signals. The proposal in Figure 4-15 is subsequently used to further augment the total control structure depicted in Figure 4-2 to produce the final complete control structure in Figure 4-16:

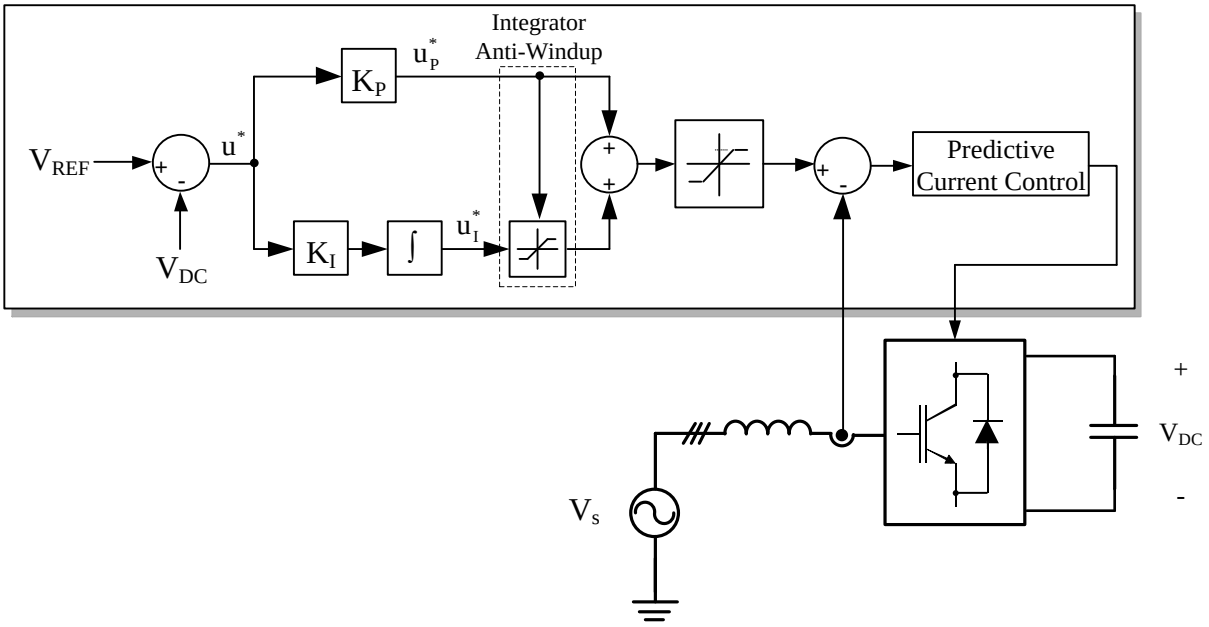

Figure 4-16: Complete Double-Loop Controller

4.4.3 Simulated Performance

The multi-loop controller found in Figure 4-16 is used to control a converter similar to the one used to simulate the current controller in the previous section. The converter in Figure 4-17 contains additional

resistors in series with the inductors with the purpose of limiting the inrush current through the converter at the instant the supply is engaged.

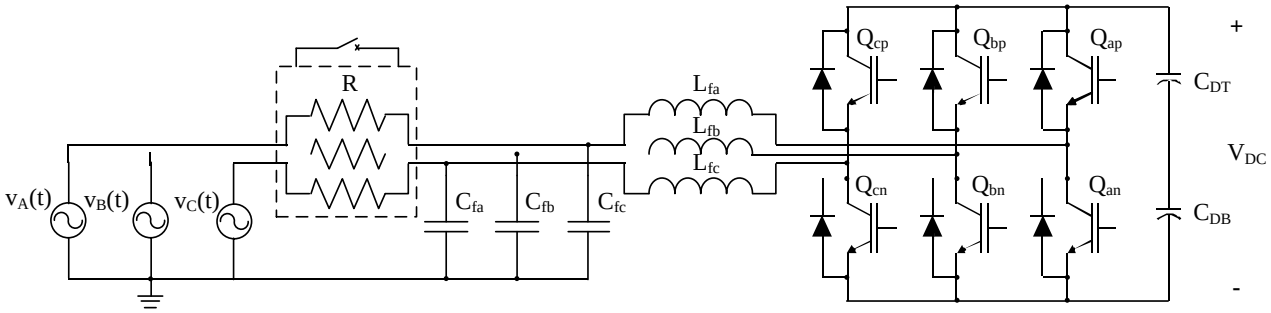

Figure 4-17: Complete Active Rectifier Simulation

A simulation of this system is again done in Simplorer to determine the converter performance with the proposed double-loop controller. It is important to point out that the integrator anti-windup is included in this simulation but the limit is set at an extremely high value so as to prevent the effect of anti-windup from influencing the performance of the voltage controller.

Firstly, consider the performance of the voltage controller. Figure 4-18 which shows the DC-link voltage during the time that the Active Rectifier starts to charge the capacitors of the DC-link to match with the voltage of the storage battery before connecting to it.

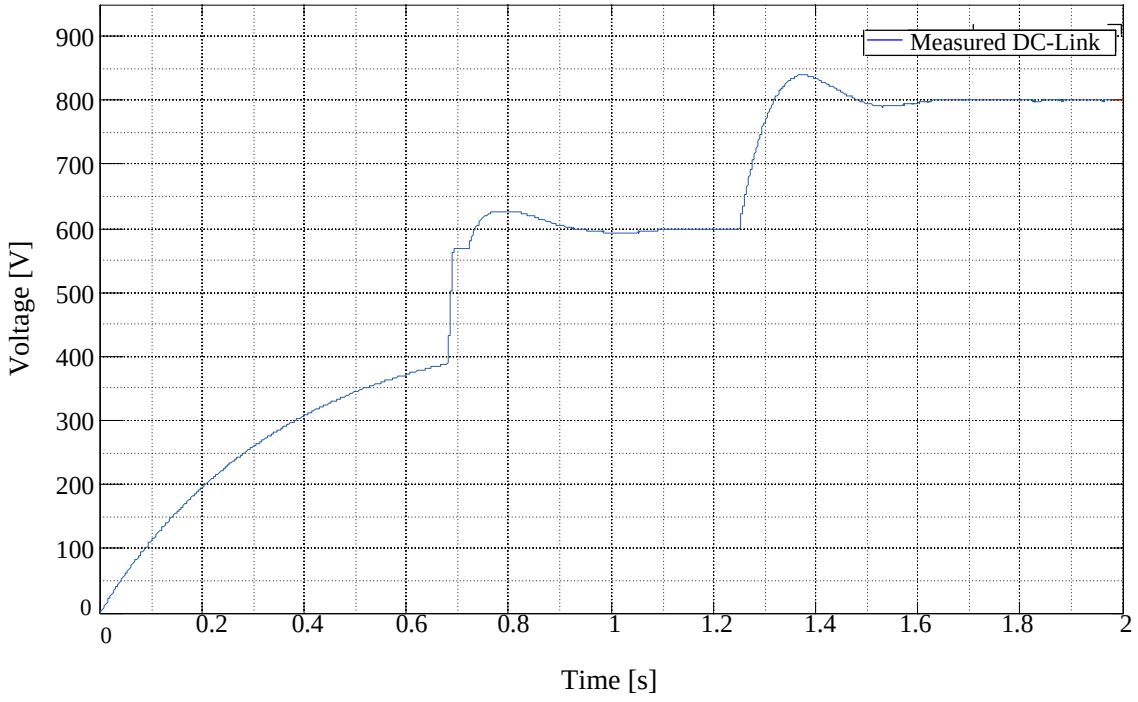

Figure 4-18: DC-Link Voltage during Active Rectifier Initialisation

The DC-link is passively charged via the anti-parallel diodes of the IGBTs up until approximately 680 ms, after which the inrush current limiting resistors are bypassed and the DC-link is further passively charged to

about 570 V. At the time instant of 720 ms the converter starts switching with a 600 V voltage reference command. A characteristic step response is seen at this moment, but is not an accurate representation of the voltage controller's performance. This is due to initial conditions of the simulation. A more accurate indication of the voltage controller's performance can be seen at 1.25 s where the reference command, V_{REF}, is stepped from 600 V to 800 V. The observed maximum overshoot is found to be approximately 21 %. This is close to the theoretical overshoot of the system as indicated by a Matlab step response for the same system. This indicates that the derived model that represents the system is a fair estimation, which enabled the subsequent design of the proposed voltage controller.

Secondly, consider the performance of the voltage controller with the storage battery connected to the DC-link. The battery can be approximated as a DC voltage source with a series resistance. The particular battery bank used in the practical system used in this project was a 780 V DC source with a 0.36 Ω series resistance. This results in the model of the system becoming:

$$\begin{aligned} G(s) &= \frac{1}{sC_{BUS}} \| r_{BAT} \\ &= \frac{r_{BAT}}{sC_{BUS}r_{BAT}+1} \end{aligned} \tag{4.20}$$

Figure 4-19(a) shows the response of the system model described by (4.20) when controlled with the same voltage controller. It can be observed that apart from an increased settling time the system maintains stability. This additionally proves that the current controller ensures good inductor current tracking as the voltage controller commands an increased current to be drawn to sustain the higher load of the included battery. Figure 4-19 (b) shows the Simplorer simulation when the battery is connected after the DC-link voltage has matched with the battery voltage. Observe that the connection of the battery causes a slight decrease of the DC voltage but recovers to 800 V with similar behaviour, as seen in Figure 4-19 (a).

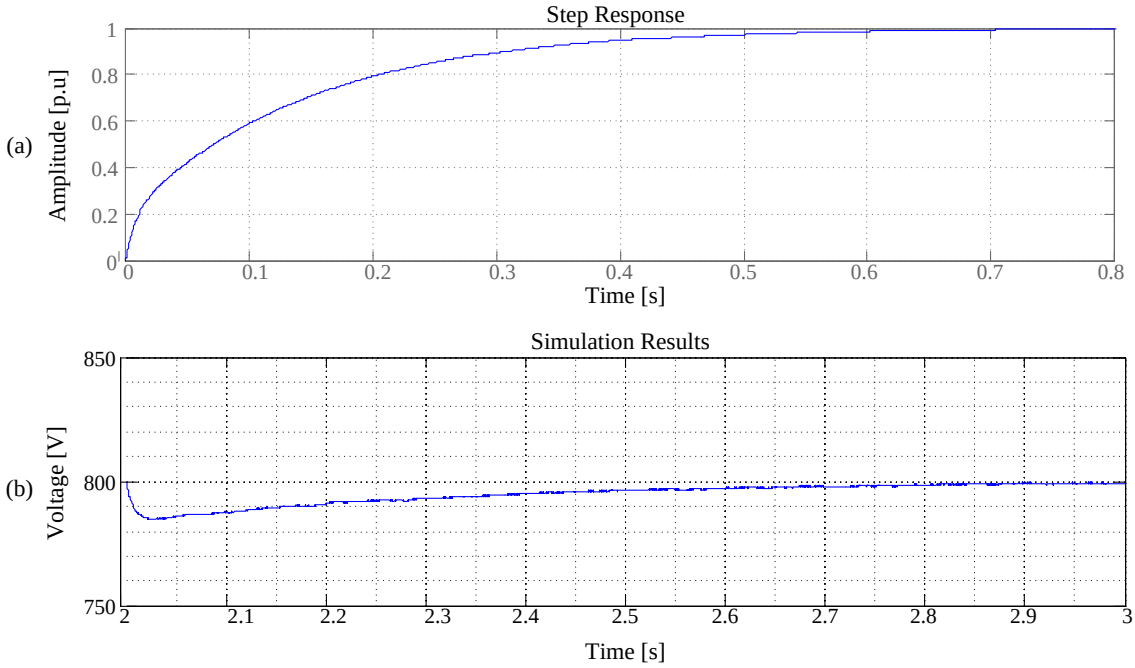

Figure 4-19: (a) Matlab Step Response with Battery included (b) Simulation Results when connecting the Battery

Finally, consider the performance of the current controller when operating in conjunction with the PI voltage controller. Figure 4-20 (a) shows the respective reference alpha- and beta current commands generated by the current controller along with the measured average inductor currents. Figure 4-20 (b) shows the individual signals generated by the proportional and integral controllers in the outer loop. These signals are summed and used as input by the inner predictive current controller. All the signals are shown from a time just before 1.25 s when the voltage reference command is stepped from 600 V to 800 V.

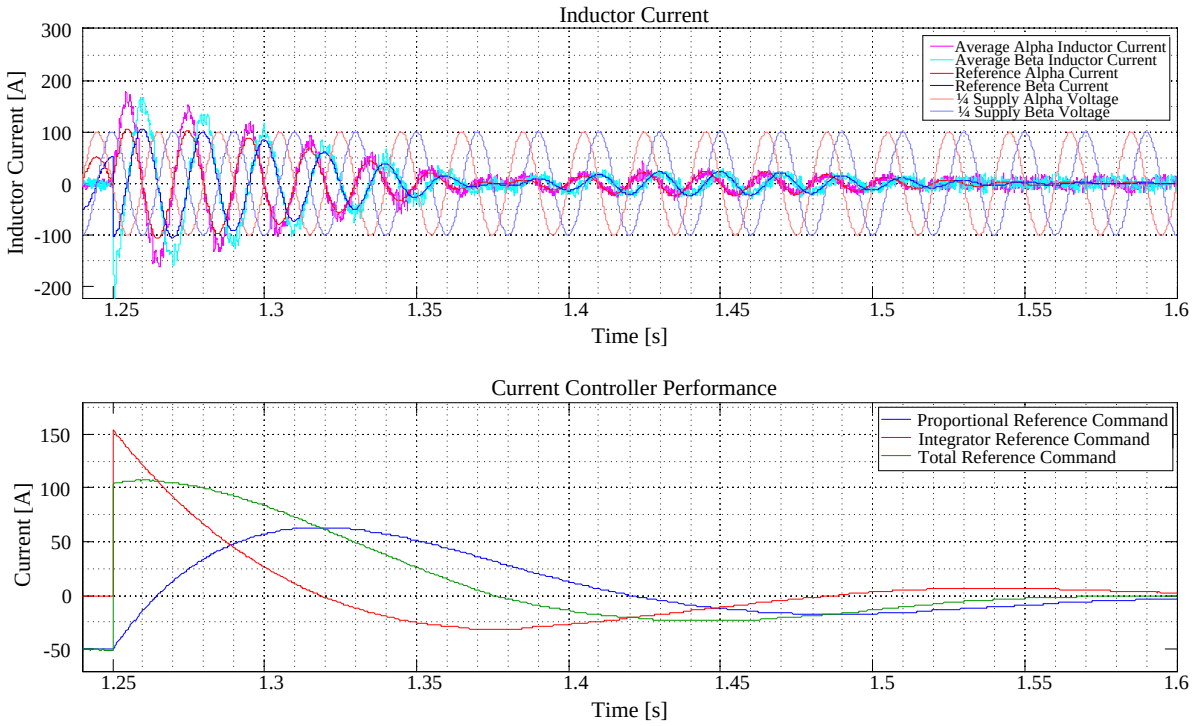

Figure 4-20: (a) System Signals (b) Voltage Controller Command Signals

When focusing on the reference commands generated by the current controller and compared with their respective supply voltage measurements, it is observable that the current controller maintains a 180° phase difference with respect to the supply voltage. The question arises when regarding the magnitude of the average inductor current in comparison with its respective reference command. This clear magnitude error is due to the notorious lack of an integrator in the predictive controller. Furthermore, the situation where the reference currents are in phase with the voltages corresponds with the voltage reference being negative at these instants.

4.5 Conclusion

A multi-loop control strategy was proposed with the inductor current being controlled in the inner loop and the outer loop constituting the control of the DC-link voltage.

A general approach to the predictive control of the inductor current was presented, developed and simulated. Simulation of the controller proved that the controller is capable of effectively ensuring reference tracking of the inductor current. The advantages of utilising SVPWM and a stationary reference frame were illustrated along with the simplicity of its implementation. A model of the system was derived which included an approximate model of the predictive current controller. This current controller was subsequently used in conjunction with a simple PI control strategy to regulate the DC-link voltage of the Active Rectifier which was simulated and compared with the theoretically derived controller. Simulations proved that the DC-link controller provided the necessary regulation of the DC-link under various conditions, such as the initial charging of the DC-link, regulation of the link under no-load condition and also when the battery load is connected.

The proposed multi-loop strategy in conjunction with the chosen strategies for the control of the both the DC voltage and inductor current, presented acceptable control performance of the Active Rectifier.

CHAPTER 5

CONTROL OF THE VOLTAGE-SOURCE INVERTER

5 CONTROL OF THE VOLTAGE-SOURCE INVERTER

5.1 Introduction

In the event of a primary power outage, the UPS will redirect power from the storage batteries to the load to ensure uninterrupted power to the load. Figure 5-1 shows a single line diagram of the line-interactive UPS and emphasises the focus of this chapter.

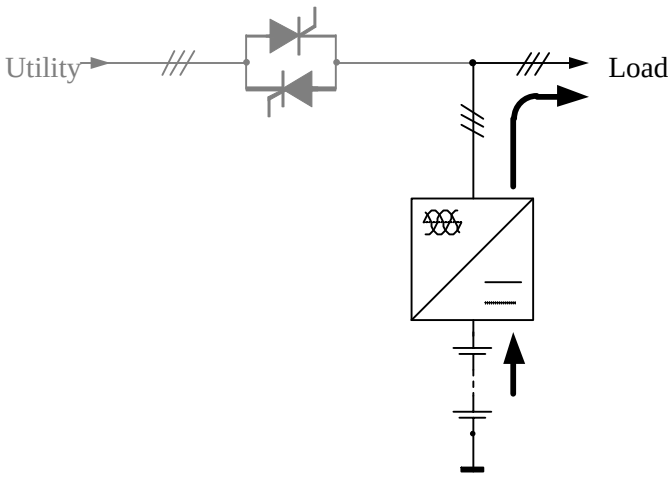

Figure 5-1: DC-AC Converter of the Line-Interactive UPS

The focus of this chapter is on the control of the switching converter when it operates as a three-phase VSI. The emphasis of the study is the research of strategies for the control of the output voltage supplied by a line-interactive UPS. The study includes the investigation of different control topologies and various strategies for the control of multiple output parameters, such as the output current and voltage.

5.2 Modelling the System

The aim in this section is to derive a model of the UPS converter that can be used in the design of all the subsequent controllers in this chapter. Figure 5-2 shows the chosen multi-loop control strategy that is employed to control the VSI. It graphically depicts that the focus of this section is to derive a usable mathematical model. It can furthermore be seen that it is possible to control the current through the inductor and the voltage across the capacitor of the output stage independently. The independent control will be proven in the subsequent text.

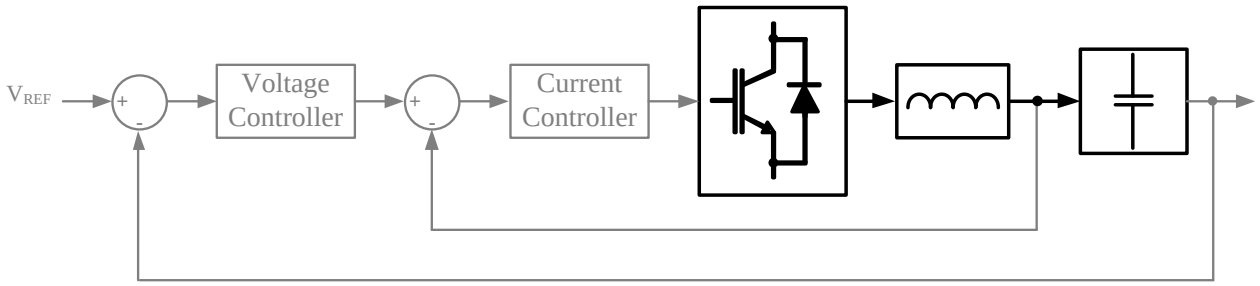

Figure 5-2: Focus on Modelling of the VSI Converter

With the purpose of deriving a model for the inverter used in the line-interactive UPS, Figure 5-3 depicts a simple single-phase VSI half-bridge topology. Buso et al point out in [48] that the second-order filter of the system shown in Figure 5-3 can be expressed as a state-space model with the following format:

$$\frac{d}{dt}\mathbf{x}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B_1}v_{CONV}(t) + \mathbf{B_2}i_O(t)$$

where $\mathbf{x}(t) = \begin{bmatrix} v_O(t) \\ i_L(t) \end{bmatrix}$ is the state vector, $v_{CONV}(t)$ is the average converter voltage and $i_O(t)$ is the output current.

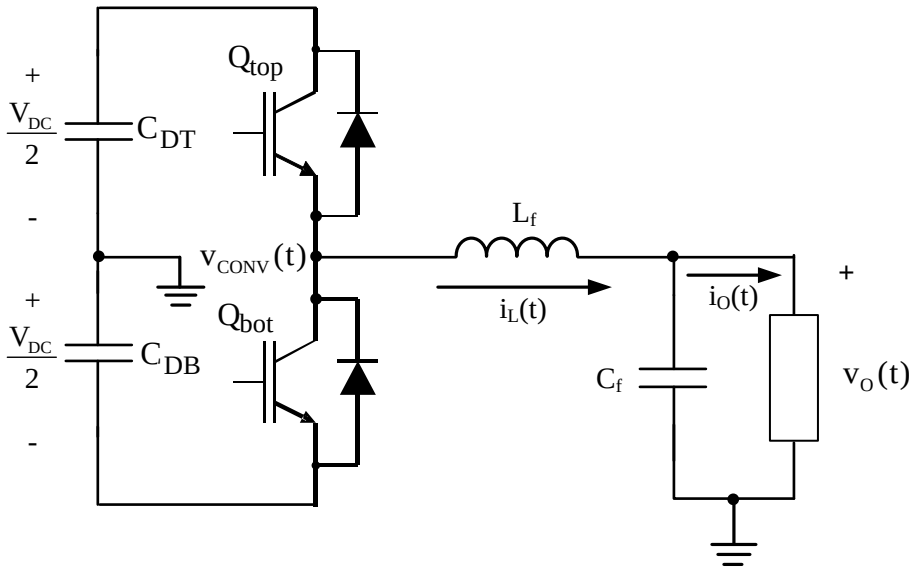

Figure 5-3: Single-Phase Half-Bridge VSI

It is known that the output capacitor current can be described as $i_C(t) = C\frac{dv_C(t)}{dt}$. This gives rise to the output voltage being described by the following differential equation, since the output voltage equals the capacitor voltage:

$$\frac{dv_O(t)}{dt} = \frac{1}{C}\left(i_L(t) - i_O(t)\right) \tag{5.1}$$

The voltage potential of the inductor can in a similar manner be described as $v_L(t) = L\frac{di_L(t)}{dt}$ which likewise results in the differential equation describing the inductor current:

$$\frac{di_L(t)}{dt} = \frac{1}{L}\left(v_{CONV}(t) - v_O(t)\right) \tag{5.2}$$

The system can consequently be described as follows:

$$\frac{d}{dt}\mathbf{x}(t) = \begin{bmatrix} 0 & \frac{1}{C} \\ \frac{-1}{L} & 0 \end{bmatrix}\mathbf{x}(t) + \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix} v_{CONV}(t) + \begin{bmatrix} \frac{-1}{C} \\ 0 \end{bmatrix} i_O(t) \tag{5.3}$$

The discrete-time equivalent of the system is described as:

$$x[k+1] = \mathbf{\Phi} x[k] + \mathbf{\Gamma_1} v_{CONV}[k] + \mathbf{\Gamma_2} i_O[k]$$

with $\Phi = e^{\mathbf{A}T_S}$, $\Gamma_1 = (e^{\mathbf{A}T_S} - \mathbf{I}_2)\mathbf{A}^{-1}\mathbf{B_1}$ and $\Gamma_2 = (e^{\mathbf{A}T_S} - \mathbf{I}_2)\mathbf{A}^{-1}\mathbf{B_2}$. The state-transition matrix Φ is calculated by using the following Taylor expansion:

$$e^{\mathbf{A}T_S} = \mathbf{I} + \mathbf{A}T_S + \frac{\mathbf{A}^2}{2!}T_S^2 + \frac{\mathbf{A}^3}{3!}T_S^3 + \ldots \tag{5.4}$$

with $\mathbf{I}$ being the identity matrix. Therefore, the discrete-time model is described as:

$$\begin{aligned} \begin{bmatrix} v_O[k+1] \\ i_L[k+1] \end{bmatrix} &= \begin{bmatrix} 1 - \frac{T_S}{2CL} + \ldots & \frac{T_S}{C} - \frac{T_S^3}{3C^2L} + \ldots \\ -\frac{T_S}{L} + \frac{T_S^3}{3CL^2} + \ldots & 1 - \frac{T_S^2}{2CL^2} + \ldots \end{bmatrix} \begin{bmatrix} v_O[k] \\ i_L[k] \end{bmatrix} \\ &+ \begin{bmatrix} -1 + \frac{T_S^2}{2CL} + \ldots \\ \frac{T_S}{L} - \frac{T_S^3}{3CL} + \ldots \end{bmatrix} v_{CONV}[k] + \begin{bmatrix} -\frac{T_S}{C} + \frac{T_S^3}{3C^2L} + \ldots \\ -1 + \frac{T_S^2}{2CL} + \ldots \end{bmatrix} i_O[k] \end{aligned} \tag{5.5}$$

Recognising the Taylor series of $\cos(x)$ and $\sin(x)$ respectively as:

$$\sin(x) = \sum_{n=0}^{\infty} \frac{(-1)^n}{(2n+1)!} x^{2n+1} = x - \frac{x^3}{3!} + \frac{x^5}{5!} - \ldots$$

$$\cos(x) = \sum_{n=0}^{\infty} \frac{(-1)^n}{(2n)!} x^{2n} = 1 - \frac{x^2}{2!} + \frac{x^4}{4!} - \ldots$$

Equation (5.5) becomes:

$$\begin{aligned} \begin{bmatrix} v_O[k+1] \\ i_L[k+1] \end{bmatrix} &= \begin{bmatrix} \cos(\omega_O T_S) & \frac{1}{\omega_O C}\sin(\omega_O T_S) \\ -\frac{1}{\omega_O L}\sin(\omega_O T_S) & \cos(\omega_O T_S) \end{bmatrix} \begin{bmatrix} v_O[k] \\ i_L[k] \end{bmatrix} \\ &+ \begin{bmatrix} 1 - \cos(\omega_O T_S) \\ \frac{1}{\omega_O L}\sin(\omega_O T_S) \end{bmatrix} v_{CONV}[k] + \begin{bmatrix} -\frac{1}{\omega_O C}\sin(\omega_O T_S) \\ 1 - \cos(\omega_O T_S) \end{bmatrix} i_O[k] \end{aligned} \tag{5.6}$$

where ω_O denotes the resonance frequency of the second-order filter and is defined as $\omega_O = \sqrt{\frac{1}{LC}}$. The sampling frequency $f_S = \frac{1}{T_S}$ is much greater than the resonance frequency ω_O. The subsequent result is that $\omega_O T_S \ll 1$, which implies $\cos(\omega_O T_S) \simeq 1$. Since $\omega_O T_S \ll 1$, then matrix elements such as $\frac{1}{\omega_O C}\sin(\omega_O T_S)$ can be simplified according to L'Hospital's rule. $\frac{1}{\omega_O C}\sin(\omega_O T_S)$ becomes $\frac{\sin(\omega_O T_S)}{\frac{\omega_O C T_S}{T_S}} = \frac{T_S}{C}\frac{\sin(\omega_O T_S)}{\omega_O T_S}$ and can be solved according to equation (5.7).

$$\begin{aligned} &\frac{T_S}{C}\lim_{\omega_O T_S \to 0}\left(\frac{\sin(\omega_O T_S)}{\omega_O T_S}\right) \\ &= \frac{T_S}{C}\lim_{\omega_O T_S \to 0}\left(\cos(\omega_O T_S)\right) \qquad \text{(According to L'Hospital)} \\ &\simeq \frac{T_S}{C} \end{aligned} \tag{5.7}$$

Consequently, the system description according to equation (5.6), can subsequently be described by equation (5.8):

$$\begin{bmatrix} v_O[k+1] \\ i_L[k+1] \end{bmatrix} = \begin{bmatrix} 1 & \frac{T_S}{C} \\ -\frac{T_S}{L} & 1 \end{bmatrix}\begin{bmatrix} v_O[k] \\ i_L[k] \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{T_S}{L} \end{bmatrix} v_{CONV}[k] + \begin{bmatrix} -\frac{T_S}{C} \\ 0 \end{bmatrix} i_O[k] \tag{5.8}$$

This signifies that the second-order filter causes the system to be described by the dynamic discrete-time equations (5.9) and (5.10):

$$v_O[k+1] = v_O[k] + \frac{T_S}{C}\left[i_L[k] - i_O[k]\right] \tag{5.9}$$

$$i_L[k+1] = i_L[k] + \frac{T_S}{L}\left[v_{CONV}[k] - v_O[k]\right] \tag{5.10}$$

The controllers that are subsequently designed are based on the system being described by these dynamic discrete-time equations.

5.3 Current Control Strategies

5.3.1 Introduction

Figure 5-4 points out that the focus of this section is on the derivation and discussion of a means of controlling the output current of the VSI. The second-order output filter removes several frequency components from both the output current and voltage. It was found that if the output inductor current is

controlled it ensures better control capability. In sections 5.3.2 and 5.3.3 proposals for the control of the inductor are given.

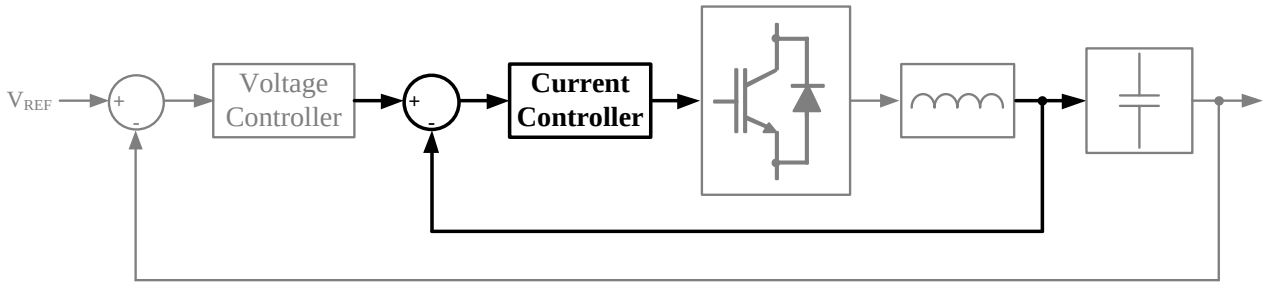

Figure 5-4: Focus on Current Control of UPS Output Current

5.3.2 Predictive Current Controller: A Mathematical Approach

5.3.2.1 Principle of Operation

Chen et al. proposed in [49] a predictive approach for the control of the valley, peak and average inductor current for basic converters such as the buck, boost and buck-boost converter. This approach was used as the foundation for the derivation of a predictive current controller for use in a VSI inverter topology.

The goal of the proposed control method is to ensure that the average inductor current follow the reference current. The duty cycle for the next switching period is calculated based on the previously sampled inductor current and input and output voltages. Consider the simple half-bridge inverter topology in Figure 5-5.

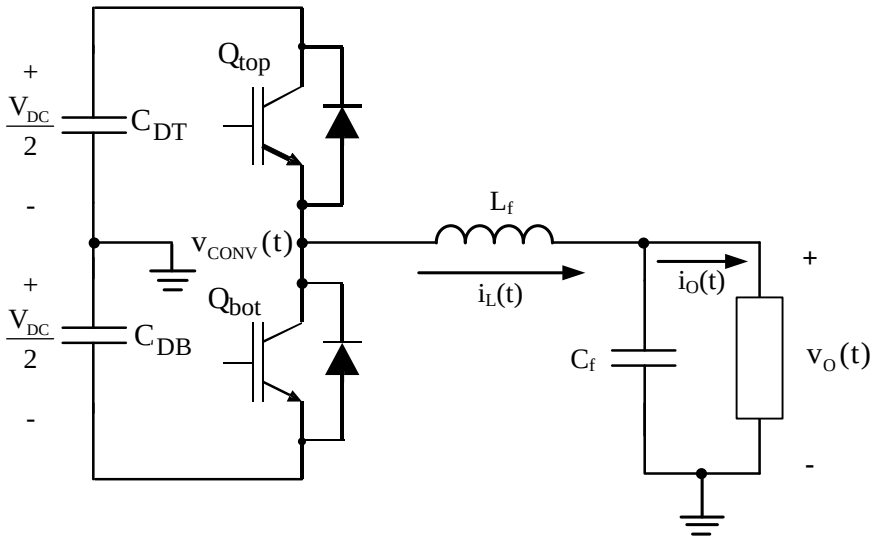

Figure 5-5: Half-Bridge VSI

Assume that the effects of dead time are negligible for the sake of simplifying the derivation of the controller. Due to the complementary switching of the top and bottom IGBTs of the half-bridge, the converter voltage $V_{CONV}(t)$ can be defined as:

$$V_{CONV}(t) = \begin{cases} \frac{V_{DC}}{2} & \text{if } Q_{top} \text{ is on} \\ -\frac{V_{DC}}{2} & \text{if } Q_{top} \text{ is off} \end{cases} \tag{5.11}$$

Subsequently, the slope of the inductor current for the case when the current is both increasing as well as decreasing, can be defined as:

$$\frac{di_L(t)}{dt} = \frac{V_{CONV}(t) - V_O(t)}{L} \tag{5.12}$$

The resulting inductor current is shown in Figure 5-6(b) for three switching cycles. The sampled inductor current at time $t = kT_S$ can be expressed as a function based on the previously sampled current at $t = (k-1)T_S$. It has been previously pointed out that the inductor current is sampled at the peak of the PWM carrier, but it is also important to note in Figure 5-6 (a) that the reference and therefore the duty cycle updates at the trough of the carrier. This results in the inductor current's duration being expressed in terms of both the duty cycle at both $t = kT_S$ and $t = (k-1)T_S$. The durations for one sampling period are indicated in Figure 5-6 (b)

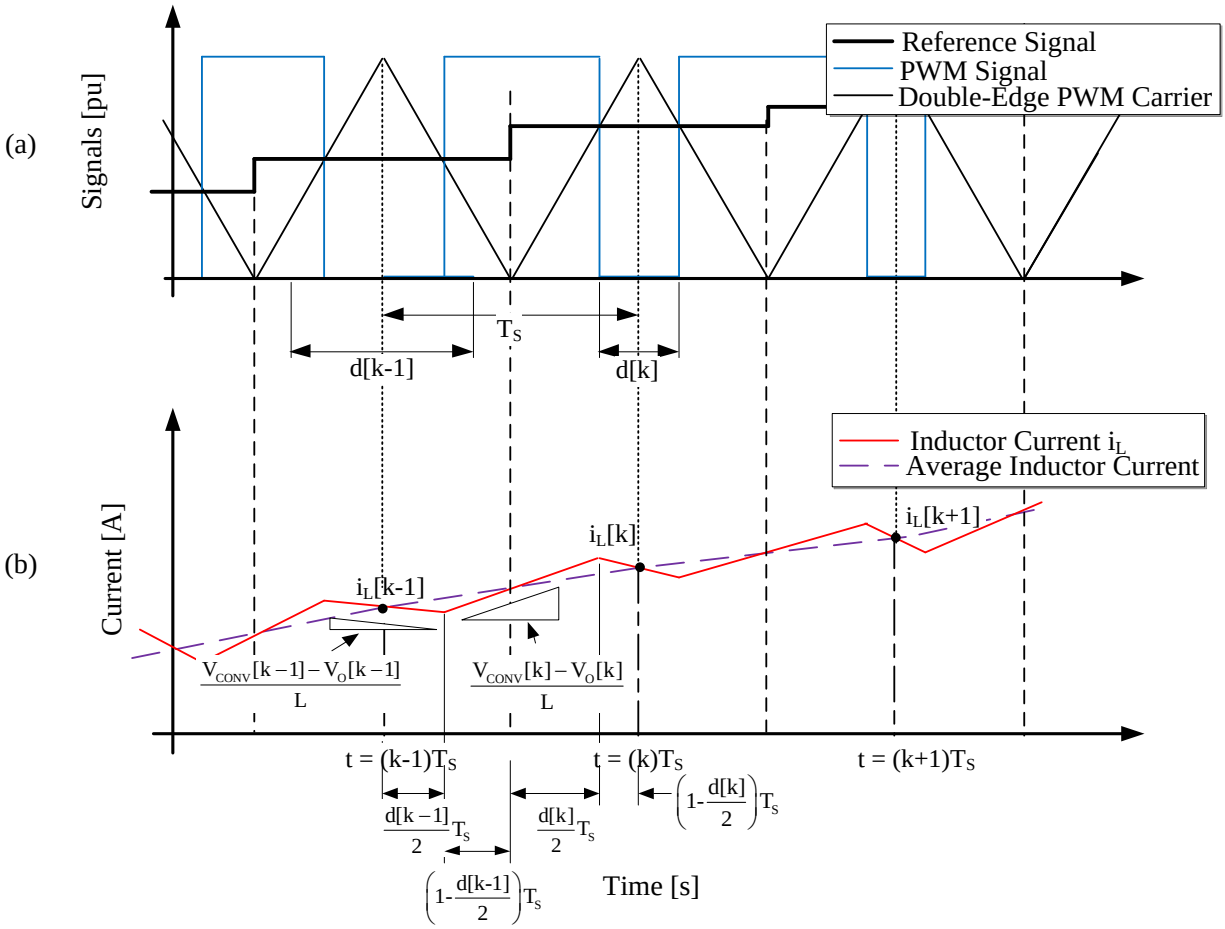

Figure 5-6: (a) Reference and PWM Signals and (b) Inductor Currents

Using the applied duty cycles d[k-1] and d[k], the inductor current can be expressed in terms of the inductor current slope as well as the previously sampled current value as:

$$\begin{aligned} i[k]=i[k-1]&+\left(\frac{V_{CONV}[k]-V_O[k]}{L}\right)\left(\frac{d[k-1]}{2}\right)T_S \\ &+\left(\frac{V_{CONV}[k]-V_O[k]}{L}\right)\left(\frac{1-d[k-1]}{2}+\frac{1-d[k]}{2}\right)T_S \\ &+\left(\frac{V_{CONV}[k]-V_O[k]}{L}\right)\left(\frac{d[k]}{2}\right)T_S \\ =i[k-1]&+\frac{V_{CONV}[k]-V_O[k]}{L}T_S \end{aligned} \tag{5.13}$$

Note that the difference of $V_{CONV}(t)$ and $V_O(t)$ between time $t=(k)T_S$ and time $t=(k+1)T_S$ is miniscule and can subsequently be accepted as constant between successive sampling periods. Applying exactly the same argumentation for the inductor current at $t=(k+1)T_S$ the inductor current $i_L[k+1]$ can similarly be expressed in terms of $i_L[k]$:

$$\begin{aligned} i[k+1]=i[k]&+\left(\frac{V_{CONV}[k+1]-V_O[k+1]}{L}\right)\left(\frac{d[k]}{2}\right)T_S \\ &+\left(\frac{V_{CONV}[k+1]-V_O[k+1]}{L}\right)\left(\frac{1-d[k]}{2}+\frac{1-d[k+1]}{2}\right)T_S \\ &+\left(\frac{V_{CONV}[k+1]-V_O[k+1]}{L}\right)\left(\frac{d[k+1]}{2}\right)T_S \\ =i[k]&+\frac{V_{CONV}[k+1]-V_O[k+1]}{L}T_S \end{aligned} \tag{5.14}$$

Substitution of (5.13) into (5.14) results in the prediction of the inductor current for the next switching period in terms of the previously sampled inductor current:

$$i_L[k+1]=i_L[k-1]+\frac{T_S}{L}\left(V_{CONV}[k+1]-V_O[k+1]+V_{CONV}[k]-V_O[k]\right) \tag{5.15}$$

Equation (5.15) serves as the foundation for the proposed control law and is subsequently used to derive the converter voltages in the stationary reference frame:

$$\begin{aligned} V_{CONV}^{\alpha}[k+1]&=\frac{L}{T_S}\left(i_L^{*\alpha}[k+1]-i_L^{\alpha}[k-1]\right)-V_{CONV}^{\alpha}[k]+V_O^{\alpha}[k+1]+V_O^{\alpha}[k] \\ V_{CONV}^{\beta}[k+1]&=\frac{L}{T_S}\left(i_L^{*\beta}[k+1]-i_L^{\beta}[k-1]\right)-V_{CONV}^{\beta}[k]+V_O^{\beta}[k+1]+V_O^{\beta}[k] \end{aligned} \tag{5.16}$$

with $V_{CONV}^{\alpha}[k+1]$ and $V_{CONV}^{\beta}[k+1]$ being the respective alpha- and beta- components of the converter voltage and $i_L^{*\alpha}[k+1]$ and $i_L^{*\beta}[k+1]$ the corresponding current references.

5.3.2.2 Simulated Performance

To determine the effectiveness of this proposed current controller, a simulation is done of a three-phase converter that employs this current controller. Figure 5-7(a) show the actual alpha- and beta inductor currents with respect to the reference current commands, whereas Figure 5-7(b) depicts the output voltage.

A clear tracking error can be observed on the output current. The error is exacerbated during a load step when the controller is incapable of even ensuring a constant current magnitude.

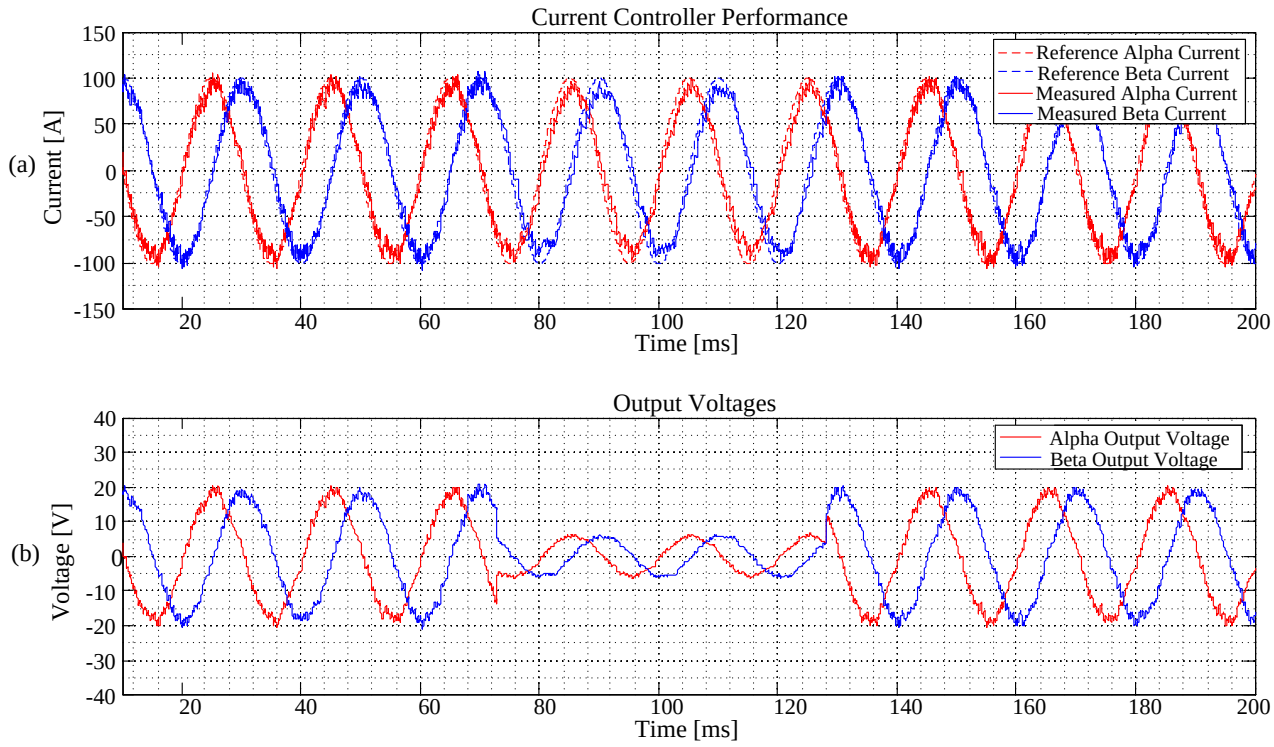

Figure 5-7: Performance of Current Controller

After doing this simulation, it was deemed necessary to consider an alternative approach to control the inductor current of a VSI. In the following section discusses a predictive current control scheme that is based on a two- switching period prediction.

5.3.3 Predictive Current Controller: A Physical Approach

5.3.3.1 Principle of Operation

This approach is a predictive implementation for the control of the inductor current. To point out the obvious, the controller operates as a dead-beat controller in that it produces an input reference command signal to the converter with the aim of driving the tracking error to zero. This control approach is basically an application of discrete time dynamic state feedback by applying digital control theory. This theoretical

approach will however not be followed, but instead the derivation of the controller will be approached from the physical operation of the converter and the modulator.

The model of the VSI that is described in Figure 5-3 includes the complete half-bridge converter. The average of converter voltage $v_{CONV}(t)$ can be represented by an ideal voltage source which supplies power to a load with an output voltage $v_O(t)$ via the second-order filter. The equivalent series resistance (ESR) of the inductor is included with the aim of improving the controller's capability. The averaged model is subsequently depicted as:

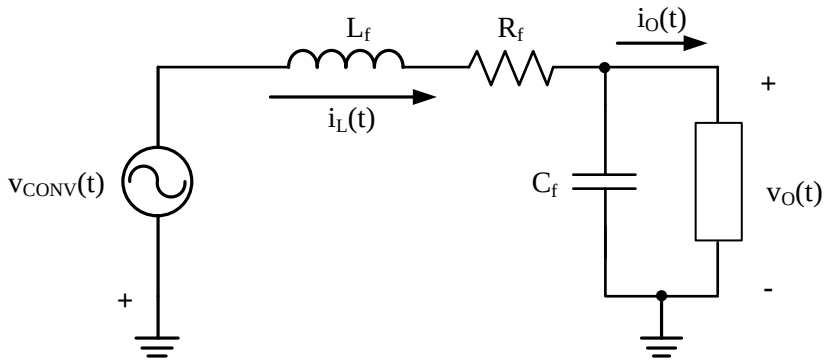

Figure 5-8: Averaged Single-Phase VSI

First note that it is assumed that the sampling frequency is much greater than the resonance frequency ω_O of the LC-filter. In other words, we assume that $\omega_O Ts=1$. Under this assumption, it is noticeable that the impedance of the capacitor of the second-order filter becomes negligible with respect to the impedance of the inductor at the control frequency. Consequently, the output voltage is independent of the current injected to the inductor. Accordingly, the capacitor is neglected from the second-order filter and only the inductive component is considered. This consequently leads to the system being described by equation (5.10).

$$i_L[k+1]=i_L[k]+\frac{T_S}{L}\left[v_{CONV}[k]-v_O[k]\right]$$

The goal of the proposed controller is to determine the average converter voltage $\overline{v_{CONV}}(t)$ for each control iteration that will result in the average inductor current $i_L(t)$ equalling the reference current command after two switching periods [31]. The methodology is to determine $\overline{v_{CONV}}(t)$ at instant kT_S. This voltage will be used by the converter during the next switching period that occurs between time instants $(k+1)T_S$ and $(k+2)T_S$ to drive the inductor current in the required direction to ensure that the average inductor current equals the reference inductor current by $(k+2)T_S$. To clarify this operation, consider Figure 5-9 which shows the inductor current, converter voltage and current reference for three switching periods. Notice that the actual inductor current at $t=(k+1)T_S$ equals the reference current command at $t=(k-1)T_S$.

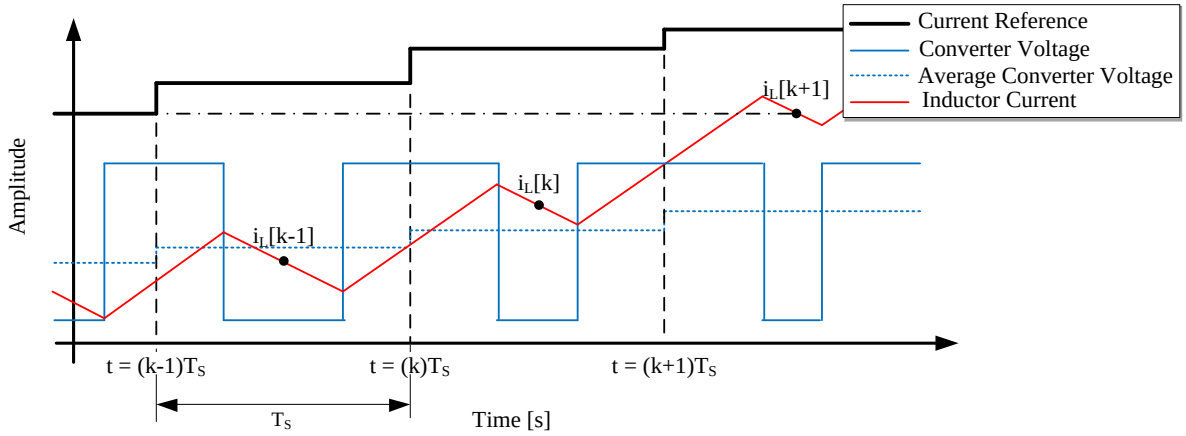

Figure 5-9: Average and Instantaneous Signals

The reference current is predicted by two switching periods with respect to the actual average inductor current of the system. The converter voltage is consequently determined with this predicted current reference which will result in the average current at $t=(k+1)T_S$ equalling the value of the current reference at $t=(k-1)T_S$

Following this argumentation, the predictive controller proposed in [31] and [48] was derived. This controller was further augmented to include the series resistance of the inductor. Equation (5.10) describes the dynamics of the inductor current in terms of the voltage potential across it. Additionally, the average inductor voltage can be expressed in terms of the inductor current in equation (5.17) by using Figure 5-8.

$$v_L[k]=v_{CONV}[k]-R_f i_L[k]-v_O[k] \tag{5.17}$$

Substitution of equation (5.17) into equation (5.10) results in $i_L[k+1]$ being described as:

$$i_L[k+1]=\frac{T_S}{L}\left(v_{CONV}[k]-v_O[k]\right)+i_L[k]\left(1-\frac{T_S R_f}{L}\right) \tag{5.18}$$

Advancing equation (5.18) by one discrete step gives:

$$i_L[k+2]=\frac{T_S}{L}\left(v_{CONV}[k+1]-v_O[k+1]\right)+i_L[k+1]\left(1-\frac{T_S R_f}{L}\right) \tag{5.19}$$

Subsequently substituting $i_L[k+1]$ that is described by equation (5.18) into equation (5.19) results in the deadbeat control law being states as follows:

$$v_{CONV}[k+1]=\frac{L}{T_S}\left(i_L[k+2]-\left(1-\frac{T_S R_f}{L}\right)^2 i_L[k]\right)-\left(1-\frac{T_S R_f}{L}\right)v_{CONV}[k]+v_O[k+1]+\left(1-\frac{T_S R_f}{L}\right)v_O[k] \tag{5.20}$$

The voltage $v_O[k+1]$ can again be predicted as described in section 4.3. The proposed control law can subsequently be directly employed for the control of the alpha-and beta-voltages of the stationary reference frame, thanks to the independent behaviour of these voltages as proven in section 3.2. Figure 5-10 shows a simulated result of the controller's performance. The three-phase system was subjected to a large load step. The load step occurs from 73 ms to 128 ms and can be seen from the obvious reduction in output voltage while the output current is kept constant through the load step.

5.3.3.2 Simulated Performance

The controller was simulated in a three-phase VSI that was subjected to a load step to determine if the controller is capable of sustained reference tracking under varying load conditions. Figure 5-10(a) shows the inductor alpha- and beta current of the VSI. The instant the load step is engaged and released can be seen from Figure 5-10(b). These simulation results in the controller performing exceptionally when compared to the current controller in section 5.3.2.

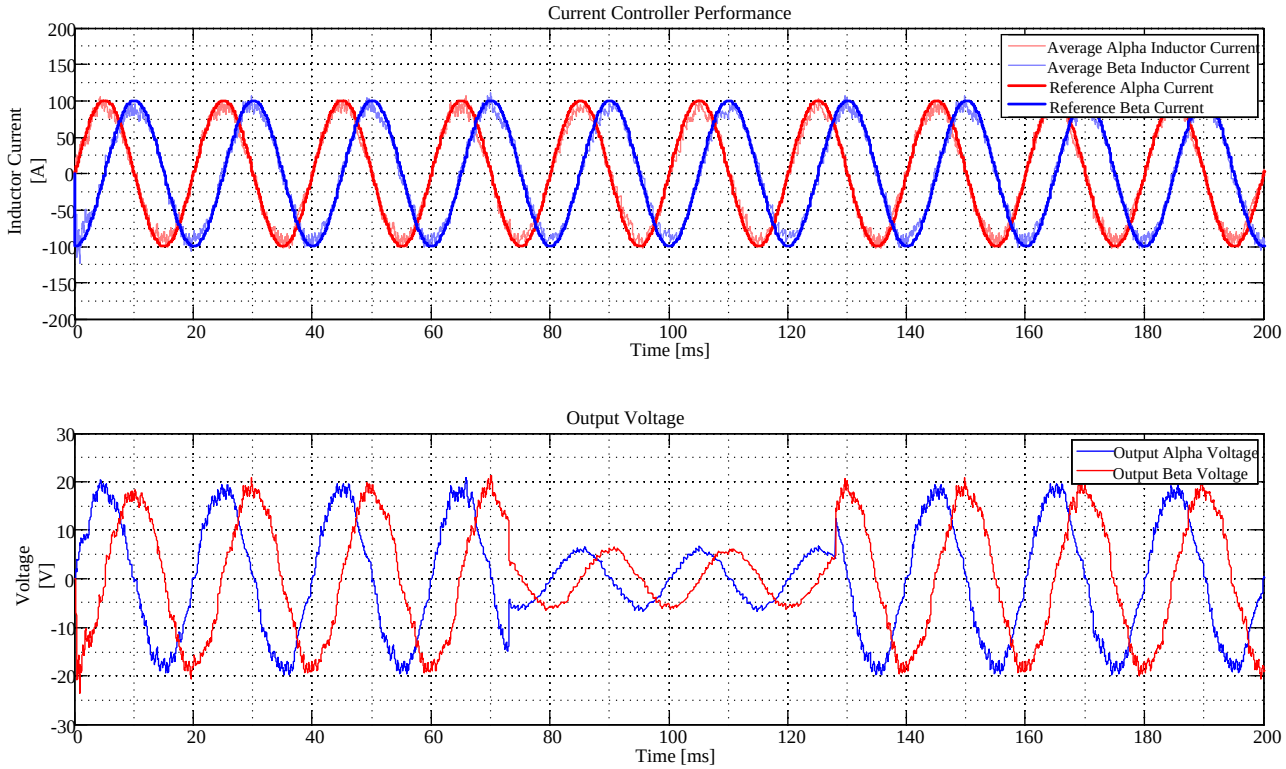

Figure 5-10: Two-Cycle Predicted Current Controller Performance

5.3.4 Conclusion

Analysis of the simulated results show that the current controller based on a two-cycle prediction performs much better that the controller proposed by Chen. No phase lag is present and reference tracking is sustained under varying system conditions. It can be seen that the proposed control method provides the capability of ensuring very accurate reference tracking. The utilisation of the closed-loop current controller effectually results in the VSI operating as a controlled current source with a predefined system response and tracking capability [31].

5.4 Voltage Control Strategies

The previous section provided a means of accurately controlling the VSI as a controlled current source. It is however desirable to operate the VSI as a controlled voltage source in the line-interactive UPS. To achieve

this, an additional controller is required that will ensure accurate reference tracking and fast system response under various load conditions. It is for this reason that numerous control approaches and strategies are proposed in the subsequent sections. These controllers are analysed, compared with each other and finally compared to a base case system. The base case system is a simple open-loop voltage controller. The intention of comparing to a base case is to gauge the proposed controllers' capabilities.

Figure 5-11 provides a graphical depiction of where the focus is in the control of the VSI. After establishing a sound controller that is capable of providing accurate current performance under numerous load situations, the current controller must be automatically regulated by an external control loop. Figure 5-11 furthermore shows how the proposed multi-loop control topology is employed. The inner control loop is controlled by the external outer loop which in turn is driven by the output voltage of the VSI.

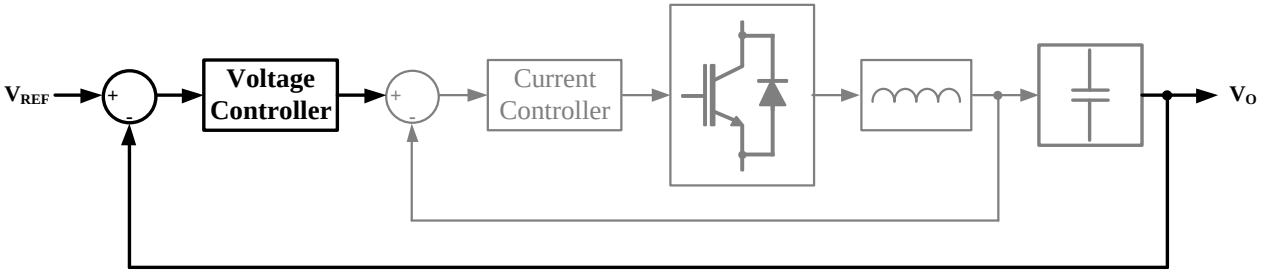

Figure 5-11: Focus on UPS Output Voltage Controller

To provide a low impedance path to the load in the frequency spectrum of the voltage controller, the converter output must be capacitive [31]. It therefore necessitates the inclusion of capacitors on the output. These output capacitors have the additional advantage of providing partial power factor correction and give the UPS an energy storage capability to sustain the load in the absence of a primary energy source [31]. Even though this provides an obvious advantage from the load's perspective, it will be shown that these output capacitors can impede the tracking capability of closed-loop voltage controllers.

In section 5.2 a model of the VSI were derived where it was concluded that the output voltage can be described by equation (5.9). The equation shows that the output voltage can be controlled by only considering the capacitor voltage of the second-order output filter. When trying to design a voltage controller that is capable of controlling a wide spectrum of loads, it is required to determine the load that will result in the worst possible situation. This is achieved by considering the transfer function of the converter from the voltage controller's perspective. Equation (5.9) shows that the transfer function can be expressed solely in terms of the filter capacitor. Therefore the transfer function as seen by the voltage controller, is given as:

$$G_V(s)=\frac{1}{sC_{filter}} \tag{5.21}$$

The simplest load is a purely resistive load. Suppose a low Ohmic resistor is driven by a converter which corresponds with a high power flow through the converter. The transfer function will subsequently be augmented resulting in $G_V(s)$ being expressed as:

$$G_V(s)=R_{load}\|\frac{1}{sC_{filter}} = \frac{R_{load}}{sC_{filter}R_{load}+1} \tag{5.22}$$

To determine the worst load condition, consider the bode-plots and open-loop root loci of these respective representations of the system in Figure 5-12. Analysis of these system responses shows that a system consisting of only the output capacitors is more prone to instability. It can conclusively be said that the closed-loop controller must be designed for the worst-case scenario. Stability under worst-case circumstances will ensure stability under other circumstances. It should however be noted that to ensure stability for the worst possible case, some of the controller's capabilities need to be sacrificed. Such a sacrifice would for example be to give up some of the bandwidth of the controller to ensure stable operation over a larger range of load conditions.

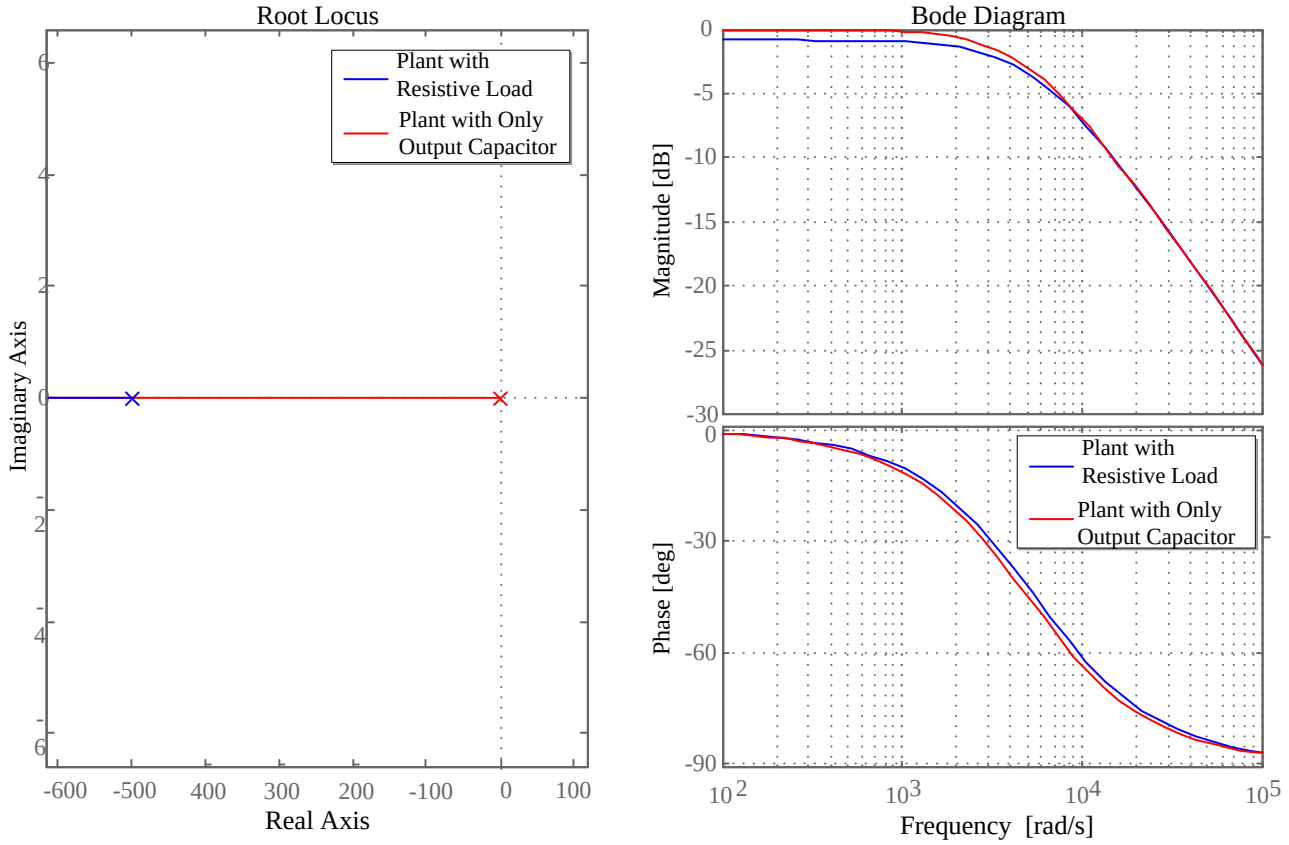

Figure 5-12: System Root Loci and Bode Plots

The current controller proposed by Buso et al was discussed in section 5.3.3. This control approach provides the best control performance of all the current controllers considered in this project. It is for this reason that this controller is used in the inner loop of the multi-loop topology. The current controller operates at a

considerably higher bandwidth (i.e at the switching frequency) with respect to the bandwidth of the voltage controller. The current controller's magnitude response can thus be approximated as constant unity with respect to the voltage controller. It is however important to note that this is only true if the bandwidth of the inner loop is considerably higher than the bandwidth of the controller in the outer loop. As discussed in section 5.3.3, the controller is based on a two-cycle prediction to achieve accurate reference tracking. In other words, if a reference signal is input to the current controller at $t=kT_S$, it will only realise the reference current after two switching periods. Taking into consideration its unity gain along with its two-cycle delay, the current controller can be modelled as a Padé approximated two-cycle delay:

$$G_I(s)=\frac{1-T_S s}{1+T_S s} \tag{5.23}$$

The transfer function of the current controller is therefore used in the control of the subsequent voltage controllers.

5.4.1 Open-Loop Voltage Controlled

5.4.1.1 Principle of Operation

With the objective of establishing a base-case the performance of a VSI that is controlled by an open-loop controller is investigated. No closed-loop strategy is employed for the control of either the output inductor current nor the output voltage. For this reason, the dead-time compensation scheme proposed in section 3.4 cannot be implemented. It is however imperative that a certain amount of blanking-time be introduced between the top- and bottom IGBTs of the respective converter legs to prevent cross-conduction between the voltage rails. It was made clear in section 3.4 that this blanking time affects the output voltage when the output current is positive as well as negative; the approximate loss of output voltage over a 200 μs period therefore amounts to:

$$\begin{aligned} V_{O(LOSS)} &= \frac{9.6}{200}400 \\ &= 19.2 \text{ V} \end{aligned} \tag{5.24}$$

5.4.1.2 Simulated Performance

The three-phase system depicted in Figure 5-13 was simulated in Simplorer where a 300 % load step was performed on the system. As explained in the previous section, no dead time compensation method was included in the simulation to correct for the errors made due to the included blanking time between the top and bottom IGBTs.

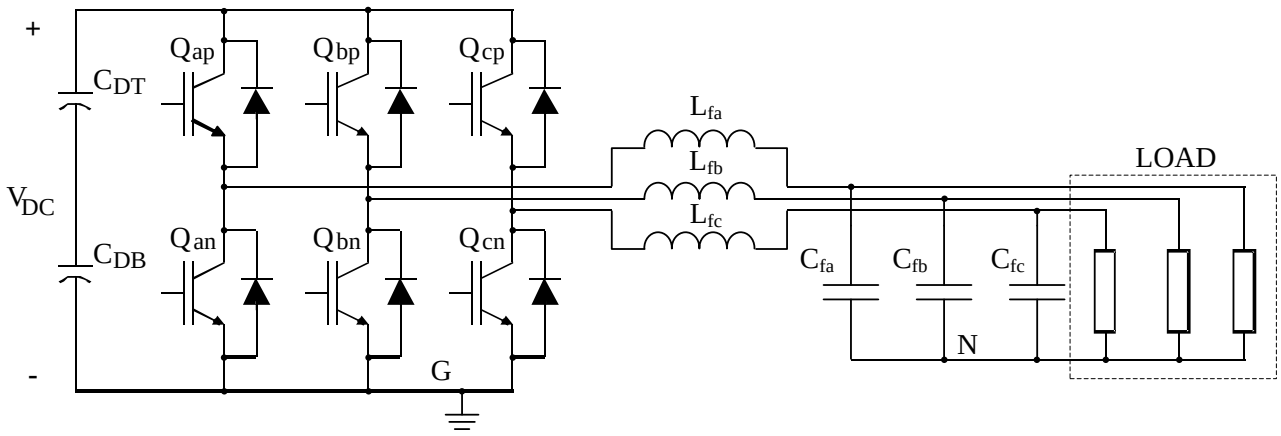

Figure 5-13: Simplorer Simulation Three-Phase Open-Loop VSI Model

The operating parameters of the simulated system are given in Table 5-1.

Table 5-1: Open-Loop Simulation Parameters

Simulated System Parameters	
Parameter	**Value**
V_{DC}	760 V
L	400 µH
C	200 µF
f_S	5 kHz
Blanking Time	5 µs
Load Step	3.33 Ω
Load Release	10 Ω

The results of the simulation are depicted in Figure 5-14. Figure 5-14 (a) shows the output alpha- and beta voltages of the system along with the respective reference voltages. The reference magnitude was set to 400 V and it can be observed that the output voltage magnitude is lower than the commanded 400 V. In fact, the simulated magnitude of the output voltage is approximately 380 V, which closely corresponds with the calculated voltage loss determined by equation (5.24).

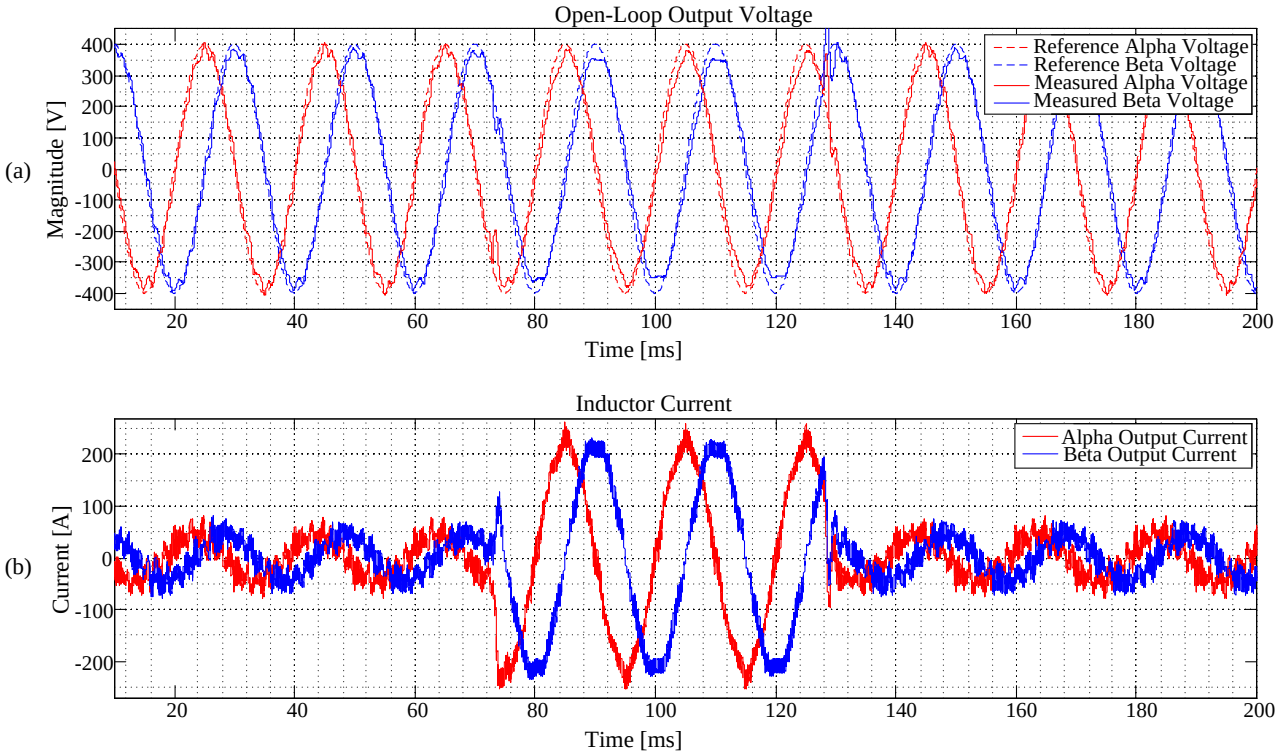

Figure 5-14: Simplorer Results of Open-Loop Controlled VSI

Apart from the implied ramifications on the magnitude of the output voltage, the open-loop controller also loses reference tracking at the peaks of the voltage which is a clear indication of the inability of this control scheme to compensate for output voltage distortions. In the subsequent sections several approaches to control the output voltage and attempt to minimise and even mitigate these distortions will be presented and discussed.

5.4.2 Alpha-Beta Control: A Classical Control Approach

5.4.2.1 Principle of Operation

In section 3.2 it was shown that the Clarke transform provides the ability to control a three phase balanced symmetrical system within a 2-DOF coordinate system. Therefore, the control effort is optimised by 33 % since only two voltage vectors (V_α and V_β) need to be controlled instead of every single voltage of the three-phase system. Ensuring balance and good tracking of the alpha- and beta voltages will consequently ensure similar performance in the three-phase voltages.

The first approach that is taken in the control of the output voltage is to start with a very basic control scheme. The purpose of this approach is to gauge the system's controllability and at the same time determine the capability of a controller based on classical control theory. Classical control theory provides a means of controlling the output voltage by utilising a simple PI controller. The time domain equivalent of the controller output can be defined as:

$$u_C(t)=K_P e(t)+K_I\int_0^t e(t)dt \tag{5.25}$$

for all time t. The variable u_c represents the control variable produced by the voltage controller based on the voltage error $e(t)$ between the reference and actual voltage. Figure 5-15 provides a graphical depiction of the proposed control scheme. It can be seen that both the alpha- and beta voltage paths are controlled with two identical PI controllers. These controllers are totally independent from each other because section 3.2 emphasised that the alpha- and beta voltage vectors operate independently from each other.

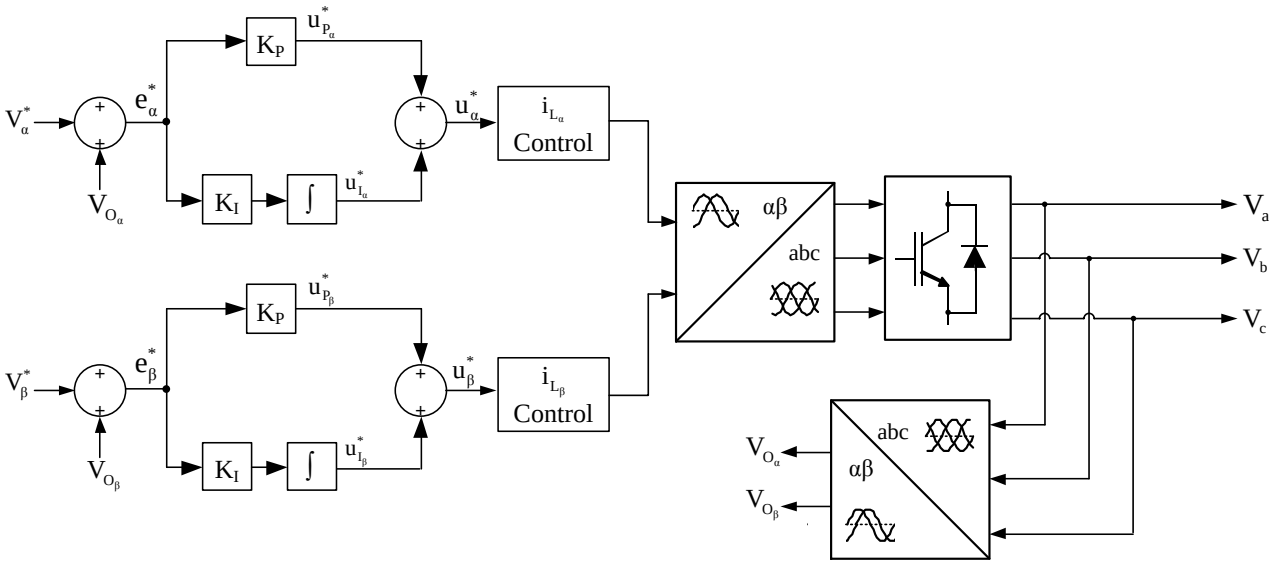

Figure 5-15: A Simple PI Control Proposal

As discussed at the beginning of section 5.4, it is desirable to design the controller for the worst possible load condition. It has been identified that an open-circuit load condition will be the worst case where only the capacitors of the second-order filter will be connected. It would therefore make sense to design the controller for a system with this load condition. The question however now arises as to how the influence of the load can be modelled in the system. To achieve this, the load needs to be included in the model of the system. An accurate compromise is to describe the system according to equation (5.21) but to include a load with a high Ohmic value in parallel to the output capacitor. This effectively describes the system as a parallel combination of the output capacitor and an open-circuit. The transfer function that is used in the design of the voltage controller is described by equation (5.26):

$$\begin{aligned} G_V(s) &= Z_{load} \| \frac{1}{sC_{filter}} \\ &= \frac{Z_{load}}{sC_{filter}Z_{load}+1} \end{aligned} \tag{5.26}$$

The motivation for including the load in the model is that doing so will ensure the controller's awareness of the load behaviour. Following the fundamentals of classic control theory, the open-loop transfer function of

the system consists of the PI controller, current controller and plant model. The open-loop transfer function is therefore described as:

$$G_{OL}(s)=\left(K_P+\frac{K_I}{s}\right)\left(\frac{1-T_S s}{1+T_S s}\right)\left(\frac{Z_{load}}{sC_{filter}Z_{load}+1}\right) \tag{5.27}$$

To ensure system stability over the complete bandwidth range of the voltage controller, the transfer function at the control bandwidth ω_{CL} must equal -1. In other words, $G(j\omega_{CL})=-1$ which corresponds with the well-known magnitude and phase criterion. The magnitude criteria requires that $|G(j\omega_{CL})|=1$ which produces equation (5.28):

$$K_P^2+\left(\frac{K_I}{\omega_{CL}}\right)^2-(\omega_{CL}C_{filter})^2-\left(\frac{1}{Z_{load}}\right)^2=0 \tag{5.28}$$

Similarly, to ensure that $G(j\omega_{CL})=-1$ the phase criterion requires

$$\angle G(j\omega_{CL})=-180°+n.360 \qquad n = 1, 2, 3, ...$$

Applying the phase criteria on the open-loop system, produces equation (5.29):

$$\omega K_P=K_I\arctan\left(-180°+90°+PM+2\arctan(\omega_{CL}T_S)+\arctan(\omega_{CL}Z_{load})\right) \tag{5.29}$$

where PM represents the phase margin required by the voltage controller. Note that equations (5.28) and (5.29) now provide a means of determining the control gains K_P and K_I according to the design specifications ω_{CL} and PM.

According to [31], it is advisable to choose the voltage controller's bandwidth in the order of ten times the fundamental frequency. Therefore the bandwidth can be chosen as $\omega_{CL}=500\ \text{Hz}$. Changes in the load condition such as for example a load step will directly influence the system. This is evident from the fact that the system model is directly dependent on the load. To ensure stability across a wide spectrum of load conditions it is recommended that a relatively large phase margin be chosen. Doing so will ensure that the system poles will be less likely to have a phase larger than 180° and probable consequential instability. A phase margin of $PM = 30°$ is therefore chosen. Under these conditions the control parameters are obtained as:

$$K_P=0.627$$
$$K_I=-144.3\ (\text{rads}^{-1})$$

It can be seen from these controller gains that the system will without a doubt be unstable. Figure 5-16 furthermore proves the system's instability. The bode-plot of the system shows that the system is unstable at the chosen bandwidth frequency of 500 Hz.

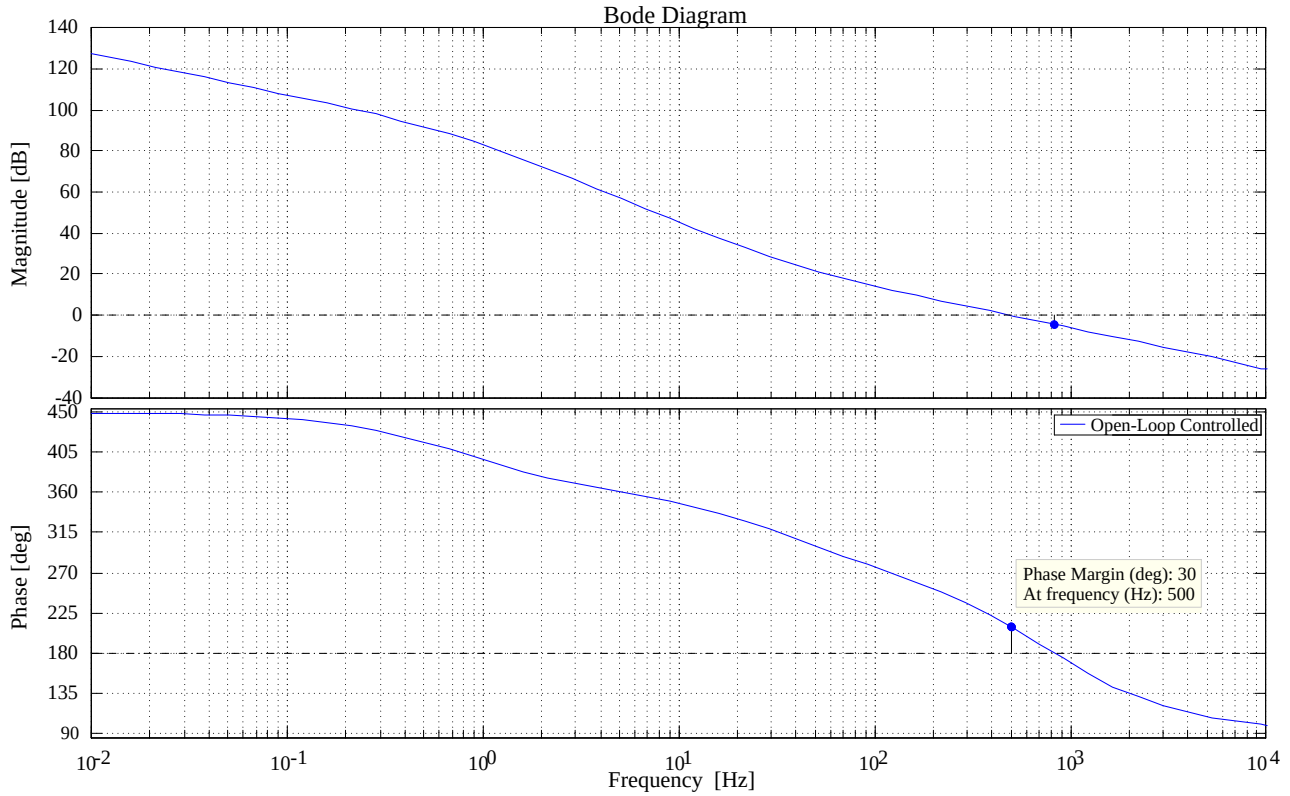

Figure 5-16: Bode Diagram of Initially Proposed PI Controller

It is therefore obvious that a sacrifice needs to be made in the desired control specifications. It is however important that the bandwidth of the system be as high as possible. If it is not, this will result in the controller being incapable of sustaining good reference tracking performance and even ensuring stability under largely varying load conditions such as large load steps. For this reason it can be concluded that the phase margin needs to be sacrificed, which in turn increases the possibility of instability since the locus of the system phase is closer to 180°. If the bandwidth is kept at $f_{CL} = 500\ \text{Hz}$ but the phase margin is lowered to $PM = 5°$, the gains are obtained as:

$$\begin{aligned} K_P &= 0.59 \\ K_I &= 701.2\ (\text{rads}^{-1}) \end{aligned} \tag{5.30}$$

The motivation for choosing such a low phase margin, is that it results in strong integral control capability which in turn ensures good steady state tracking. It may be worrying to see that the phase margin is so low, but the following simulation shows that stability is ensured during a load step. In chapter 6 the system's stability in a practically implemented system will be further demonstated.

Figure 5-17 depicts the results of a simulation done in Matlab. The system was subjected to a load step from a no-load condition to a low Ohmic load drawing approximately 125 A per phase.

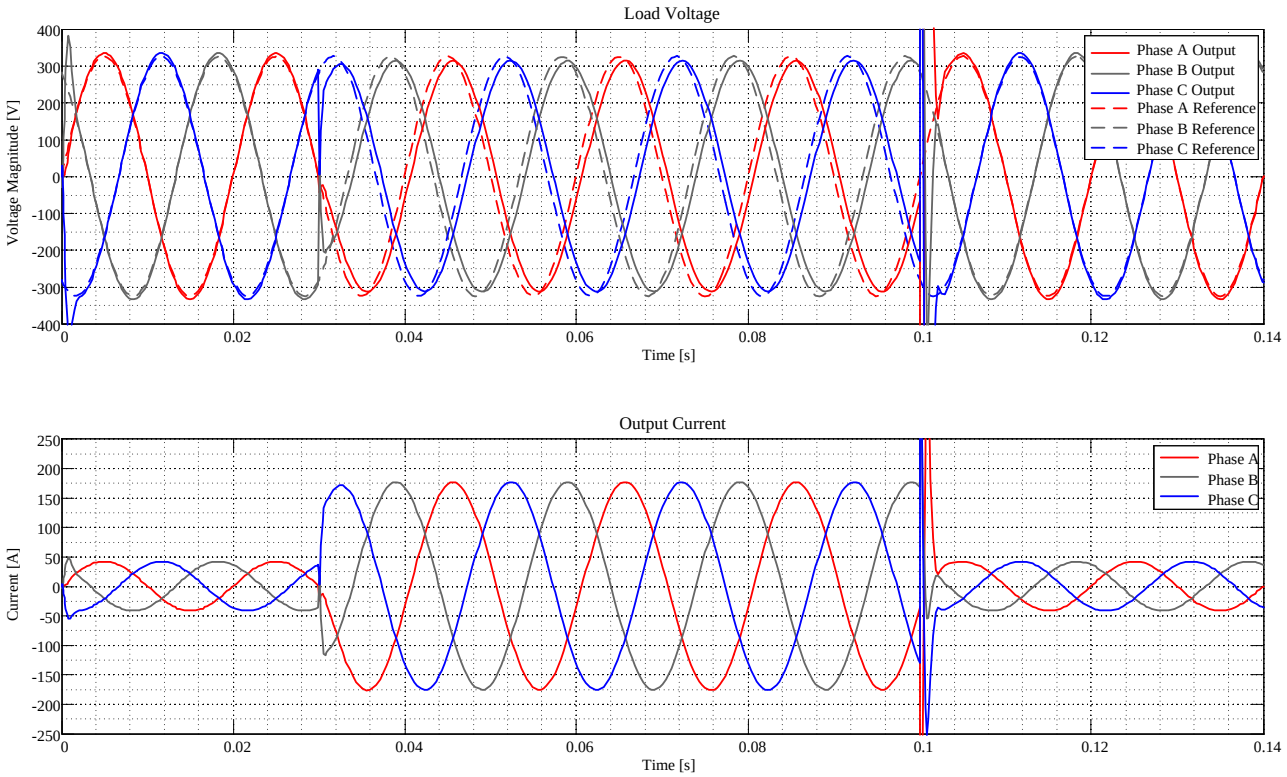

Figure 5-17: Matlab Simulated Performance Results of Proposed PI Control of αβ-Voltages

It can be seen that the system is capable to sustaining stability when a load step is made. A lag in phase of more than 10° is however observed during the load step. The phase lag phenomenon is explained by the incapability of the integrator to remove the steady-state tracking error effectively. The signal that the integrator is attempting to control is a continually varying signal. To further examine this phenomenon the commands of the respective alpha and beta controllers are depicted in Figure 5-18. When focusing especially on the integral command signals, it is evident that the integrator has to compensate for the varying feedback signal continuously.

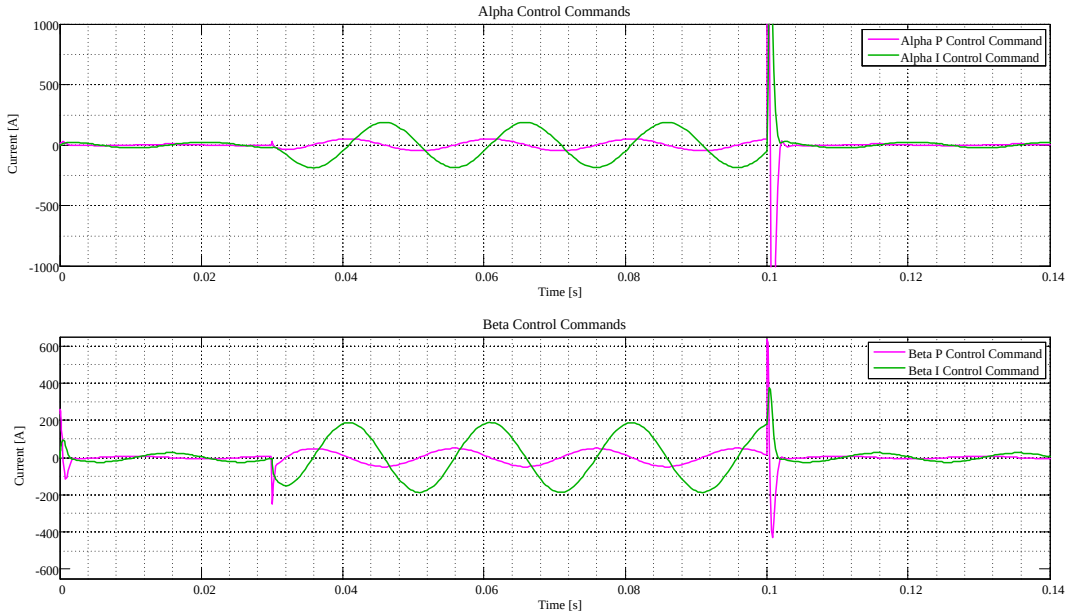

Figure 5-18: PI Control Commands

The integrator is thus never able to compensate for the tracking error completely, due to the alternating characteristic of the "steady-state" signal.

5.4.2.2 Simulated Performance

The three-phase system depicted in Figure 5-19 was simulated in Simplorer where a 300 % load step was performed on the system. The dead time compensation method proposed in section 3.4 was included in the simulation to correct for the errors made due to the included blanking time between the top and bottom IGBTs.

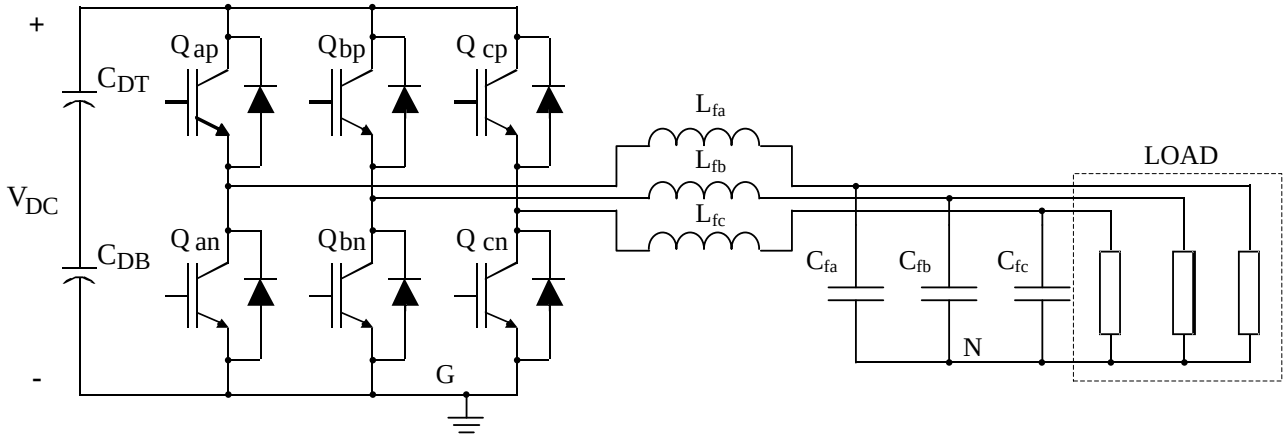

Figure 5-19: Model for Simulation of PI Control of the αβ Voltages Vectors

Furthermore, the controller proposed in section 5.3.3 was used in the inner loop to control the current, since it provided the best performance. Additionally, the integral anti windup scheme discussed in section 4.4 is also included in the simulation. The parameters of the simulated system are given in Table 5-2:

Table 5-2: Simulation Parameters of PI Controller

Simulated System Parameters	
Parameter	**Value**
V_{DC}	800 V
L	400 µH
C	200 µF
f_S	5 kHz
Dead Time	5 µs
Load Step	3.33 Ω
Load Release	10 Ω

Figure 5-20 (a) shows the alpha- and beta- output voltage along with the respective reference voltages. The output alpha- and beta inductor current are also included to point out the instant the load step occurs. Figure 5-20 (b) shows the proportional and integral control command signals for the alpha- and beta voltages respectively. Note that the integrator command signal needs to alternate constantly due to the alternating nature of its input signal. Therefore the integrator is unable to successfully settle and consequently is incapable of completely removing the tracking error.

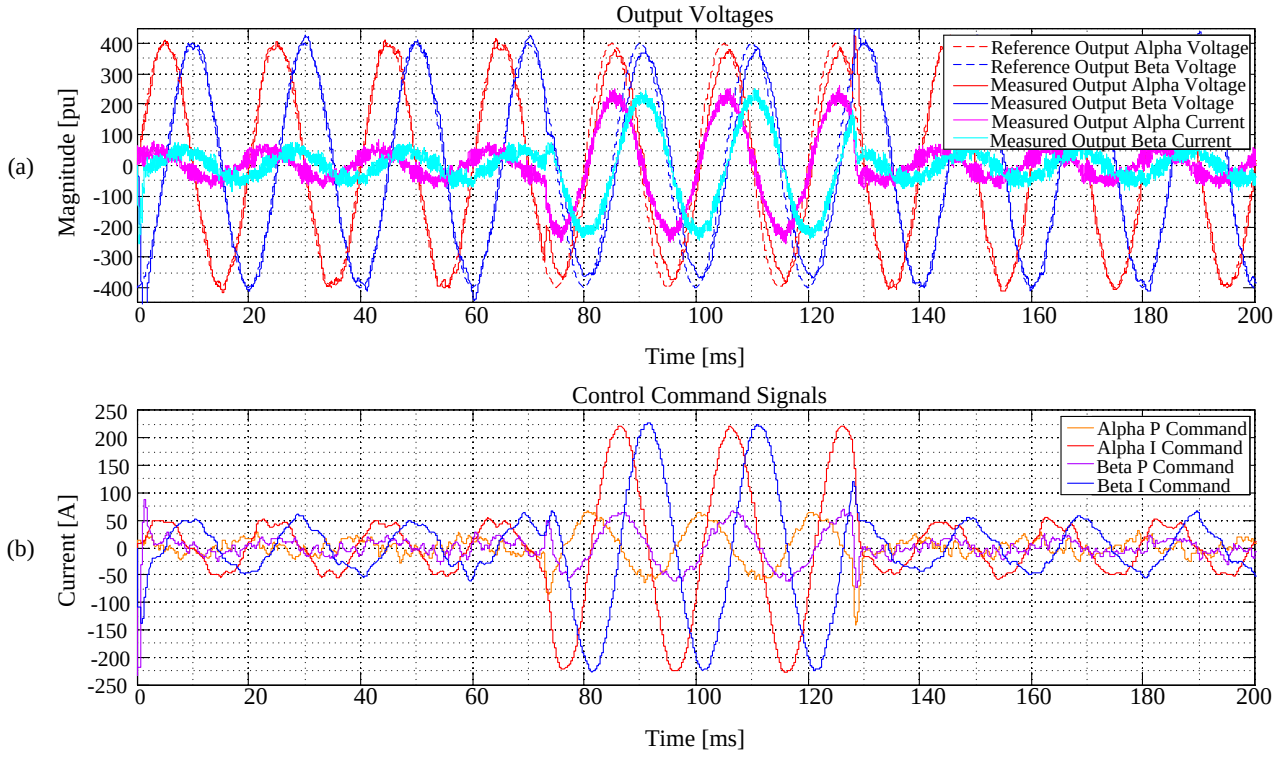

Figure 5-20: Simplorer Results of PI Control of αβ Voltages

To improve the conditions under which the integrator performs, it can conclusively be said that an integrator must control a signal with a relatively low frequency. In the next section this proposal will be discussed in detail. A control approach similar to the controller described in this section, is followed except that the integrator is solely used for the control of the magnitudes of the respective alpha- and beta voltages.
Finally, it is deductible that the controller is able achieve a certain degree of reference tracking, but is highly susceptible to changes in the system's parameters. The poor tracking performance is evident when the load changes (as seen in Figure 5-20 (a)). Therefore, the individual PI control of the alpha- and beta voltages produces unsatisfactory performance results and has very weak dynamic stiffness. It is thus not recommended for the closed-loop control of three-phase output voltages.

5.4.3 Alpha-Beta Control: An Alternative Approach

5.4.3.1 Principle of Operation

In this section the aim is to propose a controller which is an improvement on the one proposed in the last section. It was concluded in the previous section that to ensure good integrator performance it is recommended to utilise an integrator for the control of a signal with a relatively low frequency. It is for this reason that the control approach in Figure 5-21 is suggested.

The alpha- and beta voltage vectors in Figure 5-21 are controlled with a proportional controller whereas the magnitude of the vector $\overrightarrow{\mathbf{V}_{\alpha\beta}^{*}}$ is controlled with an integrator. The integrator command is therefore multiplied by $\cos\omega tu$ and $\sin\omega tu$ respectively to produce the corresponding alpha- and beta commands.

The proposal to control the output voltage magnitude will solve the integrator problem that was described in the previous section. The change in the magnitude of the $\overrightarrow{\mathbf{V}_{\alpha\beta}^{*}}$ vector has a very low frequency. Control of this relatively constant signal will most certainly result in improved integrator performance.

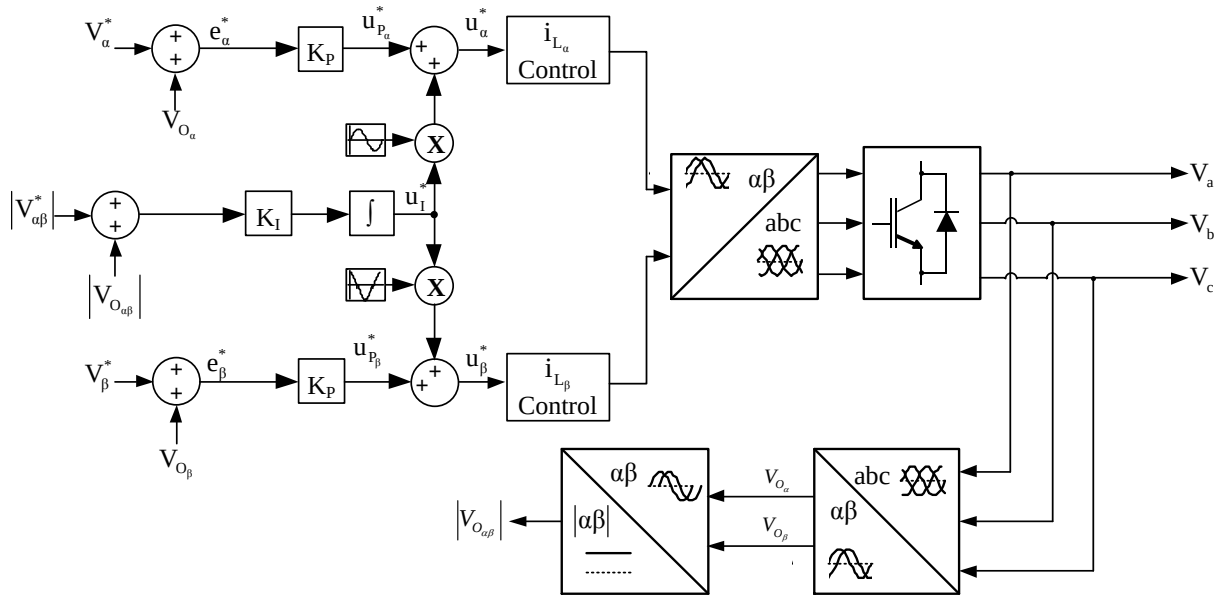

Figure 5-21: Proportional Control of αβ Voltage Vectors and Integral Control of $V_{\alpha\beta}^*$ Vector Magnitude

The consequence of separately controlling the magnitude of the vector is that the controller will observe different models of the system. The model seen by the proportional controllers remains unchanged and therefore exactly as expressed by equation (5.26):

$$G(s)=\frac{Z_{load}}{sC_{filter}Z_{load}+1}$$

The integrator controls the magnitude of the output voltage vectors and this implies that the model that is used in the design of the integrator is different from equation (5.26). However, it is desired to design the system at a considerably lower frequency than the bandwidth of the current controller. As long as the bandwidth of the integrator controller is considerably lower than the bandwidth of the overall voltage controller (ω_{CL}) then K_I can be determined in a similar fashion as in the previous section [31].

The previous controller required a strong integrator to be capable of ensuring reference tracking of the output voltages. The control bandwidth was for this reason chosen high relative to the controller in this section. It is however not as critical to have an integral controller with such a high bandwidth since it controls a low frequency signal. Choosing the control frequency at $f_{CL}=200\,\text{Hz}$, the proportional gain obtained is $K_P=0.213$. The integrator controls the magnitude of the $\overrightarrow{\mathbf{V}^*_{\alpha\beta}}$ vector and therefore has a very low frequency response. Designing the integrator to ensure a constant transient response and a phase margin of $PM=30°$, the integrator gain obtained is $K_I=167.4$.

5.4.3.2 Simulated Performance

The controller was also simulated in Simplorer. Exactly the same system as represented in Figure 5-19 is simulated and the system's parameters are also exactly as expressed in Table 5-2.

It can be seen in Figure 5-22 (b) that the integrator is more appropriately utilised. As observed in Figure 5-22 (a) it is consequently able to remove the tracking errors in the magnitude of the output voltages effectively. The consequence of this is that the control efforts of the proportional controllers are also reduced. It can therefore be seen that by simply using the integrator for the control of a steady-state signal effectually results in a considerable reduction in control noise.

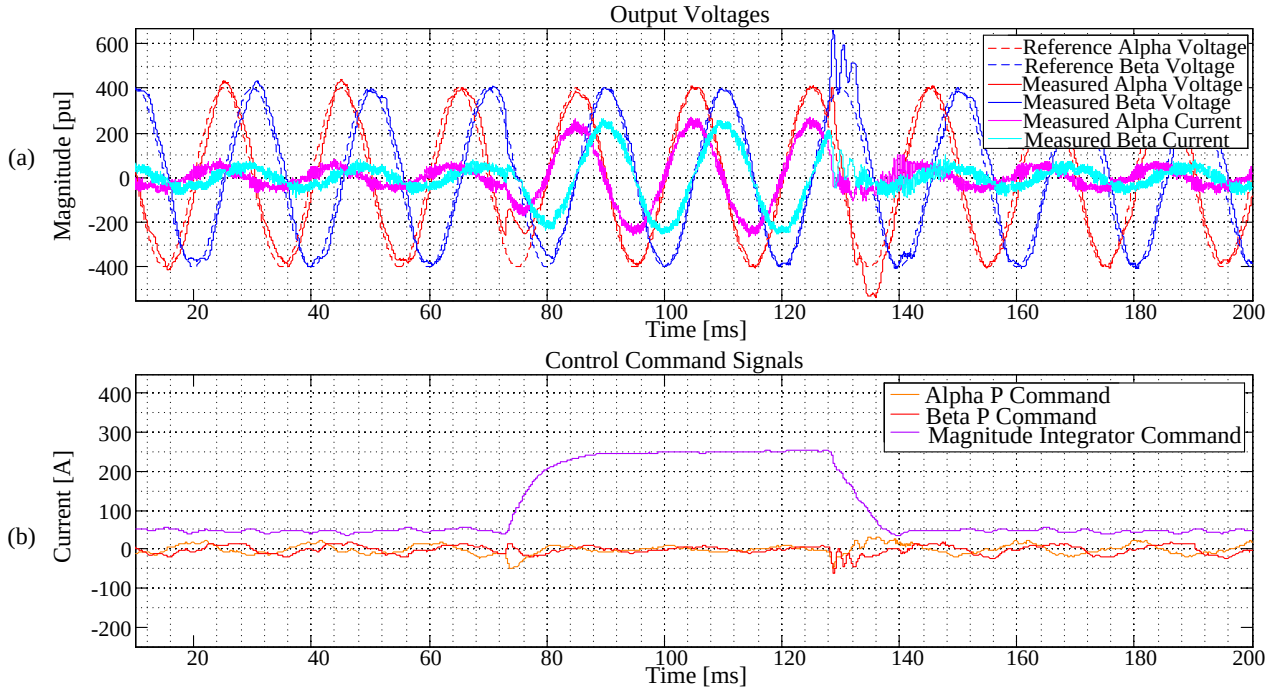

Figure 5-22: Control Performance of αβ-Voltage Controller with additional Integral Magnitude Control

The alpha- and beta output voltages are shown in Figure 5-22 (a). Observe that the controller is capable of ensuring that the magnitude stays constant throughout the load step. The trade-off in achieving this relatively constant output voltage magnitude is a lower bandwidth.

The lower bandwidth can be explained when considering bode plot in Figure 5-23. As explained in section 5.4.1, the system is designed for the case when the load is an open-circuit. The bode-plot shows that the system indeed performs as designed, since it has a phase margin of 30° at 200 Hz. Note however that as the load is increased, the bandwidth of the system is considerably reduced. A phase lag is observed in Figure 5-22 (a) and occurs in the case when a load is connected. The reduced control bandwidth is what causes this phase lag. The phase error is however not of a great concern since it is unlikely that the small phase error ($\approx 3.6°$) will have a significant effect on the load.

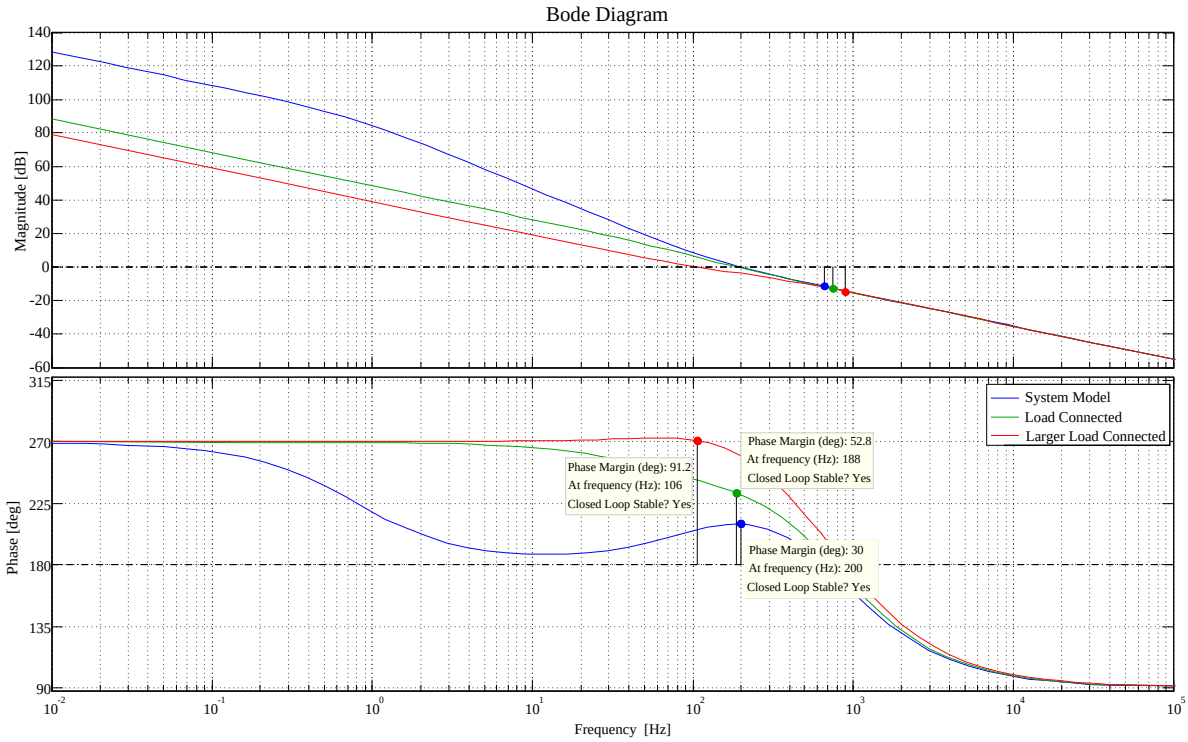

Figure 5-23: Bode-Plots of System with Different Load Impedances

The huge over-voltage phenomenon that occurs when the load is released is of greater concern. It is a direct result of the lower system bandwidth when a large load is connected. The 600 V voltage spike is unacceptable and deviates considerably from the specifications set out in both the local NRS-048 [13] and international IEC 62040-3 specifications [9].

In conclusion, this controller is an improvement on the previous controller in that it is capable of achieving a good magnitude response, but loses tracking when a load release occurs. The resulting over-voltage is unacceptable and thus the use this controller to control the three-phase output voltages of a VSI is not advisable..

5.4.4 Direct-Quadrature (DQ) Controller

5.4.4.1 Principle of Operation

The controllers in sections 5.4.1 and 5.4.3 both operate in the stationary frame reference. The voltage vectors are continuously rotating at the angular velocity of the output voltages. The controller proposed in section 5.4.3 showed that an integrator is capable of more effectively controlling a relatively constant signal. The controller is even capable of achieving near zero tracking error of the reference signal. In general, AC regulators perform unsatisfactorily since a conventional PI controller suffers significant steady-state amplitude and phase errors.

In section 3.3 the direct-quadrature transform and the advantage it provides by transforming a rotating voltage vector in the stationary reference frame to a static vector in a rotational reference frame were discussed. In effect, the Park transform converts a three-phase AC system to a two-phase based DC system. The static characteristic of the voltage vector provides a great opportunity to use the inherent characteristic of the integrator to remove the steady-state tracking error.

The synchronisation of the rotational reference frame with the angle of $\overrightarrow{\mathbf{V}^*_{\alpha\beta}}$ produces a constant D- and Q signal under ideal conditions. Considering that the controller in section 5.4.3 was able to control a DC signal quite effectively, it is clear to say that controlling a constant D- and Q signal can improve the capabilities of the voltage controller. It is therefore worthwhile to investigate the effectiveness of controlling of these DC signals to produce the output voltages. Buso [31] proposed a method of controlling the inductor current based on the DQ reference frame. This proposal was used as a foundation for the derivation of a voltage controller that is similarly based in the DQ reference frame.

Zmood points out in [50] that a controller in the synchronous reference frame operates on DC quantities and is therefore capable of providing infinite gain and consequently achieving zero steady-state error. The DQ transform shifts the AC reference sinusoids to the DC frequency region. The result is that a conventional PI controller can now operate in a DC environment. The proportional term is independent of frequency and the integral gain is effectively infinite in the DC system. Consequently the transient response is totally determined by the proportional term thanks to its frequency independence. The steady-state response is in turn solely determined by the integral term. The DC environment therefore provides the advantage that the transient and steady-state responses can be analysed separately. The control scheme depicted in Figure 5-24 is thus proposed.

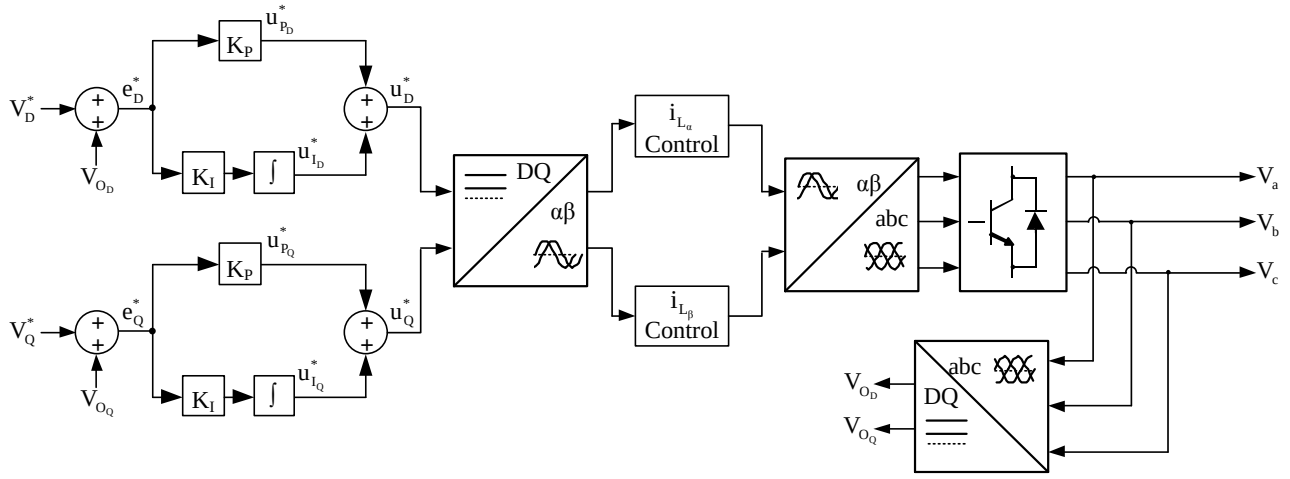

Figure 5-24: PI Controller based on the DQ Reference Frame

The conversion of the ABC voltages to equivalent DQ voltages is achieved by using equation (3.8), and conversion of the DQ voltage vectors back to the stationary reference frame is achieved by using equation (3.10). With the objective of achieving good reference tracking on the output voltage, it was recommended in section 3.3 that the $\overrightarrow{V_{DQ}^{*}}$ vector should be synchronised with the D-axis of the rotational reference frame. So doing ensures that the rotation of the reference vector is sustained at the angular velocity of the rotational reference frame and has a constant magnitude equivalent to the required magnitude of the output voltages. It is therefore advisable to drive the D-component to 400 V and the Q-component to 0 V.

To obtain a controller bandwidth of f_{CL} = 400 Hz, the proportional gain is obtained as K_P = 0.49. Similarly, to achieve a phase margin of PM = 25°, the integral gain is chosen as K_I = 270.87.

5.4.4.2 Simulated Performance

To determine the performance of the PI controller that is based in the DQ rotational reference frame, the three-phase system depicted in Figure 5-19 is simulated under exactly the same conditions and system specifications as set out in Table 5-2. A load step that is identical to the simulations in sections 5.4.1 and 5.4.3 is again performed. So doing it ensures a good comparison of the DQ controller with the other proposed control schemes.

The reference voltage $\overrightarrow{V_{DQ}^{*}}$ was constructed by driving its D-component with a constant 400 V signal and its Q-component with a 0 V signal. In Figure 5-25 simulated performance results of the respective D and Q output voltages which correspond with the D- and Q components of the reference vector are shown.

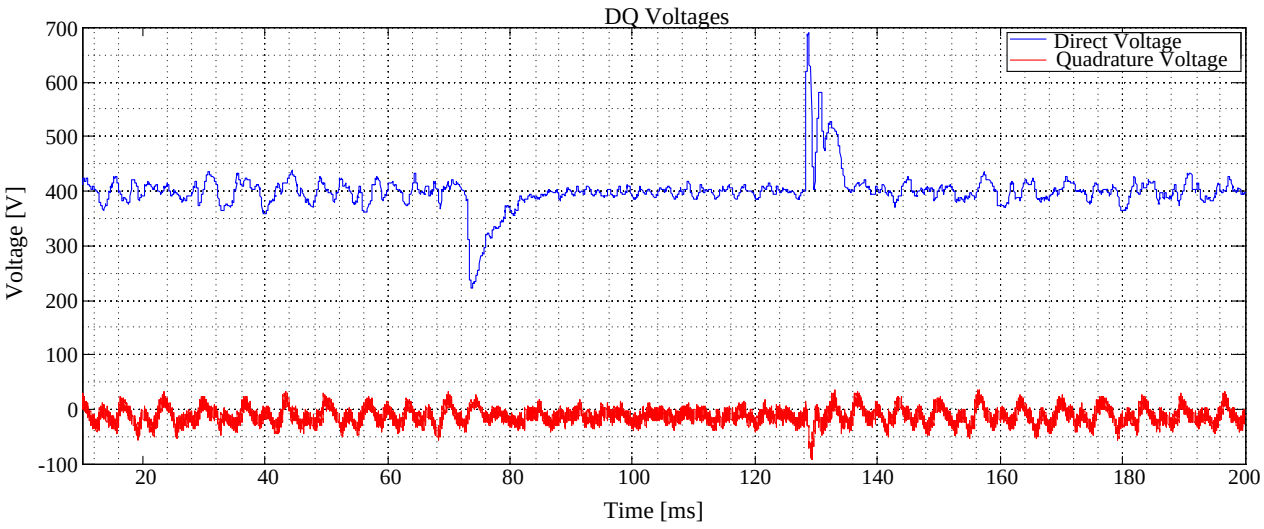

Figure 5-25: Simulated Direct- and Quadrature Voltages of DQ Controller

In power systems, the D voltage corresponds with active power being delivered by the VSI, since the voltage vector is in phase with the angular velocity of the output and therefore the output current. Similarly, the Q voltage corresponds with reactive power delivered by the VSI. It can be seen that the quadrature voltage is successfully controlled around zero. The voltage controller attempts to transfer purely active power to the load. It is often the case that the load is not purely resistive and therefore incapable of only drawing active power. A phase difference between the output voltage and output current will thus be observed. The current controller ensures that this phase difference is correctly maintained between the output voltage and the output current.

The capacitors of the output filter also draw reactive power from the VSI. The slight deviation from zero on the quadrature voltage is therefore due to the reactance of these output capacitors. It can however be seen in Figure 5-25 that the DQ controller is capable of sustaining the reactive power requirements of the load throughout the entire load step. The load step corresponds with a step in active power being drawn from the VSI. It is therefore obvious that transients are observed in the D voltage of the output. Figure 5-26(a) shows the output alpha- and beta voltages along with the corresponding inductor current. It is clear that the DQ controller is capable of ensuring excellent steady-state tracking of the reference. The tracking error is indeed also zero. No phase error is observed and the reference is followed much more successfully than by the previously proposed controllers.

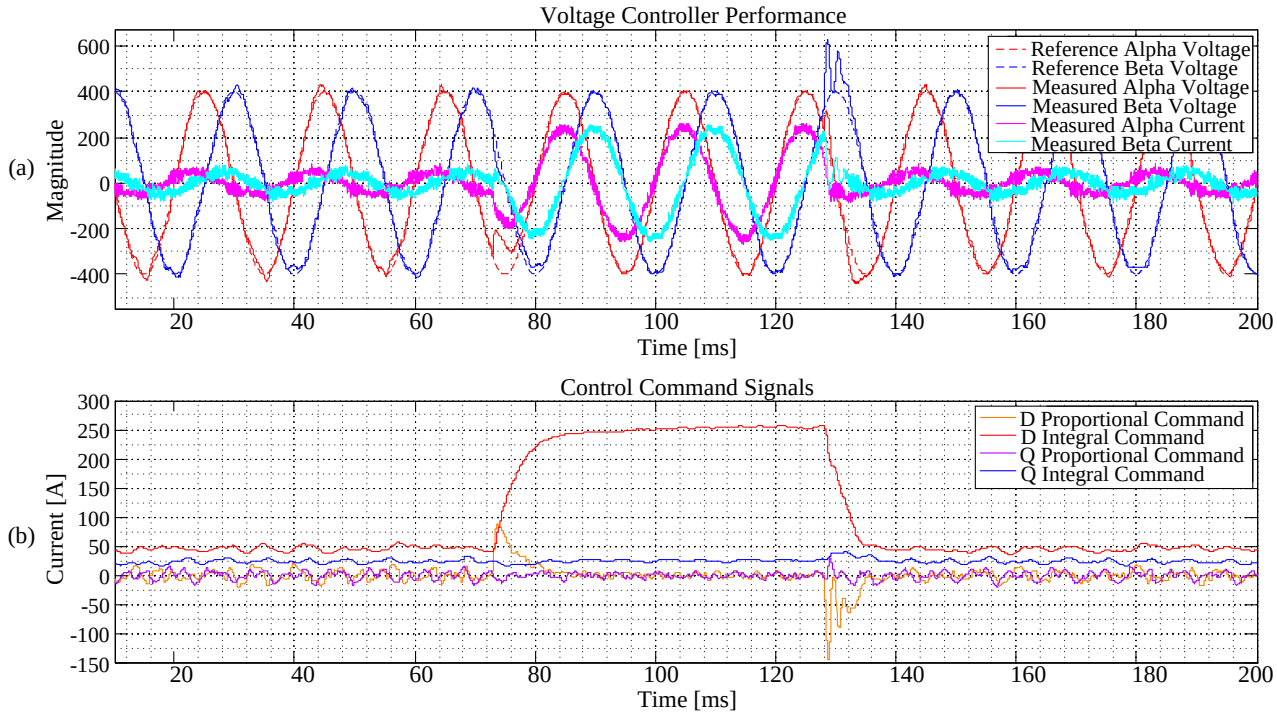

Figure 5-26: Simulated Performance of PI Control of the D- and Q Voltages

Figure 5-26(b) shows the control commands of the proportional and integral controllers on the D- and Q voltages respectively. It is observed that the quasi DC nature of the D and Q voltages indeed improves the capability of the controller to achieve near zero tracking error. The controllers are able to produce a

command that corresponds with the power demands of the load. The DC nature of the D and Q voltages ensures that little strain is put on the proportional controller and results in the P controller to remove higher frequency transient errors more successfully.

The overshoot of the output voltage however is again of great concern. The cause of this over-voltage is the low bandwidth of the controller. The controller is as a consequence unable to remove this high frequency transient behaviour. It would thus seem obvious to increase the bandwidth of the controller. The problem with this increase is that the bandwidth can not be increased since an excessively high bandwidth will result in the controller operating more closely to the instability threshold. The advantages gained from using a two-prediction current controller results in the disadvantage of introducing a two cycle delay in the system. The delay causes a reduction in the range of stable operation of subsequently designed voltage controllers.

Apart from the overshoot that occurs under a load release condition, the DQ controller performs exceedingly better than the controllers proposed thus far.

5.4.5 P+Resonant Controller

5.4.5.1 Principle of Operations

The DQ controller showed that the settling time of the integral controller is undesirably long in the presence of step variations. The problem can effectively be solved by considering an alternative implementation of the integrator in Figure 5-27. The Park transform can be expressed as the multiplication of a vector $\overrightarrow{e_{\alpha\beta}}$ by the complex vector $e^{j\theta}$. Buso [31] shows that a parallel structure (shown in Figure 5-27) can be obtained by reconstructing the αβ-vector from the direct and inverse Park sequences. Based on this parallel structure, the integrator can be implemented by using the direct and inverse Park transform. The error vector $\overrightarrow{e_{\alpha\beta}}$ that is produced from the difference between the reference signal and the output feedback is thus used as input to reproduce the stationary reference frame equivalent vector $\overrightarrow{V_{\alpha\beta}}$.

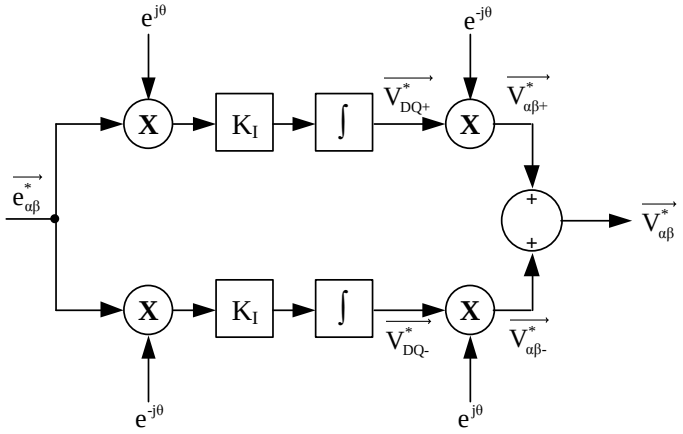

Figure 5-27: Rotational Reference Frame Equivalent Integrator

According to [31] and Carnieletto et al [51] the transfer function $\frac{\overrightarrow{V_{\alpha\beta}}}{\overrightarrow{e_{\alpha\beta}}}$ can thus be expressed by equation (5.31):

$$\begin{aligned}\frac{\overrightarrow{V_{\alpha\beta}}(s)}{\overrightarrow{e_{\alpha\beta}}(s)} &= \frac{\overrightarrow{V_{\alpha\beta+}}(s)}{\overrightarrow{e_{\alpha\beta+}}(s)} + \frac{\overrightarrow{V_{\alpha\beta-}}(s)}{\overrightarrow{e_{\alpha\beta-}}(s)} \\ &= \frac{K_I}{s+j\omega} + \frac{K_I}{s-j\omega} \\ &= \frac{2K_I s}{s^2+\omega^2}\end{aligned} \tag{5.31}$$

The implementation of the integrator from the direct and inverse Park transforms provides the added advantage that the integrator functions as a second-order resonant band filter at a selective frequency ω. The integrator now also functions as a resonant controller which resonates at the angular velocity at which the synchronous reference frame rotates. The resonant controller functions in the DQ coordinate system and therefore is used for the control of quasi DC signals. Furthermore, the resonant controller has infinite gain at the resonant frequency and can achieve zero steady-state tracking error in the rotating reference frame [51] thanks to the DC characteristics of the signals in the DQ coordinate system.

It has been established that the proportional controller is frequency independent, which implies that the direct and inverse Park transform does not have an effect on the proportional controller, as it has on the integrator. The proposed control transfer function is therefore described by equation (5.32):

$$D(s)=K_P+\frac{K_I s}{s^2+\omega_O^2} \tag{5.32}$$

where ω_O represents the chosen resonant frequency of the controller. Increasing the gain of the filter reduces the selectivity of the filter but provides a shorter settling time. Conversely, if the gain is decreased it results

in stronger filter selectivity but a longer settling time. In effect the resonant controller can be tuned in a similar way a band-pass filter's quality factor is tuned.

5.4.5.2 Simulated Performance

Again this controller is simulated in a three-phase VSI that is identical to the simulation model used in the previous controllers. The system's parameters are again exactly the same as given by Table 5-2. The D- and Q voltages of the output are depicted in Figure 5-28.

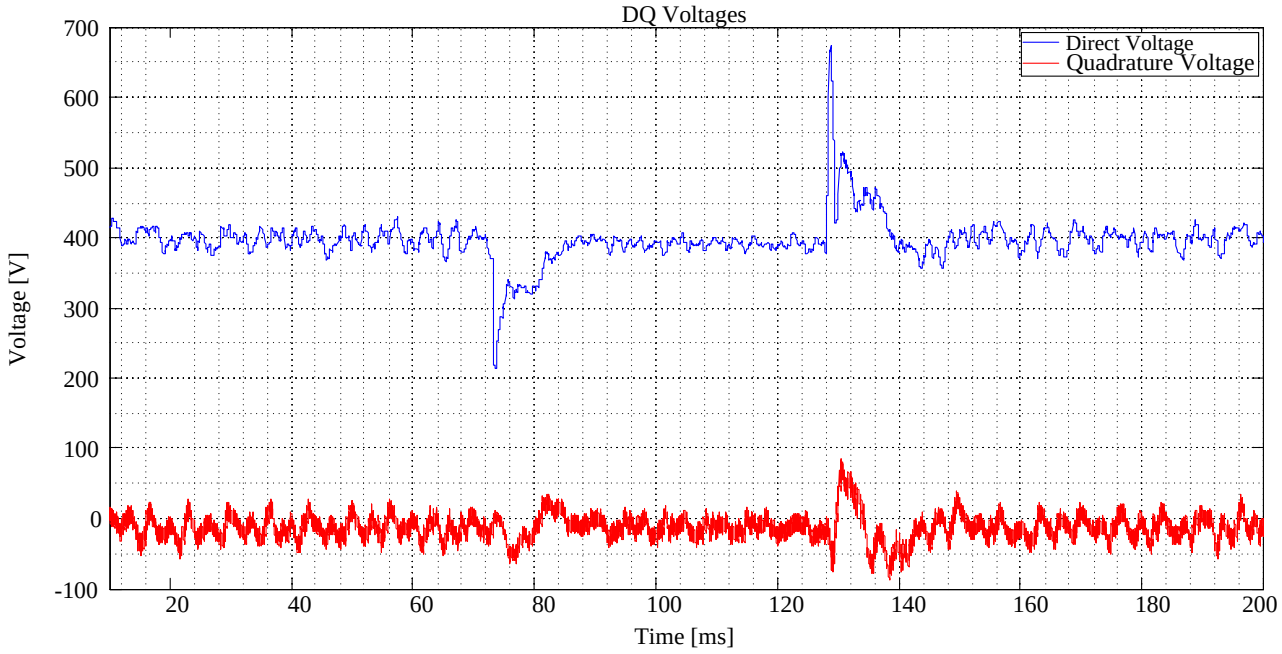

Figure 5-28: Simulated D- and Q Voltage of P+Resonant Controller

Examination of Figure 5-28 illuminates the fact that the P+Resonant controller achieves at least the performance capabilities obtained by the DQ controller. Similar transients are observed on the D voltage at times $t \approx 73\,ms$ and $t \approx 127\,ms$. These transients are similar to the transients produced by the DQ controller which can be observed in Figure 5-26. Furthermore, similar small transients can be seen on the Q voltage at the same time instants. These transients are caused by the gain of the resonant controller being extremely smaller at frequencies that do not equal the resonant frequency ω_0. The bode diagram of the resonant controller is depicted in Figure 5-29 and shows that the controller's gain is lower at frequencies that deviate from the resonant frequency.

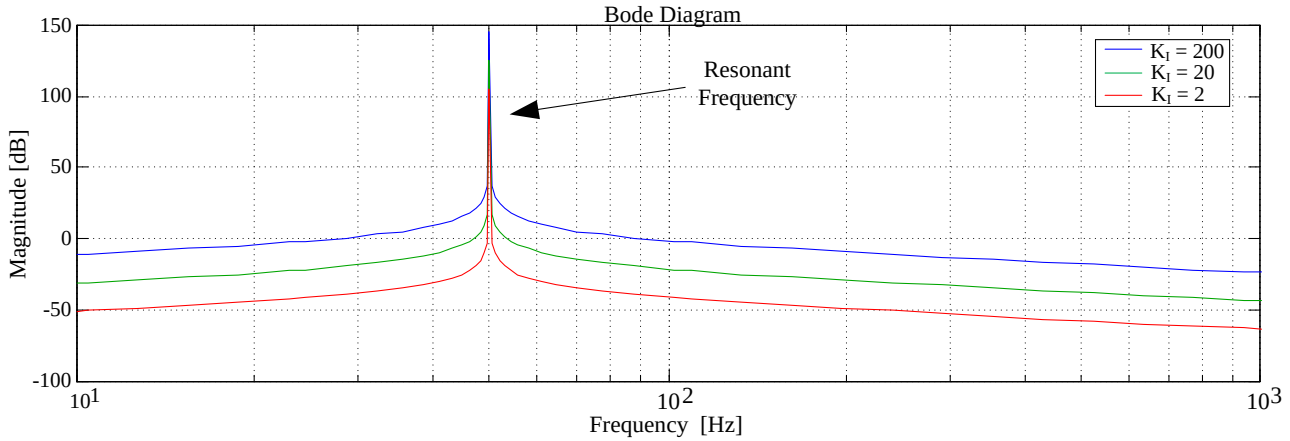

Figure 5-29: Bode Diagram of Resonant Controller

The consequence is that transitions such as step variations cannot be mitigated as successfully as signal at the resonant frequency. When looking at the output voltages of the controlled three-phase system in Figure 5-30, it can be seen that the P+Resonant controller is similarly capable of ensuring excellent reference tracking.

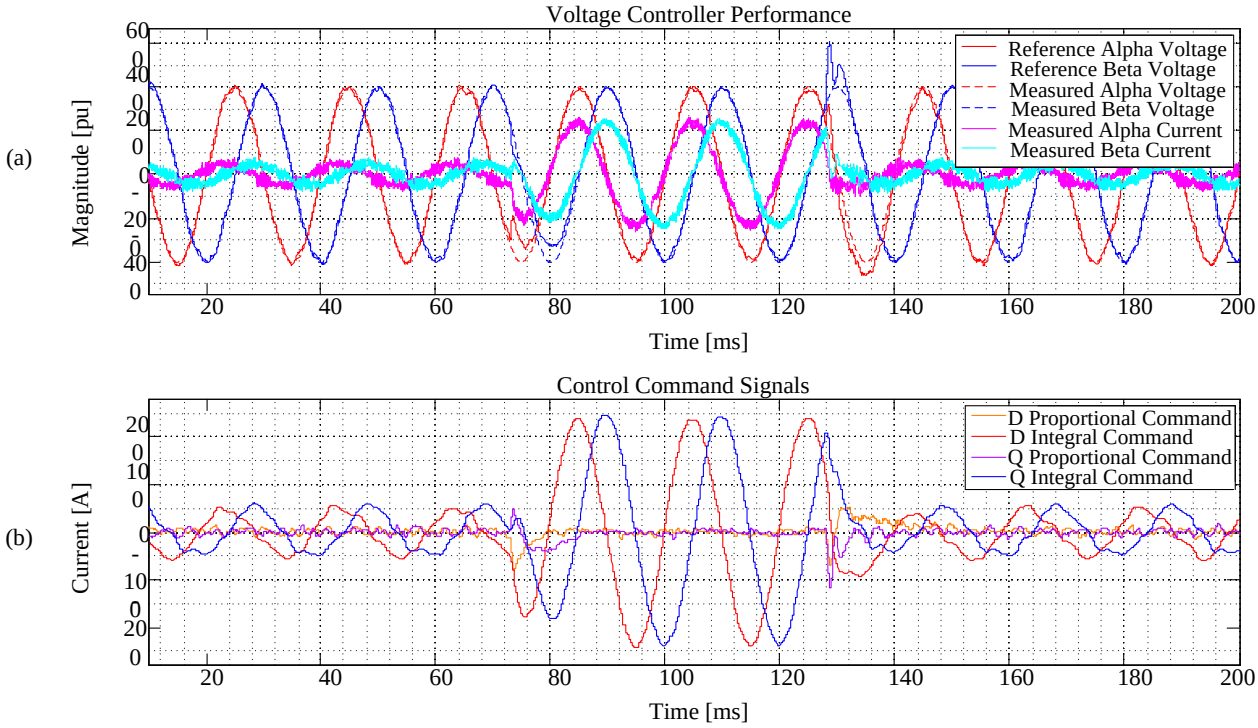

Figure 5-30: Simulated Performance of P+Resonant Controller

Former simulations of the previous controllers showed great deviation from the reference voltage under a load release condition. Figure 5-30(a) shows that there is still an overshoot on the output voltage but that it is more successfully mitigated by the P+Resonant controller.

The controller operates on the error signals of the alpha- and beta voltages. Therefore the proportional controllers are based in the stationary reference frame. The resonant controller however alleviates the control effort of these controllers by utilising the direct and inverse Park transforms. The result is that the integral

command remains a sinusoid that is similar to the alpha- and beta voltages but is capable of achieving zero tracking error thanks to the Park transform. Analysis of Figure 5-30(b) shows the proportional and resonant control command signals of respective alpha- and beta voltages. It can be seen that the P+Resonant controller provides a great reduction in unnecessary control noise. Unwanted control noise can result in the oscillation of the control system and even instability. In chapter 6 practical evidence of the advantages gained from reducing the control noise of a system will be provided.

In general however the P+Resonant controller provides a relatively good system response. It achieves the best performance of all the PI controllers considered in this project. The P+Resonant controller is thus cautiously recommended for the closed-loop control of the output voltage of a three-phase VSI. The caution is because of the still relatively large overshoot on the output voltage under a load release. In chapter 6 the measured result of the practically implemented system will be shown. There it will be seen that this overshoot is however still far within the tolerable RMS range according to the NRS-048 specification.

5.4.6 Predictive Voltage Controller

5.4.6.1 Principle of Operations

A predictive scheme for the control of the output voltage was proposed by Buso et al in [31] and [48]. A similar physical approach was taken to control the voltage of the output capacitor. The diagrammatical presentation of the multi-loop control scheme containing the predictive voltage controller is shown in Figure 5-31. The proposed voltage controller operates by predicting the change in the current of the output capacitor. When this is done, the current flow through the capacitor is controlled and in turn the voltage potential across the capacitor is similarly controlled. The current controller that is employed with this controller is the predictive current controller derived in section 5.3.3.

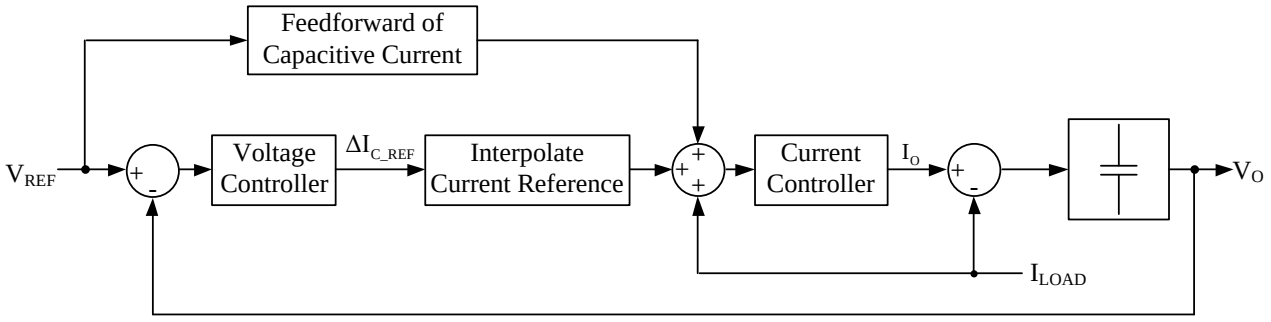

Figure 5-31: Predictive Voltage Controller

The predictive current controller is based on a two-cycle prediction to achieve satisfactory results. In other words, the controller requires two sampling periods to make the actual output current equal to the reference current which consequently means that the actual current always lags the reference current by two sampling cycles. It is very important to take note that the sampling rate at which the voltage controller operates can not

be equal to the sampling rate of the current controller. The dynamic delay imposed by the current controller undermines the system's stability. It is for this reason that the sampling rate of the voltage controller is set to half the sampling rate of the current controller. The effect of setting $T_{S\_V}=2T_S$ ensures that from the voltage controller's perspective, the delay caused by the current controller become insignificant [31].

Section 5.2 provided a means of modelling the output voltage with equation (5.9). Using equation (5.9) at the sampling rate that is half of the current controller, the output voltage can be described as:

$$v_O[h+1]=v_O[h]+\frac{T_{S\_V}}{C}\left[i_L[h]-i_{LOAD}[h]\right] \tag{5.33}$$

where h denotes the discrete domain in which the voltage controller operates. Advancing this equation by one sampling cycle:

$$v_O[h+2]=v_O[h+1]+\frac{T_{S\_V}}{C}\left[i_L[h+1]-i_{LOAD}[h+1]\right] \tag{5.34}$$

Substituting equation (5.33) into equation (5.34) and assuming that the output current changes slowly such that $I_{LOAD}[h+1]=I_{LOAD}[h]$, the deadbeat control equation of the voltage controller is obtained:

$$I_O^*[h+1]=-I_O^*[h]+\frac{C}{T_{S\_V}}\left(V_O^*[h+2]-V_O[h]\right)+2I_{LOAD}[h] \tag{5.35}$$

Using equation (5.35) will result in a voltage controller that is able to control the output voltage, but Figure 5-31 shows several refinements and improvements that can be made to ensure greater dynamic stiffness and robustness of the voltage controller.

Upon closer examination of Figure 5-31 it can be seen that the capacitor current is fed forward based on the reference voltage. The controller is implemented in the stationary reference frame which makes the feed forward of the capacitor current really simple. Since the voltage potential across a capacitor C lags the current through that capacitor by 90°, the capacitor current can be calculated as follows:

$$\begin{aligned} i_C^\alpha &= \frac{-V_C^\beta}{2\pi fC} \\ i_C^\beta &= \frac{V_C^\alpha}{2\pi fC} \end{aligned} \tag{5.36}$$

Once the capacitor current is fed forward and the output load current is measured, the only purpose that remains for the voltage controller is to compensate for errors made in the feed forward of the capacitor current and measurement of the load current. Considering that the capacitor current can be expressed in terms of the output inductor current and the output load current as $i_C=i_L-i_{LOAD}$ the deadbeat expression in equation (5.35) becomes:

$$\Delta I_C^*[h]=\frac{C}{T_{S\_V}}\left(V_O[h+2]-V_O[h]\right)-\Delta I_C^*[h-1] \tag{5.37}$$

The change in capacitor current in this equation is therefore used in combination with the fed forward capacitor current and the measured load current to update the current controller once every two switching periods. The current controller is approximated as a pure two cycle delay. Although this is an accurate approximation, the inherent assumption made during the approximation will result in the degradation of the voltage controller's performance. The consequence is that the voltage controller is not capable of achieving exactly a deadbeat response.

Operating the voltage controller at half the sampling rate of the current controller produces the fastest possible response from the voltage controller. A possible detrimental consequence of operating the voltage controller at half the rate is that - from the current controller's perspective - the change in the inductor current i_L^* required by the voltage controller is seen as a sequence of step reference variations [48]. A transient is initiated every time the current reference is updated. With the objective of smoothing the transition between reference updates, a simple linear interpolation of the current reference is implemented. The improvement of the current reference that is produced by the voltage controller is shown in Figure 5-32. It can be seen that high frequency oscillating components are removed when the voltage control output is interpolated.

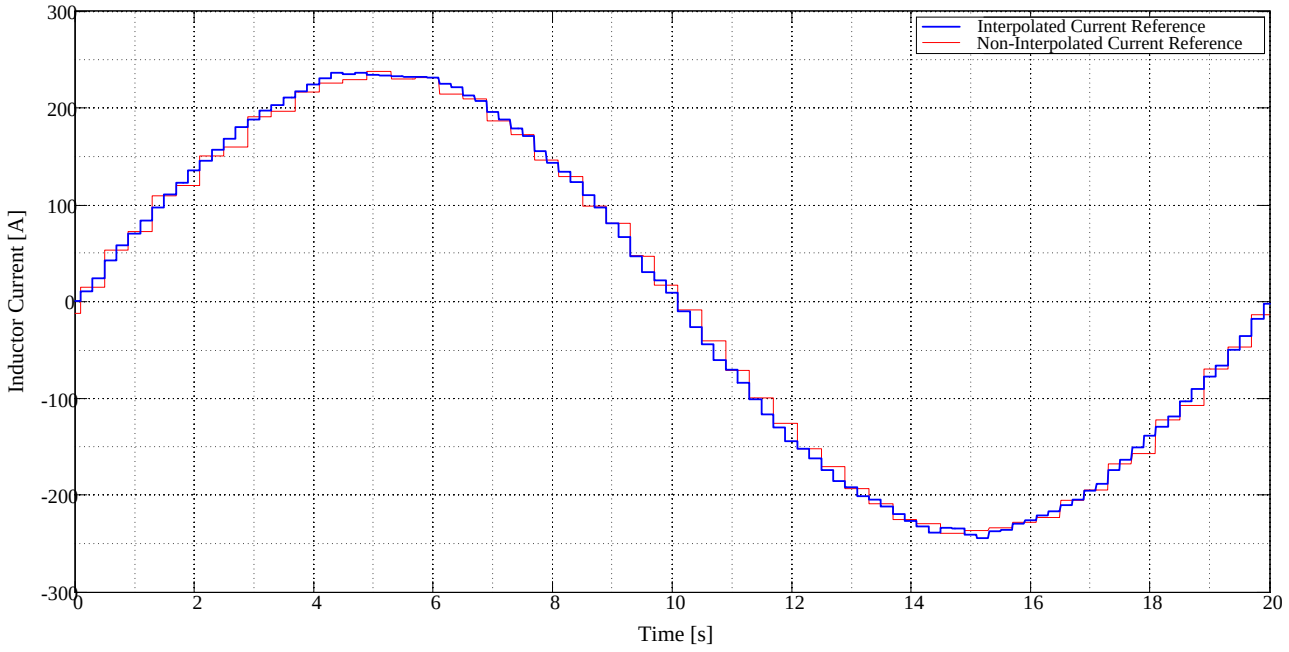

Figure 5-32: Current Reference Improvement by Interpolation

The interpolation is achieved by means of a simple interpolation method. Figure 5-33 shows the average inductor current over four switching cycles. It can be seen that since the voltage controller operates at half the rate of the current controller, the h index is only increased once every two switching periods.

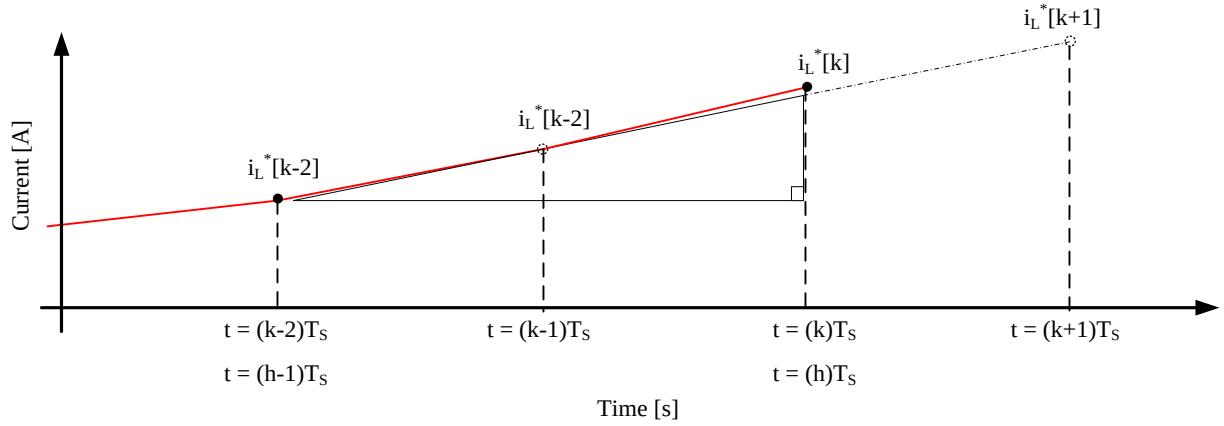

Figure 5-33: Simple Linear Interpolation Method

The voltage controller is unable to provide a current reference at $t = (k+1)T_S$ and it is therefore required to interpolate the current reference. At time $t = kT_S = hT_S$, the $\frac{dI_L(t)}{dt}$ is determined from the previous two switching periods. This rate of change is then used to determine the current at $t = (k+1)T_S$. Basically, the interpolation method is achieved by using equation (5.38):

$$i_L^*[k+1] = i_L^*[k] + \frac{i_L^*[h] - i_L^*[h-1]}{2T_S} T_S \tag{5.38}$$

By using interpolation to determine the odd reference commands, the change in capacitor current expressed in equation (5.37) becomes:

$$\Delta I_C^*[h] = \frac{2}{5}\frac{C}{T_S}\left(V_O[h+2] - V_O[h]\right) - \frac{4}{5}\Delta I_C^*[h-1] + \frac{1}{5}\Delta I_C^*[h-2] \tag{5.39}$$

Bester [44] points out that due to the lack of an integrator to provide a means of mitigating the steady-state errors, this controller is hugely dependent on the system parameters. Any deviations from the set parameters, such as the filter inductor and capacitor values, will directly impede the controller's performance. It therefore seems obvious that an integrator needs to be included in the control scheme to counteract these errors.

The voltage controller operates under the condition that the resonant frequency of the output filter is considerably lower than the switching frequency of the system. It is recommended in [48] to ensure that a ratio of ≈ 20 between the sampling frequency f_S and the resonance frequency $f_O = \frac{1}{2\pi\sqrt{LC}}$. Due to the IGBTs being incapable of high switching frequencies, a relatively low switching frequency of 5 kHz is used in the practical converter. This made it difficult to achieve the recommended ratio.

To ensure a ratio of approximately 20 between f_S and f_O it will be necessary either to increasing the inductance or the capacitance of the output filter. Increase of the inductance is not recommended since this will adversely affect the capabilities of the predictive current controller. Reduced steady-state tracking and

overall deterioration of controller performance will result if the inductance is overly increased. The only other option is therefore the increase of the capacitance. There is however also a corresponding disadvantage associated with this increase. To achieve the required ratio, the capacitance has to be drastically increased, directly resulting in an increase of continuous current drawn by the capacitors, since $i_C(t) = C\frac{dv_C(t)}{dt}$. This implies reduced UPS effectiveness, but more importantly, the large capacitance results in large in-rush currents during initialisation of the line-interactive UPS.

The inrush currents experienced during initialisation of the line-interactive UPS occurs when the DC-link is charged with the aim of matching the voltage with the storage battery voltage. The DC-link is initially passively charged by means of the anti-parallel diode of the individual IGBTs. The current drawn during this stage is limited by resistors connected in series with the converter. Under normal conditions, these resistors are thereafter short-circuited and the DC-link is further actively charged. When the capacitance is however drastically increased with the objective of meeting the required ratio requirement, large inrush currents are again experienced which can cause damage to the system. When the resistors are short-circuited, the voltage of the output filter capacitors is increased. When the capacitance is relatively low, this will not be a problem since a small amount of current will be drawn from the utility supply to bias the capacitors at this new voltage potential. On the other hand, when the capacitance is considerably larger, the amount of current required to bias the capacitors at the new voltage is greatly increased. The current becomes so large that it even results in extremely large $\frac{dV}{dt}$ signal and subsequently large EMI pulses which causes the system to trip.

It is conclusive that the increase of neither the inductance nor the capacitance is possible with the aim of meeting the required ratio between f_S and f_O. Failure to ensure a large enough ratio results in a distinguishable error in the magnitude of the output voltage. It has been successfully established that the predictive controller is prone to steady-state tracking errors, which can be resolved by the inclusion of an integrator that controls the magnitude of the output voltage.

5.4.6.2 Simulated Performance

The predictive controller is simulated in a three-phase VSI that is identical to the simulation model used in the previous controllers. The system's parameters are again exactly the same as given by Table 5-2.

The output alpha- and beta voltages are shown in Figure 5-34(a). When comparing these output voltages with the corresponding output voltages of the other controllers proposed in the previous sections, it can with great certainty be said that the controller delivers exceptionally better results. The controller is able to ensure good reference tracking under both steady-state and transient situations.

A large overshoot on the output voltage was observed in the previously proposed controllers –to a greater or lesser extent- under a load release condition. Although there is still an observable overshoot on the output voltage when a load is released, it is much better mitigated.

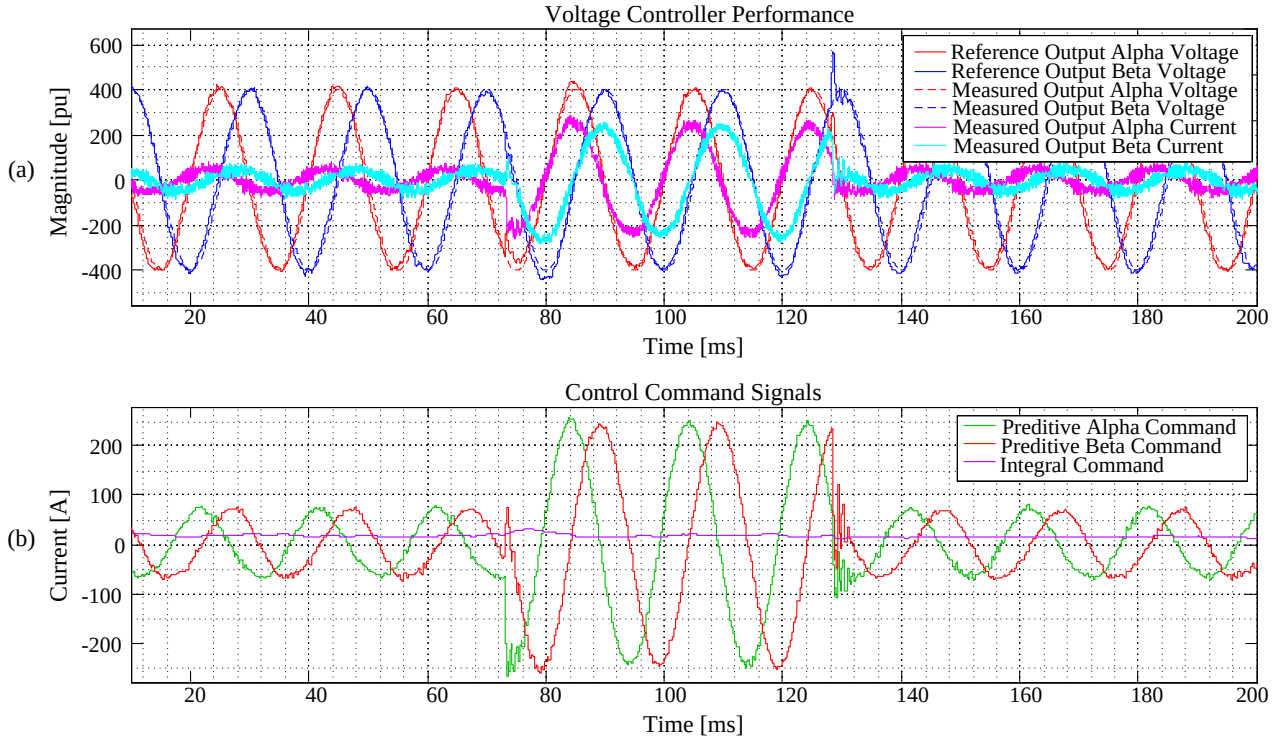

Figure 5-34: Simulated Performance of Predictive Voltage Controller

The predictive controller ensures that the overshoot peak is not as large as the other controllers and is even capable of mitigating the consequential oscillations in a much shorter time. It was observed that with the absence of an integrator in the voltage control system only resulted in an error being made with the magnitude of the output voltage. It was for this reason that an integrator was included for the control of the magnitude of the output voltage vector $\overrightarrow{V_{\alpha\beta}}$.

Figure 5-34(b) depicts the control commands that are produced by the voltage controller. It can be seen that the introduction of an integrator in parallel with the predictive controller produces a nearly constant command signal to correct the magnitude error. Yet, it is interesting to note that this integral command signal is small in comparison with the predictive alpha- and beta commands.

Finally, the predictive voltage controller proposed in this section performs very well to the control the output voltages produced by a VSI. It is capable of mitigating both steady-state and transient errors and ensures stability under harsh load conditions.

5.5 Conclusion

This chapter provided several control schemes for the regulation of both the inductor current and the output load voltage. An approach that is based on the average inductor current and the mathematically approximated magnitude of the inductor current ripple was developed. Simulation and analysis of this controller's capability pointed out the controller's poor performance.
A predictive control schemes was subsequently developed to regulate the inductor current. This control scheme proved to perform exceptional and proved to ensure good current regulation under large load variations. This current controller was subsequently utilised in the inner loop in a double-loop control scheme.

Several control schemes was also investigated for the regulation of the three-phase output voltage of the DC-AC converter. A base-case was established by investigating the capabilities of a simple open-loop controlled system. Thereafter, an elementary classic PI controller was developed. This controller provided an improvement upon the open-loop controlled system, but still performed poorly. An alternative approach to the classic PI controller provided a slight improvement.

A control schemes that is based in the DQ reference frame however provided a substantial improvement on the results provided of the above-mentioned controllers. Steady-state and transient tracking errors was greatly reduced. A P+Resonant controller was subsequently developed. This controller operates by suppressing all signals except the signals at the fundamental frequency of 50 Hz. Simulations showed that this controller produces very good tracking of the reference voltages and is therefore highly recommended for the control of the output voltages.

Finally, a predictive voltage regulation scheme was developed that is based on the physical operation of the DC-AC converter. The principle of operation and derivation of the controller was provided and simulations were done to gauge this controller's performance. Simulations showed that the predictive voltage controller is capable of very successfully mitigating many – if not all – transient and steady-state tracking errors.

CHAPTER 6

EXPERIMENTAL INVESTIGATION

6 EXPERIMENTAL INVESTIGATION

6.1 Introduction

The designed closed-loop control schemes were tested on a practical line-interactive UPS system. The objective was to gauge the controllers' capabilities against each other. Practical measurements of the system were also done when it was controlled by a completely open-loop controller. No current or voltage control scheme was implemented. The system that was used to conduct the practical evaluation of all the controllers is shown in Figure 6-1. It shows a single-line diagram of the line-interactive UPS system. The three-phase VSI received power from a battery with a nominal voltage of approximately 760 V under no-load conditions. The system was subjected to a load transition by applying a load step from a no-load condition.

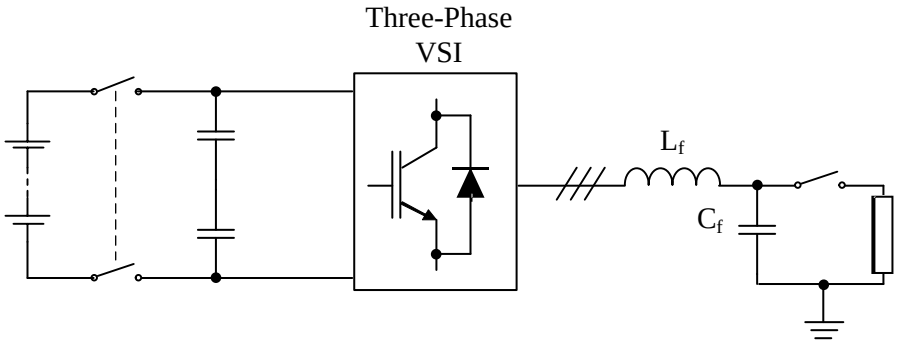

Figure 6-1: Practical Three-Phase VSI

The parameters of the system are described by Table 6-1:

Table 6-1: Practical System Parameters

System Parameters	
Filter Inductance L_f	400 μH
Filter Capacitance Cf	200 μF
Fundamental Output Frequency	50 Hz
Switching Frequency	5 kHz
Nominal DC Voltage	760 V

In this chapter an experimental investigation on the practical performance capabilities of the closed-loop voltage control schemes developed in chapter 6, will be described.

6.2 Open-Loop Controlled Experimental Investigation

The system was initially evaluated without implementing any digital closed-loop control schemes. Neither the output voltage nor the output current was controlled. The purpose of this investigation was to establish a base case for the gauging of the other closed-loop controllers. All the subsequent closed-loop controlled results will be compared with this open-loop performance. Since the focus is on the control of the output voltage, the base-case only provides the results of the output voltage when the system was subjected to an approximate 140 kW load step from a no-load condition. Figure 6-2 provides the measured output voltages of the system. The duration that the load is engaged, is also indicated.

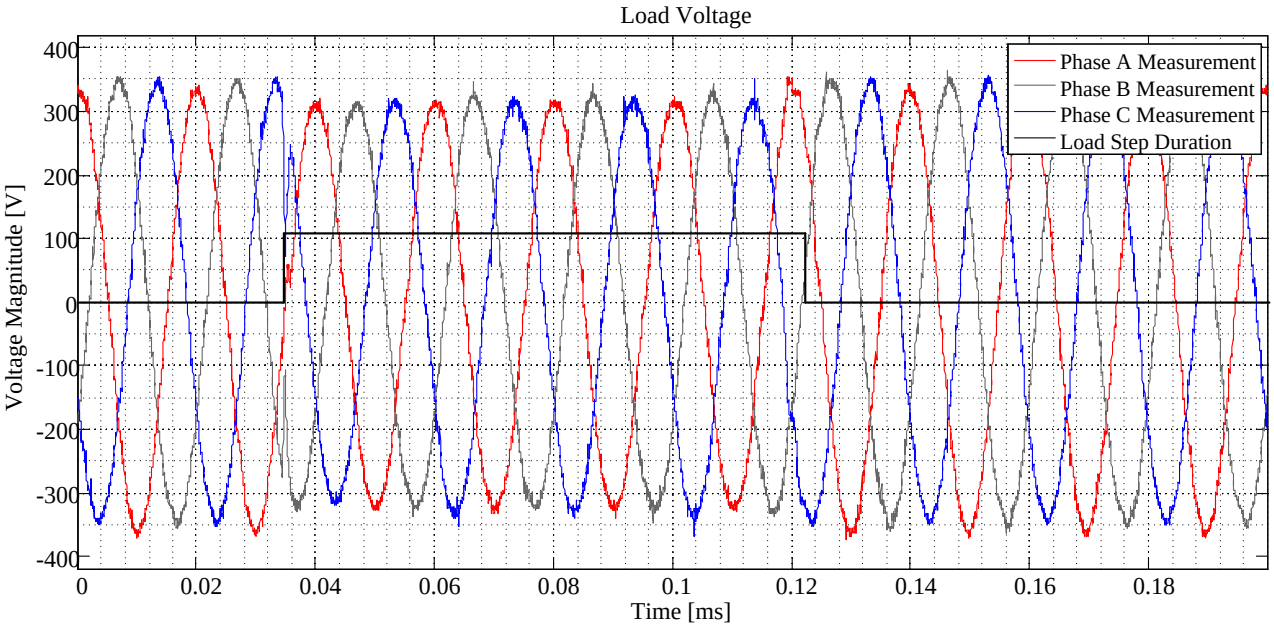

Figure 6-2: Open-Loop Output Voltage Measurement

It can be seen that the open-loop controller is not capable of maintaining a relatively unchanging voltage magnitude. The output voltage of each phase has a magnitude of 245 V_{RMS} when no load is applied. This amounts to a steady-state error of 6.5 %. When the load is engaged, the magnitude however drops to approximately 228 V_{RMS}. Although this voltage is more accurate, the large drop in voltage is still unacceptable, since the system is greatly influenced by the load.

Moreover, the open-loop controlled output does not contain any dead-time compensation scheme. The blanking-time included on a converter leg is 4.8 µs. To compensate for this voltage loss due to the blanking-time included between the top- and bottom IGBT of each converter leg, the magnitude of the actual reference applied to the VSI had to be increased. This is a rudimentary method of compensation but due to a lack of feedback in the open-loop control system, a more accurate compensation technique could not be implemented. Even when the effect of dead-time was compensated, the open-loop controlled output still had large steady state error and the above mentioned voltage drop.

The NRS048-2:2004 regulation on the quality of electricity supply stipulates that the RMS voltage of a LV network may not deviate more that 15 % from the nominal 230 V_{RMS}. The greatest error in the output voltage occurs when the load is not connected, but this is still within the acceptable performance stipulated by the NRS048 regulation.

The NRS048 regulation calculates the RMS voltages using a 20 ms window and sliding this window at 10 ms intervals [13]. The RMS voltage of the output voltages depicted in Figure 6-2 was consequently calculated and is shown in Figure 6-3.

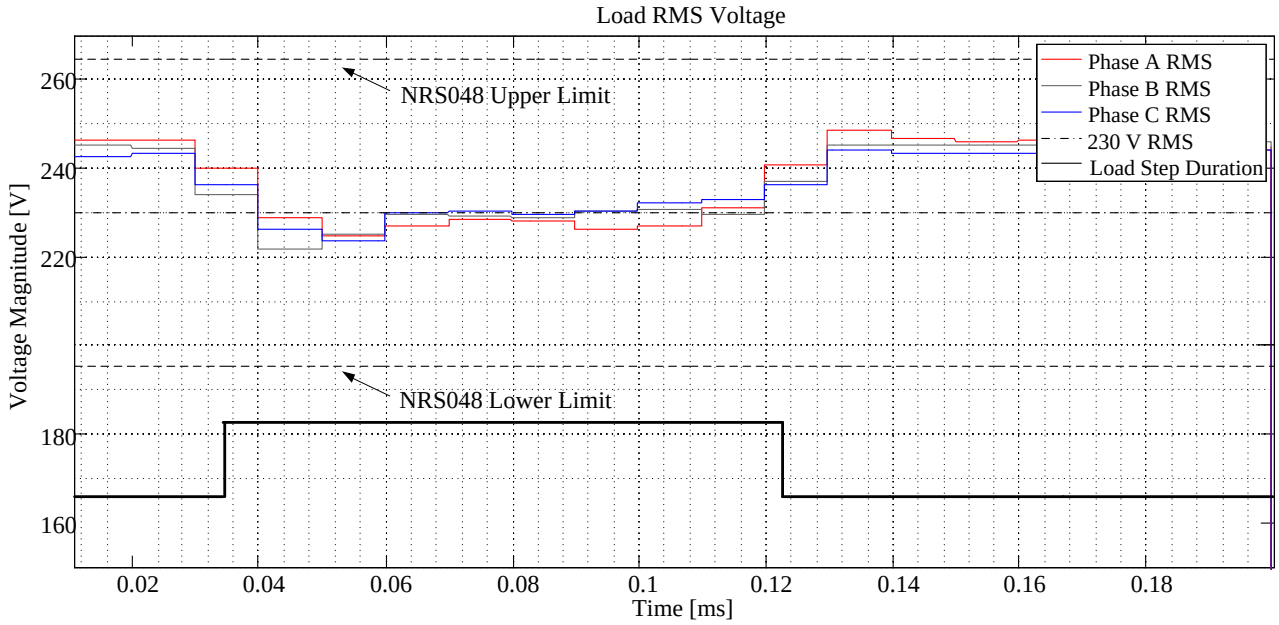

Figure 6-3: Open-Loop RMS Analysis

A quick analysis of the RMS result in this figure shows that the open-loop controller is incapable of accurate steady-state tracking, nor is it capable of quickly mitigating transient errors.

6.3 Evaluation of Classically Approached Alpha-Beta Voltage Control

The classically approached PI controller designed and discussed in section 5.4.1, was implemented in the system. The transient response of the system that is controlled by this closed-loop voltage controller is depicted in Figure 6-4. In section 5.4.2 the poor performance obtained when using this simple classical approach of the traditional PI controller, was discussed. As expected, the output voltage has a poor average steady-state tracking error of almost 7.4 %.

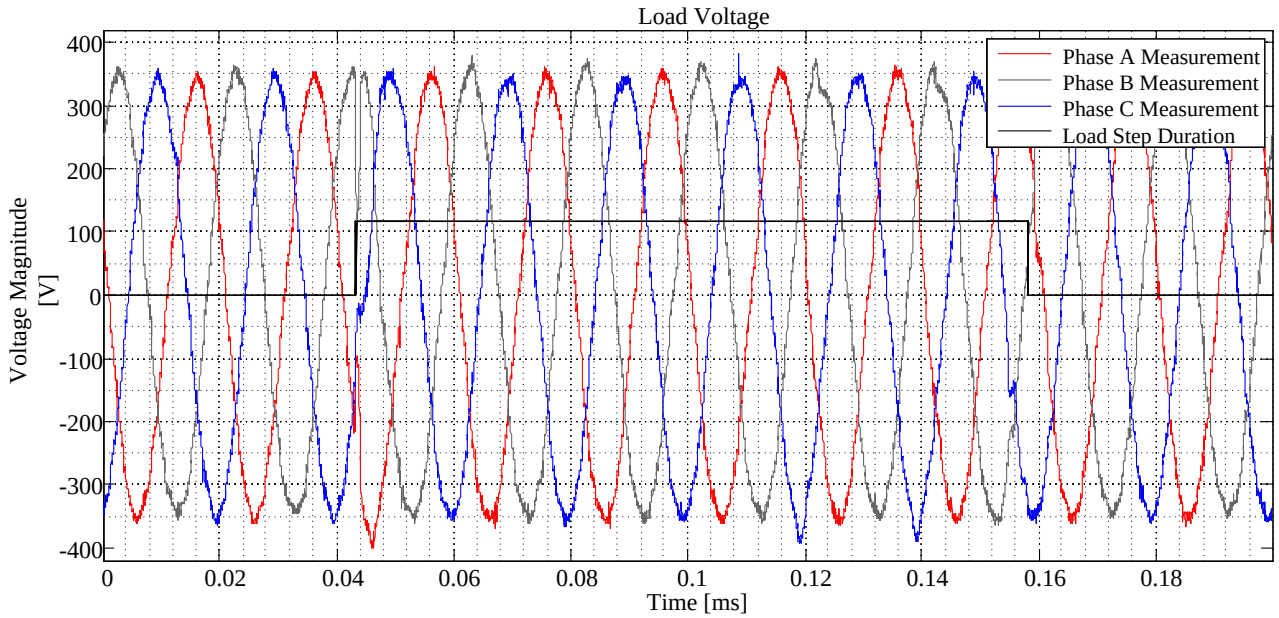

Figure 6-4: Classical PI Controlled Output Voltage Measurement

After analysing the measurements obtained in Figure 6-4 according to the assessment method set out by the NRS048 regulation, the RMS values of the voltages are calculated. These are as depicted in Figure 6-5.

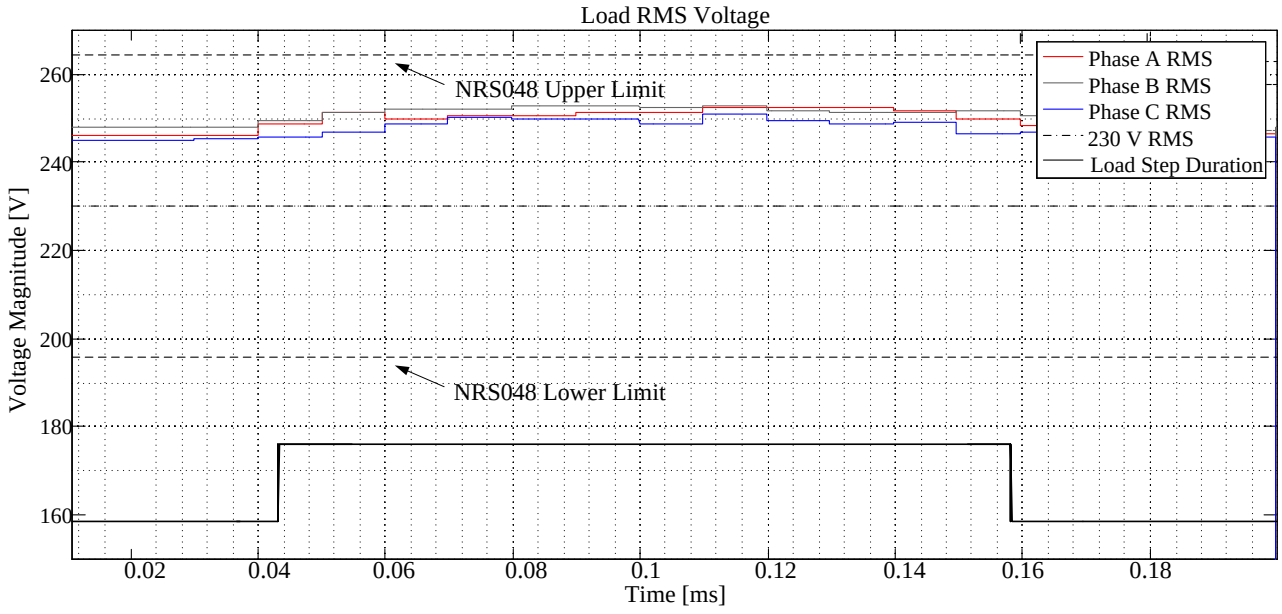

Figure 6-5: Classical PI Control RMS Analysis

The advantage provided by this closed-loop controller is that it is able to mitigate the transient errors on the output voltage more rapidly. There is also a smaller deviation in the voltage magnitude between load transitions in comparison with the open-loop controlled system. Apart from this, it can conclusively be said that the classic PI control of the output voltage provides insufficient performance.

6.4 Evaluating an Alternative Approach of Alpha-Beta Voltage Control

The output voltage measurements of the alternatively approached PI control scheme are shown in Figure 6-6. The integral control of solely the magnitude of the output voltage vector $\overrightarrow{\mathbf{V}_{\alpha\beta}}$ evidently produces output voltages that have both a relatively constant magnitude throughout the load step as well as a lower steady-state tracking error. The measured average output voltage magnitude is 234 V_{RMS} which amounts to a 1.7 % error.

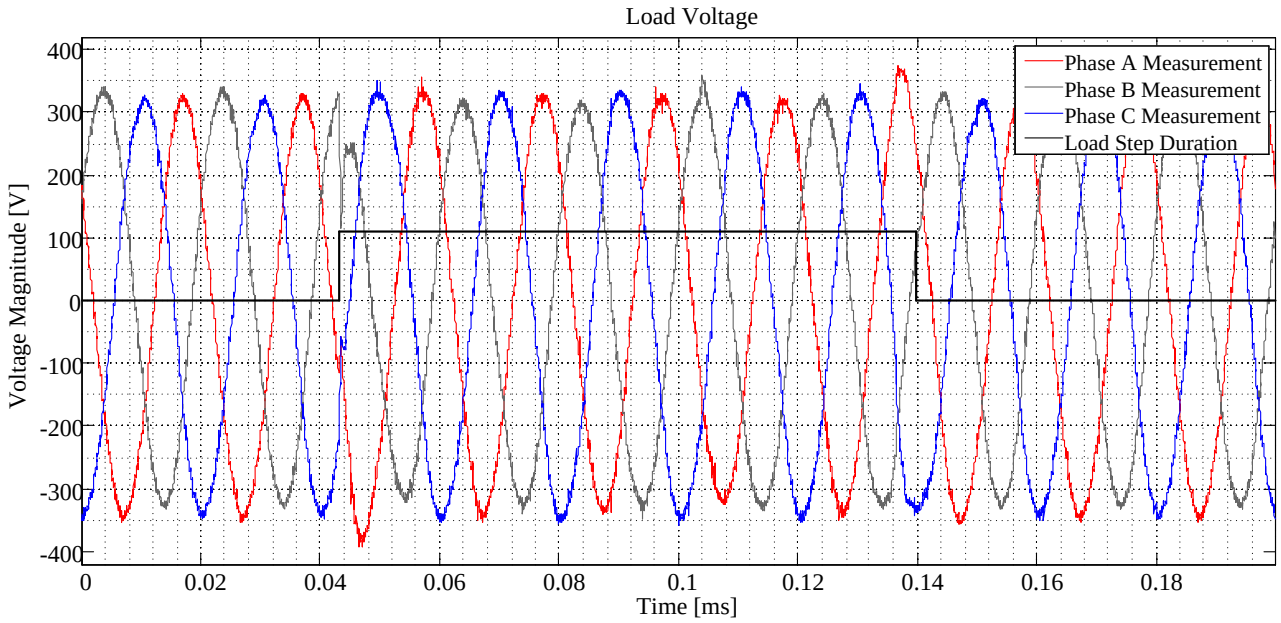

Figure 6-6: Classical PI Control Alternative Output Voltage Measurement

Examination of the RMS assessment shown in Figure 6-7 further shows that the voltage magnitude is kept within the allowable limit stipulated by NRS048-2:2004 regulation. Due to the low bandwidth of the implemented controller, the transient error upon the release of the load cannot be removed rapidly. The deviation is however still within allowable tolerances.

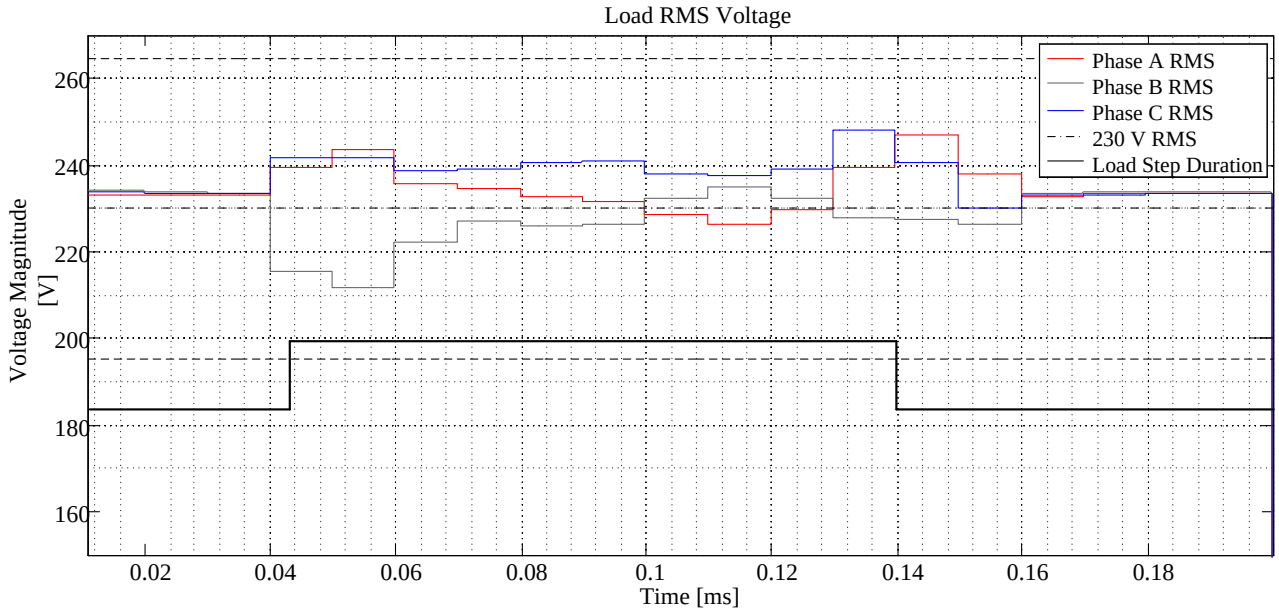

Figure 6-7: Classical PI Control Alternative RMS Analysis

Furthermore, the output voltages are once again unbalanced due to the poor performance of the controller which is based on classical control theory.

6.5 Evaluating the Voltage Controller Based in the DQ Reference Frame

The performance of the controller discussed in section 5.4.4 is shown in Figure 6-8. It depicts the output voltage of the VSI through a load step.

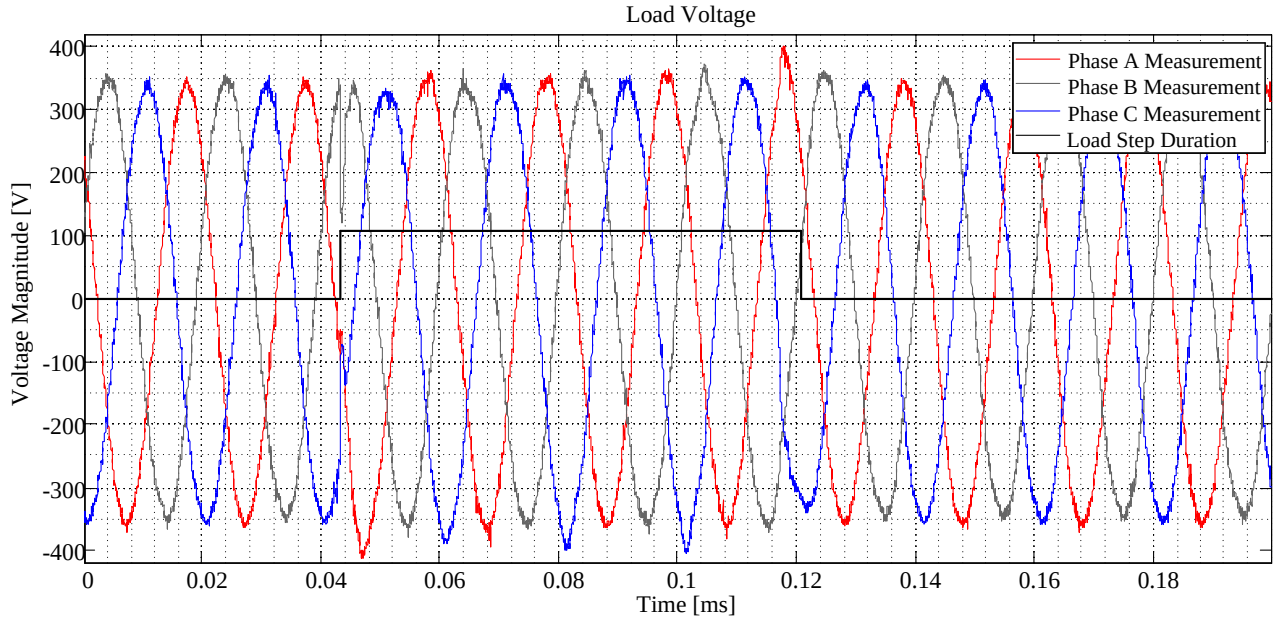

Figure 6-8: DQ Controlled Output Voltage Measurement

It is evident that this controller is more capable of controlling the output under varying load conditions. From Figure 6-9 it can be seen that the output voltage is 243 V_{RMS} which measures as a 5.7 % steady-state tracking error.

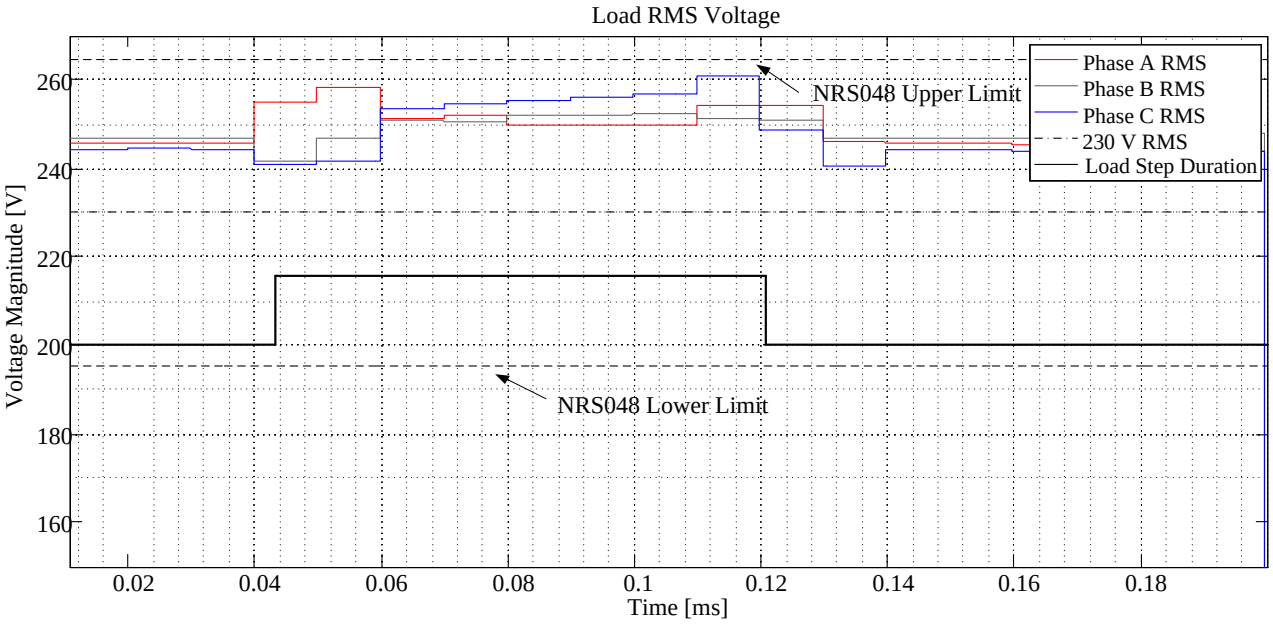

Figure 6-9: DQ Controlled RMS Analysis

When the load is engaged, the voltage deviates to approximately 252 V_{RMS} which implies a large error of 9.6 %. The DQ controller is however capable of ensuring balance between the phases and is more successful at regulating the voltage through a load step.

6.6 Evaluation of P+Resonant Voltage Control

The P+Resonant controller developed in section 5.4.5 provides significantly improved control of the output voltages. Figure 6-10 provides the measurement of the VSI output voltage when controlled by the P+Resonant controller. It can be seen that balance between the phases is maintained to within 1 V throughout the load step. The average output voltage magnitude amounts to 233 V_{RMS} which is equivalent to a 1.3 % steady-state error. The voltage magnitude stays unchanged throughout the load step.

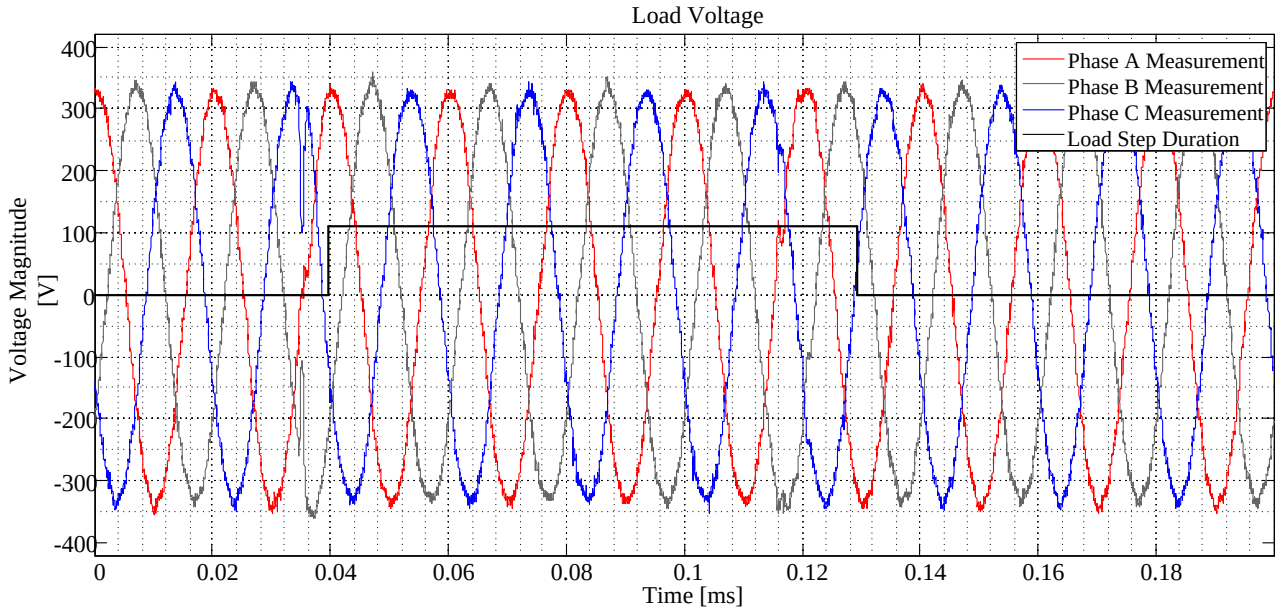

Figure 6-10: P+Resonant Controlled Output Voltage Measurement

RMS voltages are calculated according to NRS048-2:2004 regulation specifications and are depicted in Figure 6-11. A greatly improved mitigation of the transient error can be seen when compared with the results of the previous controllers.

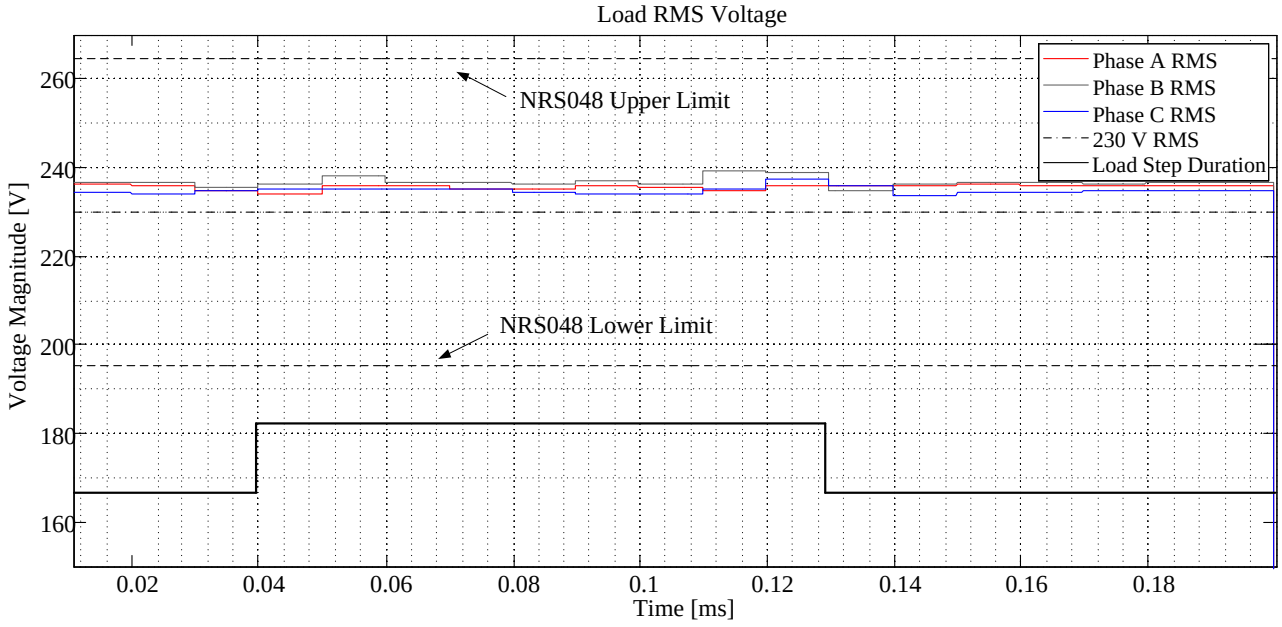

Figure 6-11: P+ Resonant Controlled RMS Analysis

It can conclusively be said that the P+Resonant controller performs exceptional under varying load condition and is very successful and accurately controlling the output voltage of the system. The P+Resonant controller is therefore highly recommended for the control of the output voltage.

6.7 Evaluating a Predictive Voltage Controller

The utilisation of a predictive controller has its advantages and disadvantages. The disadvantage is – as discussed in section 5.4.6 – that the controller is heavily dependent on the parameters of the system. Any deviations will directly influence the performance of the controller. This increased sensitivity also illuminates the controller's similar sensitivity to control noise.

Due to the predictive nature of the controller, any noise fed back to the controller will impede the performance capability of the controller. The advantage provided by the predictive controller however greatly outweighs the disadvantages. The controller is much more successful at controlling the output voltage under varying load conditions as is evident in Figure 6-12. The diagram shows the measurements of the output voltages.

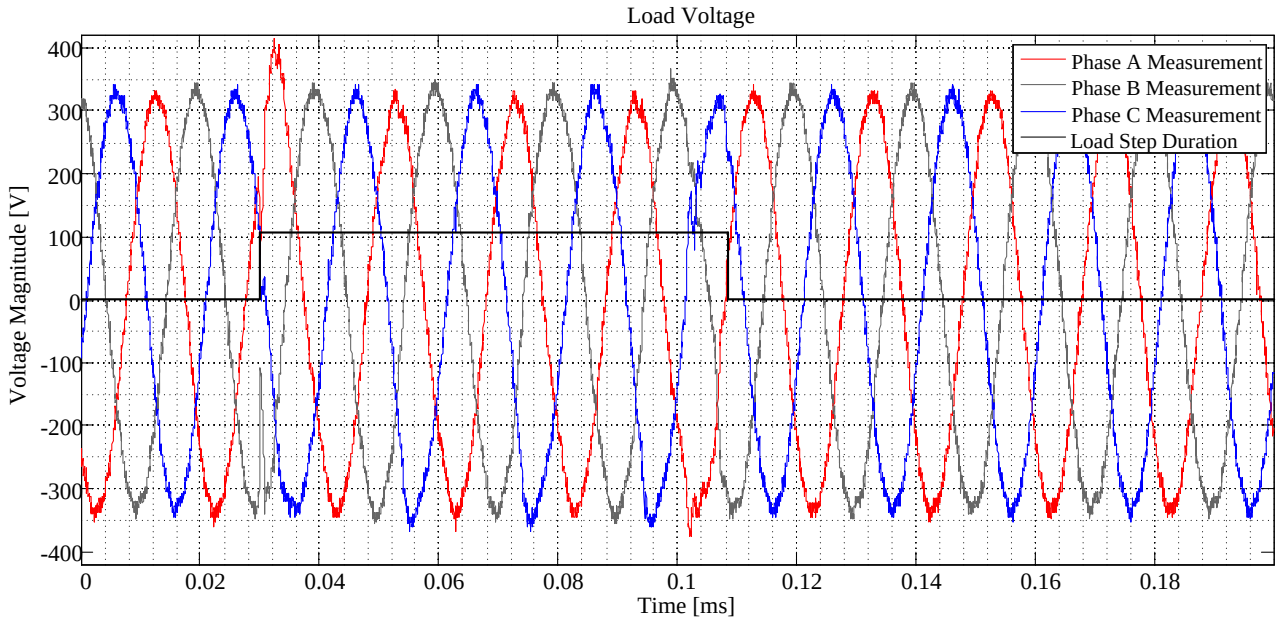

Figure 6-12: Predictive Controlled Output Voltage Measurement

The output voltage magnitude under no load conditions is measured at 233 V_{RMS} which amounts to a very low steady-state tracking error of 1.3 %. This is shown in the RMS assessment in Figure 6-13. When inspecting the performance results obtained by the open-loop controller, it can be seen that the steady-state output voltage varies by as much as 17 V when the load is engaged. The predictive controller is on the other hand capable of providing a smaller change in the steady-state RMS voltage on all the phases throughout the load step. This alone is already an improvement provided by the predictive controller. In Figure 6-13 the RMS voltage of the output voltages are analysed. It can be observed that the voltage does not deviate by a large degree when the load is engaged. A manner of concern is however the slight imbalance between the phases when the load is engaged. It has been previously mentioned that the predictive controller is very sensitive to changes in the system's parameters. The discrete components, such as the filter inductor and the output capacitor, of the practical system are slightly mismatched. These small mismatches does not have a

greatly impact on the performance of the controller in the case of mediocre load conditions. However, these mismatches are exaggerated when a very high power load is connected. The large amount of current drawn by the load exploits these small mismatches and the result is seen as the slight imbalance of the output voltage. The output voltage magnitudes are 228 V_{RMS}, 235 V_{RMS}, 240 V_{RMS} for phase A, B and C respectively which amounts to a 0.8 %, 2.2 % and 4.3 % steady-state errors for the respective phases.

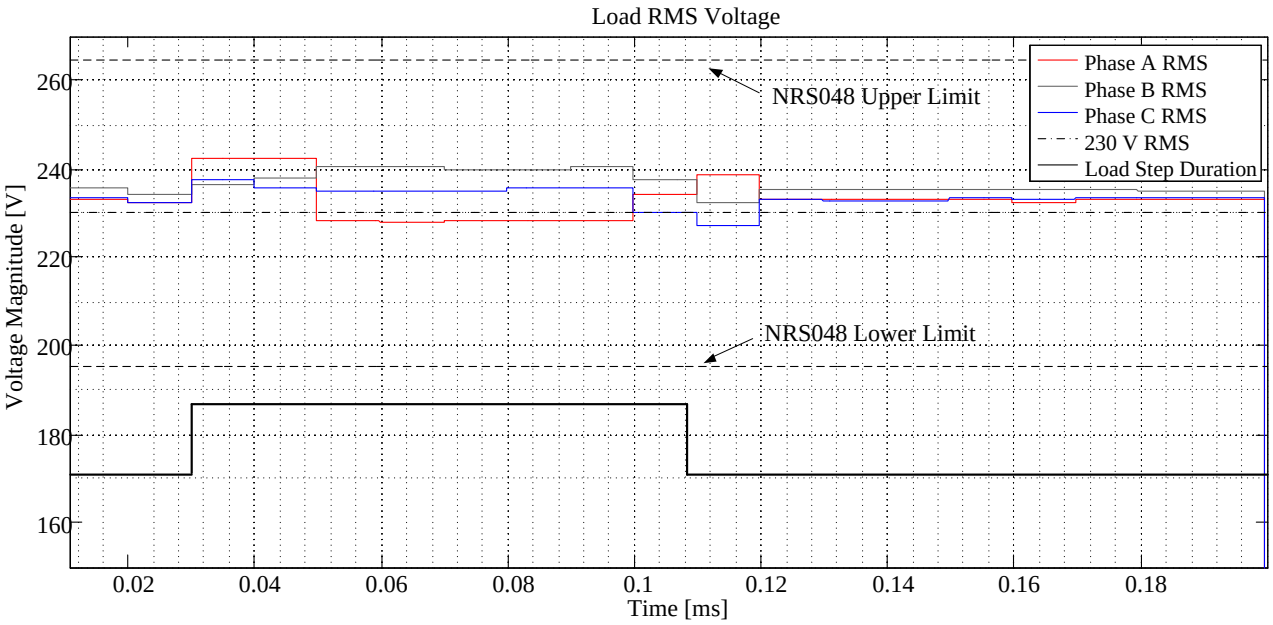

Figure 6-13: Predictive Controlled RMS Analysis

It was discussed in section 5.4.6 that an integrator is utilised in conjunction with the predictive controller. This is due to the predictive controller's incapability to mitigating steady-state errors. The integrator however controls the magnitude of the $\overrightarrow{\mathbf{V}_{\alpha\beta}^{*}}$ vector and is therefore incapable of removing the unbalance in the system. An unbalance control scheme is required to mitigate the unbalance in the system. The small imbalance in the output voltage is however still within acceptable NRS048 limit.

In section 5.4.6 the obvious advantages provided by the inclusion of capacitors on the output was discussed, but it can be observed that under a load release the controller still struggles to achieve good tracking of the output voltage. The relatively poor tracking is due to the large amount of energy stored in the filter inductor and output capacitor that now has no path along which it can be dissipated. Consequently, it is required that the control effort be drastically increased to remove this energy.

In summary however the predictive controller provides good performance and control of the output voltage. Good performance is still ensured even under varying load conditions.

6.8 Conclusion

This chapter provided an experimental investigation of the controllers' developed in Chapter 5. These voltage control schemes were implemented in a practical line-interactive UPS system with the measured results shown in this chapter.

It was seen that the open-loop controller is incapable of mitigating neither steady-state nor transient errors on the output voltages. The most elementary closed-loop voltage controller was a simple PI controller and it was seen that this controller did not provide a significant improvement in comparison with the open-loop controller. In fact, the classically approached PI controller has a steady-state tracking error of 7.4 %, which is more than the 6.5 % error achieved by the open-loop controller. Apart from providing a lower steady-state error than the open-loop controller, the simple PI controller performed rather poorly.

An alternatively approached PI controller however did provide a good result and ensured good reference tracking of the output voltages. It was capable of ensuring a better steady-state performance which had an error of 1.7 %. A controller based in the DQ reference frame was also evaluated and performed more poor than the performance provided by the open-loop controller. It was capable of ensuring a change in steady-state voltage that was less than the open-loop controller when a load variation occurred. The DQ-based controller however performed poorly under steady-state condition by providing a 9.6 % steady-state error.

The P+Resonant controller however greatly improved upon these poor results by producing a low steady-state error of only 1.3 %. This low tracking error was maintained indefinitely. Large changes in the load conditions did not adversely affect the controller's performance.

A predictive controller was also developed and produced a steady-state error of 1.3 % under no-load conditions but the output voltages became unbalanced under high-load conditions. This resulted in the tracking error to also slightly increase. The worst-case tracking error was 4.3 % under full-load conditions.

Table 6-2 summarises the performances of all controllers considered in this study. It shows the steady-state RMS voltages of each respective controller while it operated under no-load and high-load conditions. Additionally, the percentage tracking error of each measurement is also given to aid in the evaluation of the controllers' performance.

Table 6-2: RMS Voltage and Tracking Error of Controllers under No-Load and High-Load Conditions

	No-Load			High-Load		
	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
Open-Loop Controller	247 V	246	244	228	229	230
	7.40%	6.90%	6.10%	0.90%	0.40%	0%
Classical PI Controller	248	247	245	252	253	251
	7.80%	7.40%	6.50%	9.60%	10%	9.10%
Alternative PI Controller	233	224	224	232	226	238
	1.30%	2.60%	2.60%	0.90%	1.70%	3.50%
DQ Controller	246	247	245	250	253	256
	6.90%	7.40%	6.50%	8.70%	10%	11.30%
P+Resonant Controller	236	236	234	235	236	234
	2.60%	2.60%	1.70%	2.20%	2.60%	1.70%
Predictive Controller	233	236	234	228	235	240
	1.30%	2.60%	1.70%	0.90%	2.20%	4.30%

Considering the result in sections 6.6 and 6.7 as well as the summary in Table 6-2, it can conclusively be said that the P+Resonant controller performed better than the predictive controller. The steady-state tracking error of the P+Resonant controller remained unchanged under large load changes whereas the predictive controller produced output voltage that became unbalanced under high-load conditions.

CHAPTER 7

CONCLUSIONS AND RECOMMENDATIONS

7 CONCLUSIONS AND RECOMMENDATIONS

7.1 General Investigation

A general investigation was done on the predominant UPS topologies that are used in the industry. According to the international IEC 62040-3 regulation, the UPS topologies were defined as being either passive-standby, double-conversion of line-interactive. Among the three UPS topologies, the line-interactive UPS topology proved to provide several advantages without either overcomplicating or increasing the cost of the UPS.

A digital control system was developed in order to effective regulate both the UPS system's voltages and current and thereby ensuring the mitigation of the steady-state tracking error. To establish closed-loop control of the system it was necessary to acquire the system's voltages and currents. Several measurement solutions were analysed with the aim of obtaining a means of providing very accurate system telemetry to the digital controller. An in-depth study was also conducted on the operation of the ADC as well as various ADC popular architectures.

A study of literature was also done on the different pulsewidth modulation techniques. The advantages and disadvantages of each was discussed and an appropriate modulation scheme was selected that would ensure the best result.

Several techniques were investigated which either simplified or improved the operation of a three-phase converter. The Clarke and Park transformation methods proved advantageous in the operation of a three-phase converter. The Clarke transform in particular provided the means of increasing the dynamic range of operation of the three-phase converter. These methods provided the foundation for the development of several of the closed-loop controllers developed in the subsequent chapters.

7.2 Dead-Time Compensation

A study was done on the effect dead-time has on the output voltage of a switching converter in chapter 3. It was shown how dead-time could greatly degrade the quality of the voltage produced by the converter. With the objective of mitigation this degradation, an average-based and pulse-based dead-time compensation technique was developed.

The pulse-based technique was obtained by a study of literature where two modes of operation were identified. A third mode of operation was however identified and the compensation technique was augmented to include this new mode of operation. The average-based technique was also obtained from literature where a linear slope at the zero-crossing region of the converter's output current was proposed.

Both these techniques were implemented and simulation as well as a practical evaluation proved that these compensation methods are extremely effective and greatly improved the tracking capability of the subsequently developed closed-loop controllers.

7.3 DC-Link Regulation

To achieve effective control of the DC-link voltage of the switching converter, a multi-loop control strategy was employed and developed in chapter 4. A study of literature provided a simple means of controlling the inductor current of the converter by using a single-cycle prediction of the reference output current. Practical evaluation of this control scheme showed that it is very effective at regulating the output inductor current. This current controller completed the inner-loop of the double-loop control. The achieve regulation of the DC-link voltage, a voltage controller was employed for the outer-loop. A simple PI controller was developed and proved to achieve very accurate control of the DC-link voltage. It is worthwhile to mention that the dead-time compensation techniques aided in the mitigation of the steady-state tracking error of the DC-link regulator.

7.4 Control of VSI Output Voltage

In chapter 5 an extensive study was done in both the control of the output inductor current as well as the control of the output voltage produced by the three-phase VSI. Two predictive control schemes for the regulation of the inductor current were studied. The first technique was obtained from literature where a single-cycle prediction was done. This prediction was based on the previously measured average inductor current. This inductor current measurement was subsequently used in conjunction with the inductor ripple current to calculate the current reference for the next switching cycle. Simulations showed however that this control has insufficient steady-state tracking capability. This is – in part – caused by the fact that the ripple current used in the calculation of the predicted reference is solely based on theoretical calculations. A few assumptions were furthermore also made to provide a control law that can be practically implemented. These assumptions were used in the calculation of the ripple current contributed to the steady-state tracking error of the controller.

Buso provided a very effective means of controlling the inductor current. This current controller is also a predictive-based controller, but a two-cycle prediction is done. The control law was derived by considering the physical operation of the switching converter. Simulations showed that the current controller was very effective at ensuring very good tracking of the reference current under huge load variations. This predictive current controller was subsequently used in a double-loop control strategy for the control of the output voltage of the VSI.

Initially, a few simple PI controllers were developed to regulate the output voltage of the three-phase VSI. These controllers however proved to be very sensitive to changes in the load conditions. This was unacceptable since the controller must be capable of ensure a high quality output voltage under a wide

spectrum of load conditions. Thereafter, the rotational reference frame provided by the Park transform was further investigated. A controller was developed that was based in this rotational reference frame and proved to be highly effective at ensuring a stable unchanging output voltage. Based on the success of this controller, a resonant controller was develop that has the same characteristics are a narrow band-pass filter. The fundamental frequency of 50 Hz was selected as the pass-band of the "filter". The controller was implemented in a practical system and evaluations provided the best results obtained from all the developed controllers.

A predictive voltage controller was also developed. This controller regulated the current of the output capacitors. If the capacitor current could be controlled, it would effectively ensure good regulation of the corresponding output capacitor voltage. The predictive controller employed a two-cycle prediction to mitigate the tracking error on the output voltage. Simulations showed that this controller provided very good regulation of the output voltage under very large load variations. Upon practical evaluation however the controller's performance did not measure up to the expectations set by the simulation results. Further investigation showed that the predictive controller is very sensitive to the system parameters. Any deviation of the physical system's discrete components from the model used in the derivation of the controller directly affected the controller's performance. The deviations had a miniscule effect on the output voltage under low load conditions. If a large load was however connected to the system, the output voltage was slightly affected. The large amount of current drawn from the converter exaggerated the effect of any small deviations. The result was a slight imbalance of the three-phase output voltage.

In conclusion, it was established that the resonant controller provided the best possible result in the output voltage produced by the three-phase VSI. It ensured that the output voltage remained unchanged throughout a very large load step. A steady-state tracking error of only 1 % was made. This low tracking error was maintained throughout a large regime of load variations. The predictive controller also provided satisfactory results but its sensitivity to changes in the system parameters resulted in output voltages that were inferior to the quality produced by the resonant controller.

7.5 Recommendations

All targets in this project were achieved and satisfactory results obtained. It was observed that the predictive control approach promises great potential. It is for this reason recommended to further investigate voltage regulation with predictive controllers. The study also illuminated the sensitivity predictive controllers have to slight imbalances of the system's discrete components. It is thus recommended to also investigate unbalance compensation techniques.

8 BIBLIOGRAPY

[1] H. Mohan, T. Undeland, and W. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd ed. 2003.

[2] W. Sölter, "A New International UPS Classification by IEC 62040-3," in *Telecommunications Energy Conference*, 2002, pp. 541-545.

[3] R. Fourie, "The Development of a IGBT-Based Tap Changer," Master's Thesis, Stellenbosch University, Stellenbosch, 2009.

[4] J. Serdyn, "Electronic Voltage Regulation Technology for Rural Electrification," Master's Thesis, Stellenbosch University, Stellenbosch, 2008.

[5] J. Brooks, "Solid State Transformer Concept Development," Naval Construction Battalion Center, 1979.

[6] J. Van der Merwe, "The Solid-State Transformer Concept: A New Era in Power Distribution," in *IEEE AFRICON*, 2009.

[7] ESKOM Enterprises. www.eskom.co.za.

[8] IEC 61000-4, "Electromagnetic compatibility (EMC)".

[9] IEC 62040-3, "Method of Specifying the Performance and test Requirements".

[10] S. Karve, "Three of a Kind [UPS Topologies, IEC Standard]," *IEE Review*, vol. 46, no. 2, pp. 27-31, Mar. 2000.

[11] J. Samstad and M. Hoff, "Technical Comparison of On-Line vs. Line-Interactive UPS Designs," APC White Paper, 2004.

[12] N. Rasmussen, "The Different Types of UPS Systems," APC White Paper, 2003.

[13] NRS 048-2:2004, "Voltage Characteristics, Compatibility Levels, Limits and Assessment Methods," 2004.

[14] Maxim Integrated Products. (2002, Jun.) Understanding Single-Ended, Pseudo-Differential and Fully-Differential ADC Inputs. Application Note AN1108.

[15] W. Kester. MT - 020: ADC Architecture I: The Flash Converter. Electronic Document. [Online]. http://www.analog.com/static/imported-files/tutorials/MT-020.pdf

[16] Maxim Integrated Products. (2010, Sep.) Understanding Flash ADCs. Application Note AN810.

[17] Maxim Integrated Products. (2000, Mar.) Pipeline ADCs Come of Age. Application Note.

[18] W. Kester. MT- 024: ADC Architecture V: Pipelined Subranging ADCs. Electronic Document. [Online]. http://www.analog.com/static/imported-files/tutorials/MT-024.pdf

[19] Maxim Integrated Products. (2001, Mar.) Understanding Pipelined ADCs. Application Note AN1023.

[Online]. http://pdfserv.maxim-ic.com/en/an/AN1023.pdf

[20] Maxim Integrated Products. (2001, Mar.) Understanding SAR ADCs. Application Note AN1080. [Online]. http://pdfserv.maxim-ic.com/en/an/AN1080.pdf

[21] T. Kugelstadt. (2000, Feb.) The Operation of the SAR ADC Based on Charge Redistribution. Application Journal.

[22] W. Kester. MT - 021: ADC Architecture II: SAR ADCs. Electronic Document. [Online]. http://www.analog.com/static/imported-files/tutorials/MT-021.pdf

[23] H. S. Black, *Modulation Theory*. D. van Nostrand Company, 1953.

[24] H. W. van der Broeck, H. C. Skudelny, and G. V. Stanke, "Analysis and Realization of a Pulsewidth Modulator Based on Voltage Space Vectors," in *IEEE Transaction on Industry Applications*, 1988, pp. 142-150.

[25] F. Koeslag, "A Detailed Analysis of the Imperfections of Pulsewidth Modulated Waveforms on the Output Stage of a Class D Audio Amplifier," PhD Thesis, Stellenbosch University, Stellenbosch, 2009.

[26] J. G. Proakis and D. G. Manolakis, *Digital Signal Processing: Principles, Algorithms, and Applications*, 4th ed. Prentice Hall.

[27] H. Haus and J. Melcher, *Electromagnetic Field and Energy*. Prentice-Hall Incorparated, 1989.

[28] Analog Devices. (2006) AD7266 Dual 2 MSPS 12-Bit SAR ADC. Datasheet.

[29] Texas Instruments. (2002, Nov.) UCC27424 Dual 4 A High-Speed Low-Side MOSFET Driver. Datasheet.

[30] ON Semiconductor. (2000, Nov.) MTP27N10E 27 A, 100 V Power MOSFET. Datasheet.

[31] S. Buso and P. Mattavelli, *Digital Control in Power Electronics*, J. Hudgins, Ed. Morgan & Claypool Publishers, 2006.

[32] P. Horowitz and W. Hill, *The Art of Electronics*, 7th ed. Cambridge University Press, 2005.

[33] J. A. du Toit, "Development and Analysis of a Distrbuted Control Strategy for Power Electronic Converters," PhD Thesis, Stellenbosch University, 2002.

[34] D. E. Destefan, "AC and DC Shunts - Can You Believe Their Specs?," in *Instrumentation and Measurement Technology Conference (IMTC)*, 2003, pp. 1577-1582.

[35] D. W. Ackermann, "Current Transformer Measurements and Distorted Current Waveforms with Secondary Load Impedance," in *AFRICON*, 1999, pp. 765-768.

[36] LEM. LA 305-S/SP1 Current Transducer. Datasheet.

[37] J. Pankau, D. Leggate, D. W. Schlegel, R. J. Kerkman, and G. L. Skibiniski, "High-Frequency Modeling of Current Sensors," *IEEE Transaction on Industry Application*, vol. 35, no. 6, pp. 1374-1382, Nov. 1999.

[38] M. G. Ryan, R. D. Lorenz, and R. W. De Doncker, "Modeling of Multileg Sine-Wave Inverters: A

Geometric Approach," *IEEE Transactions on Industrial Electronics*, vol. 46, no. 6, pp. 1183-1191, Dec. 1999.

[39] D. G. Zill and M. R. Cullen, *Advanced Engineering Mathematics*, 2nd ed. Jones and Bartlett Publishers, 2000.

[40] W. S. Oh, Y. T. Kim, and H. J. Kim, "Dead Time Compensation of Current-Controlled Inverter Using Space Vector Modulation Method," in *International Power Electronics and Drive Systems Conference*, 1995, pp. 347-378.

[41] L. De Wit, "Flicker Mitigation in Industrial Systems," Masters Thesis, Stellenbosch University, Stellenbosch, 2006.

[42] F. M. Welgemoed, "Shunt Reactive Compensation of Voltage Dips and Unbalance," Masters Thesis, Stellenbosch University, Stellenbosch, 2010.

[43] I. K. Hobbs, H. J. Beukes, and F. Koeslag, "Analytical Characterization of Dead Time in the Zero-Crossing Region of the Inductor Current," in *AFRICON '09*, 2009, pp. 1-7.

[44] D. D. Bester, "Control of Series Compensator for Power Quality Compensator," Maste's Thesis, Stellenbosch University, Stellenbosch, 1999.

[45] M. Wolf, W. van der Merwe, and H. Mouton, "A Low Computational Double-Loop Control Strategy for DC-AC Inverter," in *South African Universities Power Engineering Conference (SAUPEC)*, Stellenbosch, 2009.

[46] J. D. Glover and M. S. Sarma, *Power Systems: Analysis and Desing*, 3rd ed. Brooks/Cole.

[47] G. Franklin, N.-E. Abbas, and A. Emami-Naeini, *Feedback Control of Dynamic Systems*. Prentice Hall, 2002.

[48] S. Buso, S. Fasolo, and P. Mattavelli, "Uninterruptible Power Supply Multiloop Control Employing Digital Predictive Voltage and Current Regulators," *IEEE Transactions on Industry Applications*, vol. 37, no. 6, pp. 1846-1854, Nov. 2001.

[49] J. Chen, A. Prodić, R. W. Erickson, and D. Maksimović, "Predictive Digital Current Programmed Control," *IEEE Transaction on Power Electronics*, vol. 18, no. 1, pp. 411-419, Jan. 2003.

[50] D. N. Zmood and D. G. Holmes, "Stationary Frame Current Regulation of PWM Inverters with Zero Steady-State Error," *IEEE Transactions on Power Electronics*, vol. 18, no. 3, pp. 814-822, May 2003.

[51] R. Carnieletto, D. B. Ramos, M. G. Simoes, and F. A. Farret, "Simulation and Analysis of DQ Frame and P+ Resonant Controls for Voltage Source Inverter to Distributed Generation," in *Power Electronics Conference COBEP ;09*, 2009, pp. 104-109.

[52] IEEE 1547-2003, "IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems," 2003.

[53] IEEE 519-1992, "Harmonic Limits," 1992.

[54] IEC 519-1992, "IEEE Recommended Practices and Requirements for Harmonic Control in Electrical

Power Systems," 1992.

[55] Burr-Brown. (2000) Principles of Data Acquisition and Conversion. Application Note.

[56] R. Silva-Ortigoza and H. Sira-Ramírez, *Control Design Tecnhiques in Power Electronics Devices*. Mexico City, Mexico: Springer, 2006.

[57] M. Gopal, *Digital Control and Sate Variable Methods*, 2nd ed. McGraw-Hill, 2003.

[58] M. Gopal, *Control Systems: Principles and Design*, 2nd ed. McGrawHill, 2002.

[59] M. J. Ryan, R. D. Lorenz, and R. W. De Doncker, "Modeling of Multileg Sine-Wave Inverters," *IEEE Transaction on Industrial Electronics*, vol. 46, no. 6, pp. 1183-1191, 1999.

[60] H. d. T. Mouton, *Electronics 414 Notes*. Stellenbosch University.

Appendix A Mathematical Derivations

A.1 Voltage Measurements

The measurement circuit that has been utilised in the system has been analysed and its transfer function derived. The nodal analysis method has been used to obtain the transfer function of the circuit. Consider Figure A-8-1 which portrays this circuit and identifies the nodes that was used to construct the equations for the nodal analysis:

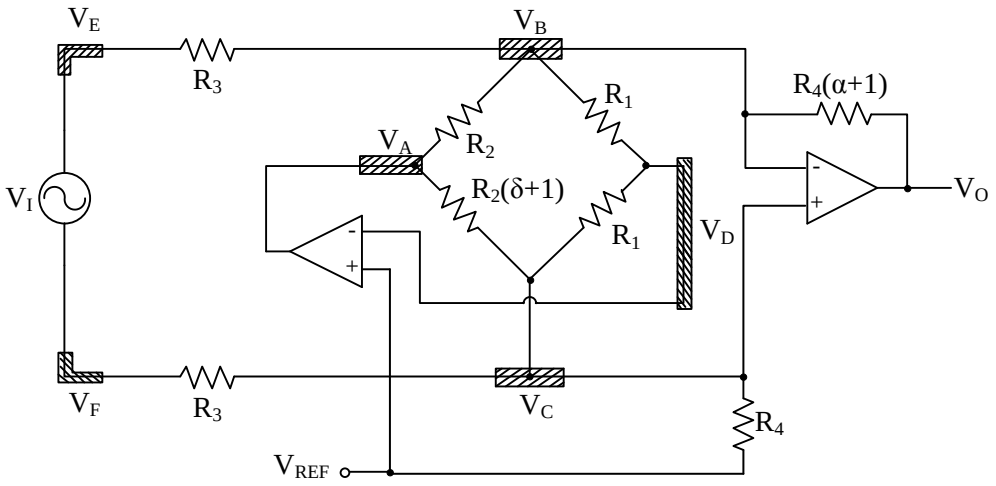

Figure A-8-1: Voltage Measurement Circuit

The variables V_E and V_F respectively represent the differential and common-mode input to the circuit.
Using the selected nodes, the following equations were obtained:

$$\begin{aligned}
&\frac{V_A - V_B}{R_2} + \frac{V_A - V_C}{R_2(\delta+1)} = 0 \\
&\frac{V_B - V_A}{R_2} + \frac{V_B - V_D}{R_1} + \frac{V_B - V_E}{R_3} + \frac{V_B - V_O}{R_4(\alpha+1)} = 0 \\
&\frac{V_C - V_A}{R_2(\delta+1)} + \frac{V_C - V_D}{R_1} + \frac{V_C - V_F}{R_3} + \frac{V_C}{R_4} = 0 \\
&\frac{V_D - V_B}{R_1} + \frac{V_D - V_C}{R_1} = 0
\end{aligned} \tag{9.1}$$

Rearranging the above equations such that V_A, V_B, V_C and V_D are explicitly expressed in terms each other and α and δ:

APPENDIX A

$$\frac{V_D - V_B}{R_1} + \frac{V_D - V_C}{R_1} = 0$$

$$V_D\left[\frac{1}{R_1} + \frac{1}{R_1}\right] = \frac{V_B}{R_1} + \frac{V_C}{R_1} \tag{9.2}$$

$$V_D = \frac{V_B + V_C}{2}$$

$$\frac{V_A - V_B}{R_2} + \frac{V_A - V_C}{R_2(\delta+1)} = 0$$

$$V_A\left[\frac{\delta+2}{R_2(\delta+1)}\right] = \frac{V_B(\delta+1) + V_C}{R_2(\delta+1)} \tag{9.3}$$

$$V_A = \frac{V_B(\delta+1) + V_C}{\delta+2}$$

$$\frac{V_B - V_A}{R_2} + \frac{V_B - V_D}{R_1} + \frac{V_B - V_E}{R_3} + \frac{V_B - V_O}{R_4(\alpha+1)} = 0$$

$$V_B\left[\frac{1}{R_2} + \frac{1}{R_1} + \frac{1}{R_3} + \frac{1}{R_4(\alpha+1)}\right] = \frac{V_A}{R_2} + \frac{V_D}{R_1} + \frac{V_E}{R_3} + \frac{V_O}{R_4(\alpha+1)}$$

$$V_B\left[\frac{R_1R_3R_4(\alpha+1) + R_2R_3R_4(\alpha+1) + R_1R_2R_4(\alpha+1) + R_1R_2R_3}{R_1R_2R_3R_4(\alpha+1)}\right] \tag{9.4}$$

$$= \frac{R_1R_3R_4(\alpha+1)V_A + R_2R_3R_4(\alpha+1)V_D + R_1R_2R_4(\alpha+1)V_E + R_1R_2R_3V_O}{R_1R_2R_3R_4(\alpha+1)}$$

$$V_B = \frac{R_1R_3R_4(\alpha+1)V_A + R_2R_3R_4(\alpha+1)V_D + R_1R_2R_4(\alpha+1)V_E + R_1R_2R_3V_O}{R_1R_3R_4(\alpha+1) + R_2R_3R_4(\alpha+1) + R_1R_2R_4(\alpha+1) + R_1R_2R_3}$$

and

$$V_C\left[\frac{1}{R_2(\delta+1)} + \frac{1}{R_1} + \frac{1}{R_3} + \frac{1}{R_4}\right] = \frac{V_A}{R_2(\delta+1)} + \frac{V_D}{R_1} + \frac{V_F}{R_3}$$

$$V_C\left[R_1R_3R_4 + R_2R_3R_4(\delta+1) + R_1R_2R_4(\delta+1) + R_1R_2R_3(\delta+1)\right]$$

$$= R_1R_3V_A + R_2R_3(\delta+1)V_D + R_1R_2(\delta+1)V_F \tag{9.5}$$

$$V_C = \frac{R_1R_3V_A + R_2R_3(\delta+1)V_D + R_1R_2(\delta+1)V_F}{R_1R_3R_4 + R_2R_3R_4(\delta+1) + R_1R_2R_4(\delta+1) + R_1R_2R_3(\delta+1)}$$

By substituting (9.2) and (9.3) into (9.4), the following is obtained for V_B:

$$V_B = \frac{R_1R_3R_4(\alpha+1)V_A + R_2R_3R_4(\alpha+1)V_D + R_1R_2R_4(\alpha+1)V_E + R_1R_2R_3V_O}{R_1R_3R_4(\alpha+1) + R_2R_3R_4(\alpha+1) + R_1R_2R_4(\alpha+1) + R_1R_2R_3}$$

APPENDIX A

$$V_B = \frac{R_1R_3R_4(\alpha+1)\left[\frac{V_B(\delta+1)+V_C}{\delta+2}\right] + R_2R_3R_4(\alpha+1)\left[\frac{V_B+V_C}{2}\right] + R_1R_2R_4(\alpha+1)V_E + R_1R_2R_3V_O}{R_1R_3R_4(\alpha+1) + R_2R_3R_4(\alpha+1) + R_1R_2R_4(\alpha+1) + R_1R_2R_3}$$

$$= \frac{\left[\frac{R_1R_3R_4(\alpha+1)(\delta+1)}{\delta+2} + \frac{R_2R_3R_4(\alpha+1)}{2}\right]V_B + \left[R_1R_3R_4\frac{\alpha+1}{\delta+2} + R_2R_3R_4\frac{\alpha+1}{2}\right]V_C + R_1R_2R_4(\alpha+1)V_E + R_1R_2R_3V_O}{R_1R_3R_4(\alpha+1) + R_2R_3R_4(\alpha+1) + R_1R_2R_4(\alpha+1) + R_1R_2R_3}$$

$$V_B\left[1 - \frac{\frac{R_1R_3R_4(\alpha+1)(\delta+1)}{\delta+2} + \frac{R_2R_3R_4(\alpha+1)}{2}}{R_1R_3R_4(\alpha+1) + R_2R_3R_4(\alpha+1) + R_1R_2R_4(\alpha+1) + R_1R_2R_3}\right]$$

$$= \frac{\left[R_1R_3R_4\frac{\alpha+1}{\delta+2} + R_2R_3R_4\frac{\alpha+1}{2}\right]V_C + R_1R_2R_4(\alpha+1)V_E + R_1R_2R_3V_O}{R_1R_3R_4(\alpha+1) + R_2R_3R_4(\alpha+1) + R_1R_2R_4(\alpha+1) + R_1R_2R_3}$$

$$V_B\left[R_1R_3R_4(\alpha+1) + R_2R_3R_4(\alpha+1) + R_1R_2R_4(\alpha+1) + R_1R_2R_3 - \frac{R_1R_3R_4(\alpha+1)(\delta+1)}{\delta+2} - \frac{R_2R_3R_4(\alpha+1)}{2}\right]$$

$$= \left[R_1R_3R_4\frac{\alpha+1}{\delta+2} + R_2R_3R_4\frac{\alpha+1}{2}\right]V_C + R_1R_2R_4(\alpha+1)V_E + R_1R_2R_3V_O$$

$$V_B = \frac{\left[R_1R_3R_4\frac{\alpha+1}{\delta+2} + R_2R_3R_4\frac{\alpha+1}{2}\right]V_C + R_1R_2R_4(\alpha+1)V_E + R_1R_2R_3V_O}{R_1R_3R_4(\alpha+1) + R_2R_3R_4(\alpha+1) + R_1R_2R_4(\alpha+1) + R_1R_2R_3 - \frac{R_1R_3R_4(\alpha+1)(\delta+1)}{\delta+2} - \frac{R_2R_3R_4(\alpha+1)}{2}} \quad (9.6)$$

Applying the same for V_C, equations (9.3) and (9.4) are substituted into (9.5):

$$V_C = \frac{R_1R_3V_A + R_2R_3(\delta+1)V_D + R_1R_2(\delta+1)V_F}{R_1R_3R_4 + R_2R_3R_4(\delta+1) + R_1R_2R_4(\delta+1) + R_1R_2R_3(\delta+1)}$$

$$V_C = \frac{R_1R_3\left[\frac{V_B(\delta+1)+V_C}{\delta+2}\right] + R_2R_3(\delta+1)\left[\frac{V_B+V_C}{2}\right] + R_1R_2(\delta+1)V_F}{R_1R_3R_4 + R_2R_3R_4(\delta+1) + R_1R_2R_4(\delta+1) + R_1R_2R_3(\delta+1)}$$

$$V_C = \frac{\left[R_1R_3\frac{\delta+1}{\delta+2} + R_2R_3\frac{\delta+1}{2}\right]V_B + \left[R_1R_3\frac{1}{\delta+2} + R_2R_3\frac{\delta+1}{2}\right]V_C + R_1R_2(\delta+1)V_F}{R_1R_3R_4 + R_2R_3R_4(\delta+1) + R_1R_2R_4(\delta+1) + R_1R_2R_3(\delta+1)}$$

$$V_C\left[1 - \frac{R_1R_3\frac{1}{\delta+2} + R_2R_3\frac{\delta+1}{2}}{R_1R_3R_4 + R_2R_3R_4(\delta+1) + R_1R_2R_4(\delta+1) + R_1R_2R_3(\delta+1)}\right]$$

$$= \frac{\left[R_1R_3\frac{\delta+1}{\delta+2} + R_2R_3\frac{\delta+1}{2}\right]V_B + R_1R_2(\delta+1)V_F}{R_1R_3R_4 + R_2R_3R_4(\delta+1) + R_1R_2R_4(\delta+1) + R_1R_2R_3(\delta+1)}$$

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$$V_C\left[\frac{R_1R_3R_4+R_2R_3R_4(\delta+1)+R_1R_2R_4(\delta+1)+R_1R_2R_3(\delta+1)-R_1R_3\frac{1}{\delta+2}-R_2R_3\frac{\delta+1}{2}}{R_1R_3R_4+R_2R_3R_4(\delta+1)+R_1R_2R_4(\delta+1)+R_1R_2R_3(\delta+1)}\right]$$

$$=\frac{\left[R_1R_3\frac{\delta+1}{\delta+2}+R_2R_3\frac{\delta+1}{2}\right]V_B+R_1R_2(\delta+1)V_F}{R_1R_3R_4+R_2R_3R_4(\delta+1)+R_1R_2R_4(\delta+1)+R_1R_2R_3(\delta+1)} \tag{9.7}$$

$$V_C=\frac{\left[R_1R_3\frac{\delta+1}{\delta+2}+R_2R_3\frac{\delta+1}{2}\right]V_B+R_1R_2(\delta+1)V_F}{R_1R_3R_4+R_2R_3R_4(\delta+1)+R_1R_2R_4(\delta+1)+R_1R_2R_3(\delta+1)-R_1R_3\frac{1}{\delta+2}-R_2R_3\frac{\delta+1}{2}}$$

Substituting V_C into V_B:

$$V_B=\frac{\left[R_1R_3R_4\frac{\alpha+1}{\delta+2}+R_2R_3R_4\frac{\alpha+1}{2}\right]V_C+R_1R_2R_4(\alpha+1)V_E+R_1R_2R_3V_O}{R_1R_3R_4(\alpha+1)+R_2R_3R_4(\alpha+1)+R_1R_2R_4(\alpha+1)+R_1R_2R_3-\frac{R_1R_3R_4(\alpha+1)(\delta+1)}{\delta+2}-\frac{R_2R_3R_4(\alpha+1)}{2}}$$

$$\left[R_1R_3R_4\frac{\alpha+1}{\delta+2}+R_2R_3R_4\frac{\alpha+1}{2}\right]\left\{\frac{\left[R_1R_3\frac{\delta+1}{\delta+2}+R_2R_3\frac{\delta+1}{2}\right]V_B+R_1R_2(\delta+1)V_F}{R_1R_3R_4+R_2R_3R_4(\delta+1)+R_1R_2R_4(\delta+1)+R_1R_2R_3(\delta+1)-R_1R_3\frac{1}{\delta+2}-R_2R_3\frac{\delta+1}{2}}\right\}$$

$$V_B=\frac{+R_1R_2R_4(\alpha+1)V_E+R_1R_2R_3V_O}{R_1R_3R_4(\alpha+1)+R_2R_3R_4(\alpha+1)+R_1R_2R_4(\alpha+1)+R_1R_2R_3-\frac{R_1R_3R_4(\alpha+1)(\delta+1)}{\delta+2}-\frac{R_2R_3R_4(\alpha+1)}{2}}$$

$$\left\{\frac{\left[R_1R_3R_4\frac{\alpha+1}{\delta+2}+R_2R_3R_4\frac{\alpha+1}{2}\right]\left[R_1R_3\frac{\delta+1}{\delta+2}+R_2R_3\frac{\delta+1}{2}\right]}{R_1R_3R_4+R_2R_3R_4(\delta+1)+R_1R_2R_4(\delta+1)+R_1R_2R_3(\delta+1)-R_1R_3\frac{1}{\delta+2}-R_2R_3\frac{\delta+1}{2}}\right\}V_B$$

$$+\left\{\frac{R_1R_2(\delta+1)\left[R_1R_3R_4\frac{\alpha+1}{\delta+2}+R_2R_3R_4\frac{\alpha+1}{2}\right]}{R_1R_3R_4+R_2R_3R_4(\delta+1)+R_1R_2R_4(\delta+1)+R_1R_2R_3(\delta+1)-R_1R_3\frac{1}{\delta+2}-R_2R_3\frac{\delta+1}{2}}\right\}V_F$$

$$V_B=\frac{+R_1R_2R_4(\alpha+1)V_E+R_1R_2R_3V_O}{R_1R_3R_4(\alpha+1)+R_2R_3R_4(\alpha+1)+R_1R_2R_4(\alpha+1)+R_1R_2R_3-\frac{R_1R_3R_4(\alpha+1)(\delta+1)}{\delta+2}-\frac{R_2R_3R_4(\alpha+1)}{2}}$$

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$$V_B\left\{1-\frac{\left[R_1R_3R_4\frac{\alpha+1}{\delta+2}+R_2R_3R_4\frac{\alpha+1}{2}\right]\left[R_1R_3\frac{\delta+1}{\delta+2}+R_2R_3\frac{\delta+1}{2}\right]}{R_1R_3R_4+R_2R_3R_4(\delta+1)+R_1R_2R_4(\delta+1)+R_1R_2R_3(\delta+1)-R_1R_3\frac{1}{\delta+2}-R_2R_3\frac{\delta+1}{2}}\right\}$$

$$\left\{\frac{R_1R_2(\delta+1)\left[R_1R_3R_4\frac{\alpha+1}{\delta+2}+R_2R_3R_4\frac{\alpha+1}{2}\right]}{R_1R_3R_4+R_2R_3R_4(\delta+1)+R_1R_2R_4(\delta+1)+R_1R_2R_3(\delta+1)-R_1R_3\frac{1}{\delta+2}-R_2R_3\frac{\delta+1}{2}}\right\}V_F$$

$$=\frac{+R_1R_2R_4(\alpha+1)V_E+R_1R_2R_3V_O}{R_1R_3R_4(\alpha+1)+R_2R_3R_4(\alpha+1)+R_1R_2R_4(\alpha+1)+R_1R_2R_3-\frac{R_1R_3R_4(\alpha+1)(\delta+1)}{\delta+2}-\frac{R_2R_3R_4(\alpha+1)}{2}}$$

$$V_B\left\{\frac{\begin{array}{c}R_1R_3R_4+R_2R_3R_4(\delta+1)+R_1R_2R_4(\delta+1)+R_1R_2R_3(\delta+1)-R_1R_3\frac{1}{\delta+2}-R_2R_3\frac{\delta+1}{2}\\-\left[R_1R_3R_4\frac{\alpha+1}{\delta+2}+R_2R_3R_4\frac{\alpha+1}{2}\right]\left[R_1R_3\frac{\delta+1}{\delta+2}+R_2R_3\frac{\delta+1}{2}\right]\end{array}}{R_1R_3R_4+R_2R_3R_4(\delta+1)+R_1R_2R_4(\delta+1)+R_1R_2R_3(\delta+1)-R_1R_3\frac{1}{\delta+2}-R_2R_3\frac{\delta+1}{2}}\right\}$$

$$\left\{\frac{R_1R_2(\delta+1)\left[R_1R_3R_4\frac{\alpha+1}{\delta+2}+R_2R_3R_4\frac{\alpha+1}{2}\right]}{R_1R_3R_4+R_2R_3R_4(\delta+1)+R_1R_2R_4(\delta+1)+R_1R_2R_3(\delta+1)-R_1R_3\frac{1}{\delta+2}-R_2R_3\frac{\delta+1}{2}}\right\}V_F$$

$$=\frac{+R_1R_2R_4(\alpha+1)V_E+R_1R_2R_3V_O}{R_1R_3R_4(\alpha+1)+R_2R_3R_4(\alpha+1)+R_1R_2R_4(\alpha+1)+R_1R_2R_3-\frac{R_1R_3R_4(\alpha+1)(\delta+1)}{\delta+2}-\frac{R_2R_3R_4(\alpha+1)}{2}}$$

$$V_B=$$

$$=\left\{\frac{\begin{array}{c}R_1R_3R_4+R_2R_3R_4(\delta+1)+R_1R_2R_4(\delta+1)+R_1R_2R_3(\delta+1)\\-R_1R_3\frac{1}{\delta+2}-R_2R_3\frac{\delta+1}{2}\\-\left[R_1R_3R_4\frac{\alpha+1}{\delta+2}+R_2R_3R_4\frac{\alpha+1}{2}\right]\left[R_1R_3\frac{\delta+1}{\delta+2}+R_2R_3\frac{\delta+1}{2}\right]\end{array}}{R_1R_3R_4+R_2R_3R_4(\delta+1)+R_1R_2R_4(\delta+1)+R_1R_2R_3(\delta+1)-R_1R_3\frac{1}{\delta+2}-R_2R_3\frac{\delta+1}{2}}\right\}$$

$$\left\{\frac{R_1R_2(\delta+1)\left[R_1R_3R_4\frac{\alpha+1}{\delta+2}+R_2R_3R_4\frac{\alpha+1}{2}\right]}{R_1R_3R_4+R_2R_3R_4(\delta+1)+R_1R_2R_4(\delta+1)+R_1R_2R_3(\delta+1)-R_1R_3\frac{1}{\delta+2}-R_2R_3\frac{\delta+1}{2}}\right\}V_F$$

$$\frac{+R_1R_2R_4(\alpha+1)V_E+R_1R_2R_3V_O}{R_1R_3R_4(\alpha+1)+R_2R_3R_4(\alpha+1)+R_1R_2R_4(\alpha+1)+R_1R_2R_3-\frac{R_1R_3R_4(\alpha+1)(\delta+1)}{\delta+2}-\frac{R_2R_3R_4(\alpha+1)}{2}}$$

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$$V_B = \left\{\frac{R_1R_3R_4 + R_2R_3R_4(\delta+1) + R_1R_2R_4(\delta+1) + R_1R_2R_3(\delta+1) - R_1R_3\frac{1}{\delta+2} - R_2R_3\frac{\delta+1}{2}}{R_1R_3R_4 + R_2R_3R_4(\delta+1) + R_1R_2R_4(\delta+1) + R_1R_2R_3(\delta+1) - R_1R_3\frac{1}{\delta+2} - R_2R_3\frac{\delta+1}{2} - \left[R_1R_3R_4\frac{\alpha+1}{\delta+2} + R_2R_3R_4\frac{\alpha+1}{2}\right]\left[R_1R_3\frac{\delta+1}{\delta+2} + R_2R_3\frac{\delta+1}{2}\right]}\right\}$$

$$\left[\begin{array}{l}
\left\{\frac{R_1R_2(\delta+1)\left[R_1R_3R_4\frac{\alpha+1}{\delta+2} + R_2R_3R_4\frac{\alpha+1}{2}\right]}{R_1R_3R_4 + R_2R_3R_4(\delta+1) + R_1R_2R_4(\delta+1) + R_1R_2R_3(\delta+1) - R_1R_3\frac{1}{\delta+2} - R_2R_3\frac{\delta+1}{2}}\right\} \\
\frac{}{R_1R_3R_4(\alpha+1) + R_2R_3R_4(\alpha+1) + R_1R_2R_4(\alpha+1) + R_1R_2R_3 - \frac{R_1R_3R_4(\alpha+1)(\delta+1)}{\delta+2} - \frac{R_2R_3R_4(\alpha+1)}{2}}V_F \\
+ \\
\frac{R_1R_2R_4(\alpha+1)}{R_1R_3R_4(\alpha+1) + R_2R_3R_4(\alpha+1) + R_1R_2R_4(\alpha+1) + R_1R_2R_3 - \frac{R_1R_3R_4(\alpha+1)(\delta+1)}{\delta+2} - \frac{R_2R_3R_4(\alpha+1)}{2}}V_E \\
+ \\
\frac{R_1R_2R_3}{R_1R_3R_4(\alpha+1) + R_2R_3R_4(\alpha+1) + R_1R_2R_4(\alpha+1) + R_1R_2R_3 - \frac{R_1R_3R_4(\alpha+1)(\delta+1)}{\delta+2} - \frac{R_2R_3R_4(\alpha+1)}{2}}V_O
\end{array}\right]$$

(9.8)

Considering equation (9.8), it is evident that V_B is expressed in terms of a constant multiplied by the sum of the multiples of the other variables V_E, V_F and V_O. Analysing the first constant:

$$\frac{\begin{array}{c}R_1R_3R_4 + R_2R_3R_4(\delta+1) + R_1R_2R_4(\delta+1) + R_1R_2R_3(\delta+1) \\ -R_1R_3\frac{1}{\delta+2} - R_2R_3\frac{\delta+1}{2}\end{array}}{\begin{array}{c}R_1R_3R_4 + R_2R_3R_4(\delta+1) + R_1R_2R_4(\delta+1) + R_1R_2R_3(\delta+1) - R_1R_3\frac{1}{\delta+2} - R_2R_3\frac{\delta+1}{2} \\ -\left[R_1R_3R_4\frac{\alpha+1}{\delta+2} + R_2R_3R_4\frac{\alpha+1}{2}\right]\left[R_1R_3\frac{\delta+1}{\delta+2} + R_2R_3\frac{\delta+1}{2}\right]\end{array}}$$

$$= \frac{\left\{R_1R_3R_4 + R_2R_3R_4(\delta+1) + R_1R_2R_4(\delta+1) + R_1R_2R_3(\delta+1) - R_1R_3\frac{1}{\delta+2} - R_2R_3\frac{\delta+1}{2}\right\}}{\left\{R_1R_3R_4 + R_2R_3R_4(\delta+1) + R_1R_2R_4(\delta+1) + R_1R_2R_3(\delta+1) - R_1R_3\frac{1}{\delta+2} - R_2R_3\frac{\delta+1}{2}\right\}}$$

$$-R_3^2R_4(\alpha+1)(\delta+1)\left[\frac{R_1}{\delta+2} + \frac{R_2}{2}\right]^2$$

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$$= \frac{1}{1 - \dfrac{R_3^2 R_4 (\alpha+1)(\delta+1)\left[\dfrac{R_1}{\delta+2} + \dfrac{R_2}{2}\right]^2}{\left\{R_1R_3R_4 + R_2R_3R_4(\delta+1) + R_1R_2R_4(\delta+1) + R_1R_2R_3(\delta+1) - R_1R_3\dfrac{1}{\delta+2} - R_2R_3\dfrac{\delta+1}{2}\right\}}}$$

$$= \frac{1}{1 - \dfrac{R_3^2 R_4 (\alpha+1)(\delta+1)\left[\dfrac{R_1}{\delta+2} + \dfrac{R_2}{2}\right]^2}{\left\{R_1R_3R_4 + R_2R_3R_4(\delta+1) + R_1R_2R_4(\delta+1) + R_1R_2R_3(\delta+1) - R_1R_3\dfrac{1}{\delta+2} - R_2R_3\dfrac{\delta+1}{2}\right\}}}$$

$$= \frac{1}{1 - \dfrac{R_3^2 R_4 (\alpha+1)(\delta+1)\left[\dfrac{R_1}{\delta+2} + \dfrac{R_2}{2}\right]^2}{R_3\left[R_1R_4 + R_2R_4(\delta+1) + R_1R_2(\delta+1) - R_1\dfrac{1}{\delta+2} - R_2\dfrac{\delta+1}{2} + \dfrac{R_1R_2R_4(\delta+1)}{R_3}\right]}}$$

$$= \frac{1}{1 - \dfrac{R_3 R_4 (\alpha+1)(\delta+1)\left[\dfrac{R_1}{\delta+2} + \dfrac{R_2}{2}\right]^2}{R_1R_4 + R_2R_4(\delta+1) + R_1R_2(\delta+1) - R_1\dfrac{1}{\delta+2} - R_2\dfrac{\delta+1}{2} + \dfrac{R_1R_2R_4(\delta+1)}{R_3}}} \tag{9.9}$$

For large values of R_3:

$$\lim_{R_3 \to \infty} \left\{ \frac{R_3 R_4 (\alpha+1)(\delta+1)\left[\dfrac{R_1}{\delta+2} + \dfrac{R_2}{2}\right]^2}{R_1R_4 + R_2R_4(\delta+1) + R_1R_2(\delta+1) - R_1\dfrac{1}{\delta+2} - R_2\dfrac{\delta+1}{2} + \dfrac{R_1R_2R_4(\delta+1)}{R_3}} \right\} \tag{9.10}$$

$$\to \infty$$

Then

$$\lim_{R_3 \to \infty} \left\{ \frac{1}{1 - \dfrac{R_3^2 R_4 (\alpha+1)(\delta+1)\left[\dfrac{R_1}{\delta+2} + \dfrac{R_2}{2}\right]^2}{\left\{R_1R_3R_4 + R_2R_3R_4(\delta+1) + R_1R_2R_4(\delta+1) + R_1R_2R_3(\delta+1) - R_1R_3\dfrac{1}{\delta+2} - R_2R_3\dfrac{\delta+1}{2}\right\}}} \right\} \tag{9.11}$$

$$= 0$$

Thus for large values of R_3

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$$\frac{R_1R_3R_4 + R_2R_3R_4(\delta+1) + R_1R_2R_4(\delta+1) + R_1R_2R_3(\delta+1) - R_1R_3\frac{1}{\delta+2} - R_2R_3\frac{\delta+1}{2}}{R_1R_3R_4 + R_2R_3R_4(\delta+1) + R_1R_2R_4(\delta+1) + R_1R_2R_3(\delta+1) - R_1R_3\frac{1}{\delta+2} - R_2R_3\frac{\delta+1}{2} - \left[R_1R_3R_4\frac{\alpha+1}{\delta+2} + R_2R_3R_4\frac{\alpha+1}{2}\right]\left[R_1R_3\frac{\delta+1}{\delta+2} + R_2R_3\frac{\delta+1}{2}\right]} = 0$$

If this constant equals zero, then V_B will also equal zero according to equation (9.8). Consequently, the output of the circuit can be expressed in terms of the inputs to the circuit:

$$0 = \frac{\left\{\frac{R_1R_2(\delta+1)\left[R_1R_3R_4\frac{\alpha+1}{\delta+2} + R_2R_3R_4\frac{\alpha+1}{2}\right]}{R_1R_3R_4 + R_2R_3R_4(\delta+1) + R_1R_2R_4(\delta+1) + R_1R_2R_3(\delta+1) - R_1R_3\frac{1}{\delta+2} - R_2R_3\frac{\delta+1}{2}}\right\}}{R_1R_3R_4(\alpha+1) + R_2R_3R_4(\alpha+1) + R_1R_2R_4(\alpha+1) + R_1R_2R_3 - \frac{R_1R_3R_4(\alpha+1)(\delta+1)}{\delta+2} - \frac{R_2R_3R_4(\alpha+1)}{2}}V_F$$

$$+ \frac{R_1R_2R_4(\alpha+1)}{R_1R_3R_4(\alpha+1) + R_2R_3R_4(\alpha+1) + R_1R_2R_4(\alpha+1) + R_1R_2R_3 - \frac{R_1R_3R_4(\alpha+1)(\delta+1)}{\delta+2} - \frac{R_2R_3R_4(\alpha+1)}{2}}V_E$$

$$+ \frac{R_1R_2R_3}{R_1R_3R_4(\alpha+1) + R_2R_3R_4(\alpha+1) + R_1R_2R_4(\alpha+1) + R_1R_2R_3 - \frac{R_1R_3R_4(\alpha+1)(\delta+1)}{\delta+2} - \frac{R_2R_3R_4(\alpha+1)}{2}}V_O \quad (9.12)$$

By multiplying (9.12) with

$$R_1R_3R_4(\alpha+1) + R_2R_3R_4(\alpha+1) + R_1R_2R_4(\alpha+1) + R_1R_2R_3 - \frac{R_1R_3R_4(\alpha+1)(\delta+1)}{\delta+2} - \frac{R_2R_3R_4(\alpha+1)}{2}$$

equation (9.12) is simplified to

$$-R_1R_2R_3V_O = \left\{\frac{R_1R_2(\delta+1)\left[R_1R_3R_4\frac{\alpha+1}{\delta+2} + R_2R_3R_4\frac{\alpha+1}{2}\right]}{R_1R_3R_4 + R_2R_3R_4(\delta+1) + R_1R_2R_4(\delta+1) + R_1R_2R_3(\delta+1) - R_1R_3\frac{1}{\delta+2} - R_2R_3\frac{\delta+1}{2}}\right\}V_F + R_1R_2R_4(\alpha+1)V_E$$

$$V_O = \frac{1}{-R_1R_2R_3}\left\{\frac{R_1R_2(\delta+1)\left[R_1R_3R_4\frac{\alpha+1}{\delta+2} + R_2R_3R_4\frac{\alpha+1}{2}\right]}{R_1R_3R_4 + R_2R_3R_4(\delta+1) + R_1R_2R_4(\delta+1) + R_1R_2R_3(\delta+1) - R_1R_3\frac{1}{\delta+2} - R_2R_3\frac{\delta+1}{2}}\right\}V_F + \frac{R_1R_2R_4(\alpha+1)}{-R_1R_2R_3}V_E$$

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$$V_O = \frac{-1}{R_3}\left\{\frac{(\delta+1)\left[R_1R_3R_4\,\frac{\alpha+1}{\delta+2}+R_2R_3R_4\,\frac{\alpha+1}{2}\right]}{R_1R_3R_4+R_2R_3R_4(\delta+1)+R_1R_2R_4(\delta+1)+R_1R_2R_3(\delta+1)-R_1R_3\,\frac{1}{\delta+2}-R_2R_3\,\frac{\delta+1}{2}}\right\}V_F+\frac{-R_4(\alpha+1)}{R_3}V_E \tag{9.13}$$

However, for small values of R_3:

$$\lim_{R_3\to 0}\left\{\frac{R_3R_4(\alpha+1)(\delta+1)\left[\frac{R_1}{\delta+2}+\frac{R_2}{2}\right]^2}{R_1R_4+R_2R_4(\delta+1)+R_1R_2(\delta+1)-R_1\,\frac{1}{\delta+2}-R_2\,\frac{\delta+1}{2}+\frac{R_1R_2R_4(\delta+1)}{R_3}}\right\}$$

But according to L' Hospital:

$$\begin{aligned}
&\lim_{R_3\to 0}\left\{\frac{R_3R_4(\alpha+1)(\delta+1)\left[\frac{R_1}{\delta+2}+\frac{R_2}{2}\right]^2}{R_1R_4+R_2R_4(\delta+1)+R_1R_2(\delta+1)-R_1\,\frac{1}{\delta+2}-R_2\,\frac{\delta+1}{2}+\frac{R_1R_2R_4(\delta+1)}{R_3}}\right\}\\
&=\lim_{R_3\to 0}\left\{\frac{R_4(\alpha+1)(\delta+1)\left[\frac{R_1}{\delta+2}+\frac{R_2}{2}\right]^2}{-\frac{R_1R_2R_4(\delta+1)}{R_3^2}}\right\}\\
&=\lim_{R_3\to 0}\left\{\frac{-R_3^2}{R_1R_2R_4(\delta+1)}R_4(\alpha+1)(\delta+1)\left[\frac{R_1}{\delta+2}+\frac{R_2}{2}\right]^2\right\}\\
&=0
\end{aligned} \tag{9.14}$$

Consequently:

$$\begin{aligned}
&\lim_{R_3\to 0}\left\{\frac{1}{1-\frac{R_3R_4(\alpha+1)(\delta+1)\left[\frac{R_1}{\delta+2}+\frac{R_2}{2}\right]^2}{R_1R_4+R_2R_4(\delta+1)+R_1R_2(\delta+1)-R_1\,\frac{1}{\delta+2}-R_2\,\frac{\delta+1}{2}+\frac{R_1R_2R_4(\delta+1)}{R_3}}}\right\}\\
&=1
\end{aligned} \tag{9.15}$$

If $V_B \neq 0$, then equation (9.13) is not valid anymore and is consequently not an accurate transfer function of the circuit. However, R_3 will never be of such a small value such that it will result in equation (9.13) being invalid.Thus for all practical situations equation (9.13) is an accurate transfer function of the circuit since R3 will always be a significantly large value.

Considering the circuit in terms of differential and common-mode input signals:

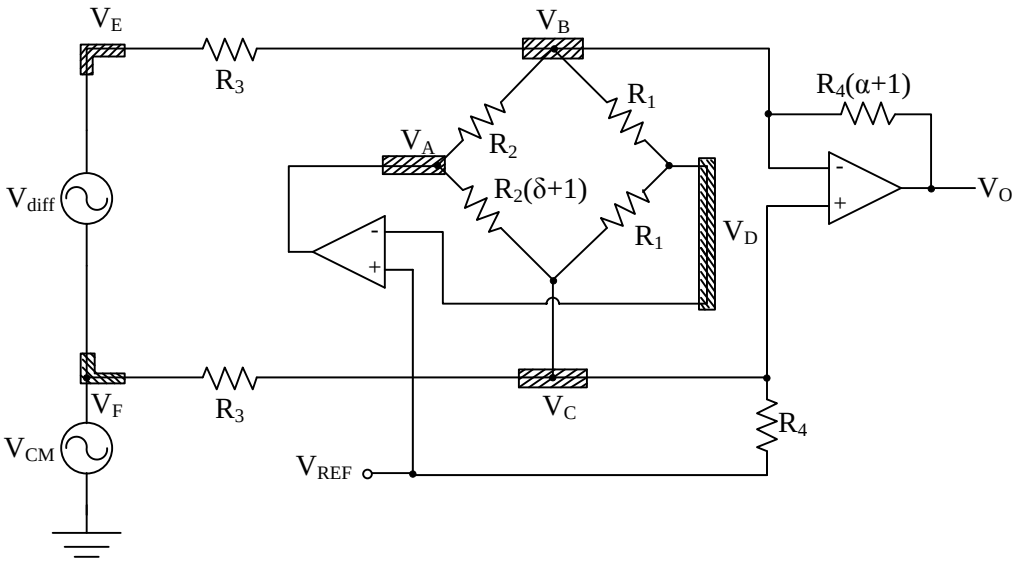

Fig A-8-2: Voltage Measurement Circuit

Equation (9.13) can be rewritten in terms of the common-mode and differential input voltages:

$$V_O = \frac{-1}{R_3}\left\{\frac{(\delta+1)\left[R_1R_3R_4\frac{\alpha+1}{\delta+2}+R_2R_3R_4\frac{\alpha+1}{2}\right]}{R_1R_3R_4+R_2R_3R_4(\delta+1)+R_1R_2R_4(\delta+1)+R_1R_2R_3(\delta+1)-R_1R_3\frac{1}{\delta+2}-R_2R_3\frac{\delta+1}{2}}\right\}V_{CM}+\frac{-R_4(\alpha+1)}{R_3}V_{diff} \quad (9.16)$$

A.2 Current Measurements

Consider the circuit used to measure the current in the system in Figure A-8-3:

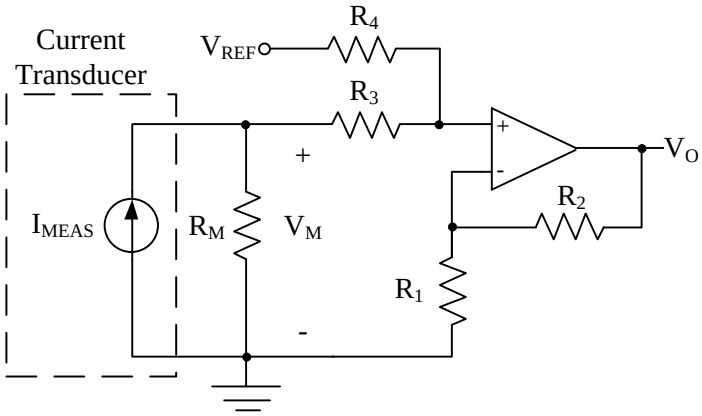

Figure A-8-3: Current Measurement Circuit

Nodal analysis of this circuit results in the voltage at the positive input terminal of the op amp to be found as:

$$\frac{V_p-V_M}{R_3}+\frac{V_P-V_{REF}}{R_4}=0$$
$$V_p=\frac{R_4V_M+R_3V_{REF}}{R_3+R_4} \quad (9.17)$$

where V_P represents the voltage node at the non-inverting input of the op amp. The voltage at the inverting input terminal for the op amp V_n is ideally equal to the voltage at the positive input terminal. Using this presumption, the following nodal equation is constructed:

$$\frac{V_n}{R_1}+\frac{V_n-V_O}{R_2}=0$$
$$\frac{V_O}{V_n}=1+\frac{R_2}{R_1} \tag{9.18}$$
$$V_O=\left(1+\frac{R_2}{R_1}\right)V_p$$

Using (9.17) and (9.18) the output voltage in terms of the measured current and the reference voltage is:

$$V_O=\left(1+\frac{R_2(\delta+1)}{R_1}\right)\left(\frac{R_4}{R_3+R_4}V_M+\frac{R_3}{R_3+R_4}V_{REF}\right) \tag{9.19}$$

Appendix B Circuit Derivations

B.1 Schmitt Trigger

Section 2.8.1 discussed a circuit to establish real-time sensing of the states of contactor and circuit breakers in the line-interactive UPS system. The circuit is depicted in Figure B-1:

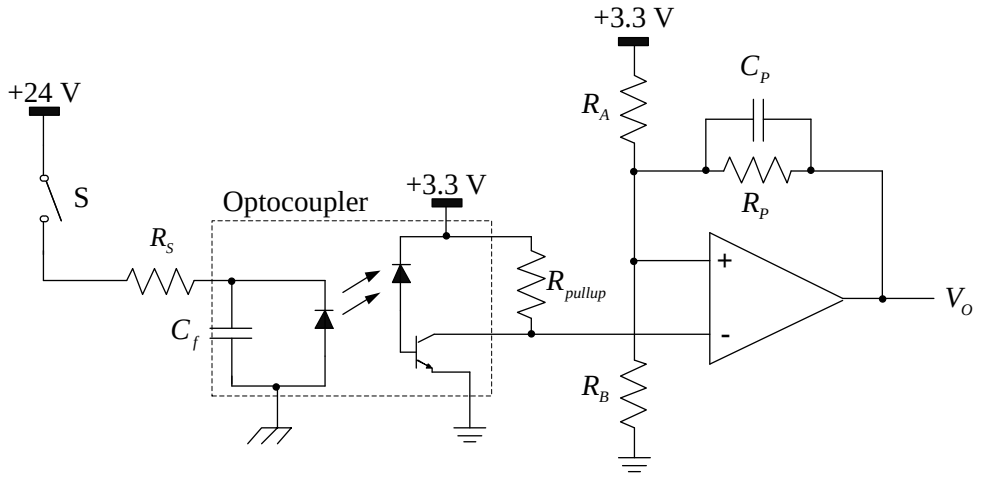

Figure B-1: Sensing Circuit

The positive feedback resistor R_f is used to establish the amount of hysteresis around the threshold established by resistors R_A and R_B. The hysteresis equals the output swing attenuated by a resistive divider former by R_f and $R_A \| R_B$.For a hysteresis voltage V_{hys}, the feedback resistor R_f is calculated as:

$$R_f = \frac{\frac{V_+ R_A R_B}{V_{hys}} - R_A R_B}{R_A + R_B} \tag{9.20}$$

Since $V_+ = 3.3\text{ V}$, $R_A = R_B = 10\text{ k}\Omega$ and choosing a hysteresis of $V_{hys} = 200\text{ mV}$, the resistor is found to be $R_f = 77.5\text{ k}\Omega$. $R_f = 68\text{ k}\Omega$ and produces a hysteresis of $V_{hys} = 226\text{ mV}$.

B.2 Voltage Measurement Circuit

The voltage measurement circuit discussed in section 2.10.1 is again depicted in Figure B-2:

APPENDIX B

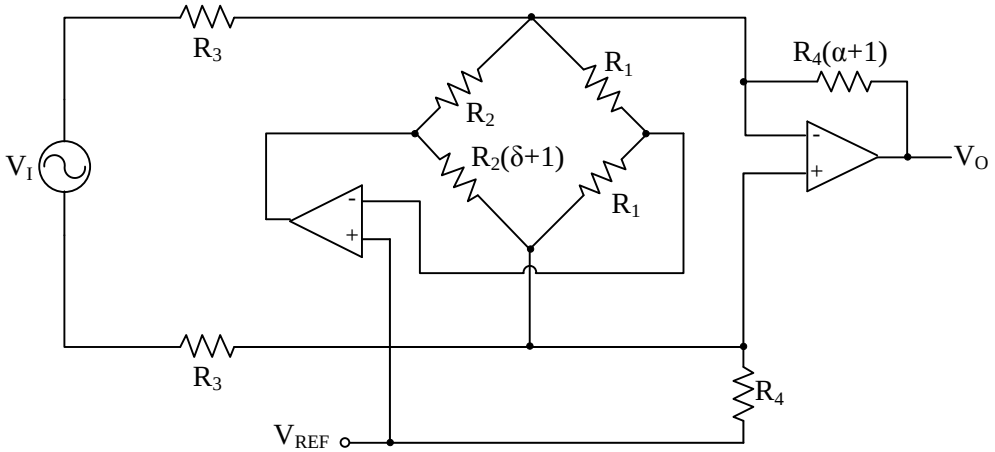

Figure B-2: Voltage Measurement Circuit

The resistors were chosen to be as follows:

$$\begin{aligned} R_1 &= 10\text{k}\Omega \\ R_2 &= 1\ \text{k}\Omega \\ R_3 &= 1\ \text{M}\Omega \\ R_4 &= 8.2\ \text{k}\Omega \end{aligned} \tag{9.21}$$

To ensure that the output signal range is -0 ≤ V_o ≤ 3., the α parameter was calculated by using the boundary condition such that V_o = 3.3 V when 230V_{RMS} is input. Thus when

$$\begin{aligned} V_{diff} &= -230\sqrt{2} \\ &= -325.3\ \text{V} \end{aligned} \tag{9.22}$$

and V_{CM} = 0, the output must equal 3.3 V, which results in α being calculated as:

$$\begin{aligned} \alpha &= \frac{3.3R_3 - V_{diff}R_4}{V_{diff}R_4} \\ &= 0.23 \end{aligned} \tag{9.23}$$

To maintain symmetry of the circuit it is recommended to keep δ = 0.