Compound Converter as MPPT, Battery Regulator and Bus Regulator for Satellite Power Systems

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fulfillment of the requirements for
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at the University of Stellenbosch

Supervisor: Prof. JHR Enslin

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Declaration

I, the undersigned, hereby declare that the work contained in this thesis is my own original work, unless otherwise stated, and has not previously, in its entirety or in part, been submitted at any university for a degree.

HJ Beukes
December 10, 1993

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Opsomming

'n Nuwe saamgestelde-energie omsetter vir lae aardwentelbaan satelliete word voorgestel, deur die parallelle drywingsomsettingstegniek, 'n nuwe maksimum drywingspuntvolger tegniek, gebaseer op die karakteristiek van die sonpaneel, en die piekstroom geprogrammeerde beheertegniek toe te pas. Hierdie tegnieke word gebruik vir lae EMG, hoë effektiviteit, hoë betroubaarheid, stabiliteit en volume vermindering.

Die belangrikste beperking van satelliet kragstelsels is die hoeveelheid energie wat beskikbaar is vanaf die drywingsbron (fotovoltaiese generator). Die kragstelsel moet daarom ontwerp word om die beste gebruik te maak van die beskikbare energie. Meganies, moet die stelsel klein en lig wees.

Verskeie fotovoltaïese kragstelsels gebruik afsonderlike omsetters vir elke funksie van die stelsel. Dit veroorsaak dat baie van die energie in die omsetters verlore gaan.

Die doel van hierdie tesis is om enkele saamgestelde omsetter voor te stel wat die volgende funksies het:

1. Sonpaneel regulering vir maksimum drywing
2. Battery spanningsregulering
3. Bus spanningsregulering

Die tesis beskryf die ontwikkeling van die saamgestelde omsetter in die Sunsat kragstelsel in die besonder. 'n Prototipe ontwerp word vergelyk met die spesifikasies van die stelsel. Toetsresultate en voorstelle vir verdere werk word gegee.

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Summary

A new compound energy converter for low earth orbit satellites is proposed, employing the parallel power conversion technique, a new maximum power point tracking technique based on the characteristics of the PV panel, and the peak current-programmed control technique. These techniques are used for low EMI, high power conversion efficiency, high reliability, stability and size reduction.

The major limitation of satellite power systems is the amount of energy available from the power source (PV generator). The power system should therefore be designed to make most efficient use of the available energy. Mechanically, the system must be small and lightweight.

Several efforts in designing PV power systems use separate converters for each duty the power system should perform. This causes much energy to be lost in the serial path of power flow.

The purpose of this thesis is to introduce and analise a single compound power converter that serves the following purposes:

1. PV array regulation for maximum power (MPPT)
2. Battery voltage regulation
3. Bus voltage regulation

This thesis details the development of the compound converter in the Sunsat power system (SPS). To test the design, a prototype system was constructed to match the requirements of the (SPS). Test results are presented and suggestions for further research are given.

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List of Symbols

A_{core}	cross-sectional area of magnetic core $[mm^2]$
ADCS	attitude determination and control system
A_w	window area of core bobbin $[mm^2]$
BU	battery unit
C	filter capacitor or capacitance $[F]$
C_C	input filter capacitor $[F]$
CMOS	complementary metal oxide semiconductor
COMMS	communication, eg. transmitters and receivers
D	diode or uncontrolled switch
DSP	digital signal processing
dc/dc	direct current to direct current
E	energy $[J]$
E_M	energy not stored in battery $[J]$
E_S	energy stored in battery $[J]$
ESR	equivalent series resistance
FET	field effect transistor
d	duty cycle
DOD	depth of discharge
f	frequency $[Hz]$
I	steady state current $[A]$
i	current $[A]$
I_B	battery current $[A]$
I_C	converter current
I_{PV}	PV current $[A]$
I_O	output current $[A]$
I_L	inductor current $[A]$
L	filter inductor or inductance
LEO	low earth orbit
mmf	magnetic motoric force
MPPT	maximum power point tracker
MRU	main regulator unit
n	turns ratio
N_P	number of primary turns
N_S	number of secondary turns
OBC1	onboard computer number 1
OBC2	onboard computer number 2
P	power $[W]$
P_O	output power $[W]$
P_{PV}	PV power $[W]$
PPCT	parallel power conversion technique

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PV	photovoltaic
PWM	pulse width modulation
P&O	power and optics
Q	transistor, FET, or controlled switch
R	resistance [Ω]
RAM	random access memory
rms	root mean square
SED	"Stellenbosch Elektroniese Dienste"
SPS	Sunsat power system
Sunsat	Stellenbosch University Satellite
t_{on}	on time of one switch of push-pull converter [t]
TTMS	telemetry and modems
V	steady state voltage [V]
v	instantaneous voltage [V]
VLSI	very large scale integration
Z	impedance [Ω]
Δ	dead time of push-pull converter [s]
η	efficiency
η_{MPPT}	efficiency of MPPT
η_{BR}	efficiency of battery regulator
η_B	efficiency of battery
η_R	efficiency of bus regulator
η_W	efficiency of wires
η_W	total efficiency
η_1	converter efficiency from PV generator to load
η_2	converter efficiency from PV generator to battery
ω	angular frequency [rad/s]

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Chapter 1

Overview

1.1 Introduction

The University of Stellenbosch is currently developing a ($0.45 \times 0.45 \times 0.45$ m) Low Earth Orbit (LEO) micro-satellite. Sunsat (Stellenbosch University Satellite) will mainly be used for communication and mapping purposes.

Sunsat will be launched into a circular polar orbit at 805 km altitude. The orbit will be sun synchronized, that means that the angle between the orbit and the rays from the sun stays constant. During the 100 min period for an orbit, the earth rotates 25°, equivalent to 2770 km at the equator. The orbit plane at 99° inclination processes a revolution per year to remain sun synchronous, ie always passing overhead at 10:30 and 22:30. Two satellite passes in the morning between 08:45 and 12:10 and two at night provide nearly 40 min of communication time at a range of less than 2800 km [26], [25], [22].

The Sunsat Power System (SPS) consists of a photovoltaic (PV) Generator, a Main Regulator Unit (MRU), a Battery Unit (BU) and distributed voltage regulator units on the other satellite trays, as shown in Fig. 2.1. These trays are located in the structure of Fig. 1.1 in the following order (from top to bottom):

1. ADCS: Attitude determination and control system
2. RAM: Random access memory
3. OBC2: Onboard computer number 2
4. OBC1, DSP: Onboard computer number 1 and DSP modems
5. Telecommand: Command from ground station
6. TTMS: Telemetry and modems
7. COMMS: Communication, eg. transmitters and receivers

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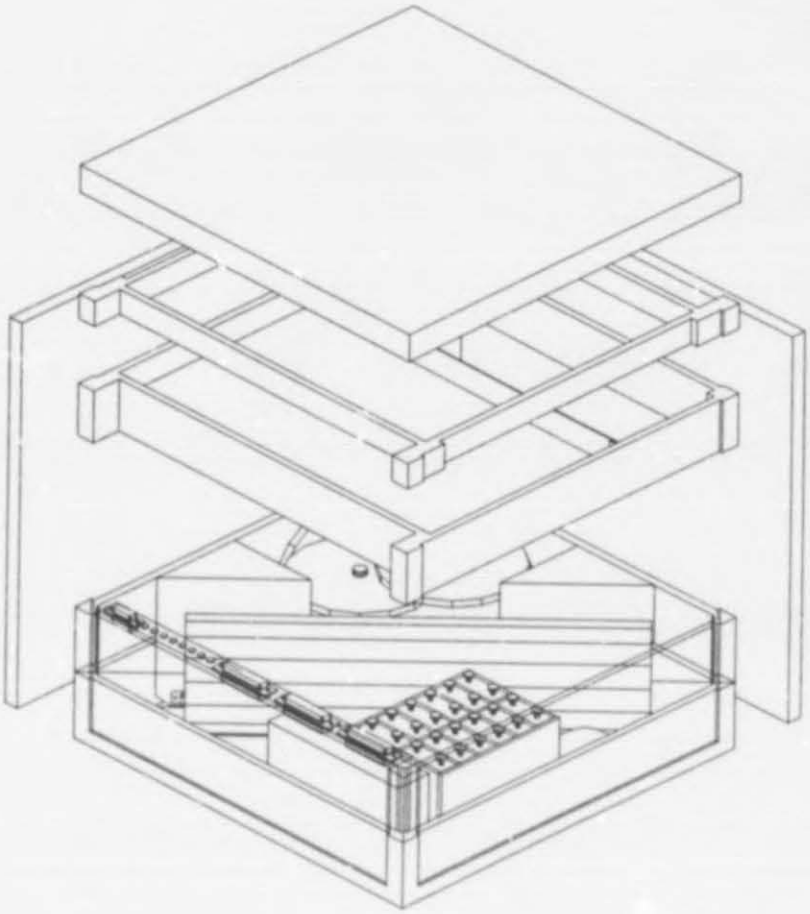

Figure 1.1: Part of Sunsat's mechanical structure Drawn by SED

8. P&O: Power and Optics

The power system receives its instructions from the telecommand subsystem on tray 5 and housekeeping signals are supplied to the telemetry subsystem on tray 6. The telecommand is the interface between the onboard computers (trays 3 and 4) and the power system, as well as the interface between ground control and the power system. The telemetry signals are used by the computers and ground control before making decisions in controlling the power system.

The MRU will be located in the space behind the optics cylinder on the bottom tray (tray 8) of the satellite as shown in Fig. 1.1. The location of the BU is evident from this figure. The four side-panels are covered with solar cells to form the PV Generator.

The major limitation of satellite power systems is the amount of energy available from the power source (PV generator). The power system should therefore be designed to make most efficient use of the available energy. Mechanically, the system must be small

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and lightweight.

Several efforts in designing PV power systems use separate converters for each duty the power system should perform. This causes much energy to be lost in the serial path of power flow.

The purpose of this thesis is to introduce and analise a single compound power converter that serves the following purposes:

1. PV array regulation for maximum power (MPPT)
2. Battery voltage regulation
3. Bus voltage regulation

1.2 Satellite Power Systems

The main purpose of the MRU is to supply the satellite subsystems with power from the PV Generator and to store the remaining energy in the battery unit (BU). The simplest way to do this is shown in Fig. 1.2(a).

The circuit in Fig. 1.2(a) represents a topology where the power from the PV Generator is directly fed to the battery and the load through a serial diode. The purpose of the diode is to prevent the battery from discharging into the PV generator in low insolation conditions. The problem with this topology is that the operating voltage of the PV generator is determined by the battery voltage. This is not necessarily the maximum power point of the generator. A device is needed between the generator and the battery that will match the battery voltage and the maximum power point voltage of the generator under all conditions. This device is called a maximum power point tracker (MPPT) and is included in Fig. 1.2(b).

The circuit in Fig. 1.2(b) represents a topology where all the power needed by the load will be drawn, and the remaining energy delivered by the generator will charge the battery. At some stage the battery will be fully charged. The energy will then be dissipated in the battery as heat, which is totally undesirable. This can be prevented by regulating the power to the battery. A battery regulator is therefore included in the power path to the battery, as shown in Fig. 1.2(c).

The circuit in Fig. 1.2(c) supplies an unregulated bus to the load, but the battery is not isolated from it. To regulate the bus voltage and to isolate it from the battery, a third device is included, namely a bus regulator, which is shown in Fig. 1.3(a).

With regard to other existing satellite power systems, the tendency over the past few years has been that more designers use the regulated bus system architecture [6], [11].

The following advantages of the regulated bus can be listed [8]:

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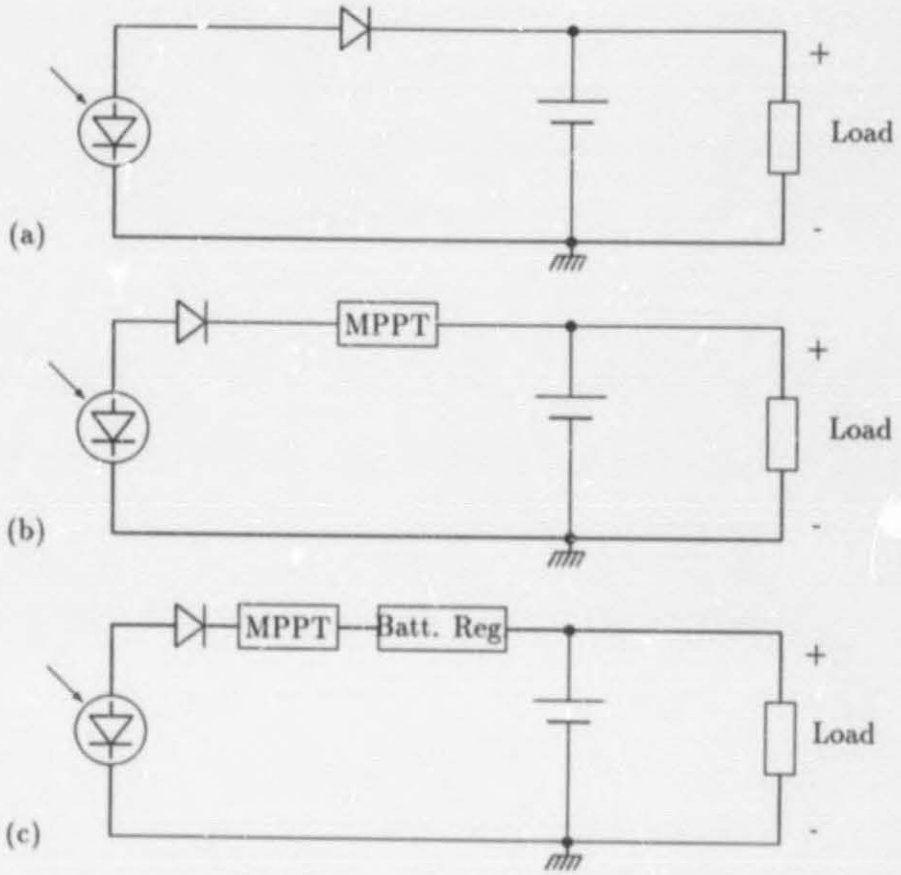

Figure 1.2: (a) A basic power circuit, (b) A power circuit with an MPPT included, (c) A power circuit with an MPPT and battery regulator

- low and controlled source impedance for the decentralised loads
- better EMC susceptibility behaviour (low frequency filtering)
- better source coupling performance (allows the simultaneous and controlled transfer of energy from several power sources)
- greater development flexibility

The overall efficiency of a power system (Fig. 1.3(a)) comprises the efficiency of the subsystems. A power system that consists of an MPPT (η_{MPPT}), a battery regulator (η_{BR}), a battery backup (η_B), a bus regulator (η_R) and wiring (η_W), will have a total efficiency (η_T) of [9]:

$$\eta_T = \eta_{MPPT} \cdot \eta_{BR} \cdot \left[\frac{E_M + \eta_B E_S}{E_M + E_S}\right] \cdot \eta_R \cdot \eta_W \tag{1.1}$$

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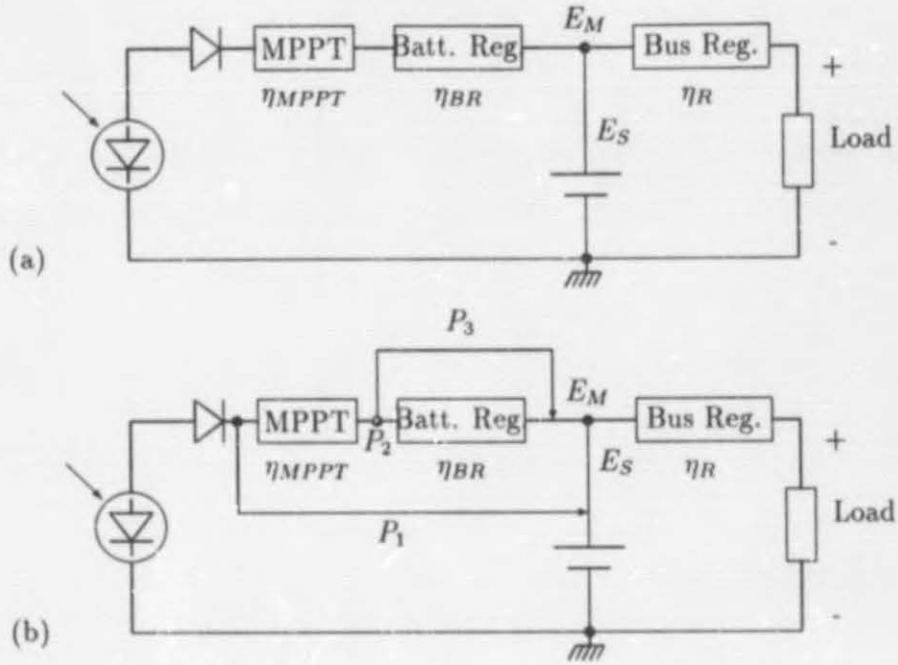

Figure 1.3: (a) A power circuit with an MPPT, a battery regulator and a bus regulator, (b) Illustration of the application of the PPCT.

where E_M is the energy required by the load and E_S is the excess power stored in the battery. Contrary to cascade power conditioning systems (Fig. 1.3(a)), where only a single route for the flow of power between the source and the load exists, the parallel power conversion technique (PPCT) [9] employs parallel routes of higher efficiency for power flow between the source and the load, as shown in Fig. 1.3(b) (P_1, P_2 and P_3).

1.3 Maximum Power Control

In this section the theory which led to the development of the maximum power point tracker (MPPT) in Section 3.7, is discussed.

1.3.1 Characteristics of a PV Panel

Effect of Irradiance

As the irradiation levels increase, the PV current also increases. The maximum power point of the panel increases at a steep positive slope, proportional to the irradiation. Higher irradiation levels result in associated higher power maxima, if the cell temperature is constant. This trend also continues for irradiation levels higher than one sun. The only

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parameter that influences the irradiation level of the solar panels is the angle by which the solar rays reach the panel [10].

Effect of Cell Temperature Variations

The cell temperature of the PV panel is a function of the insulation levels, the satellite temperature, the rate at which the cell is cooled and the way the panel is constructed. An increase in cell temperature will result in a lower open circuit voltage and a lower maximum power point, but associated with it is a slightly higher short-circuit current.

The combined effect of cell temperature and irradiance level can greatly affect available power from the PV generator. By using maximum power control some power loss can be avoided [10].

1.3.2 Maximum Power Point Tracking

To obtain maximum power output from an array of photovoltaic cells under changing insolation and temperature conditions, it is necessary to use a circuit to optimize the electrical operating conditions of the array. This circuit is called a maximum power point tracker and normally consists of a power section and a control section [19]. As mentioned in the previous paragraphs, the power section is incorporated in the compound converter.

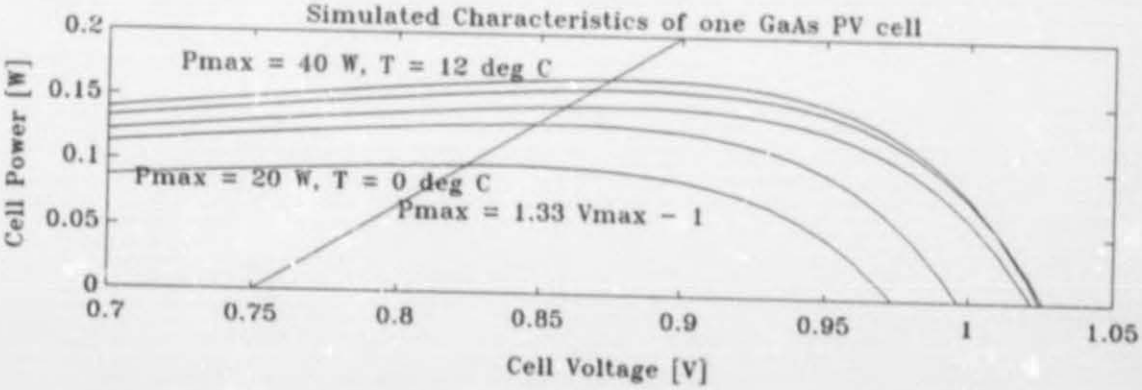

Figure 1.4: MPPT loci with insolation and temperature as parameters

The objective of the control section is to control some parameters of the converter, such as the duty cycle, in such a way as to operate the photovoltaic array at its maximum power point. Previously used methods of achieving this goal include voltage-feedback and power feedback methods [19].

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1.3.3 Voltage-Feedback Methods

The simplest control method is to keep the array near the maximum power point by regulating the array voltage and matching it to a fixed reference voltage. It is assumed that any variations in the insolation and temperature of the array are insignificant, and that the constant reference voltage is an adequate approximation of the true maximum power point.

A step further is to vary the array reference voltage according to variations in the array temperature and insulation. One way to get information related to array temperature and insulation is to measure the array or cell open-circuit voltage. This can be done by using a small open-circuited reference cell, electrically separate from the rest of the array. For a satellite, a reference cell would be difficult to use, because of the necessity of leaving space for it on the solar array, and problems in making it adequately representative of the entire array. To overcome these problems, the actual open-circuit array voltage can be measured by momentarily interrupting the normal operation of the array and the MPPT. It is found that setting the reference voltage to a fixed fraction of the open-circuit voltage results in adequate tracking of the maximum power point over variations in insulation and temperature [17].

1.3.4 Power-Feedback Methods

A controller which directly finds the actual maximum power point, instead of estimating it from measurements of other quantities, has the advantage of being independent of any previous knowledge of the array characteristics. Such a controller needs to have a measurement indicative of the array power, and an algorithm implemented in software or hardware to find a local power maximum.

Measuring Power

Since the initial objective is to operate the photovoltaic array at its maximum power point, many systems measure and maximize the power at the photovoltaic array terminals [9]. The controller in [9] uses a low cost microprocessor. The array voltage and current are measured at the input of the converter and digitally multiplied to represent the array power. This value forms the basis of the MPPT loop, since it is used in a basic hill climbing algorithm to follow the maximum power point of the solar array. Pulsewidth modulation is performed in such a way that the voltage of the loaded solar array is at the maximum power point.

It is more important, however, to maximize the actual usable power: the output power of the MPPT. Despite the theoretical advantage of measuring output power, the penalty for measuring array power is very small, and therefore either can be used. This is because typical MPPTs are very high in efficiency over a wide range of operating points, and

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maxima of input and output powers occur very close to the same point [19].

The array power can be measured by multiplying its voltage and current, either with a microprocessor or with an analog multiplier. In either case, the complexity, expense, and power required to measure and multiply the two quantities are undesirable. In [10] it is pointed out that with a battery of approximately constant voltage for a load, the output power can be maximized by just maximizing output current.

For many loads, a voltage measurement would work equally well as the measurement of the current . However, in the case of a battery being the load, the MPPT output voltage changes relatively little with changes in output power, whereas the output current varies strongly. Furthermore, measuring the current output instead allows many MPPT outputs to be connected in parallel. In the case of the compound converter the battery and the constant voltage bus are two parallel outputs of the MPPT.

1.3.5 Maximizing Algorithms

One general approach to the problem of finding a local maximum of output power by adjusting array voltage is to sense the derivative, $\frac{dP_{PV}}{dV_{PV}}$, and to use feedback to force this quantity to zero. Variations of this scheme are used in many published maximum power point tracker designs. One common variation is to dispense with explicit dependence on V_{PV}, and to directly use a control parameter instead, such as the duty cycle. The derivative used is then $\frac{dP_{PV}}{dD}$, and thus no inner feedback loop controlling array voltage is needed. As discussed in the previous section, P_{PV} is also not used explicitly. The derivative actually used is $\frac{dI_C}{dD}$. This method is used in [19].

A new simplified control strategy, based on positive feedback control of the output current, was introduced for the MPPT [10]. It has a high reliability, because of its low complexity.

This controller uses a simple control law, which represents the output power characteristics of the PV array shown in Fig. 1.4. It is obtained from a signal directly proportional to the output current of the converter, which is also proportional to the power output of the converter to the battery and to the load, because the battery voltage is slowly changing and the output voltage is kept constant independently:

$$P_{PV} = \frac{P_O}{\eta_1} + \frac{P_B}{\eta_2} = k_1 I_O + k_2 I_B \tag{1.2}$$

where $k_1 = \frac{V_L}{\eta_1}$ and $k_2 = \frac{V_B}{\eta_2}$ and η_1 and η_2 is the equivalent power conversion efficiency of the converter to the load and to the battery respectively.

This MPPT was implemented as in [10], but it was not successful and the theoretical analysis of this idea led to the development of an MPPT based on negative feedback of output power.

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1.4 Parallel Power Conversion

Using the parallel power conversion technique (PPCT), a technique for Maximum Power Point Tracking (MPPT) was introduced, employing a capacitor in series with the PV array and the battery unit [9]. Fig. 1.5 shows the technique schematically.

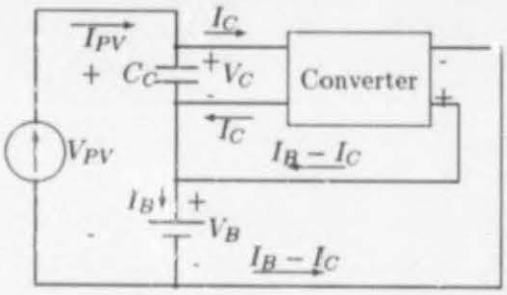

Figure 1.5: MPPT with capacitor in series with PV array and battery

Most of the time the capacitor C_C is the decoupling capacitor at the input of the converter and no extra capacitor is needed. Maximum power point tracking is performed by controlling the converter output current to load the PV array in such a manner as to keep the PV array at its maximum power point. When the capacitor voltage V_C, for instance, is equal to the battery voltage V_B, the power delivered to the battery equals the power delivered to the capacitor. Under this condition, half of the PV power is supplied directly to the battery at an efficiency of nearly 100%, if the conduction losses of the cabling are ignored, while the other half is converted to the battery by means of the power converter. When the converter in Fig. 1.5 operates at an efficiency of η_m, the effective PV converter efficiency employing the PPCT (η_{me}) can, in general, be written as follows[1] [9]:

$$\eta_{me} = \frac{P_{out}}{P_{in}} = \frac{Input\ Power\ to\ Battery}{Output\ Power\ from\ PV\ Array}$$

$$= \frac{V_B I_C + \eta_m V_C I_C}{(V_C + V_B) I_{PV}}$$

$$\eta_{me} = \frac{1 + \eta_m \frac{V_C}{V_B}}{1 + \frac{V_C}{V_B}} \tag{1.3}$$

This means that the efficiency improvement becomes significant when the capacitor voltage is smaller or equal to the battery voltage [9]. The SPS PV array consists of enough cells in series to maintain an average PV voltage (maximum power) of 24 V, because the battery voltage is nominal 12 V.

[1]Note that I and V refer to average values

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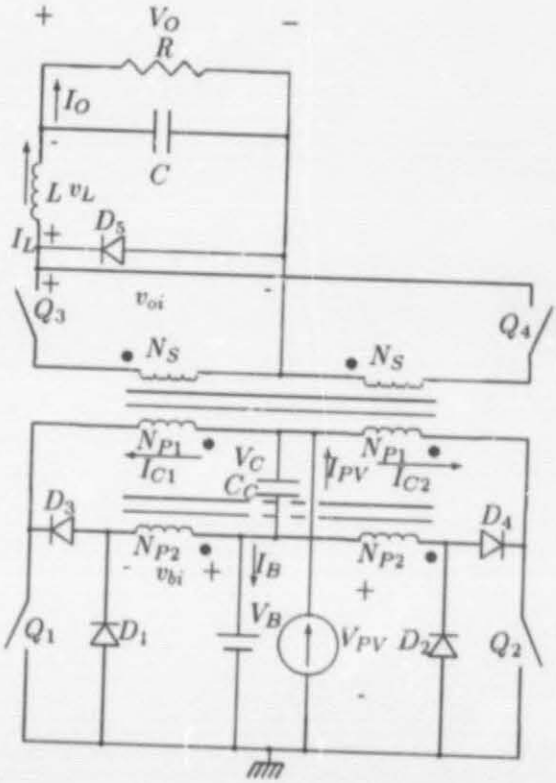

Figure 1.6: Circuit diagram of Compound Converter

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1.5 Development of a Compound Converter

The discussions in the previous sections led to the development of the compound converter. The circuit diagram of the compound converter is shown in Fig. 3.1. The load current consists of current supplied by the solar array and current supplied by the battery. Referring to Fig. 3.1, the load current can be written as follows:

$$I_O = n_1 I_{PV} - n_2 I_B \tag{1.4}$$

where $n_1 = \frac{N_{P1}}{N_S}$ and $n_2 = \frac{N_{P2}}{N_S}$. From (3.1) two states of the converter can be specified, namely when I_B is positive or zero and negative respectively. The analysis and synthesis of the compound converter is detailed in Chapter 3.

1.6 Summary

This chapter was an introduction to satellite power systems. After looking at several topologies of power systems, the decision was made to use a topology consisting of a maximum power point tracker, a battery regulator and a bus voltage regulator. These converters have the disadvantage that they decrease the efficiency of the power system. By using a compound converter that makes use of the parallel power conversion technique, the aim for the rest of this thesis is to increase the total system efficiency.

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Chapter 2

The Sunsat Power System

2.1 Introduction

The Sunsat Power System (SPS) block diagram is shown in Fig. 2.1.

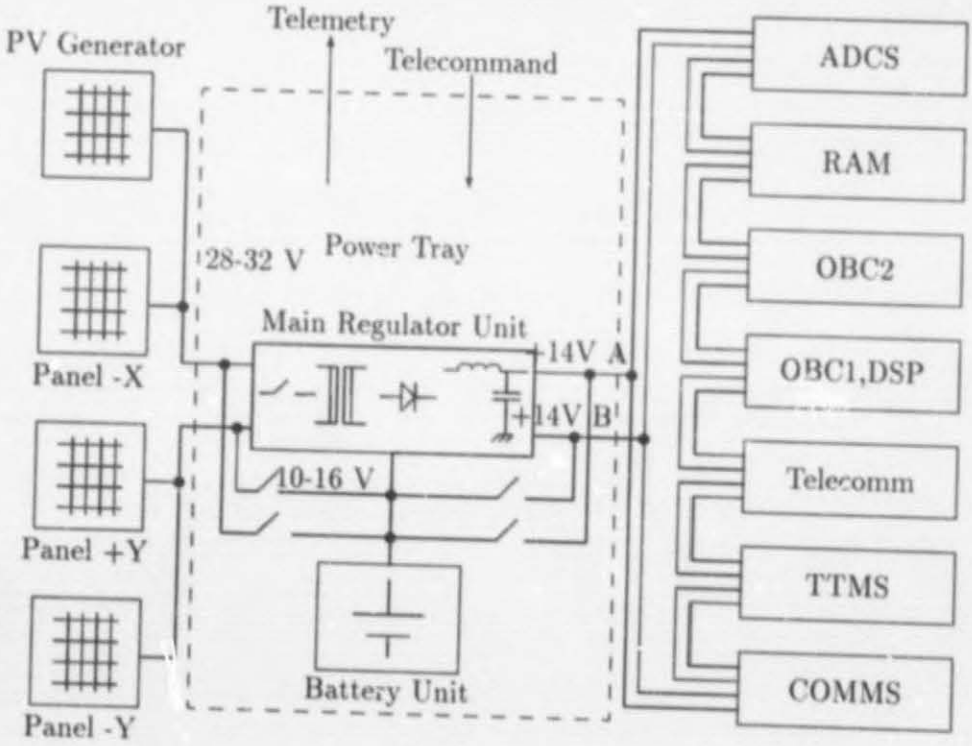

Figure 2.1: The Sunsat power system block diagram

The PV Generator integrated with the BU forms the core of the power system. The BU supplies the load during eclipse intervals and helps the PV generator to meet the peak

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load. Proper sizing and operating modes of the SPS are very important. For the best possible performance of a power system, power simulation is suggested.

The appropriate size of the PV array and the battery are dictated by the following requirements:

1. Average load over one orbit
2. Peak load over one orbit
3. Peak power output of the battery
4. Ability of the battery to support the load for the whole eclipse interval
5. Ability of the PV array and battery to jointly support the system peak demand

The main restriction in the sizing of the power system, however, is the maximum mass and size of the satellite. The first step in designing the SPS was to design the PV Generator as large as possible with the limited space on the satellite. The second step was to make a prediction of the load profile by simulating the power system. The size of the BU and MRU were chosen according to the power simulation . It was also evident from the simulation that power management is important in the SPS.

2.2 PV Generator

The first step in designing the PV generator was to decide upon the cell material to be used. Silicon is still the solar cell choice for most spacecraft because of its low price, availability and proven track record. Gallium arsenide ($GaAs$), however, is becoming more popular, because it is a more efficient producer of electricity, is more resistant to radiation, and loses less of its efficiency to the intense sunlight in Space. Indium phosphide (InP) as solar cell material is similar to $GaAs$ in efficiency, but is even more radiation resistant. At this stage there are no economical methods to process it, and it is therefore not frequently used. The logical choice of material to use, therefore, is $GaAs$.

The major suppliers of satellite solar cells in the U.S. are Applied Solar Energy Corporation (ASEC) and Spectrolab. In Europe the major suppliers are EEV and AEG. AEG has supplied solar panels to several satellites from as early as 1965. Examples of satellites still in orbit with AEG panels are: Intelsat VII, Spot4, Polar Platform and Cluster. EEV has done much research on $GaAs$ on the solar panels of: LIPS III, EURECA, UoSAT-E, UoSAT-F, STRV1A & B and STRV1. EEV will be the logical supplier for the Sunsat PV Generator, for economical reasons and because Sunsat is in the same category as the UoSATs.

The only area available for the PV Generator is on the four side-panels of the satellite. The PV Generator Specifications in App. B were composed by using the data of the EEV

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GaAs solar cells, and fitting these cells on to the available area. A graphical presentation of the composition of each PV panel, with its electrical interfaces with the rest of the SPS, is shown in the schematic diagrams of App. G.

2.3 Power Simulation

The Sunsat power system was simulated by writing a simulation programme in `Turbo Pascal`[1] in order to do proper sizing of the BU and the MRU. It was also important to see if the PV generator can produce enough energy for all the subsystems.

The first step was to simulate the orbit and footprint of the satellite as well as the borders of South Africa as accurately as possible. From here the load profile could be simulated, the programme knowing when each subsystem would operate and the amount of energy each system would use in each position in the orbit. These data are shown in Table 2.1. P_{on} is the peak power, t_e is duty ratio of maximum power consumption, day is 1 when the system does not operate during eclipse intervals, Latnd, Latsb, Loneb and Lonwb are the borders for maximum power consumption, P_{off} is the power consumption for the rest of an orbit and t_{ne} is the duty ratio in this part.

The power produced by the PV Generator was simulated according to the programme's knowledge of the effective area made up by solar cells (A) from App. B and the angle by which the solar rays reach the panels (ϕ_i):

$$P(t) = \sum_{i=1}^{4} K \times A \times cos\left(\phi_i(t)\right) \tag{2.1}$$

K is the solar constant or the amount of power on 1 m^2 perpendicular to the incoming rays in space and has a value of about 1 kW.

Most of the energy falling on to the PV panels is useless, because the cells can only convert light in a certain optical range to electrical energy. The rest of the energy is dissipated as heat. Also, the efficiency is heat dependent. By using data from the temperature simulation [40] written in `Matlab-386`[2] the effect of cell temperature was included. The degradation of the panels within space was also included.

The path the power has to flow was simulated by simulating the efficiency of all the power converters at different power points. This was done by a linear approximation of the efficiency curves.

Knowing what power is available, the programme subtracts the power needed by the load in order to get the power which must be stored in the battery unit. By integrating this power in time, the state of charge of the battery is obtained.

[1] Borland
[2] MathWorks Inc.,Natick MA, USA

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Tray	Unit	$P_{on}[W]$	$t_c[\%]$	day	Latnb	Latsb	Loneb	Lonwb	P_{off}
ADCS 2+1	Star Sensor	2.6	33	0	90	-90	180	-180	0
	Reaction Wheels	0.11	25	1	SANB	SASB	SAEB	SAWB	0
	Horizon Sensor	0.88	33	0	90	-90	180	-180	0
	CCD Sun Sensor	0.88	33	0	90	-90	180	-180	0
	PV Sun Sensor	0.5	33	0	90	-90	180	-180	0
	8031	0.5	33	0	90	-90	180	-180	0
	T800	0.5	33	0	90	-90	180	-180	0
	Magneto Meter	0.5	100	0	90	-90	180	-180	0
	Magneto Torquer	32	5	1	SANB	SASB	SAEB	SAWB	0
RAM 2+1	RAM	3	50	0	90	-90	180	-180	1
	Imager Digital	1	100	1	SANB	SASB	SAEB	SAWB	0
OBC2	OBC2	2.5	20	0	90	-90	180	-180	1
OBC1,DSP	OBC1	2.5	20	0	90	-90	180	-180	1
	DSP	0.7	100	0	90	-90	180	-180	0
Telecomm	Telecommand	0.25	100	0	90	-90	180	-180	0
TTMS	Telemetry	2.24	100	0	90	-90	180	-180	0
	Modems	1	100	0	90	-90	180	-180	0
Comms	CMDR	1	100	0	90	-90	180	-180	0
	UHFR	2	100	0	SANB	SASB	SAEB	SAWB	1
	VHFR	2	100	0	SANB	SASB	SAEB	SAWB	1
	UHFT	0.45	100	0	SANB	SASB	SAEB	SAWB	0.225
	VHFT	0.45	100	0	SANB	SASB	SAEB	SAWB	0.225
	SBT	5	100	1	SANB	SASB	SAEB	SAWB	0
	P/A	20	100	0	SANB	SASB	SAEB	SAWB	0
	RXSynth	0.05	20	0	30	-90	60	0	0
	TXSynth	0.05	10	0	30	-90	60	0	0
Op,Power	Imager Analog	28.5	100	1	SANB	SASB	SAEB	SAWB	0
	Power	2	100	0	90	-90	180	-180	0
	Reaction Wheels	15	25	1	SANB	SASB	SAEB	SAWB	0

Table 2.1: Power consumption of subsystems

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Later the simulation was incorporated in the overall Sunsat simulation [39], which was written in *SIMuWIN*[3], a Microsoft Windows[4] application. *SIMuWIN* is a complete software environment for the simulation of nonlinear dynamic systems [31]. It is one of the new generation block-diagram-based simulation languages. This is a more accurate simulation, because fewer approximations are made, e.g. lookup tables are used to implement efficiency curves.

Detail information on the power simulation can be found in App. E and in [1], [37].

Fig. 2.2 is a typical output of the simulation without load management.

The first output shows the power supply from the PV Generator. It is clear that the satellite is sun synchronous, because the same power curve repeats itself during each orbit (angle between orbit and incoming rays is constant). The maximum power supply is 40 W, while the minimum power supply is 20 W.

The second output is the power demand of the satellite. The peak power demand in this curve is more than 150 W. This is too high compared to the average load of 20 W. By doing proper load management this value should be limited.

The third output gives the state of charge of the battery. It can be seen that if peak power consumption occurs during an eclipse, the battery is so deeply discharged that it needs about 14 orbits to recharge. The power consumption should therefore be limited during eclipse by means of proper load management.

The fourth output is the position of the satellite in its orbit.

2.4 Battery Unit

The battery unit will have a nominal voltage of 12 V. This value has been chosen because the battery will be directly connected to the bus in case of MRU failure. In this mode of operation, the subsystems should still be able to operate from the battery voltage. From the power simulation in Section 2.3, the capacity of the battery was determined to be at least $4Ah$. The battery shall therefore consist of 11 1.2 V cells, each rated at at least 4 Ah.

The first step in designing the BU was to decide upon the electrochemical technology to use. The three existing technologies for small satellites are nickel-cadmium ($NiCd$), nickel-metal hydride ($NiMH$) and nickel-hydrogen (NiH_2). $NiCd$, of course, is the oldest technology, and only one supplier's database [13] contains a total of 117 spacecraft with approximately 644 total mission years of successful $NiCd$ performance without a recorded failure. $NiMH$ is an emerging technology that appears amenable for powering small spacecraft. In this technology the cadmium or negative electrode from $NiCd$ is

[3]University of Stellenbosch
[4]Microsoft Corporation

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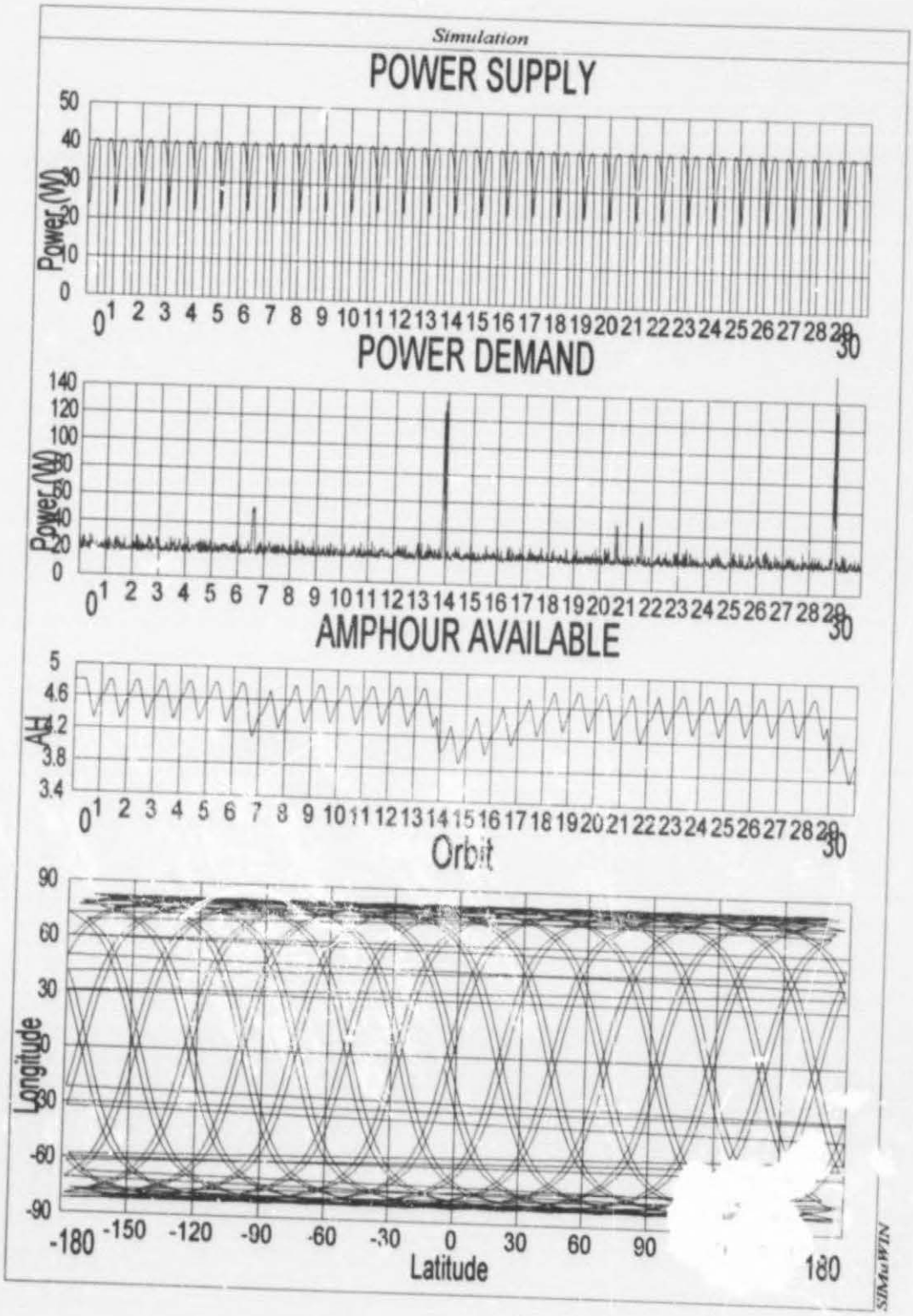

Figure 2.2: Simulation in *SIMuWIN*

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replaced by the metal-hydride electrode to form this electrochemical couple. $NiMH$ provides a reduction in both weight and volume as compared to $NiCd$ technology. NiH_2 is another emerging technology that appears amenable for powering small spacecraft. In this technology, the superior capability of the NiH_2 electrochemistry is combined with the simplicity and robustness of $NiCd$ packaging technology. At 20 % depth of discharge (DOD), the number of charge-discharge cycles of the different technologies is as follows:

- commercial $NiCd$: 2 500
- space qualified $NiCd$: 15 000 cycles
- $NiMH$: 24 000 cycles
- NiH_2: 64 000 cycles

The expected lifetime of the SPS is 5 years. This means that, according to Section 2.3, the BU will have approximately 144 000 charge-discharge cycles. Most of the time, however, the DOD will be much less than 20 %.

The next step in designing the BU was to consider different suppliers' products. The main suppliers were contacted, with the following responses: The Ilbercraft cells are too big for the SPS. Yardney and Eagle Picher can supply NiH_2 cells, perfect for the SPS. Due to a lack of funds, the $NiCd$ technology was chosen, because SAFT can supply 8 Ah cells at a special price.

By using the data of the SAFT 8 Ah battery cells, the BU Specifications in App. D were composed. [7], [18], ,[15], [13] and [36] contain useful information on batteries. A graphical representation of the battery composition with its electrical interfaces with the rest of the SPS is shown in the schematic diagrams of App. G. Note that each cell has a parallel diode to prevent any open-circuit failure.

2.5 Main Regulator Unit

The characteristics of the main regulator unit (MRU) is detailed in Chapter 1. From the power simulation it is evident that the appropriate size of the MRU is as follows:

1. Average load over one orbit: 25 W
2. Peak load over one orbit: 100 W

The nucleus of the MRU is the Compound Converter (CC) which will be analised, designed and tested in the following chapters. Two of these converters (A and B) will be used in parallel for redundancy (no single-point failures). This can be done because the compound converter is much smaller than separate converters in series are. Each converter will be able to handle 70 % of the peak power consumption. Only one converter will

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Signal	Description
REGSD_A	regulator A shut-down
REGSD_B	regulator B shut-down
SP_BATT1	PV gen. 1 batt. connect
SP_BATT2	PV gen. 2 batt. connect
BATT_+14A1	battery +14VA connect
BATT_+14A2	battery +14VA connect
BATT_+14B1	battery +14VB connect
BATT_+14B2	battery +14VB connect

Table 2.2: Telecommand Signals

be in operation at normal load conditions. At peak load the second converter will automatically start operating. This is accomplished by regulating the two buses somewhat differently and connecting them through diodes. In case one converter fails, the other converter will be able to supply 70 % of the peak demand to the subsystems. A fail-safe mode is also included for when both regulators fail. This implies that the unregulated battery-voltage will be available for the distributed regulators.

The state of the MRU is determined by the telecommand signals. In case some part or the entire MRU fails, the telecommand will switch power through an alternative route. The functional descriptions of the telecommand signals are listed in Table 2.2. In the system block diagram (Fig. A.1) of App. A the telecommand switches are shown. These switches consist of p-channel MOSFETs [5] as power switch and a simple drive circuit, as shown in Fig. G.7 in App. G.

The telemetry sensors monitor the condition of the power system and are also part of the MRU. The functional descriptions of the telemetry sensors are listed in Table 2.3. In the system block diagram (Fig. A.1) of App. A the telemetry sensing points are shown. They consist of current, voltage and temperature sensors, as shown in Fig. G.13 and Fig. G.14 of App. G.

2.6 Power Distribution System

There is a rapid growth of distributed power architecture in space electronic systems [30]. Distributed power architectures replace multiple central power sources with a single bulk supply which is converted to the end-use voltages by dc/dc converters located at the point of need.

In the Sunsat distributed power system engineers power all the subsystems from a single +14 V bus and a central +12 V battery bank rather than from redundant wiring for

[5] Metal-oxide- semiconductor field-effect transistor

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Signal	Description
I_SP_+X	panel +X current
V_SP_+X	panel +X voltage
I_SP_-X	panel -X current
V_SP_-X	panel -X voltage
I_SP_+Y	panel +Y current
V_SP_+Y	panel +Y voltage
I_SP_-Y	panel -Y current
V_SP_-Y	panel -Y voltage
V_BATT	battery voltage
I_BATT	battery current
T_BATT	battery temperature
V_+14V_A	regulator A voltage
I_+14V_A	regulator A current
V_+14V_B	regulator B voltage
I_+14V_B	regulator B current
T_REG_A	regulator A temp
T_REG_B	regulator B temp

Table 2.3: Telemetry Signals

each voltage level throughout the satellite. In addition to saving weight and space, this architecture has made it easier to design and upgrade separate subsystems without making complete changes to overall system wiring. The use of converters also makes it easier to control the quality of power. Dc/dc converters can provide very close regulation of output voltages in spite of fluctuations in input voltage and load, an important feature for many sensitive subsystems.

The shift toward distributed power is also supported by fundamental changes in the kinds of components going into electronic systems. In the Sunsat project CMOS is the most common technology for the VLSI systems. With CMOS devices throughout the system, many boards require +5 V as well as +12 V. Many other voltages are also required. This means that more central power supplies are required.

CMOS presents electrical characteristics that complicate the design of central power systems. CMOS circuits use power during switching by charging and discharging parasitic capacitances, causing step function load changes. By placing the power supply at the point of need rather than in a low-voltage centralized power system, potential problems from distribution path inductances and backpanel and connector pin impedances are minimized.

In order to use centralized power systems, one should provide central supplies at all the different voltages needed, a central filtering and thermal management system, and interconnect wiring to the boards. For the distributed power version of the same system,

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one central +14 V nominal bulk supply is provided, and dc/dc converters supply the power levels needed at the appropriate voltages. When a board needs multiple voltages, dual or triple outputs are used, or more packages are used. In the distributed system, most of the converters are placed on a single board for which they are supplying power. The general principles of distributed power design are straightforward, but two significant problems must still be solved when power supplies are moved from a central location to the point of use.

The first of these is noise. When several switching power supplies are placed in the system, conducted and reflected ripple from the converters themselves needs to be measured and controlled.

The second is heat. When power supplies are compressed into small cases and mounted on logic boards, care should be taken that heat generated during the conversion process is dissipated.

The design of the power distribution system is done in [35]. An example of the distributed regulation is given in App. G. The voltage levels needed on the different trays are shown in the power flow diagram of Fig. A.1 in App. A. Table 2.4 is a summary of the power and voltage levels needed by the subsystems.

2.7 Power Management

The PV Generator integrated with the BU should support the load during the sunlight period. However, energy management may be called in if the demand is higher than the supply, which makes it necessary to drop some of the loads.

Some subsystems will require high power for a short time, eg. when pictures are taken. The powersystem has to be designed to support the base load and to provide enough power to handle these requirements.

Due to the nature of the power system it is necessary to take a comprehensive look at the generation and distribution of power and the possible energy management opportunities. In fact, the objective of energy management is to develop realistic schedules while reducing the power system size and storage requirements. This can be accomplished by minimizing the energy excess/shortage and the battery cycling, and by avoiding distribution overload. Energy management is designed to account for the many and unexpected changes in the load profile and new payloads onboard.

There are two goals behind selecting the appropriate energy management schedule. The first is to generate a valid schedule that can be satisfied according to resource requirements. The second is to reduce the energy excess/shortage and the battery cycling.

On some of the larger spacecraft, computer technologies are required to perform the load management functions. PICON (process intelligent control) [4] is a system tool

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Tray	Unit	V[V]	Tol[V]	I[A]	P[W]
ADCS		+5	4.5-5.5	0.02	0.1
		-5	0.5-5.5	0.1	0.5
		+12	10-18	0.167	2
		+15	0.5	0.033	2
		-15	0.5	0.133	0.5
RAM	RAM	+5	4.5-5.5	1	5
	Imager Digital	+5	4.5-5.5	0.4	2
OBC2	Onboard Computer 2	+5	4.5-5.5	0.5	2.5
		+12	0.5	0.04	0.5
OBC1,DSP	Onboard Computer 1	+5	4.5-5.5	0.5	2.5
		+12	0.5	0.04	0.5
	DSP	+5	4.5-5.5	0.5	2.5
		+12	0.5	0.04	0.5
Telecomm	Telecommand	+5	4-6	0.025	0.125
TTMS	Modems	+5	4-6	0.08	0.4
		+12	10-16	0.005	0.06
	Telemetry	+5	5-5	0.01	0.05
		+5	4.5-5.5	0.15	0.75
COMMS	UHF Rx	+5	4-8	0.03	0.15
	VHF Rx	+5	4-8	0.03	0.15
	UHF Tx	+5	4-8	0.03	0.15
	VHF Tx	+5	4-8	0.03	0.15
	L Band Rx	+12	10-15	0.05	0.6
	S Band Tx	+12	10-15	3.333	40
	30 MHz Power Amp	+12	10-15	1	12
	Synthesizers	+5	4.95-5.45	0.02	0.1
P & O	Power Control	+12	10-16	0.1	1
	Imager Analog	+5	0.1	0.9	4.5
		-5	0.1	0.3	1.5
		+15	0.5	0.9	13.5
		-15	0.5	0.6	9.0
	Reaction Wheels	+8	0.5	0.900	7.2
		-8	0.5	0.900	7.2

Table 2.4: Voltages and power needed by the satellite subsystems

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for the Space Station to provide complex, semi-intelligent control for many space station operations. In smaller spacecraft such as Sunsat, load management is performed by flight controllers and ground-based schedulers.

A second level of load management is included in hardware on the satellite trays as part of the power distribution system. The power supplies to the systems with the highest power consumption will be switched off after a maximum operating time via a power switch controlled by an RC timer. This means that if the telecommand or onboard computers fail to switch the system off, it will automatically switch off after a default time.

2.8 Schematic Diagrams

All the schematic diagrams of the SPS are given in App. G.

Fig. G.1 to Fig. G.4 show each solar panel consisting of 5 strings of 36 cells. Each string is connected separately to two pins of a socket for redundancy.

Fig. G.5 shows the interface connections between the different units of the power system. This diagram is important for the integration of the power system and the satellite.

Fig. G.6 shows the connectors of the main regulator unit (MRU).

Fig. G.7 shows how the different parts of the power system are connected. Note that each telecommand switch is made up by 4 switches, to prevent any short-circuit or open-circuit failures.

Fig. G.8 shows main regulator A and Fig. G.9 shows main regulator B. These regulators will work in parallel for redundancy. Regulator A uses panels +X and -X as source and regulator B uses panels +Y and -Y as source. This means that there will be no double maximum power point for any MPPT, because panels on opposite sides of the satellite cannot be irradiated on the same time.

Fig. G.10 and Fig. G.11 show the power supplies for the regulators in the MRU.

Fig. G.12 shows the battery unit of the satellite.

Fig. G.13 and Fig. G.14 show the telemetry sensors of the power system.

Fig. G.15 shows the ring bus which is the power interface between the power system and the rest of the satellite trays.

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2.9 Summary

In this chapter the Sunsat power system was discussed. A power simulation programme was neccessary for the sizing of power system components. It is also necessary for proper power management.

The PV Generator will consist of $GaAs$ solar cells, and the battery will consist of space qualified $NiCd$ cells. Power management will be done mainly by means of the onboard computers and the ground station via the telecommand subsystem.

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Chapter 3

Analysis and Synthesis of a Compound Converter

3.1 Introduction

In this chapter the development of the compound converter as nucleus of the MRU is detailed. A power conversion system always consists of two parts, i.e. the power electronics and the control. This chapter starts with an analysis of the power electronics. After it has been analysed, it will be synthesized in the following section. The control will then be analysed and synthesized.

The control system consists of two parts, namely the bus regulation part and the PV voltage regulation part. The analysis of the bus voltage regulation follows in Section 3.4, and it is designed in Section 3.5. The PV voltage regulation is analysed in Section 3.6 and designed in Section 3.7.

3.2 Analysis of the Compound Converter

The idealized circuit diagram of the compound converter is shown in Fig. 3.1. The load current consists of current supplied by the solar arrays and current supplied by the battery. Referring to Fig. 3.1, the load current can be written as follows:

$$I_O = n_1 I_{PV} - n_2 I_B \tag{3.1}$$

where $n_1 = \frac{N_{P1}}{N_S}$ and $n_2 = \frac{N_{P2}}{N_S}$. From Eq. 3.1 two states of the converter can be specified, namely when I_B is positive or zero and when it is negative.

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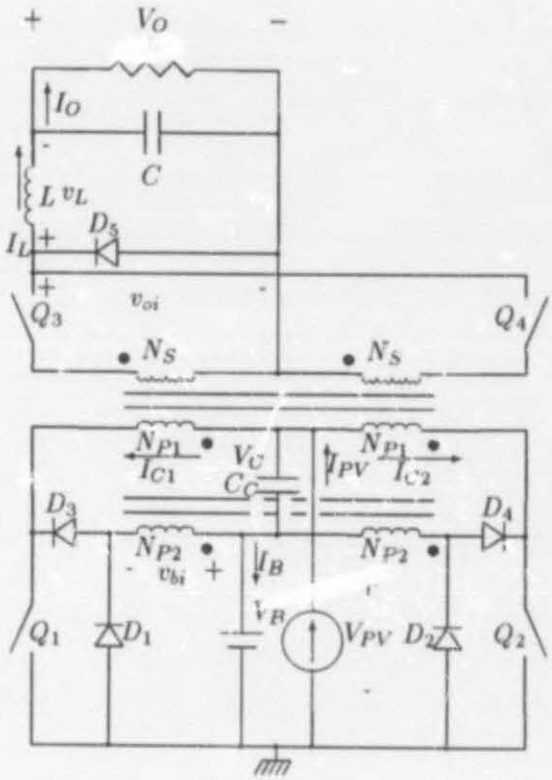

Figure 3.1: Circuit diagram of Compound Converter

3.2.1 Converter State 1 ($I_B \geq 0$)

I_B positive means that current flows into the battery (Fig. 3.1) when the current from the PV array exceeds the current required by the load (I_O).

From Eq. 3.1

$$I_B = \frac{n_1 I_{PV} - I_O}{n_2} \geq 0 \tag{3.2}$$

because $n_1 > n_2$. The compound converter is an arrangement of two push-pull converters working in parallel. The push-pull converter is an arrangement of two forward converters working in antiphase. Fig. 3.1 shows the basic compound configuration, and its associated waveforms for state 1 are shown in Fig. 3.2. It can be seen from these waveforms that, because of the presence of the two sets of switching transistors, the average current in each set is reduced to 50% over the equivalent forward converter. In the interval between transistor conductions, diode D_5 conducts, acting as flywheel diode.

In Fig. 3.1, when Q_1 and Q_3 is on during t_{on1} the result is $v_{oi} = \frac{N_S}{N_{P1}} V_{PV} = \frac{N_S}{N_{P2}} V_B$ in Fig. 3.2(a). Therefore, the voltage across the filter inductor is given as

$$v_L = \frac{N_S}{N_{P1}} V_{PV} - V_O \qquad 0 < t < t_{on1} \tag{3.3}$$

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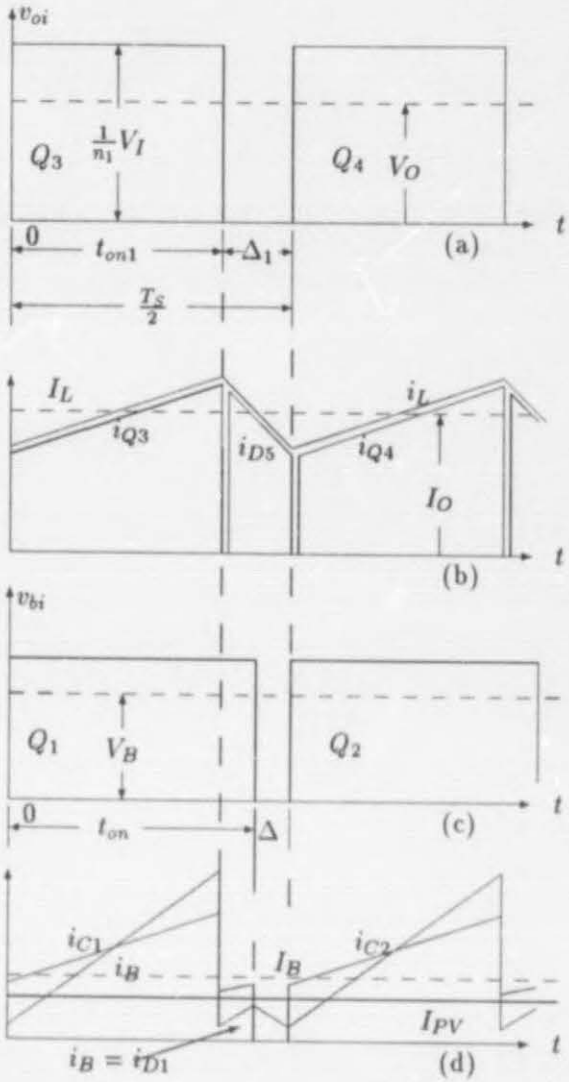

Figure 3.2: Waveforms of the compound converter in state 1

and i_L through Q_3 increases linearly as shown by Fig. 3.2(b).

During the interval Δ_1 when Q_3 and Q_4 are off, the inductor current is conducted by D_5 (Fig. 3.2(b)). Therefore, during $t_{on1} < t < (t_{on1} + \Delta_1)$:

$$v_L = -V_O \tag{3.4}$$

and

$$i_{D5} = i_L \tag{3.5}$$

The next half-cycle consists of t_{on1} (during which Q_2 is on), and the interval Δ_1. The waveforms repeat with a period $\frac{T_s}{2}$ and $t_{on1} + \Delta_1 + \frac{T_s}{2}$. Equating the time integral of

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the inductor voltage during one repetition period $\frac{T_S}{2}$ to zero using Eq. 3.3 and Eq. 3.4 yields:

$$V_O = \frac{2d_1 V_{PV}}{n_1} \tag{3.6}$$

where $d_1 = \frac{t_{on1}}{T_S}$ is the duty ratio of the switches Q_3 and Q_4 and the maximum value it can attain is 0.5. The average value of the v_{oi} waveform in Fig. 3.2(a) equals V_O.

In Fig. 3.1, when Q_1 is on during t_{on}, the result is $v_{bi} = \frac{N_S}{N_{P2}} V_{PV}$ in Fig. 3.2(c). Therefore, the voltage across the inductance to the battery (leakage inductance of transformer) is given as

$$v_{Lb} = \frac{N_{P2}}{N_{P1}} V_{PV} - V_B \qquad 0 < t < t_{on} \tag{3.7}$$

and i_B through D_1 increases linearly as shown by Fig. 3.2(d).

During the interval Δ when Q_1 and Q_2 are off, the inductor current is split equally between the two half-windings of N_{P2}. Therefore, during $t_{on} < t < (t_{on} + \Delta)$:

$$v_{Lb} = -V_B \tag{3.8}$$

and

$$i_{D1} = i_{Lb} \tag{3.9}$$

The next half-cycle consists of t_{on} (during which Q_2 is on), and the interval Δ. The waveforms repeat with a period of $\frac{T_S}{2}$ and $t_{on} + \Delta + \frac{T_S}{2}$. Equating the time integral of the inductor voltage during one repetition period $\frac{T_S}{2}$ to zero using Eq. 3.7 and Eq. 3.8 yields:

$$V_B = \frac{2dV_{PV}n_2}{n_1} \tag{3.10}$$

where $d = \frac{t_{on}}{T_S}$ is the duty ratio of the transistors Q_1 and Q_2 and where the maximum value it can attain is 0.5. The average value of v_{bi} waveform in Fig. 3.2(c) equals V_B.

The i_{PV} waveform (Fig. 3.2 (d)) is the sum of the currents supplied to the load and the battery by the PV generator, transformed by the n_1 and n_2 ratios respectively.

Antiparallel diodes over Q_1 and Q_2 are needed to provide a path for the current required, due to the leakage flux of the transformer.

Due to a slight and unavoidable difference in the switching times of the two transistors Q_1 and Q_2, there is always an imbalance between the peak values of the two switch currents. This imbalance can be eliminated by means of peak-current control of the converter, which will be discussed in Section 3.4.

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3.2.2 Converter State 2 ($I_B < 0$)

I_B negative means that current flows out of the battery when the current required by the load (I_O) exceeds the current from the PV array.

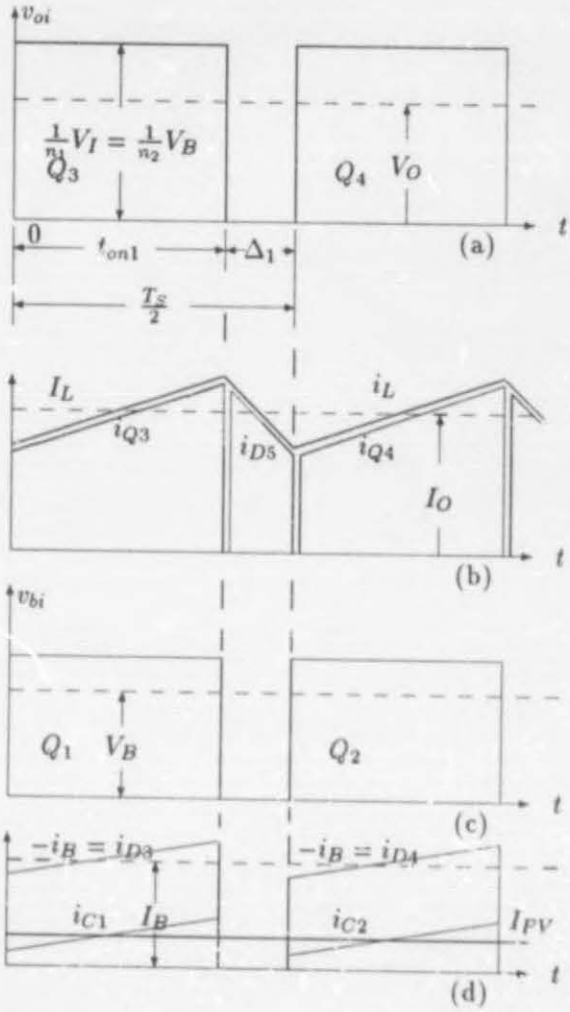

Figure 3.3: Waveforms of the compound converter in state 2

From (3.1)

$$I_B = \frac{n_1 I_{PV} - I_O}{n_2} < 0 \tag{3.11}$$

because $n_1 > n_2$.

In this circuit state the power delivered by the PV array is not enough for the load. As soon as the output voltage V_O drops, the voltage across N_S also drops, causing the voltage across N_{P2} to drop and the battery current I_B to reverse direction. The battery starts delivering current to the load. I_B now adds to the PV current I_{PV} through diodes D_3 and D_4.

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Description	Value
Load Voltage	$V_O = +14\ V$
Maximum Load Current	$I_{O,max} = 5\ A$
Output Voltage Riffle	$\Delta V_O = 0.05\ V$ or 10% (-40bB)
Minimum Battery Voltage	$V_{B,min} = +10\ V$
Maximum Battery Voltage	$V_{B,max} = +16\ V$
Minimum PV Voltage	$V_{PV,min} = 24\ V$
Maximum PV Voltage	$V_{PV,max} = 34\ V$

Table 3.1: Specifications for the Converter

The waveforms of this circuit state are shown in Fig. 3.3. The first part of the description of state 1 is also applicable to this state. It is obvious that the inductor current (Fig. 3.3(b)) is the sum of the currents from the solar array and the battery (Fig. 3.3(d)), transformed by the ratios n_1 and n_2 respectively.

3.3 Synthesis of the Compound Converter

This section represents the synthesis of the compound converter. The design specifications needed in designing the converter power electronics are listed in Table 3.1.

3.3.1 Inductor Design

The information required to build the inductor includes the inductance L, the peak current $I_{L,max}$, the maximum rms inductor current $I_{L,rms}$, and the switching frequency f_S.

The minimum inductor current is chosen as $I_{L,min} = 1\ A$ to ensure that the inductor operates in the continuous conduction mode during normal operation when the load needs 24 W. The peak inductor current is chosen as $I_{L,max} = 2.5\ A$ to realize an output current (average inductor current) of 1.75 A (Fig. 3.4(a)). If the inductor discharges, the voltage across it is equal to the output voltage, as discussed in the analysis of Section 3.2. Using this information from Fig. 3.4(a), it is evident that the slope of the discharging inductor is determined by the inductance. The inductance can therefore be calculated as follows:

$$i_L(t_2) - i_L(t_1) = \frac{1}{L}\int_{t_1}^{t_2} v_L\, dt \tag{3.12}$$

$$\Rightarrow -1.5 = \frac{1}{L}\int_{7\mu s}^{14.5\mu s} -14\, dt$$

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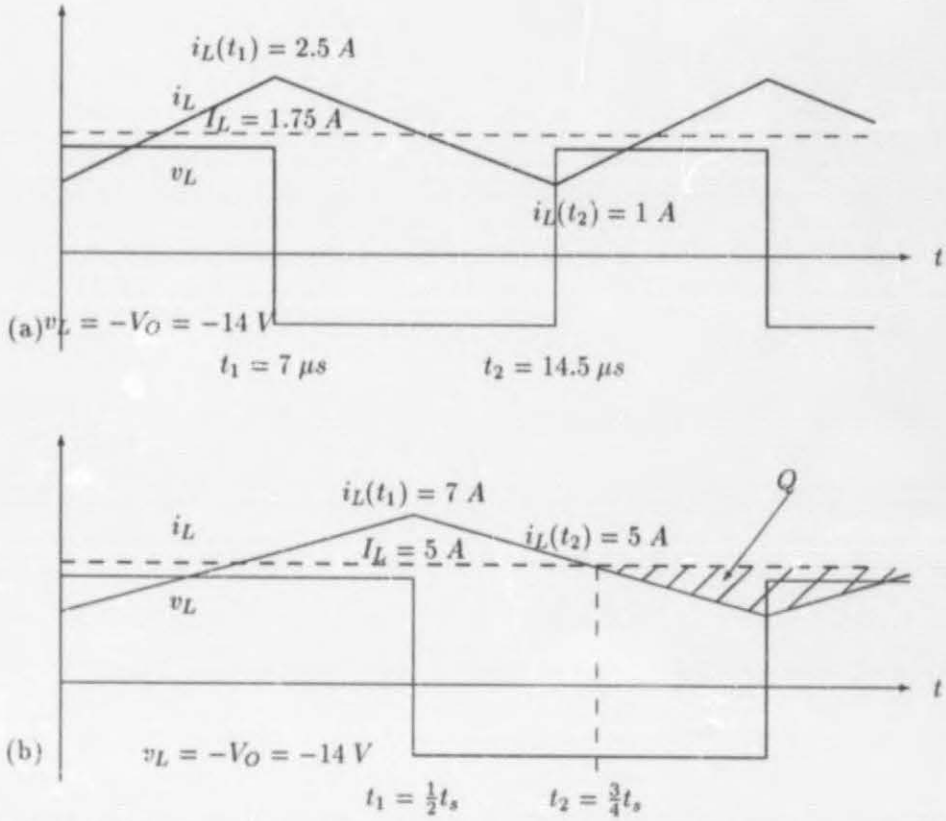

Figure 3.4: (a) Inductor current and voltage during minimum operation (b) Inductor current and voltage during maximum operation

$$\Rightarrow L \geq 70\ nH$$

The inductance is chosen as $L = 7\ \mu H$.

The maximum rms inductor current is equal to the maximum output current, or $I_{L,rms} = I_{O,max} = 5\ A$. In this state the duty cycle will be at a maximum . The compensation discussed in Section 3.4 limits the duty cycle to 50 %. Assuming that the inductance is constant, the maximum value of the inductor current can be obtained as follows, using Eq. 3.12 and Fig. 3.4(b):

$$i_L(t_1) = \frac{1}{L}\int_{t_1}^{t_2} v_L\ dt + i_L(t_2) \tag{3.13}$$

$$\Rightarrow I_{L,max} = i_L(t_1) = \frac{1}{7.10^{-6}}\int_{7.1.10^{-6}}^{10.7.10^{-6}} -14\ dt + 5 = 7\ A$$

All the values needed for designing the inductor are known and the parameters in Table 3.2 are obtained using the design procedure given in App. F.1.

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Description	Value
Core Shape	Potcore
Core Material	3B8
Core Size	P26/16
Number of turns	$n = 20$
Conducter diameter	$d = 1.25\ mm$
Air gap size	$g = 0.03\ mm$

Table 3.2: Inductor parameters

3.3.2 Transformer Design

The tranformer consists of three sets of windings, namely primary windings from the PV generator (N_{P1}), primary windings from the battery (N_{P2}) and secondary windings to the load (N_S).

From Eq. 3.6 the maximum turns ratio between the PV generator and the load is obtained as

$$n_1 < \frac{0.5 \times 28}{14} = 1 \tag{3.14}$$

where 0.5 is the maximum duty cycle for the load regulation.

From Eq. 3.10 the maximum turns ratio between the battery and the load is obtained as

$$n_2 < \frac{0.96 \times 10}{14} = 0.686 \tag{3.15}$$

where 0.96 is the maximum duty cycle.

The required design input information for finding the size of the transformer core is the peak primary rms voltage $V_{P,rms}$ and the peak primary rms current $I_{P,rms}$ of one set of primary windings, if the converter is operating at maximum load and the transformer operating frequency is $f_O = 35\ kHz$, because the transformer frequency of a push-pull converter is half the switching frequency. The primary input from the battery will be used, assuming that the PV generator does not supply any power.

The required information for finding the size of the conductors is the peak primary rms current $I_{P,rms}$ of both the primary windings and the turns ratios n_1 and n_2.

The peak secondary voltage is equal to $V_{I,max} = 16\ V$, because the on-voltage drop across the switches is small.

If the battery supplies all the power in the peak load condition, the rms current in one battery primary winding is

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Description	Value
Core Shape	Potcore
Core Material	3B8
Core Size	P30/19
Number of primary 2 turns	$N_{P2} = 3$
Number of primary 1 turns	$N_{P1} = 6$
Number of secondary turns	$N_S = 7$
Primary 2 conducter diameter	$d_{P2} = 0.6\ mm$
Primary 1 conducter diameter	$d_{P1} = 0.5\ mm$
Secondary conducter diameter	$d_S = 0.5\ mm$

Table 3.3: Transformer parameters

$$I_{P2,rms} = \frac{I_{S,rms}\frac{1}{n_2}}{2} = \frac{5 \times 1.5}{2} = 3.75\ A \tag{3.16}$$

If the PV generator supplies all the power in the peak load condition, rms current in one PV generator primary winding is

$$I_{P1,rms} = \frac{I_{S,rms}\frac{1}{n_1}}{2} = \frac{5 \times 1}{2} = 2.5\ A \tag{3.17}$$

because the rms secondary current of one winding is equal to half the rms inductor current. By using these values in the transformer design procedure of App. F.2, the transformer parameters in Table 3.3 are obtained.

3.3.3 Output Filter Capacitor

The shaded area in Fig. 3.4(b) represents the charge stored in the capacitor during maximum load. From the geometry of the current waveform, the charge is:

$$Q = \frac{T}{2}\frac{\Delta I_L}{2} = \frac{14.3.10^{-6}}{2} \times \frac{4}{2} = 14.3\ \mu C \tag{3.18}$$

The filter capacitor should be large enough to store and release this charge to prevent a voltage riffle (Δ) on the bus greater than 0.1 V. From the definition of capacitance:

$$C = \frac{Q}{\Delta V} = \frac{14.3.10^{-6}}{0.1} = 143\ \mu F \tag{3.19}$$

The filter capacitance must therefore be at least 143 μF with a voltage handling capability of at least 14 V.

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3.3.4 Switching Elements

The compound converter has two sets of controlled switches, namely the primary switches and the secondary switches.

The primary switches, Q_1 and Q_2 in Fig. 3.1 switch to keep the PV generator at its maximum power point. These switches are transistors. The basic design parameters in selecting the transistors are voltage blocking capability at turn-off and its current carrying capacity at turn-on. An important decision is whether to use bipolar transistors or MOSFETs. Each of these transistors offers distinct advantages over the other, the bipolar being less expensive, while the MOSFET offers circuit simplicity because of simpler drive circuits. It is important to note that the bipolar transistor has a limited working frequency cutoff, which is around 50 kHz, while the MOSFET may be used in switching frequencies up to 200 kHz. The logical choice, therefore, is MOSFETs, because the switching frequency is $f_S = 70\ kHz$.

In eclipse, Q_1 and Q_2 switch to deliver power to the load supplied by the battery. The current will be at a maximum in this state when the battery voltage is at its minimum value of $V_B = 10\ V$. Fig. 3.4(b) shows the peak inductor current as 7 A which is equal to the peak secondary current. The peak primary current from the battery will then be

$$I_{P2} = \frac{I_S}{n_2} = \frac{7}{0.686} = 10\ A \tag{3.20}$$

The peak current-handling capability of the switches must be well above 10 A in order to be prepared for radiation degradation. The maximum voltage across the switches will occur when the PV generator is at its maximum voltage, namely 31 V.

To minimize the losses, the on-resistance ($R_{DS,on}$) must be as low as possible. Such a MOSFET is the IRF540, with an on-resistance of $R_{DS,on} \approx 0.1\ \Omega$. It also has a maximum current and drain-source capability of 25 A and 100 V respectively, according to [23], which satisfies the requirements above.

The secondary switches, Q_3 and Q_4 in Fig. 3.1, switch to regulate the bus voltage at 14 V. The secondary side of the compound converter is similar to the secondary side of a push-pull regulator. To control the output voltage, the current through the rectifiers should be blocked with duty cycle d_1. To do this, the rectifiers (diodes) should be replaced by controllable switches (transistors). It is difficult, however, to drive transistors in these positions because the voltage levels at the input and output of the switches vary considerably. The antiparallel parasitic diodes of the MOSFETs cause further problems. The best solution is to leave the rectifying diodes where they are and to control the current flow with an extra p-channel MOSFET connected to the centre-tap of the secondary windings.

Fig. 3.4(b) shows the peak inductor current as 7 A, which is equal to the peak secondary current and to the current going through the MOSFET and the diodes.

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The diodes must also be able to switch easily at the switching frequency of 70 kHz. At this frequency, Schottky diodes are normally a better choice. The Schottky diode has a low forward voltage drop, even at high forward currents. As the junction temperature increases in a Schottky, the forward voltage drop becomes even lower. Reverse recovery time is negligible, because this device is a majority-carrier semiconductor, and therefore there is no minority-carrier storage charge to be removed during switching. Unfortunately there are two drawbacks associated with Schottky diodes, which make them unsuitable for the compound converter. First, their reverse blocking capability is low, and second, their higher reverse leakage current makes them more susceptible to thermal runaway than other diodes.

Fast-recovery diodes can switch fast and have high blocking voltage capabilities, but have the disadvantage of having relatively high forward voltage drops. The BYW29/150 fast-recovery diodes, with maximum current of 7.3 A and maximum blocking voltage of 150 V, are selected for the compound converter.

The maximum voltage across the control MOSFET is the maximum of $\frac{1}{n_2}V_{B,max}$ and $\frac{1}{n_1}V_{PV,max}$, which is 31 V. To minimize the losses, the on-resistance ($R_{DS,on}$) must be as low as possible. P-channel MOSFETs have higher on-resistances than n-channel MOSFETs. More than one MOSFET can be used in parallel, to reduce the resistance. A MOSFET with a relatively low on-resistance of $R_{DS,on} = 0.3\ \Omega$ and maximum current and drain-source voltage capabilities of 10 A and 60 V respectively, according to [23], is the IRF9530, which satisfies the requirements above.

Diodes D_1 and D_2 in Fig. 3.1 act as rectifiers when power is delivered to the battery. The maximum current to the battery occurs during maximum illumination and minimum load. The power to the battery then is $40\ W - 20\ W = 20\ W$. And if the battery is at minimum charge, the current is $\frac{20}{10} = 2\ A$.

In the compound converter, the antiparallel diodes are needed to provide a path for the current required, due to the leakage flux of the transformer.

3.3.5 Snubber Design

Capacitive Snubbers

Snubbers are needed in diode circuits to minimize overvoltages. These overvoltages occur in circuits because of the stray leakage inductance L_σ in series with the diode, and the snap-off of the diode reverse recovery current.

The secondary side of the converter without the control switch is shown in Fig. 3.5(a). When all the primary switches are off, one half of the output current flows through each diode. When a converter switch turns on, so that a positive voltage is applied across the primary side, the secondary side of the circuit can be represented by Fig. 3.5(b), where the current through D_1 will increase and that through D_2 will decrease. Consider

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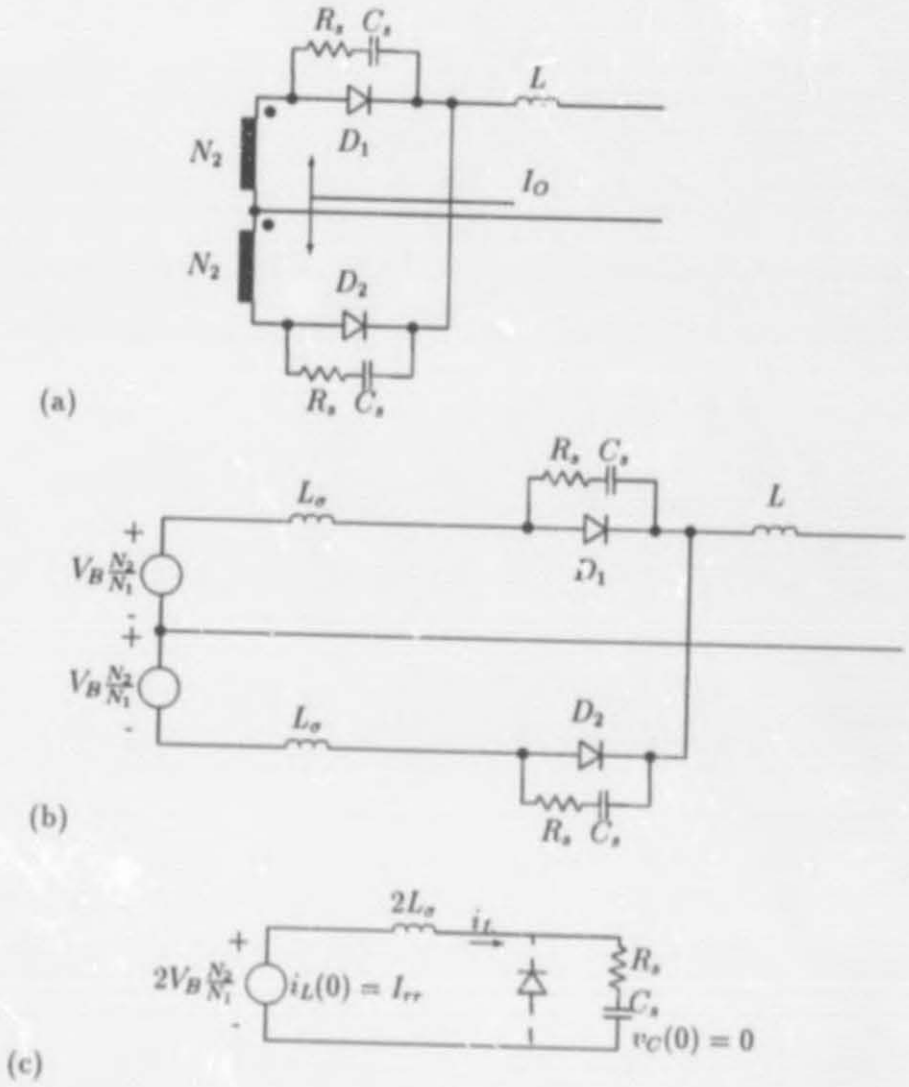

Figure 3.5: Secondary diodes with snubber

the instant at which the peak reverse recovery current I_{rr} snaps off in D_2 as the initial instant, and the equivalent circuit of Fig. 3.5(c) results. There should be a snubber across each diode in this circuit.

Treating the instant of diode snap-off at peak reverse recovery current I_{rr} as $t = 0$, the initial inductor current in the equivalent circuit of Fig. 3.5(c) is I_{rr} and the initial snubber capacitor voltage is zero. The current I_{rr} is calculated by knowing the reverse recovery time $t_{rr} = 35\ ns$ and $\frac{di}{dt} = 50\ A/\mu s$ from the data of the BYW29-150 in [33] as:

$$I_{rr} = \frac{di}{dt} t_{rr} = 50.10^6 \times 35.10^{-9} = 1.75\ A$$

To establish a baseline circuit, the snubber resistance R_s is assumed to be zero. The

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capacitor voltage (which is the negative of the diode voltage in the baseline circuit) can be obtained as follows: With the inductor current i_L and the capacitor voltage v_{C_s} as the state variables, the circuit equations are:

$$2L_\sigma \frac{di_L}{dt} + v_{C_s} = 2V_B \frac{N_S}{N_{P2}}$$

$$C_s \frac{dv_C}{dt} = i_L$$

The solution of v_{C_s} for $t \geq t_0$ is then:

$$v_{C_s}(t) = 2V_B \frac{N_S}{N_{P2}} - 2V_B \frac{N_S}{N_{P2}} cos\, \omega_0 t + I_{rr}\sqrt{\frac{L_\sigma}{C_s}} sin(\omega_0 t) \tag{3.21}$$

where

$$\omega_0 = \frac{1}{\sqrt{L_\sigma C_s}} \tag{3.22}$$

By introducing a baseline capacitance C_{base} given by

$$C_{base} = 2L_\sigma \left[\frac{I_{rr}}{2V_B \frac{N_S}{N_{P2}}}\right]^2 \tag{3.23}$$

it is possible to express Eq. 3.21 as

$$v_{C_s}(t) = 2V_B \frac{N_S}{N_{P2}} \left[1 - cos\, \omega_0 t + \sqrt{\frac{C_{base}}{C_s}} sin(\omega_0 t)\right] \tag{3.24}$$

By means of a time derivative the maximum value of v_{C_s} can be calculated as

$$V_{C_s,max} = 2V_B \frac{N_S}{N_{P2}} \left[1 + \sqrt{1 + \frac{C_{base}}{C_s}}\right] \tag{3.25}$$

In the snubber without resistance, the energy oscillates between the snubber capacitor and the inductance, causing large oscillations in the current and the voltage, which is undesirable.

If the diode snubber resistance R_s is included, these oscillations are dampened. According to [27] the optimal resistance is

$$R_s = \frac{2V_B \frac{N_S}{N_{P2}}}{I_{rr}} = \frac{2 \times 12 \times 7}{3 \times 1.75} = 32\ \Omega \tag{3.26}$$

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and the optimal capacitance is $C_s = C_{base}$. The baseline capacitance cannot be calculated without knowing L_σ. L_σ was found by setting $C_s = 47\ nF$ and measuring the oscillation frequency w_0. Knowing C_s and $\omega_0 = 4.10^6\ rad/s$, L_σ is found from Eq. 3.22 as $1.32\ \mu H$. The snubber capacitance is then calculated from Eq. 3.23

$$C_s = 2 \times 1.32.10^{-6} \left[\frac{1.75 \times 3}{2 \times 12 \times 7} \right]^2 = 2.6\ nF$$

The energy loss in the resistor R_s is given by [27] as

$$\begin{aligned} W_R &= \frac{1}{2} L_\sigma I_{rr}^2 + \frac{1}{2} C_s \left(2V_B \frac{N_S}{N_{P2}} \right)^2 \\ &= \frac{1}{2} 1.32.10^{-6} 1.75^2 + \frac{1}{2} 2.6.10^{-9} \left(24 \frac{7}{3} \right)^2 = 6\ \mu W \end{aligned} \tag{3.27}$$

3.3.6 Gate drive circuitry

Only two external components, a resistor and Schottky diode, are required to insure proper operation of the PWM, while delivering the high current drive pulses.

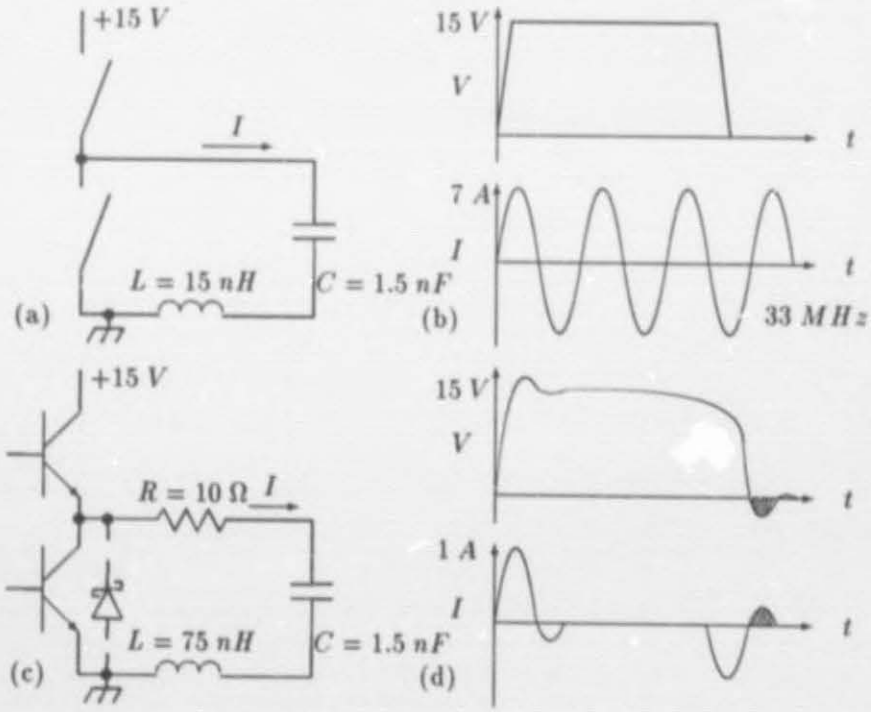

Figure 3.6: Drive circuit

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Typical gate-to-source input characteristics of most FETs reveal approximately 1500 pF of capacitance in series with 15 nH of source inductance. At first, the series gate current limiting resistor will not be used to exemplify its necessity. Also, the totem pole transistors are replaced with ideal (lossless) switches. A $\frac{dv}{dt}$ rate of 0.5 V per nanosecond is typical for the UC1846 and will be incorporated. Assuming that there are no external circuit parasitics of R, L or C, the PWM; therefore is driving an L-C resonant tank with no attenuation (Fig. 3.6(b)). The driving function is a 15 V pulse derived from the auxiliary supply voltage. The resulting current waveform is shown in Fig. 3.6(b), having a peak current of approximately 7 A at a frequency of $\frac{1}{2\pi\sqrt{LC}} = 33\ MHz$. In a practical application, the transistors and other circuit parameters, fortunately, are less than ideal. The results above are unlikely to happen in most designs; however, they will occur at a reduced magnitude, if not prevented altogether. Limiting the peak current through the IC is accomplished by placing a resistor between the totem-pole output and the gate of the MOSFET. The value is determined by dividing the totem-pole collector voltage 15 V by the peak current rating of the IC's totem-pole. Without this resistor, the peak-current is limited only by the $\frac{dv}{dt}$ rate of the totem-pole and the FET gate capacitance. For this example, a collector supply voltage of 15 V is used, with an estimated totem-pole saturation voltage of approximately 2 V. Limiting the peak gate-current to 1 A maximum requires a resistor of 10 Ω. Placing the resistor in series with the collector and the auxiliary voltage source will only limit the turn-on current. Therefore it must be placed between the PWM and gate, to limit both turn-on and turn-off currents.

Actual circuit parasitics also play a key role in the drive behavior. The inductance of the FET source lead (10 nH) is generally small in comparison with the layout inductance. To model this network, an approximation of 10 nH/cm PCB trace can be used. In addition, the inductance between the pins of the IC and the die can be rounded off to 10 nH per pin. It now becomes apparent that circuit inductances can quickly add up to 100 nH, even with the best of PCB layouts. An estimate of 60 nH was used to simulate the PC board. The equivalent circuit is shown in Fig. 3.6(c). A 15 V pulse is applied to the network using 10 Ω as the current limiting resistance. The resulting voltage and current waveforms at the totem-pole output are shown in Fig. 3.6(d). The shaded areas of each graph are of particular interest. During this time, the lower totem-pole transistor is saturated. The voltage of its collector is negative with respect to its emitter (ground). In addition, a positive output current is being supplied to the RLC network through the collector of this saturated NPN transistor. The IC specifications indicate that neither of these two conditions are tolerable. One approach is to increase the limiting resistance, in order to change the response from underdampened to slightly overdampened. This will occur when:

$$R_{gate} \geq 2\sqrt{LC} \tag{3.28}$$

Unfortunately, this also reduces the peak drive current, thus increasing the switching times of the FETs, which is undesirable. The alternate solution is to limit the peak current, and to alter the circuit to accept the underdampened network. The use of a Schottky diode from the PWM output to ground will correct both situations. Being connected with the anode to ground and the cathode to the output, it will prevent the output voltage from going excessively below ground, and will also provide a current path.

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To be effective, the diode selected should have a forward voltage drop of less than 0.3 V at 200 mA. The 3 A 1N5822 diode has a voltage drop of 0.15 V at 200 mA, as shown by the graphs in [33], and is used in all the driving circuits. The diode will conduct during the shaded part of the curve shown in Fig. 3.6(d) when the voltage goes negative and the current is positive. The current is allowed to circulate as long as it does not adversely affect the IC performance. Placing the diode as close to the PWM generator as possible will enhance circuit performance.

3.3.7 Selection of Capacitors

In power electronics, basically three types of capacitors are used: electrolytic, metallized polypropylene and ceramic.

Electrolytic Capacitors

Aluminium electrolytic capacitors offer a large capacitance per unit volume and are polarized. The large capacitance is due to the aluminium foil connected to the positive terminal being etched in such a way that its surface is porous like a sponge. This results in an increase in its surface area by as much as a factor of 100 compared to its original unetched area. On this etched foil, an insulating layer of aluminium oxide is formed electrochemically. The negative terminal of the capacitor is connected to another aluminium foil which is in electrical contact with the liquid electrolyte, which is an electrically conducting material.

Because of the resistance of the electrolyte, these capacitors have a significant equivalent series resistance (ESR). These capacitors should not be used at temperatures below the specified minimum temperature, since the tendency of the electrolyte to crystallize results in a larger resistance. The ESR in the output filter capacitors must be low, to minimize the ripple in the output voltage.

The capacitor package or can is sealed at the top with an insulating layer that surrounds the electrical terminals. The rate of evaporation of the electrolyte through the seal increases significantly with rising temperature. Therefore, the capacitor lifetime decreases significantly with rising temperature. It should be noted that the electrolytic capacitors have by far the shortest lifetime of any element, active or passive, used in power electronic converters. The temperature within the capacitor depends on the power loss. This loss increases with the rms current because of ohmic losses in the capacitor. For a given current, the ripple voltage across the dielectric decreases with increasing frequency. Therefore, the dielectric power loss decreases with increasing frequency. For a given lifetime of the capacitor, its current-carrying capacity increases with increasing frequency and decreasing ambient temperature.

The use of tantalum as the metal for an electrolytic capacitor allows for a very different form of construction, in which the oxide film is stable and able to withstand reversals

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of voltage [32]. Tantalum capacitors can be used without a steady polarising voltage, they can be run with the electrolyte virtually dry, and they generally havebetter characteristics than the aluminium type of electrolytic capacitor. Experience with the use of tantalum has led to the development of dry electrolytes and very reliable military standard electrolytes. These capacitors will be used as filter capacitors for the converter.

Metallized Polypropylene Capacitors and Ceramic Capacitors

In the snubbers capacitors must handle large currents, but the capacitance value required is small. Metallized polypropylene capacitors are a good choice for such applications because of a very small loss coefficient of the polypropylene dielectric material. The dielectric losses are proportional to the square of the voltage and frequency. Since the voltage across the dielectric is proportional to the current and inversely proportional to the frequency, the dielectric power loss is proportional to the frequency. Therefore, for a specified temperature, the current-handling capacity increases slightly with frequency.

Ceramic capacitors have extremely low series inductance.

3.3.8 Resistors

At rated power, the temperature of a resistor is in the range of 300°- 400°C. To avoid such high temperatures, the power loss in the resistors is limited to approximately half its rated power.

3.3.9 Managing Thermal Dissipation

Heat dissipation is a problem in implementing power electronic components in space. Since no converter is 100% efficient, some of the input power converted is released as heat, which must be removed in order to prevent excessive internal temperatures.

The heat producing elements are placed in close thermal contact with a metal heat conducting surface on the bottom or baseplate of the case, as shown in Fig. D.2. It is important to prevent that the temperature of the power handling components becomes considerably higher than the case temperature. When parts are subjected to overtemperature, operation may become degraded, reliability is impaired and component life is shortened.

A thermal path must be provided, which can conduct internally generated heat to the outside.

The first step in designing a heat sink or thermal management system is to find the power dissipated in the converter. This value is determined by subtracting the power delivered to the load from the total power supplied to the converter. Any power that is

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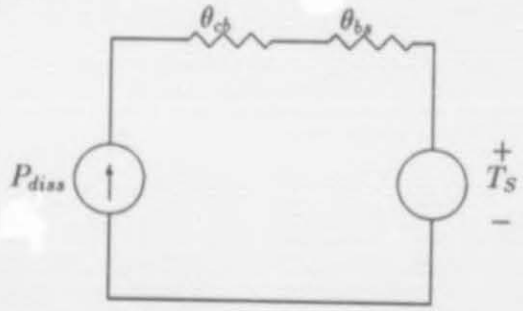
not delivered to the load ends up as heat in the converter, and must be removed. This value may be calculated as follows:

$$\begin{aligned} P_{diss} &= \frac{P_{out}}{efficiency} - P_{out} \\ &= \frac{140}{0.8} - 140 = 35\ W \end{aligned} \tag{3.29}$$

Heat energy is transferred from regions of high temperature to regions of low temperature via three basic mechanisms:

- Radiation: Electromagnetic transfer of heat between masses at different temperatures
- Conduction: Transfer of heat through a solid medium
- Convection: Transfer of heat through the medium of a fluid – typically air

While convection will be the dominant heat transfer mechanism in most applications, the other two mechanisms are the only two active in space. Consideration is given only to radiation and conduction.



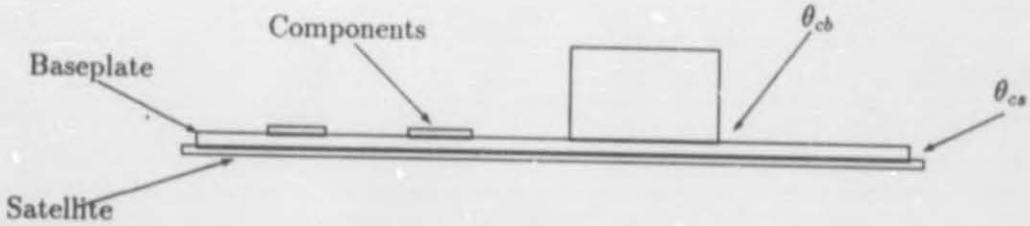


Figure 3.7: Baseplate attached to satellite bottom

Radiant heat transfer occurs continuously between objects at different temperatures which are exposed to each other. The net effect on the temperature of an individual part is dependent on many factors:

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- Its temperature relative to other parts
- Relative orientations of the parts
- Surface finishes
- Spacings

The difficulty in quantifying many of these factors, combined with the universal presence of radiant energy exchange, makes calculation of radiational temperature effects both a complex and generally imprecise task.

Heat will be conducted from the component into the baseplate into an attached heatsink. Heat conducted across the interfaces between the component and the baseplate, and the baseplate and the heatsink, will result in a temperature drop, which must be controlled. As shown in Fig. 3.7, the interfaces can be modelled as thermal resistances in series with the dissipated power flow. The component temperature will be the sum of the temperature rise in the interfaces and the temperature of the heatsink to which the baseplate is attached. If not controlled, the temperature rise across a surface interface can be significant . The areas of the interfaces are made as large as possible and as thin as possible, and a thermal compound should be used to fill surface irregularities.

The MRU will be situated on the bottom tray of the satellite, as shown in Fig. C.1 of App. C. This side will always be directed towards the earth, and away from the sun, in the shadow of the satellite. The temperature of the outside surface will be below $-10°C$. The satellite aluminium body is therefore a sufficient heat sink.

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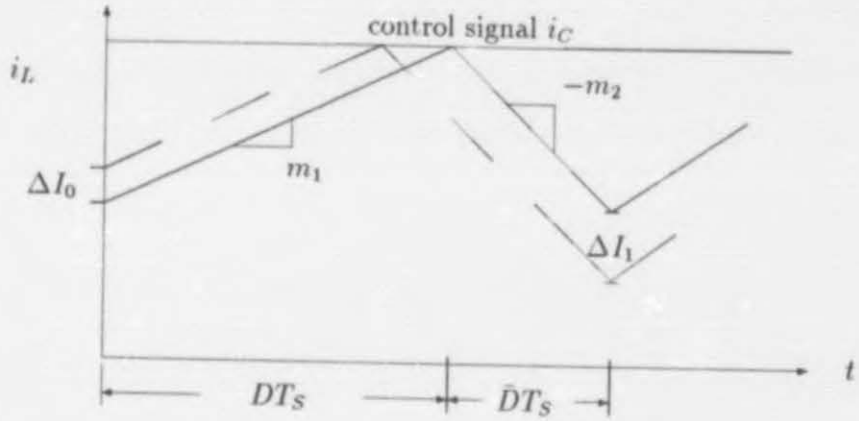

Figure 3.8: Propagation of perturbation in inductor current

3.4 Analysis of the bus voltage regulation

The control system measures changes in inductor current which control the output voltage instantaneously (peak-current control). Peak-current control has several advantages over the conventional duty-ratio scheme:

- Since the switch is turned off when its current reaches the control signal level, failures due to excessive switch current can be prevented simply by limiting the maximum value of the control signal.
- The peak-current control, relative to the conventional scheme, effectively removes one pole from the loop gain, simplifying the design of the feedback network.
- Peak current sensing will automatically provide flux balancing, thereby eliminating the need for complex balance schemes in the push-pull family.

In order to design the control system, the first objective is to obtain the equivalent small-signal circuit model of the converter, which represents both the input and output properties, and which can be embedded in the model of the complete regulator, so that the overall dynamic properties and stability can not only be analyzed but also designed.

A fixed-frequency peak-current converter is subject to oscillation. The second objective is to develop design techniques for eliminating this potential instability.

3.4.1 Peak-current control Instability

As mentioned above, a peak-current converter is subject to instability [12]. The cause of the problem lies in the fact that the peak-current control scheme constitutes an internal feedback loop (the level of the inductor current determines when the switch is turned

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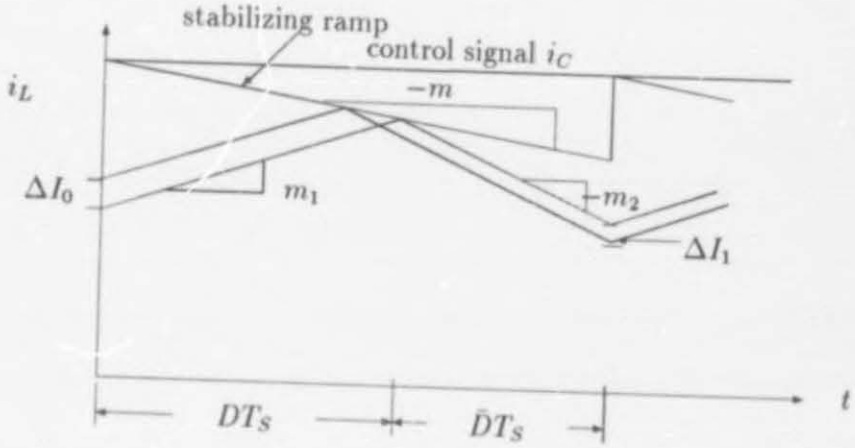

Figure 3.9: Propagation of a perturbation in presence of ramp

off). It is found that the oscillation generally occurs when the total duty ratio exceeds 0.5.

The effect can be explained with the help of the waveforms in Fig. 3.8, which is a straight line plot of the inductor current that flows through the power switch when it is on. The control signal is also plotted.

Suppose the inductor has a rising slope of m_1 and a falling slope of $-m_2$ in steady state. Clearly, since the steady state waveform is periodic,

$$\frac{m_2}{m_1} = \frac{D}{\bar{D}} \tag{3.30}$$

where D is the duty ratio and $\bar{D} = 1 - D$. If there is a perturbation, relative to the steady state, of ΔI_0 in the inductor current in the beginning of a period, the waveforms show that after one cycle the error will have become

$$\Delta I_1 = -\left(\frac{m_2}{m_1}\right)\Delta I_0 = -\left(\frac{D}{\bar{D}}\right)\Delta I_0 \tag{3.31}$$

Therefore, after n cycles the perturbation will be

$$\Delta I_n = -\left(\frac{D}{\bar{D}}\right)^n \Delta I_0 \tag{3.32}$$

Apparently, the steady state is not a stable solution if the duty ratio is greater than 0.5.

This potential instability can be illiminated by the addition of a suitable cyclic artificial ramp to either the switch current waveform or the control signal. Waveforms for this modification are shown in Fig. 3.9, in which the control signal is given a cyclic falling

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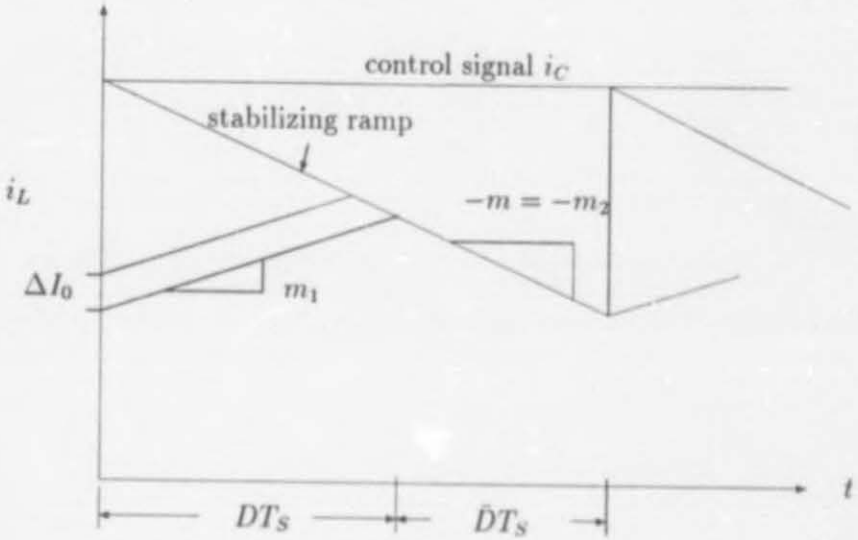

Figure 3.10: Elimination of perturbation

slope $-m$. An argument similar to that used previously shows that now a perturbation ΔI_0 is carried into

$$\Delta I_n = -\left(\frac{m_2 - m}{m_1 + m}\right)^n \Delta I_0 \tag{3.33}$$

after n cycles. A suitable choice of the ramp slope $-m$ can therefore cause this perturbation to die out, even if the duty ratio is greater than 0.5. In particular, if m is chosen to be equal to m_2 (the magnitude of the falling current slope), Eq. 3.33 shows that any perturbation of the inductor current will disappear at the end of one cycle, therefore guaranteeing inner loop stability and simultaneously providing the fastest possible transient response of the current, as shown in Fig. 3.10.

Note that, for duty ratios less than 0.5, while the system will be stable in the absence of an artificial ramp, the best possible transient response is only attained if a ramp of the correct slope is used. Therefore, this compensation scheme benefits system performance for any operation condition, not just cases where an artificial ramp is required to avoid instability. The same results hold if an artificial ramp of slope m is added to the inductor current instead of the control signal.

3.4.2 State-space Model of the Converter

The secondary circuit of the compound converter has two operating states, namely when one diode is on or when both are off. The equivalent circuits for the two conduction modes are given in Fig. 3.11. In this circuit, it is assumed that all reactive components

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are ideal.

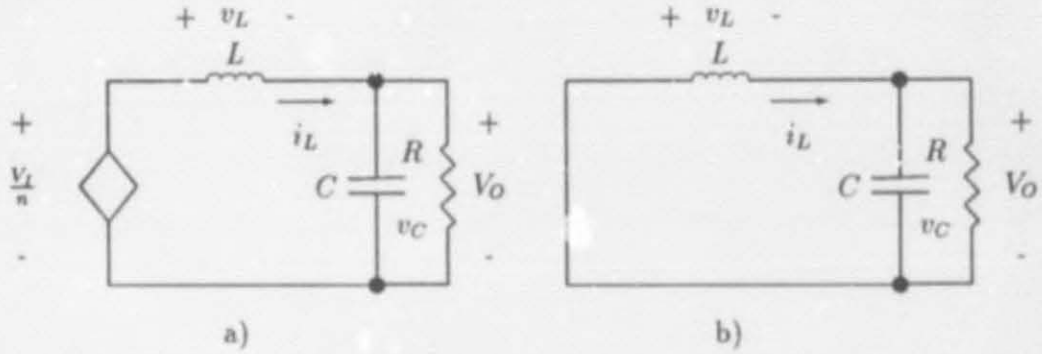

Figure 3.11: Equivalent circuit when (a) one of the transistors is turned on and (b) both are turned off.

The objective is to formulate a small-signal model for the converter from which the transient and stability characteristics of a closed-loop system can be investigated [27].

State-Variable Description of each Circuit State

In the converter operating in continuous-conduction mode, there are two circuit states: One state corresponds to when a diode is on and the other to when both diodes are off (shown in Fig. 3.11). During each circuit state, the linear circuit is described by means of the state-variable vector $\mathbf{x}$, consisting of the inductor current and the capacitor voltage.

$$\mathbf{x} = \begin{bmatrix} i_L \\ v_C \end{bmatrix} \tag{3.34}$$

During each circuit state, the following holds:

$$\dot{\mathbf{x}} = \mathbf{A_1}\mathbf{x} + \mathbf{B_1}v_I \tag{3.35}$$

during t_{on}, and

$$\dot{\mathbf{x}} = \mathbf{A_2}\mathbf{x} + \mathbf{B_2}v_I \tag{3.36}$$

during Δ, where $\mathbf{A_1}$ and $\mathbf{A_2}$ are state matrices and $\mathbf{B_1}$ and $\mathbf{B_2}$ are vectors.

The output v_O can be described in terms of their state variables alone, as

$$v_O = \mathbf{C_1}\mathbf{x} \tag{3.37}$$

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during t_{on}, and

$$v_O = \mathbf{C_2 x} \tag{3.38}$$

during Δ, where $\mathbf{C_1}$ and $\mathbf{C_2}$ are transposed vectors.

The state equations for the two circuit modes depicted in Fig. 3.11 (a) and (b) are:

$$\frac{di_L}{dt} = -\frac{1}{L}v_C + \frac{1}{nL}v_I \tag{3.39}$$

$$\frac{dv_C}{dt} = \frac{1}{C}i_L + \frac{-1}{RC}v_C \tag{3.40}$$

$$v_O = v_C \tag{3.41}$$

for t_{on} and

$$\frac{di_L}{dt} = -\frac{1}{nL}v_C \tag{3.42}$$

$$\frac{dv_C}{dt} = \frac{1}{C}i_L + \frac{-1}{RC}v_C \tag{3.43}$$

$$v_O = v_C \tag{3.44}$$

for Δ. Then:

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_C}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \times \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{nL} \\ 0 \end{bmatrix} v_I \tag{3.45}$$

and

$$v_O = \begin{bmatrix} 0 & 1 \end{bmatrix} \times \begin{bmatrix} i_L \\ v_C \end{bmatrix} \tag{3.46}$$

during t_{on}, and

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_C}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \times \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_I \tag{3.47}$$

and

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$$v_O = \begin{bmatrix} 0 & 1 \end{bmatrix} \times \begin{bmatrix} i_L \\ v_C \end{bmatrix} \tag{3.48}$$

during Δ.

Therefore

$$\mathbf{A_1} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \tag{3.49}$$

and

$$\mathbf{A_2} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \tag{3.50}$$

and

$$\mathbf{B_1} = \begin{bmatrix} \frac{1}{nL} \\ 0 \end{bmatrix} \tag{3.51}$$

and

$$\mathbf{B_2} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{3.52}$$

and

$$\mathbf{C_1} = \begin{bmatrix} 0 & 1 \end{bmatrix} \tag{3.53}$$

and

$$\mathbf{C_2} = \begin{bmatrix} 0 & 1 \end{bmatrix} \tag{3.54}$$

result.

Averaging the State-variable description

To produce an average description of the circuit over the switching period, the equations corresponding to the two foregoing states are time weighted and averaged, resulting in the following equations:

$$\dot{\mathbf{x}} = [\mathbf{A_1}d + \mathbf{A_2}(1-d)]\mathbf{x} + [\mathbf{B_1}d + \mathbf{B_2}(1-d)]v_I \tag{3.55}$$

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and

$$v_O = [\mathbf{B_1}d + \mathbf{B_2}(1-d)]\mathbf{x} \tag{3.56}$$

Introducing small ac perturbations and separation into ac and dc components

Small ac perturbations, represented by "~", are introduced in the dc steady-state quantities, which are represented by the uppercase letters. Therefore

$$\mathbf{x} = \mathbf{X} + \tilde{\mathbf{x}} \tag{3.57}$$

$$v_O = V_O + \tilde{v}_O \tag{3.58}$$

$$d = D + \tilde{d} \tag{3.59}$$

and

$$v_I = V_I + \tilde{v}_I \tag{3.60}$$

By using Eqq. 3.57 through 3.60 into Eq. 3.55 and recognizing that in steady state, $\dot{\mathbf{X}} = 0$,

$$\dot{\tilde{\mathbf{x}}} = \mathbf{AX} + \mathbf{B}V_I + \mathbf{A}\tilde{\mathbf{x}} + \mathbf{B}\tilde{v}_I + [(\mathbf{A_1} - \mathbf{A_2})\mathbf{X} + (\mathbf{B_1} - \mathbf{B_2})V_I]\,\tilde{d} \tag{3.61}$$

results, where terms containing products of $\tilde{\mathbf{x}}$ and $\tilde{d}$ are neglected and

$$\mathbf{A} = \mathbf{A_1}D + \mathbf{A_2}(1-D) \tag{3.62}$$

and

$$\mathbf{B} = \mathbf{B_1}D + \mathbf{B_2}(1-D) \tag{3.63}$$

The steady state equation is obtained from Eq. 3.61 by setting all the time derivatives and the perturbation terms to zero. Therefore the steady state equation is

$$\mathbf{AX} + \mathbf{B}V_I = 0 \tag{3.64}$$

Placed into Eq. 3.61, this results in

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$$\dot{\tilde{\mathbf{x}}} = \mathbf{A}\tilde{\mathbf{x}} + \mathbf{B}\tilde{v}_I + [(\mathbf{A_1} - \mathbf{A_2})\mathbf{X} + (\mathbf{B_1} - \mathbf{B_2})V_I]\,\tilde{d} \tag{3.65}$$

Similarly, using Eqq. 3.57 through 3.64 into Eq. 3.56 results in

$$V_O + \tilde{v}_O = \mathbf{CX} + \mathbf{C}\tilde{\mathbf{x}} + [(\mathbf{C_1} - \mathbf{C_2})\mathbf{X}]\,\tilde{d} \tag{3.66}$$

where

$$\mathbf{C} = \mathbf{C_1}D + \mathbf{C_2}(1 - D) \tag{3.67}$$

In Eq. 3.66, the steady state output voltage is

$$V_O = \mathbf{CX} \tag{3.68}$$

and therefore

$$\tilde{v}_O = \mathbf{C}\tilde{\mathbf{x}} + [(\mathbf{C_1} - \mathbf{C_2})\mathbf{X}]\,\tilde{d} \tag{3.69}$$

Using Eqq. 3.64 and 3.68, the steady state dc voltage transfer function is:

$$\frac{V_O}{V_I} = -\mathbf{CA}^{-1}\mathbf{B} \tag{3.70}$$

Transformation of the ac equations into the frequency domain

Eqq. 3.65 and 3.69 consist of the ac perturbations. Using Laplace transformation in Eq. 3.65

$$s\tilde{\mathbf{x}}(\mathbf{s}) = \mathbf{A}\tilde{\mathbf{x}}(\mathbf{s}) + \mathbf{B}\tilde{v}_I(s) + [(\mathbf{A_1} - \mathbf{A_2})\mathbf{X} + (\mathbf{B_1} - \mathbf{B_2})V_I]\,\tilde{d}(s) \tag{3.71}$$

or

$$\tilde{\mathbf{x}}(\mathbf{s}) = [s\mathbf{I} - \mathbf{A}]^{-1} \times [(\mathbf{A_1} - \mathbf{A_2})\mathbf{X} + (\mathbf{B_1} - \mathbf{B_2})V_I]\,\tilde{d}(s) + [s\mathbf{I} - \mathbf{A}]^{-1} \times \mathbf{B}\tilde{v}_I(s) \tag{3.72}$$

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3.4.3 Extension of the State-space Method for peak-current mode

State-space average Eq. 3.65 was developed to facilitate the design of the feedback network for the switching regulator. In the conventional single-state feedback approach, duty ratio variations are related to variations in the output voltage by a compensation network (Fig. 3.12).

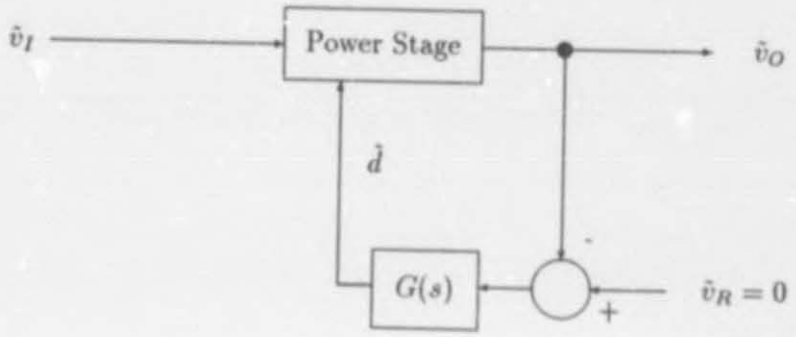

Figure 3.12: Small-signal block diagram of duty ratio mode

$$\tilde{d}(s) = -G(s)\tilde{v}_O(s) \qquad \tilde{v}_R = 0 \tag{3.73}$$

From Eq. 3.71, the transfer function characterizing the forward path from the duty ratio through the power stage to the output voltage can be found:

$$\tilde{v}_O(s) = F(s)\tilde{d}(s) \tag{3.74}$$

Then the product $F(s)G(s)$ is the loop gain of the regulator, and a Bode plot analysis of this loop gain allows determination of $G(s)$, so that stability and large system bandwidth are simultaneously achieved.

Peak-current control is clearly different from this conventional single-state approach, since both the output voltage and the inductor current are directly involved in determination of the duty ratio.

In peak-current control the current feedback loop can be specified independently of regulator feedback. Hence, only the voltage feedback compensation $G(s)$ is to be determined. Therefore, if the previously designed current loop is absorbed into the forward converter path, as in Fig. 3.13, the small-signal properties of this new system are described by a linear model, independent of the regulator feedback compensation still to be chosen, with inputs $\tilde{v}_I$ and $\tilde{i}_C$. Note that only a single, simple feedback loop is evident, the other more complicated path now being an intrinsic part of the converter model. With such a model, determination of the compensation $G(s)$ is accomplished by the same simple

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single-state feedback analysis as that described at the beginning of this section for the duty ratio mode, with $\tilde{i}_C$ taking the place of $\tilde{d}$.

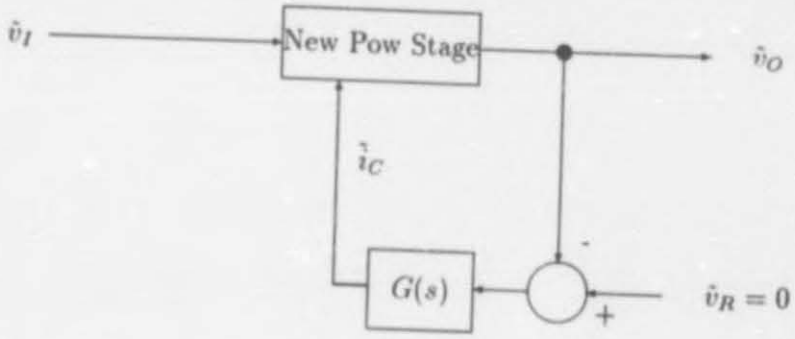

Figure 3.13: Small-signal block diagram with peak-current control

The development of the desired extension of the modelling technique is now undertaken.

The peak-current control in Fig. 3.13 can be described by a set of linear differential equations in the following form:

$$s\tilde{\mathbf{x}} = \mathbf{a_2}\tilde{\mathbf{x}} + \mathbf{b_2}\tilde{v}_I + \mathbf{c_2}\tilde{i}_C \tag{3.75}$$

with $\tilde{v}_I$ and $\tilde{i}_C$ as the input to the system. Laplace transformations are used throughout this section. The problem is to determine $\mathbf{a_2}$, $\mathbf{b_2}$ and $\mathbf{c_2}$. Once they are known, an equivalent circuit model can be inferred from Eq. 3.75.

Two pieces of information are used in arriving at the peak-current control state equation:

1. The state-space averaged Eq. 3.71 for the frequency domain:

$$s\tilde{\mathbf{x}} = \mathbf{a_1}\tilde{\mathbf{x}} + \mathbf{b_1}\tilde{v}_I + \mathbf{c_1}\tilde{d} \tag{3.76}$$

   where

$$\mathbf{a_1} = \mathbf{A} \tag{3.77}$$

$$\mathbf{b_1} = \mathbf{B} \tag{3.78}$$

$$\mathbf{c_1} = [(\mathbf{A_1} - \mathbf{A_2})\mathbf{X} + (\mathbf{B_1} - \mathbf{B_2})V_I] \tag{3.79}$$

2. A description of the effects of the current feedback loop, in the form of a control constraint, relating variations $\tilde{i}_L$ in the peak current to control variations $\tilde{i}_C$, and

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possibly also to variations in other states $\tilde{\mathbf{x}}$, the input voltage $\tilde{v}_I$ and duty ratio $\tilde{d}$ results in:

$$\tilde{i}_L = f_1(\tilde{i}_C, \tilde{x}, \tilde{v}_I, \tilde{d}) \tag{3.80}$$

These two pieces of information are combined on the basis of the intuitive notion that the inductor current is changed in status from an unknown state to a driving term, while the duty ratio modulation loses its importance as an independent input. In a mathematical expression of this idea, the state equation for $\tilde{i}_L$ from the state-space averaged Eq. 3.76 is used to solve for $\tilde{d}$, which results in a duty ratio expression:

$$\tilde{d} = g(\tilde{x}, \tilde{v}_I, \tilde{i}_L) \tag{3.81}$$

$$\tilde{d} = \frac{nL}{V_I}(s\tilde{i}_L + \frac{\tilde{v}_C}{L} - \frac{D}{nL}\tilde{v}_I) \tag{3.82}$$

From Eq. 3.76

$$s\begin{bmatrix} \tilde{i}_L \\ \tilde{v}_C \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \times \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_C \end{bmatrix} + \begin{bmatrix} \frac{D}{nL} \\ 0 \end{bmatrix} \tilde{v}_I + \begin{bmatrix} \frac{V_I}{nL} \\ 0 \end{bmatrix} \tilde{d} \tag{3.83}$$

The expression for $\tilde{d}$ (Eq. 3.82) is then substituted into Eq. 3.83, and all terms involving $\tilde{i}_L$ are collected as part of a new driving term. The result is a reformulated version of Eq. 3.76:

$$s\begin{bmatrix} \tilde{i}_L \\ \tilde{v}_C \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \times \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tilde{v}_I + \begin{bmatrix} s \\ 0 \end{bmatrix} \tilde{i}_L \tag{3.84}$$

Note that the state equation for $\tilde{i}_L$ now is just $s\tilde{i}_L = s\tilde{i}_L$. The duty ratio expression (Eq. 3.82) combined with Eq. 3.84 has the same number of independent equations as the state-space averaged Eq. 3.76, from which it was derived.

Eq. 3.84 still does not describe the peak-current control mode, since it was derived solely from the state-space averaged Eq. 3.76. However, it is now easy to insert the second piece of information, the description of the effects of the current loop as detailed in the control constraint (3.80). The peak-current state equation is then obtained as

$$s\begin{bmatrix} \tilde{i}_L \\ \tilde{v}_C \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \times \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tilde{v}_I + \begin{bmatrix} \frac{s}{n} \\ 0 \end{bmatrix} \tilde{i}_C \tag{3.85}$$

Note that the current i_L is no longer a state and the order of the system is therefore reduced by one. The new power stage of Fig. 3.11 is shown in Fig. 3.14 (a).

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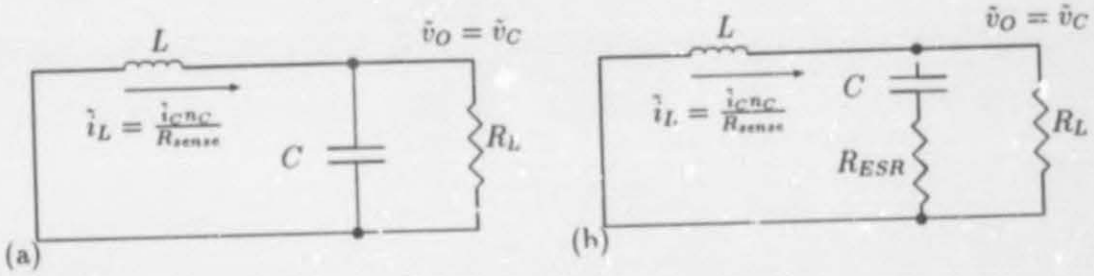

Figure 3.14: (a) Small-signal model of the converter; (b) model with ESR

The open-loop transfer function (F(s)) without compensation (G(s)) can be found using Eq. 3.85:

$$\frac{\tilde{v}_O}{\tilde{i}_C} = \frac{\frac{1}{nC}}{s + \frac{1}{RC}} \tag{3.86}$$

It can easily be seen that this is a single-pole transfer function with roll-off frequency at $\frac{1}{RC}$. For stability reasons the roll-off frequency will be changed, with the inclusion of a pole-zero pair as compensation network.

The small-signal model of the converter with the capacitor R_{ESR} is shown in Fig. 3.11 (b). The impedance seen by the inductor current is:

$$\begin{aligned} Z &= R_{ESR} + \frac{1}{sC} \| R_L \\ &= \frac{R_L(1 + sR_{ESR}C)}{1 + sC(R_{ESR} + R_L)} \end{aligned} \tag{3.87}$$

The transfer function then becomes:

$$\frac{\tilde{v}_O}{\tilde{i}_C} = \frac{k(1 + sR_{ESR}C)}{1 + sC(R_{ESR} + R_L)} \tag{3.88}$$

The control-to-output gain will vary with output loading, and as the load is increased, the gain decreases. The output capacitor ESR will determine the frequency at which the zero occurs, therefore changing the gain as a function of ESR. To ensure stability through all the combinations of load and ESR, the voltage amplifier will be compensated to cross 0 *db* at approximately one fifth of the switching frequency with an ample phase margin.

The pole and zero occur at:

$$\begin{aligned} f_p &= \frac{1}{2\pi(R_L + R_{ESR})C} \\ &= \frac{1}{2 \times \pi \times (7.8 + 0.016) \times 200.10^{-6}} = 100\ Hz \text{ (average load)} \end{aligned}$$

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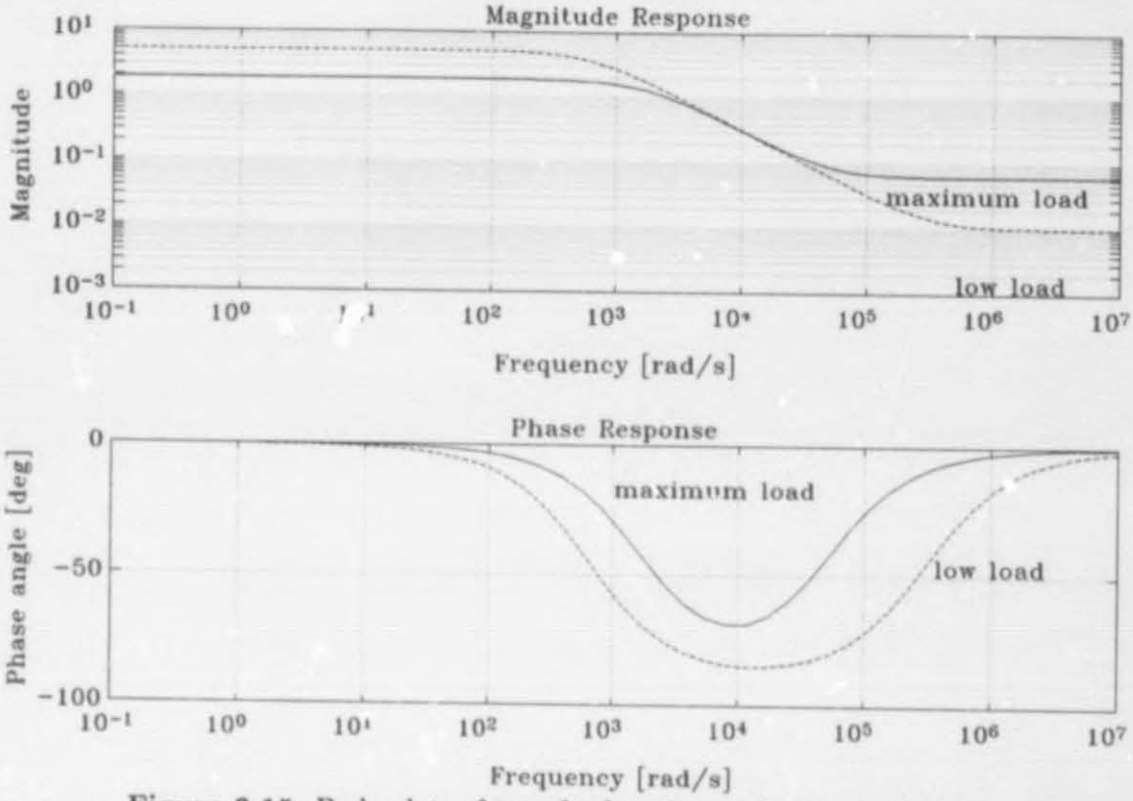

Figure 3.15: Bode plots of transfer function without compensation

$$= \frac{1}{2 \times \pi \times (2.8 + 0.1) \times 200.10^{-6}} = 275\ Hz \text{ (maximum load)} \tag{3.89}$$

and

$$\begin{aligned} f_z &= \frac{1}{2\pi R_{ESR} C} \\ &= \frac{1}{2 \times \pi \times 0.1 \times 200.10^{-6}} = 8\ kHz \text{ (average load)} \\ &= \frac{1}{2 \times \pi \times 0.016 \times 200.10^{-6}} = 50\ kHz \text{ (maximum load)} \end{aligned} \tag{3.90}$$

The gain (k) is

$$\begin{aligned} k &= 3 R_{sense} n_c R_L \\ &= 3 \times \frac{220}{1000} \times 7.8 = 5.10 \text{ (average load)} \\ &= 3 \times \frac{220}{1000} \times 2.8 = 1.86 \text{ (maximum load)} \end{aligned} \tag{3.91}$$

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The control-to-output gain can be plotted along with the desired 0 *db* crossing point, and an estimate of the compensation network required for the error amplifier can be made. The compensation should have a zero at approximately 1 kHz, and a gain of -16 *db* at this frequency. By placing a resistor $R_C = 68\ k\Omega$ and capacitor $C_C = 2.2\ nF$ in the voltage feedback loop, a pole-zero pair is included in the transfer function. This compensation is synthesised in Section 3.5.1.

The compensated response is plotted in Fig. 3.15 and the uncompensated response is plotted in Fig. 3.16. Low-frequency gains of 100 *db* at full load, and 115 *db* at light load are obtained, with a 0 *db* crossing at approximately 1.6 kH for both.

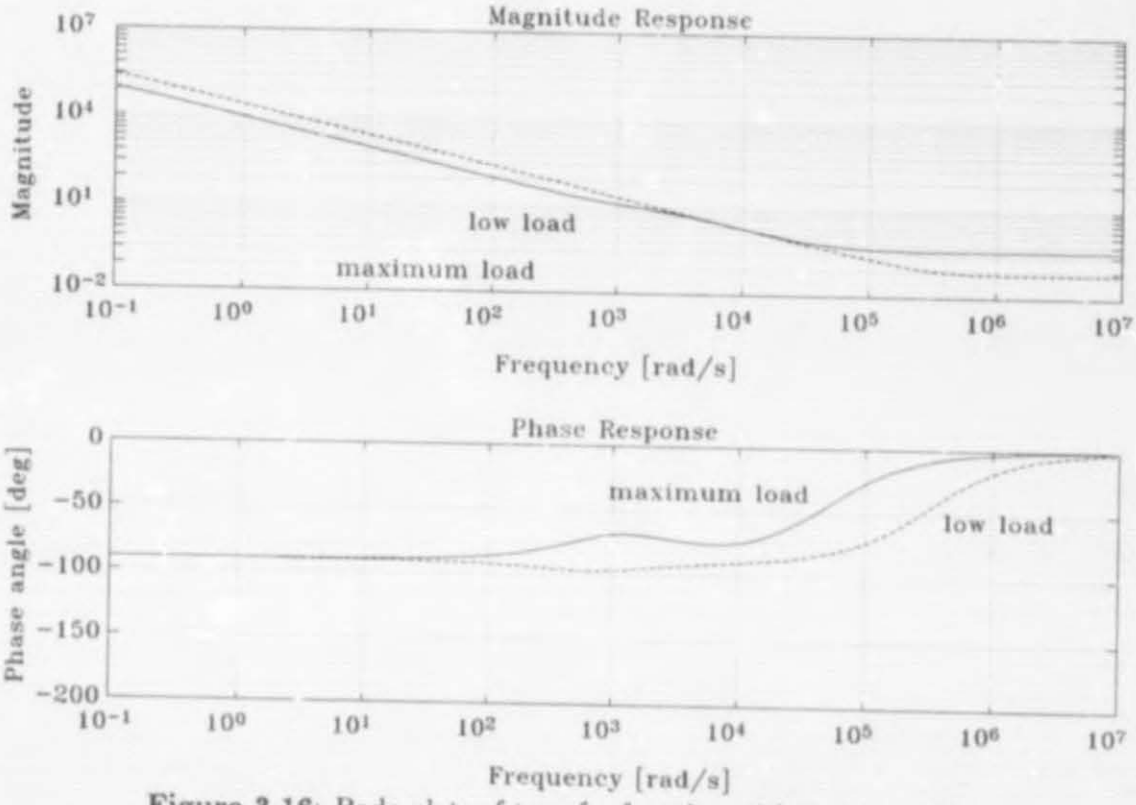

Figure 3.16: Bode plots of transfer function with compensation

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3.5 Synthesis of bus voltage regulation

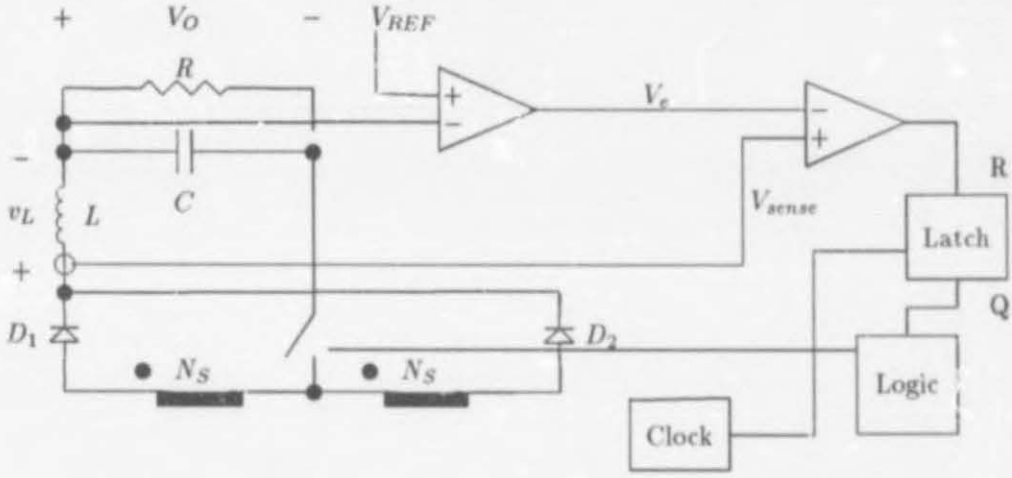

Figure 3.17: Converter with block diagram of the bus control circuit

Practically, peak-current control means that, instead of the error voltage being compared to a voltage ramp, it is compared to an analogue of the inductor current, forcing the peak current to follow the error voltage.

Fig. 3.17 illustrates a simplified block diagram of the converter employing peak-current control. Since the average inductor current can change only if the error signal changes, the inductor may be replaced by a current source, and the order of the system reduced by one.

Although there are many advantages to peak-current control, this technique is difficult to implement without suitable integrated circuits that can perform the associated control functions discussed in the previous section. A new integrated circuit designed specifically for control of peak-current control is the UC1846 [33].

3.5.1 Voltage Feedback

The UC1846 provides a 5.1 V reference. By voltage division, 0.15 V is obtained as reference at the positive input of the voltage error amplifier (Fig. 3.18):

$$V_+ = 5.1\ V \times \frac{R_2}{R_1 + R_2} = 0.22\ V \tag{3.92}$$

if $R_1 = 2k2$ and $R_2 = 100\ \Omega$. If the output reaches the required 14 V level, the negative input of the amplifier should be at 0.22 V. This means

$$V_- = 14\ V \times \frac{R_4}{R_3 + R_4} = 0.22\ V \tag{3.93}$$

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if $R_1 = 11k$ and $R_2 = 100\ \Omega$.

The compensation resistor R_C and capacitor C_C are shown in Fig. 3.18. The transfer function of this circuit is:

$$\frac{V_O}{V_e} = \frac{Z_f}{Z_i} \tag{3.94}$$

$$= \frac{R_C + \frac{1}{sC_C}}{R_3} \tag{3.95}$$

$$= \frac{1 + sR_CC_C}{sR_3C_C}$$

The feedback compensation, therefore, adds a pole at the origin and a zero at $f_z = \frac{1}{2\pi R_C C_C} = 1\ kHz$ to the transfer function, if $R_C = 68\ k\Omega$ and $C_C = 2.2\ nF$.

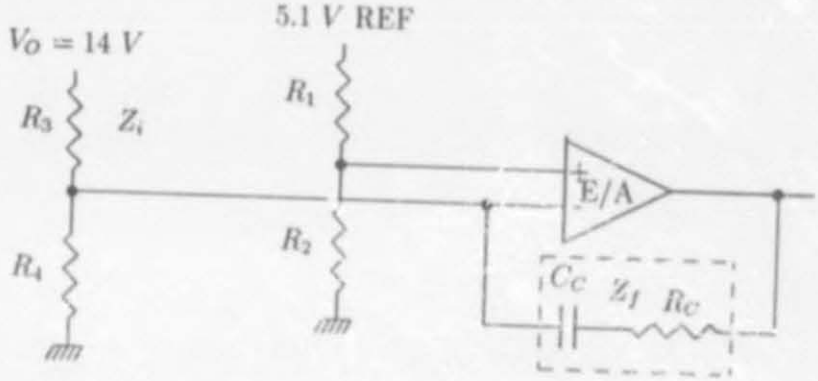

Figure 3.18: Voltage Feedback

3.5.2 Current-Sense Amplifier

The current-sense amplifier may be used in a variety of ways to sense peak inductor current for comparison with an error voltage. The maximum swing on the inverting input of the PWM comparator is limited to approximately 3.5 V by the internal regulated supply. Accordingly, for a fixed gain of 3, maximum differential voltages must be kept below 1.2 V at the current-sense inputs. Fig. 3.19 depicts two methods of sensing sense schemes. Direct resistive sensing is the simplest; however, a lower peak voltage may be required to minimize power loss in the sense resistor. Transformer coupling can provide isolation and increase efficiency at the cost of added complexity. Regardless of the scheme, the largest sense voltage consistent with low power losses should be chosen for noise immunity. Typically, this will range from several hundred millivolts in some resistive sense circuits to the maximum of 1.2 V in transformer coupled circuits [33].

The current is sensed by the second method mentioned above. The secondary current (I_{sn}) of the current transformer is $\frac{1}{1000}$ times the primary current (I_{pp}). It therefore has

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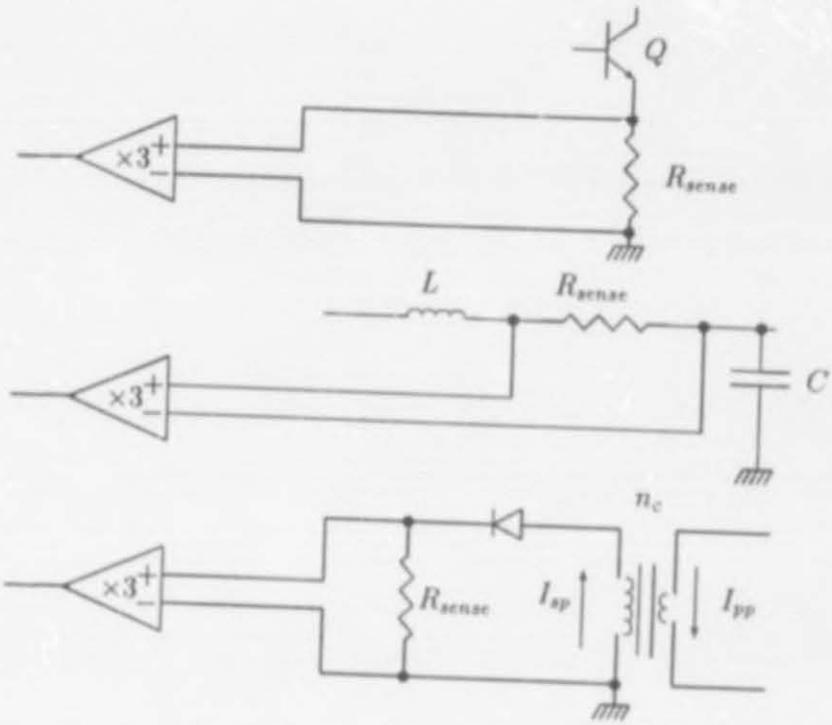

Figure 3.19: Various current-sense schemes

a peak value of

$$I_{sp} = \frac{1}{1000} I_{pp} = 0.007\ A \tag{3.96}$$

This value can be transformed to a value limited by 1.2 V by multiplying it with a resistance of 220 Ω.

In addition, caution should be exercised when using a configuration that senses inductor current. As the switch is turned on, a large instantaneous current spike can be generated as the collector capacitance of the switch is discharged. This spike will often be of sufficient magnitude and duration to trip the current-sense latch and result in erratic operation of the PWM circuit, particularly at lower duty cycles. A small RC filter in series with the input is generally all that is required to reduce the spike to an acceptable level as shown in Fig. 3.20.

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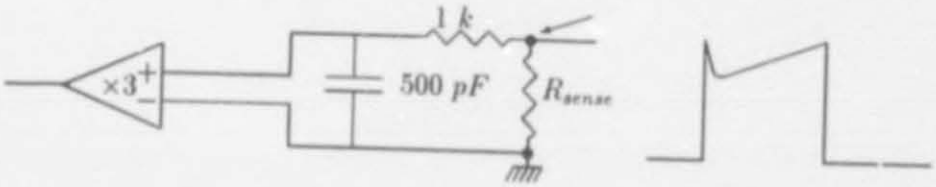

Figure 3.20: RC filter for reducing switch transients

3.5.3 Oscillator

Referring to Fig. 3.21, an external resistor R_T is used to generate a constant current into a capacitor C_T in order to produce a linear sawtooth waveform [33]. Oscillator frequency may be approximated by selecting R_T and C_T, so that

$$f_{osc} = \frac{2}{R_T\, C_T} \tag{3.97}$$

where R_T can range from 1 $k\Omega$ to 500 $k\Omega$ and C_T is above 100 pF. For $R_T = 5.6\ k\Omega$ and $C_T = 4.7\ nF$ the oscillator frequency is $f_{osc} \approx 70\ kHz$.

Again referring to Fig. 3.21, the oscillator generates an internal clock pulse used to stop both outputs, and to prevent simultaneous cross conduction during switching transitions. This output dead time is controlled by the oscillator fall time. Fall time, in turn, is controlled by C_T according to the formula:

$$\tau_d = 145\ C_T \left[\frac{12}{12 - \frac{3.6}{R_T}} \right] \tag{3.98}$$

For large values of R_T:

$$\tau_d = 145 C_T = 68\ \mu s \tag{3.99}$$

Although timing capacitors as small as 100 pF can be used successfully in low-noise environments, it is generally recommended that C_T be kept above 1000 pF to minimize noise effects on the oscillator frequency.

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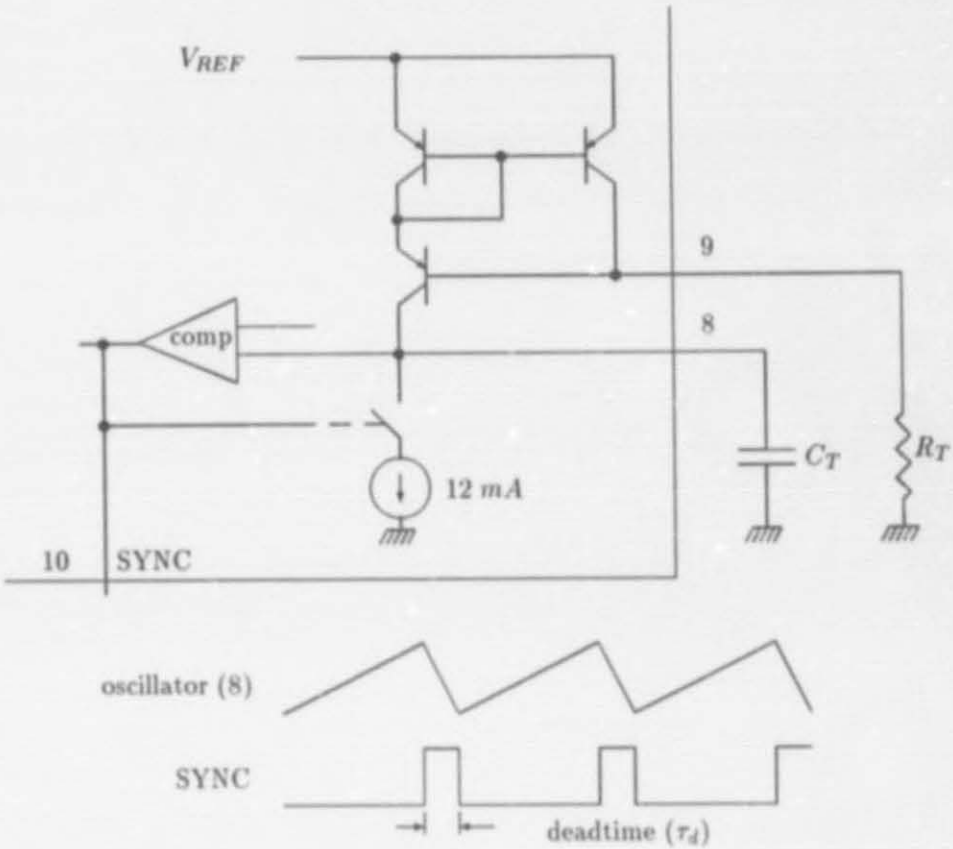

Figure 3.21: Oscillator Circuit

3.5.4 Current Limit

One of the most attractive features of a current-mode converter is its ability to limit peak inductor currents on a pulse-by-pulse basis, by simply limiting the error voltage to a maximum value. Referring to Fig. 3.22, peak current limiting in the UC1846 [33] is accomplished, using a divider network, R_5 and R_6, to set a predetermined voltage at pin 1.

This voltage, in conjunction with Q_1, acts to clamp the output of the error amplifier at a maximum value. Since the base emitter drop of Q_1, and the forward drop of the diode very nearly cancel each other out, the negative input of the comparator will be clamped at the value $V_{pin1} - 0.5\ V$. Following this through to the input of the current-sense amplifier yields:

$$V_{CS} = \frac{V_{pin1} - 0.5}{3} \tag{3.100}$$

where V_{CS} is the differential input voltage of the current-sense amplifier. Using this relationship, a value for maximum inductor current in terms of external programming

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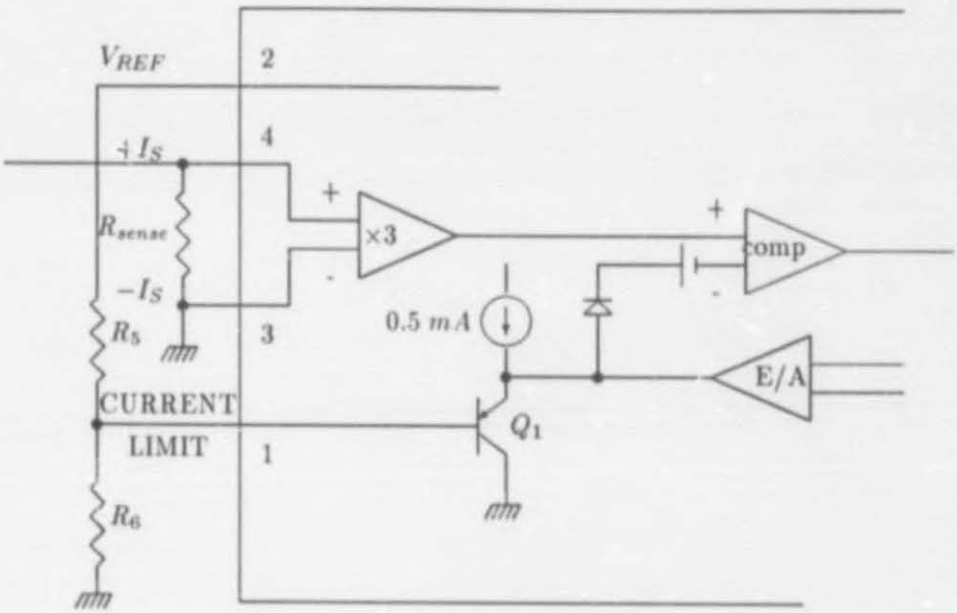

Figure 3.22: Peak current limit set up

resistors can be derived, resulting in:

$$I_{CL} = \frac{\frac{R_6(V_{REF})}{R_5+R_6} - 0.5}{3R_S} \tag{3.101}$$

R_5 also supplies holding current for the shutdown circuit, and therefore should be selected prior to selecting R_6, as outlined in the next section. The current is limited to the peak inductor current $I_L = 7\ A$ as obtained from Fig. 3.4(b). For $I_{CL} = 5\ A$, $R_5 = 10\ k\Omega$ and $R_6 = 1\ M\Omega$.

As may be seen from Eq. 3.101, any signal less than 0.5 V at the current-limit input will guarantee both outputs to be off, making pin 1 a convenient point for both shutting down and slow-starting the PWM circuit. Both the under-voltage lockout and shutdown functions are connected internally to this point. If a capacitor is used to hold pin 1 low (Fig. 3.23), then, as the input voltage increases above the under-voltage lockout level, the capacitor will charge and gradually increase the PWM duty cycle to its operating point. In a similar manner, if the shutdown amplifier is pulsed, the shutdown SCR will be fired and the capacitor discharged, guaranteeing a shutdown and soft restart cycle independent of input pulse width.

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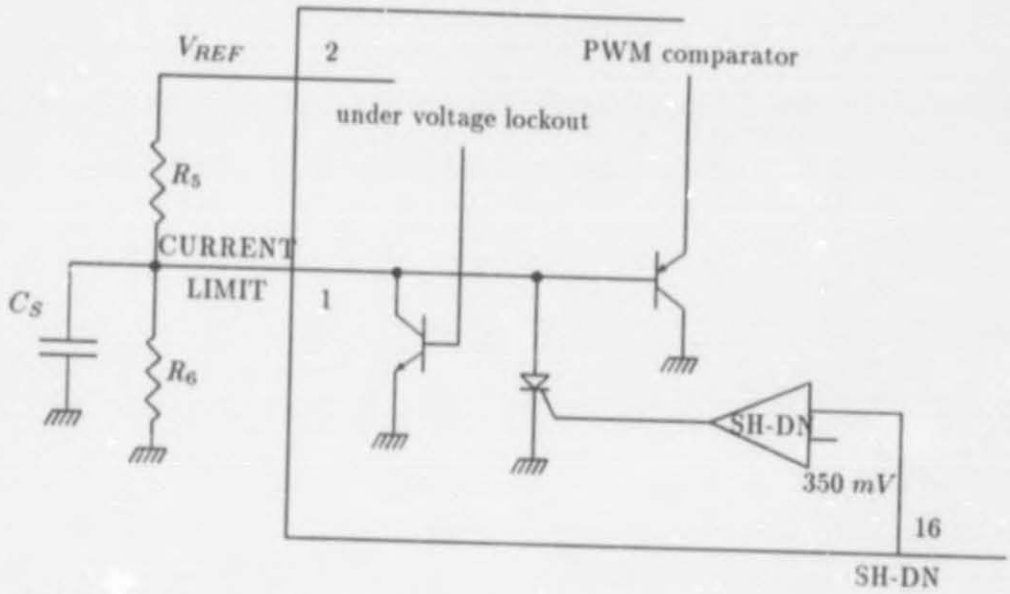

Figure 3.23: Using under-voltage lockout and shutdown to initiate a slow start

3.5.5 Shutdown

The shutdown circuit, shown in Fig. 3.24, is used for remote shutdown of the converter by the telecommand. The circuit may be divided into an input section consisting of a comparator with a 350 mV temperature compensated offset, and an output section consisting of a three-transistor latch. Shutdown is accomplished by applying a signal greater than 350 mV to pin 16, causing the output latch to fire, and setting the PWM latch to provide an immediate signal to the outputs. At this point, several things can happen. Q_1 requires a minimum holding current, I_H, of approximately 1.5 mA, in order to remain in the latched state. Therefore, if R_5 is chosen greater than 5 $k\Omega$, Q_1 will discharge any capacitance, $C_S = 1\ \mu F$, on pin 1 to ground, commutating the output latch and allowing C_S to recharge. If R_5 is chosen less than 2.5 $k\Omega$, Q_1 will discharge C_S and remain in the latched state until power is switched off [33]. This is why R_5 is chosen well above 2.5 $k\Omega$ as 10 $k\Omega$.

3.5.6 Compensation of peak-current control

In a current mode control PWM IC, the error voltage is generated at the output of the error amplifier and compared to the inductor current at the PWM comparator. At this node, subtracting the compensation ramp from the error voltage, or adding it to the current-sense input, will have the same effect: to decrease the pulse width as a function of duty cycle. It is more convenient to add the slope-compensating ramp to the current input. A portion of the oscillator waveform available at the timing capacitor (C_T) will be resistively summed with the inductor current. This is connected to the PWM comparator

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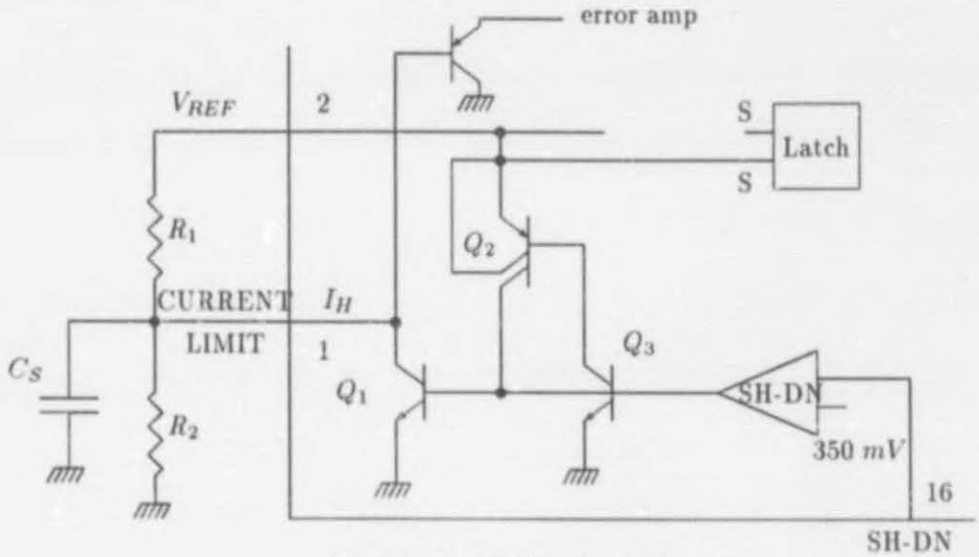

Figure 3.24: Shutdown Circuitry

at the current-sense input. The compensation circuit is shown in Fig. 3.25(a).

Resistors R_1 and R_2 form a voltage divider from the oscillator output to the current-limit input, superimposing the slope compensation on the inductor current waveform. Capacitor C_1 is a coupling capacitor and allows the voltage swing of the oscillator to be used without adding offset circuitry. Capacitor C_2 forms a RC-filter with R_1 to suppress the leading edge glitch of the inductor current wave. The ratio of resistor R_2 to resistor R_1 will determine the exact amount of slope compensation added.

For purposes of determining the resistor values, capacitors C_t (timing), C_1 (coupling), and C_2 (filtering) can be removed from the circuit. The oscillator voltage (v_t) is the peak-to-peak amplitude of the sawtooth waveform. The simplified model is represented schematically in Fig. 3.25(b).

The inductor downslope is from Section 3.3.1

$$\begin{aligned} \frac{di}{dt} &= \frac{V_O}{L} \\ &= \frac{14}{7.10^{-6}} = 2\ A/\mu s \end{aligned} \tag{3.102}$$

After it has been sensed by the current transformer, it is converted to a voltage through the sense resistor.

$$s_i = \frac{di}{dt}\frac{R_s}{n_c} = 2.10^6 \times \frac{220}{1000} = 4$$

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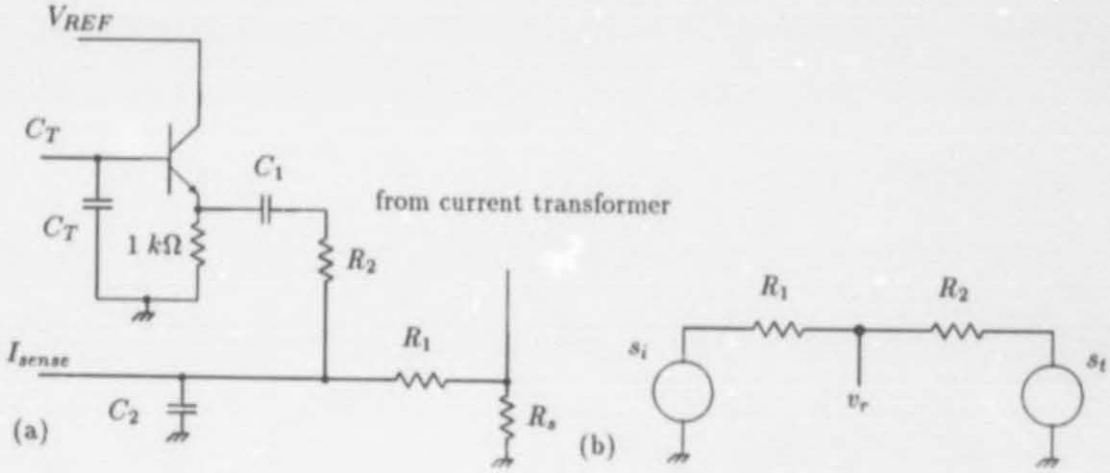

Figure 3.25: (a)Compensation Circuitry, (b)Superposition

The oscillator charge slope is

$$s_t = \frac{\Delta v_t}{t_{on}} = \frac{3}{2 \times 14.10^{-6}} = 107\ V/ms$$

If one uses the circuit in Fig. 3.25(b) and superposition, the voltage at the current-sense becomes:

$$\begin{aligned} v_r &= \frac{s_i R_1}{R_1 + R_2} + \frac{s_t R_2}{R_1 + R_2} \\ &= p_i + p_t \end{aligned} \tag{3.103}$$

where $p_i = \frac{s_i R_1}{R_1+R_2}$ and $p_t = \frac{s_t R_2}{R_1+R_2}$.

The slope compensation can now be calculated as $s_t = m s_i$, where m is the amount of inductor downslope to be introduced. Solving:

$$R_2 = R_1 \frac{p_t}{p_i m} \tag{3.104}$$

In Section 3.4.1 it is found that, for the best results, the compensation slope must equal the downslope of the inductor current . Therefore, $m = 1$. R_1 has a value of $1\ k\Omega$ from Section 3.5.2 and therefore is

$$R_2 = 1.10^3 \times \frac{107}{440} = 243\ k\Omega$$

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3.6 Analysis of the PV Control

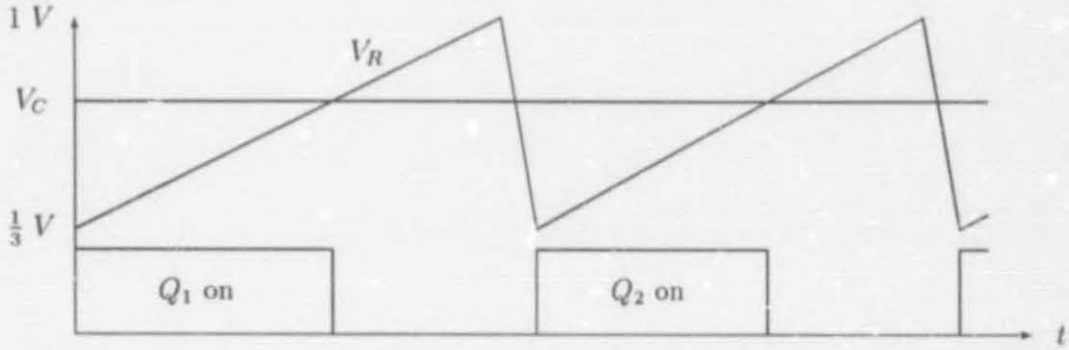

Figure 3.26: Waveforms of the PWM generator

The pulse width modulator for the MPPT compares a control voltage (V_C) with a ramp waveform (V_R) and amplifies the difference to give a square waveform which drives the switching elements of the converter. These waveforms are shown in Fig. 3.26.

The ramp waveform is the oscillator capacitor voltage of the control circuit clock, as described in Section 3.5. This waveform is described by Eq. 3.105:

$$V_R = \frac{2t}{3\tau} + \frac{1}{3}$$
$$\frac{2}{3}D + \frac{1}{3} \tag{3.105}$$

where D is the duty ratio and τ is the period of the ramp waveform. From this equation the duty ratio can be obtained in terms of the control voltage as:

$$D = \frac{3}{2}V_C - \frac{1}{2} \tag{3.106}$$

The relationship between the solar panel voltage (V_{PV}) and the duty ratio (D) can be obtained from the voltage transfer equation (Eq. 3.10) of the compound converter as:

$$V_{PV} = \frac{12}{D} \tag{3.107}$$

Inserting Eq. 3.107 in Eq. 3.106 gives:

$$V_{PV} = \frac{24}{3V_C - 1} \tag{3.108}$$

By setting the control voltage V_C equal to a constant k_2 times the output power subtracted from an offset k_1, or $V_C = k_1 - k_2P$, the system shown in Fig. 3.27 is obtained.

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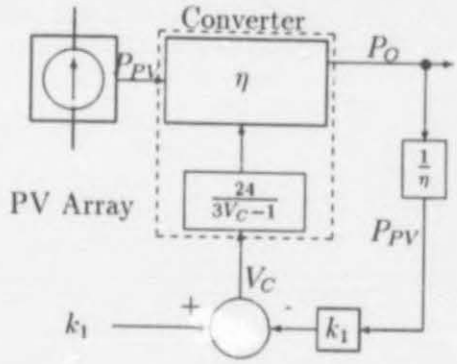

Figure 3.27: Diagram of negative feedback MPPT

3.7 Design of the PV Control

The purpose of this section is to design the MPPT control shown in Fig. 3.27. The MPPT control consists of an analog adder to add the battery current to the bus current, with a gain that compensates for the average efficiency of the converter. It further multiplies the current with a gain equal to the average output voltage, to obtain a value representative of the PV generator power (P_{PV}). The adder has a negative gain, because the power must be subtracted from a constant (k_1).

The next step is to add this signal to the constant (k_1). The desired control signal (V_C) is now used to control the duty cycle. The duty cycle of the converter controls the array voltage (V_{PV}) internally as discussed previously.

Inverting Adder

The inverting adder is shown in Fig. 3.28.

The currents to be added are $i_1 = \frac{v_1}{R_1}$ and $i_2 = \frac{v_2}{R_2}$. The output voltage $v_3 = -iR_2$, because the input voltage and current of the operational amplifier are zero. Adding the input currents:

$$\begin{aligned} i_3 &= i_1 + i_2 \\ \Rightarrow \frac{v_3}{R_2} &= -\left(\frac{v_1}{R_1} + \frac{v_2}{R_2}\right) \\ \Rightarrow v_3 &= -\frac{R_2}{R_1}(v_1 + v_2) \end{aligned} \tag{3.109}$$

The gain of the inverting adder ($\frac{R_2}{R_1}$) is obtained in the next equations. Power from the PV generator is obtained as follows:

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$$P_{PV} = I_{ss}\frac{V_O}{\eta} = 11.2 I_{ss}$$

where I_{ss} is the sensed current and $V_O = 14\ V$ is the average output voltage and $\eta = 0.8$ is the average efficiency of the converter. The current is sensed with a current transformer with a turns ratio $n_c = \frac{1}{1000}$. The sensed current goes to a sense resistor $R_S = 220\ \Omega$. The sense voltages v_1 and v_2 in Fig. 3.28 therefore are:

$$\begin{aligned} v_1 &= I_O\frac{220}{1000} \\ v_2 &= I_B\frac{220}{1000} \end{aligned} \tag{3.110}$$

It is evident that a gain of 0.22 is already built into the sampling of the output current. $\frac{R_2}{R_1}$ must then be:

$$\frac{R_2}{R_1} = \frac{V_O}{\eta}k_2\frac{1000}{220} = 0.09$$

$R_1 = 34\ k\Omega$ if the filter resitance is also added. Then $R_2 = 3.2\ k\Omega$.

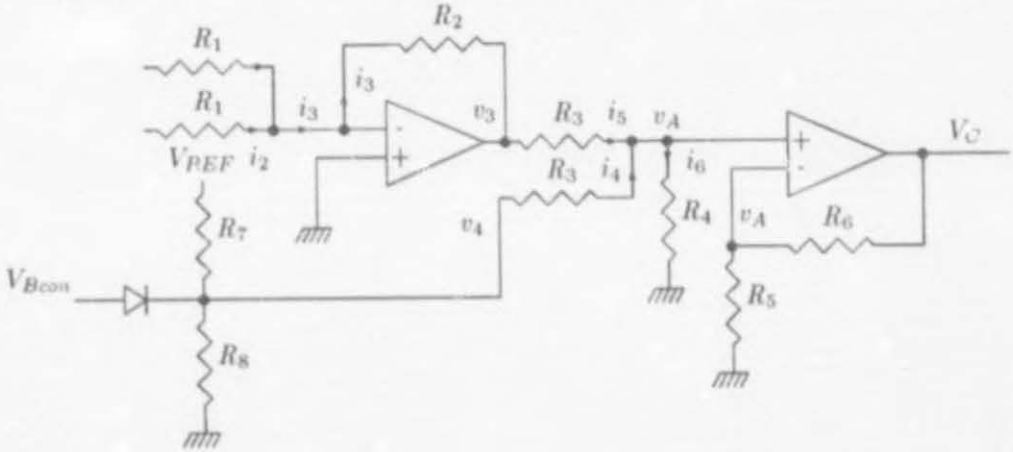

Figure 3.28: Implementation of MPPT function

Noninverting Adder

In Fig. 3.28 the voltage $v_A = i_6 R_4$ where,

$$i_6 = i_4 + i_5$$

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$$\begin{aligned} &= \frac{v_3 - v_A}{R_3} + \frac{v_4 - v_A}{R_3} \\ \Rightarrow v_A &= \frac{R_4}{R_3}(v_3 - v_A + v_4 - v_A) \\ &= \frac{v_3 + v_4}{3} \end{aligned} \tag{3.111}$$

By applying voltage division, the output voltage is obtained as follows:

$$\begin{aligned} V_C &= \left(1 + \frac{R_2}{R_1}\right) v_A \\ &= \left(1 + \frac{R_2}{R_1}\right)\left(\frac{v_3 + v_4}{3}\right) \end{aligned} \tag{3.112}$$

For unity gain $\frac{R_6}{R_5} = 2$ and choosing $R_6 = 200\ k\Omega$, R_5 becomes $100\ k\Omega$.

v_4 is the input of the offset k_1 that is set by voltage devision from the $5\ V$ reference voltage of the PWM IC. If $R_7 = 10\ k\Omega$, R_8 is obtained as:

$$R_8 = \frac{\frac{k_1}{V_{REF}} R_7}{1 - \frac{k_1}{V_{REF}}} = 1.5\ k\Omega$$

Battery Protection

The Battery Unit is protected by preventing the battery from overcharging. This is done by monitoring the battery voltage; as soon as it goes over the limit, the PV voltage (V_{PV}) is regulated to the upper limit away from the maximum power point. In this condition the power received from the PV generator is very low, and in the worst case, when minimum power is required by the load and maximum power is available from the PV generator, the current to the battery is a few mA.

As soon as the battery voltage drops below the lower limit, the MPPT starts operating again and the battery is charged. This is done by means of a hysteresis circuit.

Fig. 3.29(a) shows the charge curve of the battery. It is evident that the voltage reaches a sudden peak when fully charged. This peak is used as an indication that the battery is charged. The charge curve is sensed by voltage division (R_1 and R_2 in Fig. 3.29(b)).

Q_1 and Q_2 share an emitter resistor. It is essential that Q_2's resistor be larger than Q_2's. In that way the threshold used to turn on Q_1, which is one diode drop above the emitter voltage, rises when Q_1 is turned off, since the emitter current is higher with Q_2 conducting. This produces hysteresis in the trigger threshold.

Assume Q_1 is on and Q_2 is therefore off. R_3 is chosen as $1.5\ k\Omega$. The emitter current is then approximately $I_E = \frac{V_{REF}}{R_3} = \frac{5}{1500} = 3\ mA$. To switch Q_1 off, the voltage at its base

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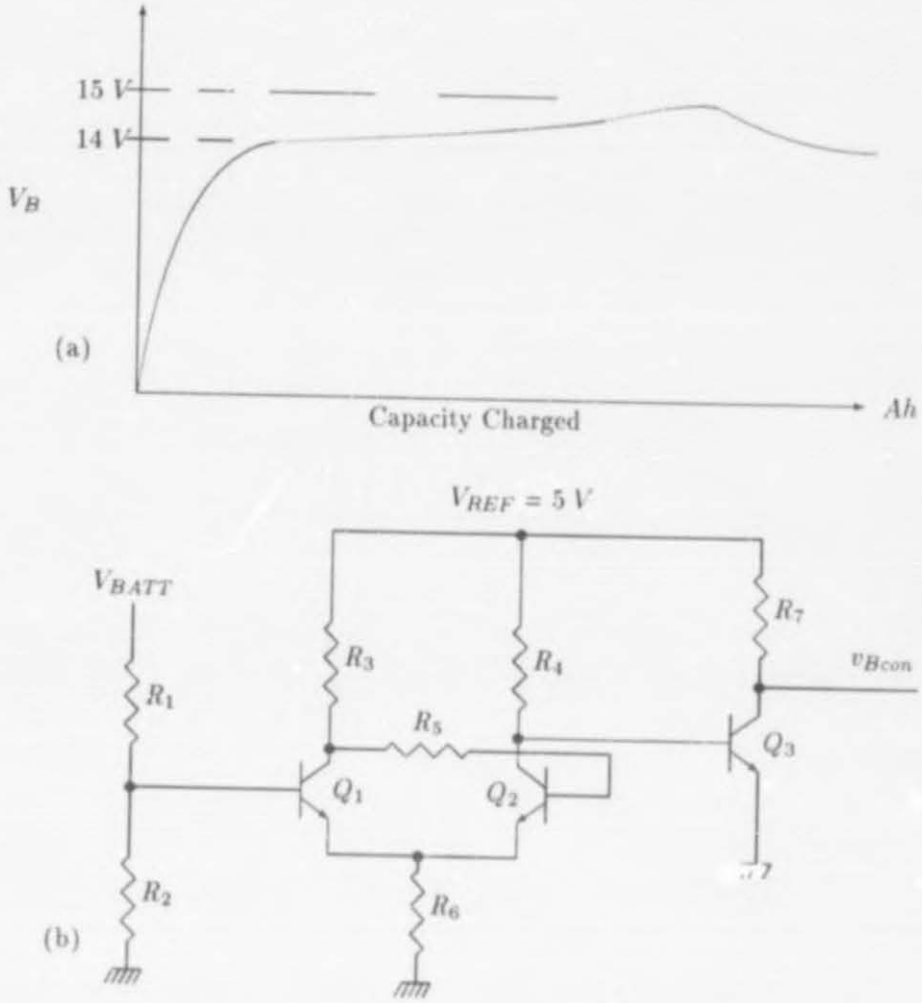

Figure 3.29: (a) Battery charge curve (b) Battery protection circuit

must be

$$V_{BEon} + I_E R_6 = 0.7 + 3.10^{-3} \times 47 < 0.85\ V$$

Q_1 must switch off when the battery voltage V_B is less than 11 V. By means of voltage division the resistors R_1 and R_2 are selected as 120 $k\Omega$ and 10 $k\Omega$ respectively, to give a base voltage of 0.85 V. After Q_1 is switched off, it must stay off until $V_B = 14\ V$. The base voltage then is 1 V. This voltage corresponds to an emitter voltage of 0.3 V and an emitter current of 6 mA. The purpose of Q_2 is to provide this current when Q_1 is off and the collector resistor R_4 limits it. $R_4 = \frac{V_{REF}}{I_E} = 820\ \Omega$.

Transistor Q_3 is used in an inverting stage. It is evident that when the battery is charged and Q_1 is on, Q_2 is off and Q_3 is on, with 5 V on the output. This signal is added to the constant k_1 of the MPPT and disables it. V_{PV} causes the power to roll over the maximum power point of the PV generator, with the result that the power from it is decreased enough to limit the current to the battery to a few mA. The battery charge

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regulation then is in trigger charged mode.

3.7.1 Synchronization

It is important that the two control circuits of the compound converter are synchronised. In this section the clocks of the two circuits are synchronised.

The timing capacitor C_T of the MPPT control circuit will be used as a summing junction for the analog sawtooth and digital sync input. The PWM is allowed to run independently using its own R_T and C_T components in standard configuration. For synchronization a digital sync pulse will be superimposed on the C_T waveform.

The sync pulse quickly raises the voltage at C_T above the PWM comparator threshold. This forces a change in the oscillator charge/discharge status and operation. The oscillator then begins its normal discharge cycle, synchronised to the sync signal. This digital sync pulse simply adds to the analog C_T input voltage above the upper threshold of the comparator.

In practice, this approach is best implemented by bringing C_T to ground through a small resistance (33 Ω). This low value is selected in order to have minimal offset and effects on the initial oscillator frequency. The sync pulse will be applied across the resistor.

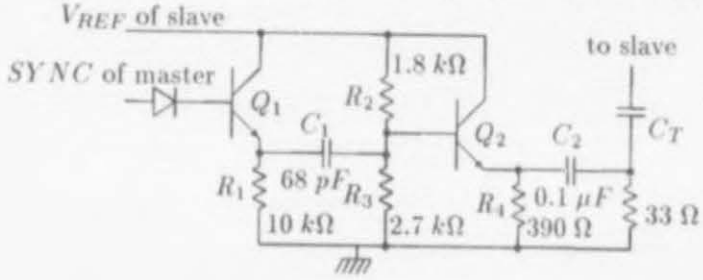

Figure 3.30: Sync circuit

The sync circuit is shown in Fig. 3.30. A positive going signal acts as input to the base of transistor Q_1, which operates as an emitter follower. The leading edge of the sync signal is coupled into the base of Q_2 through capacitor C_1, developing a voltage across R_4 in phase with the sync input, with a time duration of $R_C C_1$, where R_C is the equivalent resistance as seen by the capacitor. The calculation of R_C follows. Q_2 is biased by R_2 and R_3. The voltage at the base of Q_2 is:

$$\begin{aligned} V_B &= 5 \times \frac{R_3}{R_2 + R_3} \\ &= 5 \times \frac{2.7.10^3}{2.7.10^3 + 1.8.10^3} = 3\ V \end{aligned} \tag{3.113}$$

Assume that the base-emitter on-voltage is 0.7 V, which means that the voltage across R_4 is 2.3 V. This gives an emitter-current of $\frac{2.3}{390} = 5\ mA$. Assume that $\beta_0 = 100$, $r_b = 0$

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and $r_o = \infty$.

$$\begin{aligned}
\Rightarrow g_m &= \frac{I_C}{V_T} \\
&= \frac{5.10^{-3}}{25.10^{-3}} = 0.2\ \mho \\
\Rightarrow r_\pi &= \frac{\beta_0}{g_m} \\
= \frac{100}{0.2} &= 500\ \Omega \\
\Rightarrow R_i &= r_\pi + R_L(\beta_0 + 1) = 3.5\ k\Omega
\end{aligned} \tag{3.114}$$

where $R_L = R_4 \| 33\ \Omega$. The resistance R_C then is:

$$R_C = R_3 \| R_C = 1.5\ k\Omega$$

and the time duration of the generated signal then is 100 ns, which is significantly smaller than the switching period. This signal is driven through C_2 to the slave timing capacitor, forcing synchronization of the slave to the master.

3.8 Summary

In this chapter the compound converter was analysed and designed. Component values were obtained, which are shown in the schematic diagrams in App. G. The thermal and physical properties of components were looked at carefully in order to find out which components are the best for space applications. Stability was also an important design constraint.

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Chapter 4

Practical Evaluation of the Converter

4.1 Introduction

In this chapter the prototype of the compound converter is evaluated against the main design specifications. The prototype converter is shown in Fig. 4.1.

The first section consists of waveforms used to prove the analysis and design of different parts of the compound converter. The test results of the maximum power point tracker (MPPT) is given in Section 4.3. In Section 4.4 the efficiency is shown. The noise measurements are given in Section 4.5.

4.2 Measured Waveforms

4.2.1 Practical Arrangement

The practical arrangement of the power system breadboard model for measuring main circuit waveforms is shown in Fig. 4.2. Commercial solar panels are used for the PV generator. It is situated on the outside of the laboratory and is connected to the compound converter through the cables on the right. The battery unit is situated on the left of the picture. Note that the earth connection of the oscilloscope probe is made as short as possible by wrapping it around the tip, to reduce EMI.

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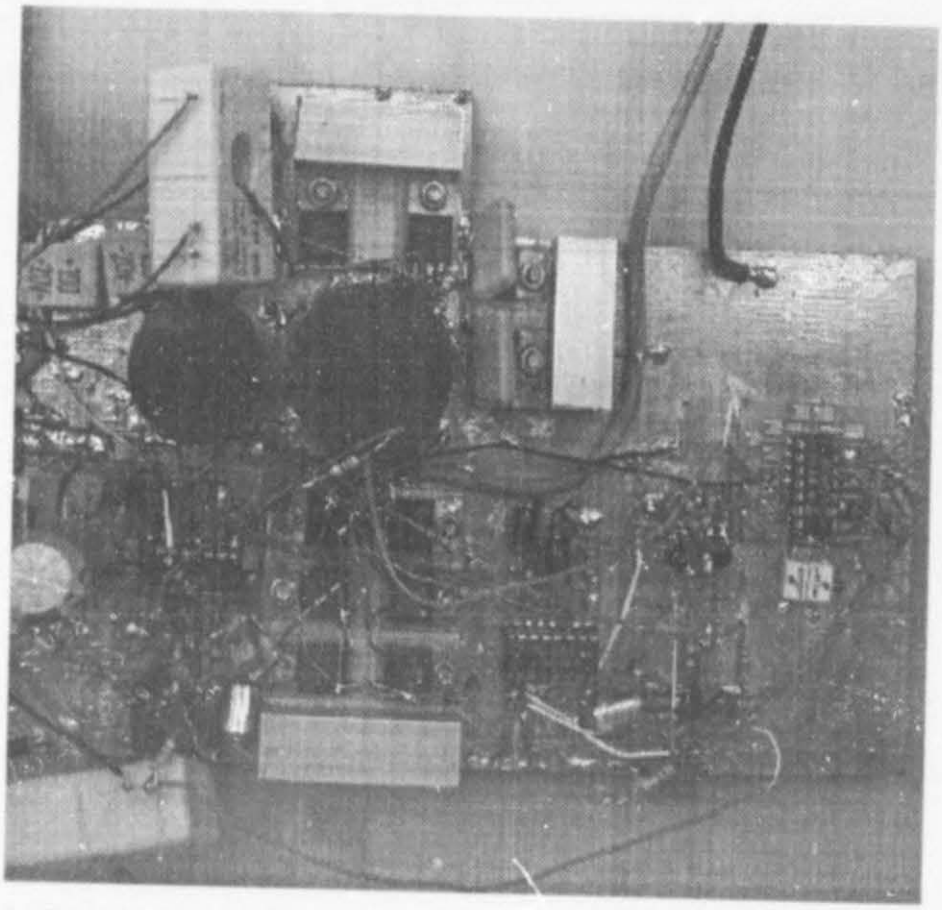

Figure 4.1: Picture of the prototype Compound Converter Taken with Sunsat's CCD Camera

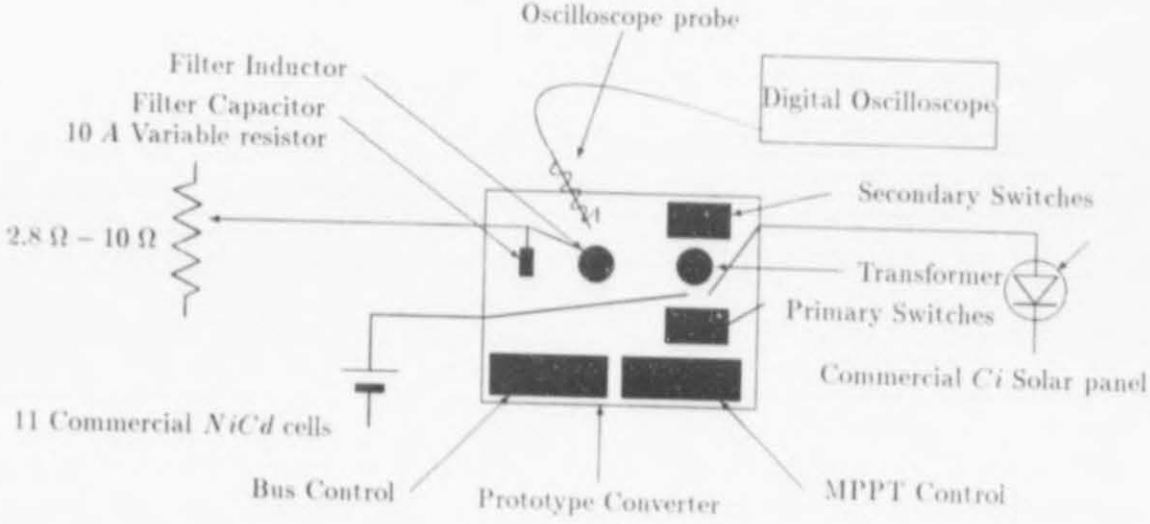

Figure 4.2: Practical arrangement for measuring waveforms

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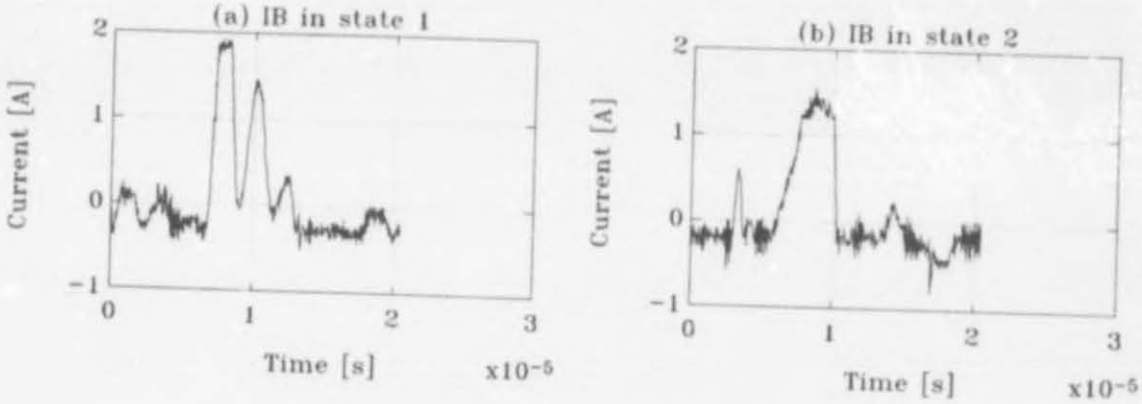

Figure 4.3: (a) I_B in state 1, (b) I_B in state 2

4.2.2 Battery Current

The battery current waveform in converter state 1 is shown in Fig. 4.3 (a). When the primary switch switches on, a large current spike occurs. The rest of the waveform is the same as predicted in the analysis. The current has a steep slope, because the inductance to the battery is very low.

The waveform in Fig. 4.3(b) represents the battery current in converter state 2. Again, there is a large current spike after which the current increases steeply due to the low inductance. At the instant the secondary switch switches on, the current starts increasing at a different slope, as predicted in Fig. 3.3.

4.2.3 Peak-Current Control

In this section the peak-current control compensation is illustrated practically. The waveform in Fig. 4.4(a) represents the inductor current without compensation. It is clear that the control is unstable, because the error adds up during each cycle.

The waveform in Fig. 4.4(b) represents the inductor current with compensation. In this case the control is stable.

The current sense voltage without compensation in the voltage feedback loop, is shown in Fig. 4.5 (a). It can be seen that the system is unstable and oscillations occur at a frequency of 1 kHz.

In Fig. 4.5 (b) the compensation in the voltage feedback loop is included. It is evident that the system is stable.

These results prove that the desired compensation for the peak-current control, discussed in Section 3.4 is effective.

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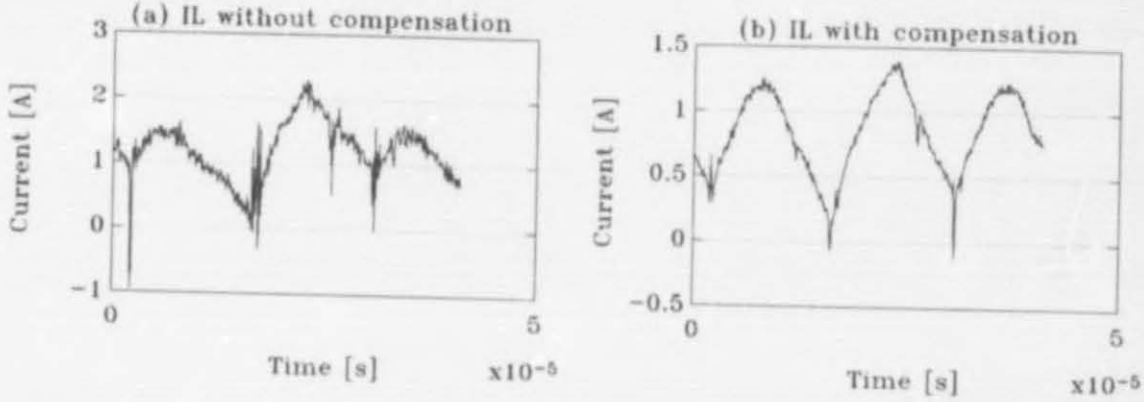

Figure 4.4: (a) Peak-current control without compensation, and (b) with compensation

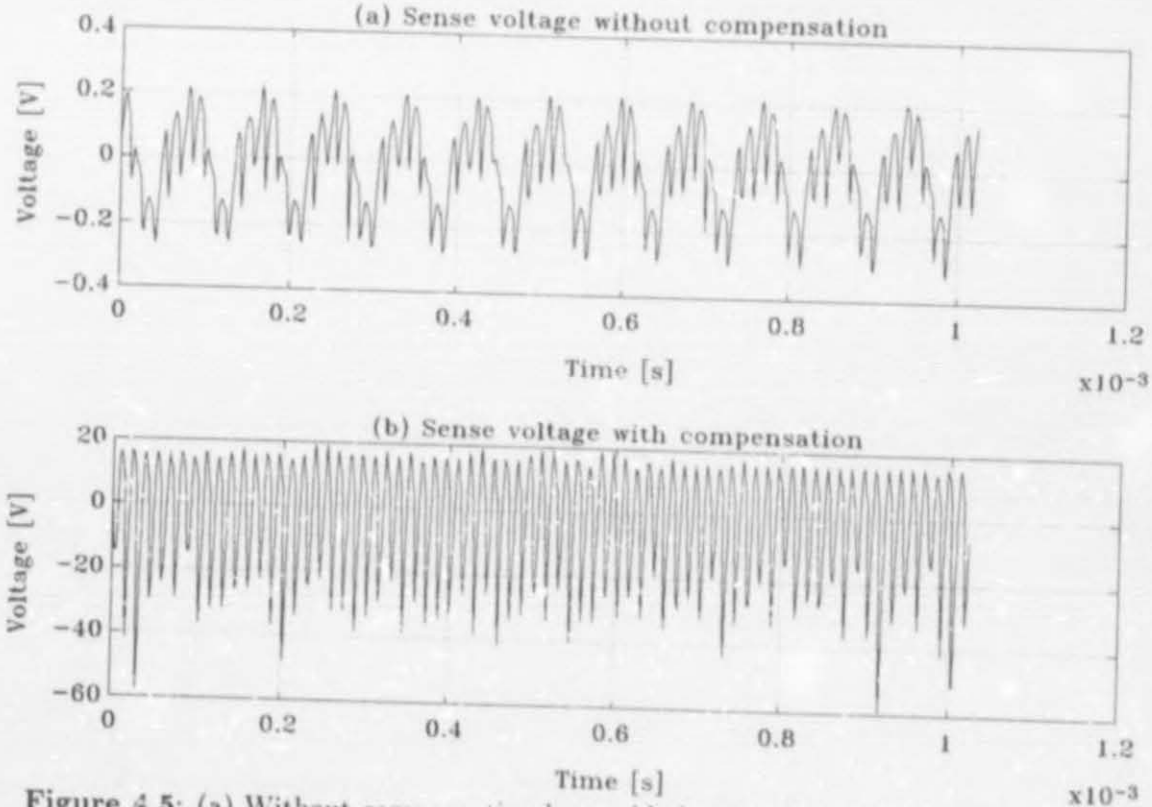

Figure 4.5: (a) Without compensation in outside loop, and (b) with compensation

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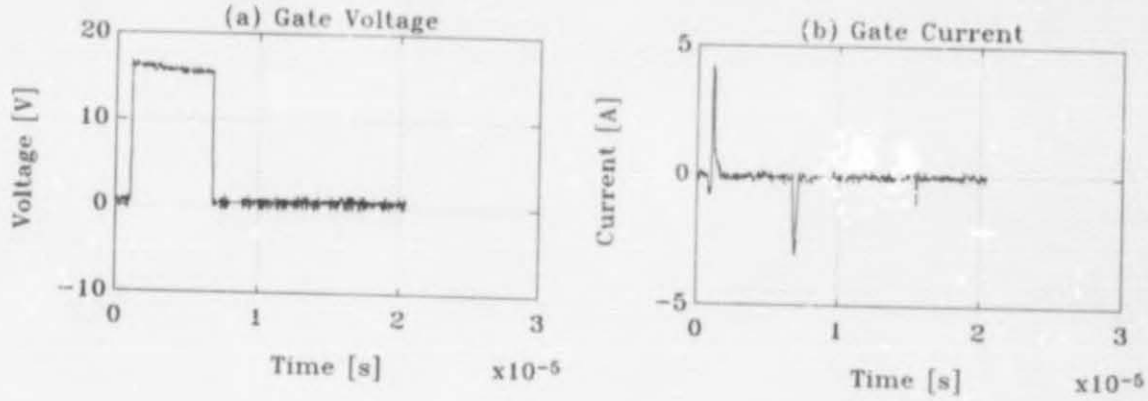

Figure 4.6: Gate drive waveforms

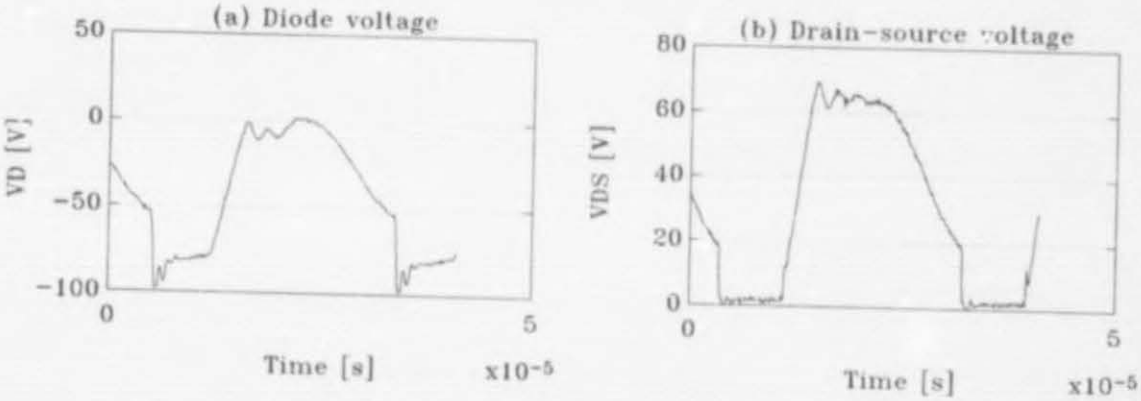

Figure 4.7: (a) Diode Voltage (b) Drain-source voltage

4.2.4 Gate Waveforms

Fig. 4.6(a) shows the gate voltage waveform. It can be seen that there is almost no voltage overshoot. The current waveform is shown in Fig. 4.6(b). The peak current seems to be near the maximum for the UC1846 and should be limited with a higher gate resistance.

4.2.5 Snubber Waveforms

Fig. 4.7(a) represents the voltage acoss a rectifier diode with a capacitive snubber. It is equal to the snubber capacitor voltage. The energy does not oscillate between the leakage inductance and the snubber capacitance, because of a damping resistance, as discussed in Section 3.3.5.

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Referring to Fig. 4.7(a): While the diode is on, the voltage across it is approximately zero. When the diode switches off as a result of the control switch switching off, the voltage across the snubber capacitor increases slightly, causing the overall diode voltage to increase. When all the energy from the stray inductances is absorbed by the capacitor, it starts dissipating it into the snubber resistance, causing the voltage to decrease. Later the other diode switches on, causing a negative voltage across the secondary winding on this side. This results in a negative voltage across the diode.

Referring to Fig. 4.7(b), it can be seen that the primary switches switch on hard. The snubber discharge curve can be seen on this waveform, because it is transformed from the secondary side.

4.3 Maximum Power Point Tracking

4.3.1 Practical Arrangement

The practical arrangement for testing the MPPT is shown in Fig. 4.8.

4.3.2 Test Results of MPPT

The MPPT was tested by first measuring the operating point of the converter. The PV generator was then quickly disconnected from the converter, and points close to the operating point of the converter were measured.

These points are given in Table 4.1 . The first point, in each case, is the operating point, and the following points are the points around this operating point. In each case the measured operating point was the maximum power point.

When the panels with the right voltage range for the engineering model are available, better test results will be obtained.

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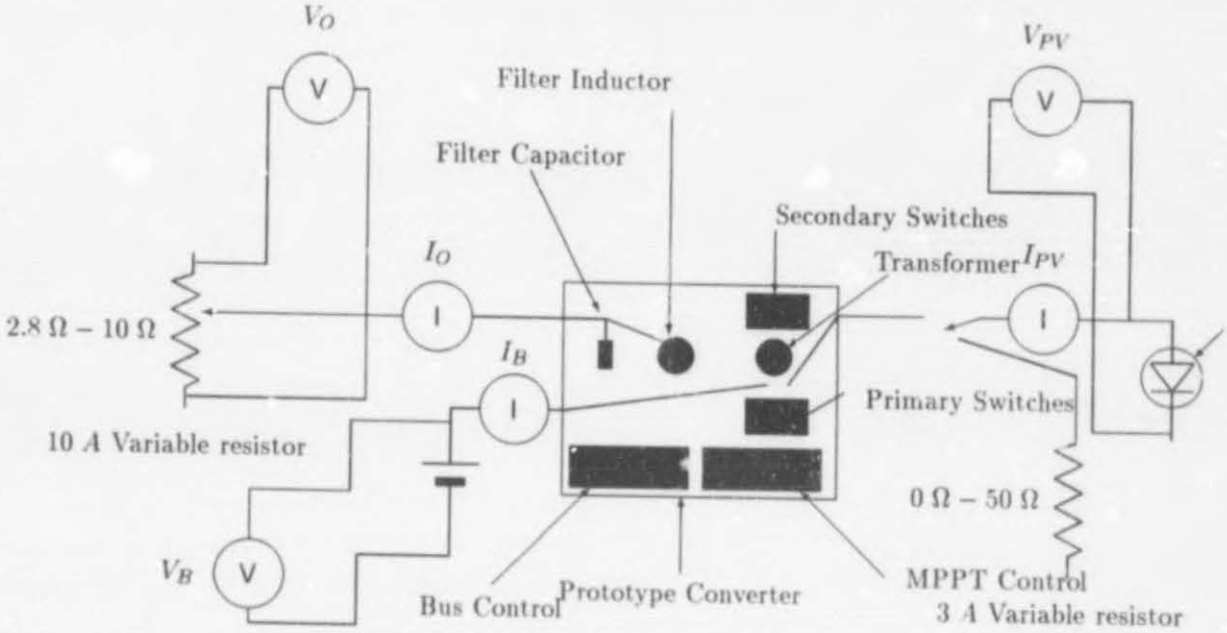

Figure 4.8: Practical arrangement for measuring MPPT

Test	I_{PV} [A]	V_{PV} [V]	P_{PV} [W]
1	0.85	30.5	25.9
	0.90	25.7	23.1
	0.80	32.1	25.6
2	0.76	30.2	23.0
	0.76	30.7	22.8
	0.74	31.0	22.9
3	0.72	20.9	21.5
	0.71	30.1	21.4
	0.73	29.0	21.2
	0.71	30.0	21.3
	0.69	31.0	21.4
	0.67	32.0	21.4
4	0.85	30.7	26.1
	0.83	29.0	24.1
	0.78	24.2	24.2
5	0.64	29.5	18.9
	0.63	28.0	17.6
	0.60	30.7	18.0

Table 4.1: MPPT Measurements

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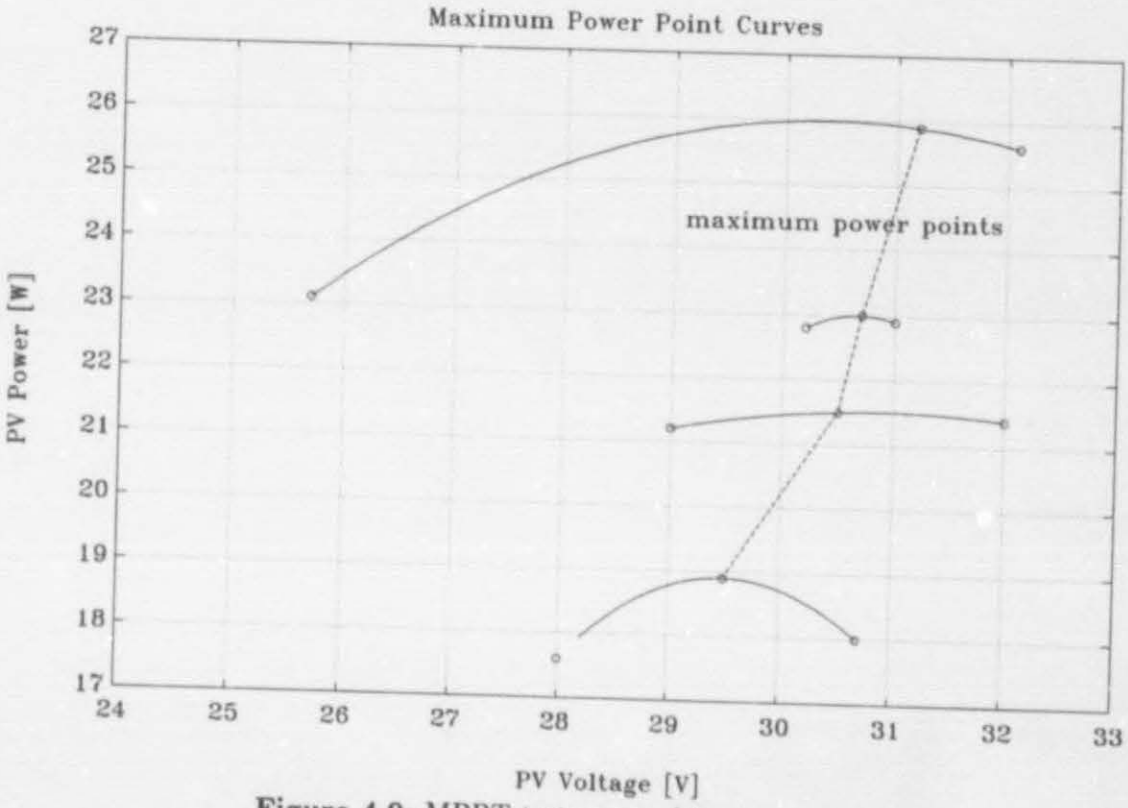

Figure 4.9: MPPT testcurves of the converter

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4.4 Efficiency Measurements

4.4.1 Practical Arrangement

The practical arrangement for measuring the efficiency of the converter is shown in Fig. 4.10.

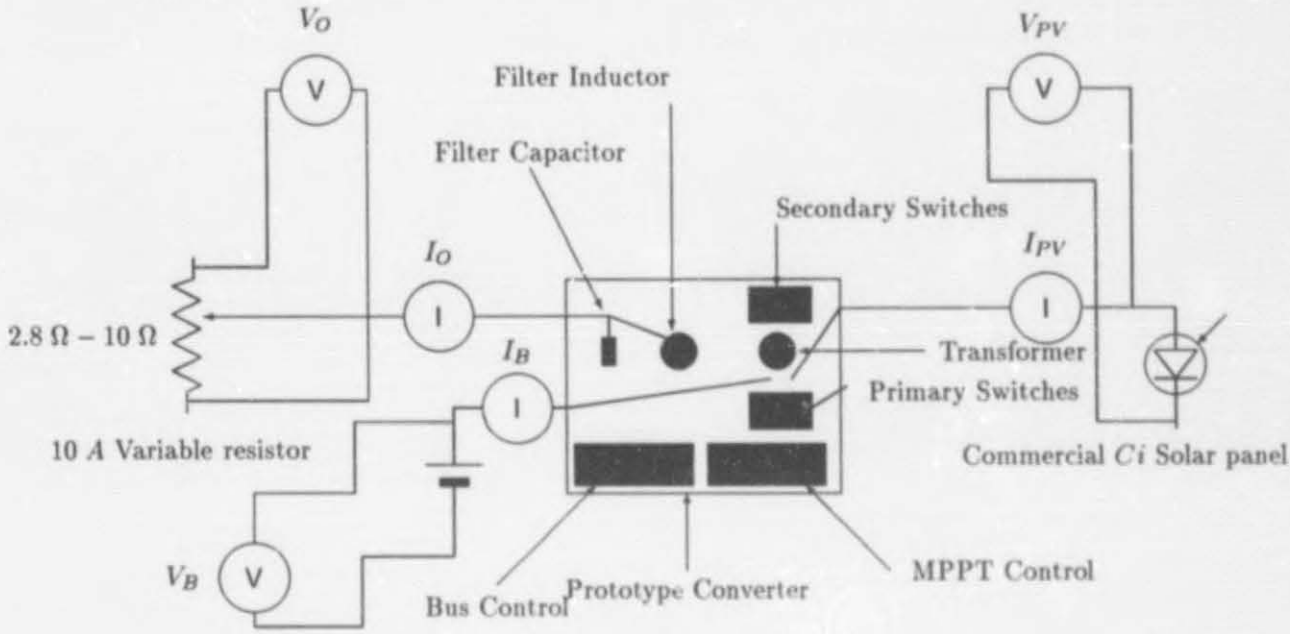

Figure 4.10: Practical arrangement for measuring efficiency

4.4.2 Test Results

Table 4.3 represents the efficiency of the compound converter in different conditions of load current and battery current. η_1 is the actual efficiency and η_2 is the efficiency of the converter when the losses in the control circuitry are ignored. It is evident that the control circuit has a great influence on the efficiency.

Fig. 4.11 shows an efficiency curve of the converter. It can be seen that the efficiency decreases with a decreasing battery current. Normally the efficiency increases with higher output power. This is what causes the sudden rise in efficiency as shown on the curve.

To improve on the present design of the compound converter in terms of efficiency, it is important to know where the losses occur in the circuit. The losses can be grouped in power electronic losses and control losses. In previous chapters some predictions were made for certain losses. The losses were measured at critical places in the cicuit with a 40 W load. These results are shown in Table 4.3.

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I_B	P_B	I_L	P_L	I_{PV}	V_{PV}	P_{PV}	P_O	η_1	η_2
0.50	7.50	2.0	28.0	1.40	33	46.2	35.5	76.8	85.5
0.75	11.25	1.6	22.4	1.35	32	43.2	33.7	77.9	87.3
1.00	15.00	1.3	18.2	1.32	33	43.6	33.2	76.2	85.3
1.25	18.75	1.0	14.0	1.30	35	45.5	32.8	72.0	81.0
1.50	22.50	0.6	8.4	1.22	35	42.7	30.9	72.4	81.7
1.75	26.25	0.2	2.8	1.14	35	39.9	29.0	72.7	82.7

Table 4.2: Efficiency Measurements

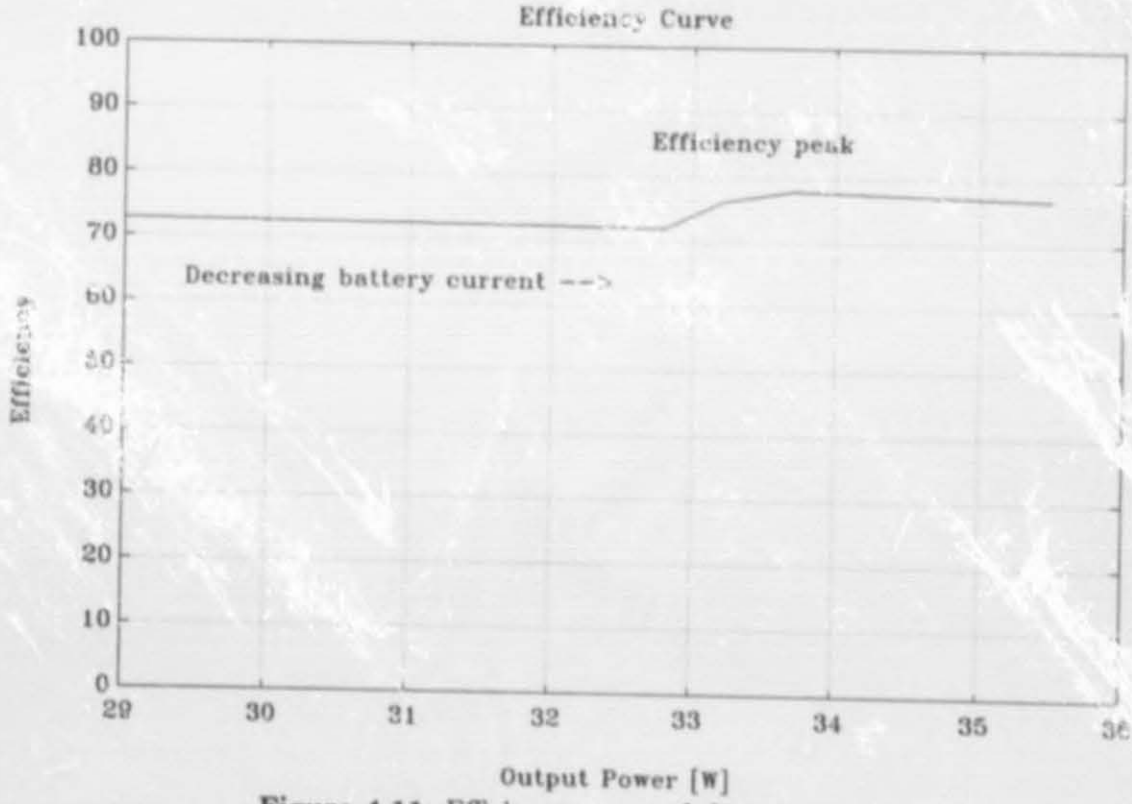

Figure 4.11: Efficiency curves of the converter

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Description	Losses [W]
Supply power for UC1846 IC's	$0.42 \times 2\ W$
Supply power for a LEM modules	$1.2 \times 2\ W$
Primary diode losses	$2.25\ W$
Secondary diode losses	$1.75\ W$
Primary FET conduction losses	$1.5\ W$
Secondary FET conduction losses	$2\ W$
Primary FET switching losses	$1.25\ W$
Secondary FET switching losses	$1.75\ W$

Table 4.3: Loss-measurements

4.5 Noise Measurements

The noise measurements were done using information from [24]. The compound converter, like all switching converters, first transforms a dc input voltage to an ac voltage and then converts the ac voltage back to the desired dc voltage. It generates unwanted signals that can be conducted or transmitted throughout the system. The magnitude of these signals is determined by the frequency of the ac voltage, internal and external filtering, and, at high frequencies (above about 1 MHz), the mounting and connection scheme of the conveter. It is also affected by the nature of the switching topology that generates the signals. In general, pulse-width modulated converters that keep a constant switching frequency create noise in a predictable bandwidth, which can facilitate attenuation. Resonant or zero-switching converters can create less intrinsic noise, but their load-dependent variable switching frequencies tend to generate noise over wide frequency excursions, making them difficult to control. For the compound converter, however, it is important to measure and control the three most significant types of noise:

- Input differential mode noise,
- Input common mode noise,
- Output noise.

The following section briefly defines each type, suggests measurement techniques, and identifies attenuation strategies.

4.5.1 Input Differential Noise

Input differential mode noise is noise current that flows because of a voltage difference between the two input conductors. The input noise of a converter can be modelled as shown in Fig. 4.12(a). The converter switching transistors are simulated by a switch Q_1

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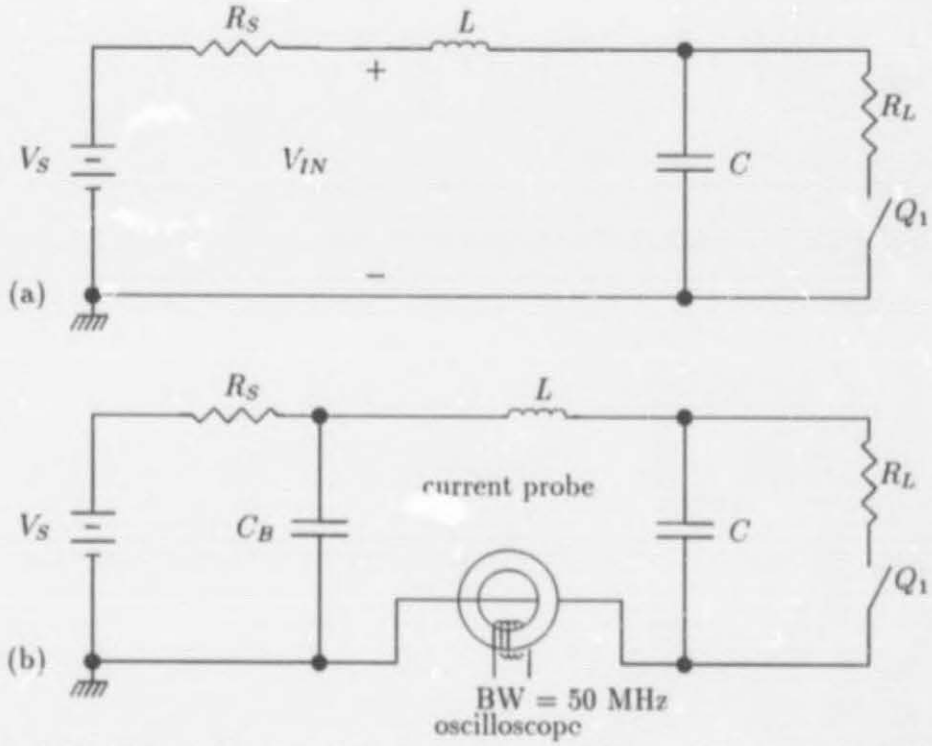

Figure 4.12: Input differential mode noise measurement with (a) voltage probe and with (b) current probe

which turns on and off at the switching frequency of the converter. The load is simulated by a variable resistor R_L which changes with the load. L and C make up an input filter built into the converter.

In the setup of Fig. 4.12(a), a voltage measurement is made across the input terminals of the converter by means of a voltage probe. The quantity measured is the input ripple current times the equivalent source impedance. But to measure the actual ripple current, the source impedance must be known, and source impedances depend on poorly controlled parameters of the components in the output of the source supply. At frequencies above a MHz even placement of wires on the bench will make a significant difference in the measured noise results. If an ideal zero impedance should be used, the measured noise voltage would always be zero, no matter how high the noise current.

More accurate test results can be obtained by the test setup in Fig. 4.12(b). The noise current of the converter is measured directly by means of a current probe; so the source impedance Z_S will make little difference in the current measured. The effects of Z_S are further reduced by the bypass capacitor C_B, which should be a high quality unit with small series inductance and resistance over the frequency band of interest (the switching frequency and above). The connecting wires from C_B to the converter should be as short as possible, to minimize parasitic inductance and radiated noise. If the internal filtering of the converter is not sufficient to attenuate the differential noise to the levels needed in the system, additional LC sections may be added on to the input. The capacitors should

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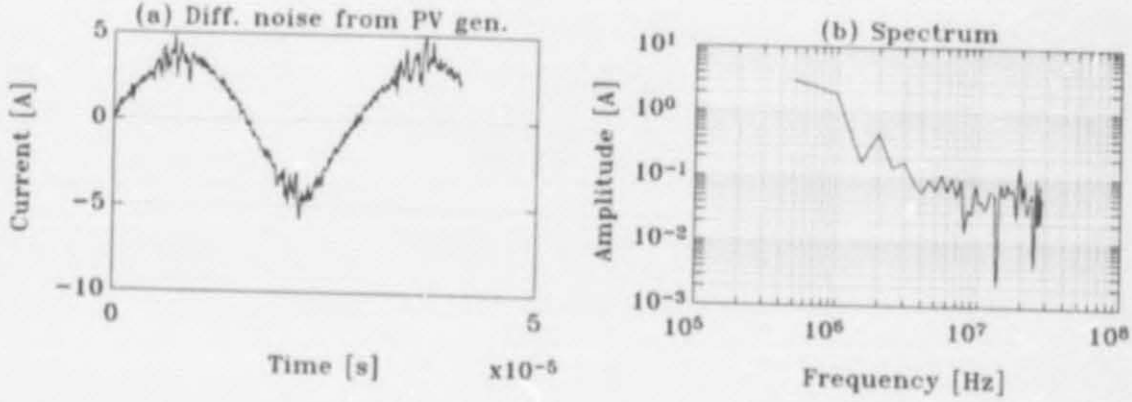

Figure 4.13: (a) Measured input differential mode noise of PV Generator (b) Spectrum of input differential mode noise

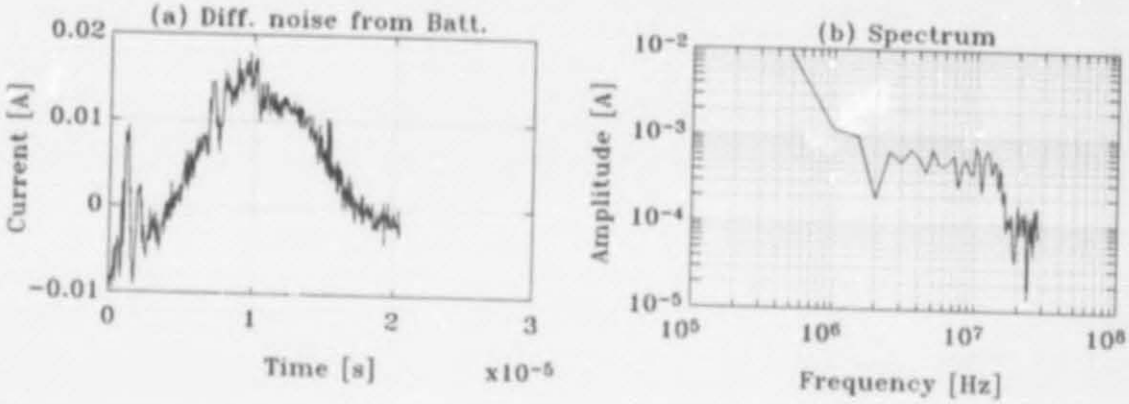

Figure 4.14: (a) Measured input differential mode noise of Battery (b) Spectrum of input differential mode noise

be quality tantalums with low equivalent series resistance (ESR) and equivalent series inductance (ESL) over the frequency band being filtered. Pot cores are typically used for the inductors.

For the filter to work correctly, the Thevenin impedance on the converter side of the filter must be lower than the input impedance of the converter. This is important because all switching power supplies are constant power, negative input impedance devices. As their input voltage goes up, the input current must go down, in order to keep the input power approximately constant. Since the input impedance of the converter is negative and the output impedance of the added filter will be positive, it is possible for them to cancel out to zero at some frequencies and become unstable. The measured waveform for the PV generator is shown in Fig. 4.13(a), with the spectrum in Fig. 4.13(b), and is shown in Fig. 4.14 for the battery as input.

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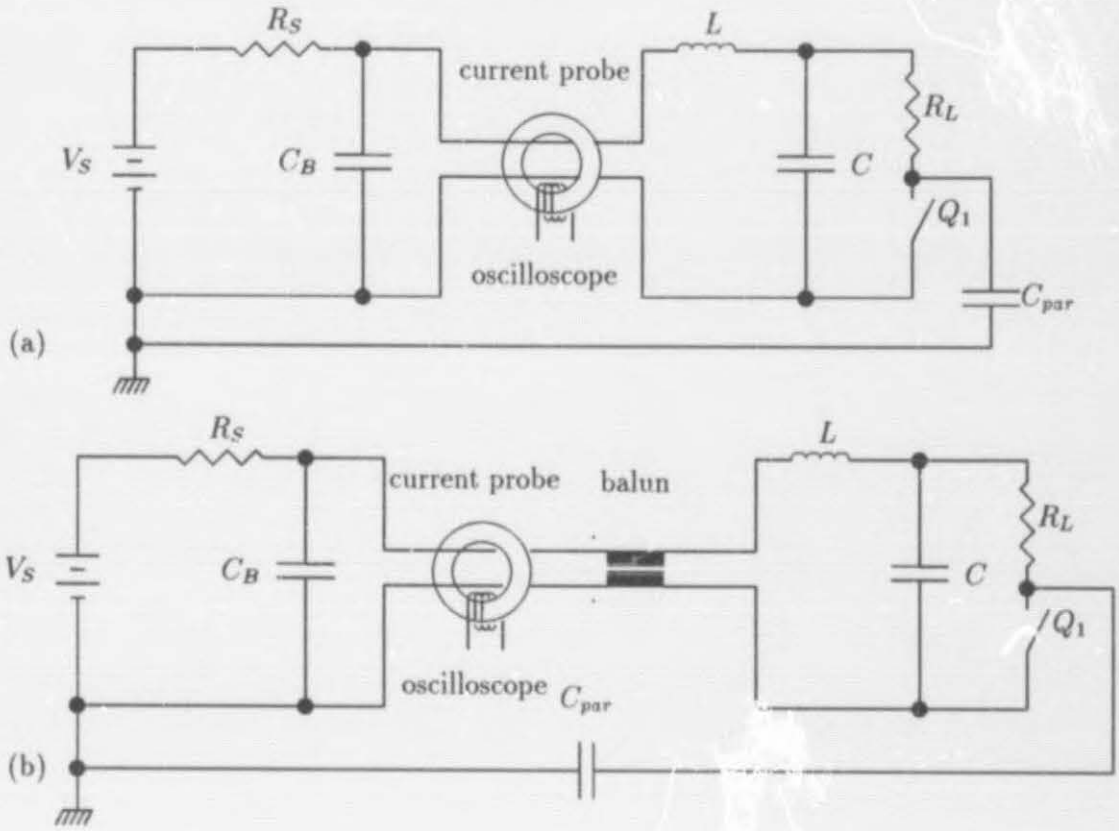

Figure 4.15: (a) Input common mode noise measurement (b) Input common mode noise measurement with balun

4.5.2 Input Common Mode Noise

Fig. 4.15(a) shows how to measure input common mode noise. In the compound converter, switching transistors are mounted in close thermal contact with the chassis, as discussed in Section 3.3.9. To maximize heat transfer, the electrical insulation between the collector or drain of the switching transistor is made as thin as practically possible. This creates a parasitic capacitance from the drain or collector of the transistor to the chassis. When the switch opens or closes, noise current will flow from the switch through the parasitic capacitance, through R_L and C, and then through the ground connection back to the chassis. This noise current is small, but an LC filter in the converter is ineffective against it because the current flows around it instead of through it. The measured waveform is shown in Fig. 4.16(a) for the PV generator as input, with the spectrum in Fig. 4.16(b), and is shown in Fig. 4.17 for the battery as input.

The common mode noise can be filtered with a balun as shown in Fig. 4.15(b). A balun is an inductor with two windings, both with the same number of turns. The balun presents a high inductance to the common mode current, but virtually none to the differential mode current. Note that both the dots on the balun are on the input side of the converter. This

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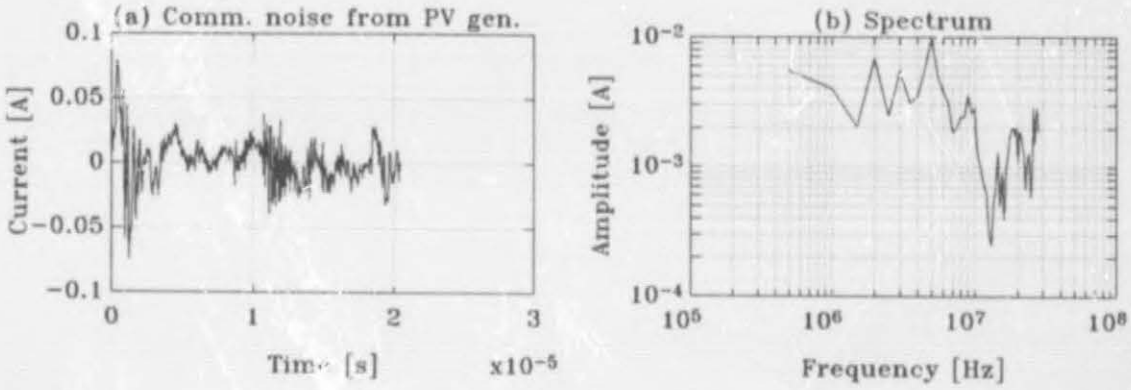

Figure 4.16: (a) Measured input common mode noise of the PV generator, (b) Spectrum of input common mode noise

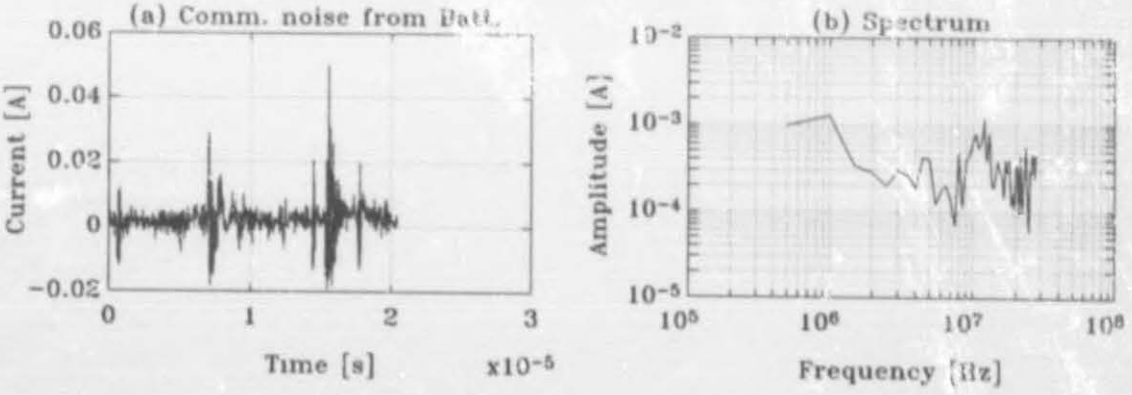

Figure 4.17: (a) Measured input common mode noise with the battery as input, (b) Spectrum of input common mode noise

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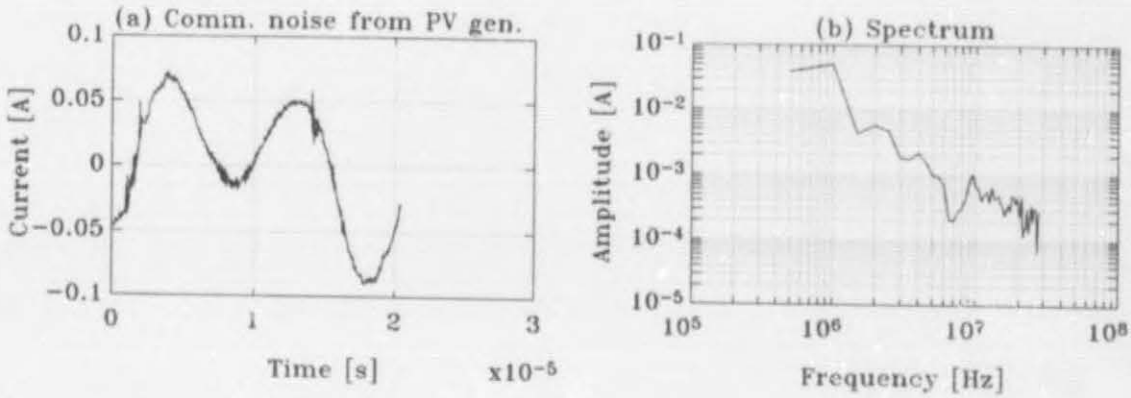

Figure 4.18: (a) Measured input common mode noise of PV generator with balun filter, (b) Spectrum of input common mode noise with balun

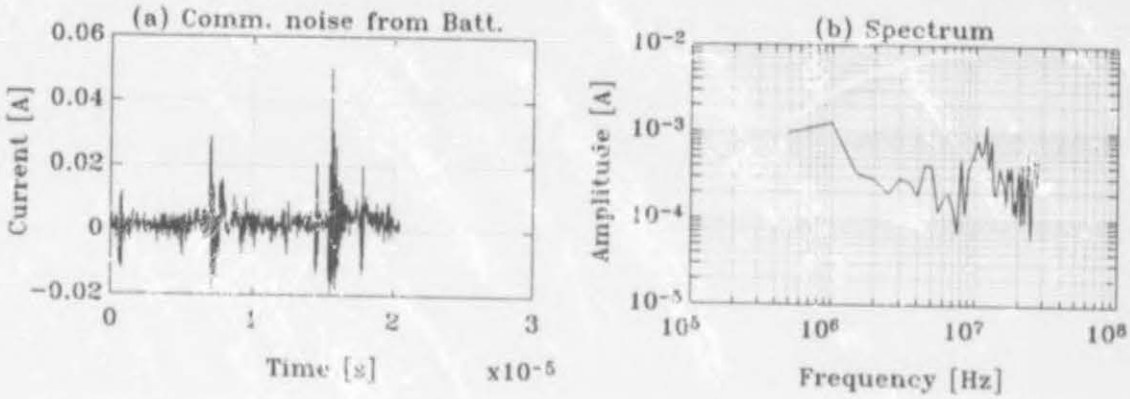

Figure 4.19: (a) Measured input common mode noise of battery with balun filter, (b) Spectrum of input common mode noise with balun

means that the differential current (including the load current) flows into the dot in the top winding and out of the dot on the bottom winding. Since the currents are equal and opposite and the turns in both windings are the same, the net flux in the core caused by the differential current is zero, even though the load current can be very high. As a result a high permeability ungapped core can be used for the balun, and it can have a relatively high common mode inductance with only a few turns. The much smaller common mode noise current flows primarily through the bottom winding and through both windings in the same direction. Thus the balun represents a high impedance to common mode noise currents. The measured waveform for the is shown in Fig. 4.18(a) PV generator, with the spectrum in Fig. 4.18(b), and is shown in Fig. 4.19 for the battery as input.

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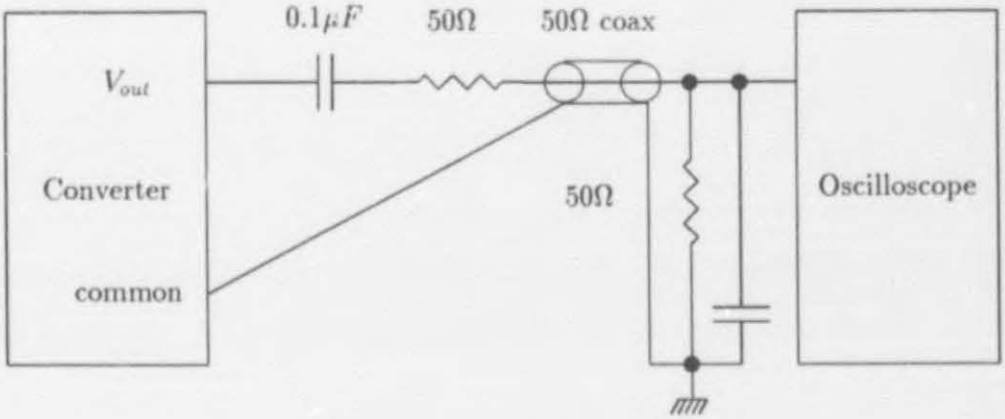

Figure 4.20: Output Noise Measurement

4.5.3 Output Noise

Output ripple voltage measurements are difficult to make, even under the best conditions. Depending on the techniques used, results may vary widely.

As with input noise current, there are two components of output voltage ripple: differential and common mode. Common mode is usually dominated by current conducted through stray capacitances to the supply line. It is of little interest in most power designs, but it does cause problems when measuring output ripple. The common mode component may have a bandwidth of several 10 MHz, an area where most oscilloscopes have poor common mode rejection. As a result, common mode noise may appear as differential noise. Consequently, when measuring output differential noise, it is best to connect input and output commons to the case, and to use the case as a single point ground for all test equipment, in order to minimize common mode interference.

The output differential noise is the noise voltage that appears between the two output terminals. The method used to measure differential output ripple is shown in Fig. 4.20. To reduce the pickup of radiated noise, the measurement must be carried out at the converter . The 50 Ω coaxial cable, lead lengths (including the ground lead) must be as short as possible, in order to reduce the pickup of radiated noise. A parallel capacitance of 2700 pF at the scope reduces the bandwidth to approximately 2 MHz to permit viewing of the fundamental frequency component of the ripple. The measured waveform is shown in Fig. 4.21.

If the internal output filtering of the converter is not sufficient to bring the noise levels within system requirements, additonal LC sections may be added on to the output. Like the input filter, the capacitors should be quality tantalums with low equivalent series resistance (ESR) and equivalent series inductance (ESL) over the frequency band being filtered. Such a filter has already been designed for the distributed regulator of the communications tray. If the noise on the bus causes any problems additional filters will be used.

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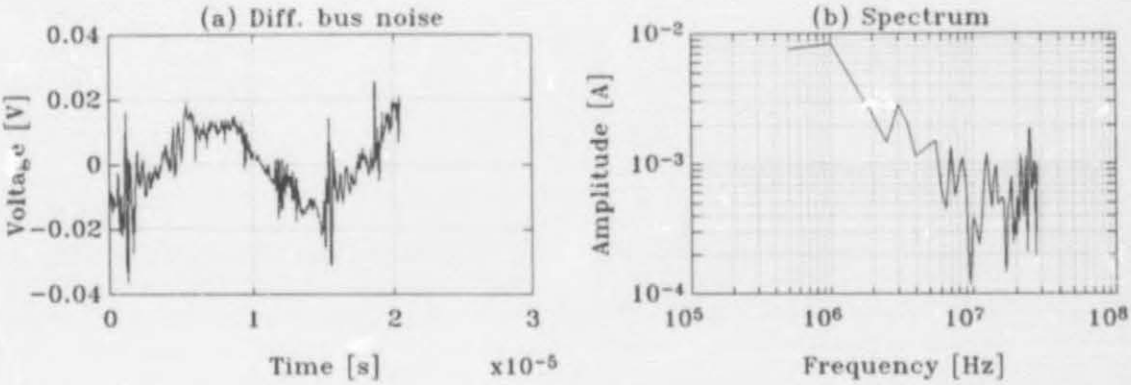

Figure 4.21: (a) Measured output noise (b) Spectrum of output noise

4.6 Mechanical Tests

Temperature and vacuum tests have been done on another converter in [38]. These tests will be done on the compound converter as well, at a later stage. Vibration testing facilities are available in the laboratories of Houwtec. These facilities will be used for vibration tests. It is especially important to see if the magnetic components will survive these tests.

4.7 Summary

In this chapter some of the main circuit waveforms were given. The waveforms correspond well with those predicted in previous chapters. Reasons were also given for differences.

Some results of the maximum power point tracker were also given. From these results it is almost certain that the MPPT will work for Sunsat. The results in this report were, however, done with commercial solar panels.

The efficiency is not as high as predicted, because of the high power consumption of the control circuit.

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Chapter 5

Conclusions and Recommendations

The prototype system was analyzed, designed and constructed. Several tests have been done on it, which led to the following conclusions:

- The converter is small in size and mass. It therefore does not occupy much space and mass on the satellite.
- Peak-current control gives it a good transient response.
- The power electronic part of the converter has very low losses. There is a 10% increase in efficiency over cascaded systems. The control, however, has high power losses. For future work on this project, it is recommended that the control circuit should be built by selecting components more carefully. The principles, however, can stay the same.
- The efficiency can be further improved by using more p-channel MOSFETs in parallel in the secondary control, because their on-resistance is somewhat higher than that of the n-channel MOSFETs.
- In the prototype it was difficult to minimize the influence of the parisitic components on the measurements. In the future they should be prevented in the circuit layout.
- The compound converter is a good idea for satellite power systems, but needs more refinement. It is recommended that the main regulator of the engineering model should be a shunt regulator.
- The battery should be protected more carefully.

A design review with experts on space power systems from ECS was held, which led to the following conclusions:

- The power switches throughout the satellite must be duplicated with a different technology. At the moment only p-channel MOSFETs are used. Solid-state relays can also be incorporated, but it is very expensive.

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- The gates of all the MOSFETs must be protected by means of zener diodes.
- Metal and ceramic components should be used instead of plastics, because damping is a very important constraint for an optical payload.
- The charging of batteries before launching is important.
- The power must be disconnected from the system during launching.
- The way in which the power will be switched on is important.
- Diodes should not be used as voltage references, because it is thermal unstable.

Recommendations for the Sunsat Power System:

At this stage it is evident that the best option for the Sunsat Power System is a simple, reliable topology which will protect the BU very carefully.

The battery management system on board the satellite should automatically protect the batteries and cells against open circuit failures, undervoltage, overvoltage, over-temperature and over-pressure [14].

The parameters used to indicate the state of charge of the battery are cell voltage, temperature and pressure. Two of these parameters are usually used to determine the end of charge criteria; however, all three parameters are interdependent. The battery mounting platform temperature varies with mission phases, seasonal changes and operational modes, and if cell failures and degradation are taken into account it is very difficult to set the end-of-charge criteria precisely, prior to launch. Programmable end of charge levels are preferred. Battery end-of-charge and overcharge protection levels must be high enough to ensure that the battery can be fully charged and low enough to prevent overcharging. The stability of the protection levels is critical, and where feasible it should be possible to inhibit them in case of failure [14].

It is suggested that a shunt regulation concept be used for battery protection, as shown in Fig. G.17 for the +X and -X panels, and Fig. G.18 for the +Y and -Y panels (App. G). The reason why opposite panels are connected is that only one can supply power at a time, and that therefore the single MOSFETs will never have to work twice as hard.

In these diagrams only show the power electronic part of the regulation. The control is done via the CONT1 to CONT5 ports. Note that the panels, battery and load is directly connected, with no regulation inbetween. The reliability is further increased by disconnecting the five strings from one another.

The charge-current is reduced by short-circuiting enough strings of the PV generator. If the battery is fully charged, only one string will be used and the battery will be trickle-charged.

In case of a short-circuit failure, the battery is disconnected by the diodes. The diodes are therefore very important, and enough redundancy is provided to prevent any failures. The telemetry sense resistors will be made up with enough parallel paths for power flow.

Stellenbosch University https://scholar.sun.ac.za

References

Journal and Conference Publications

[1] HJ Beukes, KE Dowson, JHR Enslin, "Simulation and Analysis of the Stellenbosch University Satellite (Sunsat) Power System", *Proceedings of IEEE AFRICON'92*, Sept 1992, pp 221–224

[2] HJ Beukes, KE Dowson, JHR Enslin, "Simulation program for Stellenbosch University Satellite (Sunsat) power system", *The Transactions of the South African Institude of Electrical Engineers*, Vol 84, No 1, March 1993, pp 32–36

[3] HJ Beukes, JHR Enslin, "Analysis of a New Compound Converter as MPPT, Battery Regulator and Bus Regulator for Satellite Power Systems", *Proceedings of IEEE PESC'93*, June 1993, pp 846–852

[4] M Bauzguenda, S Rahman, "Energy Management Onboard the Space Station — A Rule-Based Approach",*IEEE Trans on Aerospace and Electronic Systems*, Vol 27, No 2, March 1992, pp 302-310

[5] W Burns, A Ohri, "Improving off line converter performance with current-mode control", *Proceedings of Powercon 10*, 1983

[6] A Capel, A Batlle,"Power Distribution System for a Synthetic Aperture Radar",*Proceedings of the European Space Power Conference*, Vol 1, Sept 1991, pp 115–129

[7] WD Cook, "Small Satellite Nickel Hydrogen Power Applications", *Eagle Picher Industries, Inc.*, 1992

[8] A Duchene, B Lacore,"The Hermes Spaceplane Power Subsystem Conditioning and Distribution",*Proceedings of the European Space Power Conference*, Vol 1, Sept 1991, pp 257–290

[9] JHR Enslin, DB Snyman, "Combined Low-Cost, High-Efficient Inverter, Peak Power Tracker and Regulator for PV Applications", *IEEE Transactions on Power Electronics*, Vol.6, No.1, Jan. 1991, pp 73–82

[10] JHR Enslin, DB Snyman, "Simplified Feed-Forward Control of the Maximum Power Point in PV Installations", *Proceedings of IECON'92*, Nov. 1992, pp 542–547

[11] P Galantini, M Lombardo,"The SAX Electrical Power Subsystem",*Proceedings of the European Space Power Conference*, Vol 1, Sept 1991, pp 131–136

Stellenbosch University https://scholar.sun.ac.za

[12] S Hsu, A Brown, L Rensink, RD Middlebrook, "Modelling and analysis of switching dc-to-dc converters in constant frequency current-programmed mode", *Proceedings of IEEE-PESC*, 1979, pp 284–301

[13] GC Klein, DF Schmidt, "Current and emerging technology for powering small satellites with secondary cells and batteries", *Proceedings of the 7th Annual AIAA/USU Conference on Small Satellites*, Sept 1993, pp 1–14

[14] D Levins, "Protection Consepts used in Spacecraft Power Systems",*Proceedings of the European Space Power Conference*, Sept 1991, pp 157–162

[15] DF Pickett, "Progress in Battery Technology since the First CSULB Annual Battery Conference and Prospects for the Future", *IEEE AES Magezine*, April 1992, pp 6–8

[16] R Redl, NO Sokal, "Near-optimum dynamic regulation of dc-dc converters using feed-forward of output current and input voltage with current-mode control", *IEEE Trans on Power Electronics*, PE-1, no 3, 1986, pp 181–192

[17] JJ Schoeman, JD van Wyk, "A simplified maximal power controller for terrestrial photovoltaic panel arrays", *IEEE PESC-82 Rec.*, 1982, pp 361–367

[18] JJ Smithrick, SW Hall, "Effect of KOH Concentration on LEO Cycle Life of IPV Nickel-Hydrogen Flight Cell Update II", *IEEE AES Magezine*, April 1992, pp 9–13

[19] CR Sullivan, MJ Powers, "A High-Efficiency Maximum Power Point Tracker for Photovoltaic Arrays in a Solar-Powered Race Vehicle", *Proceedings of IEEE PESC'93*, June 1993, pp 574–580

[20] PJ Wolfs, C Kwong, GF Ledwich, "A single-phase converter with a high-frequency current sourced link",*IEEE Trans on Power Electronics*, Vol 7, No 4, Oct. 1992, pp 683–692

[21] DB Snyman, JHR Enslin, "Analysis and Experimental Evaluation of a New MPPT Converter Topology for PV Installations", *Proceedings of IECON'92*, Nov. 1992, pp 548–553

Textbooks, Magazines, Databooks and Reference Manuals

[22] J Coetzee, "Satellietstryd in SA", Finansies & Tegniek, 7 Aug. 1992, pp 26

[23] Power MOSFETs, Harris Semiconductors, 1991, pp 4-289–4-293

[24] "Designing with a distributed-power architecture", Interpoint catalog, 1992

[25] JS Jones, "Sunsat Unveiled", Space, Vol 7, No 5, Sept. 1991

[26] G Milne, "Satellite technology in South Africa", Dataweek, 17 Jan. 1992, pp 17–18

Stellenbosch University https://scholar.sun.ac.za

[27] N Mohan, TM Undeland, WP Robbins, "Power Electronics: Converters, Applications and Design", Wiley, New York, 1989

[28] National, Linear Data Book, 1988

[29] Philips, Components and Materials, Part 4, 1981

[30] P Questad, "Designing with a Distributed Power Architecture", Interpoint Power Conversion Products, 1992

[31] Simuwin Users Manual, Department of Electrical and Electronic Engineering, University of Stellenbosch, Version 1.00, July 1993

[32] IR Sinclair, "Passive Components: a user's guide" Heinemann Newnes, Oxford, 1990

[33] Unitrode, International Semiconductor Data Book, 1984–85

Internal Reports

[34] HJ Beukes, Analysis, design and construction of a current-fed push-pull dc/dc regulator for Sunsat

[35] HJ Beukes, Distributed Regulators in the Sunsat Power System, Febr. 1993

[36] HJ Beukes, First Design of Battery Unit, Febr. 1993

[37] HJ Beukes, Power Simulation, May 1992

[38] HJ Beukes, Testing of Vicor Regulator, Nov. 1992

[39] R de Villiers, "Kubernetika 823", Sept. 1993

[40] ML Englington, Initial Thermal Modeling for Sunsat, March 1993

[41] Sunsat Technical Specifications, Aug. 1992

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Appendix A

Power System Functional Diagram

The functional diagram of the Sunsat Power System (SPS) is shown in Fig. A.1. The dashed blocks represent different trays. The energy is supplied by the 4 PV panels on the outside panels, which form the PV Generator. This is connected to the main regulator unit (MRU) on the P&O tray. The MRU consists of two regulators, A and B, which supply two +14 V busses, $+14V_A$ and $+14V_B$, to the other satellite trays. These regulators are also connected to the battery unit (BU) for energy backup. On each tray the two power buses are connected via diodes. From here the voltage is filtered and regulated to the desired voltage level for each application.

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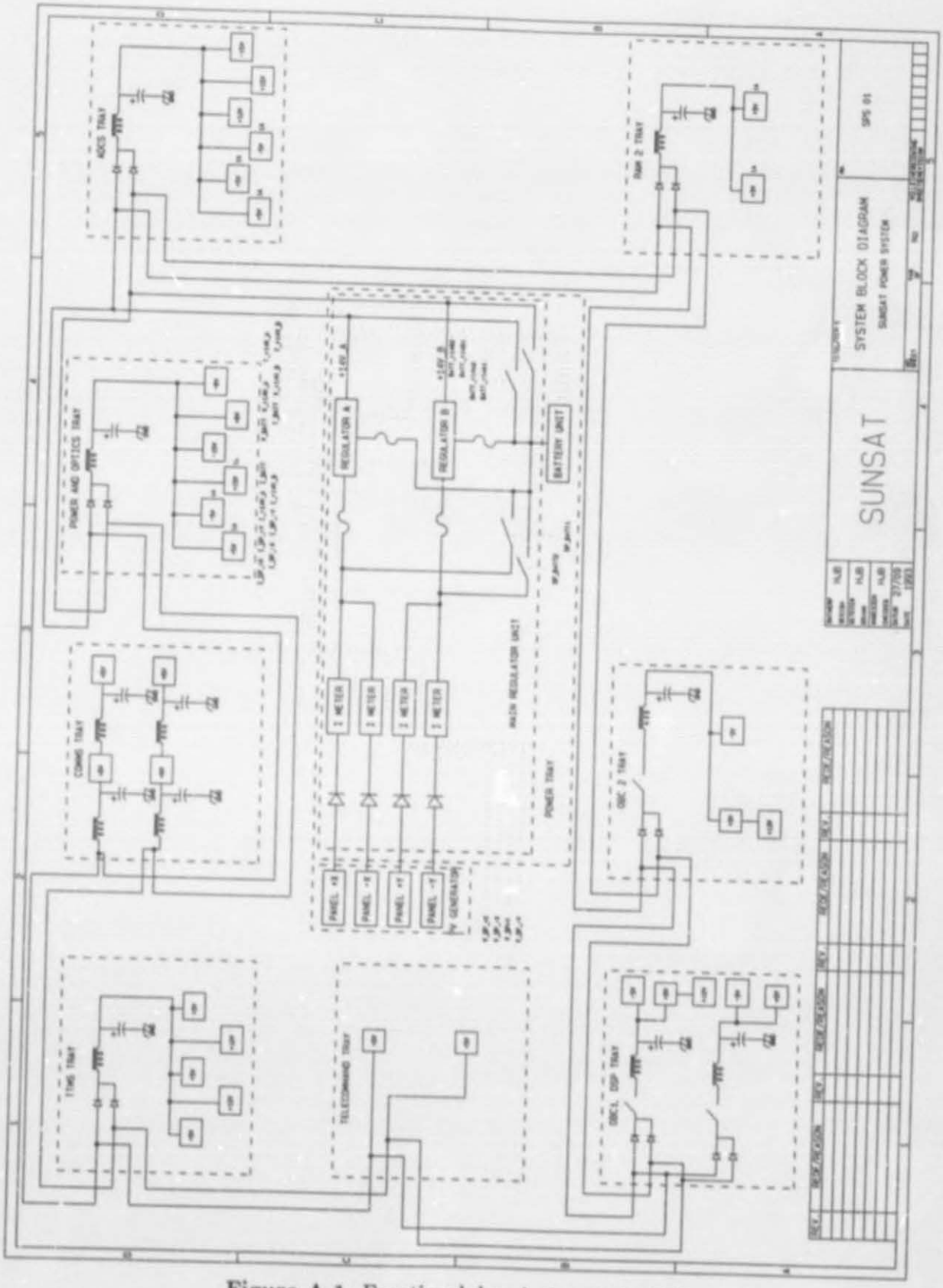

Figure A.1: Functional description of the SPS

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Appendix B

PV Generator Specifications

Scope

This specification gives characteristic and performance requirements for each of four identical panels which, unless otherwise specified, shall be met under all lab integration and space environmental conditions until ten years after launch.

Location and purpose

The solar panels are mounted externally on the +X (front), -X (back), +Y (right) and -Y (left) panels of the satellite. Their purpose is to supply electrical energy to the the satellite through the main regulation unit. Each panel contains a torque coil which is used by the attitude control system. The panels also provide thermal isolation of the internals of the satellite from the space environment and provide some radiation shielding.

Functional description

- The panels generate power when illuminated by the sun.
- Temperature is sensed for telemetry purposes.
- The torque coils generate a magnetic movement when energised.

Characteristics

Design requirements

The solar panels shall have the following major characteristics:

1. High energy conversion efficiency
2. Reliability
3. Slow degradation in relation to radiation

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Absorbtivity

The absorbtion capacity in relation to the solar spectrum shall be $0.8 < \alpha < 0.85$

Emissivity

The emissivity relative to a block body at the same surface temperature shall be $0.8 < \sigma < 0.85$

Torque coil

Each panel shall contain a torque coil. It shall be

- wound into a channel (0.43×0.43 $m$tube of1×1 cm) at the edge of the solar array substrate panels,
- contain 100 turns of 30 AWG (0.5 mm diameter) silver plate copper, KYNAR covered, single strand wire
- have a resistance at 25°C of $40\ \Omega < R < 60\ \Omega$

Temperature Sensing

The centre temperature of each panel shall be sensed. The temperature of the upper left corner and the upper middle of panel +X shall be sensed. Four temperature sensing points are available for supplier data.

Performance

Power output

Each solar panel shall provide at least 30 W of peak power at 1 SC (solar constant), AM0 (air mass zero), 25°C, BOL and 25 W at EOL (5 years).

Maximum power point voltage

There shall be sufficient solar cells in a string to provide a maximum power point voltage of at least 20 V (average 24 V) under all conditions.

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Efficiency

The solar cells shall have a rated efficiency of at least 14%.

Temperature sensor accuracy

Temperature sensor errors from −40°C to +60°C shall be less than 3°C.

Electrical interfaces

A D-subminiature connector socket with 15 contacts is used at the bottom of panel +X with signals as follows:

Pin	Signal	I/O	V	Tolerance	Rise time	Description
1	GND	I	0	0-0	NA	earth
2	+XS1	O	24	20-36	NA	power output for string 1
3	+XS2	O	24	20-36	NA	power output for string 2
4	+XS3	O	24	20-36	NA	power output for string 3
5	+XS4	O	24	20-36	NA	power output for string 4
6	+XS5	O	24	20-36	NA	power output for string 5
7	GND	I	0	0-0	NA	earth
8	GND	I	0	0-0	NA	earth
9	GND	I	0	0-0	NA	earth
10	+XS1	O	24	20-36	NA	power output for string 1
11	+XS2	O	24	20-36	NA	power output for string 2
12	+XS3	O	24	20-36	NA	power output for string 3
13	+XS4	O	24	20-36	NA	power output for string 4
14	+XS5	O	24	20-36	NA	power output for string 5
15	GND	I	0	0-0	NA	earth

A D-subminiature connector socket with 15 contacts is used at the bottom of panel -X with signals as follows:

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Pin	Signal	I/O	V	Tolerance	Rise time	Description
1	GND	I	0	0-0	NA	earth
2	-XS1	O	24	20-36	NA	power output for string 1
3	-XS2	O	24	20-36	NA	power output for string 2
4	-XS3	O	24	20-36	NA	power output for string 3
5	-XS4	O	24	20-36	NA	power output for string 4
6	-XS5	O	24	20-36	NA	power output for string 5
7	GND	I	0	0-0	NA	earth
8	GND	I	0	0-0	NA	earth
9	GND	I	0	0-0	NA	earth
10	-XS1	O	24	20-36	NA	power output for string 1
11	-XS2	O	24	20-36	NA	power output for string 2
12	-XS3	O	24	20-36	NA	power output for string 3
13	-XS4	O	24	20-36	NA	power output for string 4
14	-XS5	O	24	20-36	NA	power output for string 5
15	GND	I	0	0-0	NA	earth

A D-subminiature connector socket with 15 contacts is used at the bottom of panel +Y with signals as follows:

Pin	Signal	I/O	V	Tolerance	Rise time	Description
1	GND	I	0	0-0	NA	earth
2	+YS1	O	24	20-36	NA	power output for string 1
3	+YS2	O	24	20-36	NA	power output for string 2
4	+YS3	O	24	20-36	NA	power output for string 3
5	+YS4	O	24	20-36	NA	power output for string 4
6	+YS5	O	24	20-36	NA	power output for string 5
7	GND	I	0	0-0	NA	earth
8	GND	I	0	0-0	NA	earth
9	GND	I	0	0-0	NA	earth
10	+YS1	O	24	20-36	NA	power output for string 1
11	+YS2	O	24	20-36	NA	power output for string 2
12	+YS3	O	24	20-36	NA	power output for string 3
13	+YS4	O	24	20-36	NA	power output for string 4
14	+YS5	O	24	20-36	NA	power output for string 5
15	GND	I	0	0-0	NA	earth

A D-subminiature connector socket with 15 contacts is used at the bottom of panel -Y with signals as follows:

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Pin	Signal	I/O	V	Tolerance	Rise time	Description
1	GND	I	0	0-0	NA	earth
2	-YS1	O	24	20-36	NA	power output for string 1
3	-YS2	O	24	20-36	NA	power output for string 2
4	-YS3	O	24	20-36	NA	power output for string 3
5	-YS4	O	24	20-36	NA	power output for string 4
6	-YS5	O	24	20-36	NA	power output for string 5
7	GND	I	0	0-0	NA	earth
8	GND	I	0	0-0	NA	earth
9	GND	I	0	0-0	NA	earth
10	-YS1	O	24	20-36	NA	power output for string 1
11	-YS2	O	24	20-36	NA	power output for string 2
12	-YS3	O	24	20-36	NA	power output for string 3
13	-YS4	O	24	20-36	NA	power output for string 4
14	-YS5	O	24	20-36	NA	power output for string 5
15	GND	I	0	0-0	NA	earth

A D-subminiature connector socket with 15 contacts is used at the top of the +X panel for the torque coil inputs and temperature outputs on the ADCS tray as follows:

Pin	Signal	I/O	V	Tolerance	Rise time	Description
1-4	+XTCA	I	14	10-16	3 ms	torque coil input A
12-15	+XTCB	I	14	10-16	3 ms	torque coil input B
5,6	+XTC	I	5	5-5	1 μs	centre temperature sensor
7,8	+XTL	I	5	5-5	1 μs	corner temperature sensor
9,10	+XTE	I	5	5-5	1 μs	edge temperature sensor
11	GND	I	0	0-0	NA	earth

A D-subminiature connector socket with 15 contacts is used at the top of the -X panel for the torque coil inputs and temperature outputs on the ADCS tray as follows:

Pin	Signal	I/O	V	Tolerance	Rise time	Description
1-4	-XTCA	I	14	10-16	3 ms	torque coil input A
12-15	-XTCB	I	14	10-16	3 ms	torque coil input B
5,6	-XTC	I	5	5-5	1 μs	centre temperature sensor
11	GND	I	0	0-0	NA	earth

A D-subminiature connector socket with 15 contacts is used at the top of the +Y panel for the torque coil inputs and temperature outputs on the ADCS tray as follows:

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Pin	Signal	I/O	V	Tolerance	Rise time	Description
1-4	+YTCA	I	14	10-16	3 ms	torque coil input A
12-15	+YTCB	I	14	10-16	3 ms	torque coil input B
5,6	+YTC	I	5	5-5	1 μs	centre temperature sensor
7	+YTGA	I	5	5-5	1 μs	gradient temperature sensor A
8	+YTGB	I	5	5-5	1 μs	gradient temperature sensor B
9	+YTGC	I	5	5-5	1 μs	gradient temperature sensor C
10	+YTGD	I	5	5-5	1 μs	gradient temperature sensor D
11	GND	I	0	0-0	NA	earth

A D-subminiature connector socket with 15 contacts is used at the top of the -Y panel for the torque coil nputs and temperature outputs on the ADCS tray as follows:

Pin	Signal	I/O	V	Tolerance	Rise time	Description
1-4	-YTCA	I	14	10-16	3 ms	torque coil input A
12-15	-YTCB	I	14	10-16	3 ms	torque coil input B
5,6	-YTC	I	5	5-5	1 μs	centre temperature sensor
11	GND	I	0	0-0	NA	earth

Mechanical parameters and interfaces

The structure of the solar panel is shown in Fig. B.1.

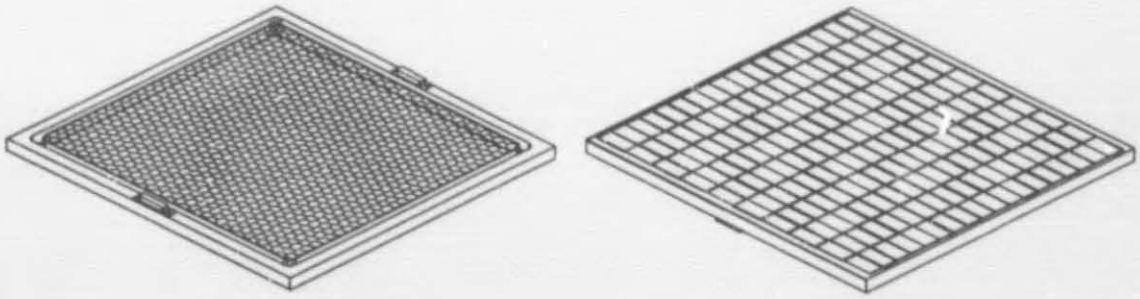

Figure B.1: Structure of Sunsat solar panel Drawn by SED

Mass

The total mass budget per panel is:

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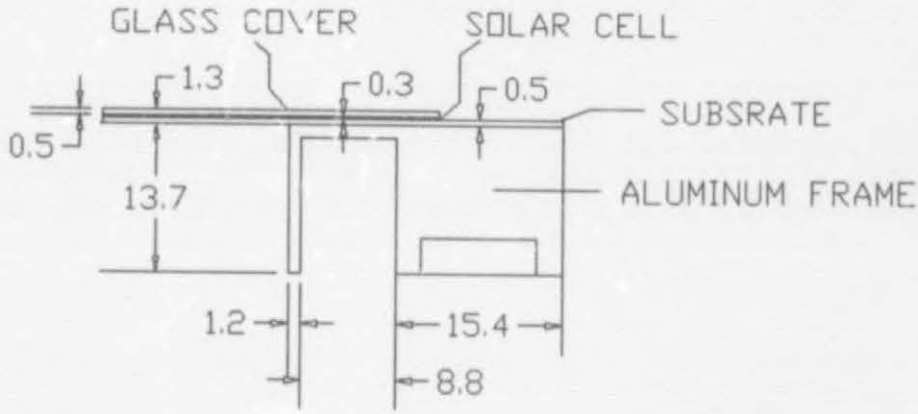

Figure B.2: Side view of the solar panel Drawn by SED

Item	Mass
Solar cells	0.225 kg
Substrate, mechanical	0.625 kg
Electrical components	0.150 kg
Total solar panel	1.000 kg

Dimensions

The dimensions of each solar panel is as follows:

- height = 400 mm
- width = 420 mm
- thickness = 15 mm

as shown in Fig. D.2

The layout of one solar panel is shown in Fig. B.4. The panel consists of 180 cells in 5 strings of 36 serial cells each. The serial connection of cells are as follows:

String	Cells
String 1	A18-B18
String 2	C18-D18
String 3	E18-F18
String 4	G18-H18
String 5	I18-J18

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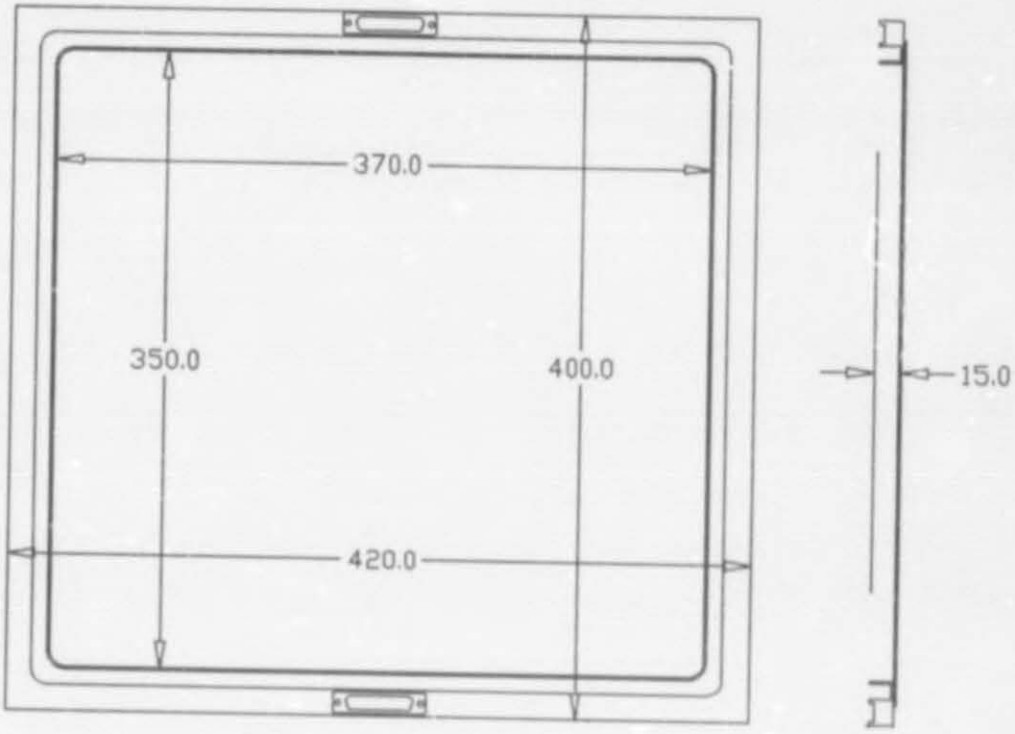

Figure B.3: Dimensions of the solar panel Drawn by SED

Resonant Frequency

The lowest resonant frequency of the panel when attached to the satellite shall be 110 Hz.

Reliability

- The unit shall use parts from the Sunsat Approved Parts List only, or for which approval has been given by the QA officer.
- Parts selection shall include consideration of the vacuum, radiation, and temperature cycling environment the unit will be subjected to.
- Worst case design calculations, including allowance for component tolerance and drift, shall be presented.
- Acceptance tests shall be defined, in order to verify that no detectable malfunctions are present in the unit.
- Development, assembly, and testing of the unit shall comply with the general QA guidelines.

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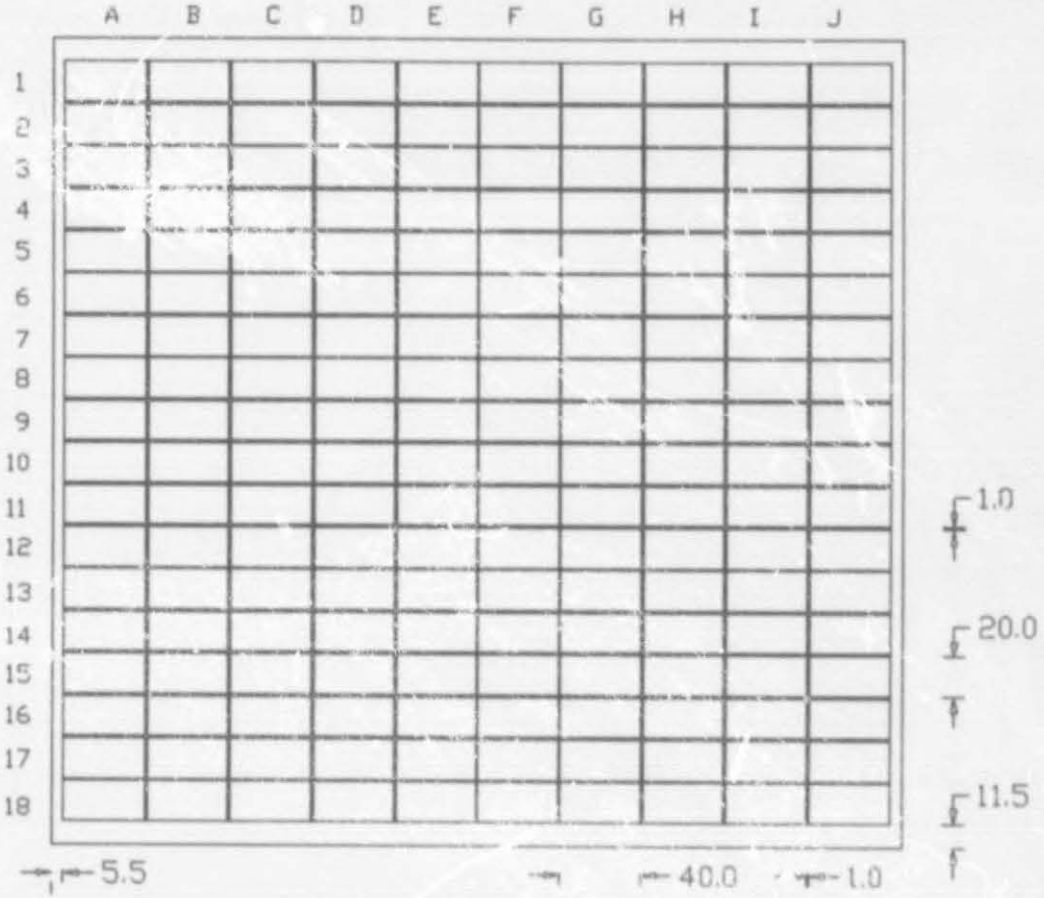

Figure B.4: Layout of the solar panel Drawn by SED

- There may not be any single point failure nodes.
- Each solar panel shall include 5 parallel strings of solar cells for redundancy.

Maintainability

The design of the unit shall make allowance for extensive integration tests.

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Environmental specifications

Temperature

The panels shall operate to specification for 5 years and not fail due to temperature cycling from $-40°C$ to $+55°C$ every 100 minutes for a period of 10 years.

Vibration

The unit shall pass the vibration tests specified in Section 3.13 of the Sunsat specifications [41].

U.V. Stability

The degradation in power output resulting from U.V. illumination shall be less than 30% over 5 years in space.

Shadow/hot-spot protection

Temporary shadowing will not cause permanent cell damage.

Transportability and storage

Reasonable protective panels shall be provided for protection during integration. Each panel shall be supplied in a shock-resistant box able to protect the panel during a drop from any orientation onto concrete from a height of $2\ m$.

Design and construction standards

Design and construction shall be according to accepted good practices. Solar cell welding connections shall be done by using a quality control process. Sufficient test points shall be provided to enable correct operation of all the solar cells.

Materials, processes, parts, surface finishes

All materials selected shall be suitable for space use. Evaporation under vacuum conditions and condensation on optical surfaces is of major concern.

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Electromagnetic compatibility

The unit must operate in conjunction with transmitters and receivers operating at thermal noise limits. Consideration must be given to the possible need for RF bypassing in the panels and RF chokes in the connection leads.

Name plates and markings

Each panel shall be marked as Sunsat panel +X,-X,+Y,-Y and thus identified in all measurements and tests.

Acceptance tests

A full set of acceptance tests shall be defined and executed. The acceptance criteria shall be selected in such a manner that a panel passing the test will meet performance requirements at temperature and life extremes.

The tests include the following:

1. Thermal cycling
2. Thermo-optical properties, including I-V-T curves for each panel
3. U.V. Stability
4. Shadow/hot-spot protection
5. High temperature performance stability
6. Electron/Proton irradiation tests

Qualification

A qualification test programme shall be defined, which over-stresses the qualification model to a sufficient extreme in order to explore potential design weaknesses, and assure that adequate design margins exist. If necessary, the tests shall monitor internal test points.

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Appendix C

Main Regulator Unit Specifications

Scope

This specification gives characteristic and performance requirements of the main regulator unit (MRU) which, unless otherwise specified, shall be met under all lab integration and space environmental conditions until ten years after launch.

Location and purpose

The MRU shall be located between the reaction wheels and the optics on the power and optics tray of the satellite, as shown in Fig. C.1.

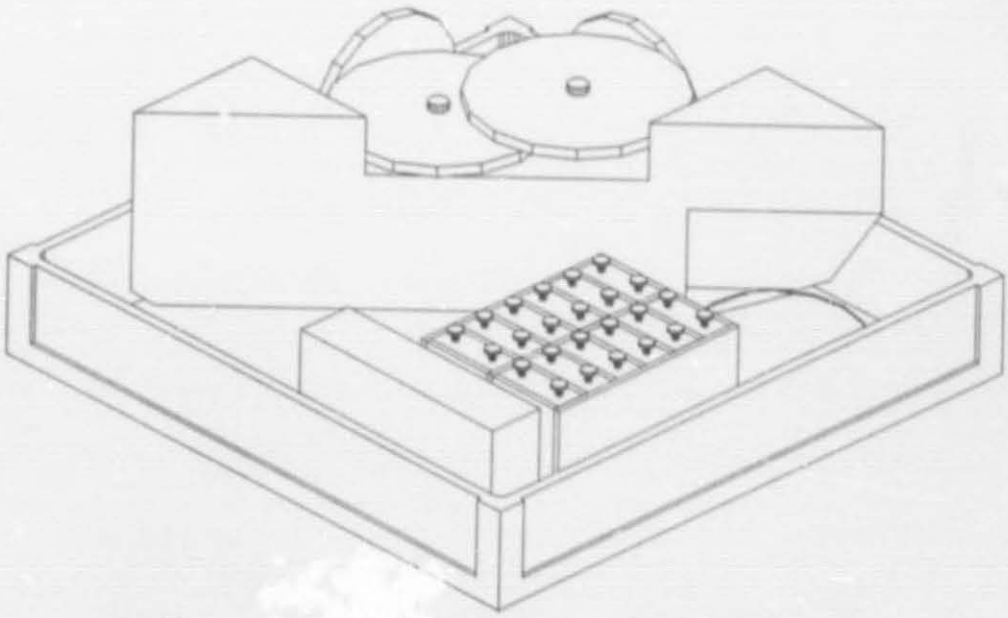

Figure C.1: Power and optics tray Drawn by SED

The purposes of the MRU are the following:

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- To receive the energy from the PV generator
- To supply power to all the subsystems in the form of a +14 V bus
- To store excess energy in battery unit
- To retrieve energy from battery during eclipse

Functional description

The MRU shall receive unregulated energy from the solar panels. The MRU shall consist of:

- A maximum power point tracker (MPPT) to keep the PV voltage at the maximum power point.
- A battery regulator to protect the battery from overcharging.
- A bus voltage regulator, to supply the rest of the subsystems with a regulated voltage.

The MRU shall receive its instructions from the telecommand. Housekeeping signals shall be supplied to the telemetry subsystem.

Characteristics

The MPPT battery charge regulator shall keep the output voltage of the solar panels at the maximum power point voltage.

Performance

Power Output Specifications

The power tray shall be able to supply survival power of 5 W continiously. It shall provide a maximum power of 140 W and an average power of 25 W.

Electrical interfaces

A D-subminiature connector plug with 15 contacts is used for the panel +X input with signals as follows:

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Pin	Signal	I/O	V	Tolerance	Rise time	Description
1	GND	O	0	0-0	NA	earth
2	+XS1	I	24	20-36	NA	power input for string 1
3	+XS2	I	24	20-36	NA	power input for string 2
4	+XS3	I	24	20-36	NA	power input for string 3
5	+XS4	I	24	20-36	NA	power input for string 4
6	+XS5	I	24	20-36	NA	power input for string 5
7	GND	O	0	0-0	NA	earth
8	GND	O	0	0-0	NA	earth
9	GND	O	0	0-0	NA	earth
10	+XS1	I	24	20-36	NA	power input for string 1
11	+XS2	I	24	20-36	NA	power input for string 2
12	+XS3	I	24	20-36	NA	power input for string 3
13	+XS4	I	24	20-36	NA	power input for string 4
14	+XS5	I	24	20-36	NA	power input for string 5
15	GND	O	0	0-0	NA	earth

A D-subminiature connector plug with 15 contacts is used for the panel -X input with signals as follows:

Pin	Signal	I/O	V	Tolerance	Rise time	Description
1	GND	O	0	0-0	NA	earth
2	-XS1	I	24	20-36	NA	power input for string 1
3	-XS2	I	24	20-36	NA	power input for string 2
4	-XS3	I	24	20-36	NA	power input for string 3
5	-XS4	I	24	20-36	NA	power input for string 4
6	-XS5	I	24	20-36	NA	power input for string 5
7	GND	O	0	0-0	NA	earth
8	GND	O	0	0-0	NA	earth
9	GND	O	0	0-0	NA	earth
10	-XS1	I	24	20-36	NA	power input for string 1
11	-XS2	I	24	20-36	NA	power input for string 2
12	-XS3	I	24	20-36	NA	power input for string 3
13	-XS4	I	24	20-36	NA	power input for string 4
14	-XS5	I	24	20-36	NA	power input for string 5
15	GND	O	0	0-0	NA	earth

A D-subminiature connector plug with 15 contacts is used for the panel +Y input with signals as follows:

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Pin	Signal	I/O	V	Tolerance	Rise time	Description
1	GND	O	0	0-0	NA	earth
2	+YS1	I	24	20-36	NA	power input for string 1
3	+YS2	I	24	20-36	NA	power input for string 2
4	+YS3	I	24	20-36	NA	power input for string 3
5	+YS4	I	24	20-36	NA	power input for string 4
6	+YS5	I	24	20-36	NA	power input for string 5
7	GND	O	0	0-0	NA	earth
8	GND	O	0	0-0	NA	earth
9	GND	O	0	0-0	NA	earth
10	+YS1	I	24	20-36	NA	power input for string 1
11	+YS2	I	24	20-36	NA	power input for string 2
12	+YS3	I	24	20-36	NA	power input for string 3
13	+YS4	I	24	20-36	NA	power input for string 4
14	+YS5	I	24	20-36	NA	power input for string 5
15	GND	O	0	0-0	NA	earth

A D-subminiature connector plug with 15 contacts is used for the panel -Y input with signals as follows:

Pin	Signal	I/O	V	Tolerance	Rise time	Description
1	GND	O	0	0-0	NA	earth
2	-YS1	I	24	20-36	NA	power input for string 1
3	-YS2	I	24	20-36	NA	power input for string 2
4	-YS3	I	24	20-36	NA	power input for string 3
5	-YS4	I	24	20-36	NA	power input for string 4
6	-YS5	I	24	20-36	NA	power input for string 5
7	GND	O	0	0-0	NA	earth
8	GND	O	0	0-0	NA	earth
9	GND	O	0	0-0	NA	earth
10	-YS1	I	24	20-36	NA	power input for string 1
11	-YS2	I	24	20-36	NA	power input for string 2
12	-YS3	I	24	20-36	NA	power input for string 3
13	-YS4	I	24	20-36	NA	power input for string 4
14	-YS5	I	24	20-36	NA	power input for string 5
15	GND	O	0	0-0	NA	earth

A D-subminiature connector plug with 9 contacts is used for the battery with signals as follows:

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Pin	Signal	I/O	V	Tolerance	Rise time	Description
1	GND	O	0	0-0	NA	earth
2	VBATT	I/O	12	10-16	NA	battery voltage
3	VBATT	I/O	12	10-16	NA	battery voltage
4	T_BATT	O	5	0-5	1 μs	battery temperature
5	GND	O	0	0-0	NA	earth
6	GND	O	0	0-0	NA	earth
7	VBATT	I/O	12	10-16	NA	battery voltage
8	VBATT	I/O	12	10-16	NA	battery voltage
9	GND	O	0	0-0	NA	earth

A D-subminiature connector plug with 15 contacts is used for the ring bus with signals as follows:

Pin	Signal	I/O	V	Tolerance	Rise time	Description
1	+14V_A	O	14	13.8–14.2	NA	+14 A output
2	+14V_A	O	14	13.8–14.2	NA	+14 A output
3	GND	O	0	0-0	NA	earth
4	+14V_B	O	14	13.8–14.2	NA	+14 B output
5	+14V_B	O	14	13.8–14.2	NA	+14 B output
6	GND	O	0	0-0	NA	earth
7	GND	O	0	0-0	NA	earth
8	GND	O	0	0-0	NA	earth
9	+14V_A	O	14	13.8–14.2	NA	+14 A output
10	+14V_A	O	14	13.8–14.2	NA	+14 A output
11	GND	O	0	0-0	NA	earth
12	+14V_B	O	14	13.8–14.2	NA	+14 B output
13	+14V_B	O	14	13.8–14.2	NA	+14 B output
14	GND	O	0	0-0	NA	earth
15	GND	O	0	0-0	NA	earth

A D-subminiature connector plug with 9 contacts is used for the telecommand with signals as follows:

Pin	Signal	I/O	V	Tolerance	Rise time	Description
1	REGSD_A	I	5	0-5	1 μs	regulator A shut-down
2	REGSD_B	I	5	0-5	1 μs	regulator B shut-down
3	SP_BATT1	I	5	0-5	1 μs	PV gen. 1 batt. connect
4	SP_BATT2	I	5	0-5	1 μs	PV gen. 2 batt. connect
5	GND	O	0	0-0	NA	earth
6	BATT_+14A1	I	5	0-5	1 μs	battery +14VA connect
7	BATT_+14A2	I	5	0-5	1 μs	battery +14VA connect
8	BATT_+14B1	I	5	0-5	1 μs	battery +14VB connect
9	BATT_+14B2	I	5	0-5	1 μs	battery +14VB connect

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A D-subminiature connector socket with 25 contacts is used for the telemetry with signals as follows:

Pin	Signal	I/O	V	Tolerance	Rise time	Description
1	I_SP_+X	O	5	0-5	1 μs	panel +X current
2	V_SP_+X	O	5	0-5	1 μs	panel +X voltage
3	I_SP_-X	O	5	0-5	1 μs	panel -X current
4	V_SP_-X	O	5	0-5	1 μs	panel -X voltage
5	I_SP_+Y	O	5	0-5	1 μs	panel +Y current
6	V_SP_+Y	O	5	0-5	1 μs	panel +Y voltage
7	I_SP_-Y	O	5	0-5	1 μs	panel -Y current
8	V_SP_-Y	O	5	0-5	1 μs	panel -Y voltage
9	V_BATT	O	5	0-5	1 μs	battery voltage
10	I_BATT	O	5	0-5	1 μs	battery current
11	T_BATT	O	5	0-5	1 μs	battery temperature
12	V_+14V_A	O	5	0-5	1 μs	regulator A voltage
13	I_+14V_A	O	5	0-5	1 μs	regulator A current
14	V_+14V_B	O	5	0-5	1 μs	regulator B voltage
15	I_+14V_B	O	5	0-5	1 μs	regulator B current
16	T_REG_A	O	5	0-5	1 μs	regulator A temp
17	T_REG_B	O	5	0-5	1 μs	regulator B temp
18	+5V_TEL	O	5	0-5	1 μs	5V reference
19	+5V_TEL	O	5	0-5	1 μs	5V reference
20-25	GND	O	0	0-0	NA	earth

Mechanical parameters and interfaces

Mass

Item	Mass
Converters	1,00 kg
Mechanical	1,60 kg
Total MRU	2,60 kg

Volume restriction

The dimensions of the MRU enclosure are shown in Fig. D.2

Reliability

- The unit shall only use parts from the Sunsat Approved Parts List, or for which approval has been given by the QA officer.

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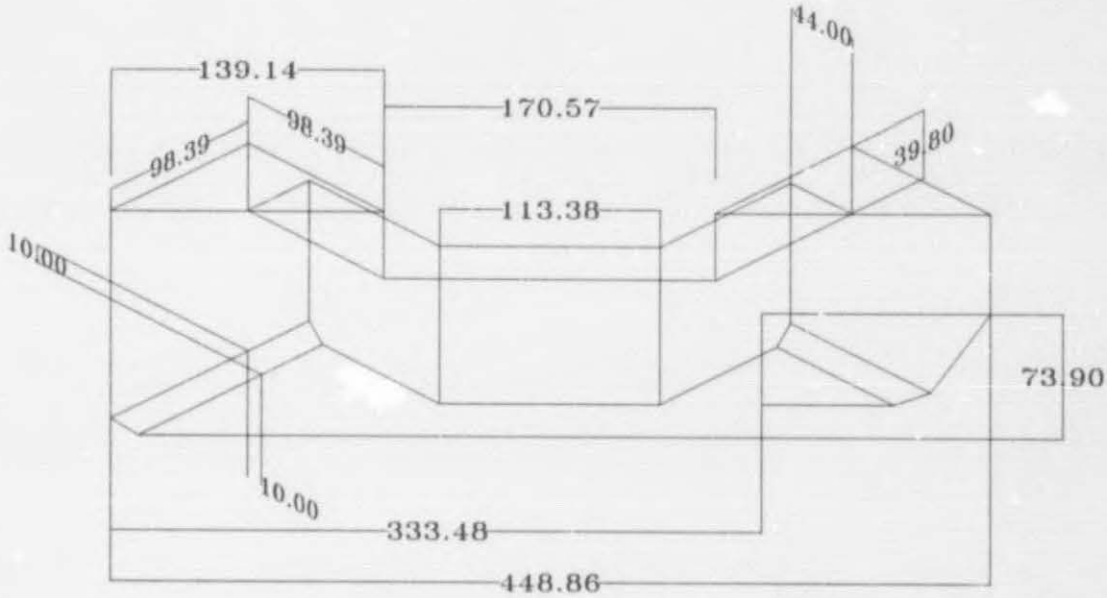

Figure C.2: Power and optics tray Drawn by SED

- Parts selection shall include consideration of the vacuum, radiation, and temperature cycling environment the unit will be subjected to.
- Worst case design calculations, including allowance for component tolerance and drift, shall be presented.
- Acceptance tests shall be defined to verify that no detectable malfunctions are present in the unit.
- Development, assembly, and testing of the unit shall comply with the general QA guidelines.
- There may be no single point failure nodes.
- The bus shall be over-current protected. Short circuit protection is provided in the distributed regulators of the various subsystems.
- The control unit shall be able to initiate and maintain MRU operation under the following conditions:
    1. Highly discharged battery with solar insolation.
    2. Loss of all (wire) links with launcher.
    3. Loss of all (rf) links with ground control.

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4. Loss of communication with onboard computer.

Maintainability

The design of the unit shall make allowance for extensive integration tests.

The unit shall be designed in such a way as to ensure that no damage will be caused by a short-circuit on the power bus.

Environmental specifications

Temperature

Operation: −30°C to +60°C Storage: −30°C to +60°C

Vibration

The unit shall pass the vibration tests specified in Section 3.13 of the technical specifications in [41].

Transportability and storage

Attachments shall be provided for storage during integration. The unit will not be transported separately.

Design and construction standards

Design and construction shall be according to accepted good practices.

Sufficient internal test points shall be provided, to enable correct operation of important subsections of the unit to be monitored.

Materials, processes, parts, surface finishes

All materials selected shall be suitable for space use.

Conformal surface coatings on PCB's are required.

Surface finishes that need to be covered with multi-layer insulation shall be suitable for its adhesion.

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The chassis shall be machined from aluminum 6061-T6 alloy and all non-mating surfaces shall be painted black.

Electromagnetic compatibility

The unit must operate in conjunction with transmitters and receivers operating at thermal noise limits, and must comply with the following requirements:

Emitted interference The fields radiated from the unit shall not cause a signal of more than $--110\ dBm$ as measured in any $1\ MHz$ bandwidth by a dipole antenna at a half wavelength from the unit.

Conducted interference The unit shall not inject a current of more than $1\ mA$ RMS AC on to any supply line at a frequency above [illegible]$0\ kHz$.

Susceptibility The unit shall meet all performance requirements while subjected to

1. A RF field strength of $10\ W$ at $0.5\ m$ at any frequency from $25\ MHz$ to $2.5\ GHz$.
2. $0.5\ V$ RMS at any frequency from $25\ MHz$ to $2.5\ GHz$ applied between earth and any electrical line.

Acceptance tests

A full set of acceptance tests shall be defined and executed. The acceptance criteria shall be selected in such a way that a unit passing the test will meet performance requirements at temperature and life extremes.

Qualification

A qualification test programme shall be defined, which over-stresses the qualification model to a sufficient extreme in order to explore potential design weaknesses, and assure that adequate design margins exist. If necessary, the tests shall monitor internal test points.

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Appendix D

Battery Unit Specifications

Scope

This specification gives characteristic and performance requirements of the battery unit (BU) which, unless otherwise specified, shall be met under all lab integration and space environmental conditions until ten years after launch.

Location and purpose

The BU shall be located on the power and optics tray of the satellite, as shown in Fig. D.1.

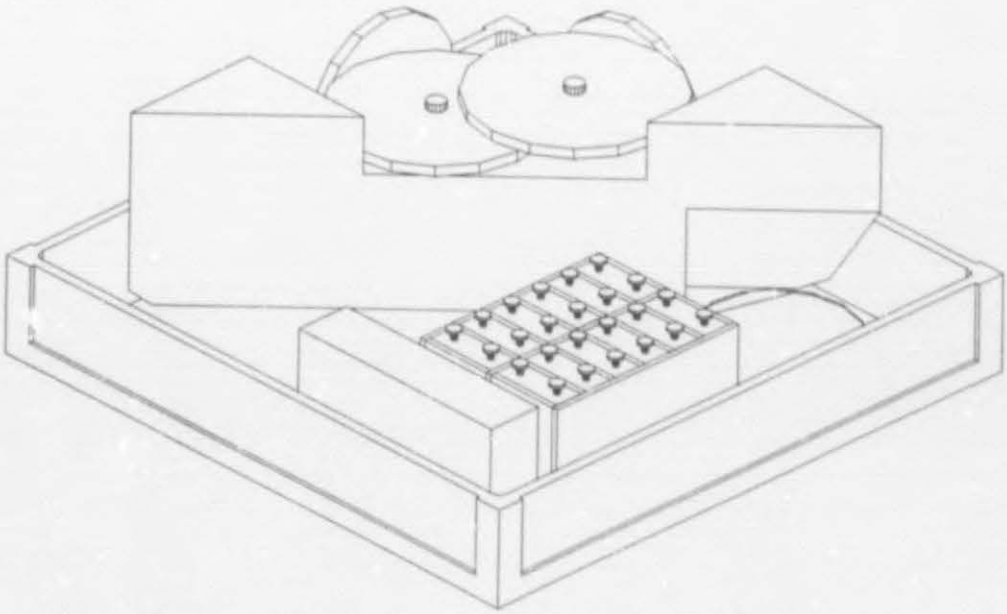

Figure D.1: Power and optics tray Drawn by SED

The purposes of the BU are the following:

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- Store excess energy
- Supply energy to satellite in the eclipse

Functional description

The BU shall receive regulated energy from the main regulator unit (MRU). This shall be stored in an array of battery cells for later use in the satellite eclipse or when power demand is higher than the power available from the PV panels.

Characteristics

Power Storage Specifications

The battery shall consist of 11 $NiCd$ space qualified prismatic cells, each rated at 8Ah. The maximum battery voltage shall be 15 V at full charge. The minimum battery voltage shall be 10 V when it is 25% discharged.

Performance

Power Output Specifications

The power tray shall be able to supply survival power of 5 W continuously. It shall provide a maximum power of 140 W and an average power of 25 W.

Electrical interfaces

A D-subminiature connector socket with 9 contacts is used for the MRU with signals as follows:

Pin	Signal	I/O	V	Tolerance	Rise time	Description
1	GND	O	0	0-0	NA	earth
2	VBATT	I/O	12	10-16	NA	battery voltage
3	VBATT	I/O	12	10-16	NA	battery voltage
4	T_BATT	O	5	0-5	1 μs	battery temperature
5	GND	O	0	0-0	NA	earth
6	GND	O	0	0-0	NA	earth
7	VBATT	I/O	12	10-16	NA	battery voltage
8	VBATT	I/O	12	10-16	NA	battery voltage
9	GND	O	0	0-0	NA	earth

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Mechanical parameters and interfaces

Mass

Item	Mass
Battery cells	4.00 kg
Mechanical	0.50 kg
Total BU	4.50 kg

Volume restriction

The volume restriction of the BU is shown in Fig. D.2.

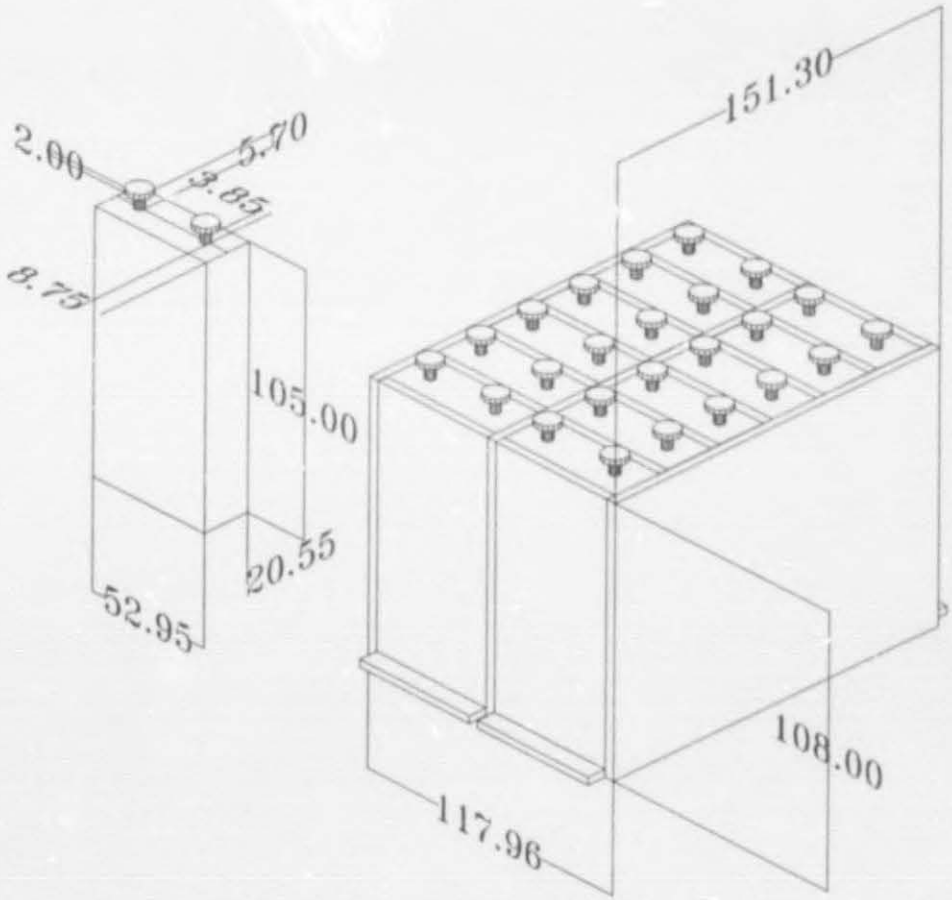

Figure D.2: Battery dimensions Drawn by SED

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Reliability

- The unit shall only use parts from the Sunsat Approved Parts List, or for which approval has been given by the QA officer.
- Parts selection shall include consideration of the vacuum, radiation, and temperature cycling environment the unit will be subjected to.
- Worst case design calculations, including allowance for component tolerance and drift, shall be presented.
- Acceptance tests shall be defined, to verify that no detectable malfunctions are present in the unit.
- Development, assembly, and testing of the unit shall comply with the general QA guidelines.
- There shall be no single point failure nodes.
- The maximum depth of discharge of the battery shall be consistent with the power system lifetime of five years.
- The battery shall consist of cells of similar capacities, since a low capacity cell in the battery may become reverse-charged during discharge and suffer permanent damage.

Maintainability

The design of the unit shall make allowance for extensive integration tests.

Environmental specifications

Temperature

Operation: −30°C to +60°C Storage: −30°C to +60°C

Vibration

The unit shall pass the vibration tests specified in Section 3.13 of the technical specifications in [41].

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Transportability and storage

Attachments shall be provided for storage during integration. The unit will not be transported separately.

Design and construction standards

Design and construction shall be according to accepted good practices.

Sufficient internal test points shall be provided, to enable correct operation of important subsections of the unit to be monitored.

Materials, processes, parts, surface finishes

All materials selected shall be suitable for space use. The battery shall be sealed and suitable for use in space.

Susceptibility The unit shall meet all performance requirements while subjected to

1. A RF field strength of 10 W at 0.5 m at any frequency from 25 MHz to 2.5 GHz.
2. 0.5 V RMS at any frequency from 25 MHz to 2.5 GHz applied between earth and any electrical line.

Acceptance tests

A full set of acceptance tests shall be defined and executed. The acceptance criteria shall be selected in such a way that a unit passing the test will meet performance requirements at temperature and life extremes.

Qualification

A qualification test programme shall be defined, which over-stresses the qualification model to a sufficient extreme in order to explore potential design weaknesses, and assure that adequate design margins exist. If necessary, the tests shall monitor internal test points.

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Appendix E

Power Simulation

Turbo 5.5 Power Simulation

The Turbo 5.5 code for the power simulation is listed below in the programme psim.pas.

Program psim.pas

```
programme Powersimulation;


uses crt, graph;



var teta, phi : array[0..3600] of real;
    parr, temp : array[1..4,1..101] of real;
    starttime, endtime, SAstart, SAend : array[0..16] of real;
    endteta : array[0..251] of real;
    arr : array[0..1600] of real;
    n, m, res, orbit, t, startint, endint,
    SAstartint, SAendint, xmax, nmin, nmax, charge : integer;
    leftb, rightb, topb, bottomb, leftbp, rightbp, topbp,
    bottombp, time, rfoot, length, pmax, pinmax, imax, cap,
    dodpers, apdemand, ppdemand, apavail, ppavail : real;
    orbitc : double;
    firstday : longint;
    f1, f2 : text;
    name, option : string;
const Rearth = 6348;
{**************POSITION AND TIME SIMULATION**************}
    procedure Input;
        var c: char;
            p,q : integer;
    begin
        clrscr; {Simulation period}
        write('Enter day of simulation ');
        readln(firstday);
        writeln;
        leftb := 17; {SA borders in degrees}
        rightb := 33;
        topb := 117;
        bottomb := 125;
        rfoot := 2918; {radius of footprint}

        write('Enter the amount of testpoints in the
        footprint ');
        readln(res); {accuracy}
        writeln;
        write('Do you want the satelite to spin ? ');
        readln(c);
        if (c = 'n') OR (c = 'N') then begin
            option := 'stationary';
            assign(f1,'c:stat1.dat');
            assign(f2,'c:Tstat.dat')
        end;
        if (c = 'y') OR (c = 'Y') then begin
            option := 'spin';
            assign(f1,'c:spin1.dat');
            assign(f2,'c:Tspin.dat')
        end;
        reset(f1);
        reset(f2);
        for p := 1 to 101 do
            readln(f1,parr[1,p],parr[2,p],parr[3,p],
            parr[4,p]);
            readln(f2,temp[1,p],temp[2,p],temp[3,p],
            temp[4,p]);
        close(f1);
        close(f2);
        endteta[0] := 0; {initial conditions}
        arr[0] := 0;
        assign(f1,'c:input.dat');{Read initial cond}
        reset(f1);
        for p := 1 to 251 do
            readln(f1,endteta[p]);
        close(f1)
    end;
    procedure Test(x,y:real); {Testpoint in specified area}
    begin
        if (x > leftbp) AND (x < rightbp) AND (y < topbp)
        AND (y > bottombp) then begin
            t := t + 1;
            arr[t] := time
        end
    end;procedure Crossarea(phit,tetat : real);
        {Compare footprint with specified area}
        var phi0, teta0, x, y, dx: real;
    begin
        phi0 := phit;
        teta0 := tetat;
        dx := rfoot/res;
        x := -rfoot;
        repeat
            y := sqrt(sqr(rfoot)-sqr(x));
            tetat := teta0 + y/Rearth * 180/pi;
            phit := phi0 + x/(Rearth * abs(sin(tetat*pi/180))) * 180/pi;
            Test(phit,tetat);
            x := x + dx;
        until x = rfoot;
        repeat
            y := -sqrt(sqr(rfoot)-sqr(x));
            tetat := teta0 + y/Rearth * 180/pi;
            phit := phi0 + x/(Rearth * abs(sin(tetat*pi/180))) * 180/pi;
            Test(phit,tetat);
            x := x - dx;
        until x = -rfoot
    end;
    procedure Day(m : integer); {Simulates one day's satelite position}
        var dteta, dphi : real;
    begin
        teta[0] := endteta[m-1];
        orbitc := (firstday-1)*360/25.1;
        phi[0] := 0;
        dteta := (360/251);
        dphi := 0.1;
        time := 0;
        t := 0;
        orbit := 1;
        endtime[1] := 0;
        starttime[orbit] := 0;
        for n := 1 to 3600 do begin
            teta[n] := teta[n-1] + dteta;
            phi[n] := phi[n-1] + dphi;
            if phi[n] > 180 then begin
                topbp := 360 - bottomb;
                bottombp := 360 - topb;
                leftbp := leftb + 180;
                rightbp := rightb + 180
            end;
            if phi[n] > 180 then begin
                topbp := topb;
                bottombp := bottomb;
                leftbp := leftb;
                rightbp := rightb
            end;
            time := time + 24*60/3600;
            gotoxy(5,7);
            write('coordinates: ',phi[n]:8:3,teta[n]:8:3);
            Crossarea(phi[n],teta[n]);
            if teta[n] > 360 then begin
                teta[n] := teta[n] - 360;
                endtime[orbit] := time;
```

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```
                SAstart[orbit] := arr[1];
                SAend[orbit] := arr[t];
                gotoxy(10,10);
            writeln('orbit',orbit:3,' start at',starttime[orbit]:8:1,' min
                end at',endtime[orbit]:8:1, ' min');
                if endtime[orbit] <> 0 then begin
                    gotoxy(10,11);
                writeln('SA coverage start at',SAstart[orbit]:8:1,' min
                end at',SAend[orbit]:8:1, ' min')
                end;
                if SAend[orbit] = 0 then begin
                    gotoxy(10,11);
                    writeln('No SA coverage in this orbit ')
                end;
                orbit := orbit + 1;
                starttime[orbit] := time;
                t := 0;
                arr[1] := 0;
                arr[0] := 0
            end; {if teta[n]}
            if n = 3600 then begin
                endtime[orbit] := time;
                SAstart[orbit] := arr[1];
                SAend[orbit] := arr[t];
                gotoxy(10,11);
                writeln(' ')
            end
        end
    end;
    procedure Graphout(ymax, aver : real; heading : string);
        var xscale, yscale, xgridscale, preorbit : real;
            xstip, ystip, preystip, prexstip, graphmode,
            graphdriver, av, point, sw : integer;
            m,n : longint;
    begin
        graphdriver := Detect;
        Initgraph(graphdriver,graphmode,'');
        xscale := GetmaxX/(1440);
        yscale := 0.75 * 0.5 * GetmaxY/ymax;
        Rectangle(0,0,GetmaxX,GetmaxY);
        OuttextXY(100,2,heading);
        OuttextXY(450,2,option);
        Str(firstday,heading);
            OuttextXY(350,2,heading);
            OuttextXY(300,2,'Day: ');
        Str(0,heading);
            OuttextXY(2,GetmaxY-av+40,heading);
        Str(1440,heading);
            OuttextXY(GetmaxX-50,GetmaxY-av+40,heading);
        Str(ymax:5:2,heading);
            OuttextXY(170,300,heading);
        Str(aver:5:2,heading);
            OuttextXY(170,310,heading);
            OuttextXY(2,300,'Peak value = ');
            OuttextXY(2,310,'Average value = ');
        av := round(GetmaxY/2);
        preystip := 0;
        prexstip :=0;
        for n := 0 to 1440 do begin
            ystip := round(yscale*arr[n]);
            xstip := round(xscale*n);
            Line(prexstip,av-preystip,xstip,av-ystip);
            preystip := ystip;
            prexstip := xstip
        end;
        Line(0,av,GetmaxX,av);
        xgridscale := GetmaxX/1440;
        m := 0;
        if orbitc <> round(orbitc) then
            m := round(orbitc) + 1;
        if orbitc <> round(orbitc) then
            m := round(orbitc);
        preorbit := endtime[1] * xgridscale;
        sw := 50;
        if (endtime[1] - starttime[1]) >= 100.4 then
            m := m + 1;
        for n := m to (m + orbit) do begin
            point := round(preorbit + (n-m) * 100.4 * xgridscale);
            Line(point,av-4,point,av+4);
            Str(n,heading);
            OuttextXY(point,av+10,heading);
            Str((n-m)*100.4:5:1,heading);
            OuttextXY(point,av+sw,heading);
            if sw = 50 then
                sw := 60
            else if sw = 60 then
                sw := 50
        end;
        OuttextXY(round(GetmaxX/2),av+20,'orbits');
        OuttextXY(round(GetmaxX/2),av+70,'time in min.')
    end;
{**************POWER DEMAND SIMULATION**************}
procedure RxTx;
begin
    for n := startint to endint do begin
        arr[n] := 0;
        arr[n] := arr[n] + 3 {1 VHF or UHF transmitter}
    end;
    for n := SAstartint to SAendint do begin
        arr[n] := arr[n] - 3;
        arr[n] := arr[n] + 10 {full power over SA}
    end;
    for n := startint to (startint + 49) do begin
        if n <> 1440 then
        arr[n] := arr[n] + 3;
    end; {1 VHF or UHF transmitter}
    for n := SAstartint to SAendint do begin
        arr[n] := arr[n] - 3;
        arr[n] := arr[n] + 10 {full power over SA}
    end;
    for n := startint to endint do
        arr[n] := arr[n] + 2.5; {5 UHF & VHF receivers}
    for n := SAstartint to SAendint do
        arr[n] := arr[n] + 30; {s mode transponder over SA}
    for n := startint to (startint + 4) do begin {most of the time over}
        if n <> 1440 then begin
            m := startint + 10 * (n - startint); {Africa and Antarctica}
            arr[m] := arr[m] + 2
        end; {2 transmitter synthesizers}
    end;
    for n := startint to (startint + 9) do begin {most of the time over}
        if n <> 1440 then begin
            m := startint + 5 * (n - startint) + 5; {Africa and Antarctica}
            arr[m] := arr[m] + 2 {2 receiver synthesizers}
        end;
    end;
    for n := SAstartint to SAendint do
        arr[n] := arr[n] + 3; {29 MHz transmitter over SA}
    for n := startint to endint do
        arr[n] := arr[n] + 0.04; {4 modems}
    for n := startint to endint do
        arr[n] := arr[n] + 0.06; {6 multiplexers}
    for n := startint to endint do
        arr[n] := arr[n] + 0.7; {4 demodulators}
    for n := startint to endint do
        arr[n] := arr[n] + 0.5 {command decoder}
end;
procedure ADCS;
begin
    for n := startint to (startint + 4) do begin
        if n <> 1440 then begin
            m := startint + 4 * (n - startint) + 20;
            arr[m] := arr[m] + 9 {3 reaction wheels over SA}
        end;
    end;
    for n := startint to (startint + 4) do begin
        if n <> 1440 then begin
            m := startint + 20 * (n - startint) + 15;
            arr[m] := arr[m] + 10 {6 magnetotorquers}
        end;
    end;
    for n := startint to endint do
        arr[n] := arr[n] + 1; {magnetometer}
    for n := startint to (startint + 30) do begin
        if n <> 1440 then begin
            m := startint + 3 * (n - startint);
            arr[m] := arr[m] + 2 {4 horizon sensors}
        end
    end
end;
procedure Telemetry;
begin
    for n := startint to endint do
        arr[n] := arr[n] + 2
end;
procedure Computer;
begin
    for n := startint to (startint +19) do begin
        if n <> 1440 then begin
            m := startint + (n - startint) * 5;
            arr[m] := arr[m] + 5
        end
    end
end;
procedure Ranging;
begin
    for n := startint to (startint + 19) do begin
        if n <> 1440 then begin
            m := startint + (n - startint) * 5 + 1;
            arr[m] := arr[m] + 5
        end
    end
end;
procedure Imager;
```

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```
    begin
        for n := startint to endint do {over SA}
            arr[n] := arr[n] + 5
    end;procedure Experiment;
    begin
        for n := startint to (startint + 19) do begin
            if n ¿ 1440 then begin
                m := startint + (n - startint) * 5 + 4;
                arr[m] := arr[m] + 5
            end
        end
    end;
    procedure DistributedRegulators;
    begin
        for n := startint to endint do
            arr[n] := arr[n]/0.85
    end;
    procedure Busregulator;
        var busregeff, sto : real;
    begin
        for n := startint to endint do
            sto := arr[n]/80;
        if sto ¿= 1/3 then begin
            busregeff := 0.225 * sto + 0.675;
            arr[n] := arr[n] / busregeff
        end;
        if sto ¿ 1/3 then begin
            busregeff := 2.25 * sto;
            arr[n] := arr[n] / busregeff
        end
    end;
    procedure Oneorbit;
    begin
        RxTx;
        ADCS;
        Telemetry;
        Computer;
        Ranging;
        Imager;
        Experiment;
        DistributedRegulators;
        Busregulator;
        for n := startint to endint do begin
            if xmax ¿ arr[n] then
                xmax := round(arr[n]);
            if nmin ¿ n then
                nmin := n;
            if nmax ¿ n then
                nmax := n
        end
    end;
    procedure Daypower(d : integer);
        var o : integer;
    begin
        xmax := 0;
        nmin := 10;
        nmax := 0;
        startint := 1;
        endint := 101;
        SAstartint := round(SAstart[1]);
        SAendint := round(SAend[1]);
        oneorbit;
        startint := round(starttime[1]);
        endint := round(endtime[1]);
        for n := startint to endint do
            arr[n] := arr[101-endint+n];
        for o := 2 to (orbit) do begin
            startint := round(starttime[o]);
            endint := round(endtime[o]);
            SAstartint := round(SAstart[o]);
            SAendint := round(SAend[o]);
            Oneorbit
        end
    end;
    function Average : real;
        var sum :real;
    begin
        sum := 0;
        for n := 1 to 1440 do
            sum := sum + arr[n];
        Average := sum/1440
    end;
    function Peak : real;
        var PP : real;
    begin
        PP := 0;
        for n := 1 to 1440 do begin
            if abs(arr[n]) ¿ PP then
                PP := abs(arr[n])
        end;
        Peak := PP
    end;
```

```
{**************SIMULATION OF POWER AVAILABLE**************}
    procedure Effarea;
        var area : real;
    begin
        area := sqr(0.45);
        for n := 1 to 101 do begin
            for m := 1 to 4 do
                parr[m,n] := area * parr[m,n]
        end
    end;
    procedure Powerfromsun;
        var arr, arraytempeff, timefactor : real;
        solarconst = 1353;
    begin
        assign(f1,'c:sunp.dat');
        rewrite(f1);
        pmax := 0;
        for n := 1 to 101 do begin
            teta[n] := 0;
            for m := 1 to 4 do begin
                parr[m,n] := parr[m,n] * solarconst;
                arraytempeff := (-0.033 * temp[m,n] + 20.3)/100;
                timefactor := (-2.778E-3 * firstday + ¿00)/100;
                parr[m,n] := parr[m,n] * arraytempeff * timefactor;
                if pmax ¿ parr[m,n] then
                    pmax := round(parr[m,n]);
                teta[n] := teta[n] + parr[m,n];
            end;
            writeln(f1,teta[n]);
        end;
    close(f1);
    end;
    procedure Maxpfollower;
        var foleff, sto : real;
    begin
        for n := 1 to 101 do begin
            sto := teta[n]/pmax;
            if sto ¿= 1/3 then begin
                foleff := 0.225 * sto + 0.675;
                teta[n] := teta[n] * foleff
            end;
            if sto ¿ 1/3 then begin
                foleff := 2.25 * sto;
                teta[n] := teta[n] * foleff
            end
        end
    end;
    procedure Powerin;
        var correct : real;
    begin
        pinmax := 0;
        correct := 0;
        endint := round(endtime[1]);
        for n := 0 to nmax do begin
            if n ¿ 101 then begin
                correct := correct + 0.4;
                if correct ¿= 1 then begin
                    m := 101;
                    correct := correct - 1
                end;
            if correct ¿ 1 then
                m := 100;
            teta[n] := teta[n-m]
        end
    end;
        for n := 0 to endint do begin
            phi[n] := arr[n];
            arr[n] := teta[n+m-endint];
            if pinmax ¿ round(arr[n]) then
                pinmax := round(arr[n])
        end;
        for n := (endint+1) to nmax do begin
            phi[n] := arr[n];
            arr[n] := teta[n-endint];
            if pinmax ¿ round(arr[n]) then
                pinmax := round(arr[n])
        end
    end;
    procedure Liobattery;
    begin
        for n := nmin to nmax do begin
            arr[n] := arr[n] - phi[n];
            if arr[n] ¿ 0 then
                arr[n] := arr[n]/28;
            if arr[n] ¿ 0 then
                arr[n] := arr[n]/22;
            if imax ¿ round(arr[n]) then
                imax := abs(round(arr[n]))
        end
    end;
    procedure Capacity;
        var ratcap, temp, battempeff : real;
```

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```
    begin
        ratcap := 4;
        temp := 0;
        if temp ¿ 40 then
        battempeff := 1.2;
        if temp ¿ 40 then
            battempeff := (-6 * temp + 360)/100;
        cap := ratcap * battempeff
    end;
    procedure Amphour;
        var dod : real;
    begin
        arr[nmin-1] := cap;
        dod := 0;
        charge := 0;
        for n := nmin to nmax do begin
            if (arr[n-1] ¿= cap) AND (arr[n] ¿ 0) then
                arr[n] := arr[n-1];
            if (arr[n-1] ¿ cap) OR (arr[n] ¿ 0) then
                arr[n] := arr[n-1] + arr[n] / 60;
            if (arr[n] ¿ cap) AND (arr[n-1] ¿= cap) then
                charge := charge + 1;
            if (cap - arr[n]) ¿ dod then
                dod := cap - arr[n];
            dodpers := dod/cap * 100
        end
    end;
begin {main}
    Input;
    Day(firstday);
    Daypower(firstday);
        Graphout(Peak, Average ,'Powerdemand');
        OuttextXY(220,300,'W');
        OuttextXY(220,310,'W');
        read'n;
    Effarea;
    Powerfromsun;
    Powerin;
        Graphout(Peak, Average ,'Power from sun');
        OuttextXY(220,300,'W');
        OuttextXY(220,310,'W');
        readln;
    Itobattery;
        Graphout(Peak, Average ,'Current to battery');
        OuttextXY(220,300,'A');
        OuttextXY(220,310,'A');
        readln;
    Capacity;
    Amphour;
        Graphout(Peak, Average,'Amphour of battery');
        OuttextXY(220,300,'Ah');
        OuttextXY(220,310,'Ah');
        Str(charge,name);
        OuttextXY(170,280,name);
        Str(dodpers:5:2,name);
        OuttextXY(170,290,name);
        OuttextXY(2,280,'Discharge cycles = ');
        OuttextXY(2,290,'Depth of discharge = ');
        OuttextXY(220,280,'cycles');
        OuttextXY(220,290,'%');
        readln
end.
```

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SIMuWIN Power Simulation

The power simulation in *SIMuWIN* is illustrated in the next three figures. Fig. E.1 shows the main power simulation module (**powtest.dgm**) of the block diagram based program. Fig. E.2 is the module (**ssenmod**) which represents the power supply simulation in the main module. Fig. E.3 represents the module (**pwrmod**) which represents the power demand simulation in the main module.

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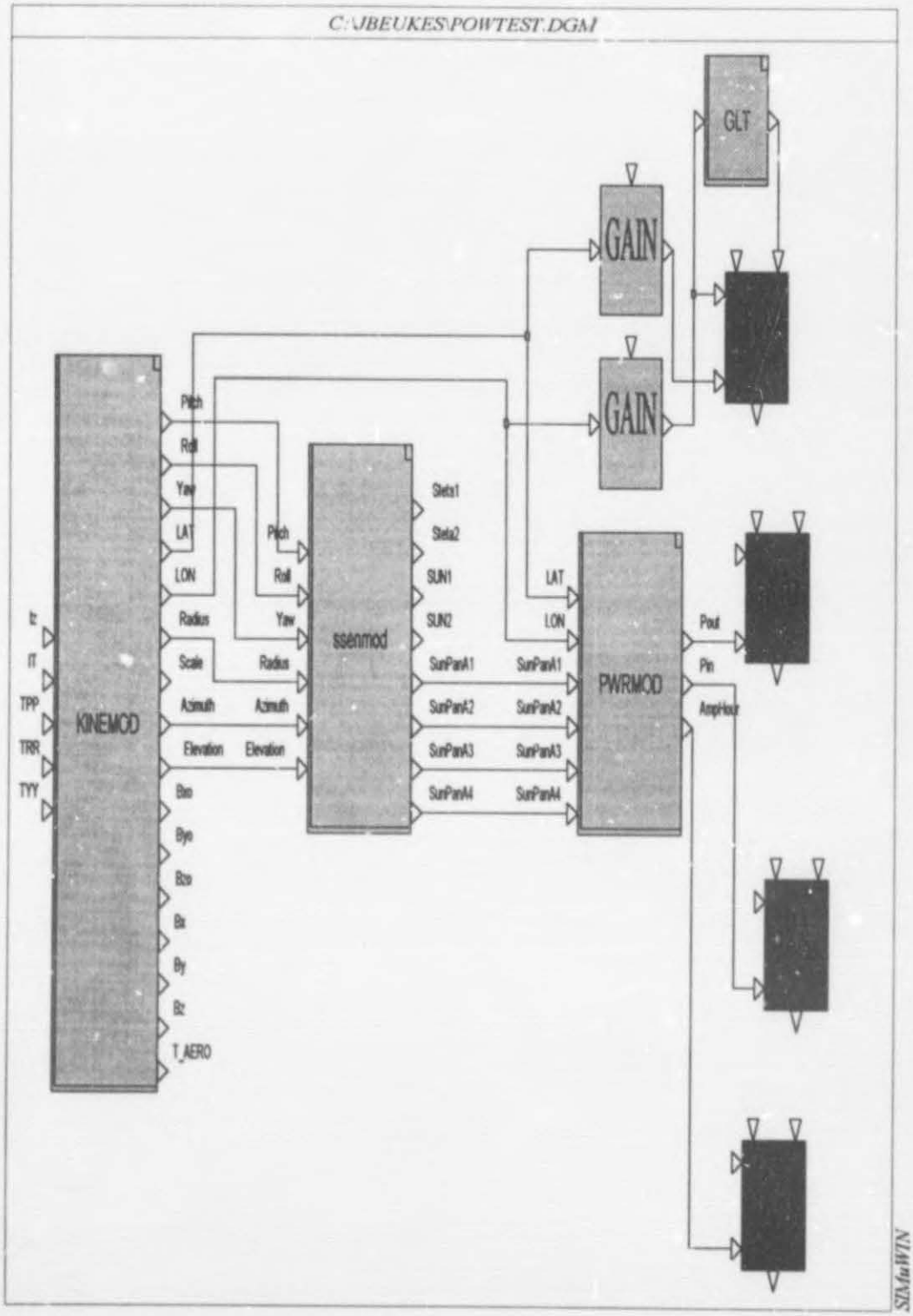

Figure E.1: Main power simulation module Drawn by R de Villiers

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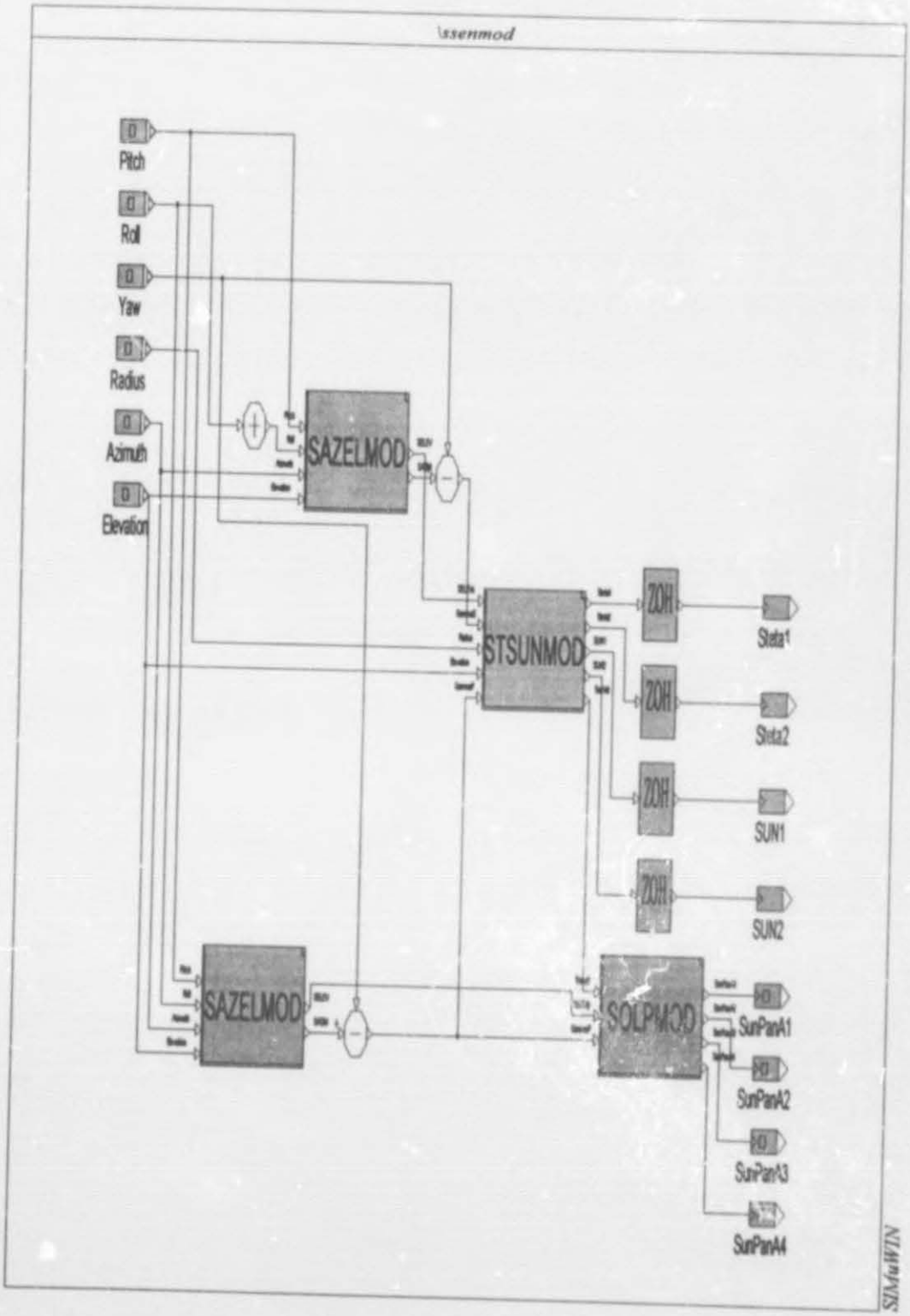

Figure E.2: Module simulating power supply Drawn by R de Villiers

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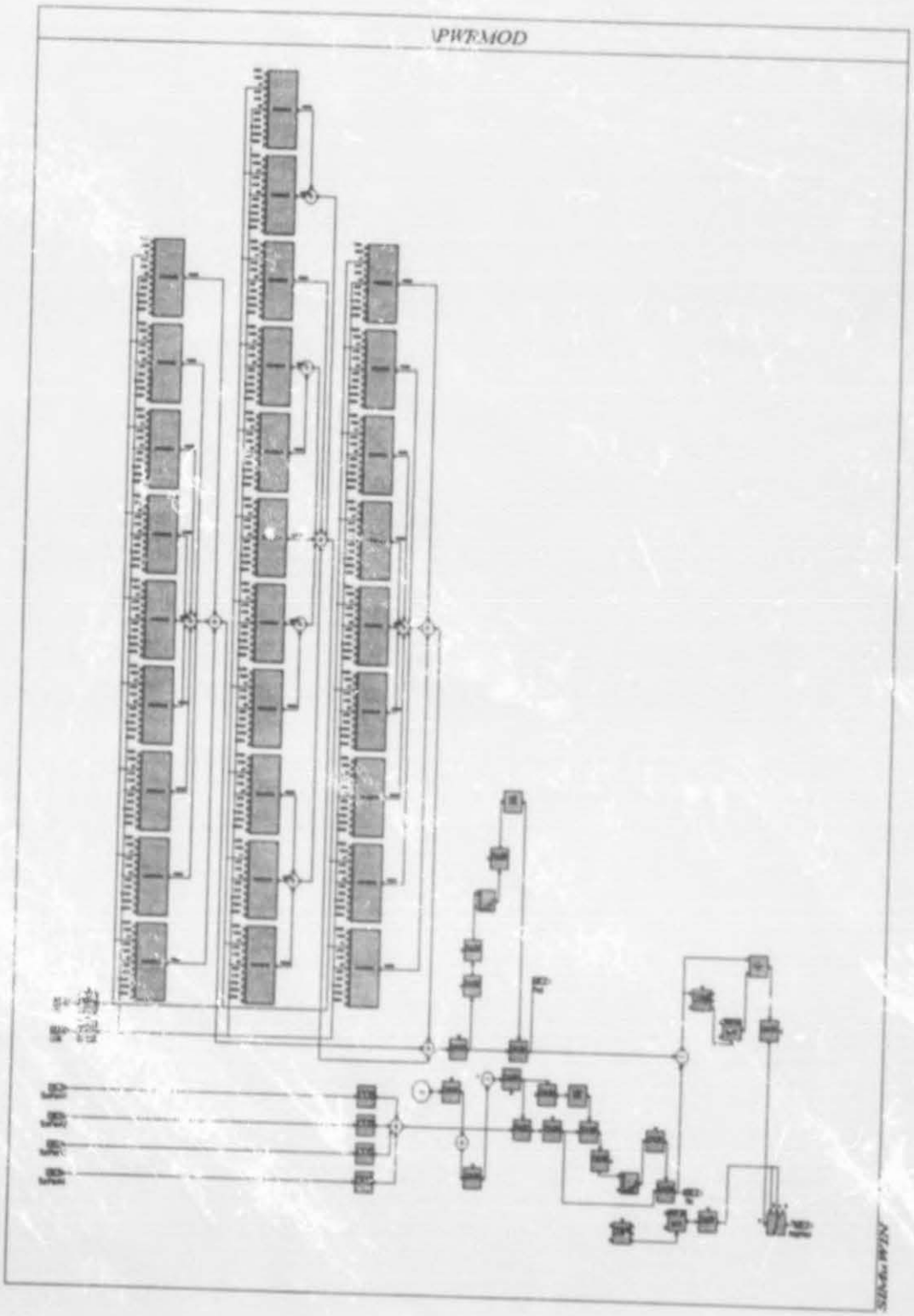

Figure E.3: Module simulating power demand Drawn by R de Villiers

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Appendix F

Design of Magnetic Components

F.1 Inductor Design

The inductor design procedure in [27] is used in this section.

Core Material and B_{max}

In an inductor, the flux ϕ and the flux density B are proportional to the current i_L. The current through the filter inductor is shown in Fig. 3.4, where

$$\frac{\Delta I_L}{I_{L,max}} = \frac{\Delta B}{B_{max}} \tag{F.1}$$

and the switching frequency f_S is also known. B_{max} can initially be assumed to be equal to the saturation flux density B_{sat}. The 3B8 Philips core material is used, and the maximum flux density is therefore $B_{max} = B_{sat} = 350\ mT$ from [29]. This allows ΔB to be estimated from Eq. F.1 as 262.5 mT. Knowing ΔB and f_S, the losses are obtained from loss curves shown in [29]. If the core losses are too high, either a smaller value of B_{max} can be used in Eq. F.1 or a better core material must be selected. If the core losses are low, a material with a higher saturation flux density could be chosen. A commonly used upper limit for core losses is 10 mW/cm^3. 3B8 material is chosen, for its low core losses and a relative high saturation flux density.

Core Size and Shape

Knowing B_{max} and the material, a core size and shape can be selected from [29]. A variety of shapes are available. To suit the given application, potcores are chosen, because the shape forms a built-in shield and therefore has no mutual fields with surrounding components. An initial choice of the core size can be made using Eq. F.9. The parameters on the left-hand side of the equation are the design inputs. For the initial estimate, assume that $k_{Cu} = 0.6$ and $J = 2\ A/mm^2$. B_{max} is known from Eq. F.1. The area product

$$A_w A_{core} > \frac{L_{max} I_{L,max} I_{L,rms}}{k_{Cu} J B_{max}}$$

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$$= \frac{7.10^{-6} \times 7 \times 5}{0.6 \times 2.10^{6} \times 0.35} = 0.589.10^{-9}\ m^4 \tag{F.2}$$

allows the core size to be picked, using the information on potcores in [29]. The P26/16 core, with $A_w A_{core} = 3.66.10^{-9}\ m^4$, is chosen.

Bobbin

A bobbin is provided with cores, and the effective cross-sectional area $A_w = 9.7\ mm^2$ for winding on the bobbin is given, as shown in Fig. F.1.

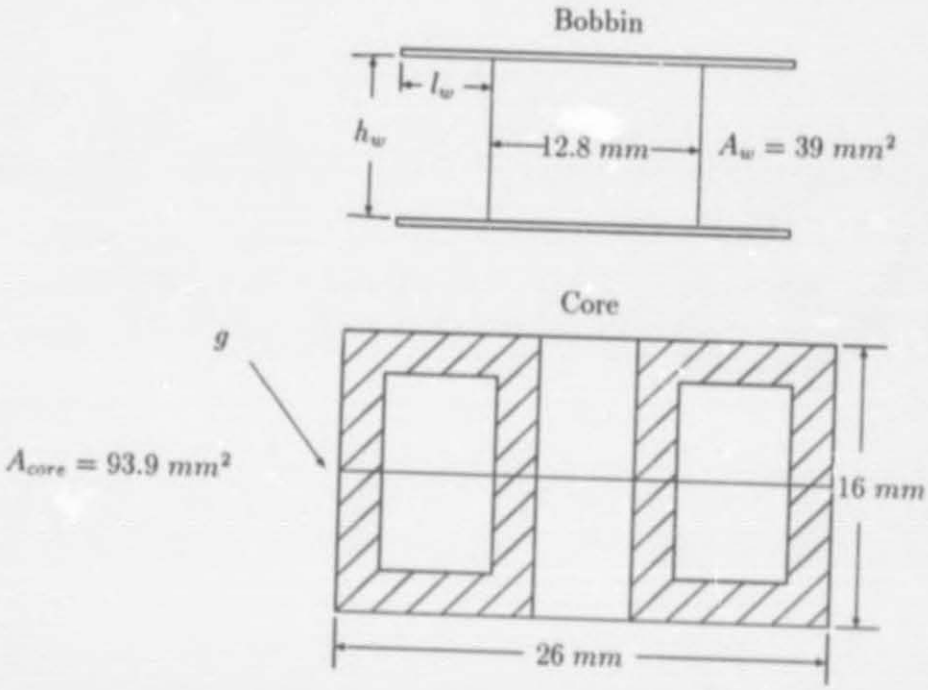

Figure F.1: Bobbin and Potcore dimensions

Copper Wire

Knowing $I_{L,rms}$, the cross-sectional area of the copper wire can be chosen from thermal considerations, so that the highest temperature in the middle of the winding is less than the specified maximum temperature for the insulating material on the wire. The surface-to-volume ratio of the winding decreases with the increasing dimension l_w defined in Fig. F.1. Therefore, from thermal considerations, a larger inductor must be designed, for lower loss per unit volume.

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The maximum permissible current density decreases with increasing bobbin size, as described in [27]. Using this information, it can be seen that the current density is not limited by core heat restrictions, because $l_w = 4.4\ mm$. The current density is chosen as $J = 4\ A/mm^2$. The cross-sectional area of the copper wire in terms of $I_{L,rms}$ and J is

$$A_{Cu} = \frac{I_{rms}}{J} = \frac{5}{4} = 1.25\ mm^2 \tag{F.3}$$

The diameter, therefore, is 0.6 mm. From wire tables, the nearest wire with a cross-sectional area equal to or greater than A_{Cu} is selected.

Assuming a fill-factor k_{Cu} for the winding to be in the range of 0.6 to 0.8, the number of turns N is given by

$$A_w k_{Cu} = N A_{Cu} \tag{F.4}$$

Eqq. F.3 and F.4 yield

$$N = A_w \frac{k_{Cu} J}{I_{L,rms}} = 20 \tag{F.5}$$

where N is the maximum number of turns possible for the given $I_{L,rms}$ and the selected core.

Maximum L for the Selected Core

Having selected B_{max} above, and knowing the core cross-sectional area A_{core}, one can give the maximum flux in the core as

$$\phi_{max} = B_{max} A_{core} = 350\ mT * 93.9\ mm^2 = 32.9\ \mu Weber \tag{F.6}$$

To calculate the maximum possible inductance of the inductor, the air gap must be chosen so that, at $I_{L,max}$, the flux is ϕ_{max} (known from Eq. F.6). Use of the definition of inductance in terms of current and flux linkage results in

$$L_{max} I_{L,max} = N \phi_{max} \tag{F.7}$$

then

$$L_{max} = \frac{N \phi_{max}}{I_{L,max}} = \frac{20 \times 32.9.10^{-6}}{7} = 94\ \mu H \tag{F.8}$$

The inductance given in Eq. F.8 is the maximum inductance possible with the selected core, and is well above the minimum value obtained in Section 3.3.1.

Combining Eqq. F.5 and F.8 yields

$$L_{max} I_{L,max} I_{L,rms} = \{k_{Cu} J B_{max}\} A_w A_{core} \tag{F.9}$$

For the selected number of turns N, combining Eqq. F.8 and F.5 in Eq. F.9 results in

$$L I_{L,max} I_{L,rms} = k_{Cu} J B_{max} A_w A_{core} \tag{F.10}$$

Eq. F.10 shows that the $L_{max} I_{L,max} I_{L,rms}$ product results in the product of two areas associated with the core multiplied by the term within the brackets, which contains quantities that are material- and slightly size-dependent. The area product $A_w A_{core}$ is an indicator of core size and of weight.

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Air Gap

The air gap is calculated on the basis of maximum assumed flux density B_{max} which is generated by the peak current $I_{L,max}$. Because of the fringing of the flux, as indicated in Fig. F.2, the effective cross-sectional area of the air gap A_g can be estimated, as shown in Fig. F.2. The flux density in the air gap can be estimated as

$$B_{g,max} = \frac{A_{core} B_{max}}{A_g} \tag{F.11}$$

where $A_g = 1.1 A_{core} = 103.3\ mm^2$, and

$$H_g = \frac{B_g}{\mu_0} \tag{F.12}$$

From Ampere's law, at the peak current

$$\oint H_{g,max}\, dl = N I_{L,max} \tag{F.13}$$

If a high relative permeability is assumed for the core material in Fig. F.1, so that most of the mmf is dropped in the air gap, Eq. F.13 becomes

$$H_{g,max} g = N I_{L,max} \tag{F.14}$$

The air-gap length g can be estimated from Eqq. F.11, F.12, and F.14 as

$$g = \frac{\mu_0 A_g N I_{L,max}}{A_{core} B_{max}} = \frac{4\pi.10^{-7} \times 1.1 \times 7}{0.35} = 0.03\ mm \tag{F.15}$$

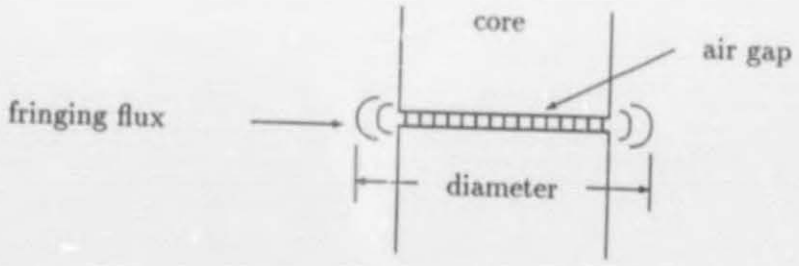

Figure F.2: Fringing flux and an estimation of the area of the air gap A_g

For the specific air gap given by the foregoing equation, $I_{L,max}$ will produce ϕ_{max} exactly, thus satisfying Eq. F.5.

Fringing flux shown in Fig. F.2 "cuts" the copper wire of the winding and thus produces eddy current losses in the winding. These losses can be reduced by using distributed air gaps.

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Loss Estimation

The core losses are obtained from losscurves provided by the core manufacturer. The material chosen has very low core losses. The winding losses can be estimated by calculating the winding resistance. Knowing the cross-sectional area ($A_{Cu} = 1.25\ mm^2$) and the length of the copper wire ($20 \times 53 = 1\ m$), the dc resistance of the winding at the operating temperature can be estimated.

$$R_{Cu} = \frac{l_{Cu}}{A_{Cu}}\sigma_{Cu} = \frac{1}{1.25.10^{-6}}17.10^{-9} = 14\ m\Omega \tag{F.16}$$

The power loss in the copper therefore is

$$P_{Cu,loss} = I_L^2 R_{Cu} = 0.35\ W \tag{F.17}$$

There are additional eddy current losses in the winding, especially if ΔB is large.

F.2 Transformer Design

The transformer design procedure in [27] is used in this section.

Core Material and B_{max}

In a transformer with bidirectional ac excitation, $\Delta B = B_{max}$. Since the core losses depend on ΔB, B_{max} is chosen to be much smaller than B_{sat}. The chosen material is 3B8 from Philips, because it has a high B_{sat}. From [29] $B_{sat} = 350\ mT$, and B_{max} is chosen as $250\ mT$.

Core Sizes and Shapes

Knowing the voltage waveform, the flux ϕ can be obtained as

$$v_P = N_P \frac{d\phi}{dt} \tag{F.18}$$

where it is recognized that the average voltage is zero. For a square-wave voltage input with $d = 0.5$, as shown in Fig. F.3, Eq. F.18 becomes

$$N_P = \frac{V_P}{4 f_O \phi_{max}} \tag{F.19}$$

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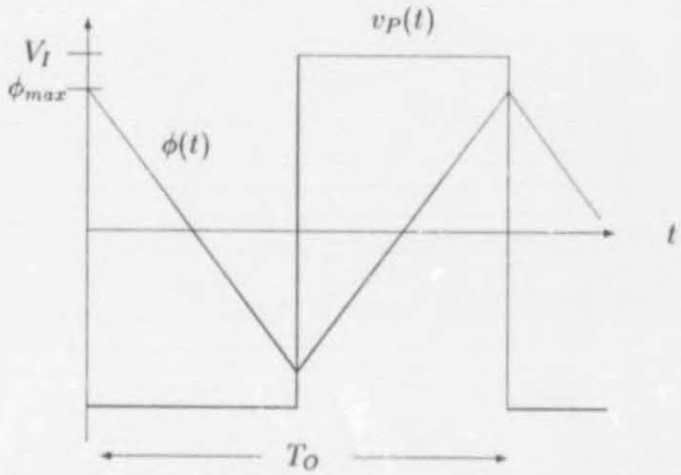

Figure F.3: Transformer flux waveform when $v_P(t)$ is a squarewave

where $f_O = \frac{1}{T_O}$ is the operating frequency. An initial selection of core size can be made using Eq. F.34, where S and the frequency f_O are known from the design inputs. Approximate estimates of k_{Cu}, J and B_{max} are made in the same manner as was described for the inductor in Section F.1. This allows the product $A_w A_{core}$ to be estimated and the core size to be selected using the information in [29].

$$\begin{aligned} A_{core}A_w &> \frac{V_{P,rms}I_{P,rms}}{2k_{Cu}JB_{max}f_O} \\ &= \frac{16 \times 3.75}{2 \times 0.5 \times 4.10^6 \times 0.25 \times 35.10^3} \\ &= 1.714.10^{-9}m^4 \end{aligned}$$

The P30/19 core has a $A_{core}A_w = 7.53.10^{-9}$ and is selected for the transformer core. Now that the core area A_{core} is known, B_{max} is selected, as in the discussion in Section F.1. Therefore, $\phi_{max} = A_{core}B_{max}$ can be substituted into Eq. F.34 to yield

$$\begin{aligned} N_{P1} &> \frac{V_{P1,max}}{4f_O A_{core}B_{max}} \\ &= \frac{31}{4 \times 35.10^3 \times 137.10^{-6} \times 0.25} = 6 \end{aligned} \tag{F.20}$$

$$N_{P2} > \frac{V_{P2,max}}{4f_O A_{core}B_{max}}$$

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$$= \frac{16}{4 \times 35.10^3 \times 137.10^{-6} \times 0.25} = 3 \tag{F.21}$$

N_{P1} and N_{P2} is chosen as 6 and 3 respectively, and therefore

$$N_S > \frac{N_{P1}}{n_1} = \frac{6}{1} = 6 \tag{F.22}$$

and

$$N_S > \frac{N_{P2}}{n_2} = \frac{3}{0.686} = 4.4 \tag{F.23}$$

By choosing $N_S = 7$ Eqs. 3.14, 3.15, F.22 and F.23 are satisfied.

Bobbin

The bobbin for a transformer wound on a potcore is shown in Fig. F.1. Based on the initial core selection, the dimensions l_w and h_w are known, and the effective area is $A_w = 55\ mm^2$.

Copper Wire

From thermal considerations similar to those discussed in the design of inductors, the current density is deducted as $J = 4\ A/mm^2$.

All windings are designed for the same current density so that

$$A_{Cu,P1} = \frac{I_{P1}}{J} = \frac{3.75}{4} = 0.94\ mm^2 \tag{F.24}$$

$$A_{Cu,P2} = \frac{I_{P2}}{J} = \frac{2.5}{4} = 0.625\ mm^2 \tag{F.25}$$

$$A_{Cu,S} = \frac{I_S}{J} = \frac{2.5}{4} = 0.625\ mm^2 \tag{F.26}$$

The diameters of the conductors, therefore, are $N_{P1} = 0.6\ mm$, $N_{P2} = 0.5\ mm$ and $N_S = 0.5\ mm$.

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Assuming that the magnetizing current is negligible and that power is only supplied by the battery during maximum load,

$$N_{P2}I_{P2} = N_S I_S \tag{F.27}$$

Combining Eq. F.27, F.25 and F.26 yields

$$N_{P2}A_{Cu,P2} = N_S A_{Cu,S} \tag{F.28}$$

Assume that the same winding fill factor k_{Cu} for the primary and secondary windings yields

$$A_w k_{Cu} = N_{P2}A_{Cu,P2} + N_S A_{Cu,S} \tag{F.29}$$

Using the dimensions calculated above in these equations, it can be seen that the windings fit on the core. Combining Eqq. F.28 and F.29, the area of the copper wire can be estimated as

$$A_{Cu,P2} = \frac{A_w k_{Cu}}{2N_{P2}} \tag{F.30}$$

$$A_{Cu,S} = \frac{A_w k_{Cu}}{2N_S} \tag{F.31}$$

Maximum Current for the Selected Core

With A_{Cu} selected in Eq. F.31, the maximum allowable currents at the current density J are

$$I_{P2,max} = \frac{k_{Cu}JA_w}{2N_{P2}} \tag{F.32}$$

$$I_{S,max} = \frac{k_{Cu}JA_w}{2N_S} \tag{F.33}$$

If $I_{P2,max}$ and $I_{S,max}$ are smaller than the current required by the design specifications, a larger core must be selected. The opposite is true if the maximum currents possible are too large.

The volt-ampere rating can be obtained by combining Eqq. F.19 and F.32 and assuming $I_P = I_{P,max}$

$$S = V_P I_P = [2k_{Cu}JB_{max}]A_{core}A_w f_S \tag{F.34}$$

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This Eq. shows that the maximum volt-ampere rating for the selected core is proportional to the product of the two areas associated with the core and the operating frequency. The quantities within the square brackets are material and slightly size-dependent. Another important conclusion to be drawn is that for a given VA-rating, the core size varies inversely proportional to the frequency, as long as B_{max} is kept constant. The same procedure could be followed by assuming that all the power is delivered by the PV array.

Leakage Inductance

Because of the electrical isolation requirement, it is not possible to interwind primary and secondary winding conductors. The flux density in the window depends inversely on the window height, and therefore the leakage inductance varies inversely according to the (window height)^2. The leakage inductance of the transformer will therefore be large. However, it is used to the advantage of the converter, in the sense that it forms the filter inductance to the battery.

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Appendix G

Schematic Diagrams

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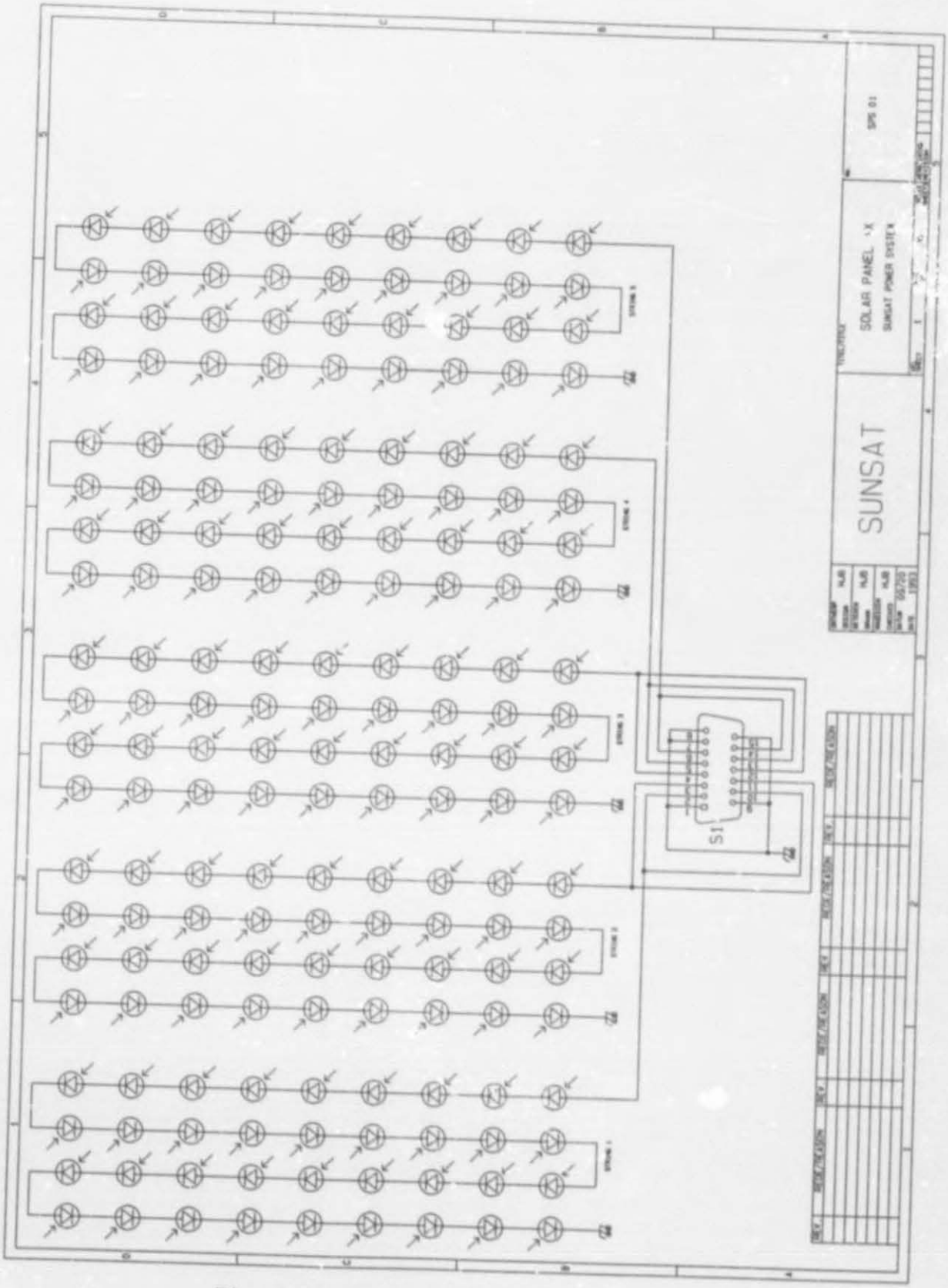

Figure G.1: PV Panel +X of the PV Generator

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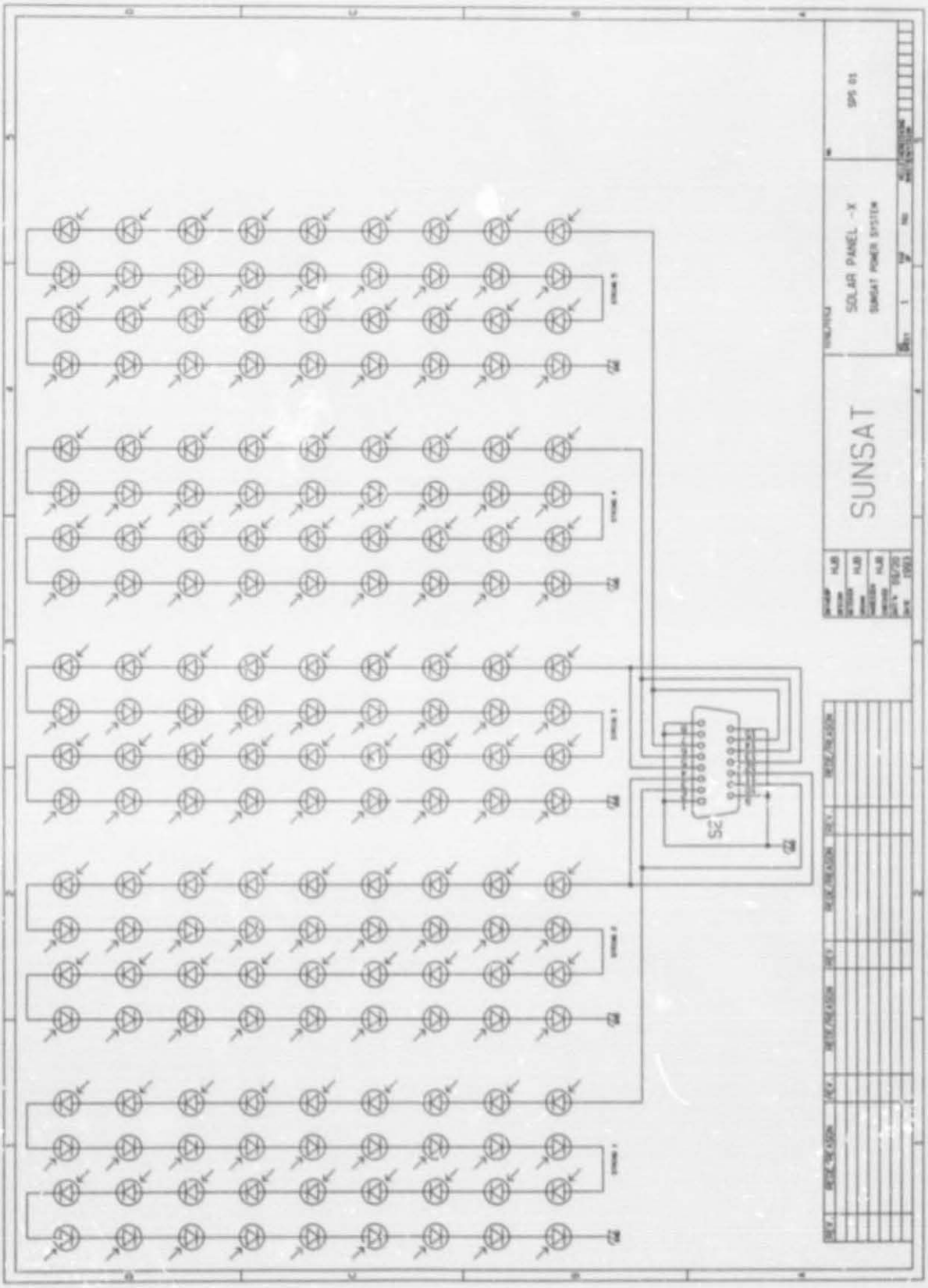

Figure G.2: PV Panel -X of the PV Generator

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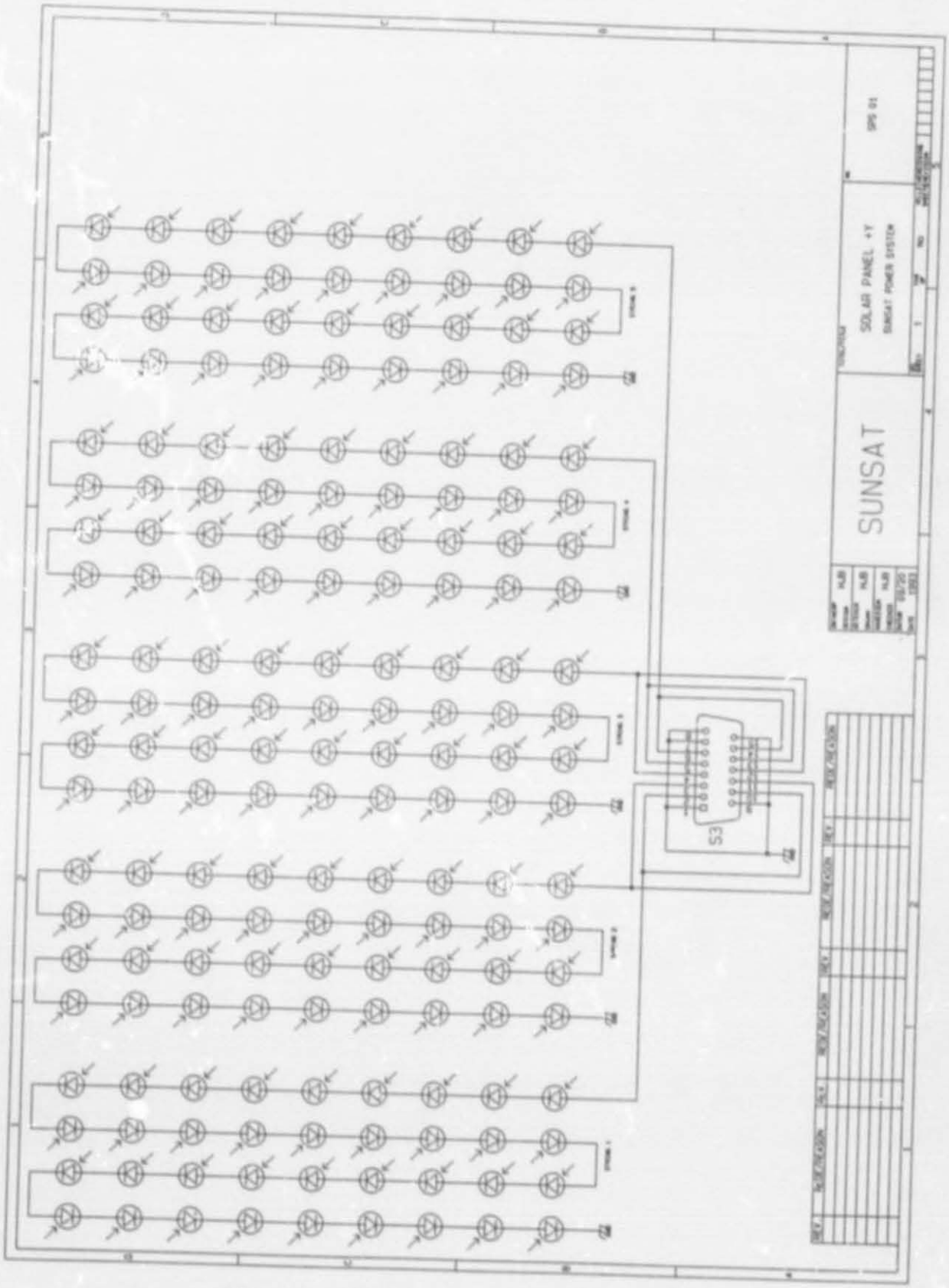

Figure G.3: PV Panel +Y of the PV Generator

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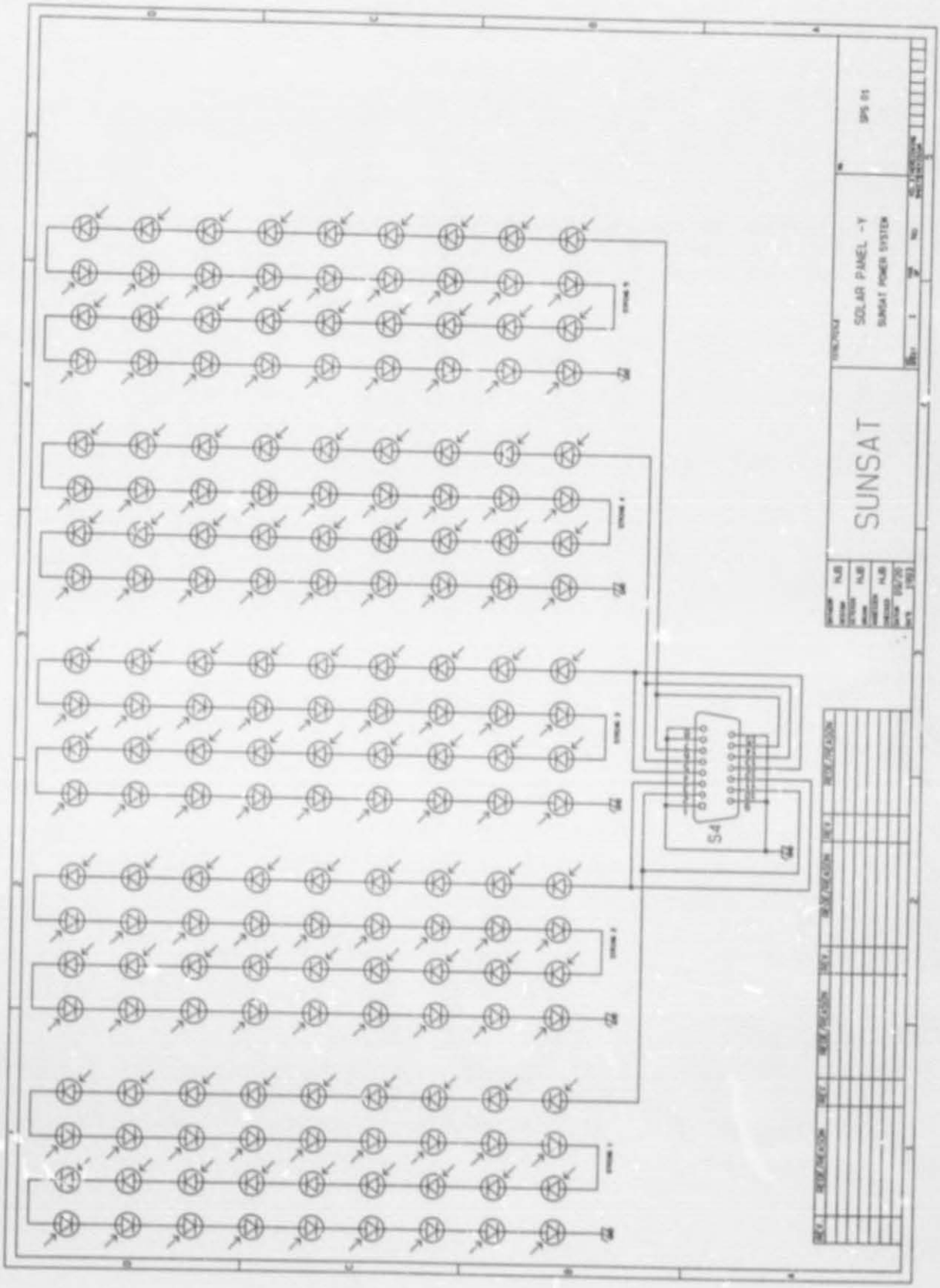

Figure G.4: PV Panel -Y of the PV Generator

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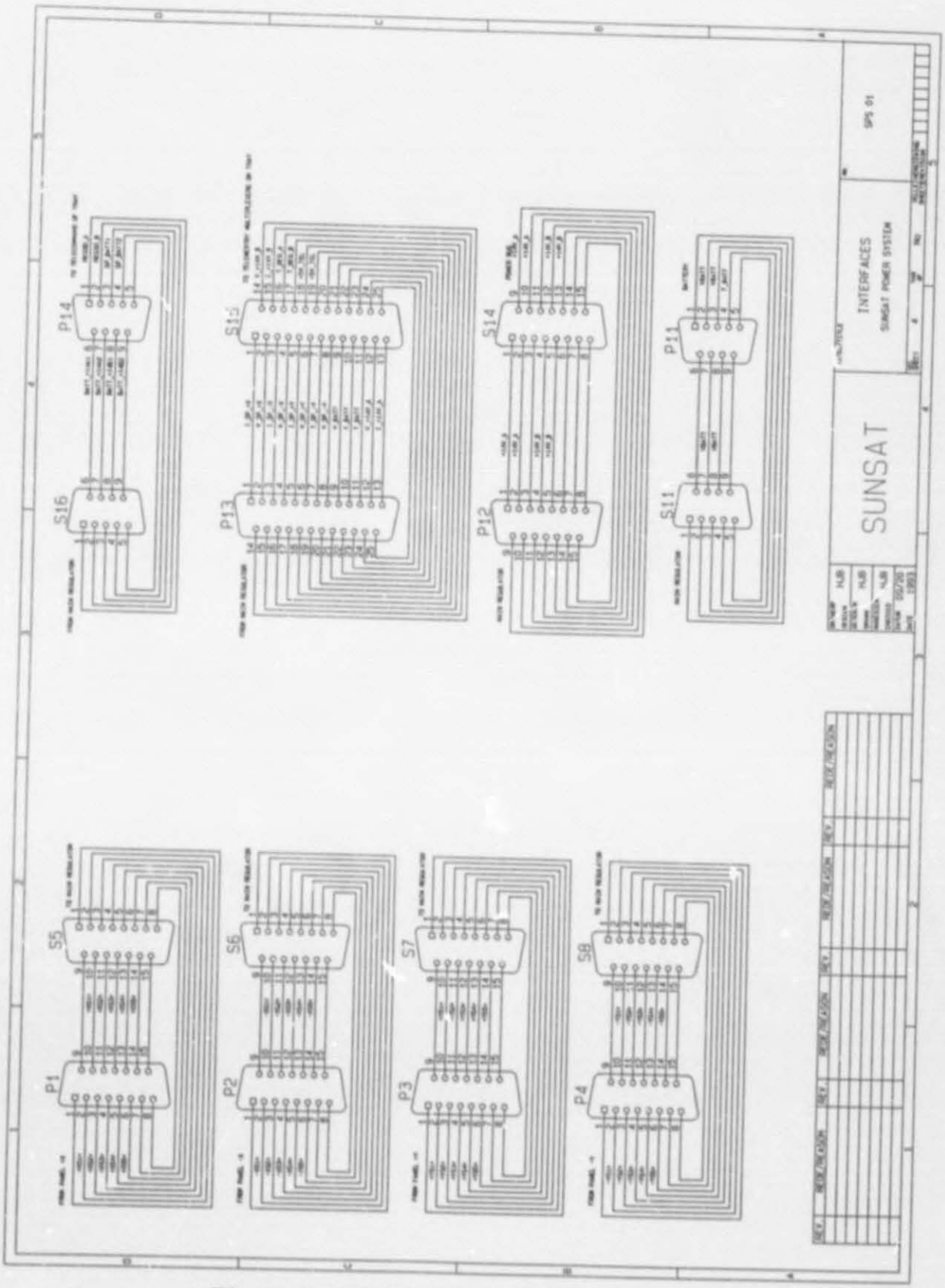

Figure G.5: MRU interface cables and connectors

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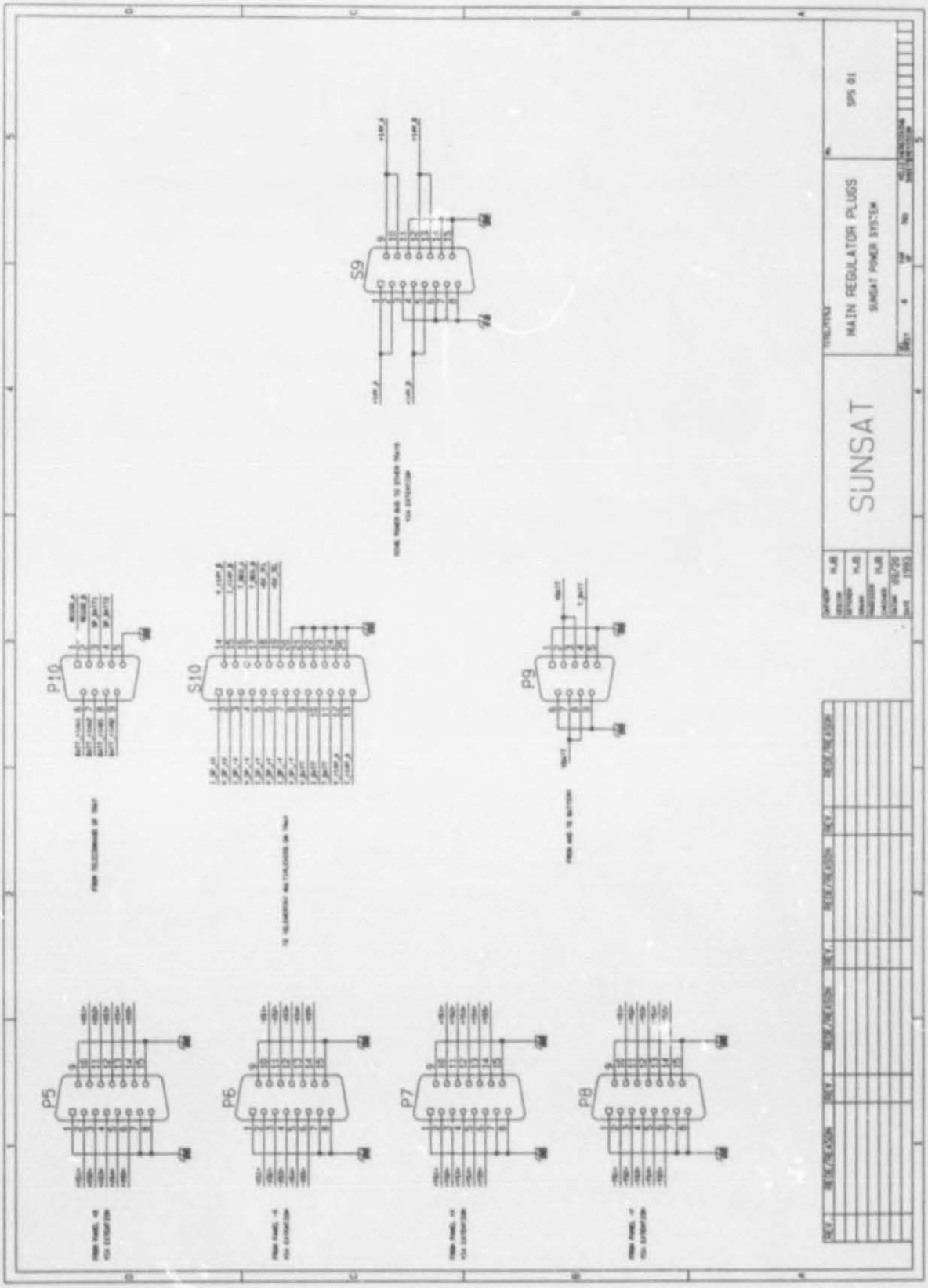

Figure G.6: Connectors on MRU

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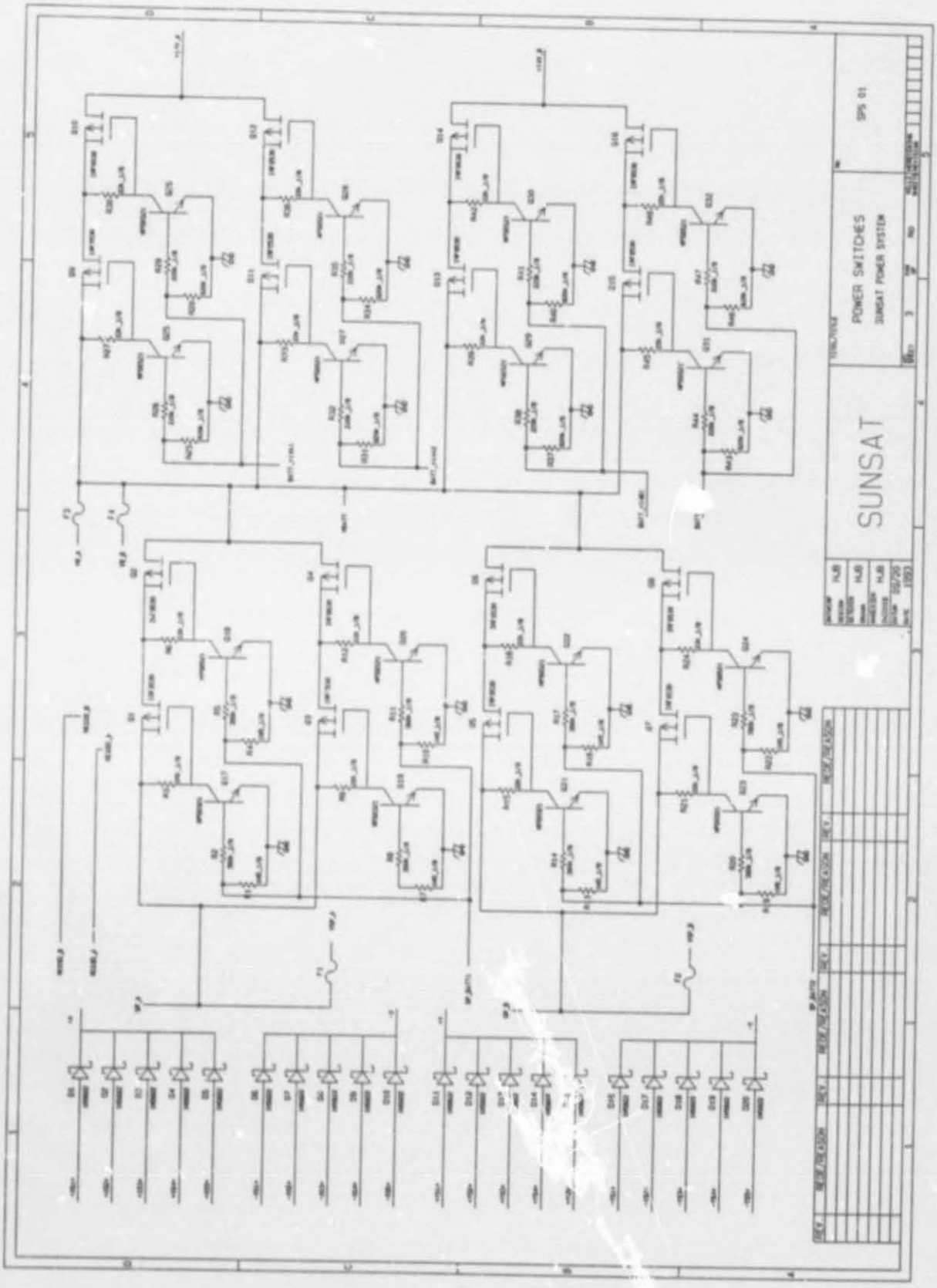

Figure G.7: Power switches of MRU

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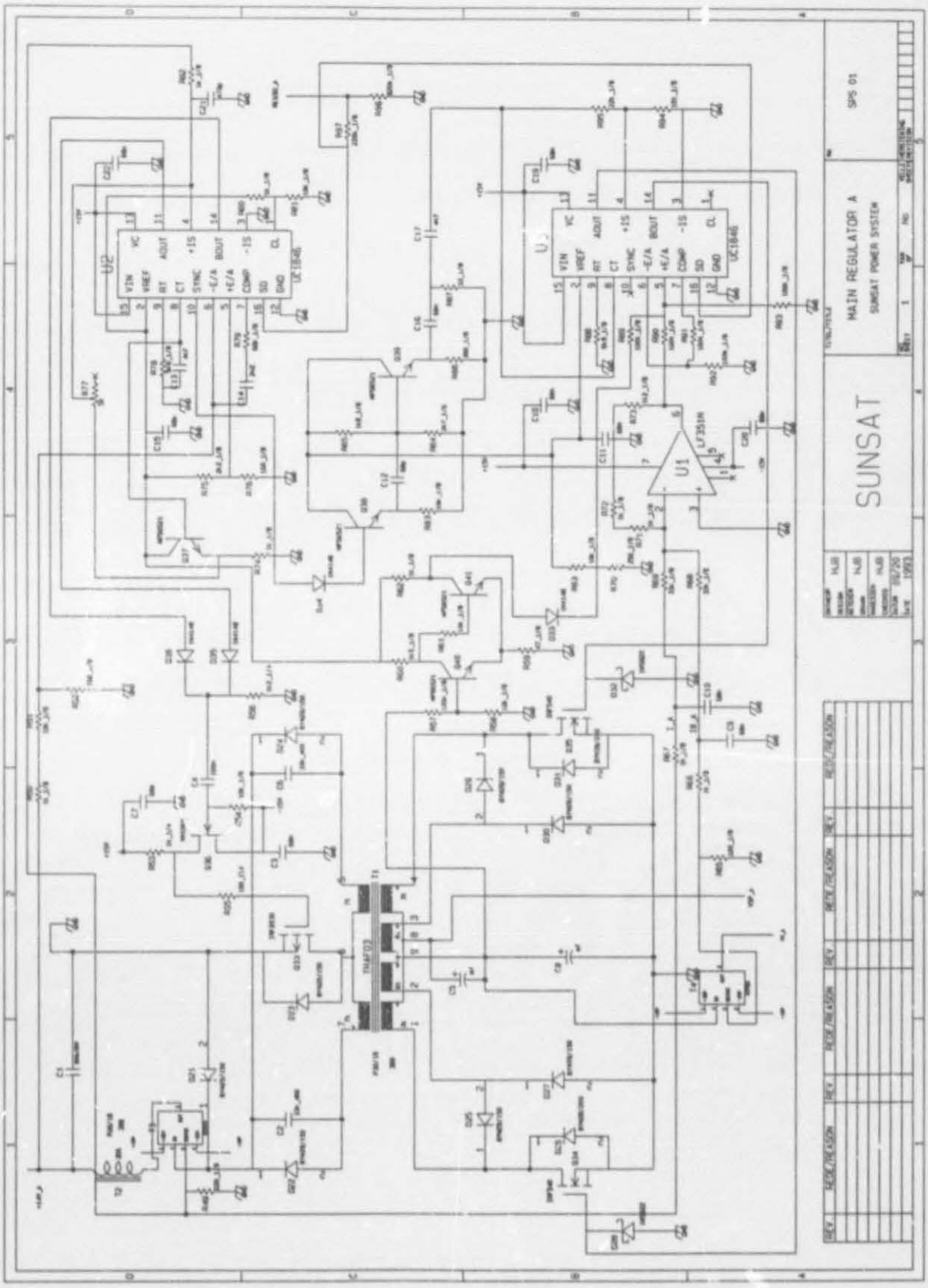

Figure G.8: Main Regulator A

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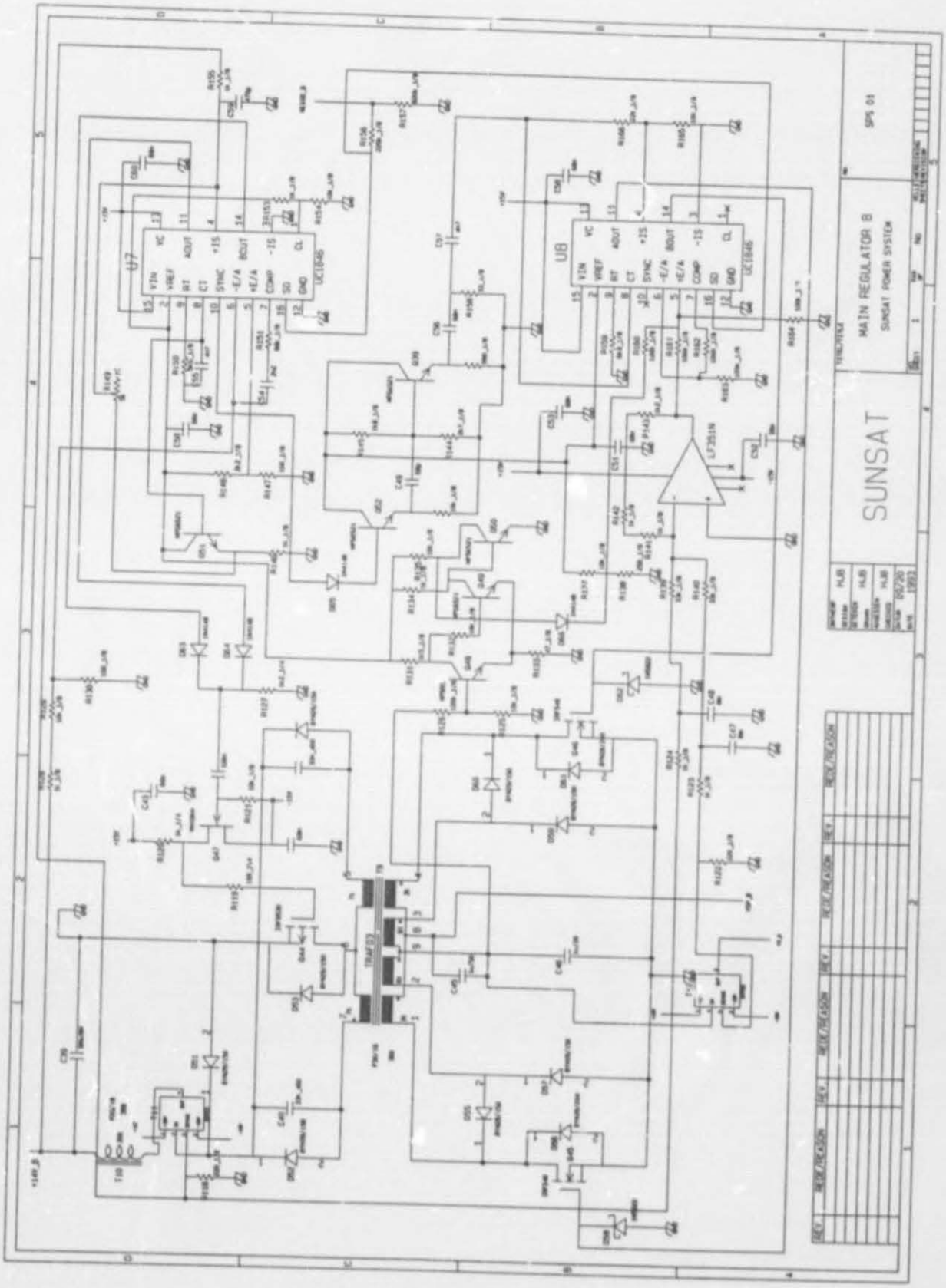

Figure G.9: Main Regulator B

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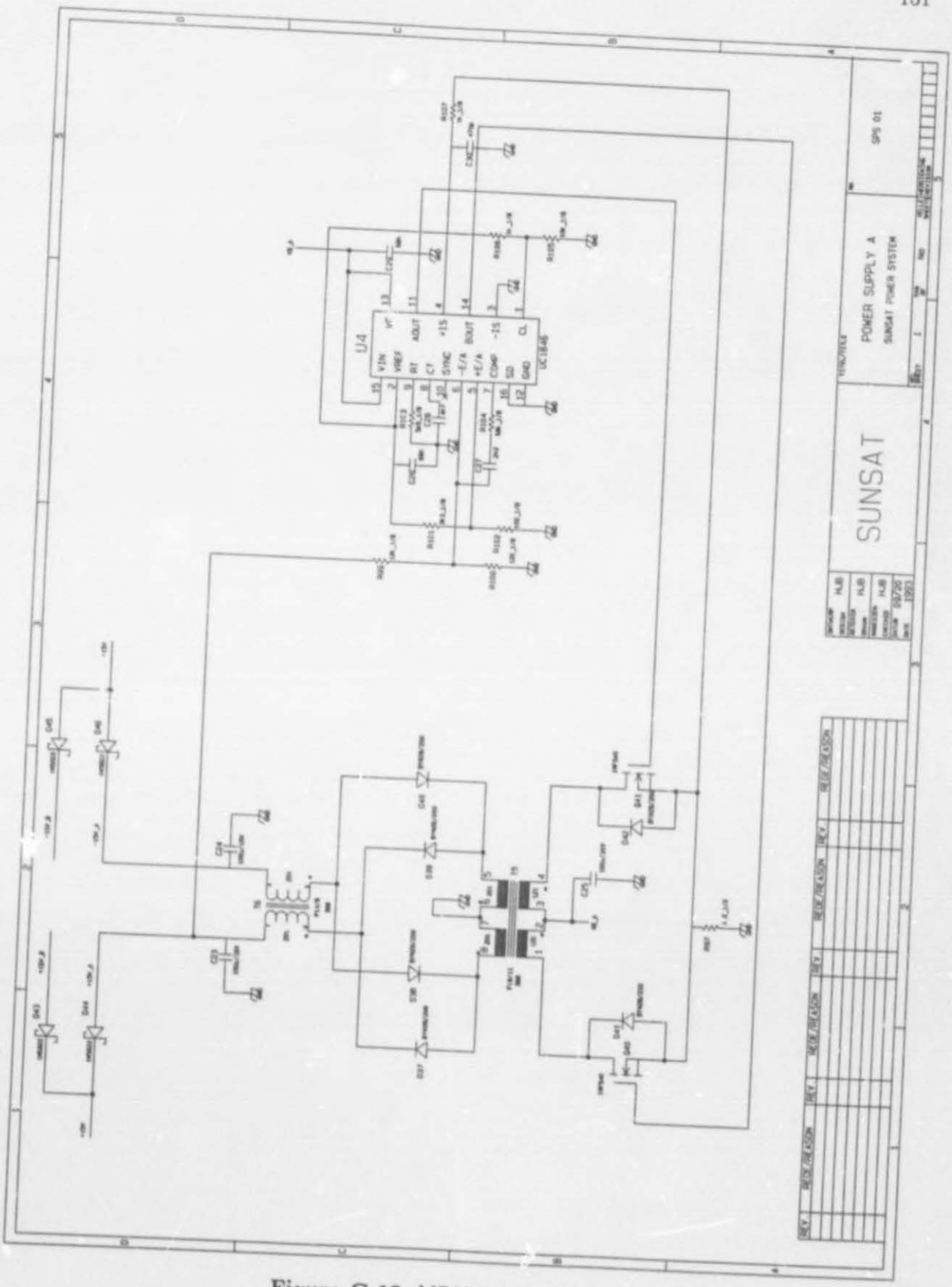

Figure G.10: MRU Power Supply A

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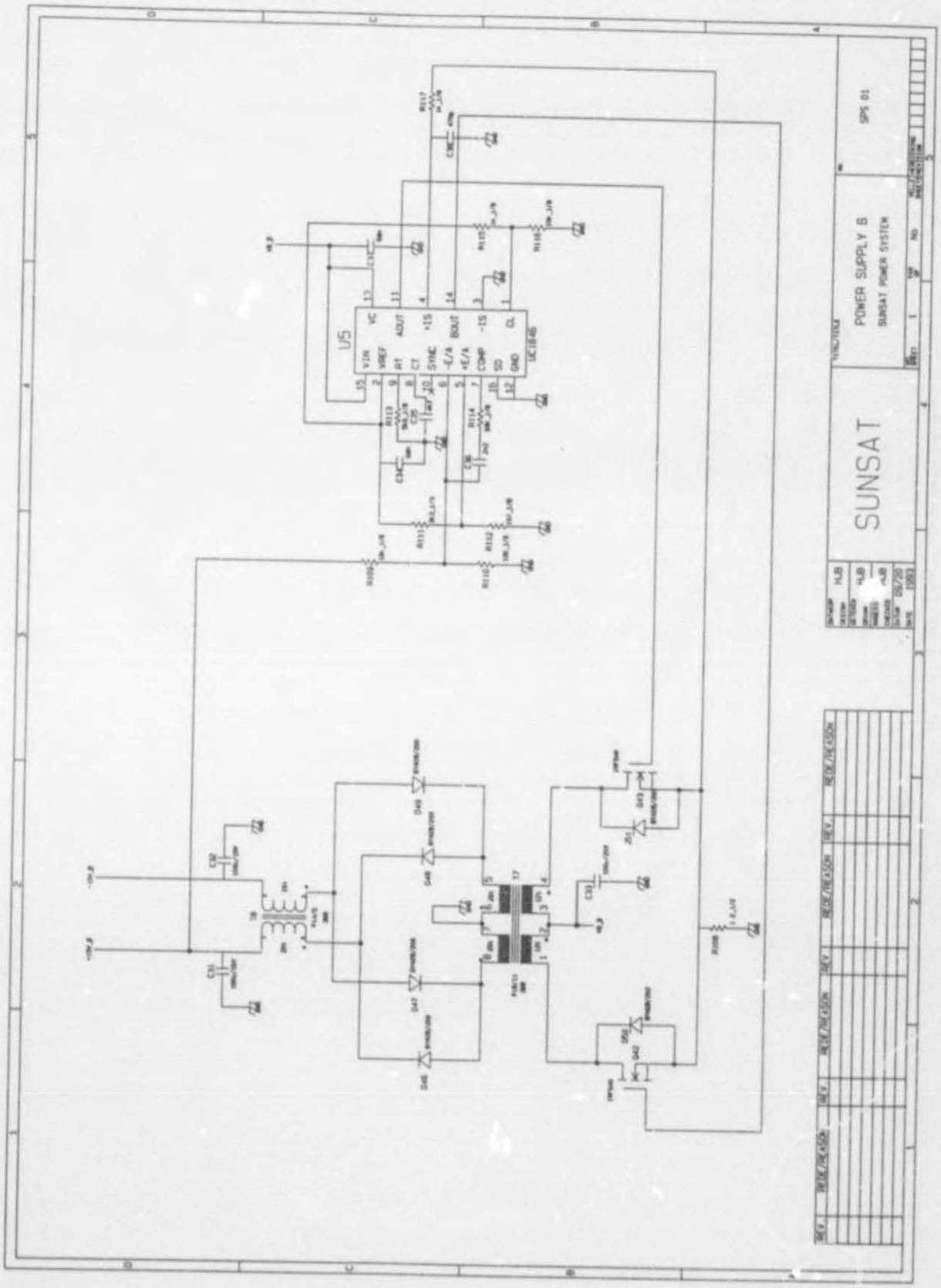

Figure G.11: MRU Power Supply B

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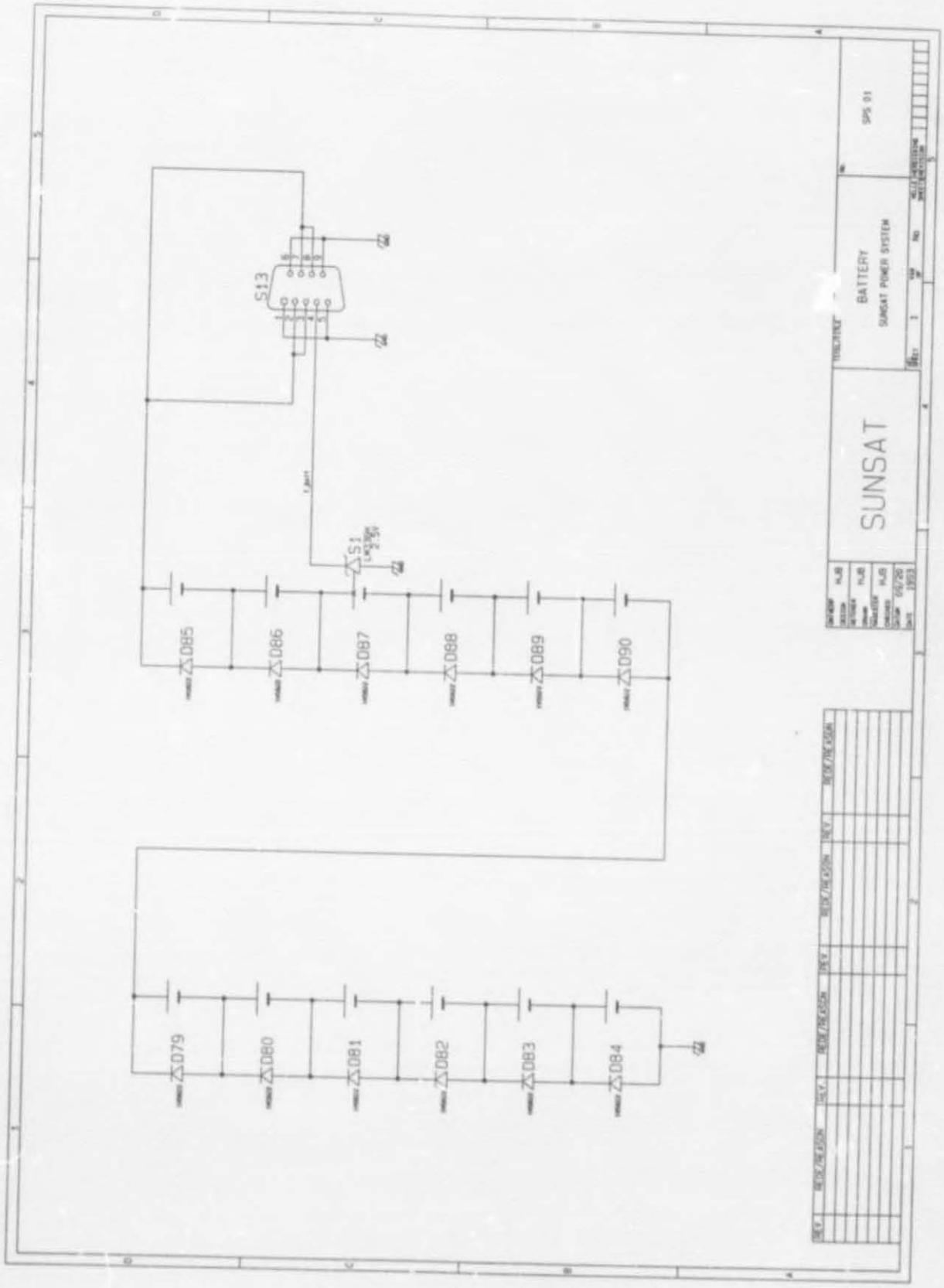

Figure G.12: Battery Unit

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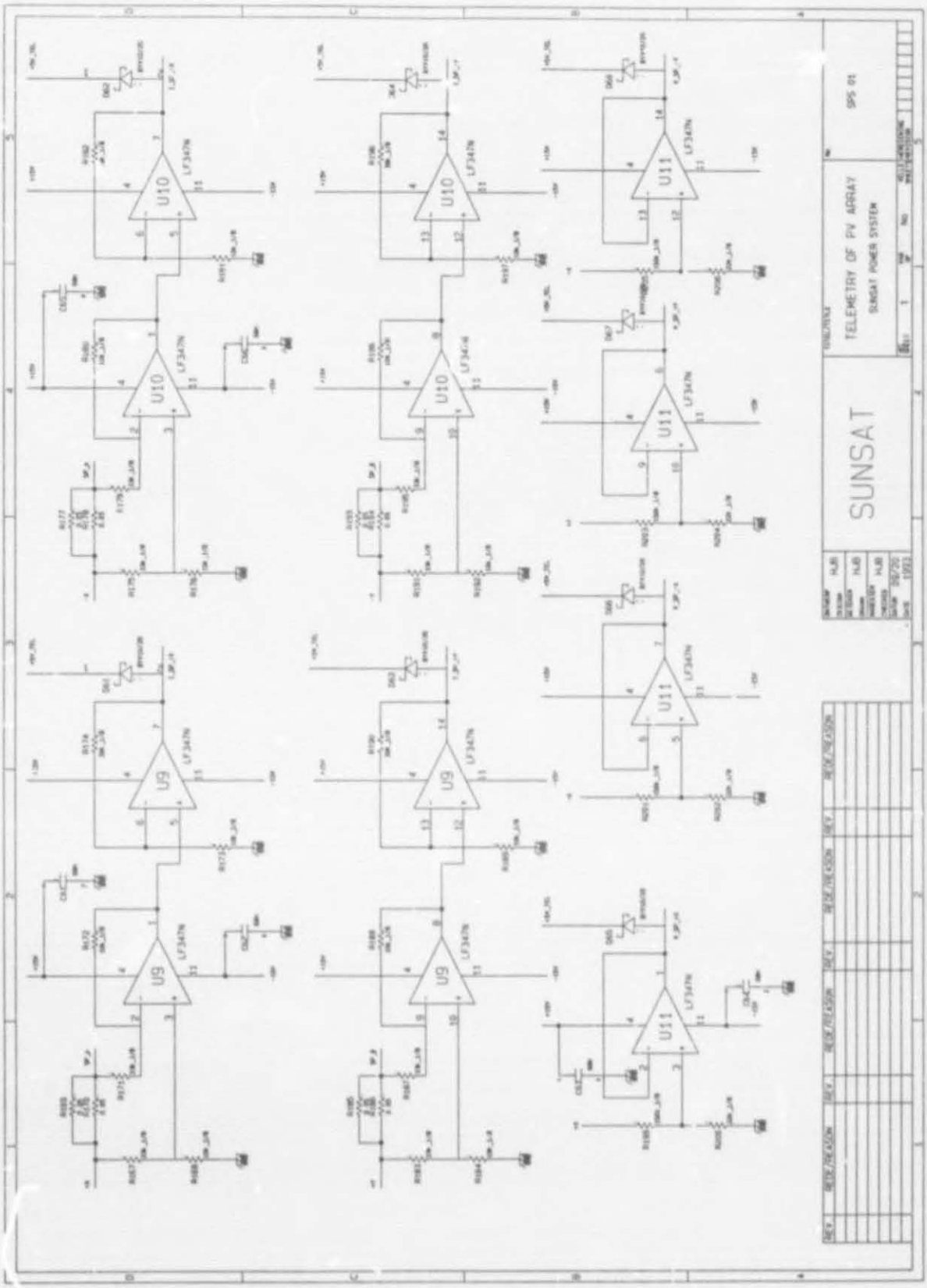

Figure G.13: Telemetry Sensors of PV Generator

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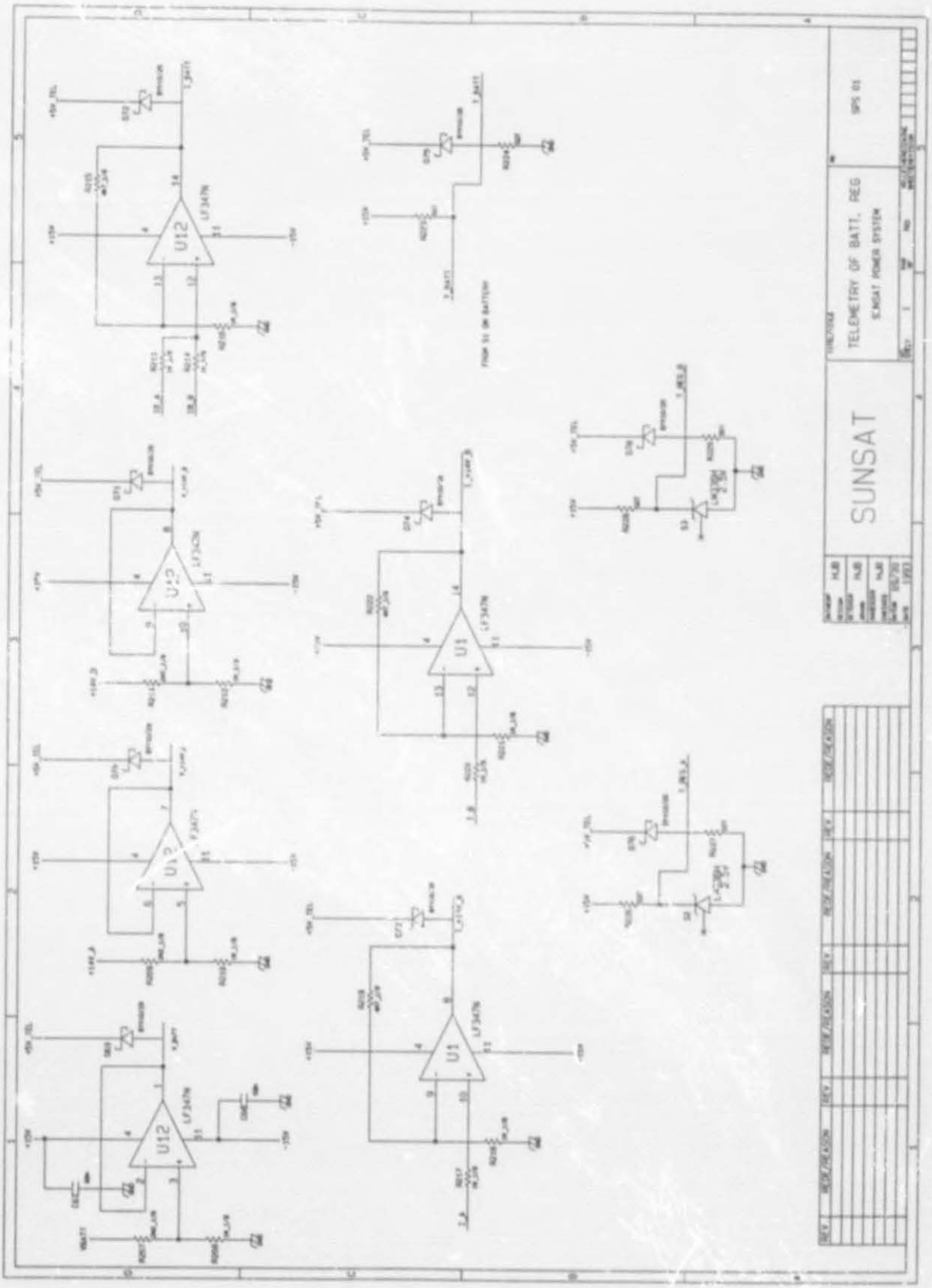

Figure G.14: Telemetry Sensors of battery and regulators

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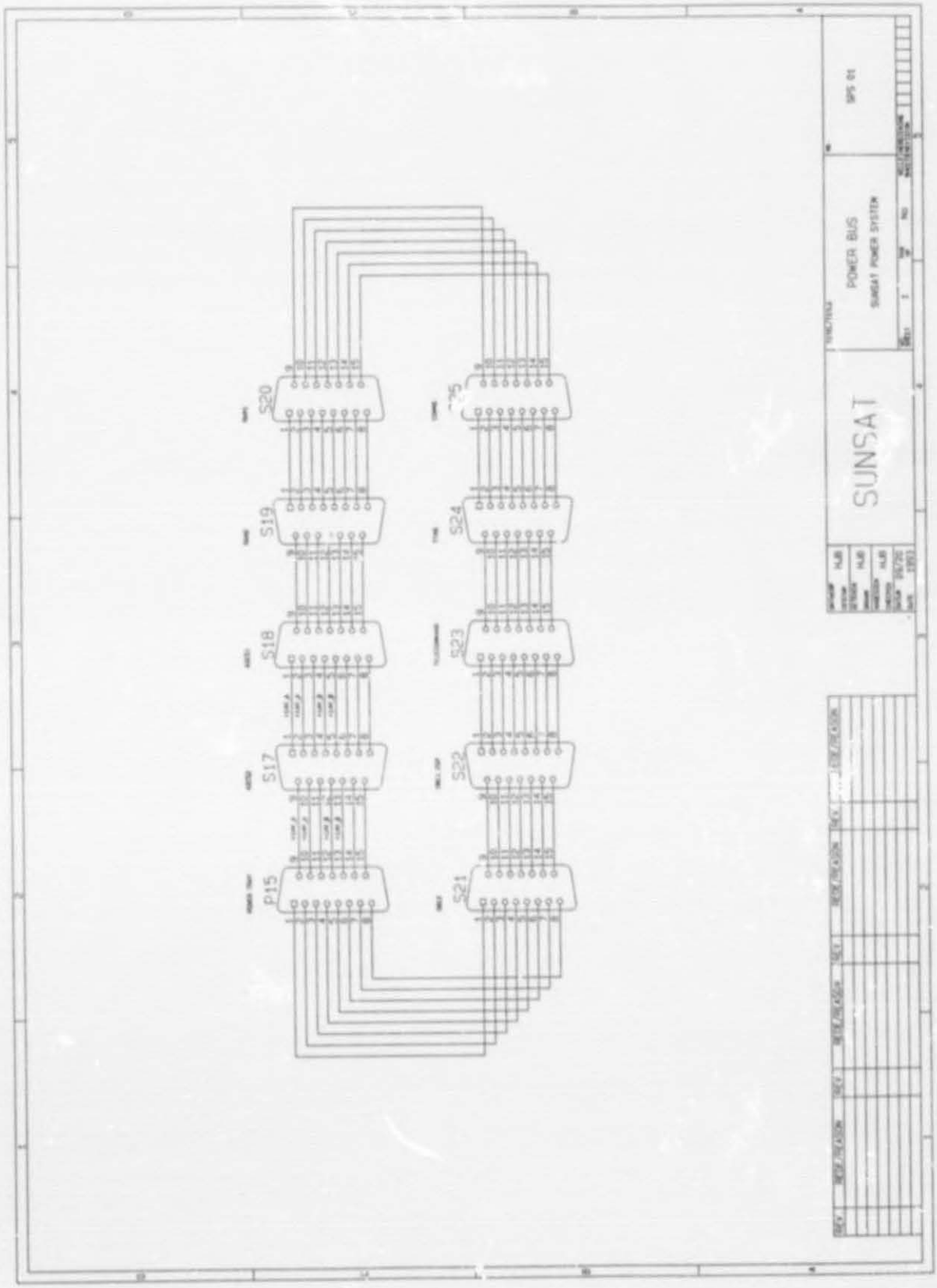

Figure G.15: Ring Bus to the other satellite trays

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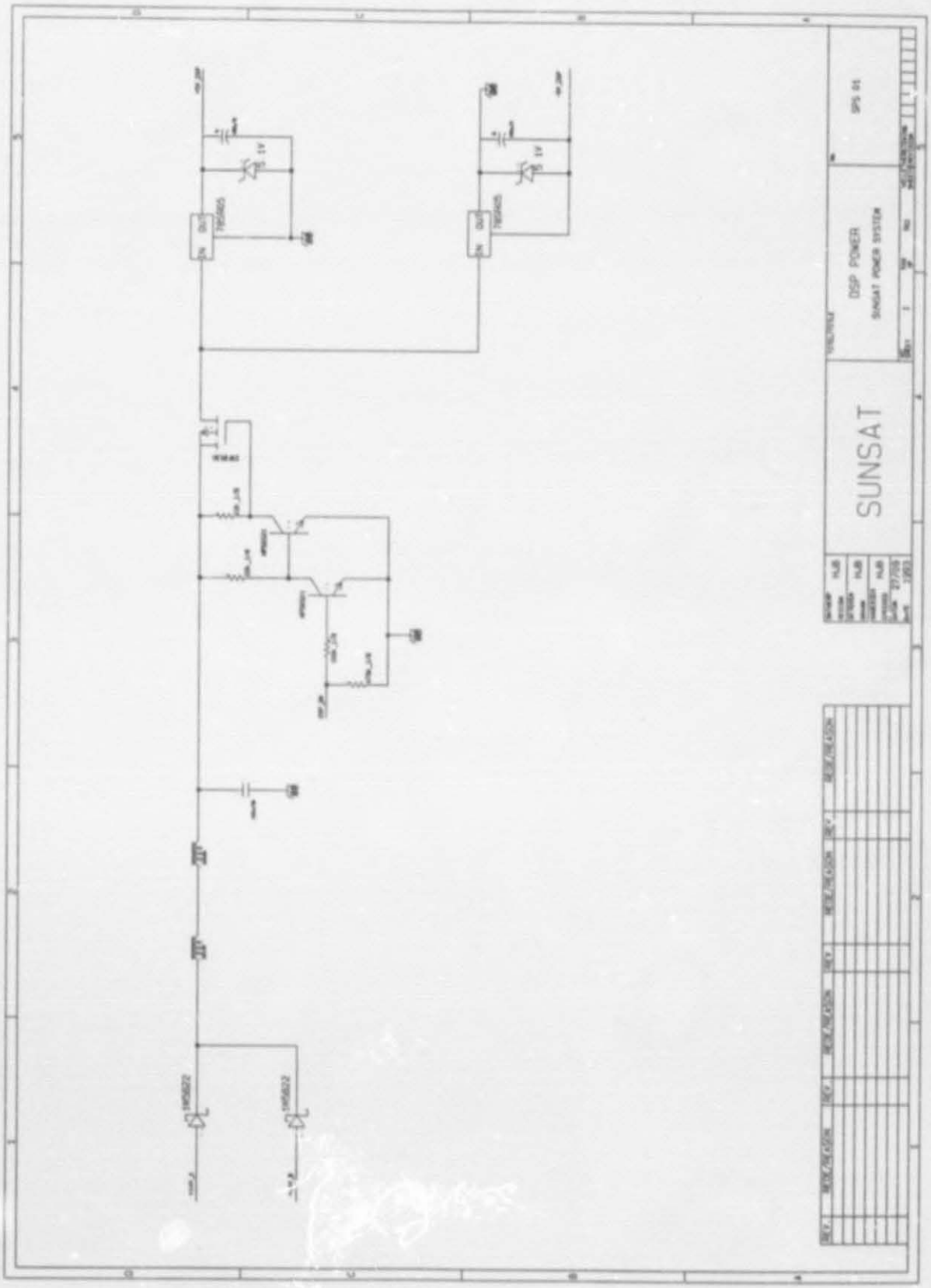

Figure G.16: Power Distribution of Modems

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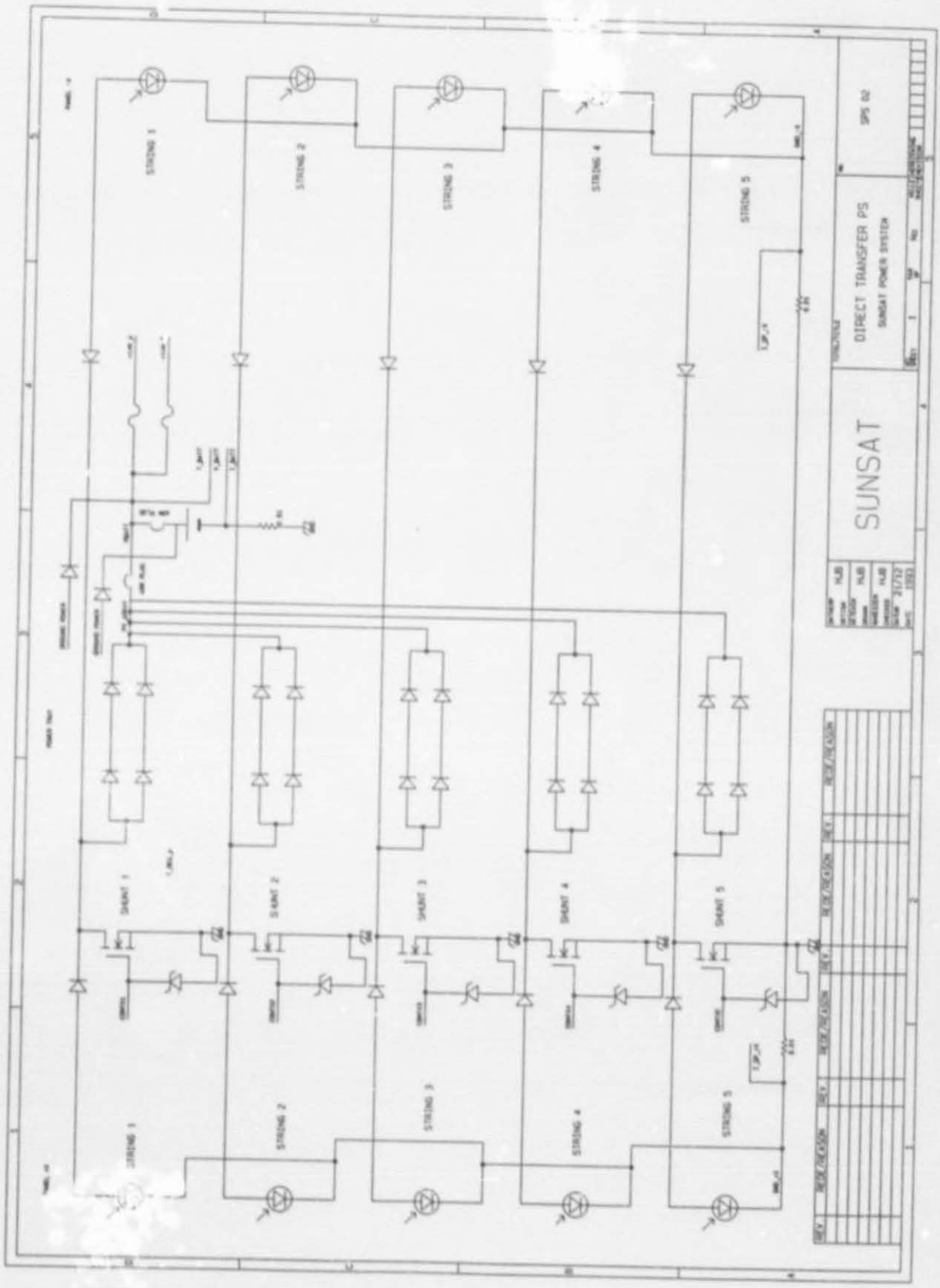

Figure G.17: Shunt regulator for +X and -X panels

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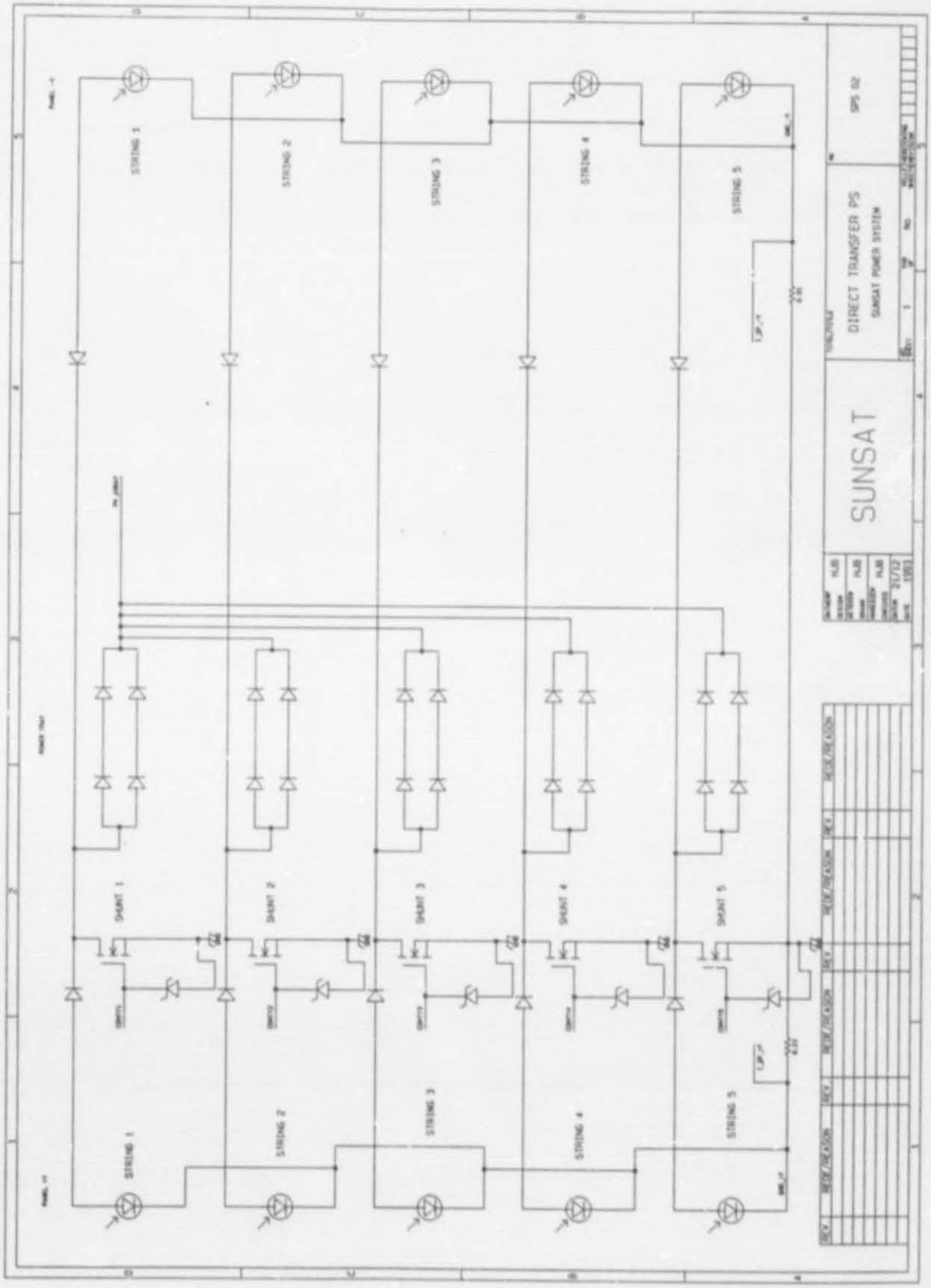

Figure G.18: Shunt regulator for +Y and -Y panels