

Design and Implementation of a RSFQ Superconductive Digital Electronics Cell Library

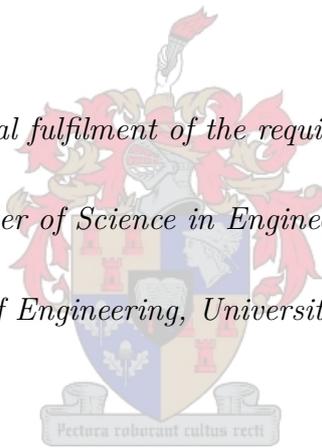
By

Rodwell S Bakolo

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at the Faculty of Engineering, University of Stellenbosch



Supervisor: Dr. Coenrad J. Fourie

Department of Electrical and Electronic Engineering

21 November 2011

Declaration

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Abstract

Design and Implementation of a RSFQ Superconductive Digital Electronics Cell Library

Rodwell S. Bakolo

Thesis: MscEng (Elec)

October 2011

Rapid Single Flux Quantum (RSFQ) cells are key in the design of complex and applicable RSFQ electronic circuits. These cells are low-level circuit elements that are used repeatedly to build larger, applicable RSFQ circuitry.

Making these cells simple to layout and manufacture, but reliable for extensive use demands a careful development process for RSFQ cells. Cell functionality is verified through simulations, thereafter the cell is laid out in special software packages. Inductance of on-chip superconductor structures is extracted through careful modelling with numerical field solver software.

A cell library has been developed by incorporating existing or published cells after further analysis and optimization, as well as developing new cells. Cells that have been adapted into the library include the Josephson transmission line (JTL), Splitter, Merger, D-Flip Flop (DFF), T-Flip Flop (TFF), NOT, AND, OR and XOR, DC-SFQ and SFQ-DC and PTL Driver and Receivers. New cells include NOR, NAND and XNOR. The cells were designed for the IPHT's RSFQ1D $1kA/cm^2$ and Hypres' $4.5kA/cm^2$ processes.

The cells in the library have good bias current operating margins obtained through simulations ($> \pm 26\%$). All cells have all the parameters listed in the thesis including extracted inductance values.

In order to have a complete and verified RSFQ cell library, cells have been sent for fabrication at IPHT and Hypres facilities. These cells can now be tested on-chip, in the laboratory, to establish functionality and practical bias current margins. All test signal patterns and bias currents required for testing are defined to allow co-workers or collaborators to test the cells.

Opsomming

Design and Implementation of a RSFQ Superconductive Digital Electronics Cell Library

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Tesis: M.Sc.Eng. (Elek)

Ocktober 2011

”Rapid Single Flux Quantum” (RSFQ) selle is van sleutelbelang in die ontwerp van komplekse en toepaslike RSFQ elektroniese stroombane. Hierdie selle is laevlak stroombaanelemente wat herhaaldelik gebruik word om groter RSFQ bane mee te bou.

Versigtige ontwikkeling is nodig om hierdie selle eenvoudig vir uitleg en vervaardiging te hou terwyl dit ook betroubaar is vir wye gebruik. Self funksionaliteit word geverifieer deur middel van simulaties, waarna selle vir vervaardiging uitgelê word in spesiale sagtewarepakette. Induktansie van supergeleierstrukture op vervaardigde skyfies word deur versigtige modellering met behulp van numeriese veldoplossingsagteware onttrek.

In hierdie tesis is ’n selbiblioteek ontwerp deur bestaande (gepubliseerde) selle verder te analiseer en optimeer, en deur nuwe selle te ontwerp om die biblioteek volledig te maak. Selle wat aangepas is vir hierdie biblioteek sluit die Josephson-Transmissielyn (JTL), Verdeler, Samevoeger, D-Wipkring (DFE), T-Wipkring (TFF), NIE, EN, OF en XOF, asook die DC-SFQ en SFQ-DC selle en Passiewe Transmissielyn (PTL) drywers en ontvangers in. Nuwe selle sluit die NOF, NEN en XNOF hekke in. Die selle is ontwerp en uitgelê vir beide IPHT se RSFQ1D $1kA/cm^2$ en Hypres se $4.5kA/cm^2$ prosesse.

Die selle in die biblioteek toon goeie voorspanningstroom-werksmarges, soos verkry deur simulatie ($> \pm 26\%$). Parameters en berekende induktansies vir alle selle word in die tesis gelys vir naslaandoeleindes.

Vir die daarstel van ’n volledige en geverifieerde RSFQ selbiblioteek is selontwerpe vir vervaardiging na IPHT en Hypres gestuur. Aangesien vervaardiging slegs een maal per jaar by IPHT gedoen word, is die skyfies egter nog nie beskikbaar nie. Na vervaardiging kan die skyfies egter getoets word om self funksionaliteit in die laboratorium te meet. Ten einde hierdie toetsing vir enige medewerker te vergemaklik, word alle toetsparameters soos voorspanningstroom en intreesinpatrone in die tesis gedefinieer.

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Abbreviations

RSFQ Rapid Single Flux Quantum

DC Direct Current

SQUID Superconducting Quantum Interference Device

IPHT Institute of Photonic Technology

SFQ Single Flux Quantum

SUNY State University of New York

JJ Josephson Junction

GDS Graphic Database System

FSM Finite State Machine

LTS Low Temperature Superconductor

HTS High Temperature Superconductor

LASI Layout System for Individuals

CMOS Complementary Metal Oxide Semiconductor

Chapter 1

Introduction

1.1 Background

A tale of a sweet little accident

In 1911, K. Onnes and G. Holst made a discovery that was special and unexpected. With a modest objective to try and find out the electrical resistance of Mercury at low temperatures, suddenly as they kept on reducing the temperature, the resistance vanished instantaneously. Below 4.2K, Mercury lost its electrical resistance. The question was how and why that had happened. The term superconductivity came up to describe materials that could carry electrical current with no resistance. The sweet little accident brought a fresh excitement and challenges throughout the science community. Scientists had to find out and possibly answer the crucial question and in the process new discoveries were made and theories were developed. The sweet little tale of Superconductivity!

The discovery of the quantum microscopic phenomenon of superconductivity in 1911 [1] resulted in several developments. The discovery of the Josephson junction – a device based on superconductor materials, followed in 1962. This discovery aided scientists and engineers to develop among others things, the most sensitive magnetometers ever realized called Superconductive Quantum Interference Devices (SQUIDs). Later on, circuits based on the Josephson junction were presented. RSFQ circuits were presented in the late nineteen-eighties by K. Likharev and Semenov as a high speed, low power technology based on the Josephson junction [4].

RSFQ circuits remain the world's fastest digital logic, and offer switching speeds several orders of magnitude above the operating speeds of the most advanced CMOS circuits to date. At the time they were presented, RSFQ circuits showed high speeds in the range of hundreds of Gigahertz. Worth noting is a TFF that was demonstrated to operate at a speed of 770GHz [5]. The high switching speeds of RSFQ circuits can be attributed to the two-terminal Josephson junction, because of its intrinsic ability to propagate

small signals at high speeds with very little power consumed. The Josephson junction is presented in detail in the next chapter.

RSFQ has for a long time promised to be a partner and eventual successor of Complementary Metal Oxide Semiconductor (CMOS) in applications where high speed processing and high speeds switching are required. This technology has however over the years faced a number of challenges which include the requirement for low operating temperatures (4K), good magnetic shielding, lack of funding and no clear commercial applications. In recent years, researchers at various institutions have worked hard to put the technology back on track. Analogue to digital converters (ADCs), digital to analogue converters (DACs), low density memory circuits, network switches and many other circuits have been developed and made available for commercial use [6]. One aspect fundamental to the design of complex and applicable RSFQ circuitry is the development of cell libraries.

1.2 Motivation and Objectives

As in CMOS, cells are the basic elements in designing and eventual building of complex and applicable circuitry. A cell is the smallest electronic element set up in such a way as to achieve a specific circuit function or task such as a driver, a logic function such as AND or as a matching element.

RSFQ cell libraries exist at some academic institutions and commercial establishments at different levels of circuit integration. Presently, with the exception of the FLUXON-ICS IPHT library, cells at these institutions are not made readily available to external users. To advance RSFQ circuit research and integration, cell library development is fundamental.

Cells in a library need to be of good working margins to cover for fabrication tolerances and variations in operating conditions. A cell with poor operating margins becomes the weakest point in a complex circuit and as a result, it affects the overall margins of the RSFQ product. This therefore, demands that proper and careful attention be given to all the steps followed in the process of developing a cell library.

To advance research in RSFQ circuits in Africa in general and at Stellenbosch in particular, a cell library had to be developed. This would in turn aid anyone to experiment with new circuits using the cells in the Library.

The work presented in this thesis had one objective; to develop a standard RSFQ cell library for the University of Stellenbosch. Cells developed here will be made available to the broader research community. The objective was broken down into smaller measurable tasks as outlined below.

1. To adapt cells from the available and accessible cell libraries under different design rules and current densities. Adapted cells are to be optimized and best operating parameter values obtained or estimated accordingly.
2. To design new cells so that every digital function is made available in the cell library. Cells to be designed included the NAND, NOR and XNOR. These cells do not exist in the libraries currently accessible and made available to researchers at the institution.
3. To simulate all the cells (adapted or designed) at circuit level and make sure that they work and acceptable margins obtained. Cells that do not produce the right margins have to be re-designed and proper adjustments done until they worked according to specifications.
4. To develop layouts for all the cells in specified software packages. Layouts are the actual cells. A chip designer will need layouts to build complex circuits. Completed cell layouts are to be committed to a repository in GDS format and made available to other researchers. Layout development is to be accompanied by extraction of circuit parameters such as inductance. This has to be done to match the expected design values with the actual values on the layouts. Any differences need to be taken into consideration for verification so that the circuit still works and that acceptable margins are still attainable.
5. To send the completed layouts for the cells for fabrication at either Institute of Photonic Technology (IPHT) in Germany or Hypres in the USA, or both. Cells sent to these facilities to be in line with their design rules and regulations.
6. To have all the fabricated cells tested on-chip in the laboratory. This had to be done to ensure the cells work in the a practical set-up and that the cells could be put to use on a larger scale as part of a complex circuit. Input parameters such as bias currents to be varied in order to obtain on-chip working margins.

1.3 Organization of the Thesis

The following chapters will give a further background to the work outlined and chapters are dedicated to specific tasks.

Chapter 2: Josephson junction

This chapter is dedicated to the general theory of superconductivity, but to a larger extent, presents the theory behind the Josephson junction. Attention has been given to the actual parameters that matter in RSFQ circuits. Temperature dependency of the Josephson junction is also given as it is usually neglected in simulations and when presenting models for the junction.

Chapter 3: RSFQ Technology

The theory behind RSFQ is presented and the current trends and achievements outlined. Shortcomings are presented as well to give the relevance of this work much ground. From its introduction, many researchers have been busy looking at RSFQ technology from every angle to try and mitigate the challenges it has been facing. The cells in the Library have been designed for two processes; Hypres' $4.5kA/cm^2$ and the IPHT's $1kA/cm^2$ processes. Both of these processes are presented in this part of the thesis.

Chapter 4: RSFQ Cells

All the cells are presented in this chapter. Each is presented in circuit form with accompanying theory and how it works. A layout for each cell is also given and necessary comments made on margins obtained and inductance extraction. Each cell is unique but not entirely independent from each other and all cells are treated as such. Cells are normally simulated and tested with interface cells; this gives a near-practical set of results. This chapter forms the core of the work presented in this thesis.

Chapter 5: On-Chip RSFQ Cell Testing and Results

Chapter five presents the procedure for on-chip testing for all the fabricated cells. Each cell has its test concept and layout presented. Testing of cells was to be done in the laboratory with a cryocooler or Helium cooling providing the necessary cryogenic environment. In addition layouts for some of the chips are discussed in this chapter.

Chapter 6: Conclusions and Recommendations

Highlights of the work presented in this thesis are given in this chapter. Problems encountered at each implementation stage are outlined and a number of recommendations given on the areas that still need attention to further compliment the efforts of this work.

Chapter 2

Josephson Junction

*I can do all things through Christ who strengthens me - **Philippians 4:13***

This chapter discusses the basics behind the Josephson junction with a little background theory on superconductivity as a preamble. Much of the attention is given to the parameters that affect the operation and DC response of the Josephson junction. Simulation results are also presented to show how the junction behaves and why it is the right device for RSFQ electronics. Models are normally used to closely describe the operation of the Josephson junction under different environments and applications. It is for this reason that an effort has been made to present the various parameters that are used to build simulation models, including temperature dependency, which is not easy to incorporate in such models.

2.1 Background to Superconductivity

Superconductivity is a phenomenon that occurs below specific critical temperatures, in some special materials, that is characterized by the loss of electrical resistance. Below the critical temperature, T_C , the superconductor material not only loses its resistance, but also expels all the magnetic flux that existed before being cooled. The superconductor becomes diamagnetic - due to the acquired ability to weaken magnetic field [7]. The phenomenon is well observed during the normal - to - superconductor transition. It is also called the Meissner effect [1]. The superconductor is able to expel the magnetic field by cancelling it out through a perpetual surface current. This expulsion though, is not ideal as some of the external flux is able to penetrate the superconductor to a small depth called the *London penetration depth*, λ [1]. Different superconductor materials have different values of λ .

At the sub-atomic level, superconductivity is caused in materials when the electron attraction overcomes the repulsion [8]. The Coulomb force causes repulsion between

electrons and attraction between electrons is provided by the lattice. In normal situations (i.e. no superconductivity) electrons, being equal in charge, repel one another. That is however reversed when a material enters the superconductive state.

A superconductor can, however, lose its superconductivity when too much current flows through it or it is subjected to too strong a magnetic field. Critical current, I_C , and critical magnetic field, H_C , are the points at which superconductivity is lost - the superconductor becomes normal and it can no longer expel magnetic field until either the field or current is reduced below the critical values [9].

The type of superconductors that completely expel the magnetic flux when $H < H_C$ is called Type I superconductors. Superconductors under this type are usually pure elements like Mercury, Aluminium, Lead and Tin. Type II superconductors do not completely expel all the flux inside them, even when the applied field is less than the critical field, $H < H_C$. Type II superconductors are thus not perfectly diamagnetic. In Type II superconductors, superconducting vortices penetrate the superconductor, carrying a magnetic flux equivalent to the magnetic flux quantum, Φ_0 .

$$\Phi_0 = \frac{hc}{2e} \cong 2.07 \times 10^{-15} \text{Wb} \quad (2.1)$$

The imperfect expulsion of magnetic flux in Type II superconductors results in a superconductor state with non-zero resistance. The resistance is, however, quite small and can be ignored. Most of the practical applications of superconductivity employ Type II materials. In 1961, Deaver and Fairbank [10] established that in a superconducting ring, magnetic flux exists in small quantized amounts as integer multiples of the flux quantum, Φ_0 . This was a crucial discovery that enabled further research in superconductor electronics. Specially, flux quantization theory is applied in RSFQ circuits and SQUIDS. Examples of Type II superconductors include pure elements like Niobium and Vanadium and also some metal alloys and complex copper oxides.

Superconductors are also described and categorized based on their critical temperatures. The first category of superconductors to be discovered was the low temperature superconductors in 1911, followed by the high temperature type in 1986. These two categories are discussed next.

2.1.1 Low-Temperature Superconductors (LTS)

Low T_C superconductors are universally referred to as *classical* and they were the first to be discovered in 1911 [10]. This category of superconductors has much lower critical temperatures, mostly below $10K$. Such materials include Mercury ($4.2K$), Aluminium ($1.18K$) and Niobium ($9.3K$), amongst other materials [10]. Liquid Helium is a coolant of choice for this category, because of its low boiling point ($4K$). For a long time,

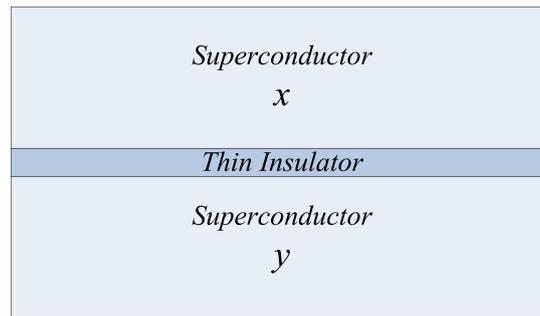


Figure 2.1: Conceptual diagram of the Josephson Junction

Niobium has been the prominent superconductor for low- T_C electronics. An oxide of Aluminium is used in Niobium-based Josephson junctions as a thin insulator and the junction become $Nb/AlO_3/Nb$.

2.1.2 High Temperature Superconductors (HTS)

The critical temperature of HTS is much higher than the LTS. In 1986, Bednorz and Muller discovered superconductivity in LBCO (an oxide of Lanthanum, Barium and Copper) with a critical temperature of $\sim 35K$. This was a very exciting and ground breaking discovery into another domain of superconductivity. The high T_C means that less intense cooling is required to bring the material to the superconductive state. Higher critical temperatures were realized in the subsequent years, such as YBCO (an oxide of Yttrium, Barium and Copper) with a T_C of $\sim 90K$. Even higher critical temperatures have been discovered with some oxides achieving superconductivity at $130K$ [10][11].

The only challenge with promising trends is the increased prominence of noise with an increase in operating temperatures. Any circuit designs with HTS have to take this into consideration and work on reducing the effects of noise.

Liquid Nitrogen is used to cool down the metals below their critical temperatures, because of its much higher boiling point than Helium used in LTS.

2.2 Josephson junction

A Josephson junction is a two-terminal three layer device. It is made up of two superconductor layers separated by a thin insulating material. Fig. 2.1 illustrates the concept.

The JJ depends on the Josephson Effect, which was predicted by Josephson in 1962 [1, 10, 11]. The Josephson Effect defines the tunnelling of electrons through the insulating material at a temperature of absolute zero (0K). The electron tunnelling offers an explanation to the flow of electrical current in the junction when a small current

(i.e. less than the critical temperature I_C) is applied. The BCS theory (named after the authors Bardeen, Cooper and Schrieffer) further illustrates that in superconductors, electrons exist in pairs known as Cooper pairs. The Cooper pairs are able to tunnel through the insulation barrier into the other superconductor material thereby aiding a flow of electrical current.

Superconductors arranged as in Fig. 2.1 can be described with a single wave function with a defined phase, $\Psi_{x,y}(r)$. The phase relation function is only meaningful if the superconductors are separated by a meaningful distance. If the separation $r = 0$ the superconductor layers become one and $\Psi_{x,y}(r) = 0$. However if the superconductors are too far apart, the phase relation becomes undefined.

The formation of the Josephson junction by two superconductor plates and an insulator separation necessitates the inclusion of other circuit parameters; Resistance and Capacitance. The origin and significance of these parameters are hereby discussed.

2.2.1 Junction Resistance and Capacitance

Resistance

By increasing the current flowing through a junction, an idealized I-V curve of the Josephson junction can help to support the inclusion of resistance in the junction model. Referring to the Cooper pair theory [8], the Cooper pairs tunnel through the junction insulation when $I < I_C$ and no voltage develops across the junction. The current that continually flows through the junction when $I < I_C$ is caused by the tunnelling of the cooper pairs. When $I = I_C$, the junction develops a voltage across its plates - the superconductor plates - see Fig 2.1. This voltage is precisely equal to $2\Delta_0/e$. where Δ_0 is the energy gap. This voltage potential is large enough to break the Cooper pairs into single stand alone electrons. In Fig. 2.1, it can be observed that, after the junction develops this potential, a linear response is produced by the junction. The junction is said to have transitioned from the superconductor state to the voltage (normal) state. Such a response is depicted in Fig 2.2 by the solid line with a precondition that the operating temperature is below T_C . If $T > T_C$ the response will be purely ohmic as represented by the dashed line in Fig 2.2. A further increase in the applied current simply extends the linear response.

The voltage across the junction increases with increased applied current, which translates into a proportional relationship $V \propto I$ and therefore $V = kI$. where k is a parameter to be defined next. It is known as the *Normal Resistance* R_n , because it is universally accepted to result from the tunnelling of normal electrons across the junction insulation barrier. Unlike the super electrons - in Cooper pairs - normal electrons have a wave function that has a random phase. The undefined pattern of the phase means that the normal electrons move in all directions in a random pattern, thereby hitting each other.

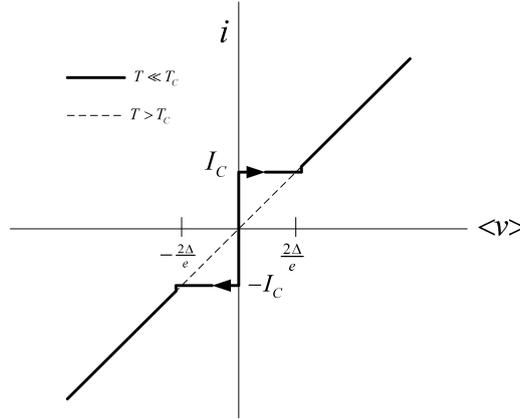


Figure 2.2: Josephson Junction response to gradual increases in applied current i - redrawn after [1]

When electrons hit each other their velocities are changed and so are their directions of motion. This introduces some form of resistance or drag to the motion of electrons, which can only be expressed in circuit form as a resistance. The normal electrons can occur in superconductors, but they are largely due to the break up of Cooper pair electrons.

From this explanation, it clearly shows that R_n depends on the junction area, which contributes the total electrons to tunnel, and the current density (J_C). Considering that the junction has two states, the total conductance in the junction can be expressed as a voltage dependent function, $G(v)$ at $T = 0K$.

$$G(v) = \begin{cases} 0 & \text{if } |v| < 2\Delta_0/e \\ \frac{1}{R_n} & \text{otherwise} \end{cases} \quad (2.2)$$

where $G(v)$ is the the dependent conductance, which is the reciprocal of the normal resistance.

The two fluid model however, presents a rather interesting addition to this concept. It says that even at $|v| < 2\Delta_0/e$, normal electrons exist and can result in a resistance through normal tunnelling. The resulting resistance is called the *Sub-gap Resistance*, R_{sg} . The sub-gap resistance appears at non-zero temperature and it is therefore accurate to present it as a temperature dependent parameter, $R_{sg}(T)$, although some imperfect junction may still show this resistance even at zero temperature. At this instance, the resistance is referred to as *Leakage Resistance*. It is therefore accurate to express (2.2) as follows [1, 10, 11]:

$$G(v) = \begin{cases} \frac{1}{R_{sg}(T)} & \text{if } |v| < 2\Delta_0/e \\ \frac{1}{R_n} & \text{otherwise} \end{cases} \quad (2.3)$$

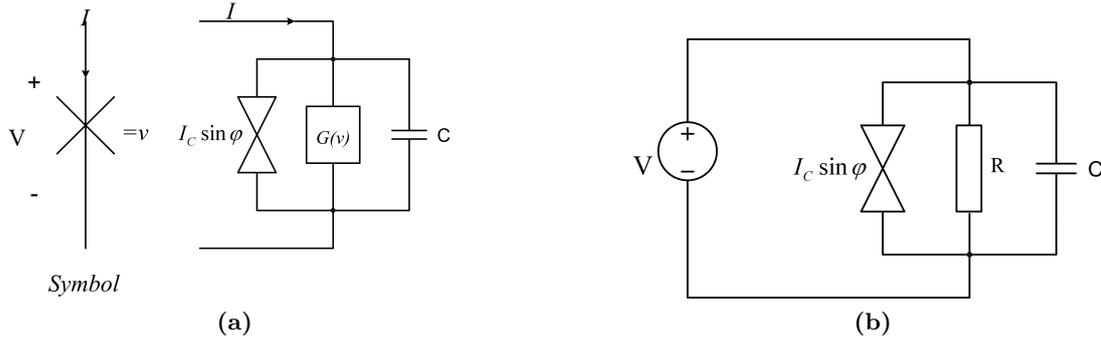


Figure 2.3: The Josephson Junction generalized model [1]: (a) shows the voltage dependent conductance branch, $G(v)$ while (b) show R as a replacement of $G(v)$ as explained in the text.

This expression further shows the dependency of $G(v)$ on temperature.

Therefore, the junction should include a resistance in its circuit model which takes the form of R_n or R_{sg} .

Capacitance

The arrangement of the superconductor layers with an insulation barrier as a separation creates a capacitor with the superconductor layers acting as capacitor plates and the insulator as the dielectric. Suppose d is the thickness of the insulator, or the separation between the two superconductor layers, and A the effective area of the junction, then the total capacitance can be expressed as

$$C = \frac{\epsilon A}{d} \quad (2.4)$$

where ϵ represents the permeability of the insulation barrier.

With resistance and capacitance presented, a generalized model of the Josephson junction can be analysed showing the three parallel branches. Fig. 2.3 illustrates the model.

The $G(v)$ branch is simplified by employing some necessary assumptions to make the analysis easier, but as practical as possible. It simplifies to $\frac{1}{R_n}$. This simplification removes the temperature dependency of the junction as it was represented by $R_{sg}(T)$, and therefore the resulting junction model is approximate. The resulting model is called the Resistively Capacitively Shunted Junction (RCSJ) or simply Resistively Shunted Junction (RSJ) as shown in Fig. 2.3.

By applying Kirchhoff's current law a generalized expression for the total current i flowing into the junction is shown;

$$i = I_C \sin \phi + \frac{v}{R_n} + C \frac{dv}{dt} \quad (2.5)$$

The first part of the equation shows the phase dependency of the super current that flows through the junction. If $v = \frac{\Phi_0}{2\pi} \frac{d\varphi}{dt}$, then (2.5) becomes

$$i = I_C \sin \varphi + \frac{1}{R_n} \frac{\Phi}{2\pi} \frac{d\varphi}{dt} + C \frac{\Phi_0}{2\pi} \frac{d^2\varphi}{dt^2}. \quad (2.6)$$

2.2.2 DC Response of the Josephson Junction

RSFQ circuits are based on DC and therefore it is necessary to present the response it exhibits to DC sources. The junction's response depends on a number of factors, which include time constants, the characteristic voltage and the Stewart-McCumber parameter [1].

1. Time Constants: Two time constants are crucial; the Josephson time constant $\tau_J = \frac{1}{2\pi f_J}$, where $f_J = \frac{v_o}{\Phi_0}$, represents the Josephson frequency and the capacitive time constant $\tau_{RC} = RC$. The capacitive time constant can be controlled by varying the value of R . These time constants affect the overall switching speed of the junction.
2. Characteristic voltage: A constant voltage which is dependent on the junction geometry, material and fabrication density. The significance of this parameter is further discussed in the coming sections. It is expressed as $V_o = I_C R_n$. Any resistance connected in shunt with the junction affects the value of the resistance and hence V_o .
3. The Stewart-McCumber parameter β_C : It is the ratio of the capacitive time constant to the Josephson time constant, $\beta_C = \frac{\tau_{RC}}{\tau_J}$.

$$\beta_C = \frac{2\pi I_C R_n^2 C}{\Phi_0} \quad (2.7)$$

The DC response of the junction is looked at by analyzing three instances defined by the value of β_C . Two border cases are used where the value of $\beta_C \ll 1$ and $\beta_C \gg 1$, and one general case. (2.6) forms the basis of all the analyses pertaining to junction response.

$$\beta_C \ll 1$$

For $\beta \ll 1$, τ_J is dominant and dictates the operation of the junction. This is the case, because the value of C is too small and often neglected in analyses. Therefore $\tau_{RC} \ll \tau_J$ and the junction model does not have the capacitor branch. When $I < I_C$ all the current flows through the basic junction branch (Fig. 2.3). However, when $I > I_C$ some of the current flows into the resistor branch and creates a voltage across the junction terminals. Upon reduction of the current from above I_C , the response of the junction retraces the

earlier pattern as the current was increased. Fig. 2.4(a) shows the response. As shown in the figure, no hysteresis occurs. The small value of the capacitance improves the switching speed of the junction.

$$\beta_C \gg 1$$

The second boundary case is when $\beta_C \gg 1$. In this case the capacitance is large and therefore $\tau_{RC} \gg \tau_J$. The behaviour of the junction depends on the RC product, because now τ_J has little effect. For $I < I_C$ two solutions exist. The first solution relates to a super current that still flows despite τ_J being insignificant. The second part relates to a voltage across the resistor due to some of the current that flows through it. This behaviour is shown in Fig. 2.4(b). Everything normalizes when $I > I_C$, because now one solution exists and the voltage varies linearly with the applied current. The I-V characteristic in this case is hysteric, because upon subsequent reduction in current, the junction response follows a different path evident when $I < I_C$ again as shown in Fig 2.4(c). This is due to the slow discharge of the large capacitance, and the arrangement behaves like an RC circuit.

$$\beta_C \sim 1$$

Lastly, the general case assumes $\beta_C \sim 1$ and therefore $\tau_{RC} = \tau_J$. This means that all the three branches in the junction model contribute to the overall response. From $I = 0$ to $I > I_C$, the response is similar to the case where $\beta_C \gg 1$ shown in Fig. 2.4(b). However, when current is gradually reduced from the voltage state (i.e. $I > I_C$), the response follows a new path determined by the current i_{min} , which is dependent on the value of β_C [1]. Refer to Fig. 2.4(d). The response is hysteric but comparatively much better than when $\beta_C \gg 1$.

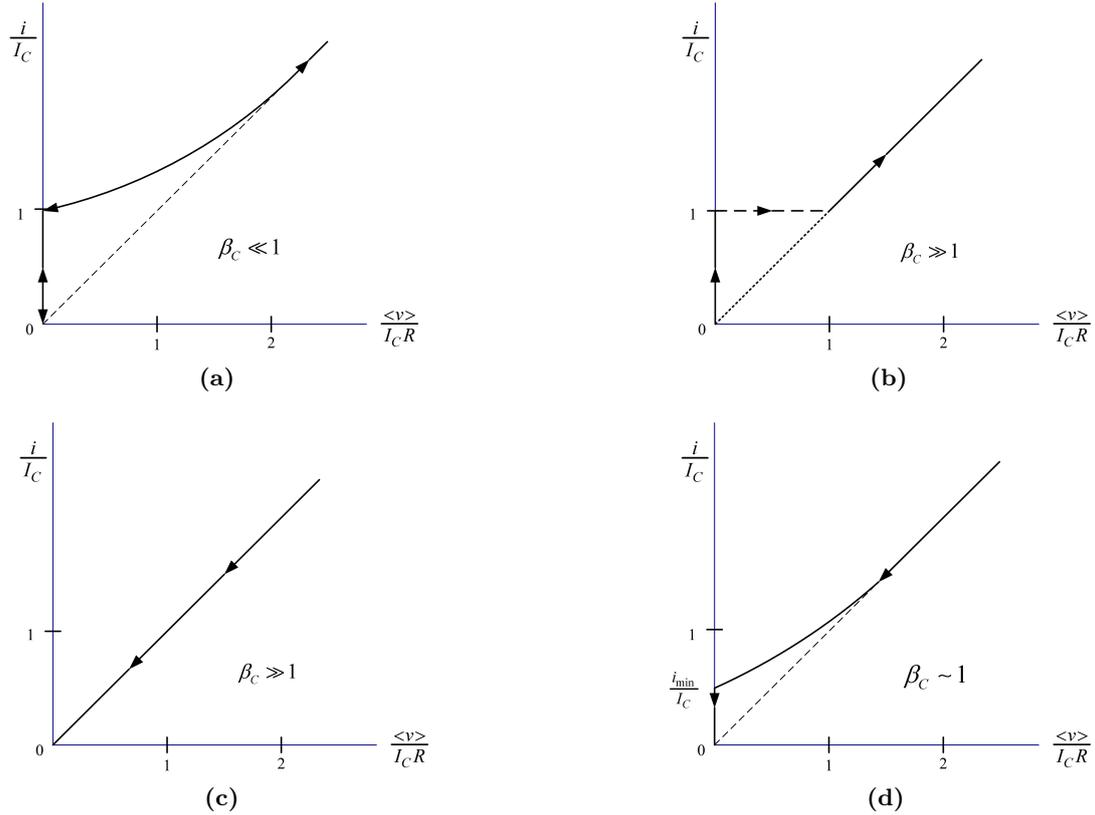


Figure 2.4: I-V Characteristics for a Josephson Junction with different values of β_C - Redrawn after [1]. (a) $\beta_C \ll 1$, (b) $\beta_C \gg 1$ with increasing current supply, (c) $\beta_C \gg 1$ with decreasing current supply and (d) $\beta_C \sim 1$.

2.3 Modelling the Josephson junction for SPICE simulation

As a fundamental building block of RSFQ circuits, the Josephson junction needs to have its behaviour and different parameters well known. Behaviour of electronic components can be obtained through experiments and simulations. The latter seems to be a better option in terms of cost and time. Simulations however, require that the element in question be well defined in the simulation package.

Several simulation packages like *WR-Spice* and *JSIM* [12], have the Josephson junction defined and quite usable. It was however noted that the junction behaviour does not vary with temperature, because it is assumed that the junction is already in superconductive state, therefore parameters remain unchanged throughout the simulation.

In order to carry out better simulations, the temperature aspect of the junction has to be brought into the picture. Several papers and books were consulted on the possible way of bringing temperature as an integral element in the Josephson junction circuits' simulation. The upcoming part of this discussion seeks to outline parameters of the junction and possible integration with temperature dependency aspects.

2.3.1 Josephson Junction Parameters

According to Yohannes et al [13], a number of parameters are required in the design and characterization of the Josephson junction. These parameters are usually realized through the fabrication process and are related to the junction's area. These parameters include the critical current (I_C), physical area of the junction (A), normal resistance (R_n), sub-gap resistance (R_{sg}), specific capacitance (C_s), and gap voltage (V_g). All these parameters are collectively known as primary parameters. Secondary parameters include the $I_C R_n$ product and the characteristic voltage, $V_m = I_C R_{sg}$.

The critical current is the super-current that flows through the Josephson junction before a voltage is developed across it. It defines the junction because it is derived directly from the area of the junction. The normal resistance and the sub-gap resistances represent two states through which the junction goes when it switches. The sub-gap resistance represents the tunnelling of normal electrons which were part of Cooper pairs. These electrons can only tunnel if there is enough excitation such as temperature. The sub-gap resistance disappears at a temperature of absolute zero, because the electrons are not free to tunnel. When the Josephson junction switches on, the sub-gap resistance disappears and the normal resistance appears across the junction, representing the tunnelling of normal electrons flowing due to the existing superconducting state. The normal resistance (R_n) represents the ON state of the junction. Further to this, the $I_C R_n$ product is a very important parameter in Superconductor Integrated Circuit (SIC) technology, because it is inversely proportional to the operating speed in single flux quantum (SFQ) devices [14]. The relationship can be approximated as [15].

$$t_{max} = \frac{3\Phi_0}{I_C R_n} \quad (2.8)$$

where t_{max} is the maximum delay. The $I_C R_n$ product calls for better fabrication techniques to increase its value in order to increase switching speeds for SICs. At the time of writing, new fabrication techniques are being developed to optimize the product. Typical products today, are pegged at around $2.5mV$. For the $20kA/cm^2$ Hypres niobium process the $I_C R_n$ is $2.2mV$ [16].

2.3.2 Temperature dependence of the Josephson Junction

Both R_{sg} and I_C are known to vary with temperature [1]. The former displays the behaviour of the junction before it switches on. Since the transition to superconductivity occurs at a specific temperature, T_C , it is worth noting that at other temperatures the resistance will have different values and the junction will behave differently. The transition from sub-gap to normal resistances occurs at a specific voltage, as shown in (2.3). The I-V characteristic of the Josephson junction with the transition shown in (2.3) is shown in Fig. 2.5.

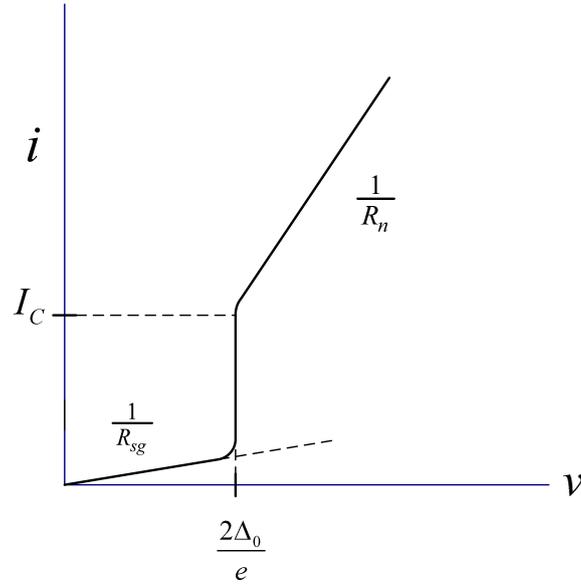


Figure 2.5: I-V curve of a the Josephson junction (RCSJ model) with $\beta_c \gg 1$, incorporating R_{sg} - after [1]

2.3.2.1 Variation of V_g with temperature

At a temperature other than absolute zero, the I-V characteristics show rounded shapes due to the presence of the sub-gap resistance [10]. The resistance R_n is temperature independent as its behaviour is purely ohmic. This indicates that the change in shape of the I-V characteristics is brought about by changes in the value of R_{sg} . In the absence of a well defined relationship between R_{sg} and temperature, we turn to other relationships which could be of great importance. Close to the critical temperature T_C , the gap voltage can be approximated by [10]

$$V_g \approx 1.74V_{g0}\sqrt{1 - \frac{T}{T_C}}. \quad (2.9)$$

where $V_{g0} = V_g(T = 0)$. It is further claimed that the expression is valid for a wide range of temperatures, which eventually makes it a good approximation.

2.3.2.2 Variation of I_C with temperature

The variation of the critical current is crucial, because if it is not properly checked, the switching characteristics of the Josephson junction would be affected rendering circuits unusable. The critical current variation with temperature in real tunnelling junctions can be expressed by [10].

$$I_C(T) = \frac{\pi\Delta(T)}{2eR_n} \tanh \frac{\Delta(T)}{2kT} \quad (2.10)$$

where $\Delta(T)$ is the temperature dependency of the gap voltage [17]. This equation

shows how temperature variation may affect the $I_C R_n$ product and eventually impact negatively on circuit performance.

2.4 Chapter Conclusion

The theory behind superconductivity as the benchmark for the Josephson junction has been presented. Basic parameters of the junction have been explained while paying much attention to their relevance and impact on junction response. An attempt has also been made to enlighten the temperature dependence of the junction. It has to be noted, however, that for low- T_C superconductors, the effect of temperature on junction operation is not crucial, as long as it does not result in instabilities that may bring about loss of superconductivity. Temperature variation become crucial for high- T_C superconductors because the increase in temperature brings about thermal noise.

Chapter 3

RSFQ Circuits

"Imagination is more important than knowledge." - Albert Einstein

RSFQ circuits offer an alternative to CMOS technology for certain applications. A decade ago, microprocessor integration increased and so did the clock speeds. The processors were quite fast and handled consumer requirements of the day quite well. However, increased performances demanded more power and therefore a lot of heat was produced by such devices. Improvements were made and clock speeds were reduced or kept constant while increasing the number of cores per chip. Other technologies like hyper threading and parallel processing were also incorporated to improve performance.

Semiconductors continue to serve the consumer needs quite well, but a threshold will soon be reached and semiconductors might not cope with an ever hungry consumer market for high speed and high processing applications. Fabrication techniques will soon reach a point where attempts to further increase integration will only increase production costs. RSFQ technology is projected to become the eventual partner (to form hybrid circuits) and successor of CMOS technology. Apart from being a challenger to the current technology, RSFQ in itself is a technology to adopt for the future. However RSFQ still suffers from low integration. This chapter discusses the fundamentals of RSFQ technology, progress made and the necessary elements that make the technology work.

3.1 Theoretical Background

RSFQ logic is a superconductor based digital electronics family. It was presented in 1991 by two Russian scientists K.K. Likharev and V.K Semenov [4]. The technology is based on the Josephson junction. In RSFQ digital circuits, a logic HIGH (1) and logic LOW (0) are represented by the presence and absence of a flux quantum (Φ_0), respectively. The Josephson junction is the active component in RSFQ and that comes

with advantages. The Josephson junction is a low power device, it dissipates very little power when it switches on. The voltage is quite small which makes handling, propagation and storage comparatively effortless. Specifically the following are the good attributes of the Josephson junction in RSFQ:

- In RSFQ circuits, the voltages are small and equivalent to approximately $3mV$ [4] (gap voltage for Niobium Josephson junctions). Such a small voltage means less power to switch and propagate.
- The Josephson junction is a high speed switching device, such that switching delays of $1.5ps$ [4] have been reported. This ensures high speeds propagation in RSFQ circuits.
- Josephson junction fabrication technologies are very similar to the those used in the semiconductor industry, therefore there is no need to have a complete overhaul in the fabrication facilities [4].

The two terminal nature of the Josephson junction means more Josephson junctions are required than transistors for a circuit of equal functionality [18].

3.1.1 Josephson Junction Switching

As indicated in Chapter 2, the Josephson junction switches when the applied current to the junction exceeds its critical current ($I > I_C$). The aftermath is that a voltage equivalent to the flux quantum develops across the junction.

$$\int v(t)dt = \Phi_0 = \frac{h}{2e} \simeq 2.07mV/ps \quad (3.1)$$

The junction switching is also characterized by a junction phase leap of 2π [19]. Taking some insight from a setup where a junction is in a superconducting ring (Fig. 3.1(a)), the phase change in a junction can be shown as

$$\phi = 2\pi \frac{\Phi}{\Phi_0}. \quad (3.2)$$

In this case Faraday's relation has been used, where $V = \dot{\Phi}$. It is therefore natural to analyze Josephson circuits using magnetic flux. In (3.2), if the applied flux Φ becomes equal to the flux quantum, then it signifies the switching of the junction and $\phi = 2\pi$. Fig. 3.1(b) illustrates the switching of the junction, coupled with the phase leap.

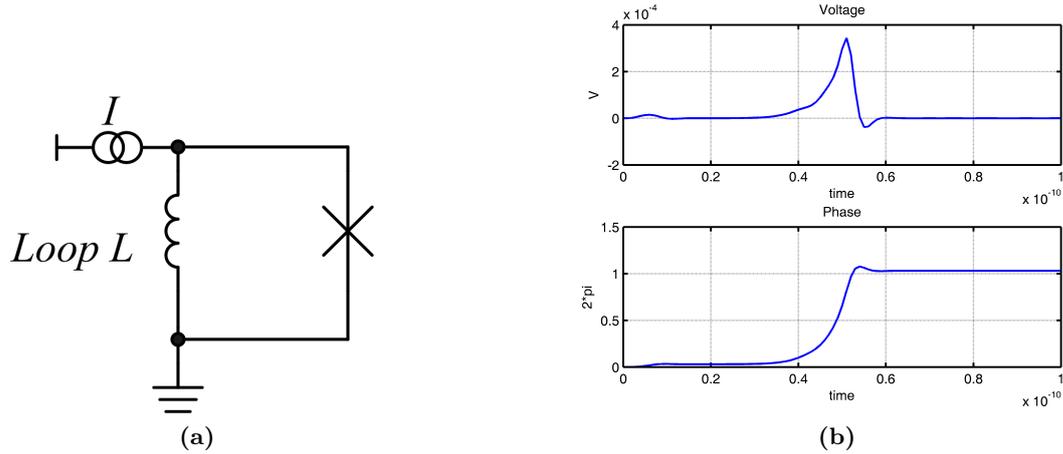


Figure 3.1: A Josephson junction in a superconducting loop, (a) and an illustration of the flux quantum and phase change, (b).

3.1.2 Josephson Junction Damping

In RSFQ circuits, an effort is made to always eliminate oscillations in Josephson junctions. Junction switching often results in oscillations which are dependent on the junction capacitance. The requirement is that $\beta_C = 1$, because at this value the junction is critically damped and little or no oscillations occur. The junction capacitance and resistance are part of the junction and cannot be changed to achieve $\beta_C = 1$. However, a resistor (R_s) is normally added in shunt with the junction to modify the behaviour and achieve critical damping. (2.7) is therefore modified as

$$\beta_C = \frac{2\pi I_C R_{eff}^2 C}{\Phi_0} \quad (3.3)$$

where $R_{eff}^{-1} = R_n^{-1} + R_s^{-1}$. The value of R_s depends on the current density of the junction (J_C). This is the case with the two current densities considered in this thesis, $1\text{ kA}/\text{cm}^2$ and $4.5\text{ kA}/\text{cm}^2$. The need to have R_s reduces with increased process fabrication current density, because the capacitance becomes smaller and so does R_n . The bias resistor takes much of the area occupied by a junction on a chip.

3.2 RSFQ Circuit Elements

RSFQ circuits rely on some discrete components which, when connected in a specific manner, achieve a circuit functionality.

3.2.1 Discrete Elements

RSFQ circuits are made up of three discrete elements, the Josephson junction which is the active component, inductance for the formation of superconducting loops, and regulation and distribution of electrical current. Bias currents are the third element for RSFQ circuits, which lift the current in Josephson junctions to enable switching with incoming pulses.

3.2.2 Functional Elements

Three functional elements exist for RSFQ circuits. Those that are concerned with the transmission and storage of flux quanta and decision making elements. A description of these three elements follows.

3.2.2.1 Transmission of a Flux Quantum

The switching of a Josephson junction produces a flux quantum which is the basic signal in RSFQ circuits. Elements exist whose main purpose is to propagate a fluxon over a number of stages with no losses. Switching power is obtained from the bias current sources. Such elements are made up of Josephson junctions and small inductances. The small loop inductances ensure that no flux trapping occurs. Fig. 3.2 illustrates such an element.

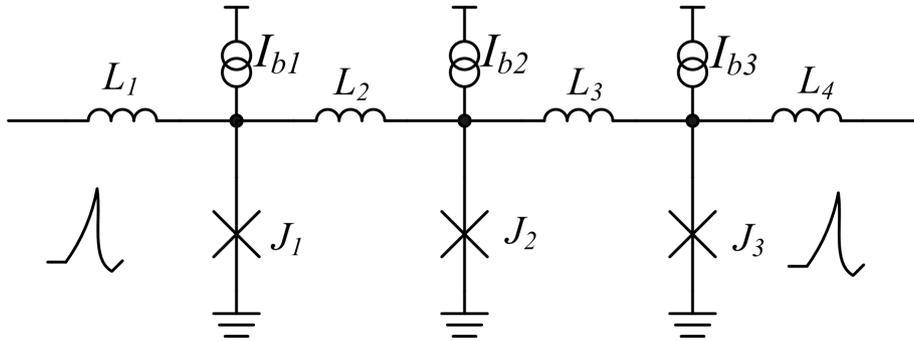


Figure 3.2: Transmission element for a flux quantum

A flux quantum (shown as a pulse in Fig. 3.2) comes in through inductance L_1 and together with the bias I_{b1} induces an 2π leap in junction J_1 , then J_2 , followed by J_3 . This subsequent switching of the three junctions reproduces the input flux quantum at the output. This element relies heavily on the inductances being small, so that no flux gets trapped in a loop ($L = \frac{\Phi_0}{I}$). Amplification of the the flux can occur if $I_{CJ1} < I_{CJ2} < I_{CJ3}$ and the bias current were to follow that same order [4]. A practical circuit that does this function is called a Josephson Transmission Line (JTL) [20]. Transmission of the flux quantum can occur in both directions, but due to Meissner's theory once,

J_1 switches it achieves a resistive state and can not switch until the flux quantum is cleared to J_3 by J_2 . Each junction is biased at $\approx 0.7I_C$ and for the inductance to be non-storing the following criterion , $LI_C \sim 0.5\Phi_0$, has to be satisfied [19].

3.2.2.2 Storage of a Flux Quantum

A need arises in specific RSFQ circuits to store and delay a flux quantum for a long time. Such circuits are characterized by large loop inductances, so that typically $LI_C \sim 1.25\Phi_0$ [4]. Consider Fig. 3.3 .

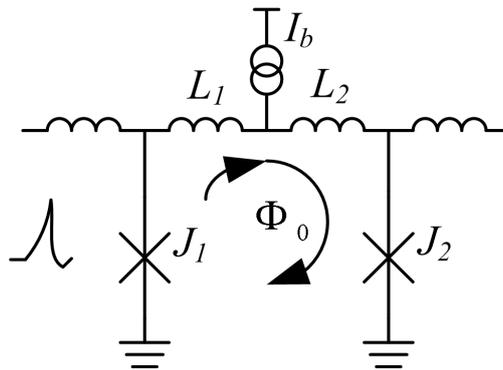


Figure 3.3: A flux storing element

An incoming pulse propagates into the loop $J_1 - L_1 - L_2 - J_2$ through the switching of J_1 . The flux quantum remains in the loop because $L = L_1 + L_2$ is quite large. The current due to the trapped flux quantum, together with the bias current, are not enough to trigger a 2π leap in J_2 . The trapped flux can only be removed if another pulse further biases and triggers J_2 .

3.2.2.3 RSFQ Decision Element

A decision element is thus called, because it offers control in RSFQ circuits. It enables clocking to be incorporated in most RSFQ circuits. Such an element is often achieved by a Josephson junction comparator [4, 21]. Fig. 3.4 shows a simplified comparator that achieves this functionality.

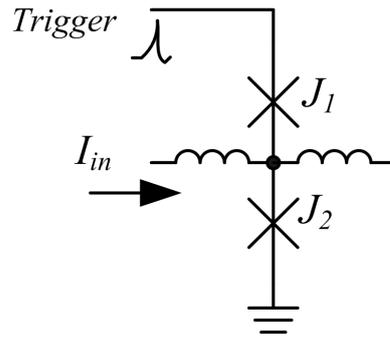


Figure 3.4: A Josephson Junction Comparator

Either J_1 or J_2 will switch depending on the availability of the input signal I_{in} . The input, I_{in} , biases J_2 and an incoming trigger signal will switch J_2 and not J_1 . Otherwise, if there was no input signal, J_1 will switch and the output will remain unchanged. The circuit is ideal to read out and liberate a stored pulse, such as the one that could be trapped in a circuit shown in Fig. 3.3.

3.3 RSFQ Basic Clocking

RSFQ circuits can be divided into Asynchronous and Synchronous types. Asynchronous circuits produce outputs almost immediately after inputs are applied. They do not possess any memory. Synchronous circuits, on the other hand, do have some memory and they require clocking to produce an output that is based on the memory state and the inputs.

It is shown in Chapter 4 that asynchronous circuits include the JTL, pulse splitter, merger, passive transmission line (PTL) drivers and receivers, and the interface cells of the DC-SFQ and SFQ-DC converters. All the flip-flops and gates fall under the synchronous category, and these include DFF, NOT, OR, NOR, AND, NAND, XOR and XNOR gates.

Several attempts have been made to improve the clocking mechanisms for RSFQ synchronous circuits. Clocking at cell level is not a big problem. The main target in cell design has to be one clock per cell. Clocking mechanisms become crucial in big circuits where the clock signal needs to be available at specific times (timing). A clock signal is only meaningful if a specific data input pulse is available before the clock signal. The output is generated depending on the circuit functionality. Thus, any clocking scheme that is crafted has to take this into consideration. Two clocking schemes are presented next and they both belong to *Line clocking: Counter flow* and *Concurrent flow* [4, 22].

3.3.1 Counter-flow clocking

In counter-flow, the clock propagates in the opposite direction to the data flow. For this type of clocking to work some condition needs to be met.

$$\tau, \tau_C > \delta \quad (3.4)$$

where the cell delay is denoted as δ and the clock period τ and the delay between cells as τ_C . Counter-flow clocking is illustrated in Fig 3.5.

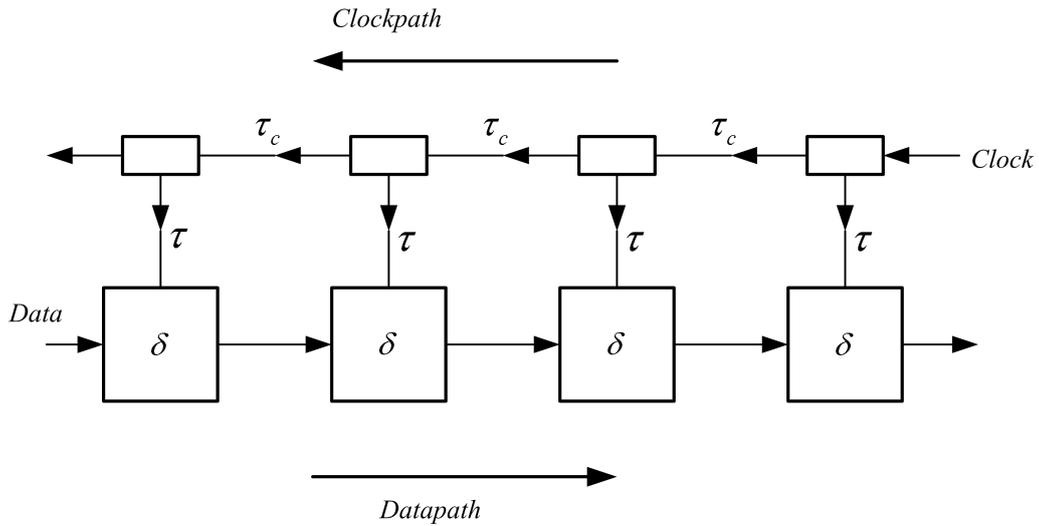


Figure 3.5: Counter-flow clocking illustration

Data and clock flow are in the directions shown. Using a shift register analogy, the output stage gets the clock after 3τ . In counter-flow, clock skew (the difference between the arrival time of the clock at clock inputs to blocks at the beginning and end of the data path) for a system that has n blocks, is positive (3.5). Counter-flow has the advantage that it helps to clear the blocks before new data is loaded and shifted. In addition, counter-flow clocking enables RSFQ circuits to be clocked at much higher frequencies, thereby maximizing their operating speeds [23].

$$Skew = t_1 - t_n \quad (3.5)$$

For a system that has n blocks.

3.3.2 Concurrent Clocking

In concurrent clocking, the clock path is the same as the data path. The condition in (3.4) has to be satisfied for the clocking to work, and the blocks need to be empty before applying a clock [22]. Fig. 6 illustrates concurrent clocking.

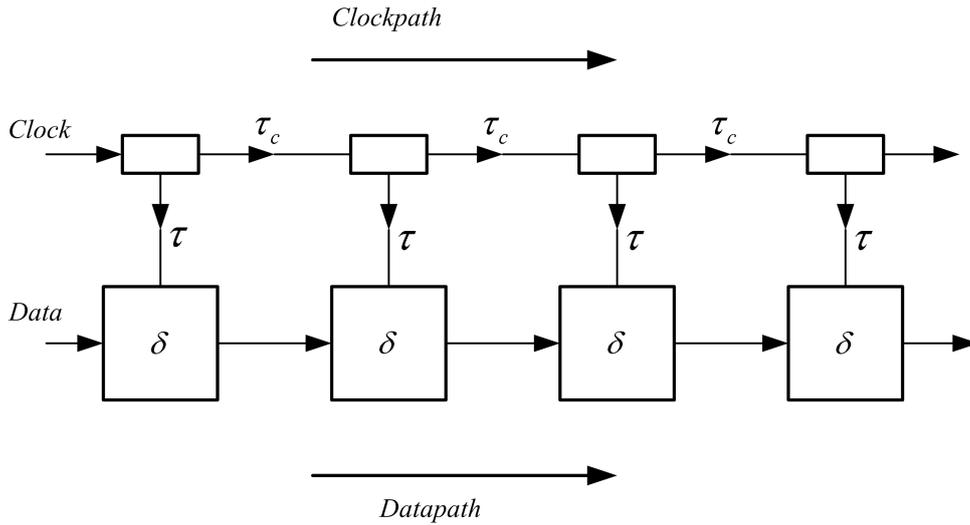


Figure 3.6: Concurrent clocking illustration

In both counter-flow and concurrent clocking, it is a well observed fact that the slowest block affects the clock speed. This element is crucial in cell design to make sure there is minimum delay imposed by a single cell. It is a good design principle that only one clock input is provided per cell to minimize cell delays.

In RSFQ circuits, the clock is a series of quantum flux pulses which are equal in power and width [24]. The clocking schemes are quite basic and some improvements have been made and presented. However, counter-flow and concurrent clocking are used in further testing of the cells in the library being presented.

3.4 Fabrication Processes

The Cells presented in the thesis are designed specifically for the IPHT's $1kA/cm^2$ (IPHT) and *Hypres*' $4.5kA/cm^2$ (Hypres) fabrication processes. The fabrication processes were chosen because of their simplicity and clear design rules, that are readily available, and that the fabrication facilities are open to commercial customers. IPHT and Hypres are both Niobium fabrication processes. These two processes are hereby described.

The two processes are similar with main differences appearing on the Josephson junctions areas and parameter values, such as inductance and sheet resistance. Both of these processes have design rules that define metal layers, insulation layers, vias specifying clearly their minimum sizes, minimum allowable spacing between layers of the same type, as well as different types. Design rules help the designer to build layouts that have a higher chance of being fabricated with minimum errors. The design rules of these processes are outlined in Appendices C and D.

Josephson junctions are defined between two niobium layers (denoted as M1 and M2) and an insulation layer of aluminium oxide. The junction therefore becomes a $Nb/AlO_3/Nb$ trilayer. In the Hypres process the niobium trilayer is deposited onto an entire wafer and junction areas are defined using a $1x$ lithography and etching [25]. IPHT adopts a similar process. Table 3. 1 summarizes the various layers and their functions, for the two processes. IPHT has only three niobium, layers where M2 acts as the wiring layer, while Hypres, apart from M2 has an additional wiring layer in M3.

| Parameter/Layer | IPHT | Hypres |
|---------------------------------------|----------------|-----------------|
| Josephson Junction Counter-electrode | I1C | I1C |
| Niobium Layers | M0, M1, and M2 | M0,M1,M2 and M3 |
| Resistor Layer (Molybdenum) | R1 | R2 |
| Contact pads on Chips (Titanium/Gold) | R2 | R3 |
| Contact vias | I0, I1 and I2 | I0, I1 and I2 |
| Specific Capacitance ($pF/\mu m^2$) | 0.05 | 0.059 |
| $I_C R_n$ Product | $256\mu V$ | $1.96mV$ |

Table 3.1: A comparison of the IPHT and Hypres processes

The design rules in Appendices C and D have more information, but of special mention is the parameter estimation values for inductance and sheet resistance for the two processes. Table 3.2 gives a summary of these estimations, which were obtained after examining several samples [13, 25, 26]. The increase in sheet resistance/square with increase in fabrication density means less space is occupied by bias resistors, thereby leaving more space for more Josephson junctions.

| Parameter | IPHT | Hypres |
|--|------------|---------|
| Sheet Resistance/Sq (Ω/\square) | 1 | 2.1 |
| Inductance/Sq (pH/\square) | M1 0.52 | M1 0.47 |
| | M2 0.81 | M2 0.71 |
| | M2-M1 0.64 | M3 1.36 |

Table 3.2: Parametric estimates for IPHT and Hypres

The inductance values/square are all with respect to the M0 layer. The resistor layers are either done in R1 (IPHT) or R2 (Hypres) with vias (in I1B) to the M2 layer.

3.4.1 Moats

Josephson junctions are very sensitive devices and any flux trapped in them may cause circuits to malfunction [27, 28]. To reduce chances of flux trapping in junctions, moats are created in the ground plane, using specific layers provided in the design rules. The

Hypres process provides creation of moats, especially around junctions in M0 layer. Layer M0N is used to create moats in cell layouts made for the IPHT process.

Published results show that the creation of moats does not significantly affect the inductance of nearby conductors [27]. However, caution has to be exercised to create moats at specific clearance. M0 and M0N layers are not allowed to cross under any transmission line layers (M1, M2, M3) as this will interfere with current paths and hence affect inductance values. This is the reason to have moats confined to open spaces in cells. It is an observed fact that small (minimum) thickness moats around junctions are more efficient at trapping flux than thick block ones. All the cells presented in this thesis have moats created at strategic positions in cells.

3.5 Developments in RSFQ

From the time it was reported in 1991, RSFQ has seen slow development due to a number of factors (see Section 1.1). Nonetheless, several developments can be pointed out, like RSFQ processors, memory chips, data converters such as analogue to digital converters (ADCs), and digital to analogue converters (DAC) and many other circuits [6, 21]. Being a new technology with commercial potential, information sharing is still a problem. RSFQ circuits, just like CMOS rely on cells to achieve connectivity of functional blocks to create complex circuits. Cell libraries are proprietary and developments in this area are not shared much. This leaves institutions to develop their own cell libraries, hence the work presented in this thesis.

3.6 Chapter Conclusion

The basics behind RSFQ technology has been presented, with much attention given to RSFQ theory and its fundamental building blocks. The chapter also gave an insight into the clocking regimes in use and the fabrication technologies used in the development of the cells presented. Some of the elements presented in this chapter are explained in detail in the upcoming chapters. Chapter 4 presents that main focus of this project which is the standard RSFQ cell development. All the cells are presented in that chapter.

Chapter 4

RSFQ Cells

“Imagination is not only the uniquely human capacity to envision that which is not, and, therefore, the foundation of all invention and innovation. In its arguably most transformative and revelatory capacity, it is the power that enables us to empathize with humans whose experiences we have never shared.”

J.K. Rowling

The chapter presents the cells developed while highlighting the procedures and tools employed at every stage. Krasniewski defines a RSFQ cell as a circuit which is repeatedly used as a component for large circuits [29]. Such small circuits are presented in this chapter as items in the just developed RSFQ cell library.

RSFQ cell libraries are proprietary, largely because they often address the design culture and tenets of a specific organization or research entity. IPHT and SUNY have cell libraries available on the web [30, 31]. These cell libraries offered a design benchmark to most of the cells presented in this work. Cells designed and fabricated for different libraries exist, but only few are presented to the engineering fraternity. Meazawa *et al* presented two cell libraries for the National Institute of Advanced Industrial Science and Technology (AIST) for $1.6kA/cm^2$ and $10kA/cm^2$ processes [32, 33]. No circuit and parameter details of the fabricated cells are given which confirms the proprietary nature of cell libraries. The work presented by Meazawa offers a different dimension in cell design and some of the results obtained in this work are compared with the results presented by the authors.

Cells presented in this work are specifically designed for the IPHT's $1kA/cm^2$ RSFQ1D and the Hypres $4.5kA/cm^2$ processes. Design rules for these processes were strictly followed during layout design.

This chapter presents the various steps followed in RSFQ cell development. In addition all the cells, adapted and designed are presented. The presentation format is in such a way that each cell has an optimized circuit used in simulation, simulation results,

layouts for the two processes and necessary description, operation and any necessary documentation. Where required, finite state machine (FSM) transition diagrams (i.e. Moore and Mealey), are used to further describe cell operation.

4.1 Stages in Cell Development

4.1.1 Circuit Simulation Stage

Electrical circuit simulation is the first stage in cell development. Simulations are done in *SPICE* or *SPICE* based CAD software such as *Niopulse* [34]. Inductance values, Josephson junction critical currents, and bias currents are carefully calculated before simulation to achieve proper circuit functionality. Electrical simulations are done to determine if the circuit produces the right waveforms as specified at expected intervals. At this stage parameters that produce the right results are known and used in the subsequent cell development stages. Once the circuit produces the right results, initial circuit operating margins are obtained. If the margins are narrow then optimization can be done at this stage to obtain acceptable margins. Optimization enables the designer to arrive at the best possible parameter values that produce the best margins. This process in return gives the circuit a high probability of working after fabrication taking into account that fabrication, processes can introduce variations in some parameters (tolerances) [2].

Niopulse was the CAD software of choice for circuit simulations in this work. *Niopulse* runs spice engines like JSIM, *WR_Spice* and *Spice_3F5*. Apart from the user friendly graphical user interface (GUI), *Niopulse* generates a *SPICE* netlist for the circuit being simulated. The netlist can be exported to any computer running the Spice engine in question. In addition, *Niopulse* offers many functions, such as margin analysis, optimization tools and layout development, which are still being perfected by the developers. Waveforms generated can be exported as MAT files for further analysis in MATLAB.

4.1.1.1 Josephson Junction Models

Two Josephson junction models were used during simulations. These two reflect the two fabrication processes employed in this work: The IPHTs $1kA/cm^2$ and Hypres $4.5kA/cm^2$. To achieve critical damping - a requirement in RSFQ circuits ($\beta \sim 1$), different values of shunt resistors are used (3.3). The models used to reflect the variations are shown in Table 4.1. The IPHT employs a simplified model of the Josephson junctions in circuit simulations.

| Name | Parameter | Value (IPHT) | Value (Hypres) |
|-------|----------------------------|--------------------------------|-------------------------------|
| icrit | Junction critical current | $1.0mA$ (Area = $100\mu m^2$) | $1.0mA$ (Area = $22\mu m^2$) |
| cap | Junction capacitance | $5.0pF$ | $1.3pF$ |
| rn | Normal resistance | 90Ω | 1.92Ω |
| r0 | Subgap resistance | – | 13Ω |
| vg | Gap voltage | – | $2.5mV$ |
| delv | Gap voltage spread | – | $0.1mV$ |
| cct | Critical current model | – | 1 |
| rtype | Quasiparticle branch model | 0 | 1 |

Table 4.1: IPHT and Hypres Josephson junction Models used in *Niopulse* circuit simulations

Parameters such as *cct*, *rn* and *cap* are scaled with the actual Josephson junction area which can be defined separately. The much smaller capacitance for the Hypres model is attributed to the reduced junction area which results in junctions that switch faster. The quasi-particle branch models (*rtype* 0-4) were defined by Whiteley Research [35] and serve to extend the RSJ model of the Josephson junction. *Rtype* 0 is the unshunted approximate model and much smaller resistors are required for shunting although no direct relationship exists between *Rtype* and R_s values. On the other hand, *Rtype* 1 defines a standard piecewise model which corresponds to the response depicted in Fig. 2.5. Shunting resistor values are almost double the values used in IPHTs *Rtype* 0. Larger values of R_s signify the reduced requirement of shunting in Josephson junctions as J_c increases.

Once circuit simulation results are satisfactory and initial optimization done, cell layout can be done. Cell layout is done once satisfactory circuit simulation results and acceptable optimization results have been obtained. The cell layout stage is discussed next.

4.1.2 Cell Layout Stage

Each cell has to be laid out properly and verified before fabrication. Layout design defines the metal and insulation layers, their dimensions and hence parameter values, like inductance and sheet resistance. Several tools exist that are used for cell layouts. In this work *LASI* (*L*ayout *S*ystem for *I*ndividuals) [36] and *Niopulse* were used. *LASI* is widely used and is a manual based tool. *LASI*, however, lacks closed-loop design mechanisms (i.e. *no design rule checker - DRC - and no layout versus schematic verification* [2]) and designs have to be verified manually. *Niopulse*, on the other hand promises to be ideal as it has a closed loop design mechanism, but it is still under development. All the cell layouts presented in this work were laid out in *LASI*.

4.1.2.1 Additional Guidelines Used During Cell Layout

Additional rules and guidelines on cell dimensions are used. The main aim is to effectively use chip, space thereby creating space for more cells per chip and also to incorporate some form of uniformity in all the cells. Table 4.2 presents the dimensions used for the IPHT and Hypres cells. These are not standard dimension and other organizations may have their own.

| Type of Cell | Dimensions (μm) |
|--------------|------------------------|
| Hypres | 100×100 |
| | 200×100 |
| | 200×200 |
| IPHT | 150×150 |
| | 300×150 |
| | 300×300 |

Table 4.2: Cell dimensions used for this library

To ensure equal current distribution at contacts between cells, standardized width of contacts at strategic points are used. For the IPHT process the contact width is $10\mu m$ positioned midway at $75\mu m$ for a 150×150 cell. With the Hypres process, a width of $7\mu m$ and a midway positioning at $50\mu m$ for 100×100 cell is used. DC bias connections are located but not restricted to upper corners to ensure uniformity and to allow adjacent cells to use a common DC bias connections thereby improving space usage. Fig. 4.1 illustrates the cell dimensioning.

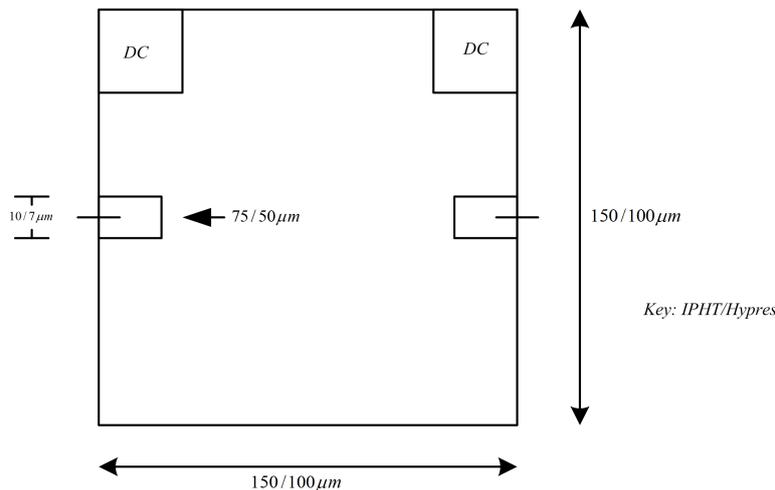


Figure 4.1: Typical cell dimensions and interface positions

A stage that is inherently part of layout is parameter extraction. Such parameters include inductance, bias resistors and Josephson junction critical currents as a function of area.

4.1.3 Inductance Extraction

Inductance is not a straight forward parameter to estimate and extract [37] [27]. Inductance depends on the penetration depth of a specific material and its thickness as well as the loop area. That is the reason why the inductance/square values in Table 3.2 are different for different superconductor layers. Margin analysis results indicate that inductance, varied within tolerance, has no significant effect on the overall margins. But this does not mean inductance variations do not affect circuit operation. Inductance drifts can affect bias currents, thereby affecting junction switching. In addition, leakage currents between cells can be observed when inaccurate inductance values are included [38]. These leakage currents can affect the junctions at the terminals of cells, thereby contributing to circuit malfunction. Large inductance at undesired points in a circuit may result in unnecessary flux trapping, which has a high potential of causing the circuit to malfunction.

Estimated per square values outlined in design rules are only used at initial layout design level. Inductance extraction is crucial, because Josephson junction and contact vias contribute to the total inductance in a circuit. Besides, connected blocks forming corners and T-sections on the layout can not be easily estimated or calculated. Inductance also depends on the distribution of electrical currents in the conductor [38]. This can not be taken into account accurately during manual estimation of inductance. Analytical methods, such as the ones proposed by Chang [37], fail to account for intricate structures like vias, junctions and T-sections.

Inductance extraction is a resource intensive process and requires special software running inductance calculation algorithms, such as *FastHenry*. *InductEx* [39] is a program that uses a superconductive version of *FastHenry* to calculate the inductance of specified superconducting structures on a chip. It works by dividing a complex structure into 3-dimensional (3D) models. It then generates a file to be used by *FastHenry* in calculating the inductance. Finally, *InductEx* solves a multi-port network of self and mutual inductance from the *FastHenry* outputs.

Other tools for estimating inductance exist. *Slime* [40] and *Induct* [41] are 2D analytical tools that are based on Chang's algorithms [37]. These tools are quite effective at estimating inductance of simple microstrip lines [2]. 2D tools are quite fast and not as demanding on computing resources as the 3D tools, such as *FastHenry*, which uses numerical methods to estimate inductance of complex structures. The advantage with 3D tools lies in their effectiveness and accuracy in estimating inductance.

4.1.3.1 Example: Inductance Extraction of a Josephson Transmission Line (JTL)

The extraction of inductance begins with the removal of necessary layers and junctions. Fig 4.2 shows a JTL (*Fig 4.8*) with other layers removed. Only the layers necessary in

the extraction process remain on the layout. Josephson junctions are replaced by M1 and M2 layers with VIAs in I1B, covering the effective junction areas and any contacts between M1 and M2. The effective paths from the Josephson junctions to the ground plane create parasitic inductance. There is nothing much a designer can do about them, apart from analyzing their effects on the circuit operating margins, and compensating accordingly. A common ground plane is used as a reference, although a *method of images* [38], which does not use the ground plane, can be used.



Figure 4.2: A JTL with all other layers removed

An inductance schematic circuit is then developed from the stripped layout. Fig. 4.3 shows a circuit from which the Spice file is developed. The stripped layout is then converted to the industrial format, Graphic Database System (GDS). *Inductex* then uses the GDS and the Spice file to map out structures on the layout. It then generates an input file which has the necessary segmentation that form a 3D image for FastHenry to use in the iterative estimation of inductance.

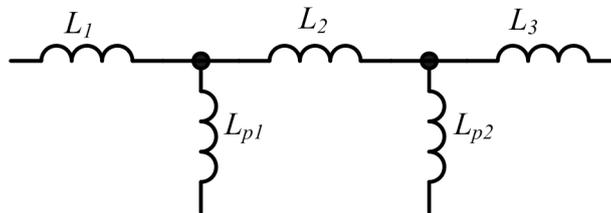


Figure 4.3: Inductance schematic derived from Fig. 4.2

A 3-D model generated by *InductEx* for the extraction of JTL inductance is shown in Fig. 4.4. Table 4.3 shows the inductance extraction results for a JTL. These results were obtained after a number of adjustments on the layout to make sure that the inductance values were within the margin $\pm 5\%$ or within any acceptable range. L_{p1} and L_{p2} are parasitic inductance at the two Josephson junctions. All values are in pH.

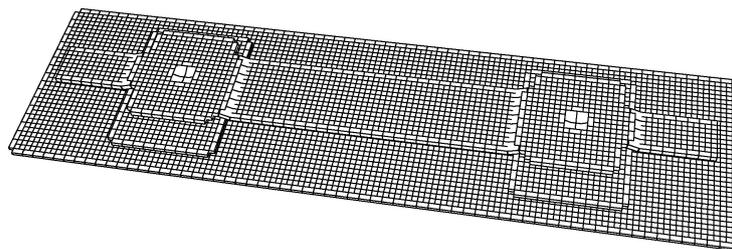


Figure 4.4: 3D Inductance extraction model generated by *Inductex* for a JTL

| Inductor | Design | Extracted | AbsDiff | PerceDiff |
|----------|--------|-----------|---------|-----------|
| L1 | 2.0 | 2.0922 | +0.0922 | +4.61 |
| L2 | 4.0 | 4.1526 | +0.1526 | +3.82 |
| L3 | 2.0 | 2.0923 | +0.0011 | +4.61 |
| Lp1 | 0.3 | 0.2989 | +0.0011 | -0.36 |
| Lp2 | 0.3 | 0.2982 | +0.0011 | -0.36 |

Table 4.3: Inductance Extraction results by *Inductex*

The inductance values, like the ones shown in Table 4.3, are then used for further circuit simulation. If the results are unsatisfactory, then the layout can be modified and further extraction done.

4.1.4 Fabrication and On-Chip Testing

Carefully designed cells, with all parameters extracted or estimated and design rule compliance verified manually, are sent for fabrication. The fabrication of these cells is done by private institutions - IPHT and Hypres - and the fabrication details are therefore not presented here. The whole process of cell development is illustrated in Fig. 4.5.

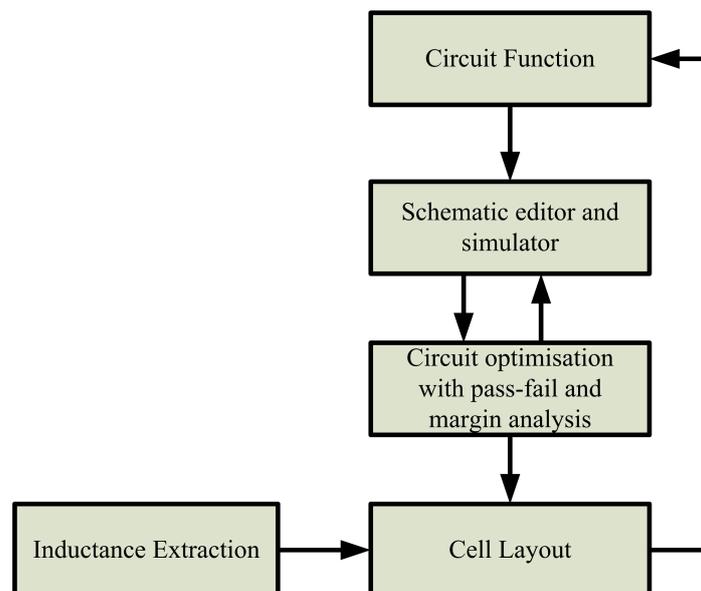


Figure 4.5: Cell development process flow diagram, after [2]

To verify if the cells work in a practical setup after fabrication, they have to be tested on-chip in the laboratory. Chapter 5 describes in detail the on-chip testing and presents the results obtained.

4.2 Cells in the Library

Cells in the library are hereby presented. Each cell has general operational description based on the circuit simulation schematic, operational waveforms and layouts for both IPHT and Hypres processes. Slight parameter variations between the two types (based on the fabrication process) of cells are presented as required. Cells presented include the JTL, splitter, confluence buffer, DFF, TFF, NOT, AND, OR, NAND, NOR, XOR, XNOR, DC-SFQ, SFQ-DC, PTL driver and PTL receiver.

4.2.1 Josephson Transmission Line - JTL

The JTL, shown Fig. 4.6, is used in RSFQ circuits mainly to connect cells over a short distance. It introduces a small, but noticeable delay ($\sim 5ps$) between cells. However, a JTL offers the much needed matching between cells and prevents loading. A JTL can also be used to boost output current of a cell, provided the output junction is larger than the input (i.e $I_{CJ2} > I_{CJ1}$).

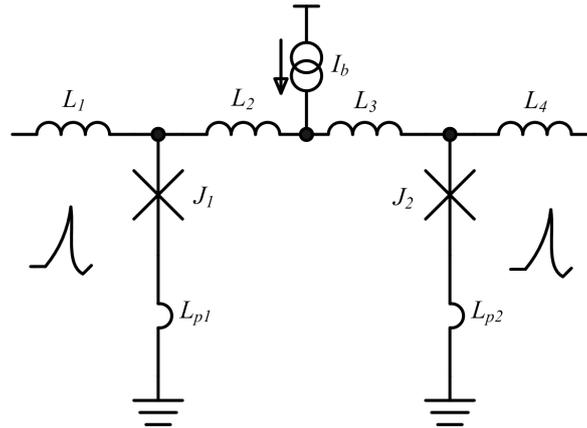


Figure 4.6: The JTL with all parasitics included

Extracted Parameters:

IPHT: $J_1 = J_2 = 250\mu A$, $L_1 = 2.08pH$, $L_2 = L_3 = 2.01pH$, $L_4 = 2.08pH$ and $L_{p1} = L_{p2} = 290fH$. Bias Current $I_b = 351.4\mu A$

Hypres: $J_1 = J_2 = 250\mu A$, $L_1 = 1.94pH$, $L_2 = L_3 = L_4 = 1.93pH$ and $L_{p1} = L_{p2} = 131fH$. Bias Current $I_b = 360.1\mu A$

A JTL is fundamentally made up of two Josephson junctions, inductors and a bias source, as shown in Fig. 4.6. The bias current I_b creates an $\sim 0.7I_C$ bias in both J_1 and J_2 . This causes J_1 to switch on easily when a flux quantum is made available at the input. The flux is then available in the loop $J_1 - L_2 - L_3 - J_2$. Due to the small inductance, J_2 is instantaneously triggered and switches to the voltage state. The flux quantum is then effectively transferred to the output. Because the system works on threshold, input does not have to be a full flux quantum. This being the case, a JTL can be used to reconstruct and recover weak signals. Spice simulation results for the JTL are shown in Fig. 4.7.

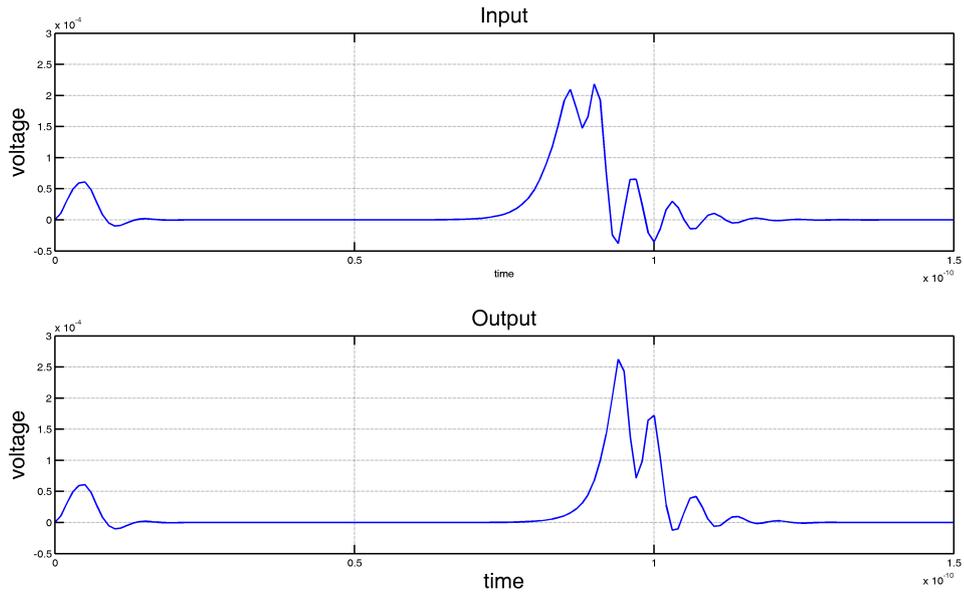


Figure 4.7: JTL waveforms generated in Spice with *Niopulse*

Layouts for the JTL, done in LASI, are shown in Figure 4.8 and Fig. 4.9 for the IPHT and Hypres processes, respectively. The layouts are presented with a key indicating all the layers used. The layer names used are according to design rules. Different colour schemes for layers are used in the two processes.

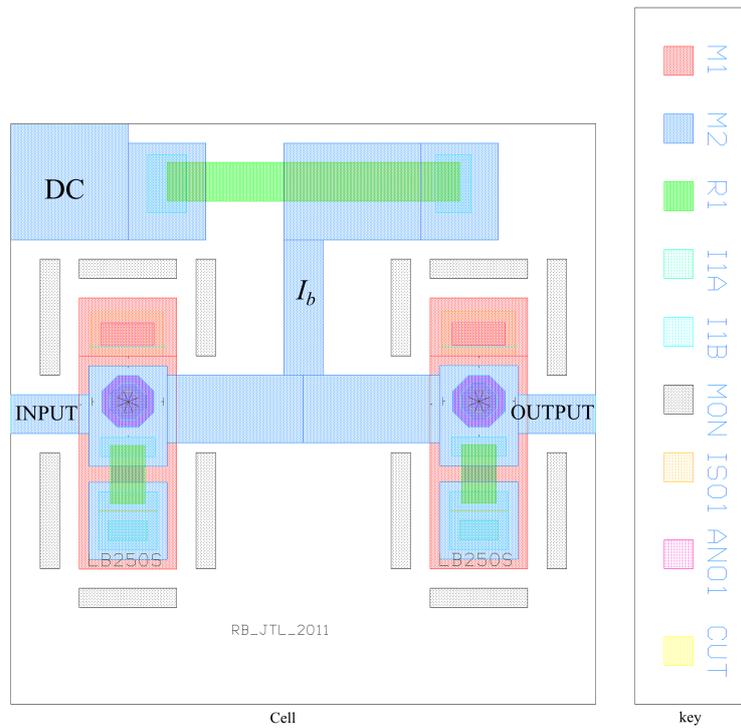


Figure 4.8: JTL Cell for IPHT - Laid out on a $150 \times 150 \mu\text{m}$ space

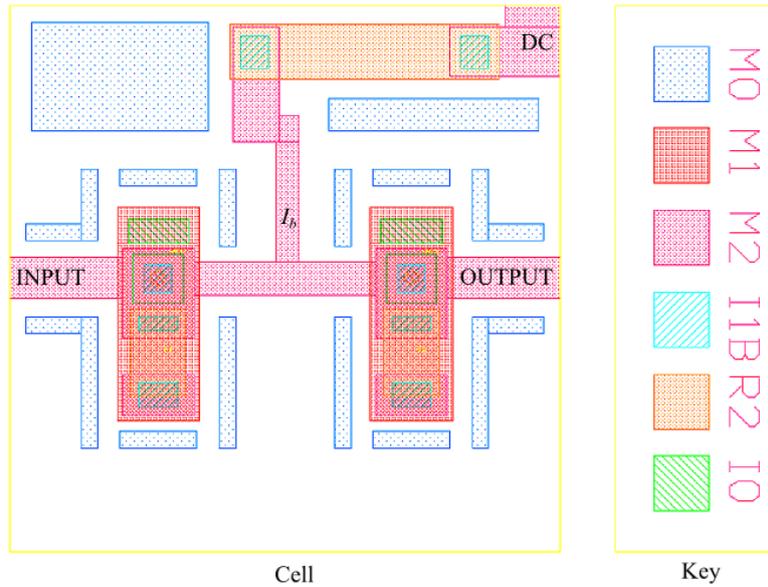
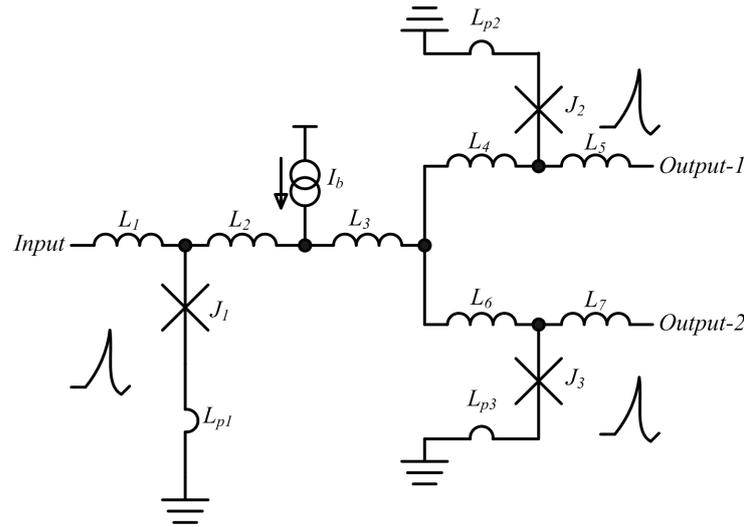


Figure 4.9: JTL Cell for Hypres - Laid out on a $100 \times 100 \mu\text{m}$ space

The two layouts are the same in functionality. The only difference is on the layout space used. The DC line may be put on either of the two top corners. As a standard, moats are used to protect the Josephson junctions from accidental trapped flux, see Section 3.4.1.

4.2.2 Splitter

RSFQ circuits have a maximum fan-out of one. It is required in some circuit designs to mitigate this limitation to feed an output to a number of circuits. A splitter is a circuit that reproduces an input pulse through its two output drivers, thereby increasing the fan-out to two. For this arrangement to work, it requires that the critical current of the primary driver junction to be larger than the output junctions by a factor of $\sim \sqrt{2}$ [4]. This is done to ensure that there is enough current to trigger the two output junctions.

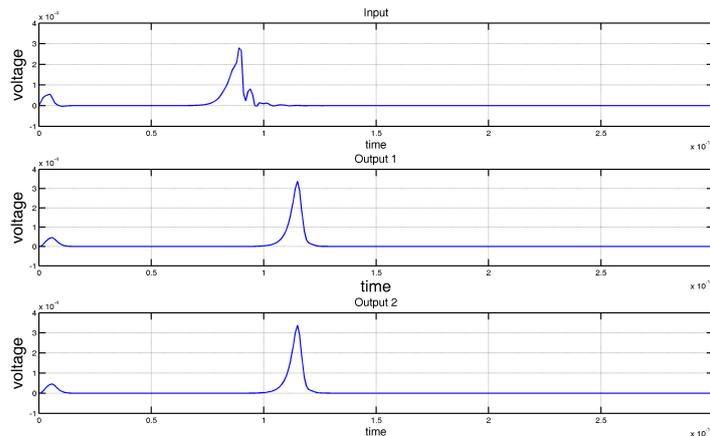

Figure 4.10: The splitter circuit schematic

Extracted Parameters:

IPHT: $J_1 = 325\mu A$, $J_2 = J_3 = 250\mu A$, $L_1 = 1.2pH$, $L_2 = 1.32pH$, $L_3 = 300fH$, $L_4 = 1.5pH$, $L_5 = 1.8pH$, $L_6 = 1.5pH$, $L_7 = 1.8pH$, $L_{p1} = 488fH$ and $L_{p2} = L_{p3} = 300fH$. Bias Current $I_b = 577.8\mu A$

Hypres: $J_1 = 325\mu A$, $J_2 = J_3 = 250\mu A$, $L_1 = 1.25pH$, $L_2 = 1.43pH$, $L_3 = 200fH$, $L_4 = 1.49pH$, $L_5 = 1.74pH$, $L_6 = 1.5pH$, $L_7 = 1.75pH$, $L_{p1} = 167fH$ and $L_{p2} = L_{p3} = 168fH$. Bias Current $I_b = 567.7\mu A$

The splitter is shown in Fig. 4.10. The bias current I_b lifts currents in all three junctions. An incoming signal through L_1 easily switches on J_1 and the resulting flux quantum is pushed into the two superconducting loops $J_1-L_2-L_3-L_4-J_2$ and $J_1-L_2-L_3-L_6-J_3$. Due to the small inductance in the two loops and the symmetrical nature of the loops, J_2 and J_3 switch on simultaneously and outputs 1 and 2 register output pulses thereby reproducing the input at two outputs. Simulation results for the splitter are shown in Fig. 4.11.


Figure 4.11: Simulation Waveforms for the Splitter

It is normal practice to connect the splitter output through JTLs to prevent loading and

unnecessary switching of J_2 and J_3 , but circuit design constraints may not allow such additions. As an alternative, buffer junction (series junctions) can be connected immediately after J_2 and J_3 to prevent leakage current from the output side from switching these junctions.

Layouts for the splitter are shown in Fig. 4.12 and Fig. 4.13. These layouts were made on cell spaces of $150 \times 150 \mu m$ (IPHT) and $100 \times 100 \mu m$ (Hypres).

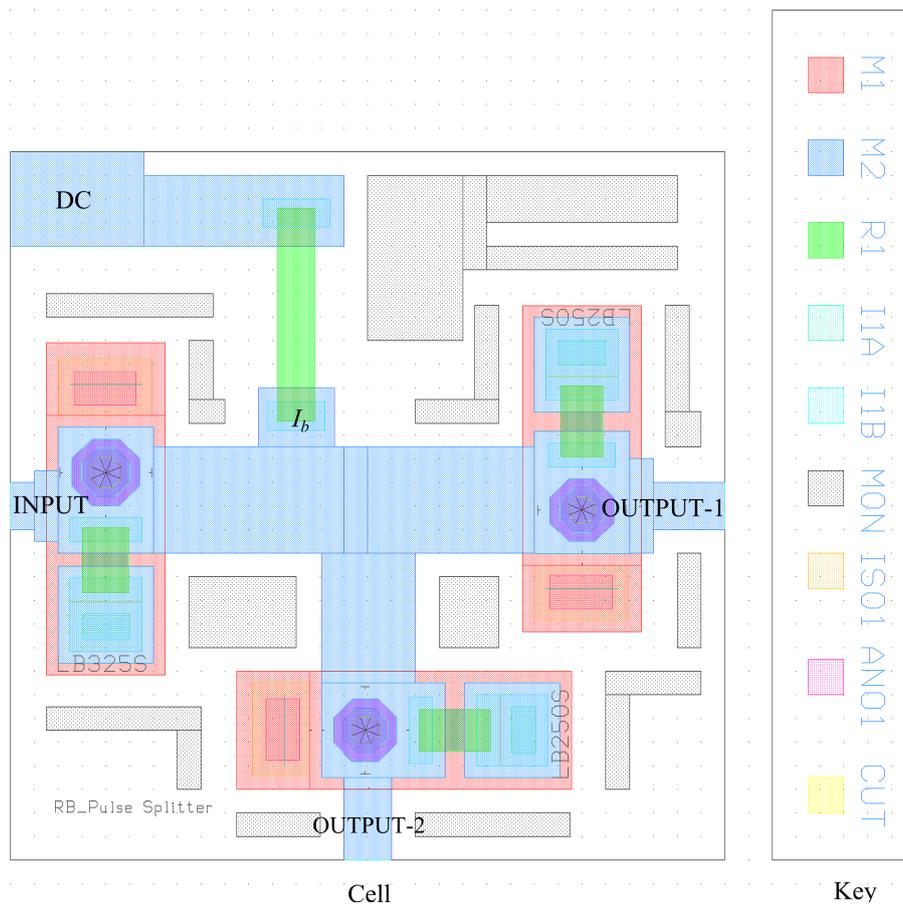


Figure 4.12: Splitter Layout for the IPHT process - $150 \times 150 \mu m$

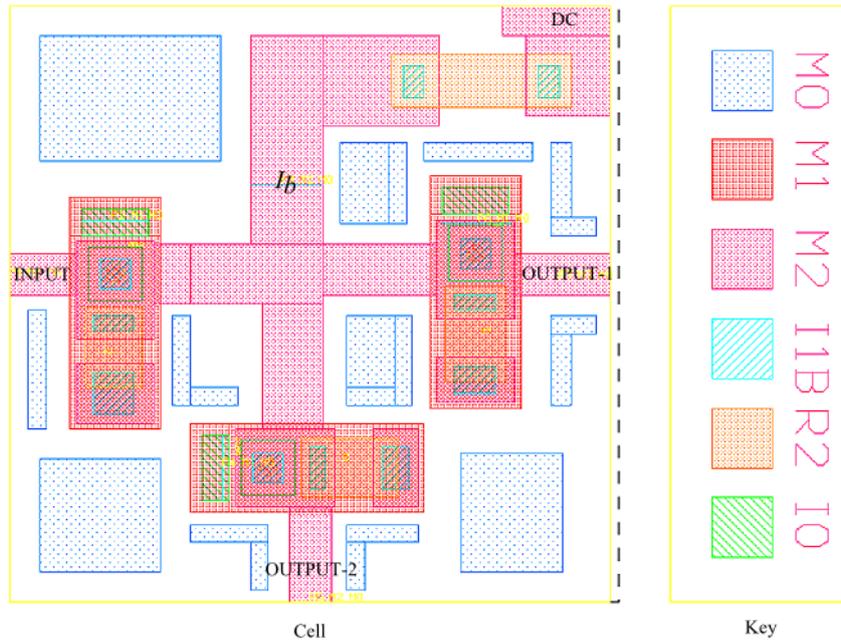


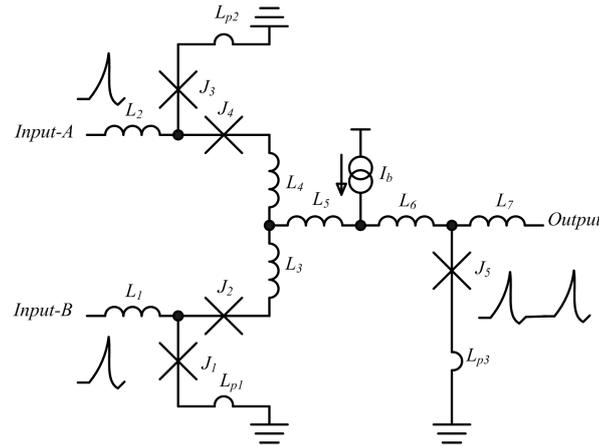
Figure 4.13: Splitter Layout for the Hypres process - $100 \times 100 \mu\text{m}$

4.2.3 Confluence Buffer (Merger)

A confluence buffer (Merger) shown in Fig. 4.14 is an RSFQ circuit that combines and channels two input signals into a single output. In essence, it merges two signal lines.

A typical merger is made up of 5 Josephson junctions, as can be seen in the schematic in Fig. 4.14. Junction J_1 and J_3 are primary drivers that propagate the input pulses at the two inputs into the respective loops $J_1 - J_2 - L_3 - L_5 - L_6 - J_5$ and $J_3 - J_4 - L_4 - L_5 - L_6 - J_5$. The bias current, I_b , lifts the currents in junctions J_1 , J_3 and J_5 . J_1 and J_3 are biased to switch with an input with large enough current to reflect the actual presence of a pulse at the inputs. In contrast, J_5 is biased to switch on easily.

In order to protect the primary drivers, J_1 and J_3 , from affecting the switching of each other, buffer junctions J_2 and J_4 are used. When J_1 switches on with an incoming pulse, J_4 switches on to eliminate the pulse that would otherwise trigger the switching of J_3 . The switching of J_2 can be explained in a similar way.

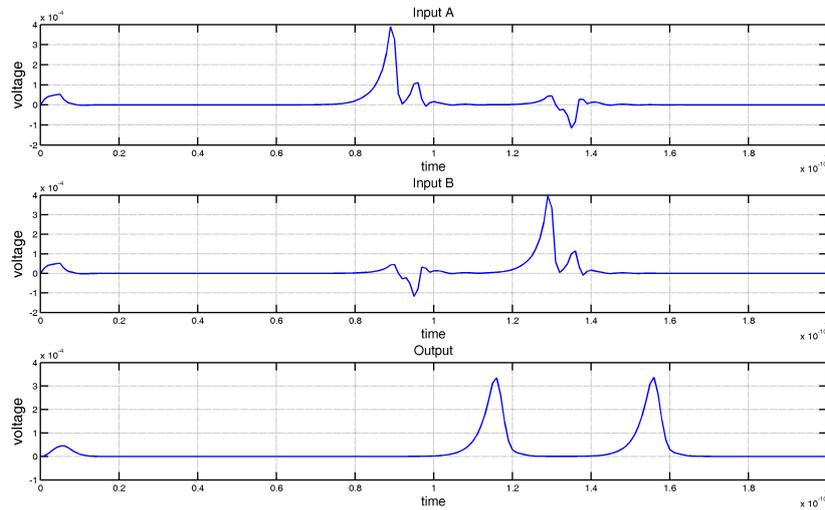

Figure 4.14: Optimized Circuit for a Merger

Extracted Parameters:

IPHT: $J_1 = J_3 = 250\mu A$, $J_2 = J_4 = 200\mu A$, $J_5 = 250\mu A$, $L_1 = L_2 = 1.84pH$, $L_3 = 1.67pH$, $L_4 = 1.55pH$, $L_5 = 200fH$, $L_6 = 2.02pH$, $L_7 = 1.85pH$, $L_{p1} = 269fH$, $L_{p2} = 236fH$ and $L_{p3} = 429fH$. Bias Current $I_b = 472.7\mu A$

Hypres: $J_1 = J_3 = 250\mu A$, $J_2 = J_4 = 225\mu A$, $J_5 = 300\mu A$, $L_1 = 1.44pH$, $L_2 = 1.3pH$, $L_3 = 1.16pH$, $L_4 = 1.14pH$, $L_5 = 100fH$, $L_6 = 1.4pH$, $L_7 = 1.64pH$, $L_{p1} = 214fH$, $L_{p2} = 271fH$ and $L_{p3} = 308fH$. Bias Current $I_b = 541.67\mu A$

The protective switching of J_2 and J_4 is aided by the bias current and by having junctions that have smaller critical currents than the primary driver junctions (i.e. $I_{CJ1} > I_{CJ2}$ and $I_{CJ3} > I_{CJ4}$). This design makes sure that J_2 and J_4 switch on first before J_1 and J_3 can thereby upholding the right operation of the cell.


Figure 4.15: Confluence Buffer simulation waveforms

Simulation waveforms for the Merger are shown in Fig. 4.15. From the waveforms the action of J_2 and J_4 can be observed as the two primary drivers try to switch ON negatively at corresponding points in the input waveforms. The output signal is an effective merging of the two input signals. The merger work correctly when there is a

considerable delay between the two inputs. If two input signals arrive at the two inputs simultaneously, the circuit becomes unstable and only one SFQ pulse is produced at the output.

Layouts for the Merger are shown in Figs. 4.16 and 4.17. The IPHT cell was laid out on a $150 \times 150 \mu m$ and the Hypres cell on a $100 \times 100 \mu m$ space. The series junctions (buffer junctions) contribute to the inductance values of L_3 and L_4 .

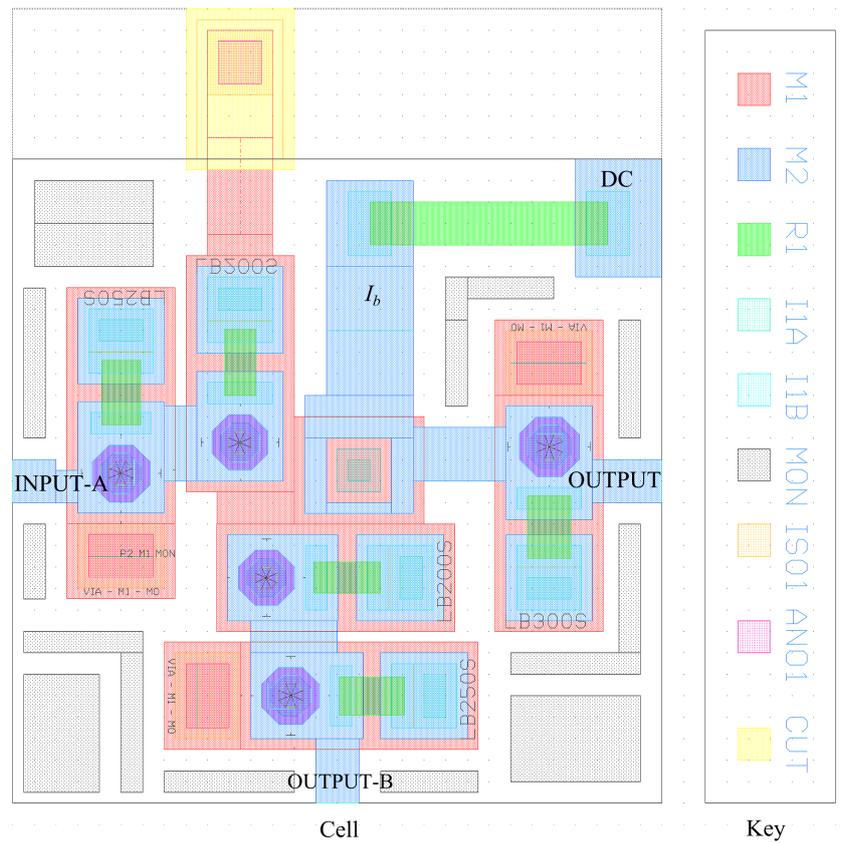


Figure 4.16: Merger cell layout for the IPHT process - $150 \times 150 \mu m$

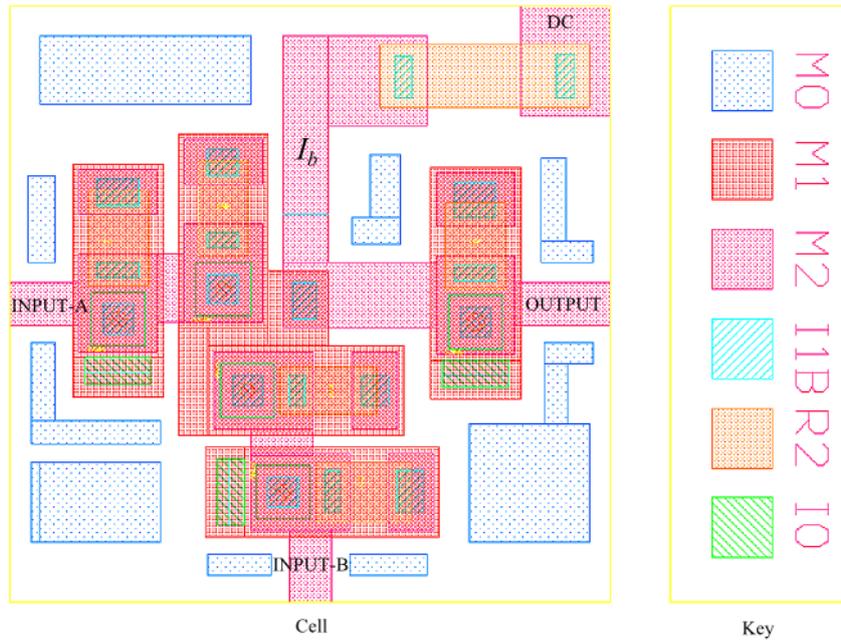


Figure 4.17: Merger cell layout for the Hypres process - $100 \times 100 \mu\text{m}$

4.2.3.1 IPHT's CUT Cell

In the IPHTs fabrication process, a CUT cell is used to protect series junctions from charge accumulation damage during fabrication. The CUT cell provides a temporary junction connection to ground. This connection is then burnt out using a laser. Without the CUT cell the critical currents of the series junction would drift with a margin as high as 20%. The CUT cell is made using a normal M1 to Ground VIA which is then covered entirely with a CUT layer. This cell can be seen in all the IPHT cells presented here wherever series junctions are present. Fig. 4.18 shows the CUT cell.

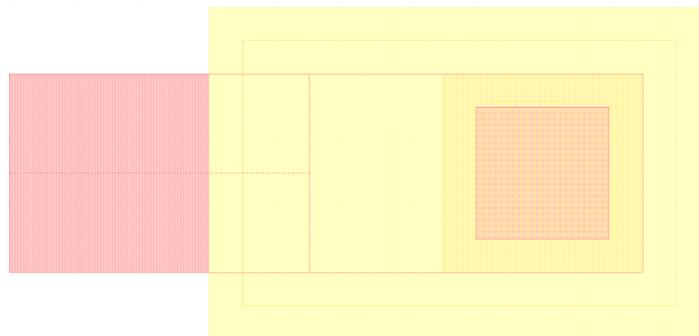


Figure 4.18: IPHT's CUT cell. The dimensions of the CUT cell are standard and set to IPHT's fabrication rules

4.2.4 Delay Flip Flop (DFF)

By far one of the most important cells in RSFQ circuits, a DFF is a bistable cell with a clock dependent operation. A DFF is able to store a single flux quantum (SFQ) until a clock pulse clears it. This attribute can also be applied in the building of low density memory circuits. The RSFQ Delay flip flop is currently used in building circuits such as shift registers and counters.

A DFF is shown in Fig. 4.19. It has 5 junctions and two bias currents. Alternate arrangements exist with 3 junctions [31] and 7 junctions [15]. Both of these are shown in Appendix A. The 5 junction DFF is chosen because of its good operating margins and intermediate number of junction, which still offers immunity from leakage currents from the output side. In Fig. 4.19, I_{b1} biases J_2 and a SFQ pulse at the input easily triggers a 2π leap in J_2 . The resulting SFQ pulse immediately enters the loop $J_2 - L_2 - L_3 - J_4$. The large inductance in the loop causes the SFQ pulse to be trapped within it. The current contribution by the SFQ pulse and I_{b1} is not enough to switch J_4 and the SFQ pulse stays in the loop indefinitely. Any other SFQ pulse coming from the input will not enter the loop because J_2 is still in its voltage state.

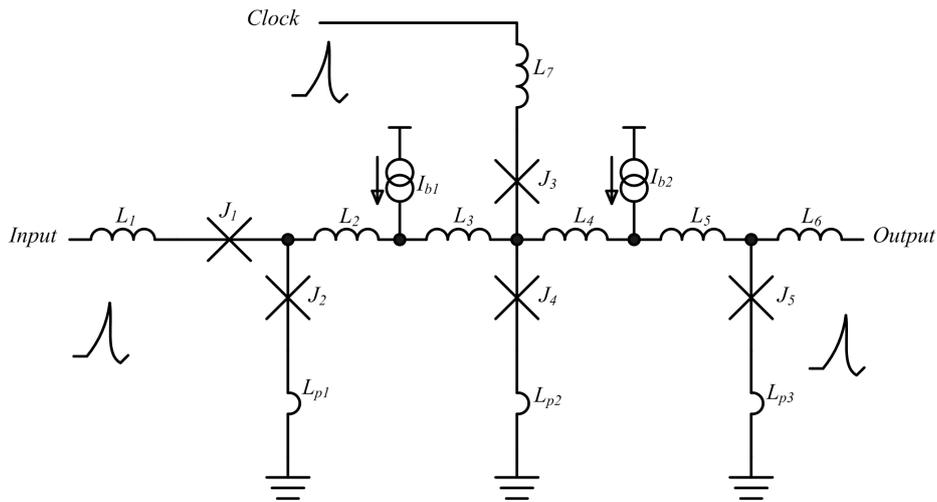


Figure 4.19: DFF Schematic

Extracted parameters:

IPHT: $J_1 = 175\mu A$, $J_2 = 200\mu A$, $J_3 = 150\mu A$, $J_4 = 250\mu A$, $J_5 = 250\mu A$, $L_1 = 2.72pH$, $L_2 = 1.84pH$, $L_3 = 5.51pH$, $L_4 = 1.76pH$, $L_5 = 985fH$, $L_6 = 2.74pH$, $L_7 = 2.82pH$, $L_{p1} = 399fH$, $L_{p2} = 142fH$ and $L_{p3} = 193fH$. Bias Currents: $I_{b1} = 230\mu A$ and $I_{b2} = 135.06\mu A$.

Hypres: $J_1 = 175\mu A$, $J_2 = 200\mu A$, $J_3 = 150\mu A$, $J_4 = 250\mu A$, $J_5 = 250\mu A$, $L_1 = 1.83pH$, $L_2 = 1.25pH$, $L_3 = 6.49pH$, $L_4 = 1.88pH$, $L_5 = 1.06pH$, $L_6 = 1.86pH$, $L_7 = 1.47pH$, $L_{p1} = 286fH$, $L_{p2} = 193fH$ and $L_{p3} = 52fH$. Bias Currents: $I_{b1} = 224.14\mu A$ and $I_{b2} = 185.7\mu A$.

The comparator setup of J_3 and J_4 serves to channel the clock signal and liberate the trapped SFQ pulse in the loop. The comparator works as described in Section 3.2.2.3. The design of the comparator requires that $I_{CJ3} < I_{CJ4}$. If an SFQ pulse exists in the loop and a clock pulse arrives at the clock input then J_4 switches. Otherwise, if there is no SFQ pulse trapped in the loop, J_3 will switch and the clock pulse is lost. Due to the

small inductance in loop $J_4 - L_4 - L_5 - J_5$ the switching of J_4 immediately triggers J_5 . The output follows the input at each and every clock pulse. The operation of the DFF can be summarized as shown in Table 4.4 and the simulation results are shown in Fig. 4.21. The Moore diagram shown in Fig. 4.20 shows the state transition in the DFF.

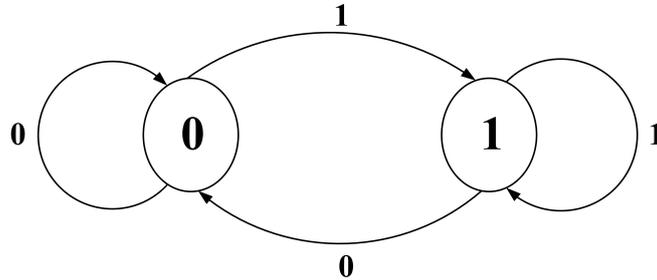


Figure 4.20: Moore diagram for the DFF
The states are as shown i.e. 0 = LOW and 1 = HIGH

| Input | Clock | Output |
|-------|-------|--------|
| 0 | 0 | 0 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |

Table 4.4: Function table for the DFF

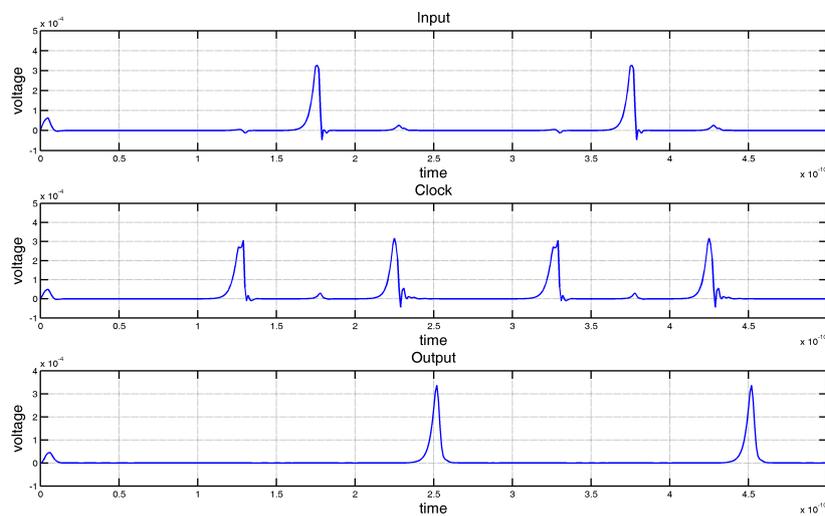


Figure 4.21: DFF Simulation Waveforms

The layouts for the DFF are shown in Figs. 4.22 and 4.23. The IPHT cell was laid out on a $150 \times 150 \mu m$ while the Hypres version fitted on a $100 \times 100 \mu m$ cell space.

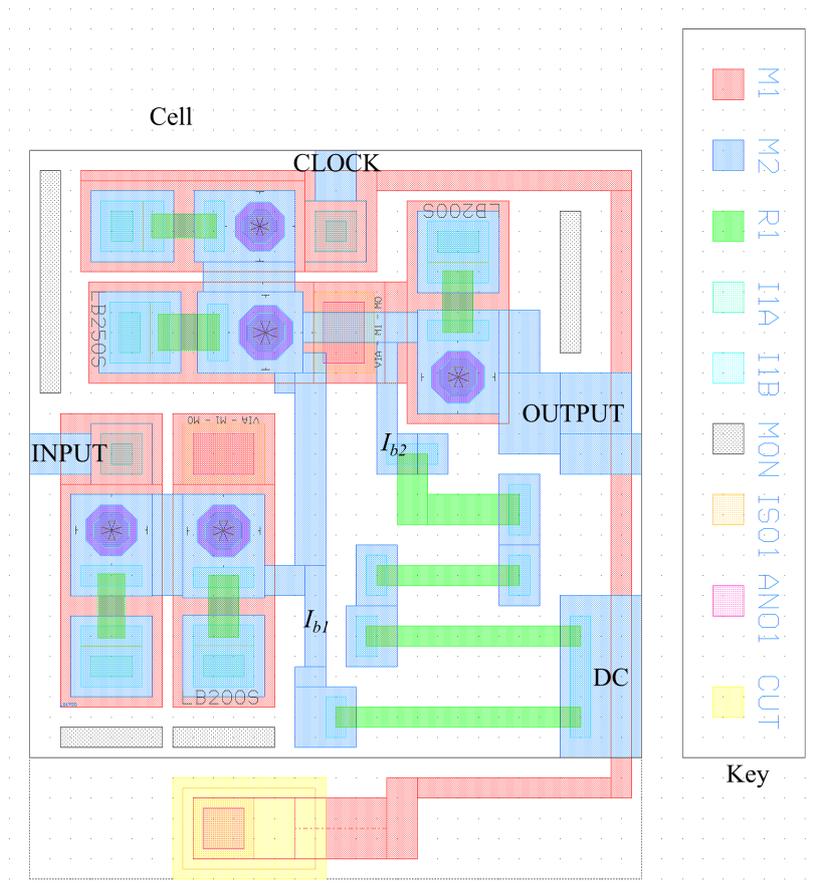


Figure 4.22: DFF Layout for the IPHT process - $150 \times 150 \mu\text{m}$

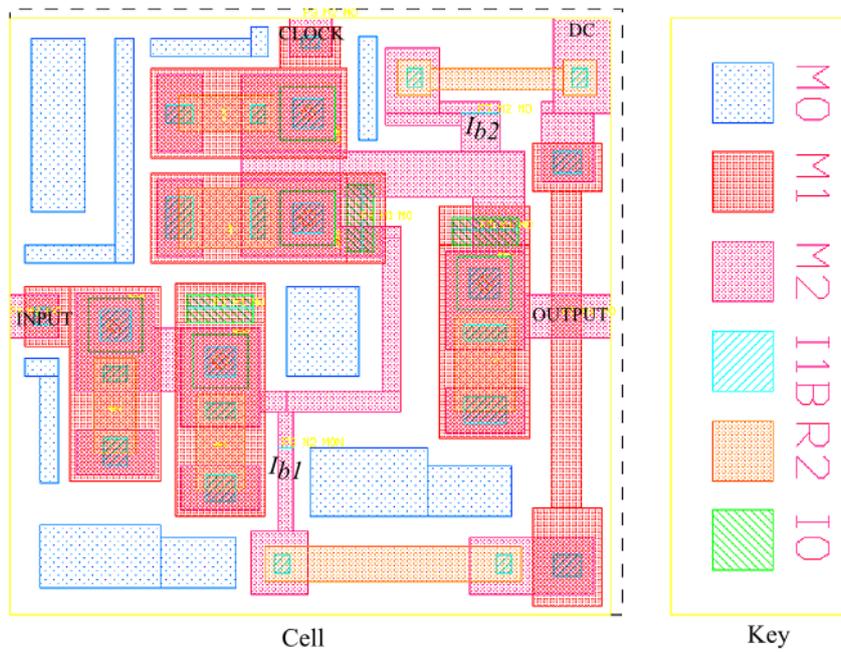


Figure 4.23: DFF Layout for the Hypres process - $100 \times 100 \mu\text{m}$

4.2.5 Toggle Flip Flop (TFF)

The version of TFF discussed here has one input and one output. An alternate version exists which has one input but two outputs. The second version is presented in Appendix B. A TFF is a bistable circuit and its operation depends on its previous state.

A circuit schematic for the TFF shown in Fig. 4.24, is built around a flux loop $L_6 - J_5 - L_7 - J_3 - L_5$ and two JTLs, one at its input and another at its output. The input JTL ($L_1 - J_2 - L_2 - L_3 - J_2 - L_4$) propagates the input SFQ pulse into the loop (Assuming no SFQ existed in the loop before). The current from the SFQ pulse divides through L_5 and L_6 and flows to ground through J_4 and J_6 . I_{b2} biases J_4 and J_5 and they switch on with the incoming current from the SFQ pulse. Two scenarios arise: the switching on of J_4 increases the circulating current in the loop and the switching of J_5 prevents the excess current from switching J_6 , which may eventually trigger the switching of J_7 . The large inductance, L_7 ensures that the current keeps circulating in the loop. The entry of a second input SFQ pulse switches J_3 and J_6 instead. The switching of J_6 immediately triggers J_7 , thereby producing a high on the output. This eventually clears the loop of any stored flux.

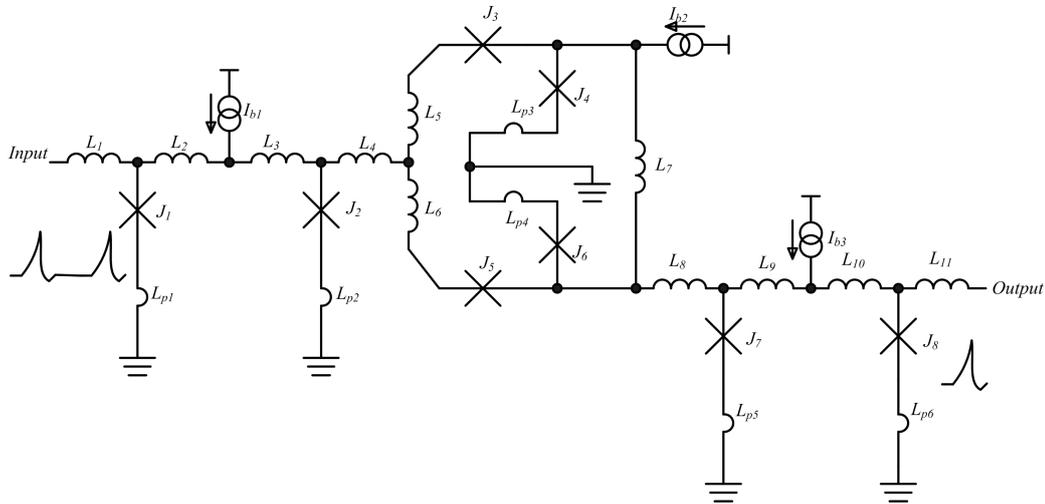


Figure 4.24: A T-Flip-Flop schematic

Extracted Parameters:

IPHT: $J_1 = J_2 = 250\mu A$, $J_3 = 175\mu A$, $J_4 = 300\mu A$, $J_5 = 150\mu A$, $J_6 = 250\mu A$, $J_7 = 200\mu A$, $J_8 = 250\mu A$, $L_1 = 2.03pH$, $L_2 = 1.4pH$, $L_3 = 1.83pH$, $L_4 = 1.27pH$, $L_5 = 819fH$, $L_6 = 988fH$, $L_7 = 4.489pH$, $L_8 = 2.31pH$, $L_9 = 2.95pH$, $L_{10} = 1.15pH$, $L_{11} = 1.16pH$, $L_{p1} = 405fH$, $L_{p2} = 324fH$ and $L_{p3} = 284fH$ Bias Currents: $I_{b1} = 360\mu A$, $I_{b2} = 295.5\mu A$ and $I_{b3} = 260\mu A$.

Hypres: $J_1 = J_2 = 250\mu A$, $J_3 = 175\mu A$, $J_4 = 300\mu A$, $J_5 = 150\mu A$, $J_6 = 250\mu A$, $J_7 = 200\mu A$, $J_8 = 250\mu A$, $L_1 = 1.68pH$, $L_2 = 1.4pH$, $L_3 = 1.87pH$, $L_4 = 973fH$, $L_5 = 1.32pH$, $L_6 = 2.13pH$, $L_7 = 5.4pH$, $L_8 = 3.33pH$, $L_9 = 3.03pH$, $L_{10} = 1.26pH$, $L_{11} = 1.63pH$, $L_{p1} = 286fH$, $L_{p2} = 193fH$, $L_{p3} = 52fH$, $L_{p4} = 276fH$, $L_{p5} = 344fH$, and $L_{p6} = 350fH$ Bias Currents: $I_{b1} = 360\mu A$, $I_{b2} = 295.5\mu A$ and $I_{b3} = 260\mu A$.

The process repeats for all ensuing SFQ pulses and frequency division by two is achieved. A state diagram for the TFF is shown in Fig. 4.25. The simulation results in Fig. 4.26 confirm the frequency division. An input at $5GHz$ is scaled down to $2.5GHz$. The operation of the TFF is summarized in Table 4.5.

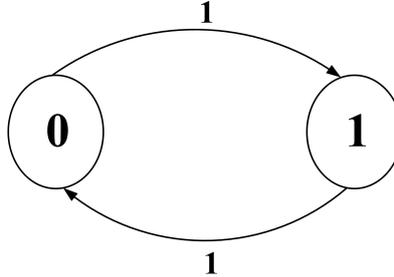


Figure 4.25: TFF Moore Diagram

The states are as shown i.e 0 = LOW and 1 = HIGH

| Input | Loop State | Output |
|-------|------------|--------|
| 0 | 0 | 0 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |

Table 4.5: Functional Table for a TFF

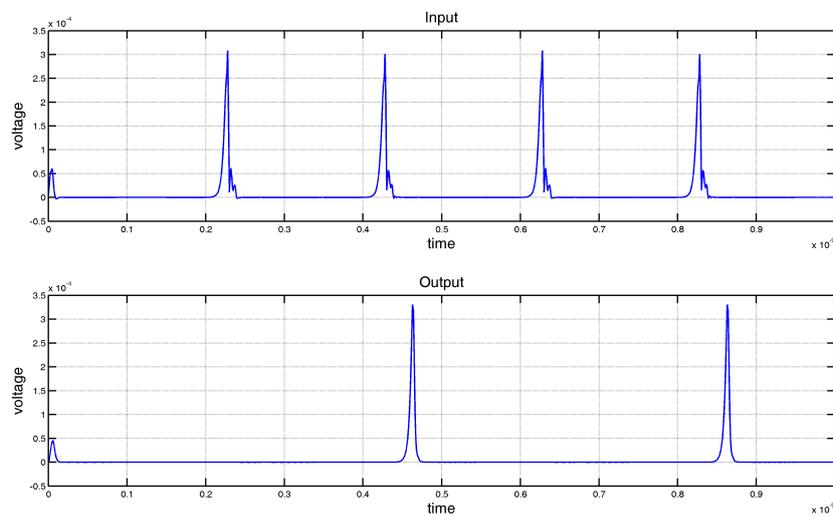


Figure 4.26: TFF Simulation Waveforms

The TFF has its layouts presented in Fig. 4.27 and Fig. 4.28 for the IPHT and Hypres in that order. The IPHT cell covers a space of $300 \times 150\mu m$ and the Hypres cell on $200 \times 100\mu m$.



Figure 4.27: TFF Cell laid out for the IPHT process - $300 \times 150\mu m$

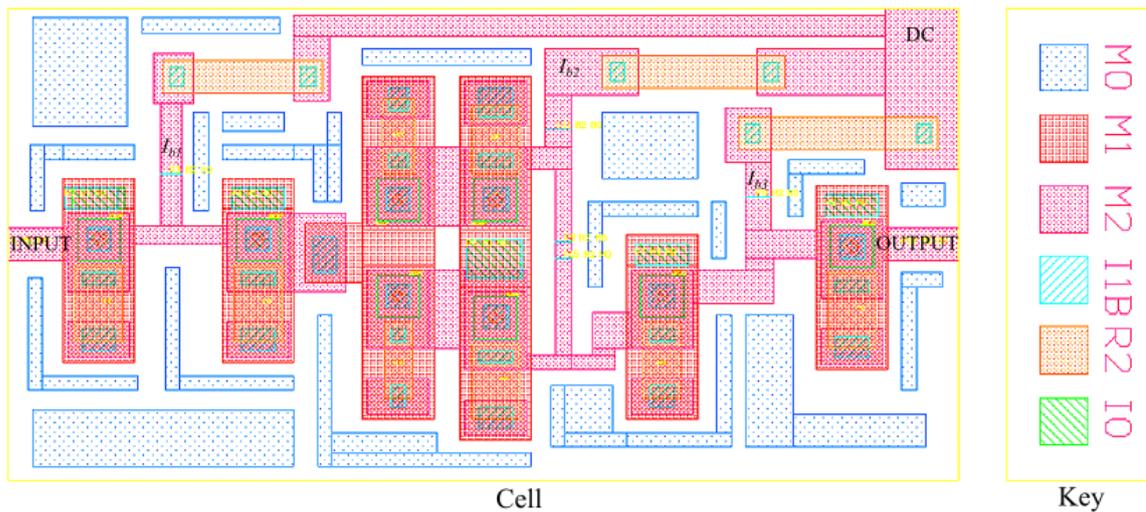


Figure 4.28: TFF Cell laid out for the Hypres process - $200 \times 100\mu m$

4.2.6 NOT Cell

In any digital electronic regime, superconductor or otherwise, a circuit that produces the inversion of the input becomes important. A NOT cell produces the inversion of the input.

A circuit schematic is shown in Fig. 4.29. As can be seen, the NOT cell has 8 Josephson junctions and 4 bias currents. The operation of the cell is slightly similar to that of the TFF discussed earlier. They both depend on the flux loops. A notable contrast is that the NOT cell is a clocked and its operation does not depend entirely on the flux

loop. The input JTL $L_1 - J_1 - L_2 - L_3 - J_2 - L_4$ propagates an input pulse through J_3 into the flux loop $J_4 - L_7 - L_8 - J_5 - L_6$, through the switching of J_4 . Depending on the condition of the flux loop, J_4 easily switches on due to the bias current I_{b2} and the incoming SFQ pulse. The large inductance in the loop, L_6 , ensures that the SFQ pulse remains trapped and its current superimposes on I_{b2} to further increase the current bias to J_5 .

An incoming clock pulse through the half JTL propagates into the loop $J_6 - L_{14} - L_{15} - J_5 - L_8 - L_9 - J_7$. Due to already increased current in the flux loop, the clock easily triggers the switching of J_5 and not J_7 . The output registers a LOW and the flux loop is cleared. Assuming the flux loop was empty, J_7 would switch first to the clock input and a HIGH output would register. In summary, the output is always the inverse of the input.

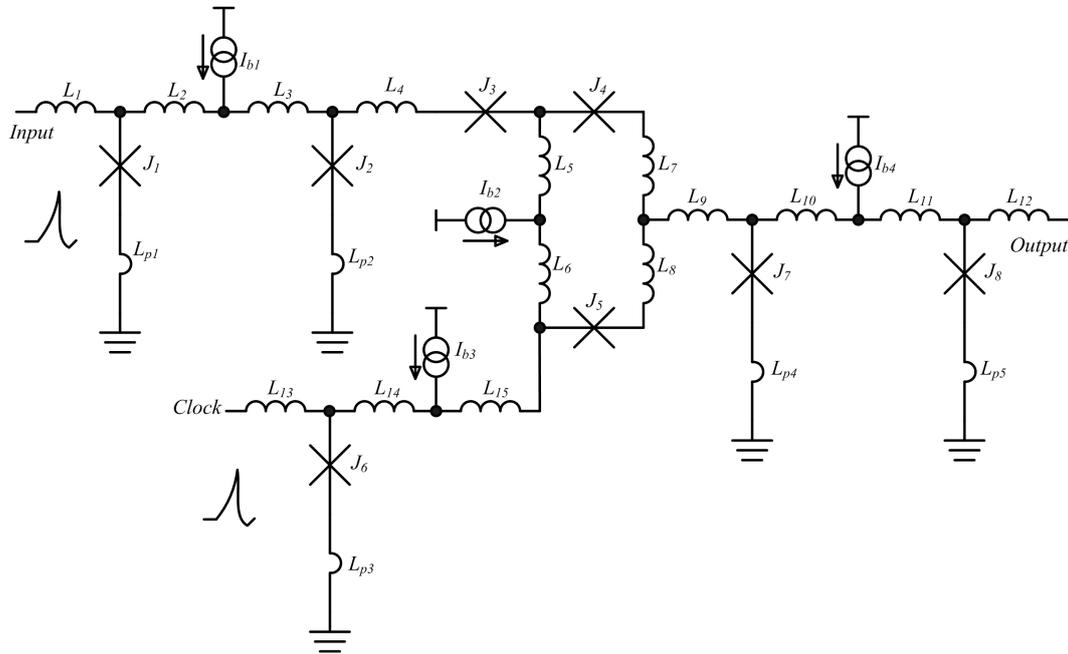


Figure 4.29: NOT cell schematic

Extracted Parameters:

IPHT: $J_1 = 250\mu A$, $J_2 = 350\mu A$, $J_3 = 150\mu A$, $J_4 = 175\mu A$, $J_5 = 275\mu A$, $J_6 = 275\mu A$, $J_7 = 250\mu A$, $J_8 = 250\mu A$, $L_1 = 1.22pH$, $L_2 = 740fH$, $L_3 = 750fH$, $L_4 = 1.67pH$, $L_5 = 100fH$, $L_6 = 6.2pH$, $L_7 = 700fH$, $L_8 = 500fH$, $L_9 = 1.32pH$, $L_{10} = 2.29pH$, $L_{11} = 1.06pH$, $L_{12} = 2.27pH$, $L_{13} = 1.62pH$, $L_{14} = 500fH$, $L_{15} = 500fH$, $L_{p1} = 409fH$, $L_{p2} = 493fH$, $L_{p3} = 346fH$, $L_{p4} = 380fH$, $L_{p5} = 330fH$. Bias Currents: $I_{b1} = 250\mu A$, $I_{b2} = 240.1\mu A$, $I_{b3} = 155.7\mu A$, $I_{b4} = 185.1\mu A$.

Hypres: $J_1 = 250\mu A$, $J_2 = 300\mu A$, $J_3 = 150\mu A$, $J_4 = 175\mu A$, $J_5 = 300\mu A$, $J_6 = 275\mu A$, $J_7 = 300\mu A$, $J_8 = 250\mu A$, $L_1 = 1.47pH$, $L_2 = 1.21fH$, $L_3 = 750fH$, $L_4 = 1.09pH$, $L_5 = 300fH$, $L_6 = 6.35pH$, $L_7 = 825fH$, $L_8 = 593fH$, $L_9 = 1.15pH$, $L_{10} = 1.5pH$, $L_{11} = 920fH$, $L_{12} = 1.87pH$, $L_{13} = 1.62pH$, $L_{14} = 500fH$, $L_{15} = 500fH$, $L_{p1} = 226fH$, $L_{p2} = 311fH$, $L_{p3} = 586fH$, $L_{p4} = 108fH$, $L_{p5} = 112fH$. Bias Currents: $I_{b1} = 250\mu A$, $I_{b2} = 236.4\mu A$, $I_{b3} = 155.7\mu A$, $I_{b4} = 185.5\mu A$.

Margin analysis results show that the flux loop is the most sensitive element of the circuit with the narrowest margins registered on J_5 . Junction J_3 acts as an escape junction and it eliminates any backward current that would otherwise switch J_2 , causing the circuit to malfunction. J_3 switches first before J_2 can.

A Mealey transition diagram for the NOT cell is shown Fig. 4.30. The operation of the NOT is supported by the function table as shown in Table 4.6, and simulation waveforms depicted in Fig. 4.31.

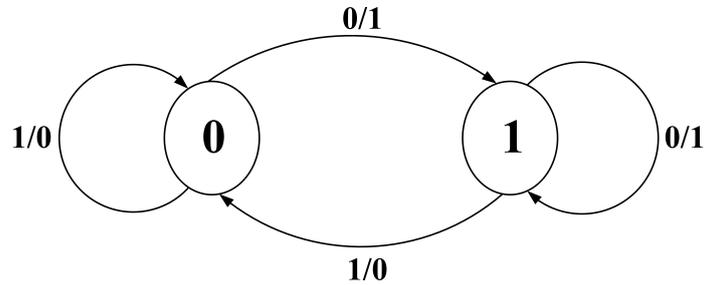


Figure 4.30: Mealey transition diagram for the NOT
The states are as shown i.e. 0 = LOW and 1 = HIGH

| Loop State | Clock | Output |
|------------|-------|--------|
| 0 | 0 | 0 |
| 1 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

Table 4.6: NOT Function Table

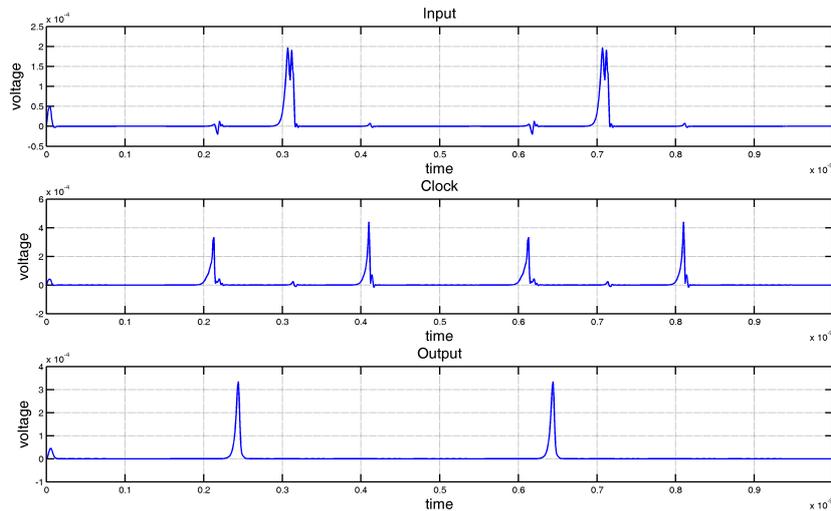


Figure 4.31: NOT Simulation waveforms

Cell layouts for the NOT were done while employing the same orientation in both IPHT and Hypres. The IPHT cell fitted on a $300 \times 150 \mu\text{m}$ space while the Hypres cell occupied a $200 \times 100 \mu\text{m}$ space. They are both shown in Figs. 4.32 and 4.33.

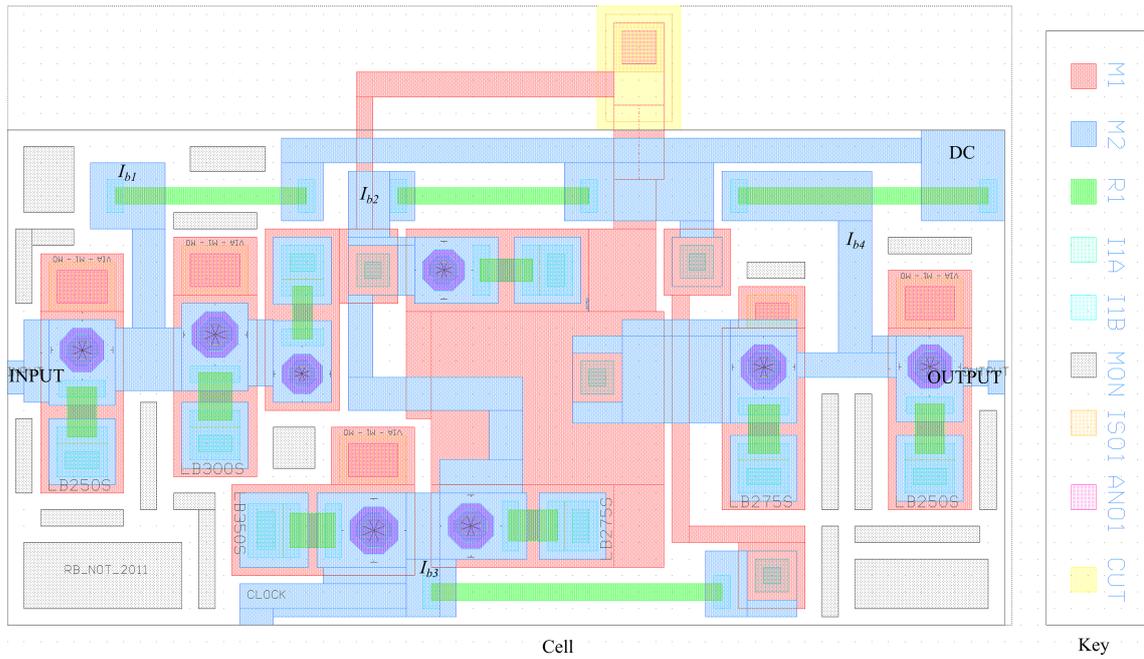


Figure 4.32: NOT Cell for the IPHT process - $300 \times 150\mu\text{m}$

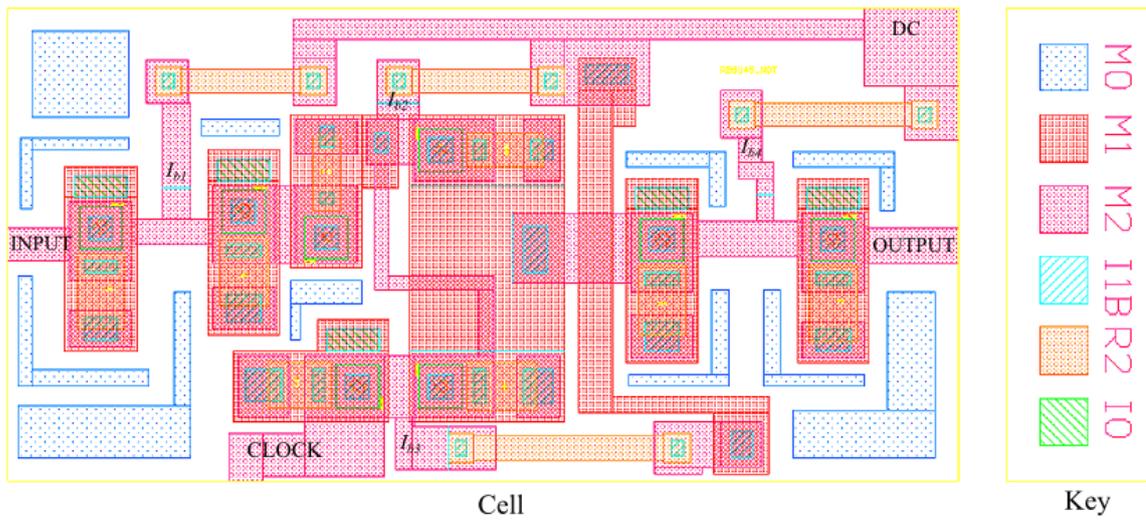


Figure 4.33: NOT Cell for the IPHT process - $200 \times 100\mu\text{m}$

4.2.7 OR Cell

An OR cell produces a HIGH output if either of the two inputs is HIGH. It can therefore be used to isolate a condition where both inputs are LOW. An RSFQ version of the OR cell is shown in Fig. 4.34 in its circuit schematic form. It is a two input cell, but unlike the CMOS version, this version requires clocking. The need for clocking increases the complexity of the cell but more control is made available.

The OR cell shown below has two parts; a Merger and a slightly modified DFF. It has a

total of 9 Josephson junctions and two bias sources. Other configurations exist but this particular design was adopted, because of its superior bias margins. A Merger alone can act as an OR cell, but a huge drawback would be lack of control and a condition where both inputs are HIGH would be difficult to handle. The modified DFF can hold a data pulse until a clock pulse arrives. It is vital to note that this circuit needs only one input to be HIGH. This being the case, loop $J_7 - L_8 - J_9$ will only hold one SFQ until it gets cleared. Any pulse that arrives afterwards will not be allowed in the loop and will be lost through J_6 . In addition, J_6 prevents any backward pulse from reaching J_5 .

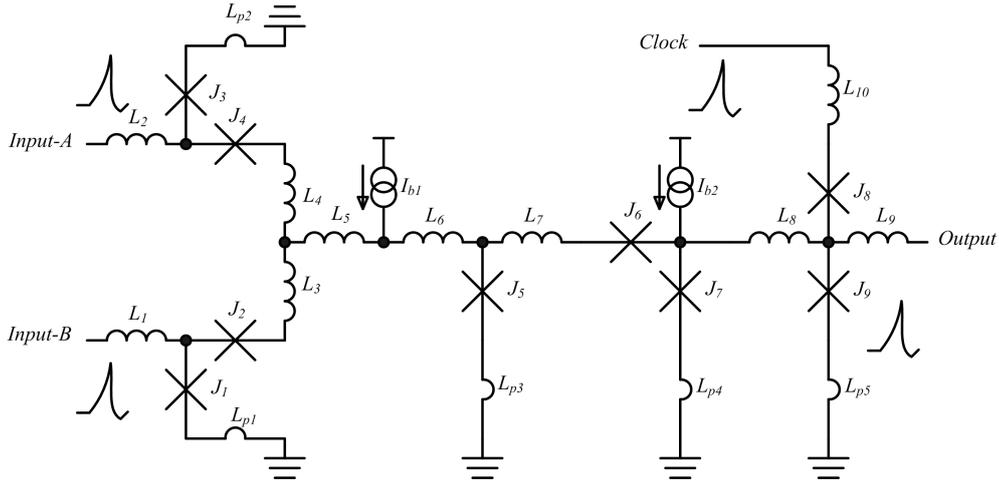


Figure 4.34: OR cell schematic

Extracted Parameters:

IPHT: $J_1 = J_3 = 250\mu A$, $J_2 = J_4 = 175\mu A$, $J_5 = 250\mu A$, $J_6 = 250\mu A$, $J_7 = 225\mu A$, $J_8 = 175\mu A$, $J_9 = 200\mu A$, $L_1 = 1.17pH$, $L_2 = 1pH$, $L_3 = 1.14pH$, $L_4 = 1.52pH$, $L_5 = 800fH$, $L_6 = 2.36pH$, $L_7 = 1.4pH$, $L_8 = 10.5pH$, $L_9 = 3pH$, $L_{10} = 2.22pH$, $L_{p1} = 310fH$, $L_{p2} = 364fH$, $L_{p3} = 285fH$, $L_{p4} = 1.042pH$, $L_{p5} = 296fH$. Bias Currents: $I_{b1} = 250\mu A$, $I_{b2} = 240.1\mu A$

Hypres: $J_1 = J_3 = 250\mu A$, $J_2 = J_4 = 175\mu A$, $J_5 = 250\mu A$, $J_6 = 250\mu A$, $J_7 = 225\mu A$, $J_8 = 200\mu A$, $J_9 = 225\mu A$, $L_1 = 1.15pH$, $L_2 = 1.14pH$, $L_3 = 1.5pH$, $L_4 = 1.5pH$, $L_5 = 800fH$, $L_6 = 2.35pH$, $L_7 = 1.54pH$, $L_8 = 10.5pH$, $L_9 = 3.2pH$, $L_{10} = 1.93pH$, $L_{p1} = 149fH$, $L_{p2} = 154fH$, $L_{p3} = 130fH$, $L_{p4} = 660fH$, $L_{p5} = 52fH$. Bias Currents: $I_{b1} = 250\mu A$, $I_{b2} = 240.1\mu A$

Due to the modified nature of the output, L_9 is made slightly larger to prevent current leakage from the output from causing J_9 to switch. A Mealey state machine shown in Fig. 4.35 depicts the transitions in the OR cell. Table 4.7 shows the function table for the OR cell followed by simulation results in Fig. 4.36.

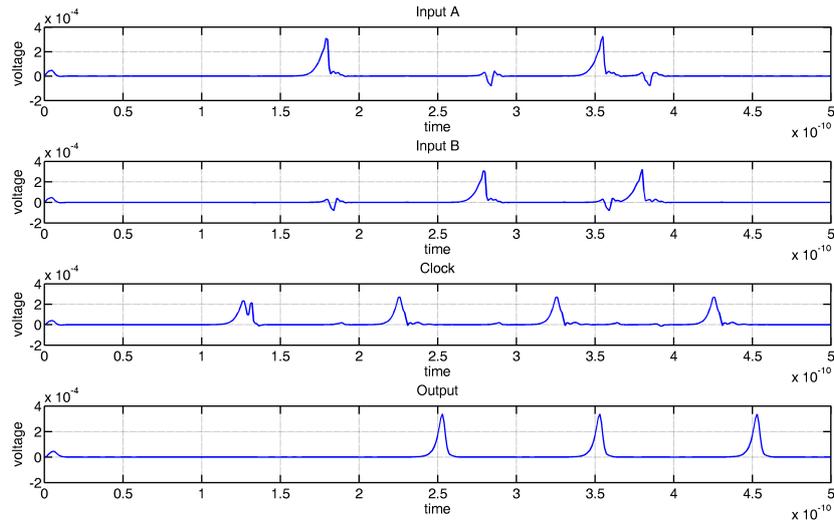


Figure 4.36: OR cell simulation waveforms

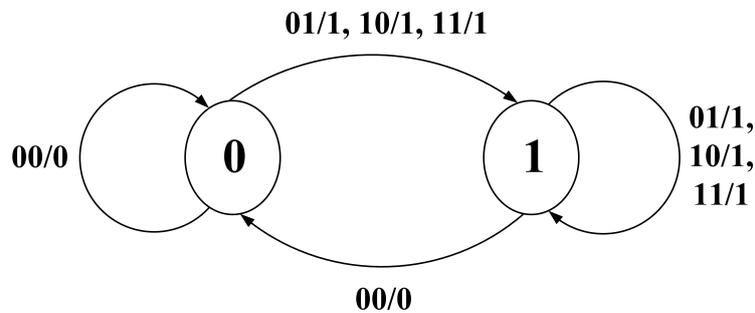


Figure 4.35: Mealey state diagram for the OR Cell
The states are as indicated, i.e. 0 → *LOW*, 1 → *HIGH*

| Input-A | Input-B | Clock | Output |
|----------|----------|----------|----------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 |

Table 4.7: OR Function Table

Layouts for the OR cell are shown in Figs. 4.37 and 4.38 for the IPHT and Hypres processes respectively.

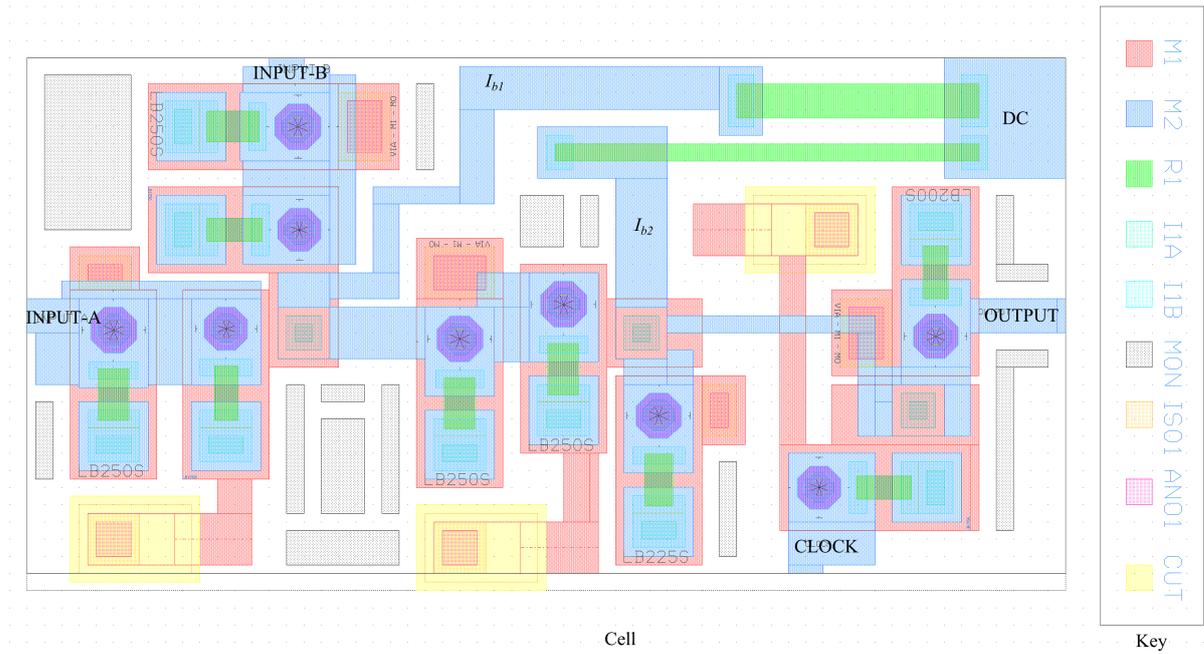


Figure 4.37: OR Cell layout for IPHT - $300 \times 150 \mu m$

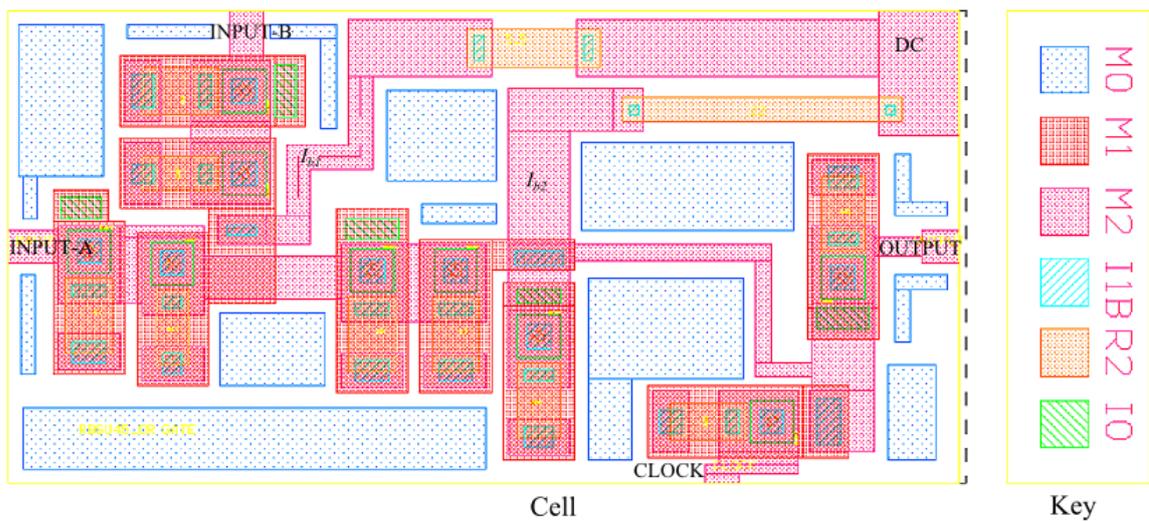


Figure 4.38: OR Cell layout for Hypres - $200 \times 100 \mu m$

4.2.8 NOR Cell

The NOR cell, as expected, does the exact opposite to what the OR does. It produces a HIGH output when both inputs are LOW. This manner of operation means that the output is not triggered by the currents caused by the input SFQ pulses and therefore a separate circuit needs to interpret the absence of an SFQ as a trigger condition.

The NOR cell was therefore designed to first be able to detect the states of either inputs and make their state(s) available to a sub-circuit that inverts these state(s). A NOR cell

designed with this approach has a modified Merger to bring the two inputs onto a single stream and its output is matched and propagated into a modified NOT function. In this way, the clocking is only required at the NOT stage. In addition, the modifications done, made sure that the cell had the minimum possible number of Josephson junctions. The resulting design is shown in Fig. 4.39

The operation of the NOR cell is hereby discussed with reference to Fig. 4.39. If both inputs are LOW, the flux loop $J_8 - L_{12} - L_{13} - J_9 - L_{11} - L_{10}$ remains empty. A clock pulse will in this state easily switch on J_{10} (Refer to Section 4.2.6) and the output is HIGH. If, however, an SFQ pulse is trapped in the loop (i.e. either Input A or Input B or both are high), J_9 instead switches on at each clock pulse and the output is LOW all the time.

Inductance L_6 was designed to be slightly larger so that less current goes into J_5 . This design protects this junction from switching on due to the bias currents (I_{b1} and I_{b2}) only, which would cause the whole circuit to malfunction. A Mealy machine for the NOR is shown in Fig. 4.40, and its operation is summarized in Table 4.8.

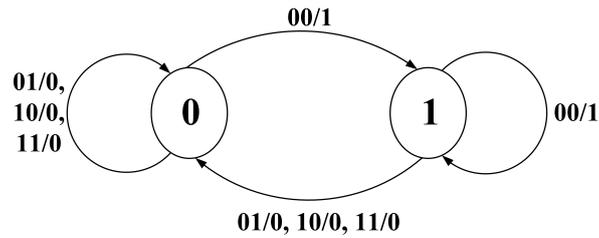


Figure 4.40: Mealy Machine for the NOR cell

The states are as indicated, i.e 0 \rightarrow LOW, 1 \rightarrow HIGH

| Input-A | Input-B | Clock | Output |
|----------|----------|----------|----------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 |

Table 4.8: NOR cell Functional Table

Simulation results done with Niopulse are shown in Fig. 4.41. It can be seen that the output is HIGH only when both inputs are LOW.

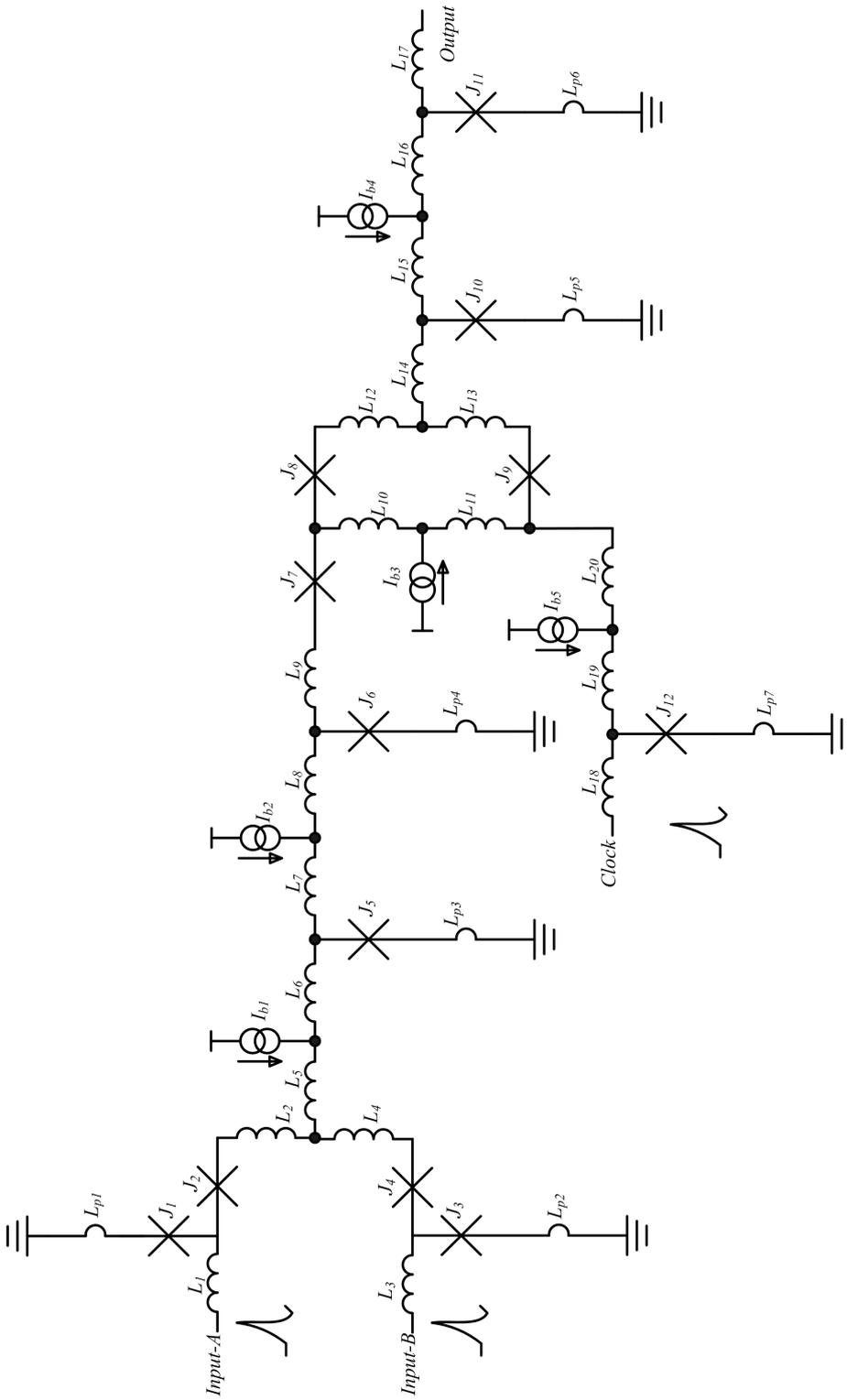


Figure 4.39: NOR Cell Schematic

Extracted and optimized parameters:

IPHT: $J_1 = J_3 = J_5 = J_{11} = 250\mu\text{A}$; $J_2 = J_4 = 200\mu\text{A}$; $J_9 = 275\mu\text{A}$; $J_{10} = J_{12} = 300\mu\text{A}$; $J_7 = J_8 = 150\mu\text{A}$; $J_6 = 325\mu\text{A}$; $L_1 = L_2 = 960\text{fH}$; $L_2 = L_4 = 1.86\text{pH}$; $L_5 = 945\text{fH}$; $L_6 = 4.96\text{pH}$; $L_7 = 2.03\text{pH}$; $L_8 = 1.96\text{pH}$; $L_9 = 2.85\text{pH}$; $L_{10} = 100\text{fH}$; $L_{11} = 6.63\text{pH}$; $L_{12} = 1.69\text{pH}$; $L_{13} = 200\text{fH}$; $L_{14} = 560\text{fH}$; $L_{15} = 1.55\text{pH}$; $L_{16} = 2.2\text{pH}$; $L_{17} = 1.5\text{pH}$; $L_{18} = 1.86\text{pH}$; $L_{19} = 1.14\text{pH}$; $L_{20} = 1.08\text{pH}$; $L_{p1} = 644\text{fH}$; $L_{p2} = 644\text{fH}$; $L_{p3} = 192\text{fH}$; $L_{p4} = 234\text{fH}$; $L_{p5} = 268\text{fH}$; $L_{p6} = 246\text{fH}$; $L_{p7} = 263\text{fH}$; *Bias Currents:* $I_{b1} = 351.4\mu\text{A}$; $I_{b2} = 226\mu\text{A}$; $I_{b3} = 173.3\mu\text{A}$ and $I_{b5} = 155.7\mu\text{A}$.

Hypres: $J_1 = J_3 = J_5 = J_{11} = 250\mu\text{A}$; $J_2 = J_4 = 200\mu\text{A}$; $J_9 = J_{10} = J_{12} = 300\mu\text{A}$; $J_7 = J_8 = 150\mu\text{A}$; $J_6 = 325\mu\text{A}$; $L_1 = L_2 = 1.17\text{pH}$; $L_2 = L_4 = 1.68\text{pH}$; $L_5 = 655\text{fH}$; $L_6 = 3.64$; $L_7 = L_8 = 1.6\text{pH}$; $L_9 = 2.16\text{pH}$; $L_{10} = 100\text{fH}$; $L_{11} = 6.7\text{pH}$; $L_{12} = 1.8\text{pH}$; $L_{13} = 440\text{fH}$; $L_{14} = 395\text{fH}$; $L_{15} = 1.0\text{pH}$; $L_{16} = 1.97\text{pH}$; $L_{17} = 1.27\text{pH}$; $L_{18} = 1.4\text{pH}$; $L_{19} = 1.07\text{pH}$; $L_{20} = 800\text{fH}$; $L_{p1} = 288\text{fH}$; $L_{p2} = 287\text{fH}$; $L_{p3} = 84\text{fH}$; $L_{p4} = 116\text{fH}$; $L_{p5} = 274\text{fH}$; $L_{p6} = 118\text{fH}$; $L_{p7} = 263\text{fH}$; *Bias Currents:* $I_{b1} = 351.4\mu\text{A}$; $I_{b2} = 226\mu\text{A}$; $I_{b4} = 162.5\mu\text{A}$ and $I_{b5} = 155.7\mu\text{A}$.

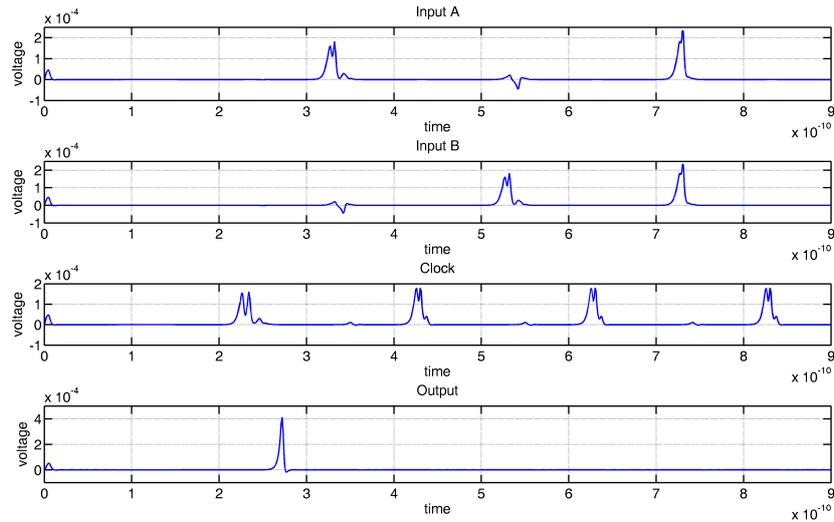


Figure 4.41: NOR simulation waveforms

LASI layouts for the IPHT and Hypres processes are shown in Figs. 4.42 and 4.43. Clocked two-input cells require a large space due to a usual requirement of more Josephson junctions, but also to be able to accommodate two connecting JTLs on each side without any overlaps between them. The IPHT cell occupies a space of $300 \times 300 \mu\text{m}$ while the Hypres version fits on a $200 \times 200 \mu\text{m}$ space.

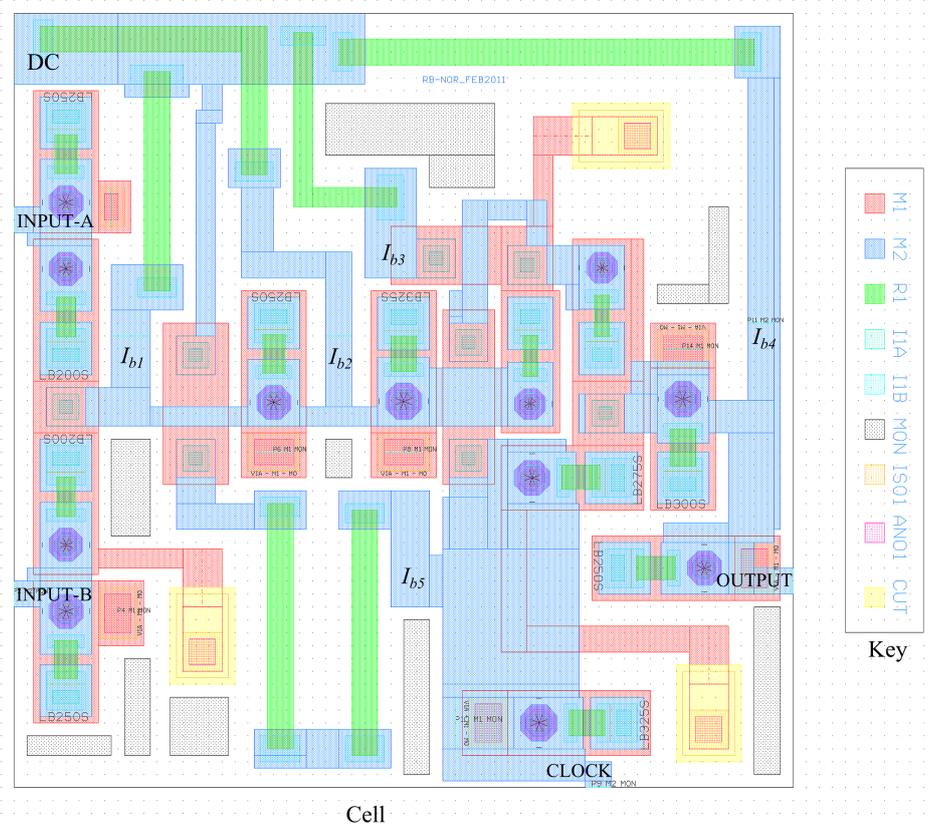


Figure 4.42: NOR Cell Layout for IPHT process - $300 \times 300 \mu\text{m}$

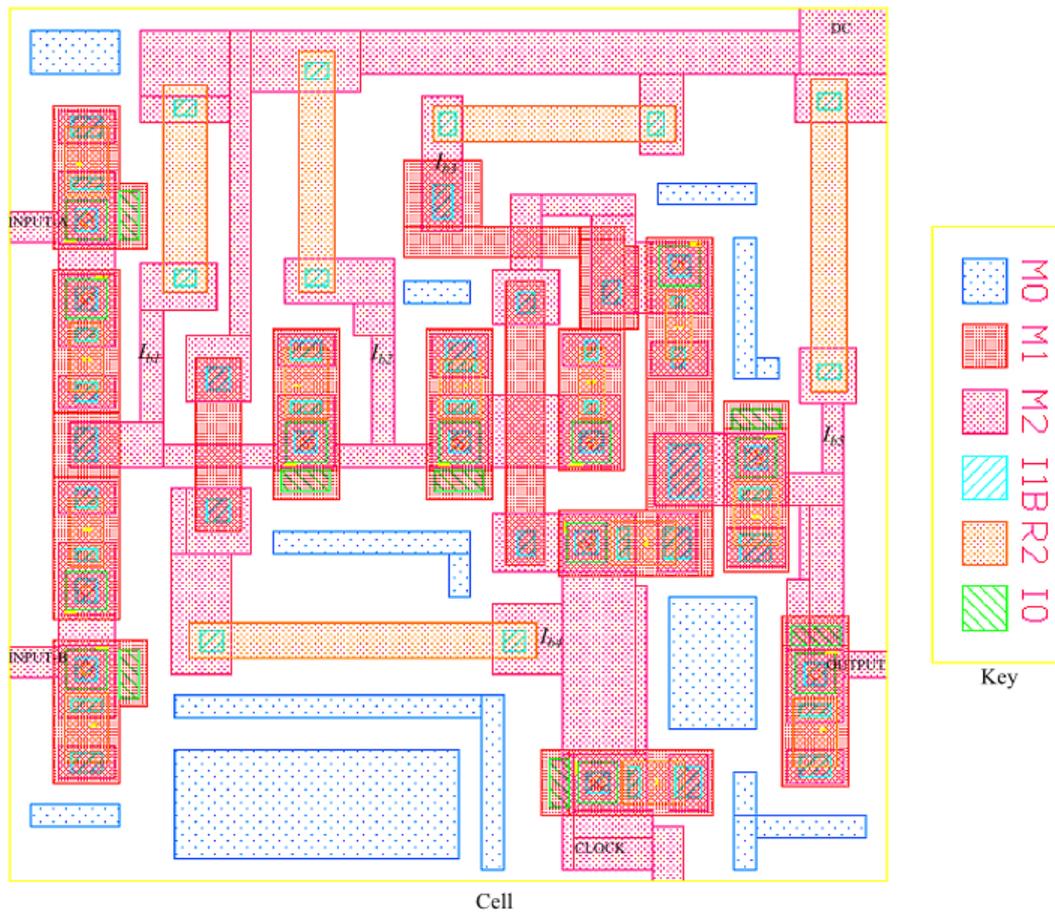


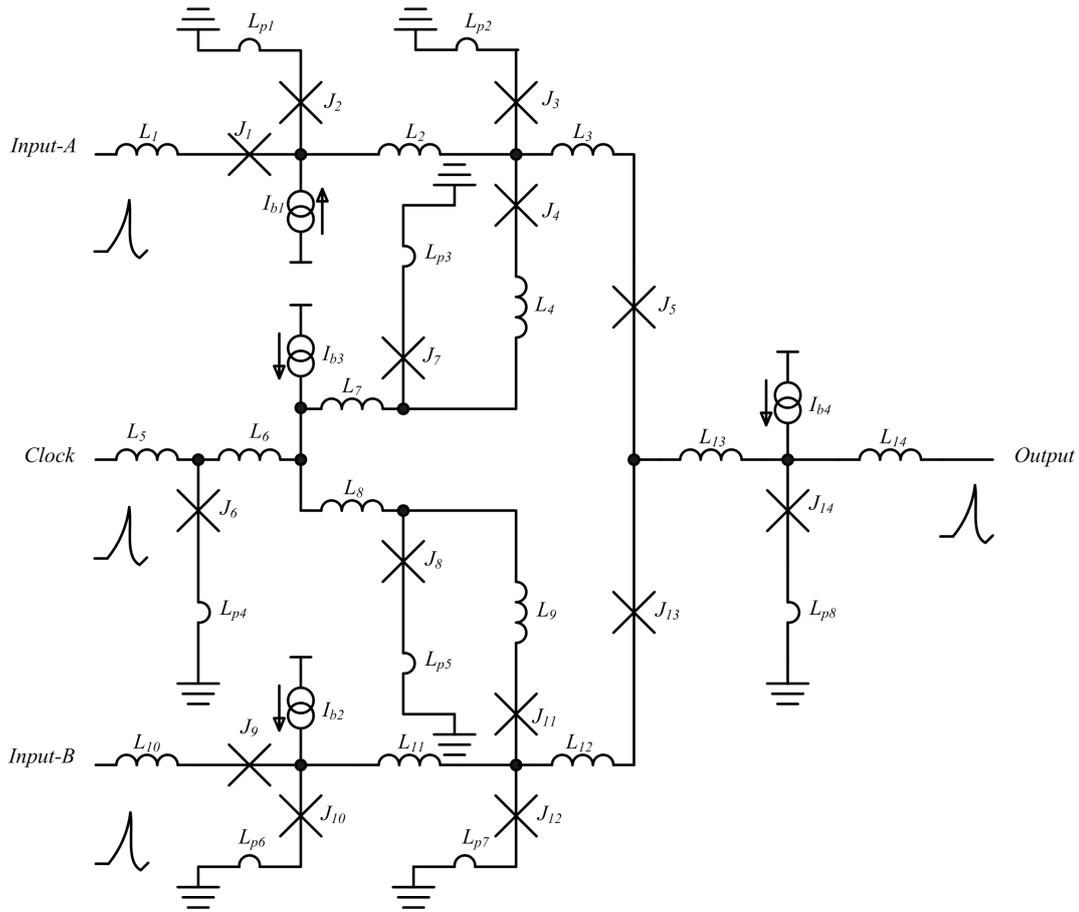
Figure 4.43: NOR Cell Layout for Hypres process - $200 \times 200 \mu\text{m}$

4.2.9 AND Cell

The AND cell is an RSFQ cell that produces a HIGH only if both of its inputs are HIGH. It becomes useful when the occurrence of two conditions needs to trigger an external circuit.

An optimized version of the AND cell is shown in Fig. 4.44. It can be noted that the AND cell has 14 Josephson junctions and 4 bias currents. In essence, the AND has 4 sub-circuits, two modified input DFFs for both inputs, a Splitter for clock distribution to the DFFs and an output half JTL, whose switching depends on the DFFs' output currents.

SFQ pulses at both inputs will raise currents in loops $J_2 - L_2 - J_3$ and $J_{10} - L_{11} - J_{11}$. The arrival of clock pulses from the splitter switches on J_3 and J_{11} , which will both push current to the output J_{14} . The current from these two junctions, superimposed on I_{b4} , is enough to switch on the output junction J_{14} . This junction will only switch on if there is a high enough current which, in this setup, can only emanate from SFQ pulses being available at both inputs. This is how the AND function is achieved by the schematic in Fig. 4.44.


Figure 4.44: AND Cell circuit schematic

Extracted Parameters:

IPHT: $J_1 = J_3 = J_9 = J_{12} = 225\mu A$, $J_2 = J_7 = J_8 = J_{10} = 250\mu A$, $J_4 = J_{11} = 175\mu A$, $J_5 = J_{13} = 150\mu A$, $J_6 = 325\mu A$ and $J_{14} = 300\mu A$; $L_1 = 2.13pH$, $L_2 = 8.33pH$, $L_3 = 3.33pH$, $L_4 = 3.5pH$, $L_5 = 500fH$, $L_6 = 500fH$, $L_7 = 2.25pH$, $L_8 = 2.25pH$, $L_9 = 3.5pH$, $L_{10} = 1.996pH$, $L_{11} = 8.12pH$, $L_{13} = 1.8pH$, $L_{14} = 2.29pH$; $L_{p1} = 180fH$, $L_{p2} = 300fH$, $L_{p3} = 300fH$, $L_{p4} = 300fH$, $L_{p5} = 300fH$, $L_{p6} = 180fH$, $L_{p7} = 300fH$, $L_{p8} = 600fH$; Bias Currents: $I_{b1} = I_{b3} = 175.1\mu A$; $I_{b2} = 577.8\mu A$; and $I_{b4} = 144.4\mu A$

Hypres: $J_1 = J_3 = J_9 = J_{12} = 225\mu A$, $J_2 = J_7 = J_8 = J_{10} = 250\mu A$, $J_4 = J_{11} = 200\mu A$, $J_5 = J_{13} = 200\mu A$, $J_6 = 325\mu A$ and $J_{14} = 325\mu A$; $L_1 = 2.17pH$, $L_2 = 6.45pH$, $L_3 = 2.5pH$, $L_4 = 3.52pH$, $L_5 = 1.28pH$, $L_6 = 1.5pH$, $L_7 = 1.9pH$, $L_8 = 1.6pH$, $L_9 = 3.08pH$, $L_{10} = 2.2pH$, $L_{11} = 6.45pH$, $L_{13} = 977fH$, $L_{14} = 2.03pH$; $L_{p1} = 83fH$, $L_{p2} = 540fH$, $L_{p3} = 134fH$, $L_{p4} = 132fH$, $L_{p5} = 215fH$, $L_{p6} = 96fH$, $L_{p7} = 305fH$, $L_{p8} = 302fH$; Bias Currents: $I_{b1} = I_{b3} = 175.1\mu A$; $I_{b2} = 577.8\mu A$; and $I_{b4} = 144.4\mu A$.

State transitions for the AND cell are shown Fig. 4.45. The operation of the AND cell is summarized in functional table in Table 4.9. In addition, simulation results are shown in Fig. 4.46.

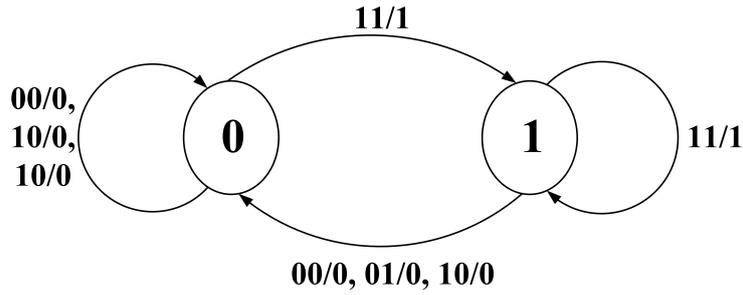


Figure 4.45: Mealey state diagram for the AND operation
 The states are as indicated, i.e 0 → *LOW*, 1 → *HIGH*

| Input-A | Input-B | Clock | Output |
|----------|----------|----------|----------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 |

Table 4.9: Functional table for AND cell

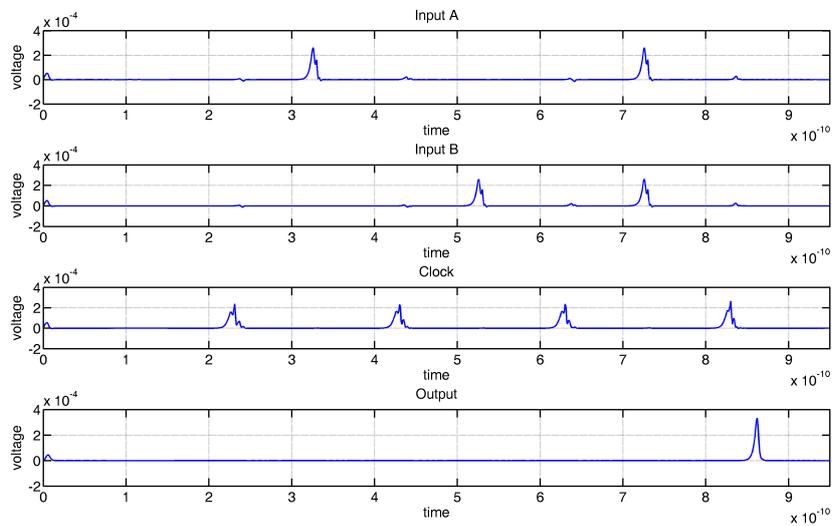


Figure 4.46: AND Cell simulation waveforms

Layouts for the AND cell are shown in Figs. 4.47 and 4.48. Like most IPHT cells, CUT cells are added to protect series junctions. The IPHT cell occupies and $300 \times 300 \mu\text{m}$ space while the Hypres cell covers a $200 \times 200 \mu\text{m}$ space.

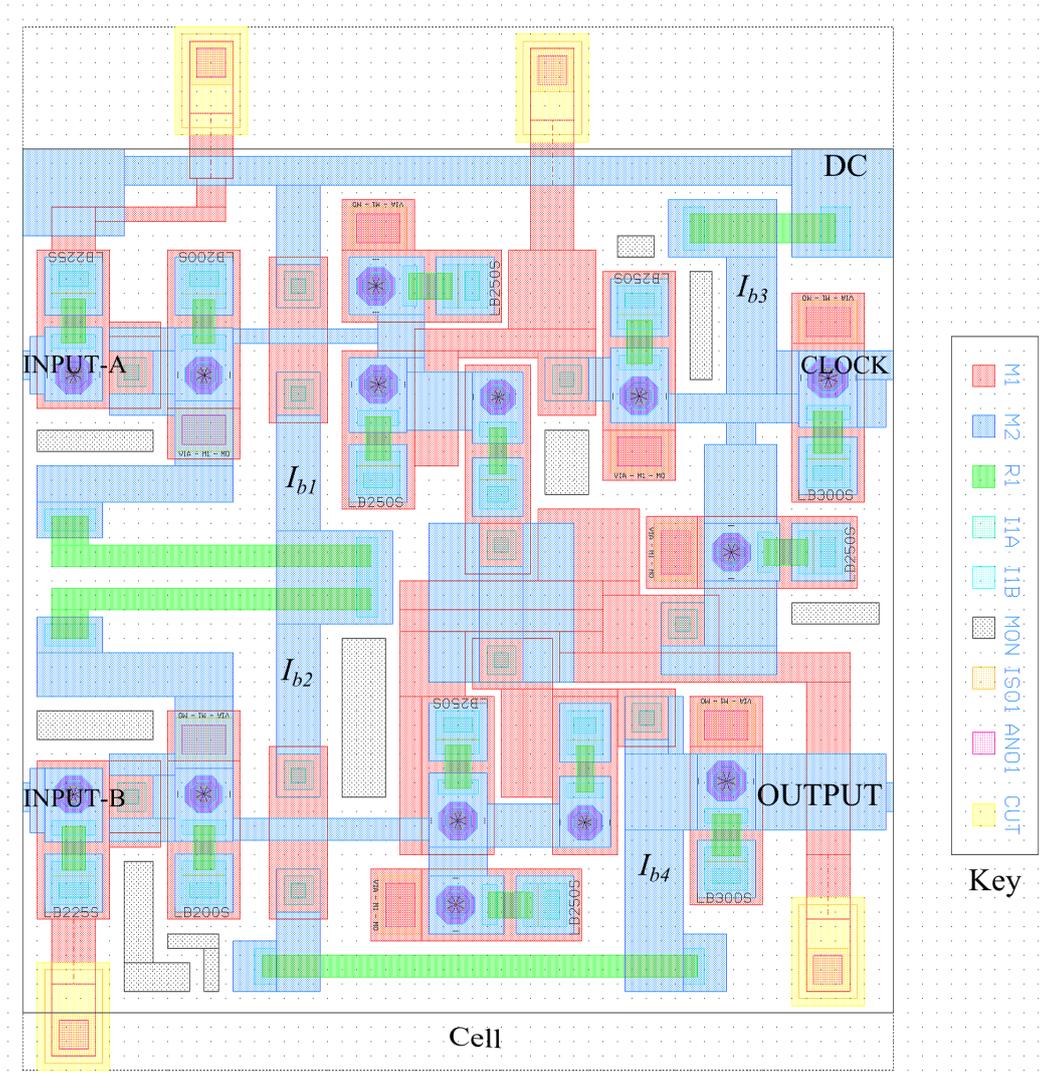


Figure 4.47: AND cell layout for IPHT - $300 \times 300 \mu\text{m}$

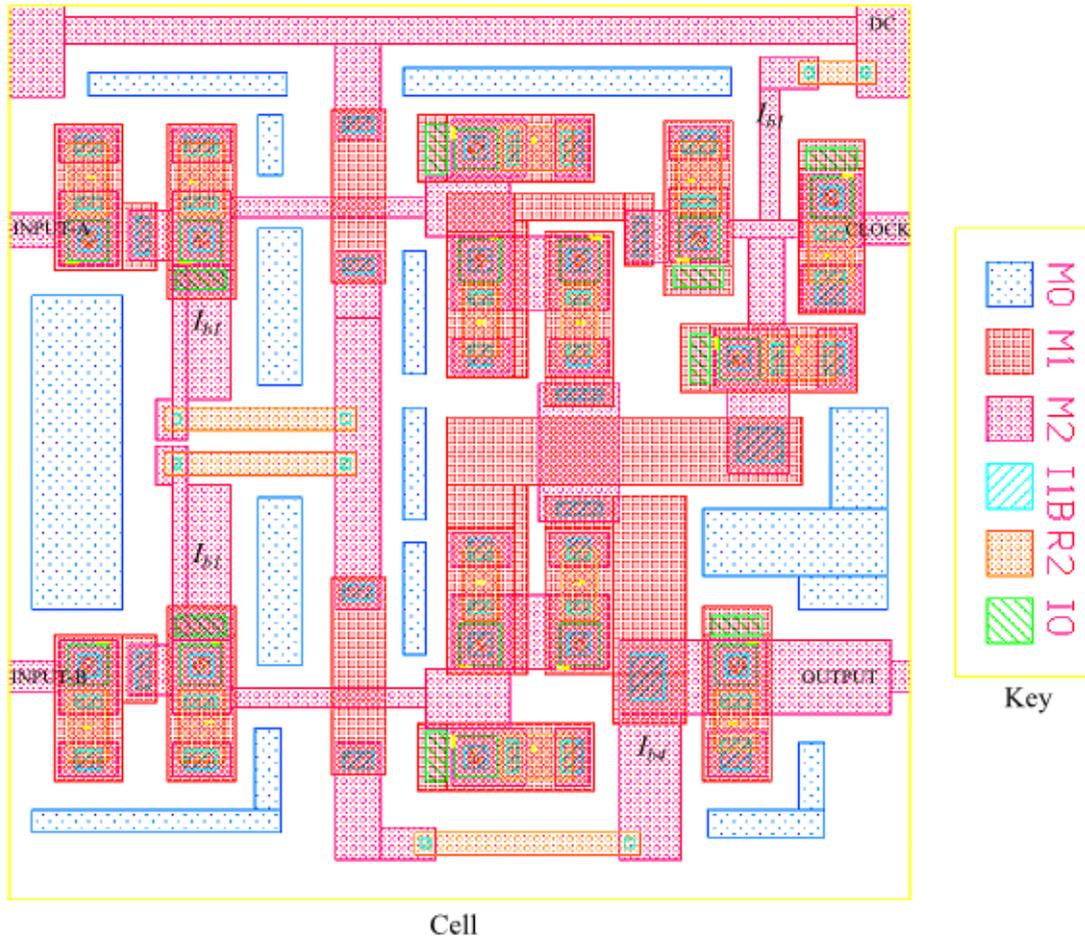


Figure 4.48: AND cell layout for Hypres - $200 \times 200 \mu\text{m}$

4.2.10 NAND Cell

The NAND cell is a direct inversion of the AND cell. It produces a HIGH output for all input combinations, except when they are both HIGH. In semiconductor electronics, NOR and NAND cells are known to be the simplest cells and they can be used to build other logic cells. It is, however, different in RSFQ circuits in that the NOR and NAND cells are quite complex. The NAND cell presented here has a count of 16 Josephson junctions.

The NAND cell, shown in Fig. 4.50, was designed with the NOT, Merger and Splitter cells in consideration. Taking into account the work done by DeMorgan presented in his theorems, the NAND operation can be synthesized as

$$Y = \overline{A.B} \quad (4.1)$$

where A and B are inputs and Y is the output.

A design based on (4.1) would result in a direct cascade of an AND and a NOT cell. This would require two clock signals that are properly synchronized. Such a design is thus undesirable. Using DeMorgan's Theorem, (4.1) becomes

$$Y = \overline{A} + \overline{B}. \quad (4.2)$$

(4.2) therefore results in a simpler design that requires only one clock signal. Two NOT cells follow each input and their outputs go through a modified Merger (shown as a plus enclosed in an ellipse). The design is illustrated in block form in Fig. 4.49.

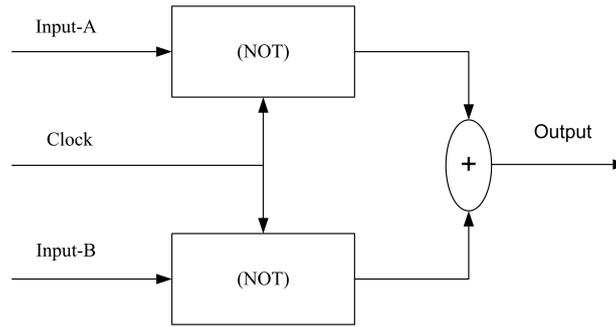


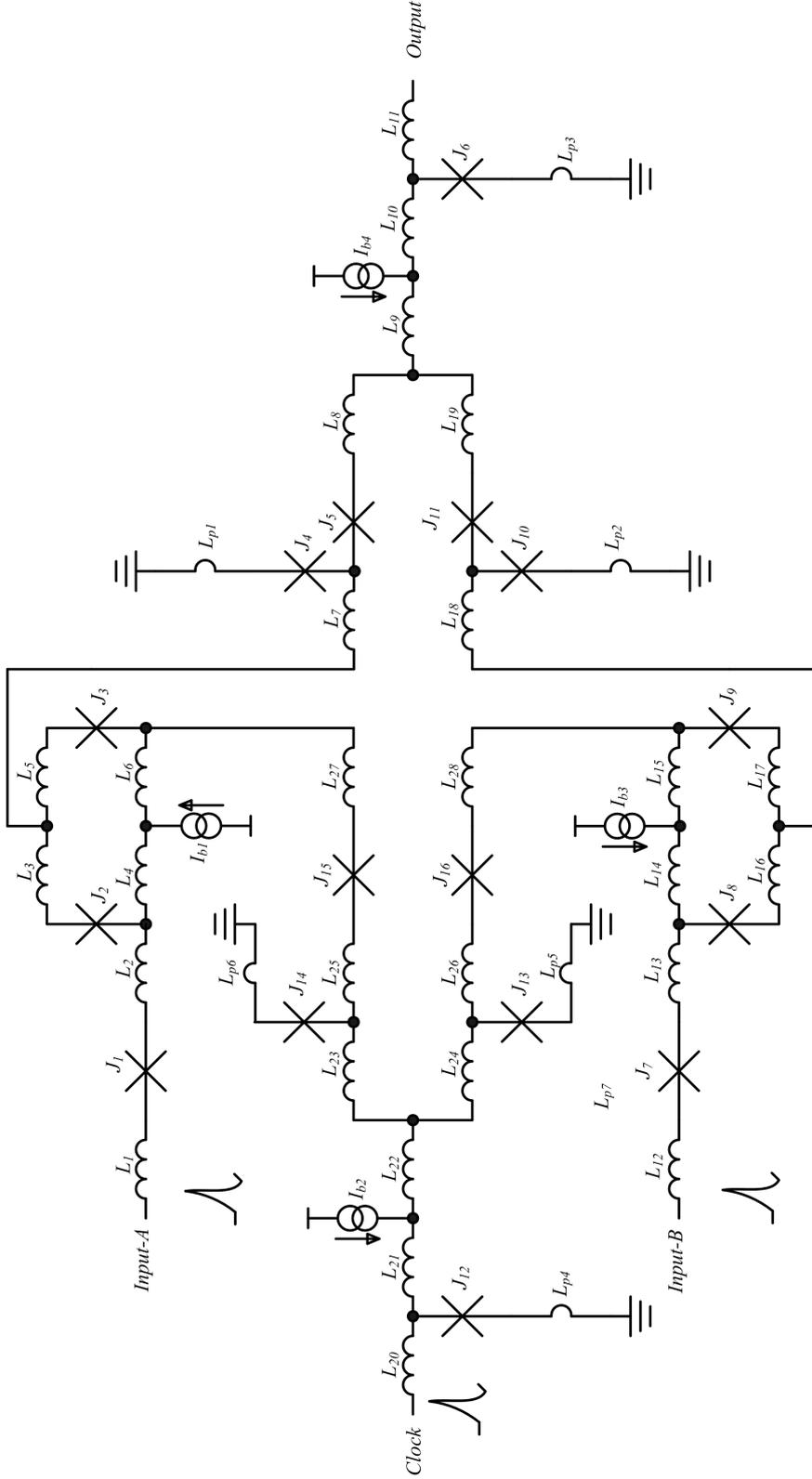
Figure 4.49: Conceptualized block design of the NAND cell

The approach depicted in Fig. 4.49 results in a circuit schematic for the NAND cell shown in Fig. 4.50. Two flux storage loops; Loop 1 - $J_2 - L_4 - L_6 - J_3 - L_5 - L_3$ and Loop 2 - $J_8 - L_{14} - L_{15} - J_9 - L_{17} - L_{16}$, provide temporary storage of the input SFQ pulses and they also provide bit inversion (Refer to the NOT cell operation).

The clock input is split through J_{12} , J_{13} and J_{14} , which form a Splitter (with all inductances included) to ensure that one clock signal is made available to both input channels at the same time. This ensures the synchronization of the two sub-circuits (the two loops).

An SFQ pulse at Input-A enters Loop 1 through J_2 which switches easily, as it is biased by I_{b1} . The large inductance in the loop (L_6) causes the SFQ pulse to be stored in the loop. The stored SFQ pulse and I_{b1} further bias J_3 even more and increases the switching probability of J_3 to 1 at the incoming clock pulse. The clock pulse therefore triggers a 2π leap in J_3 and the trapped SFQ is lost. This translates into no input pulse to the Merger section (at L_7) of the NAND cell and a LOW output is registered. An SFQ pulse applied at Input-B results in an identical operation.

However, if Input-A receives no SFQ pulse, the flux loop remains empty (i.e. no trapped flux) and an incoming clock pulse will be insufficient to switch ON J_3 and J_4 switches ON instead. The output now registers a HIGH. A HIGH output is registered regardless of the state at Input-B.


Figure 4.50: NAND Cell Schematic

Extracted Parameters:

IPHT: $J_1 = J_7 = 100\mu A$, $J_2 = J_8 = J_{15} = J_{16} = 150\mu A$, $J_3 = J_4 = J_9 = 175\mu A$, $J_{14} = J_{13} = J_{11} = 250\mu A$, $J_{10} = 200\mu A$ and $J_6 = 225\mu A$, $J_{12} = 225\mu A$, $L_1 = 888fH$, $L_2 = 1pH$, $L_3 = 836fH$, $L_4 = 200fH$, $L_5 = 536fH$, $L_6 = 6.2pH$, $L_7 = 2.04pH$, $L_8 = 1.47pH$, $L_9 = 624fH$, $L_{10} = 926fH$, $L_{11} = 1.65pH$, $L_{12} = 620fH$, $L_{13} = 1pH$, $L_{14} = 570fH$, $L_{15} = 6.65pH$, $L_{16} = 845fH$, $L_{17} = 366fH$, $L_{18} = 2.75pH$, $L_{19} = 1.48pH$, $L_{20} = 1.644pH$, $L_{21} = 1.81pH$, $L_{22} = 100fH$, $L_{23} = 1.84pH$, $L_{24} = 500fH$, $L_{25} = 600fH$, $L_{26} = 2.6pH$, $L_{27} = 2.6pH$, $L_{28} = 1.54pH$, $L_{29} = 379fH$, $L_{30} = 151fH$, $L_{31} = 187fH$, $L_{32} = 275fH$, $L_{33} = 336fH$, $L_{34} = 335fH$; *Bias Currents*: $I_{b1} = I_{b3} = 175.1\mu A$; $I_{b2} = 577.8\mu A$; and $I_{b4} = 144.4\mu A$

Hypres: $J_1 = J_7 = 100\mu A$, $J_2 = J_8 = J_{15} = J_{16} = 150\mu A$, $J_3 = J_4 = J_9 = 175\mu A$, $J_{14} = J_{13} = J_{11} = 250\mu A$, $J_{10} = 200\mu A$ and $J_6 = 225\mu A$, $L_1 = 476fH$, $L_2 = 1.0pH$, $L_3 = 1.08pH$, $L_4 = 677fH$, $L_5 = 789fH$, $L_6 = 6.01pH$, $L_7 = 1.7pH$, $L_8 = 900fH$, $L_9 = 492fH$, $L_{10} = 805fH$, $L_{11} = 1.825pH$, $L_{12} = 390fH$, $L_{13} = 1pH$, $L_{14} = 317fH$, $L_{15} = 6.08pH$, $L_{16} = 1.15pH$, $L_{17} = 270fH$, $L_{18} = 2.53pH$, $L_{19} = 884fH$, $L_{20} = 1pH$, $L_{21} = 1pH$, $L_{22} = 100fH$, $L_{23} = 774fH$, $L_{24} = 765fH$, $L_{25} = 677fH$, $L_{26} = 560fH$, $L_{27} = 2.6pH$, $L_{28} = 1.54pH$, $L_{29} = 260fH$, $L_{30} = 261fH$, $L_{31} = 194fH$, $L_{32} = 46fH$, $L_{33} = 47fH$; *Bias Currents*: $I_{b1} = I_{b3} = 175.1\mu A$; $I_{b2} = 577.8\mu A$; and $I_{b4} = 144.4\mu A$

Junctions J_{15} and J_{16} protect the clock splitter output junctions J_{13} and J_{14} by switching ON whenever backward SFQ pulse try to enter the splitter. Without these junctions, it was observed that J_{13} and J_{14} switched ON unnecessarily due to backward pulses thereby causing the circuit to either drop in operating margins or completely malfunction.

The state transitions that occur in the NAND cell are shown in Fig. 4.51 and its operation is summarized in the function table shown in Table 4.10.

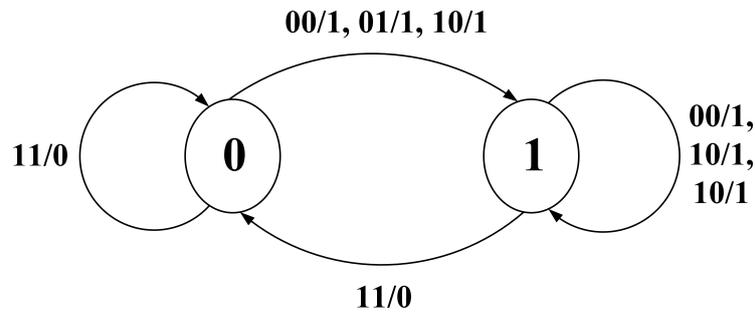


Figure 4.51: Mealey finite state machine for the NAND cell

| Input-A | Input-B | Clock | Output |
|----------|----------|----------|----------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 |

Table 4.10: Functional Table for the NAND Cell

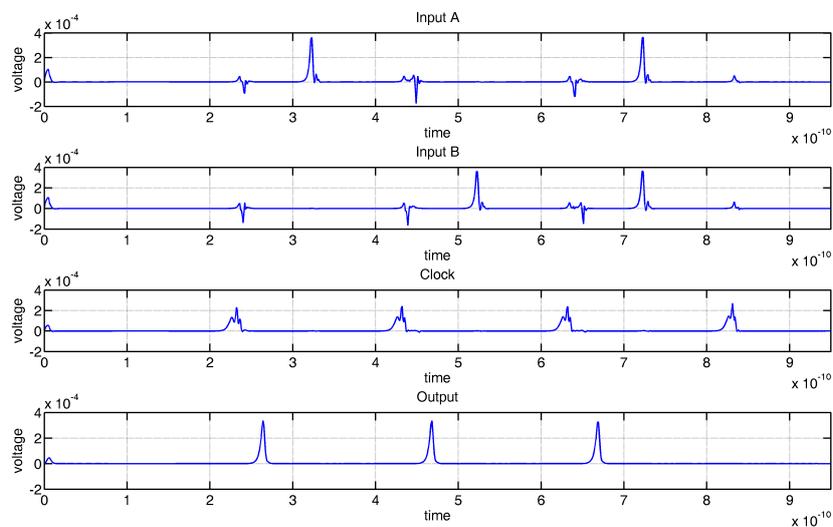


Figure 4.52: NAND Simulation waveforms

The NAND cell was simulated in Niopulse and waveforms are shown in Fig. 4.52. It can be observed that the NAND produces SFQ pulses for all combinations except, when both inputs are HIGH. The NAND cell is a large cell and layouts occupied spaces of $300 \times 300 \mu\text{m}$ and $200 \times 200 \mu\text{m}$ for IPHT and Hypres respectively. The layouts are shown in Figs. 4.53 and 4.54.

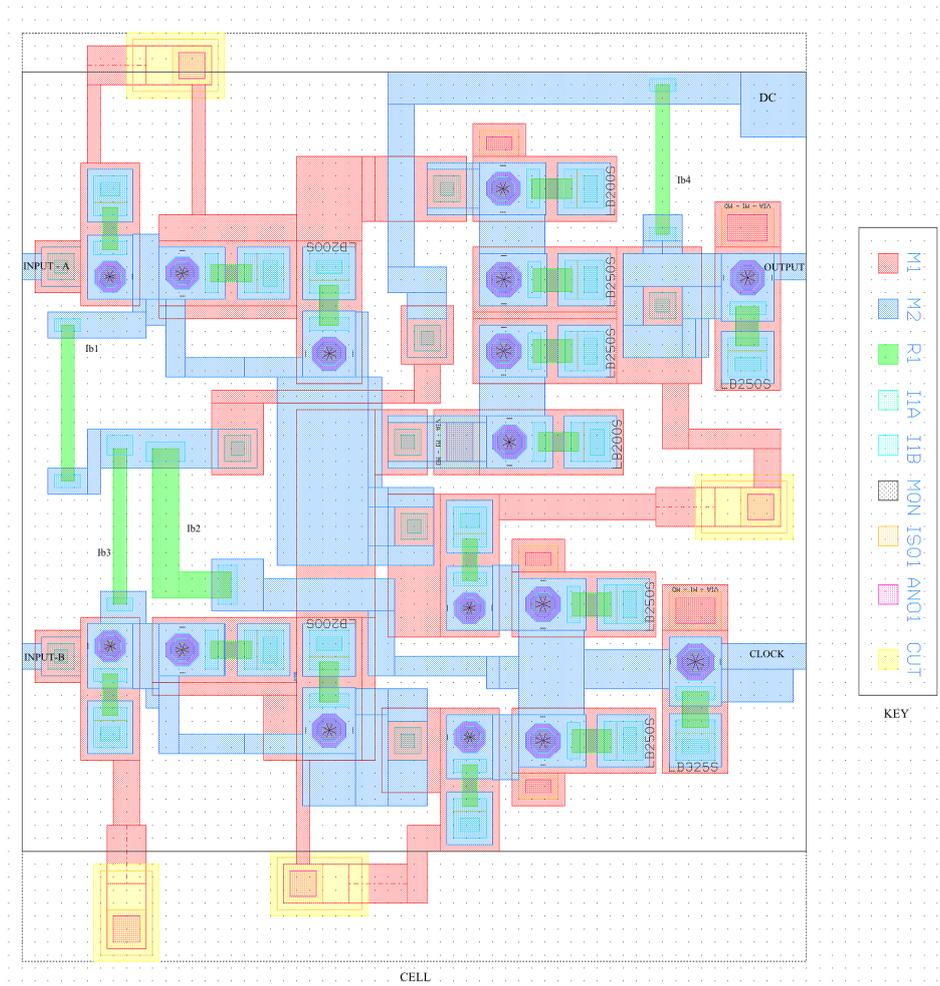


Figure 4.53: NAND Cell layout for the IPHT process - $300 \times 300 \mu\text{m}$

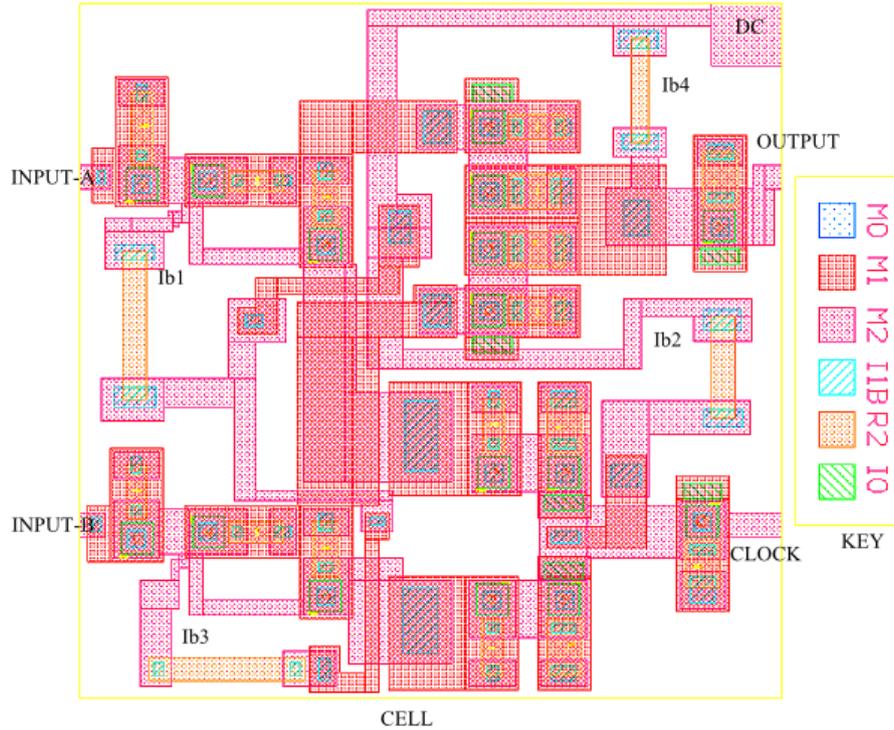


Figure 4.54: NAND Cell layout for the Hypres process - $200 \times 200 \mu m$

4.2.11 XOR Cell

An Exclusive-OR (XOR) cell produces a HIGH output if its two inputs have different states. It effectively performs the Modulo-2 addition. An XOR is used to check digital system bit consistency, thereby detecting bit errors. An approach for determining bit error rates in superconductor circuits, using XOR gates, was demonstrated by S. Kim [42].

The RSFQ XOR cell is shown in Fig. 4.55 and at the time of writing it is the standard cell schematic. The circuit in the figure was modified to improve clock signal drive by including the clock input half JTL and adding isolation with the output half JTL. The cell has a total of 11 Josephson junctions and 3 bias current inputs.

The cell is built around two flux storing loops, *Loop 1* - $J_2 - L_2 - J_3 - L_3 - L_7 - J_7 - J_{10}$ and *Loop 2* - $J_5 - L_5 - J_6 - L_4 - L_7 - J_7 - J_{10}$. Current I_{b1} biases J_2 and J_5 and maintains the two loops by providing circulation currents.

A SFQ pulse at Input A switches J_2 and it then propagates into *Loop 1*. The SFQ pulse remains in the loop until a clock pulse clears it. A similar behaviour is demonstrated when a SFQ pulse at input B is propagated into *Loop 2* through the switching of J_5 . If both inputs have no pulses, then the loops' conditions remain unchanged. An applied clock pulse does not change anything, as J_{10} can not switch. However, if Input - A or

B receives an SFQ pulse then, either of the two loops has a trapped SFQ pulse, thereby providing enough bias current for J_{10} . It then becomes much easier for J_{10} to switch at the incoming clock pulse. This propagates a SFQ pulse to the output and a HIGH output is registered.

An unstable condition occurs when both inputs are HIGH. This unstable state is shown in the state diagram as *state 11* (Fig. 4.56). The current in both loops is quite large and enough to trigger the switching of J_{10} (this would result in an invalid XOR output). Instead, J_7 is made to switch in this condition. For this to work the design is such that $J_7 < J_{10}$ in terms of junction area and hence critical current. When J_7 switches, both stored pulses are lost and a clock pulse alone can not switch ON J_{10} . A LOW output is therefore registered.

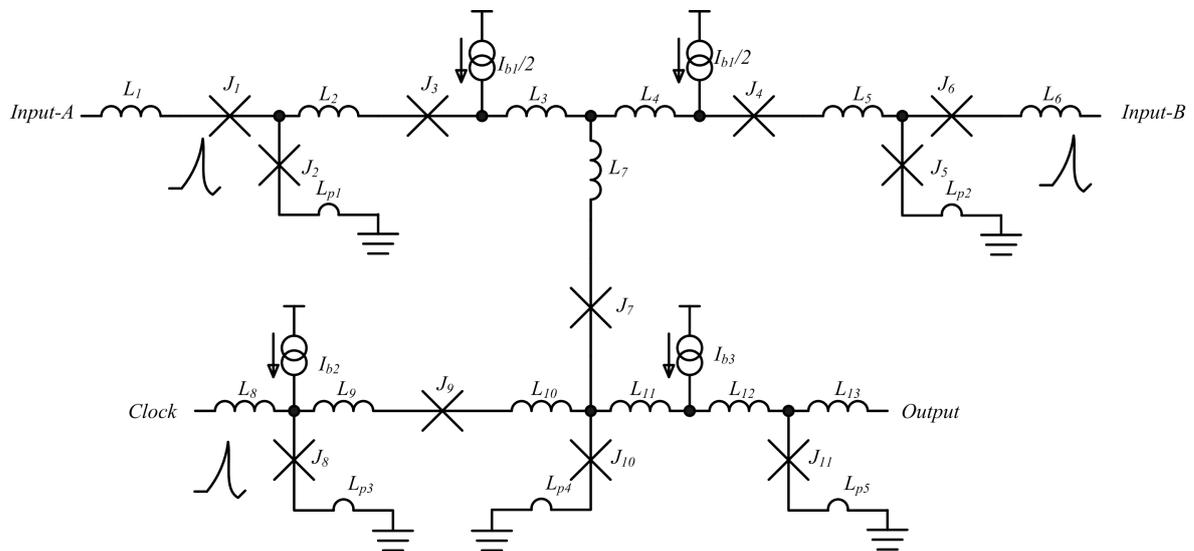


Figure 4.55: XOR cell schematic

It is a good design tenet to protect the output junction in a comparator arrangement. This is the case to protect the junction from being switched ON by external backward currents. In Fig. 4.55, L_{11} is made large to meet this design criteria. In this case, I_{b3} has little effect on J_{10} . Further isolation is provided by the output half JTTL.

The operation of the XOR cell is summarized in the Moore diagram shown in Fig 4.56 and the function table in Table 4.11, followed by simulation results in Fig. 4.57 which were obtained in *Niopulse*. It can be observed from the results that when both inputs are HIGH, J_7 switches and the output goes LOW. The Moore diagram for the XOR cell in Fig. 4.56 was chosen to have four states in order to show the unstable state more effectively.

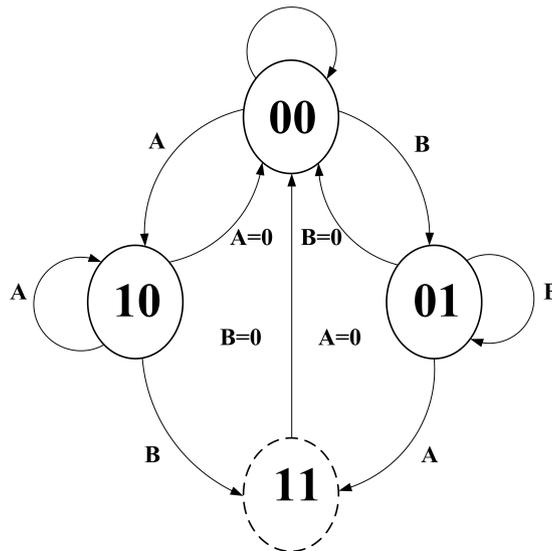


Figure 4.56: Moore state diagram for the XOR
 State 00 \rightarrow *LOW*, 01, 10 \rightarrow *HIGH*. State 11 is unstable and is corrected by J_7 (see the schematic) and it transitions into state 00 all the time [31].

| Input-A | Input-B | Clock | Output |
|----------|----------|----------|----------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 |

Table 4.11: XOR Functional Table

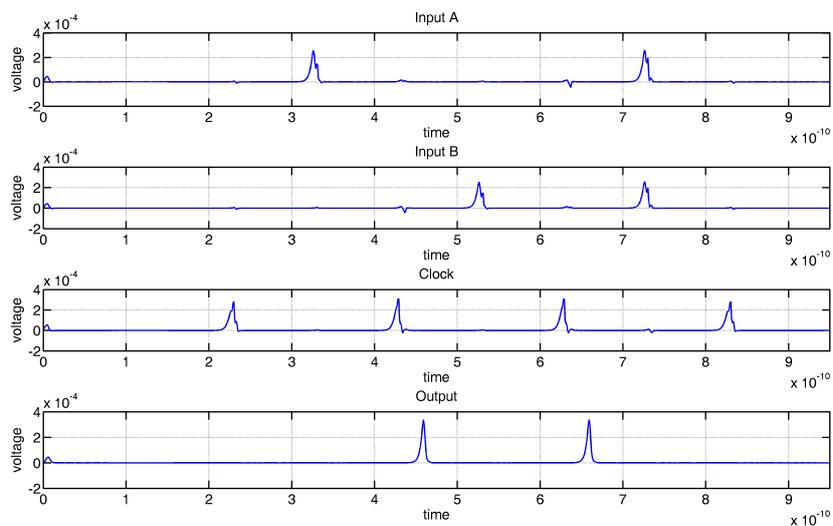


Figure 4.57: Simulation waveforms for the XOR cell

IPHT and Hypres Layouts for the XOR are shown in Figs. 4.58 and 4.59.

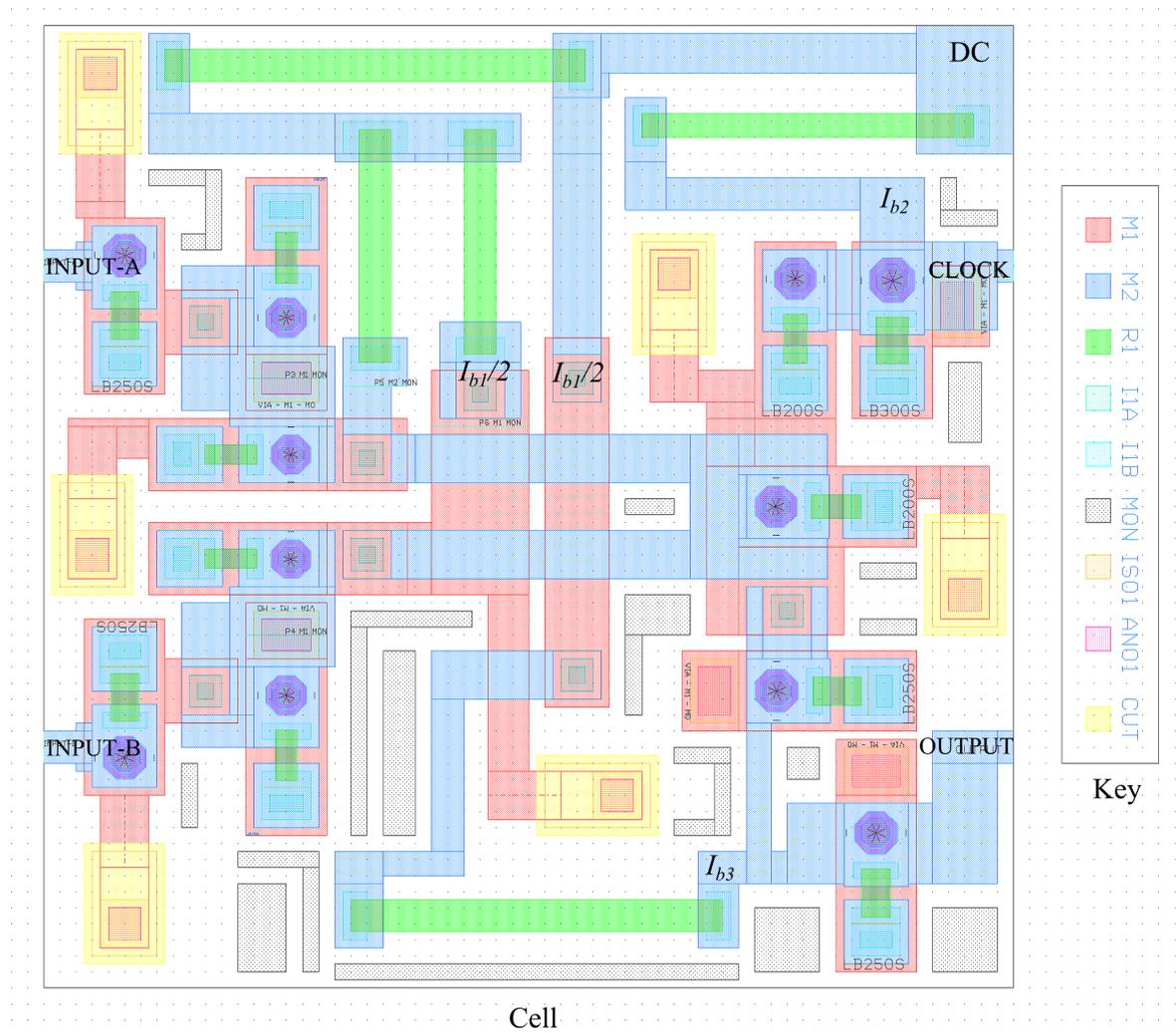


Figure 4.58: XOR cell layout for the IPHT process - $300 \times 300 \mu\text{m}$

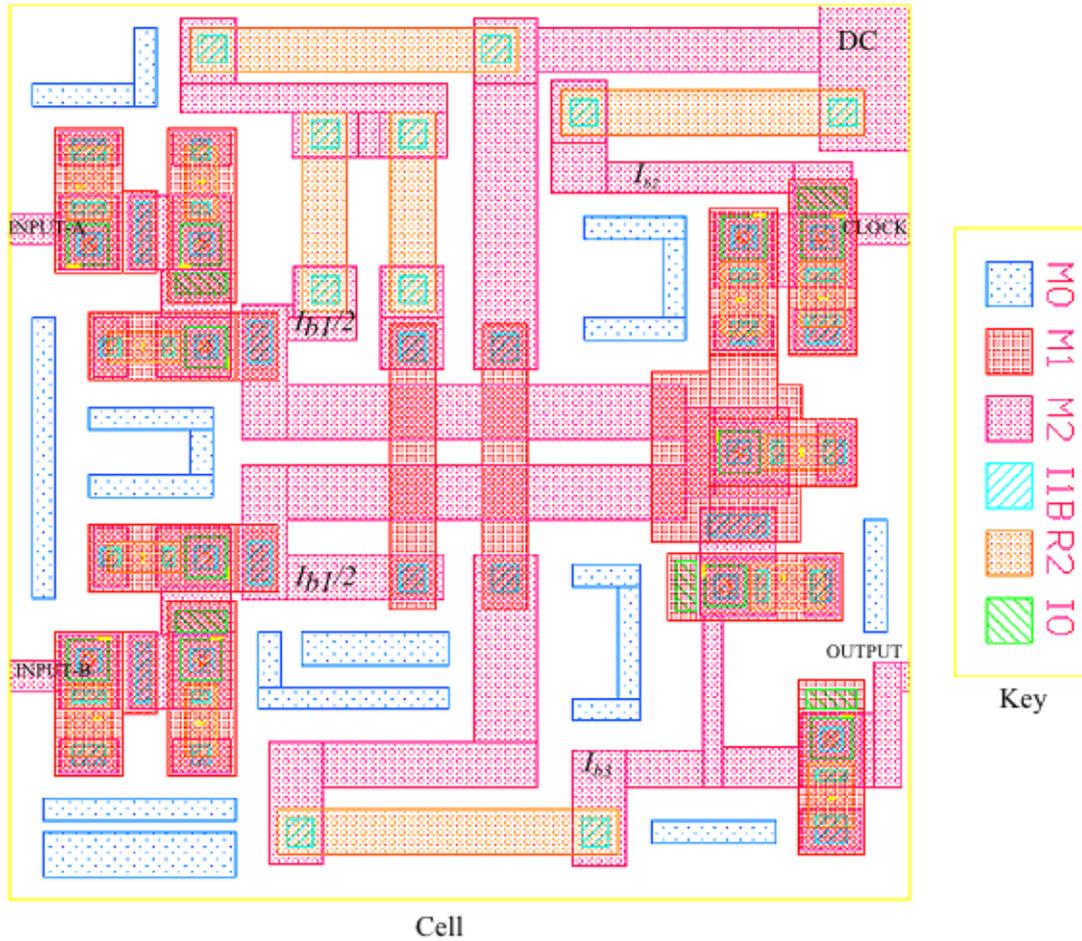


Figure 4.59: XOR cell layout for the Hypres process - $200 \times 200 \mu\text{m}$

4.2.12 XNOR Cell

The XNOR is the third new cell. It was designed with close attention to the operation of the XOR operation. It produces a HIGH output when both inputs have equal states and a LOW output when the inputs have different states. The designed XNOR is shown in schematic form in Fig. 4.60.

The XNOR cell has three functional elements: an XOR ($L_1 - J_1 - J_2 - L_3 - L_4 - J_4 - J_3 - L_2 - L_5 - J_5 - J_6 - J_7$), a modified clock Splitter and a flux loop ($J_9 - L_8 - L_{10} - J_{10} - L_9$). In the XOR section, the operation is such that when either of the inputs has an SFQ, it is propagated into one of the loops. The large inductance L_3 and L_4 ensure that the flux remains trapped in one of the loops (see XOR operation). The trapped flux produces enough current for proper biasing of J_6 , such that it switches easily at the arrival of a clock pulse through J_7 . The XOR output is LOW when both inputs are LOW, because the additional current is unavailable to bias J_6 . An unstable condition arises when both inputs are HIGH. There would be more than enough current to trigger the switching of J_6 , but this would mean departing from the normal XOR operation

| Input-A | Input-B | Clock | Output |
|----------|----------|----------|----------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 |

Table 4.12: XNOR Functional Table

and in this case J_5 switches before J_6 can. This clears the trapped SFQ pulses and the XOR output registers a LOW. In summary for this XOR element $00 \rightarrow 0$, $11 \rightarrow 0$ and $01 \rightarrow 1$, $10 \rightarrow 1$. For the XNOR operation this trend needs to be inverted as depicted in the function table, Table 4.12.

The XNOR operation is performed by the flux loop which traps the SFQ pulses from the XOR sub-circuit. The XOR outputs enter the flux loop through the switching of J_9 and remains there until a clock pulses arrives to clear them. The clock pulses that control the flux loop are delayed through the JTL ($J_{14} - L_{18} - L_{19} - J_{15} - L_{20}$) to ensure synchronization. Inductance L_{20} is made larger to reduce the loop currents, otherwise the circuit malfunctions. The flux loop, together with the delayed clock pulse, perform the inversion of the XOR outputs. As a result, the output produced is that of an XNOR cell. Table 4.12 summaries this XNOR operation with emphasis on the combinations that produce a HIGH output.

The simulation results for the XNOR cell are shown in Fig. 4.61. The simulation results confirm the XNOR operation.

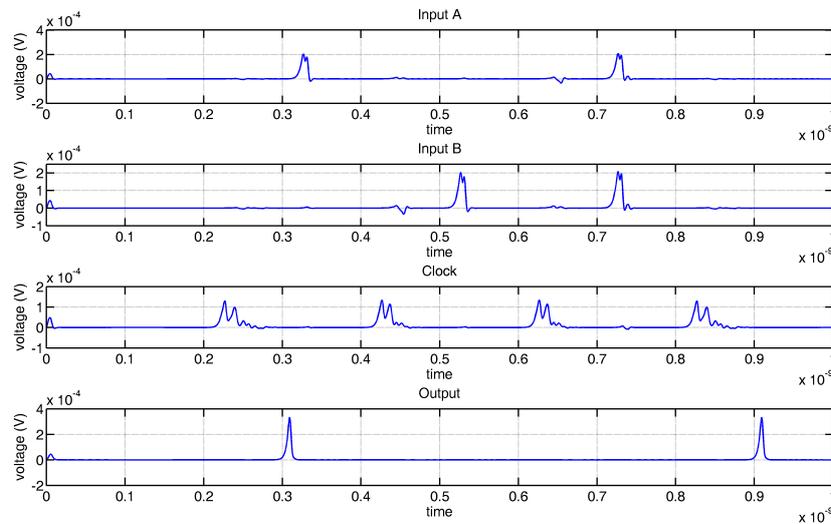


Figure 4.61: simulation results for the XNOR

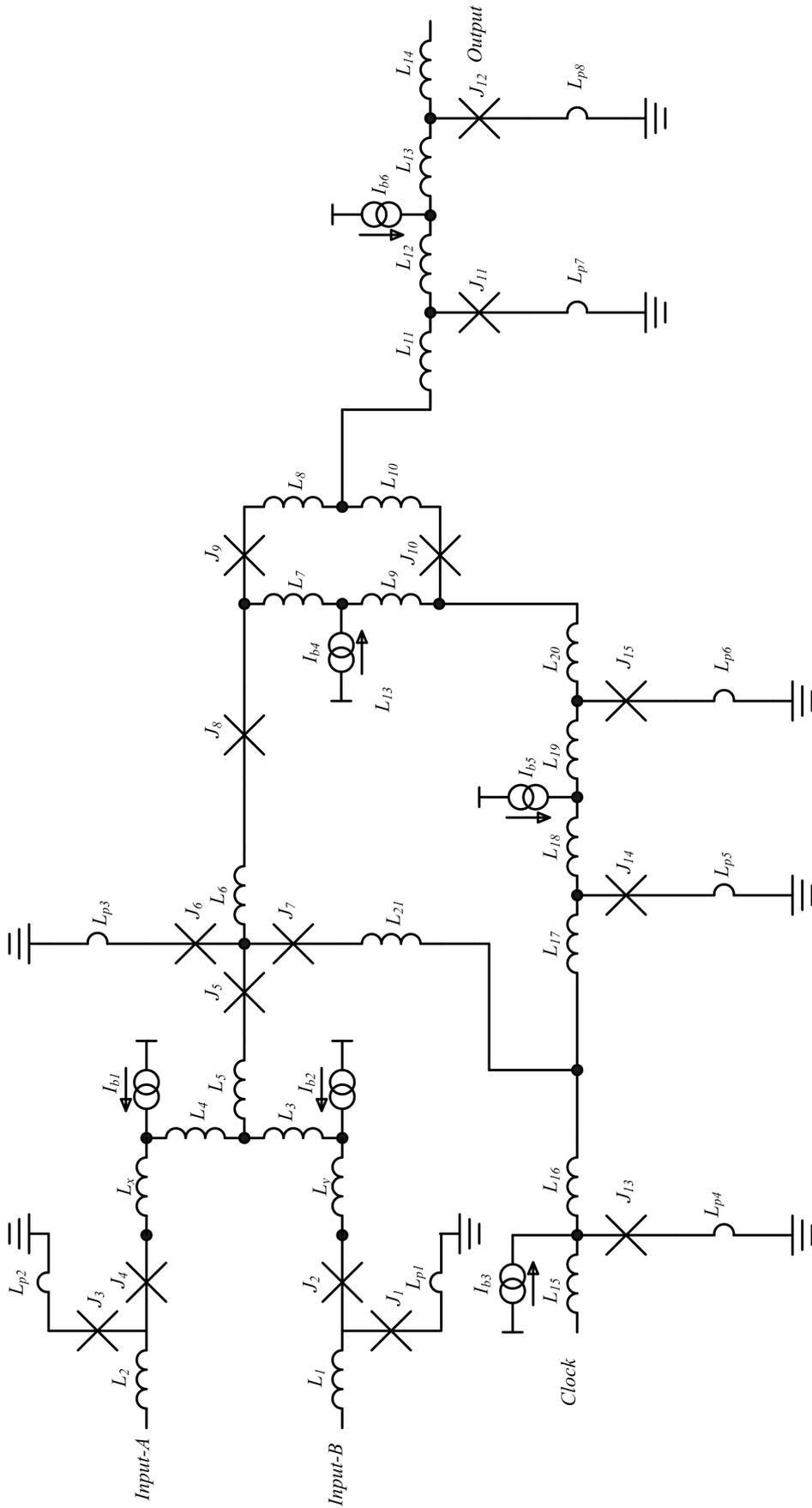


Figure 4.60: XNOR cell schematic

Extracted Parameters:

IPHT: $J_1 = J_3 = J_7 = 200\mu A$, $J_5 = J_8 = 175\mu A$, $J_2 = J_4 = J_9 = J_{10} = J_{11} = 150\mu A$, $J_{12} = J_{14} = J_{15} = 225\mu A$, $J_{13} = 325\mu A$ and $J_6 = 300\mu A$, $L_1 = 1.3pH$, $L_2 = 1.3pH$, $L_3 = 6.4pH$, $L_4 = 6.4pH$, $L_5 = 330fH$, $L_6 = 1.02pH$, $L_7 = 310fH$, $L_8 = 1.02pH$, $L_9 = 6.52pH$, $L_{10} = 133fH$, $L_{11} = 2.04pH$, $L_{12} = 1.26pH$, $L_{13} = 1.61pH$, $L_{14} = 2.07pH$, $L_{15} = 1.42pH$, $L_{16} = 820fH$, $L_{17} = 3.28pH$, $L_{18} = 2.01pH$, $L_{19} = 2.01pH$, $L_{20} = 650fH$, $L_{21} = 650fH$, $L_x = L_y = 1.2pH$, $L_{p1} = 370fH$, $L_{p2} = 372fH$, $L_{p3} = 600fH$, $L_{p4} = 184fH$, $L_{p5} = 230fH$, $L_{p6} = 230fH$, $L_{p7} = 260fH$, $L_{p8} = 262pH$; Bias Currents: $I_{b1} = I_{b2} = 140.5\mu A$; $I_{b3} = 260\mu A$, $I_{b4} = 288.9\mu A$, $I_{b5} = 130\mu A$ and $I_{b6} = 188.4\mu A$

Hypres: $J_1 = J_3 = J_7 = 200\mu A$, $J_5 = J_8 = 175\mu A$, $J_2 = J_4 = J_9 = J_{10} = J_{11} = 150\mu A$, $J_{12} = J_{14} = J_{15} = 225\mu A$, $J_{13} = 325\mu A$ and $J_6 = 325\mu A$, $L_1 = 1pH$, $L_2 = 1pH$, $L_3 = 6.33pH$, $L_4 = 6.24pH$, $L_5 = 210fH$, $L_6 = 966fH$, $L_7 = 292fH$, $L_8 = 1.12pH$, $L_9 = 6.4pH$, $L_{10} = 133fH$, $L_{11} = 2.01pH$, $L_{12} = 1.08pH$, $L_{13} = 1.45pH$, $L_{14} = 2.11pH$, $L_{15} = 1.35pH$, $L_{16} = 1.02pH$, $L_{17} = 3.68pH$, $L_{18} = 1.6pH$, $L_{19} = 21.6pH$, $L_{20} = 6.02pH$, $L_{21} = 520fH$, $L_x = L_y = 1.04pH$; $L_{p1} = 265fH$, $L_{p2} = 251fH$, $L_{p3} = 451fH$, $L_{p4} = 153fH$, $L_{p5} = 45fH$, $L_{p6} = 45fH$, $L_{p7} = 162fH$, $L_{p8} = 157pH$; Bias Currents: $I_{b1} = I_{b2} = 140.5\mu A$; $I_{b3} = 260\mu A$, $I_{b4} = 288.9\mu A$, $I_{b5} = 130\mu A$ and $I_{b6} = 188.4\mu A$

The XNOR cell had to go through several stages of design to try and get a circuit that had good functionality and wider bias margins. It is a very sensitive circuit, in that variations in inductance and Josephson junction critical currents ($> \pm 40\%$ and $> \pm 20\%$ in that order), may cause the circuit to malfunction. As such, the layouts for the XNOR cell had to be done with the highest accuracy to keep parameter values close to the initial design values. Layout of cells brings with it parasitics which require to be included in final and optimized designs. As a result, some Josephson junction critical currents had to be altered to reflect the changes brought about by the parasitics. The biggest challenge in the layout design was to keep L_6 and L_{21} to within $1pH$.

The XNOR cell was laid out on a space of $450 \times 300\mu m$ (IPHT) and $300 \times 200\mu m$ (Hypres). This makes the XNOR cell the largest cell in the library. With 15 Josephson junctions, the XNOR cell could have been laid out on $300 \times 300\mu m$ (IPHT) and $200 \times 200\mu m$ (Hypres) spaces but due to the large number of bias resistors (6) and 4 larger inductors (each $\sim 6pH$), such spaces were inadequate.

The layouts for XNOR are shown in Figs. 4.62 and 4.63 for the two processes. All extracted parameters are provided alongside the schematic in Fig. 4.60.

Table 4.13 at the end of this chapter gives a summary and a quick reference on the attributes of the cells presented in this thesis. It shows the cell space, bias current margins, cell delays and total bias current needed to properly test the cells.

4.2.13 DC-SFQ Converter Cell

The function of a DC-SFQ cell is to provide a more accurate SFQ pulse when it is excited with a slow rising DC current. The DC-SFQ circuit schematic is shown in Fig. 4.64. Its operation was presented by Kaplumenko V.K. *et al.*[43] and available in the IPHT and SUNY cell libraries [30, 31].

Junctions J_1 and J_2 , with inductor L_1 , form a superconducting loop and they act as a single junction interferometer (SQUID). A slowly rising DC current applied at the input will trigger J_2 if it becomes larger than the junction's critical current. The switching of J_2 produces an SFQ pulse that quickly propagates to the output and a negative SFQ pulse (anti-flux [31]) which remains trapped in the interferometer loop. The anti-flux reduces the current in the SQUID loop by causing a negative current ($\frac{\Phi_0}{L_1}$) to flow through L_1 to ground. The current then falls below the critical value of J_2 and the superconducting state of the loop is restored. One SFQ is therefore produced.

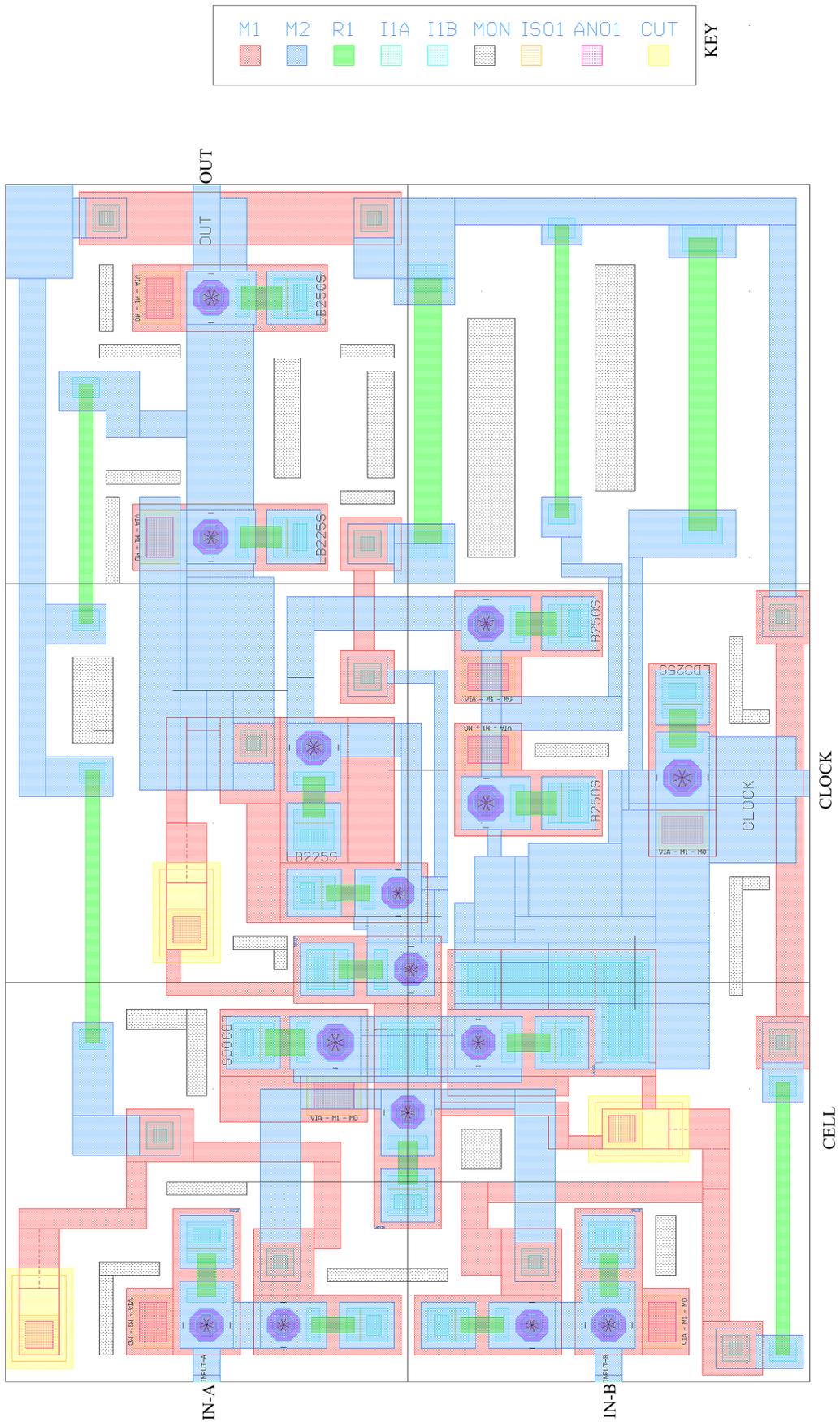


Figure 4.62: XNOR cell Layout for the IPHT process - $450 \times 300 \mu\text{m}$

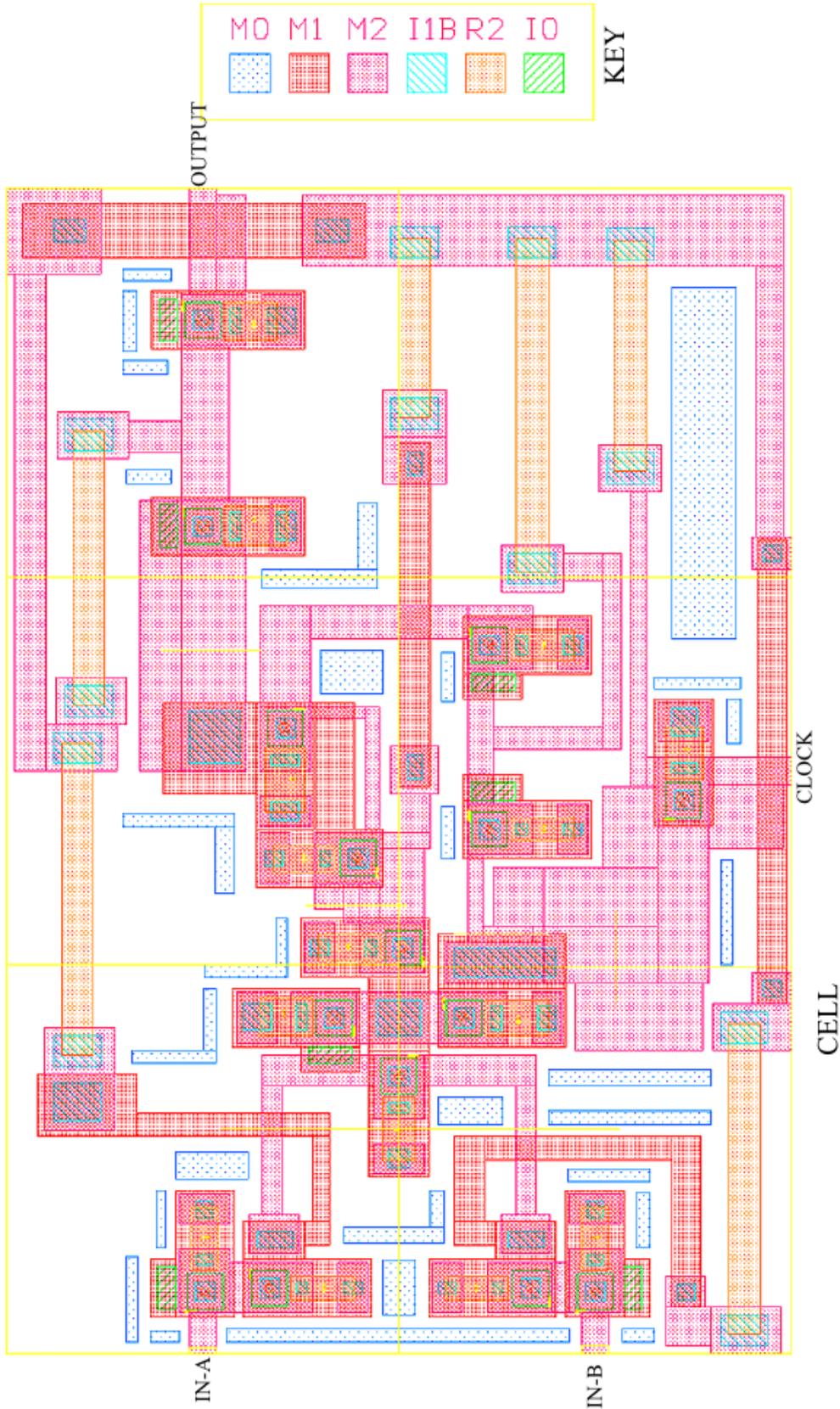


Figure 4.63: XNOR cell Layout for the Hypres process - $300 \times 200 \mu m$

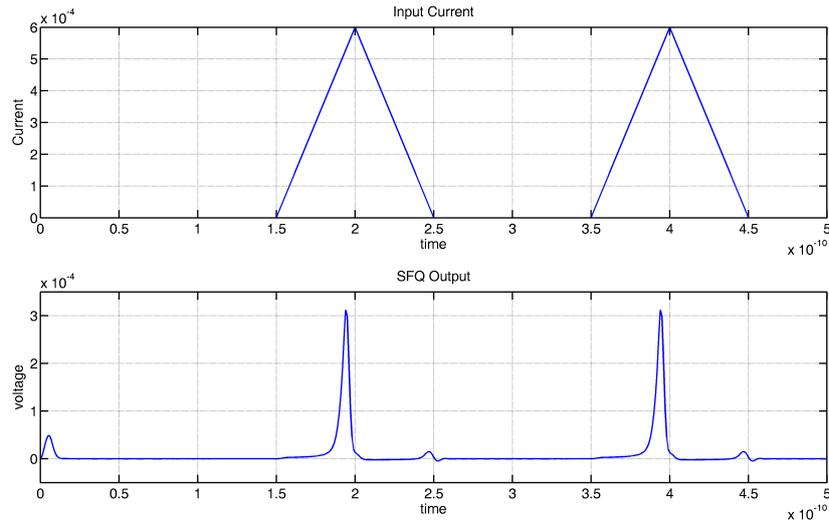


Figure 4.65: Simulation Waveforms for the DC-SFQ cell

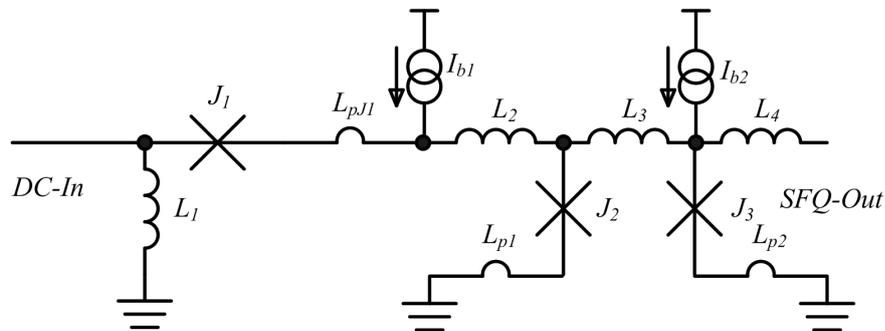


Figure 4.64: DC-SFQ Schematic

Extracted Parameters:

IPHT: $J_1 = 225\mu A$, $J_2 = 225\mu A$, $J_3 = 250\mu A$, $L_1 = 3.904$, $L_2 = 1.126pH$, $L_3 = 4.484pH$, $L_4 = 2.080pH$, $L_{p1} = 198fH$, $L_{p2} = 110fH$, $L_{pJ1} = 604fH$, Bias Currents: $I_{b1} = 275\mu A$, $I_{b2} = 175\mu A$.

Hypres extracted values are within $\pm 5\%$ of the IPHT values.

A decrease in the applied current only results in J_1 flipping and no SFQ pulse is produced. The waveforms in Fig. 4.65 illustrate the increasing input current and the output SFQ pulses. The output half JTL built around J_3 offers current amplification and possible matching to the output load.

Layouts for the DC-SFQ Cell are shown in Figs. 4.66 and 4.67. The IPHT cell layout is a directly adapted from the IPHT cell library.

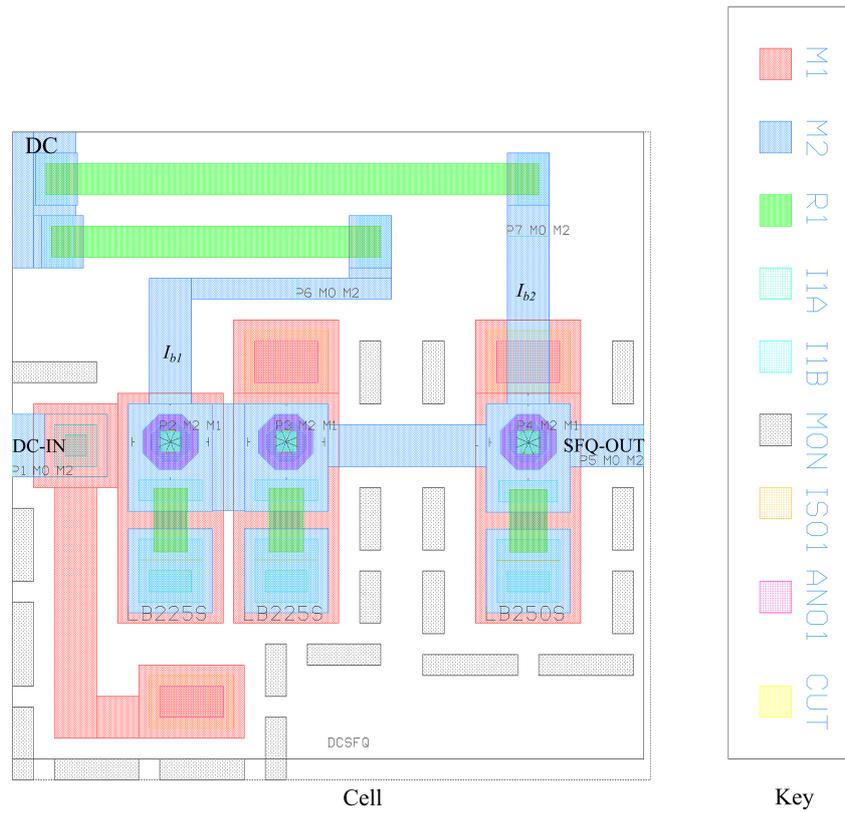


Figure 4.66: DC-SFQ cell Layout for the IPHT process - $150 \times 150\mu m$

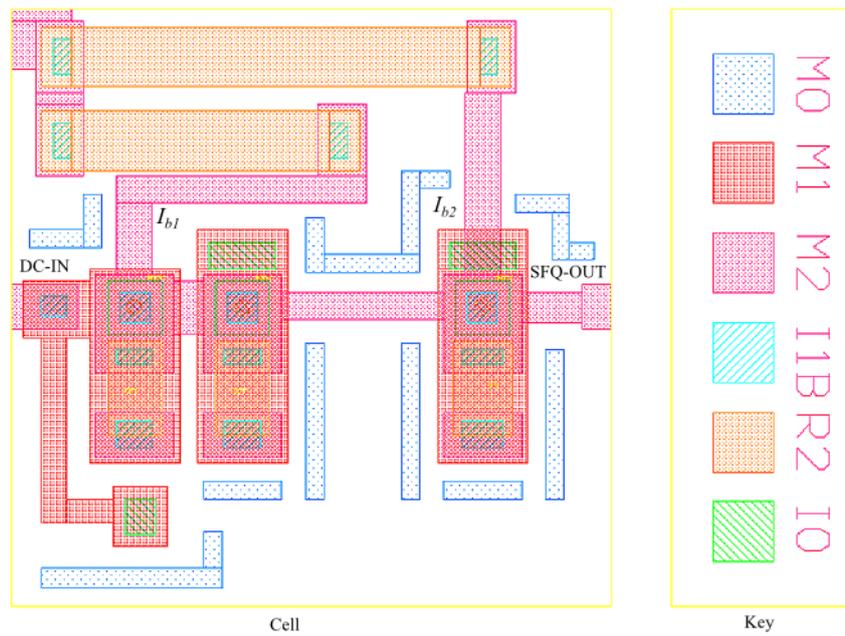


Figure 4.67: DC-SFQ cell Layout for the Hypres process - $100 \times 100\mu m$

4.2.14 SFQ-DC Converter Cell

The SFQ-DC cell is used to transform a series of SFQ pulses into a DC voltage, thereby providing the much needed interface to room temperature electronics. The SFQ-DC cell consists of a TFF coupled to a circuit that monitors the internal state of the TFF. The operation of the SFQ-DC cell is hereby described with reference to its schematic shown in Fig. 4.68.

An input SFQ pulse enters J_1 , which switches ON and propagates the pulse into the TFF loops and changes the state of the SQUID loops [43]. At first J_5 switches, because the bias current I_{b2} increases the phase change in J_5 , thereby increasing its flipping probability. The SFQ pulse produced by J_5 is distributed and keeps circulating in the loop and causes J_5 and J_4 to switch alternately. The pulse remains in the loop, because of the large quantising inductance L_5 and L_6 .

Junctions J_6 and J_7 form a directly coupled interferometer that continuously monitors the internal state of the TFF loops. The result being that the disturbances in the TFF loop is picked up as a dense series of pulses. The pulses are filtered and a fairly steady DC voltage is recorded at the output. The RL combination of R_1 and L_7 provides the filtering.

A second SFQ pulse at the input will switch J_2 first, before J_5 because J_2 is continuously biased by current from the stored SFQ pulse. This results in the loss of both the trapped SFQ pulse and the next pulse. The loop becomes superconducting and so does the monitoring interferometer ($L_8 - J_6 - J_7$) and 0V DC output is registered [31].

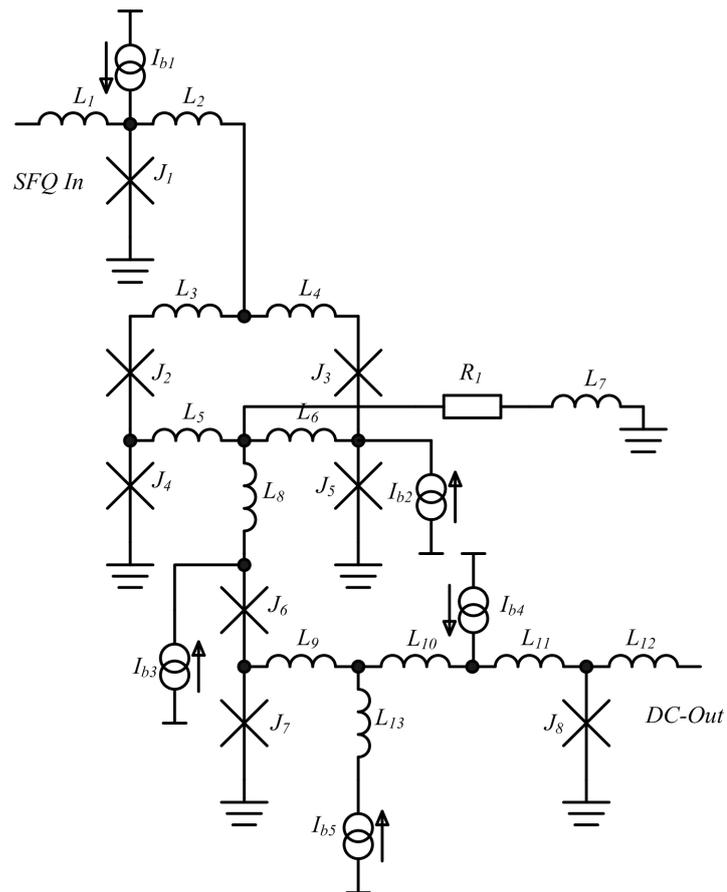


Figure 4.68: SFQ-DC cell schematic

Simulation results for the converter are shown in Fig. 4.69. I_{b5} provides tuning of the output voltage by altering the phase changes in J_7 . This current can either be positive or negative as dictated by the required operating point. Extracted parameters for the SFQ-DC cell are not provided because the cells are directly from the IPHT [30]. The DC-SFQ and SFQ-DC cells were tested at University of Ilmenau and incorporated into this library as working cells.

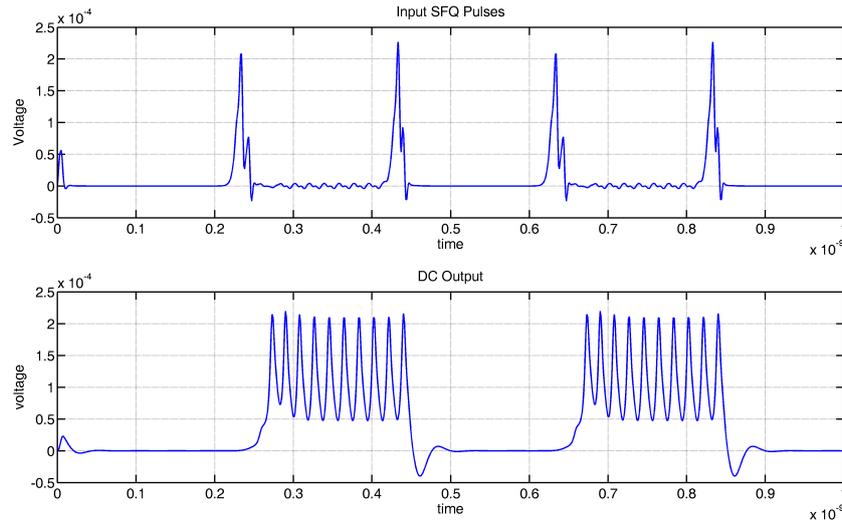


Figure 4.69: Simulation results of the IPHT Version of the SFQ-DC Cell. Note that the average voltage (DC) is almost half of the Characteristic voltage for the IPHT process - i.e. $250\mu V$.

Layouts done for the two fabrication process are shown in Fig. 4.70 and Fig. 4.71. It can be noted that the Hypres version of the SFQ-DC has more junctions (10) while the IPHT design has 8. The IPHT layout is from the Ilmenau library [30] (more modern), while the Hypres layout is from an older Ilmenau schematic.

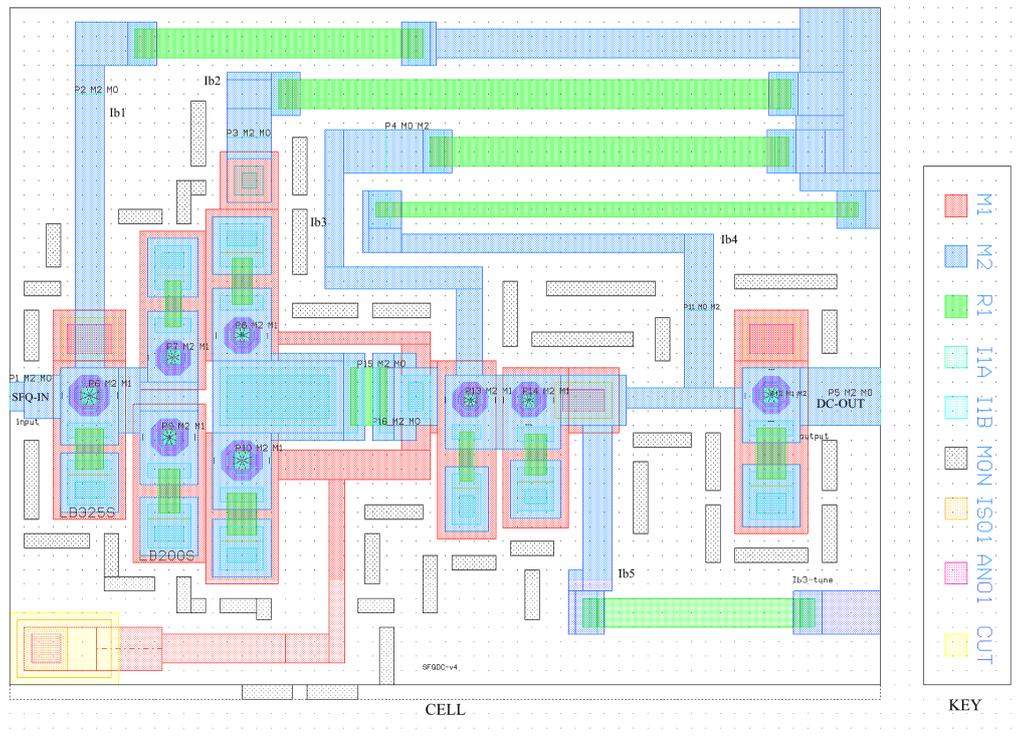


Figure 4.70: SFQ-DC layout for the IPHT process

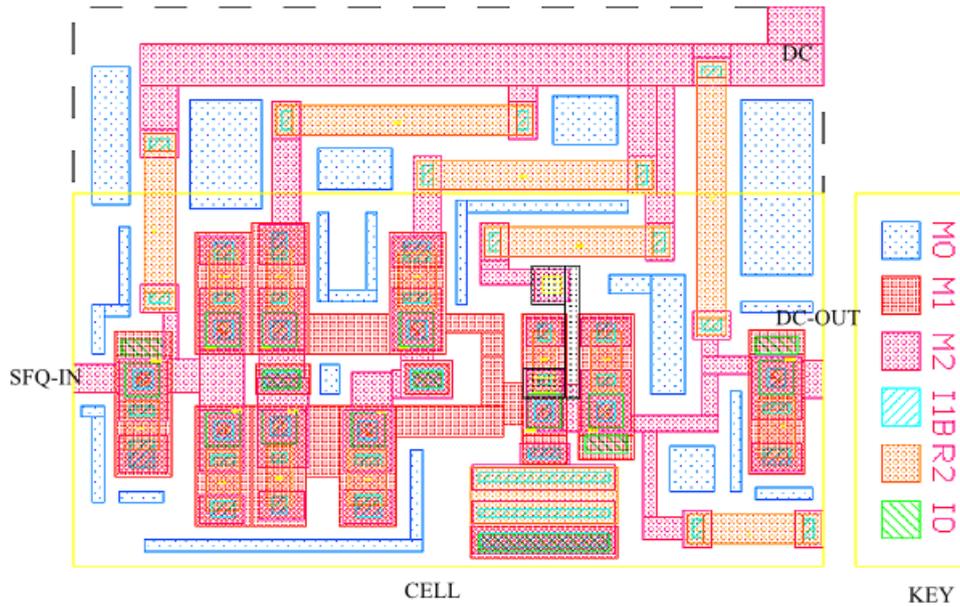


Figure 4.71: SFQ-DC layout for the Hypres process

4.2.15 Passive Transmission Line Driver and Receiver

In RSFQ electronics cells are normally connected using JTLs. This approach is only effective over short distances on the superconductor chip. The limitations with JTLs as interconnecting cells include increased propagation delays and increased power consumption [44]. A microstrip passive transmission line (PTL) has the ability to transfer picosecond pulses at a speed close to that of light without any loss over distances as large as 10 cm [45]. The PTL, just like any other transmission line, has a characteristic impedance Z_o , and any circuit connected to it has to be matched to it to avoid reflections. Specific circuits exist that are properly matched to the PTL for different Josephson current densities (J_C). The PTL driver is used to match and propagate SFQ pulses onto a PTL and the PTL receiver detects and amplifies the signal for the PTL line to the adjoining SFQ circuit. This concept is depicted in Fig. 4.72. The PTL Driver and Receiver cells are presented next.



Figure 4.72: A Model of a PTL showing the driver and receiver

4.2.15.1 PTL Driver

A PTL driver has two main purposes, to provide enough signal power to be propagated over the PTL and to match the PTL to the output JTL. The matching aspect is done by

including a small resistor just before the PTL, by making the McCumber parameter of the output junction of the PTL driver larger than one (typically $\beta_c = 4$). The schematic of a PTL Driver is shown in Fig. 4.73. Without careful observation, the PTL driver looks just like an ordinary JTL except for the series resistor R . Apart from improving the matching characteristics of the PTL driver, R ensures that the SFQ pulse is spread to enable propagation on the PTL as a voltage, i.e. it is decoupling resistor [30]. It also prevents flux storage in the output loop.

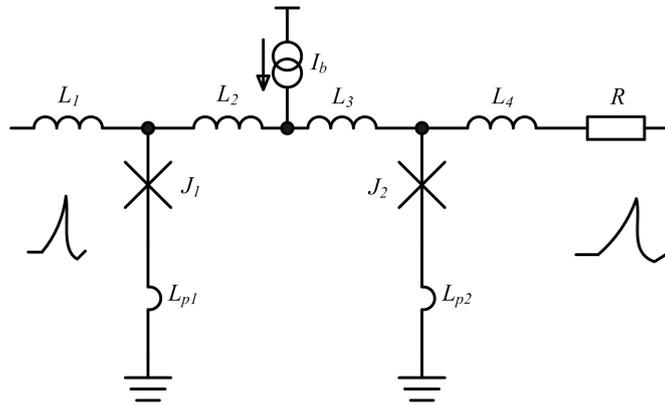


Figure 4.73: PTL Driver Schematic

4.2.15.2 PTL Receiver

The receiver recovers the voltage pulse on the PTL and transforms it back to an SFQ pulse. To ensure proper matching to the PTL, β_c of the input junction (J_1) is also made larger than one, just as J_2 in the driver. In the receiver schematic shown in Fig. 4.74, J_1 switches to the incoming voltage pulse. This, therefore means the bias current I_b and the critical current of J_1 can be adjusted at design level to achieve proper sensitivity of the receiver. Junction J_2 amplifies the SFQ pulse generated by J_1 . In addition J_2 provides matching to the output RSFQ circuit, with $\beta_c = 1$.

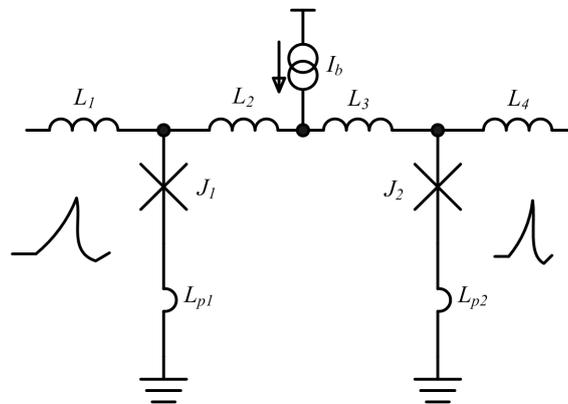


Figure 4.74: PTL Receiver Schematic

| Cell | Cell Space (μm) | Delay (ps)* | No. of JJs | Total Bias**(μA) | Bias Margins*** |
|----------|-----------------------------------|---------------|------------|-------------------------|--------------------------|
| JTL | 150 \times 150/100 \times 100 | \sim 6.5/4 | 2 | 351.4/360.1 | \pm 43%/ \pm 45% |
| Splitter | 150 \times 150/100 \times 100 | \sim 7/5 | 3 | 577.8/567.7 | \pm 45%/ \pm 43% |
| Merger | 150 \times 150/100 \times 100 | \sim 13/6.5 | 5 | 472.7/541.67 | \pm 32.4%/ \pm 32.4% |
| TFF | 300 \times 150/200 \times 100 | N/A | 8 | 915.5/915.5 | \pm 34.2%/ \pm 32.4% |
| DFF | 150 \times 150/100 \times 100 | \sim 12/5 | 5 | 365.06/409.9 | \pm 37.8%/ \pm 34.2% |
| NOT | 300 \times 150/200 \times 100 | \sim 25/15 | 8 | 830.85/827.5 | \pm 35.1%/ \pm 40% |
| AND | 300 \times 300/200 \times 200 | \sim 30/12 | 14 | 1072.4/1072.4 | \pm 33%/ \pm 36% |
| OR | 300 \times 300/200 \times 200 | \sim 10/4.5 | 9 | 551.5/591.3 | \pm 34%/ \pm 29% |
| XOR | 300 \times 300/200 \times 200 | \sim 20/10 | 11 | 738.4/757.7 | \pm 36%/ \pm 36% |
| NOR | 300 \times 300/200 \times 200 | \sim 30/15 | 12 | 1132/1121.6 | \pm 32.4%/ \pm 36% |
| NAND | 300 \times 300/200 \times 200 | \sim 22/12 | 16 | 1120.3/1134.2 | \pm 26.1%/ \pm 27% |
| XNOR | 400 \times 300/300 \times 200 | \sim 30/18 | 15 | 1147.9/1133.5 | \pm 26%/ \pm 27.1% |
| DC-SFQ | 150 \times 150/100 \times 100 | N/A | 3 | 450/450 | \pm 43.2%/N/A |
| SFQ-DC | 300 \times 150/200 \times 100 | N/A | 8/10 | 1095/1095 | \sim |

Table 4.13: Cell Summary based on simulation results: Presented as IPHT/Hypres

* Delay is defined as the time it takes for a cell to produce an output after a clock signal (synchronous) or input signals (asynchronous) are applied.

**The total bias current required for the proper functioning of a cell

***Bias margins obtained at a clock/input frequency of 10GHz.

4.3 Design of Bistable Circuits using π - phase-shifters

As described in Chapter 3, RSFQ circuits have the three building elements, Josephson junctions, bias currents and inductance. A constant bias current supply is required to initiate a phase change in the junctions concerned (see equat (3.2) where $\Phi = LI$). The current in the superconducting loops should be high enough to initiate a phase change equal to π , which signifies the presence of half a fluxon. Such a phase change ensures the switching of a Josephson junction at the arrival of an SFQ pulse which raises the current beyond the junction's critical value. This feature has been used throughout traditional RSFQ circuit design to date.

RSFQ bistable circuits rely on flux storage loops that are characterized by large inductances capable of trapping a quantum of magnetic flux. Such loops are based on the principle described in Section 3.2.2.2. Fig. 4.73 below shows some of the traditional configurations used in some of cells presented in this chapter. For these storage loops to work, a bias source is used to meet the phase change requirement in junctions. In the case of Fig. 4.73(a), the DFF, the bias current and the incoming flux initiate a phase shift in J_2 . In the TFF configuration (Fig. 4.73(b)), the bias current causes a phase change in J_3 and J_4 such that they switch simultaneously and the TFF operation starts.

Recent development have yielded a special Josephson junction whose current-phase relation is different from the conventional junction,

$$I = I_C \sin(\varphi + \pi) \quad (4.3)$$

which translates to $I = -I_C \sin(\varphi)$. Such a junction introduces a phase shift that is equal to π . This device, in essence, introduces a loop current that effectively eliminates the need for a bias current to introduce and sustain phase shifts. The ability to initiate the phase shift is inherent and for this to happen, careful implementation starts from layout to fabrication. Such junctions boast of a number of advantages which include reduction in current requirements per cell, thereby reducing power consumption and improved bit error rates in bistable circuits by eliminating shunt resistors, which may act as noise generators or pick-ups [46].

New approaches are being reported, one notable method as reported by [47][48], whereby a flux quantum is deliberately trapped by an integrated passive phase shifting element to introduce phase changes in superconducting loops. In Fig. 4.75(a), J_1 can be replaced by a π - junction thereby eliminating the need for the bias current. Likewise in part Fig 4.75(b), π -junctions can assume the positions of junctions J_1 and J_3 . The loop bias currents become unnecessary.

Both of these approaches are quite attractive and offer diverse approaches to RSFQ circuit design at a time when this technology needs to be put to full use.

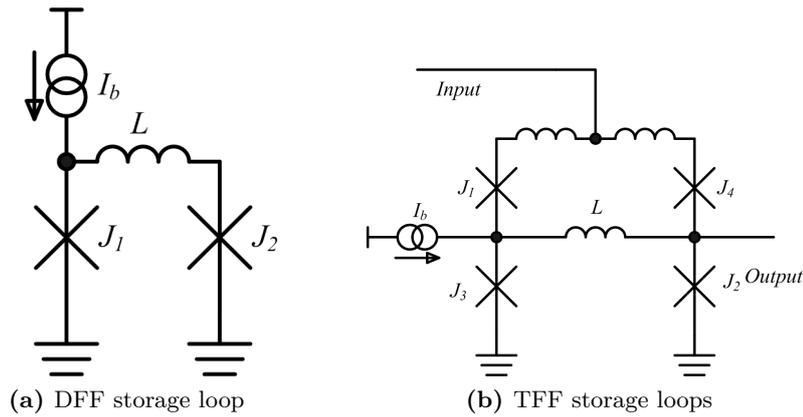


Figure 4.75: Conventional storage loops

4.4 Chapter Conclusion

The chapter presented the procedure used in RSFQ cell development. Inductance extraction is key in RSFQ circuits to ensure correct values at the right points on the cells. All the inductance values listed for each cell are extracted values. They are the actual values on the layouts. All the cells in the library have been presented. New cells of NOR, NAND and XNOR have been presented with all parameter values listed accordingly. Secondary parameters such as bias margins and delay are shown in tabular form in Table 4.13.

Chapter 5

On-Chip Cell Testing

“To invent, you need a good imagination and a pile of junk.” **Thomas Alva Edison**

The final and arguably the most involving stage in RSFQ cell development is the on-chip testing of cells. In Chapter 4, all the cells, both adapted and new, were presented. These cells need to be tested after fabrication. On-chip testing is a crucial process, because through it, cell functionality and final operating margins are established. As accurate as they may seem, simulations may have some estimations in Josephson junction models, that in the end may show a system with the best obtainable margins. On-chip testing reveals the practical attributes of a cell. Cell malfunction at this stage may emanate from a poor layout or to a lesser extent from fabrication errors. In this chapter, on-chip testing procedures are presented together, with the testing layouts for most of the cells presented in Chapter 4. RSFQ is a low-temperature category of electronics, therefore a cryogenic environment is required. Cryocooler and liquid helium testing regimes are also presented and compared in this Chapter.

5.1 Design of Layouts for On-Chip Testing

5.1.1 Interface cells

RSFQ circuits are pulse based and cannot be connected directly to common laboratory equipment. Interface cells (DC-SFQ and SFQ-DC) are used to interface RSFQ circuits to room temperature electronics. It can be observed from the test layouts presented in this chapter that signal entry points from room temperature electronics to RSFQ circuits go through a DC-SFQ cell first. A SFQ-DC converts the SFQ pulses from the pulse based RSFQ to voltage standard for the room temperature electronics.

5.1.2 Josephson Transmission Lines

The JTL was introduced in the earlier chapters as a connecting cell. It provides the much needed isolation between cells, matching and also pulse shaping and amplification. In order to feed a cell with the most accurate SFQ pulse, two JTL are used in cascade before the cell under test.

5.1.3 Bias Current Lines

RSFQ circuits are normally biased using current sources and not voltage sources. The reason being that voltage lines are more prone to noise pick-ups and make it much more difficult to control the bias values. In a more effective testing approach, the three sections of the test layout, i.e Input (DC-SFQ, 2 JTLs), Cell Under Test (C.U.T) and output (2 JTLs and a SFQ-DC) are given separate bias lines to avoid any interaction between the three elements and also to allow bias current adjustment of the cell under test. In this case three bias current sources are built and adjusted to provide enough current for each of the three parts. This lump sum current then divides to the various parts of the test cell as required by the bias resistors in each cell. A block diagram for the test layout is shown in Fig. 5.1. This layout can serve only simple cells with one input and one output. This approach was used in the simulation of all the cells presented in Chapter 4. Multiple input cells have test layouts that follow a similar test layout approach.

5.1.4 Test Instruments and Nature of Signals

Different cells require different numbers of test signals. For instance, an OR cell requires two input channels, clock channel and an output channel. All these channels require the same arrangement of a DC-SFQ and 2 JTLs. This translates into a test circuit that has 3 DC-SFQ cells, 8 JTLs and one SFQ-DC cell. Common laboratory instruments are used to provide signals to RSFQ circuits through high speed channels. These instruments must be properly shielded, because of the high sensitivity nature of RSFQ circuits to magnetic flux. External devices must therefore provide clean signals at all times. In simulations, a triangular pulse is used as input to the DC-SFQ to produce a continuous series of SFQ pulses as required. The triangular input signal can be seen in the block diagram in Fig. 5.1

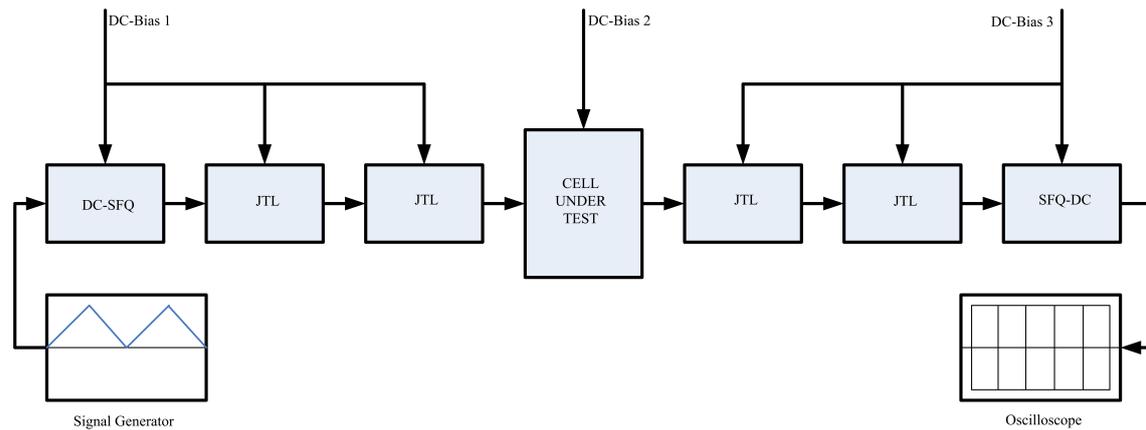


Figure 5.1: A simplified test layout block diagram for a one-input one-output cell most suited for low-frequency tests. The signal generator is a voltage source driving a controlled current source, while the oscilloscope is preceded by a differential gain of 10,000.

5.2 Testing of RSFQ Cells in Cryocooler and Liquid Helium

RSFQ circuits require low temperatures to operate, $4.2K$ for the niobium based circuits presented in this work. Cooling of superconductor circuits to cryogenic temperatures can be achieved either by immersing the superconductor circuit in liquid helium (He) or by using a closed cycle cryogenic refrigerator (*Cryocooler*). These two methods are discussed next.

5.2.1 Liquid Helium Cooling

This type of cooling involves the mounting an RSFQ circuit onto a specialized rod called a *Cryoprobe*. The cryoprobe is then inserted into a dewar of boiling liquid helium. Co-axial cables are mounted on the cryoprobe frame to carry signals to and from the superconductor chip at the tip. The cryoprobe is shown in a photo in Fig. 5.2 and is also shown in diagrammatic form in Fig. 5.3. The signal lines are capable of carrying DC and high frequency signals (low GHz) with very little attenuation, thereby offering a good electrical interface between the room-temperature and low temperature electronics.

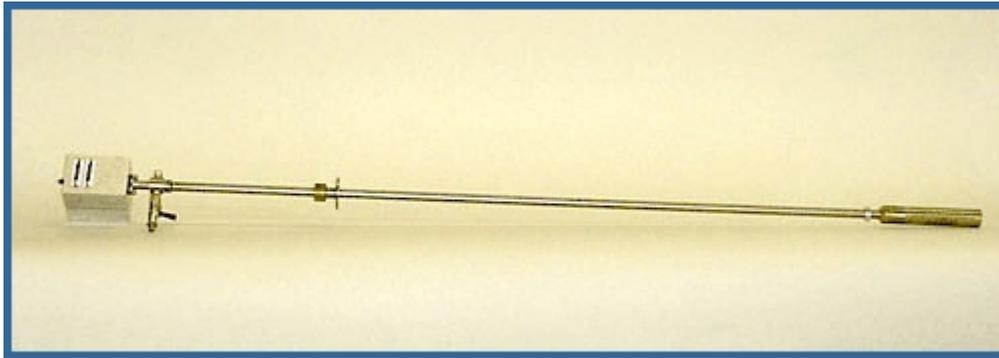


Figure 5.2: A photograph of a typical Cryoprobe - with a shield on the right end to protect the electronics under test. (a JVS-620 DF Cryoprobe by HPD Inc.)

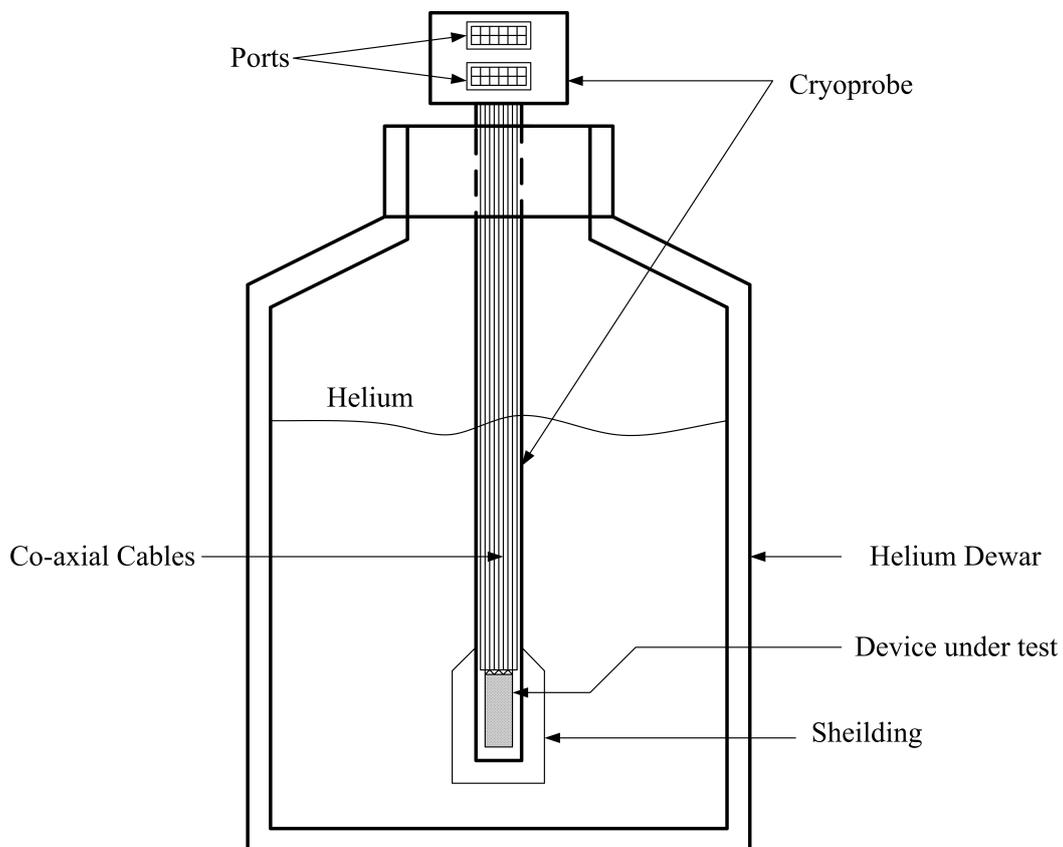


Figure 5.3: Diagram of a cryoprobe inserted in a helium bath

Helium testing has the advantage that no temperature oscillations occur and therefore a constant $4.2K$ temperature is assured. The drawbacks for helium cooling include the high cost of helium, the associated difficulty in filling up the dewar with helium and high maintenance costs [49]. These drawbacks mean that helium cooling is only suitable for laboratory environments. In addition, the nature of the system whereby a chip is attached to a probe and then inserted into dewar comes with isolation problems [50].

5.2.2 Cryocooler Cooling

Cryocooler based cooling is also used in the testing of RSFQ circuits in laboratories. Ideal for RSFQ applications are those coolers that have a cold temperature of $4K$, which is below the critical temperature of niobium ($9.2K$). Several types of cryocoolers exist and made by different manufacturers. Cryocoolers for RSFQ circuits are either based on the *Gifford-McMahon* (GM) principle or *Pulse Tube* (PT) based or a combination of both [51]. In both GM and PT based cryocoolers, the compressor is separated from the cold head. GM and PT cryocoolers are based on a gas flow that oscillates and regenerative heat exchange. Unlike the GM, PT has no moving parts in the cold region. This makes the PT more robust and more reliable. In addition PT offers more cooling power than the GM. The cold heads for GM and PT are shown in Fig. 5.4. Both systems employ two stages of cooling, where stage 2 is at $4K$.

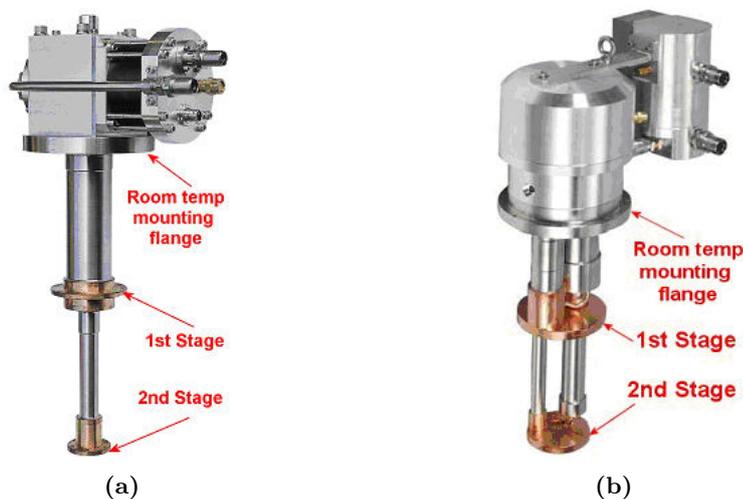


Figure 5.4: GM (a) and PT (b) cryocooler cold heads

For a cryocooler system to work, it usually requires three phase power for the compressor, water cooling if required and a vacuum (see Fig. 5.5). The vacuum is normally created by special pumps. It can be observed in Fig. 5.5 that these pumps are called *diffusion* and *turbo molecular* pumps. A vacuum equivalent to $10^{-6}atm$ is typically obtained from $1atm$, using these two pumps. These parts can be seen in Fig. 5.5 and the photo in Fig. 5.6.

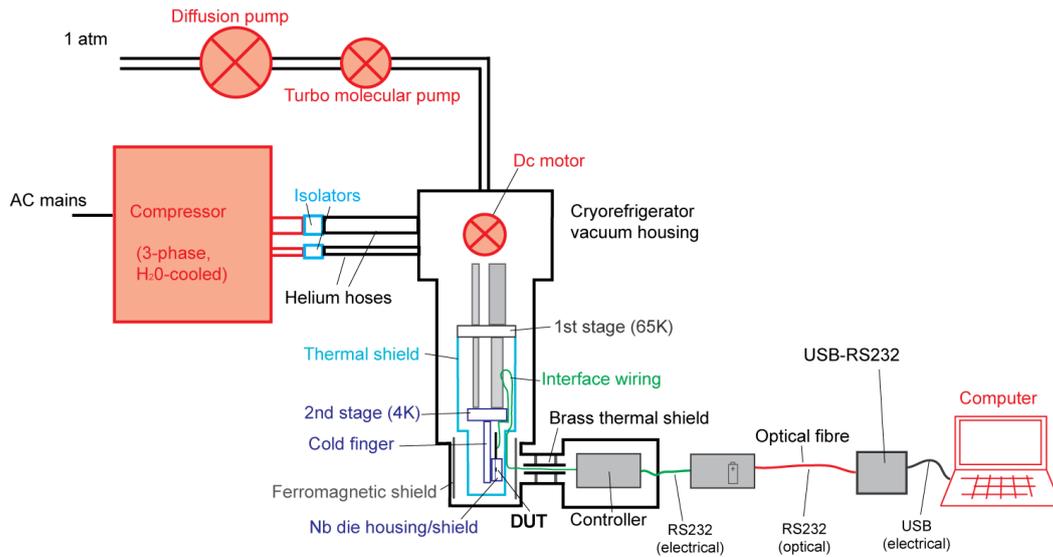


Figure 5.5: A diagram for the Pulse-Tube Cryocooler in use at the University of Stellenbosch [3]

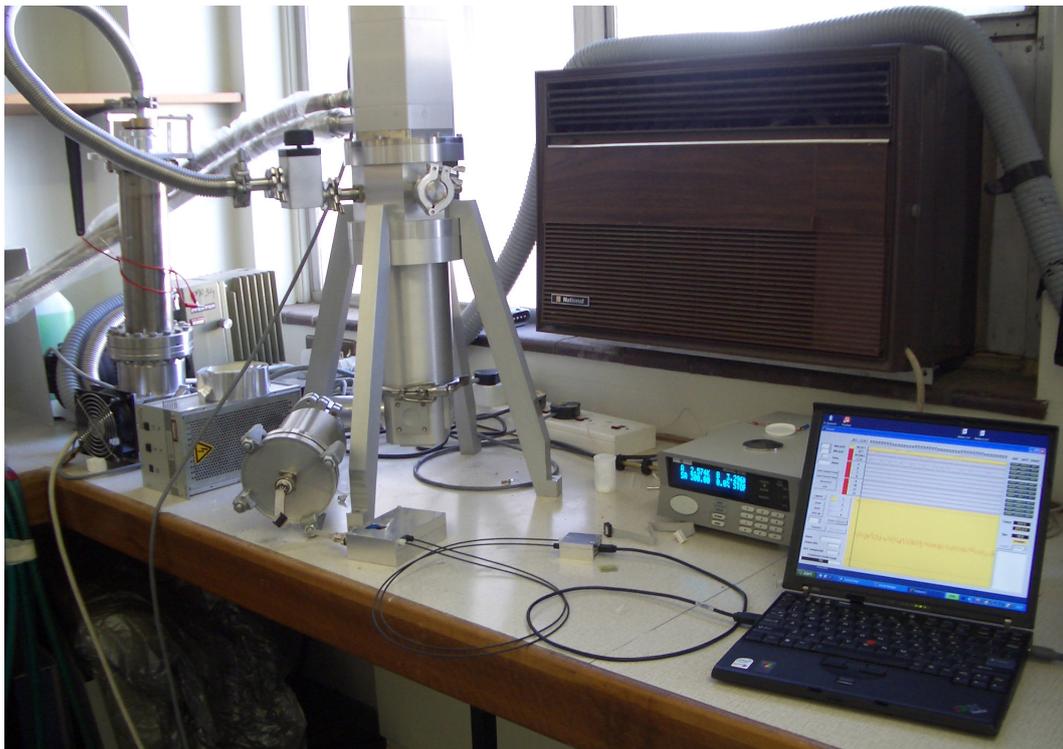


Figure 5.6: A photo for the Pulse-Tube Cryocooler cold head in use at the University of Stellenbosch

In Figs. 5.5 and 5.6 a laptop computer is used to generate control signals. It is then isolated optically to prevent the electrical noise generated by the computer from reaching the sensitive Cell Under Test (referred to as Device Under Test (DUT) in Fig. 5.5).

In addition, in Fig. 5.5 two cooling stages; First stage and Second stage, are shown with their corresponding temperatures. The helium is pumped into the cold finger through

two hoses by a compressor that operates at roughly $1.6Hz$. This oscillation brings about temperature variations.

The cryocooler suffers from temperature oscillations observed at the cycles of helium cooling. The fluctuations observed by researchers at Hypres are within $\pm 200mK$, which is similar to that measured at Stellenbosch. The conditions under which this value was arrived at are not clear. The cooling power from cryocoolers is low, typically $0.5W$ at $4K$ (CryoMech ST405 pulse tube refrigerator), while other cryocoolers deliver around $1W$ at the same temperature. Such low power cooling demands that heat generated by bias lines and contributed by ambience be below the cooling power to maintain the RSFQ circuits at $4K$.

5.2.3 Additional information on cell testing in cryocoolers and liquid helium

Helium and cryocooler test setups need to incorporate magnetic shielding to protect the superconductor chip under test from the earth's field. Such protection is normally provided by a degaussing coil and magnetic shields [52]. In a cryocooler setup, a ferromagnetic shield is often used for this purpose.

Leads carrying signals in the testing setups for superconductor circuits need to be highly optimized. Attenuation and heat generation/conduction can not be ignored [53]. For example, a cell may require a bias current of $1A$ and the conductor carrying the current generate heat (proportional to I^2R). Efforts are required to minimize the conduction of this heat into the superconductor circuits under test. A common approach is to use coaxial cables with low attenuation and low heat conduction [53].

Tests of superconductor circuits are done in two parts [49]. The first part is called low frequency testing which aims at establishing circuit functionality. Signals in the order of $1kHz$ are used. The second type is high frequency testing that seeks to investigate the maximum operating frequency of the circuit under test. Signals as high as $20GHz$ or more are used. High frequency testing is quite challenging and requires more control. In addition, the conductors used should be able to carry such high frequency signals with negligible attenuation.

5.3 RSFQ Testing Procedure

RSFQ circuit testing is quite a complex process. In this section an example is given for a DC-to-DC RSFQ circuit. Such a circuit has an input DC-SFQ followed by a number of JTLs and then an SFQ-DC converter. The RSFQ circuit is contained in either a liquid helium Dewar or in a cryocooler cold head. Conductors come in and out of such an environment to the external control, signal sources and sinks.

A triangular pulse is an input of choice for low-frequency testing because of it can be made to rise and fall slowly. The DC-SFQ produces an SFQ pulse when the input current exceeds $\sim 600\mu A$ and continues to do so at another step of the same current magnitude. In Fig. 5.7, It can be observed that the input (yellow) exceeds slightly thrice the switching current thereby producing 3 SFQ pulses in one rise. It can be observed in the output signal (purple) taking into account that the SFQ-DC divides the input frequency by two. The circuit under test was manufactured in the Hypres $4.5kA/cm^2$ process and tested in helium at the University of Ilmenau in 2010. Output of the SFQ-DC is $300\mu V_{p-p}$.

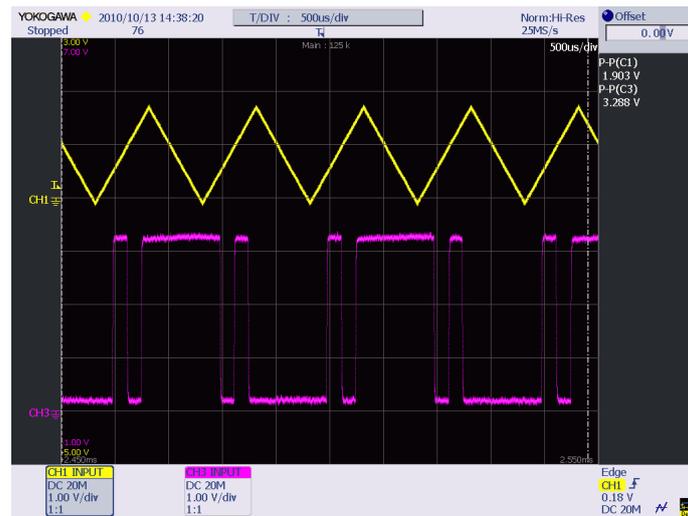


Figure 5.7: DC-DC testing results in a liquid helium Dewar with a triangular wave input



Figure 5.8: DC-DC testing results in a liquid helium Dewar with a square wave input

The results shown in Fig. 5.8 are those of the same DC-DC but with a square wave as input. It can be observed in both plots that the input (yellow) is a voltage. To realize the required current to the DC-SFQ, a 1Ω resistor is used. In this plot, the input signal is such that only one SFQ pulse is produced when the current rises above the threshold value. The output (purple), gives the plot from the SFQ-DC.

Throughout such testing arrangement, signals are carefully injected and controlled to achieve the right results. All the remaining cells in this thesis will have to go through such a process to confirm if they work as expected.

Signal leads are run using co-axial cables due to their good frequency response and no crosstalk between conductors. This, however, demands that the loads be properly matched to the cables to prevent signal reflection and signal energy loss. Co-axial cables have a characteristic impedance Z_o of 50Ω . In the chips, all signal entry and exit points are connected through resistors of that value to provide matching. Bias current cables, on the hand, are twisted-pair with low-frequency cut-off.

5.4 Cell Test Layouts

This section presents the test-layout structures as illustrated in Fig. 5.1. All cells have similar layouts with interface cells and JTLs connected as required. In order to send the cells for fabrication cells are integrated onto a chip. The chip provides all the necessary signal and bias current routing for all the cells integrated.

Since most layouts are similar, it is not necessary to present all the test layouts for cells here. For example, clocked two input - one output cells have similar layouts. However, all the cells form part of the chip, because they all need to be fabricated before testing. Interface cells such as the DC-SFQ and SFQ-DC were already tested and they work. They are, therefore, used here as testing aids. Test layouts for selected cells are presented next.

5.5 Chip Design and Layouts

The final stage is to have all the test layouts incorporated onto a chip(s) for fabrication at Hypres and IPHT. Both processes have a few guidelines on how to create layouts that fit on specific chip sizes.

The Hypres process requires chip sizes of $5mm \times 5mm$ with a $150\mu m$ clearance ($75\mu m$ on each side for dicing) or $10.15mm \times 10.15mm$ with a $150\mu m$ clearance as well. For the IPHT process chip sizes $5mm \times 5mm$, $6.4mm \times 6.4mm$ and $12.8mm \times 12.8mm$ and separation between chip of $100\mu m$ is required for cutting during dicing.

In this work, only the $5mm \times 5mm$ chip sizes were considered in both processes as a starting point. This choice came with a disadvantage in that the test layouts require more chips for them to fit and sent for fabrication together.

Sample chips are shown in Figs. 5.18 and 5.19 as IPHT and Hypres in that order. Due to the large number of connections required per test layout, only a few could be

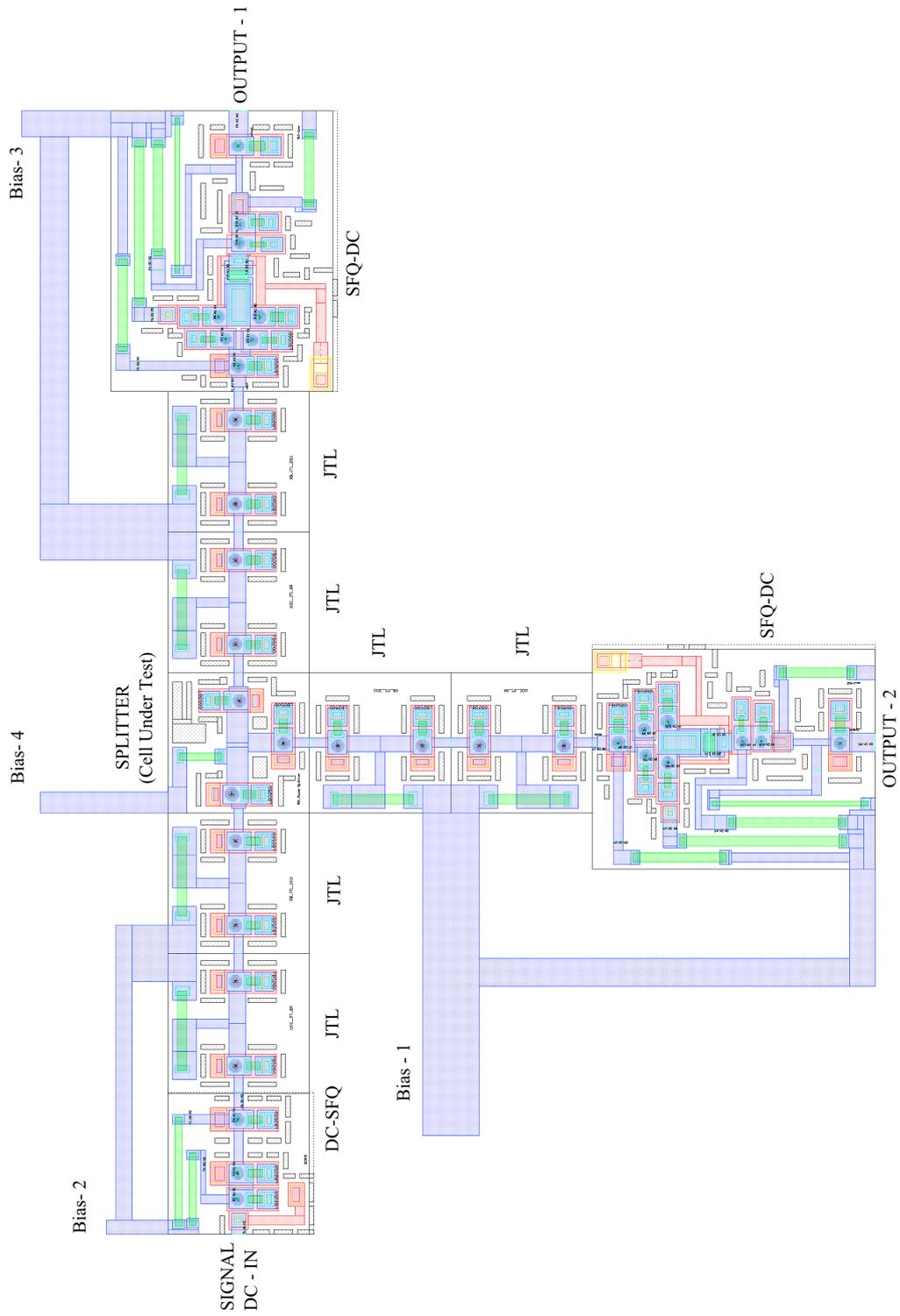


Figure 5.9: Splitter layout for on-chip testing

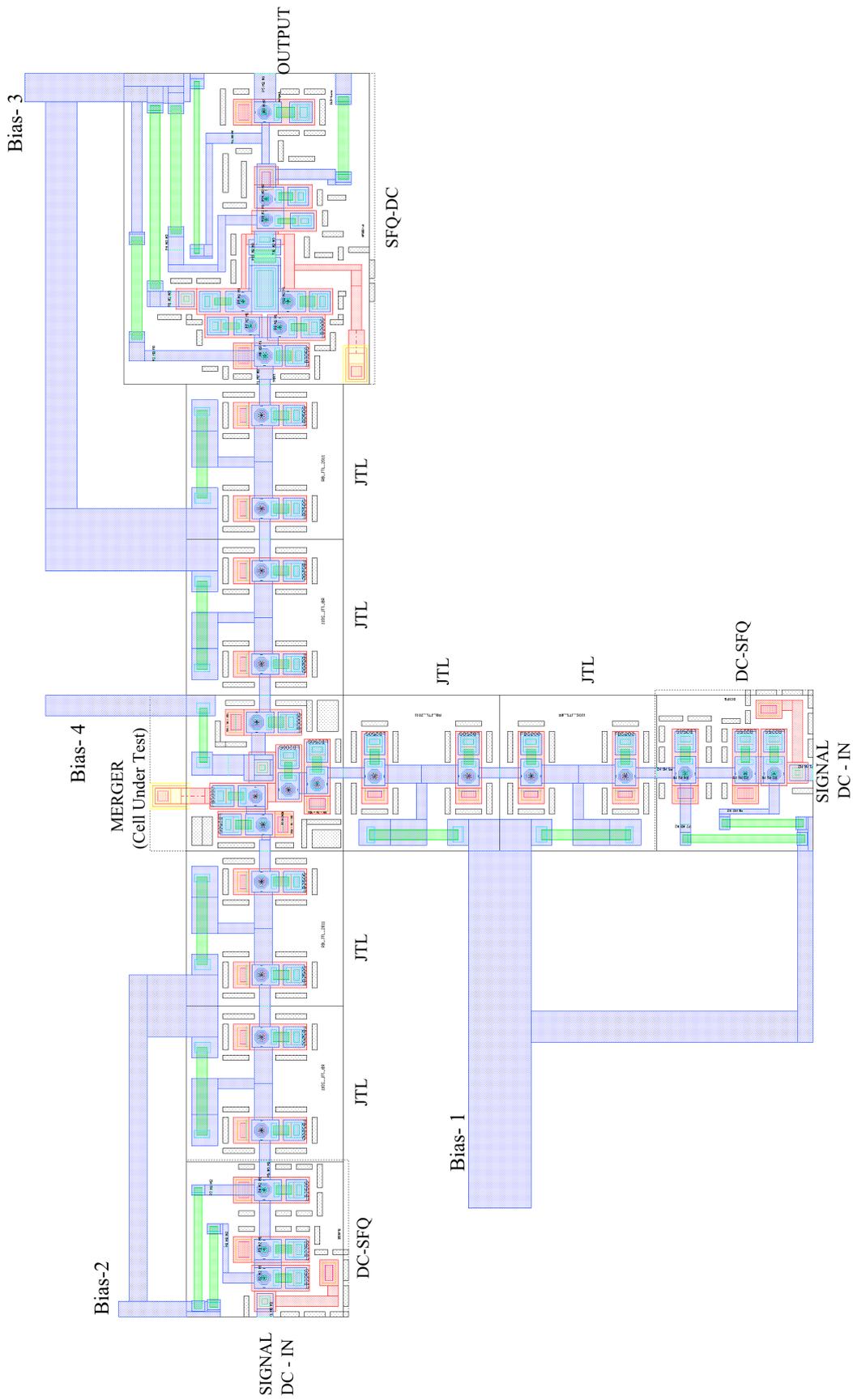


Figure 5.10: Merger layout for On-chip testing. The test layout has three sections: two input channels and one output channel. *Bias - 1* and *Bias - 2* may have a single source as they both feed input sections and little interaction is expected.

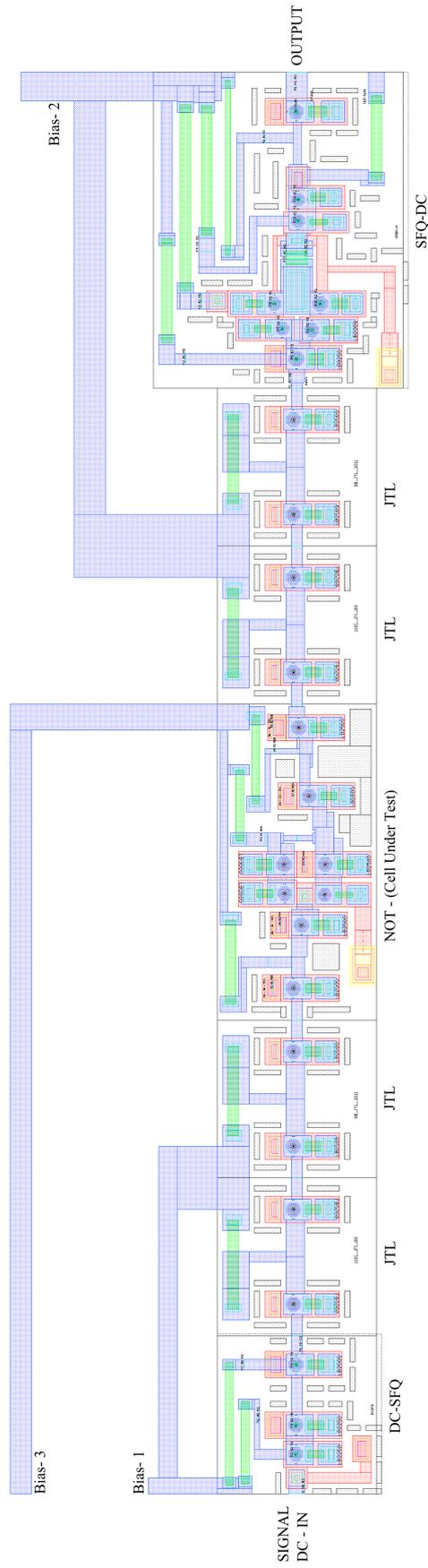


Figure 5.12: NOT Cell On-chip test layout for the IPHT process

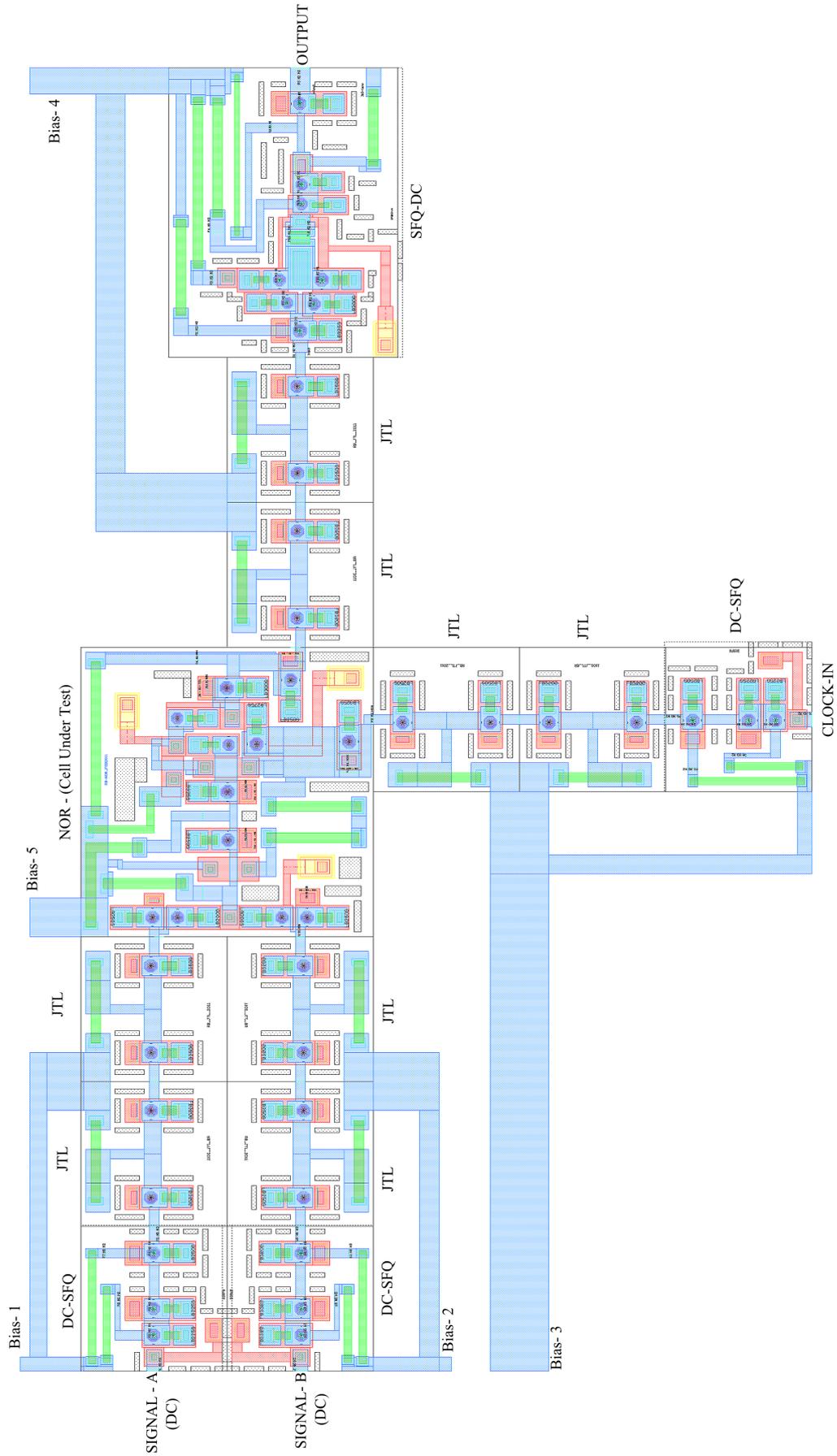


Figure 5.13: NOR cell on-chip test layout for the IPHT fabrication process

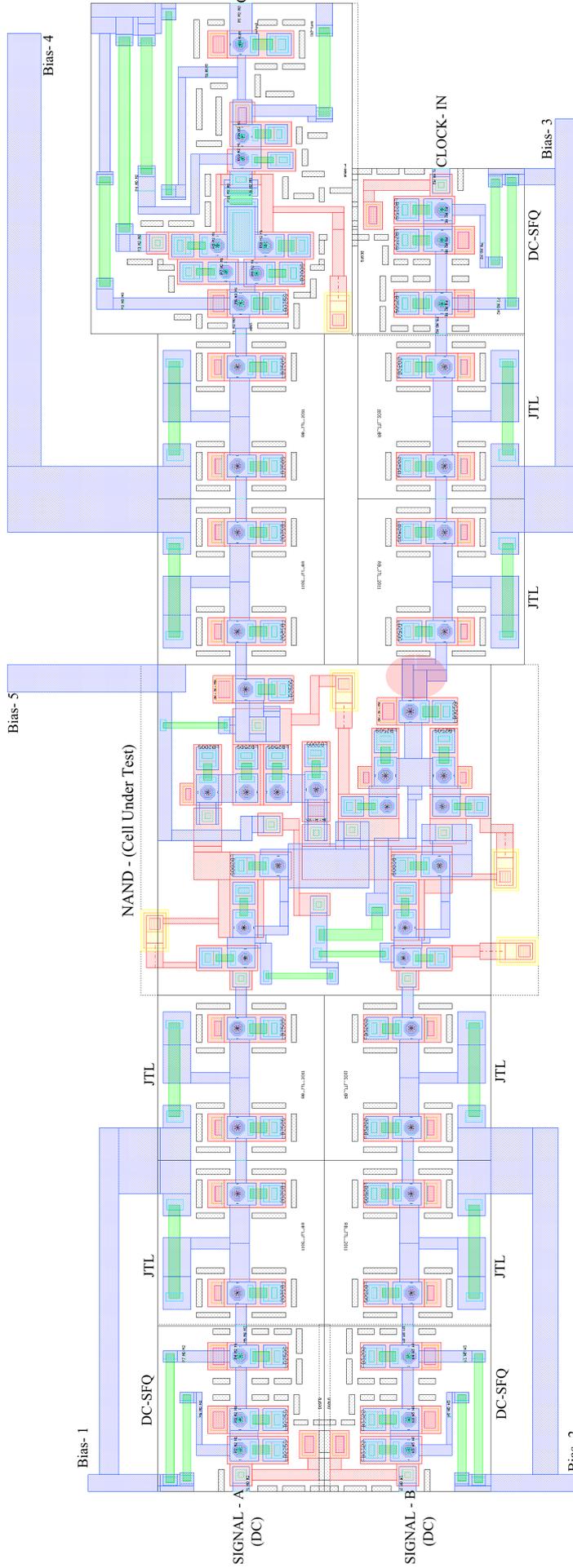


Figure 5.14: NAND cell's On-chip test layout for the IPHT fabrication process

Due to the size of the SFQ-DC, clock input of the NAND cell does not align with the output of the JTL. This interface point had to be modified to reflect the same inductance values. The point being referred to is marked with a reddish ellipse on the Figure.

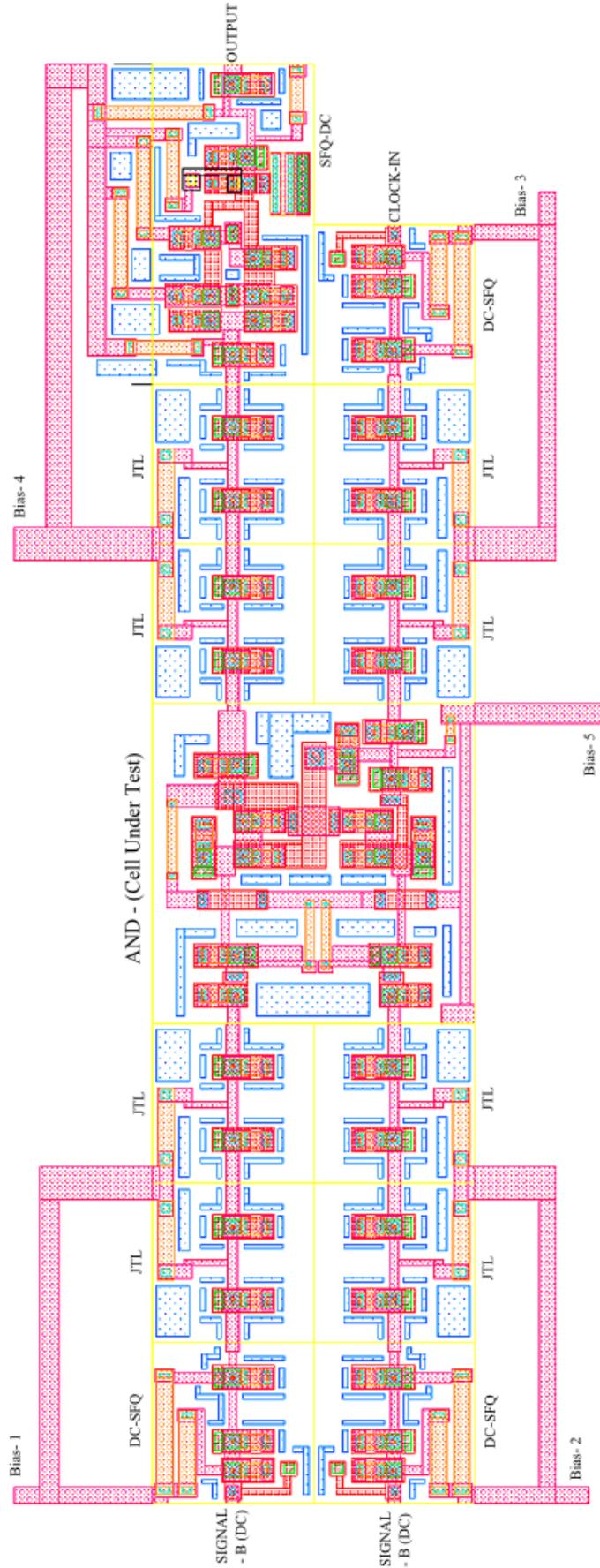


Figure 5.15: AND cell's On-chip test layout for the Hypres fabrication process

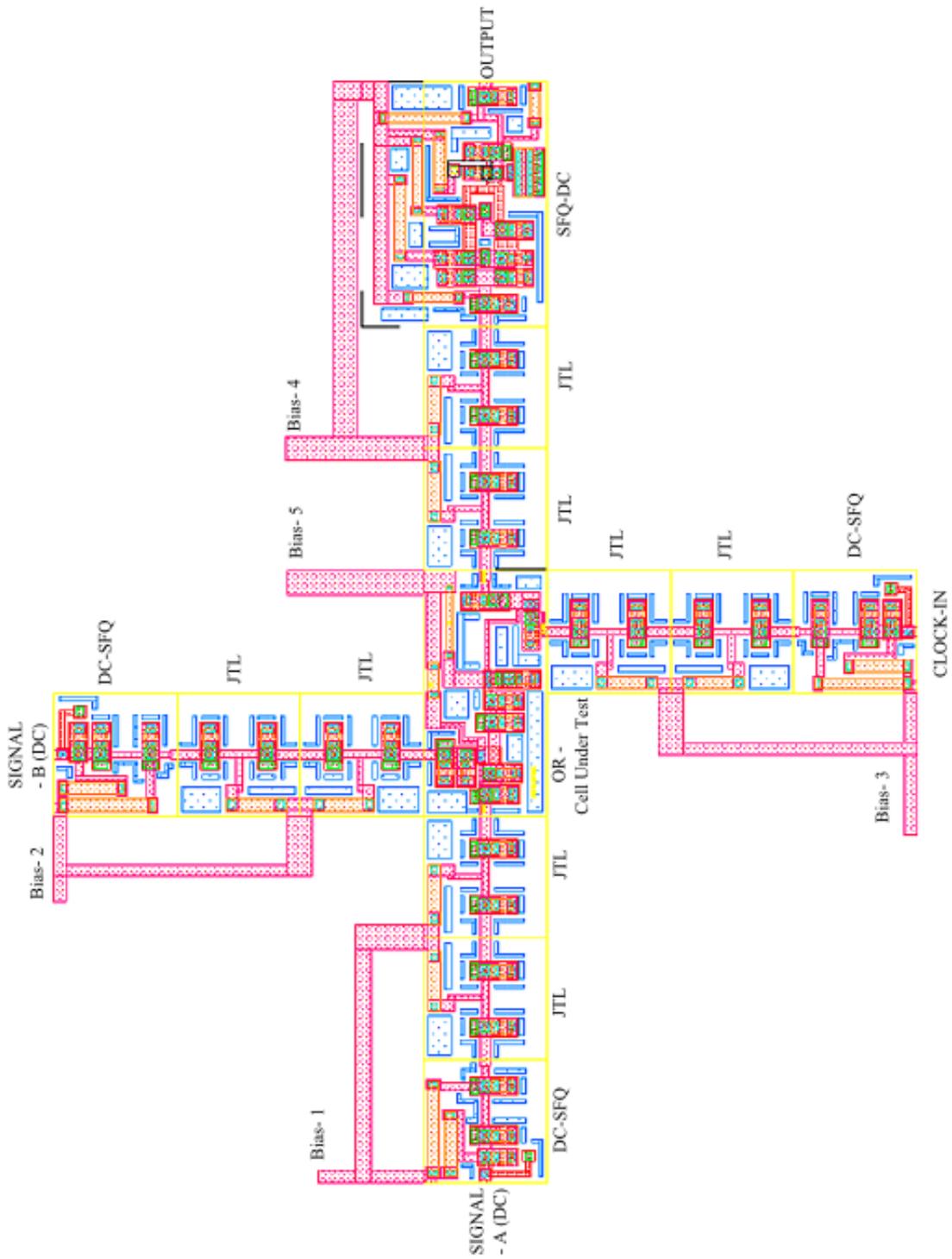


Figure 5.16: OR cell's On-chip test layout for the Hypres fabrication process

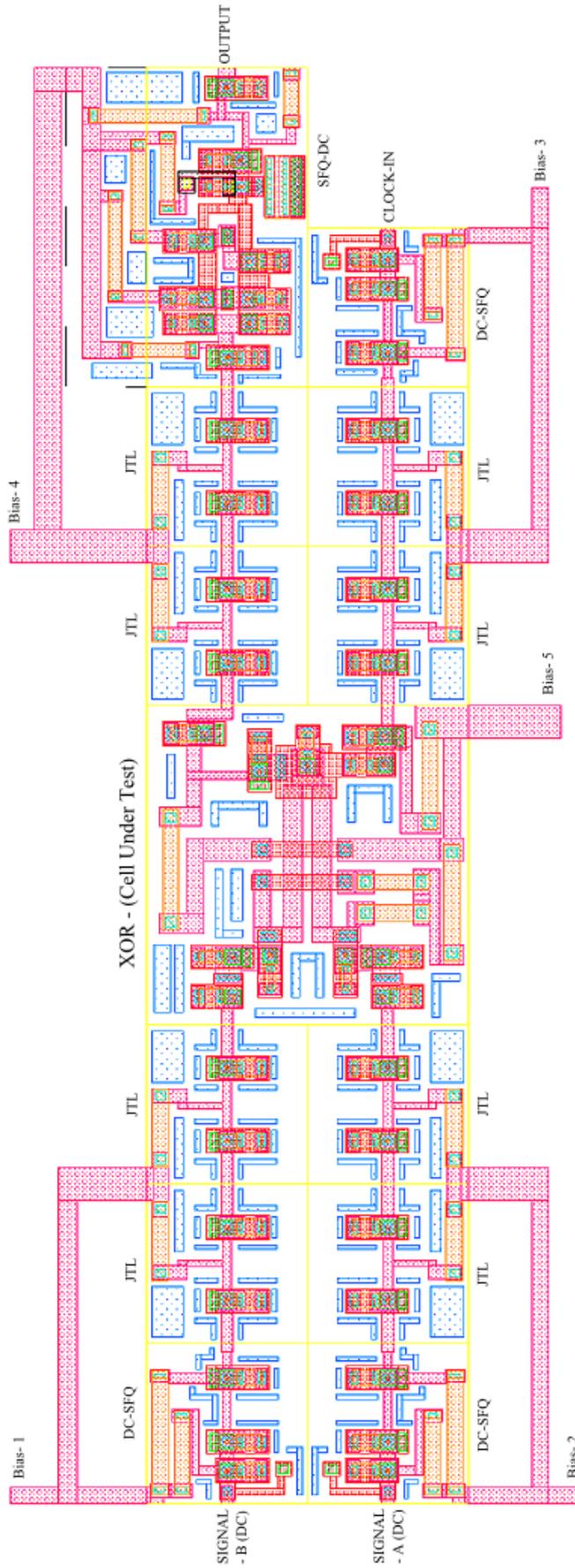


Figure 5.17: XOR Cell's On-chip test layout for the Hypres fabrication process

accommodated on a Chip. The IPHT chip has the Splitter, Merger, DFF and NAND cells test layouts while the Hypres chip has the XOR, OR and AND test layouts. More chips are therefore required to accommodate all the test layouts.

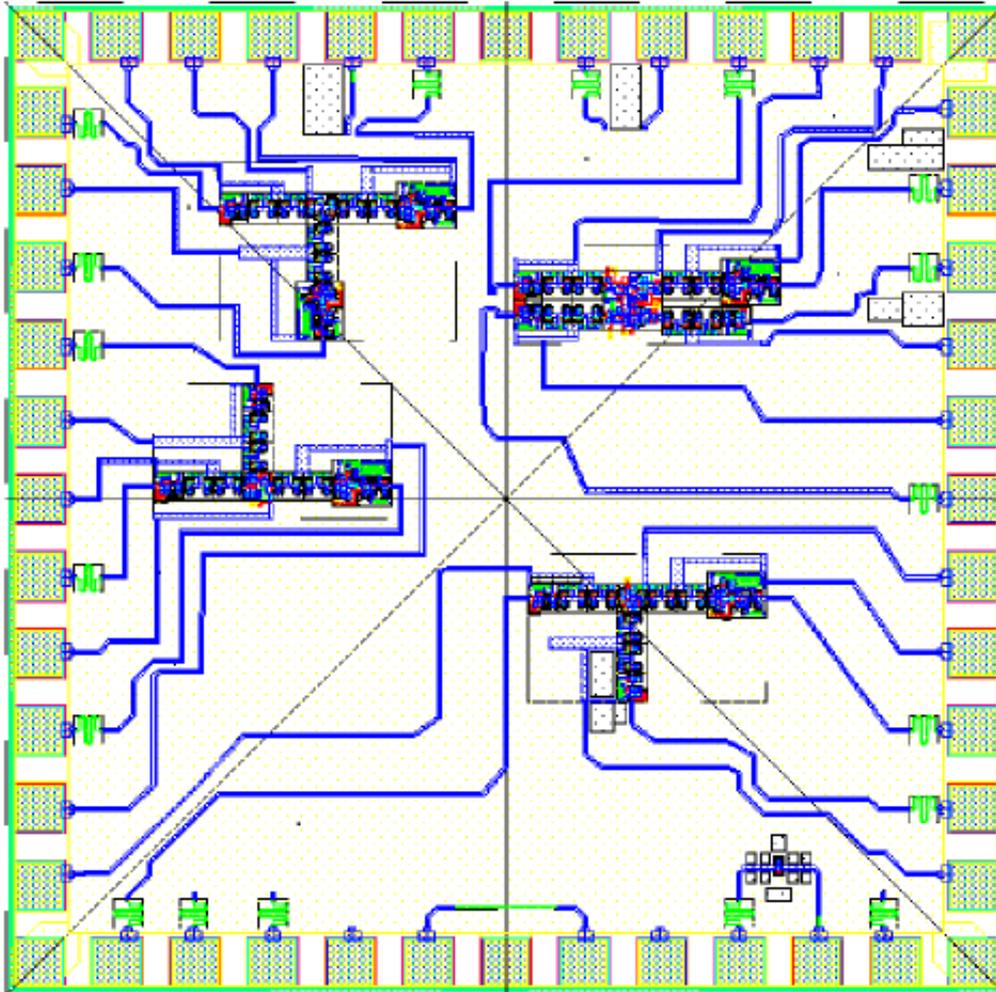


Figure 5.18: A sample chip for the IPHT process - $5\text{mm} \times 5\text{mm}$

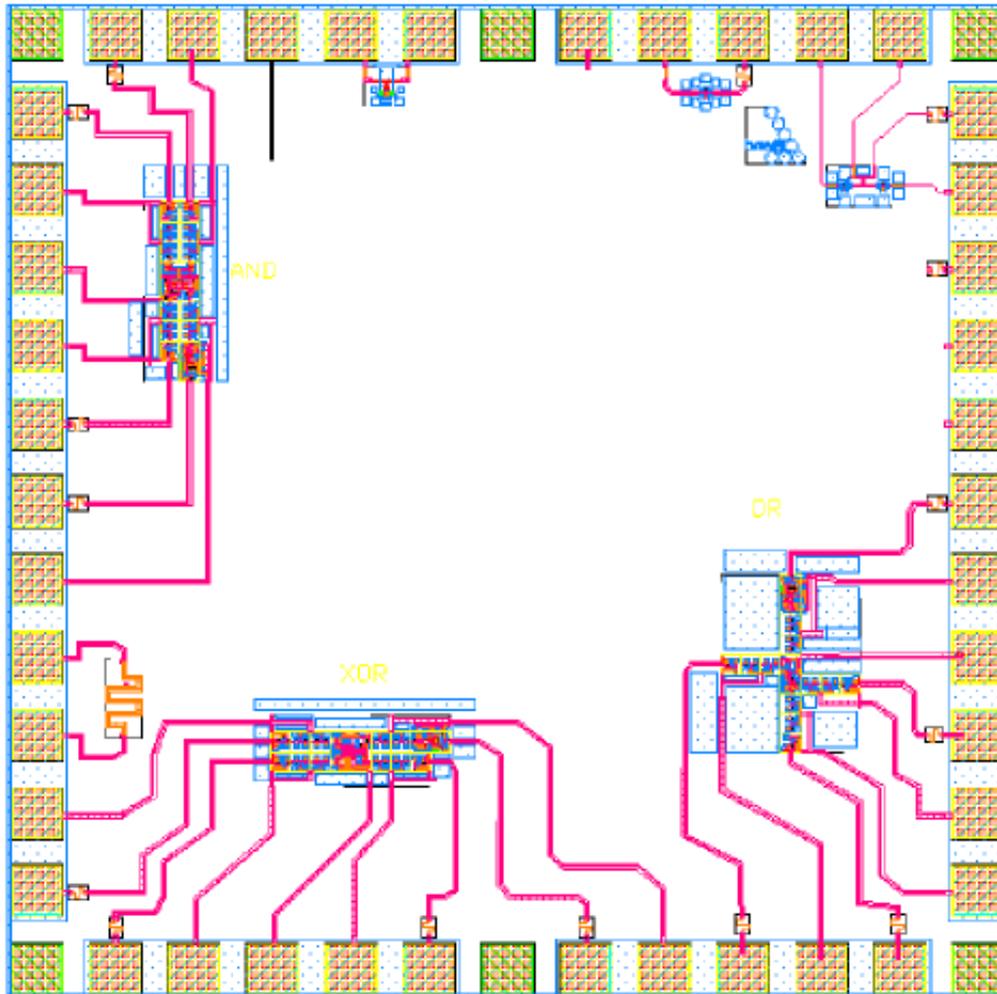


Figure 5.19: A sample chip for the Hypres process - $5mm \times 5mm$

5.6 Chapter Conclusion

In this chapter, the need for on-chip testing for cells is emphasized. Example layouts for both IPHT and Hypres are given. Some of these layouts for testing have been incorporated in the chips shown in Figs. 5.18 and 5.19. Cells will be tested after fabrication to establish simulated functionality and bias current margins. Due to the numerous connections required for each test layout, only four test layouts could fit on one chip. This translates to about 2 to 3 chips to accommodate all the cells in the library for each fabrication process.

Chapter 6

Conclusions and Recommendations

“To unpathed waters, undreamed shores” - William Shakespeare

6.1 Conclusions

An RSFQ cell library has been designed and implemented with both adapted and new cells. In total, the library has 17 cells with diverse functionalities. Bistable cells (gates) such as the DFF, AND, OR, XOR, NAND, NOR and XNOR, signal processing cells such as the Splitter, Merger, NOT, TFF and interface and connecting cells such as the PTL Driver and Receiver, SFQ-DC and DC-SFQ and of course the JTL are now part of the library. Most cells have all the parameters provided in the thesis to give room for further developments, designs and analyses of cells and complex RSFQ circuits.

Cells in the library have been submitted for fabrication at IPHT and Hypres. Once fabrication is done, laboratory on-chip testing of these cells will be carried out. At this stage functionality and bias margins will be investigated and documented accordingly. The analysis will be slightly different for the new cells. It will be the first time they will be tested being new cells. The new cells include NOR, NAND and XNOR.

Cells were designed to enable a tiling approach. Signal entry and exit points are located at similar locations in each cell. This makes it easy to connect cells and may save chip space.

The following conclusions can be made from the work presented in this thesis.

- Cells adapted from the IPHT and SUNY cell libraries were simulated and optimized. New or modified layouts were done. Good bias margins were obtained, over $\pm 30\%$.

- New cells have been designed and incorporated into the library. These cells show very good bias margins. The NOR cell has an overall bias margin of $\pm 32\%$, the NAND $\pm 29\%$ and the XNOR with a bias margin of $\pm 26\%$. The cells were laid out and all inductance values extracted.

6.2 Recommendations

The following recommendations are made specifically to this work and RSFQ cell design in general.

- *Cell Design* : The NAND cell is large and it was a huge challenge to design. The design presented in the thesis aimed at having the minimum number of Josephson junctions, but at the same time, preserving the functionality with good bias margins. An alternative design would be to incorporate driver junctions at each input. But this approach means an obvious increase in the number of junctions and an increase in bias current required to sustain the cell operation.
- *Parameter extraction*: Inductance extraction was done with *Inductex* and all the values are presented in the thesis. However, *Inductex* only handles extraction of inductances and all other parameters such as bias resistors, had to be estimated manually using design rule guidelines. The bias resistor values may not be very accurate. *Inductex* is undergoing changes and it is recommended that extraction of these resistors be done later on.

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Appendix A

Alternative schematics for a DFF

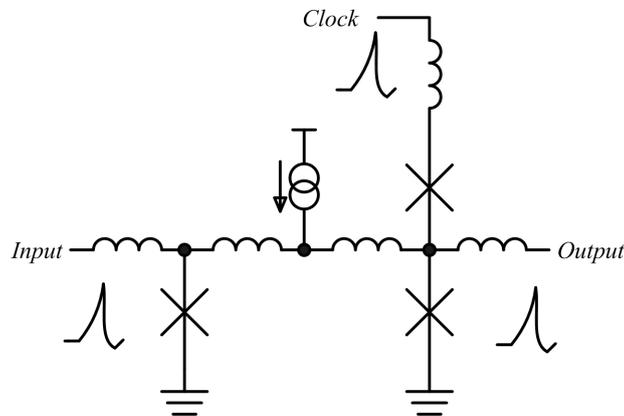


Figure A.1: 3 Junction DFF

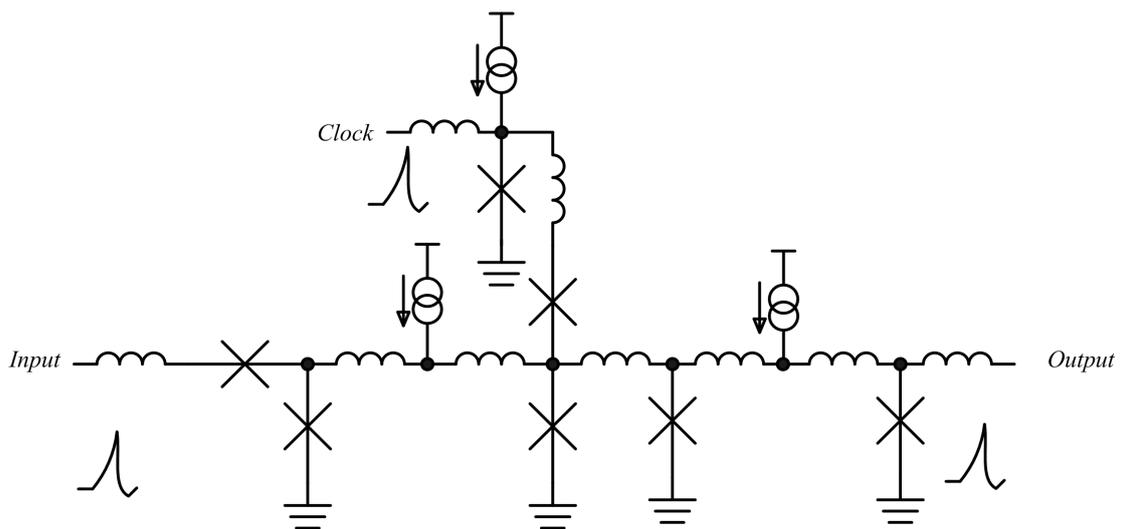


Figure A.2: 7 Junction DFF

Appendix B

A 2-Output TFF Schematic

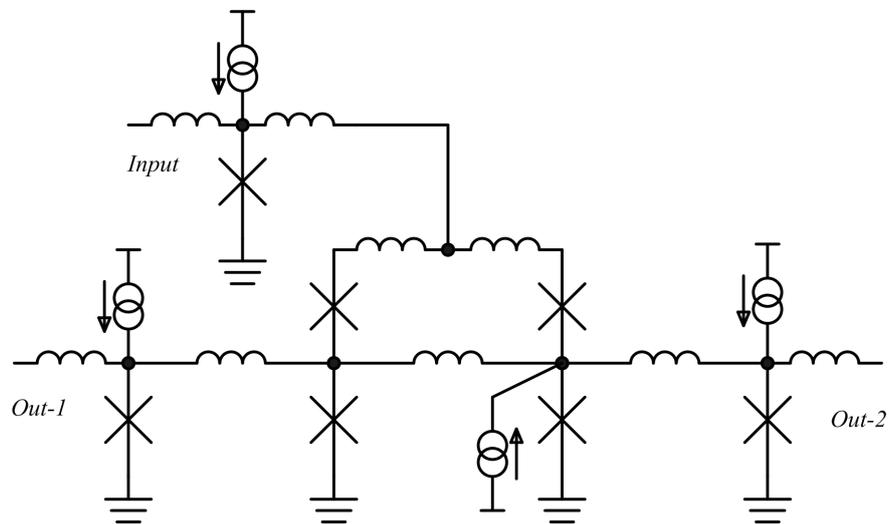


Figure B.1: A 2-Output TFF schematic

Appendix C

IPHT's $1kA/cm^2$ Process Design Rules

Process RSFQ1D-1.2

Rapid Single Flux Quantum (RSFQ) – Design Rules for Nb/Al₂O₃-Al/Nb-Process at

Version 22.06.2007

IPHT Jena

Address: Institute of Photonic Technology (IPHT)

**Department of Quantum Detection
P.O. Box 100 239
D - 07702 Jena
Germany**

Contact: Dr. H.-G. Meyer (Head of Department)

phone: + 49 3641 206116
FAX: + 49 3641 206198
e-mail: hans-georg.meyer@ipht-jena.de

Dr. J. Kunert (RSFQ Design)

phone: + 49 3641 206126
FAX: + 49 3641 206199
e-mail: juergen.kunert@ipht-jena.de

Internet: <http://www.ipht-jena.de>

Process RSFQ1D-1.2

RSFQ design rules IPHT Jena Version 1.2**Nb/Al₂O₃-Al/Nb-technology Process : RSFQ1D**

Date: 6/22/2007

A. Photomasks:

| Mask | GDSII No. | Name | Layout polarity | Color | Material | Thickness /nm | Description | Mask polarity | Wafer resist |
|------|-----------|------|-----------------|------------|--------------------------------|---------------|--|---------------|--------------|
| A | 1 | M0 | positive | yellow | Nb | 200 | Ground plane | dark | + |
| B | 2 | I0A | negative | magenta | Nb ₂ O ₅ | 50 | Holes in anodisation | clear | - |
| C | 3 | I0B | negative | magenta | SiO | 200 | Holes in isolation | clear | - |
| D | 4 | I0C | | | SiO | | Reserved | | |
| E | 5 | M1 | positive | Red | Nb | 250 | Wiring1 | dark | + |
| F | 6 | T1 | positive | Cyan | Nb/Al/Nb | 60/12/30 | Trilayer package | clear | - |
| G | 7 | I1A | negative | Light blue | Nb ₂ O ₅ | 70 | Holes in anodisation, Definition of junction | clear | - |
| H | 8 | CUT | positive | Light gray | --- | --- | Cutting of bridges for anodisation | clear | + |
| I | 9 | I1B | negative | Light blue | SiO | 150 | Holes in isolation | clear | - |
| J | 10 | R1 | positive | green | Mo | 80 | Resistance layer | clear | + |
| K | 11 | I2 | negative | coral | SiO | 150 | Holes in isolation | clear | - |
| L | 12 | M2 | positive | Blue | Nb | 350 | Wiring 2 | dark | + |
| M | 13 | R2 | positive | Dark green | | | Bond pads, optional | dark | - |

Positive layout polarity means you design the physical structures as seen on the screen, negative means you design holes in the material. Clear mask polarity means that the mask is transparent wherever the patterns are drawn and dark means the opposite case.

B. Auxiliary Layers:

| GDS II-No. | Name | Layout polarity | Place on mask | Description |
|------------|--------|-----------------|-----------------------------|---|
| 15 | SMA | Positive | all | Used for labels on masks |
| 16 | SMC | Positive | L-M2 | Used for labels on chip |
| 17 | MON | Negativ | A-M0 | Defines holes in M0 plane by XOR with A-M0 |
| 18 | TEXT | Positive | none | Used for help lines and notes |
| 19 | TERM | --- | none | Defines ports for L-meter inductance calculation |
| 20 | INVERT | --- | All with dark mask polarity | Area to invert polarity to use only masks with polarity clear |

Remarks and auxiliary layers:

- Structures in layer SMA (GDS II-No. 15) are put **on all masks**.
- Holes in the M0 plane (moats) can be drawn on a separate layer MON (GDS II-No. 17). For photo mask production this layer will be subtracted from layer M0 (GDS II-No. 1).
- TEXT layer (GDS II-No. 18) is used for additional text and other structures (lines, polygons etc.) during layout generation. It is **not put on masks**.
- To meet the correct value the holes in anodisation will be increased of 100nm by a resize operation during data prepatation

Process RSFQ1D-1.2

C. Basic design rules:

1. Patterns (for all layers)

- Only polygon patterns with edge angles of 45°, 90° and 135° should be used.



For example :

(an customer has to take in account that using of an edges with angles different from $n \times 45^\circ$ are approximated with rectangular steps).

- Data points on a grid smaller than 0.1 μm will be rounded to this 0.1 μm during compilation of the data for the e-beam writer.
- The number of edges should be as low as possible. That means that one big



Rectangle is better than such a structure (if it is possible).

It is recommended

to use a grid of 2.5 μm for the corners of polygons and the centers of Josephson junctions (JJs). Only in special cases other grid values should be used. It is strongly recommended to use a grid of 25 μm for long interconnection lines. This means, that at least one edge of patterns in M2, M1 or M0, which have to be connected to the contact pads, must be on the 25 μm grid.

2. Width and spacing inside single layers

2.1 Layers M0, M1, M2:

- Width $\geq 5 \mu\text{m}$.
- Spacing $\geq 5 \mu\text{m}$, $\geq 2.5 \mu\text{m}$ if strip length $\leq 75 \mu\text{m}$.

2.2 Layer M2:

- Width W and spacing S of long interconnection lines between circuits and contact pads should be as large as the layout permits (standard value $W = S$, $W = 100 \mu\text{m}$).

2.3 Layer I0A, I0B, I1A, I1B, I2:

- Minimum contact hole size is 5 $\mu\text{m} \times 5 \mu\text{m}$,
- Spacing between different contact holes is $\geq 5 \mu\text{m}$.
- Spacing Inside I0A, I1A $\geq 2.5 \mu\text{m}$

Process RSFQ1D-1.2

2.4 Layer I1A:

- Size of Josephson junction is defined by I1A. The JJs have an octagon form and the smallest JJ has an area of 12.5 μm^2 with an inner diameter (see page 7) of the octagon of 3.8 μm .

2.5 Layer CUT:

- For cutting wires in M0 or M1; these lines have to be longer than 15 μm .

2.6 Layer T1:

- Spacing $\geq 5 \mu\text{m}$.
- T1 used only to form JJ. Size of JJ is defined by I1A.

2.7 Layer R1:

- Width $\geq 5 \mu\text{m}$.
- Spacing $\geq 5 \mu\text{m}$, $\geq 2.5 \mu\text{m}$ if strip length $\leq 75 \mu\text{m}$.
- Widths of bias resistors are fixed to 10 μm , spacing $\geq 5 \mu\text{m}$.
- Widths of shunt resistors should be no less than 10 μm , spacing $\geq 5 \mu\text{m}$.

3. Spacing between different layers

3.1 All layers:

- Spacing between edges of structures in different layers is usually $\geq 2.5 \mu\text{m}$.
- Exception in JJ: If area of I1A < area of I2A then distance $> 2.0 \mu\text{m}$.

3.2 Layers T1, I1B, and I2:

- Radius of octagonal area in T1 for JJs is 2.0 μm larger than the radius of window in isolation layer I1B. T1 and I2 coincide.

3.3 Layers T1 and M1:

- Distance to next edges below has to be $\geq 2.5 \mu\text{m}$.

3.4 Layers I1A and I1B:

- Radius of octagonal contact holes in I1B for JJs is 2.0 μm larger than the radius of JJs (I1A).
- For vias: spacing between I1B and I1A is $\geq 2.5 \mu\text{m}$.

3.5 Layers I1B and I2:

- Radius of octagonal contact holes in I2 for JJs is 2.0 μm larger than the radius of holes in I1B.
- For vias: spacing between I1B and I2 is $\geq 2.5 \mu\text{m}$.

3.6 Layers I1A and I2:

- Edges of contact holes in I1A may coincide with I2, if smallest size in via is defined by I1B.

3.7 Layers CUT, I0A, I0B, and I1A:

- Below CUT edges of I0A, I0B and I1A may coincide.
- If CUT, I0A, I0B, and I1A coincide, then CUT can cross structures in M0 or M1, but not both.

Process RSFQ1D-1.2

- Spacing Between I0A and I1A $\geq 2.5 \mu\text{m}$

3.8 Layers CUT, and T1:

- Spacing between CUT and T1 is $\geq 19 \mu\text{m}$.

3.9 Layers M2, and I1A:

- Radius of octagonal area in M2 for JJs is $2.5 \mu\text{m}$ larger than the radius of window in isolation layer I1A.

4. Overlap and crossing of edges between different layers

4.1 Vias:

- Overlap distance for metallisation to largest window in isolation/anodisation is $2.5 \mu\text{m}$.
- Via from M0 to M2 must include M1.

4.2 Layer T1:

- Crossing of any structure by T1 is not allowed.

4.3 Layer R1:

- It is only possible to connect R1 by M2 using holes in I2. Other crossings of any structure by R1 are not allowed.
- Distance to next edges below has to be $\geq 2.5 \mu\text{m}$.

4.4 Layers R1 and I2:

- Outside the connection with M2 the R1 has to be covered by I2.

4.5 Layers R1 and M2:

- In the contact hole of layer I2 the resistor has to be covered completely by M2. Overlap of M2 and R1 in the windows of I2 has to be $2.5 \mu\text{m}$ for shunting resistors and $5 \mu\text{m}$ for the bias current resistors.
- Crossings of R1 and M2 should be avoided as far as possible.

We offers Design Rules Check (DRC) for customers. The layouts will be checked before starting photo mask preparation.

5. Chip placement on wafer

The wafer size is 4 inch in diameter. One wafer contains 32 chips placed in the center, structures for photo mask alignment and a contact pad for the anodisation. The chip size is $12.8 \times 12.8 \text{ mm}^2$ with user area of $12.7 \times 12.7 \text{ mm}^2$, cf. appendix 3. The distance of 0.1 mm between different chips is necessary for cutting of the chips. For anodisation each chip has to be connected to a $100 \mu\text{m}$ wide wire between the chips. This has to be done in layer M0.

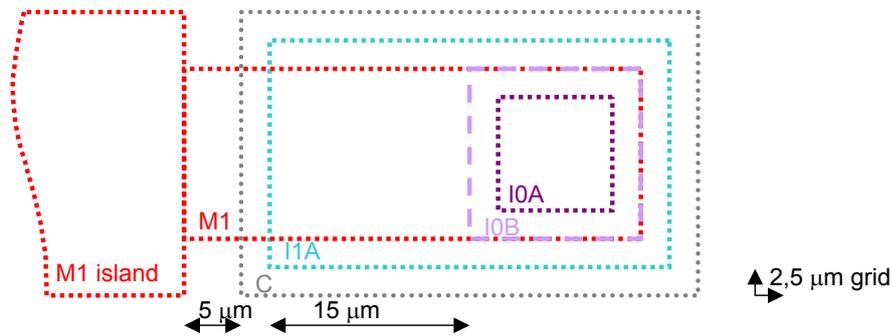
Our standard chip contains 48 contact pads each with a size of $0.65 \times 0.65 \text{ mm}^2$ and placed on chip edges on a $50 \mu\text{m}$ distance from the border the of chip. The distance between the centers of the contact pads is 1.005 mm .

Customers can realize their own chip dimensions. If wanted, customers can use library cells (JJs of different dimensions, shunted JJs, sections of Josephson Transmission Lines, chip outline, pads, ...).

Process RSFQ1D-1.2

6. Anodisation and cutting

Anodisation of the surface of Niobium is necessary for a good isolation between the metal layers. Therefore all structures in M0 have to be connected to the 50 μm wide wire around the chip. If this is not guaranteed by layout, this has to be done with additional wires. Later these additional wires have to be removed. The same has to be done for M1. In M1 it is also possible to make connections to M0. The additional wires for anodisation are removed by the cutting process step. To cut wires it is necessary to put a window for anodisation and isolation below the cut frame. That means for removing a bridge in M1 you have to put windows in I1A and CUT, for removing a bridge in M0 you have to put windows in I0A, I0B, I1A and CUT. The overlap of M0 or M1 and CUT must be more than 15 μm . The length of metal path between design structure and CUT window edge must be more than 5 μm . For anodisation M1 islands we recommend following structure.



Recommended design of a cut able contact structure for anodisation of M1

7. Requirements for GDS II file correctness

- GDS II files must be in BLOCK FORMAT, i.e. in size portions of 512 bytes (mostly by default),
- For POLYGONS (GDS II : BOUNDARIES) you can not use non-orientable self-intersecting polygons. Only orientable self-intersecting polygons (also called re-entrant boundaries) are allowed,
- DATATYPES are ignored,
- Zero width PATHS and TEXT can be used for documentation in layer TEXT,
- For physical text on the mask/wafer you can not use POLYGONS or PATHS, only GDS II TEXT in layer SMC (GDS II-No. 16). You can use font0, font1, font2, and font3 (without font names),
- TEXT will be represented on the mask/wafer by a simple rectangular font,
- Use only PATHTYPE 0 (normal) or 2 (extended), not PATHTYPE 1 (rounded),
- USER UNIT = 1x10E-6,
- RESOLUTION = 0.001 user unit.

Process RSFQ1D-1.2

D. Technology description:**1. Josephson junctions parameters**

| | Nominal value | Intra wafer tolerance | On wafer homogeneity | On chip homogeneity |
|------------------------------|------------------------|-----------------------|----------------------|---------------------|
| Josephson current density | 1000 A/cm ² | ± 20 % | ± 15 % | ≤ ± 5 % |
| Sheet resistance of Mo-layer | 1.0 Ω | ± 20 % | ± 10 % | ≤ ± 5 % |

2. Stripline inductance

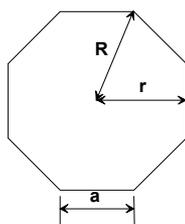
| Layer | L _{square} | Intra wafer tolerance | On wafer homogeneity | On chip homogeneity |
|-------------------|---------------------|-----------------------|----------------------|---------------------|
| M1-M0 | 0.52 pH | ± 10 % | ± 5 % | ≤ ± 2 % |
| M2-M1 (across M0) | 0.64 pH | ± 10 % | ± 5 % | ≤ ± 2 % |
| M2-M0 | 0.81 pH | ± 10 % | ± 6 % | ≤ ± 2 % |

Remarks:

- **Inductances** were measured in interferometers with micro strips of 100 μm length and 10 μm width.
- **London penetration depth** for magnetic field: (87 ± 5) nm.
- **Capacitance:** Measured value of specific capacitance (defined from Fiske steps; measurements at JJs with w = 10 μm l = 30 μm and 100 μm) is (0.05 ± 0.002)pF/μm².

3. Nominal values of area, critical current, diameter, and shunt resistor for JJs

| | | | | | | | |
|------------------------|-------|--------|--------|------|--------|-------|--------|
| A/μm ² | 12.5 | 17.7 | 20.6 | 23.8 | 30.8 | 36.7 | 59.9 |
| I _c /units* | 1.00 | 1.50 | 1.75 | 2.00 | 2.50 | 3.00 | 5.00 |
| I _c /μA | 125 | 187.50 | 218.75 | 250 | 312.50 | 175 | 625.00 |
| ∅/μm | 3.8 | 4.6 | 5.0 | 5.4 | 6.1 | 6.7 | 8.5 |
| C _J /pF | 0.625 | 0.885 | 1.03 | 1.19 | 1.54 | 1.835 | 3.0 |
| R _s /Ω** | 2.10 | 1.40 | 1.20 | 1.05 | .85 | .70 | .40 |



$$\emptyset = 2r$$

Remarks:

*The normalized I_c values are for developers using PSCAN. The unit I_c is 125 μA.

**The R_s value is calculated for adjusting β_c=1.

- JJs areas are realized as octagons.
- Measured ratios of critical currents are correct within ± 5 %.
- The nominal I_cR_n value is about 256μV.

Process RSFQ1D-1.2

E. Multi custom wafer rules:

To reduce costs we recommend to place designs of some customers together on one wafer. For decreasing the time of placement and better matching conditions:

- Send flat hierarchy designs including only the top cell
- Use chip size of 12.8mm x 12.8 mm, 6.4mm x 6.4mm or 5mm x 5mm
- Set the origin [point 0, 0] to the lower left corner and follow gds2 design rule [rule 7]

F. Future plans for improvement of the Niobium process:

At this time the development of our technology is still in progress. Therefore in the next release of our technology description some changes will be made.

G. Note:

Violation of the design rules may be permitted in special cases, e.g. for connections between trilayer and wiring.

H. Release Notes:

Version 1.1, Date 24.8.2005:

3.8 Layers CUT, and T1:

- Spacing between CUT and T1 is $\geq 19 \mu\text{m}$.

3.9 Layers M2, and I1A:

- Radius of octagonal area in M2 for JJs is $2.5 \mu\text{m}$ larger than the radius of window in isolation layer I1A.

Version 1.2, Date 22.06.2007

A. Photomaske: Column "Wafer resist"

2.3 Layer I0A, I0B, I1A, I1B, I2:

- Spacing Inside I0A, I1A $\geq 2.5 \mu\text{m}$

3.7 Layers CUT, I0A, I0B, and I1A:

- Spacing Between I0A and I1A $\geq 2.5 \mu\text{m}$

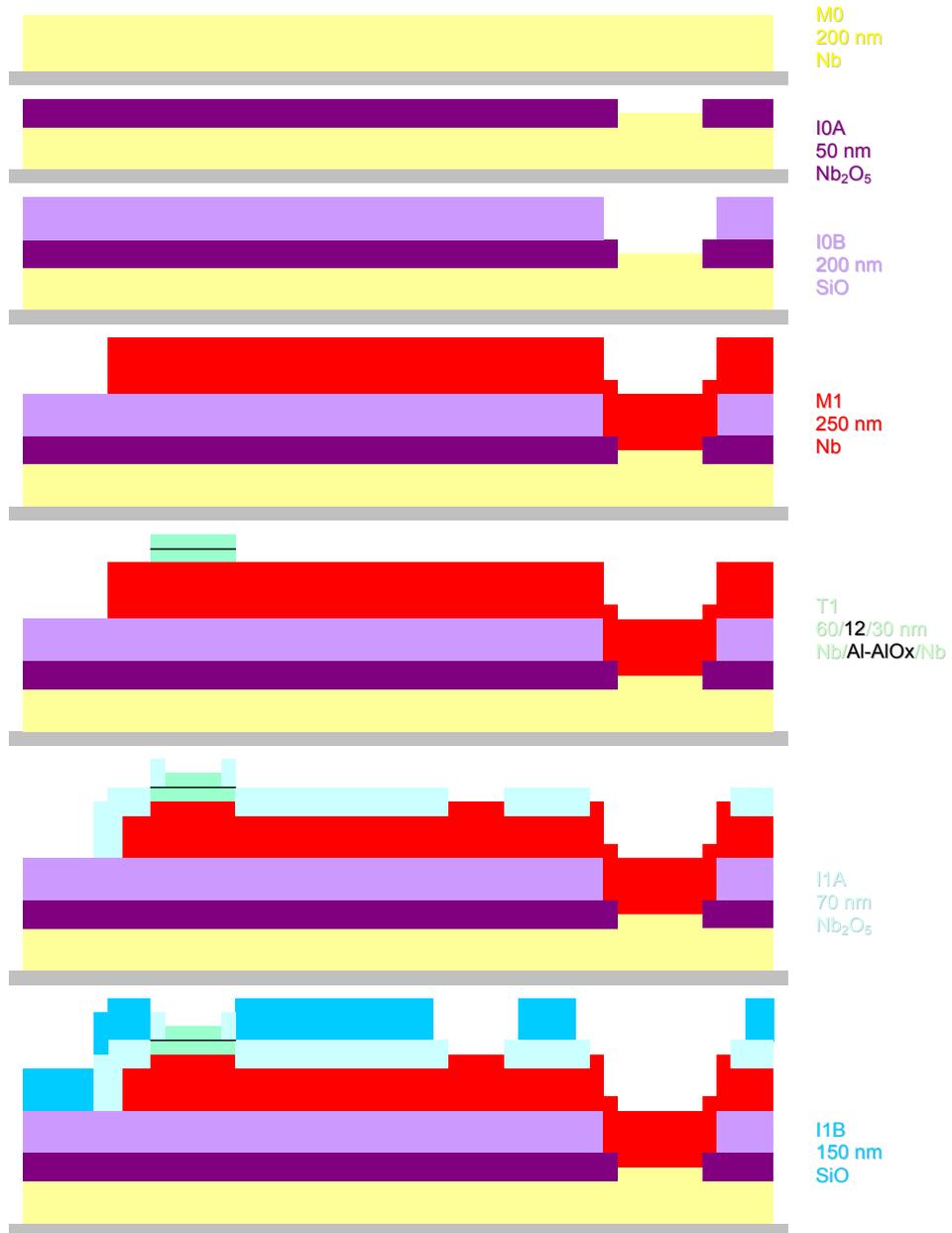
I. Appendix:

1. Contents of the FLUXONICS Foundry layout library

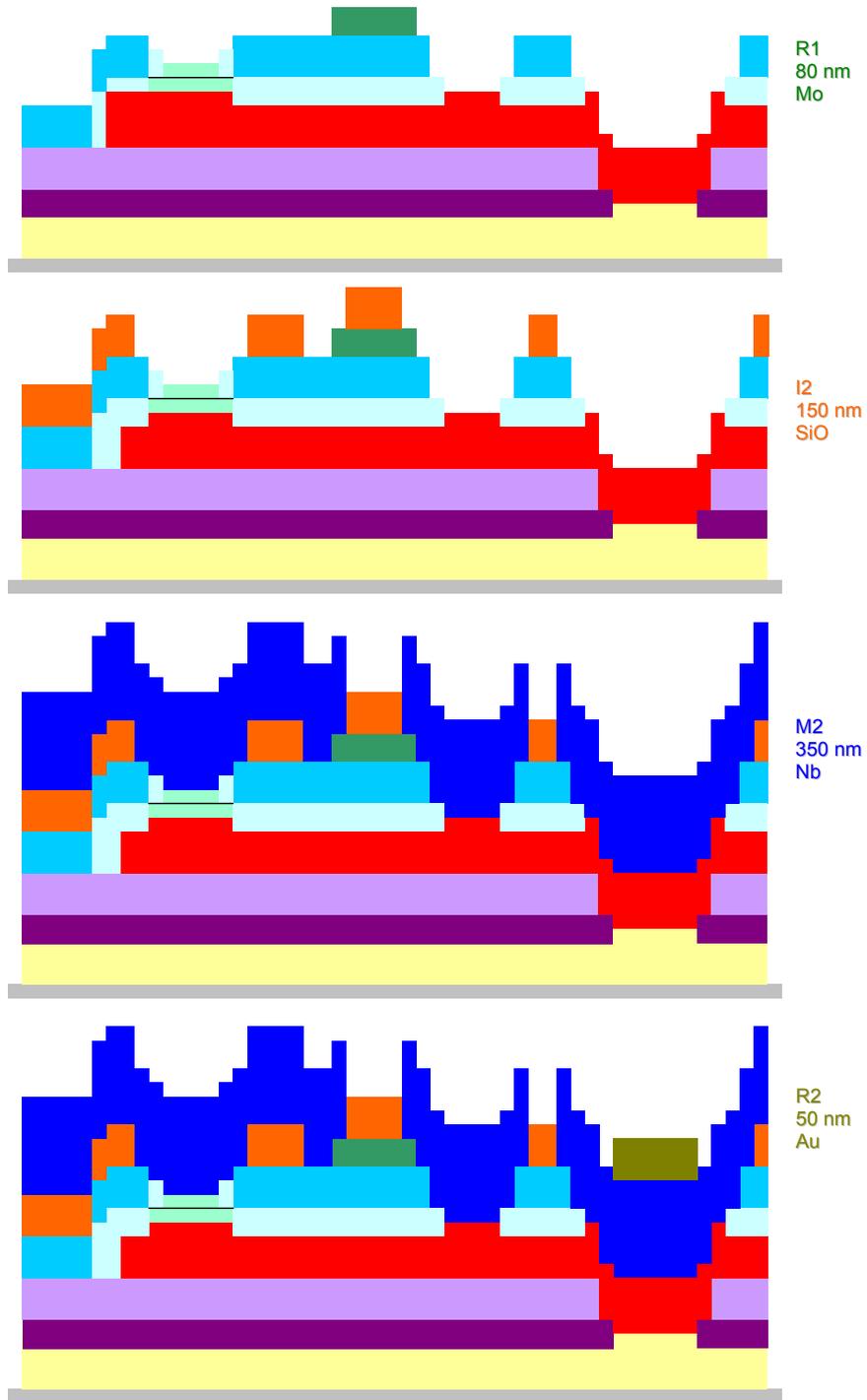
- Josephson Junctions, shunted and unshunted,
- Pads,
- Chip outline,
- Vias,
- Resistors,
- dc/SFQ & SFQ/dc (dc to Single Flux Quantum & Single Flux Quantum to dc) converters.

Process RSFQ1D-1.2

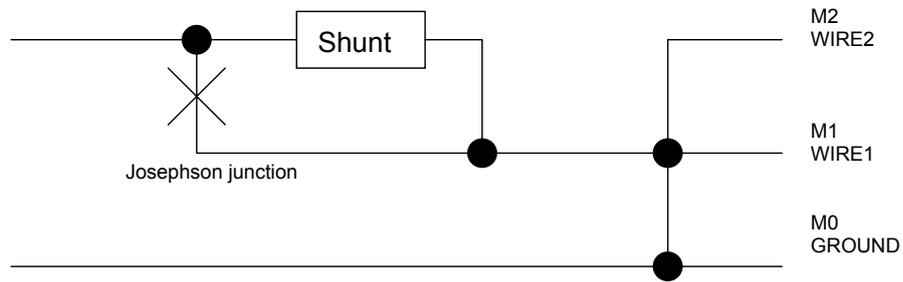
2. Cross section of RSFQ sandwich for the process RSFQ1D



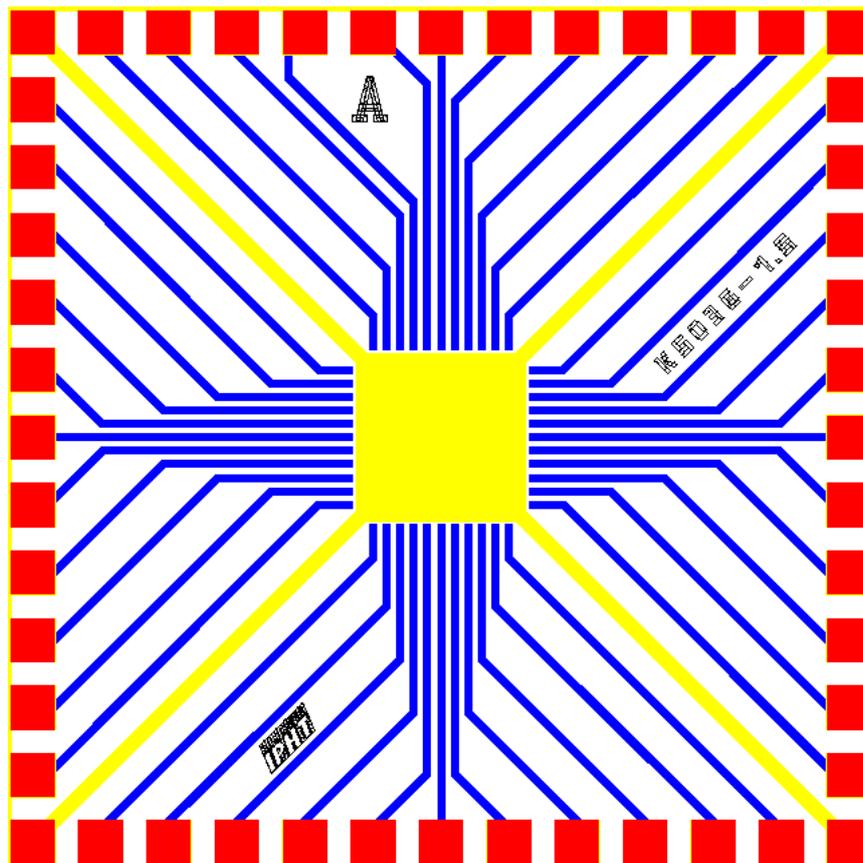
Process RSFQ1D-1.2



Process RSFQ1D-1.2



3. Standard RSFQ chip layout



The standard chip layout: dimensions 12.8 × 12.8 mm², 48 contact pads with dimensions 0.65 × 0.65 mm² each.

Appendix D

Hypres 4.5kA/cm² Process Design Rules



NIOBIMUM INTEGRATED CIRCUIT FABRICATION

PROCESS #03-10-45

DESIGN RULES

REVISION #24, JAN 11, 2008

Direct all inquiries, questions, comments and suggestions concerning these design rules and/or HYPRES fabrication to:

Sergey K. Tolpygo
Tel. (914) 592-1190 x7813, Fax (914) 347-2239, Email: stolpygo@hypres.com

Direct all inquiries concerning submission of design files for IC fabrication to:

Masoud Radparvar
Tel. (914) 592-1190 x7827, Fax (914) 347-2239, Email: masoud@hypres.com

Preface

HYPRES, Inc. has developed and sustains several fabrication processes for superconductor electronics. This document specifies the design rules of HYPRES fabrication process #03-10-45 for niobium-based superconducting integrated circuits. This information constitutes a self-contained guide to the physical layout of devices and circuits within the scope of the standard HYPRES fabrication process. Adherence to these rules will provide cost-effective, high yield designs.

1.0 General Description

- 1.1 This HYPRES IC fabrication process uses only refractory materials, with the exception of a Ti/Pd/Au metallization layer used primarily for contact pads. Niobium is used as the superconducting material due to its comparably high critical temperature, electrical and thermal stability, and ability to be thermally cycled many times without degradation. Niobium/Aluminum-Oxide/Niobium Josephson tunnel junctions are made by depositing an *in-situ* trilayer across the entire wafer and subsequently defining junction areas by 1x photolithography and etching. This method yields good uniformity and reproducibility of junction parameters.
- 1.2 HYPRES currently offers three processes with three different critical current densities of Nb/AIO_x/Nb trilayer: 0.03 kA/cm² (0.3 μA/μm²), 1.0 kA/cm² (10 μA/μm²), and 4.5 kA/cm² (45 μA/μm²).
- 1.3 The Josephson junctions can be interconnected into circuit configurations using four superconducting layers (junction base electrode (layer M1), two Nb wiring layers (layers M2 and M3) and superconducting Nb ground plane (layer M0)).
- 1.4 One normal metal layer is used to provide medium-value resistors, which can be used for shunting Josephson junctions, current distribution, etc. The sheet resistance of this layer is given in the table below for all three processes.
- | Process Jc | Sheet Resistance at 4.5K, Ohm/ | Material | Tc, K | Thickness, nm |
|-------------------------|--------------------------------|------------|-------|---------------|
| 0.03 kA/cm ² | 2.0±0.20 | Ti/AuPd/Ti | 0.0 | 100±10 |
| 1.0 kA/cm ² | 1.0±0.15 | Mo | 0.9 | 70±10 |
| 4.5 kA/cm ² | 2.1±0.3 | Mo | 0.9 | 40±6 |
- 1.5 Silicon dioxide is deposited to provide insulation between the conducting layers. Anodization of the base electrode of trilayer provides additional insulation to Josephson junctions.
- 1.6 Our standard fabrication process uses 6-inch (150 mm) diameter oxidized Si wafers.
- 1.7 HYPRES Niobium Process Flow Overview

| # | Layer | GDS# | Mask polarity | Description |
|----|-------|------|---------------|--|
| | | | | Nb deposition |
| 1 | M0 | 30 | - | M0 patterning (holes in niobium ground plane) |
| | | | | SiO ₂ deposition |
| 2 | I0 | 31 | - | Contact (via) between M1 and ground plane |
| | | | | Nb/AIO _x /Nb trilayer deposition (see 1.2) |
| 3 | I1A | 2 | + | Counter-electrode (junction area) definition for 0.03 or 1.0 kA/cm ² process. |
| 3a | I1C | 4 | + | Counter-electrode (junction area) definition for 4.5 kA/cm ² process. |
| | | | | Base electrode anodization |
| 4 | A1 | 5 | + | Anodization layer patterning |
| 5 | M1 | 1 | + | Trilayer base electrode patterning |
| | | | | SiO ₂ deposition |
| | | | | Resistive layer deposition (see 1.4) |
| 6 | R2 | 9 | + | Resistor patterning |
| | | | | SiO ₂ deposition |
| 7 | I1B | 3 | - | Contact (via) between M2 and (I1A, R2, or M1) |
| | | | | Nb deposition |
| 8 | M2 | 6 | + | M2 layer patterning |
| | | | | SiO ₂ deposition |
| 9 | I2 | 8 | - | Contact (via) between M2 and M3 |
| | | | | Nb deposition |
| 10 | M3 | 10 | + | M3 layer patterning |
| | | | | Ti/Pd/Au contact metallization deposition |
| 11 | R3 | 11 | + | Contact pad patterning |

2.0 Layout Design Rules

2.1 Minimal size and spacing for each layer is specified in the following table.

| 1 | M0 | Negative ⁽¹⁾ | μm | 6 | R2 | Positive | μm |
|---|--------------------|--------------------------------|--------------------|----|------|--------------------------------|--------------------|
| | 1.1 | M0 spacing to M0 | 2.0 | | 6.1 | R2 spacing to R2 | 2.0 |
| | 1.2 | M0 minimal size ⁽⁵⁾ | 2.0 | | 6.2 | R2 minimal size ⁽⁵⁾ | 3.0 |
| | 1.3 | M0 spacing to I0 | 1.5 | | 6.3 | R2 surround I1B | 1.5 |
| | 1.4 | M0 spacing to M1 | 1.0 | | 6.4 | R2 spacing to M2 | 1.0 ⁽³⁾ |
| | 1.5 | M0 spacing to R2 | 1.5 ⁽³⁾ | 7 | I1B | Negative | |
| 2 | I0 | Negative | | | 7.1 | I1B spacing to I1B | 2.0 |
| | 2.1 | I0 minimal size | 2.5 | | 7.2 | I1B minimal size | 2.0 |
| | 2.2 | I0 spacing to I1A | 1.5 ⁽²⁾ | | 7.3 | I1B surrounded by M2 | 1.5 |
| | 2.3 | I0 surrounded by M1 | 1.5 | 8 | M2 | Positive | |
| | 2.4 | I0 spacing to R2 | 1.0 | | 8.1 | M2 spacing to M2 | 2.5 |
| 3 | I1A ⁽⁴⁾ | Positive | | | 8.2 | M2 minimal size ⁽⁵⁾ | 2.0 |
| | 3.1 | I1A spacing to I1A | 2.0 | | 8.3 | M2 surround I2 | 1.5 |
| | 3.2 | I1A minimal size | 1.5 | 9 | I2 | Negative | |
| | 3.3 | I1A surrounded by A1 | 1.0 | | 9.1 | I2 minimal size | 3.0 |
| | 3.4 | I1A spacing to M1 | 1.5 | | 9.2 | I2 surrounded by M3 | 1.5 |
| | 3.5 | I1A spacing to R2 | 0.5 | 10 | M3 | Positive | |
| 4 | A1 | Positive | | | 10.1 | M3 spacing to M3 | 2.5 |
| | 4.1 | A1 spacing to A1 | 2.0 | | 10.2 | M3 minimal size ⁽⁵⁾ | 2.0 |
| | 4.2 | A1 minimal size | 2.0 | | 10.3 | M3 contact width with R3 | 3.0 |
| | 4.3 | A1 surrounded by M1 | 0.5 | 11 | R3 | Positive | |
| | 4.4 | A1 spacing to R2 | 0.5 | | 11.1 | R3 spacing to R3 | 5.0 |
| | 4.5 | A1 surround I1A or I1C | 1.0 | | 11.2 | R3 minimal size ⁽⁵⁾ | 3.0 |
| | 4.5 | A1 surround I1B | 1.5 | | | | |
| 5 | M1 | Positive | | | | | |
| | 5.1 | M1 spacing to M1 | 2.5 | | | | |
| | 5.2 | M1 minimal size ⁽⁵⁾ | 2.5 | | | | |
| | 5.3 | M1 spacing to R2 | 1.0 ⁽³⁾ | | | | |
| | 5.4 | M1 surround I1B | 1.5 | | | | |

(1) "Negative" (dark-field) mask means, that the corresponding physical layer on the wafer will be removed from the design area. "Positive" (clear-field) mask means, that the physical layer will remain on the wafer in the design area.

(2) HYPRES cannot guaranty the quality (*V_m*, etc.) and the precise critical current (*I_c*) of junctions residing in I0 hole. I1A patterns may not overlap with I0 patterns.

(3) R2 patterns may not cover steps (M0, I0, or M1). We also recommend avoiding unnecessary crossings between M2 and R2 patterns.

(4) All rules for layer I1C are the same as for I1A.

(5) Minimal size is the minimal size of the real object (not mask), please see table 3.1 for bias value

3.0 Physical Layer Process Specifications

3.1 Since the fabrication process involves projection photolithography and etching, the size of structures on the wafer may differ somewhat from the design layout (*i.e.* feature size on the photomask). This change in size is called “bias”. In the table below, the bias is defined as the shift of the object’s border due to its enlargement/reduction relatively to its image on the mask. A positive bias means larger objects on the wafer than in the design.

| Layer | Material | Bias (3.1), μ | Physical layer properties: Resistance, Capacitance, etc. | Thickness nm |
|----------|--------------------------------|-------------------|--|--------------|
| M0 | Nb | 0.2±0.2 | Nb, superconductor. Penetration depth $\lambda_L = 90$ nm | 100±10 |
| I0 | SiO ₂ | 0.2±0.2 | SiO ₂ , insulator. Capacitance: 0.28 fF/ $\mu\text{m}^2 \pm 20\%$ | 150±15 |
| M1 | Nb | 0.0±0.1 | Trilayer base electrode, superconductor. $\lambda_L = 90$ nm | 135±10 |
| I1A, I1C | AlO _x /Nb | 0.0±0.1 | Trilayer counter electrode and tunnel barrier (see 3.2 and 3.3) | 50±5 |
| A1 | Nb ₂ O ₅ | | Insulation on top of the base electrode surrounding I1A | 40±5 |
| | SiO ₂ | | SiO ₂ , insulator. Capacitance: 0.42 fF/ $\mu\text{m}^2 \pm 20\%$ | 100±10 |
| R2 | | 0.0 ± 0.2 | (see table in 1.4) | |
| | SiO ₂ | | SiO ₂ insulator. Capacitance: 0.42 fF/ $\mu\text{m}^2 \pm 20\%$ | 100±10 |
| I1B | | - 0.1 ± 0.2 | Contact hole through the above two SiO ₂ layers | |
| M2 | Nb | - 0.2 ± 0.1 | Nb, superconductor. Penetration depth $\lambda_L = 90$ nm ±5% | 300±20 |
| | SiO ₂ | | SiO ₂ insulator. Capacitance: 0.08 fF/ $\mu\text{m}^2 \pm 20\%$ | 500±40 |
| I2 | | 0.1 ± 0.2 | Contact hole through the above insulator | |
| M3 | Nb | - 0.4 ± 0.2 | Nb, superconductor. Penetration depth: $\lambda_L = 90$ nm ±5% | 600±50 |
| R3 | Ti/Pd/Au | 0.0 ± 1.0 | Contact pads metallization | 350±60 |

3.2 We recommend using Josephson junctions of **circular** shape. The deviation of the radius of the circle in I1A (I1C) layer is within +/- 0.1 μm (see table 3.1). HYPRES **does not guarantee** high accuracy area for the small objects of other shapes in I1A or I1C layer.

3.3 The dependence of JJ specific capacitance vs. critical current density can be approximated by the following formula:

$$C_s = \frac{1.0}{24.7 - 2.0 \cdot \ln j_c} \quad (\text{pF} / \mu\text{m}^2)$$

here, C_s is specific capacitance in pF/ μm^2 and j_c is critical current density in $\mu\text{A}/\mu\text{m}^2$.

This gives us roughly 50 fF/ μm^2 at 10.0 $\mu\text{A}/\mu\text{m}^2$, 59 fF/ μm^2 at 45.0 $\mu\text{A}/\mu\text{m}^2$, and 37 fF/ μm^2 at 0.3 $\mu\text{A}/\mu\text{m}^2$. That is in a good agreement with the experimental data.

3.4 The critical current per micron width for Nb films is given in the following table

| Nb Layer | M0 | M1 | M2 | M3 |
|----------------------------|------|------|------|------|
| I_c (mA/ μm) | 20.0 | 30.0 | 50.0 | 70.0 |

If the wire crosses over steps, its I_c may drop by more than 50%. Please, see the minimal width of a wire in table 2.1 and the bias in table 3.0 before designing current transmitting lines.

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4.0 Lithography features

4.1 Mask Grid Size

| Mask | Layer | Grid Size [μm] |
|------|----------|-----------------------------|
| M0 | Negative | 0.5 |
| I0 | Negative | 0.5 |
| M1 | Positive | 0.5 |
| I1A | Positive | 0.1 |
| I1C | Positive | 0.1 |
| A1 | Positive | 0.5 |
| R2 | Positive | 0.5 |
| I1B | Negative | 0.1 |
| M2 | Positive | 0.5 |
| I2 | Negative | 0.5 |
| M3 | Positive | 0.5 |
| R3 | Positive | 0.5 |

4.2 Layers I1A, I1C and I1B have a grid size of 0.1 μm . All remaining layers must use a grid size of 0.5 μm . Every vertex coordinates are being rounded up to a multiple of these numbers.

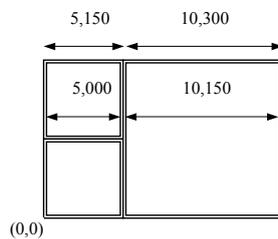
4.3 All layouts are **mirror imaged** when printed on wafers.

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5.0 Designs Submission Formats

- 5.1 The layout file must be in GDS-II format.
- 5.2 Please submit designs to HYPRES through File Transfer Protocol (FTP) at <ftp://customer@ftp.hypres.com> or, if the size of the file is **less than 10 MB**, via E-mail to masoud@hypres.com.
- 5.3 The active chip area is limited by 5000 μm x 5000 μm and surrounded by 150- μm dicing channels. Dicing channels between chips are 150 μm wide. That means that 75 μm on each side of each die is consumed in dicing. No objects are allowed in the dicing channel.
- 5.4 It is also allowed to submit 1-cm chips. In this case, the die size is 10.3 mm x 10.3 mm and the actual size of the chip is 10.15 mm x 10.15 mm. All other sizes should be negotiated with HYPRES prior the submission.
- 5.5 When delivering layouts to HYPRES, send **only one file**, with all chips placed together in a single “supercell” with **5150- μm** grid. The “supercell” should be a cluster of chips (see example below), with the lower left corner of the cluster placed at (0, 0). The super cell area should therefore be exactly 5150 x 5150 x $N \times M$, where $N \times M$ is the number of chips.



- 5.6 **No cell name may exceed 60 characters.** Cell names will be truncated to this size automatically and might clobber other cells.

6.0 Cycle Time

- 6.1 One week is required to fabricate the photo masks.
- 6.2 Six weeks are required to process wafers.
- 6.3 Two days are required for dicing, Process Control Monitor testing, and packaging of chips.
- 6.4 Total cycle time is 8 weeks and 2 days from mask release. Note: Cycle times may change depending upon customer requirements.
- 6.5 On average HYPRES has 8 mask releases per year. See www.hypres.com for up-to-date information and schedules.