# A fixed switching frequency technique for finite-control-set model predictive control for the control of single-phase converters

by

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*Dissertation presented for the degree of Doctor of Philosophy in Engineering in the Faculty of Engineering at Stellenbosch University*

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# Declaration

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# Uittreksel


## 'n Vaste skakelfrekwensieskema vir eindige beheerversameling modelgebaseerde voorspellende beheer vir die beheer van enkelfase drywingselektroniese omsetters

*("A fixed switching frequency technique for finite-control-set model predictive control for the control of single-phase converters")*

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'n Vasteskakelfrekwensieskema vir eindige beheerversameling modelgebaseerde voorspellende beheer word aangebied ten einde 'n vaste skakelfrekwensie te bewerkstellig wat goed vergelyk met pulsewydtemodulasie-gebaseerde lineêre beheer, terwyl die voordele van modelgebaseerde voorspellende beheer terselfdertyd behou word. Die beheerder word in twee dele opgedeel, nl. die vooraf berekening en stoor van die voorspellingsvergelykings se koëffisiënte en die aanlynevaluering van die beheerder. 'n Vergelyking vir die gemiddelde waarde oor een of meer skakelperiodes word vooraf bereken vir elke geldige skakelkeuse en elke monster-stap in die skakelperiode en dit word dan in 'n opkyktabel gestoor. Die aanlynbeheerder gebruik hierdie opkyktabel om die korrekte voorspellingsvergelykings te laai, gebaseer op die huidige posisie in die skakelperiode. Hierdie strategie verminder die aanlyn-berekeningskoste sodat 'n hoër monsterfrekwensie met 'n langer voorspellingshorison bereik kan word.

Die beheerder word eksperimenteel geverifieër vir die uittreespanningsbeheer en intreebusstabilisering van 'n 12.75 kV mediumspanning elektroniese spanningsreguleerder sodat mediumspanningsdistribusievoerders gereguleer kan word. Die gedetaileerde ontwerp van die spanningsreguleerder word volledig behandel en bestaan uit 'n multivlak WS-na-WS-omsetter wat in 'n newe-serie konfigurasie aan 'n transformator gekoppel is. Die lekinduktansie van die transformator en die intreebuskapasitor skep 'n $LC$-intreefilter wat kan

resoneer. Simulasie en eksperimentele resultate wys dat die beheerder 'n vaste skakelfrekwensie handhaaf met 'n goeie uittree-spanningsgolfvorm en oorgangsgedrag terwyl die resonante gedrag onderdruk word.

Daar word verder gewys dat die beheerder veralgemeen kan word. Hiervoor word die beheerder gedemonstreer vir die uittree-spanningsbeheer en die aktiewe kapasitor balansering van 'n vlieëndekapasitor-omsetter met 'n $LC$-uittreefilter. Eksperimentele resultate wys dat die beheerder 'n vaste skakelfrekwensie handhaaf met vinnige oorgangsgedrag en 'n goeie uittreegolfvorm met 'n lae THD terwyl die vlieënde kapasitore aktief gebalanseer word.

Laastens word die beheerder se prestasie met 'n pulswydtemodulasie-gebaseerder lineêre beheerder vergelyk. Die twee beheerders word omvattend deur simulasie geëvalueer en die resultate wys dat die voorspellende beheerder goed vergelyk met die lineêre beheerder in terme van golfvormkwaliteit en oorgangsgedrag.

# Abstract


## A fixed switching frequency technique for finite-control-set model predictive control for the control of single-phase converters

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A fixed switching frequency scheme for finite-control-set model predictive control is presented. The purpose of the control scheme is to achieve an output waveform quality that compares well to that of a pulse-width-modulator-based linear controller, while retaining the benefits of model predictive control such as the ability to easily control multiple variables without complex control loops. By enforcing a fixed switching frequency it becomes easier to ensure that resonant poles are not excited and assists with EMI compliance. The controller is divided into two parts: The off-line calculation and storage of the coefficients of the prediction equations and the on-line evaluation of the controller. For every valid actuation choice at each sampling step in the switching period, an equation for the average value over one or more switching periods is calculated and stored in a lookup table. The on-line controller uses the lookup table to load the appropriate equations, based on the current position within the switching period. This reduces the on-line calculation effort and allows higher sampling rates to be achieved while predicting over a long prediction horizon.

The controller is implemented and experimentally verified for the voltage control and input-bus stabilisation of a 12.75 kV medium voltage electronic voltage regulator for the regulation of medium voltage distribution feeders. The voltage regulator design is discussed in detail and consists of a multi-level AC-to-AC converter topology that is connected in a shunt-series configuration to an appropriate transformer. The leakage inductance of the transformer together with the large input-bus capacitor forms an input $LC$-filter that may become resonant. It is shown through simulation and experimental

results that the controller is able to maintain a fixed switching frequency with good reference tracking and waveform quality while suppressing the input-bus resonance.

It is further shown that the control scheme can be generalised. This is experimentally demonstrated for the voltage control and capacitor balancing of a five-level flying capacitor converter with an output $LC$ filter. The results show that the controller is able to maintain a fixed switching frequency with a fast transient response, a good waveform quality with a low THD while also actively keeping the flying capacitor voltages balanced.

Lastly, the controller is compared to a pulse-width-modulator-based linear resonant regulator for the current control of a single-leg inverter. The two controllers are extensively evaluated through simulation and the results show that the model predictive controller compares well to the linear controller in terms of waveform quality and transient response.

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# Contents

# List of Figures

# List of Tables

# Publications

## Conference papers

### Authored

- D. M. Tomlinson, T. Mouton, R. M. Kennel and P. Stolze, *"Model predictive control of an ac to ac converter with input and output LC filter."*, Industrial Electronics and Applications (ICIEA), 2011 6th IEEE Conference on , vol., no., pp.1233,1238, 21-23 June 2011

- Males Tomlinson, Dewald Abrie and Toit Mouton, *"Series-Stacked Medium Voltage Electronic Voltage Regulator."*, Energy Conversion Congress and Exposition (ECCE), 2011 IEEE , vol., no., pp.1087,1093, 17-22 Sept. 2011

- Males Tomlinson, Toit Mouton,Ralph Kennel and Peter Stolze. *"Model Predictive Control with a Fixed Switching Frequency for an AC-to-AC Converter"*, Industrial Technology (ICIT), 2013 IEEE International Conference on , vol., no., pp.570,575, 25-28 Feb. 2013

- Males Tomlinson, Toit Mouton,Ralph Kennel and Peter Stolze. *"Model Predictive Control with a Fixed Switching Frequency for a 5-level Flying Capacitor Converter"*, ECCE Asia Downunder (ECCE Asia), 2013 IEEE , vol., no., pp.1208,1214, 3-6 June 2013

- Males Tomlinson, Toit Mouton,Ralph Kennel and Peter Stolze. *"A generic approach to implementing finite-set model predictive control with a fixed switching frequency"*, Industrial Electronics (ISIE), 2014 IEEE 23rd International Symposium on, vol., no., pp.330,335, 1-4 June 2014

- Males Tomlinson, Toit Mouton and Ralph Kennel. *"Finite-Control-Set Model Predictive Control with a Fixed Switching Frequency vs. Linear Control for Current Control of a Single-leg Inverter"*, Sensorless Control for Electrical Drives and Predictive Control of Electrical Drives and Power Electronics (SLED/PRECEDE), 2015 IEEE International Symposium on, Oct 2015

**Co-authored**

- Peter Stolze, Daniël du Toit, Males Tomlinson, Ralph Kennel and Toit Mouton, *"Predictive Torque Control of an Induction Machine Fed by a Flying Capacitor Converter."*, IEEE Africon 2011.
- Peter Stolze, Daniël du Toit, Males Tomlinson, Ralph Kennel and Toit Mouton, *"Model Predictive Control of a Flying Capacitor Converter with Output LC Filter for UPS Applications."*, IEEE Africon 2011.
- Peter Stolze, Mathias Kramkowski , Toit Mouton, Males Tomlinson and Ralph Kennel, *"Increasing the Performance of Finite-Set Model Predictive Control by Oversampling"*, IEEE International Conference on Industrial Technology, 2013
- Toit Mouton, Peter Stolze, Tobias Geyer, Males Tomlinson, Ralph Kennel, *"Predictive control vs. linear control for current control of a single-leg inverter"*, Sensorless Control for Electrical Drives and Predictive Control of Electrical Drives and Power Electronics (SLED/PRECEDE), 2013 IEEE International Symposium on, Oct 2013
- Stolze, P. and Karamanakos, P. and Tomlinson, M. and Kennel, R. and Mouton, T. and Manias, S., *"Heuristic variable switching point predictive current control for the three-level neutral point clamped inverter"*, Sensorless Control for Electrical Drives and Predictive Control of Electrical Drives and Power Electronics (SLED/PRECEDE), 2013 IEEE International Symposium on, Oct 2013
- Peter Stolze, Males Tomlinson, Ralph Kennel and Toit Mouton, *"Heuristic finite-set model predictive current control for induction machines"*, ECCE Asia Downunder (ECCE Asia), 2013 IEEE

## Journal papers

- Males Tomlinson, Toit Mouton, Ralph Kennel and Peter Stolze. *"A fixed switching frequency scheme for finite-control-set model predictive control - Concept and algorithm "*, Accepted for Transactions on Industrial Electronic, 2016 IEEE

# Nomenclature

### Notation conventions and definitions

| | |
|---|---|
| $a$ | Scalar |
| $A$ | Scalar |
| $\mathbf{A}$ | Matrix |
| $\mathbf{a}$ | Vector |
| $\dot{a}$ | The time derivative $\frac{\mathrm{d}a}{\mathrm{d}t}$ of the variable |
| $\dot{\mathbf{a}}$ | The time derivative $\frac{\mathrm{d}\mathbf{a}}{\mathrm{d}t}$ of the vector |
| $=$ | Equality |
| $\in$ | Is an element of, belongs to |
| $\cdot$ | A general place holder for any variable or expression |
| $\{\cdot\}$ | Set |
| $[\cdot]$ | Matrix or row vector |
| $\ldots$ | "and so forth" in a horizontal direction |
| $\vdots$ | "and so forth" in a vertical direction |
| $\ddots$ | "and so forth" in a diagonal direction |

### Abbreviations

| | |
|---|---|
| AC | Alternating current |
| ADC | Analogue to digital converter |
| BOD | Break-over diode |
| CCS-MPC | Continuous control set model predictive control |
| CMRR | Common-mode rejection rate |
| DC | Direct current |
| DESAT | Desaturation |
| D-MPC | Direct model predictive control |
| DPC | Direct power control |
| DTC | Direct torque control |
| EMF | Electromotive force |
| EMI | Electromagnetic interference |
| ESR | Equivalent series resistance |

| | |
|---|---|
| FCC | Flying capacitor converter |
| FCS-MPC | Finite-control-set model predictive control |
| FFT | Fast Fourier transform |
| FIR | Finite impulse response |
| FOC | Field-oriented control |
| FPGA | Field-programmable gate array |
| GPC | Generalised predictive control |
| I/O | Input-output |
| IC | Integrated circuit |
| IGBT | Insulated-gate bipolar transistor |
| IIR | Infinite impulse response |
| KLV | Kirchhoff's voltage law |
| LCD | Liquid crystal display |
| LED | Light emitting diode |
| LPF | Low pass filter |
| LV | Low voltage |
| MIMO | Multiple-input multiple-output |
| MOSFET | Metal-oxide field-effect transistor |
| MPC | Model predictive control |
| MV | Medium voltage |
| MVEVR | Medium voltage electronic voltage regulator |
| OPP | Optimized pulse pattern |
| P-DPC | Predictive direct power control |
| PI | Proportional integral |
| PWM | Pulse width modulation |
| RMS | Root mean square |
| SAH | Sampling and hold |
| SISO | Single-input single-output |
| SMC | Sliding mode control |
| SNR | Signal to noise ratio |
| SVM | Space vector modulation |
| THD | Total harmonic distortion |
| VAC | Voltage (alternating current) |
| VDC | Voltage (direct current) |
| VOC | Voltage-oriented control |
| ZOH | Zero-order hold |

## Variables

*Converter modelling:*

| | |
|---|---|
| $C$ | Capacitance [F] |
| $L$ | Inductance [H] |
| $R$ | Resistance [Ω] |
| $C_{bus}$ | Bus capacitance [F] |
| $C_s$ | Snubber capacitance [F] |
| $C_o$ | Output filter capacitance [F] |
| $C_F$ | Flying capacitance [F] |
| $L_{eq}$ | Equivalent input inductance (including leakage inductance) [H] |
| $L_o$ | Output filter inductance [H] |
| $R_{load}$ | Load resistance [Ω] |
| $R_b$ | Bleeding or equivalent parallel resistance [Ω] |
| $R_{esr}$ | Equivalent series resistance [Ω] |
| $R_{C_F}$ | Flying capacitor equivalent series resistance [Ω] |
| $R_{C_o}$ | Filter capacitor equivalent series resistance [Ω] |
| $R_{C_{bus}}$ | Bus capacitor equivalent series resistance [Ω] |
| $R_{L_o}$ | Filter inductor equivalent series resistance [Ω] |
| $R_{L_{eq}}$ | Input inductor equivalent series resistance [Ω] |
| $v_{DC}$ | DC voltage source [V] |
| $v_{bus}$ | Scalar DC-bus voltage [V] |
| $v_t$ | Scalar terminal voltage at transformer secondary windings [V] |
| $v_p$ | Scalar input voltage at the primary terminals of the transformer [V] |
| $v_{out}$ | Scalar output or load voltage [V] |
| $i_{in}$ | Scalar input current [A] |
| $i_{L_o}$ | Scalar current through filter inductor $L_o$ [A] |
| $i_{out}$ | Scalar output or load current [A] |
| $e_s$ | Scalar sinusoidal voltage source [$V_{RMS}$] |
| $T_x$ | Power electronic switch with gate driver signal $x$ |
| $\overline{T_x}$ | Power electronic switch with inverted gate driver signal $x$ |
| $\omega$ | Resonant frequency (filter design) [rad/s] |
| $\omega_n$ | Natural undamped resonant frequency (filter design) [rad/s] |
| $\zeta$ | Damping ratio (filter design) |

*Model predictive controller design:*

| | |
|---|---|
| $T_{sw}$ | Switching period [s] |
| $T_s$ | Sampling period [s] |
| $N$ | Number of sampling steps $T_s$ in the switching period $T_{sw}$ |

| | |
|---|---|
| $n$ | Step counter for indicating the step position in $N$ (unless defined otherwise) |
| $w$ | Weighting factor |
| $s_x$ | Scalar switching function that is applied to the gate drive signal $x$ |
| $\mathbf{S}$ | Switching vector containing the individual switching functions |
| $S_N$ | The number of unique switching states that can be represented by $\mathbf{S}$ |
| $\sigma_N$ | The number of switching transitions in each switching period |
| $d$ | Duty cycle |
| $L$ | Prediction level: Indicates the vertical axis on the two-dimensional plane with regions |
| $L_N$ | The number of prediction levels on the vertical axis on the two-dimensional plane with regions |
| $C$ | Number of PWM carriers |
| $\mathbf{A_s}$ | Continuous-time state-space matrix describing the switching vector $\mathbf{S}$ |
| $\mathbf{B_s}$ | Continuous-time state-space matrix describing the switching vector $\mathbf{S}$ |
| $\mathbf{C_s}$ | Continuous-time state-space matrix describing the switching vector $\mathbf{S}$ |
| $\mathbf{D_s}$ | Continuous-time state-space matrix describing the switching vector $\mathbf{S}$ |
| $\mathbf{F_s}$ | Discrete-time state-space matrix describing the switching vector $\mathbf{S}$ |
| $\mathbf{G_s}$ | Discrete-time state-space matrix describing the switching vector $\mathbf{S}$ |
| $\mathbf{x}$ | State vector |
| $\bar{\mathbf{x}}$ | Predictor-estimate of the state vector |
| $\tilde{\mathbf{x}}$ | State-estimate error |
| $\hat{\mathbf{x}}$ | Current-estimate of the state vector |
| $\mathbf{x}^*$ | State vector reference input |
| $\mathbf{x}^*_{av}$ | Average value of the state vector reference input |
| $\mathbf{x}^p$ | Predicted state vector |
| $\mathbf{x}^p_{av}$ | Average value of the predicted state vector over the prediction period |
| $\mathbf{u}$ | State-space input vector |
| $\mathbf{y}$ | State-space output vector |
| $\mathbf{\Lambda_s}$ | Off-line calculation prediction-coefficient matrix in state-space form |
| $\mathbf{\Gamma_s}$ | Off-line calculation prediction-coefficient matrix in state-space form |

### Subscripts

| | |
|---|---|
| $\mathbf{S}$ | Indicates that the variable corresponds the switching vector $\mathbf{S}$ |
| $av$ | Average value |

### Matrix operations

| | |
|---|---|
| $\mathbf{I}$ | Identity matrix of appropriate dimension |
| $\mathbf{A}^{-1}$ | Inverse of a matrix |

# Chapter 1

# Introduction

Model predictive control (MPC) is a technique that has been successfully used in industrial process control for many years. The use of MPC was possible since the time constants in these processes were sufficiently long to give the more primitive micro controllers ample time to do the calculations. Within the last ten years, model predictive control of power electronics gained new interest with the technological advancement of micro controllers and FPGAs. As the processing power and complexity of these devices improved, it allowed more complex calculations to be done in real-time. For MPC, this allowed the implementation of faster controllers with higher sampling rates and higher switching frequencies while controlling multiple state variables.

A subset of MPC, Finite-Control-Set Model Predictive Control (FCS-MPC), has gained recent popularity for its ability to control multiple state variables without the need for complex control loops. This proved especially useful for the control of multi-level converters and electrical motor drive systems. However, FCS-MPC is typically characterised by a variable switching frequency and obtaining an output waveform quality that compares well to that of PWM remains a challenge.

In this dissertation, a fixed switching frequency scheme for FCS-MPC is presented to achieve an output waveform quality that compares well to that of a PWM controller, while retaining the benefits of MPC. This controller is implemented for the control of a 12.75 kV medium voltage electronic voltage regulator for medium voltage distribution feeders. The voltage regulator consists of a multi-level AC-to-AC converter topology that is connected in a shunt-series configuration to an appropriate transformer. The control scheme is developed as a generalised scheme and further evaluated for the voltage control and capacitor balancing of a five-level flying capacitor converter. Finally, the controller is compared to a PWM-based linear PI controller for current control of a single leg inverter.

## 1.1 Research statement

This study focuses on the development of a fixed switching frequency technique for Finite-Control-Set Model Predictive Control (FCS-MPC). A method is presented to achieve a fixed switching frequency by using the waveform characteristics of PWM carriers to define prediction regions, where only a specific switching transition is allowed within each region. In order to maintain a fixed switching frequency as well as accurate reference tracking over the entire range of the controlled variables, the controller is sampled at a much higher rate than the desired switching frequency. It is possible to predict multiple switching periods ahead by making assumptions about the future pulse widths based on the current pulse widths. This is accomplished by defining fixed sequences of concatenated prediction regions over the switching period. It will be shown that by using this scheme, the computational effort associated with the longer prediction horizons and the higher sampling rate can be reduced.

The controller is divided into two parts: a) The off-line calculation and storage of the coefficients of the prediction equations and b) the on-line evaluation of the controller. For every valid actuation choice at each sampling step in the switching period, an equation for the average value over one or more switching periods is calculated and stored in a lookup table. The on-line controller then loads the appropriate equations, based on the current position within the switching period, and applies the current measurement values to obtain the prediction results.

The primary control task is the control of a multi-level AC-to-AC converter with an *LC* output filter for voltage regulation purposes. However, it will also be shown that this controller can be generalised and applied to an arbitrary converter topology. This is demonstrated for output voltage regulation and capacitor balancing of a five-level flying capacitor converter as well as for current control of a simple single-leg inverter.

## 1.2 Research methodology

The evolution of the control problem is explained with reference to the well established PWM scheme. This is done in order to gain a clear understanding of the limitations of conventional finite-control-set model predictive control with a variable switching frequency when compared to the output waveform quality of PWM controllers. It is shown that although the control algorithm of a regularly sampled PWM controller is only sampled once in every switching period, the digital implementation of the associated PWM modulator is evaluated at a much higher sampling rate, resulting in a more accurate application of the duty cycle.

The carrier waveforms of PWM are used to develop a scheme where switching constraints are placed on the controller by defining prediction regions. These constraints are

chosen such that a fixed switching frequency is enforced with a pulse train similar to that of PWM. Due to the fact that the prediction regions are organised in known concatenated sequences, assumptions can be made about the future pulse widths. It is shown that this reduces the number of prediction choices and consequently the computational effort.

A generalised controller structure is formulated by using established state space theory. A state space model is derived for each switching state of the converter without obtaining a single linearised model. Off-line symbolic solvers are used to numerically pre-calculate the computationally intensive predictions and store them in a lookup table. This allows for a minimum on-line calculation effort to obtain the predictions over a horizon of a number of switching periods.

## 1.3 Dissertation outline

The dissertation is divided into the following chapters:

**Chapter 2: Background and motivation**

This chapter presents a literature background, motivations and objectives for the development of a fixed switching frequency technique. An overview is given on the current work in the field of Finite-Control-Set Model Predictive Control (FCS-MPC) and the fundamental concepts are explained. The limitations of the existing FCS-MPC techniques are explained together with the control problem and intended objectives.

**Chapter 3: FCS-MPC with a fixed switching frequency**

This chapter presents the development of a FCS-MPC method to achieve a fixed switching frequency. In the first part of this chapter, the concept of prediction regions based on the carrier waveforms of PWM is explained. To account for these constraints, a method for predicting the average value is presented. This is extended to allow for predictions to be made over a number of switching periods while minimizing the number of prediction choices. In the second part of this chapter, the modelling and practical implementation of a generalised controller on an FPGA is discussed. This includes the off-line calculation and storage of prediction coefficients and the implementation of the on-line controller. Lastly, it is shown that state estimation can be used to obtain state variables that cannot be measured.

**Chapter 4: Control of a medium voltage electronic voltage regulator**

The implementation and control of a medium voltage electronic voltage regulator (MVEVR) using FCS-MPC with a fixed switching frequency is the primary control objective and is presented in this chapter. The MVEVR topology consists of a series-stacked AC-to-AC

converter topology that is connected in a shunt-series configuration to an appropriate transformer. The controller is implemented and evaluated by simulation to obtain the ideal behaviour. These results are verified against experimental measurements to confirm the expected behaviour.

**Chapter 5: Control of a five-level flying capacitor converter**

The control of a five-level flying capacitor converter is presented to illustrate the FCS-MPC control method with a fixed switching frequency for the generalised case. The controller is evaluated in simulation and the results are compared to experimental measurement results.

**Chapter 6: Predictive control vs. PWM-based linear control for current control of a single leg inverter**

The FCS-MPC method with a fixed switching frequency is compared to a PWM-based a linear resonant regulator for the current control of a single-leg inverter. The aim of this chapter is to compare the performance of the predictive controller to a well known linear control scheme. The two control strategies are tested in simulation and the results are discussed.

**Chapter 7: Conclusion**

The work in this dissertation is concluded and future work is discussed.

**Appendices**

The detailed theoretical and hardware design of the medium voltage electronic voltage regulator is discussed in the appendices. The state space model derivations for all the converter topologies discussed in this dissertation is included at the end of the appendix.

## 1.4 Summary of contributions

The main contributions of this study to the body of knowledge are:

1. A scheme for achieving a fixed switching frequency with finite-control-set model predictive control that produces a pulse train similar to that of PWM. This scheme consists of the following concepts:

    a) A sampling rate that is much higher than the desired switching frequency.

    b) Switching constraints that are defined by using PWM carrier waveforms to define prediction regions during which only specific switching transitions can be made.

c) The ability to emulate the pulse patterns of various PWM carrier distributions such as phase shifted carriers, phase-disposition and carrier-disposition.

d) A method for predicting the future pulse widths over the switching period based on the current position within the switching period.

e) A method for reducing the computational effort of longer prediction horizons by reducing the number of prediction choices.

f) An off-line pre-calculation scheme and an on-line controller for practically realising the controller on an FPGA. This includes the off-line pre-calculation and storage of the prediction equation coefficients in a lookup table to minimize the number of on-line computations.

g) A generalised controller and modelling scheme that makes use of established state space modelling to realise a controller for an arbitrary converter topology.

h) The Euler forward method is used to extrapolate the future behaviour of an unknown load by including the extrapolation in the state space model of the converter. This improves the prediction accuracy for longer prediction horizons.

2. The control method has been implemented and experimentally verified on the following converter topologies

   a) A 12.75 kV single-phase voltage regulator consisting of multi-level AC-to-AC converter modules connected in a shunt-series configuration to an appropriate transformer has been developed and experimentally verified.

   b) The voltage control and capacitor balancing has been demonstrated on a single-phase 5-level flying capacitor converter with an output $LC$ filter.

3. It is shown that the performance of FCS-MPC with a fixed switching frequency compares well to a well-tuned linear PI controller for current control of a single-leg inverter.

# Chapter 2

# Background and Motivation

## 2.1 Introduction

This chapter presents a literature background, motivation and objectives for the development of a fixed switching frequency technique for finite-control-set model predictive control. In Section 2.2, a brief overview is given of the most important control methods in power electronics. This is followed, in Section 2.3, by a more detailed look at finite-control-set model predictive control. In order to understand the motivation behind the work discussed in this dissertation, the limitations of the conventional direct model predictive control methods with respect to the control problem is discussed in Section 2.4. Lastly, the history of the control problem as well as the objectives are presented in Section 2.5

## 2.2 Control methods in power electronics

### 2.2.1 General overview

This section presents a basic overview of the most important control methods used in power electronics and electric drive applications. The purpose of this section is not to discuss each control method in detail, but to highlight the different characteristics of each method and their placement within the context of control in power electronics.

A high-level classification of the different control methods are presented in [4] and are discussed in this section. The control in power electronics can be divided into five major control philosophies namely Hysteresis control, Linear control, Sliding mode control, Predictive control and Artificial intelligence. A breakdown of this classification is shown in Figure 2.1 and is briefly summarised in the following:

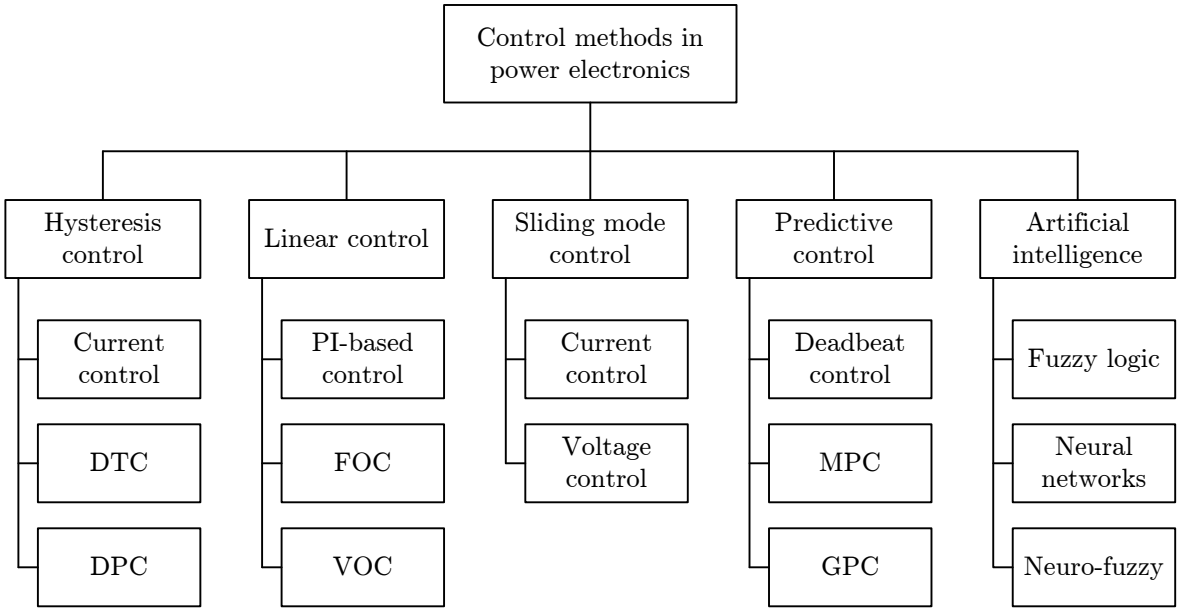



Figure 2.1: Classification of control methods used in power electronics [4]

### Hysteresis control

Hysteresis control is a particular type of bang-bang control and is a non-linear control method that originates from analogue control methods [5]. In order to implement this type of controller on a digital micro-controller, a very high sampling rate is required. The hysteresis controller has a variable switching frequency and does not require a modulator. It works in principle by defining a hysteresis band or hysteresis width within which the error is to be contained. As the error reaches one of the boundaries, the controller immediately changes the switching state in order to force the error in a trajectory that keeps it within the hysteresis band. This method produces some of the fastest control responses, but, with its variable switching frequency it leads to a spread spectrum and resonance problems in some applications. In higher power applications it may also pose a challenge for thermal control of the power switches and may require expensive and bulky filters to comply with EMI emission policies. This control method has been used for simple current control [5] as well for direct torque control (DTC) [6] and direct power control [7].

### Linear control

The operation of switched power converters are non-linear by nature [8]. In order to obtain a linear control behaviour, a modulation technique such as PWM (Pulse Width Modulation) or Space Vector Modulation (SVM) is required, although SVM is essentially just a variation of regular sampled PWM [9]. In principle, PWM works by creating pulse trains with a fundamental average that is the same as that of the target waveform at any instant. This is accomplished by comparing a lower frequency reference signal to a high frequency carrier. The primary objective is therefore to have an output where the low-frequency component is tracking the reference input. As a secondary objective, the

pulses may be arranged in a more effective way to minimize switching losses, unwanted harmonic distortion and any other performance requirement.

Various techniques have been proposed for obtaining a linearised model of the converter as well as for compensating for the PWM modulator [1]. Techniques for obtaining a linearised model is presented in [9] and [10] although a more accurate model of the PWM modulator has recently been proposed in [1] and compared to model predictive control in [2].

In linear control of power electronics, the three types of control strategies that are most widely used are Proportional-Integral (PI) based controllers for current and voltage control (amongst others) [5], Voltage-Oriented Control (VOC) for grid-tie inverters [11] and Field-Oriented Control (FOC) [12] for motor drive applications. Although these control methods can be challenging for converter topologies with multiple controlled variables such as matrix and multi-level converters, variations of these control methods are widely used in the power converter industry today.

#### Sliding mode control

Sliding Mode Control (SMC) falls under the class of robust control techniques and is aimed at eliminating or minimizing the effects of model uncertainties and external disturbances on the control performance. It is a type of variable structure control that is specifically suited for non-linear systems. The control action is discontinuous and follows a pre-defined control switching law. This causes the system to rapidly switch between switching states - or substructures as it is defined. In order to limit the switching frequency, constraints can be placed or a quasi-sliding mode control method can be implemented that makes use of a PWM modulator [13]. It has been implemented for power electronic applications in [14; 15] and [16] and more information can be obtained from these books [17; 18].

#### Predictive control

Predictive control is characterised by the use of a model of the system to predict the optimal future sequence of actuation. This method is discussed in further detail in the section hereafter.

### 2.2.2 Predictive control

This section presents an overview of the principle concepts of predictive control and where it fits into the larger class of controllers and therefore a short description of the characteristics of the different predictive control methods are discussed.

Predictive control does not describe one specific control method, but consists of a wide class of controllers that uses a model of the system or some pre-defined criteria to predict

the future behaviour of the controlled state variables or parameters. The predictions are used to obtain the optimal points of actuation by following an optimization criterion [19].

As proposed in [19], predictive control can be divided into four categories namely, deadbeat control, hysteresis based control, trajectory based control and model predictive control. With deadbeat control a prediction is made for the optimal actuation point such that the error between the reference and the controlled variable are zero at the next sampling instance.

The optimization criterion for hysteresis based control is to keep the controlled variables within predefined boundaries where as with trajectory based control, the controlled variables are forced to follow given references. The optimization criterion for model predictive control (MPC) is expressed as a cost function that is to be minimized. The cost function is flexible in that it can include reference tracking, a hysteresis band or even some other system parameter such as the minimization of the switching frequency. A

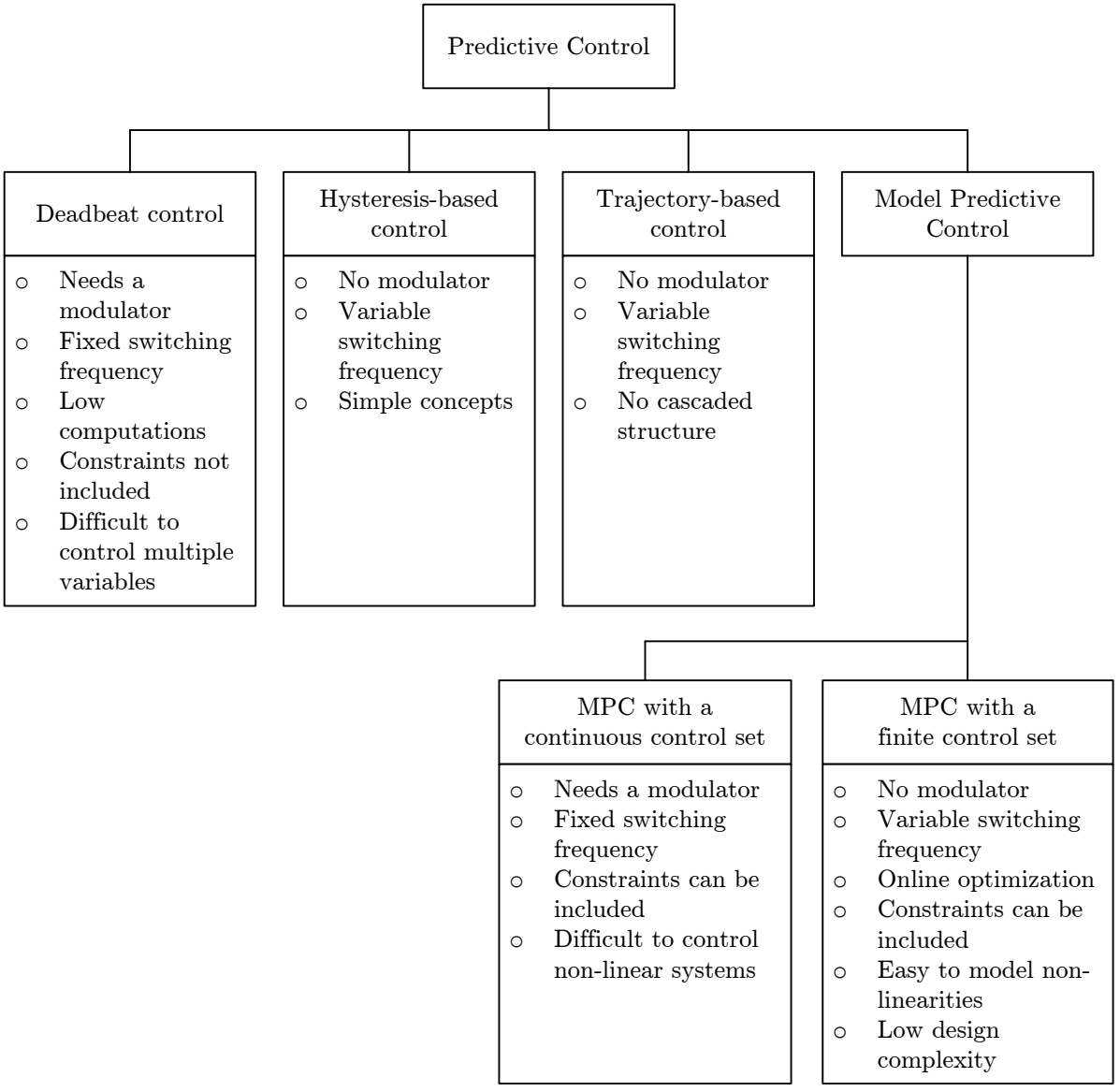



Figure 2.2: Classification of predictive control methods used in power electronics [19]

block diagram with the classification of predictive control methods is given in Figure 2.2.

### Deadbeat Control

At every sampling instance a model of the system is used to calculate the required control reference that will force the error between the controlled variable and the reference input to become zero at the next sampling instance. The control reference is applied to the converter by means of a modulator.

Deadbeat control provides a fast dynamic response, but is often very susceptible to unanticipated influences such as an inaccurate model. The performance of the controller can easily deteriorate as a result of an inaccurate model, unmodelled delays and errors in the model. A further disadvantage is that constraints and non-linearities of the controlled variables are difficult to incorporate into deadbeat control [19].

### Model-Based Hysteresis Control

Model-based hysteresis control works on the principle of keeping the controlled variables within the boundaries of a hysteresis area or space. The controller predicts the outcome for all the valid switching states and selects the state that keeps the controlled variables within the hysteresis boundaries for the longest time. Hysteresis based control is characterized by a variable switching frequency and the switching states are directly applied to the converter without the need for a modulator. By choosing the switching state that keeps the controlled variables within the hysteresis boundaries for the longest time, a reduction in the switching frequency is obtained.

### Trajectory Based

A model of the system is used to calculate all the possible trajectories of the system that the controlled variables can follow. The calculations are typically done off-line and stored in a lookup table. When the control is executed, the stored trajectories are used to determine the shortest route between the initial state and the desired state. The control is then constantly steered along the trajectories to reach the desired state. Trajectory based control has no cascaded structure, requires no modulator and applies the switching states directly to the converter and produces a variable switching frequency.

### Model Predictive Control

Model predictive control (MPC) is characterised by the use of a mathematical model of the system to predict the anticipated future behaviour and can be divided into two wide categories: MPC with a continuous control set (CCS-MPC) and MPC with a finite control set (FCS-MPC).

With CCS-MPC, the control output is a continuous reference signal that requires a modulator to generate the appropriate actuation commands. Consequently, this type of controller is characterised by a fixed switching frequency.

FCS-MPC, on the other hand, considers the converter as a finite set of models, where each model corresponds to a specific switching state. The switching states are directly applied to the converter without a modulator and typically results in a variable switching frequency. In the following section, direct model predictive control with a finite control set is discussed in more detail.

## 2.3 Finite-control-set model predictive control

### 2.3.1 Introduction

Model predictive control (MPC) has been used in industrial process control for decades. This was possible since the time constants in these processes were sufficiently long enough to give the more primitive micro controllers ample time to do the calculations [20]. In recent years, model predictive control of power electronics gained new interest with the technological advancement of micro controllers and FPGAs [4]. As the processing power and complexity of these devices improved, it allowed more complex calculations to be done in real-time. For MPC, this allowed the implementation of faster controllers with higher sampling rates and switching frequencies while controlling multiple state variables [19; 21].

Finite-Control-Set Model Predictive Control (FCS-MPC) presents characteristics that are favourable for controlling multi-level converters and electric motor drive systems where multiple state variables need to be controlled [21; 4]. In [19], a survey of the most important types of predictive control in power electronics and drives is discussed, in [22] the applications of MPC in power electronics is reviewed and in [4], a comprehensive overview of the general principles of FCS-MPC is presented. In the literature this type controller is commonly referred to as Finite-Control-Set Model Predictive Control (FCS-MPC) [23], although it has also been termed Finite-Set Model Predictive Control (FS-MPC) in [24] or Direct Model Predictive Control (D-MPC) in [25].

FCS-MPC has been applied to a number of power converter topologies and drive applications and the following concise summary highlights the most import work: The most important types of converters include the control of a Neutral-Point Clamped Converter [26], a Matrix Converter [27], a Direct Converter [28; 29; 30], a Flying-Capacitor Converter [31; 32; 33; 34; 35; 36; 37], a Diode-Clamped Converter [38], an Active Front-End Rectifier [39], a Three-Phase Neutral-Point Clamped Converter [26; 40; 41], a Three-Phase AC/DC/AC Converter [42], a Voltage Source Inverter [43; 44] and an AC-to-AC Converter [45].

The implementation of current control of an inverter using FCS-MPC is discussed in [43; 25] and similar strategies for the current control of three- and four-level inverters is given in [46; 26] and [47] respectively. An assessment of FCS-MPC with a comparison to linear control is presented in [48] and [2].

In [42; 27] it is shown that it is possible to control both active and reactive power and in [40; 33] torque and flux control of an induction motor is discussed as well as an implementation for sensor-less control in [49]. Furthermore, in [50] the control of a permanent magnet synchronous motor is discussed.

In [51], [45] and [36], FCS-MPC techniques have been implemented for the voltage control of converters with second order $LC$ output filters. FCS-MPC has shown that the

typical double-loop control strategy used with linear controllers is not needed and the output voltage is directly controlled. In [36] is was shown that in order to account for the dynamic behaviour of the second order filter, a higher prediction horizon is required.

As the prediction horizon is increased, the number of predictions and the required computational power increases exponentially and may pose a challenge for practical realization. Several methods have been proposed to achieve long prediction intervals and a review of some of these strategies are discussed in [52]. These include the so-called move blocking strategy [53], extrapolation [54; 55; 56] and an event-based horizon strategy, which is a combination of Optimized Pulse Patterns (OPPs) and MPC [57]. In this dissertation, an alternative strategy is presented in Chapter 3.2.3 for increasing the prediction horizon while remaining computationally efficient.

With the conventional FCS-MPC prediction techniques presented in [4], the control is evaluated and applied at equidistant instances in time. This results in a variable switching frequency where the maximum switching frequency is half of the sampling frequency. As discussed in [45], this presents a problem for certain applications since the switching frequency cannot be maintained for all references. This results in a voltage and current spectrum that is spread over a wide range of frequencies and that will change as the sampling frequency or reference is changed [19].

Some applications may require a certain THD limit on the output voltage and current or may require an output spectrum that is concentrated within a specific frequency band to comply with EMI requirements or to avoid possible resonance. A method for shaping the output frequency spectrum has been proposed in [44] where a frequency weighted cost function is implemented by including a narrow-band stop filter term in the cost function.

In other applications it may be required to reduce the switching losses. It has been shown in [26] that switching losses can be reduced by reducing the switching frequency. This has been accomplished by adding a weighting term to the cost function that penalises the commutations.

Alternatively, a fixed switching frequency technique can be implemented which allows for easier EMI filter design and power switch loss calculations. A constant switching frequency Predictive Direct Power Control (P-DPC) algorithm has been presented in [58; 59; 60]. A fixed switching frequency is obtained by selecting an optimal set of concatenated voltage vectors that are stored in a lookup table as pre-calculated sequences. The voltage vector sequences are chosen over a fixed period which results in a fixed switching frequency. The control problem is then solved by computing the times when each voltage vector in the sequence should be applied in order to converge towards the reference values. This is accomplished by calculating the slopes of the output variable for each voltage vector and performing a simple geometrical analysis.

In [45; 36; 37], an alternative predictive control method is proposed for achieving a fixed switching frequency. This method uses the analogy of a PWM carrier to construct

a concatenated sequence of prediction regions during which only specific switching states can be applied. By applying these constraints, assumptions can be made about the times when the next switching states should be applied – thereby eliminating the need for a geometrical analysis. This method forms part of the work that is presented in this dissertation and it is discussed in further detail in Chapter 3.

### 2.3.2 Control scheme

Finite-Control-Set Model Predictive Control (FCS-MPC) is a subset of the wider family of Model Predictive Controllers (MPC) and is characterised by the use of a model of the system to predict the future behaviour of the controlled variables. Unlike PWM-based linear control, FCS-MPC does not follow a cascaded control loop structure, it does not make use of a modulator and does not require linearisation techniques to obtain a single linearised model.

It considers the system as a finite set of linear models where each model represents a unique physical switching state. These models are used at each sampling instance to predict the future behaviour for each switching state to determine the optimal sequence of actuation to achieve the control objective. This allows the prediction and evaluation of a finite control set.

The control objective is described by a predefined cost function that is to be minimized and the optimal actuation choice is directly applied to the power converter. A receding horizon policy is followed and the predictions are made up to an horizon $h$. However, only the first actuation choice in the sequence is applied and a new sequence is calculated at the next sampling instance.

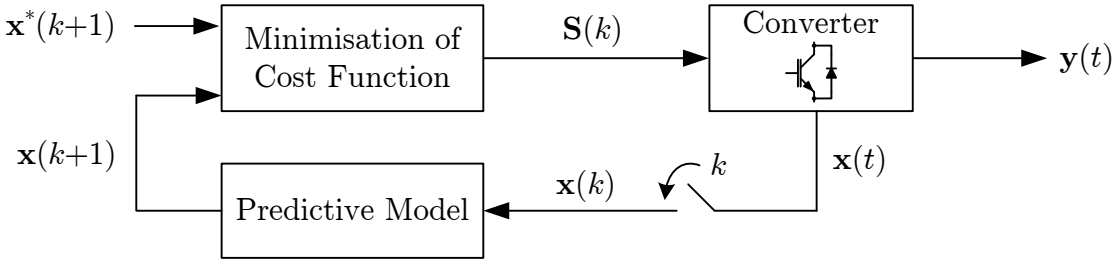



Figure 2.3: Block diagram of the general FCS-MPC control scheme [4; 23]

The block diagram of a general FCS-MPC control scheme is shown in Figure 2.3. This is the most basic scheme and it is assumed that the entire state vector $\mathbf{x}(t)$ of the power converter is measurable or known. If only the output vector $\mathbf{y}(t)$ is known, some state estimation technique such as a state observer or Kalman filter [61] may be used to obtain an estimated state vector $\hat{\mathbf{x}}(t)$.

At every sampling instance $k$, the sampled state vector $\mathbf{x}(k)$ is updated. The state vector is used to make a prediction for every possible actuation choice at $k+1$ or for every

actuation sequence up to the horizon $k+h$. Each prediction is compared to the reference input $\mathbf{x}^*(k+1)$ in a cost function. The actuation choice that minimizes the cost function is selected and is applied directly to the power converter by way of the state vector $\mathbf{S}(k)$. This operation is executed at every sampling instance.

According to [4], this control structure has several advantages:

- Intuitive and conceptually simple to understand.
- It can be applied to a variety of systems and configurations.
- Easy to control multiple state variables.
- It allows for the compensation of dead time and delays.
- Easy to include non-linearities in the model.
- Constraints can easily be added to the cost function.
- The controller is easy to implement.
- Modifications and extensions can easily be added to the controller for specific applications.

and some disadvantages:

- It has a much larger number of calculations when compared to classic controllers.
- The accuracy of the model has a direct impact on the quality of the controller.
- If the system parameters change over time it is unable to adapt without considering some additional estimation and adaptation algorithms.

### 2.3.3 System modelling

FCS-MPC considers the converter as a finite set of linear models, where each model represents a valid switching state. If the switches are considered as ideal switches, with only two switching states, the number of switch combinations is given by

$$N = 2^s \tag{2.1}$$

where $N$ is the number of switch combinations and $s$ the number of switches. Depending on the converter topology, there may be more switching combinations than valid switching states. If, for instance, a full bridge converter is used and the switches are assumed to be ideal, the number of switch combinations becomes $N = 2^4 = 16$. However, a constraint is placed on the two switches of each phase arm. The two switches may never be turned *on*

at the same time and is usually switched as a complementary pair. Therefore, although four switching combinations are possible, each phase arm only has two valid switching states. The number of switches in Equation 2.1 can therefore be replaced with the number of valid switching states [4]. In the case of the full bridge converter, the number of valid switching combinations becomes $N = 2^2 = 4$.

In the conventional FCS-MPC methods presented in [4], for example, the system modelling is accomplished by deriving equations that describe the dynamic behaviour of the controlled variables. However as a more generic approach [37], the converter can also be modelled by a state space representation [61] such as

$$\dot{\mathbf{x}}(t) = \mathbf{A_s}\mathbf{x}(t) + \mathbf{B_s}u(t) \tag{2.2}$$

$$\mathbf{y}(t) = \mathbf{C_s}\mathbf{x}(t) + \mathbf{D_s}u(t) \tag{2.3}$$

where the boldface subscript $\mathbf{S}$ indicates the switching vector that is described by the state space model. Although the state space approach may include dynamic behaviour that is uncoupled from the controlled variables and which is not required to make the predictions, it provides a generic modelling format. It is worth noting that although uncoupled uncontrolled variables are included in the model, it does not necessarily mean that they will be calculated when predictions are performed.

FCS-MPC is evaluated in discrete time steps and the evaluation of the predictions for a discrete-time state space representation [61] can be calculated by

$$\mathbf{x}(k+1)_\mathbf{S} = \mathbf{F_s}\mathbf{x}(k) + \mathbf{G_s}u(k) \tag{2.4}$$

and

$$\mathbf{y}(k) = \mathbf{C_s}\mathbf{x}(k) + \mathbf{D_s}u(k) \tag{2.5}$$

where

$$\mathbf{F_s} = e^{\mathbf{A_s}T_s} \tag{2.6}$$

and

$$\mathbf{G_s} = \int_0^{T_s} e^{\mathbf{A_s}\tau}\mathrm{d}\tau \cdot \mathbf{B_s} \tag{2.7}$$

for a sampling period $T_s$.

### 2.3.4 Predictions

In [4], MPC is defined as an optimization problem that consists of minimizing the cost function for a predefined prediction horizon, $h$, in discrete time. For a simple case, when the horizon is taken as 1, the predictions are made for $k + 1$. However, when a larger prediction horizon is chosen, predictions are made for each valid switching sequence up

to $k+h$. The entire sequence is evaluated in the cost function, but since the control is re-evaluated with new measurements at every sampling instant, only the first state in the sequence is applied. This is called a *Receding Horizon* strategy, where the horizon keeps moving away as the controller steps forward in time.

An increased prediction horizon typically increases the accuracy with which the optimal actuation point is selected. However, an increased prediction horizon increases the computational time and as such, a balance should be sought between the sampling frequency and the allowed execution time of the predictions.

### 2.3.5 Approximations

The FCS-MPC control is implemented in discrete-time and as such, a discrete-time model is required. The predictions can be performed by using the discrete-time state space notation given in Equation 2.4. Alternatively, the derivative of the state variables can be obtained by using simpler approximations such as a first-order Euler Forward approximation, or for higher order systems, a fourth-order Runge-Kutta approximation [4; 23].

#### 2.3.5.1 Euler-forward approximation

The Euler Forward approximation of a derivative is given by

$$\frac{\mathrm{d}x}{\mathrm{d}t} \approx \frac{x(k+1)-x(k)}{T_s}. \tag{2.8}$$

If applied to the continuous state space representation in (2.2) [62] , the discrete-time state space representation becomes

$$x(k+1) \approx T_s \cdot \Big(\mathbf{A}\cdot\mathbf{x}(k)+\mathbf{B}\cdot\mathbf{u}(k)\Big)+\mathbf{x}(k). \tag{2.9}$$

#### 2.3.5.2 Runge-Kutta Approximation

The error induced by the Euler Forward Approximation introduces a significant error when higher order systems is evaluated [4]. The fourth order Runge-Kutta method provides a more accurate approximation by averaging four slopes rather than one. The fourth order approximation is given by

$$\mathbf{x}(k+1) = \mathbf{x}(k) + \frac{1}{6}T_s \cdot \big(\mathbf{R}_0 + 2\mathbf{R}_1 + 2\mathbf{R}_2 + \mathbf{R}_3\big) \tag{2.10}$$

where

$$\mathbf{R}_0 = \mathbf{A}\mathbf{x}(k) + \mathbf{B}\mathbf{u}(k) \tag{2.11}$$

$$\mathbf{R}_1 = \mathbf{A}\cdot\left(\mathbf{x}(k)+\frac{T_s}{2}\mathbf{R}_0\right)+\mathbf{B}\cdot\mathbf{u}(k) \tag{2.12}$$

$$\mathbf{R}_2 = \mathbf{A}\cdot\left(\mathbf{x}(k)+\frac{T_s}{2}\mathbf{R}_1\right)+\mathbf{B}\cdot\mathbf{u}(k) \tag{2.13}$$

$$\mathbf{R}_3 = \mathbf{A}\cdot\big(\mathbf{x}(k)+T_s\mathbf{R}_2\big)+\mathbf{B}\cdot\mathbf{u}(k). \tag{2.14}$$

### 2.3.6 Cost function design

One of the fundamental concepts that define FCS-MPC is the use of a cost function to describe the control objectives. The cost function typically consists of one or more weighted terms where each term represents the control criteria of a specific controlled variable or system parameter. This criteria is chosen in such a way that the desired control outcome is the minima of that criteria. An example of such a criteria is the minimization of the error between a control reference input and the corresponding state variable. The importance of each term in the control outcome is implemented by applying a weighting factor $w$ to each term. As such, the cost function is typically written in the following form:

$$g = w_1|x_1^* - x_1^p| + w_2|x_2^* - x_2^p| + w_3 f(x_3^p) \tag{2.15}$$

where, in this example, $w_1$, $w_2$ and $w_3$ are the weights of each term, $x_1^*$ and $x_2^*$ are reference inputs, $x_1^p$, $x_2^p$ and $x_3^p$ are predicted values of the controlled state variables and $f(\cdot)$ is some function that evaluates the predicted state variable $x_3^p$. In this case, the first two terms describe a reference tracking problem by evaluating the respective tracking errors and the last term is some arbitrary function that may perform any one of a number of tasks such as limiting the controlled variable within certain boundaries.

Several cost function terms have been presented in [4] which relate to different control requirements for a system. In this section, a brief overview of the most important cost function terms in [4] are discussed which include: reference tracking, enforcement of actuation constrains such as the minimization of the switching frequency and reduction of switching losses, hard constraints to keep certain parameters within specified boundaries and the shaping of the spectral content of the control output.

#### 2.3.6.1 Reference tracking

Reference tracking generally consists of the minimization of the error between the desired reference input and the actual state variable [61; 4]. In power converters and motor drive applications, typical examples of reference tracking include current control, voltage control, power control, torque control and speed control.

The error is defined as the distance between the reference and the predicted state variable and can be obtained by calculating the absolute value, the squared value or the integral value of the error over the predicted period:

$$g = ||x^* - x^p|| \qquad \text{(norm)} \tag{2.16}$$

$$g = |x^* - x^p| \qquad \text{(absolute value)} \tag{2.17}$$

$$g = (x^* - x^p)^2 \qquad \text{(squared value)} \tag{2.18}$$

$$g = \left| \int_k^{k+1} \big(x^*(t) - x^p(t)\big) \mathrm{d}t \right| \qquad \text{(integral value)} \tag{2.19}$$

where $g$ is the cost, $x^*$ is the reference value and $x^p$ is the predicted value.

When the cost function only contains one term, the absolute value and squared value error will give similar results. However, when more than one term is added to the cost function or a higher prediction horizon is used the squared value error terms produce better tracking results. The reason for this behaviour is that when the magnitude of an error is $0 < |err| < 1$, the magnitude will become quadratically smaller with respect to the other terms when the square is taken. Likewise, when the magnitude of the error is $|err| > 1$, the error will become quadratically bigger than the other terms when the square is taken. This leads to small errors being suppressed and larger errors being highlighted – which leads to better overall tracking.

Compared to the absolute and squared value error terms, the integral value term is more complex to implement, but leads to more accurate reference tracking. The integral error term considers the trajectory of the variable over the predicted period by calculating the mean value of the error and not only looking at the final value.

#### 2.3.6.2 Actuation constraints

Some applications may require that the control effort be reduced to a minimum while maintaining an acceptable level of reference tracking. The control effort in power electronics can be defined as the energy needed to accomplish the control task. As such, it relates to the switching losses and thermal management of the semiconductor devices. The switching losses is a function of the switching frequency, the voltage across the switch and the current through the switch. By taking these parameters into account, the minimization of the control effort can be included in the cost function.

In [4], two methods for reducing the control effort is presented. The first method considers the minimization of the switching frequency while maintaining an acceptable reference tracking. The second method evaluates the incurred switching losses for each actuation choice by taking the variation in voltage and current into account.

##### Minimization of the switching frequency

This method attempts to reduce the control effort by reducing the switching frequency. For FCS-MPC methods that implement a fixed switching frequency technique, this method is fruitless and may even degrade the controller performance. For control methods with a variable switching frequency, a term can be added to the cost function that penalises the number of commutations. Such a cost function can be expressed as

$$g = w_1|x^* - x^p| + w_2 \cdot n \tag{2.20}$$

where the first term is for reference tracking and the second term is for penalising the number of commutations. The number of commutations $n$ can be calculated by

$$n = \sum_{m=1}^{N} |S_m(k) - S_m(k-1)| \tag{2.21}$$

where the switching state vector $\mathbf{S}$ is defined as

$$\mathbf{S} = (S_1, S_2, S_3, \ldots, S_N) \tag{2.22}$$

**Minimization of the switching losses**

The switching losses can be minimized without reducing the switching frequency by taking the voltage and current at the switches into account. This method can be implemented with both a variable and a fixed switching frequency technique. In [63] an equation for calculating the energy dissipation of one switching event is proposed and in [4], a simplified expression is presented that can be included in the cost function as

$$g = w_1|x^* - x^p| + w_2 \sum_{j=1}^{N} \Delta i_c^p(j) \Delta v_{ce}^p(j) \tag{2.23}$$

where the first term is for reference tracking and the second term penalises the switching losses. In the second term, $N$ is the number of controlled switches, $\Delta i_c^p$ is the predicted change in the collector current and $\Delta v_{ce}^p$ is the predicted change in collector-emitter voltage across the IGBT switch. As with the other cost functions, the priority of the terms are determined by the weighting factors $w_1$ and $w_2$.

#### 2.3.6.3 Hard constraints

Traditional cascaded control schemes often includes reference saturation to prevent variables from exceeding certain limits [61]. For example, when the voltage of an $LC$ output filter is controlled, a limit may be placed on the peak inductor current during large voltage step changes. This can be done by limiting the peak reference value of the inner current loop. Alternatively, a limit may be required for the peak capacitor voltage of a flying capacitor converter during transient effects.

With FCS-MPC there are no cascaded control loop structures and all the controlled variables are added as terms in the cost function. Limits can therefore be applied by modifying the cost function and adding an appropriate term. The objective of the cost function is to obtain the sequence of actuations that will minimize the cost function. If a state variable $x$ reaches a limit, the cost function must be modified to prevent those actuation choices which will lead to $x$ exceeding the predefined limit $x_{max}$. This can be achieved by adding a non-linear term $f_{lim}(x^p)$ to the cost function [4] and is implemented as

$$f_{lim}(x^p) = \begin{cases} 0 & \text{if} \quad |x^p| \leq x_{max} \\ \infty & \text{if} \quad |x^p| > x_{max} \end{cases} \tag{2.24}$$

If the variable is within the predefined limits, the term has no influence on the cost function. If the limit is exceeded, the term will force the cost function to infinity or some arbitrarily large value. Unlike linear controllers, no integrator anti-windup techniques are required when implementing hard constraints.

#### 2.3.6.4 Spectral manipulation

The manipulation of a variable switching frequency will ultimately affect the spectral content of the converter output. In addition to the switching frequency, whether it is variable or fixed, the control reference input, the topology of the plant as well as external disturbances may affect the spectral content of the controlled output. In some applications, such as a three-phase inverter with an $LCL$ filter, resonance may occur if the spectral content contains significant power close to the resonant frequency of the filter. By controlling the spectral content, a variable switching frequency can be forced to concentrate within a specific frequency band or the output can be forced to avoid specific resonant frequencies.

In [44], a cost function term is proposed in the form of:

$$g = w \cdot F(x^* - x_p) \tag{2.25}$$

where $F$ is a discrete-time filter of order $n$:

$$F(z) = \frac{b_0 z^0 + b_1 z^{-1} + b_2 z^{-2} + \cdots + b_n z^{-n}}{a_0 z^0 + a_1 z^{-1} + a_2 z^{-2} + \cdots + a_n z^{-n}}. \tag{2.26}$$

The frequency response of the filter is effectively a weighting function that applies a weight to specific frequency bands based on the type of filter. For example, if a band-stop filter is applied, the spectral content will tend to concentrate at the centre frequency of the filter. If a low-pass filter is applied, the spectral content will concentrate above the cut-off frequency. Conversely, if a high-pass filter is applied the spectral content will be concentrated below the filter cut-off frequency.

In [64], a similar method is presented where the spectral content is manipulated by implementing a Discrete Fourier Transform function instead of a filter.

#### 2.3.6.5 Integrating action

The cost function terms that have been discussed until now only use current measurement values to make predictions. According to [65], this approach can be regarded as a proportional control action. By only looking into the future, the cost is only proportional to the deviation of the controlled variables based on current measurement values.

If model inaccuracies are present, an error is made when the future behaviour is predicted. This often leads to a steady state tracking error that cannot be accounted for. One solution to resolve this error is to include a history of past errors in the cost

function. In theory, this can be accomplished by adding an integrator term that evaluates the current deviation [65]:

$$g = w_1 \int (x^* - x^p)\,\mathrm{d}t. \tag{2.27}$$

However in practice, the integrator can be implemented as a low-pass filter (LPF). This can be realised in hardware as a simple Infinite Impulse Response (IIR) filter that is essentially an exponentially weighted moving average. If the filter input is $x(k)$ and the output is $y(k)$, the first order LPF can be implemented as

$$y(k) = \alpha x(k) + (1 - \alpha)y(k - 1) \tag{2.28}$$

where $\alpha$ is the smoothing factor or the degree of weighting decrease. The smoothing factor $\alpha$ is a function of the number of time periods $N$ that need to be considered in the moving average and the relationship is given by

$$\alpha = \frac{2}{N + 1} \tag{2.29}$$

and where $N$ is

$$N = \tau f_s \tag{2.30}$$

with $\tau$ being the time period of the filter and $f_s$ the sampling frequency. The resulting cost function for reference tracking and steady state error correction is

$$g = w_1|x^* - x^p| + w_2 \cdot f_y(x^p) \tag{2.31}$$

where $f_y$ is the filter output and $w_2$ is the weighting factor. If a higher prediction horizon is calculated, the filter should be stepped through each prediction up to the horizon.

### 2.3.7 Weighting factor selection

As shown in the previous section, the cost function typically consists of one or more weighted terms where each term represents the control criteria of a specific controlled variable, system parameter or constraint. The controlled variables may have different units of measure such as voltage, current, torque, flux, power, speed, switching frequency, etc. It may also be that two controlled variables of the same unit of measure may have different orders of magnitude. The purpose of the weighting factors is therefore to normalise the magnitude of the terms with respect to each other so that each term is given equal preference. In the event that one controlled variable should enjoy preference over another, the weight of that term can be adjusted to increase its importance in the cost function.

If only one variable or the components of the same variable is controlled, it is not necessary to add weighting factors to the terms. However, if more than one controlled variable is added to the cost function, it may be necessary to normalise their magnitudes

and apply a certain priority to each term by adjusting their respective weighting factors. This will result in a trade-off between the performance of the different controlled variables and parameters.

In [4] it has been suggested that for a controlled variable $x$, a normalization factor $x_n$ can be applied to the term. Typically the normalization factor can be chosen as the nominal value of $x$ and applied to the weighting factors as

$$g = \frac{w}{x_n}|x^* - x^p| \tag{2.32}$$

or

$$g = \frac{w}{x_n^2}(x^* - x^p)^2. \tag{2.33}$$

where $x^*$ is the reference and $x^p$ is the predicted future value of $x$ and $w$ is the adjustable weighting factor.

Unfortunately there are no control design theories, analytical or numerical methods for designing the weighting factors. At this point in the literature, an accepted method of tuning the weighting factors is to start off with an initial set of weights and gradually adjusting the weights until a satisfactory control output is obtained.

Guidelines for adjusting the weighting factors have been presented in [4]. In order to determine the success of the tuning, a measure of merit is required. For current control this could be the measure of the steady state tracking error, phase error or THD. It is suggested that when the cost function has a primary controlled variable with secondary controlled variables, one could start with a weighting factor of $w_1 = 1$ for the primary variable and a weighting factor of $w_2 = 0$ for the secondary variable. By running a simulation and gradually increasing the value of $w_2$, a satisfactory weighting factor can be obtained by observing the output. The same principle applies when more than one secondary variable exists. If more than one term with an equal importance is present, all those terms should start with an initial weighting factor of one. In [4] it has been suggested that a branch and bound algorithm can be used to assist in obtaining appropriate weighting factors.

## 2.4 Limitations of Conventional FCS-MPC Methods

In power electronic converters with high power ratings, the limiting factor is often switching losses. Various MPC methods have been presented [4; 19; 24; 66; 67] to minimize the switching frequency while attempting to track the reference as close as possible. A lower switching frequency, however, comes at a cost which usually results in a larger ripple current and voltage and consequently a higher THD. In motor drive applications, where the current is controlled, a larger ripple current may be an acceptable price to pay to reduce switching losses. In voltage regulation applications, however, it may not be the case. The amplitude and THD of the output voltage are often important specifications which need to be contained within specified limits. It is therefore preferable to have a control strategy

that combines the advantages of FCS-MPC with output voltage quality characteristics comparable to that of PWM. It is therefore against the benchmark of PWM that the FCS-MPC technique for a fixed switching frequency is proposed in Chapter 3.

In order to gain a clear understanding of the motivations for the proposed control strategy, the evolution of the control problem is explained in relation to the well established PWM scheme. A controller based on PWM is typically implemented by comparing a carrier waveform with a reference signal to produce a pulse train, as shown in Figure 2.4. When the reference is higher than the carrier waveform, the pulse train output is in the high state. Likewise, when the reference is lower than the carrier waveform, the output is inverted to the low state. The duration of the pulses is therefore a function of the reference signal and can be translated to a duty cycle, which represents the fraction of the pulse width during which the output is in the high state [9].

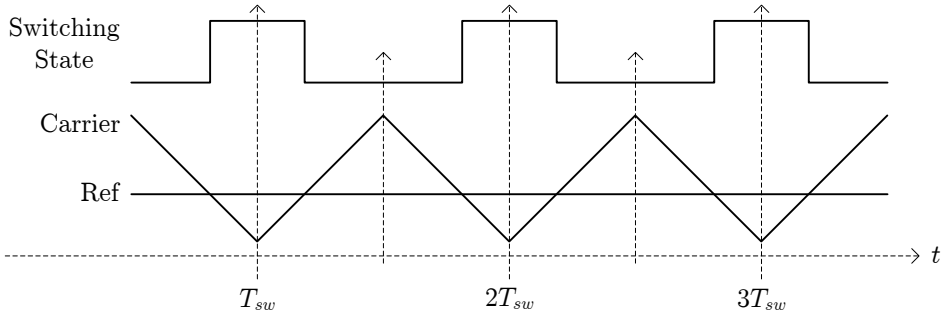
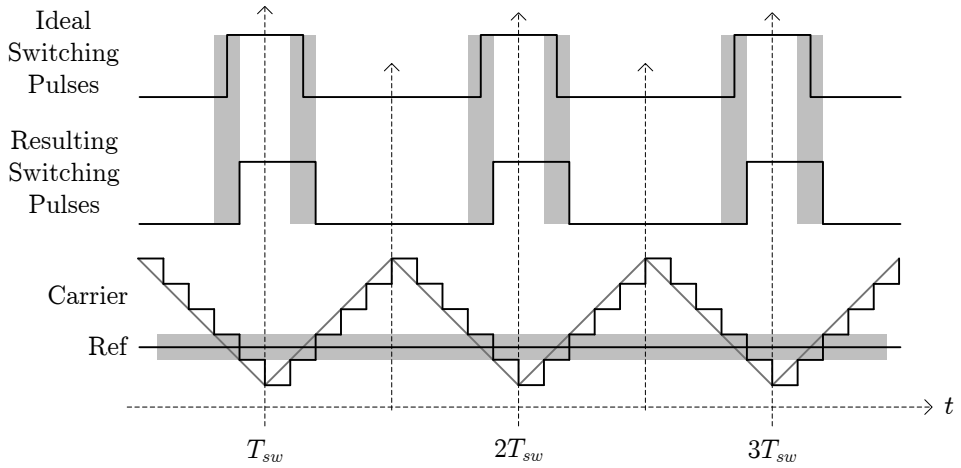
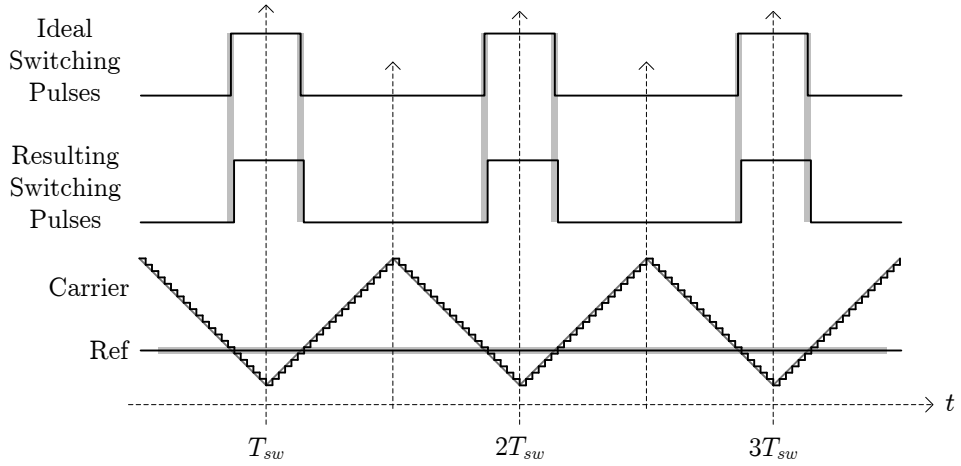



Figure 2.4: Depiction of a triangular PWM carrier waveform with reference and resulting pulse train.

PWM control schemes can be implemented by using either an analogue circuit or a digital micro processor [5]. With an analogue control loop, the pulse train is typically obtained by using analogue comparators to accurately determine the point where the reference crosses the carrier waveform. With a microprocessor, the carrier waveform is typically implemented by using a digital counter that is incremented or decremented at a clock speed which is much higher than the switching frequency. The counter can be seen as a discretized version of the analogue carrier. Therefore, as the counter value passes a given reference value, the output of the digital modulator is inverted in the same way as the analogue comparator. This coarse quantization process can be modelled as quantization noise, which raises the noise floor of the PWM signal. The faster the counter's clock speed is with respect to the switching frequency (i.e. the more counts within each switching period), the less quantization noise will be added to the PWM signal. This is depicted in Figure 2.5a and 2.5b, where (a) is less accurate than (b). The discrete carrier waveform can therefore be translated to a continuous carrier with a discrete duty cycle, where the resolution of the duty cycle depends on the sampling rate of the carrier.




(a) Reduced modulator accuracy when evaluating the carrier by using less steps.




(b) Increased modulator accuracy when evaluating the carrier waveform and reference by using more steps.

Figure 2.5: Depiction of a discrete implementation of a PWM carrier waveform and reference together with the resulting output pulse train.

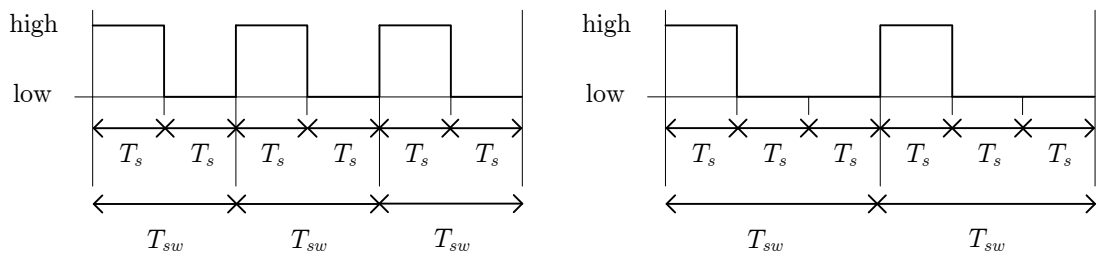
With regular sampled PWM, measurement samples are taken and the duty cycle is updated once in every switching period $T_{sw}$ [9]. However, in some PWM implementations the duty cycle may be updated at a much higher rate than the frequency of the carrier waveform [68]. Regardless of the rate at which the duty cycle is updated, the reference may cross the carrier waveform only twice in each switching period to ensure that a fixed switching frequency is produced.

The accuracy of a PWM based controller is therefore not only dependent on the rate at which the control algorithm updates the duty cycle, but also the accuracy with which the modulator applies the duty cycle. In contrast, FCS-MPC does not make use of a modulator and the accuracy with which the control is applied, is determined only by the rate at which the control algorithm is evaluated. In order to obtain tracking that is comparable to that of PWM, the FCS-MPC control algorithm has to be evaluated at a rate that is much higher than the desired switching frequency.

Finite-Control Set Model Predictive control (FCS-MPC) is based on the use of a finite set of models of the system, with each model representing a switching state, to predict the future behaviour of the controlled variables. With the conventional FCS-MPC methods [4; 19; 24; 26; 43; 44; 38; 51; 69; 70; 21], the system is evaluated at a discrete time step $k$ and the future values of the controlled variables are predicted for each switching state at time step $k+1$. The predicted state variables are evaluated in a cost function and the state that minimises the cost function is selected and applied directly to the converter. The switching state of the converter is therefore evaluated and changed at equidistant instants in time; usually every sampling period $T_s$, and kept in that state until the next sampling period.

The switching period is defined as the time in which the switches are turned on and off once [8]. If the definition of the switching frequency is applied to the gating signals of the conventional FCS-MPC methods, the resulting switching frequency is found to be variable with a maximum that is limited to half the sampling frequency. This can be demonstrated by applying the analogy of the duty cycle of PWM to the FCS-MPC control method.

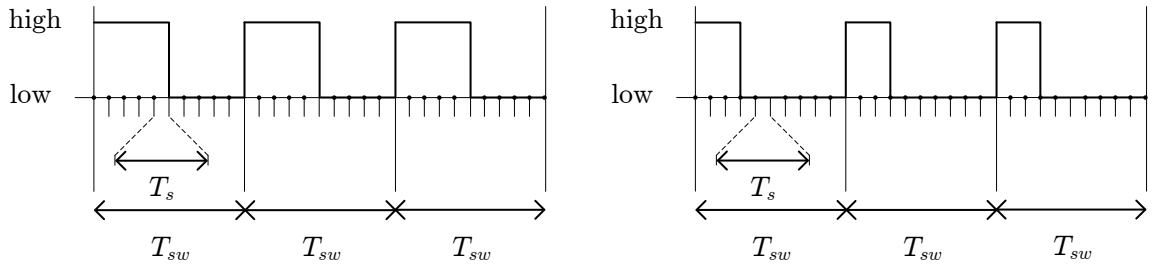
Consider a desired FCS-MPC reference that is equivalent to a duty cycle of $d = \frac{1}{2}$, as depicted in Figure 2.6(a). It is shown that the maximum resultant switching frequency occurs at $d = \frac{1}{2}$, while the effective switching frequency is limited to half the sampling frequency. Now, consider an FCS-MPC reference that is equivalent to a duty cycle of $d = \frac{1}{3}$, as depicted in Figure 2.6(b). It is evident that the maximum resultant switching frequency for a reference that is equivalent to $d = \frac{1}{3}$, is limited to a maximum that is a third of the sampling frequency. This illustrates that in order to maintain a high effective switching frequency for every reference, the control algorithm has to be evaluated at a much higher rate than the switching frequency. This is supported by the illustration of the discrete PWM modulator. In the same way that the discrete modulator has to evaluate the carrier at a much higher rate to apply an accurate duty cycle, the FCS-MPC control method has to evaluate the controller at a faster rate if the same waveform quality as PWM is to be obtained.




(a) Maximum switching frequency at $d = \frac{1}{2}$ (b) Reduced switching frequency when $d = \frac{1}{3}$

Figure 2.6: Depiction of the switching pulses when evaluating and applying control at the same frequency

If the FCS-MPC control is evaluated, for example, ten times faster than the desired maximum switching frequency, as depicted in Figure 2.7, it is possible to maintain the same effective switching frequency while the reference is varied. This is illustrated in Figure 2.7b where the maximum switching frequency for a reference equivalent to $d = \frac{1}{3}$ remains the same as a reference that is equivalent to $d = \frac{1}{2}$. It is further shown that as the sampling frequency is increased, (i.e. the more sample steps in each switching period) the more accurately the reference can be tracked.




(a) Switching pulses equivalent to $d = \frac{1}{2}$ (b) Switching pulses equivalent to $d = \frac{1}{3}$

Figure 2.7: Depiction of the switching pulses when evaluating and applying control at a frequency ten times higher than the desired maximum switching frequency. The effective switching frequency remains the same in both (a) and (b).

Figure 2.6 illustrates the ideal case where the pulses are evenly distributed and have the same pulse width for a given static reference. Conventional FCS-MPC methods evaluate and apply control at every sampling period, $T_s$. If the conventional methods are directly applied, the resulting pulse train will not be evenly distributed, as is depicted in Figure 2.7, but will follow the behaviour that is depicted in Figure 2.6.

Various techniques have been presented [4; 24; 66] to limit the switching frequency by adding soft constraints to the cost function as well as hard constraints which limit the physical number of switching transitions. Soft constraints are typically implemented in the cost function as terms that penalise the number of transitions. The switching frequency is therefore limited by selecting the state that minimizes the tracking error for the least number of switching transitions. These methods, however, typically predict one sampling period $T_s$ ahead and do not take the repetitive nature of the desired pulse train into account. In some cases a higher prediction horizon may be chosen [21; 19], but this presents challenges in terms of practical implementability and complexity, especially when a large number of switching possibilities have to be evaluated in a small amount of time.

In order to realise a practical FCS-MPC controller with waveform quality that is comparable to PWM, a method is required to reduce the number of prediction possibilities in order to allow the controller to be evaluated at a sufficiently high rate. Additionally, an alternative prediction method is needed which predicts the switching behaviour across one switching period, $T_{sw}$, and not only across one sampling period, $T_s$.

## 2.5 Control problem and objectives

### 2.5.1 Background

Mechanical tap changers are commonly used as voltage regulators on distribution feeders to manage voltage regulation. With the growing demand for embedded renewable generation, the impact of embedded sources on distribution feeders necessitates the investigation of future grid devices such as power electronic converters. In [71], an investigation was done to determine the influence of photovoltaic generators on the voltage control of distribution feeders and how the maximum generator penetration levels of these feeders can be increased. The study found that the maximum penetration level of the feeders are limited by the rapid voltage change or voltage rise on the feeder.

Various technologies for increasing the penetration level of distributed generation were discussed and, among those, are the use of electronic voltage regulators. It was shown that when conventional on-load tap changers are replaced by electronic voltage regulators with continuous regulation, it is possible to increase the base penetration levels by between 50% and 80%.

This prompted the investigation for the use of power electronic devices to replace mechanical tap changers and the work in this dissertation forms part of that research initiative. The use of power electronic devices for medium and high voltage applications has been limited until now, due to the fact that the operating voltage is much higher than the maximum breakdown voltage of any commercially available IGBT. In [72], it is shown that an AC-to-AC converter in an auto-transformer configuration can be used to apply control to 10 % of the line voltage and thereby limit the maximum voltage across the power electronic switches. This approach was implemented and experimentally demonstrated in [73] for a 6.35 kV distribution line and in [74] for a 12.75 kV.

The detailed hardware design of the Medium Voltage Electronic Voltage Regulator (MVEVR) in [74] is presented in Appendix A. The design is analysed by simulation and the expected behaviour is experimentally verified for a single-phase 12.75 kV configuration. The MVEVR consists of a multi-level AC-to-AC converter topology that is connected to a transformer in a shunt-series configuration. The control of multi-level converters, especially for high voltage and high power configurations, often poses a challenge and requires strict balancing and stability to ensure that the physical limits of the hardware are not exceeded and that thermal limits of the IGBTs are maintained.

### 2.5.2 Objectives

The control objectives describe the desired behaviour and expected outcome of the system and ultimately determine how the controller is designed. In this dissertation, the control of a series-stacked medium voltage electronic voltage regulator MVEVR is the primary

objective.

Conventional implementations of FCS-MPC [4; 19; 24; 26; 43; 44; 38; 51; 69; 70; 21] are typically characterised by a variable switching frequency, a high noise floor and a large voltage and current ripple when doing voltage and current control. This is largely due to the fact that FCS-MPC has a much lower resolution on the time axis when compared to a discrete implementation of a PWM modulator with a linear controller. However, FCS-MPC also presents advantages over PWM with linear controllers when controlling multi-level converters. As previously discussed in this chapter, some of these advantages include the control of multiple state variables without the need for complex control loops, a controller design that is intuitive and easy to adapt and the fact that no modulator saturation or integrator wind-up can occur. The objective is therefore to develop a FCS-MPC control method with a fixed switching frequency that will compare well to the waveform quality of PWM and which provides the benefits of MPC by controlling multiple state variables.

### Summary of control objectives

*Control of multiple state variables.* Both the MVEVR and the flying capacitor converter requires the control of multiple state variables. The MVEVR consists of two individual AC-to-AC converter modules that are series stacked and the output voltage of each module should be controlled and balanced. The modules are driven from a transformer with one primary winding and two secondary windings, each serving as isolated voltage sources. The large leakage inductance of the transformer windings, connected directly to the bus of each module, may introduce a resonant effect between the transformer leakage inductance and the bus capacitor. In order to keep the bus voltage from resonating, the input current and bus voltage of each module should also be controlled. With the flying capacitor converter, the output voltage should be controlled while actively balancing the two flying capacitor voltages.

*Low total harmonic distortion and accurate reference tracking.* The MVEVR is implemented as a voltage regulator on medium voltage distribution feeders. Consequently, the output voltage waveform should have a low total harmonic distortion (THD) as well as good reference tracking.

*Fast response to reference, load or input changes.* Especially on long distribution feeders in rural areas, the sudden change of a large load can cause a significant voltage drop at the input side of the regulator and a significant change in the load current. The controller should compensate for step changes with acceptable transient effects and maintain the regulator for varying load conditions.

*Fixed switching frequency.* Most inverters are designed so that the resonant frequency of its filters are not excited by the switching frequency or side bands. However, when a variable switching frequency is employed on such a system, such as the MVEVR, the lower switching frequencies may excite the resonant effect between the bus capacitor and leakage inductance. In [44; 4], it is shown that for a variable switching frequency the output frequency spectrum can be manipulated by adding an appropriate term to the cost function. However, it was shown that the method proved to be less effective at low frequencies. If a fixed switching frequency is implemented, it becomes easier to ensure that resonant poles are not excited. As a further advantage, a fixed switching frequency becomes helpful for loss calculations by ensuring that the system always operates within safe thermal limits and assists with EMI compliance.

*Independent of the load impedance.* In most power inverter applications the load is unknown and the controller should be able to track the reference for a range of load conditions. The controller should therefore make provision for an unknown load and maintain tracking accuracy while minimizing transient effects.

*Insensitive to deviations in the plant model.* Although a converter is designed with known components values, the actual values often varies. This is due to component tolerances, temperature fluctuations as well as parasitic inductance and capacitance that are not taken into account. The controller should be able to track the references even when small deviations in the plant model occurs.

*Reject converter imperfections such as dead time.* The controller should be able to reject imperfections in the converter such as dead time, measurement delays and computational delays.

*Reject measurement noise disturbances.* No measurement is perfectly free from noise. High power converters are especially prone to measurement noise as a result of switching. Although design precautions are usually taken to minimize measurement noise, the controller should still be able to reject measurement noise, should it be present.

### Achieving the objectives

The proposed FCS-MPC control method for a fixed switching frequency is developed in Chapter 3. The design and experimental verification of the MVEVR hardware is presented in Appendix A and the controller design and evaluation is detailed in Chapter 4. To demonstrate the control method in general, the control of a five-level flying capacitor converter is presented in Chapter 5 and the control of a single-leg inverter is compared to a linear PWM-based controller in Chapter 6.

## 2.6 Summary

This chapter presented a brief overview of the background and motivation behind the work presented in this dissertation. In the fist part of this chapter, the an overview of the control of power electronics is given with a more detailed view on finite-control-set model predictive control. Thereafter the limitations of existing MPC techniques are discussed followed by the control problem and objectives of the subsequent chapters in this text.

# Chapter 3

# Finite-Control-Set Model Predictive Control With a Fixed Switching Frequency

## 3.1 Introduction

This chapter presents the development of a Finite-Control-Set Model Predictive Control (FCS-MPC) method to achieve a fixed switching frequency. The first section of this chapter, Section 3.2, forms the foundation of this dissertation and presents the detailed development of an FCS-MPC method to achieve a fixed switching frequency. In order to achieve a fixed switching frequency, switching constraints are defined by using the behaviour of PWM to define regions during which only specific switching transitions can be made. To account for these constraints in the predictions, a method for predicting the average value over one switching period is presented. This method is then further extended to allow predictions to be made over a horizon of multiple switching periods.

The modelling and practical implementation of the controller is discussed in Section 3.3. An overview of the control block diagram is given together with the modelling and implementation of the controller, the modelling of an unknown load, considerations for obtaining the control reference and the implementation of the cost function. The realisation of the controller is divided into two parts: The calculation and storage of off-line calculations and the execution of the on-line controller. The practical realisation of these two parts are discussed and a generalised controller structure is derived for implementation on an FPGA.

Lastly, in practical systems the complete state vector is not always directly available through measurements and in such cases state estimation is required. In Section 3.4, the implementation of a switched current estimator is discussed, due to it's simplicity and ease of implementation. Although not presented in this text a more sophisticated estimator such as a Kalman filter can also be used.

## 3.2 FCS-MPC method to achieve a fixed switching frequency

### 3.2.1 Switching constraints based on a triangular carrier

The proposed switching constraints are derived by using the switching behaviour of PWM to define regions where only specific switching states may be applied. The goal is to limit the number of predictions to a choice between only two possible switching states for a given segment in time. In this section, the constraints are defined for a case where the behaviour of one triangular carrier is used. Thereafter the constraints are extended to follow the behaviour of PWM with two phase shifted triangular carriers, followed by the definition for any number of triangular carriers. Lastly, the implementation of Phase-Disposition and Carrier-Disposition PWM is discussed.

#### 3.2.1.1 One carrier

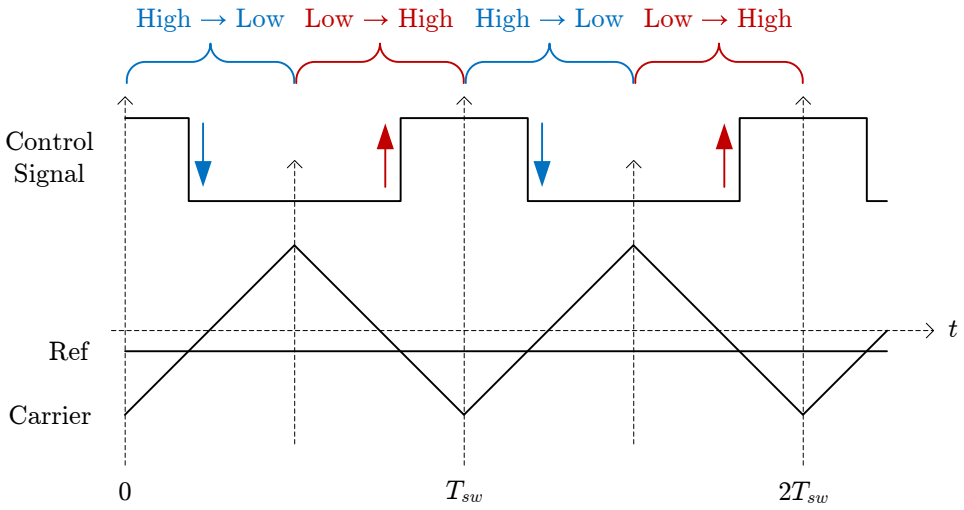



Figure 3.1: Depiction of the PWM pulse train for a single triangular carrier

The switching behaviour of regularly sampled PWM with a triangular carrier is depicted in Figure 3.1. For the purpose of describing the switching behaviour of the carrier, the period is taken between two minima points of the carrier waveform. A PWM modulator with one carrier produces a repetitive pattern of transitions between two switching states where a specific transition is bound to a specific segment of the carrier's period. In the first half of the switching period, $0 \leq t < \frac{T_{sw}}{2}$, the control signal begins in a *high* state and remains *high* until the reference intersects with the carrier. After the intersection, the control signal turns *low* and remains *low* for the remainder of the first half of the period. Therefore, the first half of the period represents a time segment during which one *high*-to-*low* transition can be made and where the point of transition is determined by

the reference. The inverse is true for the second half of the carrier's period. The second half of the period, $\frac{T_{sw}}{2} \leq t < T_{sw}$, represents a time segment during which one *low*-to-*high* transition can be made. This behaviour can be used with FCS-MPC to achieve fixed frequency switching by defining time segments during which only a specific transition is allowed to occur and which may only occur once.

In Figure 3.1 it is shown that the switching transitions occur at arbitrary positions within the switching period, where the reference crosses the carrier. However, FCS-MPC does not use a carrier but applies the switching states directly to the plant. The switching states can therefore only be updated at intervals of the sampling period $T_s$. To allow the FCS-MPC controller to apply a switching state at positions within the switching period, the sampling frequency has to be higher than the switching frequency.

The ratio between the sampling frequency and the switching frequency can be defined by choosing a switching frequency, $f_{sw}$, with period $T_{sw}$ and choosing a desired sampling frequency, $f_s$, with period $T_s$ such that

$$\frac{T_{sw}}{T_s} = N \tag{3.1}$$

where

$$N \quad \in \quad \{2, 4, 6, \dots\} \tag{3.2}$$

and

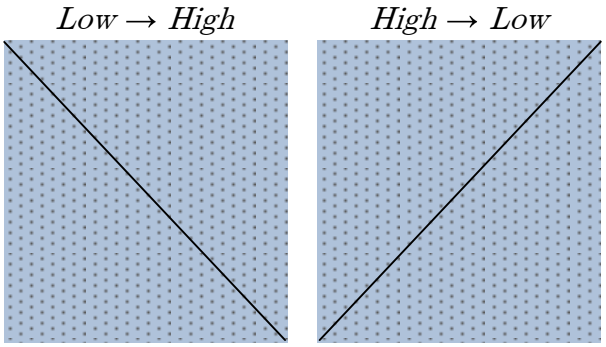
$$N \geq \sigma_N \tag{3.3}$$

with $\sigma_N$ being the number of switching transitions in each switching period. For a single triangular carrier $\sigma_N = 2$. This allows the control algorithm to be evaluated $N$ times during every switching period and at least once for every possible transition. A step index $n$, shown in Figure 3.3, is defined as the switching period step counter and is incremented with each sampling period $T_s$. The step counter is defined as

$$n \quad \in \quad \{0, 1, 2, 3, \dots, N-1\} \tag{3.4}$$

and is used to keep track of the position within each switching period. The step counter, $n$, is not a discrete implementation of a PWM carrier and is always incremented from 0 to $N-1$ in steps of 1. Although the analogy of a PWM carrier is used to define the FCS-MPC constraints, it should not be mistaken for continuous predictive control with a modulator.

In power electronics applications, triangular and sawtooth carriers are typically used, although other types of carriers exist [9]. The carrier waveforms can therefore be viewed as a construct of straight line segments. In this context, a line segment is defined as a single straight line that ends at any intersection with another line or a peak. It was shown that with PWM, each line segment of the carrier constitutes a transition from one switching state to another. This same principle can be applied to FCS-MPC by using the line segments to describe a choice between two switching states.




(a) *Low*-to-*High* transition (b) *High*-to-*Low* transition

Figure 3.2: The two region types for a triangular carrier, representing two switching transitions.

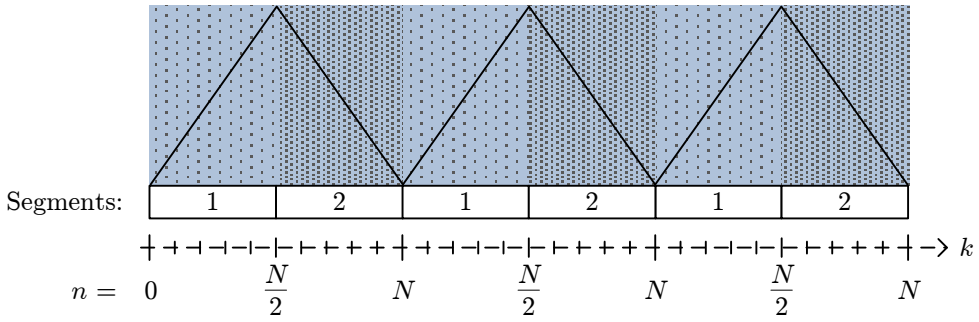


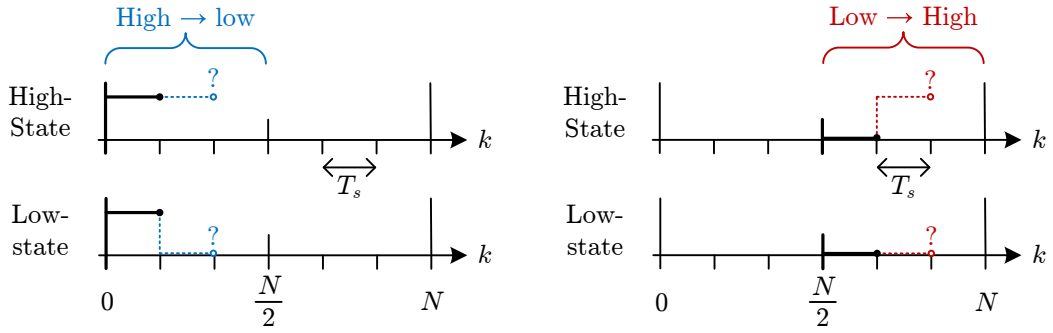

Figure 3.3: Layout of the prediction segments for a single triangular carrier

The line segments can therefore be used to define regions within which the predictive control problem is reduced to a choice between two switching states. This is accomplished by defining a region as a rectangular area which encloses a line segment such that the line stretches diagonally across the region. For a triangular carrier two types of regions are defined and is shown in Figure 3.2. A region with a line segment stretching diagonally from the top-left to the bottom-right corner represents a region within which a *low*-to-*high* switching transition can be made. Inversely, a region with a line stretching from the lower-left to the upper-right corner represents a region within which a *high*-to-*low* transition can be made.

A depiction of a triangular carrier and corresponding regions are shown in Figure 3.3. Each switching period contains two line segments and therefore two prediction regions. The first region is defined for the time interval $0 \leq t < \frac{T_{sw}}{2}$ and the second for the time interval $\frac{T_{sw}}{2} \leq t < T_{sw}$. The switching period $T_{sw}$ can therefore be divided into time segments, where each time segment corresponds to the constraints of a region that falls within that time interval.

For the discrete implementation, the time segments can be defined as a range of the step index $n$. Time segment 1 can be defined for the step index range $0 \leq n < \frac{N}{2}$ and corresponds to a region during which a *high*-to-*low* transition can be made. Time segment

2 is defined for the step index range $\frac{N}{2} \leq n < N$ and corresponds to the region during which a *low*-to-*high* switching transition can be made.




(a) Segment 1 prediction choices

(b) Segment 2 prediction choices

Figure 3.4: Prediction behaviour corresponding to a single triangular carrier.

When the step index $n$ is in the range of time segment 1, the predictive controller is evaluated according to the constraints that are defined for the region with a *high*-to-*low* switching transition. A depiction of the prediction choices for time segment 1 is shown in Figure 3.4a. At the beginning of time segment 1, when $n = 0$, it is assumed that the switching state starts in the *high* state. A prediction is made one time step $T_s$ in advance for both switching states and the state that minimises the cost function is selected. The predictions are performed for each step $n$ until a *low* state is selected. Once a *low* state is selected, the controller stops evaluating the system and remains in the *low* state until the end of that time segment is reached.

Although it is assumed that segment 1 starts in the *high* state, if at $n = 0$ the controller decides on the *low* state, the *low* state is immediately applied without first applying a *high* state and the entire segment 1 remains in the *low* state. During segment 1 it is expected that a *high*-to-*low* transition should be made, but if the control evaluation never decides on a *low* state during the segment the entire segment 1 is allowed to remain *high* without forcing a *high*-to-*low* transition.

When the step index $n$ is within the range of segment 2, the controller is evaluated according to the constraints of the given region, which is a *low*-to-*high* transition. The prediction behaviour is the same as that of time segment 1, but for the inverse of the switching states as depicted in Figure 3.4b. A prediction is made for one time step $T_s$ in advance for both of the switching states and the state that minimises the cost function is selected. The controller is executed for each step $n$ until the *high* state is selected. Once a *high* state is selected, the evaluations stop and the control signal remains in the *high* state until the end of the segment, when $n = N$. When the end of the switching period is reached, $n$ is reset to 0 and the control is evaluated for the next switching period.

This method reduces the control problem to a choice that is always between two switching states and allows the FCS-MPC controller to be evaluated at a rate that is

much higher than the switching frequency. A fixed switching frequency is achieved by dividing the switching period into time segments and allowing only one predefined switching transition to occur in that segment.

The implementation of the constraints for one carrier represents the control of a system which only has two switching states. However, FCS-MPC controllers are often implemented on systems with multiple switching states where multiple state variables are to be controlled. In the following sections, the controller is elaborated for two carriers, which represents a system with four possible switching states. Thereafter, the control strategy is defined for any number of carriers representing any number of switching states. By predicting only one time step $T_s$ in advance, the repetitive nature of the expected pulse train is not taken into account. Later on, an alternative method is presented for predicting the average value over the switching period $T_{sw}$.

#### 3.2.1.2 Two Phase-Shifted Carriers

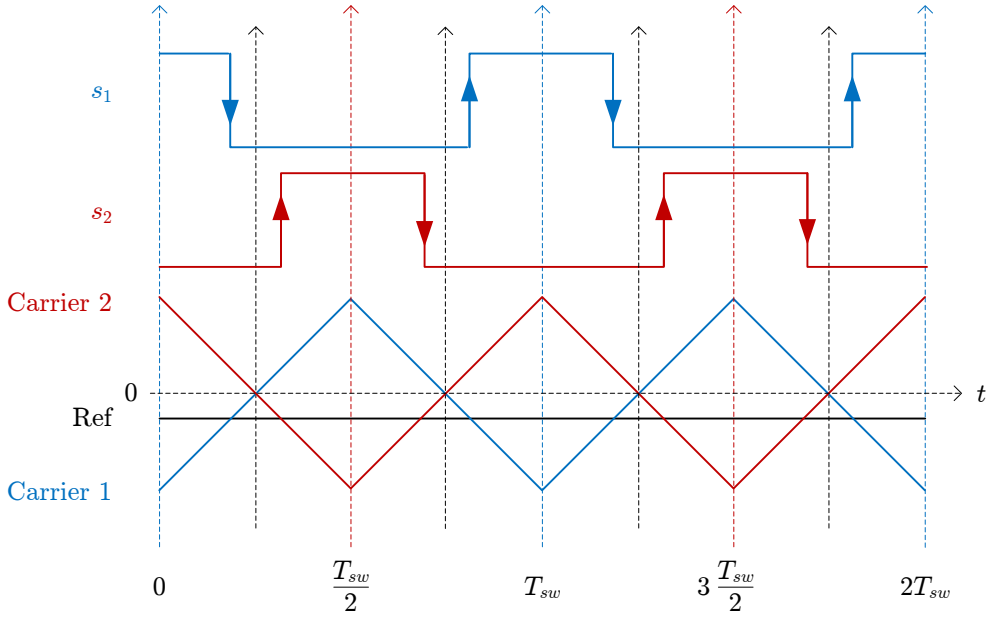
FCS-MPC does not use a modulator, but produces a switching vector $\mathbf{S}$ that is directly applied to the plant. When PWM with one carrier is used, one switching function is generated that can be taken as a scalar function $s$ that is directly applied to the plant. The function $s$ can be in one of two states; a *high* state or a *low* state. However, when PWM with more than one carrier is used, a switching function is generated for each carrier. These functions can be defined by a switching vector such as

$$\mathbf{S} = [s_1, s_2, s_3, \ldots, s_n] \tag{3.5}$$

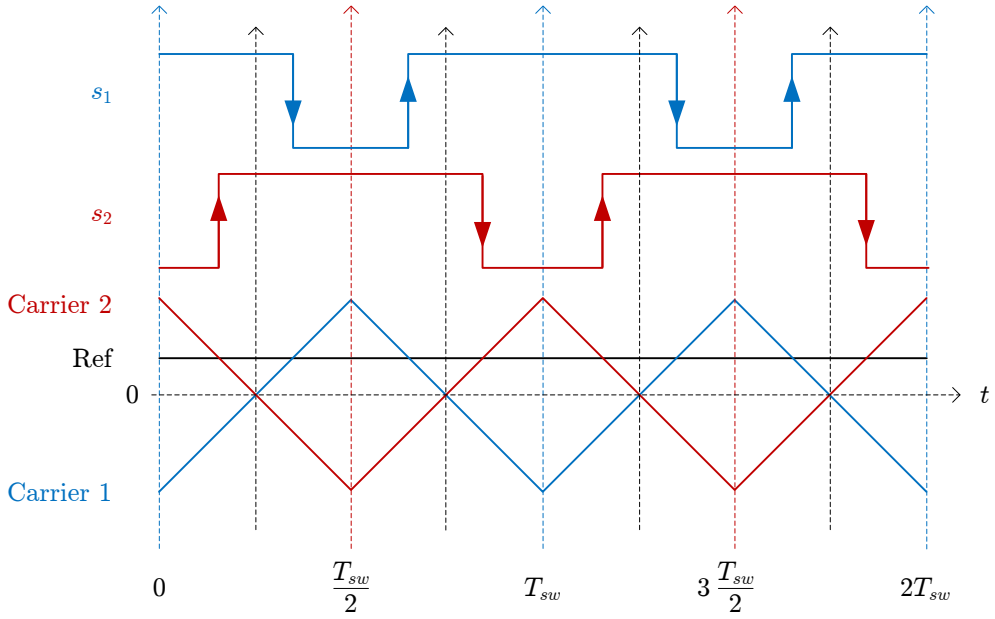
where $\mathbf{S}$ is the switching vector and $s_1$ to $s_n$ are the switching functions of each carrier.

The switching behaviour of PWM, with two triangular carriers are depicted in Figure 3.5. In the previous section it is shown that a PWM modulator with one carrier produces a repetitive pattern of transitions between two states where a specific transition is bound to a specific segment of the carrier's period. However, when two carriers are employed, one of two different switching transitions are bound to the same segment of time. A switching transition in this context is defined as a transition between two distinct switching vectors. Compare the same time segment $0 \leq t < \frac{T_{sw}}{4}$ in Figures 3.5a and 3.5b: When the reference is in the negative, $s_1$ has a *high*-to-*low* transition while $s_2$ remains in the *low* state. When the reference is positive, $s_1$ remains in the *high* state while $s_2$ has a *low*-to-*high* transition. This shows that two different transition patterns exist; one for when the reference is positive and another when the reference is negative. A summary of these transitions is given in Table 3.1.

Choose a switching frequency $f_{sw}$ and sampling frequency $f_s$ according to the definitions in (3.1), (3.2) and (3.3). For two carriers, eight distinct switching transitions exist, but only four can be applied during one switching period. In the previous section, a time segment was defined as a segment of the switching period during which only one transition




(a) Reference below the intersection of the two carriers.




(b) Reference above the intersection of the two carriers.

Figure 3.5: Depiction of PWM with two phase shifted triangular carriers and their respective switching functions.

may be made. Therefore, the number of time segments in a switching period represents the number of transitions that is allowed. The value of $\sigma_N$ in (3.3) is thus the number of time segments in each switching period. For the case of two carriers, $\sigma_N$ becomes four. This allows the controller to be evaluated $N$ times during every switching period and at least once for each transition.

Define the switching period step counter $n$ according to the definition in (3.4) and divide the carrier waveform into regions by enclosing each individual line segment diagonally

**Reference in the negative half:**

| **Period:** | $0 \leq t < \frac{T_{sw}}{4}$ | $\frac{T_{sw}}{4} \leq t < \frac{T_{sw}}{2}$ | $\frac{T_{sw}}{2} \leq t < \frac{3T_{sw}}{4}$ | $\frac{3T_{sw}}{4} \leq t < T_{sw}$ |
|---|---|---|---|---|
| **State of $s_1$:** | *high*-to-*low* | *low* | *low* | *low*-to-*high* |
| **State of $s_2$:** | *low* | *low*-to-*high* | *high*-to-*low* | *low* |

**Reference in the positive half:**

| **Period:** | $0 \leq t < \frac{T_{sw}}{4}$ | $\frac{T_{sw}}{4} \leq t < \frac{T_{sw}}{2}$ | $\frac{T_{sw}}{2} \leq t < \frac{3T_{sw}}{4}$ | $\frac{3T_{sw}}{4} \leq t < T_{sw}$ |
|---|---|---|---|---|
| **State of $s_1$:** | *high* | *high*-to-*low* | *low*-to-*high* | *high* |
| **State of $s_2$:** | *low*-to-*high* | *high* | *high* | *high*-to-*low* |

Table 3.1: Summary of the switching transitions for two phase shifted triangular carriers.

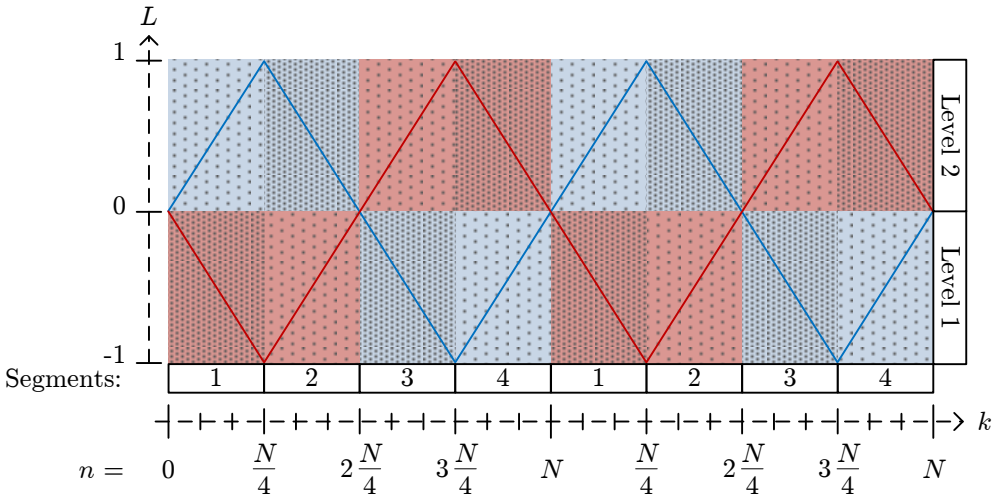



Figure 3.6: Layout of the prediction segments for two phase shifted triangular carriers.

within each region.

A depiction of the waveform and regions are given in Figure 3.6. It is shown that one period of the combined carrier waveforms can be constructed by eight line segments, which defines eight prediction regions.

When one carrier is used the regions are arranged along the one dimensional time axis, where each region corresponds to a time segment. However, when more than one carrier is used the regions are arranged along the time axis but a vertical axis is added which is defined as the region level. Therefore, when two carriers are used, two levels are defined and two regions are bound to the same time segment.

It is shown in Figure 3.6 that the regions in level 1 are bound within the vertical range $-1 \leq L < 0$ and the regions in level 2 within the range $0 \leq L < 1$. The period step index $n$ is divided into a range of prediction segments where each segment corresponds to the constraints of the regions that fall within that range. The ranges of the four time

segments are defined as

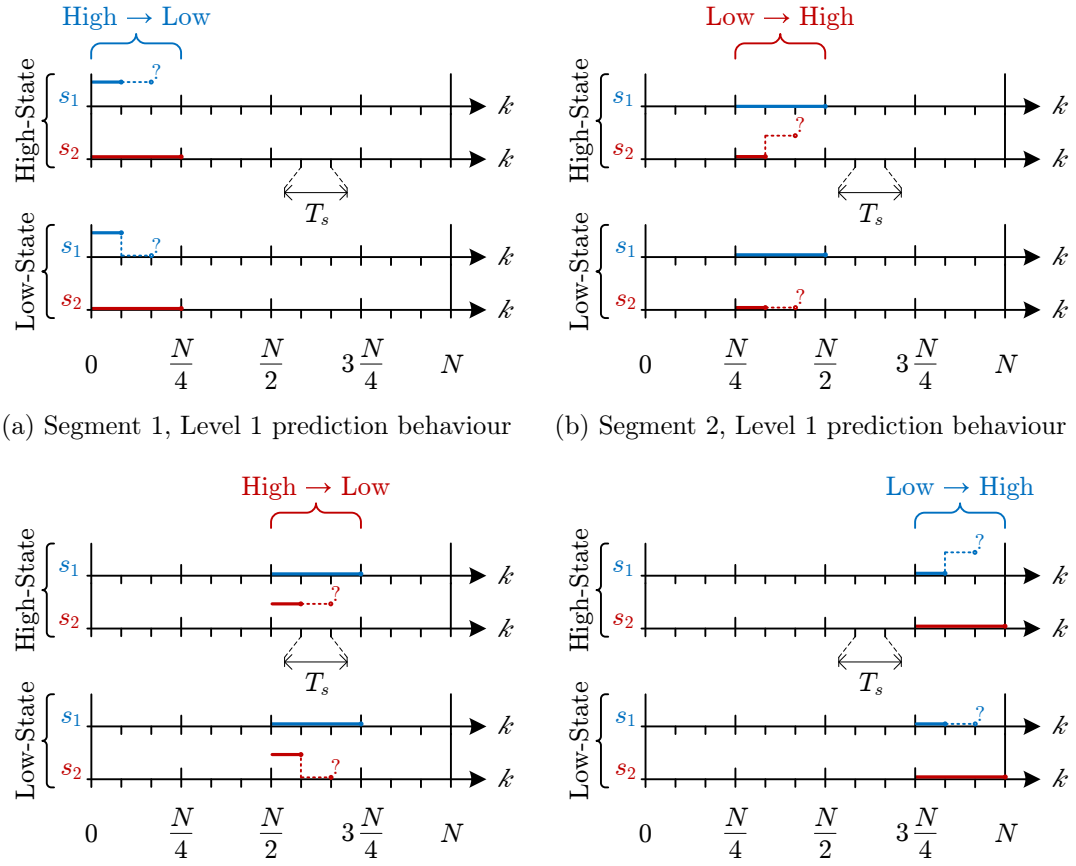
$$0 \leq n < \frac{N}{4} \tag{3.6}$$

$$\frac{N}{4} \leq n < \frac{N}{2} \tag{3.7}$$

$$\frac{N}{2} \leq n < \frac{3N}{4} \tag{3.8}$$

$$\frac{3N}{4} \leq n < N. \tag{3.9}$$

The prediction behaviour of the four regions during level 1 is depicted in Figure 3.7.




(a) Segment 1, Level 1 prediction behaviour

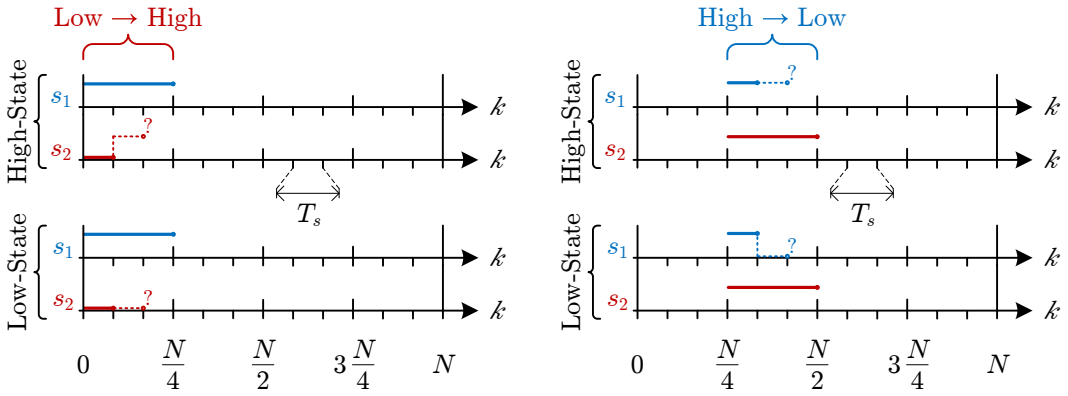
(b) Segment 2, Level 1 prediction behaviour

(c) Segment 3, Level 1 prediction behaviour

(d) Segment 4, Level 1 prediction behaviour

Figure 3.7: Prediction behaviour for Level 1 of two phase shifted triangular carriers.

During time segment 1 a prediction is made, one $T_s$ in advance, for the two possible switching states of $s_1$ while the state of $s_2$ is kept *low*. Time segment 1 is evaluated until a *low* state is applied to $s_1$ or until the end of the segment is reached. During time segment 2, the state for $s_1$ is forced *low* and kept *low* while predictions are made for $s_2$. Time segment 2 is evaluated until the state of $s_2$ has done a *low*-to-*high* transition or until the end of the segment is reached. The behaviour of time segment 3 is similar to segment 2, with the difference that a *high*-to-*low* transition for $s_2$ is expected. In the last segment, $s_2$ is kept *low* while predictions are made for $s_1$.




(a) Segment 1, Level 2 prediction behaviour

(b) Segment 2, Level 2 prediction behaviour

(c) Segment 3, Level 2 prediction behaviour

(d) Segment 4, Level 2 prediction behaviour

Figure 3.8: Prediction behaviour for Level 2 of two phase shifted triangular carriers.

During level 1, the switching function of one of the two carriers is kept *low* for an entire time segment while a prediction is made for the other switching function. The prediction behaviour of level 2 is similar to that of level 1, with the difference being that the one switching function is kept *high*, while a prediction is made for the other. The prediction behaviour of level 2 is shown in Figure 3.8. This method simplifies the prediction problem by defining time segments, based on the characteristics of PWM, during which only one of two switching vectors may be selected.

### Selecting the Prediction Level

When two carriers are used, two prediction levels exist for each prediction segment, which results in four prediction choices. However, the predictions should always be reduced to a choice between two switching states. Three methods are proposed for determining which prediction level should be used.

*Method 1: Reverse Duty Cycle.* In some applications of voltage control, the phase difference between the reference input and the duty cycle of PWM may be considered negligible.

In such cases, the duty cycle $d$ can be calculated as a function

$$d = f(x_{out}, \mathbf{U}) \tag{3.10}$$

where $x_{out}$ is the primary controlled state variable and $\mathbf{U}$ is the converter input. When the FCS-MPC controller performs the predictions for a given time segment, the duty cycle $d$ is used to determine the region level that should be used during the time segment. This method can be used with any number of prediction levels.

*Method 2: Static Segment Counting.* This method is valid for any implementation of the proposed FCS-MPC method but can only be applied when the switching period is divided into $N$ steps according to (3.1) and (3.2) and where (3.3) is replaced with

$$N \geq 2\sigma_N \tag{3.11}$$

where $\sigma_N$ is the number of prediction segments in each switching period. This requires that each prediction segment should have at least two prediction steps.

This method works on the principle of counting the number of segments during which the switching function remains in one state and incrementing or decrementing the prediction level accordingly.

When the switching function of a certain number of consecutive time segments remain in the *high* state for the full duration of the segment (i.e. no switching transition has been made), the prediction level is incremented. Likewise, when the switching function of a certain number of time segments remain in the *low* state for the full duration of each segment, the prediction level is decremented. A threshold can be defined to set the number of consecutive segments required before a transition is made.

*Method 3: Anchored Static Segment Counting.* In some implementations of Method 2, a low level-transition threshold is desired. However, when the threshold is taken too low the control algorithm can start to run between the prediction levels during transients, resulting in exacerbated transient effects. This phenomenon only becomes a problem when three or more prediction levels are defined. The Anchored Static Segment Counting method can be used to suppress exacerbated bouncing between prediction levels.

Anchored Static Segment Counting is obtained by applying Method 2 to determine the desired level $L$, but defining an Anchor Level $L_A$ according to Method 1 and restricting $L$ to

$$(L_A - 1) \leq L \leq (L_A + 1) \tag{3.12}$$

together with

$$1 \leq L \leq (L_N) \tag{3.13}$$

where $L_N$ is the defined number of prediction levels. Note that this method can only be applied when three or more carriers are defined and is not applicable to the example of two carriers.

#### 3.2.1.3 Switching vector lookup table

In the previous sections it is shown that the analogy of PWM carriers can be used to construct regions during which only one switching transition is allowed. This is accomplished by defining the regions along a two-dimensional plane based on the points of intersection of the carriers. The horizontal axis depicts the time axis which divides the switching period into time segments and the vertical axis depicts the region levels for each time segment.

In order to find the switching vectors that correspond to a given region, the PWM switching functions can be used. Consider the summary of the switching transitions for two phase shifted triangular carriers in Table 3.1. The table summarises the transitions of each switching function for different time intervals and for different reference off-sets. Each time interval corresponds to a time segment and each reference off-set corresponds to a region level.

It is shown in the table that for a corresponding region, only one switching function makes a transition while the other remains constant. This represents the two switching vectors that can be applied in the region. Each region begins with an initial switching vector $\mathbf{S}_A$ and ends with a final switching vector $\mathbf{S}_B$, if a transition has been made.

A switching vector lookup table can be generated that is a function of the time segment and prediction level by using the PWM switching transitions given in Table 3.1. For each region, define $\mathbf{S}_A$ as the switching vector that is applied before a transition is made and $\mathbf{S}_B$ as the switching vector after a transition has been made. The resulting switching vector lookup table for the regions constructed from the two triangular carrier is given in Table 3.2.

When the on-line controller is executed, the switching vectors can simply be read from the lookup table for the current segment of time and region level.

| | **Segment 1** | **Segment 2** | **Segment 3** | **Segment 4** |
|---|---|---|---|---|
| **Level 1** | $\begin{bmatrix}\mathbf{S}_A = [1,0] \\ \mathbf{S}_B = [0,0]\end{bmatrix}$ | $\begin{bmatrix}\mathbf{S}_A = [0,0] \\ \mathbf{S}_B = [0,1]\end{bmatrix}$ | $\begin{bmatrix}\mathbf{S}_A = [0,1] \\ \mathbf{S}_B = [0,0]\end{bmatrix}$ | $\begin{bmatrix}\mathbf{S}_A = [0,0] \\ \mathbf{S}_B = [1,0]\end{bmatrix}$ |
| **Level 2** | $\begin{bmatrix}\mathbf{S}_A = [1,0] \\ \mathbf{S}_B = [1,1]\end{bmatrix}$ | $\begin{bmatrix}\mathbf{S}_A = [1,1] \\ \mathbf{S}_B = [0,1]\end{bmatrix}$ | $\begin{bmatrix}\mathbf{S}_A = [0,1] \\ \mathbf{S}_B = [1,1]\end{bmatrix}$ | $\begin{bmatrix}\mathbf{S}_A = [1,1] \\ \mathbf{S}_B = [1,0]\end{bmatrix}$ |

Table 3.2: State vector lookup table for the regions constructed from two triangular carriers.

#### 3.2.1.4 n-Number of phase-shifted carriers

A prediction pattern can be derived from any number of carrier waveforms for a system with any number of unique switching states. The number of unique switching states

$S_N$ that describe the plant is a function of the number of carriers. Where each carrier represents a choice between two states, $S_N$ can be defined as

$$S_N = 2^C \tag{3.14}$$

with $C$ being the number of carriers.

FCS-MPC generates a switching vector $\mathbf{S}$, which is directly applied to the switches of the converter. The switching vector can be defined as a function of the number of carriers, $C$, as

$$\mathbf{S} = [s_1, s_1, s_3, \ldots, s_C] \tag{3.15}$$

where $s$ represents the switching function of each carrier.

Where the phase of the carriers are evenly distributed across the switching period, such that

$$\Delta\theta = \frac{2\pi}{C} \tag{3.16}$$

where $\Delta\theta$ is the phase difference between the carriers, then the number of time segments, $\sigma_N$, in each switching period, $T_{sw}$, is defined as

$$\sigma_N = 2C \tag{3.17}$$

and the number of levels, $L_N$, as

$$L_N = C. \tag{3.18}$$

An example of the regions for four phase shifted carriers is shown in Figure 3.9. It is shown that when four carriers are used, eight time segments are defined with four levels.

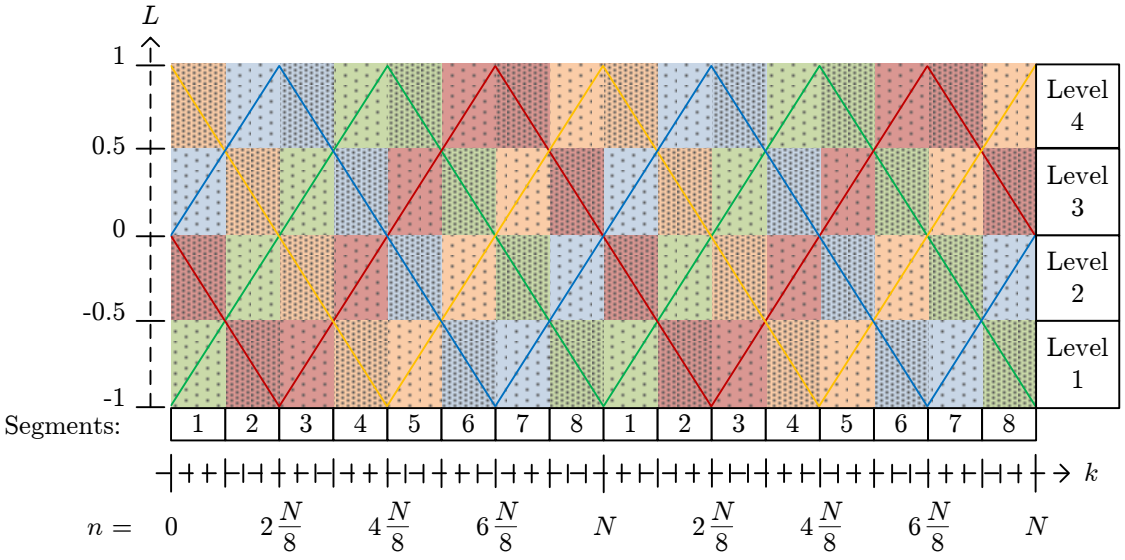



Figure 3.9: Layout of the regions for four phase shifted triangular carriers.

#### 3.2.1.5 Other carrier distributions

*Carrier distribution with phase-disposition*

The prediction constraints discussed in the previous section are derived by using phase shifted triangular carriers [9] as a guide. This is done to introduce the concept for the most basic carrier distribution but it can also be used with any other distribution technique. The prediction regions for two triangular carriers with phase disposition is shown in Figure 3.10. The two carriers are phase shifted by 180° and the levels are phase shifted by 90° with respect to each other. The number of time segments and levels remain the same but the order of the regions are shifted between level 1 and level 2. As with the phase shifted carriers, phase-disposition can also be implemented for any number of carriers.

*Carrier distribution with carrier-disposition*

With carrier disposition the carriers are kept in phase but with a vertical offset so that the carriers never intersect one another. This is shown in Figure 3.11. The number of levels and regions also remain the same as defined in Section 3.2.1.2 and the evaluation and execution of the controller remains the same as discussed in the previous sections.

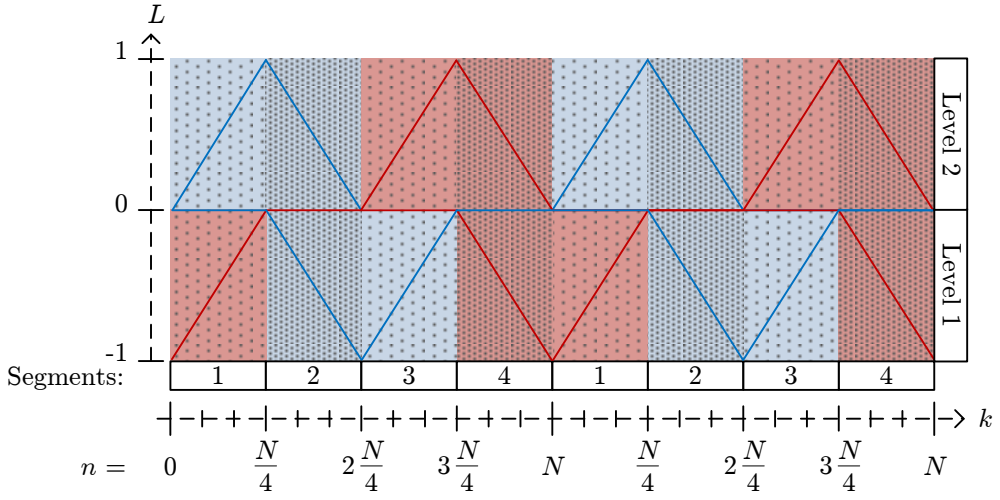



Figure 3.10: Layout of the prediction segments for two triangular carriers with phase-disposition.

### 3.2.2 Prediction method for an averaged receding-horizon policy

The switching constraints discussed in the previous section is defined according to the switching behaviour of a PWM pulse train for a triangular carrier. It was shown that at every sampling step $T_s$ a prediction is made for the switching state at one sampling step in advance. This allows the predictive controller to decide whether to stay in the current switching state or to switch to the next state immediately. Each switching period is divided into time segments during which only a specific switching transition can be made.

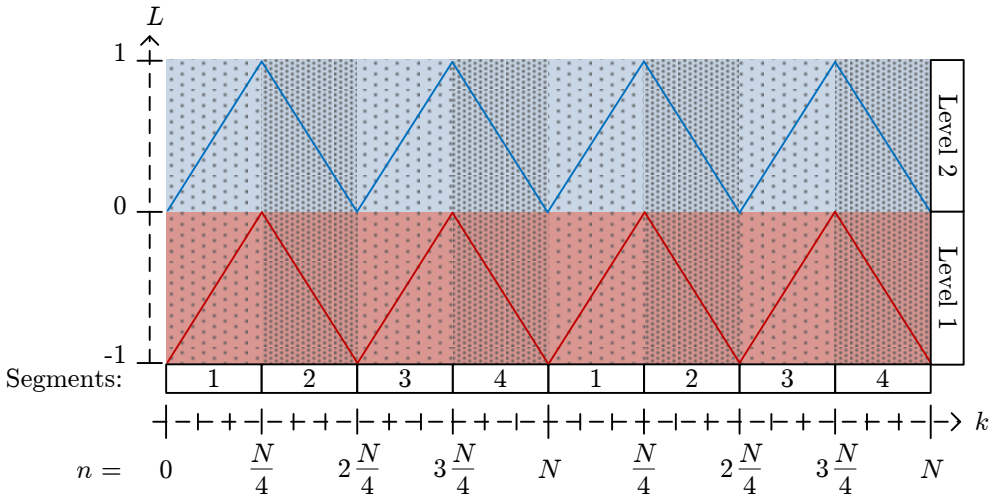



Figure 3.11: Layout of the prediction segments for two triangular carriers with carrier disposition.

This forces the FCS-MPC controller to follow the same pattern of switching transitions as that of PWM.

Ideally, if the sampling frequency of the controller is taken sufficiently higher than the switching frequency, it is expected that the resulting pulse train for a given reference should be similar to that of PWM. However, in the discussion on the limitations of conventional FCS-MPC, it was shown that when the controller is evaluated and applied at the same rate the switching frequency varies. When the predictions of the proposed constraints are made by predicting only one sampling period ahead, the switching constraints and the desired repetitive pulse train will not be taken into account. As a result, the switching transitions are not applied at the optimal positions and the FCS-MPC method fails to produce a good quality output voltage.

In the next Section 3.2.2.1 an alternative method is presented that allows the prediction of one switching period, $T_{sw}$, ahead by taking the repetitive nature of the switching constraints into account. Due to the calculation effort it is not practically feasible with today's hardware to perform an on-line prediction of each sampling step across an entire switching period. To overcome this limitation a method is presented in Section 3.2.2.2 for calculating the average value of the switching state by doing off-line calculations and storing the results in a lookup table.

### 3.2.2.1 Prediction Window

With many applications of current and voltage control the switching frequency is much higher than that of the control reference. It can therefore be assumed that the reference input is constant across one switching period. This allows a prediction to be made for the next pulse width based on the width of the current pulse.

To mimic the pulse train of PWM with a triangular carrier, it is assumed that the

predicted switching pulses are mirrored around the beginning and end of each switching period. A depiction of the prediction window and pulse train for one triangular carrier is shown in Figure 3.12. The width of the predicted pulses is given by $2\Delta\tau$, which is determined by the current position within the switching period, as well as the prediction segment and current switching state. In the first half of the switching period, the width of one side of the pulse is taken as the period between the start of $T_{sw}$ and the current position $t_1$. In the second half, the width of the pulse is taken as the period between the current position $t_2$ and the end of $T_{sw}$.

Two predictions should be made during every evaluation: *a)* the system remains in the current switching state for one more sampling step and *b)* the system switches immediately to the other state. The two predictions can be performed by assuming that the pulse width is increased by one sampling step or that it remains at its current width. This is illustrated in Figure 3.13.

In Figure 3.13a, the prediction window is shown for segment 1, when a *high*-to-*low* transition is predicted. This prediction determines whether it is better to leave the pulse width as it is, or to increase each side with one $T_s$. As the evaluation steps forward in time, the pulse width of the predicted pulses increase until a switching transition occurs or until the end for the segment is reached.

The prediction window for segment 2 is shown in Figure 3.13b. During segment 2 it is assumed that the system starts in the *low* state and that a *low*-to-*high* transition is made. A prediction is made to determine whether each side of the pulses should decrease by one $T_s$ or remain as it is. As the evaluation steps forward the predicted pulse width shrinks until a switching transition is made or the end of the segment is reached.

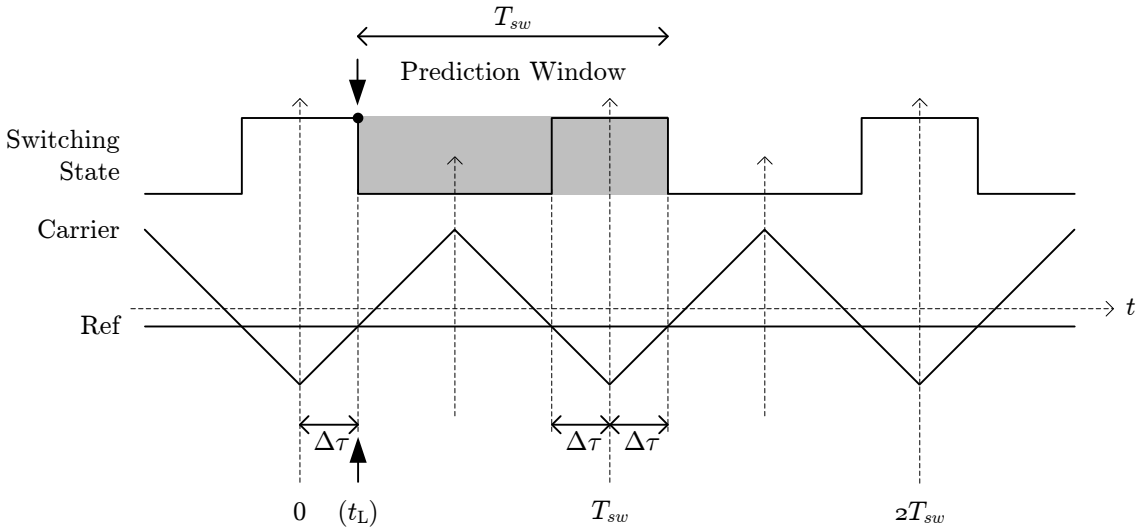
It is shown that during segment 1 the expected behaviour of segment 2 is included in the prediction. However, when the end of segment 1 is reached, a new evaluation begins according to segment 2. This allows the controller to predict the point of transition at each side of the pulse.

#### 3.2.2.2 Averaged off-line calculations

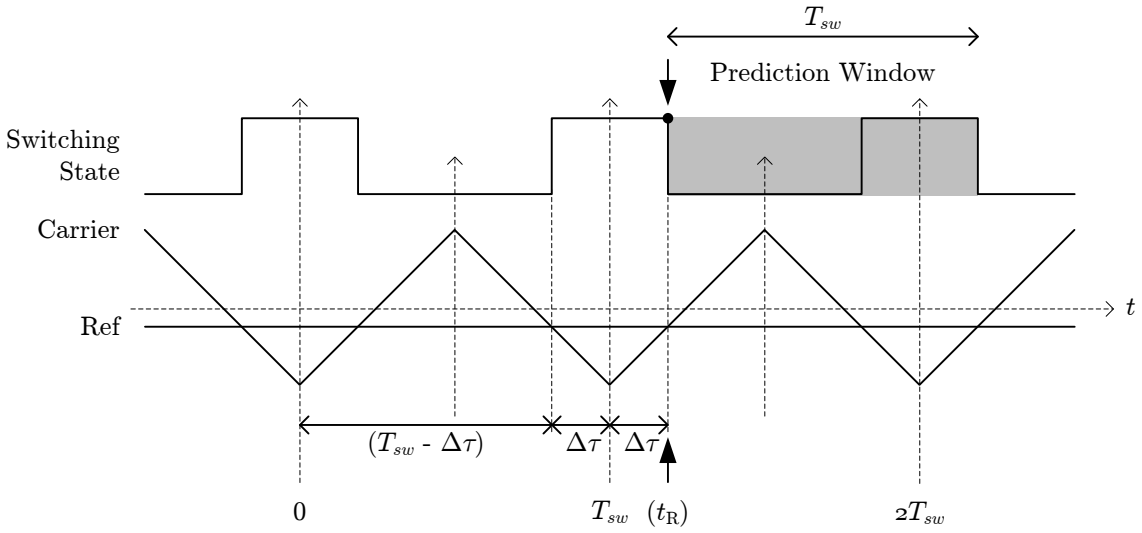
It is not practical to do an on-line calculation of all the sampling steps across one switching period. In this section, a method is proposed to reduce the on-line calculations to a single calculation of the average value of the entire switching period by creating an off-line lookup table.

The plant can be modelled by a state space representation [61], such as

$$\begin{aligned} \dot{\mathbf{x}}(t) &= \mathbf{A_s}\mathbf{x}(t) + \mathbf{B_s}u(t) \\ \mathbf{y}(t) &= \mathbf{C_s}\mathbf{x}(t) + \mathbf{D_s}u(t) \end{aligned} \tag{3.19}$$




(a) Prediction window when predicting in segment 1, on the left half of the switching period




(b) Prediction window when predicting in segment 2, on the right half of the switching period

Figure 3.12: Depiction of the PWM pulse train of a triangular carrier with the prediction window.

where

$$\mathbf{S} = \begin{cases} 1 & \text{for the } \textit{high} \text{ switching state} \\ 0 & \text{for the } \textit{low} \text{ switching state} \end{cases} \tag{3.20}$$

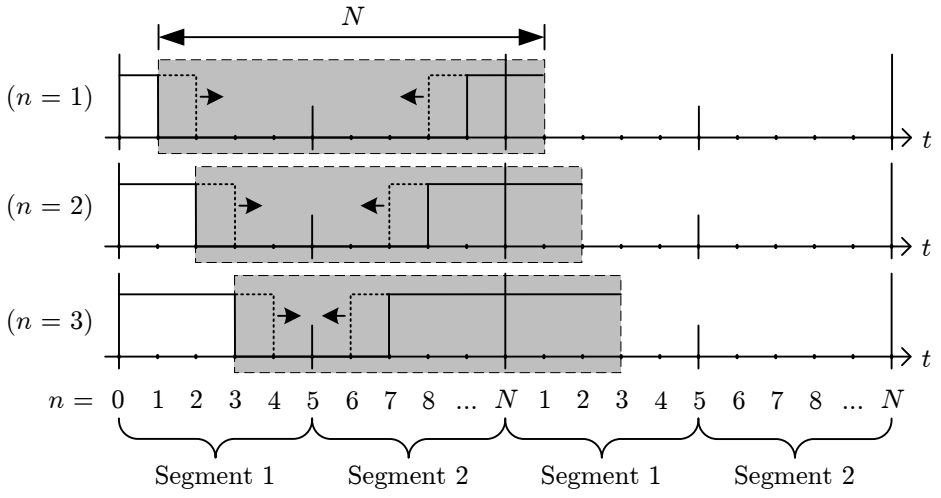
indicates the different state space models for each switching vector $\mathbf{S}$. In this instance, the switching vector is only a scalar value.

The discrete-time state space form [61] of the plant can be used to predict the future state variables one sampling step ahead and is given by

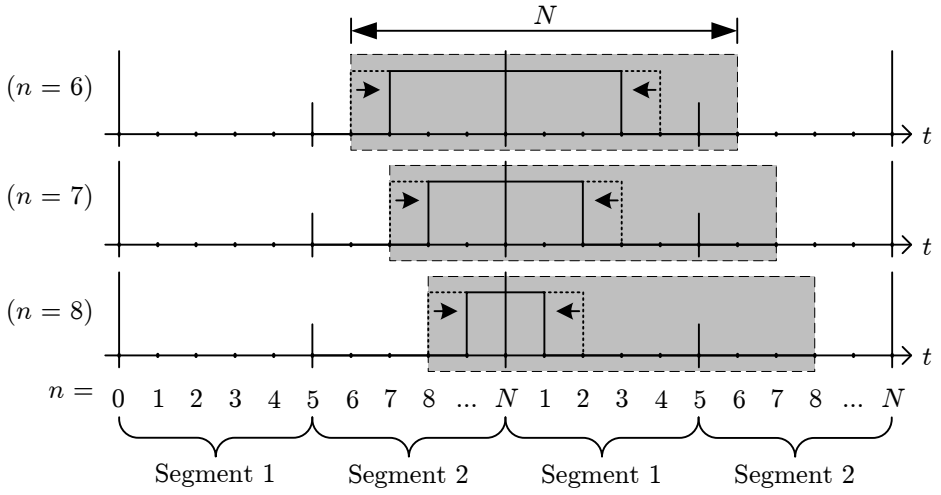
$$\mathbf{x}(k+1) = \mathbf{F_s}\mathbf{x}(k) + \mathbf{G_s}u(k) \tag{3.21}$$

and

$$\mathbf{y}(k) = \mathbf{C_s}\mathbf{x}(k) + \mathbf{D_s}u(k) \tag{3.22}$$




(a) Predictions during segment 1




(b) Predictions during segment 2

Figure 3.13: Depiction of the predicted pulse train across one switching period.

where

$$\mathbf{F_s} = e^{\mathbf{A_s}T_s} \tag{3.23}$$

and

$$\mathbf{G_s} = \int_0^{T_s} e^{\mathbf{A_s}\tau} \mathrm{d}\tau \cdot \mathbf{B_s} \tag{3.24}$$

for a sampling period $T_s$. An equation for the predicted average state vector, when one triangular carrier is used, can be calculated by using Equation 3.21 and stepping through the switching pattern given in Figure 3.13. The two prediction equations for segment 1, when $n < \frac{N}{2}$, is given by

$$\mathbf{x}_{av}^{p}(k,n)_{low} = \frac{1}{T_{sw}} \left( \sum_{m=k}^{k+(N-2n-1)} T_s \mathbf{x}(m+1)_{\mathbf{s}=0} + \sum_{m=k+(N-2n)}^{k+(N-1)} T_s \mathbf{x}(m+1)_{\mathbf{s}=1} \right) \tag{3.25}$$

and

$$\mathbf{x}_{av}^{p}(k,n)_{high} = \frac{1}{T_{sw}}\left(\left[T_s\mathbf{x}(m+1)_{\mathbf{s}=1}\right]_{m=k} + \sum_{m=k+1}^{k+(N-2n-2)} T_s\mathbf{x}(m+1)_{\mathbf{s}=0} + \sum_{m=k+(N-2n-1)}^{k+(N-1)} T_s\mathbf{x}(m+1)_{\mathbf{s}=1}\right) \tag{3.26}$$

where $k$ is the discrete time step and $n$ is the period step index.

Likewise, the predictions for segment 2, when $\frac{N}{2} \leq n < N$, is given by

$$\mathbf{x}_{av}^{p}(k,n)_{low} = \frac{1}{T_{sw}}\left(\left[T_s\mathbf{x}(m+1)_{\mathbf{s}=0}\right]_{m=k} + \sum_{m=k+1}^{k+2(N-n-1)-1} T_s\mathbf{x}(m+1)_{\mathbf{s}=1} + \sum_{m=k+2(N-n-1)}^{k+(N-1)} T_s\mathbf{x}(m+1)_{\mathbf{s}=0}\right) \tag{3.27}$$

and

$$\mathbf{x}_{av}^{p}(k,n)_{high} = \frac{1}{T_{sw}}\left(\sum_{m=k}^{k+2(N-n)-1} T_s\mathbf{x}(m+1)_{\mathbf{s}=1} + \sum_{m=k+2(N-n)}^{k+(N-1)} T_s\mathbf{x}(m+1)_{\mathbf{s}=0}\right). \tag{3.28}$$

These equations describe the predictions for a horizon of one switching period. To calculate the predictions for a higher horizon, the same equations can be iterated until the horizon is reached.

The prediction equations are computationally expensive to calculate on-line. However, since the system consists of a finite set of switching states that are evaluated over a switching period with a known number of sampling steps, the predictions can be done off-line and stored in a lookup table. The predictions are calculated as a function of the current state vector, $\mathbf{x}[k]$, the control input $\mathbf{u}[k]$ and the prediction step index, $n$. This allows the prediction equations to be stored in a state space form, such as

$$\mathbf{x}_{av}^{p}(k,n)_{\mathbf{s}} = \mathbf{\Lambda}(n)_{\mathbf{s}}\mathbf{x}(k) + \mathbf{\Gamma}(n)_{\mathbf{s}}\mathbf{u}(k) \tag{3.29}$$

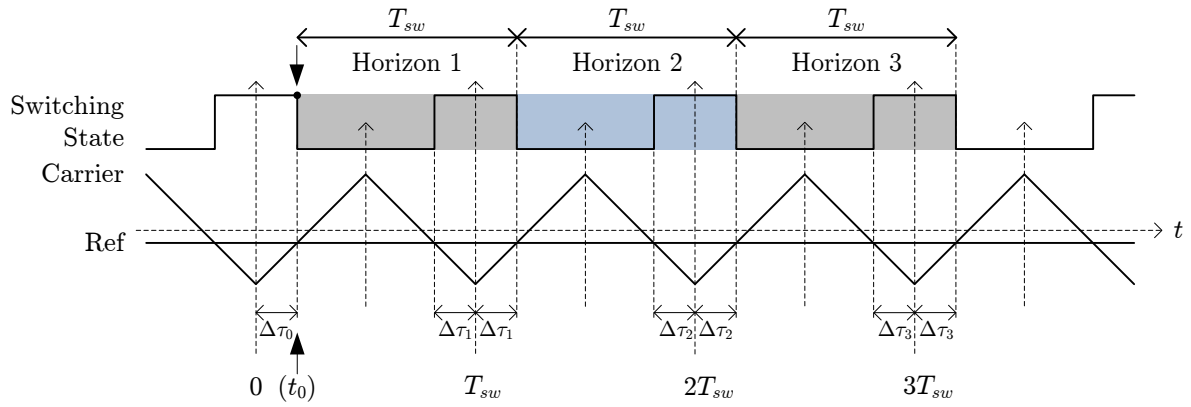
which only requires a vector multiplication with the state vector and input.

### 3.2.3 Increasing the prediction horizon over multiple switching periods

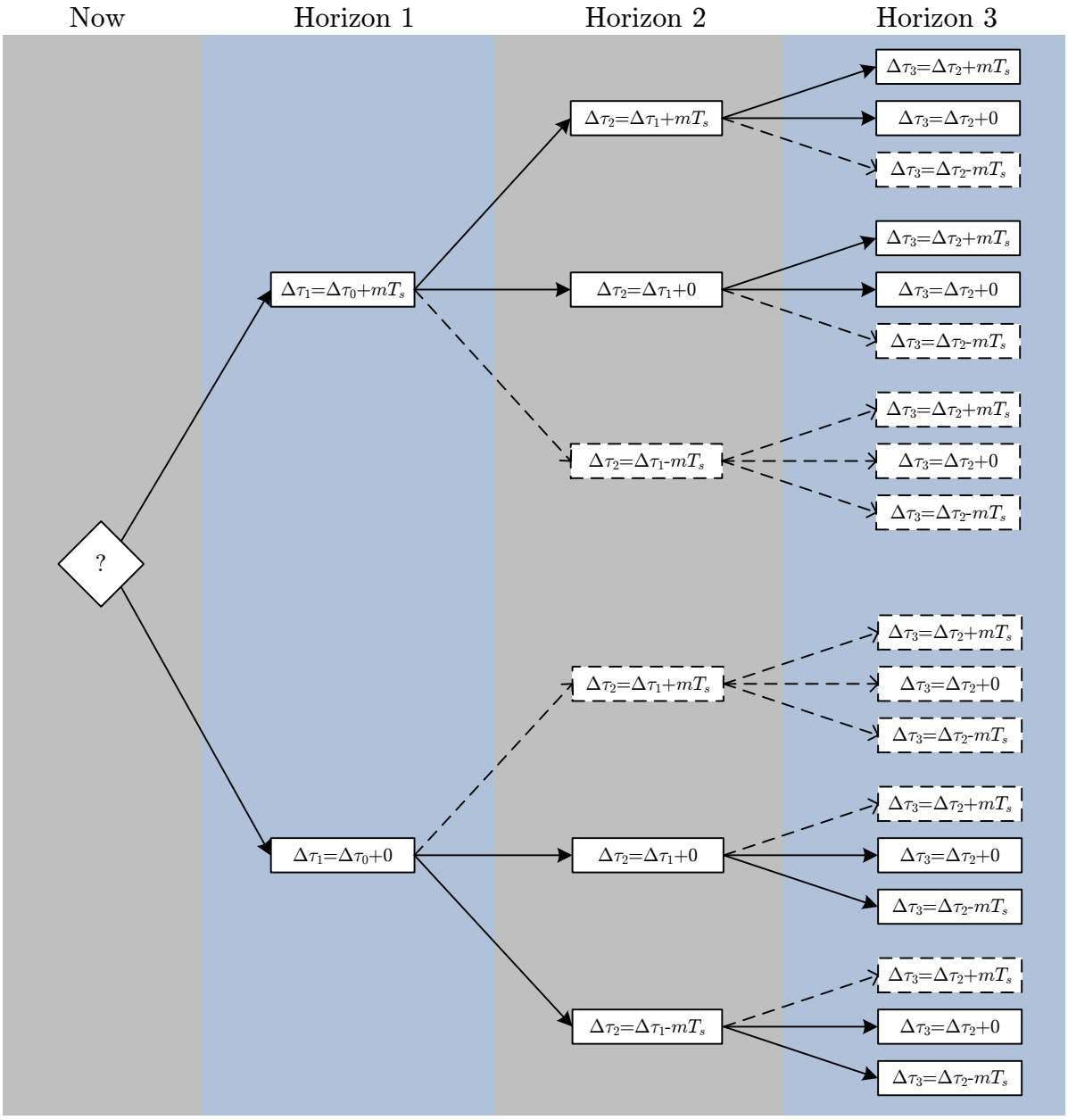
With conventional FCS-MPC methods, the prediction horizon is defined as the number of sampling steps predicted into the future. For each horizon the number of evaluations increase exponentially and if not constrained the number of prediction choices becomes

$$p = (S_N)^h \tag{3.30}$$

where $p$ is the number of prediction choices, $S_N$ is the number of switching states and $h$ is the horizon length. This shows that the number of evaluations at each sampling instance

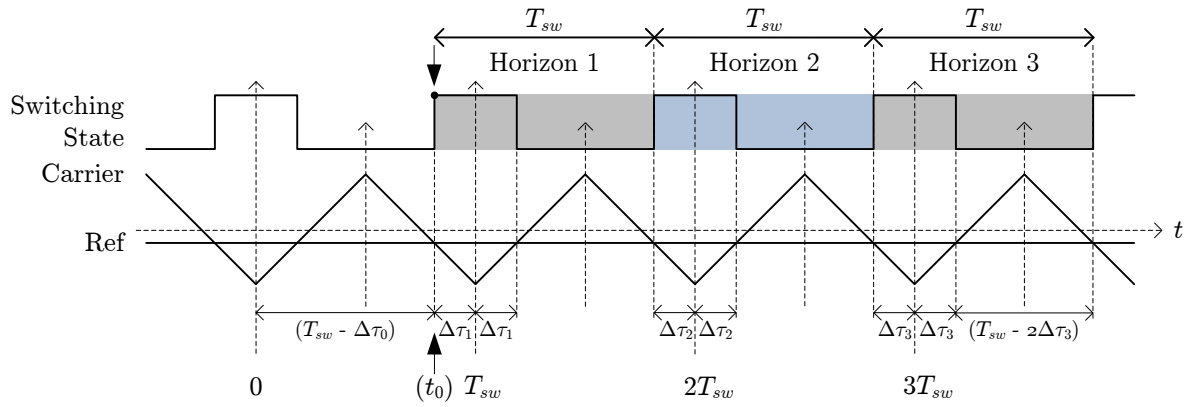



(a) Prediction window during segment 1, on the left half of the switching period

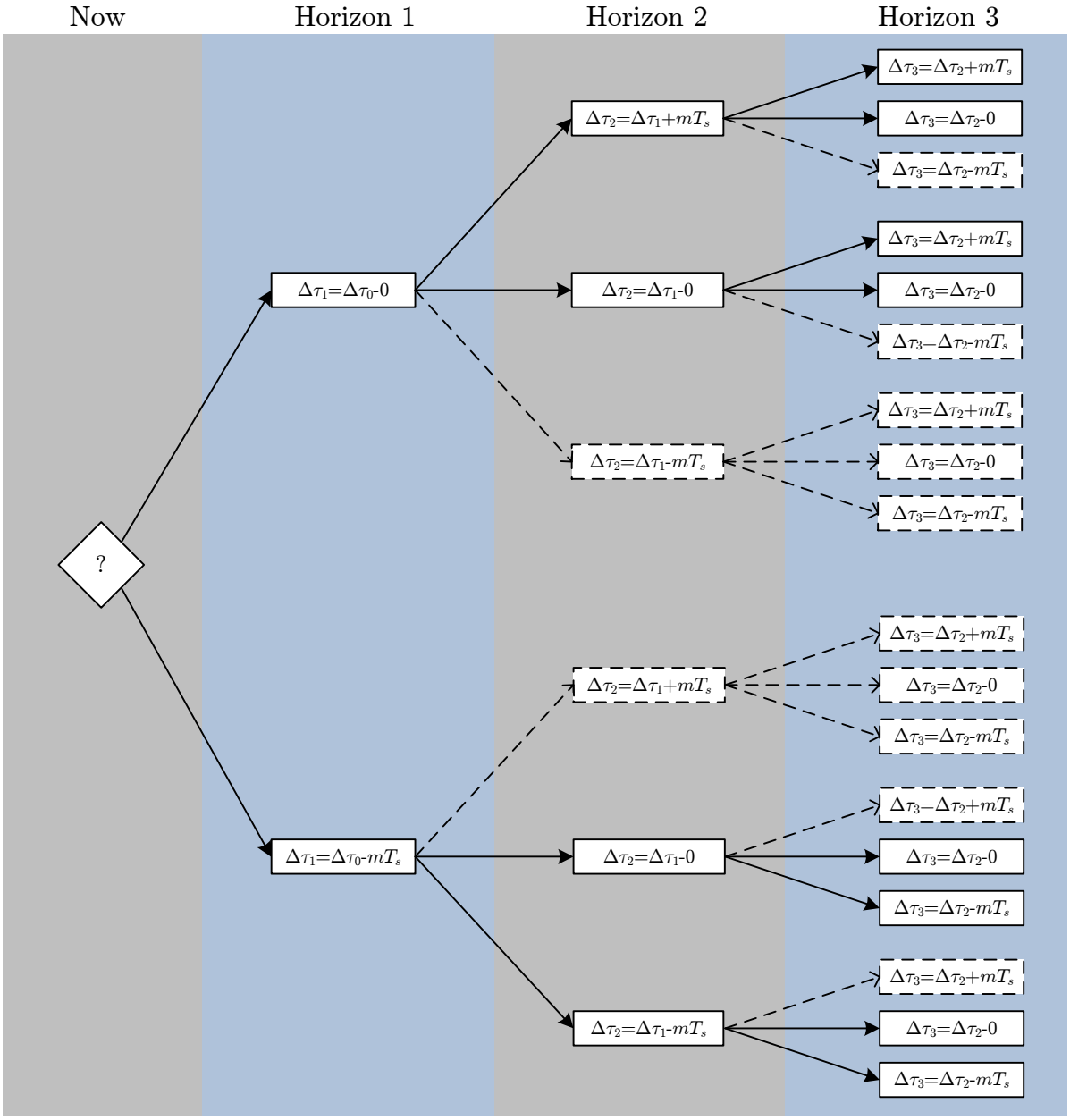



(b) Tree of prediction choices for an increasing pulse width

Figure 3.14: Depiction of the prediction choices for a horizon of 3, when evaluating the left half of a switching period.




(a) Prediction window during segment 1, on the left half of the switching period




(b) Tree of prediction choices for a decreasing pulse width

Figure 3.15: Depiction of the prediction choices for a horizon of 3, when evaluating when evaluating the right half of a switching period.

grows rapidly when the horizon is increased and a practical limit is quickly reached for complex systems. With some inverter topologies the number of prediction choices can be reduced by physical restrictions of the hardware or by ignoring redundant states for a given voltage vector. Even so, in most cases only a horizon of a few sampling steps are practically feasible on an FPGA or micro controller.

Unlike most conventional FCS-MPC techniques the prediction method presented in the previous section does not predict one sampling step ahead but rather the average value across one switching period. Although each switching period is divided into $N$ sampling steps, the online calculation of the average value remains a single calculation. Thus for the controller discussed in this chapter the prediction horizon is defined for the number of switching periods $T_{sw}$ predicted and not the number of sampling periods $T_s$.

The principle of operation of the proposed controller is to advance in steps of the sampling period and predict the behaviour for one switching period ahead. The average value of the controlled variable is forced towards the average value of the reference over the switching period. This is done by estimating the future average value of the reference or by assuming that the reference remains constant over one switching period.

The controller is evaluated by advancing through the switching period $T_{sw}$ in sampling steps of $T_s$ until the optimal pulse width or point of transition is found. Ideally that principle should be applied to obtain the optimal point of transition for each switching period in the future. However, the goal of the proposed control technique is to reduce the number of predictions in order to increase the sampling rate and it is not practically feasible to step through each future switching period to find the optimal point of transition.

In order to work around this limitation, two assumptions can be made about the future pulse widths. Consider the depiction in Figures 3.14a and 3.15a which shows a triangular carrier with the resulting PWM pulse train. In order to mimic the depicted behaviour with FCS-MPC, the predicted future pulse widths for each horizon can be defined as

$$\Delta\tau_n = \{0, 1, 2, 3, h\} \tag{3.31}$$

where $n$ indicates the horizon step index and $h$ the number of horizons predicted. For the *first assumption* it can be assumed that the pulse width will only increment or decrement in multiples of $T_s$ during the subsequent switching periods, such that

$$\Delta\tau_{n+1} = \Delta\tau_n \pm mT_s. \tag{3.32}$$

Choose $m$ to be one of two constant values

$$m = \begin{cases} 0 \\ \{1, 2, 3, ...\} \end{cases} \tag{3.33}$$

which allows the pulse width to either remain unchanged or to be incremented or decremented with a multiple of $T_s$.

The resulting prediction choices can be presented as a ternary tree, where each horizon has the choice to either reduce, maintain or increase the pulse width. A depiction of the ternary tree for predictions during the left half of the switching period is shown in Figure 3.14b. During the first half of the switching period the controller is evaluated for an increasing pulse width by advancing until a switching transition is made. As such, the pulse width during the first horizon cannot be reduced and the initial branch of the ternary tree is reduced to only two branches.

During the second half of the switching period, the controller is evaluated for a decreasing pulse width. The pulse width during the first horizon therefore cannot be increased and the initial branch is also reduced to only two branches, as shown in Figure 3.15b.

In both cases, the first horizon only has two branches and each subsequent branch has three sub-branches. This brings the number of predictions $p$ during each evaluation step, for a horizon $h$, to

$$\begin{aligned} p &= 3^h - 3^{h-1} \\ &= \frac{2}{3} \times 3^h. \end{aligned} \tag{3.34}$$

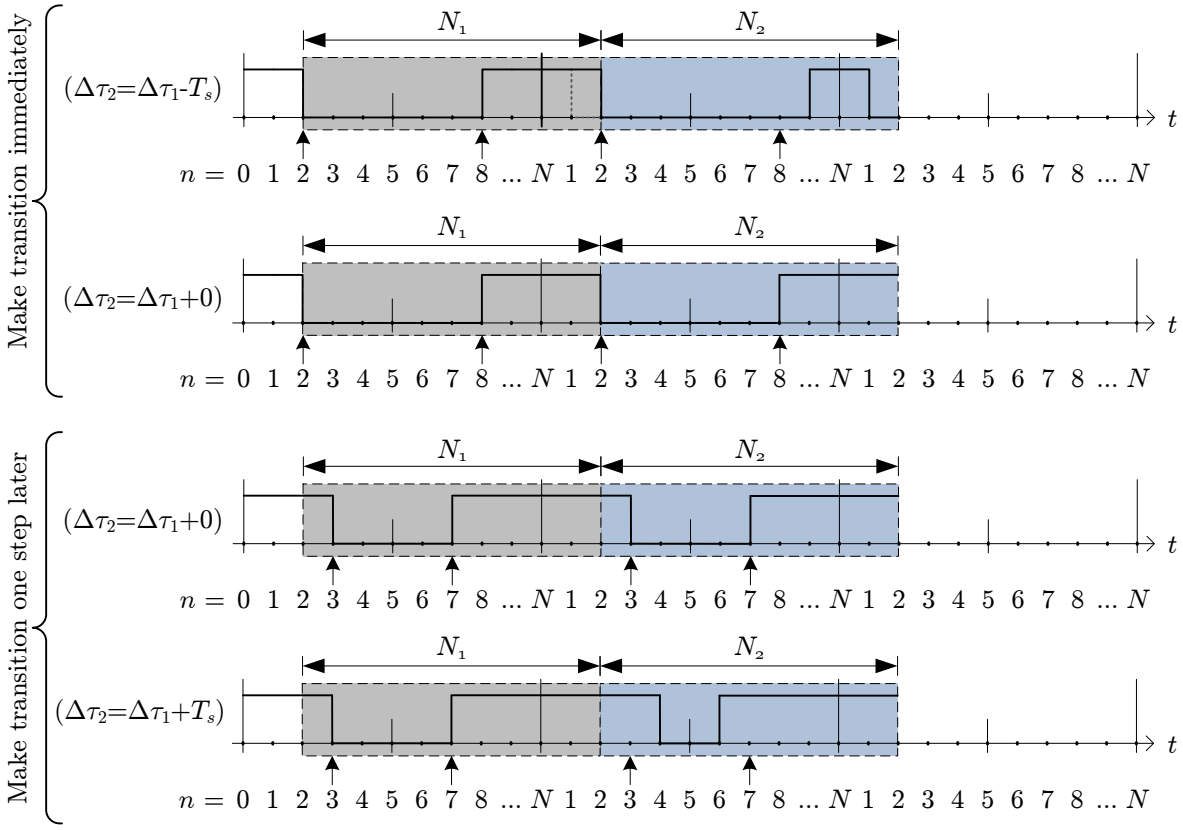
From the equation it is evident that a horizon of 3 will result in 18 prediction steps, which is a significant reduction from the initial 27 choices.

Since one of the goals of the control algorithm is to reduce the number of predictions, a *second assumption* can be made. It can be assumed that up to the predicted horizon, the pulse width will either *(a)* have an increasing trend or *(b)* have a decreasing trend. For an increasing trend, the pulse width will either remain unchanged or be increasing. And likewise, for a decreasing trend the pulse width will either remain unchanged or be decreasing. If the assumption is applied to the ternary tree, the tree is reduced to a binary tree. In Figures 3.14b and 3.15b, the reduced binary tree is indicated by the bold lines and blocks. The number of predictions is therefore further reduced to

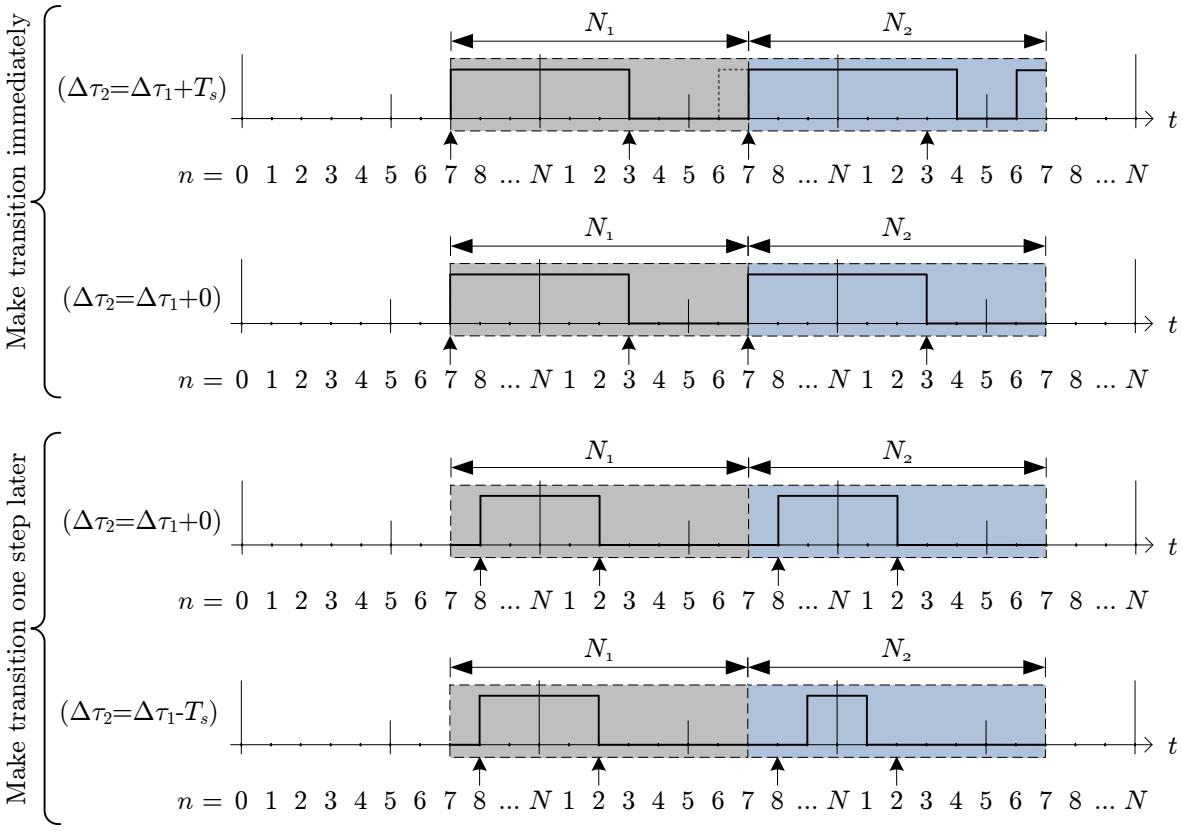
$$p = 2^h \tag{3.35}$$

such that a horizon of 3 only has 8 prediction choices and a horizon of 2 only has 4 choices. To illustrate the predictions in terms of the discrete samples, the predicted pulse trains for a horizon of 2 is depicted in Figure 3.16. The figure shows the prediction choices for an increasing pulse width at the top and a decreasing pulse width at the bottom. The pulse train for each prediction step is pre-calculated off-line and stored in a lookup table. This is done $N$-times for each step $n$ in the switching period.

This does not provide an optimal solution for the future switching periods but it does indicate the trend of an increasing or decreasing pulse width which is sufficient for reducing overshoot and ringing during large reference steps – as will be shown in later chapters. It is important to note that although the pulse width of future switching periods are




(a) Predictions during segment 1, on the left half of the switching period




(b) Predictions during segment 2, on the right half of the switching period

Figure 3.16: Depiction of the prediction choices and corresponding pulse trains for a horizon of 2

predicted only the first point of transition is applied, which is consistent with a receding horizon policy.

The consequence of this assumption is that for a sinusoidal time-varying reference the non-optimal solution may introduce a steady state tracking error that is directly proportional to the horizon length – the longer the horizon, the larger the tracking error may become. The error is introduced by the fact that the pulse width is linearly incremented for subsequent switching periods. If the switching frequency is much higher than the reference, the error is negligible. However, if the switching frequency and the reference frequency becomes closer, the error may become significant.

If the dynamics of a plant, such as the output voltage of an $LC$ filter, are much slower than the switching frequency, the controller will not be able to predict and react optimally when transient effects occur. This typically results in overshoot and ringing when a large reference step is applied. By increasing the prediction horizon the controller's ability to observe and react to the slower plant dynamics is improved, which also improves the transient response. This presents a trade-off, because an increased prediction horizon improves the transient response of the controller but it deteriorates the steady state tracking performance. This phenomenon is contrary to conventional FCS-MPC where very long prediction horizons improve the steady state tracking performance.

One solution is to define an error band with two modes of operation. The first mode of operation can be defined for steady state tracking, when the controlled variable is within the error band. The second mode of operation can be defined when the controlled variable is in a transient state or outside the error band. The controlled variable will typically find itself outside the error band during large reference steps or due to large disturbances.

By defining the two modes of operation a more optimal reaction can be obtained from the controller. For example, during steady state the horizon can be chosen as one but during transients, the horizon can be extended to improve the transient behaviour by quickly bringing the controlled variable back within the error band. This eliminates the tracking error introduced with higher prediction horizons when the system is in steady state. A similar approach was used in [75] to obtain a better transient response with model predictive pulse pattern control by distinguishing between the two modes for steady-state and transient operation.

## 3.3 Modelling and implementing the controller

### 3.3.1 Overview

This section presents the realisation and practical implementation of the proposed control method. In Section 3.2 an FCS-MPC control method is derived for achieving a fixed switching frequency. This is accomplished by sampling at a much higher rate than the desired switching frequency but still predicting for an entire switching period.

The switching period is divided into constrained prediction regions that are derived from the behaviour of PWM. Each prediction region is defined in such a way that only one switching transition may occur. The purpose of this is to reduce the number of prediction choices to only two states. This is done to reduce the number of on-line calculations, which allows the controller to be sampled at a much higher rate.

The principle of operation is to advance in steps of the sampling period while predicting the average value of the controlled variable for multiples of the switching period, based on the current region. The predictions are used to determine the optimal time to apply the switching transition for the given region. The method consists of two parts; the off-line calculation and storage of the lookup table and the on-line execution of the controller.

With conventional FCS-MPC methods [4; 19; 24; 26; 43; 44; 38; 51; 69; 70; 21] the equations for describing the predictions of the controlled variables are derived specifically for the given topology and set-up. In the following sections, a more generic approach is presented by using established state space theory [61] to develop a general method for modelling and implementing an arbitrary topology without the need to derive specific prediction equations – while attempting to remain computationally efficient.

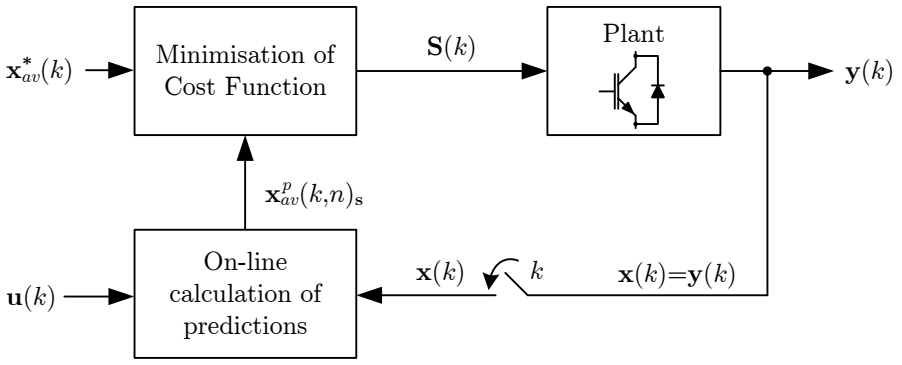
In Section 3.3.2, the control block diagram is discussed together with the modelling of the plant. The modelling of an unknown load is discussed in Section 3.3.3 and in the subsequent Section 3.3.5, a brief discussion about the cost function is presented.

The purpose of the control block diagram is to describe the principle of operation of the on-line controller in a simplified and visual manner. However, the practical realisation of that description may not be as trivial. In Section 3.3.6, the practical implementation of the off-line calculation of the lookup table and the storage data structure is presented. Lastly, the realisation of the on-line controller on an FPGA is presented.

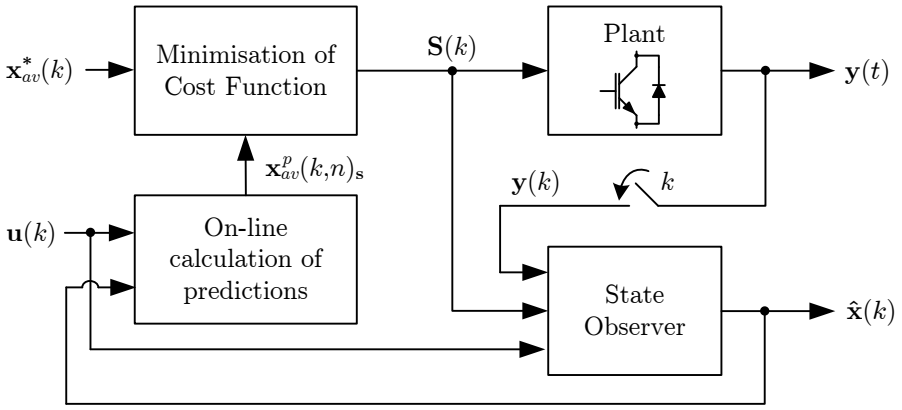
### 3.3.2 Control block diagram and plant modelling.

#### Block diagram

Conventional FCS-MPC methods [4] evaluate the system at every sampling instance and predict the behaviour at the next sampling instances. With some controllers a scheme may be in place to reduce the number of switching possibilities based on a voltage vector or some other system parameter. Likewise, the proposed method for a fixed switching




(a) All state variables measurable




(b) State variables estimated

Figure 3.17: Control block diagrams

frequency also evaluates the system at every sampling instance and predicts the average behaviour over the subsequent switching periods. The number of prediction choices are also constrained by using the characteristics of PWM to define prediction regions. Given the similarities it is expected that the block diagram of the proposed control method and that of conventional FCS-MPC will be the same, and it is.

The block diagram of the proposed FCS-MPC method is shown in Figure 3.17 and it is exactly the same as that of conventional FCS-MPC. The block diagram is divided into two scenarios; In Figure 3.17a the block diagram is shown when all the state variables are measurable and in Figure 3.17b the block diagram is adapted to accommodate a state observer.

When all the state variables are measurable, the measurements $\mathbf{x}(t)$ are sampled and directly used for the on-line calculation of the predictions. The online-calculation keeps track of the predefined prediction regions and the position within the switching period. Based on the region and the position index $n$, the average value is predicted by loading and multiplying the measurements with the appropriate matrices from the lookup table. The calculation is repeated for every permitted switching state in the specified region.

After the predictions are calculated the resulting averaged state vector $\mathbf{x}^p_{av}(k,n)_\mathbf{s}$ for each switching vector is passed to the cost function. The cost function uses the predicted average state vector together with an estimated average of the reference $\mathbf{x}^*_{av}(k)$. The

choice that minimizes the cost function is selected and the corresponding switching state or state vector $\mathbf{S}(k)$ is applied directly to the plant.

In a real-world setting it is seldom that all the state variables are directly measured. In such cases the unmeasured state variables can estimated. In some cases the relationship between the unmeasured and the measured variables may be trivial and in other cases it may not be. In order to present a general solution the concept of a state observer or estimator is used. In Figure 3.17b the plant output $\mathbf{y}(t)$ is sampled and fed to a state observer.

The state observer can be seen as a closed-loop model of the real plant that is fed with exactly the same inputs. In order to account for model inaccuracies and disturbances, the output of the real plant is fed back to the observer. From the block diagram it is shown that the observer is fed with the measured output $\mathbf{y}(k)$, the measured plant input $\mathbf{u}(k)$, and the switching vector $\mathbf{S}(k)$. The observer output is the estimated full state vector $\hat{\mathbf{x}}(k)$, which is used to perform the on-line calculations.

### Plant modelling

FCS-MPC does not use one linearised model but considers a model for each switching state and is modelled by the non-homogeneous state equation

$$\begin{aligned}\dot{\mathbf{x}}(t) &= \mathbf{A_s}\mathbf{x}(t) + \mathbf{B_s}u(t)\\ \mathbf{y}(t) &= \mathbf{C_s}\mathbf{x}(t) + \mathbf{D_s}u(t)\end{aligned} \tag{3.36}$$

where the subscript $\mathbf{S}$ indicates the model for the switching vector. By using the established state space representation a more generic approach can be presented for modelling and implementing an arbitrary topology without the need to derive specific prediction equations.

In order to predict the future behaviour, a solution for the state equation at some future time $t_1$ is required. The solution of (3.36) at $t_1$ is given by [61]

$$\mathbf{x}(t_1) = e^{\mathbf{A}(t_1-t_0)}\mathbf{x}(t_0) + \int_{t_0}^{t_1} e^{\mathbf{A}(t_1-\tau)}\mathbf{B}\mathbf{u}(\tau)\,\mathrm{d}\tau. \tag{3.37}$$

In many of the conventional FCS-MPC methods a simple $1^{\text{st}}$ order Euler-Forward or Euler-Backward approximation [4] is sufficient to predict the state variables at an arbitrary time $t_1$. Alternatively, for a more accurate approximation, the $4^{\text{th}}$ order Runge-Kutta method [4] can be used. However, in this text the state equation is discretized specifically for the sampling period $T_s$ such that

$$\begin{aligned}\mathbf{x}(k+1) &= \mathbf{F_s}\mathbf{x}(k) + \mathbf{G_s}u(k)\\ \mathbf{y}(k+1) &= \mathbf{C_s}\mathbf{x}(k+1) + \mathbf{D_s}u(k+1).\end{aligned} \tag{3.38}$$

The discretization could be done in any number of ways such as approximating (3.37) with the 4$^{\text{th}}$ order Runge-Kutta method or by using a zero-order hold, first-order hold or Bilinear transformation [61]. For a practical implementation, a zero-order hold transformation using the `c2d` function in Matlab is a fast and sufficient solution.

### 3.3.3 Modelling an unknown load current

In most power inverter applications the load is an unknown parameter that may vary unpredictably. As such the load is often modelled as an unknown current source and in order to obtain the current it must either be measured or estimated.

With the conventional FCS-MPC methods, an assumption is made about the dynamic behaviour of the unknown load current. The load current is usually a 50 Hz or 60 Hz sinusoidal waveform and the sampling frequency is usually in the order of kilohertz. As such, it can be assumed that the dynamic behaviour of the current over one sampling period is

$$\frac{\mathrm{d}i_{load}}{\mathrm{d}t} \approx 0. \tag{3.39}$$

However, the control method presented in Section 3.2 predicts multiple switching periods ahead and not only a few sampling periods. If it is assumed that (3.39) is true, an error is introduced in the predictions. This manifests as a tracking error that varies as the load varies.

One solution to overcome this problem is to use the Euler-backward method to approximate the dynamic behaviour as

$$\frac{\mathrm{d}i_{load}}{\mathrm{d}t} \approx \frac{i_{load}(k) - i_{load}(k-1)}{T_s}. \tag{3.40}$$

If the state vector $\mathbf{x}(k)$ is the $n \times 1$ matrix,

$$\mathbf{x}(k) = \begin{bmatrix} x_1(k) & x_2(k) & x_3(k) & \dots & x_n(k) \end{bmatrix}^\top \tag{3.41}$$

then let $x_n(k)$ be the unknown load current $i_{load}(k)$.

In order to add the dynamics of (3.40) to the state space model, increase the state vector by appending a new state variable $x_{n+1}$ so that the new state vector becomes

$$\mathbf{x}(k) = \begin{bmatrix} x_1(k) & x_2(k) & x_3(k) & \dots & x_n(k) & x_{n+1}(k) \end{bmatrix}^\top. \tag{3.42}$$

With $x_n(k)$ as the unknown load current, define that

$$x_{n+1}(k) = x_n(k-1) \tag{3.43}$$

and that

$$\frac{\mathrm{d}x_{n+1}}{\mathrm{d}t} \approx \frac{\mathrm{d}x_n}{\mathrm{d}t}. \tag{3.44}$$

The dynamic behaviour in (3.40) can then be rewritten by substituting $x_n(k-1)$ with Equation (3.43) so that

$$\frac{\mathrm{d}x_n}{\mathrm{d}t} \approx \frac{x_n - x_{n+1}}{T_s} \tag{3.45}$$

which presents a more accurate assumption of the dynamic behaviour of the unknown load current over longer prediction horizons.

### Discrete-time state space model

The two equations (3.45) and (3.44) can be used in the differential equations that describe the system to solve the state space matrices in continuous time or discrete time. If the discrete-time state space matrices have already been found for the sampling period $T_s$, the dynamic behaviour of the unknown load current can be amended without having to re-solve the state matrices.

The Euler forward method is given by

$$\frac{\Delta x_n}{\Delta t} \approx \frac{x_n(k+1) - x_n(k)}{T_s}. \tag{3.46}$$

Rewriting (3.46) for $x_n(k+1)$, the equation becomes

$$x_n(k+1) = \frac{\Delta x_n}{\Delta t} T_s + x_n(k). \tag{3.47}$$

If $\Delta t = T_s$, then (3.47) becomes

$$x_n(k+1) = x_n(k) + \Delta x_n. \tag{3.48}$$

The term $\Delta x_n$ can be found by using the Euler-backwards approximation

$$\frac{\Delta x_n}{\Delta t} \approx \frac{x_n(k) - x_n(k-1)}{T_s} \tag{3.49}$$

and solving for $\Delta x_n$ with the assumption that $\Delta t = T_s$ also holds true,

$$\Delta x \approx x_n(k) - x_n(k-1). \tag{3.50}$$

By substituting (3.50) and (3.43) into (3.48), the equation becomes

$$\begin{aligned} x_n(k+1) &= x_n(k) + \Delta x_n \\ &= x_n(k) + \big(x_n(k) - x_n(k-1)\big) \\ &= 2x_n(k) - x_n(k-1) \\ &= 2x_n(k) - x_{n+1}(k). \end{aligned} \tag{3.51}$$

Using (3.51) and (3.43), the discrete state space equation can be directly amended by including the new dynamic behaviour of the unknown load current,

$$\mathbf{x}(k+1) = \left[\begin{array}{ccccc:c} a_{11} & a_{12} & a_{13} & \dots & a_{1n} & 0 \\ a_{21} & a_{22} & a_{23} & \dots & a_{2n} & 0 \\ a_{31} & a_{32} & a_{33} & \dots & a_{3n} & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & \dots & 2 & -1 \\ \hdashline 0 & 0 & 0 & \dots & 1 & 0 \end{array}\right] \cdot \left[\begin{array}{c} x_1(k) \\ x_2(k) \\ x_3(k) \\ \vdots \\ x_n(k) \\ \hdashline x_{n+1}(k) \end{array}\right] + \left[\begin{array}{c} b_1 \\ b_2 \\ b_3 \\ \vdots \\ b_n \\ \hdashline 0 \end{array}\right] \mathbf{u}(k). \tag{3.52}$$

Note that unlike the conventional FCS-MPC methods, this equation is not used to calculate the absolute value at the predicted horizon it is used for the averaged off-line calculations to recursively step up to prediction horizon in steps of the sampling period.

If a state observer is used, this model can also be used for estimating the unknown load current. However, since the state observer only updates for one sampling period, the assumption about the dynamic behaviour in (3.39) should be adequate.

### 3.3.4 Control reference

The control reference is an input that is given to the controller with the expectation that the corresponding output will converge to that value in a finite amount of time. The amount of time and the path that the controller takes to bring the output to the reference depends on the controller's closed loop characteristics and design. Model predictive control is built on the principle of predicting the expected future behaviour, based on a model of the system to find the optimal way of bringing the output to the reference point. In order for the future predictions to be of any service the future reference value should also be known. This presents two scenarios: (a) the reference generating function is known to the controller or (b) the reference generating function is unknown to the controller.

#### Known reference function

When the reference generating function is known, the future reference can easily be obtained by simply adding a time off-set or phase shift. For example, consider the sinusoidal reference function

$$x^*(t) = A\sin(\omega t) \tag{3.53}$$

where $t$ can be replaced with $kT_s$ for discrete time. To obtain the future reference at some time $t_2$, the result can be obtained by simply applying $t_2$ to the known function. In most cases the prediction horizon remains fixed and the future reference can be found by simply adding a fixed phase shift $\Phi$ to the reference function such as

$$x^*(t) = A\sin(\omega t + \Phi). \tag{3.54}$$

The on-line predictions calculate the average value over the prediction horizon, so the reference should also be for the average value. For a sinusoidal reference function, it can be assumed that the average reference value of the time period between $t_1$ and $t_2$ is

$$t_{av} = \frac{t_1 + t_2}{2} \tag{3.55}$$

which is halfway between $t_1$ and $t_2$. If $t_1 = kT_s$ and $t_2 = (k + Nh)T_s$, where $h$ is the fixed horizon length and $N$ is the number of samples $T_s$ in each switching period $T_{sw}$, the discrete time $t_{av}$ can be written as

$$\begin{aligned} t_{av} &= \frac{kT_s + (k + Nh)T_s}{2} \\ &= kT_s + \frac{Nh}{2}T_s. \end{aligned} \tag{3.56}$$

By substituting (3.56) into (3.53), the discrete-time reference becomes

$$\begin{aligned} x^*(k) &= A\sin\left(\omega(kT_s + \frac{Nh}{2}T_s)\right) \\ &= A\sin\left(\omega(kT_s) + \omega\frac{Nh}{2}T_s\right) \\ &= A\sin\left(\omega(kT_s) + \Phi\right) \end{aligned} \tag{3.57}$$

which leads to the fixed phase shift

$$\Phi = \omega\frac{Nh}{2}T_s. \tag{3.58}$$

### Unknown reference function

When the reference function is not known to the controller certain assumptions have to be made in order to estimate the future reference value. The easiest and most simple solution is to assume that the reference remains constant over the predicted horizon. If the prediction horizon is only a few sampling steps this assumption is often sufficient with a negligible tracking error. However, if multiple switching periods are predicted, as is the case with the controller in this chapter, then a significant tracking error is introduced which is proportional to the horizon length.

An alternative solution is to use the past knowledge of the reference to anticipated the future value. This can be done by using the same technique that is used to extrapolate the unknown load current in the previous section. Although second and third degree functions may also be used, the first order extrapolation is considered to be sufficient for mitigating the tracking error. The Euler backward method

$$\frac{\Delta\mathbf{x}^*}{\Delta t} \approx \frac{\mathbf{x}^*(k) - \mathbf{x}^*(k-1)}{T_s} \tag{3.59}$$

can be used to obtain the change in the reference $\Delta\mathbf{x}^*$ by assuming that $\Delta t = T_s$, which leads to

$$\Delta\mathbf{x}^* = \mathbf{x}^*(k) - \mathbf{x}^*(k-1). \tag{3.60}$$

The first order Euler forward method

$$\frac{\Delta \mathbf{x}^*}{\Delta t} \approx \frac{\mathbf{x}^*(k+n) - \mathbf{x}^*(k)}{nT_s}. \tag{3.61}$$

can be used to obtain the change in the reference for $nT_s$ samples in the future by assuming that $\Delta t = T_s$ and substituting (3.60) into (3.61) so that

$$\begin{aligned} \mathbf{x}^*(k+n) &= \mathbf{x}^*(k) + n \cdot \Delta \mathbf{x}^* \\ &= \mathbf{x}^*(k) + n\big(\mathbf{x}^*(k) - \mathbf{x}^*(k-1)\big) \\ &= (n+1)\mathbf{x}^*(k) - n\mathbf{x}^*(k-1). \end{aligned} \tag{3.62}$$

This allows the reference to be extrapolated for any number of samples $n$ into the future. In order to extrapolate to $t_{av}$, the discrete time $(k+n)$ can be found by dividing (3.56) by $T_s$ and solving for $n$, which results in

$$n = \frac{Nh}{2}. \tag{3.63}$$

### 3.3.5 Cost function

One of the fundamental concepts that define FCS-MPC is the use of a cost function to describe the control objective. The cost function is evaluated for each valid prediction choice and the actuation sequence that minimises the cost function is applied. In the previous sections, a method of defining hard constraints is presented which forces the system to follow a fixed switching frequency. This is accomplished by limiting certain actuation choices for predefined periods of time. These hard constraints are implemented separately from the cost function and cannot be impacted by the cost function design.

In [4], several cost function terms are discussed which relate to different control requirements for the system. Amongst these are terms for reference tracking, hard constraints for keeping variables within certain bounds, actuation constraints for minimization of the switching frequency, the reduction of switching losses as well as the shaping of spectral content.

All of these cost function terms can be implemented with the FCS-MPC method presented in this text. It should be noted that the hard constraints which enforce the fixed switching frequency are implemented separately from the cost function. As a result, the cost function terms that are used for reducing the switching frequency or the switching losses will be fruitless and may even degrade the overall tracking performance of the controller. The method for doing spectral shaping can be implemented, but it will be ineffective if the intention is to shape the switching frequency. Hard constraints can be applied in the exact same manner as with conventional FCS-MPC to keep a variable within certain bounds.

In this dissertation, the two most common cost function terms that can be used with the fixed switching frequency method is discussed. These are reference tracking and the enforcement of hard constraints.

### Reference tracking

Reference tracking generally consists of the minimization of the error between the actual state variable and the desired reference [4; 61]. For the fixed switching frequency method, the error can be expressed in the same manner as conventional FCS-MPC where the *norm* $||\cdot||$ of the averaged predicted state variable and the averaged future reference is taken as

$$g = ||x^* - x^p|| \tag{3.64}$$

and the tracking of multiple state variables as weighted terms

$$g = w_1||x_1^* - x_1^p|| + w_2||x_2^* - x_2^p|| + w_3||x_3^* - x_3^p|| + \dots \tag{3.65}$$

where $w_1, w_2, w_3, \dots$ are the respective weights for each term. When a term's magnitude relative to the other is smaller, its impact on the cost function is reduced which leads to a lower control priority for that state variable. To balance the importance of the controlled variables the weights of the terms can be adjusted to compensate for the difference in reference magnitudes. Alternatively, if the importance of a specific state variable is required to be higher than the others, the weight of that specific term can be increased accordingly.

The *norm* $||\cdot||$ can be implemented as either a sum of absolute values

$$g = w_1|x_1^* - x_1^p| + w_2|x_2^* - x_2^p| + w_3|x_3^* - x_3^p| + \dots, \tag{3.66}$$

or as the sum of square values

$$g = w_1(x_1^* - x_1^p)^2 + w_2(x_2^* - x_2^p)^2 + w_3(x_3^* - x_3^p)^2 + \dots \tag{3.67}$$

In [4], a third implementation of the *norm* is presented which calculates the integral values over the sampling period:

$$g = \left| \int_k^{k+1} \big(x^*(\tau) - x^p(\tau)\big) \mathrm{d}\tau \right| \tag{3.68}$$

which leads to the mean value being evaluated and not just the final value. However, the predictions used with the fixed switching frequency method already predicts the average value over the prediction horizon and for that reason the calculation of the integral value is not considered.

This leaves the choice between using absolute valued terms or squared value terms. When the cost function has only one reference tracking term, both the absolute value and squared value term will produce the exact same results. When more than one reference tracking term is used, squared valued terms will provide better overall reference tracking.

The reason for this behaviour is that when the magnitude of an error is $0 < |err| < 1$, the magnitude will become quadratically smaller with respect to the other terms when

the square is taken. Likewise, when the magnitude of the error is $|err| > 1$, the error will become quadratically bigger than the other terms when the square is taken. This leads to small errors being suppressed and larger errors being highlighted – which leads to better overall tracking.

#### Hard constraints

Traditional cascaded control schemes often include reference saturation to prevent variables from exceeding certain limits [61]. For example, when the voltage of an $LC$ output filter is controlled, a limit may be placed on the peak inductor current during large voltage step changes. This can be done by limiting the peak reference value of the inner current loop. Alternatively, a limit may be required for the peak capacitor voltage of a flying capacitor converter during transient effects.

With FCS-MPC there are no cascaded control loop structures and all the controlled variables are added as terms in the cost function. Limits can therefore be applied by modifying the cost function and adding an appropriate term. The objective of the cost function is to obtain the sequence of actuations that will minimize the cost function. If a state variable $x$ reaches a limit, the cost function must be modified to prevent those actuation choices which will lead to $x$ exceeding the predefined limit $x_{max}$. This can be achieved by adding a non-linear term $f_{lim}(x^p)$ to the cost function [4] which is defined as

$$f_{lim}(x^p) = \begin{cases} 0 & \text{if} \quad |x^p| \leq x_{max} \\ \infty & \text{if} \quad |x^p| > x_{max} \end{cases} \tag{3.69}$$

The purpose and application of the cost function with the fixed switching frequency method therefore remains the same as that of conventional FCS-MPC. The only difference is that the switching frequency is limited separately from the cost function and the predictions are made by reading coefficients from a pre-calculated lookup table.

### 3.3.6 The calculation and storage of the off-line predictions

For a simple FCS-MPC control scheme, the predictions can be calculated on-line using an Euler-Forward or a 4th order Runge-Kutta approximation [19]. However, the prediction algorithm that has been presented in Chapter 3.2 is too complex to calculate on-line in a reasonable time. The fact that the model of the system is defined for a finite number of switching states and that the prediction algorithm is defined for a finite number of step sizes the total number of predictions for each switching state and step index $n$ can be calculated off-line and stored in a lookup table.

In Chapter 3.2.2.2, the off-line equations are derived and the four equations: (3.25), (3.26), (3.27) and (3.28) are obtained. These equations represent the four possible calculations that can be made for each pseudo carrier when two carriers are used. Although an analytical solution for the off-line predictions can be found, a more scalable numerical

approach is followed by using the Matlab symbolic toolbox or the open source Python SymPy symbolic toolbox. Both software packages are sufficient but the SymPy symbolic toolbox is used for the experimental evaluations in the subsequent chapters.

A symbolic expression of the off-line prediction equations can be numerically obtained by using (3.38) and starting with a symbolic state vector as the initial state $\mathbf{x}(k)$ and a symbolic vector $\mathbf{u}(k)$ as the input. Note that $\mathbf{u}(k)$ is not the control input but the driving source of the plant.

The symbolic solution of (3.25), (3.26), (3.27) and (3.28) remains a linear expression and can be simplified and transformed back into the state space representation:

$$\mathbf{x}_{av}^{p}(k,n)_{\mathbf{s}} = \mathbf{\Lambda}(n)_{\mathbf{s}}\mathbf{x}(k) + \mathbf{\Gamma}(n)_{\mathbf{s}}\mathbf{u}(k). \tag{3.70}$$

An equation of the predicted average state vector $\mathbf{x}_{av}^{p}(k,n)_{\mathbf{s}}$ is found for each switching vector $\mathbf{S}$. In this solution the equations are not only a function of the current sampling instance but also of the current step index $n$. An equation is therefore found for each switching vector $\mathbf{S}$ and each step index $n = \{0, 1, 2, \ldots, N-1\}$. The $\Lambda(n)_{\mathbf{s}}$ matrix can be obtained by finding the Jacobian matrix of $\mathbf{x}_{av}^{p}(k,n)_{\mathbf{s}}$ with respect to the symbolic vector $\mathbf{x}(k)$ for the given $n$. Likewise, $\Gamma(n)_{\mathbf{s}}$ is obtained by taking the Jacobian with respect the symbolic input vector $\mathbf{u}(k)$. The results of the off-line calculations are therefore the $\Lambda$ and $\Gamma$ matrices. The matrices can be stored in a lookup table and recalled when doing on-line predictions.

Each of the off-line matrices corresponds to a specific switching state that is to be applied at the present sampling instance $k$. These switching states can also be stored in a lookup table to correspond to the prediction matrices.

### Memory structure for off-line storage

In order to recall the calculated prediction matrices a practical memory structure is needed. Consider the memory structure presented in Figure 3.18. Each entry in the prediction matrices represent a coefficient that is multiplied with a variable or vector. These coefficients can be numbered from entry $\#0$ to $\#L-1$, where $L$ is the total number of entries in both matrices as shown in the figure. For $N$ sample steps in the switching period, each set of coefficients are stored in sequence, from $n = 0$ to $n = N-1$, and repeated for each set of prediction equations. The first memory blocks are used to store all the coefficients for the *high*-state predictions of segment 1. The subsequent memory blocks are used to store the *low*-state predictions of segment 1. This process is repeated for all the segments until all the coefficients have been stored.

The prediction coefficients can easily be recalled by setting the address to the start of the memory block containing the required prediction type and applying an offset with respect to the prediction step $n$.

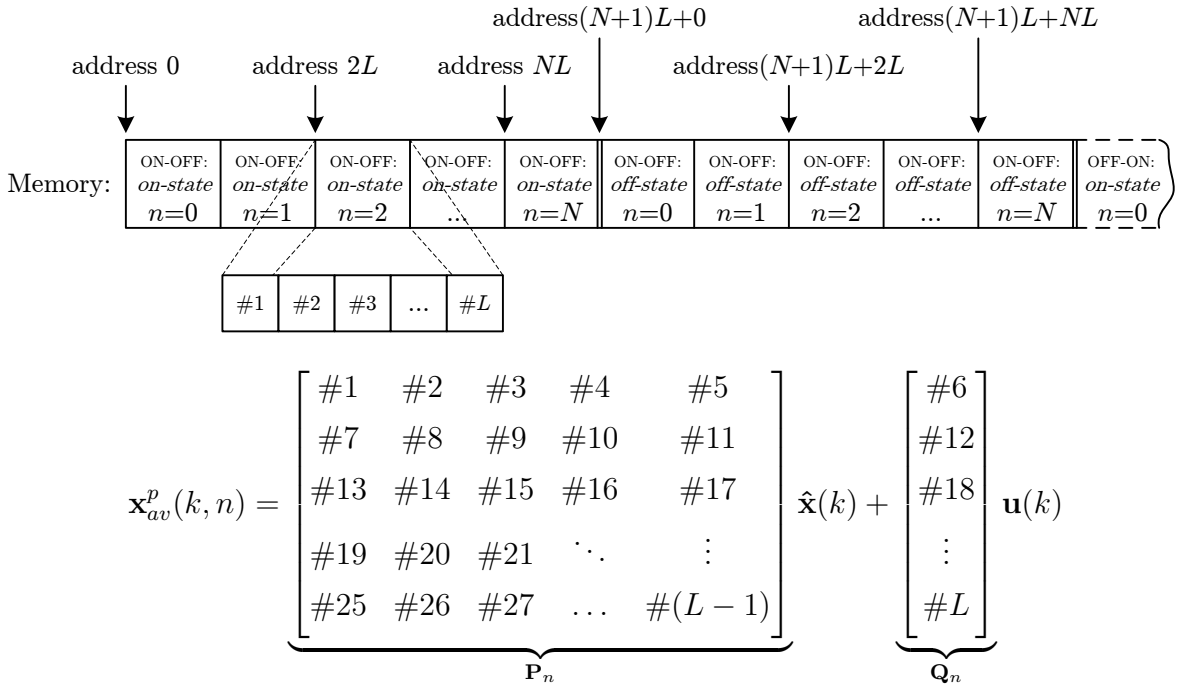



Figure 3.18: Memory structure for storing the prediction matrices .

### 3.3.7 Realising the on-line controller

The fixed switching frequency method is divided into two parts; the calculation and storage of the off-line prediction matrices and the on-line controller. In this section the on-line controller is discussed.

The on-line controller represents the continuous sequence of operations that are executed in real time. The top-level functional description of the on-line controller is represented by the control block diagram shown Figure 3.17. The block diagram gives the top-level overview of the feedback loop without describing what happens within each block. In this section the detailed realisation of the control block diagram is presented for the implementation on an FPGA.

The on-line calculation of predictions work on the principle of sampling at a much higher rate than the switching frequency by dividing the switching period into $N$ sampling steps. Each switching period is further divided into time segments with one or more prediction regions assigned to each time segment. For each region a set of prediction matrices are pre-calculated off-line and stored in a lookup table as a function of (a) the sampling instance, (b) the time segment and (c) the region level. When the controller is evaluated on-line, the prediction matrices corresponding to these three parameters are loaded and used to make the predictions.

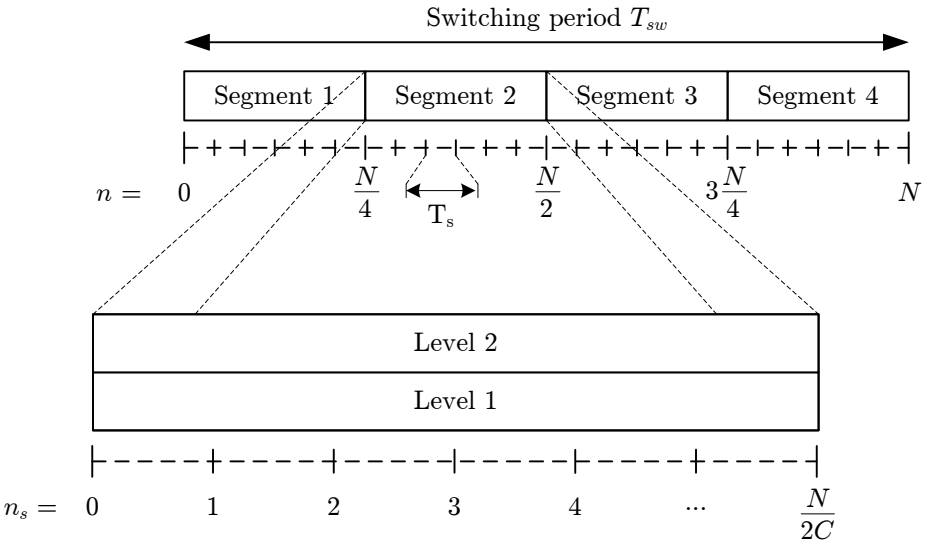



Figure 3.19: Depiction of the switching period divided into segments and levels when two triangular carriers are used.

### Region position counters

Consider the depiction in Figure 3.19 of a switching period divided into time segments when two triangular carriers are used. It is shown that the switching period is divided into four time segments and each segment has two prediction levels, which corresponds to the two prediction regions per time segment.

As the controller evaluates each switching period, it steps through every time segment in steps of the sampling period and makes a prediction based on the region at the given segment and level. The predictions are made by loading the appropriate prediction matrices for that region from the lookup table. This requires the controller to keep track of the three parameters: (a) the sampling steps in each segment, (b) the segments in each switching period and (c) the region levels.

With $C$ being the number of pseudo carriers and $N$ the number of sampling steps in the switching period, define the number of sampling steps in each time segment as

$$N_s = \frac{N}{2C}. \tag{3.71}$$

and define $n_s \in \{0, 1, 2, \ldots, (N_s - 1)\}$ as the counter for keeping track of the sampling position in each time segment. Then, define $seg \in \{1, 2, 3, \ldots, 2C\}$ as the counter for keeping track of the segments in each switching period and define $lev \in \{1, 2, 3, \ldots, C\}$ as the variable for keeping track of the current region level.

By defining these three counters the correct $\Lambda$ and $\Gamma$ matrices can be loaded from the lookup-table at each sampling instance. A flow diagram describing the practical implementation of the counter variables is shown in Figure 3.20.

The sampling step counter $n_s$ starts at zero and is incremented with each sampling instance. When $n_s = N_s$, it marks the start of the next time segment. At that point $n_s$

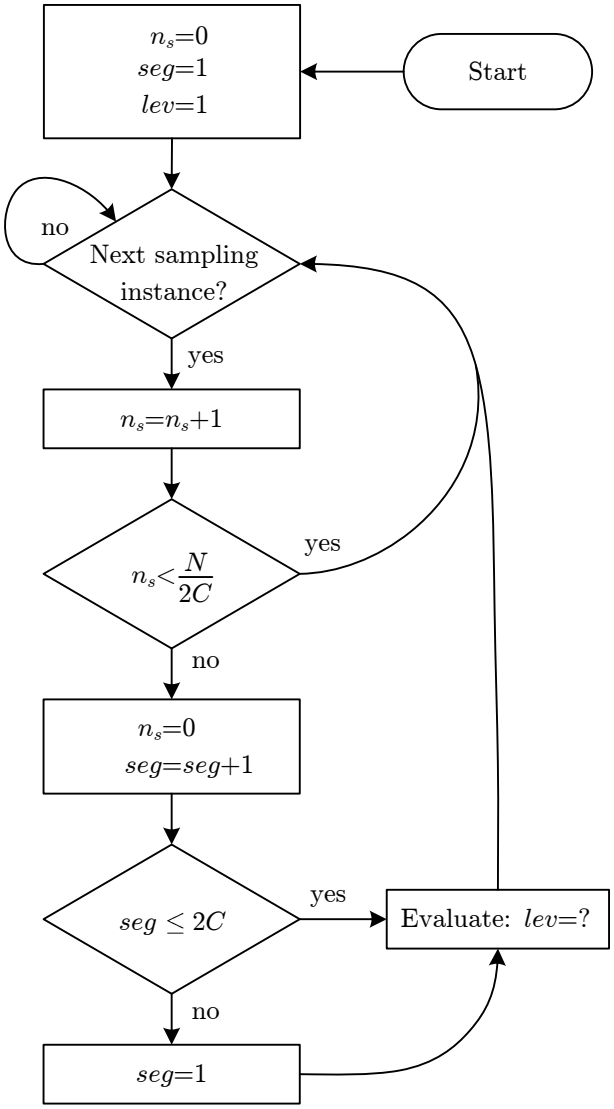



Figure 3.20: Flow diagram: Implementation of the counter variables for keeping track of the current sampling position, time segment and region level.

is zeroed and the segment counter $seg$ is incremented by one. At the start of every time segment the region level is evaluated, based on the criteria in Chapter 3.2.1.2, and the region level counter $lev$ is updated. This process is repeated until all the segments in the switching period are evaluated and the end of the switching period is reached. At that point the segment counter is reset and the sequence is restarted for the next switching period.

### FPGA implementation

The on-line controller can be realised as a finite-state machine on an FPGA by using the Mealy state model. The Mealy state model is based on the principle that the output of a state is determined by both the state of the circuit and its present input values [76]. This structure allows the controller to do operations in a sequence, where the next operation

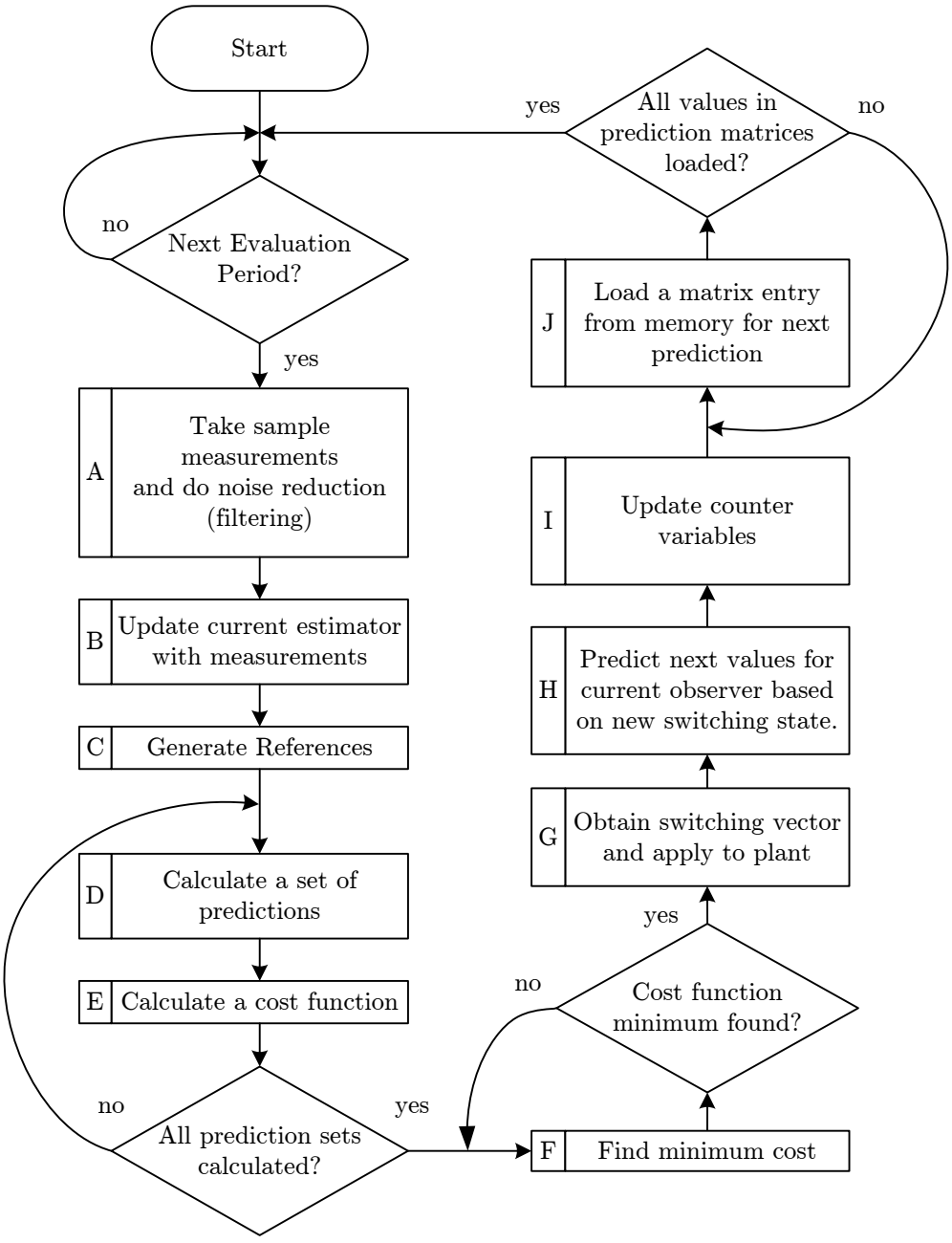



Figure 3.21: On-line controller flow diagram.

depends on the outcome of the previous calculation.

With digital controllers it is often important to minimize the computational delay between the sampling time of the measurements and the point at which the control command is communicated to the plant. If not anticipated, a large computational delay may introduce an unwanted tracking error and increase the noise floor [61]. For this reason, an FPGA is chosen for its ability to do many computations in parallel. For example, a matrix multiplication of an arbitrary size can be computed in one clock cycle by defining the appropriate logic circuit. This allows complex predictions to be calculated in only a few clock cycles.

A flow diagram describing the functional sequence of operations of the finite-state

machine is shown in Figure 3.21. The sequence of operations are ordered in such a way as to minimize the time between the sampling instance when the measurements are taken and the instance when the control command is updated. This is done by pre-calculating known operations for the next sampling instance at the end of the present sampling instance, after the control command is applied. The flow diagram are described be the following sequence of states and each state is executed in one FPGA clock cycle:

***State A:*** The first state is applied at the start of the sampling period. A sample measurement is taken and depending on the hardware it may be necessary to apply noise suppression filtering in software.

***State B:*** After the measurements are taken the current estimator is updated with the new value. If all the state variables are measured, this state is skipped.

***State C:*** Depending on the implementation, the control references may be dependent on or more state variables. If this is the case, the references should be generated after the current estimator is updated. If the references are dependent on a state variable that are directly measured, it should still be updated using the estimated state vector and not with the directly measured state variables. The estimator may introduce a small delay or phase shift to the estimated state vector and the state variables of the measured and estimated state vectors should therefore not be mixed.

***States D and E:*** To utilize the logic elements on the FPGA more efficiently, the same architecture for calculating one prediction can be used for calculating all the predictions recursively. This is accomplished by calculating one prediction in *State D* and it's corresponding cost function in *State E* and repeating this sequence until all the predictions are evaluated. This can be realised by setting up an array $R$ to hold the values of every matrix $\Lambda$ and $\Gamma$ that are preloaded from memory. It is not always necessary to predict the entire averaged state vector $\mathbf{x}_{av}^{p}(k,n)$, hence only the required rows from the $\Lambda$ and $\Gamma$ can to be loaded. The rows of $\Lambda$ and $\Gamma$ can be combined as one row in the array $R$. For example, if the prediction equation is

$$\mathbf{x}_{av}^{p}(k,n) = \begin{bmatrix} \#1 & \#2 & \#3 \\ \#5 & \#6 & \#7 \\ \#9 & \#10 & \#11 \end{bmatrix} \mathbf{x}(k) + \begin{bmatrix} \#4 \\ \#8 \\ \#12 \end{bmatrix} \mathbf{u}(k). \tag{3.72}$$

and only $x_1$ and $x_3$ is to be controlled, the array $R$ will contain

$$R = [\#1, \#2, \#3, \#4, \#9, \#10, \#11, \#12, \cdots] \tag{3.73}$$

The matrices for all the prediction choices are sequentially loaded into the array and the matrix multiplication is implemented as a multiply-and-add structure that will calculate

in one clock cycle by using the form

$$\begin{aligned} x^p_{av}(k,n)_1 &= R(0+h)x_1(k) + R(1+h)x_2(k) + \cdots + R(4+h)u(k) \\ x^p_{av}(k,n)_3 &= R(5+h)x_1(k) + R(6+h)x_2(k) + \cdots + R(8+h)u(k) \end{aligned} \tag{3.74}$$

where $h$ is the array offset for the other prediction choices. This allows the different predictions to be calculated recursively by simply incrementing the offset variable $h$.

***State F:*** After the cost functions are calculated, the results are recursively evaluated until the minimum is found. For a horizon of one the minimum is found at the first evaluation but for larger prediction horizons, the number of predictions increase and the evaluation are repeated several times.

***State G:*** Each prediction region corresponds to one of two switching vectors and are stored in a lookup table. For the minimum cost function and region, the correct switching vector can be loaded from the lookup table and directly applied to the plant.

***States H and I:*** After the new switching vector has been applied, the controller has time to do housekeeping before the next sampling instance. During this time the next values of the current observer is calculated and the counter variables of the controller is updated.

***State J:*** The predictions are done by multiplying the present state vector with the precalculated prediction matrices. This is done by loading the matrices from memory into the multiplier buffers, ready to be used when the new state vector is updated. To limit the number of logic elements, the matrices are not loaded as a whole, but the values in each matrix is loaded one-by-one from memory. Consequently, this process consumes the most time and acts as the limiting factor of the maximum sampling rate and prediction horizons that can be practically realised. After all the prediction matrices are loaded the controller waits for the next sampling instance to occur.

## 3.4 FCS-MPC with state estimation

### 3.4.1 State estimation

In this section the existing theory of observer design [61] is adapted to create a switched observer for a finite-control-set model predictive controller. In practical systems the complete state vector is not always directly available through measurements. In such cases, a full-state observer is required to estimate the state vector, based on the measured state variables. A current estimator is chosen for it's simplicity and ease of implementation, although a more sophisticated state estimator such as a Kalman filter can also be used.

The state observer is realised by placing an equivalent model in parallel with the actual system and driving it with the same inputs and control signals as the real plant. If the model and the real system start at the same known conditions, it is expected that the output vector of the model would follow the output of the real system. However, the observer model is only a representation of the real system and unmodelled dynamics and external influences remain uncertain. As a result the model would gradually diverge from the real system and the state vector would become unreliable.

To correct the divergence the output state vector of the real system is measured and compared to the output of the model. The error between the real and the modelled output vector is used to correct the tracking error - by adjusting the model according to a certain gain vector.

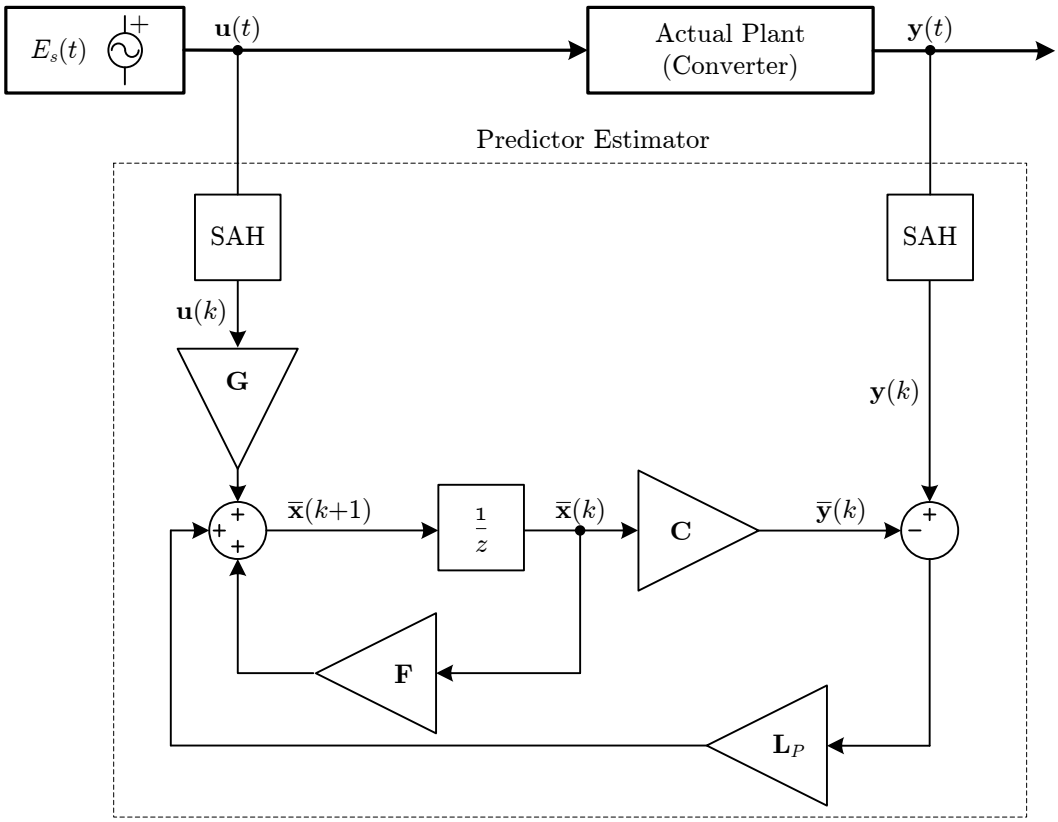
### 3.4.2 Predictor estimator

The predictor estimator uses measurements at the discrete time step $k$ to predict the estimated state vector at $k+1$. The equation describing the predictor estimator [61] is given by

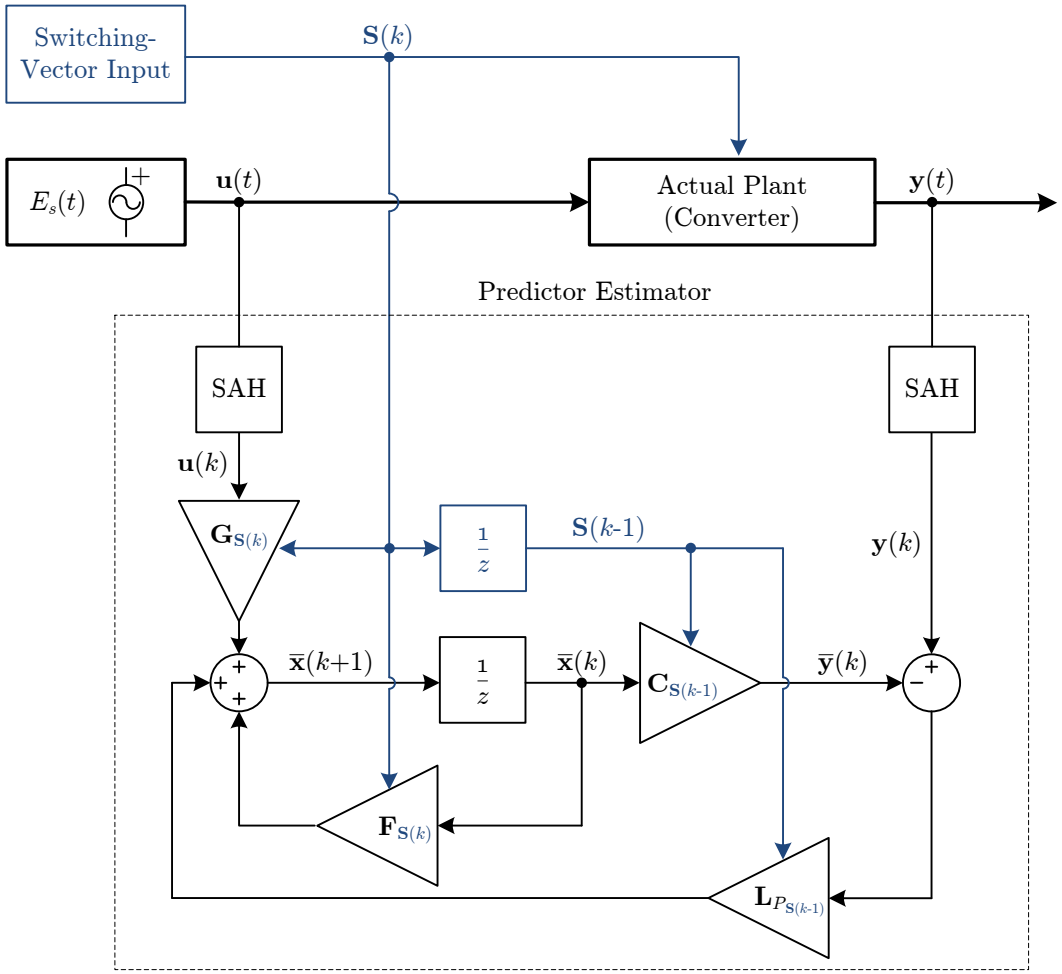
$$\bar{\mathbf{x}}(k+1) = \mathbf{F_S}\bar{\mathbf{x}}(k) + \mathbf{G_S}u(k) + \mathbf{L_{ps}}\left(\mathbf{y}(k) - \mathbf{C_S}\bar{\mathbf{x}}(k)\right) \tag{3.75}$$

where $\bar{\mathbf{x}}(k+1)$ represents the estimated state vector at $k+1$ and $\mathbf{L_{ps}}$ the estimator feedback gain. A block diagram depicting the predictor estimator is shown in Figure 3.22a. The estimator is designed for a single linear plant model that is driven by the plant input $\mathbf{u}(t)$. However, with model predictive control the plant is described by a finite set of linear models, each representing a physical switching state.

In (3.21), the physical switching state is indicated by the switching vector subscript, $\mathbf{S}$, and the same principle can be applied to the predictor estimator. The switching vector, $\mathbf{S}(k)$, is updated at time $k$ and represents the switching state that the system will be in from $k$ up to $k+1$. The predictor estimator corrects the tracking error by using measurements at time $k$. However, the tracking error occurred during sampling period between $k-1$ and $k$. As a result the tracking error should be corrected with the switching vector of $\mathbf{S}(k-1)$ and not $\mathbf{S}(k)$. The adapted equation for the predictor estimator then




(a) Predictor estimator




(b) Switched predictor estimator

Figure 3.22: Predictor estimator block diagrams

becomes

$$\bar{\mathbf{x}}(k+1) = \mathbf{F}_{\mathbf{S}(k)}\bar{\mathbf{x}}(k) + \mathbf{G}_{\mathbf{S}(k)}\mathbf{u}(k) + \mathbf{L}_{\mathbf{p}_{\mathbf{S}(k-1)}}\left(\mathbf{y}(k) - \mathbf{C}_{\mathbf{S}(k-1)}\bar{\mathbf{x}}(k)\right). \tag{3.76}$$

A block diagram of the adapted predictor estimator is shown in Figure 3.22b. If the state estimate error is defined as

$$\tilde{\mathbf{x}}(k) = \mathbf{x}(k) - \bar{\mathbf{x}}(k) \tag{3.77}$$

then the state estimate error dynamics can be described by

$$\tilde{\mathbf{x}}(k+1) = \left(\mathbf{F}_{\mathbf{S}(k)} - \mathbf{L}_{\mathbf{p}_{\mathbf{S}(k)}}\mathbf{C}_{\mathbf{S}(k)}\right)\tilde{\mathbf{x}}(k) \tag{3.78}$$

for the finite set of switching combinations in $\mathbf{S}(k)$. If the actual error dynamic poles are given by

$$\det\left(\mathbf{F}_{\mathbf{S}(k)} - \mathbf{L}_{\mathbf{p}_{\mathbf{S}(k)}}\mathbf{C}_{\mathbf{S}(k)}\right) = 0 \tag{3.79}$$

and the desired error dynamic poles are defined by the characteristic equation

$$\alpha(z)_{\mathbf{S}(k)} = z^n + \alpha_1 z^{n-1} + \cdots + \alpha_{n-1}z + \alpha_n = 0 \tag{3.80}$$

with $n$ being the order of the system for each valid switching vector $\mathbf{s}(k)$, then the estimator design equation becomes

$$\det\left(zI - (\mathbf{F}_{\mathbf{S}(k)} - \mathbf{L}_{\mathbf{p}_{\mathbf{S}(k)}}\mathbf{C}_{\mathbf{S}(k)})\right) = \alpha(z)_{\mathbf{S}(k)} \tag{3.81}$$

As a rule of thumb [61], the estimator poles can be chosen to be two to six times faster than that of the controller. The pole placement and estimator gain calculation can be done using Ackerman's formula or the *place.m* function in Matlab®.

### 3.4.3 Current estimator

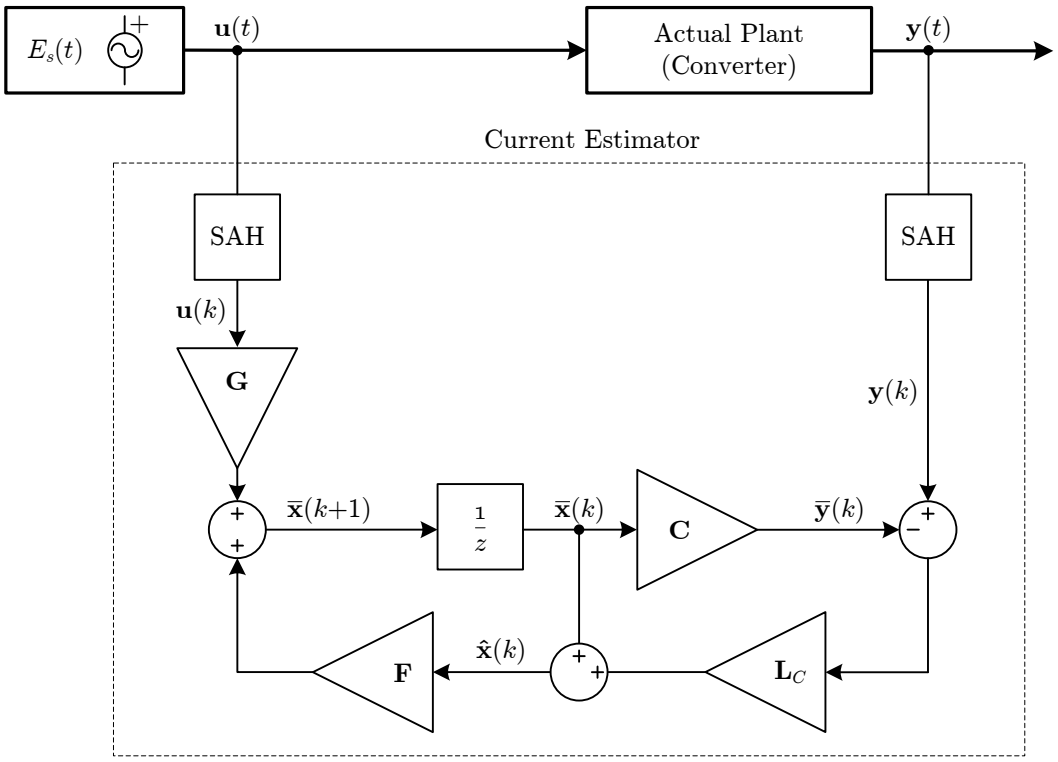
The current estimator uses measurements at time step $k$ to estimate the state vector at $k$. The equation describing the current estimator is given by

$$\hat{\mathbf{x}}(k) = \bar{\mathbf{x}}(k) + \mathbf{L}_{\mathbf{c}_{\mathbf{S}(k)}}\left(\mathbf{y}(k) - \mathbf{C}_{\mathbf{S}(k)}\bar{\mathbf{x}}(k)\right) \tag{3.82}$$

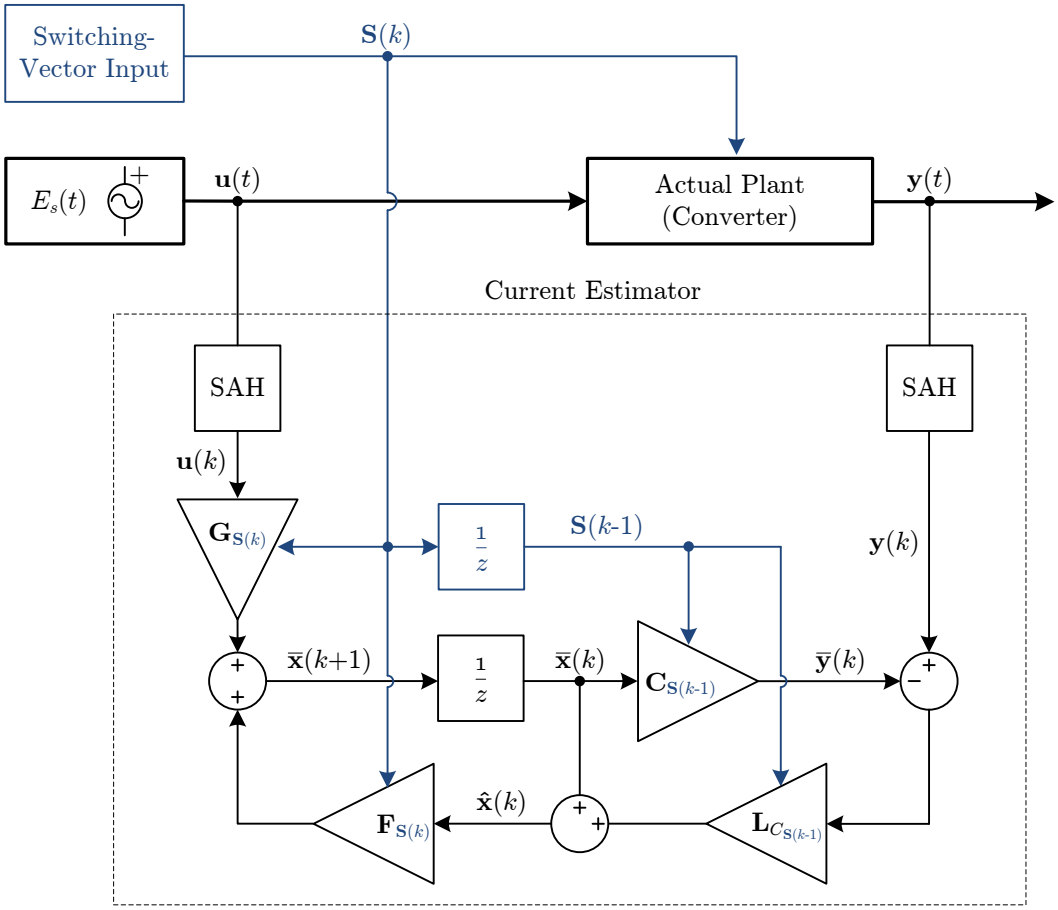
where $\hat{\mathbf{x}}(k)$ is the estimate of the state vector at $k$ for the present switching vector $\mathbf{S}(k)$, $\mathbf{L_c}$ is the current estimator gain and $\bar{\mathbf{x}}(k)$ is the predicted state estimate at $k$. The predicted state estimate is calculated at time step $k$ and used at $k+1$. The equation for the predicted state estimate is given by

$$\bar{\mathbf{x}}(k+1) = \mathbf{F}_{\mathbf{S}(k)}\hat{\mathbf{x}}(k) + \mathbf{G}_{\mathbf{S}(k)}u(k). \tag{3.83}$$

A block diagram of the current estimator is shown in Figure 3.23a. The current estimator is also designed for a single linear plant model. In order to use the current estimator




(a) Current estimator




(b) Switched current estimator

Figure 3.23: Current estimator block diagrams

with model predictive control, the estimator has to be described by a finite set of linear models, each representing a physical switching state.

In (3.21) and (3.76) the physical switching state is indicated by the switching vector subscript $\mathbf{S}(k)$. The switching vector $\mathbf{S}(k)$ is updated at time $k$ and represents the switching state that the system will be in from $k$ up to $k+1$. The current estimator corrects the tracking error at time $k$ using measurements at $k$. However, the tracking error was introduced between time $k-1$ and $k$, when the switching state was represented by $\mathbf{S}(k-1)$. Therefore, the switching state of (3.82) is given by $\mathbf{S}(k-1)$ while the switching state of (3.83) is given by $\mathbf{S}(k)$. The two adapted current estimator equations then become

$$\hat{\mathbf{x}}(k) = \bar{\mathbf{x}}(k) + \mathbf{L}_{\mathbf{c}_{\mathbf{S}(k-1)}} \left(\mathbf{y}(k) - \mathbf{C}_{\mathbf{S}(k-1)}\bar{\mathbf{x}}(k)\right) \tag{3.84}$$

and

$$\bar{\mathbf{x}}(k+1) = \mathbf{F}_{\mathbf{S}(k)}\hat{\mathbf{x}}(k) + \mathbf{G}_{\mathbf{S}(k)}u(k). \tag{3.85}$$

A block diagram of the adapted current estimator is shown in Figure 3.23b.

The current estimator gain $\mathbf{L_c}$ is related to the predictor estimator gain $\mathbf{L_p}$ through the static relationship

$$\mathbf{L_p} = \mathbf{F}^{-1}\mathbf{L_p}. \tag{3.86}$$

The current estimator gain can therefore be designed by using the same technique as for the predictor estimator and converting the result using (3.86).

### 3.4.4 Observability

In order for a system to be observable the entire set of models for each switching vector should be observable. The observability test verifies that the current state vector can be determined by using only the output vector as reference. The system is said to be observable, when the observability matrix has full rank. The observability test [61] is given by,

$$rank\left(\begin{bmatrix}\mathbf{C_S} & \mathbf{C_S A_S} & \mathbf{C_S A_S}^2 & \dots & \mathbf{C_S A_S}^{n-1}\end{bmatrix}^{\mathrm{T}}\right) = n \tag{3.87}$$

with $n$ being the order of the model and the subscript $\mathbf{S}$ the set of models corresponding to the switching vector.

## 3.5 Summary

This chapter presented the development of a finite-control-set model predictive control method for achieving a fixed switching frequency. The control of multi-level converters, especially for high voltage and high power configurations, often poses a challenge and requires strict balancing and stability to ensure that physical limits are not exceeded.

FCS-MPC was chosen for its ability to control multiple state variables without the need for complex control loops. However, it was shown that conventional FCS-MPC techniques are typically characterised by a variable switching frequency with a high noise floor. For the purpose of power quality on electrical distribution networks, the output voltage waveform should conform to strict grid codes and maintain a low THD. As such, an output waveform with a fixed switching frequency was preferred as it lowers the noise floor and contains the spectrum to known frequencies.

In order to achieve FCS-MPC with a guaranteed fixed switching frequency, hard constraints were applied separately from the cost function and the sampling rate was increased with respect to the desired switching frequency. The constraints were derived by using the switching behaviour of PWM to define regions where only specific switching vectors may be applied.

It was shown that the switching period can be divided into constrained prediction regions that are derived from the behaviour of PWM. Each prediction region is defined in such a way that only one switching transition may occur in that region. The purpose of this is to reduce the number of prediction choices to a choice between only two states. This was done in order to reduce the number of on-line calculations, which allows the controller to be sampled at a much higher rate.

The principle of operation is to sample the controller at a much higher rate then the switching frequency and advance in steps of the sampling period while predicting the average value of the controlled variable for multiples of the switching period, based on the current region. This is done to determine the optimal time to apply the switching transition for the given region. The method consists of two parts; the off-line calculation and storage of prediction matrices in a lookup table and secondly the on-line execution of the controller.

The off-line calculation of prediction matrices were done to reduce the number of on-line calculations which allows the controller to increase the resolution on the time axis. A general controller architecture was derived by using the established state-space representation. This allows the controller to be implemented for an arbitrary topology by only using a state space model of the plant.

A general architecture for implementing the online controller on an FPGA was presented. It was shown that although the switching frequency is constrained without using the cost function, the control block diagram remains the same as that of conventional FCS-MPC. The on-line predictions are reduced to a multiply and add operation where the current state vector and input vector are simply multiplied with the appropriate prediction matrices from the lookup table.

Lastly, it was shown that if the full state vector is not directly available through measurements, a switched state observer can be used.

In the subsequent chapters, the practical implementation and experimental evaluation

of the derived control method is discussed on three topologies. In Chapter 4, the implementation and experimental evaluation of the controller on the medium-voltage electronic voltage regulator is discussed. To verify the results, the controller is further evaluated for a five-level flying capacitor converter in Chapter 5. Lastly, in Chapter 6 the controller is evaluated and compared to linear control with PWM by using a single-leg inverter topology.

# Chapter 4

# Control of a medium-voltage electronic voltage regulator

## 4.1 Introduction

In this chapter, the hardware topology and control of a medium-voltage electronic voltage regulator for continuously regulating the voltage on a medium-voltage electrical distribution feeder is presented. Mechanical tap changers are commonly used as voltage regulators on distribution feeders to manage voltage levels. With the growing demand for embedded renewable generation, the impact of embedded sources on distribution feeders necessitates the investigation of future grid devices for maintaining the quality of supply. In [71], an investigation was done to determine the influence of photo-voltaic generators on the voltage control of distribution feeders and how the maximum generator penetration levels of these feeders can be increased. The study found that the maximum penetration level of the feeders are primarily limited by the rapid voltage change or voltage rise on the feeder.

Various technologies for increasing the penetration level of distributed generation were discussed including the use of electronic voltage regulators. It was shown that when conventional on-load tap changers are replaced by electronic voltage regulators with continuous regulation it is possible to increase the base penetration levels by between 50 % and 80 %.

In this chapter, an electronic voltage regulator topology is presented that is able to continuously regulate the voltage on a medium-voltage feeder. In order to react to rapid voltage changes on the feeder as well as fast changing load conditions, a controller design using FCS-MPC with a fixed switching frequency is presented.

## 4.2 Electronic voltage regulator hardware

This section provides and overview of the electronic voltage regulator topology and operation for the purpose of understanding the controller design requirements. For the detailed design of the voltage regulator see Appendix A and for the complete model derivations see Appendix C.

### 4.2.1 Hardware specifications and requirements

The voltage regulator is required to regulate the voltage on a medium-voltage feeder. A circuit diagram, depicting the connection of three voltage regulators to a three-phase line is shown in Figure 4.1. Three voltage regulators are connected in a star configuration with each phase having its own independent regulator. Since all three voltage regulators are identical, only one voltage regulator design is necessary.

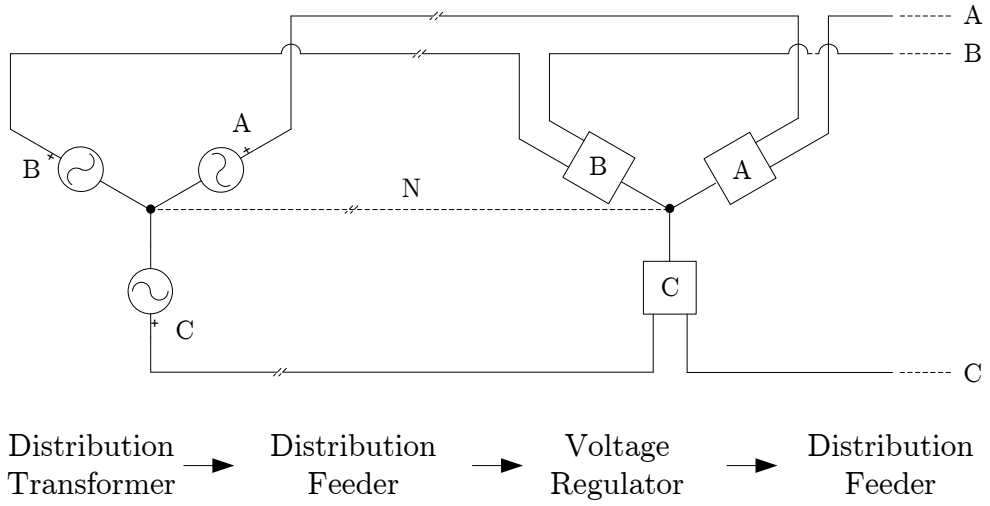



Figure 4.1: Diagram of a three-phase distribution feeder with three voltage regulators connected in a star configuration.

According to the South African NRS-048 standard for quality of electricity supply [77], the voltage on a medium voltage network may deviate from the agreed nominal voltage by a maximum of 10 %. Furthermore, it is assumed that the deviation of the line voltage will mostly be lower than the nominal voltage as a result of loading or losses in the distribution feeder. Therefore, the voltage regulator can be designed as a boosting regulator with a maximum boosting capability of 10 % above the input voltage. The NRS-048 standard also requires that any voltage harmonic distortion above 1 kHz should be lower than 0.2 % and the voltage regulator should provide sufficient filtering.

Furthermore, the distribution feeder has a nominal current rating of 100 $A_{rms}$ and the regulator must handle a maximum continuous current of 100 $A_{rms}$ for every input and output voltage.

Distribution feeders are typically equipped with circuit breakers and surge arrestors to protect the line against voltages that go out of bounds or over-current conditions. In order for the line protection to function correctly, the voltage regulator may not break continuity of the distribution feeder during a fault condition or when the regulator is not operational. The regulator should therefore handle any fault current for a small duration of time, until the line protection is activated. The voltage regulator specifications are summarised in Table 4.1.

Table 4.1: Voltage regulator specifications.

| **Specification** | **Value** |
|---:|---|
| Regulator Setup: | Boosting |
| Input Voltage Per Regulator (nom): | 12.7 kV |
| Input Voltage Deviation Range: | $\pm 10$ % |
| Maximum Input Voltage Per Regulator (peak): | 19.76 kV |
| Maximum Output-Voltage Regulation: | $V_{input}$ + 10 % |
| Number of AC-to-AC converter Modules: | 2 |
| Single Phase Power Rating (nom): | 1.27 MVA |
| Three Phase Power Rating (nom): | 3.82 MVA |
| Power Rating per AC-to-AC Converter Module: | 63.5 kVA |
| Maximum Output Voltage Ripple: | $\leq 0.1$ % |

### 4.2.2 Electronic voltage regulator topology

The use of IGBT based systems for medium and high voltage applications have been limited since the operating voltage is much higher than the breakdown voltage of commercially available IGBTs. Furthermore, the switching losses in higher voltage IGBTs limit the switching frequency and consequently limit the quality of the output voltage. One solution of dealing with these limitations is to split the system into lower voltage modules and stacking them in series.

The medium-voltage (MV) regulator, discussed in [72] and [73] was designed to regulate a nominal line voltage of 6.35 kV. This is done by connecting an AC-to-AC converter across the series winding of an autotransformer and controlling only 10% of the line voltage. In order to regulate at higher voltages, control has to be split between more than one AC-to-AC converter. This chapter discusses the control of a 12.75 $kV_{LN}$ voltage regulator consisting of two modules, each controlling 5% of the total line voltage. In order to regulate a three-phase line, three single-phase 12.75 $kV_{LN}$ regulator units can be connected in a star configuration.

Instead of using a hard-wired autotransformer, a three-winding transformer is used with one primary winding (common winding) and two isolated secondary windings (series windings) as shown in Figure 4.2 [78]. The winding ratios are chosen such that each secondary terminal voltage is 5% of the primary voltage. Each secondary winding is used

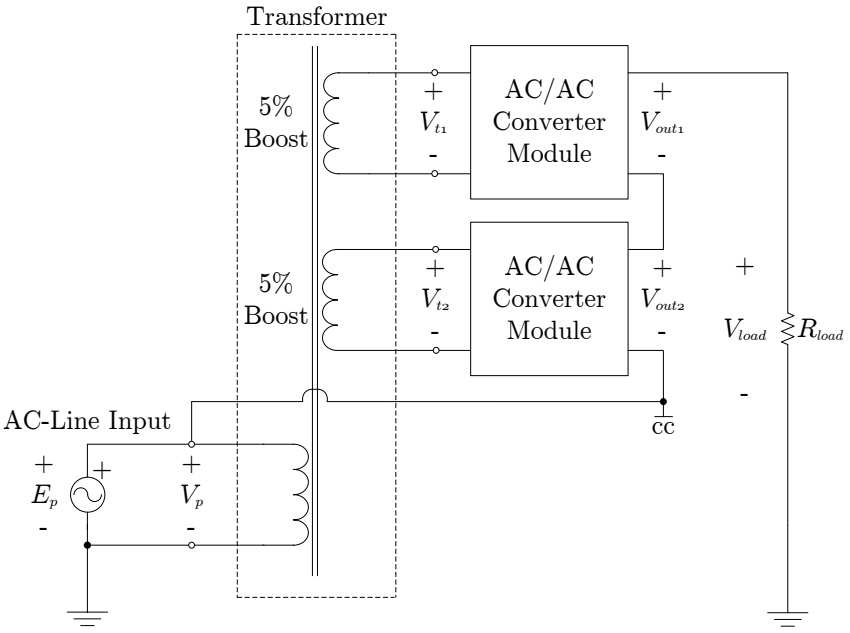



Figure 4.2: Schematic diagram of the shunt-series configuration with cascaded voltage regulator modules.

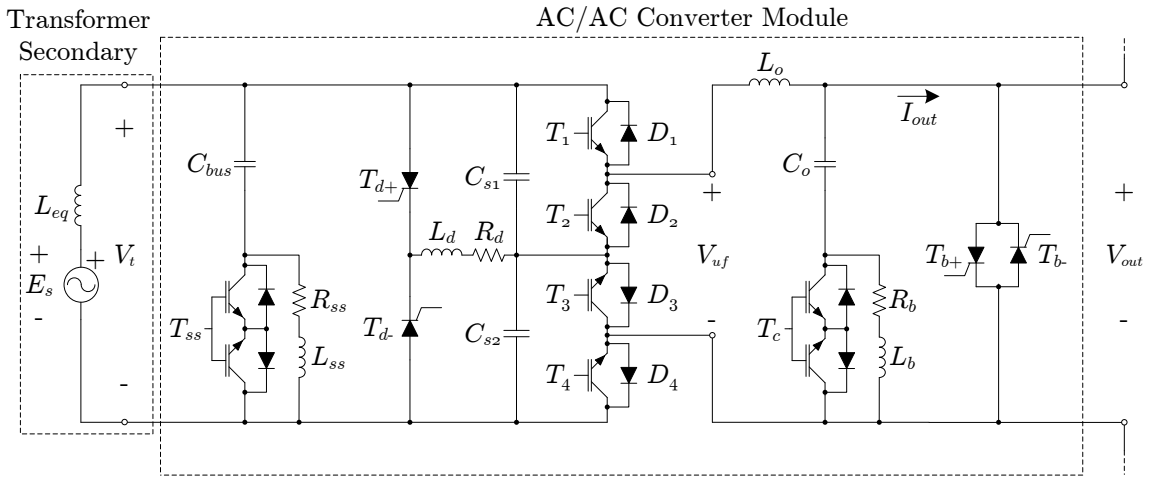


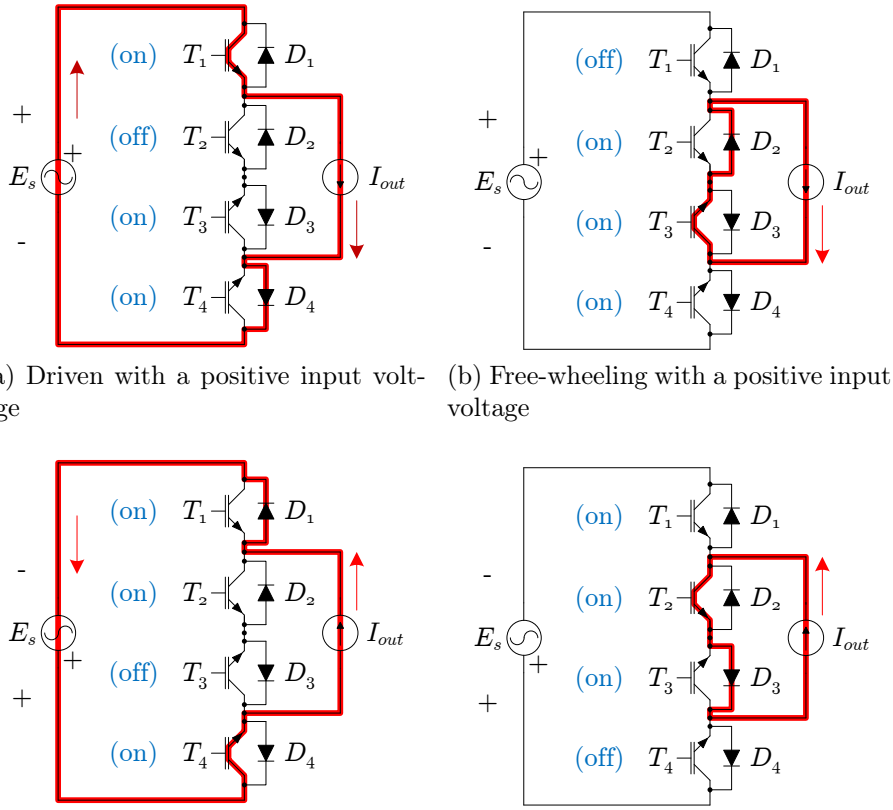

Figure 4.3: AC-to-AC converter topology with protection mechanisms.

as an isolated voltage source for two AC-to-AC converter modules. The two converter outputs are connected in series, with the top converter connected to the load side of the line and the bottom converter connected to the primary winding of the transformer. This creates a shunt-series configuration where multiple converter modules can be series-stacked to allow for higher voltage operation. With this configuration, control is applied to only 10% of the line voltage which reduces the power requirements of the regulator to only 10% of the transmitted power.

### AC-to-AC converter

The AC-to-AC converter topology that is used in [72] and [73] for the development of a 6.35 kV voltage regulator has the disadvantage that the IGBT snubber capacitor voltage can exceed the input bus voltage under fault conditions. For this reason an alternative AC-to-AC converter topology [79], [80] shown in Figure 4.3, is chosen for the multilevel regulator configuration in this text. The voltage across the IGBT snubber capacitors, $C_{s1}$ and $C_{s2}$ cannot exceed the input bus voltage, $V_t$, since they are effectively connected in parallel to the capacitor $C_{bus}$ through the free-wheeling diodes $D_1$, $D_2$, $D_3$ and $D_4$. As a result, only one over-voltage protection mechanism is needed for the input bus.

The circuit diagram of the converter, shown in Figure 4.3, is simply an AC-to-AC chopper circuit with an output $LC$ filter, configured to allow for positive and negative voltages. The output $LC$ filter, represented by inductor $L_o$ and capacitor $C_o$, is required to comply with utility requirements on voltage quality.




(a) Driven with a positive input voltage

(b) Free-wheeling with a positive input voltage

(c) Driven with a negative input voltage

(d) Free-wheeling with a negative input voltage

Figure 4.4: AC-to-AC converter driving and free-wheeling conduction paths for each switching state

The converter can be seen as consisting of two synchronous buck converters, one for a positive terminal voltage $V_t$ and one for a negative terminal voltage. During a positive half cycle, the IGBTs $T_1$ and $T_2$ are switched as a complimentary pair while $T_3$ and $T_4$

remain on. This is illustrated in Figure 4.4 (a) and (b), which shows that the load is either driven by the positive input voltage or is allowed to free wheel. Likewise, during a negative half cycle $T_3$ and $T_4$ are switched as a complimentary pair while $T_1$ and $T_2$ remain on, as shown in Figure 4.4 (c) and (d).

Although there are four possible switch combinations for each AC-to-AC converter module, this shows that if the sign of the input voltage is taken into account only one of two states is applied at any given time: a *driving* state or a *free-wheeling* state. By taking the symmetry of the topology into account, the equivalent circuit for the *driving* state and *free-wheeling* state for the positive and negative half-cycles becomes the same.

The AC-to-AC converter modules are superimposed and floating at the line voltage, but for the purpose of control, it is not necessary to include the transformer and line voltage in the prediction model. The superimposed line voltage can be accounted for by adjusting the control references accordingly.

### Commutation mechanisms

The two snubber capacitors, $C_{s1}$ and $C_{s2}$, solve the commutation problems usually associated with AC-to-AC converters. During dead time, when all four switches are off, a path has to exist for the current through the inductor $L_o$. For this purpose, $C_{s1}$ and $C_{s2}$ are used together with the diodes $D_1$, $D_2$, $D_3$ and $D_4$. Furthermore, when all the switches are turned off, a return path for the current through the equivalent transformer inductance $L_{eq}$ is created through the bus capacitor $C_{bus}$.

The snubber capacitors $C_{s1}$ and $C_{s2}$ are used to prevent the voltage across the IGBTs from exceeding the maximum bus voltage during dead time. Both capacitors are designed to be identical and the maximum dead time is estimated as 2 $\mu$s. The maximum operating bus voltage, $V_{t(op)}$, is 988 V. Based on the maximum allowed voltage of the capacitors, the maximum allowed bus voltage $V_{t(max)}$ is chosen as 1 200 V.

During normal operation, when the chopper is in the free-wheeling state, capacitor $C_{bus}$ provides a return path for the current through the transformer inductance $L_{eq}$. During this time, the bus voltage has to remain within the 1 200 V limit. If the system is switched at a fixed switching frequency of 10 kHz, the maximum free-wheeling time, $t_{off}$, is taken to be one switching period $T_{sw}$. The maximum output current is taken as 100 $A_{rms}$ with a maximum ripple of $\pm 30\%$ while the output voltage is taken as 635 V with a maximum ripple of $\pm 1\%$.

### Protection mechanisms

The bus capacitor and snubber capacitors are designed to provide a path for the inductor currents for only a specified amount of time. If that time is exceeded during a fault condition, the capacitor voltages would increase beyond their ratings. For this reason, over-voltage protection is implemented by means of a dump-crowbar.

The two thyristors, $T_{d+}$ and $T_{d-}$, are connected across the input bus to a dump resistor $R_d$ as shown in Figure 4.3. Each thyristor is set up to act as a crowbar [81], [82] by using a breakover diode driver [83], [84], [72] to trigger the thyristor when an over-voltage occurs.

When a short-circuited fault or overloading of the distribution feeder occurs, over-voltage and over-current protection of the AC-to-AC converter modules is required. This is achieved by adding a bypass-crowbar across the output terminals of each AC-to-AC converter module. The bypass-crowbar is implemented by using the thyristors $T_{b+}$ and $T_{b-}$ as shown in Figure 4.3 [81], [82]. Over-current conditions are detected and triggered by the controller while over-voltage conditions are triggered using a breakover diode trigger circuit.

The crowbar is connected across the filter capacitor $C_o$ and short-circuits the capacitor when closed. To prevent $C_o$ from being damaged, a filter cut-out is implemented which consists of the IGBT pair $T_c$ and bleed resistor $R_b$.

The bypass-crowbar driver is self-powered and operates independently from the controller power supply. To maintain continuity of the distribution feeder, the crowbar is set up as normally closed. Therefore, the controller has to actively keep the crowbar-bypass open during normal operation.

If a large voltage is applied across the input of the AC-to-AC converter when the bus capacitor is discharged, large inrush currents will occur as the bus capacitor is being charged. In order to to limit the inrush current and rate of rise of current ($\mathrm{d}i/\mathrm{d}t$), a soft-start mechanism is implemented. The soft-start is connected in series with the bus capacitor $C_{bus}$ and is realised by using the IGBT pair $T_{ss}$, limiting resistor $R_{ss}$ and the limiting inductor $L_{ss}$. During inrush, switch $T_{ss}$ is kept open while $C_{bus}$ is charged through the limiting resistor and inductor $R_{ss}$ and $R_{ss}$. After the bus capacitor has been charged, switch $T_{ss}$ is closed at the appropriate time and normal switching may commence.

### Filter resonance

The bus capacitor $C_{bus}$ is designed to keep the bus voltage below 1200 V while the converter is in the the *free-wheeling* state by providing a return path for the input inductor current. Each AC-to-AC converter is connected to a secondary windings of the transformer, which acts as an isolated voltage source. The leakage inductance of the transformer together with the line inductance is estimated by the equivalent input inductance $L_{eq}$ and equivalent series resistance $R_{Leq}$, as shown in Figure 4.3.

The equivalent input inductance seen by the converter together with the bus capacitor creates an input $LC$ filter that may vary, depending on the point of installation on the line. However, for the purpose of design, the line inductance can be ignored and only the leakage inductance of the transformer can be taken into account.

As a consequence, the input $LC$ filter does not provide much design room in terms of the cut-off frequency and damping. Furthermore, if the output voltage is controlled to

have a pure 50 Hz sinusoidal waveform, harmonics on the input voltage will be severely under-damped. Likewise, if the resonant frequency of the filter is excited, there will be little damping to attenuate the resonance. It is therefore important to know the resonant frequency and to ensure that the controller suppresses any possible resonant effects.

Unlike the input bus, the output $LC$ filter is designed specifically to comply with the grid standard [77] for voltage quality. This leaves room to design the output filter to comply with the standard and to have a resonant frequency that will not be excited by the switching frequency.

The natural undamped resonant frequency of an $LC$ circuit is given by

$$\omega_n = \frac{1}{\sqrt{LC}} \tag{4.1}$$

where $L$ is the inductance, $C$ the capacitance. However, both the input and output filters are connected to a load and can be estimated as an $LCR$ circuit with a resonant frequency at

$$\omega = \sqrt{\frac{1}{LC} - \frac{1}{(RC)^2}}. \tag{4.2}$$

With an estimated experimental transformer leakage inductance of 138.4 $\mu H$ and a 90 $\mu F$ bus capacitor, the undamped natural frequency of the input filter becomes

$$\begin{aligned} \omega_n &= \frac{1}{\sqrt{138.4\mu\text{H} \cdot 90\mu\text{F}}} \\ &= 8960 \text{ rad/s} \end{aligned} \tag{4.3}$$

which is approximately 1.42 kHz.

If the maximum nominal current is 100 $\text{A}_{rms}$ and the maximum nominal bus voltage is 698 $\text{V}_{rms}$, the maximum load as seen by the input bus can be estimated as 6.98 $\Omega$. This leads a maximum damped resonant frequency of

$$\begin{aligned} \omega &= \sqrt{\frac{1}{(138.4\mu\text{H} \cdot 90\mu\text{F})} - \frac{1}{(6.98\ \Omega \cdot 90\mu\text{F})^2}} \\ &= 8817.5 \text{ rad/s} \end{aligned} \tag{4.4}$$

which is 1.4 kHz. This shows that for the input bus, the resonant frequency will vary between 1.4 kHz and 1.42 kHz.

The damping ratio of an $LC$ low-pass filter with loading resistor $R$ is given by

$$\zeta = \frac{1}{2R}\sqrt{\frac{L}{C}}. \tag{4.5}$$

For the above mentioned parameter values, the maximum damping factor of the input $LC$ pair becomes $\zeta = 0.089$. This shows that even under maximum loading, the input bus remains under-damped and may encounter unwanted ringing if not anticipated. When designing the controller it is therefore important to ensure that the input bus resonant frequency is avoided or suppressed.

### Experimental laboratory set up

A photograph of the experimental laboratory set up of the MVEVR is shown in Figure 4.5. The voltage regulator consists of two AC-to-AC converter modules that are mounted onto separate insulated cross-beams within a metal frame as shown in the figure. The transformer is placed behind the voltage regulator and is not clearly visible in the photograph. The heatsinks for the IGBTs of the two respective converter modules are force air-cooled by the fans that are visible at the front each converter module.

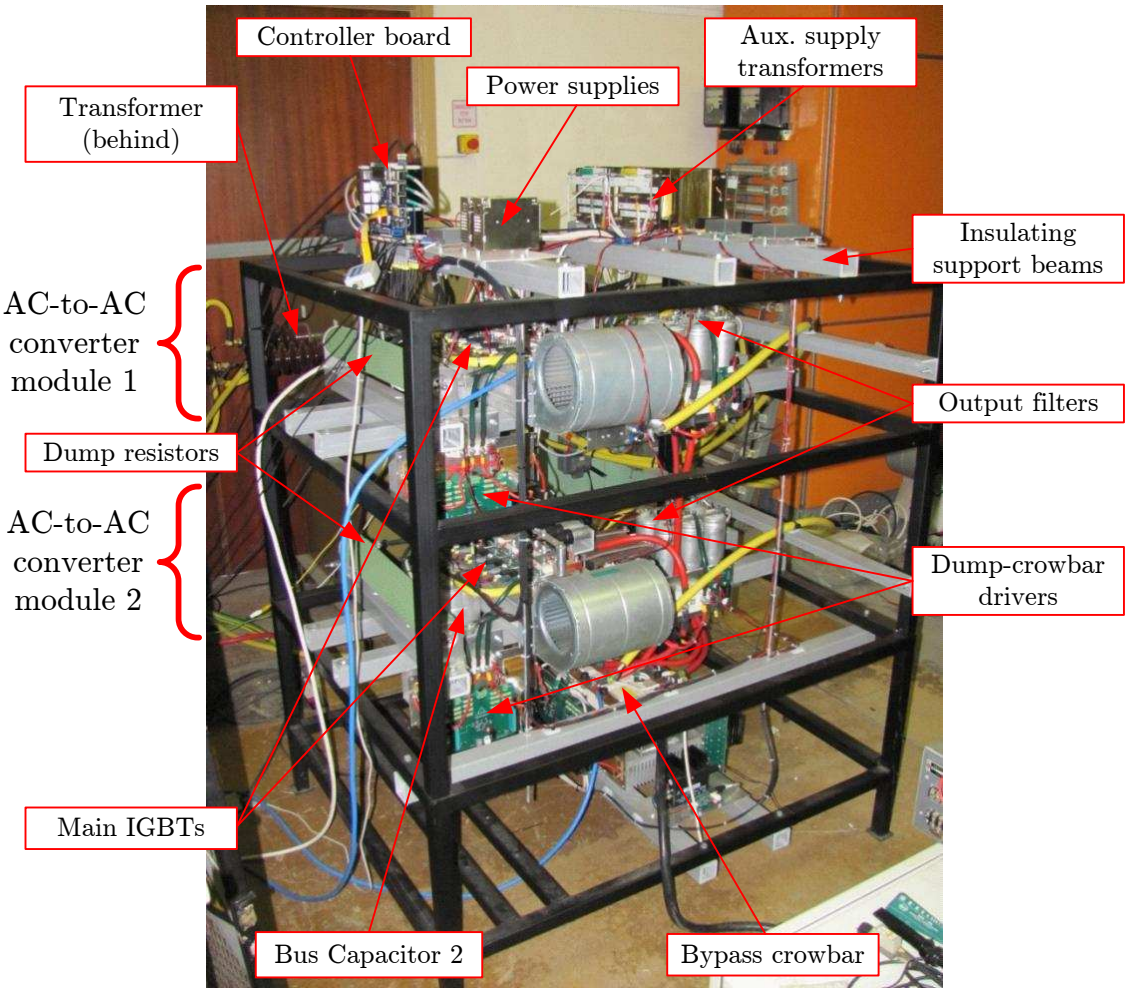



Figure 4.5: Photograph of the experimental set up of the medium voltage electronic voltage regulator

## 4.3 Controller design: FCS-MPC with a fixed switching frequency

### 4.3.1 Plant model and control objectives

In the previous section it was shown that the voltage regulator consists of two AC-to-AC converter modules that are connected in a shunt-series configuration to an appropriate transformer. For the purpose of control, it is not necessary to take the entire transformer configuration into account and only the two AC-to-AC converter modules together with the transformer leakage inductance may be considered.

The topology for the two cascaded AC-to-AC converter modules can be simplified by assuming that the snubber capacitors, which are in parallel with the bus capacitor, becomes negligible. Furthermore, the output $LC$ filters of the two modules can be reconfigured and taken as a single output filter. This reduces the plant model by eliminating two state variables. The resulting circuit diagram of the simplified model is shown in Figure 4.6.

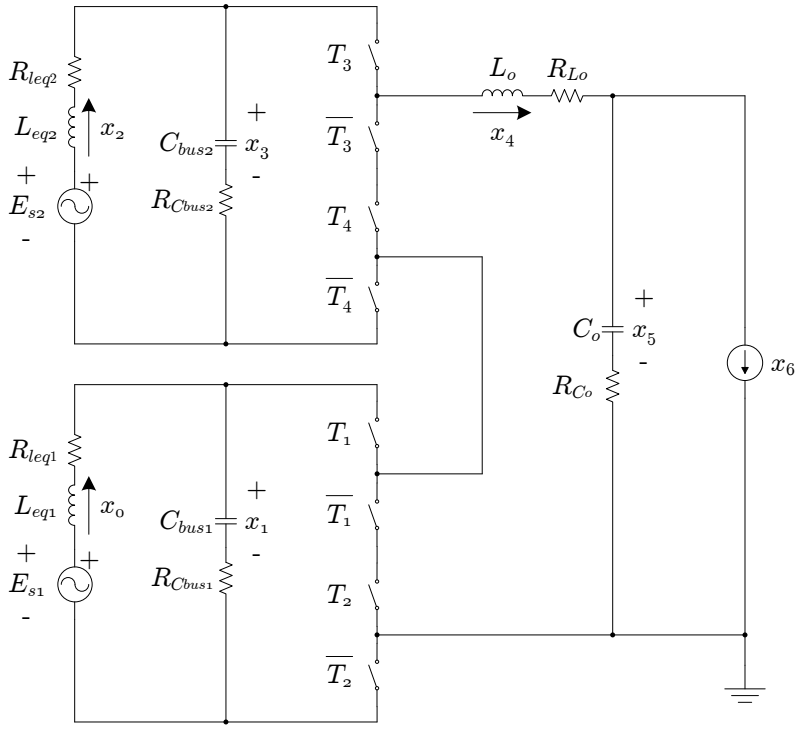



Figure 4.6: Simplified circuit diagram of two cascaded AC-to-AC converters with an unknown load.

The simplified circuit diagram has eight actuation choices but, by taking the symmetry between the positive and negative half-cycles into account, the number of states that can be applied becomes four: *free-wheel–free-wheel*, *free-wheel–drive*, *drive–drive* and *drive–free-wheel*. FCS-MPC considers the system as a finite set of models where each model

represents an actuation choice. Due to the symmetry of the topology the state-space models also follow these four switching states. A complete derivation of the state-space matrices for each switching state is given in Appendix C.1.

From the diagram it is shown that the model contains seven state variables that can be described by the state vector $\mathbf{x}$ as

$$\begin{aligned}\mathbf{x} &= \begin{bmatrix} x_0 & x_1 & x_2 & x_3 & x_4 & x_5 & x_6 \end{bmatrix}^\top \\ &= \begin{bmatrix} I_{in1} & V_{t1} & I_{in2} & V_{t2} & I_{L_o} & V_{out} & I_{out} \end{bmatrix}^\top . \end{aligned} \tag{4.6}$$

For industrial applications it is not always possible or desirable to measure all the state variables due to cost. However, for the purpose of demonstrating the control method, two scenarios will be presented: (a) all the state variables are directly measured and (b) the two module input currents $I_{in1}$ and $I_{in2}$ and load current $I_{out}$ are estimated.

In the simplified diagram the converter modules are driven by the two voltage sources $E_{s1}$ and $E_{s2}$. These voltage sources represent the ideal internal voltages of the secondary windings of the transformer prior to the leakage inductance. The output voltage of these sources are considered to be identical and is obtained by measuring the voltage on the primary winding of the transformer and scaling the measurement according to the transformer winding ratios. The winding ratios can be obtained by measuring the voltages across the primary and secondary terminals when no load is connected to the secondary terminals.

### Control objectives

The primary control objective is to control the output voltage $V_{out}$ by tracking a sinusoidal reference signal. In addition to that, as a secondary control objective, the controller should suppress resonance on the input bus by controlling the input current and only allowing lower frequency components.

The controlled output voltage should have a low THD, respond fast to reference and load step changes and be independent of the load impedance. Although the controller is designed for a system with known component values, the actual values often vary due to component tolerances, temperature and parasitic inductance and capacitance. As such, the controller should be able to tolerate small deviations in the plant model and reject converter imperfections such as dead time. Lastly, although design precautions are taken to minimize measurement noise, the controller should still be able to reject a reasonable level of noise, should it be present.

## 4.3.2 Controller design

### 4.3.2.1 Controller scheme

The FCS-MPC control scheme with a fixed switching frequency is implemented according to the control block diagram in Figure 3.17b which makes use of a state observer to estimate the unmeasured state variables.

The off-line calculations are done by using Python together with the Numpy and SymPy libraries. The on-line controller is implemented on an FPGA with a clock frequency of 20 MHz according to the state flow diagram in Figure 3.21.

### 4.3.2.2 Control references

#### Output voltage

The primary purpose of the voltage regulator in Figure 4.2 is to regulate the line or feeder voltage at a pre-defined reference voltage $V^*_{load}$. The difference between the regulator input voltage $V_p$ at the primary terminals of the transformer and the regulator output voltage to the load $V_{load}$ is determined by the combined AC-to-AC converter output voltage $V_{out}$ according to the relationship

$$V_{load} = V_p + V_{out}. \tag{4.7}$$

Using the relationship in (4.7), the control reference $V^*_{out}$ of the AC-to-AC converter modules can be written as

$$V^*_{out} = V^*_{load} - V_p. \tag{4.8}$$

The reference voltage $V^*_{out}$ can be realised by a sinusoidal function generator of the form

$$V^*_{load}(t) = A\sin(\omega t + \Phi + \Theta) \tag{4.9}$$

where $A$ is the reference amplitude, $\omega$ is the measured network frequency in rad/$s$, $\Phi$ is the phase shift to account for the average predicted value across the switching period and $\Theta$ is the phase shift between the input and output of the AC-to-AC converter.

The control reference is recalculated and updated on-line at every sampling instance. The amplitude $A$ can be obtained by using a sliding window to calculate the RMS value of the input voltage $V_p$. To allow for a faster response to changes in the line voltage, the sliding window can be used to calculate the RMS value over a quarter of the period of the line frequency. By using the relationship in (4.8), the amplitude of $V^*_{out}$ is obtained.

Ideally the network frequency should be at 50 Hz. However as the utility tries to match demand, the network frequency my deviate slightly from the declared 50 Hz [77]. The controller should allow for this deviation by detecting and synchronising the reference signal to the network frequency.

The phase shift $\Phi$ is used to compensate for the averaged predictions over the switching period and is implemented as given in (3.58). The phase shift $\Theta$ is used to account for

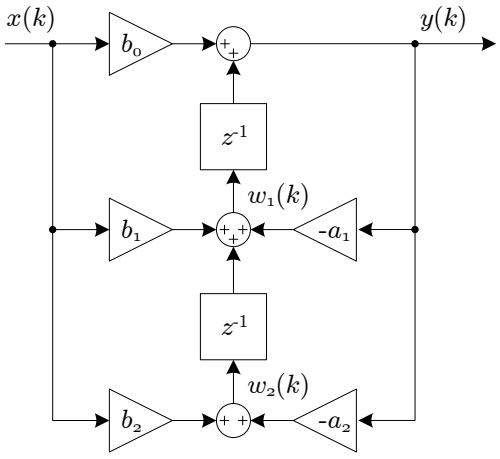



Figure 4.7: Transposed direct form II IIR filter structure

the phase shift that is introduced by the input and output *LC* filters. The AC-to-AC converter topology does not implement DC energy storage and may introduce an error at the zero-crossings under severe loading. If needed, the phase can be adjusted for large loads to compensate for the phase shift.

### Suppression of input current resonance

It was shown that under certain conditions the leakage inductance of the transformer may resonate with the bus capacitors in an under-damped manner. In order for the controller to damp the resonance, control references for the desired input currents are needed.

On medium voltage distribution feeders it cannot be assumed that the load current will have a perfect sinusoidal waveform and as such, a sinusoidal control reference will only be of value in laboratory configurations. In order to find a practical control reference without strictly enforcing a sinusoidal waveform, a second-order low-pass filter can be used.

The resonant frequency is typically much higher than the fundamental 50 Hz network frequency. By passing the input current through a low-pass filter, the filtered signal can be used as the control reference for suppressing the higher resonant frequencies. This does not provide an optimal control reference as it distorts the unknown current waveform and introduces a small phase shift, but, it is sufficient for the purpose of damping the resonance.

The filter can be realised as a digital filter by using the transposed direct form II IIR filter structure as shown in Figure 4.7 [85]. The transfer function for a second-order direct form II transposed filter is given by

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}} \tag{4.10}$$

and the implementation equations are given by

$$\begin{aligned} y(k) &= b_0 x(k) + w_1(k-1) \\ w_1(k) &= b_1 x(k) - a_1 y(k) + w_2(k-1) \\ w_2(k) &= b_2 x(k) - a_2 y(k). \end{aligned} \tag{4.11}$$

The selection of the type of filter depends on the choice of characteristics that are important. For example, a Butterworth LPF is designed to have a maximally flat frequency response in the passband while a Chebyshev type I filter has a pass-band ripple but a sharper cut-off slope. If the cut-off frequency is much higher than the 50 Hz network frequency then a Butterworth filter should be sufficient. If the cut-off frequency is lower and a sharper response is needed, a Chebyshev type I filter can be used. Both these filters introduce a phase shift in the pass-band that cannot be avoided, but, for the purpose of resonance damping the phase shift of a second order filter is acceptable. For the voltage regulator, a Butterworth filter is chosen with a cut-off frequency at 750 Hz.

The coefficients of the transfer function can be obtained by using filter design tools such as the `butter()` and `cheby1()` functions in Matlab® or the `scipy.signal.butter()` and `scipy.signal.cheby1()` functions in Python with Scipy library.

#### 4.3.2.3 Cost function

The control of the output voltage $V_{out}$ and the resonant damping of the input-bus voltages $V_{t1}$ and $V_{t2}$ can both be implemented as a reference tracking problem. The control objective for reference tracking is to minimize the error between the reference signal and the controlled state variable. This can be accomplished by defining a cost function for reference tracking by using the weighted sum of square values method.

In order to anticipate the transient effects during large voltage reference steps and load steps, the prediction horizon can be increased as discussed in Chapter 3.2.3. This is accomplished by defining an error band and increasing the prediction horizon when the error-band threshold $x_{thres}$ is exceeded. The error-band function is used to activate the cost function terms that correspond to the higher prediction horizons, and is defined as

$$f_{err}\big(x_{err}(k)\big) = \begin{cases} 0 & \text{if} \quad |x_{err}(k)| < x_{thres} \\ 1 & \text{if} \quad |x_{err}(k)| \geq x_{thres} \end{cases} \tag{4.12}$$

with

$$x_{err}(k) = x^*(k) - x(k). \tag{4.13}$$

Regardless of the horizon, the error $x_{err}(k)$ is always the difference between the measured state variable $x$ and the desired reference point $x^*$ at the present time instance $k$.

By using the error-band function, the cost function for tracking the output voltage with a prediction horizon of three can be written as

$$\begin{aligned} g_{V_{out}} = w_1 &\left( V^*_{out1} - V^p_{out1(av)} \right)^2 \\ &+ w_2 \left( V^*_{out2} - V^p_{out2(av)} \right)^2 f_{err}(V_{out(err)}) \\ &+ w_3 \left( V^*_{out3} - V^p_{out3(av)} \right)^2 f_{err}(V_{out(err)}) \end{aligned} \tag{4.14}$$

The error $V_{err(out)}$ is the difference between the present state variable and reference and is used to calculate the error function for all the horizon terms beyond the first one.

The state variable $V^p_{out1(av)}$ is the averaged predicted value of the output voltage over the first prediction horizon, $V^p_{out2(av)}$ at the second horizon and $V^p_{our3(av)}$ at the third. Likewise, the references at each horizon step is indicated by $V^*_{out1}, V^*_{out2}$ and $V^*_{out3}$. Note that the horizon is determined for the switching period $T_{sw}$ and not the sampling period $T_s$.

When $V_{out}(k)$ is within the bounds of $V_{thres}$, the system is considered to be in steady state and the terms relating to the higher prediction horizons are zeroed. If the threshold is exceeded, the error functions becomes non-zero and the predictions are made up to the maximum horizon.

For the purpose of damping the input currents, a horizon of one is sufficient. By using a sum of squares, the cost function is given by

$$g_{V_t} = w_4 \left( I^*_{Leq1} - I^p_{Leq1(av)} \right)^2 + w_5 \left( I^*_{Leq2} - I^p_{Leq2(av)} \right)^2. \tag{4.15}$$

The combined cost function for controlling the output voltage and damping the input currents then becomes

$$\begin{aligned} g &= g_{V_{out}} + g_{V_t} \\ &= w_1 \left( V^*_{out1} - V^p_{out1(av)} \right)^2 \\ &+ w_2 \left( V^*_{out2} - V^p_{out2(av)} \right)^2 f_{err}(V_{out(err)}) + w_3 \left( V^*_{out3} - V^p_{out3(av)} \right)^2 f_{err}(V_{out(err)}) \\ &+ w_4 \left( I^*_{Leq1} - I^p_{Leq1(av)} \right)^2 + w_5 \left( I^*_{Leq2} - I^p_{Leq2(av)} \right)^2 \end{aligned} \tag{4.16}$$

### Weighting factor adjustment

The importance of each term in the cost function is determined by multiplying each term with a weighting factor $w$. This allows the controller to place an emphasis on more important controlled variables and allowing the less important variables to have a lesser impact.

At this point there are no control design theories or analytical and numeric methods to adjust the weighting factors [4]. The weights are typically obtained by iterative evaluation until an acceptable response is obtained.

For the design of this controller the weights of each prediction horizon term of the output voltage $V_{out}$ is taken to be equal such that

$$w_1 = w_2 = w_3 \tag{4.17}$$

and the importance of the two secondary controlled variables are also taken to be equal such that

$$w_4 = w_5. \tag{4.18}$$

The weighting factors are adjusted by selecting an initial value for the primary controlled variable weights $w_1$,$w_2$ and $w_3$ and setting the secondary controlled variable weights $w_4$ and $w_5$ to zero. The weighting factors $w_4$ and $w_5$ are then gradually incremented until the desired response is obtained. The chosen weighting factor selection for the simulation and experimental results is given in the respective sections to follow.

## 4.4 Controller evaluation through simulation

### 4.4.1 Simulation overview

In order to evaluate the experimental measurement results, a benchmark for the ideal case is required. This section presents a benchmark for the expected experimental behaviour of the proposed FCS-MPC control method by way of simulation results. In Section 4.4.2 the behaviour of the control algorithm is extensively evaluated for a DC-to-AC configuration. The DC-to-AC configuration provides a way of verifying the controller without taking the AC input dynamics into account. In Section 4.4.3 the controller is evaluated for an AC-to-AC configuration and the stabilisation of the input filter is discussed. A summary of the results are given in Section 4.4.4.

In Appendix C.1 two sets of models are derived for the simulation. The one set of models is used to simulate the actual plant and includes a known load. The other set of models are used for the predictive controller and considers the load as an unknown current source. The schematic diagram of the simulated plant is shown in Figure 4.8

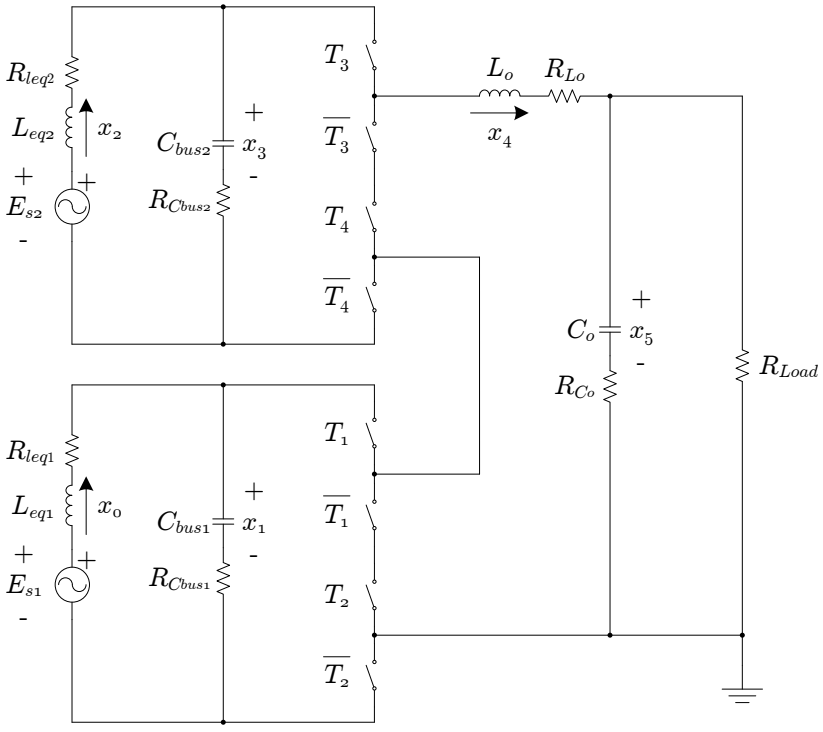



Figure 4.8: Schematic diagram of two cascaded AC-to-AC converter modules used for the simulation of the voltage regulator.

In order to compare the simulation results with practical measurements, the measured component values of the real system is used. Since the DC-to-AC configuration is driven from a rectifier and the AC-to-AC configuration is driven from an AC voltage source, the equivalent input inductance $L_{eq}$ of the plant model will be different for a DC input

voltage than for an AC input voltage. The measured parameters that are used for the simulation is summarised in Table 4.2.

Table 4.2: Measured component values of the real system and control parameters used for the control evaluations.

| DC-to-AC Setup | | AC-to-AC Setup | |
|---|---|---|---|
| Component | Value | Component | Value |
| $E_s$ | 200 $V_{DC}$ | $E_s$ | 635$V_{rms}$ |
| $L_{eq}$ | 9 $\mu$H | $L_{eq}$ | 140 $\mu$H |
| $R_{Leq}$ | 19 m$\Omega$ | $R_{Leq}$ | 19 m$\Omega$ |
| $C_{bus}$ | 90 $\mu$F | $C_{bus}$ | 90 $\mu$F |
| $R_{Cbus}$ | 1 m$\Omega$ | $R_{Cbus}$ | 1 m$\Omega$ |
| $C_{s1}$ | 1.41 $\mu$F | $C_{s1}$ | 1.41 $\mu$F |
| $R_{Cs1}$ | 1 m$\Omega$ | $R_{Cs1}$ | 1 m$\Omega$ |
| $C_{s2}$ | 1.41 $\mu$F | $C_{s2}$ | 1.41 $\mu$F |
| $R_{Cs2}$ | 1 m$\Omega$ | $R_{Cs2}$ | 1 m$\Omega$ |
| $L_o$ | 850 $\mu$H | $L_o$ | 850 $\mu$H |
| $R_{Lo}$ | 60 m$\Omega$ | $R_{Lo}$ | 60 m$\Omega$ |
| $C_o$ | 75 $\mu$F | $C_o$ | 75 $\mu$F |
| $R_{Co}$ | 6 m$\Omega$ | $R_{Co}$ | 6 m$\Omega$ |
| $R_{load}$ | 20 $\Omega$ | $R_{load}$ | 25 $\Omega$ |
| Control Parameter | Value | Control Parameter | Value |
| $F_s$ | 400 kHz | $F_s$ | 400 kHz |
| $F_{sw}$ | 10 kHz | $F_{sw}$ | 10 kHz |
| N | 40 steps | N | 40 steps |
| Horizon | 3 periods | Horizon | 3 periods |
| $V_{out(err)}$ | 5 V | $V_{out(err)}$ | 100 V |
| $W_1$ | 2 | $W_1$ | 2 |
| $W_2$ | 2 | $W_2$ | 2 |
| $W_3$ | 2 | $W_3$ | 2 |
| $W_4$ | 1 | $W_4$ | 1 |
| $W_5$ | 1 | $W_5$ | 1 |

### 4.4.2 Simulation results for a DC-to-AC configuration

In this section, a DC-to-AC simulation is performed to evaluate the response of the controller across the output range of the converter. Only the output voltage $V_{out}$ is controlled and no resonant suppression is needed for a DC input bus. The controller is evaluated for steady state operation, reference step response, load step response, an input voltage step response, the influence of measurement noise as well as the frequency spectrum. A sampling rate of 400 kHz is used with a switching frequency of 10 kHz.

#### Steady state

The simulation results for the output voltage during steady state operation is shown in Figure 4.9a. The output voltage is given a 50 Hz sine wave as reference, an amplitude of 90 % and a 20 Ω resistive load. The results show that under ideal conditions, the output voltage tracks the reference with a THD of 0.11 %, a tracking phase error of 0.0185° and an amplitude error of -6 mV.

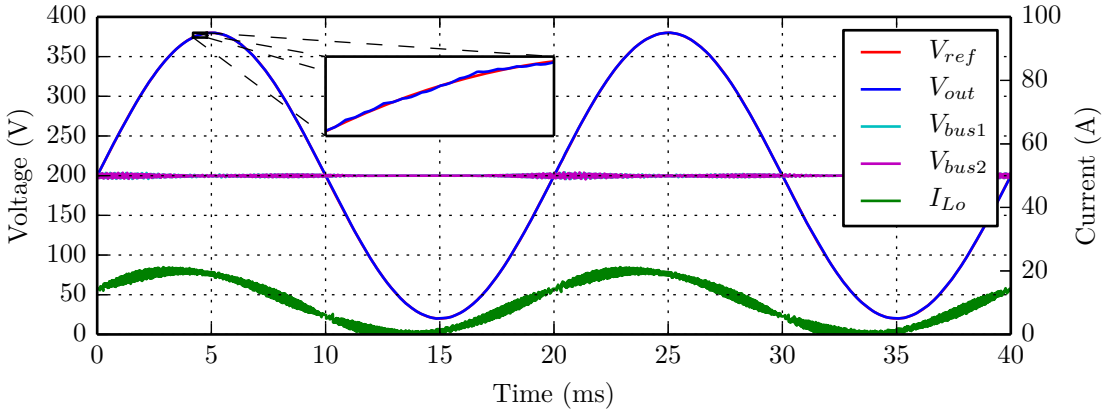
An FFT plot of the frequency spectrum is shown in Figure 4.9b. The two converter module's switching patterns are interleaved which result in a clear fixed switching frequency at 20 kHz. The raised noise floor, especially at the lower frequencies, can be attributed to the use of a binary prediction tree instead of a ternary tree as well as quantisation noise caused by the discrete sampling of the controller. A binary tree represents a reduced number of prediction choices as depicted in Figures 3.14b and 3.15b. When a ternary prediction tree is used, the noise floor at the lower frequencies are improved, but at the cost of a higher calculation effort. Furthermore, as the sampling frequency is increased, the quantisation noise is also reduced.

#### Output voltage reference step

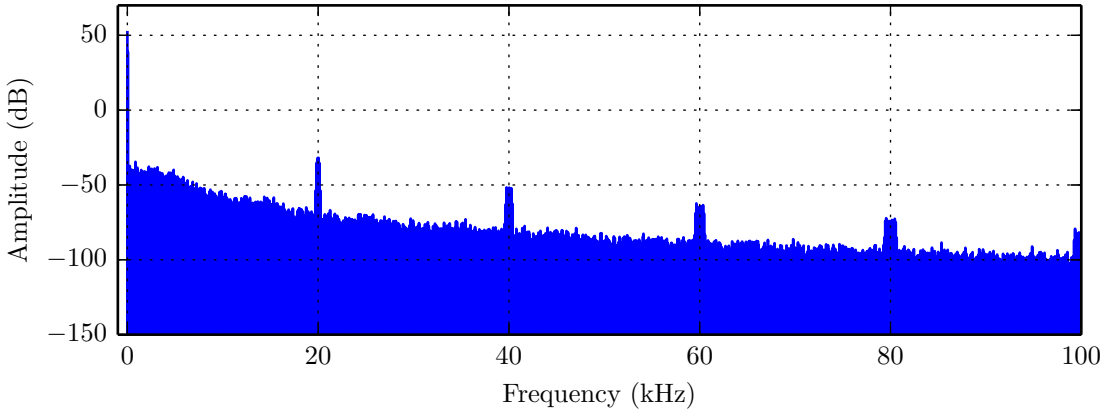
To show the controller's response to a sudden reference change, a voltage reference step is simulated. The simulation is set up with an initial voltage reference at 30 % after which it is stepped up to 90 %. Simulation results for the step response is shown in Figure 4.10. At 25 ms the voltage reference is stepped up and the output voltage immediately starts increasing at the maximum rate of rise. The inductor current is shown to have a sharp initial spike, which corresponds to the sudden change in load current. This shows that the controller has a fast reaction time and responds within one sampling instance to the load step with negligible overshoot. Likewise, during the reference step down, a fast reaction time is observed with negligible overshoot.

#### Load step

The controller's response to a load step is evaluated with a 200 V DC source and an output voltage reference at 90 %. An increasing load step is simulated from 20 Ω to 7.5 Ω




(a) Output voltage waveform




(b) Frequency spectrum of the output voltage waveform

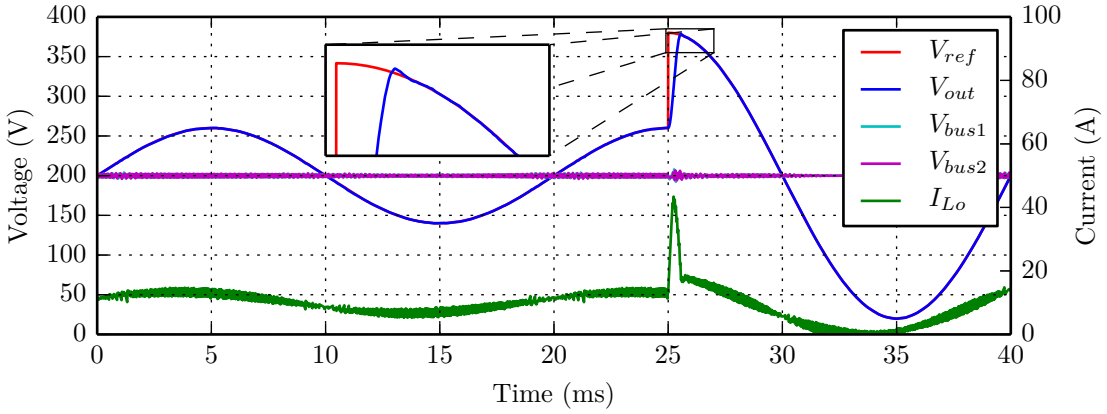
Figure 4.9: DC-to-AC simulation results for steady state conditions at a fixed switching frequency of 10 kHz and interleaved output switching frequency of 20 kHz. (THD: 0.11 %, Phase Error: 0.0185°, Amplitude error: -6 mV)

as shown in Figure 4.11a. The output voltage shows a sudden dip while the filter inductor current increases at the maximum rate of rise. The dip in the output voltage is a result of the characteristics of the *LC* filter. The load is connected across the filter capacitor and a sudden change in load will discharge the capacitor before the current through the filter inductor can respond. However, the controller corrects the dip no overshoot.

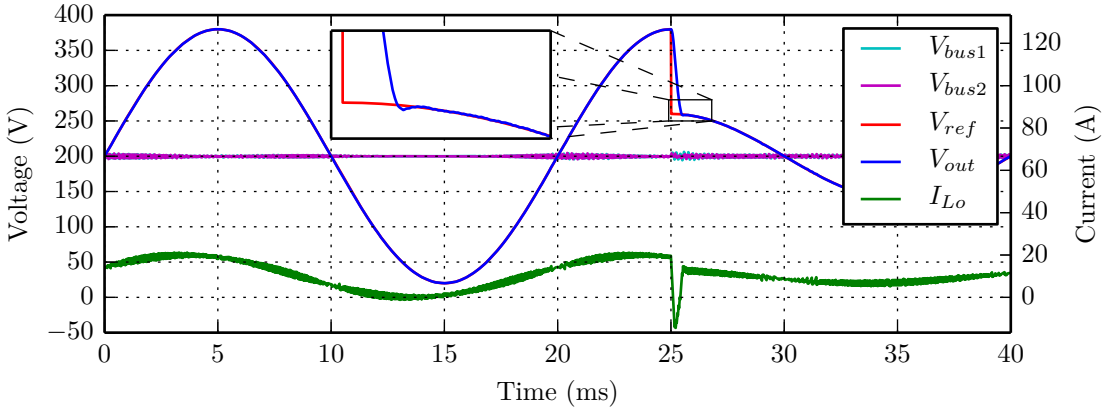
Likewise the results of a decreasing load step in Figure 4.11b shows that when the resistive load is stepped from 7.5 Ω to 20 Ω, the output voltage has a sudden spike. This is attributed to the fact that the current through the filter inductor cannot change instantaneously, which results in a voltage overshoot across the filter capacitor. If the load had inductive reactance, this effect would not be that dramatic. This confirms that controller reacts quickly for an increasing and decreasing load step change.

### Input voltage step

The AC-to-AC converter module is used as a voltage regulator and should react to changes at the input side as well as load changes. An input voltage step is simulated to verify the system's response to a change at the input side. The simulation is set up with a sinusoidal




(a) Reference step up from 30 % to 90 %



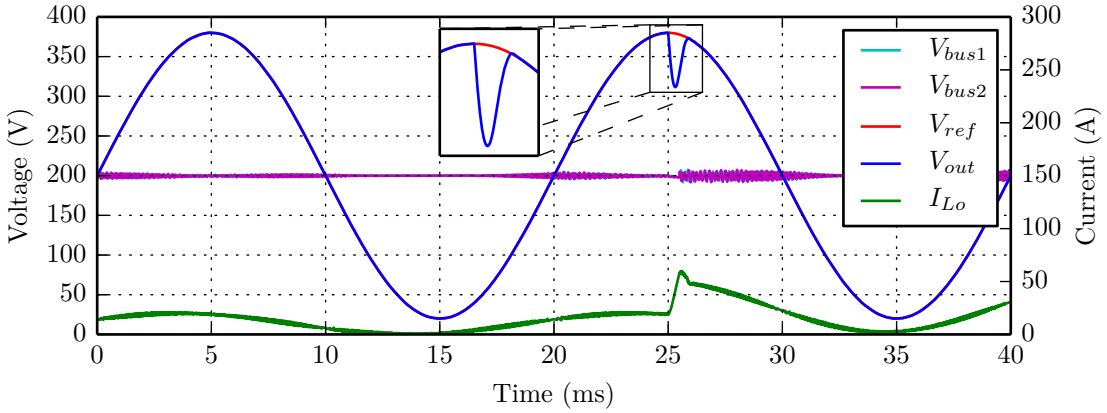

(b) Reference step down from 90 % to 30 %

Figure 4.10: DC-to-AC simulation results for output voltage reference steps with a prediction horizon of 3.

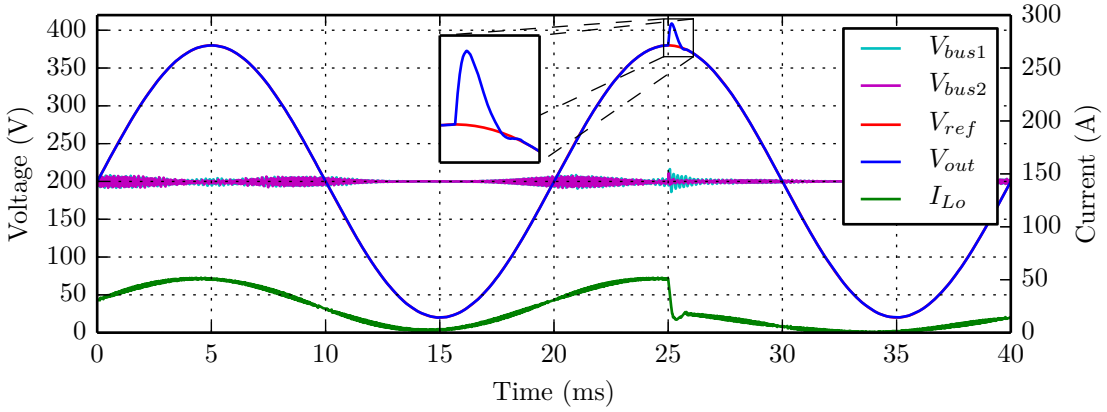
voltage reference at a 90 %, a resistive load of 20 Ω and DC-bus step change from 200 V to 250 V. In Figure 4.12, the results show that no change in the output voltage is observed when the input voltage is stepped.

### Effects of measurement noise

The controller evaluates the system at 400 kHz, which increases susceptibility to noise. To evaluate the effects of noise on the controller, the control is evaluated by adding white Gaussian noise to the measurements with a given signal-to-noise ration (SNR). The simulation is done using the same parameters at the steady state evaluation. A graph indicating the THD and RMS tracking error of the output voltage versus the SNR of the measurement signals is shown in Figure 4.13. When the SNR is above 50 dB, the noise has negligible effect on the controller. However, when the SNR goes below 50 dB, the THD and RMS tracking error of the output voltage begin to deteriorate. This shows that if sufficient care is taken when designing the measurement hardware, the higher sampling frequency would not be severely affected by noise.




(a) Load step up from 20 Ω to 7.5 Ω




(b) Load step down from 7.5 Ω to 20 Ω

Figure 4.11: DC-to-AC simulation results for load steps with a prediction horizon of 3.

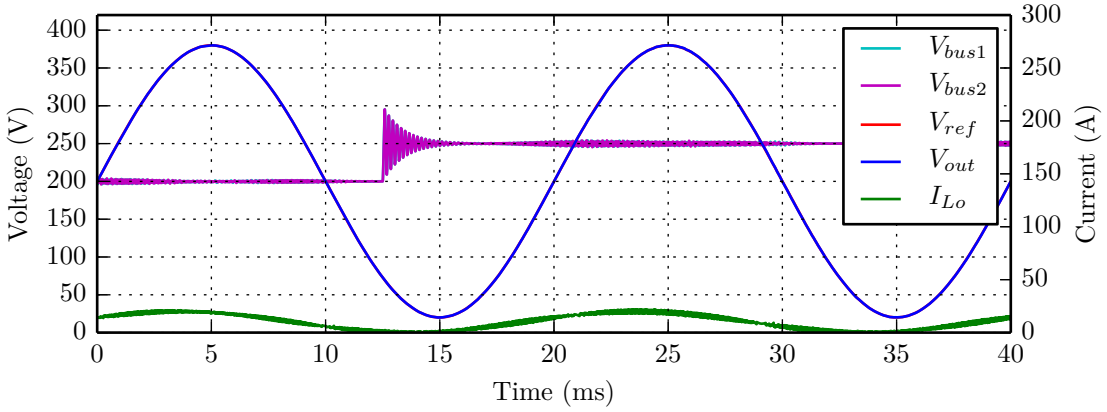



Figure 4.12: DC-to-AC simulation results for an input voltage step with a prediction horizon of 3.

### Switching Pulses

The resulting switching pulses of the proposed FCS-MPC method is evaluated by a DC-to-DC simulation with a 200 V input voltage. The switching pulses that are generated by the controller is similar to the expected switching pulses of Regular Sampled PWM. However, the FCS-MPC method allows flexibility and the resulting pulses are not necessarily centred perfectly around the beginning of each switching period. In Figure 4.14a, the output

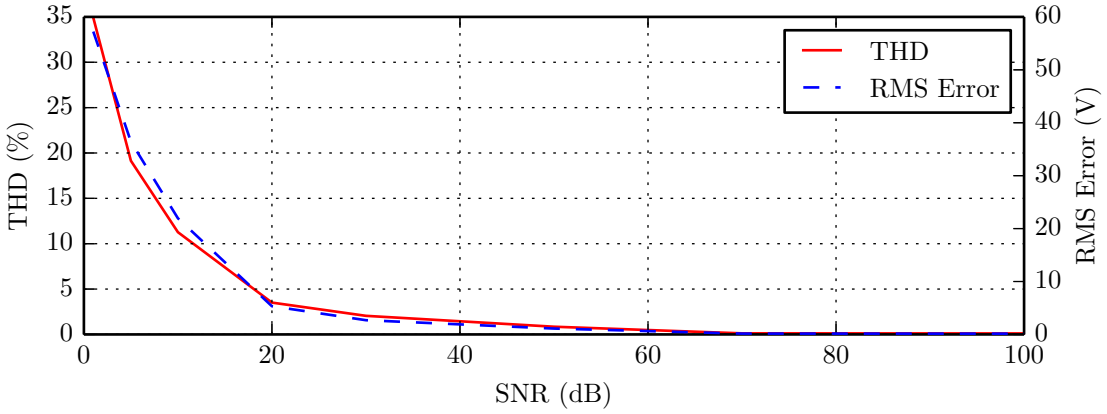
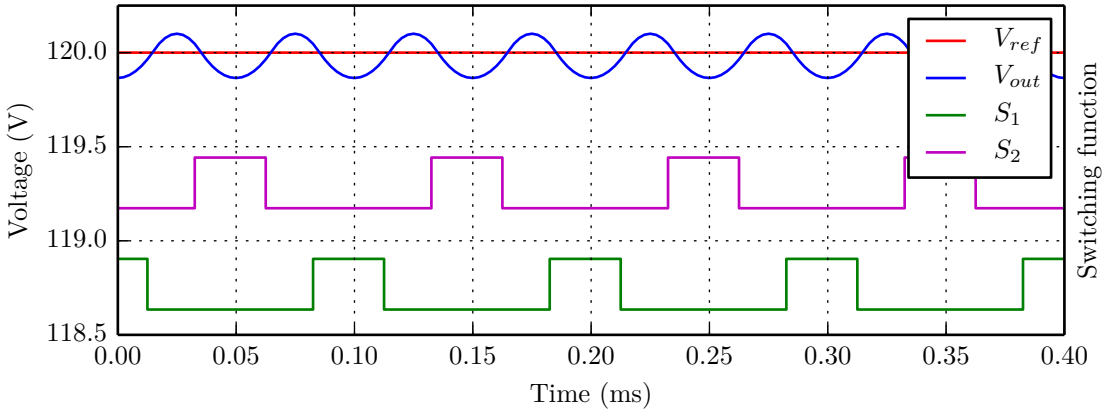
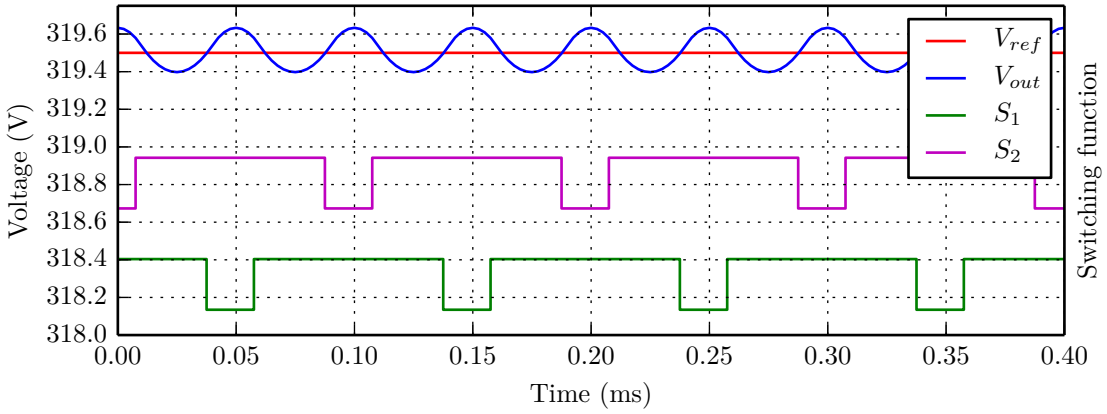



Figure 4.13: Influence of unfiltered measurement noise with a DC-to-AC simulation.




(a) Reference at 30 %




(b) Reference at 80 %

Figure 4.14: 10 kHz switching pulses for a DC-to-DC simulation.

voltage reference is set at 60 V, which is 30 % of the input voltage. The pulses are evenly distributed and resembles the expected switching pattern of PWM at a duty cycle of 0.3. If the reference is increased, as shown in Figure 4.14b, the pulse width increases, but remains approximately centred around the beginning of each switching period. This confirms the expected behaviour of the proposed prediction method.

### 4.4.3 Simulation results for an AC-to-AC configuration

In the previous section DC-to-AC simulations are presented to evaluate the controller's response without the effects of an AC voltage source. In this section an AC-to-AC simulation is performed to evaluate the response of the controller when the converter is driven from an AC source. This requires the control of the output voltage $V_{out}$ as well as the resonant suppression of the input currents $I_{Leq1}$ and $I_{Leq2}$. The controller is evaluated for steady state operation, reference step response, load step response and an input voltage step. A sampling rate of 400 kHz is used with a switching frequency of 10 kHz. A summary of the component values and parameters that are used for the simulation is given in Table 4.2.

#### Steady state

The simulation results for the output voltage during steady state operation is shown in Figure 4.15. The output voltage is given a 50 Hz sine wave as reference and a 25 Ω resistive load.

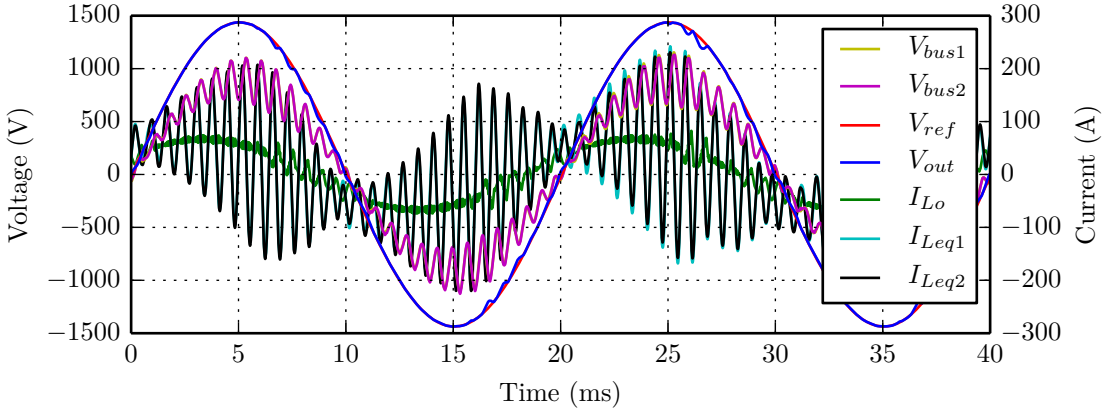
In Figure 4.15a it is shown than when the input filter resonance is not suppressed the input currents and bus voltages resonate severely which degrades the output voltage. Figure 4.15b shows that when damping is applied the resonance is suppressed and the output voltage waveform is improved. The results show that with resonance damping the output voltage tracks the reference with a THD of 0.13 %, a tracking phase error of 0.034° and an amplitude error of -1.5 V. The output voltage has a peak reference of 1437 V which results in an amplitude error of 0.001 %.

The frequency spectrum of the steady state waveform is shown in Figure 4.15c. The two converter module's switching patterns are interleaved which results in a 20 kHz switching frequency at the output filter which is clearly visible on the FFT. As with the DC-to-AC simulation, the FFT of the AC-to-AC simulation shows a raised noise floor at the lower frequencies. This is attributed the use of a binary prediction tree which eliminates some prediction choices together with quantisation noise caused by the discrete sampling of the controller.

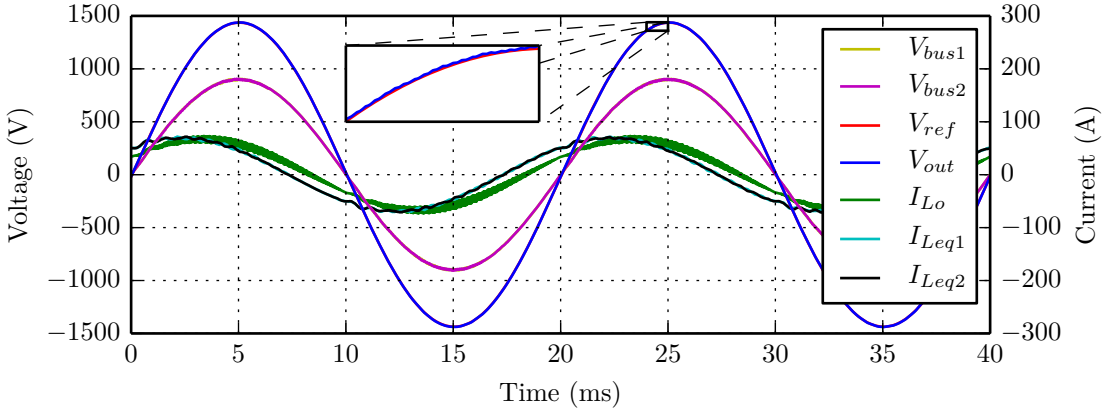
#### Output voltage reference step

Simulation results for the response of a reference step-up from 40 % to 70 % is shown in Figure 4.16. The output filter consists of a second order output filter and with linear controllers, a double loop strategy is usually followed by controlling the inductor current with a faster inner loop and the capacitor voltage with the slower outer loop.

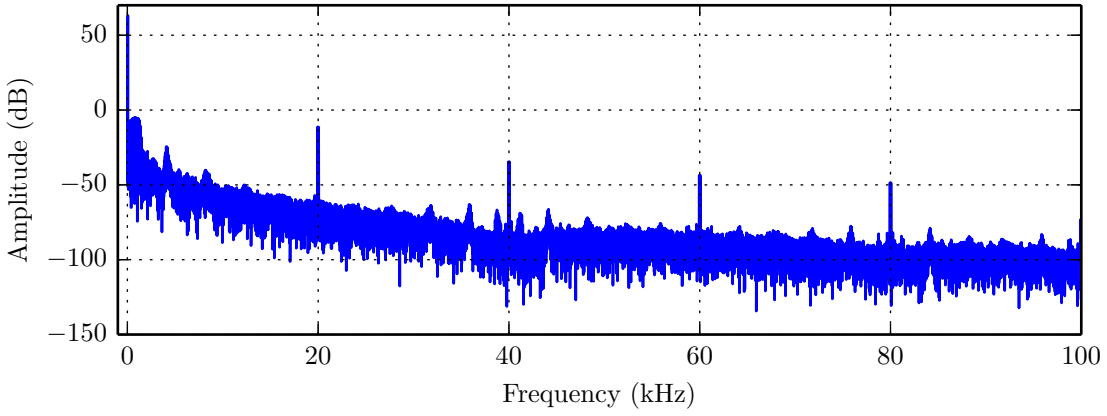
The FCS-MPC controller on the other hand only controls the output voltage but takes into account the future behaviour of the voltage based on a model that includes the




(a) Voltage reference at 80 % without input resonance damping




(b) Voltage reference at 80 % with input resonance damping. (THD: 0.13 %, Phase error: 0.034°, Amplitude error: -1.5 V)




(c) Frequency spectrum of the steady state waveform

Figure 4.15: AC-to-AC simulation results for steady state conditions at a fixed switching frequency of 10 kHz and a prediction horizon of 3

behaviour of the inductor. In order to take the behaviour of the second order filter into account the prediction horizon should be long enough to observe the filter dynamics.

To illustrate the effects of the prediction horizon length the simulation is repeated for a horizon of 1 and of 6. In Figure 4.16a it is shown that when a horizon of 1 is used, the predictions does not effectively take the dynamics of $LC$ filter into account which leads to overshoot and ringing. In Figure 4.16b it is shown that when the prediction horizon is increased to 6, the overshoot and ringing is significantly reduced.

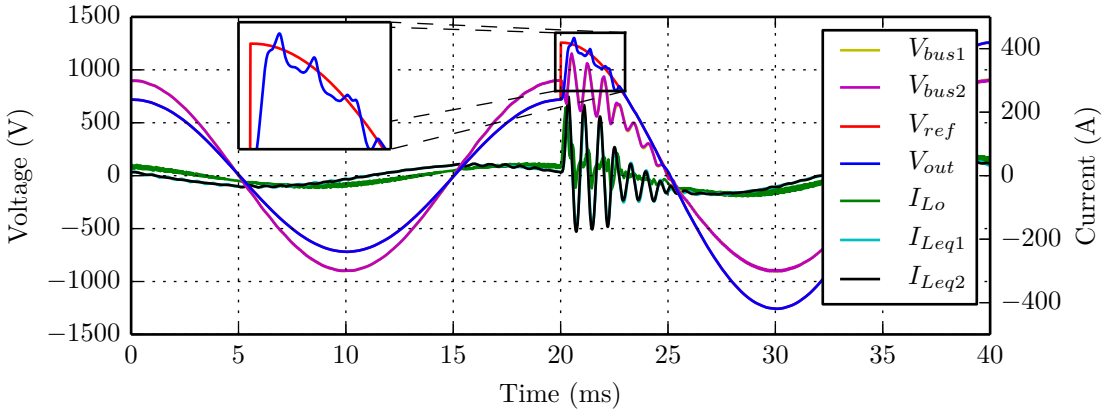
The same behaviour can be observed for a reference step down as shown in Figures 4.16c and 4.16d where the reference is stepped from 70 % to 40 %.

### Load step

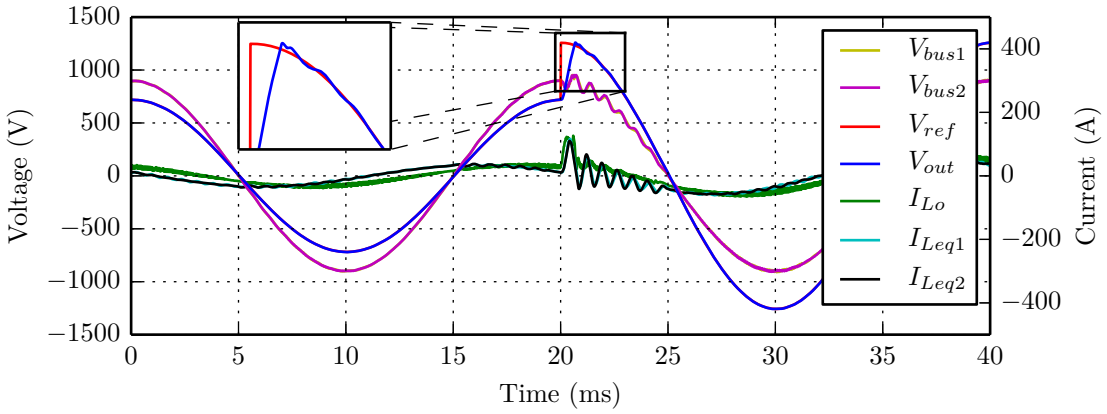
The controller's response to a load step is evaluated and the results are given in Figure 4.17. At 17.5 ms, a load step-up is simulated from 100 Ω to 20 Ω as shown in Figure 4.17a. The output voltage shows a negligible disturbance while the filter inductor current increases at the maximum rate of rise. The controller acts quickly and maintains reference tracking while the inductor current increases. Some ringing at the input bus is observed that dies away as the controller suppresses the resonance. In Figure 4.17b the load is stepped down from 20 Ω to 100 Ω while maintaining reference tracking of the output voltage without significant disturbance. The results show that the controller is able to act quickly to load changes without significant effects on the output voltage waveform.

### Input voltage step

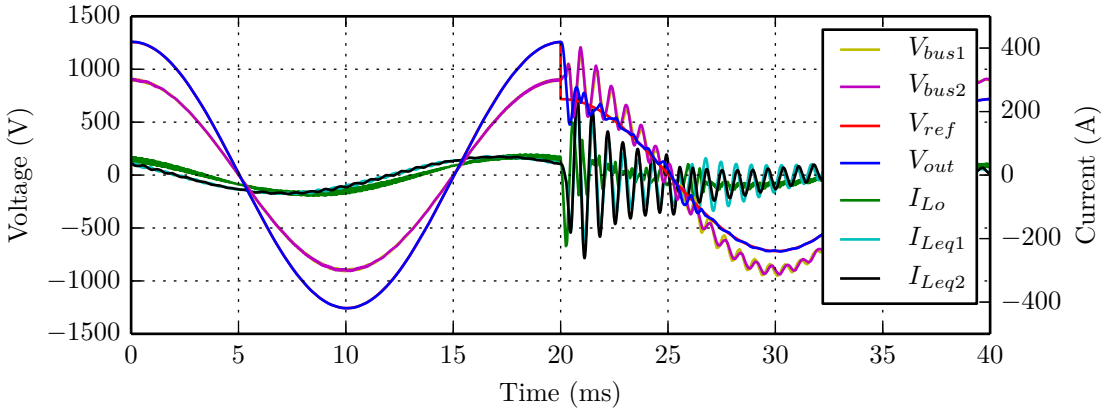
The AC-to-AC converter is used as a voltage regulator and should respond to changes at both the input and output. Figure 4.18a shows the simulation results where the input voltage is stepped up by 10 %. As the input voltage is stepped up, the bus voltage steps with some ringing as a results of the under-damped input $LC$ filter. The resonance at the input bus causes a small disturbance on the output voltage, but, the controller is effective damping the resonance and maintaining reference tracking. Similar results are observed for an input voltage step down as shown in Figure 4.18b.



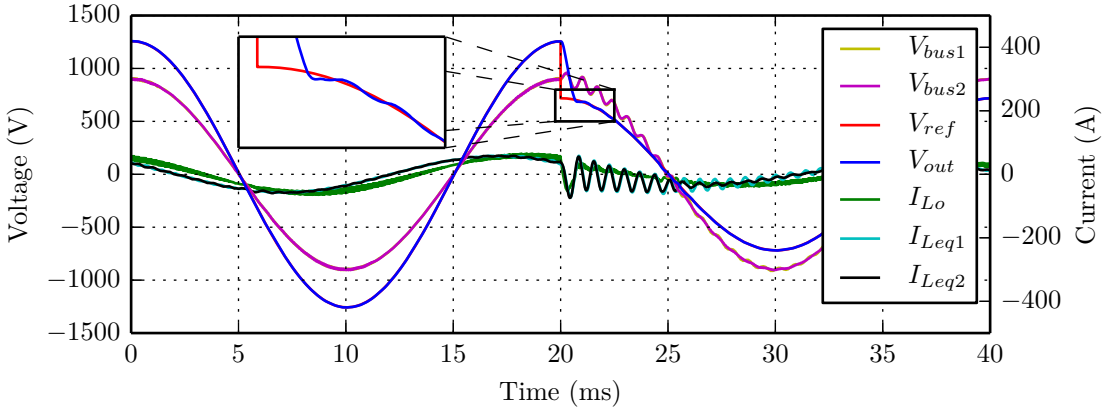

(a) 40 % to 70 % reference step with a prediction horizon of 1




(b) 40 % to 70 % reference step with a prediction horizon of 6

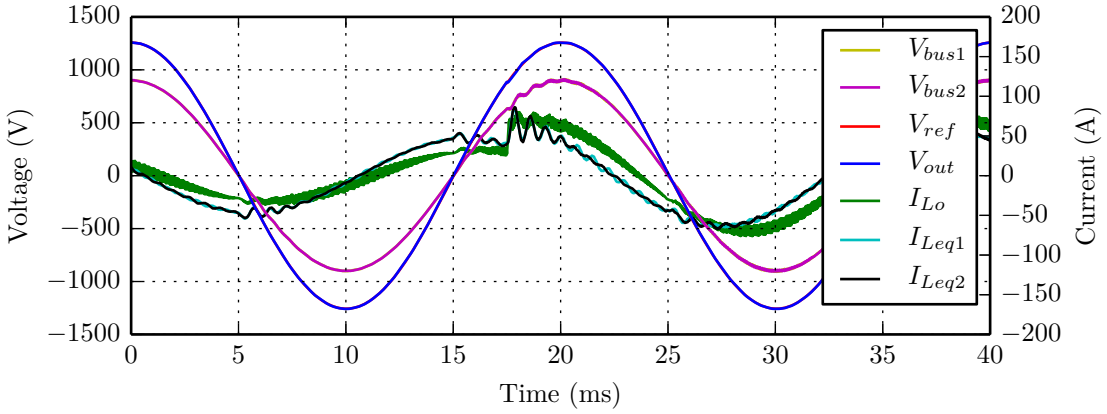



(c) 70 % to 40 % reference step with a prediction horizon of 1

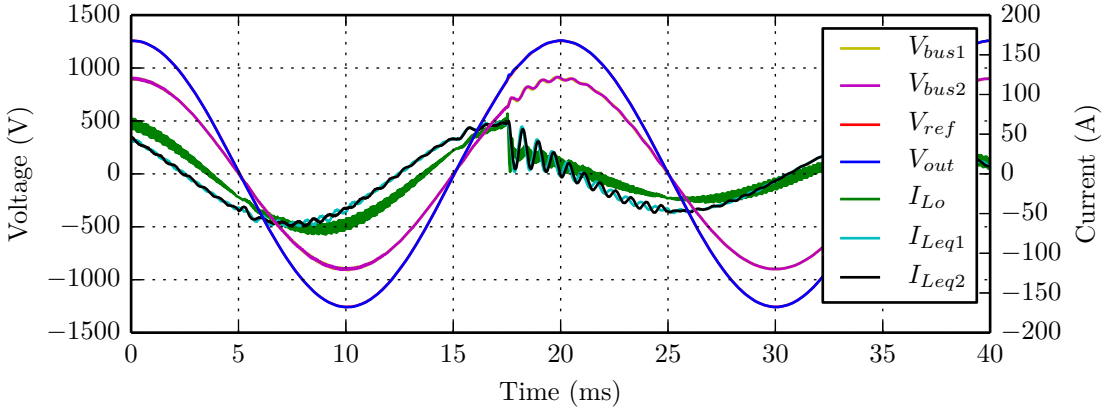



(d) 70 % to 40 % reference step with a prediction horizon of 6

Figure 4.16: AC-to-AC simulation results for output voltage reference steps




(a) Load step up from 100 Ω to 20 Ω




(b) Load step down from 20 Ω to 100 Ω

Figure 4.17: AC-to-AC simulation results for a load step

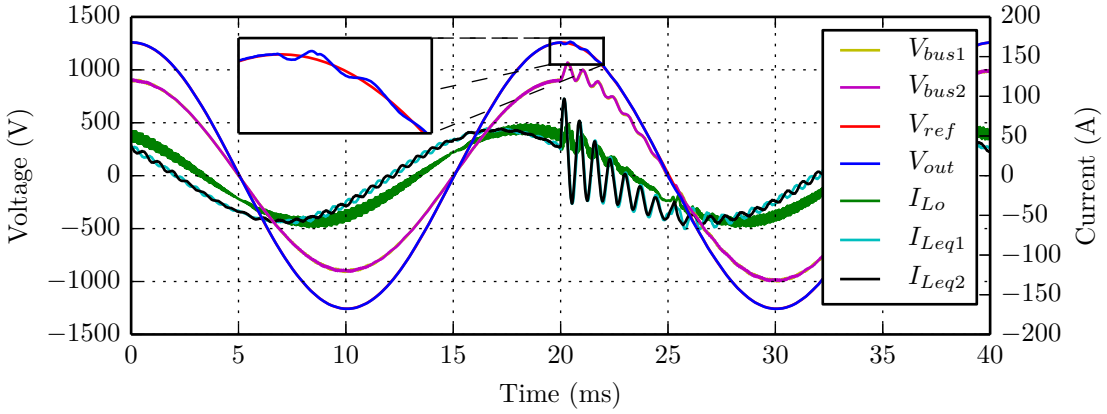
### 4.4.4 Conclusion of simulation results

The controller is shown to have a good steady state sinusoidal reference tracking performance with both a DC input and AC input. The FFT clearly shows the fixed interleaved switching frequency at 20 kHz with its multiples at 40 kHz, 60 kHz and 80 kHz. It was shown that at the lower frequency spectrum there is a raised noise floor that can be attributed to quantisation noise and the use of a binary prediction tree instead of a ternary tree. Even with the raised noise floor the controller kept a low THD with a small phase and amplitude error.

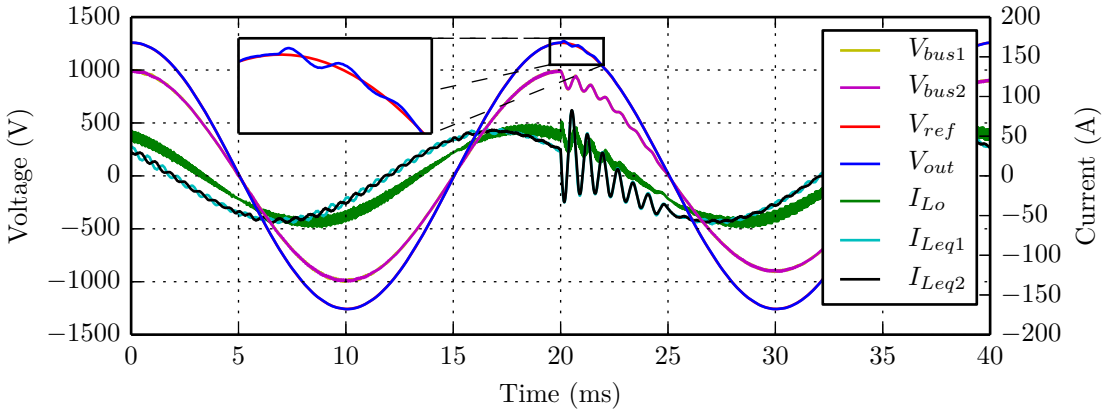
With the AC input bus, it was shown that when the input current resonance is not suppressed, significant resonance occurs which dramatically degrades the waveform quality of the output voltage.

Results for an output voltage reference step showed that when a prediction horizon of one is used the controller reacts with overshoot and ringing. It was further shown that by increasing the prediction horizon, the controller is able to better anticipate the dynamics of the plant and minimize overshoot and ringing.

The controller showed to have a fast reaction to load step changes and is able to maintain reference tracking. In the case where the load step exceeds the $LC$ filter's rate




(a) Input voltage step up by 10 %




(b) Input voltage step down by 10 %

Figure 4.18: AC-to-AC simulation results for input voltage step changes

of change, the controller reacts quickly to bring the output voltage back to the reference with negligible overshoot and ringing.

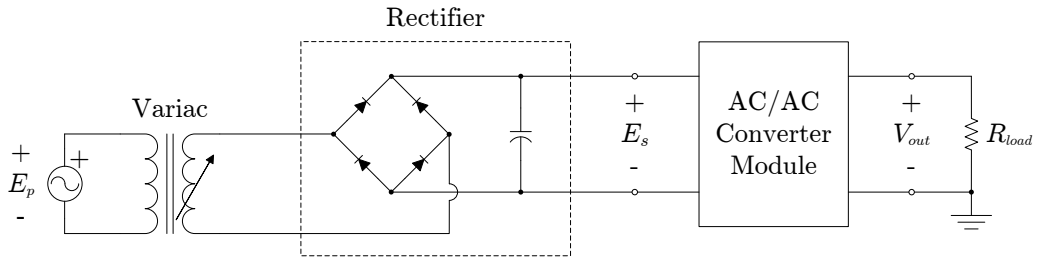
The effect of measurement noise on the controller was evaluated by adding White Gaussian Noise to the unfiltered state variables. It was shown that when the SNR is above 50 dB, the noise has a negligible effect on the controller. When the SNR goes below 50 dB, the THD and RMS tracking error begins to deteriorate. This showed that if sufficient care is taken with the design of the measurement hardware, measurement noise should not be a problem for a practical system.

## 4.5 Experimental verification and results

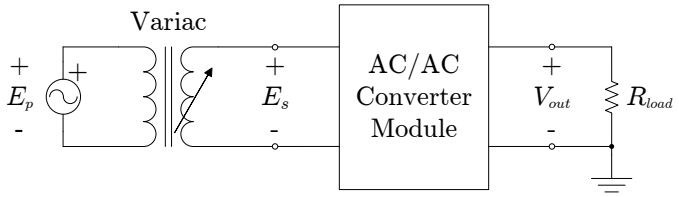
### 4.5.1 Overview

This section presents the verification of the FCS-MPC control method with a fixed switching frequency through experimental measurements. The controller is experimentally evaluated on one AC-to-AC converter module for a DC input bus and AC input bus respectively.

The proposed FCS-MPC control method with a prediction horizon of one switching period is tested on one AC-to-AC converter module according to the experimental set-up in Figure 4.19. The control is implemented with a switching frequency of 10 kHz and a sampling frequency of 400 kHz, which allows 40 evaluations per switching period. Control is only applied to the output voltage and no stabilization of the input bus is performed.

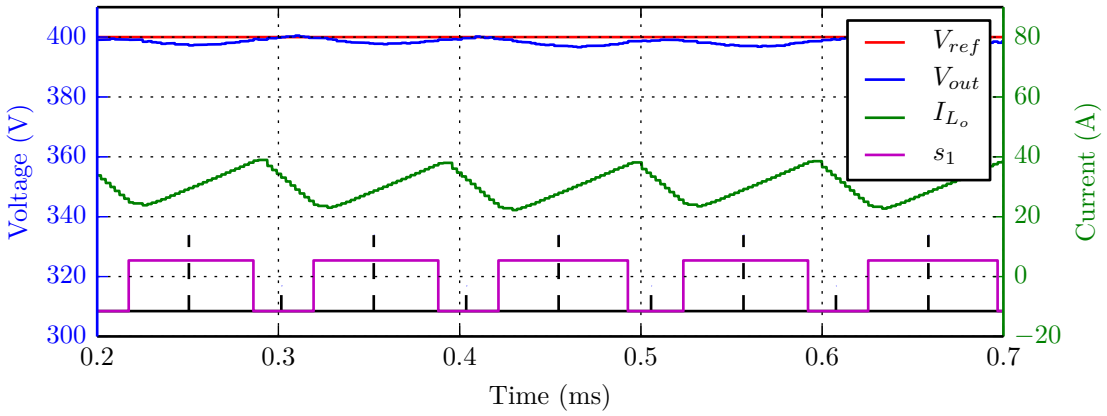



(a) DC-to-AC control test configuration

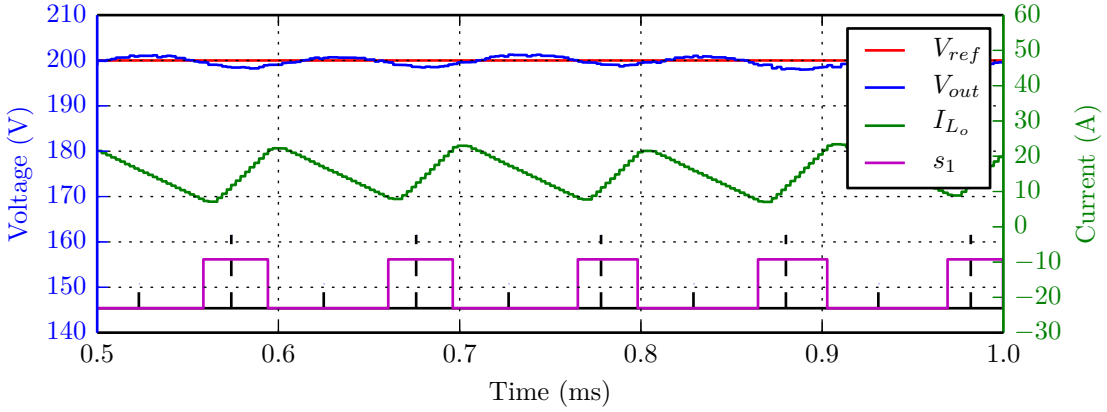



(b) AC-to-AC control test configuration

Figure 4.19: AC-to-AC converter hardware configurations used for the controller tests.




(a) Reference voltage at 400 V




(b) Reference voltage at 200 V

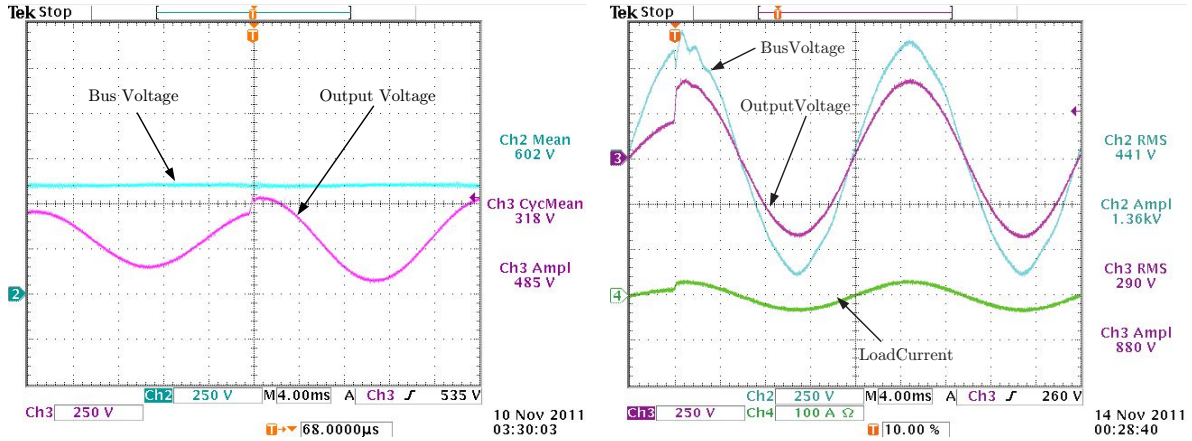
Figure 4.20: Experimental measurements of the switching pattern, output voltage and inductor current. The measurements are directly read from the FPGA with Altera® Signal Tap.

### 4.5.2 Results: One AC-to-AC converter module

#### Switching Pulses

The switching pattern was evaluated by using the DC-to-DC test set-up. The controller's variables were captured in real time from the FPGA by using Altera® Signal Tap software. The data of the switching pulses, switching period, inductor current, output voltage and output reference is presented in Figure 4.20. In Figure 4.20a the output voltage is tracking a 400 V reference. The switching waveform displays the expected pulse width and follows a fixed switching frequency. The pulses naturally centre around the beginning of each switching period but are allowed freedom to shift as needed. The results for a reference at 200 V are shown in Figure 4.20b. The width of the pulses is reduced and they remain centred around the beginning of each period.

These experimental results confirm the expected behaviour shown for the ideal simulation results in Figure 4.14. This confirms that the control algorithm is able to enforce a fixed switching frequency on a practical system and maintain good reference tracking.




(a) DC-to-AC reference step

(b) AC-to-AC reference step

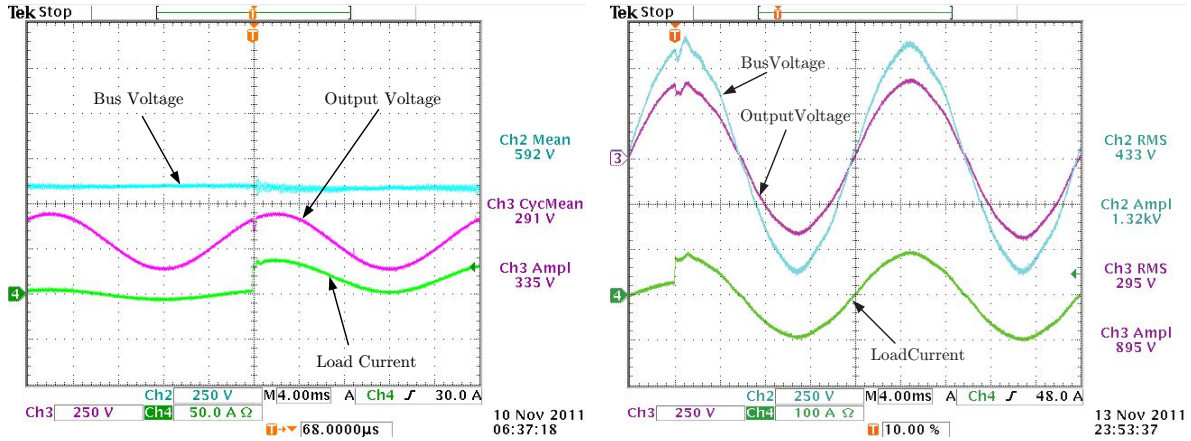
Figure 4.21: Practical measurements of an output voltage reference step for one AC-to-AC converter module

### Reference Step

In Figure 4.21a, the controller's response to a reference step for a DC-to-AC configuration is presented and confirms the simulation results shown in Figure 4.10a. It is shown that the output voltage quickly steps to the new reference without significant transient effects. In Figure 4.21b the reference step is tested for an AC-to-AC configuration. As the reference is stepped, the output voltage quickly steps to the new reference. However, some transient effects are visible with some overshoot and ringing on the input bus voltage. This can be attributed to the fact that a prediction horizon of only one is used together with the fact that the input voltage includes the third, 7th and 9th harmonics while the output voltage is tracking a 50 Hz sine wave. The input bus is therefore under-damped with respect to the harmonics, which causes some ringing during transient effects. The experimental results compare well to the expected simulation results in Figure 4.16b. The simulation results show that when the prediction horizon is increased, the transient effects can be anticipated and corrected.

### Load Step

The practical measurements of a load step for a DC-to-AC configuration is shown in Figure 4.22. The response to a load step corresponds to the expected behaviour of the simulations in Figures 4.11 and 4.17. At the point where the load step is applied, the output voltage drops, but recovers quickly as the current through the filter inductor rises. This shows that the controller is able to maintain tracking for different load conditions. The response to a load step for an AC-to-AC configuration is shown in Figure 4.22b. At the point where the load is stepped, the output voltage drops and recovers as the current through the filter inductor increases. Some transient effects are visible on the bus voltage, which could be suppressed by adding control of the bus voltage to the cost function.




(a) DC-to-AC load step

(b) AC-to-AC load step

Figure 4.22: Practical measurements of a load step for one AC-to-AC converter module

These results show that the controller is able to maintain tracking during dynamic load conditions.

### 4.5.3 Conclusion of experimental results

This section presented the experimental measurement results of the fixed switching frequency FCS-MPC control algorithm on the voltage regulator hardware. The controller was implemented and tested on one AC-to-AC converter module and proved to be effective. However, it was shown that the prediction horizon can be increased and further control can be added to the cost function to stabilise the input bus voltage during transient conditions. The results conclude that the proposed control method is successful in achieving the desired objectives and compared well to the expected simulation results in Chapter 4.4.

## 4.6 Summary

This chapter presented the design overview of a medium voltage electronic voltage regulator and the design of an accompanying controller by using the FCS-MPC method with a fixed switching frequency.

The controller was extensively evaluated through simulation and verified by experimental measurements. It was shown that the controller meets the expected design criteria and proved to be effective. A detailed summary is given at the end of each section in this chapter.

# Chapter 5

# Control of a five-level flying capacitor converter

## 5.1 Introduction

In this chapter the FCS-MPC method with a fixed switching frequency is evaluated for the voltage control and capacitor balancing of a five-level flying-capacitor converter with an $LC$ output filter. The flying-capacitor converter is chosen for the difficulty of actively balancing its capacitor voltages with conventional linear control methods. Using FCS-MPC, it will be shown that output voltage reference tracking with a low THD waveform can be obtained while actively controlling the flying capacitor voltages.

An overview of the converter topology is discussed in Section 5.2 and the prediction models are derived in Appendix C.2. The controller scheme and design is presented in Section 5.3 and the expected behaviour under ideal conditions are evaluated by simulation in Section 5.4. Lastly, the expected simulation results are confirmed by experimental measurements in Section 5.5.

## 5.2 Flying-capacitor converter topology

The schematic diagram of the flying-capacitor converter topology is shown in Figure 5.1. The converter consists of four pairs of power electronic switches $T_1, T_2, T_3$ and $T_4$, where each pair is switched in complimentary with $\bar{T}_1, \bar{T}_2, \bar{T}_3$ and $\bar{T}_4$. To allow individual control of the flying capacitors the four switching pairs are switched independently, which corresponds to PWM with four carriers. The converter has a second-order $LC$ output filter and drives a resistive load. The component values used in the simulation are given in Table 5.1.

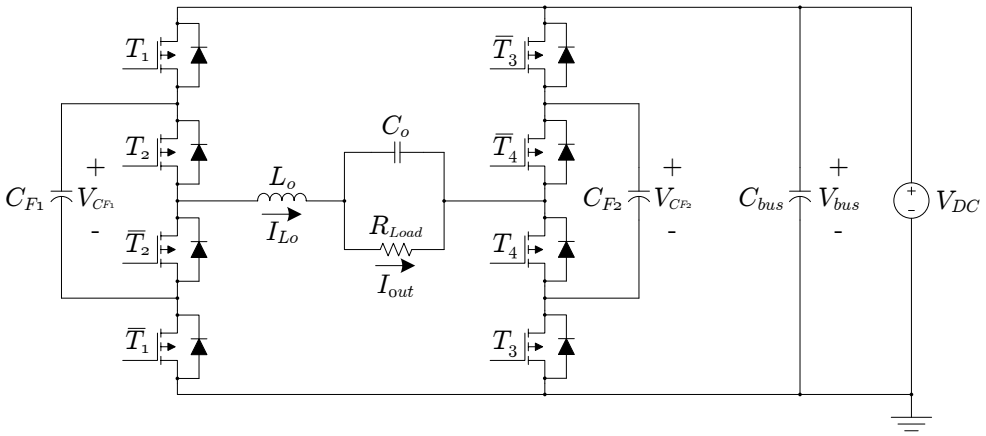



Figure 5.1: Schematic diagram of the flying capacitor converter.

Table 5.1: Approximate measured flying-capacitor converter component values.

| Component | Value | Component | Value |
|---|---|---|---|
| $V_{dc}$ | 60 V | $R_{Load}$ | var |
| $L_o$ | 3 mH | $R_{L_o}$ | 3 mΩ |
| $C_o$ | 15 $\mu$F | $R_{C_o}$ | 1.5 mΩ |
| $C_{F1}$ | 300 $\mu$F | $R_{C_{F1}}$ | 1.5 mΩ |
| $C_{F2}$ | 300 $\mu$F | $R_{C_{F2}}$ | 1.5 mΩ |
| $C_{bus}$ | n/a | $R_{b2}$ | 10 MΩ |
| – | – | $R_{b1}$ | 10 MΩ |

## 5.3 Controller design: FCS-MPC

### 5.3.1 Plant model and control objectives

For the purpose of calculating the predictions, the converter topology can be modelled to include the equivalent series resistor (ESR) of the capacitors and inductors. However, to allow the off-line solvers to converge a parasitic or bleeding resistor $R_b$ is added in parallel to each flying capacitor.

The input DC voltage and the bus capacitor can be assumed to act as an ideal DC voltage source $V_{DC}$ and can be modelled as a single DC voltage source $V_{DC}$.

The unknown load impedance can be modelled as an unknown current source where the dynamic behaviour is assumed to follow a first-order Euler extrapolation as discussed in Chapter 3.3.3.

The state vector is given by

$$\begin{aligned}\mathbf{x} &= \begin{bmatrix} x_0 & x_1 & x_2 & x_3 & x_4 \end{bmatrix}^\top \\ &= \begin{bmatrix} I_{L_o} & V_{out} & V_{C_{F1}} & V_{C_{F2}} & I_{load} \end{bmatrix}^\top . \end{aligned} \tag{5.1}$$

where $I_{L_o}$ is the filter inductor current, $V_{out}$ is the output voltage, $V_{C_{F1}}$ and $V_{C_{F2}}$ are the flying capacitor voltages and $I_{load}$ is the load current. The plant input is given by $V_{DC}$.

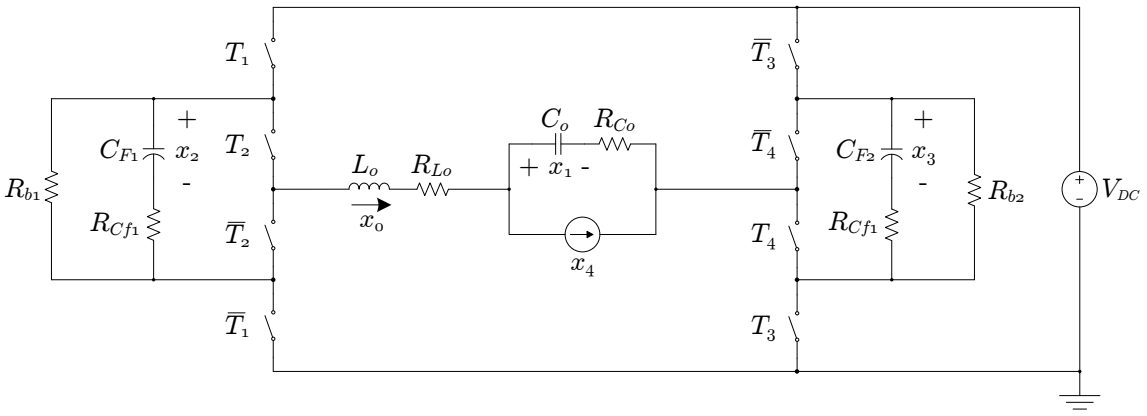



Figure 5.2: Flying-capacitor converter prediction model.

**Control objectives**

The primary control objective is to control the output voltage by tracking a 50 Hz sinusoidal reference signal. In addition to that, the controller must actively balance the flying capacitor voltages to half the bus voltage.

For the purpose of voltage control, the output voltage waveform should have a low THD, a fast response to reference step changes as well as to load step changes.

## 5.3.2 Controller design

### 5.3.2.1 Controller scheme

The controller follows the same control scheme as for the medium-voltage regulator in Chapter 4.3.2.1. The control scheme with a fixed switching frequency is implemented according to the control block diagram in Figure 3.17b which makes use of a state observer to estimate the unmeasured state variables.

The off-line calculations are done by using Python together with the Numpy and SymPy libraries. The on-line controller is implemented on an FPGA with a clock frequency of 20 MHz according to the state flow diagram in Figure 3.21.

### 5.3.2.2 Control references

**Output voltage**

The output reference voltage $V^*_{out}$ can be realised by a sinusoidal function generator of the form

$$V^*_{load}(t) = A\sin(\omega t + \Phi) \tag{5.2}$$

where $A$ is the reference amplitude, $\omega$ is the measured network frequency in rad/$s$, $\Phi$ is the phase shift to account for the average predicted value across the switching period. The control reference is recalculated and updated on-line at every sampling instance.

**Capacitor voltage balancing**

The flying capacitor voltages should be kept at half the bus voltage. The control references can be obtained by passing the measured bus voltages through a first order low-pass filter and taking half of the result. For the purpose of removing the switching ripple from the bus voltage, a LPF with a cut-off frequency $f_c$ of 500 Hz is sufficient. Since the ideal bus voltage should only contain a DC component, the phase shift introduced by the filter has no impact.

The discrete-time implementation of a first-order $RC$ LPF [85] produces the exponentially-weighted average of the input and is realised by the equation

$$y(k) = \alpha x(k) + (1-\alpha)y(k-1) \tag{5.3}$$

where $x(k)$ is the present filter input, $y(k)$ is the present filter output, $y(k-1)$ is the previous filter output and $\alpha$ is the filter coefficient. The filter coefficient, as a function of the sampling period $T_s$ and cut-off frequency $f_c$, is given by

$$\alpha = \frac{2\pi f_c T_s}{1 + 2\pi f_c T_s}. \tag{5.4}$$

By using (5.3), the filtered bus voltage is calculated with

$$\overline{V_{DC}}(k) = \alpha V_{DC}(k) + (1-\alpha)\overline{V_{DC}}(k-1) \tag{5.5}$$

and the control reference of the two flying-capacitor voltages is obtained as

$$V^*_{C_F}(k) = 0.5\overline{V_{DC}}(k). \tag{5.6}$$

#### 5.3.2.3 Cost function

The control of the output voltage $V_{out}$ and the balancing of the flying-capacitor voltages $V_{C_{F1}}$ and $V_{C_{F2}}$ can be implemented as a reference tracking problem in the same way as for the medium voltage regulator in Chapter 4.3.2.3. The control objective for reference tracking is to minimize the error between the reference signal and the controlled state variable. This can be accomplished by defining a cost function for reference tracking by using the weighted sum of square values method.

In order to anticipate the transient effects during large voltage reference steps and load steps, the prediction horizon can be increased as discussed in Chapter 3.2.3. This is accomplished by defining an error band and increasing the prediction horizon when the error-band threshold $x_{thres}$ is exceeded. The error-band function is used to activate the cost function terms that correspond to the higher prediction horizons, and is defined as

$$f_{err}\big(x_{err}(k)\big) = \begin{cases} 0 & \text{if} \quad |x_{err}(k)| < x_{thres} \\ 1 & \text{if} \quad |x_{err}(k)| \geq x_{thres} \end{cases} \tag{5.7}$$

with

$$x_{err}(k) = x^*(k) - x(k). \tag{5.8}$$

Regardless of the horizon, the error $x_{err}(k)$ is always the difference between the measured state variable $x$ and the desired reference point $x^*$ at the present time instance $k$.

By using the error-band function, the cost function for tracking the output voltage with a prediction horizon of three is written as

$$\begin{aligned} g_{V_{out}} = {} & w_1\left(V^*_{out1} - V^p_{out1(av)}\right)^2 \\ & + w_2\left(V^*_{out2} - V^p_{out2(av)}\right)^2 f_{err}(V_{out(err)}) \\ & + w_3\left(V^*_{out3} - V^p_{out3(av)}\right)^2 f_{err}(V_{out(err)}) \end{aligned} \tag{5.9}$$

The error $V_{err(out)}$ is the difference between the present state variable and reference. It is used to calculate the error function for all the horizon terms beyond the first one.

The state variable $V^p_{out1(av)}$ is the averaged predicted value of the output voltage over the first prediction horizon, $V^p_{out2(av)}$ at the second horizon and $V^p_{our3(av)}$ at the third. Likewise, the references at each horizon step is indicated by $V^*_{out1}, V^*_{out2}$ and $V^*_{out3}$. Note that the horizon is determined for the switching period $T_{sw}$ and not the sampling period $T_s$.

When $V_{out}(k)$ is within the bounds of $V_{thres}$, the system is considered to be in steady state and the terms relating to the higher prediction horizons are zeroed. If the threshold is exceeded, the error functions becomes non-zero and the predictions are made up to the maximum horizon.

The transient effects of the secondary controlled variables, the capacitor voltages, are not as important and a horizon of one is sufficient. The cost function terms for balancing the capacitor voltages is therefore given by

$$g_{V_{CF}} = w_4\left(V^*_{C_{F1}} - V^p_{C_{F1}(av)}\right)^2 + w_5\left(V^*_{C_{F2}} - V^p_{C_{F2}(av)}\right)^2. \tag{5.10}$$

The combined cost function for controlling the output voltage and balancing the flying-capacitor voltages then becomes

$$\begin{aligned} g &= g_{V_{out}} + g_{V_CF} \\ &= w_1\left(V^*_{out1} - V^p_{out1(av)}\right)^2 \\ &+ w_2\left(V^*_{out2} - V^p_{out2(av)}\right)^2 f_{err}(V_{out(err)}) + w_3\left(V^*_{out3} - V^p_{out3(av)}\right)^2 f_{err}(V_{out(err)}) \\ &+ w_4\left(V^*_{C_{F1}} - V^p_{C_{F1}(av)}\right)^2 + w_5\left(V^*_{C_{F2}} - V^p_{C_{F2}(av)}\right)^2 \end{aligned} \tag{5.11}$$

### Weighting factor adjustment

The importance of each term in the cost function is determined by multiplying each term with a weighting factor $w$. This allows the controller to place an emphasis on more important controlled variables and allowing the less important variables to have a lesser impact.

For the design of this controller, the weights of each prediction horizon term of the output voltage $V_{out}$ is taken to be equal such that

$$w_1 = w_2 = w_3 \tag{5.12}$$

and the importance of the two secondary controlled variables are also taken to be equal such that

$$w_4 = w_5. \tag{5.13}$$

The weighting factors are adjusted by selecting an initial value for the primary controlled variable weights $w_1$,$w_2$ and $w_3$ and setting the secondary controlled variable weights $w_4$ and $w_5$ to zero. The weighting factors $w_4$ and $w_5$ are then gradually incremented until the desired response is obtained. The chosen weighting factor selection for the simulation and experimental results is given in the respective sections to follow.

## 5.4 Controller evaluation through simulation

### 5.4.1 Simulation overview

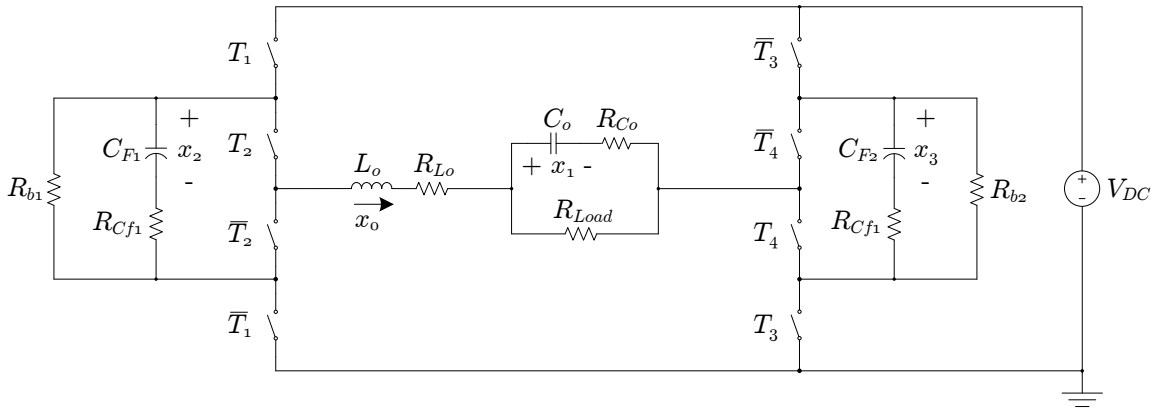



Figure 5.3: Flying-capacitor converter simulation model.

In this section the control of the flying-capacitor converter is evaluated by way of simulation. The purpose of the simulation is to investigate the behaviour of the controller under ideal conditions and to set a benchmark for the experimental measurements. In order to achieve this the real measured component values are used and are listed in Table 5.1.

The simulation consists of two sets of models where each set contains a model for each switching state. The first set of models is used to simulate the physical plant while the second set of models are used for the predictions in the controller. Both sets of models are derived in Appendix C.2. The model for the physical plant is shown in Figure 5.3. The load impedance is modelled as a simple resistive load and the equivalent series resistance of the capacitors and inductors are taken into account. The equivalent parallel leakage or bleeding resistors are also included for the flying capacitors to allow the convergence of the numeric solvers. The parameters used with the FCS-MPC controller is summarised in Table 5.2.

Table 5.2: Flying-capacitor converter controller simulation parameters.

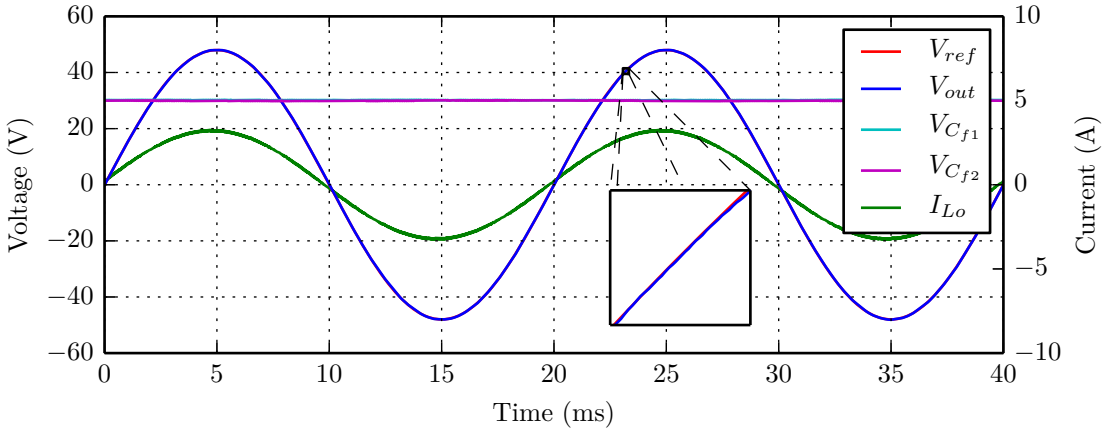
| Control Parameter | Value |
|---|---|
| $F_s$ | 400 kHz |
| $F_{sw}$ | 10 kHz |
| N | 40 steps |
| Horizon | 6 periods |
| $V_{out(err)}$ | 1 V |
| $W_1$, $W_2$, $W_3$ | 1 |
| $W_4$, $W_5$ | 20 |

### 5.4.2 Simulation results

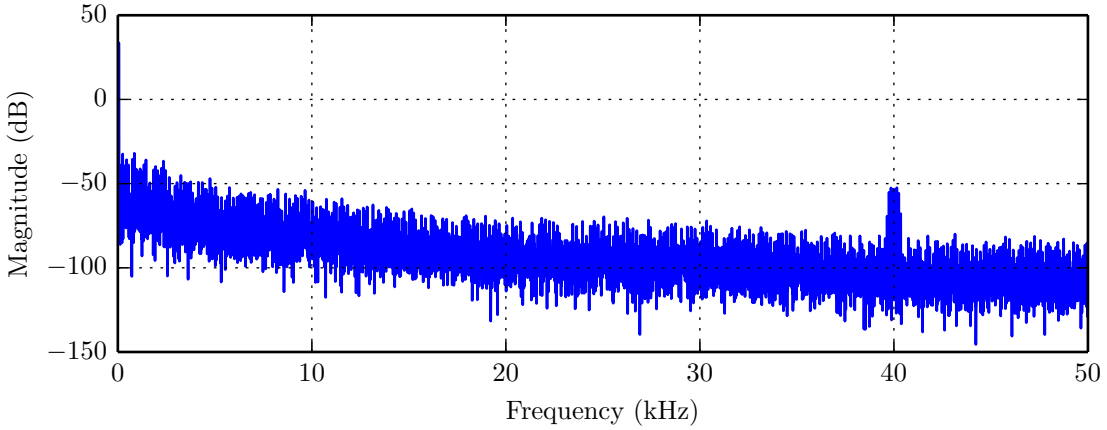
#### Steady state

The simulation results for the output voltage and flying capacitor voltages during steady state is shown in Figure 5.4. The output voltage is given a 50 Hz sinusoidal wave with a 0 V offset and an amplitude that is 80 % of the bus voltage. The flying capacitor voltages are controlled to be 50 % of the input bus voltage and the load is chosen as 15 Ω. The results show that under ideal conditions, the output voltage tracks the reference with an amplitude error of -3.8 mV, a phase error of -0.003° and a THD of 0.15 %.

The FFT plot of the frequency spectrum in Figure 5.4b clearly shows the 10 kHz switching frequency and the resulting 40 kHz component seen at the load as a result of the interleaved switching. At the lower end of the frequency spectrum, a raised noise floor is observed that can be attributed to quantisation noise and the fact that a binary prediction tree is used and not a ternary tree. However, due to the assumptions made about the future behaviour of the pulse widths, a ternary tree would reduce the noise floor but not eliminate it.




(a) Output voltage waveform




(b) Frequency spectrum of the output voltage waveform

Figure 5.4: FCC simulation results for steady state conditions at a fixed switching frequency of 10 kHz. (THD: 0.15 %, Phase Error: -0.003°, Amplitude error: -3.8 mV)

### Balancing the flying capacitor voltages

To show that the controller is not balanced through natural balancing [86], a simulation is set up to force the flying capacitor voltages into a controlled unbalance and back into balance. The simulation results in Figure 5.5 shows that at 45 ms, the two flying-capacitor voltages are forced from balance at 30 V to unbalance at 20 V and 40 V respectively. The capacitor voltages are kept in unbalance at their reference positions until their are actively brought back into balance at 115 ms. During the transient period, a limited degradation of the output voltage waveform is observed, as is expected. This shows that even during transient effects of the secondary controlled variables, control of the primary variable remains satisfactory.

### Output voltage reference step

The controller's response to a sudden reference step change is simulated and the results are shown in Figure 5.6. In Figure 5.6a, the reference is stepped from 30 % up to 80 % with a prediction horizon of 6. It is shown that a small amount of overshoot with an apparent

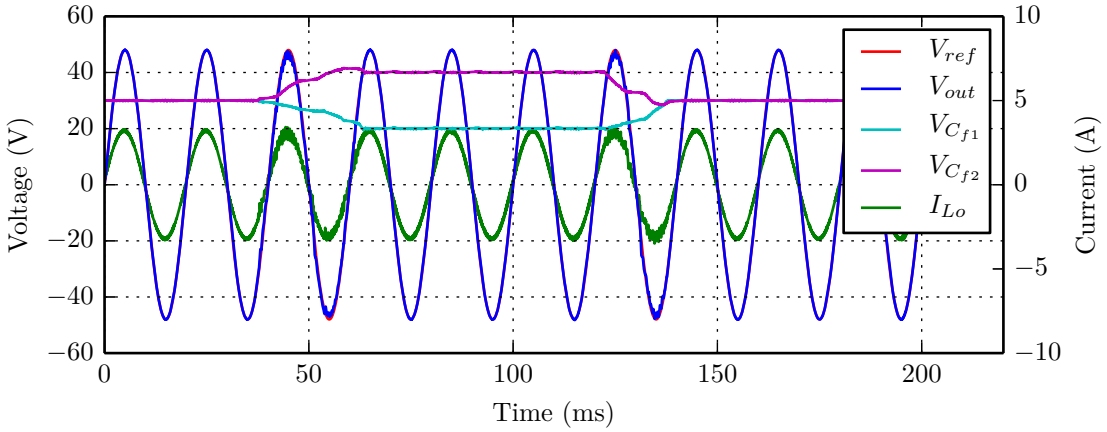
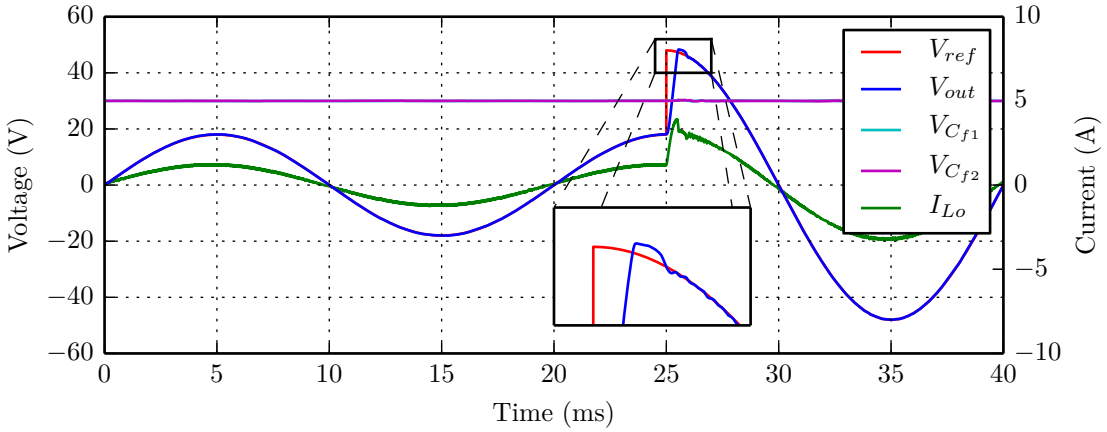


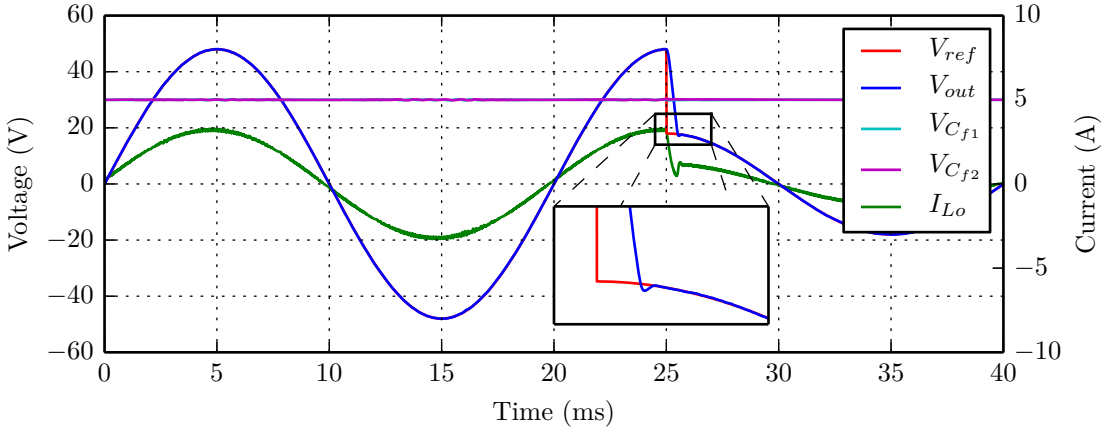

Figure 5.5: FCC simulation results for controlling the flying capacitor voltages.

delay and settling time of 1.5 ms is observed. The apparent delay can be attributed to the control task simultaneously keeping the flying-capacitor voltages in balance.

In Figure 5.6b, the reference is stepped down from 80 % to 30 %. Again, negligible overshoot is observed which settles in less than 1 ms. This shows that the controller is able to react quickly to reference step changes with good transient response.




(a) Reference step up from 30 % to 80 %



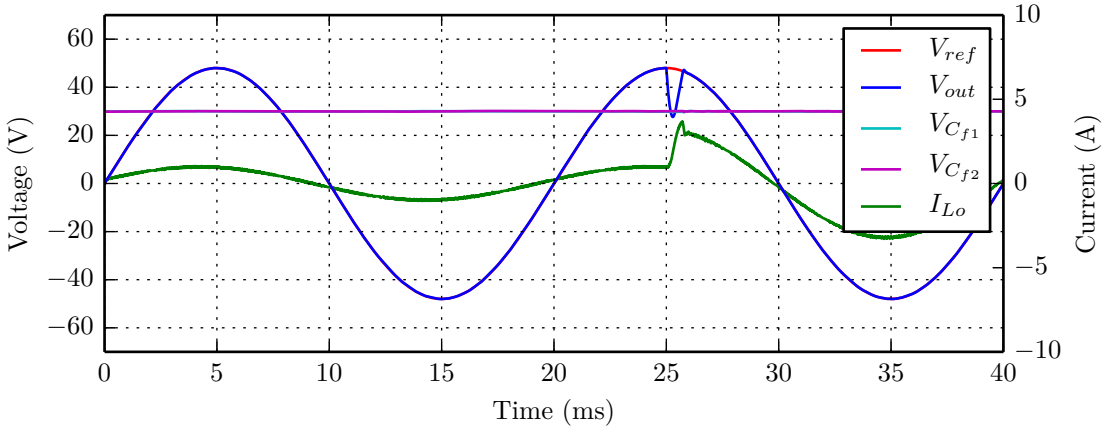

(b) Reference step down from 80 % to 30 %

Figure 5.6: FCC simulation results for output voltage reference steps with a prediction horizon of 6.

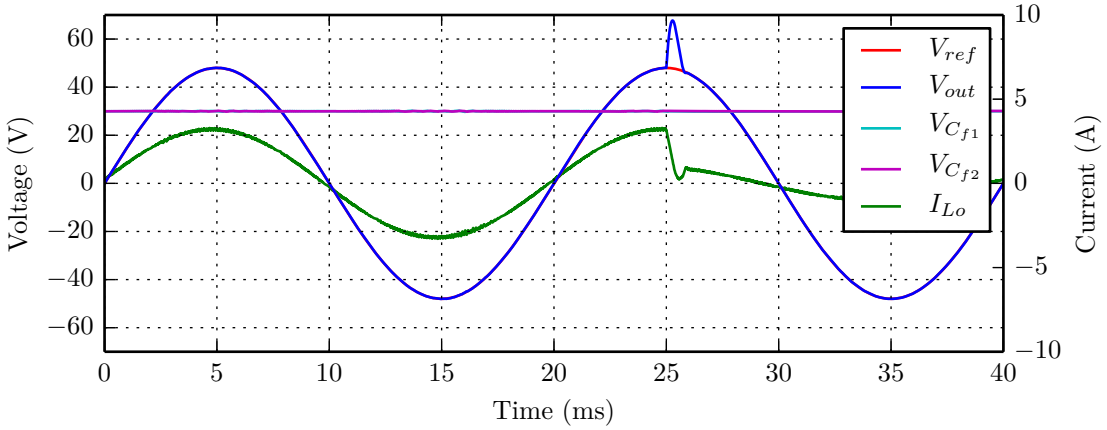
### Load step

The controller's response to loads steps are evaluated by simulating a load step between 50 Ω and 15 Ω. In Figure 5.7a the results of an increasing load step is shown. At the point where the resistive load is stepped the load current changes almost instantly but the filter inductor current cannot. This causes the output voltage droop as the filer inductor current increases. It is shown that after the droop, the output voltage recovers with practically no overshoot or ringing.

The same response is observed in Figure 5.7b where the load is stepped down. The inductor current causes a spike on the output voltage which recovers quickly with no overshoot or ringing. This behaviour demonstrates that the controller responds quickly, even to extreme load changes, with a good transient response.




(a) Load step up from 50 Ω to 15 Ω




(b) Load step down from 15 Ω to 50 Ω

Figure 5.7: FCC simulation results for load steps up and down.

### Switching pulses

The FCS-MPC control technique is based on the principle of placing hard restrictions that forces the switching functions to follow a pattern that is similar to that of regularly

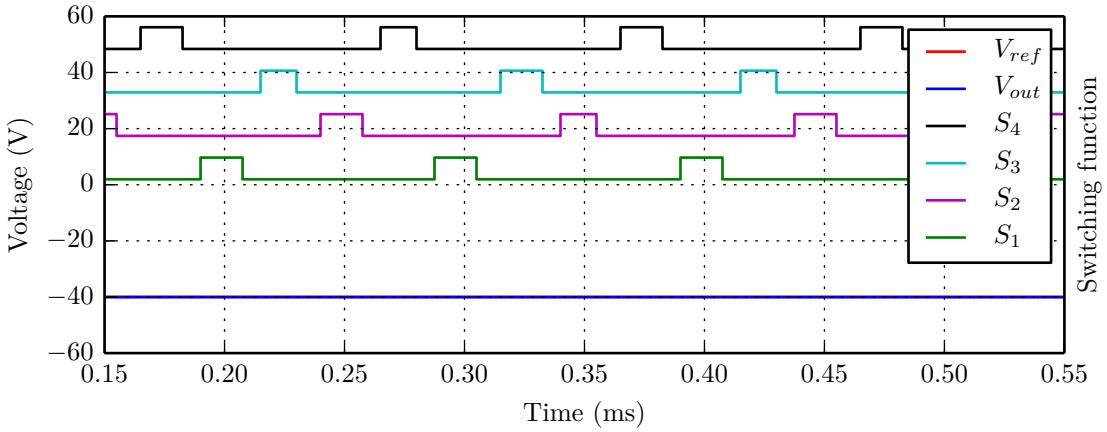
sampled PWM. In Figure 5.8 the switching pulses are shown for a DC output voltage at each prediction level. As the reference is increased from -40 V up to +40 V, the pulse widths are increased correspondingly. This confirms that the hard constraints are effective and follows the expected behaviour.

### 5.4.3 Conclusion of simulation results

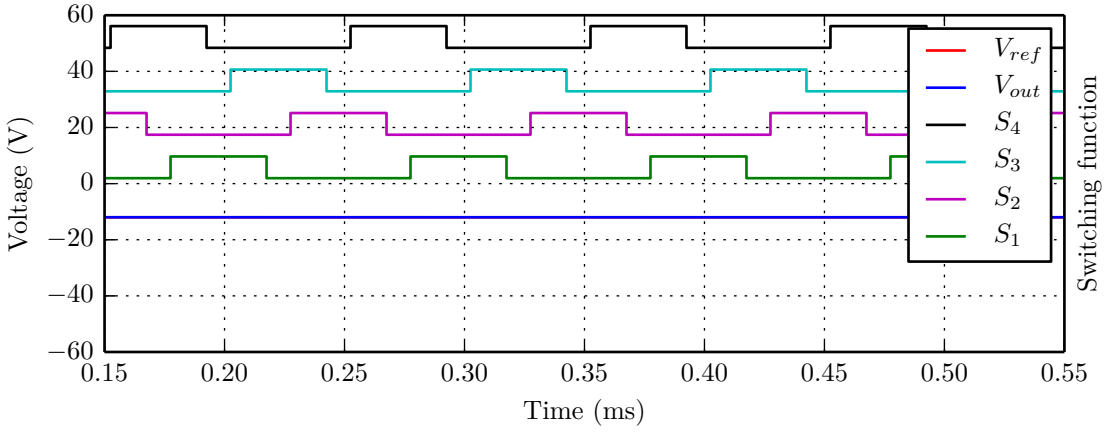
The simulation results showed that the controller effectively tracks the output voltage reference while simultaneously balancing the flying capacitor voltages. The output voltage waveform quality proved to have a low THD with a small phase and amplitude error.

It was further shown that the controller can actively control the flying-capacitor voltages while maintaining control of the output voltage.

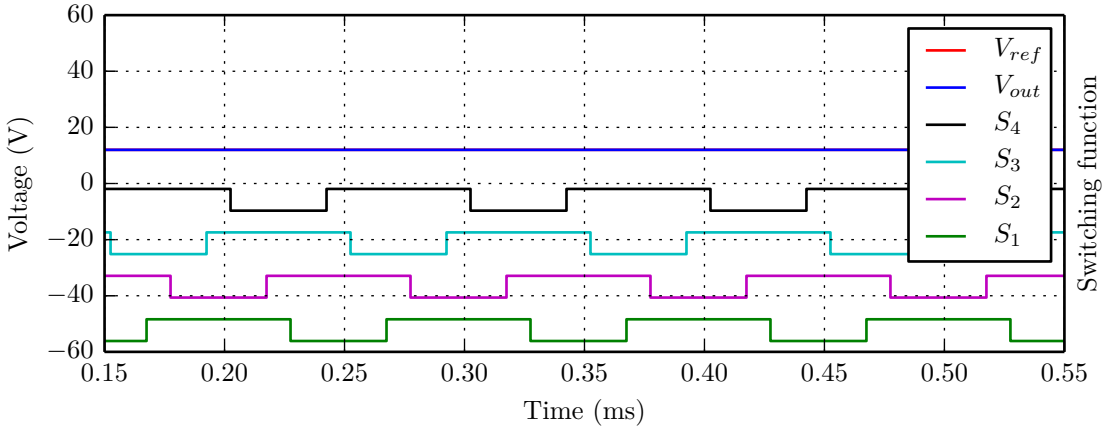
Furthermore, the controller has a fast response to reference and load step changes and recovered quickly with little or no overshoot and no ringing.



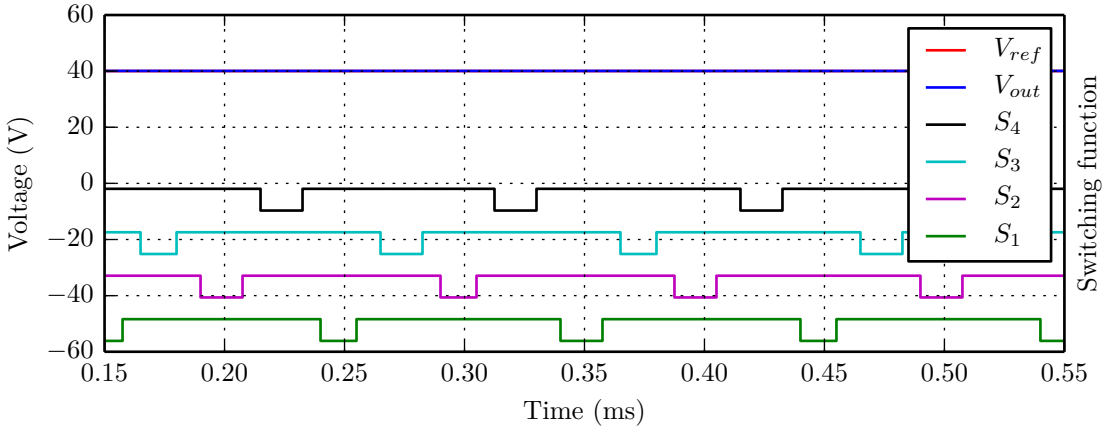

(a) Pulses for a reference of -40 V at prediction level 1




(b) Pulses for a reference at -12 V at prediction level 2




(c) Pulses for a reference of +12 V at prediction level 3




(d) Pulses for a reference of +40 V at prediction level 4

Figure 5.8: 10 kHz switching pulses at different prediction levels for the FCC converter.

## 5.5 Experimental verification and results

### 5.5.1 Overview

This section presents the practical evaluation of the fixed frequency FCS-MPC control method on the five-level flying capacitor converter. The controller is implemented according to the behaviour of four phase shifted triangular carriers. A switching frequency of 10 kHz is selected and the control is evaluated at 400 kHz. Due to the interleaved nature of the switching pulses, the switching frequency at the filter becomes 40 kHz. Control is applied to the output voltage as well as the two flying capacitor voltages. The converter is driven from a 60 V DC voltage source and under normal conditions the flying capacitor voltage should be balanced at 30 V. The controller parameters are summarised in Table 5.3

Table 5.3: Flying-capacitor converter controller parameters for the experimental evaluation

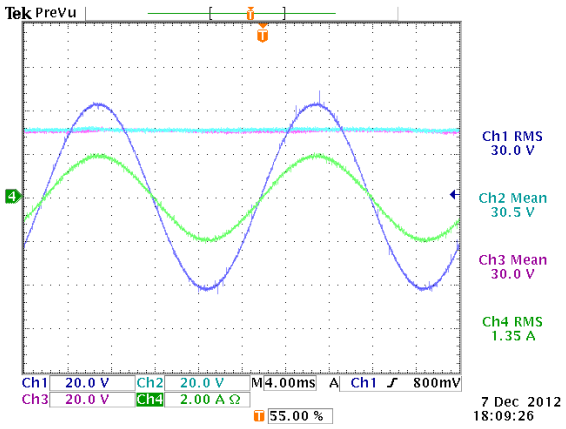
| Control Parameter | Value |
|---|---|
| $F_s$ | 400 kHz |
| $F_{sw}$ | 10 kHz |
| N | 40 steps |
| Horizon | 2 periods |
| $V_{out(err)}$ | 1 V |
| $W_1$, $W_2$, $W_3$ | 1 |
| $W_4$, $W_5$ | 20 |

### 5.5.2 Experimental results

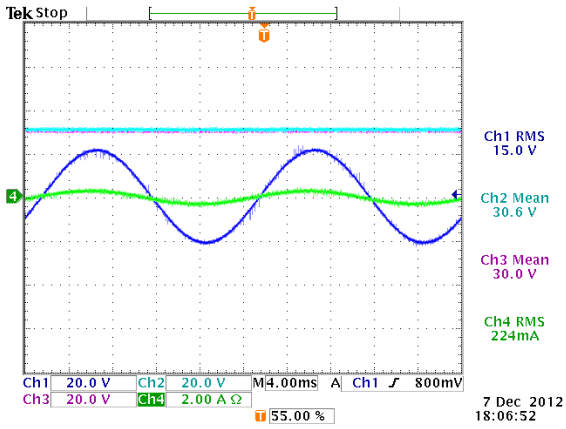
#### Steady state

The controller's performance during steady state conditions are evaluated by tracking a sinusoidal reference with an amplitude at 30 V and 15 V respectively while keeping the flying-capacitor voltages in a balanced state at 30 V DC. The experimental results in Figures 5.9a and 5.9b show that for both reference choices the controller maintains steady tracking with a fixed switching frequency. In Figure 5.9c it is shown that when flying-capacitor voltage references are set in unbalance at 45 V and 15 V respectively, the controller is able to maintain the output voltage tracking while the flying capacitor voltage are kept in unbalance.

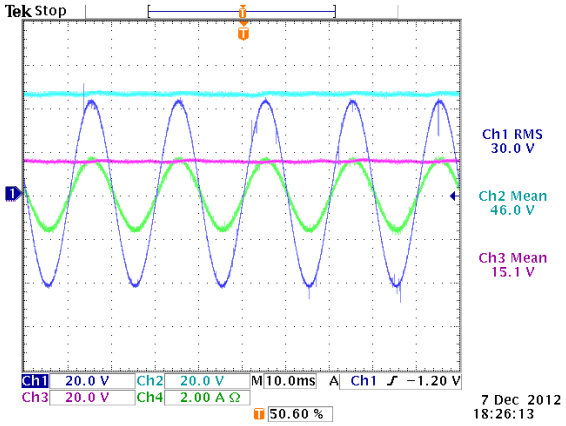
A Fast Fourier Transform (FFT) of the unfiltered output voltage during steady state is shown in Figure 5.9d. The 50 Hz component is clearly visible on the left and a large switching component is visible at 40 kHz. This shows that the effective switching frequency at the filter is fixed at 40 kHz.



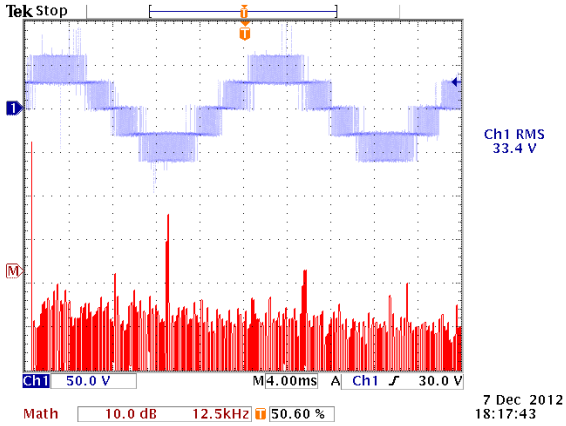

(a) Voltage reference at 30 V with balanced capacitor voltages




(b) Voltage reference at 15 V with balanced capacitor voltages




(c) Voltage reference at 30 V with unbalanced capacitor voltages




(d) FFT of the unfiltered output voltage

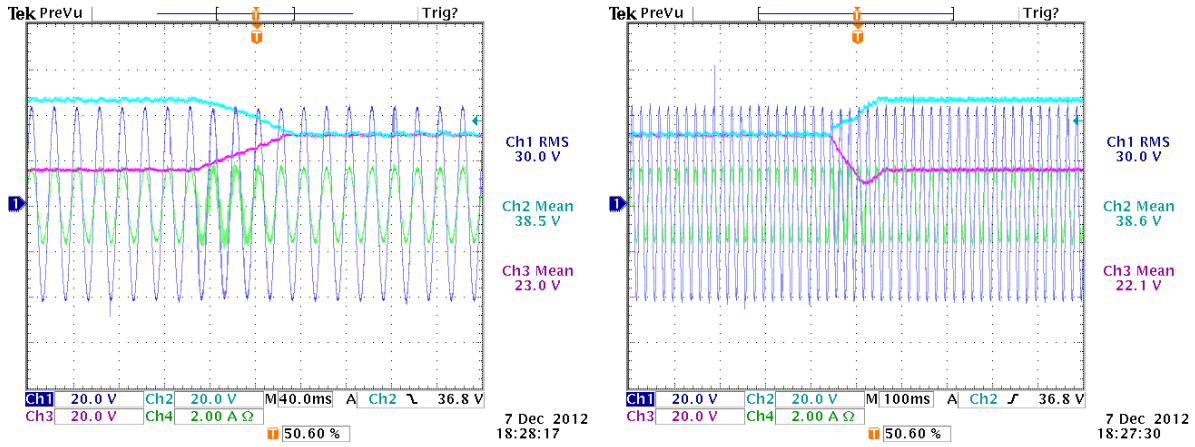
Figure 5.9: Practical measurement of the FCC converter under steady state conditions.

### Balancing the flying capacitor voltages

The flying capacitor converter has mechanisms of natural balancing of the flying capacitor voltages [65; 86]. To show that the capacitor voltages are indeed controlled, two practical measurements are taken. In Figure 5.10a the capacitor voltages are initially kept in unbalance at 15 V and 45 V respectively and then balanced at 30 V. In Figure 5.10b, it is shown that the capacitor voltages are initially kept in balance at 30 V but then forced into unbalance at 15 V and 45 V respectively. During the transient time of the capacitor voltages, reduced tracking is observed on the output voltage. However, during steady state conditions, the output voltage was kept at an amplitude 30 V, regardless of the forced flying-capacitor capacitor unbalance.

### Output voltage reference step

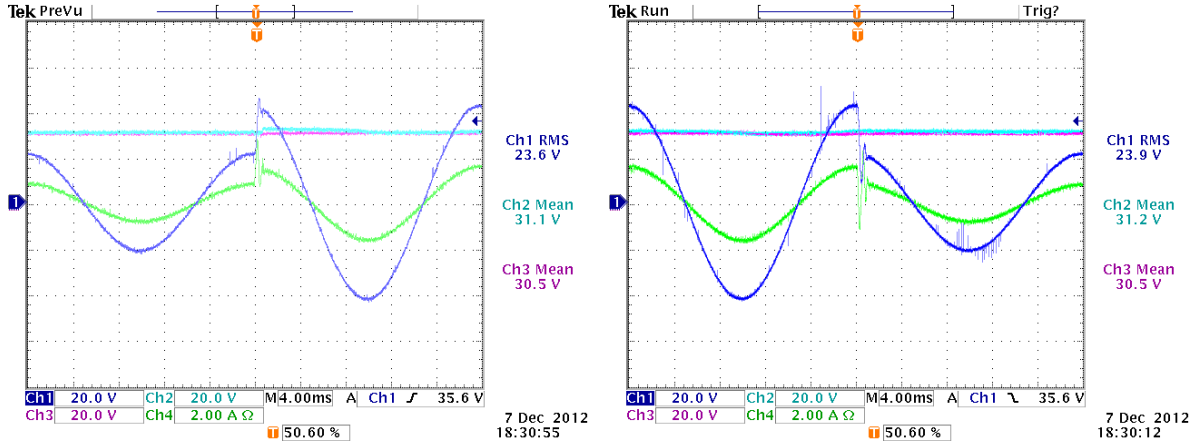
Figure 5.11 presents the experimental results for an output voltage reference step with a prediction horizon of one. The reference is stepped from 15 V to 30 V and from 30 V to 15 V respectively while maintaining capacitor balancing. It is shown that the controller




(a) Bring capacitor voltages into balance (b) Bring capacitor voltages into unbalance

Figure 5.10: Controlling the secondary controlled variables.

reacts quickly to changes in the voltage reference, but allows some overshoot and settling as is expected of a prediction horizon of one.

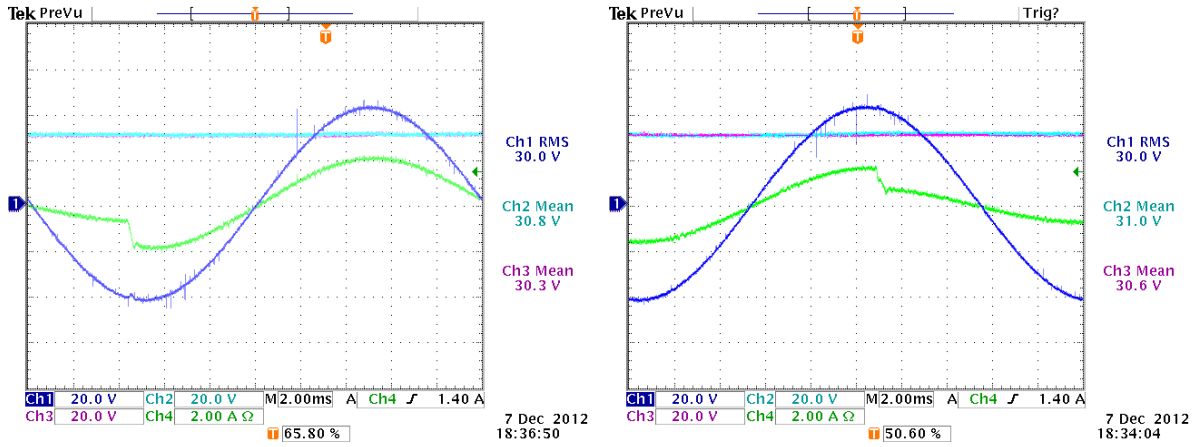



(a) Voltage reference step up from 15 V to 30 V (b) Voltage reference step down from 30 V to 15 V

Figure 5.11: Practical measurement of the FCC converter for output voltage reference steps.

### Load step

The controller's behaviour under load step conditions are shown in Figure 5.12. When a large load step is applied, a small dip in the output voltage occurs as expected, but the control reacts quickly and corrects the error as the current through the filter inductor increases. When the load is stepped down, no significant transient effects can be observed on the output voltage waveform. The practical results compare well to the expected simulation results.




(a) Load step up

(b) Load step down

Figure 5.12: Practical measurement of the FCC converter for load steps.

### 5.5.3 Conclusion of experimental results

This section presented the experimental measurement results for controlling a five-level flying capacitor converter with the fixed switching frequency FCS-MPC method.

The measurement results confirm that the controller is able to switch at a fixed switching frequency with a good output waveform quality. The controller performed with good results under steady state conditions and it proved to react quickly to load and reference step changes. The experimental results confirm the expected behaviour of the simulations in Chapter 5.4 and proves the be successful.

## 5.6 Summary

In this chapter the controller design, implementation and experimental evaluation of a five-level flying capacitor inverter were presented. The controller was designed by using the FCS-MPC method with a fixed switching frequency and a similar approach to that of the medium voltage regulator in Chapter 4 was used.

The control objectives were to balance the flying-capacitor voltages while the output voltage is tracking a sinusoidal reference signal. Simulation results evaluated the controller's response under ideal conditions and it was shown that the controller is able to maintain a fixed switching frequency, produce an output signal with a low THD and maintain balance of the flying-capacitor voltages. The controller further showed that it can react quickly to reference and load step changes with little or not overshoot and ringing.

Experimental measurements confirmed the simulation results and proved to be effective and practically feasible.

# Chapter 6

# Predictive control vs. PWM-based linear control for current control of a single-leg inverter

## 6.1 Introduction

This chapter presents a comparison of the fixed switching frequency finite-control-set model predictive control scheme with a linear resonant regulator for the current control of a single-leg inverter. The aim of this chapter is to compare the performance of the predictive controller to a known linear control scheme. The single-leg inverter topology is chosen for its simplicity and the fact that no control scheme has an apparent advantage over the other.

In [2], a comparison is made between an optimally-tuned over-sampled linear resonant regulator [1; 68] and a regularly sampled dead-beat like predictive control. The comparison is made for current control of a single-leg inverter that is driving a resistive-inductive load with an unknown sinusoidal back-EMF voltage source. It was shown that a well-tuned and sophisticated linear regulator can outperform the predictive control scheme. During steady state conditions both controllers displayed good reference tracking abilities although the linear controller performed better. When model inaccuracies are present the linear controller delivered much better results than the predictive controller.

In this chapter the same comparison is recreated for the current control of a single leg inverter but for the FCS-MPC control scheme. The same linear controller that is presented in [2] is compared to the FCS-MPC control scheme with a fixed switching frequency. The physical system and control task is presented in Chapter 6.2, an overview of the linear control scheme design is discussed in Chapter 6.3.1 and the predictive control scheme design is discussed in Chapter 6.3.2. The two control schemes are compared by way of simulation results in Chapter 6.4 and the conclusions are discussed in Chapter 6.5.

## 6.2 Physical system and control task

The physical system consists of a single-leg two-level inverter that is shown in Figure 6.1. The inverter is connected to a resistive-inductive load with a back-EMF voltage source. For the real plant, the back-EMF voltage is implemented as a 50 Hz sinusoidal voltage source with an amplitude of 120 V. For the controller design, the back-EMF voltage source can be considered as an unknown disturbance.

The two IGBT switches are switched as a complimentary pair – when $S_1$ is turned on $S_2$ is off, and vice versa. The DC-link voltage $V_{dc}$ is divided into two ideal DC voltage sources of $0.5V_{dc}$ each. The inverter has two switching possibilities that can produce a voltage of $+0.5V_{dc}$ and $-0.5V_{dc}$ respectively. The resistive-inductive load is given by $L_o$ and $R_o$ and the back-EMF voltage is given by $V_{emf}$. A summary of the component values are given in Table 6.1.

The load, together with the back-EMF voltage, is a linear first order system and can be described by two differential equations, one for each switching state, as

$$\frac{\mathrm{d}}{\mathrm{d}t}I = -\frac{R_o}{L_o}I - \frac{1}{L}V_{emf} - \frac{1}{L}0.5V_{dc} \tag{6.1}$$

and

$$\frac{\mathrm{d}}{\mathrm{d}t}I = -\frac{R_o}{L_o}I - \frac{1}{L}V_{emf} + \frac{1}{L}0.5V_{dc}. \tag{6.2}$$

and is represented in state space form $\dot{\mathbf{x}} = \mathbf{Ax} + \mathbf{Bu}$ as

$$\dot{I} = \left[-\tfrac{R_o}{L_o}\right] \cdot \left[I\right] + \begin{bmatrix} -\frac{0.5}{L_o} & -\frac{1}{L_o} \end{bmatrix} \begin{bmatrix} V_{dc} \\ V_{emf} \end{bmatrix} \tag{6.3}$$

and

$$\dot{I} = \left[-\tfrac{R_o}{L_o}\right] \cdot \left[I\right] + \begin{bmatrix} -\frac{0.5}{L_o} & -\frac{1}{L_o} \end{bmatrix} \begin{bmatrix} V_{dc} \\ V_{emf} \end{bmatrix} \tag{6.4}$$

where the state vector consists of $I$ and the input vector of $V_{dc}$ and $V_{emf}$.

For the design of the linear controller, a linearised model of the plant can be obtained by combining (6.1) and (6.2) and introducing a duty cycle $d$ such that

$$\frac{\mathrm{d}}{\mathrm{d}t}I = -\frac{R_o}{L_o}I - \frac{1}{L}V_{emf} + \frac{0.5}{L}V_{dc} \cdot d \tag{6.5}$$

where the duty cycle $d$ is in the range $[-1...1]$.

For the purpose of investigating the effects of DC-bus voltage ripple on the two control algorithms, the physical plant can be adapted as shown in Figure 6.2. This is accomplished by adding two DC bus capacitors, $C_{b1}$ and $C_{b2}$, to the DC bus and placing two inductors, $L_{in1}$ and $L_{in2}$, in series between the DC-link voltage source and the bus capacitors. The resistors $R_{in1}$ and $R_{in2}$ are the ESR resistances of the respective inductors and $R_{b1}$ and $R_{b2}$ are the respective ESR resistances of the two bus capacitors.

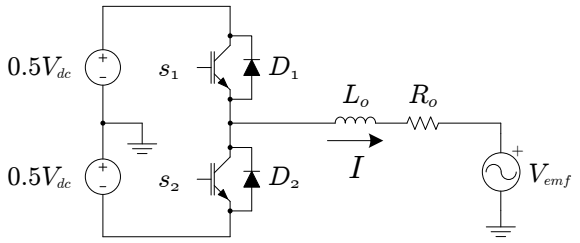



Figure 6.1: Single-leg inverter topology

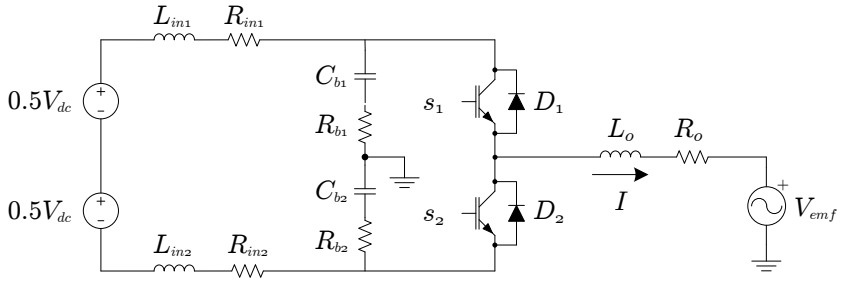



Figure 6.2: Single-leg inverter topology for evaluating DC-bus voltage ripple

Table 6.1: Single-leg inverter component values

| Component | Value | Component | Value |
|---|---|---|---|
| $V_{dc}$ | 400 V | $R_o$ | 3.5Ω |
| $V_{emf}$ | 120 VAC | $R_{in}$ | 1 Ω |
| $f_{emf}$ | 50 Hz | $R_b$ | 10 mΩ |
| $L_o$ | 300 $\mu$H | $C_b$ | 1000 $\mu$F |
| $L_{in}$ | 0.5 mH | – | – |

**Control task**

The controlled variable $I$ is the current through the resistive-inductive load. The control task is to perform current regulation by means of tracking a sinusoidal reference signal. The current reference should be tracked as accurately as possible during steady state conditions and should react fast to a step response and transients. The control scheme should maintain regulation even when model deviations and uncertainties are introduced. This includes the rejection of measurement noise, fluctuations of the DC-link voltage as well as compensation for the unknown back-EMF voltage. Blanking time should not have a significant influence on the controller's performance and should be taken into account when designing the controller.

## 6.3 Controller designs

### 6.3.1 Linear control scheme

In order to subject the predictive control scheme to the same comparison as presented in [2], the linear regulator is not re-designed but the same controller from [2] is used. This

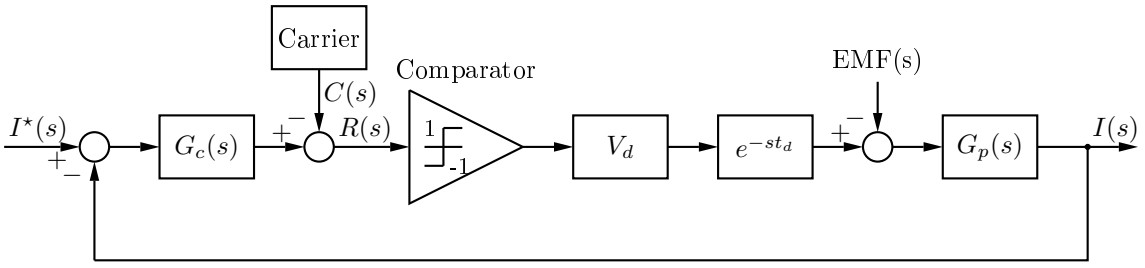



Figure 6.3: PWM current regulator feedback loop [1; 2]

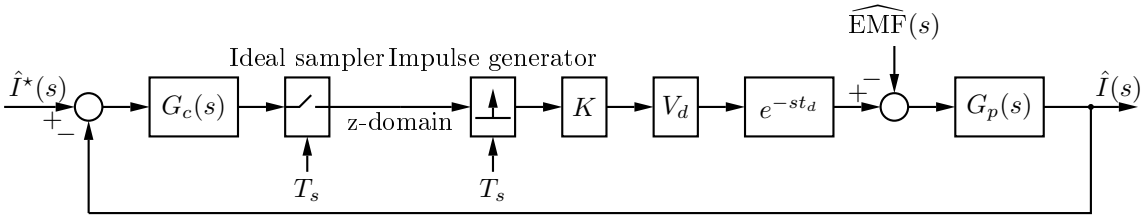



Figure 6.4: Current regulator feedback loop $z$-domain small-signal model [1; 2]

chapter presents a brief overview of that controller design and a more detailed design procedure can be found in [1].

The linear current regulator uses a highly-oversampled PWM control scheme that can be implemented digitally on an FPGA at a clocked sampling rate of 10 MHz. The high oversampling rate of the controller emulates an analogue control loop which results in an increased control bandwidth when compared to conventional regularly sampled digital control loops [87] as well as an improved transient response [88]. The analogue control loop design procedure typically treats the pulse width modulator as a simple gain block. In [2; 1] it was shown that this assumption provides a suboptimal design and that a more accurate model, developed in [89], provides a better results.

The block diagram of the PWM current regulator is shown in Figure 6.3. The reference current input is given by $I^*(s)$ followed by the compensator transfer function $G_c s$. The sawtooth carrier is represented by the carrier signal $C(s)$ and is subtracted from the modulating waveform to give $R(s)$. The comparator evaluates $R(s)$ and passes a gain block $V_d$, where $V_d$ is half the DC bus voltage. The combined transport delays in the feedback loop is represented by the delay block $t_d$. The unknown back-EMF voltage at the load is modelled as a disturbance signal that is subtracted from the signal that is passed to the $RL$ load transfer function $G_p(s)$. The transfer function of $G_p(s)$ is given by:

$$G_p(s) = \frac{\frac{1}{L_o}}{s + \frac{R_o}{L_o}}. \tag{6.6}$$

In [2] a small signal model of the control loop is presented and is shown in Figure 6.4. The small-signal control loop is based on a small-signal model of the comparator, developed in [89], which models the comparator as a sampling operation followed by an impulse generator with an equivalent small-signal gain $K_{ss}$. The gain is a function of the slope

$\dot{r_0}$ of the signal at the comparator input, just prior to the zero-crossings. According to [89; 1], the gain is given by

$$K_{ss} = \frac{2V_d f_s}{|\dot{r_0}|} \tag{6.7}$$

The small-signal sampling operation samples the reference signal every time the reference intersects the carrier. This results in a sampling frequency that is equal to the switching frequency of the converter. The sampling operation creates a virtual discrete-time $z$-domain in the short link between the sampler and the impulse generator. In [1] it is shown that it is possible to transform between the continuous-time $s$-domain and this virtual $z$-domain by using a modified version of the impulse-invariance method [89].

In [2] it is stated that the PWM pulse train contains high-frequency ripple components. These ripple components are fed back into the feed-back loop which cause an aliasing error during sampling and a change in the small-signal gain due to the ripple gradient at the sampling instance. In most cases this results in a time-varying reduction of the loop gain.

In order to account for these ripple components, a simple ripple compensation technique for a single-sided modulator from [90; 68] is employed. The ripple compensation strategy works by way of adding the sawtooth carrier to the output of the PWM modulator and cancelling the unmodulated edge of the PWM waveform. In [68] it was shown that by doing a block diagram manipulation the introduction of the additional carrier waveform is equivalent to pre-distortion of the real carrier. In practice the distorted carrier can be realised by calculating the pre-distorted carrier off-line and storing the results in a lookup table.

The approach followed in [2] was to design the feedback compensator directly in the virtual $z$-domain for the switching frequency and then transforming it back to the $s$-domain to obtain the continuous-time compensator. The compensator is designed to track a 50 Hz sinusoidal reference by placing two resonant open-loop poles at 50 Hz on the unit circle. To prevent integrator wind-up a modified version of the strategy in [91] is used.

### 6.3.2 Model predictive control scheme

The FCS-MPC controller for a fixed switching frequency follows the design procedures as discussed in Chapter 3.3. The control scheme is implemented according to the control-loop block diagram in Figure 6.5 and does not make use of a state observer. It is assumed that all the state variables are measurable for this implementation.

The off-line calculations are done by using Python together with the Numpy and Sympy libraries. The fixed switching frequency is at 2 kHz and the controller is designed for a sampling frequency of 400 kHz, which results in 200 evaluations per switching period. The *RL* load is a linear first-order system and a prediction horizon of one is sufficient for predicting transient effects.

Table 6.2: Single-leg inverter controller simulation parameters.

| Control Parameter | Value |
|---|---|
| $F_s$ | 400 kHz |
| $F_{sw}$ | 2 kHz |
| N | 200 steps |
| Horizon | 1 periods |
| $W_1$ | 1 |

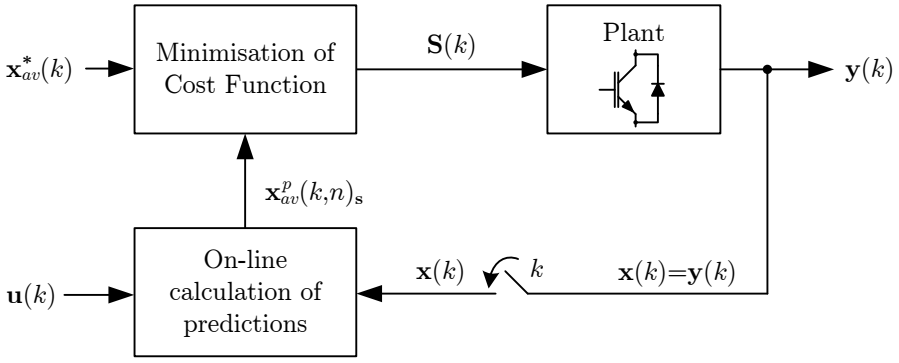



Figure 6.5: Predictive controller feedback loop

### Control reference

The control reference input is simply a sinusoidal function generator of the form

$$I^*(t) = A\sin(\omega t + \Phi) \tag{6.8}$$

where $A$ is the reference amplitude, $\omega$ is the output current waveform frequency in rad/$s$ and $\Phi$ is the phase shift to account for the average predicted value across the switching period. The control reference is assumed to be a known time-varying function but, in cases where the control reference is not known prior to the sampling instance, several extrapolation techniques can be used as discussed in Chapter 3.3.4.

### Cost function

The current regulator can be implemented in the cost function as a reference tracking problem. In this case the load current is the only controlled variable and the cost function can be designed by using the absolute value of the error with a weighting factor $W$ of one. In the previous chapters the cost function included an error band function that allows the prediction horizon to be increased during transient effects. However, for a prediction horizon of one this is not needed and it is not included in this cost function. The cost function for reference tracking of one controlled variable is therefore given as

$$g = |I^* - I^p_{av}| \tag{6.9}$$

## 6.4 Simulation results

The two control algorithms are compared by way of several simulation configurations. This includes the evaluation of the steady state tracking error, step response, effects of blanking time and measurement noise as well the effects of DC bus voltage ripple and incorrect model parameters.

The simulations are evaluated by visibly comparing the waveforms and by taking the FFT and comparing the amplitude and phase at the reference frequency.

### Steady state sinusoidal reference tracking

In the first simulation the steady state response of the controller under ideal conditions is evaluated. The current reference is set at 10 A and the simulation results are recorded in Figure 6.6.

The predictive controller (top) shows good reference tracking with an amplitude error of 26.5 mA and a phase error of 0.056°. The FFT clearly shows the 50 Hz fundamental and the 2 kHz component with its distinctive side-bands at the switching frequency. These results also compare similar to the PWM-based predictive controller that was evaluated in [2] and both exhibit similar spectral content.

The PWM-based linear controller (bottom) has better reference tracking with an amplitude error of 10.1 $\mu$A and a phase error of 0.000059°.

### Step response

The simulation results for a step response from 5 A to 10 A is shown in Figure 6.7. Both controllers have almost perfect reference tracking with no delay or overshoot. This shows that the high sampling rate of 400 kHz enables the predictive controller to produce an equally good result by overcoming the delay that is present for the predictive control scheme in [2].

### Effect of blanking time

Blanking time is a necessity in any power inverter that introduces a non-linearity that is often unaccounted for with linear controllers. One feature of model predictive control is that the non-linearities can be included in the model. This is illustrated by applying a 5 $\mu s$ blanking time to simulation model. For this simulation the prediction model was updated to include the blanking time.

The simulation results in Figure 6.8 shows that both control schemes are able to handle blanking time without affecting the steady state performance of the controller. The predictive controller (top) has an amplitude error of 36.4 mA and a phase error of 0.024° and the linear controller has an amplitude error of 10.3 $\mu$A and a phase error of

0.000058°. This shows that if the blanking time is included in the model, the predictive controller maintains steady state tracking accuracy.

### Effect of measurement noise

The effect of measurement noise is evaluated by using the estimated noise measured with a hall-effect current transducer circuit. All measurements taken by the predictive controller passes through a 400 kHz low pass filter before being used by the controller. The simulation results in Figure 6.9 clearly shows visible measurement noise on the current waveforms and a raised noise floor for both the linear controller and the predictive controller. The amplitude error of the predictive controller (top) is 21.6 mA with a phase error of 0.0097° and the amplitude error of the linear controller (bottom) is 76.5 $\mu$A with a 0.000060° phase error.

### Effect of DC bus voltage ripple

Any practical inverter will be subjected to some form of DC bus voltage ripple. To evaluate the controllers' response to unanticipated DC bus voltage ripple, two DC-link capacitors of a 1000 $\mu F$ with a 10 m$\Omega$ ESR are added in series across the DC bus. Additionally, two 0.5 mH inductors with an ESR of 1 $\Omega$ is inserted in the positive and negative bus bars as shown in the adapted topology in Figure 6.2. This results in a DC-link voltage ripple of 32 V peak-to-peak across each DC-link capacitor.

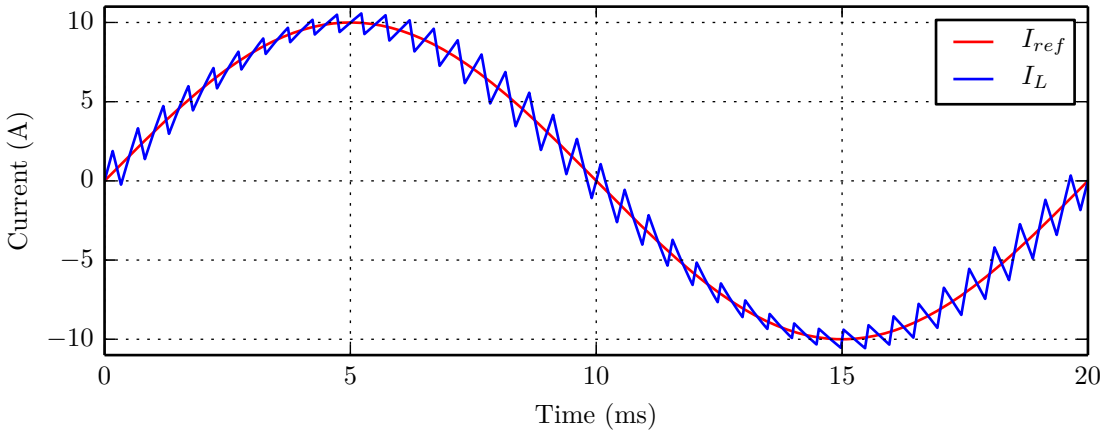
With the simulation of both controllers, the two DC-link voltages are measured across the DC-link capacitors and the controllers are not adapted to include the DC-link capacitors in their models.

The simulation results are shown in Figure 6.10. The predictive controller (top) produces a steady state amplitude error of 26.1 mA and a phase error of 0.032° while the the linear controller (bottom) maintains a 10.1 $\mu$A amplitude error and a 0.000044° phase error. This shows that both controllers are able to react to the unanticipated voltage ripple on the DC-link.

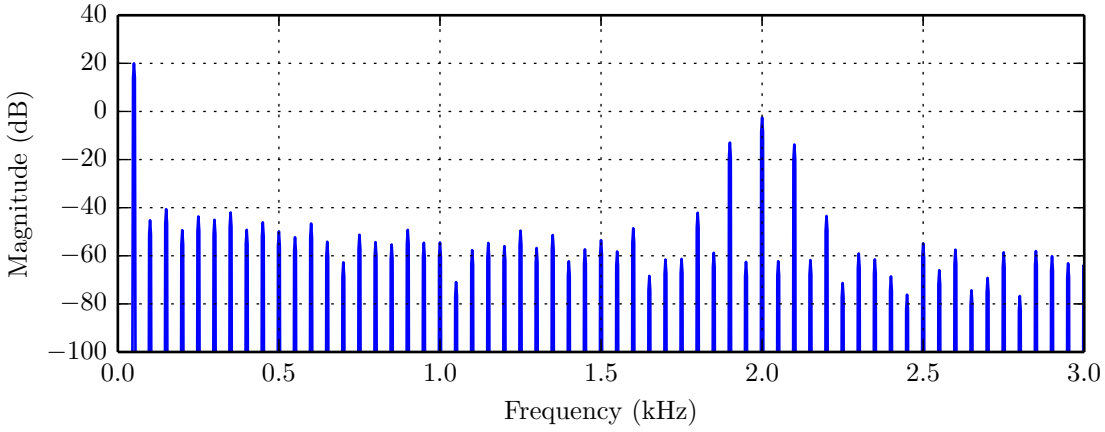
### Effect of changes in component values

Lastly, the control algorithms' sensitivity to model inaccuracies are evaluated by reducing the load inductor and resistor values by 50 % to 8.5 mH and 1.75 $\Omega$ respectively. The simulation results in Figure 6.11 shows that the linear controller (bottom) is able to maintain accurate steady state tracking with an amplitude error of 10.6 $\mu$A and a phase error of 0.000049°. The predictive controller exhibits less accurate results with an amplitude error of 1.01 A and a phase shift of 2.8°. This clearly shows that although the predictive controller is able to react fast to some unknown parameters as shown with the DC bus

voltage ripple, big changes in the model parameters have a big impact on the controller's performance.




(a) Predictive control

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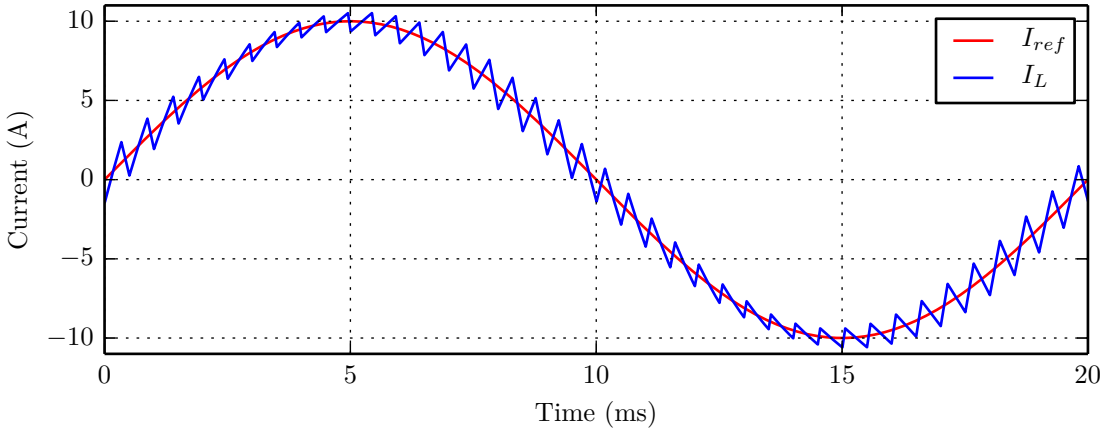
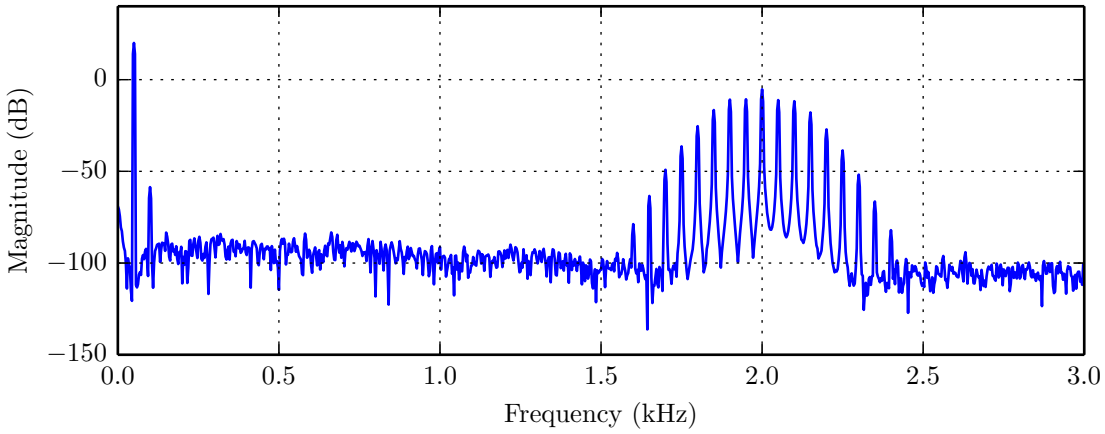
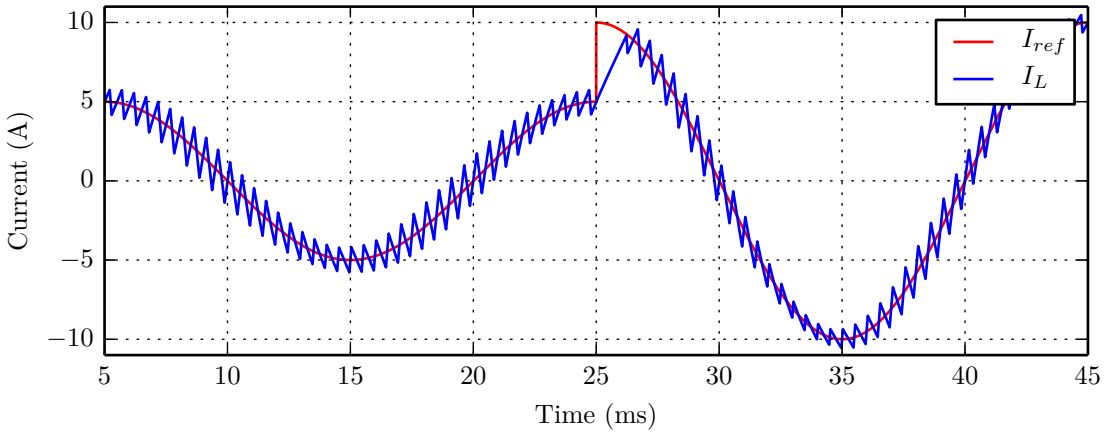



(c) Linear control

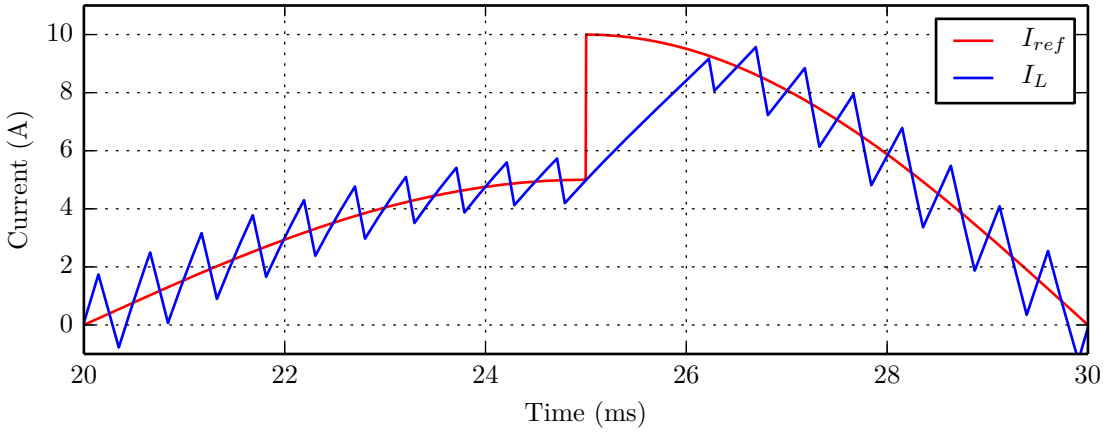



(d) Linear control

Figure 6.6: Steady state sinusoidal current reference tracking




(a) Predictive control

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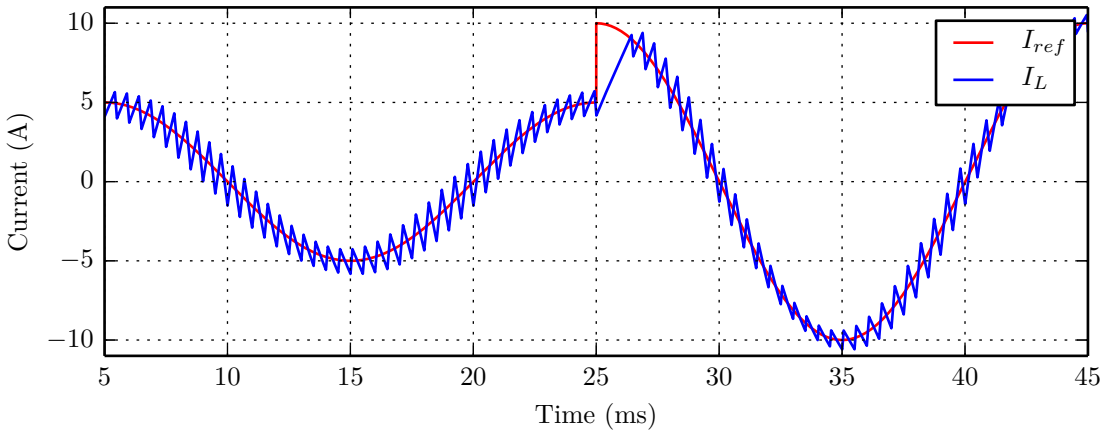
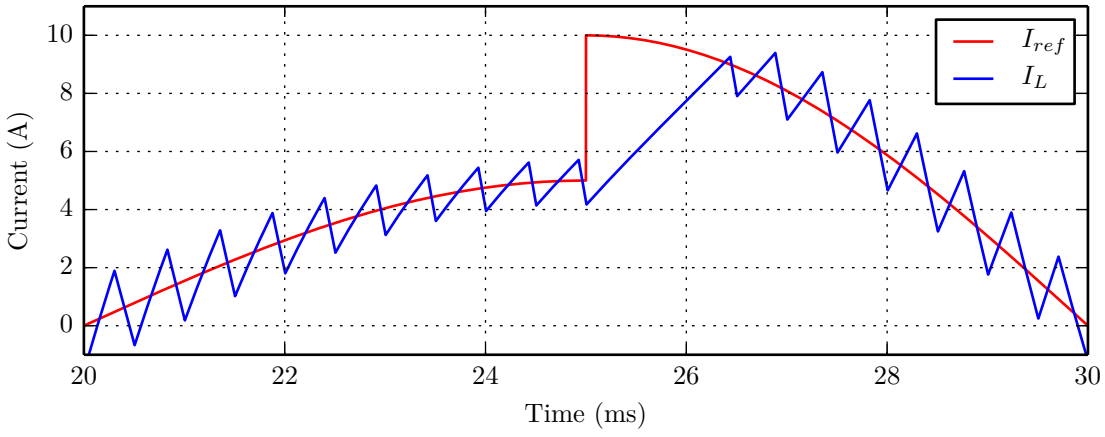
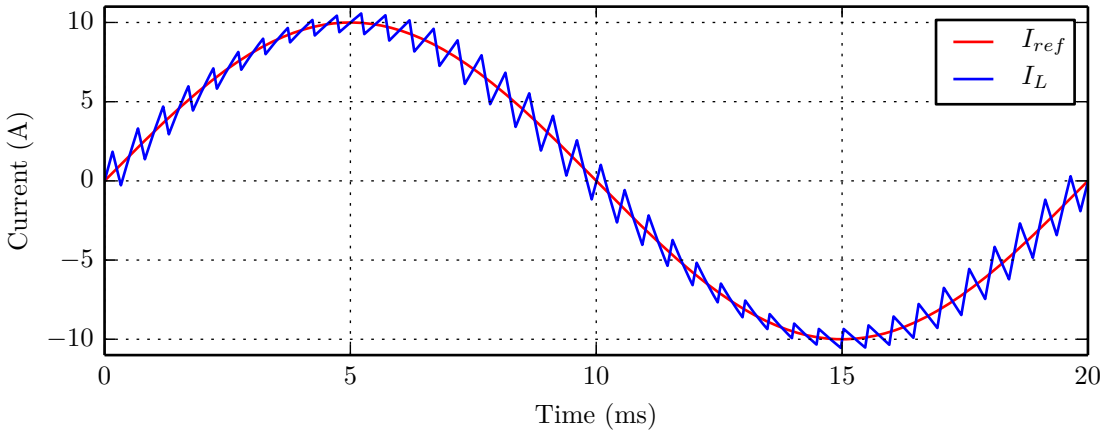



(c) Linear control

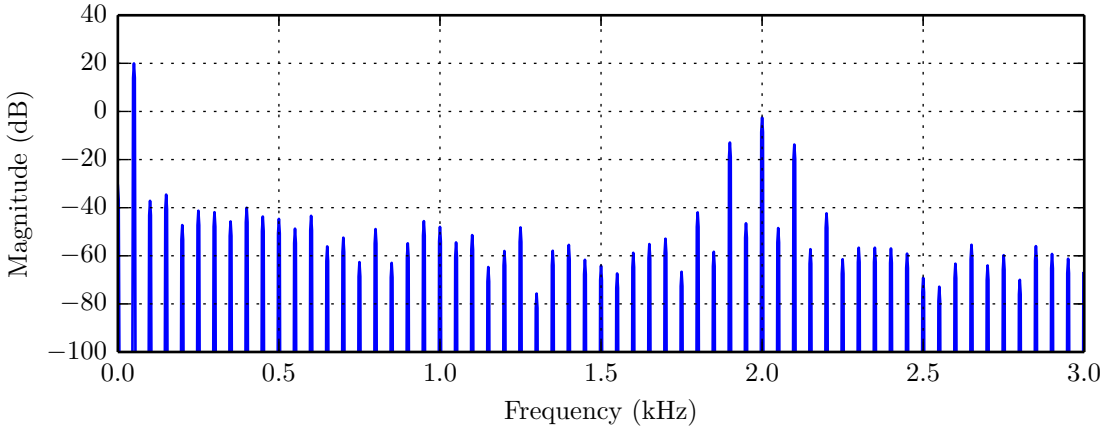



(d) Linear control

Figure 6.7: Step response from 5 A to 10 A




(a) Predictive control

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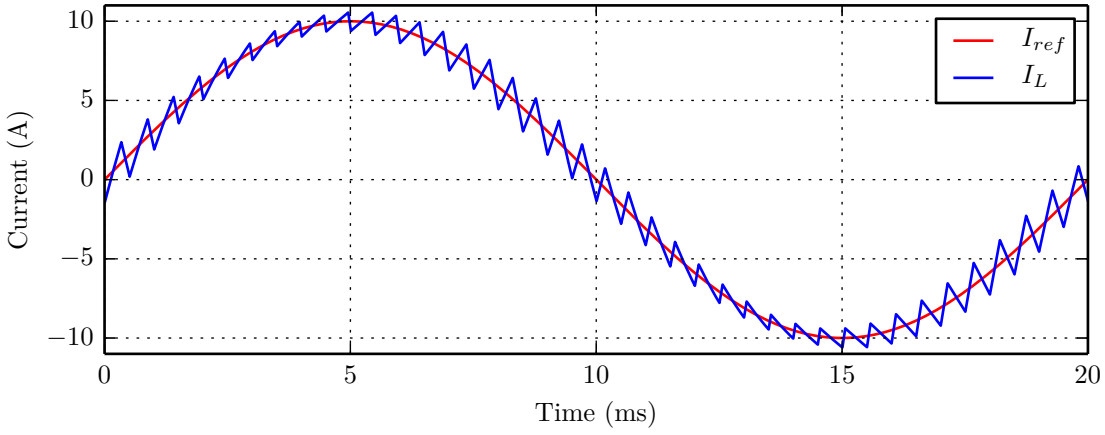
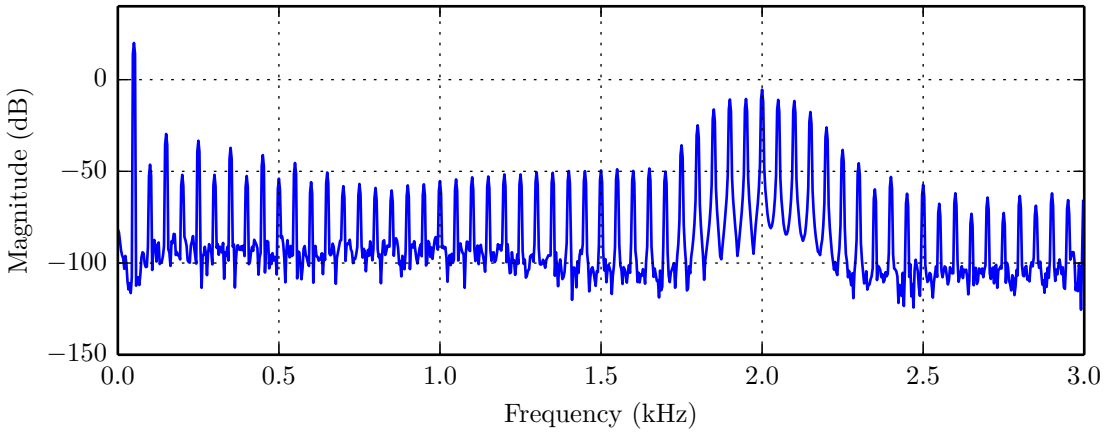
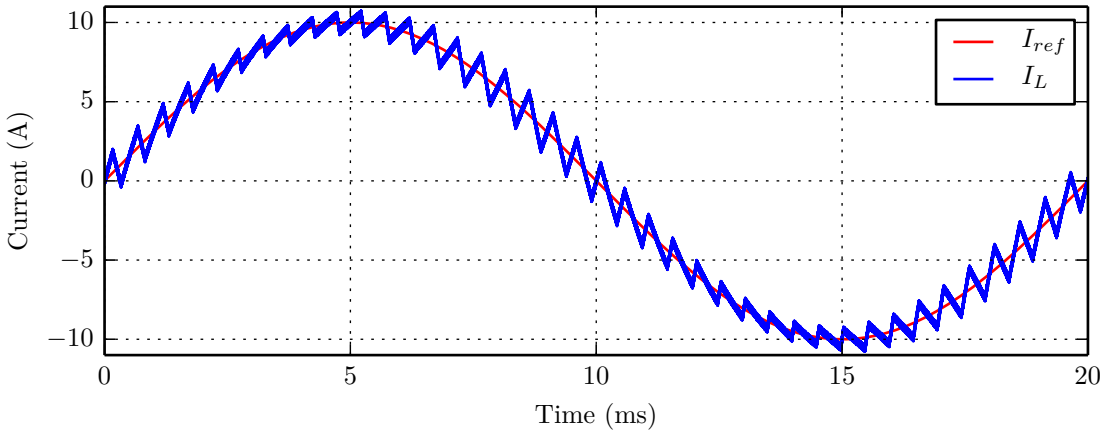



(c) Linear control




(d) Linear control

Figure 6.8: Effect of blanking time

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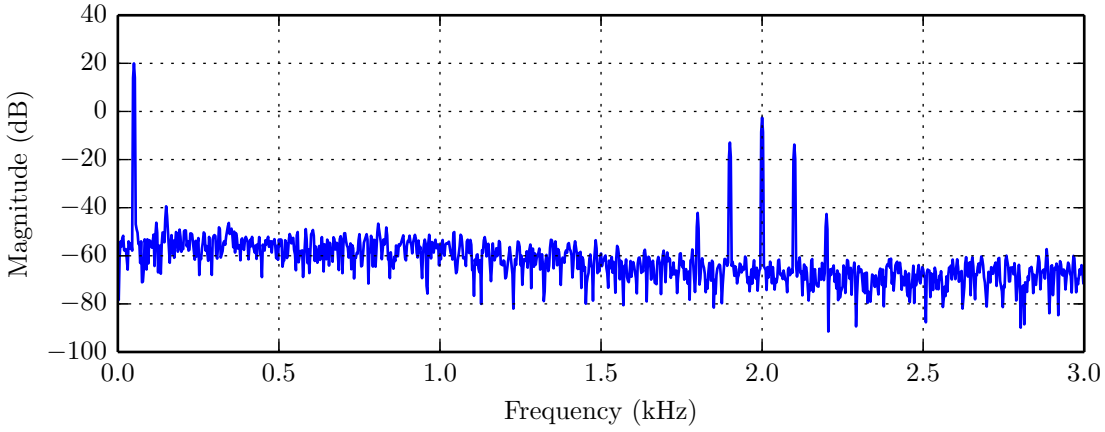


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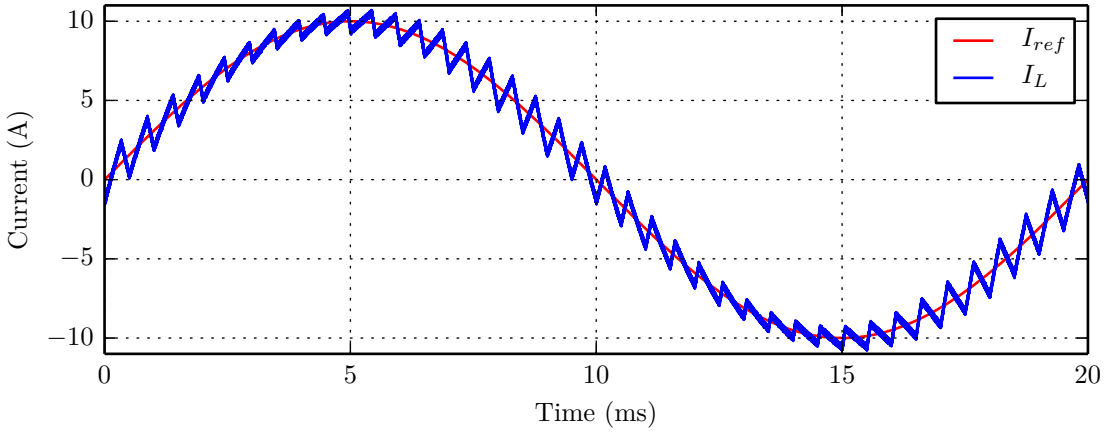
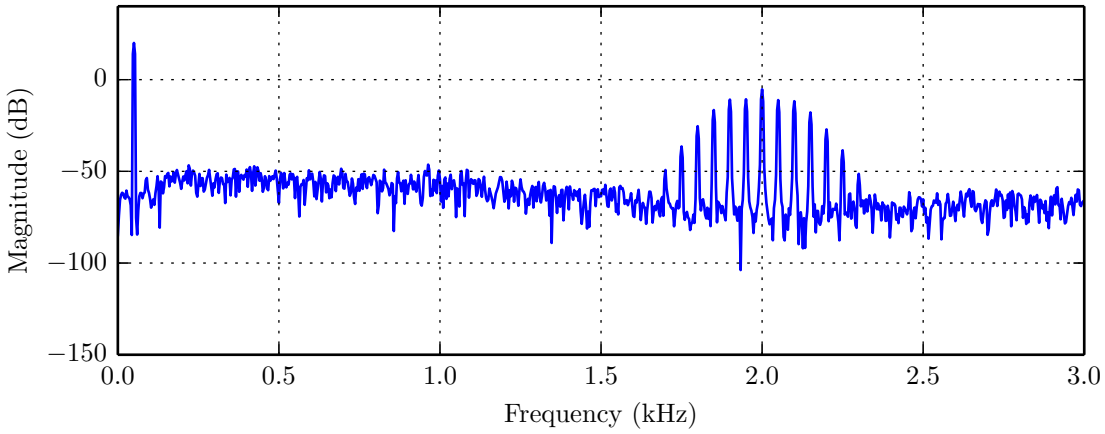
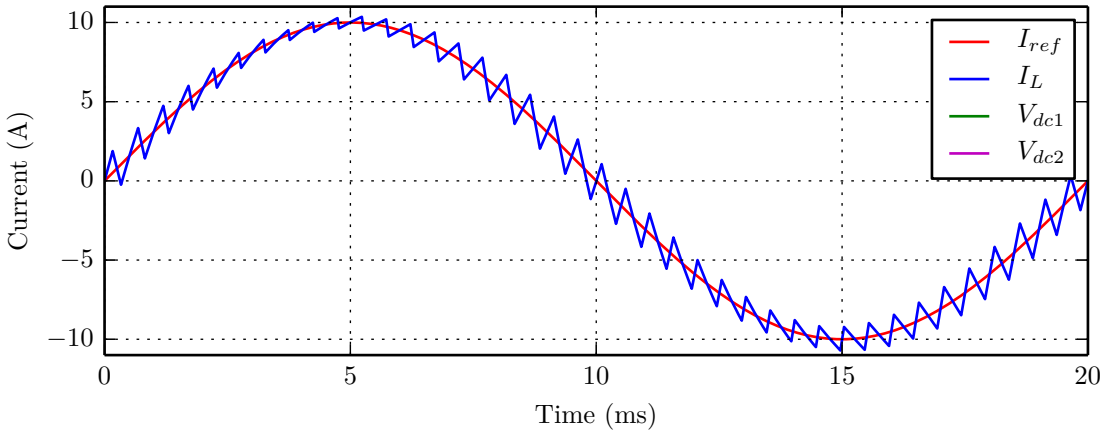



(c) Linear control

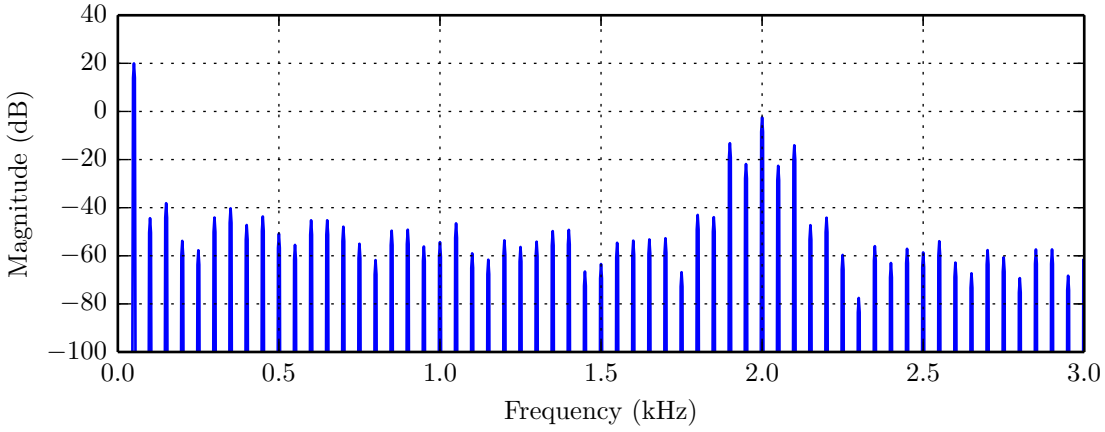



(d) Linear control

Figure 6.9: Effect of measurement noise




(a) Predictive control

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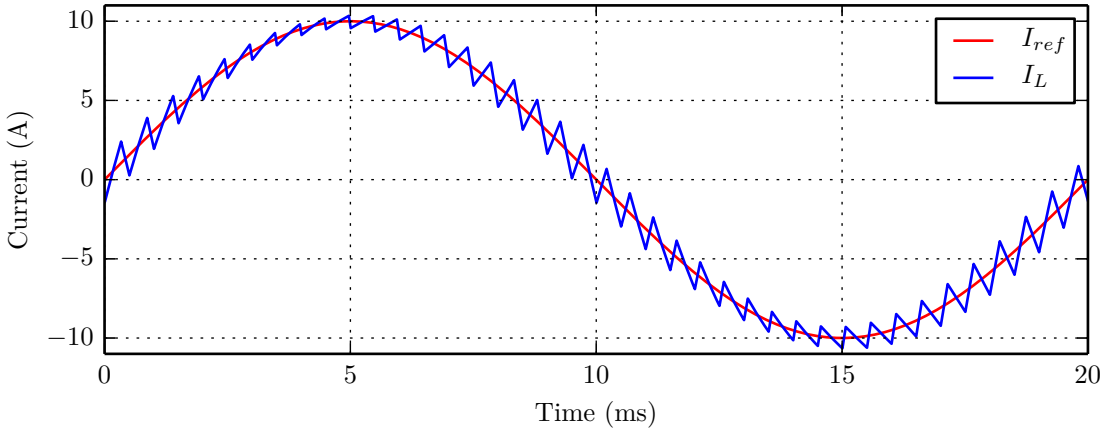
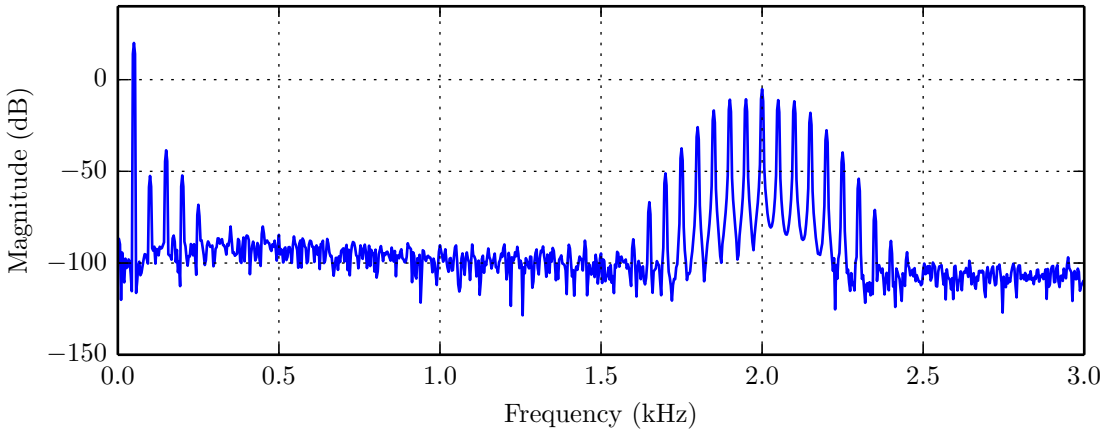
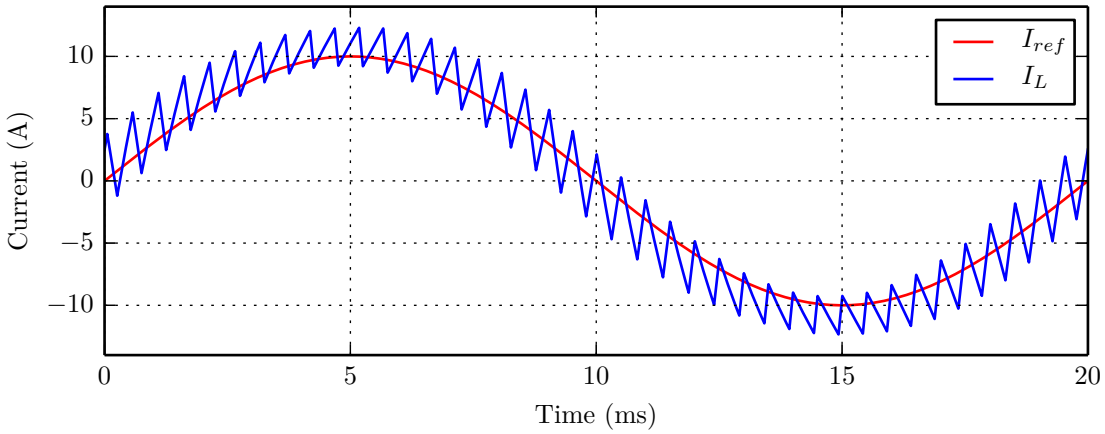



(c) Linear control

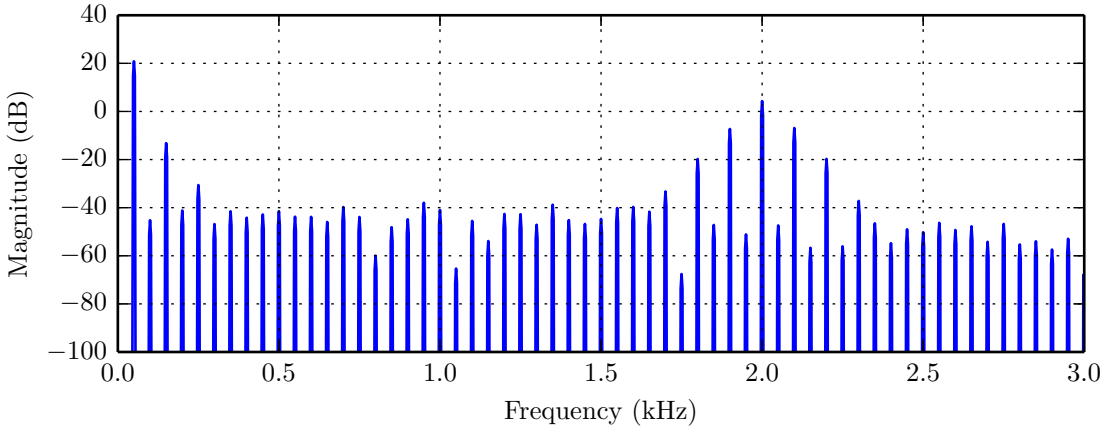



(d) Linear control

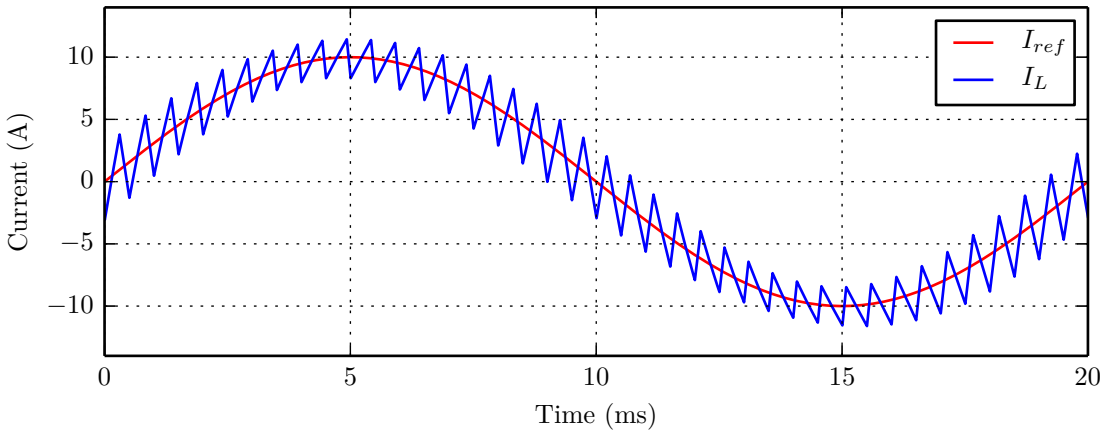
Figure 6.10: Effect of DC bus voltage ripple



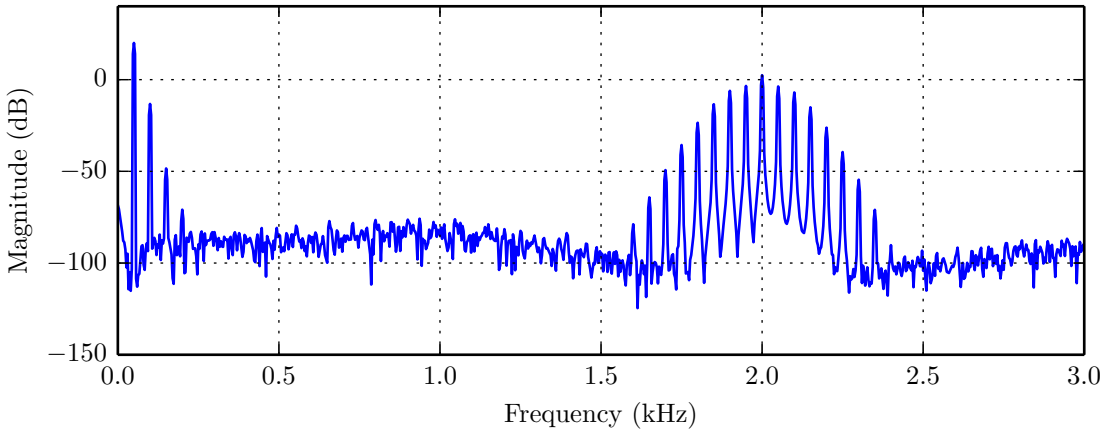

(a) Predictive control




(b) Predictive control




(c) Linear control




(d) Linear control

Figure 6.11: Effect of changes in component values

## 6.5 Conclusion of comparison

In this chapter the comparison in [2] between predictive control and linear control for current control of a single-leg inverter is recreated to compare the performance of the FCS-MPC control scheme with a fixed switching frequency to a well-tuned and highly oversampled PWM-based linear controller.

This chapter followed the same single-leg inverter topology and parameter values as given in [2]. The two control algorithms were compared by way of several simulation configurations which included the evaluation of the steady state tracking error, step response, effects of blanking time and measurement noise as well the effects of DC bus voltage ripple and incorrect model parameters.

The linear controller produced near perfect reference tracking with a very small amplitude and phase error. The predictive controller also produced very good reference tracking and, although not as small as the PWM-based linear controller, the amplitude error and phase error compared well for a controller with a much lower sampling rate and no modulator.

Both controllers had near perfect reference tracking during a reference step response and both reacted fast with no overshoot or ringing.

It was further shown that when non-linearities such as blanking time is included in the prediction model, the predictive controller maintained a small steady state tracking error.

The controllers' response to unanticipated disturbances were evaluated by introducing measurement noise to the current measurement. The linear controller effectively rejected the noise as did the predictive controller. This was accomplished by applying a low-pass filter to all the measurements of the predictive controller.

As expected the highly over-sampled PWM-based linear controller produced a smaller amplitude and phase error than the predictive controller with a fixed switching frequency. However, given that the predictive controller is sampled at a much slower rate than the PWM modulator, more quantisation noise is present which affects the comparative amplitude and phase error performance. Nevertheless the predictive controller performed very well and proved that it is effective in maintaining a fixed switching frequency with good reference tracking characteristics.

# Chapter 7

# Conclusions

## 7.1 Conclusions

The objective of this study was to develop a FCS-MPC control method with a fixed switching frequency that will compare well to the waveform quality of PWM and which provides the benefits of MPC by controlling multiple state variables.

In Chapter 2 the limitations of conventional implementations of FCS-MPC were discussed and it was shown that those implementations are typically characterised by a variable switching frequency, a high noise floor and large voltage and current ripple when doing voltage and current control. This was accounted to the fact that FCS-MPC has a much lower sampling rate and consequently a much lower resolution on the time-axis when compared to PWM-based linear controllers. This was illustrated by comparison with the well established PWM scheme. It was shown that although the control algorithm of a regularly sampled PWM controller is only sampled once in every switching period, the digital implementation of the associated PWM modulator is evaluated at a much higher sampling rate, resulting in a more accurate application of the duty cycle.

To overcome the limitations associated with FCS-MPC, a scheme was presented in Chapter 3 to achieve a fixed switching frequency. In order to maintain a fixed switching frequency as well as accurate reference tracking over the entire range of the controlled variables, a more computationally-effective method was derived that allowed for much higher sampling rates to be achieved. Experimentally, a sampling frequency of 400 kHz with a switching frequency of 10 kHz was achieved on an FPGA.

The carrier waveforms of PWM was used to develop a scheme where switching constraints are placed on the controller by defining concatenated sequences of prediction regions that are repeated for each switching period. These prediction regions were chosen in such a way that a fixed switching frequency is enforced with a pulse train that is similar to that of PWM. By using the repeated nature of the scheme, it allows predictions to be made over a horizon of multiple switching periods while limiting the number of prediction choices to $2^h$, where $h$ is the switching period horizon length. This scheme was developed

to mimic the pulse patterns of PWM for any number of carriers that are either phase shifted, phase disposed or carrier disposed.

In Section 3.3 a generalised controller scheme was derived and modelled by using established state-space theory. The generalised controller was divided into two parts: 1) The off-line pre-calculation of the computationally intensive predictions and storage of results in a lookup table, and 2) The on-line implementation of the controller.

For the off-line calculations, a load-independent state-space model of each possible switching state is obtained. This was done by modelling the load as an unknown current source and including it in the state-space model. To account for long prediction horizons, the dynamic behaviour of the load current is modelled by an Euler-forward estimation, which results in an extrapolation of the past measurement values over the prediction horizon. Each switching period is divided into a concatenated sequence of prediction regions which represents a finite number of prediction possibilities for each sampling position within the switching period. As a result, the computationally intensive calculations for predicting over the given horizon can be calculated off-line and stored in a lookup table. This was accomplished with numerical methods by using Python and the SymPy symbolic toolbox to symbolically solve the predictions in terms of the state vector. It was shown that the results of these symbolic solutions could be simplified and rewritten in the form of a state-space equation. This approach allows the off-line predictions to be stored in the form of state-space matrices in a lookup table.

The on-line controller then simply loads the appropriate prediction matrices from the lookup table, based on the current position within the switching period, and multiplies it with the current state vector and plant input. The plant input in this case is the measured driving input power source to the plant. By using this approach, the online calculation effort is reduced to a matrix loading and multiplication function. It was shown that if the FPGA architecture is correctly designed, the entire matrix multiplication can be done in one clock cycle, which is 50 ns when a 20 MHz clock frequency is used.

The major limiting factor that restricts the sampling rate with respect to the switching frequency is the FPGA clock frequency and the speed at which the prediction matrices can be loaded from the lookup table. For the experimental evaluations, the individual values in each matrix were loaded individually from memory. This restricted the sampling rate to 400 kHz. If an FPGA with a higher clock frequency is used and the matrix-loading process could be redesigned to load faster, it would be possible to have a sampling rate beyond 1 MHz.

The controller design was evaluated by simulation and the expected results were confirmed by experimental measurements. This was done for three inverter topologies: 1) The primary objective of this study was the control of a multi-level AC-to-AC converter with an $LC$ output filter for voltage regulation on MV distribution networks. 2) To illustrate the generalised controller scheme, the controller was also evaluated for the voltage

regulation and capacitor balancing of a five-level flying-capacitor converter. 3) Lastly, the performance of the controller was compared in simulation to a well-tuned linear PI-controller for current control of a single-leg inverter.

The control objectives of the AC-to-AC converter was to provide output voltage regulation with good steady state reference tracking and a low THD while simultaneously suppressing resonance at the input bus. Through simulation and experimental results it was shown that a clear fixed switching frequency was maintained with a pulse train that resembles that of PWM. FFT plots clearly showed the fundamental switching frequency with its multiples at higher frequencies. The lower frequency spectrum had a raised noise floor compared to the higher frequency spectrum which can be attributed to quantisation noise. It was shown that when control is applied to the input bus, current resonance is suppressed which improved the overall tracking performance of the output voltage. It was further shown that during reference step changes, overshoot and ringing is visible when a prediction horizon of one is used. When the prediction horizon was increased, the controller was able to anticipate the overshoot and ringing and provided good transient results. However it was shown that due to the optimization technique to reduce the number of prediction choices over the prediction horizon, the steady-state tracking performance gradually deteriorated as the prediction horizon was increased. This was overcome by applying an event-based horizon strategy where the horizon is only increased when the tracking error is increased. The event-based horizon proved to be effective en provided good steady-state and transient results.

The generalised controller scheme was experimentally evaluated for the voltage regulation and capacitor balancing of a five-level flying-capacitor converter. Simulation and experimental results showed that the controller can effectively track the output voltage while actively balancing the flying-capacitor voltages. The results reconfirmed the expected and measured behaviour that was obtained from the AC-to-AC converter topology.

Lastly, the performance and output waveform quality of the FCS-MPC scheme was extensively compared to that of a PWM-based linear-resonant regulator. The two controllers were evaluated in simulation under ideal conditions for current control of a single-leg inverter. During steady-state tracking the predictive controller had an amplitude error of 26.5 mA, 0.056° while the linear regulator only had an error of 10.1 $\mu$A, 0.000059°. During a step response however, both controllers had almost the exact near perfect tracking. It was further shown that the MPC controller was able to handle the effects of blanking time, measurement noise and unanticipated DC-bus voltage ripple without any significant degradation of the tracking performance. However, the FCS-MPC controller did prove to be sensitive to model inaccuracies. This was evaluated by reducing the plant component values by 50 % without adjusting the controller model. Although the FCS-MPC controller remained stable, this led to a fixed steady-state tracking error that could not be accounted for. The linear controller, however, were able to correct itself when these

inaccuracies were introduced.

From these results it is concluded that the proposed FCS-MPC scheme to achieve a fixed switching frequency is effective and practically realisable in hardware. It was shown that the poor output waveform quality that is often associated with FCS-MPC can be improved by increasing the controller's sampling rate. By applying hard constraints according to the proposed scheme, a fixed switching frequency can be maintained which provided an output waveform quality that is comparable to that of a PWM-based controller while controlling multiple state variables.

## 7.2 Recommendations and future work

1. The scope of the research project was limited to the control of single-phase converters. The control scheme was therefore only implemented for current and voltage control of single-phase converters. This approach could be further developed to include the control three-phase converters and motor drive applications.

2. Longer prediction horizons during steady-state tracking of a sinusoidal reference may deteriorate the tracking performance due to the fact that an assumption is made about the pulse width increases over the subsequent switching periods of the prediction horizon. With each switching period over the prediction horizon the pulse width is incremented by a fixed value. To account for the varying reference over the prediction horizon this fixed value could be gradually increased.

3. An integrating control action, as discussed in Chapter 2.3, can be implemented in the cost function. However, to remain computationally efficient, the integrating action can be included in the state space model and the prediction can pre-calculated off-line.

# Appendices

# Appendix A

# Design of the medium voltage electronic voltage regulator hardware

## A.1 Introduction

In this chapter the detailed design of the medium voltage electronic voltage regulator that is presented in Chapter 4.3 is discussed. For an overview of the topology and basic operation, see Chapter 4.3.1.

This chapter is divided into the following sections:

- Section A.2: Transformer specifications
- Section A.3: Design of the AC-to-AC converter modules
- Section A.4: Design of the protection mechanisms
- Section A.5: Integration of the controller hardware and peripherals
- Section A.6: Experimental hardware verification

## A.2 Transformer specifications

According to requirements, the MVEVR should be able to perform voltage regulation on a 22 kV three-phase distribution feeder. This is achieved by connecting three single-phase regulators in a start configuration. The nominal voltage across each single-phase regulator is calculated as the line-neutral voltage,

$$\begin{aligned} \mathrm{V}_{LN(nom)} &= \frac{\mathrm{V}_{LL}}{\sqrt{3}} \\ &= \frac{22 \ \mathrm{kV}}{\sqrt{3}} \\ &= 12.7 \ \mathrm{kV}. \end{aligned} \tag{A.1}$$

The standard for quality of electricity supply allows for a ±10% deviation from the nominal voltage [77]. By adding 10% to the line voltage, the maximum peak line-neutral voltage is given by

$$\begin{aligned} \mathrm{V}_{LN-peak} &= (1.1)\frac{\sqrt{2}\mathrm{V}_{LL}}{\sqrt{3}} \\ &= 19.76 \ \mathrm{kV} \end{aligned} \tag{A.2}$$

Each MVEVR unit consists of two AC-to-AC converter modules, connected in an autotransformer configuration to an appropriate transformer. The transformer consists of a primary winding (common winding) and two isolated secondary windings (series windings), wound around the same core as shown in Figure A.1. The secondary windings act as isolated voltage sources for the two AC-to-AC converter modules. The two AC-to-AC converter modules are series stacked and connected to the primary side of the transformer in an autotransformer configuration. Since the MVEVR has to regulate 10% of the line voltage, each AC-to-AC converter has to regulate 5% of the line voltage. The voltage across the secondary windings of the transformer is therefore 5% of $V_{LN}$. The transformer winding ratios is given by

$$\frac{\mathrm{V}_p}{\mathrm{V}_{t1}} = \frac{\mathrm{V}_p}{\mathrm{V}_{t2}} \tag{A.3}$$

Table A.1: Transformer specifications and parameters.

| | |
|---|---|
| Transformer Power Rating (nom) : | 127 $\mathrm{kVA}_{rms}$ |
| Primary terminal voltage (nom) : | 12.7 $\mathrm{kV}_{rms}$ |
| Input voltage deviation : | ±10% |
| Number of secondary windings : | 2 |
| Secondary terminal voltage, $V_{s1}$ : | 635 $\mathrm{V}_{rms}$ |
| Secondary terminal voltage, $V_{s2}$ : | 635 $\mathrm{V}_{rms}$ |
| Transformer Ratio under full load ($V_p$ : $V_{s1}$) : | 20:1 |
| Transformer Ratio under full load ($V_p$ : $V_{s2}$) : | 20:1 |
| Primary full load current : | 10 $\mathrm{A}_{rms}$ |
| Secondary full load current (each) : | 100 $\mathrm{A}_{rms}$ |

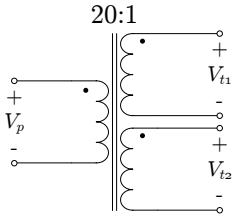



Figure A.1: Schematic diagram of the transformer windings.

where

$$\mathrm{V}_{t1} = (0.05)\mathrm{V}_p. \tag{A.4}$$

Substituting (A.4) into (A.3) gives us the transformer ratio of

$$\begin{aligned} \frac{\mathrm{V}_p}{\mathrm{V}_{t1}} &= (0.05)\mathrm{V}_p \\ &= \frac{\mathrm{V}_p}{0.05 \cdot \mathrm{V}_p} \\ &= 20. \end{aligned} \tag{A.5}$$

According to the specifications, the maximum line current is $100A_{rms}$ and each secondary winding is therefore required to safely conduct $100A_{rms}$. The system is connected in an autotransformer configuration with two secondary windings and one primary winding. The current through the primary winding is given by

$$\begin{aligned} \mathrm{I}_P &= \mathrm{I}_{t1}\left(\frac{\mathrm{V}_{\mathrm{t1}}}{V_p}\right) + \mathrm{I}_{t2}\left(\frac{\mathrm{V}_{\mathrm{t2}}}{V_p}\right) \\ &= \frac{100\ \mathrm{A}}{20} + \frac{100\ \mathrm{A}}{20} \\ &= 10\ \mathrm{A}_{rms} \end{aligned} \tag{A.6}$$

and the nominal power requirements of the transformer is given by

$$\begin{aligned} \mathrm{S}_{1\Phi} &= \mathrm{V}_p \cdot \mathrm{I}_p \\ &= (12.75\ \mathrm{kV})(10\ \mathrm{A}) \\ &= 127\ \mathrm{kVA}. \end{aligned} \tag{A.7}$$

In order for the AC-to-AC converter to properly apply control, an accurate model of the system is required. For this reason, it is important to find the equivalent leakage inductance as seen from the secondary terminals of the transformer.

As a guideline, the maximum leakage inductance for general distribution transformers can be estimated around 0.05 p.u. Usually the base power, $S_{base}$, is taken as the transformer power, $S_{1\phi}$. However, the transformer consists of one primary and two equal secondary windings. Since the two AC-to-AC converter modules are series stacked, the current through the two secondary windings is essentially the same. As a result, the power

in each secondary winding can be taken as half of the total transformer power. The base power at each secondary winding can therefore be taken as

$$\begin{aligned} \mathrm{S}_{base} &= \frac{\mathrm{S}_{1\Phi}}{2} \\ &= \frac{127\ \mathrm{kVA}_{rms}}{2} \\ &= 63.5\ \mathrm{kVA} \end{aligned} \tag{A.8}$$

and the base voltage as

$$\mathrm{V}_{base} = \mathrm{V}_{t1}. \tag{A.9}$$

The base impedance can be calculated using the base power and base current

$$\begin{aligned} \mathrm{Z}_{base} &= \frac{\mathrm{V}^2}{\mathrm{S}_{base}} \\ &= \frac{(635\ \mathrm{V})^2}{63.5\ \mathrm{kVA}} \\ &= 6.35\ \Omega. \end{aligned} \tag{A.10}$$

The reactance as a result of the leakage inductance is given by

$$\begin{aligned} \mathrm{X}_{eq} &= (0.05)\mathrm{Z}_{base} \\ &= (0.05)(6.35\Omega) \\ &= 317\mathrm{m}\Omega \end{aligned} \tag{A.11}$$

which allows us to calculate the equivalent leakage inductance,

$$\begin{aligned} \mathrm{L}_{\mathrm{eq}} &= \frac{\mathrm{X}}{2\pi f} \\ &= \frac{317.5\mathrm{m}\Omega}{2\pi 50\mathrm{Hz}} \\ &= 1.01\ \mathrm{mH}. \end{aligned} \tag{A.12}$$

The value of the equivalent leakage inductance can be used as a guideline for the maximum expected inductance, when designing the protection mechanisms. The real value of the leakage inductance is expected to be less and will be measured for the practical system.

The voltage drop across the leakage inductance under full load conditions can be taken as the voltage across $X_{eq}$,

$$\begin{aligned} \mathrm{V}_x &= \mathrm{I}_{nom} \cdot \mathrm{X}_{eq} \\ &= (100\mathrm{A})(317\mathrm{m}\Omega) \\ &= 31.7\mathrm{V}_{rms} \end{aligned} \tag{A.13}$$

which has a 5% variation in the nominal voltage between full load and no load. The transformer specifications are summarized in Table 4.1.

## A.3 Design: AC-to-AC Converter

### A.3.1 Overview

This section discusses the detail design and component selection for the circuit elements of the AC-to-AC converter topology that is discussed in Chapter 4.2.2 and is shown Figure 4.3. The AC-to-AC converter topology consists of four IGBTs with their respective free-wheeling diodes, an output $LC$ filter, snubber capacitors and a bus capacitor. The remaining components in the circuit diagram form part of the protection mechanisms and is discussed in Section A.4.

In A.3.2 of this section, the power ratings and losses associated with each switching element is calculated in order to select the proper IGBTs. The switching losses and conduction losses are calculated for the IGBTs as well as the conduction losses in the free-wheeling diodes. From the switching scheme, the total loss in the system is determined and the efficiency is calculated.

The loss calculations are used in Section A.3.3 to do a thermal analysis of the IGBT junction temperatures, case temperatures and heatsink temperature in order to obtain the proper heatsink thermal resistance. An analysis of the heatsink temperature versus IGBT collector current is presented as well as the relationship between the IGBT junction temperature and collector current for various heatsinks.

The following two sections, A.3.4 and A.3.5, discuss the detail design of the inductor and capacitor for the output $LC$ filter. The filter inductor has to limit the current ripple to 30% while the capacitor has to limit the voltage ripple to 1%. The design considerations are evaluated and a practical realisation is presented.

In the following section, A.3.6, the detail design of the two snubber capacitors is discussed. The snubber capacitors are added to solve the commutation problem by limiting the rate of rise of the voltage across the IGBTs and providing a return path for the filter inductor current during dead time.

Since the leakage inductance on the input side has a significant inductance, the snubber capacitors are not sufficient to provide a return path for leakage inductance current. Section A.3.7 discusses the design of a bus capacitor that is capable of limiting the rate of rise of voltage across the input bus when the IGBTs are turned off for a maximum time of one switching period. Practical considerations are evaluated and a practical realisation is presented.

The AC-to-AC converter is evaluated in Section A.3.8 with extensive simulation results, verifying the design and showing the expected behaviour of the system.

The design is concluded in Section A.3.9 together with a table of all the components, designed values, selected hardware manufactures and model numbers.

### A.3.2 IGBT Requirements and Loss Calculations

In order to select the proper IGBTs, the power ratings and losses associated with each switching element has to be calculated. The IGBT, model SKM600-GA167D from SEMIKRON, is considered and verified in this section. The switching elements consist of IGBTs $T_1$, $T_2$, $T_3$ and $T_4$ together with their free-wheeling diodes $D_1$, $D_2$, $D_3$ and $D_4$, as shown in Figure 4.3. There are four possible switching states and each switching element has different losses during each state.

The first two switching states, shown in Figure A.2 (A) and (B), are used during the positive half-cycle of $E_s$ while the second two states, shown in Figure A.2 (C) and (D), are used during the negative half-cycle. For the purpose of loss calculations, it is assumed that the output current $I_{out}$ is in phase with the input voltage $E_s$, which results that only one IGBT and one diode conduct at a time: $T_1$ and $D_4$ conduct during state (A), $T_3$ and $D_2$ conduct during state (B), $T_4$ and $D_1$ conduct during state (C) and $T_2$ and $D_3$ conduct during state (D). Each conducting element dissipates energy as a result of their on-state voltage. However, the IGBTs have additional losses associated with turning on and turning off which will be evaluated separately from the conduction losses. Since the IGBTs are switched as complimentary pairs, there will always be two IGBTs switching at a time.

#### Conduction Losses

The average conduction losses for the IGBTs and their free-wheeling diodes are derived in [79] and given in terms of the duty-cycle $D$, output current $I_{out}$ and respective on-state voltage $V_{on}$. The average IGBT conduction losses are given by

$$P_{cond(T_1)} = \frac{D}{\pi} I_{out(peak)} V_{ce(sat)} \tag{A.14}$$

$$P_{cond(T_2)} = \frac{(1-D)}{\pi} I_{out(peak)} V_{ce(sat)} \tag{A.15}$$

$$P_{cond(T_3)} = \frac{(1-D)}{\pi} I_{out(peak)} V_{ce(sat)} \tag{A.16}$$

$$P_{cond(T_4)} = \frac{D}{\pi} I_{out(peak)} V_{ce(sat)} \tag{A.17}$$

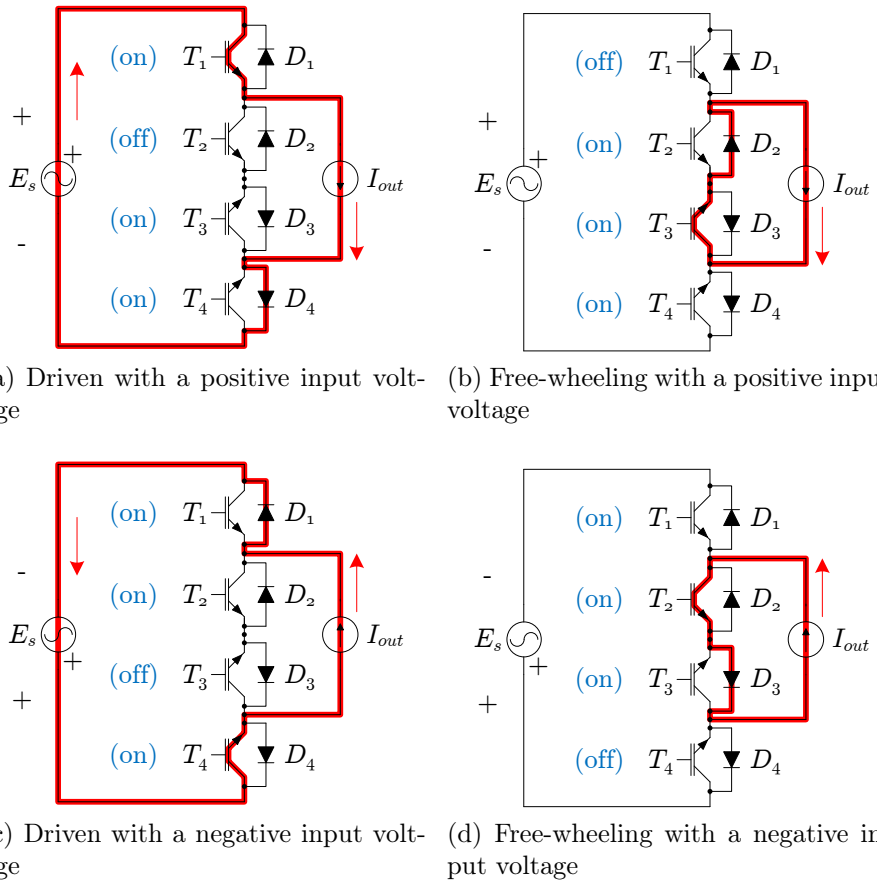
and the losses for the free-wheeling diodes are given by

$$P_{cond(D_1)} = \frac{D}{\pi} I_{out(peak)} V_{F(Diode)} \tag{A.18}$$

$$P_{cond(D_2)} = \frac{(1-D)}{\pi} I_{out(peak)} V_{F(Diode)} \tag{A.19}$$

$$P_{cond(D_3)} = \frac{(1-D)}{\pi} I_{out(peak)} V_{F(Diode)} \tag{A.20}$$

$$P_{cond(D_4)} = \frac{D}{\pi} I_{out(peak)} V_{F(Diode)}. \tag{A.21}$$




(a) Driven with a positive input voltage

(b) Free-wheeling with a positive input voltage

(c) Driven with a negative input voltage

(d) Free-wheeling with a negative input voltage

Figure A.2: AC-to-AC converter driving and free-wheeling conduction paths for each switching state

The maximum conduction losses for $T_1$, $T_4$, $D_1$ and $D_4$ happen when the duty cycle is one, while the maximum losses for $T_2$, $T_3$, $D_2$ and $D_3$ occur when the duty cycle is zero. However, the total conduction losses for the combined switches will remain constant for every duty cycle.

By substituting the respective maximum values for $D$, $I_{out(peak)} = \sqrt{2}(100)(1.15)$ A, $V_{on(IGBT)} = 2.9$ V and $V_{on(diode)} = 1.9$ V the maximum conduction loss per IGBT and diode becomes

$$P_{cond(max)IGBT} = 150 \text{ W} \tag{A.22}$$

and

$$P_{cond(max)Diode} = 98.3 \text{ W}. \tag{A.23}$$

According to the switching states in Figure A.2, only two IGBTs and two diodes conduct at a time. The total conduction losses, calculated at a duty cycle of $D = 0.5$, is therefore

given by

$$\begin{aligned} P_{cond(total)} &= P_{cond(T_1)} + P_{cond(T_3)} + P_{cond(D_2)} + P_{cond(D_4)} \\ &= P_{cond(T_4)} + P_{cond(T_2)} + P_{cond(D_1)} + P_{cond(D_3)} \\ &= 2\,(75\text{W} + 49.2\text{ W}) \\ &= 496\text{ W}. \end{aligned} \tag{A.24}$$

### Switching Losses

The switching losses in each IGBT can be calculated by using the turn-on and turn-off energy, $E_{on}$ and $E_{off}$, given in the device datasheet [73], [79]. The values for $E_{on}$ and $E_{off}$ is given for a specific voltage with a specific collector current. However, the driving voltage $V_d$ and collector current $I_c$ are both sinusoidal and are given by

$$V_d(t) = V_d \sin(\omega_0 t) \tag{A.25}$$

and

$$I_c(t) = I_c \sin(\omega_0 t) \tag{A.26}$$

with

$$\begin{aligned} \omega_0 &= 2\pi f_0 \\ &= 2\pi 50\text{ rad/s}. \end{aligned} \tag{A.27}$$

Since the voltage and current change over time, a normalised value for the turn-on and turn-off energy is needed to scale the energy according to the current and voltage at each switching period. If the SKM600-GA167D IGBT from SEMIKRON is used, the normalised energy becomes

$$\begin{aligned} E_{nor} &= \frac{E_{on} + E_{off}}{V_{cc} I_c} \\ &= \frac{80\text{ mJ} + 45\text{ mJ}}{1200\text{V} \times 100\text{A}} \\ &= 1.0416 \times 10^{-6} \end{aligned} \tag{A.28}$$

where $V_{cc}$ and $I_c$ are given on the data sheet at which the turn-on and turn-off energy is measured. The energy dissipated in one IGBT during the $i$'th switching period due to switching, can be approximated [73] by

$$\begin{aligned} E_{i(switch)} &\approx V_d(t_i) \times I_c(t_i) \times E_{nor} \\ &= V_d \sin(\omega_0 t_i) I_c \sin(\omega_0 t_i) E_{nor} \\ &= V_d I_c E_{nor} \sin^2(\omega_0 t_i). \end{aligned} \tag{A.29}$$

The average power dissipated due to switching over half a period of $T_0$ is given by

$$\begin{aligned} P_{switch} &= \frac{1}{T_0}\sum_{i}^{N} E_{i(switch)} \\ &= \frac{1}{T_0 T_s}\sum_{i}^{N} V_d I_c E_{nor} \sin^2(\omega_0 t_i)\cdot T_s \\ &\approx \frac{I_c V_d E_{nor}}{T_0 T_s}\int_0^{\frac{T_0}{2}} \sin^2(\omega_0 t)\mathrm{d}t \\ &\approx \frac{1}{4} I_c V_d E_{nor} f_s \qquad \text{(A.30)} \\ &\approx \frac{1}{4}(162.6\text{A})(898\text{V})(1.0416\times 10^{-6})(10\ \ \text{kHz}) \\ &\approx 380\text{W}. \qquad \text{(A.31)} \end{aligned}$$

Only two IGBTs are switched at time and the total power dissipation as a result of switching is therefore given by

$$\begin{aligned} P_{switch(total)} &= 2\times P_{switch} \\ &= 2\,(380\ \text{W}) \\ &= 760\text{W}. \qquad \text{(A.32)} \end{aligned}$$

The combined losses of all the IGBTs and free-wheeling diodes in each AC-to-AC converter module is calculated by adding the total conduction and switching losses together,

$$\begin{aligned} P_{loss(total)} &= P_{cond(total)} + P_{switch(total)} \\ &= 496\text{W} + 760\text{W} \\ &= 1.256\ \text{kW}. \qquad \text{(A.33)} \end{aligned}$$

For the purpose of thermal design, the maximum losses that can be incurred in an IGBT is taken as the maximum conduction losses in (A.22) together with the switching losses in (A.31),

$$\begin{aligned} P_{IGBT(max)} &= P_{cond(\max)IGBT} + P_{switch} \\ &= 150\ \text{W} + 380\ \text{W} \\ &= 530\ \text{W} \qquad \text{(A.34)} \end{aligned}$$

while the maximum losses per diode is simply the maximum conduction losses given in (A.23). The nominal power throughput of each AC-to-AC converter module is given by

$$\begin{aligned} P_{converter} &= V_{out} I_{out} \\ &= (635\ \text{V})(100\ \text{A}) \\ &= 63.5\text{kW}. \qquad \text{(A.35)} \end{aligned}$$

Using (A.33) and (A.35), the efficiency of the AC-to-AC converter can be calculated,

$$\begin{aligned}\eta &= \frac{P_{converter} - P_{loss(total)}}{P_{converter}} \times 100 \\ &= \frac{63.5 \text{ kW} - 1.256\text{kW}}{63.5 \text{ kW}} \times 100 \\ &= 98 \text{ \%}. \end{aligned} \tag{A.36}$$

### A.3.3 Thermal design for IGBT's

The losses incurred by the IGBTs and diodes generate heat that must be disposed of. Each semiconductor device has a maximum allowed junction or core temperature that may not be exceeded. A thermal analysis is done to ensure that the heat generated at the core is effectively conducted away from the junction and dissipated into the atmosphere using an appropriate heatsink and cooling. The P16/360F forced air-cooled heatsink [92] from SEMIKRON is considered for the prototype and verified in this section.

The ability to conduct heat energy is modelled by a thermal resistance, $R_\theta$, which is defined in units of Kelvin per Watt (K/W). The thermal resistance is used to calculate the change in temperature when a certain amount of power is transferred and is given by [8],

$$\begin{aligned}\Delta T &= T_b - T_a \\ &= P \times R_\theta. \end{aligned} \tag{A.37}$$

A model, indicating the temperatures and thermal resistances, is shown in Figure A.3. The IGBT and diode junction temperatures are given by $T_{vj(I)}$ and $T_{vj(D)}$ respectively. The thermal resistance ($R_\theta$) between the IGBT junction and the outside of the casing is given by $R_{\theta(jc)I}$. Likewise, the diode's junction-to-case thermal resistance is given by $R_{\theta(jc)D}$. From the figure it is shown that each IGBT and diode pair share a common case temperature, $T_{case}$. Likewise, the thermal resistance from case-to-sink is given by $R_{\theta(cs)}$ and from sink-to-ambient by $R_{\theta(sa)}$. All four IGBT packages are mounted onto a single heatsink with a common sink temperature, $T_{sink}$. The IGBTs and diodes each have a maximum junction temperature $T_{vj}$ of 150°C which may not be exceeded. The maximum case temperature $T_{case}$ is determined by calculating the change in temperature from junction to case when maximum losses are incurred. The losses in the IGBT are far more than the losses in the diode and since the diode and IGBT are connected in anti-parallel, only one of the two will dissipate energy at a time. The case temperature is therefore calculated for maximum IGBT losses only. Using the losses calculated in (A.34) together with a thermal resistance $R_{\theta(jc)I}$ of 0.44 K/W and a junction temperature of

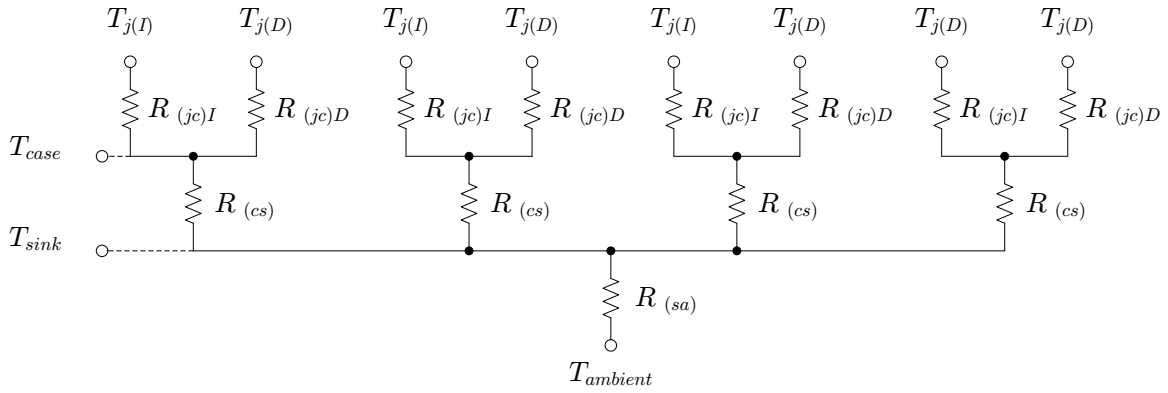



Figure A.3: Model of the thermal resistances and temperatures of four IGBTs with free-wheeling diodes, mounted onto a single heatsink.

150°C, the case temperature is calculated by rewriting (A.37) for $T_a$,

$$\begin{aligned} T_{case} &= T_{vj(i)} - P_{IGBT(max)} R_{\theta(jc)I} \\ &= 150°\text{C} - (530\ \text{W})(0.044\ \text{K/W}) \\ &= 126.7°\text{C}. \end{aligned} \tag{A.38}$$

The maximum heatsink temperature is calculated in the same manner as (A.38). Using a thermal resistance $R_{\theta(cs)}$ of 0.038 K/W, results in a heatsink temperature of

$$\begin{aligned} T_{\text{sink}} &= T_{case} - P_{IGBT(max)} R_{\theta(cs)} \\ &= 133.3°\text{C} - (530\ \text{W})(0.038\ \text{K/W}) \\ &= 113.2°\text{C}. \end{aligned} \tag{A.39}$$

Since all four IGBTs are mounted onto the same heatsink, the power transferred from heatsink to ambient equals the combined losses of all the dissipating IGBTs and diodes calculated in (A.33). An appropriate heatsink is chosen by calculating the required sink-to-ambient thermal resistance, $R_{\theta(sa)}$, needed to ensure that the sink temperature remains low enough for the amount of power dissipated. Rewriting (A.37) for $R_\theta$ and taking the ambient temperature as 50°C, the minimum thermal resistance required to ensure safe operation is given by

$$\begin{aligned} R_{\theta(sa)} &\leqslant \frac{T_{sink} - T_{ambient}}{P_{loss(total)}} \\ &\leqslant \frac{113.2°\text{C} - 50°\text{C}}{1.256\ \text{kW}} \\ &\leqslant 0.050\ \text{K/W}. \end{aligned} \tag{A.40}$$

The graph in Figure A.4 shows a linearised approximation of the IGBT junction temperature versus current for various values of $R_{\theta(cs)}$. The P16/360F forced air-cooled heatsink from SEMIKRON has a steady state thermal resistance of 0.0322 K/W which should be sufficient for the prototype setup. Figure A.5 shows the expected junction and heatsink

temperature versus collector current for the P16/360F heatsink model at an ambient temperature of 50°C.

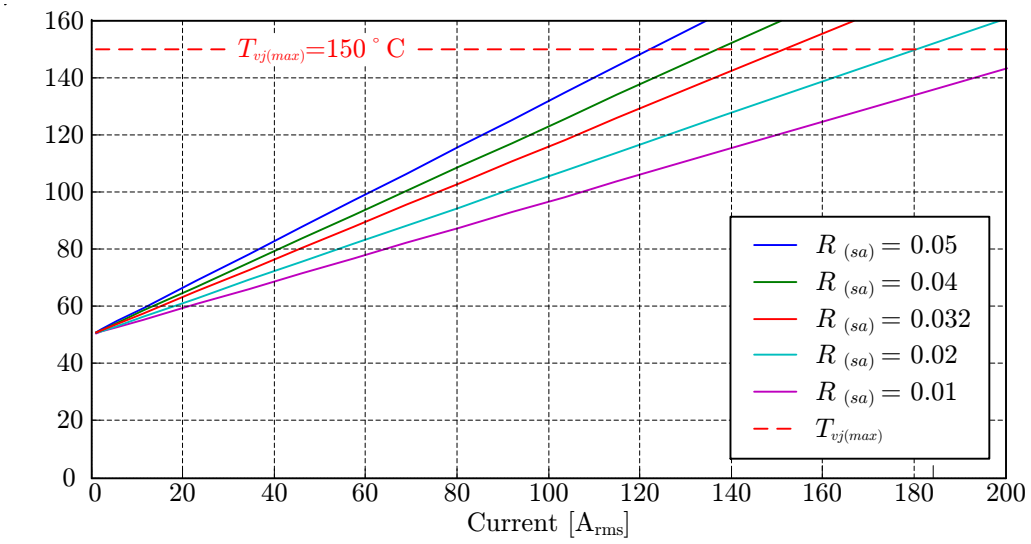



Figure A.4: IGBT Junction temperature vs. collector current for various heatsink-to-ambient thermal resistance values.

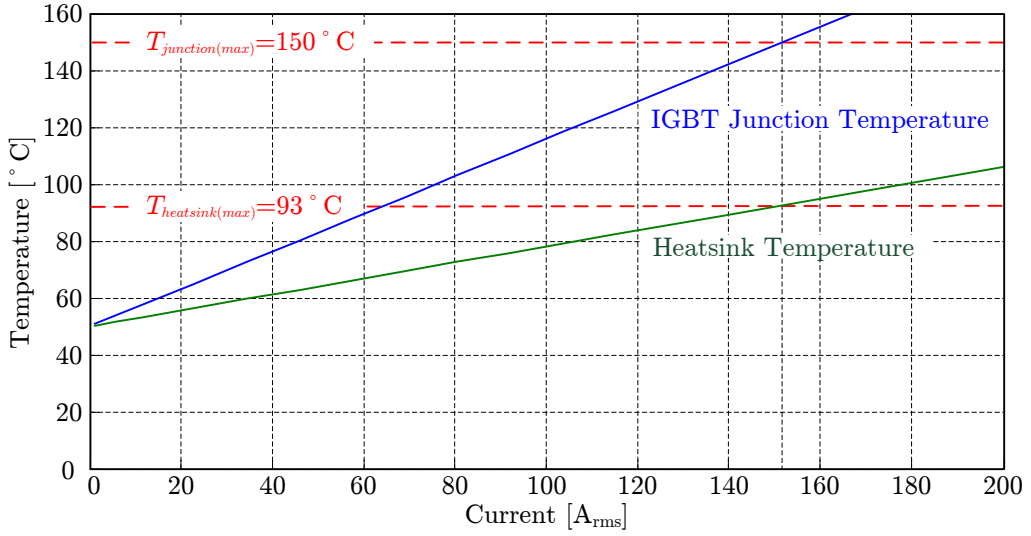



Figure A.5: Heatsink and IGBT junction temperature vs. current for the P16/360F forced air-cooled heatsink.

### A.3.4 Filter Inductor Design

The AC-to-AC converter can be seen as consisting of two synchronous buck converters, one for a positive and one for a negative terminal voltage which simplifies the filter design to that of a simple buck converter. The minimum value for the filter inductor in terms of

maximum current ripple is given by [8],

$$L \geqslant \frac{\mathrm{V}_{s1(\max)} T_s}{4\Delta I_{L(max)}}. \tag{A.41}$$

The specifications require a current ripple of no more than 30%. The maximum change in output current is therefore taken as 30% of the peak value,

$$\begin{aligned} \Delta I_{L(max)} &= \sqrt{(2)}(100\mathrm{A}_{rms})(0.3) \\ &= 42.4 \text{ A}. \end{aligned} \tag{A.42}$$

For a frequency of 10 kHz, the period is $T_s = 100\mu$s. The maximum output voltage of the AC-to-AC converter is the maximum input voltage across the secondary winding, $\mathrm{V}_{s1(max)} = 898$V. Substituting these values into (A.41), gives the minimum inductor value of

$$\begin{aligned} L &\geqslant \frac{(898 \text{ V})(100\mu s)}{4(42.4 \text{ A})} \\ &\geqslant 530 \ \mu\text{H}. \end{aligned} \tag{A.43}$$

The filter inductor has to be realised using a compact and light weight design. For this reason an inductor using the Kool M$\mu$ E-shape core, model 00K160LE026, from Magentics is used. The inductor consists of 16 E-cores, eight at the top and eight at the bottom. The physical dimensions amount to a height of 76 mm, a width of 160 mm and a length of 158.4 mm. There are 28 windings, consisting of seven parallel strands, where each strand has a diameter of 1.8 mm. This amounts to a measured inductance between 530 $\mu$H and 600 $\mu$H. For the purposes of calculation, the inductance is taken as the minimum value of 530 $\mu$H.

### A.3.5 Filter Capacitor Design

The maximum allowed voltage ripple is specified to be no greater than 1%. This results in a maximum change in voltage with a positive and negative deviation of

$$\begin{aligned} \Delta \mathrm{V}_{out(max)} &= (1\%)(\mathrm{V}_{s1}) \\ &= (0.01)(898 \text{ V}) \\ &= 8.98 \text{ V}. \end{aligned} \tag{A.44}$$

The minimum value for the filter capacitor of a buck converter in terms of maximum change in voltage and current is given by [8]

$$C \geqslant \frac{T_s \Delta I_{o(max)}}{8\Delta V_{o(max)}}. \tag{A.45}$$

Substituting $\Delta I_{o(max)}$ from (A.42) and $\Delta V_{o(max)}$ from (0.43) for a switching frequency of 10 kHz, gives us a minimum capacitor value of

$$\begin{aligned} C &\geqslant \frac{100\mu s(42.4)}{8(8.98)} \\ &\geqslant 59\mu F. \end{aligned} \tag{A.46}$$

Considering the availability of capacitors, the 440 $V_{rms}$, 50 $\mu$F, model: 01-05-0128, capacitor from Afcap is chosen. By placing two capacitors in series, the voltage rating becomes 880 $V_{rms}$ with a resulting capacitance of 25 $\mu$F. In order to satisfy the minimum value of 59 $\mu$F, three of these capacitor pairs can be placed in parallel which amounts to a total capacitance of 75 $\mu$F. The output filter's cut-off frequency should by high enough for a 50 Hz sine wave to pass without any significant attenuation. However, the cut-off frequency should also be low enough to sufficiently attenuate the switching frequency. If the minimum design values are maintained, the filter cut-off frequency should be satisfactory. Taking the filter capacitor value as 75 $\mu$F and the filter inductor value as 530 $\mu$H, the filter cut-off frequency is verified as

$$\begin{aligned} f_c &= \frac{1}{2\pi\sqrt{LC}} \\ &= \frac{1}{2\pi\sqrt{(530\mu\text{H} \times 75\mu\text{F})}} \\ &= 798 \text{ Hz} \end{aligned} \tag{A.47}$$

which is sufficient for the design requirements.

It is assumed that the average inductor current flows through the load and the ripple component through the filter capacitor. The current ripple is at a maximum when the change in inductor current, $\Delta I_L$ and the input voltage, $\Delta V_{s1}$ is at a maximum. The equation for the maximum RMS capacitor current is given by [8],

$$I_{C(rms)} = \sqrt{\frac{1}{T_s}\int_0^{\frac{T_s}{2}} \left(\frac{2(\Delta I_{L(max)})}{T_s}\cdot t - \frac{\Delta I_{L(max)}}{2}\right)^2 \mathrm{d}t + \frac{1}{T_s}\int_{\frac{T_s}{2}}^{T_s} \left(\frac{-2(\Delta I_{L(max)})}{T_s}\cdot t + \frac{3(\Delta I_{L(max)})}{2}\right)^2 \mathrm{d}t.} \tag{A.48}$$

By substituting $\Delta I_{L(max)}$ from (A.42), into (A.48) for a switching frequency of 10 kHz, the RMS capacitor current becomes

$$I_{C(rms)} = 12.23\text{A}. \tag{A.49}$$

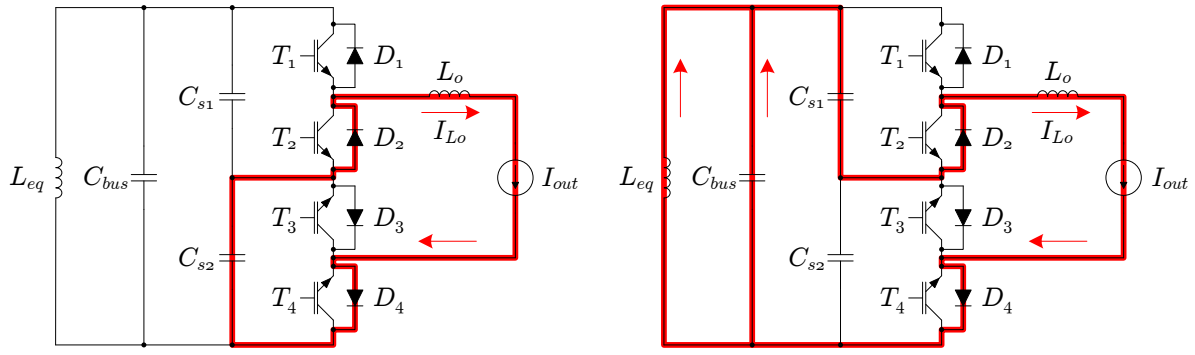
### A.3.6 IGBT Snubber Capacitor Design

Two snubber capacitors, $C_{s1}$ and $C_{s2}$, are placed across each buck converter to solve the commutation problems usually associated with AC-to-AC converters. During dead time,

when all four IGBTs are switched off, a return path has to exist for the current through the filter inductor $L_o$. For a positive inductor current, two return paths are possible. Figure A.6 (A) shows the shortest return path through snubber capacitor $C_{s2}$ and diodes $D_2$ and $D_4$. Although the shorter return path exists, a second return path is created as a result of line and parasitic inductances. The second return path is created through snubber capacitor $C_{s1}$ and diodes $D_2$ and $D_4$, as shown in Figure A.6 (B).

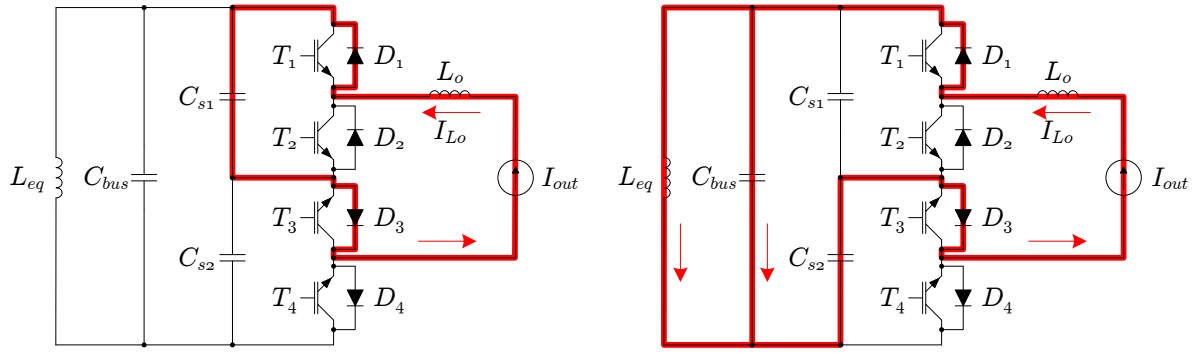
Likewise, for a negative filter-inductor current, two return paths are created as shown in Figure A.7 (A) and (B). The shorter return path is created through snubber capacitor $C_{s1}$ and diodes $D_1$ and $D_3$ while the longer return path is created through snubber capacitor $C_{s2}$ and diodes $D_1$ and $D_3$.

It is important to note that the equivalent transformer leakage inductance is not taken into account during the snubber design. The return path for the transformer leakage inductance will be addressed in the bus capacitor design in the next section. The




(Bottom snubber capacitor) (Top snubber capacitor)

Figure A.6: Return paths for positive filter inductor current.




(Top snubber capacitor) (Bottom snubber capacitor)

Figure A.7: Return paths for negative filter inductor current

current through a capacitor is a function of change in the capacitor voltage. Therefore, as the capacitor allows current to pass through, the voltage across the capacitor will increase.

The capacitor values should therefore be designed that the rise in voltage during dead time remains below the maximum allowed bus voltage.

Dead time can safely be estimated for a maximum of 2$\mu$s.The maximum bus voltage under normal conditions is 898 $V_{peak}$ with a $\pm$10 V deviation which results in a maximum operating voltage of 988 $V_{peak}$. The maximum allowed bus voltage is limited by the components with the lowest voltage rating which, in this case, is specified to be a minimum of 1 700 $V_{rms}$ . By adding a sufficient safety factor, the maximum allowed bus voltage is chosen as 848 $V_{rms}$ which has a peak value of 1 200 $V_{peak}$. If the maximum bus voltage under normal operating conditions is 988 $V_{peak}$, the allowed change in voltage becomes

$$\begin{aligned}\Delta V_{t(\max)} &= V_{t(max)} - V_{s1(max)} \\ &= 1200 V_{peak} - 988 V_{peak} \\ &= 212 \text{ V}. \end{aligned} \tag{A.50}$$

The maximum output current under normal conditions is 100 $A_{rms}$ $\pm$10%, which results in a peak current of

$$\begin{aligned} I_{out(max)} &= (1.1)\sqrt{2}(100 \text{ A}) \\ &= 155.6 \text{ A}_{peak}. \end{aligned} \tag{A.51}$$

The equation for the current through a capacitor in terms of change in voltage and time is approximated by

$$I_c \approx C\frac{\Delta V}{\Delta T}. \tag{A.52}$$

Using Equation (A.52) and rewriting for $C$, the minimum snubber capacitor value is calculated as

$$\begin{aligned} C_{s1} &= C_{s2} \\ &\geqslant I_{out(max)} \frac{\Delta T_{off}}{\Delta V_{t(max)}} \\ &\geqslant 155.6 \text{ A} \cdot \frac{2\mu\text{s}}{212 \text{ V}} \\ &\geqslant 1.46\mu\text{F}. \end{aligned} \tag{A.53}$$

The IGBTs are limited to 1 700 V and it would be sufficient to choose a capacitor of the same voltage rating. Each snubber capacitor can be realised by placing three 0.47 $\mu$F capacitors in parallel. The capacitor, model E62.C58-471E40, from Elektronicon has an AC voltage rating of 1 700 VAC and is ideal for this application. The total snubber capacitance then becomes 1.41 $\mu$F, which is close enough to the required value.

### A.3.7 Input-Bus Capacitor Design

During normal switching, the bucking converter is in either an *on* or *off* state. During an *off*-state, either $T_1 = off$ or $T_4 = off$ while the other IGBTs remain on. The *off*-state

allows the output current to free-wheel, but gives no return path for the transformer leakage inductance current. The snubber capacitors, discussed in the previous section, are designed to provide a return path for only a certain amount of time, $2\mu$s. However, the converter switches at a frequency of 10 kHz, which means that the converter can be in the *off*-state for 100 $\mu$s. As a result, the bus voltage can rise far beyond the rated specifications if no additional return path is provided. In order to address this problem, a bus capacitor $C_{bus}$ is placed across the input bus as shown in Figure 4.3.

The minimum value for $C_{bus}$ can be calculated by substituting Equations (A.50) and (A.51) into (A.53) and taking $\Delta T_{off} = 100\mu$s,

$$\begin{aligned} C_{bus} &\geqslant I_{out(max)} \frac{\Delta T_{off}}{\Delta \mathrm{V}_{t(max)}} \\ &\geqslant 155.6 \text{ A} \cdot \frac{100\mu\text{s}}{212 \text{ V}} \\ &\geqslant 73.4\mu\text{F}. \end{aligned} \tag{A.54}$$

The bus capacitor can be practically realised by using a single metal-can capacitor from the E62 heavy duty AC/AC capacitor range from Elektronicon. The voltage rating of the IGBTs are limited to 1 700 VAC and it is therefore safe to choose a bus capacitor with a voltage rating of 2 000 VAC. The capacitor, model E62.S32-903C60, is single metal-can capacitor with a diameter of 136 mm, a length of 245 mm, a capacitance of 90 $\mu$F, an AC voltage rating of 2 000 V and a current rating of 100 A. The compact design and high voltage rating makes it an ideal choice without having to use bulky series-stacked capacitors.

### A.3.8 Design Verification by Simulation

The design of the AC-to-AC converter is verified by simulation using Ansoft's Simplorer 8 software package. The simulation is set up according to the schematic diagram given in Figure A.8 and the component values in Table A.2. The AC-to-AC converter is simulated with a step size of 100 ns using open-loop PWM control control at 10 kHz. The simulation parameters are chosen for the maximum allowed input voltage and load current which are

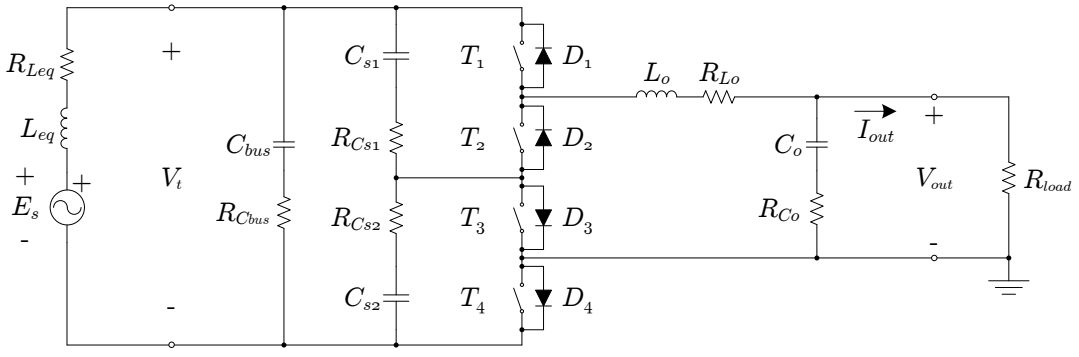



Figure A.8: Circuit diagram used for simulating the AC-to-AC converter.

Table A.2: Component values used in the simulation of the AC-to-AC Converter.

| Component | Value |
|---|---|
| $E_{s1}$ | 698.5 $V_{rms}$ |
| $L_{eq(\max)}$ | 1.01 mH |
| $L_o$ | 530 $\mu$H |
| $C_{bus}$ | 90 $\mu$F |
| $C_o$ | 75 $\mu$F |
| $C_{s1}$ | 1.41 $\mu$F |
| $C_{s2}$ | 1.41 $\mu$F |
| $Z_{load}$ | 3.5 $\Omega$ |

taken as 10% above the nominal values. Two types of dead time are implemented in the simulation. The first type of dead time involves only two complementary switching pairs at a time, $T_1$ and $T_2$ or $T_3$ and $T_4$, when there is no voltage sign change. The second type of dead time involves all the switching elements and happens when the sign of the bus voltage ($V_t$) changes.

**Verifying the topological behaviour.**

*Filter Capacitor:* In order to verify the topological switching and expected output voltage for both negative and positive input voltages, the simulation is set up with an open-loop duty cycle of 0.5 and a resistive load of 3.5 $\Omega$. The simulation results for the input voltage versus output voltage is shown in Figure A.9. The peak input voltage is 988 V and the expected output voltage is 494 V. However, due the voltage drop across the leakage inductance and filter inductor, the peak output voltage becomes 478 V. The filter capacitor was chosen as 75 $\mu$F, which is 16 $\mu$F larger than the minimum value in (A.46). The resulting output voltage ripple, $\Delta$V, is 8 V and amounts to approximately 0.8% of the input voltage. The simulation results for the output voltage therefore compares better than the maximum ripple specification of 1%.

*Filter Inductor:* The simulation results for the filter inductor current and output current are given in Figure A.10. The filter inductor is an important component in limiting the current that passes through the filter capacitor. It is therefore important to verify the maximum current ripple to ensure safe operation. The maximum current ripple at nominal values are designed to be 30%. The maximum filter inductor ripple occurs at a duty cycle of 0.5, as shown in Figure A.10. From the figure we see that the maximum change in current, $\Delta I_{Lo}$, is 47 A which amounts to a 33% current ripple. However, the simulation is done for an input voltage that is 10% above the nominal value, which corresponds to the 10% increase seen in the simulation.

*Bus Capacitor:* The bus capacitor is used to provide a return path for the current through the transformer leakage inductance. The size of the capacitor determines the amount with which the bus voltage changes when the system is switching. The capacitor

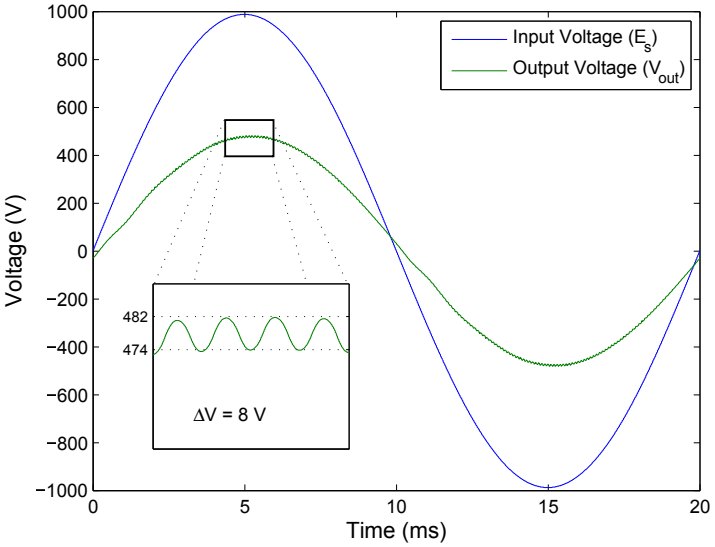



Figure A.9: Simulation results of the Input Voltage ($E_s$) and Output Voltage ($V_{out}$) waveforms for PWM switching at 10 kHz with a duty cycle of 0.5 .

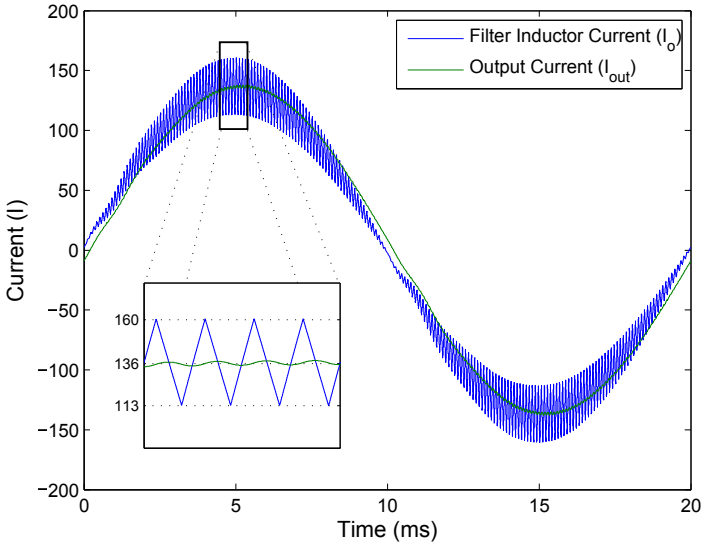



Figure A.10: Simulation results of the Inductor Current ($I_o$) and Output Current ($I_{out}$) waveforms for PWM switching at 10 kHz under full load conditions with a duty cycle of 0.5 .

was designed to keep the bus voltage below 1 200 V for a maximum input current of 110 $A_{rms}$ while the switches are off for a maximum time interval of 100 $\mu$s. In Section A.3.7, the bus capacitor's value was chosen as 90 $\mu$F which is 16.6 $\mu$F more then the calculated minimum value. The bus voltage, ripple component and input current are shown in Figure A.11. The figure shows a voltage ripple of 38 V for a duty cycle of 0.5 with an input current of 66 A. This would amount to a rise in bus voltage of 76 V if the system suddenly remained in the off state for 100 $\mu$s. Comparing the rise in voltage with the input current to Equation A.52, we see that the bus capacitor is sufficient in

maintaining a safe bus voltage when switching under all normal conditions.

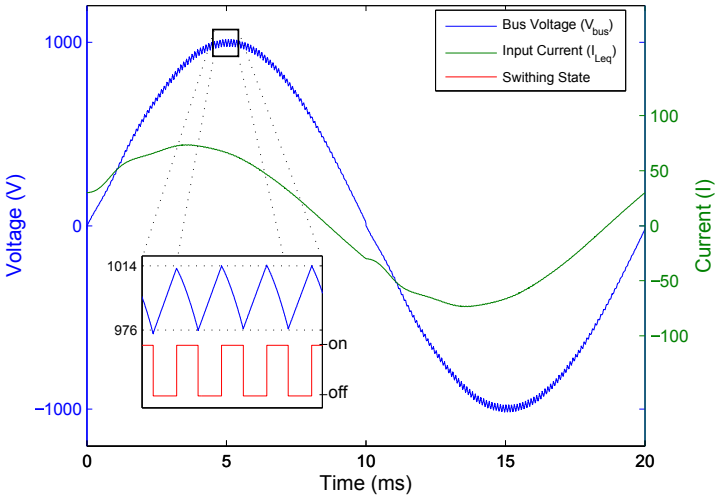



Figure A.11: Simulation results of the Bus Voltage ($V_t$) and input current ($I_{Leq}$) waveform and the AC-to-AC converter's switching state for PWM switching at 10 kHz under a full load current ($I_{out}$) of 100 $A_{rms}$ and an Input Voltage ($E_s$) of 698.5 $V_{rms}$ with a duty cycle of 0.5 .

### Verifying the snubber capacitors

The snubber capacitors provide a return path for the current through the filter inductor $L_o$ when all four switches are turned off during dead time. This dead time is applied when the input-bus voltage changes sign and commutation is changed from the one pair of switches to the other. As the snubber capacitors pass current, their voltages rise and this rise is dependent on the amount of current flowing through the filter inductor.

The first simulation is set up with an input voltage of 698 $V_{rms}$, a resistive load of 3.5 Ω and a duty cycle of 0.5. If the voltage and current is in phase, the current through $L_o$ will also be zero when the voltage passes a zero-crossing. The simulation result of the snubber capacitor ($C_{s1}$) voltage is shown in Figure A.12. For a resistive load it is therefore shown that the snubber capacitor has no significant change in voltage at the zero-crossing.

The second simulation is set up with a resistive-inductive load of $3.5\angle{-45}°$ Ω for the same input voltage and duty cycle. In Figures A.13b and A.14b it is shown that there are two return paths for the current. The one return path is through snubber capacitor $C_{s1}$ and the other through snubber capacitor $C_{s2}$. Looking at the direction of flow of the current, we see that $C_{s1}$ will charge in the positive direction while $C_{s2}$ will charge in the negative direction. Since the two snubber capacitors are connected in series and placed in parallel to the bus capacitor, it is expected that the voltages across both would balance to approximately the same values. This is seen to be true in Figures A.13a and A.14a.

The voltage across $C_{s1}$ charges to +90 V while the voltage across $C_{s2}$ charges to -90 V. In (A.50), the maximum rise in voltage is calculated to be no more than 212 V under worst case conditions. Comparing the snubber capacitor voltages to the design specifications, we see that the rise in voltage for the chosen snubber capacitors is more than sufficient for protecting the IGBTs even under worst case conditions.

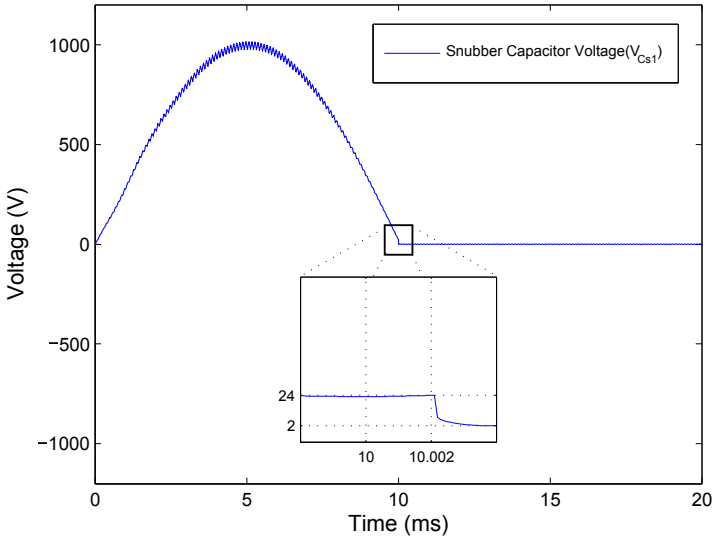
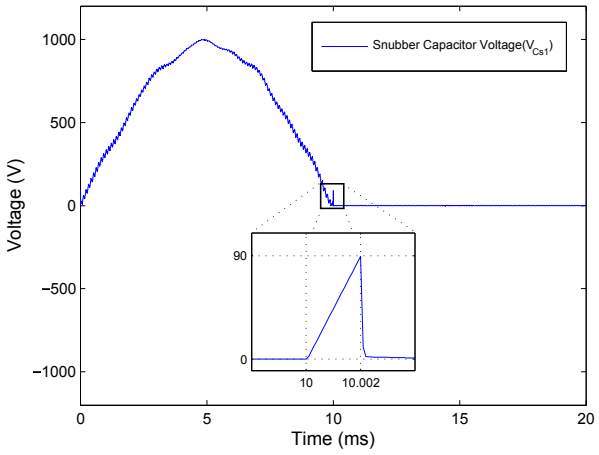
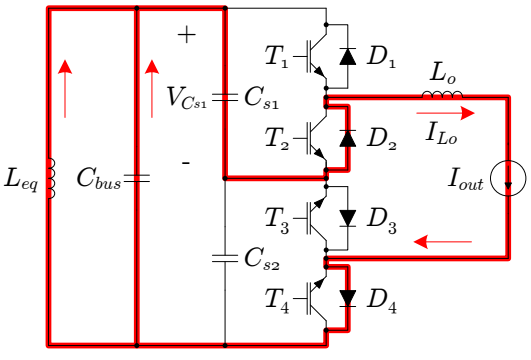



Figure A.12: Simulation results of the Snubber Capacitor Voltage ($V_{Cs1}$) waveform during dead time for a resistive load with PWM switching at 10 kHz under a full load current ($I_{out}$) of 100 $A_{rms}$ and an Input Voltage ($E_s$) of 698.5 $V_{rms}$ with a duty cycle of 0.5 .

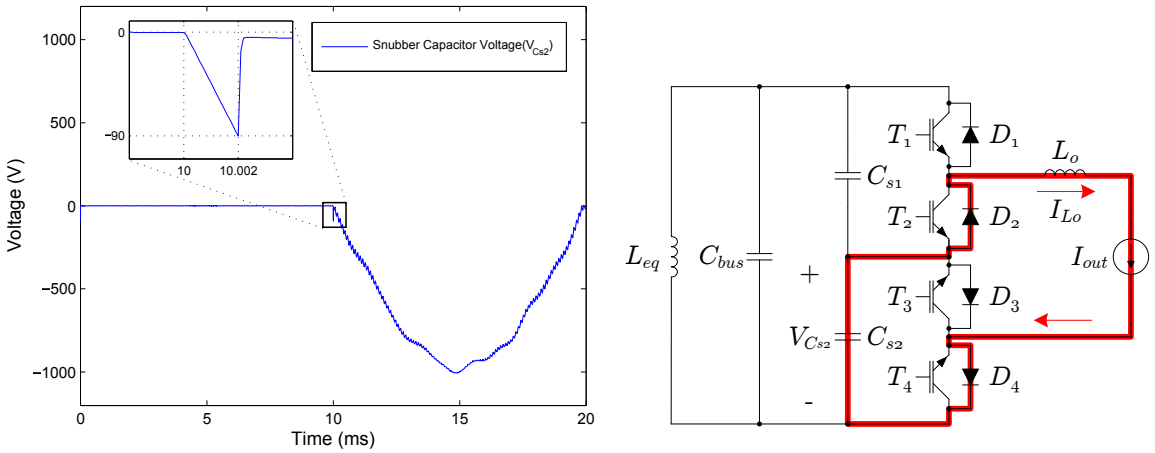



(a) Snubber Capacitor Voltage ($V_{Cs1}$) waveform.




(b) Dead time current conduction path.

Figure A.13: Simulation results of the Snubber Capacitor Voltage ($V_{Cs1}$) during dead time for a pure inductive load with PWM switching at 10 kHz under a full load current ($I_{out}$) of 100 $A_{rms}$ and an Input Voltage ($E_s$) of 698.5 $V_{rms}$ with a duty cycle of 0.5 .




(a) Snubber Capacitor Voltage ($V_{Cs2}$) waveform. (b) Dead time current conduction path.

Figure A.14: Simulation results of the Snubber Capacitor Voltage ($V_{Cs2}$) during dead time for a pure inductive load with PWM switching at 10 kHz under a full load current ($I_{out}$) of 100 $A_{rms}$ and an Input Voltage ($E_s$) of 698.5 $V_{rms}$ with a duty cycle of 0.5 .

### A.3.9 Summary

The AC-to-AC converter can be seen as two synchronous buck converters, connected in such a way to allow for both positive and negative input voltages. This section included the design and selection of the proper IGBTs, a thermal analysis and heatsink design as well as the design of an output *LC* filter, IGBT snubber capacitors and input-bus capacitor.

To select the proper IGBTs, the power ratings and losses associated with each switching element was calculated. The IGBT, model SKM600-GA167D, from SEMIKRON consists of one IGBT and one free-wheeling diode in a single package and was selected for use as the switching elements. The maximum losses incurred in an IGBT amounted to 530 W while the maximum losses in a diode amounted to 98.3 W. The total losses of all the IGBTs together, following the switching pattern, amounted to 1.256 kW at a total efficiency of 98%.

The losses incurred by the IGBTs and diodes generate heat that must be disposed of. A model, indicating the temperatures and thermal resistances between the IGBTs, the heatsink and the ambient were derived. It was shown that the thermal resistance of the heatsink should not be greater than 0.050 K/W and the P16/360F force air-cooled heatsink from SEMIKRON with a thermal resistance of 0.0322 K/W was chosen.

The *LC* filter was designed to limit the current ripple to 30% and the voltage ripple to 1%. The filter inductor value was calculated to be no less than 530 $\mu$H while the Kool M$\mu$ E-shape cores from Magnetics were used to realise a compact 530 $\mu$F inductor with dimensions (H)76 mm × (W)160 mm × (L)158.4 mm. A 75 $\mu$F filter capacitor was designed and realised by placing two 440 V, 50 $\mu$F capacitors from Afcap in series and connecting three of these pairs in parallel.

The commutation problems usually associated with AC-to-AC converters were solved by placing two snubber capacitors, $C_{s1}$ and $C_{s2}$ across each buck converter. The snubber capacitors provide a return path for the filter inductor current during dead time and was realised by placing three 1 700 V, 0.47 $\mu$F capacitors from Elektronicon in series.

Likewise, the bus capacitor $C_{bus}$ was designed to provide a return path for the current through the transformer leakage inductance $L_{eq}$ and limiting the rate of rise of the bus voltage when the converter is in the *off* state. The bus capacitor was designed and compactly realised by using a single 2 000 V, 90 $\mu$F capacitor from Elektronicon's E62 Heavy Duty AC/AC range.

Simulation results verified the theoretical design of the output $LC$ filter, the snubber capacitor behaviour as well as the bus capacitor voltage under worst case conditions. Results showed that the filter complied with the required specifications and that the bus and snubber voltages remained within safe limits during normal switching.

A summary of the components, selected values, manufacturers and models are given in Table A.3.

Table A.3: Summary of components and their designed values for the AC-to-AC converter.

| Component | Value | Manufacturer | Model |
|---|---|---|---|
| $T_1$, $T_2$, $T_3$, $T_4$ | 1 700 V, 660 A | Semikron | SKM600-GA167D |
| Heatsink | $R_\theta = 0.0322$ K/W | Semikron | P16/360F |
| $C_o$ | 75 $\mu$F = (50 $\mu$F & 50 $\mu$F) $\times$ 3 | Afcap | 01-05-0128 |
| $C_{s1}, C_{s2}$ | 1.41 $\mu$F = 0.47 $\mu$F $\times$ 3 | Elektronicon | E62.C58-471E40 |
| $C_{bus}$ | 90 $\mu$F | Elektronicon | E62.S32-903C60 |
| $L_o$ | 530 $\mu$F | Magnetic | 00K160LE026 E-cores |

# A.4 Design: Protection Mechanisms

## A.4.1 Overview

This section discusses the detail design of the protection mechanisms of the AC-to-AC converter. The protection mechanisms consist of four parts, the input-bus dump-crowbar, the output bypass-crowbar, the filter cut-out and the soft-start. The respective circuit elements are included in the circuit diagram of the AC-to-AC converter as shown in Figure 4.3. The input-bus dump-crowbar is given by thyristors $T_{d+}$ and $T_{d-}$, inductor $L_d$ and dump resistor $R_d$. The bypass-crowbar is given by thyristors $Tb+$ and $Tb-$ while the filter cut-out is given by IGBT pair $T_c$, inductor $L_b$ and bleed resistor $R_b$. Lastly, the soft-start is given by IGBT pair $T_{ss}$, limiting resistor $R_{ss}$ and limiting inductor $L_{ss}$.

Section A.4.2 discusses the detail design of the input-bus dump-crowbar and its driver hardware. The dump-crowbar is designed to protect the input-bus against over-voltage conditions by triggering thyristor $T_{d+}$ or $T_{d-}$ when over-voltage conditions occur. The energy of the condition is then dissipated using dump resistor $R_d$. A breakover-diode circuit for triggering the thyristors are discussed in the first part of the design followed by the design of the dump resistor and inductor. The design is concluded with the selection criteria for the thyristors and the design of the appropriate snubbers.

Section A.4.3 discusses the detail design of the bypass-crowbar. The bypass-crowbar is designed to protect the output of the AC-to-AC converter against over-voltage conditions and to provide an alternative path for fault currents. The thyristors are triggered using the same breakover-diode circuit as discussed in Section A.4.2. In the first part of the design, the proper thyristors and snubbers are selected. Thereafter the thyristor loss calculations are performed and the appropriate heatsink is designed.

Section A.4.4 discusses the detail design of the filter cut-out. The bypass-crowbar effectively short-circuits the filter capacitor when it is closed. For this reason, the filter cut-out is designed to protect the filter capacitor when the bypass is closed by discharging the capacitor through a bleeding resistor. The design includes the calculation of a sufficient bleed resistor, IGBT selection, loss calculations and thermal design.

The design of the soft-start is discussed in Section A.4.5. If a large voltage is applied across the input of the AC-to-AC converter when the bus capacitor is discharged, large inrush currents will occur as the bus capacitor is being charged. In order to to limit the inrush current and rate of rise of current ($\mathrm{d}i/\mathrm{d}t$), a soft-start mechanism is implemented.

Each of the protection mechanisms are evaluated by simulation in Section A.4.6 and summarised in Section A.4.8.

### A.4.2 Input-Bus Dump-Crowbar Design

The bus capacitor is designed to provide a return path for the transformer leakage inductance current when the converter is in the *off* state. If the system is operating at full load and a fault occurs such that the converter remains in the *off* state, there will be no sufficient return path for the current flowing through inductor $L_{eq}$. This will cause capacitor $C_{bus}$ to charge up, exceeding the component's rated voltage.

In order to prevent such over-voltage conditions, a dump-crowbar is implemented. The crowbar consists of two thyristors, $T_{d+}$ and $T_{d-}$, and dump resistor $R_d$, as shown in Figure 4.3. When an over-voltage condition occurs, one of the thyristors are triggered and a return path is created through the dump resistor and the free-wheeling diodes, $D_1$ and $D_2$ or $D_3$ and $D_4$. This will cause the bus capacitor to discharge through dump resistor $R_d$. However, the thyristor can only switch off when the current drops below its holding current, which will happen only when the bus voltage $V_t$ reaches a zero crossing. As a result, the transformer will continue to drive the dump resistor for the remainder of the voltage half-cycle, until a zero crossing is reached.

#### Dump resistor design

For a worst case scenario, resistor $R_d$ must be able to dump the energy contained in the bus capacitor as well as a complete half cycle of the sinusoidal bus voltage $E_s$. The maximum allowed input current during fault conditions should be limited to 150 $A_{rms}$. By choosing the maximum current as 150 $A_{rms}$ at a bus voltage of 1 200 V, the dump resistor value is calculated as

$$\begin{aligned} R_d &= \frac{V_{bus(max)}}{I_{bus(max)}} \\ &= \frac{1200\ \text{V}}{\sqrt{2}(150\text{A})} \\ &= 5.6\ \Omega \end{aligned} \tag{A.55}$$

When a fault occurs, bus capacitor $C_{bus}$ is charged up to 1 200 V before discharging. If

$$C_s = 91.4\mu F \tag{A.56}$$

the energy contained in the capacitor at 1 200 V is

$$\begin{aligned} E &= \frac{1}{2}CV^2 \\ &= \frac{1}{2}(91.4\mu)(1200)^2 \\ &= 65.8\ \text{J}. \end{aligned} \tag{A.57}$$

The $CR$ time constant, when a 5.6 Ω dump resistor is used, is given by

$$\begin{aligned}\tau &= CR \\ &= (91.4\mu F)(5.6\Omega) \\ &= 512\mu\text{s}. \end{aligned} \tag{A.58}$$

Assuming that the discharge is negligible after 5 time constants, the capacitor will discharge in

$$\begin{aligned} t_c &= \tau \times 5 \\ &= (512\mu\text{s})(5) \\ &= 2.56 \text{ ms} \end{aligned} \tag{A.59}$$

The energy dissipated by $R_d$ as a result of $E_s$ can be calculated by integrating the instantaneous power over one half cycle. The worst case transformer voltage, nominal voltage plus ten percent, can be described as a sinusoidal voltage source

$$E_s(t) = 990\sin(2\pi 50t) \tag{A.60}$$

and the power dissipated in the dump resistor as a result of $E_s(t)$ is given by

$$\begin{aligned} p(t) &= \frac{{E_s}^2(t)}{R_d} \\ &= \frac{(990\sin(2\pi 50t))^2}{5.6}. \end{aligned} \tag{A.61}$$

The energy dissipated by $R_d$ is therefore found by integrating (A.61) over one half-cycle of 10 ms,

$$\begin{aligned} E &= \int_0^{0.01} p(t)\text{dt} \\ &= \int_0^{0.01} \frac{(990\sin(2\pi 50t))^2}{5.6}\text{dt} \\ &= 875 \text{ J} \end{aligned} \tag{A.62}$$

The total power dissipation in $R_d$ is therefore the sum of (A.57) and (A.62) which results in a power dissipation of

$$E_{C(total)} = 940.8 \text{ J}. \tag{A.63}$$

The dump-crowbar is effectively connected in parallel with the bus capacitor. When the bus capacitor is discharged, the rate of rise of current ($\text{d}i/\text{d}t$) may exceed the critical rate of rise specified for the thyristor. As a result, the dump resistor has to include a certain amount of inductance to limit the rate of rise of current though the thyristor. This inductance is represented by inductor $L_d$, which is placed in series with the dump resistor $R_d$.

The critical rate of rise of current $(\mathrm{d}i/\mathrm{d}t)_{CR}$ for the thyristor and free-wheeling diodes are specified not to exceed 200 $\mu$s. If the bus capacitor is discharged from 1 200 V, the minimum inductance can be calculated as

$$\begin{aligned} L_d &\geqslant V_{max}\left(\frac{\mathrm{d}t}{\mathrm{d}i}\right)_{CR} \\ &\geqslant (1200\ \mathrm{V})\left(\frac{1}{200\mu\mathrm{s}}\right) \\ &\geqslant 6\ \mu\mathrm{H}. \end{aligned} \tag{A.64}$$

Taking a safety factor of two, the minimum series inductance for $L_d$ becomes

$$L_d \geqslant 12\mu\mathrm{H} \tag{A.65}$$

A single wire wound resistor with sufficient inductance can be used or alternatively, an inductor can be placed in series with the dump resistor to provide additional inductance as required.

### Thyristor selection criteria

The SKMT92/16E thyristor from SEMIKRON [3] is chosen and evaluated. The crowbar is typically triggered only once over an extended period. The thyristor is chosen with a sufficient voltage-blocking capability and current rating.

The crowbar is triggered when the bus voltage reaches 1 200 V. This requires a blocking voltage of 1 200 V with an added safety margin. The SKMT92/16E has a repetitive peak off-state and reverse blocking voltage of 1600 V, which adds a 400 V margin for safety.

For the 5.6 Ω dump resistor calculated in (A.55), the peak discharge current is 214 A. Once the thyristor is triggered, the equivalent sinusoidal voltage source ($E_s$) continues to drive the dump resistor until a zero crossing is reached. For a worst case scenario, the capacitor is completely discharged after which a complete half-cycle of the sinusoidal bus voltage is applied. The SKMT92/16E has a maximum continues RMS current rating ($I_{T(rms)}$) of 150 A, a 10 ms surge on-state current rating ($I_{TSM}$) of 2 000 A and an $i^2t$ rating of 20 000 $\mathrm{A}^2\mathrm{s}$. Since the crowbar is not continuously driven, only a single pulse of energy is dissipated at a time. The thyristor does not require a large heatsink and the metal of the converter housing should be sufficient for heat dissipation.

### Thyristor Snubber design

A snubber is needed to limit the rate of rise of voltages $(\mathrm{d}v/\mathrm{d}t)$ across the thyristor during device turn-off or during the forward blocking state [8]. A certain amount of inductance exists within the thyristor module itself as well as the circuit it is connected to. As a result, the current lags with respect to the voltage and that has to be taken into account during thyristor turn-off. After a voltage zero-crossing, the thyristor becomes

reverse biased while the current is still flowing in the forward bias direction. As the current reaches the zero-crossing, the thyristor already has an applied reverse voltage. This reverse voltage causes a reverse recovery current to flow while the thyristor junction is discharged. As the junction is discharged, a certain snap-off point occurs where the thyristor stops conducting in the reverse direction. The inductance in the system however does not allow the current to suddenly stop and an alternative path has to exist for the current to die away. For this reason a $RC$-snubber, $R_s$ and $C_s$ as shown in Figure A.16, is connected across the anode and cathode of the thyristor.

The values for the $RC$ snubber can be obtained by using empirical methods together with the availability of components in stock. A SPICE simulation can be set up for a $L$-$C$-$R$ loop with initial conditions according to the worst case reverse recovery voltage and current. The $L$ represents the parasitic inductance and $RC$ the snubber. Iterating through the component values in stock, sufficient values for the snubber are found and chosen as

$$C_s = 330 \text{ nF} \tag{A.66}$$

and

$$R_s = 68\ \Omega. \tag{A.67}$$

**Breakover-diode trigger design**

The thyristors are triggered using the breakover diode (BOD) circuit diagram in Figure A.16. A breakover diode is essentially a small thyristor consisting of a four layer structure without a gate connection [83]. The silicon layers are constructed in such a way that when the forward voltage exceeds the specified breakover voltage, a controlled turn-on is initiated. As a result, a BOD can be seen as a small self-triggering thyristor that triggers when its forward voltage exceeds the breakdown voltage. Like a thyristor, the BOD will continue to conduct until the current falls below the holding current threshold. As a result of the silicon structure, a BOD has an asymmetric structure [83] and cannot block a high reverse voltage. A soft recovery diode is therefore typically added in series to provide reverse blocking capabilities.

The BOD is connected across the anode and gate in series with a current-limiting resistor $R_2$. A low-pass filter consisting of $R_1$ and $C_1$ together with diode $D_2$ is added to block off any BOD displacement current caused by positive $\mathrm{d}v/\mathrm{d}t$. A voltage suppression diode $D_1$, is added to suppress unwanted voltages as a result of the current through the low-pass filter. A snubber capacitor and resistor, $C_s$ and $R_s$ is placed in parallel with the thyristor to limit $\mathrm{d}v/\mathrm{d}t$ as well as protection during turn-off.

When the forward voltage across the thyristor exceeds the BOD breakover voltage, the BOD closes and current is allowed to flow through $R_2$, $BOD$, $D_1$ and $D_2$ to the gate. As current passes through the gate, thyristor turn-on occurs and the forward voltage drops to the thyristor on-state voltage. The BOD will turn off as soon as the thyristor is turned

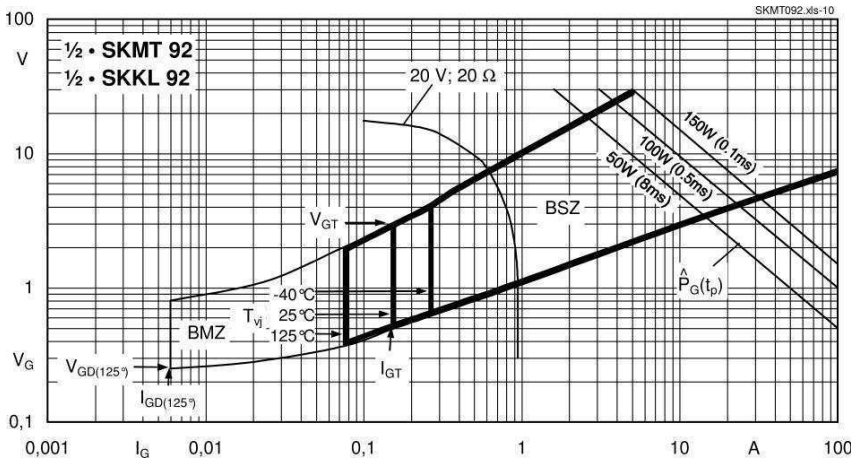



Figure A.15: SEMIKRON SKMT92 thyristor gate trigger characteristics [3].

on since the on-state voltage of the BOD is typically higher than that of the thyristor. A breakover diode from IXYS is chosen with a breakover voltage of $V_{bo} = 1\,200$ V and an *on*-state voltage of $V_T = 3.4$ V. A Zener diode with $V_z = 3.3$ V is chosen for $D_1$ and a soft recovery diode with forward voltage $V_F = 0.7$ V is chosen for $D_2$.

The gate trigger characteristics for the SKMT92 thyristor is shown in Figure A.15. The figure shows a graph of the gate voltage versus the gate current with two indicated regions. The first region is marked *BMZ*, which is a German acronym for *area of possible firing*. The second region is marked *BSZ*, which means *area of safe firing*. To ensure that the thyristor is turned on correctly, the gate voltage and current should fall within the *BSZ* zone. The line of optimal firing is given by the 20 V, 20 Ω line. From this information, the thyristor gate trigger current is chosen as $I_{GT} = 1$ A with at a gate trigger voltage of $V_{GT} = 5$ V, which falls safely within the *BSZ* zone.

The value for the current limiting resistor $R_2$ can be found by taking Kirchhoff's Voltage Law (KLV) around the anode-gate-cathode-anode loop,

$$V_{BO} - R_2 I_{GT} - V_{T(bod)} - V_Z - V_F - V_{GT} = 0 \tag{A.68}$$

and solving for $R_2$,

$$\begin{aligned} R_2 &= \frac{V_{BO} - V_{T(bod)} - V_Z - V_F - V_{GT}}{I_{GT}} \\ &= \frac{1200\text{ V} - 3.4\text{ V} - 3.3\text{ V} - 0.7\text{ V} - 5\text{ V}}{1\text{ A}} \\ &= 1.187\text{ k}\Omega. \end{aligned} \tag{A.69}$$

The typical turn-*on* time for the thyristor is around 100$\mu$s which requires that $R_2$ should dissipate the pulse energy for the specified amount of time. The energy dissipated during

each trigger pulse is given by

$$\begin{aligned} E_{R2} &= {I_{GT}}^2 R_2 t_q \\ &= (1\text{A})^2(1187\Omega)(100\mu\text{s}) \\ &= 118.7 \text{ mJ}. \end{aligned} \tag{A.70}$$

Likewise, the power rating for $D_2$ and $D_1$ should be sufficiently greater than 3.3 W and 1 W respectively.

According to the IXBOD data sheet [84], the low-pass filter with component values $R_1 = 700\ \Omega$ and $C_1 = 47$ nF would be sufficient to block any displacement current caused by the BOD during positive $\mathrm{d}v/\mathrm{d}t$.

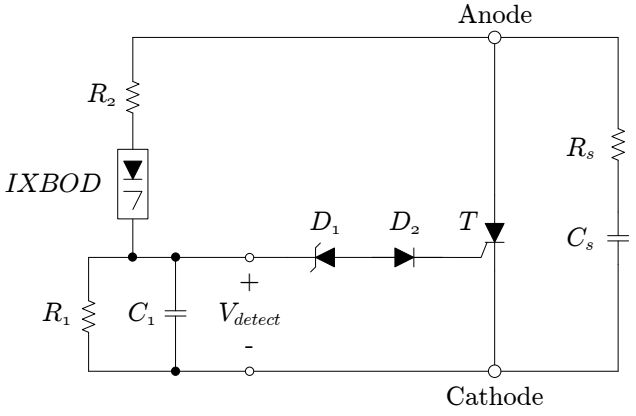



Figure A.16: Breakover diode circuit for triggering a thyristor under over-voltage conditions.

### A.4.3 Bypass-Crowbar Design

The bypass-crowbar serves three purposes: to maintain continuity of the distribution feeder when the controller is not powered, to protect the AC-to-AC converter against fault currents and to protect the IGBTs of the AC-to-AC converters against over-voltages when a shorted fault occurs on the output side of the regulator. The bypass-crowbar therefore acts as a controllable, bi-directional, normally-closed switch capable of handling large fault currents. It is implemented using two thyristors, $T_{b+}$ and $T_{b-}$, connected in anti-parallel across the output of each AC-to-AC converter.

Continuity of the distribution feeder should be maintained when the controller is not powered or during fault conditions. For this reason, the bypass driver circuit is designed to be self powered and normally closed. During normal operation, the controller has to actively keep the bypass open while the AC-to-AC converter is switching. If the control signal to the bypass falls away, the thyristors will simply close and the AC-to-AC converters will be cut out.

Since the continuity of the distribution feeder may not be broken, the regulator should be able to handle large fault currents in order for distribution feeder protection to take effect. Fault currents are detected by the controller which responds by activating the bypass to redirect the current away from the AC-to-AC converters. Various thyristors are considered in [73] and the SKET 740 thyristor from SEMIKRON is suggested as a good choice. The SKET 740 has an $i^2t$ rating of 6 480 000 $A^2s$, a surge on-state current rating $I_{TSM}$ of 36 kA and an average on-state current of 740 A. Since the bypass-crowbar opened within the same voltage rating as the dump-crowbar, the same $RC$-snubber can be used as designed for the dump-crowbar in Section A.4.2.

Each AC-to-AC converter module is designed to handle only 5% of the input line voltage which is superimposed upon the input line voltage. The converters are therefore floating with respect to the neutral point of the distribution feeder. If a shorted fault occurs at the output side of the distribution feeder, the output terminals of the AC-to-AC converters will be exposed to the entire line voltage. To protect the AC-to-AC converters, the bypass-crowbar is equipped with the same BOD trigger circuit used for the input-bus dump-crowbar in Figure A.16. When the voltage across the thyristors exceed 1 200 V, the BOD trigger will close the thyristors even when the controller is not powered. This allows for a much faster response without the need for the controller.

### Thyristor loss calculations and requirements

The power dissipation versus mean on-state current per thyristor is given in the device data sheet [93]. The mean on-state current is calculated as a half-cycle of the sinusoidal output current. By choosing a maximum output current of 150 $A_{rms}$, to allow for over-current conditions, the average current is calculated by dividing the peak of the sinusoidal current by $\pi$,

$$\begin{aligned} I_{TAV} &= \frac{I_{out(peak)}}{\pi} \\ &= \frac{\sqrt{2}(150\text{A})}{\pi} \\ &= 68 \text{ A}. \end{aligned} \tag{A.71}$$

From the device datasheet, the power dissipation ($P_{thy(loss)}$) at 68 $A_{av}$ is approximately 90 W per thyristor.

### Heatsink design for thyristors

The maximum heatsink temperature is given by

$$\begin{aligned} T_{sink} &= T_{vj(max)} - (R_{\theta(j-c)} + R_{\theta(c-s)})P_{thy(loss)} \\ &= 125°\text{C} - (0.042 \text{ K/W} + 0.01 \text{ K/W})(90 \text{ W}) \\ &= 120.3°\text{C}. \end{aligned} \tag{A.72}$$

All four thyristors, two from each AC-to-AC converter module, are mounted onto the same heatsink. At any time, only a maximum of two thyristors can be conducting, which results in a maximum power dissipation of 180 W. The minimum thermal resistance of the thyristor heatsink is given by

$$\begin{aligned} R_{\theta(s-a)} &= \frac{T_{sink} - T_{ambient}}{P_{loss(total)}} \\ &= \frac{120.3°\text{C} - 50°\text{C}}{180\ \text{W}} \\ &= 0.39\ \text{K/W} \end{aligned} \tag{A.73}$$

### A.4.4 Filter Cut-Out Design

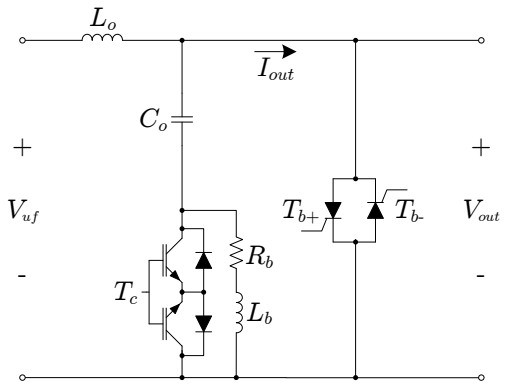



Figure A.17: Output $LC$-filter of the AC-to-AC converter with the bypass crowbar and filter cut-out.

The bypass-crowbar is implemented using thyristors $T_{b+}$ and $T_{b-}$, as shown on the schematic diagram in Figure A.17, and is connected across the output of the AC-to-AC converter. Consequently, the filter capacitor, $C_o$, is short circuited when the bypass is closed. To prevent damage to the capacitor and thyristors, two back-to-back IGBTs are placed in series with the filter capacitor to form a bi-directional cut-out switch, $T_c$. A bleed resistor $R_b$ with equivalent series inductance $L_b$ is placed in parallel with the cut-out. When the thyristors are closed, $T_c$ is opened and the capacitor is allowed to discharge through $R_d$.

However, the bypass-crowbar can be triggered by the BOD circuit which operates independently from the controller. As a result, the filter cut-out has to be controlled directly by the bypass-crowbar driver so that the filter can disconnected at the same instant that the bypass receives the BOD trigger. A schematic diagram of the control signals are shown in Figure A.18. If the controller sends a *low* signal (blue) to the bypass driver, the thyristors will close and a *low* signal is sent back to the controller. A *low* signal is also sent to the filter cut-out so that the filter can be disconnected. The turn-on

time of the thyristors are longer than the turn-off time of the cut-out IGBTs, which gives sufficient dead-time before the capacitor is short circuited.

When the bypass is closed, the filter cut-out should remain open long enough for the capacitor to completely discharge. However, the BOD trigger pulse width is in the order of 10 $\mu$s, which is too short for the capacitor to discharge. A timer circuit is therefore added to the bypass-crowbar driver to extend the BOD pulse width. This allows the capacitor to completely discharge before it is switched back into the circuit. Figure A.18 shows the short BOD trigger pulse in red, with the extended control pulse transmitted to the filter cut-out and the controller.

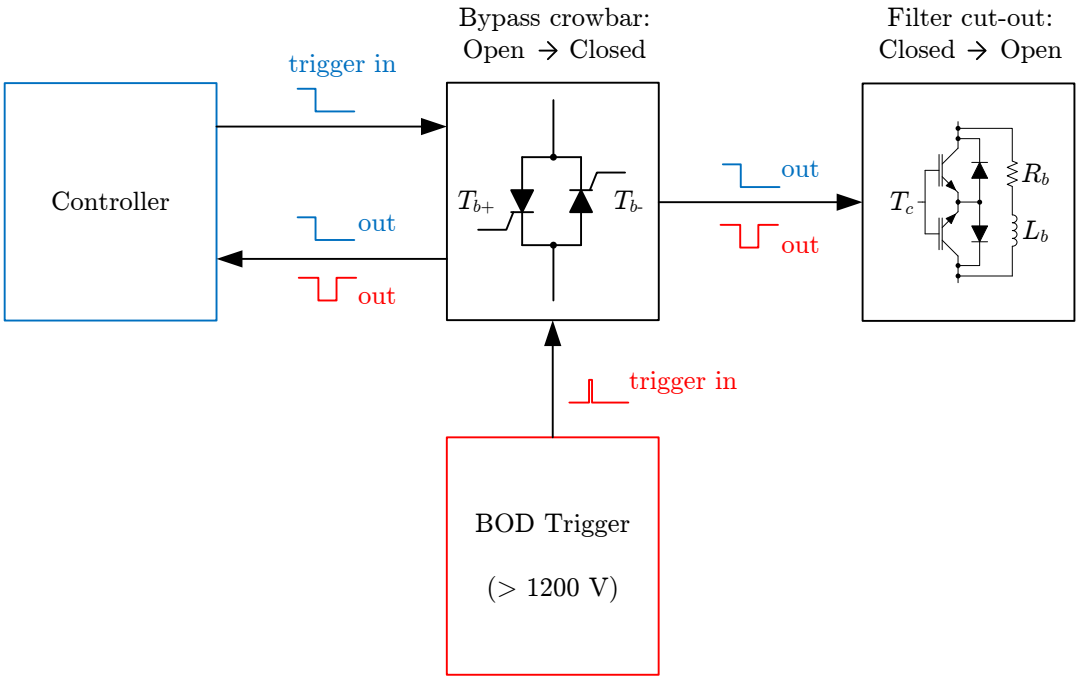



Figure A.18: Block diagram of the communication and signals between the controller, bypass-crowbar and filter cut-out.

### Bleed resistor calculations

The bleed resistor has to dissipate the energy contained in the filter capacitor $C_o$ for the maximum allowed output voltage. The bypass-crowbar triggers at 1 200 V, which limits the capacitor voltage. The energy contained in the capacitor at 1 200 V is therefore

$$\begin{aligned} E_c &= \frac{1}{2} C_o \mathrm{V}_{\max}^2 \\ &= \frac{1}{2}(75\mu\mathrm{F})(1200\mathrm{V})^2 \\ &= 54 \text{ J}. \end{aligned} \tag{A.74}$$

Since the bypass-crowbar is connected in parallel with the capacitor, the rate of rise of current ($\mathrm{d}i/\mathrm{d}t$) through the thyristors has to be limited by ensuring the equivalent series

inductance $L_b$ of the bleed resistor is large enough. The same value of 12 $\mu$H can be used for $L_b$ as calculated in (A.64) and (A.65). The discharge time is determined by the value of the bleed resistor $R_b$. If a bleed resistor with value of 470 $\Omega$ is used, the discharge time is calculated for five time constants,

$$\begin{aligned} t_{DC} &= 5 \times \tau \\ &= 5 \times R_b C_o \\ &= 5 \times (470\Omega)(75\mu\text{F}) \\ &= 176.25 \text{ ms}. \end{aligned} \tag{A.75}$$

The timer circuit on the bypass-crowbar should therefore keep the filter cut-out open for at least 177 ms.

Should the controller lose power, the filter cut-out will open when the control signal is lost and the capacitor will be protected when the bypass closes. If the filter cut-out driver itself loses power, the filter will also open and provide protection. The system can therefore settle into a safe state and maintain continuity of the distribution feeder even when power to the controller and driver boards fail.

### Filter cut-out IGBT loss calculations

The filter cut-out $T_c$ is used as a bi-directional switch to disconnect the filter capacitor when the bypass-crowbar is closed. Since the cut-out IGBTs are only switched when the bypass is opened or closed, the switching losses are ignored and only the conduction losses are taken into account. The cut-out switch consists of two IGBTs, placed back-to-back, with two anti-parallel diodes connected across them. As a result, only the conduction losses of one IGBT and one diode are taken into account when $T_c$ is closed. The SKM150GM12T4G IGBT module from SEMIKRON is considered since it consists of two back-to-back IGBTs and corresponding anti-parallel diode. The current through

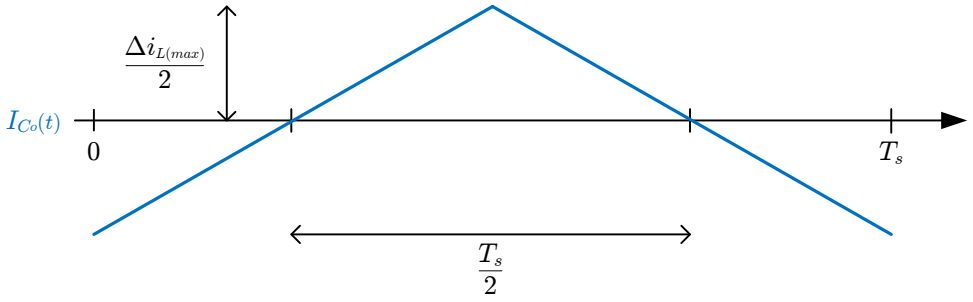



Figure A.19: Depiction of the filter capacitor current over one switching period.

the filter capacitor, depicted in Figure A.19, is a triangle wave that is symmetrical around zero. Each IGBT-diode pair conducts either during the positive or the negative side of the waveform shown. The average current through an IGBT and diode can therefore be

calculated by taking the average of either the positive or the negative part of the capacitor current. Using the waveform in Figure A.19 with (A.42) and a switching period ($T_s$) of 100 $\mu$s, the average current becomes

$$\begin{aligned} I_{av(cond)} &= \frac{1}{T_s}\left(\frac{1}{2}\cdot\frac{T_s}{2}\cdot\frac{\Delta I_L}{2}\right) \\ &= \frac{\Delta I_L}{8} \\ &= \frac{42.4}{8} \\ &= 5.3 \text{ A} \end{aligned} \tag{A.76}$$

The diode has a forward voltage of 2.49 V and the IGBT has an on-state voltage of 2.45 V. Using (A.76) together with the on-state and forward voltage, the power dissipated in the entire IGBT module becomes

$$\begin{aligned} P_{loss(tot)} &= \left(V_{ce(sat)} + V_F\right) I_{av(cond)} \\ &= (2.45 + 2.49)(5.3) \\ &= 26.18 \text{ W} \end{aligned} \tag{A.77}$$

**Heatsink design for filter cut-out IGBTs**

The SKM150GM12T4G has a maximum case temperature rating of 125°C and a thermal resistance from case-to-sink of 0.038 K/W [94]. Both IGBTs and diodes are packaged into a single module with a common casing for all the elements. If the case temperature is kept below the maximum rating, the heatsink can be designed without the need for calculating the individual junction temperatures. Using (A.77), the maximum heatsink temperature is calculated as

$$\begin{aligned} T_{sink} &= T_{case} - R_{\theta(c-s)} P_{loss(tot)} \\ &= 125^\circ\text{C} - (0.038\text{K/W})(26.18\text{W}) \\ &= 124^\circ\text{C}. \end{aligned} \tag{A.78}$$

The IGBT module should be mounted onto a heatsink or a surface with a sink-to-ambient thermal resistance of

$$\begin{aligned} R_{\theta(s-a)} &\leqslant \frac{T_{sink} - T_{ambient}}{P_{loss(tot)}} \\ &\leqslant \frac{124^\circ\text{C} - 50^\circ\text{C}}{26.18 \text{ W}} \\ &\leqslant 2.82 \text{ K/W}. \end{aligned} \tag{A.79}$$

## A.4.5 Soft-start Design

The initial line voltage that can be applied to the regulator may be at a zero-crossing and large inrush currents will occur as a result of the bus capacitor being charged. In order

to to limit the inrush current and rate of rise of current ($\mathrm{d}i/\mathrm{d}t$), a soft-start mechanism is implemented. The soft-start is connected in series with the bus capacitor, $\mathrm{C}_{bus}$, and is realised using the IGBT pair $\mathrm{T}_{ss}$, limiting resistor $R_{ss}$ and limiting inductance $\mathrm{L}_{ss}$. During inrush, switch $\mathrm{T}_{ss}$ is kept open while $\mathrm{C}_{bus}$ is charged through the limiting resistor and inductor $\mathrm{R}_{ss}$ and $\mathrm{L}_{ss}$. After the bus capacitor has been charged, switch $\mathrm{T}_{ss}$ is closed at the appropriate time and normal switching may commence.

The system is designed for a maximum input voltage of 698.5 $\mathrm{V}_{rms}$ and an overload current of 150 $\mathrm{A}_{rms}$. In order to limit the current for the maximum input voltage, the limiting resistance $\mathrm{R}_{ss}$ becomes 4.7 Ω.

The the same criteria for maximum rate of rise of current that is used for the filter cut-out and dump-crowbar can be used for the limiting inductance. Therefore, using the same inductance as calculated in (A.65), the limiting inductance becomes 12 $\mu$H.

Switch $\mathrm{T}_{ss}$ is realised using the same SKM150GM12T4G IGBT module from Semikron that is used for the filter cut-out. The IGBT module consists of two back-to-back IGBTs with their corresponding anti-parallel diodes. The limiting soft-start resistor is realised using a high power, 4.7 Ω, 200 W wire wound resistor. Unlike the filter cut-out, the soft-start IGBTs does not conduct continuously and no heatsink design is required. Mounting the IGBT module onto a metal casing or plate should be sufficient.

### A.4.6 Design Verification by Simulation

The design of the protection mechanisms are verified by simulation using Ansoft's Simplorer 8 software package. The simulation is set up according to the schematic diagram given in Figure A.20 and the component values in Table A.4. The value for $L_{\mathrm{eq}}$ is chosen as the worst case value designed for in Section A.2. The converter is switched using the commutation scheme with open-loop PWM at 10 kHz and a simulation step size of 100 ns.

Table A.4: Component values used in the simulation of the protection mechanisms.

| Component | Value | Component | Value |
|---|---|---|---|
| $\mathrm{E}_{s1}$ | 698.5 $\mathrm{V}_{rms}$ | $\mathrm{E}_{p}$ | 13.97 $\mathrm{kV}_{rms}$ |
| $\mathrm{L}_{eq(\max)}$ | 1.01 mH | $\mathrm{L}_{line}$ | 1.01 mH |
| $\mathrm{L}_{o}$ | 530 $\mu$H | $\mathrm{L}_{b}$ | 12 $\mu$H |
| $\mathrm{L}_{d}$ | 12 $\mu$H | $\mathrm{L}_{ss}$ | 12 $\mu$H |
| $\mathrm{C}_{bus}$ | 90 $\mu$F | $\mathrm{C}_{s1}$ | 1.41 $\mu$F |
| $\mathrm{C}_{s2}$ | 1.41 $\mu$F | $\mathrm{C}_{o}$ | 75 $\mu$F |
| $\mathrm{R}_{ss}$ | 4.7 Ω | $\mathrm{R}_{d}$ | 5.6 Ω |
| $\mathrm{R}_{b}$ | 470 Ω | $\mathrm{R}_{line}$ | 0.01 Ω |
| $\mathrm{Z}_{load}$ | 139 Ω | | |

### Dump-crowbar simulation

The dump-crowbar test simulation is set up using a resistive-inductive load of $139\angle -45° \ \Omega$ to provide a lagging current. For a worst case scenario, the dump resistor has to dissipate the energy contained in the bus and snubber capacitors as well as a complete half-cycle of the input voltage source ($E_s$). A fault is generated at 30 ms, when the bus voltage ($V_t$) sign changes from positive to negative. At that point all the switches, $\mathrm{T}_1$, $\mathrm{T}_2$, $\mathrm{T}_3$ and $\mathrm{T}_4$, are opened while the bypass-crowbar ($\mathrm{T}_b$) is closed and the filter cut-out ($\mathrm{T}_c$) is opened.

Since the current through the transformer leakage inductance ($L_{eq}$) is lagging with respect to the bus voltage, there is still a positive current flowing when the voltage reaches a zero-crossing. However, the only return path for the current is through the bus and snubber capacitors, which results in the bus voltage charging in the positive direction. This can be seen in the simulation result of the bus voltage waveform in Figure A.21a. At 30 ms, the decreasing bus voltage starts to increase, but then decreases again when the dump-crowbar is activated shortly thereafter.

Snubber capacitors $C_{s1}$ and $C_{s2}$ provide a return path the filter inductor current ($\mathrm{I}_{Lo}$) when the IGBTs stop switching. Unlike the input bus capacitor, the voltage across the two snubber capacitors charge in opposite directions as they are forced to supply current to the filter inductor. The dump-crowbar thyristors, $\mathrm{T}_{d+}$ and $\mathrm{T}_{d-}$, are set up to trigger when their forward bias voltage exceeds 1 200 V. The thyristors are connected in such a way that they will trigger when the voltage across the snubber capacitors exceed the 1 200 V threshold. The snubber capacitor voltages are shown in Figures A.21b and A.21c. When the fault is triggered, both snubber capacitors charge in the opposite directions as a result of $I_{Lo}$. However, in Figure A.21b it is shown that the voltage across $C_{s1}$ begins to decrease before reaching the 1 200 V threshold. Likewise, it is shown in Figure A.21c that the voltage across $C_{s2}$ begins to discharge. But, unlike $C_{s1}$, the voltage across

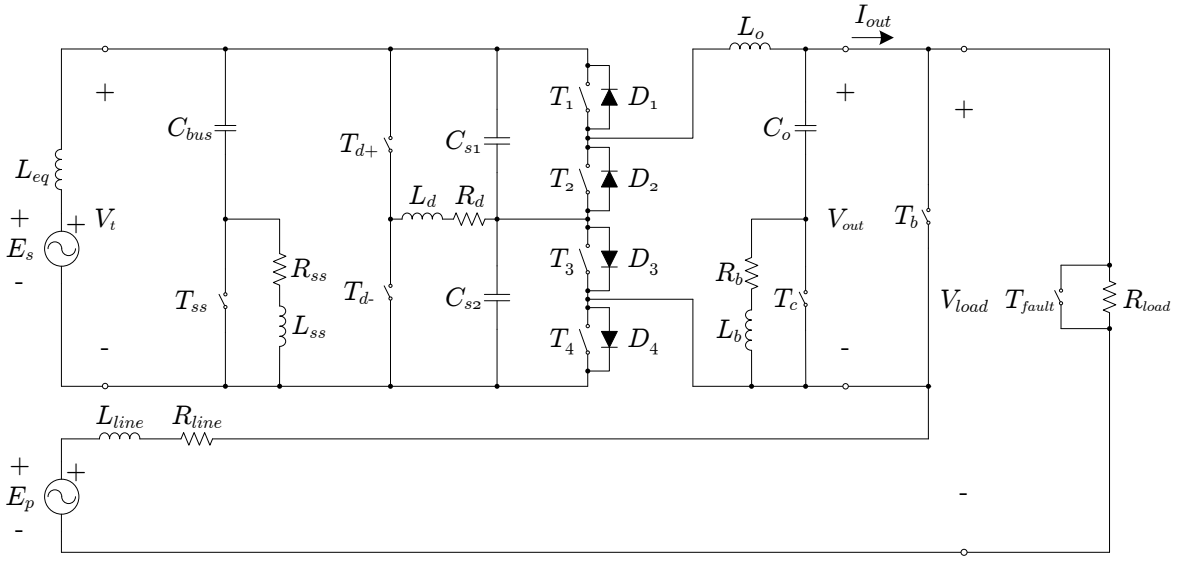
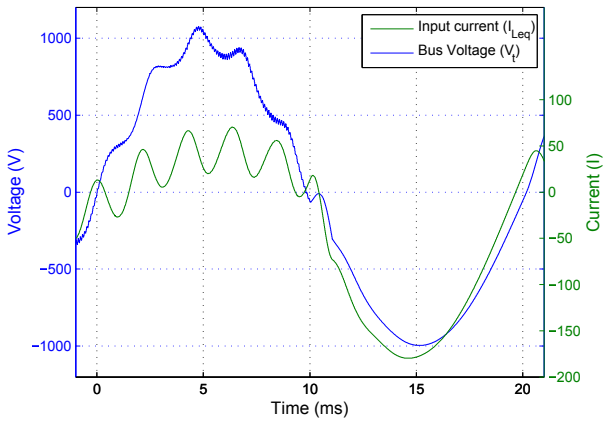
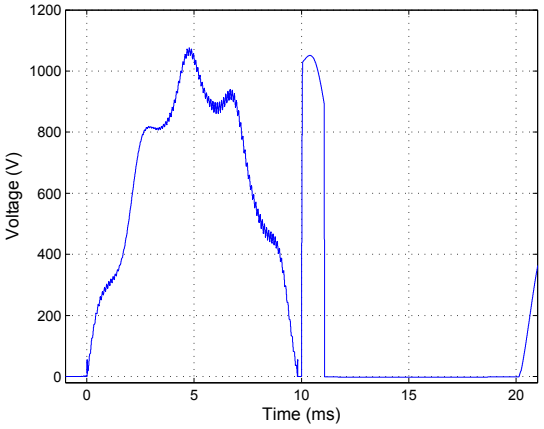


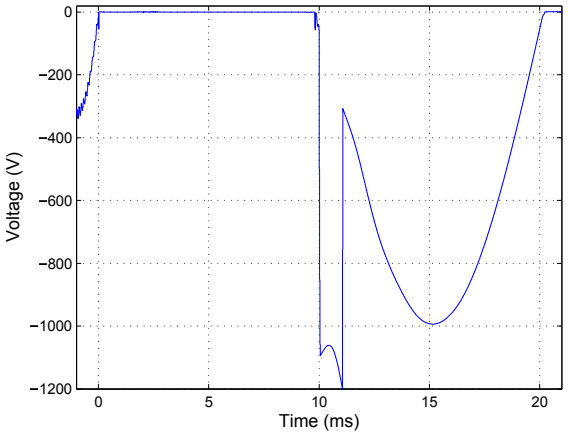

Figure A.20: Schematic layout for verifying the design of the protection mechanisms.



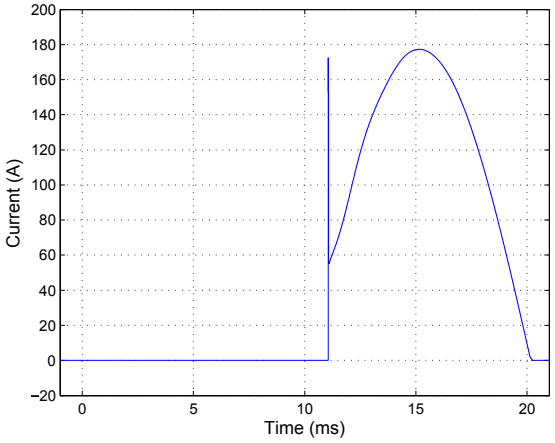

(a) Simulation result of the voltage waveform across the bus capacitor $C_{bus}$ and input current waveform through $L_{eq}$.




(b) Simulation result of the voltage waveform across the snubber capacitor $C_{s1}$.




(c) Simulation result of the voltage waveform across the snubber capacitor $C_{s2}$.




(d) Current waveform through dump resistor ($R_d$) for the maximum waveform duration and amplitude.

Figure A.21: Simulation results for verifying the correct operation of the input-bus dump-crowbar during a fault condition.

the capacitor then begins to charge again in the negative direction until it reaches the 1 200 V threshold. The change in snubber voltages before reaching the threshold can be attributed to the bus voltage changing direction. As the bus voltage changes direction, a conduction path is created from the negative terminal to the positive terminal through $C_{s1}$ and $C_{s2}$. The voltage across $C_{s1}$ starts to decrease as the bus voltage increases in the negative direction. Since $C_{s2}$ is charged in the negative direction, the negative bus voltage together with $I_{Lo}$ will continue to charge $C_{s2}$ in the negative direction, as show in Figure A.21b.

After reaching the voltage threshold, thyristor $T_{b-}$ is triggered and $C_{s2}$ is allowed to discharge through $R_d$. A conduction path is created through $R_d$, which relieves $C_{s1}$ and $C_{s2}$ from the stress induced by $I_{Lo}$. Figure A.21d shows simulation results for the current waveform through $R_d$. The capacitor discharge current can be seen by the initial spike,

followed by the current induced by driving source $E_{s1}$.

The simulation results correspond to the expected behaviour under the worst case scenario and provides effective protection against unforeseen system shut-downs.

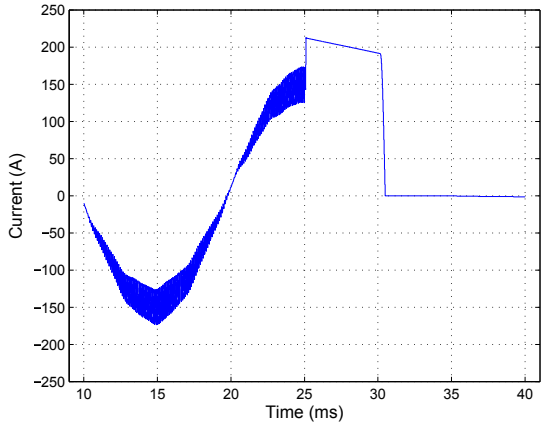
### Bypass-crowbar and Filter Cut-Out simulation

The over-current and bypass test is set up using a resistive load of 139 Ω. A short circuited line fault is induced by closing the switch $T_{fault}$ that is connected across the load. This effectively short circuits the load and puts the full line voltage across the output filter of the AC-to-AC converter. As a result, the current through the filter inductor will increase and the voltage across the filter capacitor will rapidly charge in the negative direction as shown in Figures A.22a and A.22c.

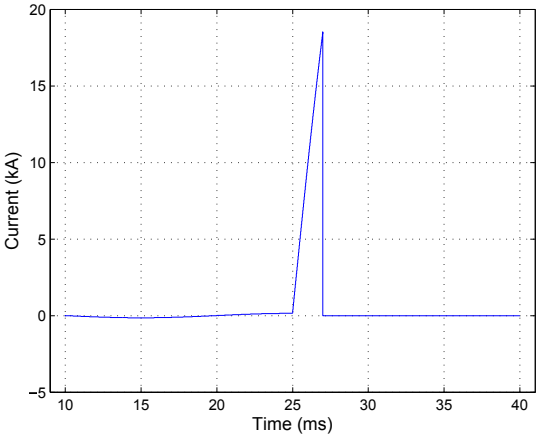
The bypass-crowbar can be activated by the controller when the filter inductor current exceeds the 212 A threshold or by a break over diode circuit when the voltage across the bypass thyristors exceed 1 200 V. In the case of a short circuited fault, any one of the two trigger conditions can active the bypass depending on which limit is exceeded first. In the case of this simulation, the current limit is exceeded before the voltage limit as shown in Figure A.22a. At 25 ms the fault is induced and the filter inductor current rapidly increases until the bypass is triggered as 25 ms. After the bypass has closed, the filter inductor current is left to free-wheel through the bypass $T_b$, IGBT $T_3$ and diode $D_2$ as shown by the shallow declining waveform between 25 ms and 30.1 ms. At 30.1 ms the input bus voltage sign changes and the commutation is switched such that $T_3$ and $T_4$ are turned off while $T_1$ and $T_2$ are turned on. This diverts the free-wheeling path and the inductor current is quickly brought to zero. However, since the output is diverted through the bypass, the output current $I_{out}$ is left to increase until the distribution feeder circuit breaker is opened as shown in Figure A.22b.

The filter cut-out is designed to protect the filter capacitor from being short-circuited when the bypass is closed. As shown in Figure A.22c, the output voltage and filter capacitor voltage follow each other as expected until the fault is induced. At 25 ms, the filter capacitor is rapidly charged in the negative direction until 25 ms, when the bypass is closed and the filter cut-out is opened. The output voltage drops to zero and the filter capacitor is left to gradually discharge through the bleed resistor $R_b$.

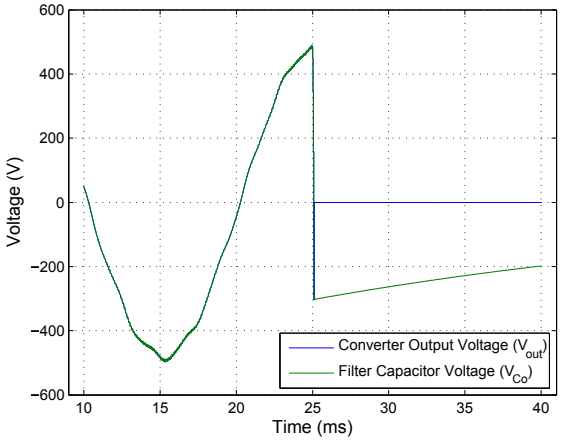
The protection mechanisms therefore prove to be effective in simulation however, the speed at which the bypass is triggered and the filter cut-out is opened is instantaneous and ideal. In the practical system, there will be a 2 $\mu$s to 5 $\mu$s turn-on delay which will result in slightly higher over-voltage and over-current conditions. This would not be a problem since the practical distribution feeder inductance is expected to be larger than the conservative value used in the simulation.




(a) Simulation result of the filter inductor current waveform ($I_{Lo}$).




(b) Simulation result of the output current waveform ($I_{out}$).



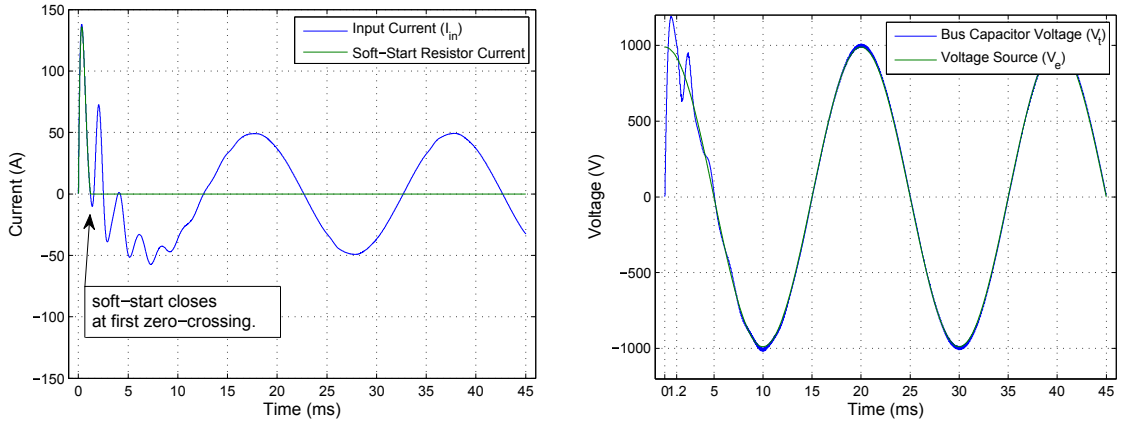

(c) Simulation results of the output voltage ($V_{out}$) waveform and filter capacitor waveform ($V_{Co}$).

Figure A.22: Simulation results for verifying the correct operation of the bypass crowbar during over-current or over-voltage conditions.

### A.4.7 Soft-Start Simulation

The soft-start simulation is set up using a sinusoidal voltage source with an initial value that is 90° out of phase. The soft-start switch, $T_{ss}$, is initially open and the bus capacitor, $C_{bus}$ is left to charge through the soft-start resistor and inductor, $R_{ss}$ and $L_{ss}$. The purpose of the soft start is to limit the inrush current to acceptable levels when the full bus-voltage is applied before the converter starts switching. Commutation and switching is programmed to commence only after the soft-start has safely switched.

The simulation results for the input-bus and soft-start resistor current are shown in Figure A.23a and the input and bus voltage in Figure A.23b. At time zero, a voltage is applied to the bus while the $C_{bus}$ is discharged. In Figure A.23a, it is shown that the current starts to rise, but is limited by $R_{ss}$. At 1.2 ms, the input-current transient passes zero and the soft-start switch, $T_{ss}$, is closed at that point. The input current transient continues to die away while the soft-start current remains zero. As $T_{ss}$ is closed, $C_{bus}$ is




(a) Simulation results of the input and soft-start resistor current waveforms.

(b) Simulation results of the bus voltage and voltage source during soft-starting.

Figure A.23: Simulation results for verifying the correct operation of the soft-starting mechanism.

directly connected in to bus and switching is commenced.

This simulation verifies the correct functioning of the soft-start mechanism and its method of operation.

### A.4.8 Summary

This section discussed various protection issues associated with the AC-to-AC converter and presented solutions to protect the converter from exceeding any voltage and current ratings. A dump-crowbar was designed to protect the input bus against over voltage conditions while a bypass-crowbar was presented to protect the output side from over-voltage and over-current conditions and to maintain continuity of the distribution feeder.

The dump-crowbar on the input bus was constructed by using two thyristors, one for each polarity, and connecting them to a dump resistor. The thyristors were designed to self-trigger using a 1 200 V breakover diode from IXYS, which allows them to turn on when their forward bias voltage exceeds 1 200 V. The SKMT92/16E thyristor from SEMIKRON was selected and an appropriate *RC* snubber was designed.

The bypass-crowbar was designed to serve three purposes: to maintain continuity of the distribution feeder when the controller is not powered, to protect the AC-to-AC converter against fault currents and to protect the IGBTs of the AC-to-AC converters against over-voltages when a shorted fault on the output side occurs. The bypass was designed as a controllable, bi-directional, normally-closed switch capable of handling large fault currents. It was implemented using two SKET740 thyristors from SEMIKRON and triggered using the same breakover diode from IXYS.

However, it was shown that the crowbar effectively short-circuits the filter capacitor which prompted the design of a filter cut-out. The cut-out was implemented by placing two back-to-back IGBTs and a bleed resistor in parallel and connecting them in series

Table A.5: Summary of components and their designed values for the protection mechanisms

| **Breakover Diode Circuit** | | |
|---|---|---|
| Component | Value / Model | Manufacturer |
| $R_1$ | 700 Ω | |
| $R_2$ | 1.18 kΩ | |
| $R_s$ | 68 Ω | |
| $C_1$ | 47 nF | |
| $C_2$ | 330 nF | |
| $D_1$ | 3.3V, »3.3W | |
| $D_2$ | »1W, Fast-recovery | |
| BOD | IXBOD1-12RD | IXYS |
| **Dump-Crowbar** | | |
| Component | Value / Model | Manufacturer |
| $T_{d+}$, $T_{d-}$ | SKMT92/16E | SEMIKRON |
| $R_d$ | 5.6 Ω | |
| $L_d$ | 12 $\mu$H | |
| **Bypass-Crowbar & Filter Cut-Out** | | |
| Component | Value / Model | Manufacturer |
| $T_{b+}$, $T_{b-}$ | SKET 740 | SEMIKRON |
| $T_c$ | SKM150GM12T4G | SEMIKRON |
| $R_b$ | 470 Ω | |
| $L_b$ | 12 $\mu$H | |
| **Soft-Start** | | |
| Component | Value / Model | Manufacturer |
| $T_{ss}$ | SKM150GM12T4G | SEMIKRON |
| $R_{ss}$ | 4.7 Ω | |
| $L_{ss}$ | 12 $\mu$H | |

with the filter capacitor. When the IGBTs are turned off, the capacitor is left to safely discharge through the bleed resistor. The filter cut-out was compactly realised using the SKM150GM12T4G, back-to-back, IGBT module from SEMIKRON.

A soft-start mechanism was introduced to limit inrush currents when the bus capacitor is discharged and a voltage is applied to the input bus of the AC-to-AC converter. The soft-start was implemented in the same way as the filter cut-out by placing two back-to-back IGBTs and a soft-start resistor in parallel and connecting them in series with the bus capacitor. When the IGBTs are turned off, the inrush current is limited by the resistor. The same SKM150GM12T4G IGBT module from SEMIKRON is used to realise the soft-start switch.

Simulation results showed the effective behaviour of the protection mechanisms en verified the expected response. It was shown that the dump-crowbar effectively limits the bus voltage to 1 200 V while the bypass-crowbar diverts the large fault currents when a shorted fault in the distribution feeder occurs. The soft-start was also shown to be

effective in limiting the inrush current when a large initial voltage is applied to the input bus.

A summary of the components, selected values, manufacturers and models are given in Table A.5.

# A.5 Controller Hardware and Peripherals

## A.5.1 Overview

This section gives an overview of the controller hardware and the peripheral circuits. A functional overview and description of operation is discussed. The detail design of the main controller and optic driver boards are discussed in [62].

A functional overview of the main controller board and it's interconnections with other hardware is discussed in Section A.5.2. In the following Section, A.5.3, a simplified description is given of the functional process within the main FPGA controller board. The FPGA and channels to the user interface, analogue measurement circuits and fibre-optic drivers are presented. The operation of the measurement hardware is discussed Section A.5.4 and the detail design is presented in Appendix B. Section A.5.5 gives a complete overview of the small-signal power supply strategy with voltage rails, isolation barriers and power consumption. In the last section, the controller hardware and peripherals are concluded in a short summary.

## A.5.2 Controller Hardware Functional Layout

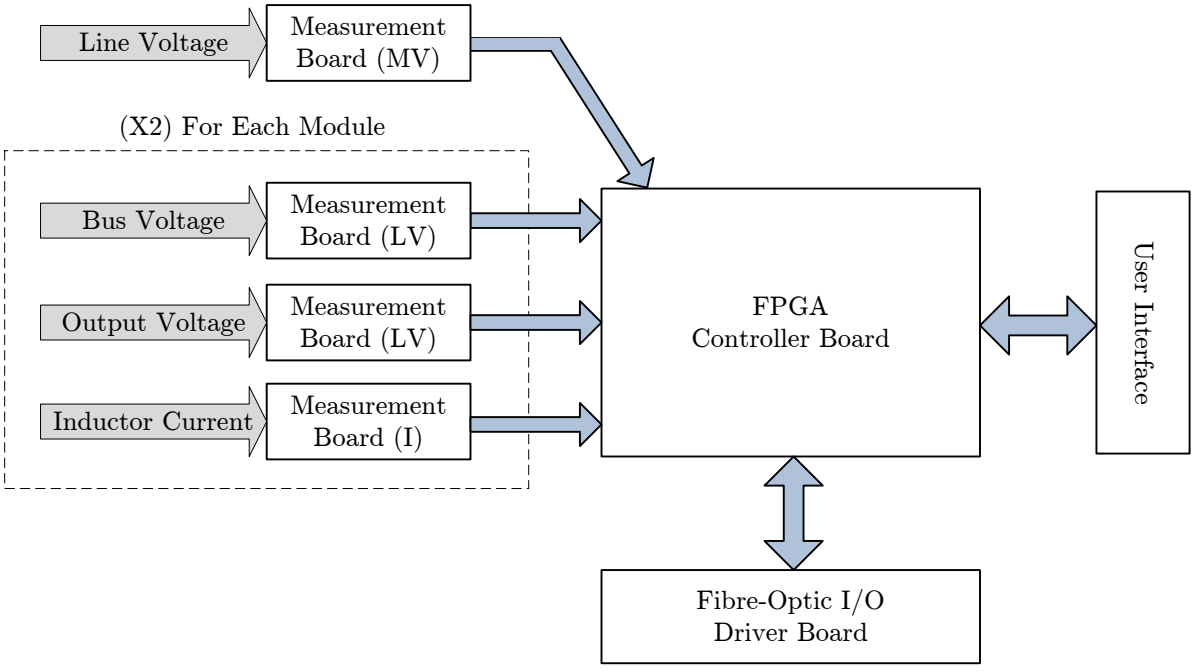



Figure A.24: Block diagram of the FPGA controller board and peripheral connections.

The voltage regulator consists of two AC-to-AC converter modules, which are series stacked and connected in an autotransformer configuration as shown in Figure 4.2. The topology is designed in such a way that more than two AC-to-AC converter modules can be series stacked to allow for regulation at higher voltages. For the case of two converter

modules, as discussed in this thesis, the voltage difference between two modules are low enough so that only one controller board is needed to control both converters.

To minimise common-mode interference, the controller's common voltage is grounded to the bottom output terminal of the lower converter module, which is connected to the positive side of the incoming distribution feeder voltage. The controller-common is marked as point *cc* in Figure 4.2.

In order to perform control, voltage and current measurements of both converter modules as well as the distribution feeder are needed. The measurements can be divided into three types: low voltage measurements (0 to 1.2 kV), medium voltage measurements (1.2 kV to 14 kV) and current measurements (0 to 200 A). Each converter module requires a measurement of the input bus voltage ($V_t$), converter output voltage ($V_{out}$) and the filter inductor current ($I_{Lo}$). In order to regulate the distribution feeder voltage, a medium voltage measurement of the incoming distribution feeder is needed.

The controller hardware setup is shown in Figure A.24 with the FPGA controller board acting as the central hub for all the other boards. A voltage or current measurement is taken, as shown on the left of the diagram, using a measurement board and passed directly to the FPGA board in the form of a differential analogue signal. The measurement boards are powered directly from the controller board and the differential signals are measured with respect the controller's common voltage.

The controller is placed with respect the controller-common point, *cc*, as shown in Figure 4.2 and therefore it is not possible to control the IGBTs and thyristors physically from the FPGA board. As a result, a fibre-optic driver board is used to translate the digital I/O ports to fibre-optic links that can safely be taken to any isolated driver board. Furthermore, since the controller is floating with respect to physical ground, it is not possible to touch the controller by hand. A remote user interface, in the form of optically linked push buttons, are connected to the controller board to allow the user to change system parameters and navigate a LCD display. A block diagram showing the fibre-optic links connected to the optic driver board is given in Figure A.25. Each converter module has four bi-directional optical links connected to the four main IGBTs. The controller uses the transmitting signal to turn the IGBTs on and off while the receiving link is used to act on overcurrent conditions by monitoring the IGBT's DSAT voltages. A further bi-directional link is connected to the bypass-crowbar. The transmitting link from the controller is used to manually open and close the crowbar while the receiving link is used to inform the controller when the crowbar has triggered from an overvoltage condition. A receiver is connected from the dump crowbar to inform the controller when the dump has triggered.

For correct commutation with respect to the sign of the bus voltage, an accurate sign detector is implemented. The sign detector reads the sign of the bus voltage and transmits the signal to the optical driver board. A soft-start mechanism is implemented using only

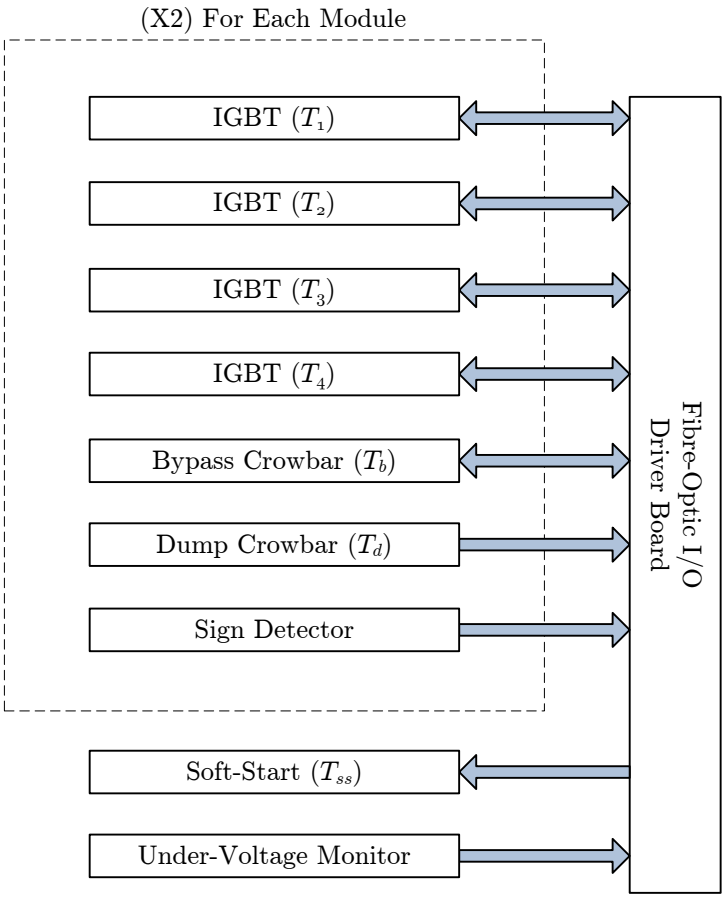



Figure A.25: Block diagram of the fibre-optic connections to the optic driver board.

one optic transmitter to simultaneously control the soft-start of both modules. Lastly, one optic receiver is used to read the status of the undervoltage monitor to allow the controller to act when the power to the driver circuits fail.

### A.5.3 Main Controller

The FPGA controller board is based on the Cyclone III family of FPGA's from Altera and forms the central hub for all the peripheral circuit boards. A block diagram describing the connections to the various peripheral hardware is shown in Figure A.26.

On the controller board, provision is made for a user interface by means of an on-board LCD display and four push buttons. However, a user cannot touch the controller during operation and a separate I/O header is reserved to connect a remote user interface to controller.

The controller board also has eight differential analogue input ports of which seven are utilised, as shown in the block diagram. Each differential input signal is passed through a buffer to provide protection against overvoltages before being passed through a passive low pass filter. The low pass filter is used to prevent aliasing by attenuating higher frequency noise. After being filtered, the signal is passed through a high speed 12-bit differential analogue-to-digital converter and sent to the FPGA.

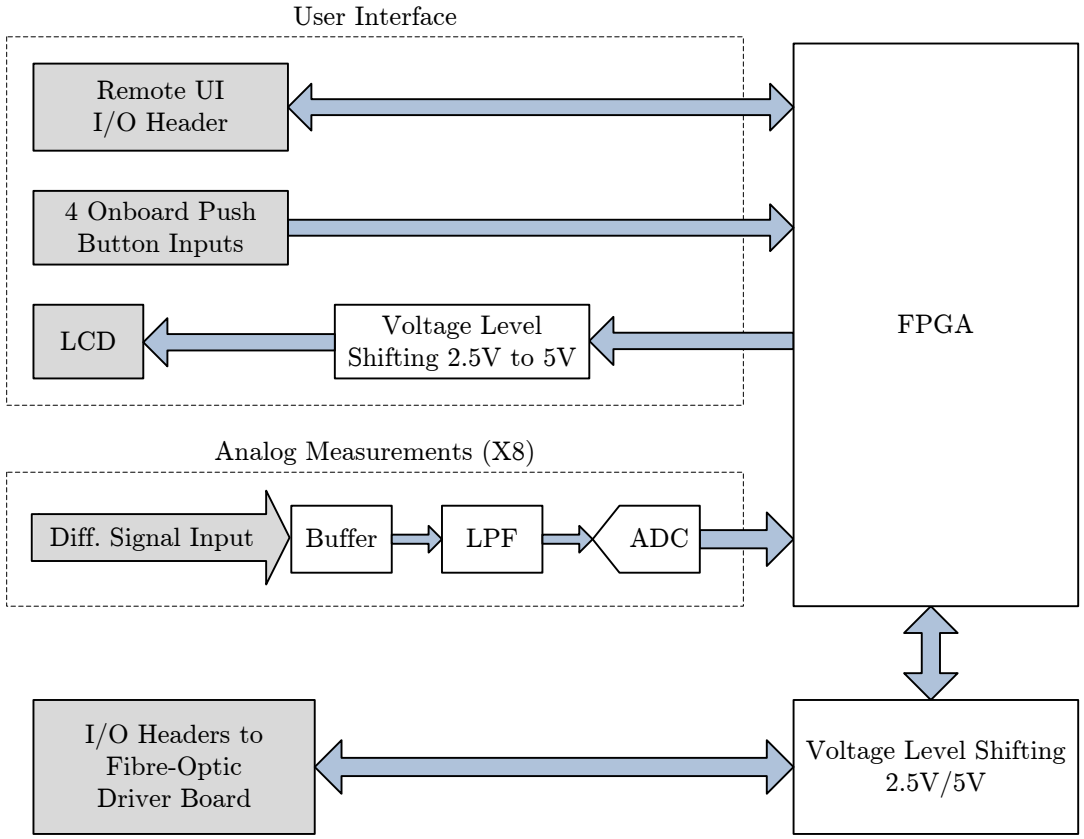



Figure A.26: Simplified functional block diagram of FPGA controller board layout.

The optic driver board is connected directly to the FPGA controller board via I/O headers to provide an interface between the fibre-optic cables and the FPGA itself. However, the optic transmitters and receivers operate at 5 V whereas the FPGA operates at 2.5 V. For this reason, a voltage translation IC is used to translate between the FPGA voltage levels and that of the optic driver board.

### A.5.4 Measurement Hardware Design

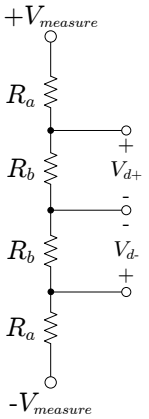



Figure A.27: Differential voltage measurement.

*Low Voltage Measurements*

The low voltage measurement boards are used to measure the voltages at the input bus and output of the AC-to-AC converter. The boards are designed to measure voltages up to 1 200 V and is implemented by taking a differential measurement across four voltage divider resistors. A circuit diagram with the voltage divider and differential measurement points are shown in Figure A.27. A high resistance is chosen for $R_a$ and a low resistance for $R_b$. A scaling and level-shifting circuit is used to translate the differential signals to a compatible voltage level before being transmitted to the controller board. The complete circuit design and schematic diagrams are given in Appendix B.8.

*Medium Voltage Measurements*

For the purpose of distribution feeder voltage control, a measurement of the line voltage is needed. The medium voltage measurement is implemented by using the LV100-4000/SP12 voltage transducer from LEM. The voltage transducer has galvanic isolation between the primary side and the electronic measuring board, which provides additional protection when overvoltages may occur.

The voltage transducer has a large internal current limiting resistor between the input terminals. The voltage transducer translates the primary voltage by measuring the current through the resistor using a Hall Effect sensor. The current is then transferred to the secondary circuit which linearly delivers a small output current based on the measured current at the resistor. The measuring range of the LEM LV100-4000/SP12 is only 6 kV, but can be increased to 14 kV by placing an appropriate resistor in series with the transducer.

A resistor is connected across the small-signal output of the voltage transducer and a measurement circuit is used to read, scale and level shift the signal before being transmitted to the controller board. The detail design of the measurement circuit and the LEM module is presented in Appendix B.9.

*Current Measurements*

The current measurement design is done in a similar way as the medium voltage measurement board. The LA305-S current transducer from LEM is used to measure the current through the filter inductor, $L_o$. The current transducer also makes use of a Hall Effect sensor and works in a similar way as the voltage transducer. In this case, the current is measured directly and linearly translated to a small-signal current at the output terminal. The same measurement board, as used for the voltage transducer, is used but with different levels of scaling and level shifting. The detail design and calculations for the measurement board is given in Appendix B.10.

### A.5.5 Power Management

Each AC-to-AC converter requires different isolated small-signal power supplies to power the various driver boards. These power supplies are sourced from a small signal voltage

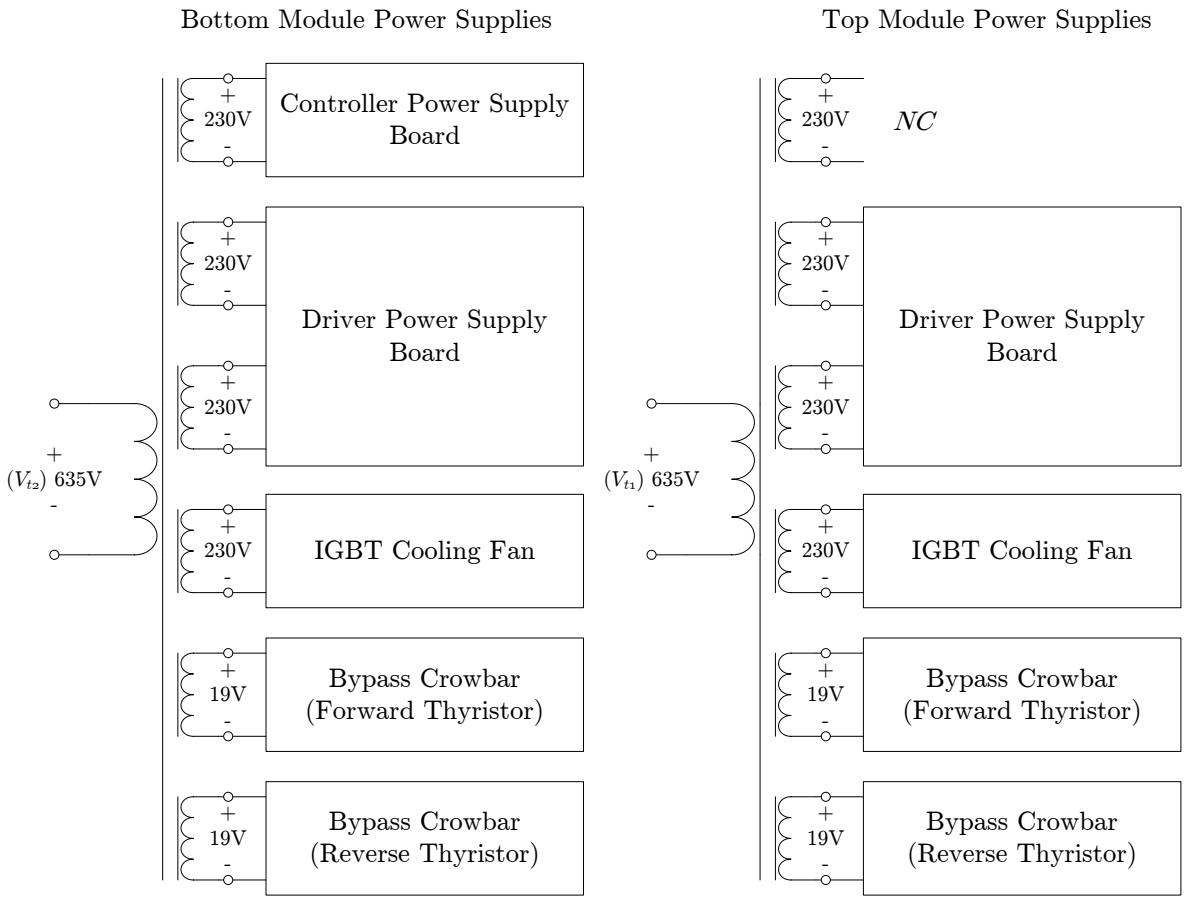



Figure A.28: Block diagram of the isolated small signal power power supplies.

transformer that is tapped from the 635 VAC input bus voltage, $V_t$, of each converter module. The secondary side of the transformer has multiple isolated windings that power various isolated power supply boards and drivers.

A schematic block diagram describing the supply transformer is shown in Figure A.28. There are six isolated windings, of which four supply 230 VAC and two provide 19 VAC. The power supplies for both converter modules are identical, except for the bottom converter, which powers the controller hardware as well.

The two 19 V terminals are used to directly supply isolated power the bypass crowbar. One 19 V supply is used for the forward bias thyristor and the other for the reverse bias thyristor. The cooling fan of the forced cooled heatsink is also directly powered, using one the of the 230 V terminals. The remaining 230 V terminals are used to power the driver circuits and the controller board's power supplies as shown in the schematic.

The power distribution of the driver boards are shown in Figure A.29. The two 230 VAC sources are fed to two Traco AC-to-DC supply modules. The top Traco module supplies +12 V rails and the bottom Traco module supplies + 5V rails.

The +12 V rail is used to feed the dump-crowbar driver, the filter cut-out and the soft-start driver. The +5 V rail is used to power the main IGBT drivers and the sign detector. Each driver board is equipped with a Recom isolated DC-to-DC converter. This

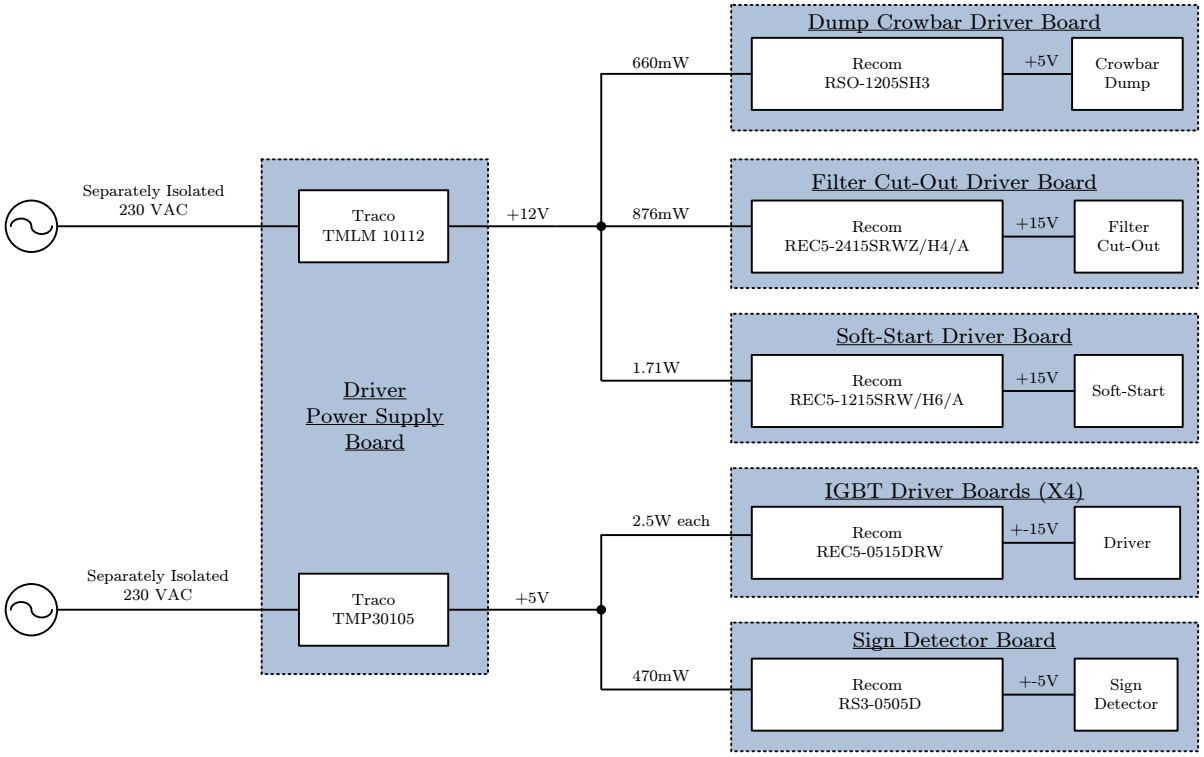



Figure A.29: Power distribution diagram for the driver power supply board.

allows each driver board to be isolated while using the same input voltage. It should be noted that all five driver boards could have been powered from a single +12 V rail but, due to a lack of availability of +12 V Recom power supplies, +5 V Recom supplies were used.

The power consumption of each driver board is measured under full load conditions and indicated at the input line of each block in the diagram.

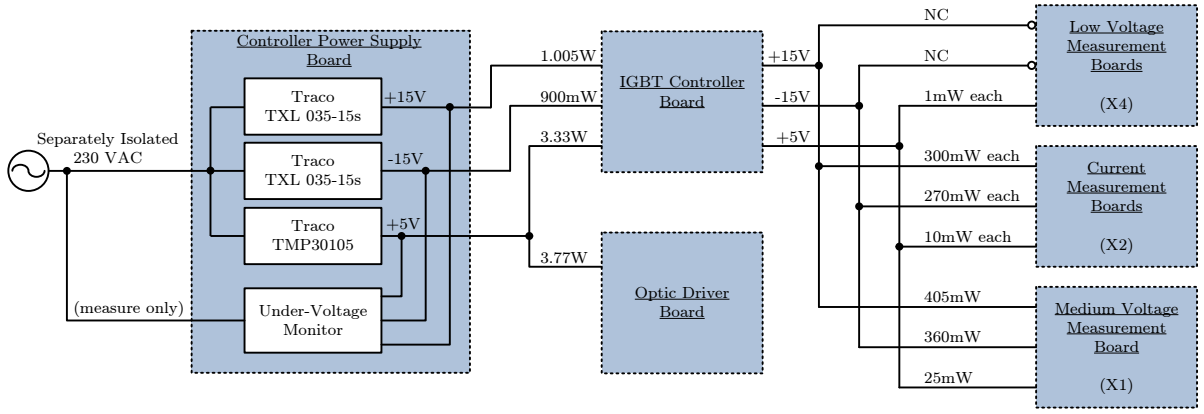



Figure A.30: Power distribution diagram for the controller power supply board.

The power distribution of the controller power supplies are shown in Figure A.30. The controller power supply is fed from a single isolated 230 V winding on the supply transformer. The 230 VAC is fed to two Traco TXL035-15s AC-to-DC supplies to provide

+15 V and -15 V rails. The 230 V input is also connected to a Traco TMP30105 AC-to-DC supply to provide +5 V rails.

From the figure is shown that the +5 V is fed to the controller and optic driver board while the ±15 V rails are only fed to the controller board. Since each measurement board is separately plugged into the controller board using shielded cable, the power supplies to the measurement boards have to run through the controller board as shown in the diagram. No additional isolation supplies are needed for the controller hardware since all the connected PC boards share the same common voltage.

The power consumption of the input supply rail to each board was measured and is indicated at the input of each block on the diagram.

### A.5.6 Summary

This section presented an overview of the layout of the control hardware in the form of functional block diagrams.

The main FPGA control was shown with it's ports and connections to the various peripheral boards. The ports consist of eight differential analogue inputs for translating analogue readings from the measurement boards, I/O ports for connecting the fibre-optic driver board and an I/O header for an external remote user interface. The controller board also has an LCD display and 4 tactile push buttons.

The FPGA controller board is based in the Cyclone III family of FPGA's from Altera. The analogue inputs are passed through a protection buffer, low pass filter and fast 12-bit analogue-to-digital converter. The I/O ports for the fibre-optic drivers are passed through a voltage lever shifter, to translate between the 5 V at the driver and 2.5 V at the FPGA. The remote user interface header are connected directly to the FPGA without any buffer or voltage translator.

In order to do measurements for control, three types of analogue measurement boards were presented: low voltage measurements (up to 1.2 kV), medium voltage measurements (1.2 kV to 14 kV) and current measurements (up to 200 A). The low voltage measurements are taken by measuring a differential voltage across voltage divider resistors. The medium voltage measurements are taken using the LEM LV100-4000/SP12 voltage transducer while current measurements are taken by using the LEM LA305-S current transducer.

In the last section, a complete overview of the small-signal power distribution is presented. Two small-signal transformers consisting of a primary winding and six isolated secondary windings are connected across the input bus of each AC-to-AC converter. This allows each module to be powered by its own transformer. The different secondary windings are then used as isolated sources to power the various drivers and power supply boards of each converter. Since there is only one controller, the controller power supply board was power from the lower converter module.

# A.6 Experimental hardware verification

## A.6.1 Overview

This section provides experimental verification of the hardware design. The dump-crowbar hardware design is evaluated in Section A.6.4 by disconnecting the small signal power to the controller while the AC-to-AC converter is switching a large load current. The voltage waveforms across the snubber capacitors are presented together with the current through the dump resistor. In Section A.6.5, the operation of the bypass-crowbar and filter cut-out is evaluated by triggering a pseudo-fault. The results are used verify the closing of the bypass and the protection of the bus capacitor by the filter cut-out and bleed resistor. An evaluation of the start-up and shut-down sequences are presented in section A.6.6 to confirmed safe turn-on and turn-off of the converter modules. The test is set up to verify if the converter module correctly takes up current from the bypass during start-up and correctly reverts current back to the bypass during shut- down. The regulator's voltage and current capabilities are verified in Section A.6.7. Due to limitations of the testing facility, the test is split up into two parts. The first test is set up to verify the voltage capability of the regulator and the second test is set up to verify the current capability of the converter modules.

A summary of the results are presented at the end of this chapter, in Section A.6.8.

## A.6.2 Test Setup

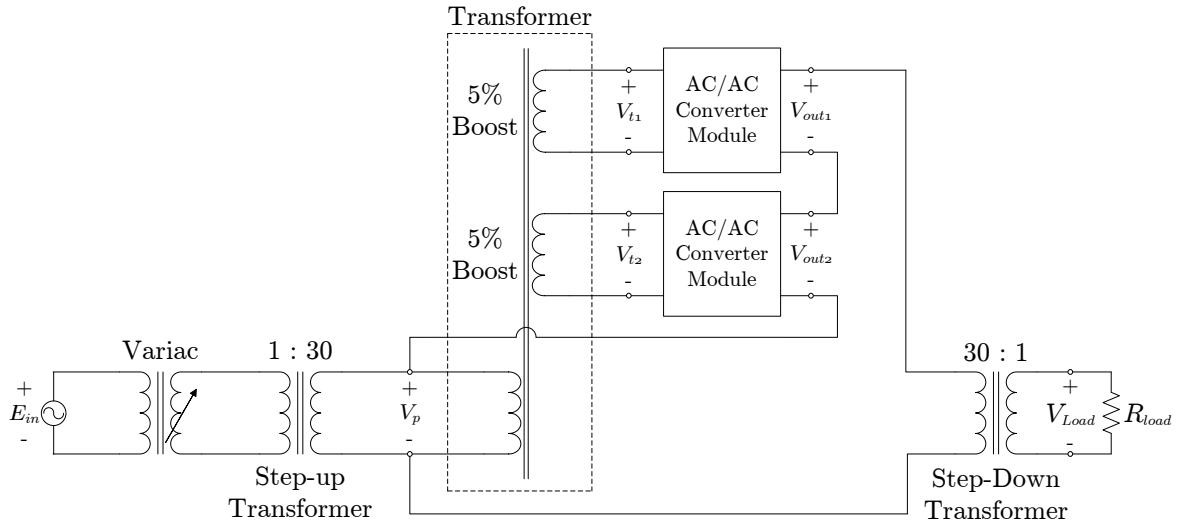


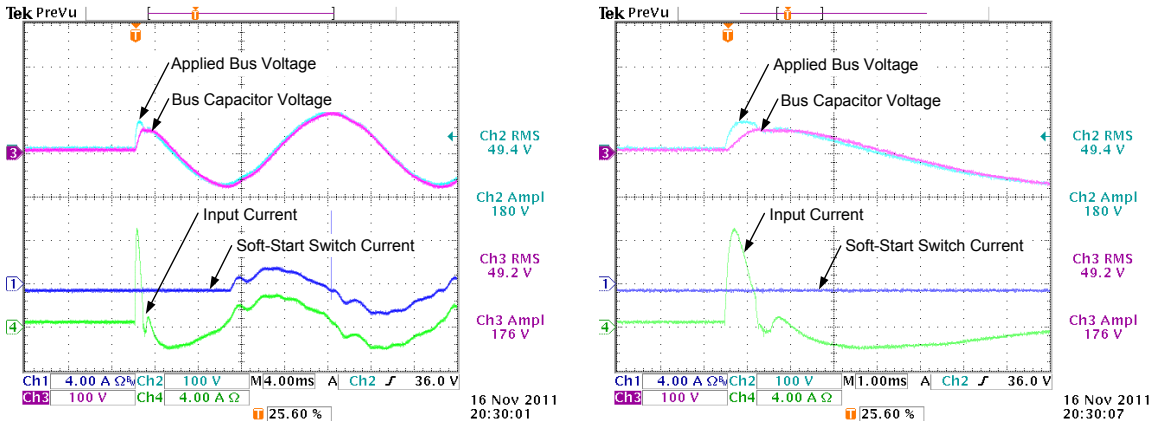

Figure A.31: Test setup for verifying the voltage regulator operation.

The MVEVR is designed to regulate the voltage of a 12.75 kV distribution feeder.The test facility does not have a 12 kV supply and a step-up and step-down transformer configuration is implemented. As shown in Figure A.31, the voltage capability test is set

up using a 400 V supply. The AC source is connected to a 400 V, 80 A variac which is stepped up to 12 kV using a step-up transformer. The variac provides a variable line voltage that is used to test the regulator operation at different input voltage levels. Lastly, a passive load is connected through a step-down transformer to the output of the voltage regulator.

The test setup is used in this section to verify the correct operation of the voltage regulator and its sub components.

### A.6.3 Soft-start Test




(a) Overview oscilloscope screen-shot of the soft-start operation.

(b) Close-up oscilloscope screen-shot of the soft-start operation.

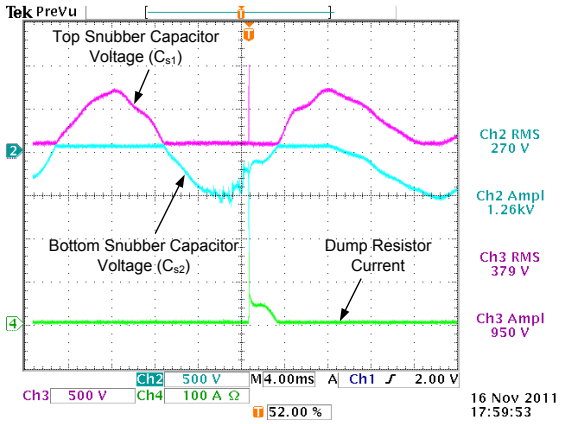
Figure A.32: Practical measurements of the soft-start operation.

The converter modules have large bus capacitors and if a distribution feeder voltage is applied at a peak, large inrush currents will occur. To limit the inrush current during power-up, a soft-start mechanism was introduced in Chapter A.4.5. The soft-start mechanism consists of soft-start resistor, connected in series with the capacitor and a soft-start switch, connected in parallel with the resistor.

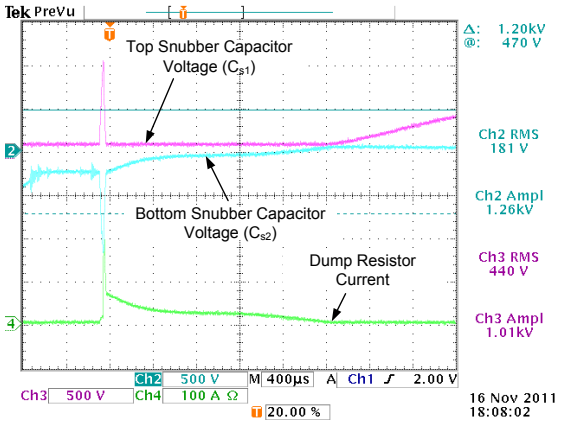
Practical measurements of the soft-start procedure is presented in Figure A.32. Initially the supply voltage is zero and the soft-start switch is open. As the source is applied, the bus voltage rises steeply while the bus capacitor is allowed to rise gradually. As shown, the input current has a damped spike when the voltage is applied, which limits the inrush. After the current reaches a zero-crossing, the soft-start switch is closed and the resistor is bypassed. This is indicated at the point where the switch starts conducting.

It is important to note that the initial inrush shown on the input current is a result of the bus capacitor and the snubber capacitors. However, since the snubber capacitors are small, their effect will be much less than that of the bus capacitor when higher voltages are applied. This test illustrated the correct operation of the soft-start mechanism and showed that the inrush current is successfully damped.

### A.6.4 Dump-crowbar Test




(a) Overview oscilloscope screen-shot of the snubber capacitor voltages and dump resistor current.




(b) Close-up oscilloscope screen-shot of the snubber capacitor voltages and dump resistor current.

Figure A.33: Practical measurements of a dump-crowbar trigger when the controller loses power during operation.

The dump-crowbar, presented in Chapter A.4.2, is designed to protect the input bus against over-voltage conditions. When the controller loses power, all the IGBTs are turned off and the only return paths for the leakage inductance and filter inductor currents are through the snubber and bus capacitors. The dump-crowbar is designed as self-triggering thyristors that close when the bus voltage exceeds 1200 V, which allows the energy to be dissipated in a dump resistor.

To evaluate the operation of the dump-crowbar, the small signal power supply to the controller board was turned off while the regulator was switching under a large load current. Figure A.33 shows the voltage across each snubber capacitor and the current through the dump resistor. As the power to the controller is removed, the control signals become unstable as shown by the ripple on the bottom snubber voltage. As the controller's power supply dies away, all the IGBTs are opened and the snubber capacitors are suddenly charged which results in a voltage spike. The bottom snubber capacitor reaches 1200 V before the top snubber and the bottom crowbar thyristor is triggered. As the thyristor is closed, the current through the dump resistor spikes as the voltage spike across the snubber is discharged. After the spike is discharged, the distribution feeder voltage source continues to drive the dump resistor until a zero-crossing is reached and the thyristor is turned off.

The results show that the dump-crowbar reacts quickly to over-voltage conditions and responds even when the small signal power supply is lost.

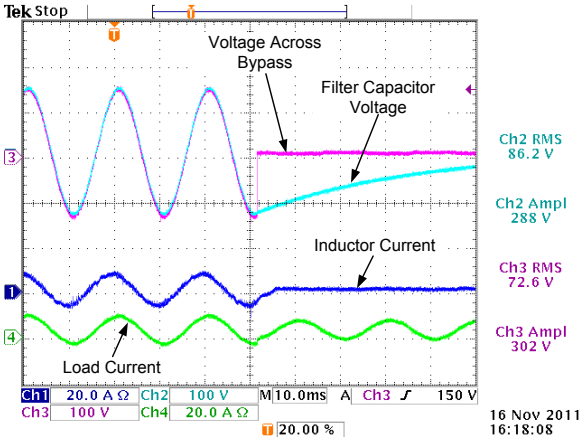



Figure A.34: Practical measurements of the bypass-crowbar and filter cut-out operation.

### A.6.5 Bypass and Filter Cut-out Test

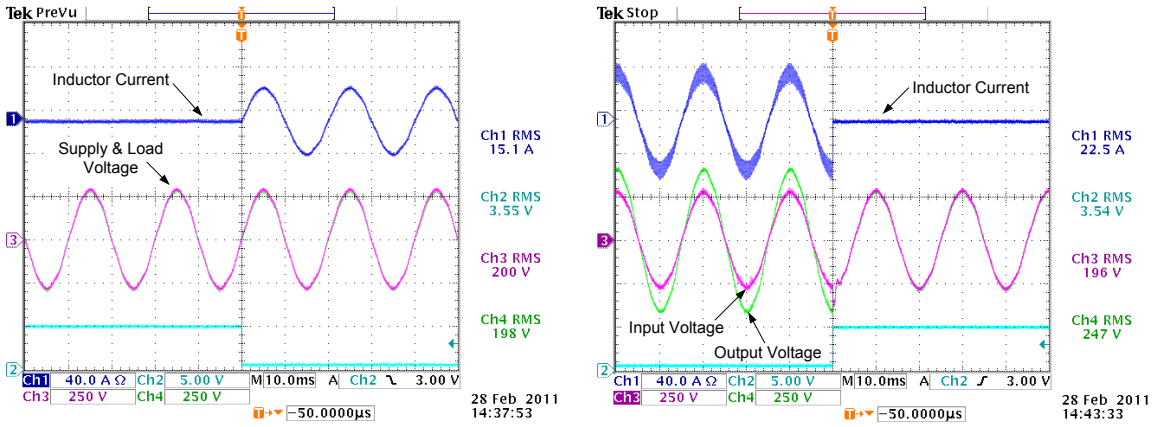
The bypass-crowbar, presented in Chapter A.4.3, is designed to protect the converter module during fault conditions and to ensure continuity of the distribution feeder. However, since the bypass-crowbar is connected across the output of the converter, a filter cut-out mechanism is implemented to protect the filter capacitor against being short circuited. The filter cut-out consists of a bleeding resistor that is connected in series with the capacitor and a cut-out switch, which is connected in series with the resistor. When the bypass is closed, the cut-out switch is opened and the capacitor is left to discharge through the resistor.

To evaluate the operation of the bypass and filter cut-out, a fault is triggered on the peak of the output voltage. Figure A.34 shows the measurement results of the bypass and filter cut-out. At the point when the bypass is closed, the voltage across the output of the converter drops to zero. At the same time, the converter stops switching and the filter cut-out is opened. The capacitor is left to discharge as shown, while the inductor current dies away. As the load current is diverted through the bypass, the output voltage is no longer boosted and a small drop in the load current is observed. This demonstrates the correct operation of the bypass by protecting the converter while maintaining continuity of the distribution feeder.

### A.6.6 Start-up and Shut-down

When the voltage regulator is turned off and connected to a source, the by-pass crowbar remains normally closed and allows the input to pass through to the load. When the regulator is turned on, the bypass-crowbar is opened and the current is passed through the AC-to-AC converter before switching commences. To safely switch over from the bypass to the converter, the controller waits for a voltage zero-crossing on the load side before opening the bypass.

Figure A.35a shows the measurement results of the system during start-up. Initially




(a) Input and output voltage with inductor current during start-up.

(b) Input and output voltage with inductor current during shut-down.

Figure A.35: Practical measurements of the complete voltage regulator during start-up and shut-down.

the bypass is closed, indicated by the zero inductor current. At a voltage zero-crossing, the bypass is opened and the current is passed through the inductor as shown. During this test, the converter was not set to boost, but simply to pass the input through after switching over. This process is clearly illustrated and proves to be successful.

When an over-voltage or over-current fault occurs, the bypass-crowbars are closed and the load current is diverted from the converters. This ensures that fault currents are not passed through the converter modules and maintains continuity of the distribution feeder.

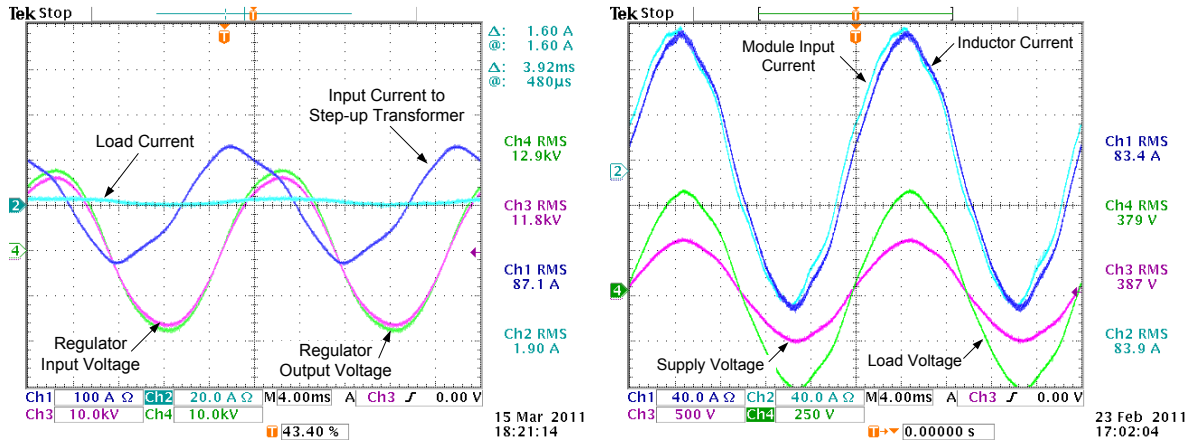
Figure A.35b shows the measurement results for a sudden fault trigger. The voltage regulator is set to boost when the fault is triggered. At the trigger, the bypass is closed and the converter stops switching. The output voltage drops to the same level as the input voltage and the filter inductor current drops to zero. This shows that the system can safely bypass the converter on the account of a fault.

### A.6.7 Voltage Regulator Open-Loop Boosting Capability Test

To verify the correct operation of the designed hardware at the specified ratings, the system is tested using open-loop PWM control. Due to limitations of the testing facility, the voltage capability test and current capability test cannot be performed at the same time.

The regulator is supplied with 11.8 kV and set to boost with 9 %. Measurement results for the voltage capability test are shown in Figure A.36a. The input voltage is shown to be 11.8 kV and an output voltage of 12.9 kV. This demonstrates that the hardware can switch at the specified voltage ratings while boosting at a specified setting.

Due to the limitations of the variac and the supply line, the voltage regulator cannot be tested for the full current rating of 100 A at 12 kV. To evaluate the current capability, the converter modules are directly connected to the variac by removing all the other




(a) Voltage capability test.

(b) Current capability test.

Figure A.36: Practical measurements of the complete voltage regulator for voltage and current capability tests.

transformers. Figure A.36b shows the input current and filter inductor current for one AC-to-AC converter module while switching. It is shown that the converter is able to switch 83.4 A while boosting the input voltage. Although the current rating of 100 A could not be verified, the test result of 83.4 A is sufficient to prove feasibility.

These test results show that the practical regulator measurements comply with the design specifications. The following sections will continue to evaluate the voltage regulator under closed loop control.

### A.6.8 Summary

Before the voltage regulator was tested at the full voltage rating, the correct operation of the hardware and protection mechanisms were evaluated at lower test voltages. In Section A.6.3, the soft-start mechanism was verified to ensure that the inrush currents are limited to acceptable levels. Test results showed the soft-start mechanism is able to successfully limit the inrush currents and proves to be effective.

In Section A.6.4, the dump-crowbar was evaluated by removing the small signal power to the controller while the AC-to-AC converter is switching a large load current. Results showed that the breakover diode circuit is successful in triggering a dump-thyristor when the snubber or bus capacitors exceeded 1200 V.

The operation of the bypass-crowbar and filter cut-out was evaluated in Section A.6.5 by triggering a pseudo-fault. Results showed that the filter cut-out opens as the bypass is closed. The bus capacitor is able to safely discharge while the load current is diverted through the bypass which confirms a successful design.

Section A.6.6 presented an evaluation of the start-up and shut-down sequences and confirmed safe turn-on and turn-off. The converter module was able to safely take up current at a zero-crossing, as the bypass was opened. Furthermore, it was also shown

that converter can safely shut down and revert the current back to the bypass.

Finally, in the last hardware test, the voltage regulator's voltage and current capabilities were evaluated in Section A.6.7. Due to limitations of the testing facility, the test was split up into two parts. One test was set up to verify the voltage capability and the other test was set up to verify the current capability. Both tests were performed using open-loop PWM control. Measurement results showed that the regulator was able to boost the input from 11.9 kV. Furthermore, the current capability test showed that the converter modules can safely be switched at the specified current ratings.

# Appendix B

# Design of the driver and measurement boards for the medium voltage electronic voltage regulator

## B.1 Overview

This chapter presents the detail design of the driver and measurement boards of the MVEVR. The following sections present a description of the hardware, the requirements and the detail design of the circuits. Note that the detail design of the controller board is not included in this chapter and can be found in [62].

The designs presented in this chapter are the result of several design iterations and may differ from the schematics of the PCB versions installed on the actual system. However, most PC-boards on the actual system have been adapted to match the designs presented in this chapter.

**Acknowledgement**

I would like to acknowledge and thank Heinrich Fuchs, especially for his contribution to the design of the main IGBT drivers, the soft-start drivers as well as the sign detector board.

**The following designs are discussed in this chapter:**

- Section B.2: Dump-crowbar driver
- Section B.3: Bypass driver
- Section B.4: Filter cut-out driver
- Section B.5: Soft-start drivers

- Section B.6: Main IGBT drivers
- Section B.7: Sign detector
- Section B.8: Low voltage measure board
- Section B.9: Medium voltage LEM measure board
- Section B.10: LEM current measure board

Table B.1: Dump-crowbar thyristor configuration component values.

| **Dump-Crowbar Thyristor Configuration** | | |
|---|---|---|
| Designator | Value/Model | Description |
| $R_1$, $R_3$ | 700 Ω | |
| $R_2$, $R_4$ | 1.18 kΩ | |
| $R_{s+}$, $R_{s-}$ | 68 Ω | |
| $C_1$, $C_2$ | 47 nF | |
| $C_{s+}$, $C_{s-}$ | 330 nF | |
| $D_1$, $D_4$ | IXBOD1-12RD | 1200 V breakover diode |
| $D_2$, $D_5$ | 1N5333BG | 3.3 V Zener diode |
| $D_3$, $D_6$ | ES2D | Ultrafast plastic rectifier |
| $T_{d+}$, $T_{d-}$ | SKMT92/16E | Thyristor |

## B.2 Dump Crowbar Driver Board Design

### B.2.1 Description and Requirements

The design of the dump crowbar topology and breakover-diode trigger circuit was discussed in Section A.4.2 of the hardware design chapter. A circuit diagram with the thyristor configuration and breakover-diode trigger circuits are shown in Figure B.1. The breakover-diode circuit was designed to automatically trigger the thyristors during a fault condition, when the forward voltage across a thyristor exceeded 1200 V. Since the breakover-diode circuit reacts independently from the main controller, feedback is needed to tell the controller when a fault has occurred. This requires the implementation of a trigger detection circuit that measures the gate voltage and communicates to the controller via an fibre-optic link when the gate threshold voltage is exceeded.

Typically, the voltage across the gate and cathode of the thyristor is measured to determine when the thyristor is turned on. However, when using the breakover diode circuit with smaller, faster thyristors, the rise in voltage at the gate is small and the turn-on time quick. As a result, turn-on is not always captured and the controller does not respond to the trigger. To improve accuracy the gate trigger is measured before the two protection diodes, indicated at $V_{detect\_top}$ for the top thyristor and $V_{detect\_bottom}$ for the bottom thyristor, as shown in Figure B.1.

The breakover diode circuit only drives the thyristor gate until the it has turned on. The maximum gate pulse width can therefore be taken as the thyristor turn-on time, which is in the order of 3 $\mu$s. To make sure that the controller acknowledges the fault trigger, the trigger detection circuit must extend the measured gate pulse width up to at least 1 ms.

The two thyristor cathodes are joined together, which places the common voltage for both thyristor drivers at the same potential, 0 $V_{iso}$. This allows for the design of one trigger detection circuit to detect a rise in gate voltage on both thyristors and one fibre-optic transmitter to communicate to the controller.

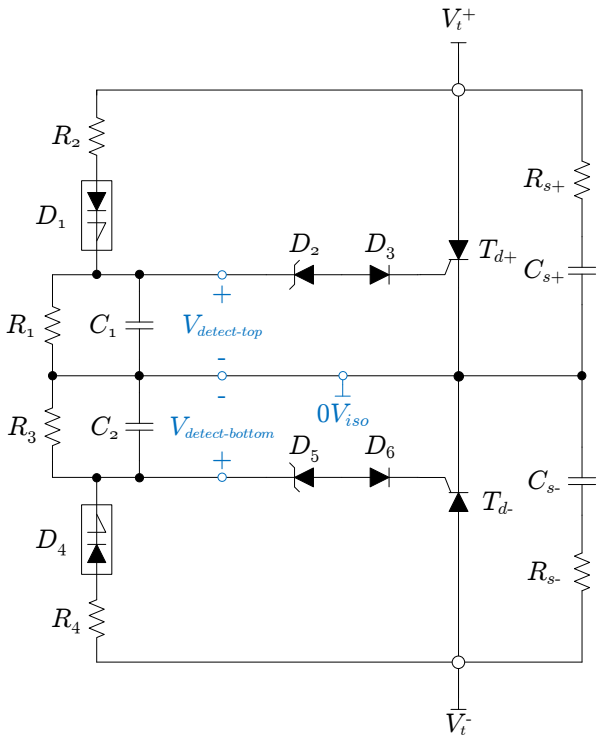



Figure B.1: Schematic diagram of the dump crowbar thyristor configuration.

## B.2.2 Design

### Power Supply

The layout of the power supplies to the controller and driver boards were discussed in Section A.5.5 of the hardware design chapter. The driver boards for the protection mechanisms are all fed from a single isolated +12 V rail. However, the common voltage for the dump crowbar differs from that of the bypass crowbar and the filter cut-out. For this reason, a regulated DC-to-DC converter with 3 kV isolation from Recom is considered. Model RSO-1205SH3 is a 12 V to 5 V, single rail, regulated DC-to-DC converter with a 1 W power capability. The voltage regulator is indicated in Figure B.2 by $U_1$. The Recom unit requires no additional components but, due to the cabling of the 12 V rail, two capacitors are added to the input side to provide stability and to filter high frequency noise. The value for $C_1$ is chosen as 4.7 $\mu$F to provide rail stability while $C_2$ is chosen as 100 nF to filter any high frequency noise. The control pin 3 on $U_1$ is used to power down the regulator. That function is not used and pin 3 can simply be grounded at the input side. The two output pins are regulated and can directly be used as the supply rails for the isolated circuit.

### Trigger summation

The thyristor cathodes are connected to each other such that the common voltage for both thyristor breakover-diode circuits are at the same voltage node. Since only one

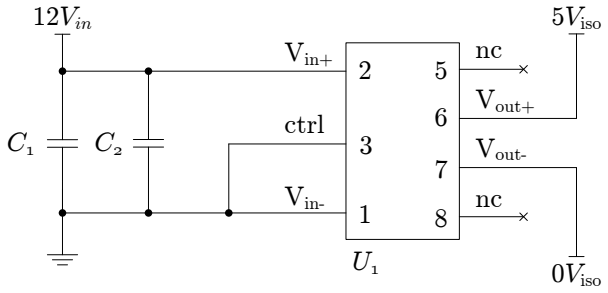



Figure B.2: Schematic diagram of the dump-crowbar trigger detector power supply.

Table B.2: Dump-crowbar trigger detector power supply component values.

| **Dump-Crowbar Trigger Detector Power Supply** | | |
|---|---|---|
| Designator | Value/Model | Description |
| $C_1$ | 4.7 $\mu$F | |
| $C_2$ | 100 nF | |
| $U_1$ | RSO-1205SH3 | Isolated DC-DC Regulator |

thyristor will trigger at a time, a single detection circuit can be used to monitor the voltage at both gates. The two gate voltages are monitored simultaneously by using a trigger summation circuit that acts as a logic OR function. This circuit is indicated in the "Trigger Summation" block in Figure B.3.

The small signal diodes, $D_1$ and $D_2$, together with the limiting resistors, $R_1$ and $R_2$, allow for only the gate with the highest voltage to pass to the trigger detector circuit. Resistor $R_3$ provides a path for the current to allow the diodes to turn on. This results in an OR function where the gate with the highest voltage is passed while the gate with the lower voltage is blocked.

Resistors $R_1$ and $R_2$ forms a voltage divider circuit with $R_3$. If all three resistors are chosen to be 10 k$\Omega$, voltage node $V_2$ becomes

$$V_2 = \begin{cases} \frac{1}{2}(V_{detect\_top} - V_f) & \text{when} \quad V_{detect\_top} > V_{detect\_bottom} \\ \frac{1}{2}(V_{detect\_bottom} - V_f) & \text{when} \quad V_{detect\_bottom} > V_{detect\_top} \end{cases} \tag{B.1}$$

where $V_f$ is the forward bias voltage of the diodes.

### Trigger detector

The trigger detector circuit consists of a comparator, configured to pull the output low when the input voltage exceeds a threshold. The threshold reference voltage is obtained by using a voltage divider, using $R_5$ and $R_6$. If the threshold voltage is chosen as 600 mV and $R_6$ as 10 k$\Omega$, $R_5$ can be taken as 68 k$\Omega$. To keep the input impedance of the comparator high, $R_4$ and $R_7$ are both chosen as 10 k$\Omega$. To eliminate chatter around the comparator trigger voltage, hysteresis is added by placing a 330 k$\Omega$ resistor, $R_{14}$, between the positive

input and output of the comparator. Doing a nodal analysis, the threshold voltage at the positive input becomes 0.88 V when the comparator output is *HIGH* and 0.606 V when the output is *LOW*.

Capacitor $C_1$ is chosen as 100 nF to filter any high frequency noise from the supply rail that may affect the voltage reference. Resistor $R_8$ provides loading for the output of the comparator and can be chosen as 10 kΩ. To protect the comparator against high voltage spikes, the input is protected by selecting a 3.3 V Zener diode at $D_3$.

### Extend trigger pulse width

The gate trigger pulse of the thyristor is of a short duration, in the order of 3 $\mu$s. To ensure that the controller acknowledges the trigger pulse, a 555-timer is implemented to extend the trigger pulse width. The 555-timer circuit, shown in the *Extend trigger pulse width* block in Figure B.3, is set up for mono stable operation with a normally low output. With the application of a negative-going pulse to the TRIG pin, the output is driven high. The output duration, $t_w$, is determined by $R_{10}$ and $C_3$ and given by

$$t_w = 1.1 R_9 C_3. \tag{B.2}$$

By choosing $R_{10}$ as 10 kΩ and $C_3$ as 100 $\mu$F, the output pulse duration becomes 1.1 ms. Resistor $R_9$ is used as a pull-up resistor for the output port and can be taken as 1 kΩ. For mono stable operation, capacitor $C_2$ is connected to pin 5 and chosen as 100 nF.

### Fibre-optic driver and transmitter

The fibre-optic transmitter, model HFBR1521, is typically driven by a high speed voltage comparator such as the LM311. In Figure B.3, the comparator is given by $U_3$ and the optic transmitter by $U_4$. To protect the system against damaged fibre-optic links, the transmitter is set up to transmit a *HIGH* signal when no fault is triggered and a *LOW* signal when a fault occurs.

The internal comparator of the LM311 is set up to turn the transistor of the output-stage off when the input is *true* and on when the input is *false*. Using the 5 V supply rail, resistors $R_{11}$ and $R_{12}$ are used as a voltage divider for obtaining a threshold voltage of 2.5 V. Both resistors can therefore be chosen as 10 kΩ. Capacitor $C_4$ is used to filter high frequency noise from the reference voltage and can be chosen as 100 nF. The output of the 555-timer is connected to the negative input terminal of the comparator. When a fault occurs, the output of the 555-timer is driven high, the comparator input becomes *false* and the output transistor in $U_3$ is turned on. When the output transistor is on, the optic transmitter is short circuited and no signal is transmitted. When the input to the comparator is *true*, the transistor is open and an optic signal is transmitted.

The typical forward input current, $I_{Fdc}$, of the optic transmitter is given in the data sheet as 60 mA with a forward voltage, $V_f$, of 1.67 V . The forward current is limited by

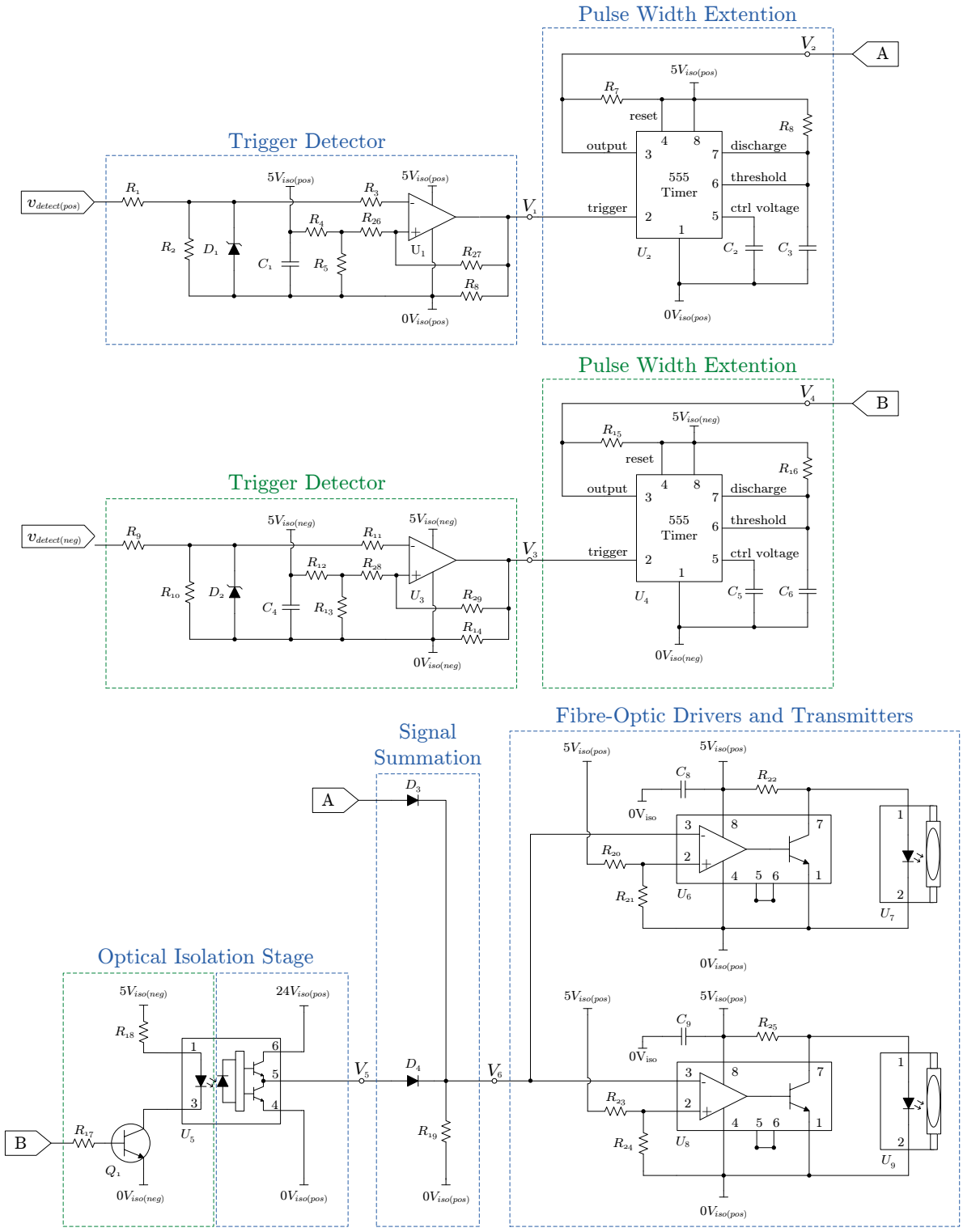



Figure B.3: Schematic diagram of the dump-crowbar trigger detector circuit.

Table B.3: Dump-crowbar trigger detector circuit component values.

| **Dump-Crowbar Trigger Detector Circuit** | | |
|---|---|---|
| Designator | Value/Model | Description |
| $R_1$, $R_2$, $R_3$, $R_4$, $R_6$, $R_7$, $R_8$, $R_9$, $R_{10}$, $R_{11}$, $R_{12}$ | 10 kΩ | |
| $R_5$ | 68 kΩ | |
| $R_{13}$ | 55 Ω | |
| $R_{14}$ | 330 kΩ | |
| $D_1$, $D_2$ | 1N148W-V-GS08 | Small singnal Fast swithing diode |
| $D_3$ | 1N5337BG | 4.7 V Zener Diode |
| $C_1$, $C_2$, $C_3$, $C_4$ | 100 nF | |
| $C_5$ | 4.7 $\mu$F | |
| $U_1$ | TLV3501 | High-Speed Comparator |
| $U_2$ | NE555D | Precision Timer |
| $U_3$ | LM311D | Differential Comparator |
| $U_4$ | HFBR1521 | Fibre-Optic Transmitter |

resistor $R_{13}$. If the forward voltage is taken as 1.67 V, the voltage across the $R_{13}$ becomes 3.33 V. Using Ohm's law, the required resistance for limiting the current to 60 mA is 55.5 Ω.

Since $R_{13}$ is a current limiting resistor, it is important to take its power consumption into account. Using the current and voltage across $R_{13}$, the power consumption of the resistor becomes

$$\begin{aligned} P_{R12} &= (5V_{iso} - V_f) \cdot I_{Fdc} \\ &= (3.33\ V) \cdot 60\ \text{mA} \\ &= 200\ \text{mW} \end{aligned} \tag{B.3}$$

To limit the effect of parasitic inductance on the 5 $V_{iso}$ rail on the turn-on time of the optic transmitter, capacitor $C_5$ is placed close to the current limiting resistor $R_{13}$. The datasheet of the optic transmitter recommends a value of 4.7 $\mu$F for $C_5$.

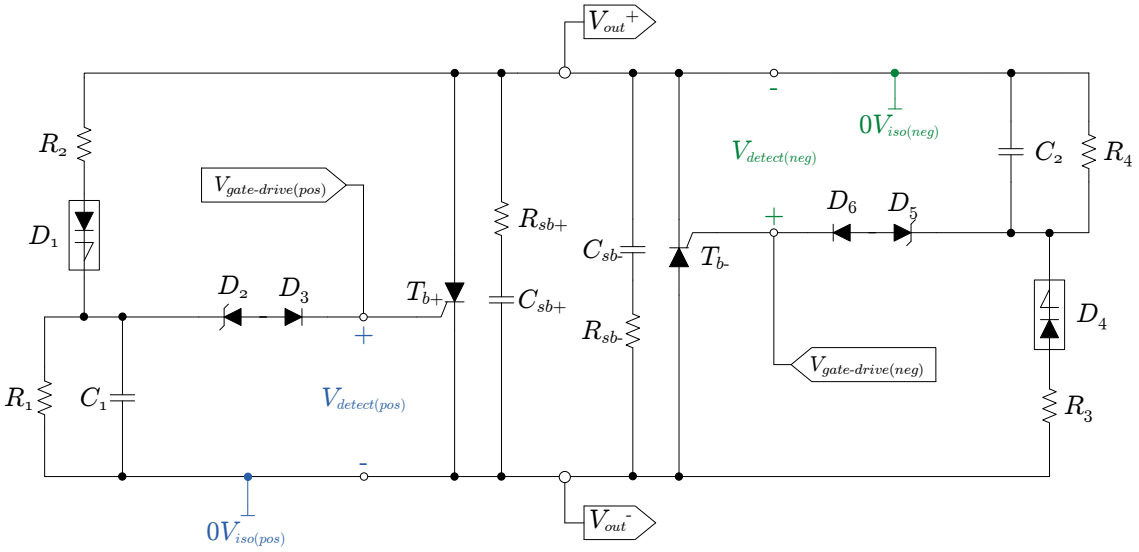



Figure B.4: Schematic diagram of the bypass crowbar thyristor configuration.

# B.3 Bypass Driver Board Design

## B.3.1 Description and Requirements

The design of the bypass-crowbar topology was discussed in Section A.4.3. The schematic diagram of the bypass-crowbar, given in Figure B.4, shows the two anti-parallel thyristors, $T_{b+}$ and $T_{b-}$, with their respective $RC$-snubbers and breakover-diode trigger circuits. The bypass crowbar is required to operate within three modes of operation.

During the first mode of operation, the main controller is operational and has full control over the bypass. The controller should be able open and close the bypass at will. The second mode of operation ensures continuity of the distribution feeder when the controller fails. When the control signal from the main controller is lost, the bypass acts as a normally closed switch by firing the thyristors using its own independent power supplies. During the third mode of operation, the breakover-diode triggers are used to close the bypass. The breakover-diode triggers override the control signal from the controller and closes the bypass when the voltage across a thyristor exceeds 1200 V.

Since the bypass can trigger on its own, the control signal for the filter cut-out is communicated directly from the bypass driver to the filter cut-out driver. This requires two optic transmitters, one for feedback to the controller and one for controlling the filter cut-out.

The crowbar driver board can be divided into two functional circuits. The one functional circuit detects and communicates the status of the thyristors to the controller and filter cut-out, much like the driver board of the dump-crowbar. The other functional circuit is a manual thyristor driver that reads a control signal from the controller and fires the thyristors accordingly.

Table B.4: Bypass-crowbar thyristor configuration component values.

| **Bypass-Crowbar Thyristor Configuration** | | |
|---|---|---|
| Designator | Value/Model | Description |
| $R_1$, $R_3$ | 700 Ω | |
| $R_2$, $R_4$ | 1.18 kΩ | |
| $R_{sb+}$, $R_{sb-}$ | 68 Ω | |
| $C_1$, $C_2$ | 47 nF | |
| $C_{sb+}$, $C_{sb-}$ | 330 nF | |
| $D_1$, $D_4$ | IXBOD1-12RD | 1200 V breakover diode |
| $D_2$, $D_5$ | 1N5333BG | 3.3 V Zener diode |
| $D_3$, $D_6$ | ES2D | Ultrafast plastic rectifier |
| $T_{b+}$, $T_{b-}$ | SKET740 | Thyristor |

## B.3.2 Design

### Power Supplies

Unlike the dump crowbar, the two thyristors are connected in anti-parallel. This requires two separately isolated driver and trigger detector circuits with two isolated power supplies. In Figure B.4, the common voltage for $T_{b+}$ is given by $0V_{iso(pos)}$ and the common voltage for $T_{b-}$ by $0V_{iso(neg)}$.

The circuit diagram of the isolated power supplies are shown in Figure B.5. The bypass crowbar operates independently from the main controller and requires its own power supplies. A transformer with one primary and two secondary windings are connected across the 635 V input bus of each AC-to-AC converter module as discussed in the power management design in Section A.5.5. The 635 V bus voltage is stepped down to 19 V and used to power the isolated thyristor drivers. This ensures that the thyristors are always powered when the MVEVR is connected to the grid.

The isolated power supplies each consists of a simple full-bridge rectifier circuit. The 19 VAC input is rectified to 24 VDC using a full-bridge rectifier IC, DBLS201G-RD, from TSC. The rectifiers are indicated by $D_1$ and $D_2$ in Figure B.5. Capacitors $C_1$ and $C_3$ are used to filter the ripple component from the rectified voltage. Designing for 1 A current with a 1 V ripple, the capacitance of the filter capacitor is calculated by approximating

$$I_c \approx C\frac{\Delta v}{\Delta t} \tag{B.4}$$

and rewriting for C such that

$$\begin{aligned} C &= I\frac{\Delta t}{\Delta v} \\ C &= (1\text{ A})\frac{10\text{ ms}}{1\text{ V}} \\ C &= 10000\ \mu\text{F}. \end{aligned} \tag{B.5}$$

A 5 V supply is obtained by using a simple, LM7805, linear regulator with a 1 A current rating. The voltage regulator, indicated by $U_1$ and $U_2$, is directly connected to

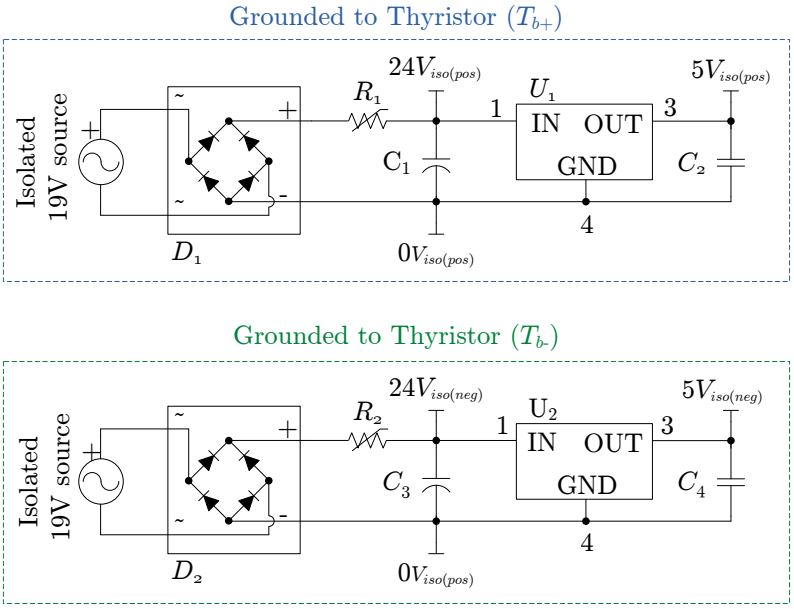



Figure B.5: Schematic diagram of bypass-crowbar power supplies.

Table B.5: Bypass-crowbar power supplies component values.

| **Bypass-Crowbar Power Supplies** | | |
|---|---|---|
| Designator | Value/Model | Description |
| $R_1$, $R_2$ | B57237-S220-M | Thermistor |
| $D_1$, $D_2$ | DBLS201G-RD | Full bridge rectifier |
| $U_1$, $U_2$ | MC7805CD2T | 5 V Regulator |
| $C_1$, $C_3$ | 10000 $\mu$F | |
| $C_2$, $C_4$ | 100 nF | |

the 24 V supply rail as shown in the figure. A 100 nF smoothing capacitor is connected to the 5 V rail at the output of the regulator to eliminate possible high frequency noise. The smoothing capacitors are given by $C_2$ and $C_4$.

### Bypass Trigger Detection

Figure B.6 presents a functional block diagram of the trigger detection implementation. Each thyristor has its own isolated trigger detector circuit, powered by the isolated power supplies. The trigger for $T_{b+}$ is grounded at $0V_{iso(pos)}$ as well as the ground plane for the fibre-optic transmitters. The trigger for $T_{b-}$ is grounded to $0V_{iso(neg)}$ and the trigger signal is communicated to the side with the optical transmitters using an optocoupler. The signal of the two trigger detection circuits are added using an OR-function circuit and transmitted using fibre-optic transmitters.

The circuit diagram of the bypass trigger detection circuits are shown in Figure B.7. The circuit consists of two isolated *trigger detector* and *pulse width extension* circuits that are identical to the corresponding circuit block designs of the dump-crowbar driver board discussed in Section B.3.

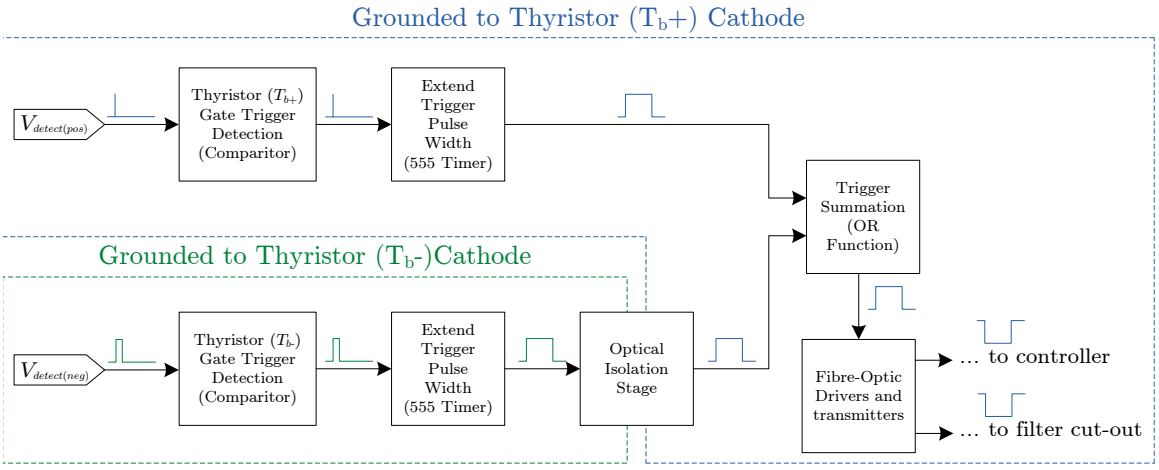



Figure B.6: Functional block diagram of the bypass-crowbar trigger detector circuit.

Since the two trigger detector circuits have different ground planes at different voltage potentials, the trigger signal at $V_4$ is translated to $V_5$ using an optocoupler, as shown in the *Optical Isolation State* block in Figure B.7. The maximum voltage difference between the two ground planes is limited to the peak voltage across the bypass-crowbar, which is 1200 V.

The ACPL-W302 optocoupler from Avago has an isolation barrier of 1000 VAC for continuous and is used to implement $U_5$. The input side is driven by transistor $Q_1$ and current limiting resistor $R_{18}$. If the input current is chosen as 15 mA and the supply rail as 5 V, $R_{18}$ can be chosen as 330 Ω. Any general purpose NPN transistor, such as the MMBT2222A, can be used to implement $Q_1$. During the on-state, the transistor should be driven into saturation. The base current is determined by $R_{17}$ together with the pull-up resistor, $R_{15}$, of the 555-timer. However, $R_{15}$ should allow enough current to drive $Q_1$ on hard and should be chosen as 1kΩ. For safety, $R_{17}$ is added and chosen as 10 Ω. The output is pulled high to 24 V when the input is high and pulled to $0V_{iso(pos)}$ when the input is low.

The trigger signal from the two thyristors are added together using the same logic OR function as with the dump-crowbar. Resistor $R_{19}$ allows $D_3$ and $D_4$ to turn on and can be chosen as 10 kΩ.

The design of the fibre-optic transmitters are identical to the *Fibe-Optic Driver and Transmitter* design for the dump-crowbar.

### Thyristor Driver

The schematic diagram for the thyristor driver circuit is given in Figure B.8. The fibre-optic receiver, $U_1$, is implemented using the HFBR-2521 optic receiver from Avago. The output pin is connected to the internal 1 kΩ pull-up resistor and used to drive two transistors, $Q_1$ and $Q_2$. Transistor $Q_1$ directly switches the thyristor gate driver that is on ground plane, $0V_{iso(pos)}$, while $Q_2$ drives an optocoupler for switching the thyristor on

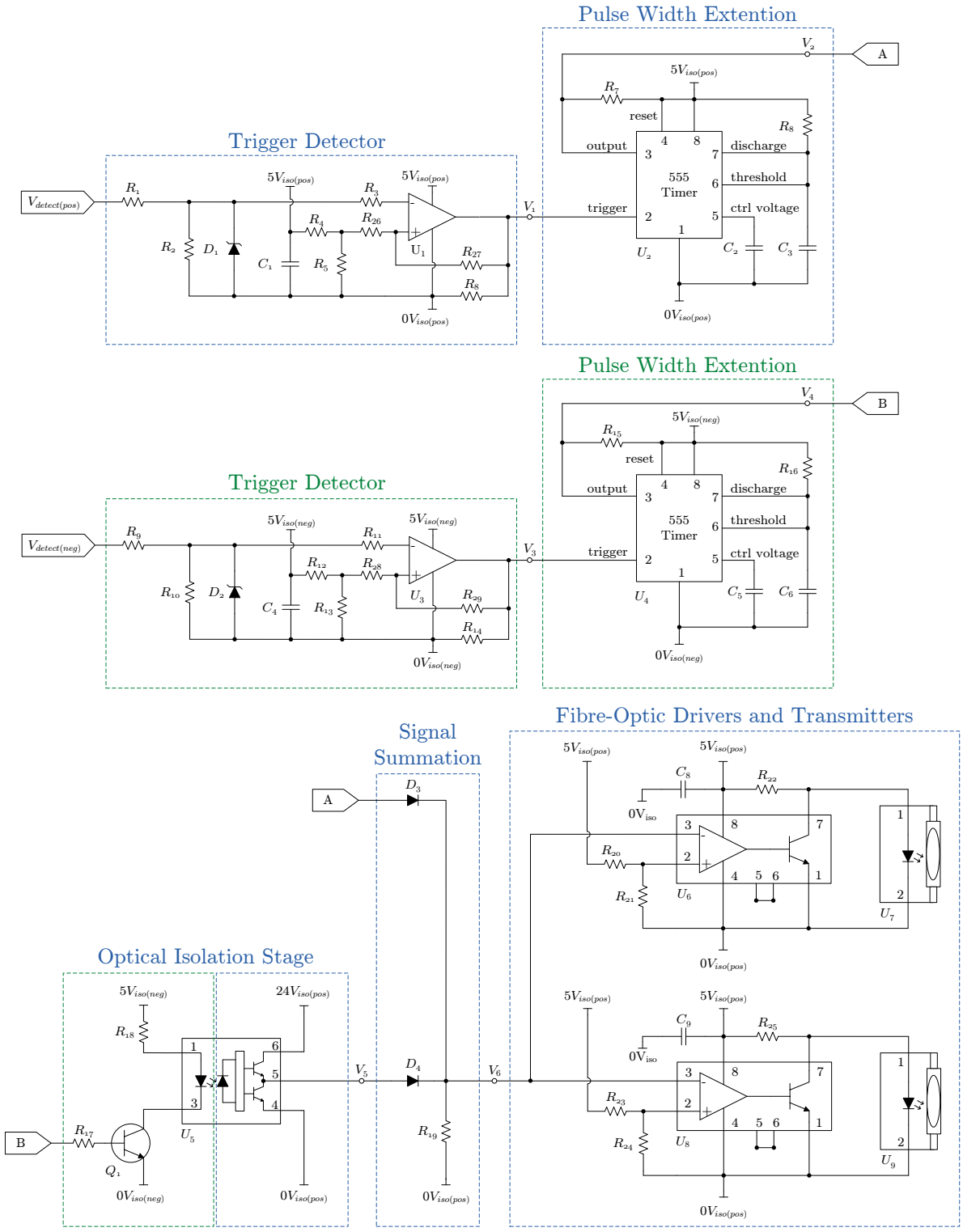



Figure B.7: Schematic diagram of the bypass-crowbar trigger detector.

Table B.6: Bypass-crowbar trigger detector component values.

| **Bypass-Crowbar Trigger Detector** | | |
|---|---|---|
| Designator | Value/Model | Description |
| $R_1$, $R_2$, $R_3$, $R_5$, $R_6$, $R_7$, $R_8$, $R_9$, $R_{10}$, $R_{11}$, $R_{12}$, $R_{13}$, $R_{14}$, $R_{16}$, $R_{19}$, $R_{20}$, $R_{21}$, $R_{23}$, $R_{24}$, $R_{26}$, $R_{28}$ | 10 kΩ | |
| $R_4$ | 68 kΩ | |
| $R_{15}$ | 1 kΩ | |
| $R_{17}$ | 10 Ω | |
| $R_{18}$ | 330Ω | |
| $R_{22}$, $R_{25}$ | 82Ω | 500 mW |
| $R_{27}$, $R_{29}$ | 330 kΩ | |
| $C_1$, $C_2$, $C_3$, $C_4$, $C_5$, $C_6$ | 100 nF | |
| $C_8$, $C_9$ | 4.7 $\mu$F | |
| $D_1$, $D_2$ | 1N5337BG | 4.7 V Zener Diode |
| $D_3$, $D_4$ | 1N148W-V-GS08 | Small singnal Fast swithing diode |
| $Q_1$ | MMBT2222A | General Purpose NPN Transistor |
| $U_1$, $U_3$ | TLV3501 | High-Speed Comparator |
| $U_2$, $U_4$ | NE555D | Precision Timer |
| $U_5$ | ACPL-W302 | Optocoupler |
| $U_6$, $U_8$ | LM311D | Differential Comparator |
| $U_7$, $U_9$ | HFBR1521 | Fibre-Optic Transmitter |

ground plane, $0V_{iso(neg)}$.

The base resistors, $R_1$ and $R_7$, limit the base currents. However, both base resistors are pulled high through the 1 kΩ internal pull-up resistor of $U_1$ and a 10 Ω resistor can be used for both $R_1$ and $R_7$.

The optocoupler, $U_2$, is the same ACPL-W302 model used with the trigger detection circuit. Limiting the input current to 15 mA while using a 5 V voltage rail, resistor $R_8$ becomes 330 Ω.

When transistor $Q_1$ is turned off, MOSFET $Q_2$ is turned on and resistor $R_2$, in series with $R_3$, is used to limit the rate at which the gate of $Q_2$ is charged. However, when $Q_1$ is turned on, $R_2$ limits the current through $Q_1$ while $R_3$ limits the rate that the gate of the MOSFET is discharged. If the peak charging current is taken as ≈50 mA and the 24 V rail is used, $R_2$ can be chosen as 470 Ω and $R_3$ as 22 Ω. Both $Q_2$ and $Q_3$ can be implemented using the IRFS52N15DPbF power MOSFET from International Rectifier.

The driver circuit is designed to fire the thyristors when no control signal is received from the controller. When $Q_2$ is turned off, the gate of $Q_3$ is pulled high through $R_4$, $Q_3$ is turned on and current is passed to the thyristor gate. $R_4$ therefore limits the current through $Q_2$ and the rate with which the gate of $Q_3$ is charged. By limiting the current to ≈50 mA, $R_4$ can be chosen as 470 Ω.

Table B.7: Bypass-crowbar manual thyristor driver component values.

| **Bypass-Crowbar Manual Thyristor Driver** | | |
|---|---|---|
| Designator | Value/Model | Description |
| $R_1$, $R_7$ | 10 Ω | |
| $R_2$, $R_4$, $R_8$, $R_9$, $R_{10}$ | 470Ω | |
| $R_3$ | 22Ω | |
| $R_5$, $R_{11}$ | 22Ω | >30 W |
| $R_6$, $R_{12}$ | 10 kΩ | |
| $D_1$, $D_3$ | ES2D | Ultrafast Plastic Rectifier |
| $D_2$, $D_4$ | General purpose LED | |
| $U_1$ | HFBR2521 | Fibre-Optic Receiver |
| $U_2$ | ACPL-W302 | Optocoupler |
| $Q_1$, $Q_2$ | MMBT2222A | General Purpose NPN Transistor |
| $Q_3$, $Q_4$, $Q_5$, $Q_6$ | IRFS52N15DPBF | Power MOSFET |

Resistor $R_5$ limits the current injected into the gate of the thyristor. By limiting the gate current to ≈1 A, $R_5$ can be chosen as 22 Ω. To protect the driver against reverse recovery currents from the thyristor gate, diode $D_1$ is placed in series with the thyristor gate. To indicate when the thyristor is being fired, an LED, $D_2$, can be placed at the emitter of $Q_3$ with a current limiting resistor, $R_6$. The value for $R_6$ can be chosen as 10 kΩ.

The design of the *Isolated Thyristor Gate Driver* block is identical to the design of the *Thyristor Gate Driver* block with the exception of $R_9$. Resistor $R_9$ limits rate with which the gate of $Q_5$ is charged and discharged. If the peak charging current is limited to ≈50 mA, $R_9$ can be selected as 470 Ω.

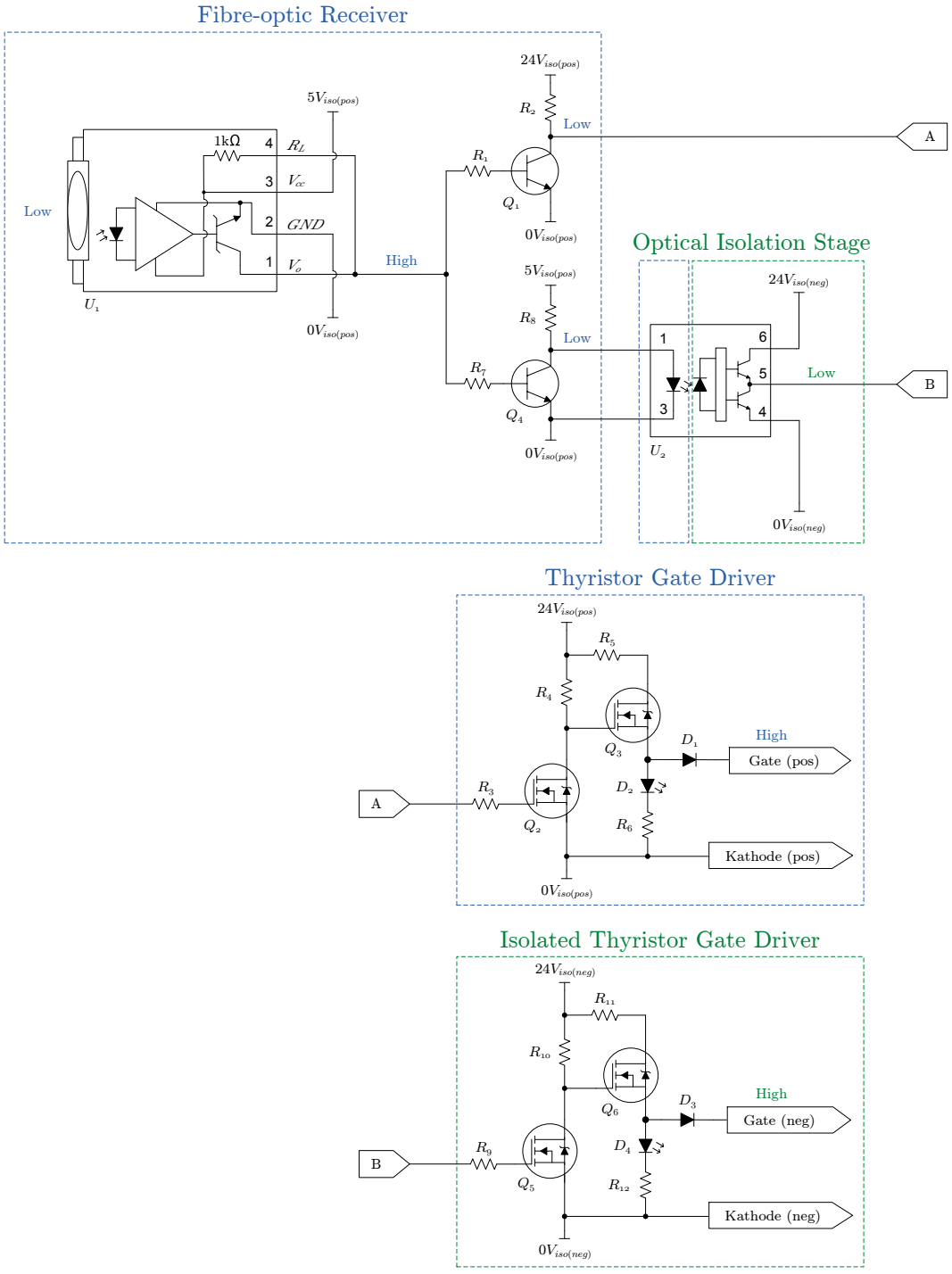



Figure B.8: Schematic diagram of the bypass-crowbar manual thyristor driver.

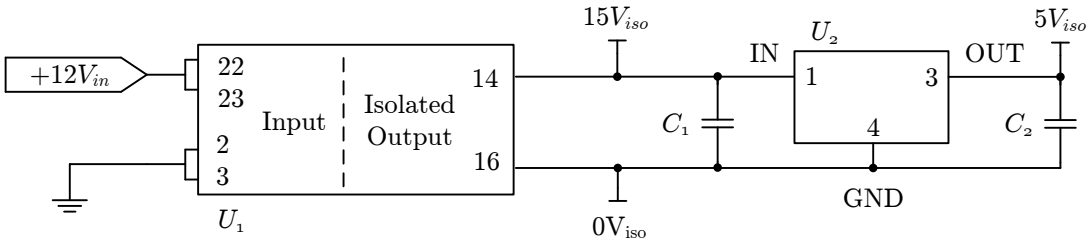



Figure B.9: Schematic diagram of the filter cut-out power supply.

# B.4 Filter Cut-out Driver Board Design

## B.4.1 Description and Requirements

This section discusses the design of a simple IGBT driver circuit for turning the filter cut-out IGBTs on and off. The filter cut-out driver receives its control signal from the bypass-crowbar via a fibre-optic receiver. To protect the filter capacitor against a faulty fibre-optic connection, the driver is designed to turn the IGBTs on when the signal is high and off when the signal is low. Therefore, should the signal be lost, the filter capacitor is safely disconnected.

## B.4.2 Design

### Power Supplies

The ground plane of the driver circuit is floating at the same potential as the IGBT emitters. Since the driver board is powered with the same 12 V supply as the dump-crowbar and soft-start, an isolated power supply is needed. The isolated DC-to-DC converter module, REC5-2415SRWZ/H4/A, from Recom is selected for this purpose. The Recom module accepts a 9 to 36 V input, has a regulated 15 V, 5 W output and offers 4 kVDC isolation.

The schematic diagram of the power supply circuit is given in Figure B.9. The Recom module, indicated by $U_1$, requires no support circuits and is directly connected to the 12 V input. The regulated output is directly used for the 15 V rail. However, capacitor $C_1$ is added to the 15 V output as a smoothing capacitor and can be chosen as 100 nF.

To supply 5 V to the fibre-optic receiver, a LM7805 linear voltage regulator is used. The regulator is indicated by $U_2$ in the circuit diagram. A smoothing capacitor, $C_2$, of 100 nF is connected to the output of $U_2$ to suppress noise on the 5 V rail.

### IGBT Driver Circuit

The filter cut-out consists of two back-to-back IGBTs. The two emitters are connected together and allows one driver circuit to be used to drive both IGBTs simultaneously. The circuit diagram of the IGBT driver circuit is shown in Figure B.10. The driver consists

Table B.8: Filter cut-out power supplies component values.

| **Filter Cut-Out Power Supplies** | | |
|---|---|---|
| Designator | Value/Model | Description |
| $U_1$ | REC5-2415SRWZ/H4/A | Isolated DC-DC Regulator |
| $U_2$ | MC7805CD2T | 5 V Regulator |
| $C_1$, $C_2$ | 100 nF | |

of a fibre-optic receiver, $U_1$, a transistor, $Q_1$, for translating the 5 V signal to 15 V and a complementary transistor pair, $Q_2$ and $Q_3$, to drive the IGBT gates.

The output of the optic receiver is connected to the internal, 1 kΩ, pull-up resistor pin. In order to translate the 5 V output of the optic receiver to 15 V, a general purpose, 2N222, NPN transistor is used. The transistor is either turned on hard or turned off completely. When $Q_1$ is turned off, $R_1$ acts as a pull-up resistor for the base of the complementary pair. When $Q_1$ is turned on, $R_1$ acts as a limiting resistor for the collector current.

Choosing the value for $R_1$ is a trade-off between the power dissipation and the speed with which $Q_2$ and $Q_3$ is switched. If the collector current is to be kept below 50 mA, $R_1$ can be chosen as 330 Ω. If $V_{ce(sat)}$ is given as 0.3 V, the collector current, $I_c$, when $Q_1$ is on, becomes 44.5 mA. The power consumed in $R_1$ is therefore given by

$$\begin{aligned} P_{R1} &= I_c^2 R_1 \\ &= (44.5 \text{ mA})^2 (330 \ \Omega) \\ &= 653.5 \text{ mW}. \end{aligned} \tag{B.6}$$

To allow a margin of safety, $R_1$ should therefore be chosen with a power rating of at least 1.2 W.

Resistors, $R_2$ and $R_3$, limit the rate of charge of the IGBT gates and determines the speed with which the IGBTs are turned on. From the IGBT data sheet, the gate resistor can be chosen between 2 Ω and 10 Ω. To ensure fast turn-on, $R_2$ and $R_3$ can be chosen as 6 Ω. When the IGBTs are switched at a high frequency, the losses in the IGBT gate resistor can be significant. However, the filter cut-out is used as a safety mechanism and will typically only switch during start-up, shut-down and fault conditions. But, for safety, $R_2$ and $R_3$ can be selected with a power rating of 1 W.

To minimise parasitic inductance when turning the IGBTs on, capacitor $C_1$ is chosen as $\approx$ 20 $\mu$F and placed close the the collector of $Q_2$. The IGBT gate has a maximum allowed gate voltage of ±20 V. To protect the gates against overvoltage conditions, 18 V Zener diodes $D_1$, $D_2$, $D_3$ and $D_4$ are placed appropriately between each gate and emitter.

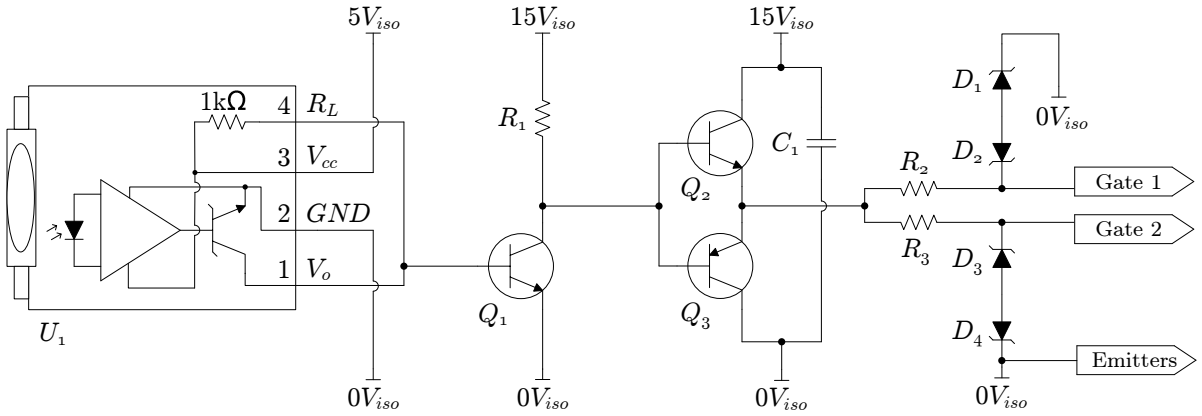



Figure B.10: Schematic diagram of the filter cut-out IGBT driver.

Table B.9: Filter cut-out IGBT driver component values.

| **Filter Cut-Out IGBT Driver** | | |
|---|---|---|
| Designator | Value/Model | Description |
| $R_1$ | 330Ω | |
| $R_2$, $R_3$ | 22Ω | 500 mW |
| $Q_1$ | MMBT2222A | General Purpose NPN Transistor |
| $Q_2$, $Q_3$ | PBSS4540Z | 40 V low VCEsat NPN transistor |
| $C_1$ | $\approx 20\mu$F | |
| $D_1$, $D_2$, $D_3$, $D_4$ | BZV55-C18 | 18 V Zener Diode |
| $U_1$ | HFBR2521 | Fibre-Optic Receiver |

## B.5 Soft-start Driver Board Design

### B.5.1 Description and Requirements

This section discusses the design of the soft-start mechanism. The soft-start mechanism works on the same basis as the filter cut-out, by disconnecting the bus capacitor and allowing it to charge through a soft-start resistor. Like the filter cut-out, the soft-start IGBTs are normally open until they are closed by the controller.

### B.5.2 Design

The same IGBTs and configuration that is used for the filter cut-out, is used for the soft-start. The design of the driver board therefore remains identical to the design of filter cut-out driver in Section B.4, with the exception of one additional circuit.

The soft-start mechanism on all the AC-to-AC converter modules are activated at the same instance in time. To save I/O ports on the controller, each soft-start driver board is given a fibre-optic transmitter for forwarding the signal to the soft-start of the next AC-to-AC converter module. The circuit diagram of the additional fibre-optic transmitter is given in Figure B.11. The circuit consists of a driver transistor $Q_4$ and an optic

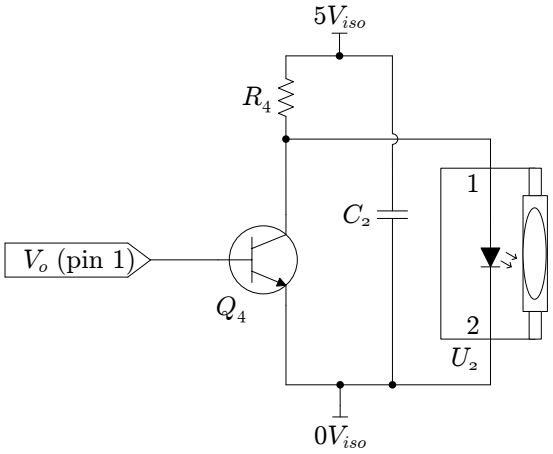



Figure B.11: Schematic diagram of the soft-start feedback circuit.

Table B.10: Soft-start feedback circuit component values.

| **Soft-Start Feedback Circuit** | | |
|---|---|---|
| Designator | Value/Model | Description |
| $R_4$ | 55 Ω | 250 mW |
| $C_2$ | 4.7 $\mu$F | |
| $Q_4$ | MMBT2222A | General Purpose NPN Transistor |
| $U_2$ | HFBR1521 | Fibre-Optic Transmitter |

transmitter, $U_2$. The base of $Q_4$ is directly connected to the output pin of the fibre-optic receiver, $U_1$, that is presented in Figure B.10.

The typical forward input current, $I_{Fdc}$, of the optic transmitter is given in the data sheet as 60 mA with a forward voltage, $V_f$, of 1.67 V . The forward current is limited by resistor $R_4$. If the forward voltage is taken as 1.67 V, the voltage across the $R_4$ becomes 3.33 V. Using Ohm's law, the required resistance for limiting the current to 60 mA is 55.5 Ω.

Since $R_4$ is a current limiting resistor, it is important to take its power consumption into account. Using the current and voltage across $R_4$, the power consumption of the resistor becomes

$$\begin{aligned} P_{R4} &= (5V_{iso} - V_f) \cdot I_{Fdc} \\ &= (3.33\ V) \cdot 60\ \text{mA} \\ &= 200\ \text{mW} \end{aligned} \tag{B.7}$$

To limit the effect of parasitic inductance on the 5 $V_{iso}$ rail on the turn-on time of the optic transmitter, capacitor $C_2$ is placed close to the current limiting resistor $R_4$. The datasheet of the optic transmitter recommends a value of 4.7 $\mu$F.

# B.6 Main IGBT Driver Board Design

## B.6.1 Description and Requirements

This section discusses the design of the driver boards for the main IGBTs of the AC-to-AC converter. Each IGBT driver board requires an IGBT gate drive circuit for switching the IGBTs and a desaturation (DESAT) detection circuit for protecting the IGBT against overloading. This requires a fibre-optic receiver for receiving the control signal from the controller and a fibre-optic transmitter for the communicating the DESAT status.

To protect the IGBT against damaged fibre-optic connections, the IGBT has to be turned off when the fibre-optic signal is *LOW*. Likewise, when the $V_{ce}$ voltage is normal (i.e. below the DESAT threshold) the DESAT detection circuit should return a *HIGH* optic signal.

## B.6.2 Design

### Power supplies

The IGBT driver board requires +15 V, -15 V, +5 V and -5V. The circuit diagram of the power supplies is shown in Figure B.12. All the IGBT driver boards are powered from a single isolated +5 V supply rail and since the IGBT gates are not driven with respect to the same voltage plane, each driver board requires an isolated DC-to-DC supply. For this reason, the Recom, REC5-0515DRW, DC-to-DC regulator with 4 kV isolation is selected and indicated by $U_1$ on the schematic diagram. The Recom module has a 5 V single rail input and a regulated ±15 V output as shown.

It should be noted that the Recom module selected for the main IGBT driver boards and the sign detector board uses a +5 V input while the other driver boards use a +12 V input. This was done because of a lack of availability of Recom modules with a 12 V input. Ideally, all the driver boards should be powered from the same +12 V source.

To supply +5 V, a linear voltage regulator, LM7805, is directly connected to $+15\text{V}_{iso}$ rail, indicated by $U_2$. Two 1 $\mu$F capacitors, $C_1$ and $C_2$ are placed across the input and output of $U_2$ to provide stability.

The -5 V voltage rail is obtained by using the LM337, adjustable, linear voltage regulator. The output voltage of $U_3$ is set by adjusting the value of $R_1$. From the datasheet, the output voltage ratio is determined by,

$$-V_{out} = -1.25\text{V}\left(1 + \frac{R_2}{R_1}\right) + (-I_{adj} \times R_2) \tag{B.8}$$

where $I_{adj}$ is 65 $\mu$A and $R_2$ is 120 Ω. If $R_1$ is chosen as 390 Ω, the output voltage becomes 5.3 V. According to recommendations in the datasheet, two 1 $\mu$F capacitors, $C_3$ and $C_4$ should be added for stability.

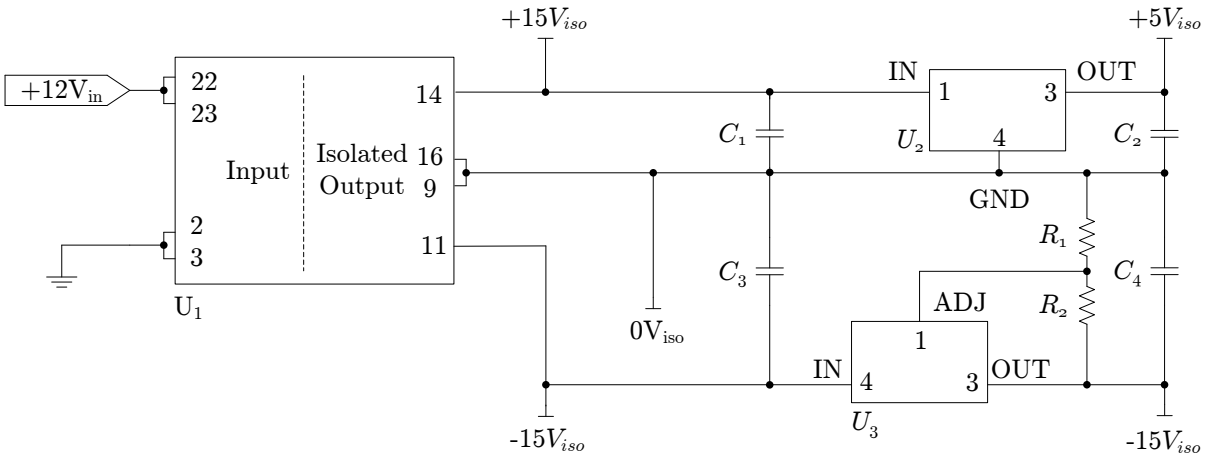



Figure B.12: Schematic diagram of the main IGBT driver power supplies.

Table B.11: Main IGBT driver power supplies component values.

| **Main IGBT Driver Power Supplies** | | |
|---|---|---|
| Designator | Value/Model | Description |
| $R_1$ | 390 Ω | |
| $R_2$ | 120 Ω | |
| $U_1$ | REC5-0515DRW | Isolated DC-DC Regulator |
| $U_2$ | LM7805 | +5V Linear Voltage Regulator |
| $U_3$ | LM337 | Adjustable Negative Regulator |
| $C_1$, $C_2$, $C_3$, $C_4$ | 1 $\mu$F | |

### IGBT driver

The driver circuit for the main IGBTs is similar to the design of the filter cut-out and soft-start drivers, with the exception of an added component for pulling the IGBT gate to a negative voltage to speed up the turn-off time. The circuit diagram of the IGBT driver circuit is shown in Figure B.14.

The driver circuit consists four functional steps. The first step is the fibre-optic receiver, $U_1$, for receiving the control signal. The second step is a general purpose 2N222 NPN transistor, $Q_1$, for driving $U_2$. The third is an HCPL-J312-300E optocoupler, $U_2$, for translating the signal at $5\text{V}_{\text{iso}}$ to $15\text{V}_{\text{iso}}$ and $0\text{V}_{\text{iso}}$ to $-5\text{V}_{\text{iso}}$. The last step is the PBSSx450Z complementary transistor pair, $Q_2$ and $Q_3$, for driving the IGBT gate.

The output of the optic receiver is connected to the internal, 1 kΩ, pull-up resistor pin 4 and the base of $Q_1$. This allows $Q_1$ to be either turned on hard or turned off completely. Resistor $R_1$ acts as a current limiting resistor for driving the optocoupler. If the current is to be limited at 15 mA, $R_1$ can be chosen as 330 Ω.

The *HIGH* signal is translated to 15 V by connecting the $V_{CC}$ pin of the optocoupler to $+15\ \text{V}_{\text{iso}}$ and the *LOW* signal is translated to -5 V by connecting the $V_{EE}$ pin to $-5\ \text{V}_{\text{iso}}$.

Resistor $R_2$ limits the initial current through the base when the complementary pair

changes state. Both transistors have a maximum base current rating of 2 A and a respective base-emitter, emitter-base voltage of 1.3 V. If $R_2$ is chosen as 18 Ω, the peak base current becomes

$$\begin{aligned} I_B &= \frac{15\mathrm{V_{iso}} - (-5\mathrm{V_{iso}}) - \mathrm{V_{BE(sat)}}}{R_2} \\ &= \frac{15\ \mathrm{A} - (-5\ \mathrm{V}) - 1.3\mathrm{A}}{18\ \Omega} \\ &\approx 1\ \mathrm{A} \end{aligned} \tag{B.9}$$

and falls within the device limits.

The IGBT gate resistor $R_3$ limits the rate of charge and discharge of the IGBT gate and consequently determines the speed with which the IGBT is switched. From the IGBT data sheet, the gate resistor can be chosen as 4.5 Ω. Since the gate is constantly switched, it is important to verify the power dissipation within $R_3$. The typical gate charge for a 20 V change in the gate voltage is given in the datasheet as 4000 nC. Since the capacitor is both charged and discharged during each switching period, the total change in charge, d$Q$, becomes 8000 nC. The average gate current is calculated by taking the change of charge over one switching period such that,

$$\begin{aligned} I_G &= \frac{\mathrm{d}Q}{\mathrm{d}T} \\ &= \frac{8000\ \mathrm{nC}}{100\ \mu\mathrm{s}} \\ &= 80\ \mathrm{mA}. \end{aligned} \tag{B.10}$$

The power dissipated in $R_3$ as a result of $I_G$ then becomes 28.8 mW. However, the gate is charged and discharged with pulses that have large peaks and the resistor should be able to handle such peaks. The peak gate resistor power therefore becomes

$$\begin{aligned} P_RG &= \frac{\left(V_{G(on)} - V_{G(off)}\right)^2}{R_G} \\ &= \frac{(20\ \mathrm{V})^2}{4.5\ \Omega} \\ &= 89\ \mathrm{W}. \end{aligned} \tag{B.11}$$

Typically, the resistor manufacturer provides a graph indicating the *continuous pulse load* versus *pulse duration*, as shown in the example Figure B.13. If the pulse duration is taken as the sum of the turn-on time, $T_{d(on)}$, and turn-off time, $t_{d(off)}$, the correct resistor can be selected. To minimise parasitic inductance when turning the IGBTs on, capacitor $C_1$ is chosen as ≈ 20 $\mu$F and placed close the the collector of $Q_2$. The IGBT gate has a maximum allowed gate voltage of ±20 V. To protect the gates against overvoltage conditions, 18 V Zener diodes $D_1$ and $D_2$ are placed appropriately between each gate and emitter. Lastly, a 10 kΩ resistor, $R_4$, is placed between the IGBT gate and emitter to pull the gate to zero when power to the driver board is lost.

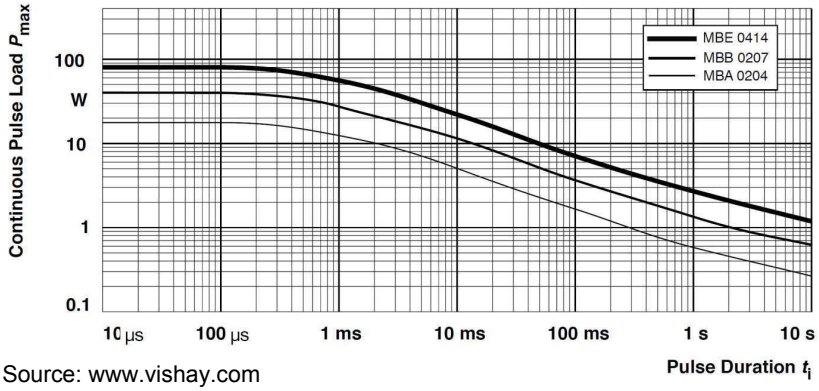



Figure B.13: Example graph of the *continuous pulse load* versus *pulse duration* for a linear film resistor from Vishay.

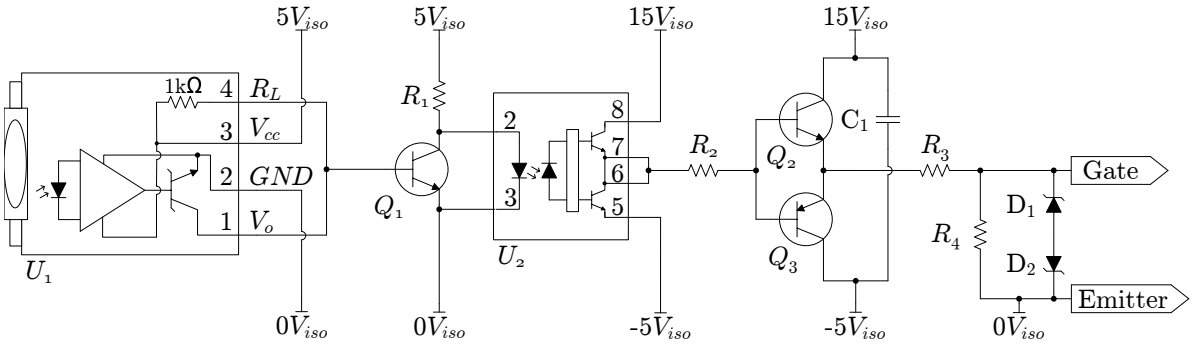



Figure B.14: Schematic diagram of the main IGBT driver.

Table B.12: Main IGBT driver circuit component values.

| **Main IGBT Driver Circuit** | | |
|---|---|---|
| Designator | Value/Model | Description |
| $R_1$ | 330 Ω | |
| $R_2$ | 18 Ω | |
| $R_3$ | 4.5 Ω | High Pulse Power Withstand |
| $R_4$ | 10 kΩ | |
| $C_1$ | $\approx 20\mu$F | |
| $U_1$ | HFBR-2521 | Fibre-Optic Receiver |
| $U_2$ | HCPL-J312-300E | Optocoupler |
| $D_1$, $D_2$ | BZV55-C18 | 18 V Zener Diode |
| $Q_1$ | MMBT2222A | General Purpose NPN Transistor |
| $Q_2$ | PBSS4540Z | 40 V low VCEsat NPN transistor |
| $Q_3$ | PBSS5540Z | 40 V low VCEsat PNP transistor |

**DESAT-detection circuit**

When the IGBT is overloaded, the large collector current forces the IGBT out of saturation and the $V_{ce}$ voltage begins to increase from $V_{ce(sat)}$. This is dangerous since the losses in the IGBT greatly increases with a rise in $V_{ce}$ and could damage the device. The DESAT-detection circuit measures the $V_{ce}$ voltage and triggers a signal when the voltage exceeds a certain threshold. The circuit diagram for implementing DESAT detection is shown in Figure B.15.

The $V_{ce}$ voltage is measured between the IGBT collector and emitter as shown. Diode $D_1$ is used as a blocking diode when the IGBT is turned off and the blocking voltage is high. The maximum voltage across the IGBTs, before the protection kicks in, is 1200 V. The STTH112 diode from ST Micro Electronics is chosen for $D_1$ since it has a repetitive peak reverse blocking voltage of 1200 V and a current rating of 1 A.

Resistor $R_1$ and capacitor $C_1$ is a low pass $RC$ filter for suppressing noise and false triggers. The cut-off frequency for a low pass $RC$ circuit is given by

$$f_c = \frac{1}{2\pi R_1 C_1}. \tag{B.12}$$

For a cut-off frequency in the order of 30 kHz, $R_1$ can be chosen as 100 Ω and $C_1$ as 50 nF. Substituting the values into Equation B.12, the cut-off frequency becomes 31.8 kHz. T

When the IGBT is turned on, $V_{ce}$ is in saturation and $D_1$ is forward biased. To allow $D_1$ to turn on, resistor $R_2$ is used as a current limiting resistor. To ensure $D_1$ turns on, the value for $R_2$ can be chosen as 1 kΩ. Taking the worst case voltage drop across $R_2$ as 14.3 V, the losses in $R_2$ remains below 250 mW. However, if a resistor with a lower power rating is preferred, $R_2$ may also be chosen as 10 kΩ.

When the IGBT is turned off, $D_1$ is reverse biased and $R_2$ acts as a pull-up resistor. Although there should be no voltage drop across $R_2$ when $D_1$ is reverse biased, transient effects could cause a substantial voltage drop when the IGBT collector is pulled high. To clamp the voltage across $R_2$, a Schottky diode, $D_2$ is placed in parallel with the resistor. The LS103B small signal Schottky diode from Vishay is chosen. It has a reverse blocking voltage of 30 V and a maximum forward voltage drop of 370 mV.

The DESAT detection threshold is determined by the two voltage divider resistors, $R_3$ and $R_4$. The DESAT threshold voltage across the collector and emitter, $V_{ce(thres)}$, is chosen as approximately 7 V. The voltage, $V_{in(-)}$, at the negative input pin of $U_1$ is given by

$$\begin{aligned} V_{in(-)} &= V_{ce(thres)} + V_F + V_{R1} \\ &= V_{ce(thres)} + V_F + \left(15V_{iso} - V_F - V_{ce(tresh)}\right)\frac{R_1}{R_1 + R_2} \\ &= 7\text{ V} + 1\text{ V} + (15\text{ V} - 1\text{ V} - 7\text{ V})\frac{100\ \Omega}{100\ \Omega + 1\ \text{k}\Omega} \\ &= 8.6\text{ V} \end{aligned} \tag{B.13}$$

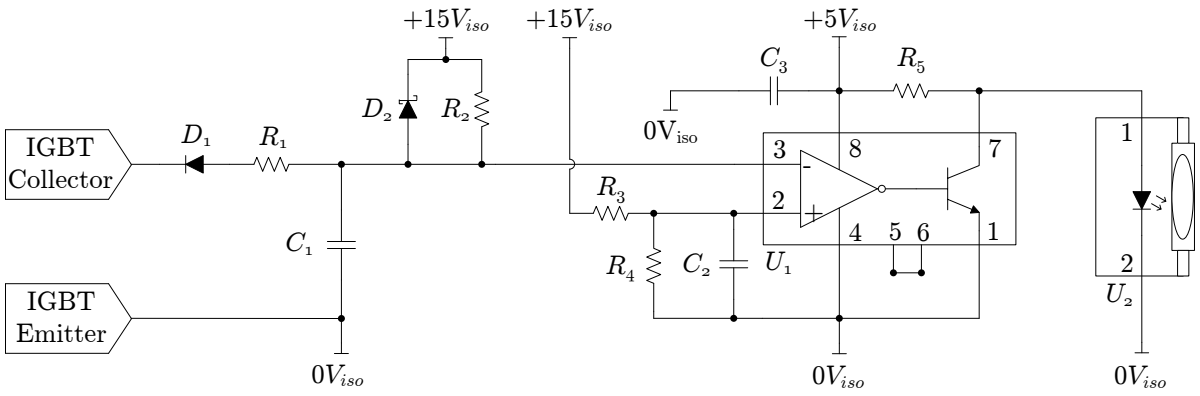



Figure B.15: Schematic diagram of the main IGBT DESAT-status feedback.

Table B.13: Main IGBT DESAT-status feedback circuit component values.

| **Main IGBT DESAT-Status Feedback** | | |
|---|---|---|
| Designator | Value/Model | Description |
| $R_1$ | 100 Ω | |
| $R_2$ | 1 kΩ | |
| $R_3$ | 10 kΩ | |
| $R_4$ | 12 kΩ | |
| $R_5$ | 55 Ω | |
| $C_1$ | 50 nF | |
| $C_2$ | 100 nF | |
| $C_3$ | 4.7 $\mu$F | |
| $D_1$ | STTH112U | High voltage ultrafast rectifier |
| $D_2$ | LS103B | Small Signal Schottky Diode |
| $U_1$ | LM311D | Differential Comparator |
| $U_2$ | HFBR1521 | Fibre-Optic Transmitter |

where $V_F$ is the maximum forward voltage across $D_1$.

By choosing the voltage divider resistors, $R_3$ as 10 kΩ and $R_4$ as 12 kΩ, the threshold reference voltage at $V_{in(+)}$ of the comparator becomes 8.1 V. To suppress noise on the threshold reference, a 100 nF capacitor, $C_2$, is placed across $R_4$.

The typical forward input current, $I_{Fdc}$, of the optic transmitter, $U_2$, is given in the data sheet as 60 mA with a forward voltage, $V_f$, of 1.67 V . The forward current is limited by resistor $R_5$. If the forward voltage is taken as 1.67 V, the voltage across the $R_5$ becomes 3.33 V. Using Ohm's law, the required resistance for limiting the current to 60 mA is 55.5 Ω. To speed up the turn-on time of $U_2$, a 4.7 $\mu$F capacitor, $C_3$, is placed close to $R_5$ to minimise the effects of parasitic inductance in the voltage supply rail.

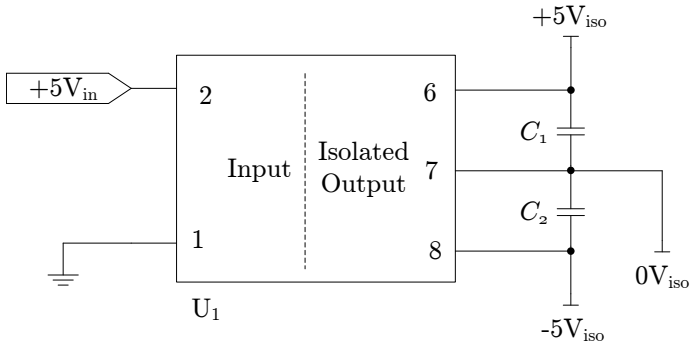



Figure B.16: Schematic diagram of the power supply for the sign detector board.

Table B.14: Sign detector power supplies component values.

| Sign Detector Power Supplies | | |
|---|---|---|
| Designator | Value/Model | Description |
| $C_1$, $C_2$ | 4.7 $\mu$F | |
| $U_1$ | RS3-0505D | Isolated DC-DC Regulator |

# B.7 Sign Detector Design

## B.7.1 Description and Requirements

The purpose of the sign detector board is to accurately indicate the sign of the bus voltage of the AC-to-AC converter. This function is essential for applying the correct commutation scheme when switching the main IGBTs.

When the bus voltage is negative the board should send a *HIGH* optic signal and when the bus voltage is positive, a *LOW* signal.

## B.7.2 Design

### Power Supply

The sign detector board requires a +5 V and -5 V voltage rail. The Recom, RS3-0505D, single-to-dual isolated DC-to-DC converter module with 3 kV isolation is selected for this purpose. The module converts a single +5 V input to a regulated dual ±5 V voltage rail and requires no additional support circuits. However, to increase stability, two 4.7 $\mu$F capacitors are placed across each voltage rail. A circuit diagram of the power supply is given in Figure B.16.

### Sign Detector

The sign detector circuit consists of a clamped voltage divider and a comparator, set up with hysteresis as shown in Figure B.17. Resistors $R_1$ and $R_2$ form the voltage divider circuit with two Zener diodes clamping the voltage across $R_2$. The value of $R_2$ is chosen

larger than the value of $R_1$ to allow the Zener diodes, $D_1$ and $D_2$, to clamp closer to the voltage zero-crossing. When the diodes start clamping, $R_1$ acts as limiting resistor for the current through the diodes.

In the initial design, the value of $R_1$ was chosen as 15 kΩ, the value of $R_2$ as 560 kΩ and the BZV55-2V7 Zener diodes for $D_1$ and $D_2$. The forward voltage across the Zener diode is 0.9 V and the reverse Zener voltage is 2.7 V.

If the total voltage drop across the clamping diodes is taken as 3.6 V and the maximum RMS bus voltage as 698 V, the total power dissipation in $R_1$ becomes

$$\begin{aligned} P_{R1} &= \frac{(V_{bus} - V_{clamp})^2}{R_1} \\ &= \frac{(698\text{ V} - 3.6\text{ V})^2}{150\text{ k}\Omega} \\ &= 32\text{ W}. \end{aligned} \tag{B.14}$$

Resistor $R_1$ should be chosen with a voltage rating that can withstand the maximum bus voltage of 1200 V under fault conditions.

As a design note, the power dissipation in $R_1$ can be greatly reduced without affecting the functioning of the voltage divider and clamp. As an alternative, the value of $R_1$ can be chosen as 150 kΩ and the value of $R_2$ as 560 kΩ while using the same BZV55-2V7 Zener diodes. Using these values, the power dissipated in $R_1$ becomes,

$$\begin{aligned} P_{R1} &= \frac{(V_{bus} - V_{clamp})^2}{R_1} \\ &= \frac{(698\text{ V} - 3.6\text{ V})^2}{150\text{ k}\Omega} \\ &= 3.2\text{ W}. \end{aligned} \tag{B.15}$$

The LM311D differential comparator is selected for $U_1$. To avoid chatter around the comparator threshold, hysteresis is added by means of $R_3$ and $R_4$. The threshold voltage of the comparator is determined by the state of the comparator output, $V_{comp}$ such that

$$V_{thres} = V_{comp} \times \frac{R_3}{R_3 + R_4}. \tag{B.16}$$

When $V_{comp}$ is *HIGH*, the voltage is equal to the forward voltage across the optic transmitter $U_2$, which 1.67 V. When $V_{comp}$ is *LOW*, the voltage is equal to the low-level output voltage of $U_1$, which is 0.75 V.

If $R_3$ is chosen as 15 kΩ and $R_4$ as 68 kΩ, the threshold voltage becomes 0.3 V when $V_{comp}$ is *HIGH* and 0.1 V when $V_{comp}$ is *LOW*. This leaves a hysteresis band of 0.2 V, which is sufficient for eliminating chatter. However, a further 1 nF capacitor, $C_2$, is placed between the differential input pins of $U_1$ to suppress noise caused by the switching IGBTs.

The LM311D data sheet suggests placing a 1 MΩ resistor, $R_6$, between pin 2 and 4 for improved stability.

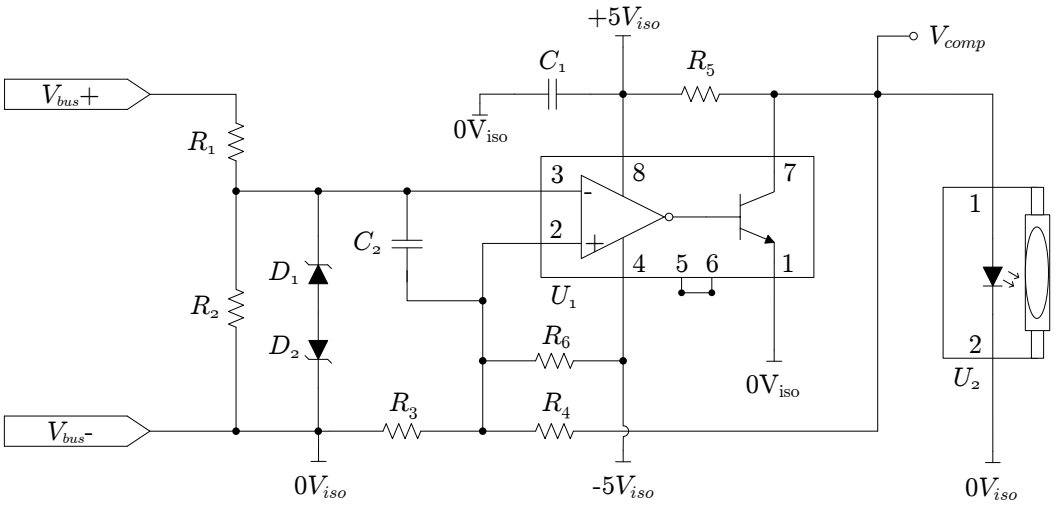



Figure B.17: Schematic diagram of the sign detector circuit.

Table B.15: Sign detector circuit component values.

| **Sign Detector Circuit** | | |
|---|---|---|
| Designator | Value/Model | Description |
| $R_1$ | 150 kΩ | |
| $R_2$ | 560 kΩ | |
| $R_3$ | 15 kΩ | |
| $R_4$ | 68 kΩ | |
| $R_5$ | 55Ω | |
| $R_6$ | 1 MΩ | |
| $C_1$ | 4.7 $\mu$F | |
| $C_2$ | 100 nF | |
| $D_1$, $D_2$ | BZV55-2V7 | 2.7 V Zener Diode |
| $U_1$ | LM311D | Differential Comparator |
| $U_2$ | HFBR1521 | Fibre-Optic Transmitter |

To limit the current through the fibre-optic transmitter to 60 mA, $R_5$ is chosen as 55 Ω. Lastly, a 4.7 $\mu$F capacitor, $C_1$, is placed close to $R_5$ for supply rail stability.

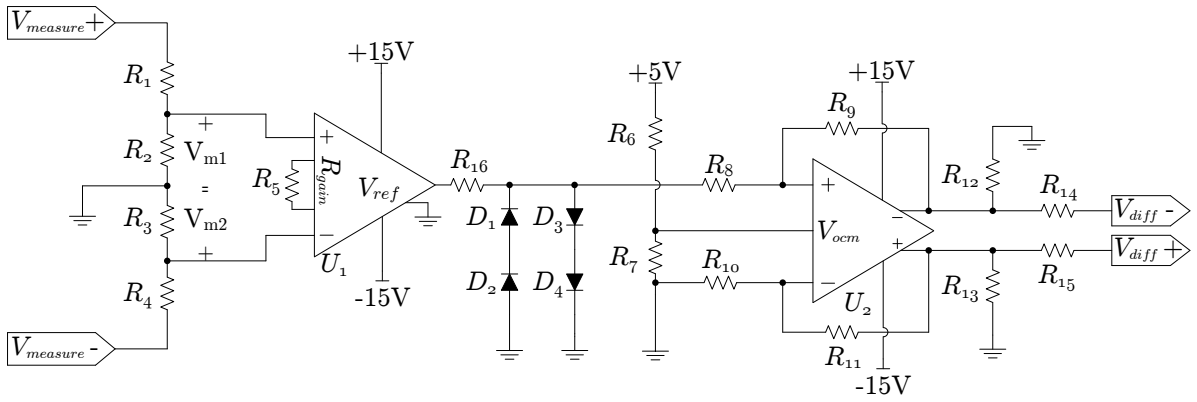



Figure B.18: Schematic diagram of the low voltage measurement board using differential voltage measurements.

# B.8 Low Voltage Measurements

## B.8.1 Description and Requirements

This section discusses the design of the low voltage measurement boards for measuring the voltages on the AC-to-AC converters. The voltage measurements are taken by using differential voltage measurements across voltage divider resistors. The maximum voltage on each converter module is limited by the protection mechanisms to 1200 V. However, the maximum differential measurements under normal operation can be limited to 1000 V.

One main controller is used to control both modules and all the measurements are taken with respect to the ground plane of the main controller. This requires a common mode voltage rating of at least 2400 V.

The measurement board connects directly to the main controller by means of a differential signal pair. Futhermore, no power supplies are required as the main controller supplies the measurement board directly with 5 V, +15 V and -15 V.

## B.8.2 Design

The circuit diagram of the measurement circuit is shown in Figure B.18. The voltage is measured between terminals, $V_{measure+}$ and $V_{measure-}$, using the voltage divider resistors, $R_1$, $R_2$, $R_3$ and $R_4$.

In order to limit measurement noise, a differential instrumentation amplifier with a high common mode rejection rate is chosen for $U_1$. The differential voltage is defined in [95] as

$$V_d = V_{m1} - V_{m2} \tag{B.17}$$

and the common mode voltage as

$$V_{cm} = \frac{V_{m1} + V_{m2}}{2} \tag{B.18}$$

Table B.16: Low voltage measurement circuit component values.

| **Low Voltage Measurement Circuit** | | |
|---|---|---|
| Designator | Value/Model | Description |
| $R_1$, $R_4$ | 2 MΩ | |
| $R_2$, $R_3$ | 2 kΩ | |
| $R_5$ | $\infty$ | Leave open |
| $R_6$, $R_7$, $R_8$, $R_9$, $R_{10}$, $R_{11}$, $R_{12}$, $R_{13}$ | 10 kΩ | |
| $R_{14}$, $R_{15}$, $R_{16}$ | 27Ω | |
| $D_1$, $D_2$, $D_3$, $D_4$ | 1N148W-V-GS08 | Small singnal Fast swithing diode |
| $U_1$ | INA129U | Instrumentation Amplifier |
| $U_2$ | THS4521 | Fully Differential Amplifier |

When the same noise is present on both measurements, $V_{m1}$ and $V_{m2}$, the differential voltage becomes zero. When

$$V_{m1} = \frac{V_{measure}}{2} \tag{B.19}$$

and

$$V_{m2} = \frac{-V_{measure}}{2} \tag{B.20}$$

the differential voltage becomes

$$V_d = V_{measure}. \tag{B.21}$$

The measured voltages can therefore be written as

$$V_{m1} = \left(\frac{R_2}{R_1 + R_2}\right) \cdot \frac{V_{measure}}{2} \tag{B.22}$$

and

$$V_{m2} = \left(\frac{R_3}{R_4 + R_3}\right) \cdot \frac{-V_{measure}}{2}. \tag{B.23}$$

If $R_1$ is equal to $R_4$, $R_2$ is equal to $R_3$ and B.22 and B.23 is substituted into B.17, $V_d$ becomes

$$\begin{aligned} V_d &= \left(\frac{R_2}{R_1 + R_2}\right) V_{measure} \\ &= \left(\frac{R_3}{R_4 + R_3}\right) V_{measure}. \end{aligned} \tag{B.24}$$

The value of $V_d$ becomes a scaled version of $V_{measured}$ with a ratio dependant on the values of $R_1$, $R_2$, $R_3$ and $R_4$. The ADC on the controller board can only handle a maximum differential voltage of 1 V. Choosing $R_1 = R_4 = 2M\Omega$ and $R_2 = R_3 = 2k\Omega$ with a maximum measured voltage of 1000V, the output of the differential amplifier becomes

$$V_d(max) = 1\text{V}$$

In order to adjust the range of the ADC, an instrumentation amplifier is used with an adjustable gain. It is desirable that the instrumentation amplifier has a good CMRR to

eliminate noise from the environment and an easy way of adjusting the differential gain. The INA129 from Texas Instruments is used for $U_1$ because it has a wide supply range, an excellent CMRR of 120dB and its input is protected from overvoltage spikes. The gain can be adjusted with resistor $R_5$, which is defined in the data sheet as $R_G$ such that

$$G = 1 + \frac{49.4k\Omega}{R_G}. \tag{B.25}$$

The 1 $V_{peak}$ measurement is sufficient and no gain adjustment is needed. Therefore, by leaving $R_5$ open, the gain can be taken as unity.

To protect the ADC against overvoltage conditions, diodes $D_1$, $D_2$, $D_3$ and $D_4$ are added. When the voltage exceeds 1.4 V, the diodes turns on and clamps the voltage. To protect the output port of $U_1$, a current limiting resistor, $R_{16}$, is placed in series between $U_1$ and the clamping diodes. The value of $R_{16}$ can be taken as 27 Ω.

A fully differential amplifier, $U_2$, is used as a line driver to send the measured signal as a differential pair to the main controller board. The THS4521 amplifier from Texas Instruments is selected. The amplifier can be set up with unity gain by choosing, $R_8$, $R_9$, $R_{10}$ and $R_{11}$ to be equal to 10 kΩ. Additionally, $R_{12}$ and $R_{13}$ is placed as small loading resistors and can also be chosen as 10 kΩ. The cable between the measurement and controller board introduces capacitance and inductance to the line. To suppress possible oscillation between the amplifier and the line, two 27 Ω resistors, $R_{14}$ and $R_{15}$ is placed in series with the differential line outputs. To allow positive and negative swing, both $U_1$ and $U_2$ are power by the ±15 V rails. Resistors $R_6$ and $R_7$ are used as a voltage divider circuit to provide a 2.5 V common mode offset for $U_2$.

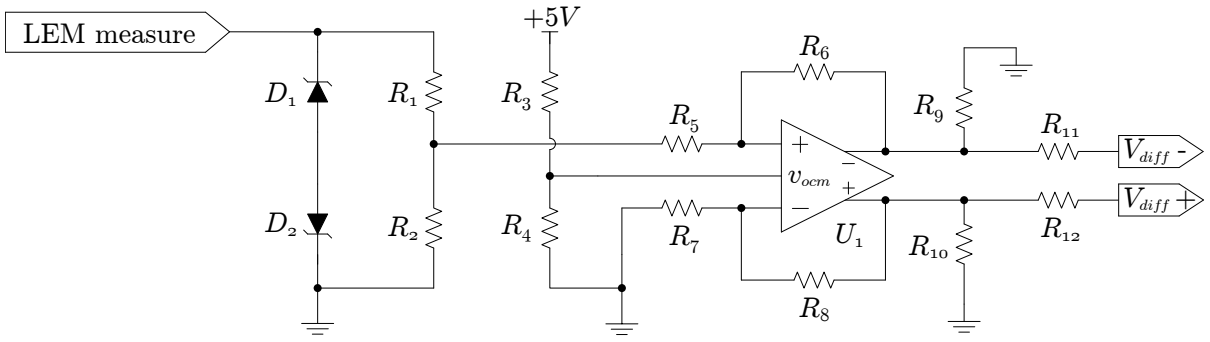



Figure B.19: Schematic diagram of the medium voltage measurement board using a LEM module.

Table B.17: Medium voltage measurement circuit component values.

| **Medium Voltage Measurement Circuit** | | |
|---|---|---|
| Designator | Value/Model | Description |
| $R_1$ | 32.5Ω | |
| $R_2$ | 14.1Ω | |
| $R_3$, $R_4$, $R_5$, $R_6$, $R_7$, $R_8$, $R_9$, $R_{10}$ | 10 kΩ | |
| $R_{11}$, $R_{12}$ | 27Ω | |
| $D_1$, $D_2$ | BZV55-C3V3 | 3.3 V Zener Diode |
| $U_1$ | THS4521 | Fully Differential Amplifier |

# B.9 Medium Voltage Measurements

## B.9.1 Description and Requirements

This section discusses the design of the medium voltage measurement boards for measuring the 12.75 kV distribution feeder voltage. The voltage measurements are taken using the LEM LV100-4000/SP12 voltage transducer. The output port delivers a current that is proportional to the measured voltage and provides Galvanic isolation from the measured voltage. To translate the current, a measurement circuit is needed to convert the current into an appropriate differential voltage that can be sent to the controller board.

## B.9.2 Design

The LEM LV100-4000/SP12 module is configured for a nominal voltage of 4 $kV_{rms}$. However, higher voltages can be measured by adding series resistors to the primary measuring side. The LEM module has a 1.6 $M\Omega$ internal series resistor with a hall effect sensor, used to measure the current through the resistor. The measured current is translated to a current at the output pin, linearly proportional to the current through the series input resistor.

For the nominal voltage of 4 $kV_{rms}$, the primary nominal RMS current, $I_{pn}$, is 2.5 mA. If the measuring voltage is increased, the measuring resistance must be increased to allow

2.5 mA when the desired nominal voltage is applied. To allow for a 10 % deviation in the 12.75 kV line, the measured nominal voltage can be taken as 14 kV. The additional external measurement resistance, $R_{PM}$, to be added in series with the primary input terminals of the LEM module then becomes

$$\begin{aligned} R_{\text{PM}} &= \frac{V_{\text{nom(rms)}}}{I_{\text{PN(rms)}}} - R_{\text{internal}} \\ &= \frac{14\ \text{kV}}{2.5\ \text{mA}} - 1.6\ \text{M}\Omega \\ &= 4\ \text{M}\Omega. \end{aligned} \tag{B.26}$$

Using voltage division, the power dissipated in $R_{\text{PM}}$ becomes

$$\begin{aligned} P_{Rpm} &= V_{Rpm}^2 \cdot \frac{1}{R_{\text{PM}}} \\ &= \left( \frac{V_{\text{nom(rms)}} R_{\text{PM}}}{R_{\text{PM}} + R_{\text{internal}}} \right)^2 \cdot \frac{1}{R_{\text{PM}}} \\ &= \left( \frac{14\ \text{kV} \times 4\ \text{M}\Omega}{4\ \text{M}\Omega + 1.6\ \text{M}\Omega} \right)^2 \cdot \frac{1}{4\ \text{M}\Omega} \\ &= 25\ \text{W}. \end{aligned} \tag{B.27}$$

The output of the LEM module delivers a current proportional to the input voltage. At the nominal voltage the output current, $I_{\text{M}}$, is given as 50 $\text{mA}_{\text{rms}}$ at an offset of 0 mA. This results in a peak current of 70.7 mA.

The circuit diagram of the measurement circuit is shown in Figure B.19. Two resistors, $R_1$ and $R_2$, are connected in series with the LEM output port and a measurement is taken across $R_2$. The peak voltage across $R_2$ should be 1 V when the LEM output current, $I_{\text{SN}}$, is 70.7 mA. Using Ohm's law, the required resistance for $R_2$ becomes 14.1 Ω. To protect the measurement circuit against overvoltage conditions, two 3.3 V Zener diodes, $D_1$ and $D_2$, are connected to the LEM output pin as shown. When the peak voltage of 1 V is measured across $R_2$, the voltage across both $R_1$ and $R_2$ should clamp at 3.3 V. The value for $R_1$ is therefore calculated as

$$\begin{aligned} R_1 &= \frac{V_{clamp}}{I_{\text{M}}} - R_2 \\ &= \frac{3.3\ V}{70.7\ mA} - 14.1\ \Omega \\ &= 32.5\ \Omega \end{aligned} \tag{B.28}$$

A fully differential amplifier, $U_1$, is used as a line driver to send the measured signal as a differential pair to the main controller board. The THS4521 amplifier from Texas Instruments is selected. The amplifier can be set up with unity gain by choosing, $R_5$, $R_6$, $R_7$ and $R_8$ to be equal to 10 kΩ. Additionally, $R_9$ and $R_{10}$ is placed as loading resistors and can also be chosen as 10 kΩ. The cable between the measurement and controller

board introduces capacitance and inductance to the line. To suppress possible oscillation between the amplifier and the line, two 27 Ω resistors, $R_{11}$ and $R_{12}$ is placed in series with the differential line outputs. To allow positive and negative swing, both $U_1$ and the LEM module is power by the ±15 V rails. Resistors $R_3$ and $R_4$ are used as a voltage divider circuit to provide a 2.5 V common mode offset for $U_1$.

Table B.18: Current measurement circuit component values.

| **Current Measurement Circuit** | | |
|---|---|---|
| Designator | Value/Model | Description |
| $R_1$ | 5.9Ω | |
| $R_2$ | 13.5Ω | |
| $R_3$, $R_4$, $R_5$, $R_6$, $R_7$, $R_8$, $R_9$, $R_{10}$ | 10 kΩ | |
| $R_{11}$, $R_{12}$ | 27Ω | |
| $D_1$, $D_2$ | BZV55-C3V3 | 3.3 V Zener Diode |
| $U_1$ | THS4521 | Fully Differential Amplifier |

## B.10 Current Measurements

### B.10.1 Description and Requirements

The current measurements are done using the LEM LA305-S current transducer. The measurement of the current transducer works on the same principle as the LEM voltage transducer and the same measurement circuit, given in Figure B.19, can be used. The only differences between the LEM voltage transducer and current transducer measurement boards are the values for resistors $R_1$ and $R_2$.

### B.10.2 Design

The nominal RMS output current of the LEM current transducer is 120 mA. This results in a peak nominal current, $I_{\text{SN}}$, of 170 mA. If the peak measured voltage across $R_2$ is taken as 1 V, using Ohm's law, the value for $R_2$ becomes,

$$\begin{aligned} R_2 &= \frac{V_{R2}}{I_{\text{SN}}} \\ &= \frac{1\text{ V}}{170\text{ mA}} \\ &= 5.9\ \Omega. \end{aligned} \tag{B.29}$$

Taking the voltage across both $R_1$ and $R_2$ as 3.3 V, the value for $R_1$ becomes

$$\begin{aligned} R_1 &= \frac{V_{clamp}}{I_{\text{M}}} - R_2 \\ &= \frac{3.3\ V}{170\ mA} - 5.9\ \Omega \\ &= 13.5\ \Omega. \end{aligned} \tag{B.30}$$

The remaining component values remain the same as calculated in the design of the voltage transducer board in Section B.9. A complete list of the component values are given in Table B.18.

# Appendix C

# Model Derivations

## C.1 Model Derivation of Two Cascaded AC-to-AC Converter Modules

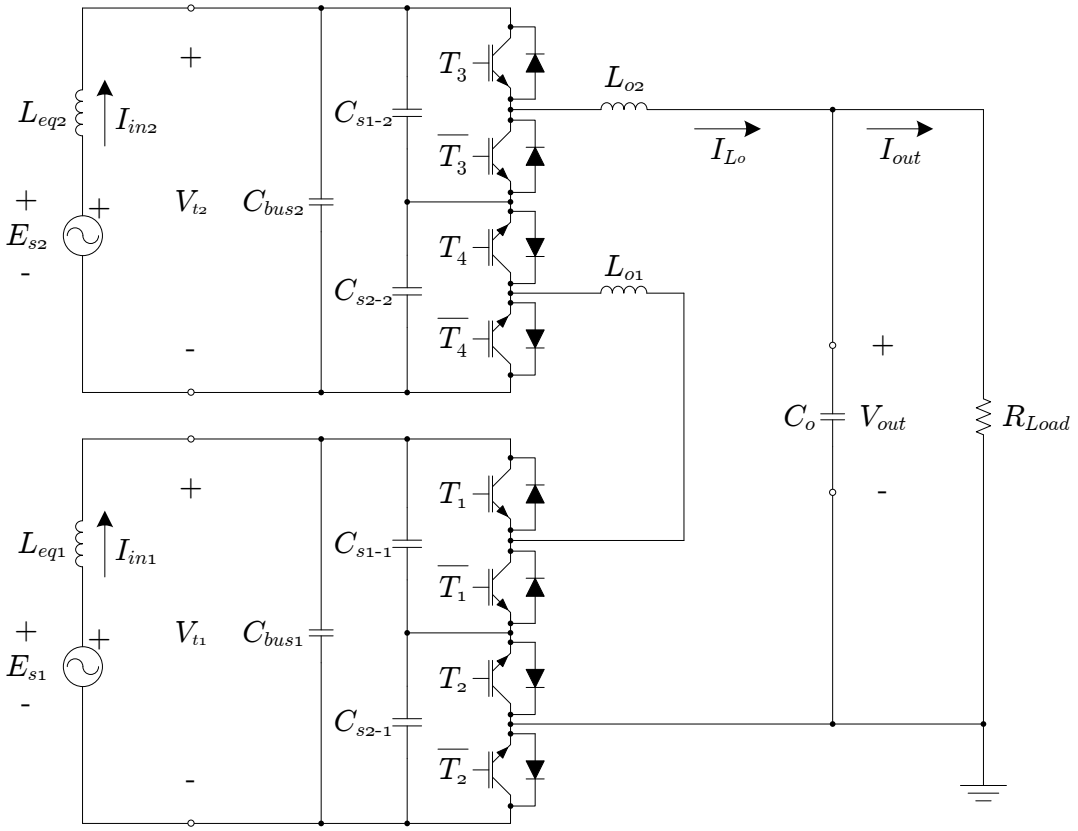



Figure C.1: Schematic diagram with the topology of two cascaded AC-to-AC converters.

This section presents the detailed derivation of the discrete state-space models that describe the switching states of two cascaded AC-to-AC converter modules, shown in Figure C.1. In Chapter 4.4, the control of two cascaded converters is evaluated numerically by simulating the response of the converter to the controller. The simulation requires a

model of the converter that includes a known load resistance. In the first part of this section the model of the actual plant, used to simulate the converter, is derived.

To account for dynamic loads, the control algorithm requires a model of the converter that is independent of the load impedance. In the second part of this section, the state-space models for the predictive control algorithm is derived without the load impedance by assuming that the load is an unknown current source.

In Appendix A, it was shown that each AC-to-AC converter module has four possible switching states: an *on-state* and *off-state* for a positive input voltage and an *on-state* and *off-state* for a negative input voltage. The number of possible switching states are given by $2^s$, where $s$ is the number of unique switching pairs. If two converter modules are switched together, this results in a 16 unique switching states. However, each converter module are symmetrical for both positive and negative voltages. If it is assumed that the input voltages, $e_{s1}$ and $e_{s2}$, are always in phase, the number of unique switching pairs can be reduced to two. This reduces the number of unique switching states to four.

### C.1.1 Derivation of the Simulation Model with a Known Load

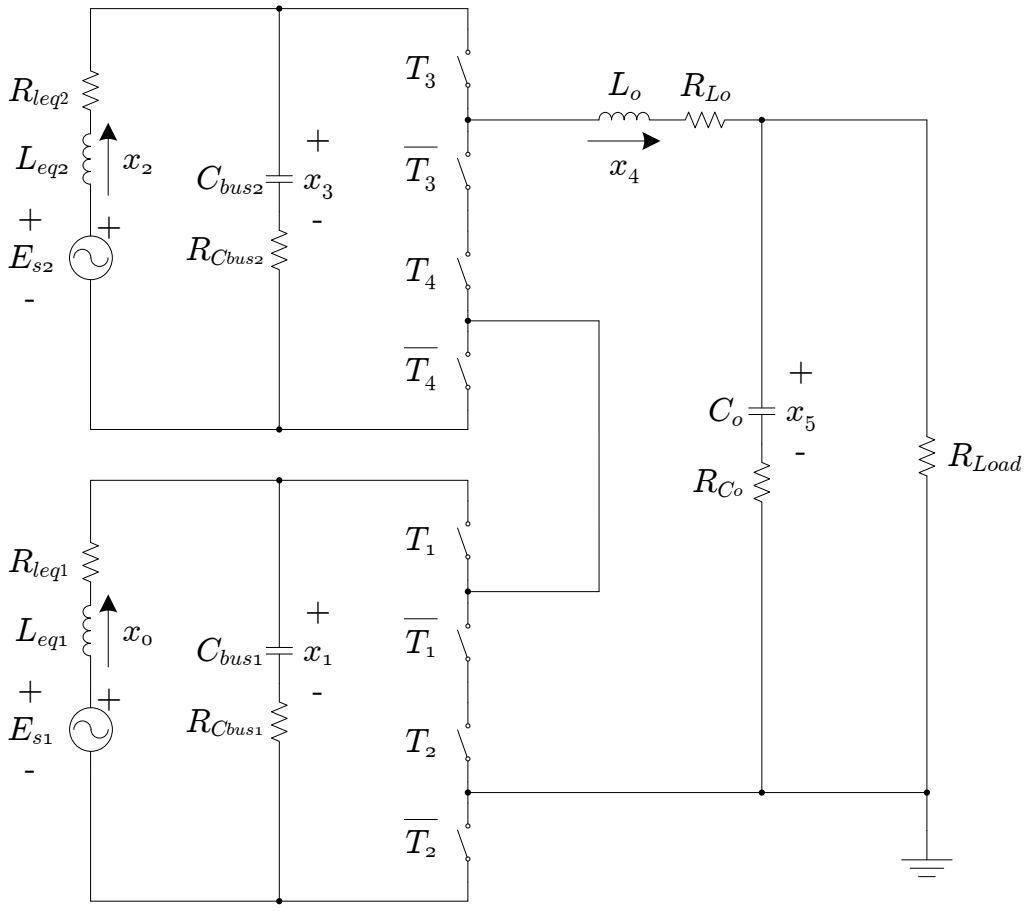



Figure C.2: Equivalent circuit diagram of two cascaded AC-to-AC converters with a known load.

This section presents the derivation of the four unique state-space models that describe the switching states of two cascaded AC-to-AC converter modules. The equivalent circuit diagram of the cascaded converter is given in Figure C.2. The two inductors, $L_{o\_1}$ and $L_{o\_2}$ are in series and can be combined into one equivalent filter inductor $L_o$. The equivalent series resistances (ESR) are also included for the capacitors and inductors. The state vector, $\mathbf{x}(t)$, can therefore be defined as

$$\begin{aligned}\mathbf{x}(t) &= \begin{bmatrix} i_{in\_1}(t) & v_{t\_1}(t) & i_{in\_2}(t) & v_{t\_2}(t) & i_{L_o}(t) & v_{out}(t) \end{bmatrix}^\top \\ &= \begin{bmatrix} x_0(t) & x_1(t) & x_2(t) & x_3(t) & x_4(t) & x_5(t) \end{bmatrix}^\top .\end{aligned} \tag{C.1}$$

The state vector has six unique state variables and in order to find the state-space matrices, six unique differential equations are required for each switching state. These equations can be found by taking Kirchoff's voltage and current laws and applying them to all the voltage loops and nodes. The dynamic behaviour for the current through a capacitor is described by

$$i_C(t) = C\frac{\mathrm{d}v}{\mathrm{d}t} \tag{C.2}$$

and the dynamic behaviour for the voltage across an inductor by

$$v_L(t) = L\frac{\mathrm{d}i}{\mathrm{d}t}. \tag{C.3}$$

In a real system it is not always practical to measure all the state variables. If a state observer is used, the measured output vector, $\mathbf{y}(t)$, can be defined as

$$\begin{aligned}\mathbf{y}(t) &= \begin{bmatrix} i_{in\_1}(t) & i_{in\_2}(t) & i_{L_o}(t) & v_{out}(t) \end{bmatrix}^\top \\ &= \begin{bmatrix} x_0(t) & x_1(t) & x_4(t) & x_5(t) \end{bmatrix}^\top .\end{aligned} \tag{C.4}$$

Since the output vector is calculated by [61]

$$\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) + \mathbf{D}\mathbf{u}(t), \tag{C.5}$$

and remains the same for every switching state, the $\mathbf{C}$ and $\mathbf{D}$ matrices remains the same for all the switching states.

The $\mathbf{C}$ matrices therefore becomes

$$\mathbf{C}_S = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{C.6}$$

and the **D** matrices

$$\mathbf{D}_S = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}. \tag{C.7}$$

The **A** and **B** matrices for each switching state is derived in the follows section by using the six unique differential equations that describe each switching state and solving the equations simultaneously such that

$$\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \tag{C.8}$$

holds true, where $\mathbf{u}(t)$ is

$$\mathbf{u}(t) = \begin{bmatrix} e_{s\_1}(t) \\ e_{s\_2}(t) \end{bmatrix}. \tag{C.9}$$

The cascaded converter can be viewed as a multiple-input, multiple-output (MIMO) system. From the schematic diagram it is evident that the two inputs, $e_{s1}$ and $e_{s2}$, are always connected to the equivalent input inductance and bus capacitor. As a result the input state matrix, **B**, will be the same for all the switching states. Solving **B** according to differential equations, as discussed in the following sections, the input state matrix becomes

$$\mathbf{B}_S = \begin{bmatrix} \frac{1}{L_{eq1}} & 0 \\ 0 & 0 \\ 0 & \frac{1}{L_{eq2}} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}. \tag{C.10}$$

## Switching State 0

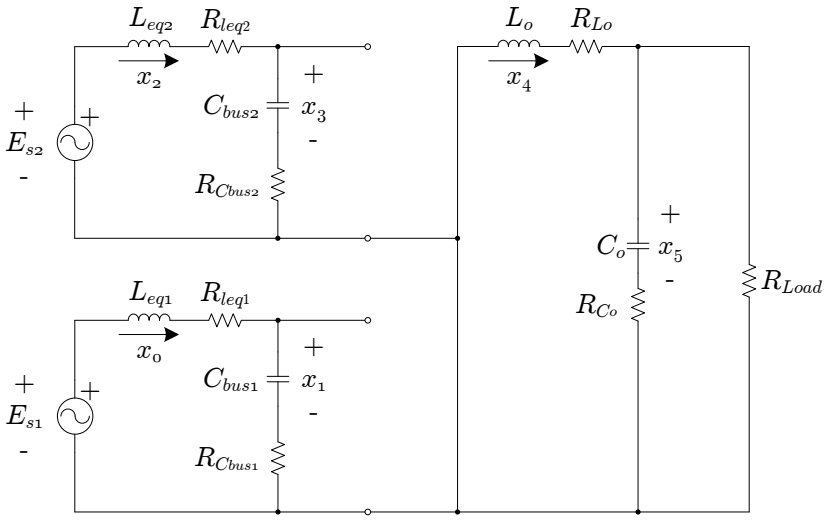



Figure C.3: Schematic circuit diagram of switching state 0, when both converter modules are in the *off-state*.

The six unique differential equations that describe this switching state is

$$0 = R_{L_{eq1}} x_0 + L_{eq1}\dot{x}_0 + x_1 + R_{C_{bus1}} C_{bus1}\dot{x}_1 - e_{s1} \tag{C.11}$$

$$0 = C_{bus1}\dot{x}_1 - x_0 \tag{C.12}$$

$$0 = R_{L_{eq2}} x_2 + L_{eq2}\dot{x}_2 + x_3 + R_{C_{bus2}} C_{bus2}\dot{x}_3 - e_{s2} \tag{C.13}$$

$$0 = C_{bus2}\dot{x}_3 - x_2 \tag{C.14}$$

$$0 = R_{L_o} x_4 + L_o\dot{x}_4 + x_5 + R_{C_o} C_o\dot{x}_5 \tag{C.15}$$

$$0 = C_o\dot{x}_5 + \frac{x_5 + R_{C_o} C_o\dot{x}_5}{R_{load}} - x_4 \tag{C.16}$$

Simultaneously solving the six equations for

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{C.17}$$

then the $\mathbf{A}$ state-space matrix for switching state 0 becomes

$$\mathbf{A}_{S(0)} = \begin{bmatrix} -\frac{R_{C_{bus1}}+R_{L_{eq1}}}{L_{eq1}} & -\frac{1}{L_{eq1}} & 0 & 0 & 0 & 0 \\ \frac{1}{C_{bus1}} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{R_{C_{bus2}}+R_{L_{eq2}}}{L_{eq2}} & -\frac{1}{L_{eq2}} & 0 & 0 \\ 0 & 0 & \frac{1}{C_{bus2}} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{R_{load}R_{C_o}+R_{load}R_{L_o}+R_{C_o}R_{L_o}}{L_o(R_{load}+R_{C_o})} & -\frac{R_{load}}{L_o(R_{load}+R_{C_o})} \\ 0 & 0 & 0 & 0 & \frac{R_{load}}{(C_o(R_{load}+R_{C_o}))} & -\frac{1}{C_o(R_{load}+R_{C_o})} \end{bmatrix} \tag{C.18}$$

## Switching State 1

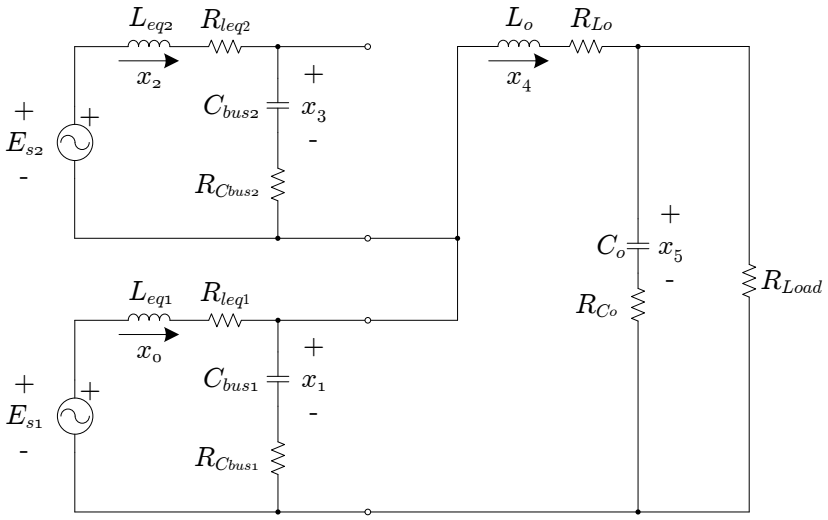



Figure C.4: Schematic circuit diagram of switching state 1, when the bottom converter is in the *on-state* and the top converter is in the *off-state*.

The six unique differential equations that describe this switching state is

$$0 = R_{L_{eq1}} x_0 + L_{eq1}\dot{x}_0 + x_1 + R_{C_{bus1}} C_{bus1}\dot{x}_1 - e_{s1} \tag{C.19}$$

$$0 = C_{bus1}\dot{x}_1 + x_4 - x_0 \tag{C.20}$$

$$0 = R_{L_{eq2}} x_2 + L_{eq2}\dot{x}_2 + x_3 + R_{C_{bus2}} C_{bus2}\dot{x}_3 - e_{s2} \tag{C.21}$$

$$0 = C_{bus2}\dot{x}_3 - x_2 \tag{C.22}$$

$$0 = R_{L_{eq1}} x_0 + L_{eq1}\dot{x}_0 + R_{L_o} x_4 + L_o\dot{x}_4 + x_5 + R_{C_o} C_o\dot{x}_5 - e_{s1} \tag{C.23}$$

$$0 = C_o\dot{x}_5 + \frac{x_5 + R_{C_o} C_o\dot{x}_5}{R_{load}} - x_4 \tag{C.24}$$

Simultaneously solving the six equations for

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{C.25}$$

then the $\mathbf{A}$ state-space matrix for switching state 1 becomes

$$\mathbf{A}_{S(1)} = \begin{bmatrix} -\frac{R_{C_{bus1}}+R_{L_{eq1}}}{L_{eq1}} & -\frac{1}{L_{eq1}} & 0 & 0 & \frac{R_{C_{bus1}}}{L_{eq1}} & 0 \\ \frac{1}{C_{bus1}} & 0 & 0 & 0 & -\frac{1}{C_{bus1}} & 0 \\ 0 & 0 & -\frac{R_{C_{bus2}}+R_{L_{eq2}}}{L_{eq2}} & -\frac{1}{L_{eq2}} & 0 & 0 \\ 0 & 0 & \frac{1}{C_{bus2}} & 0 & 0 & 0 \\ \frac{R_{C_{bus1}}}{L_o} & \frac{1}{L_o} & 0 & 0 & -\frac{R_{load}R_{C_o}}{L_o(R_{load}+R_{C_o})} + -\frac{R_{C_{bus1}}+R_{L_o}}{L_o} & \frac{R_{C_o}}{L_o(R_{load}+R_{C_o})} - \frac{1}{L_o} \\ 0 & 0 & 0 & 0 & \frac{R_{load}}{C_o(R_{load}+R_{C_o})} & -\frac{1}{C_o(R_{load}+R_{C_o})} \end{bmatrix} \tag{C.26}$$

## Switching State 2

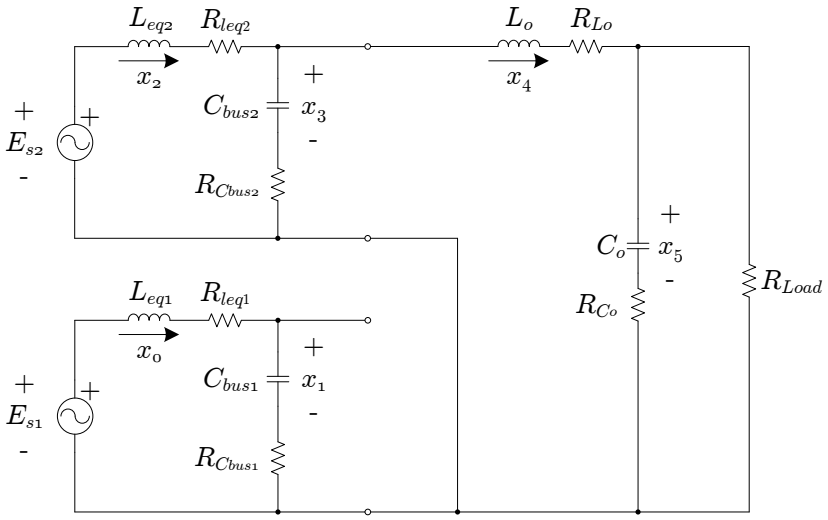



Figure C.5: Schematic circuit diagram of switching state 2, when the top converter is in the *on-state* and the bottom converter is in the *off-state*.

The six unique differential equations that describe this switching state is

$$0 = R_{L_{eq1}} x_0 + L_{eq1}\dot{x}_0 + x_1 + R_{C_{bus1}} C_{bus1}\dot{x}_1 - e_{s1} \tag{C.27}$$

$$0 = C_{bus1}\dot{x}_1 - x_0 \tag{C.28}$$

$$0 = R_{L_{eq2}} x_2 + L_{eq2}\dot{x}_2 + x_3 + R_{C_{bus2}} C_{bus2}\dot{x}_3 - e_{s2} \tag{C.29}$$

$$0 = C_{bus2}\dot{x}_3 + x_4 - x_2 \tag{C.30}$$

$$0 = R_{L_{eq2}} x_2 + L_{eq2}\dot{x}_2 + R_{L_o} x_4 + L_o\dot{x}_4 + x_5 + R_{C_o} C_o\dot{x}_5 - e_{s2} \tag{C.31}$$

$$0 = C_o\dot{x}_5 + \frac{x_5 + R_{C_o} C_o\dot{x}_5}{R_{load}} - x_4 \tag{C.32}$$

Simultaneously solving the six equations for

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{C.33}$$

then the $\mathbf{A}$ state-space matrix for switching state 2 becomes

$$\mathbf{A}_{S(2)} = \begin{bmatrix} -\frac{R_{C_{bus1}}+R_{L_{eq1}}}{L_{eq1}} & -\frac{1}{L_{eq1}} & 0 & 0 & 0 & 0 \\ \frac{1}{C_{bus1}} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{R_{C_{bus2}}+R_{L_{eq2}}}{L_{eq2}} & -\frac{1}{L_{eq2}} & \frac{R_{C_{bus2}}}{L_{eq2}} & 0 \\ 0 & 0 & \frac{1}{C_{bus2}} & 0 & -\frac{1}{C_{bus2}} & 0 \\ 0 & 0 & \frac{R_{C_{bus2}}}{L_o} & \frac{1}{L_o} & -\frac{R_{load}R_{C_o}}{L_o(R_{load}+R_{C_o})} + -\frac{R_{C_{bus2}}+R_{L_o}}{L_o} & \frac{R_{C_o}}{L_o(R_{load}+R_{C_o})} - \frac{1}{L_o} \\ 0 & 0 & 0 & 0 & \frac{R_{load}}{C_o(R_{load}+R_{C_o})} & -\frac{1}{C_o(R_{load}+R_{C_o})} \end{bmatrix} \tag{C.34}$$

## Switching State 3

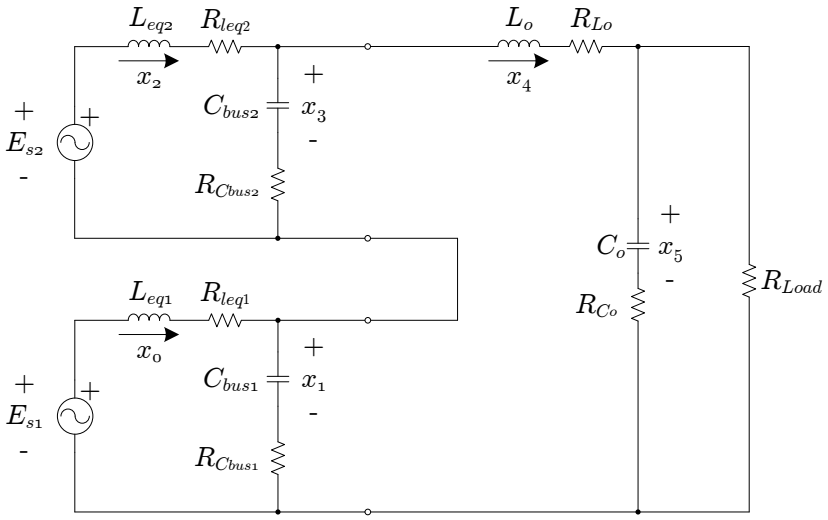



Figure C.6: Schematic circuit diagram of switching state 3, when both converter modules are in the *on-state*.

The six unique differential equations that describe this switching state is

$$0 = R_{L_{eq1}} x_0 + L_{eq1}\dot{x}_0 + x_1 + R_{C_{bus1}} C_{bus1}\dot{x}_1 - e_{s1} \tag{C.35}$$

$$0 = C_{bus1}\dot{x}_1 + x_4 - x_0 \tag{C.36}$$

$$0 = R_{L_{eq2}} x_2 + L_{eq2}\dot{x}_2 + x_3 + R_{C_{bus2}} C_{bus2}\dot{x}_3 - e_{s2} \tag{C.37}$$

$$0 = C_{bus2}\dot{x}_3 + x_4 - x_2 \tag{C.38}$$

$$0 = R_{L_{eq1}} x_0 + L_{eq1}\dot{x}_0 + R_{L_{eq2}} x_2 + L_{eq2}\dot{x}_2 + R_{L_o} x_4 + L_o\dot{x}_4 + x_5 + R_{C_o} C_o\dot{x}_5 - e_{s1} - e_{s2} \tag{C.39}$$

$$0 = C_o\dot{x}_5 + \frac{x_5 + R_{C_o} C_o\dot{x}_5}{R_{load}} - x_4 \tag{C.40}$$

Simultaneously solving the six equations for

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{C.41}$$

then the **A** state-space matrix for switching state 3 becomes

$$\mathbf{A}_{S(3)} = \begin{bmatrix} -\frac{R_{C_{bus1}}+R_{L_{eq1}}}{L_{eq1}} & -\frac{1}{L_{eq1}} & 0 & 0 & \frac{R_{C_{bus1}}}{L_{eq1}} & 0 \\ \frac{1}{C_{bus1}} & 0 & 0 & 0 & -\frac{1}{C_{bus1}} & 0 \\ 0 & 0 & -\frac{R_{C_{bus2}}+-R_{L_{eq2}}}{L_{eq2}} & -\frac{1}{L_{eq2}} & \frac{R_{C_{bus2}}}{L_{eq2}} & 0 \\ 0 & 0 & \frac{1}{C_{bus2}} & 0 & -\frac{1}{C_{bus2}} & 0 \\ \frac{R_{C_{bus1}}}{L_o} & \frac{1}{L_o} & \frac{R_{C_{bus2}}}{L_o} & \frac{1}{L_o} & -\frac{R_{load}R_{C_o}}{L_o(R_{load}+R_{C_o})} + -\frac{R_{C_{bus1}}+R_{C_{bus2}}+R_{Lo}}{L_o} & \frac{R_{C_o}}{L_o(R_{load}+R_{C_o})} - \\ 0 & 0 & 0 & 0 & \frac{R_{load}}{(C_o(R_{load}+R_{C_o}))} & -\frac{1}{(C_o(R_{load}+R_{C_o})} \end{bmatrix} \tag{C.42}$$

### C.1.2 Derivation of the Simulation Model with an Unknown Load

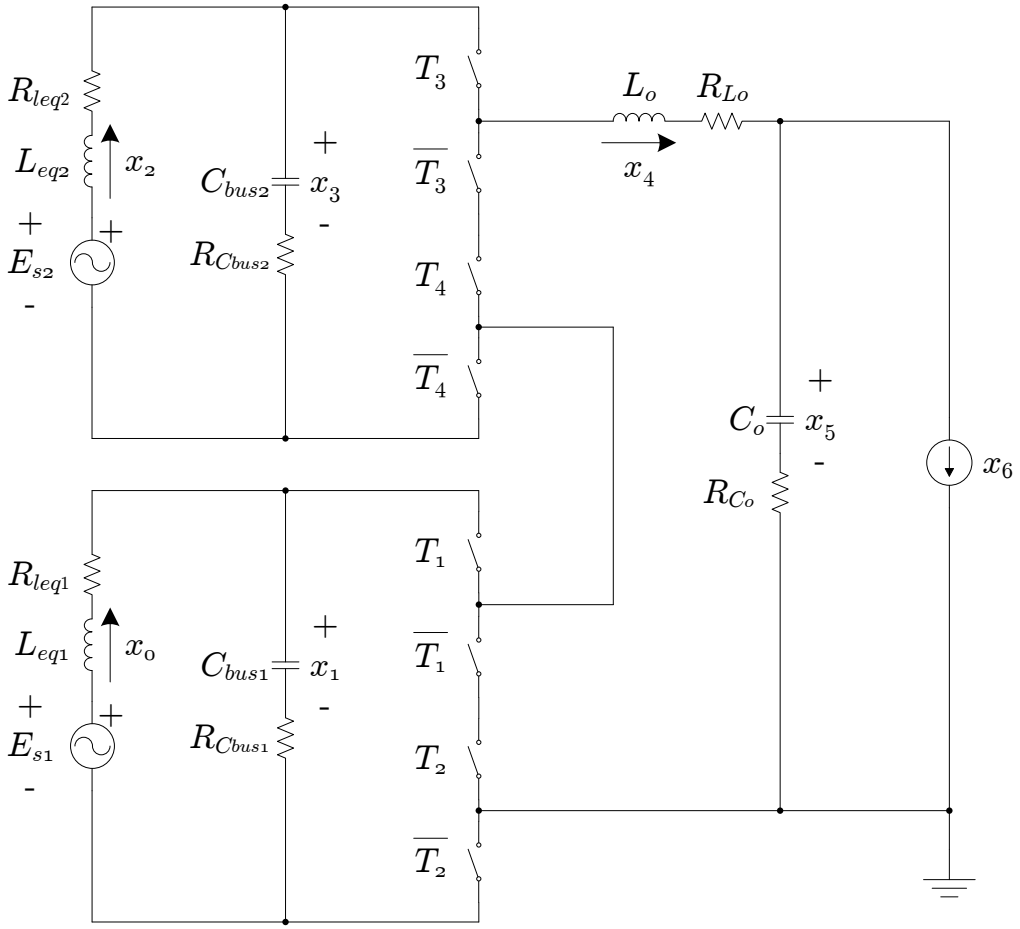



Figure C.7: Equivalent circuit diagram of two cascaded AC-to-AC converters with an unknown load.

This section presents the derivation of the four unique state-space models that describe the switching states of two cascaded AC-to-AC converter modules when the load is unknown. The equivalent circuit diagram of the cascaded converter is given in Figure C.7. The two inductors, $L_{o\_1}$ and $L_{o\_2}$ are in series and can be combined into one equivalent filter inductor $L_o$. The equivalent series resistances (ESR) are also included for the capacitors and inductors. The state vector, $\mathbf{x}(t)$, is defined as

$$\begin{aligned}\mathbf{x}(t) &= \begin{bmatrix} i_{in\_1}(t) & v_{t\_1}(t) & i_{in\_2}(t) & v_{t\_2}(t) & i_{L_o}(t) & v_{out}(t) & i_{out}(t) \end{bmatrix}^\top \\ &= \begin{bmatrix} x_0(t) & x_1(t) & x_2(t) & x_3(t) & x_4(t) & x_5(t) & x_6(t) \end{bmatrix}^\top .\end{aligned} \tag{C.43}$$

The state vector has seven unique state variables and in order to find the state-space matrices, seven unique differential equations are required for each switching state. These equations can be found by taking Kirchoff's voltage and current laws and applying them to all the voltage loops and nodes. The dynamic behaviour for the current through a capacitor is described by

$$i_C(t) = C\frac{\mathrm{d}v}{\mathrm{d}t} \tag{C.44}$$

and the dynamic behaviour for the voltage across an inductor by

$$v_L(t) = L\frac{\mathrm{d}i}{\mathrm{d}t}. \tag{C.45}$$

If the unknown load current, $x_6(t)$, is a 50 Hz sine wave, it can be assumed that it is constant over one switching period, $T_{sw}$, and the dynamic behaviour becomes [51]

$$\frac{\mathrm{d}x_6}{\mathrm{d}t} = 0. \tag{C.46}$$

In a real system it is not always practical to measure all the state variables. If a state observer is used, the measured output vector, $\mathbf{y}(t)$, can be defined as

$$\begin{aligned}\mathbf{y}(t) &= \begin{bmatrix} i_{in\_1}(t) & i_{in\_2}(t) & i_{L_o}(t) & v_{out}(t) \end{bmatrix}^\top \\ &= \begin{bmatrix} x_0(t) & x_1(t) & x_4(t) & x_5(t) \end{bmatrix}^\top .\end{aligned} \tag{C.47}$$

Since the output vector is calculated by [61]

$$\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) + \mathbf{D}\mathbf{u}(t), \tag{C.48}$$

and remains the same for every switching state, the $\mathbf{C}$ and $\mathbf{D}$ matrices remains the same for all the switching states.

The **C** matrices therefore becomes

$$\mathbf{C}_P = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 \end{bmatrix} \tag{C.49}$$

and the **D** matrices

$$\mathbf{D}_P = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}. \tag{C.50}$$

The **A** and **B** matrices for each switching state is derived in the follows section by using the seven unique differential equations that describe each switching state and solving the equations simultaneously such that

$$\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \tag{C.51}$$

holds true, where $\mathbf{u}(t)$ is

$$\mathbf{u}(t) = \begin{bmatrix} e_{s\_1}(t) \\ e_{s\_2}(t) \end{bmatrix}. \tag{C.52}$$

The cascaded converter is viewed as a multiple-input, multiple-output (MIMO) system and from the schematic diagram it is evident that the two inputs, $e_{s1}$ and $e_{s2}$, are always connected to the equivalent input inductance and bus capacitor. As a result the input state matrix, **B**, will be the same for all the switching states. Solving **B** according to differential equations, as discussed in the following sections, the input state matrix becomes

$$\mathbf{B}_P = \begin{bmatrix} \frac{1}{L_{eq1}} & 0 \\ 0 & 0 \\ 0 & \frac{1}{L_{eq2}} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}. \tag{C.53}$$

## Switching State 0

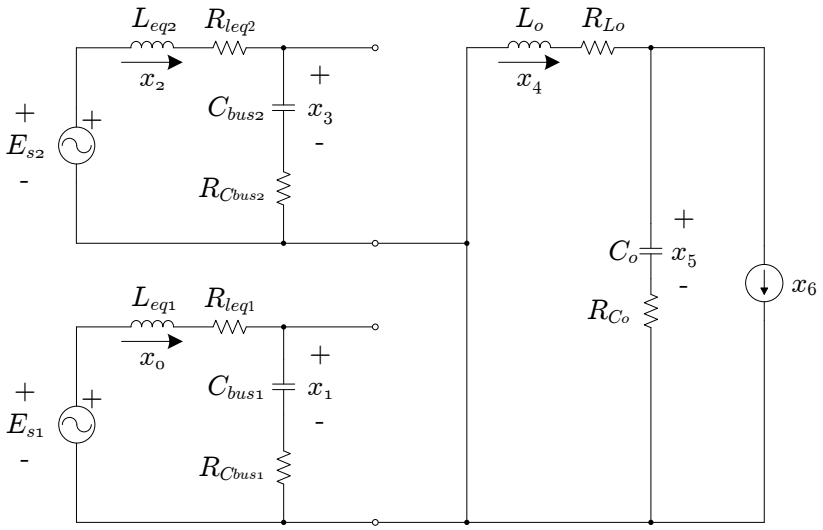



Figure C.8: Schematic circuit diagram with an unknown load for switching state 0, when both converter modules are in the *off-state*.

The seven unique differential equations that describe this switching state is

$$0 = R_{L_{eq1}} x_0 + L_{eq1}\dot{x}_0 + x_1 + R_{C_{bus1}} C_{bus1}\dot{x}_1 - e_{s1} \tag{C.54}$$

$$0 = C_{bus1}\dot{x}_1 - x_0 \tag{C.55}$$

$$0 = R_{L_{eq2}} x_2 + L_{eq2}\dot{x}_2 + x_3 + R_{C_{bus2}} C_{bus2}\dot{x}_3 - e_{s2} \tag{C.56}$$

$$0 = C_{bus2}\dot{x}_3 - x_2 \tag{C.57}$$

$$0 = R_{L_o} x_4 + L_o\dot{x}_4 + x_5 + R_{C_o} C_o\dot{x}_5 \tag{C.58}$$

$$0 = C_o\dot{x}_5 + x_6 - x_4 \tag{C.59}$$

$$0 = \dot{x}_6 \tag{C.60}$$

Simultaneously solving the seven equations for

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{C.61}$$

then the **A** state-space matrix for switching state 0 becomes

$$\mathbf{A}_{P(0)} = \begin{bmatrix} -\frac{(R_{C_{bus1}}+R_{L_{eq1}})}{L_{eq1}} & -\frac{1}{L_{eq1}} & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_{bus1}} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{(R_{C_{bus2}}+R_{L_{eq2}})}{L_{eq2}} & -\frac{1}{L_{eq2}} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_{bus2}} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{(R_{C_o}+R_{L_o})}{L_o} & -\frac{1}{L_o} & \frac{R_{C_o}}{L_o} \\ 0 & 0 & 0 & 0 & \frac{1}{C_o} & 0 & -\frac{1}{C_o} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{C.62}$$

## Switching State 1

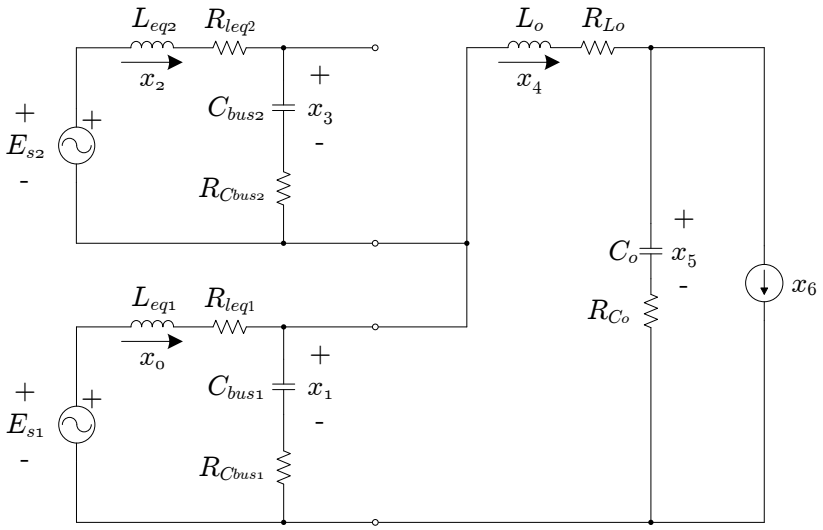



Figure C.9: Schematic circuit diagram with an unknown load for switching state 1, when the bottom converter is in the *on-state* and the top converter is in the *off-state*.

The seven unique differential equations that describe this switching state is

$$0 = R_{L_{eq1}} x_0 + L_{eq1}\dot{x}_0 + x_1 + R_{C_{bus1}} C_{bus1}\dot{x}_1 - e_{s1} \tag{C.63}$$

$$0 = C_{bus1}\dot{x}_1 + x_4 - x_0 \tag{C.64}$$

$$0 = R_{L_{eq2}} x_2 + L_{eq2}\dot{x}_2 + x_3 + R_{C_{bus2}} C_{bus2}\dot{x}_3 - e_{s2} \tag{C.65}$$

$$0 = C_{bus2}\dot{x}_3 - x_2 \tag{C.66}$$

$$0 = R_{L_{eq1}} x_0 + L_{eq1}\dot{x}_0 + R_{L_o} x_4 + L_o\dot{x}_4 + x_5 + R_{C_o} C_o\dot{x}_5 - e_{s1} \tag{C.67}$$

$$0 = C_o\dot{x}_5 + x_6 - x_4 \tag{C.68}$$

$$0 = \dot{x}_6 \tag{C.69}$$

Simultaneously solving the seven equations for

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{C.70}$$

then the **A** state-space matrix for switching state 1 becomes

$$\mathbf{A}_{P(1)} = \begin{bmatrix} -\frac{(R_{C_{bus1}}+R_{L_{eq1}})}{L_{eq1}} & -\frac{1}{L_{eq1}} & 0 & 0 & \frac{R_{C_{bus1}}}{L_{eq1}} & 0 & 0 \\ \frac{1}{C_{bus1}} & 0 & 0 & 0 & -\frac{1}{C_{bus1}} & 0 & 0 \\ 0 & 0 & -\frac{(R_{C_{bus2}}+R_{L_{eq2}})}{L_{eq2}} & -\frac{1}{L_{eq2}} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_{bus2}} & 0 & 0 & 0 & 0 \\ \frac{R_{C_{bus1}}}{L_o} & \frac{1}{L_o} & 0 & 0 & -\frac{(R_{C_{bus1}}+R_{C_o}+R_{L_o})}{L_o} & -\frac{1}{L_o} & \frac{R_{C_o}}{L_o} \\ 0 & 0 & 0 & 0 & \frac{1}{C_o} & 0 & -\frac{1}{C_o} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{C.71}$$

## Switching State 2

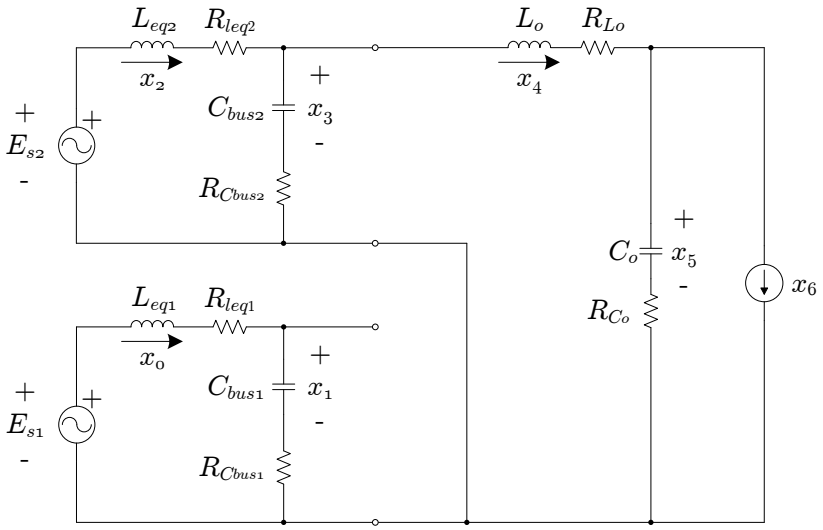



Figure C.10: Schematic circuit diagram with an unknown load for switching state 2, when the top converter is in the *on-state* and the bottom converter is in the *off-state*.

The seven unique differential equations that describe this switching state is

$$0 = R_{L_{eq1}} x_0 + L_{eq1}\dot{x}_0 + x_1 + R_{C_{bus1}} C_{bus1}\dot{x}_1 - e_{s1} \tag{C.72}$$

$$0 = C_{bus1}\dot{x}_1 - x_0 \tag{C.73}$$

$$0 = R_{L_{eq2}} x_2 + L_{eq2}\dot{x}_2 + x_3 + R_{C_{bus2}} C_{bus2}\dot{x}_3 - e_{s2} \tag{C.74}$$

$$0 = C_{bus2}\dot{x}_3 + x_4 - x_2 \tag{C.75}$$

$$0 = R_{L_{eq2}} x_2 + L_{eq2}\dot{x}_2 + R_{L_o} x_4 + L_o\dot{x}_4 + x_5 + R_{C_o} C_o\dot{x}_5 - e_{s2} \tag{C.76}$$

$$0 = C_o\dot{x}_5 + x_6 - x_4 \tag{C.77}$$

$$0 = \dot{x}_6 \tag{C.78}$$

Simultaneously solving the seven equations for

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{C.79}$$

then the **A** state-space matrix for switching state 2 becomes

$$\mathbf{A}_{P(2)} = \begin{bmatrix} -\frac{(R_{C_{bus1}}+R_{L_{eq1}})}{L_{eq1}} & -\frac{1}{L_{eq1}} & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_{bus1}} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{(R_{C_{bus2}}+R_{L_{eq2}})}{L_{eq2}} & -\frac{1}{L_{eq2}} & \frac{R_{C_{bus2}}}{L_{eq2}} & 0 & 0 \\ 0 & 0 & \frac{1}{C_{bus2}} & 0 & -\frac{1}{C_{bus2}} & 0 & 0 \\ 0 & 0 & \frac{R_{C_{bus2}}}{L_o} & \frac{1}{L_o} & -\frac{(R_{C_{bus2}}+R_{C_o}+R_{L_o})}{L_o} & -\frac{1}{L_o} & \frac{R_{C_o}}{L_o} \\ 0 & 0 & 0 & 0 & \frac{1}{C_o} & 0 & -\frac{1}{C_o} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{C.80}$$

## Switching State 3

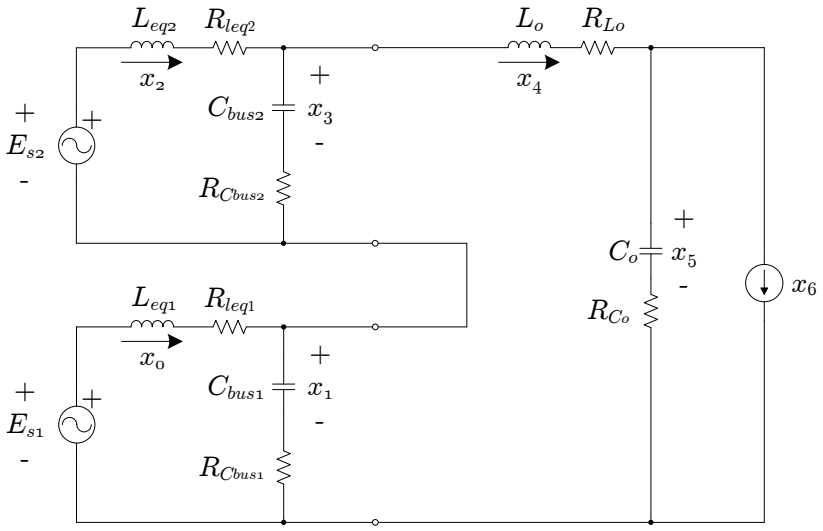



Figure C.11: Schematic circuit diagram with an unknown load for switching state 3, when both converter modules are in the *on-state*.

The seven unique differential equations that describe this switching state is

$$0 = R_{L_{eq1}} x_0 + L_{eq1}\dot{x}_0 + x_1 + R_{C_{bus1}} C_{bus1}\dot{x}_1 - e_{s1} \tag{C.81}$$

$$0 = C_{bus1}\dot{x}_1 + x_4 - x_0 \tag{C.82}$$

$$0 = R_{L_{eq2}} x_2 + L_{eq2}\dot{x}_2 + x_3 + R_{C_{bus2}} C_{bus2}\dot{x}_3 - e_{s2} \tag{C.83}$$

$$0 = C_{bus2}\dot{x}_3 + x_4 - x_2 \tag{C.84}$$

$$0 = R_{L_{eq1}} x_0 + L_{eq1}\dot{x}_0 + R_{L_{eq2}} x_2 + L_{eq2}\dot{x}_2 + R_{L_o} x_4 + L_o\dot{x}_4 + x_5 + R_{C_o} C_o\dot{x}_5 - e_{s1} - e_{s2} \tag{C.85}$$

$$0 = C_o\dot{x}_5 + x_6 - x_4 \tag{C.86}$$

$$0 = \dot{x}_6 \tag{C.87}$$

Simultaneously solving the seven equations for

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{C.88}$$

then the **A** state-space matrix for switching state 3 becomes

$$\mathbf{A}_{P(3)} = \begin{bmatrix} -\frac{(R_{C_{bus1}}+R_{L_{eq1}})}{L_{eq1}} & -\frac{1}{L_{eq1}} & 0 & 0 & \frac{R_{C_{bus1}}}{L_{eq1}} & 0 & 0 \\ \frac{1}{C_{bus1}} & 0 & 0 & 0 & -\frac{1}{C_{bus1}} & 0 & 0 \\ 0 & 0 & -\frac{(R_{C_{bus2}}+R_{L_{eq2}})}{L_{eq2}} & -\frac{1}{L_{eq2}} & \frac{R_{C_{bus2}}}{L_{eq2}} & 0 & 0 \\ 0 & 0 & \frac{1}{C_{bus2}} & 0 & -\frac{1}{C_{bus2}} & 0 & 0 \\ \frac{R_{C_{bus1}}}{L_o} & \frac{1}{L_o} & \frac{R_{C_{bus2}}}{L_o} & \frac{1}{L_o} & -\frac{(R_{C_{bus1}}+R_{C_{bus2}}+R_{C_o}+R_{L_o})}{L_o} & -\frac{1}{L_o} & \frac{R_{C_o}}{L_o} \\ 0 & 0 & 0 & 0 & \frac{1}{C_o} & 0 & -\frac{1}{C_o} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{C.89}$$

## C.2 Model Derivation of the 5-level H-Bridge Flying Capacitor Converter

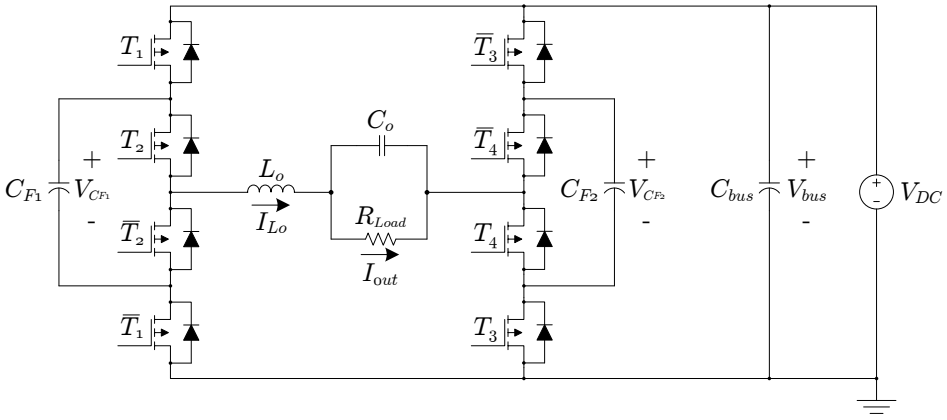



Figure C.12: Schematic diagram of the 5-level H-bridge flying capacitor converter.

This section presents the derivation of the state-space models for each switching state of the H-bridge Flying Capacitor Converter (FCC) that is evaluated in Chapter 5. The state-space models are used to calculate the prediction equations that are stored off-line according to the algorithm that is discussed in Chapter 3. Consider the schematic

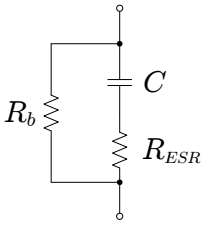



Figure C.13: Equivalent model of the flying capacitors.

diagram of the practical FCC converter topology in Figure C.12. The converter consists of two phase arms where each phase arm has two complementary switching pairs. When switch $T_1$ and $T_2$ are both turned *on* or both turned *off*, the one terminal of capacitor $C_{f1}$ is left to float. Likewise, when $T_3$ and $T_4$ are both in the same switching state, capacitor $C_{f2}$ is left to float, hence the name, flying capacitor converter. However, the disconnected capacitors may present a problem when solving the differential equations by using a numerical software toolbox.

The higher the number of levels of the FCC converter, the more switching states exist and the derivation of the models and calculation of the off-line prediction equations can become too cumbersome to calculate by hand. In such cases it is often useful to derive and solve the differential equations by using software such as Python. Python, together with the numerical package, Numpy, and the symbolic toolbox, Sympy, is sufficient to

symbolically solve all the switching states of the 5-level FCC converter. To ensure that the symbolic solver can solve the equations for all the switching states, a large bleeding resistor is added in parallel to each flying capacitor as well as the equivalent series resistances of all the capacitors and inductors. The equivalent model of the flying capacitor is shown in Figure C.13

The state vector, $\mathbf{x}(t)$, containing the state variables can be defined as

$$\begin{aligned}\mathbf{x}(t) &= \begin{bmatrix} i_{Lo}(t) & v_{out}(t) & v_{C_{f1}}(t) & v_{C_{f2}}(t) & i_{out}(t) \end{bmatrix}^\top \\ &= \begin{bmatrix} x_0(t) & x_1(t) & x_2(t) & x_3(t) & x_4(t) \end{bmatrix}^\top .\end{aligned} \tag{C.90}$$

To have a model that is independent of the load resistance, the load can be modelled by an unknown current source, $x_4(t)$. If the DC bus is viewed as an ideal voltage source, the bus capacitor, $C_{bus}$, can be ignored and the estimated circuit diagram of the flying capacitor converter becomes as shown in Figure C.14.

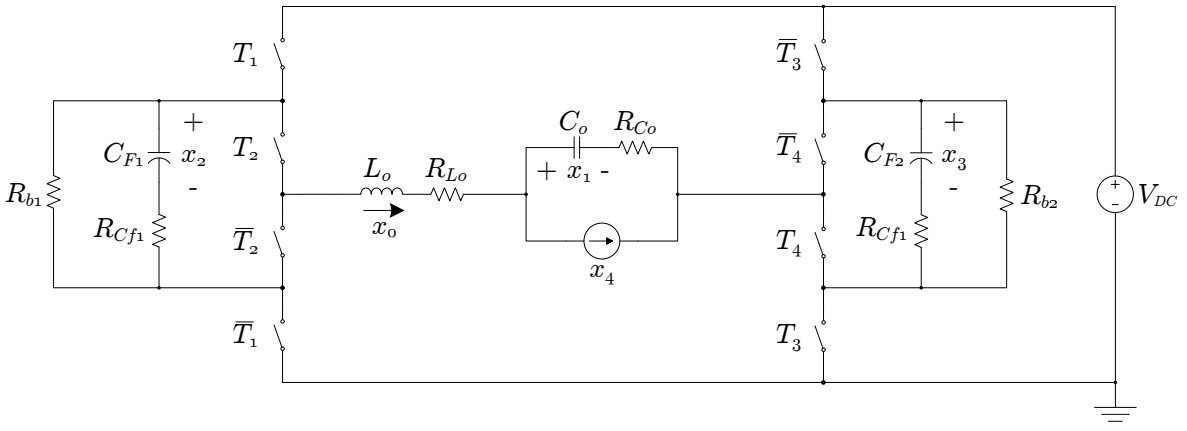



Figure C.14: Estimated circuit diagram of the FCC Converter used to derive the prediction models.

The state vector has five unique state variables and in order to find the state-space matrices, five unique differential equations describing the dynamic behaviour for each state are required. These equations can be found by taking Kirchoff's voltage and current laws and applying them to all the voltage loops and nodes. The dynamic behaviour for the current through a capacitor is given by

$$i_C(t) = C\frac{\mathrm{d}v}{\mathrm{d}t} \tag{C.91}$$

and the dynamic behaviour for the voltage across an inductor by

$$v_L(t) = L\frac{\mathrm{d}i}{\mathrm{d}t}. \tag{C.92}$$

If the unknown load current, $x_4(t)$, is a 50 Hz sine wave, it can be assumed that it is constant over one switching period, $T_{sw}$, and the dynamic behaviour becomes [51]

$$\frac{\mathrm{d}x_4}{\mathrm{d}t} = 0. \tag{C.93}$$

If all the state variables of the FCC converter are measured and equivalent series resistances in the measurements are ignored, the output vector, $\mathbf{y}(t)$, becomes

$$\begin{aligned}\mathbf{y}(t) &= \begin{bmatrix} i_{Lo}(t) & v_{out}(t) & v_{C_{f1}}(t) & v_{C_{f2}}(t) & i_{out}(t) \end{bmatrix}^\top \\ &= \begin{bmatrix} x_0(t) & x_1(t) & x_2(t) & x_3(t) & x_4(t) \end{bmatrix}^\top .\end{aligned} \tag{C.94}$$

Since the output vector is calculated by [61]

$$\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) + \mathbf{D}u(t), \tag{C.95}$$

and remains the same for every switching state, the $\mathbf{C}$ and $\mathbf{D}$ matrices remains the same for all the switching states.

The $\mathbf{C}$ matrices therefore becomes

$$\mathbf{C} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{C.96}$$

and the $\mathbf{D}$ matrices

$$\mathbf{D} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}. \tag{C.97}$$

The $\mathbf{A}$ and $\mathbf{B}$ matrices for each switching state is derived in the follows section by using the five unique differential equations that describe each switching state and solving the equations simultaneously such that

$$\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}u(t) \tag{C.98}$$

holds true, where $u(t)$ is the measured DC bus voltage.

## Switching State 0

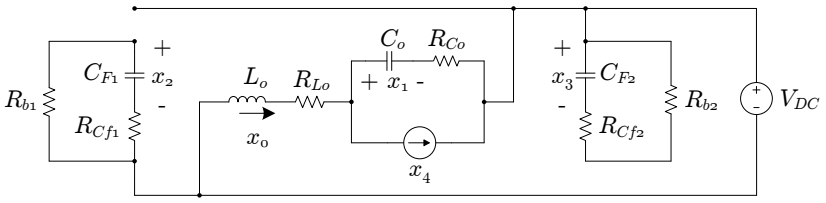



Figure C.15: Schematic circuit diagram of switching state 0 when $T_4$(off), $T_3$(off), $T_2$(off), $T_1$(off).

The five unique differential equations that describe this switching state is

$$0 = L_o\dot{x}_0 + r_{L_o}x_0 + x_1 + r_{C_o}C_o\dot{x}_1 + V_{DC} \tag{C.99}$$

$$0 = C_{f1}\dot{x}_2 + \frac{1}{r_{b1}}\left(x_2 + r_{C_{f1}}C_{f1}\dot{x}_2\right) \tag{C.100}$$

$$0 = C_{f2}\dot{x}_3 + \frac{1}{r_{b2}}\left(x_3 + r_{C_{f2}}C_{f2}\dot{x}_3\right) \tag{C.101}$$

$$0 = x_0 - C_0\dot{x}_1 - x_4 \tag{C.102}$$

$$0 = \dot{x}_4. \tag{C.103}$$

Simultaneously solving the five equations for

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}V_{DC} \tag{C.104}$$

then the $\mathbf{A}$ and $\mathbf{B}$ matrices for switching state 0 becomes

$$\mathbf{A}_{(0)} = \begin{bmatrix} \frac{(-r_{C_o}-r_{L_o})}{L_o} & \frac{-1}{L_o} & 0 & 0 & \frac{r_{C_o}}{L_o} \\ \frac{1}{C_o} & 0 & 0 & 0 & \frac{-1}{C_o} \\ 0 & 0 & \frac{-1}{C_{f1}(r_{b1}+r_{C_{f1}})} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{C_{f2}(r_{b2}+r_{C_{f2}})} & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{C.105}$$

$$\mathbf{B}_{(0)} = \begin{bmatrix} -\frac{1}{L_o} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{C.106}$$

## Switching State 1

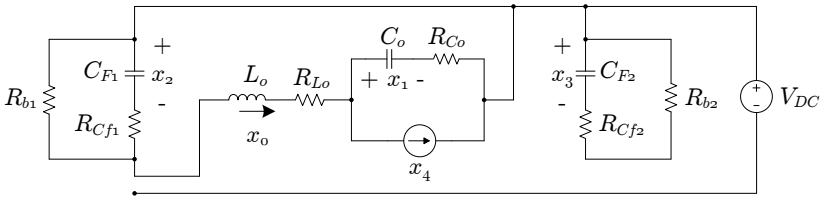



Figure C.16: Schematic circuit diagram of switching state 1 when $T_4$(off), $T_3$(off), $T_2$(off), $T_1$(on).

The five unique differential equations that describe this switching state is

$$0 = L_o\dot{x}_0 + r_{L_o}x_0 + x_1 + r_{C_o}C_o\dot{x}_1 + x_2 + r_{C_{f1}}C_{f1}\dot{x}_2 \tag{C.107}$$

$$0 = x_0 - C_{f1}\dot{x}_2 - \frac{1}{r_{b1}}\left(x_2 + r_{C_{f1}}C_{f1}\dot{x}_2\right) \tag{C.108}$$

$$0 = C_{f2}\dot{x}_3 + \frac{1}{r_{b2}}\left(x_3 + r_{C_{f2}}C_{f2}\dot{x}_3\right) \tag{C.109}$$

$$0 = x_0 - C_0\dot{x}_1 - x_4 \tag{C.110}$$

$$0 = \dot{x}_4. \tag{C.111}$$

Simultaneously solving the five equations for

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}V_{DC} \tag{C.112}$$

then the $\mathbf{A}$ and $\mathbf{B}$ matrices for switching state 1 becomes

$$\mathbf{A}_{(1)} = \begin{bmatrix} \frac{-r_{b1}r_{C_{f1}}}{L_o(r_{b1}+r_{C_{f1}})} - \frac{r_{C_o}}{L_o} - \frac{r_{L_o}}{L_o} & \frac{-1}{L_o} & \frac{r_{C_{f1}}}{L_o(r_{b1}+r_{C_{f1}})} - \frac{1}{L_o} & 0 & \frac{r_{C_o}}{L_o} \\ \frac{1}{C_o} & 0 & 0 & 0 & \frac{-1}{C_o} \\ \frac{r_{b1}}{C_{f1}(r_{b1}+r_{C_{f1}})} & 0 & \frac{-1}{C_{f1}(r_{b1}+r_{C_{f1}})} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{C_{f2}(r_{b2}+r_{C_{f2}})} & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{C.113}$$

$$\mathbf{B}_{(1)} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{C.114}$$

## Switching State 2

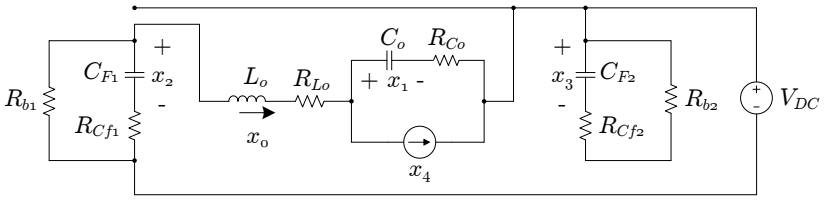



Figure C.17: Schematic circuit diagram of switching state 2 when $T_4$(off), $T_3$(off), $T_2$(on), $T_1$(off).

The five unique differential equations that describe this switching state is

$$0 = L_o\dot{x}_0 + r_{L_o}x_0 + x_1 + r_{C_o}C_o\dot{x}_1 - x_2 - r_{C_{f1}}C_{f1}\dot{x}_2 + V_{DC} \tag{C.115}$$

$$0 = x_0 + C_{f1}\dot{x}_2 + \frac{1}{r_{b1}}\left(x_2 + r_{C_{f1}}C_{f1}\dot{x}_2\right) \tag{C.116}$$

$$0 = C_{f2}\dot{x}_3 + \frac{1}{r_{b2}}\left(x_3 + r_{C_{f2}}C_{f2}\dot{x}_3\right) \tag{C.117}$$

$$0 = x_0 - C_0\dot{x}_1 - x_4 \tag{C.118}$$

$$0 = \dot{x}_4. \tag{C.119}$$

Simultaneously solving the five equations for

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}V_{DC} \tag{C.120}$$

then the $\mathbf{A}$ and $\mathbf{B}$ matrices for switching state 2 becomes

$$\mathbf{A}_{(2)} = \begin{bmatrix} \frac{-r_{b1}r_{C_{f1}}}{L_o(r_{b1}+r_{C_{f1}})} - \frac{r_{C_o}}{L_o} - \frac{r_{L_o}}{L_o} & \frac{-1}{L_o} & \frac{-r_{C_{f1}}}{L_o(r_{b1}+r_{C_{f1}})} + \frac{1}{L_o} & 0 & \frac{r_{C_o}}{L_o} \\ \frac{1}{C_o} & 0 & 0 & 0 & \frac{-1}{C_o} \\ \frac{-r_{b1}}{C_{f1}(r_{b1}+r_{C_{f1}})} & 0 & \frac{-1}{C_{f1}(r_{b1}+r_{C_{f1}})} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{C_{f2}(r_{b2}+r_{C_{f2}})} & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{C.121}$$

$$\mathbf{B}_{(2)} = \begin{bmatrix} -\frac{1}{L_o} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{C.122}$$

## Switching State 3

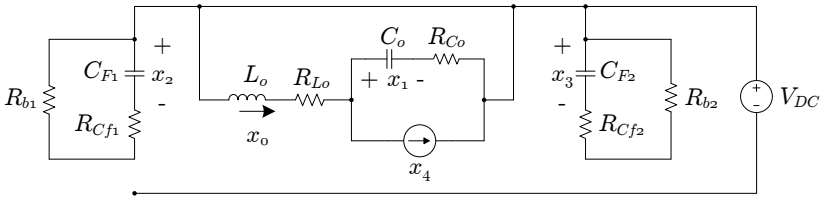



Figure C.18: Schematic circuit diagram of switching state 3 when $T_4$(off), $T_3$(off), $T_2$(on), $T_1$(on).

The five unique differential equations that describe this switching state is

$$0 = L_o\dot{x}_0 + r_{L_o}x_0 + x_1 + r_{C_o}C_o\dot{x}_1 \tag{C.123}$$

$$0 = C_{f1}\dot{x}_2 + \frac{1}{r_{b1}}\left(x_2 + r_{C_{f1}}C_{f1}\dot{x}_2\right) \tag{C.124}$$

$$0 = C_{f2}\dot{x}_3 + \frac{1}{r_{b2}}\left(x_3 + r_{C_{f2}}C_{f2}\dot{x}_3\right) \tag{C.125}$$

$$0 = x_0 - C_0\dot{x}_1 - x_4 \tag{C.126}$$

$$0 = \dot{x}_4. \tag{C.127}$$

Simultaneously solving the five equations for

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}V_{DC} \tag{C.128}$$

then the $\mathbf{A}$ and $\mathbf{B}$ matrices for switching state 3 becomes

$$\mathbf{A}_{(3)} = \begin{bmatrix} \frac{(-r_{C_o}-r_{L_o})}{L_o} & \frac{-1}{L_o} & 0 & 0 & \frac{r_{C_o}}{L_o} \\ \frac{1}{C_o} & 0 & 0 & 0 & \frac{-1}{C_o} \\ 0 & 0 & \frac{-1}{C_{f1}(r_{b1}+r_{C_{f1}})} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{C_{f2}(r_{b2}+r_{C_{f2}})} & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{C.129}$$

$$\mathbf{B}_{(3)} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{C.130}$$

## Switching State 4

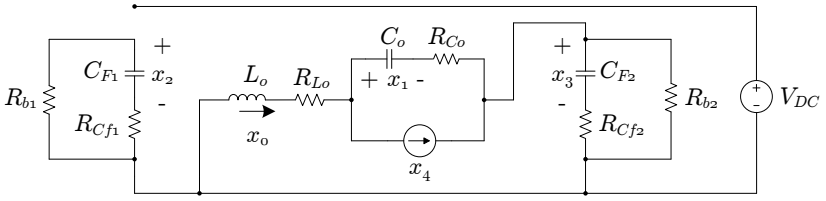



Figure C.19: Schematic circuit diagram of switching state 4 when $T_4$(off), $T_3$(on), $T_2$(off), $T_1$(off).

The five unique differential equations that describe this switching state is

$$0 = L_o\dot{x}_0 + r_{L_o}x_0 + x_1 + r_{C_o}C_o\dot{x}_1 + x_3 + r_{C_{f2}}C_{f2}\dot{x}_3 \tag{C.131}$$

$$0 = C_{f1}\dot{x}_2 + \frac{1}{r_{b1}}\left(x_2 + r_{C_{f1}}C_{f1}\dot{x}_2\right) \tag{C.132}$$

$$0 = x_0 - C_{f2}\dot{x}_3 - \frac{1}{r_{b2}}\left(x_3 + r_{C_{f2}}C_{f2}\dot{x}_3\right) 0 \qquad = x_0 - C_0\dot{x}_1 - x_4 \tag{C.133}$$

$$0 = \dot{x}_4. \tag{C.134}$$

Simultaneously solving the five equations for

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}V_{DC} \tag{C.135}$$

then the $\mathbf{A}$ and $\mathbf{B}$ matrices for switching state 4 becomes

$$\mathbf{A}_{(4)} = \begin{bmatrix} \frac{-r_{b2}r_{C_{f2}}}{L_o(r_{b2}+r_{C_{f2}})} - \frac{r_{C_o}}{L_o} - \frac{r_{L_o}}{L_o} & \frac{-1}{L_o} & 0 & \frac{r_{C_{f2}}}{L_o(r_{b2}+r_{C_{f2}})} - \frac{1}{L_o} & \frac{r_{C_o}}{L_o} \\ \frac{1}{C_o} & 0 & 0 & 0 & \frac{-1}{C_o} \\ 0 & 0 & \frac{-1}{C_{f1}(r_{b1}+r_{C_{f1}})} & 0 & 0 \\ \frac{r_{b2}}{C_{f2}(r_{b2}+r_{C_{f2}})} & 0 & 0 & \frac{-1}{C_{f2}(r_{b2}+r_{C_{f2}})} & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{C.136}$$

$$\mathbf{B}_{(4)} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{C.137}$$

## Switching State 5

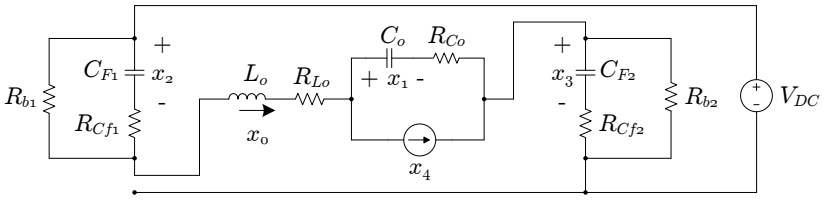



Figure C.20: Schematic circuit diagram of switching state 5 when $T_4$(off), $T_3$(on), $T_2$(off), $T_1$(on).

The five unique differential equations that describe this switching state is

$$0 = L_o\dot{x}_0 + r_{L_o}x_0 + x_1 + r_{C_o}C_o\dot{x}_1 + x_3 + r_{C_{f2}}C_{f2}\dot{x}_3 - V_{DC} + x_2 \; + r_{C_{f1}}C_{f1}\dot{x}_2 \tag{C.138}$$

$$0 = x_0 - C_{f1}\dot{x}_2 - \frac{1}{r_{b1}}\left(x_2 + r_{C_{f1}}C_{f1}\dot{x}_2\right) \tag{C.139}$$

$$0 = x_0 - C_{f2}\dot{x}_3 - \frac{1}{r_{b2}}\left(x_3 + r_{C_{f2}}C_{f2}\dot{x}_3\right) 0 \qquad = x_0 - C_0\dot{x}_1 - x_4 \tag{C.140}$$

$$0 = \dot{x}_4 \tag{C.141}$$

Simultaneously solving the five equations for

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}V_{DC} \tag{C.142}$$

then the $\mathbf{A}$ and $\mathbf{B}$ matrices for switching state 5 becomes

$$\mathbf{A}_{(5)} = \begin{bmatrix} \frac{-r_{b1}r_{C_{f1}}}{L_o(r_{b1}+r_{C_{f1}})} - \frac{r_{b2}r_{C_{f2}}}{L_o(r_{b2}+r_{C_{f2}})} - \frac{r_{C_o}}{L_o} - \frac{r_{L_o}}{L_o} & \frac{-1}{L_o} & \frac{r_{C_{f1}}}{L_o(r_{b1}+r_{C_{f1}})} - \frac{1}{L_o} & \frac{r_{C_{f2}}}{L_o(r_{b2}+r_{C_{f2}})} - \frac{1}{L_o} & \frac{r_{C_o}}{L_o} \\ \frac{1}{C_o} & 0 & 0 & 0 & \frac{-1}{C_o} \\ \frac{r_{b1}}{C_{f1}(r_{b1}+r_{C_{f1}})} & 0 & \frac{-1}{C_{f1}(r_{b1}+r_{C_{f1}})} & 0 & 0 \\ \frac{r_{b2}}{C_{f2}(r_{b2}+r_{C_{f2}})} & 0 & 0 & \frac{-1}{C_{f2}(r_{b2}+r_{C_{f2}})} & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{C.143}$$

$$\mathbf{B}_{(5)} = \begin{bmatrix} \frac{1}{L_o} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{C.144}$$

## Switching State 6

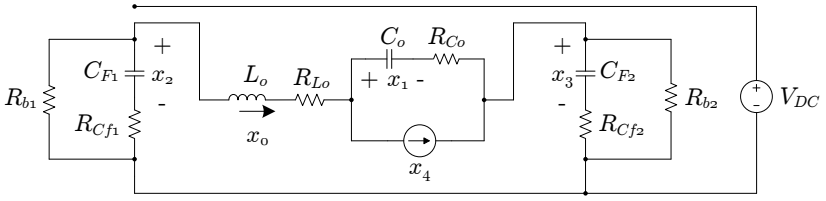



Figure C.21: Schematic circuit diagram of switching state 6 when $T_4$(off), $T_3$(on), $T_2$(on), $T_1$(off).

The five unique differential equations that describe this switching state is

$$0 = L_o\dot{x}_0 + r_{L_o}x_0 + x_1 + r_{C_o}C_o\dot{x}_1 + x_3 + r_{C_{f2}}C_{f2}\dot{x}_3 - x_2 \; - r_{C_{f1}}C_{f1}\dot{x}_2 \tag{C.145}$$

$$0 = x_0 + C_{f1}\dot{x}_2 + \frac{1}{r_{b1}}\left(x_2 + r_{C_{f1}}C_{f1}\dot{x}_2\right) \tag{C.146}$$

$$0 = x_0 - C_{f2}\dot{x}_3 - \frac{1}{r_{b2}}\left(x_3 + r_{C_{f2}}C_{f2}\dot{x}_3\right) \tag{C.147}$$

$$0 = x_0 - C_0\dot{x}_1 - x_4 \tag{C.148}$$

$$0 = \dot{x}_4. \tag{C.149}$$

Simultaneously solving the five equations for

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}V_{DC} \tag{C.150}$$

then the $\mathbf{A}$ and $\mathbf{B}$ matrices for switching state 6 becomes

$$\mathbf{A}_{(6)} = \begin{bmatrix} \frac{-r_{b1}r_{C_{f1}}}{L_o(r_{b1}+r_{C_{f1}})} - \frac{r_{b2}r_{C_{f2}}}{L_o(r_{b2}+r_{C_{f2}})} - \frac{r_{C_o}}{L_o} - \frac{r_{L_o}}{L_o} & \frac{-1}{L_o} & \frac{-r_{C_{f1}}}{L_o(r_{b1}+r_{C_{f1}})} + \frac{1}{L_o} & \frac{r_{C_{f2}}}{L_o(r_{b2}+r_{C_{f2}})} - \frac{1}{L_o} & \frac{r_{C_o}}{L_o} \\ \frac{1}{C_o} & 0 & 0 & 0 & \frac{-1}{C_o} \\ \frac{-r_{b1}}{C_{f1}(r_{b1}+r_{C_{f1}})} & 0 & \frac{-1}{C_{f1}(r_{b1}+r_{C_{f1}})} & 0 & 0 \\ \frac{r_{b2}}{C_{f2}(r_{b2}+r_{C_{f2}})} & 0 & 0 & \frac{-1}{C_{f2}(r_{b2}+r_{C_{f2}})} & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{C.151}$$

$$\mathbf{B}_{(6)} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{C.152}$$

## Switching State 7

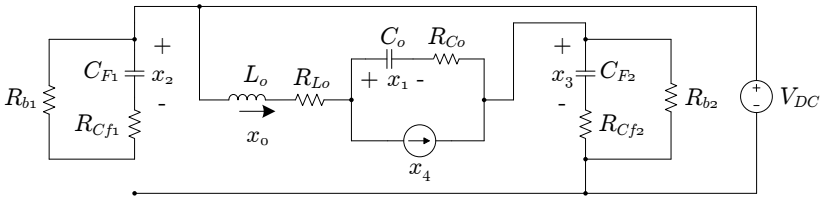



Figure C.22: Schematic circuit diagram of switching state 7 when $T_4$(off), $T_3$(on), $T_2$(on), $T_1$(on).

The five unique differential equations that describe this switching state is

$$0 = L_o\dot{x}_0 + r_{L_o}x_0 + x_1 + r_{C_o}C_o\dot{x}_1 + x_3 + r_{Cf2}C_{f2}\dot{x}_3 - V_{DC} \tag{C.153}$$

$$0 = C_{f1}\dot{x}_2 + \frac{1}{r_{b1}}\left(x_2 + r_{C_{f1}}C_{f1}\dot{x}_2\right) \tag{C.154}$$

$$0 = x_0 - C_{f2}\dot{x}_3 - \frac{1}{r_{b2}}\left(x_3 + r_{C_{f2}}C_{f2}\dot{x}_3\right) \tag{C.155}$$

$$0 = x_0 - C_0\dot{x}_1 - x_4 \tag{C.156}$$

$$0 = \dot{x}_4 \tag{C.157}$$

Simultaneously solving the five equations for

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}V_{DC} \tag{C.158}$$

then the $\mathbf{A}$ and $\mathbf{B}$ matrices for switching state 7 becomes

$$\mathbf{A}_{(7)} = \begin{bmatrix} \frac{-r_{b2}r_{Cf2}}{L_o(r_{b2}+r_{Cf2})} - \frac{r_{Co}}{L_o} - \frac{r_{Lo}}{L_o} & \frac{-1}{L_o} & 0 & \frac{r_{Cf2}}{L_o(r_{b2}+r_{Cf2})} - \frac{1}{L_o} & \frac{r_{Co}}{L_o} \\ \frac{1}{C_o} & 0 & 0 & 0 & \frac{-1}{C_o} \\ 0 & 0 & \frac{-1}{C_{f1}(r_{b1}+r_{Cf1})} & 0 & 0 \\ \frac{r_{b2}}{C_{f2}(r_{b2}+r_{Cf2})} & 0 & 0 & \frac{-1}{C_{f2}(r_{b2}+r_{Cf2})} & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{C.159}$$

$$\mathbf{B}_{(7)} = \begin{bmatrix} \frac{1}{L_o} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{C.160}$$

## Switching State 8

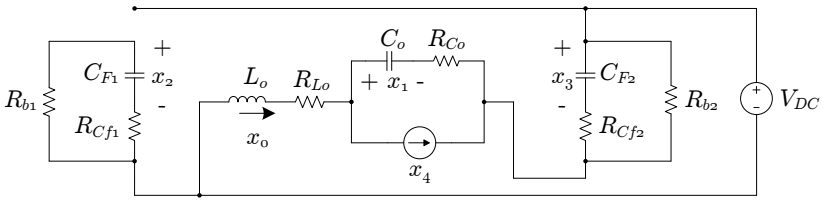



Figure C.23: Schematic circuit diagram of switching state 8 when $T_4$(on), $T_3$(off), $T_2$(off), $T_1$(off).

The five unique differential equations that describe this switching state is

$$0 = L_o\dot{x}_0 + r_{L_o}x_0 + x_1 + r_{C_o}C_o\dot{x}_1 - x_3 - r_{C_{f2}}C_{f2}\dot{x}_3 + V_{DC} \tag{C.161}$$

$$0 = C_{f1}\dot{x}_2 + \frac{1}{r_{b1}}\left(x_2 + r_{C_{f1}}C_{f1}\dot{x}_2\right) \tag{C.162}$$

$$0 = x_0 + C_{f2}\dot{x}_3 + \frac{1}{r_{b2}}\left(x_3 + r_{C_{f2}}C_{f2}\dot{x}_3\right) \tag{C.163}$$

$$0 = x_0 - C_0\dot{x}_1 - x_4 \tag{C.164}$$

$$0 = \dot{x}_4. \tag{C.165}$$

Simultaneously solving the five equations for

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}V_{DC} \tag{C.166}$$

then the $\mathbf{A}$ and $\mathbf{B}$ matrices for switching state 8 becomes

$$\mathbf{A}_{(8)} = \begin{bmatrix} \frac{-r_{b2}r_{C_{f2}}}{L_o(r_{b2}+r_{C_{f2}})} - \frac{r_{C_o}}{L_o} - \frac{r_{L_o}}{L_o} & \frac{-1}{L_o} & 0 & \frac{-r_{C_{f2}}}{L_o(r_{b2}+r_{C_{f2}})} + \frac{1}{L_o} & \frac{r_{C_o}}{L_o} \\ \frac{1}{C_o} & 0 & 0 & 0 & \frac{-1}{C_o} \\ 0 & 0 & \frac{-1}{C_{f1}(r_{b1}+r_{C_{f1}})} & 0 & 0 \\ \frac{-r_{b2}}{C_{f2}(r_{b2}+r_{C_{f2}})} & 0 & 0 & \frac{-1}{C_{f2}(r_{b2}+r_{C_{f2}})} & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{C.167}$$

$$\mathbf{B}_{(8)} = \begin{bmatrix} -\frac{1}{L_o} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{C.168}$$

## Switching State 9

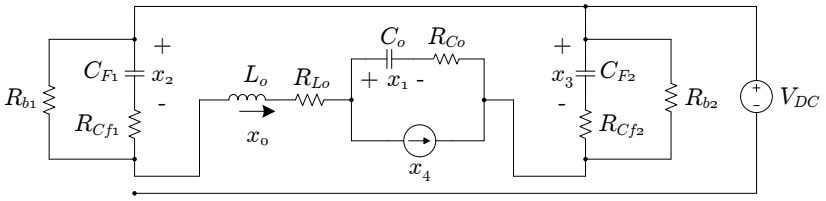



Figure C.24: Schematic circuit diagram of switching state 9 when $T_4$(on), $T_3$(off), $T_2$(off), $T_1$(on).

The five unique differential equations that describe this switching state is

$$0 = L_o\dot{x}_0 + r_{L_o}x_0 + x_1 + r_{C_o}C_o\dot{x}_1 - x_3 - r_{C_{f2}}C_{f2}\dot{x}_3 + x_2 \ + r_{C_{f1}}C_{f1}\dot{x}_2 \tag{C.169}$$

$$0 = x_0 - C_{f1}\dot{x}_2 - \frac{1}{r_{b1}}\left(x_2 + r_{C_{f1}}C_{f1}\dot{x}_2\right) \tag{C.170}$$

$$0 = x_0 + C_{f2}\dot{x}_3 + \frac{1}{r_{b2}}\left(x_3 + r_{C_{f2}}C_{f2}\dot{x}_3\right) \tag{C.171}$$

$$0 = x_0 - C_0\dot{x}_1 - x_4 \tag{C.172}$$

$$0 = \dot{x}_4 \tag{C.173}$$

Simultaneously solving the five equations for

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}V_{DC} \tag{C.174}$$

then the $\mathbf{A}$ and $\mathbf{B}$ matrices for switching state 9 becomes

$$\mathbf{A}_{(9)} = \begin{bmatrix} \frac{-r_{b1}r_{C_{f1}}}{L_o(r_{b1}+r_{C_{f1}})} - \frac{r_{b2}r_{C_{f2}}}{L_o(r_{b2}+r_{C_{f2}})} - \frac{r_{C_o}}{L_o} - \frac{r_{L_o}}{L_o} & \frac{-1}{L_o} & \frac{r_{C_{f1}}}{L_o(r_{b1}+r_{C_{f1}})} - \frac{1}{L_o} & \frac{-r_{C_{f2}}}{L_o(r_{b2}+r_{C_{f2}})} + \frac{1}{L_o} & \frac{r_{C_o}}{L_o} \\ \frac{1}{C_o} & 0 & 0 & 0 & \frac{-1}{C_o} \\ \frac{r_{b1}}{C_{f1}(r_{b1}+r_{C_{f1}})} & 0 & \frac{-1}{C_{f1}(r_{b1}+r_{C_{f1}})} & 0 & 0 \\ \frac{-r_{b2}}{C_{f2}(r_{b2}+r_{C_{f2}})} & 0 & 0 & \frac{-1}{C_{f2}(r_{b2}+r_{C_{f2}})} & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{C.175}$$

$$\mathbf{B}_{(9)} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{C.176}$$

## Switching State 10

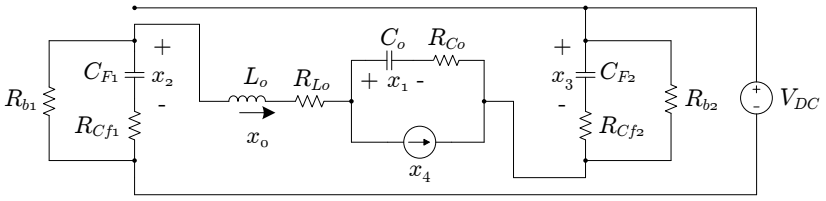



Figure C.25: Schematic circuit diagram of switching state 10 when $T_4$(on), $T_3$(off), $T_2$(on), $T_1$(off).

The five unique differential equations that describe this switching state is

$$0 = L_o\dot{x}_0 + r_{L_o}x_0 + x_1 + r_{C_o}C_o\dot{x}_1 - x_3 - r_{C_{f2}}C_{f2}\dot{x}_3 + V_{DC} - x_2 - r_{C_{f1}}C_{f1}\dot{x}_2 \tag{C.177}$$

$$0 = x_0 + C_{f1}\dot{x}_2 + \frac{1}{r_{b1}}\left(x_2 + r_{C_{f1}}C_{f1}\dot{x}_2\right) \tag{C.178}$$

$$0 = x_0 + C_{f2}\dot{x}_3 + \frac{1}{r_{b2}}\left(x_3 + r_{C_{f2}}C_{f2}\dot{x}_3\right) \tag{C.179}$$

$$0 = x_0 - C_0\dot{x}_1 - x_4 \tag{C.180}$$

$$0 = \dot{x}_4 \tag{C.181}$$

Simultaneously solving the five equations for

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}V_{DC} \tag{C.182}$$

then the $\mathbf{A}$ and $\mathbf{B}$ matrices for switching state 10 becomes

$$\mathbf{A}_{(10)} = \begin{bmatrix} \frac{-r_{b1}r_{C_{f1}}}{L_o(r_{b1}+r_{C_{f1}})} - \frac{r_{b2}r_{C_{f2}}}{L_o(r_{b2}+r_{C_{f2}})} - \frac{r_{C_o}}{L_o} - \frac{r_{L_o}}{L_o} & \frac{-1}{L_o} & \frac{-r_{C_{f1}}}{L_o(r_{b1}+r_{C_{f1}})} + \frac{1}{L_o} & \frac{-r_{C_{f2}}}{L_o(r_{b2}+r_{C_{f2}})} + \frac{1}{L_o} & \frac{r_{C_o}}{L_o} \\ \frac{1}{C_o} & 0 & 0 & 0 & \frac{-1}{C_o} \\ \frac{-r_{b1}}{C_{f1}(r_{b1}+r_{C_{f1}})} & 0 & \frac{-1}{C_{f1}(r_{b1}+r_{C_{f1}})} & 0 & 0 \\ \frac{-r_{b2}}{C_{f2}(r_{b2}+r_{C_{f2}})} & 0 & 0 & \frac{-1}{C_{f2}(r_{b2}+r_{C_{f2}})} & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{C.183}$$

$$\mathbf{B}_{(10)} = \begin{bmatrix} -\frac{1}{L_o} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{C.184}$$

## Switching State 11

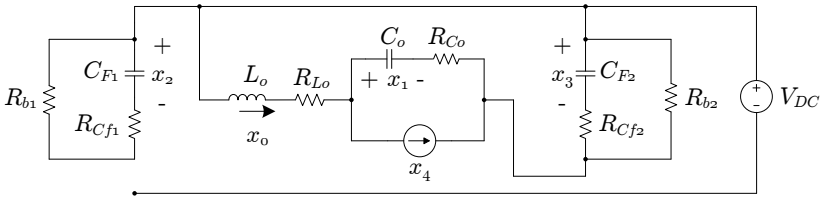



Figure C.26: Schematic circuit diagram of switching state 11 when $T_4$(on), $T_3$(off), $T_2$(on), $T_1$(on).

The five unique differential equations that describe this switching state is

$$0 = L_o\dot{x}_0 + r_{L_o}x_0 + x_1 + r_{C_o}C_o\dot{x}_1 - x_3 - r_{C_{f2}}C_{f2}\dot{x}_3 \tag{C.185}$$

$$0 = C_{f1}\dot{x}_2 + \frac{1}{r_{b1}}\left(x_2 + r_{C_{f1}}C_{f1}\dot{x}_2\right) \tag{C.186}$$

$$0 = x_0 + C_{f2}\dot{x}_3 + \frac{1}{r_{b2}}\left(x_3 + r_{C_{f2}}C_{f2}\dot{x}_3\right) \tag{C.187}$$

$$0 = x_0 - C_0\dot{x}_1 - x_4 \tag{C.188}$$

$$0 = \dot{x}_4. \tag{C.189}$$

Simultaneously solving the five equations for

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}V_{DC} \tag{C.190}$$

then the $\mathbf{A}$ and $\mathbf{B}$ matrices for switching state 11 becomes

$$\mathbf{A}_{(11)} = \begin{bmatrix} \frac{-r_{b2}r_{C_{f2}}}{L_o(r_{b2}+r_{C_{f2}})} - \frac{r_{C_o}}{L_o} - \frac{r_{L_o}}{L_o} & \frac{-1}{L_o} & 0 & \frac{-r_{C_{f2}}}{L_o(r_{b2}+r_{C_{f2}})} + \frac{1}{L_o} & \frac{r_{C_o}}{L_o} \\ \frac{1}{C_o} & 0 & 0 & 0 & \frac{-1}{C_o} \\ 0 & 0 & \frac{-1}{C_{f1}(r_{b1}+r_{C_{f1}})} & 0 & 0 \\ \frac{-r_{b2}}{C_{f2}(r_{b2}+r_{C_{f2}})} & 0 & 0 & \frac{-1}{C_{f2}(r_{b2}+r_{C_{f2}})} & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{C.191}$$

$$\mathbf{B}_{(11)} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{C.192}$$

## Switching State 12

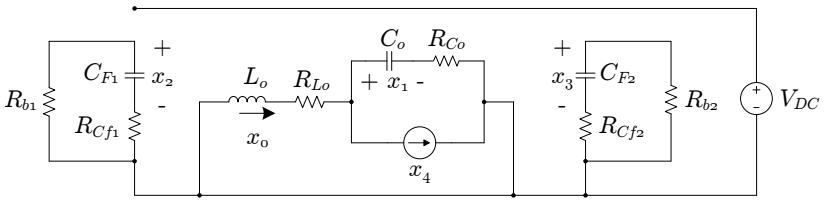



Figure C.27: Schematic circuit diagram of switching state 12 when $T_4$(on), $T_3$(on), $T_2$(off), $T_1$(off).

The five unique differential equations that describe this switching state is

$$0 = L_o\dot{x}_0 + r_{L_o}x_0 + x_1 + r_{C_o}C_o\dot{x}_1 \tag{C.193}$$

$$0 = C_{f1}\dot{x}_2 + \frac{1}{r_{b1}}\left(x_2 + r_{C_{f1}}C_{f1}\dot{x}_2\right) \tag{C.194}$$

$$0 = C_{f2}\dot{x}_3 + \frac{1}{r_{b2}}\left(x_3 + r_{C_{f2}}C_{f2}\dot{x}_3\right) \tag{C.195}$$

$$0 = x_0 - C_0\dot{x}_1 - x_4 \tag{C.196}$$

$$0 = \dot{x}_4. \tag{C.197}$$

Simultaneously solving the five equations for

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}V_{DC} \tag{C.198}$$

then the $\mathbf{A}$ and $\mathbf{B}$ matrices for switching state 12 becomes

$$\mathbf{A}_{(12)} = \begin{bmatrix} \frac{(-r_{C_o}-r_{L_o})}{L_o} & \frac{-1}{L_o} & 0 & 0 & \frac{r_{C_o}}{L_o} \\ \frac{1}{C_o} & 0 & 0 & 0 & \frac{-1}{C_o} \\ 0 & 0 & \frac{-1}{C_{f1}(r_{b1}+r_{C_{f1}})} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{C_{f2}(r_{b2}+r_{C_{f2}})} & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{C.199}$$

$$\mathbf{B}_{(12)} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{C.200}$$

## Switching State 13

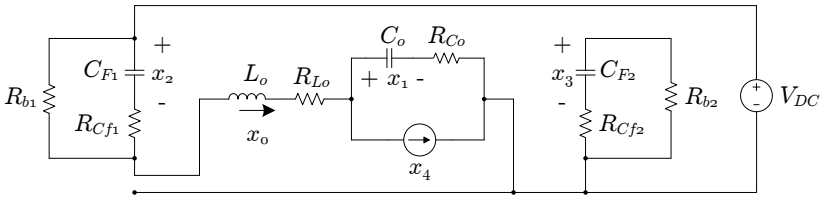



Figure C.28: Schematic circuit diagram of switching state 13 when $T_4$(on), $T_3$(on), $T_2$(off), $T_1$(on).

The five unique differential equations that describe this switching state is

$$0 = L_o\dot{x}_0 + r_{L_o}x_0 + x_1 + r_{C_o}C_o\dot{x}_1 - V_{DC} + x_2 \ + r_{C_{f1}}C_{f1}\dot{x}_2 \tag{C.201}$$

$$0 = x_0 - C_{f1}\dot{x}_2 - \frac{1}{r_{b1}}\left(x_2 + r_{C_{f1}}C_{f1}\dot{x}_2\right) \tag{C.202}$$

$$0 = C_{f2}\dot{x}_3 + \frac{1}{r_{b2}}\left(x_3 + r_{C_{f2}}C_{f2}\dot{x}_3\right) \tag{C.203}$$

$$0 = x_0 - C_0\dot{x}_1 - x_4 \tag{C.204}$$

$$0 = \dot{x}_4. \tag{C.205}$$

Simultaneously solving the five equations for

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}V_{DC} \tag{C.206}$$

then the $\mathbf{A}$ and $\mathbf{B}$ matrices for switching state 13 becomes

$$\mathbf{A}_{(13)} = \begin{bmatrix} \frac{-r_{b1}r_{C_{f1}}}{L_o(r_{b1}+r_{C_{f1}})} - \frac{r_{C_o}}{L_o} - \frac{r_{L_o}}{L_o} & \frac{-1}{L_o} & \frac{r_{C_{f1}}}{L_o(r_{b1}+r_{C_{f1}})} - \frac{1}{L_o} & 0 & \frac{r_{C_o}}{L_o} \\ \frac{1}{C_o} & 0 & 0 & 0 & \frac{-1}{C_o} \\ \frac{r_{b1}}{C_{f1}(r_{b1}+r_{C_{f1}})} & 0 & \frac{-1}{C_{f1}(r_{b1}+r_{C_{f1}})} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{C_{f2}(r_{b2}+r_{C_{f2}})} & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{C.207}$$

$$\mathbf{B}_{(13)} = \begin{bmatrix} \frac{1}{L_o} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{C.208}$$

## Switching State 14

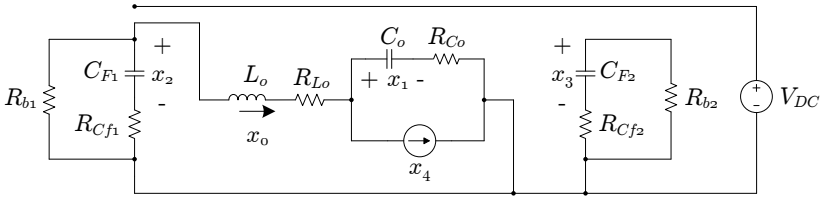



Figure C.29: Schematic circuit diagram of switching state 14 when $T_4$(on), $T_3$(on), $T_2$(on), $T_1$(off).

The five unique differential equations that describe this switching state is

$$0 = L_o\dot{x}_0 + r_{L_o}x_0 + x_1 + r_{C_o}C_o\dot{x}_1 - x_2 \; - r_{C_{f1}}C_{f1}\dot{x}_2 \tag{C.209}$$

$$0 = x_0 + C_{f1}\dot{x}_2 + \frac{1}{r_{b1}}\left(x_2 + r_{C_{f1}}C_{f1}\dot{x}_2\right) \tag{C.210}$$

$$0 = C_{f2}\dot{x}_3 + \frac{1}{r_{b2}}\left(x_3 + r_{C_{f2}}C_{f2}\dot{x}_3\right) \tag{C.211}$$

$$0 = x_0 - C_0\dot{x}_1 - x_4 \tag{C.212}$$

$$0 = \dot{x}_4. \tag{C.213}$$

Simultaneously solving the five equations for

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}V_{DC} \tag{C.214}$$

then the $\mathbf{A}$ and $\mathbf{B}$ matrices for switching state 14 becomes

$$\mathbf{A}_{(14)} = \begin{bmatrix} \frac{-r_{b1}r_{C_{f1}}}{L_o(r_{b1}+r_{C_{f1}})} - \frac{r_{C_o}}{L_o} - \frac{r_{L_o}}{L_o} & \frac{-1}{L_o} & \frac{-r_{C_{f1}}}{L_o(r_{b1}+r_{C_{f1}})} + \frac{1}{L_o} & 0 & \frac{r_{C_o}}{L_o} \\ \frac{1}{C_o} & 0 & 0 & 0 & \frac{-1}{C_o} \\ \frac{-r_{b1}}{C_{f1}(r_{b1}+r_{C_{f1}})} & 0 & \frac{-1}{C_{f1}(r_{b1}+r_{C_{f1}})} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{C_{f2}(r_{b2}+r_{C_{f2}})} & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{C.215}$$

$$\mathbf{B}_{(14)} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{C.216}$$

## Switching State 15

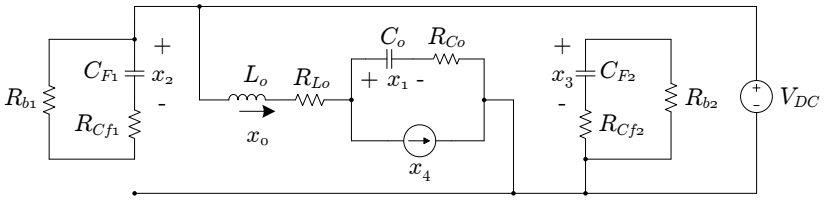



Figure C.30: Schematic circuit diagram of switching state 15 when $T_4$(on), $T_3$(on), $T_2$(on), $T_1$(on).

The five unique differential equations that describe this switching state is

$$0 = L_o\dot{x}_0 + r_{L_o}x_0 + x_1 + r_{C_o}C_o\dot{x}_1 - V_{DC} \tag{C.217}$$

$$0 = C_{f1}\dot{x}_2 + \frac{1}{r_{b1}}\left(x_2 + r_{C_{f1}}C_{f1}\dot{x}_2\right) \tag{C.218}$$

$$0 = C_{f2}\dot{x}_3 + \frac{1}{r_{b2}}\left(x_3 + r_{C_{f2}}C_{f2}\dot{x}_3\right) \tag{C.219}$$

$$0 = x_0 - C_0\dot{x}_1 - x_4 \tag{C.220}$$

$$0 = \dot{x}_4. \tag{C.221}$$

Simultaneously solving the five equations for

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}V_{DC} \tag{C.222}$$

then the $\mathbf{A}$ and $\mathbf{B}$ matrices for switching state 15 becomes

$$\mathbf{A}_{(15)} = \begin{bmatrix} \frac{(-r_{C_o}-r_{L_o})}{L_o} & \frac{-1}{L_o} & 0 & 0 & \frac{r_{C_o}}{L_o} \\ \frac{1}{C_o} & 0 & 0 & 0 & \frac{-1}{C_o} \\ 0 & 0 & \frac{-1}{C_{f1}(r_{b1}+r_{C_{f1}})} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{C_{f2}(r_{b2}+r_{C_{f2}})} & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{C.223}$$

$$\mathbf{B}_{(15)} = \begin{bmatrix} \frac{1}{L_o} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{C.224}$$

# Bibliography

[1] Mouton, T., de Beer, A., Putzeys, B. and McGrath, B.: Modelling and design of single-edge oversampled pwm current regulators using z-domain methods. In: *ECCE Asia Downunder (ECCE Asia), 2013 IEEE*, pp. 31–37. June 2013.

[2] Mouton, T., Stolze, P., Geyer, T., Tomlinson, M. and Kennel, R.: Predictive control vs. linear control for current control of a single-leg inverter. In: *Sensorless Control for Electrical Drives and Predictive Control of Electrical Drives and Power Electronics (SLED/PRECEDE), 2013 IEEE International Symposium on*, pp. 1–8. Oct 2013.

[3] Data sheet: Skmt 92, skkl 92, semikron. .

[4] Rodriguez, J. and Cortes, P.: *Predictive Control of Power Converters and Electrical Drives*. 1st edn. John Wiley & Sons, Ltd., 2012.

[5] Buso, S. and Mattavelli, P.: *Digital Control in Power Electronics*. 1st edn. Morgan & Claypool, 2006.

[6] Takahashi, I. and Noguchi, T.: A new quick-response and high-efficiency control strategy of an induction motor. *Industry Applications, IEEE Transactions on*, vol. IA-22, no. 5, pp. 820–827, Sept 1986. ISSN 0093-9994.

[7] Ohnishi, T.: Three phase pwm converter/inverter by means of instantaneous active and reactive power control. In: *Industrial Electronics, Control and Instrumentation, 1991. Proceedings. IECON '91., 1991 International Conference on*, pp. 819–824 vol.1. Oct 1991.

[8] Mohan, N.: *Power electronics: converters, applications, and design*. John Wiley & Sons, Hoboken, NJ, 2003. ISBN 9780471226932.

[9] Holmes, D.G. and Lipo, T.A.: *Pulse Width Modulation for Power Converters: Principles and Practice*. IEEE press series on power engineering. Piscataway IEEE Press, 2003.

[10] Middlebrook, R. and Cuk, S.: A general unified approach to modelling switching-converter power stages. In: *Power Electronics Specialists Conference, 1970 IEEE*, pp. 18–34. April 1976. ISSN 0275-9306.

[11] Kazmierkowski, M. and Malesani, L.: Current control techniques for three-phase voltage-source pwm converters: a survey. *Industrial Electronics, IEEE Transactions on*, vol. 45, no. 5, pp. 691–703, Oct 1998. ISSN 0278-0046.

[12] Blaschke, F.: The principle of field-orientation applied to transvector closed-loop control system for a rotating field machine. In: *Siemens Review*, vol. XXXIX, pp. 217–220. 1972.

[13] Tan, S.-C., Lai, Y., Tse, C. and Cheung, M.: A fixed-frequency pulsewidth modulation based quasi-sliding-mode controller for buck converters. *Power Electronics, IEEE Transactions on*, vol. 20, no. 6, pp. 1379–1392, Nov 2005. ISSN 0885-8993.

[14] Sira-Ramirez, H. and Silva-Ortigoza., R.: *Control Design Techniques in Power Electronics Devices*. Springer, 2006.

[15] Mattavelli, P. and Spiazzi, G.: *The Power Electronics Handbook: Industrial Electronics Series*. CRC Press, 2002.

[16] Abrie, D.: *Supervisory control and sliding-mode control of a direct AC-AC medium-voltage voltage regulator*. Master's thesis, Stellenbosch University, 2012.

[17] Utkin., V.I.: *Sliding Modes in Control Opitmization*. Springer-Verlag, 1992. Translated from1981Russian language edition.

[18] Edwards, S. and Spurgeon, C.: *Sliding Mode Control - Theory and Applications*. Taylor & Francis Group, 1998.

[19] Cortés, P., Kazmierkowski, M.P., Kennel, R.M., Quevedo, D.E. and Rodríguez, J.: Predictive control in power electronics and drives. *Industrial Electronics, IEEE Transactions on*, vol. 55, no. 12, pp. 4312 –4324, Dec 2008. ISSN 0278-0046.

[20] Morari, M. and Lee, J.H.: Model predictive control: Past, present and future. *Computers and Chemical Engineering*, vol. 23, no. 4-5, pp. 667–682, August 1999.

[21] Linder, A., Kanchan, R., Kennel, R. and Stolze, P.: *Model-Based Predictive Control of Electric Drives*. Cuvillier Verlag Göttingen, June 2010.

[22] Vázquez, S., Leon, J., Franquelo, L., Rodriguez, J., Young, H., Marquez, A. and Zanchetta, P.: Model predictive control: A review of its applications in power electronics. *Industrial Electronics Magazine, IEEE*, vol. 8, no. 1, pp. 16–31, March 2014. ISSN 1932-4529.

[23] Rodriguez, J., Cortes, P., Kennel, R. and Kazmierkowski, M.: Model predictive control – a simple and powerful method to control power converters. In: *Power Electronics and Motion Control Conference, 2009. IPEMC '09. IEEE 6th International*, pp. 41 –49. may 2009.

[24] Stolze, P., Kramkowski, M., Mouton, T., Tomlinson, M. and Kennel, R.: Increasing the performance of finite-set model predictive control by oversampling. In: *Industrial Technology (ICIT), 2013 IEEE International Conference on*, pp. 551–556. Feb 2013.

[25] Linder, A. and Kennel, R.: Direct model predictive control - a new direct predictive control strategy for electrical drives. In: *Power Electronics and Applications, 2005 European Conference on*, pp. 10 pp.–P.10. 2005.

[26] Rodríguez, J., Pontt, J., Cortés, P. and Vargas, R.: Predictive control of a three-phase neutral point clamped inverter. In: *Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th*, pp. 1364 –1369. June 2005.

[27] Vargas, R., Rodriguez, J., Ammann, U. and Wheeler, P.: Predictive current control of an induction machine fed by a matrix converter with reactive power control. *Industrial Electronics, IEEE Transactions on*, vol. 55, no. 12, pp. 4362–4371, Dec 2008. ISSN 0278-0046.

[28] Dang, H., Wheeler, P. and Clare, J.: A control analysis and implementation of high voltage, high frequency direct power converter. In: *IEEE Industrial Electronics, IECON 2006 - 32nd Annual Conference on*, pp. 2096–2102. Nov 2006. ISSN 1553-572X.

[29] Catucci, M., Clare, J. and Wheeler, P.: Predective control strategy for zcs single stage resonant converter. In: *IEEE Industrial Electronics, IECON 2006 - 32nd Annual Conference on*, pp. 2905–2910. Nov 2006. ISSN 1553-572X.

[30] Catucci, M., Clare, J. and Wheeler, P.: Predictive control strategies for zcs direct converter hv power supply. In: *Power Electronics and Applications, 2005 European Conference on*, pp. 10 pp.–P.10. 2005.

[31] Silva, E., McGrath, B., Quevedo, D. and Goodwin, G.: Predictive control of a flying capacitor converter. In: *American Control Conference, 2007. ACC '07*, pp. 3763–3768. July 2007. ISSN 0743-1619.

[32] Stolze, P., du Toit, D., Tomlinson, M., Kennel, R. and Mouton, T.: Model predictive control of a flying capacitor converter with output lc filter for ups applications. In: *AFRICON, 2011*, pp. 1–6. Sept 2011. ISSN 2153-0025.

[33] Stolze, P., du Toit, D., Tomlinson, M., Kennel, R. and Mouton, T.: Predictive torque control of an induction machine fed by a flying capacitor converter. In: *AFRICON, 2011*, pp. 1–6. Sept 2011. ISSN 2153-0025.

[34] Stolze, P., Landsmann, P., Kennel, R. and Mouton, T.: Finite-set model predictive control of a flying capacitor converter with heuristic voltage vector preselection. In: *Power Electronics and ECCE Asia (ICPE ECCE), 2011 IEEE 8th International Conference on*, pp. 210–217. May 2011. ISSN 2150-6078.

[35] du Toit, D., Mouton, H., Kennel, R. and Stolze, P.: Predictive control of series stacked flying-capacitor active rectifiers. *Industrial Informatics, IEEE Transactions on*, vol. 9, no. 2, pp. 697–707, May 2013. ISSN 1551-3203.

[36] Tomlinson, M., Mouton, T., Kennel, R. and Stolze, P.: Model predictive control with a fixed switching frequency for a 5-level flying capacitor converter. In: *ECCE Asia Downunder (ECCE Asia), 2013 IEEE*, pp. 1208–1214. June 2013.

[37] Tomlinson, M., Mouton, T., Kennel, R. and Stolze, P.: A generic approach to implementing finite-set model predictive control with a fixed switching frequency. In: *Industrial Electronics (ISIE), 2014 IEEE 23rd International Symposium on*, pp. 330–335. June 2014.

[38] Cortés, P., Rodríguez, J., Alepuz, S., Busquets-Monge, S. and Bordonau, J.: Finite-state model predictive control of a four-level diode-clamped inverter. In: *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, pp. 2203 –2208. June 2008. ISSN 0275-9306.

[39] Cortes, P., Rodriguez, J., Antoniewicz, P. and Kazmierkowski, M.: Direct power control of an afe using predictive control. *Power Electronics, IEEE Transactions on*, vol. 23, no. 5, pp. 2516–2523, Sept 2008. ISSN 0885-8993.

[40] Stolze, P., Bauer, F., Landsmann, P., Kennel, R. and Mouton, T.: Predictive torque control of an induction machine fed by a neutral point clamped inverter. In: *Predictive Control of Electrical Drives and Power Electronics (PRECEDE), 2011 Workshop on*, pp. 24–29. Oct 2011.

[41] Stolze, P., Karamanakos, P., Tomlinson, M., Kennel, R., Mouton, T. and Manias, S.: Heuristic variable switching point predictive current control for the three-level neutral point clamped inverter. In: *Sensorless Control for Electrical Drives and Predictive Control of Electrical Drives and Power Electronics (SLED/PRECEDE), 2013 IEEE International Symposium on*, pp. 1–8. Oct 2013.

[42] Rodriguez, J., Pontt, J., Correa, P., Lezana, P. and Cortes, P.: Predictive power control of an ac/dc/ac converter. In: *Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005*, vol. 2, pp. 934–939 Vol. 2. Oct 2005. ISSN 0197-2618.

[43] Rodríguez, J., Pontt, J., Silva, C.A., Correa, P., Lezana, P., Cortés, P. and Ammann, U.: Predictive current control of a voltage source inverter. *Industrial Electronics, IEEE Transactions on*, vol. 54, no. 1, pp. 495 –503, Feb 2007. ISSN 0278-0046.

[44] Cortés, P., Rodríguez, J., Quevedo, D.E. and Silva, C.: Predictive current control strategy with imposed load current spectrum. *Power Electronics, IEEE Transactions on*, vol. 23, no. 2, pp. 612 –618, March 2008. ISSN 0885-8993.

[45] Tomlinson, M., Mouton, T., Kennel, R. and Stolze, P.: Model predictive control with a fixed switching frequency for an ac-to-ac converter. In: *Industrial Technology (ICIT), 2013 IEEE International Conference on*, pp. 570–575. Feb 2013.

[46] Perantzakis, G., Xepapas, F., Papathanassiou, S. and Manias, S.: A predictive current control technique for three-level npc voltage source inverters. In: *Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th*, pp. 1241–1246. June 2005.

[47] Perantzakis, G., Xepapas, F. and Manias, S.: Efficient predictive current control technique for multilevel voltage source inverters. In: *Power Electronics and Applications, 2005 European Conference on*, pp. 10 pp.–P.10. 2005.

[48] Young, H., Perez, M., Rodriguez, J. and Abu-Rub, H.: Assessing finite-control-set model predictive control: A comparison with a linear current controller in two-level voltage source inverters. *Industrial Electronics Magazine, IEEE*, vol. 8, no. 1, pp. 44–52, March 2014. ISSN 1932-4529.

[49] Patsakis, G., Karamanakos, P., Stolze, P., Manias, S., Kennel, R. and Mouton, T.: Variable switching point predictive torque control for the four-switch three-phase inverter. In: *Sensorless Control for Electrical Drives and Predictive Control of Electrical Drives and Power Electronics (SLED/PRECEDE), 2013 IEEE International Symposium on*, pp. 1–8. Oct 2013.

[50] Fuentes, E., Silva, C., Quevedo, D. and Silva, E.: Predictive speed control of a synchronous permanent magnet motor. In: *Industrial Technology, 2009. ICIT 2009. IEEE International Conference on*, pp. 1–6. Feb 2009.

[51] Cortés, P., Ortiz, G., Yuz, J.I., Rodríguez, J., Vazquez, S. and Franquelo, L.G.: Model predictive control of an inverter with output LC filter for UPS applications. *Industrial Electronics, IEEE Transactions on*, vol. 56, no. 6, pp. 1875 –1883, June 2009. ISSN 0278-0046.

[52] Karamanakos, P., Geyer, T., Oikonomou, N., Kieferndorf, F. and Manias, S.: Direct model predictive control: A review of strategies that achieve long prediction intervals for power electronics. *Industrial Electronics Magazine, IEEE*, vol. 8, no. 1, pp. 32–43, March 2014. ISSN 1932-4529.

[53] Cagienard, R., Grieder, P., Kerrigan, E. and Morari, M.: Move blocking strategies in receding horizon control. In: *Decision and Control, 2004. CDC. 43rd IEEE Conference on*, vol. 2, pp. 2023–2028 Vol.2. Dec 2004. ISSN 0191-2216.

[54] Geyer, T., Papafotiou, G. and Morari, M.: Model predictive direct torque control-part i: Concept, algorithm, and analysis. *Industrial Electronics, IEEE Transactions on*, vol. 56, no. 6, pp. 1894–1905, June 2009. ISSN 0278-0046.

[55] Papafotiou, G., Kley, J., Papadopoulos, K., Bohren, P. and Morari, M.: Model predictive direct torque control-part ii: Implementation and experimental evaluation. *Industrial Electronics, IEEE Transactions on*, vol. 56, no. 6, pp. 1906–1915, June 2009. ISSN 0278-0046.

[56] Geyer, T.: Generalized model predictive direct torque control: Long prediction horizons and minimization of switching losses. In: *Decision and Control, 2009 held jointly with the 2009 28th Chinese Control Conference. CDC/CCC 2009. Proceedings of the 48th IEEE Conference on*, pp. 6799–6804. Dec 2009. ISSN 0191-2216.

[57] Geyer, T., Oikonomou, N., Papafotiou, G. and Kieferndorf, F.: Model predictive pulse pattern control. *Industry Applications, IEEE Transactions on*, vol. 48, no. 2, pp. 663–676, March 2012. ISSN 0093-9994.

[58] Aurtenechea, S., Rodriguez, M., Oyarbide, E. and Torrealday, J.: Predictive direct power control - a new control strategy for dc/ac converters. In: *IEEE Industrial Electronics, IECON 2006 - 32nd Annual Conference on*, pp. 1661–1666. Nov 2006. ISSN 1553-572X.

[59] Larrinaga, S., Vidal, M., Oyarbide, E. and Apraiz, J.: Predictive control strategy for dc/ac converters based on direct power control. *Industrial Electronics, IEEE Transactions on*, vol. 54, no. 3, pp. 1261–1271, June 2007. ISSN 0278-0046.

[60] Pacas, M. and Weber, J.: Predictive direct torque control for the pm synchronous machine. *Industrial Electronics, IEEE Transactions on*, vol. 52, no. 5, pp. 1350–1356, Oct 2005. ISSN 0278-0046.

[61] Gopal, M.: *Digital control and state variable methods: conventional and neural-fuzzy*. Tata McGraw-Hill Publishing Company, 2009.

[62] du Toit, D.: *Predictive Control of a Series-Input, Parallel-Output, Back-to-Back, Flying-Capacitor Multilevel Converter*. Master's thesis, Stellenbosch University, 2011.

[63] Schafmeister, F., Rytz, C. and Kolar, J.: Analytical calculation of the conduction and switching losses of the conventional matrix converter and the (very) sparse matrix converter. In: *Applied Power Electronics Conference and Exposition, 2005. APEC 2005. Twentieth Annual IEEE*, vol. 2, pp. 875–881 Vol. 2. March 2005.

[64] Kouro, S., La Rocca, B., Cortes, P., Alepuz, S., Wu, B. and Rodriguez, J.: Predictive control based selective harmonic elimination with low switching frequency for multilevel converters. In: *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*, pp. 3130–3136. Sept 2009.

[65] Thielemans, S.: *Balancing and Control of Power Electronic Flying Capacitor Multilevel Converters*. Ph.D. thesis, Universiteit Gent, 2012.

[66] Tomlinson, M., Mouton, T., Kennel, R. and Stolze, P.: Model predictive control of an AC-to-AC converter with input and output LC filter. In: *Industrial Electronics and Applications (ICIEA), 2011 6th IEEE Conference on*, pp. 1233 –1238. June 2011. ISSN pending.

[67] Vázquez, S., Leon, J., Franquelo, L., Carrasco, J., Martínez, O., Rodríguez, J., Cortés, P. and Kouro, S.: Model predictive control with constant switching frequency using a discrete space vector modulation with virtual state vectors. In: *Industrial Technology, 2009. ICIT 2009. IEEE International Conference on*, pp. 1 –6. Feb 2009.

[68] Mouton, T. and Putzeys, B.: Digital control of a PWM switching amplifier with global feedback. In: *Audio Engineering Society Conference: 37th International Conference: Class D Audio Amplification*. 2009.
Available at: `http://www.aes.org/e-lib/browse.cfm?elib=15218`

[69] Pérez, M.A., Cortés, P. and Rodríguez, J.: Predictive control algorithm technique for multilevel asymmetric cascaded H-bridge inverters. *Industrial Electronics, IEEE Transactions on*, vol. 55, no. 12, pp. 4354 –4361, Dec 2008. ISSN 0278-0046.

[70] Schröder, D.: Predictive control strategies for converter and inverter. In: *Industrial Technology, 2009. ICIT 2009. IEEE International Conference on*, pp. 1 –8. Feb 2009.

[71] Nye, J.: *Increasing distributed generation penetration when limited by voltage regulation.* Master's thesis, Stellenbosch University, 2014.

[72] Fourie, R. and du T. Mouton, H.: Development of a mv igbt based solid-state tap changer. *AFRICON, 2009*, vol. 1, pp. 1–6, September 2009.

[73] Fourie, R.: *The Development of a IGBT-based Tap Changer.* Master's thesis, Universiteit van Stellenbosch, Stellenbosch, South Africa, 2009.

[74] Tomlinson, M., Abrie, D. and Mouton, T.: Series-stacked medium voltage electronic voltage regulator. In: *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, pp. 1087 –1093. Sept 2011.

[75] Geyer, T., Oikonomou, N., Papafotiou, G. and Kieferndorf, F.: Model predictive pulse pattern control. *Industry Applications, IEEE Transactions on*, vol. 48, no. 2, pp. 663–676, March 2012. ISSN 0093-9994.

[76] Brown, S. and Vranesic, Z.: *Fundamentals of digital logic with VHDL design.* McGraw-Hill, 2005.

[77] Electricity supply - quality of supply part 2: Voltage characteristics, compatibility levels, limits and assessment methods.

[78] Winders, J.: *Power transformers: principles and applications.* Marcel Dekker, New York, 2002. ISBN 0824707664.

[79] van Schalkwyk, C.: *Analysis and design of a voltage regulator based on an AC-to-AC converter.* Master's thesis, Universiteit van Stellenbosch, Stellenbosch, South Africa, 2003.

[80] Meynard, T. and Lefeuvre, E.: Cutting electric power converter. March 2002.

[81] Bauer, P. and de Haan, S.: Electronic tap changer for 500 kVa/10 kv distribution transformers: design, experimental results and impact in distribution networks. In: *Industry Applications Conference, 1998. Thirty-Third IAS Annual Meeting. The 1998 IEEE*, vol. 2, pp. 1530 –1537 vol.2. Oct 1998. ISSN 0197-2618.

[82] Bauer, P. and De Haan, S.: Solid state tap changers for utility transformers. In: *Africon, 1999 IEEE*, vol. 2, pp. 897 –902 vol.2. 1999.

[83] Lawatsch, H. and Vitins, J.: Protection of thyristors against overvoltage with breakover diodes. *Industry Applications, IEEE Transactions on*, vol. 24, no. 3, pp. 444 –448, may/jun 1988. ISSN 0093-9994.

[84] Data sheet: Ixys breakover diodes, ixys.

[85] Proakis, J.G. and Manolakis, D.G.: *Digital Signal Processing: Principles, Algorithms and Applications*. Pearson Prentice Hall, 2007.

[86] van der Merwe, J.W.: *Natural Balancing Mechanisms in Converters*. Ph.D. thesis, Stellenbosch University, 2011.

[87] Corradini, L., Stefanutti, W. and Mattavelli, P.: Analysis of multi-sampled current control for active filters. In: *Industry Applications Conference, 2007. 42nd IAS Annual Meeting. Conference Record of the 2007 IEEE*, pp. 1608–1615. Sept 2007. ISSN 0197-2618.

[88] Bocker, J. and Buchholz, O.: Can oversampling improve the dynamics of pwm controls? In: *Industrial Technology (ICIT), 2013 IEEE International Conference on*, pp. 1818–1824. Feb 2013.

[89] Risbo, L.: Discrete-time modeling of continuous-time pulse width modulator loops. In: *Audio Engineering Society Conference: 27th International Conference: Efficient Audio Power Amplification*. Sep 2005.
Available at: `http://www.aes.org/e-lib/browse.cfm?elib=13263`

[90] Putzeys, B.: Simple, ultralow distortion digital pulse width modulator. In: *Audio Engineering Society Convention 120*. May 2006.
Available at: `http://www.aes.org/e-lib/browse.cfm?elib=13498`

[91] Goodwin, G., Graebe, S. and Salgado, M.: *Control System Design*. Prentice Hall, 2001. ISBN 9780139586538.

[92] Data sheet: P16 heatsink, semikron.

[93] Data sheet: Sket740, semikron.

[94] Data sheet: Skm150gm12t4g, semikron. .

[95] Neamen, D.A.: *Electronic circuit analysis and design*. 2nd edn. McGraw-Hill, 2001.