The Design and Characterization of Diode Detectors

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Declaration

I, the undersigned, hereby declare that the work contained in this thesis is my own work and has not previously in its entirety or in part been submitted at any university for a degree.

WJC Koen Date

Abstract

The use of diode detectors for power measurement and AM demodulation is not a new subject. The design and characterization of optimum diode detectors can, however, always be improved. In this thesis a step-by-step design procedure is presented for the design of various diode detectors. The design itself is not a complex task, but the success of the results depends on the characterization of both the detector and the diode. A method to extract optimized diode models from DC and small signal measurements are presented. Analyzing the detector circuit with the harmonic balance technique does the characterization of the detector. These results can be used to create an error-correcting algorithm to compensate for the non-linear behavior of diode detectors and to improve the dynamic range and sensitivity of the design.

Opsomming

Die gebruik van diode detektors vir drywingmetings en AM demodulasie is nie 'n nuwe begrip nie. Die ontwerp en karakterisering van optimum diode detektors kan egter altyd verbeter word. 'n Stap-vir-stap prosedure word in hierdie tesis beskryf waarvolgens verskeie detektors ontwerp kan word. Die ontwerp, op sig self, is nie 'n ingewikkelde proses nie, maar die sukses van die detektor hang af van die karakterisering van beide die detektor en die diode. 'n Metode om diode modelle vanuit GS- en kleinseinmetings te onttrek word bespreek. Die karakterisering van die detektor word gedoen deur die baan met die harmonieke balans metode op te los. Hierdie resultate kan gebruik word om 'n algoritme te skep wat kompenseer vir die nie-lineêre gedrag van die detektor. Die dinamiese bereik en sensitiwiteit van die ontwerp kan sodoende verbeter word.

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Contents

List of Figures

List of Tables

Chapter 1

1 Introduction

When diode detectors are under discussion, the subject of the non-linear behavior of semiconductors must receive good attention. The semiconductors can be restricted to diodes, and more specifically Schottky diodes, for this thesis.

The strive for linear responses, or at least a response that can be described mathematically, forces the need for a precise analysis of the device in discussion. In our case the device is the diode detector. To take this statement further: In order to do a precise analysis of diode detectors, the diodes must be accurately characterized. These two subjects form the basis of discussion in this thesis. It is just not good enough to discuss the design of diode detectors for specific applications, without presenting a technique by which its response can be linearised or predicted.

When the response of a diode detector is discussed, there are three performance parameters that are referred to. The first is the response of the voltage detected by the diode detector over varying input power, secondly its response over varying frequency and thirdly for temperature variance.

The aim of the thesis is to present techniques for designing diode detectors up to X-band. Techniques will also be presented for characterizing Schottky diodes over the frequency band it is needed for. The harmonic balance technique, as one method towards describing detector's responses, is implemented. This technique is the first step towards creating an error-correcting algorithm to linearise a detector's response.

The path through this thesis is:

1.1 Microwave diodes

The subject on microwave diodes is a widely discussed topic. The variety of diodes on the market today makes it difficult in deciding what diode to use when. In chapter 2 the subject is discussed theoretically and a few suggestions are made on how to choose the correct diode for an application. The emphasis is laid on detector diodes, which is the subject of discussion, in this thesis. Schottky, PIN, tunnel, Gunn, varactor and IMPATT diodes are under discussion. Schottky diodes, however, excel in the use in detector applications and receive extensive attention.

The small and large signal model of the Schottky diode is used throughout this thesis as a building block for detector design. The importance and reason for the presence of each parameter is underlined, to clarify the behavior of diodes under various conditions.

1.2 Schottky Barrier Diode detectors

If the decision is made on what diode to use, the next step towards the design of detectors is to describe and understand the behavior of the detector circuit (the diode is included in this circuit). In order to do this, there must be decided on a detector topology. The application of the detector is the important player in making this decision. The detector circuit and different topologies are discussed and motivated in chapter 2.

The performance characteristics of the diodes used and procedures to get maximum performance out of them are also discussed. These performance characteristics, expressed in mathematical terms, form the basis of the design procedures and equations presented in chapter 6.

The behavior of detectors under various conditions, for example temperature and high frequency, are also examined to find ways to analyze or compensate for unwanted effects.

1.3 The Characterization of Diodes

Without the proper characterization of the diodes in use, results will be inaccurate. In order to design an optimum detector and also to do an accurate analysis of the circuit, characterization is important.

Techniques to extract the Schottky diode model from DC and small signal measurements are presented. A de-embedding technique, as well as an optimization algorithm, is discussed by which an optimized model can be extracted.

The extraction of the models for the diodes used in this thesis is done over the frequency band it is needed for. These models are extracted for different biasing levels and are used in the design examples discussed in chapter 6.

1.4 The Design of Matching Circuits

Maximum performance can only be obtained from a detector if it is properly matched to the source.

Narrowband, wideband and resistive matching techniques are presented in the form of matching algorithms. The matching is done with the addition of transmission lines and short circuit stubs to the detector circuit.

The relationship between the sensitivity of a detector and the VSWR are also discussed to get an understanding of the dependence of these characteristics on each other.

1.5 The Design of Diode Detectors

With the above-mentioned results and techniques, it is possible to develop an algorithm to design diode detectors. In chapter 6 the design is discussed step-by- step.

User inter-action is, however, still necessary to reach the design specifications. Three different types of detector designs are discussed, namely small signal detectors with maximum sensitivity, small signal detectors with maximum bandwidth and large signal detectors.

Practical design examples are presented for later analysis and measurements in chapter 8.

1.6 Analysis Algorithms

The last step in the detector design procedure is to analyze the designed detector circuit. The techniques and algorithms to do this analysis are discussed in chapter 7.

The first technique is the Ritz-Galerkin method, by which the response of the detector is calculated by the summation of Bessel functions. A more proper analysis technique, the harmonic balance method, is also discussed. The implementation of these techniques is discussed in detail, but the application to the design examples are discussed in chapter 8.

These two techniques can be used to implement a computer-based error-correcting algorithm for diode detectors.

1.7 Simulated Results and Measurements

To verify all the design examples and analysis techniques, it is necessary to compare simulations with other simulation packages as well as with practical measurements.

Various plots are presented to report on the success of all the above mentioned techniques in chapter 8.

Chapter 2

2 Microwave Diodes

Microwave diodes are among the most versatile components in use today – they mix, detect, amplify, oscillate, attenuate, switch, multiply, limit, and shift phase. One will be hard pressed to find any other single type of component that could accomplish all of these functions.

Different kinds of microwave diodes are discussed in this chapter together with their applications and electrical representations. At the end of this chapter a few diodes are selected that will be used in the design examples. The reasons for selecting these diodes are also explained in the following two chapters.

2.1 Schottky Diodes

The Schottky-barrier (or hot carrier) type is a majority carrier – its conduction is by means of a predominant carrier (in this case, electrons, although p-type silicon has holes for majority carriers). The energy, or Schottky barrier exists at the metal to semiconductor interface because of the difference in the work functions of the two materials. The barrier is unaffected by a reverse-bias, but is decreased by a forward bias. This is a familiar characteristic of a rectifying diode. Therefore, when the device is forward biased, the majority carriers can be easily injected from the semiconductor material into the metal, where the energy level is now much higher. Once in the metal, the majority carrier gives up this excess energy in a very short time, after which they become a part of the free electrons of the metal. When reverse biased, the energy level of the barrier is too high for the electrons to overcome and the device does not conduct. These characteristics indicate the Schottky-barrier's potential for being very efficient high frequency mixers and detectors.

Although there is little difference in the theory of operation of both point contact and Schottky-barrier diodes, they differ in the manner by which the rectifying junction is formed. The point contact junction is realized by the pressure contact of a metal whisker against the semiconductor material, establishing a metal-semiconductor rectifying barrier. Instead of the pressure contact, the Schottky-barrier diode has its rectifying barrier formed by a metal contact deposited on the silicon epitaxial layer. This technique achieves a near ideal metal to semiconductor interface. The use of a conductive pad above the junction allows the whisker wire to be thermal-compression bonded, thus eliminating the need for a pressure contact while increasing the mechanical reliability of the device.

To obtain a diode that approaches the ideal junction conversion loss it is necessary to minimize the loss factors R_s, C_j and L_s. The metallic junction (R_j) is shunted by the barrier capacitances. The series resistance (R_s) is a result of the bulk resistivity of the heavily doped silicon substrate. L_s is the inductance of the gold whisker wire that is bonded to the metallized area over the junction and C_p is the case capacitance.

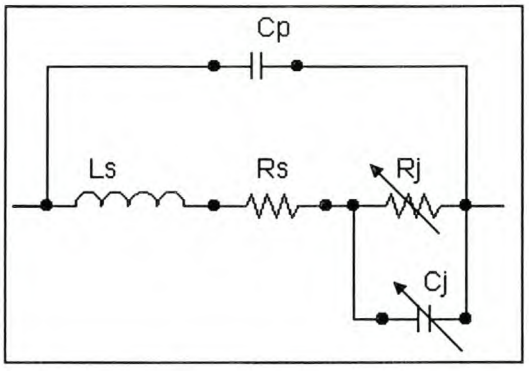


Figure 2-1 The Schottky diode model

Two parameters limit the flow of energy to the barrier. Power can be dissipated in R_s and shorted across the barrier by C_j; however, minimizing both parameters can reduce this dispersion. The RF mismatch caused by L_s and C_p can be eliminated by external matching circuitry. However, it is important to minimize L_s both for its effect on operating bandwidth and on conversion loss. So when looking for a Schottky diode the important things to remember are that R_s, C_j an L_s should always be as low as possible.

Two common but very important applications for the Schottky diode are as mixers and detectors.

Detectors are essentially low sensitivity receivers that function on the basis of direct rectification of the RF signal through the use of a non-linear resistive element – the Schottky diode. Generally detectors can be classified into two distinct types; the small signal type, also known as square-law detectors; and the large signal type, either linear or peak detectors.

The former operation is dependent on the slope and curvature of the I-V characteristic (current-voltage) of the diode in the neighborhood of the bias point. The output of the detector is proportional to the power input to the diode, that is, the output voltage (or current) is proportional to the square of the input voltage.

The large-signal detector operation is dependent on the slope of the I-V characteristic in the linear portion, consequently the diode functions essentially as a switch. In large signal detection, the diode conducts over a portion of the input cycle, and the output current of the diode follows the peaks of the input signal waveform with a linear relationship between the output current and the input voltage.

It can be seen how the characteristics of the Schottky-barrier diode can be used to provide low conversion loss mixers and very efficient detectors. They are far superior to the old point contact diode and can be used in these applications through X-band.

2.2 PIN Diodes

The PIN diode is distinguished from the normal p-n junction type by an area called an intrinsic region, sandwiched between the p-doped and n-doped silicon layers. (Doping is the term used to describe the addition of impurities to a semiconductor material to increase conduction). The intrinsic layer has almost no doping and is consequently a very high resistance. When forward biased is applied across the diode, the conductivity of the layer is increased, creating an electrically variable resistor at microwave frequencies. As the bias current is increased the resistance of the diode decreases, making the PIN diode ideal for use as a variable attenuator.

The parameters that characterize a PIN diode are V_B, C_j, R_s, τ_L and θ_j. The voltage breakdown (V_B) is controlled by the width of the intrinsic layer and directly limits the RF voltage swing that may be applied to the device. C_j is the junction capacitance in the fully depleted state. For most PIN diodes 50 V is enough to fully deplete the intrinsic layer. The capacitance is chosen to be a value compatible with the circuit in which the device is to be used. The device area for a fixed voltage breakdown controls C_j. R_s is the total RF resistance of the device. R_s is usually measured at a frequency of 1 GHz unless otherwise specified. Carrier lifetime (τ_L) influences the resistance of the intrinsic layer and the switching properties of the diode. The thermal resistance (θ_j) indicates the continuous wave power-handling capability of a PIN diode.

Because of the unique properties of the PIN diode, it may be used in the following applications:

- Voltage or current controlled attenuators
- Modulators
- Low and high power switches
- Phase shifters
- Limiters (passive and active)

The basic small signal equivalent circuit of the PIN diode as used in circuit analysis is shown in Fig. 2-2. The circuit consists of an inductance (L_s) in series with R_s and C_j. The inductance is due to the ribbon or wire used to connect the PIN chip. A parasitic capacitance (C_p) caused by the package in which the diode is mounted, shunts both the elements of the chip and the inductance. Another parasitic capacitance, (C_f), found between the contact ribbon or wire and the chip mounting surface that shunts the active part of the PIN chips, has been omitted since its value is very small.

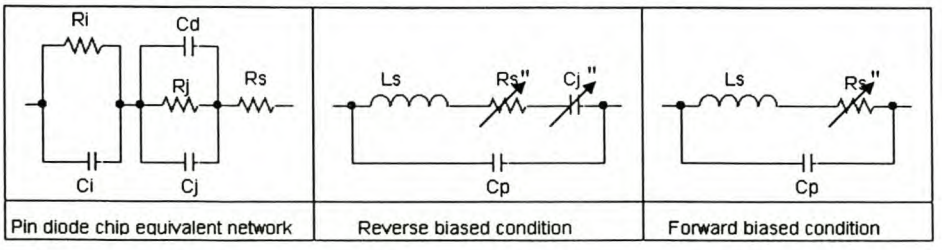
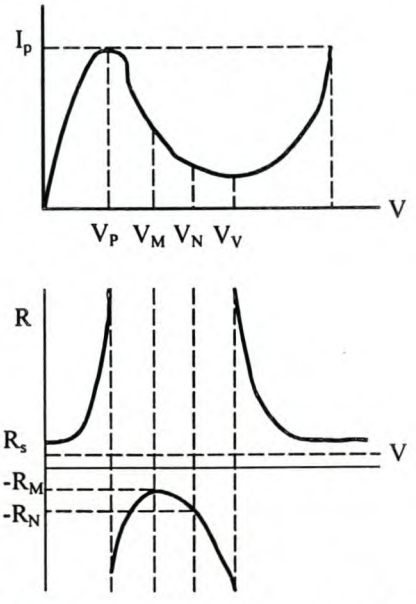


Figure 2-2 The PIN Diode Equivalent Circuits

2.3 Tunnel Diodes

The tunnel diode is a pn junction device with a very high doping on both sides of the junction. The tunnel diode differs from the pn junction diode primarily because of its high doping level. The impurity level in microwave pn junction diodes is in the range of 10^{16} to 10^{18} atoms/cubic centimeters, while values of 10^{19} atoms/cubic centimeters are quite common for the tunnel diode. In electrical specifications, the tunnel diode is highly conductive near zero bias, whereas the pn junction signal diode does not start conducting until it is forward biased to 0.6 volts.



Figuré 2-3 Two characterization curves of tunnel diodes

Fig. 2-3 shows the two curves that characterize tunnel diodes. On top is the I-V curve (current vs. voltage); at the bottom is the R-V (resistance vs. voltage). Two important points concerning these curves should be defined. The first is R_M (minimum negative resistance), which is the terminal minimum negative resistance that occurs at the inflection point on the I-V curve. Measurement of this value is made at a low frequency so the reactive component present can be neglected. The second point is R_N (negative resistance at a minimum K). The value K (noise constant) is a term dependent on temperature, diode current, junction resistance and diode voltage at which the measurement is made. The normal operating point for tunnel diode amplifiers is in the region of R_N and is defined as the value of negative resistance at minimum K. The noise constant does not vary rapidly with junction resistance in this region, so the exact operating point is usually determined by linearity and gain requirements. Values of R_M vary from 35 to 70 Ω depending on the value of I_p used. Values of R_N can range from 40 to the neighborhood of 120 Ω, once again, depending on I_p.

The package capacitance is a function of the package type. Specified values are average values for the specific type of package. In high frequency diodes, the junction capacitance is often much less than the package capacitance.

The effect of series inductance is somewhat dependent upon the diode mounting in the microwave circuit. The values specified are average values for diodes mounted in series with the center conductor of a coaxial transmission line.

The junction resistance is the dynamic resistance of the diode junction. It varies from almost zero where the diode is heavily back-biased, to infinity at the valley current point. It is also approximately zero when the diode is biased heavily in the forward direction.

The series resistance is a combination of contact resistance and spreading resistance, determined by pulsing the diode far into the forward region (where the junction resistance is very low), measuring the incremental resistance with a small sampling pulse on top of the biasing pulse.

Measuring the total capacitance with the diode biased at the valley voltage, then subtracting the package capacitance determines the junction capacitance.

The main applications of tunnel diodes are as amplifiers and oscillators. Tunnel diode amplifiers are lightweight, inexpensive, ultra-low noise components that are useful in the front end of receivers to improve the sensitivity of communications systems. Since tunnel diodes are free from transit time effects, they are a logical choice for use as high frequency microwave oscillators.

2.4 Varactor Diodes

Considerable controversy exists as to why a varactor is capable of frequency multiplication. Step-recovery, abrupt-junction and punch-through are terms being used. The difference in these terms is simply the behavior of the junction capacitance (C_j) as a function of bias voltage.

The step-recovery theory states that as a diode is driven towards forward conduction by the first half cycle of the input signal, it stores a very large charge and appears as a very low impedance. As the input signal reverses polarity, this charge is extracted and the diode remains in the low impedance state until all of the charge is removed. At this time, the diode instantaneously snaps to a very high impedance state, an action that generates a spike of power, which is thought to be the source of harmonic energy. Little, if any acknowledgement was given to the non-linear reactance theory, based on reverse-bias junction capacitance alone. Diodes tailored to enhance this characteristic are called step-recovery diodes or snap varactors.

The punch-through theory of charge-storage multipliers, however, does not accept the fact that the charge-recovery step is the fundamental mechanism by which harmonics are generated. It is argued that should such a fast step exist in any tuned multiplier circuit, the

very presence of any inductance would drive the diode into avalanche breakdown. The multiplication process must therefore be due to some other phenomenon – the non-linear reactance theory. The type of varactor now considered exhibits an abrupt change in its capacitance versus bias characteristics. As a direct result of this relationship, the diode's stored-charge capability versus drive level also exhibits an abruptness. The bias voltage at which this transition in charge-storage capability takes place is termed the punch-through voltage.

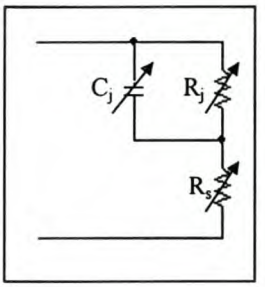


Figure 2-4 The Varactor diode model

The active element of a varactor diode consists of a semiconductor wafer containing a junction of well-defined geometry, usually formed by diffusion.

C_j is the junction capacitance, which is a function of the applied voltage. R_j is the junction resistance, which is in shunt with C_j and is also a function of bias. Finally, R_s is the series resistance, which may be a function of bias, including the resistance of the semiconductor on either side of the junction through which the conduction current passes and the resistance of the ohmic electrical contacts to the wafer.

Varactor diodes are normally operated under reverse bias, where the junction resistance, which is usually 10 MΩ or more, is negligible in comparison with the microwave capacitive reactance of the junction. Therefore, the equivalent circuit of a forward biased varactor at microwave frequencies is generally more complicated, since it must include the diffusion of the injected carriers as well as the effect of these carriers on the conductance of the semiconductor material.

At low frequencies, the varactor exhibits the conventional forward and reverse characteristics of an ordinary diode. For forward bias the diode current increases exponentially with the applied voltage, and for reverse bias a small saturation current (I_s) flows. When the reverse bias is increased to the avalanche breakdown voltage (V_B), the diode reverse current increases very rapidly, since it is limited only by the small diode resistance and any external resistance that is present in the circuit.

The possible applications for varactors include pulse shaping and broadband spectrum generation. Their better-known uses are as frequency multipliers, parametric amplifiers, and tuning elements.

2.5 Gunn Diodes

GaAs transferred-electron oscillators and amplifiers are taking over a significant section of the microwave market. Avalanche diodes may be preferred in the 1 to 10 watt ranges where, in exchange for efficiency, some noise can be tolerated, but for low noise, moderate power, wide bandwidth and high reliability the above mentioned are dominating. The devices used in these amplifiers and oscillators are the Gunn diodes.

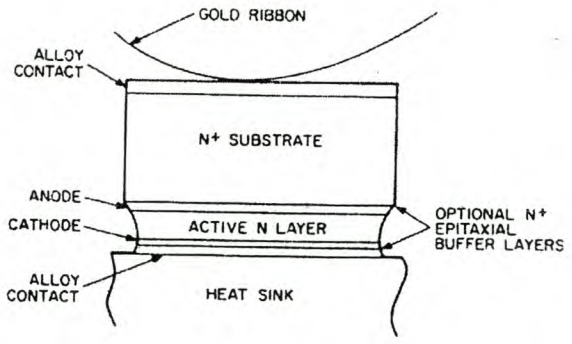


Figure 2-5 The cross section of a Gunn diode

Fig. 2-5 shows the cross section of a typical Gunn diode. The four major factors determining its RF performance are:

- N-active layer
- Ohmic contact
- Bonding-heat sinking
- Package design

The n-active layer is the area where the negative resistance of the device is generated. It is of great importance as it makes the Gunn diode perform as it does. The ohmic (or alloy) contacts are of importance since they determine the amount of conduction in the device. The bond for best heat sinking is, of course, very important, as power must be channeled from the diode chip itself to the heat sink to preserve the chip and allow for the best RF performance. Finally the package design is very critical, because the package itself introduces microwave and thermal parasitics which can significantly degrade RF performance and/or reliability of the Gunn diode.

When the Gunn diode is biased in the negative resistance region the field distribution within the sample rearranges it to form a thin, high field domain with the rest of the sample experiencing a sub-threshold field. The domain drifts through the sample at the saturated drift velocity and collapses when it reaches the anode. The bias current then momentarily increases until a new domain forms at the cathode. It is the periodic current increase, which results in high frequency power being made available to the external circuit.

The output frequency thus is determined basically by transit time effect (the time it takes for one bunch to get from the cathode to the anode), but in practice it is possible to vary

the frequency over about one octave by tuning the external resonant circuit. (The modulation of the bias voltage by the RF voltage developed in the resonant circuit can cause the instantaneous diode voltage to fall below the diode threshold.)

Before discussing applications of Gunn diodes, some precautions to be taken when operating them should be listed. Initially, Gunn diodes should be operated from a constant voltage power supply. The required operating voltage range is determined by the threshold field, power dissipation and breakdown considerations. The data sheets should be carefully checked for maximum voltage ratings. Although in some circumstances it is possible to obtain a greater output by operating at higher voltages (pulsed conditions), no guarantee of reliability is given. The quoted ratings are maximum values and the power supply should be free of any over-voltage transients (which are most likely to occur during switch-on). Bias polarity must, of course, also be heeded very carefully.

Since the frequency pushing characteristics of these devices can be as high as 30 MHz/V, noise and ripple on the power supply can produce a significant amount of FM noise on the oscillator output. A well-stabilized power supply is therefore necessary to reduce frequency noise modulation.

Gunn diodes are now widely used in the 4 to 60 GHz range as power sources for pumps, sweepers, intrusion alarms, and fuses; they are used as transmitters in radars, beacons, transponders, speed sensors, radio and data links, they serve as local oscillators and amplifiers for communication equipment.

An expanding use of Gunn diodes is the field of wideband, tuned oscillators, such as YIG type for sweepers and ECM receivers. The low-noise characteristic and wide bandwidths of Gunn diodes yield full band tuned oscillators for wideband receivers.

Future extensions of Gunn diode uses will be in the medium power area of 1-5 Watts. Whenever a lightweight, inexpensive, battery operated microwave source is part of a system, you would do well to seriously consider the Gunn diode.

2.6 IMPATT Diodes

The IMPATT diode is an avalanche transit time diode and gets its name from the phenomena **IMP**act **A**valanche **T**ransit **T**ime. The basic structure of a silicon pn junction IMPATT diode, from the semiconductor point of view, is identical to that of a microwave varactor diode. The important differences between the two diodes are in their modes of operation and in thermal designs.

Fig. 2-6 shows a typical dc current versus voltage characteristic for a pn-junction diode. In the forward bias direction, the current increases rapidly for voltages above 0.5 volts. In the reverse direction, a very small current flows until the breakdown voltage is reached.

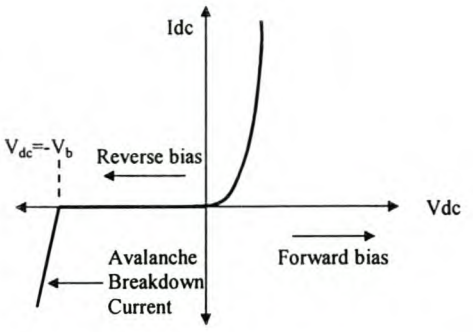


Figure 2-6 The characteristic of a pn Junction Diode

Varactor diodes normally operate with a forward bias or with a reverse bias with a dc operating point well above V_b. IMPATT diodes, on the other hand, operate in the avalanche breakdown region; that is, with a dc reverse voltage greater than Vb and substantial reverse current flowing.

IMPATT diodes have two basic applications – amplifiers and oscillators. One form of amplifier in which IMPATT's are used is the reflection amplifier. In this type of circuit, a circulator must be used to eliminate multiple reflections from distorting waveforms or building up oscillations. A circulator converts the two-terminal diodes into a two-port amplifier with separate input and output ports. At the input port, the impedance should be resistive and not reactive. The matching network to the diode must provide the proper impedance match to the diode to obtain real input impedance. In addition to canceling the reactive component of the diode, the input filter circuit must be present to the diode impedance that prevents the diode from breaking into oscillation.

Amplifiers and oscillators built with what are termed low Q fixed-tuned diodes are the simplest possible IMPATT circuits. The only difference between them is in the choice of the real part of the load impedance.

Low Q oscillators have their primary use in applications where the frequency stability and noise characteristics of the diode can be controlled by injection phase-locking techniques, as in the final output stage of an FM telecommunications transmitter where the injection-locked oscillator functions as a power amplifier. Another application is as an up converter pump, where the frequency of the oscillator is controlled by a low power, high stability injection-locking signal, such as a crystal controlled oscillator/varactor multiplier or a high Q cavity-stabilized IMPATT oscillator. This arrangement is also suitable in a continuous wave (cw) Doppler radar transmitter.

IMPATT amplifiers are also suitable as final power amplifiers in medium power cw transmitters and they can replace the currently used traveling wave tube amplifiers in

many cases. Power gains of 10 dB with 0.5 W output power and 1 GHz bandwidth are obtainable from a single diode amplifier.

High Q low-noise IMPATT oscillators with fixed tuning are also available. The noise performance and frequency stability achievable with these oscillator designs are compatible with local oscillator requirements in radar, telemetry, and telecommunications receivers.

2.7 Conclusion

The discussion on the whole spectrum of microwave diodes was done for the sake of completeness. The use of Schottky diodes in detector applications, however, is by far superior to the other diodes that were discussed. The availability of Schottky diodes, as well as their relative ease of implementation, promotes its use. Its characteristics, as discussed, enable the proper use of Schottky diodes for detector applications.

The Schottky diodes that are used are indicated in Table 2-1.

Frequency [Hz]	Small signal < -20 dBm	Large signal > -20 dBm
< 1 GHz	HSMS-2850	HSMS-2820
< 5 GHz	HSMS-2820	HSMS-2820
< 12 GHz	HSMS-8101	HSMS-8101

Table 2-1 Schottky diodes that are used in this thesis

3 Schottky Barrier Diode Detectors

This chapter describes the characteristics of Schottky barrier diodes intended for use in diode detectors or receiver circuits, and discusses design features of such circuits. The detector circuit is broken into building blocks and the design of each block will be discussed separately in the following chapters.

The Schottky diode as mentioned in chapter 2 receives particularly good attention, because the design examples are based on these characteristics. The aim of this chapter is to serve as an introduction to the design chapters 5 and 6.

3.1 Introduction

Although a diode detector is less sensitive than a heterodyne receiver, its simplicity and low cost can outweigh this disadvantage. For example, a diode detector requires no local oscillator power; it generally uses only a single diode; it is capable of being built with a large RF bandwidth; and it is much less critical to design and maintain than a heterodyne receiver. These advantages make it useful as beacon receivers, missile guidance receivers, fuse-activating receivers, countermeasure receivers and power leveling and signal monitoring detectors.

The detector circuit can be broken into three blocks in Fig. 3-1.

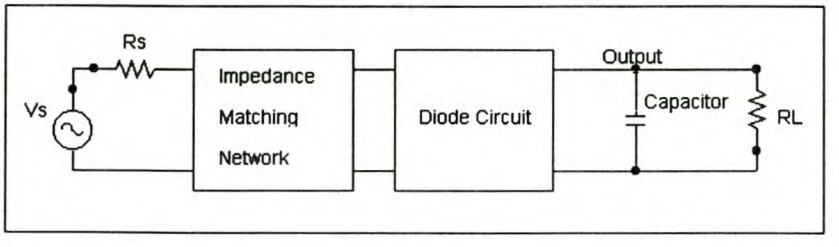


Figure 3-1 Block diagram of a detector circuit

The RF impedance matching network is important to obtain the best performance possible from a given diode circuit. The design will be described in a following section.

The diode circuit can take many forms, depending on the demands of the specific design. Four of them are shown in Fig. 3-2.

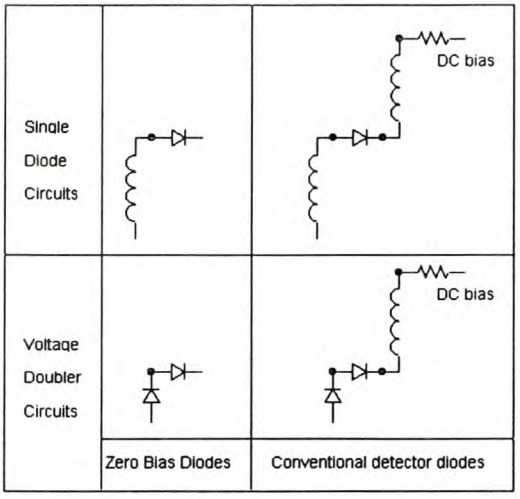


Figure 3-2 Common types of diode circuits

Single diode circuits offer simplicity and minimum cost as their advantage. The voltage doubler produces a higher output for a given input power and offers lower input impedance to the source, simplifying the input impedance matching network. Either can be realized using conventional or zero bias Schottky diodes [43].

A typical diode detector circuit is shown in Fig. 3-3. The operation of this circuit is quite simple. At RF, the bypass capacitor appears as a short circuit, and the input RF choke (RFC_1) appears as an open circuit. The input RF filter is optimized to match the signal source impedance to the diode's RF impedance over a specified bandwidth. Ideally, all of the available signal power is delivered to the diode. Due to the nonlinearity of the diode, the data signal is extracted from the modulated RF signal and appears across the load

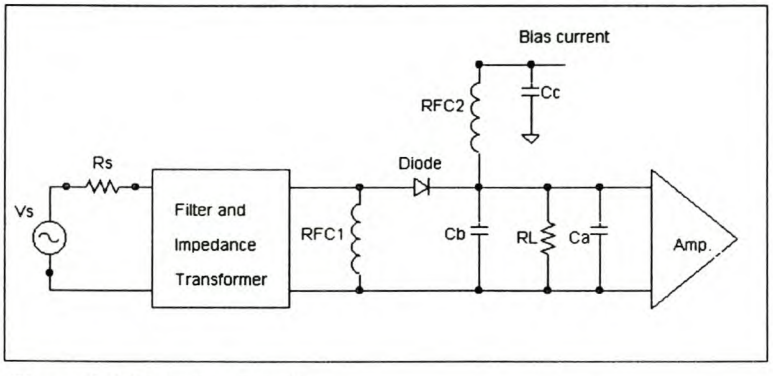


Figure 3-3 Detector circuit

resistance. That is if the detector is used as a receiver. At data frequencies, RFC1 acts as a short circuit, while C_b and the DC bias filter, consisting of RFC2 and C_c, both appear as high impedances. RFC1 also serves as a return path for the DC bias current. Finally, the capacitor (C_A) shown in Fig. 3-3 separates the RF from the detected side of the circuit. It can be either lumped (as a chip soldered to the PC board) or distributed (as a patch etched

into the circuit). It must provide a good RF short circuit to the diode, to insure that all the RF voltage appears across the diode terminals. However, it must be small at data frequencies, so that it does not load the rest of the circuit [23].

3.2 Diode performance Characteristics

The performance characteristics that are used to describe diode detectors are Tangential Sensitivity, Video resistance and Voltage sensitivity.

3.2.1 Tangential Sensitivity (TSS)

This is the lowest signal power level for which the detector will have a specified signal-to-noise ratio at the output of the amplifier. The units for TSS are dBm or milliwatts. TSS does not depend entirely on intrinsic diode parameters and many factors affect the measured TSS value for a given diode. The most important factors are:

- RF frequency
- Bandwidth
- Diode DC Bias current
- Test mount or circuit
- Output amplifier noise figure

For an exact TSS specification, the effective bandwidth should be stated as the lower and the upper 3 dB frequencies of the entire output circuit, including the diode's output resistance. (See section 3.2) A statement of only the bandwidth of the output amplifier can be misleading because it does not always determine the overall or effective bandwidth of the system. The limitation on overall bandwidth can come both from the circuit between the diode output and the amplifier input or the instrumentation circuit after the amplifier, i.e. oscilloscope or meter.

Because the upper 3 dB frequency is usually several orders of magnitude greater than the lower 3 dB frequency, it is common to state only the upper 3 dB frequency. The implication is that the response of the output circuit of the detector to the modulating signal extends from DC to the actual bandwidth. In practice, the low frequency response very seldom extends down to DC, because this will include the flicker noise contribution of the diode and the output amplifier, both of which deteriorate TSS. If the diode is expected to be used in a system that will require low frequency response, then the low frequency 3 dB point of the test system must be stated. Failure to do so can lead to gross differences in TSS between the test system and the actual system if the diode's flicker noise corner frequency f_N is high, i.e. greater than 50 kHz.

To obtain maximum sensitivity at any given frequency, most detector diodes must be forward DC biased. Bias, however introduces shot and flicker noise in the diode, and reduces the diode video resistance. These effects exert a competitive influence on TSS – therefore, the bias value must be stated.

A tangential signal is, furthermore, defined on a C.R.T. display as a pulse whose bottom level coincides with the top level of the noise on either side of the pulse. Although the corresponding signal-to-noise ratio depends on many factors, as previously discussed, the generally accepted ratio of 8 dB at the output correlates well with the tangential appearance on the oscilloscope for practical systems [27].

A useful production test system uses an RMS voltmeter to compare signal output to noise output. The noise level is observed on the meter with RF signal off, but with DC bias applied to the D.U.T. Then the specified tangential level is applied and the increase in RMS voltmeter reading must correspond to 8 dB or more. This test will be visualized in chapter 8 on some design examples.

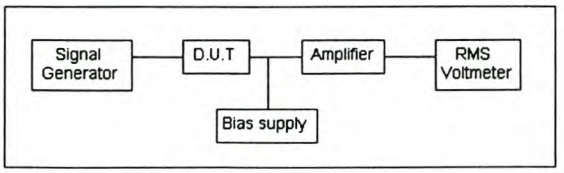


Figure 3-4 TSS Test System

To theoretically describe the threshold performance, various definitions have been used [23], [33]

$$TSS_{(dBm)} = -107 + 5\log B_V + 10\log I_d + 5\log\left[R_A + \frac{28}{I_d}\left(1 + \frac{f_n}{B_V}\ln\frac{B_V}{f_l}\right)\right] + 10\log\left[1 + \frac{R_s C_j^2(i) f^2}{I_d}\right] \quad \textbf{[3-1]}$$

B_V Bandwidth in Hz
I_d Diode DC bias in uA
f_n Diode flicker noise corner frequency, Hz
f_l Output circuit low frequency 3 dB point, Hz
R_s Diode series resistance, Ω
$C_j(i)$ Junction capacitance, pF, at bias current I_d
f Operating frequency, GHz
R_A Amplifier equivalent noise resistance, kΩ

This expression reveals that the only significant diode parameters that effect the detector sensitivity are the three parameters f_n, R_s and C_j. The measurement or extraction of the flicker noise corner frequency is not discussed in this thesis. The values given by manufacturers' data sheets are accepted as accurate enough.

3.2.2 Video Resistance (R_v)

The video resistance is simply the small signal low frequency dynamic resistance of the diode and is dependent on the DC bias current. The value of the bias current used is the same that is used in the TSS test.

R_v consists of the sum of the diode's series resistance (R_s) and the junction resistance (R_j) [23]

$$R_v = R_s + R_j \quad \text{[3-2]}$$

R_j is obtained by differentiating the diode voltage-current characteristic and is given by

$$R_j = \frac{nkT}{q(I_s + I_0)} \quad \text{[3-3]}$$

where I_0 is the bias current and I_s is the saturation and is negligible when the diode is operated in the optimum bias region.

3.2.3 Voltage Sensitivity

This parameter specifies the slope of the output voltage versus the input signal power. It is bias, load resistance, signal level, and RF frequency dependent, and all of these conditions must be specified. It is particularly sensitive to signal level, which must be kept well within the square law dynamic range of the diode. That is if the detector is operated in only the square law region.

Given knowledge of the package parasitics, the chip parasitics, the diode's saturation current and the load resistance, one can calculate the voltage sensitivity of a Schottky diode [15],[17].
Neglecting parasitic and reflection losses:

$$\gamma = \beta \Big/ \frac{\partial I}{\partial V} \quad \text{[3-4]}$$

and

$$\frac{\partial I}{\partial V} = \frac{I_0 + I_s}{1/\alpha} \quad \text{[3-5]}$$

The theoretical current sensitivity is 20 amperes per watt, therefore if α=38.4615

$$\gamma = \frac{0.52}{I_0 + I_s} \quad \text{[3-6]}$$

Consideration of the effects of junction capacitance, load resistance and reflection loss will bring eq. 3-6 closer to reality.

The effect of junction capacitance on current sensitivity has been derived [17]. Adding this effect to the voltage sensitivity gives

$$\gamma = \frac{0.52}{I_{s+0}(1+\omega^2 C_j^{\ 2} R_s R_v)} \qquad [3\text{-}7]$$

A detector diode may be considered as an output voltage source of impedance R_v feeding a load resistance R_L. The voltage across the load is reduced by the ratio of R_L to R_v+R_L:

$$\gamma = \frac{0.52}{I_T(1+\omega^2 C_j^{\ 2} R_s R_j)(1+R_v/R_L)} \qquad [3\text{-}8]$$

The analysis thus far has assumed that all incident power is absorbed by the diode. Normally this is a good assumption because low loss matching circuits can be designed to eliminate reflection losses. With zero bias detectors, however, the mismatch may be so severe that it is not possible to eliminate these reflection losses. In fact, most of the incident power may be absorbed by losses in the matching network. If we go to the other extreme and assume no matching, the sensitivity becomes:

$$\gamma = \frac{0.52(1-\rho^2)}{I_T(1+\omega^2 C_j^{\ 2} R_s R_j)(1+R_v/R_L)} \qquad [3\text{-}9]$$

where ρ is the reflection coefficient of the diode.

From eq. 3-9 one can see that the load resistance R_L must be large compared to the diode's junction resistance R_j. The former is often set to 100 kΩ or higher, but the designer does not always have control over it. R_j can, of course, be lowered through an increase in DC bias current I_b. However, since it appears in the denominator of the equation, raising bias current too high can reduce the sensitivity.

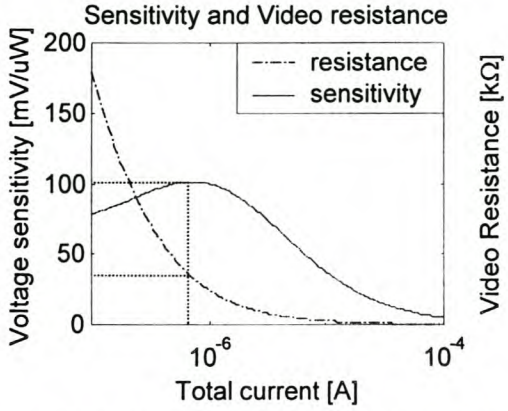


Figure 3-5 Voltage sensitivity and Video resistance as a function of total current

In Fig. 3-5 the tradeoff between sensitivity and junction resistance is clearly shown. For this n-type diode operating at 915 MHz, a choice of 0.8 uA total DC current will result in

the maximum value of sensitivity but with R_j=40 kΩ. As shall be seen in a later chapter, an impedance of 40 kΩ cannot be matched to 50 Ω. This high level of sensitivity is unavailable in a practical circuit design.

Also from eq. 3-3, it can be seen that C_j and R_s must be minimized in order to obtain the maximum voltage sensitivity. Unfortunately, in the design of Schottky diodes, a change (such as reducing contact diameter) which reduces C_j will increase R_s. Obviously, the effect of C_j will be more significant in a detector operating in X-band, while R_s will be the important parasitic for a detector operating in the tens of MHz.

3.3 Square-law and Linear Detection

3.3.1 Diode Basics

The job of the detector diode is to convert input RF power to output voltage. At low power levels, the transfer characteristic of a Schottky diode follows a square-law rule, with voltage output proportional to power (voltage squared) input. As input power is increased, the slope of the Vo/Pin curve flattens out to more nearly approximate a linear (voltage output proportional to RF voltage input) response.

At small signal levels, the Schottky diode can be represented by a linear equivalent circuit, as was discussed in chapter 2. To summarize:

R_j is the junction resistance of the diode, where the RF power is converted into a data voltage output. For maximum output, all the incoming RF voltage should ideally appear across R_j. C_j is the junction capacitance of the diode chip itself. It is a parasitic element which shorts out the junction resistance, shunting RF energy to the series resistance R_s. R_s is also a parasitic resistance representing losses in the diode's bondwire, the bulk silicon at the base of the chip and other loss mechanisms. RF voltage appearing across R_s results in power loss as heat. L_p and C_p are package parasitic inductance and capacitance, respectively. Unlike the two chip parasitics, they can easily be tuned out with an external impedance matching network.

3.3.2 Detection Law

Over a wide range of input power level (P) the output voltage (V) follows the formula [44]

$$V = K\left(\sqrt{P}\right)^{\alpha} \qquad \text{[3-10]}$$

At low levels, below –20 dBm, α is two. This is the square-law region. When DC biased current is used, the diode impedance is independent of power level. At higher power levels the diode impedance changes with power. At these levels, the value of α can be as

low as 0.8. The slope is related to the diode capacitance, frequency and load resistance. When the circuit is retuned at each power level, the output and the slope increase.

The effect of frequency and diode capacitance on voltage sensitivity

The diode junction capacitance shunts the junction resistance. Detected voltage is reduced because some of the input current flows through the capacitance and never reaches the resistance where detection takes place. The effect is more serious at higher frequencies because capacitance susceptance is proportional to frequency. Similarly, the effect is more serious for higher capacitance diodes.

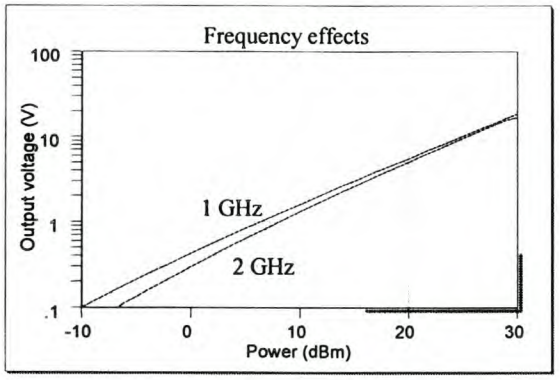


Figure 3-6 Effect of higher frequency on detection slope

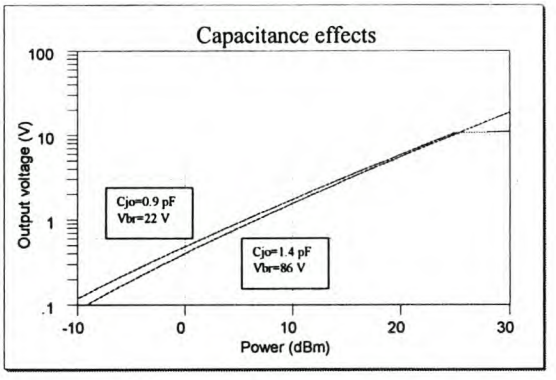


Figure 3-7 Effect of higher capacitance on detection slope

The effect of frequency and diode capacitance on the slope at high-level detection

Fig. 3-6 shows how the slope of the detection characteristic becomes steeper at higher frequencies. The output voltage at 2 GHz is nearly equal to the 1 GHz voltage above 22 dBm. The main reason for this behavior is the lower value of junction resistance at higher power.

Since frequency and diode capacitance appear in the degradation factor (eq. 3-11) as the product f*C, the increasing slope at higher frequencies also happens at higher capacitance. This is shown in Fig. 3-7.

Effect of breakdown voltage

In Fig. 3-7 the curves cross so that above 25 dBm the voltage detected by the HSMS-2800 is higher than the voltage detected by the lower capacitance HSMS-2824. The degradation factor analysis does not explain this crossover. It is related to the effect of breakdown voltage. At high power levels the negative portion of the input signal is large enough to cause reverse conduction. This negative detected voltage reduces the output level and the curve levels off. At higher levels the negative detected voltage will dominate and the curve will reverse direction and have a negative slope.

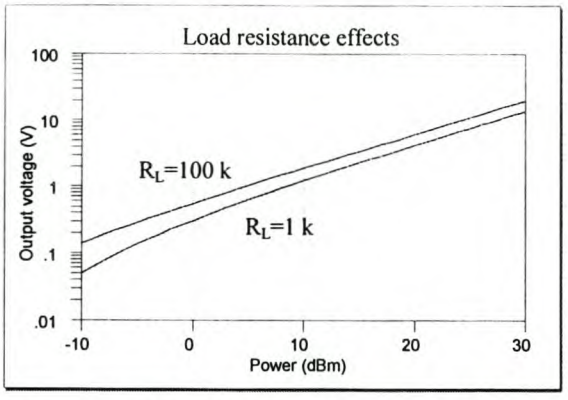


Figure 3-8 The effect of load resistance on the detection slope

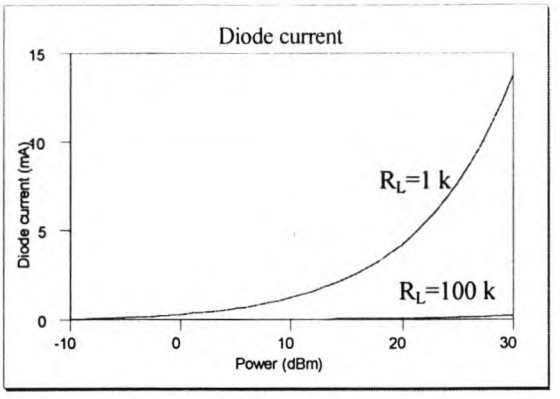


Figure 3-9 The effect of load resistance on the diode current

The effect of load resistance on detection slope

Fig 3-8 shows that the slope of the detection curve increases when the load resistance is decreased from 100 kΩ to 1 kΩ. The detection law increases. The rectified current at high power causes a decrease in the degradation factor due to low C_j and R_j. When the load resistance is decreased the rectified current increases. The degradation factor decreases so the slope is steeper.

Detection degradation

Parasitic series resistance and junction capacitance degrade the performance of Schottky detectors. Some of the voltage applied across the diode appears across the series resistance R_s and is not available to be detected by the junction resistance R_j. A more serious effect is the division of current between the junction resistance and the junction capacitance. The degradation factor is [22]

$$\deg radation = 1 + \frac{R_s}{R_j} + 4\pi^2 f^2 C_j^{\,2} R_s R_j \qquad \textbf{[3-11]}$$

3.4 The Necessity of Bias Current

Conventional Schottky detector diodes are tested and specified with 20 mA of DC bias. The bias current reduces the junction resistance so that most of the detected voltage appears across the load resistance. In some applications the diode is used to monitor power rather than to detect a low level signal. In this case, the signal level may be high enough to reduce the junction resistance sufficiently without the use of DC bias.

3.4.1 Junction Resistance

A detector diode may be considered as a voltage source in series with the diode resistance. The output voltage is taken from a load resistance in series with the diode.

This circuit is a voltage divider. The detected voltage is divided between the diode and the load. The useful output voltage is [18]

$$V_0 = \frac{V_{oc} R_L}{R_L + R_D} \qquad [3\text{-}12]$$

For best performance the ratio of diode resistance to load resistance should be small. In many cases load resistance cannot exceed 100 kΩ in order to keep the response time small enough to handle fast pulses. That is if the diode needs to demodulate a pulsed signal.

3.4.2 Measured Detected Voltage

Fig. 3-10 shows the detected voltage with 20 uA bias and with zero bias. Above –20 dBm the rectified current is high enough to change the diode junction resistance. The upper curves show the detected voltage when the circuit is tuned at each input power level to match the changing diode impedance. The lower curves show the reduced output level when the tuning is not changed.

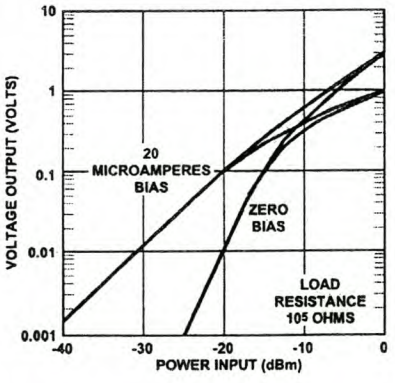


Figure 3-10 Detection characteristics of Schottky diode [18]

The lower diode resistance with DC bias is small compared to the load resistance. In this case the measured voltage is the open circuit voltage.

With zero bias the diode resistance is much higher than the load resistance so most of the detected voltage appears across the diode. However, at higher input levels rectified current flows through the diode and reduces the junction resistance. The voltage divider action is no longer significant and the output approaches the detected voltage of the biased diode.

3.5 The Voltage Doubler

Diode detectors may be combined in various ways to produce higher output voltages than would be produced by a single diode. Such a detector is shown in Fig.3-2 in section 3-1

The voltage doubler circuit offers several advantages. First the voltage output of two diodes are added in series, increasing the overall value of voltage sensitivity for the network. Secondly, the RF impedances of the two diodes are added in parallel, making the job of reactive matching a bit easier [43], [31].

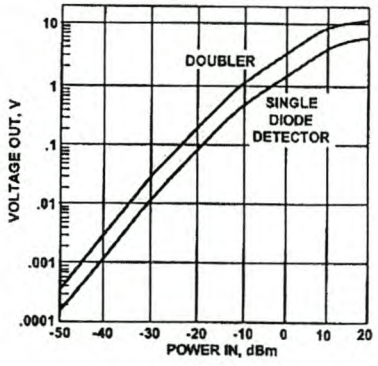


Figure 3-11 Voltage doubler matched at each power level [43]

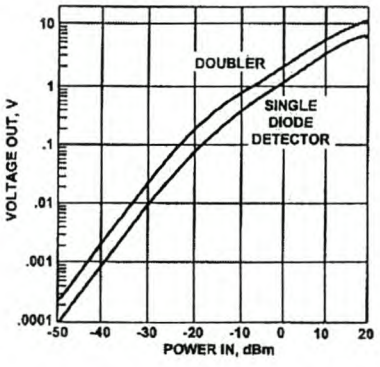


Figure 3-12 Voltage doubler matched at –30 dBm [43]

3.6 The Diode Detector at Temperature Extremes

The zero bias Schottky diode detector is ideal in applications to fabricate a receiver, which consumes no primary power. However, its performance is heavily dependent upon its saturation current, which is a strong function of temperature. At both low and high temperature extremes, this dependence can lead to degradation in performance.

A Schottky diode can be represented by a linear equivalent circuit as discussed in chapter 1 and in more detail in chapter 2.

L_p, C_p, and R_L are constants. R_s has some small variation with temperature, but that variation is not a significant parameter in analysis. C_j is a function of both temperature and DC bias, but the concern is more with zero bias detectors and the temperature is not significant. Rj is a key element in the performance of a detector.

3.6.1 Junction Resistance

Three different currents affect the junction resistance of a Schottky diode. The first is the diode's own saturation current, I_s. The second is externally applied bias current, I_0. The third is $I_c=V_0/R_L$, the circulating current produced by rectification in the diode. In the small signal region of interest in this discussion, where $I_c < I_s$, the equation for junction resistance is, as previously mentioned

$$R_j = \frac{nkT}{q(I_s + I_0)} \qquad [3\text{-}13]$$

where n is the diode ideality factor (emission coefficient), k is Boltzmann's constant (1.38062×10^{-23} J/K), q is the electronic charge (1.60219×10^{-19} C), and T is temperature in Kelvin.

The equation for saturation current is given by [21], [49]

$$I_s = I_{s0}\left(\frac{T}{T_0}\right)^{\frac{2}{n}} e^{\frac{-q\psi}{k}\left(\frac{1}{T}-\frac{1}{T_0}\right)} \qquad \text{[3-14]}$$

where T_0 is 273 K (room temperature), I_{s0} is saturation current measured at room temperature and ψ is the metal-semiconductor Schottky barrier height.

Combining these two equations produces a relation for R_j as a function of temperature.

3.6.2 Performance of Detector over Temperature

The two performance parameters of interest are the bandwidth and voltage sensitivity of the detector. The analysis of bandwidth as a function of temperature is straightforward and will be shown first.

The output circuit has a low pass filter response, with a 3 dB cutoff frequency defined by

$$f_c = \frac{1}{2\pi C_T R_T} \qquad \text{[3-15]}$$

where

$$R_T = \frac{R_j R_L}{R_j + R_L}. \qquad \text{[3-16]}$$

Using the variation in R_j, the variation in bandwidth can be computed. Typical values of R_L=100 kΩ and C_T=100 pF were used to compute the curve of cutoff frequency vs. temperature shown in Fig. 3-13 for the HSMS-2850 Schottky diode.

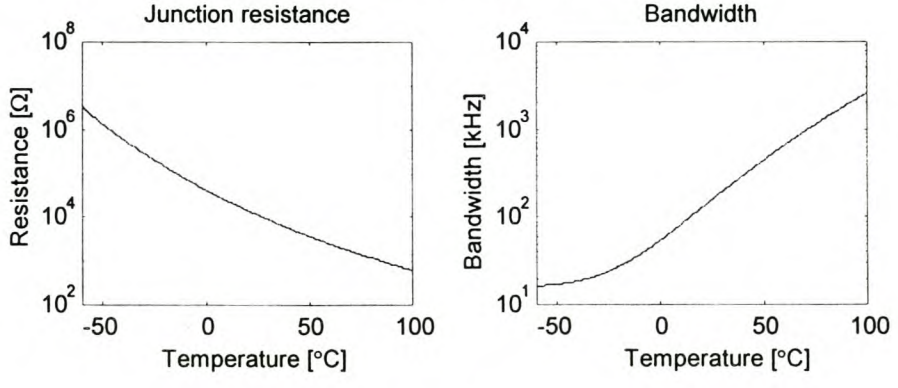


Figure 3-13 The behavior of junction resistance and bandwidth due to temperature variations

As can be seen from this plot, bandwidth can deteriorate to a value as low as 30 kHz. Of course, a reduction in C_T will improve bandwidth, but there are practical limits to how low total capacitance can be made. Similarly, a reduction in R_L will increase bandwidth, but at the expense of voltage sensitivity, according to the following relationship [21]

$$\gamma = \gamma_{oc} \frac{R_L}{R_L + R_j} \qquad \text{[3-17]}$$

where γ_{oc} is the detector's voltage sensitivity for $R_L = \infty$.

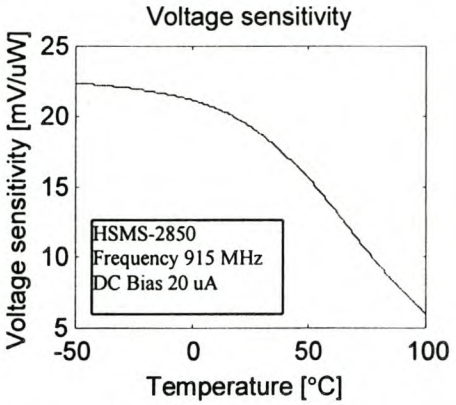


Figure 3-14 The variation of voltage sensitivity over temperature

The effect on voltage sensitivity due to temperature variations can be significant. Performance improves at lower temperatures in a predictable manner. Typical behavior of voltage sensitivity vs. temperature is shown in Fig.3-14. The temperature dependence of current sensitivity was studied by Cowley and Sorensen [33], but the analysis was not extended to the voltage sensitivity. For the ideal diode with infinite cutoff frequency (zero series resistance and/or zero junction capacitance) there is no temperature effect on voltage sensitivity. The inverse temperature behavior of current sensitivity is balanced by the direct temperature variation of the diode barrier resistance. That is, for current sensitivity [15]

$$\beta = \frac{q}{2nkT} \qquad \text{[3-18]}$$

and for diode junction resistance

$$R_j = \frac{nkT}{qI} \,. \qquad \text{[3-19]}$$

In these equations, T is temperature in Kelvin, I is bias current in milliamperes and n, q and k are constants.

The analysis of voltage sensitivity as a function of temperature for a Schottky diode detector is complex. It can, however, partially be done by the method of Ritz and Galerkin which will be discussed properly in chapter 6.

3.6.3 Compensation Methods

Conventional DC biased detectors generally operate from a continuous current of 10 to 30 uA and offer greater temperature stability than the zero bias Schottky detector. However, these are devices with saturation currents in the nanoampere range. Nevertheless, the use of supplement DC bias current suggests itself as a solution to poor bandwidth and low sensitivity at low temperatures, as is illustrated in Fig. 3-16. The addition of supplement DC bias current has no effect on the sensitivity of the detector at higher temperatures.

RF impedance mismatch is the major cause for poor voltage sensitivity at higher temperatures. To compensate for poor sensitivity at high temperatures, the input-matching network must be adjusted. Matching must be done at the higher temperatures, letting the match at lower temperatures degrade. The matching of detectors is discussed in chapter 5.

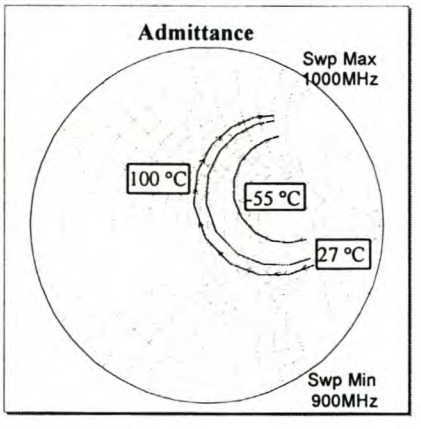


Figure 3-15 Effect of temperature on the input admittance of detector

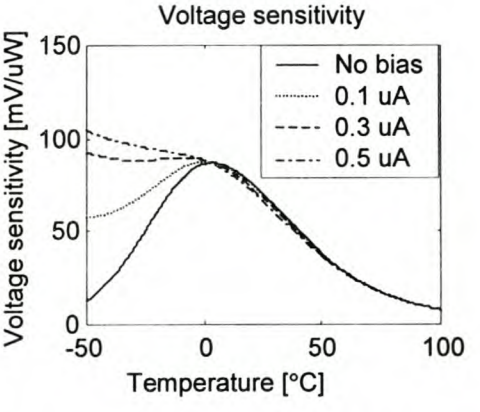


Figure 3-16 Improvement of the sensitivity at low temperatures

3.7 Conclusion

It is now clear that the design of optimum diode detectors is a well researched and discussed subject. It is possible to describe the behavior of detectors mathematically and to develop some design equations to assist in optimum designs. Design techniques, however, is still a matter of making sacrifices in one area (e.g. detection sensitivity) while gaining in another (dynamic range). It is important to have a good understanding on what

is needed to achieve and what is an important design specification that needs to be satisfied.

Different approaches must be followed when designing for large bandwidth, maximum sensitivity or maximum dynamic range small signal detectors. To design large signal detectors needs once again a different approach.

In the following chapters the behavior of the Schottky diodes proposed for use in this thesis are well defined by means of small and large signal models. These models will be used in further design and analysis, for example the design of matching circuits and the proper analysis of detector circuits by means of harmonic balance simulations.

4 The Characterization of Diodes

Schottky diodes that are widely in use are well defined in manufacturers' data sheets. In order to do a more proper and accurate analyses of diode performance and in particular the performance of diode detectors, it is necessary to extract a diode model, based on accurate measurements.

The measurement of all the elements that make up the equivalent circuit for a packaged Schottky diode is a complex task. Various techniques are used for each element. The task can be divided into two parts - firstly the linear parameters of the model and secondly the more complex nonlinear parameters. When linear or nonlinear analyses are performed on diode circuits, both the diode wafer and its package must be accurately modeled.

In this chapter the simplified Spice model will be discussed, because of its value for the later use in the Harmonic Balance algorithm, as well as the parameter extraction method. An extraction method for the intrinsic and extrinsic parameters, from the diode's IV-data and small signal data is developed. Finally an optimization algorithm is presented to refine the model.

4.1 The Spice Model

Spice uses three equivalent circuits in diode analysis: transient, AC, and noise circuits. Components of these circuits form the basis for all element and model equations.

The fundamental component in the DC equivalent circuit is the DC diode current, I_d. For noise and AC analyses, the actual I_d current is not used. The partial derivative of I_d with respect to the terminal voltage V_d is used instead [14].

$$gd = \frac{\partial I_d}{\partial V_d} \qquad \textbf{[4-1]}$$

where

$$I_d = I_s\left[e^{\alpha_a(V_d - I_d R_s)} - 1\right] \qquad \textbf{[4-2]}$$

gd is used in the **H**armonic **B**alance algorithm [HB] as well. It will be discussed in chapter 6.

The small signal junction capacitance can be described by [15], [49]

$$C_j = \frac{C_{j0}}{\left(1 - V_d/V_j\right)^{1/2}} \qquad V_d > V_j \qquad \textbf{[4-3]}$$

A more detailed discussion of this simplified equation is done in section 4-3.

This is a simplified representation of the Spice model, ignoring many of the parameters that are not applicable to the basic functioning of the Schottky diode. For a detailed discussion on the Spice model – see Appendix A

Spice parameters	Description
I_s	Saturation current
α_a	$\alpha_a=q/nkT$
q	Electron charge
n	Ideality factor
k	Boltzmann constant
T	Junction temperature
R_s	Series resistance
ϕ	Barrier potential
C_{j0}	Junction capacitance

Table 4-1 The Spice parameters

4.2 Parameter Extraction from the IV-curve

A typical diode DC IV characteristic in the forward bias region is shown in Fig. 4-1. Because of the voltage drop across the series resistance, the terminal voltage and current have the characteristic as indicated in eq [4-2], where V_d and I_d are the terminal voltage and current, respectively. At low current levels, the voltage drop across the resistance can be ignored. Equation [4-2] can then be simplified to [49], [32]

$$I_d = I_s e^{\alpha_a V_d} \qquad [4\text{-}4]$$

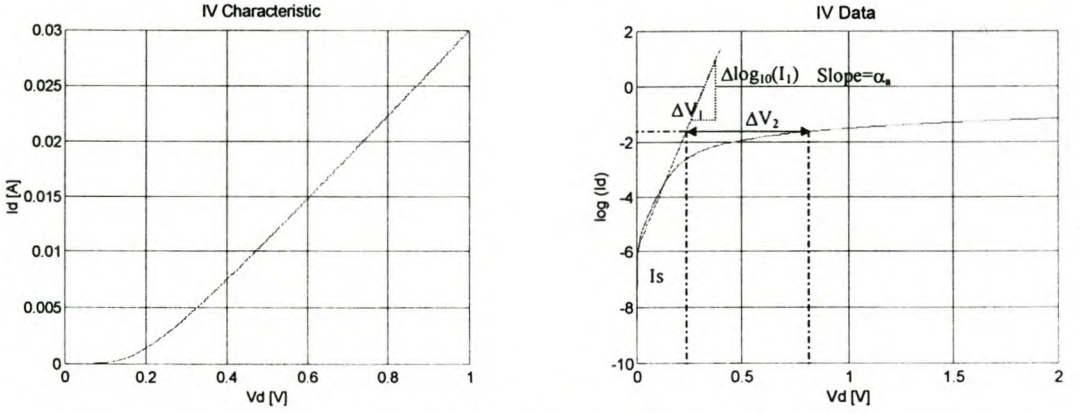


Figure 4-1 The DC IV characteristics of a Schottky diode on a linear and logarithmic scale

Thus

$$\log_{10}(I_d) \approx \log_{10}(I_s) + \frac{\alpha_a}{\ln(10)} V_d \qquad [4\text{-}5]$$

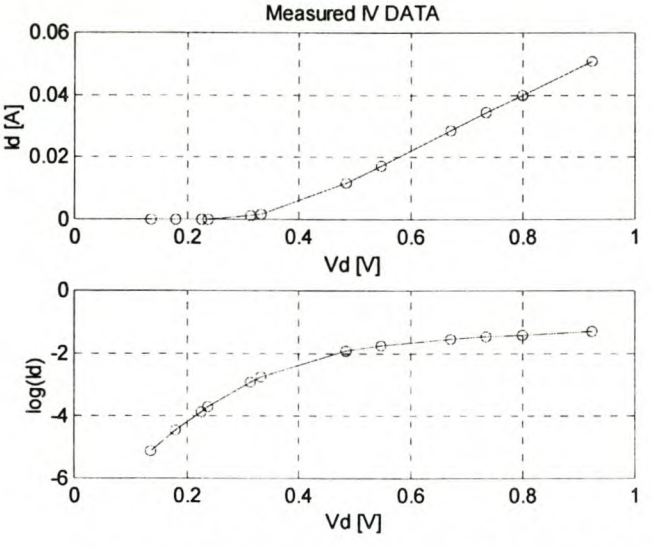
Equation [4-5] states that $\log_{10}(I_d)$ is a linear function of V_d with a slope of $\alpha_a/\ln(10)$ and intercepting the y axis at $\log_{10}(I_s)$. As indicated in Fig. 4-1, the slope of the line is $\Delta\log_{10}(I_1)/\Delta V_1$

$$\alpha_a = \frac{\ln(10) \times \Delta \log_{10}(I_1)}{\Delta V_1} \qquad [4\text{-}6]$$

By extending the straight line at low currents, I_s is the intercept point of the straight line at the current axis.

At high current levels, the IV characteristic deviates from a straight line due to the additional voltage drop across the series resistance. For a first-order approximation, the value of this resistance can be assumed constant. To determine its value from a DC IV characteristic, a current level must be chosen where the additional voltage drop is evident; thus, the voltage difference at that point between the measured data and the straight line is the additional voltage drop across the series resistance. R_s is simply

$$R_s = \frac{\Delta V_2}{I_2}. \qquad [4\text{-}7]$$



Parameter	Value
Is	2.04e-7 A
Rs	9.5 Ω
α	28.0811

Figure 4-2 The measured IV characteristic of a Schottky diode and its extracted parameters

Let us test this method with measured results. The IV-characteristics of a Schottky diode was measured and the results are shown in Fig.4-2. The IV-extraction method is applied to the measured data and the extracted parameters are indicated in the table in Fig. 4-2.

By using eq [4-2], which describes the IV-curve of a Schottky diode, a comparison can be made between the model and the measured curve. The parameter values obtained by the above technique are in excellent agreement with the actual data. Their optimal values can be obtained by fitting eq [4-2] to the DC I-V characteristic data. The values that have been derived from the technique above can be used as the starting values for optimization.

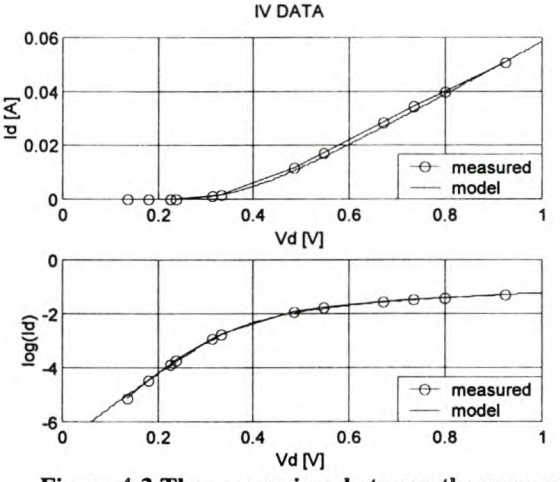


Figure 4-3 The comparison between the measured data and the model for the IV characteristic

Manufacturers may also provide data for the video resistance. The video resistance is defined as [32]

$$R_v = R_s + \frac{1}{\partial I_d / \partial V_d} = R_s + \frac{1}{\alpha_a (I_d + I_s)} \qquad \textbf{[4-8]}$$

This data may be used for model verification.

4.2.1 Optimizing the results obtained by the IV characteristics

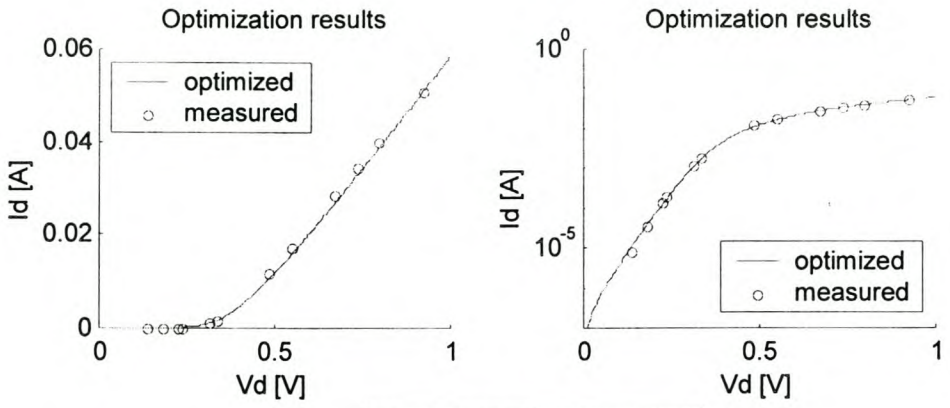
The model extracted thus far is fairly accurate over the whole bandwidth. The strive for improved accuracy, forces us to optimize the model. A detailed discussion on Newton's optimization algorithm is done in Appendix B. To apply this method on the current problem is not very difficult. The implementation of the algorithm will not be discussed in detail in this chapter and more emphasis will be laid on the results of the optimization.

The algorithm is based on the diode current eq [4-2] and therefore it is necessary to optimize only three parameters namely I_s, R_s and α_a.

The error function is the difference in the measured current and the calculated current. The error that is minimized is the sum of the squares of the error function.

Fig. 4-4 indicates the results after the optimization of the model. The optimized model parameters are shown in the table in Fig. 4-4. It does not differ to a large extent of the

results obtained in Fig.4-2. The values in Fig.4-2 were used as the starting values to the optimization algorithm.



Parameter	Value
Is	2.118e-7 A
Rs	9.489 Ω
α	27.959

Figure 4-4 The optimized results of the IV model compared with the measured results

The results obtained from the IV extraction method can be used with confidence. The application of the optimization algorithm is not really necessary, because the improvement is not worth the time it takes for the optimization to complete.

4.3 Parameter Extraction from CV-curve

The CV-curve of a Schottky diode is not always known. It is not always possible to measure it, however, some manufacturers' data sheets contain some CV-curve information. It is sometimes useful to extract the junction capacitance directly from the data sheet if you have confidence in the measurements [49], [32].

The diode junction capacitance is formulated as:

$$C_j(V_d) = C_j(0)\left(1 - \frac{V_d}{V_j}\right)^{-\gamma(V_d)} + C_D \qquad V_d \le V_j$$
$$C_j(V_d) = C_j(0)(0.2)^{-\gamma(V_d)} + C_D \qquad V_d > V_j \qquad \textbf{[4-9]}$$

V_j is the junction built-in voltage and $C_j(0)$ is the depletion capacitance at $V_d=0$.
γ is a function of V_d and expressed by a third order polynomial as follows:

$$\gamma(V_j) = \gamma_0 + G_{C1}V_j + G_{C2}V_j^{\,2} + G_{C3}V_j^{\,3} \quad \text{[4-10]}$$

C_D is the diffusion capacitance, which is written as:

$$C_D = C_{D0}e^{\alpha_c V_j} \quad \text{[4-11]}$$

The CV characteristic has been formulated in eq [4-9]. At low to moderate current levels, the capacitance is dominated by the junction depletion capacitance and the diffusion capacitance can be neglected. For a first order approximation, $\gamma(V_d)$ can be assumed constant, i.e. G_{C1}, G_{C2}, and G_{C3} are equal to zero.

Manufacturers normally provide a value of the total capacitance at zero bias. Subtracting the package parasitic capacitance from this value, the intrinsic capacitance at zero bias, i.e. C_{j0}, is the obtained.

V_j and γ_0 are technology dependant. V_j is the junction built in voltage. Its value depends on the material properties, doping profile and junction type. γ_0 is dependent on the junction type.

If manufacturers provide the CV characteristic curve, V_j and γ_0 can be determined using two points on the curve at large reverse voltages. Since at large reverse voltages

$$1 + \frac{V_d}{V_j} \approx \frac{V_d}{V_j} \quad \text{[4-12]}$$

then

$$\frac{C_1}{C_2} \approx \left(\frac{V_2}{V_1}\right)^{\gamma_0} \quad \text{[4-13]}$$

where C_1 is the capacitance at reverse bias V_1 and C_2 the capacitance at reverse bias V_2. Therefore

$$\gamma_0 \approx \frac{\ln(C_1/C_2)}{\ln(V_2/V_1)} \quad \text{[4-14]}$$

After extracting C_{T0} and γ_0, ϕ can be derived from the following equation.

$$V_j = \frac{V_2}{(C_{j0}/C_2)^{1/\gamma_0}} \quad \text{[4-15]}$$

Optimal values can once again be obtained by curve fitting eq [4-15] to the measured data.

4.4 Small Signal Parameter Extraction

4.4.1 The use of TRL Calibration

The purpose of vector network analyzer calibration is to establish a reference plane for subsequent s-parameter measurements. The reference plane typically corresponds to the input and output ports of the device under test, such that the calibration enables microprocessor correction for the effects of cables, connectors, microstrip feedlines, and the interior circuitry of the VNA. The TRL technique is preferred over other calibration methods because well characterized opens, shorts and loads are not required, and a reference plane can be easily established (by setting the length of the feedlines) at any distance from the edge of the board.

4.4.2 Designing TRL standards

To properly design a set of TRL standards, it is necessary to know the substrate parameters, the desired characteristic impedance of the transmission lines, and a desired center frequency. Three standards are then created, a thru line, an open line and a delay line. The measurement reference plane is set by the lengths of the thru and the open line; specifically the reference plane is established at the midpoint of the thru line. Let the length of the thru line be, I_{thru}, then the nominal length of the delay line is given by

$$I_{delay} = I_{thru} + I_{\lambda/4} \qquad \text{[4-16]}$$

where $I_{\lambda/4}$ is a quarter wavelength at the center frequency.

For an EM wave propagating down a microstrip transmission line, part of the electric field is the substrate (dielectric) and the other part is in air. This disparity in dielectric constant values requires the set of an effective dielectric constant, which can be approximated by

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} \qquad \text{[4-17]}$$

Where ε_r is the substrate relative dielectric constant. We can now define the equation for the wavelength of the wave propagating on the transmission line (guide wavelength)

$$\lambda_g = \frac{c}{f\sqrt{\varepsilon_{eff}}} \qquad \text{[4-18]}$$

where c is the speed of light in a vacuum and f is the design frequency.

A detailed discussion on the TRL calibration method and the design of the calibration jig is done in Appendix C.

4.4.3 Measuring the s-parameters

A vector network analyzer is used to measure the s-parameters of the different standards. The extraction of the s-parameters of the device being measured are calculated externally with a simple MATLAB algorithm [50].

In order to verify the accuracy of the TRL calibration, four measurements are done. The thru, line and reflect measurements are made as well as another line measurement to represent the device being measured.

The results of the above mentioned setup is indicated in Fig. 4-5.
As can be seen from the results the, TRL-calibration will have an improvement in measurements. The reflections measured are below –50 dBm which is very good.

The confidence we have in the measuring setup allows us now to measure the s-parameters of a diode.

It is important to have a close understanding of the model that will be extracted and the behavior of the device at different frequencies and bias currents. The understanding is needed in deciding on a frequency span and bias current that will exploit the behavior of the elements of the model.

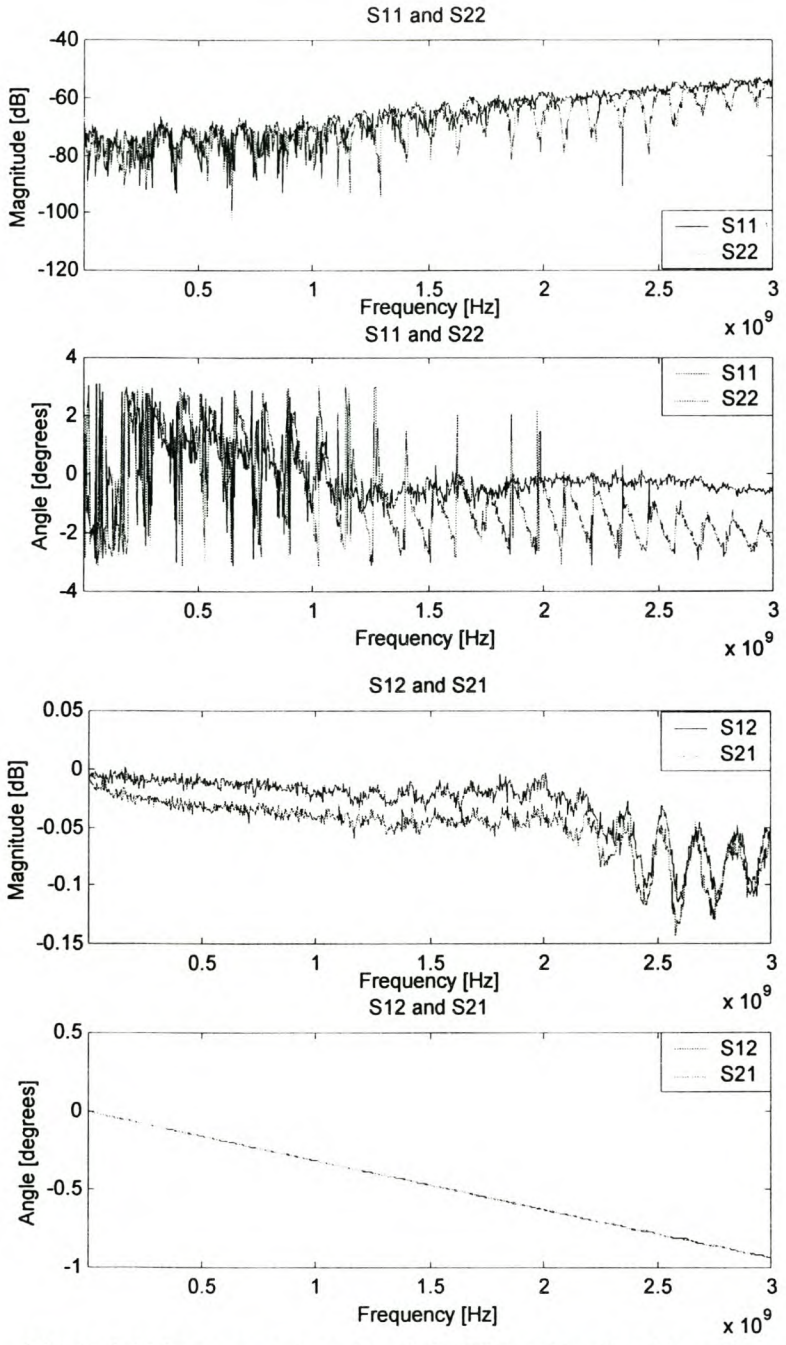


Figure 4-5 The measured results of the TRL calibration kit, with a piece of transmission line as the device

Frequency span

By a close examination of the model it is realized that the capacitance (both junction and parasitic) plays an important role at higher frequencies, but is not a major player at lower frequencies. At lower frequencies, the series resistance and junction resistance can be

more easily extracted. The junction resistance and capacitance, however, are both non-linear parameters and need to be characterized over the whole operating bandwidth. Therefore although the behavior of the diode at different frequencies can be used to extract the model-parameters more easily, it is still necessary to consider the whole operating bandwidth when working with the non-linear junction parameters.

Biasing of the Diode
It is possible to exploit the characteristics of the diode even more by controlling the bias current.

4.5 De-embedding the Diode Model

The diode model's parameters can be described by intrinsic and extrinsic parameters. The extrinsic parameters are usually the parasitic values of the diode and are well defined in data sheets. The intrinsic parameters, however, is crucial because it describes the voltage and current in the junction. The junction parameters have a direct influence on the detector performance, because it is the junction that performs the conversion between RF power and voltage output. As a start, the diode's extrinsic parameters can be de-embedded, leaving only the intrinsic parameters. This can be done as indicated in Fig.4-6 The model is seen as a two-port device and the s-parameters are used as the input [26].

The values of the extrinsic parameters (package of diode) are indicated in Table 4-2. These values are a good starting point for the model extraction from small signal measurements. It is also used to do the de-embedding of the model [19].

	Element:	**Ll**	**Cl**	**Cp**	**Ls**
	Description	**Leadframe Inducance**	**Leadframe Capacitance**	**Package Capacitance**	**Bondwire Inductance**
	Units:	**nH**	**pF**	**pF**	**nH**
SOT-23	To 3 GHz	0.5	0	0.08	1
SOT-3x3	To 3 GHz	0.4	0	0.03	0.7
SOT-3x3	To 6 GHz	0.8	0.05	0.03	0.7

Table 4-2 The extrinsic parameter values of the diodes used in this thesis

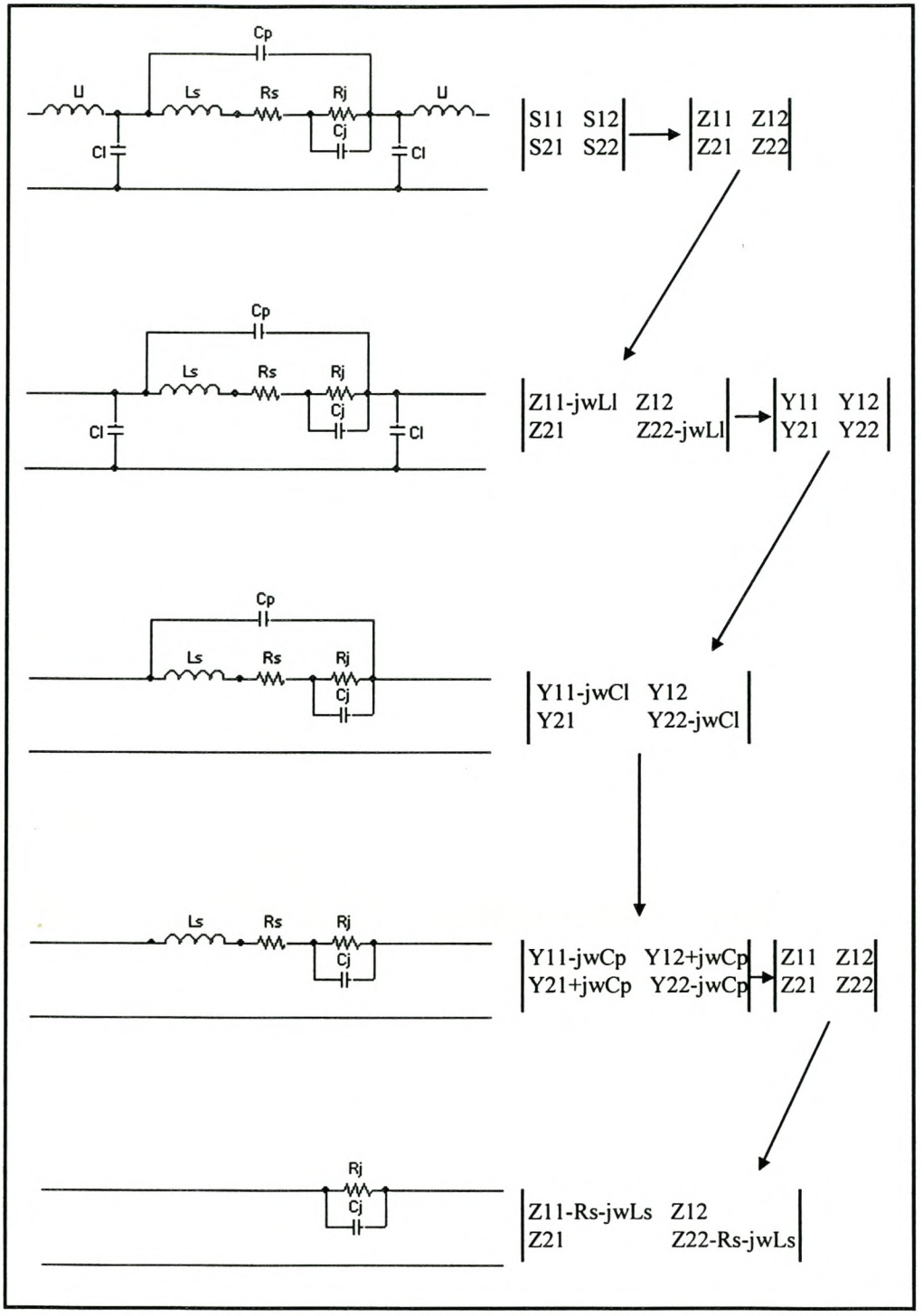


Figure 4-6 The method of de-embedding applied to the packaged Schottky diode

4.5.1 Calculation of Junction Parameters

The ε_k-term of the error function for a parallel R-C branch circuit, that is the weighted difference between measured response Y and calculated impedance at frequency point k, is described by Fujiang Lin [22] as

$$\varepsilon_k = \overline{\omega_k}\left(Y_k - \frac{1}{R} - j\omega_k C\right) \qquad \text{[4-19]}$$

with the weighted function as

$$\overline{\omega_k} = 1/\sqrt{f_k} \ . \qquad \text{[4-20]}$$

It can be derived that

$$C = \frac{1}{2\pi}\frac{\sum_k Y_k''}{\sum_k f_k} \qquad \text{[4-21]}$$

and

$$G = \frac{1}{R} = \frac{\sum_k Y_k'/f_k}{\sum_k 1/f_k} \ . \qquad \text{[4-22]}$$

If the Schottky diode model is de-embedded to the intrinsic level, the junction resistance and capacitance can be extracted using equations [4-19] to [4-22].

4.5.2 Application to Simulated Data

To prove that this method of de-embedding the diode model is delivering proper results, the method is firstly tested by simulated data. The small signal parameters are created by a simulation package, with the diode represented by its Spice model. The s-parameters are shown in Fig.4-7. No bias current is used, which results in a high input impedance.

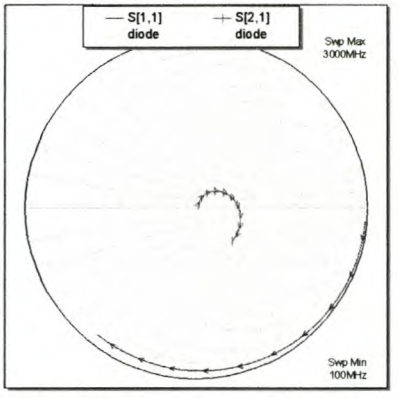


Figure 4-7 The s-parameters of the Spice model created by a simulation package

The de-embedding is done up up to the intrinsic level, as explained in the previous section. The intrinsic parameters can now be calculated by using equations [4-19]-[4-22]. The parameter values of the diode model are indicated in table 4-3.

The lumped parameter model can now be compared to the diode Spice model, to get an indication of the validity of the model. The results are indicated in Fig. 4-8.

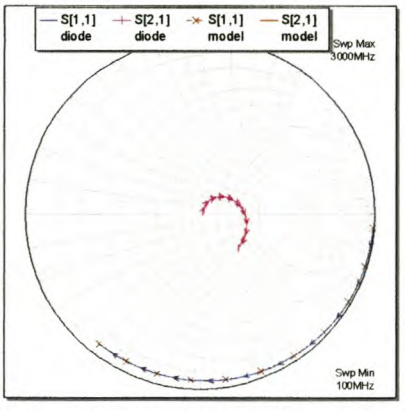


Figure 4-8 The results of the extracted model compared with the Spice model

Parameter	Value
R_j	9987 Ω
C_j	0.178 pF
R_s	25 Ω
C_p	0.08 pF
L_s	1 nH
C_l	1 pF
L_l	1 nH

Table 4-3 The extracted parameters for the simulated data

It can be seen that the intrinsic parameters can be analytically calculated with equations [4-19]-[4-22], if the extrinsic parameter values are well defined. The next step will be to

test the method with measured data, obtained by the TRL-calibration method, as discussed in a previous section.

4.5.3 Application to Measured Data

The success of de-embedding the model lies in the accuracy of the s-parameter measurements as well as the accuracy of the extrinsic parameters obtained from manufacturers data sheets and DC analysis.

The method of only calculating the intrinsic parameters is tested with measured s-parameters of the HSMS-2850 Schottky diode with 35 uA biasing current. The frequency range is 300 kHz to 3 GHz. The s-parameters are extracted by doing the TRL calibration as previously discussed.

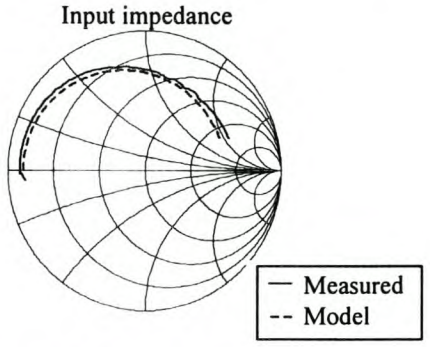


Figure 4-9 The comparison of the measured input impedance with the extracted model

Parameter	Value
R_j	831 Ω
C_j	0.76 pF
R_s	9.5 Ω
L_s	1 nH
C_p	0.08 pF
L_l	1 nH

Table 4-4 The extracted parameters

As can be seen, the method is fairly accurate. The model can still be refined by applying an optimization algorithm to the model and measured data. The parameter values as indicated in table 4-4 can be used as the starting values for optimization.

4.6 Optimization of the Diode Model

The model in Fig.4-10 is presented as the complete diode model with all the parasitic elements included.

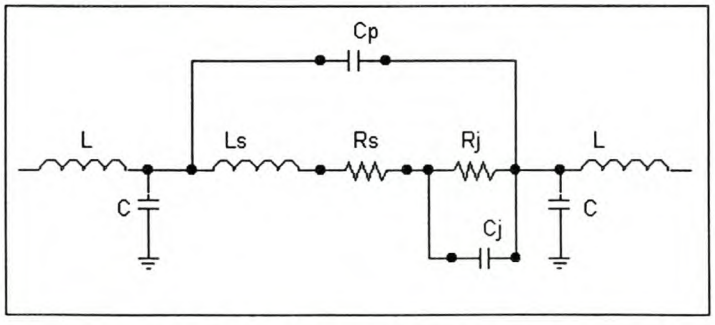


Figure 4-10 Model of Schottky diode with packaging

An optimization program can now be used to extract a more accurate model from the measured s-parameters, using the values already calculated as the starting values for optimization.

The first step in optimizing the model is to determine the sensitivity of each parameter towards the s-parameters. This is done by calculating the s-parameters, while varying a parameter of the model. The change in the error function is effectively calculated for a change in parameter value.

Starting with the most sensitive parameter, each parameter is optimized individually. The method of optimizing all seven parameters at the same time was investigated, but did not deliver satisfactory results.

4.6.1 Determination of Sensitivity of Parameters

The change in the error function was theoretically calculated for a percentage change of each parameter. The percentage change in parameters was held to a maximum of 1 %. The error function is the weighted sum of the squared difference between measured and calculated data.

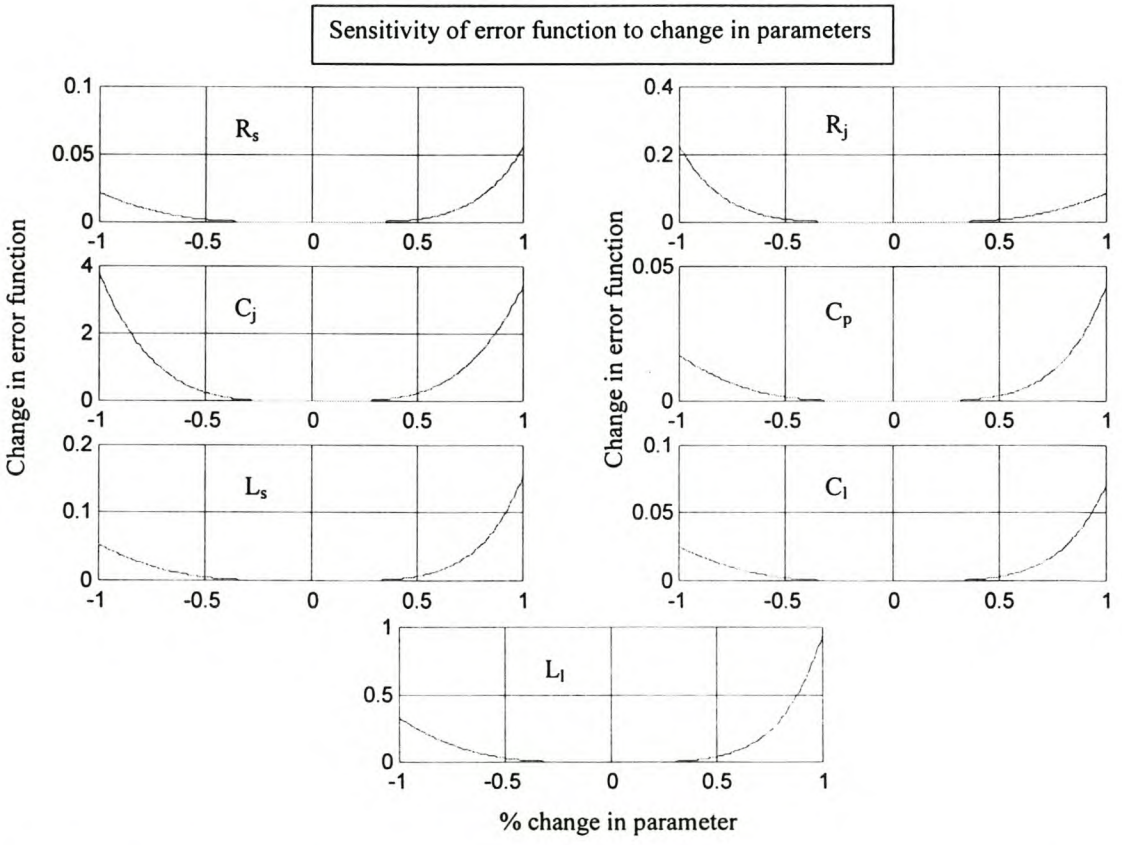


Figure 4-11 The comparison of the sensitivity of the model parameters on the error function

Position	Parameter
1	C_j
2	L_l
3	R_j
4	L_s
5	R_s
6	C_l
7	C_p

Table 4-5 The order of sensitivity of the parameters

4.6.2 The Optimization Algorithm

Newton's algorithm, as discussed in Appendix B, was once again implemented to minimize the error function.

$$error = \sum_{i}^{m} \frac{1}{\sigma_{11}} \left(S_{11}^{c}(i) - S_{11}^{m}(i) \right) + \frac{1}{\sigma_{21}} \left(S_{21}^{c}(i) - S_{21}^{m}(i) \right) \qquad [4\text{-}23]$$

where σ_{11} and σ_{21} are the maximum values of S_{11}^{c} and S_{21}^{c}, respectively. It serves as the weighting function.

The first parameter to be optimized is indicated in table 4-5. Figure 4-12 states the procedure followed to optimize all the parameters.

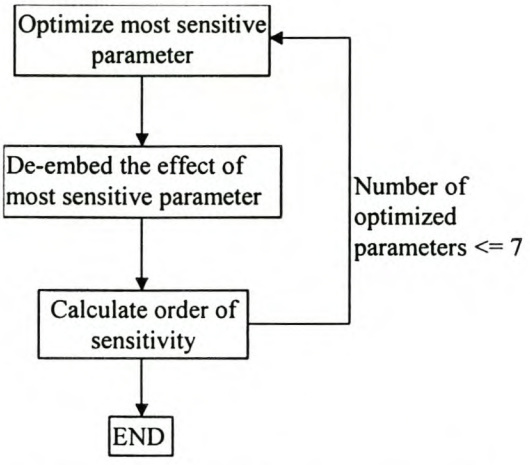


Figure 4-12 The method of optimizing the model parameters

The de-embedding of the model was described in section 4-5, while the sensitivity calculation is done on exactly the same principal as discussed above. The order of sensitivity is calculated after each optimized parameter is de-embedded.

4.6.3 Results

The results of the optimization algorithm can be seen in Fig. 4-13 and table 4-6.
The algorithm has improved the response of the Schottky diode model over the lower frequency band, but not as much at the higher frequencies. The reason for this may be that C_L is not included in this model. It is only included for models extracted for frequencies above 6 GHz. This will definitely affect the behavior at higher frequencies.

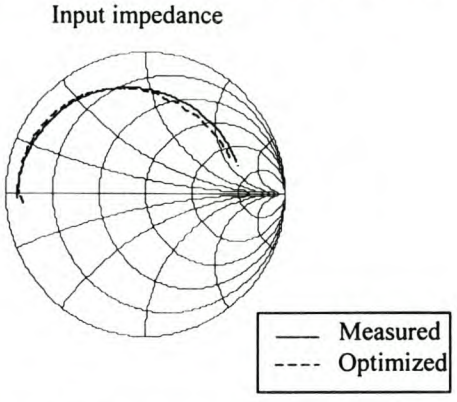


Figure 4-13 The comparison of the measured input impedance to the optimized model

Parameter	Optimized Value
R_j	1149 Ω
C_j	0.782 pF
R_s	6.383 Ω
L_s	1.076 nH
C_p	0.0821 pF
L_l	0.9568 nH

Table 4-6 The optimized model parameters

The change in the parameter values to obtain this slight improvement is not significant due to the small difference between the optimized parameters and the original extracted ones. The optimization algorithm can, however, be useful if the method of de-embedding is not successful.

4.7 Examples of Parameter Extraction

The method of parameter extraction, as discussed in this chapter, was implemented on the Schottky diodes selected in chapter 2. Where applicable, the verification of the behavior of the nonlinear elements (R_j and C_j) according to the discussed equations is also done. The calculated results are tabulated.

4.7.1 HSMS-2810

These Schottky diodes are specifically designed to feature very low flicker noise. For the purpose of this thesis, the HSMS-2810 is characterized up to 3 GHz.

The optimized results for the DC extraction as well as the small signal parameter extraction method are indicated in table 4-7. It is compared with the Spice parameters from the data sheets.

Parameter	Optimized	Extracted	Spice
I_s	2.11e-8	2.06e-8	4.8e-9
R_s	12.82	12.85	10
N	*	*	1.08
E_G	*	*	0.69
C_{jo}	0.81e-12	0.73e-12	1.1e-12
V_j	*	*	0.65
α	29.81	29.9	*

Table 4-7 Schottky diode parameters for HSMS 2810

(* parameter that is not extracted from measurements)

The extracted and Spice parameters of the HSMS 2810 Schottky diode are in reasonable good agreement. The extracted saturation current does differ a bit from the value obtained from its data sheets, but it will not influence a biased detector design seriously.

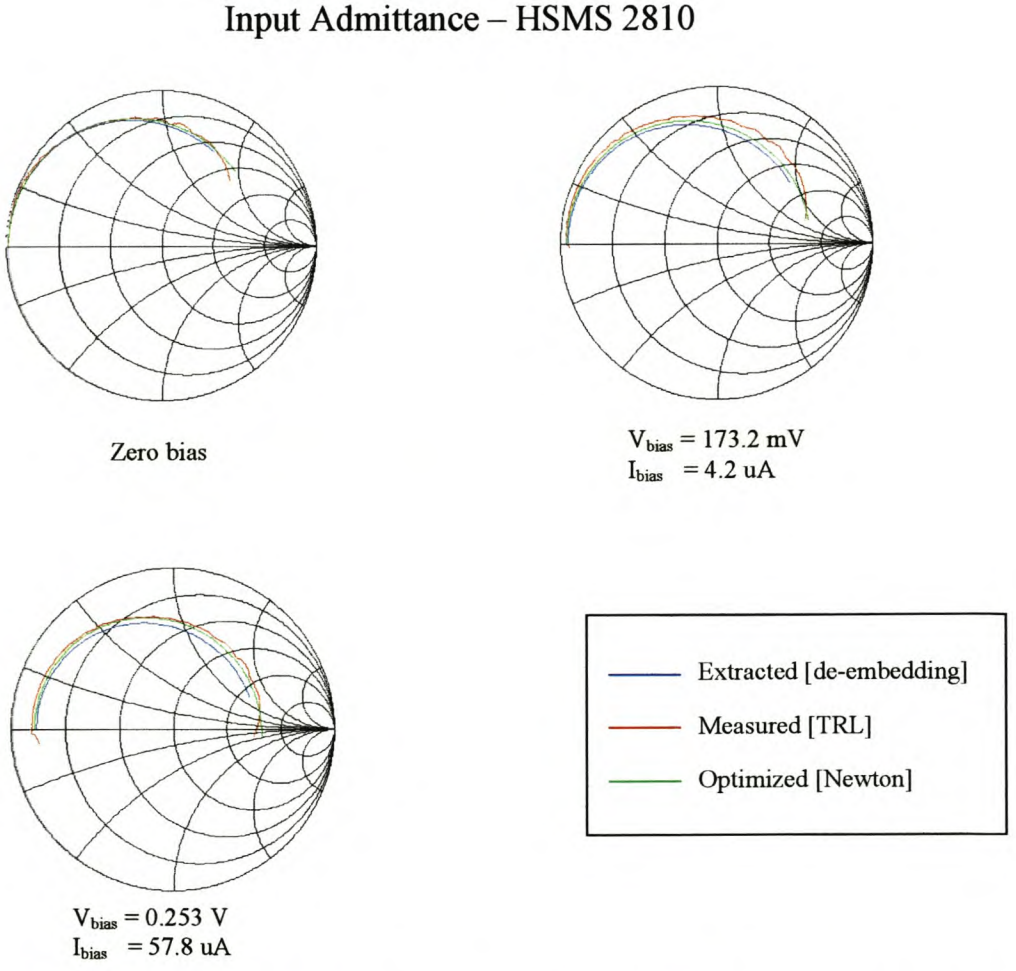


Figure 4-14 The comparison of the measured input admittance to the extracted one for the HSMS 2810 diode

The extraction of the intrinsic junction parameters was done by means of the de-embedding procedure previously discussed. These values were optimized with the Newton algorithm to obtain the values expressed in table 4-8.

A comparison of the input admittances for the measured, extracted and optimized procedures is indicated in Fig. 4-14 for different bias currents. It can be seen that there is a very good agreement between the extracted model and the measured one.

Bias current (A)	R_j [opt.] (Ω)	R_j [calc.] (Ω)	C_j [opt.] (F)	C_j [calc.] (F)
Zero	185.97e3	1.323e6	0.81e-12	0.81e-12
4.2e-6	2.635e3	6.61e3	1.05e-12	1e-12
57.8e-6	672.2	482.85	1.25e-12	1.15e-12

Table 4-8 The effect of bias current on the extracted and calculated intrinsic parameters – HSMS 2810

The calculated values from table 4-8 were obtained from equations [3-3] and [4-3]. The junction capacitance values are in good agreement with the extracted ones. The junction resistance does differ quite severely at very low bias currents. The reason for this is the difference between the data sheet and extracted saturation current. At higher bias currents the effect of I_s gets smaller and the comparison in junction resistance improves. If a biased detector is therefore designed, the design equations describing the junction parameters can be used with confidence. However, if a zero biased detector is designed, it is advisable to extract the junction parameters, especially the junction resistance. This will be demonstrated with HSMS 2850 Schottky diode, which is a zero bias diode.

4.7.2 HSMS-2820

This series of Schottky diodes is the best all-round choice for most applications, featuring low series resistance, low forward voltage at all current levels and good RF characteristics. The diode model is extracted for frequencies up to 3 GHz.

A comparison between the extracted and Spice parameters, obtained from the DC and small signal extraction method are once again indicated in table 4-9.

Parameter	Optimized	Extracted	Spice	Units
I_s	1.97e-8	1.93e-8	2.2e-8	A
R_s	13.05	13.05	6	Ω
N	*	*	1.08	
E_G	*	*	0.69	eV
C_{jo}	0.89e-12	0.86e-12	0.7e-12	F
V_j	*	*	0.65	V
α	30.27	30.34	*	

Table 4-9 Schottky diode parameters for HSMS 2820

(* parameter that is not extracted from measurements)

The parameter values are, once again, in good agreement and provide a good fit with the diode's DC characteristics. The only relative big difference between the extracted values and the values provided by the manufacturer is the series resistance value. This resistance will influence the detector design, especially at the lower frequencies. R_s is slightly dependent on bias current and temperature, but usually it is acceptable to ignore these effects. It is, however, possible that this can be the reason for the difference in value.

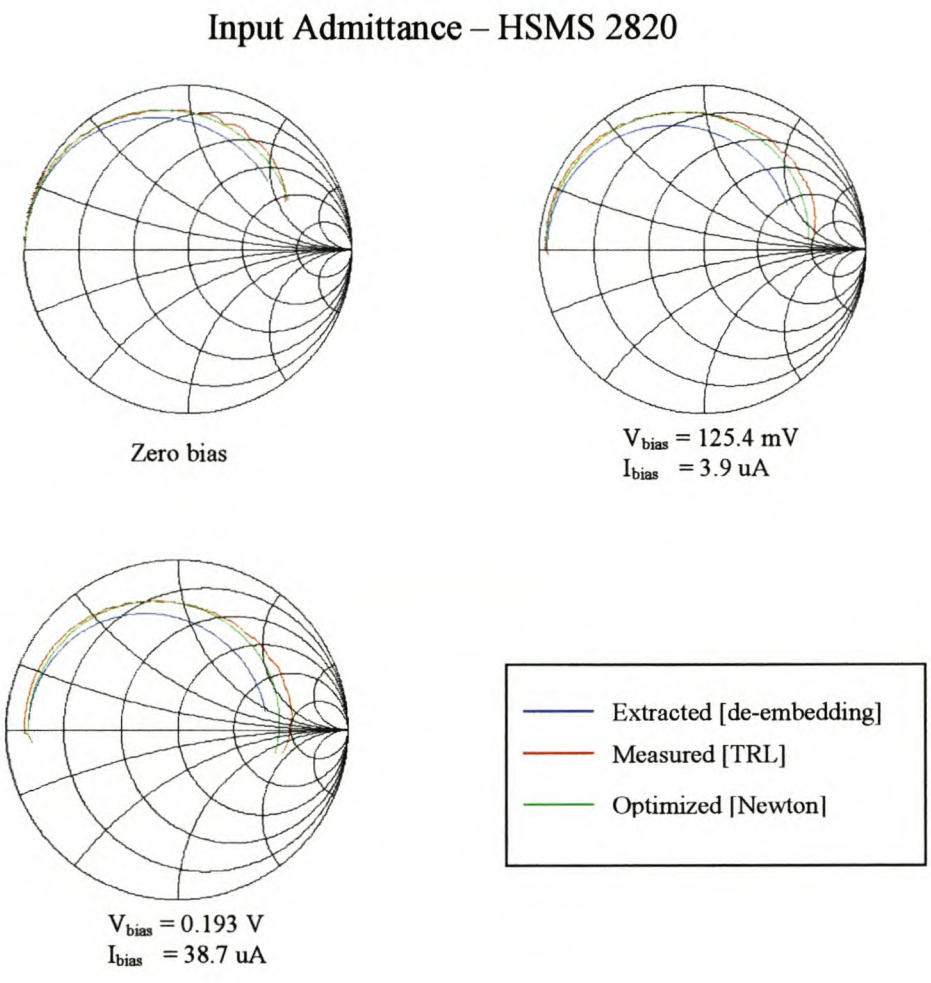


Figure 4-15 The comparison of the measured input admittance to the extracted one for the HSMS 2820 diode

The extraction of the intrinsic junction parameters were done by means of the de-embedding procedure and refined by using the optimization algorithm of Newton. The results are indicated in table 4-10.

A comparison between the extracted, measured and optimized input admittances for the HSMS 2820 diode at different bias current gives satisfactory results. (Fig. 4-15)

Bias current (A)	R_j [opt.] (Ω)	R_j [calc.] (Ω)	C_j [opt.] (F)	C_j [calc.] (F)
Zero	115.1e3	1.417e6	0.89e-12	0.89e-12
3.9e-6	2.542e3	7.12e3	1.05e-12	0.99e-12
38.7e-6	768.3	721.05	1.29e-12	1.06e-12

Table 4-10 The effect of bias current on the extracted and calculated intrinsic parameters – HSMS 2820

The calculated parameters in table 4-10 are obtained from equations [3-3] and [4-3]. The differences between the extracted values and optimized ones are in the same order as for the HSMS 2810 diode. The explanation in section 4.7.2 is also valid. An increase in bias current improves the similarity.

4.7.3 HSMS-2850

This family of zero bias Schottky diodes has been designed and optimized for use in small signal applications. For the purpose of this thesis, the HSMS-2850 is characterized up to 3 GHz.

A comparison between the extracted (obtained from measurements) and Spice (obtained from data sheets) parameters are indicated in table 4-11.

Parameter	Optimized	Extracted	Spice	Units
I_s	2.06e-5	2.06e-5	3e-6	A
R_s	23.64	23.64	25	Ω
N	*	*	1.06	
E_G	*	*	0.69	eV
C_{jo}	0.13e-12	0.202e-12	0.18e-12	F
V_j	*	*	0.35	V
α	17.75	17.74	*	

Table 4-11 Schottky diode parameters for HSMS 2850

(* parameter that is not extracted from measurements)

As in the case for the HSMS 2810 diode, the only parameter that differs to a certain extent from the manufacturers' parameter, is the saturation current. Being a zero biased diode, does effect the influence this will have on the design of a detector.

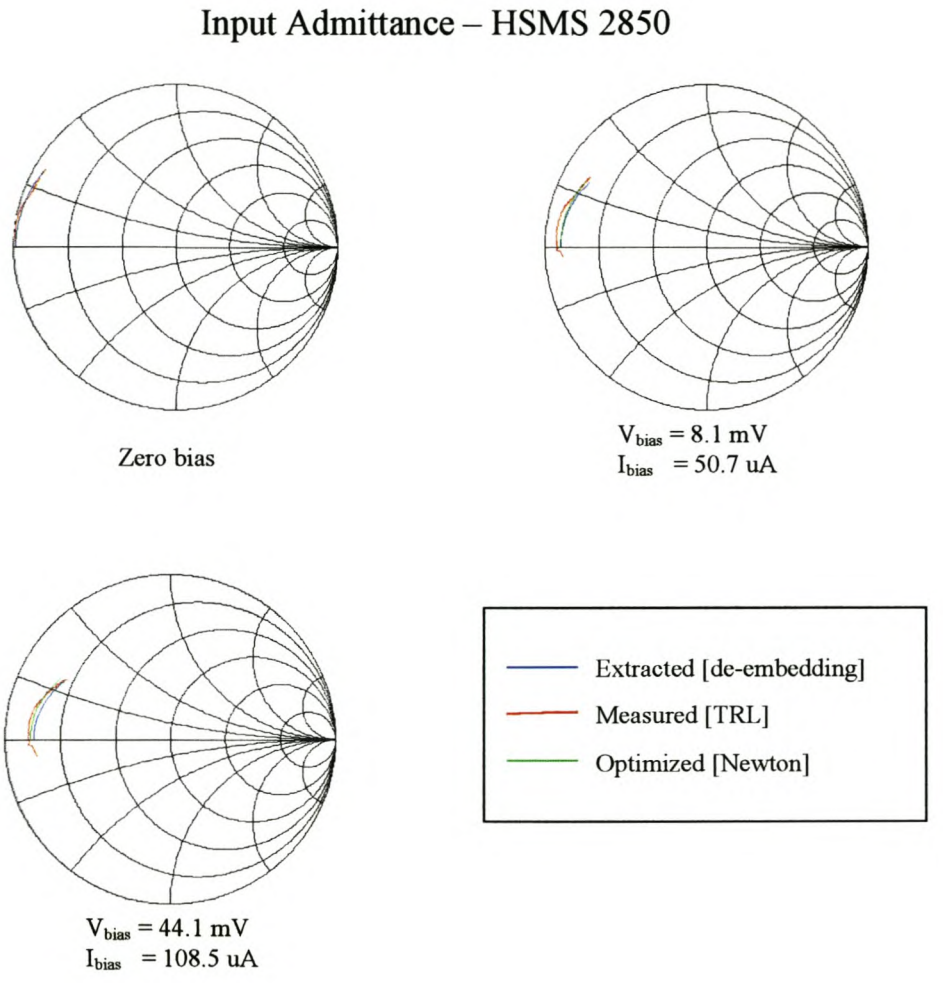


Figure 4-16 The comparison of the measured input admittance to the extracted one for the HSMS 2850 diode

The intrinsic junction parameters were obtained from the de-embedding procedure and the Newton optimization algorithm. The results are shown in table 4-12.

The comparison between the measured, extracted and optimized input admittance results in fig 4-16 gives satisfactory results for different bias currents.

Bias current (A)	R_j [opt.] (Ω)	R_j [calc.] (Ω)	C_j [opt.] (F)	C_j [calc.] (F)
Zero	14.28e3	1.35e3	0.13e-12	0.13e-12
50.7e-6	981.12	391.57	0.16e-12	0.13e-12
108.5e-6	611.35	216.26	0.22e-12	0.14e-12

Table 4-12 The effect of bias current on the extracted and calculated intrinsic parameters – HSMS 2850

The calculated parameters in table 4-12 were obtained from equation [3-3] and [4-3]. The junction capacitance is once again in good agreement with its extracted value, but the difference in junction resistance is not acceptable. The HSMS 2850 diode is a zero biased diode and therefore no bias current is used. It is advisable to use the extracted values for the intrinsic parameters, instead of the manufacturers' values indicated on the diode's data sheets. This will improve the results of the matching circuit to a large extent.

4.7.4 HSMS-8101

This low cost microwave Schottky diode is specifically designed for use at X/Ku bands. For the purpose of this thesis, the HSMS-8101 diode is characterized in the 8-12 GHz band.

The Spice parameters presented in the HP data sheets are indicated in table 4-13.

Parameter	Optimized	Extracted	Spice	Units
I_s	3.13e-8	2.94e-8	4.6e-8	A
R_s	10.52	10	6	Ω
N	*	*	1.09	
E_G	*	*	0.69	eV
C_{jo}	0.143e-12	0.139e-12	0.18e-12	F
V_j	*	*	0.5	V
α	35.67	35.96	*	

Table 4-13 Schottky diode parameters for HSMS 8101

(* parameter that is not extracted from measurements)

The parameters extracted from the DC IV characteristics are also indicated in table 4-13

To successfully extract the intrinsic parameters from small signal measurements needs more skill. Due to the high frequency range [X-band] it is more difficult to characterize the diode. Temperature effects the measurements and parasitic elements have a bigger influence on results. The model will not be extracted for temperature variance. Temperature effects will be considered for the detector circuit simulations only.

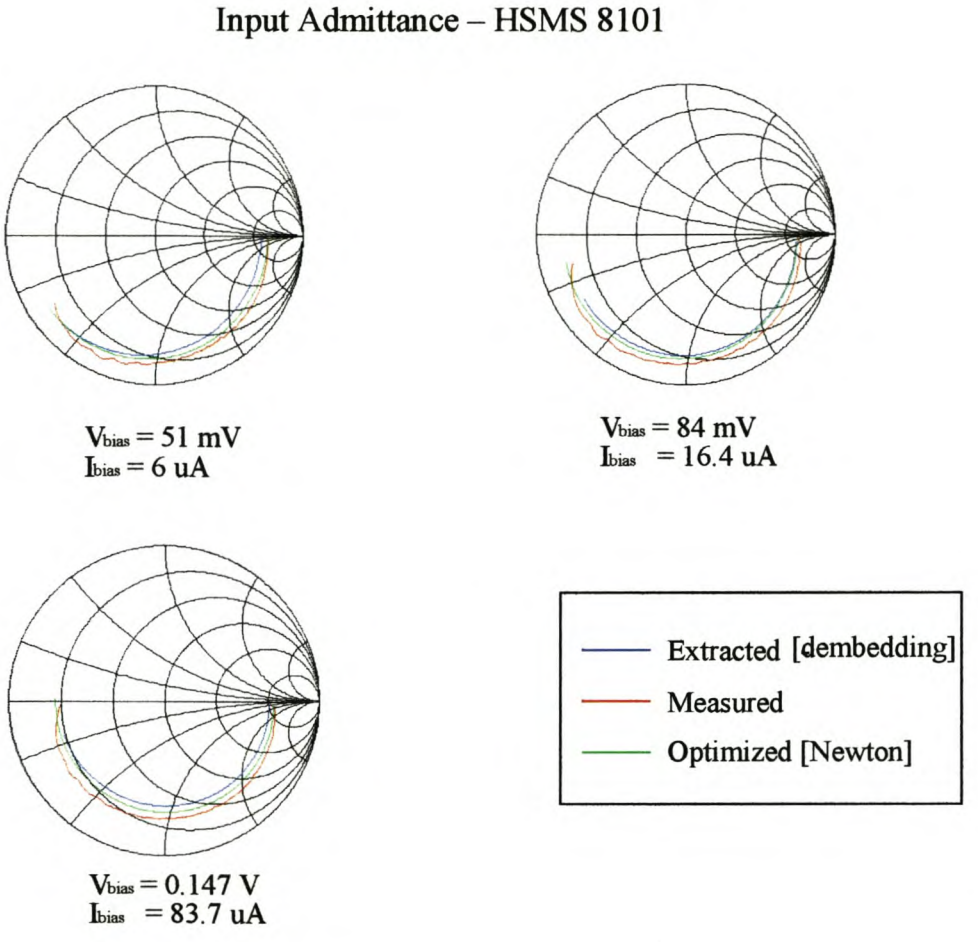


Figure 4-17 The comparison of the measured input admittance to the extracted one for the HSMS 8101 diode

The effect of R_s and R_j will be more at the lower frequencies, while the other parasitic parameters will have a larger influence at the higher frequencies. This was discussed in chapter 2.

Bias current (A)	R_j [opt.] (Ω)	R_j [calc.] (Ω)	C_j [opt.] (F)	C_j [calc.] (F)
6e-6	4.23e3	4.62e3	0.143e-12	0.151e-12
16.4e-6	2.21e3	1.7e3	0.146e-12	0.156e-12
83.7e-6	651	333.4	0.166e-12	0.17e-12

Table 4-14 The effect of bias current on the extracted and calculated intrinsic parameters –HSMS 8101

The calculated values in table 4-14 are once again obtained from eq [3-3] and [4-3]. The calculated values compares reasonably well with the extracted values. The difference will not lead to gross differences in design and simulation applications.

4.8 Conclusions

It is shown that the characterization of the Schottky diode by means of a Schottky diode model can be done from DC and small signal measurements.

The method of de-embedding the extrinsic parasitic parameters is used to calculate the nonlinear intrinsic junction parameters. The method is very successful if the parasitic parameters are known from data sheets.

The method is extended further with the addition of an optimization algorithm to improve the extracted model. The poor sensitivity of some of the parameters prevent the optimization algorithm of convergence. By optimizing each parameter individually, from the most sensitive to the least sensitive parameter, good results are obtained. The effect of each optimized parameter is de-embedded, before optimizing the next.

The design equations, describing the nonlinear junction parameters, are fairly accurate in predicting the values, although at very low biasing levels (and zero bias) it is advised to use the extracted parameters.

The models extracted for the diodes used, proves that the Schottky diode model can be successfully extracted through measurements.

5 The Design of Matching Circuits

The most crucial part in the design of diode detectors is the matching circuit. It influences the sensitivity and dynamic range of the detector to a large extent. A poorly matched detector will have an understandably disappointing small signal performance. In this chapter, some design techniques will be investigated and applied to practical detector circuits. In most cases the designer must make the decision between the importance of sensitivity and VSWR. In small signal detectors, sensitivity is very important. In large signal detectors it is not that crucial. The matching circuitry for large signal detectors is therefore much easier to design or does not need design at all.

5.1 Background

The use of tables for designing impedance matching filters for real loads is well known. Simple complex loads can often be matched by this technique by incorporating the imaginary portion of the load into the first element. This technique is rarely useful for matching diodes, because the equivalent circuit for the diode must include several real and imaginary elements. The diode is represented by its extracted or Spice model. A narrowband or wideband matching technique can be used to match the detector circuit. The use of Chebyshev filters for matching purposes was also examined, but is discussed in Appendix D [46].

5.2 Calculation of the Input Impedance of a Diode

In order to design a good matching network, the input impedance of the diode must be accurately calculated. It is done by using the diode model as building block. Both the Spice- and the extracted model, from DC – and small signal measurements, are used.

The input impedance of a diode is a function of power absorbed. The diode impedance will change when a matching circuit is added. A matching circuit designed for a diode with for example one milliwatt incident power would be incorrect for a diode absorbing one milliwatt. That is why the rectified or bias current is monitored. A diode model is extracted or calculated for a specific bias current.

To calculate the input impedance is simple (see Fig. 4-10)

$$Z_{in} = (Z_{R_j} \parallel Z_{C_j} + R_s + Z_{L_s}) \parallel Z_{C_p} \qquad \textbf{[5-1]}$$

The values of the parameters in eq [5-1] is calculated or extracted at a specific bias current. The calculation of an optimum bias current will be discussed in chapter 6.

From [5-1] the Y-parameters can be calculated

$$Y11 = {}^{1}\!/_{Z_{in}}$$

$$\begin{aligned} Y21 &= -Y11 \\ Y22 &= Y11 \\ Y12 &= Y21 \end{aligned} \qquad \textbf{[5-2]}$$

The effect of other extrinsic parameters, for example connectors, will influence the Y-or Z-parameters as calculated above
[see figure 4-10]

$$\begin{aligned} Y11 &= Y11 + G \\ Y22 &= Y22 + G \end{aligned} \qquad \textbf{[5-3]}$$

where G is the admittance of the extrinsic capacitance C_L.

To add the extra inductance, the Y-parameters are converted to Z-parameters [16].

$$Z11 = \frac{Y22}{Y11.Y22 - Y12.Y21}$$

$$Z21 = \frac{-Y21}{Y11.Y22 - Y12.Y21}$$

$$Z12 = \frac{-Y21}{Y11.Y22 - Y12.Y21}$$

$$Z22 = \frac{Y11}{Y11.Y22 - Y12.Y21} \qquad \textbf{[5-4]}$$

The impedance of the extrinsic inductance can now be added

$$\begin{aligned} Z11 &= Z11 + Y \\ Z11 &= Z11 + Y \end{aligned} \qquad \textbf{[5-5]}$$

where Y is the impedance of the extrinsic inductance L_L.

The Z-parameters can then be converted back to Y-parameters [16].

$$Y11 = \frac{Z22}{Z11.Z22 - Z12.Z21}$$

$$Y12 = \frac{-Z12}{Z11.Z22 - Z12.Z21}$$

$$Y21 = \frac{-Z21}{Z11.Z22 - Z12.Z21}$$

$$Y22 = \frac{Z11}{Z11.Z22 - Z12.Z21} \qquad [5\text{-}6]$$

Y11 is the parameter that will be matched to the source input impedance, usually 50 Ω.

5.2.1 The Modeling of Transmission Lines for Matching

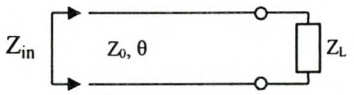


Figure 5-1 Transmission line parameters

The immittance of a transmission line is given by [39]

$$Zin = Z_0 \frac{Z_L + jZ_0 \tan(\theta)}{Z_0 + jZ_L \tan(\theta)}$$

$$Yin = Y_0 \frac{Y_L + jY_0 \tan(\theta)}{Y_0 + jY_L \tan(\theta)} \qquad [5\text{-}7]$$

For an open-circuited line, $Z_L = \infty$ and $Y_L=0$, hence

$$Zin_0 = -jZ_0 \cot(\theta)$$
$$Yin_0 = jY_0 \tan(\theta) \qquad [5\text{-}8]$$

For a shorted line, $Z_L=0$ and $Y_L=\infty$, hence

$$Zin_s = jZ_0 \tan(\theta)$$
$$Yin_s = -jY_0 \cot(\theta) \qquad [5\text{-}9]$$

where Z_L , Y_L are the load impedance and admittance and Z_0 , Y_0 are the characteristic impedance and admittance of the transmission line, respectively.
θ is the electrical length of the transmission line

Eq [5-7] to [5-9] is implemented in MATLAB to design the matching network, for a load admittance calculated as discussed before.

5.3 Narrowband Matching

The simplest type of impedance matching would be to match at the center frequency and accept the results at other frequencies. This technique will be explained by means of an example. The HSMS-2850 will be considered which is a zero bias Schottky diode.

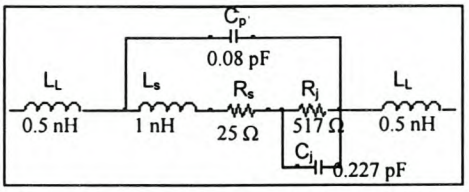
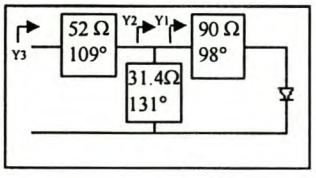


Figure 5-2 The Schottky diode model for the HSMS-2850 zero bias diode

The input impedance (or admittance as plotted in Fig. 5-3) is calculated as discussed in section 5.2, over a frequency span between 900 MHz and 930 MHz.



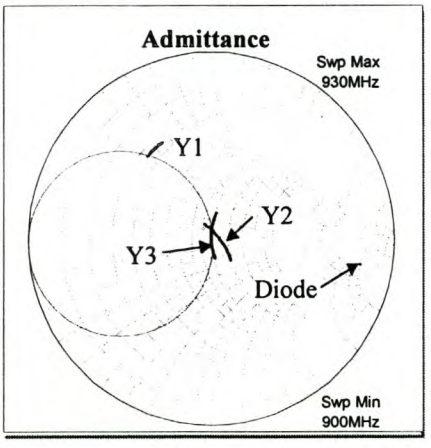


Figure 5-3 The narrowband matching technique for Schottky diodes

The first step in doing a narrowband match, is to add a piece of transmission line in series with the diode, resulting in position Y1 on the Smith chart in Fig. 5-3. Y1 is on the unity real circle.

The second step is to add a transmission line shunted to ground, pulling the admittance to Y2 on the same figure.

The third and final step centers the theoretical mismatch and functions as an input line to the connector.

5.4 Broadband Matching

Broadband design techniques must consider the entire frequency band in the matching procedure. It is usually sufficient to work with the center and end frequencies. A two-step procedure is as follows [25]

- First a length of series transmission line is added to the diode to make the conductance at band edges equal to the inverse of the conductance at resonance.
- The other element in the matching circuit is a shunt resonant transmission line shorted to ground, to bring the band edges together. Characteristic impedance and length are best determined by solving the resonance equations at band edge frequencies.

The easiest way to explain this technique properly will be by means of an application example. Let us consider an extracted Schottky diode model shown in Fig.5-4 in the 8-12 GHz frequency band.

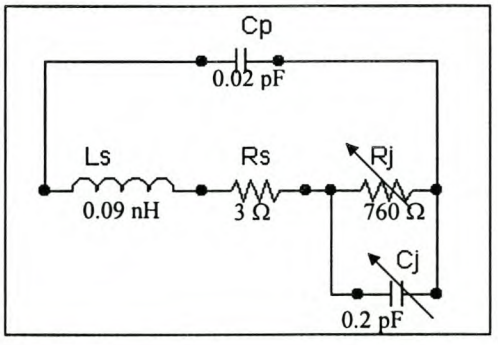


Figure 5-4 The Schottky diode model for a wideband match

Fig.5-5 shows the three steps in the matching procedure for the detector diode. The two-step matching technique as mentioned above was implemented in MATLAB as a wideband-matching algorithm.

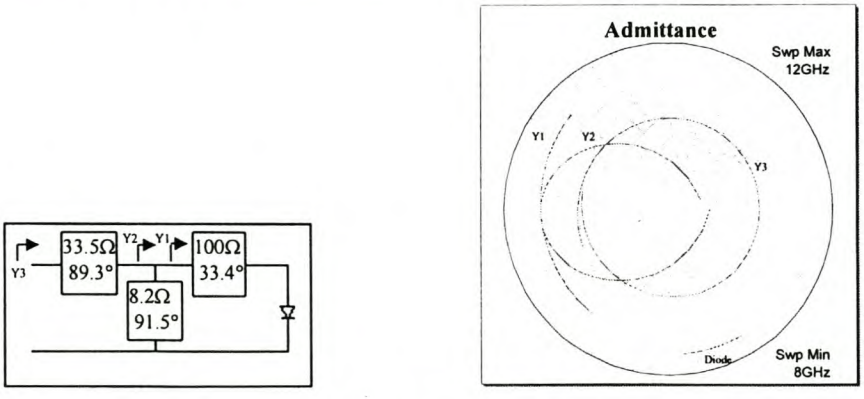


Figure 5-5 The wideband matching technique for Schottky diodes

The first step, as mentioned above, is to add a piece of transmission line, with characteristic impedance and an electrical length as indicated in Fig.5-5, to the diode. The Y1 curve in Fig.5-5 is reached, obtaining equal conductance at the band edges and the inverse of this value at the center frequency. It is not always possible to make the center frequency conductance equal to the inverse of the band edge frequencies. There can, however, be compensated for this by adding a third step to the procedure as will be discussed below. A short circuit transmission line stub is used to resonate the band edges. The reason for using a short circuit and not an open circuit stub is to create a DC return path for the diode. A short circuit is also better defined than an open circuit, which is a deciding factor.

The characteristic impedance and electrical length are calculated by solving the resonance equations [5-7]-[5-9]

$$\frac{50}{Z_0 \tan\theta} + X_1 = 0$$

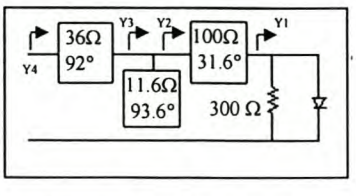
$$\frac{50}{Z_0 \tan(k\theta)} + X_2 = 0 \qquad \textbf{[5-10]}$$

where X_1 and X_2 are the normalized conductance at the band edges and
k is the relationship between the band edges ($k=f_{high}/f_{low}$)
Z_0 is the characteristic impedance of the stub
θ is the electrical length of the stub

Eq [5-10] must be solved simultaneously to calculate Z_0 and θ.

Y2 is reached in Fig. 5-5. The final step is to add another piece of transmission line to center the matching curve on the smith chart, reaching Y3 in Fig. 5-5

A good starting value for the characteristic impedance, of the third piece of transmission line, is found by estimating the final value of center frequency conductance and calculating the geometric mean of this value and the value at Y2. The final value may be estimated by assuming the final admittance plot will have the same diameter on the Smith Chart as Y2 [25].



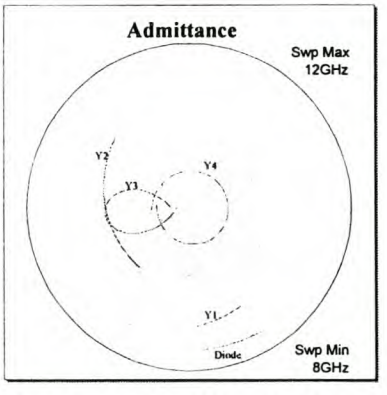


Figure 5-6 The wideband matching technique for Schottky diodes with a shunt resistance

Although the maximum VSWR obtained in this example is adequate for many detector applications, a smaller reflection coefficient is required in some cases in order to avoid deterioration of performance of adjacent circuits. It is often permissible to sacrifice some sensitivity in order to improve the VSWR. This technique is indicated in Fig.5-6. The diode admittance is firstly moved closer to the center of the Smith Chart by adding a 300 Ω resistor across the diode. The three matching elements are then added as before.

Sensitivity may be traded for VSWR by adjusting the value of the shunt resistor. Another technique for reducing mismatch loss in detector diodes is the use of increased bias current. As discussed before, this reduces the junction resistance, and the diode is therefore a better match to 50 Ω.

Unfortunately the reduction of junction resistance increases the loss in the diode series resistance. An increase in bias current also deteriorates the tangential sensitivity, which was discussed in section 2.

5.5 Implementation in MATLAB

The techniques discussed in this chapter are implemented in Matlab.

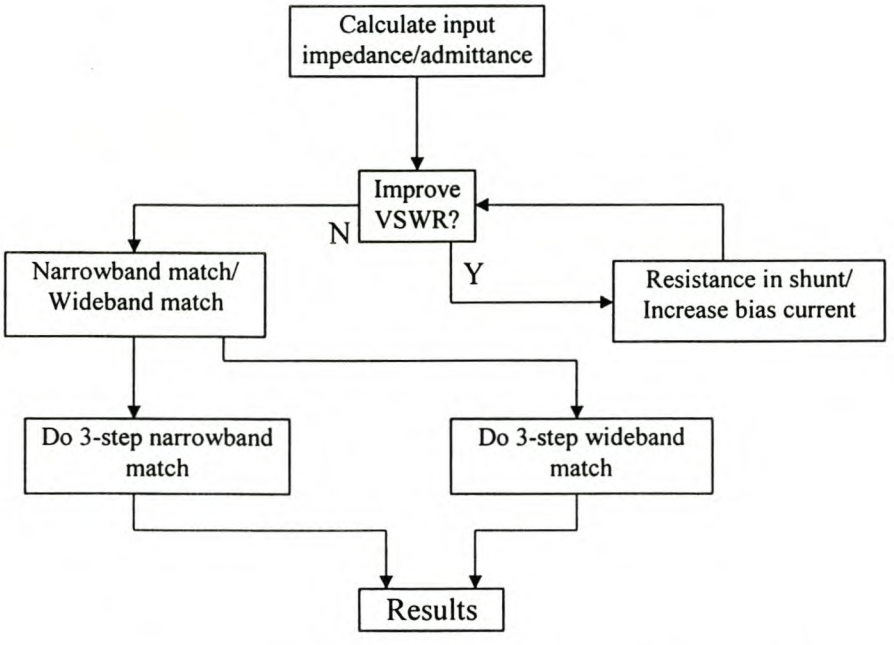


Figure 5-7 Block diagram representation of the matching module

5.6 Resistive Matching for Large Signal Detectors

As mentioned before, detector circuits can be divided into two types, large signal (P_{in} > -20 dBm) and small signal (P_{in} < -20 dBm). In general, the large signal detector use resistive impedance matching at the input to improve flatness over the frequency band. This is possible since the input signal levels are high enough to produce adequate output voltages without the need for a high Q reactive input matching network. These circuits are self-biased therefore no external DC bias is needed.

5.7 Conclusion

It is clear that although the matching of a detector circuit seems quite simple, there is much to consider when designing the circuit. The matching circuit influences the small signal performance of the detector to a large extent. When matching for a flat response over a wide band there are a few prices to pay. Firstly a deterioration of the sensitivity of the detector is on line. This can be due to the extensive use of bias current to improve the VSWR, or the addition of a shunt resistance to the diode. Both of these methods have a negative influence on the sensitivity of the detector. The reasons were discussed in this chapter and previous ones. A second parameter that is affected is the TSS. An extensive use of bias current introduces flicker noise in the diode, deteriorating the smallest signal to be measured (TSS). The use of a shunt resistance also affect this parameter, because of the power lost in the resistor instead of being converted to a measurable output voltage.

Taking everything into consideration, if reflections are a serious threat to other circuits in the system design, it is worth it to improve the VSWR by techniques as discussed above. However, if this is not the case and operation specifications are well met with the original design, especially if the design is narrow band, a perfect wideband match is not crucial. The extensive use of bias current or the use of a shunt resistance will not necessarily result in an improvement in performance.

6 The Design of Diode Detectors

6.1 Introduction

The design of various types of detectors will be discussed in this chapter. For example zero biased detectors, small signal detectors with maximum sensitivity or maximum bandwidth, as well as large signal detectors.

The first four chapters covered the theory of Schottky diodes and its behavior; how to extract a reliable model for the diode; the performance characteristics and behavior of Schottky detectors; some design features and equations; different matching techniques for narrowband and wideband matching. Simulations and measurements were done on examples to highlight certain behaviors and extreme cases. In this chapter all the knowledge and experience obtained in the previous chapters are combined in a MATLAB algorithm for detector design.

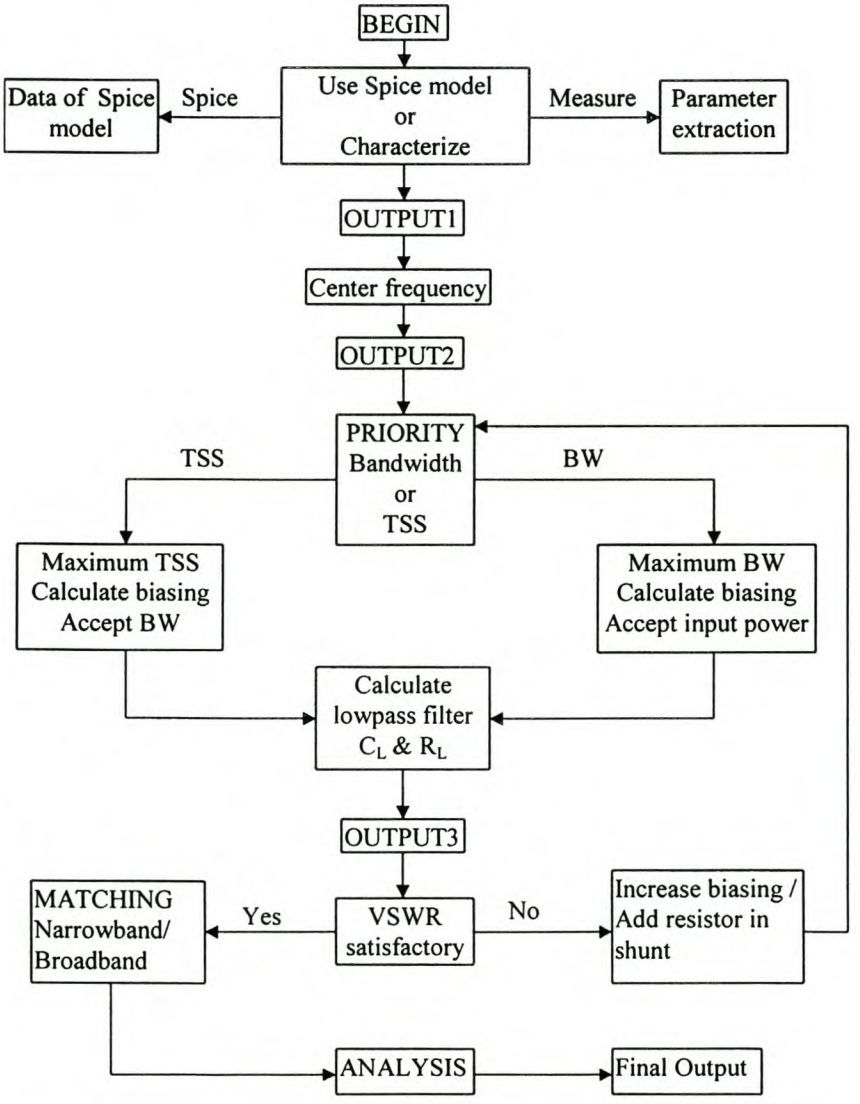


Figure 6-1 Block diagram of the algorithm to design diode detectors

NAME	OUTPUT DATA
OUTPUT1	IV curve; R_j, C_j
OUTPUT2	TSS
OUTPUT3	Sensitivity; VSWR
Final Output	V_{out}, Sensitivity

Table 6-1 Description of output results produced by the detector design algorithm

6.2 Bias Current

Apart from the design of the matching circuit of a diode detector, the design of the bias current has the largest influence on a detector's performance. The bias current influences the voltage sensitivity, tangential sensitivity, bandwidth and input impedance (therefore the VSWR).

It is necessary to make one important decision when designing diode detectors. That is, whether you want to design a detector with maximum bandwidth or maximum TSS (in other words dynamic range) or maximum sensitivity. Both cases are considered.

6.2.1 Design for Maximum TSS

The design of the bias current for maximum TSS is largely based on two equations presented in chapter 3. The equation for TSS, eq [3-1], and the equation expressing voltage sensitivity, eq [3-8]. There is of course also the option to use a zero biased diode in which case the design of bias current can be neglected.

Considering eq [3-1] it can be shown that there is a value of bias current for which the detector will have a maximum TSS. This can be calculated by finding the local minimum of eq [3-1].

The calculation is not a straightforward differential due to the complexity of the equation. The calculation is done with a simple algorithm performing a linear search. The search-region is divided into a minimum of five sections. The average value of each section is calculated, keeping the section with the smallest average. This is done repeatedly until the minimum value and corresponding external bias current is found.

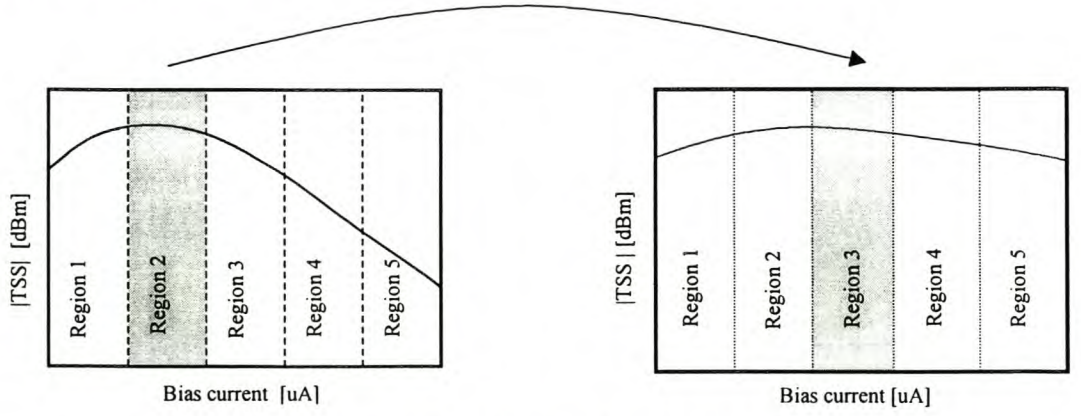


Figure 6-2 Graphical representation of the calculation of the minimum TSS

If we assume that the output amplifier contributes negligible noise compared to the diode, R_A can be neglected in eq [3-1]. Differentiating this simplified expression yields an approximate value of the optimum bias as [23]

$$I_d(opt)_{uA} = R_s(\Omega)[C_j(i)_{pF}]^2[f_{GHz}]^2 \qquad \textbf{[6-1]}$$

6.2.2 Design for Maximum Bandwidth

In the design for maximum bandwidth a different approach is necessary, because matching together with the output circuit, are the limiting factors in this design and not the bias current.

If the designer wants to put a limit on the input power to the detector, a bias current can be calculated that will result in maximum bandwidth. This can be done by once again using eq [3-1]. With bandwidth as the subject of the equation and bias current as the unknown, a linear search can be performed, as before, resulting in maximum bandwidth in correspondence with the bias current.

As mentioned before, the current is not the limiting factor, the output circuit and the matching circuit are. This is discussed in chapter 5 and section 6-3.

The design of bias current is done at a specific design chosen temperature, by using the temperature variant variables at the design temperature. The temperature variant variables are I_s and R_j. These characteristics are described by eq [3-13] and [3-14]

The bias current calculated are used to finalize the diode model on which further design is done. The two parameters in the diode model that are directly influenced by the bias current is the junction resistance and capacitance.

6.3 Output Circuit

In the output circuit, R_L represents the load or amplifier input resistance, and C_L represents the amplifier input capacitance as, the stray and cable capacitances that may be present in the output circuit as well as the RF bypass capacitor. These R and C elements will impose a limit on the upper 3 dB cut-off frequency of this circuit, which is given by

$$f_{u(3dB)} = \frac{1}{2\pi R_L C_L}. \qquad \textbf{[6-2]}$$

The R_LC_L time constant can be reduced by reducing all the element values within certain limits. A severe reduction in the value of the bypass capacitance will lead to poor RF isolation and a decrease in the signal level delivered to the diode. The reactance of this capacitor at the operating frequency should be kept less than 10 % of the RF impedance

of the diode. At low RF frequencies and wide bandwidths, this capacitor can be replaced by a low pass filter structure as shown in Fig. 6-3

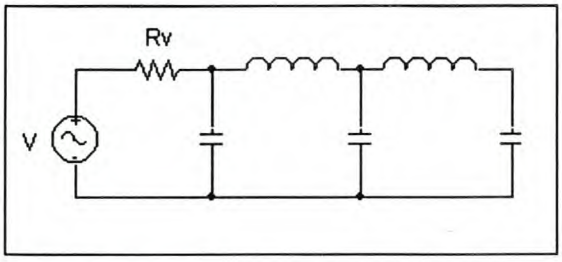


Figure 6-3 A lowpass structure

Alternately, either R_L or R_v can be reduced. The amount that R_L can be reduced is often limited if voltage amplification is desired since the output voltage of the detector is maximized by making R_L large. R_v of the diode can be lowered by increasing the bias current. Although this results in reduced sensitivity, it may be needed to achieve the required bandwidth. A reduction of video resistance has other beneficial effects. It can, for instance, be adjusted to be the optimum source resistance value for a minimum noise figure of the video amplifier. When this is desired, R_v should be adjusted so that [23]

$$R_v = \sqrt{R_{NS} R_{NP}} \qquad \textbf{[6-3]}$$

where R_{NS} is the equivalent series noise resistance of the amplifier and R_{NP} is the equivalent parallel noise resistance of the amplifier.

6.4 Removing the DC Offset

If the detector structure is taken into consideration, one important aspect that has not been discussed, is removing a possible DC offset. A DC offset will be present at the output of the detector due to the diode's biasing. To remove the offset does not have to be a problem. If the detector is operated at very low power levels (Pin < -40 dBm), compensation for the offset is necessary to increase the sensitivity that can be measured. The limitation, however, is on the side of the measuring device and not the detector.

Two possible solutions are presented:
The use of a low noise operational amplifier will remove any DC offset, without adding excessive unnecessary noise to the system. The amplifier must be tuned until a DC value of zero is obtained at the needed input level.

A more system-based solution will be to use a second identical biased diode to drive the low noise operational amplifier. The second diode will have exactly the same properties as the first, for example, temperature effects. This solution, however, means the use of the unconnected pair diode package which is more expensive and sometimes unavailable. [see Appendix G]

6.5 Design Example 1 – 950 MHz

6.5.1 Background

This detector is for use as a field strength meter. The detector is the final building block in the design of the power meter system. It must convert the RF power to a DC voltage that can be digitally logged.

Specifications	Value
Operating frequency	935 MHz – 960 MHz
Measurable power	-55 dBm – -10 dBm

Table 6-2 Specifications of design example 1 – 950 MHz

Taking these specifications into consideration, there are a few decisions and observations the designer must make. Firstly, this is a small signal detector operating over a relative narrow band. It will be a good starting point to design a narrowband, maximum sensitivity detector. However a wideband matching circuit will also be considered.

6.5.2 Schottky Diode and Models

The first step, and probably the most important one, is to decide on an appropriate diode. The decision making factors are the operating frequency and if a bias or zero-bias diode will be used. Let us firstly consider the zero-bias HSMS-2850 HP Schottky diode. It is optimized for use in small signal applications at frequencies below 1.5 GHz and is ideal where primary (DC bias) power is not available.

The Schottky diode model is already extracted for this diode in chapter 4 and will be used as it is. A good idea is to also consider the Spice model for this diode, because the designer does not always want to go through the trouble of extracting a model. A comparison will be made between the two models.

Parameter	Units	Extracted	Spice
C_{jo}	pF	0.13	0.18
E_G	eV	*	0.69
I_s	A	2.1e-5	3e-6
N		*	1.06
R_s	Ω	23.64	25
V_j	V	0.35	0.35

Table 6-3 Model parameters for design example 1 – 950 MHz

The Spice parameters that are used in the detector design and analysis are indicated in table 6-3. (* indicates the parameters that does not need to be extracted)

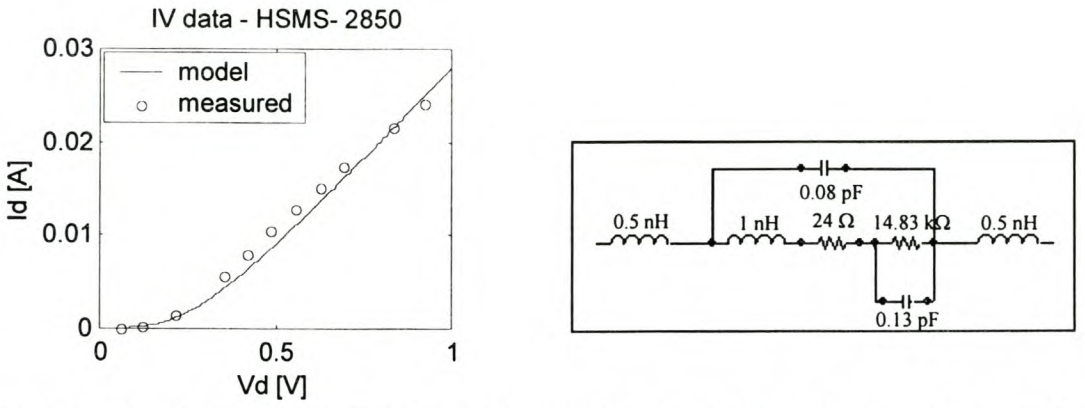


Figure 6-4 The IV curve and small signal model of the HSMS 2850 diode for Design example 1 - 950 MHz

As discussed in chapter 4, the junction resistance and capacitance are non-linear and are described by eq [2-3] and [4-3]. These two nonlinear parameters have the biggest influence on detector performance and needs to be well defined.

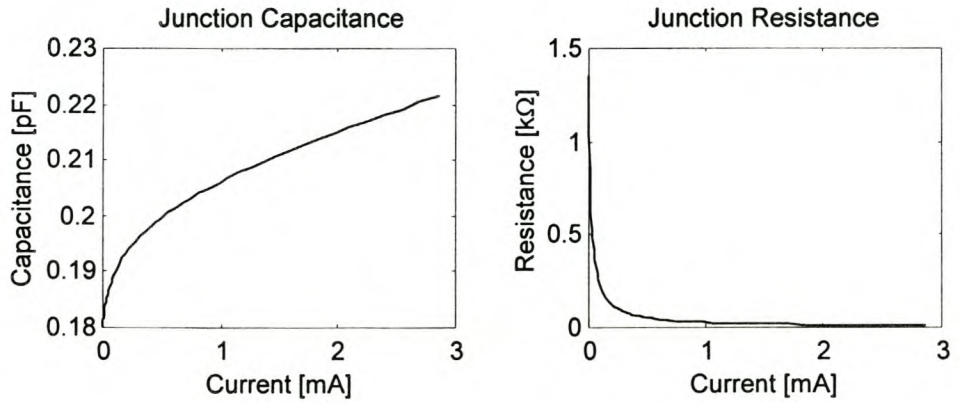


Figure 6-5 The junction parameters performance over bias current for Design example 1 - 950 MHz

6.5.3 Bias Current

Due to the use of the zero bias Schottky diode, there is no initial design for bias current. The bias current influences the sensitivity and it is therefore not known if the measurable power of table 6-2 will be reached. The diode, however, is optimized for small signal detection in the operating frequency region, which at this stage must be accepted as guarantee for the design.

6.5.4 Output Circuit

As previously said, the operating frequency is between 935 and 960 MHz, which give a bandwidth of 25 MHz. The application of the design, however, is as a power meter and not as a receiver. The design of the output circuit is therefore less crucial, due to the absence of a detected video signal. The output circuit serves as the separation between the RF and the detection side of the circuit. It must provide a good RF short circuit to the diode, to insure that all the RF voltage appears across the diode terminals.

A capacitance of $C_L = 100$ pF will be adequate for this application, together with a load resistance of $R_L > 100$ kΩ. The load resistance is the input impedance of either a pre-amplifier or the measuring equipment being an oscilloscope or RMS voltmeter. For both cases $R_L > 100$ kΩ is a reasonable ask.

6.5.5 Matching Circuit

The matching of the detector design, thus far, to a source impedance of 50 Ω is a crucial part of the design. A wideband match, as discussed in chapter 5, is done first. The detector is matched over the span of 900 MHz to 1 GHz.

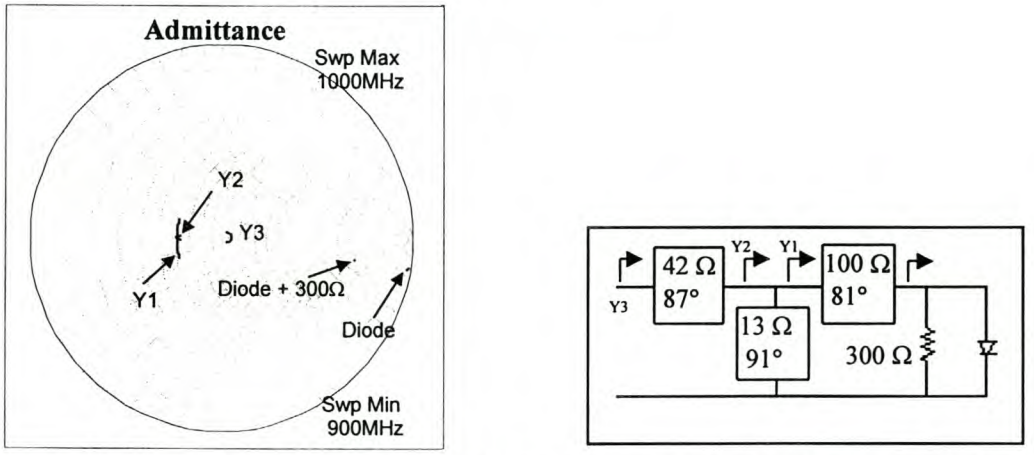


Figure 6-6 Representation of the wideband matching technique applied on design example 1 – 950 MHz

The result of the three step matching technique, discussed in chapter 5, is shown in Fig.6-6. A 300 Ω resistor is added in shunt to improve the VSWR before matching is done.

The realization of the detector at 950 MHz as presented in Fig. 6-6 and 6-9 is not very elegant and a bit too large. It is possible to use lumped elements with distributed elements to decrease the size of the design.

Another design is presented that includes the lumped inductance of 68 nH. It is a narrowband match and consists of much shorter transmission lines, which is a positive improvement.

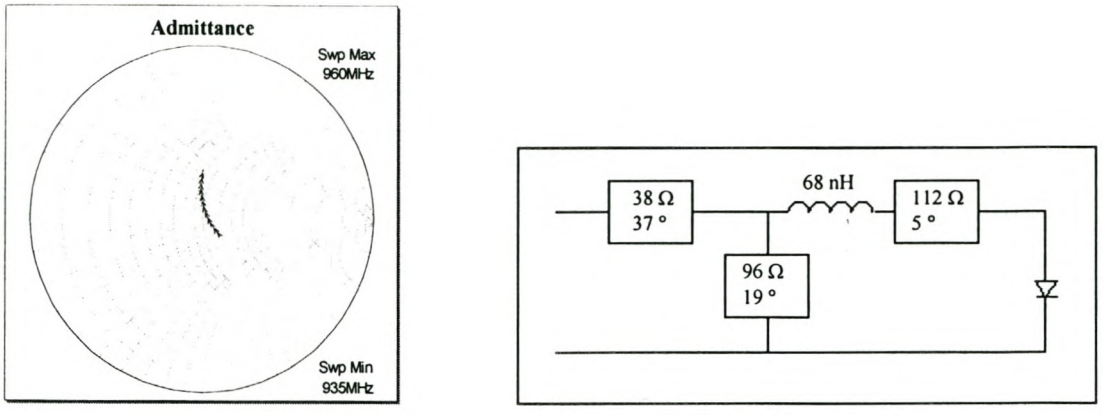


Figure 6-7 Representation of the narrowband matching technique applied to design example 1 – 950 MHz

6.5.6 The Final Design

The two designs are designed in microstrip. A detailed discussion on the calculation of the line lengths and widths are done in Appendix E. The results are summarized in this chapter.

Center frequency	950 MHz
Wavelength [λ]	316 mm
Wavelength [λ_g]	238 mm
ε	2.51
Substrate height	1.581 mm

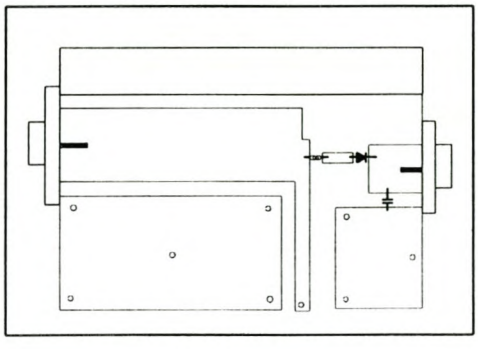


Figure 6-8 The circuit layout and parameters for Design example 1 – 950 MHz [1]

Center frequency	950 MHz
Wavelength [λ]	316 mm
Wavelength [λ_g]	251 mm
ε	2.17
Substrate height	0.508 mm

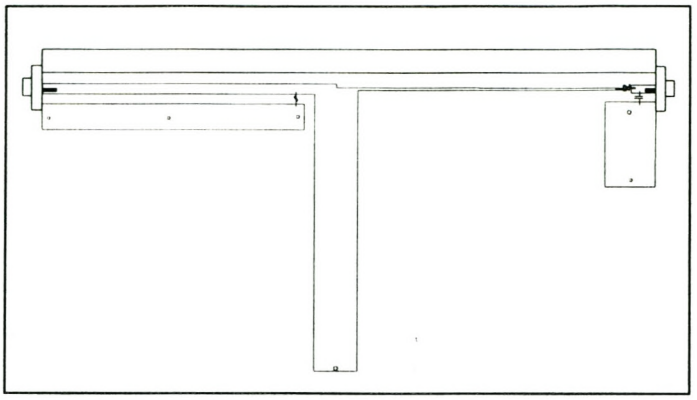


Figure 6-9 The circuit layout and parameters for Design example 1 - 950 MHz [2]

6.6 Design Example 2 – 2.45 GHz

6.6.1 Background

The design of this detector is for a narrowband, minimum tangential sensitivity application (optimized for lowest possible detection). The application is for the measurement of possible leakage of power in microwave ovens.

Specifications	Value
Operating frequency	2.4 GHz – 2.5 GHz
Measurable power	Minimum tangential sensitivity

Table 6-4 Specifications for design example 2 – 2.45 GHz

The design specifications are indicated in table 6-4

6.6.2 Schottky Diode and Models

The Schottky diode in discussion to be used in this application is either the HP HSMS-2810 or the HSMS-2820. Their characteristics are very similar and it was decided to use the HSMS-2820 diode. It features low series resistance, low forward voltage at all current levels and good RF characteristics. The diode is optimized for use at frequencies below 3 GHz, which is adequate for this application.

The Schottky diode model parameters are extracted up to 3 GHz in chapter 4. The extracted parameters, as well as the calculated and Spice parameters, are indicated in table 6-5.

Parameter	Units	Extracted	Spice
C_{jo}	pF	0.89	0.7
E_G	eV	*	0.69
I_s	A	1.97e-8	2.2e-8
N		*	1.08
R_s	Ω	13.05	6
V_j	V	0.65	0.65

Table 6-5 Model parameters for design example 2 – 2.45 GHz

(* indicates the parameters that does not need to be extracted)

The small signal parameters as well as the DC characteristics used in this design are indicated in Fig. 6-10. Both models were extracted and expressed in chapter 4. The model is adequate for frequencies up to 3 GHz.

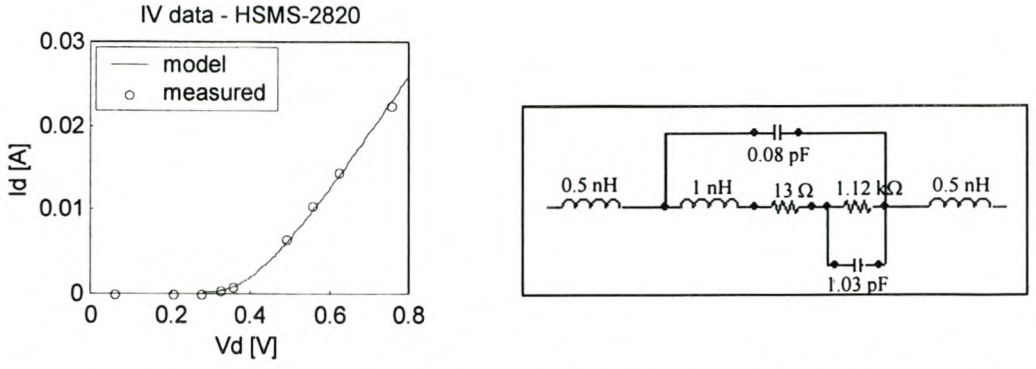


Figure 6-10 The IV curve and small signal model of the HSMS 2820 diode for Design example 2 – 2.45 GHz

The nonlinear junction parameters are described in Fig. 6-11.

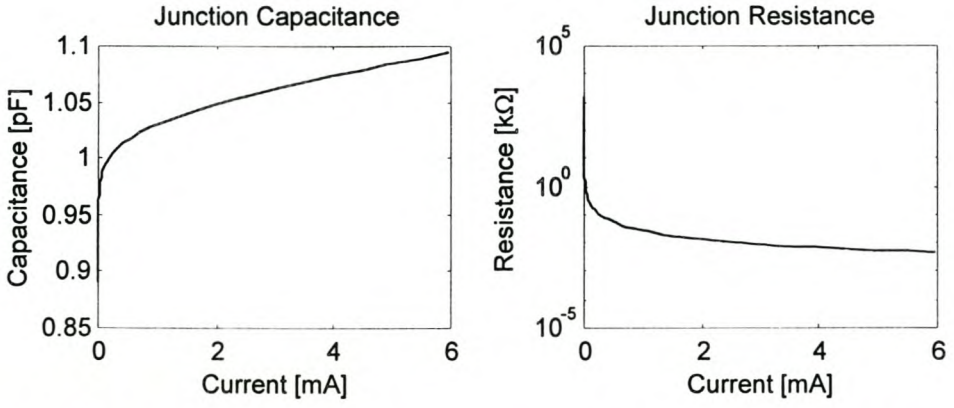


Figure 6-11 The junction parameters performance over bias current for Design example 2 – 2.45 GHz

6.6.3 Bias Current

For this design the use of bias current is worth discussing. The design is for minimum tangential sensitivity [TSS]. The design equations are discussed in section 6.2 and can be applied to the design specifications of this detector design.

The parameters used to calculate TSS is indicated in table 6-6

Parameter	Value	Parameter	Value
B_v	100 MHz	R_s	13.05 Ω
I_d	**Calculate**	C_{j0}	0.89 pF
f_N	3 kHz	F	2.45 GHz
f_L	100 Hz	R_A	500 Ω

Table 6-6 The parameters used in the calculation of TSS – design example 2 – 2.45 GHz

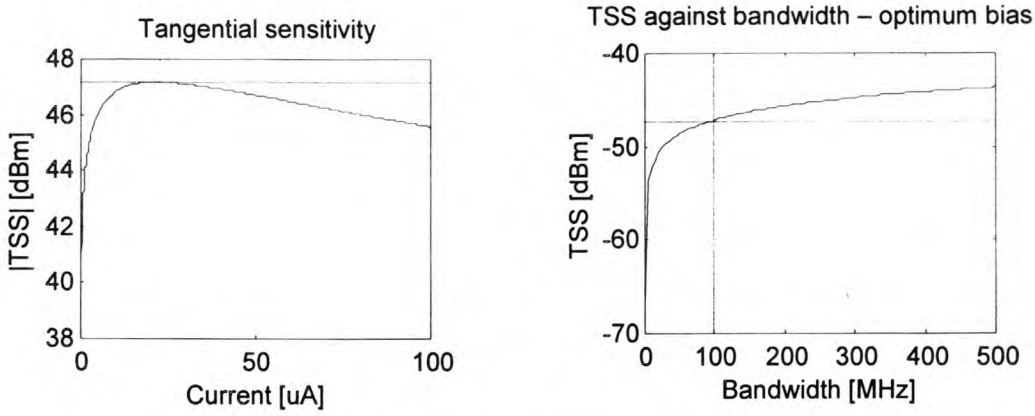


Figure 6-12 Graphical representation of TSS

The calculated optimum bias current is 24.86 uA, which result in a minimum TSS of – 47.12 dBm.

If it is accepted that the amplifier contributes negligible noise compared to the diode to the system, the optimum bias current can be calculated by eq [6.1], which is an easier calculation. The calculation leaves an optimum bias current of 62 uA. The first calculated bias current of 25 uA is used, which is the more accurate calculation.

6.6.4 Output Circuit

The output circuit once again serves as the separation between the RF and the detection side of the circuit and must provide a good RF short circuit to the diode. Since the application is power measurement and not a receiver, the design of the output circuit has more freedom. The load resistance must be large, if possible not lower than R_L = 100 kΩ to maximize the detected voltage. A capacitance of C_L = 100 pF is adequate for this application.

Applying eq [6-2] gives the upper 3 dB cutoff frequency of $f_{u(3\ dB)}$ = 15.89 kHz. The cutoff frequency can be increased by either reducing the load resistance or capacitance, but this will effect the sensitivity of the detector. Sensitivity is important in this application and the relative small cutoff frequency is not a problem.

6.6.5 Matching Circuit

It was decided to do a narrowband match on the biased Schottky diode as discussed above. The first step is once again to calculate the input impedance or admittance either by measurement and the model extraction method, or by using the Spice parameters from the manufacturers' data sheets together with the nonlinear junction equations. The results obtained by the two methods are in good agreement with each other, especially when the diode is biased with an optimum bias current.

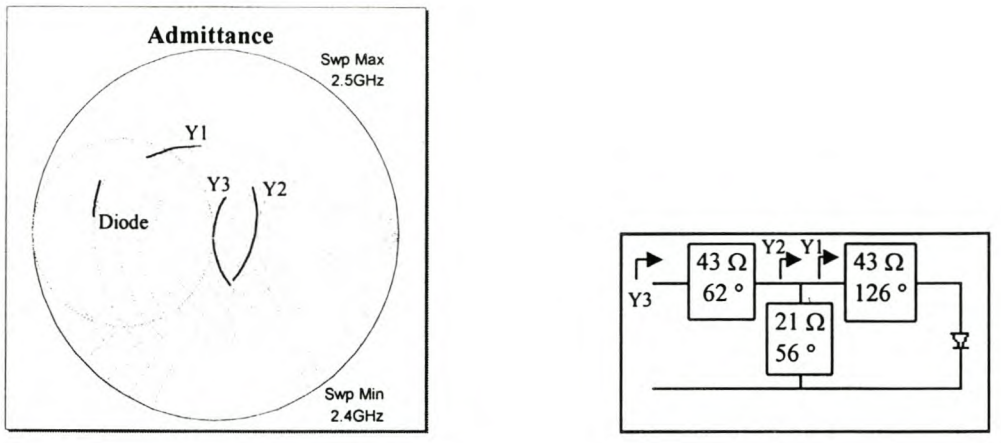


Figure 6-13 Representation of the three step narrowband matching technique applied on design example 2 – 2.45 GHz

The three-step narrowband matching technique is illustrated in Fig.6-13 The bias current of 25 uA is enough to insure a good match, without using an additional shunt resistance as previously discussed to improve the VSWR.

6.6.6 The Final Design

When a detector with optimum bias current is designed, it is worth to discuss the method of designing a high input RF impedance on the DC excitation path. It must serve as the RF choke, preventing any RF leakage. The excitation is done on the DC side of the diode with the matching circuit serving as the DC return path. A radial stub is designed as a RF choke at high frequencies. The theory of radial stub design is discussed in [51] and only the results are shown here.

The detector circuit is realized in microstrip – see Appendix E for a discussion.

Center frequency	2.45 GHz
Wavelength [λ]	122 mm
Wavelength [λ_g]	97 mm
ε	2.17
Substrate height	0.508 mm

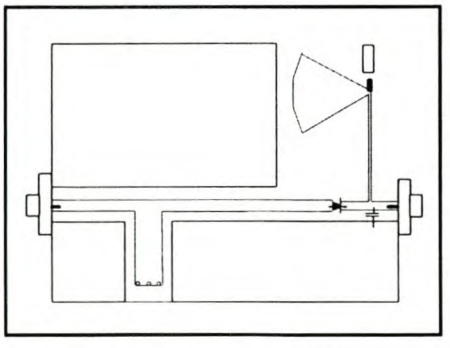


Figure 6-14 The layout and important parameters of design example 2 – 2.45 GHz

6.7 Design Example 3 – 10 GHz

6.7.1 Background

This is a detector example designed for maximum sensitivity at a center frequency of 10 GHz. Its application is to detect the output of a FM discriminator in the X-band.

Specifications	Value
Operating frequency	8 GHz – 12 GHz
Measurable power	-40 dBm – 10 dBm

Table 6-7 Specifications of design example 3 – 10 GHz

The specifications of the design is indicated in table 6.7

6.7.2 Schottky Diode and Models

The Schottky diode used in this application is the HP HSMS-8101. The diode is optimized for use at frequencies of 10-14 GHz (X-band). Its low capacitance contributes to the optimum use in the X-band.

The Schottky diode model parameters are extracted up to 12 GHz in chapter 4. The extracted parameters, as well as the calculated and Spice parameters, are indicated in table 6-8.

Parameter	Units	Extracted	Spice
C_{jo}	pF	0.142	0.18
E_G	eV	*	0.69
I_s	A	3.13e-8	4.6e-8
N		*	1.09
R_s	Ω	10	6
V_j	V	0.5	0.5

Table 6-8 Model parameters for design example 3 – 10 GHz

(* indicates the parameters that does not need to be extracted)

The DC characteristics and small signal diode model is indicated in Fig. 6-15.

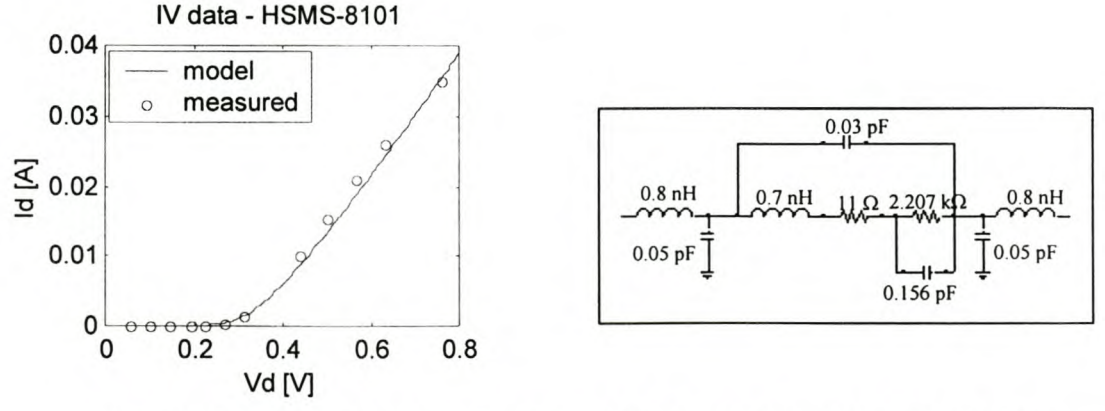


Figure 6-15 The IV curve and small signal model of the HSMS-8101 diode for Design Example 3 –10 GHz

Due to the higher frequency of the design, the stray capacitance, modeling the package legs and connector needs to be included in the small signal model.

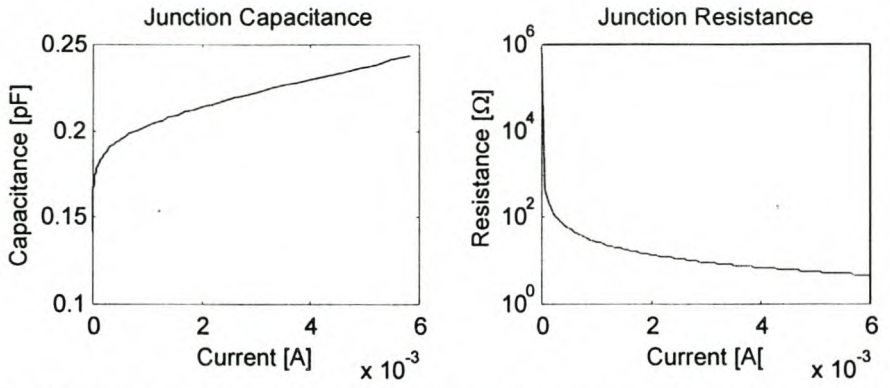


Figure 6-16 The junction parameters performance over bias current for Design example 3 – 10 GHz

6.7.3 Bias Current

The use of bias current needs to be discussed. Although this is a wideband design (8-12 GHz), tangential sensitivity (dynamic range) is also very important. It will therefore be better to place the constraint on bandwidth and design for maximum sensitivity.

The parameters used to calculate the optimum bias current is indicated in table 6-9.

Parameter	Value	Parameter	Value
B_v	4e9 GHz	R_s	Ω
I_d	**Calculate**	C_{j0}	pF
f_N	3 kHz	F	10 GHz
f_L	100 Hz	R_A	500 Ω

Table 6-9 The parameters used in the calculation of TSS – Design Example3 – 10 GHz

The optimum bias current is calculated on 25.21 uA, giving a tangential sensitivity of -38.21 dBm. This calculated value is within the design specifications.

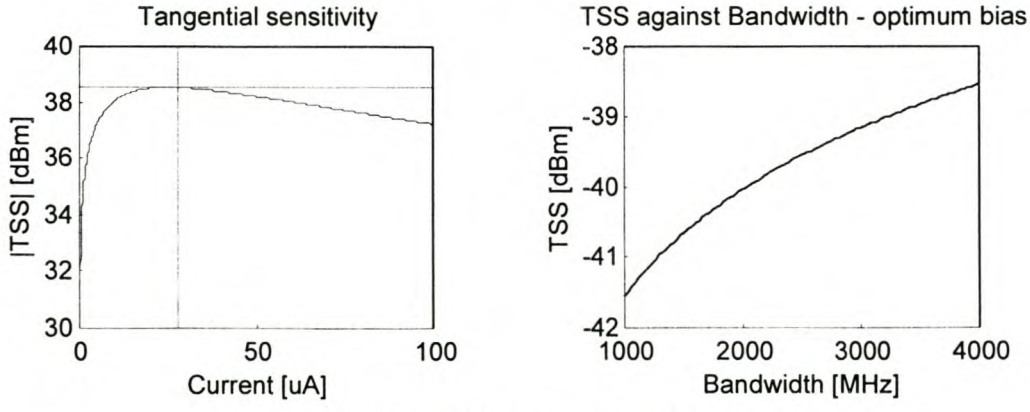


Figure 6-17 Graphical representation of TSS

The small signal model of Fig. 6-16 is the result of a bias current of 25 uA, in other words the optimum bias current.

6.7.4 Output Circuit

The output resistance needs to be as large as possible, usually it is equivalent to the input impedance of a low noise amplifier. The load resistance of 100 kΩ, used up to this point, is once again adequate. The load capacitance must serve as the RF short. At 10 GHz this is not a problem and C_L=100 pF will once again do for this application.

6.7.5 Matching Circuit

This design example is a wideband application and therefore needs a wideband matching circuit. The first step before applying the three step matching procedure is to calculate the diode's input impedance. The diode model that is used for this calculation was discussed in chapter 4. The Spice model is in good agreement with the model extracted from the measurements.

The results of the three step matching technique is illustrated in Fig. 6-17

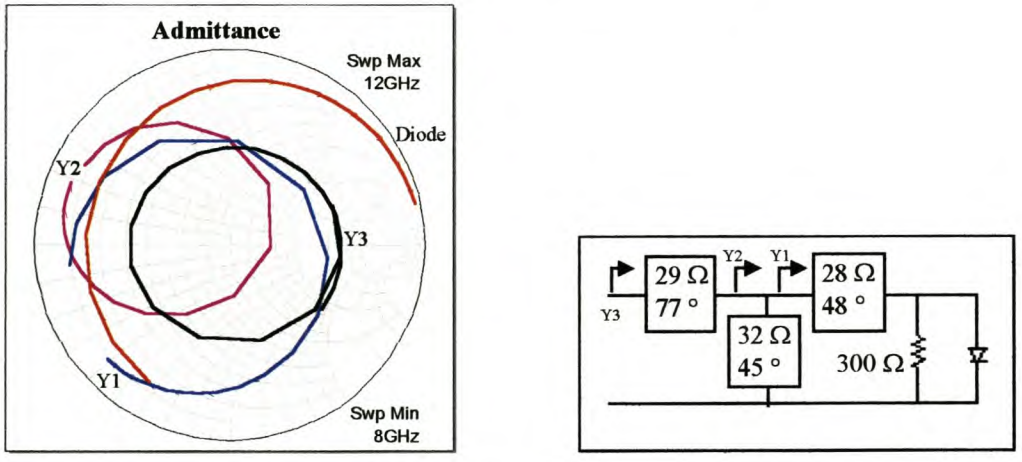


Figure 6-18 Representation of the three step wideband matching technique applied on design example 3 – 10 GHz

The VSWR of the design is once again improved by the addition of a shunt resistance of 300 Ω. (not indicated on the Smith chart)

6.7.6 The Final Design

The final step of matching – the addition of the third transmission line - is modified to improve practical representation. It is replaced with a tapered line. The design is represented in microstrip.

Center frequency	10 GHz
Wavelength [λ]	30 mm
Wavelength [λ_g]	23.83 mm
ε	2.17
Substrate height	0.508 mm

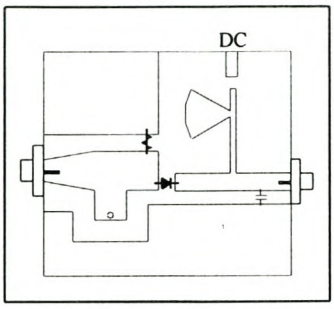


Figure 6-19 The layout and important parameters of design example 3 – 10 GHz

6.8 Conclusions

In this chapter a design procedure was presented to design diode detectors. The procedure was presented as a step-by-step method for three different kinds of detectors. Firstly, small signal maximum sensitivity detectors; secondly, small signal maximum bandwidth detectors; and finally large signal detectors. The design of biasing current, the output circuit and the matching circuit of the detector were discussed.

The chapter was concluded with three design examples, to present the method practically.

Chapter 7

7 Analysis Algorithms

In this chapter emphasis is laid on the development of analysis algorithms that describes the behavior of detector circuits.

The first algorithm is the Ritz-Galerkin method, which describes the detector output curve by means of a summation of Bessel functions. The algorithm can handle bias current, load resistance and temperature variances in the detector.

The second algorithm applies the Harmonic Balance (HB) technique to analyze a detector circuit properly. All the parasitic parameters of a diode can be taken into consideration as well as temperature, bias and load resistance effects.

The purpose of these algorithms is to serve as error-correcting algorithms to compensate for the nonlinear behavior of diode detectors at higher power levels.

7.1 Ritz-Galerkin Method

It was already shown that diode detectors exhibit true square-law behavior at low power levels. At higher power levels, there is a gradual change to a linear (peak-detecting) law. The Ritz-Galerkin method provides an algebraic approach to the large-signal analysis of exponential diode detector circuits.

7.1.1 Background

The Ritz-Galerkin method is used to obtain a closed-form algebraic solution that relates the output voltage of a detector circuit to the incident RF power. The solution is valid over the full dynamic range from square law to linear.

The diode is modeled as an exponential device obeying

$$I_d = I_s(e^{\alpha v} - 1) \qquad [7\text{-}1]$$

in series with a resistance R_s and α=e/(nkT), where n is the diode ideality factor and k is Boltzmann's constant. The junction capacitance is presented in parallel with the diode.

A relation is sought between the incident RF power, P_{inc}, and the output voltage V_{out}. P_{inc} is the power impinging on the input port of the detector circuit, regardless of its matching or non-linearity. P_{abs} is that portion of P_{inc} actually absorbed by the nonlinear detector circuit.

Practical detectors are normally operated in a non-maximum power transfer mode. In the RG analysis the differential equation of the detector circuit is solved approximately, yielding a relation between the RF generator voltage, $V_g(t)$, and the output voltage, V_{out}. The P_{inc} is found from $V_g(t)$.

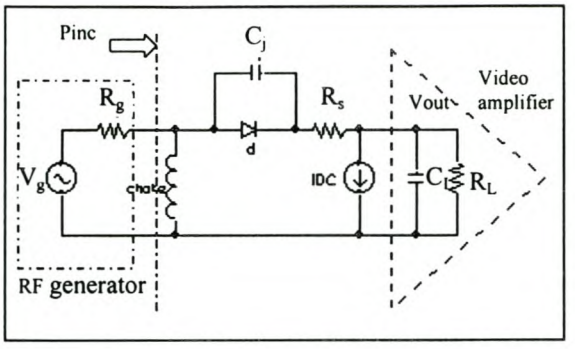


Figure 7-1 The detector circuit as analyzed by theRitz-Galerkin method

The differential equation is [41],[42]

$$\Pi_0\left(\alpha\sqrt{8R_g P_{inc}}\right)=\underbrace{\left(1+\frac{I_0}{I_s}+\frac{V_0}{R_L I_s}\right)\exp\left\{\left[1+\frac{R_g+R_s}{R_L}\right]\alpha V_0+\alpha R_s I_0\right\}}_{\zeta} \qquad [7\text{-}2]$$

where

Π_0 is the zero order modified Bessel function.
α is a constant value (α=e/nkT where n is the ideality factor, k is Boltzmann's constant, T is temperature in °Kelvin and e is the electron charge)
R_g is the source resistance
P_{inc} is the incident power
I_0 is the bias current
I_s is the saturation current of the diode
V_0 is the measured output voltage
R_L is the load resistance

This expression includes the bias current I_0. The actual detector response can be found from eq [7-2] by calculating the input P_{inc} as a function of the output quantity V_0, an operation requiring the inverse of the modified Bessel function. In the absence of input power, the static output $V_0(0)$ is found by solving eq [7-2] for P_{inc}=0. The change in V_0 in response to a finite P_{inc} is given by

$$\Delta V_0 = V_0(P_{inc}) - V_0(0) \qquad [7\text{-}3]$$

7.1.2 Application of Theory

Eq [7-2] can be implemented in MATLAB and the response of a diode detector can be calculated according to the Ritz-Galerkin theory.

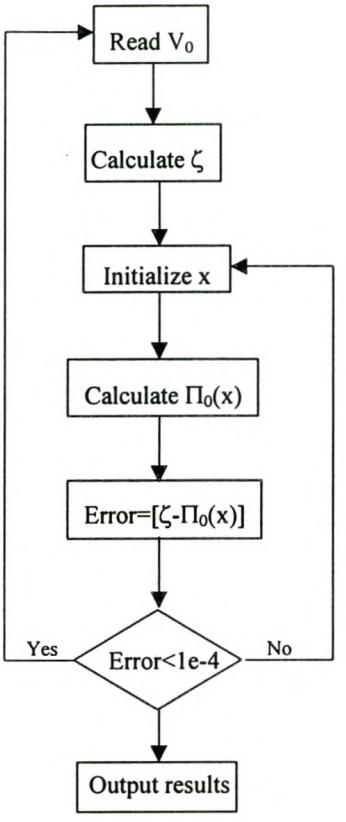


Figure 7-2 Block diagram of the Ritz-Galerkin algorithm

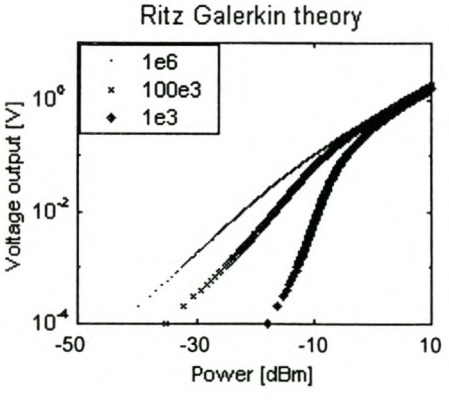


Figure 7-3 Output result of detector for varying load resistance -RG

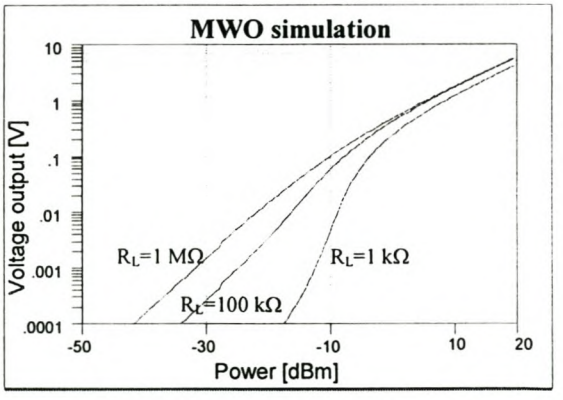


Figure 7-4 Output result of detector for varying resistance - MWO

Although the Ritz-Galerkin theory is in good agreement with the **M**icrowave **O**ffice simulations, all the diode parameters were not included in the MWO simulation. The effect of other parasitic parameters will have a significant influence on results, especially at higher frequencies. To include these effects in the RG-theory will make the algorithm extremely complex and difficult to implement. The RG-theory does not consider high frequency effects. It only includes the effects of load resistance, bias current and temperature.

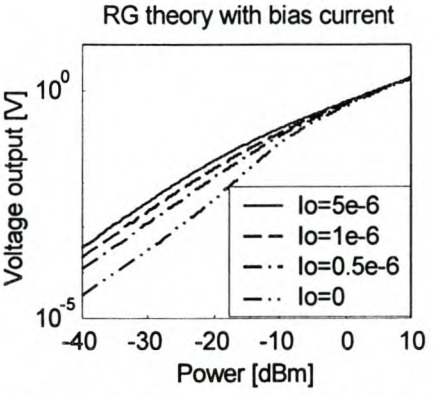


Figure 7-5 The output of Ritz-Galerkin method for a detector with varying bias

Fig 7-5 shows the effect of increasing DC forward bias current, I_0, on the detector transfer characteristic. The tendency is to move the characteristic towards the idealized square law/linear-law shape, with no further change of shape thereafter.

7.1.3 Conclusion

The averaging method of Ritz and Galerkin can be used to obtain a closed-form solution for the nonlinear behavior of diode detectors. This solution is valid over a very large dynamic range. The Ritz-Galerkin method is successful in providing the basis for an easily implemented error-correcting algorithm for power-measurement systems when there are variations of load, bias current and temperature.

7.2 Harmonic Balance Method

In this section the harmonic balance method, as a nonlinear circuit simulator, will be discussed and implemented on a detector circuit. [6], [37], [48]

7.2.1 Background

When transient information is needed, there is no alternative to time-domain methods in circuit analysis. However, these methods have some shortcomings when used to compute the steady-state response of nonlinear microwave circuits. In nonlinear circuits, several frequencies exist even if all time-varying sources are sinusoids of the same frequency, due to nonlinear effects.

Harmonic balance analysis effectively partitions a circuit into two subcircuits: the linear subcircuit, which contains all the linear parts, and the nonlinear subcircuit, which contains only nonlinear elements. The two circuits are connected by a port as indicated in Fig. 7-6

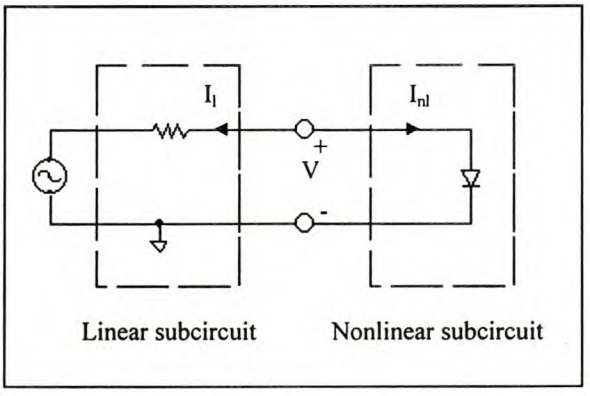


Figure 7-6 The presentation of a linear and nonlinear subcircuit

The voltage at the interconnecting port, the DC, fundamental frequency, and its harmonics, are treated as variables. The harmonic balance process iteratively tries to find a voltage that satisfies the linear circuit equation of the linear subcircuit, and the nonlinear equation, describing the nonlinear subcircuit. The linear equation are easily solved in the frequency domain, but the nonlinear equation must be solved in the time domain. The frequency and time domain quantities are related by a Fourier series.

A detector circuit, as shown for example in Fig. 7-6, can be solved by the harmonic balance method without much trouble.

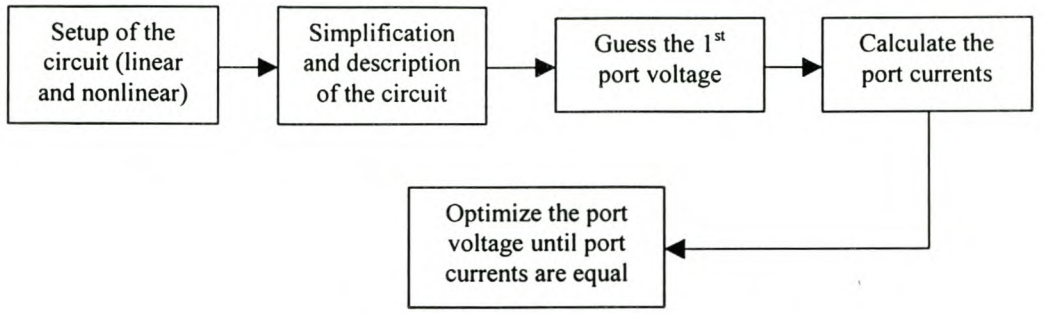


Figure 7-7 Block diagram description of the procedure followed to setup the HB-algorithm

7.2.2 The Simplification of the Circuit

In order to implement the harmonic balance method, the detector circuit must be in its simplest form. The nonlinear subcircuit (the diode) is represented by the nonlinear model of the diode, consisting of the nonlinear resistance and capacitance. The linear subcircuit consists of the Thevenin representation of the remaining part of the detector circuit, including the diode parasitic values, the load resistance and capacitance and the source impedance.

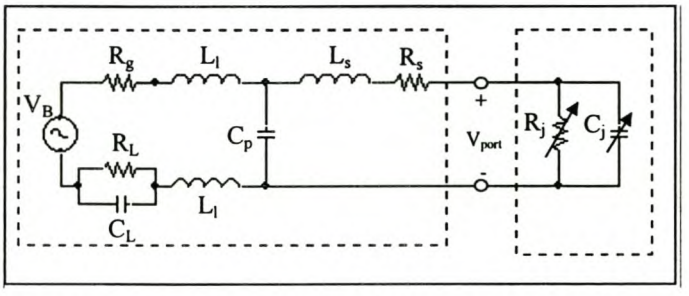


Figure 7-8 The linear and nonlinear subcircuits with the diode's parasitic values included

Looking into the linear subcircuit from the port side:

$$Z_{TH} = \left[R_g + R_L \| Z_{C_L}\right] \| Z_{C_p} + R_s + Z_{L_s} \qquad [7\text{-}4]$$

$$V_{TH} = \frac{Z_{C_p}}{R_L \| Z_{C_L} + R_g + + Z_{C_p}} . V_B \qquad [7\text{-}5]$$

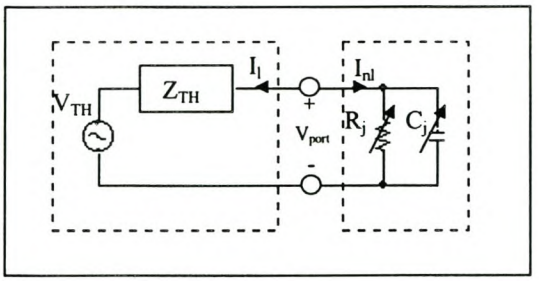


Figure 7-9 The Thevenin equivalent of the linear subcircuit

See Appendix F for the simplification of the detector circuit with all the parasitics included – for X-band designs.

7.2.3 The Calculations of Port Voltages and Currents

Let us first consider the nonlinear subcircuit and its currents. The current through the nonlinear resistance is described by the diode-equation.

$$i_{res} = I_s e^{\alpha v_{port}} - 1 \qquad \text{[7-6]}$$

The current through the nonlinear capacitance is also known. The junction capacitance for Schottky diodes is well defined for small signals.

$$C_j = \frac{C_{j0}}{\left(1 - \frac{v_{port}}{V_j}\right)^{1/2}} \qquad V_{port} < V_j \qquad \text{[7-7]}$$

The current through the capacitor can be easily calculated.

$$i_{cap} = C_j \frac{dv_{port}}{dt} \qquad \text{[7-8]}$$

The calculation of dv_{port}/dt will be discussed (see eq [7-20] and eq [7-21]).

The nonlinear current is, therefore:

$$i_{nl} = i_{res} + i_{cap} \qquad \text{[7-9]}$$

The linear current is equally simple to compute. It is done in the frequency domain and the admittance of the linear subcircuit needs to be known at all the harmonics.

For example:

$$Y = \begin{vmatrix} Y(0) & 0 & 0 & \cdots & 0 \\ 0 & Y(1) & 0 & \cdots & 0 \\ 0 & 0 & Y(2) & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & Y(K) \end{vmatrix} \qquad \textbf{[7-10]}$$

For a starting point, the value of the v_{port} voltage is considered known, although it is calculated by means of an optimization algorithm. v_{TH} is the voltage the detector circuit is excited with and is known.

The bridge between the frequency and time domain is the Fourier transform. Let us first consider the Fourier transform.

Let $v_{TH}(t)$ be a combination of a finite number of sinusoids. The, all steady-state waveforms in the circuit are approximately described by an appropriate truncated set of frequencies [37].

$$\Lambda_K = \{\omega_0 = 0, \omega_1, \ldots, \omega_K\} \qquad \textbf{[7-11]}$$

v_{TH} is expanded as

$$v_{TH}(t) = V_s(0) + \sum_{k=1}^{K} \left(V_s^c(k) \cos \omega_k t + V_s^s(k) \sin \omega_k t \right) \qquad \textbf{[7-12]}$$

$v_{TH}(t)$ is expressed in the frequency domain

$$V_{TH} = V_s^c(k) - jV_s^s(k) \qquad \textbf{[7-13]}$$

where $V_s(0)$ is the DC-component
$V_s^c(k)$ is the real coefficient
$V_s^s(k)$ is the imaginary coefficient

The conversion between the time and frequency domain can thus be done successfully with the Fourier transform.

To get back to the linear current in Fig. 7-9, it can be expressed as follows:

$$I_L = Y\left[V_{port} - V_{TH}\right] \quad \text{[7-14]}$$

where V_{port} and V_{TH} are both in the frequency domain.

By calculating the inverse Fourier transform, the linear current can be converted back to the time domain.

$$i_L = F^{-1}(I_L) \quad \text{[7-15]}$$

Both the linear and nonlinear currents are now defined or calculated.

7.2.4 The Optimization Algorithm

An optimization algorithm is implemented to calculate the correct port voltages and currents. The Newton optimization technique is used and proved to be very successful. The method is discussed in Appendix B.

One of the important equations in the optimization algorithm is the error function. It makes perfect sense to define this function to be the sum of the linear and nonlinear currents, which must be minimized to zero.

For the HB algorithm the error function is defined as

$$error = \sum R(i_l) + R(i_{nl}) \quad \text{[7-16]}$$

As can be seen, only the real parts of the linear and nonlinear currents are considered. The optimization algorithm only considers the currents that will have a direct effect on the voltage output of the detector. This proves to be more than acceptable for accurate simulation results.

Jacobian Computation

When the HB equation is solved by Newton's method, the Jacobian of the HB error is required. The Jacobian can be computed numerically using differences. Although this approach to Jacobian computation is extremely simple to code, forming the Jacobian using numerical differences can consume the majority of computation time in a HB algorithm. Considerable savings are obtained when the Jacobian is computed analytically or semi-analytically.

The calculation of the Jacobian matrix, however, is the most complex and most critical part in the optimization algorithm and needs some attention [37].

The error function is already defined in eq. [7-16]. It is now necessary to start to define the Jacobian. The Jacobian will be the voltage differential of the error function.

$$J = \frac{\partial(i_{nl} + i_l)}{\partial v_{port}} = G_{nl} + S_l \qquad [7\text{-}17]$$

The Jacobian of the linear and nonlinear port currents will be calculated separately and added at the end.

Jacobian of Nonlinear Current

The nonlinear current is described in eq. [7-9]. The voltage differential of eq. [7-17] can once again be separated into two parts. The current through the nonlinear resistance is considered first and secondly, the current through the nonlinear capacitance.
From eq. [7-6]

$$\frac{di_d}{dv_{port}} = I_s \alpha \left[e^{\alpha v_{port}} \right] \qquad [7\text{-}18]$$

From eq. [7-8] and applying the chain rule:

$$\frac{di_c}{dv_{port}} = \underbrace{\frac{dC_j}{dv_{port}} \frac{dv_{port}}{dt}}_{Q} + \underbrace{C_j \frac{d}{dv_{port}} \left[\frac{dv_{port}}{dt} \right]}_{D} \qquad [7\text{-}19]$$

Let us firstly consider Q:
The calculation of dv_{port}/dt is not a straightforward differential. It can, however, be done in the frequency domain. Differentiating in the time domain is equivalent to multiplying with (s=jw) in the frequency domain. [40]

$$F\left[\frac{df(t)}{dt} \right] = (jw) F(w) \qquad [7\text{-}20]$$

Therefore,

$$\frac{dv_{port}}{dt} = F^{-1}\left[jwk V_{port} \right] \qquad [7\text{-}21]$$

where jwk is a diagonal matrix, representing the differential in the frequency domain at every harmonic.

$$jwk = \begin{bmatrix} jw(0) & 0 & 0 & \cdots & 0 \\ 0 & jw(1) & 0 & \cdots & 0 \\ 0 & 0 & jw(2) & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & jw(K) \end{bmatrix} \quad [7\text{-}22]$$

The calculation of dC_j/dv_{port} can be done directly from eq. [7-7]

$$\frac{dC_j}{dv_{port}} = \frac{C_{j0}}{2V_j}\left(1 - \frac{v_{port}}{V_j}\right)^{-3/2} \quad [7\text{-}23]$$

It is thus possible to calculate Q analytically.

Let us now consider D:
C_j is simply a diagonal matrix of junction capacitance. D, however, must be computed analytically.

D can be rewritten as follows:

$$D = \frac{d}{dt}\underbrace{\left[\frac{dv_{port}}{dv_{port}}\right]}_{T} \quad [7\text{-}24]$$

It simplifies to:

$$D = \begin{bmatrix} \Omega(1) & \Omega(K) & \cdots & \Omega(2) \\ \Omega(2) & \Omega(1) & \cdots & \Omega(3) \\ \vdots & \vdots & \ddots & \vdots \\ \Omega(K) & \Omega(K-1) & \cdots & \Omega(1) \end{bmatrix} \quad [7\text{-}25]$$

where

$$\Omega = F^{-1}\left[jwk.F(T)\right] \quad [7\text{-}26]$$

That concludes the calculation of the Jacobian for the nonlinear current.

Jacobian of Linear Current
The Jacobian of the linear current must be calculated numerically. The linear current was calculated above as in eq. [7-14]. The calculation is done in the frequency domain.

$$S = \frac{dI_L}{dV_{port}} = \frac{d\left[Y(V_{port} - V_{TH})\right]}{dV_{port}} = Y \underbrace{\frac{d(V_{port} - V_{TH})}{dV_{port}}}_{\text{dv}} \qquad \text{[7-27]}$$

eq. [7-7] can be written as:

$$S = \begin{bmatrix} y(1) & y(K) & \cdots & y(2) \\ y(2) & y(1) & \cdots & y(3) \\ \vdots & \vdots & \ddots & \vdots \\ y(K) & y(K-1) & \cdots & y(1) \end{bmatrix} \qquad \text{[7-28]}$$

where

$$y = F^{-1}[Y.dv] \qquad \text{[7-29]}$$

7.2.5 Implementation of HB Algorithm in MATLAB

When implementing the HB algorithm in MATLAB, there are a few things to consider, especially how some matrices are formed.

Firstly the symmetry of the FFT function in MATLAB (with 2 harmonics, for example):

$$FFT(v) = \left[|V(0)| \quad |V(1)| \quad |V(2)| \quad 0 \quad |V(2)| \quad |V(1)|\right] \qquad \text{[7-30]}$$

The Y-matrix must also take this symmetry into consideration:

$$Y = \begin{bmatrix} Y(0) & 0 & 0 & 0 & 0 & 0 \\ 0 & Y(1) & 0 & 0 & 0 & 0 \\ 0 & 0 & Y(2) & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & Y(2) & 0 \\ 0 & 0 & 0 & 0 & 0 & Y(1) \end{bmatrix} \qquad \text{[7-31]}$$

Finally, the jwk matrix needs also some modification due to the format of the FFT function.

$$jwk = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -jw(1) & 0 & 0 & 0 & 0 \\ 0 & 0 & -jw(2) & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & jw(2) & 0 \\ 0 & 0 & 0 & 0 & 0 & jw(1) \end{bmatrix} \quad \text{[7-32]}$$

The block diagram of the HB algorithm can be seen in Fig. 7-10.

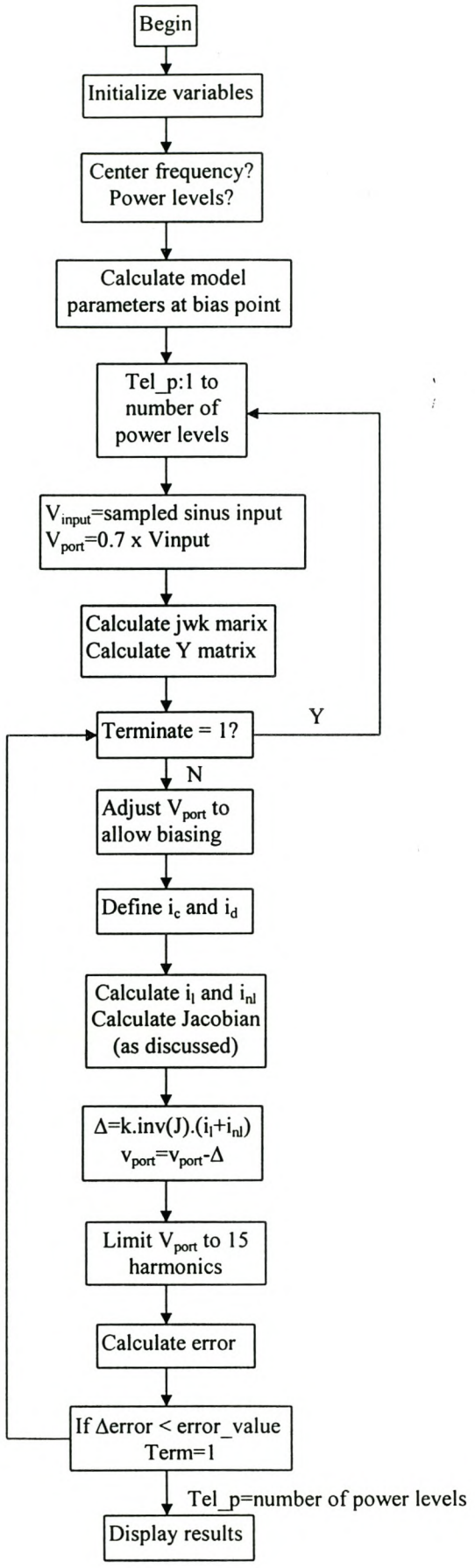


Figure 7-10 Block diagram of the implementation of the Harmonic Balance algorithm

7.2.6 Simulated Results of HB Algorithm

A complete discussion on the simulated results of the HB algorithm is done in the next chapter. It is applied to the design examples and compared with other simulation packages (PSPICE and Microwave Office) as well as with practical measurements made with the designed diode detectors.

A typical output of the HB algorithm, describing the detected voltage for a specific input power level is indicated in Fig. 7-11

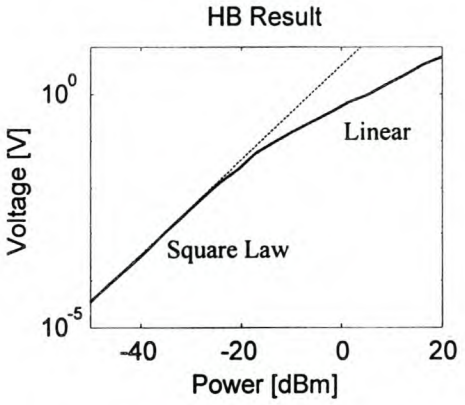


Figure 7-11 Example of simulated detector output – HB algorithm

The square law and linear region is clearly visible in this figure. The analysis was done for a zero biased detector.

7.2.7 General discussion on some aspects of the HB algorithm

Some aspects of the HB algorithm were not discussed thus far, for example the handling of bias current and temperature variation, the prevention of aliasing and minimizing the number of harmonics to decrease simulation time.

For the addition of bias current, the ideal setup is considered, where the external bias current only affects the nonlinear intrinsic diode parameters. External bias current therefore only influences the nonlinear diode current in the nonlinear subcircuit. The port voltage (voltage over diode) is calculated with the diode current equal to the external bias current. This calculated DC voltage is added to the DC component of the frequency domain port voltage to be calculated. The behavior of the diode will be the same as for a diode with external biasing.

To allow for the effect of temperature variance, the temperature dependent parameter (saturation current) is implemented as discussed in section 3-6. The temperature

dependence of the saturation current also influences the value of the junction resistance automatically.

Aliasing can be a problem if the number of samples taken of the source voltage is not enough. An increase in the number of samples, however, increase simulation time considerably. It proved to be adequate to use 64 samples for the source voltage, realizing 32 harmonics. At lower frequencies this can even be decreased to 32 samples, with 16 harmonics.

To improve the simulation time, a limit can be placed on the number of harmonics. Experimental procedures proved that it is unnecessary to work with more than 8 harmonics. The remaining harmonics can therefore be set to zero, simplifying calculations considerably and therefore improving the simulation time.

7.3 Conclusion

Two different algorithms were discussed that can be used to analyze the diode detector circuit.

The RG algorithm gives a very good prediction of a detector's output response for varying temperature and bias current. It, however, does not consider high frequency parasitic effects.

The HB algorithm does a complete analysis of the detector circuit, taking all the parasitic elements into consideration. The algorithm takes longer to execute, but results give a true indication of the performance of the complete detector circuit.

Chapter 8

8 Simulated Results and Measurements

8.1 Introduction

In this chapter the **H**armonic **B**alance algorithm [HB] is applied to the previously discussed design examples of chapter 6. It will be compared to **M**icrowave **O**ffice [MWO] and PSPICE simulations, as well as measured results.

The following results will be presented:

- The shape of the real time diode current for different power levels
  (A comparison between PSPICE and HB)
- The shape of the real time detected voltage for different power levels
  (A comparison between PSPICE and HB)
- The frequency response of the diode current for different power levels
  (A comparison between MWO and HB)
- The detected voltage over input power
  (A comparison between MWO, HB and measured results)
- The detected voltage over frequency variance
  (MWO simulation with matching circuit and measured results)
- The detected voltage with temperature variance
  (A comparison between MWO and HB)

Each design example of chapter 6 will be discussed separately, to make it possible to emphasize individual points of interest or concern.

8.2 Design Example 1 – 950 MHz

8.2.1 Verification of Matching Circuit

The input admittance of the detector is measured on a voltage network analyzer and compared with the designed results of section 6-5.

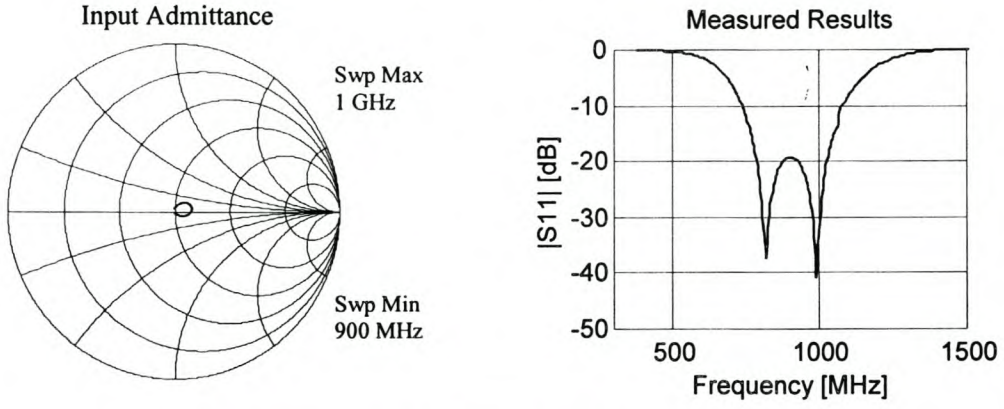


Figure 8-1 Measured results of the input match for Design Example 1

The designed matching circuit proves to be a good match for the detector and compares very good with the simulated response in section 6-4.

8.2.2 Simulations and Measurements

Let us firstly consider the detector designed as design example 1 at 950 MHz.

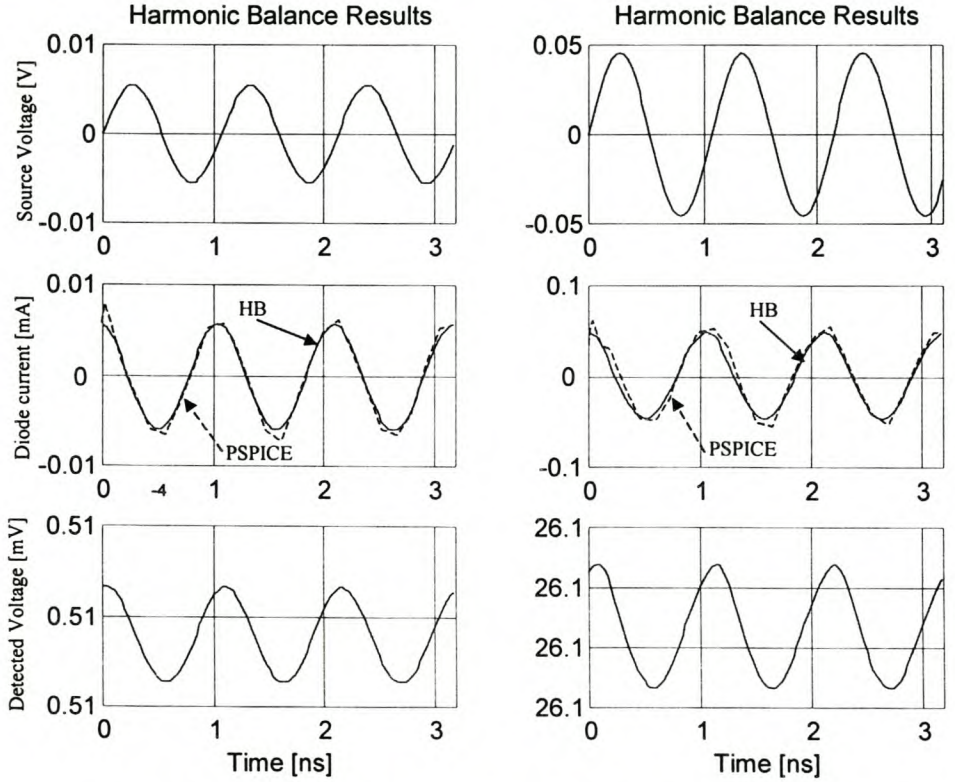


Figure 8-2 Time domain results with small signal input - Design example 1

Fig 8-2 shows the results of the Harmonic Balance technique for small input signals. It is compared with the results obtained by PSPICE.

The time domain curve of detected voltage is not a very good plot to compare with PSPICE, due to the large transient time obtained by PSPICE. The diode current, however, is a good indication to verify the correctness of the HB technique.

The HB-technique and PSPICE simulation are in very good agreement for small input signals.

Let us now consider the HB technique's performance for larger input signals (P_{in}>-20 dBm). The nonlinear behavior of the diode's junction parameters will be more critical at larger signals. More harmonics will be present and it will therefore be a good verification test for the HB technique.

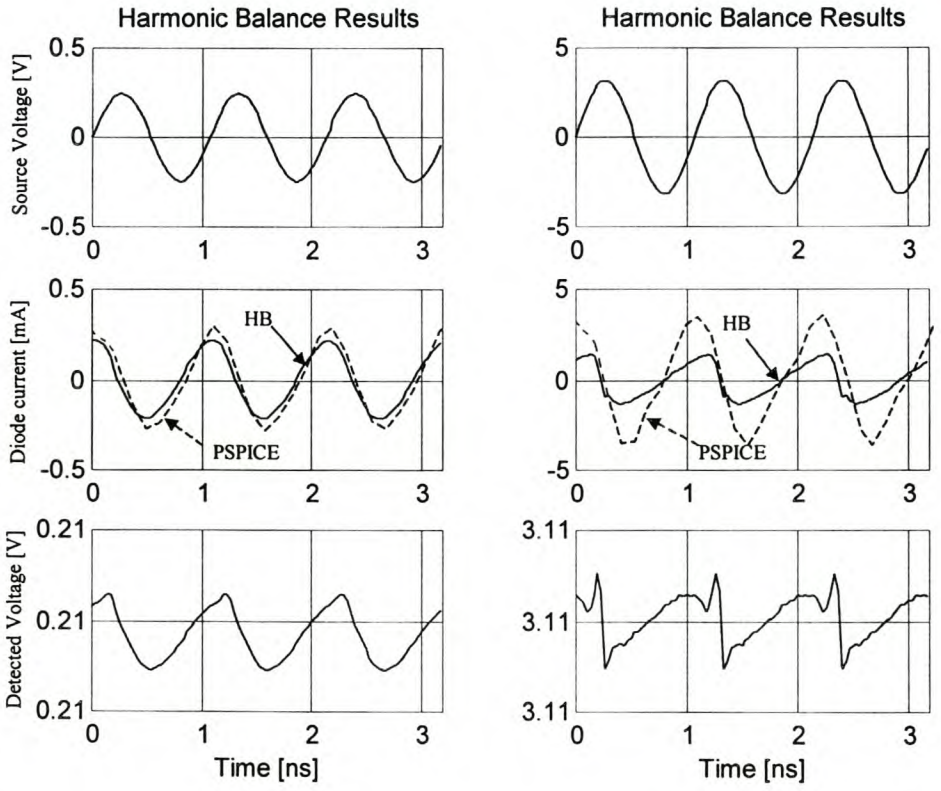


Figure 8-3 Time domain results with large signal input - Design example 1

From Fig. 8-3 is it clear that the HB-technique compares with PSPICE only up to a specific input power level. This can be explained by the implementation of eq [7-7], that describes the junction capacitance of the diode. When $V_p > 0.35$ V for the HSMS-2850 diode, eq [4-9] must be implemented as discussed in section 4-3 to be valid. PSPICE uses

a much more complex method to describe the junction capacitance at higher power levels, taking recombination, for example, into consideration. The dynamic range of this design, however, enables us to ignore differences in behavior at higher power levels, while simultaneously simplifying the HB technique.

To visualize the nonlinear effect of the diode at moderate power levels, a frequency response plot of the diode current is done, comparing the different harmonics obtained. ($V_p < 0.35$ V)

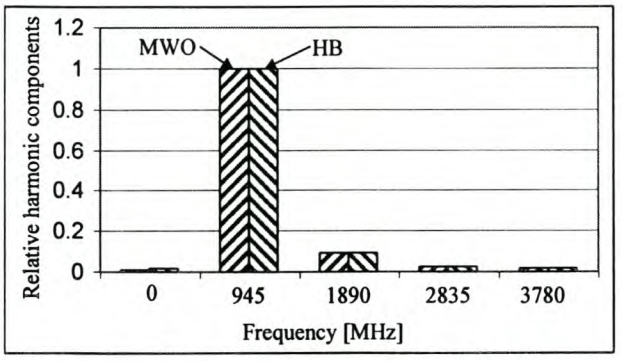


Figure 8-4 Presentation of harmonics of diode current with small signal input – Design example 1

The values in Fig. 8-4 are relative values of the fundamental harmonic. The fundamental harmonic is therefore unity for both the MWO simulation and the HB technique. (The harmonic components were verified with Microwave Office).

The difference in the detected voltage over the frequency band is non-mentionable for this small signal detector, especially if the effect of the matching circuit is not included in the analysis. This is the case for the design in discussion and a presentation of the detected voltage over the frequency band is not visualized with the HB technique.

When the matching circuit is included in the design, it is worth it to evaluate the detected response over the frequency band.

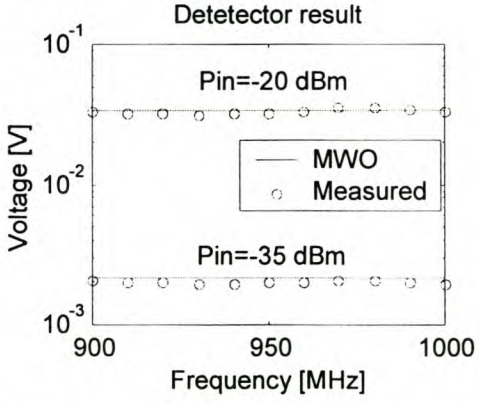


Figure 8-5 The response of the detected voltage over the frequency band – Design example 1

The effect of the center frequency match can be seen in Fig. 8-5. There is not a mentionable variance in the detected voltage over the frequency band. The result is adequate for the frequency band the detector is designed for.

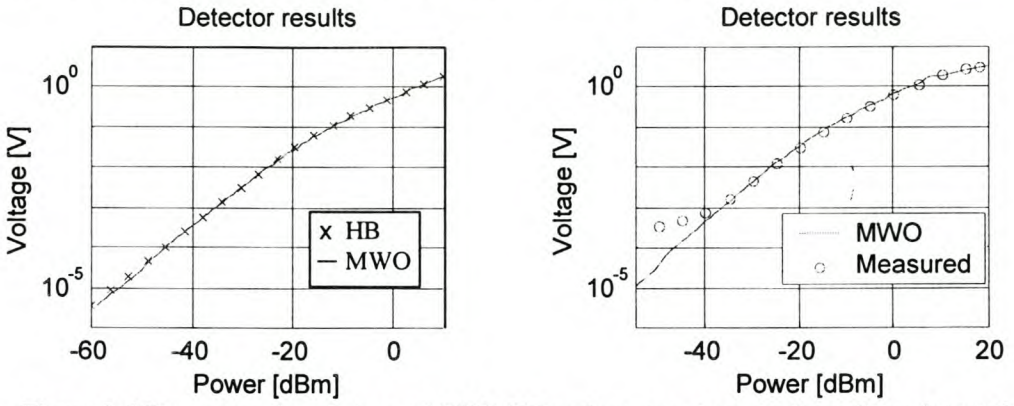


Figure 8-6 The comparison between MWO, HB and measured results for voltage detected – Design example 1

The performance of the detector over input power is presented in Fig. 8-6, with no matching done. The two simulations are in very good agreement. A comparison between the measured results and MWO simulations for the detector, with matching, is also shown in Fig. 8-6.

The effect of temperature variance is investigated for this design, although the effects are not critical for lower frequency designs.

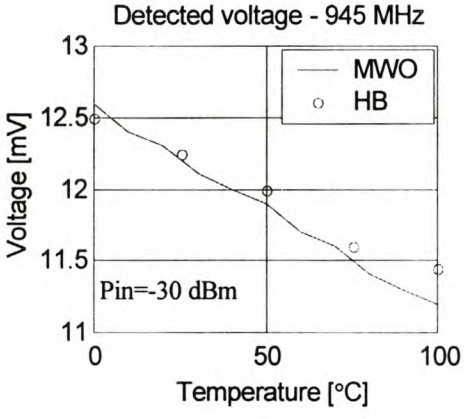


Figure 8-7 The effect of temperature on the detected voltage – Design example 1

Finally, the detector was designed to obtain a maximum dynamic range and therefore minimum tangential measurement. The method of measuring the TSS was discussed in chapter 3 and is now applied to the design example to verify the TSS predicted by the design equations.

TSS calculated [dBm]	TSS measured [dBm]	% error
Not Calculated	-45 dBm	*

8.3 Design Example 2 – 2.45 GHz

8.3.1 Verification of Matching Circuit

The input matching circuit for this design example, with 25 uA of bias current, is verified with measurement and indicated in Fig. 8-8.

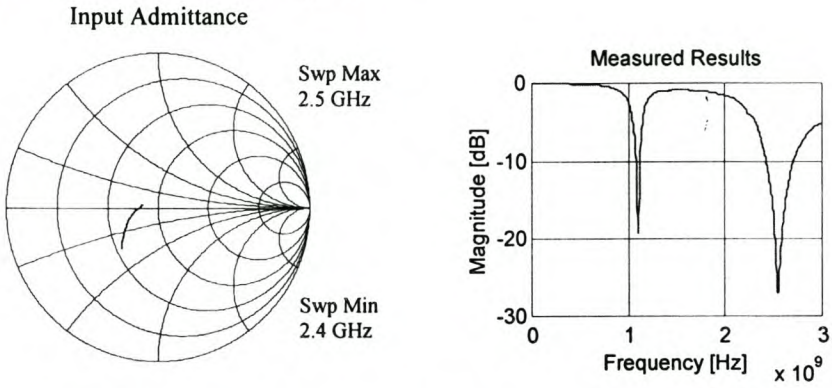


Figure 8-8 Measured results of the input match for Design example 2

The designed matching circuit proves to be a good match for the detector. The slight difference between the measured result and the designed match in chapter 6 can be explained by the effect of other parasitic parameters at the design frequency.

8.3.2 Simulations and Results

The time domain results of the HB technique applied on design example 2 are shown in Fig. 8-9.

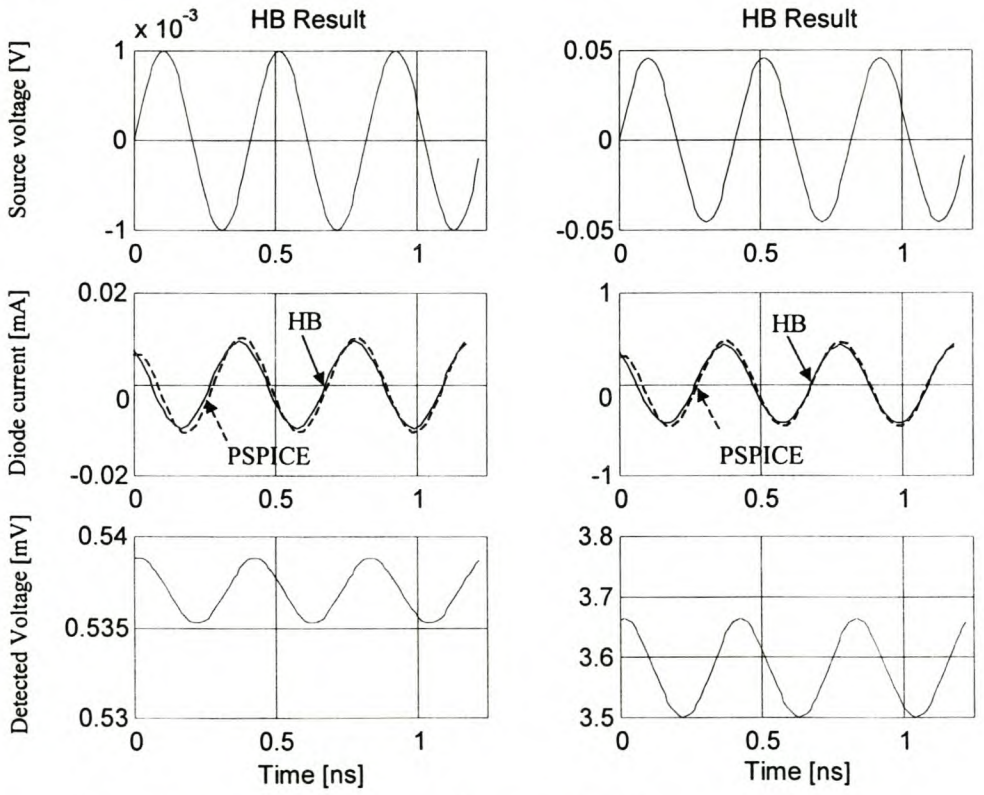


Figure 8-9 Time domain results with small signal input - Design example 2

The HB technique and PSPICE analysis are once again in good agreement for small signal input levels. From Fig. 8-9 it is visible that, as in design example 1, there is a need to improve the way the junction capacitance is defined. When the input voltage is greater than the built-in barrier potential (V_j), it is not possible to describe the junction capacitance with eq [7-7]. In appendix A the implementation of this equation is discussed for larger input levels, without creating discontinuities.

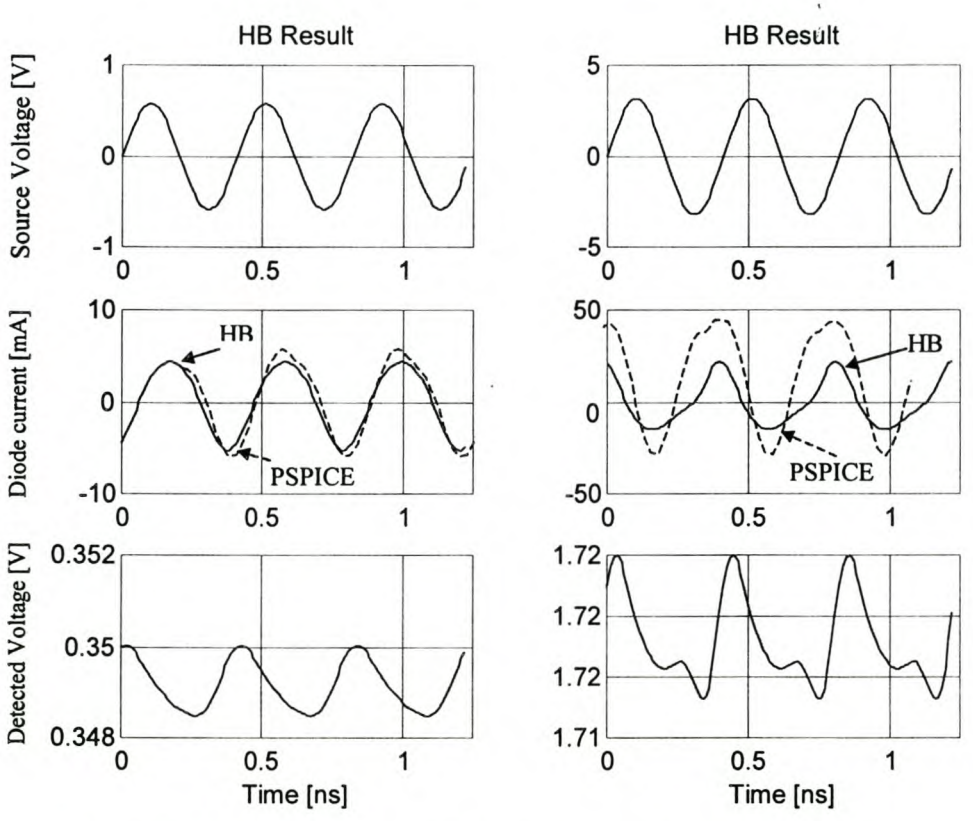


Figure 8-10 Time domain results with large signal input - Design example 2

The ripple effect in the detected voltage is more significant than is the case for design example 1. The reason for this is the higher frequency, with exactly the same output circuit and 3-dB cutoff frequency as in design example 1. It is, however, still adequate to work with the RMS value of the detected voltage as indicated in Fig. 8-10.

To get an indication of the harmonics present in the diode current for moderate input power levels, a comparative plot of the harmonics simulated by the HB technique and MWO simulation is generated.

The harmonics are once again relative values, with the fundamental harmonic as the weighted function.

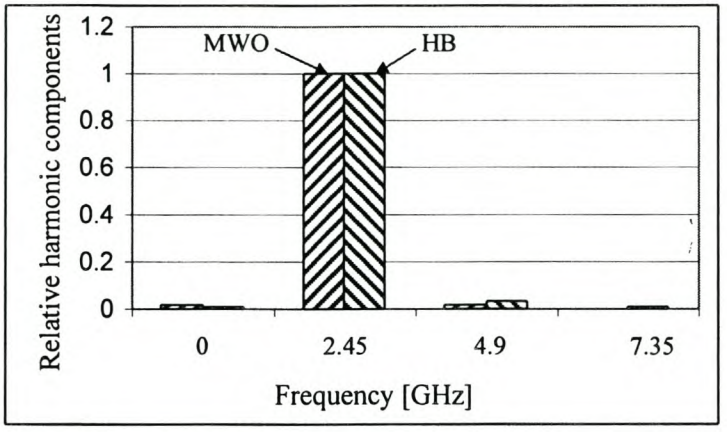


Figure 8-11 Presentation of harmonics of diode current with small signal input – Design example 2

The harmonics generated by the HSMS-2820 diode is very small for moderate power levels. There is a slight difference between the harmonics calculated by the HB technique and MWO. It can be the result of truncation errors in the optimization procedure, due to the very small values of the harmonics.

The performance of the detector over the designed frequency band is simulated with MWO and presented in Fig. 8-12. It is a narrowband design and therefore the variance over frequency is not really significant.

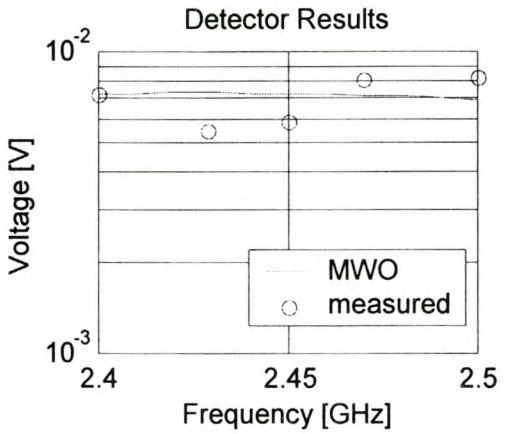


Figure 8-12 The response of the detected voltage over the frequency band – Design example 2

The performance of the detector over input power as simulated by the HB technique and MWO simulations is indicated in Fig. 8-13. The simulations were done with 25 uA bias current and no matching circuit added. A comparison between the measured results and those predicted by MWO, with the matching circuit added, is also shown in Fig. 8-13.

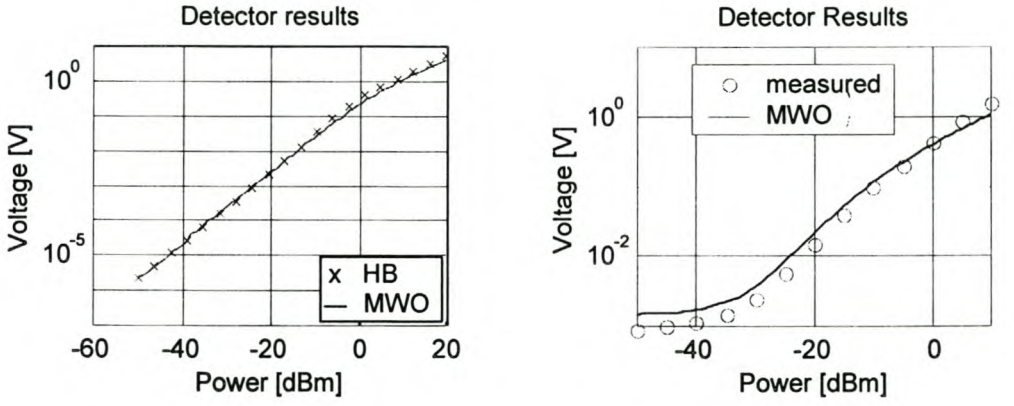


Figure 8-13 The comparison between MWO, HB and measured results for voltage detected - Design example 2

The effect of temperature variance is investigated for this design, although the effects are not critical for lower frequency designs. The detected voltage, as a function of temperature, for a fixed input is indicated in Fig. 8-14.

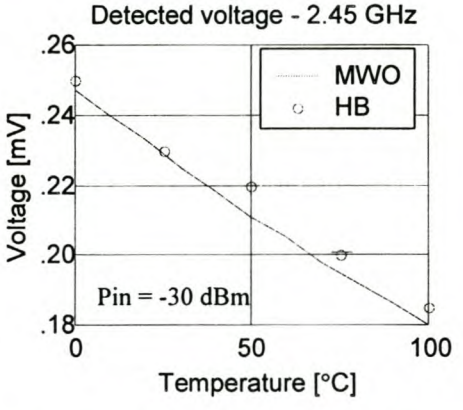


Figure 8-14 The effect of temperature on the detected voltage - Design example 2

Finally, the detector was designed to obtain a maximum dynamic range and therefore minimum tangential measurement. The method of measuring the TSS was discussed in chapter 3 and is now applied to the design example to verify the TSS predicted by the design equations.

TSS calculated [dBm]	TSS measured [dBm]	% error
-47 dBm	-43 dBm	8.5%

8.4 Design Example 3 – 10 GHz

8.4.1 Verification of matching circuit

The input matching circuit for this design example, with 25 uA of bias current, is verified by measuring the input admittance on the Vector Network Analyzer and comparing it to the calculated response in chapter 6.

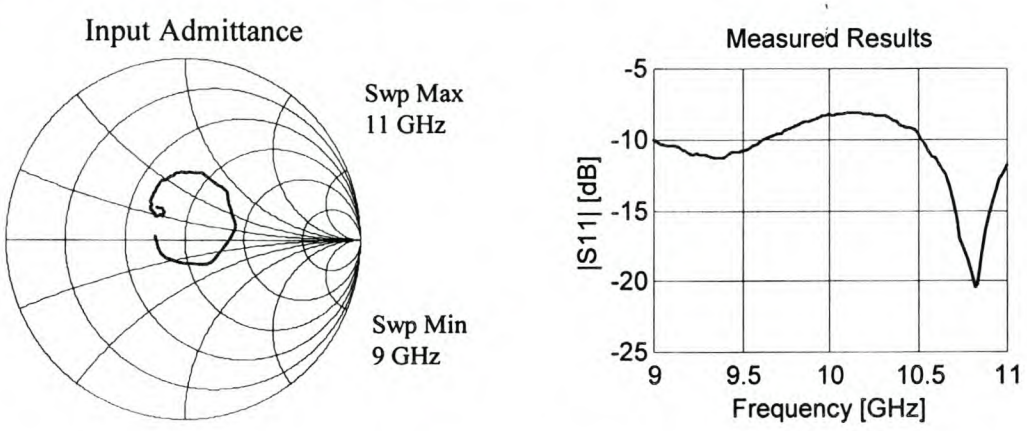


Figure 8-15 Measured results of the input match for Design Example 3

The detector is well matched in the frequency band from 9 GHz to 11 GHz. It is a narrower band than designed for. The response is reasonably flat, except between 10.5 GHz and 11 GHz where there is an improvement in the reflection. It would be possible to tune the input admittance (indicated in Fig. 8-15 on the Smith chart) to be centered in the middle of the chart, by adjusting the third element of matching. (refer to section 5-4) It is not done for this design, because the response is acceptable and in reasonable good agreement with the designed one.

8.4.2 Simulations and results

When a design in the X-band is done, the influence of the parasitic parameters in the Schottky diode model start to have a much larger influence on the detector performance. As discussed in chapter 4, the addition of the stray capacitance parameter (C_g) is necessary to extract a good model in the X-band. This extra parameter makes analysis and modeling more complex, especially the HB technique. More samples of the source voltage must be used to prevent aliasing. The addition of more samples is time consuming. The HB technique is implemented with the source voltage sampled with 128 samples. Only eight harmonics are used, with the other harmonics that are generated, set to zero.

The results of the HB technique are once again compared with PSPICE simulations for small and large input signals.

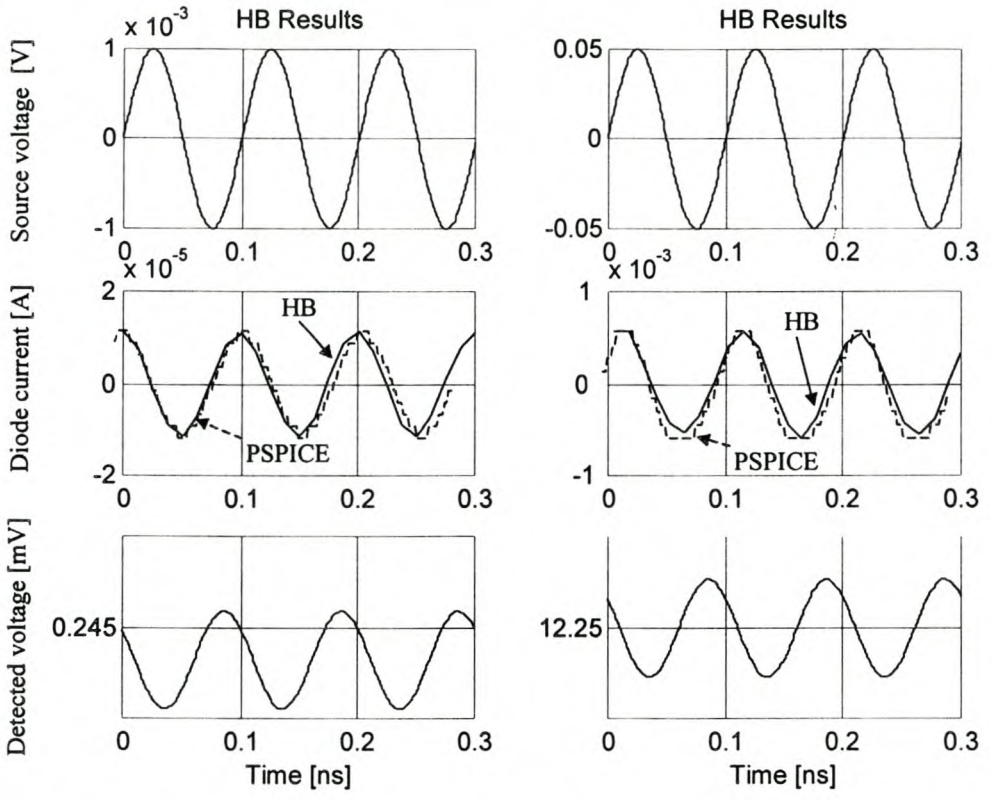


Figure 8-16 Timedomain results with small signal input – Design Example 3

The difference between the HB technique and PSPICE is already mentionable at low power levels as can be seen in Fig. 8-16. This proves the statement that there are much more to the analysis of detector circuits at higher frequencies than at lower frequencies.

At very low power levels as indicated in Fig. 8-16 the comparison between PSPICE and the HB technique is still very good. The presence of more harmonics in the diode current, calculated by the HB technique, is already visible in Fig. 8-16 and Fig. 8-17.

From Fig. 8-17 it is very clear that the presence of additional harmonics (in comparison with the PSPICE simulation) causes a serious difference between the two techniques.

The presentation of the harmonics generated by the diode at 10 GHz, calculated by both MWO and the HB technique will be discussed below.

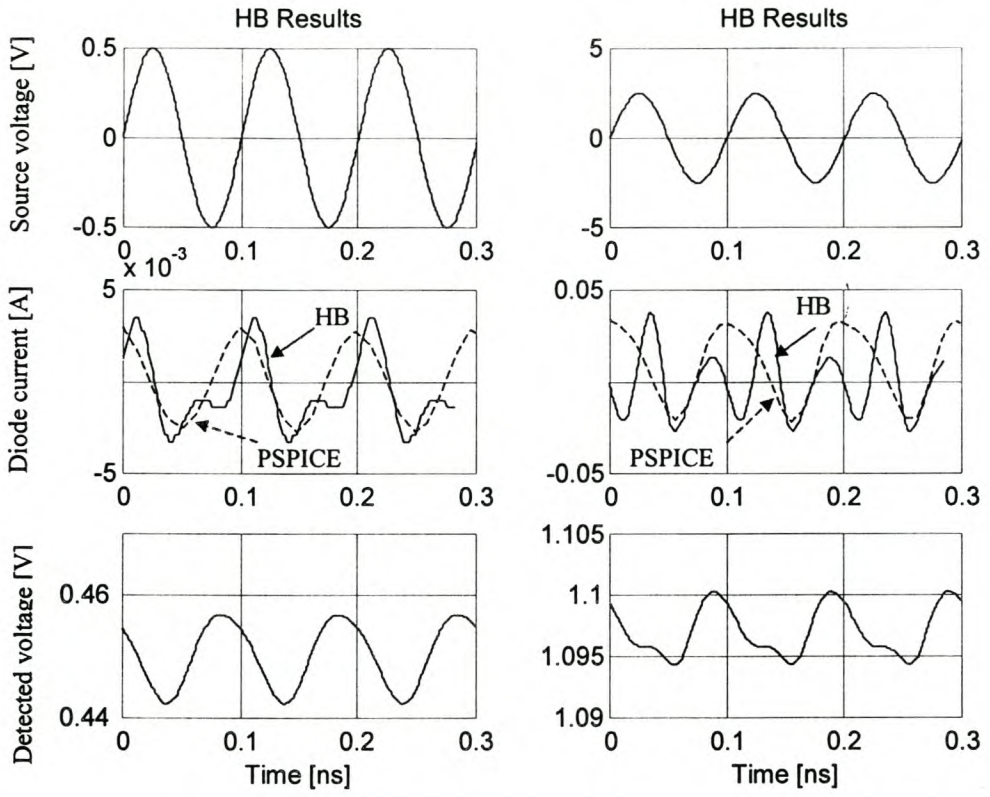


Figure 8-17 Time domain results with large signal input signal – Design example 3

The comparative harmonic plot is done for a moderate power level (P_{in} = 0 dBm). In Fig 8-18 the harmonics calculated by MWO and the HB technique are once again compared. The presence of bigger harmonics in the HB technique is the reason for the difference in the time domain diode currents.

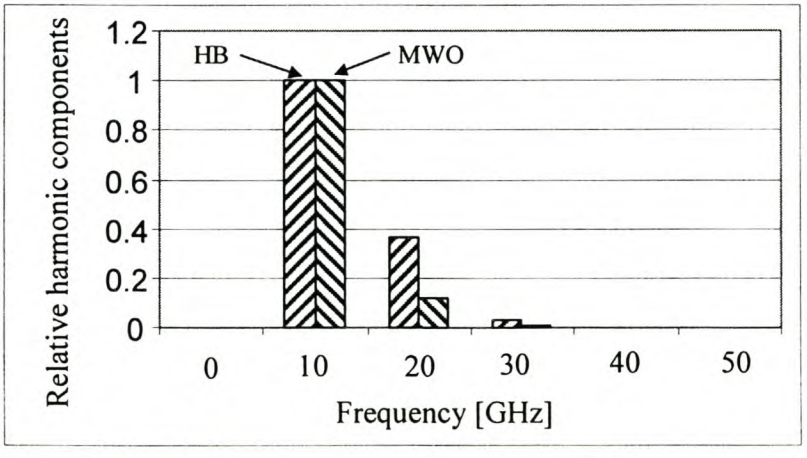


Figure 8-18 Presentation of harmonics of diode current with small signal input – Design Example 3

The reason for the difference between the two methods, that were up to this point very comparable, is not very clear. It must, however, be in the way the two non-linear junction parameters are characterized, because the non- linearity has its origin from these two parameters. The two parameters were characterized in chapter 4 over the designed frequency band for application in the HB technique and delivered good fittings with measured data.

Design example 3 is a wideband detector design and it is necessary to simulate the response of the detector (voltage detected) over frequency variance, to verify this design specification.

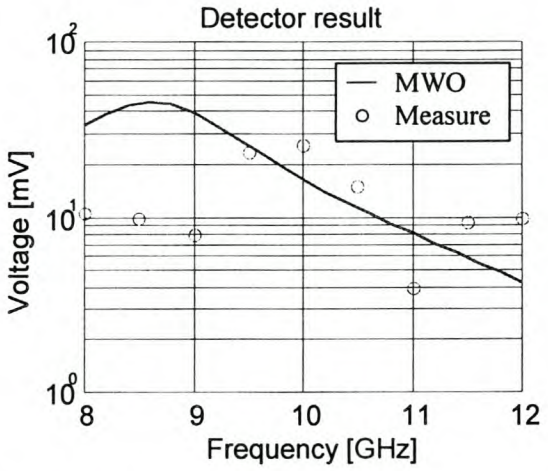


Figure 8-19 The response of the detected voltage over the frequency band - Design example 3

The comparison between MWO and the HB technique, for the response of the detector in designed frequency band, is indicated in Fig. 8-19. The response is not completely flat over the whole bandwidth, but a fair bit of flatness is obtained between 9 GHz and 11 GHz.

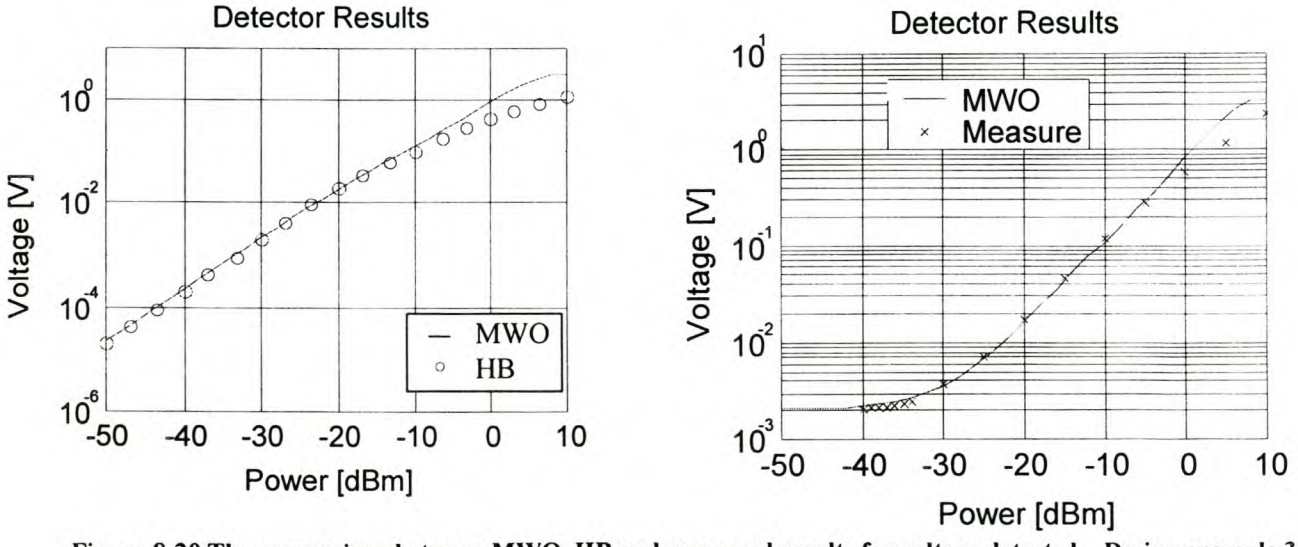


Figure 8-20 The comparison between MWO, HB and measured results for voltage detected – Design example 3

The main performance characteristic of the designed detector, namely the performance over input power is indicated in Fig. 8-20. The result of the HB technique and MWO simulation are firstly compared as it was done for the previous design examples. Secondly, a comparison is done between the measured results and MWO simulation, with the matching circuit added to the design. The measured results differ from the simulated ones at higher power levels, as was the case for the time domain results of Fig. 8-17. The reason is bigger harmonics are generated, practically, than calculated with MWO simulations, therefore the increase in non-linearity at higher power levels.

Temperature effects are important at higher frequency designs. It can have serious degradation effects on the performance of a detector. The influence of temperature variance is simulated by both the HB technique and MWO, but does not indicate a serious degradation. It is, however, still to be proven if the measured results compare well with these predictions.

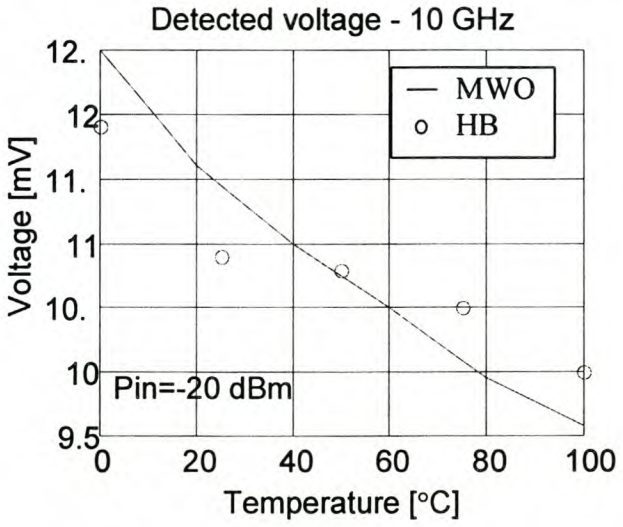


Figure 8-21 The effect of temperature on the detected voltage – Design example 3

Finally, the detector was designed to obtain a maximum dynamic range and therefore minimum tangential measurement. The method of measuring the TSS was discussed in chapter 3 and is now applied to the design example to verify the TSS predicted by the design equations.

TSS calculated [dBm]	TSS measured [dBm]	% error
-38 dBm	-41 dBm	7.3%

The output circuit is not designed for maximum bandwidth (considering the cutoff frequency) as was initially stated for the tangential sensitivity calculation. That is the reason for the improvement in TSS.

8.5 Conclusion

It was shown in this chapter that the Harmonic Balance algorithm delivers very good results compared to practical measurements and MWO simulations. Measurements were made for different input power levels and varying frequencies.

The description of the junction capacitance for larger power levels, when V_{port} becomes greater than the built in barrier potential, needs still some attention. It is possible to use the Spice model to describe the junction capacitance behavior, but it requires parameters that cannot be extracted through simple measurements.

The Harmonic Balance method creates larger harmonics at higher frequencies than MWO simulations, but it is still in good agreement with measurements made.

9 Conclusions and Recommendations

9.1 Conclusions

The subject on the design and characterization of diode detectors are thoroughly discussed in this thesis. The possibility to develop an error-correcting algorithm to compensate for any non-linear effects, for example high frequency, higher power level and temperature effects is illustrated. The response curve of a diode detector is divided into two regions, namely the square-law and linear region. By predicting the response curve (voltage detected over input power level) with analysis algorithms, it is possible to correct for the above-mentioned nonlinear effects and to extend the dynamic range of the detector.

The necessity of obtaining an accurate diode model is also underlined. Without an accurate model, it is impossible to get accurate results. The diode model is the underlying backbone of proper design and analysis.

Furthermore, a step-by-step procedure is presented to design diode detectors according to certain design specifications, namely for maximum sensitivity or maximum bandwidth. The design of the matching circuit is important for obtaining optimum results. A three-step transmission line matching technique is applied to some design examples, performing either a narrowband or wideband match.

9.1.1 The Diode Model

The extraction of the Schottky diode model delivers good results, comparing very well with the small signal measurements. The Spice model is extracted through DC and small signal measurements. The intrinsic nonlinear junction parameters are extracted first. De-embedding the model to the intrinsic level, using the data sheets' values for the package parasitic elements, does this. The amount of parasitic elements used in the model depends on the frequency range of the extraction. The model is more complex at frequencies above 6 GHz. The nonlinear parameters are calculated at a specific biasing level. This technique delivers good results, but after applying Newton's method in optimizing the model, results are improved. The method of optimizing the diode model is time consuming, but sometimes necessary, if the method of de-embedding does not give acceptable results. The sensitivity of the parameters to the error function is, however, not always good enough for convergence. Each parameter is therefore optimized individually and de-embedded, from the most sensitive to the least sensitive parameter.

The Schottky diode models of all the diodes used in this thesis are extracted through this method.

9.1.2 The Design

The design of diode detectors is broken into three parts:

Firstly, by calculating an optimum bias current, the diode can be optimized for maximum sensitivity and dynamic range or maximum bandwidth. Design equations are applied to calculate the bias current. The addition of bias current also compensates for some temperature effects.

Secondly, the output circuit is designed. The output circuit does not really need any design, although, if the detector is used as a receiver it is a good idea to consider the cutoff frequency of the low pass structure. Furthermore, the output resistance of the detector must be kept as large as possible for the detector to be sensitive over small input levels.

Thirdly, the matching circuit is designed. The matching circuit has a large influence on the detector's performance, especially over frequency variation. Good results are obtained with the narrowband and wideband matching procedure. The matching circuits are practically verified.

9.1.3 The Analysis and Error-correcting Methods

One of the main aspects of this thesis is to present an analysis algorithm that will make it possible to correct for the nonlinear behavior of diode detectors. The Harmonic Balance method is presented as one method and the Ritz-Galerkin method as another.

The Ritz-Galerkin method is successful in providing the basis for an error-correcting algorithm for power-measurement systems when there are variations in temperature, load and bias current. It does not consider high frequency parasitic effects.

The results obtained with the Harmonic Balance method compares very well with other simulation packages and practical measurements. At higher frequencies (X-band) the Harmonic Balance method generates larger higher order harmonics than other simulation packages. The reason for this is the description of the nonlinear junction capacitance, which is a very important parameter at higher frequencies. The combination of high frequency (X-band) and higher input power level (Pin > 10 dBm) has a large influence on results.

The Harmonic Balance method can be used as an error-correcting algorithm to compensate for the nonlinear effects of diode detectors, but still needs some refinement at the combination of higher power levels and high frequencies (X-band and higher).

9.2 Recommendations

The use of different detector topologies still needs to be investigated. The use of two back-to-back diodes was mentioned to increase the level of voltage to be detected and to decrease the input impedance – simplifying the matching circuit.

It was also discussed in Appendix G that using a parallel diode pair reduces the temperature effects of diode detectors even more. This topology has not been investigated and practically verified.

Finally, the Harmonic Balance algorithm can be extended to do the error-correction of diode detectors in real-time in a detector system.

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Appendix A

A1 The Spice Model

PSPICE uses three equivalent circuits in diode analysis: transient, AC, and noise circuits. Components of these circuits form the basis for all element and model equations. The noise circuit, together with the temperature equations will not be discussed in this appendix, (refer to [14])

The fundamental component in the DC equivalent circuit is the DC diode current (id). For noise and AC analyses, the actual id current is not used. The partial derivative of id with respect to the terminal voltage vd is used instead. The name for this partial derivative is, conductance.

$$gd = \frac{\partial id}{\partial vd} \qquad \textbf{[A1- 1]}$$

The drain current (id) equation accounts for all basic DC effects of the diodes. Capacitance effects are assumed to be separate from the id equations.

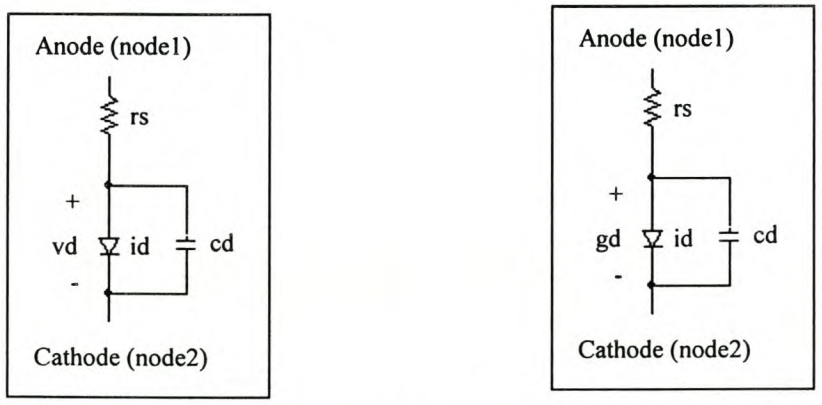

Figure A1-1Equivalent circuits for diode transient analysis and diode AC analyses

Function	Parameters
DC Parameters	IBV, IK, IS, ISW, N, RS, VB, RS
Geometric junction	AREA, M, PJ
Capacitance	CJ, CJP, FC, FCS, M, MJSW, PB, PHP, TT

Table A1-1 Junction Diode Model Parameters

(refer to [14] for a description of all the parameters)

A1.1 Junction DC equations

The basic diode is modeled in three regions:

- Forward bias
- Reverse bias
- Breakdown regions

For a forward bias diode, the anode is more positive than the cathode. The diode is turned on and conducts above 0.6 volts. The model parameter Rs should be set to limit conduction current. As the forward bias voltage increases past 0.6 volts, the limiting resistor prevents the value of the diode current from becoming too high and the solution from converging.

Forward Bias: vd > -10.vt

$$id = ISeff\left(e^{\frac{vd}{N.vt}} - 1\right) \qquad \textbf{[A1- 2]}$$

$$vd = v_{node1} - v_{node2} \qquad \textbf{[A1- 3]}$$

For reverse bias, the anode (node1) is more negative than the cathode. The diode is turned off and conducts a small leakage current.

Reverse Bias: Bveff < vd < -10.vt

$$id = -ISeff \qquad \textbf{[A1- 4]}$$

For breakdown, the parameter BV (VB) is set, inducing reverse breakdown or avalanche. This effect occurs when the anode-cathode voltage is less than BV. This action is modeled by measuring the voltage (BV) and the current (IBV) at the reverse "knee" or onset of avalanche.

Breakdown: vd < -Bveff

$$id = -ISeff.e^{-\left(\frac{vd+BVeff}{N.vt}\right)} \qquad \textbf{[A1- 5]}$$

The BV parameter is adjusted as follows to obtain BVeff:

$$ibreak = -ISeff\left(e^{\frac{-BV}{N.vt}} - 1\right) \qquad \textbf{[A1- 6]}$$

If IBVeff > ibreak, then,

$$BVeff = BV - N.vt.\ln\left(\frac{IBVeff}{ibreak}\right) \qquad \textbf{[A1- 7]}$$

Otherwise,

$$IBVeff = ibreak \qquad \text{[A1- 8]}$$

Most diodes do not behave as ideal diodes. The parameters IK and IKR are called high level injection parameters. They tend to limit exponential current increase.

Forward Bias:

$$id = \frac{id1}{1+\left(\frac{id1}{IKeff}\right)^{1/2}} \qquad \text{[A1- 9]}$$

Reverse bias:

$$id = \frac{id1}{1+\left(\frac{id1}{IK\,\mathrm{Re}\,ff}\right)^{1/2}} \qquad \text{[A1- 10]}$$

where id1 is

For vd >= -Bveff:

$$id = ISeff\left(e^{\frac{vd}{N.vt}} - 1\right) \qquad \text{[A1- 11]}$$

Otherwise:

$$id = ISeff\left(e^{\frac{vd}{N.vt}} - 1\right) - ISeff\left[e^{-\left(\frac{vd+BVeff}{N.vt}\right)} - 1\right] \qquad \text{[A1- 12]}$$

The reverse saturation current IS, emission coefficient N, and model parameter RS are estimated from DC measurements of the forward biased diode characteristics. N is determined from the slope of the diode characteristic in the ideal region. In most cases, the emission coefficient is the value of unit, but is closer to 2 for MOS diodes.

In practice, at higher levels of bias, the diode current deviates from the ideal exponential characteristic. This deviation is due to the presence of ohmic resistance in the diode as well as high-level injection effects. The deviation of the actual diode voltage from the ideal exponential characteristic at a specific current determines the values of RS. In practice, RS is estimated at several values of id and averaged, since the value of RS depends upon diode current.

A1.2 Diode Capacitance Equations

The diode capacitance is modeled by cd in Fig.A1-1. The capacitance, cd, is a combination of diffusion capacitance (cdiff), depletion capacitance (cdep), metal (cmetal), and poly capacitances (cpoly).

$$cd = cdiff + cdep + cmetal + cpoly \qquad \textbf{[A1- 13]}$$

Diffusion Capacitance Equations

The transit time (TT) models the diffusion capacitance, caused by injected minority carriers. In practice, TT is estimated from pulsed time-delay measurements.

$$cdiff = TT\frac{\partial id}{\partial vd} \qquad \textbf{[A1- 14]}$$

Depletion Capacitance Equations

The depletion capacitance is modeled by junction periphery capacitances. The formula for both bottom area and periphery capacitances is similar, except each has its own model parameters. There are two equations for forward bias junction capacitance.

The junction bottom area capacitance formula is:
vd < FC. PB

$$cdepa = Cjeff\left(1 - \frac{vd}{PB}\right)^{-MJ} \qquad \textbf{[A1- 15]}$$

vd > FC.PB

$$cdepa = Cjeff\left(\frac{1 - FC(1+MJ) + MJ\frac{vd}{PB}}{(1-FC)^{(1+MJ)}}\right) \qquad \textbf{[A1- 16]}$$

The junction periphery capacitance formula is:

Vd < FCS.PHP

$$cdepp = CJPeff\left(1 - \frac{vd}{PHP}\right)^{-MJSW} \qquad \textbf{[A1- 17]}$$

vd > FCS.PHP

$$cdepp = CJPeff\left(\frac{1 - FCS(1 + MJSW) + MJSW\,\frac{vd}{PHP}}{(1 - FCS)^{(1+MJSW)}}\right) \qquad \textbf{[A1- 18]}$$

then,

$$cdep = cdepa + cdepp \qquad \textbf{[A1- 19]}$$

Appendix B

B1 Newton's Method

The most popular robust method for the solution of systems of nonlinear algebraic equations is Newton's method.

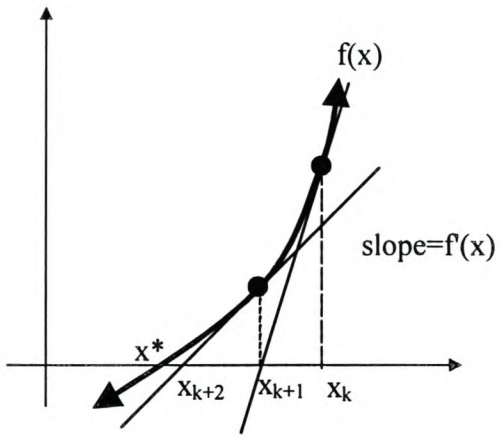

Figure B1-1 Geometrical representation of Newton's method in one dimension

Let f: $D \subset \Re \rightarrow \Re$ be a function for which a root is sought. Also, assume that an initial estimate of the root is available. At the kth iteration, f(x) is approximated by the function

$$\hat{f}(x) = f(x_k) + f'(x_k)(x - x_k) \qquad \textbf{[B1- 1]}$$

This is the linearization of f(x) around x_k. The formula that defines Newton's method in one dimension is obtained by making x_{k+1} equal to the root of the function, that is,

$$x_{k+1} = x_k - \frac{f(x_k)}{f'(x_k)} \qquad \textbf{[B1- 2]}$$

Eq. B1-2 is represented graphically in Fig. B1-1

Newton's method in n dimensions can be derived using the same reasoning. First, an affine function for each component of F(x) is defined by

$$\hat{f}^i(x) = f^i(x_k) + \sum_{j=1}^{n} \frac{\partial f^i(x_k)}{\partial x^j}\left(x^j - x_k^j\right) \qquad i = 1,\ldots,n \qquad \textbf{[B1- 3]}$$

This is the tangent hyperplane of $f^{i}(x)$ at x_k. When the n equations in B1-3 are combined in a column vector, the result is

$$\hat{F} = F(x_k) + F'(x_k)(x - x_k) \qquad \textbf{[B1- 4]}$$

Finally, a new estimate of the solution is obtained by computing the root of the n-dimensional affine function. Newton's method is defined by the resulting iterative formula

$$x_{k+1} = x_k - \left(F'(x_k)\right)^{-1} F(x_k) \qquad \textbf{[B1- 5]}$$

The use of eq B1-5 clearly requires the jacobian of F(x) to exist and be invertible in the neighborhood of the solution.

B2 Optimization Algorithm – DC Characteristics

Newton's method is applied to the DC characteristics of the diode to extract three of the diode's parameters. These parameters are Is (saturation current), Rs (series resistance) and α (α=e/nkT, which is defined before in chapter 4)

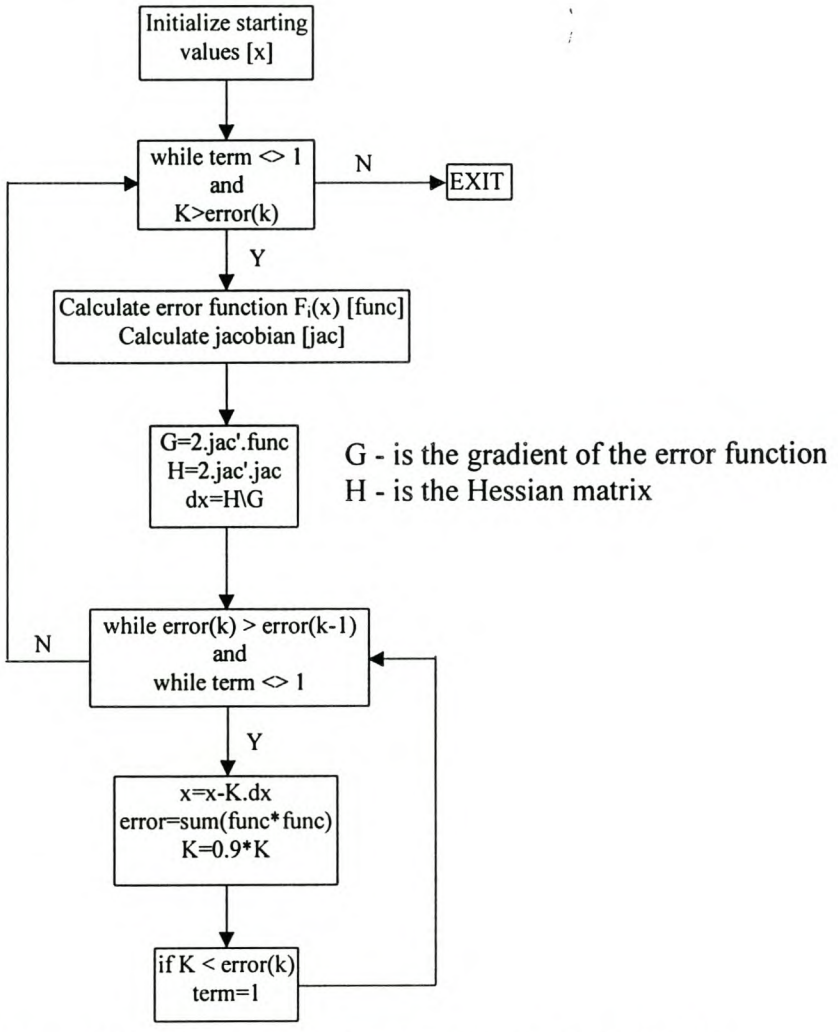

Figure B2-1 Block diagram representation of the optimization algorithm – DC characteristics

Newton's method is applied to a three-dimensional problem (Is, Rs and α). The error function, F(x), is a column vector with its length depending on the number of DC measurement made. The error function is described by

$$F^i_{error}(x) = \left| F^i_{measure}(x) - F^i_{calc}(x) \right| \qquad i = 1,\ldots,n \qquad \textbf{[B2-1]}$$

where

$F^i_{measure}(x)$ is the measured diode current for n different port voltages.

$F^i_{calc}(x)$ is the calculated diode current from equation [4-2] for the same port voltages

x is the three parameters Rs, Is, α.

The error function to be minimized is the sum of the squares of eq. B2-1.

$$error = \sum_{i=1}^{n} \left(F^i_{error}(x)\right)^2 \qquad \textbf{[B2-2]}$$

A block diagram representation of the optimization algorithm is presented in Fig. B2-1

The calculation of the jacobian matrix is done numerically. It was not necessary to put any constraints on the parameters being optimized, due to the simplicity of the error function.

Appendix B

B3 Optimization Algorithm – Small Signal Parameters

To refine the Schottky diode model, the calculated small signal parameters are fitted to the measured parameters. This procedure is done with an optimization algorithm, minimizing an error function.

The error function is

$$F(\bar{x}) = \sum_{i=1}^{m} e_i(\bar{x})^2 \qquad \text{[B3-1]}$$

where

$$e_i(\bar{x}) = \frac{1}{\sigma_{s11}} \left| s11^i_{measure} - s11^i_{model} \right| + \frac{1}{\sigma_{s21}} \left| s21^i_{measure} - s21^i_{model} \right| \qquad \text{[B3-2]}$$

m - number of points

$\bar{x}$ - unknown (row vector of model parameters)

σ_k - normalizing factor to ensure all the parameters have an equal contribution towards the function

$$\sigma_k = \max \left| S_{k\,model} \right| \qquad \text{[B3-3]}$$

The error function is minimized by adding Δx to the initial values.

$$\bar{x}^{n+1} = \bar{x}^n + \Delta\bar{x} \qquad \text{[B3-4]}$$

where

$$\Delta\bar{x} = \frac{g(\bar{x})}{H(\bar{x})} \qquad \text{[B3-5]}$$

In eq B3-5 $g(\bar{x})$ is the gradient of the error function and $H(\bar{x})$ is the Hessian matrix defined as:

$$g(\bar{x}) = 2J^T e \qquad \text{[B3-6]}$$

$$H \cong 2J^T J \qquad \text{[B3-7]}$$

with J the Jacobian matrix

$$J = \begin{bmatrix} \frac{\partial f_1}{\partial x_1} & \frac{\partial f_1}{\partial x_2} & \cdots & \frac{\partial f_1}{\partial x_j} \\ \frac{\partial f_2}{\partial x_1} & \frac{\partial f_2}{\partial x_2} & \cdots & \frac{\partial f_2}{\partial x_j} \\ \cdots & \cdots & \cdots & \cdots \\ \frac{\partial f_n}{\partial x_1} & \frac{\partial f_n}{\partial x_2} & \cdots & \frac{\partial f_n}{\partial x_j} \end{bmatrix} \qquad \textbf{[B3-8]}$$

After the search direction is obtained, a linear search is performed in this direction until a point is found that will result in an improvement of the error. This is done by adjusting α in eq B3-9 if there is not an improvement in error.

$$\bar{x}^{n+1} = \bar{x}^n + \alpha \Delta \bar{x} \qquad \textbf{[B3-9]}$$

Limits are also placed on the variables.

As was discussed in chapter 4, the success of optimization of all the model parameters simultaneously, is not guaranteed. More success was obtained by optimizing the most sensitive parameter first and holding the others constant. The starting values for optimization is obtained with the de-embedding method.

B3.1 The transformation of badly scaled systems

The reason why the optimization of all the model parameters is not that successful, is because of the difference in sensitivity. Each parameter does not have the same effect on the error function. This problem is partly solved by transforming the system to an orthogonal system. The rotation and scaling of the system is discussed in this section.

The error function for Newton's method are defined as

$$F(x) = \sum_i^N f_i(x)^2 \qquad \textbf{[B3-10]}$$

where

- f_i - the error at a specific frequency
- x - the model parameters
- N - number of points

In Newton's method, a vector Δx is searched for that will result in a minimum x*, if added to the current values of the parameters, x_0. x* indicates the minimum of the quadratic approach that fits the error function

$$x^* = x^0 + \Delta x \qquad \textbf{[B3- 11]}$$

By using a Taylor expansion around this minimum results in the following equation

$$F(x^*) = F(x^0 + \Delta x) \cong F(x^0) + \Delta x^T g(x^0) + \tfrac{1}{2} \Delta x^T H(x^0) \Delta x \qquad \textbf{[B3-12]}$$

where

$g(x^0)$ - is the gradient vector,

$H(x^0)$ - is the Hessian matrix at the current point

The Hessian matrix is symmetric due to the $J^T J$ term and is always a semi-definite that results in positive eigenvalues. The Hessian matrix can be replaced by

$$H = QDQ^T \qquad \textbf{[B3-13]}$$

where Q is a orthogonal matrix with eigenvectors and D a diagonal matrix with D_{ii} the eigenvalues of the Hessian matrix.

This results in the following substitution

$$y = D^{1/2} Q^T x \qquad \textbf{[B3-14]}$$

which also means that

$$x = QD^{-1/2} y \qquad \textbf{[B3-15]}$$

Eq B3-12 can now be written as

$$\begin{aligned} & F_x(x^*) = F_x(QD^{-1/2} y^*) = F_x(QD^{-1/2}(y + \Delta y)) \\ & = F_x(QD^{-1/2} y^0) + (QD^{-1/2} \Delta y)^T g_x(QD^{-1/2} y^0) + \tfrac{1}{2}(QD^{-1/2} \Delta y)^T QDQ^T (QD^{-1/2} \Delta y) \\ & = F_x(QD^{-1/2} y^0) + \Delta y^T D^{-1/2} Q^T g_x(QD^{-1/2} y^0) + \tfrac{1}{2} \Delta y^T \Delta y \end{aligned} \qquad \textbf{[B3-16]}$$

The function, F_x, and the gradient function, g_x, is still defined in terms of variables in the x-region, but it can, however be converted to the y-region.

The function F_y is defined to let $F_y(y^0) = F_x(x^0)$. The gradient vector, g_y, can be defined as

$$\bar{g}_y = \left(\frac{\partial F}{\partial \bar{y}}\right)^T = \left(\frac{\partial F}{\partial \bar{x}}\frac{\partial \bar{x}}{\partial \bar{y}}\right)^T = \left(\bar{g}_x{}^T\frac{\partial \bar{x}}{\partial \bar{y}}\right)^T = \left(\frac{\partial \bar{x}}{\partial \bar{y}}\right)^T \bar{g}_x = \left(QD^{-1/2}\right)^T \bar{g}_x = D^{-1/2}Q^T\bar{g}_x \quad \textbf{[B3-17]}$$

Equation B3-16 is now described with the above mentioned substitusions

$$F_y(y^*) = F_y(y+\Delta y) = F_y(y^0) + \Delta y^T g_y(y^0) + \tfrac{1}{2}\Delta y^T \Delta y \quad \textbf{[B3-18]}$$

To find Δy from this equation is not difficult, because H_y=1 and by calculating $g_y(y^0)$

$$\Delta y = -g_y(y^0) \quad \textbf{[B3-19]}$$

Newton's method therefore simplifies to a steepest gradient method in the orthogonal space.

The optimization algorithm is implemented in the same way as was done in Appendix B2 (Fig. B2-1).

Appendix C

C1 TRL Calibration Method

The Through-Reflect-Line (TRL) calibration method was partially discussed in chapter 4, but will be done in more detail in this appendix.

The reason for the need for this calibration method is already discussed in chapter 4. More emphasis is laid on the design of a TRL-kit and the measurements made with it.

C1.1 TRL Design

The design equations discussed in chapter 4 is used to design the TRL-kit presented in Fig. C1-1. The parameters are listed in table C1-1.

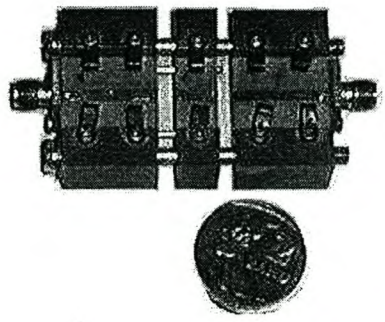

Figure C1-1 The TRL calibration jig

Relative dielectric, ε_r	2.5
Substrate height	1.133 mm
Line width [50 Ω]	3.182 mm
Through line	40 mm
Reflect line	20 mm
Delay Line	59 mm

Table C1-1 Substrate parameters and TRL standard length dimensions

C1.2 Measurements

The three calibration standards are measured only once over the frequency band the jig was designed for [6 GHz]. These measurements are used to extract all the s-parameters of the measured diodes.

The calibration measurements (S11, S21, S12, S22) for the through, reflect and line standards, together with the device measurements, are used in a MATLAB algorithm to extract the s-parameters of the device. The calibration is done externally based on the work presented by Engen and Hoer [50].

The effect of the calibration on measured results is visualized in Fig. C1-2 and Fig. C1-3.

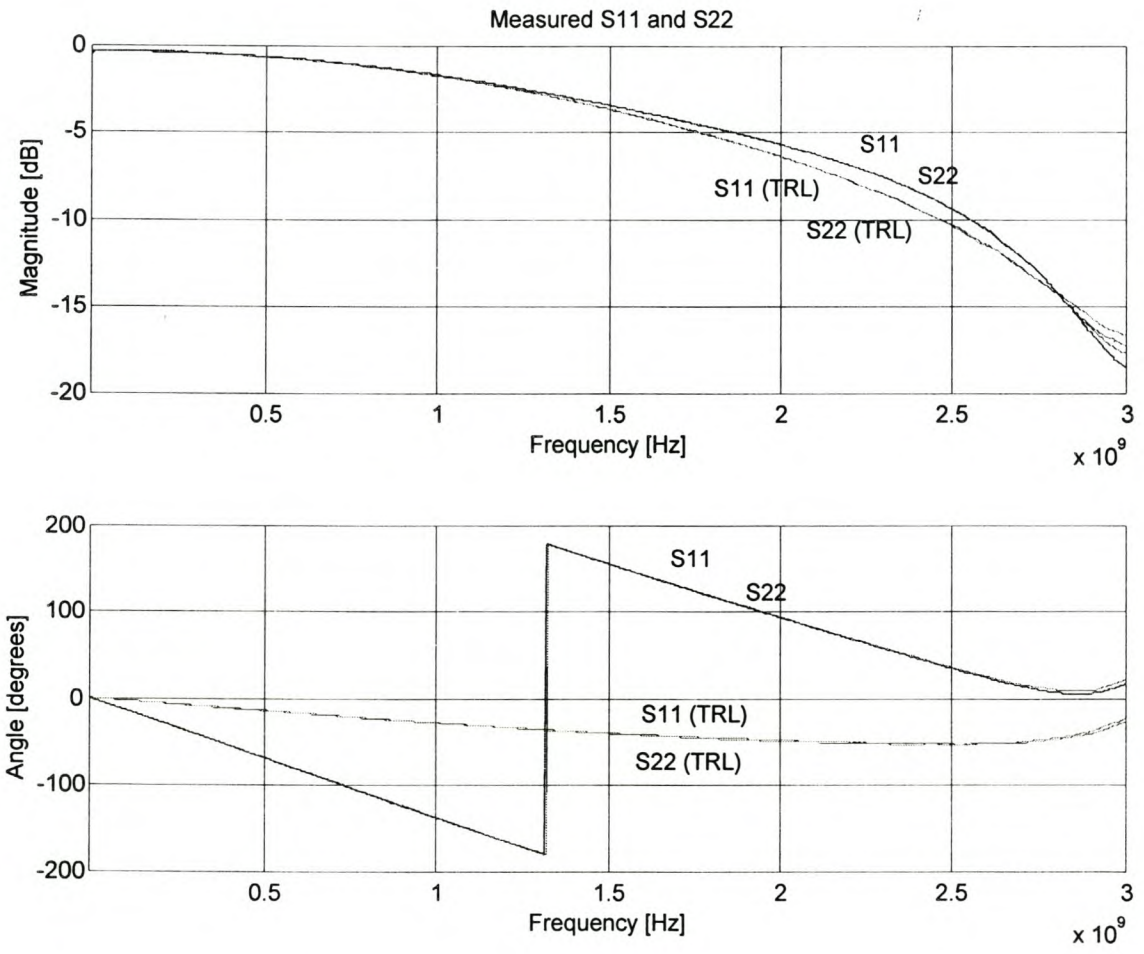

Figure C1-2 The measured small signal parameters of a diode – (1)

The biggest correction can be seen in the measured phase of the diode. The effect of the connectors and feeding transmission lines is eliminated.

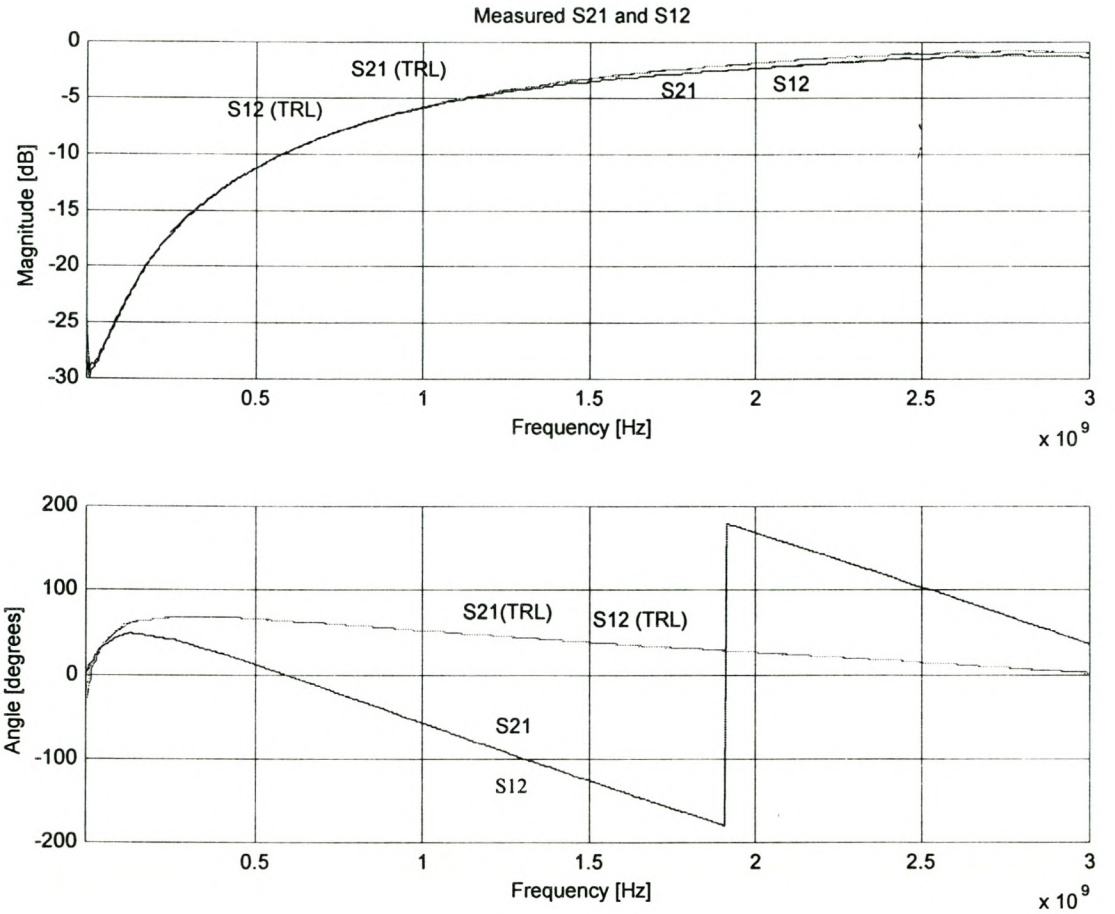

Figure C1-3 The measured small signal parameters of a diode (2)

Appendix D

D1 Impedance matching with Chebyshev filters

Explicit formulas for Chebyshev impedance matching networks, filters and interstages are presented by R. Levy [46]

A simplified theory is presented for the derivation of optimum matching networks for a restricted class of RCL loads.

D1.1 The derivation of matching networks

The requirement is an optimum matching circuit, using a given number of circuit elements, for the parallel combination of a capacitance C shunting a resistance R, across a frequency band from ω_1 to ω_2 rad/s. Other types of loads, e.g. inductive or series, may be treated similarly. The bandwidth is

$$\omega' = \omega_2 - \omega_1 \qquad \textbf{[D1-1]}$$

The first step is to obtain a lowpass match from 0 to ω'. After the lowpass matching network has been obtained, a simple lowpass-to-bandpass frequency transformation will then center the band as required. The shunt susceptance of the capacitance C is normalized to 1 mho and a passband edge of 1 rad/s, giving the normalized susceptance

$$\alpha = \omega' RC \qquad \textbf{[D1-2]}$$

A good approximation to the ideal rectangular characteristic is given by an equal ripple function as shown in Fig. D1-1, where the insertion loss of the matching network is given by

$$A(\omega) = 1 + K^2 + \varepsilon^2 T_n^2(\omega) \qquad \textbf{[D1-3]}$$

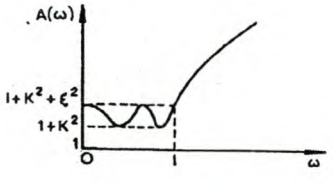

Figure D1-1 Chebyshev insertion loss function

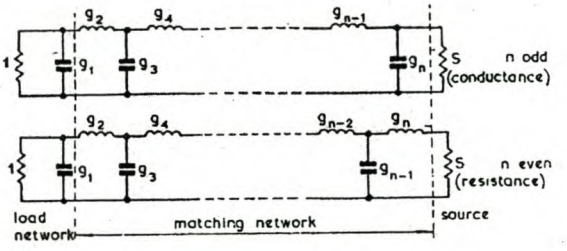

Figure D1-2 Lowpass matching networks

$T_n(\omega)$ is the chebyshev function of the first kind of degree n, i.e.

$$T_n(\omega) = \begin{cases} \cosh\left(n \cosh^{-1} \omega\right) & |\omega| \geq 1 \\ \cos\left(n \cos^{-1} w\right) & |w| \leq 1 \end{cases} \qquad \text{[D1-4]}$$

K and ε are constants determining the maximum and minimum values of A(ω) in the passband 0 to ω'. N is the number of elements in the network, including the load susceptance, as shown in Fig. Here, shunt capacitances g1, g3, g5,... represent susceptances at ω=1 and series inductances g2,g4,g6,... represent reactances at ω=1. The terminating element S has the units of conductance if n is odd and resistance if n is even. The first element in the ladder network is the susceptance α as defined in eq [D1-2], i.e.

$$\alpha = g_1 = \omega' RC \qquad \text{[D1-5]}$$

By using Fano's notation [47], constants a and b, x and y, related to K and ε of eq [D1-3] can be defined

$$\frac{1+K^2}{\varepsilon^2} = \sinh^2 na \qquad \text{[D1-6]}$$

$$\frac{K^2}{\varepsilon} = \sinh^2 nb \qquad \text{[D1-7]}$$

$$x = \sinh a \qquad \text{[D1-8]}$$

$$y = \sinh b \qquad \text{[D1-9]}$$

The values of the g_r in Fig. D1-2 are now given by

$$g_1 = \frac{2 \sin \dfrac{\pi}{2n}}{x - y} = \alpha \qquad \text{[D1-10]}$$

$$g_r g_{r+1} = \frac{4 \sin \dfrac{2r-1}{2n} \pi \sin \dfrac{2r+1}{2n} \pi}{x^2 + y^2 + \sin^2 \dfrac{r\pi}{n} - 2xy \cos \dfrac{r\pi}{n}} \qquad \text{[D1-11]}$$

for r = 1, 2, ... (n-1)

$$\frac{g_n}{S} = \frac{2 \sin \dfrac{\pi}{2n}}{x + y} \qquad \text{[D1-12]}$$

$$S = \frac{g_n}{g_1} \frac{x+y}{x-y} \qquad \text{[D1-13]}$$

The maximum and minimum values of $|\rho|$ in the passband are given by

$$|\rho|_{max} = \frac{\cosh nb}{\cosh na} \qquad \textbf{[D1-14]}$$

$$|\rho|_{min} = \frac{\sinh nb}{\sinh na} \qquad \textbf{[D1-15]}$$

In addition to n, there are two variables x and y, or a and b, to be specified before the network is completely defined, but only one quantity, α, is given. There are therefore an infinite number of possible matching networks, but only one is optimum. This is obtained by minimizing $|\rho|_{max}$, subject to the constraint imposed by eq. [D1-10] , which is usually written in the form

$$A_1^{\infty} = \frac{2}{\alpha} = \frac{\sinh a - \sinh b}{\sin \frac{\pi}{2n}} \qquad \textbf{[D1-16]}$$

The minimization condition is obtained by a method of undetermined multipliers Putting

$$b = \lambda a \qquad \textbf{[D1-17]}$$

and differentiating eq [D1-14] with respect to a gives

$$\frac{d|\rho|_{max}}{da} = \frac{n(\lambda \cosh na \sinh n\lambda a - \cosh n\lambda a \sinh na)}{\cosh^2 na} \qquad \textbf{[D1-18]}$$

so that turning points of $|\rho|_{max}$ occur when

$$\lambda = \frac{\tanh na}{\tanh n\lambda a} = \frac{\tanh na}{\tanh nb} \qquad \textbf{[D1-19]}$$

Differentiation of eq [D1-16] with respect to a gives

$$\cosh a - \lambda \cosh \lambda a = 0 \qquad \textbf{[D1- 20]}$$

that is

$$\lambda = \frac{\cosh a}{\cosh b} \qquad \textbf{[D1-21]}$$

Elimination of λ from eq [D1-19] and [D1-20] gives the final condition for minimum $|\rho|_{min}$

$$\frac{\tanh na}{\cosh a} = \frac{\tanh nb}{\cosh b} \qquad \textbf{[D1-22]}$$

A simultaneous solution of eq [D1-16] and [D1-22] lead to the values of a and b, and therefore also x and y. This completes the design of the lowpass filter.

These equations is easy to implement in a Matlab algorithm and all that is needed as input is the number of matching elements and the complex load impedance.

The process of denormalisation of the lowpass network, to give actual circuit-element values at the particular cutoff frequency ω' and terminating resistance Rl required, is performed by multiplying all capacitances in the network by 1/Rl.ω' and all inductances by Rl/ω'.

Appendix E

E1 Calculation of microstrip lines

Microstrip line is one of the most popular types of planar transmission lines. The geometry of a microstrip line is shown in Fig. E1-1. A conductor of width W is printed on a thin, grounded dielectric substrate of thickness d and relative permittivity ε_r [38]

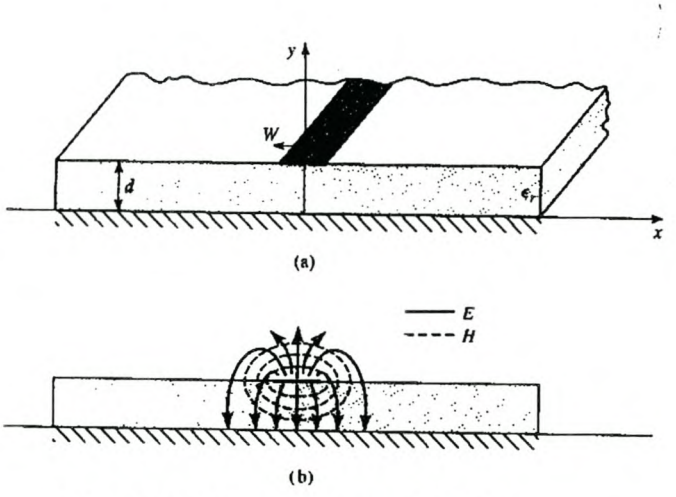

Figure E1-1 Microstrip transmission line

The phase velocity and propagation constant can be expressed as

$$v_p = \frac{c}{\sqrt{\varepsilon_e}} \qquad \textbf{[E1-1]}$$

$$\beta = k_0\sqrt{\varepsilon_e} \qquad \textbf{[E1-2]}$$

The effective dielectric constant of a microstrip line is given approximately by

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\frac{1}{\sqrt{1+12d/W}} \qquad \textbf{[E1-3]}$$

The effective dielectric constant can be interpreted as the dielectric constant of a homogeneous medium that replaces the air and dielectric regions of the microstrip.

Given the dimensions of the microstrip line, the characteristic impedance can be calculated as

$$Z_0 = \begin{cases} \dfrac{120\pi}{\sqrt{\varepsilon_e}\left[W/d + 1.393 + 0.667\ln\left(W/d + 1.444\right)\right]} & for\ W/d \geq 1 \\ \dfrac{60}{\sqrt{\varepsilon_e}}\ln\left(\dfrac{8d}{W} + \dfrac{W}{4d}\right) & for\ W/d \leq 1 \end{cases}$$

[E1-4]

For a given characteristic impedance Z_0 and dielectric constant ε_r, the W/d ratio can be found as

$$\frac{W}{d} = \begin{cases} \dfrac{8e^A}{e^{2A} - 2} & for\ W/d < 2 \\ \dfrac{2}{\pi}\left[B - 1 - \ln\left(2B - 1\right) + \dfrac{\varepsilon_r - 1}{2\varepsilon_r}\left\{\ln(B-1) + 0.39 - \dfrac{0.61}{\varepsilon_r}\right\}\right] & for\ W/d > 2 \end{cases}$$

[E1- 5]

where

$$A = \frac{Z_0}{60}\sqrt{\frac{\varepsilon_r + 1}{2}} + \frac{\varepsilon_r - 1}{\varepsilon_r + 1}\left(0.23 + \frac{0.11}{\varepsilon_r}\right)$$ **[E1-6]**

$$B = \frac{377\pi}{2Z_0\sqrt{\varepsilon_r}}$$ **[E1-7]**

The widths and lengths of microstrip lines can be calculated with these equations if the characteristic impedance, phase and frequency are known.

Appendix F

F1 Ritz-Galerkin equations

The differential equation for the detector circuit is:

$$a\left[\exp\left\{(x-y)-b\left(\dot{y}+y\right)-k\zeta\right\}-1\right]+g\left[\left(\dot{x}-\dot{y}\right)-b\left(\ddot{y}+\dot{y}\right)\right]=a\zeta+\dot{y}+y \qquad \textbf{[F1-1]}$$

where $x=\Lambda v_g$ is the forcing function and $y=\Lambda v_{out}$ is the output.

Other quantities are:

$a=\Lambda R_L I_S$
$b=(R_g+R_s)/R_L$
$g=C_j/C_L$
$k=\Lambda R_s I_s$.
$\zeta=I_0/I_s$ is a bias-current parameter.

The symbols "$\circ$" and "$\circ\circ$" indicate $d/d\tau$ and $d^2/d\tau^2$ respectively, where $\tau=t/(R_LC_L)$. For an input at frequency at ω,

$$x(\tau)=X\cos(v\tau) \qquad \textbf{[F1-2]}$$

where $v=\omega R_LC_L$ and $X=\Lambda V_g$.

To apply the RG method, the differential equation is represented in the form

$$\xi[d/d\tau, y, x]\equiv 0 \qquad \textbf{[F1-3]}$$

where ξ is a nonlinear operator.

The exact solution $y(\tau)$ is approximated by

$$\bar{y}(\tau)=\sum_{k=1}^{N} a_k\psi_k(\tau) \qquad \textbf{[F1-4]}$$

where the $\psi_k(\tau)$ are linearly independent functions and the a_k are adjustable coefficients.

In general

$$\xi\left[d/d\tau, \tilde{y}, x\right]=\varepsilon(\tau)\neq 0 \qquad \textbf{[F1-5]}$$

It can be shown that the magnitude of the residual $\varepsilon(\tau)$ is minimized by satisfying N Ritz conditions.

$$\int_{\tau_1}^{\tau_2} \xi\left[d/d\tau, \tilde{y}, x\right] \psi_k(\tau) d\tau = 0 \qquad k = 1, \ldots N \qquad \textbf{[F1-6]}$$

Resulting in N simultaneous algebraic equations in N unknowns.

In the present case $x(\tau)$ is periodic, so one could set

$$\tilde{y} = \sum_{1}^{3} a_k \psi_k(\tau) = Y_0 + Y_1 \cos(v\tau + \theta) \qquad \textbf{[F1-7]}$$

Where Y_0 is the DC component at the output and Y_1 and θ are the amplitude and phase of its ripple component. A simplification is to neglect the ripple. Then all that remains is a single unknown

$$\tilde{y} = Y_0 = \Lambda V_0 = cons\tan t \qquad \textbf{[F1-8]}$$

and only one Ritz condition is needed:

$$\int_{0}^{2\pi} \xi\left[d/d\tau, \tilde{y}, x\right] d(v\tau) = 0 \qquad \textbf{[F1-9]}$$

From [F1-1] and [F1-2]

$$\xi\left[d/d\tau, \tilde{y}, x\right] = a\left[\exp\{X\cos(v\tau) - [(1+b)Y_0 + k\zeta]\} - 1\right] - v_g \sin(v\tau) - a\zeta - Y_0$$

[F1-10]

Performing the integral

$$I_0(X) = \left(1 + \zeta + \frac{Y_0}{a}\right) \exp\{(1+b)Y_0 + k\zeta\} \qquad \textbf{[F1-11]}$$

where $I_0(X)$ is the zero-order modified Bessel function of the first kind and argument X. The disappearance of capacitance term g is a consequence of ignoring the ripple component of the output voltage.

As in linear theory the incident power is

$$P_{inc} = \frac{V_g^2}{8R_g} \qquad \textbf{[F1-12]}$$

So denormalizing [F1-11] and using [F1-12], the sought nonlinear algebraic relationship between P_{inc} and V_0 is

$$\Pi_0\left(\alpha\sqrt{8R_g P_{inc}}\right) = \left(1 + \frac{I_0}{I_s} + \frac{V_0}{R_L I_s}\right)\exp\left\{\left[1 + \frac{R_g + R_s}{R_L}\right]\alpha V_0 + \alpha R_s I_0\right\} \qquad \textbf{[F1-13]}$$

This expression includes the bias current I_0. The actual detector response can be found from () by calculating the input quantity P_{inc} as a function of the output quantity V_0, an operation requiring the inverse of the modified Bessel function. In the absence of input power, the static output $V_0(0)$ is found by solving for $P_{inc}=0$, in which case $I_0(0)=1.0$. Then the change in V_0 in response to a finite P_{inc} is given by

$$\Delta V_0 = V_0(P_{inc}) - V_0(0) \qquad \textbf{[F1-14]}$$

F2 Harmonic Balance – Simplification of the detector circuit – X-Band

In chapter 7 it was mentioned that the addition of the stray capacitance (C_g) in the Schottky diode model, makes the simplification of the circuit for Harmonic Balance applications more complex. It is necessary to include this parameter in the model at high frequency application, for example in the X-band.

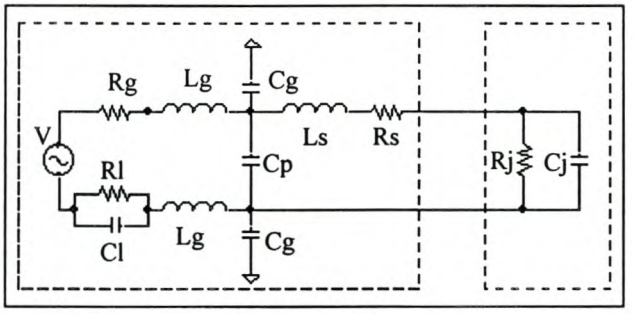

Figure F2-1 The detector circuit for a X-band application

Fig. F2-1 presents the detector circuit with all the parameters included. In order to apply the Harmonic Balance technique to the circuit, it needs to be simplified.

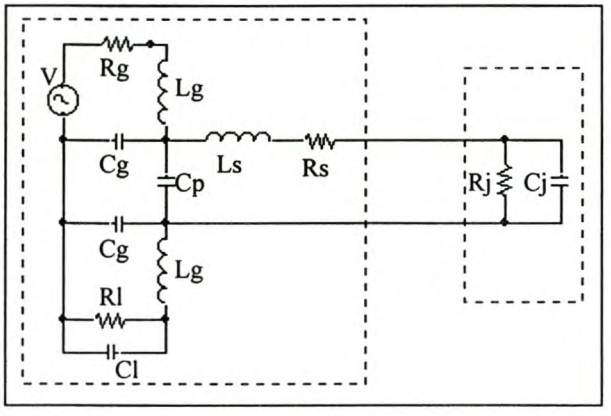

Figure F2-2 The reconstructed detector circuit for X-band applications

The circuit is reconstructed in Fig. F2-2, to make it easier to visualize the Thevenin equivalent circuit.

The circuit is simplified further to the one illustrated in Fig. F2-3

$$A = \left[Z_{Cl} \parallel Rl + Z_{Lg} \right] \parallel Z_{Cg} \qquad \textbf{[F2-1]}$$

$$B = Rg + Z_{Lg} \qquad \text{[F2-2]}$$

$$C = Z_{Ls} + Rs \qquad \text{[F2-3]}$$

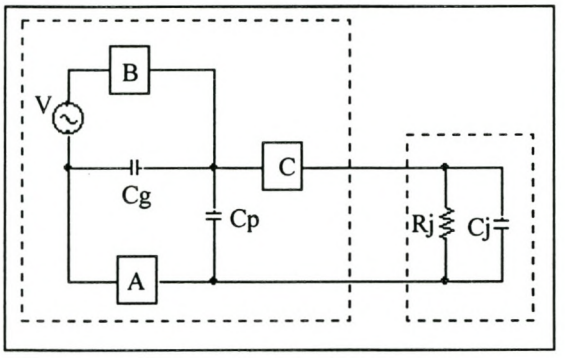

Figure F2-3 The simplified detector circuit for X-band applications

It is now much easier to calculate the Thevenin equivalent circuit, which is presented in Fig. F2-4

$$R_{TH} = C + \lfloor A + B \parallel Z_{Cg} \rfloor \parallel Z_{Cp} \qquad \text{[F2-4]}$$

$$V_{TH} = \frac{Z_{Cp} Z_{Cg}}{(Z_{Cg} + B)(Z_{Cp} + A) + BZ_{Cg}} \qquad \text{[F2-5]}$$

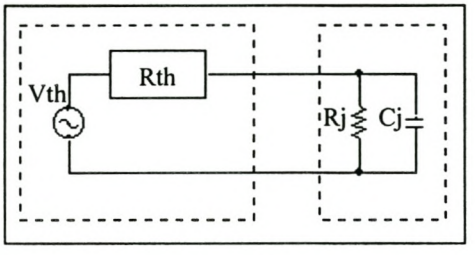

Figure F2-4 The Thevenin equivalent of the detector circuit for X-band applications

Appendix G

G1 Detector Design with Diode Pairs

In section 6-4 it was mentioned that a DC offset is present at the output of a biased detector. It is said that it is necessary to eliminate this DC offset to improve the sensitivity of the detector at lower power levels. Two methods were mentioned to implement a low noise operational amplifier to zero the output. One of the methods was to use a diode pair in the design. One diode is biased, while the input RF signal is applied to the second diode with exactly the same bias current. This method results in the detecting the RF signal. The biggest advantage of this method is the improvement in temperature effects. The effect temperature has on results is largely eliminated, because of exactly the same behavior of both diodes towards temperature.

This temperature compensated detector design is described in [35]

As previously discussed, one of the solutions to the temperature dependence problem is the addition of bias current. It reduces the junction resistance and therefore also facilitates the diode matching.

The reduction of junction resistance dependence with temperature is easily demonstrated by the inclusion of the I_{bias} term in eq [3-13]

$$R_j = \frac{nkT}{e(I_s + I_{det} + I_{bias})} \qquad \text{[G1-1]}$$

In fact as ($I_{bias} >> I_s$) R_j may be expressed as

$$R_j = \frac{nkT}{e(I_{det} + I_{bias})} \qquad \text{[G1-2]}$$

The inclusion of bias reduces the direct dependence of R_j with temperature as

$$\frac{dR_j}{dT} = \frac{nk}{e(I_{det} + I_{bias})} \qquad \text{[G1-3]}$$

However the addition of I_{bias} introduces an offset term in the current flowing through the diode (I_{diode}), which may be expressed as

$$\begin{aligned} I_{diode} &= I_{biat}(T) + I_{det} + I_s \\ &\cong I_{bias}(T) + I_{det} \\ &= I_{bias}(T) + K(T)P_{in} \end{aligned} \qquad \text{[G1-4]}$$

where

$I_{bias}(T)$ = biasing current which depends on temperature
$K(T)$ = detection sensitivity which depends on temperature
P_{in} = RF input power level

For temperature compensation it is necessary to eliminate $I_{bias}(T)$. This can be done by using the two diode configuration.

The current through the second diode is

$$I_{diode2} = I_{bias}(T) \qquad \text{[G1-5]}$$

Temperature compensation of the offset term is obtained if the bias current through each diode is made equal. Both diodes must be biased making use of the same biasing network previously described.

As previously stated, the currentthrough each diode is given by

$$\begin{aligned} I_{diode1} &= I_{bias1}(T) + K(T)P_{in} \\ I_{diode2} &= I_{bias2}(T) \end{aligned} \qquad \text{[G1-6]}$$

The key idea is to bring together the responses of the detected voltage for different temperatures at low RF input signal power levels, where errors mainly occur. This can be done by slightly modifying the biasing parameters for the offset cancellation diode.

For a given low input power level (P_{inlow}), and for the range of working temperatures [T_{max}, T_{min}] the detected current at the limits of the temperature range is given in each case by

$$\begin{aligned} I_{det}(T_{min}) &= I_{bias1}(T_{min}) + K(T_{min})P_{inlow} - I_{bias2}(T_{min}) \\ I_{det}(T_{max}) &= I_{bias1}(T_{max}) + K(T_{max})P_{inlow} - I_{bias2}(T_{max}) \end{aligned} \qquad \text{[G1-7]}$$

It would be desirable to have

$$I_{det}(T_{min}) = I_{det}(T_{max}) \qquad \text{[G1-8]}$$

so that no errors appear at P_{inlow}. The condition of eq G1-8 may be accomplished by modifying I_{bias} of the diodes used in the design.

When different biasing is used for each diode the output current is given by

$$\begin{aligned} I_{det}(T) &= K(T)P_{in} + I_{bias1}(T) - I_{bias2}(T) \\ &= K(T)P_{in} + \Delta I_{bias}(T) \end{aligned} \qquad \text{[G1- 9]}$$

For low RF input signal power levels $\Delta I_{bias}(T)$ compensates the $K(T)$ variations due to temperature drifts. For larger power levels, the term $K(T)P_{in}$ is much greater than $\Delta I_{bias}(T)$ and therefore compensation cannot occur.