MODEL PREDICTIVE CONTROL OF AC-TO-AC CONVERTER VOLTAGE REGULATOR

Youngie Klyv Chewele

Thesis presented in partial fulfilment of the requirements for the degree
Master of Engineering (Research) in the Faculty of Engineering
at Stellenbosch University

Supervisor: Prof H. du T. Mouton

Co-Supervisor: Mr Males Tomlinson

Department of Electrical & Electronic Engineering

April 2014

Declaration

By submitting this thesis electronically I declare that the entirety of the work contained therein is my own, original work, that I am the sole author thereof (save to the extent explicitly otherwise stated), that reproduction and publication thereof by Stellenbosch University will not infringe any third party rights and that I have not previously in its entirety or in part submitted it for obtaining any qualification.

March 2014

Acknowledgements

I would like to thank first and foremost my Lord and Saviour Jesus Christ for the opportunity, the will and the ability he has given me to study and complete this thesis.

I thank my supervisor Prof. Mouton for his patience, support and guidance during the research when I was going through a difficult time in my life and during the writing of this thesis.

I thank Males Tomlinson for his good guidance in the research.

I would like to acknowledge the Government of Malawi and ESCOM for their support

Lastly I thank my wife Leah and my children for allowing me the time away from them to enable me study.

Abstract

The development of fast and efficient processors, programmable devices and high power semiconductors has led to the increased use of semiconductors directly in the power supply path in order to achieve strict power quality standards.

New and advanced algorithms are used in the process and calculated on-line to bring about the required fast response to voltage variations. Losses in high voltage semiconductors increase with increased operating frequencies.

A balance between semiconductor power losses and power quality is achieved through control of power semiconductor switching frequencies.

A predictive control algorithm to achieve high power quality and limit the power losses in the high power semiconductor switches through switching frequency control is discussed for a tap switched voltage regulator.

The quality of power, voltage regulator topology and the control algorithm are discussed. Simulation results of output voltage and current are shown when the control algorithm is used to control the regulator. These results are verified by practical measurements on a synchronous buck converter.

Key words

Medium voltage converter control

Finite set model predictive control

Voltage regulators

Discretization

VHDL

Opsomming

Die ontwikkeling van vinnige en doeltreffende verwerkers, programmeerbare toestelle en hoëdrywings halfgeleiers het gelei tot 'n groter gebruik van halfgeleiers direk in die kragtoevoer pad om streng elektriese toevoer kwaliteit standaarde te bereik.

Nuwe en gevorderde algoritmes word gebruik in die proses en word aan-lyn bereken om die nodige vinnige reaksie tot spanningswisselinge te gee. Verliese in hoë-spannings halfgeleiers verhoog met hoër skakel frekwensies. 'n Balans tussen die halfgeleier drywingsverliese en spanningskwalteit is behaal deur die skakel frekwensie in ag te neem in die beheer.

'n Voorspellinde-beheer algoritme om ‘n hoë toevoerkwaliteit te bereik en die drywingsverliese in die hoëdrywingshalfgeleier te beperk, deur skakel frekwensie te beheer, is bespreek vir 'n tap-geskakelde spanning reguleerder.

Die toevoerkwaliteit, spanningsreguleerder topologie en die beheer algoritme word bespreek. Simulasie resultate van die uittree-spanning en stroom word getoon wanneer die beheer algoritme gebruik word om die omsetter te beheer. Hierdie resultate is deur praktiese metings op 'n sinkrone afkapper.

Table of Contents

List of Figures

List of Tables

List of acronyms and abbreviations

Abbreviations

AC	Alternating current
DC	Direct current
FS-MPC	Finite-set model predictive control
MPC	Model predictive control
FPGA	Field-programmable gate array
QOP	Quality of power
NERSA	National Energy Regulator of South Africa
THD	Total harmonic distortion
SST	Solid state transformer
EMI	Electromagnetic interference
MVEVR	Medium voltage electronic voltage regulator
LV	Low voltage
LC	inductor and capacitor
HV	High voltage
NLTC	No-load tap changer
DETC	De-energised tap changer
OLTC	On-load tap changer
ABB	Asea Brown Boveri
IGBT	Insulated gate bipolar transistor
HF	High frequency
AFE	Active front end
PWM	Pulse width modulation
GPC	Generalised predictive control
CARIMA	Controlled auto-regressive integrated moving average
DMC	Dynamic matrix control
QDMC	Quadratic dynamic predictive control

RHC	Receding horizon control
MIMO	Multiple input multiple output
PID	Proportional-integral-derivative
MOSFET	Metal-oxide-semiconductor field-effect transistor
ADC	Analogue to digital converter
I/O	Input/output
LCD	Liquid crystal display
Ts	Sampling period
OS	Oversampling
S(k)	Switch state now
S(k+1)	Switch state at next sampling time
FFT	Fast Fourier transform
VHDL	VHSIC hardware description language

Sets

$\mathbb{R}$	Set of (non-negative) real numbers
$\mathbb{N}$.	Set of non-negative integers
$\mathbb{R}^{nm}$	Set of real matrix with *n* rows and *m* columns

Algebraic Operators and Matrices

x_i	*i*-th element of vector x
$x \in \mathbb{R}$	x is an element of/in real number
$\|\|x\|\|$	Any vector norm of x
$\boldsymbol{x}$	**in bold** is a vector of x

Set Operator

$P \sqsubseteq Q$	The set *P* is a subset of *Q*

$P \sqsubset Q$	The set P is a strict subset of Q

CHAPTER 1
INTRODUCTION

1.1 MOTIVATION

One of the greatest things ever to have happened to mankind in the 20th century was the invention of a transistor by John Bardeen, Walter Brattain and William Shockley in 1947 at Bell, USA and the successful production of the first transistor in 1954 [1] . The invention of the transistor led to the invention of integrated circuits in 1957. The transistor is the heart of electronics and has now become central to our lives. Uses of transistors range from power electronics, computers and cell phones to specialised processors for controllers in cars and other complex systems.

As the number of transistors on integrated circuits doubles every two years following Moore's law, computing power is increasing and online control of complex and faster processes are becoming more common. This is due to shrinking transistor size, higher operating speeds and introduction of more power efficient semiconductors. As the processor die size is decreasing, the processing speed is increasing and production costs are decreasing. Low power consumption in the devices has been largely achieved by decreasing the operating voltage, parallel processing and introduction of programmable devices such as FPGAs, improvement and introduction of new semiconductor technologies and manufacturing methods.

On the other side of semiconductor technology, is the use of semiconductors in high power and high voltage electronics. The biggest challenge in power electronics has been to develop high power devices which operate at higher voltage and frequencies with minimum power loss. As the operating frequency or operating voltage increase so do the power losses. Transistors are rapidly replacing mechanical switches in power electronics due to their faster switching speeds and the ease of control by low power processors. To control these power semiconductors in power supply paths there is a need to balance between switching frequency and power losses without degrading the quality of the power supplied. The controller should be able to compute online the minimum cost with real time measurements using complex control algorithms and be able to apply the control law immediately to achieve the desired control objective.

In this research, a finite-set model predictive control (FS-MPC) algorithm that is presented which can be computed online by using an FPGA, to directly regulate the output voltage of

an AC-AC medium voltage regulator with input transformer connected in an autotransformer configuration.

1.2 BACKGROUND

In an ideal electrical power distribution system, the supply would have a constant magnitude, frequency and sinusoidal waveform [2]. The non-zero impedance of the supply system, the variation in loads, transients and outages cause the system to depart from the ideal behaviour. The non-zero impedance of the supply system is compounded by the proliferation of small distributed generation from renewable energy sources. Most of these renewable energy sources (e.g. solar and wind) are not as consistent, predictable and controllable as conventional sources of energy such as hydro, coal and nuclear. The compromised system will then operate outside the required power quality standards. The quality of supply will have an effect on the lifetime of loads connected to it, and poor quality supply can result in other economic losses such as lost production time in factories. With more sensitive electronic equipment being used in industrial processes [3], homes and offices it is imperative to maintain good power quality. With more and more sensitive equipment being connected to the power grid, the speed at which the power quality compensators operate is very important to the load.

According to NERSA, ESKOM is mandated to adhere to quality of power (PQ) standards, contained the NRS 048-2 document that is endorsed by the South African Bureau of Standards (SABS). The voltage magnitude and total harmonic distortion (THD) of the supply at the customer's point of entry has to meet certain compatibility levels as shown in Table 1-1 and Table 1-2 [4] below. The NRS standard specifies that 'The THD of the supply voltages on all LV and MV networks, including all harmonics up to the order of 40, shall not exceed 8%'

Table 1.1 Deviations from standard declared voltages

1	2
Voltage level V	**Compatibility level** %
< 500	± 10
≥ 500	± 5

Table 1.2 Compatibility levels for harmonic voltages for LV and MV networks

(Expressed as a percentage of the reference voltages)

1	2	3	4	5	6
Odd harmonics				**Even harmonics**	
Not multiples of 3		**Multiples of 3[a]**			
Harmonic order *h*	**Magnitude** %	**Harmonic order** *h*	**Magnitude** %	**Harmonic order** *h*	**Magnitude** %
5	6	3	5	2	2
7	5	9	1,5	4	1
11	3,5	15	0,5	6	0,5
13	3	21	0,3	8	0,5
$17 \leq h \leq 49$	$\{2{,}27 \times (17/h)\} - 0{,}27$	$21 \leq h \leq 45$	0,2	$10 \leq h \leq 50$	$\{0{,}25 \times (10/h)\} + 0{,}25$

[a] The levels given for odd harmonics that are multiples of 3 apply to zero sequence harmonics. Also on a three-phase network without a neutral conductor or without load connected between phase and earth, the actual values of the third and ninth harmonics might be much lower than the compatibility levels, depending on the voltage unbalance of the system.

Electrical power utilities can control the voltage quality but have very little control over load current. The power provider must find ways to provide good control of supply voltage under different types of load condition. The power utility must ensure voltage fidelity under different load conditions. There are several ways of improving the power quality. Some of the methods used in industry are as shown in Figure 1.1.

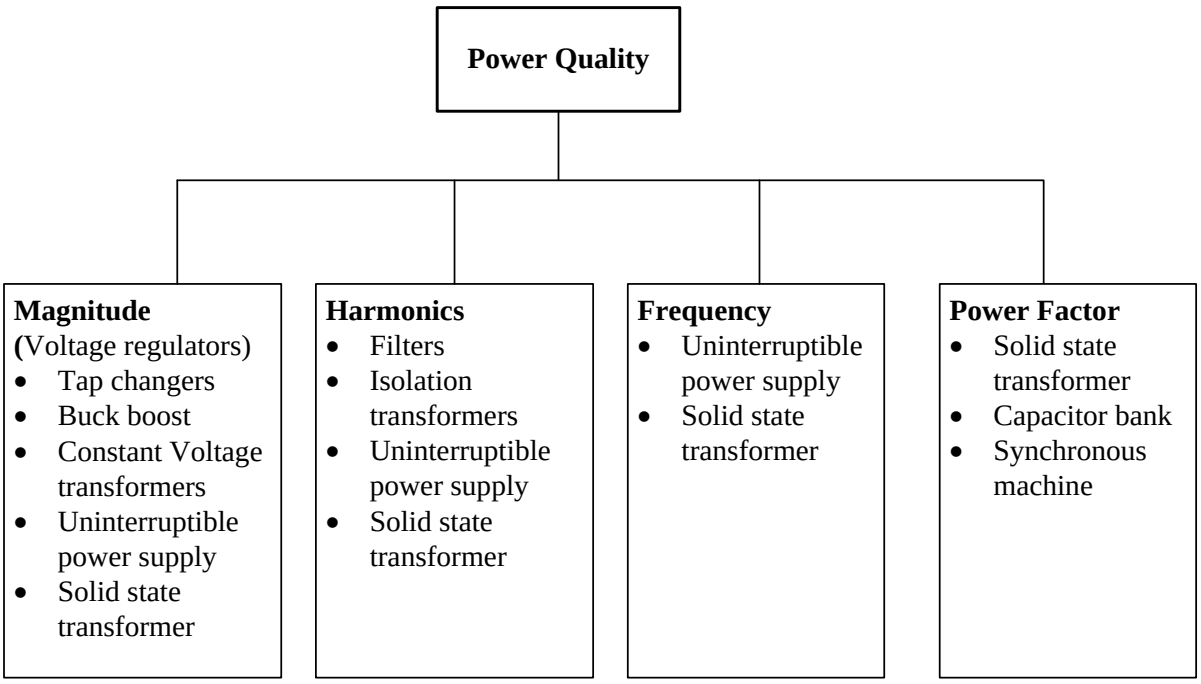


Figure 1.1 Improving power quality

Tap changers: Tap changers are variable contact mechanisms that can connect to different connection points on a transformer winding allowing a change in transformer ratio between a primary and secondary winding. These are designed to adjust the voltage and sometimes shift the phase angle [5] [6] [7]of the output by transferring taps on a power transformer. Tap changers are usually installed on the high voltage side of the transformer winding to minimise the current handling requirements of the contacts. The system is efficient but is limited to fixed tap positions only. Mechanical tap changers are slow and require frequent maintenance.

Buck boost converters: These use similar technologies to the tap changers except that the transformer is not isolated. These systems have no wave shaping and suffer from noise generated when changing taps.

Uninterruptible power supply (UPS): These provide protection in case of complete power interruption (blackout). They provide varying degrees of protection from sags, noise and brownouts depending on the topology used.

Solid state transformer: The solid state transformer (SST): consists of high power electronics with the purpose of replacing existing iron core transformers. SSTs can correct input power factor, regulate voltage, filter harmonics, provide output short circuit protection and compensate for voltage dips and swells, capable of supplying DC voltages [8].

Solid state voltage regulators: Solid state voltage regulators have high power electronics which regulate the voltage by switching at high frequency without affecting the system

operating frequency. These regulators have low pass filters at the output to filter out the high frequency harmonics caused by the switching of the devices. Swells, can be compensated for, but there is no compensation for prolonged dips.

Transient suppressors: These are power conditioners which operate by clamping transient impulses limiting them to a level that is safe for equipment.

Filters: They provide protection against low voltage high frequency noise and harmonics in the power system. They filter out electromagnetic interference (EMI) and radio frequencies.

Some of the power quality improvement mechanisms are undertaken by the power producer, like ESKOM while others are undertaken by the customer.

1.3 STUDY OBJECTIVES

The aim of this study is to design an FS-MPC based controller and implement it in an FPGA for the MVEVR while ensuring that the regulated voltage meets the NRS 048-2: 2008 standards. To achieve this goal the following things need to be done

- Review model predictive control
- Review the MVEVR topology and its behaviour
- Model the MVEVR
- Design a predictive controller
- Design a suitable mechanism for switching frequency control for the controller
- Simulate the MVEVR control using the controller designed
- Apply the controller on the MVEVR or an equivalent system

1.4 THESIS OVERVIEW

Chapter 2 of the document starts with a literature review of the voltage regulation techniques. The techniques discussed are the mechanical tap changers, the hybrid tap changers, and solid state tap changers: a discussion of solid state voltage regulator topologies then follows. After the voltage regulation techniques, model predictive control is discussed, starting with its history. Branches of model predictive control, its theory and then the finite set model predictive control and conditions for MPC stability are discussed. The theory of MPC includes a discussion of the basis of MPC as well as the prediction and control horizons.

Chapter 3 gives an overview of the hardware design and layout. The MVEVR circuit is shown and its operation and protection mechanisms are presented. The synchronous buck converter is also discussed and its operation is presented. The chapter ends with the discussion of the control board, the various software components and how they work.

Deriving the converter models is done in Chapter 4 by considering the equivalent circuits in the on and off states. The same technique is used to derive the models for the synchronous buck converter in the on and off switch positions.

Chapter 5 shows how the controller is designed. The control objectives are laid out and the required controller schematic is presented. Results of the simulation of the MVEVR and the buck converter with the controller are presented. Problems encountered with the MVEVR are presented and suggested solutions are presented and tested by the simulations.

Chapter 6 shows how the controller was integrated into the existing Altera Cyclone Iii FPGA board software in VHDL.

Chapter 7 presents the results obtained from the implementation of the controller on the synchronous buck converter under different conditions.

Conclusions and proposed future work are presented in the last chapter of the document, Chapter 8.

CHAPTER 2
LITERATURE STUDY

2.1 INTRODUCTION

Various ways of improving voltage quality were introduced in chapter1. This chapter continues by focussing on how the power quality is improved by distribution network voltage regulation then the history and theory of model predictive control will be discussed. Some of the systems explored in this chapter affect not only the voltage magnitude, but also the other aspects of power quality such as frequency, harmonics, and power factor as listed in Figure 1.1.

2.2 VOLTAGE REGULATION TECHNIQUES

2.2.1 Tap changers

Tap changers on transformers are the most common method of voltage regulation by power utilities in power transmission and distribution network transformers. A tap changer allows a variable number of turns to be selected in discrete steps, thereby producing a transformer with variable turns ratio. Tap changers are normally placed on the high voltage side of transformers where the current is low. This minimizes the current handling requirements for the contacts. Figure 2.1 shows a basic tap changer.

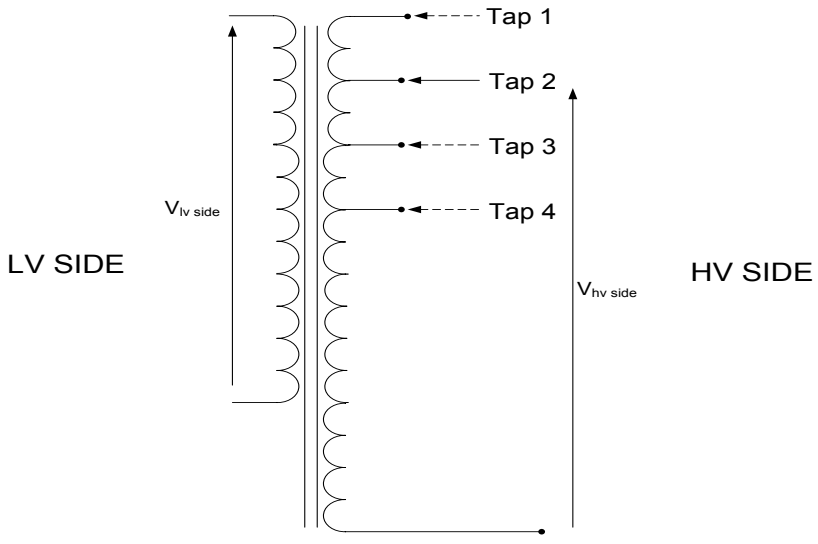


Figure 2.1 Simple tap changer overview

Tap changers are divided into three categories [9]. The three categories can be summarised into two major ones namely: off-load tap changers and on-load tap changers [10].

Off-load tap changers

Off-load tap changers are also called No-load tap changers (NLTC), off-circuit tap changers or De-energised tap changers (DETC). This type of tap changer requires interrupting the power to the transformer or equipment before changing the tap positions. NLTCs are common in transformers in power distribution networks where the loss of supply can be tolerated and where it is uneconomical to install on-load tap changers (OLTC). The tap position is set only once to accommodate small voltage variations and changed only when a long term change in system voltage profile is expected. The life of the Off load tap changer's contacts is affected by time and temperature. Lack of movement of the tap changer means there is no contact surface cleaning. Minor contact oxidation will result in large resistance which can cause thermal runaway [11].

On-load tap changers (OLTC)

Taps are changed while the equipment is live and supplying power. On-load tap changers are common in large transformers where interruption of supply is not tolerated. This is accomplished by means of mechanical tap changers or solid state tap changers

Mechanical tap changers: mechanical tap changers have contacts which physically move to connect to the new tap before disconnecting from the old tap while avoiding high circulation currents. A diverter switch is temporarily put in series with turns to limit the current as shown in Figure 2.2 [12] below. Current limiting is achieved by the use of some form of impedance (resistive impedance is used in high speed switching or reactive impedance is used in slow speed switching). Resistive impedance used in high speed switching is now the most popular method used worldwide [13]. The most common type of tap connections in a winding are at the middle or near the neutral star point of a transformer. The advantage of these arrangements is reduced stress between the tap changer and the earth, and that the contacts are subjected to less physical and electrical stress during faults.

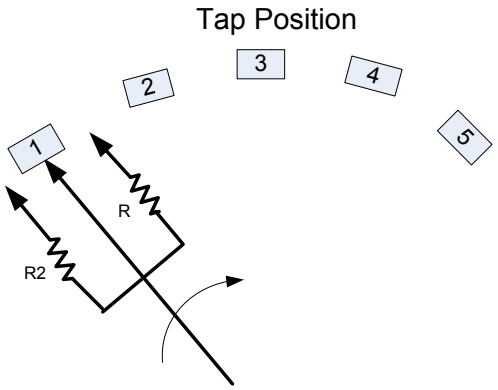


Figure 2.2 a. Position 1.

On tap 1- The main contact is carrying the load current

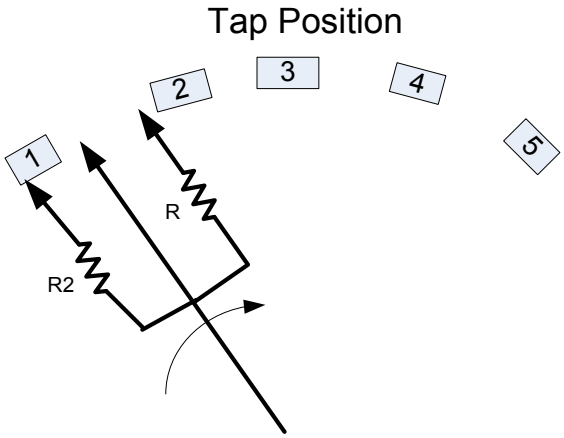


Figure 2.2 b. Position 2.

Main contact is disconnected from tap1 and auxiliary contact with R2 is connected. Load current passes through R2.

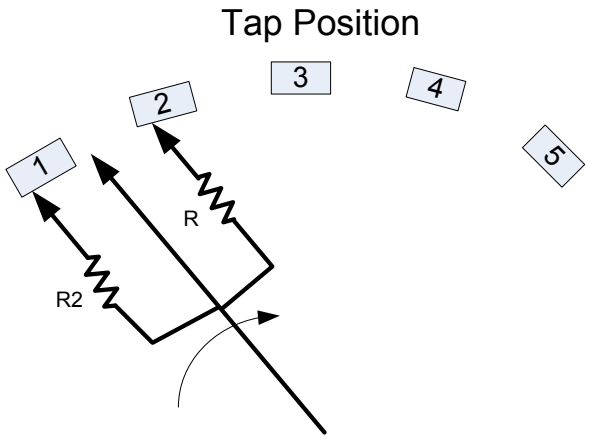


Figure 2.2 c Position 3. Contact on R has been made on the fixed contact 2. The load current is divided between transit contacts (R2 and R) on tap1 and tap2. The circulating current is limited by R and R2

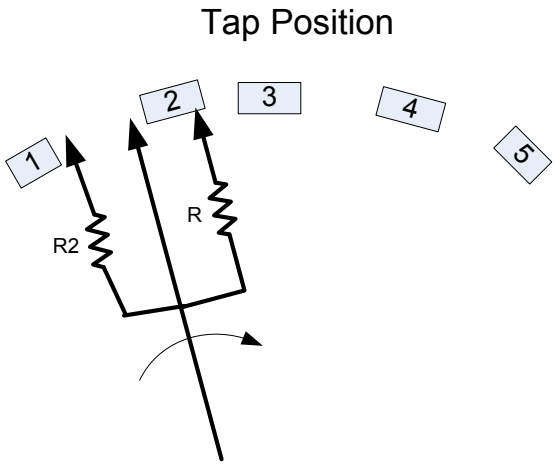


Figure 2.2 d Position 4. Only Resistor R passes load current, main contact and R2 disconnected

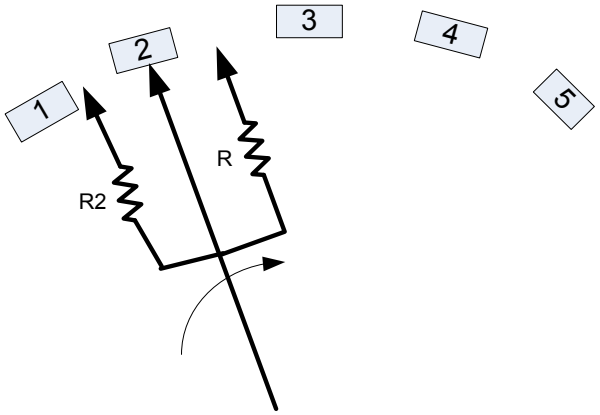


Figure 2.2 Tap Changing process from Tap 1 to Tap 2

Figure 2.2 e. Position 5. Main contact on is now connected to tap 2. Load current passes through the main contact.

The tap-changers have special arc suppression vents to quench the arc in the diverter switches while general insulation of the tap changer is achieved by immersing the whole tap-changer assembly in insulating oil. Figure 2.3 shows a typical commercial mechanical tap changer.

Old tap changers were slow and were of the inductor tap changer variety which was invented in 1926 [14]. The advantage of the inductor tap changer is its ability to pass load current continuously. Resistor based tap changers started to appear with the development of faster tap changers. Resistors can only pass load current for a very short period and require very fast operation of the tap changer. OLTCs are usually spring loaded to achieve fast transition times.

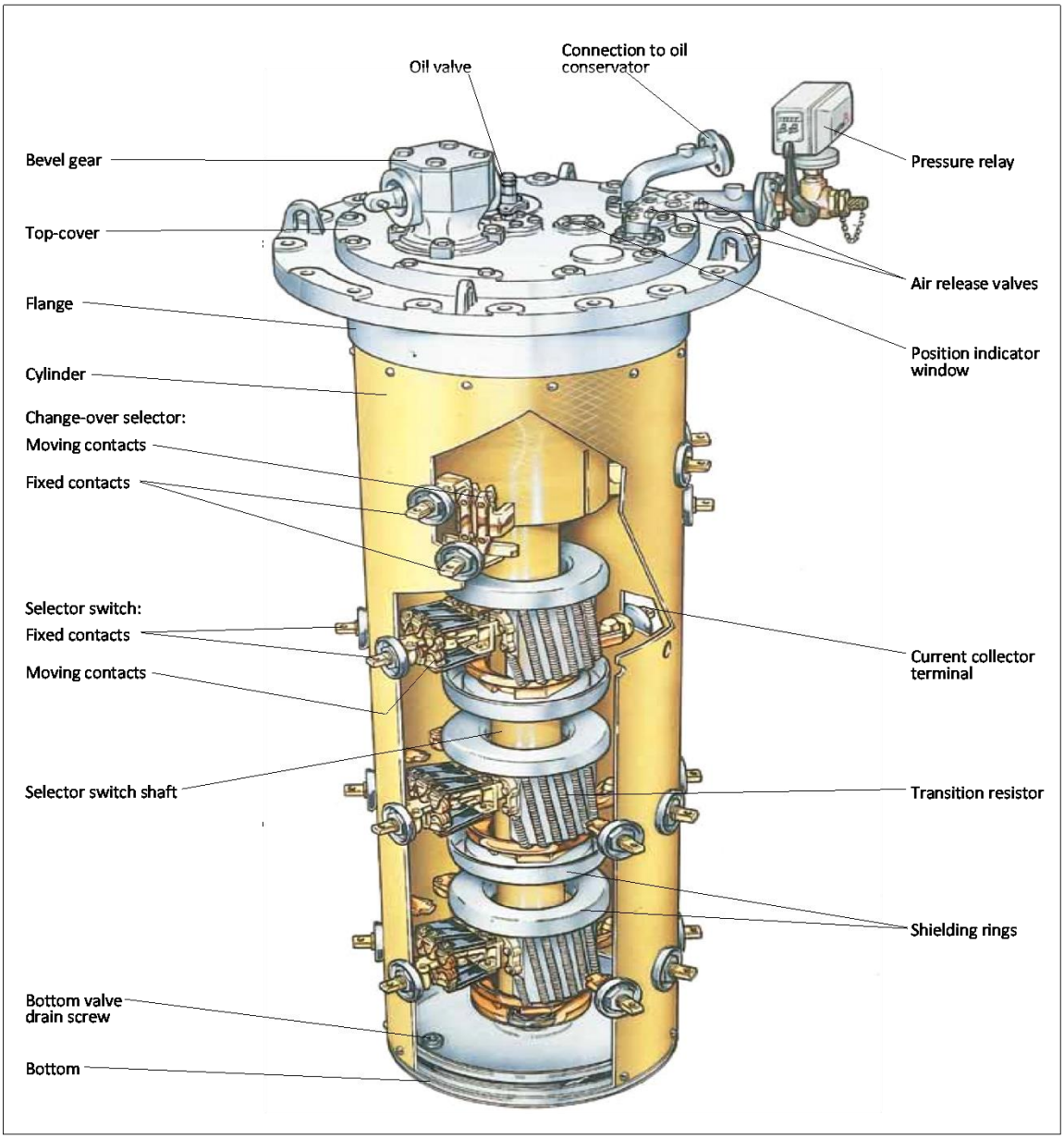


Figure 2.3 ABB OLTC changer type UBB [12]

Limitations of mechanical OLTC

- Tap-changer failure is a major factor in the failure of power transformers. It has been estimated that more than 20% of transformer failures are due to on-load tap changers

- Arc produced during make or break in the switch contacts causes degradation in the insulating oils. Some manufacturers use other media such as a vacuum or SF6 gas to minimize the arc.
- The cost of maintaining and servicing the tap-changer is high due to the necessity for replacement of insulating oil, replacement and maintenance of contacts and replacement and maintenance of all the moving parts.
- The response of the mechanical OLTC to voltage fluctuations is slow.

These limitations can be overcome by the following new circuits and schemes for on-load tap changers [15]:

1. Hybrid or electronically assisted on-load tap changers. In such type of tap changers, electronic solid state devices are used alongside mechanical switches to reduce the arc caused by tap changing.

2. Solid state or electronic on-load tap changers. In an electronic tap changer, there are no moving parts and the switches comprise only solid-state power devices.

Hybrid On-load tap-changers

In mechanical tap changers, the arc is caused by the contacts in the diverter contacts when breaking load current. Most simple mechanical OLTCs use insulation oil in the tap-changer tank as a medium for quenching the arc. The disadvantage of this method is that oil has to be replaced often. Some OLTCs improve the arc quenching by using a vacuum (e.g. tap changer type VUC from ABB [16]) or SF_6 gas based interrupters to increase the life of the contacts.

Hybrid on-load tap changers are based on electro-mechanical tap changers with solid state electronics which assist in the reduction of arc generated during the process of tap changing. Thyristors have been connected back to back to assist in the tap change process in [17].

Hybrid tap changers have the following attributes [18]:

- Less maintenance is required than for purely mechanical tap changers
- More expensive compared with electromechanical tap changer
- Poor line transient suppression

Solid state on-load tap-changers

Solid state tap changers have the same discrete tap steps that mechanical tap changers have. The difference lies in the tap changing mechanism. While mechanical tap changers rely on moving contacts, solid state tap changers rely on solid state electronics to switch

between taps. Electronic tap changers have the following advantages over the electro-mechanical tap changers [19]:

- Low maintenance cost. There are no moving parts and therefore, no arc to quench. There is almost zero maintenance cost.
- High switching speed: Switching speed can be achieved within a half cycle because of the fast switching speed of the solid state devices. Response to voltage changes is therefore fast.
- Flexible tapping: It is possible to jump taps since there are no moving parts. There are no circulating currents to worry about.
- Ease of controllability: No complex systems are required to control the tap positions as the need for motors and gears is eliminated thereby increasing the control and the speed of response to voltage changes. This means that the regulator can be used to compensate for voltage flicker, voltage sag and swell.

The disadvantages of electronic tap changers are that:

- Solid-state power switches have a larger voltage drop across them when switched on compared with mechanical switches which have very little voltage drop. This leads to more losses in the switch.
- The cost of the high power solid- state devices is high, making the cost of the tap-changer higher when compared with that of the mechanical tap changer.
- They have a lower surge and fault handling capacity compared with mechanical tap changers

Thyristor based tap changer: Thyristor based tap changers have Thyristors connected back to back at every tap as shown in Figure 2.4 [20] below.

Two thyristors are connected back to back at each tap to allow for current flow in either of the two directions. Only the thyristor pair in one tap position is ever switched on at any time to prevent short circuiting the taps. Switching between the taps can be done only when both the voltage and the current have the same polarity.

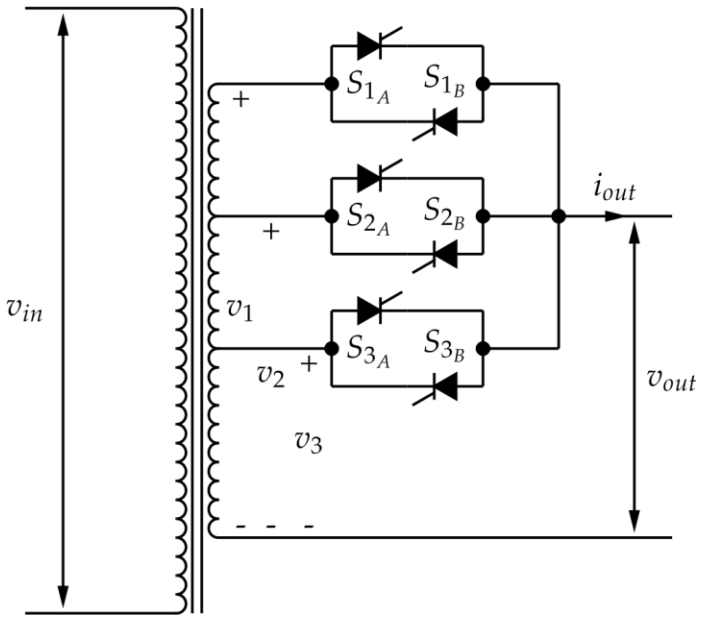


Figure 2.4 Thyristor based solid-state tap changer [20]

Consider current to be flowing through thyristor pair S_2. The output voltage v_{out} can be increased by switching on pair S_1 and then switching off pair S_2. Decreasing the voltage is achieved by switching on pair S_3 and then switching off pair S_2. The windings may be shorted for one cycle. The disadvantages of this type of tap changer are [20] :

- The secondary winding leakage impedance delays commutation from one thyristor pair to the next thyristor pair during tap change operation as the commutation period is a function of the leakage impedance, tap winding voltage and load current. This is illustrated in [20].
- As the power factor approaches unity, the available safe switching period tends to zero.
- The output wave shape is distorted and has a many harmonics. This can, however, be improved by inserting an LC filter at the output.
- Shorting of windings may damage the devices and the windings.

IGBT based tap changer

In thyristor based controllers as shown above, the harmonics have high magnitudes and are close to the fundamental frequency of the power supply. It is not recommended to use passive filters. The size and weight of the passive filters would be very high [21]. AC choppers based on IGBTs are superior to the thyristor based choppers. Some of the advantages are:

- The output voltage and current have a sinusoidal waveform
- Tap change can be performed at any time in the cycle.
- Their switching frequency is many times the fundamental system frequency and therefore, they require smaller filters
- They are more efficient
- The filters provide RFI filter.
- They have a better power factor.

Several IGBT based topologies have been proposed and implemented by different researchers. This paper will review just a few of these topologies. These chopper topologies IGBTs have two commutator cells each with current able to flow in both directions and one way voltage.

IGBT topology 1

An IGBT based tap changer shown in Figure 2.5 is connected on the primary side of a transformer on a 10 kV power grid in such a way that the IGBTs do not block all the 10kV. The IGBTs are connected to taps on the primary side of the transformer. The tap voltages are chosen to be less than the rating of the IGBT's blocking voltage. Crowbar thyristors S1 and S2 are connected in such a way that in an event of high voltage the IGBTs will be bypassed.

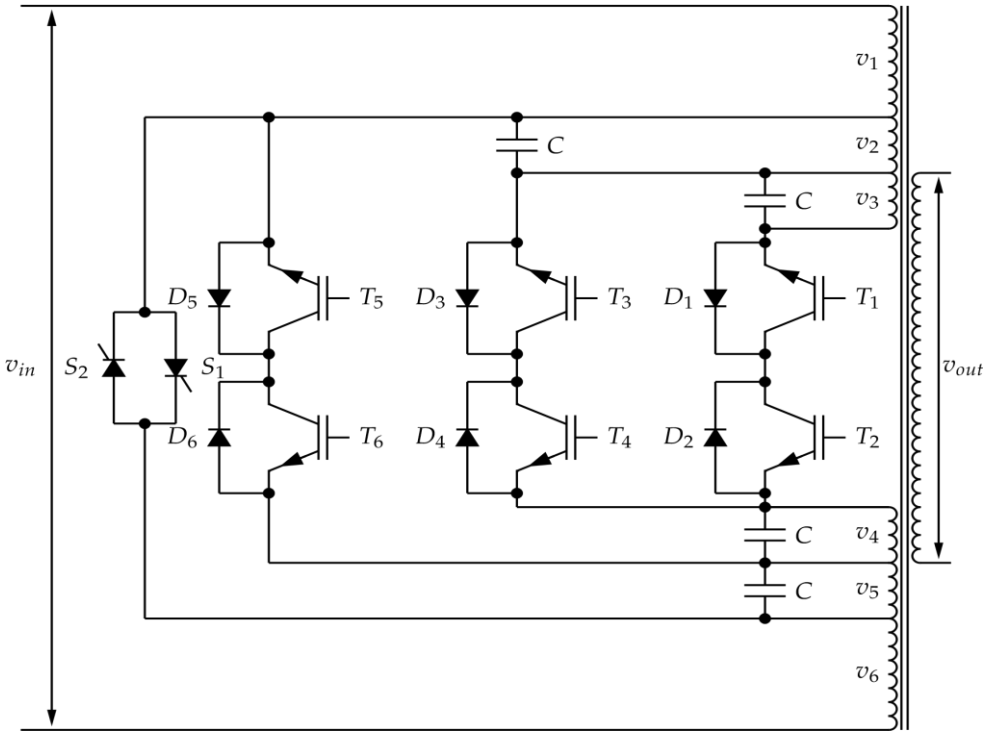


Figure 2.5 IGBT based tap changer [22]

The output voltage is controlled continuously by the use of appropriate control methods such as PWM. The fast switching of the IGBTs can bring electromagnetic interference (EMI) into the system and the high frequencies generated by the switching action may cause damage to transformer windings. As the taps increase, so must the switching elements. Each tap position requires two switching elements and hence the cost goes up.

IGBT Topology 2

The chopper shown in Figure 2.6 is the differential topology. This topology is made up of two half bridge converters placed back to back with an output LC filter. This topology does not provide neutral continuity. Making simple changes will enable neutral return as in Figure 2.8. There are several variations to this differential topology. In [23] a variation of the differential topology with an injection transformer is presented.

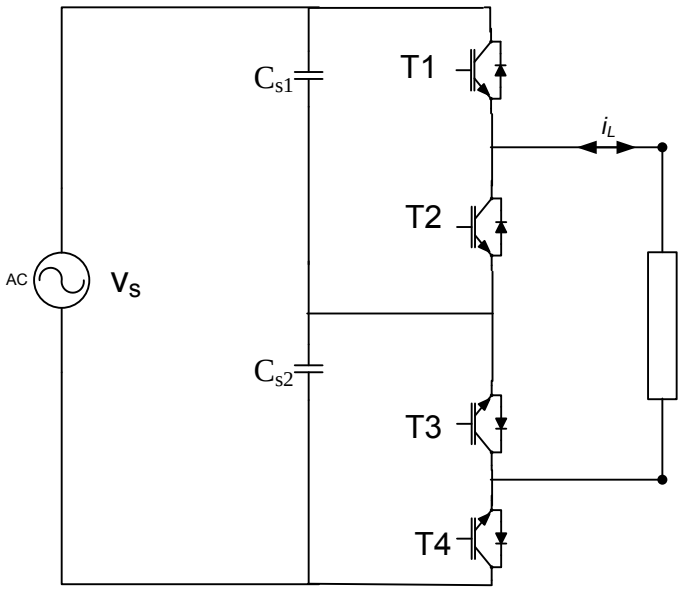


Figure 2.6 Differential chopper

IGBT Topology 3

The non-differential topology is shown in Figure 2.7 below. Snubber capacitor Cs is connected to the commutation cells to absorb the energy stored in the stray inductance in the system. T1 and T4 form one bidirectional switch while T2 and T3 form another bidirectional switch. The IGBTs in this bidirectional switch ensure that at any time the current can be controlled by one IGBT. This topology forms a standard AC-AC converter cell.

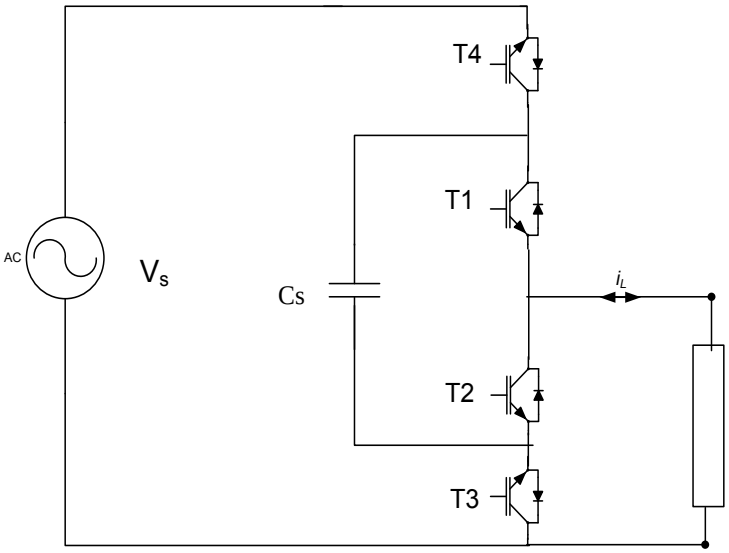


Figure 2.7 Non-differential chopper

Both the differential and non-differential converters have the same control. The control depends on the sign of the voltage source v_s. The advantage of this topology over the differential topology is the neutral continuity.

Variations of both choppers were used in [9] [23] which use two taps of a transformer. In the variation, the chopper is connected to the secondary side of a series connected winding in auto transformer configuration. The operation is similar to the topologies described above. The chopper controls only a fraction of the output voltage as shown in Figure 2.8 below

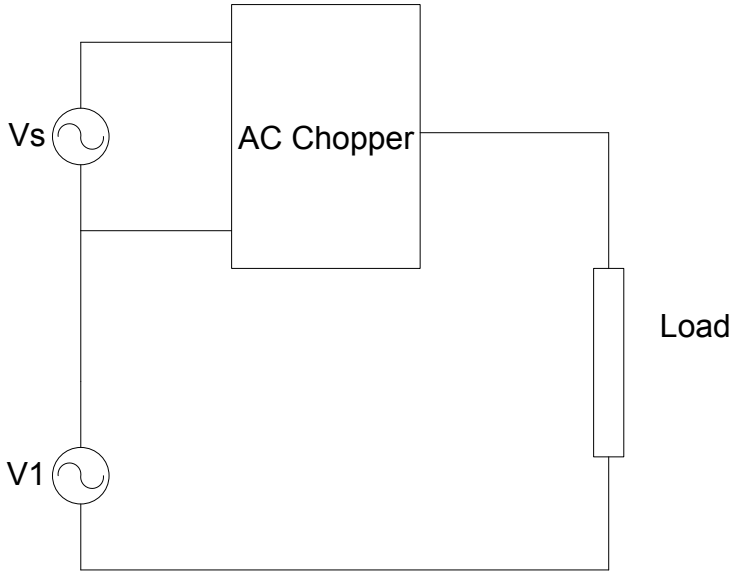


Figure 2.8 Connection of chopper on system with high voltage

This type of configuration is used on systems which operate at a much higher voltages than the IGBTs. The IGBTs are protected by a thyristor based crowbar. The states of the switches are summarised in Table 2.1 below

Table 2.1 Switch state depending on polarity of input voltage

	T1	**T2**	**T3**	**T4**	**Converter State**
$V_s > 0$	1	0	1	1	ON
	0	1	1	1	OFF
$V_s < 0$	1	1	0	1	ON
	1	1	1	0	OFF

The converters have three effective modes: the active mode, the free-wheeling mode and the bypass mode [21]

Active Mode

In this mode the converter is in the ON state. The voltage source is connected to the load through T1 or T4. Energy is transferred directly from the source to the output through the switches and the diodes as shown in Figure 2.9 below

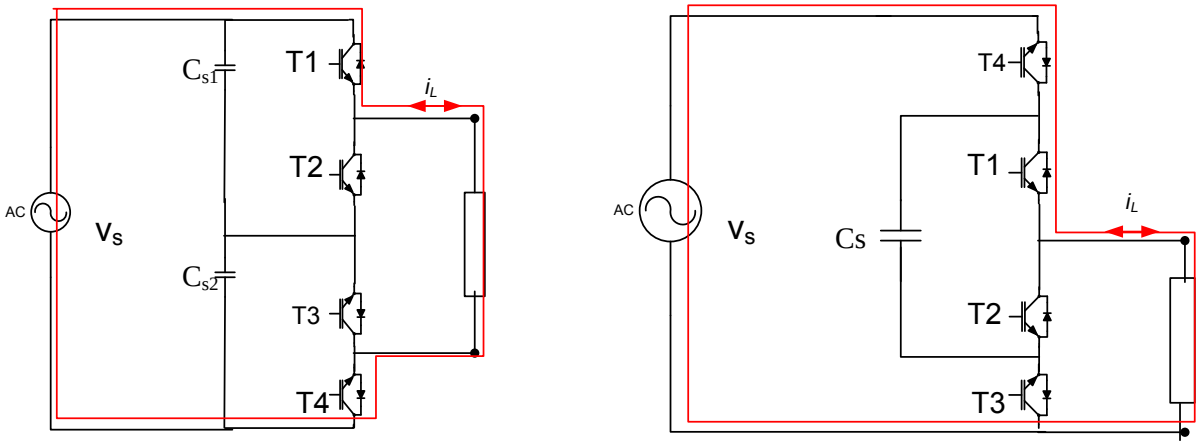


Figure 2.9 Inductor current path in active mode

The freewheeling mode

This mode is complementary to the active mode. The switches T2 and T3 are on and the current free wheels through these switches or their diodes as shown in Figure 2.10 below

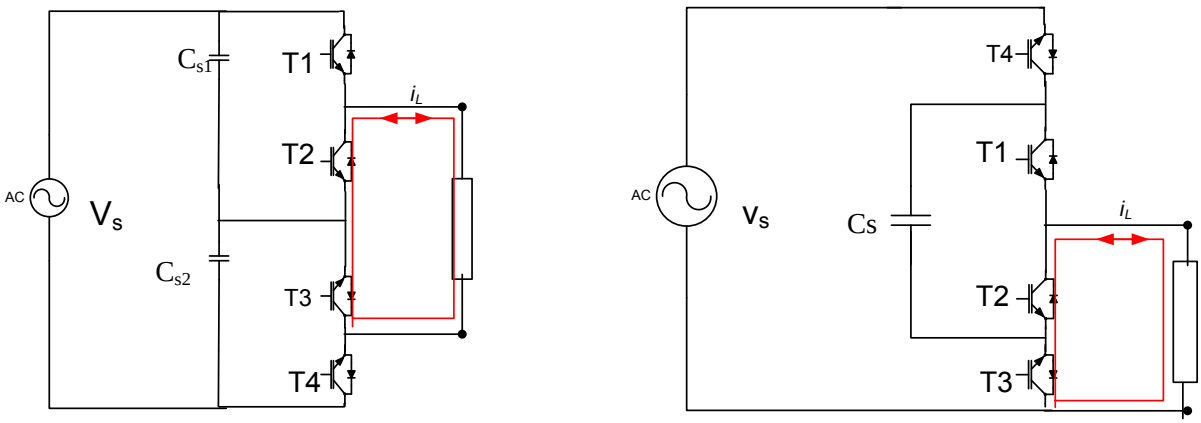


Figure 2.10 Inductor current path in freewheeling mode

Bypass mode

To avoid commutation problems during dead time, two additional switches are turned on so that during the bypass mode there is always an inductor current path for both directions. The bypass mode is imposed due to non-linearity of the power semiconductors. When the v_s is positive, T1 and T4 are turned on for safe commutation. At dead time the inductor current flows in the positive direction through the source, T4 and diode on T1 as shown in Figure 2.11 below

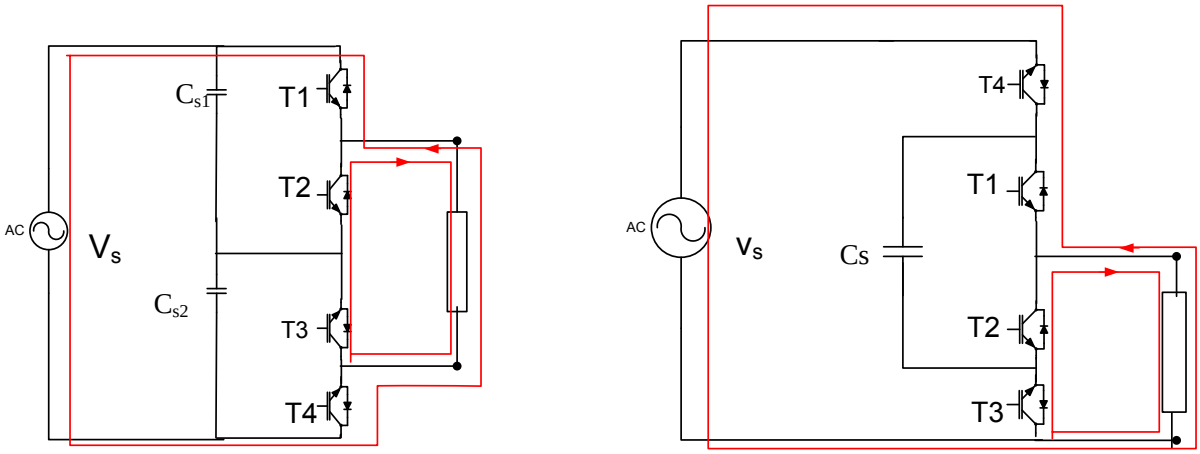


Figure 2.11 Inductor current path in bypass mode

Topology 4

The three phase topology: Three phase A.C. choppers are widely used in A.C. motor speed control. A typical three phase A.C. chopper is shown in Figure 2.12 below. There are many variations of this chopper circuit. The three phase chopper comprises differential IGBTs arranged in a three phase configuration. Its operation is slightly different from the operation of a single phase differential configuration. The operation of the three phase chopper is beyond the scope of this research.

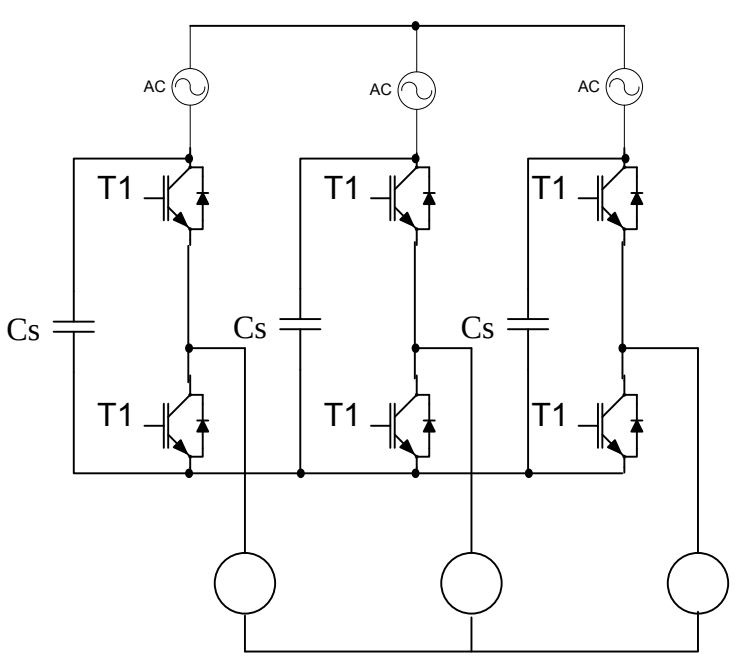


Figure 2.12 Three phase chopper [21]

2.2.2 Solid State Transformers (SST)

The SST is an AC-AC transformation with an intermediate high frequency (HF) AC stage as shown in Figure 2.13 .

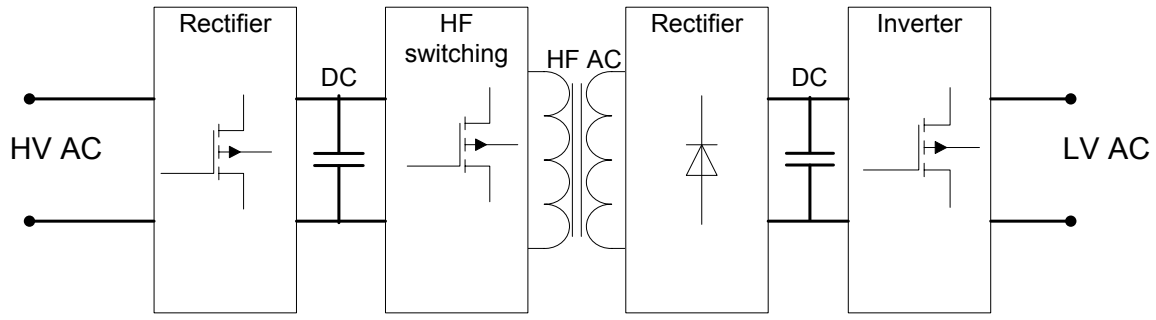


Figure 2.13 Solid state transformer concept [8]

The solid state transformer is basically made up of five stages

- **Input Rectifier:** The input rectifier is made up of active semiconductors (active front end). The DC current and voltage output can then be regulated accurately to the required level. An energy storage device e.g. a capacitor is usually put at the output. The input rectifier can be used to for reactive compensation by making it to be

capacitive. inductive or resistive. The input current can be configured to lead or lag the input voltage.

- **High Frequency(HF) switching:** The DC from the active front end (AFE) rectifier is then inverted to a high frequency AC. The output magnitude and frequency can be controlled at this stage.
- **High frequency (HF)Transformer:** The HF transformer required for transformation is much smaller than a similar rated transformer at 50 Hz.
- **Diode Rectifier**: The transformed high frequency AC is rectified using diodes. There is no control in terms of magnitude at this stage because of the passive rectifier. A capacitor is usually put at the output of the rectifier as an energy storage device.
- **Output Inverter**: The output inverter turns the DC back to AC at the required frequency. Output voltage frequency and magnitude can be accurately controlled with the inverter. Several topologies are used for the inverter. These topologies are the diode clamped, capacitor clamped and the cascaded converters.

The advantages of this type of voltage regulation are [24] [25] [26]:

- The input can be used to correct the power factor of the input power simply by configuring the AFE to be capacitive, inductive or resistive.
- Input harmonics are filtered out by the capacitors, the AFE rectifier and the output inverter.
- Output voltage is immune to input voltage dips and swells
- Output voltage frequency can be controlled precisely. The input frequency variation does not affect the output. This system can be used to supply a system running at different supply frequency e.g. supplying a 60 Hz system from a 50 Hz system.
- Output voltage can be regulated very accurately. Accuracy in voltage regulation is achieved through the control of the AFE output, HF switching output and the output inverter.

2.3 MODEL PREDICTIVE CONTROL

2.3.1 History of MPC

The earliest algorithm of Model Predictive Control was proposed by a French Engineer Richalet and colleagues in 1978 [27], but the receding horizon principle was proposed as early as 1963 by Propoi [28] in open-loop optimal feedback control.

In 1968, Rafal and Stevens [29] presented a control system with a quadratic cost, linear constraints and moving horizon of one. This was essentially an MPC formulation.

Academic interest in MPC started to grow in the nineteen eighties. Various papers were published on MPC under different titles. Titles included *Extended Prediction Self Adaptive Control* [30], *Generalised Predictive Control* [31], *Multistep Multivariable Adaptive Control (MUSMAR)* [32], *United Predictive Control* [33].

MPC later became popular in the chemical and other slow process industries due to simplicity of the algorithm and the advent of computers and the introduction of online optimisation. The MPC control system was ideal for the industry because of its capability of handling multivariable systems and constraints. Sufficient computation power was not available for use in fast processes.

With recent advances in semiconductor technology following Moore's law, the computational power of semiconductors has advanced to the extent that most of the complicated online optimizations are now possible. Microprocessors and programmable devices such as FPGAs are popularly used in modern MPC as a result of the increase in die densities, increased processing speed, better power management and improvement in parallel processing capabilities. Improved voltage and current handling capacities of power semiconductor devices have made possible direct control of motor drives and other power converters. These devices are increasingly being used in online optimisation in MPC formulations.

2.3.2 Branches of Predictive Control

Many control schemes have been proposed and are used in power electronics, the most common controllers being the linear controllers with pulse width modulation (PWM). Figure 2.14 below shows some of the control schemes available for power converters Sliding mode control has already been tested on the same medium voltage regulator of this project [34].

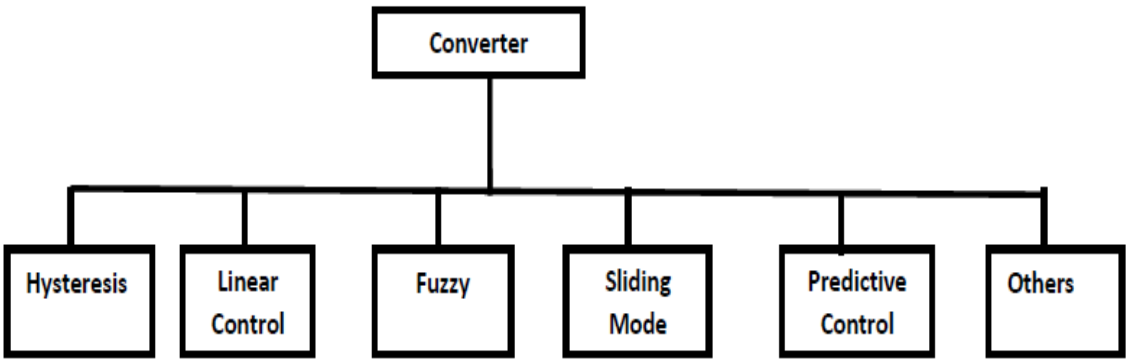


Figure 2.14 Converter control methods [35].

Predictive control can further be broken into several control schemes as shown in Figure 2.15.

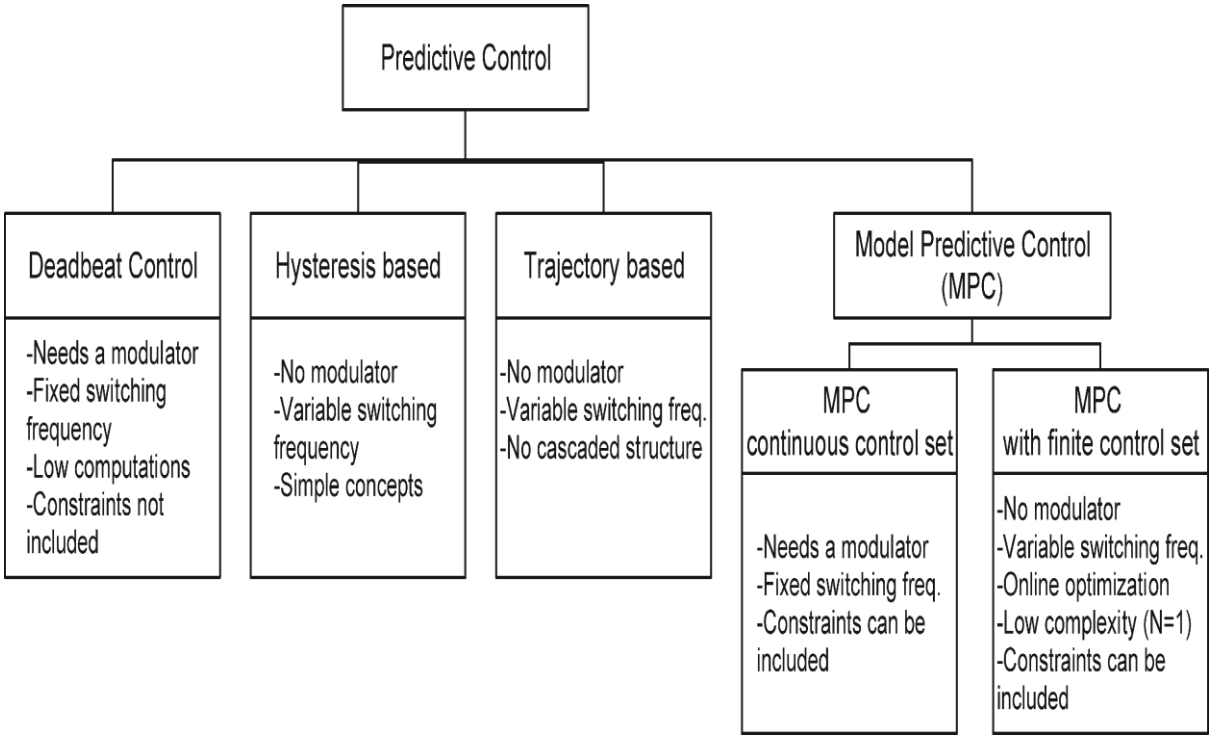


Figure 2.15 Predictive control schemes [35].

Deadbeat control, and MPC with a continuous control set require modulators such as pulse width modulation which results in a fixed switching frequency while hysteresis, trajectory and MPC with finite control set do not require a modulator.

Model predictive control is further divided into two kinds. MPC with a continuous control set and MPC with a finite set control.

MPC with continuous control set requires a modulator as shown in Figure 2.16

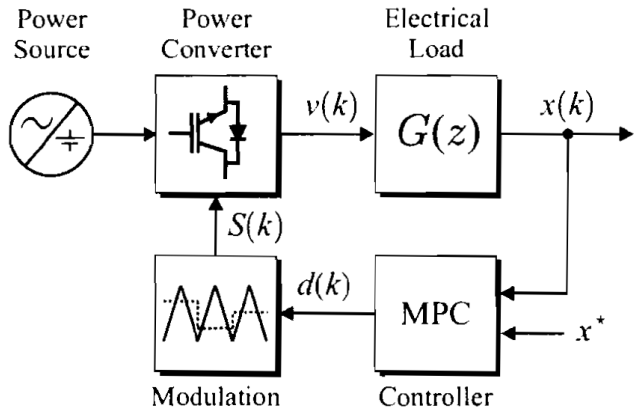


Figure 2.16 MPC with continuous control set [36]

In an MPC with a finite control set, the switch positions form part of the optimisation process. Figure 2.17 shows the finite set diagram.

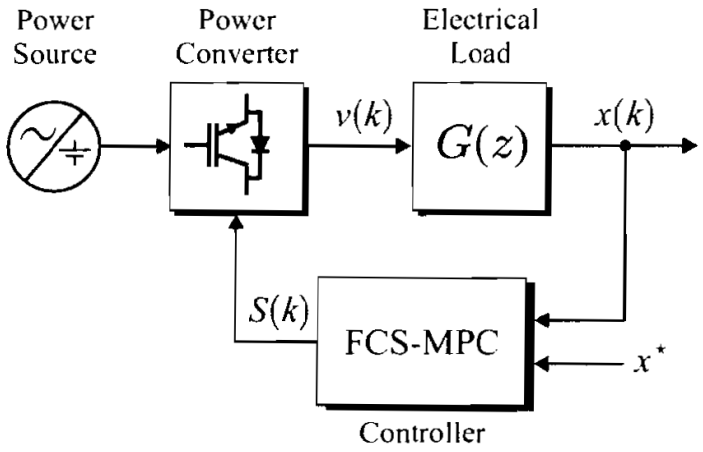


Figure 2.17 MPC with finite set [36]

2.3.3 Model Predictive control theory

Predictive thinking is natural for people for example during driving a car, the driver looks ahead and observes the shape of the road and possible obstacles. The driver brakes near a curve or steps on the gas pedal if approaching a hill and decreases speed if a slower car is in front [37]. The driver has a reference trajectory which they follow – usually road marks and signs. The driver makes all decisions based on the present status (speed, position on the

road, and vehicle performance, other cars behind and in front) and predicts the behaviour of the car in the next few moments. The further and clearer they can see (horizon), the better decisions can be made.

Dynamic optimisation [38] of processes and resources is used in decision making in many areas. Most decisions are made based on the most efficient and cost effective option for achieving a goal. In the automotive industry, car manufacturers strive and customers wish for more fuel efficient engines, whereas in the electrical power industry, more efficient transmission, and distribution networks are desired as well as more efficient end user equipment. In economics and commerce, the most cost effective options are popular choices so as to maximise profit and minimise losses.

The discrete time model of the system can be given by the following equation

$$x(k+1) = g\big(x(k), u(k)\big), x(0)$$

$$x(0) = x_0$$

which describes the future state vector $x(k+1)$ as a function of the current state vector $x(k)$ and the current input vector $u(k)$. The goal of the dynamic optimisation procedure is to find the vector of manipulated inputs, U_N = [u (0), …..,u(N-1)] that will keep the system as close as possible to the objective function over a horizon N. In practice, the sequence of the predicted manipulated inputs cannot be applied because inaccurate system models, disturbances and constraints cause its path to deviate from the predicted path. Therefore, the state is measured at every sampling period and then that measurement is used as the initial condition for predicting the next sequence of manipulated inputs. This repetitive optimisation is used to introduce feedback into the control scheme in order to mitigate the effects of inaccuracies in the system model, disturbances and constraints [39]. Only the next manipulated input is applied. This process is called model predictive control (MPC). There are many types of predictive control laws [40] such as generalised predictive control(GPC), controlled auto-regressive integrated moving average(CARIMA), dynamic matrix control (DMC), quadratic dynamic predictive control(QDMC), receding horizon control (RHC) and many more.

Model Predictive Control (MPC) refers to a class of control algorithms in which a plant or process dynamic model is used to control a process or plant by minimising an objective function. MPC uses the mathematical model of the system to predict the future behaviour. MPC is also referred to as receding horizon control. The MPC process can be summarised as follows [28] [27] [41] [40]:

- Take a measurement of the system's states and outputs

- Compute a finite horizon sequence. Time is divided into regular intervals called time slots.
- Carry out on-line optimization using a cost function and some constraints.
- Apply the vector control variable with the least cos on the controlled plant. And repeat the process.

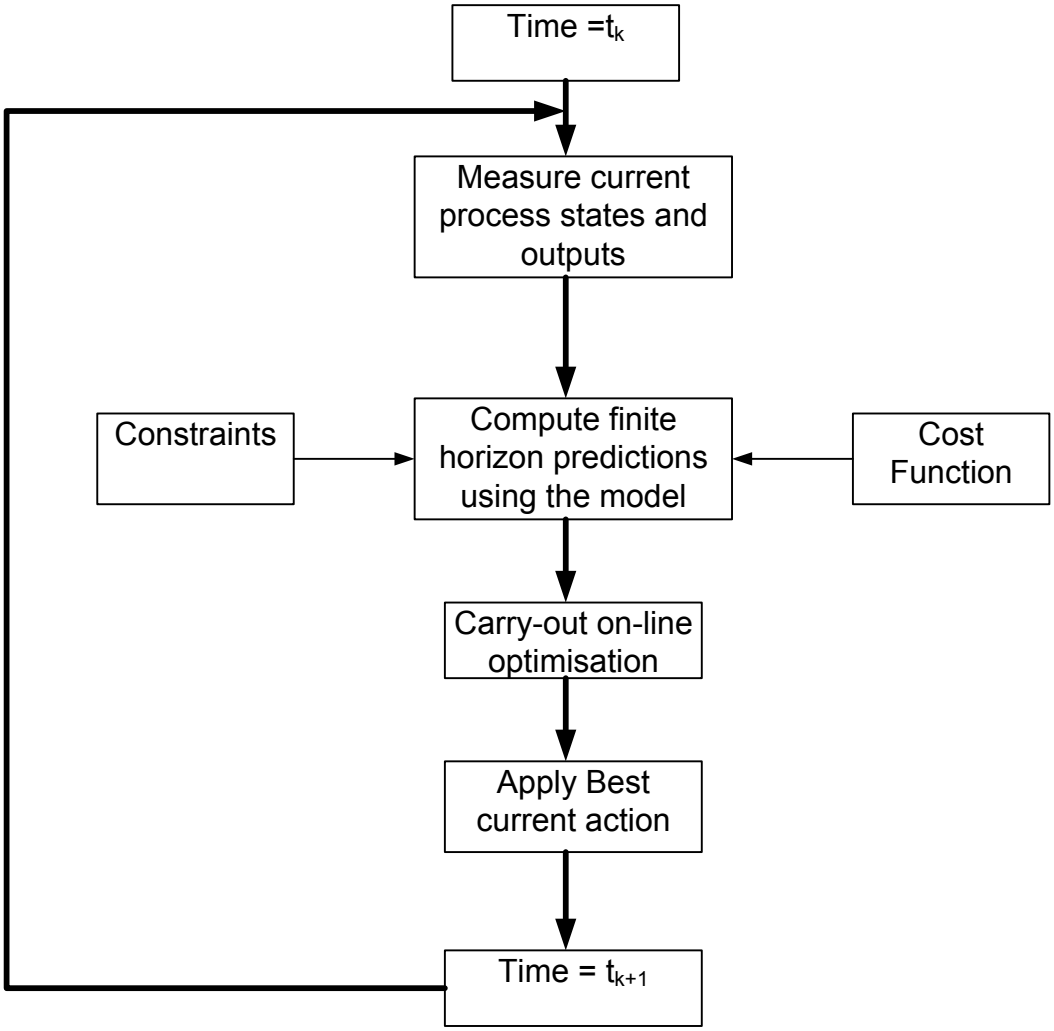


Figure 2.18 Prediction process

- A model of the plant is necessary for the controller
- The success of the controller depends on the accuracy of the model.
- State and process measurements provide feedback for the system.

MPC optimises the current time slot while taking the future time slots into account. This is done by optimising a finite time horizon but implementing only the current time slot [42]. According to [40] the components of model predictive control are:

Influence of predictions on Action

PID (proportional, integral and derivative) controllers do not explicitly consider how the present will affect the future. The future effects are accounted for only to a certain degree by the expected closed loop dynamics. MPC in contrast computes the effect of current actions over a finite horizon. The choice of the present action is dependent on its effect on the plant over the finite horizon. The future output for a prediction horizon N is $y(t+k|t)$[1] for $k = [1 \ldots . \ldots N]$ depending on known values at time t.

Predictions are based on model

The behaviour of a system must be known in order to predict the future and this requires a model of the system. Sometimes an accurate model is not required to get a good control of the system since measurements and predictions occur at every sampling time. Model uncertainties can be dealt with every time the system states are measured.

Most MPC algorithms use linear models. Linear models allow for linear predictions and control choices facilitating the easier optimisation and offline analysis of expected closed-loop behaviour. Where the system is non-linear, the system is modelled as a set of linear models. The linear approximations of the process are then used for the system.

Selecting the input

The choice of the current control action will depend on the control objectives. The control objective is achieved by assigning weighting coefficient to reflect the relative importance of various objectives. The option that minimizes the cost function (the control action that brings the process as close as possible to the reference trajectory $w_{ref}\,(t+k))$ over the prediction horizon is implemented immediately. In multiple input, multiple output (MIMO) systems, the control objectives might be different physical quantities which have different units and orders of magnitude such as voltage, current, frequency etc., therefore, the choice of the weighting coefficient becomes more complicated. There is always a trade-off of the various performance objectives to be achieved. The choice of the various constraints in the cost function becomes a matter of iteration. This scenario is common in modern MPC systems. There is no set method for choosing the best weight coefficient for the cost function [43].The future control signal $\mathrm{u(t+k|t), k = 0 \ldots . N-1}$ will be chosen from various predictions

[1] Indicates value of variable at the instant t+k calculated at instant t

Advantages and disadvantages of MPC

MPC has a lot of advantages over PID controllers in power electronics. Some of the advantages of MPC are [44]

1. MPC concepts are very intuitive and are easy to understand
2. A variety of processes can be controlled at once: anything from processes with simple dynamics to complex systems with long delay times.
3. Multiple variables can be controlled at once, without the need for complex loops, simply by including them in the cost functions. This is in contrast to traditional PID controllers which require superposition of variables where there is more than one variable to control.
4. Non-linearities, such as dead times, are included in the predictions
5. Additional constraints can easily be included in the cost function.
6. The effects of the present actions on happenings in the future are taken into account in the control system.

Some of the disadvantages of MPC are:

- The derivation of an MPC control law is more complex than it would be for the PID controller.
- Dynamic systems require that all computations be done at each sampling time.
- Requires a lot of computing if there are several constraints to be considered.
- Requires an appropriate model of the plant.

2.3.4 Control Strategy

Prediction

If the system states are defined as ‘x’ and the outputs ‘, the general form of future prediction is [40]

$$\underset{\rightarrow k}{\mathrm{x}} = P_{xx}x_k + H_x \underset{\rightarrow k-1}{\mathrm{u}} \tag{2.1}$$

$$\underset{\rightarrow k}{\mathrm{y}} = H\,\Delta \underset{\rightarrow k-1}{\mathrm{u}} + P \underset{\leftarrow k}{\mathrm{x}} \tag{2.2}$$

Where H is a Toeplitz matrix, P is a matrix whose coefficients depend on the model parameters. The arrow pointing right represents only the future values while the arrow pointing left represents present and past values.

In power electronics, circuits are made up of active components such as IGBTs and MOSFET switches and passive components such as resistors, inductors and capacitors. The state of the voltage and currents in these components depends on their parameters and time. For inductors and capacitors these become the state variables of the circuit. Resistors are modelled as ideal. An Inductor is modelled as

$$v_L(t) = L\frac{di}{dt} \tag{2.3}$$

At any time t $v_L(\mathrm{t}) = L\dot{x}(t)$

and capacitors are modelled as

$$i_C(t) = C\frac{dv}{dt} \tag{2.4}$$

At any time $i_c(\mathrm{t}) = C\dot{x}(t)$

where $x(t)$ is the value of the state variable at time t.

Circuits can be presented in a system of two equations called the state space equations. One equation is for determining the state of the system (equation 2.5) while the other is for determining the output of the system (equation 2.6). In the rest of the this document the variable y(t) will be used as the output of the system while and u(t) is used as the system input. The state derivative of the system is denoted $\dot{x}$ (t) and is dependent on the current state of the system and current input.

$$\dot{x} = g[t_0, t, x(t), \quad x(0), \quad u\ (t)] \tag{2.5}$$

$$y(t) = h[\ t, x(t), \ u\ (t)] \tag{2.6}$$

In most cases equations (2.5) and (2.6) are approximated as a linear model wherever possible. The system state change $\dot{x}\,(t)$ and the system output $y(\mathrm{t})$ become linear combinations of input and output. These reduce to equations (2.7) and (2.8) respectively.

$$\dot{x} = A\,x(t) + Bu\,(t) \tag{2.7}$$

$$y(t) = C\,x(t) + Du(t) \tag{2.8}$$

For digital (discrete) linear time – invariant systems, discrete data sets will be used

$$x\,(k+1) = A\,x(k) + Bu\,(k), \qquad k \in \mathbb{N} \tag{2.9}$$

$$y(k) = C\,x(k+1) + Du(k) \tag{2.10}$$

Matrices A, B, C and D are constant matrices. The control and state sequence must satisfy

$$x\,(k) \in \mathbb{X} \subseteq \mathbb{R}^n, \qquad k \in \{0,1,2,\ldots.\}, \tag{2.11}$$

$$u \in \mathbb{U} \subseteq \mathbb{R}^m, \qquad k \in \{0,1,2,\ldots.\}, \tag{2.12}$$

Where $\mathbb{X} \subset \mathbb{R}^{nx}$ and $\mathbb{U} \subset \mathbb{R}^{nu}$

For FS-MPC, input constraint $u\,(k) \in \mathbb{X}$, is constrained to belong to a finite set describing all the possible switch positions [36] and the state variables $x\,(k) \in \mathbb{X}$ are constrained to belong to a finite set .

Prediction and Control Horizon

With MPC, it is possible to predict the state and output of the system several steps ahead for the predicted input signals.

Control is effected only at the immediate step as shown below in Figure 2.19. Notice the prediction and control horizon move at each sampling time. MPC is thus also called receding horizon control.

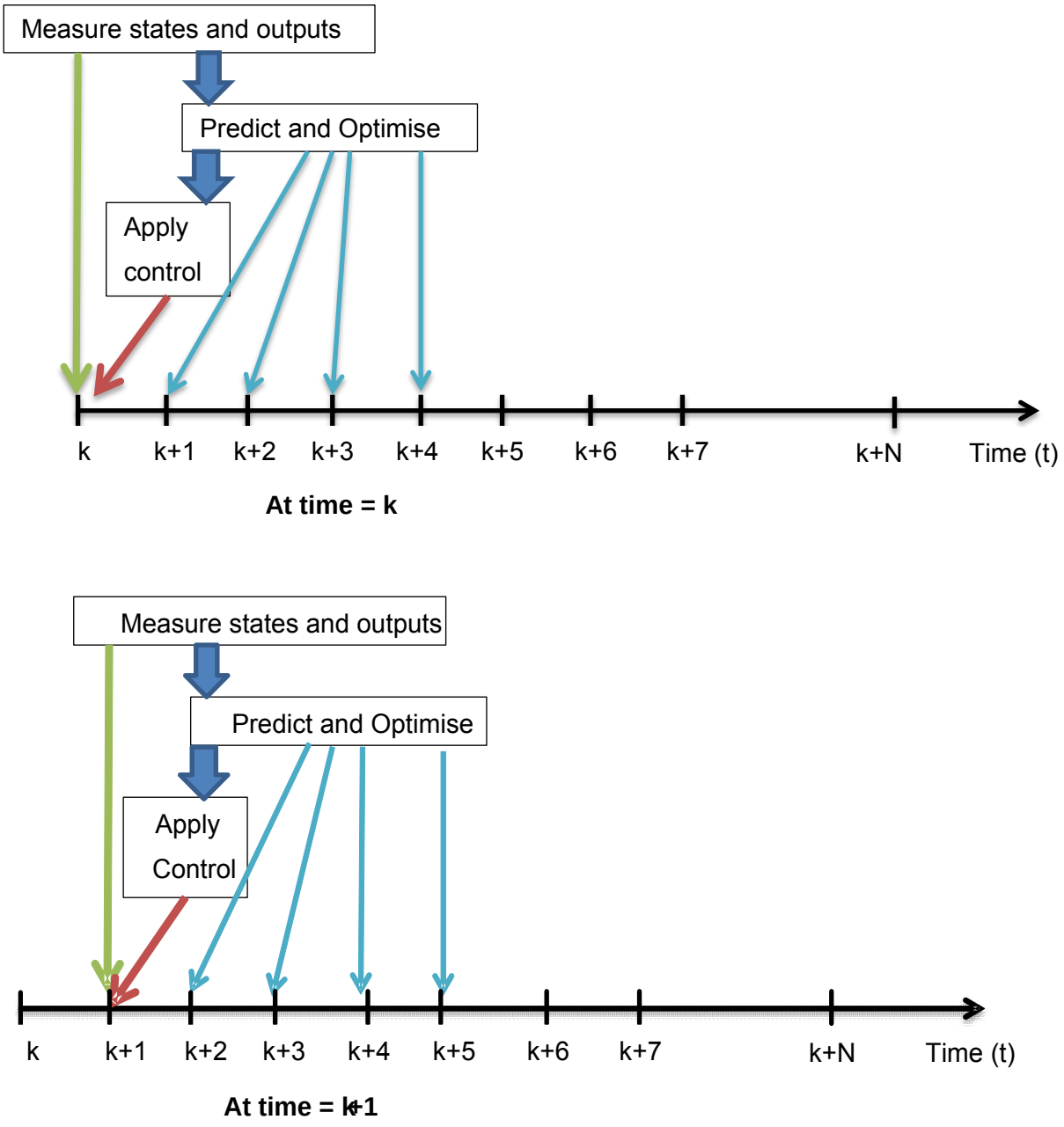


Figure 2.19 Prediction and control process

Equation 2.10 is for one step prediction. Where the prediction horizon is more than one as in Figure 2.19, the prediction algorithm is extended as follows

Prediction for two steps ahead will be

$$x\,(k+2) = A\,x(k+1) + Bu\,(k+1)$$
$$y(k+2) = C\,x(k+2) \qquad (2.13)$$

Substituting (2.10) and (2.11) into (2.14) to eliminate x(k + 1)

$$x\,(k+2) = A^2x(\mathrm{k}) + \mathrm{AB}u\,(\mathrm{k}) + \mathrm{Bu}(\mathrm{k}+1),$$
$$\mathrm{y}(\mathrm{k}+2 = \mathrm{Cx}(\mathrm{k}+2\,) \tag{2.14}$$

This recursion can be extended to give a prediction horizon up to N as [40]:

$$x\,(k+N) = A^N x(\mathrm{k}) + A^{N-1}\mathrm{B}u\,(\mathrm{k}) + A^{N-2}\mathrm{B}u\,(\mathrm{k}+1)+..+\mathrm{Bu}(\mathrm{k}+\mathrm{N}-1) \tag{2.15}$$

$$y\,(k+N) = C[A^N x(\mathrm{k}) + A^{N-1}\mathrm{B}u\,(\mathrm{k}) + A^{N-2}\mathrm{B}u\,(\mathrm{k}+1)+..+\mathrm{Bu}(\mathrm{k}+\mathrm{N}-1) \tag{2.16}$$

A vector of future state predictions can thus be formed for a horizon N as follows:

$$\underbrace{\begin{bmatrix} x(k+1) \\ x(k+2) \\ x(k+3) \\ \vdots \\ \vdots \\ x(k+N) \end{bmatrix}}_{\underset{\rightarrow k}{\mathrm{x}}} = \underbrace{\begin{bmatrix} A \\ A^2 \\ A^3 \\ \vdots \\ \vdots \\ A^N \end{bmatrix}}_{P_{xx}} x(k) + \underbrace{\begin{bmatrix} B & 0 & 0 & \dots \\ AB & B & 0 & \dots \\ A^2B & AB & B & \dots \\ \vdots & \vdots & \vdots & \vdots \\ \vdots & \vdots & \vdots & \vdots \\ A^{N-1}B & A^{N-2}B & A^{N-3}B & \dots \end{bmatrix}}_{H_x} \underbrace{\begin{bmatrix} u(k) \\ u(k+1) \\ u(k+2) \\ \vdots \\ \vdots \\ u(k+N-1) \end{bmatrix}}_{\underset{\rightarrow k-1}{\mathrm{u}}} \tag{2.17}$$

The N horizon prediction for output matrix can be formed as:

$$\underbrace{\begin{bmatrix} y(k+1) \\ y(k+2) \\ y(k+3) \\ \vdots \\ \vdots \\ y(k+N) \end{bmatrix}}_{\underset{\rightarrow k}{\mathrm{y}}} = \underbrace{\begin{bmatrix} CA \\ CA^2 \\ CA^3 \\ \vdots \\ \vdots \\ CA^N \end{bmatrix}}_{P} x(k) + \underbrace{\begin{bmatrix} CB & 0 & 0 & \dots \\ CAB & CB & 0 & \dots \\ CBA^2 & CAB & CB & \dots \\ \vdots & \vdots & \vdots & \vdots \\ \vdots & \vdots & \vdots & \vdots \\ CA^{N-1}B & CA^{\mathrm{N}-2}B & CA^{N-3}B & \dots \end{bmatrix}}_{H} \underset{\rightarrow k-1}{\mathrm{u}} \tag{2.18}$$

The computational effort required to calculate the state equation is doubled with every step increase in the prediction horizon. Figure 2.20 shows the choices encountered at each horizon interval and possibilities of outputs at each sampling time for one switch.

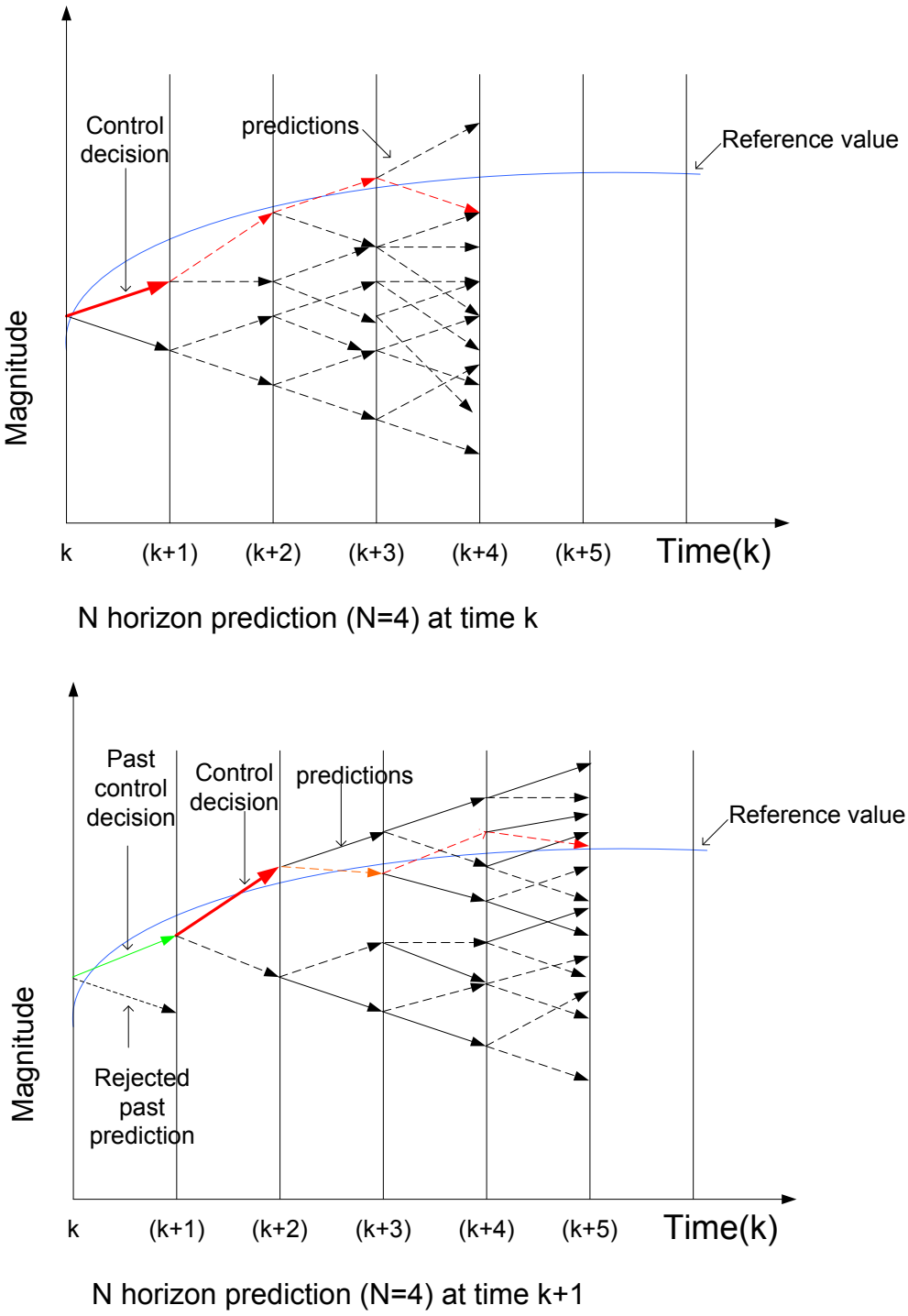


Figure 2.20 Four horizon prediction for a two position switch

At time k predictions are made for k+1 to k+4. The decision is made according only to the prediction for k+1 and the appropriate control move is made. The other prediction is discarded. At time k+1, predictions are again made for the next horizon of 4. (k +2 … k+5). The least cost state to k+2 is chosen and the control is implemented. The choice of control action to be taken is according to the optimisation process explained in the next section. The

choice of the control action at k+1 might not be according to the best trajectory predicted at time k as a result of disturbances, and the inaccuracy of the prediction model.

Optimisation

Optimisation is the selection of the action that will bring the output closest to the control objective. This is done by comparing the options available for action. In a one switch (with two possible positions) N horizon prediction as shown in Figure 2.20 the options double at each increase in horizon. Optimisation is done by minimisation of a cost function J. The cost function is presented in compact notation. There are many choices of optimisation documented. The cost function J [40],

$$J = \sum_{i=n_w}^{N_y} \|r_{k+i} - y_{k+i}\|^2 + \lambda \sum_{i=0}^{n_u-1} \|\Delta u_{k+i}\|^2 = \sum_{i=N_w}^{N_y} \|e\|^2 + \lambda \sum_{i=0}^{N_u-1} \|\Delta u_{k+i}\|^2 \quad (2.19)$$

where e represents the error (difference between the reference values and the predicted values), N_w is the initial horizon, N_y is the output horizon.

For a horizon one predictive control multiple input multiple output (MIMO) system, the cost function J can be calculated thus

$$J = \sum_{i=1}^{n} \|r_i - y_i\|^2 + \lambda \sum_{i=1}^{n} \|\Delta u_i\|^2 = \sum_{i=1}^{n} \|e_i\|^2 + \lambda \sum_{i=1}^{n} \|\Delta u_i\|^2 \quad (2.20)$$

where n is the number of input/output systems and *i* is the *i*th input/output system being controlled.

Cost factors are used to put emphasis on the various factors in the cost function. There are no clear guidelines for allocation of the cost factors [43].

2.3.5 Finite Set Model Predictive Control (FS-MPC)

Finite set model predictive control does not make use of a modulator to determine the switching signal for the converter. Switching signals are sent directly from the controller to the switch signals. The switch is determined to be ON or OFF. The power switch, S(k), is usually included in the control optimisation algorithm as a finite control set constraint [36]. For an FS-MPC, the switch is modelled as an ideal switch and therefore its other parameters can be ignored in the model. FS-MPC has been extensively used in converters [45], [46], [47], [48] , [44], [49] and [50].

Control is restricted to a combination of switch positions for all switches (finite set) represented by

$$u(k) = S(k) \in \mathbb{U} \triangleq \{0,1\}^m \subset \mathbb{R}^m, \qquad k \in \{0,1,2 \ldots .\} \tag{2.21}$$

2.3.6 Reachability and Observability

Given a system in (3.9), matrix pair (A, B) is said to be reachable if it can be driven from any state x(k) to an arbitrary state in finite time.

The reachability matrix of the pair (A, B) is defined as [44]:

$$C\ (A,B) = (B\ AB\ .\ .\ .\ A^{n-1}B) \tag{2.22}$$

The pair (A, B) is reachable if the rank of C (A, B) is equal to n.

The matrix pair (C, A) of the system in (3.9) and (3.10) is said to be observable if it is possible to determine the initial system state from a finite sequence of measurements. The observability of the matrix pair (C, A) is defined as:

$$\mathcal{O}(C,A) := \begin{pmatrix} C \\ CA \\ \vdots \\ CA^{n-1} \end{pmatrix} \tag{2.23}$$

The pair (C, A) is observable if rank of $\mathcal{O}(C,A)$ is equal to n.

2.3.7 Observer design

Sometimes, some states cannot be measured. Instead, only a reduced set of measurements given by

y(t) = C x(t) + Du(t)

is available. The feedback matrix D is assumed to be zero.

An observer has two parts: an exact model of the plant dynamics (A, B, C) and an error correcting part [51]. The equation of the observer is

$$\dot{\hat{x}} = \mathrm{A}\hat{x} + Bu + L\ (y - \hat{y}) \tag{2.24}$$

Or

$$\dot{\hat{x}} = (\mathrm{A} - \mathrm{LC})\,\hat{x} + Bu + Ly \tag{2.25}$$

where L is the observer gain. The observer gain must be selected so that, even though the initial estimate $\hat{x}(0)$ is not equal to the initial state $x(0)$, as time passes the state estimate $\hat{x}(t)$ converges to the actual state $x(t)$.

The quantity $\tilde{y} = y(t) - \hat{y}(t)$ is the output estimation error. To choose L, the state estimation error is defined

$$\dot{\tilde{x}}(\mathrm{t}) = x(t) - \hat{x}(t) \tag{2.26}$$

Its dynamics written as

$$\dot{\tilde{x}} = \dot{x} - \dot{\hat{x}}(t) \tag{2.27}$$

Substituting 3.24 in 3.27

$$\dot{\tilde{x}} = \mathrm{A}x + \mathrm{B}u - (\mathrm{A}\hat{x} + Bu + L\,(y - \hat{y})) \tag{2.28}$$

$$= \mathrm{A}(x - \hat{x}) + L\,(y - \hat{y}) \tag{2.29}$$

The control input does not appear since it cancels out because the input is fed directly into the observer through the B matrix as shown in Figure 2. 21.

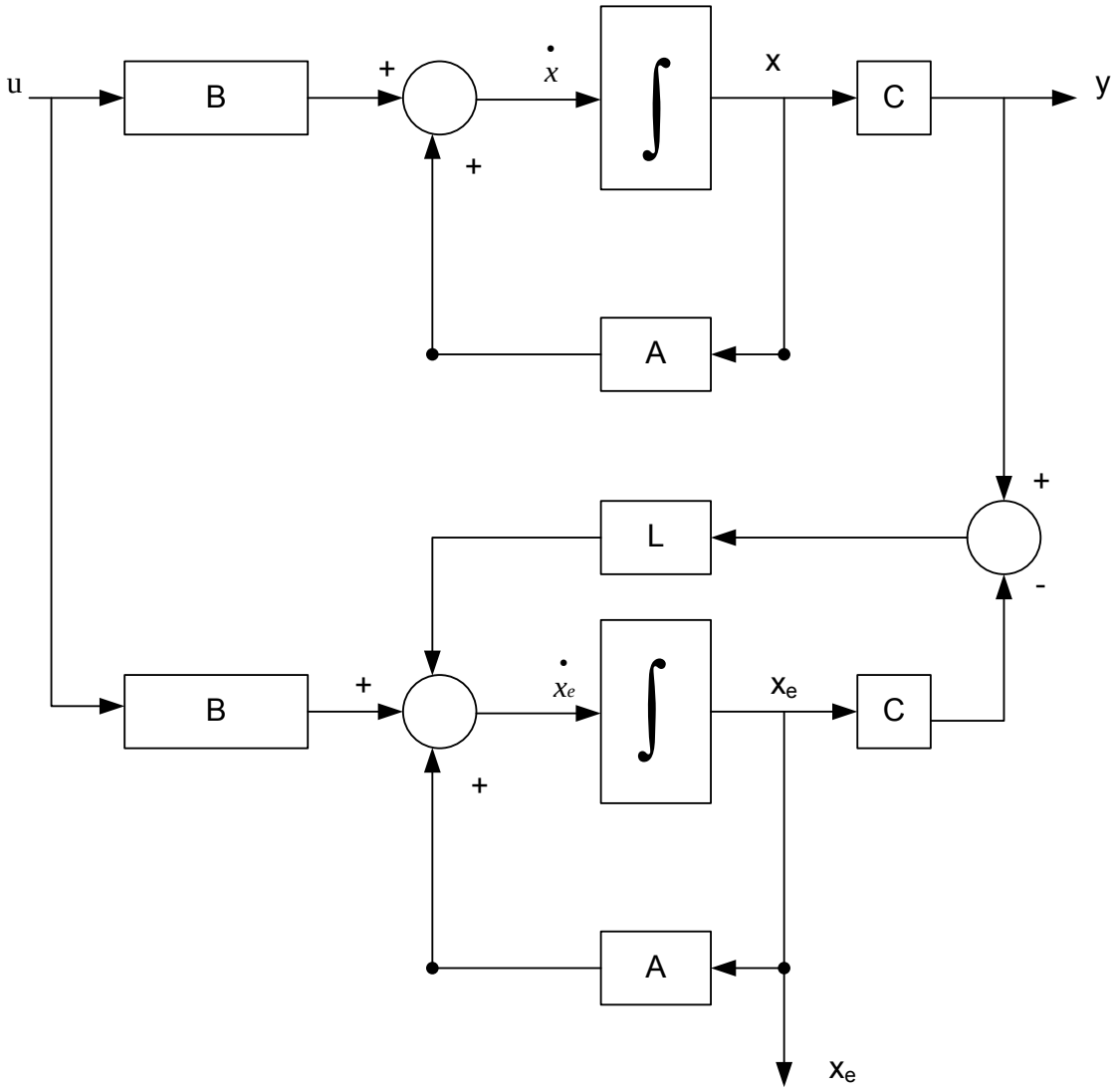


Figure 2. 21 Closed loop estimator

The error dynamics can then be obtained from 2.26 [52]as

$$\dot{\tilde{x}}(\mathrm{t}) = (A - LC)\,\hat{x}(t) \tag{2.30}$$

whose solution is [52]

$$\dot{\tilde{x}}(\mathrm{t}) = e^{(A-LC)t}\,\tilde{x}(0) \tag{2.31}$$

The observer gain matrix L should be chosen such that the eigenvalues of $(A - LC)$ have negative real parts. The state error $\tilde{x}(t)$will then decay exponentially as time approaches infinity no matter how large it may be.

In [44] the observer gain L was chosen such that the closed loop poles were 10 times faster than the open loop poles at a sampling frequency of 10 kHz.

2.3.8 MPC Stability

Determining stability of an MPC system has been a difficult subject. The results have not been valid due to constraints that are active as they are based on linear analysis [40]. To ensure existence of stability, however, a system must have the following characteristics:

- An accurate plant model: An accurate plant model will ensure an accurate prediction and hence the instability of the plant can be detected early. Prediction mismatch can cause instability [40].
- Short sampling steps and longer prediction horizon. A shorter sampling step will detect any deviation from the prediction before the plant goes out of control. Duration of the sampling step will depend on the boundary of performance set by the designer through cost functions and inputs. A longer prediction horizon will also be better able to predict any issues of possibility of future instabilities.
- Tighter cost function on performance and constraints. The tighter the cost function and constraints the better effect on stability. The plant will be forced to operate within safe operating areas and very close to the control objectives most of the time and hence prevent instances of instability.

2.4 SUMMARY

In this chapter, various voltage regulation techniques have been discussed. Among the techniques was the operation of mechanical tap changers, their advantages and disadvantages and a typical example of a commercial mechanical tap changer was shown. A short description of hybrid tap changers followed.

Solid state voltage regulators were discussed, starting with solid state tap changers and ending with solid state transformers (SST).

The chapter ended with a discussion of model predictive control: a brief history of MPC, its theory, the control strategy and the characteristics of MPC.

The next chapter will show the hardware design and layout of the system on which the control was carried out.

CHAPTER 3
HARDWARE DESIGN AND LAYOUT

This chapter provides a detailed analysis of the main parts of the voltage regulator. The main parts to be discussed are:

- Chopper topology: This is a buck converter consisting of two half bridge converters which is connected to the secondary side in an auto transformer configuration.
- The control board: The control board is based on Altera's Cyclone III fpga. The board and its operating system were developed by Stellenbosch University.

3.1 THE MVEVR CIRCUIT

3.1.1 Chopper circuit description

The MVEVR comprises separate modules each connected to a series transformer secondary winding in an autotransformer system.as shown in Figure 3.1 below.

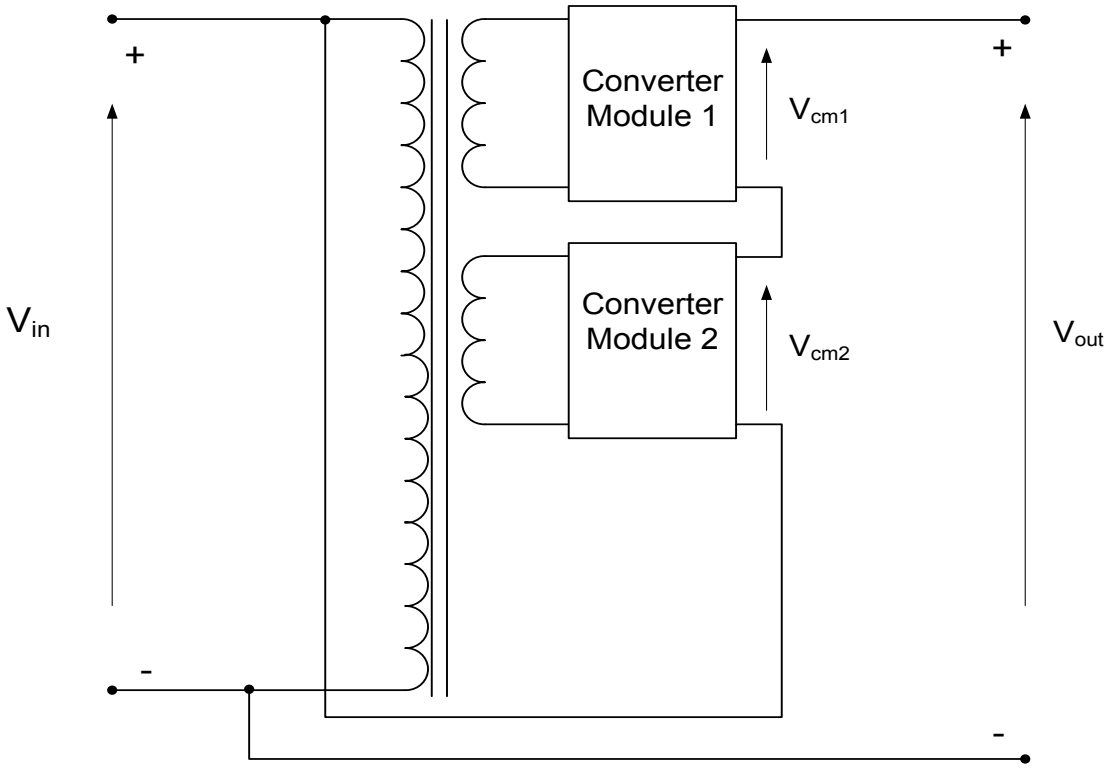


Figure 3.1 The MVEVR overview

Each of the secondary windings is rated at 5% of the input voltage. The output voltage is boosted by 10% by connecting the two windings in series with the primary winding. The advantage of this system is that IGBTs in the modules do not have to block all the system voltage. In this case the IGBTs are limited to handle 1.2kV on a 22kV system. Each module

regulates the voltage independently. Each converter module is made up of LC filters and chopper circuit.

The chopper topology used in the voltage regulator that was considered is shown in Figure 3.2

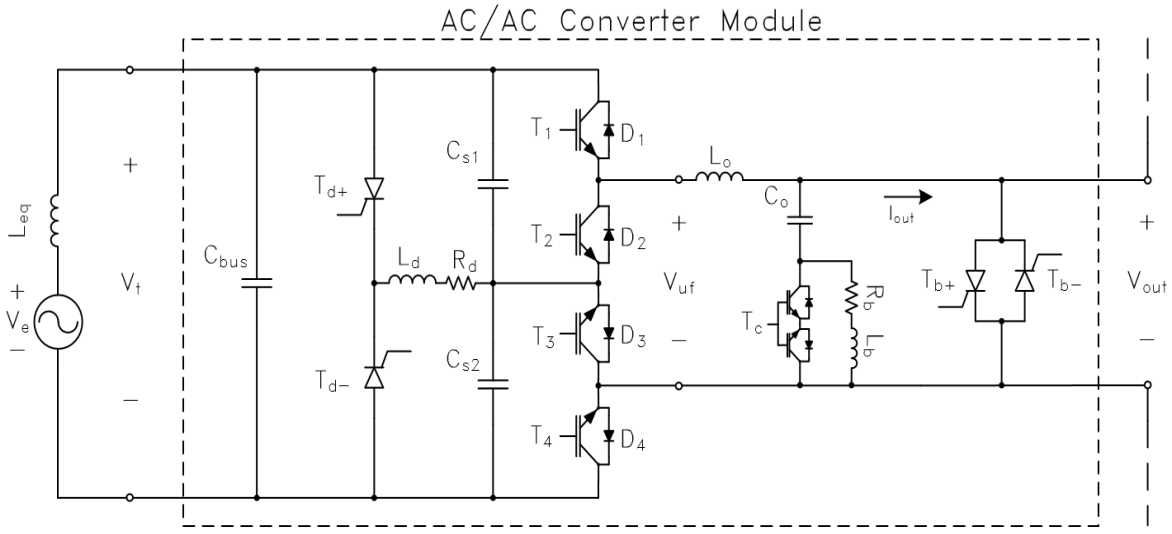


Figure 3.2 Buck AC to AC converter topology with protection mechanism [23]

The Chopper circuit consists of four IGBTs T_1 to T_4 connected in two half bridge topologies (T_1 and T_2 half bridge and T_3 and T_4 half bridge configurations). Each IGBT has its own antiparallel diode so that current can still flow the opposite direction when necessary. Snubber capacitors C_{s1} and C_{s2} are connected at the source of each half bridge converter to provide commutation when all the IGBTs are off. Inductor L_{eq} and capacitor C_{bus} form the input filter while inductor L_o and capacitor C_o form the output filter. Thyristors T_{d+} and T_{d-} together with inductor L_d and resistor R_d form the input bus dump crowbar to protect the IGBTs from bus overvoltage. Thyristors Tb_+ and T_{b-} form the bypass-crowbar to protect the IGBTs from output over voltages and short circuits.

3.1.2 How the AC chopper works

The converter diagram shown above in Figure 3.2 is made up of four IGBTs (T1, T2, T3 and T4) and their anti-parallel diodes (D1, D2, D3 and D4) forming two half bridge converters. During the positive half cycle of input voltage v_t, IGBTs T3 and T4 are constantly switched on while T1 and T2 are switched as a complementary pair as shown in Figure 3.3 and Figure 3.4. During the negative half cycle, IGBTs T1 and T2 are switched on while T3 and T4 are switched as a complementary pair as shown in Figure 3.5 and Figure 3.6.

$$On, \quad if\ Vs \geq 0\ with\ T1\ on\ T2\ off, \qquad T3\ and\ T4\ on$$

$$Off, \quad if\ Vs \geq 0\ with\ T1\ off, T2\ on, \qquad T3\ and\ T4\ on$$

$$On, \quad if\ Vs\ < 0\ with\ T3\ off, T4\ on, \qquad T1\ and\ T2\ on$$

$$Off, \quad if\ Vs\ < 0\ with\ T3\ on, T4\ off, \qquad T1\ and\ T2\ on$$

Flow of current is as illustrated in below

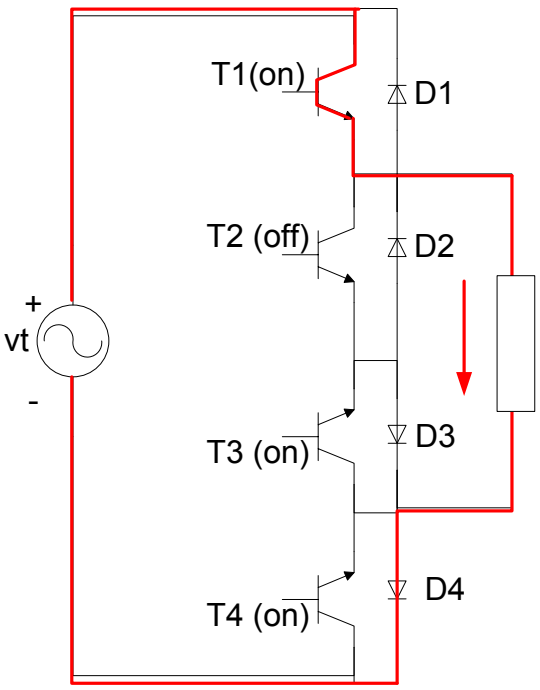


Figure 3.3 Conduction path for positive vt in ON state

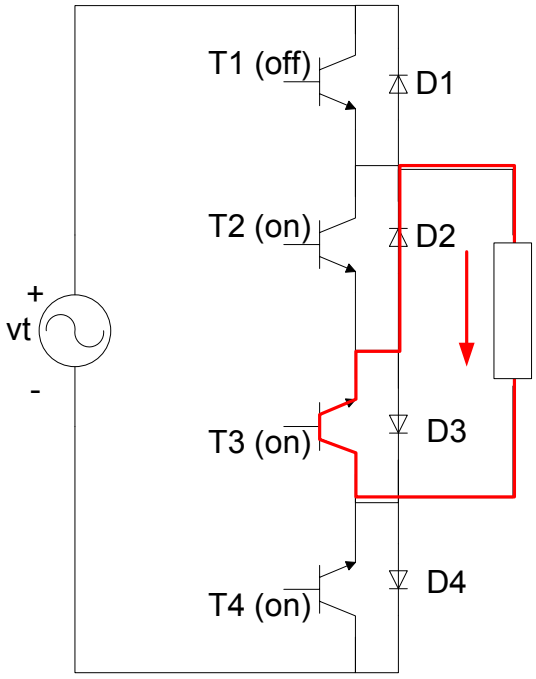


Figure 3.4 Conduction for positive voltage in OFF state

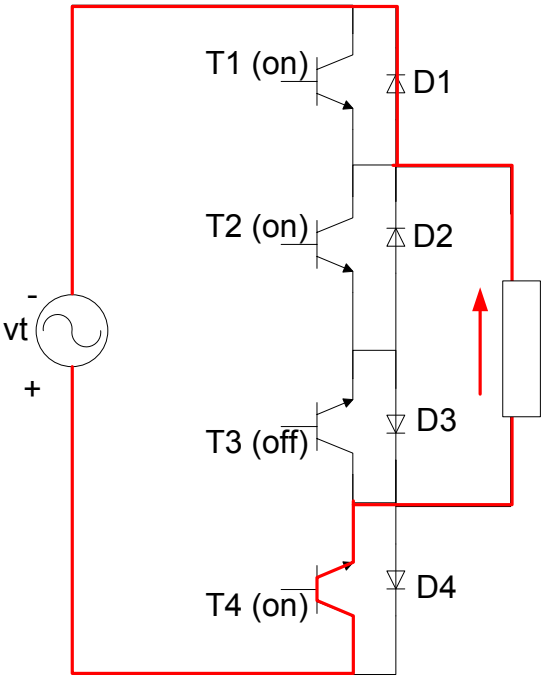


Figure 3.5 Conduction path, for negative vt for ON state

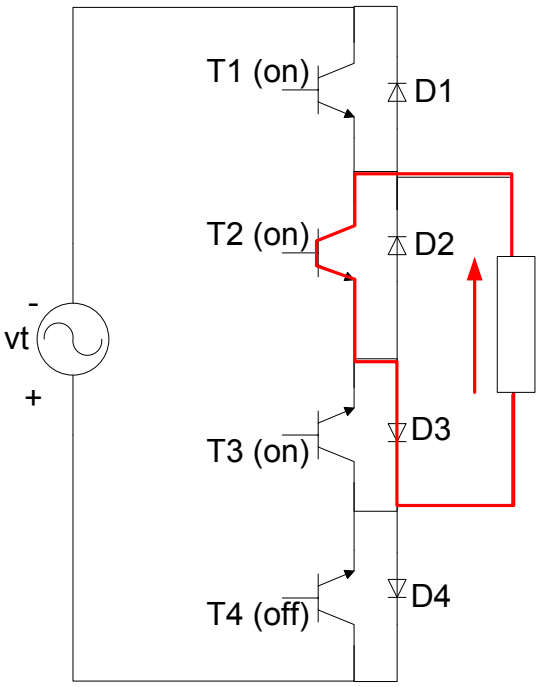


Figure 3.6 Conduction path for negative vt for OFF state

3.1.3 Protection scheme

A protection mechanism has been put in place to protect the module from damage by overvoltage and overcurrent. Faults on the system will initiate a shutdown as follows [34]:

3.1.3.1 Normal shutdown

This shutdown routine is used for safe shutdown when the fault is not critical. The shutdown sequence starts by activating the thyristor bypass crowbar T_{b+} and T_{b-} while the system is switching normally. After the bypass crowbar has operated, the IGBTs are reduced to commutation switching only to prevent the snubber capacitors C_{s1} and C_{s2} from charging to voltages that could damage the IGBTs. Normal shutdown routine can be triggered by

- Incorrect voltage frequency
- Overscaled ADC readings
- Bypass Crowbar operation
- Dump crowbar operation
- Small-signal supply under voltage
- Operator generated shutdown command

3.1.3.2 Emergency shutdown (Desat shutdown)

The Desat shutdown is initiated in the event of critical faults such as overcurrent in the IGBT transistors. Large currents cause the transistor to go beyond the saturation region. When such a critical fault is detected, the bypass crowbar will be initiated and the converter IGBTs will be forced into commutation to prevent the snubber capacitors from charging up to dangerous voltages.

3.2 THE SYNCHRONOUS BUCK CONVERTER

The synchronous buck converter is a versatile converter that can be used for DC to DC and DC to AC conversion. The topology that the controller was tested upon is as shown in Figure 3.7 below

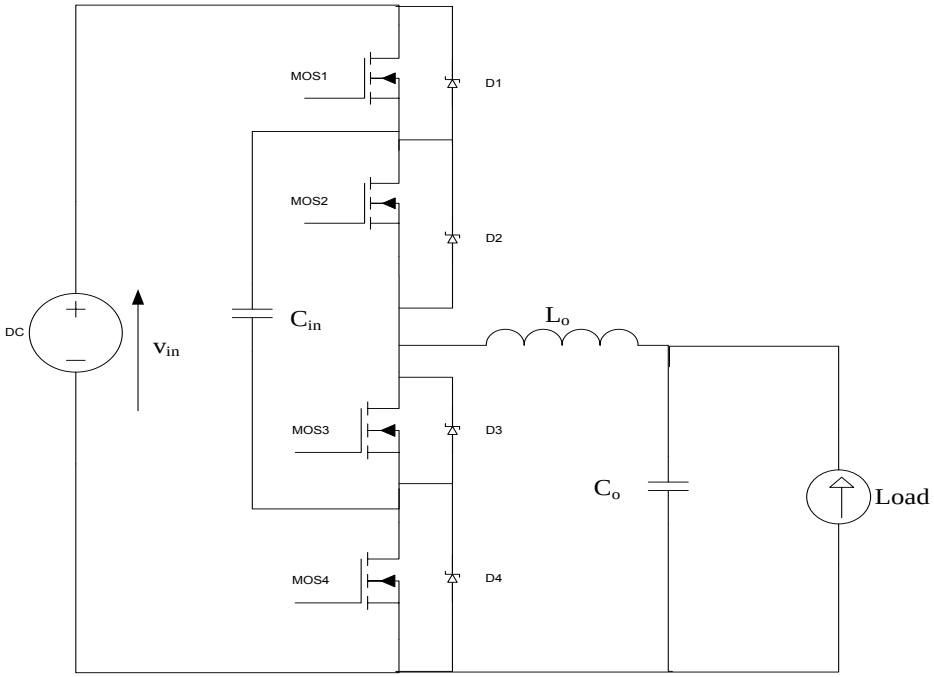


Figure 3.7 Synchronous buck converter topology

The synchronous buck converter is connected in a non-differential topology using N-channel MOSFET. Control of the converter was configured in such a way that it would act like the MVEVR by switching MOS1 and MOS 4 permanently on. MOSFET MOS2 and MOS3 were switched in complementary fashion. Because of the nature of the converter, the AC output had a DC component in it as shown in Figure 3.8 below

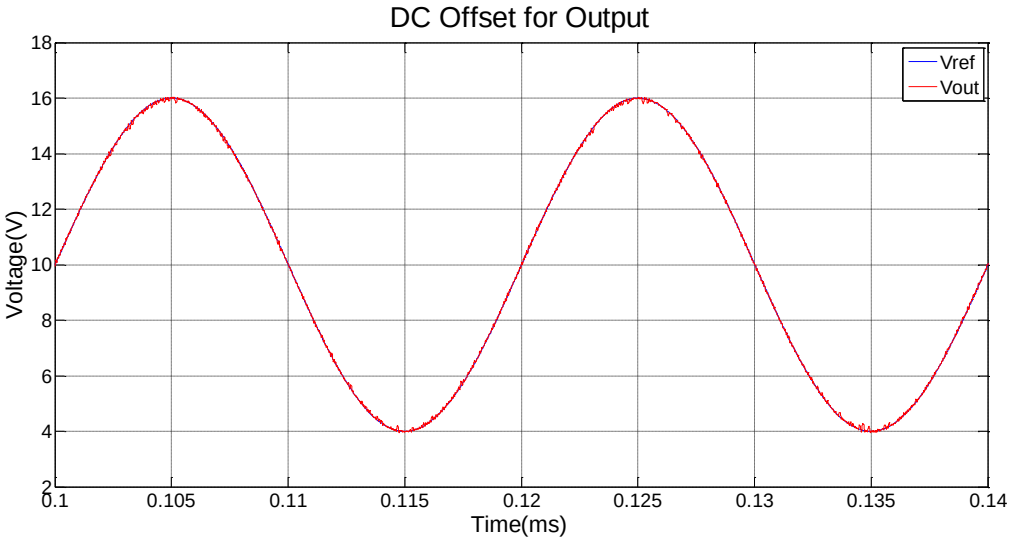


Figure 3.8 Output voltage with DC offset

3.3 FPGA CONTROL BOARD

Altera's Cyclone III is the heart of the control board that was used in this research. According to [53] FPGAs have the following advantages

- Reconfigurability of FPGAs provides designers with almost limitless flexibility. FPGAs enable rewiring of their internal circuitry to allow for a new configuration after the controller has been deployed to the field.
- Unlike processors, FPGAs use dedicated hardware for processing logic. The processing is done in parallel and competition for same the resources is minimized. Multiple control loops can be made at the same time.
- It is possible to configure an FPGA to fit the control algorithm rather than fitting a control algorithm to processor's capabilities. There are no bottlenecks caused by interrupts or event sequencers.
- FPGAs can be used to reconfigure I/O module functionality and then be reconfigured to perform the processing of signals.

3.3.1 Control board operating system

The control(FPGA) board has a backbone software system that controls how the operation of the whole system. A picture of the FPGA control board that was used in the research is shown in Figure 3.9 below.

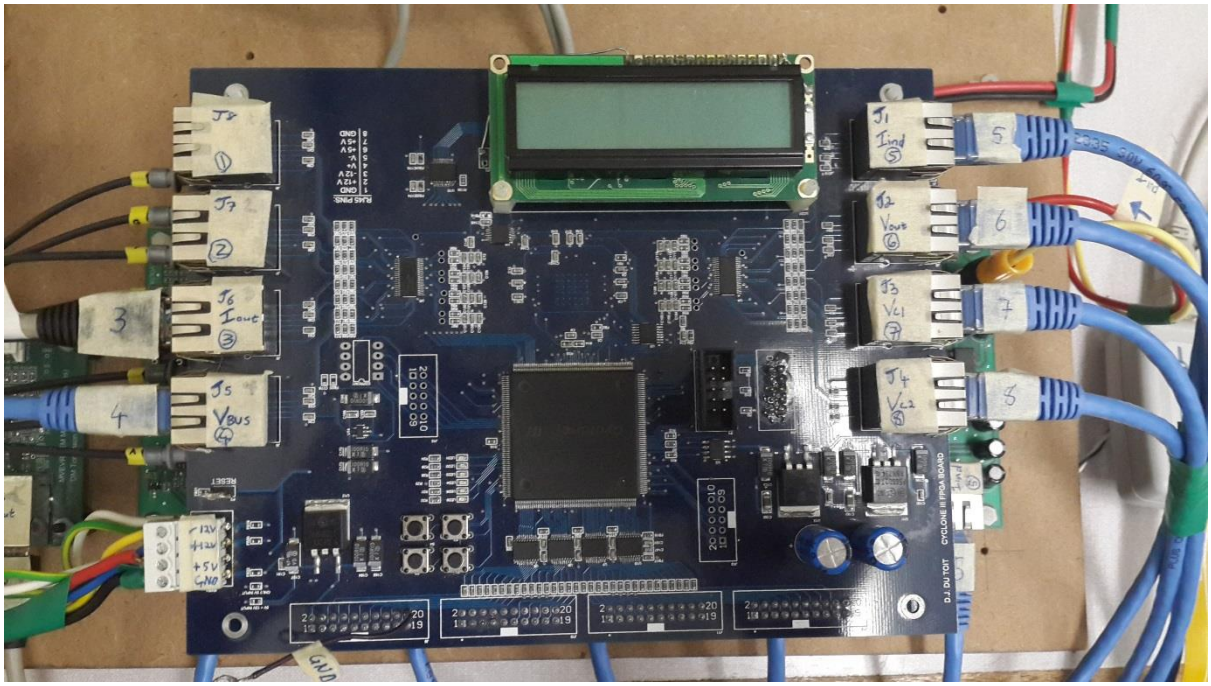


Figure 3.9 FPGA board used in the MVEVR control

The backbone software system is equivalent to the operating system in a computer. It is responsible for the operation of the user interface, the measurements, converter booting and shutdown sequences and the switching sequence of the controller IGBT transistors. The backbone system was developed together with the board over a time by researchers at Stellenbosch University [9] [34] [44]. The operating system advantage is that a researcher concentrates only on the control system that they want to implement. It is also modular, so that new modules can be added to it in order to control more modules. Researchers do not have to spend a lot of time worrying about I/Os, protection and other operation issues. The board software has the following top level structure as shown in Figure 3.10 [34]below.

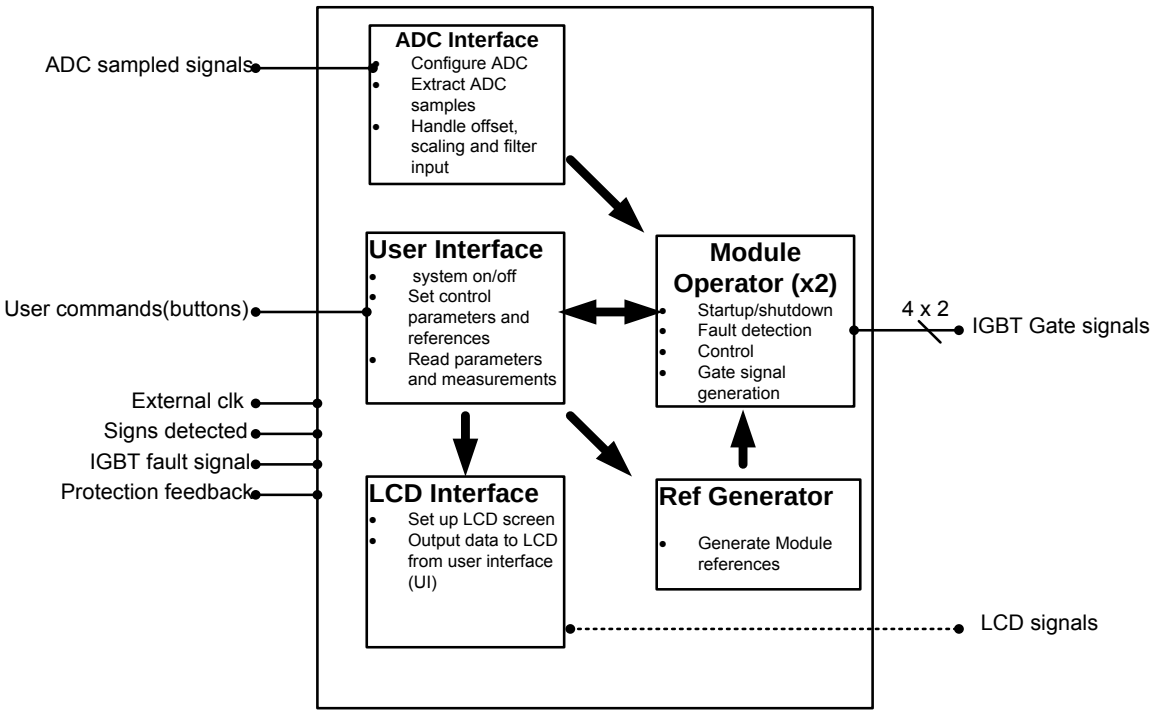


Figure 3.10 Converter operating system top level structure [34]

The top level structure comprises the ADC interface, the User interface, the LCD interface and the Ref generator. All the modules were designed in vhdl.

3.3.1 ADC Interface

The ADC interface was designed to handle and configure data from analogue to digital data capture device ADS 5272 8-channel, 12bit, 65MSPS chip. The ADC interface is made up of three modules designed to handle ADC set up, data fetch and scaling of measured quantity. The three functions the ADC interface does are as shown in Figure 3.11 below.

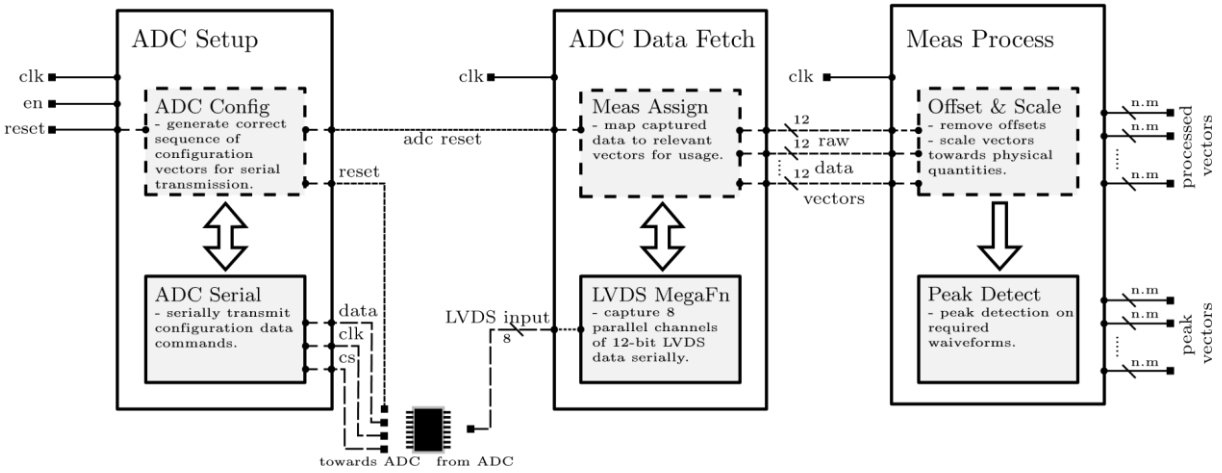


Figure 3.11 The ADC interface component structure [34]

ADC Setup This componenent sends configuration commands to the ADC for

- powering up all the channels needed for measurement
- setting operation to test or normal mode
- setting which bit to start transmitting
- locking on FPGA clock

ADC Data Fetch This component captures the transmitted serial data from the ADC channels and passes them to the Meas Process.

Meas Process This component receives data from the ADC Data Fetch component and scales the data to represent the desired quantity.

3.3.2 User Interface

The User Interface entity is basically the interface between user and the controller. It receives data from the push buttons, relaying it to the relevant process and also sends the controller data to the LCD screen as shown in Figure 3.12

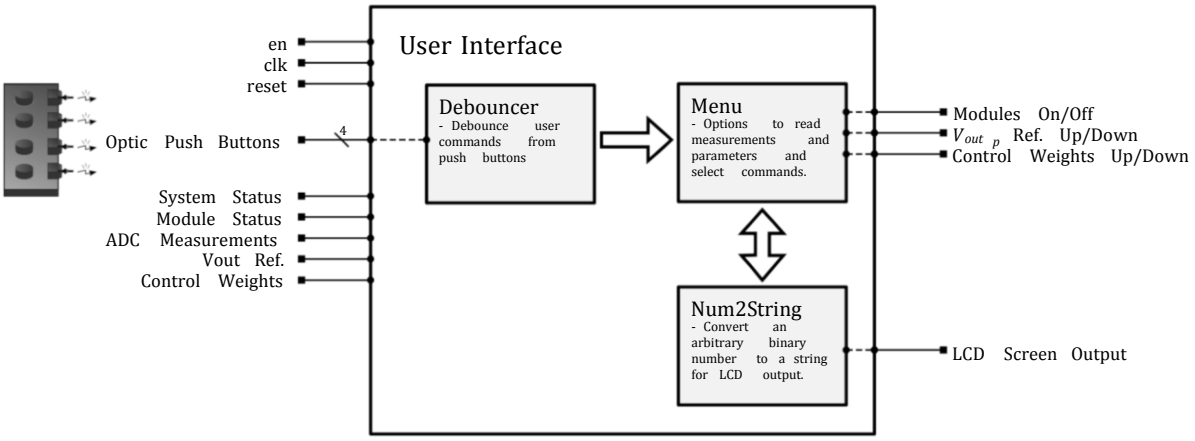


Figure 3.12 User interface component [34]

The user interface allows the user to turn the regulator on and off, vary the reference values by predefined step size and to input cost weight coefficients for the controller. The debouncer component of the UI provides a delay during button presses to prevent a reading being taken many times when a user presses once. The UI Num2string converts digital values to string for display on the lCD. This provides feedback to the user through the display of :

- System status
- Module status

- ADC measurements
- Control reference settings
- Cost function weights

3.3.3 Module Operate Interface

The Module Operate interface is responsible for supervising and controlling the voltage regulators. The Module Operate Interface (MOI) has three components as shown in Figure 3.13. The MOI executes start-up and shutdown procedures, module diagnostics and fault monitoring, commutation, generation of control signals and management of hardware protection systems.

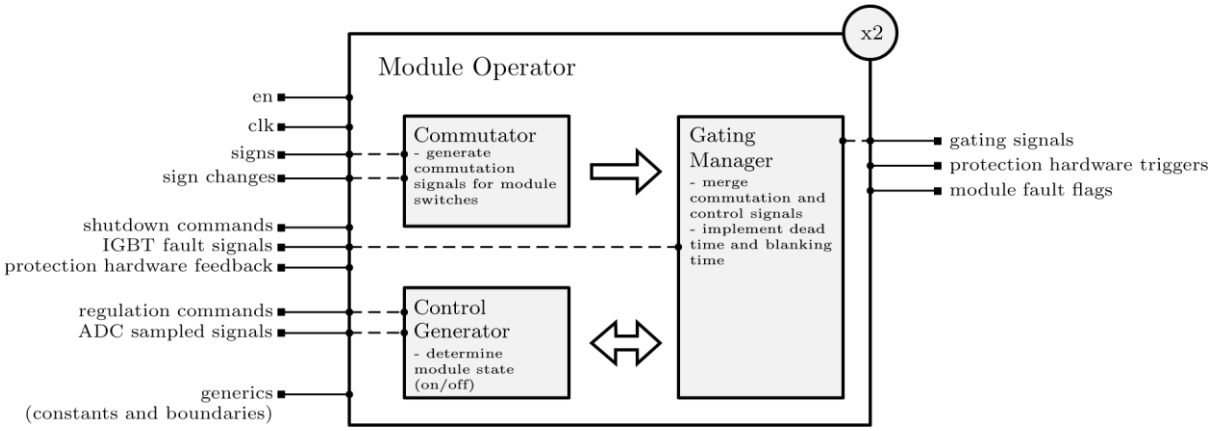


Figure 3.13 Module Operator Interface [34]

The three components of the Module Operate interface are

3.3.3.1 Commutator

The commutator has three components as shown in Figure 3.14 below

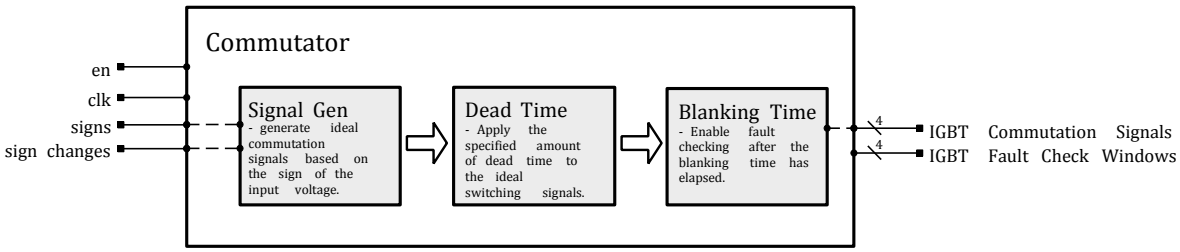


Figure 3.14 Commutation component [34]

The Signal Generator is responsible for determining which pair of IGBTs (T1 and T2 or T3 and T4) needs to be switched on continually for the half cycle depending on the polarity of the AC input voltage as explained in section 3.1.2 of this document.

Dead Time is the switch off time for all the IGBTs applied between change of commutation pairs to prevent shorting between the positive and negative rail of input supply.

Blanking time of 6 µs is applied by the gating manager during changeover of commutation pairs so that the overcurrent should not operate during this time.

3.3.3.2 Control generator

The control generator is the implementation of the Finite Set Model Predictive Control algorithm in vhdl. The operation of this component is discussed in Chapter.

The output of the control generator is the state of the controller in the next state. The next state can only be either a '1' for ON state or a '0' for the OFF state. The output is sent to the gating manager. The control generator does not deal with or monitor the blanking time, dead time or polarity of the input voltage. This gives the flexibility which allows several control algorithms and technologies to be used by just replacing the control generator with the appropriate control system.

3.3.3.3 The gating manager

The gating manager is responsible for switching the IGBts on or off depending on several factors. It is comprises of dead time, DeSat monitor and Sig composer components as shown in Figure 3.15 below.

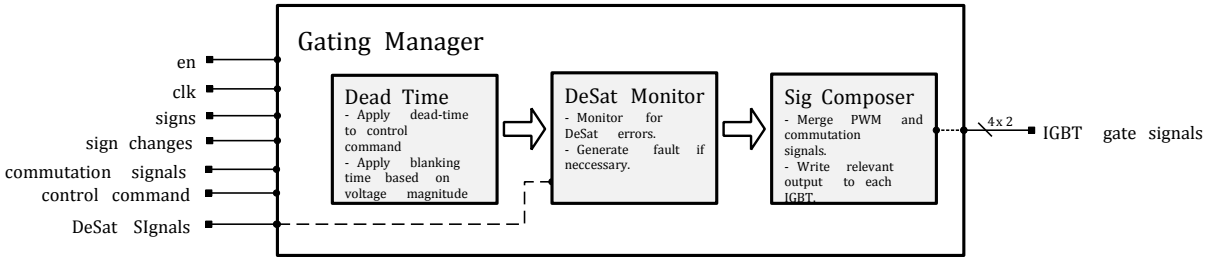


Figure 3.15 Components of the Gating Manager [34]

The gating manager is very critical to the healthy operation of the controller and therefore it requires should not be tampered with. It is responsible for applying the dead time, and also the synthesis of commutation and control generator signals. The signals are then

transmitted to the IGBT driver boards via fibre optic cables. Fibre optic cables are used to isolate the FPGA board from dangerous voltages in the driver and the IGBTs. DeSat monitoring is also done in the gating manager by comparing the saturation status signals from the IGBT driver boards with the expected saturation levels. If there is a significant difference in the levels then the protection mechanism kicks in.

CHAPTER 4
DERIVING THE CONVERTER MODELS

4.1 INTRODUCTION

Finite Set Model Predictive Control uses the plant model to predict the behaviour of the plant to a given input. An accurate model of the plant is, therefore, very important for the accurate control of the plant.

This chapter details how a model of the AC-to-AC converter voltage regulator was obtained. To make an accurate model, each of the converter component's specification was used. After deriving the system model, state space equations are derived for a continuous system starting with the secondary side of the transformer. The internal states of the system are then explicitly accounted for using state equations. The system output can be accurately predicted from the combination of the current system state and the current system input.

Several methods will be explored for discretising the continuous state space equations for digital control.

4.2 MVEVR CONVERTER EQUIVALENT CIRCUIT

Each converter module is connected to a secondary winding of the transformer as shown in Figure 4.1 [44]. The transformer can be modelled as a voltage source with leakage inductance and a series equivalent resistance.

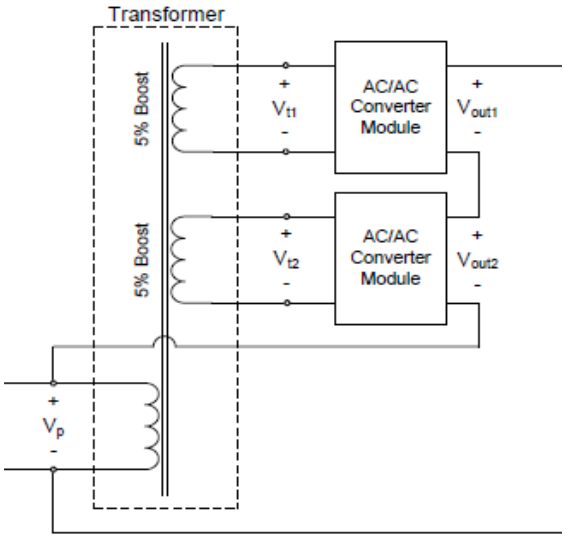


Figure 4.1 AC-to-AC converter regulator with input transformers.

Modelling Transformer

A typical transformer can be represented by an ideal transformer and the following parameters referred to the primary side of the transformer as shown in Table 4.1:

Primary winding joule losses and leakage reactance which can be represented by series inductor X_p and resistance R_p.

1. The secondary winding leakage inductance and winding joule losses represented by X_s and R_s. These are usually referred to the primary side by multiplying them by the square of the primary to secondary winding ratio as shown in the equivalent transformer in Figure 4.2

2. Core or iron losses represented by R_c and magnetizing reactance represented by $X_{M,}$ These are represented in the shunt leg of the model, whis is the magnetizing branch of the model. Iron losses are caused mostly by hysteresis and eddy current effects in the core.

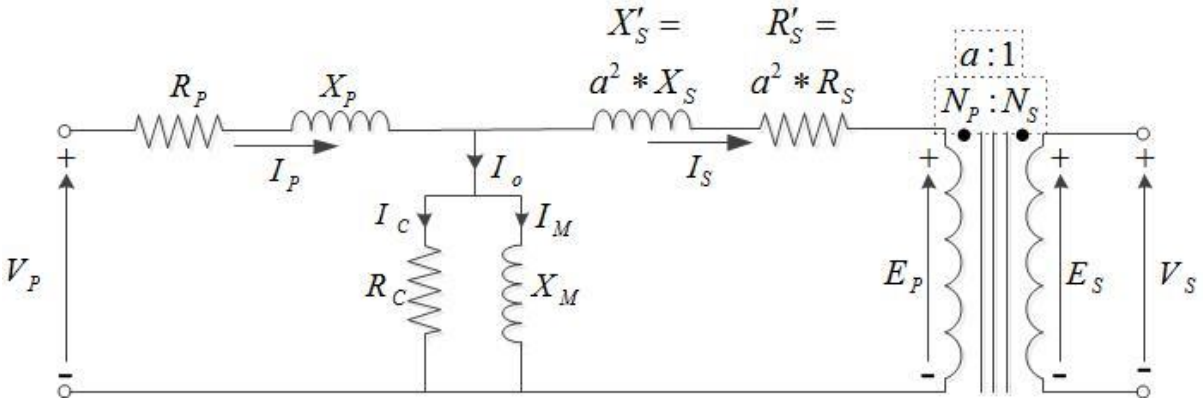


Figure 4.2 Transformer high side equivalent circuit model[2]

There are a number of ways in which these parameters can be derived. They can first be derived from a combination of the following tests: conducting an open circuit test, short circuit test, winding resistance test, and transformer ratio test. They can also be estimated from the given transformer parameters. In this research, the transformer parameters have been calculated from the parameters provided by the manufacturer.

[2] http://en.wikipedia.org//wiki/transformer#Real_Transformer_deviations_ideal

The transformer specifications are as listed in Table 4.1. The secondary windings Vt1 and Vt2 are identical and in the calculation only one secondary winding will be considered.

Table 4.1 MVEVR Transformer Specifications

	Parameter	**Rating**	**Units**
	Power rating	127	kVA
	Primary terminal voltage(rms)	12.7	kV
	Number of secondary windings	2	
	Secondary terminal voltage (Vt1)	635	V
	Secondary terminal voltage (Vt2)	635	V
	Transformer ratio (Vp: Vt1)	20:1	
	Primary full load current	10	A
	Secondary full load per winding	100	A

Leakage inductance is required to model the transformer secondary. The transformer power is taken as base $S_{base.}$. The base power of the secondary then is taken as 127kVA. For each secondary winding the base power S_{base} becomes:

$$S_{base} = \frac{S_{1\varphi}}{2} \tag{4.1}$$

$$= \frac{127\ kVA}{2}$$

$$= 63.5kVA$$

The base impedance of each of the secondary windings is

$$Z_{base} = \frac{V^2}{S_{base}} \tag{4.2}$$

$$= \frac{(635)^2}{63.5kVA}$$

$$= 6.35\Omega$$

where 635 V is the secondary voltage and S_{base} is the power base of each secondary winding.

Taking the maximum leakage inductance for distribution transformer as 0.05, the leakage inductance for each winding is

$$X_{eq} = 0.005 * Z_{base} \tag{4.3}$$

$$= 0.05 * 6.35\Omega$$

$$= 317\ m\Omega$$

The equivalent inductance then is:

$$L_{eq} = \frac{X_{eq}}{2\pi f} \tag{4.4}$$

$$= \frac{317.5\ m\Omega}{2\pi * 50Hz}$$

$$= 1.01\text{mH}$$

The series equivalent resistance for the transformer is taken as 3.0mΩ. Figure 4.3 shows the equivalent circuit for the transformer with a voltage source Vs (V_{t1} or V_{t2}) in series with equivalent leakage inductance L_{eq} and equivalent series resistance $R_{eq.}$

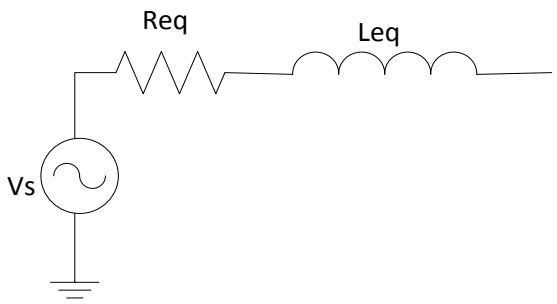


Figure 4.3 Transformer secondary winding equivalent circuit for converter

Capacitors and inductors in the converter have been modelled to their equivalent capacitance or inductance and equivalent series resistor.

The conduction paths for the circuit on 'ON' and on 'OFF' are analysed and equivalent circuits drawn as shown in Figure 4.5 and Figure 4.6.

The converter can be then split onto three equivalent circuits; the input LC filter composed of the transformer resistance and inductance and the bus capacitor, the switches (T1, T2, T3 and T4 with diodes connected in reverse parallel) and the output LC filter as shown in the Figure 4.4 below.

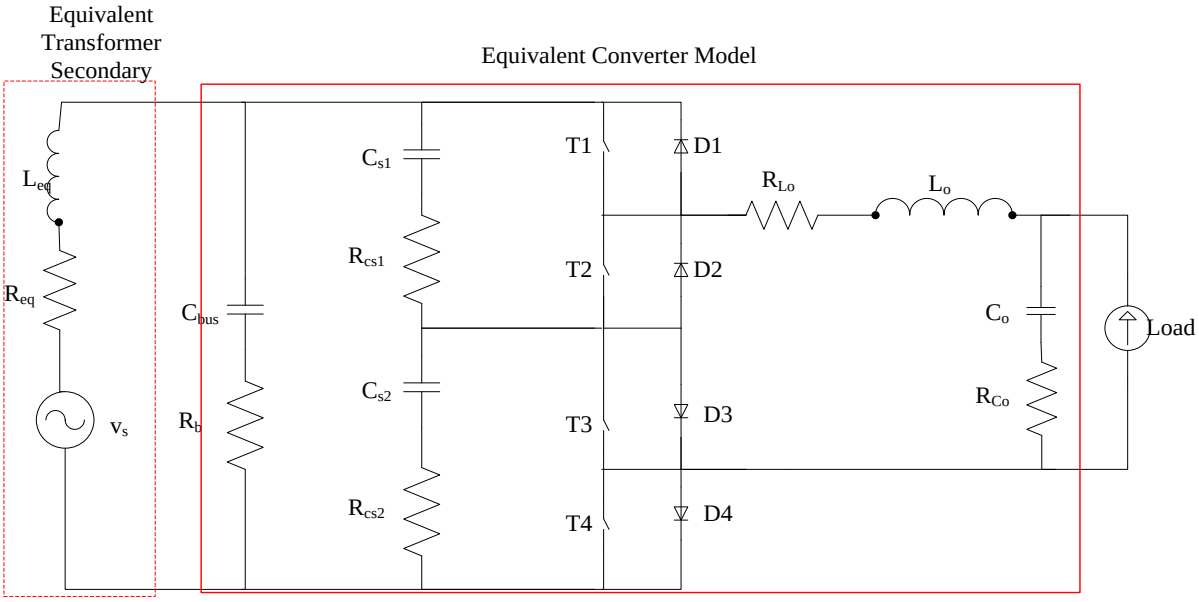


Figure 4.4 The converter equivalent model

The IGBT switches are connected to allow for both positive and negative input voltages. There are only two switching states that the plant goes to; the ON and OFF states. The circuit is symmetrical therefore the ON paths for both positive and negative voltage are the same and can be represented by a similar circuit, while on OFF the circuit paths are also the same for both positive and negative input voltage.

$$On, \quad if\ Vs \geq 0\ with\ T1\ on\ T2\ off, \qquad T3\ and\ T4\ on$$

$$Off, \quad if\ Vs \geq 0\ with\ T1\ off, T2\ on, \qquad T3\ and\ T4\ on$$

$$On, \quad if\ Vs\ < 0\ with\ T3\ off, T4\ on, \qquad T1\ and\ T2\ on$$

$$Off, \quad if\ Vs\ < 0\ with\ T3\ on, T4\ off, \qquad T1\ and\ T2\ on$$

From the circuit parameters of Chapter 2 the input filter the resonant frequency is

$$f_r = \frac{1}{2\pi\sqrt{LC}} \tag{4.5}$$

= 527.88Hz

And the output filter resonance frequency is 798.27 Hz

The system can be described by second-order linear differential equations. The results from the differential equations can be used to find a general solution in terms of the state variable x. Each state can be represented by the state matrix.

$$\dot{x} = A\,x(t) + Bu\,(t) \tag{4.6}$$

$$y(t) = C\,x(t) + Du(t) \tag{4.7}$$

$$z(t) = H\,x(t) \tag{4.8}$$

In this case, H =C so that y=z.

This is a continuous time linear invariant system. In the equation, *u* is the input voltage v_s. Matrices A and B are system parameters as outlined in Chapter 3.

The system state is a vector (t) which contains input equivalent inductor current (i_{Leq}), bus capacitor voltage (v_{cbus}), output inductor current (i_{Lo}), output capacitor voltage (v_{Co}) and output current (i_{out}).

$$x(t) = \begin{bmatrix} i_{Leq} \\ v_{Cbus} \\ i_{Lo} \\ v_{Co} \\ i_{out} \end{bmatrix} = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \end{bmatrix} \tag{4.9}$$

When the system has switched 'ON', the equivalent circuit is as shown below in Figure 4.5.

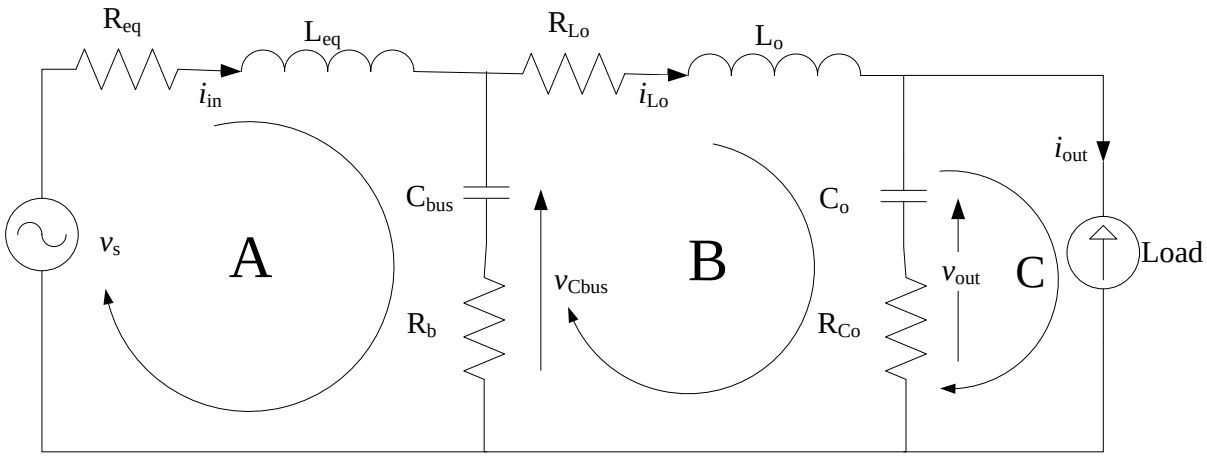


Figure 4.5 Equivalent converter circuit 'ON'

$$v_s = L_{eq}\frac{di_{in}}{dt} + iR_{eq} + v_{Cbus} + C_{bus}\, v_{Cbus} R_b \tag{4.10}$$

Re arranging the terms:

$$L_{eq}\frac{di_{in}}{dt} = -i_{in}R_{eq} - v_{Cbus} - C_{bus}\, v_{Cbus} R_b + V_s \tag{4.11}$$

Resulting to:

$$\frac{di_{in}}{dt} = -\frac{i_{in}R_{eq}}{L_{eq}} - \frac{v_{Cbus}(1 + C_{bus}\, R_b)}{L_{eq}} + \frac{V_s}{L_{eq}} \tag{4.12}$$

Current through the bus capacitor C_{bus} is given by:

$$C_{bus}\frac{dv_{Cbus}}{dt} = i_{in} - i_{Lo} \tag{4.13}$$

Change in bus capacitor voltage is given by:

$$\frac{dv_{Cbus}}{dt} = \frac{i_{in}}{C_{bus}} - \frac{i_{Lo}}{C_{bus}} \tag{4.14}$$

Looking at output voltage v_{out},

$$v_{out} = v_{C0}\,(\,1 + R_o\,C_o\,) \tag{4.15}$$

$$v_{C0}\,(1 + R_o\,C_o) = i_{Lo}R_{Lo} + L_o\frac{di_{Lo}}{dt} + v_{Cbus}(1 + C_{bus}R_b) \tag{4.16}$$

The solution for the differentiated variable is

$$\frac{di_{Lo}}{dt} = \frac{v_{Cbus}}{L_o}(1 + C_{bus}R_b) - \frac{i_{Lo}R_{Lo}}{L_o} - \frac{v_{C0}\,(1 + R_o\,C_o)}{L_o} \tag{4.17}$$

Relating the output inductor current i_{Lo} in terms of output capacitor current and output current yields:

$$i_{Lo} = C_o\frac{dv_{C0}}{\mathrm{dt}} + i_{out} \tag{4.18}$$

Rearranging the terms yields

$$\frac{dv_{C0}}{\mathrm{dt}} = \frac{i_{Lo}}{C_o} - \frac{i_{out}}{C_o} \tag{4.19}$$

Equations (4.9) to (4.13) yield the following A matrix for the 'OFF' position. With a 50Hz output current, we assume the change of the magnitude between adjacent sampling times is,

$$\frac{di_{out}}{dt} = 0 \tag{4.20}$$

From equations (4.10) to (4.20) the state matrix A is derived for the 'ON' state. The load is modelled as a current source. The output current is at supply frequency (50Hz). We assume that the output current does not change over one sampling period.

$$\frac{di_{out}}{dt} = 0 \tag{4.21}$$

$$A_1 = \begin{pmatrix} -\frac{R_{eq}}{L_{eq}} & -\frac{1+R_bC_{bus}}{L_{eq}} & 0 & 0 & 0 \\ \frac{1}{C_{bus}} & 0 & -\frac{1}{C_{bus}} & 0 & 0 \\ 0 & -\frac{1+R_bC_{bus}}{L_o} & -\frac{R_o}{L_o} & \frac{1+R_oC_o}{L_o} & 0 \\ 0 & 0 & \frac{1}{C_o} & 0 & -\frac{1}{C_o} \\ 0 & 0 & 0 & 0 & 0 \end{pmatrix} \quad (4.22)$$

When the converter switches to OFF position, the input LC filter is cut off from the load and the load is only connected to the output LC filter as shown in the equivalent circuit in Figure 4.6,

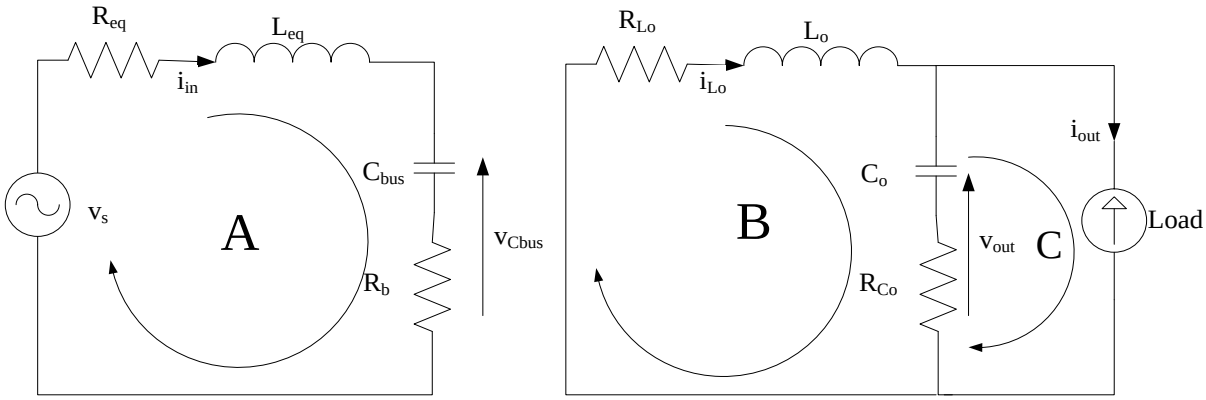


Figure 4.6 Equivalent Converter Circuit OFF

The state variables for the circuit are I_{in}, V_{cbus}, I_{Lo}, V_{out}, and I_{out}. The circuit matrix is derived as follows:

Taking mesh currents current in loop A,

$$v_s = L_{eq}\frac{di_{in}}{dt} + iR_{eq} + v_{Cbus} + i_{in}R_b \quad (4.23)$$

Rearranging the terms,

$$L_{eq}\frac{di_{in}}{dt} = -i_{in}R_{eq} - v_{Cbus} - i_{in}R_b + V_s \quad (4.24)$$

Which results to

$$\frac{di_{in}}{dt} = \frac{-i_{in}(R_{eq} + R_b)}{L_{eq}} - \frac{v_{Cbus}}{L_{eq}} + \frac{v_s}{L_{eq}} \tag{4.25}$$

And input current is the same as the Cbus current,

$$i_{in} = \mathrm{C}\frac{dv_{Cbus}}{dt} \tag{4.26}$$

In loop B,

There is no voltage source:

$$0 = L_o \frac{di_{Lo}}{dt} + i_{Lo}R_{Lo} + v_{C0} + C_o v_{Co} R_o \tag{4.27}$$

Rearranging the terms gives:

$$L_o \frac{di_{Lo}}{dt} + = -i_{Lo}R_{Lo} - v_{C0} - C_o v_{Co} R_o \tag{4.28}$$

and

$$\frac{di_{Lo}}{dt} = \frac{-i_{Lo}R_{Lo}}{L_o} - \frac{v_{C0}(1 + C_o R_o)}{L_o} \tag{4.29}$$

Relating the output inductor current i_{Lo} in terms of output capacitor current and output current yields:

$$i_{Lo} = C_o \frac{dv_{C0}}{\mathrm{dt}} + i_{out} \tag{4.30}$$

Rearranging the terms yields:

$$\frac{dv_{C0}}{\mathrm{dt}} = \frac{i_{Lo}}{C_o} - \frac{i_{out}}{C_o} \tag{4.31}$$

$$\frac{di_{out}}{dt} = 0 \tag{4.32}$$

Equations (4.23) to (4.32) yield the following A matrix for the OFF position. With a 50 Hz output current, we assume the change of the magnitude between adjacent sampling times is,

$$A_0 = \begin{pmatrix} -\frac{R_{eq}+R_b}{L_{eq}} & \frac{1}{L_{eq}} & 0 & 0 & 0 \\ \frac{1}{C_{bus}} & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{R_o}{L_o} & \frac{1+R_oC_o}{L_o} & 0 \\ 0 & 0 & \frac{1}{C_o} & 0 & -\frac{1}{C_o} \\ 0 & 0 & 0 & 0 & 0 \end{pmatrix} \tag{4.33}$$

The matrix B is identical in both states as

$$B_1 = B_0 = \begin{pmatrix} \frac{1}{L_{eq}} \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix} \tag{4.34}$$

$$C = C_1 = C_0 = \begin{pmatrix} 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \end{pmatrix} \tag{4.35}$$

$$D = 0 \tag{4.36}$$

4.3 SYNCHRONOUS BUCK CONVERTER WITH OUTPUT FILTER MODEL

A synchronous buck converter with output filter shown in Figure 4.7 was also modelled. The converter uses two n-type enhanced power MOSFETs operated in continuous conduction mode.

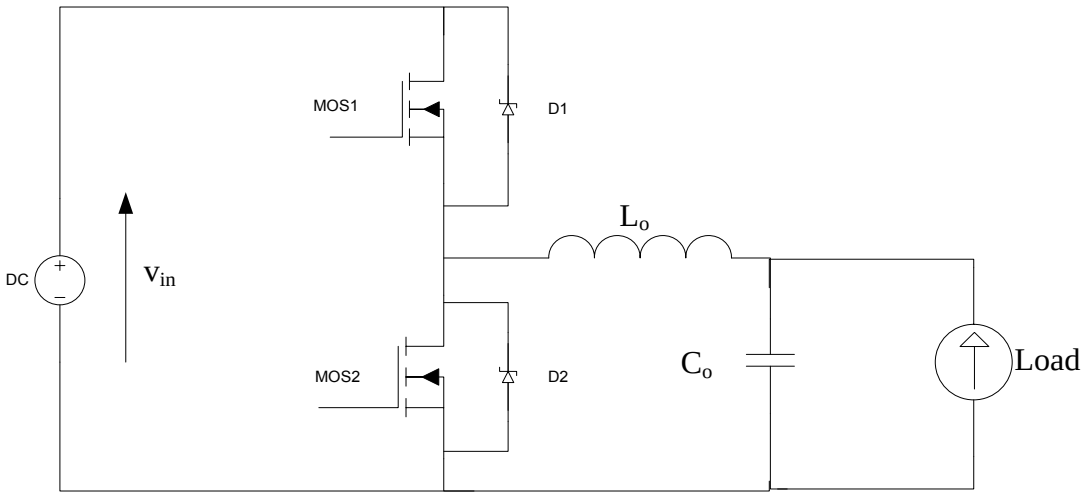


Figure 4.7 diagram of synchronous buck converter

. Switching models are derived by finding expressions for the inductor current and capacitor voltage in the ON and OFF states.

OFF state

The converter is considered switched off when both MOSFET are switched off or when MOSFET MOS1 is switched OFF and MOSFET MOS2 is switched ON. The load is disconnected from the voltage source.

Figure 4.8 shows the equivalent circuit in OFF state and the conduction paths for the currents.

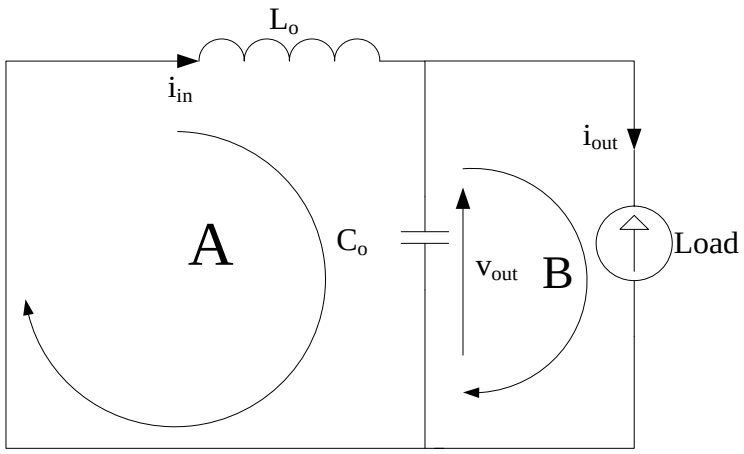


Figure 4.8: Off state of a synchronous buck converter

The equivalent switching circuit is derived by finding expressions for the three variables in the circuit; input current i_{in} (i_L), capacitor voltage v_{co} (v_{out}) and load current i_{out}

In loop A,

there is no voltage source:

$$0 = L_o \frac{di_{Lo}}{dt} + v_{C0} \tag{4.37}$$

$$L_o \frac{di_{Lo}}{dt} + = -v_{C0} \tag{4.38}$$

and

$$\frac{di_{Lo}}{dt} = -\frac{v_{C0}}{L_o} \tag{4.39}$$

Relating the output inductor current i_{Lo} in terms of capacitor current and output current

$$i_{Lo} = C_o \frac{dv_{C0}}{\mathrm{dt}} + i_{out} \tag{4.40}$$

Rearranging the terms yields

$$\frac{dv_{C0}}{\mathrm{dt}} = \frac{i_{Lo}}{C_o} - \frac{i_{out}}{C_o} \tag{4.41}$$

$$\begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} = \begin{bmatrix} i_{in} \\ v_{out} \\ i_{out} \end{bmatrix} \tag{4.42}$$

The equations from 4.37 to 4.41 for the 'OFF' model are expressed in the matrix 4.43 below:

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_o} & 0 \\ \frac{1}{C_0} & 0 & -\frac{1}{C_o} \\ 0 & 0 & 0 \end{bmatrix} * \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_o} \\ 0 \\ 0 \end{bmatrix} * v_{in} \tag{4. 43}$$

On state

The converter is switched 'ON' when MOSFET MOS1 is conducting and MOSFET MOS2 is switched off. In this state, the load is connected to the voltage source. The equivalent circuit and state variables are shown in Figure 4.9 below.

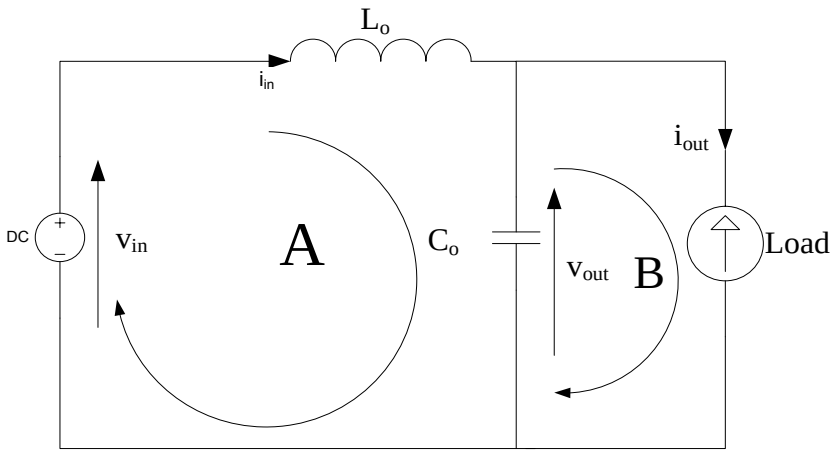


Figure 4.9: ON state of synchronous buck converter

For the current loop A,

$$v_{in} = L_{eq}\frac{di_{in}}{dt} + v_{Cbus} \tag{4.44}$$

$$\frac{di_{in}}{dt} = -\frac{v_{Cbus}}{L_{eq}} + \frac{v_{in}}{L_{eq}} \tag{4.45}$$

Relating the output inductor current i_{Lo} in terms of output capacitor current and output current:

$$i_{Lo} = C_o\frac{dv_{C0}}{\mathrm{dt}} + i_{out} \tag{4.46}$$

Rearranging the terms yields

$$\frac{dv_{C0}}{\mathrm{dt}} = \frac{i_{Lo}}{C_o} - \frac{i_{out}}{C_o} \tag{4.47}$$

With a 50 Hz output current, we assume the change of the magnitude between adjacent sampling times is

$$\frac{di_{out}}{dt} = 0 \tag{4.48}$$

The 'ON' state model expressed in matrix form is

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_o} & 0 \\ \frac{1}{C_0} & 0 & -\frac{1}{C_o} \\ 0 & 0 & 0 \end{bmatrix} * \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_o} \\ 0 \\ 0 \end{bmatrix} * v_{in} \tag{4.49}$$

Discretisation process

The systems so far have been dealt with in a continuous time. To control them using FS-MPC the system models in (4.22) – (4.48) are discretised to [54]:

$$x(k+1) = A_d x(k) + B_d\, u(k) \tag{4.50}$$

$$C_d = C \tag{4.51}$$

$$D_d = D \tag{4.52}$$

where

$$A_d = e^{A_i Ts} \tag{4.53}$$

$$B_d = \int_o^{Ts} e^{A_i \tau}\, \partial\tau \tag{4.54}$$

$$Ts = \frac{1}{f_s} \tag{4.55}$$

See Chapter 3 for details.

Ts is the sampling period and f_s is the sampling frequency.

Equations (4.1) to (4.20) of the system confirm the system to have linear differential equations which can easily be solved.

- There are a number of ways of finding solutions to the problem. Some of the solutions common in power electronics which were considered for the discretisation process are:
- The exact discretisation (linear model)
- The Runge-Kutta4 method
- Explicit Euler method (Euler forward approximation)
- Implicit Euler method (Euler backwards approximation).

The exact discretisation (linear model) is the exact solution to equations (4.43) and (4.45). This discretisation process is also used in [55] [56]. Sometimes the solution becomes very

complicated that approximation methods have to be applied as discussed in Chapter 3. The exact discretisation solution for the converter has been derived [57]as:

$$x(k+1) = e^{ATs}K + xp \tag{4.56}$$

where

x_p is the steady state value for a particular when the converter is the state.

and

K is the difference between the present plant state and the steady state i.e.

K = x_o - x_p

x_o is the initial value.

x_p is calculated from the impedances of the system when the system is in steady state where for a dc steady state, capacitors are deemed open circuits and inductors are short circuits. For the converter circuit, the steady state was deemed to be ac at 50Hz. Therefore all impedances were calculated relative to an input frequency of 50Hz.

For the capacitor, the impedance was: $z = \frac{1}{2\pi 50C}$ while for an inductor the impedance is $z = 2\pi 50L$.

Equation 4.46 will give the same result as equation 4.44.

Where the exact solution is very complicated, an approximation method that is closer to the exact method, the Runge-Kutta approximation method is used. This method is used in [58]. The Runge-Kutta (RK4) was also used in the discretisation of the model;

$$x(k+1) = x(k) + \frac{Ts}{6}(R_0(k) + 2\big(R_1(k) + R_2(k)\big) + R_3(k)) \tag{4.57}$$

$$R_0 = Ax(k) + Bu(k) \tag{4.58}$$

$$R_1(k) = A(x(k) + 0.5Ts\,R_0) + Bu(k) \tag{4.59}$$

$$R_2(k) = A(x(k) + 0.5Ts\,R_1) + Bu(k) \tag{4.60}$$

$$R_3(k) = A(x(k) + TsR_2) + Bu(k) \tag{4.61}$$

Results from the Runge–Kutta method are shown in Chapter 6.

Euler approximation methods have been used in [59] [60]. The Euler forward approximation method is a first order procedure for solving ordinary differential equations (ODEs). It is the simplest Runge-Kutta method [61]. The error per step is proportional to the square of the step size (sampling period). The basic Euler forward method formula is given by

$$\dot{x}(\mathrm{t}) = \frac{x(k+1) - x(k)}{Ts} \tag{4.62}$$

whose initial value is

$$x(t_0) = x_0 \tag{4.63}$$

Rearranging equation (4.33) yields

$$x(k+1) = x(k) + Ts\dot{x}(t) \tag{4.64}$$

where $\dot{x}(t)\ is\ a\ function\ f(x(k), u(k)$

Substituting $\dot{x}(t)$ in Equation (4.64) gives [8]:

$$x(k+1) = x(k) + Ts.f(x(k), u(k)) \tag{4.65}$$

$$x(k+1) = x(k) + Ts.(Ax(k) + Bu(k)) \tag{4.66}$$

Calculations required to implement this discretisation method are easy, but the system becomes more unstable when the sampling period (Ts) increases.

The other Euler approximation method is the Euler backwards approximation also used in [62].

$$\dot{x} = \frac{x(k) - x(k-1)}{Ts} \tag{4.67}$$

$$x(k+1) = x(k) + Ts.f(x(k+1), u(k+1)) \tag{4.68}$$

The Euler forward discretisation method is very hard to implement but is considered more stable than the Euler backward discretisation method.

Figure 4.10 below shows a comparison of the three discretisation methods at sampling times equal to 0.2 s, 0.1 s and 0.01 s.

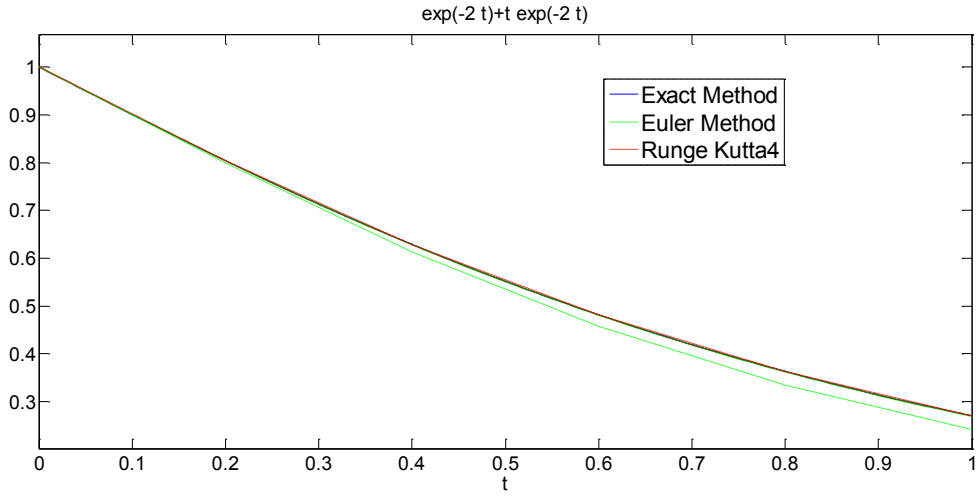


Figure 4.10 Comparison of discretisation methods with Ts = 0.2s

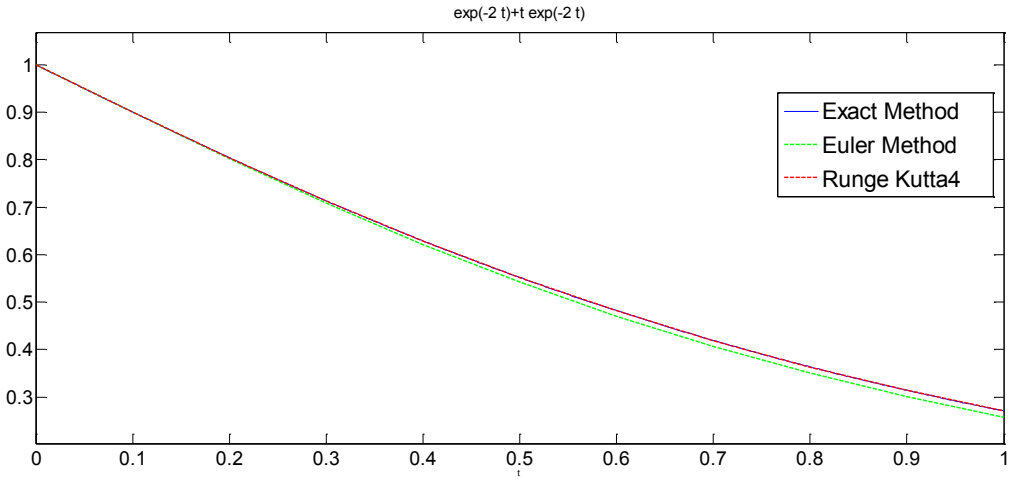


Figure 4.11 Comparison of discretisation methods with Ts = 0.1s

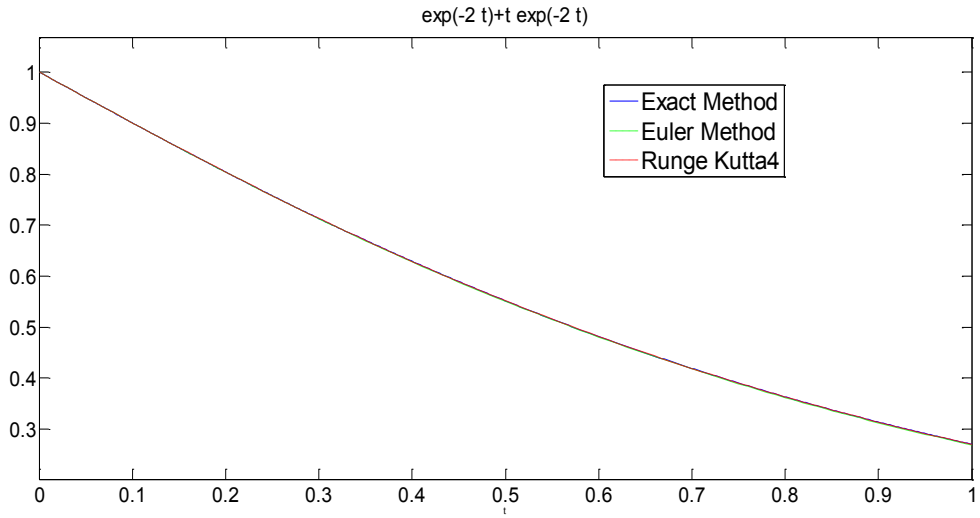


Figure 4.12 Comparison of discretisation methods with Ts = 0.01s

The Runge-Kutta4 method has less error compared to the Euler methods when the step size is large. At very small step sizes (less than 0.01s), the difference between the exact, Euler and Runge-Kutta4 methods is not noticeable.

This shows that all the three methods can be used safely in most power electronic converters where the switching frequency is for most of the time above 2.0 kHz (sampling rate of less than 0.005 s). All the three methods, the exact solution, the Runge-Kutta and Euler method, were used for the simulation of the controller in Simulink. The results from the three systems were compared as shown in Appendix A, Figure A.1 to Figure A.4 The exact discretisation method was chosen for the final controller. The choice of the exact discretisation method was based on its simplicity, accuracy and reliability. These were the factors considered for the final FPGA implementation of the controller.

4.4 Summary

The AC-to-AC Converter voltage regulator was analysed and modelled successfully. The modelling was first done in a continuous mode, starting with the secondary side of the transformer then all the circuit. The transformer was modelled as three parts: the ideal voltage source, the series resistance and the equivalent leakage inductance. These parts were modelled in the circuit.

Various common discretisation methods in power electronics were compared and two methods (exact discretization and Runge-Kutta 4 methods) were used in plant and controller simulations in Simulink due to their discretisation accuracy, stability and simplicity.

The exact solutions to the ordinary differential equations of the continuous model were found. The exact discretisation method was chosen for implementation, due to its simplicity compared to the Runge-Kutta 4 method.

CHAPTER 5
CONTROLLER DESIGN AND SIMULATION

5.1 Introduction

In Chapter 4, several methods of discretising the formula were explored. Formula (2.7) is essentially a prediction of the next state, based on the present state and present input. Two methods were chosen for implementation in the MVEVR controller simulation: The Runge-Kutta (RK4) method and the exact solution. The Euler approximation method and the exact discretization methods were used for the synchronous buck converter SIMULINK simulation.

This section shows how the controller was designed from the discretisation process. It continues from the discretisation methods used in the previous chapter (Chapter 4), continuing with an explanation of how various parameters were calculated and the method used to control the switching frequency. The chapter ends with the application of cost factors to the controller.

The first part starts with the control prediction algorithm, then the second part deals with the control of switching frequency and the final part explains how cost minimisation was achieved. SIMULINK simulation results for MVEVR and synchronous buck converter control will be shown

5.2 Design specifications (requirements)

The voltage regulator is required to be able to regulate voltage to NRS-048-2 standard as indicated in Table 1-1 and Table 1-2, at a nominal voltage of 22 kV. To achieve this, sampling was carried out at 100 kHz. The IGBT switching frequency was limited to an average of approximately 10 kHz in order to limit switching losses [34] [9] [44].

5.3 Controller schematic

The controller schematic for the MVEVR is shown in Figure 5.1, and the control process is shown in Appendix C. The controller has five components: measurements, predictor algorithm, cost minimisation, switching frequency control and the switch controller.

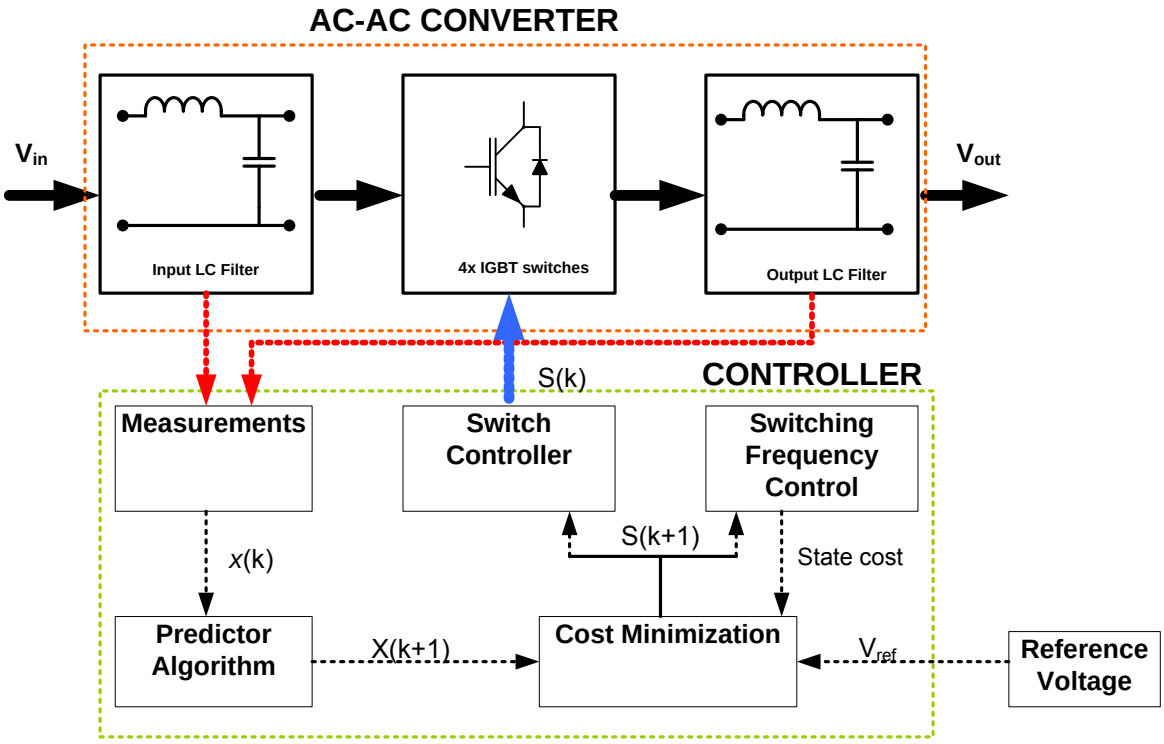


Figure 5.1 MVEVR Controller schematic

Measurements: The measurement component is responsible for measuring voltages and currents in the input and output MVEVR filters. The parameters measured are the equivalent inductor current (i_{Leq}), input voltage (v_{in}), bus capacitor voltage (v_{cbus}), output inductor current (i_{Lo}) output capacitor voltage (v_o) and output current (i_o).

Predictor Algorithm: The basics of prediction algorithms were outlined in Chapters 3 and 4. For Simulink simulation of the MVEVR control, the exact solution and the Runge-Kutta4 methods were used while for the synchronous buck converter controller simulation, the exact discretisation method and the Euler backward methods were used.

The basic predictor algorithm for the exact solution was reduced to Equation (4.56) where the values of matrix A for ON state is matrix (4.22)and the OFF state value of A is matrix (4.33). The sampling time is the reciprocal of 100 kHz. The vector value $\boldsymbol{x_o}$ takes on the value of the measured states; vector $\boldsymbol{x_p}$ and constant vector K are calculated at every sampling time, as shown in Figure 5.2 .

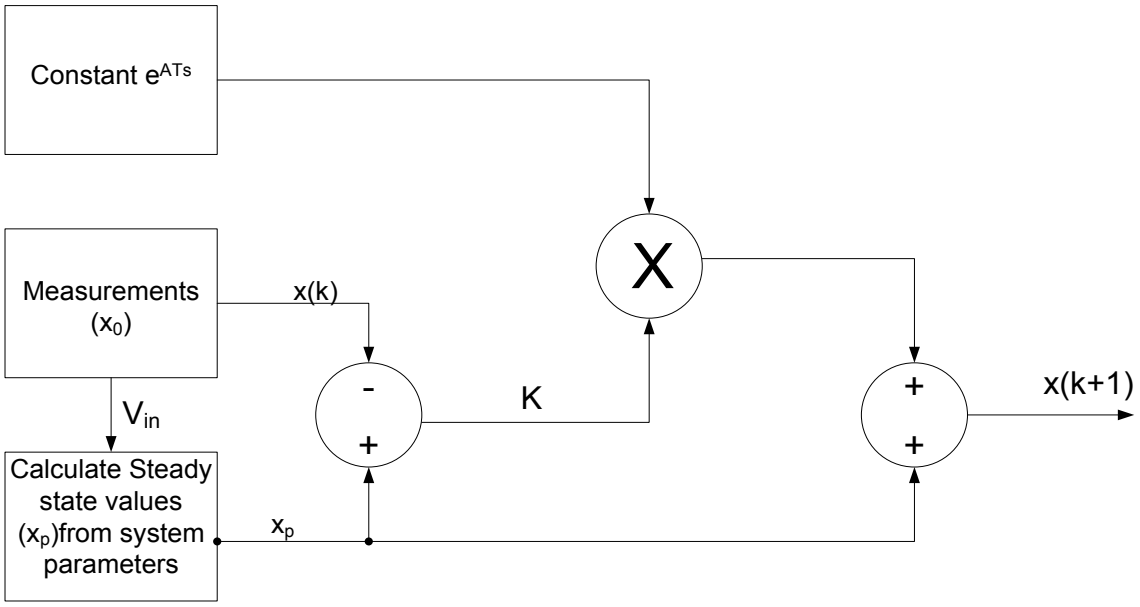


Figure 5.2 Basic diagram for prediction using exact solution

The vectors of steady state values $\boldsymbol{x_p}$ are computed at every sampling period using the input voltage v_{in} and the system parameters of the equivalent circuit for each state. The predicted values $x_{(k+1)}$ for both states are then used in the cost minimisation process. For the MVEVR controller, only the predicted output voltage v_{pred_on}, for the ON state, and v_{pred_off}, for the OFF state, are passed on to the cost minimisation.

Cost Minimisation: Cost minimisation computes the cost of a state, using several factors. In the MVEVR, the weighting coefficients used in the cost function are the voltage cost (W_v), and switching frequency weighting (W_f) and the state with minimum cost is chosen, as shown in Figure 5.3. The cost of a state is calculated as

$$J_i = W_v \left(V_{ref} - V_{pred}\right)^2 + W_f * Statecost_i \tag{5.1}$$

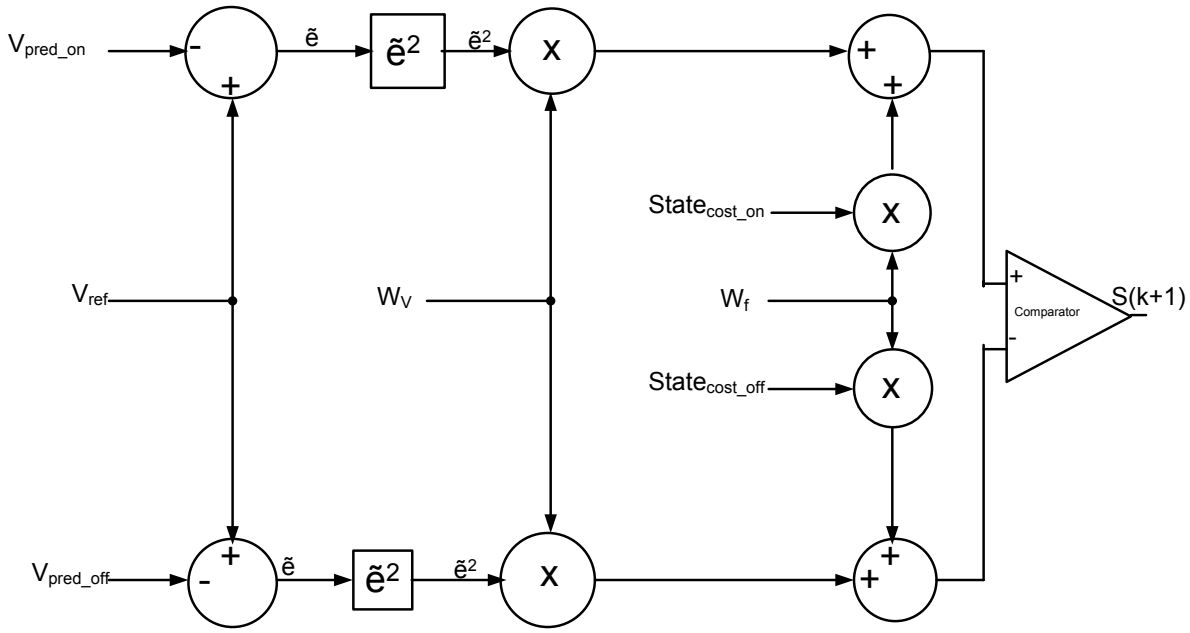


Figure 5.3 Cost minimisation process overview

In the cost minimisation function, the predicted value of voltage v(k+1) is compared to the reference voltage V_{ref} (k+1). The difference is the error $\tilde{e}$. The error is then squared. Squaring serves two purposes. The purpose is to emphasise the magnitude of the error regardless of sign. The more the predicted value deviates from the reference, the bigger the square. The squared error is multiplied to the weight coefficient assigned to the voltage error Wv. This gives the total cost of the voltage error. It is a penalty for deviating from the reference voltage. There are several ways of determining the next reference value x_{ref}(k+1).

Constant reference value: Where the reference value is constant with time, the present value is used at the next sampling period.

Time varying reference value. For time varying reference value, there are several methods that can be used.

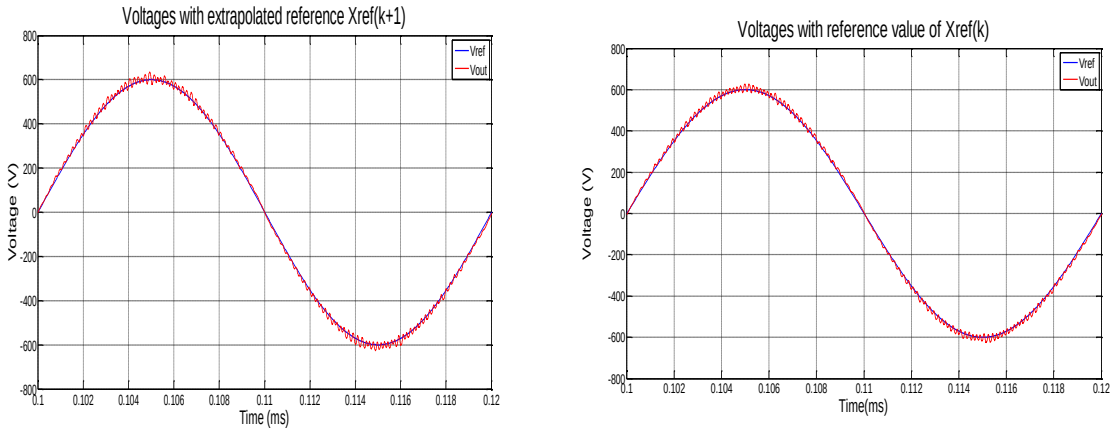
- If the function of the reference is known, the function can be calculated for k + N using the exact formula for the reference trajectory..
- For a sinusoidal wave, the reference can be advanced by extra k+N to get the reference value at N.
- Extrapolation: there are several methods of approximating the next reference value. In this research, a method that was used for extrapolation of the reference value was [63]

$$x_{ref(k+1)} = 3x_{ref(k)} - 3x_{ref(k-1)} + x_{ref(k-2)} \quad (5.2)$$

For a slowly varying reference and a high sampling rate, the difference between the present reference value $x_{ref(k)}$ and the next reference value $x_{ref(k+1)}$ is very small and therefore negligible.. In this project the reference value is a 50 Hz sinusoid. The assumption is that at a sampling rate of 100 kHz, the change in the reference value is almost zero.

$$\frac{\mathrm{d}\, x_{ref}}{dt} = 0 \tag{5.3}$$

Therefore the value of the present reference value can be used to determine the prediction error at k+1. Simulations for the reference extrapolation method in Equation (5.2) and its assumption in Equation (5.2) were done with a switching frequency of 5kHz and using system parameters in Table 5.1. .



Extrapolated Vref(k+1) b. Vref value is Vref(k)

Figure 5.4 Output voltages with extrapolated reference and with current reference value

The resulting output voltage amplitudes and THDs are similar. Therefore Equation (5.2) holds true for the project.

The second penalty is assigned to the ON state and the OFF state. A switching weighting coefficient W_f is multiplied to the cost of each state. Derivation of the state cost is explained under the switching control. For each state then, the total cost of maintaining a switching state is the sum of the voltage tracking cost and the state switching cost. The switching state with the least cost is chosen and is implemented immediately at time k to get the predicted value at k+1.

5.4 Simulation Results for MVEVR

Simulations for the MVEVR and synchronous buck converter were carried out with the component values in Table 5.1 and Table 5.2 respectively.

Table 5.1 Component Values for MVEVR simulation

Component	Value	Unit
L_{eq}	1.01	mH
R_{Leq}	0.003	Ω
C_b	90	μF
R_{Cb}	0.0015	Ω
L_o	0.53	mH
R_{Lo}	0.003	Ω
C_o	75	μF
R_{Co}	0.0015	Ω
Load	30	Ω
Vin	1500, 800	V
Vout	600	V

The simulations were carried out with Vin at 1500 unless otherwise stated.

Table 5.2 Simulation values for synchronous buck converter

Component	Value	Unit
L_o	1	mH
R_{Lo}	0.003	Ω
C_o	30	μF
R_{Co}	0.0015	Ω
V_{in}	30	V
V_{out}	20	V
Load Impedance	6	Ω

Switching frequency weighting coefficiennt. (Wf)

In FS-MPC, the switching frequency is usually much less than half the sampling frequency if no switching restrictions are imposed on the control as shown in Figure 5.5 and Figure 5.6. The MVEVR was simulated with W_v set to 1 and W_f set to 0. Figure 5.5 shows the resulting output voltage at a sampling frequency of 10 kHz while Figure 5.6 shows the output voltage at a sampling frequency of 100 kHz.

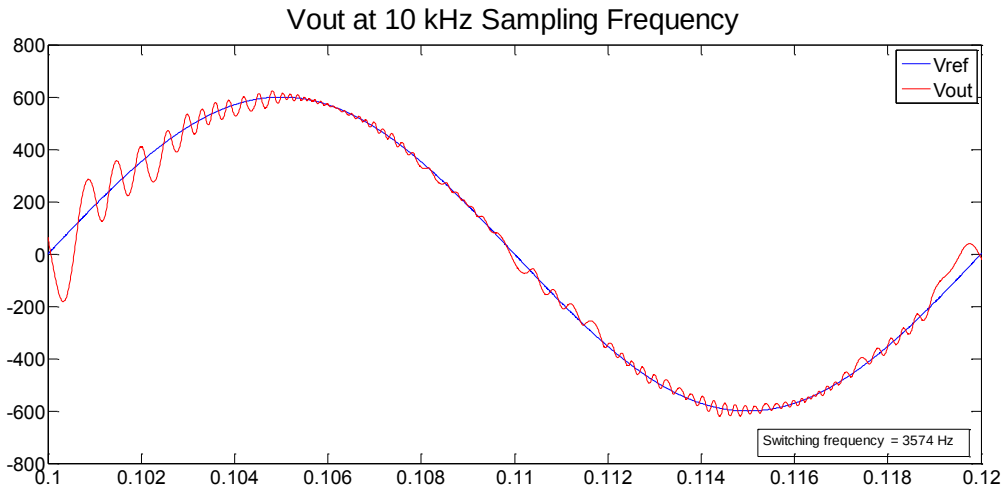


Figure 5.5 Voltage output at 10 kHz sampling frequency

The average switching frequency is 3.574 kHz which is less than half of the sampling frequency.

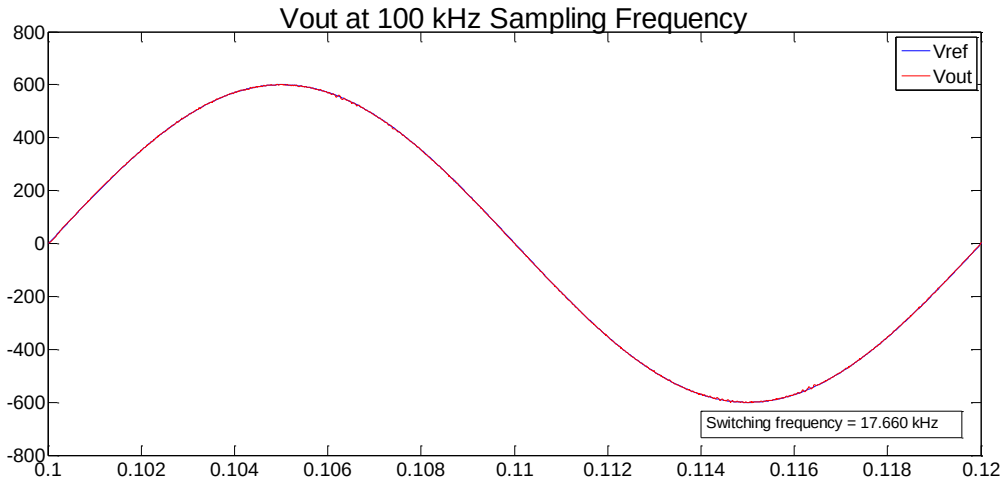


Figure 5.6 Output voltage at 100 kHz sampling frequency

With the sampling frequency of 100 kHz the average switching frequency is 17 kHz. The maximum switching frequency can be as high as 50 kHz if there is a change of state at every

sampling time. The switching frequency is normally less than or about a third of the sampling frequency.

When the switching frequency is too high, losses in the switches are high which lead to heating of the semiconductors and subsequent damage. When the switching frequency is too low, the output voltage distortion is high and has a lot of low frequency harmonics, as in Figure 5.5, and low frequency harmonics require bigger filter capacitors and inductors. FS-MPC has shown that the switching frequency varies between the high and the low extremes, which could lead to circuit resonances. Figure 5.7 shows the output voltage at 2 kHz, 5 kHz and 9.7 kHz.

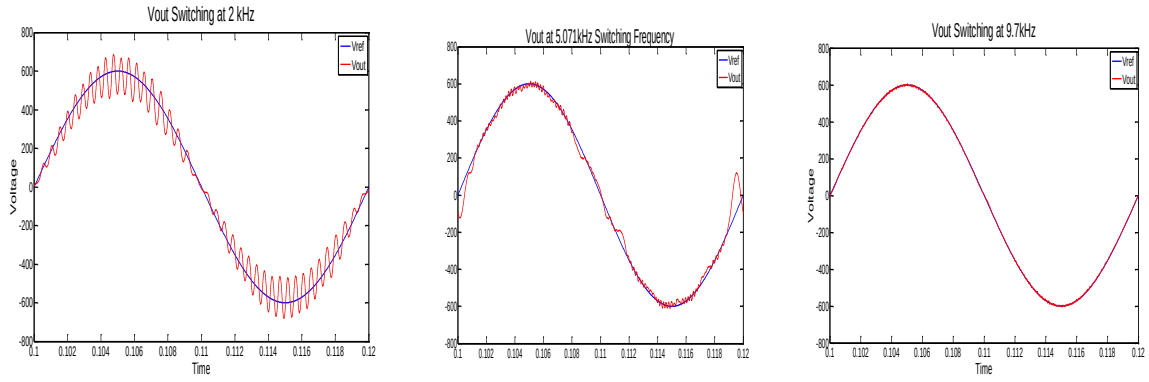


Figure 5.7 Voltages at different switching frequencies

The solution is then to sample at a much higher frequency and switch around the optimum switching frequency for the power semiconductor switches. For this research, a sampling frequency was chosen at 100 kHz, while the average switching frequency of each power semiconductor switch was controlled to approximately 10 kHz.

A schematic diagram of the switching frequency control cost for each state that was implemented is shown in Figure 5.8 below.

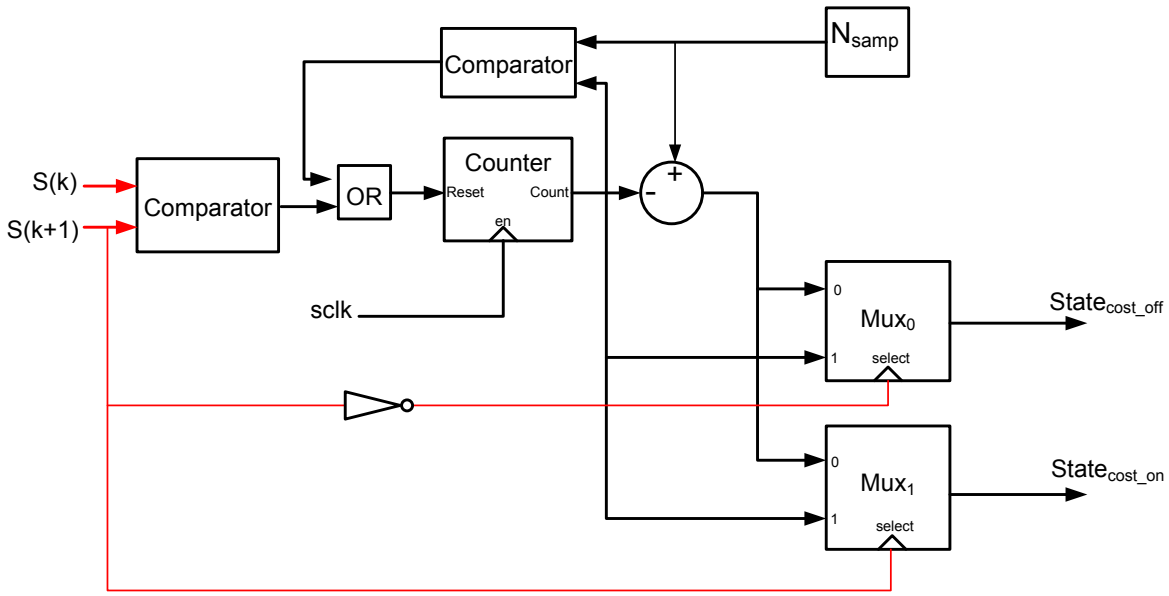


Figure 5.8. Switching frequency control cost schematic

The next state S(k+1) (result from the cost minimization function) is compared to the present switch state S(k). If S(k+1) is equal to S(k) the result from the comparator will be 0. If the two values are different, then the comparator outputs a 1 to show that there is a change of state. A change of state will reset the counter. The counter increments by one at every sampling time by the sampling clock sclk. The counter value 'count' is compared to a value $N_{samp.}$. When the counter value reaches the value of Nsamp, it causes the comparator to output a 1 which resets the counter. N_{samp} is the oversampling factor calculated by dividing the sampling frequency by the required switching frequency of each power semiconductor switch.

$$N_{samp} = \frac{f_s}{f_{sw}} \tag{5.4}$$

where Nsamp is the sampling factor, f_s is the sampling frequency and f_{sw} is the switching frequency. The counter counts the number of times a state has been active.

$$State_{cost1} = count \tag{5.5}$$

subtracting the counter value from the sampling factor

$$State_{cost2} = N_{samp} - count \tag{5.6}$$

The state cost for the active state is $State_{cost1}$ while the other state gets the $State_{cost2}$ as its cost of state. The Multiplexer Mux_0 will always output the state cost for OFF state and Mux_1

will always output the state cost for ON state. When S(k+1) is '1'(ON state), select for Mux_0 is inverted to 0 and $State_{cost2}$ is passed through to the cost function while Mux_1 will pass $State_{cost1}$ to the cost minimisation function. When S(k + 1) is 0 (OFF state) then select for Mux_0 inverts it to a 1 and $State_{cost1}$ is passed to the cost function and Mux_1 will pass $State_{cost2}$ to the cost function.

Figure 5.9 is a plot of the values for a 100 kHz sampling frequency and 10 kHz switching frequency.

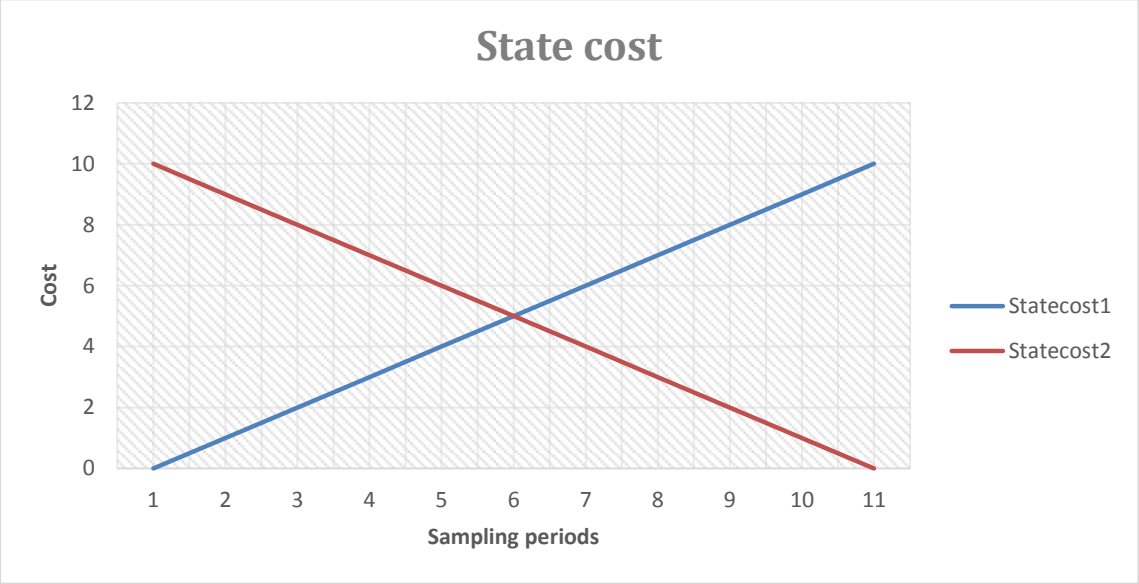


Figure 5.9 State cost for switching factor of N=10

When a state becomes active, its state cost is zero, while the state cost for the other state is 10. The advantage of this is that at the next sampling period, the total state cost of the new active state is reduced, thereby preventing an immediate change of state. The state cost of the active state increases with the increasing number of sampling periods that the state has been active, while the idle state cost decreases with the increasing number of sampling periods for which the state has been idle. After a certain number of sampling periods of no state change, the cost of the idle state becomes lower than the cost of the active state. This favours the idle state becoming active. The values of the state cost can be squared or multiplied by other factors to alter the shape of the plot and change sensitivity to switching costs according to requirements. It does not have to be linear. In the practical tests for this research, the first four sampling slots were completely blanked out to prevent any switching of the switches as in Figure 5.10. No blanking was done in the simulation tests.

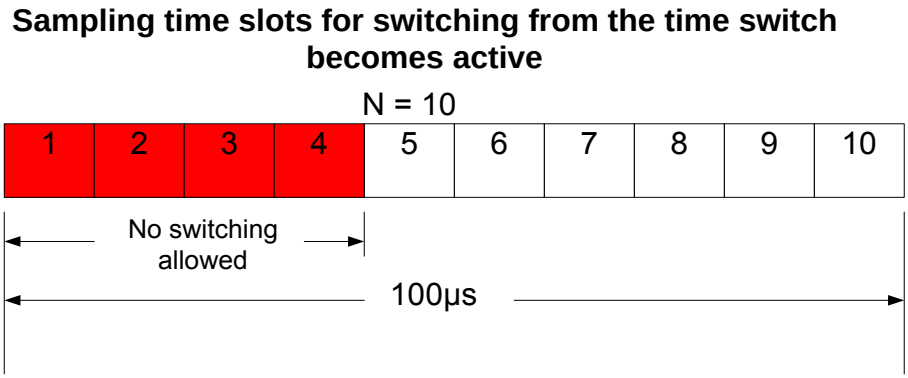
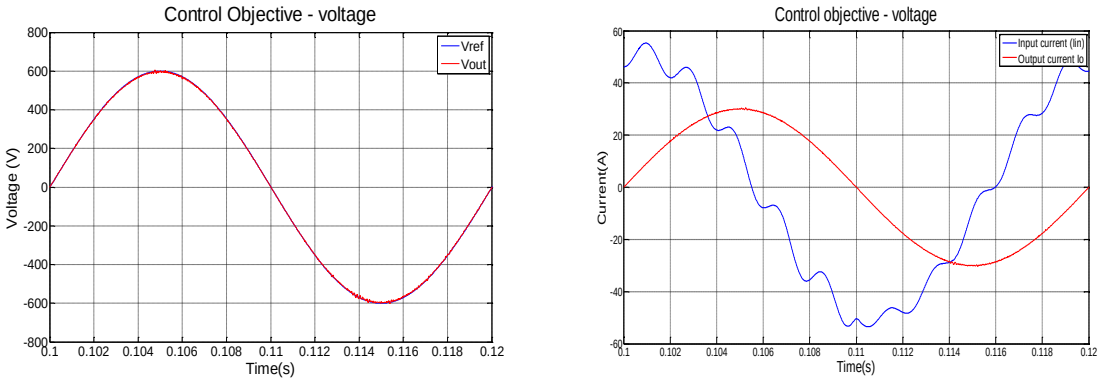


Figure 5.10 Sampling time slots with slots 1-4 blanked out

The final cost function (J), for each state, therefore, becomes a function of the squared voltage output error and switching state as

$$J_i = W_v(Vref - Vpred_i)^2 + W_f * statecost_i \quad (5.7)$$

Figure 5.11 and Figure 5.12 show the result of setting the switching frequency cost ($OS_{cost} * State_{cost}$) to 0 and setting the switching frequency as the primary control objective respectively. The simulation was done with a simulated supply at 1500 V and reference voltage (Vref) at 600 V.



a. voltages *b*. currents

Figure 5.11 Switching without frequency control

The output voltage tracks the voltage accurately enough at a switching frequency of about 18.3 kHz. This switching frequency is too high for the IGBTs. The higher the switching frequency, the lower the total harmonic distortion will be. The Simulink FFT for Figure 5.11 is shown in Figure 5.12 below.

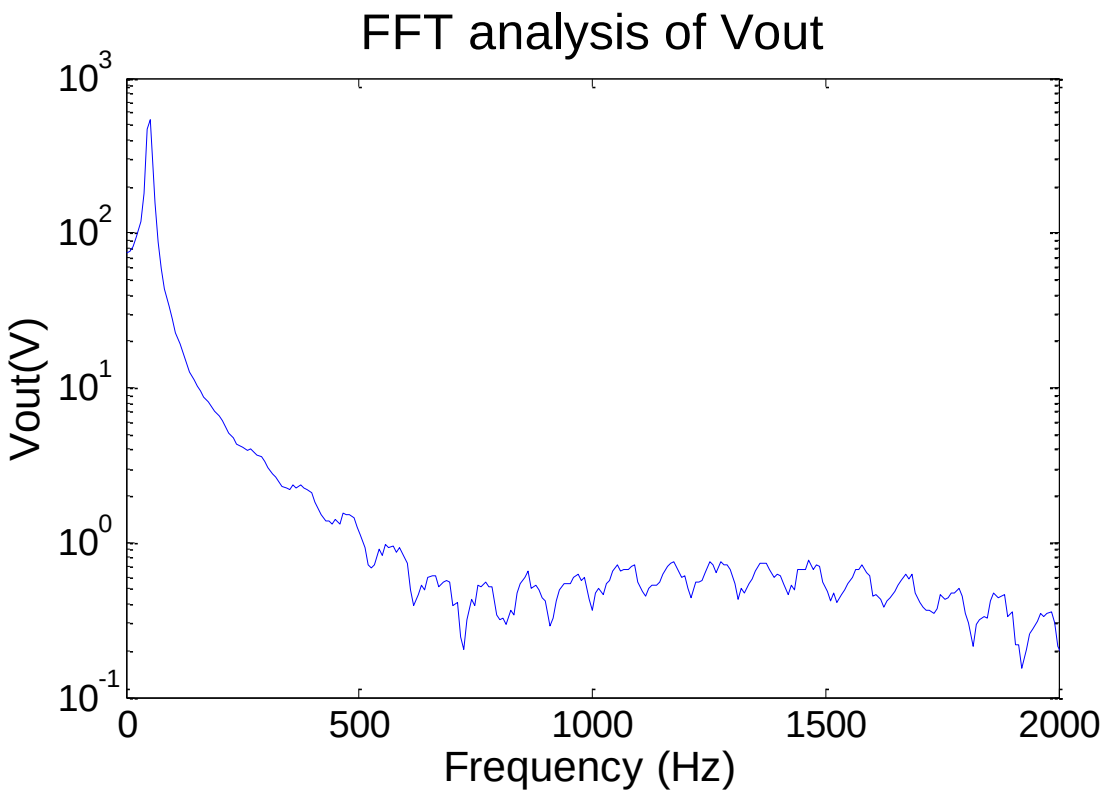
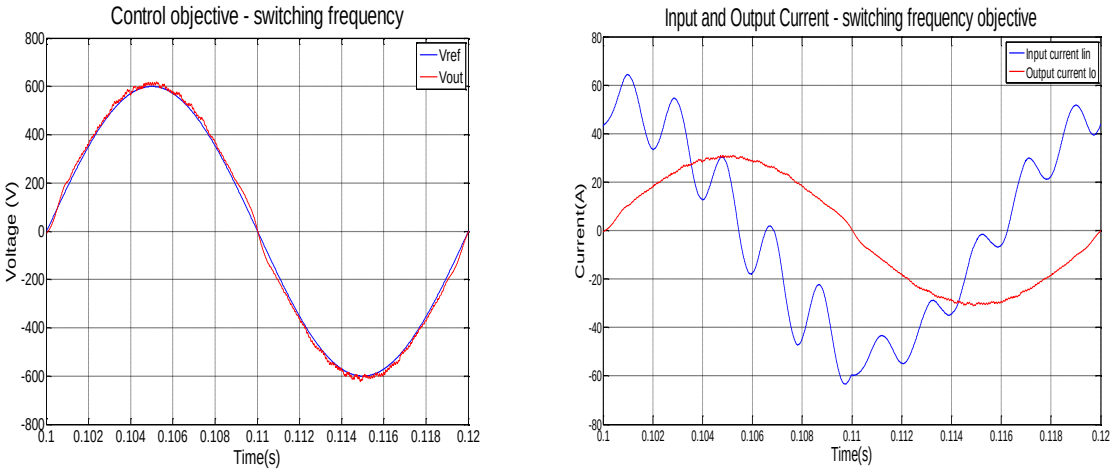


Figure 5.12 FFT Analysis of output voltage Vout

The THD for the output voltage is 0.16% and the voltage amplitude tracking error is 0.55% at a switching frequency of about 18.3 kHz.

A simulation to switch as close to 10 kHz as possible (switching frequency objective) was also done with the same conditions as for the voltage objective. The results are shown below in Figure 5.13



a. voltages *b*. currents

Figure 5.13 Control with switching frequency being the primary objective

The Simulink FFT analysis for the output voltage was taken for frequencies up to the 40th harmonic of the 50Hz supply frequency. The results are shown below in Figure 5.14

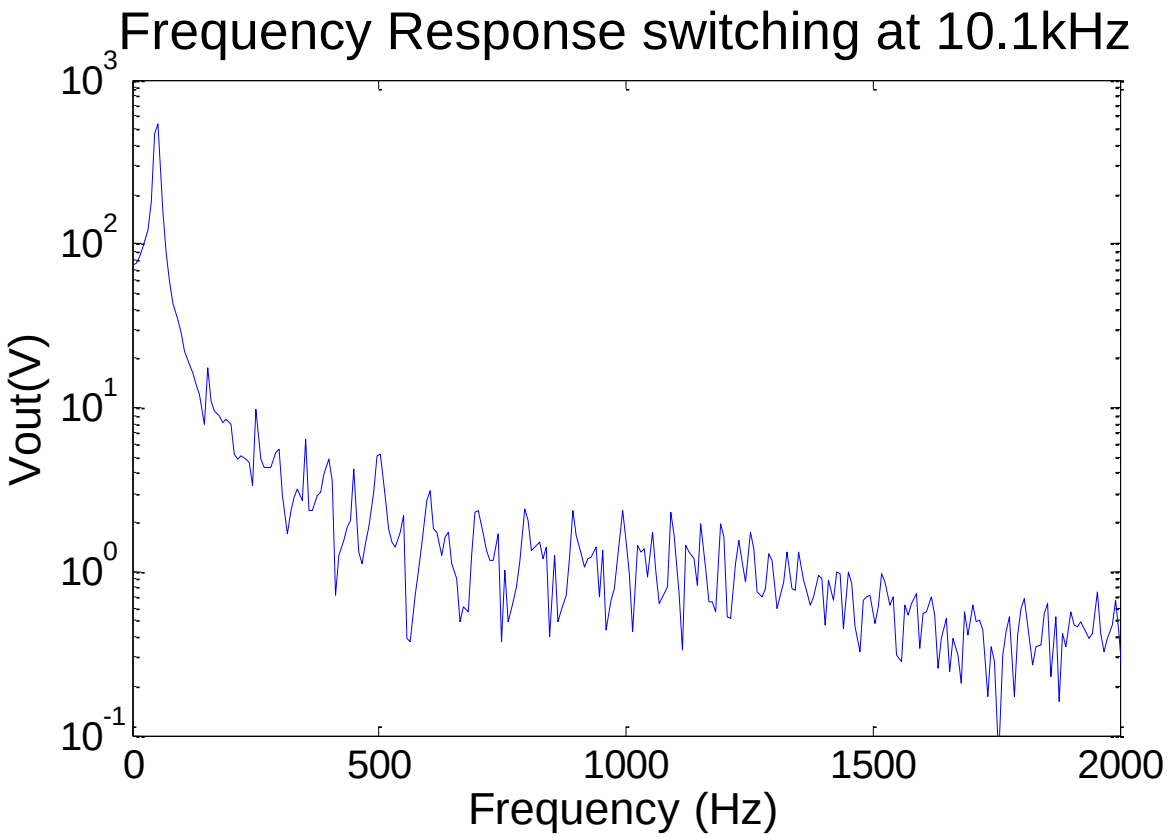
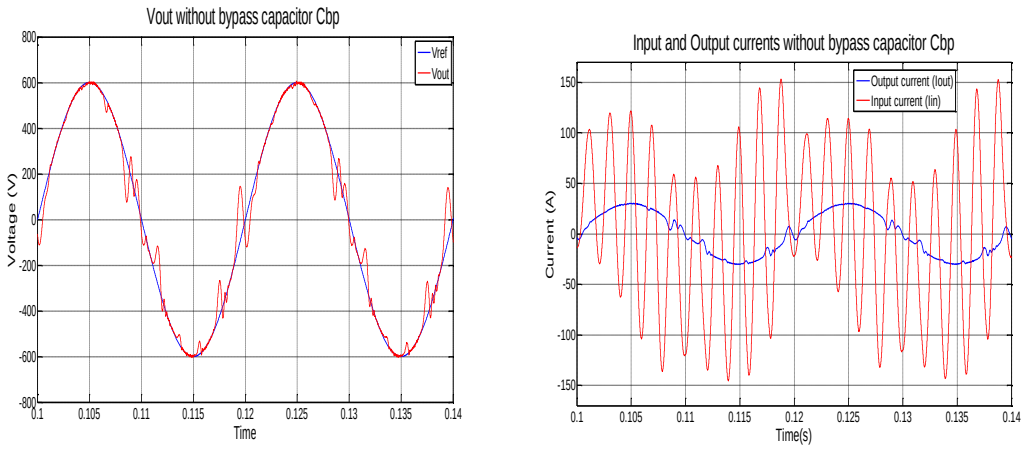


Figure 5.14 FFT analysis of Vout for switching frequency objective

The output voltage THD is now 2.51% and the voltage amplitude tracking error is at 2.8% switching at a frequency of 10.1 kHz. This output performance is still within the NRS-048-2 standard.

All the above simulations were carried out with a simulated input voltage of 1500 V and output voltage set to 600 V. At this output voltage, there was slight ringing in the input voltage. When the simulated input voltage was lowered to 800 V, there were kinks in the output voltage, especially at or near the zero crossing. There were large oscillations in input current as shown in Figure 5.15 *a* and *b*.



a. Voltage response *b*. Current response

Figure 5.15 Voltages and currents with Vin set to 800 V

FFT Analysis for the voltages and currents show that the tenth harmonic (around 500 Hz) is the culprit, as shown in Figure 5.16. This happens to be very close to the input resonance frequency of 527 Hz for L_{eq} and C_{bus} as calculated earlier in Equation 4.5.

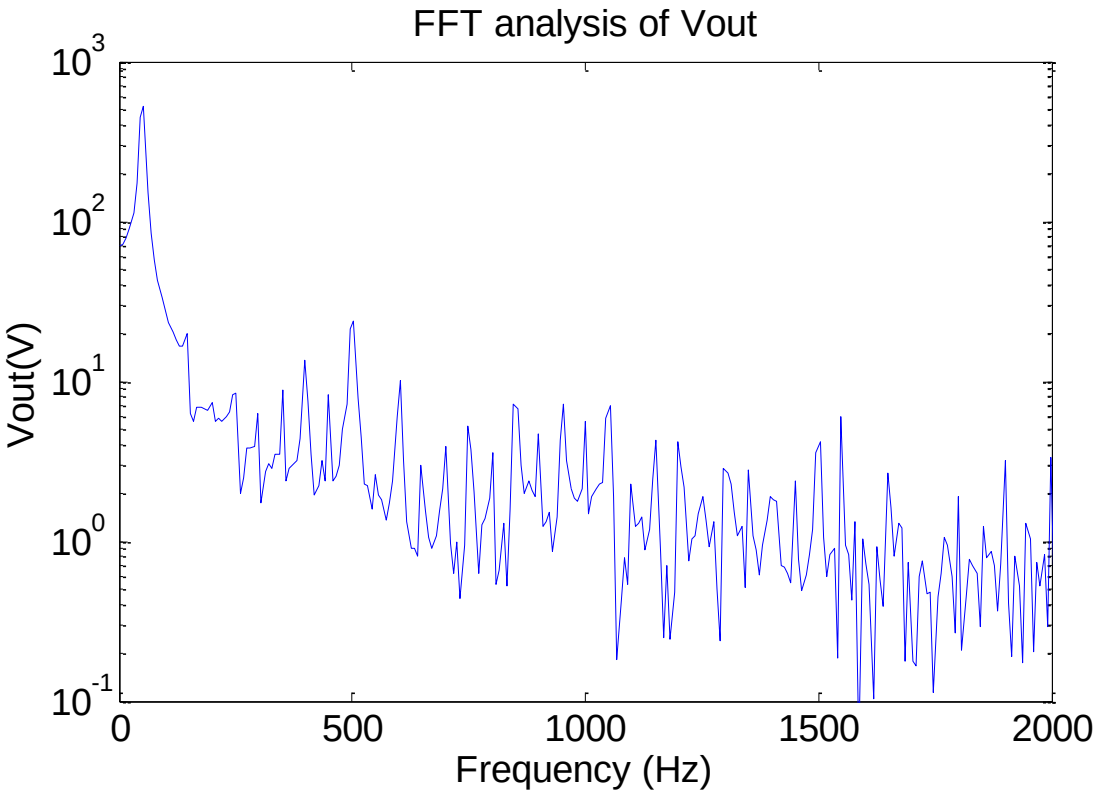


Figure 5.16 FFT analysis with Vin set at 800 V

Several solutions to the problem were explored. Two solutions were suggested. The next section discusses the solutions and their practical applications.

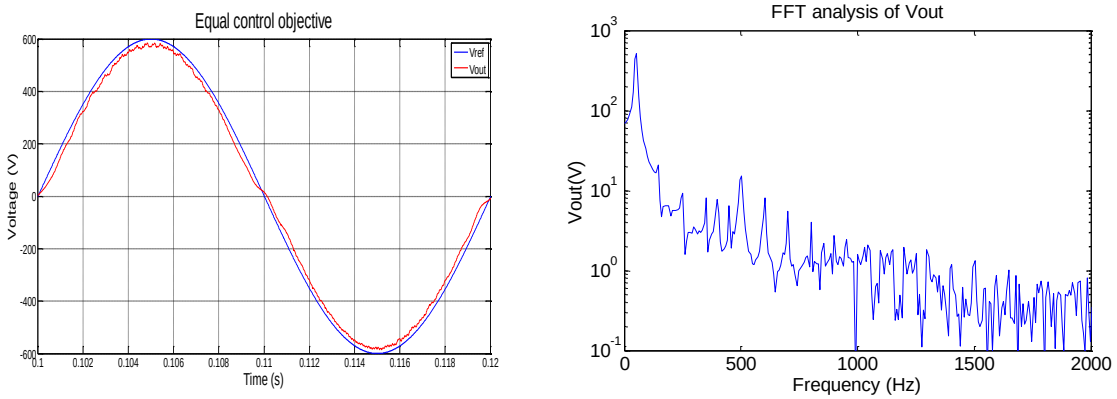
5.4.1 Solutions to input current oscillations

Two solutions were suggested for overcoming the input current oscillations.

A. Setting correct control objective

Under normal circumstances, the primary control objective is to minimise the output voltage error and the secondary objective is for the switching frequency of each IGBT to be less than 10 kHz. But with the MVEVR, simulation has shown that to prevent input current oscillations,

the IGBT switching frequency has to be high enough without damaging the IGBTs. The controller needs to have both the voltage and the switching frequency as primary objective as shown in Figure 5.17 *a* and *b*.



a. Voltage profile *b.* FFT Analysis

Figure 5.17 Voltage and FFT analysis for equal control objective

The advantage of this method is that the THD has now decreased from 13.6% to 3.72%. The third harmonic at 150Hz is now the major problem contributing about 3% to the output voltage THD. This is still within the NERSA specifications of a maximum of 5% for the third harmonic and maximum sum of 8% from 0 up to the 40th harmonic (2000 Hz). The disadvantage is on the voltage regulation. The voltage error is now 5.32% which is slightly over the limit. Considering that the MVEVR is operated as modules in a boost configuration this should pose no problem to the overall setup.

5.5 Synchronous buck converter Simulation

Several simulations were carried out on a synchronous buck converter to test the controller.

5.5.1 DC-to-DC simulation

A DC to DC test was carried out to determine the response of the controller and for comparison with actual test results.

The first simulation was done with the reference voltage set at 2 V DC. The voltage output is shown in Figure 5.18. At 2V, the switching frequency was 2.2 kHz.

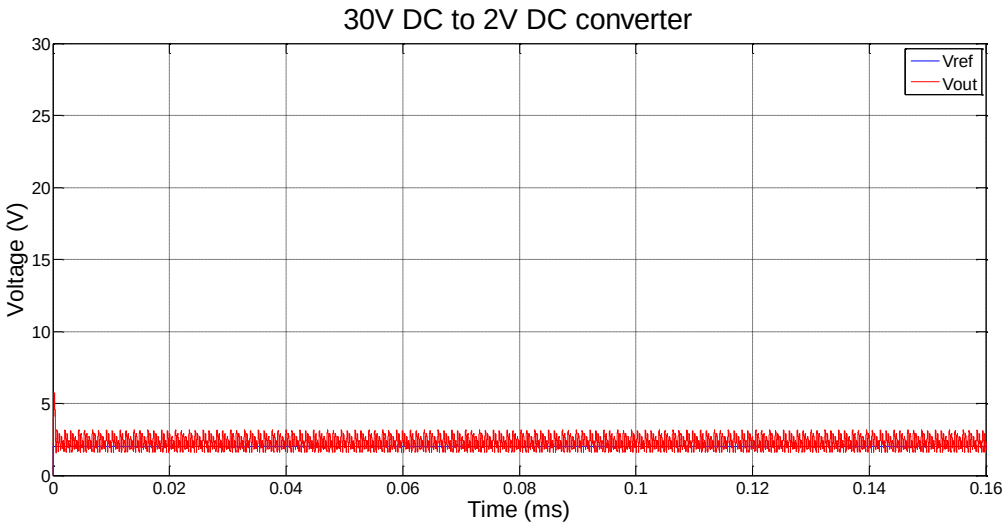


Figure 5.18 Conversion from 30 V DC to 2V DC with minimal switching frequency control

Increasing the emphasis on frequency control had undesirable results (the voltage error increases) as shown in Figure 5.19 below. It can be noted that at lower voltage the average output voltage is slightly higher than the reference.

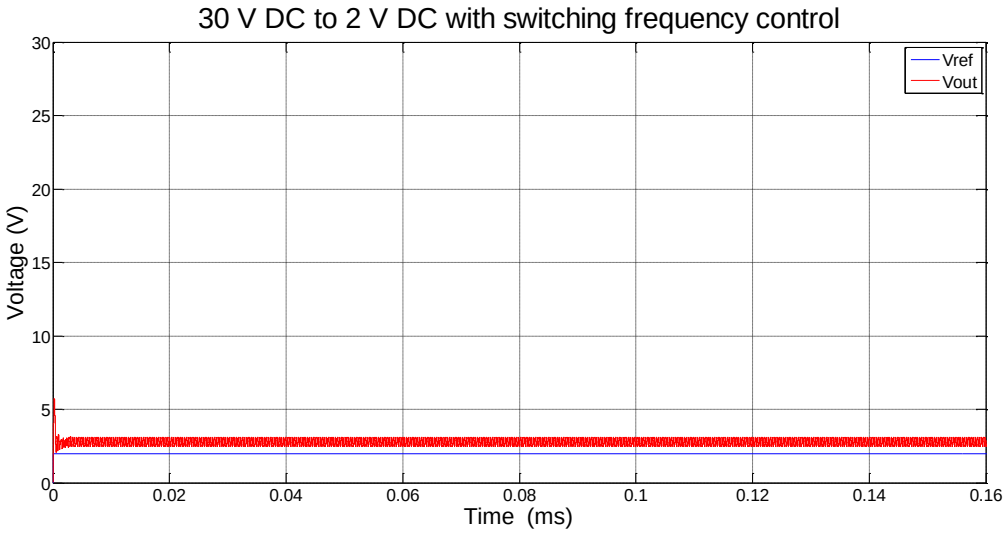


Figure 5.19 Conversion from 30V to 2 V with switching frequency control

The more emphasis that is put on the switching frequency, the bigger the error.

The second DC-to-DC simulation, the reference voltage was set to 25 V. The voltage output is as shown in Figure 5.20.

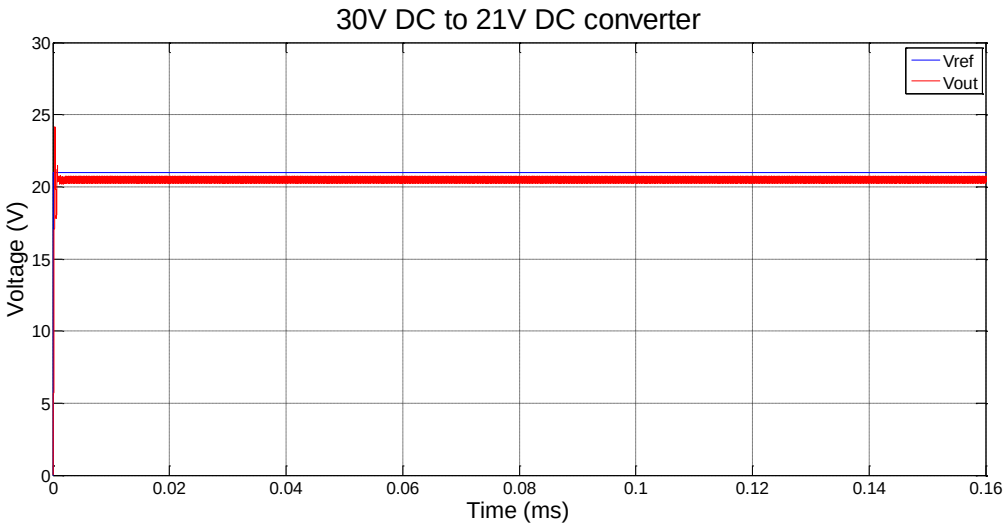


Figure 5.20 Output voltage with reference voltage set to 21 V

The switching frequency automatically increased to 6.2 kHz and the output voltage was slightly smaller than the reference voltage. Increasing the switching frequency increased the output voltage error.

5.5.2 DC to AC simulation

A DC-to-AC simulation test was run on the system. The voltage output is shown in Figure 5.21 below. The reference voltage was set to 10 V amplitude.

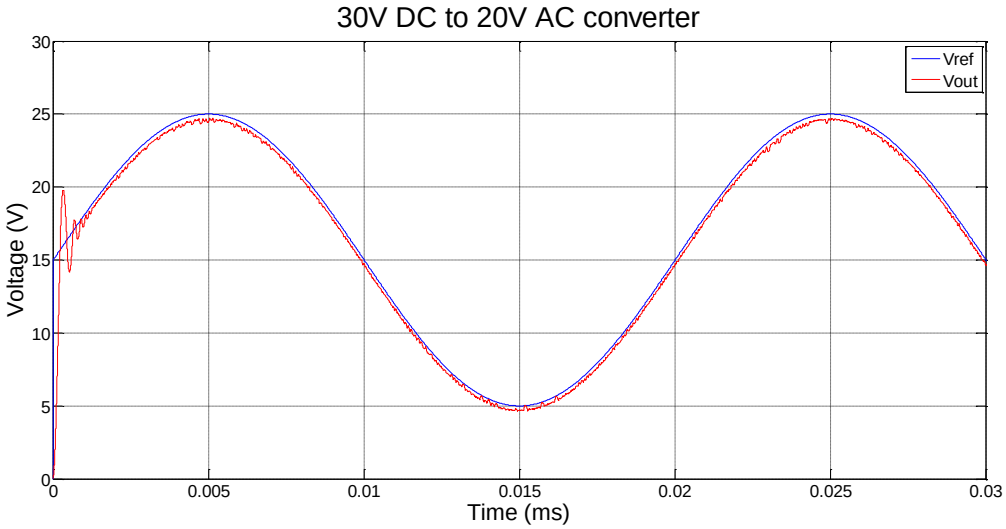


Figure 5.21 DC to AC voltage converter

The switching frequency was 7.3 kHz.

5.6 Summary

In this chapter, the controller requirements were outlined. The controller design and schematic was presented. The same controller was used for the simulation of both the MVEVR and the synchronous buck converter by changing the state matrices. The simulation results showed that FS-MPC is a viable solution for the MVEVR.

The switching frequency control was shown to be very important for proper operation of the MVEVR and synchronous buck converter. The switching frequency could be tuned to any frequency within the lower half of the sampling frequency.

Simulation results have shown that for the MVEVR, the input current is distorted when the input and reference voltages are very close. Two solutions which have effectively reduced the problem, have been suggested and tested.

The next chapter will show how the controller was implemented in a practical system.

CHAPTER 6
FPGA IMPLMENTATION OF THE CONTROLLER

6.1 INTRODUCTION

This chapter will discuss how the controller was implemented in the FPGA using VHDL. It will show how existing controller board software developed by other research students for the research lab was used to interface with the control algorithm to control the synchronous buck converter.

The control algorithm was primarily developed for the control of the MVEVR. Due to the unavailability of the MVEVR at the time the controller was completed, the controller was then adapted for the synchronous buck converter for testing purposes. The reason for testing the synchronous buck converter was because it operates on the same principles of the MVEVR converter. Therefore, if the controller could work on the buck converter then it could also work on the MVEVR.

6.2 THE ALTERA CYCLONE III BASED FPGA CONTROLLER

The University of Stellenbosch power electronics lab has over the years, developed a control board based on the Altera Cyclone III FPGA and the also the main program for the board and other necessary interface software for measurements and switching sequence for IGBTs. Much regarding the hardware and the software of the board has been discussed in Chapter 3.

Other researchers have already implemented the ADC interface for measurements and the gating manager to interface with the IGBTs. The ADC interface and the gating manager are controlled by the main program. The requirement of the present researcher was then to develop the controller program and interface it with the main program, as shown in Figure 6.1.

The Cyclone III FPGA used has many features that that were used in this design such as [34]:

- **Many Input-output banks.** There are eight input-output banks , each with four input/outputs and support for single ended differential standards
- **Large number of global clock networks and PLLs**. There are 20global clock networks and four PLLs
- **Embedded multiplier blocks.** The FPGA has 288 embedded multiplier blocks which can be configured as 18x18-bit or 9x9-bit multipliers
- **DSP IP cores**

- **JTAG BST Capabilities.** The cyclone's Joint Test Action Group (JTAG) boundary scan testing (BST) was used in the design and testing.

6.3 IMPLEMENTATION OF THE CONTROLLER

Quartus II version 11.0 was used for programming the FPGA in VHDL. Figure 6.1 shows the schematic interaction for the controller in the FPGA.

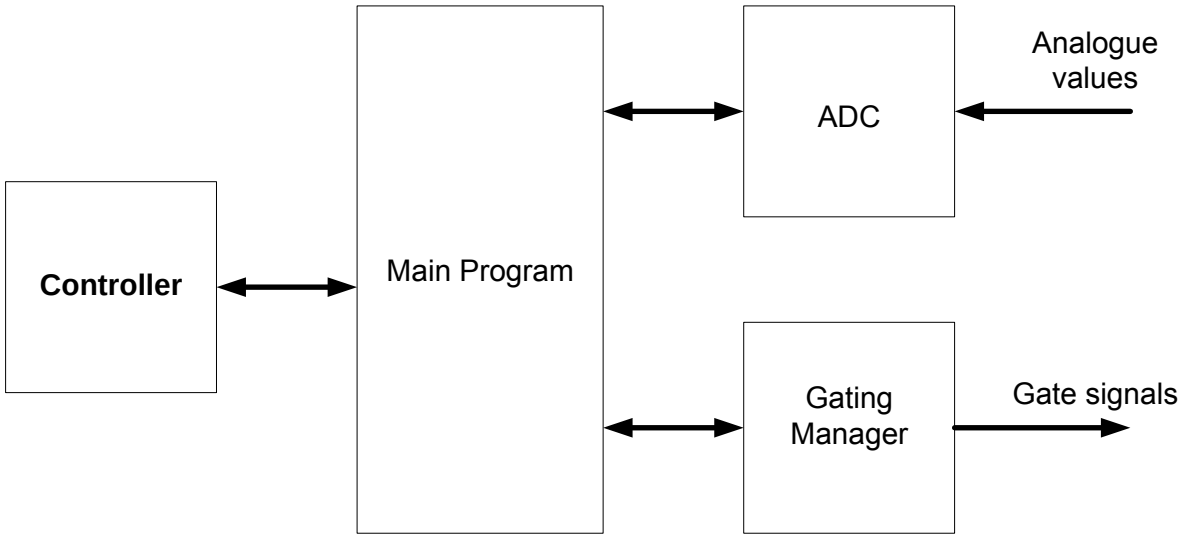


Figure 6.1 Schematic for the controller interface in the FPGA

The main program is responsible for interfacing with the ADC for all the system measurements and also interfaces with the gating manager for all the signals to and from the IGBT switches. The controller interfaces with the main program to get clock signal, measurements of state variables and to send the switch command to the IGBTs. The functions of the ADC and gating manager have been discussed in Chapter 3. The controller gets its measurements from the main program, and uses these measurements in the control algorithm, sending the required state to be implemented to the main program, regardless of the input voltage polarity. The required state can either be ON or OFF. The main program will send the control command to the gating manager which, in turn, decides which IGBTs to switch on or switch off depending on the voltage polarity and control command signal.

The board's main clock runs at 20 MHz and the controller was set to the same clock. Since the sampling frequency was set at 100 kHz, a division by 200 was used for the control cycle.

The prediction using the exact discretisation method as in Equation (4.56) was used for the control algorithm. The controller was then programmed as a finite state machine with each

state using only one clock cycle. Calculation of the control algorithm was broken down in VHDL in the following steps

1. Get measurements as **x**(k) vector. This vector becomes x(0) and calculate the particular solution vector $\mathbf{x}_p$ from Vin and system parameters
2. Calculate the value of vector **K**
3. Calculate the value of predicted vector $e^{ATs}*K + x_p$ for each state. The matrix e^{ATs} for each state, is calculated in advance offline.
4. Calculate the cost function for each state using the weighting coefficients for the control objectives given and implement the control action.
5. Calculate the cost factor required to achieve the given switching frequency for each state. This cost factor for each state will be used in the cost function at the next sampling period to determine the total cost.

A wait state was inserted into the state machine to achieve a 10 µs clock cycle for each complete process as shown in Figure 6.2. Changing the duration of the wait period, changes the sampling time and, at the same time, changes the switching frequency. It was also possible to change the switching frequency without changing the sampling frequency, by simply altering the oversampling factor in the allocation of the state switching cost in step 6.

Each part of the VHDL code was tested separately, using ModelSim VHDL simulation software to check timing. The simulation result for state cost allocation for switching frequency is shown in Figure 6.3. Notice that the cost of each state (On_OSfactor for ON state and Off_OSfactor for OFF state) changes at each clock cycle.

To reduce the burden of calculations for the prediction, only those elements in the prediction matrix which affect the output voltage were used. Prediction of input and output currents and bus voltages were ignored as they were not used in the cost function.

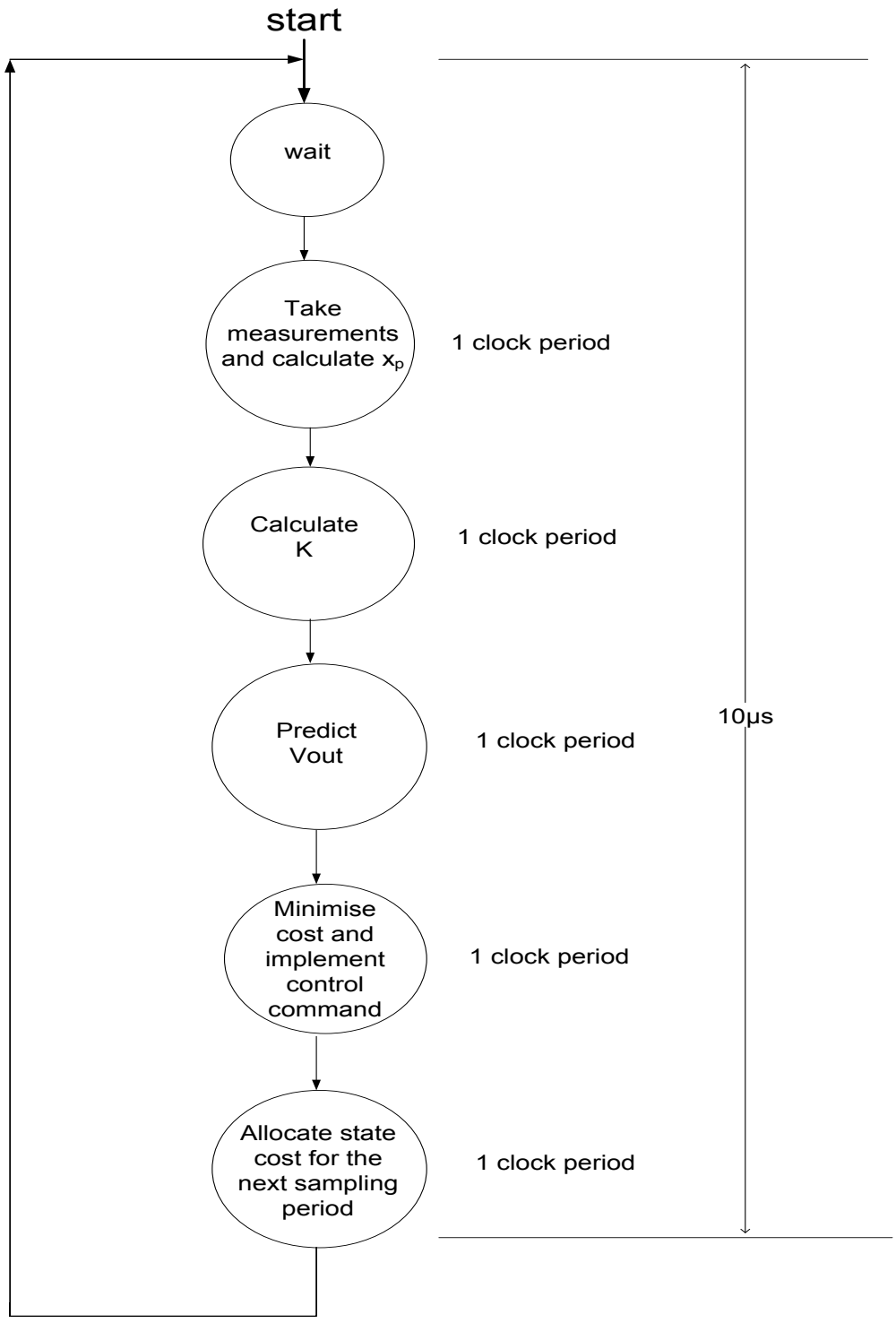


Figure 6.2 The controller finite state machine

The cost assignment to the switch state algorithm was tested as shown in Figure 6.3. The VHDL code for the cost assignment is in Appendix B

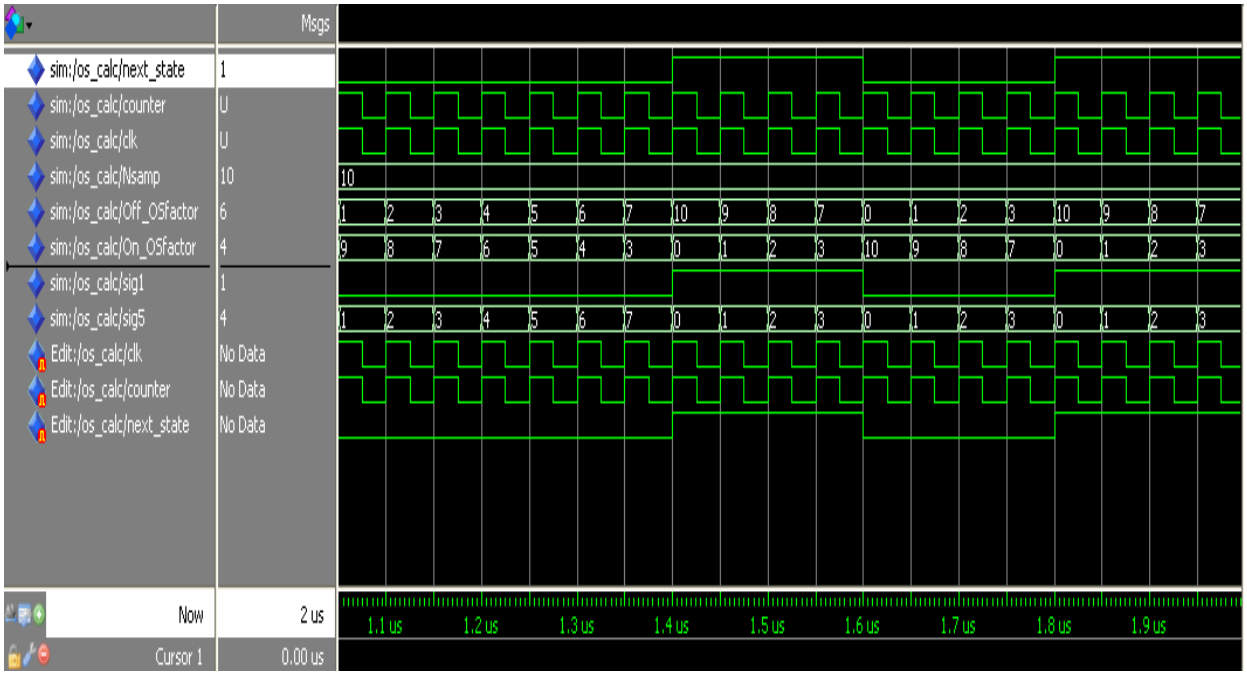


Figure 6.3 Switch state cost assignment

The value of the switch state cost changed at every rising clock edge depending on the previous switch state. The switch state cost is used in the next sampling period for the total cost evaluation of the switch state. In Figure 6.3, the state cost factor for the switch that is off is Off_Statecost while the cost for the switch that is on is On_Statecost. The next_state represents the state that is being implemented now. Every time next_state changes, the values of the Off_Statecost and On_Statecost reset accordingly. The value of the cost factor for the switch that is in a similar state as next_state, counts up by one at every rising edge of clock while the value of the switch that is dissimilar to the next_state counts down by one at every rising edge of clock. If the state of next_state is 1 then the switch that is on will take the switch state factor On_Statecost state and the other switch will take the Off_Statecost. If the state of next_state is 0 then the switch that is off will take on the value of the Off_Statecost and the switch that is on will take on the value of the On_Statecost.

6.4 SUMMARY

This chapter has discussed the Altera Cyclone II FPGA based controller:

- Some features used were outlined
- How the controller was implemented was explained
- An example of one of the component parts of the controller was presented with its Modelsim VHDL simulation results

CHAPTER 7
RESULTS AND DISCUSSION

7.1 INTRODUCTION

FS-MPC with switching frequency control was successfully implemented in SIMULINK-MATLAB simulations of the MVEVR and synchronous converter in the last chapter. This chapter will discuss the results obtained in the simulations and compare them with practical results obtained by applying the FS-MPC and switching frequency control on the real plant.

The test was carried out only on a synchronous buck converter, because work was being done on the MVEVR. FS-MPC had previously been carried on the MVEVR by in [44] with FS-MPC, but using a different switching frequency control technique. The results and discussion will, therefore, concentrate on the new switching frequency control used in this research and its effect on the output voltage.

7.2 THE SYNCHRONOUS BUCK CONVERTER

The test setup was done with the synchronous buck converter with component values as shown in Table 7.1.

Table 7.1 Synchronous buck converter component values

Component	Value	Unit
L_o	1	mH
C_o	30	µF
V_{in}	30	V
V_{out}	20,5	V
Load Impedance	60	Ω

The input voltage V_{in} and the output voltages were limited to 30 V and 20 V respectively because of voltage source load limitations. The voltages were adequate to show the effectiveness of the controller.

Figure 7.1 shows the layout of the synchronous buck converter used in the test of the controller. The system was set up to mimic the MVEVR. MOS1 and MOS4 were always switched on while MOS2 and MOS3 are switched in a complementary manner. Switching frequency control was carried out on all tests with sampling frequency at 100 kHz to prevent the switches from operating at frequencies above 10 kHz. The nature of the circuit is that the output voltage and current have to operate at a certain DC bias.

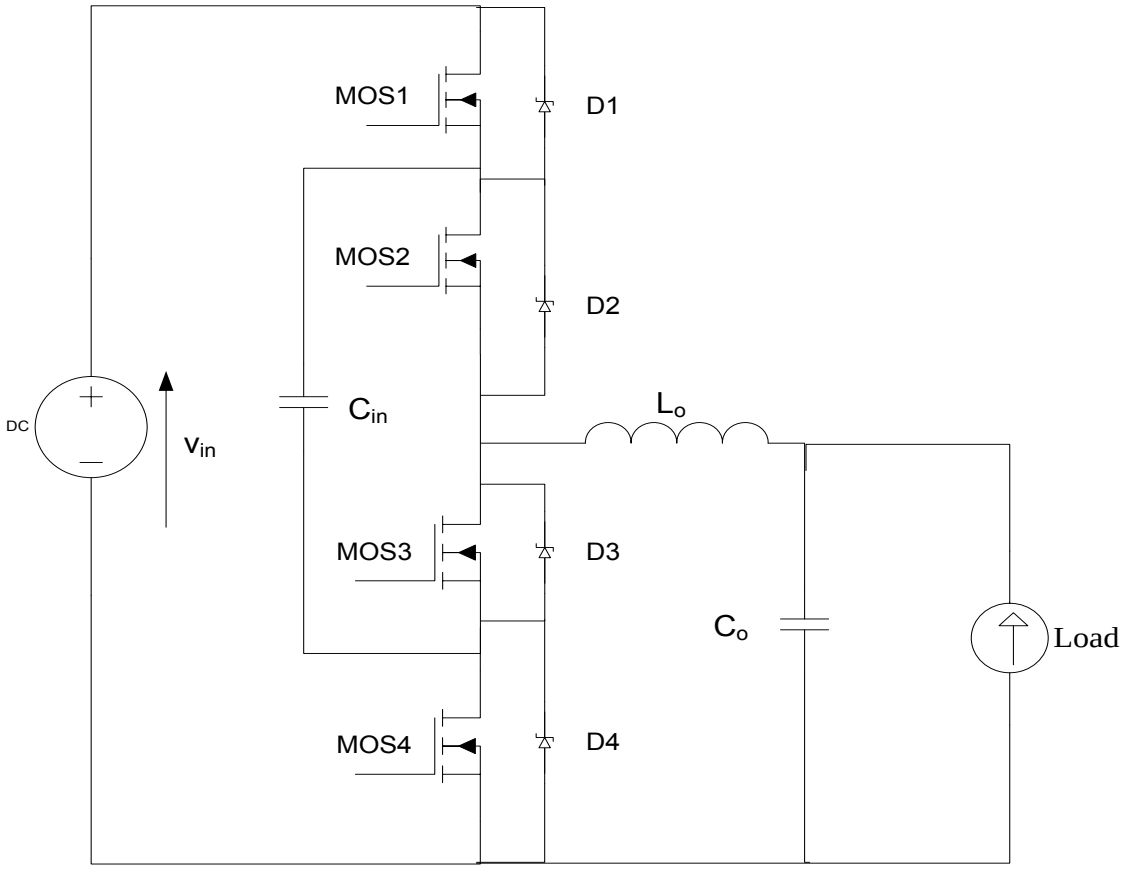


Figure 7.1 The synchronous buck converter layout for the practical tests

.

A photo of the synchronous buck converter is shown in Figure 7.2 below. The system setup comprises the controller board, measurement board, the MOSFET board and the MOSFET driver board. Two 15 μF capacitors are connected in parallel, there is a filter inductor and a variable load resistance with a maximum resistance of 66 Ω. Signals from the controller board are sent to the Mosfet board through optical cables, as shown in Figure 7.3. Optical cables are used to isolate the control board from dangerous high voltages in the MOSFET board. The measurement board is also fitted with optical isolators to isolate the control board.

Several tests were carried out on the synchronous buck converter. The tests carried out were the DC to DC conversion and DC to AC conversion, using the controller designed in Chapter 5. The reference voltage was generated by the control board software.

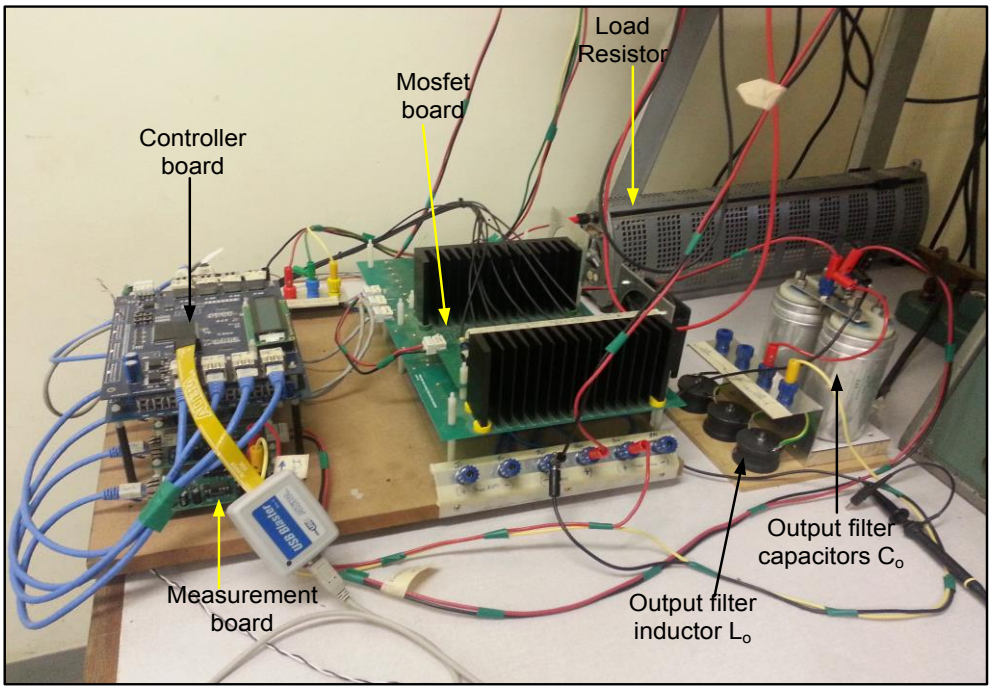


Figure 7.2 A photo of the synchronous buck converter of the system developed by Daniel du Toit and used for the practical test

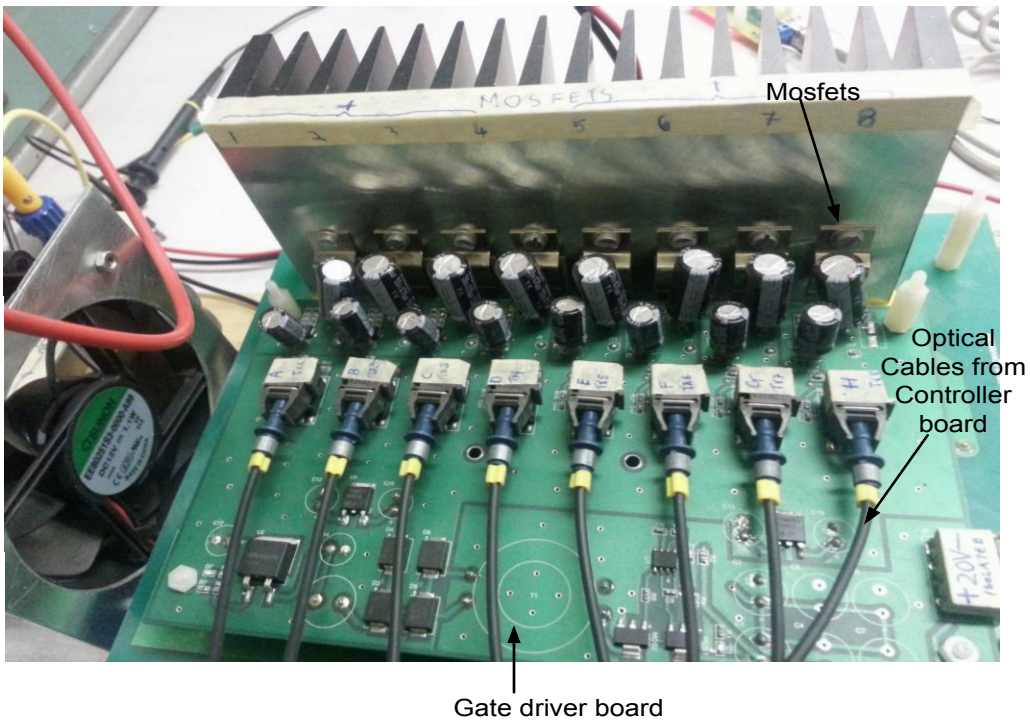


Figure 7.3 The photo of the Mosfet board and mosfet driver board used in the practical test

7.4 SYNCHRONOUS BUCK CONVERTER AS DC-TO-DC CONVERTER

The first test on the synchronous buck converter was to convert a 30 V DC to 2 V DC to see how well the result compared with the simulation. The result of this test as measured with Signaltap in Quartus, is shown in Figure 7.4 below.

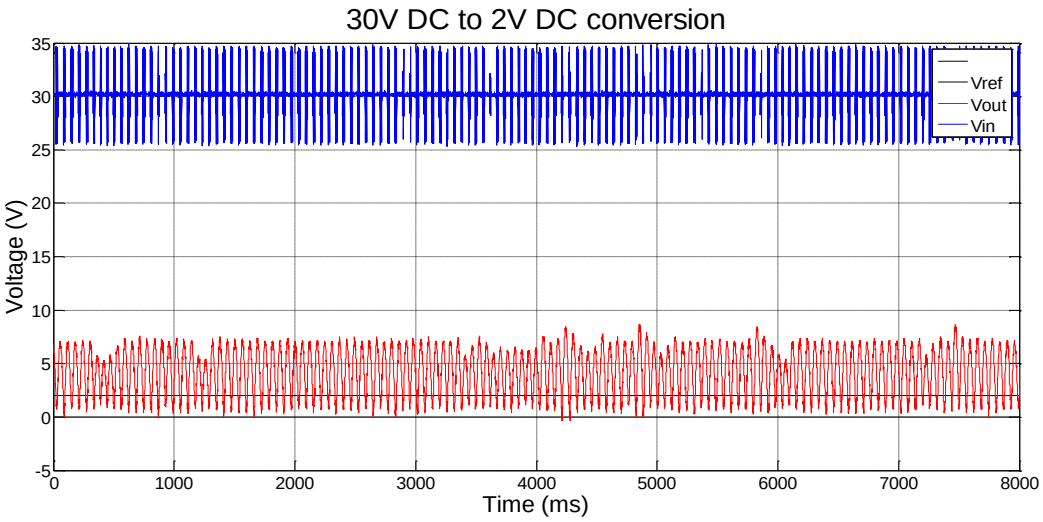


Figure 7.4 Input (blue) and output (red) voltages for the 30V DC to 2 V DC conversion test

The result shows that the switching frequency is low at 2.4 kHz and the output voltage is slightly higher than the reference voltage. The voltage fluctuation is much larger than in the simulation. The large fluctuation can largely be attributed to the measurement noise. Other than that, the response of the converter matches exactly the simulation. Increasing the cost penalty for switching frequency had the same effect as in the simulation i.e. the output voltage was higher than the reference voltage.

The reference voltage was increased to 21 V, as in the simulation. The output voltage was seen to be slightly lower than the reference voltage, as shown in Figure 7.5 below, and the switching frequency increased to about 8 kHz. The input voltage shows the same ripple, but at a higher frequency. The output voltage shows the same behaviour shown in the simulation, being slightly less than the reference voltage. Increasing the cost for switching frequency had the effect of increasing the output voltage error, as experienced in the simulation.

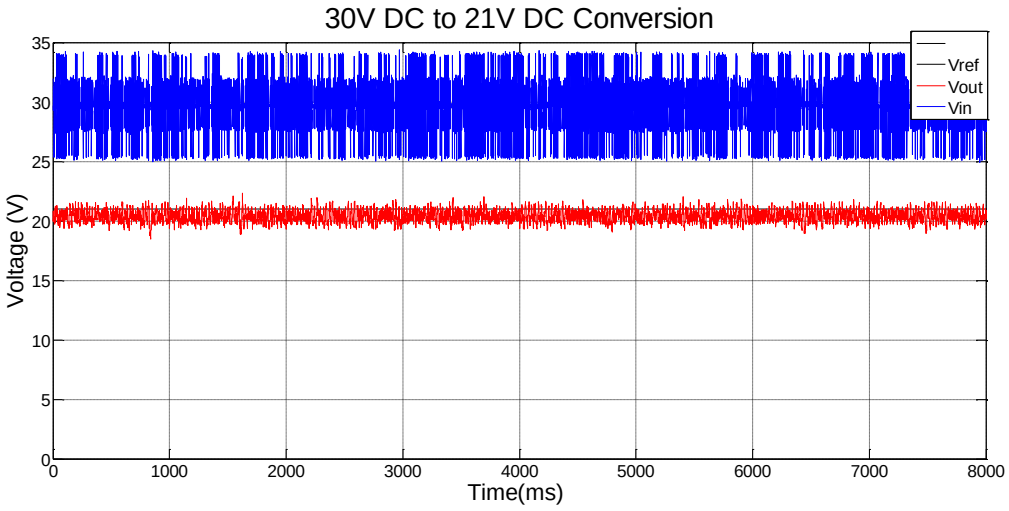


Figure 7.5 Input(blue) and output (red) voltages for 30 V DC to 21 V DC voltage converter practical results

7.5. SYNCHRONOUS BUCK CONVERTER AS A DC-TO-AC CONVERTER

The synchronous buck converter was controlled as a DC to AC converter. Several tests were carried out to determine the behaviour of the controller.

7.5.1 Sampling at 10 kHz

The controller was set to sample at a frequency of 10 kHz and the reference was set to a sinusoidal wave of amplitude of 18 V. The output voltage from the oscilloscope is shown in Figure 7.6. The blue line is the output voltage while the green line is the output current. With a sampling frequency of 10 kHz, the controller switched at an average frequency of 2.4 kHz. The output is not smooth, due to the low switching frequency. Switching frequency is especially low when the sine wave value approaches the Vin or zero. This is what was also observed in the simulations.

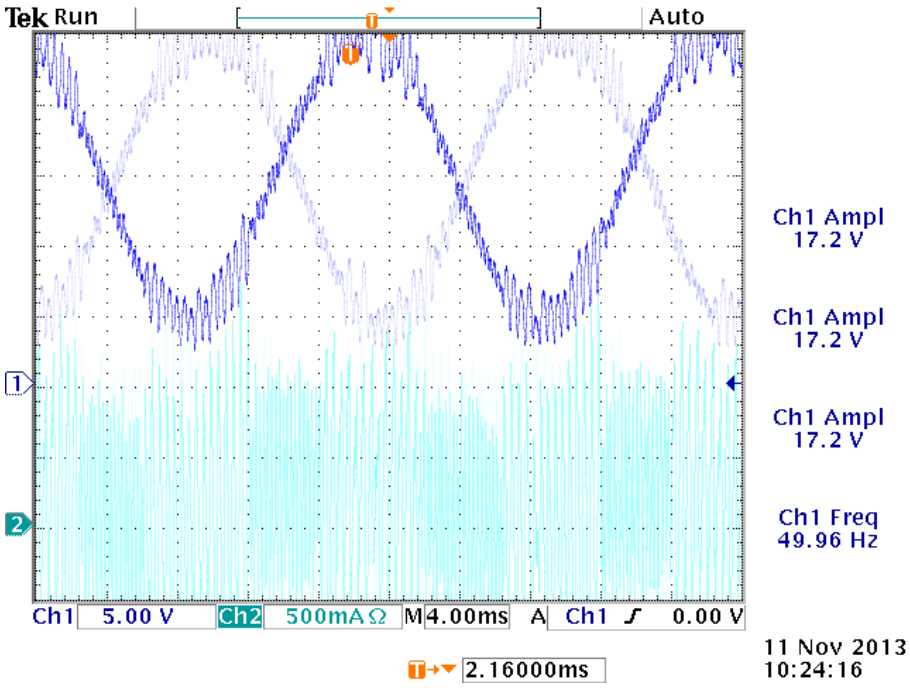


Figure 7.6 Output voltage (blue) for 10kHz sampling frequency

When sampling was set at 10 kHz, there was no frequency control, as the highest possible switching frequency is 5 kHz, which is within the safe switch operating frequency range. The controller switched at a maximum frequency of 2.4 kHz.

7.5.2 Sampling frequency set at 100 kHz

The controller sampling frequency was then set at 100 kHz with the maximum switching frequency for the switches limited to 5 kHz. The cost function was increased to get a better output voltage. The result of the test is shown in Figure 7.7 and Figure 7.8 shows the output signal when the switching frequency is increased to a limit of 10 kHz.

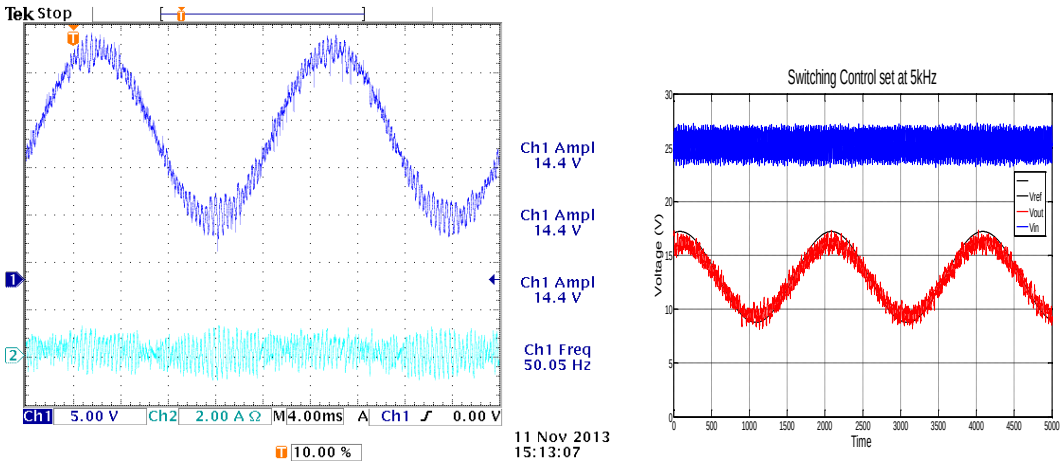


Figure 7.7 Output voltage with switching frequency limited to 5 kHz

The oscillogram on the left shows the oscilloscope measurement of the output voltage in blue and the current is shown in green. The oscillogram on the right shows the Matlab signal tap measurement. The input voltage is shown in blue, the output voltage is in red and the reference voltage is in black.

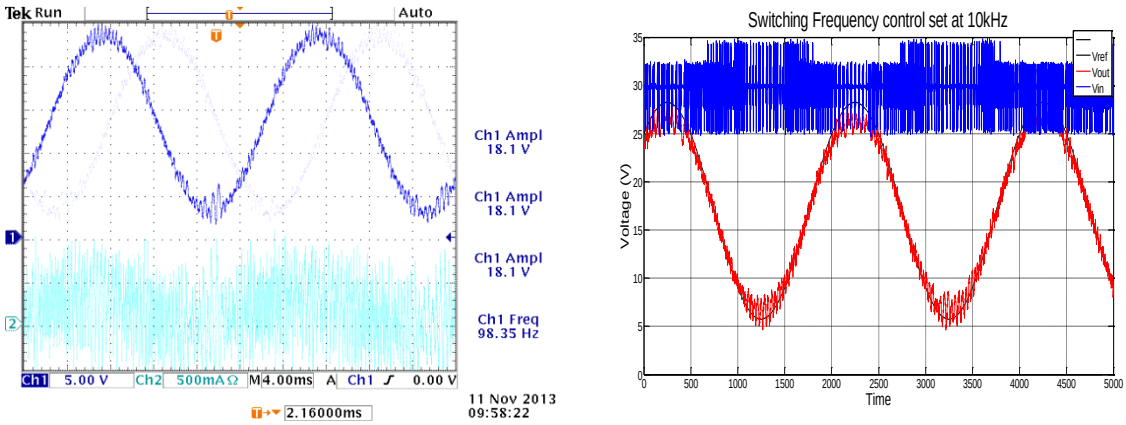


Figure 7.8 Voltages with switching frequency limited to 10 kHz

When the reference voltage was adjusted to a maximum amplitude of about 5 V from half of the supply voltage, the switching frequency was more consistent and the output voltage was smoother

7.5.3 Sampling frequency at 1 MHz

The sampling frequency was set to 1.0 MHz while the switching frequency was limited to less than 5 kHz.and then 10 kHz. With this sampling frequency, the output voltage was much smoother and more consistent, as shown below in Figure 7.9 and Figure 7.10.

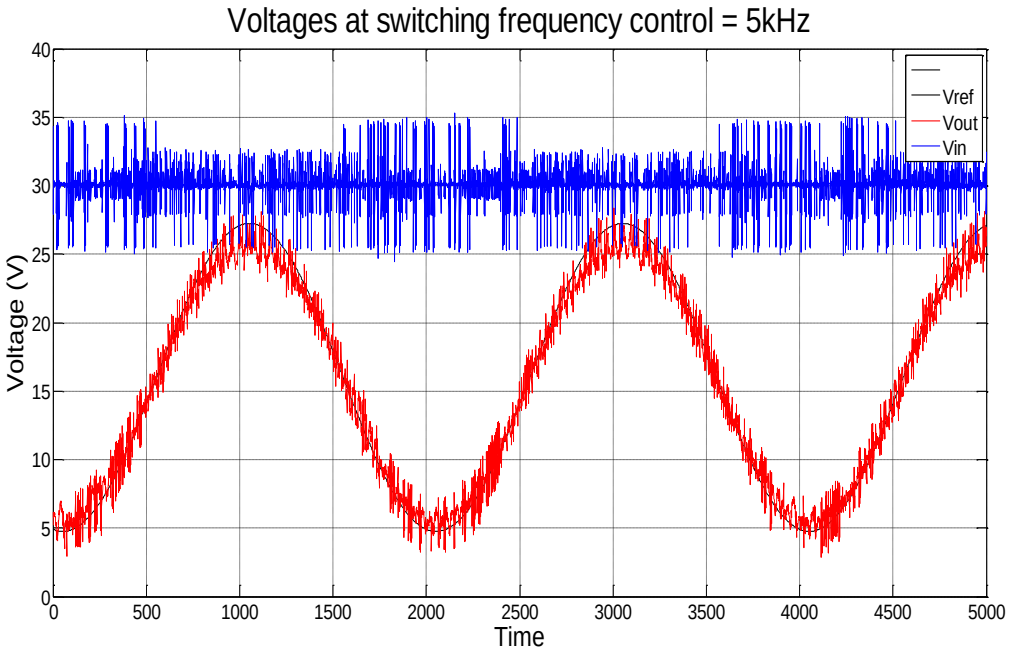


Figure 7.9 Output voltages at 1.0 MHz sampling frequency with switching frequency limited to 5 kHz

The Matlab measurement of the voltages show the blue DC input voltage, the red output voltage and the reference voltage in black. The reference voltage trace cannot be seen in the figure because the output voltage trace is over the reference line trace.

The switching frequency was then changed to a maximum of 10kHz. The resulting voltage is shown in Figure 7.10.

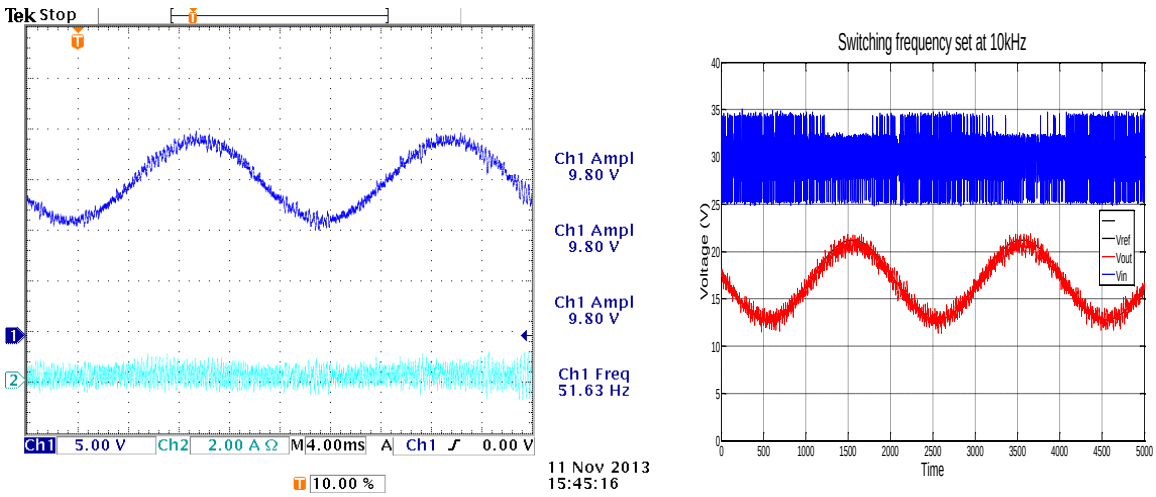


Figure 7.10 Output voltages at 1.0 MHz sampling frequency and switching frequency set at maximum of 10 kHz

The weighting coefficient for the switching frequency in the cost function was then increased to see the effect of an increased switching frequency. Figure 7.11 shows the output voltage when the cost function for the switching is increased.

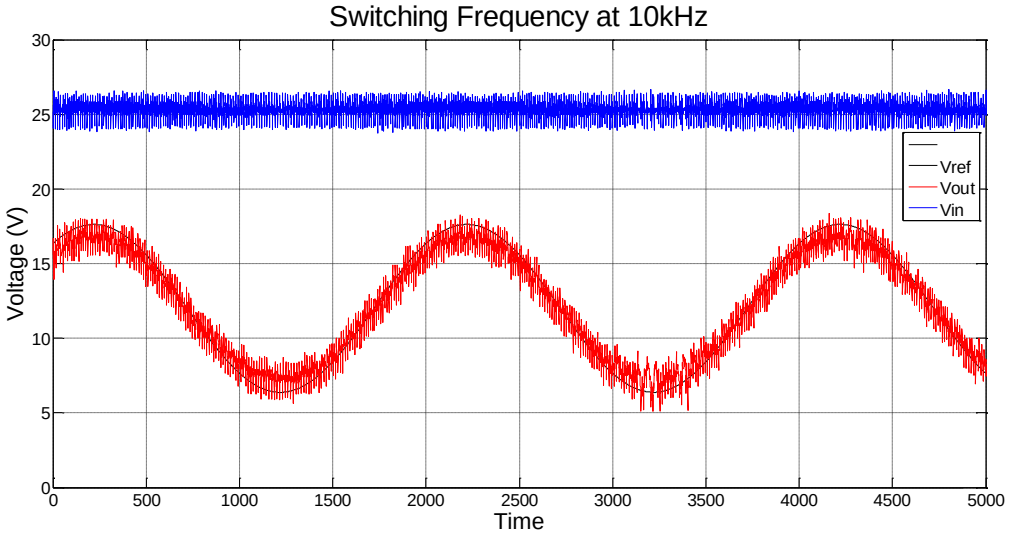


Figure 7.11 Output voltage with increased weight for switching frequency at a sampling rate of 1.0 MHz

In all the tests, the source voltage had a lot of noise which also appears on the output voltage.

7.6 SUMMARY

In this section, the Finite set Model predictive control was used to control the synchronous buck converter. Several tests have been carried out on the synchronous buck converter to check whether the switching frequency control method has any effect on the output voltage. It has been observed that increasing the switching frequency improves the output voltage. The higher the sampling frequency, the more flexible will be the switching times available for the controller. This has been further explained in Chapter 8.

CHAPTER 8
CONCLUSIONS AND FUTURE WORK

This chapter summarises and draws conclusions from the research and results obtained. It also provides areas in which more work is still needed to be done.

8.1 SUMMARY OF THE STUDY

As more and more sensitive equipment is being developed and connected to the electrical supply grids, quality of supply is very important to both electrical power suppliers and consumers and regulators. Several ways to ensure compliance with power quality standards were presented in Chapter 1 and Chapter 2.

Advancement in semiconductor technology has presented more methods for improving the power supply quality through the use of faster, cheaper and more efficient processors, and programmable devices for control and monitoring and the direct use of high voltage semiconductors in the supply path has enabled direct control of power which leads to fast response to power quality issues. Availability of the right software is of prime importance as has been seen in this study.

The study has demonstrated the use of FPGAs and high voltage IGBTs using FS-MPC to achieve power quality standards through the MVEVR. The accuracy of Matlab-Simulink and ModelSim for VHDL simulation have played a pivotal role in designing the right controller. The modularity of the FPGA board software has proved exceptionally useful and it has shortened the time necessary for implementation of the controller on the plant.

FS-MPC has been used to simulate control of MVEVR and has been successfully used on the synchronous buck converter for DC to DC and DC to AC conversion.

8.2 CONCLUSION

8.2.1 MVEVR Topology

The MVEVR is a very good system for voltage regulation. The problem of distorted input current has been documented by [34] and [44] both have controlled it using some form of control algorithm.

8.2.2 Control Algorithm

The results of the synchronous buck converter tests and the practical results were the same. This proves several things, namely:

a. The simulation softwares used were very accurate

b. The hardware models were accurate

c. The controller designed was good and suitable for implementation

d. The switching frequency control method used is effective.

e. One horizon prediction and control is sufficient for the MVEVR.

Though the control was not used on the actual plant, accuracy in the results of the simulation on the synchronous buck converter has proved beyond reasonable doubt that the same results obtained in the MVEVR simulation would be seen if the controller were to be implemented on the plant. This is due to the accuracy of the simulation software and accuracy in the plant models and good controller design.

Increasing the sampling frequency would improve on the performance of the controller by providing more options for switching slots available for the controller as shown in Figure 8.1

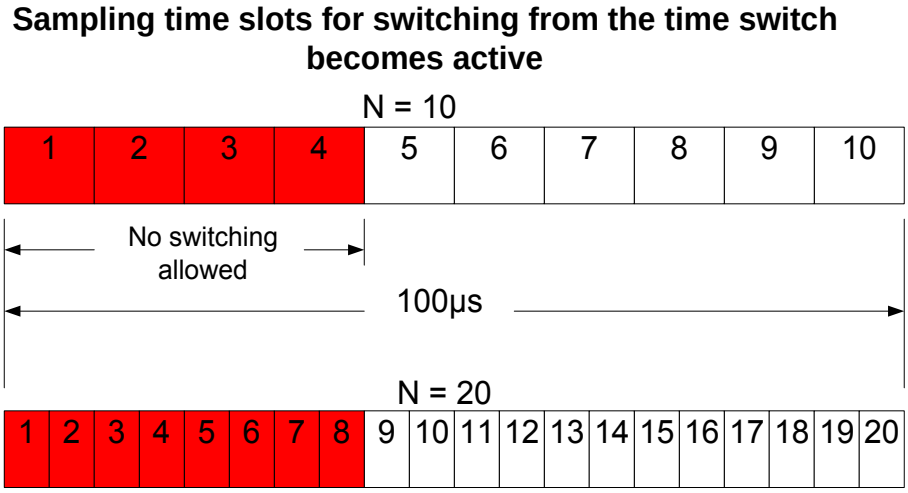


Figure 8.1 Sampling slots for switching from the time a switch changes state

When the sampling time slots are many, control is smoother, since this allows for finer control of switching frequencies, as is the case with PWM.

The implementation of FS-MPC is simpler to learn and apply than PID controllers would be.

8.3 FUTURE WORK

There is a need to adapt this switching frequency control on multilevel converters and other active front ends. Though the switching frequency control worked to improve the input frequency, there is a need to develop a dynamic cost system that would be able to

determine the best frequency control cost based on magnitude of the input voltage relative to the reference voltage.

Practical tests of the controller need to be done on the MVEVR converter in order to verify its effectiveness.

Bibliography

[1] T.Jenkins, “A brief history of semiconductors,” University of Wales, Wales, 2005.

[2] K.Schipman and F. Delince, “The importance of good power quality,” ABB Power Quality Products.

[3] S. Albert, “Total power quality solution approach for industrial electrical reliability,” Power Quality World, Newark, 2006.

[4] South African Electricity Supply Industry, “Electricity supply - quality of supply,” Standards South Africa, Pretoria, 2008.

[5] K. Gebert and K. Edwards, Transformers principles and applications, 2nd ed., Illinois: American Technical Publishers, 1974.

[6] Central Station Engineers, Westinghouse Electrical Corporation, Electrical transmission and distribution reference book, 4th Ed., Westinghouse Electrical Corporation, 1964.

[7] D. Dohnal, “On-load tap-changers for power transformers: A technical Digest,” MR Publication, Regensburg.

[8] D. J. D. Toit, “Predictive Control of a series input, parallel output, back to back, flying capacitor multilevel converter.,” MscEng Thesis, Stellenbosch University, 2011.

[9] R. Fourie, “The development of IGBT based tap changer - MScEng Thesis,” University of Stellenbosch, Stellenbosch, 2009.

[10] J. Hindmarsh, Electrical machines and their applications, 4th ed., Pergamon, 1984.

[11] P.J.Hopkins, “Electrical Contacts for off-circuit tap changers for oil immersed transformers,” IEEE, 11 October 2005. [Online]. Available: http://grouper.ieee.org/groups/transformers/subcommittees/power/DETC/Paper-ElectricalContacts-DETC_Oct2005.pdf. [Accessed 2 November 2013].

[12] ABB, “On-load tap-changers, type UBB: Technical guide,” ABB, Ludvika, 2003.

[13] D. Listrik, “Electrical Science,” 2011. [Online]. Available: http://electrical-science.blogspot.com/2010/04/transformer-tap-changer.html. [Accessed 2 November 2013].

[14] Central Station Engineers of the Westinghouse Electric Corporation, Electrical

transmission and distribution reference book, 4th Edition, 1964.

[15] R.Shuttleworth, X.Tian, C. Fan and A. Power, “New tap changing scheme,” *IEE Proc Electric power applications,* vol. 143, pp. 108-112, 1996.

[16] ABB Components, “On-load tap-changers, type VUC: Technical guide,” Ludvika, 2012.

[17] J. Faiz, “New solid state onload tap-changers topology for distribution transformers,” *IEEE transactions on power delivery,* vol. 18, January 2003.

[18] J.J.Serdyn, “Electronic Voltage regulator technology for rural electrification, Masters thesis,” Stellenbosch University, Stellenbosch, 2008.

[19] J.Faiz and B.Siahkolah, Electronic tap-changer for distribution transformers, New York: Springer, 2011.

[20] F. Yousef-Zai and D. O. Kelly, “Solid state on-load transformer tap changer,” *IEE proceeding on power applications,* vol. 143, no. 6, pp. 481-491, 1996.

[21] D.Floricau, M.Dumitrescu, I. Popa and S.Ivanov, “Basic topologies of direct PWM choppers,” *Annals of the University of Craiova, Electrical Engineering series,* vol. 30, pp. 141-146, 2006.

[22] P.Bauer and S. d. Haan, “Electronic tap changer for 500kVA/10kV distribution transformers: Design, experimental results and impact in distribution networks,” ENECO (Power Utility), The Hague, 1997.

[23] C. V. Schalkwyk, “Analysis and design of a voltage Regulator based on AC to AC converter - masters thesis,” Stellenbosch University, Stellenbosch, 2003.

[24] M. Wolf, “Design and implementation of a modular converter with application to a solid state transformer, Master's Thesis,” University of Stellenbosch, Stellenbosch, 2009.

[25] J. v. d. Merwe and H. T. Mouton, “The solid state transformer concept: A new era in power distribution,” Master's Thesis, University of stellenbosch, 2009.

[26] L. Schietekat, “Design and implementation of the main controller of a solid-state transformer, Masters thesis,” University of Stellenbosch, Stellenbosch, 2011.

[27] T.Zheng, Model predictive control Design, Rijeka: Sciyo, 2010.

[28] E.F.Camacho and C. Bordons, Model predictive Control, Springer, 2004.

[29] M. Nikolau, Model predictive controllers: A critical synthesis of theory and industrial

needs, Houston: University of Houston, 1996.

[30] C. D. Keyser and V. Cuawenberghe, “Extended prediction self-adaptive control,” *IFAC Symp. on Identification and System parameter Estimation,* pp. 1317 - 1322, 1985.

[31] D.W.Clarke, C. Mohtadi and P. Tuffs, “Generalised predictive control. part 1. The basic algorithm,” *Automatica,* vol. 23, no. 2, pp. 137 - 148, 1987.

[32] C.Greco, G. Menga, E. Mosca and G.Zappa, “Performance improvement of self tuning controllers by multistep horizons: the MUSMAR approach,” *Automatica,* vol. 20, pp. 681 - 700, 1984.

[33] R. Soeterboek, Predictive Control, A unified approach, Prentice -Hall, 1992.

[34] D. A. Johan, “Supervisory control and sliding mode control of a medium voltage direct AC-AC voltage regulator - MSCEng Thesis,” Stellenbosch University, Stellenbosch, 2012.

[35] P. Cortes, M.P.Kazmierkowski, R. Kennel, D. Quevedo and R. Jose, “Predictive Control in Power Electronics,” *IEEE Transactions on Industrial Electronics,* vol. 55, no. 12, pp. 4312 -4324, December 2008.

[36] D.E.Quevedo, R. Aguilera and T.Geyer, Predictive Control in Power Electronics and drives: basic concepts, theory and methods., In Print, 2013.

[37] W. Books, “Introduction to Predictive Control,” [Online]. Available: http://www.wiley-vch.de/books/sample/352731492X_c01.pdf. [Accessed 12 December 2012].

[38] F. Borrelli, A.Bemporad and M. Morari, Predictive control for linear and hybrid systems, Berkeley: University of Cambridge, 2011.

[39] M. Kvasnica, Real-time model predictive control via multi-parametric programming. theory and tools, Saarbucken: VDM verlag , 2009.

[40] J. Rossiter, Model-based Predictive Control - A practical approach, Boca Raton: CRC Press, 2003.

[41] J. Maciejowski, “4F3 - Predictive Control,” [Online]. Available: http://www-control.eng.cam.ac.uk/mm/4f3/predictive1.pdf. [Accessed 24 July 2012].

[42] Wikipedia, “Model Predictive Control,” 10 July 2013. [Online]. Available: http://en.wikipedia.org/wiki/Model_predictive_control. [Accessed 15 July 2013].

[43] P. Cortes, R. Vargas, S. Leon, S. Vazquez and L. Franquelo, “Guidelines for weighting Factors Design in Model Predictive Control of Power Converters and Drives.,” *IEEE International Conference on Industrial Technology,* pp. 1-7, 2009.

[44] M. Tomlinson, H. Mouton, R. Kennel and P. Stolze, “Model predictive control of and AC-to-AC converter with input and output LC filter”.

[45] P. Stolze, P. Landsmann, R. Kennel and H. Mouton, “Finite set model predictive control of a flying capacitor converter with hysteresis voltage balancing,” *INEuropean Conference on Power Electronics and Applications,* pp. 210-217, 2011.

[46] J. Rodriguez, J. Pontt, C. Silva, P.Correa and P. Cortes, “Predictive current control of a voltage source inverter,” *IEEE Transactions on Industrial Electronics,* vol. 54, no. 1, pp. 495 - 503, 2007.

[47] G. Perantzakis, F. Xepapas and S. Manias, “Efficient predictive current control technique for multilevel voltage source inverters,” *In European Conference on Power Electronics and Application,* 2005.

[48] D. Correa, P. Rodriguez, J. Lizama and I. Andler, “A predictive control scheme for current source rectifiers,” *IEEE Transactions on Industrial Electronics,* vol. 56, no. 5, pp. 1813 - 1815, 2009.

[49] R.P.Aguilera and D. Quevedo, “Capacitor Voltage Estimation for Predictive Control Algorithm of Flying Capacitor Converters”.

[50] R. P. Aguilera, D. Quevedo, T. Summers and L. P., “Predictive control algorithm robustness for achieving fault tolerance in multicell converters,” *IEEE,* pp. 3302 - 3308, 2008.

[51] Y. Kim and F. Lewis, “Dynamic Neural networks for closed loop feedback control and estimation of uncertain non-linear systems,” *Industrial and Manufacturing Systems: Neural Network Systems Techniques and Application,* pp. 213 - 271, 1998.

[52] M. Jamshidi, M.Tarokh and B.Shafai, Computer- aided analysis and design of linear control systems, Englewood Cliffs: Prentice Hall, 1992.

[53] R. Robins, “Control Engineering Europe,” IML Group plc, 05 March 2010. [Online]. Available: http://www.controlengeurope.com/article/32043/Advantages-of-FPGAs.aspx. [Accessed 2013 September 2013].

[54] Wikibooks, “Control Systems,” in *Control Systems And Control Systems Engineering*

with Classical and Modern Techniques And Advanced Concepts, Wikibooks, 2006, pp. 3 - 209.

[55] P.Stolze, M. Kramkowski, T. Mouton, M. Tomlinson and R. Kennel, "Increasing the performance of finite set model predictive control by oversampling," *IEEE International Conference on Industrial Technology (ICIT),* pp. 551-556, 25- 26Feb. 2013.

[56] H.Miranda, P.Cortes, J.I.Yuz and J. Rodriguez, "Predictive torque control of induction machines based on state-state models," *IEEE Transactions on Industrial Electronics,* vol. 56, no. 6, pp. 1916 - 1924, June 2009.

[57] M. W. Hirsch and S. Smale, Differential equations, dynamic systems and linear algebra, Academic Press, 1974.

[58] S. Iplikci, "Runge-Kutta Model-based Adaptive Control Mechanism for Non-linear Processes," *Transactions of the Institute of Measurement and Control,* vol. 35, no. 2, pp. 166-160, 2012.

[59] A. Paredes, J. Simpson, J. Pontt and C. Silva, "Predictive Current Control of a Multilevel Active Filter for Industrial Installations," in *Power Electronics, Drives and Energy Systems (PEDES) & Power India*, New Dehli, 2010.

[60] D.E.Quevedo, M.Perez and P. Cortes, "Finite control set MPC of an AFE rectifier with dynamic references," *IEEE Industrial Conference on Industrial Technology,* pp. 1265 - 1270, 2010.

[61] wikipedia.org, "Euler Method," Wikimedia Foundation, 14 May 2013. [Online]. Available: http://en.wikipedia.org/wiki/Euler_forward_method. [Accessed 22 May 2013].

[62] R.Vargas, P. Cortes, U. Ammann, J. Rodriguez and J. Pontt, "Predictive control of a three phase neutral clamped inverter," *IEEE Transactions On Industrial Electronics,* vol. 54, no. 5, pp. 2697 - 2705, 2007.

[63] T.Mouton, P. Stolze, M. T. T. Geyer and R. Kennel, "Predictive control vs. linear control for current control of a single-leg inverter," *Trans. on Power Electronics,* 2013.

[64] A. G. Gebregergis, "A three phase AC-AC matrix converter system," Master's Thesis, Stellenbosch University, 2004.

Appendix A

Control using different discretisation methods

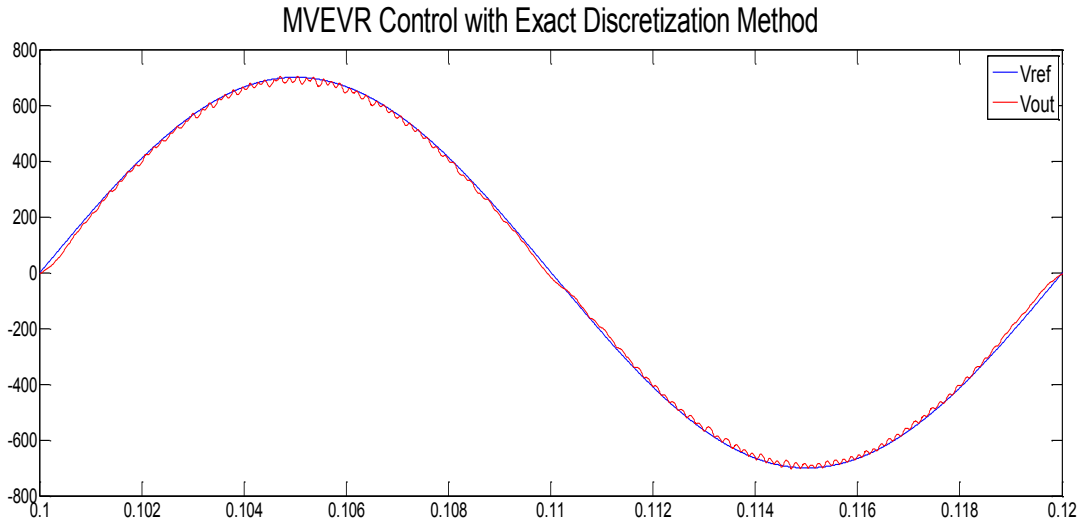


Figure A.1 Discretisation of MVEVR control using exact method of discretisation

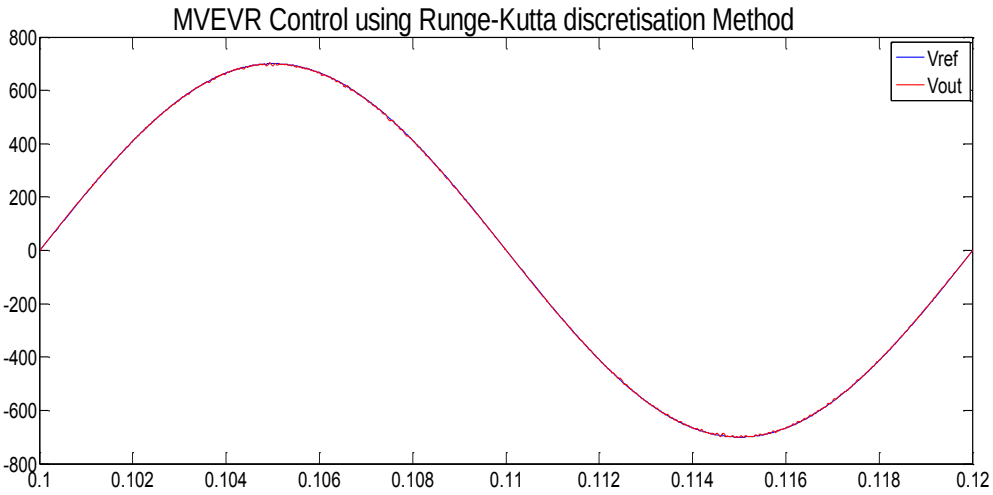


Figure A.2 Control of MVEVR using Runge Kutta discretisation method

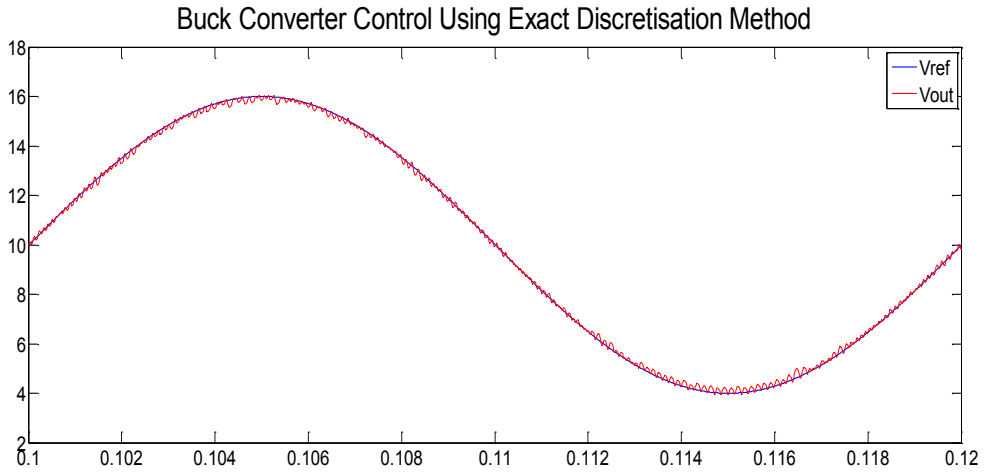


Figure A.3 Control of synchronous buck converter using exact discretisation method

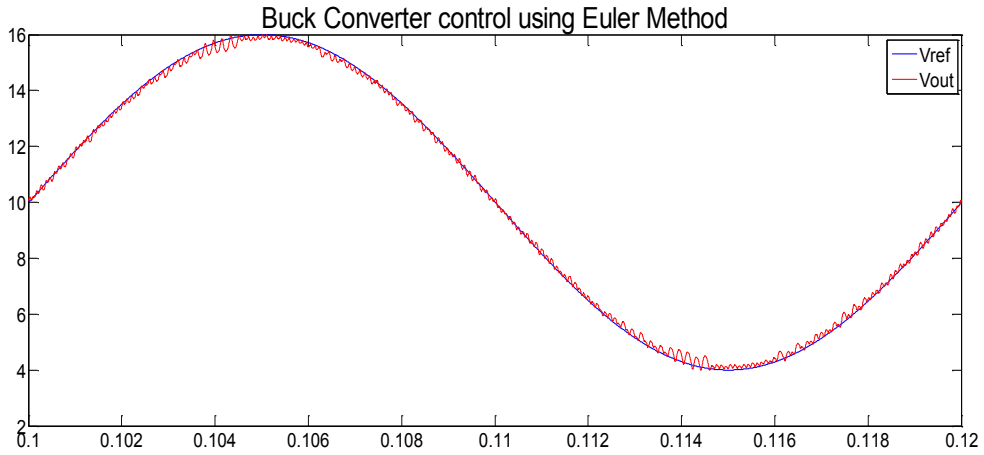


Figure A.4 Control of synchronous buck converter using Euler method

Appendix B

VHDL Code for allocating cost to switch for switching frequency control.

```
IBRARY ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
use ieee.std_logic_unsigned.all;
use ieee.fixed_pkg.all;
use ieee.fixed_float_types.all;

entity OS_Calc is
 port (next_state: in std_logic;
   clk              : in std_logic;
   Nsamp                              : in integer_range 0 to 100 :=10; -- This is Sampling_frequency/switching_frequency
   Off_OSfactor, On_OSfactor  : out integer range 0 to 100:=0); -- Cost to be allocated to each state
end OS_Calc;

architecture generated_cost of OS_Calc  is
signal  sig1       : std_logic :='0';-- This is the present state of the controller output 'ON or OFF' with OFF as initial condition
begin
process (clk)
begin
sig1 <= next_state; -- Allocate next_state to present at the next sampling slot
-- Reset the costs to initial if now_state is not equal to next_state or
--state_counter has reached the maximum count of Nsamp to give the new state the least cost and the last state the highest cost
```

```
if (next_state /= sig1) or (Nsamp == sig5) then
                sig5 <= 0;
                if next_state = '1' then
                        Off_OSfactor <= Nsamp;
                        On_OSfactor <= 0;
                else
                        On_OSfactor <= Nsamp;
                        Off_OSfactor <= 0;
end if;
-- Increment the value of cost for active state and decrement the value of the idle state
else
        sig5 <= sig5+1;
if next_state = '1' then
                        Off_OSfactor <= Nsamp – sig5;
                        On_OSfactor <= sig5;
                else
                        On_OSfactor <= Nsamp – sig5;
                        Off_OSfactor <= sig5;
                end if;
end if;
end process;
end generated_cost;
```