

Supervisory Control and Sliding Mode Control of a Medium Voltage Direct AC-AC Electronic Voltage Regulator

by

Dewald Johan Abrie

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Supervisor: Prof H du T Mouton
Department of Electrical & Electronic Engineering

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DECLARATION

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ABSTRACT

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D. J. Abrie

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Department of Electric and Electronic Engineering

Thesis: MScEng (Electronic)

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As control problems become more and more complex, techniques are required that surpass the capabilities of simple controllers that are linearized about certain parametric set points. Controllers that can operate over a large range of model parameter variations and even controllers that are largely model-independent are becoming more valuable and necessary.

In this control application, voltage regulation is done on a direct AC-AC medium voltage regulator, making use of a type of regulated autotransformer configuration. The fifth order system is shown to be prone to oscillations on the input bus. This, together with the control requirement of robustness to load variations, provides a challenging control problem that is rarely addressed in literature.

This thesis solves the control problem by means of applying sliding mode control on voltage regulator module level, and supervisory control on system level.

UITTREKSEL

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Soos die soeke na oplossings vir hedendaagse beheer probleme al hoe meer uitdagend raak, word die behoefte vir model onafhanklike en robuuste beheerders dienooreenkomstig groter. Eenvoudige beheerders wat gelineariseer is om 'n parametriese werkpunt raak ondoeltreffend vir vandag se vereistes vir doeltreffende beheer ongeag van parametriese veranderinge.

In hierdie tesis word spanning regulasie toegepas deur 'n direkte WS-na-WS medium spanning reguleerder in te span. Hierdie toestel maak gebruik van 'n tipe van outotransformator opstelling waar die sekondêre wikkings gereguleer word deur die skakelaksie van die drywingselektroniese regulasie modules. Die vyfde-orde stelsel se intree bus is geneigd om onstabiel te raak, en moet dus aktief gedemp word terwyl die uitreespanning gereguleer word. Die vereiste dat die beheer boonop robuus ten opsigte van las veranderinge moet wees maak hierdie probleem 'n monster van 'n uitdaging wat skaars in die literatuur aangeraak is.

Hierdie tesis los die probleem van robuuste beheer op deur glymodus beheer toe te pas op reguleerder module vlak, en ook deur toesighoudende beheer op stelsel vlak toe te pas.

To God, my strength, my hope, and my inspiration.

*My soul pursues you;
your right hand upholds me.*

Psalm 62:1-2

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List of Abbreviations

NERSA	National Energy Regulator of South Africa
LV	Low Voltage
MV	Medium Voltage
IV	Intermediate Voltage
HV	High Voltage
LN	Line to Neutral
VR	Voltage Regulator
VHSIC	Very High Speed Integrated Circuit
VHDL	VHSIC Hardware Description Language
VHDL-AMS	VHDL Analogue Mixed-signal
MVEVR	Medium Voltage Electronic Voltage Regulator
PDF	Probability Density Function
IGBT	Insulated-gate Bipolar Transistor
VSC	Variable Structure Control
SMC	Sliding-mode Control
QSMC	Quasi Sliding-mode Control
ANN	Artificial Neural Network
THD	Total Harmonic Distortion
LPF	Low-pass Filter
RP	Representative Point
IATE	Instantaneous Absolute Tracking Error
AC	Alternating Current
DC	Direct Current
FPGA	Field Programmable Gate Array
DSP	Digital Signal Processor

SQNR	Signal to Quantization Noise Ratio
A ³	Algorithm Architecture Adequation
ADC	Analogue to Digital Converter
LVDS	Low Voltage Differential Signalling
PWM	Pulse Width Modulation
IO	Input-Output
PLL	Phase Locked Loop
IP	Intellectual Property
JTAG	Joint Test Action Group
BST	Boundary-Scan Testing
IEEE	Institute for Electric and Electronic Engineers
FIR	Finite Impulse Response
IIR	Infinite Impulse Response
FFT	Fast Fourier Transform
PC	Personal Computer
IDE	Integrated Development Environment
STD	State Transfer Diagram
LCD	Liquid Cristal Display
LCCDE	Linear Constant Coefficient Difference Equation
RMS	Root Mean Square
MS	Mean Square
FIFO	First In First Out
EMF	Electromotive Forces

Nomenclature

Rise time Rise time refers to the time required for a signal to change from its initial state to the full value of the reference.

Overshoot Overshoot is when a signal or function exceeds its target. It is often associated with ringing.

Settling time Settling time is the time elapsed from the application of an ideal instantaneous step input to the time at which the output has entered and remained within a specified error band.

Delay time The delay time is the time required for the response to reach half the final value the very first time.

Peak time The peak time is the time required for the response to reach the first peak of the overshoot.

Steady-state error The mean value of the error between the signal and its reference over a specific sample.

List of Symbols

Constants:

$$\pi = 3.1415926535897932384626433832795$$

$$e = 2.7182818284590452353602874713526$$

Circuit Modelling

v_{LN} = line-to-neutral voltage

v_{reg1} = output voltage of regulator one

v_{reg2} = output voltage of regulator two

E_p = EMF of primary winding

E_{s1} = EMF of first secondary winding

E_{s2} = EMF of second secondary winding

N_p = Number of windings on the transformer primary side

N_{s1} = Number of windings on the first secondary coil

N_{s2} = Number of windings on the second secondary coil

I_p = Current entering the primary winding

I_{s1} = Current leaving the first secondary winding

I_{s2} = Current entering the second secondary winding

i_{in} = regulator module input current

i_{ind} = regulator module's output filter inductor current

v_{bus} = regulator module's input bus capacitor voltage

i_{out} = MVEVR output current, regulator module output current

i_{C_o} = MVEVR output current, regulator module output current

Sliding-mode Control

$\mathbf{f}(\mathbf{x}, t)$ = drift field

$\mathbf{g}(\mathbf{x}, t)$ = control input field

σ = sliding function

u = control variable

u_{eq} = equivalent control

$L_{\mathbf{f}}\sigma(\mathbf{x})$ = Lie derivative with respect to \mathbf{f}

$L_{\mathbf{g}}\sigma(\mathbf{x})$ = Lie derivative with respect to \mathbf{g}

CHAPTER 1

INTRODUCTION

“There is nothing more difficult to take in hand, more perilous to conduct, or more uncertain in its success, than to take the lead in the introduction of a new order of things.”

- Niccolo Machiavelli

1.1 Motivation and Topicality of this work

As control problems become more and more complex, techniques are required that surpass the capabilities of simple controllers that are linearized about certain parametric set points. Controllers that can operate over a large range of model parameter variations and even controllers that are largely model-independent are becoming more valuable and necessary.

In this control application, voltage regulation is done on a direct AC-AC medium voltage regulator, making use of a type of regulated autotransformer configuration. Regulating directly from AC to AC allows one to avoid rectification and thereby allows for savings on component costs. This approach does complicate the control requirements, as the input bus tends to be unstable. With the added control requirement of robustness to load variations, the control problem becomes a monster that is rarely addressed in literature.

This thesis attempts to solve this problem by means of applying sliding mode control on voltage regulation level, and supervisory control on system level.

1.2 Background

An important aspect of power distribution is the quality of power supplied. Electricity standards are imposed on power producers by the National Energy Regulator of South Africa (NERSA). The NRS048-2:2003 industry standard[2] outlines various quality of supply parameters that are to be adhered to within specified limits, such as magnitude of supply voltage, frequency, voltage unbalance, voltage harmonics and inter-harmonics, mains signalling, voltage flicker, rapid voltage changes, voltage dips, voltage swells and transient over voltages. Most of the parameters listed can be addressed by the implementation of sufficiently fast and effective voltage regulators.

The need for voltage regulators become specifically pronounced where sub-transmission/distribution lines extend their intended design length. At these lengths the resistive losses cause sufficient voltage drop to cause the line voltage amplitude to fall below the NERSA standard. The under voltage can be compensated for by hooking up an effective voltage regulator (referred to as 'VR' in the Fig. 1.1) at this point on the line. The line can then be extended further to reach nearby communities. Current tap changers used for this purpose are slow in their regulation response and are expensive to maintain. The need for fast and maintenance-friendly medium voltage regulators arise.

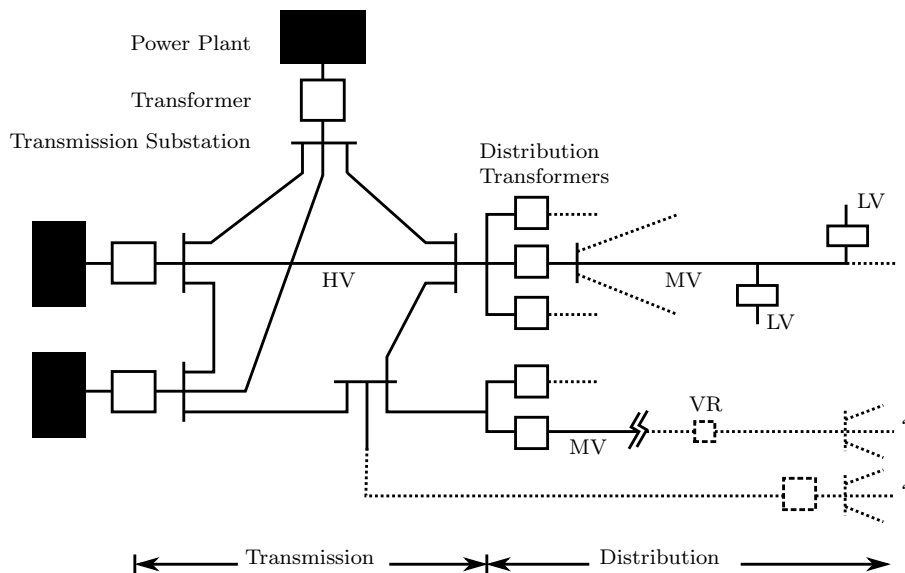


Figure 1.1: Basic representation of a power system. A voltage regulator (VR) can be used to over extend distribution lines. Adapted from [7].

1.3 Objectives of this study

- Supervisory control development to be implemented on a FPGA.
- Modelling of MVEVR
- Robust control of MVEVR regulation modules
- Miscellaneous hardware development

1.4 Contributions

1. Supervisory control with VHDL code that is modular, extensible, and reusable
2. VHDL-AMS modelling of the MVEVR to complement VHDL implementation on FPGA
3. Modelling of the MVEVR's three winding transformer in a simple form with all the equivalent impedances reflected to one of the secondary windings.
4. Sliding mode controller for AC-AC regulation modules that is particularly load insensitive
 - (a) A graphical approach for analysing the sliding mode control reachability condition was developed and applied
 - (b) A modulation signal with adaptive amplitude was developed to fix the switching frequency

1.5 Overview of this work

This thesis presents an introduction to the problem, a survey of the available literature, an overview of the control theory used, control design on system and module level, results and discussion, and finally conclusions and future work.

Chapter 2 provides some background on the need of affordable medium voltage regulators in South Africa (Section 2.1), as well as the need for robust control for these regulators (Section 2.5). A brief overview of available robust control techniques is also given.

Chapter 3 explains the basic theory of sliding mode control (Section 3.1) and provides the needed mathematical tools for stability, existence, and reachability analysis (Section 3.2). An important second-order example is presented where SMC is applied in Section 3.3 to a synchronous buck converter. This lays the foundation for Chapter 7, where sliding mode control is applied to the fifth order MVEVR.

Chapter 4 details the MVEVR component level (Section 4.2) and system level (Section 4.3) mathematical modelling together with VHDL-AMS models for computer simulation. Models and transfer functions developed here are used in Chapter 7 when applying analysing control algorithms.

Chapter 5 gives a basic overview of the FPGA design of the system controller with diagrams of the most important VHDL entities' ports and features (Section 5.5). A range of generic synthesisable VHDL components were developed for use in the sliding-mode control and the supervisory control. An overview of these components are given in Section 5.6.

Chapter 6 frames the MVEVR control problem with control objectives on module- and system- level (Section 6.2). Section 6.3 presents the design of the sliding mode controller for the MVEVR. This is an extension of the example worked through in the theoretically oriented Chapter 3. A new graphical approach to analysing reachability is demonstrated in Fig. 6.10 of Section 6.3.9. A new modulation carrier with adaptive amplitude for fixed frequency control is detailed in Section 6.3.10. The extent of robustness with regard to load variations is analysed in Section 6.3.12.

Chapter 7 presents laboratory results pertaining to closed-loop control. Results are shown for tests on waveform correction (Section 7.1), amplitude control (Section 7.2), module interaction (7.3), and system level performance (7.4).

Chapter 8 closes this thesis with conclusions (Section 8.1) and future work (Section 8.2) to be done.

CHAPTER 2

LITERATURE STUDY

“Is it a fact—or have I dreamt it—that, by means of electricity, the world of matter has become a great nerve, vibrating thousands of miles in a breathless point of time?”

- Nathaniel Hawthorne In *The House of the Seven Gables* (1851), 203.

2.1 Background of the Problem

In the early 1990's, South African state-owned power utility, ESKOM, started directing its attention to providing affordable electricity to all, regardless of ethnicity or economic class. In 1992 hundreds of electrification projects were under way to extend supply to all South Africans. In order to boost economic competitiveness in the country, ESKOM aimed to reduce electricity tariffs, and according to an international survey, managed to provide the cheapest electricity in the world. In 1994, South African Government decided to replace the national Electricity Control Board with the newly found National Electricity Regulator of South Africa (NERSA). This body was responsible for improving power quality and for establishing effective distribution, metering, and billing systems across South Africa.[3]

ESKOM undertook to electrify 1.75 million homes by the year 2000. They promptly achieved this goal by November 1999.[3] Energy Minister, Dipuo Peters, recently noted that from 1994 to 2010, access to electricity has increased from 30 % to over 80 % of the population.[58] The goal of ubiquitous electrification still continues, and new solutions for good quality and cost effective power distribution are constantly pursued.

An important aspect of power distribution is the quality of power supplied. Electricity standards are imposed on power producers by NERSA. The NRS048-2:2003 industry standard[2] outlines various quality of supply parameters that are to be adhered to within specified limits, such as magnitude of supply voltage, frequency, voltage unbalance, voltage harmonics and inter-harmonics, mains signalling, voltage flicker, rapid voltage changes, voltage dips, voltage swells and transient over voltages.

Most of the parameters listed can be addressed by the implementation of sufficiently fast and effective voltage regulators.

A given power system can generally be categorized in it's constituent phases such as generation, transmission, and distribution. Distribution can be sub-divided further into sub-transmission and reticulation. These phases, along with the voltage levels accompanying them is shown in Table 2.1. The classifications of different voltage levels are shown in Table 2.2.

Power System Phase	Voltage Levels
Generation	Generator dependent
Transmission	275 – 765 kV
Distribution	230 V – 132 kV
Sub-Transmission	33 – 132 kV
Reticulation	230 V – 33 kV

Table 2.1: Different phases of a power system and the respective voltage levels in South Africa.

On distribution level, voltages under 500 V are to remain within $\pm 10\%$ of rated values, and voltages above 500 V are to remain within $\pm 5\%$ of rated values. Doing this in an economically viable way is a significant challenge, especially in reaching small and remote distribution areas that are only reachable by long transmission/distribution lines.

Voltage Classification	Voltage Level
High Voltage (HV)	44 – 765 kV
Medium Voltage (MV)	11 – 44 kV
Intermediate Voltage (IV)	1 – 11 kV
Low Voltage (LV)	230 V – 1 kV

Table 2.2: Classification of voltage levels.

Voltage regulators are used to improve voltage levels on distribution level. In order to reach remote distribution areas, it is in some cases cheaper to over-extend a nearby medium voltage line on distribution level, rather than constructing a new high-voltage transmission line. This choice is illustrated in Fig. 2.1.

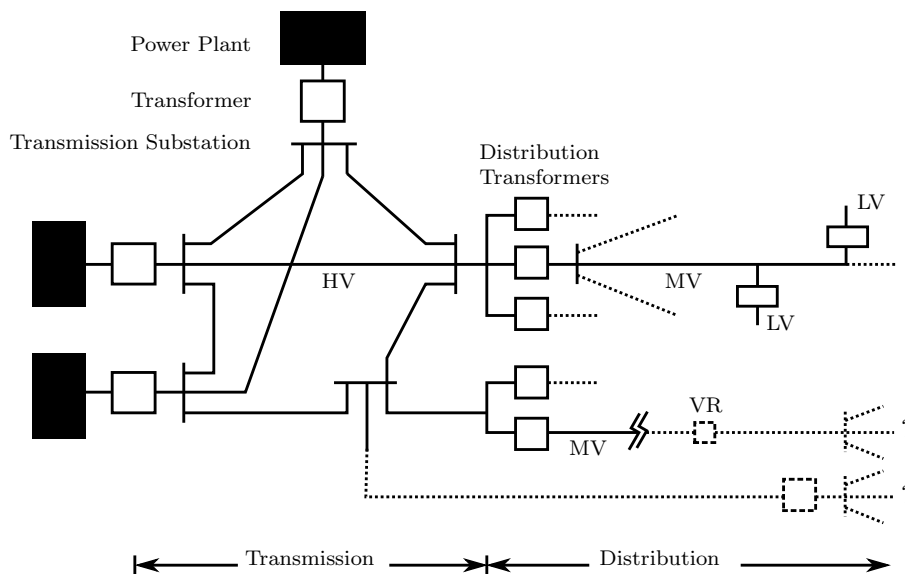


Figure 2.1: Basic representation of a power system. A voltage regulator (VR) can be used to over extend distribution lines. Adapted from [7].

The additional resistive losses due to larger currents on MV lines cause a voltage drop and thereby a deviation from the nominal voltage. These voltage drops can be compensated for with an appropriate voltage regulator. Various voltage regulator solutions exist for distribution level applications. Electromechanical tap-changing transformers are widely employed, but are slow and require frequent and expensive maintenance[8].

Power electronic solutions have fast dynamic response times and have added capabilities such as waveform correction. Solid state converters also require drastically less maintenance than devices with moving mechanical parts. However, these solutions can become expensive and reliability can be a concern due to the relatively high complexity of these devices.

Research has been done towards a cost-effective power electronic direct AC-AC converter capable of voltage regulation on medium voltage (MV) distribution lines. A study (along with cost comparisons) of competing non-power electronic solutions, as well as power electronic solutions, were done in [59]. A topology for an AC-AC power electronic voltage regulator was also proposed and implemented on reduced scale. This work was continued in [21], with an up-scaled design of the proposed topology suitable for regulation of 11 kV distribution lines. This thesis documents the realisation of this up-scaled design and the modular extension thereof towards higher input voltages, such as the current 22 kV system. One of the most challenging technical problems encountered was the development of a control scheme that would ensure internal stability as well as robustness with respect to uncertainties in the plant model.

2.1.1 The Need For Robust Control

General linear control techniques require linear models. To obtain linear models for non-linear systems, linearisation is performed around an operating point. When the system parameters change (like during load variations) the operating point also changes. This causes model inaccuracies and adversely effects control.[19, 47, p. 62]

The voltage regulator under consideration has various inescapable model uncertainties. The most prominent of these are the input- and output impedances, or rather the inductive impedance toward the generator, and the distribution load.

Complexity in Input Impedance Modelling

The input impedance of the MV regulator would be determined mostly by the length of distribution line to the nearest distribution transformer and the impedance of that transformer. This would be a complex resistive-inductive impedance and will differ from location to location. It is impractical to adapt the control scheme of the regulator for every installation. The control would therefore have to be robust with respect to input impedance.

Complexity in Load Modelling

MV loads are contingent on LV loads, which is a large source of uncertainty. When considering the load size for the purpose of determining the supply capacity required, the uncertainty can be dealt with by using probabilistic methods, rather than deterministic methods. Research into probabilistic design algorithms for LV loads appropriate to South African conditions is presented in [1]. In this research, probability density functions (PDFs) are derived from statistical load data. The PDF is strongly affected by factors such as the presence of water heating cylinders and circuit breaker size. This is in turn affected by demographic factors such as income, availability of piped water, type of dwelling, size of dwelling, ambient temperature, etc.

In most control schemes, however, probabilistic models cannot be used for controller design.¹ There is a need for control techniques that, given the possible range of load variation, would result in satisfactory dynamic performance and stable operation at any time.

¹Probabilistic models can, however, be used for offline training of artificial neural network type controllers.

2.2 Existing non-power-electronic topologies

A diligent study of existing non-power electronic topologies, along with cost comparisons were done in [59, p. 11-20]. Various advantages and disadvantages of the discussed topologies are mentioned. This thesis operates on the premise that the power-electronic solution is worth-while pursuing for its superior performance, comparable initial costs, and much cheaper maintenance costs.

2.3 Existing power-electronic solutions

Existing power electronic solutions have been documented in [59, p. 20-31]. A theoretical efficiency comparison between direct AC-AC converters and AC-DC-AC converters were also done. It was found that a direct AC-AC converter had at most 79% of the losses of two back-to-back AC-DC converters.

An existing converter with similar application as the converter documented in this thesis is found in [7, 8]. This power electronic tap changer is connected to existing taps on distribution transformers. The topology is shown in Fig. 2.2. The thyristors or IGBTs are placed on the primary taps in place of the conventional mechanical or electro-mechanical switch. If IGBTs are used as switching elements, continuous regulation of the secondary side can be achieved. This topology has advantages such that it can be integrated into existing infrastructure (distribution transformers). This is at the same time a trade-off in terms of applicability, should regulation be necessary on a line in-between distribution transformers.

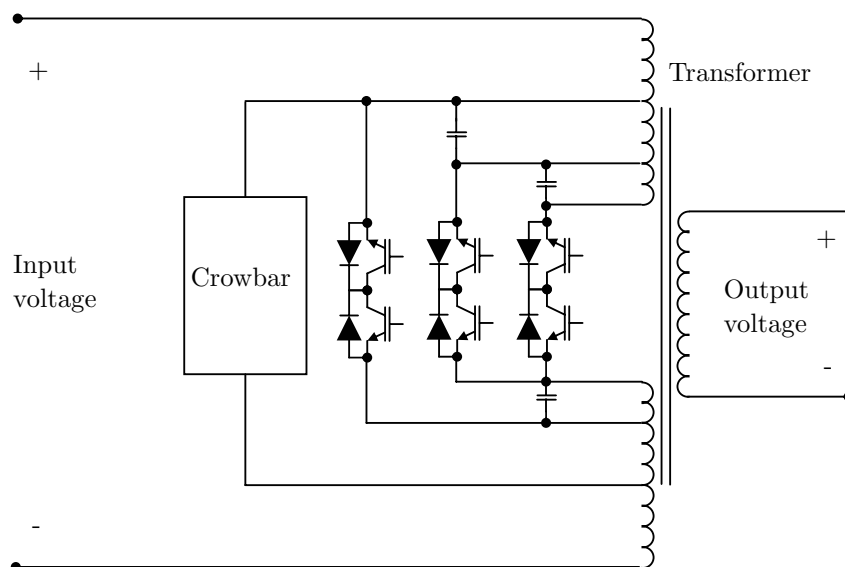


Figure 2.2: Topology proposed in [9, 7, 8]. Taken from [59].

The Chinese have recently come out with a new family of single-stage three-level AC choppers based on a capacitor-clamped base cell[36]. The buck topology of this family is shown in Fig. 2.3.

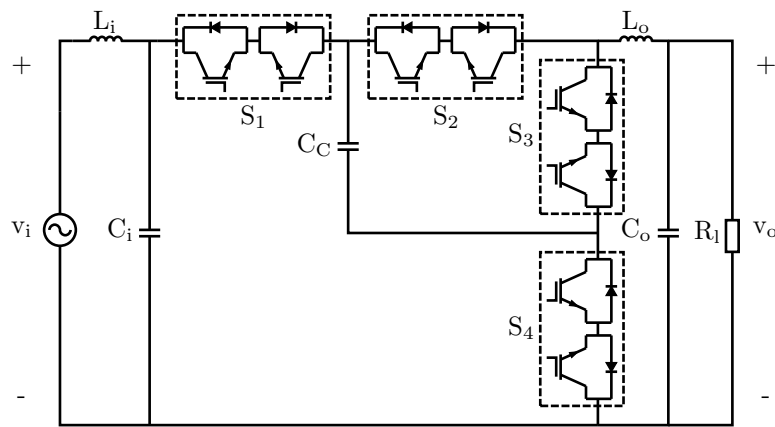


Figure 2.3: Buck topology of capacitor-clamped base cell design.

This design makes use of the general AC-AC chopper type circuit (as shown in Fig. 2.4), with the addition of input- and output filters, the clamped-capacitor C_C , and bi-directional IGBT pairs for every IGBT used in the standard cell.

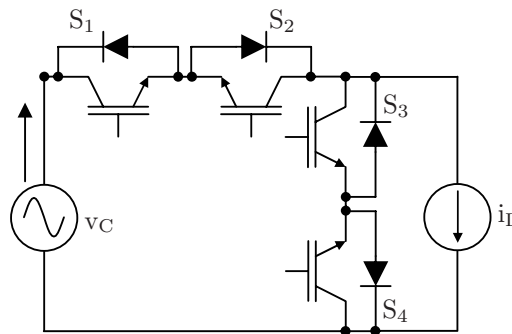


Figure 2.4: A standard AC-AC converter cell. Taken from [59, p. 55].

The originators of the base-clamped capacitor topology make claim to properties such as lower voltage stress on the power switches, bidirectional power flow, low total harmonic distortion of the output voltage, and high input power factor.[36]

The drawbacks of this system include its complexity and the increased number of switching elements. The three level operation with the addition of the clamped-capacitor, as well as the inherent non-symmetry of the topology with respect to the AC input voltage cause significant modelling (and hence control) effort.

2.4 Proposed topology

The proposed topology takes the form of an autotransformer, with multiple *regulated* series windings stacked in a series output configuration. This topology is specifically aimed at medium voltage (1 – 44kV) distribution lines. The regulator is required to be able to regulate the input voltage to up to 110% of its under-voltage value. The initial prototype was designed to operate on 11kV distribution lines, and was then modularized to allow for higher input voltages. This is done by stacking multiple regulators in series on an appropriately designed autotransformer. In any case, the design of the voltage regulator module stays the same and regulates the same input voltage. Only the transformer's number of series windings and winding-ratios need to be adapted for higher line voltages. The windings-ratio between the primary winding and any series winding is chosen such that the voltage over each regulator input does not exceed 635 V. This is 10% of the line-to-neutral (LN) voltage

of an 11 kV distribution line. The current system operates two regulators in series and is shown in Fig. 2.5. It is therefore suitable for 22kV distribution lines, where each regulator can regulate 5% of the LN voltage.

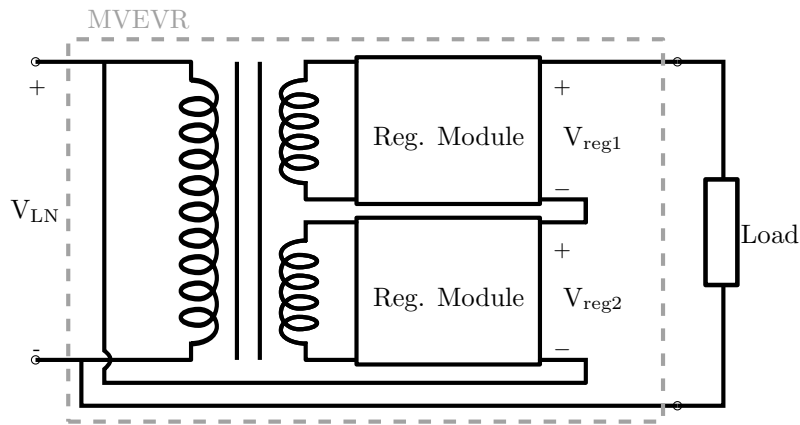


Figure 2.5: Proposed series-stacked autotransformer setup.

The topology of each regulator as in Fig. 2.6 was first proposed and investigated by [59]. Here the series winding is modelled by a voltage source, v_i and equivalent impedances, L_i and R_i . A linear, inductive load is assumed.

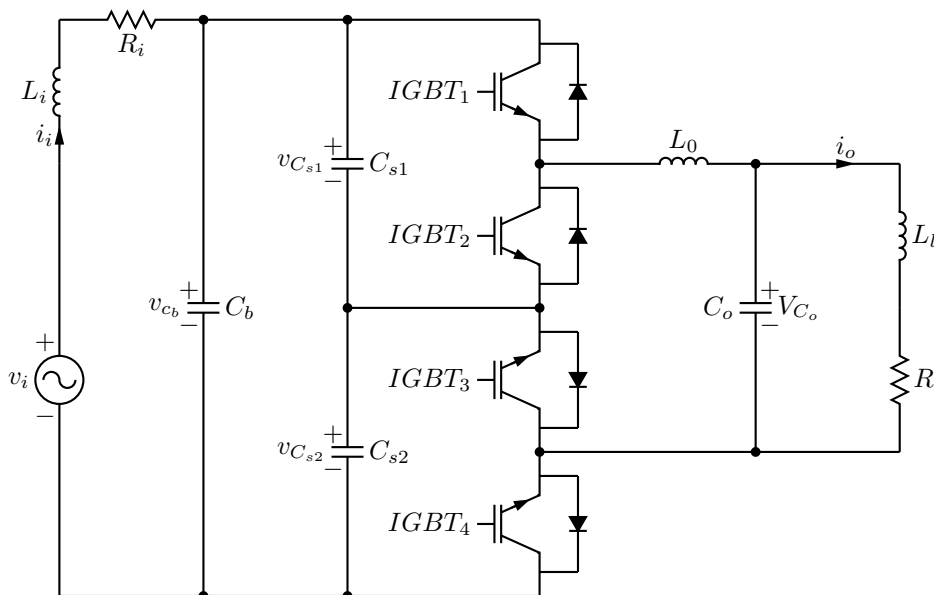


Figure 2.6: Proposed MVEVR topology.

The proposed topology is a type of differential AC-AC converter[59, p. 49]. A suitable commutation scheme for this topology is to have IGBTs 3 and 4 conducting in the positive half of the input voltage period, while IGBTs 1 and 2 fire complimentary. This effectively shorts out C_{s2} from the model during this time, and the circuit reduces to a synchronous buck converter with bi-directional power-flow. During the negative half of the input voltage period, IGBTs 1 and 2 remain switched on, while IGBTs 3 and 4 fires complimentary. This effectively shorts out C_{s1} from the model during this time, and the circuit again reduces to a synchronous buck converter with bi-directional power-flow.

In both cases, the resultant “reduced” circuit is exactly the same, and a beautiful form of topological symmetry with respect to the input voltage is established. This greatly simplifies modelling (and hence also control),

as the number of switching states is effectively reduced from four, as in the case of the general AC-AC converter cell, to two in the differential case.

2.5 Robust Control

2.5.1 Robust control schemes

Robust control is a branch of control theory that aims to minimize or eliminate the effect of model uncertainties and external disturbances on control performance. System performance is to be maintained so long as uncertainties and disturbances remain within some pre-defined boundaries.

Robustness with respect to nonlinearities, uncertainties, and exogenous perturbations can be approached in different ways. Linear control techniques aim to do this with very large feedback gains. If the gain is large enough, just about any disturbance or model discrepancy will be minimized. Non-linear control techniques can leverage non-linearities present in the system to achieve system behaviour that is robust and that would otherwise be unattainable. This section aims to provide a basic overview of robust control techniques. These techniques can be used individually or in combination.

Sliding Mode Control

Sliding mode control (SMC) is a type of variable structure control (VSC), pioneered by S.V. Emelyanov and several others in the Soviet Union during the 1950's. This control technique is specifically suitable for systems described by differential equations with discontinuous right-hand sides (non-linear systems). This includes power electronic systems, where discontinuities are introduced into the system by the switching of power transistors.

The control action is inherently discontinuous and, according to a pre-defined control switching law, causes the system to rapidly change between different substructures when the system state is on a desired manifold in the state space. The switching action constrains the system state trajectory to this *sliding manifold* as it moves toward a desired equilibrium position. Fig. 2.7 depicts the state trajectory of a second order system in the phase plane. An initial reaching phase leads to a sliding action on the sliding manifold (which in this case is a line) towards the equilibrium point.

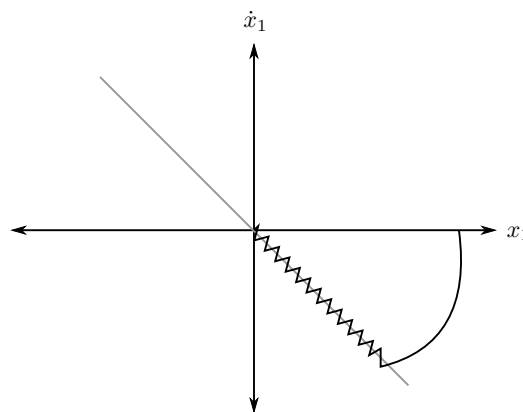


Figure 2.7: A typical phase portrait example of sliding mode control for a second order system.

The design of the sliding manifold determines the system's dynamic behaviour, and as long as the state trajectory remains on this manifold, robustness, and theoretically, even invariance to matched uncertainties and

disturbances can be achieved. Various papers provide comprehensive overviews of sliding mode control theory and applications, such as [55, 31, 15, 6, 64]. Helpful books on the topic exist, such as [18, 57], and pertaining specifically to power electronic circuits, [47, 23] was found to be very valuable. Some excellent application examples of SMC on DC-DC buck converters were found such as [39],[23, p. 8-9], and [34].

\mathcal{H}_2 and \mathcal{H}_∞ Methods

This technique was developed by Duncan McFarlane and Keith Glover of Cambridge University. This linear technique utilises computer-aided algorithms to minimize the sensitivity of a system over its frequency spectrum. Possible uncertainties and disturbances are lumped into one vector, while control outputs are lumped into another. The desired performance specifications are achieved by *loop shaping*. The closed-loop transfer function is weighted with, possibly frequency dependent, weights. These weights are then iteratively optimised with software to minimize the effect of uncertainties and disturbances.[25, p. 642] Some advantages of \mathcal{H}_∞ loop shaping is

- Commercial software is available to do the difficult maths.
- Can be implemented on multiple-input multiple-output (MIMO) system.
- Standard transfer functions and state-space methods can be used.
- The resulting robust controller needs not be tuned to exact parameter values at every installation.

Adaptive Control

Model-based control techniques rely on the accuracy of the model for generating appropriate control actions. If the modelled process changes over time, a discrepancy develops between a fixed-parameter model and the process itself. Robust control techniques generally establish bounds on these uncertainties, and guarantees control performance under a fixed control law when the system parameters vary within the bounds. In adaptive control, the control parameters are adjusted on-line to match changing properties in the control processes[25, p. 661]. The control law is thus adapted, negating the need for stringent boundaries on uncertainties. This makes adaptive controllers effective in controlling uncertain systems where no clear boundaries for uncertainties exist.

Two popular implementations of adaptive control is *self-tuning control* and *model reference adaptive system* (MRAS) control. The former technique utilizes a control law based on system parameters, but provides robustness by online estimation of uncertain parameters. The latter technique employs two control loops. The inner loop is simply a feedback loop from the process output to the controller. The outer loop is used to adapt the controller parameters based on a comparison between system performance and the desired system performance. This desired performance is estimated by a *reference model*. The challenge is to find an algorithm that is suitable for adjusting the control parameters in a way that leads to stable system with the desired performance[25, p. 589]. An conceptual diagram of an MRAS is shown in Fig. 2.8.

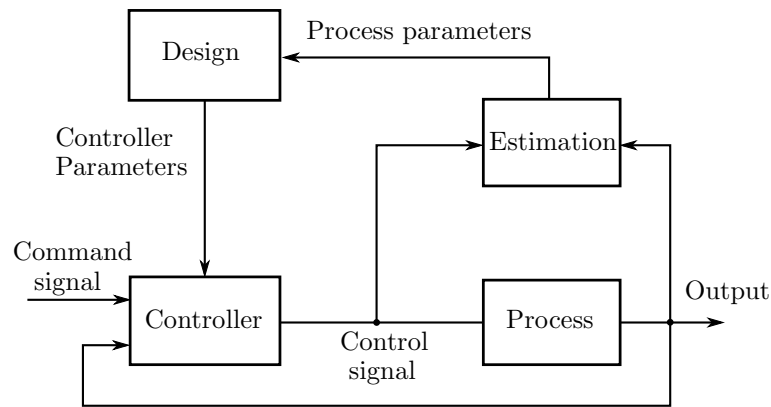


Figure 2.8: Model reference adaptive system. Taken from [25]

In [22], good robustness and dynamic performance of a DC-DC buck converter was achieved with an adaptive analogue current mode control scheme. In [10] adaptive control is combined with fuzzy control to produce a fuzzy model reference adaptive controller. This controller was designed to minimise harmonics introduced by power converters toward the source side, as well as improving the power factor.

With the advantage of robustness comes the trade-off of increased controller complexity. Besides having to devise a suitable adaptation algorithm, the designer is faced with a more challenging problem to prove stability and analyse performance for these time-varying and non-linear systems.

Neural Networks

One way of dealing with the problem of control of plants with uncertain models is to simply avoid modelling the uncertainties altogether. Artificial neural networks (ANN) can be used to approximate any continuous function with an arbitrary degree of accuracy. ANN are mechanisms for capturing statistical patterns and relationships in an information flow. The network consists of interconnected sets of nodes, arranged in various processing layers (refer to Fig. 2.9). The interconnections have adjustable weights. Weight factors in-between nodes are changed as external information flows through them, either in a separate learning phase, where exemplary system input and output pairs are used to “train” the network, or during online operation, where a learning rule evaluates the strength of the output and adjusts the weights accordingly.[25, p. 720]

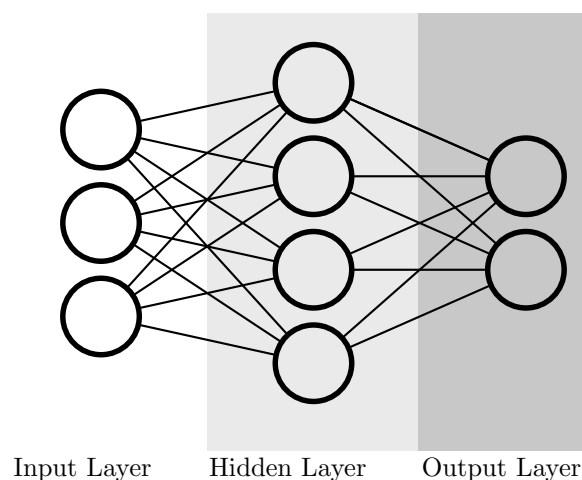


Figure 2.9: Artificial neural network with different node groupings.

The ability of ANN to approximate a plant's function can be conveniently used in techniques such as input-output feedback linearisation. In this technique, feedback is applied to an inherently non-linear plant in such a way as to exactly cancel out the known non-linearities. This renders the resulting plant behaviour linear, and control objectives can be enforced using linear techniques. Without the use of ANN, the designer is reliant on accurate mathematical models of the plant non-linearities in order to develop a feedback law for exact cancellation. However, ANN can be used to accurately approximate any non-linearities present for good cancellation. The designer is left with the challenge of finding a suitable learning procedure to adequately train the ANN for good function approximation. [25, p. 720]

A neural network based approach to the control of a DC-DC buck converter is presented in [32], and an FPGA-based adaptive recurrent fuzzy neural network control system is developed in [30] also for a buck converter.

Fuzzy Control

Another control technique that is useful for plant control without the need for parameterised models is *fuzzy control*. This technique approaches control in an *approximating* way, very similar to the way humans would operate a complex plant without needing an exact mathematical model of it. The term 'fuzzy' refers not to a lack of mathematical rigour, but rather to the algorithm's ability to deal with fuzzy concepts. A temperature control system on a complex plant would, for example, identify a certain temperature measurement as *mild*, *hot*, or *very hot*, and perform an appropriate control action according to some desired temperature state. The fuzzy control system thus operates on the basis of *linguistic variables*, where plant measurements are *fuzzified* by classifying it into pre-defined *fuzzy sets* (like hot, mild, cold) by use of *membership functions*.

In classical logic, propositions are either *true*, or *false* ('1' or '0'). In fuzzy logic, propositions can be more true or less true, taking on a range of continuous values between zero and one. For a voltage regulator, then, a "very low" input voltage would require a "very large" additive correction. *Crisp* system inputs (like voltage measurements) would be *fuzzified* and assigned to a fuzzy set, such as "very low", or "high", by membership functions. The system would approximate an appropriate reaction based on a *rule base* in the form of if-then-else statements, such as

$$\text{IF } e(k) \text{ is Positive and } v(k) \text{ is Positive THEN } \Delta u(k) \text{ is Positive,} \quad (2.1)$$

where $e(k)$ is the voltage error, $v(k)$ is the measured input voltage, and $u(k)$ is the corrective additive voltage.

This technique is useful for inferring proper control rules when dealing with very complex systems or uncertain systems for which no accurate model is available.

Combination of different robust control techniques

In [19], a comparison of fuzzy, PI and fixed frequency sliding mode controllers is made. It should be noted, however, that it is not necessary to choose strictly one of the mentioned control techniques for robust control. In many applications, a combination of more than one is used, fuzzy model reference adaptive controllers [10], adaptive sliding mode controllers [46, 20, 38], adaptive fuzzy sliding mode controllers [44, 35, 13, 26, 27], and fuzzy-neural sliding mode controllers in [29, 37, 60, 63, 65]. It is seen that sliding-mode control is found in many of these combinations. In [61], a combination of \mathcal{H}_∞ tracking-based sliding mode controller is developed via an adaptive fuzzy-neural approach. This prevalent practice of employing different techniques in unison is a strong motivation to gain a basic understanding of the different robust control methods.

For this thesis, sliding mode control is pursued as the basis of a solution for robust control. This decision was motivated by the fundamental suitability of SMC for power switching systems (systems with discontinuities in the right-hand side of the differential equations). Another motivation was the wealth of literature available on SMC applied to power converters, especially DC-DC converters. After a basic solution using SMC is found, control performance can be further optimised with adaptive, neural, fuzzy, or a combination of these techniques in additional studies.

SLIDING MODE CONTROL THEORY

“Goals allow you to control the direction of change in your favor. ”

- Brian Tracy

3.1 Introduction to Sliding Mode Control

S.V. Emelyanov and several core researchers from the Soviet Union first proposed variable structure control (VSC), a form of discontinuous nonlinear control, in the early 1950's. The plant under consideration was a linear second-order system modelled in phase variable form [31].

Since then, VSC has been developed and applied to a whole range of different classes of systems, in which the main mode of operation is sliding mode control (SMC). Another mode of VSC is *bang-bang* control. The range of applicable systems includes nonlinear systems, multi-input/multi-output systems, discrete-time systems, and stochastic systems [31].

In variable structure systems, the plant consists of multiple sub-structures with unique behavioural properties belonging to each sub-structure. VSC switches between the substructures in such a way that the performance of the plant exhibit properties that are not found in any one of the substructures by itself. VSC can in this way be used, for example, to obtain a stable plant from substructures which are all inherently unstable.

In sliding mode control, a high-speed switching control law is employed to drive the variable structure system's state trajectory onto a user specified surface in the state space (called the sliding or switching surface). In the multi-input case, multiple sliding surfaces are defined and the state trajectory is forced to move along the intersections of these surfaces. Once this interaction is reached, the states are forced by the control law to remain on it with ideally zero magnitude error for all subsequent time [15]. By proper design of the sliding surface, SMC can achieve required control specifications in terms of stability, tracking, regulation, etc. [15].

Sliding mode control exhibits superior performance compared to linear control schemes (such as classical PWM control) in its robustness, system order reduction, and better transient response. Of these properties, the robustness with respect to matched plant uncertainty and exogenous disturbances¹ stands out as highly desirable. In some cases complete invariance to these phenomena is achieved [31]. This means that, when restricted to the sliding surface, the plant's behavioural dynamics are completely determined by the switching hypersurface parameters even in the midst of uncertainties and disturbances.

In order to achieve invariance in systems under linear control, accurate and dynamic models of disturbances for unknown initial conditions are required. Sliding mode control, in contrast, requires no such detailed knowledge, but only the range of possible variation [57, p. VIII]. In that case, the sliding surface(s) and switching law can possibly be designed in such a way that the sliding mode exists regardless of the disturbances or uncertainties present.

¹Uncertainties and disturbances are referred to as “matched” when the *perturbation matching condition* holds, as presented in Eq. 3.36 later in this chapter.

Reduction of the system order is brought about only while the system is restricted to the sliding surface (which is a subset of the state space). For a system of order n , with m independent inputs, the sliding mode on the intersection of m hypersurfaces will result in a reduced order behaviour of order $n - m$ [6].

The transient response of the system in sliding mode is determined entirely by the design of the switching surface. The property of order reduction can also serve to improve the transient response, such as when a second-order plant is caused to exhibit a first order transient response.

Sliding mode controllers are computationally efficient[5] and, although in the ideal case it is required that all the state variables are sensed, only very simple algorithms are necessary for practical implementations. This is a big advantage, especially in large-order systems, where other control techniques, such as model predictive control, can become very computationally intensive.

In systems where the plant's control actuators are designed to operate purely in a switching mode (such as in power electronic systems), the discontinuous switching nature of SMC is highly appropriate and naturally suitable [28],[47]. Instead of devising a continuous control signal, whose mean value is equal to the desired discontinuous control, a more natural way is to use an algorithm that is fundamentally oriented towards discontinuous behaviour [57, p. VI].

Ideal sliding mode conditions require infinitely high switching frequencies, which do not exist in real systems. This results in high frequency oscillations about the switching surface, generally referred to in literature as "chattering" [6]. Various techniques are used to reduce and even eliminate the effect of chattering, but these have negative implications for the robustness of the system.

The sliding mode design approach conveniently allows the control problem to be divided into two subsections. Firstly the sliding function is designed to satisfy specifications on the system's dynamic performance. Secondly, a control law is selected which will constrain the system state on the sliding surface and cause the sliding function to be zero [18, preface]. This approach allows the initial problem in the design to be decoupled from performance in the steady state [57, p. VI]. The control law is employed to create the sliding mode, while the dynamic behaviour is determined by a choice of appropriate sliding functions [18, p. 5].

3.2 Important Concepts

This section will discuss some of the most important theoretical aspects of sliding mode control. Most of the theory presented is then applied to a control example at the end of the chapter.

Consider a generalized non-linear time invariant system with m inputs given in the form

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, t) + \mathbf{g}(\mathbf{x}, t) u, \quad (3.1)$$

where $\mathbf{x} \in \mathbb{R}^n$, t is time, \mathbf{f} and \mathbf{g} are both smooth, infinitely differentiable *vector fields* defined over the tangent space to \mathbf{x} , and u is the discontinuous control variable with value determined by a specific control law. The vector fields \mathbf{f} and \mathbf{g} are referred to as the *drift vector field* and the *control input field*, respectively.[47, p. 64]

A central concept in sliding mode control is that of a *sliding surface* or *sliding manifold*. The sliding surface is made up of the entire set of state vectors, S , that satisfy the algebraic restriction $\sigma(\mathbf{x}) = 0$, where σ is the *sliding function*. The sliding surface is formally defined as[47, p. 64]

$$S = \{\mathbf{x} \in \mathbb{R}^n \mid \sigma(\mathbf{x}) = 0\}. \quad (3.2)$$

The sliding function is defined in terms of the *state variables*, \mathbf{x} , in such a way that, when $\sigma(\mathbf{x}) = 0$, the

specifications of the dynamic behaviour of the system is satisfied. When the sliding function is continuously forced to be zero, the system's representative point (RP) is constrained to the sliding surface, and the system is said to be in *sliding mode*.

In order to reach, and remain on, the sliding surface, an appropriate control law, u , has to be chosen. The control law is defined in general terms as [47, p. 69]

$$u = \begin{cases} u^+ & \text{for } \sigma(x) > 0 \\ u^- & \text{for } \sigma(x) < 0 \end{cases} . \quad (3.3)$$

For a single-switch power system, where the switching action is the control variable, the following switching law is very prevalent in literature:

$$u = \begin{cases} 1 & \text{for } \sigma(x) > 0 \\ 0 & \text{for } \sigma(x) < 0 \end{cases} , \quad (3.4)$$

where the set $\{1, 0\}$ represents the switch's binary behaviour.

When the system RP is "above" or "below" the sliding surface, the control action should cause the RP to move towards the sliding surface. Once it reaches the surface, the ideally infinite fast control action constrains the RP to the sliding surface. In real systems with friction, inertia, and possible restrictions on the switching frequency this is of course not practical. In these cases the RP will be allowed to cross towards the "other side" of the sliding surface within an arbitrarily small boundary before the control action forces the RP to return towards the sliding surface.

3.2.1 Conditions for Sliding Mode

There are three conditions that must hold for sliding-mode control to be realizable [23, p. 8-5]:

- *Existence Condition* : The trajectories of the two substructures are directed toward the sliding line when they are close to it.
- *Reachability Condition*: For any initial condition, the system trajectories must reach the sliding surface within finite time.
- *Stability Condition*: The system must remain stable when confined to, and moving along, the sliding surface.

3.2.2 Existence Condition

A sufficient condition for the existence of the sliding mode is that the total time derivative of the sliding function has - at any time - opposite sign to the value of the sliding function itself. If this condition is satisfied, the sliding function will always be directed to a value of zero. If the function evaluates to a positive value, it will have a negative rate of change, causing the value to become less positive. If the function has a negative value, it will have a positive rate of change, causing the value to become less negative. This condition is expressed as follows:

$$\sigma(\mathbf{x}) \cdot \dot{\sigma}(\mathbf{x}) \leq 0. \quad (3.5)$$

This stems from Lyapunov stability theory. Consider the Lyapunov function candidate:

$$\mathbf{V}(\boldsymbol{\sigma}(\mathbf{x})) = \frac{1}{2} \boldsymbol{\sigma}^T(\mathbf{x}) \boldsymbol{\sigma}(\mathbf{x}) = \frac{1}{2} \|\boldsymbol{\sigma}(\mathbf{x})\|_2^2, \quad (3.6)$$

where $\|\cdot\|_2$ denotes the Euclidean norm, and $\|\boldsymbol{\sigma}(\mathbf{x})\|_2$ represents the distance away from the sliding surface where $\boldsymbol{\sigma}(\mathbf{x}) = 0$. A sufficient condition for the existence of the sliding mode is then that the derivative of the Lyapunov function must be negative-definite.

The derivative of the Lyapunov function is expressed as:

$$\dot{\mathbf{V}}(\boldsymbol{\sigma}) = \frac{\partial \mathbf{V}}{\partial t} + \frac{\partial \mathbf{V}}{\partial \boldsymbol{\sigma}} \cdot \frac{d\boldsymbol{\sigma}}{dt}, \quad (3.7)$$

and because $V(\boldsymbol{\sigma})$ has no direct time-dependency, $\frac{\partial \mathbf{V}}{\partial t} = 0$, and therefore

$$\dot{\mathbf{V}}(\boldsymbol{\sigma}) = \underbrace{\frac{\partial \mathbf{V}}{\partial \boldsymbol{\sigma}}}_{\boldsymbol{\sigma}^T} \underbrace{\frac{d\boldsymbol{\sigma}}{dt}}_{\dot{\boldsymbol{\sigma}}} < 0. \quad (3.8)$$

In the scalar case, where $\boldsymbol{\sigma}$ is one dimensional, Eq. 3.8 reduces to Eq. 3.5. Since control will only be applied to single-input systems in this thesis, only the one-dimensional case will be considered.

The derivative of the sliding function in Eq. 3.5 refers to the total derivative with respect to time is

$$\dot{\boldsymbol{\sigma}}(\mathbf{x}) = \frac{\partial \boldsymbol{\sigma}}{\partial t} + \frac{\partial \boldsymbol{\sigma}}{\partial \mathbf{x}} \cdot \frac{d\mathbf{x}}{dt}, \quad (3.9)$$

but since, in most cases, $\boldsymbol{\sigma}$ has no direct time dependency², $\frac{\partial \boldsymbol{\sigma}}{\partial t} = 0$, and therefore

$$\dot{\boldsymbol{\sigma}}(\mathbf{x}) = \frac{\partial \boldsymbol{\sigma}}{\partial \mathbf{x}} \cdot \frac{d\mathbf{x}}{dt} = \nabla \boldsymbol{\sigma} \cdot \dot{\mathbf{x}}, \quad (3.10)$$

where $\nabla \boldsymbol{\sigma}$ is the gradient of the sliding function, and is defined as

$$\nabla \boldsymbol{\sigma} = \left(\frac{\partial \boldsymbol{\sigma}}{\partial \mathbf{x}_1}, \dots, \frac{\partial \boldsymbol{\sigma}}{\partial \mathbf{x}_n} \right). \quad (3.11)$$

The derivative of the state variable vector, \mathbf{x} , can be conveniently expressed in terms of Eq. 3.1.

3.2.3 Reachability Conditions

The hitting or reachability condition is concerned with ensuring that, when the system state is found to be away from the sliding surface, the control system will be able to drive the system towards the sliding surface from any position in the state space.

With the switching law defined as

$$u = \begin{cases} u^+ & \text{for } \boldsymbol{\sigma}(\mathbf{x}) > 0 \\ u^- & \text{for } \boldsymbol{\sigma}(\mathbf{x}) < 0 \end{cases}, \quad (3.12)$$

let \mathbf{x}_{ss}^+ and \mathbf{x}_{ss}^- be the steady-state RPs corresponding to the inputs u^+ and u^- , respectively. Then a simple sufficient condition for reaching the sliding surface is given by [23, p. 8-6]

$$\mathbf{x}_{ss}^+ \varepsilon \boldsymbol{\sigma}(\mathbf{x}) < 0, \quad \mathbf{x}_{ss}^- \varepsilon \boldsymbol{\sigma}(\mathbf{x}) > 0. \quad (3.13)$$

²If $\boldsymbol{\sigma}$ is defined in such a way as to have a direct time dependency, then Eq. 3.9 cannot be simplified.

Quoting from [23, p. 8-6] regarding reachability,

“In other words, if [referring to the phase portrait of a second order system] the steady-state point for one substructure belongs to the region of the phase space reserved to the other substructure, then sooner or later the system RP will hit the sliding surface.”

η -Reachability

In cases of asymptotic convergence, σ slows down too much as it approaches the sliding surface for finite time convergence. In this case, the condition $\sigma \cdot \dot{\sigma} < 0$ will still hold, but the behaviour will be slow. To ensure reaching of the sliding surface in finite time, additional constraints can be placed on the reaching condition, such as the η -reachability constraint:

$$\sigma \cdot \dot{\sigma} < \eta |\sigma|, \eta > 0. \quad (3.14)$$

As illustrated in Fig. 3.1, this condition enforces an arbitrary minimum rate of convergence toward the sliding surface, even when close to it ($\sigma \simeq 0$).

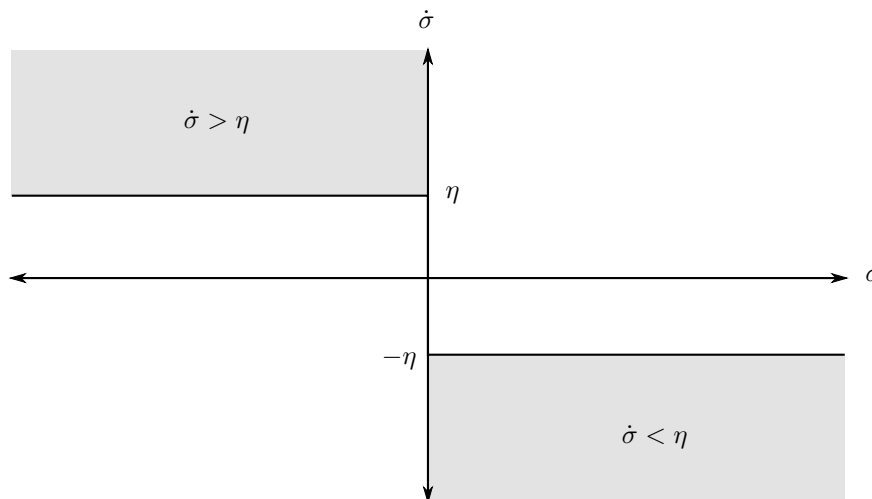


Figure 3.1: Illustration of the η -reachability condition. The condition is satisfied in the grey areas.

Reaching-Law Approach

Where the η -reachability condition enforces a minimum rate of convergence toward the sliding surface, other *reaching laws* are used to specifically prescribe the convergence trajectory [31]. The constant rate, constant and proportional rate, and power rate reaching laws are listed below, and illustrated in Figs. 3.2-3.4.

- Constant rate reaching law

$$\dot{\sigma} = -k \cdot \text{sgn}(\sigma) \quad (3.15)$$

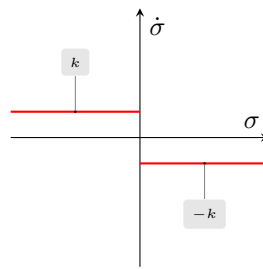


Figure 3.2: Illustration of the constant rate reaching law.

- Constant and proportional rate

$$\dot{\sigma} = -q\sigma - k \cdot \text{sgn}(\sigma) \quad (3.16)$$

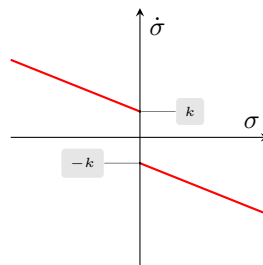


Figure 3.3: Illustration of the constant and proportional rate reaching law.

- Power rate reaching law

$$\dot{\sigma} = -k |\sigma|^\alpha \cdot \text{sgn}(\sigma), \quad 0 < \alpha < 1 \quad (3.17)$$

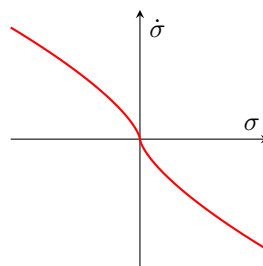


Figure 3.4: Illustration of the power rate reaching law.

With SMC, not only can the dynamic response of the system be prescribed while on the sliding surface, but by use of reaching laws, the convergence trajectory towards the sliding surface can also be prescribed. Thus the behaviour of the system can be controlled completely.

3.2.4 System Description in Sliding Mode : Equivalent Control

The concept of equivalent control was developed by Vadim Utkin and is presented in [57, p. 14]. The equivalent control represents the smooth control action that would constrain the system to the ideal sliding manifold. This is not the discontinuous control signal that is actually applied to the system, but can be thought of as the average form of the discontinuous control signal where the switching ripple is removed [18, (p. 7)].

The equivalent control for the system in Eq. 3.1 may then be written by solving for $\dot{\sigma} = 0$:

$$\dot{\sigma} = \frac{\partial \sigma}{\partial \mathbf{x}} \cdot \frac{d\mathbf{x}}{dt} \quad (3.18)$$

$$= \frac{\partial \sigma}{\partial \mathbf{x}} \cdot \overbrace{(\mathbf{f}(\mathbf{x}, t) + \mathbf{g}(\mathbf{x}, t) u_{eq})}^{\dot{\mathbf{x}}} \quad (3.19)$$

$$= L_{\mathbf{f}}\sigma(\mathbf{x}) + L_{\mathbf{g}}\sigma(\mathbf{x}) \cdot u_{eq} \quad (3.20)$$

$$= 0, \quad (3.21)$$

where u_{eq} represents the *equivalent control* input and $L_{\mathbf{f}}\sigma(\mathbf{x})$ and $L_{\mathbf{g}}\sigma(\mathbf{x})$ stands for the *Lie derivatives* with respect to \mathbf{f} and \mathbf{g} respectively [25, p. 719]. The Lie derivatives are defined as

$$L_{\mathbf{f}}\sigma(\mathbf{x}) \triangleq \sum_{i=1}^n \frac{\partial \sigma(\mathbf{x})}{\partial x_i} f_i(\mathbf{x}) \quad (3.22)$$

$$L_{\mathbf{g}}\sigma(\mathbf{x}) \triangleq \sum_{i=1}^n \frac{\partial \sigma(\mathbf{x})}{\partial x_i} g_i(\mathbf{x}). \quad (3.23)$$

Assuming that $\frac{1}{L_{\mathbf{g}}\sigma(\mathbf{x})}$ exists, the equivalent control is

$$u_{eq} = -\frac{L_{\mathbf{f}}\sigma(\mathbf{x})}{L_{\mathbf{g}}\sigma(\mathbf{x})}. \quad (3.24)$$

Even though the actual control of the system is not continuous, the system behaviour will approach the behaviour with the continuous equivalent control as the switching frequency tends to infinity. The equivalent control can be thought of as a type of average of the discontinuous control when the system is in sliding mode. This can be shown by passing the discontinuous control signal through a low pass filter [18].

The system behaviour on the sliding surface can now be expressed by substituting Eq. 3.24 into Eq. 3.1, the general expression of our discontinuous system :

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, t) - \mathbf{g}(\mathbf{x}, t) \frac{L_{\mathbf{f}}\sigma(\mathbf{x})}{L_{\mathbf{g}}\sigma(\mathbf{x})}, \quad (3.25)$$

and knowing that $L_{\mathbf{f}}\sigma(\mathbf{x}) = \frac{\partial \sigma}{\partial \mathbf{x}} \mathbf{f}(\mathbf{x}, t)$,

$$\dot{\mathbf{x}} = \left(I - \mathbf{g}(\mathbf{x}, t) \frac{1}{L_{\mathbf{g}}\sigma(\mathbf{x})} \frac{\partial \sigma}{\partial \mathbf{x}} \right) \mathbf{f}(\mathbf{x}, t) \quad (3.26)$$

$$= \mathbf{M}(\mathbf{x}, t) \mathbf{f}(\mathbf{x}, t), \quad (3.27)$$

where, as in [47, p. 66], $\mathbf{M}(\mathbf{x}, t)$ is proposed to be a *projection operator* over the tangent space to S , along the span of $\mathbf{g}(\mathbf{x}, t)$. Quoting from [47, p. 66],

“The operator $\mathbf{M}(\mathbf{x}, t)$ projects any smooth vector field defined in the tangent space of \mathbb{R}^n over

the tangent subspace to the manifold S in a parallel fashion to the $\{\text{span } \mathbf{g}(\mathbf{x}, t)\}$ or in the direction of the control input field $\mathbf{g}(\mathbf{x}, t)$.”

Take note that the projection operator is always of less than full rank. This is because the system is in sliding mode and is constrained to the sliding surface, which is a subset of the state space. For a single input system, this results in an order reduction of 1. In the case of multi-input systems, with m independent inputs, the state trajectory moves along the intersection of m hypersurfaces, resulting in the system behaviour being reduced by order m .

3.2.5 Disturbance Rejection

In order to demonstrate the property of disturbance rejection on the sliding mode, consider here a nonlinear system with additive perturbation, i.e.,

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, t) + \mathbf{g}(\mathbf{x}, t)u + \mathbf{d}(\mathbf{x}, t) \quad (3.28)$$

where $\mathbf{d}(\mathbf{x}, t) \in \mathbb{R}^n$ is an unknown and bounded disturbance. We assume that it is possible to create a sliding mode on the sliding surface, \mathbf{S} , despite the presence of the disturbance. When the system representative point (RP) hits the sliding surface, the control law will enforce the sliding function towards zero and thereby constrain the system RP to the sliding manifold.

By substituting Eq. 3.28 into Eq. 3.10 and taking the result to be zero (on the sliding manifold), the equivalent control can be solved:

$$\frac{\partial \sigma}{\partial \mathbf{x}} \dot{\mathbf{x}} = L_{\mathbf{f}}\sigma(\mathbf{x}) + L_{\mathbf{g}}\sigma(\mathbf{x})u_{eq} + L_{\mathbf{d}}\sigma(\mathbf{x}) = 0 \quad (3.29)$$

Once again, assuming that $\frac{1}{L_{\mathbf{g}}\sigma(\mathbf{x})}$ exists, one can derive the expression for the equivalent control:

$$u_{eq} = -\frac{L_{\mathbf{f}}\sigma(\mathbf{x}) + L_{\mathbf{d}}\sigma(\mathbf{x})}{L_{\mathbf{g}}\sigma(\mathbf{x})}. \quad (3.30)$$

The system behaviour is expressed by substituting Eq. 3.30 into Eq. 3.28 such that

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, t) + \mathbf{g}(\mathbf{x}, t) \frac{L_{\mathbf{f}}\sigma(\mathbf{x}) + L_{\mathbf{d}}\sigma(\mathbf{x})}{L_{\mathbf{g}}\sigma(\mathbf{x})} + \mathbf{d}(\mathbf{x}, t). \quad (3.31)$$

This equation is factorised in terms of $\mathbf{f}(\mathbf{x}, t)$ and $\mathbf{d}(\mathbf{x}, t)$ to obtain

$$\dot{\mathbf{x}} = \left(I - \mathbf{g}(\mathbf{x}, t) \frac{1}{L_{\mathbf{g}}\sigma(\mathbf{x})} \frac{\partial \sigma}{\partial \mathbf{x}} \right) \mathbf{f}(\mathbf{x}, t) + \left(I - \mathbf{g}(\mathbf{x}, t) \frac{1}{L_{\mathbf{g}}\sigma(\mathbf{x})} \frac{\partial \sigma}{\partial \mathbf{x}} \right) \mathbf{d}(\mathbf{x}, t) \quad (3.32)$$

$$= \mathbf{M}(\mathbf{x}, t) \mathbf{f}(\mathbf{x}, t) + \mathbf{M}(\mathbf{x}, t) \mathbf{d}(\mathbf{x}, t). \quad (3.33)$$

It is seen in the expression above that the control input adjusts to disturbances to effectively cancel it out, but only when the disturbance vector is in the null space³ of $\mathbf{M}(\mathbf{x}, t)$ [47, p. 70], such that

$$\left(I - \mathbf{g}(\mathbf{x}, t) \frac{1}{L_{\mathbf{g}}\sigma(\mathbf{x})} \frac{\partial \sigma}{\partial \mathbf{x}} \right) \mathbf{d}(\mathbf{x}, t) = 0. \quad (3.34)$$

The system will only be invariant to exogenous perturbations or uncertainties if the disturbance field, $\mathbf{d}(\mathbf{x}, t)$, is in the span of the control input field, $\mathbf{g}(\mathbf{x}, t)$ [47, p. 70]. For our single input system this would mean that there

³The null space of \mathbf{M} , would be the set of all vectors, $\boldsymbol{\varepsilon}$, for which $\mathbf{M}\boldsymbol{\varepsilon} = \mathbf{0}$.

would have to exist a scalar function, $\alpha(\mathbf{x}, t)$, such that

$$\mathbf{d}(\mathbf{x}, t) = \alpha(\mathbf{x}, t)\mathbf{g}(\mathbf{x}, t). \quad (3.35)$$

When the disturbance vector is thus aligned with the control vector, invariance results. In this case the disturbance is called a “matched disturbance”, and the following condition *perturbation matching condition* holds [47, p. 70]:

$$\mathbf{d}(\mathbf{x}, t) \in \text{span}\{\mathbf{g}(\mathbf{x}, t)\}. \quad (3.36)$$

The concept of complete rejection of disturbances or uncertainties stands in contrast to control methods such as \mathcal{H}_2 and \mathcal{H}_∞ , where an attempt is made to *minimize* the transfer functions of the disturbances affecting the relevant outputs [18].

It should be noted, however, that the invariance property of SMC is technically only a theoretical concept in that it only holds if, along with the perturbation matching condition, the system RP can be effectively constrained to the sliding manifold. This would require zero delay in the switching components, and is scarcely realistic. In more practical systems the system RP is rather constrained to an arbitrarily small boundary region around the sliding surface. As the size of this region increases the system will to a large extent⁴ retain its robustness, but invariance will be lost.

3.2.6 Stability Condition

System stability can be evaluated in different ways, depending on the order of the system, and the implementation of the sliding mode control. These methods are mentioned in [23, p. 8-16] and will be briefly discussed in here.

For second order systems, phase portraits can be drawn to graphically reveal the motion of the state trajectory for any initial condition. The system would be stable if, once the sliding line is reached, the state trajectory moves towards a stable point along that line. This can be determined graphically.

For systems of higher order, phase portraits are not useful any more, and stability has to be analysed using mathematical procedures. Stability can easily be ensured from systems that can be expressed in controllable canonical form (also known as input-output decoupled or companion form), such as the second-order DC-DC buck converter. Stability is then ensured in the way that the sliding coefficients of the sliding function are chosen. A system in controllable canonical form can be expressed as follows:

$$\dot{x}_i(t) = x_{i+1}(t), \quad i = 1, 2, \dots, n-1 \quad (3.37)$$

$$\dot{x}_n(t) = f(\mathbf{x}, t) + g(\mathbf{x}, t) \cdot u(\mathbf{x}, t) \quad (3.38)$$

where $f(\mathbf{x}, t)$ and $g(\mathbf{x}, t)$ are scalar functions of \mathbf{x} and t , and $u(\mathbf{x}, t)$ is the control input. In the second order case ($n = 2$), if a linear sliding line is chosen, the sliding surface is represented by

$$\sigma(\mathbf{x}) = \mathbf{C}^T \mathbf{x} = c_1 x_1 + c_2 x_2 = 0. \quad (3.39)$$

From Eq. 3.37 and 3.37 it is then apparent that, on the sliding line, the system dynamics are completely described by:

⁴The measure of robustness will of course be contingent on the size of the boundary region.

$$\dot{x}_1 = -\frac{c_1}{c_2}x_1. \quad (3.40)$$

Stability can thus be guaranteed by choosing a positive values for c_1 and c_2 . The solution to the above differential equation shows that the system state will be exponentially regulated toward zero, with time constant $\frac{c_2}{c_1}$:

$$x_1(t) = x_1(0) \cdot e^{-\frac{c_1}{c_2}t}. \quad (3.41)$$

If, as with most power converters, the system cannot be written in canonical form, stability can be analysed using the expression of equivalent control (Eq. 3.24). This is done by first deriving an average model of the converter in question (like with the method proposed by Middlebrook and Cúk in [41]) and using that to form a transfer functions of the output variables versus the control signal. The equivalent control is then substituted for the continuous control signal, and the stability is evaluated in terms of gain margin and phase margin.

3.2.7 Chattering

In ideal systems, where discontinuous control actions can be actualised without any delay, the system motion can be perfectly constrained to the sliding surface. In practical systems, this is not the case. Mechanical actuators have inertia and friction and electronic switches such as power transistors in power systems have finite turn-on and turn-off times. In power electronics, more power is dissipated in the switching elements during switching than during normal conduction. This puts a limit on the switching frequency of the transistor, to prevent thermal overload and loss of system efficiency.

Imperfections in the switching process, such as delays and hysteresis, will cause high-frequency oscillations about the sliding surface as the system is unable to respond fast enough to control requirements. These high-frequency oscillations are referred to as *chattering*.

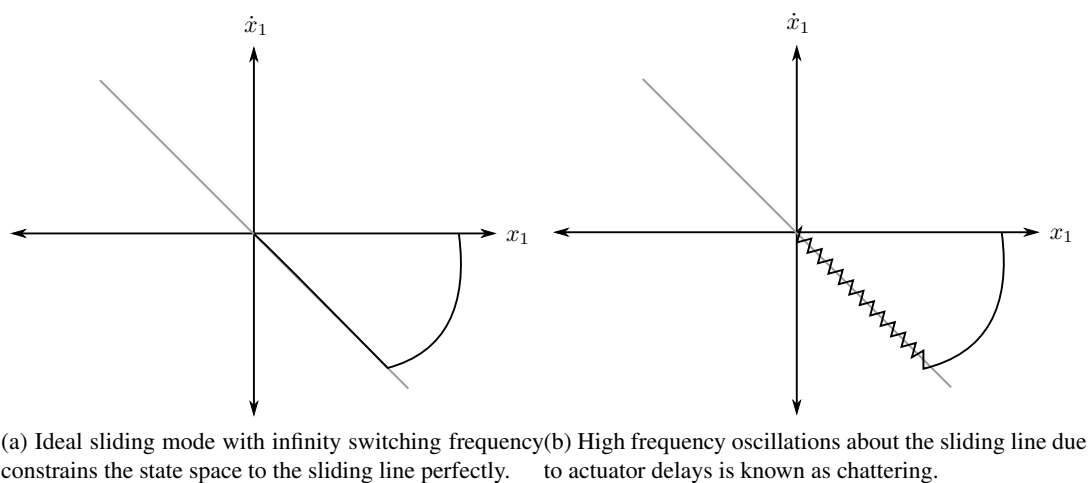


Figure 3.5: Ideal sliding mode vs sliding mode with chattering.

These high frequency oscillations can excite unmodelled and unwanted system characteristics and can also put excessive strain on the system's actuators. Various techniques [6, p. 3775] are used to reduce and even eliminate the effect of chattering, such as boundary layer control, smoothing of the discontinuous switching law, and modification of the system law to react to higher order derivatives [5] of the sliding function. In boundary layer control, the discontinuous control law is modified to constrain the system motion in the state

space to an arbitrarily small boundary layer about the sliding surface. These techniques do, however, reduce the robustness of the overall system.

The practice of allowing the system state trajectory to marginally deviate from the sliding surface is referred to in literature as “pseudo-sliding motion”. The system’s behaviour under pseudo-sliding mode control approximates the behaviour under ideal sliding mode control as the boundary layer size tends to zero. [18, p. 32]

3.2.8 Regulation Problems Vs. Tracking Problems

It is important to differentiate between regulation problems and tracking problems. In regulation problems, the control objective is to bring the system under consideration to some pre-defined equilibrium point. An example is any DC-DC power converter where the constant input voltage is regulated to an output voltage with a specified constant equilibrium value.

In tracking problems, the control objective is to cause the system under consideration to follow a time-varying reference signal. An example is a DC-AC voltage regulator (inverter) that generates a time-varying output signal according to an external sinusoidal reference. A tracking problem can, however, be transformed into a regulation problem by defining the system state, \mathbf{x} , in terms of the error between the reference signals and their corresponding measured or estimated signals. The objective then is to constantly regulate the tracking error towards an equilibrium of zero.

Even though it is straightforward to transform a tracking problem into a regulation problem, some complexities are never the less introduced into the design of the sliding mode controller. It is well known that the time derivatives of non time dependent quantities evaluate to zero. Therefore, in a “natural” regulation problem, the constant references disappear out of the derivative of the state space equations, $\dot{\mathbf{x}}$. In a “transformed” regulation problem, however, the time-varying references do not evaluate to zero upon differentiation and remain part of the sliding mode design problem. This can complicate the proof of existence and stability. Further complications arise if the references are interdependent or non-deterministic signals. Such is the case with the direct AC-AC converter described in this thesis.

3.2.9 Design Approach

The closed loop dynamical behaviour of a system under sliding-mode control has two phases. Initially the states are driven, as determined by the control law, from the initial values toward the sliding surface. During this phase the states are affected by any disturbances present. When the sliding mode is reached, and enough control energy is available to prevent overshoot, the system is ideally constrained from there on to the sliding surface. During this phase, the dynamic behaviour is determined entirely by the sliding function, and only in this phase does the system become invariant to matched disturbances and uncertainty. The control law then merely serves to enforce the prescribed dynamic behaviour.

Hence, the design procedure should involve selecting a sliding function that satisfies the specifications of dynamic behaviour imposed on the designer. Then an appropriate control law must be found such that the system representative point reaches the sliding manifold and remains on it [56]. The sliding function and control law is evaluated together to determine whether the existence, reachability and stability conditions are satisfied. If not, either the sliding function or the control law, or both must be adapted. In power converters, for example, the control action is mostly pre-determined, it being constrained to binary values due to the on/off nature of the actuators (transistors). This causes most of the design focus to shift towards the sliding function.

3.2.10 Quasi-Sliding Mode Control

Quasi-sliding mode control (also referred to as *boundary layer control*) refers to the practice of, rather than requiring the system state to absolutely remain on the sliding surface, allowing it to deviate within an arbitrarily small boundary from the sliding surface. This serves to reduce the switching frequency for the sake of preserving the switching actuators. In standard quasi-sliding mode control, the switching frequency is reduced, but not fixed. This can be undesirable in power electronics design, because switching EMI is transmitted across a broader band of frequencies. It also complicates the design of the converter's output filter, as the cut off frequency has to be designed with lower frequencies in mind. To avoid these problems, the switching frequency of the SMC can be fixed. Three techniques have been proposed to do this[19]:

1. adding a constant ramp or timing function into the controller [12]
2. applying adaptive control into the hysteresis[50, 43][43]
3. PWM based SMC controller[49].

According to [19, 49], the PWM based technique shows the best overall performance in terms of absolutely fixed frequency and controller simplicity.

3.3 Example : SMC of Synchronous Buck Converter

In this example, a SMC scheme will be developed for a synchronous buck converter. The problem is, given a DC source of $v_{in} = 898 V$, to regulate the output voltage, v_{out} , toward the reference voltage of $v_{out}^* = 600 V$.

This example is specifically chosen because it is a simplified case of the actual plant under consideration in the greater part of this thesis. SMC was also applied to a single-switch buck converter in [39],[23, p. 8-9], and [34] and this example draws from it.

3.3.1 Model

The converter topology is shown in Fig. 3.6. This topology uses two power transistors, each with an anti-parallel diode. Consequently the converter will always operate in continuous conduction mode.

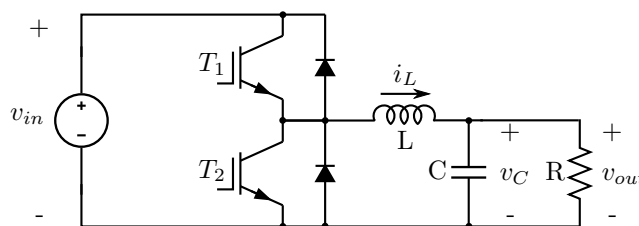


Figure 3.6: Schematic topology of a synchronous buck converter.

The switching model of the plant can be derived by finding expressions for the capacitor and inductor currents for each switching state.

On State

During the 'on' state of the converter, transistor T_1 is switched on and is conducting, and transistor T_2 is switched off. In this state, the source is connected to the load. The differential equations for the inductor current, i_L , and capacitor voltage, v_C , are presented below.

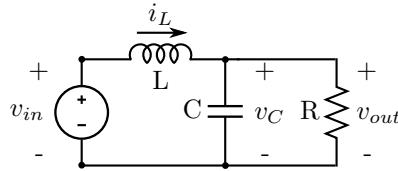


Figure 3.7: On state of a synchronous buck converter.

$$v_{in} = L \frac{di_L}{dt} + v_C \quad (3.42)$$

$$i_L = C \frac{dv_C}{dt} + \frac{1}{R} v_C \quad (3.43)$$

Off State

During the 'off' state of the converter, transistor T_2 is switched on and is conducting, and transistor T_1 is switched off. In this state, the source is disconnected from the load. The differential equations for the inductor current and capacitor voltage are presented below.

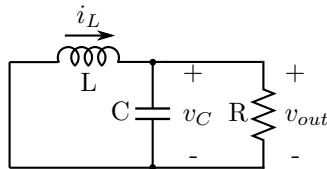


Figure 3.8: Off state of a synchronous buck converter.

$$L \frac{di_L}{dt} = -v_C \quad (3.44)$$

$$i_L = C \frac{dv_C}{dt} + \frac{1}{R} v_C \quad (3.45)$$

Switching Model

The combined switching model is expressed below:

$$\frac{d}{dt} \begin{bmatrix} i_L \\ v_C \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} v_{in} \\ 0 \end{bmatrix} u. \quad (3.46)$$

Note the presence of the switching variable, $u \in \{0, 1\}$, with 0 corresponding to the off state and 1 corresponding to the on state.

This model will now be adapted for the purpose of regulation control by defining new state variables to express control objectives. Let the state variables, x_1 and x_2 , be

$$x_1 = v_{out} - v_{out}^*, \quad (3.47)$$

$$x_2 = \frac{i_C}{C} = \frac{dv_C}{dt} = \dot{x}_1, \quad (3.48)$$

with v_{out}^* corresponding to the reference value of the output voltage. Note that the capacitor voltage, v_C , is chosen as the output variable, v_{out} . By noting that $x_2 = \frac{1}{C}i_L - \frac{1}{RC}v_C$, the system in 3.46 can now be expressed in canonical form as:

$$\frac{d}{dt} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -\frac{1}{LC} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ -\frac{1}{LC}v_{out}^* \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{LC}v_{in} \end{bmatrix} u. \quad (3.49)$$

During the switching operation of the converter, the ideal output voltage would be equal to the output voltage reference and the capacitor current would have an average value of zero. Both state variables, therefore, needs to be regulated towards zero. The phase portraits of this system can be drawn for the respective switching states by plotting x_1 versus x_2 . The respective plots for the on and the off state are shown in Fig. 3.9 and 3.10. In Fig. 3.9, the steady-state point is seen to be at about $(-600V, 0 \frac{V}{s})$, in accordance with Eqs. 3.47 and 3.48.

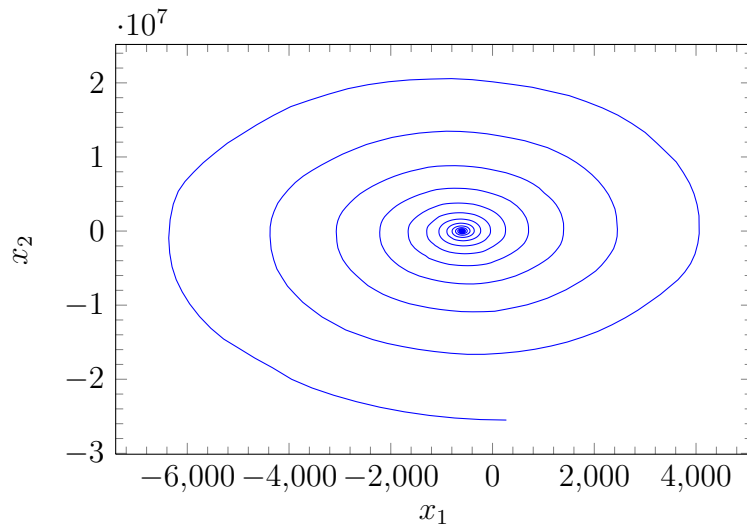


Figure 3.9: Phase portrait corresponding to $u = 0$ and initial conditions at unrest. Component values used for this phase portrait was $L = 850 \mu H$, $C = 75 \mu F$, $R = 25 \Omega$.

In Fig. 3.10, the steady-state point is seen to be at about $(298V, 0 \frac{V}{s})$, in accordance with Eqs. 3.47 and 3.48.

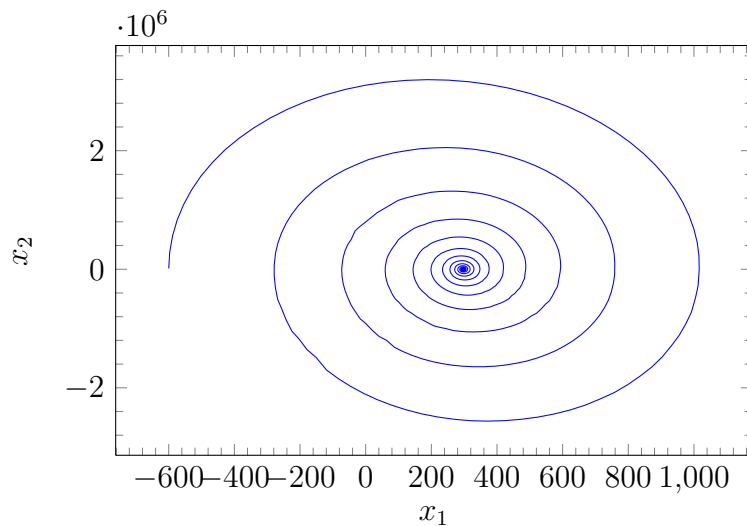


Figure 3.10: Phase portrait corresponding to $u = 1$, with the system initially at rest. Component values used for this phase portrait was $L = 850 \mu H$, $C = 75 \mu F$, $R = 25 \Omega$.

Both of the trajectories toward steady-state are seen to be stable, but oscillatory. In sliding mode, a switching scheme will be applied to achieve state trajectories that are not characteristic of any one of these substructures.

3.3.2 Specification of a Sliding Function

As mentioned in the theory overview, the selection of a sliding function is part of the design problem. The sliding function determines the dynamic behaviour of the system when in sliding mode. For this example, the sliding function will simply be a linear combination of the state space variables:

$$\sigma(\mathbf{x}) = c_1 x_1 + c_2 x_2 \quad (3.50)$$

$$= c_1 x_1 + c_2 \dot{x}_1 \quad (3.51)$$

with $\mathbf{x} = [x_1 \ x_2]^T$, and c_1, c_2 are real constants.

3.3.3 Stability

Closed-loop stability in sliding mode ($\sigma = 0$) can easily be ensured by choosing an appropriate range of values for the sliding constants c_1 and c_2 . The homogeneous solution of Eq. 3.51 can be expressed as

$$x_1(t) = x_1(0) e^{-\frac{c_1}{c_2} t}. \quad (3.52)$$

This shows that, for positive values of c_1 and c_2 , the output voltage error decays exponentially towards zero with time constant $\frac{c_2}{c_1}$. The order reduction property of SMC becomes apparent as, on the sliding line, the second order system is constrained to first order behaviour.

3.3.4 Existence Condition

The existence of the sliding function (which is a line in this case) will now be considered. It will be shown that a control law can be found such that the existence condition,

$$\sigma \dot{\sigma} < 0 \quad (3.53)$$

is always satisfied.

Firstly, an expression for $\dot{\sigma}$ will be found.

$$\dot{\sigma}(\mathbf{x}) = c_1 \dot{x}_1 + c_2 \dot{x}_2 \quad (3.54)$$

Substituting in the bottom row of Eq. 3.49,

$$\dot{\sigma}(\mathbf{x}) = c_1 x_2 - \frac{c_2}{LC} x_1 - \frac{c_2}{RC} x_2 - \frac{c_2}{LC} v_{out}^* + \frac{c_2}{LC} v_{in} u. \quad (3.55)$$

Now constraints will be placed on $\dot{\sigma}$, depending on the value of σ .

Case 1 , $\sigma < 0$:

In this case, for the existence condition to hold, we must ensure that $\dot{\sigma} > 0$. Applying this condition to Eq. 3.55:

$$c_1 x_2 - \frac{c_2}{LC} x_1 - \frac{c_2}{RC} x_2 - \frac{c_2}{LC} v_{out}^* + \frac{c_2}{LC} v_{in} u > 0 \quad (3.56)$$

$$\left(\frac{c_1 LC}{c_2} - \frac{L}{R} \right) x_2 - x_1 - v_{out}^* + v_{in} u > 0 \quad (3.57)$$

$$\left(\frac{c_1 LC}{c_2} - \frac{L}{R} \right) x_2 > x_1 + v_{out}^* - v_{in} u \quad (3.58)$$

$$x_2 > \alpha x_1 + \alpha v_{out}^* - \alpha v_{in} u, \quad (3.59)$$

where $\alpha = \frac{1}{\frac{c_1 LC}{c_2} - \frac{L}{R}}$. It is assumed that α is strictly positive. This would imply that

$$R > \frac{c_2}{c_1 C}, \quad (3.60)$$

restricting the load to a minimum value. Eq. 3.59 represents two regions in the phase plane, depending on the (binary) value of u . These regions are illustrated in Fig. 3.11. The region beneath the sliding line ($\sigma = 0$) is where $\sigma < 0$. The darkly shaded area is where the inequality in Eq. 3.59 is satisfied for $u = 1$. The lightly shaded region is where the inequality in Eq. 3.59 is satisfied for any value of u .

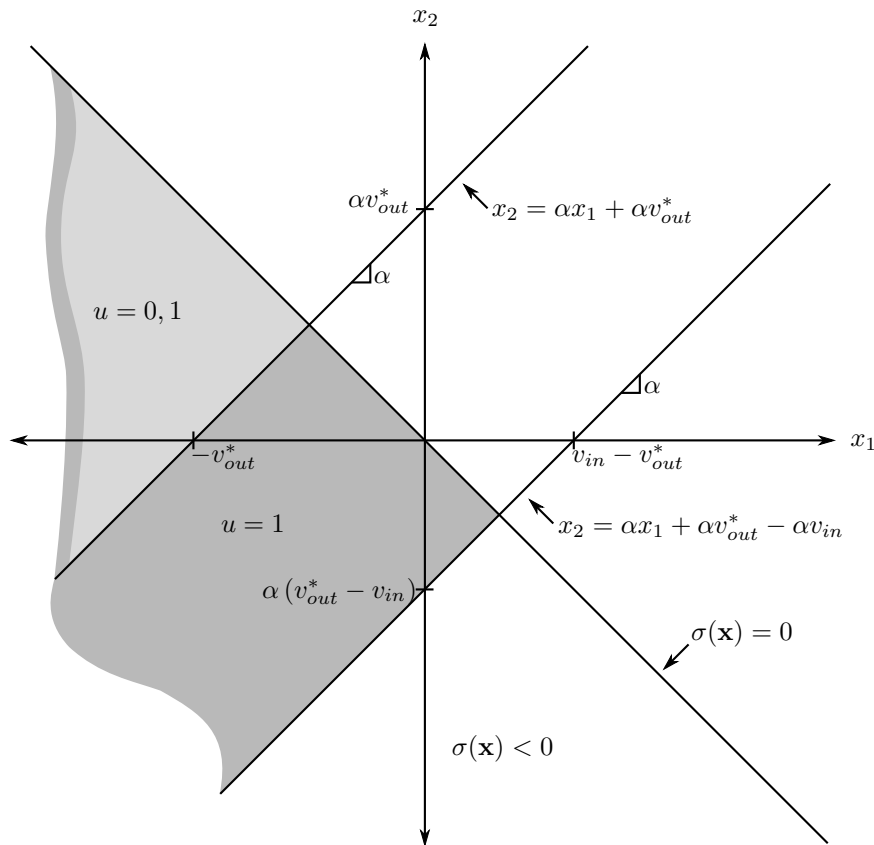


Figure 3.11: Regions of existence when $\sigma < 0$.

All of the parametric uncertainty found in the model is conveniently lumped into the factor α . This includes the uncertain resistive load. The minimum region of existence can therefore be evaluated by analysing the range of possible variation in α .

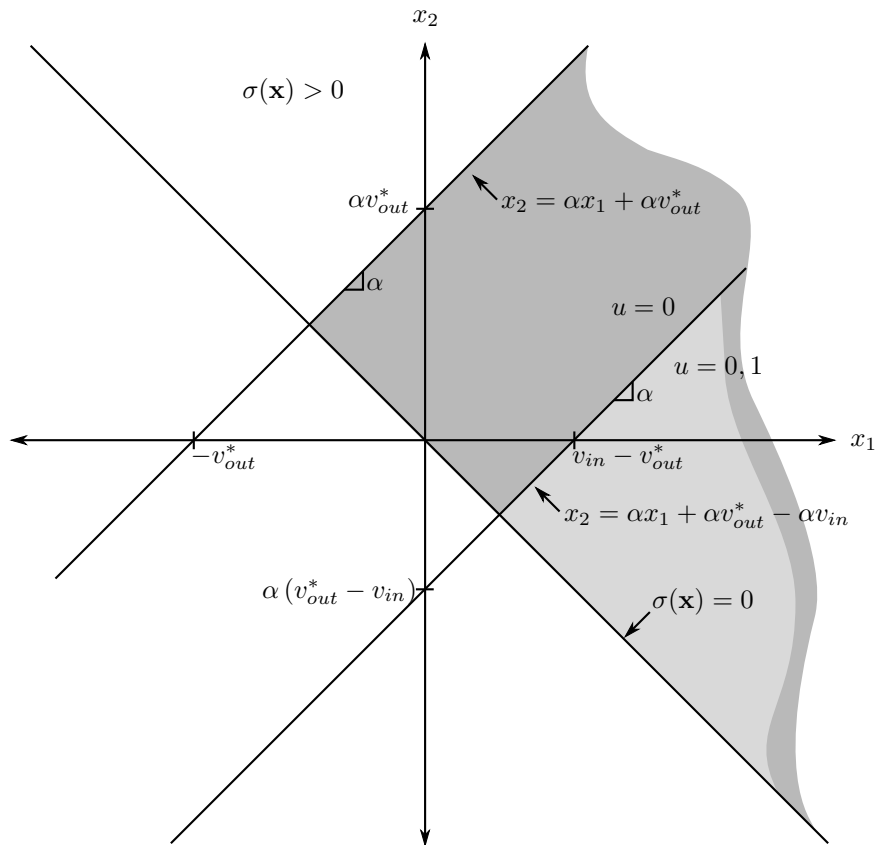
Case 2 , $\sigma > 0$:

In this case, for the existence condition to hold, we must ensure that $\sigma < 0$. Using the same procedure as in Case 1, it can be shown that the region of existence is represented by

$$x_2 < \alpha x_1 + \alpha v_{out}^* - \alpha v_{in} u, \tag{3.61}$$

where $\alpha = \frac{1}{\frac{c_1 L C}{c_2} - \frac{L}{R}}$ is, once again, assumed to be strictly positive. These regions are illustrated in Fig. 3.12. The region above the sliding line ($\sigma = 0$) is where $\sigma < 0$.

The darkly shaded area is where the inequality in Eq. 3.59 is satisfied for $u = 0$. The lightly shaded region is where the inequality in Eq. 3.59 is satisfied for any value of u .

Figure 3.12: Regions of existence when $\sigma < 0$.

General Case

The area of existence for the general case is shown in Fig. 3.13. The sliding mode exists where there are darkly shaded areas on both sides of the sliding line ($\sigma = 0$). If the system state is found in one of the other regions, the control law will have to direct it in such a way that, with every subsequent crossing of the sliding line, the distance toward the region of existence decreases.

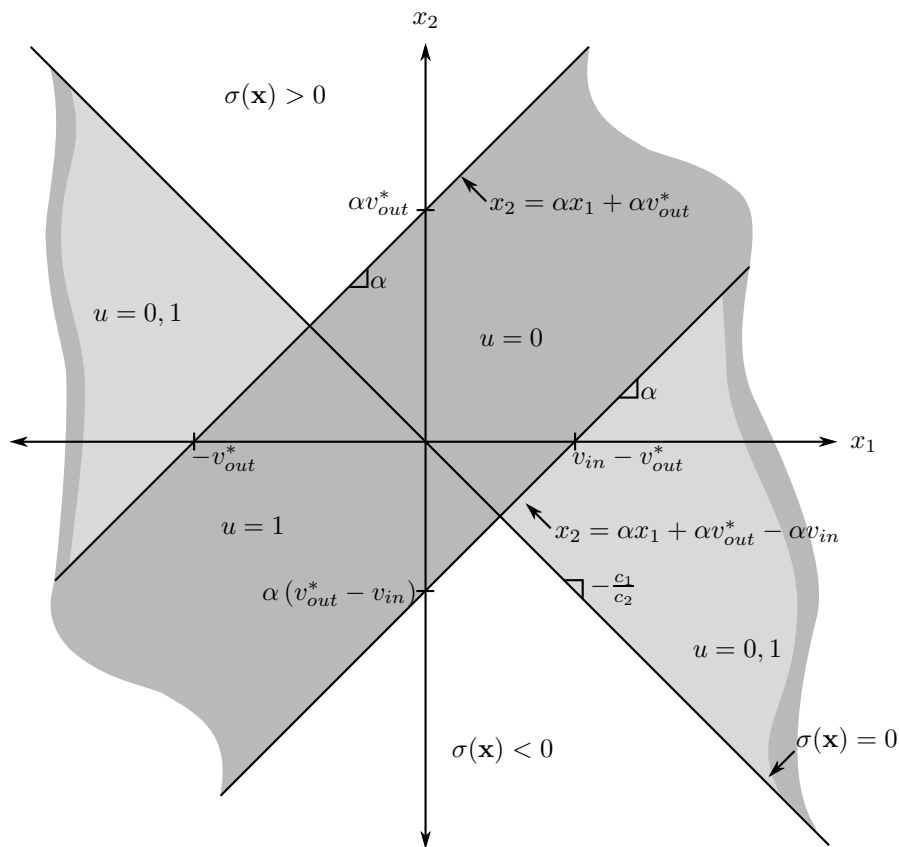


Figure 3.13: Total area of sliding mode existence for the proposed sliding function.

In order to force the system trajectory onto the sliding line, a switching law must be devised. The following switching law is most commonly employed in literature:

Algorithm 1 Commonly Employed Switching Law

$$u = \begin{cases} 1 & , \sigma < 0 \\ 0 & , \sigma > 0 \end{cases} . \quad (3.62)$$

The output of the above switching is depicted in the state space by Fig. 3.14.

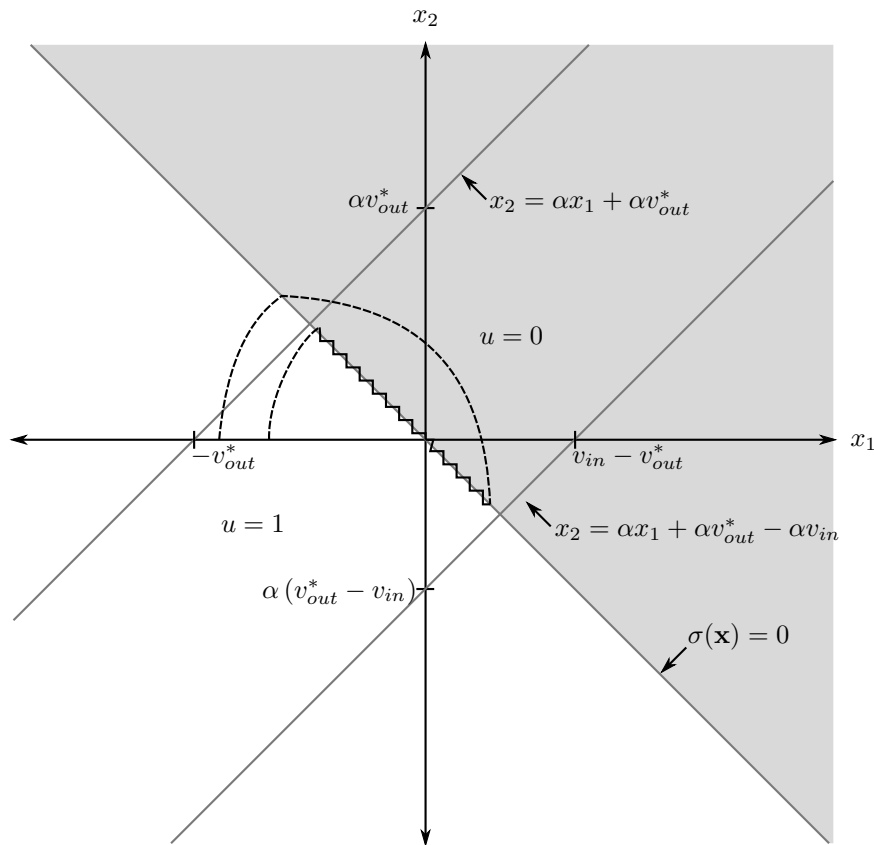


Figure 3.14: The output of the control law for the various regions on the phase plane. The shaded area corresponds to $u = 0$. The clear area corresponds to $u = 1$. Two trajectories are drawn, each starting from different initial conditions. The dashed sections correspond to the reaching phases, while the solid sections correspond to sliding mode toward the origin.

Two trajectories are drawn in Fig. 3.14, each starting with different initial conditions. The dashed part of each line represents the reaching phase. The solid part of each line represents the state trajectory in sliding mode. It is seen that, depending on the initial state, the system state trajectory might at first cross the sliding line in a region where the sliding mode is non-existent. In such an event, insufficient control energy is available to constrain the system RP to the sliding line. Overshoot results when the system state crosses into the left-hand side of the phase plane. The system state does, however, move toward the region of existence, and is eventually constrained to the sliding line. This shown that the sliding line is reachable within finite time.

It was found that the switching law can be defined in a way that could maintain reachability and decrease the likelihood of overshoot:

Algorithm 2 Modified switching law.

$$u = \begin{cases} 1 & , \sigma < 0, x_2 < \alpha x_1 + \alpha v_{out}^* \text{ or} \\ & \sigma > 0, x_2 < \alpha x_1 + \alpha v_{out}^* - \alpha v_{in} \\ 0 & , \sigma < 0, x_2 > \alpha x_1 + \alpha v_{out}^* \text{ or} \\ & \sigma > 0, x_2 > \alpha x_1 + \alpha v_{out}^* - \alpha v_{in} \end{cases} \quad (3.63)$$

Algorithm 2 essentially constrains the system trajectory in the reaching phase on a course that will cross the sliding line within the area of existence. The output of the control for the various regions in the state space, as expressed in Eq. 3.63, is depicted in Fig. 3.15.

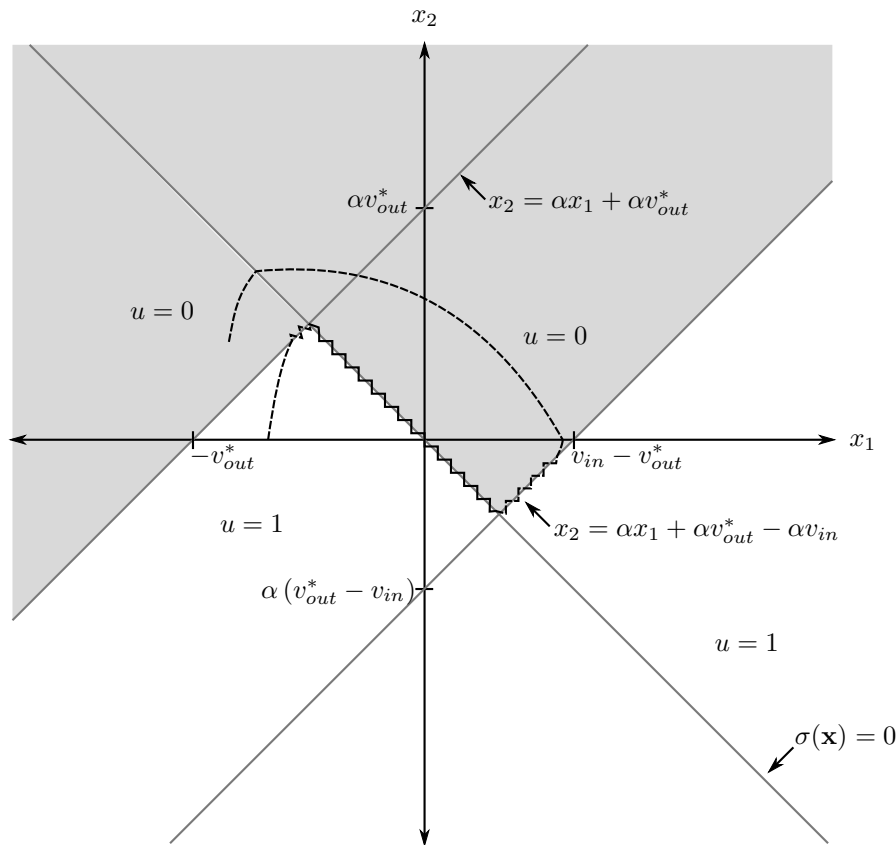


Figure 3.15: The output of the control law for the various regions on the phase plane. The shaded area corresponds to $u = 0$. The clear area corresponds to $u = 1$.

If the filter inductor has some large initial current (resulting in a large value for x_2), the trajectory will cross the sliding line for the first time outside the region of existence. This causes overshoot into the left-hand side of the phase plane. Notice that in a region around the equilibrium point, a secondary sliding action is indicated on the boundary of the shaded and clear region. Even though a type of sliding motion appears here, the system is not in sliding mode, as $\sigma \neq 0$. This sliding action does, however, help to direct the system trajectory to a region of existence. The system therefore exhibits less oscillatory behaviour in the reaching phase, as it is guided towards the area of sliding mode existence on the lines $x_2 = \alpha x_1 + \alpha v_{out}^*$ and $x_2 = \alpha x_1 + \alpha v_{out}^* - \alpha v_{in}$. At the same time the modified switching has the effect of prolonging the reaching phase. A trade-off therefore exists between time-to-sliding-mode and magnitude of transient effects.

3.3.5 Reachability

The reachability condition, as stated in Eq. 3.13 of Section 3.2.3, is that the steady state representative point for any of the two substructures must lie with the switching space reserved by the control law for the other substructure. In Fig. 3.16, the phase portraits for each of the substructures (Fig. 3.9 and 3.10) was overlaid and the sliding line was drawn. It is clear that the two steady state points, x_{ss}^+ and x_{ss}^- , are on opposite sides of the sliding line, and the condition for reachability is satisfied. As long as the reference voltage, v_{out}^* , remain within the bounds of the source voltage, v_{in} , reachability is always guaranteed for the synchronous buck converter.

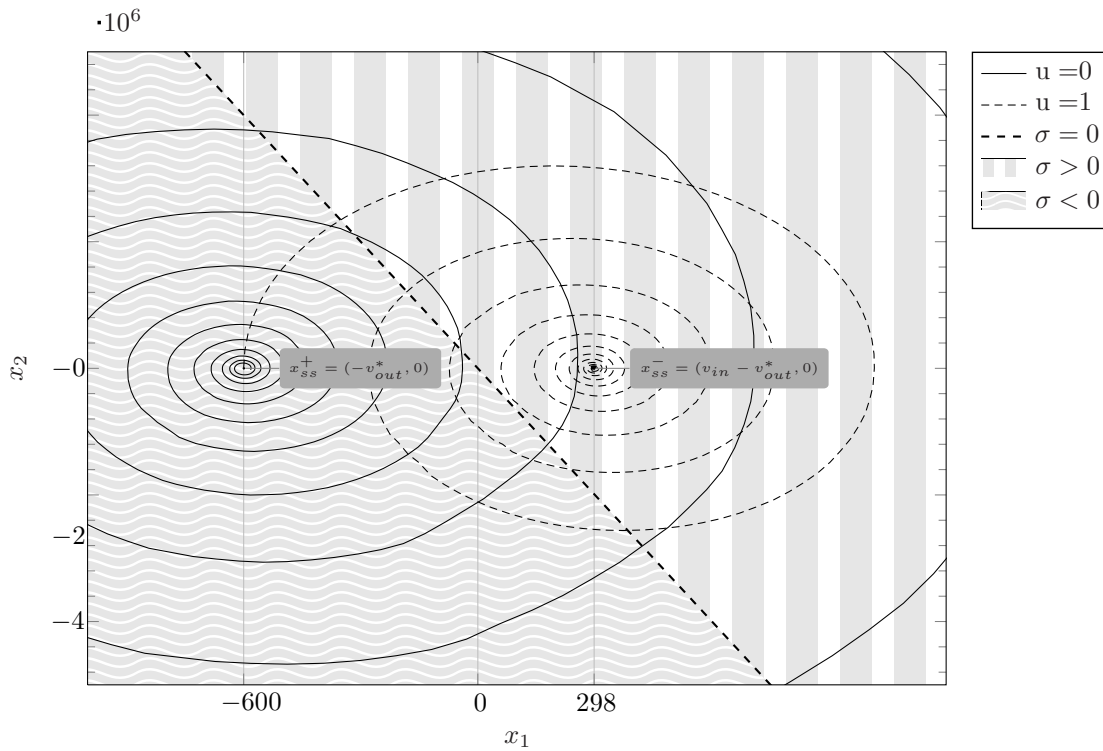


Figure 3.16: Phase portraits of the two switching states overlaid on each other.

3.3.6 Equivalent Control

The equivalent control is found by enforcing the invariance condition:

$$\begin{aligned} \dot{\sigma} \Big|_{\substack{\sigma=0 \\ u=u_{eq}}} &= 0. \end{aligned} \quad (3.64)$$

If the solution in terms of x_2 of the homogeneous form of the sliding function (Eq. 3.50) is substituted into the expression for $\dot{\sigma}$ (Eq. 3.55), the equivalent control variable appears:

$$c_1 \left(-\frac{c_1}{c_2} x_1 \right) - \frac{c_2}{LC} x_1 - \frac{c_2}{RC} \left(-\frac{c_1}{c_2} x_1 \right) - \frac{c_2}{LC} v_{out}^* + \frac{c_2}{LC} v_{in} u_{eq} = 0. \quad (3.65)$$

Solving for u_{eq} yields,

$$u_{eq} = \left(1 + \frac{c_1^2 LC}{c_2^2} - \frac{c_1 L}{c_2 R} \right) \frac{x_1}{v_{in}} + \frac{v_{out}^*}{v_{in}} \quad (3.66)$$

3.3.7 Simulations of ideal SMC

Simulations were run of the ideal SMC on a synchronous buck converter with $850 \mu\text{H}$ inductor, $75 \mu\text{F}$ capacitor, and 25Ω load. The input voltage was set to 898 V , and the reference was from zero to 600 V at time $t = 0$. The first sliding weight, c_1 was varied to see the effect on the dynamic response. The second sliding weight, c_2 , was set equal to C , the capacitance of the output filter. This means that we are effectively regulating the output voltage error and the capacitor current to zero.

Simulations with standard switching law

A simulation was performed using Algorithm 1 as the switching law, and setting constant $c_1 = 0.5$. The result is shown in Fig. 3.17. The derivative of the output voltage, x_2 , is seen to rise until the sliding line is encountered. This translates into fast response speed (100% rise time of 0.417 ms), but very large inductor current (186 A_{peak}). When the system RP crosses the sliding line, the switching law causes the system to change state and the sliding mode is reached on the second crossing.

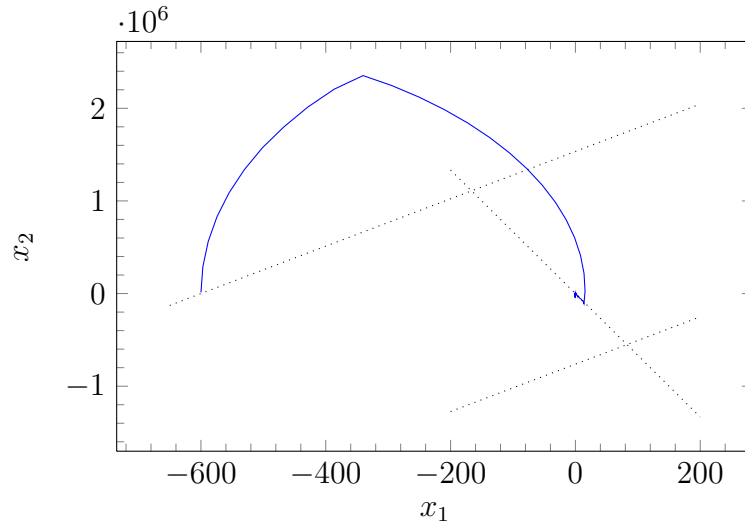


Figure 3.17: Simulation result with the standard switching law. The state trajectory can move far away from the equilibrium point before the area of existence is reached.

Various step responses with the corresponding values for c_1 are shown in Fig. 3.18 and 3.19. Fast response times are achieved and overshoot can be controlled by means of the constant c_1 . The inductor current does, however, have large initial spikes.

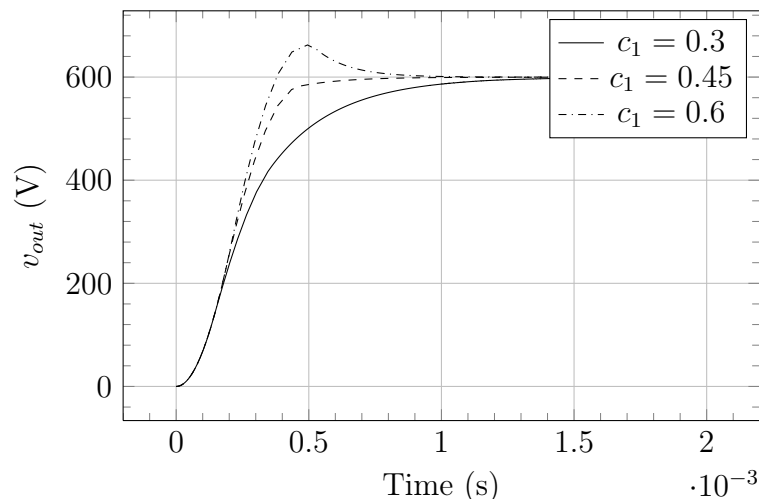


Figure 3.18: Various step responses for the output voltage, using the standard switching law.

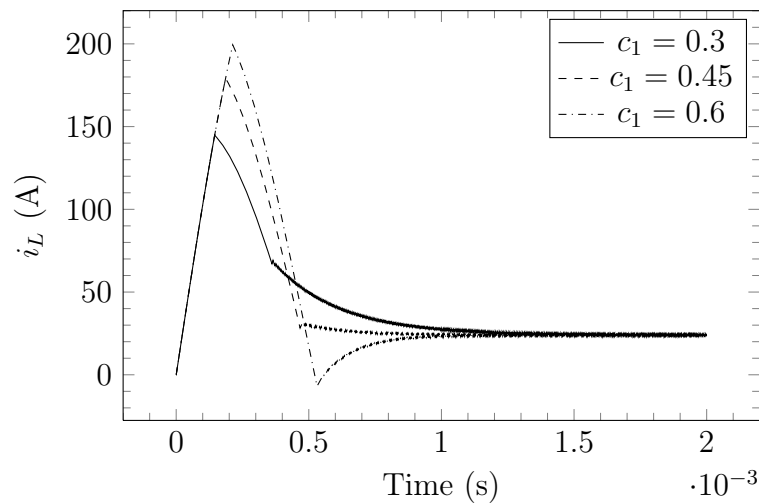


Figure 3.19: Simulation result with the standard switching law. Shorter reaching periods is at the expense of large inductor currents.

Simulations with modified switching law

A simulation was performed using Algorithm 2 as the switching law, and setting constant $c_1 = 0.5$. The result is shown in Fig. 3.20. The system RP is clearly guided by the modified switching law along one of the boundaries of existence. This causes the system to enter sliding mode on the first encounter with the sliding line. The inductor current is greatly limited ($101 A_{\text{peak}}$), at the cost of a much slower rise time (3.28 ms). It should be noted, that the decreased response time is only effective in the reaching phase. Once the system is successfully constrained to the sliding mode, the dynamic behaviour for different switching laws (but identical sliding weights) is identical.

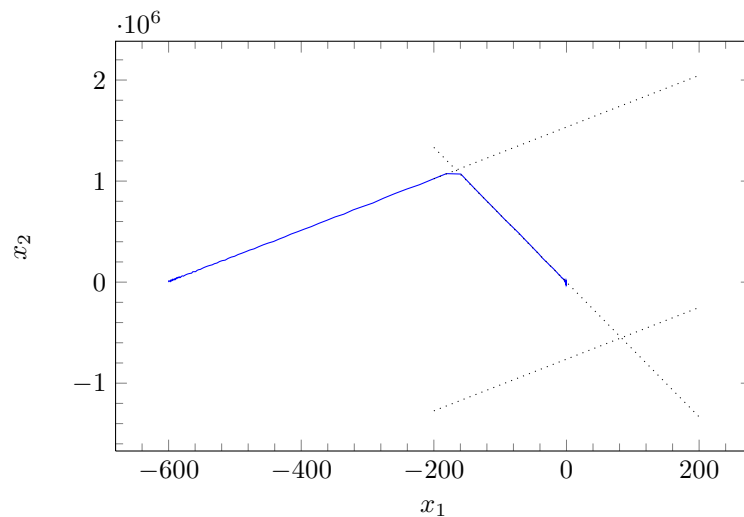


Figure 3.20: Simulation result with modified switching law. The state trajectory is guided within the region of existence.

Various step responses with the corresponding values for c_1 are shown in Fig. 3.21 and 3.22.

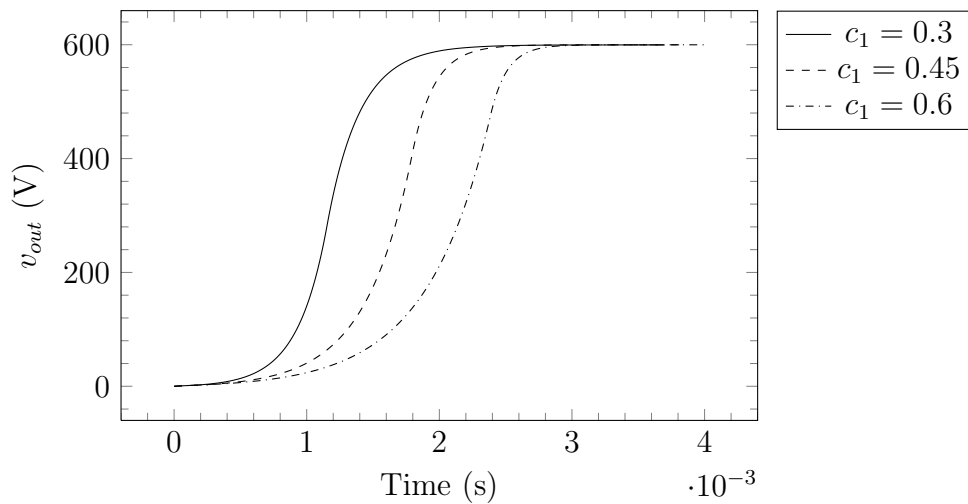


Figure 3.21: Simulation result with modified switching law. The state trajectory is guided within the region of existence.

Response times in the reaching phase is slow, but the inductor current spikes are greatly reduced.

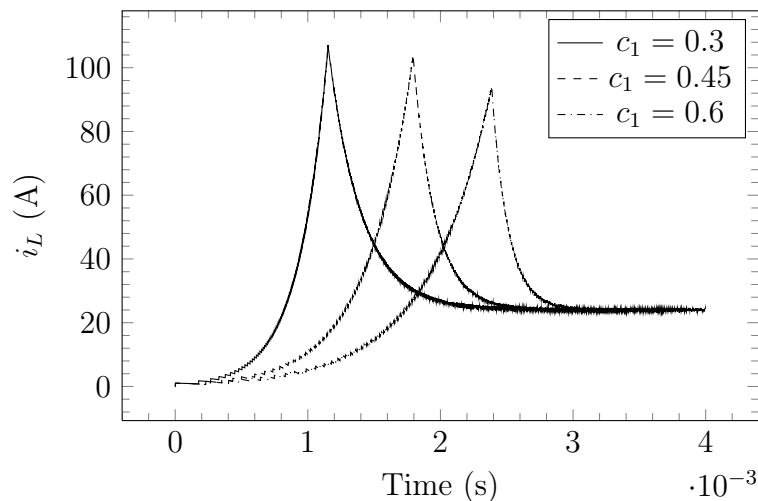


Figure 3.22: Simulation result with modified switching law. The magnitude of the current spikes during the reaching phase is reduced.

Simulation of Equivalent Control

To illustrate how the equivalent control is equivalent to the low-pass filtered switching control, the value of the control output, u , was passed through a second-order LPF with a cut off frequency of 100kHz. The result is shown together with a plot of the equivalent control (as expressed in Eq. 3.66) in Fig. 3.23. It is seen that when the system is in sliding mode (after the reaching phase is over), the equivalent control is a good average approximation of the switching control. This makes the equivalent control a powerful tool to analyse closed-loop control performance with average models, where continuous control is used.

Also note in Fig. 3.23 how, after about 1 ms, when the sliding mode is established, the equivalent control, u_{eq} , remains within its boundaries of 0 and 1. In [11], this characteristic of the equivalent control is explicitly used to determine the feasibility of a sliding motion over a proposed switching surface.

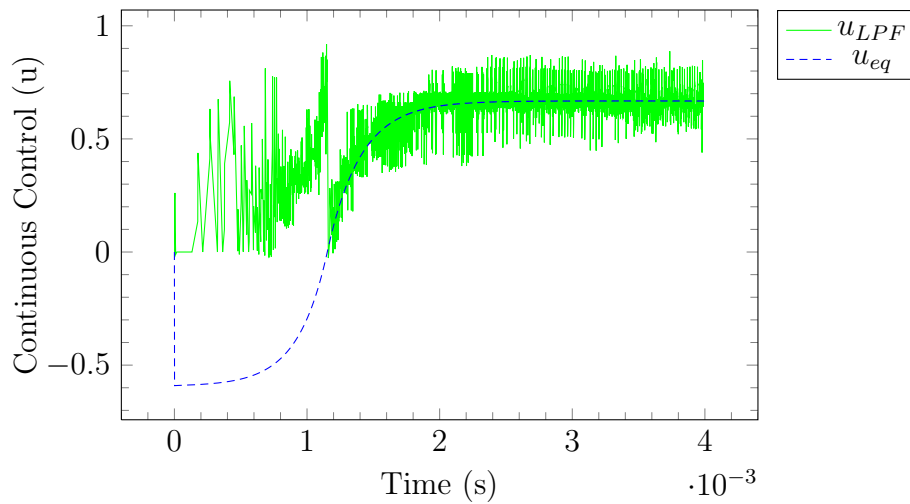


Figure 3.23: Equivalent control together with the low-pass filtered version of the actual control. This control signal was used to obtain the voltage waveform in Fig. 3.21 and the current waveform in Fig. 3.22 corresponding to $c_1 = 0.3$.

Control applied at non-zero initial values

The oscillatory effects during the reaching phased can be demonstrated by simulation with non-zero initial values. Algorithm 1 was used for the switching law. An initial charge of 898 V was put on the filter capacitor, and an initial current of 36.7 A was put through the filter inductor, with a load size of 25 Ω . A decreasing spiral is seen in the phase plane, indicating a decaying sinusoidal oscillation of the state variables in the time-domain. The spiral approaches the origin, and when the region of sliding mode existence is entered, a linear behaviour is seen.

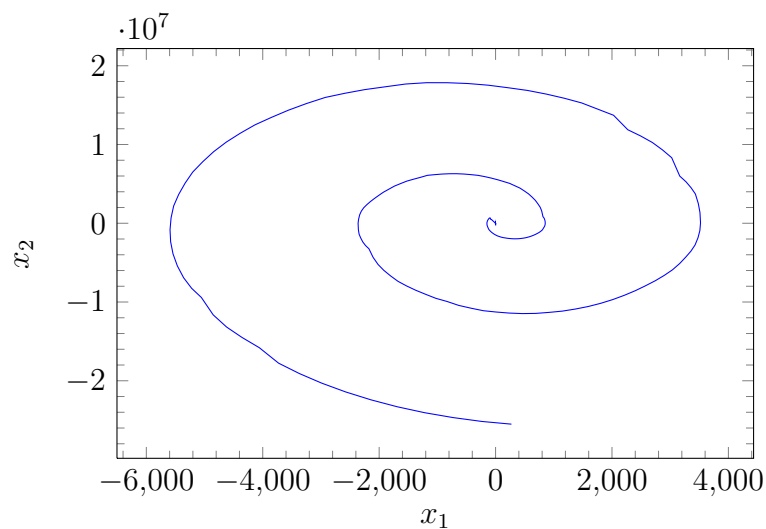


Figure 3.24: Large initial charge on the capacitor and initial current in the inductor.

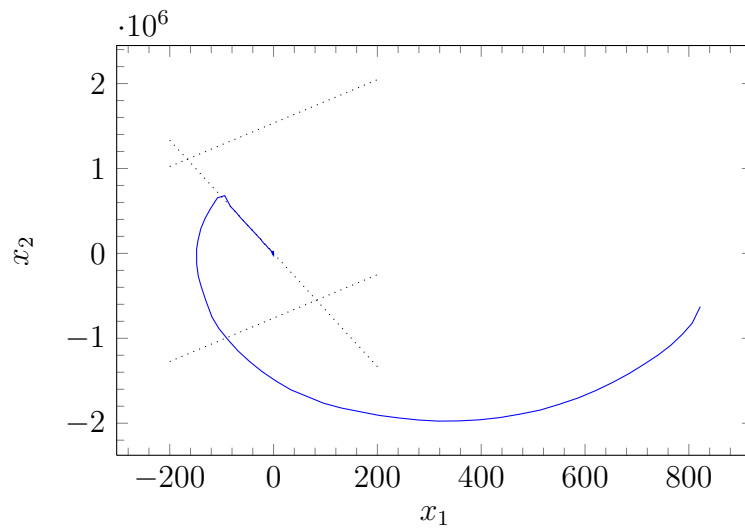


Figure 3.25: Large initial charge on the capacitor and initial current in the inductor. Zoomed in on the sliding mode, with the existence region boundaries indicated.

3.3.8 Modifications for QSMC

A new way was found to limit the switching frequency of the converter. If the calculated derivative of the output voltage is low-pass filtered before being fed into the control process, the switching frequency is effectively limited to the filter cut off frequency, provided that the filter is of high enough order. Simulations using a second order low-pass filter were effective.

There is much more that could be said about this, but it falls outside the scope of this example.

CHAPTER 4

MODELLING AND SIMULATION

“As far as the laws of mathematics refer to reality, they are not certain, and as far as they are certain, they do not refer to reality.”

- Albert Einstein

Modelling and simulation has traditionally played an enormous role in control system development. With the advent of robust control techniques such as fuzzy control and neural networks, the process of mathematical modelling has been side-stepped to a large degree¹. With sliding mode control the model is still important, as it can be used to establish whether the conditions for sliding mode are met. System modelling is also useful for analysing and predicting system behaviour, especially when it comes to the frequency domain. For these reasons, the system is modelled in detail.

4.1 Integrated Approach to Modelling, Simulation, and Design

In this project, computer technology was used to establish an integrated approach to modelling, simulation and design. Computer simulation is a powerful tool, not only for the verification of a design, but also for the entire design process. Virtual testing is used in conjunction with hardware testing, and has the advantage of being cheap and fast in comparison. Computer simulations can be used to easily analyse a circuit in both the time domain as well as the frequency domain. Analysis of sensitivity to component tolerances can be done, which is not practical to do with hardware. Simulations can therefore be used early in the design process to make informed decision-making. Simulations can then be used to verify a realised design to see if theoretical models represent reality accurately enough. Simulations are therefore used not only to verify designs, but as part of the entire design process.[45]

4.1.1 Modelling and Simulation of Circuit Elements

Modelling plays an important part in simulations. The simulation is only as good as the models it uses. With higher currents, for example, parasitic inductances play a large role in power electronic circuits. In this chapter, effort is taken to detail the design of models that include important parasitics.

In this thesis, Mentor Graphics' SystemVision² was used for circuit simulations. VHDL-AMS was used for modelling, because the MVEVR controller was also implemented in VHDL. Many of the control blocks could be ported from the synthesized controller's VHDL to SystemVision simulations and vice versa. This allows for more realistic control simulations, as the code used in simulations is very similar to that used in the final implementation.

¹This is especially advantageous in applications where the plant is too complex to model accurately.

²SystemVision is a powerful mixed signal and multi-physics simulation tool built on top of ModelSim for VHDL-AMS simulation, and combined with Spice and C modelling capabilities.

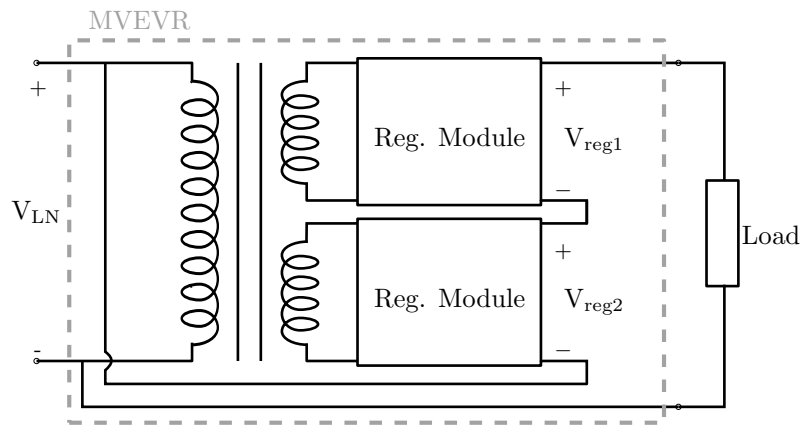


Figure 4.1: A three-winding transformer is connected in an auto-transformer-like configuration.

4.1.2 Modelling of Synthesisable VHDL System Components

For precision simulation of individual VHDL entities, Mentor Graphics' ModelSim package was used. This is a powerful application for VHDL simulation and debugging. One would typically create a *test bench* for a VHDL entity to be simulated. The test bench instantiates the component to be tested and feeds it the desired test signals. *Assertions* can be performed on the component's output response to verify correct operation.

4.2 Component Level Modelling and Simulation

In order to simulate the MVEVR system, each component in the system had to be modelled. These components include the following:

- system transformer
- bus capacitors and snubber capacitors
- switching elements
- filter inductor
- filter capacitor
- dynamic load to simulate load steps
- dynamic source to simulate voltage dips.

Parasitic components (mostly equivalent series resistance) were included in most of the models. Parasitic values were obtained by using the component data sheets for the capacitors. The magnetic components (transformer and filter inductor) were custom-made. Measurements were used to obtain values for the modelled parasitics.

4.2.1 Transformer Model

A three-winding transformer was used for the MVEVR since two regulator modules were required. The line-neutral voltage is applied to the primary tap, and regulator modules are connected to each of the two secondary taps. The transformer is wired externally in an auto-transformer-like configuration, as shown in Fig. 4.1.

This configuration contrasts with the standard auto-transformer in that each series winding is first regulated with an AC chopper before the autotransformer connections are made to the primary terminals. The transformer power and voltage ratings are displayed in Table 4.1.

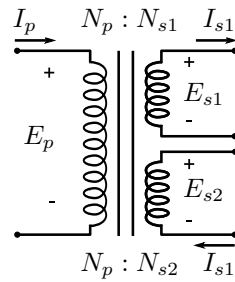


Figure 4.2: Voltage and current relations of a three-winding transformer.

Table 4.1: Transformer Ratings

Parameter	Value
Power Rating	127 kVA
Primary Voltage	12.7 kV
Primary Current	10 A
Secondary Voltage	635 V
Secondary Current	100 A

Ideal Three-Winding Transformer Relations

The ideal transformer relations for a three-winding transformer is similar to that of a two-winding transformer, and (as indicated in Fig. 4.2) is expressed as:[24]

$$N_p I_p = N_{s1} I_{s1} + N_{s2} I_{s2} \quad (4.1)$$

$$\frac{E_p}{N_p} = \frac{E_{s1}}{N_{s1}} = \frac{E_{s2}}{N_{s2}}. \quad (4.2)$$

In the per-unit system, these relations are:

$$I_{pp.u.} = I_{s1p.u.} + I_{s2p.u.} \quad (4.3)$$

$$E_{pp.u.} = E_{s1p.u.} = E_{s2p.u.}, \quad (4.4)$$

where all three windings use a common S_{base} and the voltage bases are the equal to the rated voltages for each winding.

Equivalent Circuit for a Three-Winding Transformer

A description of the T-equivalent circuit for three-winding transformers was found in [62]. The equivalent circuit is show in Fig. 4.3a. The magnetizing branch was omitted, because this impedance was seen to be much larger than the series impedances. Series resistance in the T-equivalent circuit represent eddy-current losses. In a three-winding transformer, eddy-currents are induced in a winding by the stray flux produced by the other two windings. These currents can be induced in a winding even if it is carrying no load. No single resistance in the model can therefore be attributed to a single winding, but rather is distributed among all of them.[62]

In order to calculate the impedances of the T-equivalent circuit, short-circuit tests were done to determine the series impedances. As shown in Fig. 4.3b, a voltage is applied to one of the three taps, while another is shorted, and another is left open. The current into the tap with the applied voltage is measured. The series

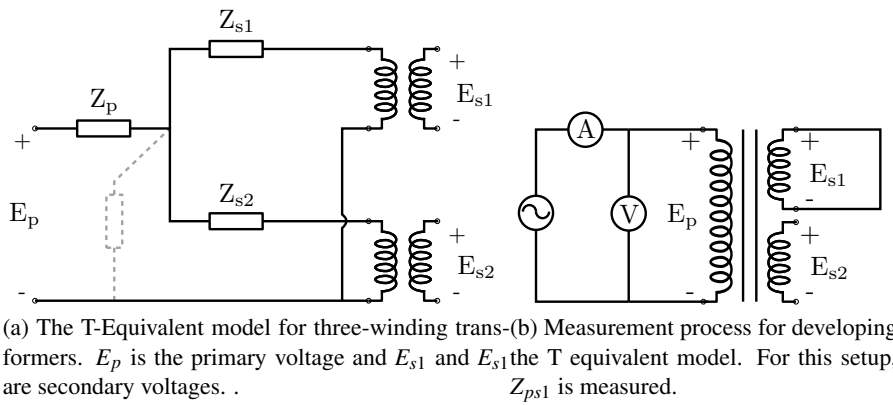


Figure 4.3: The T-Equivalent model for the three-winding transformer was integrated into the system model (Fig.4.3a). The necessary short-circuit tests were done (Fig. 4.3b) to obtain leakage inductances from which the equivalent impedances were calculated.

impedance is calculated by dividing the measured voltage by the measured current. This is done for all three windings, and the resulting values are shown in Table 4.2. The per-unit series impedances are then used in Eqs. 4.5-4.7 to calculate the equivalent impedances for the T equivalent circuit. The equivalent impedances are given by

$$Z_p = \frac{Z_{ps1} + Z_{ps2} - Z_{s1s2}}{2} \quad (4.5)$$

$$Z_{s1} = \frac{Z_{ps1} + Z_{s1s2} - Z_{ps2}}{2} \quad (4.6)$$

$$Z_{s2} = \frac{Z_{ps2} + Z_{s1s2} - Z_{ps1}}{2}, \quad (4.7)$$

where Z_{ps1} is the series impedance measured in the primary winding with a short-circuit on winding s1, Z_{ps2} is the series impedance measured in the primary winding with a short-circuit applied to winding s2, and Z_{s1s2} is the series impedance measured in winding s1 with a short-circuit applied to winding s2.

Simplified T Equivalent circuit, viewed from the secondary

In order to model each voltage regulator unit separately, it was desirable to manipulate the equivalent circuit in a way that would cause the equivalent impedances to appear on the secondary side. This was done by modelling the system as if the first secondary was the primary. The resulting model is shown in Fig. 4.4a. The accompanying set of equations to calculate the equivalent impedances were modified accordingly and is shown in Eqs. 4.8-4.10. The model was subsequently further simplified by recognising that the voltage ratio of both secondary windings relative to the primary winding is the same. The ideal transformer connected to E_{s2} in Fig. 4.4a could therefore be omitted, as shown in Fig. 4.4b. The model was simplified even further by noting that the equivalent impedances, Z_{s1} and Z_{s2} , are almost identical. This will be seen in the next subsection. This is because the two secondaries have the same winding ratio relative to the primary. It also implies that the transformer is wound symmetrically relative to the two secondaries. Assuming that the current through both regulator modules - and therefore through both secondaries - is of identical phase and magnitude, Z_{s1} and Z_{s2} can be lumped into one component, with an equivalent value of $Z_{s1} + Z_{s2}$. This is shown in Fig. 4.4c. The effect of the transformer impedances can now be modelled for each regulator separately. The equivalent impedances, as seen from either of the secondary sides, is expressed as

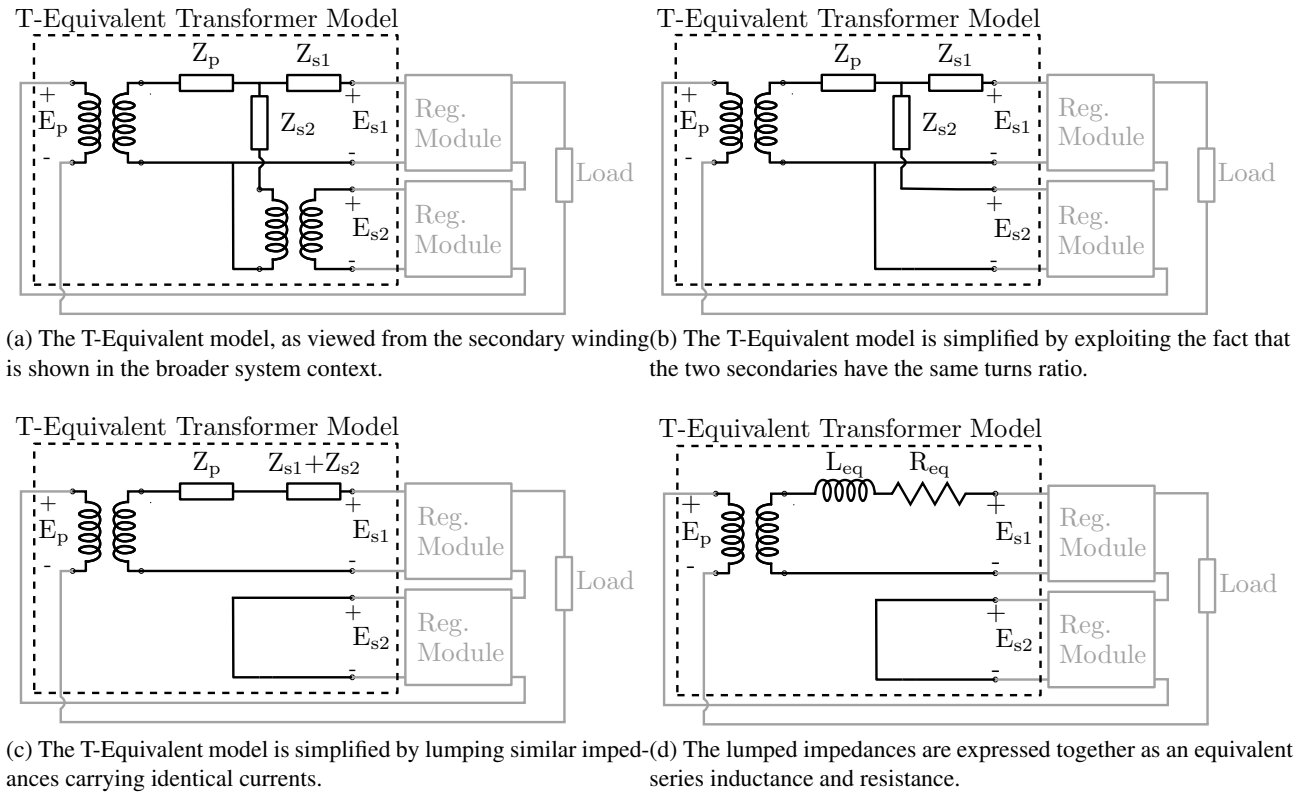


Figure 4.4: The T-Equivalent model, as seen from the secondary side, was integrated into the system model (Fig.4.4a). Various simplifications were performed as show in Figs. 4.4b-4.4d.

Table 4.2: Measurements toward a T equivalent circuit at 80% of rated current.

Measurement	Voltage Applied	Current Measured	Impedance Value	Impedance ³
Z_{s1p} ⁴	$9.00\angle 0^\circ\text{V}$	$81\angle -72^\circ\text{A}$	$110m\angle -72^\circ\Omega$	$35m\angle -72^\circ\text{p.u.}$
Z_{s1s2} ⁵	$3.13\angle 0^\circ\text{V}$	$81\angle -8.64^\circ\text{A}$	$39m\angle -8.64^\circ\Omega$	$12m\angle -8.64^\circ\text{p.u.}$
Z_{ps2} ⁶	$153\angle 0^\circ\text{V}$	$3.8\angle -66.24^\circ\text{A}$	$38\angle -66.24^\circ\Omega$	$30m\angle -66.24^\circ\text{p.u.}$

$$Z_{s1} = \frac{Z_{s1p} + Z_{s1s2} - Z_{ps2}}{2} \tag{4.8}$$

$$Z_p = \frac{Z_{s1p} + Z_{ps2} - Z_{s1s2}}{2} \tag{4.9}$$

$$Z_{s2} = \frac{Z_{s1s2} + Z_{ps2} - Z_{s1p}}{2} \tag{4.10}$$

Measurements and Resulting Model

For each impedance measurement, the base impedance was calculated by taking the quotient of the base power and the square of the voltage rating for the winding being measured, that is, $Z_{base} = \frac{V_{base}^2}{S_{base}}$. The power rating of the transformer (127 kVA) was used as the base power throughout. Measured impedances are shown in Table 4.2.

³All per unit impedances were calculated with $S_{base} = 127\text{kVA}$, the power rating of the transformer.

⁴Voltage on $s1$, short on $s2$, p open.

⁵Voltage on $s1$, short on $s2$, p open.

⁶Voltage on p , short on $s2$, $s1$ open.

Table 4.3: Equivalent Impedances for 80% of rated current.

Equivalent Impedance	Value	Value
Z_p	$-0.0060 + j0.0136 \text{ p.u.}$	$-0.01905 + j0.04318 \Omega$
Z_{s1}	$0.0060 - j0.0137 \text{ p.u.}$	$0.01905 - j0.04349 \Omega$
Z_{s2}	$0.0060 - j0.0136 \text{ p.u.}$	$0.01905 - j0.04318 \Omega$

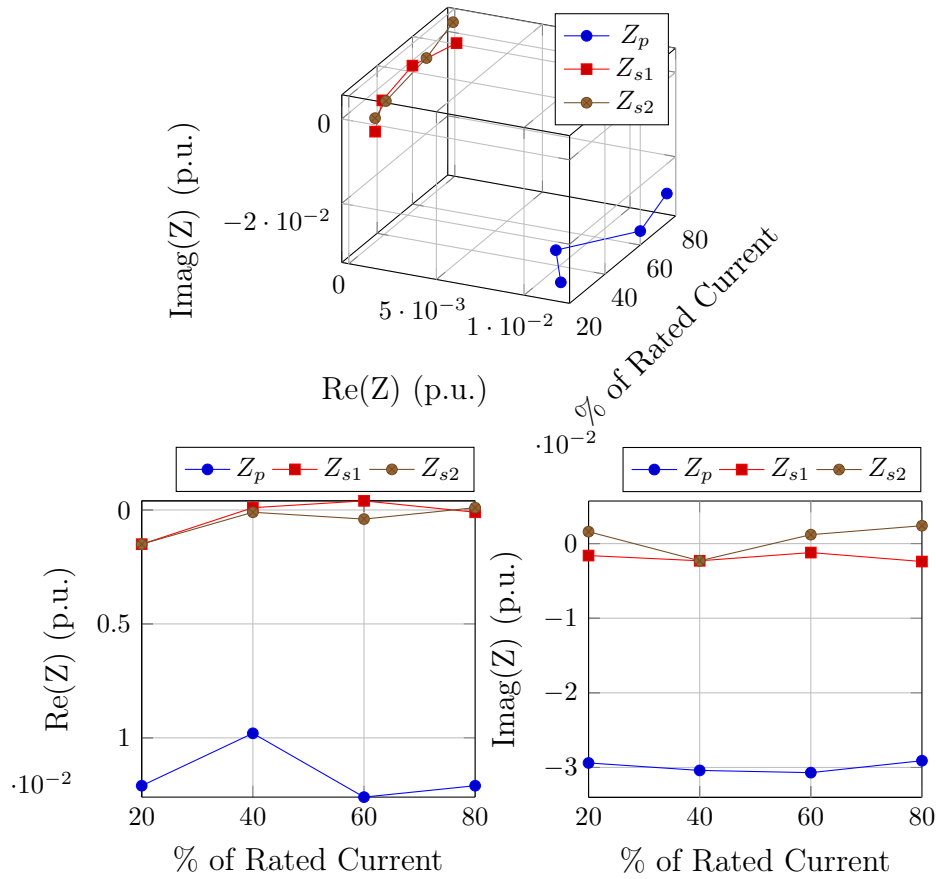
The calculated equivalent impedances at the operating point closest to rated values are shown in Table 4.3. It is seen that, of the real parts of the equivalent impedances, one of them is negative. This occurs if one of the real parts of the values of Z_{ps1} , Z_{ps2} , or Z_{s1s2} is greater than the sum of the other two values. Therefore, only one of these values can be negative for the same transformer.[62] The negative resistance also emphasises that these impedances do not represent physical quantities such as leakage inductance or resistive copper loss. They are merely part of the equivalent model. The centre point of the three impedances is also not a physical point.[24]

Impedance measurements were made at various operating points. Short circuit tests were done at 20%, 40%, 60%, and 80% of the rated current. Tests could not be done at full rated current (100 A), due to limitations on the test equipment. The T-Equivalent model assumes a linear relationship between voltage and current, but it is expected that this relationship is affected by the non-linear B-H curve of the transformer. The equivalent impedances were calculated at the four operating regions mentioned in order to see how dramatic the non-linearities are. The movement of the equivalent impedances versus increase in operating current is shown graphically in Fig. 4.5. It is seen that the impedances are delightfully linear as the current increases.

It was assumed that the magnetizing branch of the model was negligible. This was confirmed by measurement with open-circuit tests at more-or-less the same operating regions, only this time at 20 %, 40 %, 60 % and 70 % of rated *voltage*. In all the cases these (shunt) impedances were at least 10 000 times larger than the series impedances. The assumption is therefore justified.

Table 4.4: Equivalent values for lumped inductance and resistance, at 80 % of rated current.

Equivalent Impedance	Value
L_{eq}	138.4 μH
R_{eq}	19.05 m Ω

Figure 4.5: Effects of non-linear phenomena on the T-Equivalent model. It is seen that Z_{s1} and Z_{s2} are nearly identical.

The transformer loss contributions of all three windings could finally be expressed at any of the secondary windings as a simple inductor in series with a resistor. The equivalent resistance and inductances is shown in Table 4.4.

4.2.2 Capacitor Model

Fig. 4.6 shows a model of a capacitor, with capacitance, equivalent series resistance (ESR), and equivalent series inductance (ESL). The equation governing the model behaviour in terms of voltage across, v_c , and current through, i_c , is expressed in Eq. 4.11.

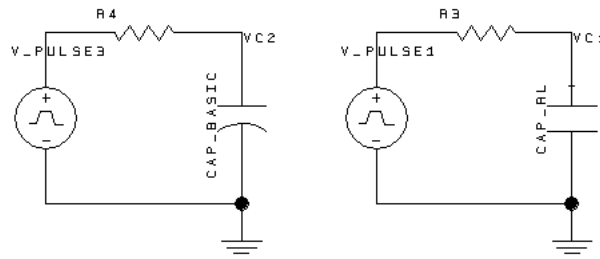


Figure 4.7: SystemVision Testbench for simulating the created VHDL-AMS models with and without parasitics.

$$v_c = \frac{1}{C} \int i_c dt + i_c R_s + L_e \frac{di_c}{dt} \quad (4.11)$$

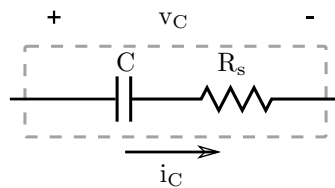


Figure 4.6: Capacitor model with equivalent series resistance and series inductance.

The above model was implemented in VHDL-AMS as shown in the listing below. The final capacitor voltage evaluates to the sum of the main capacitance effect and the series resistance and inductance effects.

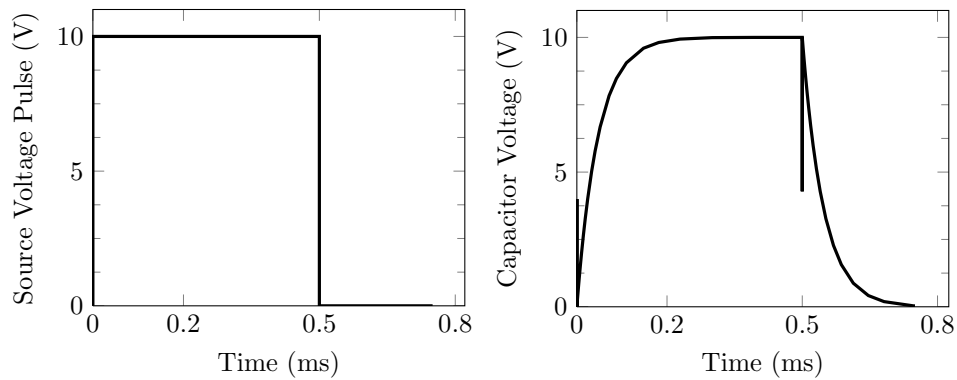
Listing 4.1: VHDL-AMS model for a practical capacitor.

```

1  -- Main capacitance effect, with optional initial voltage
2  if domain = quiescent_domain and v_ic /= real'low use
3    vc == v_ic;
4  else
5    ic == cap*vc'dot;
6  end use;
7  -- Series resistance and inductance effects
8  v_esrl == esr*i_esrl + esl*i_esrl'dot;

```

A SystemVision testbench (Fig. 4.7) was created to apply a step to the capacitor model together with a series resistance. Two circuits were set up to compare the difference between capacitor models with and without parasitic effects. The result is shown in Fig. 4.8b. Voltage spikes are seen at 0 ms and 0.5 ms due to the parasitic inductance.



(a) Test Bench Pulse Source Voltage vs. Time. (b) Capacitor Voltage vs. Time for the capacitor model with parasitics included.

Figure 4.8: Voltage of pulse source (4.8a) and voltage of capacitor model with parasitics (4.8b).

4.2.3 Inductor Model

Fig. 4.9 shows a model of an inductor, with inductance and equivalent series resistance (ESR). The equation governing the model behaviour in terms of voltage across, v_L , and current through, i_L , is expressed in Eq. 4.12.

$$v_L = L \frac{di_L}{dt} + R_s i_L \quad (4.12)$$

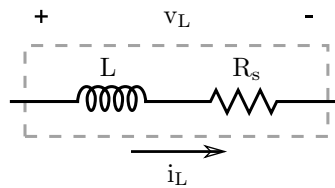


Figure 4.9: Inductor model with equivalent series resistance.

The above model was implemented in VHDL-AMS as shown in the listing below. The final inductor voltage evaluates to the sum of the main inductance effect and the series resistance effect.

Listing 4.2: VHDL-AMS model for a practical inductor.

```

1  -- Main inductance effect, with optional initial voltage
2  if domain = quiescent_domain and v_iL /= real'low use
3      vL == v_iL;
4  else
5      vL == ind*iL'dot;
6  end use;
7  -- Series resistance effects
8  v_esr == esr*i_esr;

```

A SystemVision testbench (Fig. 4.10) was created to apply a step to the capacitor model together with a series resistance. The result is shown in Fig. 4.11b. A voltage drop is seen over the inductor model with equivalent series resistance added.

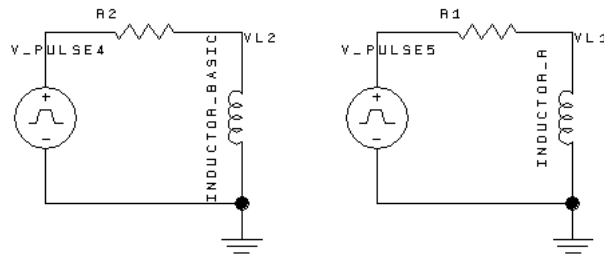
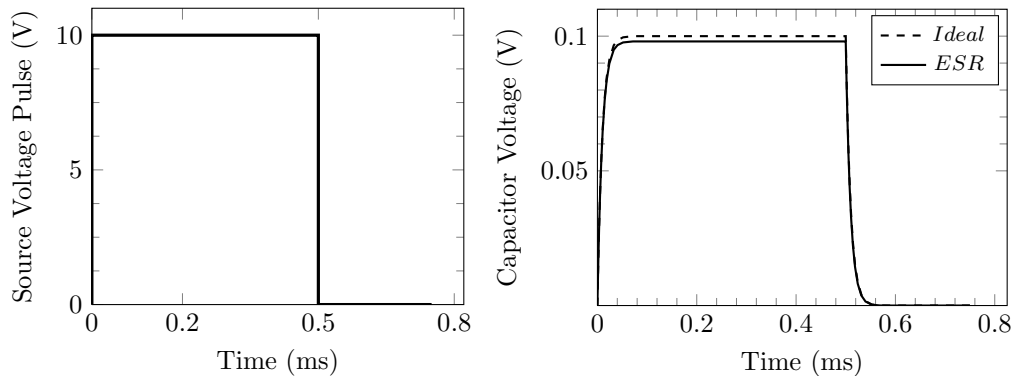


Figure 4.10: SystemVision Testbench for simulating the created VHDL-AMS models with and without parasitic effects.



(a) Test Bench Pulse Source Voltage vs. Time. (b) Inductor Current vs. Time for both the ideal and non-ideal models.

Figure 4.11: Voltage of pulse source (4.11a) and voltage of inductor model with parasitics (4.11b).

4.2.4 Dynamic Source Model

A component was required to simulate step-changes in the amplitude of the input voltage. A VHDL-AMS component was created to switch between three different reconfigurable voltage sources at pre-defined times. Fig. 4.12 shows the source voltage with a step at 5 ms and 25 ms.

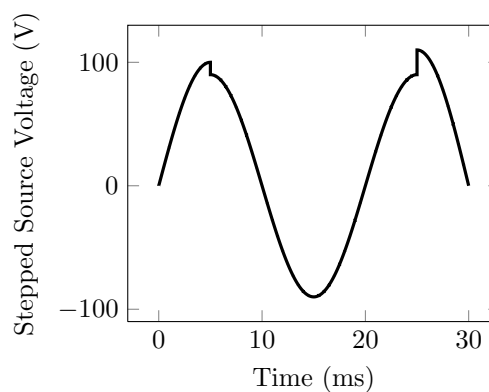


Figure 4.12: The output of the dynamic voltage source can switch from an initial amplitude to a new amplitude at a specified time, and can then also switch to a steady state voltage at a later time.

4.2.5 Dynamic Load Model

A dynamic inductive load model was designed in VHDL-AMS using SystemVision. The load elements assume pre-defined initial values, after which it switches to two other pre-defined values at pre-determined times. The

load is comprised of a resistor and inductor in series. This design was largely based on a description of a dynamic resistive load found in [45]. The listing of the dynamic inductive load is shown below.

Listing 4.3: VHDL-AMS model for a practical inductor.

```

1  --disengage load if necessary
2  if open_circuit use
3      iload == 0.0;
4  else
5      --use initial values in DC or Frequency analysis
6      if domain = quiescent_domain or domain = frequency_domain use
7          vload == r_init*iload + l_init*iload'dot;
8      else --normal governing equation
9          vload == r_eff*iload + l_eff*iload'dot;
10     end use;
11 end use;
12
13 --switch load values at appropriate times
14 switch : process is
15 begin
16     r_eff <= r_init;
17     l_eff <= l_init;
18     wait for time1;
19     r_eff <= r1;
20     l_eff <= l1;
21     wait for (time2-time1);
22     r_eff <= r2;
23     l_eff <= l2;
24     wait;
25 end process;
```

The load can be set to be disengaged by setting the generic 'open_circuit' parameter to 'true'. The initial values are used for dc and frequency analysis. The effective values of resistance and inductance are updated at the crucial intervals by the 'switch' process. Initial, intermediate, and steady-state values can be specified for the load resistance and inductance, as shown in Fig. 4.13.

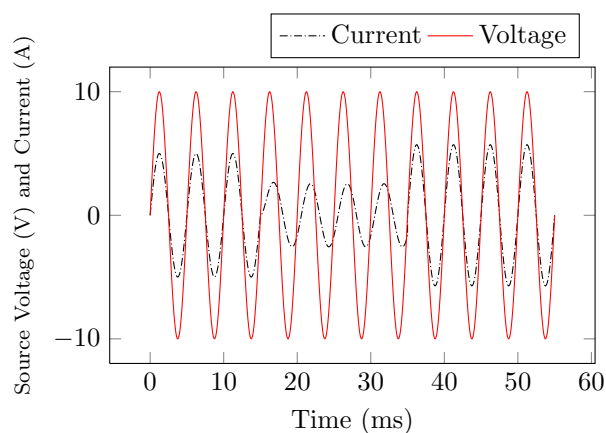


Figure 4.13: Dynamic load current and voltage waveforms. The load steps occur at 15 ms and 35 ms.

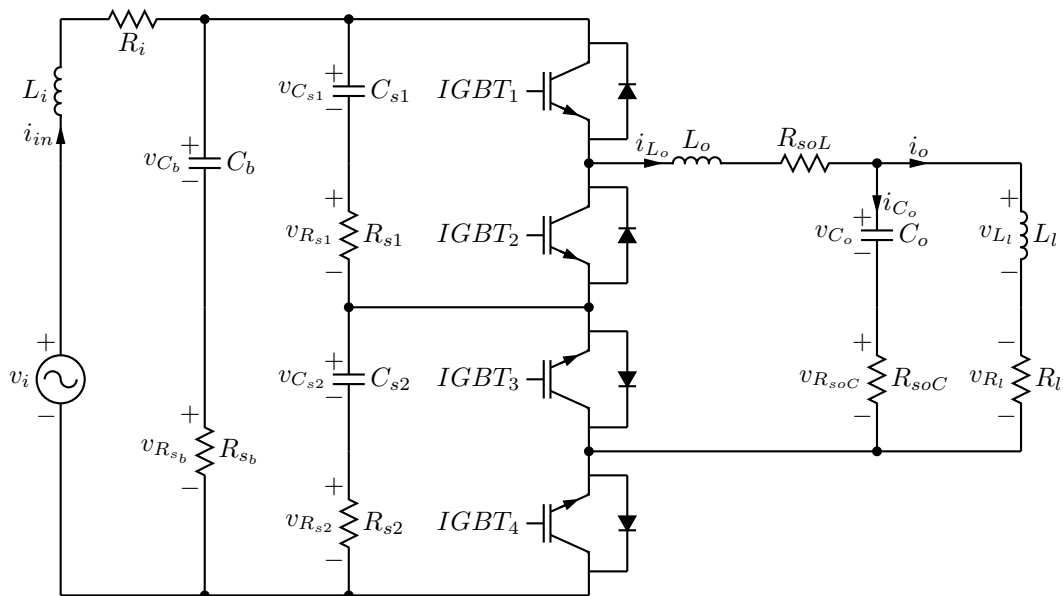


Figure 4.14: Stand-alone configuration of the MVEVR voltage regulator unit.

4.3 System Level Modelling and Simulation

The MVEVR consists of two voltage regulator units with their outputs connected in series with the input voltage. The regulator inputs are each connected to a 5% secondary terminal of a three-winding transformer, of which the primary winding is connected to the input as well.

The generic voltage regulator was first modelled as a stand-alone unit (Fig. 4.14), with a regular AC source (with equivalent leakage inductance and series resistance added) connected to the input, and a inductive load connected over the output.

A switching model was derived and differential equations were deduced for both the “on” (Fig. 4.15a) and the “off” (Fig. 4.15b) switching state. The commutation scheme used in the system allowed for some simplification to be made to the model. According to the commutation scheme, IGBTs 3 and 4 are turned on for as long as the input voltage is positive. This results in snubber capacitor C_{s2} to be shorted out, and is effectively removed from the model. Subber capacitor C_{s1} is found to be in parallel with the bus capacitor, and these two are combined into an equivalent capacitor, C_{bs} . The parasitic resistances of the two capacitors are also combined into R_{sbs} . The commutation scheme determines that IGBTs 1 and 2 are turned on whenever the input voltage is negative. This follows the natural symmetry of the circuit and, after the appropriate simplifications, yields the same equivalent circuit as in the case when the input voltage is positive.

It is clear that the load is connected to the source in the “on” state and is consequently being energized. During the “off” state, the load is disconnected from the source and the output circuit is de-energized.

State variables were assigned to each active element (inductor currents and capacitor voltages) and differential equations were derived for each state separately. Equivalent series resistances were incorporated in the model for all physical capacitors and inductors.

4.3.1 On State

The state variables were defined as follows:

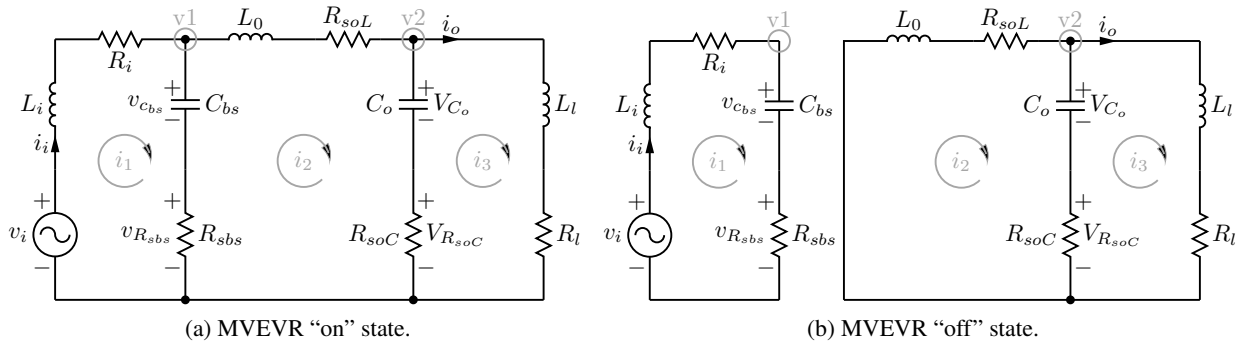


Figure 4.15: Equivalent circuit diagrams of the MVEVR switching states. Kirchhoff voltage nodes and mesh currents relevant to the calculations are shown.

$$\mathbf{x} = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \end{bmatrix} = \begin{bmatrix} i_i \\ v_{C_{bs}} \\ i_{L_o} \\ v_{C_o} \\ i_o \end{bmatrix} \quad (4.13)$$

In the “on” state, mesh currents i_1 , i_2 , and i_3 (refer to Fig. 4.15) were used respectively to derive the following equations:

$$v_i = L_i \cdot \frac{di_{in}}{dt} + R_i i_{in} + v_{C_{bs}} + C_{bs} \cdot \frac{dv_{C_{bs}}}{dt} \cdot R_{sbs} \quad (4.14)$$

$$v_{C_{bs}} + C_{bs} \cdot \frac{dv_{C_{bs}}}{dt} \cdot R_{sbs} = L_o \cdot \frac{di_{L_o}}{dt} + i_{L_o} \cdot R_{soL} + v_{C_o} + C_o \cdot \frac{dv_{C_o}}{dt} \cdot R_{soC} \quad (4.15)$$

$$v_{C_o} + C_o \cdot \frac{dv_{C_o}}{dt} \cdot R_{soC} = L_l \cdot \frac{di_o}{dt} + R_l i_o \quad (4.16)$$

Kirchhoff’s current law was applied to nodes v1 and v2 respectively to yield the following equations:

$$i_{L_o} = i_{in} - C_{bs} \cdot \frac{dv_{C_{bs}}}{dt} \quad (4.17)$$

$$i_{L_o} = C_o \cdot \frac{dv_{C_o}}{dt} + i_o \quad (4.18)$$

The solution in terms of the differentiated variables:

$$\dot{i}_{in} = -\frac{R_{sbs} + R_i}{L_i} \cdot i_{in} - \frac{1}{L_i} \cdot v_{C_{bs}} + \frac{R_{sbs}}{L_i} \cdot i_{L_o} + \frac{1}{L_i} \cdot v_i \quad (4.19)$$

$$\dot{v}_{C_{bs}} = \frac{1}{C_{bs}} \cdot i_{in} - \frac{1}{C_{bs}} \cdot i_{L_o} \quad (4.20)$$

$$\dot{i}_{L_o} = \frac{R_{sbs}}{L_o} i_{in} + \frac{1}{L_o} v_{C_{bs}} - \frac{R_{soL} + R_{soC} + R_{sbs}}{L_o} \cdot i_{L_o} - \frac{1}{L_o} \cdot v_{C_o} + \frac{R_{soC}}{L_o} \cdot i_o \quad (4.21)$$

$$\dot{v}_{C_o} = \frac{1}{C_o} \cdot i_{L_o} - \frac{1}{C_o} \cdot i_o \quad (4.22)$$

$$i_o = \frac{R_{soC}}{L_l} \cdot i_{L_o} + \frac{1}{L_l} \cdot v_{C_o} - \frac{R_{soC} + R_l}{L_l} \cdot i_o \quad (4.23)$$

This results in the following state space representation:

$$\dot{\mathbf{x}} = \mathbf{A}_{on}\mathbf{x} + \mathbf{F}_{on} \quad (4.24)$$

$$\mathbf{A}_{on} = \begin{bmatrix} -\frac{R_{s_{bs}}+R_i}{L_i} & -\frac{1}{L_i} & \frac{R_{s_{bs}}}{L_i} & 0 & 0 \\ \frac{1}{C_{bs}} & 0 & -\frac{1}{C_{bs}} & 0 & 0 \\ \frac{R_{s_{bs}}}{L_o} & \frac{1}{L_o} & -\frac{R_{soL}+R_{soC}+R_{s_{bs}}}{L_o} & -\frac{1}{L_o} & \frac{R_{soC}}{L_o} \\ 0 & 0 & \frac{1}{C_o} & 0 & -\frac{1}{C_o} \\ 0 & 0 & \frac{R_{soC}}{L_l} & \frac{1}{L_l} & -\frac{R_{soC}+R_l}{L_l} \end{bmatrix} \quad (4.25)$$

$$\mathbf{F}_{on} = \begin{bmatrix} \frac{1}{L_i} V_i \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (4.26)$$

4.3.2 Off State

In the “off” state, mesh currents i_1 , i_2 , and i_3 were used respectively to derive the following equations:

$$v_i = L_i \cdot \frac{di_i}{dt} + R_i i_{in} + v_{C_{bs}} + C_{bs} \cdot \frac{dv_{C_{bs}}}{dt} \cdot R_{s_{bs}} \quad (4.27)$$

$$L_o \cdot \frac{di_{L_o}}{dt} = -i_{L_o} \cdot R_{soL} - v_{C_o} - C_o \cdot \frac{dv_{C_o}}{dt} \cdot R_{soC} \quad (4.28)$$

$$v_{C_o} + C_o \cdot \frac{dv_{C_o}}{dt} \cdot R_{soC} = L_l \cdot \frac{di_o}{dt} + R_l i_o \quad (4.29)$$

Kirchhoff's current law was applied to nodes v_1 and v_2 respectively to yield the following equations:

$$i_{in} = C_{bs} \cdot \frac{dv_{C_{bs}}}{dt} \quad (4.30)$$

$$i_{L_o} = C_o \cdot \frac{dv_{C_o}}{dt} + i_o \quad (4.31)$$

The solution in terms of the differentiated variables:

$$\dot{i}_{in} = -\frac{R_{s_{bs}}+R_i}{L_i} \cdot i_{in} - \frac{1}{L_i} \cdot v_{C_{bs}} + \frac{1}{L_i} \cdot v_i \quad (4.32)$$

$$\dot{v}_{C_{bs}} = \frac{1}{C_{bs}} \cdot i_{in} \quad (4.33)$$

$$\dot{i}_{L_o} = -\frac{R_{soL}+R_{soC}}{L_o} \cdot i_{L_o} - \frac{1}{L_o} \cdot v_{C_o} + \frac{R_{soC}}{L_o} \cdot i_o \quad (4.34)$$

$$\dot{v}_{C_o} = \frac{1}{C_o} \cdot i_{L_o} - \frac{1}{C_o} \cdot i_o \quad (4.35)$$

$$i_o = \frac{R_{soC}}{L_l} \cdot i_{L_o} + \frac{1}{L_l} \cdot v_{C_o} - \frac{R_{soC} + R_l}{L_l} \cdot i_o \quad (4.36)$$

This results in the following state space representation:

$$\dot{\mathbf{x}} = \mathbf{A}_{off} \mathbf{x} + \mathbf{F}_{off} \quad (4.37)$$

$$\mathbf{A}_{off} = \begin{bmatrix} -\frac{R_{sbs} + R_i}{L_i} & -\frac{1}{L_i} & 0 & 0 & 0 \\ \frac{1}{C_{bs}} & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{R_{soL} + R_{soC}}{L_o} & -\frac{1}{L_o} & \frac{R_{soC}}{L_o} \\ 0 & 0 & \frac{1}{C_o} & 0 & -\frac{1}{C_o} \\ 0 & 0 & \frac{R_{soC}}{L_l} & \frac{1}{L_l} & -\frac{R_{soC} + R_l}{L_l} \end{bmatrix} \quad (4.38)$$

$$\mathbf{F}_{off} = \begin{bmatrix} \frac{1}{L_i} \cdot v_i \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (4.39)$$

4.3.3 Combined Switching Model

The “on” state and the “off” state can be combined in a switching model by introducing a discontinuous term in the right-hand-side of the differential equations. This term will be called the control variable, u , and satisfies:

$$u \in \{0, 1\} \quad (4.40)$$

where '0' represents the off state and '1' represents the on state. Then the system is represented as follows:

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, t) + \mathbf{B}(\mathbf{x}, t)u \quad (4.41)$$

$$= \mathbf{A}\mathbf{x} + \mathbf{B}u + \mathbf{F} \quad (4.42)$$

The models were combined to form the switching model in the following way:

$$\mathbf{A} = \mathbf{A}_{off} \quad (4.43)$$

$$\mathbf{B} = (\mathbf{A}_{on} - \mathbf{A}_{off}) \mathbf{x} + (\mathbf{F}_{on} - \mathbf{F}_{off}) \quad (4.44)$$

$$\mathbf{F} = \mathbf{F}_{off} \quad (4.45)$$

The above yields the following matrices:

$$\mathbf{A} = \begin{bmatrix} -\frac{R_{s_{bs}}+R_i}{L_i} & -\frac{1}{L_i} & 0 & 0 & 0 \\ \frac{1}{C_{bs}} & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{R_{soL}+R_{soC}}{L_o} & -\frac{1}{L_o} & \frac{R_{soC}}{L_o} \\ 0 & 0 & \frac{1}{C_o} & 0 & -\frac{1}{C_o} \\ 0 & 0 & \frac{R_{soC}}{L_i} & \frac{1}{L_i} & -\frac{R_{soC}+R_l}{L_i} \end{bmatrix} \quad (4.46)$$

$$\mathbf{B} = \begin{bmatrix} \frac{R_{s_{bs}} \cdot i_{L_o}}{L_i} \\ -\frac{i_{L_o}}{C_{bs}} \\ \frac{v_{C_{bs}} - R_{s_{bs}} \cdot i_{L_o} + R_{s_{bs}} \cdot i_i}{L_o} \\ 0 \\ 0 \end{bmatrix} \quad (4.47)$$

$$\mathbf{F} = \begin{bmatrix} \frac{1}{L_i} \cdot v_i \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (4.48)$$

4.3.4 Control-to-Output Averaged Model and Transfer Function

In the above section, the off-state and on-state were combined to form a switching model, with u as the control variable. This control variable is not constrained to any formal scheme of switching. With classical sliding-mode control (SMC), the switching will happen “just in time” (not at a fixed frequency), based on the state of the system relative to the references at any given time. With a PWM scheme, switching happens at a fixed frequency, with the switching time determined by a periodic modulation signal.

In simulations where the switching action is not of interest, it is useful to have an average model, where the switching dynamics are ignored, but an accurate average representation is nonetheless obtained. This is more computationally efficient, because the state variables have to be solved only once per switching period instead of at least twice (as with a PWM scheme). System representations are generally linearized during the averaging process. The averaged models are therefore also useful for deriving transfer functions. The average model in this section is derived specifically with a control-action-to-output transfer function in mind.

Average models for converters using PWM control have been thoroughly developed[41], where the known duty cycle at the start of every fixed switching period is an integral part of the model. It is not possible to derive an average model to accurately represent the “just in time” action of a converter with a classical SMC scheme because the switching frequency is not fixed, nor is the “duty cycle” known at the start of the switching period. In this thesis, a quasi-SMC scheme is developed where the switching frequency is fixed, but the effective “duty cycle” is still unknown up to the actual time of switching. It has been shown, however, that if the switching frequency is high enough, the average model for a PWM controlled converter will approximate the average behaviour of a quasi-SMC converter.[49]

An averaged model was created according to the method of Middebrook and Cúk, and was later also used to derive a transfer function for the converter.

In a PWM scheme, the duty cycle is the fundamental control input. The duty cycle, d , is defined as the fraction of the switching period that the converter is in the ‘on’ state and is a number in between 0 and 1. Relating the model of the converter’s different switching states to the duty cycle:

$$\dot{\mathbf{x}} = \begin{cases} \mathbf{A}_{on}\mathbf{x} + \mathbf{F}_{on} & \text{during } dT_s \\ \mathbf{A}_{off}\mathbf{x} + \mathbf{F}_{off} & \text{during } (1-d)T_s \end{cases} \quad (4.49)$$

and

$$x_{out} = \begin{cases} \mathbf{C}_{on}\mathbf{x} & \text{during } dT_s \\ \mathbf{C}_{off}\mathbf{x} & \text{during } (1-d)T_s \end{cases}. \quad (4.50)$$

Take note that the \mathbf{F} matrices are defined in terms of the regulator input voltage, V_i , which is a 50Hz sinusoid. This non-linear input signal is a problem for a fundamentally linear transfer function. The frequency of the input voltage is, however, much lower than the switching frequency (10kHz). The transfer function will therefore be linearized about the instantaneous value of the input voltage. The input voltage will then be expressed in the transfer function as a DC value, V_{in} . When the system's frequency response is evaluated using the transfer function under consideration, a sweep will have to be done across a range of DC operating points, representing the range of instantaneous amplitudes in the AC input voltage signal.

The system output is represented by x_{out} , and would normally be the output voltage.

The first step in the derivation of the transfer function is to take the average of the two switching states over one switching period:

$$\dot{\mathbf{x}} = [\mathbf{A}_{on}d + \mathbf{A}_{off}(1-d)]\mathbf{x} + [\mathbf{F}_{on}d + \mathbf{F}_{off}(1-d)] \quad (4.51)$$

and

$$x_{out} = [\mathbf{C}_{on}d + \mathbf{C}_{off}(1-d)]\mathbf{x} \quad (4.52)$$

The state space vector, the duty cycle, and the output signal are separated into each of their respective constant and dynamic (time-varying) components. In steady-state, the time-varying components are assumed to exhibit small changes relative to the constant components during any given switching period.

$$\mathbf{x} = \mathbf{X} + \tilde{\mathbf{x}} \quad (4.53)$$

$$d = D + \tilde{d} \quad (4.54)$$

$$x_{out} = X_{out} + \tilde{x}_{out} \quad (4.55)$$

Now Eqs. 4.53 and 4.54 are substituted into Eq. 4.51: (note that $\dot{\mathbf{X}} = 0$)

$$\dot{\mathbf{x}} = \dot{\mathbf{X}} + \dot{\tilde{\mathbf{x}}} \quad (4.56)$$

$$= [\mathbf{A}_{on}(D + \tilde{d}) + \mathbf{A}_{off}(1 - (D + \tilde{d}))](\mathbf{X} + \tilde{\mathbf{x}}) + [\mathbf{F}_{on}(D + \tilde{d}) + \mathbf{F}_{off}(1 - (D + \tilde{d}))] \quad (4.57)$$

$$\simeq \mathbf{A}_{av}\mathbf{X} + \mathbf{F}_{av} + \mathbf{A}_{av}\tilde{\mathbf{x}} + [(\mathbf{A}_{on} - \mathbf{A}_{off})\mathbf{X} + (\mathbf{F}_{on} - \mathbf{F}_{off})]\tilde{d} \quad (4.58)$$

$$\simeq \mathbf{A}_{av}\mathbf{X} + \mathbf{F}_{av} + \mathbf{A}_{av}\tilde{\mathbf{x}} + [(\mathbf{A}_{on} - \mathbf{A}_{off})\mathbf{X}]\tilde{d}, \quad (4.59)$$

$$\begin{aligned}
\dot{\mathbf{x}} &= \dot{\mathbf{X}} + \dot{\tilde{\mathbf{x}}} \\
&= [\mathbf{A}_{on}(D + \tilde{d}) + \mathbf{A}_{off}(1 - (D + \tilde{d}))](\mathbf{X} + \tilde{\mathbf{x}}) \\
&\quad + [\mathbf{F}_{on}(D + \tilde{d}) + \mathbf{F}_{off}(1 - (D + \tilde{d}))] \\
&= \mathbf{A}_{av}\mathbf{X} + \mathbf{F}_{av} + \mathbf{A}_{av}\tilde{\mathbf{x}} + [(\mathbf{A}_{on} - \mathbf{A}_{off})\mathbf{X} + (\mathbf{F}_{on} - \mathbf{F}_{off})]\tilde{d} \\
&= \mathbf{A}_{av}\mathbf{X} + \mathbf{F}_{av} + \mathbf{A}_{av}\tilde{\mathbf{x}} + [(\mathbf{A}_{on} - \mathbf{A}_{off})\mathbf{X}]\tilde{d}, \quad (4.60)
\end{aligned}$$

since $\mathbf{F}_{on} - \mathbf{F}_{off} = 0$, where

$$\mathbf{A}_{av} = \mathbf{A}_{on}D + \mathbf{A}_{off}(1 - D) \quad (4.61)$$

$$= \begin{bmatrix} -\frac{R_{sbs} + R_i}{L_i} & -\frac{1}{L_i} & \frac{R_{sbs}D}{L_i} & 0 & 0 \\ \frac{1}{C_{bs}D} & 0 & -\frac{D}{C_{bs}} & 0 & 0 \\ \frac{R_{sbs}D}{L_o} & \frac{D}{L_o} & -\frac{R_{sol} + R_{soc} + R_{sbs}D}{L_o} & -\frac{1}{L_o} & \frac{R_{soc}}{L_o} \\ 0 & 0 & \frac{1}{C_o} & 0 & -\frac{1}{C_o} \\ 0 & 0 & \frac{R_{soc}}{L_l} & \frac{1}{L_l} & -\frac{R_{soc} + R_l}{L_l} \end{bmatrix} \quad (4.62)$$

$$\mathbf{F}_{av} = \mathbf{F}_{on}D + \mathbf{F}_{off}(1 - D) \quad (4.63)$$

$$= \begin{bmatrix} \frac{1}{L_i} \cdot V_i \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}. \quad (4.64)$$

Eq. 4.59 was indicated as an approximation, because terms containing products of $\tilde{\mathbf{x}}$ and \tilde{d} were assumed to be of negligible magnitude and left out.

The constant and dynamic components of Eq. 4.59 are assumed to be entirely de-coupled and separable. In that case

$$\dot{\mathbf{X}} = \mathbf{A}_{av}\mathbf{X} + \mathbf{F}_{av} = 0. \quad (4.65)$$

Substituting Eq. 4.65 into 4.59 yields a simplified expression of the dynamic behaviour of the state space variables in steady-state:

$$\tilde{\mathbf{x}} = \mathbf{A}_{av}\tilde{\mathbf{x}} + [(\mathbf{A}_{on} - \mathbf{A}_{off})\mathbf{X}]\tilde{d}. \quad (4.66)$$

The steady state value of the converter's state space variables at a given duty cycle can be easily determined from Eq. 4.65 by solving for \mathbf{X} :

$$\mathbf{X} = \mathbf{A}_{av}^{-1} \cdot (-\mathbf{F}_{av}) \quad (4.67)$$

The above equation was solved in wxMaxima⁷, simplified, and factorised. The result is :

⁷wxMaxima is an open-source, cross-platform symbolic math solver.

$$\mathbf{X} = \frac{V_i}{(R_{sbs} - R_i)D^2 + (2R_{soC} + R_{sbs})D - R_{soL} - R_l} \cdot \begin{bmatrix} D^2 \\ R_{sbs}D^2 + (2R_{soC} + R_{sbs})D - R_{soL} - R_l \\ -D \\ -R_lD \\ -D \end{bmatrix} \quad (4.68)$$

Similarly for the output variable, Eq. 4.55 is substituted into Eq. 4.52 (note that $\dot{X}_{out} = 0$):

$$x_{out} = X_{out} + \tilde{x}_{out} = [\mathbf{C}_{on}(D + \tilde{d}) + \mathbf{C}_{off}(1 - (D + \tilde{d}))](\mathbf{X} + \tilde{\mathbf{x}}) \quad (4.69)$$

$$\simeq \mathbf{C}_{av}\mathbf{X} + \mathbf{C}_{av}\tilde{\mathbf{x}} + [(\mathbf{C}_{on} - \mathbf{C}_{off})\mathbf{X}]\tilde{d} \quad (4.70)$$

where

$$\mathbf{C}_{av} = \mathbf{C}_{on}D + \mathbf{C}_{off}(1 - D). \quad (4.71)$$

Eq. 4.70 was indicated as an approximation, because terms containing products of $\tilde{\mathbf{x}}$ and \tilde{d} were assumed to be of negligible magnitude and left out.

In steady-state, $X_{out} = \mathbf{C}_{av}\mathbf{X}$. Substituting this into Eq. 4.70 yields the following:

$$\tilde{x}_{out} = \mathbf{C}_{av}\tilde{\mathbf{x}} + [(\mathbf{C}_{on} - \mathbf{C}_{off})\mathbf{X}]\tilde{d}. \quad (4.72)$$

Time Simulation of Averaged Model

Time simulation was done using MATLAB's *expm()* function. Components and parasitic values were used as shown in Table 4.5.

The computational loop is shown in the program listing below, where *f_Vt()* evaluates to $v_i(t)$, and *mA_av* is the same as the averaged A-matrix, A_{av} . The following is done for every switching period:

1. The input voltage is changed to the next DC operating point, corresponding to the instantaneous value of a 50Hz sinusoidal signal with realistic amplitude.
2. The steady state particular solution (if the input voltage were to remain at it's current value) is determined according to Eq. 4.68.
3. The solution to $\dot{\mathbf{x}} = \mathbf{A}_{av}\mathbf{x} + \mathbf{F}_{av}$ is given by:

$$\mathbf{x} = K \cdot e^{T_s \mathbf{A}_{av}} + \mathbf{x}_p, \quad (4.73)$$

where K is a constant based on the initial conditions and \mathbf{x}_p is the steady-state particular solution.

Listing 4.4: Crucial Code Fragment of Average Model Simulation

```

1 for n = 1:N
2     %update input voltage
3     Vt = f_Vt(t(n));
4
5     %calculate steady-state (SS) value for current Vt

```

```

6     Xp_av = (Vt/(Ri*D^2+Rl)).*[(D^2); Rl; D; Rl*D; D]
7
8     %K is calculated based on SS values
9     K = X(:,n) - Xp_av;
10
11    %Solve for X using Averaged A-matrix and SS values
12    X(:,n+1) = expm((Ts)*mA_av)*K + Xp_av;
13
14    %Update Time
15    t(n+1) = t(n)+ Ts;
16 end

```

Table 4.5: Component values for time simulation of averaged model.

Component	Value	ESR
L_i	138.4 μ H	
R_i	19.05 m Ω	
C_b	90 μ F	1 m Ω ⁸
C_s	1.5 μ F	24.6 m Ω ⁹
L_o	850 μ F	314.2 m Ω ¹⁰
C_o	75 μ F	6.67 m Ω ¹¹
R_l	2.50 Ω	
L_l	20 mH	

Time simulation graphs show the switching model compared to the averaged model. The correspondence is near-perfect. The average model shows some minor divergence from the switching model in the case of the input current. This is probably due to the linearization of the average model.

⁸The ESR as specified in the datasheet was used.

⁹The ESR as specified in the datasheet was used.

¹⁰The output filter's ESR was approximated by adding the measured DC resistance to an equivalent resistance representing the theoretical core losses caused by the 10kHz current ripple.

¹¹The ESR as specified in the datasheet was used.

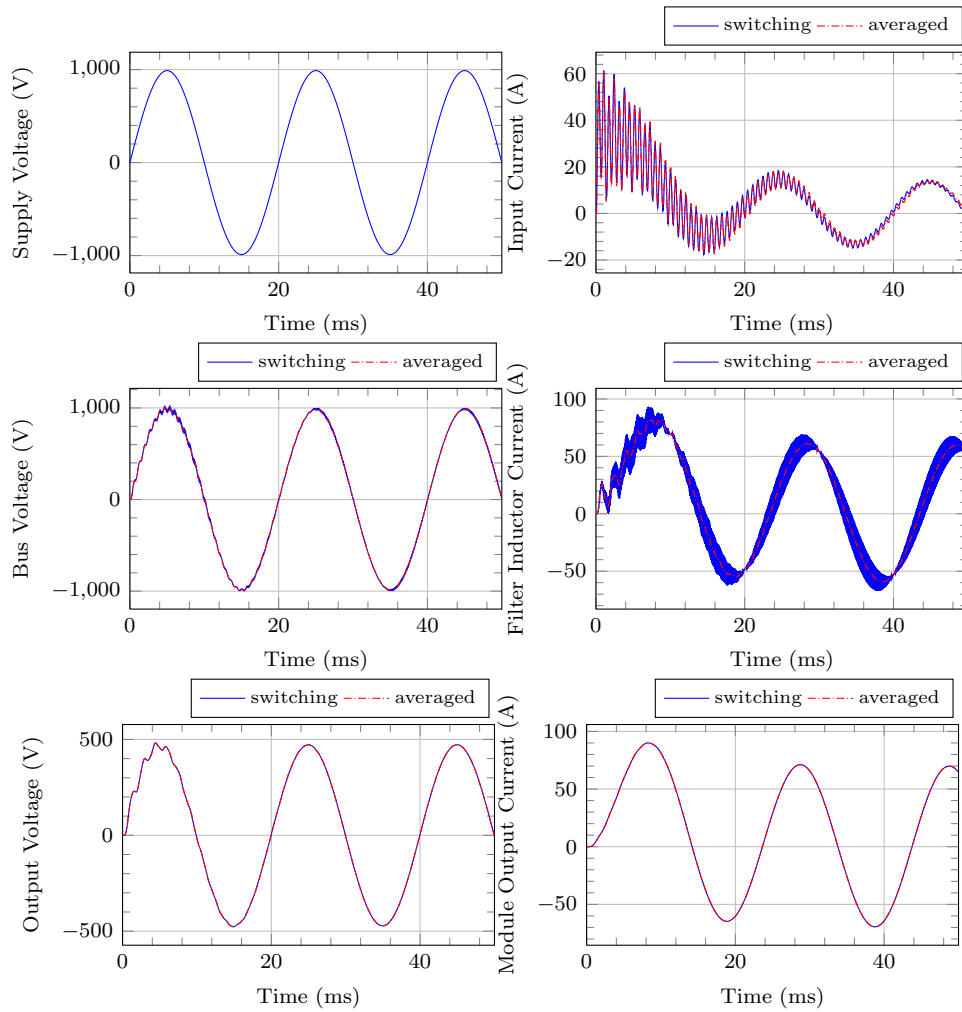


Figure 4.16: Good correspondence between the switching model (blue) and the averaged model (red).

Transfer Function of the Model

To obtain the s-domain transfer function, the Laplace transform is applied to Eq. 4.66:

$$\dot{\mathbf{x}} = \dot{\tilde{\mathbf{x}}} \simeq \mathbf{A}_{av}\tilde{\mathbf{x}} + [(\mathbf{A}_{on} - \mathbf{A}_{off})\mathbf{X}] \tilde{d}$$

$$s\tilde{\mathbf{x}}(s) = \mathbf{A}_{av}\tilde{\mathbf{x}}(s) + [(\mathbf{A}_{on} - \mathbf{A}_{off})\mathbf{X}] \tilde{d}(s) \quad (4.74)$$

$$\tilde{\mathbf{x}}(s) = (s\mathbf{I} - \mathbf{A}_{av})^{-1} [(\mathbf{A}_{on} - \mathbf{A}_{off})\mathbf{X}] \tilde{d}(s) \quad (4.75)$$

The Laplace transform is also applied to the equation describing the output variable dynamics in steady state (Eq. 4.72):

$$\tilde{x}_{out} = \mathbf{C}_{av}\tilde{\mathbf{x}} + [(\mathbf{C}_{on} - \mathbf{C}_{off})\mathbf{X}] \tilde{d}$$

$$\tilde{x}_{out}(s) = \mathbf{C}_{av}\tilde{\mathbf{x}}(s) + [(\mathbf{C}_{on} - \mathbf{C}_{off})\mathbf{X}] \tilde{d}(s). \quad (4.76)$$

By substituting Eq. 4.75 into Eq. 4.76, and solving for $\frac{\tilde{x}_{out}(s)}{\tilde{d}(s)}$, the transfer function for any output variable is obtained:

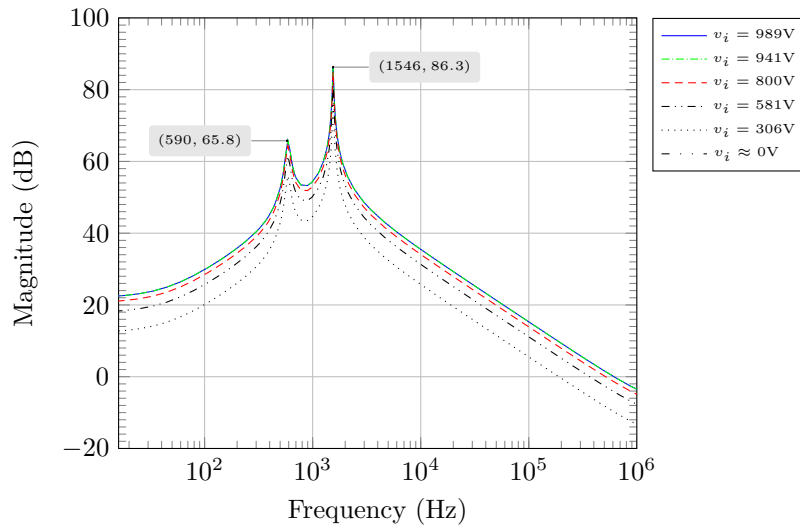


Figure 4.17: Magnitude spectrum of the transfer function, $G(s) = \frac{\tilde{V}_{bus}}{\tilde{d}}$, showing the effect of the control input on the bus voltage. The bus voltage was selected as output variable with the following selection matrices: $C_{on} = [R_{s_{bs}} \ 1 \ -R_{s_{bs}} \ 0 \ 0]$, $C_{off} = [R_{s_{bs}} \ 1 \ -R_{s_{bs}} \ 0 \ 0]$.

$$\frac{\tilde{x}_{out}(s)}{\tilde{d}(s)} = \mathbf{C}_{av}(s\mathbf{I} - \mathbf{A}_{av})^{-1}[(\mathbf{A}_{on} - \mathbf{A}_{off})\mathbf{X}] + [(\mathbf{C}_{on} - \mathbf{C}_{off})\mathbf{X}] \quad (4.77)$$

This transfer function can be used to obtain the steady-state frequency content of any of the state variables by simply choosing the appropriate \mathbf{C} selection matrices.

The transfer functions for each of the state variables were studied. The corresponding magnitude responses of the bus voltage (Fig. 4.17) and the output voltage (Fig. 4.18) are shown. The duty cycle is kept at unity, while the different magnitude responses for various input voltage magnitudes are shown. The resonant peaks remain at the same frequency as the input voltage varies. It will be shown in Section 4.3.5 that the frequency of the peaks are determined by the duty-cycle. The input voltage only causes a rise or fall in the magnitude.

The magnitude response of the output voltage is, for the lower frequencies, constantly the amplitude of the output (which is basically the same as the input, because the duty cycle is unity). The leftmost resonant peak, found at 590Hz, is caused by the interaction between the output filter and the inductive load. For a purely resistive load, this peak disappears. The rightmost resonant peak is brought about by the interaction between the transformer's leakage inductance and the bus capacitance.

It can be seen that the input current and bus voltage have natural resonance are prone to oscillations at 719Hz. This is troublesome as it can cause instability at lower frequencies.

4.3.5 Input-to-Output Average Model and Transfer Function

The transfer function derived in Section 4.3.4 was useful to see the effect of the control input on the output signal. It is also desirable to analyse the effect of input voltage perturbations on the output signals, while the effective duty cycle remains constant.

The transfer function was also modified to model $\frac{\tilde{x}_{out}}{\tilde{v}_{in}(s)}$, with $\tilde{v}_{in}(s)$ representing AC perturbations in an otherwise constant input signal. In contrast with the previous transfer function, then the 50Hz input signal (and its non-idealities) can be modelled as 'perturbations' to a DC signal with zero amplitude. In order to do this, the average model had to be modified as well.

Firstly we revisit our model, where the \mathbf{F} matrices are contingent on the now time-varying input voltage, v_i

:

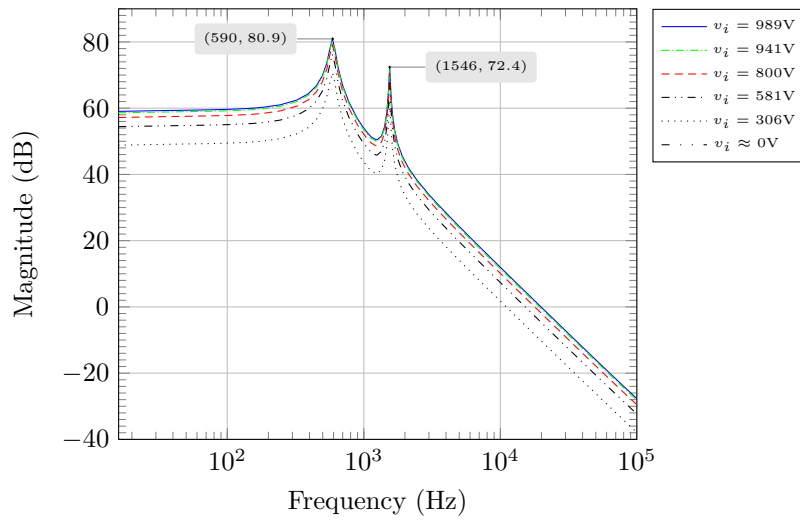


Figure 4.18: Magnitude spectrum of the transfer function, $G(s) = \frac{\hat{V}_{out}}{d}$, showing the effect of the control input on the output voltage. The output voltage was selected as output variable with the following selection matrices: $\mathbf{C}_{on} = [0 \ 0 \ R_{soC} \ 1 \ -R_{soC}]$, $\mathbf{C}_{off} = [0 \ 0 \ R_{soC} \ 1 \ -R_{soC}]$.

$$\dot{\mathbf{x}} = \begin{cases} \mathbf{A}_{on}\mathbf{x} + \mathbf{F}_{on} & \text{during } dT_s \\ \mathbf{A}_{off}\mathbf{x} + \mathbf{F}_{off} & \text{during } (1-d)T_s \end{cases} \quad (4.78)$$

and

$$x_{out} = \begin{cases} \mathbf{C}_{on}\mathbf{x} & \text{during } dT_s \\ \mathbf{C}_{off}\mathbf{x} & \text{during } (1-d)T_s \end{cases}. \quad (4.79)$$

The system output is represented by x_{out} , and would normally be the output voltage. As before, we take the average of the two switching states over one switching period:

$$\dot{\mathbf{x}} = [\mathbf{A}_{on}d + \mathbf{A}_{off}(1-d)]\mathbf{x} + [\mathbf{F}_{on}d + \mathbf{F}_{off}(1-d)]. \quad (4.80)$$

and

$$x_{out} = [\mathbf{C}_{on}d + \mathbf{C}_{off}(1-d)]\mathbf{x} \quad (4.81)$$

Written more compactly:

$$\dot{\mathbf{x}} = \mathbf{A}_{av}\mathbf{x} + \mathbf{F}_{av} \quad (4.82)$$

and

$$x_{out} = \mathbf{C}_{av}\mathbf{x}, \quad (4.83)$$

where

$$\mathbf{A}_{av} = \mathbf{A}_{on}D + \mathbf{A}_{off}(1 - D) \quad (4.84)$$

$$= \begin{bmatrix} -\frac{R_{sbs} + R_i}{L_i} & -\frac{1}{L_i} & \frac{R_{sbs}D}{L_i} & 0 & 0 \\ \frac{1}{C_{bs}} & 0 & -\frac{D}{C_{bs}} & 0 & 0 \\ \frac{R_{sbs}D}{L_o} & \frac{D}{L_o} & -\frac{R_{soL} + (R_{soC} + R_{sbs})D}{L_o} & -\frac{1}{L_o} & \frac{R_{soC}D}{L_o} \\ 0 & 0 & \frac{1}{C_o} & 0 & -\frac{1}{C_o} \\ 0 & 0 & \frac{R_{soC}}{L_l} & \frac{1}{L_l} & -\frac{R_{soC} + R_l}{L_l} \end{bmatrix} \quad (4.85)$$

$$\mathbf{F}_{av} = \mathbf{F}_{on}D + \mathbf{F}_{off}(1 - D) \quad (4.86)$$

$$= \begin{bmatrix} \frac{1}{L_i} v_i \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}. \quad (4.87)$$

$$\mathbf{C}_{av} = \mathbf{C}_{on}D + \mathbf{C}_{off}(1 - D). \quad (4.88)$$

The solution for \mathbf{X} remains the same as in Section 4.3.4 and Eq. 4.68, except that the input voltage is now time-varying. Because it varies at 50Hz, which is slow relative to the 10kHz switching frequency, the steady state is affected in a similar way as when the input was assumed to be constant.

$$\mathbf{X} = \frac{v_i}{(R_{sbs} - R_i)D^2 + (2R_{soC} + R_{sbs})D - R_{soL} - R_l} \cdot \begin{bmatrix} D^2 \\ R_{sbs}D^2 + (2R_{soC} + R_{sbs})D - R_{soL} - R_l \\ -D \\ -R_lD \\ -D \end{bmatrix}$$

Transfer Function of the Model

To obtain the s-domain transfer function, the Laplace transform is applied to Eq. 4.82:

$$\dot{\mathbf{x}} = \mathbf{A}_{av}\mathbf{x} + \mathbf{F}_{av}$$

$$s\dot{\mathbf{x}}(s) = \mathbf{A}_{av}\mathbf{x}(s) + \mathbf{F}_{av}(s) \quad (4.89)$$

$$\mathbf{x}(s) = (sI - \mathbf{A}_{av})^{-1}\mathbf{F}_{av}(s) \quad (4.90)$$

The Laplace transform is also applied to the equation describing the output variable dynamics in steady state (Eq. 4.83):

$$x_{out} = \mathbf{C}_{av}\mathbf{x}$$

$$x_{out}(s) = \mathbf{C}_{av}\mathbf{x}(s). \quad (4.91)$$

Table 4.6: Appropriate \mathbf{C} selection matrices corresponding to physical system measurements.

Measurement	\mathbf{C}_{on}	\mathbf{C}_{off}
Input current	$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 \end{bmatrix}$
Input Bus Voltage	$\begin{bmatrix} R_{sbs} & 1 & -R_{sbs} & 0 & 0 \end{bmatrix}$	$\begin{bmatrix} R_{sbs} & 1 & 0 & 0 & 0 \end{bmatrix}$
Inductor Current	$\begin{bmatrix} 0 & 0 & 1 & 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & 1 & 0 & 0 \end{bmatrix}$
Output Voltage	$\begin{bmatrix} 0 & 0 & R_{soC} & 1 & -R_{soC} \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & R_{soC} & 1 & -R_{soC} \end{bmatrix}$
Output Current	$\begin{bmatrix} 0 & 0 & 0 & 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & 0 & 0 & 1 \end{bmatrix}$

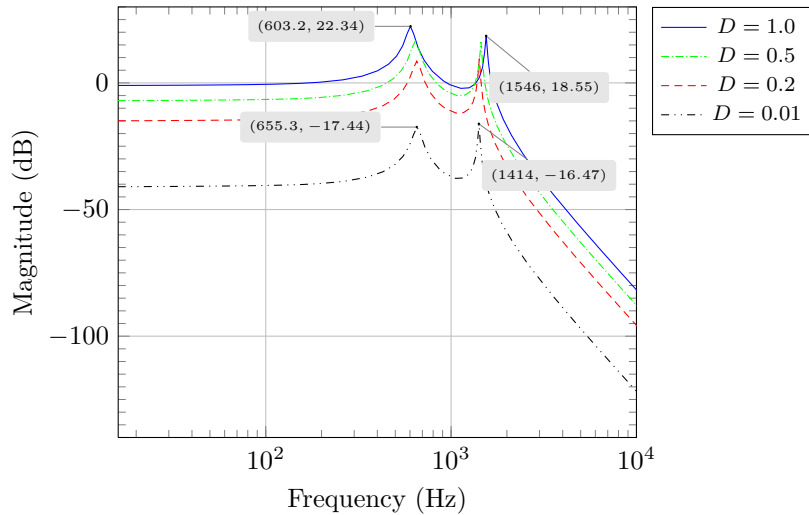


Figure 4.19: Magnitude spectrum of the transfer function, $G(s) = \frac{v_{out}}{v_i}$, showing the effect of variations on the input voltage on the output voltage. The output voltage was selected as output variable with the following selection matrices: $\mathbf{C}_{on} = [0 \ 0 \ R_{soC} \ 1 \ -R_{soC}]$, $\mathbf{C}_{off} = [0 \ 0 \ R_{soC} \ 1 \ -R_{soC}]$.

By substituting Eq. 4.90 into Eq. 4.91, and solving for $\frac{x_{out}(s)}{v_i(s)}$, the transfer function for any output variable is obtained:

$$\frac{x_{out}(s)}{v_i(s)} = \mathbf{C}_{av} (s\mathbf{I} - \mathbf{A}_{av})^{-1} \mathbf{F}_{av} \quad (4.92)$$

This transfer function can be used to obtain the steady-state frequency content of any of the state variables by simply choosing the appropriate \mathbf{C} selection matrices. A list of appropriate choices for the \mathbf{C}_{on} and \mathbf{C}_{off} matrices corresponding to actual system measurements is shown in Table 4.6.

Fig. 4.19 shows the magnitude response of $G(s) = \frac{v_{out}}{v_i}$ for various values of the duty cycle, D . The two peaks in each response represents the harmonic frequency of the leakage inductance of the transformer and the bus capacitor (on the right), and the harmonic frequency of the output filter together with the inductive load (on the left). It is seen that, for the load value in Table 4.5, any frequency on the input voltage between 1.414 kHz and 1.546 kHz will be strongly amplified.

Similarly to the output voltage, it is seen in Fig. 4.20 that any frequency on the input voltage between 1.414 kHz and 1.546 kHz will be strongly reflected on the bus voltage as well. This resonant frequency of the input's leakage inductance and the capacitances on the input bus is seen to shift around as the duty cycle varies. The larger the duty cycle becomes, the higher the resonant peak is shifted in frequency.

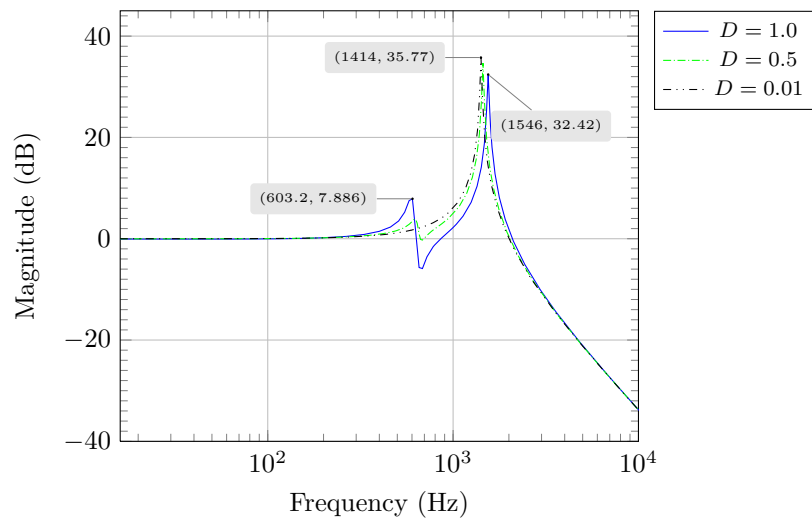


Figure 4.20: Magnitude spectrum of the transfer function, $G(s) = \frac{v_{bus}}{v_i}$, $\mathbf{C}_{on} = [R_{s_{bs}} \ 1 \ -R_{s_{bs}} \ 0 \ 0]$, showing the effect of the variations on the input voltage on the bus voltage. The bus voltage was selected as output variable with the following selection matrices: $\mathbf{C}_{off} = [R_{s_{bs}} \ 1 \ -R_{s_{bs}} \ 0 \ 0]$.

4.4 Summary

This chapter covered the modelling of the system on component level in Section 4.2. Models were developed for the following components:

- three winding transformer
- capacitor
- inductor
- dynamic source
- dynamic load.

The model of the three winding transformer was particularly productive, and the equivalent impedances will be used in in the subsequent chapters.

The system level modelling was discussed in Section 4.3, where the following models were developed:

- switching model from the combine 'on' and 'off' states
- control-to-output averaged model
- input-to-output averaged model.

The system level modelling was especially helpful in seeing vulnerabilities in the topology for oscillatory behaviour due to high gain at harmonic frequencies of the input and output filters.

CHAPTER 5

FPGA DESIGN AND SUPERVISORY CONTROL

“I cannot always control what goes on outside. But I can always control what goes on inside.”

- Wayne Dyer

5.1 Introduction to Supervisory Control

The MVEVR control architecture is based on a modular approach, where the voltage regulation is achieved by means of multiple regulator modules connected to an autotransformer type setup. The regulator modules are treated as standalone systems with their own control schemes, fault monitoring and protection mechanisms.

A supervisory control scheme is required to maintain proper operation on system level. This includes, amongst other things, system level fault monitoring (such as undervoltages on the small-signal power supply), generation of output voltage references for the regulator modules and driving of the user interface. The supervisory control was implemented on the same FPGA as the module-level control. The following sections will expand on the supervisory control design and the VHDL implementation thereof.

5.2 FPGA Design Considerations

Much debate exist between the plausibility of using digital signal processors (DSPs) *vis a vis* field programmable gate arrays (FPGAs). This thesis is based on a FPGA design, and this section will elaborate on the possibilities afforded to us because of this choice.

A FPGA is an array of configurable logic blocks that are connected to each other by a completely reprogrammable interconnection network. The FPGA memory cells control the logic blocks and their interconnections. In [42], Monmasson and Cirstea outlines three design rules for FPGA development, being:

1. *Algorithm refinement.* If a design is to be cost effective, constraints will have to be imposed on the complexity of the hardware architecture, and hence also on the complexity of algorithms used. The complexity of the control algorithms used will also have an impact on computational speed. In the MVEVR software, a decision had to be made whether to use fixed-point or floating-point arithmetic. Floating point arithmetic uses a 32-bit or 64-bit mantissa (or significant) to store significant digits, along with an exponent for scalability. With fixed-point arithmetic, any given number must be represented by a fixed number of bits for the non-decimal part and a fixed number of bits for the decimal part. This restricts the scalability of the number, but if enough bits are specified for the non-decimal part, fixed-point arithmetic can be more accurate than floating point arithmetic, with the added advantage that it is much faster to compute. With fixed-point arithmetic, word lengths can be optimised for the specific numeric value under consideration. In [40], Menard and Sentieys propose an interesting method of

automatic evaluation of the accuracy of fixed-point algorithms. A method is presented for minimizing the fixed-point word-length by taking into account the Signal to Quantization Noise Ratio (SQNR).

2. *Modularity.* The MVEVR software backbone was designed to be explicitly modular. Components were designed generically and reused wherever possible. The modularity of the VHDL code is also similar to the modularity of the MVEVR hardware. Just as, in principle, additional AC-AC regulator modules can be added to the hardware to regulate higher input voltages, additional instances of the VHDL regulator component can be easily instantiated to handle the control and protection of the respective modules.
3. *The systematic search for the best compromise between the control performances and the architectural constraints.* A so called Algorithm Architecture “Adequation” (A^3) technique is proposed. The technique utilizes data flow graphs to identify potential for parallelism in the algorithm to be implemented, as well as the scope for parallelism in the architecture at hand. This technique was not utilized in this project, due to an abundance real-estate on the FPGA used. If real-estate were a problem, algorithms could be refined with this technique.

Monmasson and Cirstea go on to outline some benefits of using FPGAs for control of electrical systems:

1. *Oversampling.* The sampling frequency is usually the same as the switching frequency, or double. If the sampling frequency is increased, more accurate regulation can be achieved. The analogue to digital converter (ADC) of the MVEVR has a sampling rate of 20MHz, while switching is done at 10kHz. This means that the system performance can be evaluated 2000 times in one switching period. Ideally, an amazing control resolution can be maintained because of this, but such large over-sampling can lead to other drawbacks. If a signal is filtered digitally at a much higher sampling rate than is necessary, multiplication errors can creep in. This is especially true if fixed point-arithmetic is used. As noted earlier, fixed point numbers are not very scalable. If the filter transfer function coefficients are very small while the signal magnitude is of much larger order, the fixed point entity storing the product will need to have a very large width in order to avoid significant truncation. With a increased sampling frequency, the magnitude of the filter coefficients decrease. This leads to a greater discrepancy in magnitude between the signal being filtered and the filter coefficients. Not only does the possibility of multiplication errors due to truncation increase, but multiplication errors accumulate quicker due to the increased frequency thereof. Because most of the sampled signals were filtered digitally, the samples were down-sampled to 100kHz. This is fifty times faster than the required control bandwidth of the system (2kHz) and is twenty five times higher than the Nyquist rate, allowing for sufficient over-sampling.
2. *Predictive Control.* Model predictive control is computationally intensive. FPGAs make full prediction of non-trivial models possible for every switching period. In [54], Tomlinson developed a full-state observer and applied full model predictive control to the MVEVR, using a fifth-order model.
3. *Current measurement improvements.* When oversampling the current of a switching converter, the average inside a sliding window can be calculated to remove the current ripple. Alternatively, in a PWM scheme, the current can be sampled at exactly the right moment (halfway into the switching period) to measure the effective average without the use of filtering mechanisms.
4. *Control of multisystems with the same controller.* In this thesis, control schemes for two independent ac-ac converters, as well as a system supervisory control scheme, are applied by use of a single FPGA control board. In [51], control of four DC motors was achieved with a single FPGA vector current controller.

5.3 Cyclone III FPGA Used

The Altera Cyclone III FPGA was used on the controller board to satisfy the logic and signal processing requirements for the system. The Cyclone III boasts many powerful features that were exploited in this design, such as:[4]

Manifold Input-Output Banks. Eight input-output (IO) banks, each with four IOs and support for multiple single-ended and differential standards. The LVDS differential standard was used on all of the IO pins.

Global Clock Networks and PLLs. The Cyclone III offers 20 global clock networks to drive global clock signals from dedicated clock pins, dual purpose clock pins, user logic, and PLLs. Up to four PLLs are also included with up to five outputs per PLL for clock management and synthesis.

Embedded Multiplier Blocks. Up to 288 embedded multiplier blocks are supported, each being capable of an individual 18 x 18-bit multiplier or two 9 x 9-bit multipliers.

DSP IP Cores. The Cyclone III comes with DSP design support with DSP IP cores such as functions for finite impulse response (FIR) filters, and fast Fourier transform (FFT) implementations.

JTAG BST Capabilities. The Cyclone III's Joint Test Action Group (JTAG) boundary-scan testing (BST) capabilities were extensively used in the design and testing process. The device supports the JTAG IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture specification. Using the boundary-scan architecture, the designer can test FPGA pin values without using physical test probes. Functional data can also be captured from the device while it is operating normally. This data is shifted serially to a PC via the JTAG interface and can be analysed and compared to expected results. This makes for a powerful testing and debugging tool.

5.4 Design and Simulation Approach

The VHDL design approach used in this thesis is shown in Fig. 5.1. The process begins with conceptualising and designing the control algorithms into SystemVision using the VHDL-AMS modelling language. The design is then implemented into synthesizable VHDL in the Altera Quartus VHDL IDE. A test bench is set up in the ModelSim VHDL simulation software where the synthesisable VHDL is simulated. If the simulation results are positive, the design is tested on the physical system. Oscilloscope measurements and Signal Tap measurements are used to evaluate the design performance. If either of the last two steps fails, the VHDL algorithm is adapted.

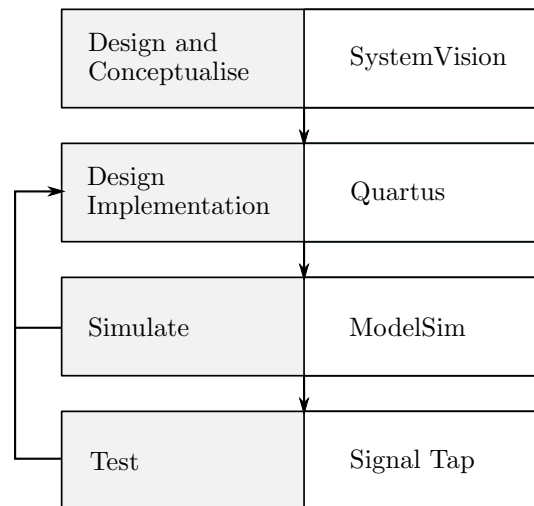


Figure 5.1: Ideal design approach, from VHDL conceptualisation to implementation, with the respective software utilised.

5.5 System Backbone Software Structure

This section will elaborate on the VHDL design of the MVEVR system backbone. This backbone is responsible for everything pertaining to system operation, from user interfaces to measurement processing to startup and shutdown sequences. The control implementation is done as a rib connected to the backbone. The top level VHDL structure, as well as the main VHDL components will be described below. Much of the VHDL structure is captured in the architecture diagrams in each section. These diagrams show the important input and output ports, as well as key operations performed. Internal processes are indicated in blocks with dashed borders. Internal components are indicated in blocks with solid borders. The data-flow, along with bus widths, between these processes and components are also indicated.

5.5.1 Top Level Structure

Fig 5.2 shows the top-level architecture of the MVEVR VHDL design. Each component in the top-level architecture interface in some way to signals external to the control board.

The ADC Interface component receives raw data signals from the ADC. These signals are processed and conveyed to the Module Operator component. The User Interface (UI) component receives external (optic push button) commands from the user. These commands are conveyed to the Module Operator, which returns various parameter values and measurement readings to the User Interface. The LCD Interface component receives data to output from the User Interface. It is also responsible for configuring the LCD hardware and correctly transmitting the data to it. The Module Operator component is instantiated once for every MVEVR regulator module. This component is responsible for everything concerning the regulator module, including startup, shutdown, control and fault detection. The Reference Generator component is responsible for analysing the magnitude of the system input voltage and generating appropriate references for the regulator modules accordingly.

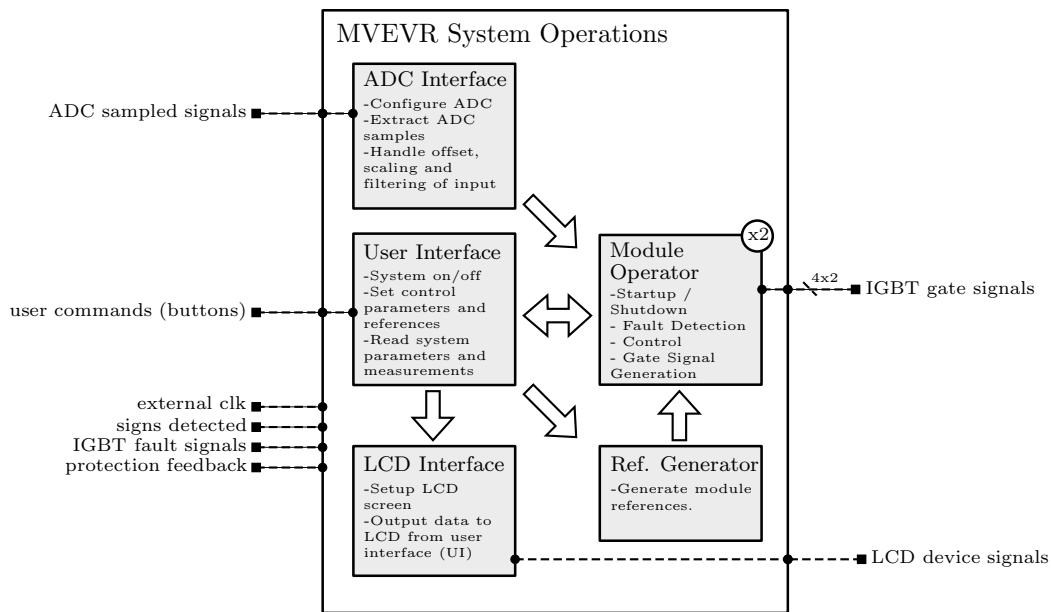


Figure 5.2: MVEVR top level architecture

The state transfer diagram (STD) in Fig. 5.3 shows the system-level startup and shutdown sequences. The supervisory control enables the peripheral processes that are necessary for safe system operation, like the ADC Interface process, the LCD Interface process, the User Interface process and the Reference Generator process. The Module Operator instances are enabled after the peripherals have started up. The Module Operator instances are kept running unless the user commands a stop via the UI, or unless a fault is detected.

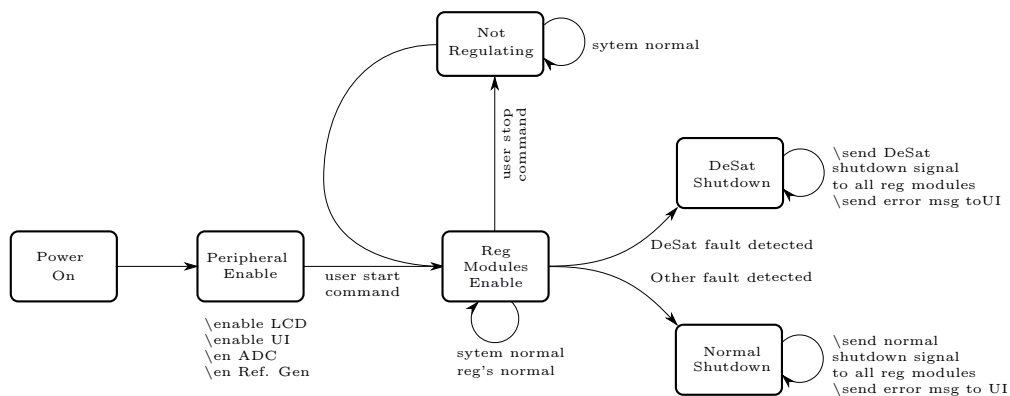


Figure 5.3: State flow of system startup and shutdown sequences

5.5.2 ADC Interface

An interface was designed in VHDL to handle the configuration and capture of data from the Texas Instruments ADS5272 8-channel, 12bit, 65MSPS, ADC. The sampling rate was reduced to the ADCs minimum rate of 20MSPS. Consequently, the external 20Mhz clock signal, which is used to run most of the FPGA processes, was used to drive the ADC as well. The ADC multiplies this clock by a factor of 12 internally in order to output entire 12bit samples serially at 20MSPS.

Three VHDL entities were designed to handle the configuration of the ADC (ADC Setup), fetching raw 120bit data vectors from the ADC (ADC Data Fetch) and processing raw data into usable physical quantities (Meas Process). The ADC Setup and ADC Data Fetch entities were designed by the author of [17], who

graciously granted us permission for use in this project. The architecture of and interaction between these entities are depicted in Fig. 5.4. A brief description of each of these three processes are given below.

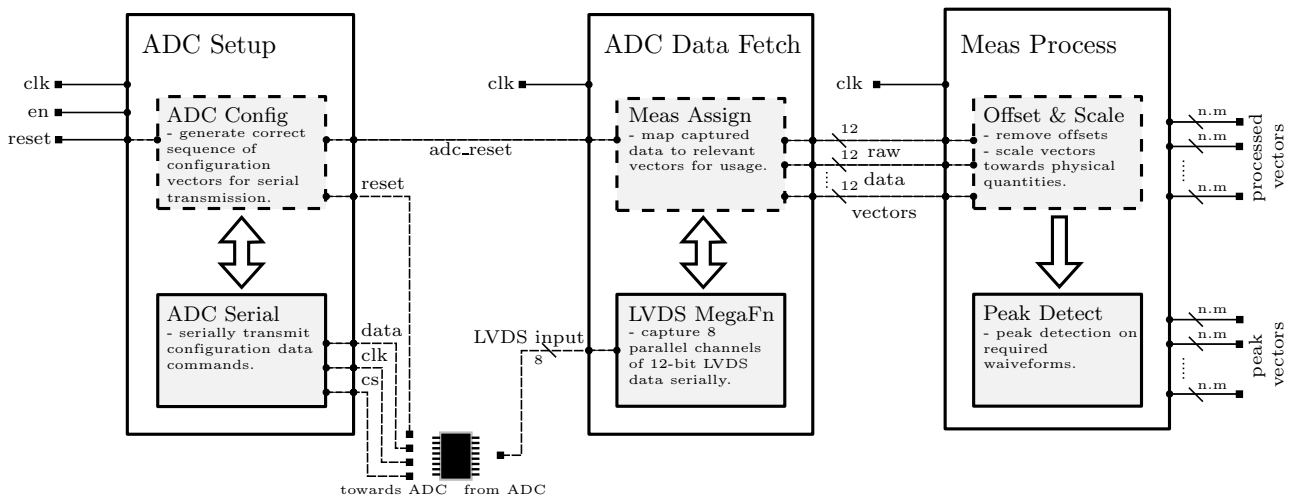


Figure 5.4: Structure of the ADC Interface component

ADC Setup This component serially configures the ADC. A state machine generates a sequence of configuration commands to:

1. power up the seven out of eight channels used for measurements
2. set up a custom test pattern if desired
3. set the mode of operation to normal operation mode or test mode
4. set most significant bit (MSB) first transmission
5. wait to lock on incoming clock from FPGA.

A component called *ADC Serial* was instantiated from inside this entity to shift the generated control commands serially towards the ADC.

ADC Data Fetch This entity uses the Altera LVDS megafunction to capture the seven channels of serially transmitted samples. The samples are then passed to Meas Process component for processing.

Meas Process The raw data received from the ADC ranges from 0 to 2^{12} (4096). Therefore, all AC measurements have an offset of 1024. This offset is subtracted, and the difference is scaled to produce a quantity that represents the desired physical unit. Peak detection is done on required waveforms by use of a peak detector component created specifically for this purpose.

5.5.3 User Interface

The User Interface entity is responsible for relaying commands from the user to the targeted system process and also relaying useful data from the system processes to the user. In order to do this, the UI component partners with the LCD Interface component to enable text-based communication with the user. The input from the mechanical push-buttons are debounced to ensure sensible user input. The relation between the different components used in this entity is shown in Fig. 5.5.

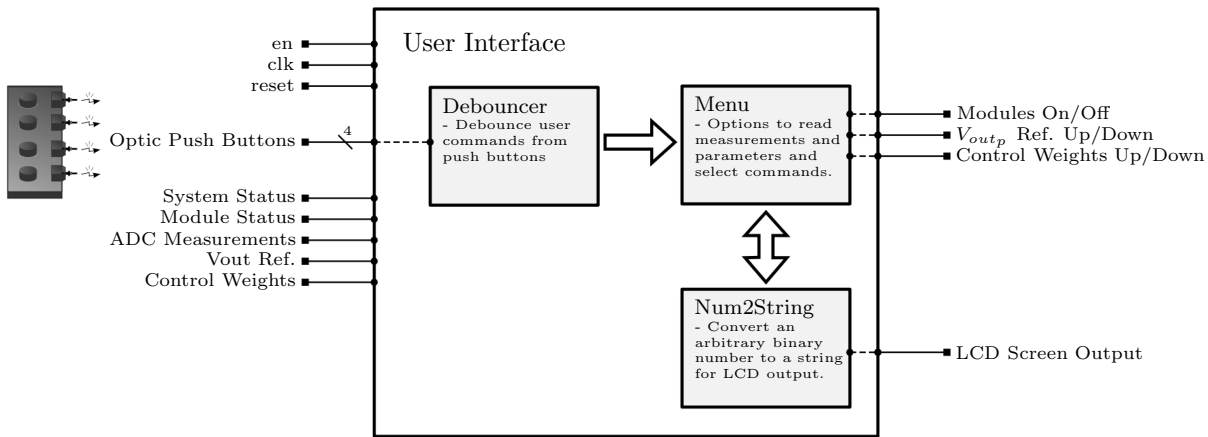


Figure 5.5: Structure of User Interface Component

The user can choose any of a range of commands from the menu such as:

- turn any given regulator on/off
- increase/decrease the output voltage reference voltage by a pre-defined step size
- manipulate weights and variables used in the control algorithms.

The user can read system measurements and variables such as:

- System Operational Status
- Module Operational Status
- ADC Measurements
- Control Reference Amplitudes
- Control Weight Values.

The menu is highly configurable and extendable and can be made to interface with virtually any of the system processes.

A special component was required to convert digital values (such as ADC measurements) to string format for display on the LCD screen. The Num2String component was created for this purpose. It is able to convert any value in between -99999 and 99999 to a six-character string. The component makes use of multiple case statements to do a form of long division.

5.5.4 LCD Interface

An interface was designed to handle the transmission of configuration data and display data to the PowerTip PC1602D LCD screen module. The interface is comprised of a process to generate control commands and data vectors, as well as a component to transmit these vectors to the LCD screen. The internal interaction in this interface is depicted in Fig. 5.6.

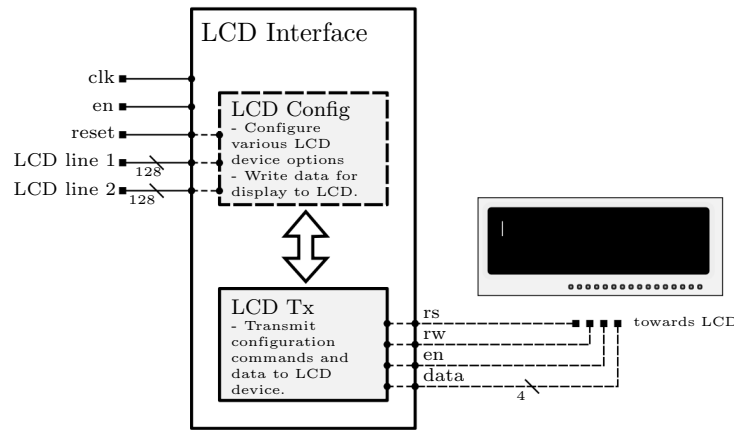


Figure 5.6: Structure of LCD Interface Component

LCD Config Firstly, the process called LCD Config generates a sequence of configuration commands and data vectors to ensure that the LCD screen is set up correctly:

1. put LCD in 4 bit data mode (this makes use of only 4 out of 8 data pins and clocks 8-bit words in 4 bits at a time)
2. use both lines on the screen
3. turn display on
4. put display in “Entry Mode”
5. clear the display
6. return the cursor to home position.

Secondly, this process watches for data from the User Interface and formats the strings received in the appropriate form of a 256-bit standard logic vector. It then passes this vector to the LCD Tx component for transmission to the LCD screen.

LCD Tx This component is comprised of a fairly intricate state machine used to transmit the received configuration and data vectors to the LCD screen module. Data is sent at a clock frequency of 100 kHz. This component was written by the author of [17], also the designer of the FPGA control board, who kindly supplied this driver for use along with the board.

5.5.5 Module Operation Interface

Out of all the VHDL components, the Module Operation Interface (MOI) is the most complex. This component is responsible for supervising and controlling the most crucial part of the system: the voltage regulators. The interaction between the various sub-components within the MOI component is depicted in Fig. 5.7.

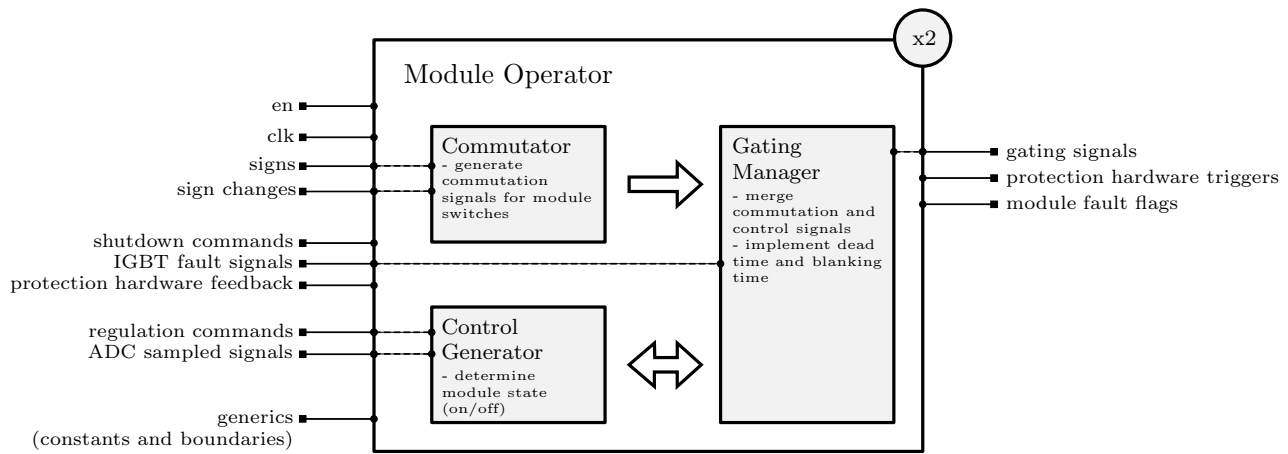


Figure 5.7: Structure of Module Operation Software

Everything regarding the regulators are managed from this component, such as:

1. startup procedures are executed from this component
2. module diagnostics and fault monitoring are performed
3. shutdown procedures are executed in the event of power-down or module faults
4. commutation signals are generated by the Commutator sub-component
5. control signals are generated by the Control Generator sub-component
6. commutation and control signals are consolidated into gating signals by the Gating Manager sub-component
7. DeSat sensing¹ is done by the Gating Manager sub-component to detect over-current faults on the IGBTs
8. managing and monitoring hardware protection mechanisms such as the soft start mechanisms, dump crowbar bypasses and filter cutouts.

Various hardware protection mechanisms that are to be managed by the MOI are shown in Fig. 5.8. For a more detailed description of the hardware protection, refer to [53].

¹De-Saturation sensing is performed by the IGBT gate-drivers on the IGBT V_{ce} voltages to sense whether the transistor moves out of its saturation region due to unacceptably large currents.

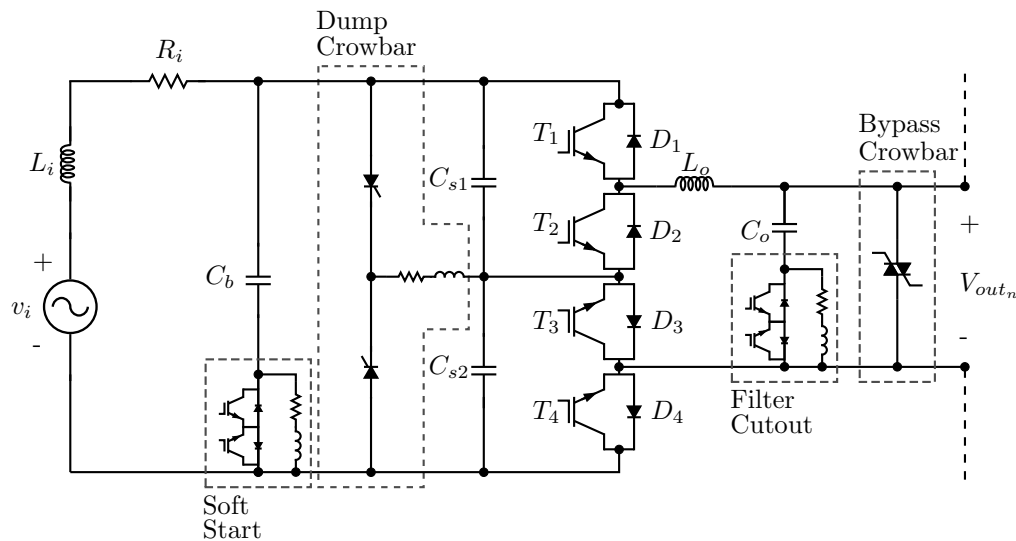


Figure 5.8: Various system module components to be managed at startup, shutdown and fault conditions including the soft start mechanism, dump crowbar, filter cutout, and bypass crowbar.

Startup Sequence

Much effort was invested into the design of the module's startup sequence. System characteristics such as available conduction paths and initial charges on module capacitors had to be taken into account to avoid breaking the path of the load current or shorting out snubber capacitors while carrying large charges. The following list describes the start-up sequence. Refer also to Fig. 5.9 for comparison with the input voltage waveform, and Fig. 4.14 for references of system components.

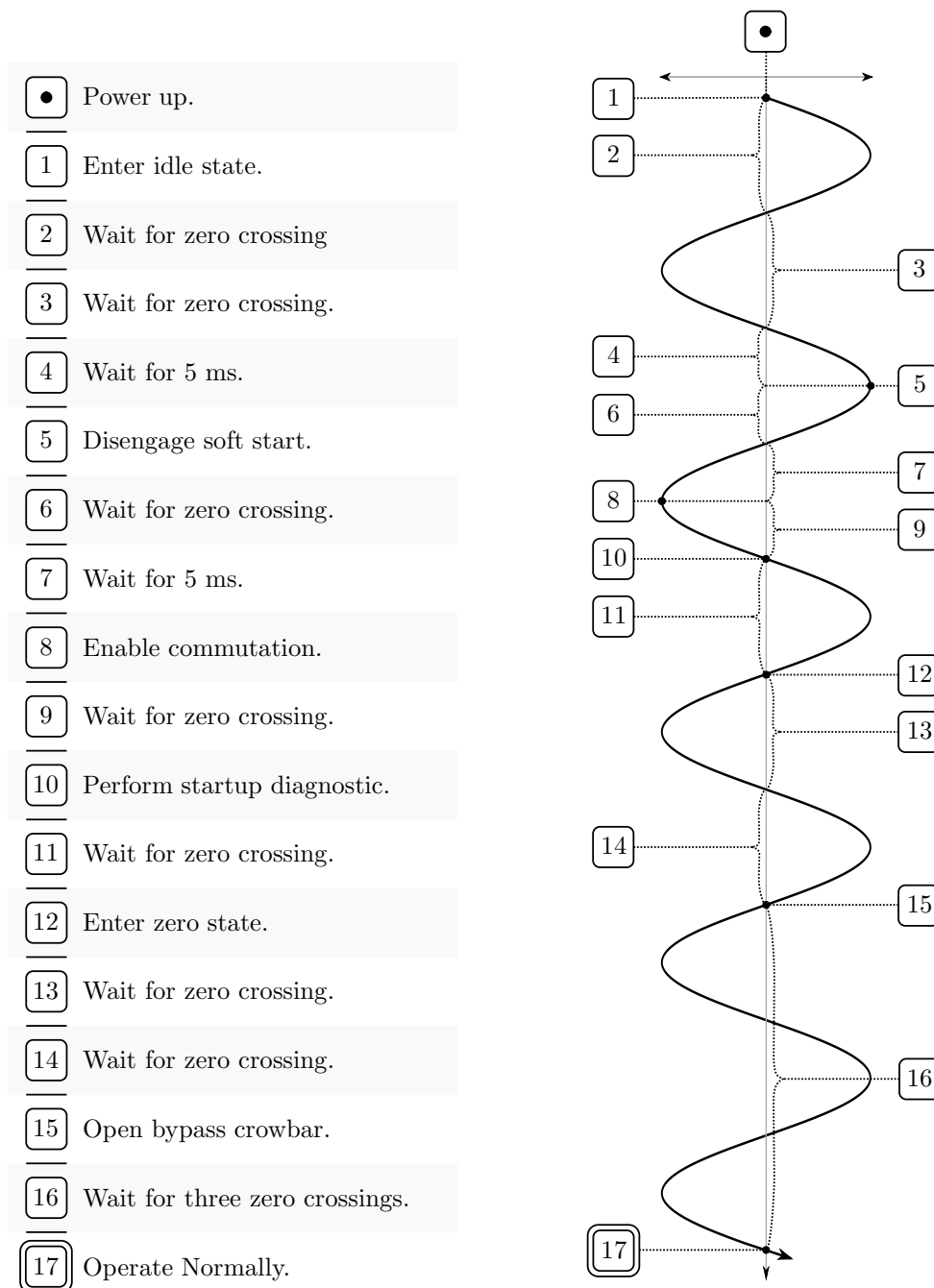


Figure 5.9: MVEVR startup sequence in order of execution, relative to the zero crossings and peaks of the regulator module input voltage waveform.

1. *Power on* (controller)
2. *Enter into Idle mode.* In this mode, all of the IGBTs are kept off. The bypass crowbar is enabled (conducting the load current).
3. *Wait for two zero crossings of the input voltage.* This is an easy way to implement a delay in the process. This is done to allow any startup transients in the bus capacitor to settle before commencing with the startup procedure. A soft start resistor is placed in series with the bus capacitor to limit inrush currents.
4. *Wait for 5 ms.* Before the soft-start hardware is disengaged, a 5 ms wait is introduced in order to disengage on a peak of the input voltage. The current though the bus capacitor lags the voltage across the bus

capacitor by 90° , or equivalently 5 ms for a 50Hz signal. Waiting for 5 ms therefore ensures that the soft-start hardware is disengaged at zero current.

5. *Disengage the soft start hardware.* The resistor is thermally incapable of carrying the capacitor current for very long. The resistive element in series with the bus capacitor is shorted out by an IGBT which thereby assumes the capacitor current.
6. *Wait until the next zero crossing.* This is working towards another peak voltage.
7. *Wait for 5 ms.* The input voltage should then again be at a peak.
8. *Enable commutation.* The commutation process is enabled at a peak of the input voltage. In this process, either the lower two IGBTs, or the upper two IGBTs of the module (refer to Fig. 4.14) are turned on for the entire half-cycle of the input voltage. This translates into a short-circuit across the corresponding snubber capacitor. During the peak of the input voltage, the voltage across the snubber capacitor being shorted is minimal $(\pm 30V)^2$. This minimizes the rate of voltage change over the capacitor when it is shorted out, and prevents unacceptably large short-circuit currents flowing through it.
9. *Wait until the next zero crossing.*
10. *Run startup diagnostic to see if the system is passive:*
 - (a) check that Bypass Crowbar is closed (conducting)
 - (b) check that Dump Crowbar is open (not conducting)
 - (c) check that the regulator input voltage frequency is 50Hz.
11. *Wait until the next zero crossing into the positive half-cycle of the input voltage.* This is in preparation for a current conduction path to be created through the regulator.
12. *Enter Zero State.* In this state, PWM switching is done with a zero duty cycle. Because the input voltage waveform is in its positive half-cycle, this translates to IGBTs 2, 3 and 4 being constantly on and IGBT1 being constantly off (refer to Fig. 4.14). In effect the regulator can now simply conduct the load current through IGBT 2 and 3 without contributing any current to the system.
13. *Wait until the next zero crossing into the negative half-cycle of the input voltage.*
14. *Wait until the next zero crossing into the positive half-cycle of the input voltage.* These two successive waits allow the system to take a couple of deep breaths before assuming the load current all by itself.
15. *Open the bypass crowbar.* The thyristors used in the bypass will only turn off once the load current crosses through zero. Sufficient time is allowed for this by waiting till the next zero crossing of the input voltage.
16. *Wait for three subsequent zero crossings.* A wait condition is implemented to allow the bypass to turn off and for any transients to disappear as the regulator to assumes the load current.

²The 30V offset is introduced by the DeSat sensing mechanism of the IGBT driver boards which are in connected parallel with the snubber capacitor.

17. *Apply normal control.* Apply the control output to the IGBTs once the system input voltage crosses zero. This is done to avoid a sudden voltage step, and hence aggressive transients, on the output filter. The regulator starts contributing current to the system. During this time, the regulator is monitored continuously:

- (a) Check that the conducting IGBTs remain in saturation (DeSat testing). This is performed by the gating manager component. The result is relayed to the system level diagnostics. If this is triggered, the active modules are shut down.
- (b) Check that Bypass Crowbar is open (not conducting).
- (c) Check that Dump Crowbar is open (not conducting).
- (d) Check that ADC measurements are within range.
- (e) Check that the regulator input voltage frequency is 50Hz.

An entity is created to monitor the system as a whole. This entity monitors the system input and output voltages, as well as the system power supply voltage level. If a fault is detected, commands are sent to each module to shut down. The design of the under-voltage detection circuitry is detailed in Section A.1.3.

Each regulator module is governed by its own instantiation of the module operator VHDL entity. If a fault is detected, the relevant module is shut down. The module also alerts the entity monitoring the system as a whole. Then all the other modules can be shut down as well. A “limp mode” can be activated, where if one module fails, the rest can still be kept running to improve the output as much as possible.

Shutdown Sequences and Fault Detection

Each MVEVR model has two shutdown sequences, namely the normal shutdown routine and the DeSat shutdown routine. These differ in the order in which system components are shut down.

Normal Shutdown The normal shutdown routine is used for safe shutdowns in non-critical fault situations. Firstly, the thyristor bypass crowbar is activated while the system is kept running (switching) for the maximum turn-on time specification of the thyristors. When it can be safely assumed that the bypass has assumed the load current, the switching is reduced to commutation only. The module is continuously made to commutate to prevent the snubber capacitors over the IGBTs to charge up. The following situations will trigger a normal shutdown:

- incorrect input voltage frequency
- small-signal supply under voltage
- out-of-bounds reading on the ADC measurements
- bypass crowbar automatic closure (over voltage or over current on the output)
- dump crowbar automatic closure (over voltage on the input)
- user generated shutdown command.

DeSat Shutdown The DeSat shutdown routine is used for emergency shutdowns when critical faults occur. This routine is carried out in the event of an over-current fault on any of the IGBT transistors. These units are rated for up to 300A continuous current and 800A surge currents. Such large surge currents cause the conducting transistors' V_{CE} voltages to suddenly rise, forcing them out of their saturation regions. In this case, the feedback from the DeSat sensing circuitry will cause the fault monitoring processes to notice an over-current fault on the relevant IGBT. This is a critical fault, as such large currents should never appear in the system. The nominal current through any one of the IGBTs should not exceed the rated load current of 100 A plus a ripple of 30 A, that is $130 A_{rms}$. During large reference steps, however, transient currents of up to 250 A can be expected. If a DeSat fault is generated in isolation from a normal ADC fault, it is indicative of a switching fault where, for example, the dead time failed and all four IGBTs are switched on at the same time, shorting the secondary winding of the transformer. This will produce large currents through the switching elements. When a DeSat error is detected, the bypass crowbar is activated and the switching scheme is reduced to only commutation immediately. The module is continuously made to commute to prevent the snubber capacitors over the IGBTs to charge up.

5.5.6 Commutation Generator

The Commutation Generator component is a crucial component in the operation of the MVEVR regulator modules. The regulator modules are designed to operate with an AC input voltage, implying that the polarity will periodically change. The switching elements are therefore arranged to form two synchronous buck converters.

During the positive half-cycle of the input voltage, the bottom two IGBTs are continually turned on, thus shorting out the bottom buck converter. During this time, the top two IGBTs fire in a complimentary fashion, which effectively puts the top buck converter to use while the bottom one is ideally just a dead short.

During the negative half-cycle, the top two IGBTs are switched continually on, which shorts out the top buck converter. During this time the bottom two IGBTs fire in a complimentary fashion, which effectively puts the bottom buck converter to use while the bottom one is ideally just a dead short.

So in this way, provision is made for AC input and output voltages. The practice of keeping a pair of IGBTs on for any half-cycle of the input voltage is referred to in this thesis as “commutation”. The signals generated for this purpose is referred to as commutation signals.

Ideal commutation signals are generated by the commutation component, which is then passed to the gating manager. The gating manager applies dead time to commutation signals when the polarity of the input voltage changes. A blanking time of $6 \mu s$ is applied, after which DeSat sensing is done on the active IGBTs to monitor for over-current faults. The gating manager also performs blanking and fault monitoring. Fig. 5.10 depicts the inner-working of the Commutation Generator component.

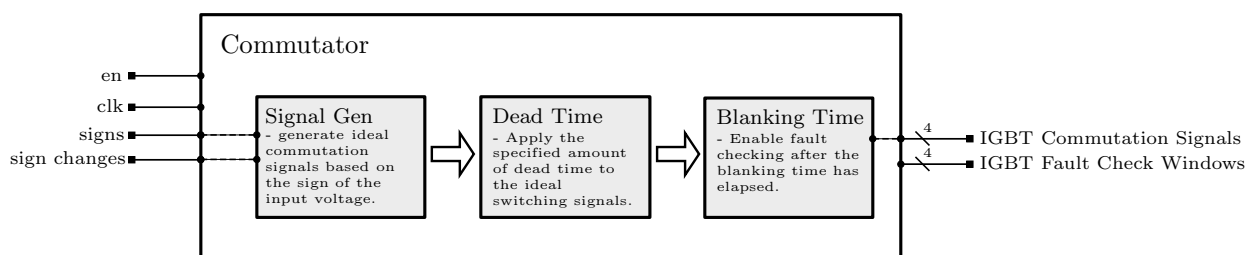


Figure 5.10: Structure of Commutation Signal Generator Component Architecture

5.5.7 Control Generator : Open Loop

Fig. 5.11 depicts the basic interaction between the components used in the open-loop control generator. The Control Generator is responsible for providing a simple binary control command to the Gating Manager. A command of '1' means that the active buck converter must connect the input voltage towards the output. A command of '0' means that the active buck converter must disconnect the input voltage from the output.

The duty cycle value is passed from the LUT to the PWM process. This process compares the duty cycle value with a generated triangular wave. When the triangular wave is greater than the duty cycle value, a control command of '1' is generated. Otherwise, '0' is generated. No dead-time is incorporated at this point. This is only done by the Gating Manager. The reason for this is to make the control component more interchangeable. Different control modules from different designers can easily be integrated into the system, because the output requirement is simply a '0' or '1'. Thus, the complexity of dead time and blanking time is shifted out of the control component to the gating manager.

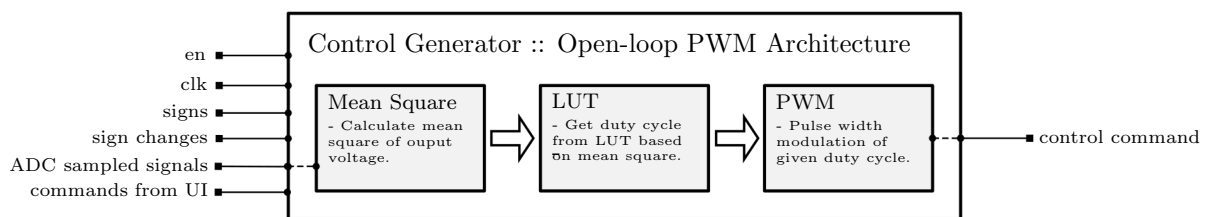


Figure 5.11: Structure of Open-loop Control Generator Component Architecture

5.5.8 Control Generator : Closed Loop

The closed loop architecture of the control generator is an implementation of fixed-frequency sliding mode control (SMC). There are three main groups of processes and sub-components (as depicted in Fig. 5.12) involved in this architecture, namely

1. processes for the generation of AC control references
2. the sliding function process
3. a process implementing a modified PWM switching law.

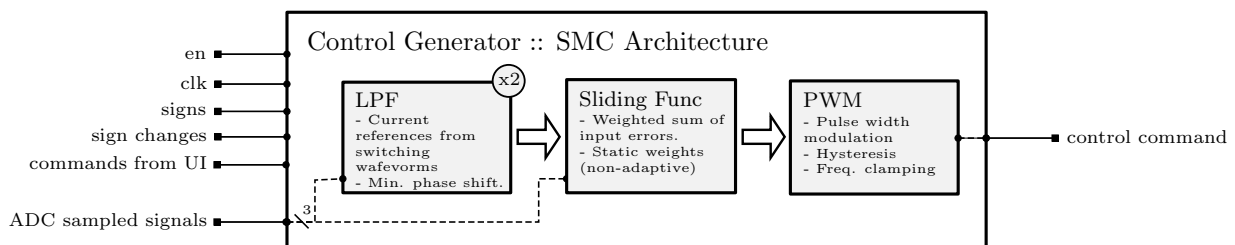


Figure 5.12: Structure of Closed-loop Control Generator Component Architecture

Three AC references are generated, namely:

1. an output voltage reference
2. an inductor current reference

3. an input current reference.

The output voltage reference is obtained by using a look-up table (LUT) to generate a 50Hz sinusoid. This signal is then scaled towards the given output voltage reference (specified by the user). If the input voltage happens to be deviating from 50Hz, there will be a slight misalignment of the reference with regard to the actual signal. This possible misalignment is kept to a minimum by constantly synchronising each zero-crossing of the reference with the zero-crossings of the input voltage.

The inductor current reference is obtained by passing the inductor current ADC measurement through a first-order low-pass filter with cut off frequency of 350Hz.

The input current reference was obtained by filtering the input current ADC measurement in the same way as the inductor current ADC measurement.

The sliding function process implements a weighted sum of errors between ADC signals and references. All of these signals are represented in fixed-point arithmetic. This results in fast computation. One of the parts to the addition is the integral of the output voltage error. A digital implementation of the trapezoidal rule (integrator) was designed for this purpose.

The PWM process is comparable to that of the open-loop PWM process in that it also makes use of a triangular modulation wave. The signal being modulated is not a duty-cycle reference, however, but the output of the sliding function. The amplitude of the PWM carrier is made to adapt to the amplitude of the sliding function to maintain control resolution. This concept is explained further in Section 6.3.10.

5.5.9 Gating Manager

The inner working of the Gating Manager is summarized in Fig. 5.13. The gating manager is responsible for consolidating the commutation and control signals into meaningful IGBT gate signals. The gate output of any given IGBT is the logical OR of its commutation and control signal. That is, while in commutation, it will be continually on, and while not, it will reflect the control action.

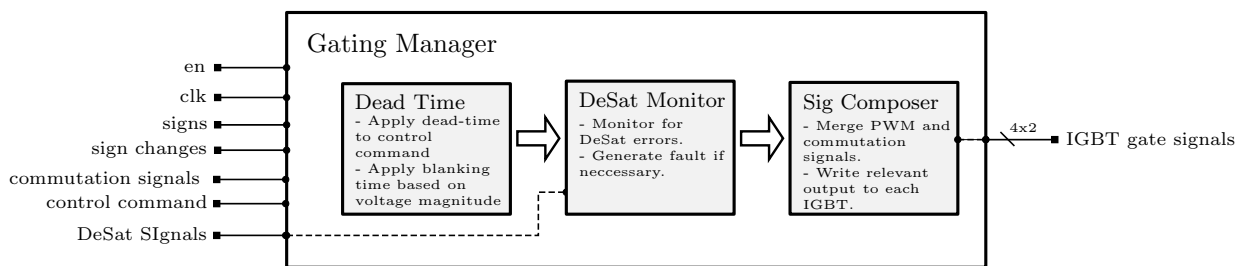


Figure 5.13: Structure of Gating Manager Component

Dead time is applied to the control signal. This is done in the Gating Manager rather than in the Control Generator, because - as long as the topology remains the same - the Gating Manager's design will not change either.³ Dead time is a crucial function, and by implementing it in a largely static file, the chances of it being broken by change is reduced. Blanking time is also applied. After the commutation and control signals are consolidated, corresponding gating signals are synthesized and transmitted towards the optic fibres for transmission to the driver boards.

DeSat fault monitoring is done on all of the IGBTs concurrently. The DeSat hardware circuit on the IGBT drivers transmit the saturation status of the transistors to the controller. The Gating Manager compares the

³The Control Generator, however, might very well be updated as new and improved control techniques are developed.

received saturation status to what is expected, and sends a fault signal to the Module Operator if the actual and expected values do not correspond. The Module Operator can then command all modules to commence with their DeSat shutdown procedures.

5.6 Synthesisable VHDL Control Components

Many useful, generally reusable, VHDL components were designed for system operation and control. Some of these include

- first order low pass filter (LPF)
- second order Chebyshev, Butterworth, and Bessel filters
- saturation component
- sawtooth and triangular modulation signal generators
- integrator component
- differentiator component.

These components were written generically with the aim of re-usability in other applications. VHDL generics were employed to make input and output signal lengths adjustable, and to allow the designer to specify critical design constants. The design of some of these components will be described in the subsequent sections.

5.6.1 Digital First Order Low Pass Filter

Digital first order low pass filters were required for the purposes of generating control reference signals, for filtering the ADC measurement signals, and various other signal processing requirements. First order filters for the following sample frequencies and cutoff frequencies (Table 5.1) were developed:

Table 5.1: Different 1st order filters designed.

Sampling Frequency	Cut off Frequency
100kHz	50 Hz
100kHz	100 Hz
100kHz	350 Hz
100kHz	500 Hz
100kHz	1.3 kHz
100kHz	2 kHz
100kHz	10 kHz
100kHz	15 kHz
20 MHz	1 kHz
20 MHz	1.2 kHz
20 MHz	50 kHz

As the design for all the first order filters follow the same approach, only the design for the filter with specification in Table 5.2 will be detailed.

Table 5.2: Filter specification for input current reference generation.

Order	Sampling Frequency	Cut off Frequency
1 st	100 kHz	500 Hz

Design The continuous-time expression used for the LPF was:

$$G(s) = K \cdot \frac{2\pi f_o}{s + 2\pi f_o} \quad (5.1)$$

with f_o being the cut off frequency in Hz. The DC gain, K , was chosen to be unity. The s-domain expression was converted to the digital domain by using the bilinear transform:

$$H(z) = G(s) \Big|_{s=\frac{2}{T} \frac{z-1}{z+1}} = G\left(\frac{2}{T} \frac{z-1}{z+1}\right), T = 50ns \quad (5.2)$$

where T is the sampling period in seconds. The resulting z-domain expression is:

$$H(z) = \frac{0.01547 + 0.01547z^{-1}}{1 - 0.9691z^{-1}}. \quad (5.3)$$

The linear constant coefficient difference equation (LCCDE) was found by firstly substituting $\frac{Y(z)}{X(z)}$ for $H(z)$ and cross-multiplying:

$$Y(z) - 0.9691 \cdot z^{-1} \cdot Y(z) = 0.01547 \cdot X(z) + 0.01547 \cdot z^{-1} \cdot X(z) \quad (5.4)$$

and secondly doing an inverse z-transform towards the discrete time domain. After rearranging:

$$y(k) = 0.01547 \cdot x(k) + 0.01547 \cdot x(k-1) + 0.9691 \cdot y(k-1). \quad (5.5)$$

The magnitude and phase response was plotted in MATLAB using the *freqz* command and is displayed in Fig. 5.14 and 5.15, respectively. The markers on Fig. 5.14 show that the gain at the cut off frequency (500 Hz) is 0.7042. This is confirmed to be correct by evaluating magnitude of the z-domain transfer function at $z = e^{sT} = e^{j\omega T}$:

$$|H(e^{j\omega T})| = \left| \frac{0.01547 + 0.01547e^{-j \cdot 2\pi \cdot 500 \cdot 10e-6}}{1 - 0.9691e^{-j \cdot 2\pi \cdot 500 \cdot 10e-6}} \right| = 0.7044. \quad (5.6)$$

At 500 Hz, the s-domain transfer function for magnitude evaluates as follows:

$$|G(j\omega)| = \left| 1.0 \cdot \frac{2\pi \cdot 500}{j \cdot 2\pi \cdot 500 + 2\pi \cdot 500} \right| = \frac{1}{\sqrt{2}} = 0.7071. \quad (5.7)$$

The z-domain expression is seen to be a good approximation of the original continuous domain expression at 1MHz.

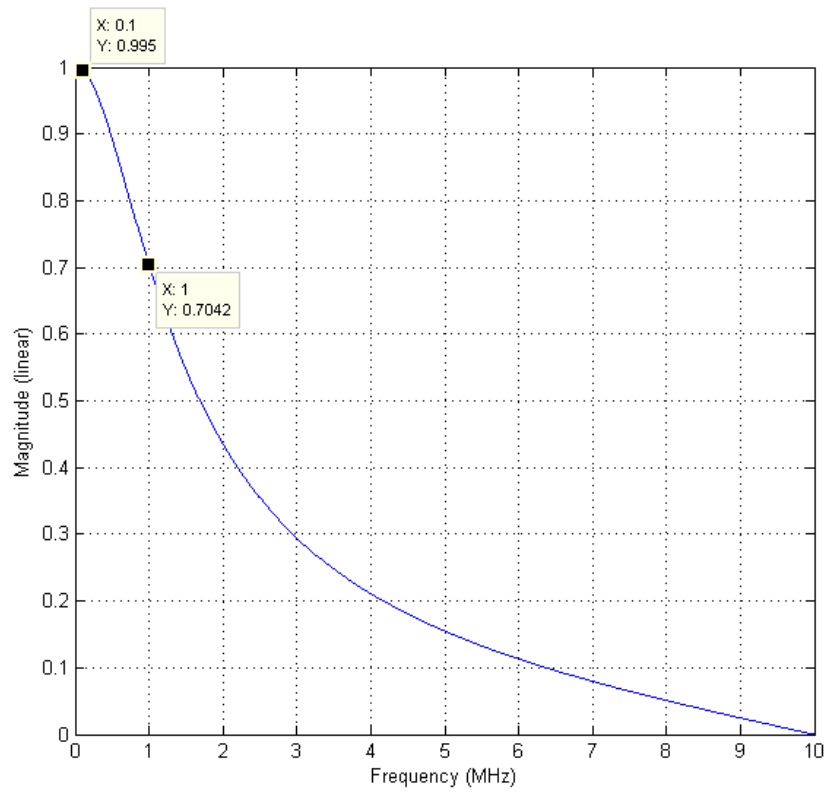


Figure 5.14: Frequency response of the anti-aliasing LPF in magnitude.

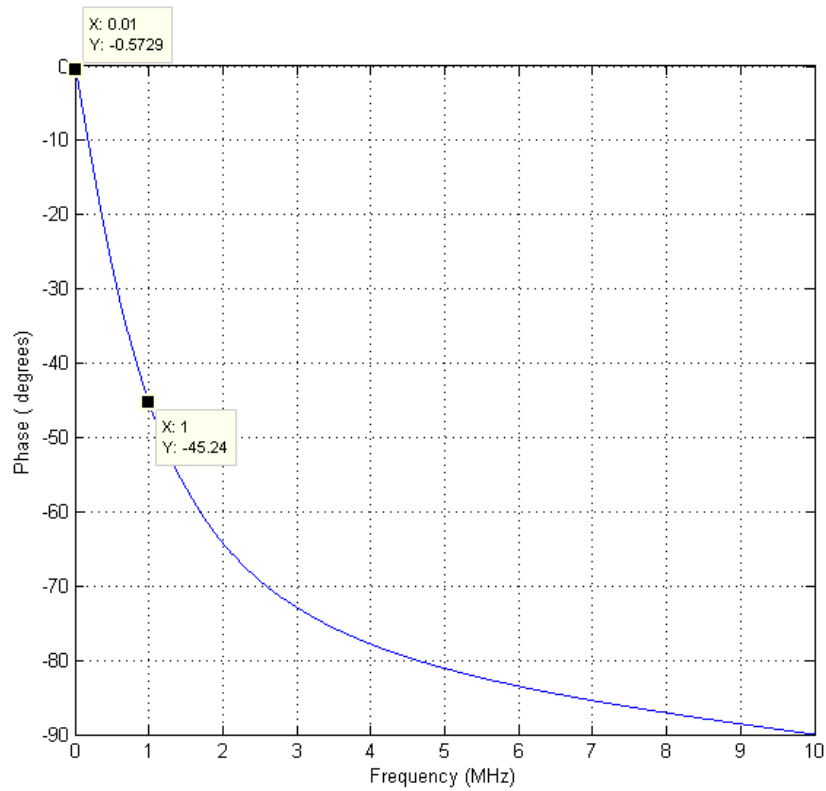


Figure 5.15: Frequency response of the anti-aliasing LPF in phase.

VHDL Implementation The VHDL implementation is shown in listing below. This design was implemented as one of many LPF architectures within the *lpf* entity. This allows for using a single entity (and hence the same input ports, output ports, and generics) for all the LPFs required in the design. The relevant architecture is then specified during instantiation.

Listing 5.1: VHDL implementation of 1st order LPF.

```

1 LPF1n : process (en, reset, clk)
2   -- -- LPF Filter Coefficients
3   constant b1 : sfixed (0 downto -20) := to_sfixed(0.015465039003347,0,-20);
4   constant b2 : sfixed (0 downto -20) := to_sfixed(0.015465039003347,0,-20);
5   --note a2 is pre-multiplied by -1 in the algorithm
6   constant a2 : sfixed (0 downto -20) := to_sfixed(0.969069921993306,0,-20);
7
8   --previous value of input signal
9   variable x_kz : sfixed (sig_in'high downto sig_in'low) := (others => '0');
10  --current value of ouptu signal
11  variable y_k : sfixed (32 downto -40) := (others => '0');
12
13 begin
14  if en = '0' and reset = '0' then
15    y_k := (others => '0');
16    sig_out <= (others => '0');
17    x_kz := (others => '0');
18  elsif rising_edge(clk) then
19    sig_out <= resize(b1*sig_in + b2*x_kz + a2*y_k,ref_bit_high,ref_bit_low);
20    --a latch will be inferred to rememeber previous value of y_k
21    y_k := resize(b1*sig_in + b2*x_kz + a2*y_k,y_k);
22    x_kz := sig_in;
23  end if;
24 end process LPF1n;

```

VHDL Simulation A test bench was created for the filter and was simulated in ModelSim. A sinusoidal test voltage with amplitude of 100 units and frequency of 500 Hz was injected it the filter. The result is show in Fig. 5.16. The output signal, *sig_out*, is seen to have a phase shift relative to the input signal, *sig_in*. This is expected. The peak amplitude of the output signal (under the cursor) is seen to be of magnitude 71 units. This translates into a filter gain of 0.71 gain at the cut off frequency. This is consistent with theoretical predictions.

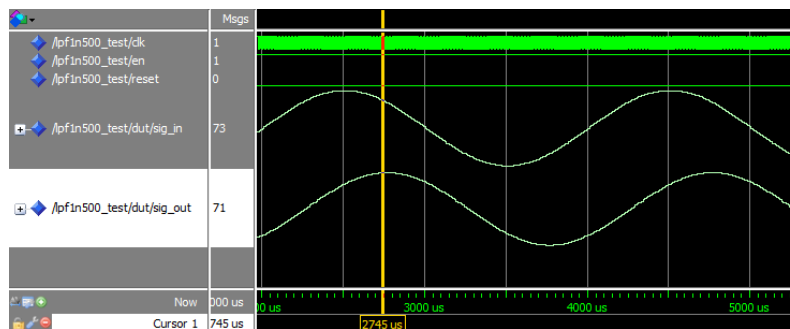


Figure 5.16: Simulation result after a sine wave was injected into the 50Hz LPF.

5.6.2 Digital Second order Chebyshev Low Pass Filter

Similar to the first order filters, a range of second order filters were developed as well. The range of designs in the final library is detailed in Table 5.3.

Table 5.3: Different 2nd order filters designed.

Type	Sampling Frequency	Cut off Frequency
Bessel	100 kHz	100 Hz
Butterworth	100 kHz	100 Hz
Chebyshev	100 kHz	350 Hz
Chebyshev	100 kHz	10 kHz
Chebyshev	20 MHz	500 Hz
Chebyshev	20 MHz	1 kHz

The second order filters were not used in the final MVEVR implementation, therefore only the design of one of the filters will be covered for purposes of illustration.

Design

A second order LPF was required to filter the derivative of the output voltage for frequency limiting purposes. The specifications are given in Table 5.4.

Table 5.4: Filter specification for input current reference generation.

Order	Sampling Frequency	Cut off Frequency
2 nd	100 kHz	10 kHz

The *cheby1* function in MATLAB was used to design a Chebyshev (type 1) second order digital filter with 0.5 dB ripple in the passband and sampling frequency and cut off frequency as already stated. The coefficients for the z-domain transfer function was found. The *b* coefficients are used in the numerator for ascending orders of *z*. The *a* coefficients are used in the denominator for ascending orders of *z*. The following MATLAB code was used to find the filter coefficients:

```

1 [b,a] = cheby1(2, 0.5, 10e3/(0.5*100e3))
2 b = 0.093092568569303 0.186185137138607 0.093092568569303
3 a = 1.000000000000000 -1.034853562936476 0.429288163109903

```

The z-domain transfer function can be expressed as

$$\frac{Y(z)}{X(z)} = \frac{0.09309 + 0.1862z + 0.09309z^2}{1.000 - 1.035z + 0.4293z^2}. \quad (5.8)$$

VHDL Implementation

Cross multiplication and inverse transform of 5.8 yields the LCCDE, which is expressed as

$$y(k) = 1.035y(k-1) - 0.4293y(k-2) + 0.09309x(k) + 0.1862x(k-1) + 0.09309x(k-2). \quad (5.9)$$

This infinite impulse response (IIR) filter was implemented in VHDL in direct form II[48], as indicated in Fig. 5.17.

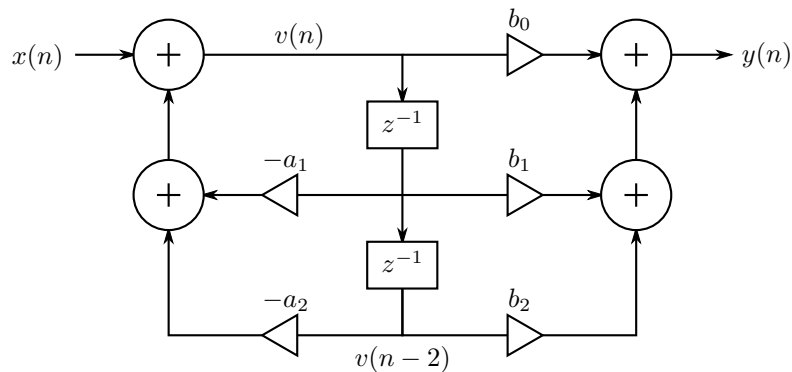


Figure 5.17: Direct form II, used for VHDL 2nd order LPF implementation.

The VHDL implementation of this design is shown below. Note that the same code can be used for a different direct form II design by just updating the values of the coefficient constants at the top.

Listing 5.2: VHDL implementation of 2st order LPF.

```

1  directFormII : process (en, reset, clk)
2    -- optimized word-lengths for coefficients
3    constant a2 : sfixed(2 downto -15) := to_sfixed(1.034853562936476, 2, -15);
4    constant a3 : sfixed(0 downto -18) := to_sfixed(0.429288163109903, 0, -18);
5    constant b1 : sfixed(0 downto -30) := to_sfixed(0.093092568569303, 0, -30);
6    constant b2 : sfixed(0 downto -30) := to_sfixed(0.186185137138607, 0, -30);
7    constant b3 : sfixed(0 downto -30) := to_sfixed(0.093092568569303, 0, -30);
8
9    variable x_k, y_k, v, v_z, v_z2 : sfixed (32 downto -40) := (others => '0');
10
11  begin
12    if en = '0' and reset = '0' then
13      y_k      := (others => '0');
14      sig_out  <= sig_in;
15      v       := (others => '0');
16      v_z     := (others => '0');
17      v_z2    := (others => '0');
18      x_k     := (others => '0');
19    elsif rising_edge(clk) then
20      x_k     := resize(sig_in, x_k);
21      v       := resize(x_k + a2*v_z - a3*v_z2, v);
22      y_k     := resize(b1*v + b2*v_z + b3*v_z2, y_k'high, y_k'low);
23      sig_out <= resize(y_k, ref_bit_high, ref_bit_low);
24      v_z2    := resize(v_z, v_z2);
25      v_z     := resize(v, v_z);
26    end if;
27  end process directFormII;

```

VHDL Simulation

The VHDL code was simulated in ModelSim. A test signal of frequency 5 kHz and amplitude 100 V was injected into the component, which is shown, along with the output signal, in Fig. 5.18. The peak value of the output signal is seen to be (under the cursor) 97 V. This corresponds to the theoretical prediction which follows:

$$|H(e^{j\omega T})| = \left| \frac{0.09309 + 0.1862e^{j \cdot 2\pi \cdot 5e3 \cdot 10e-6} + 0.09309e^{2 \cdot j \cdot 2\pi \cdot 5e3 \cdot 10e-6}}{1.000 - 1.035e^{j \cdot 2\pi \cdot 5e3 \cdot 10e-6} + 0.4293e^{2 \cdot j \cdot 2\pi \cdot 5e3 \cdot 10e-6}} \right| = 0.984. \quad (5.10)$$

The low signal resolution is a result of the slow clock frequency relative to frequency of the test wave. There are only twenty clock periods per wave period.

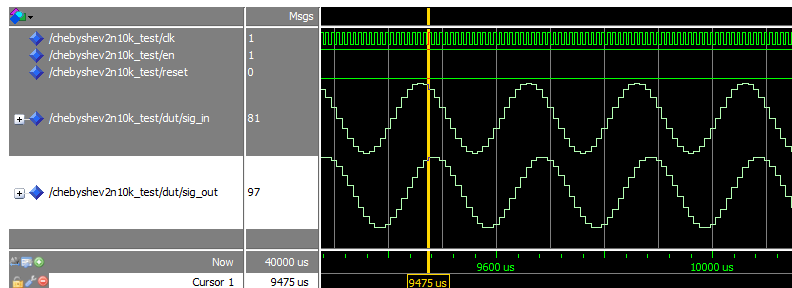


Figure 5.18: Simulation result after a 5kHz sine wave was injected into the LPF with cut off frequency of 10 kHz.

5.6.3 Digital Integrator

A digital integrator was required for the integral action on the sliding-mode control.

Design

This integrator makes use of the trapezoidal rule:

$$\int_a^b f(x) dt \simeq (b-a) \cdot \frac{f(a) + f(b)}{2}. \quad (5.11)$$

The digital equivalent of this is

$$\int f(k) \simeq \int f(k-1) + T_s \cdot \frac{f(k) + f(k-1)}{2} \quad (5.12)$$

VHDL Implementation

The VHDL implementation of the above algorithm is shown in the code listing below. Note how the generic constant *clock_period* is used to make the component re-usable for different clock speeds.

Listing 5.3: VHDL implementation of a digital integrator.

```

1 trapezoidal_rule : process (clk, en, reset)
2   variable x_kz : sfixed(in_bit_high downto in_bit_low) := (others => '0');
3   variable y_k  : sfixed(out_bit_high  downto -30) := (others => '0');
4
5 begin
6   if reset = '1' or en = '0' then
7     x_kz := (others => '0');

```

```

8     sig_out <= (others => '0');
9     elsif rising_edge(clk) then
10    sig_out <= resize(
11        y_k + to_sfixed(0.50,1,-2)*clock_period*(x_kz + sig_in),
12        out_bit_high,out_bit_low
13    );
14    -- a latch will be inferred to remember prev. value of y_k
15    y_k := resize(
16        y_k + to_sfixed(0.50,1,-2)*clock_period*(x_kz + sig_in),
17        y_k
18    );
19    x_kz := resize(sig_in,x_kz);
20 end if;
21 end process trapezoidal_rule;

```

VHDL Simulation

The VHDL code was simulated in ModelSim. A test signal of 50 Hz was injected into the component, which is shown, along with the output signal, in Fig. 5.19. The output sinusoid is seen to have a -90° phase shift relative to the input sinusoid. This is as expected.

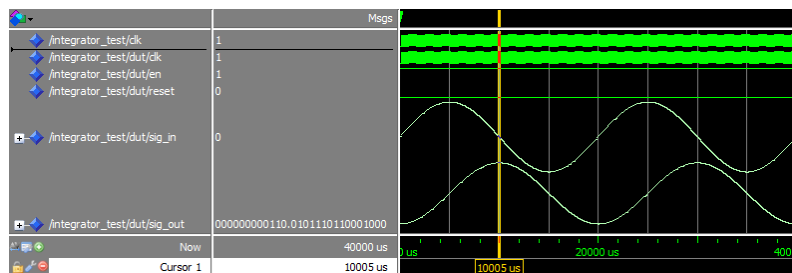


Figure 5.19: Simulation result after a sine wave was injected into the 50Hz LPF.

5.6.4 Digital Differentiator

A digital differentiator was used to implement an early version of algorithm alpha-beta where differentiated capacitor voltages were controlled.

Design

Differentiators are prone to amplify high frequency noise that is inevitably part of the system measurements. Differentiators can be approached as filters, where the frequency response for lower frequencies approximates an ideal differentiator, but where the higher frequencies are attenuated. An example of a noisy digital differentiator is the backwards difference algorithm, expressed as

$$y(n) = \frac{x(n) - x(k-1)}{T}, \quad (5.13)$$

where T is the sampling period. If T is sufficiently small, a close to ideal differentiator is obtained. A simple example of a filter with less high-frequency attenuation is the *central difference algorithm*, expressed as

$$y(n) = \frac{x(n) - x(k-2)}{2T}. \quad (5.14)$$

This can be seen as a difference which is averaged over two periods. The averaging cancels out high frequency fluctuations. The central difference algorithm was implemented and tested in VHDL.

VHDL Implementation

The VHDL implementation of the differentiator is shown in the listing below. Note that the difference signal was never divided by T . This would cause the output signal to be very large. As part of the control algorithm, the signal is scaled down immediately after differentiation, so to avoid unnecessary errors, the two multiplications were merged into one outside of the differentiation process.

Listing 5.4: VHDL implementation of central difference algorithm.

```

1  centralDifference : process (en, reset, clk)
2    --fixed point signals are kept reconfigurable
3    variable x_kz, x_kz2 : sfixed (in_vector_bit_high downto in_vector_bit_low)
4                          := (others => '0');
5    variable y_k : sfixed (out_vector_bit_high downto out_vector_bit_low)
6                          := (others => '0');
7    --sampling frequency is 100kHz, could be made generic
8    constant fs : sfixed (18 downto 0) := to_sfixed(100000.0,18,0);
9  begin
10   if en = '0' and reset = '0' then
11     y_k      := (others => '0');
12     sig_out  <= resize(sig_in,out_vector_bit_high,out_vector_bit_low);
13     x_kz     := (others => '0');
14     x_kz2    := (others => '0');
15   elsif rising_edge(clk) then
16     --central difference calculation
17     sig_out := resize(
18       to_sfixed(0.5,1,-2)*(sig_in-x_kz2),
19       out_vector_bit_high,out_vector_bit_low);
20     --one sample delay on output
21     y_k     := resize(
22       to_sfixed(0.5,1,-2)*fs*(sig_in-x_kz2),
23       y_k'high, y_k'low);
24     --two sample delay on input
25     x_kz2   := resize(x_kz,x_kz2);
26     --one sample delay on input
27     x_kz    := resize(sig_in,x_kz);
28   end if;
29 end process centralDifference;

```

VHDL Simulation

The VHDL code was simulated in ModelSim. A test signal of 50 Hz was injected into the component. The input and output signals are shown in Fig. 5.19. The output sinusoid is seen to have a 90° phase shift relative to the input sinusoid. This is as expected.

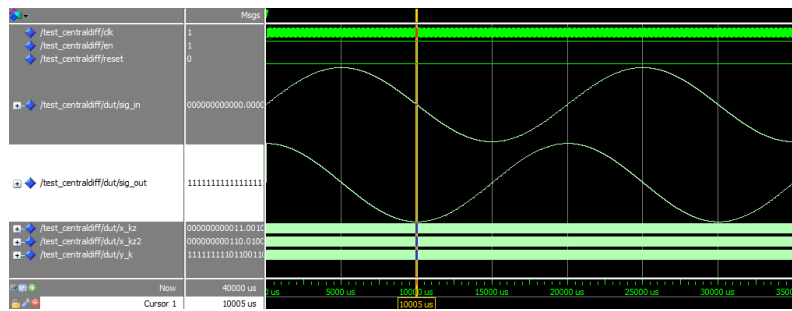


Figure 5.20: Simulation result after a 50 Hz sine wave was injected into the differentiator.

5.6.5 Mean-Square Calculator

The mean-square (MS) calculator is used as an alternative to calculating the root-mean-square (RMS) of a signal. Calculating the RMS would add unnecessary additional computational effort. This effort is avoided by calculating the MS and then using a lookup table to convert from MS to an equivalent peak-value for a 50Hz signal.

Design

The discrete mean-square is calculated as the mean value of a series of squared samples, expressed as

$$MS_d = \frac{1}{n} \sum_{i=0}^n x_i^2. \quad (5.15)$$

The mean-square algorithm was based on the above equation by taking samples at 100kHz and taking the mean over 2000 squared samples. This results in the mean square over a 20ms timeframe, which is the period of 50Hz.

The algorithm is based on a state machine with two states, namely 'hoard' and 'replace'. During the 'hoard' state, a memory array is populated with 2000 measured samples. During this time, each incoming sample is squared and added to a running-sum of squares. After the 2000th sample the mean-square is calculated by multiplying by the reciprocal of 2000.

The state machine then switches permanently to the 'replace' state, which maintains a type of first in first out (FIFO) list. The oldest sample is replaced by the incoming sample on each sample clock rising edge and the mean square is calculated by subtracting the square of the oldest sample and adding the square of the newest sample.

VHDL Implementation

The VHDL implementation of the mean-square algorithm is shown in the code listing below.

Listing 5.5: VHDL implementation of a mean-square calculator.

```

1 process (en, system_clock, sample_clock)
2   variable hoarding : boolean := true;
3   begin
4
5   if en = '0' then
6     state <= hoard;
7     hoarding := true;

```

```

8   elsif (hoarding = true) and (last_in < std_logic_vector( to_signed( 1999, 12 )))
9       then
10      state <= hoard;
11      hoarding := true;
12  elsif (hoarding = true) and (last_in = std_logic_vector( to_signed( 1999, 12 )))
13      then
14      hoarding := false;
15      state <= replace;
16  elsif (rising_edge(system_clock)) then
17
18      -- Determine the next state synchronously, based on
19      -- the current state and the input
20      case state is
21      when hoard=>
22          mean_square <= (others => '0');
23          state <= hoard;
24
25      when replace=>
26          mean_square <= resize (
27              mean_square_running*to_ufixed(0.0005,0,-23),
28              mean_square'high, mean_square'low);
29          state <= replace;
30      end case;
31
32  end if;
33 end process;
34
35 -- Determine the output based only on the current state
36 -- and the input (do not wait for a clock edge).
37 process
38 begin
39     wait until rising_edge(sample_clock);
40     case state is
41     when hoard=>
42         wave_array(to_integer(signed(last_in))) <= resize(to_ufixed(unsigned(abs(
43             wave))),V_meas_high, V_meas_low );
44         --update indexes
45         --prevent overflow
46         if (last_in < std_logic_vector( to_signed( 1999, 12 ))) then
47             last_in <= last_in + std_logic_vector( to_signed( 1, 12 ));
48             mean_square_running <= resize(
49                 mean_square_running + to_ufixed(unsigned(abs(wave))*
50                     to_ufixed(unsigned(abs(wave))),
51                     mean_square_running'high, mean_square_running'low);
52         else
53             last_in <= std_logic_vector( to_signed( 1999, 12 ));
54             mean_square_running <= resize(
55                 mean_square_running,
56                 mean_square_running'high, mean_square_running'low);
57         end if;
58         first_in <= (others => '0');

```

```

58   when replace=>
59     wave_array(to_integer(signed(first_in))) <= resize(to_ufixed(unsigned(abs(
        wave))),V_meas_high, V_meas_low ); --replace first in with new sample
60
61     mean_square_running <= resize(
62       mean_square_running
63       + to_ufixed(unsigned(abs(wave)))*to_ufixed(unsigned(abs(wave))
        )
64       - to_ufixed(unsigned(wave_array(to_integer(signed(first_in))))
        )*to_ufixed(unsigned(wave_array(to_integer(signed(first_in
        ))))),
65       mean_square_running'high, mean_square_running'low);
66
67     --update indexes
68     last_in <= first_in;
69     --prevent overflow
70     if (first_in < std_logic_vector( to_signed( 1999, 12 ))) then
71       first_in <= first_in + std_logic_vector( to_signed( 1, 12 ));
72     else
73       first_in <= (others => '0');
74     end if;
75
76   end case;
77
78 end process;

```

VHDL Simulation

The Modelsim simulation result is shown below in Fig. 5.21 where the resulting mean-square value of 'sig_in' is highlighted in orange. The test bench generates a 50Hz input sinusoid of amplitude 12,700kV_{rms}, which drops to 5kV_{rms} after 5ms.

The output is seen to be zero for the first 20ms in the 'hoard' phase of the algorithm after which it settles on a value of 161 276 877 where the ideal value is 161 290 000. This yeilds a 99.992 % accuracy. After the drop, the output takes 20ms to settle on the new mean-square value of 24997667 where the icial value would be 25000000. This yields an accuracy of 99.999%.

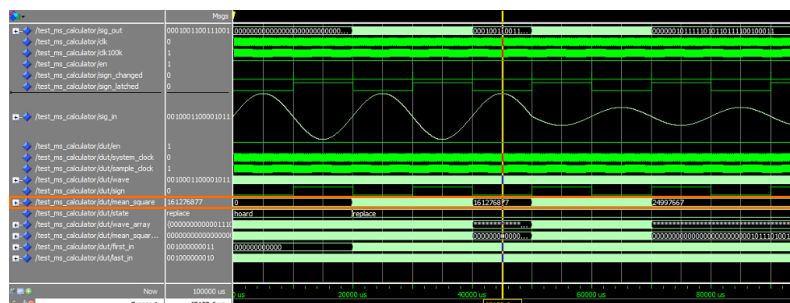


Figure 5.21: Simulation result on a 50Hz signal with amplitude of 12,700kV_{rms} up until 5ms and then 5kV_{rms} after that.

5.7 Summary

This Chapter is concluded with a summary of the main points presented:

- FGPA's have numerous valuable benefits for embedded design
- The FPGA's technical specifications were outlined
- The design and simulation approach was described
- The supervisory control design was explained by use of diagrams
- The design of generic and reusable synthesisable VHDL components were detailed.

CHAPTER 6

APPLICATION OF SLIDING MODE CONTROL

“Man’s greatness consists in his ability to do and the proper application of his powers to things needed to be done.”

- Frederick Douglass

6.1 Introduction

In Chapter 3, sliding mode control was applied to a synchronous DC-DC buck converter. This was done knowing that the MVEVR regulator module topology is effectively a combination of two synchronous buck converters that are arranged in such a way as to handle alternating input voltage polarities. To see the similarities of the MVEVR topology to the synchronous buck converter, compare Fig. 4.14 to Fig. 3.6. The MVEVR’s switching scheme determines that, during the positive half of the input voltage the top buck converter is switching, and during the negative half of the input voltage, the bottom synchronous buck converter is switching.

The main difference between the MVEVR topology and the synchronous buck converter topology is that the input source of the MVEVR module is AC, as opposed to DC, and the MVEVR module model is of the order five as opposed to the order two. The MVEVR module has three more reactive components in its model than that of the synchronous buck converter. These additional components are the leakage inductance of the auto-transformer, the input bus capacitor and the inductive load. Furthermore, it was shown in Chapter 4 that the transformer leakage inductance and the module input bus capacitor form a resonant pair that is vulnerable to oscillation and needs to be actively controlled. These added complexities transform the control problem into somewhat of a monster, and renders much of the established design techniques useless.

In this Chapter, the control problem is framed along with the control objectives. The sliding mode controller is designed, and new design methodologies are developed as the chapter progresses. Simulations are used to analyse and validate the design.

As a precursor to closed loop control, open loop control was also developed and implemented for the MVEVR, and is documented in Appendix B.

6.2 Framing the Control Problem

In this section, a SMC algorithm is developed for the MVEVR regulator unit as modelled in Chapter 4, and shown in Fig. 4.14. Each regulator module in the series-stacked configuration will be controlled separately. A system-level process will determine the discrepancy between the system (line) input voltage and the system (line) output voltage reference. The regulator modules are to cancel out these discrepancies by adding appropriate voltages to the input voltage in a series configuration. The system voltage error will be used to generate

and feed output voltage references to each of the regulator modules (refer to Fig. 4.1). Fig. 6.1 shows how the references under consideration fit into the system layout. The input line voltage (v_{LN}) is applied across the common winding of the regulated autotransformer, and the output voltage references, (v_{Reg1}^* and v_{Reg2}^*), are required for each of the regulator modules to achieve the desired line voltage across the load (v_{LN}^*).

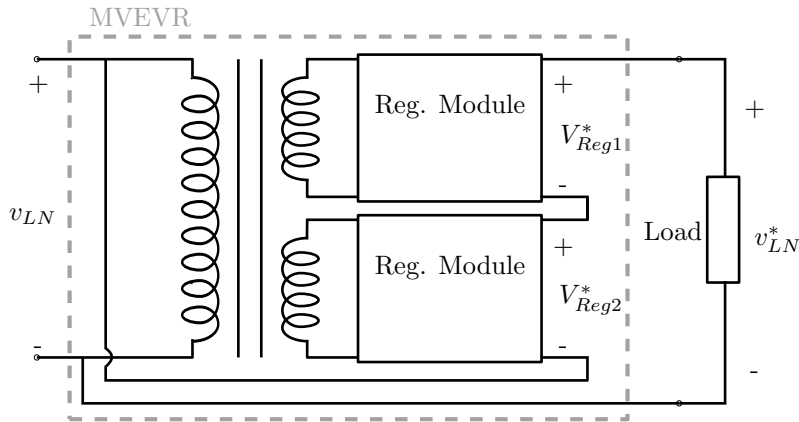


Figure 6.1: Shown is a schematic diagram of the MVEVR system configuration. The input line voltage is represented by v_{LN} , the regulator module output voltage references by v_{Reg1}^* and v_{Reg2}^* , and the desired line voltage across the load by v_{LN}^* .

An expression for the output voltage references for the individual regulators can be obtained by analysing the output voltage loop shown in Fig. 6.1. Using Kirchoff's voltage law, the following equation holds:

$$v_{LN} + v_{Reg1}^* + v_{Reg2}^* = v_{LN}^*. \quad (6.1)$$

Since both regulator modules are identical, the reference line voltage, v_{LN}^* , can be achieved if both modules can track references expressed as

$$v_{Reg1}^* = v_{Reg2}^* = \frac{v_{LN}^* - v_{LN}}{n}, \quad (6.2)$$

where n is the integer number of modules in operation. This expression assumes that the reference line voltage is of greater magnitude than the actual line voltage, the MVEVR cannot currently compensate for over-voltages.

It should be noted that Eq. 6.2 can easily be adapted, should one of the regulators fail. In this case the module fault causes the module bypass crowbar to activate, which effectively short-circuits the output of the faulty module and thereby assumes the load current from the module. The integer divider in Eq. 6.2 is decremented, and the remaining regulator keeps the system in a type of "limp mode", where the output voltage is regulated as much as possible with the available resources. This is another advantage of a modular approach to system design. If one of the modules fail, the system can still operate on the remaining module(s).

6.2.1 System Control Objectives

Before developing control system, the system control objectives must be stated. The system-level control objectives are related to the requirements on the quality of the output line voltage, guided by NERSA's regulations. These objectives are stated below.

Robust voltage amplitude regulation of the 12.7kV_{LN} distribution line, within 1 % of the rated voltage.

According to the NRS 048 standard, distribution voltages above 500 V are to remain within $\pm 5\%$ of rated values.[2] The control objective in terms of amplitude regulation will be to remain within 1% deviation of the rated line voltage. This should provide scope for the distribution line to be lengthened beyond the installation point of the MVEVR. Regulation of the line voltage amplitude must be robust with respect to uncertainties and variations of network parameters. The uncertainty applies specifically to the load impedance and the input impedance, because these parameters are largely unpredictable.

Harmonic suppression up to the order 20, with THD under 8 %

According to the NRS 048 standard,

“The THD of the supply voltage, including all harmonics up to the order 40, shall not exceed 8 %.”[2]

Although specifications are given for all harmonics up to the order 40 (2 kHz), harmonic compensation in the MVEVR will only be attempted up to the order 20 (1 kHz). The MVEVR exhibits high gain at frequencies around 1.5 kHz (refer to Fig. 4.18), and frequencies above 1 kHz are therefore avoided. This is due to unavoidable resonance between the transformer leakage inductance and the regulator bus capacitors (refer to Fig. 4.14).

6.3 MVEVR Modular SMC Design

Sliding mode control will be applied on a regulator module level. Each module will receive its own output voltage reference from a system-level process. Each module's control component is then responsible for generating corresponding references for other internal voltages and currents that need to be controlled, and for generating the appropriate control commands to reach those references.

6.3.1 Regulator Module Control Objectives

Clear objectives are required for module level control in order to design the control system according to some specifications. The control objectives are inferred from the system-level objectives as detailed below.

Robust tracking of sinusoidal output-voltage reference within 10 %

The voltage amplitude regulation target on *system level* is set at 1% deviation of the rated line voltage. Because the modules only regulate 10% of the system voltage, the system requirement implicitly sets a maximum tracking error specification on *module level* that is ten times larger than the system-level target. The system amplitude error specification can be expressed mathematically as

$$\frac{V_{LN_{rated}} - V_{LN_{out}}}{V_{LN_{rated}}} \leq 0.01, \quad (6.3)$$

where $V_{LN_{out}}$ is the output voltage amplitude of the MVEVR and $V_{LN_{rated}}$ is the reference for that same voltage.

Also, the regulated (output) line voltage is equal to the following sum:

$$V_{LN_{out}} = V_{LN} + 2 \cdot V_{Reg}, \quad (6.4)$$

with both regulator units assumed to be contributing the same voltage. Substituting Eq. 6.4 into Eq. 6.3 and rearranging yields

$$V_{LN_{rated}} - V_{LN} - 2 \cdot V_{Reg} \leq 0.01 \cdot V_{LN_{rated}}. \quad (6.5)$$

The ideal amplitude regulation relationship (zero amplitude error) is expressed as

$$V_{LN_{rated}} - V_{LN} - 2 \cdot V_{Reg}^* = 0, \quad (6.6)$$

with V_{Reg}^* being the output voltage reference of the regulator module corresponding to V_{Reg} . Subtracting Eq. 6.6 from Eq. 6.5, along with some algebraic manipulation, yields the constraint on the normalised amplitude regulation error on module level:

$$\frac{\overbrace{V_{Reg}^* - V_{Reg}}^{\text{Regulation Error}}}{V_{Reg}^*} \leq \frac{0.005 \cdot V_{LN_{rated}}}{V_{Reg}^*}. \quad (6.7)$$

It is clear from the right-hand side of the above expression that the restriction on the regulation error relaxes as the regulator amplitude reference, V_{Reg}^* , decreases. The worst case target was used as the norm. If this is met, the amplitude tracking error will always be within specifications. The worst case (maximum) regulator amplitude reference is expressed as

$$V_{Reg}^* (\text{max}) = 0.5 \cdot \left(1 - \frac{1}{1.1} \right) \overbrace{V_{LN_{rated}} - V_{LN(\min)}}^{\text{V}_{LN_{rated}} - V_{LN(\min)}}, \quad (6.8)$$

where $V_{LN(\min)}$ is the smallest input line voltage that can successfully be regulated to the rated value by boosting with the maximum MVEVR capacity of 10%.

Substituting Eq. 6.8 into the right-hand-side of Eq. 6.7 yields

$$\frac{V_{Reg}^* - V_{Reg}}{V_{Reg}^*} \leq 0.11. \quad (6.9)$$

The maximum allowable voltage amplitude regulation error for each module was therefore set to 10% .

Regulator Module Current Limitation

The steady-state load current through the MVEVR is not to exceed 100 A. Hardware protection mechanisms, as well as controller supervisory protection mechanisms are in place to bypass the regulators in the event of unavoidable over-current situations. The control algorithm will, however, be designed in such a way as to limit over currents during transients.

Over-all stability

Internal system signals are to remain bounded at all times. Oscillations at frequencies other than 50 Hz and the switching frequency must be damped. This objective speaks clearly to the need of damping oscillations on the regulator module input bus.

6.3.2 Control Design and Simulation Approach

Simulations were performed on the system throughout the entire design process to validate mathematical models, to gain an understanding of the system capabilities and constraints, and to develop suitable references and

control algorithms. The VHDL-AMS modelling language was used to develop and test control algorithms in proprietary circuit simulation software (SystemVision). This was very useful, as the developed algorithms could easily be adapted from VHDL-AMS to synthesisable VHDL for implementation on the FPGA controller. This saved time on implementing the design, and also reduced the opportunities for errors in translation from development to implementation.

6.3.3 Sliding Function Selection

An important part in the SMC design procedure is the selection of a suitable sliding function. This function expresses the control objectives in terms of the plant state variables in such a way that the objectives are satisfied when the sliding function is driven to zero. The selection of the sliding function has to take the following factors into account:

What signals are available for measurement? In ideal sliding mode control, all of the state variables are assumed to be available for measurement. In reality, this is rarely the case. Sliding mode observers can be developed for full state estimation. This does, however, add complexity and computational effort to the design. So called *output feedback* sliding mode controllers can be developed, where only the output variables are used in the sliding function. This can detract from performance, robustness, and even stability.[23] A reasonable compromise can be drawn, where a subset of the system state variables (including the output variables) are measured and controlled. If the correct state variables are controlled with appropriate references, a controller with good stability, performance and robustness can be obtained. In the MVEVR, the system input voltage, regulator input current, regulator input bus voltage, regulator output filter inductor current, regulator output voltage, and output current could be measured. The system controller board, however, could only receive eight measurements in total. Measurements of all five state variables for both regulator modules was therefore not possible, and only a subset of the state variables were measured.

What signals should be controlled? Some system variables are absolutely crucial to be controlled towards some reference, while the remaining signals will be naturally stable and follow the desired trajectory. The MVEVR regulator module has an inherently undamped input bus. The leakage inductance of the transformer, together with the bus capacitor forms an LC pair with resonant frequency in-between the closed loop bandwidth and the switching frequency. As a result, an oscillation at the resonant frequency appears on the input bus which needs to be damped. Control of either the input current or the bus capacitor current was found to be effective in damping this oscillation. Controlling the output voltage directly without regard for the output filter inductor current was insufficient for a stable, non-oscillatory response. Control was therefore added to the filter inductor current as well as the output voltage. Integral control of the output voltage error was also added to reduce the tracking error.

How will the control reference be generated? For an AC-AC voltage regulator, the only external reference is the reference of the desired output voltage. References for the controlled internal variables must be generated by the module-level control scheme. Careful consideration is necessary to ensure that appropriate reference signals can be generated. This is discussed in the following section.

Two different sliding functions emerged as good candidates for the MVEVR. The one will be referred to as sigma-alpha and the other as sigma-beta.

Sigma-Alpha

This algorithm makes use of a subset of the standard state variables (inductor currents and capacitor voltages), as developed for the MVEVR model in Section 4.3. Algorithm 3 is seen to be a linear combination of the

selected state variable errors.

Algorithm 3 Sigma-Alpha

$$\sigma_\alpha = \mathbf{C}_\alpha^T \mathbf{x}_\alpha \quad (6.10)$$

$$= \alpha_1 (i_i - i_i^*) + \alpha_2 (i_{L_o} - i_{L_o}^*) + \alpha_3 (v_{c_o} - v_{c_o}^*) + \alpha_4 \left(\int v_{c_o} - \int v_{c_o}^* \right) \quad (6.11)$$

where

$$\mathbf{C}_\alpha^T = [\alpha_1 \quad \alpha_2 \quad \alpha_3 \quad \alpha_4] \quad (6.12)$$

$$\mathbf{x}_\alpha = \begin{bmatrix} x_{\alpha_1} \\ x_{\alpha_2} \\ x_{\alpha_3} \\ x_{\alpha_4} \end{bmatrix} = \begin{bmatrix} i_i - i_i^* \\ i_{L_o} - i_{L_o}^* \\ v_{c_o} - v_{c_o}^* \\ \int (v_{c_o} - v_{c_o}^*) \end{bmatrix}, \quad (6.13)$$

and reference signals are marked with an asterisk.

The sliding function coefficients, \mathbf{C}_α^T , are usually chosen such that the mathematical conditions for sliding mode is satisfied. In this application, the sliding coefficients were all initially chosen as unity, and then adjusted until favourable simulation results were obtained.

Table 6.1 shows how the weighted terms in Eq. 6.11 of Algorithm 3 relate to the control objectives.

Table 6.1: Relation between the terms of sliding function σ_α and the control objectives.

Control Objective	Sliding Function Terms
Voltage amplitude regulation	$\alpha_1 (v_{c_o} - v_{c_o}^*) + \alpha_4 \left(\int v_{c_o} - \int v_{c_o}^* \right)$
Voltage tracking	$\alpha_1 (v_{c_o} - v_{c_o}^*) + \alpha_4 \left(\int v_{c_o} - \int v_{c_o}^* \right)$
Current limiting	$\alpha_2 (i_{L_o} - i_{L_o}^*)$
Input bus stability	$\alpha_1 (i_{in} - i_{in}^*)$
Output bus stability	$\alpha_2 (i_{L_o} - i_{L_o}^*)$

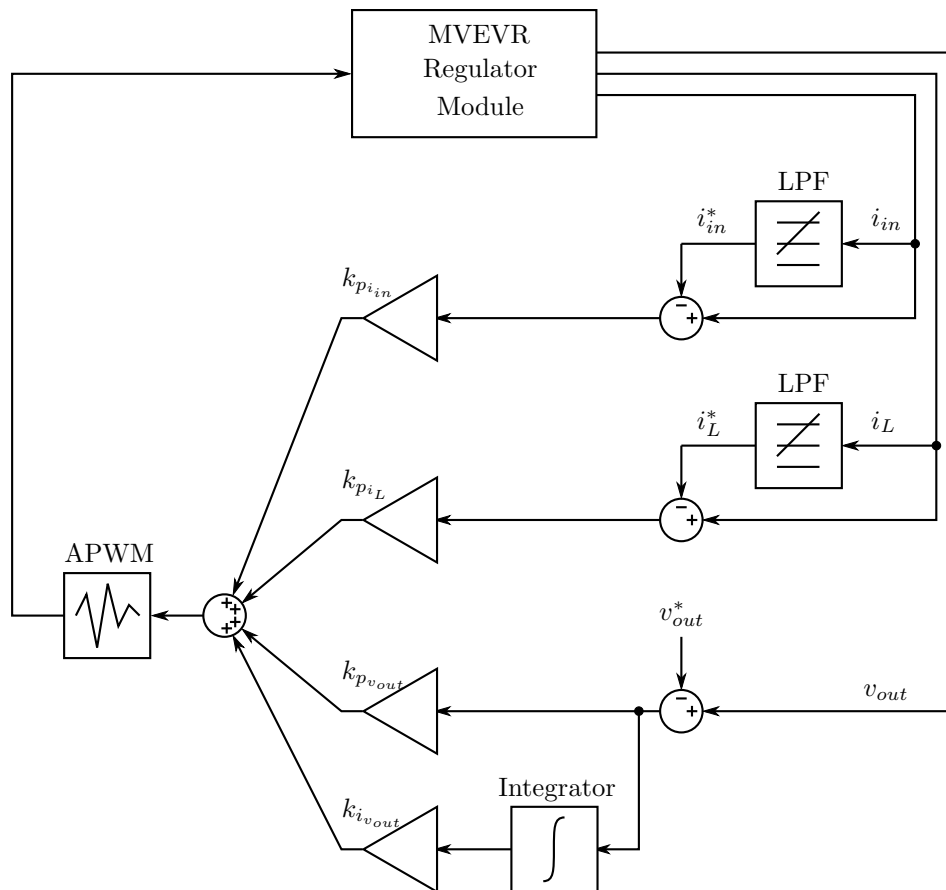


Figure 6.2: Schematic Representation of Algorithm Sigma-Alpha. The measured voltage and currents from the MVEVR module hardware are fed into the algorithm where the corresponding references are subtracted. The voltage reference comes from a system level process, while the current references are generated on the fly by low-pass filters. The error signals are weighted, added, and modulated by the adaptive pulse width modulator (APWM) to form a control signal which is fed back to the switching hardware.

Sigma-Beta

This algorithm takes an approach derived from the canonical control approach for DC-DC buck converters, as applied in [11]. Instead of controlling the inductor currents, the derivatives of the capacitor voltages (i.e. the capacitor currents) are controlled. To ensure stability on the input bus, a type of double-canonical approach is followed, where the input voltage, the derivative of the input voltage, the output voltage, and the derivative of the output voltage are controlled. One advantage of this approach is that, by measuring the capacitor voltages, the capacitor currents can easily be estimated with differentiator components. There are then only two measurements required per regulator module for control. Model invariant references are also much easier to generate for voltages than for currents. Another advantage is that no control is exerted on the load current, which can possibly result in extreme robustness (even invariance) with respect to load magnitude and load type (resistive, reactive, or non-linear). The lack of control on the load current would, however, require some extra provision to be made for current limiting. This algorithm would also require the derivation of a new model of the MVEVR regulator unit with different state variables.

After some practical tests it was found that the differentiated signals had to be fiercely filtered to reduce noise levels. A practical workaround was to rather measure the capacitor currents directly, instead of estimating them. It was also found that the control on the input voltage could be omitted without much effect. The final algorithm is shown in Algorithm 4 and is seen to be a linear combination of a new set of variable errors.

Algorithm 4 Sigma-Beta

$$\sigma_\beta = \mathbf{C}_\beta^T \mathbf{x}_\beta \quad (6.14)$$

$$= \beta_1 (\dot{v}_{Cbs} - \dot{v}_{Cbs}^*) + \beta_2 (v_{c_o} - v_{c_o}^*) + \beta_3 (\dot{v}_{c_o} - \dot{v}_{c_o}^*) + \beta_4 \left(\int v_{c_o} - \int v_{c_o}^* \right) \quad (6.15)$$

where

$$\mathbf{C}_\beta^T = [\beta_1 \quad \beta_2 \quad \beta_3 \quad \beta_4] \quad (6.16)$$

$$\mathbf{x}_\beta = \begin{bmatrix} x_{\beta_1} \\ x_{\beta_2} \\ x_{\beta_3} \\ x_{\beta_4} \end{bmatrix} = \begin{bmatrix} \dot{v}_{Cbs} - \dot{v}_{Cbs}^* \\ v_{c_o} - v_{c_o}^* \\ \dot{v}_{c_o} - \dot{v}_{c_o}^* \\ \int (v_{c_o} - v_{c_o}^*) \end{bmatrix}, \quad (6.17)$$

and reference signals are marked with an asterisk.

The sliding function coefficients for sigma-beta, \mathbf{C}_β^T , were kept the same as for sigma-alpha, with some minor adjustments to maintain stability.

Table 6.2 shows how the weighted terms in Eq. 6.15 of Algorithm 4 relate to the control objectives.

Table 6.2: Relation between the terms of sliding function σ_β and the control objectives.

Control Objective	Sliding Function Terms
Voltage amplitude regulation	$\beta_2 (v_{c_o} - v_{c_o}^*) + \beta_4 \left(\int v_{c_o} - \int v_{c_o}^* \right)$
Voltage tracking	$\beta_2 (v_{c_o} - v_{c_o}^*) + \beta_4 \left(\int v_{c_o} - \int v_{c_o}^* \right)$
Current limiting	no provision made for this
Input bus stability	$\beta_1 (\dot{v}_{Cbs} - \dot{v}_{Cbs}^*)$
Output bus stability	$\beta_3 (\dot{v}_{c_o} - \dot{v}_{c_o}^*)$

After much consideration, algorithm Sigma-Alpha was chosen for final implementation due to its versatility in addressing the control objectives. The rest of this chapter will thus focus exclusively on this algorithm, although practical results for algorithm Sigma-Beta, and a hybrid of the two, Sigma-AlphaBeta, are shown in Appendix C.

After an appropriate sliding function is found, the designer is left to find mechanisms for generating appropriate references. The sliding weights, \mathbf{C}_α^T , or \mathbf{C}_β^T , must be chosen such that the sliding mode exists, and such that the system trajectory is driven towards the stable equilibrium position (zero error). A switching law must be developed that will drive the system from its initial state onto the sliding manifold, and constrain it to that manifold where-ever and when-ever possible.

6.3.4 Reference Generation

The regulator module receives a sinusoidal output voltage reference from a system process. This reference is in-phase with the input line voltage of the MVEVR. The regulator's control processes is then responsible for generating *reachable* reference waveform for the other controlled state-variables.

In order for a reference to be reachable, it must exist within the envelope of the steady state waveforms corresponding to the 'on' and 'off' states. Sample references are shown for simulated steady-state waveforms of the controlled variables in Figs. 6.3-6.5.

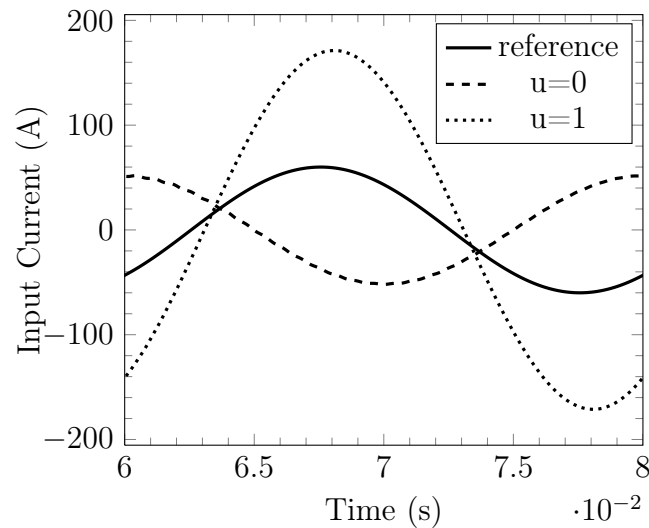


Figure 6.3: The regulator input current reference lies in-between the two possible steady-state waveforms. The 'on' state is represented by ' $u = 1$ ' and the 'off' state is represented by ' $u = 0$ '.

In the case of the input current (Fig. 6.3), it can be seen that the steady-state waveform corresponding to the 'off' state ($u = 0$) is not zero with respect to time. When the regulator is in the 'off' state, source current is still flowing from the series windings through the bus and snubber capacitors. A constant input current reference of zero would therefore not be reachable.

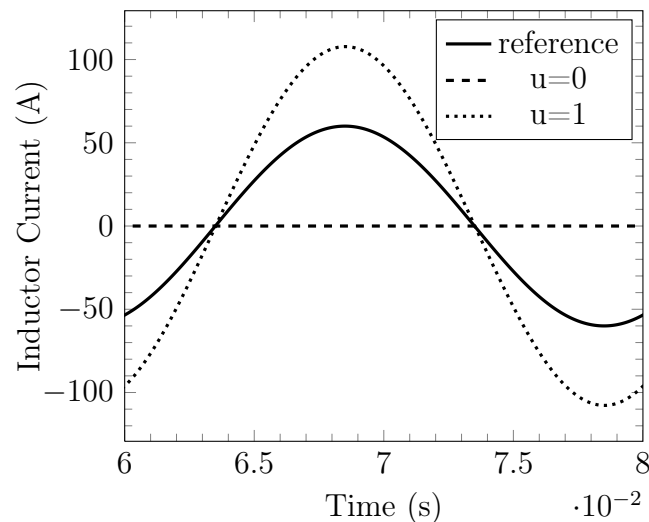


Figure 6.4: The regulator inductor current reference lies between the two possible steady-state waveforms.

Note that the inductor current steady-state waveforms (Fig. 6.4) shows no ripple. This is because no switching occurs at steady state. When switching at a near-maximum reference, instantaneous inductor current values (with ripple) could likely exceed the instantaneous steady-state value of the 'on' state. The average value of over a switching period will, however be within the upper and lower steady-state bounds.

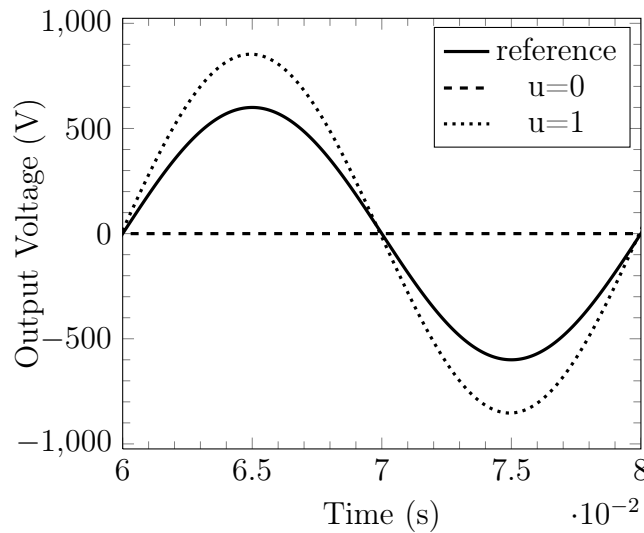


Figure 6.5: The regulator output voltage reference lies in-between the two possible steady-state waveforms.

Note that the output voltage reference (Fig. 6.5) is in phase with its steady-state counterparts. The steady-state waveform when $u = 1$ is in phase with the system input and output voltage. The reference for the regulator output voltage would therefore have to be synchronised with the system (line) input voltage.

It can be seen that the references for the input current, inductor current, and output voltage are all out of phase with respect to each other. On account of the possibly varying load impedance, there is no simple, fixed relation between the relative phase shifts, as well as the relative magnitudes, of the current references with respect to the required output voltage reference. These differ greatly with respect to the load impedance. This is because the steady-state boundary waveforms are affected by the load impedance. In fact, in the case of the input current, the upper steady-state boundary undergoes a phase-shift with respect to the lower steady state boundary when the load impedance changes. These factors complicate the reference generation process, because both the reference phase and amplitude must be controlled. A cardinal control objective is to gain robustness with respect to the load. Static references are therefore not an option.

Three approaches for reference generation are proposed in order to ensure reachability as well as load independence:

1. The first considered approach was to calculate, in real time, the required phase and amplitude values for sinusoidal current references with respect to the given output voltage reference. The resulting references would have to exist within the respective uncertain steady-state boundaries. This would require reference boundaries (steady-state waveforms), and in turn the load impedance to be estimated. If all of the state variables are not measured, a full state observer would have to be designed. This technique assumes a linear load with sinusoidal load current.
2. The second approach was to allow the system to naturally generate its own current references by simply low-pass filtering the measured currents and using these as references. (This technique is suggested in [23]). The reference for each current would, therefore, be the current signal itself with any switching ripple or oscillation suppressed. The dynamics of the filter would have to be added to the plant model as additional state variables. This approach should work well depending on the magnitude of the phase shift introduced by the filter. If the phase shift is big, it could cause the reference to become unreachable at times.

3. The third approach is an attempt to shift the control problem to a domain where references are easier to generate. This came after discovering that control could be effected by regulating the output filter capacitor current, rather than the output filter inductor current, as done in [11]. This concept was extended to the MVEVR's input filter as well. A reference for the input filter capacitor current could easily be generated by doing simple peak detection and zero-crossing detection on the voltage over the regulator unit's input bus capacitor. Because the input bus voltage is ideally sinusoidal with measureable amplitude and phase, the reference for the current into the capacitor would simply be the derivative of this sinusoid.

In an attempt to follow the first approach, a procedure was developed to, during the initial system start up, characterise the steady-state reference boundaries in terms of amplitude and phase, based on ADC measurements. An algorithm was developed to generate the required reference waves inside the envelope of their respective initial boundary waves. This was successful until the load changed, which in turn changed the steady-state boundary waveforms. The required estimation of the reference boundaries would add too much complexity to the controller, and this approach was subsequently abandoned.

The second and third approaches, as well as a hybrid between the two, were implemented with good success and the first approach will be documented further in the following sections.

Developing an expression for the current references' filter dynamics

The reference for the regulator's output filter inductor current and input current is obtained by measuring the real current and filtering out the switching ripple or any other unwanted oscillations. This will affect the dynamic behaviour of the sliding mode control, as the low-pass filter (LPF) will introduce a phase shift in the reference. It was suggested in [23, p. 8-15] that the reference filter dynamics be modelled in order to include its effect in the SMC existence analysis and equivalent control.

First order LPFs were designed for the reference generation. The s-domain filter expression is given by

$$I^*(s) = I(s) \cdot \frac{1}{\tau s + 1}, \quad (6.18)$$

where $I^*(s)$ is the current reference (LPF output) in the s-domain, $I(s)$ is the measured current (LPF input) in the s-domain and τ is the filter time constant, which can also be expressed as

$$\tau = \frac{1}{2\pi f_c}, \quad (6.19)$$

where f_c is the filter cut-off frequency in Hertz. Cross-multiplying Eq. 6.18, rearranging, and taking the inverse Laplace transform yields

$$\frac{di^*}{dt} = -\frac{1}{\tau}i^* + \frac{1}{\tau}i, \quad (6.20)$$

where i^* is the current reference and i is the measured current. During simulations, a cut-off frequency of 350 Hz was found to produce the desired response. This corresponds to a time constant of $\tau = 454.7 \mu s^{-1}$. The digital filter design and VHDL implementation are documented in Section 5.6.

The filter reference dynamics for both the regulator input current and the output filter inductor current could then be modelled as

$$\frac{d}{dt} \begin{bmatrix} i_{in}^* \\ i_{Lo}^* \end{bmatrix} = \begin{bmatrix} \frac{1}{\tau}i_{in} - \frac{1}{\tau}i_{in}^* \\ \frac{1}{\tau}i_{Lo} - \frac{1}{\tau}i_{Lo}^* \end{bmatrix}. \quad (6.21)$$

6.3.5 Model adaptations for SMC

For the purpose of applying SMC, some model adaptations were needed. The state-space switching model derived in Chapter 4, Section 4.3.3, was modified to achieve the following goals:

1. transformation from state space form to vector field representation
2. inclusion of output voltage integral dynamics
3. transformation of the tracking problem into a regulation problem.

Vector Field Representation

The state space switching model will be expressed in the form of Eq. 3.1 in Chapter 3 (restated below for convenience), where function vectors are used instead of a matrix representation. This is less compact, but will allow for more straight-forward adaptation toward reaching the control objectives listed above. The function vector, $\mathbf{f}(\mathbf{x}, t)$, is called the *drift field*, while the function vector, $\mathbf{g}(\mathbf{x}, t)$ is called the *control input field*. The system is now expressed as

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, t) + \mathbf{g}(\mathbf{x}, t) u, \quad (6.22)$$

where

$$\mathbf{f}(\mathbf{x}, t) = \mathbf{A}\mathbf{x} + \mathbf{F} = \begin{bmatrix} -\left(\frac{R_{sbs}+R_i}{L_i}\right) i_{in} - \left(\frac{1}{L_i}\right) v_{Cbs} + \left(\frac{1}{L_i}\right) v_i \\ \left(\frac{1}{C_{bs}}\right) i_{in} \\ -\left(\frac{R_{soL}+R_{soC}}{L_o}\right) i_{Lo} - \left(\frac{1}{L_o}\right) v_{Co} + \left(\frac{R_{soC}}{L_o}\right) i_o \\ \left(\frac{1}{C_o}\right) i_{Lo} - \left(\frac{1}{C_o}\right) i_o \\ \left(\frac{R_{soC}}{L_i}\right) i_{Lo} + \left(\frac{1}{L_i}\right) v_{Co} - \left(\frac{R_{soC}+R_l}{L_l}\right) i_o \end{bmatrix} \quad (6.23)$$

$$\mathbf{g}(\mathbf{x}, t) = \mathbf{B} = \begin{bmatrix} \left(\frac{R_{sbs}}{L_i}\right) i_{Lo} \\ -\left(\frac{1}{C_{bs}}\right) i_{Lo} \\ \left(\frac{1}{L_o}\right) v_{Cbs} - \left(\frac{R_{sbs}}{L_o}\right) i_{Lo} + \left(\frac{R_{sbs}}{L_o}\right) i_{in} \\ 0 \\ 0 \end{bmatrix}. \quad (6.24)$$

Augmenting the Integral Term to the Vector Field Model

Integral action was included into the control to reduce the tracking error. The integral dynamics can (trivially) be expressed as

$$\frac{d\left(\int v_{Co} dt\right)}{dt} = v_{Co}. \quad (6.25)$$

Augmenting the model in Eq. 6.22 with the above integrator dynamics yields the following model:

$$\dot{\mathbf{x}}' = \mathbf{f}'(\mathbf{x}', t) + \mathbf{g}'(\mathbf{x}', t) u, \quad (6.26)$$

with

$$\mathbf{x}' = \begin{bmatrix} i_{in} \\ v_{C_{bs}} \\ i_{L_o} \\ v_{C_o} \\ i_o \\ \int v_{C_o} dt \end{bmatrix} \quad (6.27)$$

$$\mathbf{f}'(\mathbf{x}', t) = \begin{bmatrix} -\left(\frac{R_{s_{bs}}+R_i}{L_i}\right) i_{in} - \left(\frac{1}{L_i}\right) v_{C_{bs}} + \left(\frac{1}{L_i}\right) v_i \\ \left(\frac{1}{C_{bs}}\right) i_{in} \\ -\left(\frac{R_{s_{oL}}+R_{s_{oC}}}{L_o}\right) i_{L_o} - \left(\frac{1}{L_o}\right) v_{C_o} + \left(\frac{R_{s_{oC}}}{L_o}\right) i_o \\ \left(\frac{1}{C_o}\right) i_{L_o} - \left(\frac{1}{C_o}\right) i_o \\ \left(\frac{R_{s_{oC}}}{L_i}\right) i_{L_o} + \left(\frac{1}{L_i}\right) v_{C_o} - \left(\frac{R_{s_{oC}}+R_l}{L_i}\right) i_o \\ v_{C_o} \end{bmatrix} \quad (6.28)$$

$$\mathbf{g}'(\mathbf{x}, t) = \begin{bmatrix} \frac{R_{s_{bs}} i_{L_o}}{L_i} \\ \frac{i_{L_o}}{C_{bs}} \\ \frac{v_{C_{bs}} - R_{s_{bs}} i_{L_o} + R_{s_{bs}} i_{in}}{L_o} \\ 0 \\ 0 \\ 0 \end{bmatrix}. \quad (6.29)$$

From tracking to regulation

The augmented vector field model is now expressed in terms of the error between a subset of the previous state variables and their respective references. The state-variables that are not found in the sliding function specified in Algorithm 3 have been dropped. The system is now expressed as

$$\dot{\mathbf{x}}_\alpha = \mathbf{f}_\alpha(\mathbf{x}_\alpha, t) + \mathbf{g}_\alpha(\mathbf{x}_\alpha, t) u, \quad (6.30)$$

with

$$\dot{\mathbf{x}}_\alpha = \frac{d}{dt} \begin{bmatrix} x_{\alpha_1} \\ x_{\alpha_2} \\ x_{\alpha_3} \\ x_{\alpha_4} \end{bmatrix} = \frac{d}{dt} \begin{bmatrix} i_{in} - i_{in}^* \\ i_{L_o} - i_{L_o}^* \\ v_{C_o} - v_{C_o}^* \\ \int (v_{C_o} - v_{C_o}^*) \end{bmatrix}, \quad (6.31)$$

$$\mathbf{f}_\alpha(\mathbf{x}_\alpha, t) = \begin{bmatrix} -\left(\frac{R_{s_{bs}}+R_i}{L_i} + \frac{1}{\tau}\right) i_{in} - \left(\frac{1}{L_i}\right) v_{C_{bs}} + \left(\frac{1}{L_i}\right) v_i \\ -\left(\frac{R_{s_{oL}}+R_{s_{oC}}}{L_o} + \frac{1}{\tau}\right) i_{L_o} - \left(\frac{1}{L_o}\right) v_{C_o} + \left(\frac{R_{s_{oC}}}{L_o}\right) i_o \\ \left(\frac{1}{C_o}\right) i_{L_o} - \left(\frac{1}{C_o}\right) i_o \\ v_{C_o} \end{bmatrix} + \begin{bmatrix} \left(\frac{1}{\tau}\right) i_{in}^* \\ \left(\frac{1}{\tau}\right) i_{L_o}^* \\ -\dot{v}_{C_o}^* \\ -v_{C_o}^* \end{bmatrix} \quad (6.32)$$

$$\mathbf{g}_\alpha(\mathbf{x}_\alpha, t) = \begin{bmatrix} \frac{R_{s_{bs}} i_{L_o}}{L_i} \\ \frac{v_{C_{bs}} - R_{s_{bs}} i_{L_o} + R_{s_{bs}} i_{in}}{L_o} \\ 0 \\ 0 \end{bmatrix}. \quad (6.33)$$

The control objective is then to regulate the new state variables, $x_{\alpha_{1-4}}$, to zero. The tracking problem is thus

transformed into a regulation problem.

6.3.6 Switching Control Law

Once the model is prepared to apply sliding mode control, a control law is defined that will force the system to reach the sliding surface and then remain on it. The control law is then evaluated together with the sliding function to see whether the conditions for sliding mode are satisfied. The control law is defined as follows:

$$u = \begin{cases} 0, & \sigma_{\alpha} \cdot \text{sgn}(v_{C_{bs}}) \geq 0 \\ 1, & \sigma_{\alpha} \cdot \text{sgn}(v_{C_{bs}}) < 0 \end{cases}, \quad (6.34)$$

where a value of 1 corresponds to the 'on' state of the regulator, a value of 0 corresponds to the 'off' state, and $\text{sgn}()$ is the *signum* function. From the definition in Eq. 6.34, the control output will be subject to one of four scenarios:

1. If the input bus capacitor voltage is positive, then for a positive value of σ_{α} , the control law will evaluate to 0.
2. If the input bus capacitor voltage is positive, then for a negative value of σ_{α} , the control law will evaluate to 1.
3. If the input bus capacitor voltage is negative, then for a positive value of σ_{α} , the control law will evaluate to 1.
4. If the input bus capacitor voltage is negative, then for a negative value of σ_{α} , the control law will evaluate to 0.

The switching law can be explained in the following way for positive input bus values. When the voltages or currents found in the sliding function, σ_{α} , (refer to Alg. 3) are larger than their respective references, the sliding function will assume a positive value. According to the switching law presented, the control variable, u , will evaluate to 0, and the system will "buck", causing the source on the input of the regulator module to be disconnected from the output. This will eventually cause the references to become larger than their respective signals, bringing about a change of sign in σ_{α} . The control variable will then evaluate to 1, causing the source to be connected to the input again, which causes the pattern to repeat.

For the negative half of the input bus voltage, the sliding function voltage and currents are *larger* than their respective references (in amplitude) when they are *more negative*, not *more positive*, as in the previous case. These signals are *smaller* than their references when they are *less negative* than their references. The $\text{sgn}(v_{C_{bs}})$ term in the control law serves to bring about this distinction between the positive and negative half of the input bus voltage.

6.3.7 Conditions for sliding mode

The expression of the sliding function, control law, and references must be analysed in terms of the three conditions for sliding mode laid out in Section 3.2.1. If all three conditions are satisfied, then the control should be effective. The conditions will be addressed one by one as follows.

Existence Condition

The trajectories of the two substructures are directed toward the sliding line when they are close to it.

The sliding function, σ_α , will now be analysed to see if the sliding mode exists. For ease of reference, some equations derived in section 3.2.2 regarding the condition for existence of the sliding mode will be restated:

$$\underbrace{\frac{\partial V}{\partial \sigma}}_{\sigma^T} \underbrace{\frac{d\sigma}{dt}}_{\dot{\sigma}} < 0, \quad (6.35)$$

with

$$\dot{\sigma}(\mathbf{x}) = \nabla \sigma \cdot \dot{\mathbf{x}}, \quad (6.36)$$

and

$$\nabla \sigma = \left(\frac{\partial \sigma}{\partial x_1}, \dots, \frac{\partial \sigma}{\partial x_n} \right). \quad (6.37)$$

The existence condition above is applied to the sliding function of Alg. 3 where

$$\sigma^T = \sigma_\alpha \quad (6.38)$$

$$\dot{\sigma} = \dot{\sigma}_\alpha. \quad (6.39)$$

Expressing the time-derivative of the sliding function:

$$\dot{\sigma}_\alpha = \nabla \sigma_\alpha \cdot \dot{\mathbf{x}}_\alpha \quad (6.40)$$

$$= \mathbf{C}_\alpha^T (\mathbf{f}_\alpha(\mathbf{x}_\alpha, t) + \mathbf{g}_\alpha(\mathbf{x}_\alpha, t) u) \quad (6.41)$$

$$= L_{\mathbf{f}_\alpha} \sigma_\alpha(\mathbf{x}_\alpha) + L_{\mathbf{g}_\alpha} \sigma_\alpha(\mathbf{x}_\alpha) \cdot u, \quad (6.42)$$

where

$$\mathbf{C}_\alpha^T = \begin{bmatrix} \alpha_1 & \alpha_2 & \alpha_3 & \alpha_4 \end{bmatrix} \quad (6.43)$$

$$L_{\mathbf{f}_\alpha} \sigma_\alpha(\mathbf{x}_\alpha) = \mathbf{C}_\alpha^T \mathbf{f}_\alpha(\mathbf{x}_\alpha, t) \quad (6.44)$$

$$L_{\mathbf{g}_\alpha} \sigma_\alpha(\mathbf{x}_\alpha) = \mathbf{C}_\alpha^T \mathbf{g}_\alpha(\mathbf{x}_\alpha, t). \quad (6.45)$$

The condition for existence of the sliding mode (Eq. 3.8) will now be evaluated for both switching states when the input bus voltage is positive. The MVEVR is symmetrical with respect to the AC input bus voltage in terms of topology, commutation strategy, and switching law. If, therefore, existence can be proved for the positive half of the input bus voltage, the sliding mode will exist during the negative half as well.

The result of the control law, u , is then in each case substituted into the expression for $\dot{\sigma}_\alpha$, which yields an inequality in terms of the module signals, module parameters, and sliding coefficients. The sliding coefficients (α_1 , α_2 , α_3 , and α_4) must be chosen such that the inequality holds for all time.

1. For a positive value of σ_α , the control law, u , will evaluate to 0. For the sliding mode to exist in this case, $\dot{\sigma}_\alpha$ must be negative. This yields the inequality

$$\dot{\sigma}_\alpha = L_{\mathbf{f}_\alpha} \sigma_\alpha(\mathbf{x}_\alpha) < 0 \quad (6.46)$$

$$0 > L_{\mathbf{f}_\alpha} \sigma_\alpha(\mathbf{x}_\alpha) \quad (6.47)$$

$$\begin{aligned}
0 > \alpha_1 & \left(- \left(\frac{R_{sbs} + R_i}{L_i} + \frac{1}{\tau} \right) i_{in} - \left(\frac{1}{L_i} \right) v_{C_{bs}} + \left(\frac{1}{L_i} \right) v_i + \left(\frac{1}{\tau} \right) i_{in}^* \right) \\
& + \alpha_2 \left(- \left(\frac{R_{soL} + R_{soC}}{L_o} + \frac{1}{\tau} \right) i_{Lo} - \left(\frac{1}{L_o} \right) v_{C_o} + \left(\frac{R_{soC}}{L_o} \right) i_o + \left(\frac{1}{\tau} \right) i_{Lo}^* \right) \\
& + \alpha_3 \left(\left(\frac{1}{C_o} \right) i_{Lo} - \left(\frac{1}{C_o} \right) i_o - \dot{v}_{c_o}^* \right) \\
& + \alpha_4 (v_{C_o} - v_{c_o}^*). \quad (6.48)
\end{aligned}$$

2. For a negative value of σ_α , the control law, u , will evaluate to 1. For the sliding mode to exist in this case, $\dot{\sigma}_\alpha$ must be positive. Therefore

$$\dot{\sigma}_\alpha = L_{f_\alpha} \sigma_\alpha(\mathbf{x}_\alpha) + L_{g_\alpha} \sigma_\alpha(\mathbf{x}_\alpha) \geq 0 \quad (6.49)$$

$$L_{g_\alpha} \sigma_\alpha(\mathbf{x}_\alpha) \geq -L_{f_\alpha} \sigma_\alpha(\mathbf{x}_\alpha) \quad (6.50)$$

$$\begin{aligned}
& \left(\alpha_1 \left(\frac{R_{sbs} i_{Lo}}{L_i} \right) + \alpha_2 \left(\frac{v_{C_{bs}} - R_{sbs} \cdot i_{Lo} + R_{sbs} \cdot i_i}{L_o} \right) \right) \\
& \geq -\alpha_1 \left(- \left(\frac{R_{sbs} + R_i}{L_i} + \frac{1}{\tau} \right) i_{in} - \left(\frac{1}{L_i} \right) v_{C_{bs}} + \left(\frac{1}{L_i} \right) v_i + \left(\frac{1}{\tau} \right) i_{in}^* \right) \\
& - \alpha_2 \left(- \left(\frac{R_{soL} + R_{soC}}{L_o} + \frac{1}{\tau} \right) i_{Lo} - \left(\frac{1}{L_o} \right) v_{C_o} + \left(\frac{R_{soC}}{L_o} \right) i_o + \left(\frac{1}{\tau} \right) i_{Lo}^* \right) \\
& - \alpha_3 \left(\left(\frac{1}{C_o} \right) i_{Lo} - \left(\frac{1}{C_o} \right) i_o - \dot{v}_{c_o}^* \right) \\
& - \alpha_4 (v_{C_o} - v_{c_o}^*). \quad (6.51)
\end{aligned}$$

If the sliding coefficients in the above inequalities can be chosen in such a way that the inequalities always hold true in their respective cases, then sliding mode is guaranteed to exist. However, the presence of many different time varying system signals made it difficult to extract clear boundaries for the sliding coefficients. Instead of solving these equations analytically, simulations were used to analyse whether the existence condition is satisfied during the operation of the regulator.

Reachability Condition

For any initial condition, the system trajectories must reach the sliding surface within finite time.

Reachability is motivated by referring again to Figs. 6.3-6.5. As long as the control references lie in-between their respective steady-state waveforms, then the control law should be able to drive the signals towards their references from any initial condition. This will be motivated later in this chapter with simulation results.

Stability Condition

The system must remain stable when confined to, and moving along, the sliding surface.

This can be motivated by simulation by noting that none of the voltages and currents lose stability even when harsh step- and dip- manoeuvres are performed.

6.3.8 Equivalent Control

The control variable is generally found in the derivative of the switching function, as seen in Eq. 6.42. When the system is ideally constrained to the sliding manifold, then $\sigma = \dot{\sigma} = 0$. This condition can be applied to the expression of the derivative of the sliding function ($\dot{\sigma} = 0$) to obtain an expression for the control in the ideal case. This is called the equivalent control (refer to Section 3.2.4), and will be referred to as u_{eq} .

The equivalent control is expressed as:

$$u_{eq} = -\frac{L_{f\alpha} \sigma_\alpha(\mathbf{x}_\alpha)}{L_{g\alpha} \sigma_\alpha(\mathbf{x}_\alpha)} \quad (6.52)$$

$$L_{g\alpha} \sigma_\alpha(\mathbf{x}_\alpha) u_{eq} = -L_{f\alpha} \sigma_\alpha(\mathbf{x}_\alpha) \quad (6.53)$$

$$\begin{aligned} & \left(\alpha_1 \left(\frac{R_{sbs} i_{Lo}}{L_i} \right) + \alpha_2 \left(\frac{v_{Cbs} - R_{sbs} \cdot i_{Lo} + R_{sbs} \cdot i_i}{L_o} \right) \right) u_{eq} \\ &= -\alpha_1 \left(-\left(\frac{R_{sbs} + R_i}{L_i} + \frac{1}{\tau} \right) i_{in} - \left(\frac{1}{L_i} \right) v_{Cbs} + \left(\frac{1}{L_i} \right) v_i + \left(\frac{1}{\tau} \right) i_{in}^* \right) \\ & - \alpha_2 \left(-\left(\frac{R_{soL} + R_{soC}}{L_o} + \frac{1}{\tau} \right) i_{Lo} - \left(\frac{1}{L_o} \right) v_{Co} + \left(\frac{R_{soC}}{L_o} \right) i_o + \left(\frac{1}{\tau} \right) i_{Lo}^* \right) \\ & \quad - \alpha_3 \left(\left(\frac{1}{C_o} \right) i_{Lo} - \left(\frac{1}{C_o} \right) i_o - \dot{v}_{Co}^* \right). \\ & \quad - \alpha_4 (v_{Co} - v_{Co}^*) \quad (6.54) \end{aligned}$$

During sliding mode, the equivalent control takes on a continuous value between 0 and 1. In [49], this property is used as a proof for sliding mode existence. If it can be shown that the equivalent control stays within its boundaries, then the sliding mode exists (provided that the reachability condition is also satisfied). This comes down to basically the same as the existence condition. If the sliding mode exists, then, the right-hand-side of equation 6.54 should be less than or equal to $\left(\alpha_1 \left(\frac{R_{sbs} i_{Lo}}{L_i} \right) + \alpha_2 \left(\frac{v_{Cbs} - R_{sbs} \cdot i_{Lo} + R_{sbs} \cdot i_i}{L_o} \right) \right)$.

6.3.9 Existence, Reachability and Stability Motivation by Simulation

The conditions for sliding mode can be demonstrated graphically by analysing the control signals when the system is pushed close to its boundaries. This analysis is complemented by performing controls steps at the same time to really push the regulator module as close to instability as possible.

Simulation Setup

Simulations were performed (in SystemVision) where the regulator module was tested as a standalone unit. The module input voltage, which the system supplies via the autotransformer was emulated with a voltage source and added equivalent series winding resistance and equivalent leakage inductance (refer to Sec. 4.2.1). The system load was emulated as a resistive load directly over the output terminals of the module. Fig. 6.6 below shows the simulation setup, Table 6.3 shows the regulator module component values used and Table 6.3 shows the simulation parameters.

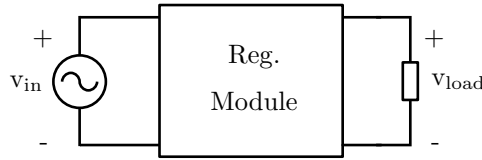


Figure 6.6: Diagram of the simulation setup.

Table 6.3: Regulator module component values for the SystemVision simulations.

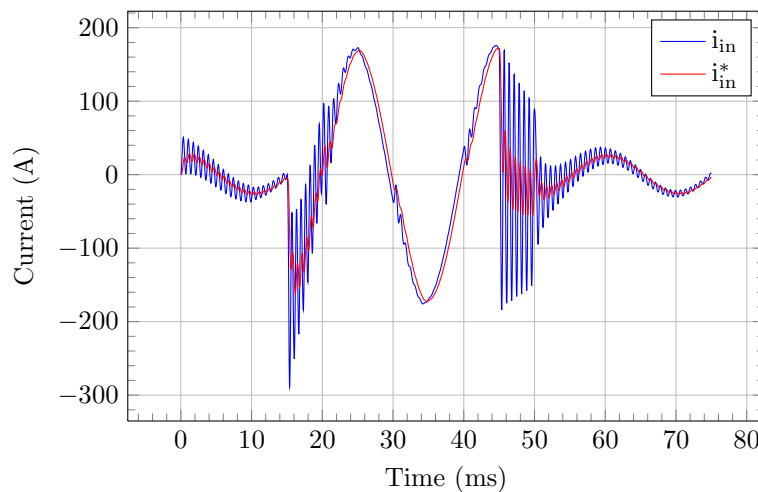
Component	Value	ESR
L_i	138.7 μH	
R_i	19 $\text{m}\Omega$	
C_b	90 μF	1 $\text{m}\Omega$
C_s	1.5 μF	24.6 $\text{m}\Omega$
L_o	750 μF	314.2 $\text{m}\Omega$
C_o	75 μF	6.67 $\text{m}\Omega$

Table 6.4: Simulation parameters for the SystemVision simulations.

Component Attribute	Time	Value
Source voltage	throughout	898.15 V_p
Load value	throughout	5 Ω
Output voltage reference amplitude	0 – 15 ms	5 V_p
Output voltage reference amplitude	15 – 45 ms	840 V_p
Output voltage reference amplitude	45 – 75 ms	5 V_p

Module Running Close to Boundaries

The system performance is most telling and interesting when stepped back and forth between its maximum and minimum performance boundaries. Simulation results are shown in Figs. 6.7-6.9. During the simulation, a reference step is performed from 5 V_p to 840 V_p . Transients are visible for the upward and downward steps and in each case the step is done on a peak, where the transients are the worst.

Figure 6.7: The module input current, i_{in} , together with its reference, i_{in}^* , is shown.

The input current in Fig. 6.7 above is seen to be marginally stable and very “ringy”. The ringing is induced by the reference steps, as well as each zero-crossing. The control system successfully guides the system to a point of greater stability as the ringing is damped until it is completely eliminated.

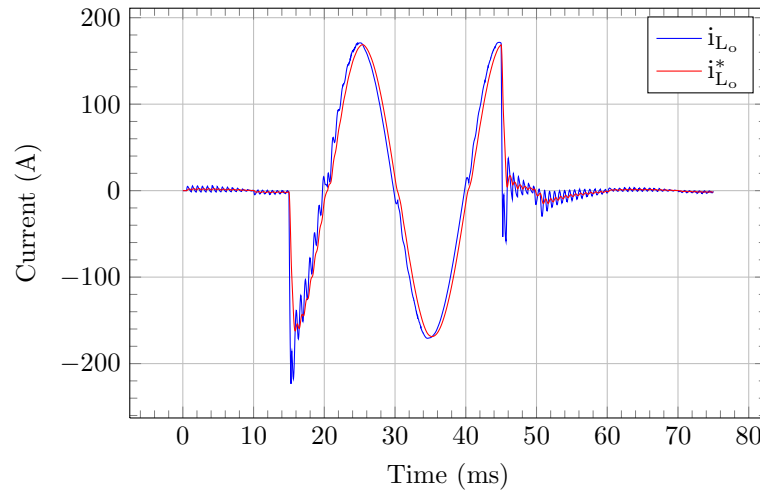


Figure 6.8: The module output filter inductor current, i_{L_o} , together with its reference, $i_{L_o}^*$, is shown.

The output filter inductor current in Fig. 6.8 is much more stable than the input current. Some ringing is observed after the reference steps, but this is controlled successfully. The ringing is more pronounced on the downward step.

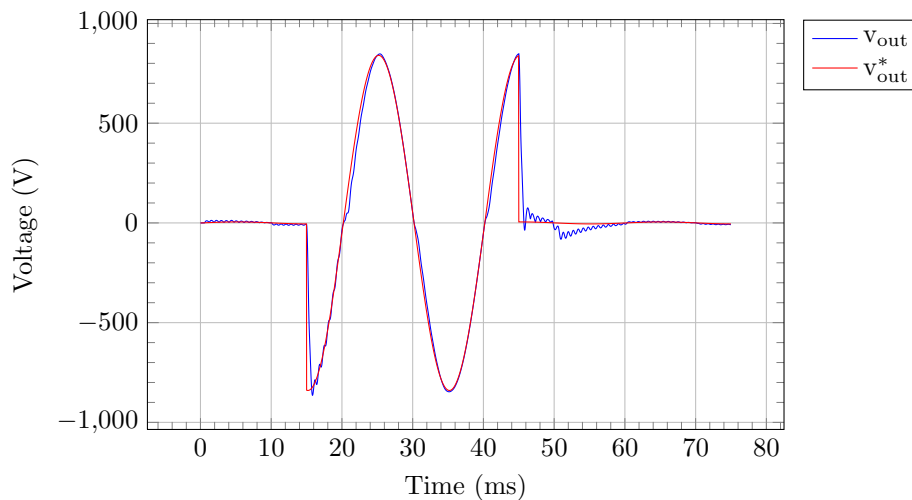


Figure 6.9: The module output voltage, v_{out} , together with its reference, v_{out}^* , is shown.

The module output voltage in Fig. 6.9 exhibits a steady state RMS error of 2.0191 V (57.1%) during the low voltage steady-state and 30.014 V (5.05%) during the high voltage steady-state. The low-reference tracking error is clearly outside of our target of less than 10% tracking error, but still within the general constraint shown in Eq. 6.7 (89%). The voltage performance shows desirable damping and reaching speeds.

Reachability Motivation

Steady-state waveforms are generated for each of the controlled voltages/currents in order to analyse reachability by simulation. This is done by creating three duplicate circuits in the simulation file. The first circuit

is constantly in the 'on' switching state, which would produce the maximum steady-state waveforms. The second circuit is constantly in the 'off' switching state, which produces the minimum steady-state waveforms. The third circuit is controlled by the SMC algorithm, producing the switching waveforms. If the references remain within the steady-state waveforms, especially when the system is pushed close to its boundaries, then the reachability condition must be satisfied.

Fig. 6.10 shows the simulation results of Figs. 6.7-6.9 for the time range where the system is in steady state, tracking its maximum reference. If the control references remain within the envelope of their respective steady-state waveforms, the condition is satisfied. For analysis purposes, the figure is divided up into four sections, A - D, each analysed in terms of the condition for reachability.

- Section A** In this section it can be seen that the sliding function, s , is clearly not constrained to zero. This means that the module is not in sliding mode, which indicates that one of the conditions for sliding mode is not satisfied. By close inspection it can be deduced that the reachability condition is not satisfied. Notice how the output voltage is running on its maximum ($V_{out_{on}}$), and how both the input current reference, i_{in}^* and the output filter inductor current reference, $i_{L_o}^*$ are outside of their steady state boundary envelopes. This means that the control system has no possible way of reaching its references. The reachability condition is therefore not satisfied.
- Section B** In this section it can be seen that the system is in sliding mode, as the sliding function evaluates to zero. The input current reference, i_{in}^* , the output filter inductor current reference, $i_{L_o}^*$ and the output voltage reference, v_{out}^* are all inside of their respective steady state boundary envelopes. A noticeable distortion pulls the output voltage away from its reference. This is due to the phase shift between the current references and the currents themselves and the necessary condition that the sliding function must be zero. The non-ideal current references produce a skewing of the sliding function. The control action nevertheless forces the sliding function to zero, and it distorts the output voltage in order to achieve this.
- Section C** This section is the symmetrical counterpart of section A. The reachability condition is not satisfied, because the current references - due to the inherent phase delay of the LPFs - are outside of their steady state envelopes.
- Section D** Section D is the symmetrical counterpart of section B. The reachability condition is satisfied, but due to the phase shift in the current references, the output voltage is distorted.

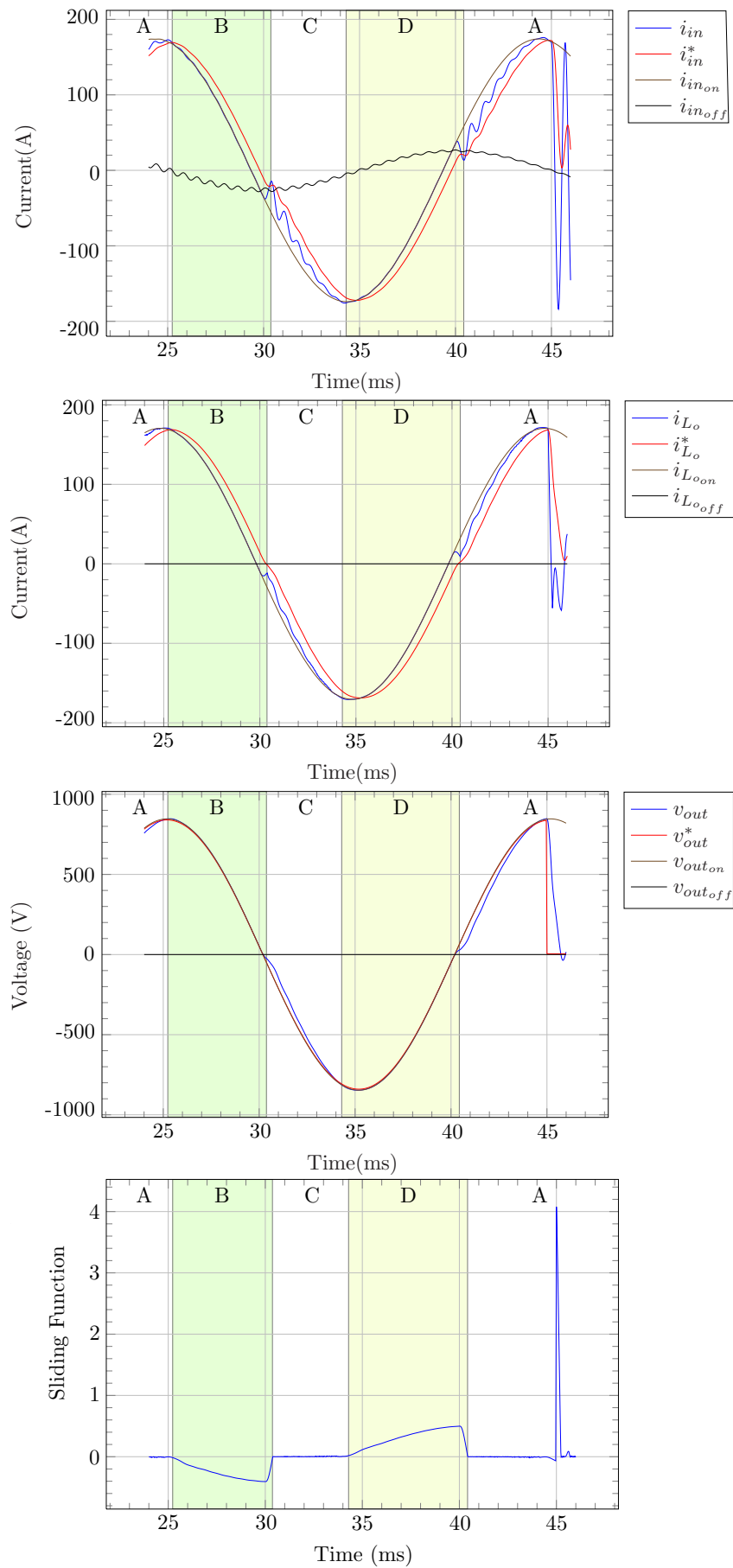


Figure 6.10: This figure demonstrates the problems related to reachability with references close to the maximum. The output voltage reference is set to $840V_p$.

It is seen from the analysis above that the reachability condition is satisfied at times, and at times it is not, depending on the position of the current references with respect to their steady-state waveforms. The areas of non-reachability are largest when the module is required to run close to its maximum limits. As the system output voltage reference is lowered, the reachability region improves greatly. Fig. 6.11 below shows, for example, that the reachability performance is greatly improved at a reference of 700V_p .

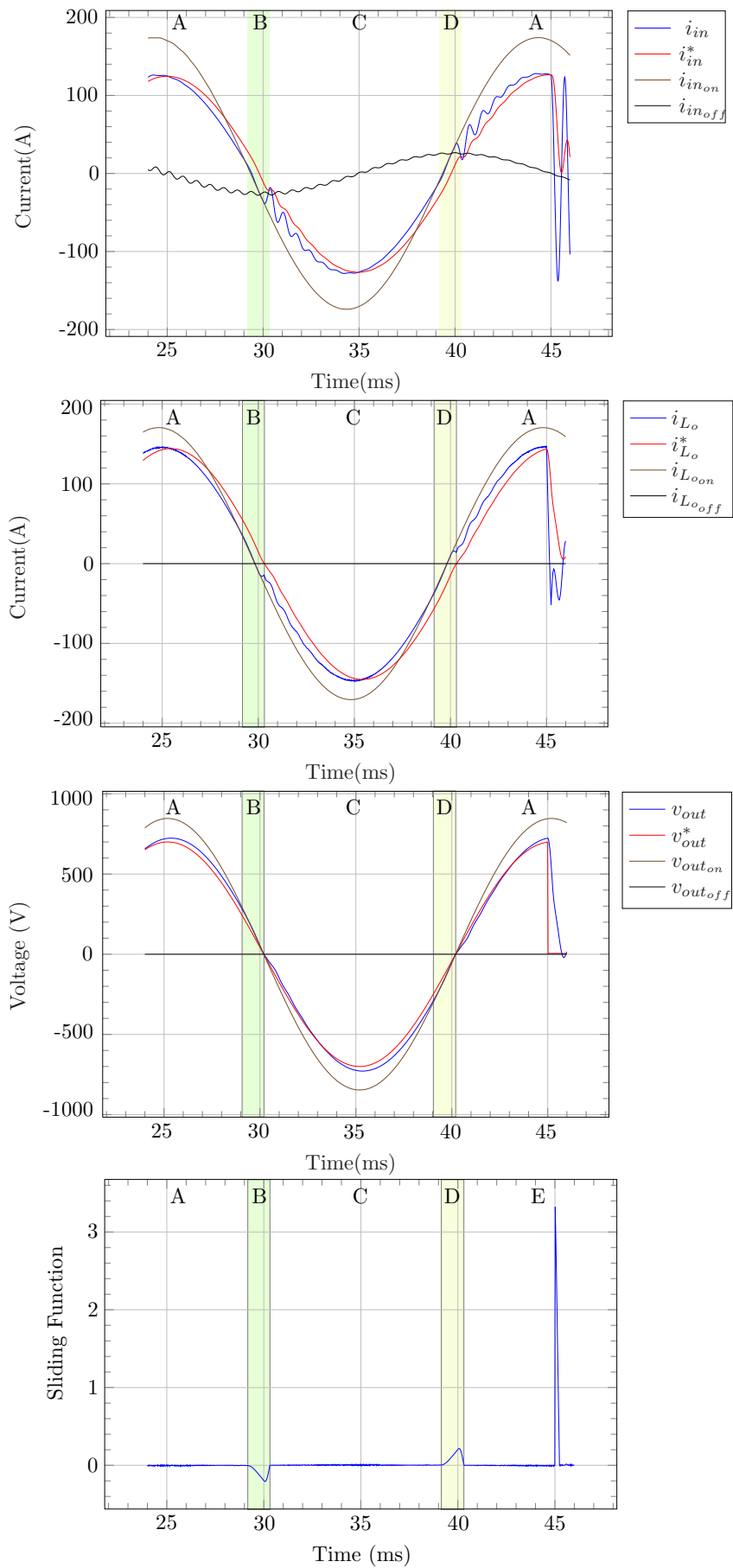


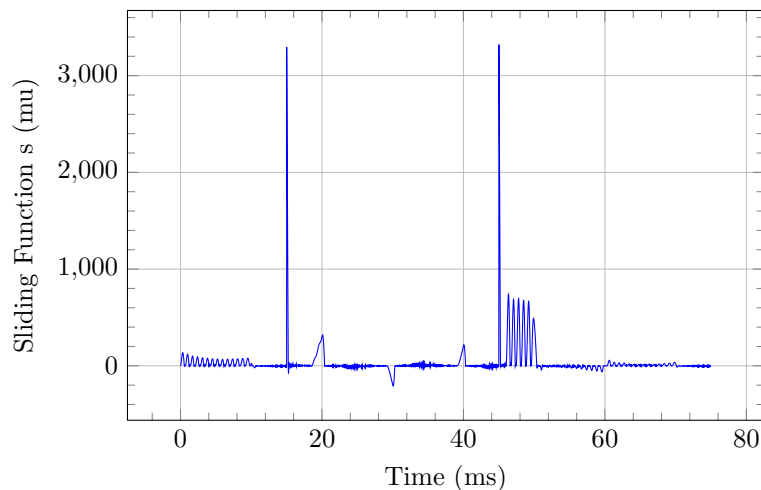
Figure 6.11: Reachability is improved as the output voltage reference amplitude lowers. The output voltage reference is set to $700V_p$.

Existence Motivation

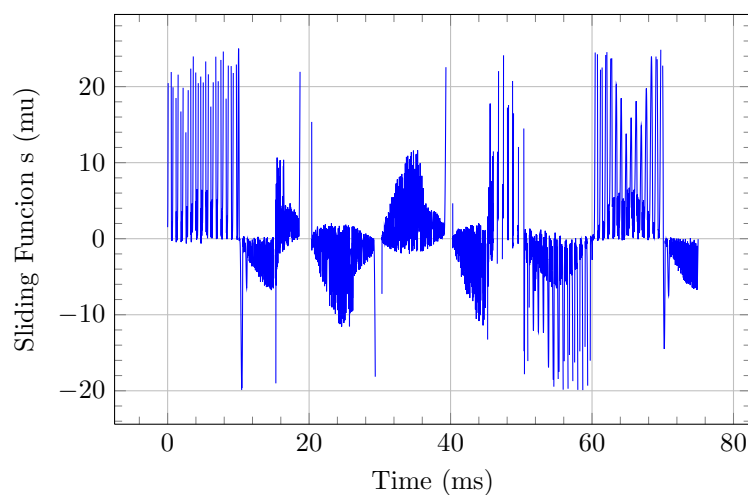
The existence condition requires that, for the given control law, the sliding function will always move towards zero. This behaviour is described by the following equation:

$$\sigma \cdot \dot{\sigma} < 0. \quad (6.55)$$

Eq. 6.55 requires a negative and positive gradient, when the sliding function is positive and negative respectively. This condition will be analysed with the assumption that the reachability condition is satisfied. The simulation results for a reference of $700V_P$ will therefore be used (as shown in Fig. 6.11), because the reachability condition is mostly satisfied. The magnified sliding function of Fig. 6.11 is shown in Fig. 6.12. In the area of existence, the sliding function will ideally be constrained to zero in the ideal case. In this simulation many factors are ideal, like zero dead time, and there is no explicit constraint on the switching frequency in the switching law. The simulation does, however, have a fixed time step of $1\mu s$ which effectively limits the switching frequency. Therefore it will be seen that in the region of existence, the switching function will be constrained to a region *around* zero.



(a)



(b)

Figure 6.12: The sliding function, s , is shown in (a), with a zoomed in view showed in (b). This simulation run corresponds to Figs. 6.7-6.9.

When the system undergoes a transient, such as during the first reference step (15 ms), for example, it moves outside of the region of existence. As the system recovers from the transient (and specifically the ringing of the input current), it moves in and out of the region of existence. This behaviour is shown more clearly in Fig. 6.13. While the existence condition is satisfied, the system is rapidly switching, as can be seen in the rapid changes of the control variable, u . When the system leaves the region of existence, the control action is ineffective in constraining the sliding function to zero. Eventually, the system returns to sliding mode existence and the cycle repeats. Importantly, the areas of non-existence become smaller and smaller, which show that even though the system will not always be in sliding mode, the control law is nevertheless able to guide the system back to the area of existence.

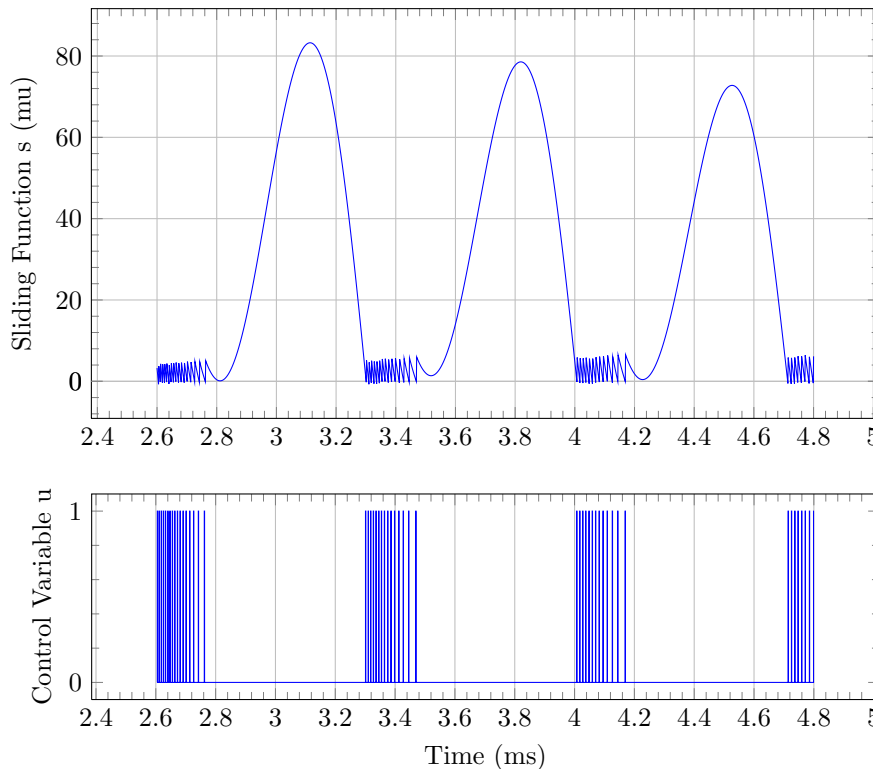


Figure 6.13: Zoomed in area of the sliding function, s together with the switching function, u , corresponding to Figs. 6.7-6.9.

After the transients have settled, the system reaches steady-state and then remains in the area of sliding mode existence. The control law constrains the sliding function to a region around zero (Fig. 6.14). Whenever the discrete simulation finds the sliding function away from zero (where the first sample dot crosses the zero line), it immediately switches in order to produce a movement back towards zero.

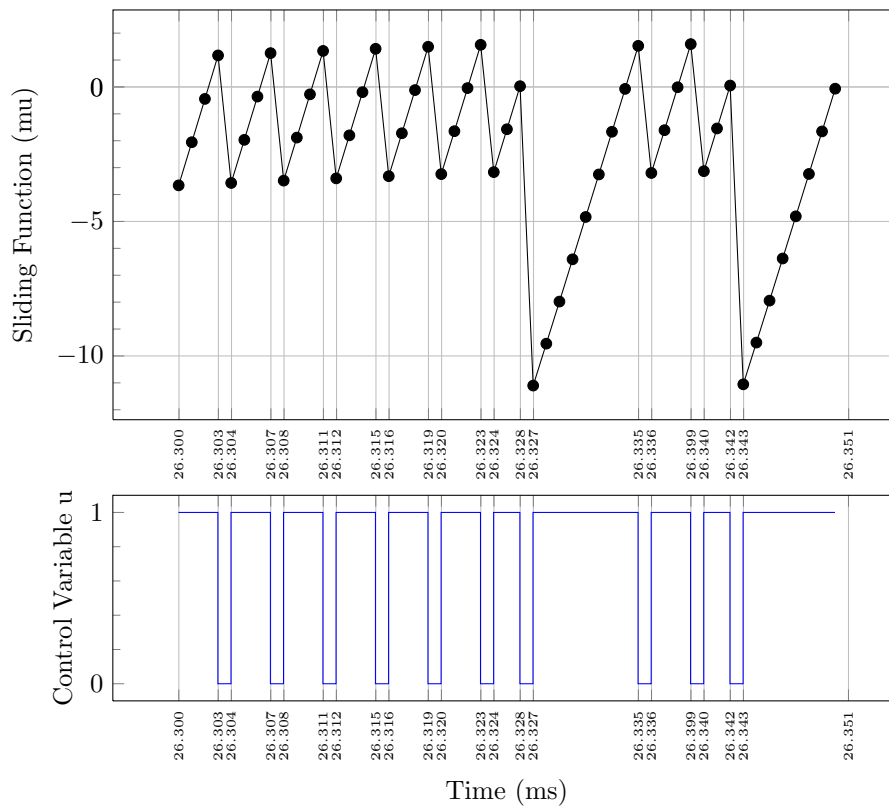


Figure 6.14: Zoomed in area of the sliding function, s together with the switching function, u , corresponding to Figs. 6.7-6.9.

Stability Motivation

From Figs. 6.7-6.9 it is clear that - even under the most challenging demands - the voltages and current remain stable. Even though the ringing is excessive at times, control is maintained and the ringing is gradually reduced and eliminated. This is not a trivial observation, as the system stability is not easily maintained. Stability on the (inherently oscillatory) input bus and the output bus is maintained by the same set of switching transistors used for voltage regulation.

6.3.10 Modifications for QSMC

The above simulations were all performed while assuming an ideal control law, expressed as

$$u = \begin{cases} 1 & , \sigma \cdot \text{sgn}(V_{in}) < 0 \\ 0 & , \sigma \cdot \text{sgn}(V_{in}) > 0 \end{cases} . \quad (6.56)$$

This switching law can however not be implemented as it is impossible to switch at an infinite frequency. The processing unit requires finite time to calculate the switching state, and the power transistors require a certain amount of dead time for safe switching operation. Rapid switching also lead to increased switching losses and the heat generated in the power transistors could lead to burn-out.

Thus, it was decided to limit the switching frequency to 10kHz by using a triangle waveform to modulate the switching function.

Modulation Signal

One of the common techniques of fixing the switching frequency (refer to Section 3.2.10) is to use a PWM scheme. A modulation signal with adaptive amplitude was designed to maintain control resolution for a wide range of sliding function magnitudes. It is undesirable for the amplitude of the modulated signal to become larger than the modulation waveform, as this would cause course control action to force the signal back into the bounds of the modulation signal. Furthermore, if the modulation waveforms amplitude is fixed at a value which is too large for some parameter states, then the deviation from zero would be larger than is necessary. Control over a large range of sliding function amplitudes therefore calls for an adaptive modulation signal.

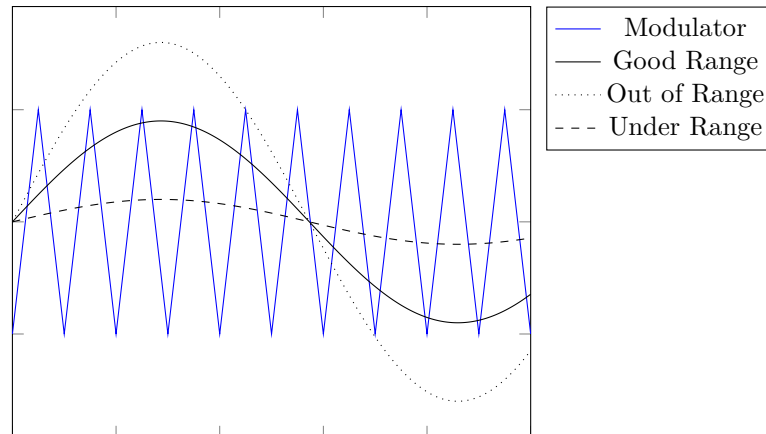


Figure 6.15: When the amplitude of the modulated signal is out of proportion to the modulator, a loss in control resolution ensues.

Adapted Switching Law

The switching law was adapted for QSMC to the following:

$$u = \begin{cases} 1 & , \sigma \cdot \text{sgn}(v_{in}) < m \\ 0 & , \sigma \cdot \text{sgn}(v_{in}) > m \end{cases}, \quad (6.57)$$

where m is the modulation signal, and $\text{sgn}(v_{in})$ is the signum function applied to the module input bus voltage. It is seen that, according to this new law, the switches' action is determined by the value of the sliding function relative to the value of the modulator (as opposed to to zero).

The final VHDL implementation of the adaptive modulator is shown in the code listing below. Firstly, the modulator amplitude is restricted to the predefined maximum value, *modHeight_max*. Secondly, the modulator amplitude tracks the low-pass filtered¹ sliding function amplitude if the modulator amplitude is smaller. Lastly, the modulator amplitude is made to decay toward a falling sliding function amplitude by subtracting a constant from the modulator amplitude on every rising clock edge. The adaptive amplitude is then used to scale the triangle wave with unity amplitude.

Listing 6.1: VHDL implementation of APWM

```

1 dynamicModShape : process is
2 begin
3   wait until rising_edge(clk);
4   --restrict modulator height to max value

```

¹The sliding function was low-pass filtered with a first order filter with cutoff frequency of 15kHz. This is to

```

5  if abs(S_lpf) > modHeight_max then
6      modHeight <= modHeight_max;
7      --adapt the mod. amplitude to the sliding f. ampl.
8  elseif abs(S_lpf) > modHeight then
9      modHeight <= resize(abs(S_lpf), modHeight);
10     --fast decay towards falling sliding f. ampl.
11     else
12         modHeight <= resize(
13             modHeight - to_sfixed(0.000315, modHeight),
14             modHeight
15         );
16     end if;
17
18     modulator <= resize(modHeight_sat*mod_10kHz, modulator);
19 end process;

```

6.3.11 Simulations of QSMC

The ideal simulations were adapted for quasi sliding mode control (QSM) in the following ways:

1. adding $2\mu s$ dead time to switching
2. fixing the switching frequency to 100kHz by modulation with an adaptive PWM modulator.

Other than the two changes mentioned, the simulation setup was kept identical to above ideal reference step from $50V_p$ to $840V_p$ and back. The resulting waveforms for the controlled voltages and currents are shown below in Figs. 6.16-6.18.

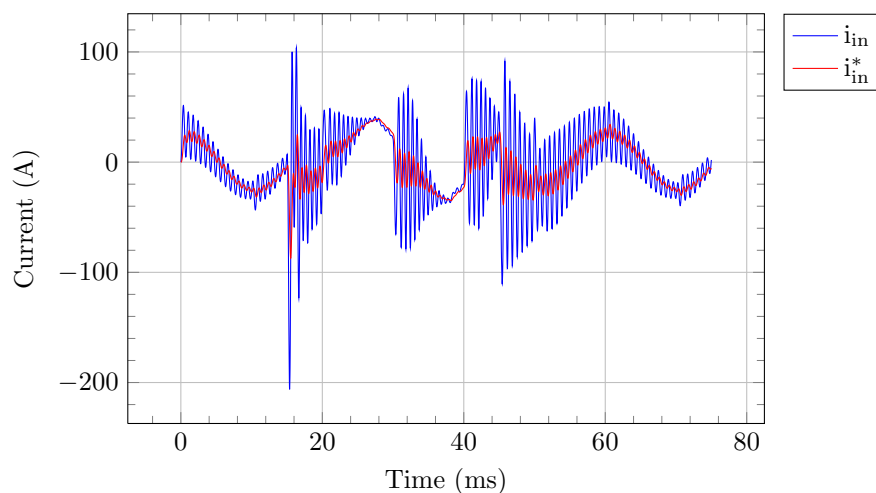


Figure 6.16: The non-ideal module input current, i_{in} , together with its reference, i_{in}^* , is shown.

The input current in Fig. 6.16 is seen to be even more ringy than in the ideal case. The ringing is induced by the reference steps, as well as each zero-crossing of the output/input voltage. At the zero crossing, the voltage regulator has no control energy, as no voltage can be added to the output, which causes the system to momentarily lose control and deviate from its references. The control system successfully guides the system back to a point of greater stability as the ringing is damped until it is completely eliminated at some points.

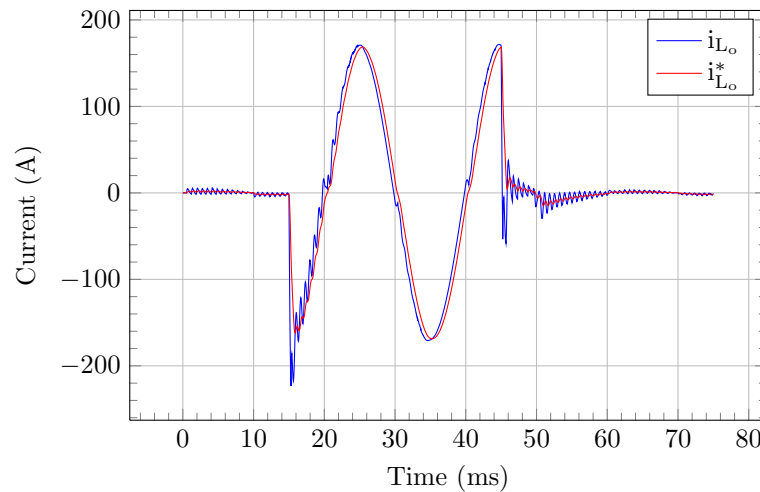


Figure 6.17: The non-ideal module output filter inductor current, i_{L_o} , together with its reference, $i_{L_o}^*$, is shown.

The output filter inductor current in Fig. 6.17 is much more stable than the input current. Although some ringing is observed after the reference steps, this is controlled successfully. The ringing is more pronounced on the downward step because the output voltage amplitude and output filter inductor current magnitudes are relatively small in comparison to the input current magnitude (which always has a component flowing through the input bus capacitor) for low output references. The control weights were tuned to maintain optimal control of the input current at higher references which results in the deterioration of the input current stability at lower references. This problem can possibly be overcome by implementing gain scheduling.

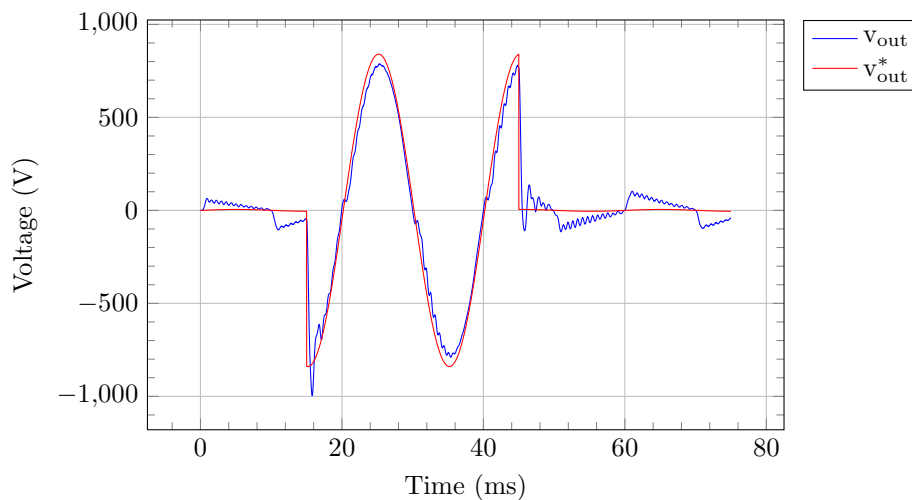


Figure 6.18: The non-ideal module output voltage, v_{out} , together with its reference, v_{out}^* , is shown.

The module output voltage is shown in Fig. 6.18 above. The overshoot is slightly increased from the ideal case and the wave exhibits some distortions due to the ringy input current. The low-amplitude reference tracking is poor and the resulting waveform is distorted. This is mainly because the ringy input current is dominating the transfer function. Once again, this problem could possibly be avoided by implementing gain scheduling on the sliding coefficients.

QSMC switching action

The switching action for QSMC differs from ideal SMC. The waveforms for the sliding function, adaptive modulation signal, and the control variable is shown below in Fig. 6.19. It can be seen that the sliding function, s , is constrained to a region close to zero, instead of zero itself, as was the case with the ideal SMC. The two high spikes in the sliding function correspond to the reference steps where the instantaneous errors are large.

The triangular modulation wave, m , is seen to adapt its amplitude according to the maximum value of the sliding function. This is to maintain control resolution.

The control variable, u , acts according to Eq. 6.57.

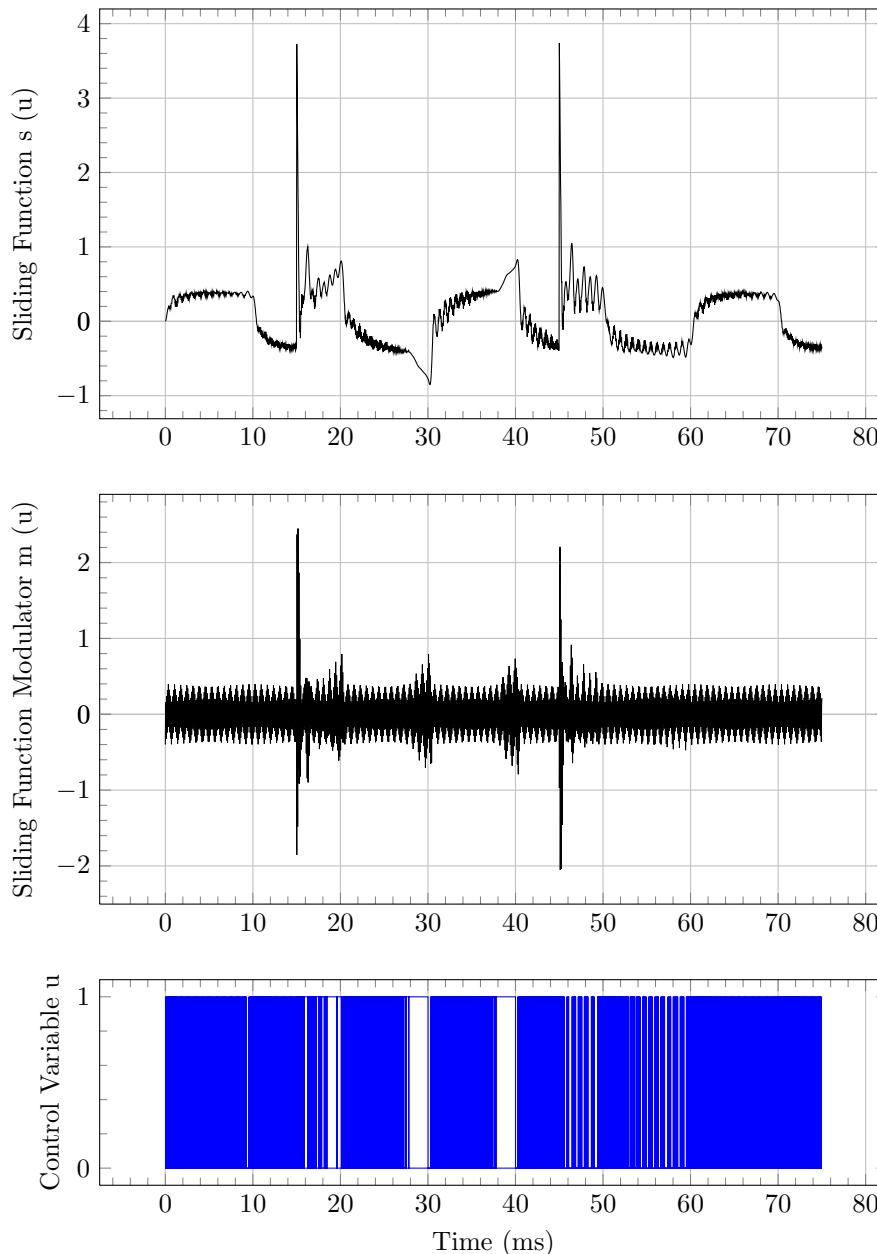


Figure 6.19: QSMC switching signals corresponding to Figs. 6.16-6.18. The sliding function (top) is seen to be constrained to an area near zero and some large peaks are observed at the moment of the reference steps. The adaptive modulation signal is shown (middle) and is adapting its magnitude to fit the sliding function. The control variable (bottom) reflects the switching action. The areas of prolonged constant state is mostly indicative of non-reachability.

A zoomed in portion of the QSMC signals are shown in Fig. 6.20. The module switches when the sliding function crosses the modulation frequency. This causes, contrary to the ideal case, the switching to happen at a point that is not necessarily zero, although close to zero.

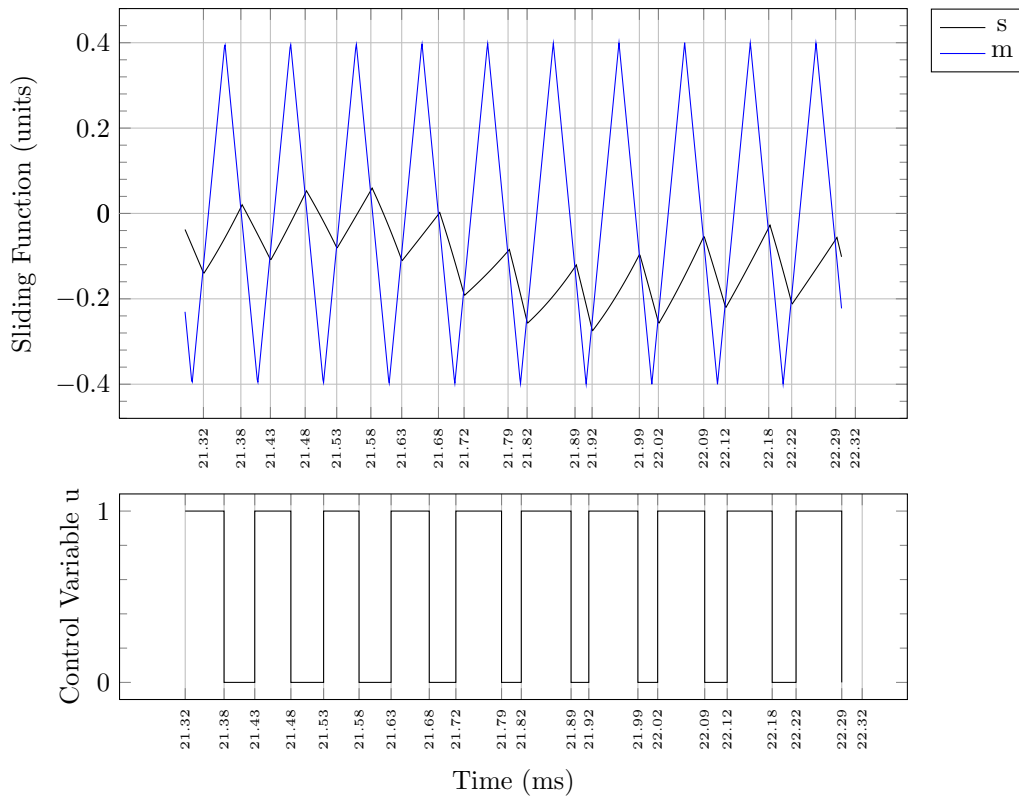


Figure 6.20: Zoomed in QSMC switching signals. The sliding function (top) is shown to be constrained to a region *near* to zero. The control variable (bottom) reflects the switching action, which is constrained to a fixed frequency of 10kHz.

6.3.12 Analysis of Robustness

In order to best gauge the performance with regard to robustness, a sensitivity analysis of the RMS value of the sliding function² was done with respect to 300% variations in the main system components. SystemVision does 12 simulation runs while varying component parameters. The results are shown in Fig. 6.21 and the simulation component values and simulation parameters are shown in Tables 6.5 and 6.6 respectively.

²The RMS value of the sliding function gives an indication of the overall control performance with respect to the references. If the RMS value is small, the system RP is constrained close to the sliding surface (good performance). If the RMS value is large, the system RP deviates far from the sliding surface (bad performance).

Table 6.5: Regulator module component values for the SystemVision sensitivity simulation.

Component	Value	ESR
L_i	138.7 μ H	
R_i	19 m Ω	
C_b	90 μ F	1 m Ω
C_s	1.5 μ F	24.6 m Ω
L_o	750 μ F	314.2 m Ω
C_o	75 μ F	6.67 m Ω
R_l	15 Ω	
L_l	15 mH	

Table 6.6: Simulation parameters for the SystemVision sensitivity simulation.

Component Attribute	Time	Value
Source voltage	throughout	898.15 V _p
Load value	throughout	15 + j4.71 Ω
Output voltage reference amplitude	throughout	840 V _p

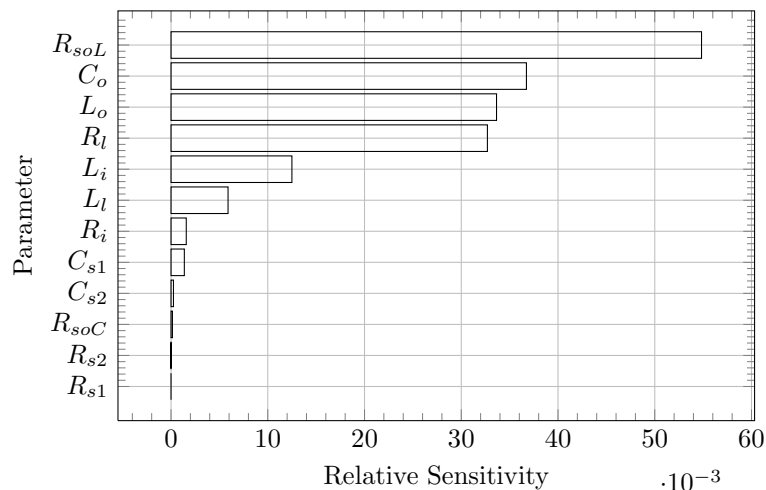


Figure 6.21: Sensitivity analysis for the circuit, with 300% variance on each component.

From Fig. 6.21 it can be seen that the circuit is most sensitive to variations in the parasitic resistance of the output filter capacitor, R_{soC} , the inductance of the output filter inductor, L_o , the capacitance of the output filter capacitor, C_o , and the load resistance, R_l . The circuit is seen to be fairly insensitive to the input inductance, L_i , the load inductance, L_l , and the input resistance, R_i . The sensitivity most of the above components are not a problem, as they can be manufactured and procured according to specification, and their values are not expected to change over their life cycle. The load and input impedance is expected to change and the system must be robust with respect to it. Robustness with respect to the load resistance is therefore of greatest concern, as the circuit is relatively sensitive to it.

To further analyse the system's robustness with respect to load variations, a load sweep was performed where the load resistance was swept between 5 Ω and 25 Ω and the load inductance was swept from 5 mH to 25 mH. The best-case performance was obtained with the resistive component at 25 Ω and the inductance at 5 mH (load has small phase), and the worst case was with the resistive component at 5 Ω and the inductance at

25 mH (load has large phase). The output voltages and reference for these two extremes are shown in Fig. 6.22. The RMS tracking error for the best-case waveform is 50.010 V (8.42% error) and the RMS error between the reference and the worst-case waveform is 72.356 V (12.18% error). An intermediate load of 10 Ω and 10 mH exhibits an RMS error of 58.396 V (9.83% error).

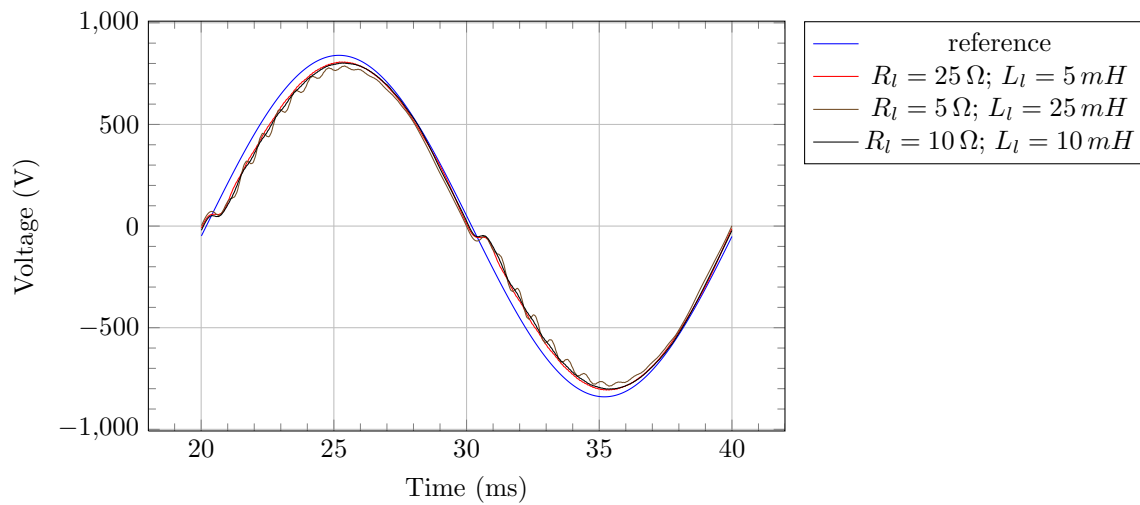


Figure 6.22: Module output voltages compared to reference with the best-case performance ($R_l = 25 \Omega, L_l = 5 \text{ mH}$) and worst-case performance ($R_l = 5 \Omega, L_l = 25 \text{ mH}$) and intermediate ($R_l = 10 \Omega, L_l = 10 \text{ mH}$).

The tracking error requirement consequently puts a constraint on the allowable load variation. For a tracking error of under 10%, the RMS tracking error must be less than 59.4 V. Fig. 6.23 was populated with the results of an array of load sweep done by simulation. The allowable loads fall under the region where e_{RMS} is less than 59.4 V. The allowable range of variation for the most sensitive parameters can thus be determined.

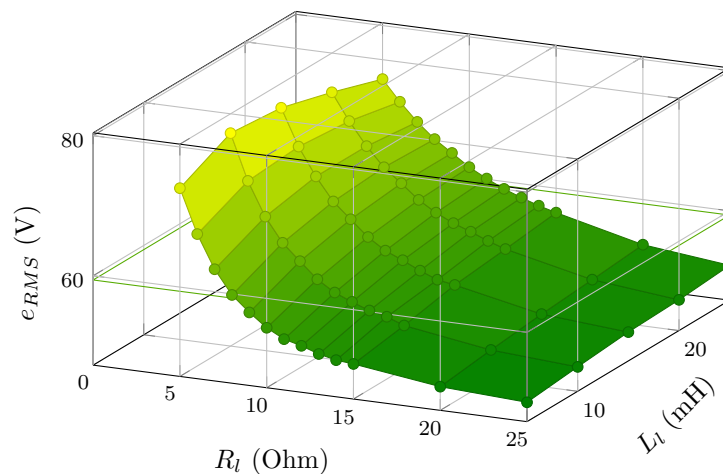


Figure 6.23: RMS tracking error for an array of reactive load values.

6.4 Summary

In this section, the design of the sliding-mode control on module level was presented. In Section 6.2, the control problem was framed, and the system level and module level control objectives were clarified.

The modular SMC design was presented in Section 6.3. Two sliding mode algorithms were developed and evaluated, after which algorithm Sigma-Alpha was chosen. Even though the conditions for sliding mode

could not be proven mathematically, a graphical analysis approach was developed as motivation instead. From this analysis, the main concern was that the conditions for reachability are broken at times due the phase delay between the controlled currents and the corresponding references. It was shown, however, that for the greater part of the regulation range, the conditions for sliding mode are satisfied for the greatest part of the system operation. When sliding mode is lost, like during zero-crossings, the switching law eventually brings the system back to sliding mode.

The modifications required for fixing the switching frequency were detailed in Section 6.3.10, where a novel adaptive modulation signal was presented.

Lastly, a method for determining the allowable range of variation in the most sensitive parameters was developed.

In the following chapter, the measured system results will be shown to compare favourably to the simulation results.

CHAPTER 7

RESULTS AND DISCUSSION

“However beautiful the strategy, you should occasionally look at the results. ”

- Winston Churchill

The main goal of this thesis is the development of robust control of the MVEVR. This chapter will therefore discuss the results related to closed loop control.

Closed loop control was attempted both with and without waveform correction. The waveform correction attempts to condition the output voltage waveform as much as possible to cancel out harmonics present in the input voltage. Waveform correction was later abandoned due to stability concerns, and amplitude regulation was done instead. The results for both are included nonetheless to give the reader insight into the control problem.

After the waveform correction results are discussed, the amplitude regulation results are presented for a single standalone regulator module, then for two modules working together. The chapter ends off with control results on system level.

7.1 Module Level Closed Loop Control Performance with Waveform Correction

In this section, various tests are presented to measure the system’s ability to do waveform correction or harmonic suppression. Firstly the test setup is detailed, after which test results on various control aspects, such as voltage tracking, current capability, transient response, and robustness, are presented.

7.1.1 Test Setup and Control Parameters

The test setup was done by treating a single regulator module as a stand-alone unit. The laboratory variac was connected directly to the regulator module’s input terminals, which would usually be connected to one of the secondary windings of the transformer. This is a 400V variac, which unfortunately limits the amplitude of the input voltage to 400V for these tests. A load was connected directly across the regulator module’s output terminals, which would usually be connected in series with the other module, the input voltage, and the load (refer to Fig. 6.1). In order to generate a load step, a contactor was used to include or exclude part of the load from the circuit. Fig. 7.1 illustrates the test setup used.

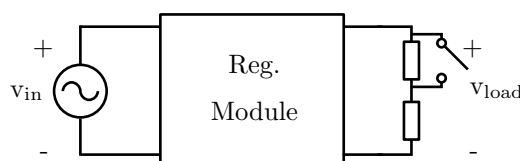


Figure 7.1: Test setup used for the single regulator module.

A sinusoidal output voltage reference was used to test the module, except where the voltage tracking performance was tested. The sinusoidal reference is generated by use of a lookup table with values appropriate for a clean sinusoid. In the case of the voltage tracking test, another lookup table was generated to produce a signal with added harmonics to the sinusoid.

7.1.2 Reference Voltage Tracking

In order to perform proper voltage regulation on system level, each module will have to inject half of the difference of the error between the system output voltage reference and the system input voltage (refer to Eq. 6.2). Voltage tracking of an arbitrary function up to the maximum required bandwidth is therefore required in each regulator module. In Fig. 7.2, a reference is generated with harmonics up to the order twenty, with amplitudes five times higher than the levels specified in the NRS 048-2 specification of 2003.[2]

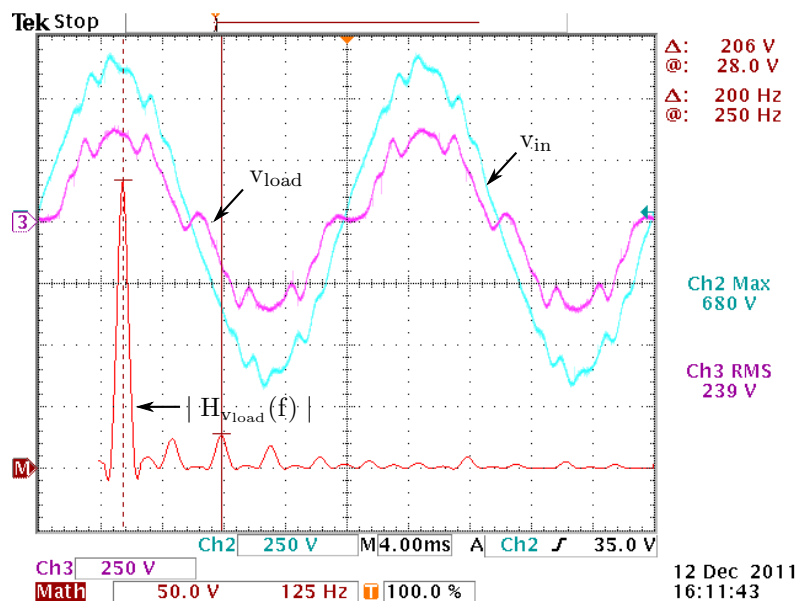


Figure 7.2: Voltage tracking of a “dirty” reference.

In Fig. 7.2, an FFT ($|H_{V_{load}}(f)|$) of the output voltage (v_{load}) is shown. The large fundamental 50 Hz component as well as the amplitude of the various harmonics can be seen.

Signaltap data was used to show the correspondence of the ADC measured output voltage to its reference. This is shown in Fig. 7.3. The output voltage is seen to track the reference well, except in a small region around the zero-crossing of the input voltage. This is expected, because when the input voltage is zero, no control energy is available.

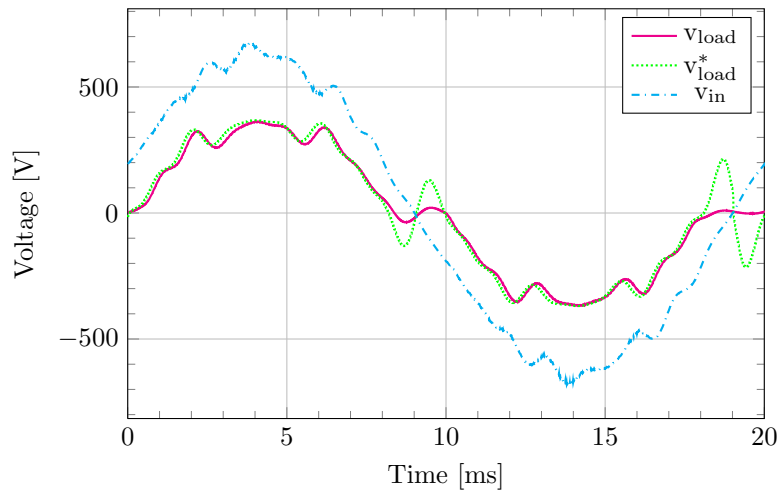


Figure 7.3: Voltage tracking of a “dirty” reference, reference included.

It was shown in Section 6.3.1 that, for a system-level output voltage tracking error of 1 %, a tracking error of about 10% is required for each of the regulator modules. In order to quantify the voltage tracking performance of the above sample, the instantaneous absolute tracking error (IATE) was calculated as shown in Eq. 7.1.

$$IATE = \left| \frac{V_{load} - V_{load}^*}{V_{load}^*} \right| \quad (7.1)$$

The resulting IATE corresponding to Fig. 7.3 is shown in Fig. 7.4. It is obvious that the IATE is enormous in the regions of time corresponding to the zero-crossing of the output voltage reference, V_{load}^* . This would necessarily cause the IATE to become very large (division by zero). This is also around the uncontrollable region, as previously mentioned. The high IATE at multiples of 10ms will therefore be ignored.

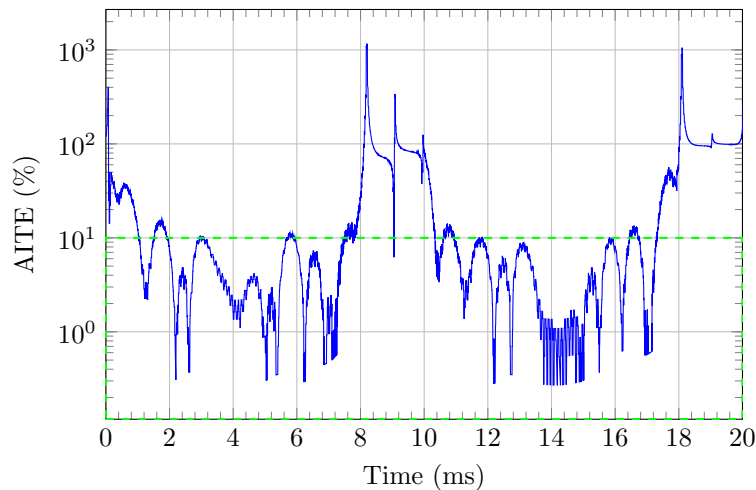


Figure 7.4: Instantaneous absolute tracking error in percentage.

Upon closer inspection, it is seen that, apart from the uncontrollable regions, the IATE is mostly within the 10 % target. It is seen that the module can successfully generate the harmonics required to cancel out harmonics found in badly distorted input signals, with a maximum instantaneous absolute tracking error of 15 %.

7.1.3 High Current Capability

Fig. 7.5 shows that the MVEVR regulator modules can carry currents up to 80 A. The value of the inductor current (i_L) is seen to be above 80 A, while the input voltage (v_{in}) is chopped from 424 V to 375 V on the output (v_{load}).

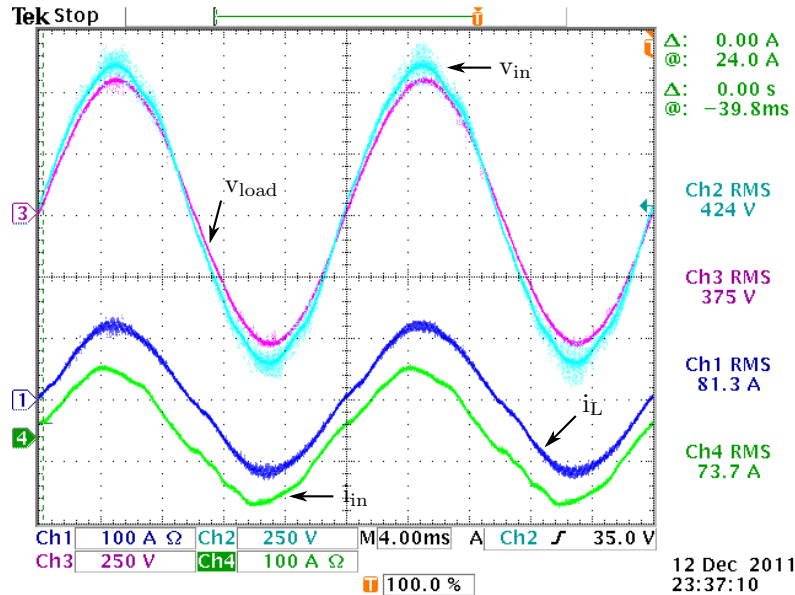


Figure 7.5: Current handling capability with a 50 Hz sinusoidal reference.

7.1.4 Transient Response to Reference Steps

A reference step of 150 V was induced to test the transient response of the voltages and currents. This is shown in Fig. 7.6. The voltage response (v_{load}) is seen to be fast with no overshoot. The input current (i_{in}) and inductor current (i_L) response show significant overshoot, but the response quickly returns to steady-state behaviour. A slight oscillation is induced on the input current. This is successfully damped by the control scheme in about 4 ms.

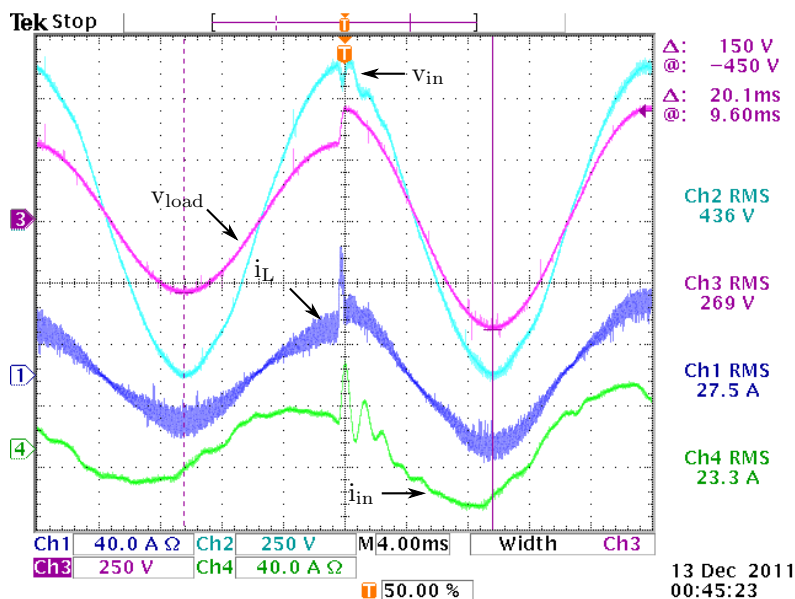


Figure 7.6: Transient response to a 150 V_p reference step.

7.1.5 Robustness with respect to Load Variations

The load step was done at an output voltage of $380\text{ V}_{\text{rms}}$. The load was stepped from $9.5\ \Omega$ to $4.75\ \Omega$. In Fig. 7.7, the output filter inductor current (i_L) is seen to increase from 62 A_p to 136 A_p within 1 ms with no overshoot. There is a slight transient on the output voltage (v_{load}), but it recovers to its steady-state value within 2 ms . Also note that the load step caused no voltage tracking error. Good robustness with respect to load variation is observed.

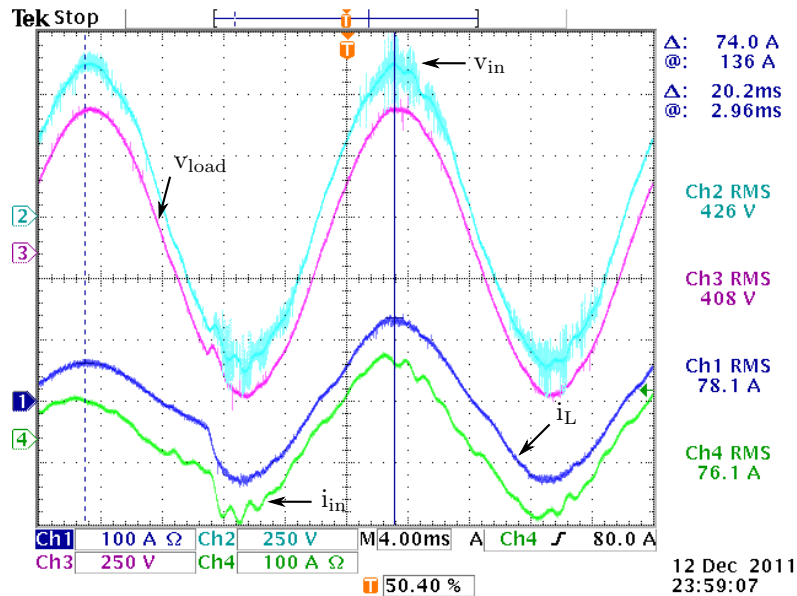


Figure 7.7: Voltage and current response to a 50 % load step.

7.1.6 Current Limiting

Current limiting was implemented by saturating the inductor current reference at a pre-defined limit, and drastically increasing the weight of the inductor current error in the sliding function once this limit has been reached. The effect is not a hard limit, but more of a current suppression, as the other terms in the sliding function still make a contribution. This is advantageous in that the system suppresses the current without losing all consideration for stability of the input current as well as the form of the output voltage. The inductor current limit is not seen as a primary responsibility of the control algorithm. The control algorithm takes a more holistic approach in terms of system stability and output quality as well as current limiting to a reasonable degree. This leaves the primary responsibility of current limiting to the protection mechanisms.

For the purposes of testing, current limiting was set to activate at 80 A_p . The currents before current limiting is shown in Fig. 7.8. The resulting load voltage (v_{load}) is clean and sinusoidal, and module inductor current (i_L) is normal and undistorted. The currents with current limiting enabled is shown in Fig. 7.9. The inductor current is seen to flatten off on the peaks after the current limiting threshold (blue horizontal lines) are crossed. The current limiting can also be observed on the flattened tops of the module input current (i_{in}).

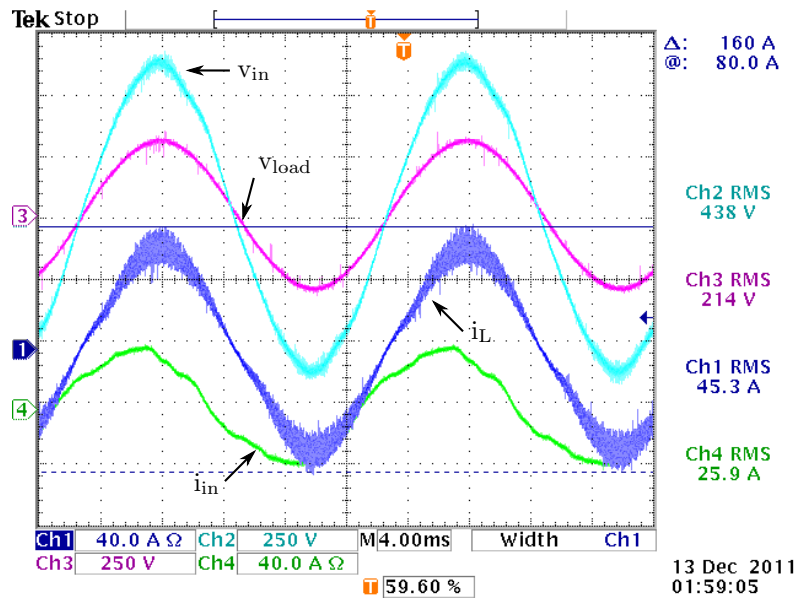


Figure 7.8: Voltages and currents are normal with current limiting not active.

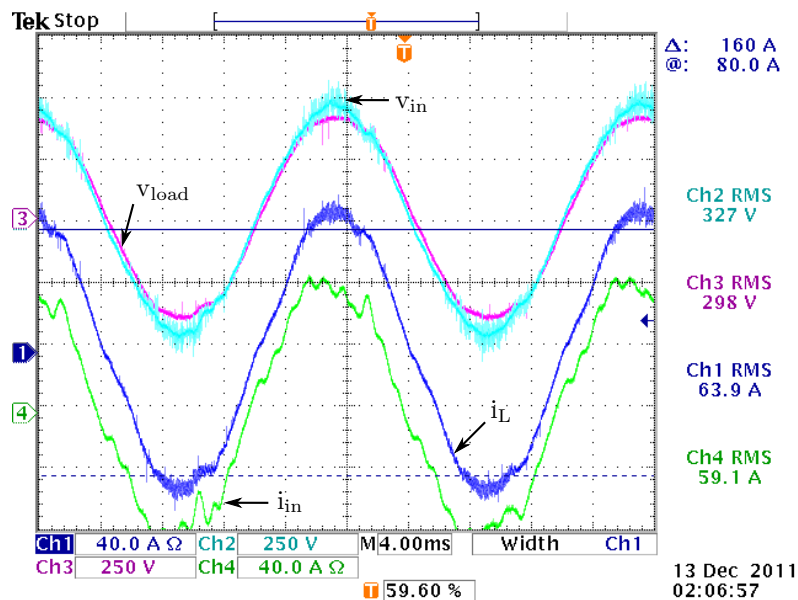


Figure 7.9: The currents are limited to a degree. The output voltage waveform is necessarily distorted as a result.

7.1.7 Stability Concerns

The above results are all very stable. However, once the RMS value of the input voltage with dirty output reference exceeded 350V, serious instability on the input bus were observed. The approach was therefore abandoned in favour of simple amplitude regulation. More work can be done to try and achieve stability with waveform correction at full rated voltage.

7.2 Module Level Closed Loop Amplitude Control Performance

The aim of the system is to regulate the system output voltage to a target RMS value. This is done by feeding sinusoidal references to the regulator modules with amplitudes such that the addition of these sinusoids to the input voltage will result in the correct RMS output voltage.

In order to test the closed loop control performance on module level, a test setup was done which treated the module as a stand-alone unit. A voltage source was connected across the module input and a load was connected over the module output. Various networks of resistors and contactors were used to perform source steps and load steps on the module. This setup is illustrated in Fig. 7.10.

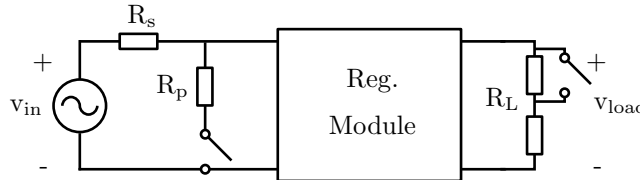


Figure 7.10: Module stand-alone test setup to test module-level control performance.

In order to achieve the source-step, R_s in Fig. 7.10 was chosen as $1\ \Omega$ and R_p was chosen as $5\ \Omega$ in order to provide for a 20% drop in the source voltage when the contactor is closed and the regulator is operating at full output voltage. At the same time the input current had to be kept close to 70 A to stay within the rating of the variac. With some nodal analysis and loop analysis, expressions can be found for the voltage over the regulator input for (1) when the contactor on the input side is open, and (2) when the contactor is closed:

$$V_{reg1} = \frac{R_L}{R_s + \frac{R_L}{D}} V_{in} \quad (7.2)$$

$$V_{reg2} = \frac{\frac{R_p \frac{R_L}{D}}{R_p + \frac{R_L}{D}}}{R_s + \frac{R_p \frac{R_L}{D}}{R_p + \frac{R_L}{D}}} V_{in}, \quad (7.3)$$

where D is the equivalent duty cycle of the regulator module, and R_L is the impedance of the resistive load.

In order to achieve the load-step, R_L could be stepped from $15\ \Omega$ to $5\ \Omega$ by shorting out two-thirds of the component resistors with a contactor.

7.2.1 Sigma-Alpha Reference Steps

Reference steps on the module output voltage reference were done on a high-impedance load ($15\ \Omega$) and a low-impedance load ($5\ \Omega$) with both upward and downward reference steps on each. In each case, the transient response is seen to include a varying measure of overshoot or undershoot and some ringing. The transient settles within a quarter 50Hz period and the resulting steady-state tracking error is within the 10% specification. The system remains consistently stable. The results are shown in Figs. 7.12 to 7.14.

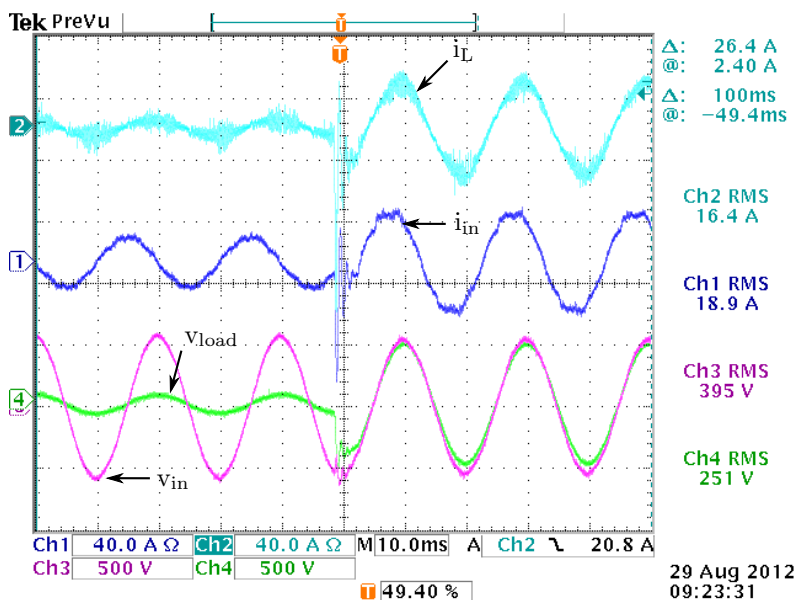


Figure 7.11: Upward reference step on sigma-alpha with 15 Ω load.

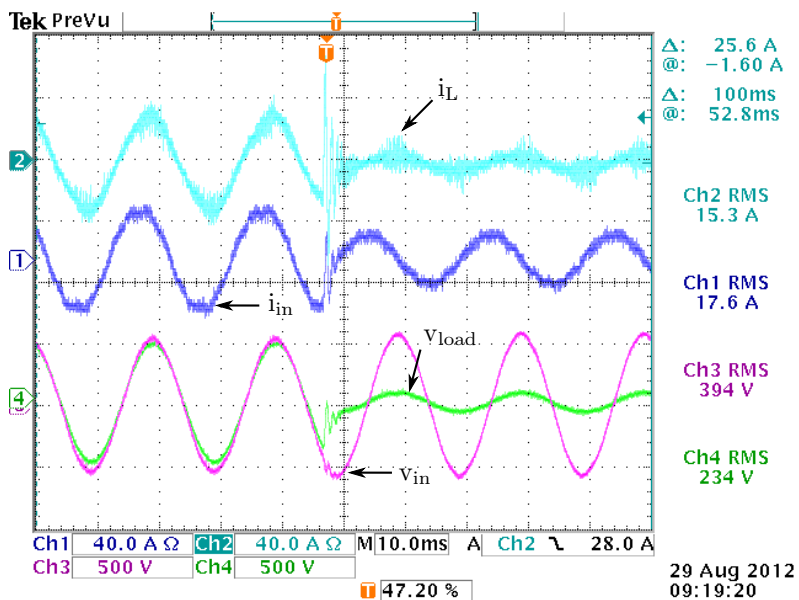
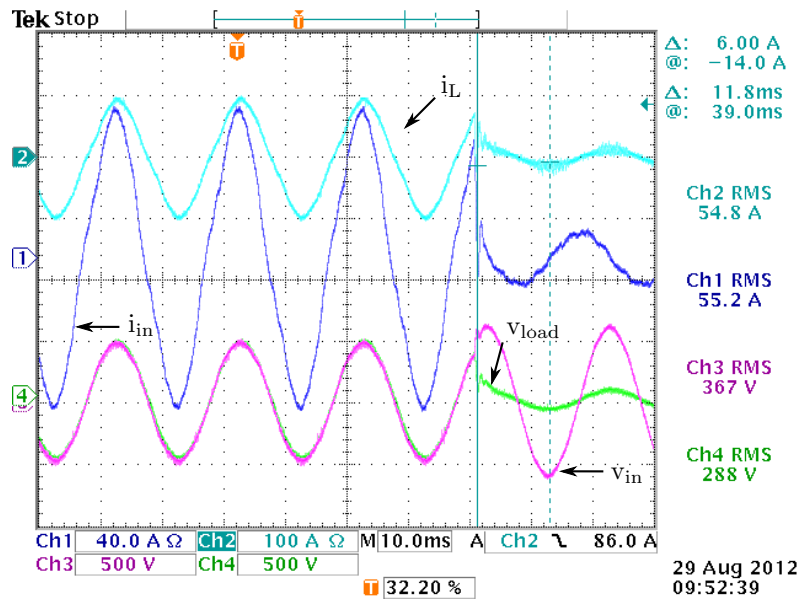
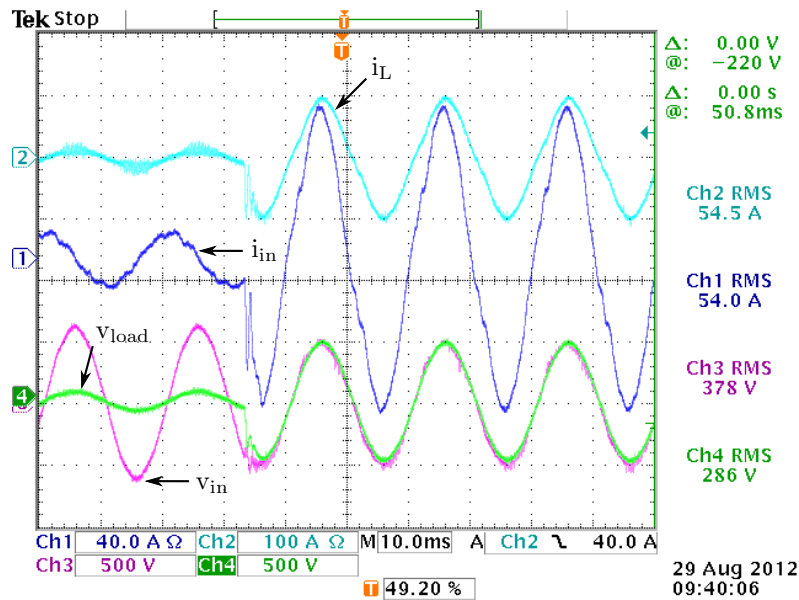
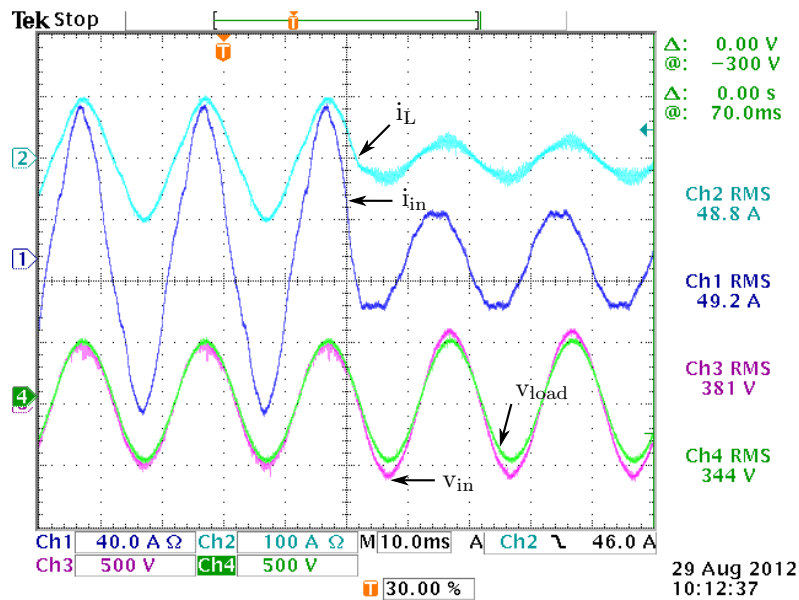
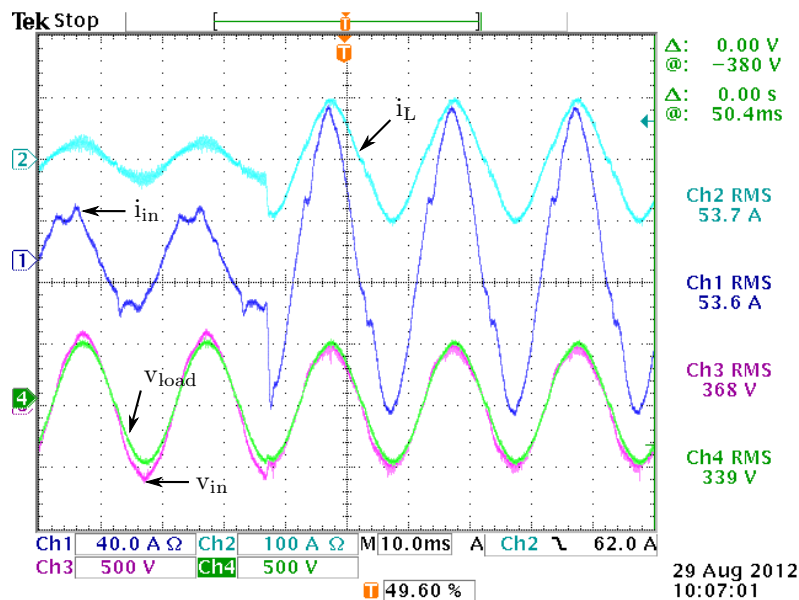


Figure 7.12: Downward reference step on sigma-alpha with 15 Ω load.

Figure 7.13: Downward reference step on sigma-alpha with $5\ \Omega$ load.Figure 7.14: Upward reference step on sigma-alpha with $5\ \Omega$ load.

7.2.2 Sigma-Alpha Load Steps

One of the crucial requirements of the control system is robustness with respect to load variations. In order to test this performance, a load step was performed where the load was stepped to a third of its value to the minimum load. The load step was between $5\ \Omega$ and $15\ \Omega$, in both directions, on the maximum voltage that the 400V variac could yield. The results are shown in Figs. 7.15 and 7.16. As the load is stepped down, the currents are seen to increase, and as the load is stepped up, the currents are seen to decrease. In both cases, the module output voltages (green) is seen to remain completely undisturbed by the load perturbation.

Figure 7.15: Load step from 5 Ω to 15 Ω .Figure 7.16: Load step from 15 Ω to 5 Ω .

7.2.3 Sigma-Alpha Source Steps

It is important that the module output voltage be invariant to dips in the input voltage as this is what the system is designed to compensate for. Input steps were generated by switching a resistive voltage divider in and out with a contactor. The supply was stepped from to 410 V to 324 V and back with a 15 Ω load and an output voltage reference of 250 V. The 5 Ω load required too much current from the supply and exceeded the supply rating. From the results in Fig. 7.17 to 7.18, it is seen that when the module input voltage (purple) dips, the module output voltage remains unchanged with no visible disturbance at all.

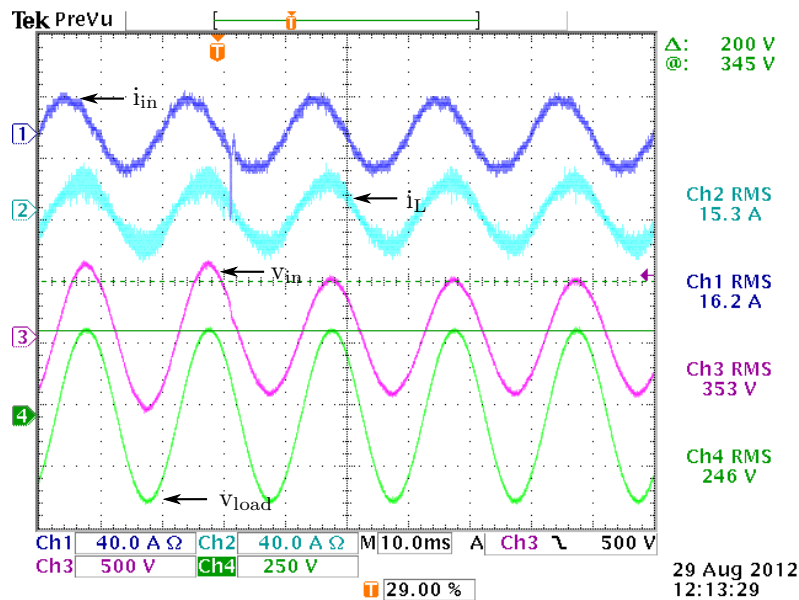


Figure 7.17: Source step from 410 V to 324 V.

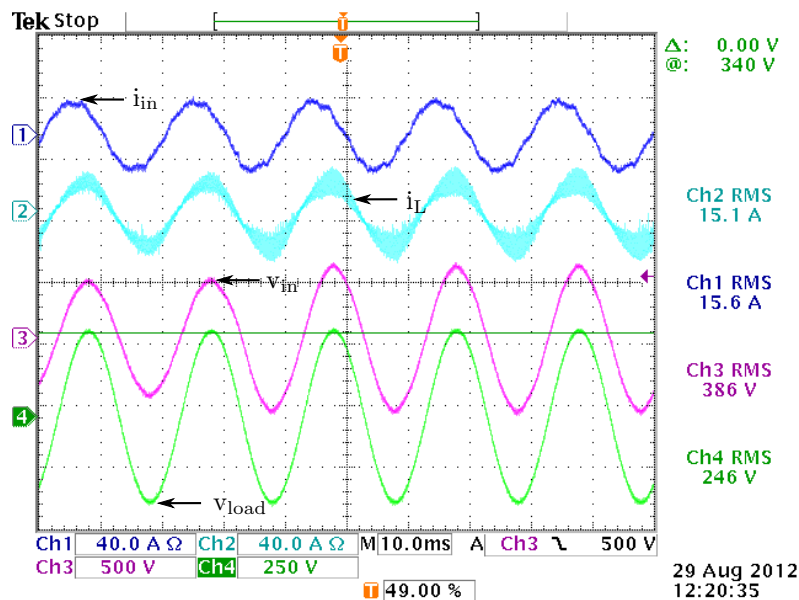


Figure 7.18: Source step from 324 V to 410 V.

7.2.4 Sigma-Alpha operating with a non-linear load

In this test, the module performance on a non-linear load was tested. This is seen as a type of load perturbation, as the relationship between the output voltage and current is no longer linear. A rectifier load was connected to the module along with a $15\ \Omega$ load. The capacitance of the rectifier capacitor was $15.6\ \text{mF}$.

From the results in Fig. 7.19 the non-linear relationship between the output voltage (green) and the output filter inductor current (cyan) is clearly seen. The distorted current that is drawn from the load cause harmonics to be reflected on the input voltage of the regulator (magenta). Nevertheless, the regulator does a fair job of achieving its design purpose of regulating the output voltage. The reference voltage was $250\ \text{V}$, whereas a voltage of $240\ \text{V}$ was reached. This is well within the 10% error specification for the module output.

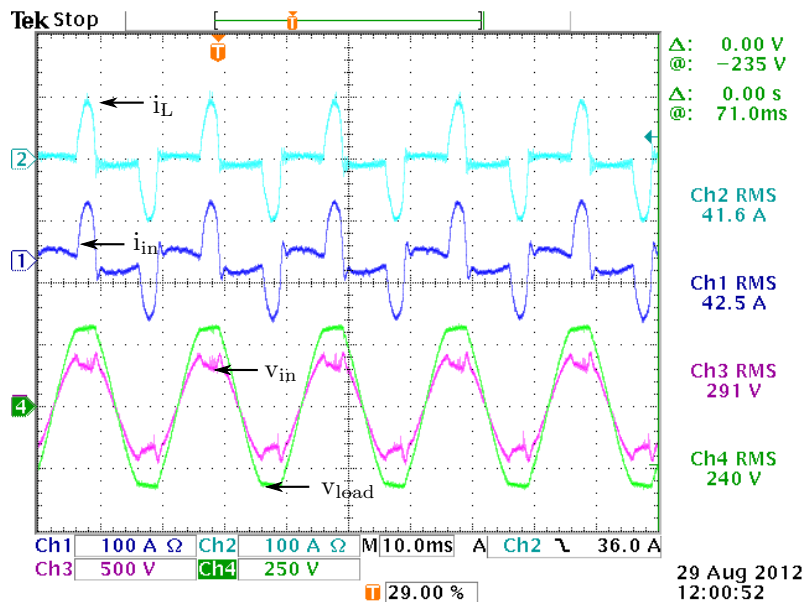


Figure 7.19: Sigma-Alpha running on a rectifier load.

7.3 Closed Loop Control Performance with Module Interaction

In this test setup, the working of the series stacked configuration of the modules were tested. The tests were done with an alternate set of transformers to avoid the high system voltages, while still keeping the voltages across the regulator modules near to rated values.

As shown in Fig. 7.20, two step-up transformers, each with winding ratio 260:420 were used to power the modules. Each module was powered from one of the transformer secondaries, while the lab variac was connected across both of the primaries in parallel.

Two different loads were used, depending on the output current required. A light indoor load was used for low currents, while a heavy-duty external load was used for higher currents.

For input voltage steps, a resistive divider was built and connected in-between the variac and the transformer primaries. The parallel resistor could be bypassed with a contactor to eliminate the most significant voltage drop. Load steps were done both on the small and the large load. The input voltage was also varied at constant output voltage reference to determine effective the range of regulation. The output loop was measured to demonstrate that the voltages add up as expected of the series-stacked configuration.

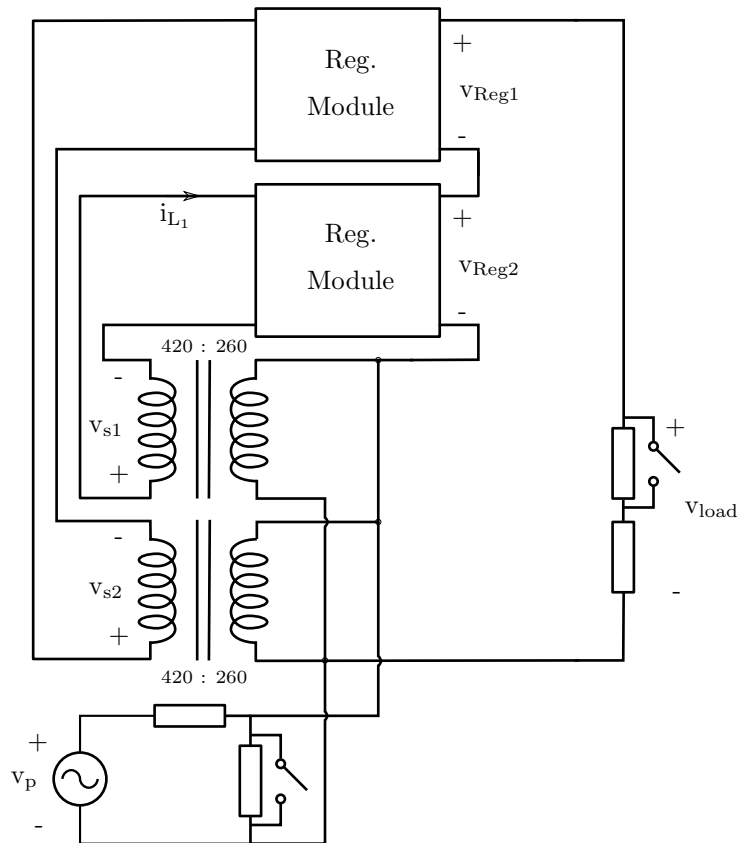


Figure 7.20: Test setup used to test the system performance.

7.3.1 Steady-State Regulation

With the modular series-stacked topology it is clear that the output voltage (v_{load}) is equal to the input voltage (v_p) in addition to the output voltages (v_{Reg1} and v_{Reg2}) of the two regulator units. The latter two dynamically adapt to ensure the correct output voltage. This is shown in Fig. 7.21.

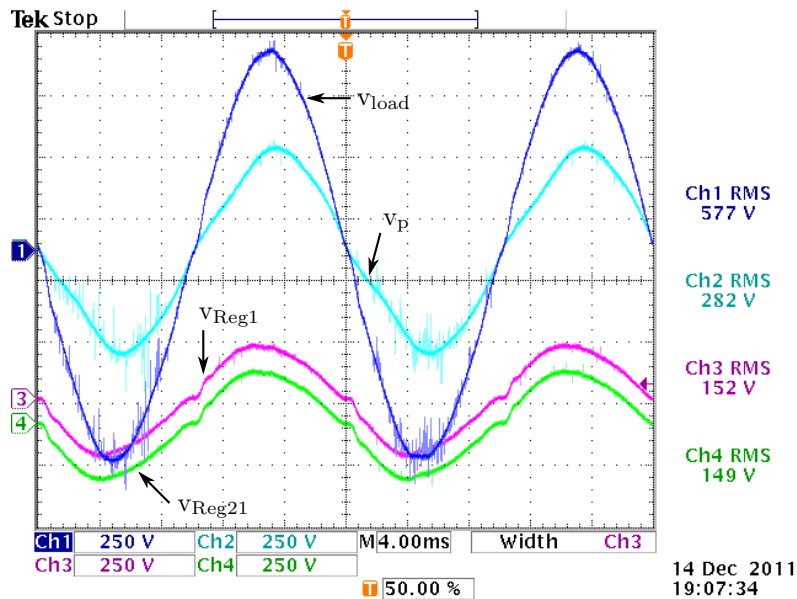


Figure 7.21: The regulator voltages, v_{Reg1} and v_{Reg2} , together with the primary voltage, v_p , add up to the load voltage, v_{load} . A small error is seen due to probe calibration difficulties.

7.3.2 Robustness with respect to Input Voltage Variations (i.e. disturbance rejection)

The system's response to a step on the input voltage might very well be the most revealing test in demonstration of the system's performance. Fig. 7.22 shows a sudden dip in the input voltage (v_p) amplitude. The output voltage (v_{load}) is seen to remain remarkably stable and with constant amplitude. The input current to module 1 (i_{i1}) and the output filter inductor current of module 1 (i_{L1}) is also seen to remain stable throughout.

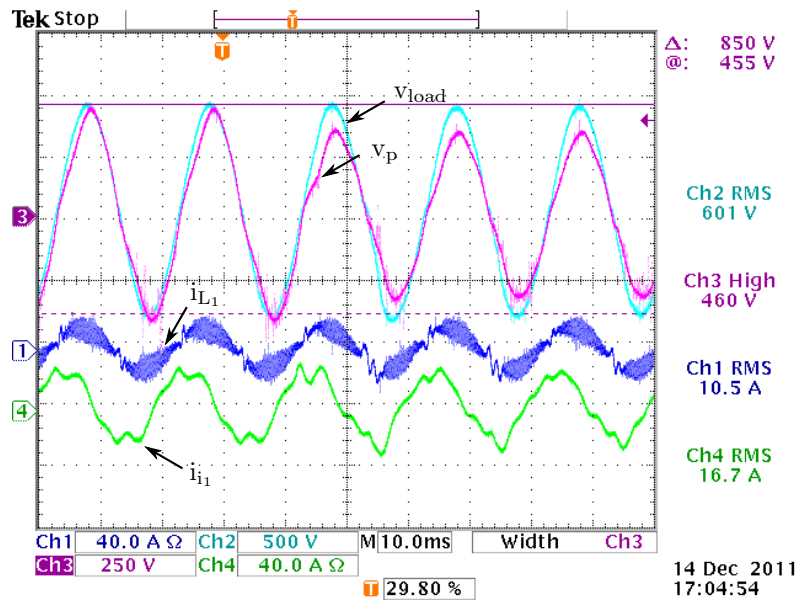


Figure 7.22: An input voltage drop was generated, of which the current and voltage response is shown.

Load Step at High Current

The control system was designed to be robust with respect to load perturbations. A 50% load step was performed to test this. Fig. 7.23 shows a load step from a smaller (13 Ω) to a larger (26 Ω) load impedance. The load current (i_{load}) is seen to suddenly decrease as a result of this. Hardly any effect is observed on the output voltage waveform (v_{load}).

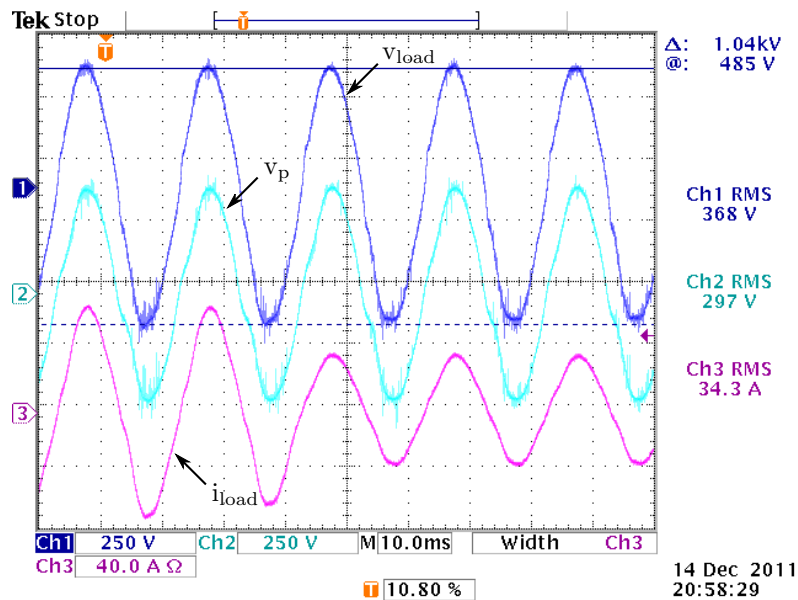


Figure 7.23: Transient response of the system input voltage, load voltage, and load current after a load step (step up) at high current.

Another load step was done from a larger (26Ω) to a smaller (13Ω) load impedance. This is shown in Fig. 7.24. As expected, the load current suddenly rises. This time, the load step occurred very close to the peak of the load current, and even then, no significant effect is seen on the output voltage waveform. The system is seen to be robust with respect to load changes.

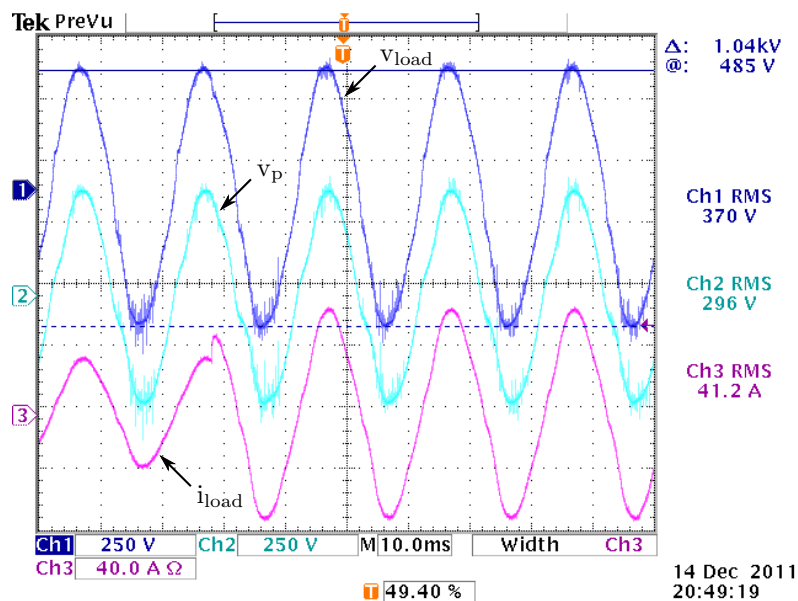


Figure 7.24: Transient response of the system input voltage, load voltage, and load current after a load step (step down) at high current.

7.4 System Level Control Performance

In this section, results will be shown and discussed for top-level system performance. Tests were done at the full rated voltage by using 400:12700 V step up and step down transformers.

7.4.1 Test Setup

The laboratory test setup is shown in Fig. 7.25. It can be seen how the step up and step down transformers were used to generate the required test voltages from the 400 V supply. The step down transformer was required to stay within the voltage rating of the available load. The MVEVR block is seen to consist of the autotransformer and the two regulator modules.

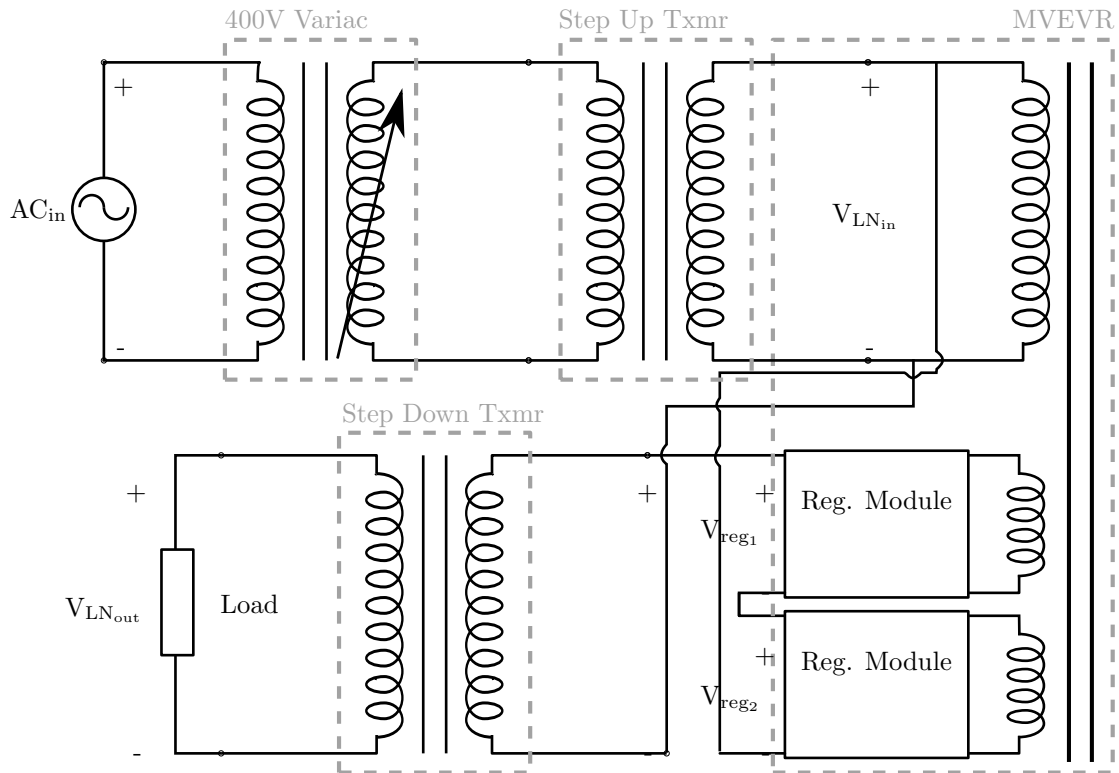


Figure 7.25: Test setup used to test the system performance.

7.4.2 Test Results

The system test results are shown below in Figs. 7.26-7.28.

Firstly, in Figs. 7.26 and 7.27, the regulation ability of the system is shown to be successful with input amplitudes of 12.5kV and 11.8kV respectively. In both cases the output voltage was successfully regulated to 12.7kV.

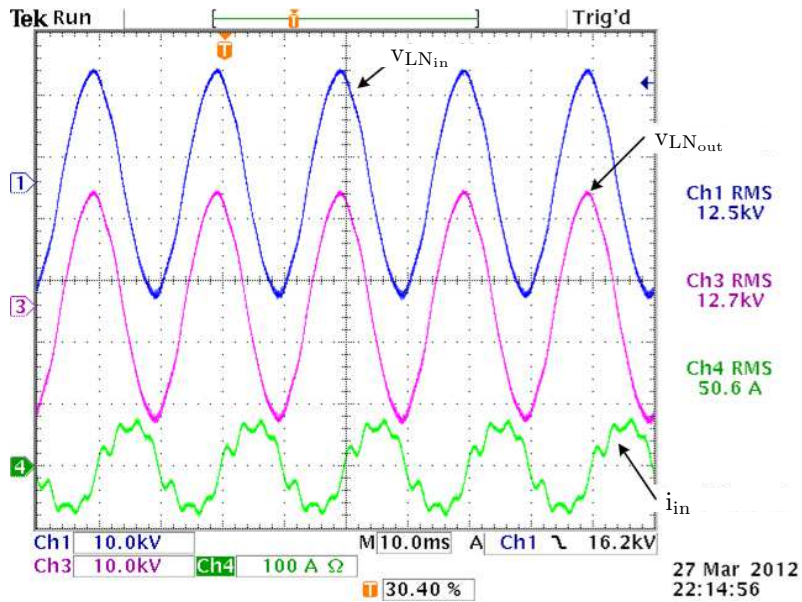


Figure 7.26: Test results with system input voltage of 12.5 kV, regulated to 12.7 kV.

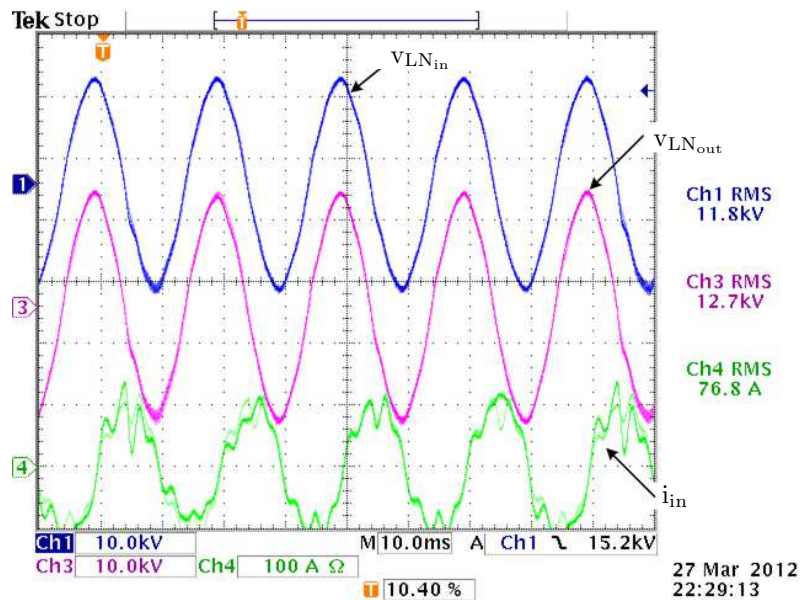


Figure 7.27: Test results with system input voltage of 11.8 kV, regulated to 12.7 kV.

Secondly, in Fig. 7.28, the response of the system to a input voltage dip is demonstrated. The system measures the mean-square of the input voltage in order to calculate the necessary boost required. The mean square reading updates for every 50 Hz period, and therefore a single period delay is seen from the dip (in the centre of the graph) to the response. The voltage is regulated to the required level without any visible transients.

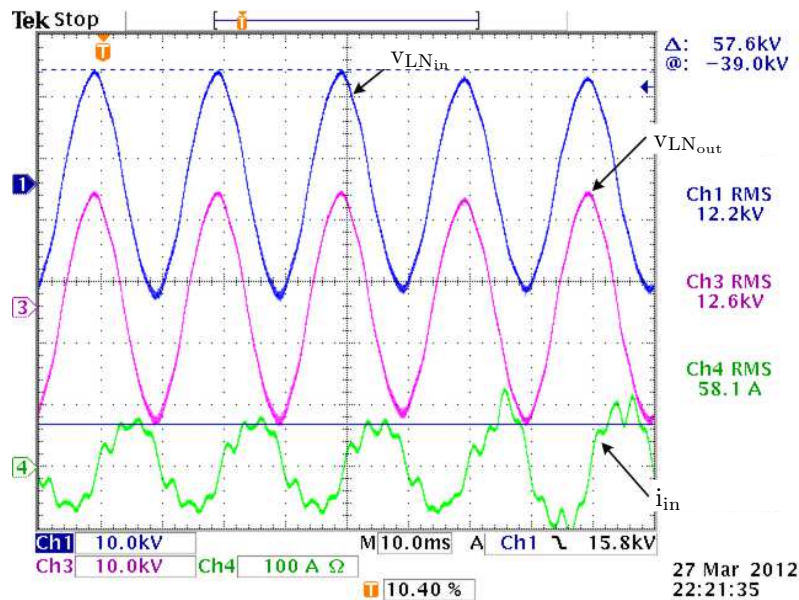


Figure 7.28: Test results with system input voltage of 12.2 kV, regulated to 12.6 kV.

7.4.3 Problems Encountered

During operation, the system remained stable, but with a periodic (8 second) ramp-like disturbance on the mean-square value. The value of the calculated mean-square value of the input voltage would steadily climb for 8 seconds and then jump back to the minimum value, where it would start climbing again. This disturbance caused unwanted transients on the system. The cause of this problem is puzzling, as the mean-square is only calculated over a 20ms window, which limits the effective “memory” of the component to far less than 8 s.

7.5 Summary

In this chapter the closed loop control results were presented. The response to various load steps, reference steps, and input voltage dips were shown in order to evaluate the robustness of the control.

Firstly, the efficacy of waveform correction was shown in Section 7.1. The results were very promising up until the point of instability at about 350 V input voltage. It was later found that one of the measurement boards were clamping the measurement at similar voltages. This could very well have been the cause of instability, so it is recommended that waveform correction be attempted again in the future.

Secondly, the results for amplitude regulation with pure sinusoidal references were shown in Section 7.2. The results for reference steps, load steps, source steps, and non-linear loads were all very good in terms of robustness of the output voltage.

Thirdly, the two regulation modules were operated together on a low-voltage system configuration in Section 7.3. The results were promising.

Lastly, the full voltage system results were shown in Section 7.4. The results show accurate voltage regulation to the nominal values with good robustness to input voltage dips.

In the next chapter, conclusions will be drawn and recommendations will be made for future work.

CHAPTER 8

CONCLUSIONS AND FUTURE WORK

“The future belongs to those who believe in the beauty of their dreams.”

- Eleanor Roosevelt

8.1 Conclusions

Much progress has been made towards developing a real voltage regulation solution for medium voltage transmission lines. Hardware circuits, supervisory control and closed loop control algorithms have been successfully designed and implemented to provide a proof-of-concept prototype.

8.1.1 Hardware

Various PC boards were designed and documented in Appendix A. An optic communication driver board was developed to transmit and receive fibre optic signals to and from the controller board. Power management boards were developed for mounting the various power regulators, and for doing undervoltage detection on the controller power supply.

8.1.2 Modelling

Although the modelling process seemed tedious and complicated, some important lessons were learnt in the process:

- the process of modeling is very helpful in gaining a better understanding of the system characteristics and behaviour
- the process of modeling can highlight vulnerabilities of the topology.

8.1.3 Supervisory Control / VHDL Design

Supervisory control was developed and implemented on the Altera Cyclone III FPGA. Chapter 5 details the FGPA design, where the supervisory control features include

- system and module safe startup and shutdown sequences
- user interface via LCD screen and pushbuttons
- measurement ADC conversion and filtering
- system level error detection such as
 - frequency detection

- under voltage detection on power supply
- overvoltage and overcurrent detection on ADC signals
- operation of soft-start and hardware bypasses
- supervision of multiple modules simultaneously
 - error monitoring and handling
 - reference generation
- reusable generic components (filters, differentiators, saturators, debouncers, waveform generators, etc.)

Through more than two years of development and testing, the supervisory control system has ensured safe system operation such that no major system components were destroyed. The lessons learnt during this study regarding VHDL design were that

- The design approach, with conceptual design in VHDL-AMS, followed by VHDL simulation, followed by VHDL testing via Signaltap is very effective.
- Effective calculation of the input voltage mean square is important to reliable system performance. This remains problematic with periodic distortions appearing on the mean square calculations.
- A generic and modular VHDL design approach is effective in keeping the code manageable and extensible.

8.1.4 Closed Loop Control

Sliding mode control was used to implement robust closed loop control in the regulator modules.

The necessary sliding mode theory is covered in Chapter 3 and modeling and simulation of the key components is detailed in Chapter 4. Modelling was done in the VHDL-AMS modelling language, which provided good integration between digital and analog circuits. It also allowed for virtually identical algorithms to be used for both simulation and implementation.

The sliding-mode algorithm development and simulations thereof is shown in Chapter 6. Simulations results of the algorithm is positive and demonstrates good performance and robustness with respect to parameter variations. Simulations are also used to motivate that the conditions for sliding mode are satisfied. This includes the reachability condition, the existence condition, and the stability condition. Some concerns remain regarding the reachability at high output references. This is caused by the phase delay between the controlled currents and their LPF references.

The system is tested physically and shows good results (Chapter 7, and Appendix C) even better than the simulation results. Various tests were done such as reference steps, input dips, load steps, non-linear loads, etc. The control shows good robustness throughout.

Some lessons learnt in terms of closed loop control were:

- Sliding-mode control is very useful for DC-DC converters and even DC-AC converters. This was demonstrated by the DC-DC buck converter example in Section 3.3.
- Design techniques are limited for high order plants as the graphical phase-portrait approach cannot be used. This design procedure is very dependent on the model as simulations had to be used extensively.

- Sliding-mode control is very useful in gaining robustness to external disturbances and parametric variations.
- Sliding-mode control is useful in limiting computational effort required, as the final control algorithm is very simple.
- Fixing the switching frequency is easily done with an adaptive PWM process.
- The development of the control system hinges on the ability to first develop quality references.

8.2 Future Work

There is still work to be done in the areas of hardware, VHDL development and control algorithms. The following is recommended.

Hardware

- Testing of hardware at rated current. This would require new step-up and step-down laboratory transformers or field tests on the national distribution lines.
- Three-phase implementation of the MVEVR by connecting three regulator systems in star configuration.
- Extension of the controller board for external long distance communication and reporting/diagnostics.

VHDL Design

- Development a component capable of robust RMS calculation on the system input voltage. The work presented in [14] could possibly be very valuable to achieving this task.
- Extension communication capabilities for remote control and operational data logging.
- Implementation of pipe-lining of the control processes for the regulator modules, rather than having each module controlled by its own instantiation. This would allow more computationally intensive algorithms, such as model predictive control, to be employed on more than one module.
- Work on achieving gate-level simulations in ModelSim for the entire design, rather than functional simulations only.

Control

- Investigation into methods of generating deterministic current references without having to use a low-pass filter. This could improve reachability and also simplify the mathematics required to prove the existence condition.
- Development of the double canonical control approach further to improve capacitor current control.
- Research into solving the instability problem with waveform correction / harmonic suppression.

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APPENDIX A

HARDWARE DESIGN

The scope of the MVEVR hardware is large and complex. It includes the power electronics, power transformers, small-signal boards and small signal supplies. This chapter covers the hardware design related to the system controller and the controller power supply. The basic power converter design, as well as the design of the various protection circuits can be found in [53].

A.1 Small-signal PC Boards

Various small-signal PC boards were used in the MVEVR system. These include the following:

- FPGA controller board
- IGBT driver boards
- optic driver/receiver board
- optic push-button boards
- voltage and current measurement boards
- system protection boards
- system soft start board
- module bus voltage sign sensing boards.

The relations between the PC boards listed above is illustrated in Fig. A.1. The optic push-button boards were created for user communication with the FPGA controller. The high electric isolation of the optic fibre medium was used to protect the user against electrocution. The receiver board was mounted directly on the FPGA board as an extension.

The optic driver board was designed to extend the optic capabilities of the controller board for internal system communication and control. This board features 16 optic receivers and 16 optic transmitters to relay communication signals to and from the IGBT driver boards, system protection boards, regulator soft start boards, and the regulator sign detection boards. In this case, optic isolation was used to protect the different boards from the large ground-potential differences between them.

The differential measurement boards were designed to interface with the analogue to digital converter (ADC) on the controller board. Various current and voltage measurements were made and processed by the FPGA controller.

The design of the FPGA board is documented in [17].

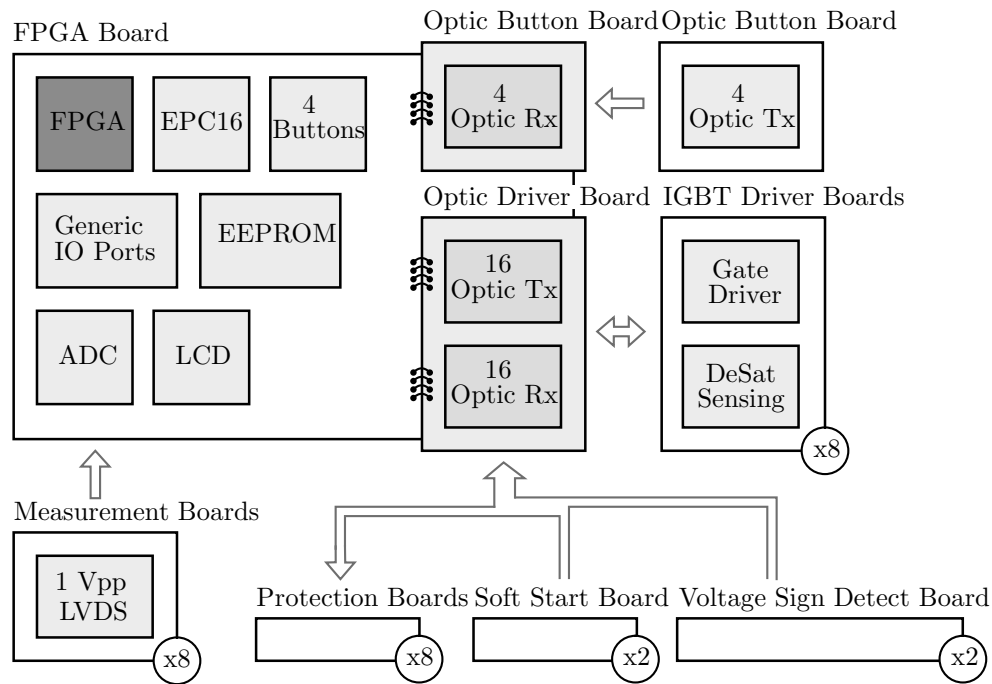


Figure A.1: Relationship between small-signal PC boards.

A.1.1 FPGA Architecture

The board is built around the Altera Cyclone III EP3C40Q240C8 FPGA. The chip features reprogrammable (SRAM) memory that can be re-programmed, but - due to the volatile nature of SRAM - is cleared when the control board loses power. The optional EPC16 configuration device was added to the board, providing the option to store the SRAM configuration in the EPC16's flash memory. Flash memory is non-volatile and is preserved during a no-power scenario. The FPGA is then automatically configured by the configuration device on power-up.

Additional Features and Capabilities

- 32 I/O ports with level shifters for 5V logic interface. This was used to drive 16 optic receivers and 16 optic transmitters.
- 15 Additional generic IO pins.
- High speed 8-channel ADC with minimum sampling rate of 20MSPS (Mega Samples per Second) per channel.
- LCD screen with 32 character display.

A.1.2 Optical Driver Board

The control board was extended to add 16 optic receivers and 16 optic transmitters for communication with the rest of the system. This provides fast data transfer with much needed optic isolation between small-signal and large-signal modules.

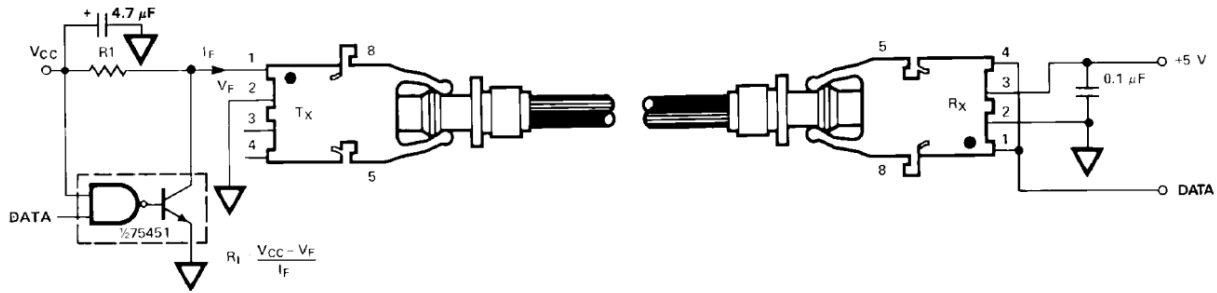


Figure 2. Typical 5 MBd Interface Circuit.

Figure A.2: Typical 5MBd Interface Circuit. Taken from [52].

The manufacturer recommended driver circuit[52] was modified to prevent a momentary “on” pulse on the optic LED when the controller is started and the power-supplies go from off to on. This modification (compare Fig. A.2 to A.3) results in a reversal of the polarity of the required data signal from the FPGA. Where it was active high before, it is now active low.

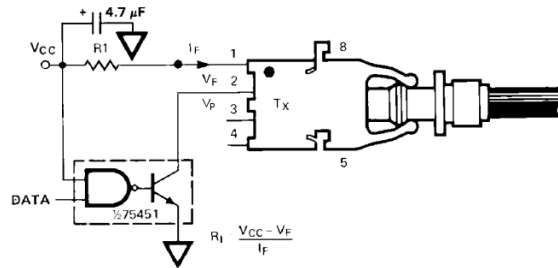


Figure A.3: Modified 5MBd Interface Circuit. Modified from version found in[52].

Resistor R_1 is left to be calculated. R_1 is designed using eq. A.1 and fig. A.4.

$$R_1 = \frac{V_{CC} - V_F}{I_F} \quad (\text{A.1})$$

$$V_F = V_{FP} + V_P \quad (\text{A.2})$$

It can be seen from fig. A.5(a) that, for a maximum cable length of 2 meters, a overdrive forward current of 43mA is needed for guaranteed performance in a temperature range of 0 – 70°C.

The SN75451B peripheral driver’s maximum output voltage (conducting), V_P , is 0.4V [33, p. 3]. Therefore the value of R_1 can be found for a maximum optic transmitter forward voltage (V_{FP}) of 2.02V [52, p. 8]:

$$V_F = V_{FP} + V_P \quad (\text{A.3})$$

$$= 2.02V + 0.4V \quad (\text{A.4})$$

$$= 2.42V \quad (\text{A.5})$$

$$R_1 = \frac{V_{CC} - V_{FP} - V_P}{I_F} \quad (\text{A.6})$$

$$= \frac{5V - 2.02V - 0.4V}{43mA} \quad (\text{A.7})$$

$$= 60.0\Omega \quad (\text{A.8})$$

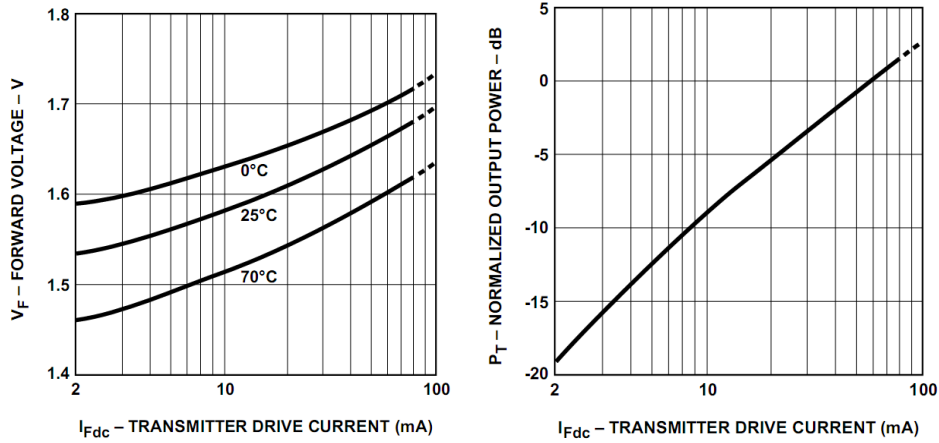


Figure A.4: (a) Typical Voltage vs. Drive Current and (b) Normalized Output Power vs. Drive Current. Taken from [52].

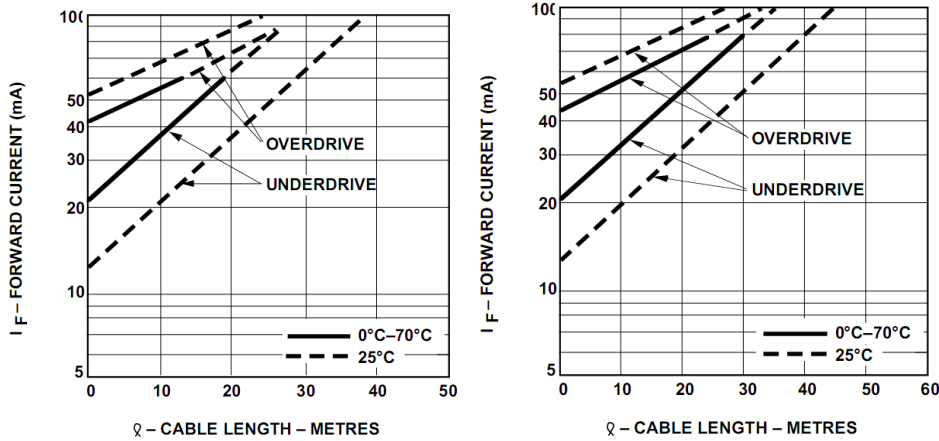


Figure A.5: (a) Guaranteed System Performance with Standard Cable (HFBR-15X1/25X1) (b) Guaranteed System Performance with Improved Cable (HFBR-15X1/25X1). Taken from [52]

A.1.3 Under Voltage Protection

Under voltage protection (UVP) was implemented on the power supply of the FPGA controller. If the system was to lose power, this protection system would send an optic pulse to the controller, which would cause the controller to carry out a power-down sequence.

The UVP is implemented on the supply side of the controller's 5V switch-mode power regulator, the TPM30105. This module accepts an AC input range of 85 – 264 VAC. The nominal voltage supplied to the power supply is 230 VAC. A peak detector circuit detects the peak supply voltage and outputs the result as a

DC voltage. A comparator is used to compare the peak value to a chosen reference. If the peak voltage drops below the specified reference, an optic pulse is generated and sent to the FPGA controller board.

The reference was chosen to be 150 VAC. This enforces a 65 V safety margin above the minimum input voltage of the power supply. In the event of a power failure, this will allow the controller some time to carry out an emergency shutdown sequence.

As illustrated in Fig. A.6, the under voltage detector is comprised of the following:

1. A resistive divider
2. Input Buffer
3. A full wave active rectifier
4. A peak detector
5. An output buffer
6. A comparator
7. An optic driver circuit

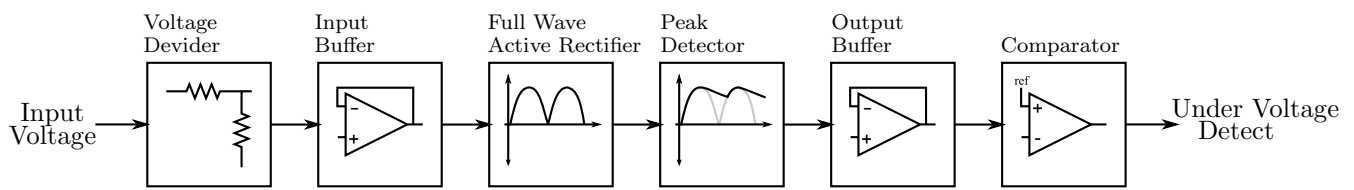


Figure A.6: A top-level representation of the under voltage protection circuit.

Resistive Divider

The resistive divider scales the nominal 230 V input signal measurement to a small signal that fits comfortably within the supply rails of the various stages of the peak detector. The resistive divider is shown in Fig. A.7. Tyco type SM moulded power resistors were used to implement the voltage divider.

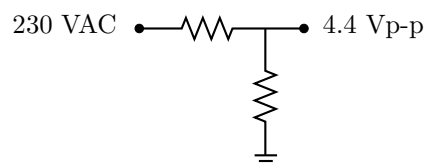


Figure A.7: Resistive divider of the UVP system.

Input Buffer

The input buffer is used to provide a high input impedance and hence protect the circuitry of the full wave rectifier in the following stage. The AD8512 operational amplifier was used for the buffer.

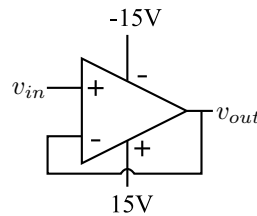


Figure A.8: Input buffer of the UVP system.

Full Wave Rectifier

A full wave active rectifier is used to avoid the turn-on voltage of the diodes and to minimize the drooping effect between peaks. This precision rectifier circuit was obtained from the supplier data sheet [16] and is shown in Fig. A.9. This circuit exploits the saturation of two single-rail op amps for full wave rectification, conveniently requiring no diodes, and consequently having no diode forward voltage drop in the output. Full wave rectification is desirable for more accurate peak detection. The AD8512 (dual package) operational amplifier was used to implement the full wave rectifier.

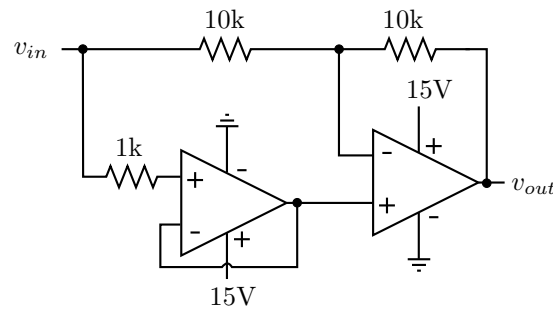


Figure A.9: Full wave rectifier of the UVP system.

Peak Detector

The peak detector is an active diode (diode and operational amplifier combination) and a capacitor. The larger the capacitor, the longer any given peak is maintained. The smaller the capacitor, the faster the measured peak droops until the next peak is found.

Care needs to be taken to find the right value for this capacitor. If it is too large, the instantaneous peak value will be deceptively large, and a sudden under-voltage will be missed. If it is too small, the drooping effect will cause false under voltage detection between consecutive peaks.

The capacitor value was chosen so that, for a constant AC input of 80% of the nominal, the drooping does not fall below the voltage corresponding to the 150V threshold. The peak detector schematic is shown in Fig. A.10. The AD8512 operational amplifier was used to implement the peak detector.

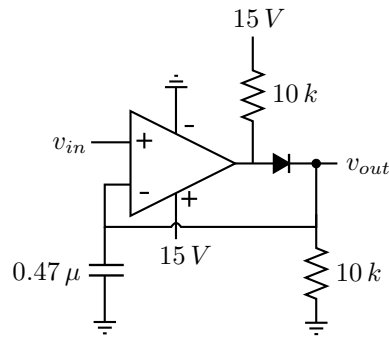


Figure A.10: Peak detector of the UVP system.

Output Buffer

The output buffer is shown in Fig. A.11. The AD8512 operational amplifier was used to implement the output buffer.

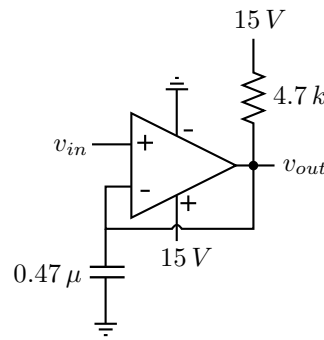


Figure A.11: Output buffer of the UVP system.

Comparator

The LM311D IC is shown in Fig. A.12 and was used as a comparator and a digital signal driver. The reference signal was generated from the 15 V supply with a variable resistive divider for fine-tuning. The 15 V digital output signal was scaled to 5 V by a resistive divider before being optically transmitted toward the controller board.

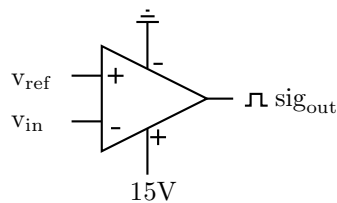


Figure A.12: Comparator of the UVP system with analog input, digital output.

Simulation and Testing

The resulting circuit was simulated in LTSpice, built, and tested. Simulations were performed to evaluate how fast the circuit can detect an abrupt supply failure. A curve was fitted to the peak signal for an exponentially decaying input signal to determine the theoretical maximum peak tracking limit. This is shown in Fig. A.13. The input signal is represented by $v(o)e^{-28t}$ V, and the detected peak is unable to perfectly track it. The peak

detector is seen to be limited to a decay rate equal to that of $v(o)e^{-21t}$ V. With an initial amplitude of $230 V_{\text{RMS}}$, this evaluates to $-6830e^{-21t} \frac{\text{Volts}}{\text{sec}}$. This is good enough, as it was shown in practical tests that, when the supply power is abruptly switched off, the power on the controller board stays on its nominal level (5 V) for more than 2 seconds after the under-voltage pulse is transmitted. This is due to large output capacitance on the power supplies, and ensures more than enough time for the controller to complete any shutdown sequence.

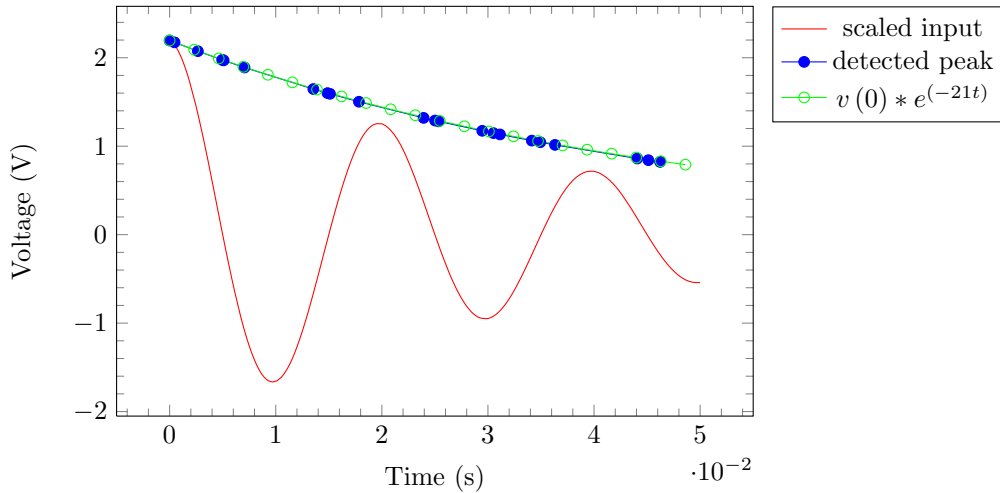


Figure A.13: The peak detection is limited in speed for quickly fading signals.

The working of the under voltage detection circuit is shown in Fig. A.14. It is seen that, when the detected peak (blue) voltage of the scaled and fully rectified input signal (red) falls below the reference voltage (green), an error signal (black) is generated. This error signal is transmitted optically to the controller board to initiate appropriate action.

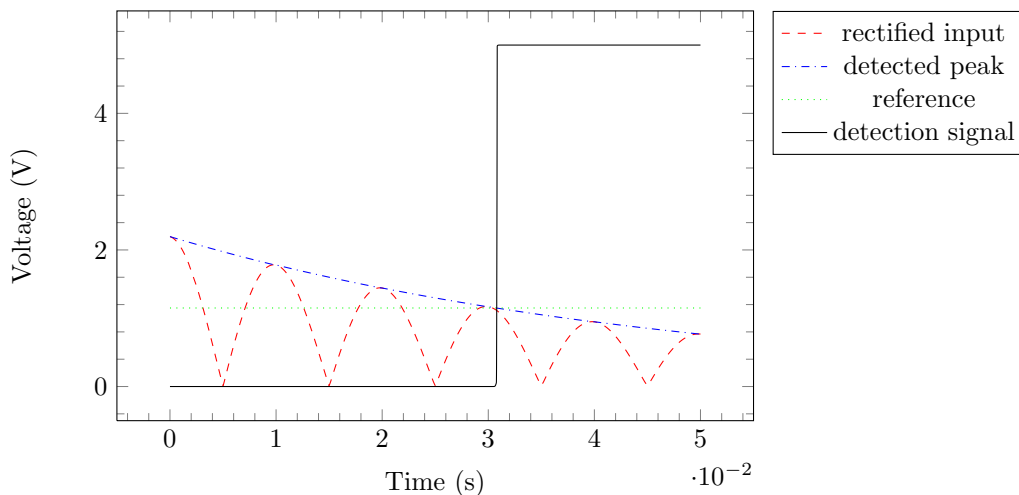


Figure A.14: Simulation of the supply under voltage detection circuit as the supply voltage is falling exponentially.

A.2 System Photographs

The chapter will be concluded with photos of the various hardware boards discussed.

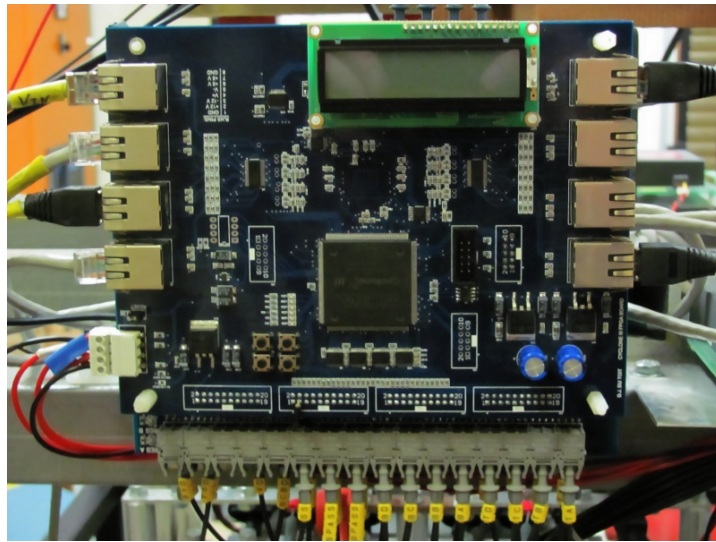


Figure A.15: Controller board installed with measurement board inputs on the left and right, LCD screen on top, with optic button inputs coming in behind it, and optic driver board showing at the bottom.

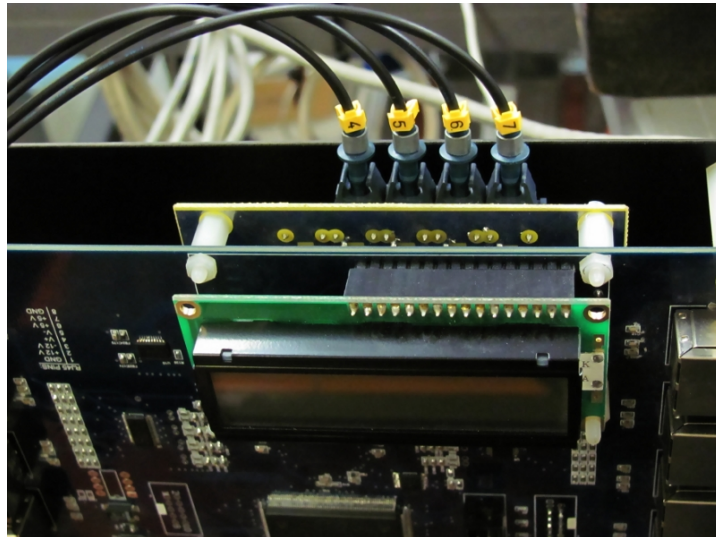


Figure A.16: Optic receivers for the push-button signals, installed on the controller board.

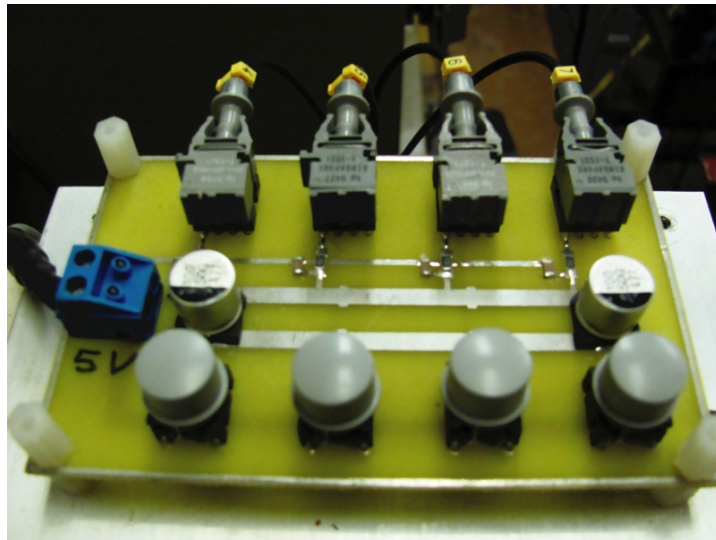


Figure A.17: Pushbuttons with optic communication to protect user from electrocution.

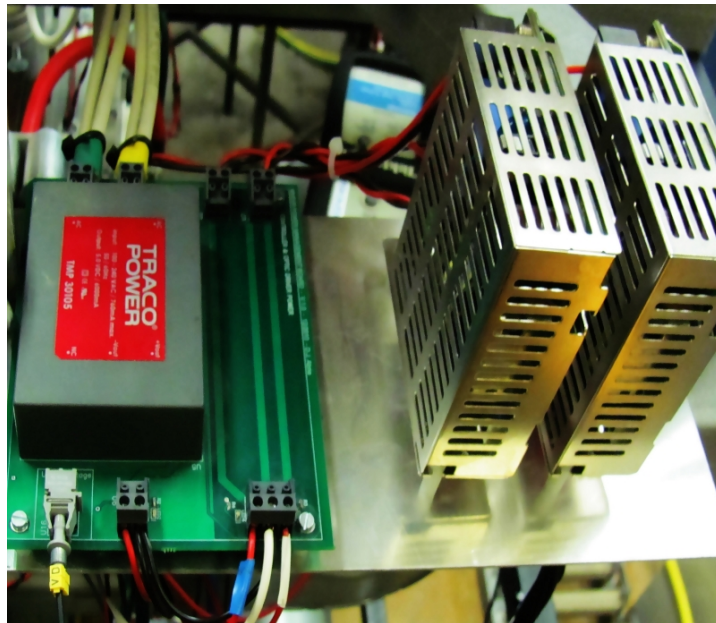


Figure A.18: Installation of small signal power supplies with + and - 15 V on the right, and 5 V mounted on the left PCB. The optic transmitter of the under voltage detection circuit can be seen on the bottom part of the PCB.

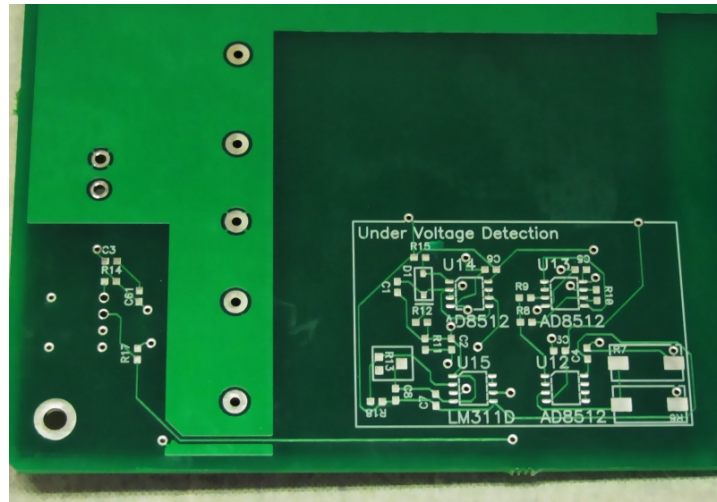


Figure A.19: The unpopulated under voltage detection circuit is shown.

APPENDIX B

OPEN-LOOP CONTROL

B.1 Open-Loop Control of the MVEVR

The open-loop control scheme can operate in one of two ways. The output voltage can be regulated based on either the peak value of the input voltage, or on the RMS (or rather the Mean Square) value of the input voltage.

In the first case, the output voltage amplitude can be directed towards the desired reference value by assuming the following relationship between the input and output voltage:

$$V_{out} = V_{in} \cdot D \quad (\text{B.1})$$

, where D is the duty cycle.

If this general relationship holds, then D can easily be computed by dividing the amplitude of the output voltage reference by the amplitude of the input voltage:

$$D = \frac{A_{V_{out_{ref}}}}{A_{V_{in}}} \quad (\text{B.2})$$

In the second case, the output voltage amplitude can be directed towards the desired reference value by calculating the mean-square of the output voltage, and then using a lookup table (LUT) to find the necessary duty cycle to produce the desired mean-square. The mean square is calculated for every half-cycle of the output voltage. Samples are squared and added to a running sum. At the end of the half-cycle, the running sum is divided by the total number of summations. This is equivalent to the following expression:

$$\text{Mean Square} = \frac{1}{n} \sum_{i=1}^n x^2(i) \quad (\text{B.3})$$

Offline calculations are done to populate the lookup table with duty cycle values calculated according to the following relationships:

$$\frac{1}{n} \sum_{i=1}^n (V_{out}(i))^2 = \frac{1}{n} \sum_{i=1}^n (V_{in}(i) \cdot D)^2 \quad (\text{B.4})$$

$$\frac{1}{n} \sum_{i=1}^n (V_{out}(i))^2 = \frac{1}{n} \cdot D^2 \cdot (\sum_{i=1}^n (V_{in}(i))^2) \quad (\text{B.5})$$

$$\frac{\frac{1}{n} \sum_{i=1}^n (V_{out}(i))^2}{\frac{1}{n} \sum_{i=1}^n (V_{in}(i))^2} = D^2 \quad (\text{B.6})$$

$$\sqrt{\frac{\frac{1}{n} \sum_{i=1}^n (V_{out}(i))^2}{\frac{1}{n} \sum_{i=1}^n (V_{in}(i) \cdot D)^2}} = D \quad (\text{B.7})$$

From Eq. B.7 it is then seen that - in a lookup table - a measured input value of $\frac{1}{n} \sum_{i=1}^n (V_{out}(i))^2$ can be mapped to an output value for the duty cycle, D, of $\sqrt{\frac{\frac{1}{n} \sum_{i=1}^n (V_{out}(i))^2}{\frac{1}{n} \sum_{i=1}^n (V_{in}(i) \cdot D)^2}}$.

The duty cycle value is passed from the LUT to the PWM process. This process compares the duty cycle value with a generated triangular wave. When the triangular wave is greater than the duty cycle value, a control command of '1' is generated. Otherwise, '0' is generated. Dead time and blanking time is then applied before the gating signals are generated and transmitted toward the IGBT drivers.

APPENDIX C

APPENDIX ADDITIONAL RESULTS

Aside from Sigma-Alpha, two other algorithms were also tested:

1. sigma-beta which controls the input bus capacitor and the output filter capacitor currents and generates sinusoidal current references based on the capacitance of the capacitor and the amplitude of voltage over it,
2. sigma-alpha-beta which is a hybrid between sigma-alpha and sigma-beta and controls the input bus capacitor current and the output filter inductor current.

Sigma-Beta Normal Regulation

The figures below show the module voltages and currents for regulation with the input bus voltage at 400 V, the load at 5 Ω load, and the module output voltage reference amplitude set to 350 V_p.

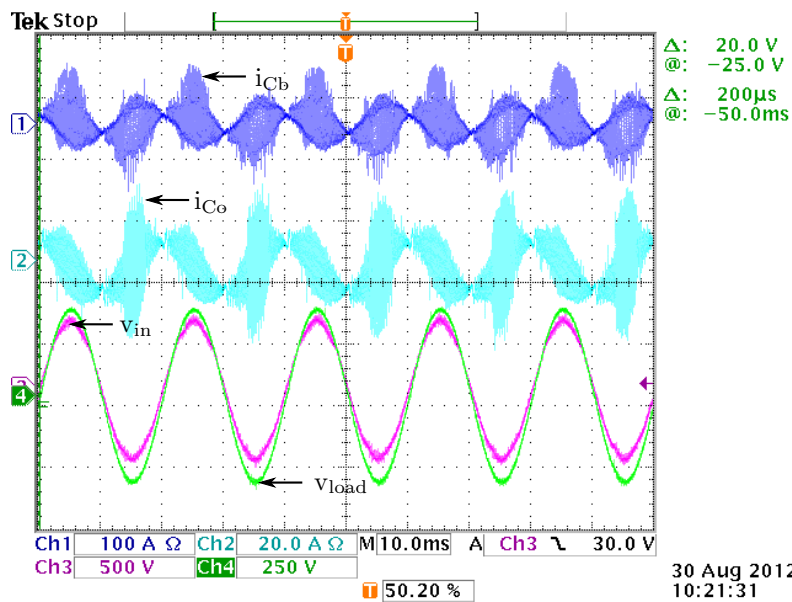


Figure C.1: Perspective view of the input capacitor current, i_{Cb} , the output filter capacitor current, i_{Co} , the input bus voltage, v_{in} , and the output voltage, v_{load} .

The output voltage amplitude is seen to be on target and the currents are stable. The waveforms correspond well to the simulations.

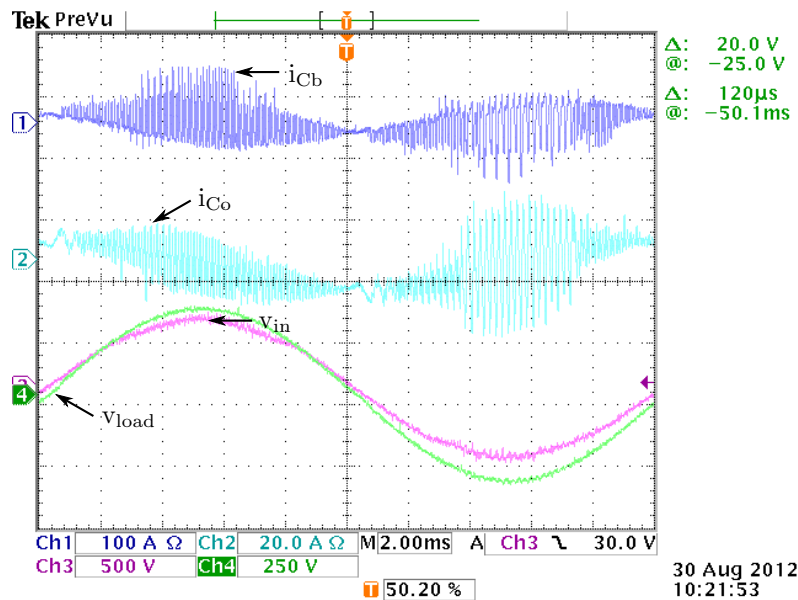
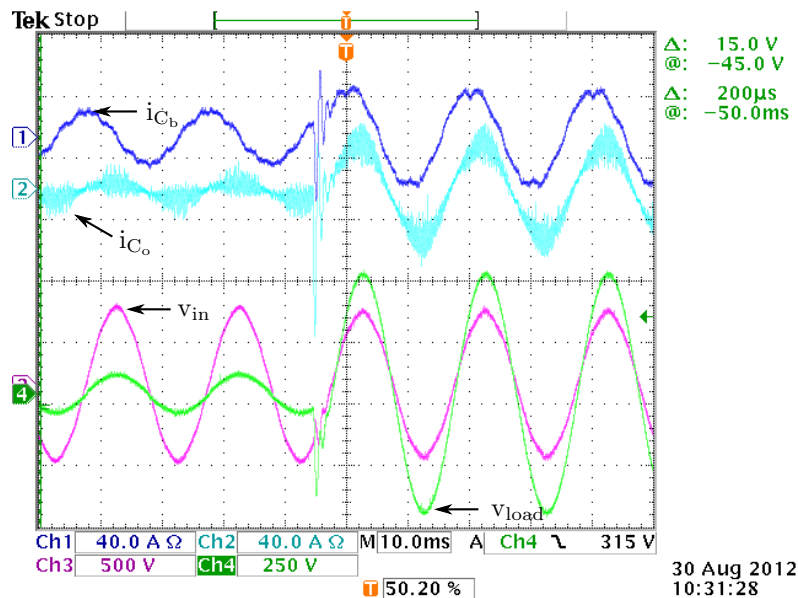


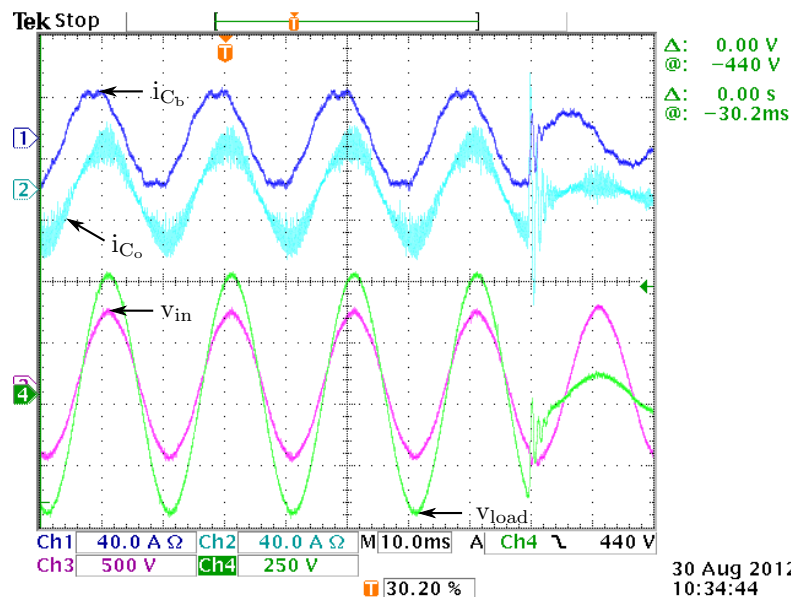
Figure C.2: Close-up view of the controlled module state variables.

Sigma-Beta Reference Steps

Reference steps on the module output voltage reference were done on a high-impedance load (15Ω) and a low-impedance load (5Ω) with both upward and downward reference steps on each.

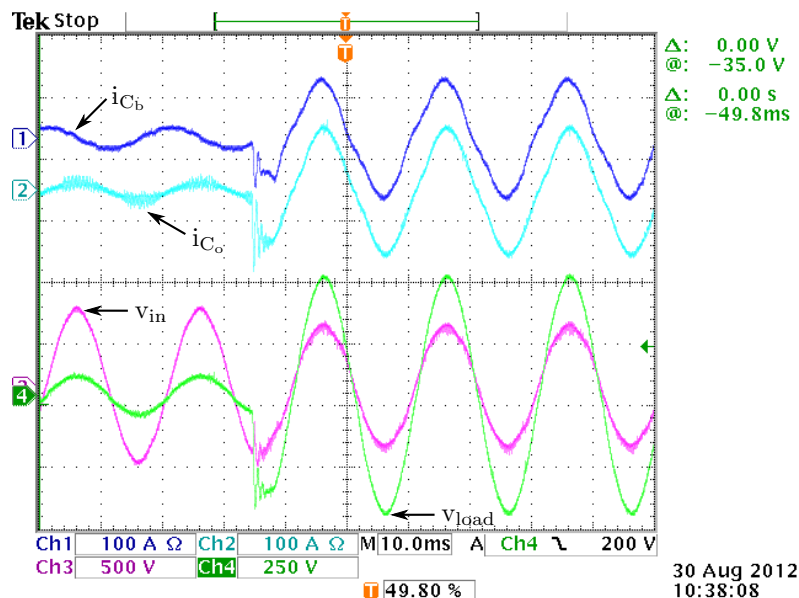
Figure C.3: Upward reference step on sigma-beta with 15Ω load.

At the instance of the reference step (Fig. C.3), some sharp transients are observed as the output voltage tracks the reference from $50V_{RMS}$ to $350V_{RMS}$. The transients are seen to transpire in about 3ms, whereafter the module remains in a stable state.

Figure C.4: Downward reference step on sigma-beta with $15\ \Omega$ load.

The downward reference step (Fig. C.4), exhibits much of the same performance as the upward step. The transient response can be controlled by adjusting the sliding coefficients of the sliding function. The overshoot and undamped behaviour can be reduced by decreasing the relative magnitude of the weight on the output voltage error. This however, was neglected, as it also increases the steady-state tracking error.

The upward and downward reference steps were also done on the lower-impedance load to see the transient performance with higher currents. This is shown in Figs. C.5 and C.6 below. The transient behaviour is seen to be much the same as in the case of the heavier load. The system maintains a fast response, good stability and good reference tracking.

Figure C.5: Upward reference step on sigma-beta with $5\ \Omega$ load.

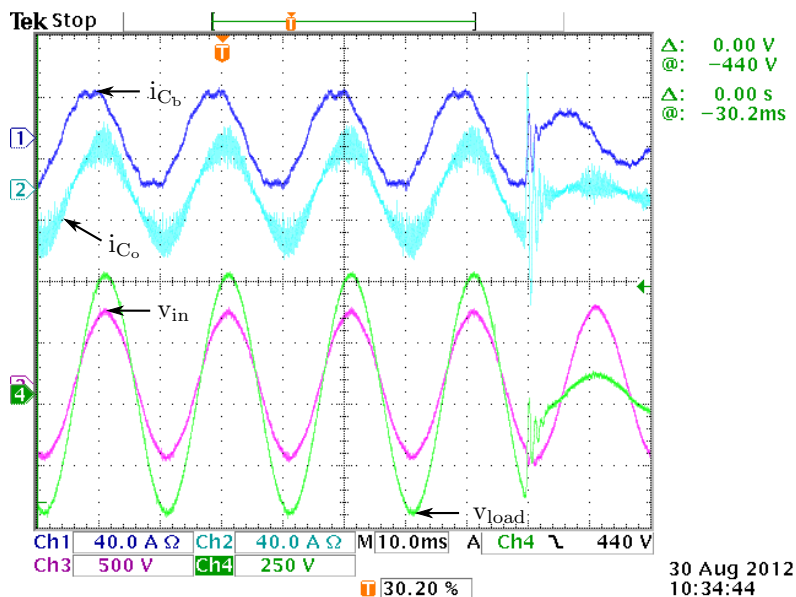


Figure C.6: Downward reference step on sigma-beta with 5 Ω load.

Sigma-Beta Load Steps

The load step was between 5 Ω and 15 Ω, in both directions, on the maximum voltage that the 400V variac could yield.

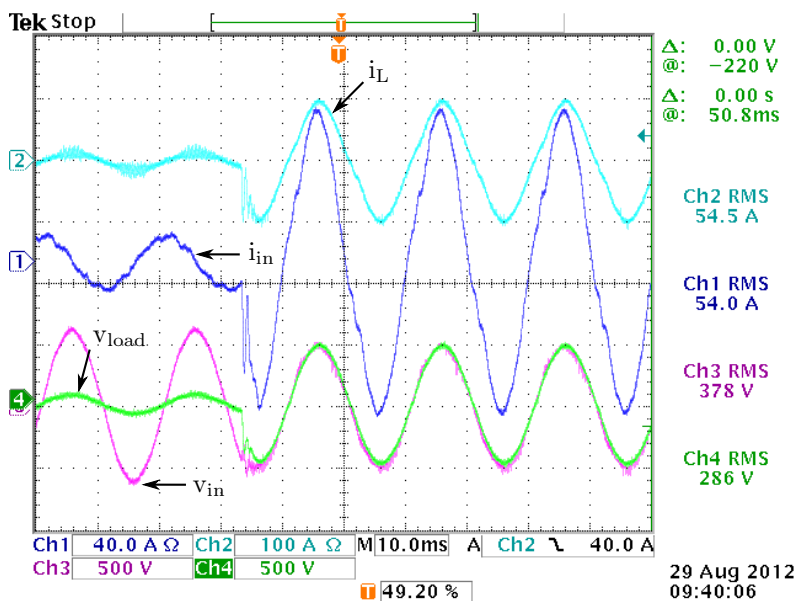


Figure C.7: Load step from 5 Ω to 15 Ω.

Notice the invariance of the module output voltage, v_{load} , as the load changes.

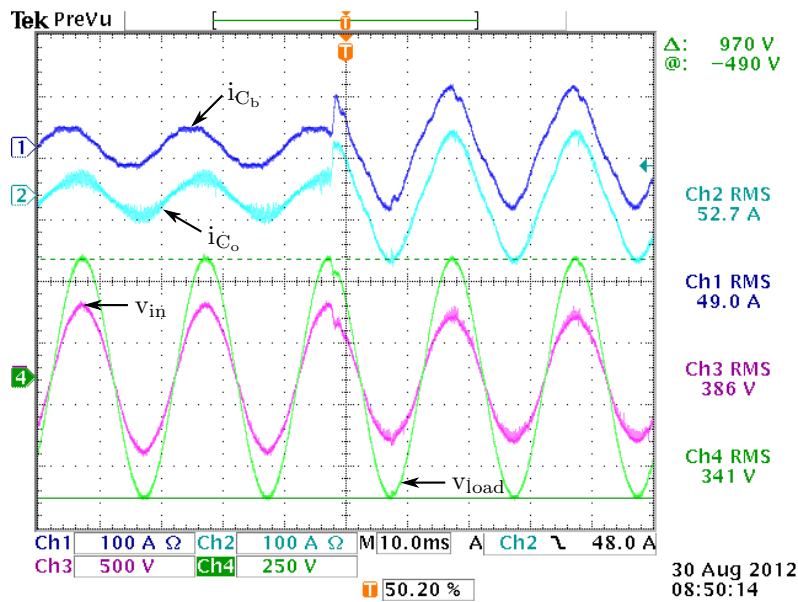


Figure C.8: Load step from 15 Ω to 5 Ω.

Sigma-Beta Source Steps

The source steps simulate a real-life undervoltage cinereo most accurately. The step was generated by switching a resistive devided in and out with a breaker. The supply was stepped from V to V and back with a 15 Ω load and a output voltage reference of 250 V. The 5 Ω load required too much current from the supply and exceeded the supply rating.

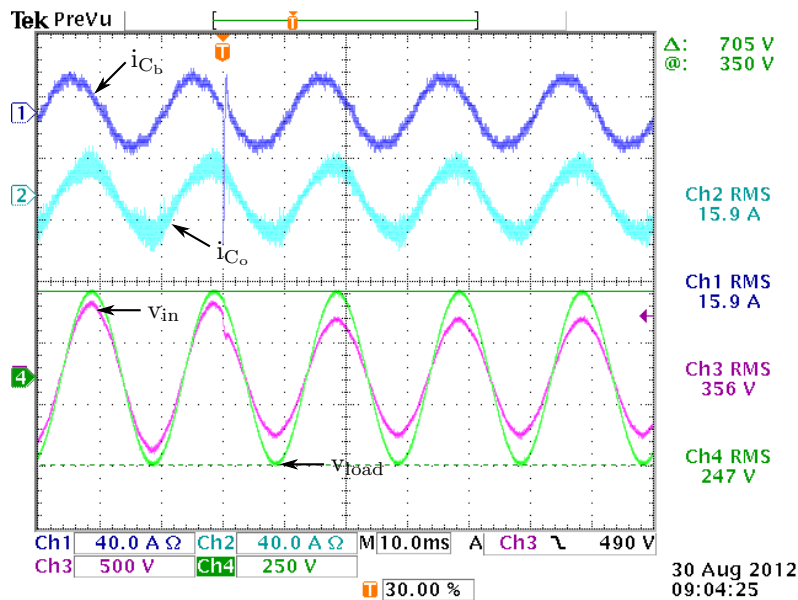


Figure C.9: Source step from 324V to 410V.

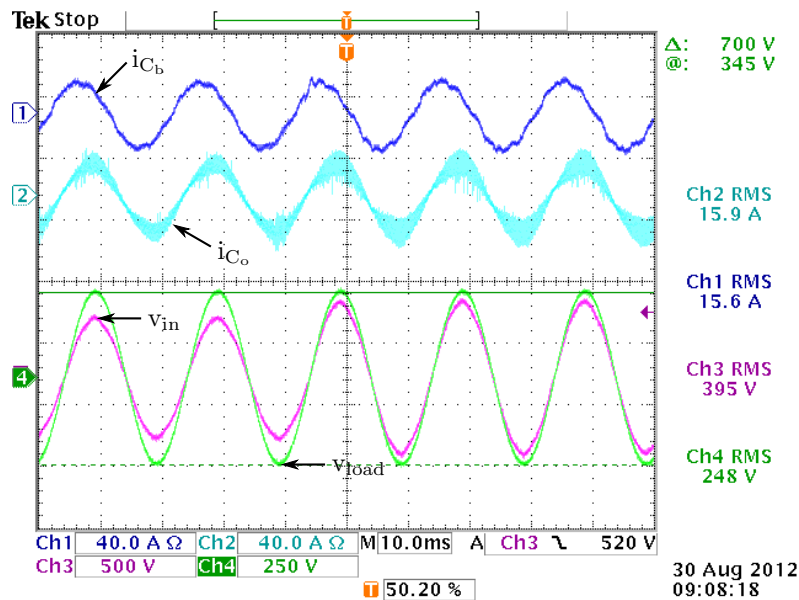


Figure C.10: Source step from 410V to 324V.

Sigma-Beta operating with a non-linear load

In this test, a rectifier load was connected to the module along with a 15Ω load. The capacitance of the rectifier capacitor was 15.6mF.

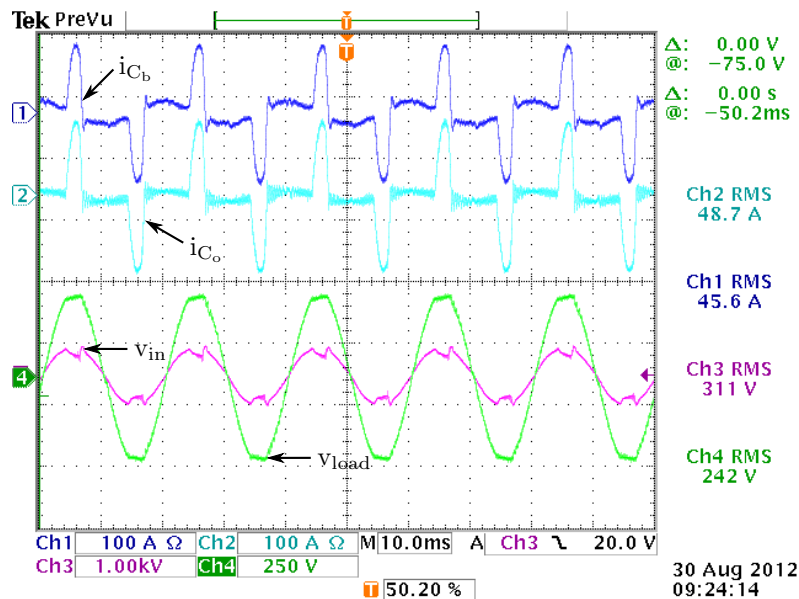


Figure C.11: Sigma-Beta running on a rectifier load.

The fast fourier transform (FFT) of the module input and output voltages were taken in order to analyse the harmonics pushed back into the power network. The magnitude is on a linear scale and a Hamming window was used. Fig. C.12 shows the FFT of the module input bus voltage. The first peak at 50Hz has amplitude of 306V and the second noteworthy peak at 150 Hz has an amplitude of 36V.

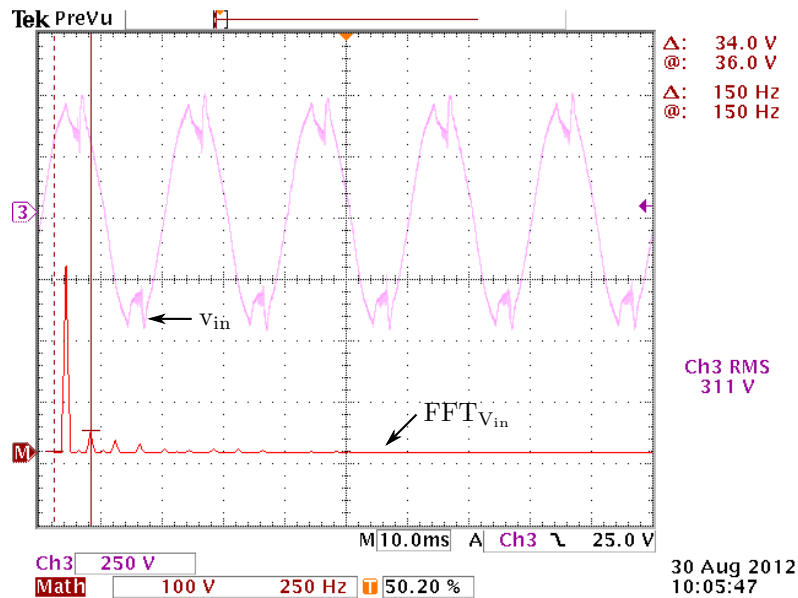


Figure C.12: FFT of the input bus voltage, v_{in} , while the module is running on a rectifier load.

Fig. C.13 shows the FFT of the module output voltage. The first peak at 50 Hz has amplitude of 242 V with small harmonics.

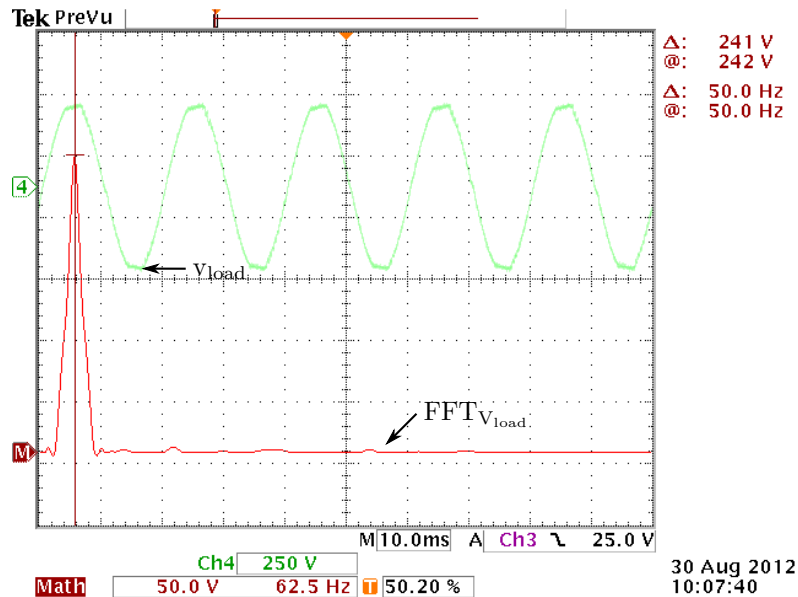


Figure C.13: FFT of the module output voltage, v_{load} , while the module is running on a rectifier load.

It is seen from the above two figures that the regulator does a fair job to regulate the output voltage to a sinusoid. The harmonics generated by the rectifier current is inevitably pushed back towards the input voltage. The system nonetheless remains in a stable and operational state.

Sigma-Alphabet Reference Steps

Reference steps on the module output voltage reference were done on a high-impedance load ($15\ \Omega$) and a low-impedance load ($5\ \Omega$) with both upward and downward reference steps on each.

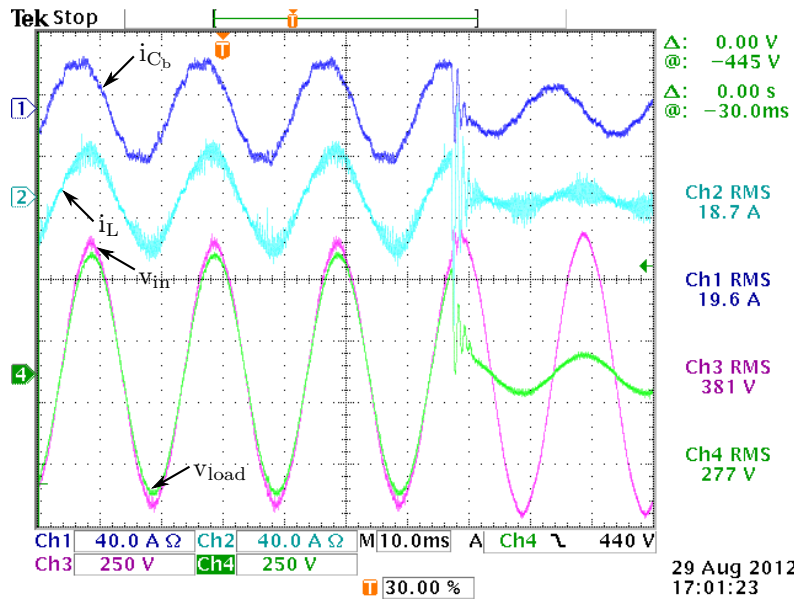


Figure C.14: Downward reference step on sigma-alpha with 15 Ω load.

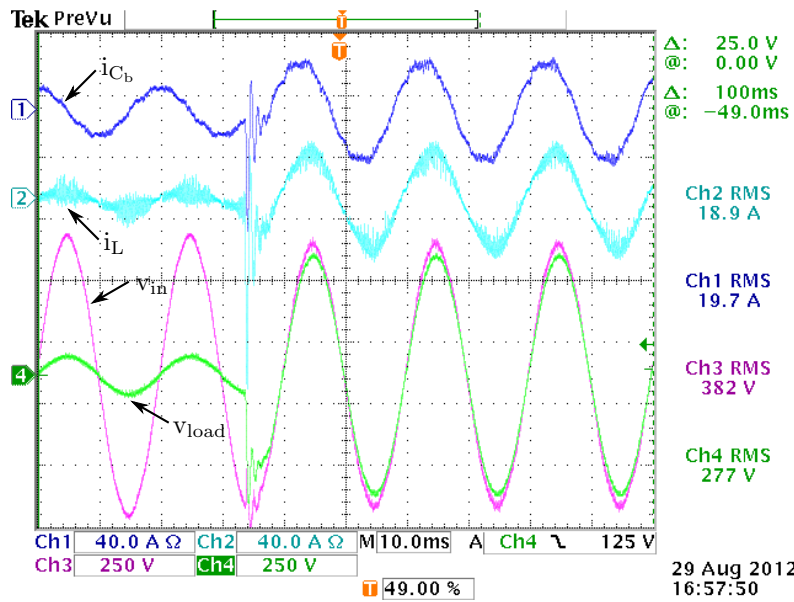


Figure C.15: Upward reference step on sigma-alpha with 15 Ω load.

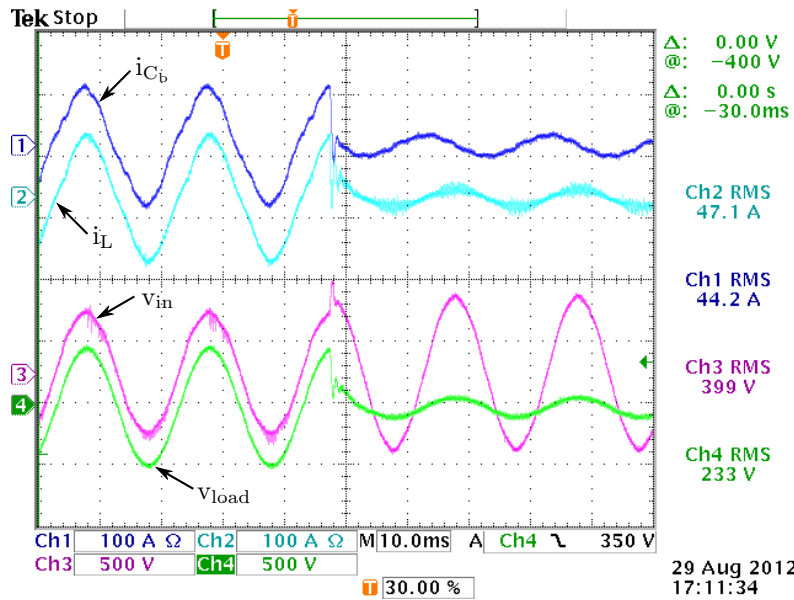


Figure C.16: Downward reference step on sigma-alpha-beta with 5 Ω load.

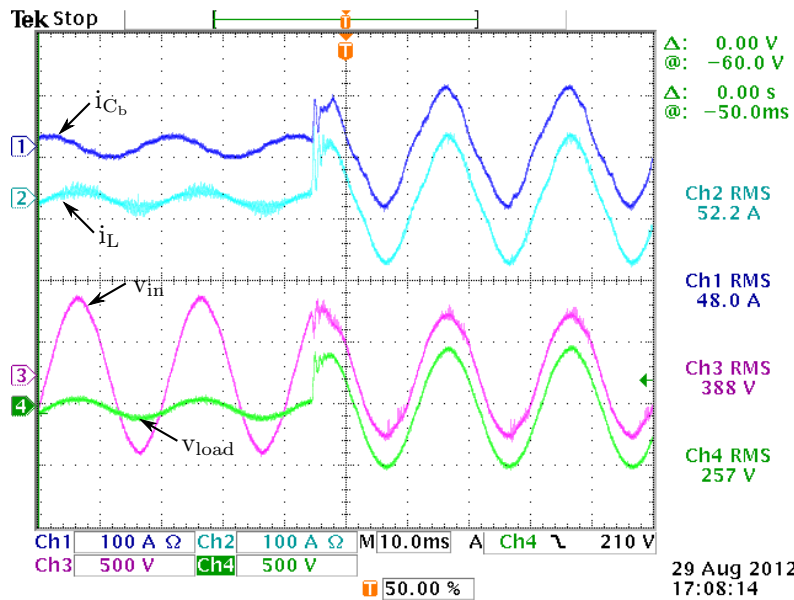


Figure C.17: Upward reference step on sigma-alpha-beta with 5 Ω load.

Sigma-AlphabetaLoad Steps

The load step was between 5 Ω and 15 Ω, in both directions, on the maximum voltage that the 400V variac could yield.

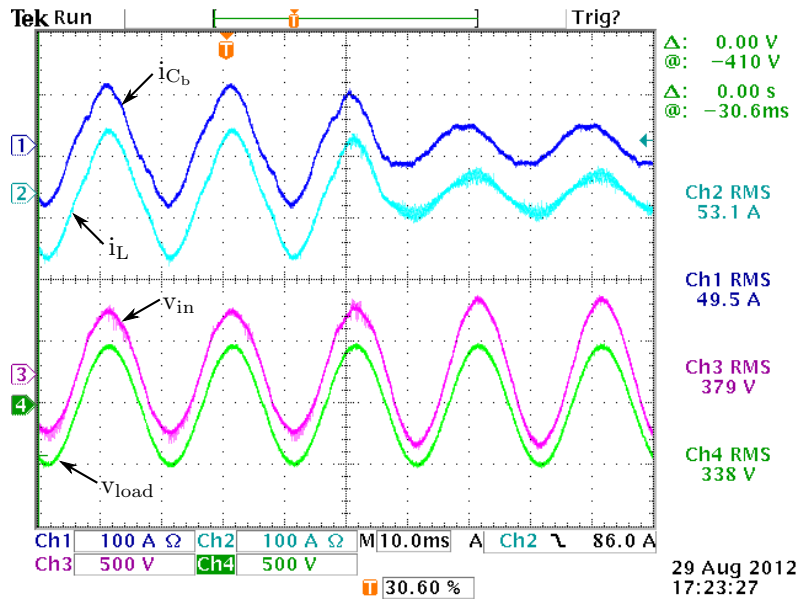


Figure C.18: Load step with sigma-alpha from 5 Ω to 15 Ω .

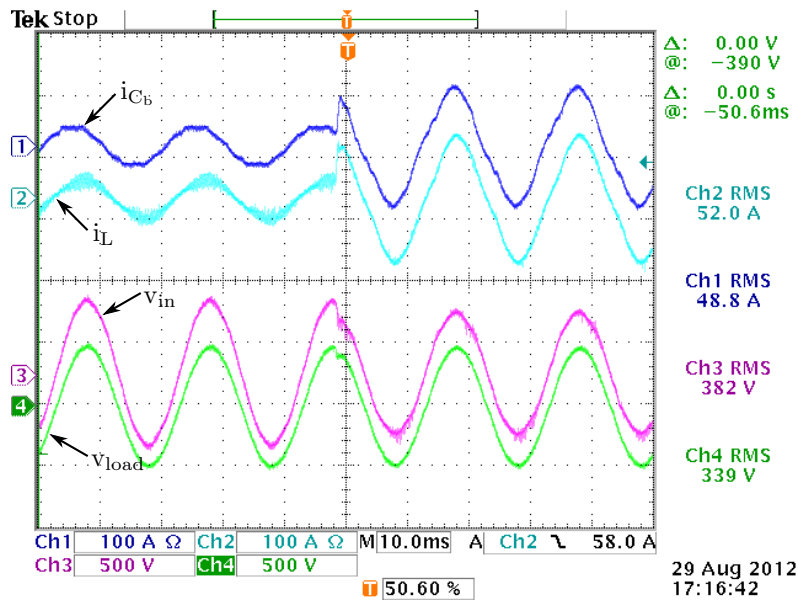


Figure C.19: Load step with sigma-alpha from 15 Ω to 5 Ω .

Sigma-Alphabeta Source Steps

The source steps simulate a real-life undervoltage cinareo most accurately. The step was generated by switching a resistive devided in and out with a breaker. The supply was stepped from V to V and back with a 15 Ω load and a output voltage reference of 250 V. The 5 Ω load required too much current from the supply and exceeded the supply rating.

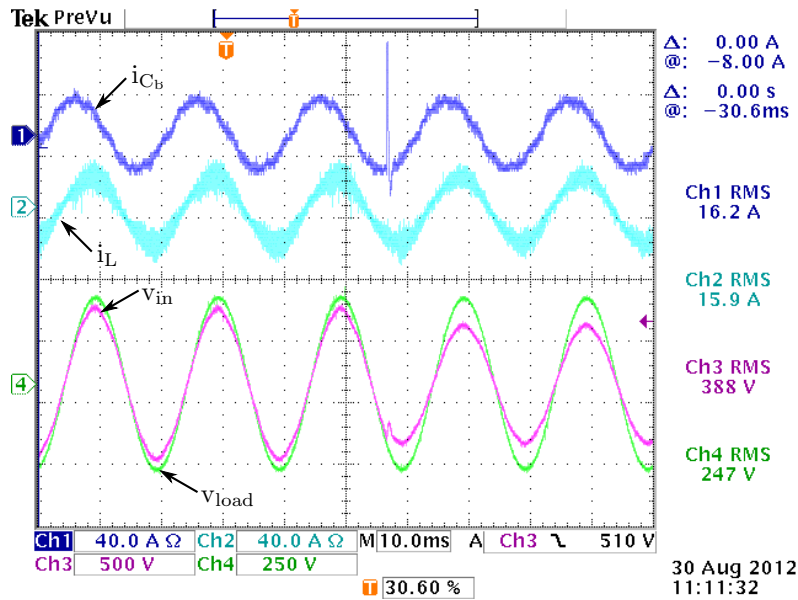


Figure C.20: Source step from 410 V to 324 V.

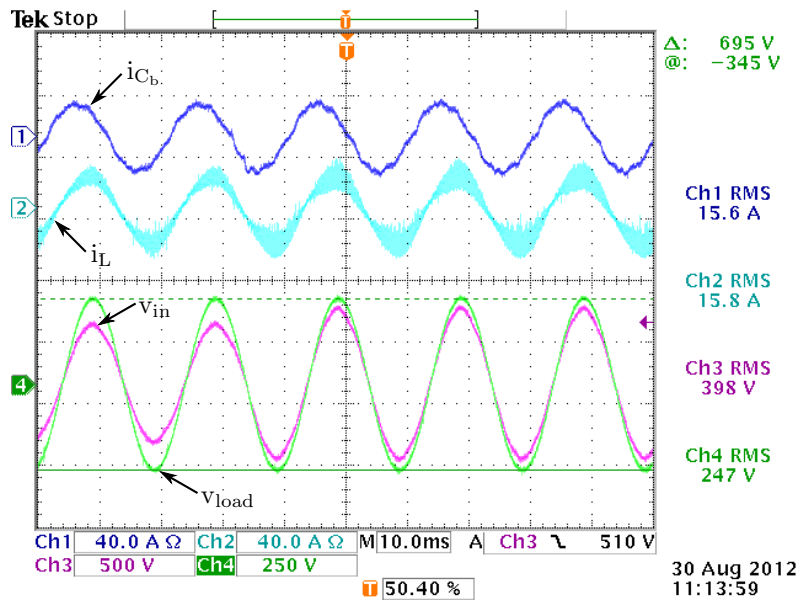


Figure C.21: Source step from 324 V to 410 V.

Sigma-Alphabeta operating with a non-linear load

In this test, a rectifier load was connected to the module along with a 15Ω load. The capacitance of the rectifier capacitor was 15.6mF.

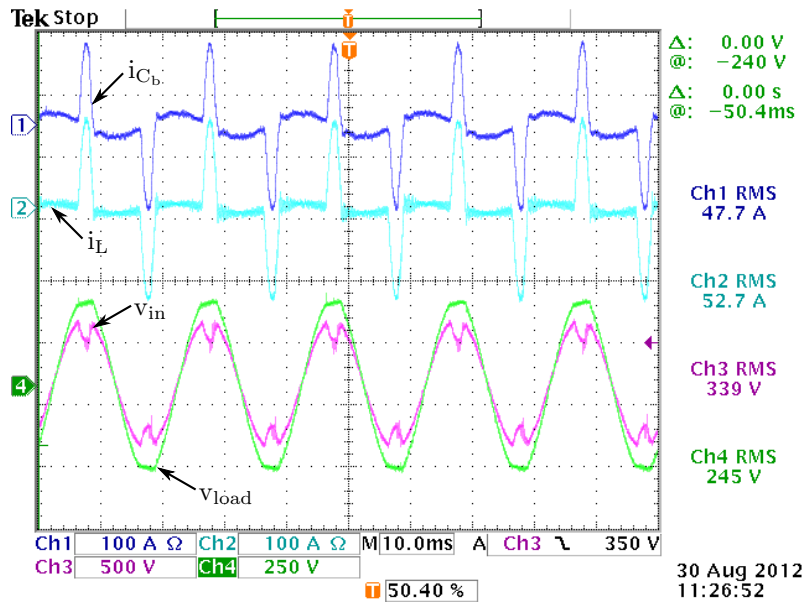


Figure C.22: Sigma-Alphabeta running on a rectifier load.