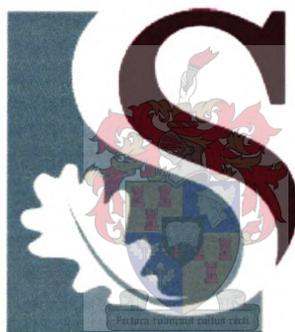


The Design and Simulation of a Superconductive, COSL Compatible Comparator and High-Speed Superconductive Analog-to-Digital Converter



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Dissertation submitted in fulfilment of the requirement for the Degree of Doctor of Philosophy in Electronic Engineering at the University of Stellenbosch.

Promoter: Professor W.J. Perold

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Declaration

I, the undersigned, hereby declare that the work contained in this dissertation is my own original work and has not previously in its entirety or part been submitted at any university for a degree.

Ian A. Powell

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Abstract

Analog-to-digital converters (ADCs) are an integral part of the interface between the analog and digital realms. This dissertation presents the design and simulation of a Complementary Output Switching-Logic (COSL) compatible, voltage state, switching logic comparator and a flash ADC for high speed applications with multi-GHz input bandwidth. Josephson technology and the COSL family of gates were utilized for this purpose.

A detailed design for the switching logic comparator is first provided. The design is verified with simulations to obtain a functional comparator. The comparator is then optimized utilizing an optimization tool developed using the scripting facilities of WRSpice. Incorporated in this tool is a Monte Carlo capability to randomly vary the component values according to Gaussian distributions, and trimming facilities to be able to trim a non-functional comparator to restore functionality. The design component values are then optimized by maximizing the yield of a comparator.

The optimized comparator is incorporated into the construction of a 4-bit quantizer of an ADC. The output from the quantizer section yields a switching-logic Gray-code output. A Gray-to-Binary converter is designed with COSL gates to convert the Gray output from the quantizer into Binary code for further processing.

The functionality, linearity, maximum input bandwidth and dynamic range of the 4-bit ADC is verified by simulation. A number of special input waveforms are used for this purpose. The performance of the comparator and the 4-bit ADC is also evaluated with thermal noise incorporated into simulation. Beat frequency simulations and Fourier spectra were also used in the evaluation of the ADC performance.

A fully functional 4-bit ADC, with a maximum input bandwidth of 10 GHz for a clock speed of 20 GHz was achieved through simulations. Beat frequency simulations revealed that the comparators have an input bandwidth greater than 19 GHz with sufficient dynamic range for an ADC of greater than 6 bits of resolution.

Due to the fact that the aperture time for the ADC is dependant on the rise time of the sampling pulse and not the width of the pulse, a much smaller aperture time is obtained which directly translates to higher input bandwidth.

Finally, a layout of a 4-bit sampler circuit was done according to the Hypres manufacturing process to enable the high-speed testing of the comparator circuits.

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Opsomming

Analoog-na-Digitale Omsetters (ADOs) vorm 'n integrale deel van die koppelvlak tussen die analoog en digitale wêreld. Hierdie proefskrif stel die ontwerp en simulatie van 'n Komplementêre Uittree Geskakelde Logika (COSL) aanpasbare, spanningstoestand, geskakelde logika vergelyker en ADO bekend. Hierdie ADO kan vir hoë spoed toepassings waar multi-GHz intree-bandwydte benodig word, aangewend word. Josephson tegnologie en die Komplementêre Uittree Geskakelde Logika (COSL) familie van hekke word vir hierdie doel gebruik.

Die volledige ontwerp vir die geskakelde logika vergelyker word eerstens gegee. Die ontwerp word met behulp van simulaties bevestig om sodoende 'n ten volle funksionele vergelyker te verkry. Die vergelyker word verder geoptimeer deur middel van 'n proses wat met behulp van programmering in WRSpice ontwikkel is. Hierdie optimaliseringsproses sluit 'n Monte Carlo proses in wat die komponentwaardes van die vergelyker onwillekeurig volgens 'n Gaussiese verspreiding verander, sowel as 'n verstellingsmeganisme waarmee 'n nie-funksionerende vergelyker verstel kan word totdat dit weer ten volle funksioneer. Die komponentwaardes word dan geoptimeer vir maksimale opbrengs van 'n vergelyker.

Die geoptimeerde vergelyker word gebruik in die konstruksie van 'n 4-bis kwantifiseerder vir 'n ADO. Die uittree van die 4-bis kwantifiseerder is in Gray kode. 'n Gray-na-Binêre kode omsetter word vir hierdie doel ontwerp deur van COSL hekke gebruik te maak.

Die volle ADO word voorts gesimuleer om die funksionaliteit, lineariteit, maksimum intreebandwydte en dinamiese bereik te verifieer. 'n Verskeidenheid van intreesone is vir hierdie doel gebruik. Die vergelyker en die 4-bis ADO is ook gesimuleer met termiese ruis om die effek daarvan te bepaal. Fourier spektra en "verskilfrekwensie" (Beat Frequency) simulaties word ook gebruik in die evaluering van die vergelyker en die ADO.

Die korrekte werking van 'n 4-bis ADO met intreebandwydte van 10 GHz met 'n klokspoed van 20 GHz is deur simulatie bevestig. Verskilfrekwensie simulaties dui aan dat die vergelykers 'n intreebandwydte van groter as 19 GHz het, met voldoende dinamiese bereik vir 6 bis resoluë.

Aangesien die vergelykers se venstertydperk bepaal word deur die stygende helling van die monsterpuls en nie deur die pulswydte nie, maak dit voorsiening vir 'n baie klein venstertydperk. 'n Klein venstertydperk is essensieel vir 'n hoë intreebandwydte.

'n Uitleg van 'n 4-bis vergelyker stadium is gedoen vir die Hypres vervaardigingsproses om die vergelyker teen hoë spoed te kan toets.

-oOo-

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A word of thanks to Cornell van Niekerk for his contributions through many a discussion over lunch, proof reading, advice regarding the layout of the dissertation and for coming to the rescue by making his computer available for printing of the manuscript when my own failed. Coenrad Fourie's help with the layout of the SLC sampler is also greatly appreciated.

Last but not least, I would like to thank my wife who kept me going through times when it seemed like the wheels were about to come off. Your love, understanding and support were much appreciated. Finally, a special thanks to my parents for their continued support and encouragement through all my years of postgraduate studies.



To my wife Roelien

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ACRONYMS

2JS	Two-Junction SQUID
ADC	Analog-to-Digital Converter
BCD	Binary Coded Decimal
COSL	Complementary Output Switching Logic
DAC	Digital-to-Analog Converter
ENOB	Effective Number Of Bits
GBC	Gray-to-Binary Convertor
JSPICE	Josephson Simulation Program for Integrated Circuit Engineering
LSB	Least Significant Bit
MSB	Most Significant Bit
OJS	One-Junction SQUID
QOJS	Quasi-One-Junction SQUID
SER	Signal-to-Error Ratio
SFDR	Spur Free Dynamic Range
SIS	Superconductor-Insulator-Superconductor
SLADC	Switching Logic Analog-to-Digital Converter
SLC	Switching Logic Comparator
SNR	Signal-to-Noise Ratio
SQUID	Superconducting Quantum Interference Device
WRSPICE	Whiteley Research Simulation Program for Integrated Circuit Engineering

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Introduction

■ Introduction

1.1 Advantages and Classification of Superconductive ADCs

- 1.1.1 Lobe-Counting Analog-to-Digital Converters
- 1.1.2 Wideband Analog-to-Digital Converters
- 1.1.3 Sigma-Delta Analog-to-Digital Converter
- 1.1.4 High Sensitivity Digital SQUIDS

1.2 Future Predictions

1.3 The Scope of this Study

1.4 Layout of Dissertation

■ Summary

■ Introduction

The following sections and Chapters will present the results of a study in designing a Superconductive Comparator for a High Speed Superconductive Analog-to-Digital Converter (ADC) as well as the construction and evaluation of such an ADC.

Analog-to-digital-converters (ADCs) are integral components of electronic systems which change signals from the analog state or realm to the discrete numbers in the digital realm, where all subsequent signal processing is performed by numerical computations in the digital domain.

Superconductive circuits based upon Josephson Junctions have a number of advantages that can be applied to ADC circuits. First, the Josephson device is a threshold device, with the superconducting critical current providing a built-in threshold. This property is fundamental to all analog comparisons performed in Josephson electronics and facilitates the conversion from the analog to the digital realm. Second, the switching time of a Josephson junction can be a few picoseconds, so the analog comparisons can be made quite rapidly. Finally, due to the phenomenon of superconducting interference, Josephson circuits, which exhibit periodic response characteristics, can be realized that will map a repeating code from an analog input.

In this Chapter it will be shown how these Josephson circuits are exploited to construct the first superconductive comparators and ADC circuits. The different ADC circuits will be discussed and compared to each other and predictions for future performance will be given.

1.1 Advantages and Classification of Superconductive ADCs

Superconductive ADCs can provide several advantages over semiconductor ADCs, such as low power dissipation, wide signal bandwidth, high dynamic range and high sensitivity to small signals. Przybysz [9] categorized superconductive ADCs in four groups. Each group uses a distinct architecture to best utilize the above mentioned advantages. This has been graphically illustrated in Fig 1.1.

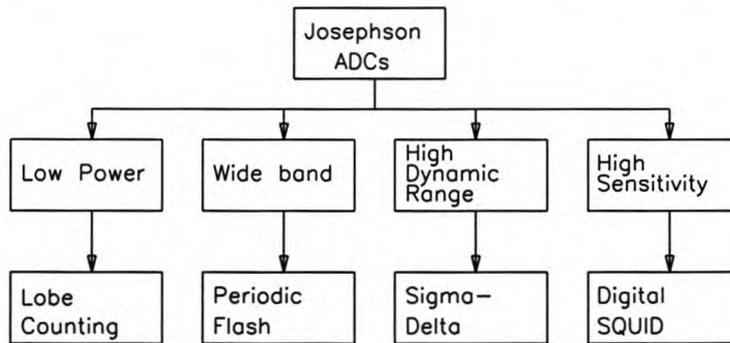


Fig. 1.1 Advantages of Superconductive ADCs and their preferred architecture [9].

Lobe counting ADCs dissipate a thousand times less power than a similar semiconductor ADC counterpart and are thus suitable for low power applications. Quasi-one-junction SQUID ADCs have performed 6-bit conversion of multi-GHz sine-wave input signals and are found in wide band ADCs. In high dynamic range ADCs. The superconductive sigma-delta ADC has performed 16-bit conversion of 10MHz signals while sampling at 40 GHz. Sensitive SQUIDS on the other hand, are utilized in SQUID microscopes to read low energy signals for non-destructive testing and bio-magnetic research.

1.1.1 Lobe-Counting Analog-to-Digital Converters

The most research has been done on the lobe-counting ADC architecture. It mainly consists of an input quantizer and a binary counter. The analog input signal is coupled to a two-junction SQUID, which generates a pulse each time a quantisation threshold is exceeded as the input level increases. A binary counter, consisting of a number of flip-flops, then counts these pulses and the final value of the counter represents the signal level.

Several variations on lobe-counting ADCs have been presented. Miller, *et al* [10] first described the correct operation of a lobe-counting ADC, while Kuo *et al* [11] reported a sampling rate of 1 Mega-samples per second on a 10-bit ADC. Kaplunenko *et al* [12] reported on an improved flip-flop. Filipenko *et al* [13] and Lee [14] proposed techniques for tracking bi-directional signals.

The main advantage of the lobe-counting ADC is its low power dissipation (typically 100 μ W for a 12-bit ADC at a sampling rate of 1 to 5 MHz). A disadvantage of this type of ADC is that the performance is limited by the maximum count rate of the flip-flop counting stages in the binary counter. High frequency, large-amplitude input signals can cause quantization boundaries to be crossed faster than the maximum count rate of the counters.

1.1.2 Wideband Analog-to-Digital Converters

Wideband ADCs require a resolution of between 6 and 8 bits, but with the highest possible input signal bandwidth that technology can provide. This high requirement can be achieved by superconductive Josephson electronics.

The periodicity of the quantum mechanical wave function in Josephson junctions is exploited to obtain a periodic response in the superconducting comparator. A block diagram of an ADC layout with comparators utilizing this periodic characteristic is given in Fig. 1.2. It is also illustrated graphically how the periodicity is used in obtaining the different levels of the ADC.

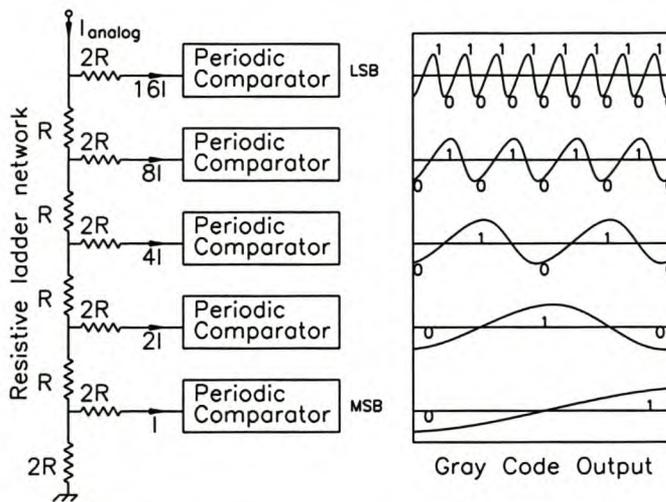


Fig. 1.2 Operational concept of a periodic-flash Analog-to-Digital Converter.

Mallick [16] analysed and simulated some of the comparators proposed by Ko [15] in an attempt to determine the feasibility of an 8-bit ADC. He predicted 7.6 effective bits of accuracy for a full-scale 500 MHz sine wave and 6.9 effective bits for a 1 GHz sine wave.

Bradley [17] designed and demonstrated the type of ADC first proposed by Ko. In a subsequent paper [18] on this subject he reported about 4 bits of resolution at 5 GHz and 3 bits of resolution at 10 GHz. He also demonstrated, by the use of beat-frequency measurements, 3 bit accurate conversion of an 8 GHz sine wave, 4 bit accurate conversion of a 4 GHz sine wave and 5 bit correct conversion at 2 GHz. This flash type ADC was also implemented by Kaplan [19] in the design of a flash digitizer with 6 bit resolution with an analog input bandwidth greater than 10 GHz.

1.1.3 Sigma-Delta Analog-to-Digital Converter

High dynamic range ADCs are required to digitize both large and small signals simultaneously. The Nyquist theorem states that when an input signal only contains frequency components in a frequency bandwidth f_B , the input signal can be characterized by digital words sampled at rates greater than $2f_B$.

High dynamic range ADCs take advantage of oversampling. Josephson ADCs can sample in the multi-GHz range. Likarev *et al* [25] proposed the first high dynamic range Josephson ADC utilizing oversampling. The lobe-counting ADC could track frequencies from DC to 50 MHz. They also predicted that, should they read the counter out at a clock rate of 200 GHz and processed the data at GHz rates, they could obtain 16 bits of resolution for a 100 MHz signal.

Sources of error in the superconducting sigma-delta ADC are thermal noise and clock jitter and will ultimately limit the resolution of the ADC.

1.1.4 High Sensitivity Digital SQUIDs

The sensitivity of superconducting quantum interference devices (SQUIDs) surpass that of semiconductor devices making it very attractive in the field of bio-magnetism for sensing brain waves, heart beats and other electrical signals in the human body.

Fujimaki *et al* [27] and Likarev *et al* [26] both designed and demonstrated digital SQUIDs by combining the SQUID and the ADC to simplify the read-out electronics.

1.2 Future Predictions

HYPRES has graphically presented the current and projected performance of high speed ADCs in Fig. 1.3 (reproduced with permission from HYPRES [44]). The two bands on the graph show the predicted performance for the high resolution ADCs and for the high input bandwidth ADCs. The performance of the ADCs is also dependent on the improvement of the manufacturing processes. HYPRES, for this reason, continues to push the limits in the manufacturing of superconducting electronics.

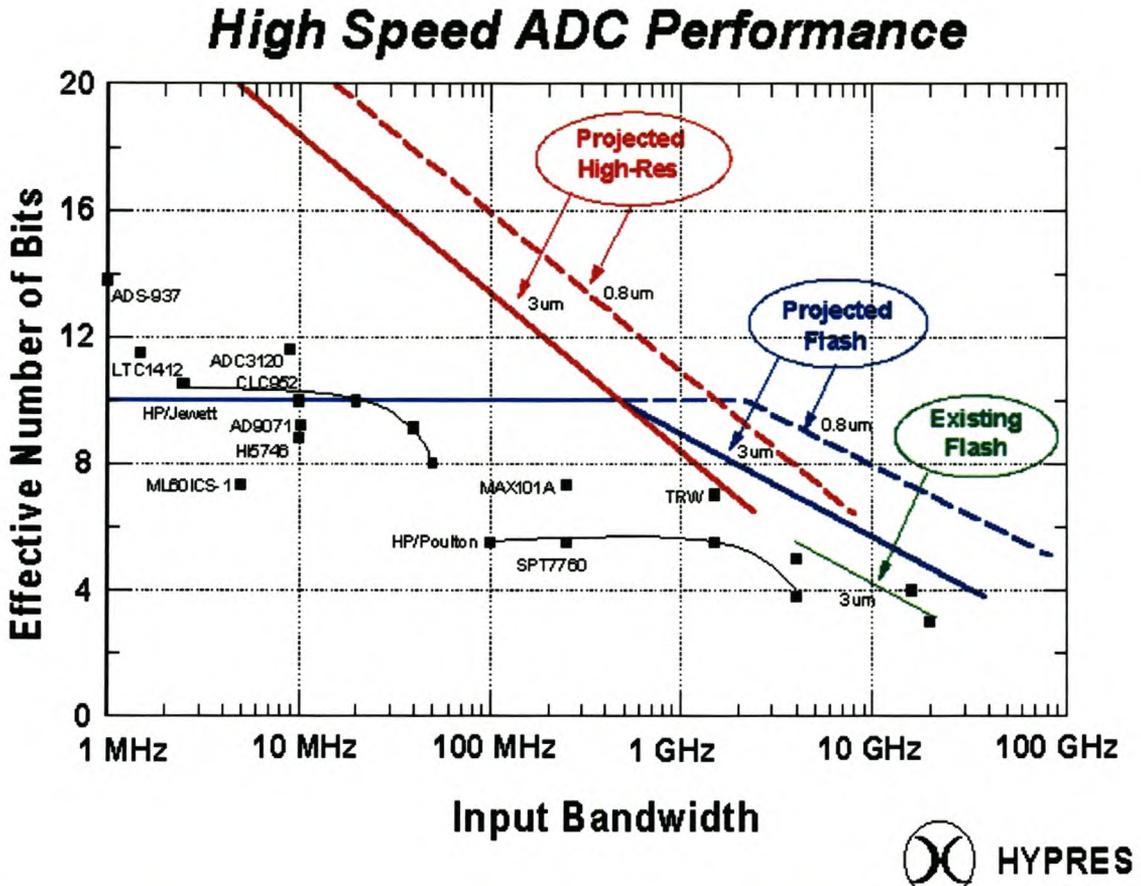


Fig. 1.3 Graphical presentation of the existing performance and the projected performance of high speed ADCs in terms of effective number of bits as a function of input bandwidth. Reproduced with permission from Hypres.

1.3 The Scope of this Study

This dissertation investigates a new design for a superconductive comparator for a high input bandwidth superconductive ADC. Contributions are made in utilizing WRSpice simulations and yield predictions to optimize the comparator circuit. The dissertation presents the following major contributions:

1. A new and novel superconductive switching logic comparator.
2. The design of a switching logic COSL compatible, high input bandwidth ADC.

The new comparator has the following advantages over other comparator designs:

- The comparator has a voltage state, switching logic output.
- The comparator output is COSL compatible and can be processed at clocking speeds greater than 18 GHz.
- This comparator was designed and optimized utilizing the Monte Carlo Method, implemented in WRSpice.
- The aperture time for the comparator is defined by the rise time of the sampling pulse and not the pulse width. The sub-picosecond aperture time provides for an ADC with a possible 5 bits of resolution at 15 GHz input bandwidth.
- The comparator does not suffer from threshold distortions and is not limited by a maximum number of useful transitions.
- The comparator design incorporates trim facilities, which make it possible to trim a non-functional comparator circuit to a fully functional comparator.

1.4 Layout of Dissertation

The dissertation has the following structure. The current Chapter serves as an introduction to the field and scope of this study. Chapter 2 provides a detailed discussion on the basic elements and building blocks of superconductive electronic circuits. These include the Josephson junction, one-junction SQUID, quasi-one-junction SQUID and the two-junction SQUID. It further discusses the new COSL family of logic gates. Lastly the subject of superconductive ADCs is discussed with special reference to the superconductive flash ADC and the use of the Quasi-One-Junction SQUIDS (QOJS) as a high speed comparator.

A summary from the study of the literature is given in Chapter 3. It also provides an insight into the design philosophy and the strategy followed in the process to arrive at a solution for the problem. The different routes that were followed and avenues that were investigated, are discussed. A novel idea for a superconductive switching logic comparator is then presented together with the design of all its building blocks. The introduction of trim facilities to be able to improve the number of functional comparator circuits, is discussed.

Chapter 4 deals with the WRSpice [40] simulations of the designed circuit. A Monte Carlo method is implemented in WRSpice. These WRSpice simulations incorporate an estimate of the manufacturing process tolerances in order to optimize and predict the yield for this design. Included in this Chapter are the incorporation of the trim facilities into WRSpice and the procedure to test the functionality of the comparator.

A superconductive flash ADC consists of a number of comparators and a data converter to convert the Gray code output from the comparators into Binary code. Chapter 5 presents the

design of a Gray-to-Binary converter and finally a complete 4-bit ADC. The correct simulated low frequency and high frequency operation of the complete ADC is shown in this Chapter.

The dissertation is concluded in Chapter 6 with an overview of the results and a discussion of future research and extensions to the presented work.

■ **Summary**

In this Chapter a broad overview was given of the basic types of ADCs and what distinguishes them from each other. Where possible, performances that have been achieved to date and advantages and disadvantages of the different types of ADCs were discussed.

A general overview and layout of the dissertation were given to provide to the reader an initial framework within which to view the detailed work that will follow.

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Theoretical and Conceptual Foundations

- **Introduction**
- 2.1 **The Josephson Junction**
- 2.2 **The One-Junction SQUID**
 - 2.2.1 Static Characteristics
 - 2.2.2 Switching Characteristics
- 2.3 **The Quasi-One-Junction SQUID**
- 2.4 **The Two-Junction SQUID**
- 2.5 **The Complementary Output Switching Logic Family**
- 2.6 **Analog-to-Digital Conversion and the Flash ADC**
 - 2.6.1 The Analog-Digital Conversion Process
 - 2.6.2 Figures of Merit for ADCs
 - 2.6.3 The Superconductive Flash ADC
 - 2.6.4 The QOJS and the Flash ADC
- **Summary**

■ Introduction

Superconductive circuits based upon Josephson Junctions have a number of advantages that can be applied to ADC circuits.

The building blocks of such superconductive Josephson circuits are the Josephson junction, one-junction and two-junction Superconducting Quantum Interference Devices (SQUIDs). This Chapter will cover the fundamentals of these devices to provide the necessary understanding when they are utilised to construct other functional circuits such as comparators, converters and Complementary Output Switching Logic (COSL) gates.

2.1 The Josephson Junction

Josephson junctions can be produced by a number of techniques that include superconductor-insulator-superconductor (SIS) structures, weak link (point contact, micro bridge) and the more recent grain boundary for high T_c superconductors. Fig 2.1 illustrates the mentioned techniques.

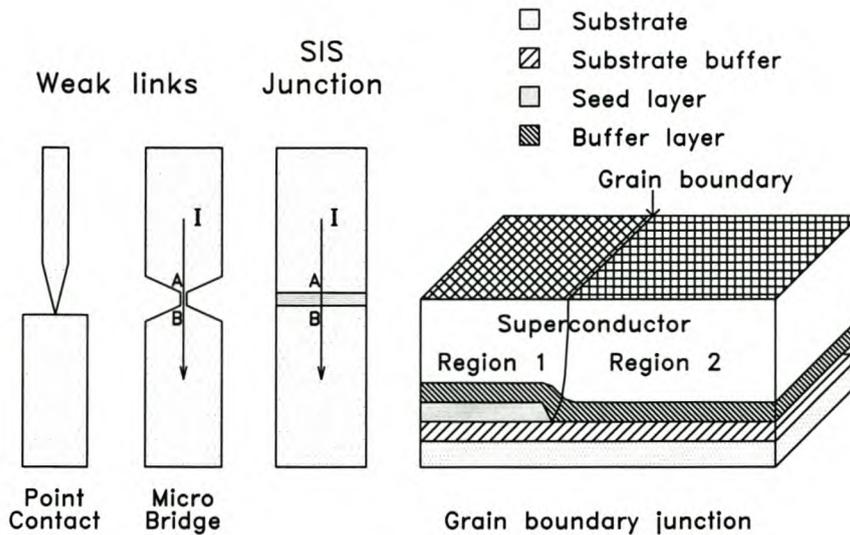


Fig. 2.1 Different structures for Josephson junctions.

Josephson [1] discovered that the probability for a Cooper pair to tunnel through an insulating barrier such as in the SIS junction corresponded to that for a single electron. He then predicted that Cooper pairs would tunnel through the junction without any voltage across the junction. This current at zero voltage is known as the Josephson current and the phenomenon is known as the *DC Josephson effect*. This Josephson current exhibits a limit to the amount of current that the tunnelling Cooper pairs can sustain to maintain zero voltage across the junction. This maximum current is known as the Josephson *critical current density* J_c . If the applied current exceeds J_c a voltage will develop across the junction.

Josephson junctions can be considered to fall into two categories, namely the basic junction and the generalized junction. When the current through the junction is restricted to less than the critical current, I_c , it is considered to be a basic Josephson junction.

When I_c is exceeded the junction is generalized and resistive and capacitive channels have to be included in parallel to the basic channel to accommodate the excess current flow. This junction is then referred to as a generalized Josephson junction.

Fig 2.2 represents the i-v curve of a typical Josephson junction.

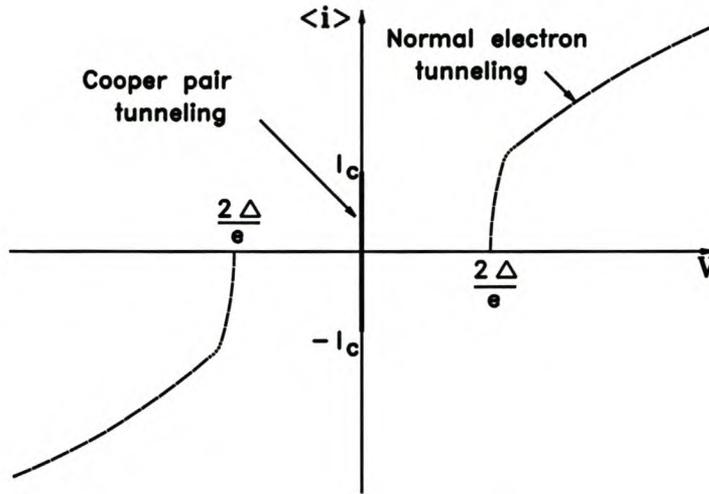


Fig. 2.2 The i-v curve for a typical Josephson junction.

An expression for the Josephson tunnelling current can be derived by employing the equations of Ginsburg and Landau [2, pp. 393-405] when it is assumed that no flux threads the junction. The current-phase relationship is given by

$$i = I_c \sin \varphi \quad (1)$$

where I_c is the critical current of the junction and φ is the gauge invariant phase. With reference to the current in Fig. 2.1, φ is defined as

$$\varphi = \varphi_A - \varphi_B - \frac{2\pi}{\Phi_0} \int_A^B \mathbf{A} \cdot d\mathbf{l} \quad (2)$$

A detailed derivation of (1), the current-phase relation, was performed in [4, pp. 145-150] and [5, pp. 93-95]. The voltage-phase relationship is obtained by the time differentiation of (2) and expressed as

$$\frac{\partial \varphi}{\partial t} = \frac{2\pi}{\Phi_0} v \quad (3)$$

It can be seen from (1) and (2) that for a constant current through the junction, φ will be a constant and for φ constant, the voltage across the junction will be zero. It is thus possible for a current to flow through the junction without a voltage being generated across the junction. If a constant voltage V is now applied across the junction, the phase difference across the junction becomes a function of time and the current will oscillate.

This phenomenon in turn is known as the *AC Josephson effect* and is related to the *Josephson frequency* given by

$$f_J = \frac{v}{\Phi_0} = \frac{|q^*|}{h} v = 483.6 \times 10^{12} v \quad [\text{Hz}] \quad (4)$$

where $q^*=2e$, and $e=1.6022 \times 10^{-19}$ C and $h= 6.6262 \times 10^{-30}$ J-s and Φ_0 the flux quantum. A schematic of a generalized Josephson junction is shown in Fig 2.3.

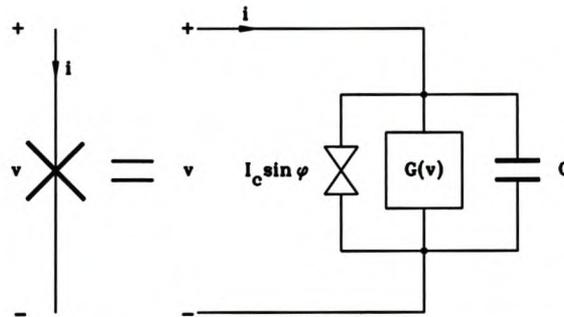


Fig. 2.3 A model of a generalized Josephson junction and its equivalent symbol

According to Kirchhoff's current law the total current for the three channels can be expressed as

$$i = I_c \sin \phi + v G(v) + C \frac{\partial v}{\partial t} \quad (5)$$

where $G(v)$ represents the conductance of the normal tunnelling channel and C the capacitance of the junction. The current through the junction is thus governed by a nonlinear differential equation.

Utilizing the voltage-phase relation in (3) and simplifying the model by replacing the voltage dependent conductance by the reciprocal of a constant resistance we obtain the resistively shunted junction (RSJ) model.

2.2 The One-Junction SQUID

2.2.1 Static characteristics

The one-junction SQUID (OJS) can be modelled by a Josephson junction and an inductor in parallel. This equivalent circuit is shown in Fig. 2.4.

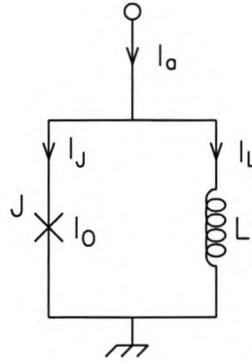


Fig. 2.4 Equivalent circuit of the one-junction SQUID.

The one-junction in Fig. 2.4 can be described by

$$\phi_a = \phi_J + \beta_L \sin \phi_J \tag{6}$$

where $\phi_J = \sin^{-1}(I_J/I_0)$ is the phase across the junction J with a critical current of I_0 , $\Phi_a = 2\pi LI_a/\Phi_0$, and $\beta_L = 2\pi LI_0/\Phi_0$. The behaviour of the device depends on the value of β_L : for $\beta_L > 1$ the SQUID flux state is hysteretic and for $\beta_L < 1$ the SQUID flux state is non-hysteretic. Fig. 2.5 shows the two flux states, where $\Phi_a = LI_a$ is the applied flux and Φ the included flux.

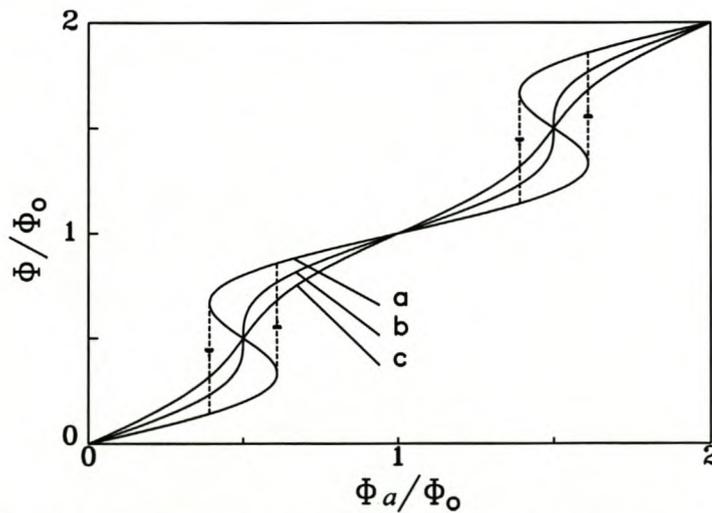


Fig. 2.5 Normalized relationship between Φ and Φ_a for different values of LI_0/Φ_0 : a) $1/\pi$ (hysteretic), b) $1/2\pi$ (at transition), c) $1/4\pi$ (non hysteretic). The dotted lines indicate the 0-1 and 1-0 flux transitions in the hysteretic state.

The current, I_a , through the OJS can also be written as

$$i_a = I_0 \sin \phi_J + i_L \quad (7)$$

Utilising the voltage-phase relationship, I_a can now be expressed in terms of the inductor current i_L as shown in (8).

$$i_a = I_0 \sin \left(\frac{2\pi L i_L}{\Phi_0} \right) + i_L \quad (8)$$

In the hysteretic state, this can be graphically illustrated in Fig. 2.6

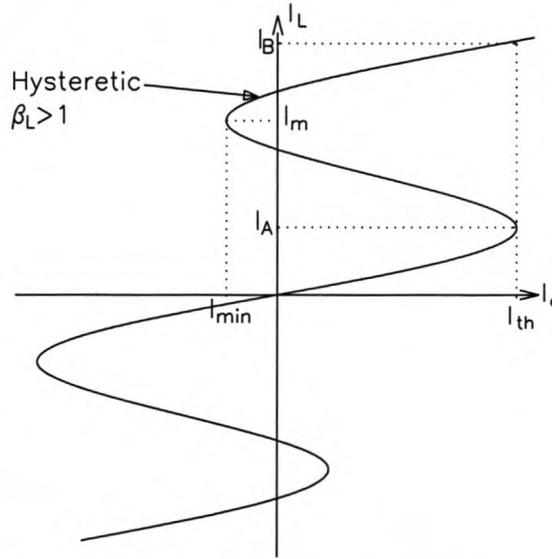


Fig. 2.6 The inductor current vs applied current for a hysteretic OJS

The value of I_a where the SQUID jumps to the next quantum state is called the threshold current, I_{th} . For input current less than I_{th} , the OJS is in the zero-flux quantum state. At point A, where the input exceeds I_{th} , one flux quantum enters the OJS loop, the OJS will jump to the one-flux quantum state and the current through the inductor will jump from I_A to I_B . The input current now has to be reduced below I_{min} before the OJS will revert back to the zero-flux quantum state. The current through the inductor, just before the transition is given by I_m . Derivations for these equations are given by Van Duzer[3].

By setting the derivative of (7) with respect to i_L equal to zero, an expression for i_L at the maximum can be obtained. Substituting this expression back into (7), yields the expression for the threshold current given by

$$I_{th} = I_0 \sin \left[\arccos \left(- \frac{1}{\beta_L} \right) \right] + \frac{I_0}{\beta_L} \arccos \left(- \frac{1}{\beta_L} \right) \quad (9)$$

where

$$\beta_L = \frac{2\pi LI_c}{\Phi_0} \quad (10)$$

The currents for I_A , I_B , I_m and I_{min} can be calculated using the following expressions:

$$I_B = I_m + \frac{I_A}{I_{th}} (I_{th} - I_{min}) \quad (11)$$

$$I_A = I_C \frac{\cos^{-1}\left(\frac{-1}{\beta_L}\right)}{\beta_L} \quad (12)$$

$$I_{min} = I_C \frac{2\pi}{\beta_L} - I_{th} \quad (13)$$

$$I_m = I_C \frac{2\pi - \cos^{-1}\left(\frac{-1}{\beta_L}\right)}{\beta_L} \quad (14)$$

2.2.2 Switching Characteristics

Knowledge about the switching characteristics of the OJS is required in the design of the pulser circuit and is used in the calculation of the rise-time, pulse width and the magnitude of the pulse. The circuit for a OJS used for calculating the switching characteristics is shown in Fig. 2.7.

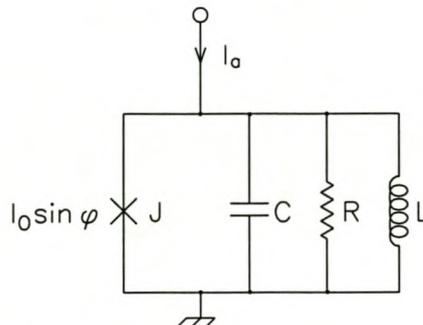


Fig. 2.7 The OJS circuit used in calculating its switching characteristics

When the Josephson Junction is treated as a nonlinear inductor, the OJS can be approximated by an equivalent parallel RLC network, characterized by the equation

$$s^2 + \frac{1}{R_{eq} C_{eq}} s + \frac{1}{L_{eq} C_{eq}} = 0 \quad (15)$$

and the 10%-90% rise time of this second order system can be approximated [39] as

$$t_{rise} = \frac{1 + 1.1\xi + 1.4\xi^2}{\omega_n} \quad (16)$$

where $R_{eq} = R$, $C_{eq} = C$, ξ the damping factor, ω_n the oscillation frequency and

$$\xi = \frac{1}{2R_{eq}} \sqrt{\frac{L_{eq}}{C_{eq}}}, \quad \omega_n = \frac{1}{\sqrt{L_{eq} C_{eq}}} \quad (17)$$

The Josephson junction behaves much like a current-source switch during the zero to one and the one to zero flux quantum transitions and for this reason the L_{eq} can be set equal to L . For critical damping, $\xi=1$, the damping resistor is given by

$$R = \frac{1}{2} \sqrt{\frac{L}{C}} \quad (18)$$

However, this is not the case for the underdamped OJS ($\xi < 1$). The Josephson junction now behaves like a nonlinear inductor rather than a current switch. The equivalent inductance, L_{eq} , is now represented by parallel combination of L and the junction small-signal inductance L_{JO} . L_{JO} is given by

$$L_{JO} = \frac{\Phi_0}{2\pi I_c \cos \phi_f} \quad (19)$$

where ϕ_f is the junction phase in the steady state. In most practical designs, however ξ is chosen to be 1 for critical damping. From the above equations it can be seen that, in practice, with a limit on the smallest inductor that can be fabricated, narrower pulses can only be obtained by utilizing Josephson junctions with higher critical current densities and smaller junction capacitances.

A sudden change in the current stored in the inductor of a OJS, such as in a flux quantum transition, the voltage across the inductor will change according to $V=LdI/dt$. The voltage waveform will therefore be of the form of a pulse.

Luong [8] and Ko [15] assume that the base width of the pulse is equal to the rise time and define the pulse width as follows:

$$t_{pw} = \frac{1}{2} t_{base} = \frac{1}{2} t_{rise} \quad (20)$$

The magnitude of the voltage pulse can be expressed in terms of the total phase change across the junction, $\Delta\phi$, when the OJS experience a zero to one flux quantum transtion. The total phase change is given by

$$\Delta\phi_{0\rightarrow 1} = \frac{2\pi L \Delta I_L}{\Phi_0} = \beta_L \frac{\Delta I_{L_{0\rightarrow 1}}}{I_c} \quad (21)$$

where ΔI_L is the change in the inductor current and V_L the voltage across the inductor. The pulse peak amplitude is now estimated as

$$V_{peak} \approx \frac{\Phi_0 \Delta\phi}{2\pi t_{pw}} = \frac{L \Delta I_L}{t_{pw}} \quad (22)$$

2.3 The Quasi-One-Junction SQUID

In order to sample or sense the current through the Josephson junction of the one-junction SQUID in Fig. 2.4, an additional junction, called the sampling junction, has to be inserted into the loop of the one-junction SQUID [15]. The sampling junction behaves much like a short circuit until the instant when sampling takes place. The equivalent circuit for the quasi-one-junction SQUID (QOJS) is shown in Fig. 2.8.

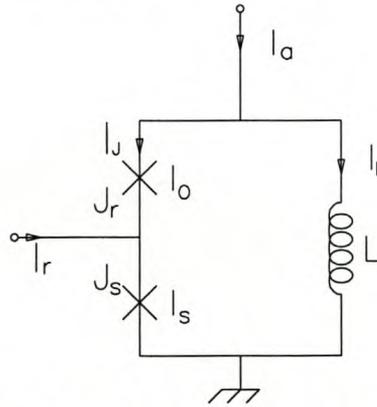


Fig. 2.8 Equivalent circuit of the quasi-one-junction SQUID.

The characteristics of the QOJS can be described by an equation similar to (6) for the OJS when the critical current I_s of the sampling junction is large compared to I_0 . It can be shown that the equation defining the QOJS threshold, simplified to the first order in I_0/I_s , corresponds to (23)

$$\phi'_a = \phi_J = \beta'_L \sin \phi_J \quad (23)$$

with

$$\beta'_L = \beta_L + \frac{1}{\sqrt{1 - (I_r / I_s)}} \left(\frac{I_0}{I_s} \right) \quad (24)$$

and

$$\phi'_a = \phi_a - \sin^{-1}\left(\frac{I_r}{I_S}\right) \quad (25)$$

where I_r is the reference current for the sampling junction. The condition for no hysteresis for the QOJS is now given by $\beta'_L < 1$. The application of the QOJS as a comparator circuit will be discussed later in Section 2.6.4.

2.4 The Two-Junction SQUID

A two-junction SQUID (2JS) is formed when two Josephson junctions are inserted into a superconductive loop. The equivalent circuit for a symmetrical 2JS is shown in Fig. 2.9. The control current I_{con} is inductively coupled to the 2JS loop with a mutual inductance M . Alternatively, the control current can also be directly injected into the SQUID loop. In most applications the gate current I_G (also referred to as bias current I_B) is coupled directly to the 2JS loop and the control current inductively. A complete theoretical analysis of the 2JS was done by Powell [38].

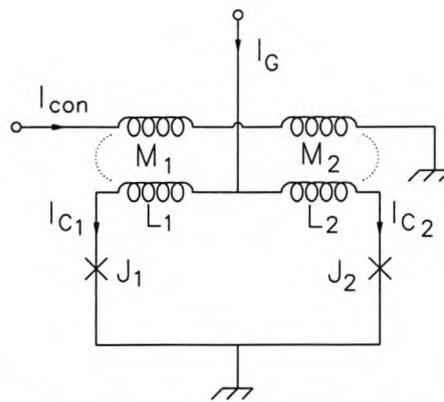


Fig. 2.9 Equivalent circuit for a two-junction SQUID with an inductively coupled control current.

When a symmetrical 2JS is cooled to its superconductive state with no externally applied magnetic field, the bias current I_G will divide equally among the two parallel paths. No voltage will be generated across the junctions as long as the current in each parallel path does not exceed the critical current of the junctions J_1 and J_2 . If the bias current becomes larger than $2I_C$ superconductivity is destroyed in the loop and an alternating voltage will be generated across the junctions. If an external magnetic field I_{con} is applied, a circulating current will be generated in the loop which will try to cancel the flux included by the loop. The magnitude of the applied dc current I_G , which will force the loop to its normal state, will thus be smaller due to the addition of the circulating current in the loop.

The behaviour of a symmetrical 2JS is characterised by its threshold curve. The threshold curve relates the maximum gate current, I_{Gmax} , to the control current, I_{con} . I_{Gmax} is the maximum gate current allowed by 2JS for a given control current, before switching from the superconductive state to the voltage state and diverting current to any external load connected to the 2JS at the point where I_G is injected into the 2JS loop.

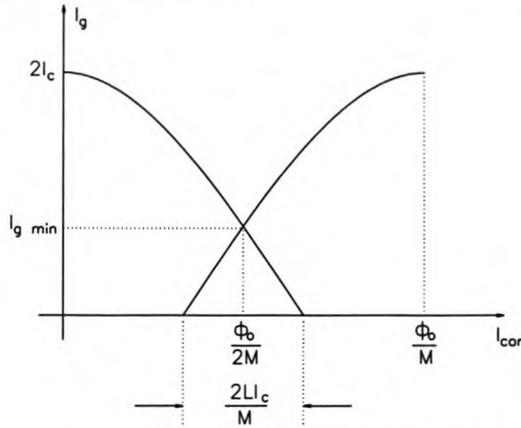


Fig. 2.10 Threshold curve for a symmetrical two-junction SQUID showing the boundaries between the superconductive and the resistive(voltage) states.

A typical threshold curve for the symmetrical 2JS with inductor values $L_1 = L_2 = L/2$, mutual inductance values $M_1 = M_2 = M/2$ and junction critical currents $I_{C1} = I_{C2} = I_C$, is shown in Fig. 2.10. This threshold curve is periodic with respect to I_{con} with a period of Φ_0/M and will therefore repeat for other values of I_{con} . Further, the two lobes in the threshold curve overlap by $2LI_C/M$. The minimum gate current, I_{Gmin} , with which the SQUID will switch to the voltage state is at the intersection of the two threshold curves. When I_{Gmin} takes on the value of I_C , which corresponds to a 50% modulation of the maximum gate current, it results in $LI_C \approx 0.5\Phi_0$.

A non-symmetrical 2JS is shown in Fig. 2.11 . If we consider the example by Fujimaki *et al* [36], it consists of Josephson junctions J_1 and J_2 , and inductance L . The critical current of J_1 is pI_m and that of J_2 is qI_m , where $p+q = 1$. The inductance is magnetically coupled to L_x through the mutual inductance M . The bias current I_b is injected into the point between the right branch inductance pL and the left inductance branch qL and together with specific ratio of p and q ensures that the maximum bias current is always I_m .

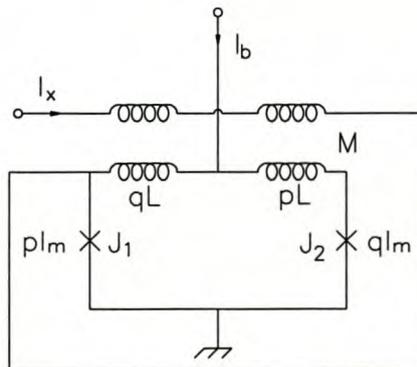


Fig. 2.11 The non-symmetrical 2JS of Fujimaki.

The current through J_1 and J_2 is represented by $pI_m \sin \phi$ and $qI_m \sin \phi$, respectively. The non-symmetrical 2JS can then be characterized by using Kirchoff's current law, expressed as

$$I_b + I_x = pI_m \sin \phi_1 + qI_m \sin \phi_2 \quad (26)$$

and the quantum condition around the 2JS loop,

$$\phi_1 + \phi_2 = \frac{2\pi\Phi}{\Phi_0} + 2\pi n \quad (27)$$

where ϕ_1 and ϕ_2 are the quantum phases across the junctions and Φ the applied flux. This equation expands to

$$\phi_1 + \phi_2 + \frac{2\pi}{\Phi_0} [qL(pI_m \sin \phi_1 - I_x) - pLqI_m \sin \phi_2 - MI_x] = 2\pi n \quad (28)$$

Fujimaki has used (26) and (28) to solve for the threshold curve where n is an integer and represents the mode number and Φ_0 represents the flux quantum (2.0679×10^{-15} Wb). Further, the normalized inductance is given by

$$\lambda = \frac{LI_m}{\Phi_0} = 1 \quad (29)$$

2.5 The Complementary Output Switching Logic Family

This superconductive voltage state logic family, Complementary Output Switching Logic (COSL), was proposed by Perold *et al.* [6]. COSL, based on the work of Fang [7] and Luong [8], was designed to operate in the 5-10 GHz clock frequency range with increased reliability and versatility over previously proposed logic families. This work was a phenomenal breakthrough in the field of superconducting logic circuits. The experts in this field were convinced that the superconducting voltage state logic would never reach these clock frequencies. Perold *et al.* [34] exceeded his initial achievements. Currently COSL elements have been tested to correctly operate at clock frequencies as high as 18 GHz [35]. This represents the upper limit of available test equipment.

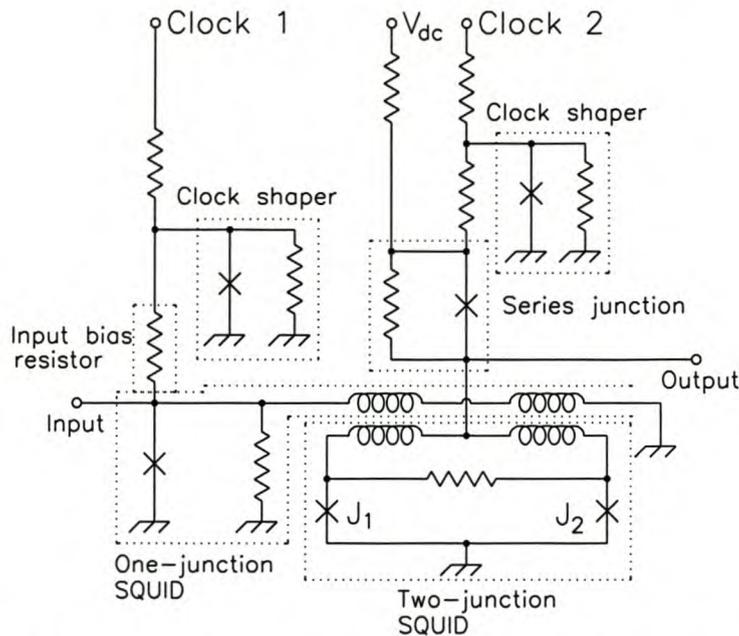


Fig. 2.12 The basic COSL gate from Perold *et al* [6] indicating the relevant sub circuits.

The basic COSL gate is shown in Fig. 2.12. The COSL gate consists of a one-junction SQUID input, a two-junction SQUID output, clock shaper and a series Josephson Junction. COSL employs a three-phase clocking scheme where all three clocks are 120° out of phase with each other. The function of the clock shaper is to clamp the clocked bias from the clocks to a constant 2.5 mV for the input and output stage when driven by a nominal clock amplitude of 10 mV. This is obtained as the Josephson junction from the clock shaper switches to the gap voltage when the current from the clock exceeds the critical current of the clock shaper junction. The series junction is paramount in obtaining the complementary outputs of the AND and OR COSL gates, depending whether it is placed above or below the output SQUID. The XOR COSL gate is obtained by inserting a Josephson junction in series with the input of an OR gate.

AND/NAND gates are designed to switch for a nominal input current of $200 \mu\text{A}$, but not for $100 \mu\text{A}$. The OR/NOR gates, however, have to switch for a nominal input current of $100 \mu\text{A}$ as well as a nominal input of $200 \mu\text{A}$. This is accomplished by using different bias resistors for the input SQUIDs. All gate outputs are designed to deliver 1 mV into 5Ω or $200 \mu\text{A}$.

The XOR gate, however, due to the $300 \mu\text{A}$ series junction are designed for two nominal inputs of $200 \mu\text{A}$ each. This will cause the series junction to switch and to cut the input off, producing the zero output with the correct clocking sequence. The XOR gate can therefore also perform a buffer or inverter function depending on the input. The buffer function is achieved if there is only one input to the gate and the invert function when one input of the two inputs is kept high. A detailed description of COSL operation is given in Reference [6].

2.6 Analog-to-Digital Conversion and the Superconductive Flash Analog-to-Digital Converter

2.6.1 Analog-to-Digital Conversion Process

The reader of this Section may already be familiar with the subject of Analog-to-Digital Conversion, however, as a matter of completeness, it is included in this Section.

Analog-to-digital converters are the vital links between the analog and the digital worlds when it is necessary to acquire analog data by digital computers. The input to the ADC is a continuous value input while the output is discrete or quantized levels. The resolution of the ADC is determined by the number of levels or the degree of quantization where the first level is called the Least Significant Bit or in short LSB. The number of levels is expressed as a power of 2, eg. 2^n where n indicates the resolution of the ADC in number of bits.

To digitally characterize an analog signal, it is necessary to sample it at specific time intervals and to obtain the value of the analog signal at that time. To ensure that an analog signal can again be reconstructed from the sampled data, it is necessary to sample the analog signal at least twice the analog signal bandwidth. This constitutes the sampling or Nyquist theorem. The number of AD conversions that can be performed in a given time interval is known as the sampling or clock rate.

The output of an ADC is usually encoded in Binary code, Gray code or BCD code, which can be readily interpreted by the digital computer. Due to the architecture, Gray code often finds application in superconductive ADCs and belongs to a class of codes referred to as “minimum-change codes”, in which only one bit in the code group changes when going from any level to the next. In Binary anything from one to all the bits can change in going from one level to the next.

A block diagram of the AD conversion process is given in Fig. 2.13.

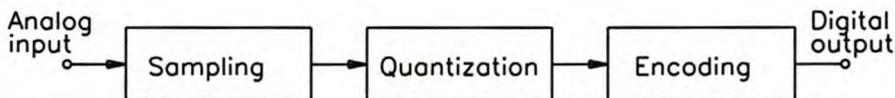


Fig. 2.13 Block diagram of the analog-to-digital conversion process.

Practical ADCs cannot perform the sampling process in zero time. The finite time required to perform this function is called the aperture time, t_{ap} . To ensure that the ADC resolution is not exceeded, the input signal is not allowed to change by more than one LSB during the aperture time. For this reason the aperture time is directly related to the analog signal bandwidth.

If we consider a sinusoidal signal of $\sin 2\pi f_B t$, the maximum slew rate is given by $2\pi f_B$. Where f_B is the signal bandwidth. For this signal to slew an amount of one LSB, a minimum time of $2/2^n 2\pi f_B = 1/2^n \pi f_B$ is required and the aperture time now has to satisfy the inequality [15].

$$t_{ap} \leq \frac{1}{2^n \pi f_B} . \quad (30)$$

The aperture time thus provides us with a measure of how well an ADC can sample the input signal. The smaller t_{ap} , the more accurate can the comparator sample the input signal and the higher the performance and input bandwidth achieved by the ADC.

The output of an ADC can only take on discrete values. This will inherently cause error, known as quantization error, in the conversion from the analog signal. Assuming that sampling takes place in the middle of the aperture time interval and that the input signal increases linearly, Fig. 2.14(a) shows the quantized output for an ideal ADC and Fig. 2.14(b) the quantization error.

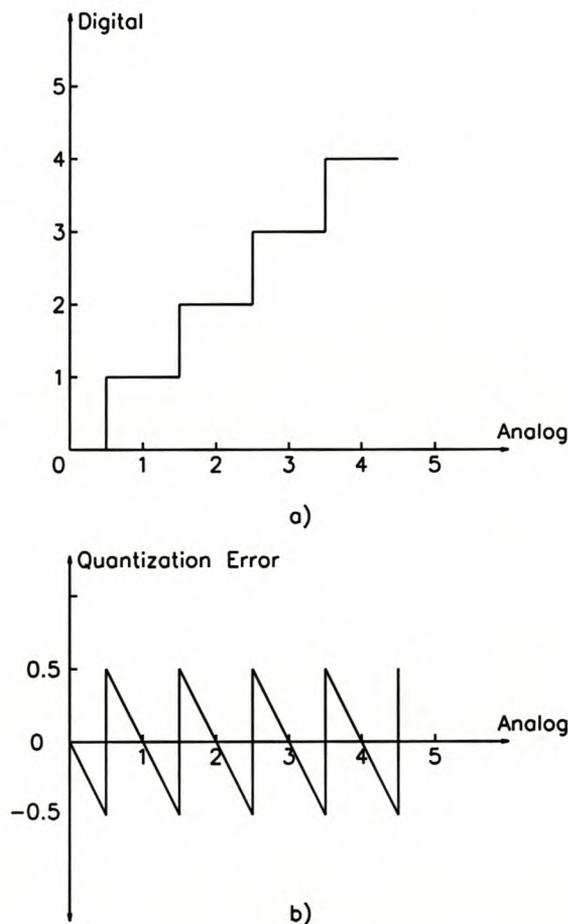


Fig. 2.14

a) The quantization characteristics and
b) the quantization error versus analog
input of an ideal ADC.

2.6.2 Figures of Merit for ADCs

According to Fang [7], if the analog signal has equal probability of reaching any signal level, then the quantization error has an average rms value of $q/\sqrt{12}$ where q is the quantization step or one LSB. An ideal n -bit converter will have a signal to error ratio (SER) of

$$SER_{ideal} = \frac{2^n}{\sqrt{12}} \quad (31)$$

The quantization function could in principle apply for arbitrarily large magnitude of analog input signals, but the quantizer in practical ADCs exhibit a maximum value or saturation level A_{sat} . The dynamic range of the quantizer is then given by

$$R_{dynamic} = \frac{A_{sat}}{q} \quad (32)$$

A practical ADC will have additional error due to circuit limitations and imperfections. Sources of such error could be the finite time response of circuits and fabrication related device mismatches causing the transitions between levels not to be as evenly spaced as in Fig 2.14(a). Under dynamic conditions the situation may arrive where the circuit cannot respond fast enough and cause uncertainties in the transitional points between levels. This is graphically illustrated in Fig. 2.15.

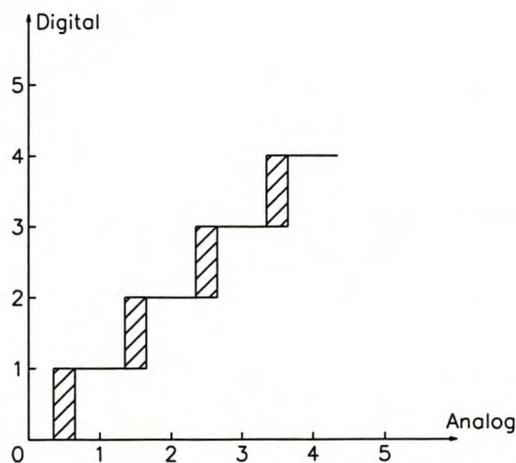


Fig. 2.15

Uncertainties in transitions between levels (shaded area), caused by dynamic effects in a practical ADC

These uncertainties result in a practical ADC having an effective bit conversion accuracy which is less than that of the ideal ADC. The relationship between the effective bit accuracy m of an n -bit converter and the signal-to-error ratio SER is given by

$$SER = \frac{2^m}{\sqrt{12}} \quad (33)$$

where $m \leq n$, and $SER \leq SER_{ideal}$ given by (31). The SNR can be obtained from the ratio of the signal power to the total noise power by taking the Fourier spectrum of the reconstructed output of the ADC when a sinusoidal input of a fixed frequency is applied to the ADC. SER is a ratio of amplitudes - full-scale signal amplitude divided by rms error amplitude. SNR is thus the square of the SER.

The effective bit accuracy is also referred to as the Effective Number Of Bits (ENOB) and can be expressed as

$$ENOB = \frac{SER_{dB} - 1.76}{6.02} \quad (34)$$

The 1.76dB corresponds to the error level of $q/\sqrt{12}$ and to express ENOB in bits it is divided by the figure of 6.02.

Again utilizing the Fourier spectrum of the reconstructed output, the Spur-Free Dynamic Range (SFDR) is another figure of merit. It is given by the ratio of the signal amplitude to the highest spurious signal within the relevant frequency band. It can be expressed in decibels or in bits by dividing the SFDR (in dB) by 6.02.

Signal-to-Error Ratio (SER/SNR), Effective Number of Bits (ENOB), Dynamic Range (DR) and Spur-Free Dynamic Range (SFDR) are all figures of merit to help to quantify the performance of an ADC and to be able to compare it with other ADCs.

2.6.3 The Superconducting Flash ADC

There are two architectures for the superconductive flash ADC, namely the periodic-threshold type and the fully parallel type. Fig. 2.16 shows, in block diagram form, the differences between the two architectures.

The periodic-flash ADC in Fig. 2.16 (a) requires only N comparators for an ADC with a resolution of N bits. The analog input signal is applied to a resistive divide-by-two ladder where the LSB receives the largest share of the analog signal current. The next bit conducts half as much current as the previous bit, while the MSB conducts the smallest fraction of the current.

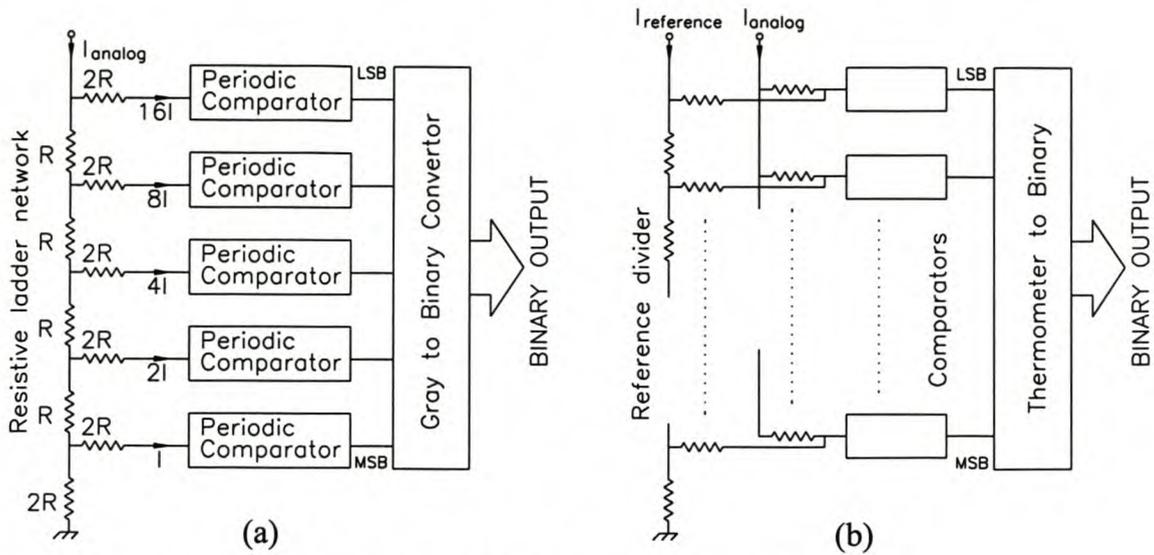


Fig. 2.16 Flash ADC architectures: a) Periodic-threshold, b) Fully parallel.

Periodic-threshold ADC comparators are usually arranged with a dc offset among the stages. This offset ensures that only one comparator will change state when the analog input signal to the comparator crosses the quantization boundary for that specific comparator. This characteristic produces a Gray-code output from the comparators. The Gray-code has the advantage that a 1-bit error in even the most significant bit comparator will only cause a 1-level error in the output of the ADC. The Gray-code can then be converted into a binary code for further processing.

The full-parallel flash ADC in Fig. 2.16 (b), however, requires $2^N - 1$ comparators to form an N bit ADC. The input analog signal is simultaneously applied to the $2^N - 1$ comparators with linearly graded thresholds to sample it and to convert it to one of the possible digital outputs. The output of the quantizer is in Thermometer-code and again needs to be converted to binary for further processing.

Although fast conversion rates can be achieved with a fully parallel ADC, the larger number of comparators required, results in a relatively large and complex circuit and requires a very large area, hardware and power consumption.

2.6.4 The Quasi-One-Junction SQUID and the Flash ADC

Zappe [31] first proposed that the intrinsic periodicity due to flux quantization in two or three junction SQUIDs can be utilized to design ADCs. It has since been exploited by many researchers [28, 29] in several designs of flash ADCs. Fang [7] and Luong [8] designed a fully parallel flash ADC using hysteretic one-junction SQUIDs and $2^N - 1$ comparator circuits in a conventional architecture.

Although all the simulations and experiments show that these devices can operate at a very high sampling rate f_s , the analog signal bandwidth were far below the $1/2 f_s$ limit imposed by the Nyquist sampling theorem. Most of these designs were limited in speed by dynamic distortions of the SQUID threshold curve shown by Kautz [30].

Ko [32,15] proposed the use of a low-inductance non-hysteretic ($\beta_L < 1$) OJS for his comparator circuit. This circuit relies on the periodic transfer function $I_J(I_a)$ of the low-inductance non-hysteretic OJS for its operation. The flux applied to the SQUID is given by $\Phi_a = LI_a$. For values of $\beta_L < 1$ the transfer function $I_J(I_a)$ is single valued. The continuous transition of I_J in the OJS eliminates the hysteresis problems and abrupt transitions experience with hysteretic OJS, two-junction and three junction SQUIDs, resulting in much less dynamic distortion. The operating principle and the transfer function for the OJS has already been discussed in Section 2.2. Fig. 2.17 shows the use of the OJS for a periodic comparator.

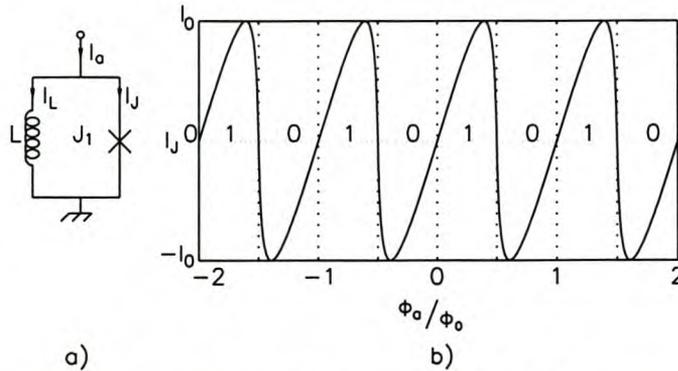


Fig. 2.17

a) Equivalent circuit of a OJS. b) The use of a non-hysteretic OJS transfer function for a periodic-threshold comparator.

The junction response time is approximately the lower limited of the comparator aperture time t_{ap} , given by (30). Eliminating the hysteresis problem, it may be possible to achieve a frequency response close to the limit set by the junction response time. Ko showed through simulations that a response time of approximately 1 ps can be achieved in a sampler using high critical current density junctions with capacitance-to-critical-current ratio of $C/I_C = 0.5$ pF/mA ($J_C \approx 10$ kA/cm² for Nb-Al-Al₂O₃-Nb junctions) which translates to sampling rates of 20 GHz and an analog signal bandwidth of at least 10 GHz. Wolf [33] *et al* also reported a 2.1 ps sampler.

The complete comparator circuit proposed by Ko is given in Fig. 2.18. It consists of a QOJS, a pulse generator and a clock circuit that provides a reference current input. Again the operation of the QOJS is described earlier in Section 2.3.

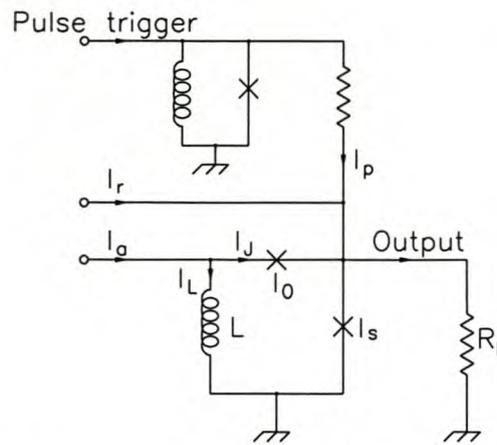


Fig. 2.18 The complete OJS comparator proposed by Ko.

In the circuit above, the quantizing current I_J , a fixed bias or reference current I_r , and a very short pulse I_p are summed at the sampling junction. This junction acts as a threshold and should the sum of the currents exceed the critical current I_s of the sampling junction at any time, the sampling junction switches and remains switched. The reference current is adjusted so that the sampling junction has a 50% probability of switching when the pulse from the pulse generator is applied in the absence of an analog input signal. In the event of I_J being positive as a result of the applied analog input I_a , at the time the pulse is applied, the sampling junction will switch to the voltage state and generate an output current through the load resistor R_L . Alternatively, if I_J is negative, the sampling junction will not switch and remain in the zero-voltage state.

This circuit by Ko also has the added advantage of allowing the construction of an N-bit ADC with only N comparators with several advantages over the full-parallel ADCs. This analog-to-digital conversion is inherently a linear conversion and in addition the complexity and power dissipation is reduced as well as the required analog input signal level.

Bradley [17, 18] improved on the work of Ko and pointed out three areas of importance. First, special care must be taken during the layout of the comparator to minimize the parasitic inductance of the superconducting loop formed by the OJS and the sampling junction. Secondly, to obtain high sensitivity and limit power consumption in the input resistive divider ladder network, a large L is required. Thirdly, to obtain a fast comparator that is less susceptible to noise, the smallest possible junction with the highest possible current density is required.

To solve this problem of small LI_J , large L , large I_J , Bradley proposed a high bandwidth, high current gain transformer to couple the input signal to the comparator. This allows for keeping the input signal level low while simultaneously keeping the non-parasitic part of the QJS inductance small. This transformer is required to provide good coupling from DC to many GHz.

Fig. 2.19 shows the incorporation of the transformer into the ADC.

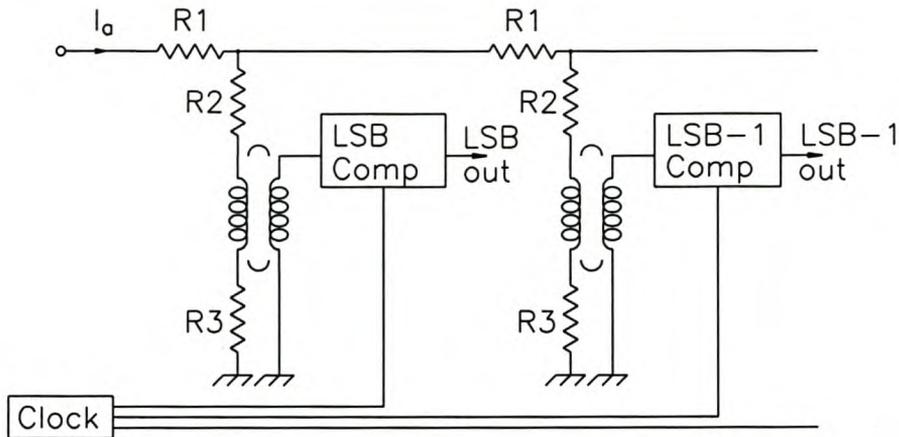


Fig. 2.19 Block diagram of the ADC with the analog input coupled through a high bandwidth transformer.

■ Summary

This Chapter provided a detailed theoretical and conceptual foundation of the basic building blocks of superconductive electronic circuits to be utilized in the design of the superconductive ADC. These building blocks include the Josephson junction, OJS, 2JS and the QOJS.

The COSL family of gates, consisting of some of the above mentioned building blocks, were discussed and how the different configurations perform the different logic functions.

The analog-to-digital conversion process was discussed and the standard figures of merit to quantify the performance of an ADC, were given. These figures of merit include SER(SNR), ENOB, DR and SFDR.

The periodic flash ADC was discussed in greater depth. It is shown how a divide-by-two ($R/2R$) resistive ladder network and the QOJS comparator were incorporated in a flash ADC. It is also important to note that the output of such an ADC is in Gray Code and that it needs to be converted to binary for further processing.

A New Approach to the Superconductive Comparator

■ Introduction

3.1 Design Philosophy

- 3.1.1 Goal
- 3.1.2 Summary from the Literature
- 3.1.3 Strategy for this Dissertation
- 3.1.4 Different Attempts to Design a High Speed Comparator

3.2 A New and Novel Idea for a Superconducting Comparator

3.3 Design of the Switching-Logic Comparator

- 3.3.1 The Pulse Generator
- 3.3.2 The Clock Shaper
- 3.3.3 The One-Junction SQUID Comparator
- 3.3.4 The Two-Junction SQUID Read-Out System
- 3.3.5 Integration of the Complete Comparator
- 3.3.6 The COSL OR-gate Buffer Stage
- 3.3.7 WRSpice Simulation of the Complete SL-Comparator
- 3.3.8 Phase Shift in the Current through the JJ of the OJS of the Comparator
- 3.3.9 Pulser Rise Time versus Pulse Width

■ Summary

■ Introduction

Following the literature study, this Chapter will set the goals for the design of a superconductive comparator and how to ultimately achieve them. All the relevant information was gathered to ascertain the current state of ADCs and where there is room for improvement. It also deals with the decisions made on how to proceed with the dissertation and the reasons why they were taken.

3.1 Design Philosophy

3.1.1 Goal

The main objective of this dissertation is to design a superconducting comparator that can be used in an analog-to-digital converter with multi-GHz input bandwidth and with the highest possible resolution. A goal of at least a 4-bit ADC with a minimum of 5 GHz input bandwidth should be obtained for the new design.

The complexity of the comparator and ADC should be kept as simple as possible. It should also be easy to integrate the comparator and ADC with the COSL logic architecture and technologies for further processing of the high speed data output.

3.1.2 Summary from the Literature

Firstly, the literature clearly shows that the latest research done by Bradley and Kaplan, based on the idea proposed by Ko, yielded the best results in the field of wideband ADCs. The following summarizes the advantages of the QOJS comparator and ADCs constructed with QOJSs:

1. Utilizing a OJS eliminates dynamic threshold curve distortions during flux state transitions generated in 2 and 3 junction SQUID comparators.
2. The QOJS comparator circuit is relatively simple.
3. Comparator allows to construct an N -bit converter with only N comparators.
4. The design is tolerant of large critical current variations.
5. This ADC architecture generates a Gray code output due to the periodic transfer function of the QOS of the comparators.
6. Demonstrated wideband operation of comparators [19, 20] in beat-frequency tests up to 30 GHz.
7. Demonstrated high speed ADC operation: 3-bit @ 8 GHz sine wave, 4-bit @ 4 GHz sine wave and 5-bit @ 2 GHz and up to 6 bits @ 10 GHz utilizing interleaving and look-back error correction techniques.

Secondly, the COSL-family of logic gates introduced by Perold *et al* [6], provides a means of processing digital data at clock speeds greater than 18 GHz (limited to 18 GHz by available test equipment).

3.1.3 Strategy for this Dissertation

The work by Bradley and Kaplan is the most relevant to our goal and was therefore studied in detail and served as a starting point for our own research and new design.

Since the output data rate of a high speed ADC will be very high, COSL gates was chosen as the architecture to be utilized in the processing of the output signal from our ADC. A Gray-to-Binary Converter is also required to convert the Gray code output from the comparator to Binary code for further processing.

It is thus required from the new design that the output of the comparators be of a switching logic nature to be COSL compatible.

3.1.4 Different Attempts in Designing a High Speed Analog-to-Digital Converter

In the quest to design a comparator many circuits and designs and combination of circuits were studied and simulated. These include hysteretic OJS, 2JSs and OJS inductively coupled to 2JSs, similar to that of Fang [7]. All these circuits and ideas did not exhibit the desired characteristics.

The QOJS comparator by Bradley [17, 18] shown in Fig. 3.1 was then analysed. Referring to Section 2.3 and Section 2.6.4, the parameter that is of interest in this design, is the current through the small junction of the QOJS. This current, as discussed in the relevant Sections mentioned above, is periodic in the applied input signal with a period given by

$$Period_{OJS} = \frac{\Phi_0}{L} [A/cycle] \quad . \quad (35)$$

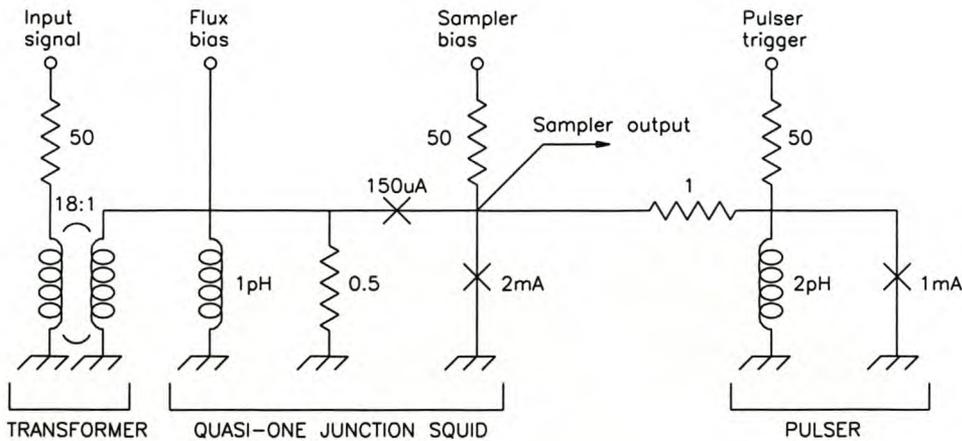


Fig. 3.1 The QOJS comparator by Bradley [18].

This current is not of a voltage state switching logic nature. To obtain a switching logic output, many circuits were investigated. Some examples are coupling the QOJS with a hysteretic SQUID to “square” the periodic output from the QOJS. The inductor of the hysteretic SQUID would then also be the inductor to couple to the read-out Section of a COSL gate in order to sample the output of the QOJS and convert it to a switching logic output. This approach was not successful due to impractical component values that were required and which would be difficult to manufacture.

3.2 A new and novel idea for a superconducting comparator

It was initially taken for granted that a symmetrical inductively coupled COSL read-out stage must be used as a read-out for the OJS. After studying the article by Fujimaki *et al* [36] on MVTL gates, the method of direct current injection into a 2JS was investigated. Two additional bias currents namely a DC bias and a clocked bias, similar to that of the COSL read-out system,

were introduced to this 2JS. A pulser circuit producing a very narrow pulse was also added to the read-out system to interrogate or sample the periodic, directly injected current from the OJS.

The novelty in the design, can be described in one of two ways. In the first, the novelty lies in that the QOJS and the 2JS read-out Section of COSL-type of architecture could be merged and integrated in a very simple circuit to form the comparator. It can be viewed that one of the Josephson junctions of the 2JS also serves as the sampling junction of the QOJS and that this junction is shared by the QOJS and the 2JS.

Alternatively, it can also be looked at from the point that the current through the series junction of the non-hysteretic OJS is injected into and sampled by the non-symmetrical 2JS. The second description will be adopted for further discussion. This design will be referred to as the switching logic comparator (SLC).

Fig. 3.2 shows the concept of the novel design of this superconductive comparator with all the sub-circuits clearly marked.

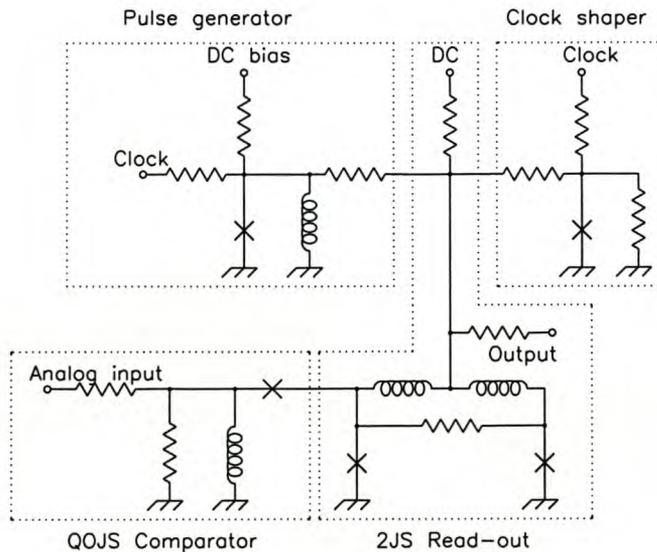


Fig. 3.2 New novel superconductive Switching Logic Comparator (SLC).

The read-out or sampler circuit consists of a 2JS, a clock shaper, a pulse generator or pulser and a DC bias circuit. The pulser provides a very narrow pulse to define the sampling instant and to comply with the requirements for the short aperture time, t_{ap} , while the clock shaper acts as a clocked bias.

This concept behind the design and its operation can be graphically illustrated through Fig. 3.3. The sinusoidal signal represents the current through the series junction of the OJS that is directly injected into the 2JS and the pulsed signal, the output of the comparator. Thresholds in the comparator are set such that it would give a pulsed output only for positive values of the current through the series junction. Alternatively it can be seen as detecting the polarity of the current from the OJS.

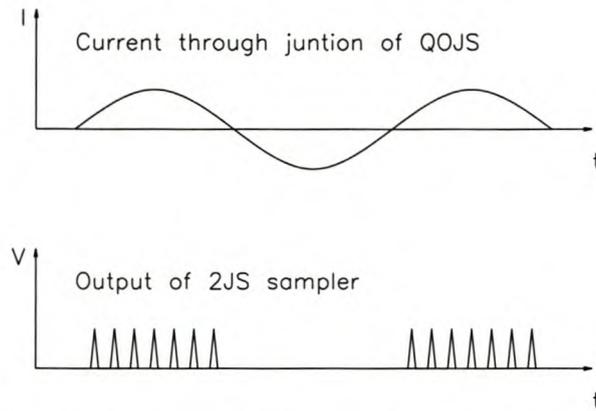


Fig. 3.3 Switching logic concept for the new comparator.

The analog input signal, with reference to Fig. 3.2, is applied to the OJS through R_1 . The periodic current through the junction, J_1 , generated as result of the applied analog input signal, is directly injected into an 2JS and sampled by the 2JS.

The threshold of the 2JS is set by the total of the sum of the currents from the pulser, clock shaper and the DC bias. The current through the series junction of the OJS, injected into the 2JS now adds to the sum of the above mentioned currents. The threshold is set to such a level that the 2JS would switch to the voltage state for positive values (see Fig. 2.17) of the periodic signal injected from the QOJS, at the instance when the narrow pulse from the pulser arrives, but not for negative values. Fig. 3.4 illustrates how the threshold is set by the sum of the DC bias, the clock shaper and the pulser.

The output from the 2JS is finally buffered by a COSL OR gate to deliver clean COSL pulses for further processing of the comparator output.

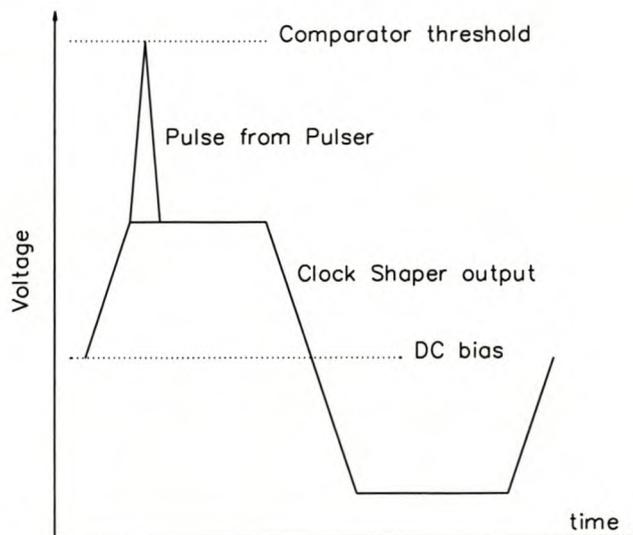


Fig. 3.4 Setup of the threshold for the SL-Comparator for no input signal

3.3 Design of the Switching-Logic Comparator

It was mentioned earlier that the initial goal is to design a 4-bit ADC with a sampling rate of 20 Giga-samples per second with a minimum of 5 GHz input bandwidth. However, the aim was to obtain the highest possible input bandwidth. The 2.5 kA process was adopted for all Josephson junctions. The following Section describes the basic design of the SL-Comparator.

3.3.1 Pulse Generator

The relationship between the analog input bandwidth and the aperture time, t_{ap} , is defined by (30). This equation states that the higher the required input bandwidth, the smaller the time, t_{ap} , in which the sampling of the analog signal has to take place. Table 3.1 provides the aperture times required for analog-to-digital conversion with respect to input bandwidth and bits of resolution. It is clear from the Table 3.1 that the required aperture time becomes very small as the resolution and input bandwidth increases.

Resolution in bits	Input bandwidth in GHz		
	5	10	15
4	3.9 ps	1.9 ps	1.33 ps
5	1.99 ps	0.99 ps	0.66 ps
6	0.99 ps	0.497 ps	0.33 ps
7	0.497 ps	0.249 ps	0.166 ps
8	0.249 ps	0.12 ps	0.083 ps

To realize these small aperture requisites for a wide analog input bandwidth, a very narrow pulse is required. A OJS with $\beta_L > 1$ is ideal for this application. The transition from zero to one flux quantum and from one to zero flux quantum, cause a positive and a negative voltage pulse respectively across the OJS. The width of the voltage pulse is typically a few picoseconds and can be utilized in small aperture sampling.

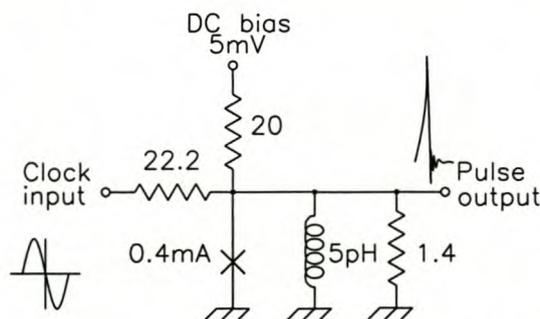


Fig. 3.5 Designed pulse generator with component values.

Fig. 3.5 shows the circuit for a OJS pulser and Fig. 3.6 illustrates how a sinusoidal clock, together with a DC bias are used to drive the OJS from zero to one flux quantum state and from one to zero flux quantum, resulting in the positive and a negative voltage pulses. This circuit has been analysed in detail by Fang [7].

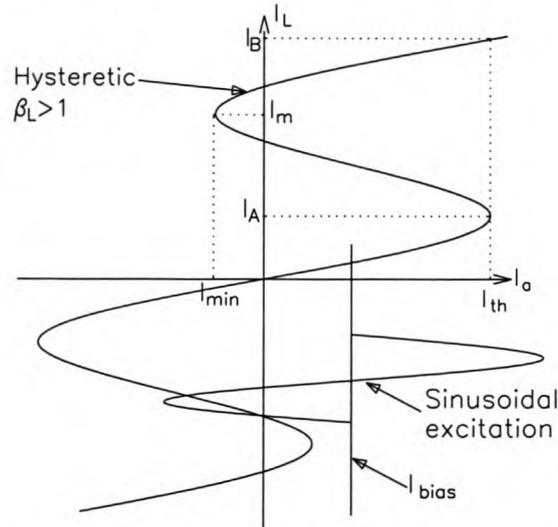


Fig. 3.6 Bias and excitation inputs to the OJS to illustrate the operation of the pulser.

The WRSpipe junction model for a JJ with a critical current of $400 \mu\text{A}$ (2.5 kA/cm^2), chosen for the JJ of the OJS, is given as follows:

* Nb 2500 A/cm2 area = 40 square microns
 .model jj2 jj(rtype =1, cct=1, icon =10m, vg =2.8m, delv =0.08m, icrit =1m, r0=30, rn =1.64706, cap =1.54894p)

The capacitance for a $400 \mu\text{A}$ junction can be calculated as $C=0.691576 \text{ pF}$. Further, it was assumed that $\xi=1$ for critical damping and $\beta=2\pi$. Using equations (9) to (22) in Section 2.2 the values for the following parameters were calculated:

L	:	5 pH	I_A	:	110.2 μA
I_{th}	:	505.1 μA	I_B	:	422.9 μA
I_{min}	:	-105.1 μA	I_m	:	289.8 μA

Referring to Fig. 3.6, I_{bias} is placed approximately halfway between I_{min} and I_{th} at a value of approximately $200 \mu\text{A}$. A bias current of $250 \mu\text{A}$ was chosen giving R_{bias} a value of 20Ω for a DC bias voltage source of 5 mV . The sinusoidal excitation is derived from the clock with a peak amplitude of 10 mV . The amplitude peak and minimum of the excitation are required to be larger than I_{th} and smaller than I_{min} respectively. A current of $200 \mu\text{A}$ above the threshold current I_{th} of the OJS was chosen and set a requirement for a peak excitation current of $450 \mu\text{A}$ giving a series resistor of 22.2Ω . This current amplitude is also sufficient to ensure that the negative peak of the excitation forces the OJS to make the transition back from the one to the zero flux quantum state. It can also be seen from Fig. 3.6 that changing the bias would cause the positive pulse to shift in time, depending when the OJS threshold is exceeded. The negative pulse would also shift in position with respect to the positive pulse. Only when the bias is exactly between the 0-to-1 and the 1-to-0 transitions, will the spacing between the positive and negative pulse be equal. For our

application the position in time of the negative pulse is of no importance and does not effect the operation of our design.

The rise time, t_{rise} , for a critically damped OJS ($\xi=1$) can be deduced from (17) to $3.5/\omega_n$ where ω_n is the oscillation frequency. With $L=5$ pH and $C=0.619$ pF, t_{rise} is calculated as 6.16 ps. The pulse width t_{pw} can now be approximated as 3 ps, one half of t_{rise} , and the maximum pulse voltage approximated by (22) as $521.3 \mu\text{V}$. The value of the damping resistor is calculated to be 1.4Ω for critical damping conditions using (18).

It is revealed from equations (9) to (22) in Section 2.3 that the pulse amplitude is dependant on the critical current chosen for the pulser while smaller pulse widths can only be achieve by utilizing junctions with higher critical currents and smaller L and C values.

The designed component values are reflected in Fig. 3.5. Fig. 3.7 shows the WRSpice simulation of the voltage pulse generated by the pulser for the above circuit.

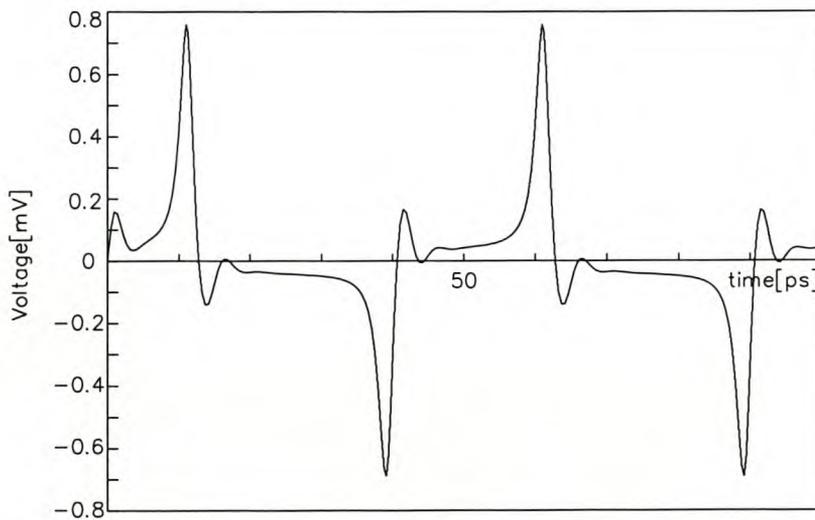


Fig. 3.7 WRSpice simulated voltage pulse of the designed pulser

3.3.2 The Clock Shaper

The clock shaper consists of a resistively damped Josephson junction. It is driven by the clock and when the current from the clock exceeds the critical current of the junction, the junction switches to the voltage state with a very sharp rising edge and clamps the voltage across the junction to the gap voltage of 2.8 mV. The advantage of the clock shaper is that it minimizes the sensitivity of the comparator circuit to variations in the clock amplitude by supplying a constant bias reference. The clock shaper was also implemented by Luong [8] and Perold *et al* [6]

The circuit for the clock shaper is given in Fig. 3.8

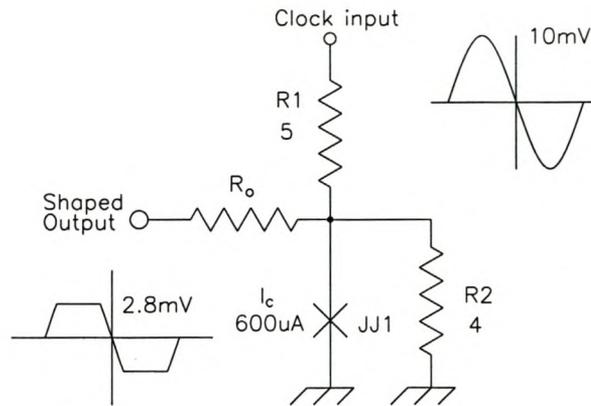


Fig. 3.8 Circuit for the clock shaper indicating the input sinusoidal excitations and the clamped output.

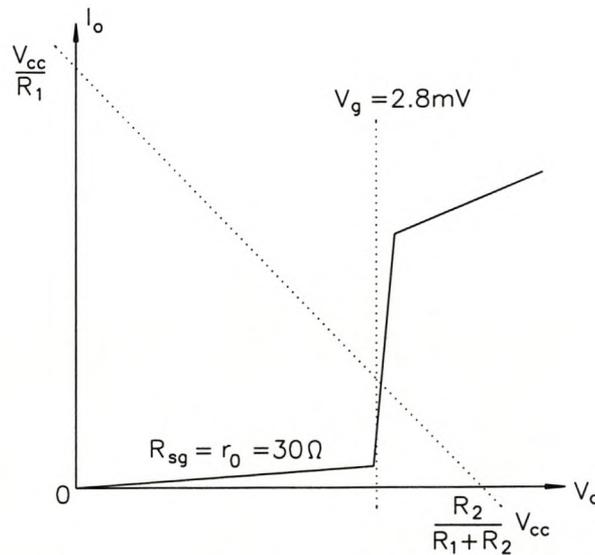


Fig. 3.9 Graphical representation of the loadline technique indicating i-v characteristics of the Josephson Junction, the intersections of the loadline and the gap voltage and subgap resistance for a 2.5 kA/cm² Josephson junction.

The load line technique illustrated in Fig. 3.9 was used to design the clock shaper. The clock shaper can be designed so that, when the junction switches to the resistive state, it switches to the gap voltage. In the sub-gap region the current through the junction is given by

$$I_o = \frac{V_o}{R_{sg}} \quad (36)$$

The load line is represented by

$$I_0 = -\frac{R_1 + R_2}{R_1 R_2} V_0 + \frac{V_{cc}}{R_1} \quad (37)$$

We start the design and choose a Josephson junction with a critical current of $600 \mu\text{A}$. For the correct operation of the clock shaper the current expressed by V_{cc}/R_1 needs to be greater than the critical current of the junction. If R_1 is chosen as 5Ω , the current is 2 mA , approximately 3 times the critical current.

Further the load line needs to intersect the i - v curve where $V_0 = 2.8 \text{ mV}$, the gap voltage. If the load line intersects at the point where the sub-gap region reaches the sub-gap voltage, the minimum value for R_2 can be calculated as 2.08Ω using (36) and (37) substituting $V_0 = 2.8 \text{ mV}$ and $R_1 = 5 \Omega$. The intersection of the load line with the V_0 axis is calculated with $R_2 = 2 \Omega$ at 2.8 mV . The first simulation was done with $R_2 = 2.5 \Omega$. It is clear from Fig. 3.10, the WRSpipe simulation of the clock shaper output for R_2 equal to 2.5Ω and 4Ω , that the clamping effect is not fully achieved for $R_2 = 2.5 \Omega$. The value for R_2 was adjusted and 4Ω yielded the best results. Fig. 3.10 shows how the clock input signal is clamped to 2.8 mV for $R_2 = 4 \Omega$.

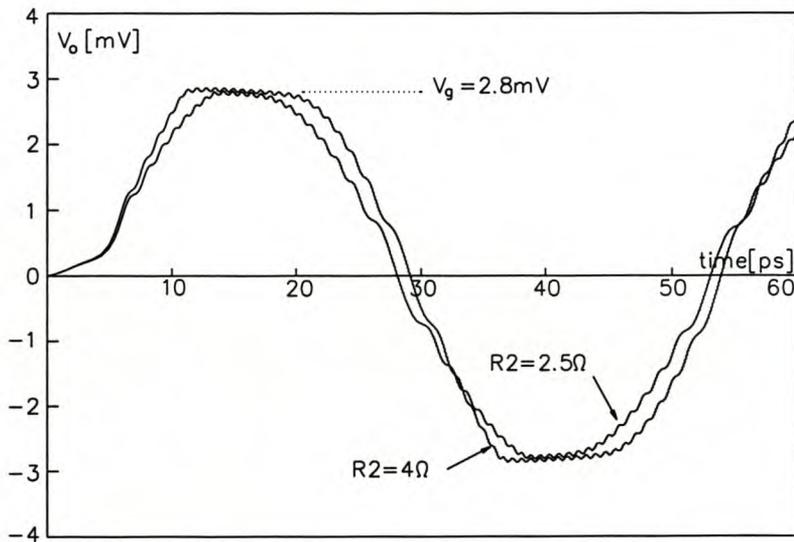


Fig. 3.10 WRSpipe simulation of clock shaper output for R_2 equal to 2.5Ω and 4Ω .

3.3.3 The One-Junction SQUID Comparator

The OJS was first studied, particularly the OJS used by Bradley [17]. In this design a OJS with $L = 0.35 \text{ pH}$, $I_c = 0.3 \text{ mA}$ and a damping resistor of 1Ω were used. We considered a OJS with three different critical currents. Table 3.2 tabulates the values calculated for β_L , C and R_{damp} for and OJS with a loop inductance of 0.35 pH .

Table 3.2 Component values for OJS with different critical currents				
I_c [mA]	B_L	L [pH]	C [pF]	R_{damp} [Ω]
0.4	0.425	0.35	0.619	0.38
0.3	0.319	0.35	0.465	0.43
0.2	0.212	0.35	0.31	0.53
0.1	0.106	0.35	0.154	0.75

The OJS was simulated with a linear ramp input for values of critical currents of 0.4 mA, 0.3 mA and 0.1 mA. The results of the simulation are shown in Fig. 3.11. The waveform of the current of the OJS with the junction with the higher critical current, exhibits a “skewness.” The waveform is slanted to the right for an increasing input current and to the left for a decreasing input current while the waveform for the OJS with the 0.1 mA junction is approximately sinusoidal for all practical purposes. The OJS with the smaller JJ, exhibiting the sinusoidal current through the junction, was considered for our design.

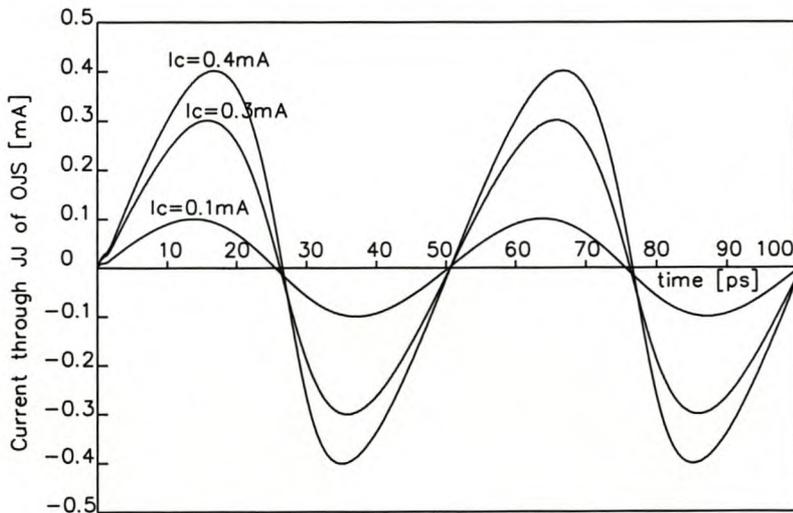


Fig. 3.11 Simulation of the current through the JJ of a OJS for different values of junction critical currents: 0.4 mA, 0.3 mA and 0.1 mA.

The designed OJS for the comparator is shown in Fig. 3.12.

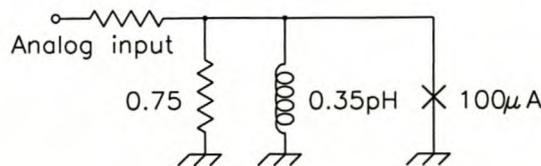


Fig. 3.12 OJS Comparator with designed component values.

3.3.4 The Two-Junction SQUID Read-Out System

The read-out system for the OJS is designed around the direct-injected non-symmetrical 2JS of Fujimaki [43], discussed in Section 2.4. For direct injection only, there is no magnetic coupling to the 2JS and the mutual inductance $M = 0$.

The first design consideration was the sampling junction of the OJS. Bradley [17, 18] used a junction with a fairly large critical current in his design for reasons explained in Section 2.3. For this reason, the sampling junction was also chosen to be large and of the value that was used by Bradley. Fujimaki [43] also showed that for $\lambda=1$ for the non-symmetrical 2JS and a ratio of $q/p=3$, yielded the maximum operating margin for the non-symmetrical 2JS.

To combine the OJS and the 2JS, several values for the maximum bias current, I_m , was considered. This translates into different values for the sampling junction (junction shared by OJS and 2JS) in the context of the 2JS. It was found that for larger values of I_{max} the effect on the skewness of the OJS was the least. Fig. 3.13 shows the current through the quantizing junction of the OJS for different values of I_m with no bias applied to the 2JS. It can be seen that the negative slope for the smaller value of I_{max} (0.5 mA) is much steeper than that for $I_{max} = 2$ mA.

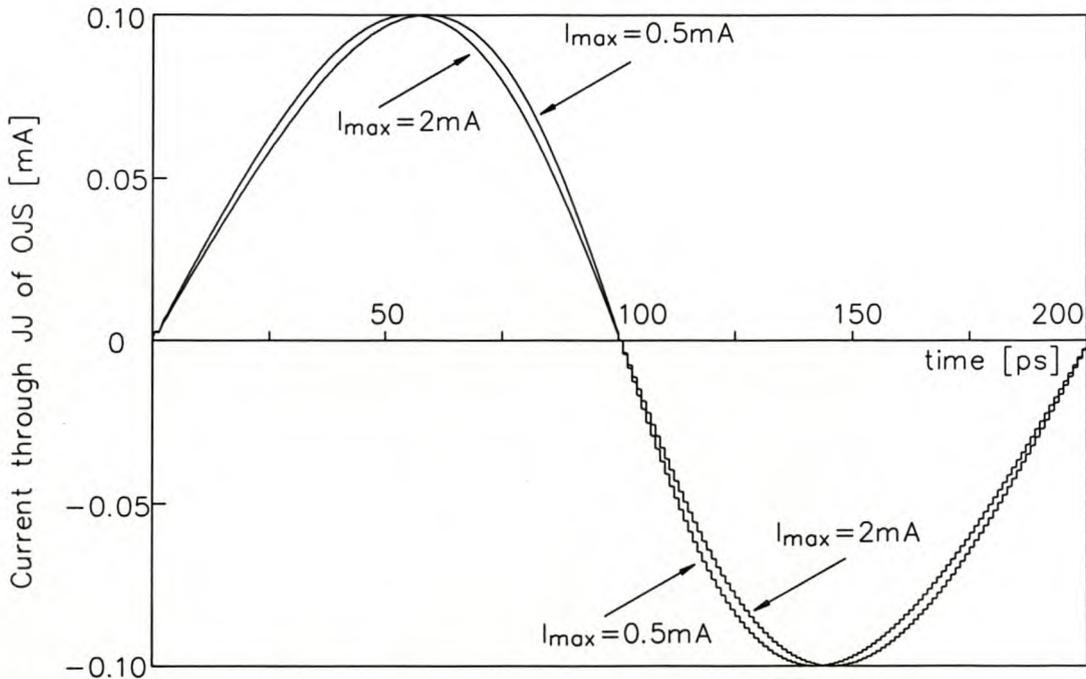


Fig. 3.13 The current through the quantizing junction of the OJS for different values of I_{max} of the 2JS.

To minimize the skewness of the current through the JJ of the QOJS, it was decided to use a maximum bias current of 2 mA. I_{max} is limited to this value as the inductor values become too small to be practically realized for the non-symmetrical 2JS. The first junction is chosen as 1.5 mA and to comply with the condition $p+q=1$ for a non-symmetrical 2JS, the second junction needs to be 500 μ A. For a maximum bias current $I_m = 2$ mA, the inductance for the 2JS is calculated as $L = 1.034$ pH and $pL = 0.775$ pH and $qL = 0.258$ pH by using (29) for the normalized inductance. It can be seen that 0.258 pH is already a very small inductor.

3.3.5 Integration of the complete comparator

Finally the pulser, the clock shaper, the DC bias and the 2JS have to be integrated to complete the read-out circuit of the comparator. The outputs from the pulser and the clock shaper and the DC bias all contribute to the bias of the 2JS or alternatively, it sets the threshold of the 2JS. The contribution of each towards the threshold was chosen to be in the following ratios: 50% from the DC bias, 20% from the clock shaper and 30% from the pulser.

The threshold curve for the 2JS was acquired using the circuit shown in Fig. 3.14 with the component values calculated in the previous Section.

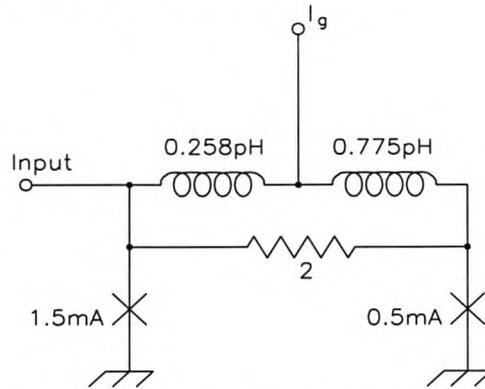


Fig. 3.14 Circuit for determining the threshold curve for the 2JS

The threshold curve was determined by observing when the 2JS crosses the threshold while linearly sweeping the gate current I_g for different values of current directly injected into the 2JS loop. As expected, this would be approximately equal to 2 mA for zero current injected, equal to the I_{max} of the 2JS. Any additional current added from the pulser, clock shaper or DC bias would lower the threshold for the 2JS. Fig. 3.15 shows the linear threshold of the directly injected 2JS in the operating region $\pm 100 \mu\text{A}$ input.

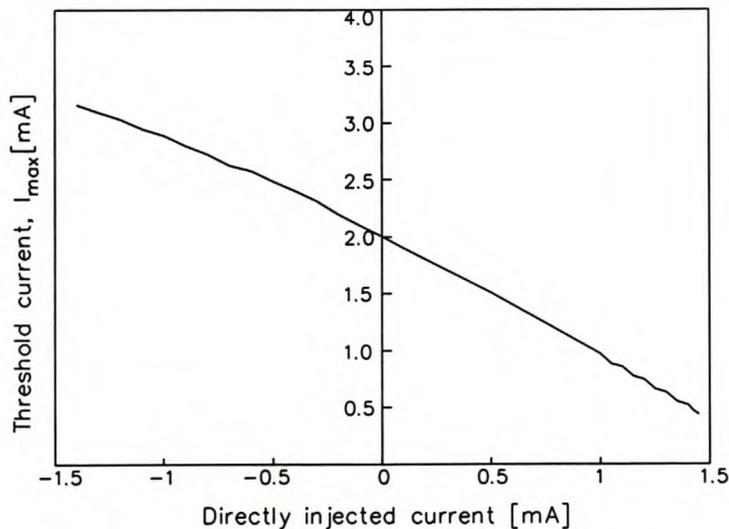


Fig. 3.15 The linear threshold curve for the 2JS

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The currents from the pulser, clock shaper and DC bias, and subsequently the values of the feeding resistor, can now be determined for their contribution ratios to the threshold:

DC bias:	50% contribution of 2 mA = 1 mA
Clock shaper	20% contribution of 2 mA = 0.4 mA
Pulser	30% contribution of 2 mA = 0.6 mA

The DC bias is provided from a 5 mV source giving a feeding resistor of $5 \text{ mV}/1 \text{ mA} = 5 \Omega$. The current from the clock shaper is derived from the 2.8 mV gap voltage and the feeding resistor is calculated as $2.8 \text{ mV}/0.4 \text{ mA} = 7 \Omega$. The feeding resistor from the pulser was calculated using the estimated pulse voltage of $521.3 \mu\text{V}$ divided by the required current of 0.6 mA. This gives a feeding resistor of 0.86Ω for the pulser.

In the implementation of the pulser and the feeding resistor by Fang [7], the feeding resistor also served as the damping resistor. This approach was also followed in this design. The complete circuit for 2JS read-out system is shown in Fig. 3.16.

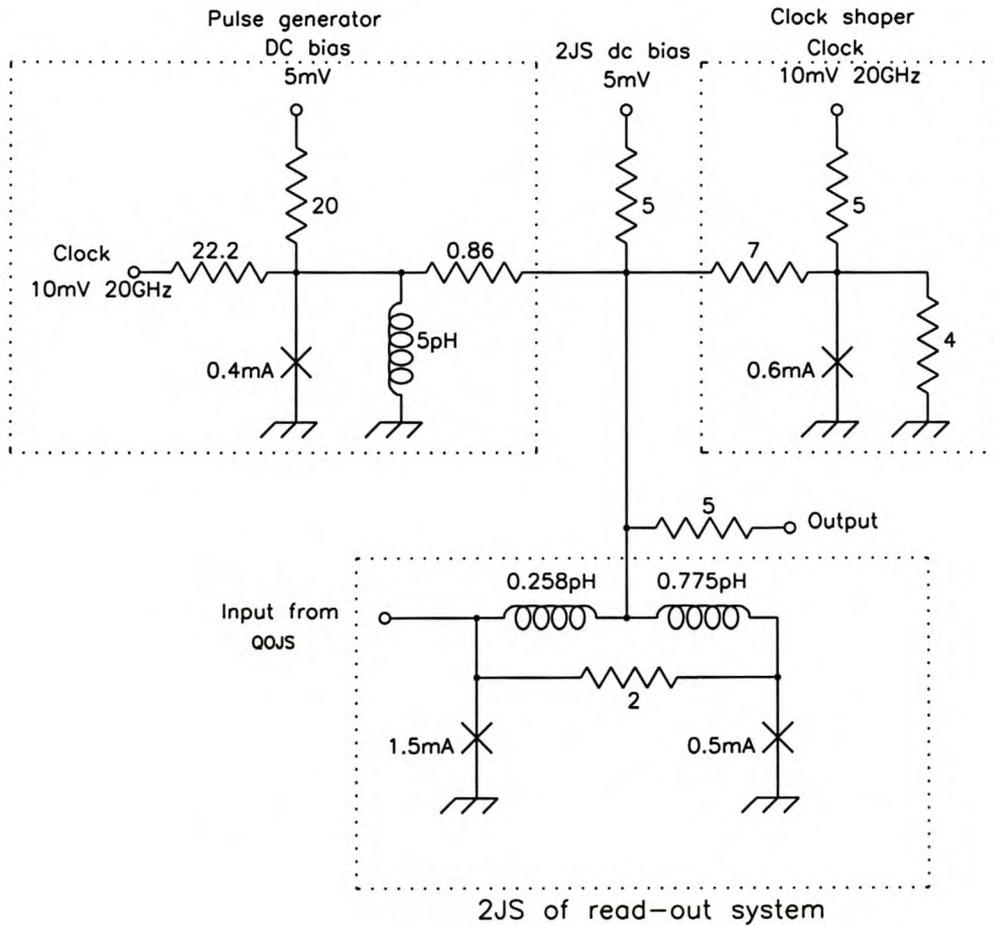


Fig. 3.16 Designed 2JS circuit with component values.

3.3.6 The COSL OR-gate Buffer Stage

The output of the SL-Comparator (SLC) is fed to the COSL OR-gate which buffers the output from the comparator and restores the pulses to full COSL pulses. The COSL OR-gate designed by Perold *et al* [6] was used without any modifications, except for the DC bias that was changed to adapt it for 20 GHz operation.

3.3.7 WRSpice Simulation of the Complete SL-Comparator

The complete SLC was implemented and simulated in WRSpice to verify the operation of the design. It was necessary to vary the component values around the calculated value to obtain a fully functional comparator.

The requirement for a correct functional comparator is that a 1:1 ratio must be obtained for the ratio of logic “1” pulses to logic “0” pulses at the output of the comparator for a linearly increasing analog signal. This is achieved by adjusting the amount of bias from each of the clock shaper, the pulser and the DC bias.

Component values were adjusted within WRSpice to obtain the above requirement. These new values for the components for the complete operational SLC are shown in Fig. 3.17. The COSL OR-gate buffer is not shown. It was necessary to lower the coupling resistor between the comparator and the OR-gate to 2.3Ω to provide sufficient driving current to the COSL gate.

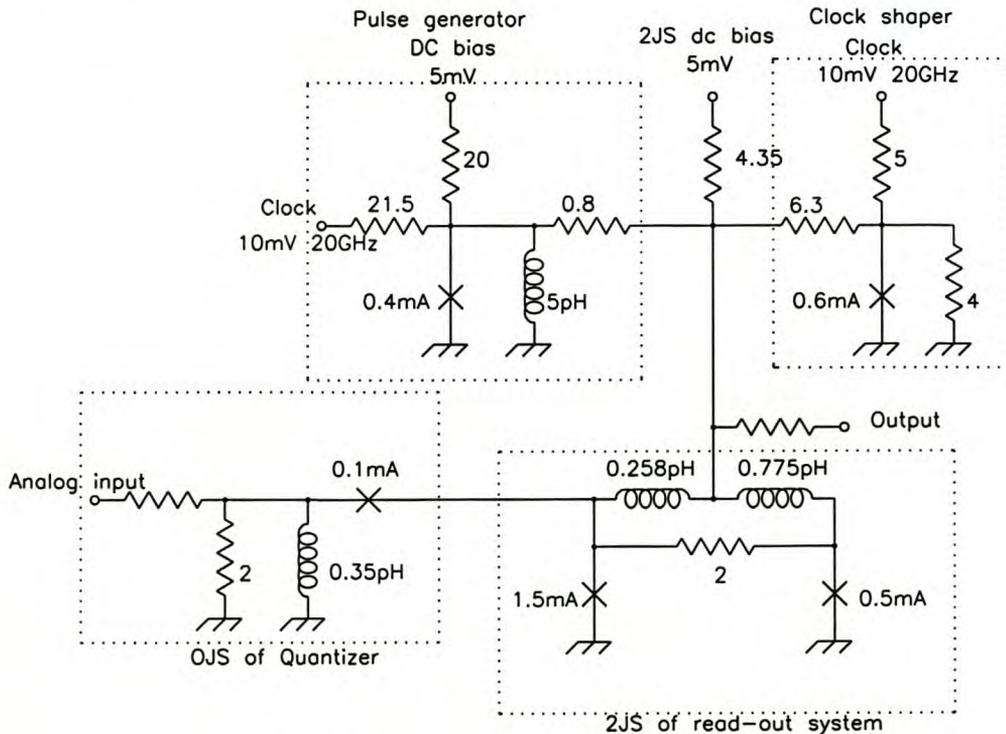


Fig. 3.17

Complete circuit for the operational SLC showing the new component values obtained by WRSpice simulation for a functional circuit.

Fig. 3.18 shows the output from the simulated SL comparator for a linear increasing analog input signal. From (35) the periodicity in the input for a OJS can be calculated in A/cycle. Every cycle correspond to 4 quantization levels of an ADC. A 4-bit ADC with 16 quantization levels thus requires 4 cycles which again translates to an input current of 4 times the current per cycle. The LSB will receive the full input current, the next bit 50% of the full input, the third bit 25% of the full input and the MSB 12.5% of the full input. These ratios are obtained by the R/2R ladder network which again requires twice the full input current at its input to divide the input current into the correct ratios. For a 0.35 pH inductor the periodicity is 5 mA/cycle, requiring 23.6 mA for a 4-bit ADC and 47.2 mA at the input of the R/2R resistor network.

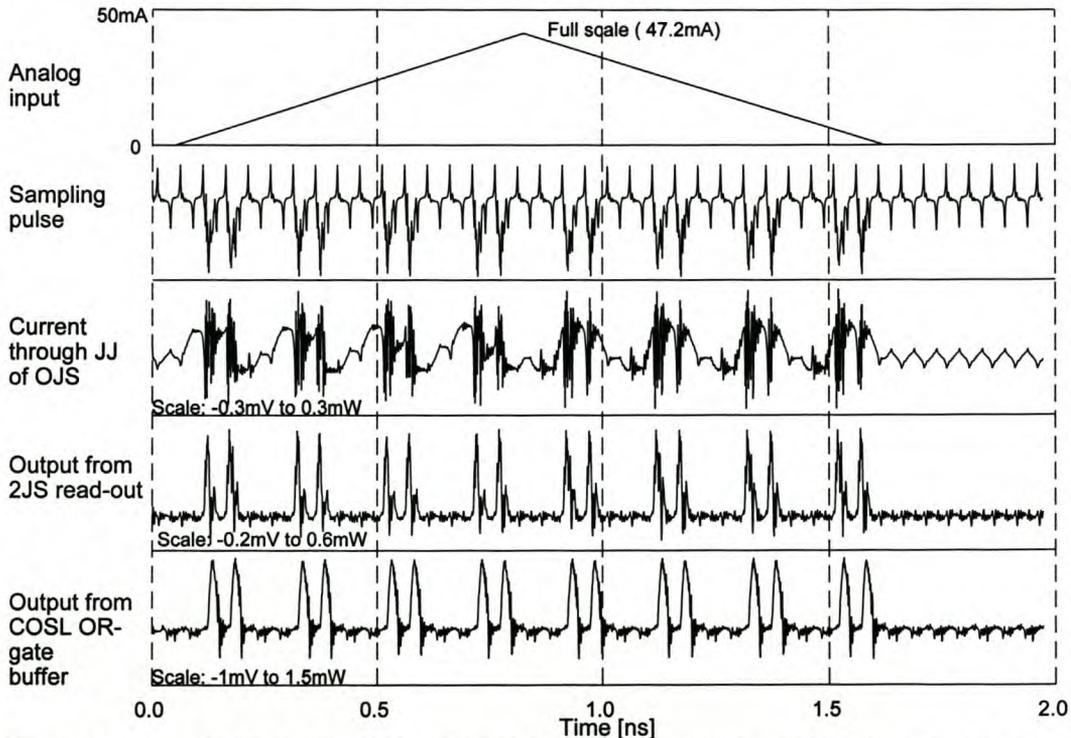


Fig. 3.18 WRSpipe simulation of the SLComparator showing the analog input signal, the sampling pulses, the current through the JJ of the OJS, the output pulses from the 2JS and the COSL buffered output pulses. The number of “1” output pulses and “0” pulses have a 1:1 ratio.

The sample pulses indicate the instances in time when the periodic current through the JJ of the OJS, generated as a result of the input signal, are sampled. The sharp pulses from the 2JS and the buffered COSL pulses are also shown.

Finally, the output of the comparator shows the 1:1 ratio between the logic “0” pulses and the logic “1” pulses for a linearly increasing analog input signal.

3.3.8 Phase Shift in the Current through the JJ of the OJS of the Comparator

A delay was observed from the time that the current through the JJ of the OJS, injected in the 2JS, is positive, until the comparator actual begins to switch for a positive value of the current injected. It was expected that the 2JS would begin switching as soon as the current injected into the 2JS becomes positive. This effect can be seen from the simulation results in Fig. 3.18.

This delay was due to a phase shift in the current through the JJ of the OJS. The same circuit in Fig. 3.17 was again simulated, but with the current contribution from the pulser and the clock shaper towards the total bias, disabled. Fig. 3.19 shows the current through the JJ for different slew rates of linear increasing analog inputs. In all the cases the currents are still symmetrical around zero but start at an initial current value of approximately $-50 \mu\text{A}$. This translates to a phase shift in the current through the JJ which in turn causes the delay in commencement of the sampling. This phase shift is caused by the DC bias from the 2JS, flowing back through the JJ into the OJS. This delay or phase shift, however, does not effect the operation of the comparator. The DC bias can still be adjusted to obtain 1:1 ratio for the output logic pulses for a full scale input.

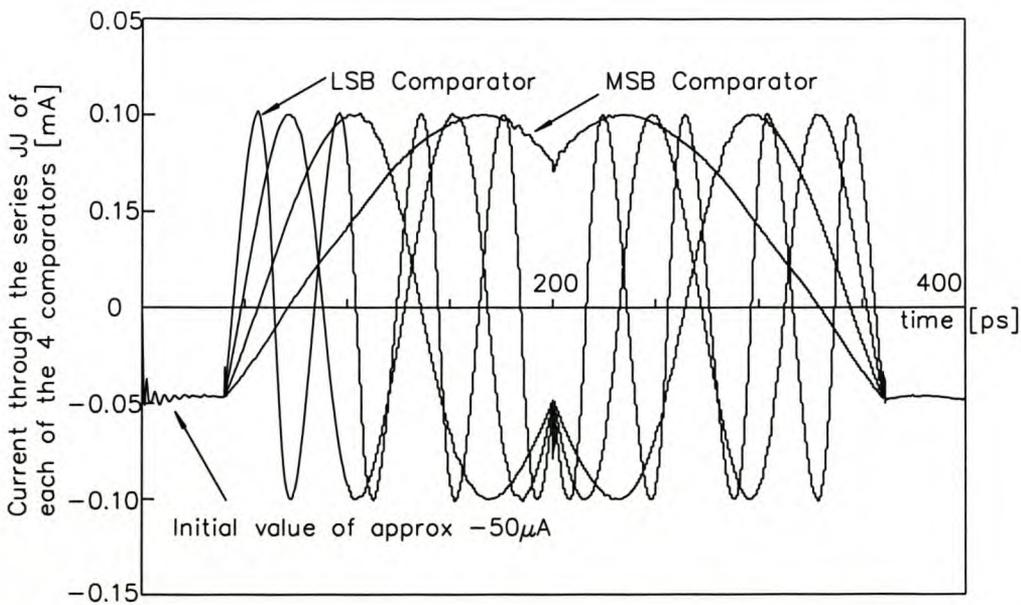


Fig. 3.19 The current through the series JJ of the OJS of the comparator for different slew rates of the analog input linear ramp.

3.3.9 Pulser Rise Time versus Pulse Width

A major advantage of the SLC design is that the aperture time is determined by the rise time of the sampling pulse and not the pulse width

When the input causes the threshold of the 2JS read-out system to be exceeded, it immediately causes the 2JS to switch to the voltage state and will produce a voltage pulse. This threshold will always be exceeded for the first time on the rising edge of the sampling pulse and will result in the switching of the 2JS. Once the 2JS has commenced switching, changes in the sampling pulse and consequently also the pulse width, is of no importance.

Previously it was shown how the threshold for the SLC was set up at zero and that any positive value of the current injected into the 2JS would cause the threshold to be exceeded. This additional current added to that of the pulser, clock shaper and DC bias, is set by the critical current of the JJ of the OJS and is equal to $100 \mu\text{A}$ for our design. Effectively, this means that at the maximum of the current injected into the 2JS, the sampling pulse would exceed the

threshold by $100\ \mu\text{A}$ and for zero input, the peak of the sampling pulse would be at the threshold level. Thus, the portion of the sampling pulse that effects the instant at which sampling takes place is from the peak and $100\ \mu\text{A}$ down from the peak and can thus be assumed as the aperture time for the SLC. This concept is graphically presented in Fig. 3.20 and is measure by utilizing the WRSpice simulation to be approximately $0.6\ \text{ps}$.

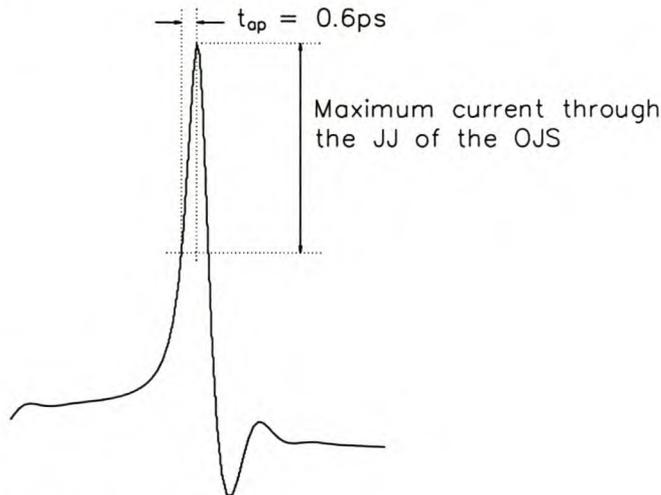


Fig. 3.20 Aperture time determination for the SLC.

This small aperture time has important implications for the performance of the SLC and the switching-logic ADC (SLADC). The smaller the aperture time, the higher the input bandwidth that can be achieved. Predictions are given in the conclusions.

For a small injected current only the tip of the sampling pulse would break through the threshold level. However, for the maximum of the injected current, the pulse will exceed the threshold as soon as the pulse rises through the point, $0.1\ \text{mA}$ from the peak of the pulse. This can cause a uncertainty of $0.6\ \text{ps}$ in the time when the input was sampled.

■ Summary

The concept and design of a novel superconductive comparator design was presented in this Chapter. The detailed design of all the sub-circuits of the comparator is discussed. These sub-circuits include the pulser, the clock shaper, the OJS, the 2JS and the COSL OR-gate buffer stage.

The sub-circuits are finally integrated to construct a SLC. The SLC was simulated in WRSpice to confirm its operation. A phase delay in the sampling response of the 2JS and its effects are discussed. It is also shown that the aperture time for the SLC is not dependent on the width of the sampling pulse but on the rise time of the pulse.

WRSpice Yield Predictions and Simulations

■ Introduction

- 4.1 Monte Carlo Analysis
- 4.2 Circuit Trimming Facilities
- 4.3 Implementation of the Monte Carlo Process and Trimming facilities in WRSpice
- 4.4 Implementation of Fail/Pass Test Procedure in WRSpice
- 4.5 Optimization of the SL-Comparator Circuit
- 4.6 WRSpice Predicted Yield of the SL-Comparator
- 4.7 Simulation of the Optimized SL-Comparator

■ Summary

■ Introduction

The predicted reliability of the SLC is verified by a Monte Carlo yield prediction process. This process incorporates the tolerances in the manufacturing process. The Monte Carlo process was also further utilized to optimize the SLC for maximum yield. This complete process was implemented in a WRSpice simulation.

At the onset of this dissertation, JSPICE [40] was the only simulation software package available to perform super conductive circuit simulations. Most of the original research and circuit simulations were done utilizing JSPICE.

Circuit simulations became much easier when WRSpice were made available for use by our engineering department. This simulation software is very user friendly, faster and extremely powerful. The new scripting option to control simulations was used extensively for the purpose of this dissertation.

4.1 The Monte Carlo Analysis

Conventionally, the reliability of circuits is predicted by margin analysis. During a margin analysis, the circuit functionality is observed while one or two parameter values are changed in two consecutive simulation runs. This method gives an indication of the sensitivity of the circuit to changes in the parameter values. This method, therefore, has the drawback that it does not take into account that, varying multiple parameters simultaneously, could have a possible effect on the reliability of the circuit.

The Monte Carlo process overcomes this shortfall by simultaneously varying all the parameter values statistically around their nominal values. The quality of the fabrication process dictates the parameter tolerances. Two spreads in values of parameters for the fabrication process are identified. The spreads are normally larger from wafer-to-wafer than on the same wafer. To incorporate this into our simulation, the following parameter value definitions were made:

1. Nominal parameter values
2. Global parameter variations (chip-to-chip) of Gaussian distribution
3. Local parameter variations (on-chip) of Gaussian distribution

WRSpice was utilized to implement the Monte Carlo process to predict the yield of the SLC, taking both global and local parameter spreads of resistors and inductors into account. Global changes in the critical current were ascribed to variations in the critical current density and local variations to changes in the areas of the Josephson junctions. Spreads of resistance and capacitance of Josephson junctions were defined by the change in the critical currents.

Spence [37] showed that the true statistical yield y of a circuit lies within the interval defined by the observed yield y' and the confidence interval L as

$$y = y' \pm L \quad (38)$$

The confidence interval is given by

$$L = k \sqrt{\frac{y'(1-y')}{N}} \quad (39)$$

where N is the number of Monte Carlo cycles and k a constant depending on the required confidence level of the prediction. Values for k vary from 2 to 2.6 for confidence levels of 95% and 99% respectively. It can be seen that a high confidence level leads to a larger confidence interval, which, in turn, can only be lowered by increasing N , the number of Monte Carlo cycles.

4.2 Circuit Trimming Facilities

In most Josephson logic circuits it is possible to adjust a non-functional circuit to become functional by trimming the voltage levels of either the DC bias or the clocks. This facility compensates for global parameter variations. This technique was also implemented successfully to trim a non-functional SLC to functional SLC.

Trimming of the DC bias was implemented for both the pulser and the 2JS of the read-out system of the comparator. In practice, this can easily be achieved by only increasing or decreasing the DC bias current to the Pulser and the 2JS.

Similar to the COSL gates, the 2JS of SLC is also biased by clock-shaping circuits that clamp the clock signals to the gap voltage and it is therefore not possible to apply trimming to the clock amplitudes. Trimming for the 2JS can thus only be accomplished through small adjustments to the DC bias.

To be able to perform reliable yield predictions by means of WRSpice simulations, it is necessary to include the process of trimming a non-functional circuit in the Monte Carlo simulations.

In the case of the Pulser, the ratio of the total bias current to the threshold current of the Josephson junction of the Pulser was considered. This ratio is compared for every set of global variations or chip-to-chip variations in parameter values, to the ratio for the circuit with nominal parameter values. The trim voltage is set to make the ratio for the circuit with global variations on its parameter values the same as it would be with nominal parameter values and no trim voltage applied. In Chapter 2 are used to calculate The threshold current, I_{th} , is calculated using (9) and (10), while the total bias current, I_{bias} , is given by V_{bias}/R_{bias} .

Trimming for the 2JS is slightly more complex. Here we consider the ratio of the sum of the total bias current and critical current of the Josephson junction of the OJS, to the sum of the critical currents of the two Josephson junctions of the 2JS. The DC trim voltage is again utilized to ensure that the above mentioned ratio for the circuit with global variations on its parameter values are the same as for the circuit with nominal parameter values and no trim voltage applied.

Trimming for all additional COSL gates to be used in the design of the complete SL comparator is done according to implementation by Perold *et al* [6].

4.3 Implementation of Monte Carlo Process Trim Facilities in WRSpice

The scripting option of WRSpice is a powerful tool and was used extensively in the fulfilment of this dissertation. WRSpice includes a script parsing and execution facility, which uses a syntax similar to that of the UNIX C-shell. Statements which are interpreted and executed by this facility can be included in circuit files through use of the *.exec* and *.control* tokens. These statements are enclosed in a block beginning with *.exec* and *.control* and ending with *.endc*. The

difference between *.exec* and *.control* is that for *.exec*, the commands are executed before the circuits parsed, and for *.control*, the commands are executed after the circuit is parsed. The syntax and statements used are described in the WRSpice manual.

In order to simulate the SLC three circuits need to be considered. These include the SLC with nominal component values (nominal circuit), the SLC with Gaussian spreads on component values (spread circuit) and thirdly, the latter circuit with the trimming facilities implemented (trim circuit). The simulation processes are then controlled from one file that source and initiate the simulation of the three circuits.

To implement the trim facilities in the simulation process, measurements are made of the bias currents during the simulation for the nominal circuit and the spread circuit. These measurements are then used to calculate the trim voltages. The calculated trim voltage is then forwarded to the trim circuit and applied to a circuit with the same spreads as the spread circuit in an attempt to correct for global variations in parameter values. This process is illustrated through the flow diagram in Fig. 5.1.

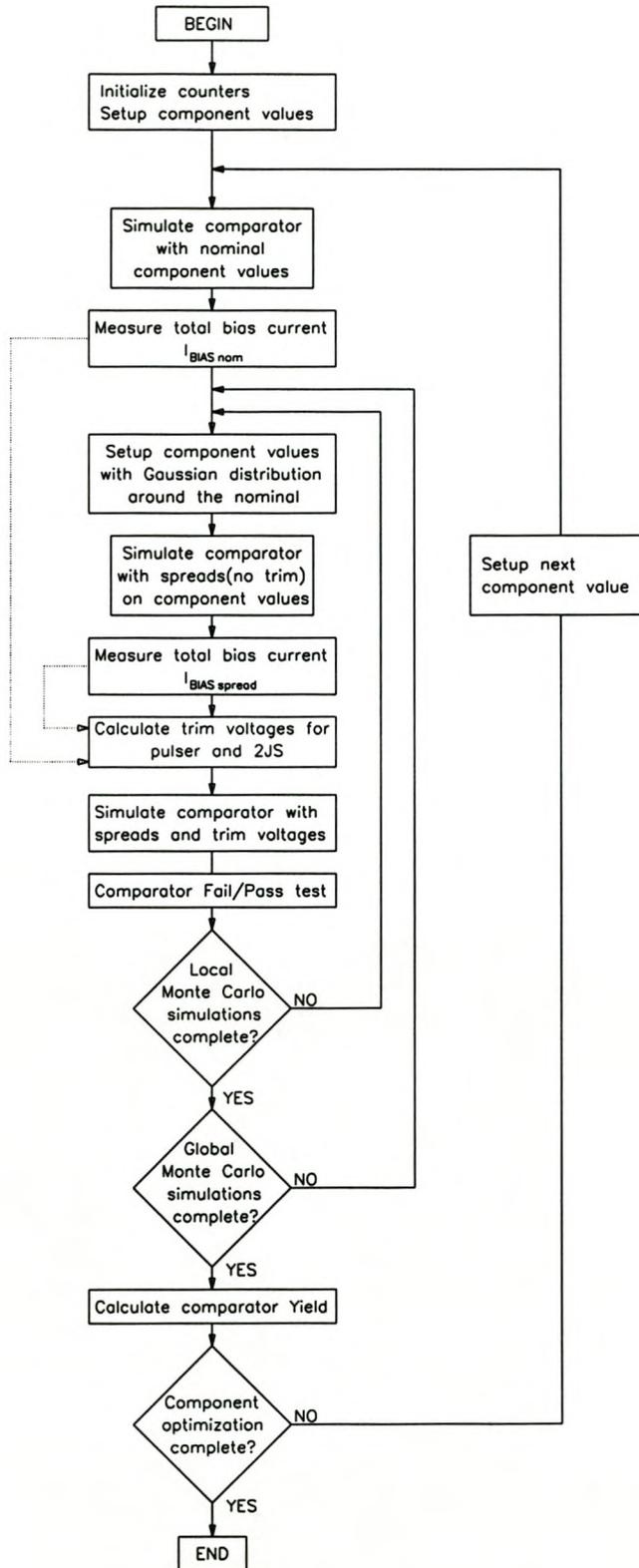


Fig. 5.1 The flow diagram for the optimisation process of the SL-comparator. The dotted lines on the left only indicates the forward passing of the measured bias currents for calculation of the trimming voltages.

Utilizing the ratios given in Section 4.2 the trim voltage for the Pulser and the 2JS are given by

$$V_{trim}(pulser) = \left[\left(\frac{I_{th}(spread) I_{bias}(nom)}{I_{th}(nom)} \right) - I_{bias}(spread) \right] R_{bias}(spread) \quad (40)$$

where I_{th} is the threshold current of the Pulser SQUID and I_{bias} the total bias current of the Pulser. The ratio of $I_{bias}(nom)$ to $I_{th}(nom)$ can be calculated to have a value of approximately 0.5 for the nominal circuit.

The trim voltage for the 2JS, in turn, is given by

$$V_{trim}(2JS) = \left[\frac{(I_{bias}(nom) + I_f(nom))(I_{J1}(spread) + I_{J2}(spread))}{(I_{J1}(nom) + I_{J2}(nom))} - (I_{bias}(spread) + I_f(spread)) \right] R_{bias}(spread) \quad (41)$$

where I_j is the critical current of the of Josephson junction of the OJS, I_{bias} the total bias current of the 2JS and I_{J1} and I_{J2} are the critical currents of the Josephson junctions of the 2JS. The derivations for (40) and (41) are given in Appendix A.

Due to the fact that it is not possible to calculate the bias currents for the circuits using pulsers and non-symmetrical 2JSs it was opted to measure these currents using simulations in WRSpice. The Control file schedules the simulation tasks and first calls for the nominal and then the spread circuit to be simulated. The total bias currents $I_{bias}(nom)$ and $I_{bias}(spread)$ are measured respectively for both the pulser and the 2JS while the input is zero. The *.measure* statement in WRSpice is used for this purpose. These measured values are then passed on to the trim circuit where the trim voltage is calculated and applied to the spread circuit to correct for the simulated variations in the component values. This method of trimming was implemented successfully.

WRSpice has a built-in Monte Carlo facility. Unfortunately due to the complexity and the structure of the simulation, this built-in Monte Carlo facility could not be used. The Monte Carlo process was therefore implemented manually into the simulation and was also controlled and scheduled from the control file.

To execute the Monte Carlo process, two nested simulation loops were utilized. The inner loop determines the number of simulations that represent the sets of local variations on the component values(resistors, inductors and junction areas), while the outer loop determines the number of simulations that represent the sets of global variations on component values(resistors, inductors and junction current densities). This allows for only one set of global variations for every fully completed inner loop, simulating a wafer-to-wafer variation of parameters.

In order to get a good statistical representation, it was decided to have only one simulation per inner loop. This constitutes one set of global variations for every local set of variations.

4.4 Implementation of Fail/Pass Test Procedure in WRSpice

To be able to assess the functionality of the SLC it has to be subjected to a consistent test procedure. For this purpose we have selected a specific input signal. The input is ramped from zero to a level of twice the threshold of the comparator. The rate of change for the ramp is chosen such that it sweeps from zero to $2I_{th}$ within two clock cycles or 100 ps, offset in such a way that the ramp starts and ends exactly between successive clock pulses. Once the ramp has reached $2I_{th}$ it is kept at this level for a period equal to one clock cycle and then ramps down to zero in the same manner as from zero to $2I_{th}$. This is illustrated graphically in Fig. 5.2.

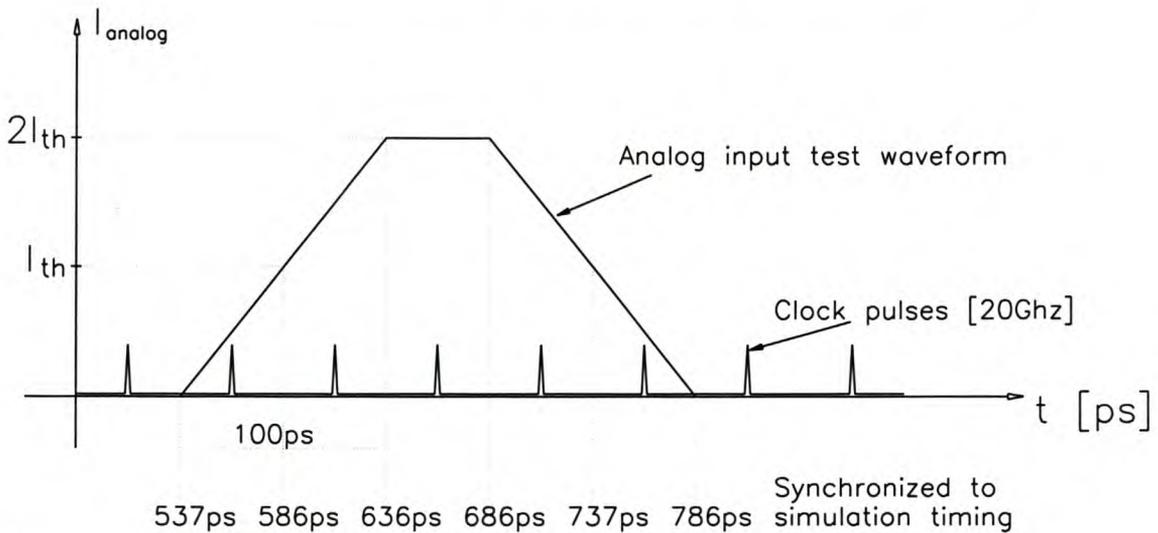


Fig. 5.2 Input signal for functionality tests for SLC.

The threshold of the comparator for input current was determined by simulation to be 1.57 mA and the time between clock pulses is 50 ps for a 20 GHz clock. The ramp is also kept at zero for some time before it commences to ensure that all transient effects have settled. This input signal is selected to yield the same output for every simulation run when the comparator is functioning correctly. The input is sampled by successive clock pulses for the following conditions indicated in Fig. 5.2:

- | | | | |
|---|---|---|-----------------|
| ① | The input signal is zero | : | no output pulse |
| ② | The input signal increasing but smaller than I_{th} | : | no output pulse |
| ③ | The input signal increasing but larger than I_{th} | : | output pulse |
| ④ | The input signal constant and larger than I_{th} | : | output pulse |
| ⑤ | The input signal decreasing but larger than I_{th} | : | output pulse |
| ⑥ | The input signal decreasing but smaller than I_{th} | : | no output pulse |
| ⑦ | The input signal zero again | : | no output pulse |

At the end of every simulation, the functionality of the circuit was evaluated by the a WRSpice procedure that checks and verifies each of the seven individual conditions mentioned above. If all the conditions are met, the circuit passes. If only one of the checks are not met, the circuit fails as a whole. The number of circuits that pass are counted and the yield is calculated as a percentage of the total circuits that were simulated.

4.5 Optimization of the SL-Comparator Circuit

Optimization of the SLC was obtained by maximizing the predicted yield from WRSpice for global and local variations of component values with Gaussian distributions.

A set of values around the nominal component value, for every component of the SLC, was generated. A complete Monte Carlo analysis was then done for each of the values in the set while the yield of the comparator was observed for a maximum. The optimized component value would be the value that corresponds to the maximum yield. This procedure was performed for all the components in the SLC. The yield slowly increased as the circuit became more and more optimized, yielding the maximum yield at the end of this process.

4.6 WRSpice Predicted Yield of the SL-Comparator

The complete source code for the WRSpice Monte Carlo yield prediction simulation is given in Appendix B. The yield simulation was performed for Global/Local spreads of 15%/10% as the 3σ spread value, which is an estimation for tolerances in the HYPRES process. Perold *et al* [6] determined through measurements that a 10% 3σ local variations is a good representation of the HYPRES process.

The yield prediction obtained from the WRSpice simulation is given in the Table 5.1. A 95% confidence level gives and confidence interval of $L=0.036$ for the observed yield of 89% and gives a true statistical yield of $89\pm 3.6\%$ while a 99% confidence level gives and confidence interval of $L=0.047$ and a true statistical yield of $89\pm 4.7\%$. The optimization showed an increase of 12% from 78% to 89% for the the yield for the comparator.

Table 5.1 WRSpice Yield predictions		
Global/Local spreads	15% global / 10% local	15% global / 5% local
Predicted Yield (%)	89	93.7

A total of 300 Monte Carlo cycles were used. To lower the confidence interval would require to increase N , the number of Monte Carlo cycles. The simulation of 5 different values for a specific component and 300 Monte Carlo cycle take an average of 213 minutes to execute in WRSpice on a 533 MHz Pentium computer 128 Meg memory.

4.7 Simulation of optimized comparator

It was found that the 1:1 ratio between the logic "0" pulses and the logic "1" pulses for a linearly increasing analog input signal, was changed by the Monte Carlo yield optimization. It was necessary to make a small adjustment to the DC bias to correct for a 1:1 ratio.

In order to ensure that the 1:1 ratio between the logic “0” pulses and the logic “1” pulses is maintained, it would thus be necessary to expand the test waveform to determine and correct this ratio.

It is believed that the threshold is crossed too fast (only one pulse between zero and the threshold and between the threshold and a value of twice the threshold - Fig. 5.2), leaving a margin for error. More checks should be done between zero, the threshold and twice the threshold. Checks below and above the threshold should be done as close as possible to the threshold. This would require a slower sweep over the threshold so that more sampling is done closer to the threshold to pin it down. This, however, would increase the number of fail/pass checks to compensate for the increase in sampling instances as a result of the slower input ramp.

The optimizing process also brought small changes to the component values of the comparator. The new values for these components are as follows:

Resistor feeding the pulser to the SLC:	0.79 Ω
DC bias resistor:	4.31 Ω
Sampler circuit inductor:	0.4 pH
2JS damping resistor:	2.5 Ω
SLC and OR gate buffer coupling resistor:	2.2 Ω

■ Summary

This Chapter discussed how the SLC simulation together with a Monte Carlo process was successfully implemented in WRSpice. The simulation was also successfully utilized to verify the functionality of the comparator and optimize the comparator circuit parameters by maximizing the WRSpice predicted yield for global and local variations with Gaussian distributions. An increase of 12 % in the yield was obtained through implementation of the trimming facilities.

Although this simulation was successful to increase the yield and optimize the comparator, it is believed not to be optimal yet. It could be improved by expanding the test signal to include the 1:1 ratio condition in the fail/pass tests.

Design of a 4-Bit High Input Bandwidth Superconductive A-D Converter

■ Introduction

5.1 Construction of the Switching-Logic ADC

- 5.1.1 Construction of the 4-bit Quantizer Section of the ADC
- 5.1.2 Design of a Gray-to-Binary Converter
- 5.1.3 Reconstruction of Input from Output of ADC

5.2 Evaluation of Switching-Logic ADC

- 5.2.1 Low Frequency Performance
- 5.2.2 Beat Frequency Simulation
- 5.2.3 Input Bandwidth Evaluation
- 5.2.4 Special Input Signals

■ Summary

■ Introduction

Previous Chapters dealt mainly with the design of all the building blocks of the main component of an ADC, namely the comparator. This Chapter will now integrate all the components necessary to construct an ADC. This includes the comparator stage and the Gray-to-Binary converter. The complete comparator is then simulated to evaluate the performance of the ADC.

5.1 Design of the 4-bit Switching-Logic ADC

5.1.1 Design of the 4-bit Quantizer Section of the ADC

According to Section 2.6.3, N comparators are required for an N -bit Flash ADC. The analog input is first divided by the resistive ladder divider network as discussed in Section 2.3 and illustrated in Fig. 1.2 and then passed on to each of the N comparators of the N -bit comparator. A value of $3\ \Omega$ was chosen for R in the $R/2R$ ladder network. Fig. 5.1 shows how the OJS switching logic comparator (SLC) are utilized to construct the comparator or quantizer section of an N -bit ADC.

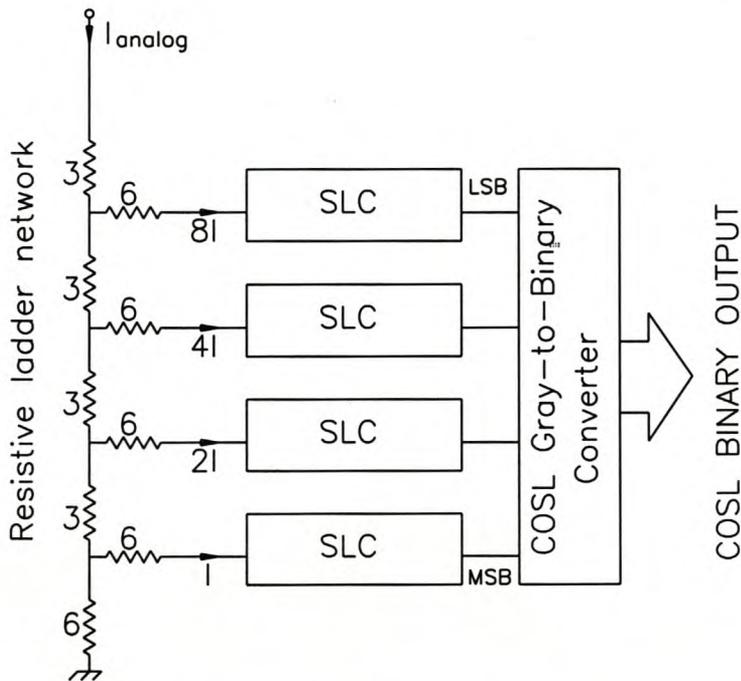


Fig. 5.1 The comparator or quantizer section of an N -bit ADC.

The output of the comparator section is in Gray-code and still needs to be converted into binary for further processing. This process and the required circuits will be discussed in the following Section.

It is important to note that during the optimization process the inductor of the OJS was optimized to $0.4\ \text{pH}$. The periodicity of the OJS now changes to $\Phi_0/L=5.16\ \text{mA/cycle}$, resulting in a required full scale input of approximately $41.4\ \text{mA}$.

5.1.2 Design of a Gray-to-Binary converter

In conventional logic design a Gray-to-Binary converter (GBC) can be constructed from XOR gates as shown in Fig. 5.2

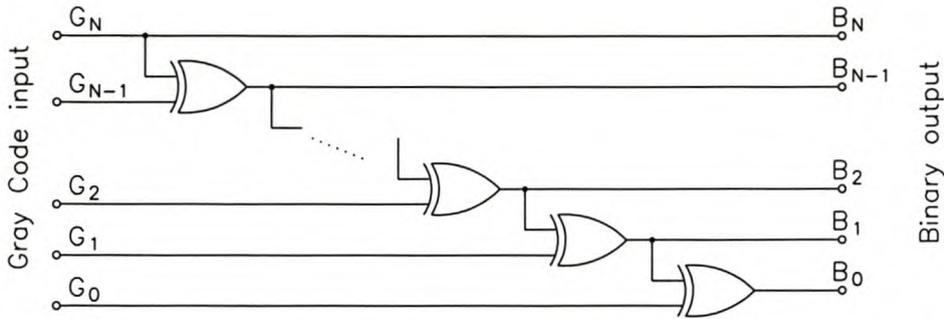


Fig. 5.2 Conventional logic design of a Gray-to-Binary Converter utilizing XOR gates.

Converting this conventional logic circuit to COSL architecture, a number of aspects has to be taken into account. These include:

1. The input and output impedance of each COSL gate
2. The fan-in and fan-out of the COSL gates
3. The three phase clocking scheme of the COSL gates
4. Propagation delay of signals through the converter

Fig. 5.3 shows the implementation of the 4-bit GBC shown in Fig. 5.2 in COSL architecture.

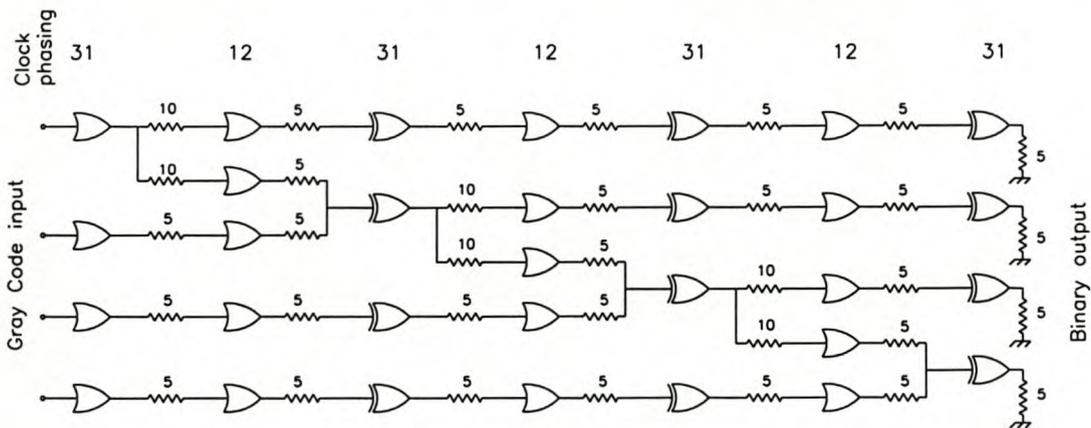


Fig. 5.3 A4-bit Gray-to-Binary Converter in COSL architecture. The correct clock phasing of the gates is shown at the top of the diagram.

When a specific gate drives two other gates each gate is coupled with a 10 Ω resistor from the driver gate. This provides an output or load impedance of 5 Ω to the driver gate. When a gate is driven from two separate gates, each of the driver gates is connected to the gate being driven

through 5Ω resistors. This ensures that each driver gate sees a 5Ω load. To ensure the correct impedance matching for the required fan-out, an additional OR gate buffer is required in front of the COSL XOR gates in the COSL converter circuit.

To ensure the correct output of the converter, it must be ensured that signals propagate correctly through the converter. This is done by buffering signals through gates using the same clocking scheme and can be seen as the additional OR and XOR gates in series to ensure synchronized propagation of the signals through the whole of the converter. Unfortunately this does cause the gate count and the propagation delay to increase. The numbers above the columns of gates indicate which clock phases are used for that column of gates. It can thus also be determined that it requires 4 clock cycles at 20 GHz or 200 ps from the time when a Gray code is applied to the input to the time the corresponding binary code appears at the output.

The complete 4bit SLADC was simulated in WRSpice for a ramp input to generate the Gray code input and to show the conversion from Gray to Binary code. Fig. 5.4 shows the Gray code input and the corresponding Binary output. The propagation delay through the converter can be clearly seen in the delay for the binary code to appear at the output.

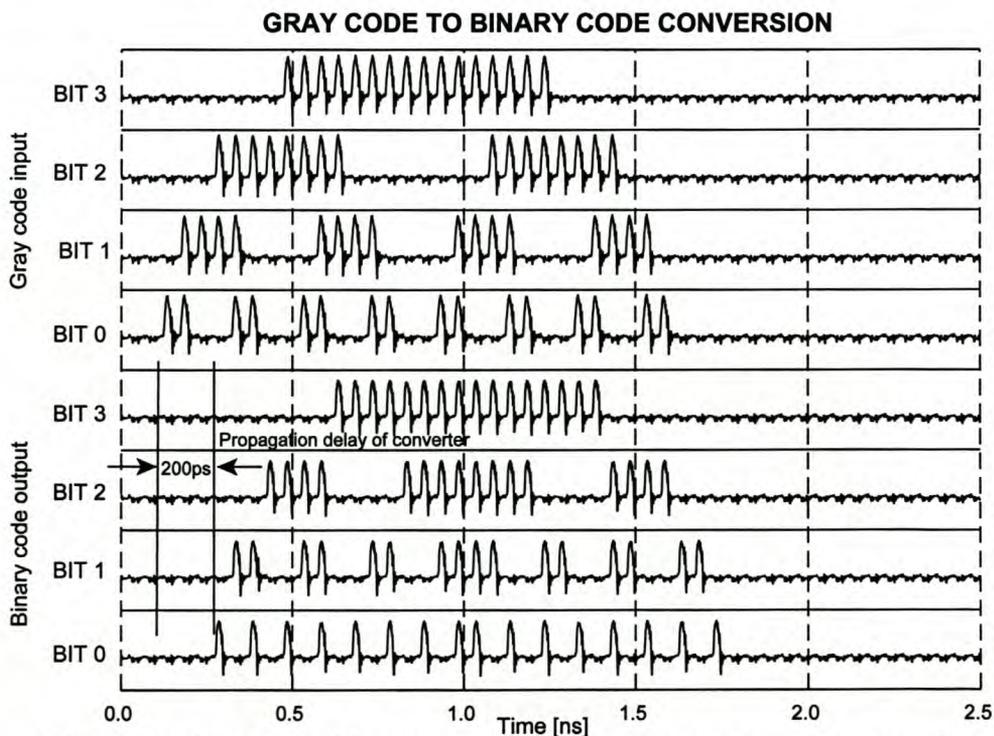


Fig. 5.4 Simulation of the Gray-to-Binary converter confirming the correct conversion from Gray code to Binary code.

5.1.3 Reconstruction of the Input from the Output of ADC

To evaluate the performance of the SLADC it is necessary to convert the output of the SLADC back to an analog signal. A switching logic digital-to-analog converter (SLDAC) is a design in its own right. For our purpose it was sufficient to use the basic resistive network as a DAC directly on the pulsed output of the SLADC. This results in a pulsed output with an envelope proportional to the analog input signal because the COSL pulses are only 1 mV in amplitude.

To obtain an envelope approximately equal to the input, voltage controlled voltage sources (VCVS) were utilized to be able to make a comparison between the input and reconstructed input from the output of the SLADC. This basic DAC is shown in Fig. 5.5. With the gain of the VCVS set to unity, the full scale output of the DAC is approximately 1.25 mV. To obtain output approximately equal to the full scale input requires a VCVS gain of approximately 40.

It must also be noted that when a spectrum is taken of this pulsed reconstruction, a 20 GHz frequency will always be present with the sum and difference components of the clock and the input symmetrically around it. Due to the fact that the COSL pulses, which also contain transients, are used for the reconstruction, it is not possible to make accurate amplitude measurements from these frequency spectrums.

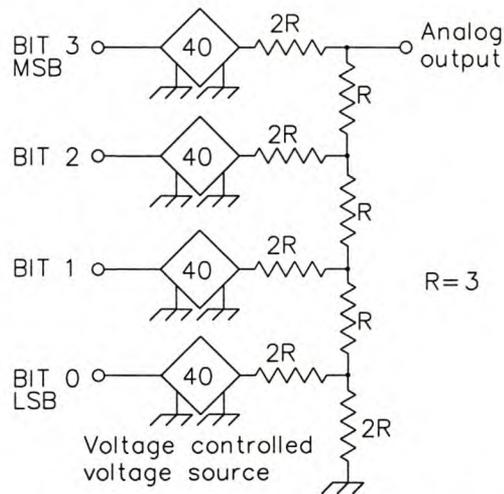


Fig. 5.5 A simple DAC circuit to convert the SL output from the SLADC to an analog signal for comparison with the analog input signal.

5.2 Evaluation of Switching-Logic ADC

It is important to establish the correct low frequency logic operation as well as the high frequency performance of the SLADC. We have chosen the following test conditions:

- Low frequency: Linear ramp input of a slew rate so that the ADC would step sequentially through all the digital levels (16 levels for a 4-bit SLADC).
- Beat frequency: 19 GHz input to determine the wide input bandwidth of the SLC and the SLADC.
- High frequency: 1 GHz, 5 GHz and 10 GHz (Nyquist limit) input signal to determine the maximum input bandwidth for the SLADC.
- Special inputs : Dual frequency input - 4 GHz and a 5 GHz to determine the linearity of the SLADC by checking for intermodulation products.

A square wave input to check for operation of the SLADC and for observing the uneven harmonics contributing to the square wave.

It is important to note that these simulations were done without considering any contributions from any noise sources.

Due to the fact that the current through the series junction of the of the OJS is periodic for both positive and negative values of input current, the comparator cannot distinguish between positive and negative inputs of the same value. The input signal therefore has to be positive and offset by a DC value equal to 50% of the full scale value to ensure that the signal falls in the range from zero to full scale for the particular resolution of the SLADC. All input signals are thus implemented so that it starts at zero or a very small value to keep transient effects from initial jumps in input values to a minimum.

For this reason sinusoidal inputs are offset and delayed to start at a zero value. Further, the first sampling pulse appears at approximately 10 ps from the start of the simulation. This 10 ps is also compensated for in the delay so that the first sampling pulse coincides with the point where the input signal starts at zero. This procedure is illustrated in Fig. 5.6.

The sole purpose of the corrections in the delay of the input signal was to help clearly verify the correct operation of the SLADC by simulation. It will serve no purpose in a practical implementation of a SLADC.

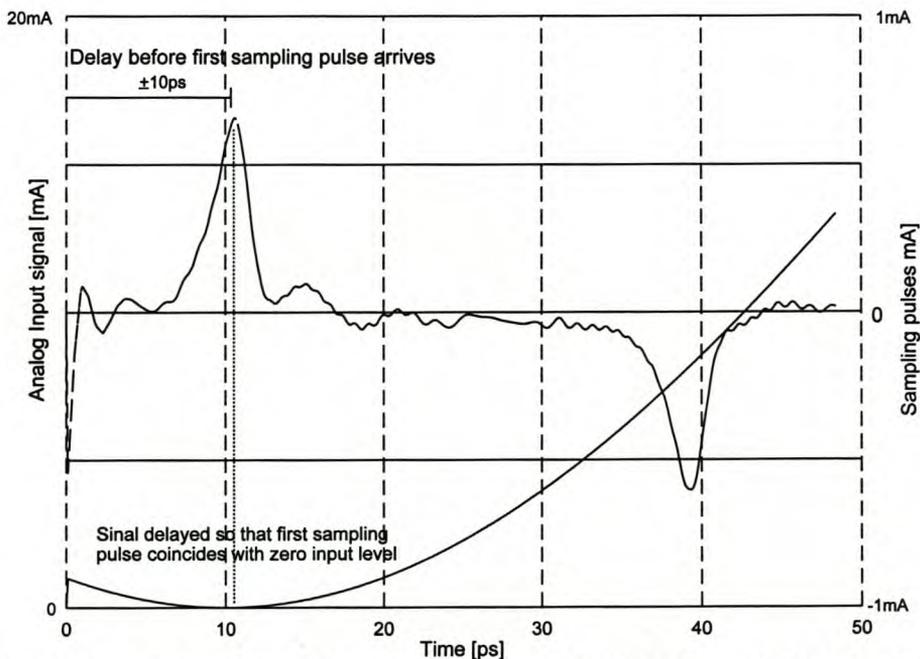


Fig. 5.6 Setting up the input signals for minimum transient effects and to synchronize input with the sampling pulses.

5.2.1 Low Frequency Logic Operation

The correct low frequency logic operation of the SLADC was verified using a linear ramp that increases to full scale and then decreases to zero again. It is required that the digital code steps sequentially through all the 16 levels for a 4-bit SLADC within a time period of 16 sampling pulses. Sampling pulses occur at 50 ps intervals (20 GHz), setting an interval for the ramp of 800 ps. Fig. 5.7 shows the input ramp and the sequential Gray code output, confirming the correct logic operation of the quantizer section.

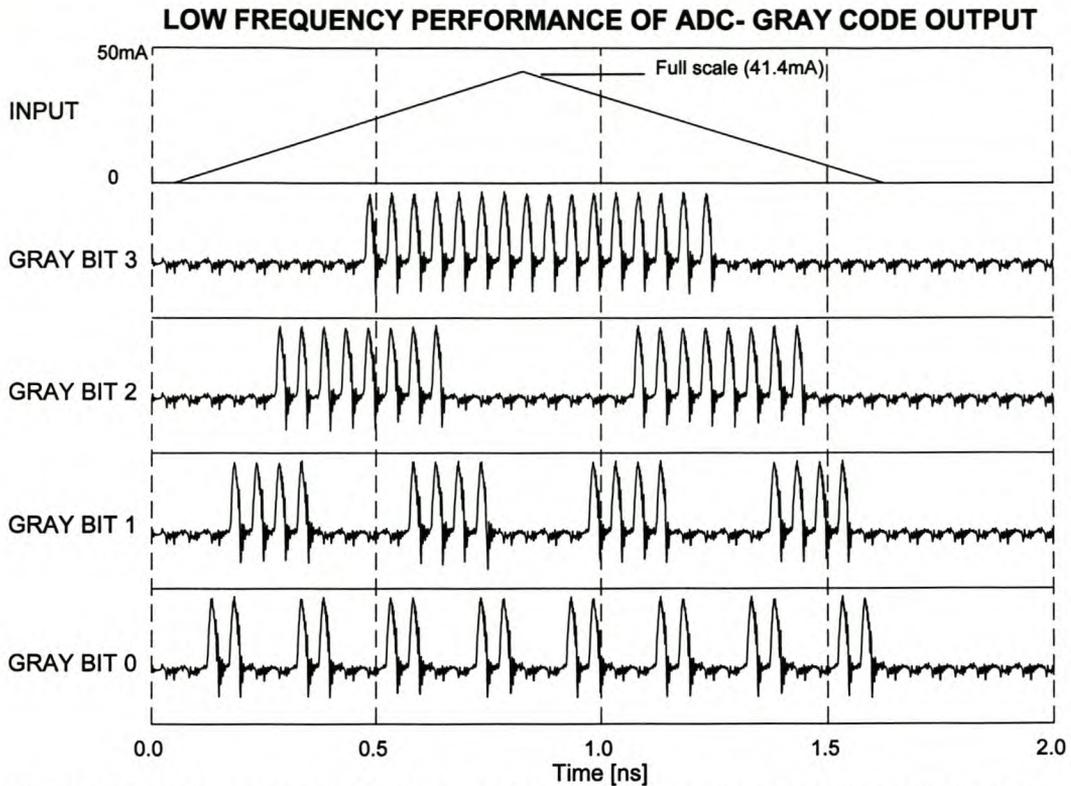


Fig. 5.7 Gray code generated to confirm the correct low frequency logic operation of the SLADC.

The input ramp signal, the pulsed reconstructed input signal together with the converted sequential binary code is shown in Fig. 5.8. This again confirms the correct low frequency logic operation of the SLADC and the Gray to Binary Converter.

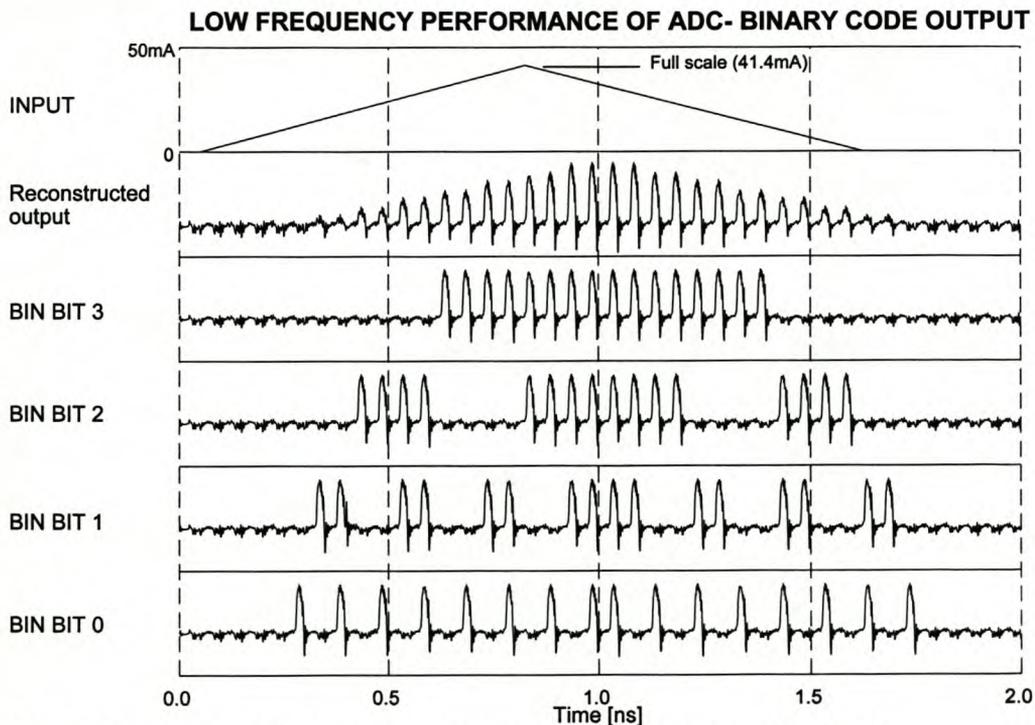


Fig. 5.8 Confirmation of the correct low frequency binary logic output of the SLADC

An enlarged view of the input ramp and the pulsed reconstructed input. is given in Fig. 5.9.

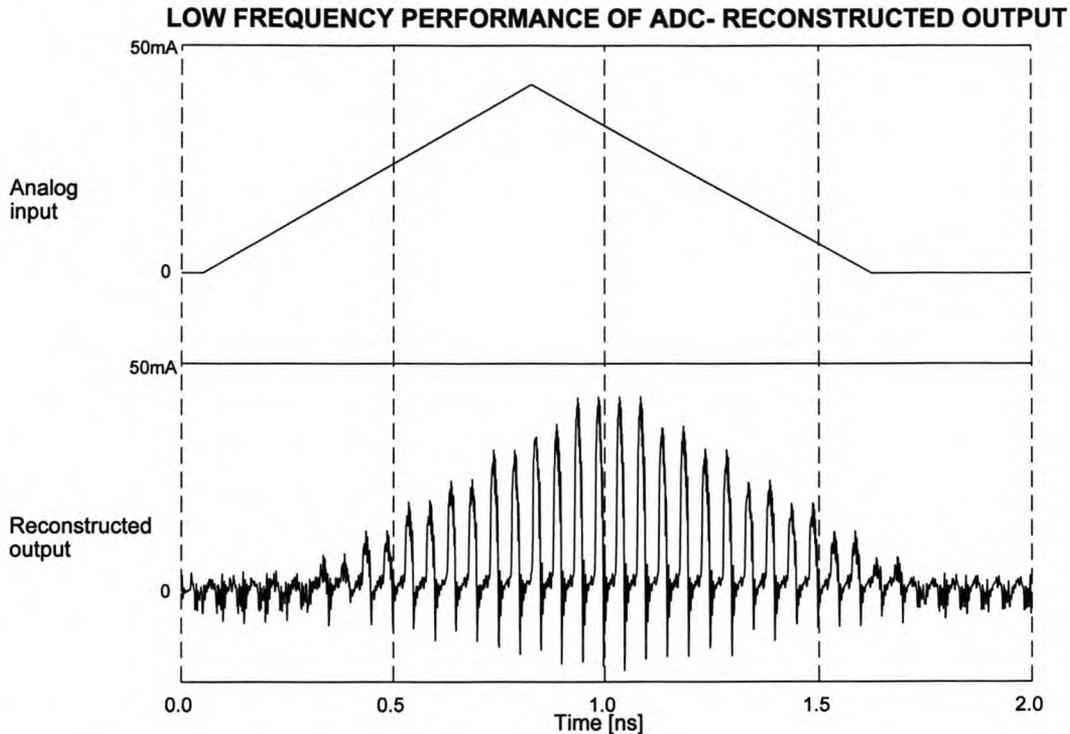


Fig. 5.9 Input ramp signal and the pulsed reconstructed input signal showing the propagation delay through the SLADC

5.2.2 Beat Frequency Simulation

The beat frequency method is used quite extensively by Bradley [17, 18] and Kaplan [19, 20] to demonstrate the wide bandwidth of their comparators. Beat frequency tests are used to display the results of high-speed sampling on a low-speed oscilloscope.

An example of their beat frequency test was an analog input sinusoidal frequency of 19,999995 GHz and a clock frequency of 20 GHz resulting in a beat frequency of 5 kHz which could easily be displayed on an oscilloscope. Between samples, the analog input signal goes through one cycle plus or minus a small increment, depending on which of the clock or input signal frequency is the highest. Successive samples are taken at nearly identical points on the waveform and consequently, most of the output bits will repeat for several samples in a row.

A beat frequency simulation was also performed on the SLADC. An input frequency of 19 GHz full scale was chosen, resulting in a 1 GHz beat frequency. Due to the maximum time that can be simulated within the available memory limitations of WRSpice, it was not possible to simulate a beat frequency of 5 kHz which would require a simulation time of 200 μ s for one cycle of the beat frequency.

Fig. 5.10 shows the 19 GHz input signal, the 50 ps sampling pulses and one cycle of the 1 GHz beat frequency, demonstrating the extremely wide input bandwidth of the flash SLADC .

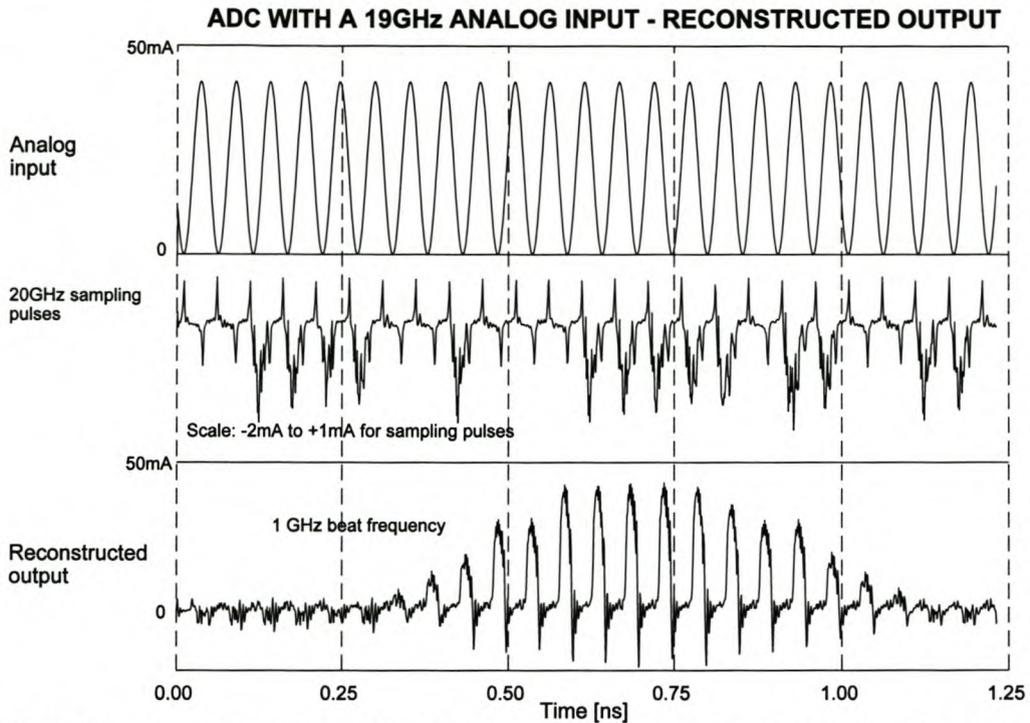


Fig. 5.10 Beat frequency simulation of an SLC with an input frequency of 19 GHz and a sampling frequency of 20 GHz.

The frequency spectrum in Fig. 5.11 shows only the 1 GHz beat frequency component and the translation of the high input frequency to a lower frequency that can be displayed on conventional instruments.

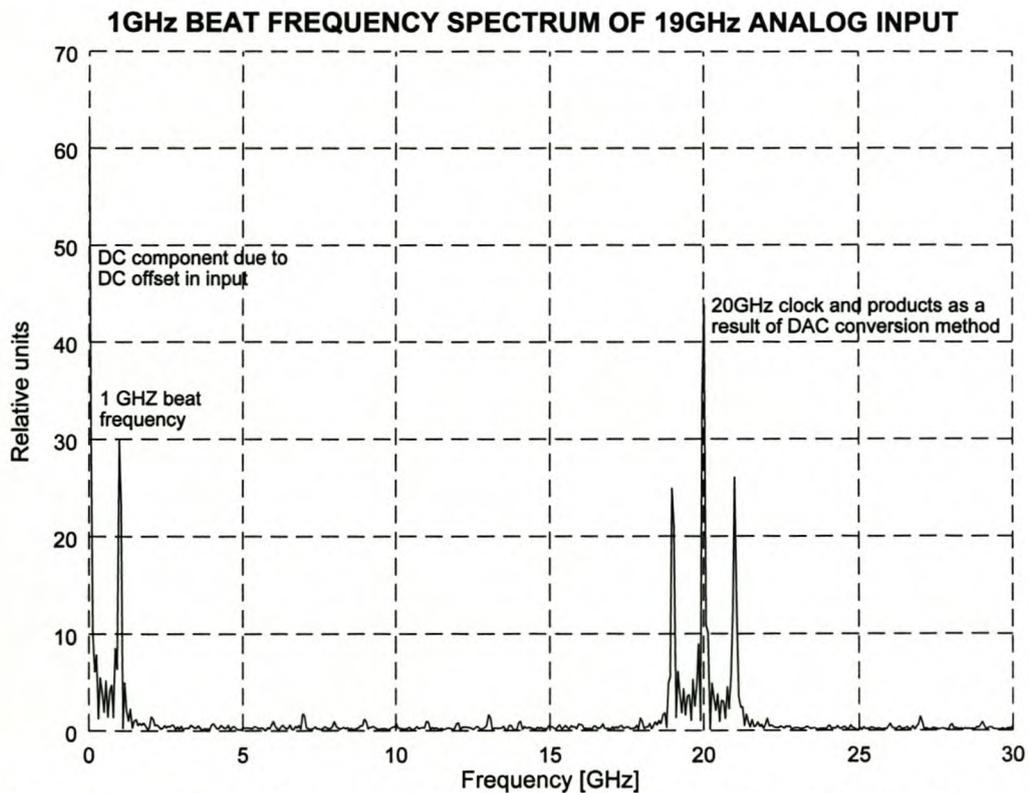


Fig. 5.11 Frequency spectrum showing only the 1 GHz beat frequency component.

5.2.3 Input Bandwidth Evaluation

Sinusoidal input signals of full scale 1 GHz, 5 GHz and 10 GHz were digitized successfully to show the high input bandwidth of the SLADC. The delays for the input signal to synchronize it with the sampling pulses and to ensure that it starts at a value close to zero, are calculated as 740 ps, 140 ps and 65 ps respectively.

Fourier transforms of the pulsed outputs were taken to reveal the frequency components of each of the 3 input frequencies. Fig. 5.12 shows the Gray code generated for the 1 GHz input while Fig. 5.13 provides the converted Binary code and the pulsed reconstruction of the input signal.

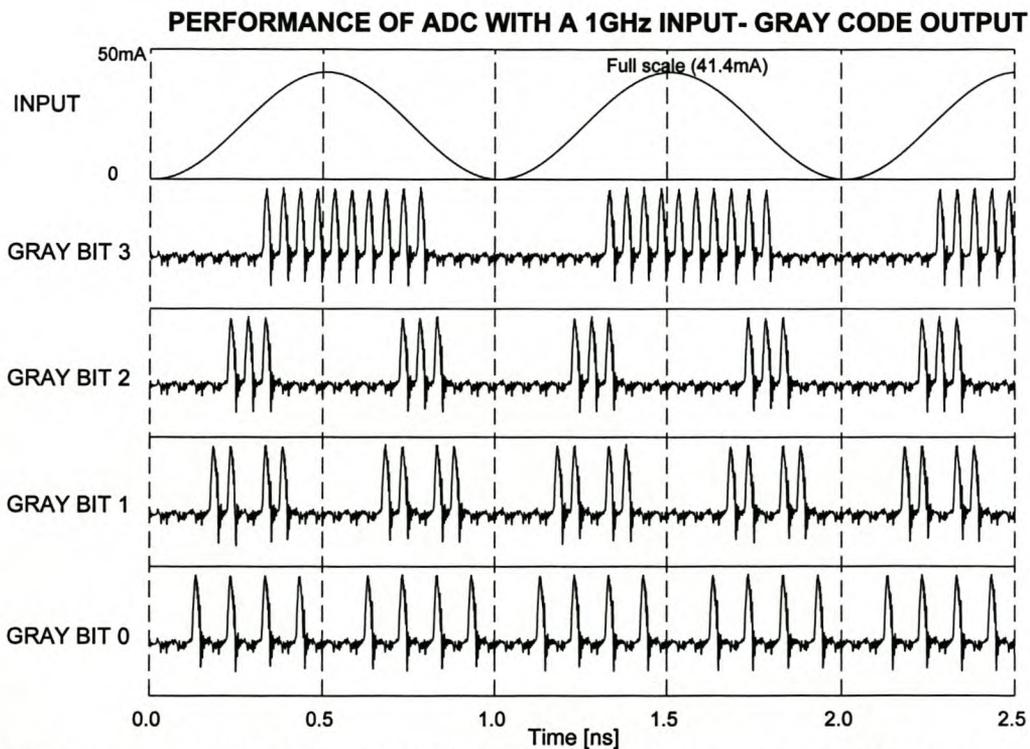


Fig. 5.12 Performance of the SLADC with a 1 GHz input signal showing the Gray-code output.

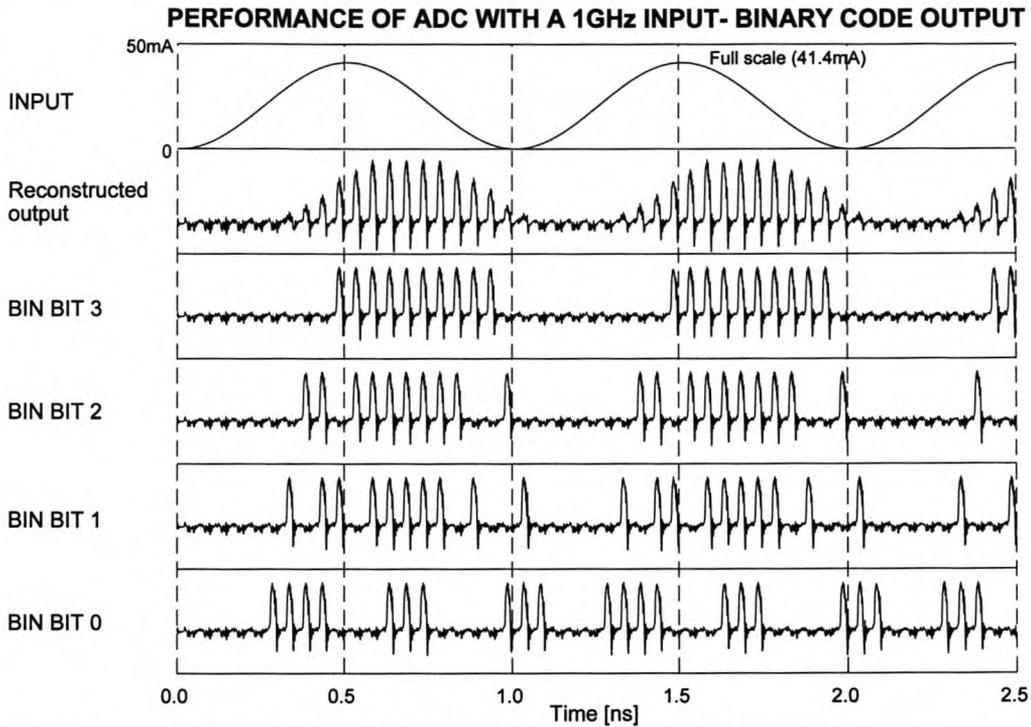


Fig. 5.13 Pulsed reconstructed 1 GHz input and the corresponding binary code.

Fig. 5.14 shows only the input and the pulsed reconstruction of the input signal.

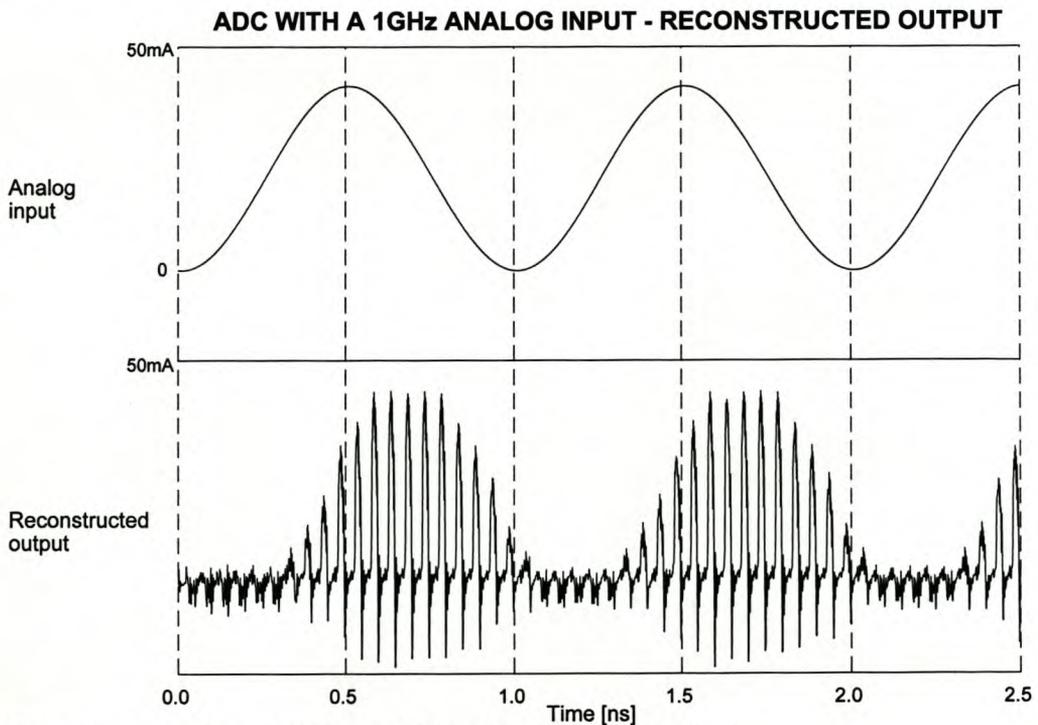


Fig. 5.14 Pulsed reconstructed input for a 1 GHz input signal.

The Fourier spectrum in Fig 5.15 reveals the fundamental 1 GHz frequency and very small uneven harmonic components. It is believed to be caused by a combination of samples taken at the slow turning points of the sinusoidal waveform resulting in quantization error and the

imperfect synchronization of sampling pulses with the input waveform. This results in a few samples being taken at the same logic level which has the effect of “squaring” the reconstructed input signal and causing the uneven harmonics to appear.

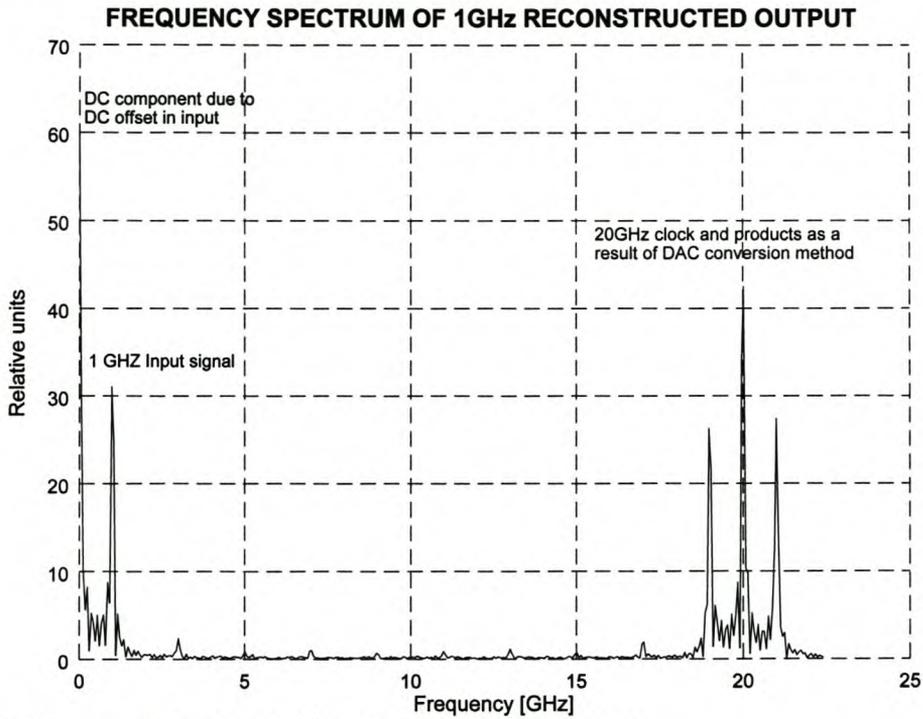


Fig. 5.15 Frequency spectrum for the 1 GHz input signal.

Fig. 5.16 and Fig. 5.17 respectively show the Gray code and binary code generated for a 5 GHz input signal.

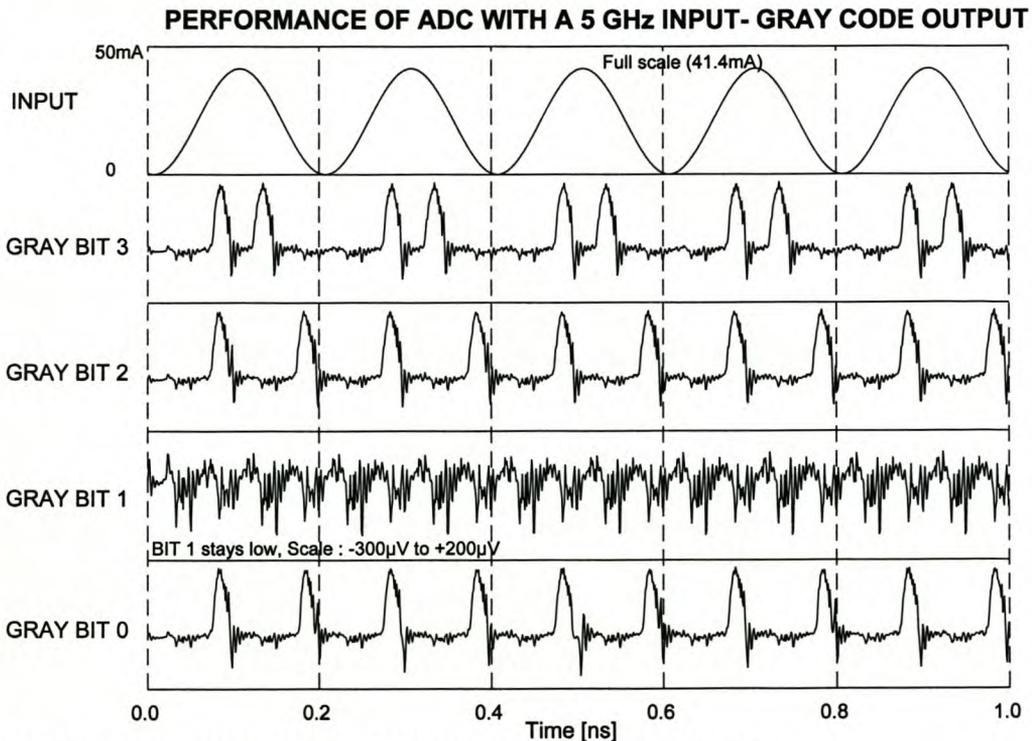


Fig. 5.16 Generated Gray code output for a 5 GHz input signal.

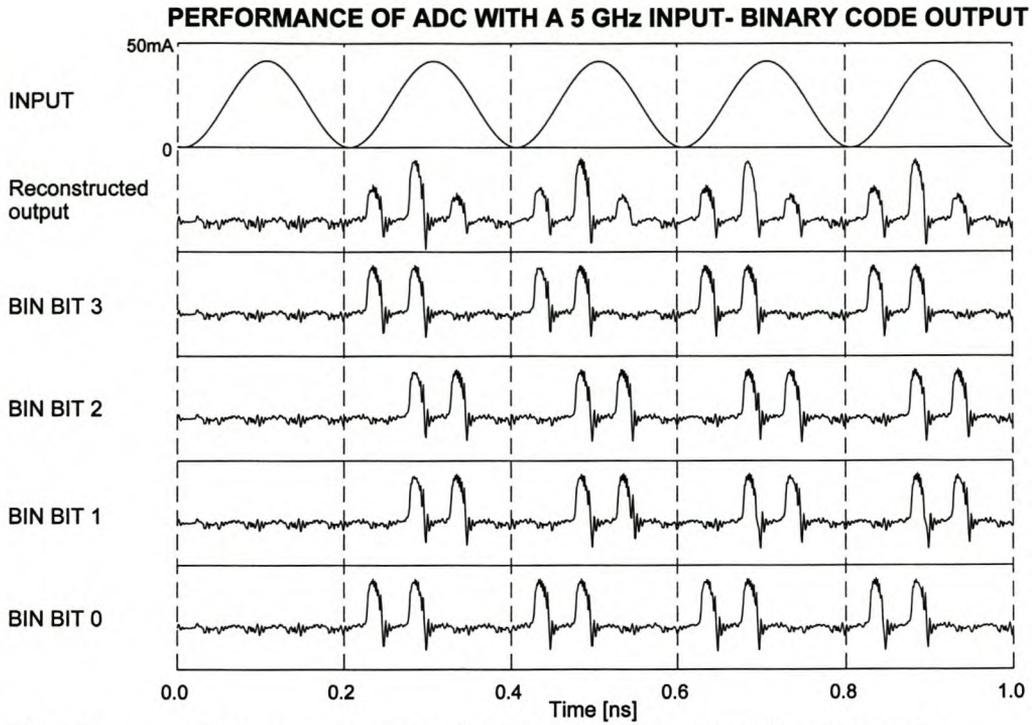


Fig. 5.17 Pulsed reconstructed 5 GHz input and the corresponding binary code.

Fig. 5.18 and Fig. 5.19 show the pulsed reconstructed 5 GHz signal and its Fourier spectrum respectively with only the 5 GHz input component present.

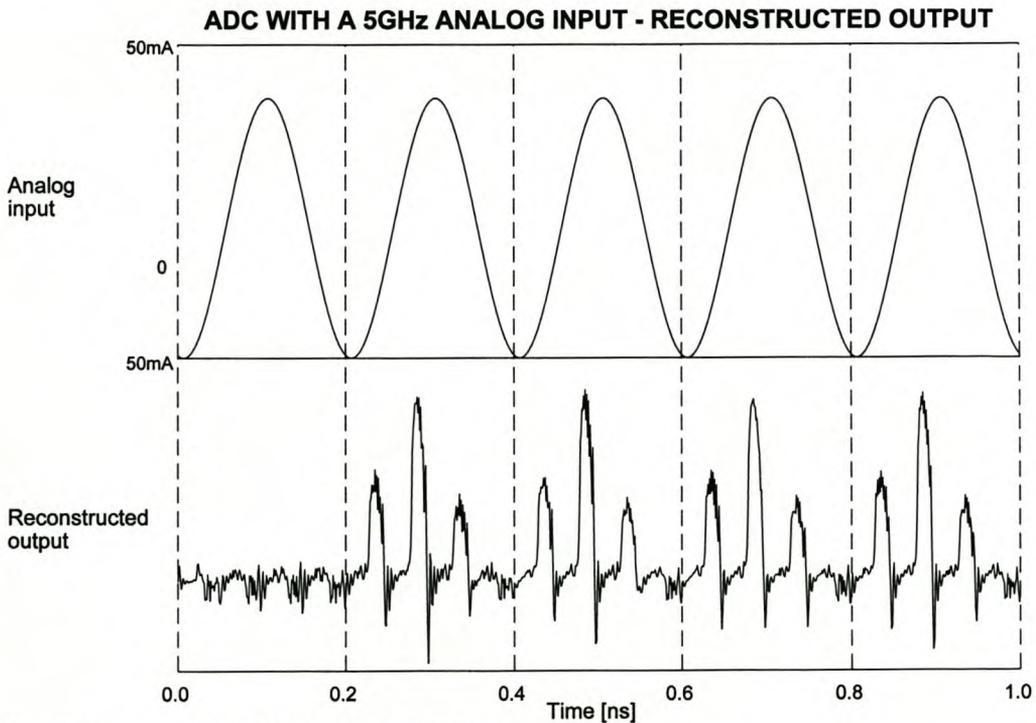


Fig. 5.18 Pulsed reconstructed 5 GHz input signal.

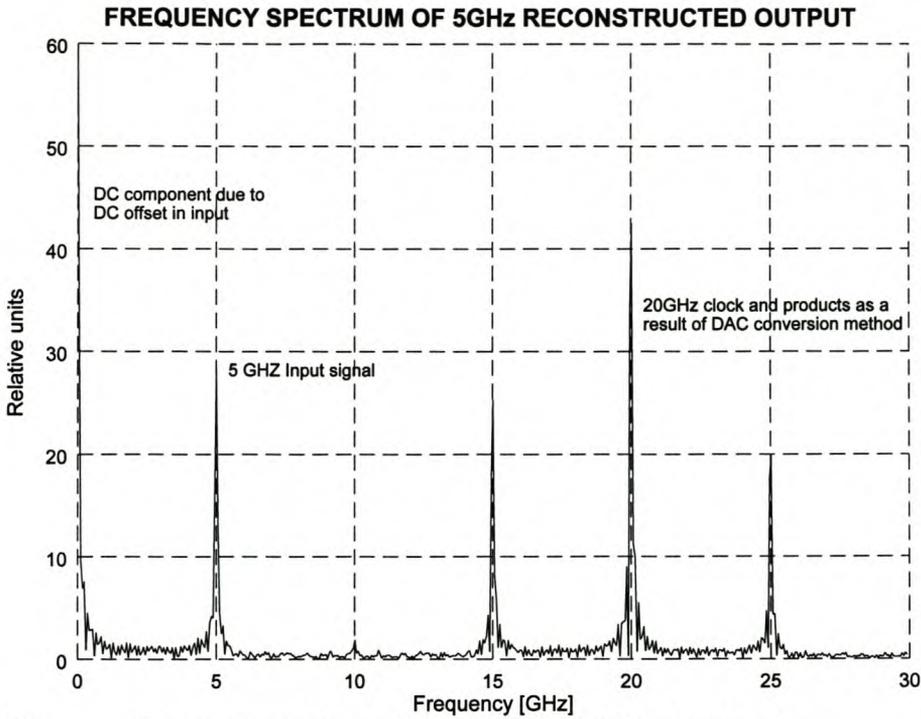


Fig. 5.19 The Fourier spectrum of the reconstructed 5 GHz input signal.

Finally, the SLADC was simulated with a 10 GHz input signal which corresponds to the Nyquist frequency. Only two samples can be taken within one cycle of the input. Sampling was synchronized to sample at the maximum and the minimum, corresponding to full scale and zero input. Fig. 5.20 and Fig. 5.21 show the zero and full scale binary sampling and reconstructed input respectively.

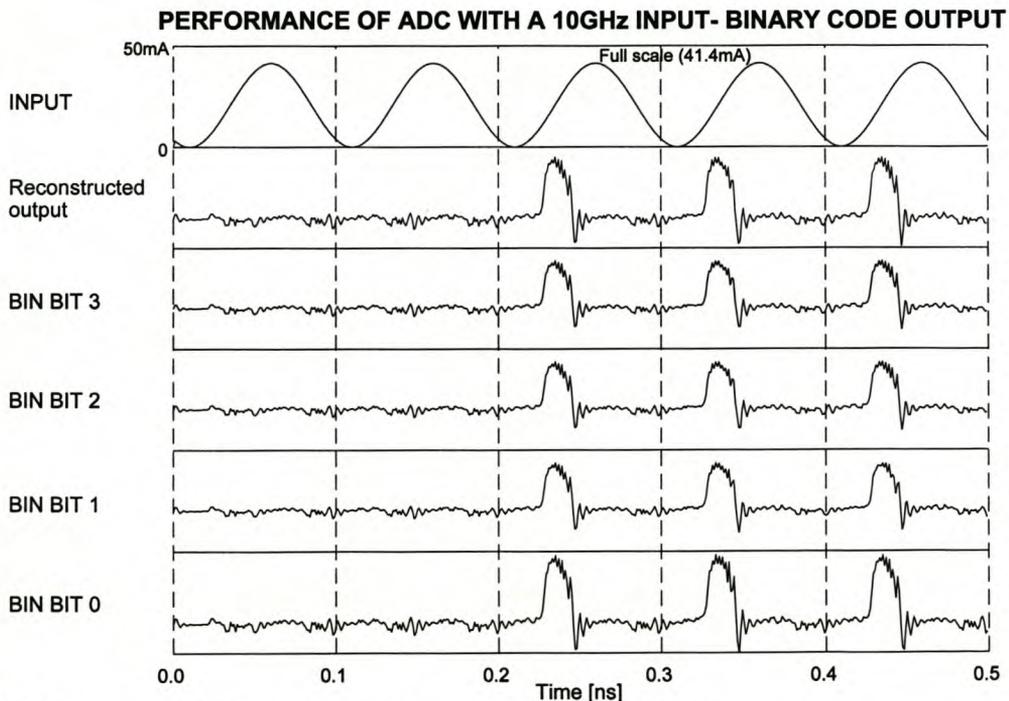


Fig. 5.20 Binary output of SLADC for a 10 GHz input signal.

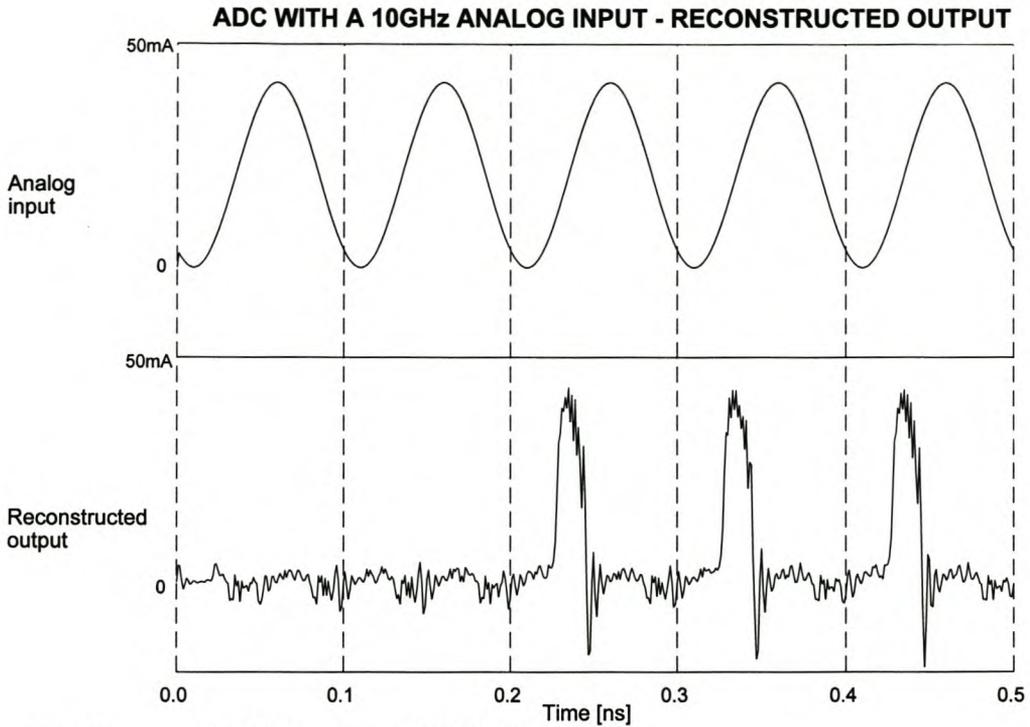


Fig. 5.21 Pulsed reconstructed 10 GHz input signal.

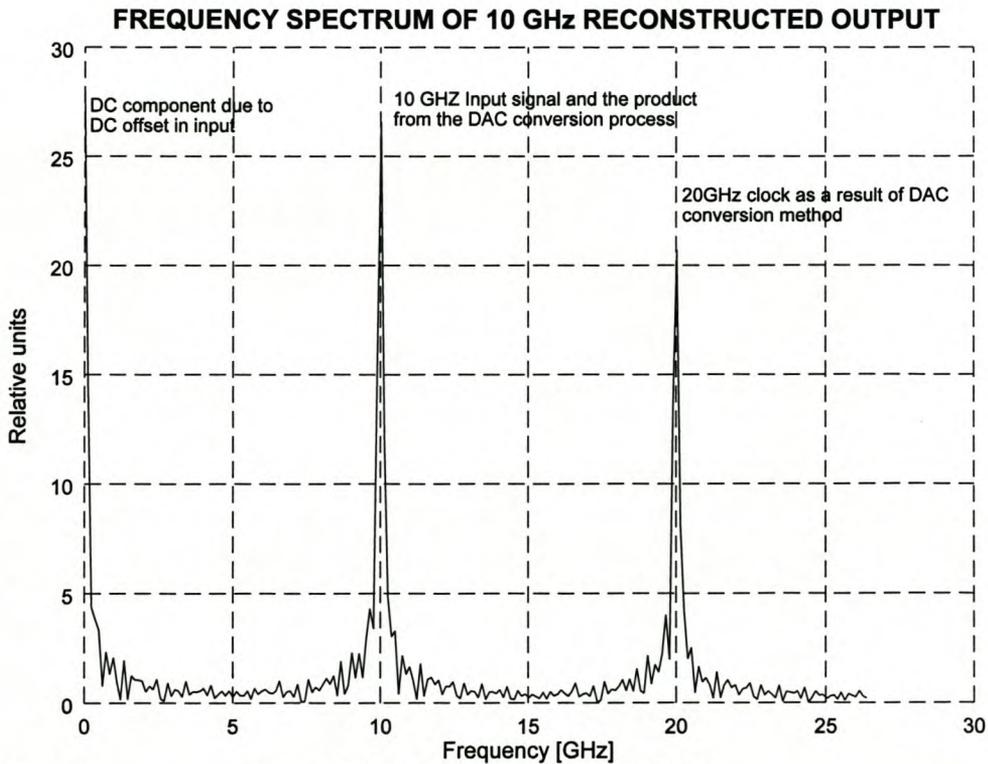


Fig. 5.22 Frequency spectrum for the 10 GHz input signal.

The frequency spectrum for the 10 GHz input signal is shown in Fig. 5.22 Note that the component as a result of the DAC conversion process is also lying at 10GHz causing the amplitude at 10 GHz to be much higher.

5.2.4 Special Input Signals

Three additional input signals were also used in the evaluation of the SLADC. These consists of an input consisting of two closely spaced sinusoidal signals, a square wave input, and a ramp with a final value of 6 times the full scale input.

The frequencies of 4 GHz and 5 GHz were chosen with an amplitude of half of full scale and a DC offset of 25% of the full scale value for the first special input signal. This results in a total DC offset of 50% of full scale and a combined full scale signal input respectively.

For this input, any non-linearities would result in intermodulation products which would include 2nd order product $(F_1 - F_2) = 1$ GHz and 3rd order products $(2F_1 - F_2) = 6$ GHz and $(2F_2 - F_1) = 3$ GHz. The input signal together with the pulsed reconstructed input is shown in Fig. 5.23.

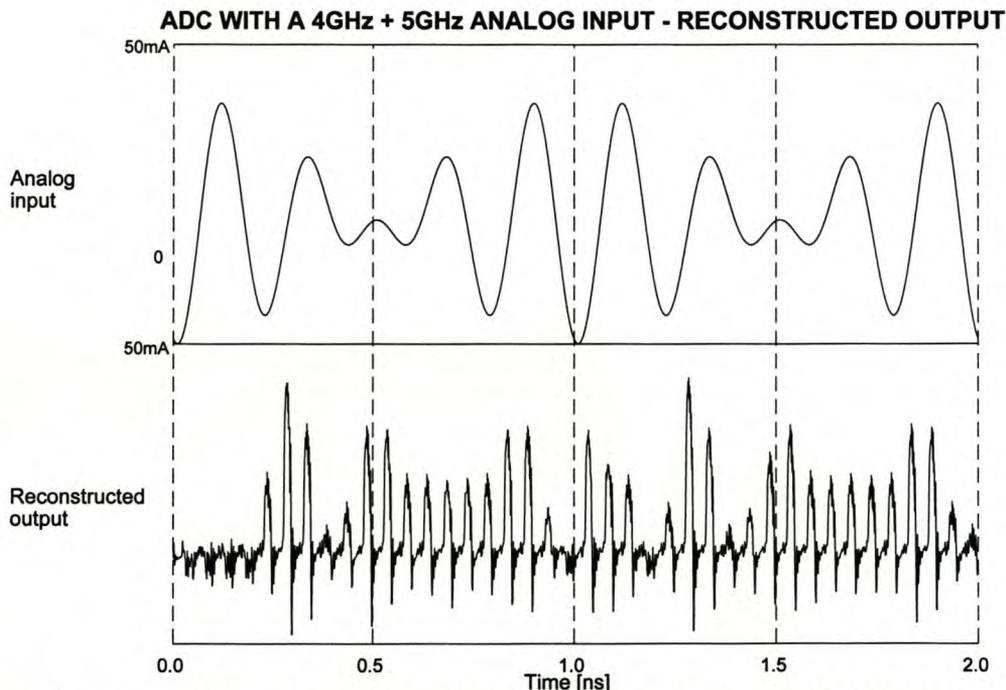


Fig. 5.23 Pulsed reconstructed input signal for the dual frequency (4 and 5GHz) input.

Fig. 5.24 shows the Fourier spectrum of the pulsed reconstructed input for the dual frequency input. It can be seen that the only frequency components present are the two input frequencies of 4 GHz and 5 GHz. No intermodulation products are visible showing there are no linearities present in the SLC or SLADC.

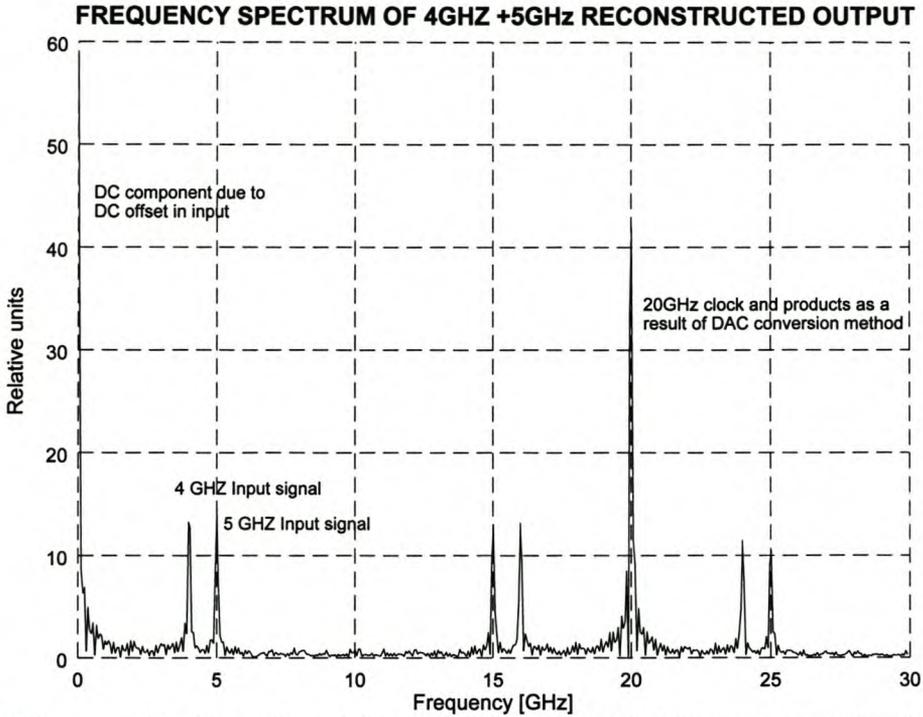


Fig. 5.24 Fourier spectrum of the pulsed reconstructed dual frequency input signal showing only the two input frequency components and no intermodulation products at $(F_1-F_2) = 1$ GHz and $(2F_1-F_2)=6$ GHz and $(2F_2-F_1)=3$ GHz.

Secondly the SLADC was subjected to a 1 GHz full scale square wave input signal. Fig. 5.25 shows the square wave input, the reconstructed input and the corresponding binary output of the SLADC.

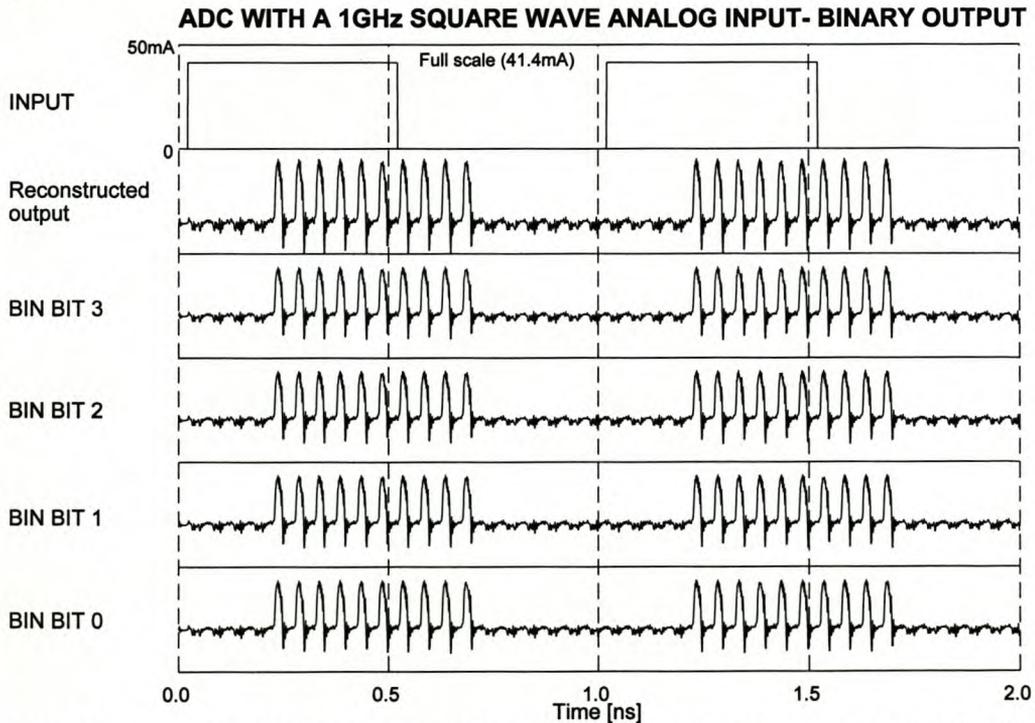


Fig. 5.25 Pulsed reconstructed input and the corresponding binary output of the SLADC

The Fourier spectrum of the pulsed reconstructed square wave in Fig. 5.26 reveals the fundamental 1 GHz frequency component as well as the uneven harmonics that forms the square wave.

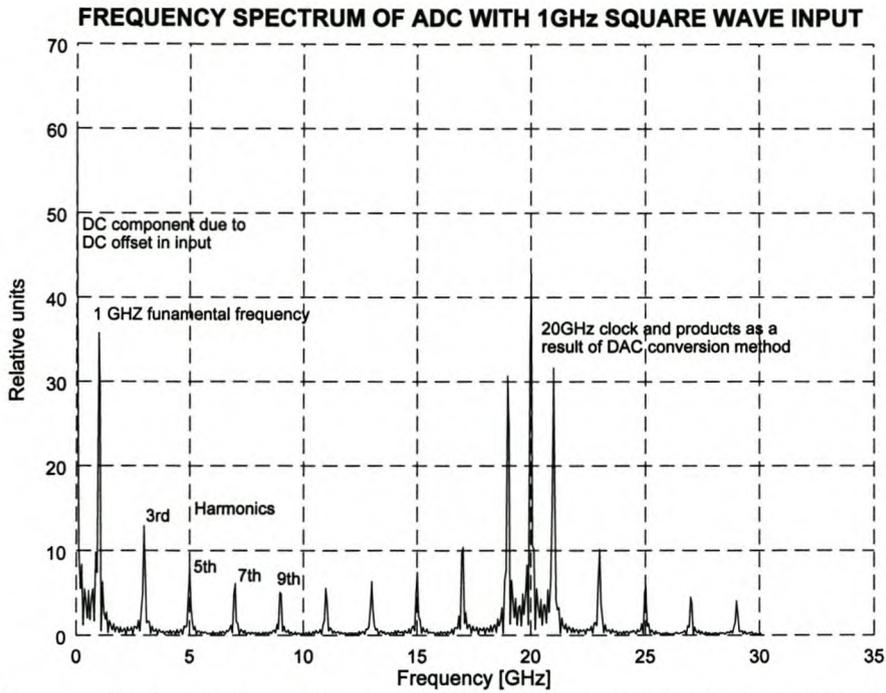


Fig. 5.26 Fourier spectrum of the square wave input revealing the fundamental and the uneven harmonics forming the square wave.

The last test input is the ramp with a final value equal to 6 times the normal full scale input of 41.4 mA. Fig. 5.27 shows the folded pulsed reconstructed input and the corresponding binary code.

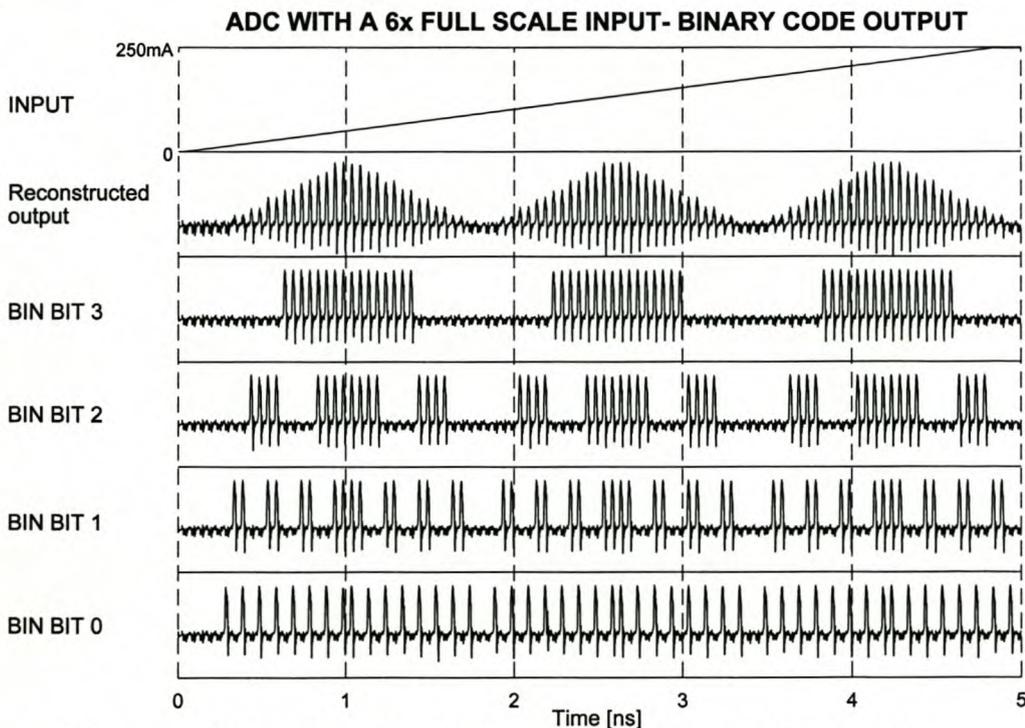


Fig. 5.27 SLADC with input increased beyond full scale, resulting in a folded reconstruction.

This input spans over 96 quantizer levels and shows sufficient transitions or dynamic range for an SLADC with 6 bits of resolution.

■ Summary

This Chapter presented the design of a 4-bit Gray-to-Binary Converter and the construction of a 4-bit SLADC by utilizing the SLC and the converter. A simple DAC converter is given to be utilized in the evaluation of the SLADC performance.

The SLADC was then evaluated for its low frequency logic operation, high frequency and maximum input bandwidth, linearity and dynamic range. A beat frequency simulation was performed to demonstrate the high bandwidth of the SLC and SLADC. Special waveforms such as a square wave input and a large input signal of 6 times the full scale value were utilized to demonstrate sufficient dynamic range for more than 6 bits of resolution.

The SLADC functioned correctly and achieved a input bandwidth of 10 GHz at a resolution of 4 bits with excellent linearity and dynamic distortion.

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Thermal noise simulations

- **Introduction**
- 6.1 **Implementation of noise in simulations**
- 6.2 **Effects of noise on the SLC**
- 6.4 **Spur Free Dynamic Range of the SLADC**
- 6.5 **Optimization with thermal noise**
- **Summary**

■ **Introduction**

Noise is a very important consideration in comparators and ADCs. This chapter describes how noise was implemented in the simulations of the SLC and SLADC. The Spur Free Dynamic Range (SFDR), an important figure of merit that provides a measure of the performance of an ADC, can also be determined by including noise in the SLADC simulation.

6.1 Implementation of noise in simulations

The implementation of thermal noise described by Jeffery [41] was adopted. Thermal noise is modelled in circuits by current sources with random values, in parallel with each resistor and Josephson junction in the circuit. Nyquist [42] has formulated the thermal agitation of charge in conductors into the Nyquist equation

$$i_{rms} = \sqrt{\frac{4k_B T}{R}} f_c \quad (42)$$

which describes the rms current fluctuations of the current sources. In this equation k_B is Boltzman's constant, T is temperature, R is the resistance. The cutoff frequency $f_c = 1/2\Delta$ where Δ is the spacing between random numbers. Should the noise be bandwidth limited, f_c represents the bandwidth.

By utilizing Equation 42 the noise is implemented in the simulations through a gaussian random number generator defined in WRSpice [40] by the text line

```
*@ define noise(r,t dt,n) gauss(sqrt(4*boltz*t/(r*2*dt)), 0 dt,n)
```

Noise is then incorporated into the simulation by applying current sources in parallel with every resistor and Josephson junction in the circuit and calling the noise function defined above. A typical call in WRSpice to the noise function is:

```
I_noise node+ node- noise($ R_val, $Temp, $t_min, $Noise_type)
```

where *node+* and *node-* refers to the circuit nodes of the parallel resistor or the Josephson junction, *R_val* the value of the resistor or Junction resistance, *Temp* the temperature, *t_min* the step size Δ and *Noise_type* to the integer which defines whether the type of noise is first-order interpolated or piece-wise-linear steps. Simulations by Jeffery[41], however, indicates that as long as the Δ time scale spacing of the noise is small compared with the time constants in the circuit, the simulation output is independent of the exact form of the input noise function.

For the noise simulations a noise spacing of $\Delta = 0.5\text{ps}$ was used. Circuit transients, which is required to be less than Δ for the Spice simulator, were calculated at time intervals of 0.1ps .

6.2 Effect of noise on the SLC

Noise was first implemented in the SLC circuit utilizing the same Fail/Pass evaluation method, described in Section 4.4, to determine the effect of noise on the comparator. Fig. 6.1 shows the

“Pass” output for the SLC with thermal noise incorporated into the simulation.

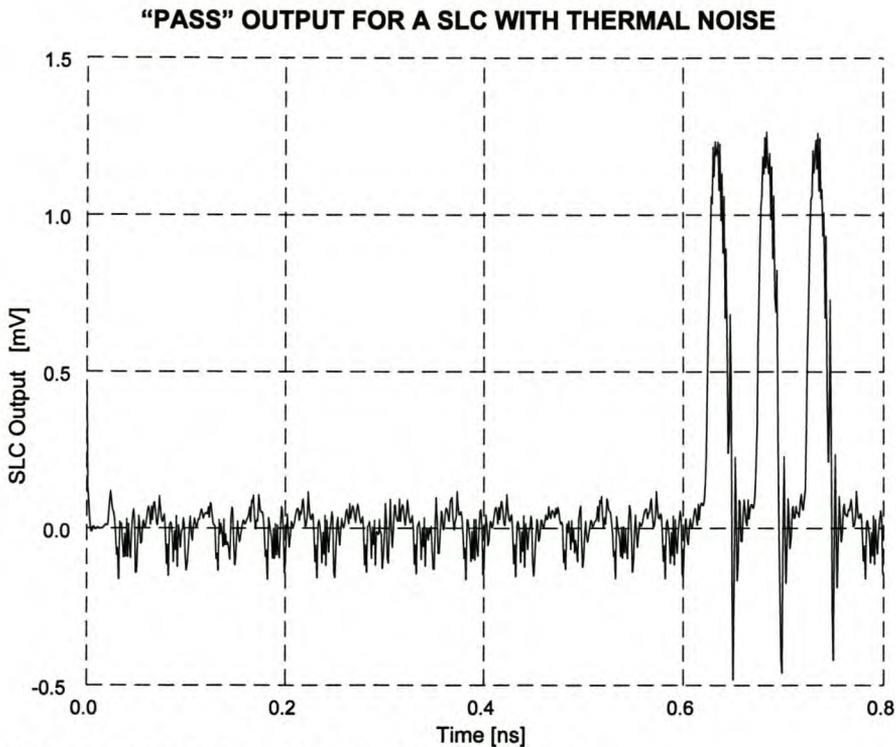


Fig. 6.1 The correct output for a SLC “Pass” with thermal noise.

A number of correct single simulations with noise indicated that it would not be possible to determine the cumulative effect of noise on the SLC from single simulations. A test similar to that of a Bit Error Rate (BER) was utilized to evaluate the performance of the SLC with noise.

The BER, used to determine bit errors for digital circuits, cannot be used directly in the case of the SLC. The SLC is inherently an analog system where an analog input crosses a threshold set by the comparator. The threshold separate two regions or levels and noise can thus cause a comparator with an analog input level near its threshold to switch to the other level. Digital circuits, on the other hand, have a large margin between logic “0” and logic “1” making it less sensitive to the effects of noise.

The Fail/Pass test for the SLC is thus a more stringent test than the BER for digital circuits and it is expected that the SLC would make more errors due to the effect of noise. The BER for digital circuits would thus not be applicable as a test for the inherent analog SLC. The principle of BER, however, was adopted as a measure to determine performance of the SLC with noise. The SLC was simulated 10 000 times with noise and evaluated with the standard Fail/Pass test. Only 3 simulations out of the 10 000 simulated, failed.

Ruck *et al* [46] have measured the BER of a HTS RSFQ comparator, integrated in a ring oscillator. A BER of less than 10^{-11} has been observed at a temperature of 39K. The BER of the two different architectures (SLC and RSFQ), however, cannot be directly compared due to the fact the one input increase linearly while the other is still an RSFQ logic pulse.

6.3 Spur Free Dynamic Range of the SLADC

The simulation of noise was further extended to the complete SLADC to evaluate the effect of noise on the complete circuit which include the resistive ladder divider network, the comparator section as well as the Gray-tot-Binary converter.

The input signal was again reconstructed using the simple DAC with the FFT taken of the reconstructed input. The SFDR can then be determined from this frequency spectrum.

The SFDR is the ratio of the largest possible input signal to the largest spurious component within the relevant frequency bandwidth of the power spectrum. Anything that affects the linearity of the comparators, such as dynamic digital errors, timing errors as well as mismatched comparator thresholds can lead to the degraded SFDR. A 4-bit ADC can at most have a SNR of $6.02 \cdot 4 + 1.76$ or approximately 26 dB.

Fig. 6.2 shows the frequency spectrum for the SLADC with noise and a 1 GHz input signal. This input was chosen as it shows small components at 2nd and 3rd harmonics due to small non-linearities in the system. A SFDR of approximately 21.7 dB is obtained.

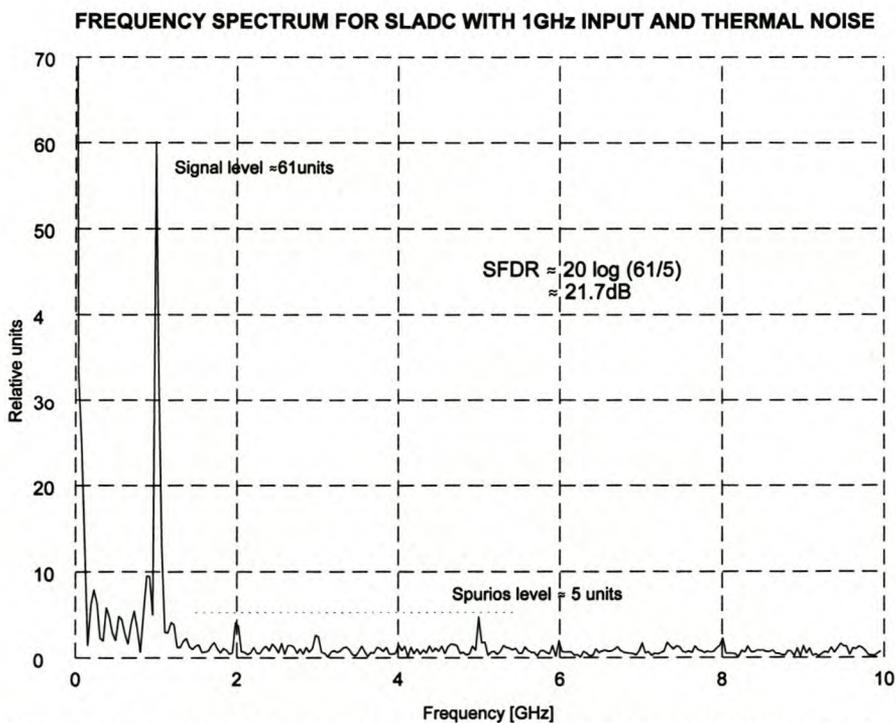


Fig. 6.2 Frequency spectrum for the SLADC with thermal noise for a 1GHz sinusoidal input.

Fig. 6.3 shows the frequency spectrum for the SLADC with noise and a 5 GHz input signal. The SLADC now shows a SFDR of approximately 26.7dB. This confirms the maximum theoretical SFDR of 26 dB as there is no visible spurs in the spectrum.

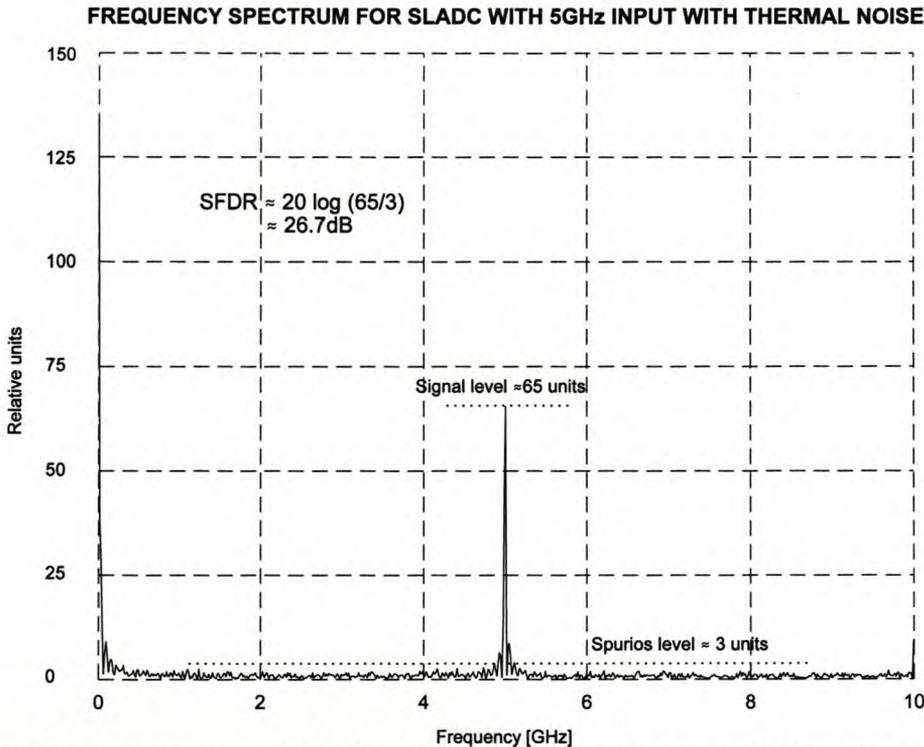


Fig. 6.3 Frequency spectrum for the SLADC with noise for a 5 GHz sinusoidal input signal.

It must be noted that this calculation is not an accurate reflection of the SFDR, however it does provide some indication of the expected SFDR. This is due to the very simple DAC used to reconstruct the input signal as well as the low resolution of the frequency spectrum. To obtain higher resolution the SLADC circuit was simulated for a much longer period. The spectrum in Fig. 6.3 was obtained by simulating the SLADC for 50ns to obtain a higher resolution for the FFT. The spectra in Fig. 6.2 and Fig 6.3 are voltage spectra and a must be taken into account when calculating the SFDR.

According to Kadin [43] there is a general tradeoff between the dynamic range of an ADC and the frequency bandwidth for any given device technology where the range decreases approximately in inverse proportion to the maximum frequency. It is thus expected that the SFDR for the SLADC would be less than that for lower bandwidth ADCs reported. The Rockwell commercial 6-bit 6Gs/sec 3GHz input bandwidth ADC achieved a SFDR of 36dB compared to a theoretical 37.9dB SFDR for a 6-bit ADC. It is thus believed that the SFDR obtained for the SLADC is within the expected range.

6.4 Optimization with thermal noise

The complete optimization process of the comparator for manufacturing process variations discussed in Chapter 4, could effectively now be repeated to include noise. The effect of noise has been investigated for a number of key components. These include the DC bias resistor, the resistors feeding current from the clock shaper and the pulser to the comparator. The change in the values for these components were negligible.

■ Summary

The effects of noise on the SLC and the SLADC were investigated in this chapter.

Out of 10 000 SLC simulations with thermal noise only 3 did not pass. The output of the SLADC, directly after the comparators, is in Gray code and a 1-bit error in even the most significant bit comparator will only cause a 1-level error in the output of the ADC.

The SLADC shows a SFDR of approximately 21.7dB for a 1GHz input with small visible harmonic components. A SFDR of approximately 26 dB confirms the maximum theoretical achievable dynamic range when a 5GHz input is applied with no visible harmonic components or spurs.

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Layout of a 4-bit SLC sampler circuit

- **Introduction**

- 7.1 **The Hypres design rules and layout techniques**

- 7.2 **Impedance matching of clocks and inputs/outputs**

- 7.3 **4-bit SLC sampler circuit layout**

- **Summary**

- **Introduction**

The layout for the superconducting SLC sampler circuit is discussed with reference to the Hypres manufacturing process. The procedure followed in the layout of the components of the circuit will be discussed with specific mention to line widths for impedance matching.

7.1 The Hypres design rules and layout techniques

The layout for the SLC sampler circuit was done in the 1kA, tri-layer, all niobium process according to the latest design rules, Rev. 19 specified on the Hypres website[44].

The latest design rules provide many advantages over previous revisions. Some of these include a 0.1 μm resolution for junction areas and a more accurate specification of the lost area for square junction areas. This enables the designer to specify and obtain junction areas with greater accuracy. Contact resistance for resistors, however, were not specified in the new design rules. The values were adopted from the previous revision.

Spread sheets were set up to calculate junction areas, resistor and inductor dimensions as well as line widths for impedance matching of the 3-phase clocks. Parameters such as offsets, bias, lost area of junctions, contact resistance, resistance and inductance of corners were incorporated into the spreadsheets.

7.2 Impedance matching of clocks and inputs/outputs

It is important to match the impedance of all sections of the complete SLC sampler circuit to each other. This is to prevent “ground bounce” caused by an unbalanced three phase clock. An unbalanced three phase clock can cause current to flow in the ground plane with the effect that all levels will float above ground and “bounce” as the currents in the ground changes.

Impedance matching is done on chip to match the different sections of SLC sampler circuit. These sections can be grouped in the SLC clock pulsers, SLC clock shapers, OR gate input stages, OR gate output stages and the amplifier clock inputs.

The junction in the SLC clock pulser is assumed to be a short circuit for most of the time and the clock will thus see an impedance of 21.3 Ω . The clock shaper clamps the voltage at 2.8V while the clock amplitude is 10mV. Thus a current of $10\text{-}2.8\text{mV}/5\Omega = 1.44\text{mA}$ will enter the clock shaper circuit. The impedance seen by the clock can therefore be calculated as $10\text{mV}/1.44\text{mA}$ or 6.9 Ω . Similarly the impedance for the OR gate input stage and OR gate output stage can be calculated to be 6.9 Ω and 13.9 Ω respectively. The output of the amplifier switches to the gap voltage and the impedance for the amplifier seen by the clock can be calculated in the same way to be 34 Ω .

The layout of the SLC sampler circuit was done in the form of a grid with the four bits as the rows and the columns consisting of the comparators, OR-gate buffers and the amplifiers. The columns of the convertor are organised according to the propagation of the 3-phase clocks through it. The clocks are then distributed from the top down each column. First the last row of a specific column, of the same phase, is connected to the row above by a micro strip line of the same impedance. The row above is then connected to the parallel combination below by a micro strip line of impedance equal to the parallel combination of impedances of the two rows below.

Finally, the three phases of the clock is matched so that each phase sees the same impedance when entering the chip. All phases are matched to the phase with the lowest impedance. Phase

three is not used and is terminated with a resistance of value equal to that of the lowest phase impedance. Phase 1 of the clock has the lowest impedance of 0.74Ω requiring a micro strip of width approximately $238 \mu\text{m}$ in layer M3. Phase 2 has an impedance of 2.47Ω requiring an M3 micro strip of approximately $69 \mu\text{m}$. A resistor of 1.07Ω in parallel is needed to match it to phase 1. Phase three is terminated in two parallel 1.49Ω resistors to also match it to phase 1.

The four outputs from the SLC sampler circuit is amplified and matched with a co-planar waveguide (Wen[45]) to approximately 50Ω before it is connected to the output pads of the chip. The impedance for a co-planar waveguide with an $\epsilon_r = 11.9$ for Silicon and a ratio of the width of the conductor to the width of the track etched in the ground plane of $w/a = 0.5$, is approximately 47.5Ω . Perold [6] has kindly made the layout available for incorporation in the layout of the SLC sampler circuit.

External interface connections are provided for DC bias/trim for the pulser circuit and read-out circuit of each of the four comparators, a common trim for all the COSL OR gates and a common DC bias for the COSL OR gates and amplifiers.

7.3 4-bit SLC sampler circuit layout

Fig. 7.1 shows the complete layout of the SLC sampler circuit and the external connections to the chip pads.

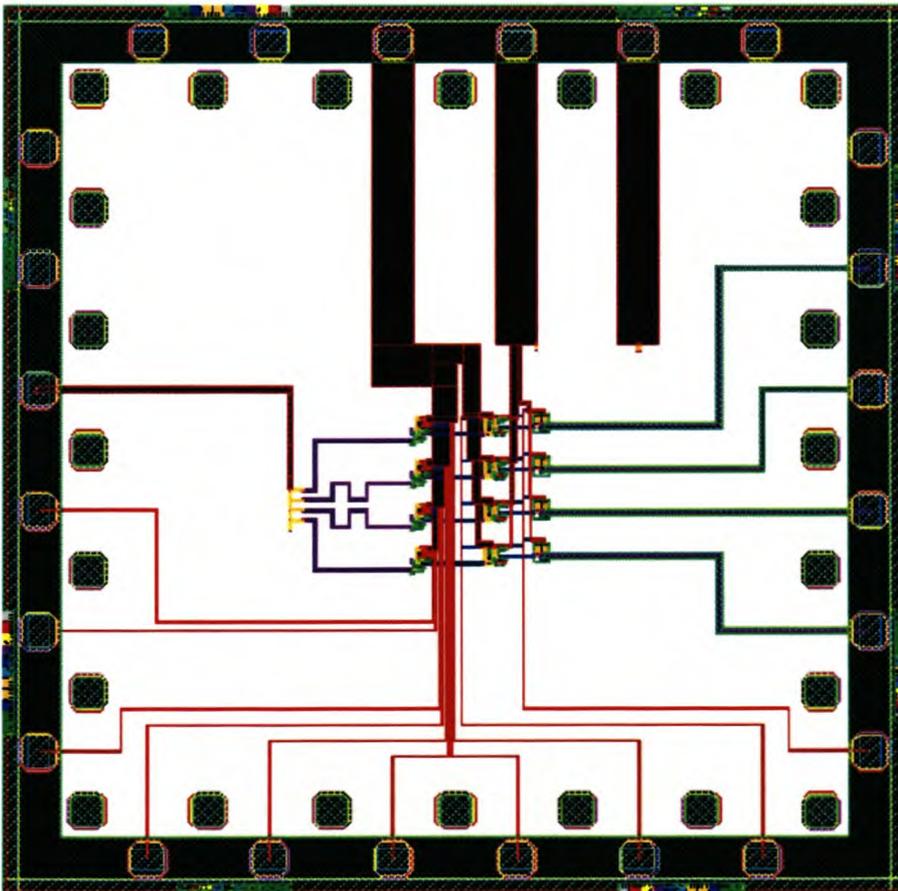


Fig. 7.1 The complete LASI layout of the SLC sampler circuit.

Fig. 7.2 shows the resistor divider network, comparators, COSL OR gates and the amplifiers of SLC sampler circuit and their interconnections. Fig. 7.3, Fig. 7.4 and Fig. 7.5 zooms in on the SLC, COSL OR gate and the amplifier respectively.

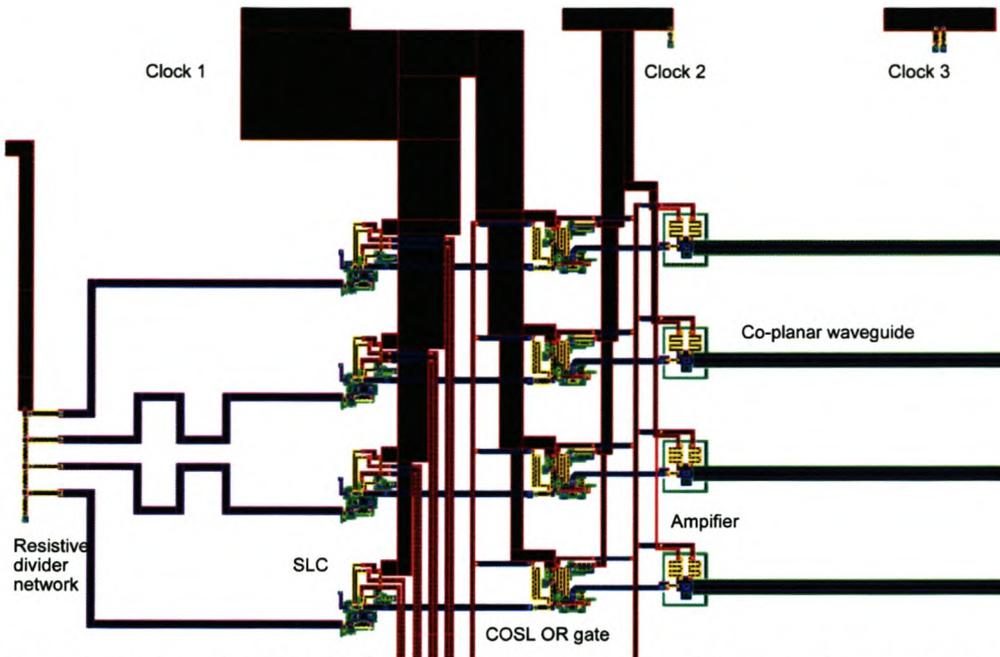


Fig. 7.2 A closer view of the SLC sampler layout showing the resistive divider network, comparators, COSL OR gates and the amplifiers.

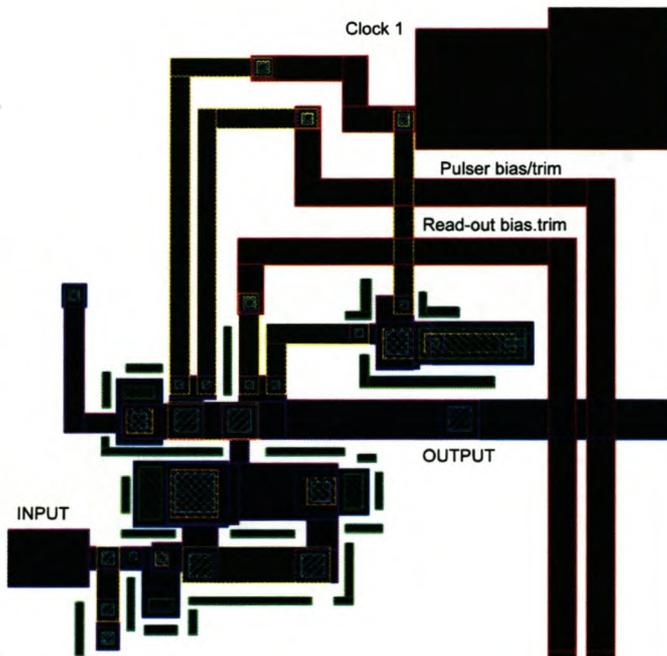


Fig. 7.3 The layout of the SLC.

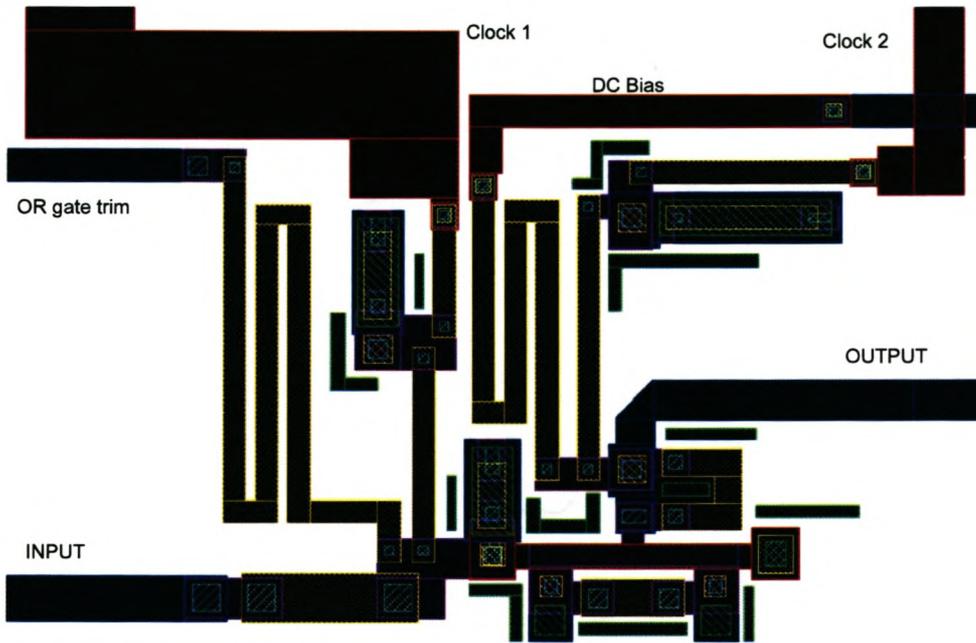


Fig. 7.4 The layout of the COSL OR gate

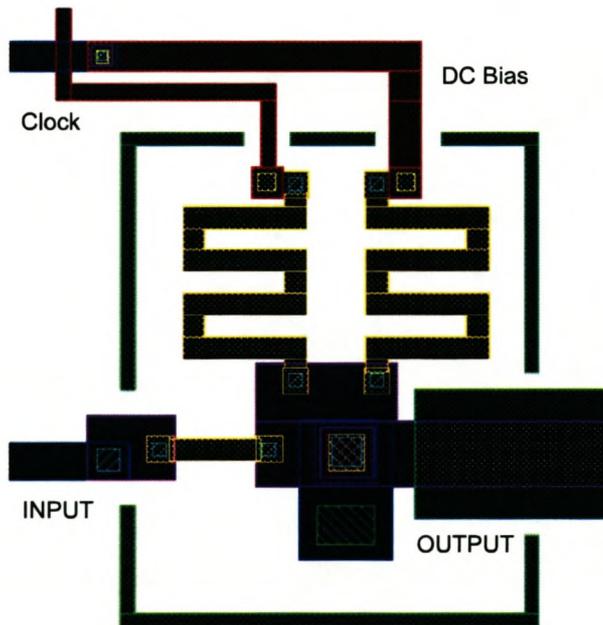


Fig. 7.5 The layout of the amplifier

■ Summary

This chapter described the layout of the 4-bit SLC sampler circuit with reference to the current design rules Hypres manufacturing process. It discussed the important issue of impedance matching the three phase clock.

This layout will provide the opportunity for high speed testing of the SLC and a 4-bit sampler circuit that can be incorporated into a full ADC.

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Conclusions

8.1 Reflections on Completed Work

- 8.1.1 Brief Summary of Dissertation
- 8.1.2 Achievements and Contributions to the Field of ADCs
- 8.1.3 SLADC Performance Prediction

8.2 Future Work and Recommendations

- 8.2.1 Improvement and Expansion of the Optimization Process
- 8.2.2 Investigation and Implementation of other Architectures
- 8.2.3 Extension of Resolution with Interleaving Techniques

8.1 Reflections

8.1.1 Brief summary of dissertation

This dissertation provided a detailed discussion on the development and evaluation of a switching logic Comparator (SLC) and a switching logic ADC (SLADC). Extensive WRSpipe simulations were done and results presented to illustrate the behaviour and performance of the SLC and SLADC.

Advantages and classification of ADCs, together with the current state of research in this field were provided. It was then followed by presentation of the detailed theoretical and conceptual foundations for the research performed in this field. Subjects included are the Josephson Junction (JJ), the One-Junction SQUID (OJS), the Quasi-One-Junction SQUID (QOJS), the Two-Junction SQUID (2JS), the COSL family of gates and finally Analog-to-Digital Converters (ADC).

The detailed design of a novel SLC is presented in Chapter 3. The philosophy behind the new design is given and how it is followed through to the actual design. A detailed account is then given of the design of the individual building blocks of the SLC. These building blocks include the Pulser, the Clock Shaper, the OJS, the 2JS read-out, the integration of all the components, the COSL OR-gate. This is followed by the implementation and simulation of the SLC in WRSpipe and a discussion on the results that were obtained.

Chapter 4 describes how the designed SLC is subjected to a Monte Carlo analysis to optimize

the design for maximum yield by incorporating tolerances representative of the manufacturing process and implementing the trimming facilities. Significant improvements in the yield were obtained from that of the original design.

This design was then successfully incorporated into the construction of a 4-bit SLADC. The output from the SLADC is in Gray code and a Gray-to-Binary Converter was designed with COSL gates to perform the conversion from Gray to Binary. These designs were all verified through WRSpice simulations. The SLADC was evaluated for the correct logic operation, maximum input bandwidth and linearity using a number of special input waveforms.

8.1.2 Achievements

- The initial goals:
- a) A comparator and ADC with a switching logic architecture in order to be COSL compatible.
 - b) Design of an ADC with the highest possible resolution and input bandwidth, with a minimum specification of 4 bits resolution and a minimum input bandwidth of 5 GHz.

These goals were achieved by the design of a comparator and an ADC that exhibits a voltage state switching logic. The minimum specification was met and exceeded by the design of a 4-bit SLADC with an 10 GHz input bandwidth. Results indicate that the initial ADC specification could be exceeded significantly in bandwidth or resolution.

The correct low frequency logic operation of both the SLC and SLADC was confirmed by linearly sweeping the input at a very specific rate to observe the correct sequential Gray and Binary codes corresponding to the analog input level.

Sinusoidal input frequencies of 1 GHz, 5 GHz and 10 GHz, equal to the Nyquist frequency, confirmed the correct high frequency operation of the SLC and SLADC.

The high input bandwidth of the SLC and SLADC was also confirmed by the beat frequency simulation performed on the SLADC. A 19 GHz sinusoidal input revealed the correct presentation of a 1 GHz beat frequency.

A dual sinusoidal frequency input was used to determine the linearity of the SLC and the SLADC. The Fourier spectrum of the input signal, reconstructed from the digital output of the SLADC revealed no intermodulation components that would have resulted if any non-linearities were present in the SLADC. The intermodulation components include 2nd order components f_1-f_2 and 3rd order $2f_1-f_2$ $2f_2-f_1$.

The response of the SLC and SLADC to a 1 GHz square wave input signal was also determined. The Fourier spectrum of the reconstructed input signal revealed the fundamental frequency and all the uneven harmonics that are inherent to a square wave waveform.

A Gray-to-Binary converter, an integral part of the SLADC, was designed and implemented successfully with COSL gates to convert the Gray code output from the quantizer section to binary for further processing of the data. Data is processed at a clock frequency of 20 GHz.

Further contributions include trimming facilities for the comparator design, which make it possible to trim a non-functional comparator circuit to a fully functional comparator. The comparator was designed and optimized utilizing a Monte Carlo Method, implemented in WRSpice. This optimization process includes the trimming facilities and with the specific fail/pass criteria described in Section 4.4 a yield of 89% was obtained. This constitutes an increase of 12% in the yield.

The design of the SLC is such that the aperture time is not determined by the width of the sampling pulse, but only by part of the rise time of the pulse. Alternatively it can be said that the SLC is edge triggered. This significantly reduce the aperture time from about 3 ps for the width of the pulse to a sub-picosecond value of approximately 0.6 ps for the applicable part of the rise time, as discussed in Section 3.3.9.

Due to the fact that the ratio of logic “0” to logic “1” can be set to 50/50 by adjusting the DC bias of the comparator the SLC comparator does not suffer from the dynamic distortions for high slew rates as experienced by Kaplan [19]. In their case they experienced the problem that the fraction during which the comparator output is “1”, is larger for positive slew rates and smaller for negative slew rates.

The comparator by Kaplan/Bradley is shown to be limited in the number of useful transitions when the input signal is increase beyond full scale, limiting the dynamic range of their ADC. For an input of five time the full scale, the LSB displayed approximately 80 useful transitions. The SLC comparator was subjected to an input of 6 times the full scale input showing 96 transitions which is sufficient dynamic range for more than 6 bits of resolution.

Due the method that was employed to sample the current in through the JJ of the OJS of the comparator, the SLC does not suffer from degradation of the physical logic signal waveform. An input ramp of 6 times full scale was applied to the 4-bit SLADC with no degradation in the binary output because the output logic pulses are generated by the 2JS and not by the actual OJS or QOJS.

8.1.3 SLADC performance prediction

The aperture time, given by (30), shows that there is always a trade off between the resolution (number of bits) and the input bandwidth for an ADC. The significant reduction in the aperture time translate into either an increase in the resolution or an increase in the input bandwidth, but not both.

Table 6.1 shows the predicted number of bits for the given input bandwidth, calculated using (30) and an aperture time of 0.6 ps.

Input Bandwidth [GHz]	Predicted number of bits
1	9.1
5	6.7
10	5.7
15	5.1
20	4.7

These predictions fall inside the Hypres projected performance band for flash ADCs, provided in the graph in Fig. 1.3 in the introduction Chapter and confirms the significant performance of the SLADC. The performance of the SLADC will thus be limited by the maximum clock rate that can be achieved by the COSL architecture.

The projected SFDR 21.7 dB of the SLADC, although determined through a crude process, also compares favourably.

8.2 Future Work and Recommendations

8.2.1 Improvement and Expansion of the Optimization Process

The WRSpice optimization process for the SLC requires further refinement to include a check to ensure a 50/50 ratio between the “0” and “1” logic levels for a linearly increasing input signal. This became apparent when it was necessary to adjust the DC bias by a small amount to re-establish a 50/50 ratio after the SLC was optimized in WRSpice.

A full optimization with thermal noise can be performed to investigate the full effect of noise on the SLC and SLADC.

8.2.3 Investigation and Implementation of other Architectures

In the presence of comparator threshold distortions there can be a marked decrease in ADC resolution. Loss in performance can be regained by architectural improvements such as redundant comparators and real-time digital error correction.

The SLC design made use of a OJS as the quantizer. In the design of the SLC the threshold distortions or “skewness” of the periodic current through the JJ of the OJS was minimized by using a JJ with a small critical current and a small inductor, effectively lowering the LI_0 product. It can be seen from the periodicity equation, $P = \Phi_0/L$ [A/cycle], that the smaller the inductor, the more input current is required and thus reducing the input sensitivity. There is, however, a maximum limit where the thresholds will begin to wash out.

Kaplan [19,20] utilized a balanced SQUID wheel to improve the high frequency performance of their single flux quantum QOJS comparator. The balanced SQUID wheel is shown in Fig. 6.1 and is used to reduce the threshold distortions at high signal slew rates while retaining high input sensitivity. The advantages of this circuit could be investigated and applied to the SLC to further enhance and improve the robustness and sensitivity of the SLC.

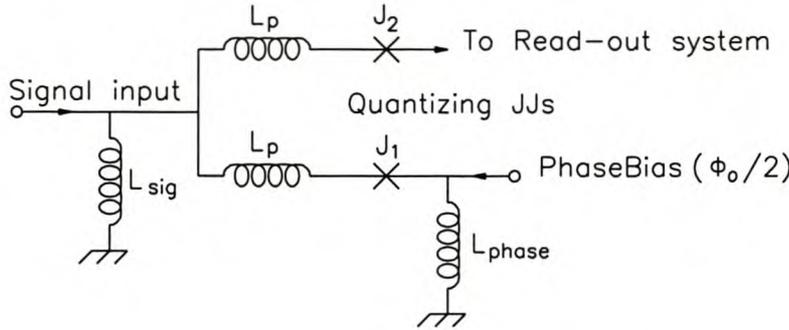


Fig. 6.1 The SQUID wheel to reduce threshold distortions at high slew rates

8.2.3 Extension of Resolution with Interleaving Techniques

Another architecture that could possibly be implemented to improve the performance of the SLC is threshold interleaving shown in Fig. 6.2. Kaplan [20] utilized the technique of interleaving thresholds to compensate for non-ideal comparator behaviour. By interleaving the thresholds of eight comparators, and combining the outputs with XOR gates, four LSB thresholds can be synthesized. The slew rate of each comparator will now only be 1/8th of the effective slew rate. Comparators for the MSBs receive the least of the input signal and exhibits the noisiest

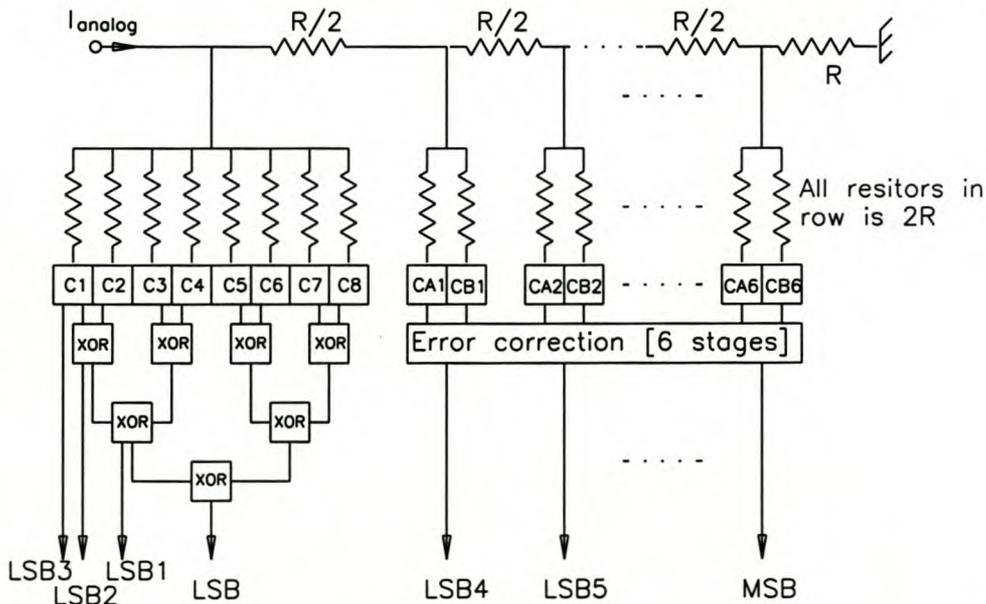


Fig. 6.2 Interleaving architecture for a 6 bit ADC, showing 8 interleaved comparators to synthesize 4 LSBs and redundant comparators to generate the 6 MSBs through real-time error correction.

thresholds. Kaplan [20] suggested the Baker code [21, 22] using two comparators and look-back logic [23, 24] to correct errors in real time for the MSBs.

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Appendix A

DERIVATION OF THE TRIM VOLTAGES FOR THE PULSER AND THE TWO JUNCTION SQUID

A.1 Trimming for the 2JS

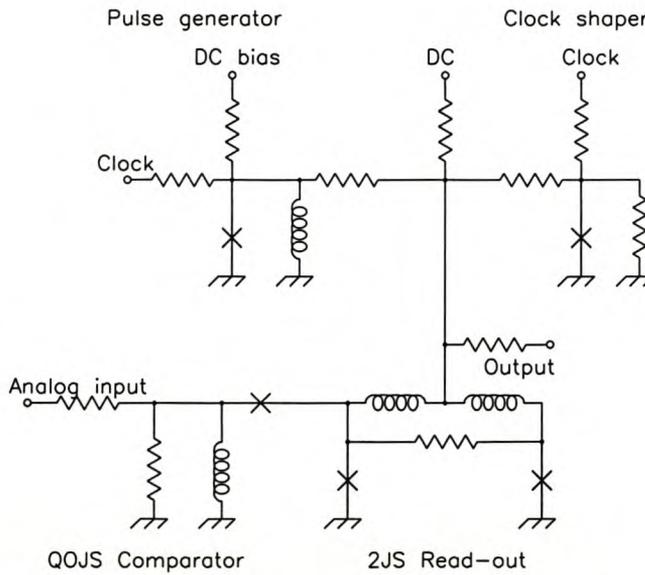


Fig. A.1 SL Comparator circuit.

Figure A.1 shows the circuit for the SLC. To implement the trim facility the following ratio of currents was considered:

$$\frac{I_{BIAS}(nom) + I_J(nom)}{I_{J1}(nom) + I_{J2}(nom)} \quad (43)$$

where $I_{BIAS}(nom)$ is the total bias current for the nominal component values, $I_J(nom)$ the nominal value of the critical current of the quantizing junction, $I_{J1}(nom)$ and $I_{J2}(nom)$ the nominal critical currents of the two junctions of the 2JS.

It is then the purpose of the additional trimming current to adjust the total bias current of a non-functional comparator to obtain a functional comparator circuit. To achieve this, the above ratio for the nominal circuit must be equal to that of a circuit with a Gaussian spread on its component values with the trim voltage implemented and we then obtain

$$\frac{I_{BIAS}(nom) + I_J(nom)}{I_{J1}(nom) + I_{J2}(nom)} = \frac{I_{BIAS}(trimmed) + I_J(spread)}{I_{J1}(spread) + I_{J2}(spread)} \quad (44)$$

where $I_{BIAS}(trimmed)$ is the total bias current, including the additional trimming current and can be expressed as

$$I_{BIAS}(trimmed) = I_{BIAS}(spread) + I_{trim} \quad (45)$$

where $I_{BIAS}(spread)$ is the total bias current of the circuit with spread on the components with out any trimming and I_{trim} the additional trimming current. The trimming voltage can be expressed as

$$V_{trim} = I_{trim} R_{BIAS}(spread) \quad (46)$$

Substituting equation 46 and 45 in equation 44 we obtain the following equation for the trim voltage.

$$r_{trim} = R_{BIAS}(spread) \left[\frac{(I_{BIAS}(nom) + I_J(nom))(I_{J1}(spread) + I_{J2}(spread))}{I_{J1}(nom) + I_{J2}(nom)} - (I_{BIAS}(spread) + I_J(spread)) \right] \quad (47)$$

In the WRSpice simulation, $I_{BIAS}(nom)$ en $I_{BIAS}(spread)$ are measured using the *.measure* statement by simulating the nominal circuit and the circuit with spreads on the component values and with no trimming applied.

A.2 Trimming for the Pulser

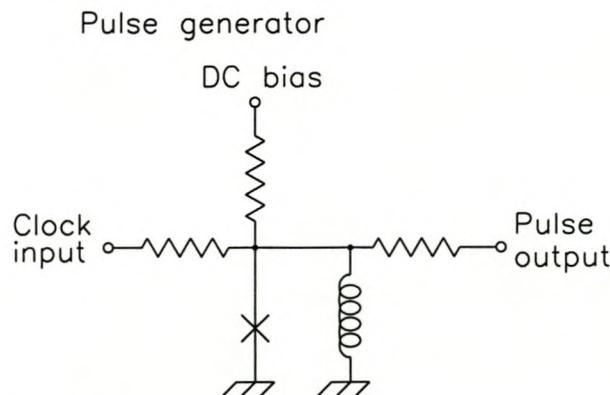


Fig. A.2 The pulser circuit.

The ratio considered for the trimming of the pulser, shown in Fig. A.2 is given by

$$\frac{I_{BIAS}(nom)}{I_{th}(nom)} = \frac{I_{BIAS}(trimmed)}{I_{th}(spread)} \quad (48)$$

Similar as for the comparator circuit, (46) and (45) for V_{trim} and $I_{BIAS}(trimmed)$ respectively, can be substituted into (48) to obtain the expression for V_{trim} for the pulser.

$$V_{trim}(pulser) = R_{trim}(spread) \left[\left(\frac{I_{th}(spread) I_{BIAS}(nom)}{I_{th}(nom)} \right) - I_{BIAS}(spread) \right] \quad (49)$$

The threshold current for an OJS with $\beta_L > 1$ for a transition from a zero to a one flux quantum was given by (9 and 10). Utilizing these equations and the nominal component values given in the Fig. A.2, $I_{th}(nom)$, β_L and $I_{BIAS}(nom)$ can be calculated as follows:

$$\begin{aligned} I_{th}(nom) &= 508.9 \times 10^{-6} \mu\text{A} \\ \beta_L &= 6.07 \\ I_{BIAS}(nom) &= 250 \mu\text{A} \end{aligned}$$

These values can be substituted into (49) to further simplify it to

$$V_{trim}(pulser) = R_{trim}(spread) [0.5 I_{th}(spread) - I_{BIAS}(spread)] \quad (50)$$

Appendix B

SOURCE CODE FOR WRSPICE SIMULATIONS OF THE SWITCHING LOGIC COMPARATOR

Simulation control file

```
#!/usr/local/WRspice/bin/wrspice
*Control for MC-analysis new_method/15%Jtol,15%Rtol,15%Ltol,10%LocalARL
*Includes Trimming for pulser
.control
reset
destroy all
*rusage all
*delete trace iplot
free all
seed 300
```

```
let NumberOfWafers=300
let NumberOfCycles=1
let NumberOfSimulations=NumberOfWafers*NumberOfCycles
let MatrixY=NumberOfSimulations-1
let MatrixX=16
let MatrixIndex=0
let CycleNumber=0
let WaferNumber=0
let NomPlot=0
let GaussPlot=0
let TrimmedPlot=0
let ChipsPassed=0
let ChipsFailed=0
let CircuitFail=0
```

```
let SimulationID=0
let FailMatrix[MatrixY][MatrixX]=0
```

```
let NoOfCompValues=5
let CompValueNo=0
let Yields[NoOfCompValues-1]=0
echo Yields= $&Yields
```

```
set Scale_factor_G=1.01
*Optimized from 1.0
```

```
*****QUASI ONE-JUNCTION AND READ-OUT
```

```
set Ij_nom_G = 0.1
*Optimized from 0
```

***** 2 Junction SQUID parameters

set lj1_nom_2jsqd_G = 1.5

*Optimized from 1.5

set lj2_nom_2jsqd_G = 0.5

*Optimized from 0.5

set L10_nom_G = 0.775p

*Optimized from 0.775p

set L9_nom_G = 0.258p

*Optimized from 0.258P

set Rbias_nom_G = 4.35

*Optimized from 4.31

set L11_nom_G = 0.4p

*Optimized from 0.35p

set R27_nom_G = 2.2

*Optimized from 2.3

set R16_nom_G = 0.85

*Optimized from 0.8

set R12_nom_G = 6.3

*Optimized from 6.4

set R32_nom_G = 2.5

*Optimized from 2

set R28_nom_G = 6

set R30_nom_G = 2

*Optimized from 2

*****PULSER

VAUES NOT CHANGED as it would affect the bias and new circuit needs to be calculated from scratch.

set L4_nom_G = 5p

*Optimized from 5p

set B6_nom_G = 0.4

*Optimized from 0.4

set R14_nom_G = 21.5

*Optimized from 21.5

set R15_nom_G = 20

*Optimized from 20

*****CLOCK SHAPER

VAUES NOT CHANGED as it would affect the bias and new circuit needs to be calculated from scratch.

set R11_nom_G = 5

*Optimized from 5

set R13_nom_G = 4

*Optimized from 4

set B5_nom_G = 0.6

*Optimized from 0.6

*****COMPOSE VALUES FOR OPTIMIZING THE CIRCUIT*****

```

*compose RbiasValues values 4.3 4.35 4.4 4.45
*compose lj_nom_G_Values values 0.08 0.09 0.1 0.11 0.12
*compose R27_nom_G_Values values 2.1 2.2 2.3 2.4 2.5
*compose lj1_2sq_G_Values values 1.4 1.45 1.5 1.55 1.6
*compose L11_nom_G_Values values 0.4p 0.425p 0.45p 0.475p 0.5p
*compose R16_nom_G_Values values 0.75 0.8 0.85 0.9 0.95
*compose R12_nom_G_Values values 6.275 6.3 6.325 6.4 6.425
*compose Scale_fac_Values values 1.005 1.02 1 1 1
*compose R32_nom_G_Values values 1 1.5 2 2.5 3
*compose R30_nom_G_Values values 1.5 1.75 2 2.25 2.5

****PULSER
*compose L4_nom_G_Values values 4.9p 4.95p 5p 5.05p 5.1p
compose B6_nom_G_Values values 0.39 0.395 0.4 0.415 0.42
*compose R14_nom_G_Values values 21.3 21.4 21.5 21.6 21.7
*compose R15_nom_G_Values values 19.8 19.9 20 20.1 20.2

****CLOCK SHAPER
*compose B5_nom_G_Values values 0.59 0.595 0.6 0.615 0.62
*compose R11_nom_G_Values values 5.8 5.9 5 5.1 5.2
*compose R13_nom_G_Values values 4.8 4.9 4 4.1 4.2

****Different q/p ratios
*compose lj1_n_2_G_Values values 1.43 1.47 1.5 1.53 1.56
*compose lj2_n_2_G_Values values 0.57 0.53 0.5 0.47 0.44
*compose L10_n_G_Values values 0.739p 0.758p 0.775p 0.791p 0.804p
*compose L9_n_G_Values values 0.295p 0.276p 0.258p 0.243p 0.23p

****Different lmax values for 2J SQD
*compose lj1_n_2_G_Values values 1.4625 1.5 1.5375 1.575 1.425
*compose lj2_n_2_G_Values values 0.4875 0.5 0.5125 0.525 0.4750
*compose L10_n_G_Values values 0.7954p 0.775p 0.7565p 0.7385p 0.8163p
*compose L9_n_G_Values values 0.2651p 0.2585p 0.2522p 0.2462p 0.2721p

echo -----
***** LOOP FOR DIFFERENT VALUES OF A COMPONENT

while CompValueNo <= (NoOfCompValues-1)

*reset
destroy all
*free all

seed 300

let FailMatrix[MatrixY][MatrixX]=0
*echo FailMatrix= $&FailMatrix
*pause

let MatrixIndex=0
let CycleNumber=0
let WaferNumber=0
let NomPlot=0
let GaussPlot=0
let TrimmedPlot=0
let ChipsPassed=0

```

```

let ChipsFailed=0
let CircuitFail=0

*set Rbias_nom_G = $RbiasValues[$CompValueNo]

*echo lj_nom_G_Values = $lj_nom_G_Values
*echo CompValueNo = $CompValueNo
*echo lj_nom_G_Values[$CompValueNo] = $lj_nom_G_Values[$CompValueNo]
*set lj_nom_G = $lj_nom_G_Values[$CompValueNo]
*let xxx = $lj_nom_G
*echo xxx= $xxx

*echo lj1_nom_2jsqd_G_Values = $lj1_2sq_G_Values
*echo CompValueNo = $CompValueNo
*echo lj1_2sq_G_Values[$CompValueNo] = $lj1_2sq_G_Values[$CompValueNo]
*set lj1_nom_2jsqd_G = $lj1_2jsqd_G_Values[$CompValueNo]
*let xxx = $lj1_nom_2jsqd_G
*echo xxx= $xxx

*echo R14_nom_G_Values = $R14_nom_G_Values
*echo CompValueNo = $CompValueNo
*echo R14_nom_G_Values[$CompValueNo] = $R14_nom_G_Values[$CompValueNo]
*set R14_nom_G = $R14_nom_G_Values[$CompValueNo]
*let xxx = $R14_nom_G
*echo xxx= $xxx

echo B6_nom_G_Values = $B6_nom_G_Values
echo CompValueNo = $CompValueNo
echo B6_nom_G_Values[$CompValueNo] = $B6_nom_G_Values[$CompValueNo]
set B6_nom_G = $B6_nom_G_Values[$CompValueNo]
let xxx = $B6_nom_G
echo xxx= $xxx

*set lj1_nom_2jsqd_G = $lj1_n_2_G_Values[$CompValueNo]
*let xxx = $lj1_nom_2jsqd_G
*echo xxx= $xxx
*set lj2_nom_2jsqd_G = $lj2_n_2_G_Values[$CompValueNo]
*let xxx = $lj2_nom_2jsqd_G
*echo xxx= $xxx
*set L10_nom_G = $L10_n_G_Values[$CompValueNo]
*let xxx = $L10_nom_G
*echo xxx= $xxx
*set L9_nom_G = $L9_n_G_Values[$CompValueNo]
*let xxx = $L9_nom_G
*echo xxx= $xxx

**** Call Circuit to measure the total Nominal Bias Current
echo
echo -----
echo
source /home/iapowell/SL_Monte/Optimising_simulations/Even_spreads/SLC_Advance_nominal.cir
*iplot v(360) v(370) v(9)
*iplot v(9)
run

NomPlot=1
set dumh=tran

```

```

set dumb = $&(NomPlot)
set dumc=.lp_nominal
set dumdd="$dumh$dumb$dumc"
let dumd = $dumdd
set lp_nominal_G = $&(dumd)
let a=$lp_nominal_G
echo lp_nominal_G=$&a

*
*           LOOP FOR THE NUMBER OF DIFFERENT WAFERS
while WaferNumber <= (NumberOfWafers-1)
**** SET UP GLOBAL SPREADS
    set Jtol_G = $&(gauss(0.15/3,1))
    set Rtol_G = $&(gauss(0.15/3,1))
    set Ltol_G = $&(gauss(0.15/3,1))
    let CycleNumber=0
*           LOOP FOR THE NUMBER OF LOCAL SIMULATIONS
    while CycleNumber <= (NumberOfCycles-1)

        let CircuitFail=0
        echo ResetCircuitFail= $&CircuitFail

        set WNo = $&WaferNumber
        set NameW = W
        set CNo = $&CycleNumber
        set NameC = C
        set SimID = $NameW$WNo$NameC$CNo
        let MatrixIndex=$SimID
        echo MatrixIndex= $&MatrixIndex

*
*           echo Hallo $&(CycleNumber)
*           echo C_CycleNumber = $&(CycleNumber)

        let Rbias_spread = $Rbias_nom_G*gauss(0.10/3,1)*$Rtol_G
        set Rbias_spread_G = $&(Rbias_spread)

        let lj_spread = $lj_nom_G*gauss(0.10/3,1)
        set lj_spread_G = $&(lj_spread)

        let lj1_spread_2jsqd = $lj1_nom_2jsqd_G*gauss(0.10/3,1)
        set lj1_spread_2jsqd_G = $&(lj1_spread_2jsqd)
        echo $&(lj1_spread_2jsqd)
        let lj2_spread_2jsqd = $lj2_nom_2jsqd_G*gauss(0.10/3,1)
        set lj2_spread_2jsqd_G = $&(lj2_spread_2jsqd)
        echo $&(lj2_spread_2jsqd)

*
*           SET UP LOCAL JUNCTION AREA SPREADS
        set Area_B05_G=$&(gauss(0.10/3,1))
        set Area_B06_G=$&(gauss(0.10/3,1))
        set Area_B11_G=$&(gauss(0.10/3,1))
        set Area_B14_G=$&(gauss(0.10/3,1))
        set Area_B15_G=$&(gauss(0.10/3,1))

*
*           SETUP LOCAL INDUCTOR SPREADS
        set Ind_L04_G=$&(gauss(0.10/3,1))
        set Ind_L09_G=$&(gauss(0.10/3,1))
        set Ind_L10_G=$&(gauss(0.10/3,1))
        set Ind_L11_G=$&(gauss(0.10/3,1))

*
*           SETUP LOCAL RESISTOR SPREADS
        set Res_R11_G=$&(gauss(0.10/3,1))

```

```

set Res_R12_G=$&(gauss(0.10/3,1))
set Res_R13_G=$&(gauss(0.10/3,1))
set Res_R14_G=$&(gauss(0.10/3,1))
set Res_R15_G=$&(gauss(0.10/3,1))
set Res_R16_G=$&(gauss(0.10/3,1))
set Res_R19_G=$&(gauss(0.10/3,1))
set Res_R27_G=$&(gauss(0.10/3,1))
set Res_R28_G=$&(gauss(0.10/3,1))
set Res_R30_G=$&(gauss(0.10/3,1))
set Res_R32_G=$&(gauss(0.10/3,1))

*
CALL CIRCUIT FOR SIMULATION OF SPREADS
source /home/iapowell/SL_Monte/Optimising_simulations/Even_spreads/SLC_Advance_spread.cir
*
iplot v(460) v(470) v(109)
*
iplot v(109)
run

GaussPlot=(2*CycleNumber)+2+(2*WaferNumber*NumberOfCycles)
*
echo $&(GaussPlot)
set dume = $&(GaussPlot)
set dumf = .lp_spread
set dumgg = "$dumh$dume$dumf"
*
echo $dumgg
let dumg = $dumgg
set lp_spread_G = $&(dumg)
*
echo $&(dumg)
let b=$lp_spread_G
echo C lp_spread_G= $&(b)

*
CALL CIRCUIT FOR SIMULATION OF TRIMS
source /home/iapowell/SL_Monte/Optimising_simulations/Even_spreads/SLC_Advance_trim.cir
*
iplot v(301) v(247) v(109)
*
iplot v(109)
run

TrimmedPlot=(2*CycleNumber)+3+(2*WaferNumber*NumberOfCycles)
*
echo $&(TrimmedPlot)
set dumk = $&(TrimmedPlot)
set duml = .lp_trimmedPulser
set dummm = "$dumh$dumk$duml"
*
echo $dummm
let dum = $dummm
set lp_trimmed_G = $&(dum)
*
echo $&(dum)
let bb=$lp_trimmed_G
echo C lp_trimmed_G=$&(bb)
echo

SimulationID=(WaferNumber*NumberOfCycles)+CycleNumber
echo SimulationID=$&SimulationID

echo

let FailMatrix[SimulationID][0]=$&(SimulationID+1)

```

```
*          CHECK EVERY PULSE OF SIMULATION FOR A FAIL OR PASS
if P0 > 1m
    let FailMatrix[SimulationID][1]=1
    let CircuitFail=1
end

if P1 > 1m
    let FailMatrix[SimulationID][2]=1
    let CircuitFail=1
end

if P2 > 1m
    let FailMatrix[SimulationID][3]=1
    let CircuitFail=1
end

if P3 > 1m
    let FailMatrix[SimulationID][4]=1
    let CircuitFail=1
end

if P4 > 1m
    let FailMatrix[SimulationID][5]=1
    let CircuitFail=1
end

if P5 > 1m
    let FailMatrix[SimulationID][6]=1
    let CircuitFail=1
end

if P6 > 1m
    let FailMatrix[SimulationID][7]=1
    let CircuitFail=1
end

if P7 > 1m
    let FailMatrix[SimulationID][8]=1
    let CircuitFail=1
end

if P8 > 1m
    let FailMatrix[SimulationID][9]=1
    let CircuitFail=1
end

if P9 > 1m
    let FailMatrix[SimulationID][10]=1
    let CircuitFail=1
end

if P10 > 1m
    let FailMatrix[SimulationID][11]=1
    let CircuitFail=1
end
```

```

    if P11 > 1m
        let FailMatrix[SimulationID][12]=1
        let CircuitFail=1
    end

    if P12 < 1m
        let FailMatrix[SimulationID][13]=1
        let CircuitFail=1
    end

    if P13 <1m
        let FailMatrix[SimulationID][14]=1
        let CircuitFail=1
    end

    if P14 < 1m
        let FailMatrix[SimulationID][15]=1
        let CircuitFail=1
    end

    if P15 > 1m
        let FailMatrix[SimulationID][16]=1
        let CircuitFail=1
    end

*echo FailMatrix= $&FailMatrix
*print /Of line FailMatrix
*echo $&FailMatrix[SimulationID][16]
*print FailMatrix[SimulationID][0,16]
*let SimResult=FailMatrix[SimulationID][0,16]
*echo $&SimResult
echo
    echo SimulationID=$&SimulationID

*
    COUNT CIRCUITS THAT FAILED AND PASSED

    if CircuitFail=1
        echo This circuit simulation failed
        ChipsFailed=ChipsFailed+1
    else
        echo This circuit simulation passed
        ChipsPassed=ChipsPassed+1
    end

echo
    echo Total chips failed = $&ChipsFailed
    echo Total chips passed = $&ChipsPassed
*
*
    echo C WaferNumber= $&(WaferNumber)
    echo C CycleNumber= $&(CycleNumber)
    CycleNumber=CycleNumber+1
echo -----
    end
* (end of while CycleNumber)

    WaferNumber=WaferNumber+1
    echo Yields= $&Yields
end
*(end of while WaferNumber)

```

```
Yield=ChipsPassed/(NumberOfWafers*NumberOfCycles)*100  
echo Yield = $&Yield
```

```
    if CompValueNo <= (NoOfCompValues-1)  
    let Yields[CompValueNo]=$&Yield  
    echo Yields= $&Yields  
    end
```

```
CompValueNo=CompValueNo+1  
end  
*(end of while CompValueNo)
```

```
*write SLCMatrix.raw FailMatrix  
echo
```

```
.endc
```

Nominal circuit simulation

SLC_Advance_nominal.cir COSL ADC comparator, nominal bias measurement

```

*
.exec
set noprintscale
set nopage
set width=256
set maxdata=120000
let Rbias_nom_L=$Rbias_nom_G
let lj_nom_L=$lj_nom_G
let lj1_nom_2jsqd_L = $lj1_nom_2jsqd_G
let lj2_nom_2jsqd_L = $lj2_nom_2jsqd_G

let L10_nom_L = $L10_nom_G
let L9_nom_L = $L9_nom_G
let L11_nom_L = $L11_nom_G
let R27_nom_L = $R27_nom_G
let R16_nom_L = $R16_nom_G
let R12_nom_L = $R12_nom_G
let R28_nom_L = $R28_nom_G
let R30_nom_L = $R30_nom_G
let R32_nom_L = $R32_nom_G

*PULSER AND CLOCK SHAPER
let L4_nom_L = $L4_nom_G
let R11_nom_L = $R11_nom_G
let R13_nom_L = $R13_nom_G
let R14_nom_L = $R14_nom_G
let R15_nom_L = $R15_nom_G
let B5_nom_L = $B5_nom_G
let B6_nom_L = $B6_nom_G

.endc
*
* ### BEGINNING OF CONTROL SPECIFICATION
*
*.control

*.endc
*
* ### BEGINNING OF TRANSIENT ANALYSIS
*
*.tran 0.1p 7n uic
.tran 0.1p 0.8n uic
.save v(360)
*

* ### BEGINNING OF CIRCUIT FILE FOR NORMAL COMPARATOR
*
* INPUT RAMP CURRENT
*I1 0 50 pwl(0 0 0.285n 0 3.485n 2.9516m 3.535n 2.9516m 6.735n 0 7n 0)
I1 0 50 pwl(0 0 0.537n 0 .636n 3.14m 0.686n 3.14m 0.786n 0 0.800n 0)
*
* CLOCK
V0 26 0 sin(0 10m 20Gig 0)
*

```

```
* DC BIAS VOLTAGE
V22 47 0 5m
*
* PULSER DC BIAS AND CLOCK
V14 39 0 sin(0 10m 20Gig 0)
V15 40 0 5m
*
*COMPARATOR CIRCUIT
B11 1 2 67 jj2 area=$((lj_nom_L)
B14 54 0 70 jj2 area=$((lj2_nom_2jsqd_L)
B15 55 0 71 jj2 area=$((lj1_nom_2jsqd_L)
B5 17 0 61 jj2 area=$((B5_nom_L)
B6 16 0 62 jj2 area=$((B6_nom_L)
L10 11 3 $&L10_nom_L
L11 1 0 $&L11_nom_L
L4 16 0 $&L4_nom_L
L9 4 11 $&L9_nom_L
R11 26 17 $&R11_nom_L
R12 41 17 $&R12_nom_L
R13 17 0 $&R13_nom_L
R14 39 16 $&R14_nom_L
R15 40 16 $&R15_nom_L
R16 16 42 $&R16_nom_L
R19 46 13 $&(Rbias_nom_L)
R27 11 8 $&R27_nom_L
R28 49 51 $&R28_nom_L
R30 1 0 $&R30_nom_L
R32 4 3 $&R32_nom_L
*
* V_SOURCES FOR CURRENT MONITORING
V16 41 13 0
V17 42 13 0
V20 47 46 0
V25 13 11 0
V26 50 49 0
V27 51 1 0
V28 8 7 0
V29 2 4 0
V32 3 54 0
V33 4 55 0

* ###BEGINNING OF NORMAL COSL OR GATE BUFFER
*
* 3 PHASE CLOCKS
V18 43 0 sin(0 10m 20Gig 16.67p)
V23 48 0 sin(0 10m 20Gig 0)
*
* DC FOR READ-OUT SQUID
V21 45 0 6m
*
* VOLTAGE SOURCE FOR CURRENT MONITORING
V19 45 44 0
V24 15 12 0
V30 5 52 0
V31 6 53 0
*
B7 14 0 63 jj2 area=0.36
B8 0 10 64 jj2 area=0.35
B9 12 9 65 jj2 area=0.34
```

```

B10 0 7 66 jj2 area=0.25
B12 52 0 68 jj2 area=0.2
B13 53 0 69 jj2 area=0.2
K1 L5 L8 0.58
K2 L6 L7 0.58
L5 72 0 5.15p
L6 7 72 5.15p
L7 6 9 2.2p
L8 9 5 2.2p
R17 43 14 10
R18 44 15 33
R20 15 14 12
R21 14 0 6
R22 0 10 2.3
R23 48 10 5
R24 12 9 5
R25 10 7 8.8
R26 9 0 5
R29 7 0 1.5
R31 6 5 1.6
*
* MEASURE TOTAL BIAS CURRENT
.measure tran lp_nominal from=150p to=280p max v(360)
H300 0 360 V25 1
R309 360 0 1
V301 370 0 @lp_nominal
R310 370 0 1

*
* JUNCTION MODEL FOR COSL OR GATE
.model jj2 jj(rtype=1, cct=1, icon=10m, vg=2.8m, delv=0.08m,
+ icrit=1m, r0=30, rn=1.64706, cap=1.54894p)
* Nb 2500 A/cm2 area = 40 square microns (generated by JJMODEL)

.end

```

Simulation of circuit with spreads on component values

SLC_Advance_spread.cir COSL ADC comparator, spread bias measurement

```

* ### INITIATE MONTE CARLO ANALYSIS*.monte
**.monte
.exec
set noprintscale
set nopage
set width=256
set maxdata=120000

**GET GLOBAL SPREADS
let Jtol_L = $Jtol_G
let Rtol_L = $Rtol_G
let Ltol_L = $Ltol_G
let Rbias_nom_L = $Rbias_nom_G
let Rbias_spread_L = $Rbias_spread_G
let lj_nom_L = $lj_nom_G
let lj_spread_L = $lj_spread_G
let lj1_spread_2jsqd_L = $lj1_spread_2jsqd_G
let lj2_spread_2jsqd_L = $lj2_spread_2jsqd_G

let L10_nom_L = $L10_nom_G

```

```
let L9_nom_L = $L9_nom_G
let L11_nom_L = $L11_nom_G
let R27_nom_L = $R27_nom_G
let R16_nom_L = $R16_nom_G
let R12_nom_L = $R12_nom_G
let R28_nom_L = $R28_nom_G
let R30_nom_L = $R30_nom_G
let R32_nom_L = $R32_nom_G
```

```
*PULSER AND CLOCK SHAPER
```

```
let L4_nom_L = $L4_nom_G
let R11_nom_L = $R11_nom_G
let R13_nom_L = $R13_nom_G
let R14_nom_L = $R14_nom_G
let R15_nom_L = $R15_nom_G
let B5_nom_L = $B5_nom_G
let B6_nom_L = $B6_nom_G
```

```
* GET LOCAL JUNCTION AREA SPREADS
```

```
let Area_B05_L=$Area_B05_G
let Area_B06_L=$Area_B06_G
let Area_B11_L=$Area_B11_G
let Area_B14_L=$Area_B14_G
let Area_B15_L=$Area_B15_G
```

```
* GET LOCAL INDUCTOR SPREADS
```

```
let Ind_L04_L=$Ind_L04_G
let Ind_L09_L=$Ind_L09_G
let Ind_L10_L=$Ind_L10_G
let Ind_L11_L=$Ind_L11_G
```

```
* SETUP LOCAL RESISTOR SPREADS
```

```
let Res_R11_L=$Res_R11_G
let Res_R12_L=$Res_R12_G
let Res_R13_L=$Res_R13_G
let Res_R14_L=$Res_R14_G
let Res_R15_L=$Res_R15_G
let Res_R16_L=$Res_R16_G
let Res_R19_L=$Res_R19_G
let Res_R27_L=$Res_R27_G
let Res_R28_L=$Res_R28_G
let Res_R30_L=$Res_R30_G
let Res_R32_L=$Res_R32_G
```

```
*echo $$(Jtol_L)
*echo $$(Rtol_L)
*echo $$(Ltol_L)
*echo $$(Area_B05_L)
*echo $$(Ind_L04_L)
*echo $$(Res_R11_L)
```

```
.endc
```

```
*
* ### BEGINNING OF CONTROL SPECIFICATION
*
```

```

*.control

*.endc
*
* ### BEGINNING OF TRANSIENT ANALYSIS
*
*.tran 0.1p 7n uic
.tran 0.1p 0.8n uic
.save v(460)
*

*****MONTE CIRCUIT*****
* ### BEGINNING OF CIRCUIT FILE FOR COMPARATOR WITH SPREADS
*
*
*SET UP LOCAL SPREADS
*.param Avar=gauss(0.1/3,1)
*.param Rvar=Rtol*gauss(0.1/3,1)
*.param Lvar=Ltol*gauss(0.1/3,1)
*.param Rtrim=Rbias_nom*Rvar
*.param lj_spread=lj_nom*Avar

* INPUT RAMP CURRENT
*1101 0 150 pwl(0 0 0.285n 0 3.485n 2.9516m 3.535n 2.9516m 6.735n 0 7n 0)
l101 0 150 pwl(0 0 0.537n 0 .636n 3.14m 0.686n 3.14m 0.786n 0 0.800n 0)

* CLOCK
V100 126 0 sin(0 10m 20Gig 0)
*
* DC BIAS VOLTAGE
V122 147 0 5m
*
* PULSER DC BIAS AND CLOCK
V114 139 0 sin(0 10m 20Gig 0)
V115 140 0 5m
*
*PULSER CIRCUIT
B106 116 0 162 jj2var area=$&(B6_nom_L*Area_B06_L)
L104 116 0 $&(L4_nom_L*Ind_L04_L*Ltol_L)
R114 139 116 $&(R14_nom_L*Res_R14_L*Rtol_L)
R116 116 142 $&(R16_nom_L*Res_R16_L*Rtol_L)
R115 140 116 $&(R15_nom_L*Res_R15_L*Rtol_L)

*COMPARATOR CIRCUIT
B111 101 102 167 jj2var area=$&(lj_spread_L)
B114 154 0 170 jj2var area=$&(lj2_spread_2jsqd_L)
B115 155 0 171 jj2var area=$&(lj1_spread_2jsqd_L)
B105 117 0 161 jj2var area=$&(B5_nom_L*Area_B05_L)

L110 111 103 $&(L10_nom_L*Ind_L10_L*Ltol_L)
L111 101 0 $&(L11_nom_L*Ind_L11_L*Ltol_L)

L109 104 111 $&(L9_nom_L*Ind_L09_L*Ltol_L)
R111 126 117 $&(R11_nom_L*Res_R11_L*Rtol_L)
R112 141 117 $&(R12_nom_L*Res_R12_L*Rtol_L)
R113 117 0 $&(R13_nom_L*Res_R13_L*Rtol_L)

```

```
R119 146 113 $$(Rbias_spread_L)
R127 111 108 $$(R27_nom_L*Res_R27_L*Rtol_L)
R128 149 151 $$(R28_nom_L*Res_R28_L*Rtol_L)
R130 101 0 $$(R30_nom_L*Res_R30_L*Rtol_L)
R132 104 103 $$(R32_nom_L*Res_R32_L*Rtol_L)
*
* V_SOURCES FOR CURRENT MONITORING
V116 141 113 0
V117 142 113 0
V120 147 146 0
V125 113 111 0
V126 150 149 0
V127 151 101 0
V128 108 107 0
V129 102 104 0
V132 103 154 0
V133 104 155 0

#####BEGINNING OF COSL OR GATE BUFFER
*
* 3 PHASE CLOCKS
V118 143 0 sin(0 10m 20Gig 16.67p)
V123 148 0 sin(0 10m 20Gig 0)
*
* DC FOR READ-OUT SQUID
V121 145 0 6m
*
* VOLTAGE SOURCE FOR CURRENT MONITORING
V119 145 144 0
V124 115 112 0
V130 105 152 0
V131 106 153 0
*

B107 114 0 163 jj2 area=0.36
B108 0 110 164 jj2 area=0.35
B109 112 109 165 jj2 area=0.34
B110 0 107 166 jj2 area=0.25
B112 152 0 168 jj2 area=0.2
B113 153 0 169 jj2 area=0.2
K101 L105 L108 0.58
K102 L106 L107 0.58
L105 172 0 5.15p
L106 107 172 5.15p
L107 106 109 2.2p
L108 109 105 2.2p
R117 143 114 10
R118 144 115 33
R120 115 114 12
R121 114 0 6
R122 0 110 2.3
R123 148 110 5
R124 112 109 5
R125 110 107 8.8
R126 109 0 5
R129 107 0 1.5
R131 106 105 1.6
*
```

```
* JUNCTION MODEL FOR COSL OR GATE
.model jj2 jj(rtype=1, cct=1, icon=10m, vg=2.8m, delv=0.08m,
+ icrit=1m, r0=30, rn=1.64706, cap=1.54894p)
* Nb 2500 A/cm2 area = 40 square microns (generated by JJMODEL)
*
*
* MEASURE TOTAL BIAS CURRENT
.measure tran lp_spread from=150p to=280p max v(460)
H400 0 460 V125 1
R409 460 0 1
V470 470 0 @lp_spread
R470 470 0 1
*
* JUNCTION MODEL WITH GLOBAL SPREAD
.model jj2var jj(rtype=1, cct=1, icon=10m, vg=2.8m, delv=0.08m,
+ icrit=$&(Jtol_L*1m), r0=30, rn=1.64706, cap=1.54894p)
* Nb 2500 A/cm2 area = 40 square microns (generated by JJMODEL)
*
.end
```

Simulation of circuit implementing the trim facilities

SLC_Advance_trim.cir COSL ADC comparator with Pulser trim voltage

```
*
* ### INITIATE MONTE CARLO ANALYSIS*.monte
```

```
** .monte
. exec
*set noprintscale
*set nopage
*set width=256
*set maxdata=1000000
```

```
**GET GLOBAL SPREADS
```

```
let Jtol_L=$Jtol_G
let Rtol_L=$Rtol_G
let Ltol_L=$Ltol_G
let Rbias_nom_L=$Rbias_nom_G
let Rbias_spread_L=$Rbias_spread_G
let lj_nom_L=$lj_nom_G
let lj_spread_L=$lj_spread_G
let lp_nominal_L=$lp_nominal_G
let lp_spread_L=$lp_spread_G
let lj1_nom_2jsqd_L=$lj1_nom_2jsqd_G
let lj2_nom_2jsqd_L=$lj2_nom_2jsqd_G
let lj1_spread_2jsqd_L=$lj1_spread_2jsqd_G
let lj2_spread_2jsqd_L=$lj2_spread_2jsqd_G
```

```
let L10_nom_L=$L10_nom_G
let L9_nom_L=$L9_nom_G
let L11_nom_L=$L11_nom_G
let R27_nom_L=$R27_nom_G
let R16_nom_L=$R16_nom_G
let R12_nom_L=$R12_nom_G
let R28_nom_L=$R28_nom_G
let R30_nom_L=$R30_nom_G
let R32_nom_L=$R32_nom_G
```

```
*PULSER AND CLOCK SHAPER
```

```
let L4_nom_L=$L4_nom_G
let R11_nom_L=$R11_nom_G
let R13_nom_L=$R13_nom_G
let R14_nom_L=$R14_nom_G
let R15_nom_L=$R15_nom_G
let B5_nom_L=$B5_nom_G
let B6_nom_L=$B6_nom_G
```

```
let Scale_factor_L=$Scale_factor_G
```

```
*echo TP Jtol_L=$&(amp;Jtol_L)
*echo TP Rtol_L=$&(amp;Rtol_L)
*echo TP Ltol_L=$&(amp;Ltol_L)
*echo TP Rbias_nom_L=$&(amp;Rbias_nom_L)
*echo TP Rbias_spread_L=$&(amp;Rbias_spread_L)
*echo TP lj_nom_L=$&(amp;lj_nom_L)
*echo TP lj_spread_L=$&(amp;lj_spread_L)
*echo TP lp_nominal_L=$&(amp;lp_nominal_L)
*echo TP lp_spread_L=$&(amp;lp_spread_L)
*echo TP Scale_factor_L=$&(amp;Scale_factor_L)
```

```

*      GET LOCAL JUNCTION AREA SPREADS
let Area_B05_L=$Area_B05_G
let Area_B06_L=$Area_B06_G
let Area_B11_L=$Area_B11_G
let Area_B14_L=$Area_B14_G
let Area_B15_L=$Area_B15_G

*      GET LOCAL INDUCTOR SPREADS
let Ind_L04_L=$Ind_L04_G
let Ind_L09_L=$Ind_L09_G
let Ind_L10_L=$Ind_L10_G
let Ind_L11_L=$Ind_L11_G

*      SETUP LOCAL RESISTOR SPREADS
let Res_R11_L=$Res_R11_G
let Res_R12_L=$Res_R12_G
let Res_R13_L=$Res_R13_G
let Res_R14_L=$Res_R14_G
let Res_R15_L=$Res_R15_G
let Res_R16_L=$Res_R16_G
let Res_R19_L=$Res_R19_G
let Res_R27_L=$Res_R27_G
let Res_R28_L=$Res_R28_G
let Res_R30_L=$Res_R30_G
let Res_R32_L=$Res_R32_G

    let Xfactor=1
    let Vdc=5m
    let Rp_bias_nom=$R15_nom_L
    let Ind_L4_nom=5p
    let Phi0=2.067834861f
    let lcp_nom=0.4m
    let B_nom=(2*pi*Ind_L4_nom*lcp_nom)/Phi0
*echo B_nom = $&(B_nom)
    let Arg=-1/B_nom
*echo Arg = $&(Arg)
    let Arcos_nom = -j(ln(Arg+j(sqrt(1-Arg^2))))
*echo Arcos_nom = $&(Arcos_nom)
    let lthp_nom= (lcp_nom*sin(Arcos_nom)+lcp_nom/B_nom*Arcos_nom)
*echo lthp_nom = $&(lthp_nom)
    let lp_bias_nom=Vdc/Rp_bias_nom
*echo lp_bias_nom = $&(lp_bias_nom)
    let Rp_bias_spread = $&(Rp_bias_nom*Res_R15_L*Rtol_L)
    let Ratio=lp_bias_nom/lthp_nom
*echo Ratio = $&(Ratio)

    let lcp_spread=lcp_nom*Area_B06_L*Jtol_L
    let Ind_L4_spread=Ind_L4_nom * Ind_L04_L*Ltol_L
    let B_spread=(2 * pi * Ind_L4_spread * lcp_spread) / Phi0
*echo B_spread = $&(B_spread)
    let Arg_spread=-1/B_spread
*echo Arg_spread = $&(Arg_spread)
    let Arcos_spread = -j(ln(Arg_spread+j(sqrt(1-Arg_spread^2))))
*echo Arcos_spread = $&(Arcos_spread)
    let lthp_spread= (lcp_spread*sin(Arcos_spread)+lcp_spread/B_spread*Arcos_spread)
*echo lthp_spread = $&(lthp_spread)
    let Vp_trim = Xfactor*(Rp_bias_spread*((lthp_spread*Ratio)-lp_bias_nom))
*echo Vp_trim = $&(Vp_trim)

```

```

echo
*echo $$(Jtol_L)
*echo $$(Rtol_L)
*echo $$(Ltol_L)
*echo $$(Area_B05_L)
*echo $$(Ind_L04_L)
*echo $$(Res_R11_L)

.endc
*
* ### BEGINNING OF CONTROL SPECIFICATION
*
*.control

*.endc
*
* ### BEGINNING OF TRANSIENT ANALYSIS
*
*.tran 0.1p 7n uic
.tran 0.1p 0.8n uic
.save v(460) v(109)
*
*****MONTE CIRCUIT*****
* ### BEGINNING OF CIRCUIT FILE FOR COMPARATOR WITH SPREADS
*
*
* INPUT RAMP CURRENT
*I101 0 150 pwl(0 0 0.285n 0 3.485n 2.9516m 3.535n 2.9516m 6.735n 0 7n 0)
I101 0 150 pwl(0 0 0.537n 0 .636n 3.14m 0.686n 3.14m 0.786n 0 0.800n 0)

* CLOCK
V100 126 0 sin(0 10m 20Gig 0)
*

* DC BIAS AND TRIM VOLTAGES
V122 147 0 5m
R301 301 0 1
V      3      0      1      3      0      1      0
$$(Rbias_spread_L)*(((($$(Ip_nominal_L)+$$(Ij_nom_L)*0.001)*$$(Ij1_spread_2jsqd_L)*$$(Jtol_L)*0.001+$$(Ij
2_spread_2jsqd_L)*$$(Jtol_L)*0.001)*$$(Scale_factor_L)/($$(Ij1_nom_2jsqd_L)*0.001+$$(Ij2_nom_2jsqd_L)*0.
001))-($$(Ip_spread_L)+$$(Ij_spread_L)*$$(Jtol_L)*0.001))
V222 247 147 v(301)

* MEASURE TOTAL BIAS CURRENT
.measure tran Ip_trimmedPulser from=150p to=280p max v(460)
H400 0 460 V125 1
R409 460 0 1
V470 470 0 @Ip_trimmedPulser
R470 470 0 1

*MEASURE PULSES FOR FAIL OR PASS

.measure tran P0 from=25p to=50p max v(109)
.measure tran P1 from=75p to=100p max v(109)
.measure tran P2 from=125p to=150p max v(109)
.measure tran P3 from=175p to=200p max v(109)
.measure tran P4 from=225p to=250p max v(109)
.measure tran P5 from=275p to=300p max v(109)
.measure tran P6 from=325p to=350p max v(109)
.measure tran P7 from=375p to=400p max v(109)
.measure tran P8 from=425p to=450p max v(109)
.measure tran P9 from=475p to=500p max v(109)

```

```

.measure tran P10 from=525p to=550p max v(109)
.measure tran P11 from=575p to=600p max v(109)
.measure tran P12 from=625p to=650p max v(109)
.measure tran P13 from=675p to=700p max v(109)
.measure tran P14 from=725p to=750p max v(109)
.measure tran P15 from=775p to=800p max v(109)

* PULSER DC BIAS, TRIM AND CLOCK
V114 139 0 sin(0 10m 20Gig 0)
V115 140 0 5m
V216 241 140 $(Vp_trim)

*PULSER CIRCUIT WITH TRIM
B106 116 0 162 jj2var area=$(B6_nom_L*Area_B06_L)
L104 116 0 $(L4_nom_L*Ind_L04_L*Ltol_L)
R114 139 116 $(R14_nom_L*Res_R14_L*Rtol_L)
R115 241 116 $(Rp_bias_spread)
R116 116 142 $(R16_nom_L*Res_R16_L*Rtol_L)

*
*COMPARATOR CIRCUIT
B111 101 102 167 jj2var area=$(Ij_spread_L)
B114 154 0 170 jj2var area=$(Ij2_spread_2jsqd_L)
B115 155 0 171 jj2var area=$(Ij1_spread_2jsqd_L)
B105 117 0 161 jj2var area=$(B5_nom_L*Area_B05_L)

L110 111 103 $(L10_nom_L*Ind_L10_L*Ltol_L)
L111 101 0 $(L11_nom_L*Ind_L11_L*Ltol_L)

L109 104 111 $(L9_nom_L*Ind_L09_L*Ltol_L)
R111 126 117 $(R11_nom_L*Res_R11_L*Rtol_L)
R112 141 117 $(R12_nom_L*Res_R12_L*Rtol_L)
R113 117 0 $(R13_nom_L*Res_R13_L*Rtol_L)

R119 146 113 $(Rbias_spread_L)
R127 111 108 $(R27_nom_L*Res_R27_L*Rtol_L)
R128 149 151 $(R28_nom_L*Res_R28_L*Rtol_L)
R130 101 0 $(R30_nom_L*Res_R30_L*Rtol_L)
R132 104 103 $(R32_nom_L*Res_R32_L*Rtol_L)
*
* V_SOURCES FOR CURRENT MONITORING
V116 141 113 0
V117 142 113 0
V120 247 146 0
V125 113 111 0
V126 150 149 0
V127 151 101 0
V128 108 107 0
V129 102 104 0
V132 103 154 0
V133 104 155 0
*
*#####BEGINNING OF COSL OR GATE BUFFER
*
* 3 PHASE CLOCKS
V118 143 0 sin(0 10m 20Gig 16.67p)
V123 148 0 sin(0 10m 20Gig 0)
*
* DC FOR READ-OUT SQUID
V121 145 0 6m
*

```

```
* VOLTAGE SOURCE FOR CURRENT MONITORING
V119 145 144 0
V124 115 112 0
V130 105 152 0
V131 106 153 0
*
B107 114 0 163 jj2 area=0.36
B108 0 110 164 jj2 area=0.35
B109 112 109 165 jj2 area=0.34
B110 0 107 166 jj2 area=0.25
B112 152 0 168 jj2 area=0.2
B113 153 0 169 jj2 area=0.2
K101 L105 L108 0.58
K102 L106 L107 0.58
L105 172 0 5.15p
L106 107 172 5.15p
L107 106 109 2.2p
L108 109 105 2.2p
R117 143 114 10
R118 144 115 33
R120 115 114 12
R121 114 0 6
R122 0 110 2.3
R123 148 110 5
R124 112 109 5
R125 110 107 8.8
R126 109 0 5
R129 107 0 1.5
R131 106 105 1.6
*
* JUNCTION MODEL FOR COSL OR GATE
.model jj2 jj(rtype=1, cct=1, icon=10m, vg=2.8m, delv=0.08m,
+ icrit=1m, r0=30, rn=1.64706, cap=1.54894p)
* Nb 2500 A/cm2 area = 40 square microns (generated by JJMODEL)
*
* JUNCTION MODEL WITH GLOBAL SPREAD
.model jj2var jj(rtype=1, cct=1, icon=10m, vg=2.8m, delv=0.08m,
+ icrit=$((Jtol_L*1m), r0=30, rn=1.64706, cap=1.54894p)
* Nb 2500 A/cm2 area = 40 square microns (generated by JJMODEL)
*
.end
```