Field Implementation of a Transient Voltage Measurement Facility Using HV Current Transformers

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Declaration

I, the undersigned, hereby declare that the work contained in this thesis is my own original work and that I have not previously in its entirety or in part submitted it at any university for a degree.

F.B. Siebrits Date

Abstract

The bandwidth of standard HV measurement devices such as capacitive voltage transformers is too limited in order to measure wideband phenomena. This thesis is concerned with the investigation into a non- intrusive HV transient voltage measurement facility using standard substation HV current transformers (CT's) configured in a transconductance topology. The sensing, summation and integration of the CT capacitive earth currents are investigated. This thesis also reports on the development of a optically isolated link using optical fibre for signal transfer and a computer based data acquisition system.

Opsomming

Standaard hoogspannings (HS) meettoerusting soos kapasitiewe spannings transformators het beperkte bandwydte vir die meet van wyeband verskynsels. Hierdie tesis handel oor die implementering van 'n HS meetstelsel wat op nie-inbrekende wyse oorgangsverskynsels meet deur middel van HS stroomtransformators wat in 'n transkonduktansie topologie gekonfigureer is. Die meet, sommasie en integrasie van kapasitoewe grondstrome word ondersoek. Hierdie tesis doen ook verslag aangaande die ontwikkeling van 'n optiese geïsoleerde koppelvlak wat gebruik word vir seinoordrag en 'n rekenaar gebasseerde data versamelaar.

This thesis is dedicated to my wife.

Acknowledgements

I would like to thank the following individuals and institutions for their contributions and support.

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- My wife Hilda for her inspiration and understanding.

Contents

Glossary of Abbreviations

HV	High Voltage
CT	Current Transformer
VT	Voltage Transformer
QOS	Quality of Supply
CVT	Capacitive Voltage Transformer
DC	Direct Current
AC	Alternating Current
PWM	Pulse Width Modulation
ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
MSPS	Million Samples per Second
EPLD	Erasable Programmable Logic Device
MSB	Most Significant Bit
LSB	Least Significant Bit
DUT	Device Under Test
MOSFET	Metal Oxide Field Effect Transistor
RMS	Root Mean Square
GPS	Global Positioning System
1PPS	One Pulse per Second
TCP/IP	Transmission Control Protocol/Internet Protocol
VI	Virtual Instrument
VHDL	Very High Speed Integrated Circuit (VHSIC) Hardware Description Language
PCI	Peripheral Component Interconnect

Chapter 1

Project Motivation and Description

1.1 Introduction

The wideband measurement of high frequency (HF) phenomena is becoming increasingly valuable with respect to the impact thereof on high voltage (HV) equipment condition monitoring and quality of supply. The maintenance of HV equipment such as current transformers (CT's), voltage transformers (VT's) and insulators is extremely expensive and time consuming. Failure of HV equipment is expensive to large-scale industries such as mining as unnecessary outages results in losses of millions of rands due to lost production and start-up costs. Eskom is furthermore increasingly engaging in Quality of Supply (QOS) agreements with customers in which Eskom pledges to conform to certain QOS criteria and in failing Eskom is liable for compensation.

The high-frequency noise generated from failing apparatus and veld fires as well as switching impulses and lightening adversely affects system performance. Long-term exposure of HV equipment to these conditions dramatically decreases the lifespan of HV equipment and may result in failure and injury.

The monitoring of the system for abnormal HF signals enables the early detection of faulty equipment and raging veld fires and assists in the observation of high frequency phenomena such as switching activities and lightning [50]. Standard wideband HV measurement devices such as capacitive dividers are bulky and require de-energising of the line for installation and de-installation [51]. This is undesirable for routine wideband measurements.

The need arise for a non-intrusive method of measuring wideband phenomena, using standard substation equipment for medium to long term periods of time.

1.2 Project Description

Standard HV measurement equipment such as CVTs lack the required bandwidth in order to measure wideband phenomena [9, 10]. The bandwidth of these devices is limited to the fundamental frequency and related harmonics. The high frequency noise generated from faulty equipment, switching activities and slower lightening impulses resides in the frequency range of 100 Hz to 100 kHz [11].

This project investigates the field implementation of a HV transient monitoring facility using a standard substation CT configured in a non-standard topology. The capacitance, which exists between the primary conductor and earthed base of the substation CT, is exploited in order to measure HF components up to 500 kHz.

The measurement location within a substation is usually far removed from the location of the instrumentation. The transfer of measured signals in HV environments using conventional copper wire results in signal corruption and poses safety hazards. This project therefore investigates the establishment of an optically isolated link using optic fibre for the transmission of measured signals. The use of optic fibre results in increased signal to noise ratios and bandwidth. Optical isolation eradicates the hazards of floating ground potentials and guarantee the safety of operating personnel.

The recording of transient waveforms is essential and therefore the implementation of a computer based data acquisition system for transient detection and recording is investigated. The data acquisition system is required to operate unattended for long periods of time and to supply each transient condition with ample identification and time stamping information.

This project is therefore concerned with the field implementation of a HV transient monitoring facility using standard substation CTs configured in non-standard topology. The project further investigates the implementation of an optically isolated measurement link using optic fibre together with a supporting data acquisition system.

1.3 Structure of this Thesis

Chapter 2 presents background on existing wideband measurement topologies and investigates the advantages and disadvantages thereof. The non-standard configuration of the substation CT is investigated and a HV transient monitoring system is presented.

Chapter 3 presents the hardware design of the supporting circuitry for the measurement configuration discussed in chapter 2.

Chapter 4 is concerned with the design of the digital optically isolated link. The optically isolated link consists of a transmitter and receiver unit connected via optical fibre. The design details of the analog and digital components are given and discussed.

Chapter 5 deals with the design of the computer based data acquisition system, which comprises an analog trigger circuit interfaced to a computer based data acquisition card. The entire data acquisition system is user configurable via a software user control interface.

Chapter 6 presents the laboratory evaluation of the transient monitoring system. The system is evaluated using computer-based simulations based on a frequency domain model of the measurement circuitry. The simulations are also verified with practical measurements.

Chapter 7 presents the field evaluation during which the transient monitoring system is tested for actual field conditions. The measured waveforms and the interpretations thereof are given and discussed.

Chapter 8 closes with an overview of the monitoring system and gives recommendations for future developments.

Chapter 2

Literature Survey and Proposed System Topology

2.1 Overview of HV Measurement Topologies

The measurement of transient waveforms on HV transmission lines is compromised by the limited bandwidth of standard substation measurement devices. Traditional voltage measurement devices such as capacitive voltage transformers (CVT) lack the required bandwidth in order to measure transient phenomena [9, 10]. Research indicates that the bandwidth of a standard CVT with the damping sub-circuit disconnected and a resistive burden of rated value connected is in the range of up to 600 Hz [1, 2]. These devices can be used for the measurement of fundamental frequency and related harmonics with relative success and measurements of up to the thirteenth harmonic can be conducted [3].

High voltage transient waveforms are however measured using specially designed wideband transducer devices such as resistive and capacitive voltage dividers [5]. Figure 2-1 shows the transient measurement arrangement using a voltage divider [45]. The wideband voltage divider comprises impedances Z_1 and Z_2. The transducer relation shown in Figure 2-1 represents the transducer output voltage V_o as result of the HV input V_i for sinusoidal steady state conditions. The voltage divider shown in Figure 2-1 is implemented by using either resistors and/or capacitors for Z_1 and Z_2.

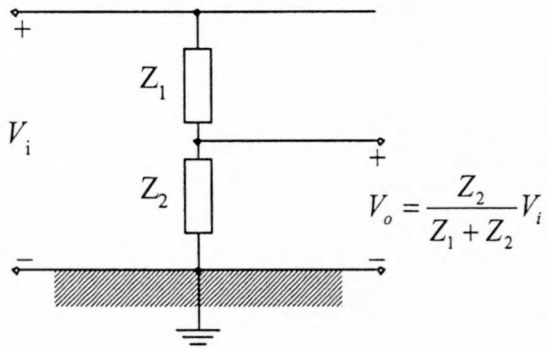

Figure 2-1 Accurate transient voltage measurement using a voltage divider.

The use of resistors constitutes a simple construction, which is lightweight and portable [45]. The presence however of stray elements limits the bandwidth of these devices and causes incorrect measurements at higher frequencies. Historical research indicates complex equivalent circuits as result of these stray capacitances and inductances for which compensation is not trivial [4].

The substitution of Z_1 and Z_2 with capacitors results in a more complicated construction. The capacitive voltage divider is shown in Figure 2-2.

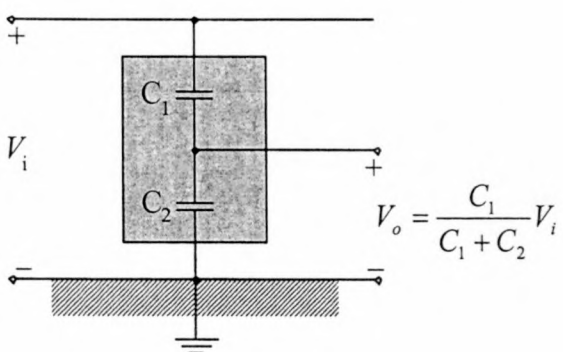

Figure 2-2 Diagram of a capacitive voltage divider.

The value of C_1 is substantially smaller than that of C_2 in order to obtain the desired attenuation factor. The voltage rating of C_1 results in large capacitor size and special construction methods are required in order to maintain portability for this device [45].

The use of the voltage dividers is advantageous towards accurately measuring transient voltages. These dividers are however expensive and in most cases troublesome to transport and install [6]. A further disadvantage of these devices is that installation and de-installation requires de-energising [7].

The objective of the research conducted in this thesis is aimed at establishing a non-intrusive transient voltage measurement facility. The employment of standard substation equipment such as CTs is investigated for use in non-standard configuration in order to measure wideband transient phenomena.

2.2 Wideband Measurements using HV Current Transformers

This section investigates the use of HV substation current transformers (CTs) for wideband voltage measurements. The HV CT is configured for wideband measurements by making use of the reflected impedance between the HV terminals and the earth-side enclosure of the substation CT [11] as shown in Figure 2-3.

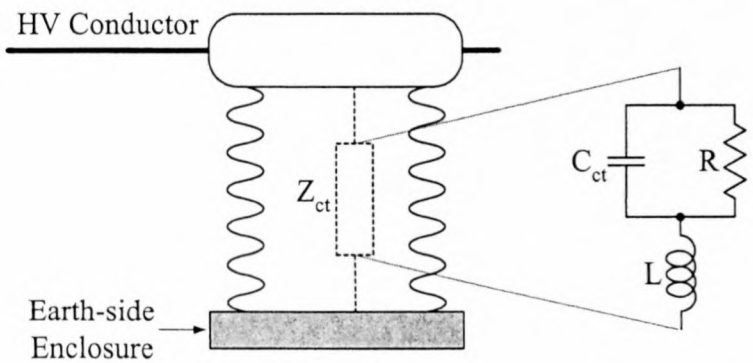

Figure 2-3 Diagram of the reflected impedance between the HV terminals and the earth side enclosure of the HV CT.

The impedance Z_p is modelled as the parallel combination of the capacitor C_{ct} and resistor R in series with the inductance L. The values of these elements are shown in Table 2-1 for a typical substation CT [11].

Table 2-1 Typical values for the modelled CT impedance.

Parameter	Value
R	2.573 MΩ
C_{ct}	1.081 nF
L	2.129 μH

Research indicates that this impedance is predominantly capacitive for frequencies in the order of 100 kHz [11], which includes transients as result of filtered lightening, switching activities and fault conditions. The use of the substation CT configured in a voltage measurement topology is capable of achieving bandwidths of up to 500 kHz

[13]. The value of the capacitance C_{ct} as shown in Table 2-1 is relatively stable throughout the frequency range 100 Hz to 100 kHz [11, 12]. The capacitive value of Z_{ct} increases in the frequency range from 100 kHz to 500 kHz as result of the CT self-resonance in the vicinity of 3 MHz [12].

2.2.1 Configuration Topologies

The CT is configurable in two possible topologies for voltage measurement namely a capacitive divider topology or a transconductance topology [11]. Both these configurations are based on the capacitance that exists between the HV terminals and the earth-side enclosure of the CT.

A diagram of the CT configured in a capacitive divider topology is shown in Figure 2-4.

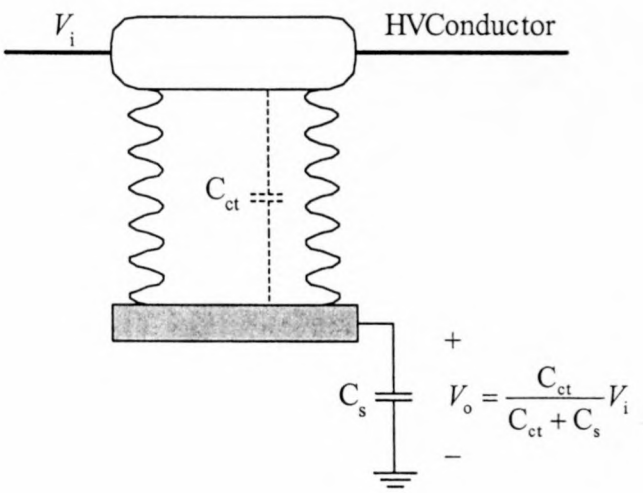

Figure 2-4 HV CT configured in a capacitive divider topology.

The primary voltage is given by $v_i(t)$ and the CT capacitance by C_{ct}. The earth side enclosure of the CT is earthed through a sensing capacitor C_s. The output voltage across C_s is given by $v_o(t)$ of which the value is as indicated in Figure 2-4. The diagram of Figure 2-4 resembles the capacitive divider used to measure wideband transients, which is shown in Figure 2-2. The earth-side enclosure of the CT is earthed through the sensing capacitor C_s, which disturbs the secure earthing arrangement of the CT. This method is therefore unsuitable for the desired non-intrusive approach. The advantage however of configuring the CT in a capacitive

divider topology is the accuracy with which transient waveforms are measured, as it resembles the configuration shown in Figure 2-2 [11].

The diagram of the CT configured in a transconductance topology is shown in Figure 2-5.

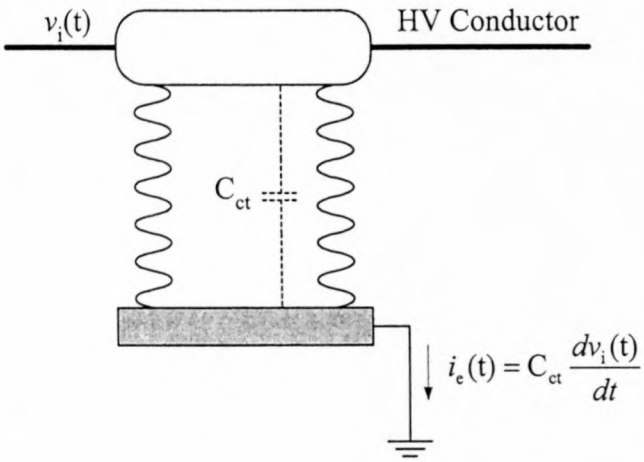

Figure 2-5 HV CT configured in transconductance topology.

The primary voltage is given by $v_i(t)$ and the CT capacitance by C_{ct}. The capacitive earth current is given by $i_e(t)$ of which the value is as shown in Figure 2-5. The primary voltage is derived by integration of the earth current $i_e(t)$. The advantage of this configuration is that the primary voltage $v_i(t)$ is derived without altering the standard CT earthing configuration [11, 13]. This renders the transconductance configuration suitable for non-intrusive wideband voltage measurement.

2.2.2 Practical Implications of the Transconductance Topology

Research indicates that the wideband measurements obtained with the CT configured in a tranconductance topology is less accurate than the CT configuration using the capacitive divider topology [11]. The sensing and integration of the capacitive earth current is required across a wide dynamic range in order to obtain accurate results. The inaccuracy of the integration process is due to inaccurate measurement of the capacitive current. The numerical integration process is also susceptible to stray DC offsets generated by the current measurement devices and results in time-varying drift of the integrated current [11].

A practical CT arrangement in a substation environment consists of multiple earth paths, which requires the accurate summation of the individual earth currents prior to integration. Furthermore, practical experience indicates that the presences of multiple earth paths results in 50 Hz circulating currents as indicated in Figure 2-6. These circulating earth currents are of the order of several amperes [7]. The summation process cancels the circulating 50 Hz in theory although minor differences in the current measurement process may result in a significant 50 Hz component present in the measured capacitive earth current [7].

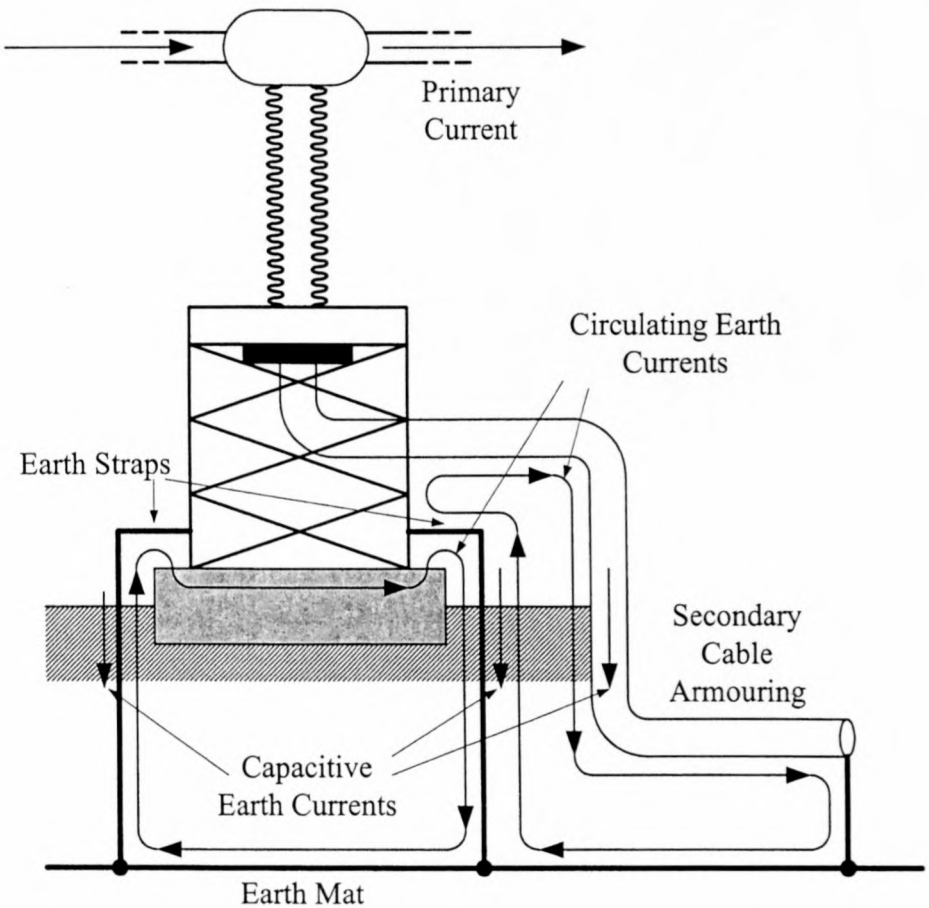

Figure 2-6 Diagram indicating circulating 50 Hz earth currents.

A copper wire twisted pair can be used for transmission of the measured current signal from the HV CT to the location of the acquisition instrumentation. However, the transmission distance may be in excess of 250 m, which results in signal corruption due to the electrically noisy substation environment.

Galvanic isolation of the measurement instrumentation and acquisition devices is important for protection of both the instrumentation and ensuring the safety of the

operating personnel. The bandwidth of normal isolation amplifiers is limited and specially designed wideband isolation amplifiers are required. [15]

Automated recording of transient phenomena is essential and therefore requires the establishment of a configurable data acquisition system capable of storing transient data as well as time stamping information for post-analysis purposes [14].

2.3 Proposed Transient Voltage Monitoring System

2.3.1 Overview

The investigation of section 2.2.2 established some practical aspects of the proposed method to measure transient voltages using the HV CT configured in a transconductance topology. This section presents and investigates a non-intrusive wideband transient voltage monitoring system.

The establishment of a medium to long-term installation for measuring transient phenomena using the HV CT configured in a transconductance topology requires the implementation of the following:

- Real time summation and integration of the individual capacitive earth currents.
- Galvanic isolation of the measurement and acquisition instrumentation.
- Event detection, capture and time stamping of the integrated current signal using a user configurable interface.

In proposed implementation, the above-mentioned criteria is achieved as follows:

- A specially designed wideband analog summation and integration circuit performs the summation of the individual capacitive earth currents and the subsequent integration thereof.
- The use of optic fibre rather than copper wire is proposed for use as a signal transmission medium. Using optic fibre ensures signal quality and isolates the measurement and acquisition instrumentation to ensure the safety of the instrumentation and operating personnel.

- Data acquisition and time stamping is performed by commercially available computer based data acquisition hardware with a software user interface, which is capable of setting transient detection and data acquisition parameters.

The proposed implementation is graphically described in Figure 2-7 for the practical substation arrangement.

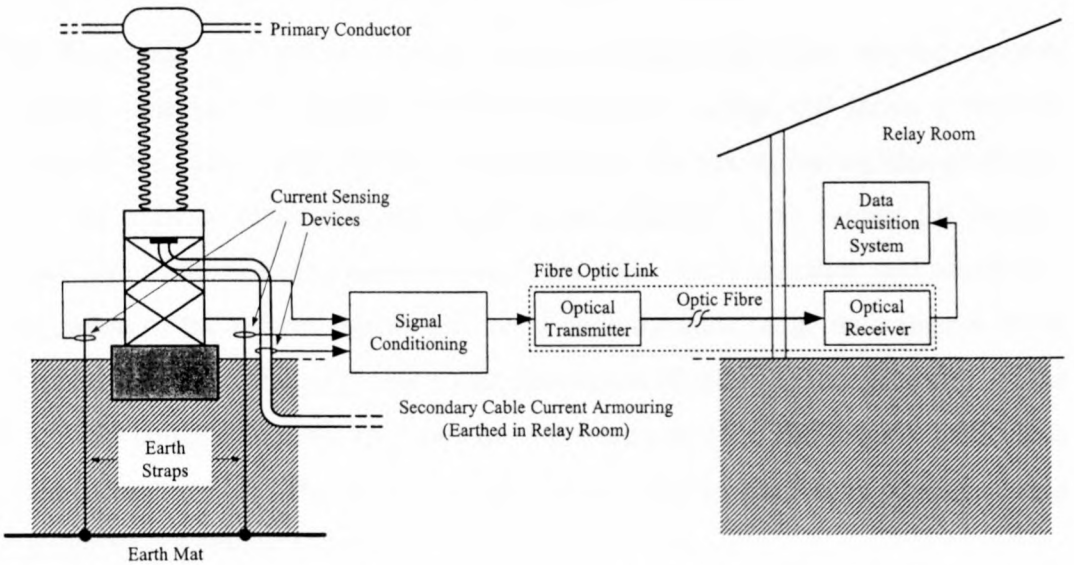

Figure 2-7 Practical substation arrangement with CT configured in a transconductance topology.

Figure 2-7 shows the multiple earth paths, which include two earth straps connecting the earth side enclosure of the CT directly to the earth mat. The third current path is created by the secondary cable armouring, which is earthed in the relay room. The signal conditioning includes the summation of the sensed earth currents and integration of the resultant earth current signal. The integrated current signal is transmitted to the data acquisition system via an optic fibre link. The individual components shown in Figure 2-7 are investigated in the subsections 2.3.2 to 2.3.5.

2.3.2 Wideband Current Sensing Devices

Proper sensing of the capacitive earth currents is important with respect to overall accuracy of the monitoring system. As mentioned earlier the presence of 50 Hz circulating currents requires careful design of the current sensing devices with respect to bandwidth and accuracy. Various methods of current sensing are available. These include the following:

- Magnetic Potentiometers (Rogowski Coil Probe)
- Hall effect sensors
- Current transformers

2.3.2.1 Magnetic Potentiometers (Rogowski Coil Probe)

The Rogowski Coil probe operates on the principle that time varying currents produces time varying magnetic fields that induce a voltage v(t) across a coil that surrounds the current path, which is proportional to the rate of current change di(t)/dt [28]. In order to obtain a signal which is proportional to the current i(t) requires integration of the voltage generated across the coil. The summation and subsequent integration of the current signals requires a wide dynamic range with respect to the practical design of the summation and integration circuitry. The geometry of the Rogowski coil is extremely important for wideband operation and requires meticulous design accuracy [28]. The use of the Rogowski coil for the purpose of current sensing is therefore not practical.

2.3.2.2 Hall Effect Sensors

The Hall effect sensor consists of a constant current conducting metal plate situated in a transverse magnetic field as shown in Figure 2-8.

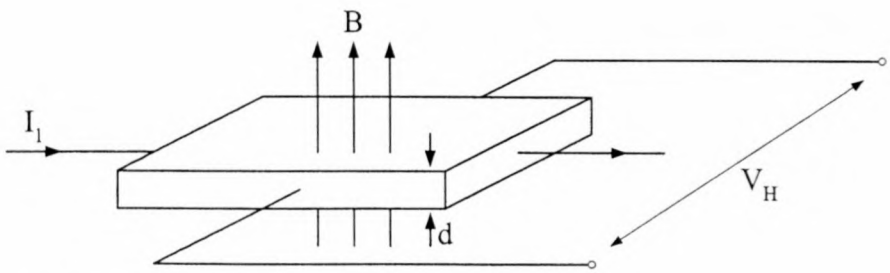

Figure 2-8 Hall effect sensor [30].

I_1 represents the constant current through the metal plate. The time varying flux density B results in a time varying voltage V_H across the metal plate as result of the Lorentz forces [29, 30]. The voltage V_H is proportional to the product of the constant current I_1 and the flux density B and inversely proportional to the plate thickness d.

Placing the Hall effect sensor in the air-gap of an iron core magnetic circuit surrounding the current path performs the measurement of high currents. The time varying current produces a time varying magnetic flux density in the air-gap. The use of Hall effect sensors is mainly for DC and low frequencies. The measurement of high frequencies and fast pulses induces noise, which affects the voltage V_H [28]. The use of Hall effect sensors is therefore not suitable for wideband current sensing.

2.3.2.3 Current Transformers

The use of current transformers with a small valued termination resistor on the secondary windings has been investigated for use in wideband current sensing. The current induced in the secondary windings results in a small voltage drop across the termination resistance, which is proportional to the primary current. This section investigates the effect on the bandwidth as result of the loading of the secondary windings.

The equivalent circuit of the current transformer is shown in Figure 2-9 [22]. R_p represents the resistance of the primary winding and R_s the resistance of the secondary winding. X_p represents the reactance of the inductance as result of the leakage flux of the primary winding. X_s represents the reactance of the inductance as result of the leakage flux of the secondary winding. X_m gives the reactance of the inductance as result of the magnetisation current while the core losses as result of hysteresis and eddy currents is given by R_c. R_l represents the load termination resistance of the secondary winding. V_s give the voltage generated across R_l.

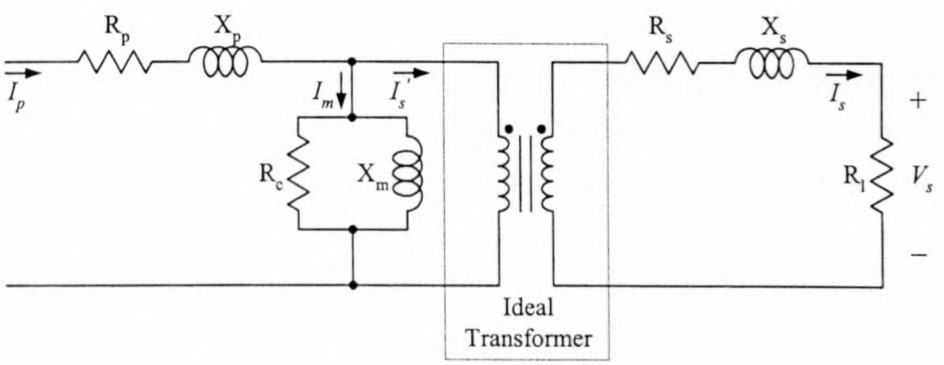

Figure 2-9 Equivalent circuit of the current transformer.

The parameters R_p and X_p concern the primary winding and are neglected in the discussion. The reflected [23] secondary current I_s' is given by the relation shown in equation (2-1).

$$I_s' = I_p - I_m \tag{2-1}$$

The amount of magnetisation current I_m is frequency dependable and is inversely proportional to the frequency due to the reactance X_m. The secondary current is smaller at lower frequencies, as more magnetisation current is necessary to sustain the required flux density. The voltage drop across X_s is larger at higher frequencies as result of the secondary winding leakage flux. This results in a smaller voltage drop across R_l.

The flux density B of the core is given by equation (2-2). The permeability of the core material is given by μ and the mean length of the core by l. N_p represents the number of primary turns and I_p the primary current.

$$B = \frac{\mu N_p I_p}{l} \tag{2-2}$$

Equation (2-2) indicates that the flux density is increased with an increase in permeability, which is reason for selecting a core material with a high permeability. However, materials with high permeability have a limited frequency response. This results into a compromise between bandwidth and permeability. Minimising the path length for the magnetic flux also increases the flux density.

The use of current transformers is promising as this method provides a simple and passive manner of current sensing. The avoidance of active current sensing at each individual current path is attractive and results in a more robust system. The current transformer topology described in this section is therefore practically suitable for current sensing purposes in substation conditions.

2.3.3 Wideband current summation and integration

The implementation of an analog current summation and integration circuit opposed to numerical integration poses numerous design challenges. Numerical integration

has the advantage of relatively unlimited dynamic range. The implementation of the summation and integration process in an analog circuit imposes a dynamic range limit as result of the fixed power supply rails. Proper gain design of the circuitry is therefore essential in order to prevent saturation. Saturation introduces non-linear behaviour, which is not reversible by post-processing routines.

The various stages of the summation and integration circuitry are implemented by using operational amplifier configurations each dictated by the unique characteristics applicable to the design requirements. The individual stages of the summation and integration circuitry are discussed in great detail in chapter 3.

The summation and integration circuitry and the optical fibre transmitter are located at the supporting structure of the HV CT. Shielding of the instrumentation from electromagnetic interference and weather elements is therefore essential.

2.3.4 Signal transmission using optic fibre

As mentioned earlier, the use of copper wire for signal transmission across great distances in electrically noisy environments results in signal corruption. Furthermore, the isolation of instrumentation and the protection of operating personnel are of utmost importance. This has lead to an investigation into the use of optic fibre rather than copper wire for signal transmission. This section provides the foundation for the design of the optical fibre link, which is discussed in detail in chapter 4.

The use of optical fibre requires the implementation of active transmitters and receivers, which often results in excessive power consumption. The design of the optically isolated link is therefore required to include reduced power consumption as a design principle. The physical size of the transmitter unit requires optimisation with respect to portability and cost.

The use of optic fibre rather than copper wire is advantageous due to the following [46, 47]:

- Immunity to electrical interference
- High bandwidth

- Lightweight construction
- Signal attenuation per unit length is less than copper.
- Low cost

The immunity of optic fibre to electrical noise makes it suitable for use in electrically noisy environments such as substations [16, 17]. As result of light being the transmission medium the bandwidth of optic fibre is virtually limited to the bandwidth of the optic fibre transmitters and receivers. The transmission of wideband signals is therefore possible using optic fibre.

There are two basic methods of signal transmission using optic fibre namely analog and digital signal transmission. Both methods are investigated with reference to their individual characteristics and requirements.

2.3.4.1 Analog Signal Transmission

Analog signal transmission utilises the linear region of the optic fibre by varying the light intensity linearly with the magnitude of the analog input signal. Using a single fibre requires the use of specialised wideband optical fibre and laser transmitters. These devices are very expensive and consume vast amounts of power [16]. The use of analog signal transmission is therefore not suitable for the required application. Analog signal transmission using optical fibre is however not without application and is widely used in the American cable television system [18].

2.3.4.2 Digital Signal Transmission

Digital signal transmission using optic fibre is more often used and is subdivided into two categories namely, Pulse Width Modulation (PWM) and digital quantification of the input signal. PWM is in essence a special case of digital quantification as the input signal is quantified as either a digital high or a digital low. PWM is implemented by comparing the input signal with a triangular wave as shown in Figure 2-10. The output of the comparator is either a digital high or low depending of the polarity of the difference between the analog signal and the triangular wave [19].

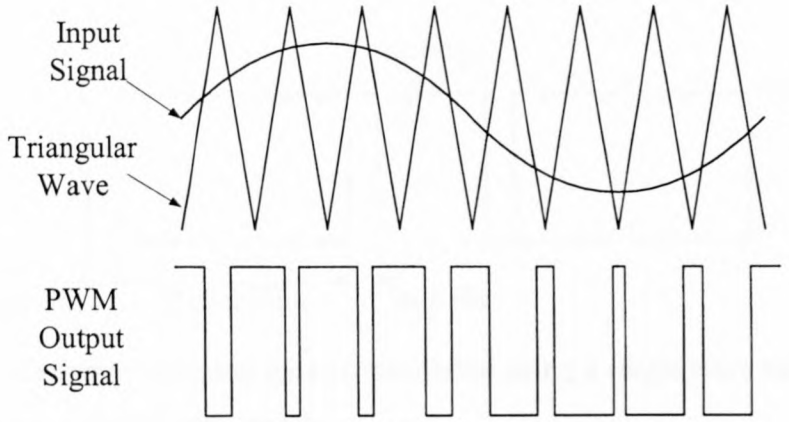

Figure 2-10 Implementation of PWM.

The stream of serial PWM data is transmitted via the optical fibre to the receiver unit. The digital signal from the receiver unit is filtered which produces the demodulated analog signal. The advantage of PWM is relative ease of implementation. The modulation frequency is however required to be at least ten to fifteen times that of the maximum input signal frequency for proper input signal preservation [19].

Digital quantification implies the use of an analog-to-digital converter (ADC). This device produces a digital representation of the analog input signal at a specified resolution and sampling rate [20]. The digital data is converted from a parallel to a serial format and transmitted via the optical fibre using an optic fibre transmitter.

The serial transmission of digital data is performed either in synchronous or asynchronous fashion [21]. Synchronous data transfer implements a master clock frequency at both the transmitting and receiving ends which specifies a preset number of bits in any given time period. This method is highly efficient for applications such as block data transfer in which volumes of data is transferred. However, synchronous data transfer lacks the adaptability to provide for discontinuous operation such as analog-to-digital conversion. Furthermore, the use of synchronous data transfers implements a separate channel for the synchronising clock signal that results in the use of an additional optic fibre channel, which is undesired for the given application.

Asynchronous data transfer requires a signal channel as the data stream contains synchronisation bits in order to synchronise the incoming data stream. Using this method, minor tolerances in the transmitter and receiver clock frequencies are allowed. An example of asynchronous data transfer is shown in Figure 2-11.

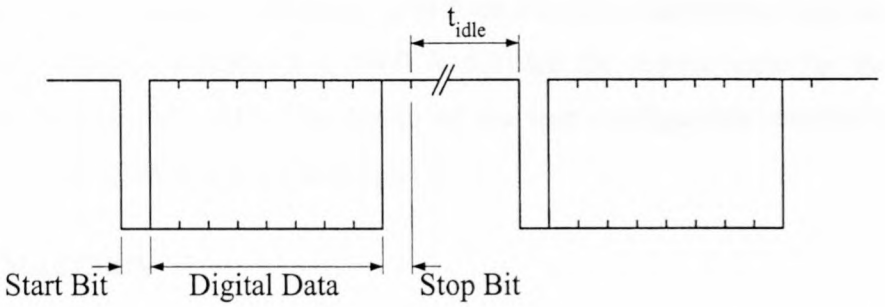

Figure 2-11 Example of digital data transmission using a single start and stop bit with an eight bit data length.

The digital data is preceded by a start bit (which is always a logic low) and terminated by a stop bit (which is always a logic high) in order to establish a data packet. These packets are transmitted sequentially and synchronisation is obtained at the falling edge of each start bit. The length of the digital data is arbitrary although elongated packets may cause synchronisation shift as result of a mismatch between transmitter and receiver clock signals. The time delay between packets is given by t_{idle} and depends on the transmission bit-rate and the frequency of the data packets. In applications that require reduced power consumption this is advantageous, as the system remains idle when data is not transmitted.

The implementation of asynchronous data transfer is more complicated than PWM as the start and stop bits are multiplexed with the digital data. The versatility however of asynchronous digital data transfer is superior to PWM and has been selected as the method for signal transfer using optic fibre.

2.3.5 Data Acquisition System

Section 2.3 indicated the need for a user configurable data acquisition system capable of detecting and recording transient conditions. The system is also required to provide time stamping information for each recorded transient voltage. The time stamping facilitates insight into the origin of the transient voltage with respect to switching activities, lightening impulses and fault conditions.

The data acquisition system has been implemented with commercially available hardware and supporting software.

The range of computer based digitiser cards from National Instruments together with the software design environment LabVIEW fulfilled the requirements for the data acquisition system [38, 44]. The design of the user configurable interface using LABVIEW is discussed in detail in chapter 5.

2.4 Summary

This chapter provided the necessary background information in order to deal with the task at hand. Section 2.1 investigated existing HV measurement topologies, which included CVT and voltage divider topologies. The bandwidth capability of the CVT measurement topology is insufficient for wideband transient voltage measurements. The voltage divider topology provides a means of conducting wideband measurements although the installation and de-installation of these devices require that the HV line be de-energised, which is impractical for routine measurements.

The utilisation of the capacitance which exists between the primary conductor and the earthed base of a standard substation CT is discussed in section 2.2. The CT capacitance is stable up to approximately 500 kHz, which gives raise to two measurement topologies namely a capacitive divider and transconductance topology. The capacitive divider topology is more accurate although it requires alteration of the secure earthing arrangement of the CT, which is undesirable. The transconductance topology requires the sensing and integration of the capacitive earth current.

The proposed transient voltage monitoring system has been given and discussed in section 2.3. The individual components of Figure 2-7 namely the current sensing topology, analog integration, optical fibre signal transfer and data acquisition system is discussed in the subsequent sections.

Chapter 3

Summation and Integration Interface

3.1 Introduction

This chapter deals with the design and implementation of the current summation and integration system. Section 3.2 provides an overview with respect to a block-diagram of the system of which the detail is discussed in sections 3.3 to 3.8. The chapter is concluded with an overview summarising the design of the current summation and integration circuitry.

3.2 Overview

Figure 3-1 shows a block-diagram overview of the summation and integration topology. The block diagram indicates the wideband measurement current transformers monitoring the current in the earth straps. A small resistor R_p terminates the secondary windings of the measurement current transformers. The earth current in the secondary cable armouring is measured using a commercially available clip-on type current probe with a voltage output, because the geometry of the secondary cable armouring is not compatible with the measurement current transformers, which is discussed in greater detail in section 3.4. The instrumentation amplifier amplifies the small voltage across R_p. The individual voltages are summated to produce a resultant current signal v_r. A band-stop filter attenuates the fundamental component of the resultant voltage prior to the integration stage, which produces the integrated current signal v_T.

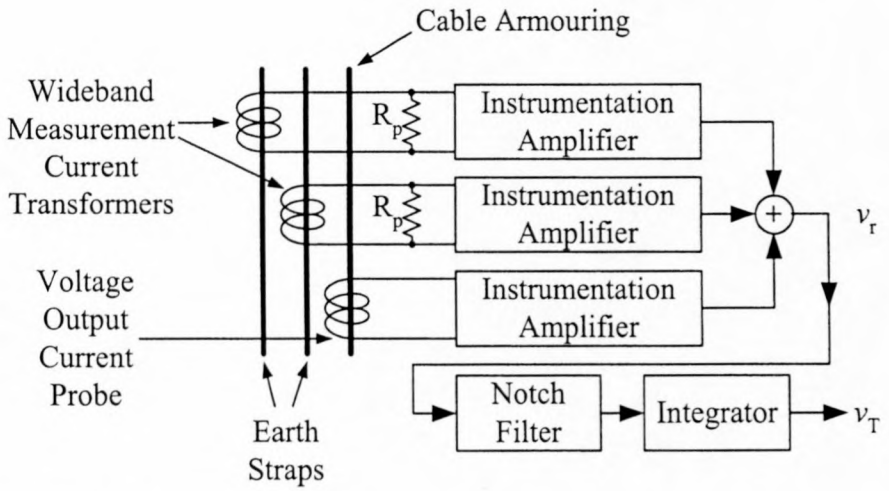

Figure 3-1 Block-diagram of summation and integration circuitry.

As stated earlier the substation current transformer has capacitive coupling between the primary conductor and the earthed base of the CT. The earth current i_e that will flow is given by equation (3-1), where C_{CT} represents the capacitive coupling of the CT, dV_p/dt the rate of change of the phase voltage and i_e the resulting capacitive current [7].

$$i_e = C_{CT} \frac{dV_p}{dt} \tag{3-1}$$

It can be seen from equation (3-1) that that the current is proportional to the derivative of the phase voltage V_p. By integration of the capacitive current i_e a scaled version of the phase voltage can be obtained.

Due to the varying nature of the phase voltage under transient conditions, the dynamic range of the capacitive current is immense. The analog summation and integration circuitry are however limited in dynamic range due to fixed power supply voltage. The design is further complicated by the need to achieve an acceptable signal to noise ratio due to high gains present in the circuit. These factors will be discussed during the course of this chapter.

3.3 Wideband Measurement Current Transformer

The current in the earth straps is measured with specially designed wideband split-core current transformers. The current in the secondary cable armouring is measured using a commercially available clamp-on current transducer. The geometry of the secondary cable armouring renders the use of the split-core current transformers impractical. The implementation of the clamp-on current sensors is discussed in section 3.4. The cross-sectional view of the current transformer is shown in Figure 3-2. The current transformer comprises two core halves, each containing fifty turns. The earth strap is the single turn primary winding of the current transformer. The secondary windings of each half are connected in an additive manner to produce a secondary current as result of a primary current. The primary to secondary winding ratio is 1:100, which implies 40 dB attenuation of the primary current.

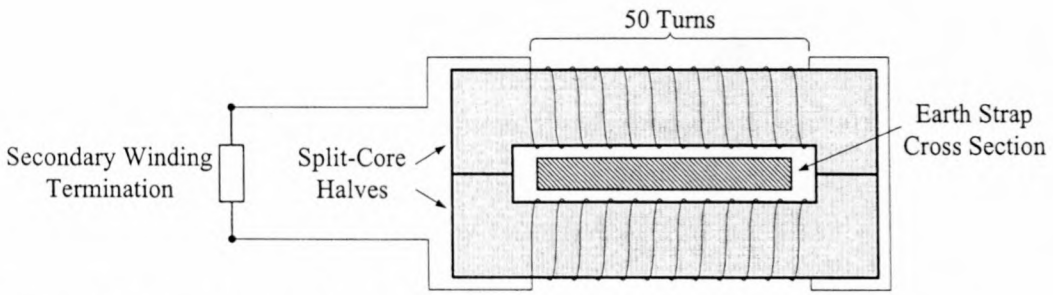

Figure 3-2 Cross-sectional view of the measurement current transformer.

The material used to manufacture the core halves is Ancorsteel CS80. This material has a permeability of 80, which is relatively low although the frequency response is flat up to approximately 100 kHz.

3.4 Clamp-on Current Sensor

The geometry of the cable armouring for the secondary windings of the substation CT differs from the earth straps in that it is a round conductor with a diameter of approximately 25 mm. The split-core current transformer is therefore inappropriate for this purpose.

The current in the secondary cable armouring is measured using a commercially available clamp-on current transducer. The current transducer produces a voltage signal and is specified for the measurement of 50 Hz or 60 Hz currents. However,

evaluation of the current transducer indicated that it is operable across a wider bandwidth, which is discussed in greater detail in section 6.2.

The output of the current transducer is terminated as shown in Figure 3-1. The current transducer is capable of producing an output signal of 200 mV for a full-scale input current of 20 A. The scaling of the output signal is discussed in section 3.5.

3.5 Instrumentation Amplification

This section describes the instrumentation amplifier circuitry used to amplify the signals from the split-core current transformers and the clamp-on current transducer.

Figure 3-3 shows the circuitry for the current sensing and amplification section using the split-core current transformers. The current in each earth strap is represented by i_{es}. The secondary winding of the split-core CT is terminated using a 0.1 Ω resistor R_1. A small voltage is generated across R_1 by the current i_s. The instrumentation amplifier U1 amplifies the small voltage across R_1 with a gain set by R_{rg} [25]. R_2 is used to provide a current path for the input bias currents of the instrumentation amplifier to prevent unnecessary input offset voltages [24]. The value of R_2 is typically 100 kΩ.

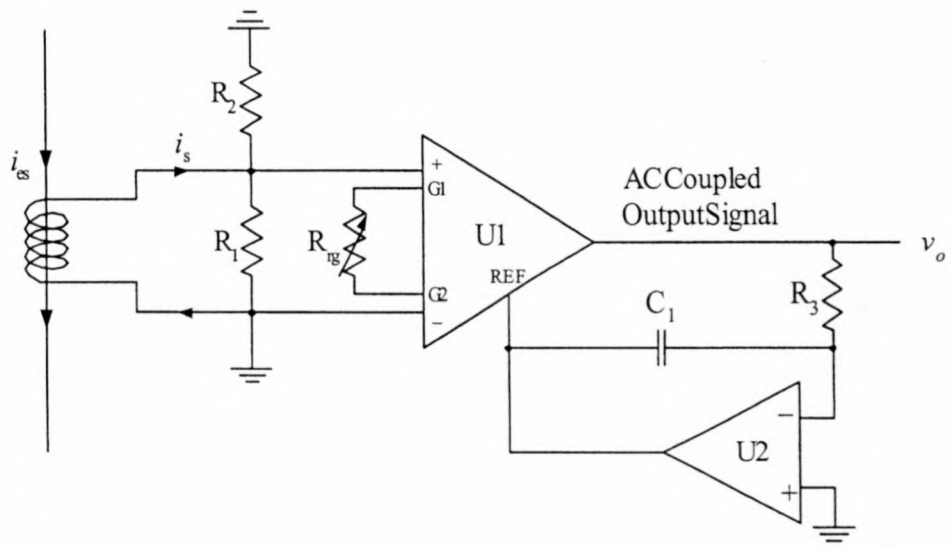

Figure 3-3 Circuit diagram of the current sensing and amplification circuitry for the split-core current transformers.

The circuit consisting of the operational amplifier U2, resistor R_3 and capacitor C_1 is used to implement a low-pass filter with the cut-off frequency given by equation (3-2) [25]. The inverted output signal of the low-pass filter is applied to the reference input of the instrumentation amplifier in order to establish an AC coupled input stage. This arrangement effectively removes DC components from the output of the amplifier stage.

$$f_c = \frac{1}{2\pi R_3 C_1} = \frac{1}{2\pi(1M\Omega)(330nF)} = 0.482\,Hz \tag{3-2}$$

The gain of the instrumentation amplifier is set to 50. The motivation for the selected gain of the instrumentation amplifier is discussed in section 3.9. The transfer function of the instrumentation amplifier and AC coupling circuit is given by equation (3-3), where ω_c represents the cut-off frequency f_c in rad/s and G the gain of the instrumentation amplifier.

$$H_{IA}(s) = \frac{Gs}{s + G\omega_c} \tag{3-3}$$

The gain and phase responses of equation (3-3) is shown in Figure 3-4.

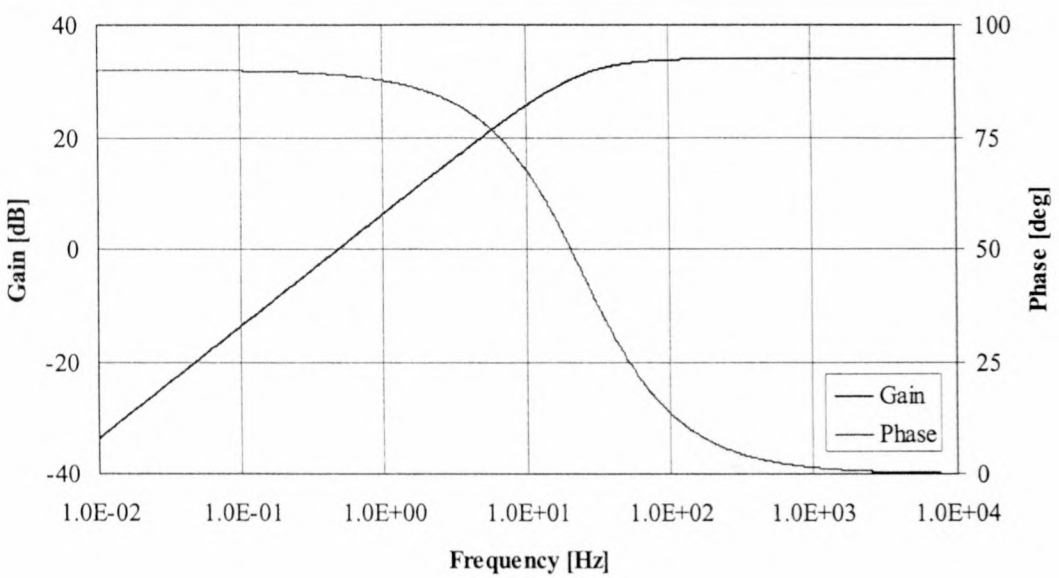

Figure 3-4 Gain and phase responses for the instrumentation amplifier.

Figure 3-4 indicates that the DC component of the instrumentation amplifier output signal is attenuated. The cut-off frequency of the combined circuit of Figure 3-3 is shifted upwards in frequency as result of the gain G. The amplitude and phase responses are however virtually recovered at 1 kHz and will not influence the desired amplitude and phase responses of the signal in the HF pass-band above 1 kHz.

The circuitry used for the clamp-on current transducer is similar to that of the split-core current transformers except for the absence of the termination resistance R_1 as shown in Figure 3-3. This circuit is shown in Figure 3-5, where the current in the secondary cable armouring is represented by i_e, the output voltage of the current transducer is given by v_i and the output voltage of the instrumentation amplifier by v_o.

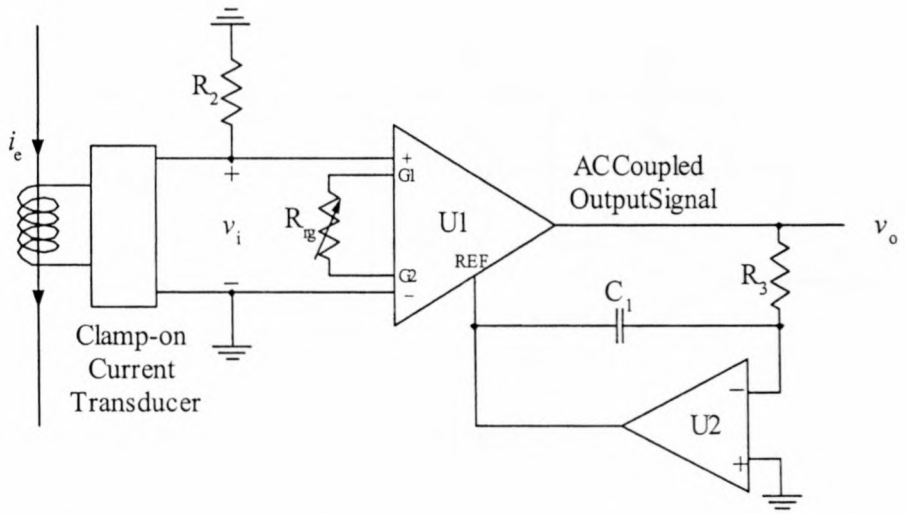

Figure 3-5 Circuit diagram of the sensing and amplification circuitry for the clamp-on current transducer.

The gain of the clamp-on current transducer is 0.01 and the gain of the instrumentation amplifier is set to 5. This gain selection is motivated in section 3.9.

3.6 Summation Circuitry

The summation circuit adds the earth current components in a constructive manner while eliminating the 50 Hz circulating current. The circulating currents in the earth straps and cable armouring are substantial when compared to the desired capacitive current and can be in the excess of 10 A [7].

The summation is achieved by implementing a unity gain, inverting summation operational amplifier configuration as shown in Figure 3-6. The transfer function of the summation circuitry is given in equation (3-4).

$$v_o = -\frac{1}{(sR_{fb}C_{fb}+1)}\left[\frac{R_{fb}}{R_1}v_{i1} + \frac{R_{fb}}{R_2}v_{i2} + \frac{R_{fb}}{R_2}v_{i3}\right] \qquad (3\text{-}4)$$

The resistor values are set to 10 kΩ to produce unity gain and the capacitance C_{fb} is typically in the order of 10 pF. Practical evaluation of this circuit revealed that signals are summated in a less than perfect manner. This is due to tolerance mismatches in the resistor values. This effect is however not serious as it can be rectified by adjusting the gain of the individual instrumentation amplifier stages.

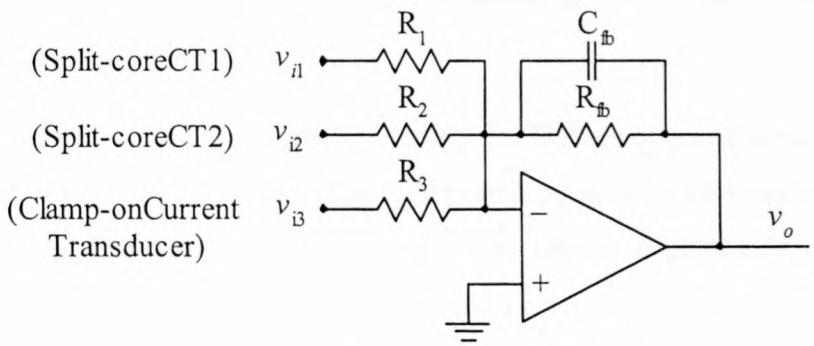

Figure 3-6 Diagram of the summation circuitry.

Capacitor C_{fb} across the feedback resistor R_{fb} is used for frequency compensation due to parasitic input capacitances at the inverting and non-inverting inputs of the operational amplifier. Although these capacitances are small, the effects can be noticeable at higher frequencies.

3.7 Band Reject Filter

As a result of mismatches between the split-core current transformers and the clamp-on current transducer the summation process discussed in section 3.6 fails to eliminate the fundamental 50 Hz circulating current signal entirely. The integrator has very high gain at low frequencies (approximately 26.2 dB at 50 Hz) and saturation will occur for a full-scale output of ±10 V if a 50 Hz signal greater than 489 mV is

applied. This is undesirable as this causes non-linearity, which is not reversible by post signal processing.

Initially a second order high pass filter was used to attenuate the 50 Hz and any other low frequency components present in the summated current signal. The transfer function of unity gain high-pass filter is given in equation (3-5) with the cut-off frequency ω_0 and the quality factor Q [26].

$$H_{HighPass}(s) = \frac{s^2}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2} \tag{3-5}$$

The aim of the design was to place the cut-off frequency of the filter as high as possible in order to obtain the maximum attenuation at 50 Hz, but to maintain an acceptable phase margin at 1 kHz.

The high-pass filter was implemented by using the Butterworth polynomial for the denominator of equation (3-5) [26]. The Butterworth polynomial provides an optimal compromise between gain and group delay. The simulated amplitude and phase responses of the high-pass filter are shown in Figure 3-7.

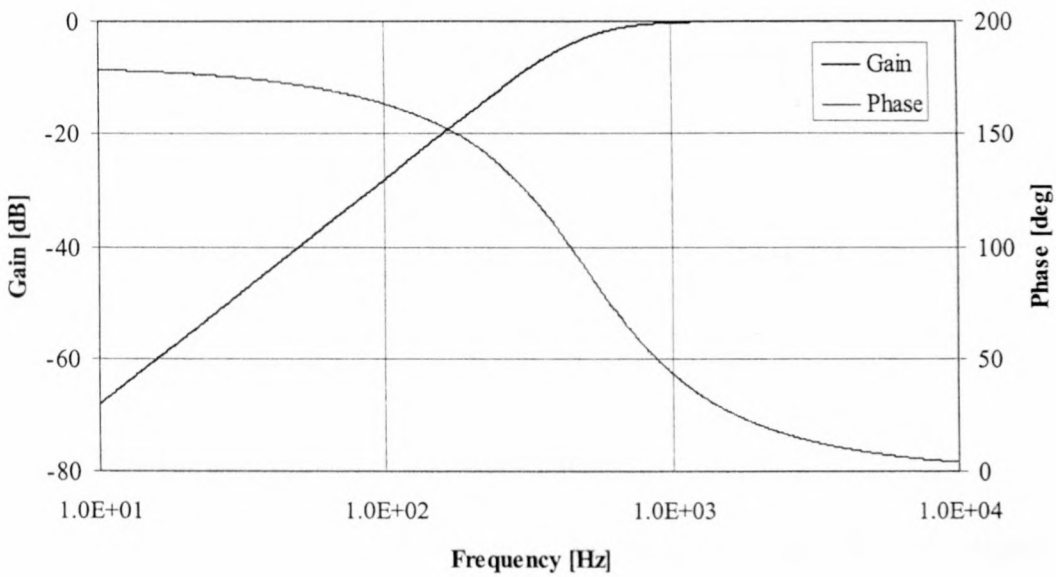

Figure 3-7 Gain and phase responses of the high-pass filter.

The cut-off frequency of the high-pass filter is situated at 500 Hz and the quality factor is 0.707, which describes the Butterworth polynomial. It was however found that the phase response of the high-pass filter failed to restore sufficiently at 1 kHz. A different approach entailed the design of a band reject filter with its centre frequency at 50 Hz. This topology attenuates the 50 Hz frequency component while improving the phase response dramatically. The presence of other low frequency components not attenuated by the band reject filter is acceptable as these components are much smaller than the fundamental component and prevent the integrator from saturation. The transfer function of the band reject filter is given in equation (3-6) [26].

$$H_{BandStop}(s) = \frac{s^2 + \omega_c^2}{s^2 + s\frac{\omega_c}{Q} + \omega_c^2} \tag{3-6}$$

Equation (3-6) gives the transfer function of the band reject filter with the centre frequency at ω_c and quality factor Q. The quality factor determines the width of attenuation at the centre frequency.

Implementation of equation (3-6) was initially realised by a single operational amplifier Sallen Key Biquad section, which is shown in Figure 3-8 [26].

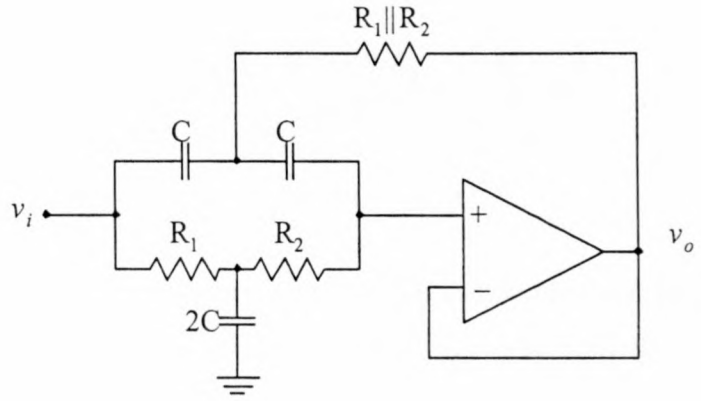

Figure 3-8 Sallen Key Biquad Band Reject Filter

Although the topology realises the transfer function in theory, this operational amplifier configuration is however less stable which causes drift of the centre frequency and quality factor. The filter is also difficult to tune.

A more complex, but more stable and tuneable filter topology is shown in Figure 3-9 [27].

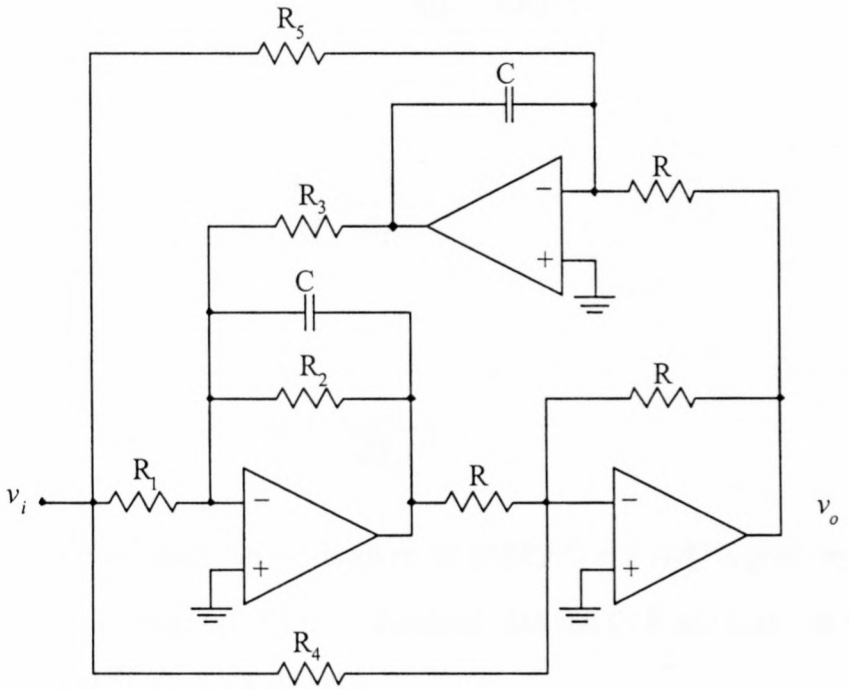

Figure 3-9 A generic Biquad Filter topology.

The generic filter topology of Figure 3-9 realises the transfer function given in equation (3-7).

$$H_{Biquad}(s) = -\frac{\frac{R}{R_4}\left(s^2 + s\frac{RR_1 - R_2R_4}{RR_1R_2C} + \frac{R_4}{RR_3R_5C^2}\right)}{s^2 + s\frac{1}{R_2C} + \frac{1}{RR_3C^2}} \tag{3-7}$$

Upon comparison of equations (3-6) and (3-7) it can be seen that by proper selection of the resistor and capacitor values, equation (3-6) can be realised. This is shown in equation (3-8) and (3-9).

$$R = R_4 = R_5 \tag{3-8}$$

$$R_1 = R_2 \tag{3-9}$$

By substitution of equations (3-8) and (3-9) into (3-7) the transfer function given in equations (3-10), (3-11) and (3-12) is obtained.

$$H_{Band\,Reject}(s) = -\frac{s^2 + \frac{1}{RR_3C^2}}{s^2 + s\frac{1}{R_2C} + \frac{1}{RR_3C^2}} \tag{3-10}$$

where

$$\frac{\omega_c}{Q} = \frac{1}{R_2C} \tag{3-11}$$

and

$$\omega_c = \frac{1}{\sqrt{RR_3C^2}} \tag{3-12}$$

Equation (3-10) indicates that ω_c^2 is given by $1/(RR_3C^2)$ and ω_c/Q is given by $1/(R_2C)$. The value of ω_c is equal to 1 for the normalised case and Q, R and C are set to 1. The values of R_2 and R_3 are calculated at 1.

Frequency scaling is used to calculate the value of C for a centre frequency of 50 Hz. As the frequency increases from 1 rad/s the capacitance decreases by a factor $2\pi(50)$ and the value of C becomes 3.183 mF. This value of C is not practical so impedance scaling is used to produce a more realistic value. The value of C is set to 680 nF and the resistors is scaled accordingly. The value of the impedance scaling constant k_z and resulting resistor values are given in equations (3-13) and (3-14) respectively.

$$k_z = \frac{3.1831\,mF}{680\,nF} = 4681.03 \tag{3-13}$$

$$R = R_1 = R_2 = R_3 = R_4 = R_5 = 4.681\,k\Omega \approx 4.7k\Omega \tag{3-14}$$

The simulated and measured magnitude and phase responses of the filter with the values given in equation (3-13) are shown in Figure 3-10 and Figure 3-10 respectively.

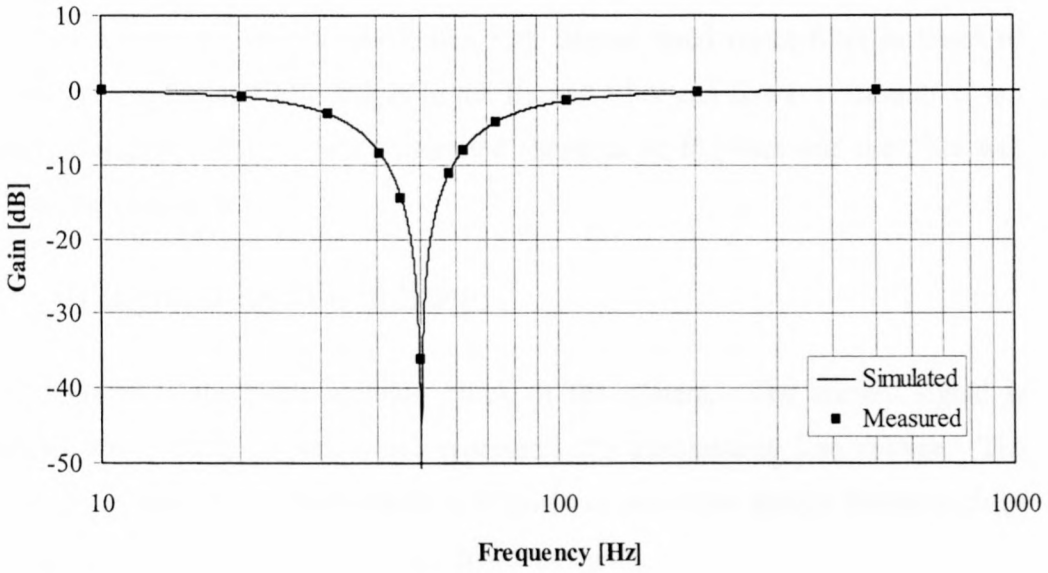

Figure 3-10 Simulated and measured gain of the band reject filter.

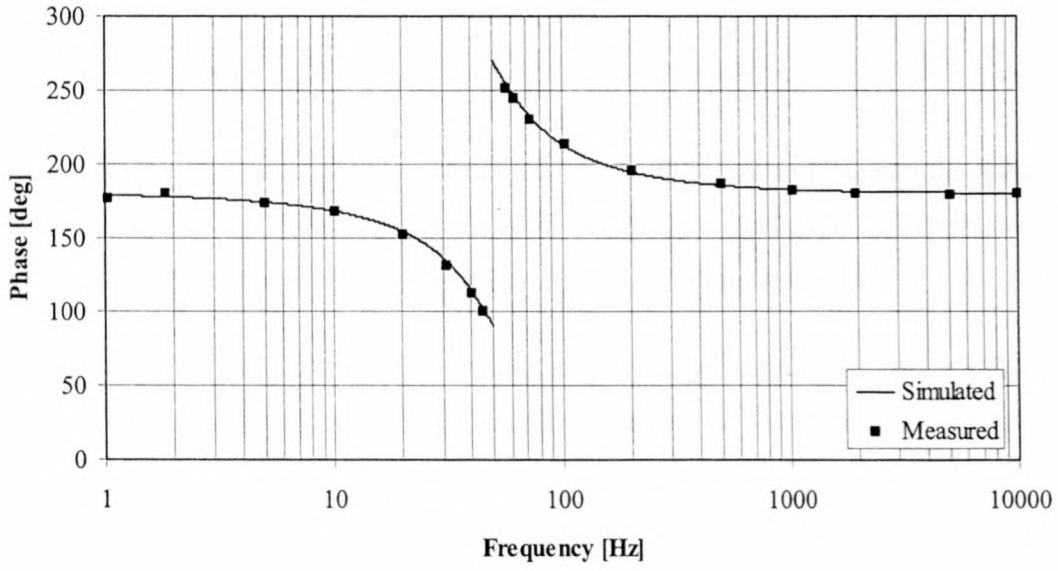

Figure 3-11 Simulated and measured phase of the band reject filter.

Figure 3-11 shows that the phase of the band reject filter approaches 180 degrees as the frequency increases. This is consistent with the inverting nature of the Biquad band reject filter. More importantly is the phase recovery at 1 kHz. The phase is virtually fully recovered and will not influence the phase response of the integrator. The level of attenuation is approximately 40 dB and is sufficient to prevent any saturation in the integrator.

Although the Biquad band reject filter is more complex and requires more elements, its performance is superior to the Sallen Key Biquad band reject filter in terms of stability. The individual gain stages in the Biquad filter can however saturate if not properly designed. This causes a saturated signal to be fed back and the filter will perform unsatisfactory.

3.8 Integrator and Gain Stage

The integrator is the main building block of the system. The current signal is converted to a voltage signal, which represents the transmission line voltage. The design of the integrator is challenging as it involves numerous design factors such as dynamic range, phase response and low frequency gain.

The transfer function describing the integrator is shown in equation (3-15), where G and ω_c represent the gain and the cut-off frequency respectively.

$$H_{\text{int}}(s) = -\frac{G}{s+\omega_c} \tag{3-15}$$

Equation (3-15) is evaluated for the normalised case with ω_c set to 1 Hz and the gain adjusted to produce unity gain at ω equals zero, i.e. where s equals jω. The gain and phase responses for the normalised evaluation are shown in Figure 3-12.

Theory requires that the phase be -90° for proper integration. Figure 3-12 shows that the phase requires approximately two decades to restore to -90° from the cut-off frequency. The integration range is therefore dependent on the position of the cut-off frequency. Moving the cut-off frequency in the direction of the origin increases this range. This causes a lower signal level in the integration range, which is rectified by increasing the integrator gain G. With an increased gain the integrator may saturate for low frequency signals. The design therefore requires an optimal relation between the cut-off frequency and gain G of the integrator.

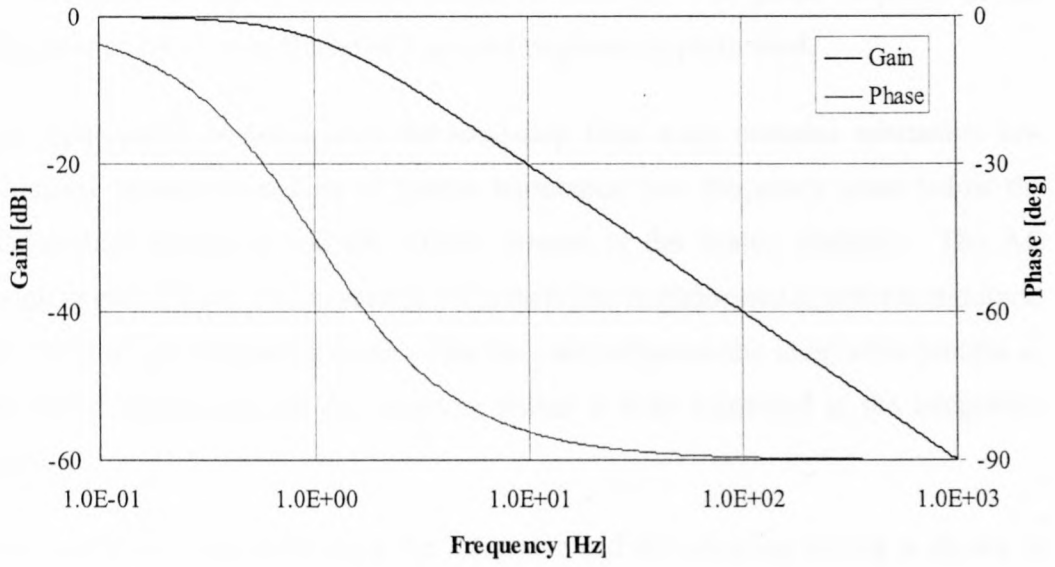

Figure 3-12 Normalised gain and phase responses of the integrator with ω_c set to 1 Hz.

The integration process is desired across three decades from 500 Hz to 500 kHz. The dynamic range of the integrator across this frequency range is therefore 60 dB. The output voltage range of the integration circuitry is $\pm 10\ V_p$, which for the above mentioned specification implies an input signal level of $\pm 10\ mV_p$ at DC. Furthermore, the integration across three decades implies an extremely high LF (low frequency) gain as the gain of the integrator is increased in order to produce a practical signal level in the integration range. This is however impractical as any low frequency noise may result in saturation of the integrator.

The upper cut-off frequency for the desired integration range is compromised by the bandwidth of the measurement current transformers. The frequency response of the measurement current transformers as discussed in section 6.2 indicates that the upper cut-off frequency is situated at approximately 100 kHz.

The cut-off frequency of the integrator is placed at 50 Hz, which results in an acceptable phase response at 1 kHz. The gain is adjusted in order to provide unity gain at 10 kHz. The desired integration range is therefore specified from 1 kHz to 100 kHz, which produces a more practical design. The dynamic range of the integrator is reduced from 60 dB to 40 dB, which implies an input signal level of

$\pm 100\ mV_p$ at DC for a full-scale output of $\pm 10\ V_p$. The phase response of the integrator at 1 kHz is sufficient and proper integration is performed.

The input signal obtained from the band-stop filter stage contains substantial low frequency content consisting of system harmonics, low frequency noise below the fundamental frequency and DC offsets present in the analog circuitry. The AC coupling circuit discussed in section 3.5 is therefore implemented in order to minimise the effect of low-frequency noise. This does not influence the integration process as the phase response of the AC coupling circuit is fully recovered in the integration range.

The transfer function describing the integrator and AC coupling circuit is shown in equation (3-16). The gain G is adjusted to provide unity gain at 10 kHz. The cut-off frequency ω_c is placed at 50 Hz and the cut-off frequency ω_{rc} of the AC coupling circuit at 0.482 Hz. The AC coupling feedback attenuation is represented by A and is set to 0.5.

$$H_{\text{int}(AC\ Coupling)}(s) = -\frac{sG}{s^2 + s\omega_c - A\omega_{rc}G} \tag{3-16}$$

The simulated gain and phase responses of the integrator and AC coupling circuit is shown in Figure 3-13.

The gain and phase responses of Figure 3-13 show that the specified integration range of 1 kHz to 100 kHz remains relatively unaffected by the AC coupling circuit.

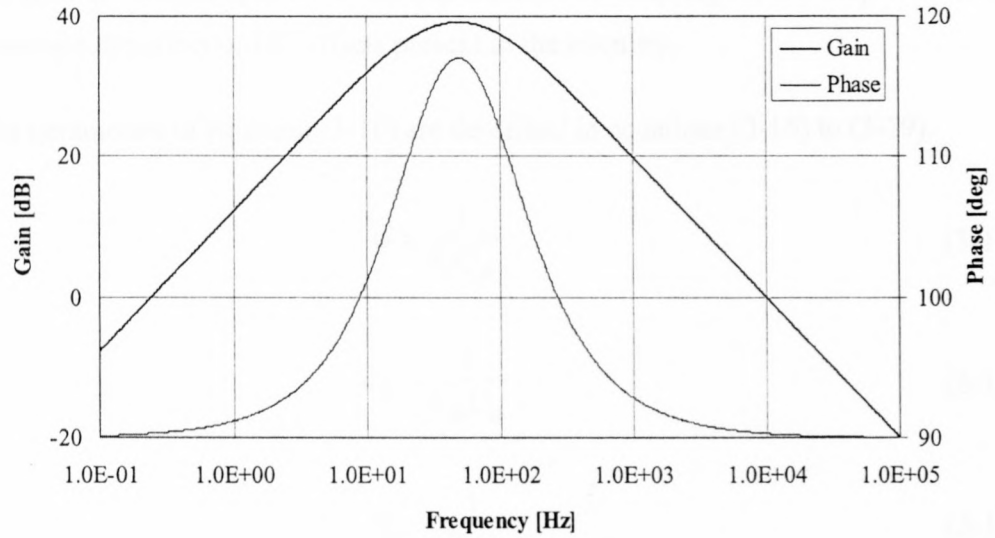

Figure 3-13 Simulated gain and phase responses of the integrator and AC coupling circuit.

The full circuit used for the integration process is shown in Figure 3-14.

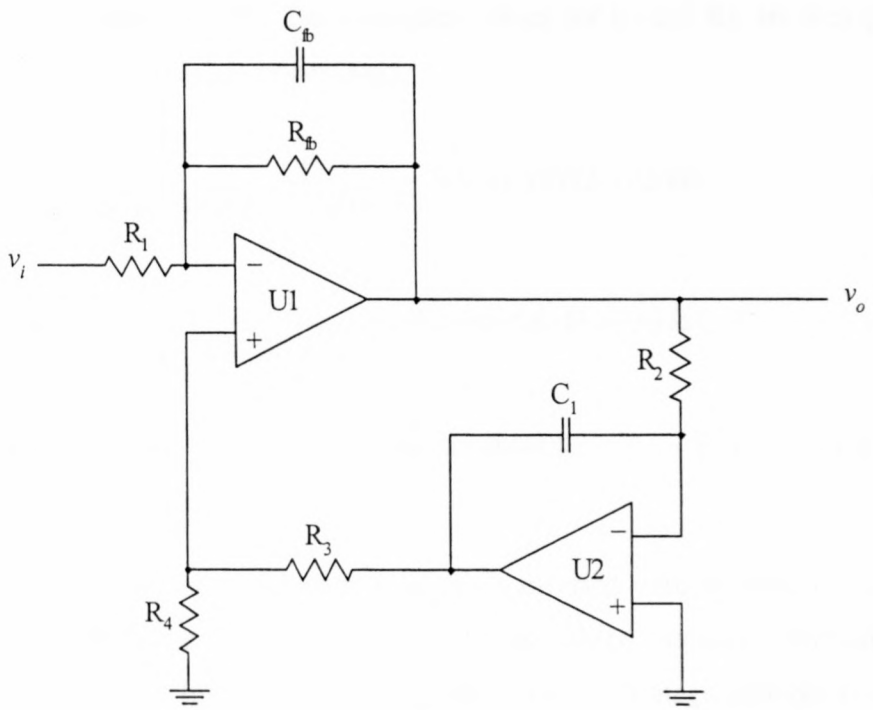

Figure 3-14 Integration circuitry including an AC coupling circuit.

The input signal to the integration circuitry is indicated by v_i and represents the output signal from the band-reject filter. The output signal is represented by v_o. The operational amplifier U1 resistors R_1 and R_{fb} and capacitor C_{fb} perform the

integration. The integrator circuit implements AC coupling on the output in order to minimise the effect of DC offsets present in the circuitry.

The parameters of equation (3-16) are described in equations (3-16) to (3-19).

$$G = \frac{1}{R_1 C_{fb}} \tag{3-17}$$

$$\omega_c = \frac{1}{R_{fb} C_{fb}} \tag{3-18}$$

$$\omega_{rc} = \frac{1}{R_2 C_1} \tag{3-19}$$

$$A = \frac{R_4}{R_4 + R_3} \tag{3-20}$$

The value of G for unity gain at 10 kHz is calculated as 62834.153. The value of the capacitor C_{fb} is set to 10 nF. The calculated values for R_1 and R_{fb} are then given by equations (3-21) and (3-22) respectively.

$$R_1 = \frac{1}{GC_{fb}} = \frac{1}{(62834.153)(10nF)} = 1591.491\,\Omega \approx 1.5\,k\Omega \tag{3-21}$$

$$R_{fb} = \frac{1}{\omega_c C_{fb}} = \frac{1}{(2\pi 50)(10nF)} = 318309.886\,\Omega \approx 318\,k\Omega \tag{3-22}$$

The values of R_2 and C_1 are as indicated in equation (3-2). The values of R_3 and R_4 are both set to 10 kΩ.

The polarity of the integrator output signal is inverted with respect to the current signal produced by the instrumentation amplifiers. This is however rectified with an inverting gain stage following the integrator. The gain stage restores the desired polarity and may be used to alter the overall gain of the system. The circuit used for the gain stage is shown in Figure 3-15.

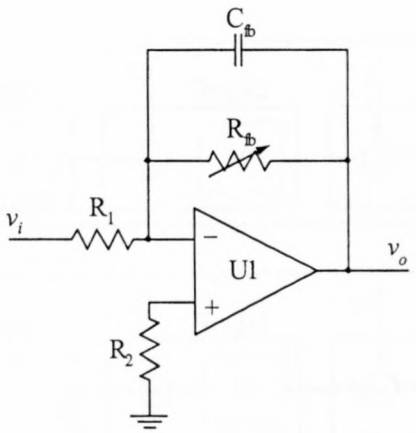

Figure 3-15 Circuit diagram for the gain stage.

The transfer function describing the gain stage of Figure 3-15 is given in equation (3-23). C_{fb} is a small valued capacitor used for compensation purposes as discussed in section 4.3.1. R_2 is used to minimise input offset voltages as discussed in section 4.3.1.

$$H_{Gain} = -\frac{R_{fb}}{R_1}\left[\frac{1}{sC_{fb}C_{fb}+1}\right] \tag{3-23}$$

3.9 System Gain Design

This section discusses the motivations for the gain selections given in the course of this chapter. The selection of gains for the individual stages is based on various factors, which includes dynamic range and noise.

Improper choice of gains results in an unsatisfactory signal-to-noise ratio. Figure 3-16 shows a block-diagram of two systems with identical total gain, although with different gain distributions. The same input signal x to both systems give the output y_A and y_B of System A and System B respectively. The noise generated by each stage is represented by v_n.

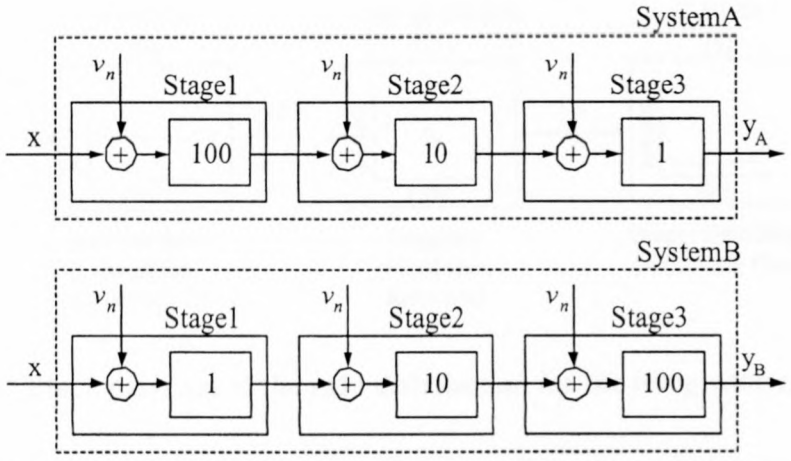

Figure 3-16 Example of proper and improper gain placement.

The output signals of System A and System B is given in equations (3-24) and (3-25) respectively.

$$y_A = 1000x + 1011v_n \tag{3-24}$$

$$y_B = 1000x + 2100v_n \tag{3-25}$$

Both systems produce the same amplification for the input signal but System 1 produces less noise than System 2. The placement of high gain is therefore preferred in earlier stages of the circuit in order to minimise the amplification of noise generated by the circuitry.

The dynamic range of the circuitry is ±10 V. The gain of the amplification stage following the integrator is set to 5. This value is adjustable for evaluation purposes as the gain of the integrator is fixed. The maximum output signal of the integrator is therefore ±2 V. Headroom of ±1 V is allowed on the output of the integrator, which results in a maximum output level of ±1 V for the integrator. The gain of the integrator is specified for unity gain at 10 kHz, which implies a gain of –20 dB at 100 kHz. A lower integrator gain results in higher gain of the amplification stage following the integrator, which is ill advised with respect to the argument of gain placement discussed earlier in this section. The maximum input signal to the integrator at 100 kHz is therefore ±10 V. The block diagram representation of the gain distribution is shown in Figure 3-17.

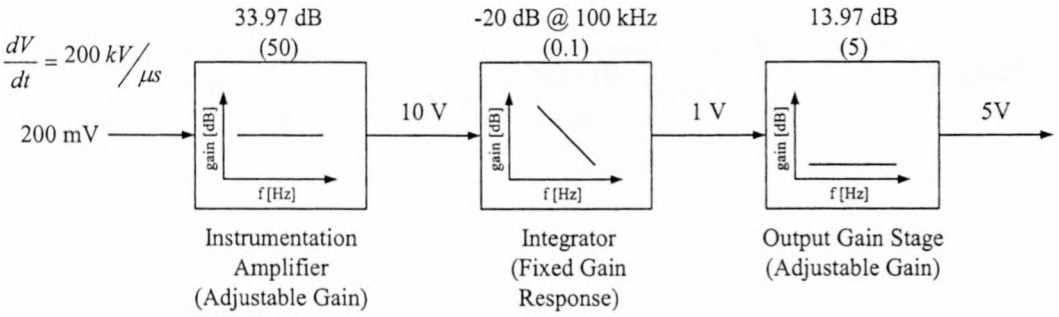

Figure 3-17 Block diagram of the gain distribution for the integrator circuitry.

The dynamic range concerning the rate of change of the transmission line voltage is determined by the gain of the instrumentation amplifiers. The voltage across the pickup resistors terminating the split-core current transformers and the output voltage from the clamp-on current transducer is amplified to produce a practical voltage level for signal conditioning purposes. The desired rate of change measurement for the transmission line voltage is set for 200 kV/µs. The calculated gain G_{IA} for the instrumentation amplifiers in the case of the split-core current transformers is shown in equation (3-26). The output signal of the instrumentation amplifier is represented by v_{IA}, the substation CT capacitance by C_{CT}, the rate of change of the transmission line voltage by dV/dt, the split-core CT attenuation by G_{CT} and the value of the termination resistance by R_p.

$$G_{IA} = \frac{v_{IA}}{C_{CT}\frac{dV}{dt}G_{CT}R_p} = \frac{10}{\left(1\times10^{-9}\right)\left(\frac{200\times10^{3}}{1\times10^{-6}}\right)(0.01)(0.1)} = 50 \qquad (3\text{-}26)$$

The gain of the instrumentation amplifier is therefore set to 50, which produces a full-scale signal of ±10 V for the desired rate of change of the transmission line voltage. This gain setting also complies with the issue of gain distribution with respect to noise, as the input signal is amplified to the maximum capable dynamic range for the circuitry.

The output of the clamp-on current transducer is a voltage signal. The gain of the instrumentation amplifier in the case of the clamp-on current transducer is therefore calculated as shown in equation (3-27). The gain of the current transducer is given by G_{CTD}.

$$G_{IA} = \frac{v_{IA}}{C_{CT}\frac{dV}{dt}G_{CTD}} = \frac{10}{\left(1\times10^{-9}\right)\left(\frac{200\times10^{3}}{1\times10^{-6}}\right)(0.01)} = 5 \qquad (3\text{-}27)$$

3.10 Summary

This chapter presents the design procedure for the summation and integration system. The system is presented at block-diagram level in section 3.2 with reference to the basic operating principles of the system. The design and implementation of the block-diagram of Figure 3-1 is extended across sections 3.3 to 3.9.

The current sensing arrangement consists of two wideband split-core current transformers and a clamp-on current transducer, which is discussed in sections 3.3 and 3.4. The split-core CT's measure the current in the earth straps and the clamp-on current transducer the current in the secondary cable armouring. The secondary current from the split-core CTs is determined using a small termination resistance and amplified using an instrumentation amplifier, which is discussed in section 3.5. The voltage signal obtained from the clamp-on current transducer is amplified for the summation process.

The summation process is discussed in section 3.6 and reference has been made to the practical effects due to tolerance variations in resistor values. The band reject filter discussed in section 3.7 attenuates the fundamental frequency in order to prevent saturation of the integrator.

The integrator stage is thoroughly discussed in section 3.8 with respect to factors such as dynamic range, low frequency gain and phase responses. The system gain selections are discussed in section 3.9 and provides valuable insight into and motivation for proper gain distribution.

Chapter 4

Optically Isolated Link

4.1 Introduction

When conducting wideband measurements in an electrically noise environment, such as a substation, the use of a conductive medium to transfer measured signals compromises signal quality. The location of the instrumentation is usually not close to the measurement point and therefore the signals must be transferred across great distances, which increases the exposure to electrical noise.

The insulation of the measurement instrumentation is very important in a high voltage environment to protect the instrumentation and the operating personnel. This implies the use of costly isolation amplifiers, which lacks the bandwidth required to conduct wideband measurements.

This chapter presents a low power isolated link using optic fibre, which is able to transfer high bandwidth signals and is insensitive to electrical noise. The subsections of this chapter will introduce the operating principle, design and implementation of the optically isolated link.

4.2 Overview

A block diagram of the isolated link is shown in Figure 4-1. It comprises two units namely a transmitter and receiver unit connected via optic fibre. The input stage of the transmitter unit consists of a buffer and anti-aliasing low-pass filter. The buffer establishes the input impedance and the low-pass filter ensures the integrity of the digital data. The signal is digitised and serially transmitted to the receiver unit. At the receiver unit the serial digital signal is translated to parallel data and converted to an analog signal. The parallel data is also available for data acquisition purposes.

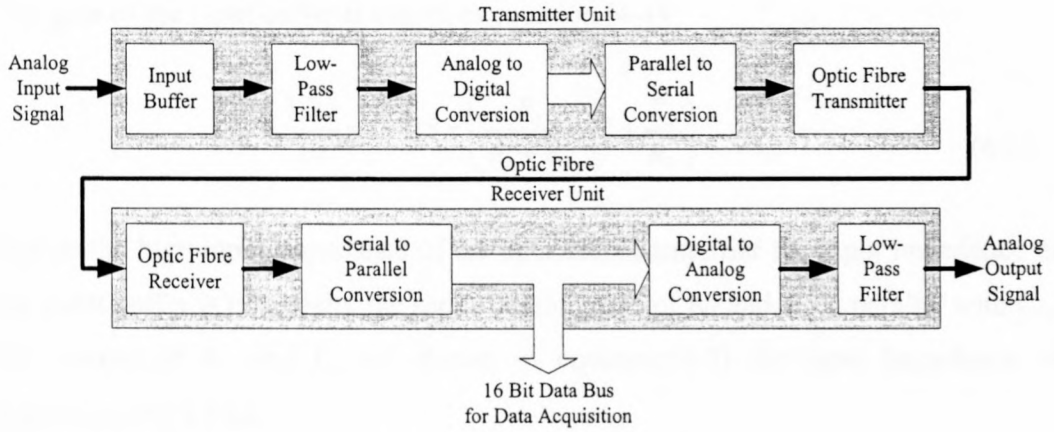

Figure 4-1 Block diagram of the optically isolated link.

4.3 Transmitter Unit

This section discusses the design of the transmitter unit as indicated in the block diagram of Figure 4-1.

4.3.1 Input Buffer

The circuit diagram of the input buffer is shown in Figure 4-2.

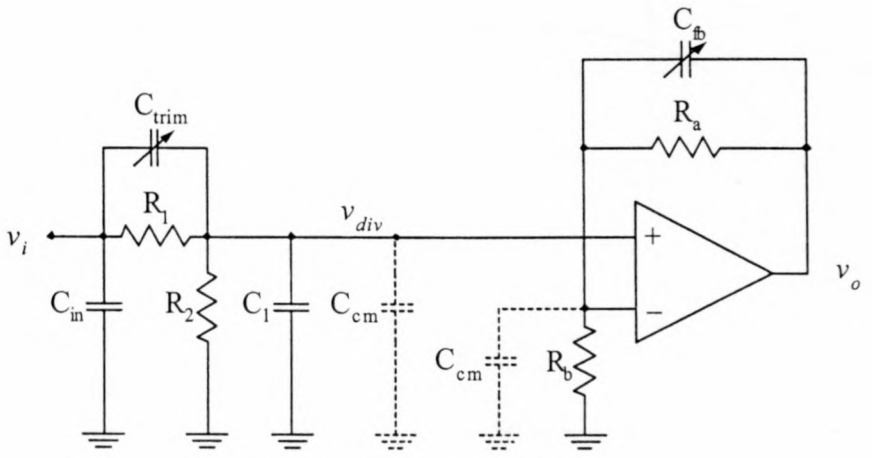

Figure 4-2 Circuit diagram of the input buffer.

Figure 4-2 shows the input buffer with the input capacitance C_{in}. R_1, R_2, C_{trim} and C_1 represent the voltage divider. C_m represents the common mode input capacitance of the operational amplifier. R_a and R_b determine the gain of the non-inverting amplifier and C_{fb} is used for compensation purposes.

The gain of the input buffer is shown in equation (4-1).

$$G_{ib} = \frac{1.25}{10} = 0.125 = \left(\frac{R_2}{R_1 + R_2}\right)\left(1 + \frac{R_a}{R_b}\right) \tag{4-1}$$

Due to the high input impedance of the operational amplifier the input impedance of the input buffer is essentially the series combination of R_1 and R_2 in parallel with C_{in}. The values of R_1 and R_2 are shown in equation (4-2) for input impedance of approximately 1 MΩ.

$$R_1 = 910\,k\Omega \text{ and } R_2 = 91\,k\Omega \tag{4-2}$$

The gain of the non-inverting amplifier is calculated at 1.375.

Figure 4-2 shows the common mode input capacitance C_{cm} of the operational amplifier. For the specific operational amplifier [31] the common mode input capacitance is 6 pF. Figure 4-3 shows the impedance of the parallel combination of R_2 and C_{cm} as a function of frequency.

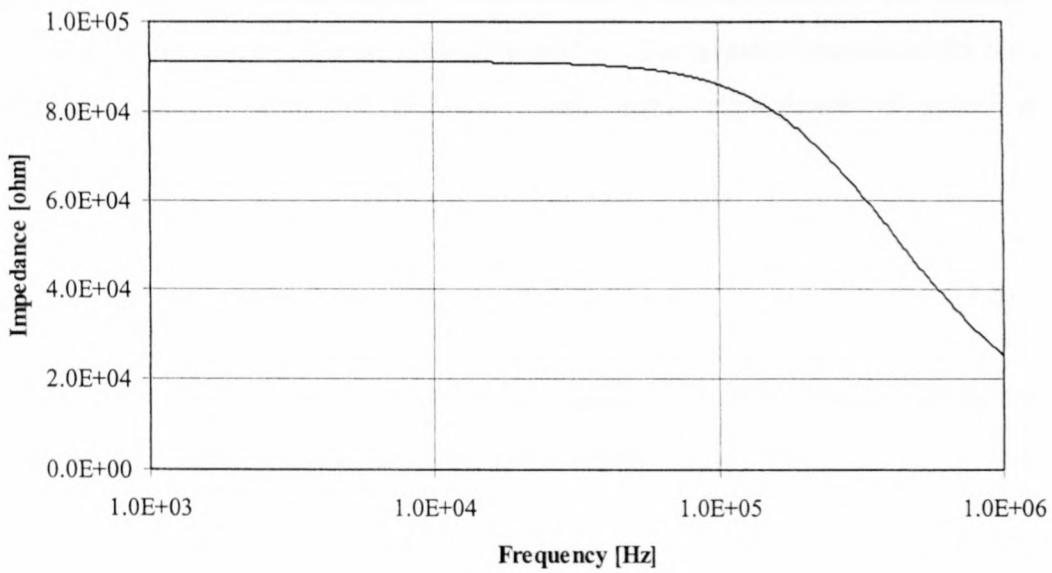

Figure 4-3 The impedance of R_2 || C_{cm} as a function of frequency.

It can be seen from Figure 4-3 that the attenuation of the voltage divider is influenced by the common mode input capacitance of the operational amplifier. The variable

capacitor C_{trim} across R_1 compensates for this effect. The transfer function of the voltage divider including C_{trim} is shown in equation (4-3).

$$H_{div}(s) = \frac{C_{trim}}{C_{trim} + C_{cm}} \left(\frac{s + \frac{1}{R_1 C_{trim}}}{s + \frac{R_2 + R_1}{R_1 R_2 (C_{trim} + C_{cm})}} \right) \tag{4-3}$$

Equation (4-3) shows that C_{trim} introduces a zero in the numerator which if set equal to the pole in the denominator can eliminate the frequency dependency of the voltage divider. The comparison results in the ratio indicated in equation (4-4).

$$\frac{R_2}{R_1} = \frac{C_{trim}}{C_{cm}} \tag{4-4}$$

With the known values of R_1, R_2 and C_{cm} the value of C_{trim} is calculated at 0.6 pF. Commercially available trimming capacitors are incapable of such small variation ability. For this reason the capacitor C_1 is introduced to increase the value of C_{cm} and therefore the value of C_{trim}.

The gain of non-inverting amplifier configuration is also affected by the common mode input capacitance of the operational amplifier. The transfer function of the non-inverting amplifier with the common mode input capacitance is given in equation (4-5).

$$H_{ni} = \left(sR_a C_{cm} + \frac{R_a + R_b}{R_b} \right) \tag{4-5}$$

The frequency response of the non-inverting amplifier referenced to 0 dB with R_a and R_b equal to 3.75 kΩ and 10 kΩ respectively is shown in Figure 4-4.

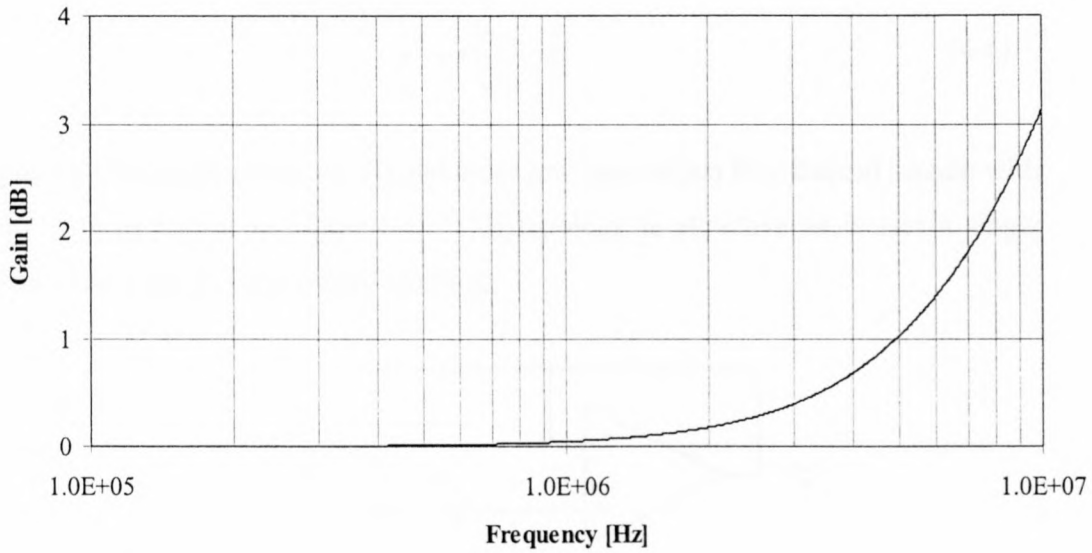

Figure 4-4 Normalised gain response of the non-inverting amplifier.

The effect of C_{cm} on the gain response of the non-inverting amplifier is negligible below 1 MHz. The need for the feedback trimming capacitor C_{fb} is therefore not necessary.

4.3.2 Anti-Aliasing Low-pass Filter

During the digitisation process the signal is sampled at a rate f_s of 1 Million Samples Per Second (MSPS). According to the Nyquist criteria [20], a signal can be successfully reconstructed if sampled at more than or equal to twice the maximum frequency present in the signal. The reason for this is that sampled frequencies above $f_s/2$ fold back symmetrically around $f_s/2$, which is known as aliasing. When a signal is sampled at 1 MSPS the 900 kHz frequency component appears in the sampled signal at 100 kHz. The filter must be designed properly in order to provide enough attenuation to prevent aliasing.

The application further requires that no time domain distortion occur due to varying delays in the system. The implementation of the low-pass filter must therefore ensure a constant group delay in the pass-band. The transfer function of the unity gain low-pass filter is given in equation (4-6) [26].

$$H_{lp}(s) = \frac{\omega_0^2}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2} \tag{4-6}$$

Equation (4-6) implements the second order low-pass Sallen Key Biquad section with unity gain as shown in Figure 4-5. This topology is attractive as it uses a single operational amplifier and is non-inverting.

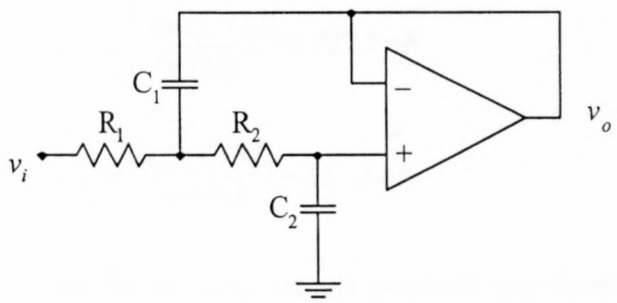

Figure 4-5 Second order low-pass filter Sallen Key Biquad topology.

The transfer function describing the filter shown in Figure 4-5 is given in equation (4-7).

$$H_{lp}(s) = \frac{\frac{1}{R_1 R_2 C_1 C_2}}{s^2 + s\left(\frac{1}{R_2 C_1} + \frac{1}{R_1 C_1}\right) + \frac{1}{R_1 R_2 C_1 C_2}} \tag{4-7}$$

The design procedure requires that R_1 and R_2 are equal to 1 for the normalised case. The resulting expressions for C_1 and C_2 are shown in equations (4-8) and (4-9) respectively.

$$C_1 = \frac{2Q}{\omega_0} \tag{4-8}$$

$$C_2 = \frac{1}{2\omega_0 Q} \tag{4-9}$$

The filter employs the Bessel Thompson polynomial in the denominator of equation (4-6). The amplitude response of the Bessel Thompson filter is slower than other filter configurations but it has a constant group delay, which is desirable in this

application [26]. Implementation of the Bessel Thompson polynomial requires that the values of ω_0 and Q are 1.732 and 0.577 respectively. The normalised values of C_1 and C_2 are therefore 0.666 and 0.5 respectively.

The cut-off frequency of the filter is placed at 250 kHz. The capacitor values are scaled by a factor $250\times10^3/1.732$ and the resulting capacitor values for C_1 and C_2 are given in equations (4-10) and (4-11) respectively.

$$C_1 = \frac{(0.66)(1.732)}{2\pi 250k} = 727.7\,nF \tag{4-10}$$

$$C_2 = \frac{(0.5)(1.732)}{2\pi 250k} = 551.3\,nF \tag{4-11}$$

These values of R_1 and R_2 are however not practical and therefore C_1 are set to 470 pF. The reason for selecting the capacitor value rather than the resistor value is the fact that resistors have less widespread intervals than capacitors and are therefore easier to match. The impedance-scaling factor is shown in equation (4-12).

$$K_z = \frac{C_1}{470pF} = \frac{727.7\,nF}{470\,pF} = 1548.3 \tag{4-12}$$

The calculated values for the resistors R_1 and R_2 and the capacitors C_1 and C_2 are given in equation (4-13) and (4-14) respectively.

$$R_1 = R_2 = 1584\,\Omega \approx 1500\,\Omega \tag{4-13}$$

$$C_1 = 470\,pF \text{ and } C_2 = \frac{553.1\,nF}{1548.3} = 357.23\,pF \approx 330\,pF \tag{4-14}$$

The amplitude response of the filter with the values given in equations (4-13) and (4-14) is shown in Figure 4-6.

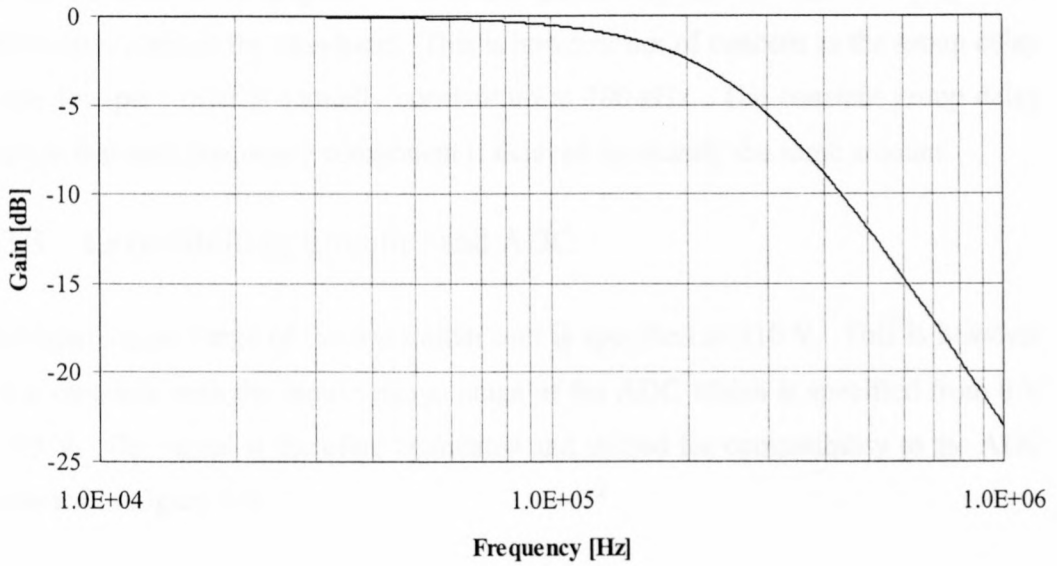

Figure 4-6 Amplitude response of the anti-aliasing low-pass filter.

Figure 4-6 shows that the gain of the low-pass filter is essentially flat up to 100 kHz. The attenuation at 900 kHz is approximately 22 dB. This implies that the aliasing of frequency components above 900 kHz will be attenuated by at least 22 dB.

The phase response and group delay of the low-pass filter is shown in Figure 4-7.

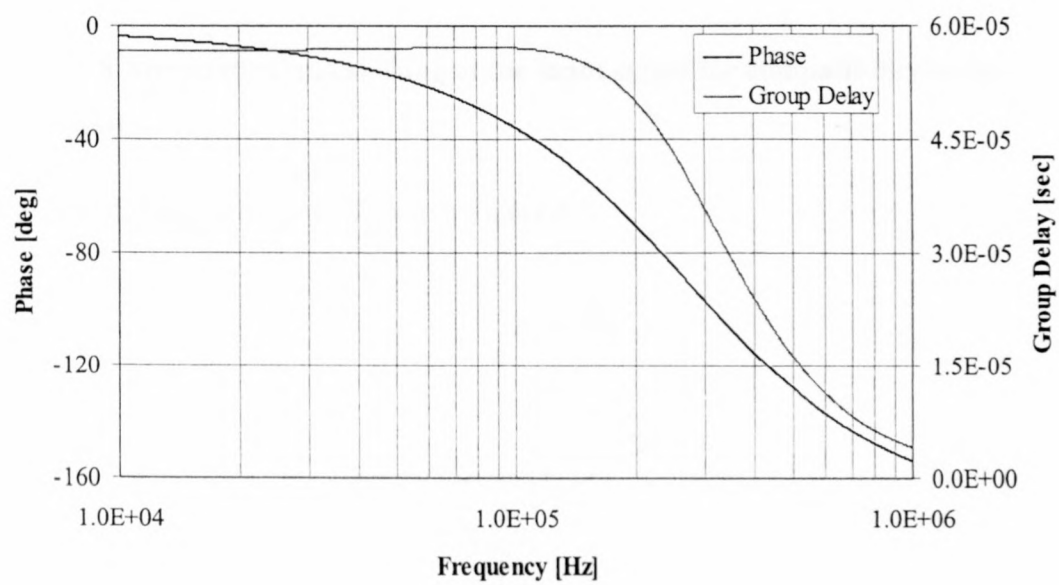

Figure 4-7 Phase response and group delay of the anti-aliasing low-pass filter.

It can be seen from Figure 4-7 that the phase response of the low-pass filter deteriorates early in the pass-band. This is however not of concern as the group delay of the low-pass filter is virtually constant up to 100 kHz. The constant group delay implies that each frequency component is delayed by exactly the same amount.

4.3.3 Level Shifting Circuitry and ADC.

The input signal range of the transmitter unit is specified at ±10 V. This is however not compatible with the input voltage range of the ADC which is specified from 0 V to 2.5 V. The signal is therefore attenuated and shifted for compatibility to the ADC as shown in Figure 4-8.

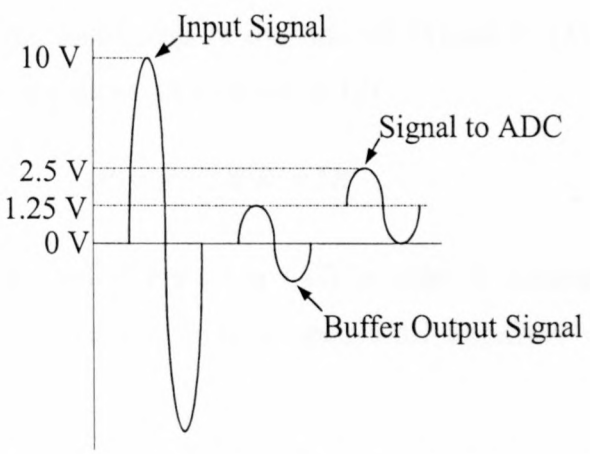

Figure 4-8 Attenuation and shifting of the input signal for compatibility to the ADC.

The level shifting circuitry is shown in Figure 4-9.

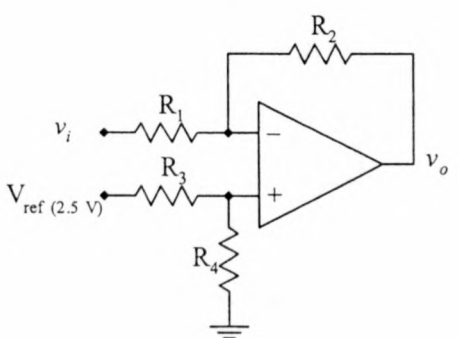

Figure 4-9 Level shifting circuitry.

The voltage v_i is the output voltage of the anti-aliasing filter. The output voltage v_o of the level shifting circuitry is shown in equation (4-15).

$$v_o = -\frac{R_2}{R_1} v_i + \frac{2R_4}{R_3 + R_4} V_{ref} \tag{4-15}$$

As shown in Figure 4-8 the full-scale input signal to the transmitter unit is attenuated to a peak level of 1.25 V. Level shifting of this signal by 1.25 V will produce a signal ranging from 0 V to 2.5 V as indicated in Figure 4-8. The resulting transfer function of Figure 4-9 is shown in equation (4-16).

$$v_o = v_i + 0.5V_{ref} \tag{4-16}$$

By comparison of the coefficients of equations (4-16) and (4-15) the resulting ratios of R_1, R_2, R_3 and R_4 are shown in equation (4-17).

$$R_1 = R_2 \text{ and } R_3 = 3R_4 \tag{4-17}$$

The values of R_1, R_2 and R_3 are set to 1 kΩ in order to minimise the effect of the common mode input capacitance of the operational amplifier. The value of R_4 is calculated at 3 kΩ.

The reference voltage for the level shifting circuitry is generated by a 2.5 V reference diode as shown in Figure 4-10.

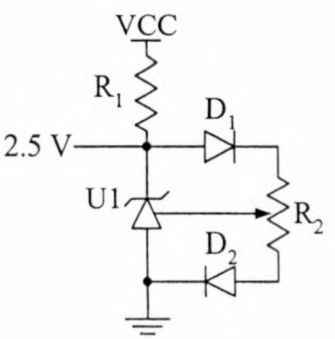

Figure 4-10 Circuit diagram of the reference voltage diode.

Resistor R_1 determines the reverse current through the reference diode U1 [32]. The variable resistor R_2 is used for tuning purposes and the diodes D_1 and D_2 are used to provide a low temperature coefficient [32]. Due to loading of the 2.5 V output of the

circuit shown in Figure 4-10 by the voltage divider R_3 and R_4 as shown in Figure 4-9 the reference voltage is below 2.5 V. This is remedied by lowering the value of R_1 in Figure 4-10, which increases the reverse current through the reference diode.

4.3.4 ADC Control and Parallel to Serial Conversion

An Erasable Programmable Logic Device (EPLD) performs the control of the ADC and the parallel to serial conversion. The design of the control logic for the EPLD is performed using Altera Max+PLUS II®. This software package performs both graphical and text based implementation of logic designs into Altera EPLD devices. The graphical design of the control logic for the transmitter unit is discussed in Appendix D.1. The flow diagram describing the ADC control and parallel to serial conversion is shown in Figure 4-11.

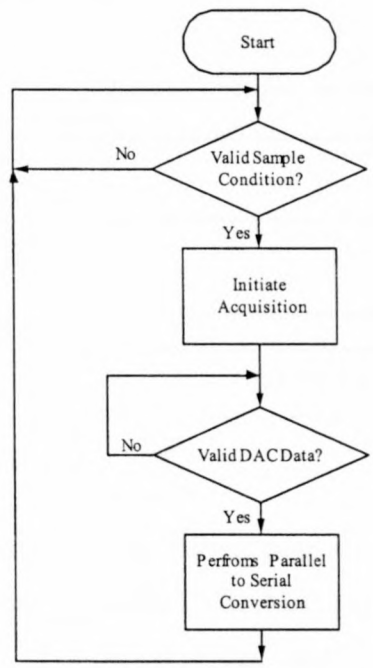

Figure 4-11 Flow diagram of the DAC control and parallel to serial conversion.

The control interface to the ADC is shown in Figure 4-12. The control line /CONVST is used to initiate a conversion cycle. The BUSY signal from the ADC indicates that a conversion cycle is in progress and the digital data bus is given by D0-D11. The Tx signal is the serial data and Clk represents the 25 MHz system clock.

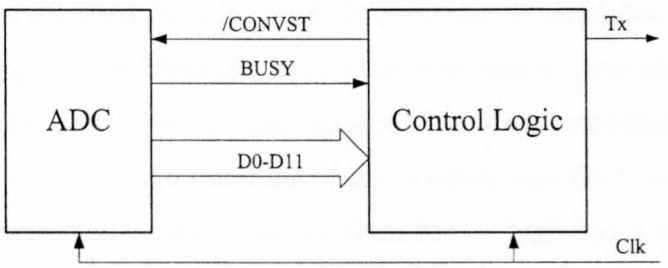

Figure 4-12 Block diagram of the ADC and EPLD.

The ADC uses successive approximation to convert the analog signal to digital data at a rate of 1 MSPS with 12-bit resolution. The timing diagram for the ADC is shown in Figure 4-13 where t_{conv} indicates the conversion time of the ADC and t_{acq} indicates the available time to acquire the data prior to the next conversion cycle. The sample period is indicated by t_{sample} and is equal to 1 µs. D0-D11 indicates the converted digital data on output pins of the ADC.

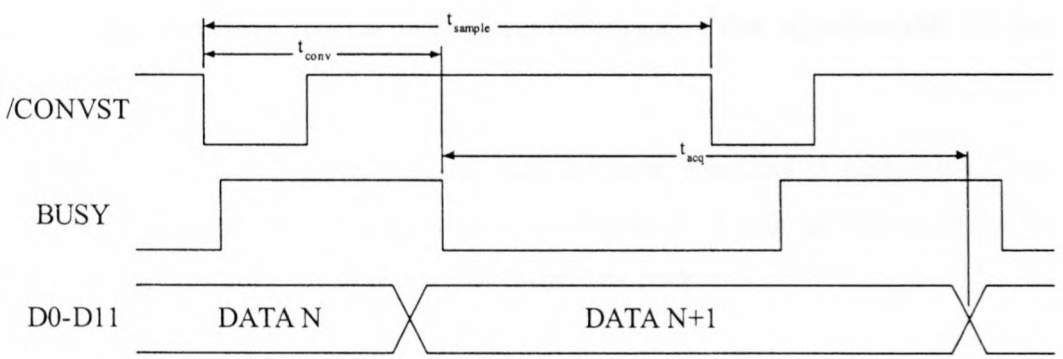

Figure 4-13 Timing diagram of the ADC.

A conversion cycle is initiated by the falling edge of /CONVST after which the BUSY signal of the ADC is pulled high. The ADC performs the conversion using 14 cycles of the CLK signal. The period of CLK is 40 ns, which implies that t_{conv} is equal to 560 ns. After the conversion cycle is complete and the digital data is stable on the output pins D0-D11 the BUSY signal is pulled low to indicate that the conversion is complete.

The digital data remains valid on D0-D11 and is not affected by the /CONVST signal. This is desirable as the digital data can still be acquired on D0-D11 during a conversion cycle initiation.

The parallel data obtained from the ADC is converted to serial data and transmitted without encoding or error checking in order to minimise system complexity, power consumption and cost. Numerous methods of data encoding are available. Manchester encoding uses the transition of levels rather than the levels itself. A logic high will be represented by the transition from low to high and a logic low will be represented by the transition from high to low. This effectively doubles the bit-rate of the system, as two bits are necessary to represent a single un-encoded bit. This type of encoding is relatively easy to implement but requires twice the bandwidth [33, 34].

Other encoding methods such as 4B5B substitute a 5-bit value for every 4 bits of data. This process has less bandwidth requirement but is more complex to implement as it uses mostly a lookup table to provide the 5-bit substitutions [33, 34].

The implementation of encoding methods involves a compromise between the bit-rate and the level of complexity. Commercial devices that perform encoding and error checking are expensive and has high power consumption that is undesirable for this application.

The data is transmitted asynchronously and no error checking is performed. The structure of the serial data packet is shown in Figure 4-14 with t_{bit} indicating the bit length and t_{dp} indicating the length of the entire data packet.

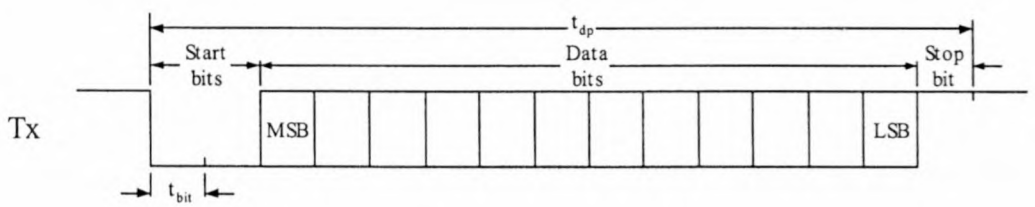

Figure 4-14 Structure of the serial data packet.

The structure of the data packet is similar to that of standard serial communication protocols. The data packet consists of two start bits followed by the 12 data bits and terminated by a single stop bit. The most significant bit (MSB) is transmitted first and the least significant bit (LSB) last.

The generation of the serial data is implemented in an EPLD by means of a shift-register topology. The individual bits of the data packet are clocked from the EPLD on each rising edge of the CLK signal. This implies a bit length t_{bit} of 40 ns, which

results into a total packet length t_{dp} of 600 ns. The design of the shift register is shown in Appendix D.1.

The complete timing diagram of the control logic is shown in Figure 4-15. The time delays t_1 and t_2 are used to indicate that the BUSY signal is asynchronous with respect to the control logic.

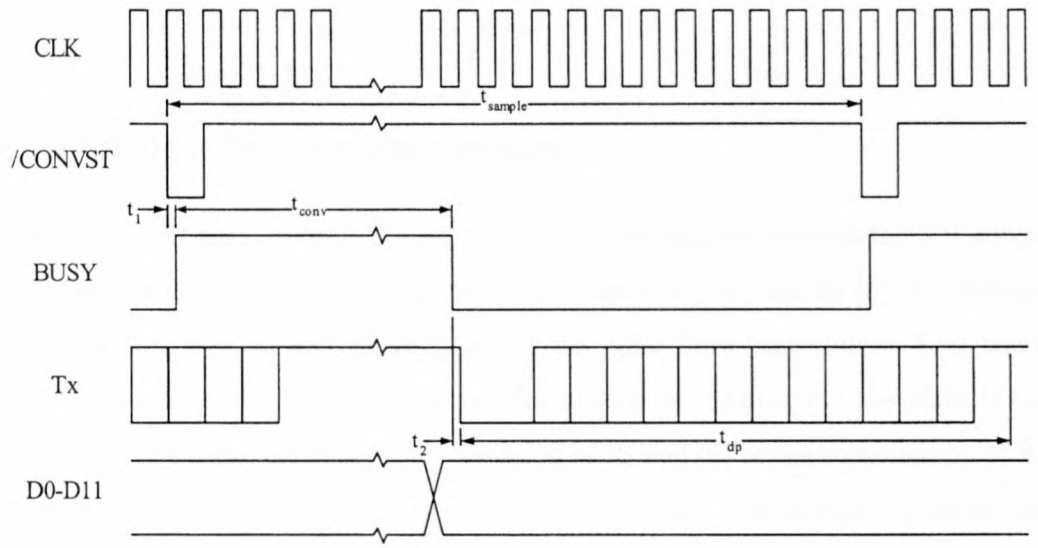

Figure 4-15 Timing diagram of the control logic with the Tx signal included.

It can be seen from Figure 4-15 that the serial data is transmitted while a new conversion sequence is initiated. This is possible, as the digital data on D0-D11 remains valid until a short time before the falling edge of BUSY.

4.3.5 Optic Fibre Transmitter

The serial digital data obtained from the parallel to serial conversion is transmitted with the circuit shown in Figure 4-16 [35]. The resistors R_1, R_2 and R_3 are used to specify the current through the optic fibre transmitter diode. The capacitor C_1 provides a greater turn-on current for the optic fibre transmitter. The 74ACTQ00 is a logic NOT-AND (NAND) package. The output of gates B, C and D are connected to increase the current sink capability of the 74ACTQ00.

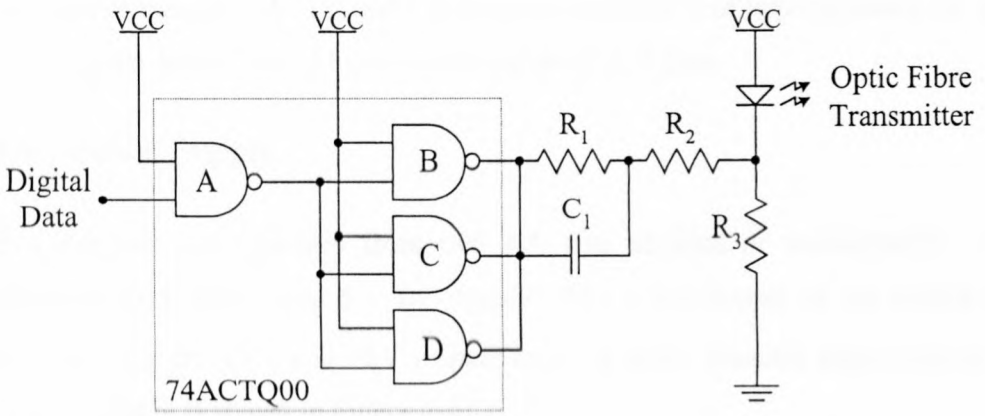

Figure 4-16 Optic fibre transmitter circuitry.

The output of the parallel NAND gate configuration is toggled between the 5 V power supply VCC and ground. In the high state the resistors R_1, R_2 and R_3 forms a voltage divider causing a small voltage drop across the optic fibre transmitter. This small voltage biases the optic fibre transmitter prior to turn-on. During the low state of the parallel NAND output the parallel combination of R_3 and the series combination of R_1 and R_2 sinks current through the optic fibre transmitter. The design equations for resistors R_1, R_2 and R_3 are given in equations (4-18), (4-19) and (4-20) respectively.

$$R_1 = \frac{R_3}{2B} \tag{4-18}$$

$$R_2 = \frac{R_3}{2B} - \frac{3}{N} \tag{4-19}$$

$$R_3 = \frac{(V_{cc} - V_f)(1+B)}{I_f} \tag{4-20}$$

In equation (4-18) B represents an empirically constant that establishes an optimum relationship between the pre-bias and the forward current I_f and N represents the amount of parallel NAND gates. V_f represents the forward voltage of the optical fibre transmitter diode. The values of the resistors and the capacitor are given in equation (4-21).

$$R_1 = 33\,\Omega,\ R_2 = 33\,\Omega,\ R_3 = 270\Omega \text{ and } C_1 = 75\ pF \tag{4-21}$$

The values of equation (4-21) results in a forward current I_f of approximately 60 mA. The associated optical power has a typical value of 18.8 dBm.

4.3.6 Power Supply

The transmitter unit operates from two AA size alkaline or rechargeable 1.2 V batteries or from an external 5 V DC supply. The power supply of the analog and digital circuitry are ±5 V and +5V respectively. A block diagram representation of the power supply is shown in Figure 4-17.

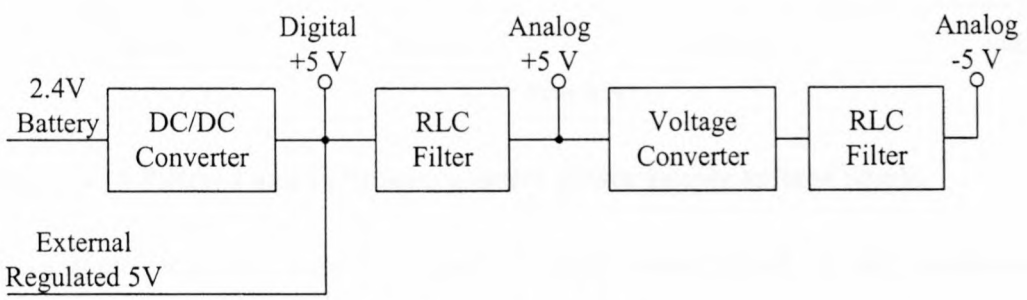

Figure 4-17 Block diagram of the power supply.

The digital +5 V is obtained by means of a commercial micro-power step-up DC/DC converter [36]. The DC/DC converter is capable of delivering 5 V at 200 mA from a 2.4 V input. The DC/DC converter employs a Burst Mode ™ topology, which results in high efficiency [36].

The RLC filter attenuates the high frequency ripple present in the output voltage of the DC/DC converter. The filtered +5 V is used to power the analog circuitry, while the unfiltered +5 V is used for the less sensitive digital circuitry. This reduces the size and power requirement of the RLC filter. The filtered and unfiltered positive power supply voltage ripple is shown in Figure 4-18.

The negative 5 V power supply is generated using a switched capacitor voltage converter [37]. The switched capacitor voltage converter generates the negative power supply voltage by storing charge in a capacitor and then transferring it to another capacitor, which is referenced in order to produce a negative voltage. The transfer of charge from one capacitor to another generates high frequency currents, which results in high frequency voltage transients due to stray inductance in the circuit.

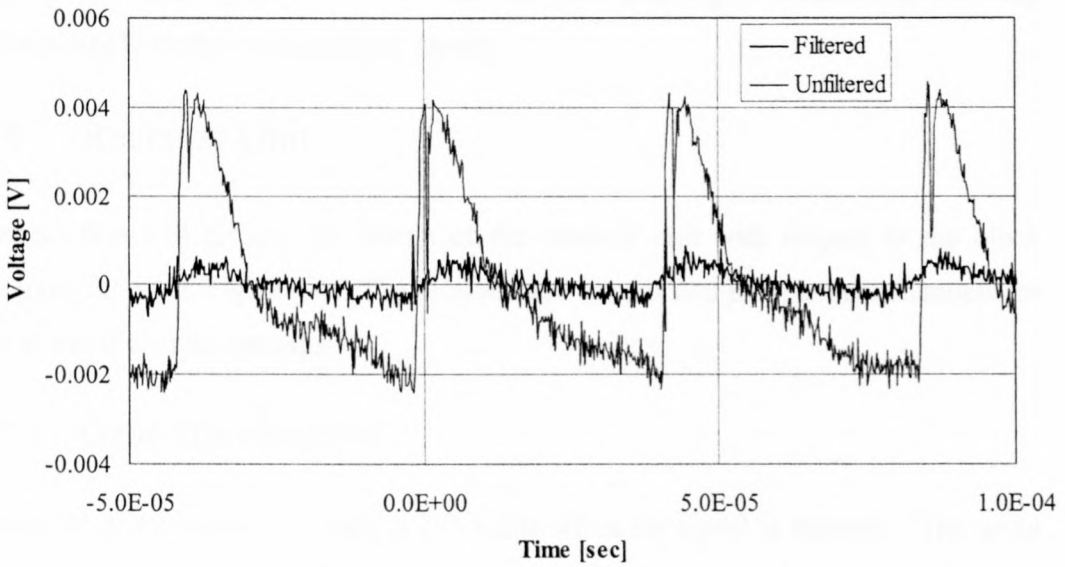

Figure 4-18 Filtered and unfiltered positive power supply voltage ripple.

These high frequency transients couple to the output signal of the operational amplifiers through the stray capacitances present in the device. These transients are reduced by filtering the output voltage of the voltage converter as indicated in Figure 4-17 and by minimising track length in order to reduce stray inductance. The voltage ripple of the analog negative power supply is shown in Figure 4-19.

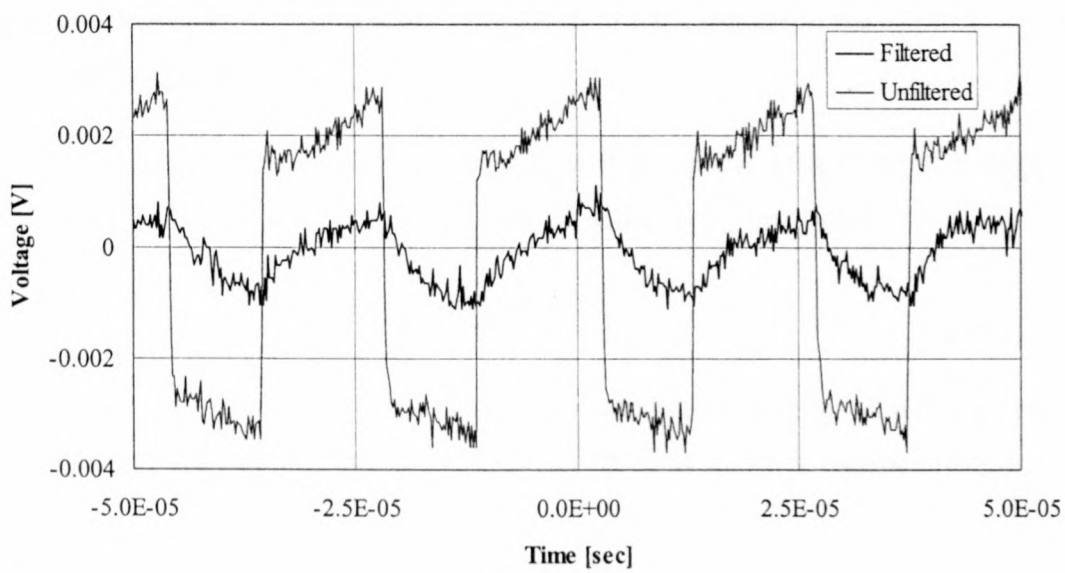

Figure 4-19 Filtered and unfiltered negative power supply voltage ripple.

Figure 4-18 and Figure 4-19 show that the RLC filtering is effective in reducing voltage ripple on the analog power supply.

4.4 Receiver Unit

This section will discuss the design of the receiver unit with respect to the block diagram shown in Figure 4-1. The receiver unit houses two independent channels for use in multi channel systems.

4.4.1 Optic Fibre Receiver

The optic fibre receiver outputs a DC value when no signal is applied. The input signal causes the output voltage to decrease with respect to the amount of optical power applied to the optic fibre receiver, which is shown in Figure 4-20.

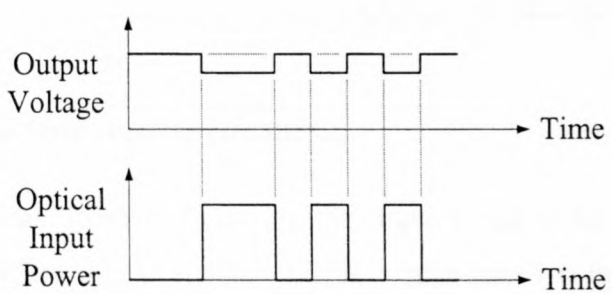

Figure 4-20 Output voltage of optic fibre receiver with respect to the applied optical input power.

The relation given in equation (4-22) calculates the response of the output voltage given the optical input power P_r [μW] and the responsivity R_p [mV/μW].

$$v_o = V_{no\ signal} - (P_r R_p) \tag{4-22}$$

The optical power of the optic fibre transmitter at a forward current of 60 mA is given as -18.8 dBm. The resulting output power is calculated as shown in equation (4-23).

$$P_{r(dBm)} = 10Log_{10}\left(\frac{P_r[\mu W]}{1000[\mu W]}\right) = -18.8\ dBm$$

$$P_r = 13.182\ \mu W \tag{4-23}$$

The given responsivity of the optic fibre receiver is given as 7 mV/μW, which results in a maximum dynamic response of 92.2 mV. The optic fibre cable attenuates the signal to some extent but can be neglected when operating across short distances.

The receiver circuitry for the optic fibre receiver is shown in Figure 4-21 [35].

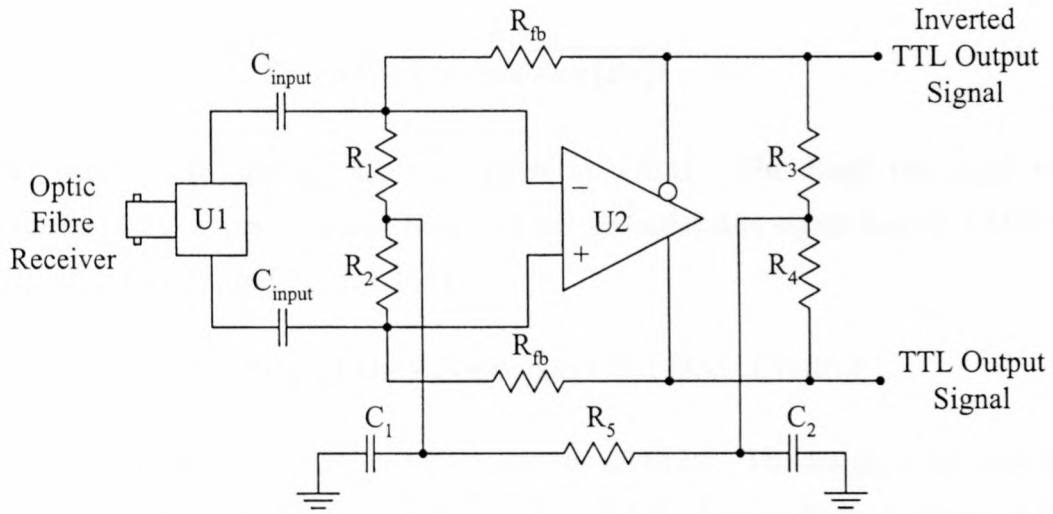

Figure 4-21 Optic fibre receiver circuitry.

The circuit shown in Figure 4-21 converts the output signal of the optic fibre receiver to a TTL compatible digital signal. U2 is a high-speed comparator capable of transition speeds of less than 10 ns.

The operation of the circuit shown in Figure 4-21 is based upon the fact that the signal has a minimum fundamental frequency. Encoding of the signal ensures a minimum fundamental frequency. Without encoding the fundamental frequency is dependent on the state of the 12 data bits. Figure 4-22 indicates a special case with all 12 data bits in the high state.

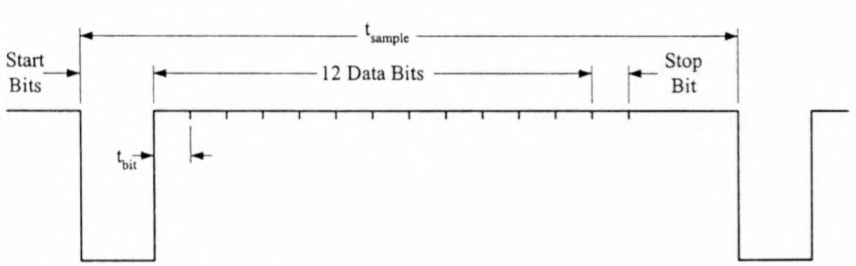

Figure 4-22 Serial data with all twelve data bits high.

Figure 4-22 shows that although the Baud rate is given by the inverse of t_{bit}, the fundamental frequency of the serial data is the inverse of the sample time t_{sample}. This is the lowest fundamental frequency that the serial signal will achieve. The input capacitance shown in Figure 4-21 is calculated with the relation shown in equation (4-24) [35].

$$C_{input} = \frac{2}{3(R_1 + R_2)(Data\ Rate[Bd])} \tag{4-24}$$

The value of R_1 and R_2 are both given as 270 Ω. The Baud rate used in equation (4-24) is the minimum Baud rate for the serial data signal namely 1 MHz. The resulting value of C_{input} is 1.234 nF.

4.4.2 Serial-to-Parallel Data Conversion and DAC Control

The serial to parallel conversion is performed by an EPLD. The design of the control logic for the receiver circuit using Altera Max+PLUS II® is shown in Appendix D.2. The flow diagram of the serial to parallel conversion routine is shown in Figure 4-23. The serial to parallel conversion is initiated by the detection of a valid start-bit. The data bits following the start-bit are sequentially sampled and upon detection of a valid stop bit written to the parallel data buffer.

The serial detection routine employs a hold-off function similar to the trigger hold-off found in digital oscilloscopes. The hold-off function is used to synchronise the detection routine to the asynchronous serial data. Upon detection of an invalid stop bit the detection routine stops monitoring of the serial signal for a preset time period, which is less than t_{sample} shown in Figure 4-22. Numerous repetitions of this process results in location of the start-bit position. Once this has been accomplished the detection routine is synchronised to the serial data signal. The hold-off function is usually performed at device power up and when a break in transmission has occurred. The timing diagram of the serial data detection sequence is shown in Figure 4-24.

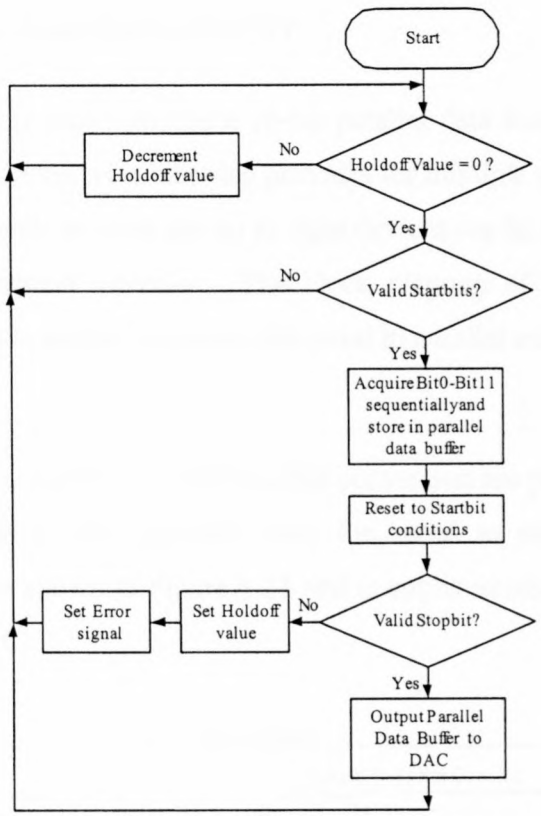

Figure 4-23 Flow diagram of the serial to parallel conversion.

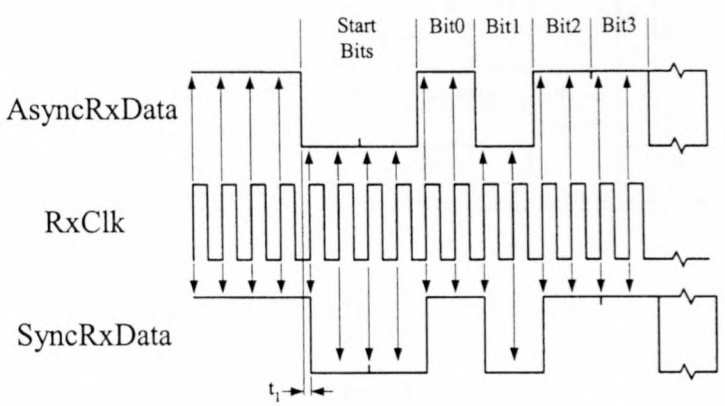

Figure 4-24 Timing diagram of the serial data detection sequence.

The detection of the received optic fibre signal AsyncRxData is asynchronous with respect to the receiver unit. The receiver unit uses a system clock frequency RxClk, which is twice the clock frequency employed in the transmitter unit. AsyncRxData is therefore sampled twice during each bit to increase reliability. The SyncRxData signal is a synchronised version of AsyncRxData with respect to the receiver clock and is hence used for the serial to parallel conversion instead of AsyncRxData. The time shift between AsyncRxData and SyncRxData is indicated in Figure 4-24 by t_1.

4.4.3 Data Acquisition Output Buffer

The optic fibre receiver unit provides a 16-bit parallel data bus to an external data acquisition system. The receiver unit also provides for multiple channels as it houses two independent channels per unit and up to eight devices can be paralleled to provide a 16-channel measurement interface. The block diagram of the interface to the external data acquisition system including the serial to parallel conversion is shown in Figure 4-25.

The data bus controller and the serial to parallel conversion are performed together in the EPLD. The digital data obtained from the serial to parallel conversion is contained in RxBuf as shown in Figure 4-25 and is continuously fed to the digital to analog converter (DAC).

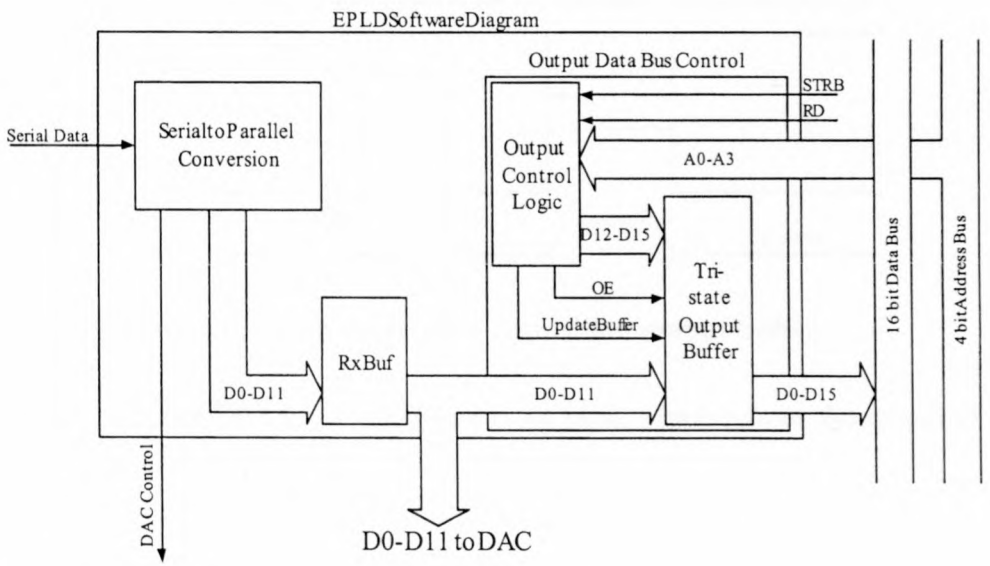

Figure 4-25 Block diagram of data bus interface.

Data bits D0-D11 of the 16-bit data bus is represented by the 12-bit parallel data obtained from the serial to parallel conversion. Bits D12-D15 is reserved bits and can be used for channel identification purposes. The 4-bit address bus A0-A3 contains the channel address and is used together with the control signals /STRB and /RD during the data acquisition process.

The timing diagram of the data acquisition output buffer is shown in Figure 4-26. Upon reception of a valid stop bit the contents of RxBuf is updated with new parallel

data. The /STRB input is synchronised with the system clock to produce the /SyncSTRB signal. The falling edge of /SyncSTRB loads the current value of RxBuf into the tri-state output buffer. The output control logic monitors the address line A0-A3 and upon detection of a valid channel address and the low state of /RD the OE signal changes D0-D15 from a high impedance state to the previously loaded parallel data.

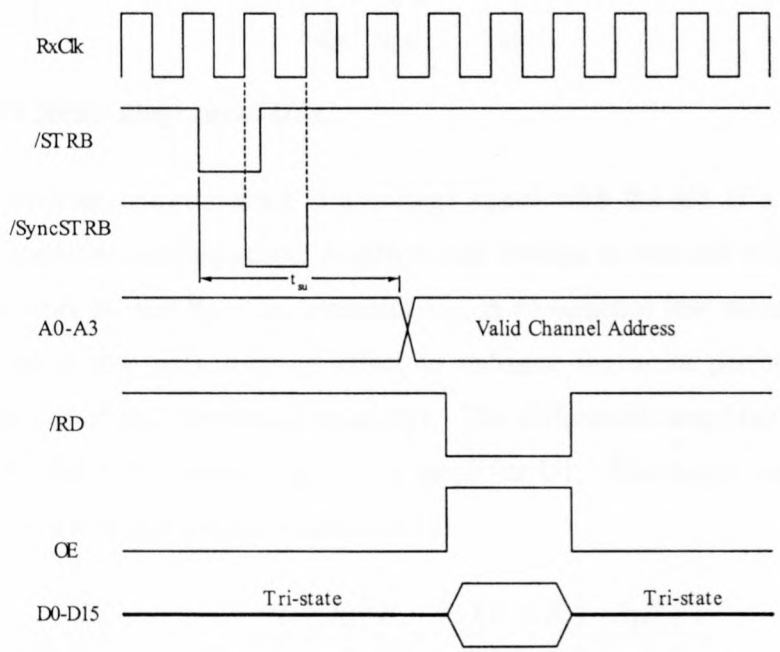

Figure 4-26 Timing diagram of the data acquisition output buffer.

After acquisition of D0-D15 the /RD line is set high, which returns the output of the output buffer to tri-state.

4.4.4 Digital-to-Analog Conversion

The receiver unit features an analog output signal for monitoring purposes, which is achieved with the aid of a high-speed current output DAC. The current output of the DAC is converted to a voltage signal with a differential operational amplifier configuration as shown in Figure 4-27.

The 12-bit parallel data is applied to the DAC and a conversion is initiated by the rising edge of DacClk. The output currents of the DAC I_{outA} and I_{outB} are complimentary to each other. The full-scale value of the output current is determined by the value of I_{ref} and can be adjusted from 2 mA to 20 mA.

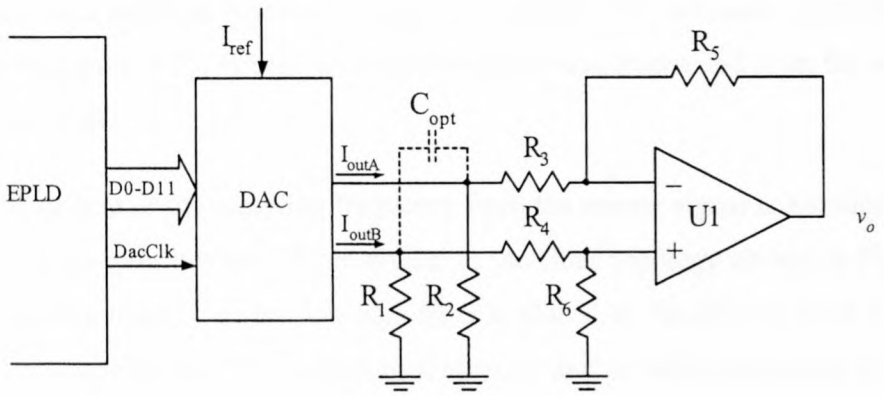

Figure 4-27 Circuit diagram of DAC.

The output currents are converted to a voltage signal with the aid of a differential operational amplifier configuration. A differential voltage is obtained with the aid of two load resistors R_1 and R_2. The capacitor C_{opt} is an optional low valued capacitor and introduces a low pass filtering effect to enhance the noise performance and improve stability of the operational amplifier. The differential amplifier consists of R_3, R_4, R_5, R_6 and a high-speed operational amplifier U1. The output voltage of the operational amplifier is given in equation (4-25).

$$v_o = -I_{outA}\frac{R_1 R_5}{R_1 + R_3} + I_{outB}\frac{R_2 R_4 R_6\left[(R_3 + R_5)(R_1 + R_3) - R_5 R_1\right]}{R_3(R_1 + R_3)\left[(R_4 + R_6)(R_2 + R_4) - R_2 R_6\right]} \qquad (4\text{-}25)$$

The full-scale value of the output current is 20 mA and the associated full-scale output voltage of the operational amplifier is ±1 V. The coefficients of I_{outA} and I_{outB} are therefore equal to 50. The mismatch of resistor values affects the common mode rejection ratio of the configuration shown in Figure 4-27. The resistor values to achieve the desired gain are shown in equation (4-26).

$$R_1 = R_2 = 25\,\Omega,\ R_3 = R_4 = 225\,\Omega \text{ and } R_5 = R_6 = 500\,\Omega \qquad (4\text{-}26)$$

4.4.5 Low-Pass Filter and Gain Stage

The reconstruction of the analog signal introduces high frequency noise due to the sampling frequency [20]. At lower frequencies the noise caused by the reconstruction process is less than at higher frequencies. At lower frequency minor transitional oscillations occur at the output of the operational amplifier due to the low slew rate of the analog signal. At higher frequency the amplitude of the oscillations increase as

the step value increase from one sample to the next. The optional capacitor C_{opt} (as shown in Figure 4-27) is used to minimise these oscillations and is in the order of a few pico farad.

The attenuation of the sampling frequency from the analog signal is accomplished by using a unity gain low-pass filter similar to the filter topology shown in Figure 4-5. The cut-off frequency of the low-pass filter is placed at 700 kHz in order to provide sufficient attenuation at the sampling frequency and to minimise phase shift in the pass-band.

The filter is implemented by using the Bessel Thompson polynomial in the denominator of equation (4-6). The design procedure is similar to section 4.3.2 with the cut-off frequency placed at 700 kHz. The normalised capacitor values are therefore determined by using equations (4-10) and (4-11) as shown in equations (4-27) and (4-28) respectively.

$$C_1 = \frac{(0.66)(1.732)}{2\pi 700k} = 259.9\,nF \tag{4-27}$$

$$C_2 = \frac{(0.5)(1.732)}{2\pi 700k} = 196.8\,nF \tag{4-28}$$

The impedance scale factor is determined by using equation (4-12) substituted with the normalised values shown in equation (4-27). The resistor and capacitor values after impedance scaling are given in equations (4-29) and (4-30) respectively.

$$R_1 = R_2 = 552.97\,\Omega \approx 560\,\Omega \tag{4-29}$$

$$C_1 = 470\ pF \text{ and } C_2 = \frac{196.8\,nF}{552.97} = 355.8\ pF \approx 330\ pF \tag{4-30}$$

As mentioned in section 4.3.2 the Bessel Thompson polynomial has a slow frequency response but exhibits a constant group delay throughout the pass-band. The amplitude response of the low-pass filter is shown in Figure 4-28 and the phase response and group delay in Figure 4-29.

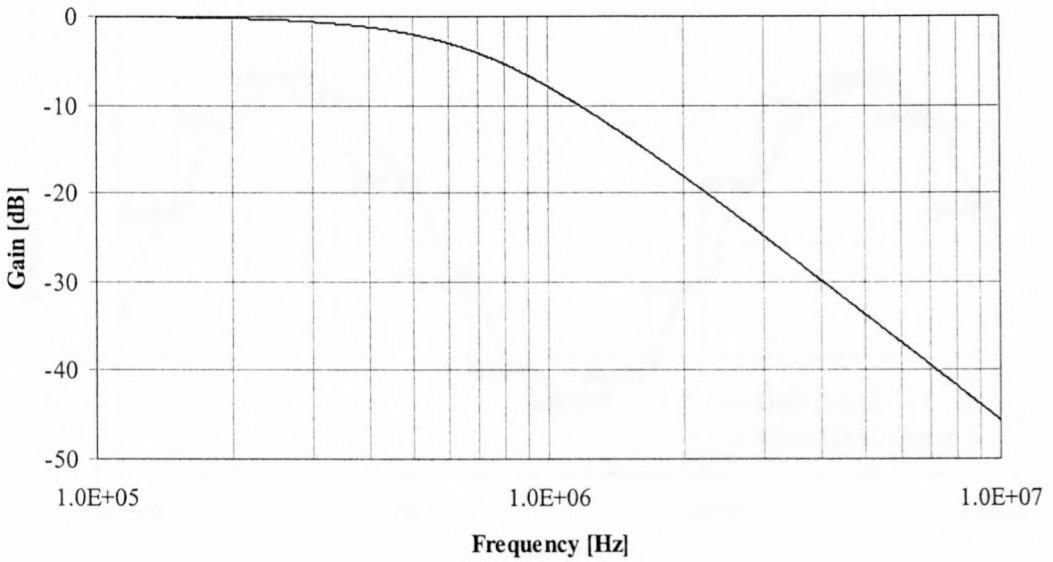

Figure 4-28 Gain response of the reconstruction low-pass filter.

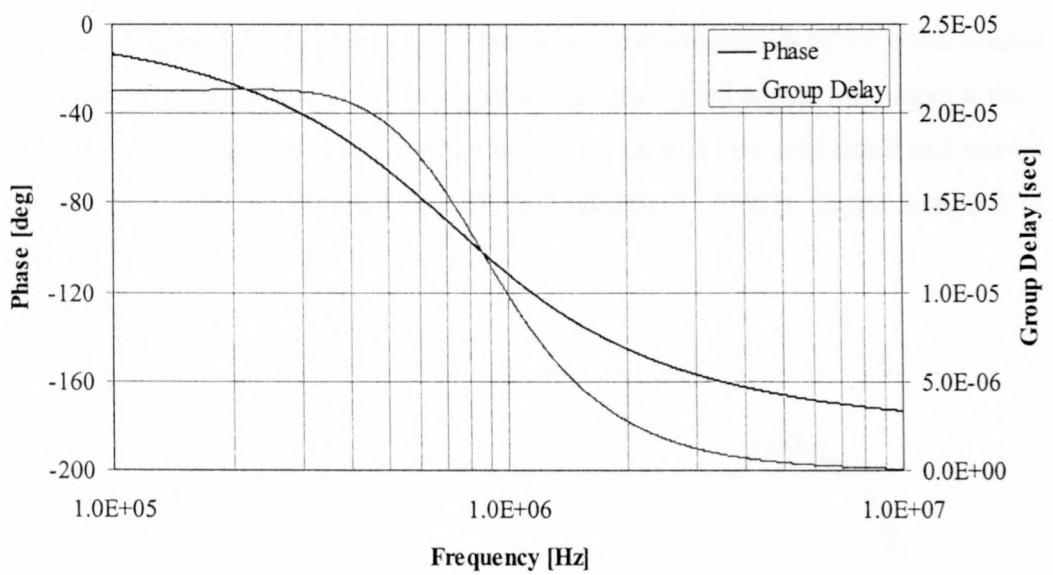

Figure 4-29 Phase response and group delay of the low-pass filter.

It can be seen from Figure 4-29 that the group delay for the low pass filter is constant well beyond 100 kHz, which is desirable for this application.

The unfiltered and filtered DAC output signal is shown in Figure 4-30, which shows a 100 kHz sinusoid sampled at 1 MSPS.

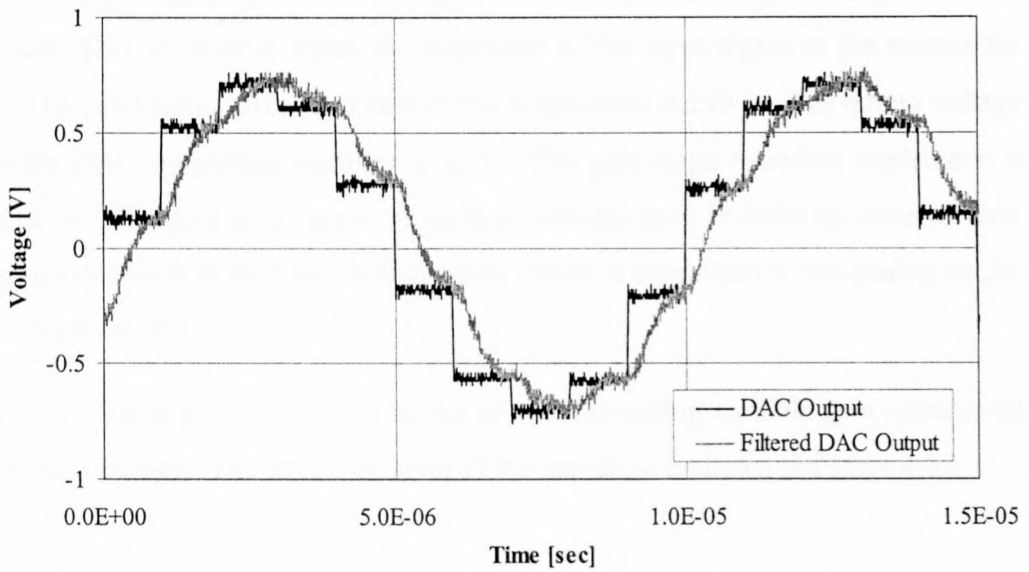

Figure 4-30 Filtered and unfiltered 100 kHz signal sampled at 1 MSPS.

As mentioned earlier the reconstruction of higher frequency signals introduces noise as shown in Figure 4-30. The filtered signal shows the attenuation of the noise caused by the reconstruction process. Filtering of the reconstructed signal introduces a time shift as shown in Figure 4-30. The amount of time shift is however small and can be neglected as shown in Figure 4-31, which indicates a 20 kHz signal sampled at 1 MSPS.

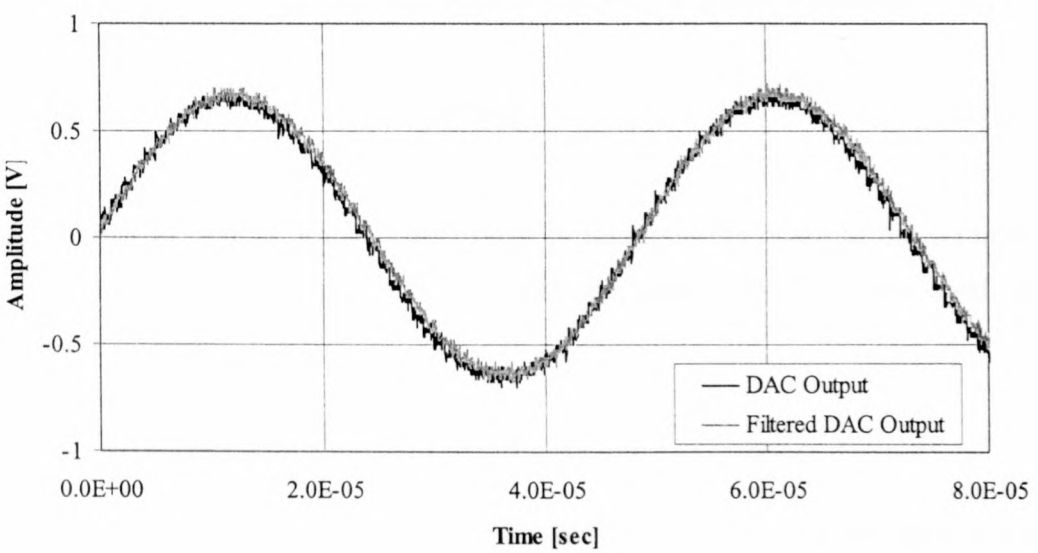

Figure 4-31 Filtered and unfiltered 20 kHz signal sampled at 1 MSPS.

The gain stage following the filter stage is used to scale the output voltage from the low pass filter in order to equal the amplitude of the input signal at the transmitter unit. The input signal to the transmitter unit is specified at ±10 V. The output voltage from the DAC supporting circuitry is ±1 V. The gain stage therefore implements a gain of 10. The gain stage is also capable of variable gain in order to accommodate other devices such as data acquisition cards, which is connected to the analog output of the receiver unit.

The gain stage is implemented by means of a non-inverting variable gain operational amplifier topology. The circuit diagram of this topology is shown in Figure 4-32.

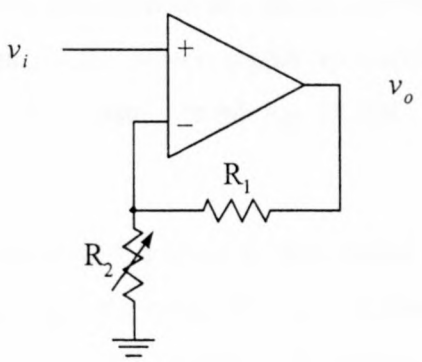

Figure 4-32 Circuit diagram of the gain stage.

The transfer function of the circuit shown in Figure 4-32 is given in equation (4-31).

$$v_o = v_i\left(1+\frac{R_1}{R_2}\right) \tag{4-31}$$

The values of R_1 and R_2 are chosen in order to minimise the effect of the common mode input capacitance of the operational amplifier, which is discussed in section 4.3.3.

4.5 Summary

This chapter presented the design of the optically isolated link. An overview of the isolated link is given in section 4.2 with respect to the block diagram shown in Figure 4-1. The design of the transmitter and receiver units are discussed in sections 4.3 and 4.4 respectively.

The design of the transmitter unit is presented with respect to the analog signal conditioning prior to digitisation and serial data transmission. The analog signal conditioning, which is discussed in sections 4.3.1 and 4.3.2 and involves buffering and filtering of the input signal for interface to standard signal transducers and to establish a low-pass frequency response for anti-aliasing purposes.

The digitisation of the analog signal is discussed in sections 4.3.3. The parallel-to-serial conversion of the digitised data is discussed in section 4.3.4 and involves the implementation of a shift register in order to create an asynchronous serial data sequence. Employing an Electrically Programmable Logic Device (EPLD) performs the hardware implementation of the parallel-to-serial conversion. The serial data is interfaced to the optical fibre by means of an optical transmitter, which is discussed in section 4.3.5. The design of the power supply is discussed in section 4.3.6 and provides insight into practical issues involving DC/DC converters and switched capacitor voltage converters.

The receiver unit is discussed with respect to the optical fibre receiver, serial data detection and digital-to-analog conversion. The optical fibre receiver is discussed in section 4.4.1 and presents a dynamic topology for reception of optic fibre signals. The asynchronous data detection and serial-to-parallel conversion is discussed in section 4.4.2, which is hardware implemented using an EPLD. Section 4.4.3 discusses the data acquisition output buffer. The digital-to-analog conversion and subsequent analog signal conditioning are discussed in sections 4.4.4 and 4.4.5 respectively.

Chapter 5

Data Acquisition System

5.1 Introduction

Due to the unpredictable nature of transient conditions on transmission lines the need arises for a data acquisition system capable of unattended monitoring and logging transient waveforms. The monitoring and logging of transient waveforms is performed on a continuous basis and over extended periods of time in order to establish a transient waveform database. This is particularly useful in determining the frequency and severity of over-voltage conditions on substation equipment.

5.2 Overview

The proposed data acquisition system must be capable of detecting a transient condition upon which the relevant data is recorded. The system is also required to provide time stamping information for the acquired transient waveforms, which provides a means of correlation between system events and the recorded data.

The block diagram describing the data acquisition system is shown in Figure 5-1.

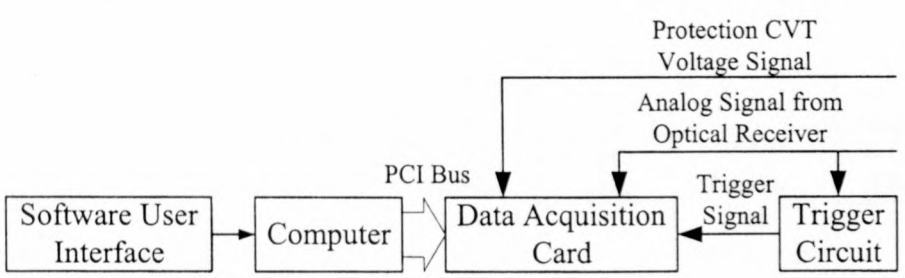

Figure 5-1 Block diagram of the data acquisition system.

The data acquisition system comprises a commercially available dual channel computer based data acquisition card controlled by a software user interface [38, 44]. The data acquisition card acquires both the protection CVT secondary phase voltage and the integrated current signals. A hardware trigger signal to the data acquisition card is generated by the analog trigger circuitry under transient conditions.

The optical isolated link described in chapter 4 performs the digitising process at a rate of 1 MSPS with a resolution of twelve bits. The NI 5102 data acquisition card used in the project is capable digitising rates of up to 20 MSPS but with a resolution of only eight bits. The motivation for this is that commercial data acquisition devices with both high-speed sampling capability and high resolution are extremely expensive. The aim of this research is to establish whether the summation and integration technique is viable, which is comfortably supported by the NI 5102.

5.3 Acquisition of the CVT Secondary Phase Voltage

The acquisition of the protection CVT secondary phase voltage signal is essential as it represents the fundamental frequency of the system. As mentioned in section 3.7 the fundamental frequency is attenuated in order to avoid saturation of the summation and integration circuitry. During the post-processing evaluation the integrated current signal is superimposed on the measured CVT signal to produce the resultant transmission line voltage.

The interface between the protection CVT secondary phase voltage and the data acquisition device is shown in Figure 5-2. R_1 and R_2 represent a voltage divider for interface to the optical fibre transmitter. The signal obtained from the optical fibre receiver is applied to channel 2 of the NI5102.

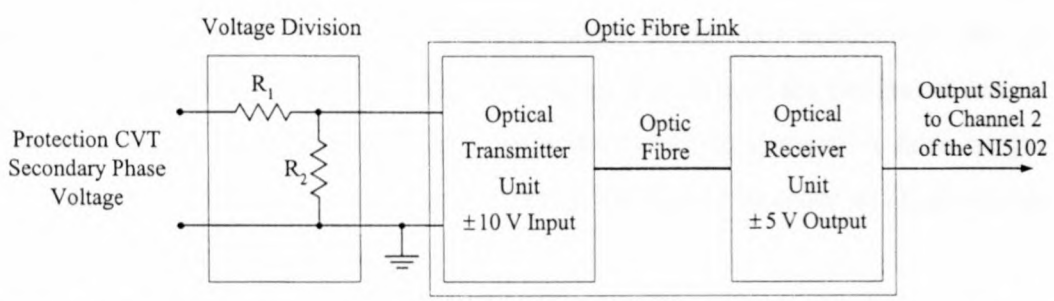

Figure 5-2 Interface between the protection CVT secondary phase voltage and the data acquisition device.

The input to output ratio of the protection CVT is 400 kV/110 V with respect to the line values, which amounts to a gain of 275×10^{-6}. The peak value of the CVT secondary phase voltage is calculated as shown in equation (5-1).

$$V_{phase\ peak} = \frac{110}{\sqrt{3}}\sqrt{2} = 89.814\ \text{V} \tag{5-1}$$

The input range of the optical fibre transmitter is ±10 V. The desired gain of the voltage divider is determined as shown in equation (5-2). V_{tx} gives the input range of the optical transmitter and K_{hr} the headroom factor to allow the CVT secondary phase voltage to exceed the rated value without saturation of the optical transmitter.

$$G_{div} = \frac{V_{tx}}{V_{phase\ peak}K_{hr}} = \frac{10}{(89.814)(2)} = 0.05567 \tag{5-2}$$

The values of R_1 and R_2 are chosen to minimise the burden on the CVT secondary phase voltage. The values of R_1 and R_2 are set to 910 kΩ and 47 kΩ respectively and the resultant value for G_{div} is shown in equation (5-3).

$$G_{div} = \frac{R_2}{R_1 + R_2} = \frac{27\times10^3}{(470\times10^3)+(27\times10^3)} = 0.04911 \tag{5-3}$$

The value of equation (5-3) closely approximates the desired value shown in (5-2). The resistor divider shown in Figure 5-2 is left uncompensated as result of the narrow bandwidth of the CVT.

5.4 Analog Trigger Circuit

The generation of the trigger signal to the data acquisition card is done by means of an analog circuit of which the block diagram is shown in Figure 5-3. The function of the analog trigger circuit is to provide a trigger signal to the data acquisition card on detection of a transient condition. The low frequency content of the integrated current signal is however substantial and may cause the circuit to generate a false trigger condition. For this reason a band-pass filter is introduced in order to attenuate the undesired frequency components.

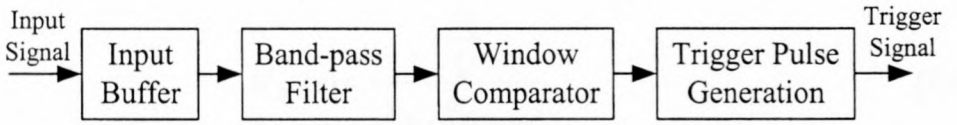

Figure 5-3 Block diagram of the analog trigger circuit.

5.4.1 Input buffer

The trigger circuit is interfaced to the input signal source by means of a voltage follower operational amplifier configuration as shown in Figure 5-4.

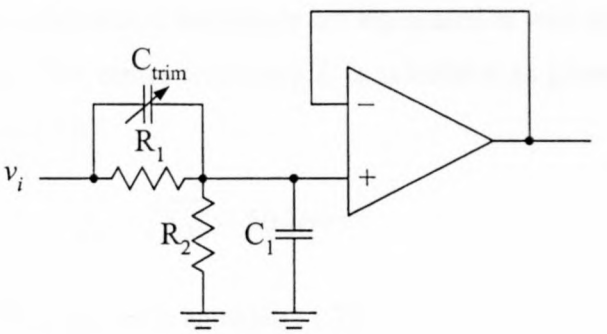

Figure 5-4 Input buffer of the analog trigger circuitry.

The voltage divider consisting of C_{trim}, R_1, R_2 and C_1 provides a versatile interface to various signal sources. The operation of the voltage divider is discussed in detail in section 4.3.1. In the desired frequency band the input impedance of the circuit shown in Figure 5-4 is effectively the series combination of resistors R_1 and R_2 due to the high input impedance of the voltage follower operational amplifier topology. The input impedance decreases with an increase in frequency, which is outside of the desired frequency range.

5.4.2 Band-pass Filter

As mentioned earlier the trigger circuit generates a trigger signal to the data acquisition card under transient conditions. A band-pass filter is implemented in order to prevent false triggering as result of the system frequency and related harmonics or from high frequency noise present in the system.

The generalised transfer function for the band-pass filter with unity gain is shown in equation (5-4) [26]. The band-pass filter is implemented with a generic biquad topology as shown in Figure 3-9.

$$H_{BP}(s) = \frac{s\frac{\omega_c}{Q}}{s^2 + s\frac{\omega_c}{Q} + \omega_c^2} \tag{5-4}$$

The lower cut-off frequency f_l is set at 5 kHz and the higher cut-off frequency f_h is set at 500 kHz. The resultant bandwidth B is then given by equation (5-5).

$$B = f_h - f_l = 500\,kHz - 5\,kHz = 495\,kHz \tag{5-5}$$

The system frequency and related harmonics are attenuated as well as high frequency noise above 500 kHz. The centre frequency f_c is calculated as given by the relation [27] shown in equation (5-6).

$$f_c = \sqrt{f_l f_h} = 50\,kHz \tag{5-6}$$

The relation for Q [27] is shown in equation (5-7).

$$Q = \frac{f_c}{B} = \frac{50\,kHz}{495\,kHz} = 0.101 \tag{5-7}$$

Upon comparison of equations (3-7) and (5-4) it can be seen that by omitting R_4 and R_5 the transfer function as given in equation (5-8) is obtained.

$$H_{BP}(s) = \frac{s\frac{1}{R_1 C}}{s^2 + s\frac{1}{R_2 C} + \frac{1}{RR_3 C^2}} \tag{5-8}$$

The design procedure selects the values of R and C as 47 kΩ and 68 pF respectively and calculates the remaining component values as shown in equations (5-9) and (5-10).

$$R_1 = R_2 = \frac{Q}{(\omega_c C)} = 4.728\,k\Omega \approx 4.7\,k\Omega \tag{5-9}$$

$$R_3 = \frac{1}{(\omega_c^2 RC^2)} = 21.912\,k\Omega \approx 22\,k\Omega \tag{5-10}$$

The gain response of the band-pass filter is shown in Figure 5-5.

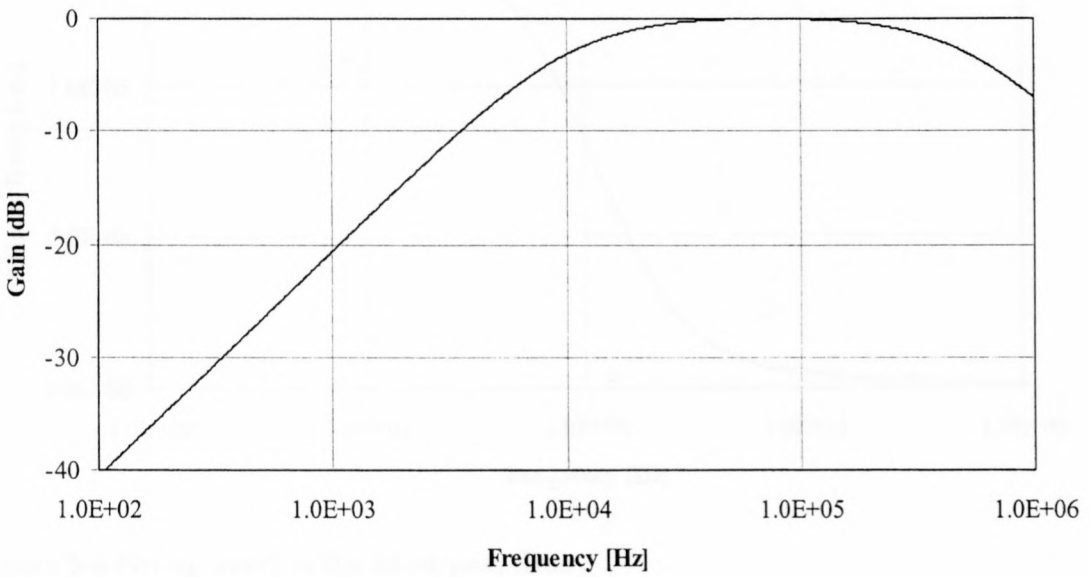

Figure 5-5 Gain response of the band-pass filter.

Figure 5-5 shows the attenuation of the system frequency and related harmonics and the pass-band in which transient components will be passed.

The phase response of the band-pass filter is ignored as only the amplitude response is of interest for trigger generation. The group delay of the band-pass filter is negligible as shown in Figure 5-6.

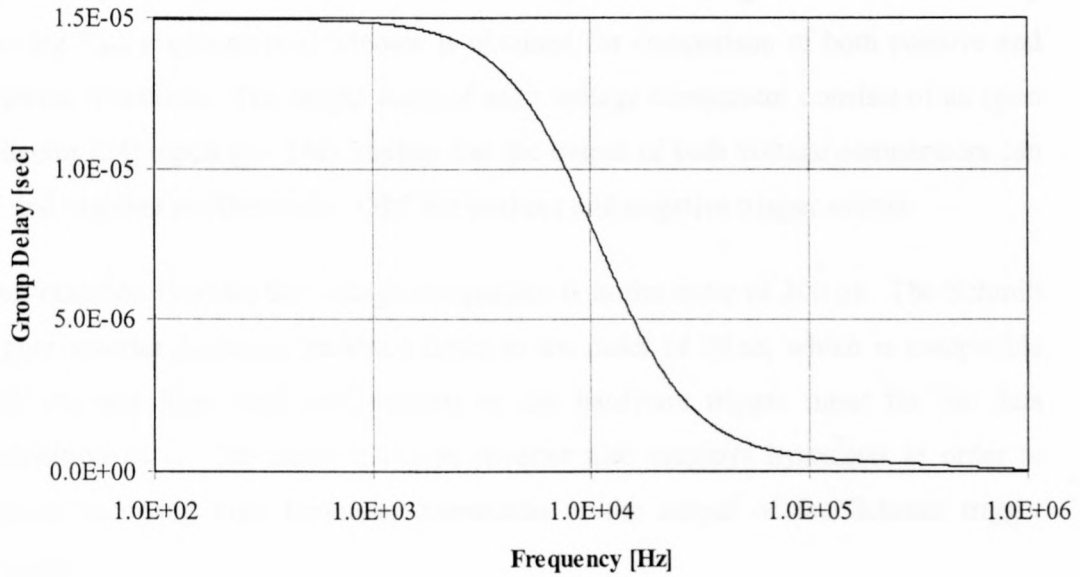

Figure 5-6 Group delay of the band-pass filter.

5.4.3 Window Comparator and Trigger Pulse Generation

The filtered signal is monitored using a window comparator circuit. The circuit diagram is shown in Figure 5-7.

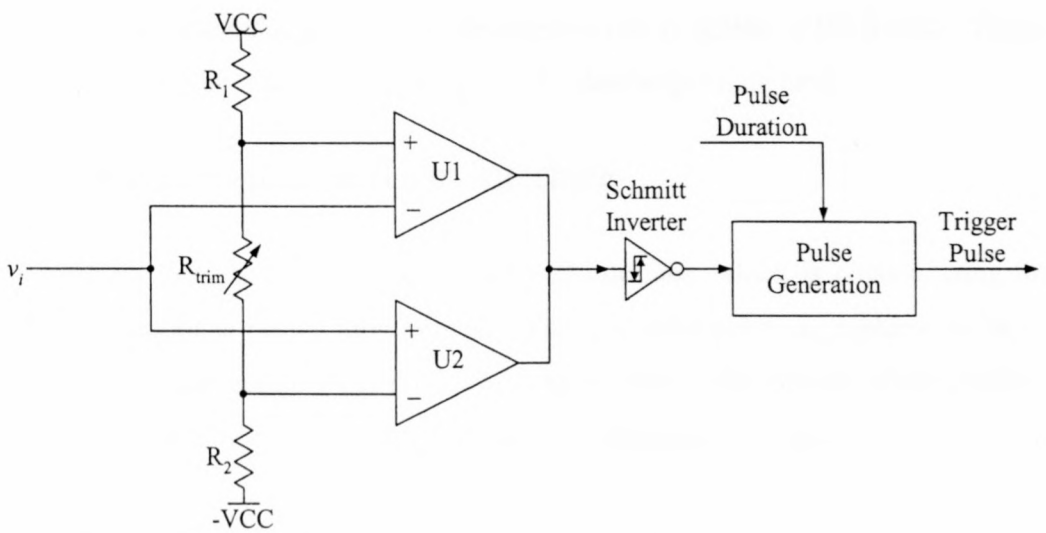

Figure 5-7 Diagram of the trigger generation circuitry.

The window comparator consists of two voltage comparators U1 and U2 configured as shown in Figure 5-7. R_1, R_2, and R_{trim} set the reference voltage levels for the voltage comparators. The positive and negative power supplies are indicated by VCC and –VCC respectively.

R_1 and R_2 are equal valued resistors and inspection of Figure 5-7 shows that by varying R_{trim} a symmetrical window is obtained for comparison of both positive and negative transients. The output stage of each voltage comparator consists of an open collector [24] topology. This implies that the output of both voltage comparators can be tied together to effectively "OR" the positive and negative trigger events.

The transition time for the voltage comparator is in the order of 200 ns. The Schmitt trigger inverter produces transition times in the order of 20 ns, which is compatible with the transition time requirements of the hardware trigger input for the data acquisition card. The Schmitt trigger inverter also employs hysteresis in order to prevent recurring high frequency transitions at the output of the Schmitt trigger inverter.

The hardware trigger input of the data acquisition card specifies a minimum pulse length for the trigger signal. The pulse generation is performed by a commercially available integrated circuit. The pulse length is externally specified by means of a resistor and capacitor combination of which the time constant is variable. The integrated circuit provides a complimentary output for both rising and falling edge trigger signal specifications, which is hardware selectable. The transition time specification of the pulse generation integrated circuit is similar to the Schmitt trigger inverter, which allows for direct interface to the data acquisition card.

5.5 Data Acquisition User Interface

This section presents the data acquisition user interface, which is created using the LabVIEW graphical design environment. The user interface is a graphical software application, which controls the NI 5102. The hardware description of the NI 5102 and the LabVIEW design environment is discussed in Appendix A and B respectively.

The software user interface controls the entire acquisition sequence from initialisation through to management of the acquired data. The acquisition parameters are user configurable, which results in a versatile data acquisition system. The specific requirements of the user interface are as follows:

(i) User configurable acquisition parameters

(ii) Visual feedback on acquisition activities

(iii) Creation of a log file for activity evaluation purposes

User configurable acquisition parameters are essential in order to establish a versatile control application. Visual feedback of the acquisition process is essential in order to assist during installation and in assessing the state of the acquired signal. The creation of a log file is invaluable during post-analysis of transient waveforms. The time and date of each transient condition is saved to file together with error information that may be generated during the acquisition process. The log file also contains the acquisition setup parameters for each acquisition sequence for post-processing purposes. Due to the complexity of the above-mentioned criteria a simplified flow diagram is shown in Figure 5-8.

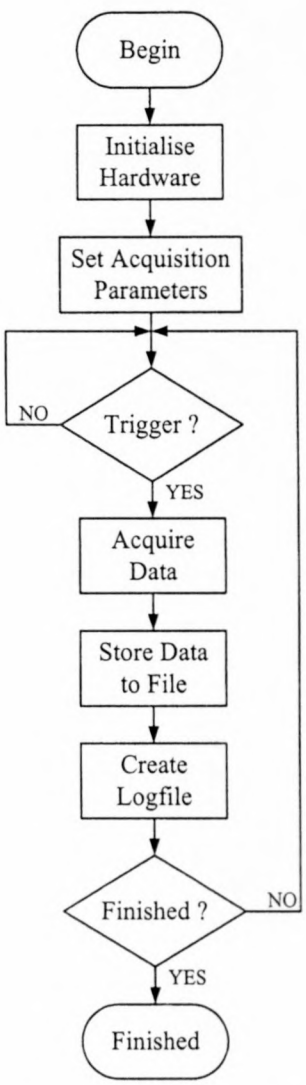

Figure 5-8 Simplified block diagram of the control software for the NI 5102.

The implementation of the control software for the NI 5102 will be discussed with respect to the visual user interface. The diagram implementation of the control software is shown in Appendix B.3.

Figure 5-9 shows the user interface of the NI 5102. The user interface is divided into four sections namely the Operation Mode Setup, Acquisition Setup, File Setup and the Control section.

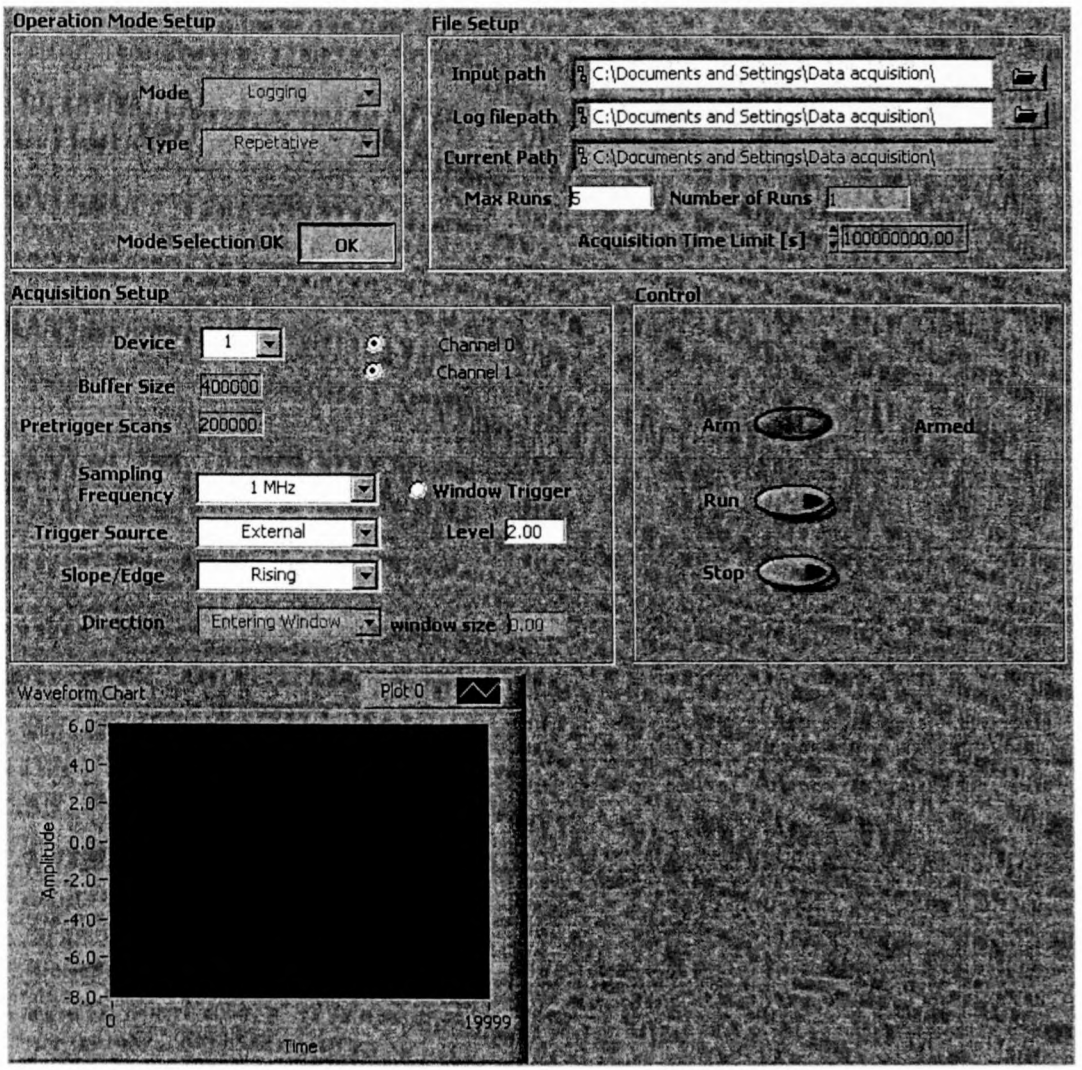

Figure 5-9 User interface of the control software for the NI 5102.

5.5.1 Operation Mode Setup

When the program is first run, only the Operation Mode Setup section is active which suggests that a mode of operation must be selected before continuing. The Operation

Mode Setup section contains two drop-down lists namely Mode and Type of which the functionality is shown in Table 5-1.

Table 5-1 Various Mode and Type selections.

Mode	Type	
Logging	Single	Repetitive
Oscilloscope	Single	Continuous

During logging mode the data sampled by the NI 5102 is saved to file and the waveform chart is updated. Oscilloscope mode of operation only updates the waveform chart and no data is stored to file.

Upon selecting Logging from the Mode drop-down list the user can further select the type of logging from the Type drop-down list. Single Logging mode suggests that upon detection of a trigger condition, one acquisition sequence is performed after which the system returns to the idle state. Repetitive Logging enables multiple acquisition sequences to be performed and is more frequently used than the Single Logging Mode.

During oscilloscope mode no data is saved to file but rather displayed on the waveform chart at the bottom left of Figure 5-9. This proves to be useful in the absence of a portable oscilloscope. The oscilloscope mode consists of two types namely single or continuous mode. Single oscilloscope mode suggests that the display is only updated upon detection of a valid trigger condition. Continuous oscilloscope mode updates the display continuously irrespective of the trigger signal.

5.5.2 Acquisition Setup

Upon selecting the OK button the Operation Mode Setup section becomes inactive and the Acquisition Setup and File Setup becomes active as shown in Figure 5-9. The various acquisition settings for the NI 5102 is shown in Table 5-2.

The triggering options include the trigger source, trigger mode and trigger levels. Edge triggering is assumed when the window-triggering box is unchecked. The user is allowed to select between rising or falling edge. Upon selecting window triggering

the Slope/Edge text box becomes inactive and the user may select whether upon entering or leaving the window a trigger condition should be generated.

Table 5-2 Description of the Acquisition Setup section.

Device	Selection of the desired acquisition device in a multiple device system.
Channel 0	Enables/Disables Channel 0
Channel 1	Enables/Disables Channel 1
Buffer Size	Sets the size of the circular buffer in number of samples
Pretrigger Scans	The amount of samples to be saved and/or displayed prior to the trigger condition. The number of pre-trigger scans must be smaller than the buffer size or else an error will be generated.
Sampling Frequency	Sets the sampling frequency.
Trigger Source	Sets the trigger source to Channel 0, Channel 1 or External
Window Trigger	Enables/Disables Window Triggering
Slope/Edge	Selects rising or falling edge triggering when Window Triggering is disabled.
Level	Sets the desired trigger level.
Direction	Selects Entering or Leaving Window when Window Triggering is enabled.
Window Size	Sets the size of the trigger window when Window Triggering is enabled.

The window size is indicated in the appropriate text box, while the window offset is given by the Level value as shown in Figure 5-10.

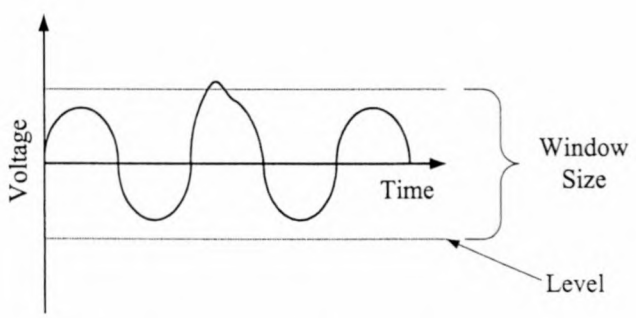

Figure 5-10 Specification of the window size and offset.

5.5.3 File Setup

The File Setup section initialises the file to which the data must be stored and the logfile in which the activities are recorded. After each successful acquisition sequence the data filename is incremented, the data stored and the logfile updated.

The maximum number of acquisition sequences is set by the *Max Runs* and *Number of Runs* gives the number of successful acquisition sequences.

5.5.4 Control Section

The Control section is responsible for initiating the acquisition sequences. The system is first armed, which serves as an indication that all the settings are valid after which the Run button initiates the acquisition sequences. The acquisition sequences will terminate after the final acquisition sequence and return to the Operation Mode Setup section. The acquisition sequence can be terminated by the Stop button after which the system returns to the Operation Mode Setup section.

5.6 Data Format and Extraction

As mentioned earlier the data is sampled at a resolution of eight bits, which results in 256 discrete intervals [20]. The binary data is represented in a two's compliment format [39] to accommodate negative numbers. The data structure into the file is however a sixteen-bit format in which the MSB of the lower byte is extended into the upper byte. This is known as sign extension. The file data structure for acquiring both input channels is shown in Figure 5-11.

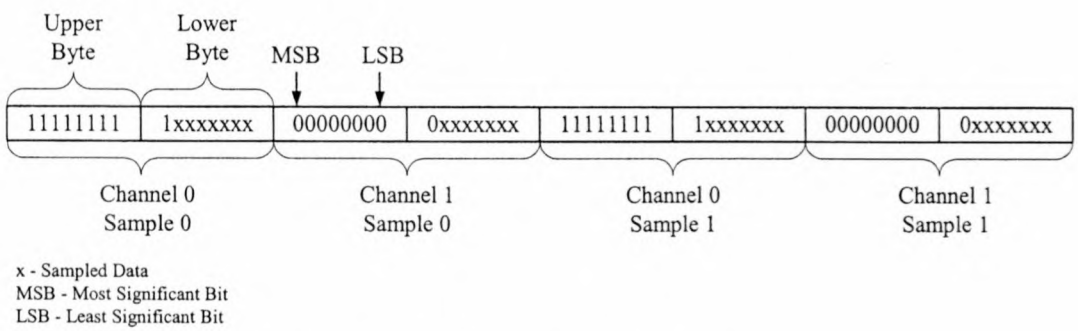

Figure 5-11 Data file structure for both input channels.

The data from the files is extracted by using the MATLAB® environment. MATLAB® enables the extraction and post processing of large amounts of data. The trigger point is obtained from the number of pre-trigger samples as shown in Figure 5-12. The time origin of the sampled data is set to the trigger point. The sample time t_s of each sample is equal to the inverse of the sampling frequency f_s obtained from the log file.

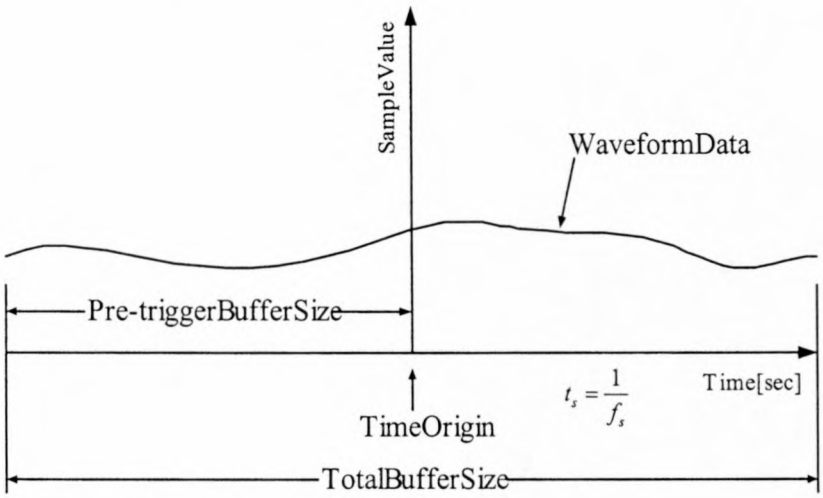

Figure 5-12 Interpretation of the saved waveform data.

The value of each sample is represented by a value ranging from 0 to 127. The eighth bit acts as a sign bit indicating polarity. The scaling of each data sample is calculated as shown in equation (5-11). V_{FS} represents the full-scale value of the optic fibre transmitter input. K_{scale} represents the subsequent scaling factor. The value of K_{scale} scales the acquired sample value in order to obtain the signal value at the input of the optical fibre transmitter.

$$K_{scale} = \frac{V_{FS}}{127} = \frac{10}{127} = 0.07874 \qquad (5\text{-}11)$$

5.7 Summary

This chapter introduced the data acquisition system. An overview of the system is given in section 5.2 with respect to the block diagram shown in Figure 5-1.

The motivation towards acquiring both the integrated current signal and the CVT secondary phase voltage is derived from the inability of the summation and integration system to produce a wideband signal including the fundamental frequency. The CVT voltage signal is acquired in order to establish a fundamental frequency upon which the transient waveform is superimposed.

The detection of the transient condition is performed by the analog trigger circuitry discussed in section 5.4. The integrated current signal is continuously monitored and upon detection of a transient condition a digital trigger signal to the data acquisition

card is generated. The analog trigger circuitry consists of an input buffer and band-pass filter, which is discussed in sections 5.4.1 and 5.4.2 respectively. The input buffer prevents unnecessary loading of the integrated current signal while the band-pass filter prevent false triggering due to noise outside of the integration range. The generation of the digital trigger signal is accomplished by implementing a window comparator, which creates a trigger on both rising and falling edges. The trigger generation is discussed in section 5.4.3.

The implementation of the graphical user interface is discussed in section 5.5 with respect to the control window shown in Figure 5-9. The user interface configures acquisition parameters, provides visual feedback on acquisition activities and creates a log file for post-analysis. The data extraction is briefly discussed in section 5.6 and presents the file data format and extraction constant.

Chapter 6

Laboratory Measurements and Analysis

6.1 Introduction

The previous chapters discussed the theoretical design of the measurement hardware in extended detail. This chapter deals with the operational verification of the design procedures in a laboratory environment. Section 6.2 deals with the measurement of the gain and phase responses for the split-core current transformers and the clamp-on current transducer. The measured data is utilised in an estimation routine in order to establish a frequency domain transfer function for these measurement devices. Section 6.3 discusses the time domain computer based simulation of the summation and integration system. Section 6.4 focuses on the practical measurements based on the simulations of Section 6.3. Section 6.5 closes with a summary of the chapter.

6.2 Measurement of the Split-core CT and Clamp-on Current Transducer Gain and Phase Responses

The equivalent circuits for the split-core current transformers and the clamp-on current transducer are inadequate to calculate a transfer function from theory. The gain and phase responses of the split-core current transformers and the clamp-on current transducer are determined by measuring each individual gain and phase responses at discrete frequencies. The arrangement for measuring the gain and phase responses for the individual devices is shown in Figure 6-1.

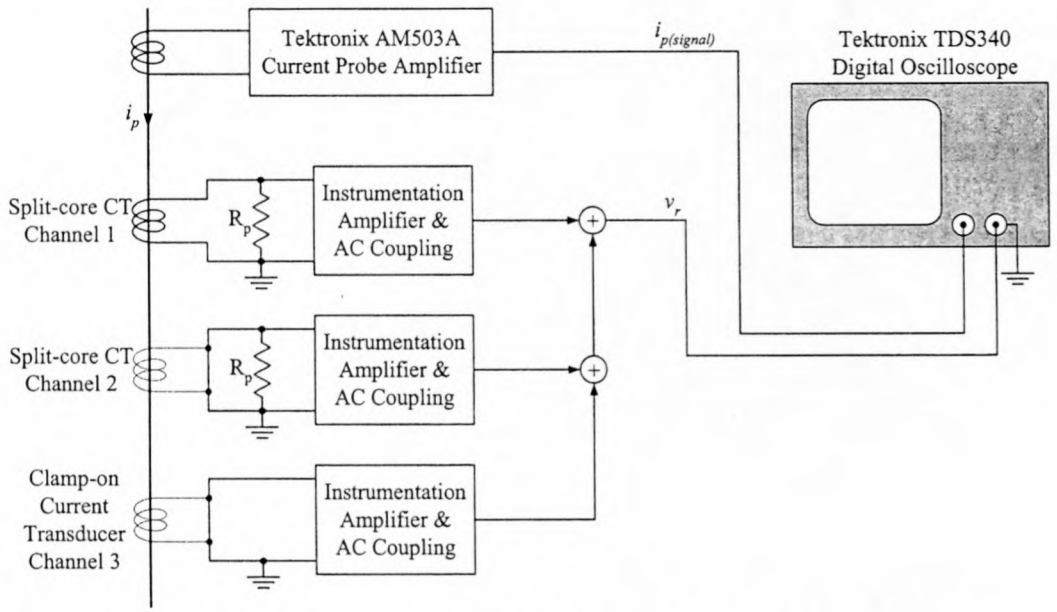

Figure 6-1 Measurement arrangement for determining the gain and phase responses of the split-core current transformers and the clamp-on current transducer.

Figure 6-1 shows the arrangement for measuring the gain and phase responses of a single split-core current transformer with the output of the other measuring devices short-circuited. The device under test (DUT) is excited with a sinusoidal input current i_p at a specified frequency. A specially designed wideband transconductance amplifier is used to generate the sinusoidal input current. The design of the wideband current amplifier is discussed in section 6.2.1. The sinusoidal input current is measured using a Tektronix wideband current probe amplifier [41]. The response of the system is measured at the output of the summation stage, which is represented by v_r. The gain and phase responses of either the split-core current transformers or the clamp-on current transducer are therefore defined from the input current i_p to the summated output voltage v_r.

6.2.1 Design of the wideband current output amplifier

The generation of the sinusoidal input current requires the use of a wideband current output amplifier. The peak value of the sinusoidal input current is required to be 1 A in order to produce a workable signal level. The circuit diagram of the amplifier is shown in Figure 6-2 [40].

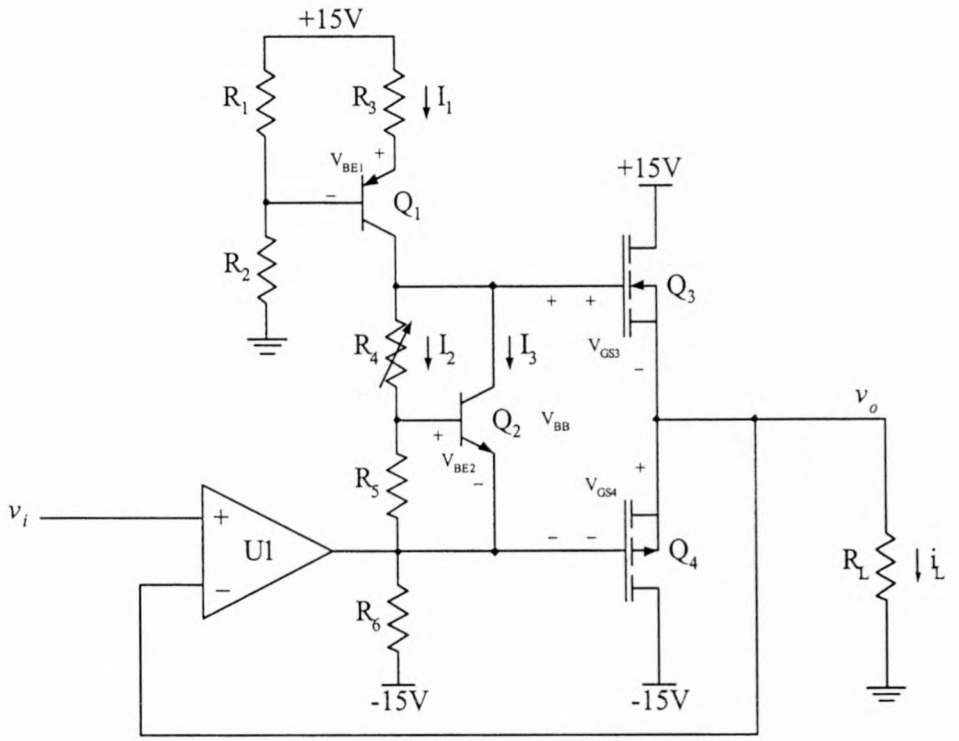

Figure 6-2 Circuit diagram of the wideband current amplifier.

Figure 6-2 shows the circuit diagram of the wideband current amplifier. The basic circuit comprises a voltage follower operational amplifier configuration U1 with a complimentary push-pull Metal Oxide Field Effect Transistor (MOSFET) output stage consisting of Q_3 and Q_4. The input signal is obtained from a commercial signal generator.

The N-channel and P-channel power MOSFET devices are represented by Q_3 and Q_4 respectively. The gate-to-source threshold voltage results in crossover distortion in the output signal. The crossover distortion is however minimised by the V_{be}-multiplier circuit [40], which consists of resistors R_4, R_5 and Q_2, which is a small signal NPN transistor. Resistors R_1, R_2 and R_3 and the PNP transistor Q_1 represents a constant current source used by the V_{be}-multiplier.

The current I_1 produced by the constant current source divides into I_2 and I_3. The current I_2 is constant as result of the base-emitter voltage V_{BE2} of the NPN transistor Q_2 across the fixed resistor R_5. The combined threshold values of V_{GS3} and V_{GS4} are represented by V_{BB}. The value of V_{BB} is adjusted by varying R_4. Resistor R_6 provides a current path for the current generated by the constant current source. The output current i_L is set by R_L.

The values of R_1 and R_2 are both set to 10 kΩ. The value of R_3 for a current I_1 of 2 mA is calculated as shown in equation (6-1).

$$R_3 = \frac{15 - V_{BE1} - \left(\frac{R_2}{R_1 + R_2}\right)15}{I_1} = \frac{15 - 0.7 - (0.5)15}{0.002} = 3.4\ k\Omega \tag{6-1}$$

I_2 is set to 0.5 mA. The resulting value of R_5 is calculated as shown in equation (6-2).

$$R_5 = \frac{V_{BE2}}{I_2} = \frac{0.7}{0.0005} = 1.4\ k\Omega \tag{6-2}$$

The threshold value for V_{GS1} and V_{GS2} is both specified between 2 V and 4 V. This implies that the combined biasing voltage V_{BB} may range between 4 V and 8 V. The maximum and minimum values of R_4 are therefore calculated as shown in equations (6-3) and (6-4) respectively with the maximum expected value of V_{BB} indicated by V_{BBmax} and the minimum value by V_{BBmin}.

$$R_4 = \frac{V_{BB\max} - I_2 R_3}{I_2} = \frac{8 - (0.0005)(1400)}{0.0005} = 14.6\ k\Omega \tag{6-3}$$

$$R_4 = \frac{V_{BB\min} - I_2 R_3}{I_2} = \frac{4 - (0.0005)(1400)}{0.0005} = 6.6\ k\Omega \tag{6-4}$$

Improper design of R_6 may result in unnecessary loading of the operational amplifier. The value of R_6 is set to produce an output voltage v_o equal to zero volts with a zero volts input signal. The value of R_6 is calculated as shown in equation (6-5). The threshold value of V_{GS4} is assumed to be 3 V.

$$R_6 = \frac{15 - V_{GS4}}{I_1} = \frac{15 - 3}{0.002} = 6\ k\Omega \tag{6-5}$$

The value of R_L is set to 1 Ω in order to minimise the power dissipation of R_L.

6.2.2 Practical measurement procedure

This section elaborates on the measurement arrangement as shown in Figure 6-1. The voltage output signal of the Tektronix current probe amplifier together with the output

signal from the summation stage is connected to the two input channels of a Tektronix TDS340 digital oscilloscope. The oscilloscope is capable of producing digital readouts of the RMS value of both channels. The oscilloscope also features a vertical cursor function in order to measure time delay.

Figure 6-3 shows a waveform representation of a typical measurement at a specified frequency. The RMS values of both signals is obtained from the digital readout and the phase difference is indicated by t_d, which is measured by moving the vertical cursors of the digital oscilloscope to the zero crossings of both signals.

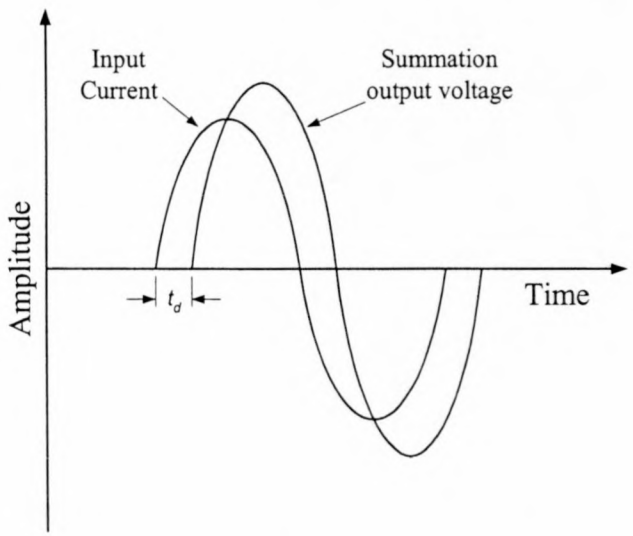

Figure 6-3 Measurement procedure for determining the gain and phase responses.

The measurement procedure is conducted for both split-core current transformers and the clamp-on current transducer, in each case short-circuiting the input of the unused measurement devices. The measured gain and phase responses of the two split-core current transformers and the clamp-on current transducer are shown in Figure 6-4, Figure 6-5 and Figure 6-6 respectively.

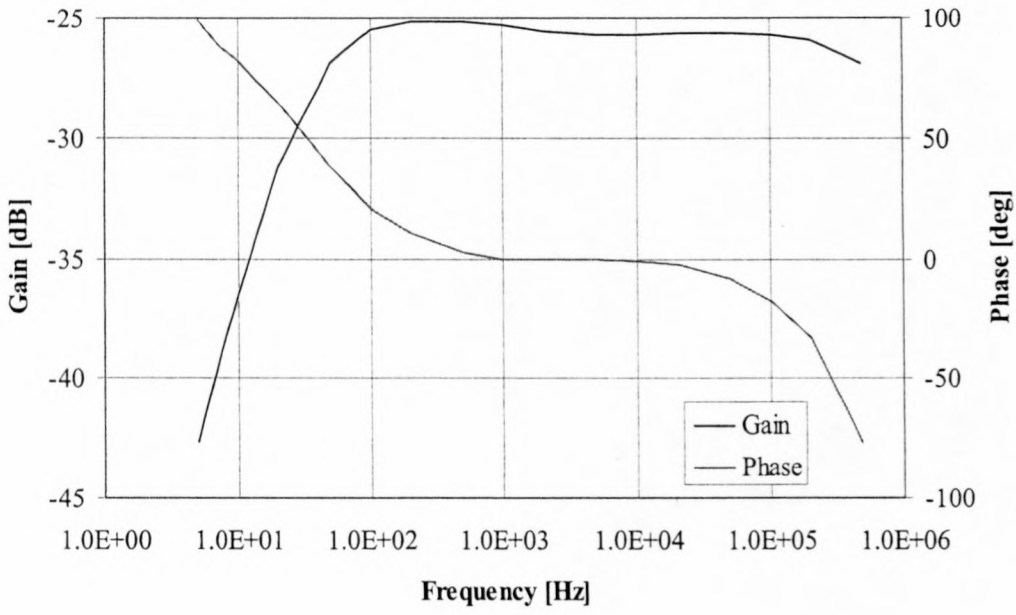

Figure 6-4 Gain and phase responses of the split-core CT connected on channel 1.

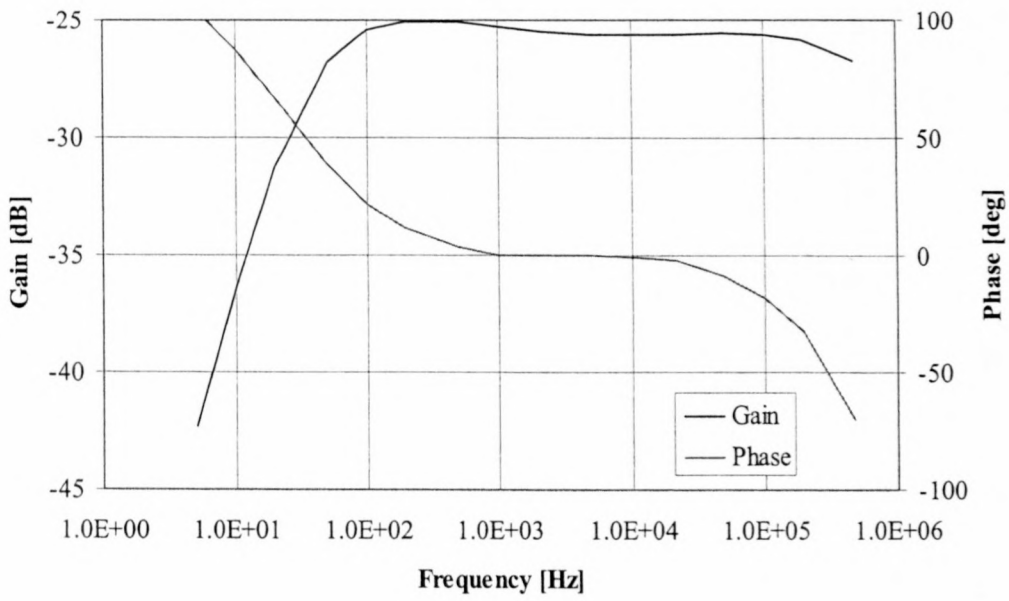

Figure 6-5 Gain and phase responses of the split-core CT connected on channel 2.

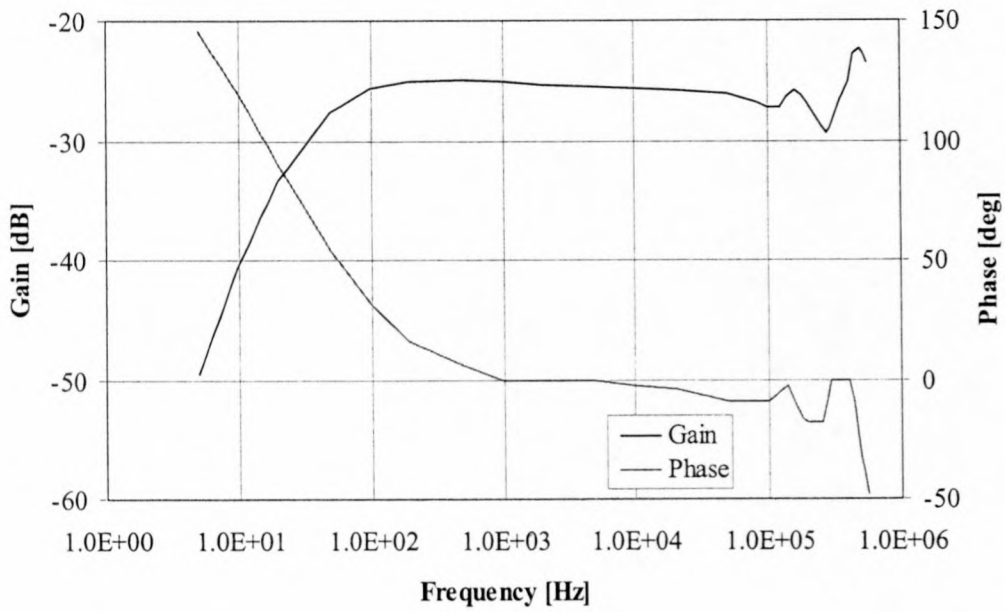

Figure 6-6 Gain and phase responses of the clamp-on current transducer connected on channel 3.

6.3 Computer Based Simulations

The time domain response of the summation and integration circuitry is evaluated by performing a computer-based software simulation. The software simulation consists of a frequency domain model describing the dynamic performance of the summation and integration circuitry, which is subjected to a time domain impulse current. The impulse current is obtained by calculating the resulting current as result of a known impulse voltage applied across a capacitor. The integrated current signal obtained from the simulation is then compared to the actual impulse voltage.

6.3.1 Frequency Domain Model

The frequency domain model of the summation and integration circuitry is obtained by cascading the individual frequency domain transfer functions given in chapter 3. The gain and phase measurements of the split-core current transformers and the clamp-on current transducer are defined at discrete frequencies. Evaluation of the gain and phase responses at frequencies other than measured require a frequency domain model of each measurement device. Such a model is obtained by employing a frequency domain estimation routine on the measured data. The frequency domain

estimation is performed using the *elis* function in the MATLAB® Frequency Domain System Identification Toolbox. The *elis* procedure provides real time visual feedback on the progress of the estimation process. The input parameters necessary for the estimation process is given as follows:

(iv) The measured frequency response data and the complex input and output Fourier data in matrix form called *Fdat* by MATLAB.

(v) The variances of each data point in *Fdat* are provided in matrix form called *vdat*.

(vi) Four other vectors describe the estimation process and are briefly discussed:

a) The vector *rppar* contains parameters, which describe the domain of the estimation either s-domain or z-domain, the order of the numerator and denominator of the estimated transfer function and the scaling frequency for the s-domain and sampling frequency for the z-domain.

b) The vector *rpalg* provides control over the iteration parameters, which includes the iteration algorithm, the manner in which the initial values is set, the maximum number of iterations and the maximum relative variation in the cost function and parameters upon termination of the estimation routine.

c) The vector *rppl* controls the plots during the iterations.

d) The vector *rpfs* contains the names of the files to be generated.

(vii) The *fixp* vector provides a means of fixing the value of certain parameters.

(viii) The *initp* vector contains the initial parameter values for the estimation process.

The *elis* procedure provides the following vectors as outputs:

(i) The estimated parameter vector called *pvect*, which contains the estimated coefficients of the transfer functions.

(ii) The vector *fit* which contains information on the estimation process such as the value of the cost function, the last change of the cost function and the last maximum change in the parameter values.

The order of the numerators and denominators were established by observation of the measured frequency response. Certain fixed parameters were provided in order to improve the convergence of the estimation algorithm. The general estimated symbolic transfer function is shown in equation (6-6) and the numerical coefficients for the respective channels in Table 6-1.

$$H_{EST}(s) = \frac{n_1 s^7 + n_2 s^6 + n_3 s^5 + n_4 s^4 + n_5 s^3 + n_6 s^2 + n_7 s}{d_1 s^8 + d_2 s^7 + d_3 s^6 + d_4 s^5 + d_5 s^4 + d_6 s^3 + d_7 s^2 + d_8 s + d_9} \qquad (6\text{-}6)$$

Table 6-1 Estimated transfer function coefficient values for channel 1, 2 and 3.

	Channel 1	Channel 2	Channel 3
n_1	0	0	-9.3×10^{-47}
n_2	0	0	-4.52×10^{-40}
n_3	0	-8.16×10^{-34}	-1.31×10^{-33}
n_4	8.96×10^{-28}	4.35×10^{-27}	-1.93×10^{-27}
n_5	-7.31×10^{-21}	2.38×10^{-22}	-1.74×10^{-21}
n_6	-9.23×10^{-16}	1.54×10^{-18}	-8.10×10^{-16}
n_7	-4.55×10^{-12}	-1.11×10^{-17}	3.81×10^{-15}
d_1	0	0	-4.30×10^{-52}
d_2	0	0	-3.85×10^{-45}
d_3	0	0	-1.16×10^{-38}
d_4	-4.46×10^{-33}	2.46×10^{-32}	-3.88×10^{-32}
d_5	-4.88×10^{-26}	8.42×10^{-26}	-4.06×10^{-26}
d_6	-1.45×10^{-19}	4.57×10^{-21}	-4.28×10^{-20}
d_7	-1.77×10^{-14}	2.84×10^{-17}	-1.46×10^{-14}
d_8	-8.38×10^{-11}	6.40×10^{-15}	-4.81×10^{-12}
d_9	-1.92×10^{-8}	3.83×10^{-14}	-2.22×10^{-10}

The evaluation of the estimated transfer functions obtained for each measurement device is shown in Figure 6-7, Figure 6-8 and Figure 6-9.

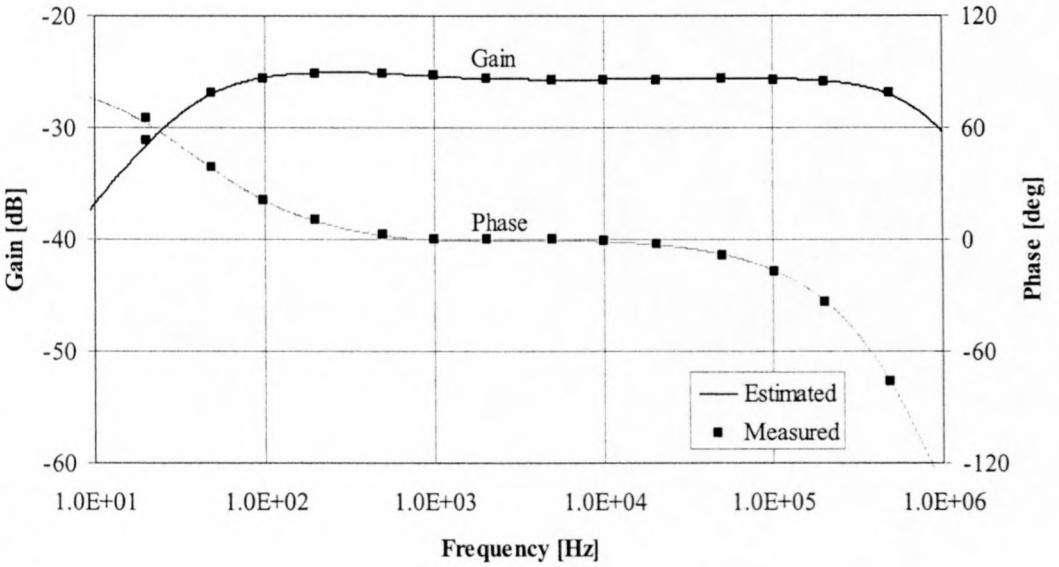

Figure 6-7 Measured and estimated gain and phase responses of the split-core current transformer connected on channel 1.

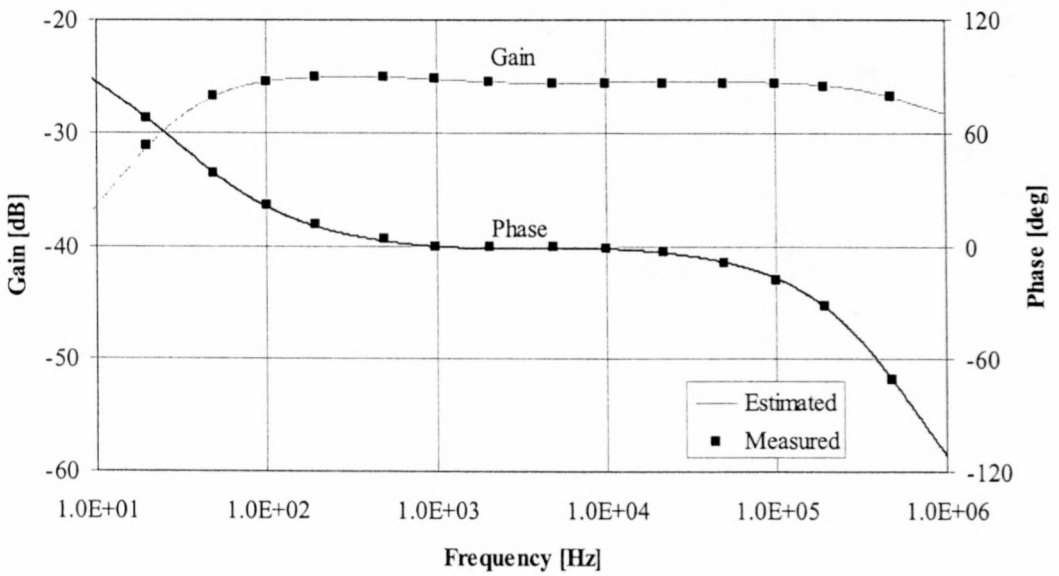

Figure 6-8 Measured and estimated gain and phase responses of the split-core current transformer connected on channel 2.

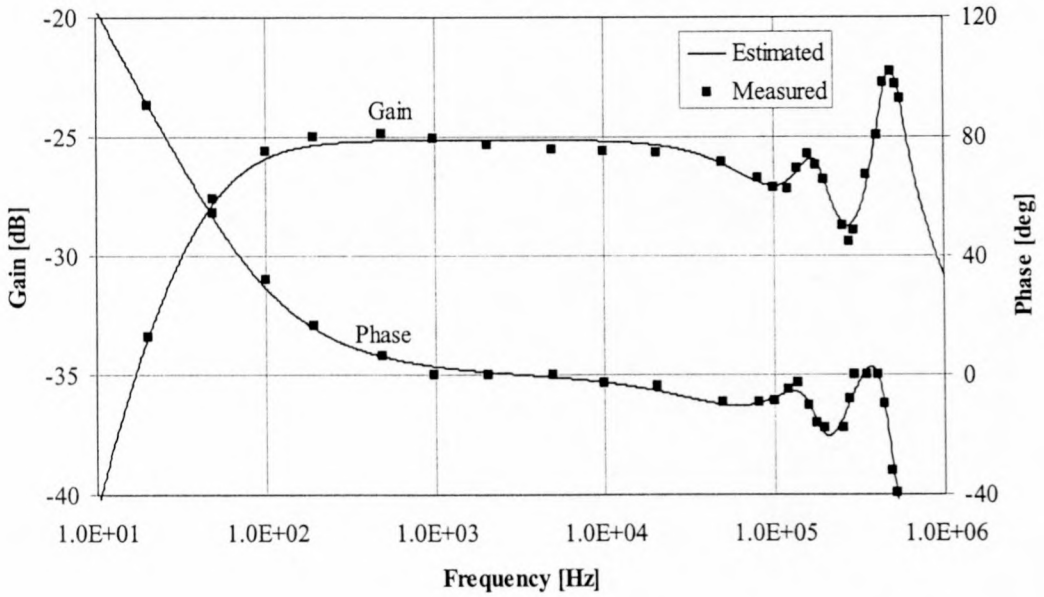

Figure 6-9 Measured and estimated gain and phase responses of the clamp-on current transducer connected on channel 3.

The time domain simulations are conducted in MATLAB® Simulink. MATLAB® Simulink is a graphical simulation extension of the MATLAB® environment, which implements systems by using a block-diagram methodology. The block-diagram implemented in MATLAB® Simulink describes the summation and integration circuitry is shown in Figure 6-10.

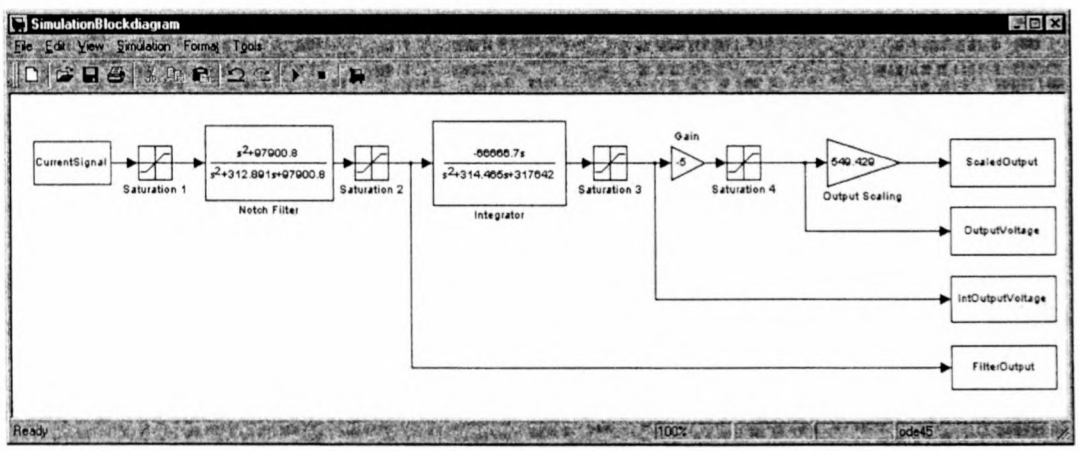

Figure 6-10 Block-diagram implementation using MATLAB® Simulink.

The input signal to the simulation is a matrix variable comprised of an equally spaced time vector and amplitude vector obtained from the MATLAB® workspace. The input variable represents the response of the individual measurement devices. The

output signals from the various stages are returned to the MATLAB® workspace as vector variables. The simulation also incorporates non-linear effects such as saturation, which occurs when the signal level exceeds the power rail of the analog circuitry. A single saturation block is utilised for the summation stage as saturation of any measurement device results in unwanted non-linear effects in the system.

The output-scaling factor shown in Figure 6-10 scales the voltage obtained from the summation and integration circuitry to the actual impulse voltage level. The scaling constant is calculated as shown in equation (6-7).

$$G_{OutputScaling} = \frac{1}{G_{scale} G_{INT} G_{OUT} C_{CT}} = 549.43 \tag{6-7}$$

G_{INT} represents the integrator gain given by equation (3-17). The value of G_{INT} is recalculated at 66666.7 for the practical component values as shown in section 3.8. G_{OUT} gives the gain of the output stage following the integrator, which is equal to 5 and C_{CT} the value of the capacitance used to generate the impulse current, which is equal to 104 nF.

G_{scale} represents the gain of the measurement devices and the instrumentation amplifiers. The theoretical value of G_{scale} is presented for the split-core CT and the clamp-on current transducer in equations (6-8) and (6-9) respectively. W gives the value of winding ratio of the split-core CT, R_p the value of the termination resistance and G_{CTD} the attenuation ratio of the clamp-on current transducer. G_{IA} gives the gain of the instrumentation amplifiers and G_{scale} the calculated gain used to scale the impulse current.

$$G_{scale} = \frac{1}{W} R_p G_{IA} = \left(\frac{1}{100}\right)(0.1)(50) = 0.05 \tag{6-8}$$

$$G_{scale} = G_{CTD} G_{IA} = (0.01)(5) = 0.05 \tag{6-9}$$

The value of 0.05 as indicated in equations (6-8) and (6-9) is verified by evaluating the response in the pass-band of the measurement devices as shown in Figure 6-7, Figure 6-8 and Figure 6-9. This observation indicates a value for G_{scale} of

approximately 0.05248. The measured value rather than the theoretical value will be utilised in calculating the integrated output scaling gain.

6.3.2 Impulse Current Generation

As mentioned in section 6.3.1 the individual responses of the measurement devices are applied to the simulation given in Figure 6-10. The measurement device response is generated in the MATLAB® workspace by evaluating the individual transfer functions of each measurement device. The impulse current used for this evaluation is generated as shown in Figure 6-11 [42]. This circuit is also utilised in the practical measurements, which is discussed in section 6.4.

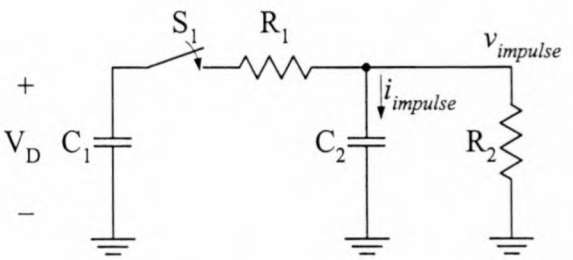

Figure 6-11 Circuit diagram for impulse current generation.

The circuit of Figure 6-11 shows a capacitor C_1 which is initially charged to a voltage level V_D. Switch S_1 is closed and the charge contained in C_1 is discharged into the remainder of the circuit represented by R_1, C_2 and R_2. The values of these elements determine the shape of the transient voltage $v_{impulse}$. The transient voltage across C_2 results in a transient current $i_{impulse}$ to flow through C_2, which is used to evaluate the response of the measurement devices. The motivation for using a capacitive impulse current and voltage is that it represents the actual substation measurement arrangement with the advantage of practical verification in a laboratory environment.

The impulse current $i_{impulse}$ and impulse voltage $v_{impulse}$ is calculated by determining the impulse response of their individual frequency response functions. This is easily performed in MATLAB® and is verified by practical measurement. The circuit diagram used to determine these frequency response functions incorporates the initial conditions and impedances of the circuit elements of Figure 6-11 in the s-domain and is shown in Figure 6-12.

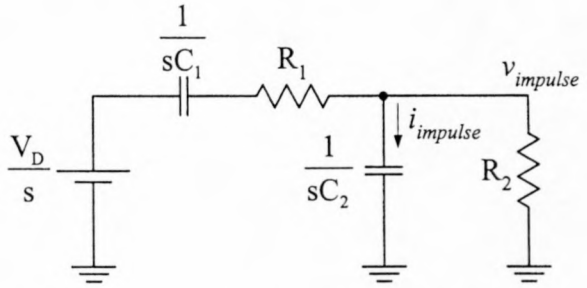

Figure 6-12 Circuit diagram in the s-domain used to determine the transfer functions of $v_{impulse}$ and $i_{impulse}$.

The initial charge condition of C_1 is represented by the voltage V_D/s and capacitor reactance $1/sC_1$ [43]. The impulse voltage and current waveforms are obtained by calculating the impulse response of the respective transfer functions. The frequency responses of the impulse voltage and impulse current are shown in equations (6-10) and (6-11) respectively.

$$V_{\mathrm{Im}\,pulse}(s) = \frac{V_D \dfrac{1}{R_1 C_2}}{s^2 + s\left(\dfrac{R_2C_2 + R_1C_1 + R_2C_1}{R_1R_2C_1C_2}\right) + \dfrac{1}{R_1R_2C_1C_2}} \qquad (6\text{-}10)$$

$$I_{\mathrm{Im}\,pulse}(s) = \frac{s\dfrac{V_D}{R_1}}{s^2 + s\left(\dfrac{R_2C_2 + C_1(R_1 + R_2)}{R_1R_2C_1C_2}\right) + \dfrac{1}{R_1R_2C_1C_2}} \qquad (6\text{-}11)$$

The transfer functions of equations (6-10) and (6-11) are evaluated for the values shown in Table 6-2.

Table 6-2 Table of component values for evaluation of equations (6-10) and (6-11).

Component	Value	Unit
V_D	100	V
C_1	657	nF
R_1	39.2	Ω
C_2	104	nF
R_2	563	Ω

The impulse voltage and current obtained from the impulse response of equations (6-10) and (6-11) for the values shown in Table 6-2 are shown in Figure 6-13 and Figure 6-14.

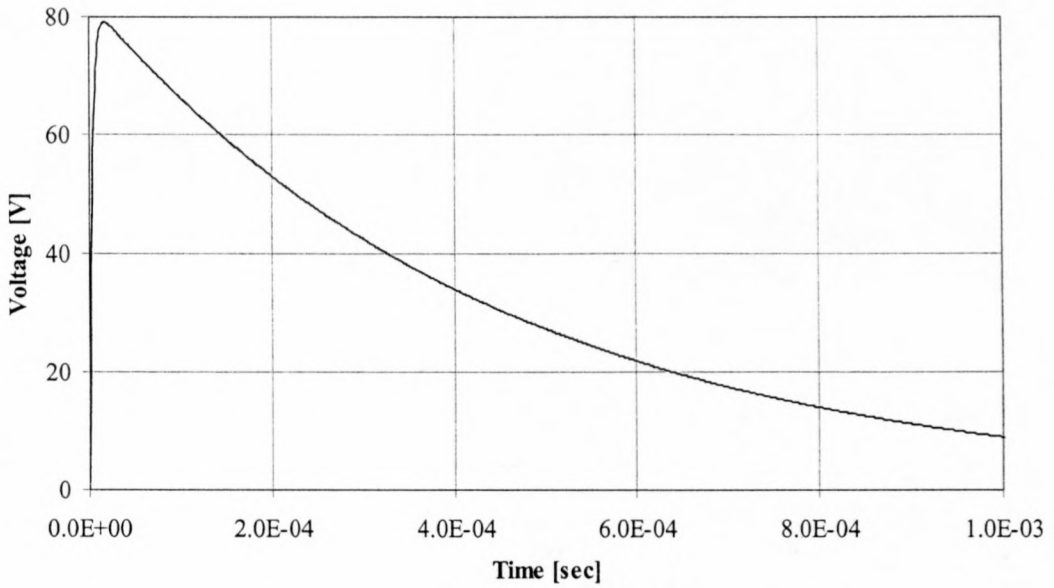

Figure 6-13 Impulse voltage obtained from the impulse response of the transfer function shown in equation (6-10).

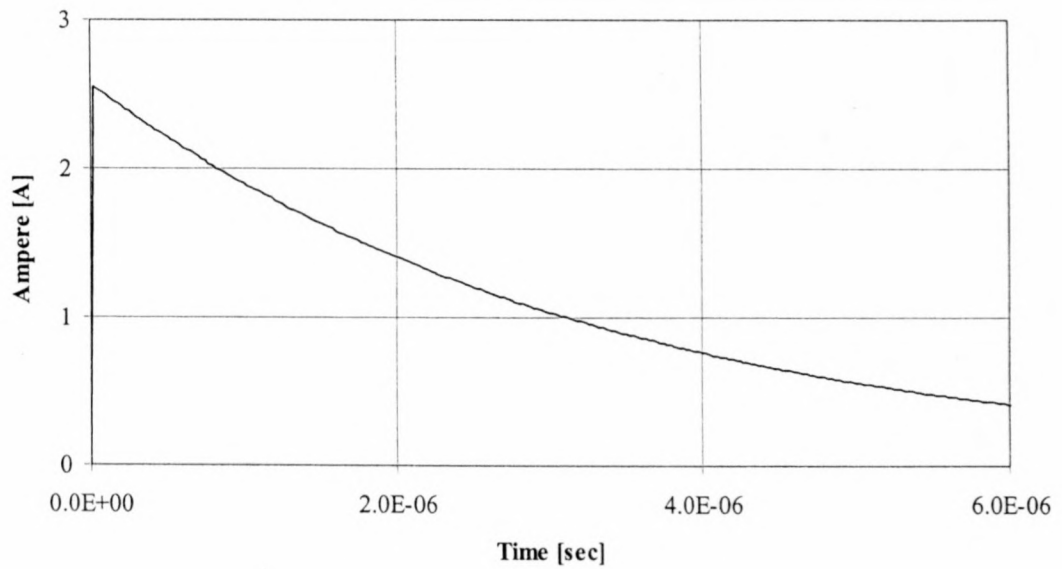

Figure 6-14 Impulse current obtained from the impulse response of the transfer function shown in equation (6-11).

6.3.3 Simulation Results

The results obtained from the time domain simulations are presented as the response of the system for each individual measurement device. The motivation is that the simulation of the system with all the measurement devices in operation requires the knowledge of the amplitude of the impulse current that flows in each current path. Recreating the simulation conditions in practice for multiple current paths is not a trivial exercise and the system is therefore evaluated for each measurement device individually. Satisfactory evaluation of each measurement device results in proper evaluation of the summation process as the individual transfer functions includes the summation stage.

The measurement devices are evaluated by obtaining the simulated responses to the impulse current shown in Figure 6-14. The impulse current is scaled with attenuation factors for comparison to the response of the split-core current transformers and the clamp-on current transducer as discussed in section 6.3.1. The response of the split-core CT connected on channel 1 is compared to the impulse current as shown in Figure 6-15.

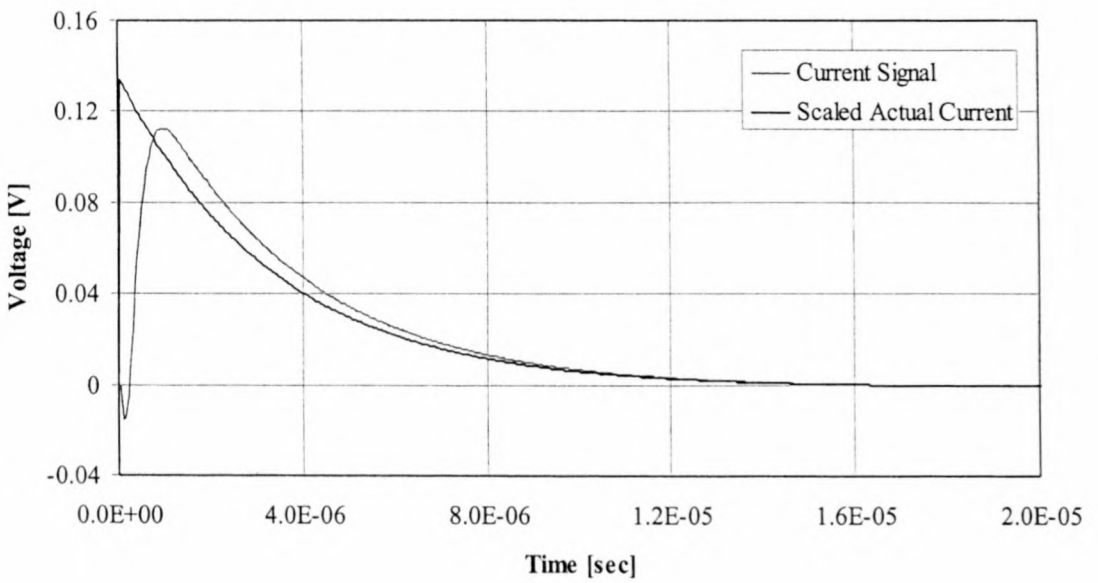

Figure 6-15 Simulated response of the split-core CT connected on channel 1 together with the simulated scaled impulse current.

The response of the split-core CT connected on channel 2 is compared to the impulse current as shown in Figure 6-16.

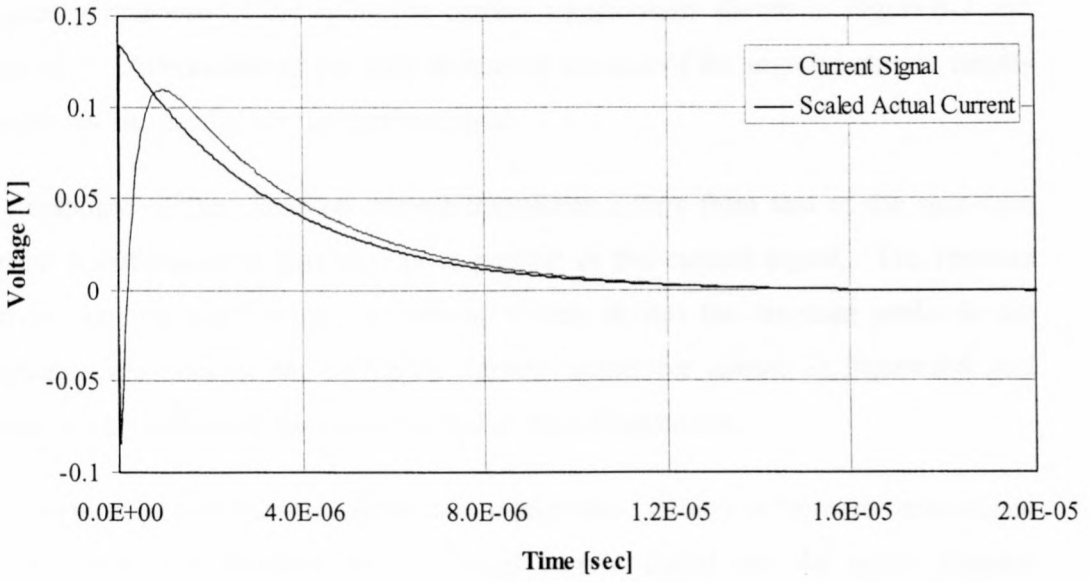

Figure 6-16 Simulated response of the split-core CT connected on channel 2 together with the simulated scaled impulse current.

The response of the clamp-on current transducer connected on channel 3 is compared to the impulse current as shown in Figure 6-17.

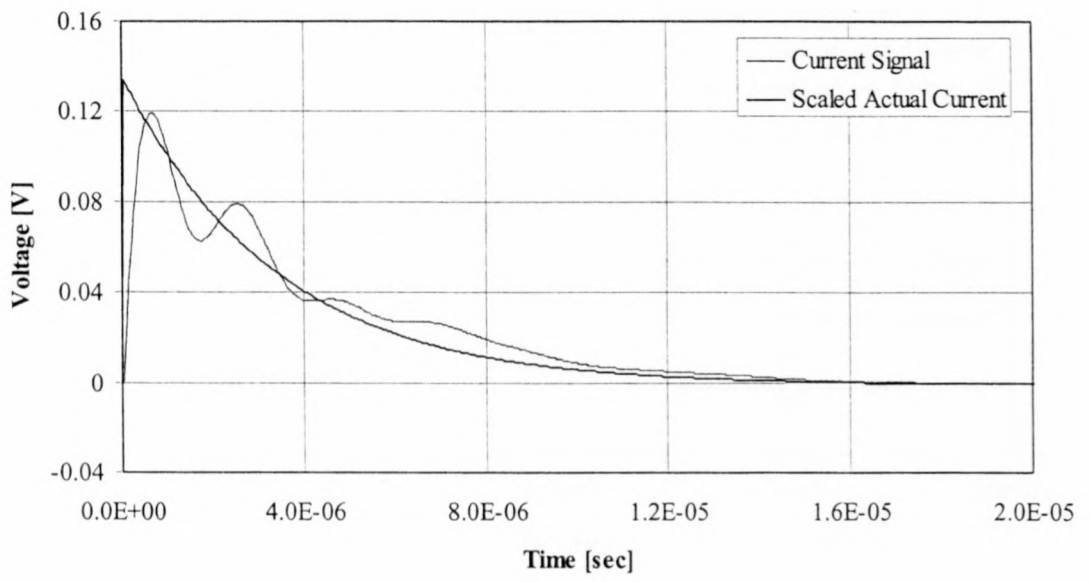

Figure 6-17 Simulated response of the clamp-on current transducer connected on channel 3 together with the simulated scaled impulse current.

Observation of the responses of the split-core current transformers shown in Figure 6-15 and Figure 6-16 indicate relative accurate correlation. The rising slope of the current signal is less than that of the actual impulse current. This is revealed in the frequency response of the split-core current transformers shown in Figure 6-7 and Figure 6-8. Attenuation of the high frequency content of the impulse current results in a slower rising edge for the current signal.

The response of the clamp-on current transducer differs from that of the split-core current transformers in that ringing is present in the current signal. The impulse current contains high frequency content, which excites the resonant peaks in the frequency response of the clamp-on current transducer shown in Figure 6-9 and results in oscillations of the current signal at these frequencies.

The performance of the summation and integration circuitry is however determined by the correlation between the integrated current signal and the actual impulse voltage. The simulated response as shown in Figure 6-15, Figure 6-16 and Figure 6-17 is applied individually to the frequency domain simulation shown in Figure 6-10. The scaled integrated current signal is compared to the actual impulse voltage. The scaled integrated current signal for the split-core CT connected on channel 1 is shown in Figure 6-18.

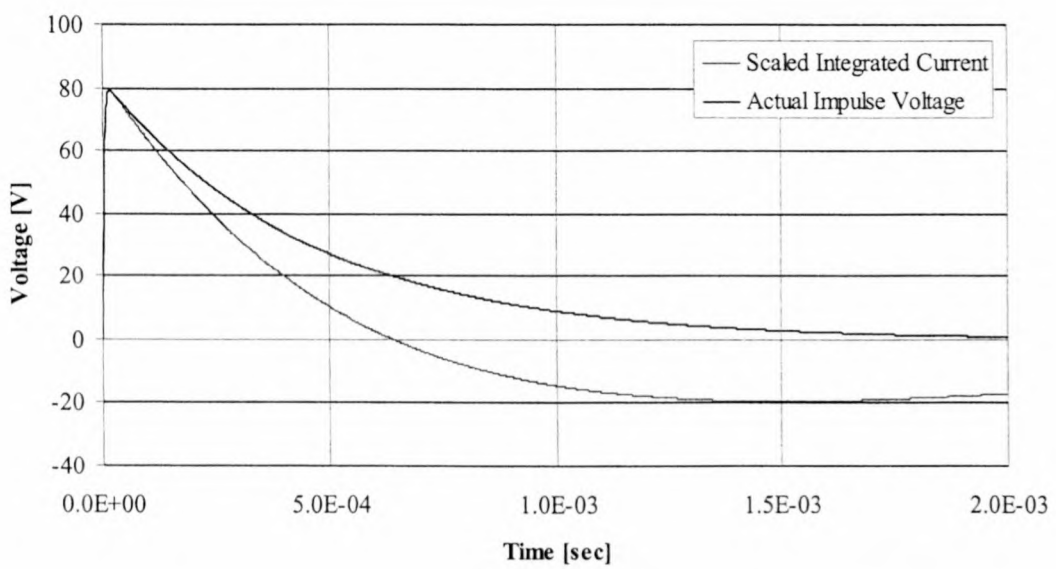

Figure 6-18 Simulated scaled integrated current and actual impulse voltage for the split-core CT connected on channel 1.

The scaled integrated current signal for the split-core CT connected on channel 2 and the clamp-on current sensor connected on channel 3 is shown in Figure 6-19 and Figure 6-20 respectively.

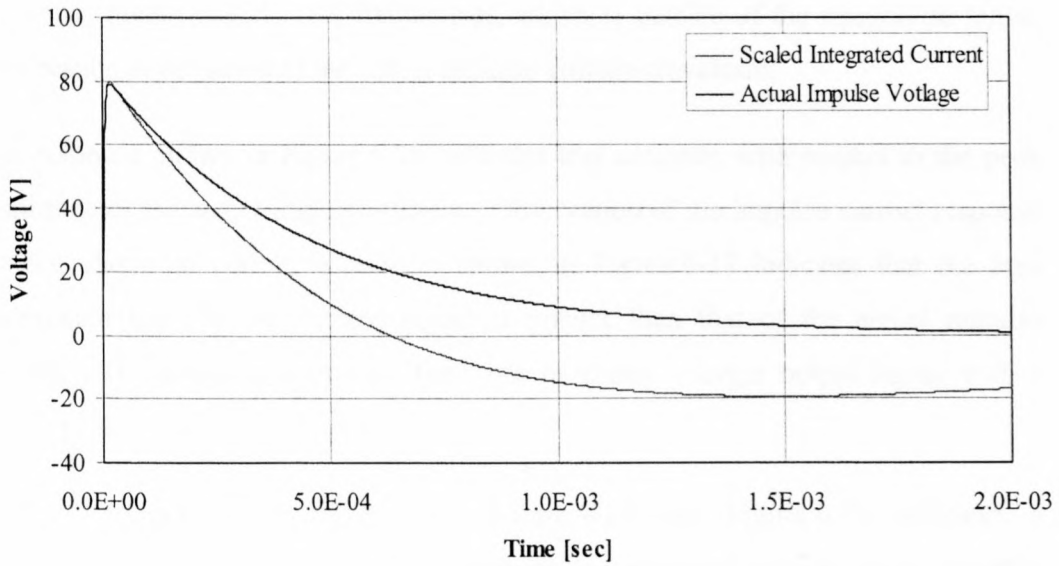

Figure 6-19 Simulated scaled integrated current and actual impulse voltage for the split-core CT connected on channel 2.

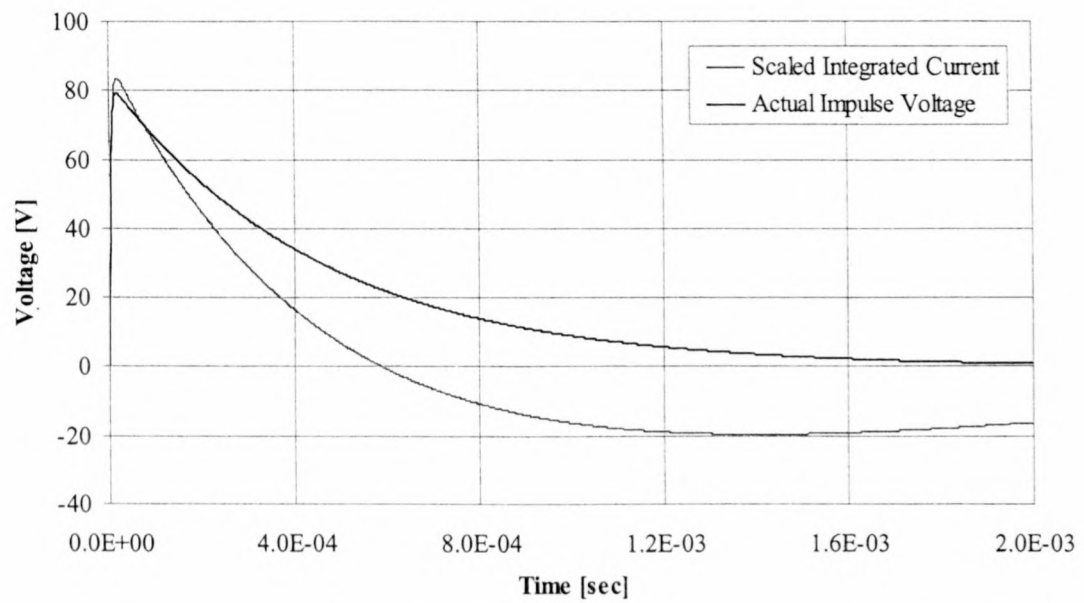

Figure 6-20 Simulated scaled integrated current and actual impulse voltage for the clamp-on current transducer connected on channel 3.

Observation of the simulation results shown in Figure 6-18, Figure 6-19 shows accurate correlation with respect to the rising slope and peak impulse value of the actual impulse voltage. The correlation to the falling slope of the actual impulse voltage is less accurate. The frequency content of the falling slope of the impulse current is predominantly low frequencies, which is outside of the integration range. This results in deviation of the actual impulse voltage waveform.

The response shown in Figure 6-20 indicates less accuracy with respect to the peak amplitude of the actual impulse current. Observation of the impulse current response for the clamp-on current transducer shown in Figure 6-17 indicates that the area underneath the impulse current signal is greater than that of the actual impulse current. The integration process therefore produces a larger output signal with a higher peak value.

Further observation of Figure 6-18, Figure 6-19 and Figure 6-20 indicates a characteristic oscillation in the falling edge of the integrated current signal, which is as result of the impulse response of the integrator. The normalised impulse response of the integrator is shown in Figure 6-21.

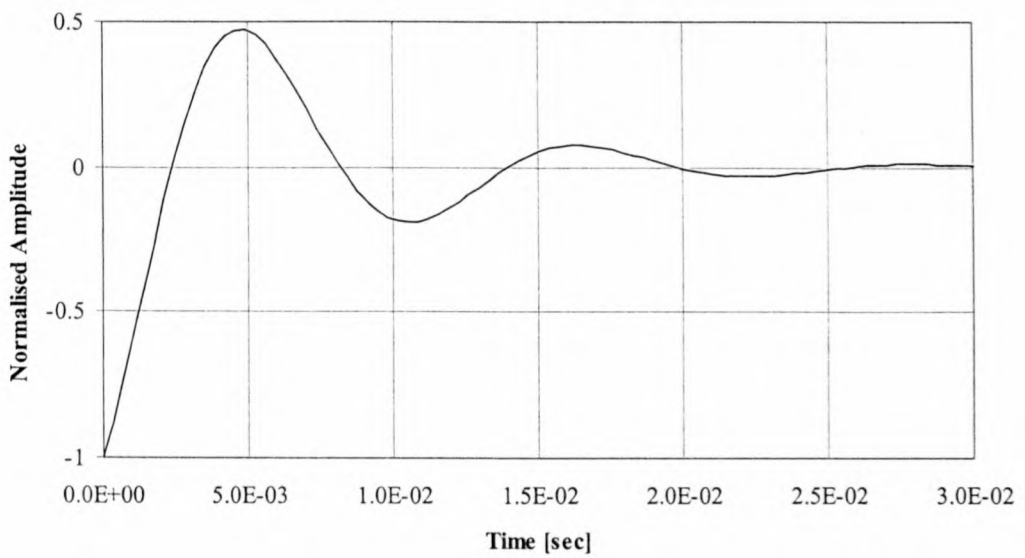

Figure 6-21 Normalised impulse response of the integrator.

The generation of the impulse response induces the broadband excitation of the integrator, which results in the waveform shown in Figure 6-21. The simulated impulse current signal shown in Figure 6-14 is similar to the input used to establish

the impulse response but is band limited. The response of the integrator as result of the impulse current signal is therefore similar to Figure 6-21 although the oscillation is less severe.

6.4 Laboratory Measurements

This section deals with the practical verification of the simulations performed in section 6.3. The measurement arrangement for the practical evaluation is shown in Figure 6-22.

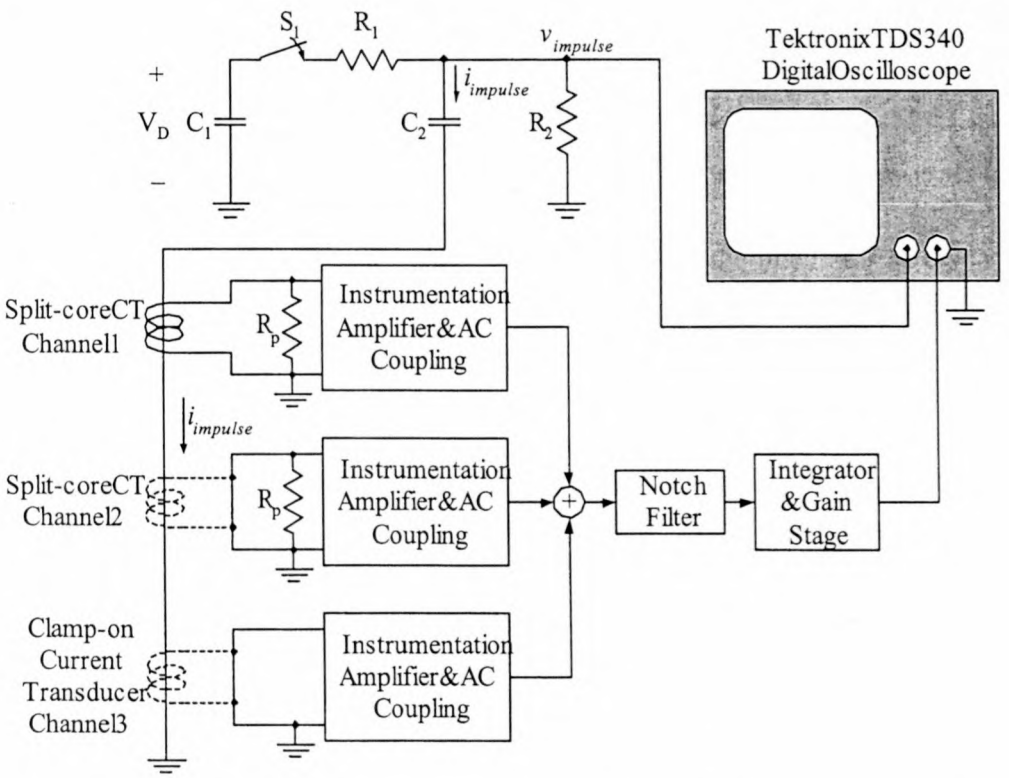

Figure 6-22 Measurement arrangement for the practical laboratory evaluation.

The measurement arrangement of Figure 6-22 shows the generation of the impulse voltage and impulse current. The integrated current signal is measured together with the actual impulse voltage for each measurement device individually.

The values of C_1, R_1, C_2 and R_2 are given by Table 6-2 The shape of the impulse transient generated by the impulse generator is therefore identical to the response shown in Figure 6-13 and Figure 6-14. The impulse generation is evaluated with respect to the simulation as discussed in section 6.3.2 by correlating the measured

impulse voltage $v_{impulse}$ and the impulse current $i_{impulse}$ with the simulated transients. The measured and simulated impulse voltage $v_{impulse}$ is shown in Figure 6-23.

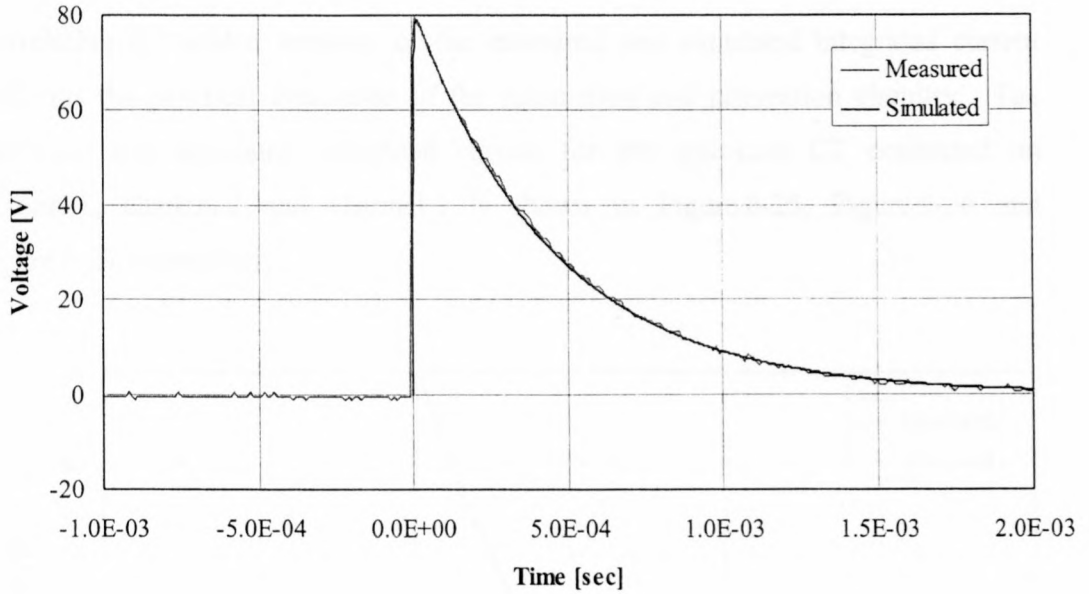

Figure 6-23 Measured and simulated actual impulse voltage.

The measured and simulated impulse current $i_{impulse}$ is shown in Figure 6-24.

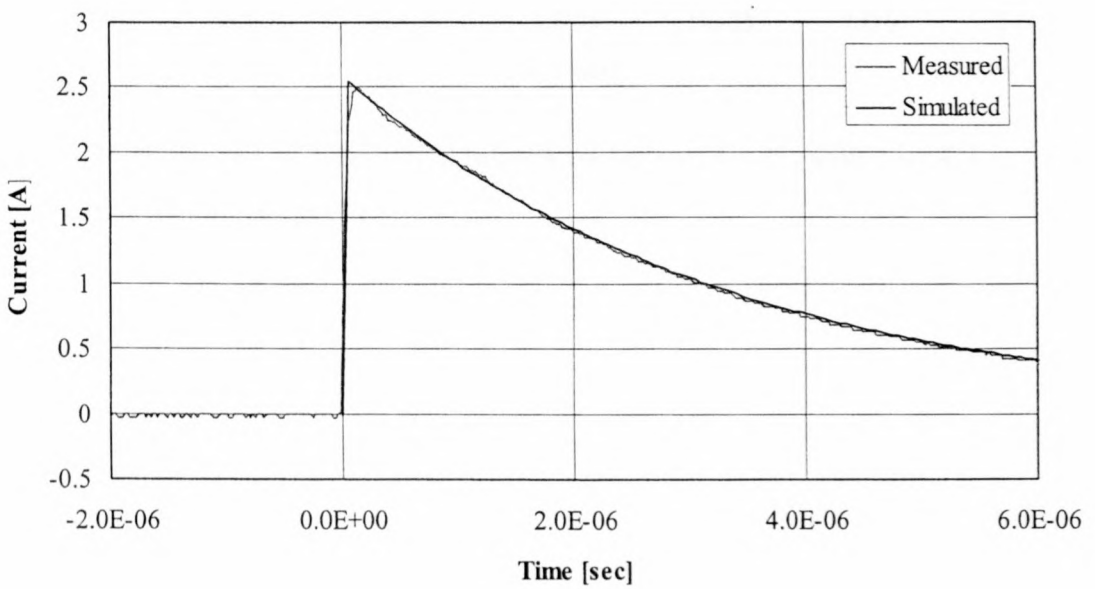

Figure 6-24 Measured and simulated actual impulse current.

The measurement arrangement for measuring the impulse current is identical to Figure 6-1, which employs the Tektronix AM503A Current Probe Amplifier to

measure the impulse current $i_{impulse}$. Observation of the impulse voltage and impulse current shown in Figure 6-23 and Figure 6-24 indicates an excellent correlation between the simulated and measured impulse voltage and impulse current.

Correlating the scaled versions of the measured and simulated integrated current performs the practical evaluation of the summation and integration circuitry. The measured and simulated integrated current for the split-core CT connected on channel 1, channel 2 and channel 3 is shown in Figure 6-25, Figure 6-26 and Figure 6-27 respectively.

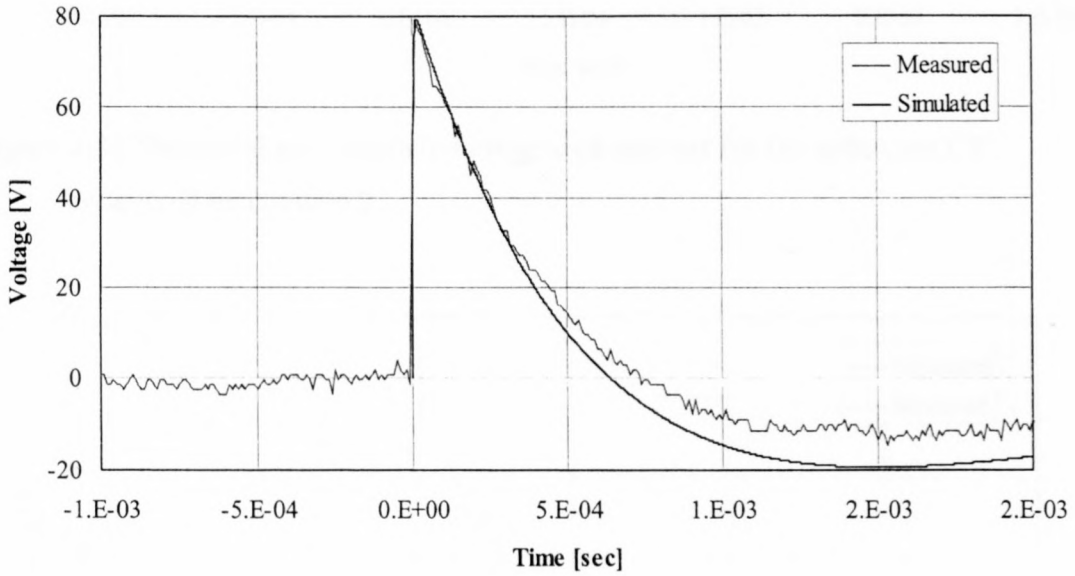

Figure 6-25 Measured and simulated integrated current for the split-core CT connected on channel 1.

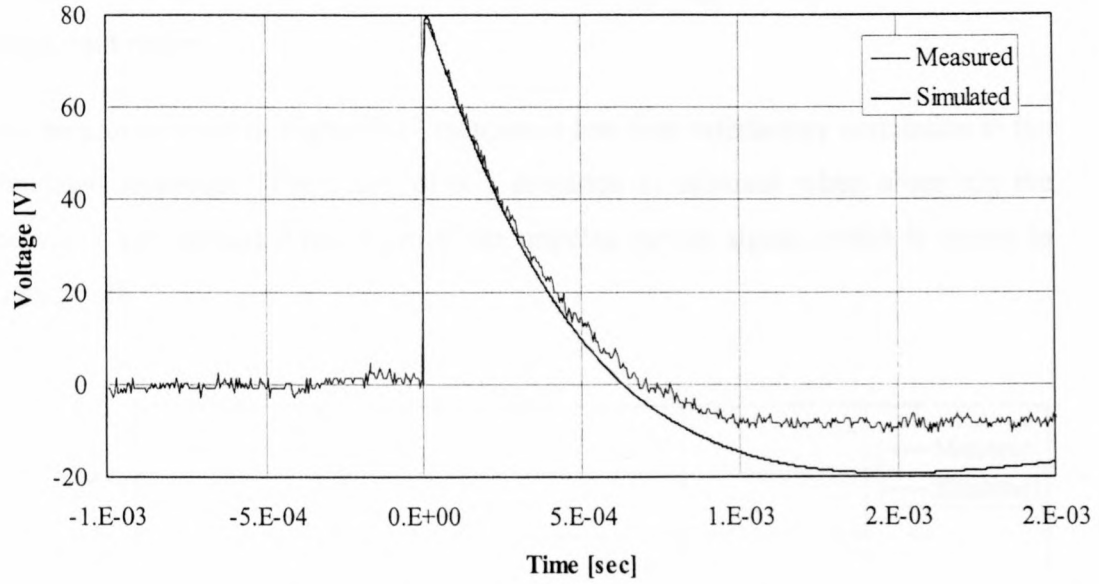

Figure 6-26 Measured and simulated integrated current for the split-core CT connected on channel 2.

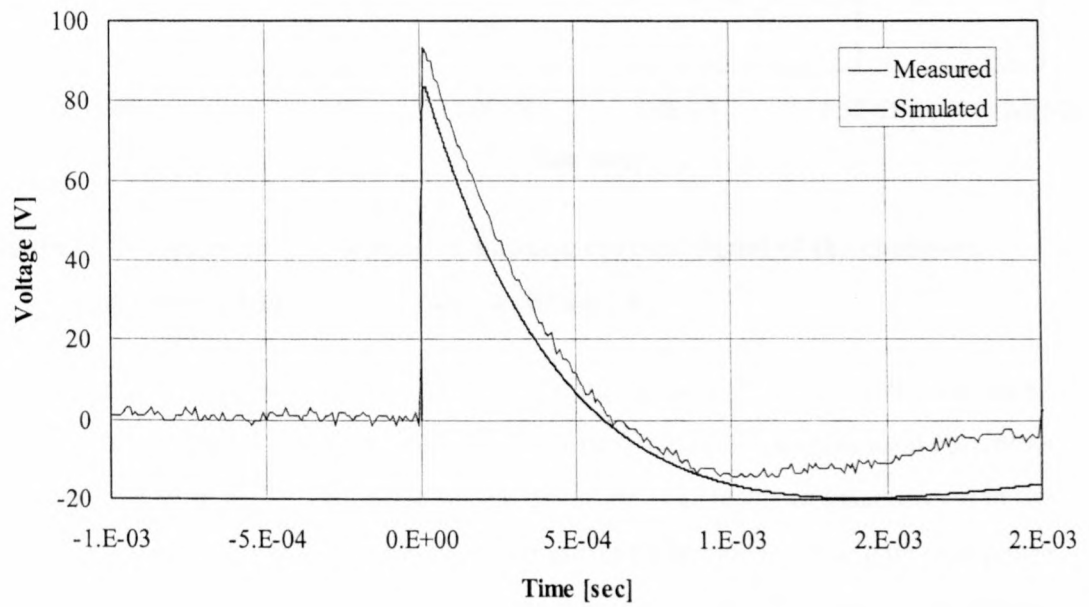

Figure 6-27 Measured and simulated integrated current for the clamp-on current transducer connected on channel 3.

The measured results shown in Figure 6-25 and Figure 6-26 shows good correlation with respect to the simulated results. The falling edge of the measured integrated current however deviates from the simulated waveform. The deviation is as result of noise present in the summation and integration circuitry, which is not included in the

simulation. This is however in the low frequency region, which is outside the integration range.

The measured result of Figure 6-27 indicates a less than satisfactory correlation to the simulated response. The cause of this deviation is apparent when observing the measured and simulated responses of the impulse current signal, which is shown in Figure 6-28.

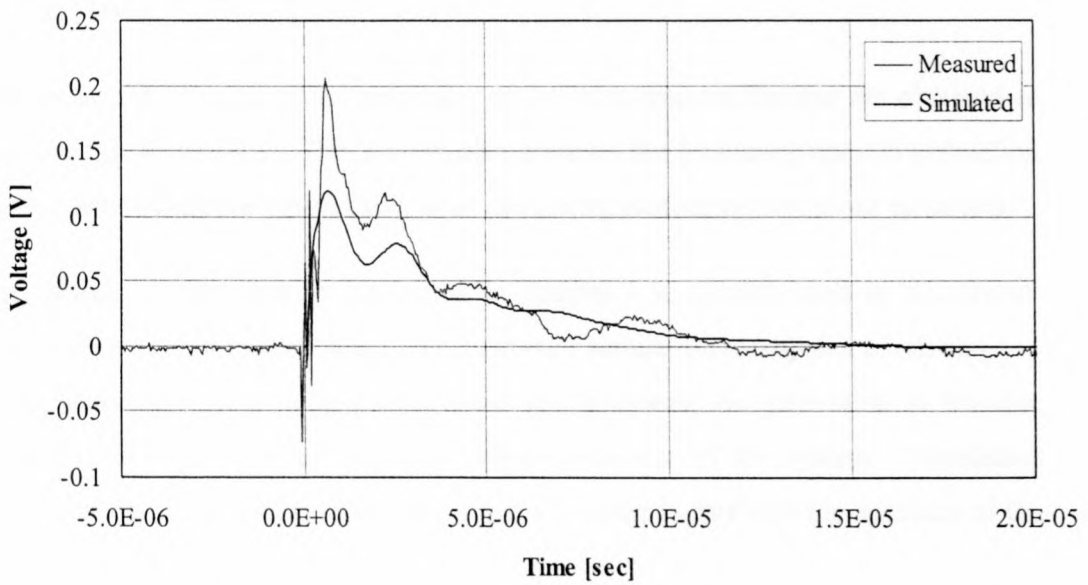

Figure 6-28 Measured and simulated impulse current signal of the clamp-on current transducer connected on channel 3.

The area underneath the measured impulse current signal is greater than the simulated impulse current signal. This results in a greater peak value in the integrated current as observed in Figure 6-27. The cause for the deviation is as result of inaccuracies in the estimated transfer function for the clamp-on current transducer. The gain and phase responses used to estimate the transfer function lacks the higher frequency information in order to establish an accurate representation.

The accuracy of the summation and integration method for impulse measurements is established by correlating the rising slope and peak impulse value of the measured and simulated impulse responses. The correlation of the falling edge is of less importance as it contains low frequencies, which is of lesser importance for transient measurements.

The laboratory measurements indicate that the scaled integrated current correlates well with the actual impulse voltage for frequencies within the integration range. The deviation from the actual impulse voltage at lower frequencies is acceptable as the aim is to establish a benchmark for transient voltage measurement.

6.5 Summary

This chapter evaluated the summation and integration circuitry on simulation and practical level.

The measured gain and phase responses of the measurement devices are obtained as discussed in section 6.2. This section also presents the frequency domain estimation routine with which the transfer functions of each measurement device are estimated.

The design of the circuitry presented in chapter 3 is implemented in a software simulation as given in section 6.3. The software simulation establish a block diagram of the summation and integration system and discusses the generation of impulse signals in order to evaluate the time domain response of the system. Simulation results are correlated with actual input signals in order to establish the accuracy of the summation and integration system.

Practical evaluation of the summation and integration circuitry are performed in section 6.4 based on the simulations of section 6.3. The conclusion of the software simulations and practical evaluations is that the split-core current transformers are better equipped to accurately measure transient waveforms. In the absence of an accurate measurement device in order to measure the earth current in the secondary cable armouring, the use of a commercially available clamp-on current transducer is a satisfactory alternative.

Chapter 7

Field Evaluation

7.1 Introduction

This chapter presents the measurements conducted in a substation environment using the summation and integration technique. The measured results are presented in section 7.2, which discusses the steady state response as well as the transient responses. Section 7.3 presents the post processing methodology of the measured data. Section 7.4 closes with a summary of chapter 7.

7.2 Measurement Results

This section presents the measurement results obtained in the substation environment. As mentioned in section 5.2, the data acquisition system acquires both the integrated current signal obtained from the summation and integration system as well as the CVT secondary phase voltage signal. The steady state performance of the acquired data is presented in section 7.2.1. The steady state performance is important as it contributes to the post processing of the acquired data, which is discussed in section 7.3. The transient results are presented in section 7.2.2.

The accuracy of the measurements with respect to a wideband transient measuring device such as a capacitive voltage divider could not be established. The time frame of the substation evaluation denied the installation of a wideband transducer. The accuracy of the measurements is however referenced to the laboratory evaluation as described in sections 6.3 and 6.4. The linearity of the summation stage in the summation and integration circuitry is employed to establish accuracy for each individual current sensing device. The combined response of the system in the

integration frequency range is therefore equal to the summation of the individual response of each current sensing device.

7.2.1 Steady state measurement results

The steady state response of the CVT voltage represents the fundamental frequency on which the transient waveforms are superimposed. The acquired CVT secondary phase voltage signal is scaled in order to obtain the actual phase voltage. The scaling factor of the acquired data is given in equation (5-11) and the scaling factor used to obtain the primary CVT phase voltage is discussed in section 5.2. The scaled CVT secondary phase voltage is shown in Figure 7-1.

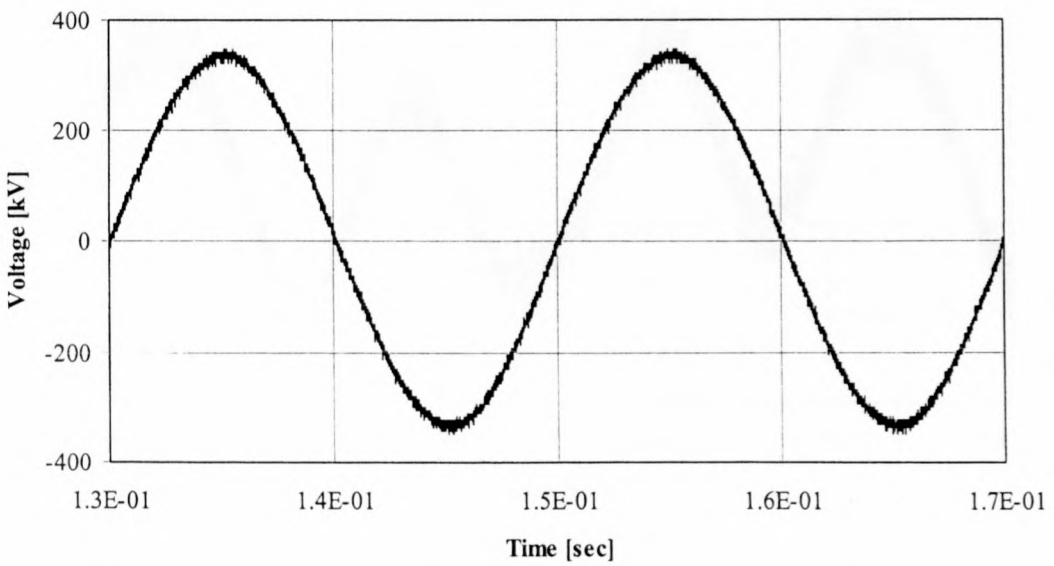

Figure 7-1 Steady state response of the CVT secondary phase voltage.

Figure 7-1 indicates a relatively uncorrupted fundamental frequency. This is due to the fact that the CVT is a narrow band device, which implies that the secondary phase voltage is predominantly the representation of the fundamental frequency with only low frequency harmonics [1, 2].

The steady state response of the acquired integrated current signal is desired to be zero. This is however accomplished in a less than perfect manner as result of the mismatch between the earth current measurement devices shown in section 6.2.

The scaling of the integrated current signal is shown in equation (7-1). This calculation is based on equation (6-7) with the same values for G_{scale}, G_{int} and G_{out} as given in section 6.3.1. The value of C_{CT} is however substituted with the substation CT capacitance, which is equal to 1.081 nF.

$$G_{OuptutScaling} = \frac{1}{G_{scale} G_{\text{int}} G_{out} C_{CT}} = 57164.6 \qquad (7\text{-}1)$$

The steady state acquisition of the summation and integration signal is shown in Figure 7-2.

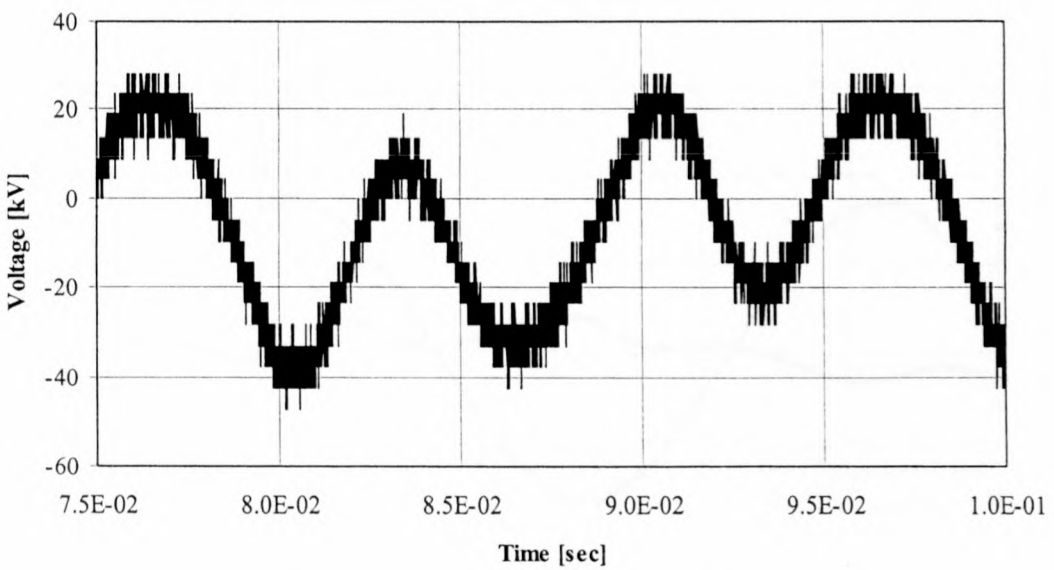

Figure 7-2 Steady state response of the scaled integrated current signal.

Figure 7-2 indicates the mismatch between the measurement devices. Comparison of Figure 6-9 with Figure 6-7 and Figure 6-8 indicates minor mismatches between the gain and phase responses at low frequencies up to approximately 1 kHz. The value of the waveform shown in Figure 7-2 is however irrelevant as the scaling factor used to scale the acquired data only applies to transient conditions within the integration range as indicated in section 3.8. The post processing discussed in section 7.3 implements digital filtering in order to attenuate the low frequency response of the measured transient waveforms.

Figure 7-2 indicates the quantisizing step size of the acquisition system, which is as result of the small signal level. The small signal level furthermore provides a means

of assessing the noise level by observing the digitisation jitter in the acquired signal. Noise results in random sampling in the vicinity of the actual signal level.

7.2.2 Transient measurement results

This section introduces the transient measurement results obtained in the substation evaluation. As result of the attenuation of the fundamental frequency in the summation and integration circuitry as shown in section 3.7, the transient data is presented together with the CVT secondary voltage. This provides insight into the location of the transient waveform on the fundamental frequency. An instance of an unsaturated acquired transient waveform is shown in Figure 7-3.

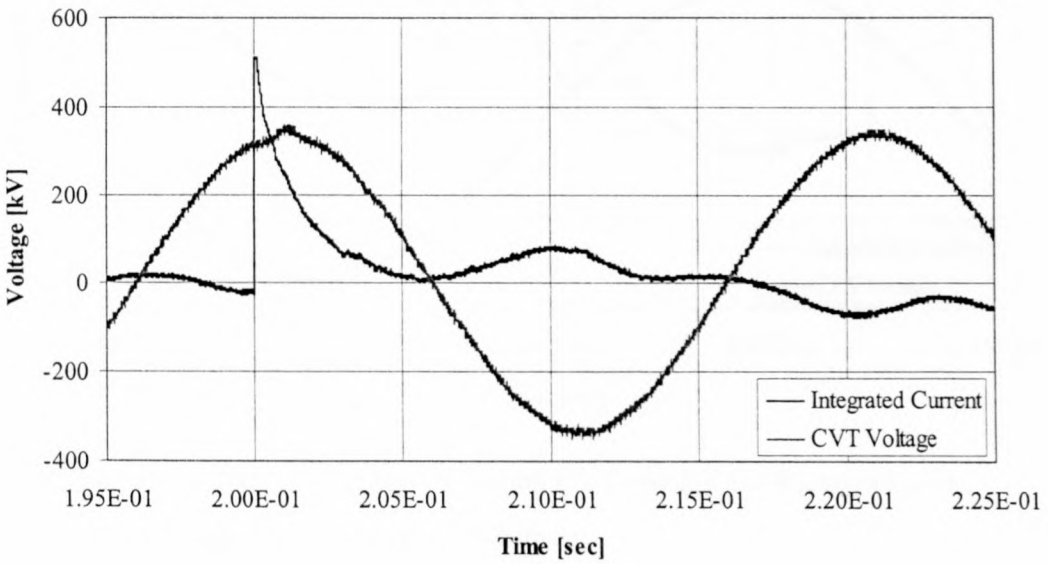

Figure 7-3 Integrated current together with CVT voltage for illustration of unsaturated operation.

Comparison of Figure 7-3 with Figure 7-2 shows the presence of low frequency noise in the integrated current signal. The steep rising slope of the integrated current shown in Figure 7-3 resides in the integration range of the summation and integration circuitry discussed in chapter 3. With respect to the laboratory evaluation of the monitoring system the rising edge and peak value of the impulse transient shown in Figure 7-3 is accepted as valid. The falling edge of the integrated current signal is however irrelevant as the associated frequency response is below the integration range.

Observation of the CVT voltage shown in Figure 7-3 indicates minor deviation from the fundamental frequency in the vicinity of the transient condition. The impulse transient has wideband frequency content, which results in wideband excitation of the CVT. As mentioned previously the bandwidth of the CVT allows measurement of up to the thirteenth harmonic, which result in the waveform shown in Figure 7-3.

Another instance of the transient measurements obtained from the substation evaluation is shown in Figure 7-4.

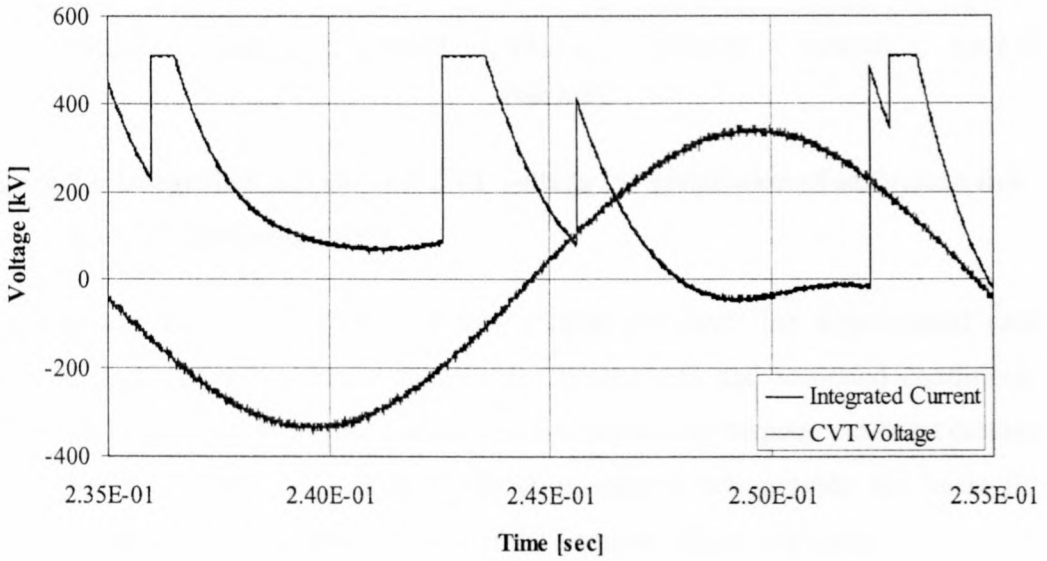

Figure 7-4 Integrated current together with CVT voltage for illustration of saturation due to low frequency content.

This waveform describes saturation as result of unwanted low frequency content present in the summation and integration circuitry. The clipping observed in Figure 7-4 corrupts the integrated current signal as transient information is absent, which is irreversible with post-processing routines.

Observation of Figure 7-5 indicates a transient condition of which the dynamic range exceeded the capability of the summation and integration circuitry.

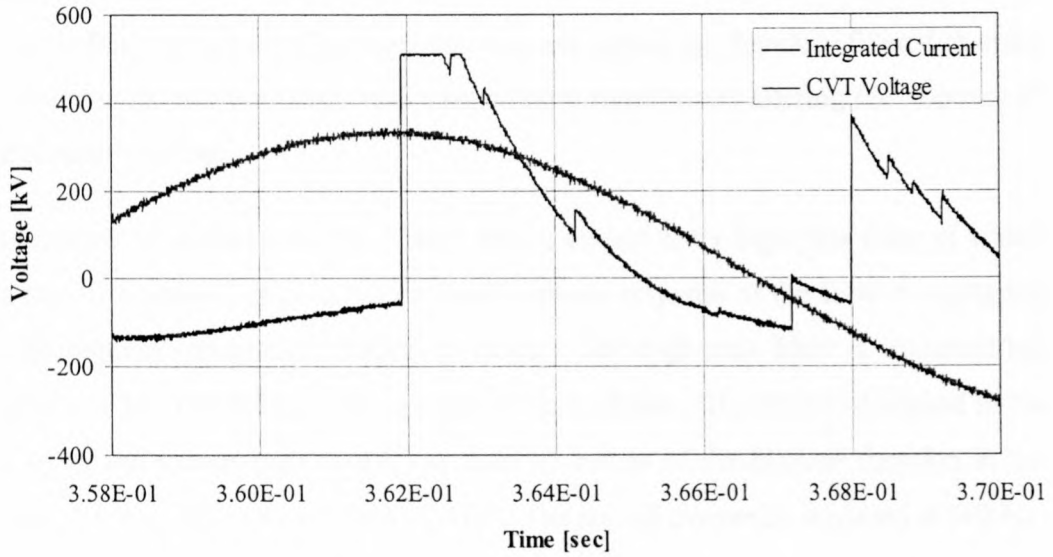

Figure 7-5 Integrated current and CVT voltage for illustration of saturation due to lack of dynamic range.

The transient waveforms shown in this section presented the unprocessed data obtained from the substation evaluation for unsaturated and saturated conditions. Observation of these results may pose an expectancy of low frequency content present in the transient data. This is however inaccurate, which provide the basis for section 7.3 in which the post-processing of the transient data is discussed.

7.3 Post-Processing of the Measured Data

The previous section introduced the CVT phase voltage and integrated current signals. As mentioned previously the attenuation of the fundamental frequency prior to integration discussed in section 3.7 necessitates the acquisition of the CVT secondary voltage in order to obtain the fundamental frequency component upon which the transient waveform is superimposed.

7.3.1 High-Pass Filtering of the Integrated Current Signal

The low frequency content observed in Figure 7-3, Figure 7-4 and Figure 7-5 is as result of the high low frequency gain of the integrator circuit. Low frequency content present in the summated current signal prior to integration is amplified and results in the waveforms shown in the above-mentioned figures. The impulse response of the

integrator shown in Figure 6-21 further alters the low frequency response of the integrated current signal. The integrated current signals are therefore filtered in order to attenuate the low frequency response, without significantly altering the response in the integration range.

The integrated current signal is filtered with a second order high-pass filter of which the cut-off frequency is placed such that the phase response of the filter is negligible in the required integration frequency range. The high-pass filter is implemented digitally in MATLAB® in order to filter the desired data. The filter is designed in the s-domain and transformed to the z-domain by means of the *bilinear* function in the Signal Processing Toolbox of MATLAB®. The cut-off frequency is placed at 500 Hz, which results in reasonable attenuation of the low frequency components without significantly altering the response in the integration frequency range. The gain and phase responses of the high-pass filter are shown in Figure 7-6.

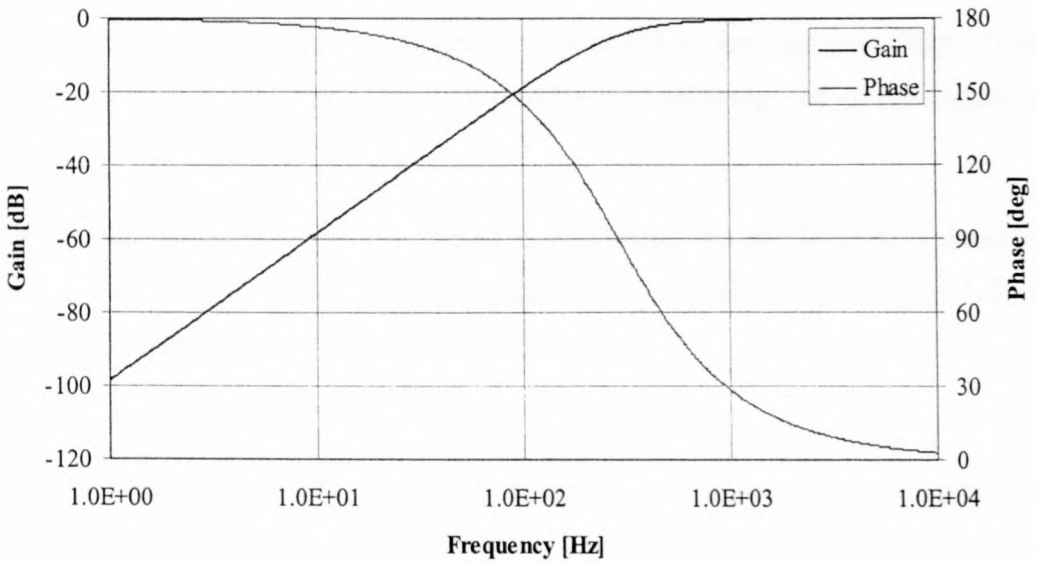

Figure 7-6 Gain and phase responses of the high-pass filter.

The impulse response of the high-pass filter contributes additional low frequency content to the integrated current signal. The normalised impulse response of the second order high-pass filter is shown in Figure 7-7.

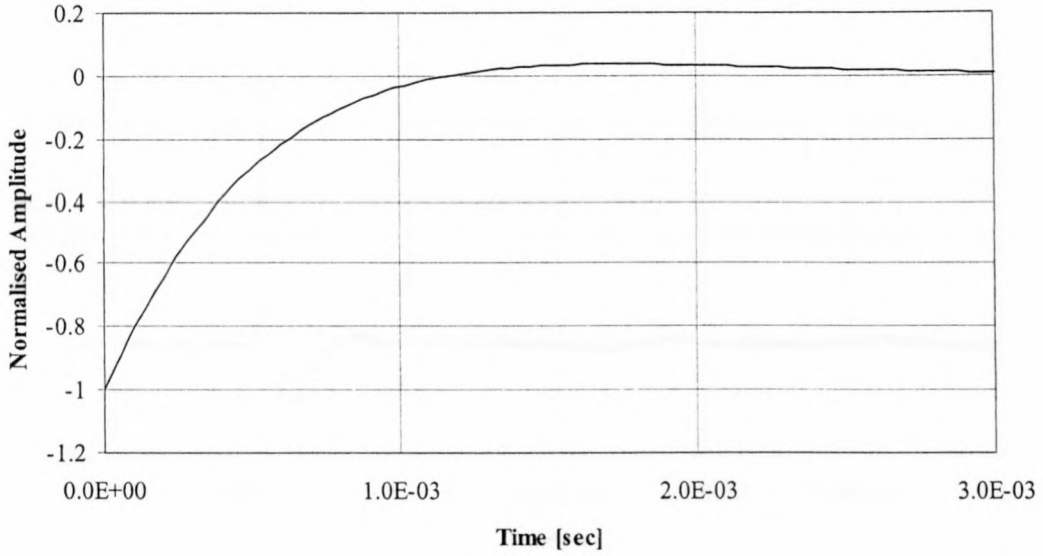

Figure 7-7 Normalised impulse response of the high-pass filter.

The effect of the impulse response of the high-pass filter is less critical as shown in Figure 7-7. The same argument presented in section 6.3.3 for the effect of the summated current signal on the integrator is extended to the high-pass filter. The effect of the impulse response of the high-pass filter on the integrated current signal is minimal.

Saturation introduces non-linearity, which is irreversible by this filtering technique. The high-pass filter is applied to the integrated current signal shown in Figure 7-3 of which the filtered version is shown in Figure 7-8.

Figure 7-8 shows the attenuation of the low frequency content present in the integrated current signal of Figure 7-3. Noticeable is the ringing effect on the falling edge of the integrated current signal, which is characteristic of the impulse response of the high-pass filter. The use of the high-pass filter in order to attenuate the low frequency response of the integrated current signal is effective.

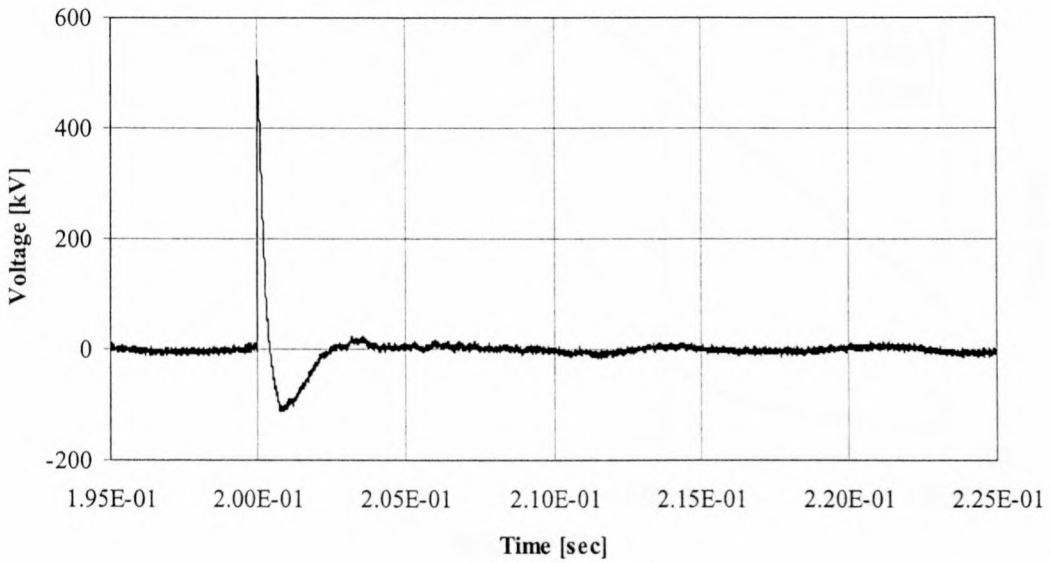

Figure 7-8 Filtered integrated current of Figure 7-3.

The impulse response of the filter, although minimal, contributes to the low frequency response of the integrated current.

7.3.2 Band-pass filtering of the CVT Voltage Signal.

As mentioned previously the CVT has a limited bandwidth of up to approximately 600 Hz. The CVT secondary voltage signal therefore contains harmonic and other low frequency information, which may result in a false perception of the low frequency response when the integrated current signal is superimposed on the CVT secondary voltage. The CVT voltage is therefore filtered in order to obtain the fundamental frequency upon which the integrated current signal is superimposed.

The secondary CVT voltage is filtered using a second order digital band-pass filter of which the centre frequency is situated at 50 Hz. The design of the band-pass filter is similar to section 5.4.2 with Q equal to 1 and ω_c equal to 50 Hz. The gain and phase responses of the band-pass filter is shown in Figure 7-9.

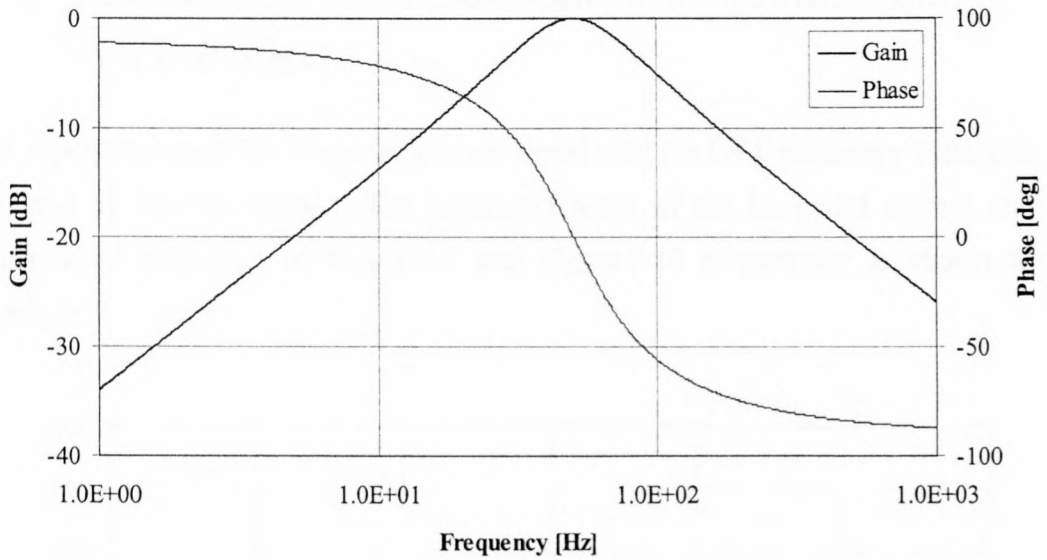

Figure 7-9 Gain and phase responses of the band-pass filter.

The impulse response of the band-pass filter is ignored, as the CVT secondary voltage signal is band limited. The band-pass filter is applied to the CVT voltage of Figure 7-3 and the result is shown in Figure 7-10.

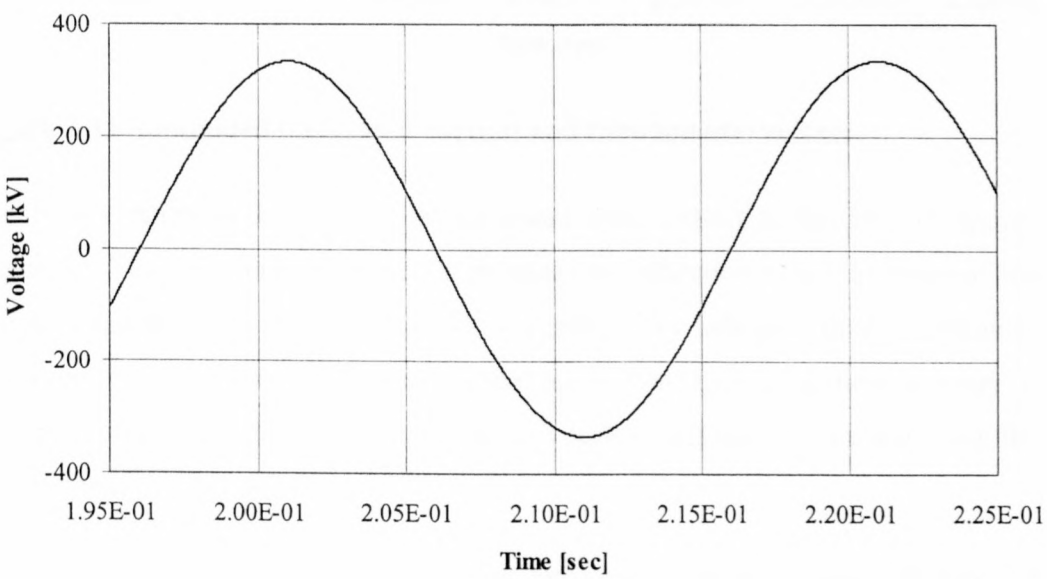

Figure 7-10 Filtered CVT voltage signal of Figure 7-3.

7.3.3 Superposition of the Integrated Current onto the Fundamental Frequency Signal

The superposition of the integrated current signal onto the CVT secondary voltage is obtained by the summation. The summated result of the integrated current and fundamental frequency of Figure 7-8 and Figure 7-10 respectively is shown in Figure 7-11.

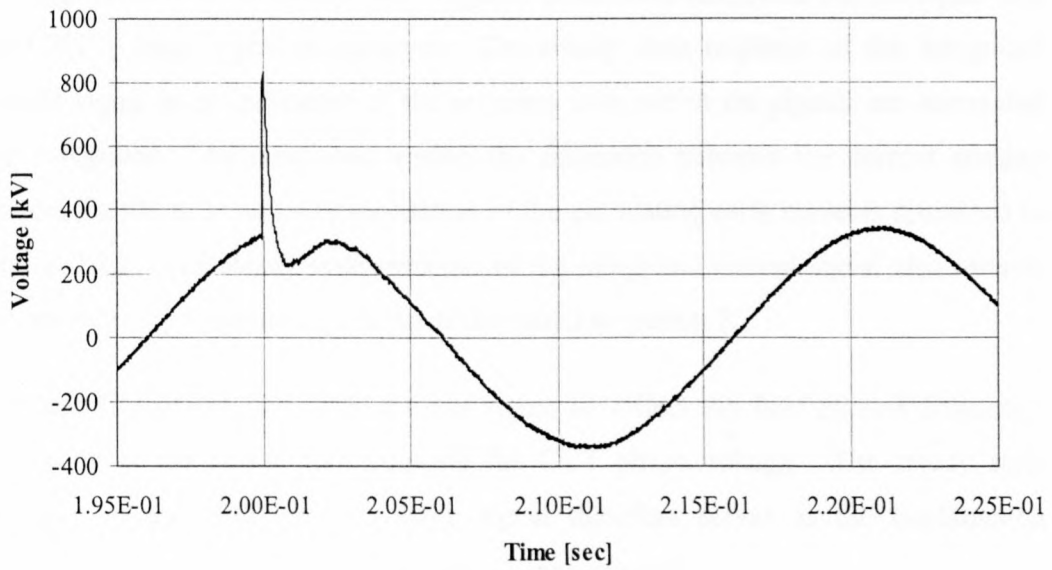

Figure 7-11 Summated integrated current and fundamental voltage.

The interpretation of Figure 7-11 is important with respect to the low frequency response. The superposition principle provides an indication of the location of the transient condition on the fundamental frequency. As indicated in the laboratory measurements discussed in section 6.4 the summation and integration circuitry is accurate in measuring the fast rising edges and peak values and less accurate with the low frequency response.

Section 7.3 presented the process of filtering and superposition for a single instance of the transient data obtained from the substation evaluation. Various instances of the integrated current and CVT voltage is presented in Appendix C, which shows the superimposed waveforms by implementing the process discussed in section 7.3.

7.4 Summary

This chapter presented the substation evaluation of the transient voltage monitoring system. The acquired data is presented in section 7.2 and discussed with reference to the steady state and transient response. The post processing of the acquired data is discussed in section 7.3 and involves the filtering and summation necessary in order to produce a representative waveform.

The significance of the steady state response of both the integrated current signal and the CVT voltage signal is apparent. The steady state response of the integrated current signal is an indication of the accuracy with which the signals are summated and integrated. As mentioned earlier the mismatch between the current sensing devices results in imperfect cancellation of the circulating earth currents discussed in section 2.2.2. The steady state response of the integrated current signal also reflects the noise level present in the system as discussed in section 7.2.1.

The inability of the integrated current signal to reflect the fundamental frequency accurately is the reason for acquiring the CVT phase voltage. The steady state response of the CVT phase voltage signal therefore serves as the fundamental frequency upon which the transient data is superimposed.

The transient response of the integrated current signal and CVT phase voltage signal is shown in section 7.2.2. Saturated and unsaturated instances of the integrated current signal are shown together with the CVT phase voltage. The saturated waveforms indicate lack of dynamic range. The CVT phase voltage is relatively uncorrupted as result of the bandwidth-limited nature of the CVT.

Section 7.3 presents the pinnacle of the thesis, which is the post-processed transient waveforms. The acquired signals are digitally filtered and superimposed in order to produce the complete transient waveform. The effects of the impulse responses of the high-pass and the band-pass filters are discussed in sections 7.3.1 and 7.3.2 respectively and contribute minimally to the low frequency response of the filtered signals.

This chapter concludes the design and evaluation of the transient voltage monitoring facility. The waveforms generated from the practical measurements provide insight

into the severity of transient overvoltage conditions in substation environments and establish a firm ground for further investigation into the effect of such transient conditions on substation equipment and insulation practices.

Chapter 8

Conclusions and Recommendations

8.1 Introduction

This chapter concludes the research conducted with a discussion of the thesis in retrospect as well as recommendations towards future developments. The discussion provides research achievements based on the milestones, which were set at the beginning of this thesis.

The recommendations given in this chapter will provide insight into the future development and implementation of the summation and integration technique.

8.2 Thesis Overview

The aim of this thesis as stated in chapter 1 was the investigation into the feasibility of a non-intrusive wideband transient voltage measurement facility using CTs configured in a transconductance topology. The feasibility of such a system is evaluated with respect to practical implementation, measurement accuracy and versatility.

8.2.1 Implementation

The advantage of the CT configured in a transconductance topology is the non-intrusive nature of transient voltage measurements. The secure earthing arrangements of the CTs are maintained and therefore the monitoring system is installed and operated under normal operating conditions. The proposed monitoring system described in section 2.3 provides a simple implementation strategy for medium to long term transient voltage monitoring.

The transient voltage monitoring system consists of a summation and integration stage, an optical isolated digital link for signal transfer and a data acquisition system with a user configurable interface. The detailed design and implementation of the above mentioned subsystems are discussed in chapters 3, 4 and 5.

Research indicates that the CT capacitance is stable up to approximately 500 kHz. The capacitive current as result of transient voltage conditions across the CT capacitance is sensed in the multiple earth paths of the CT. The individual current signals are summated and integrated in order to produce a representation of the transient phase voltage. Magnetic coupling from neighbouring transmission lines results in circulating currents being present in the multiple earth paths. The amplitude of the circulating current is in excess of several amperes. These circulating currents are however cancelled by the summation process although minor mismatch between the sensing devices results in substantial low frequency content present in the resulting current signal. As result of the high low frequency gain of the integrator the resultant current signal is filtered in order to attenuate the fundamental frequency. The integrated current signal therefore represents the transient voltage in the frequency range of approximately 1 kHz to 100 kHz.

The integrated current signal is transmitted to the data acquisition system by means of a digital optical isolated link. The link employs optic fibre, which has high bandwidth and is immune to electrical interference, which is synonymous with substation environments. The digital transfer of signals enables high signal to noise ratios and simplifies system design.

The data acquisition system serves the purpose of detecting transient conditions as well as the logging of transient data. The data acquisition system consists of a commercial computer based data acquisition card with supporting analog trigger circuitry. The acquisition system has a user configurable software interface in order to select data acquisition parameters. The acquired transient data is bundled with time stamping information in order to correlate with logged activities. The data acquisition system acquires both the integrated current signal as well as the CVT secondary phase voltage.

8.2.2 Measurement Accuracy

The CT capacitance is exploitable in two configurations namely in a capacitive divider and transconductance topology. Research indicates that the capacitive divider topology yields accurate measurements across extended bandwidth. This topology however requires that the secure earthing arrangement of the CT be altered in order to establish a capacitive divider configuration.

The transconductance topology provides a means of conducting wideband voltage measurements without alteration of the CT earthing arrangement. This method however is less accurate as result of the wide dynamic range requirement imposed on the integrator circuitry. The accuracy of the integrated current signal is dependent on both the current sensing accuracy and the integration accuracy.

Accurate measurement of the capacitive current requires the implementation of wideband current sensing devices. The multiple earth paths furthermore require accurate summation for cancellation of the circulating earth currents. Commercial wideband current sensing devices consists of Hall effect sensors in conjunction with current transformers. The Hall-effect sensor is responsible for the low frequency and the current transformer for the high frequency measurements. Using special amplifiers these wideband current sensing devices are conditioned in order to obtain a flat frequency response. These current sensing devices and amplifiers are extremely expensive and are beyond the scope of this thesis.

The geometry of the earthing conductors is not identical and necessitates the implementation of current sensing devices with different geometries. The gain and phase responses of these devices are therefore not identical, which results in minor signal mismatch at lower frequencies. The current path created by the secondary cable armouring earthed in the relay room represents high impedance during transient conditions as result of the high inductance due to the long cable length. The transient capacitive current in the secondary cable armouring is therefore small compared to the current in the earth straps. The inaccuracy of the clamp-on current transducer at high frequencies is therefore negligible.

The integrator is accurate in the specified integration range of 1 kHz to 100 kHz. The frequency range below 1 kHz is not suitable for integration purposes and an inaccurate response is obtained. The laboratory evaluation discussed in chapter 6 shows high accuracy of the summation and integration circuitry for higher frequencies. The low frequency response is however of less importance as the accurate measurement of high amplitude transient voltages is necessary to establish the effect of transient overvoltage conditions on substation equipment. The accuracy of the summation and integration circuitry is therefore adequate for transient voltage measurement.

8.2.3 Versatility

The versatility of the transient voltage monitoring system is enhanced by the optical link and data acquisition system. These components enable ease of operation under stringent conditions.

The use of the isolated optical link is advantageous as result of its electrical immunity, lightweight and durable construction and wideband measurement capability. The immunity of optical fibre against electrical interference makes it suitable for operation in electrically noisy environments with respect to signal preservation and safety. Signal to noise ratios are increased with the use of optical fibre rather than copper wire for signal transfer as signals are not influenced by electrical noise. The isolation of measurement instrumentation further protects operating personnel from injury as result of electrical shock.

The isolated link is operable across great distances as result of low signal attenuation and lightweight design, which creates implementation versatility as measurements can be conducted across distances spanning several kilometres without additional hardware. The lightweight and durable construction of optical fibre is operable in virtually any environmental condition and increases the mobility of the isolated link.

The data acquisition system enables the detection and logging of transient signals. The entire data acquisition system is user configurable by means of a Graphical User Interface (GUI). The control software is adaptable for future upgrade and provides support for built-in post-processing routines.

8.3 Recommendations

The research conducted during this thesis produced a HV transient voltage monitoring system, which achieved the design requirements stated in the objectives of this report. During the design and practical evaluation of the monitoring system certain aspects emerged which requires further investigation towards improved operation. This section presents the enhancements recommended in order to improve measurement accuracy and ease of operation. The recommendations are presented for each individual stage of the HV transient monitoring system.

8.3.1 Current Sensing

8.3.1.1 Leakage Current

The HV CT is situated in an environment, which is exposed to cyclic weather conditions that results in deposits accumulating on the CT insulation. These deposits provide a conductive medium, which results in leakage current. The magnitude of the leakage current depends on the conductance of the deposits, which is dependent on the geographical location of the CT. Figure 8-1 shows the HV CT indicating the deposits accumulating on the CT insulation. The leakage current is represented by $i_l(t)$.

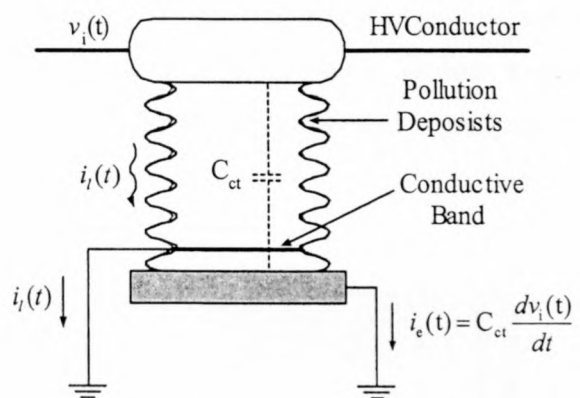

Figure 8-1 Leakage current due to deposits accumulating on the CT insulation.

The leakage current was ignored for the purpose of this research although future upgrade of the system should include sensing of the leakage current. The eradication

of the leakage current is obtained by providing a separated current path for the leakage current as shown in Figure 8-1.

8.3.1.2 Design of a Universal Current Sensing Topology

As mentioned earlier the current sensing devices used for each earth current path is dissimilar in construction as result of the geometry variation of the individual earth path conductors. The differences in gain and phase responses of the split-core CTs and the clamp-on current transducer produces inaccuracies during the summation process.

The current sensing topology should consist of a single current sensing device, which is capable of incorporating various conductor geometries. Identical current sensing devices will result in matched gain and phase responses and improved accuracy during the summation process. The input stages on the summation and integration circuitry are therefore identical and result in matched gain and phase responses for each channel.

8.3.1.3 Bandwidth Extension for the Split-Core CT

The bandwidth of the current sensing devices should be increased in order to measure the earth current more accurately. This is accomplished by extending the core composition used for the split-core current transformers to laminations of the existing core material and an iron core in order to extend the low frequency response of the split-core CT. Figure 8-2 shows the suggested arrangement for extending the bandwidth of the measurement CTs.

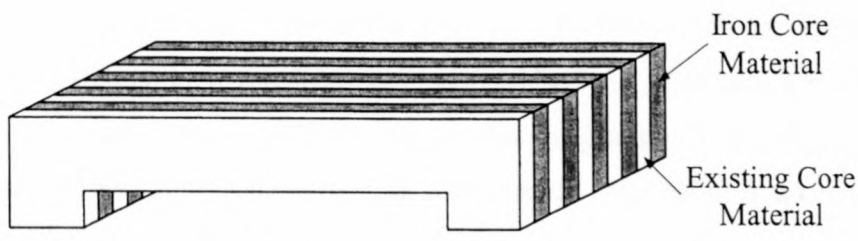

Figure 8-2 Indication of laminations for one half of the measurement CT.

The design should ensure a flat response in the transitional area of the frequency response. Improvement of the low-frequency response results in more accurate cancellation of the circulating earth current during the summation process.

8.3.1.4 Weather protection

The practical substation evaluation of the HV transient voltage monitoring system revealed corrosion of the current sensing devices as result of extreme weather conditions. This is problematic as the frequency response of the split-core CTs is affected as result of corrosion of the core material. Furthermore, the split-core CT may be damaged under transient conditions if the insulation of the CT windings is damaged. The upgrade of the split-core CT should provide a robust and watertight enclosure for protection against extreme weather conditions.

8.3.2 Summation and Integration Circuitry

8.3.2.1 Band-stop Filter

The employment of identical current sensing devices for each earth current path results in a summated current signal of which the circulating current component is virtually non-existent. The band-stop filtering of the summated current signal at the fundamental frequency is therefore unnecessary. The impulse response of the band-stop filter is eliminated and less noise is contributed to the summated current signal.

8.3.2.2 Integrator

The integration range of the integrator should be expanded in order to accommodate the frequency range from 500 Hz to 500 kHz. As stated previously the dynamic range requirement imposed on the integrator as result of the wideband specification is severe and necessitates careful design of the integrator. Lowering the cut-off frequency and DC gain of the integrator increases the integration frequency range as shown in Figure 8-3.

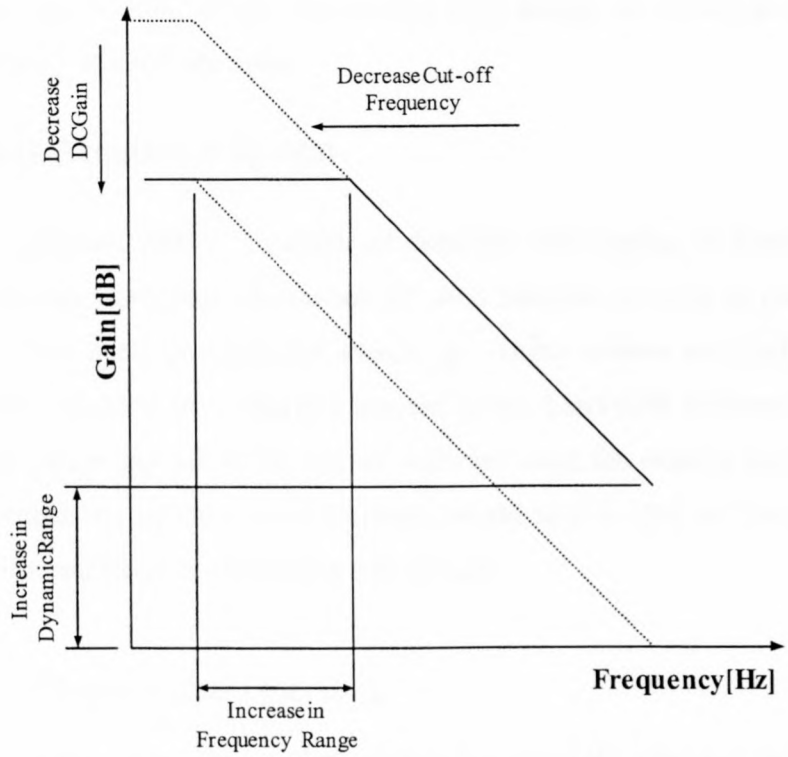

Figure 8-3 Modification of the integrator to increase frequency range.

The amplitude of the impulse response of the integrator is consequently smaller as result of lower high-frequency gain. This contributes to more accuracy in the lower frequency response of the integrator output.

The design of the integrator should exclude the AC coupling circuit as shown in Figure 3-14. Proper design of the summation and integration circuitry using operational amplifiers with low DC offsets eliminates the need for the AC coupling circuit.

8.3.2.3 General Design Enhancements

The implementation of low noise wideband operational amplifiers together with surface mount resistors and capacitors will assist in achieving the desired frequency response and signal-to-noise ratio. The design and layout of the Printed Circuit Board (PCB) used for population of the circuit components should be carried out using a four-layer instead of a two-layer board. The two outer layers of the four-layer board is utilised for component interconnection and the two inside layers are designed to be used as a ground and power plain respectively. The significance of the ground and

power plains are twofold in that it simplifies PCB design and it acts as a screening medium in order to attenuate noise.

8.3.3 Data Acquisition System

The data acquisition system is capable of detection and logging of transient signals and provides time-stamping information for each transient in order to correlate with logged activities such as controlled switching. These actions are configurable by means of the graphical user interface created in the LabVIEW environment, which supports the future upgrade of the control software using the existing hardware. The functional capability of the control software should be extended in order to support the features presented in the following subsections.

8.3.3.1 Enhanced User Operation

The control software as discussed in section 5.5 currently supports only repetitive logging. The extension of the control software to include single logging, single viewing and continuous viewing is desired to establish a versatile data acquisition system.

Viewing of the integrated current signal requires implementation of a software oscilloscope, which is supported by the LabVIEW design environment. The oscilloscope feature enables an operator to assess the state of the integrated current signal on a single shot or continuous operation basis. Single shot operation provides a visualisation of the integrated current signal in a predefined time period whereas continuous operation continuously updates the predefined time window to provide continuous viewing.

Viewing of the acquired data is desired during installation and operation. Installation of the transient voltage monitoring system requires various verification procedures such as polarity checking of the current sensing devices, which is facilitated by means of visual feedback. Satisfactory operation of the monitoring system is verified by observation of the visual feedback.

8.3.3.2 Built-in Post-Processing Routines

The digital data logged by the data acquisition system requires post-processing in order to obtain the actual transient voltage. The post-processing as discussed in section 7.3 involves the filtering, scaling and summation of the digital data in order to provide presentable waveforms.

The VI library of LabVIEW consists of various digital signal-processing routines, which is capable of processing the acquired data in order to perform filtering, scaling and summation in real time. This is advantageous as the data is immediately available for viewing purposes.

8.3.3.3 Network Connectivity

The management of information from various HV transient monitoring systems situated in far apart locations is time consuming and expensive as frequent visits to these locations are necessary in order to gather the required information.

The implementation of network connectivity in order to communicate with the various monitoring systems is desired to increase productivity. The LabVIEW design environment provides TCP/IP connectivity components for incorporation into the existing software. The TCP/IP components is interfaced with standard modems in order to establish a dial-up connection and may even be extended to cell-phone technology for remotely located monitoring systems

The dial-up connection may be used to download information from the selected monitoring system at regular intervals or the monitoring system may respond with a request after each transient condition.

8.3.3.4 Functional Extension for Fault Location Applications

The transient voltage monitoring system detects a transient condition upon which the transient data is logged. Upon detection of the transient condition a digital trigger signal is generated as discussed in section 5.4. This trigger signal prompts the data acquisition card to acquire the desired analog signals.

The trigger signal may also be interfaced to a Global Position System (GPS) fault location system [48, 49]. The GPS fault location system is equipped with a GPS receiver receiving a very accurate one-pulse-per-second (1PPS) synchronisation signal. The system maintains time information accurate to 1 μs, which can be used to determining fault locations. Upon detection of a transient condition the GPS fault location system log the exact time of the transient. The exact time on both ends of a transmission line is utilised to calculate the location of the fault accurate to 300 m [48].

8.4 Closing Remarks

The design, implementation and evaluation of the HV transient monitoring system discussed in this thesis proved successful although certain criteria requires further investigation. The non-intrusive method of transient voltage measurement utilising the substation CT configured in a transconductance topology holds vast potential for wideband measurement activities.

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Appendix A

NI 5102 Data Acquisition Card

A.1 Block diagram of the NI 5102

The NI 5102 PCI, which is a computer based high-speed digitiser card from National Instruments performs the data acquisition. A simplified block diagram [38] describing the NI 5102 is shown in Figure A-1. The operation of the NI 5102 is discussed in the following subsections with respect to the block diagram given in Figure A-1.

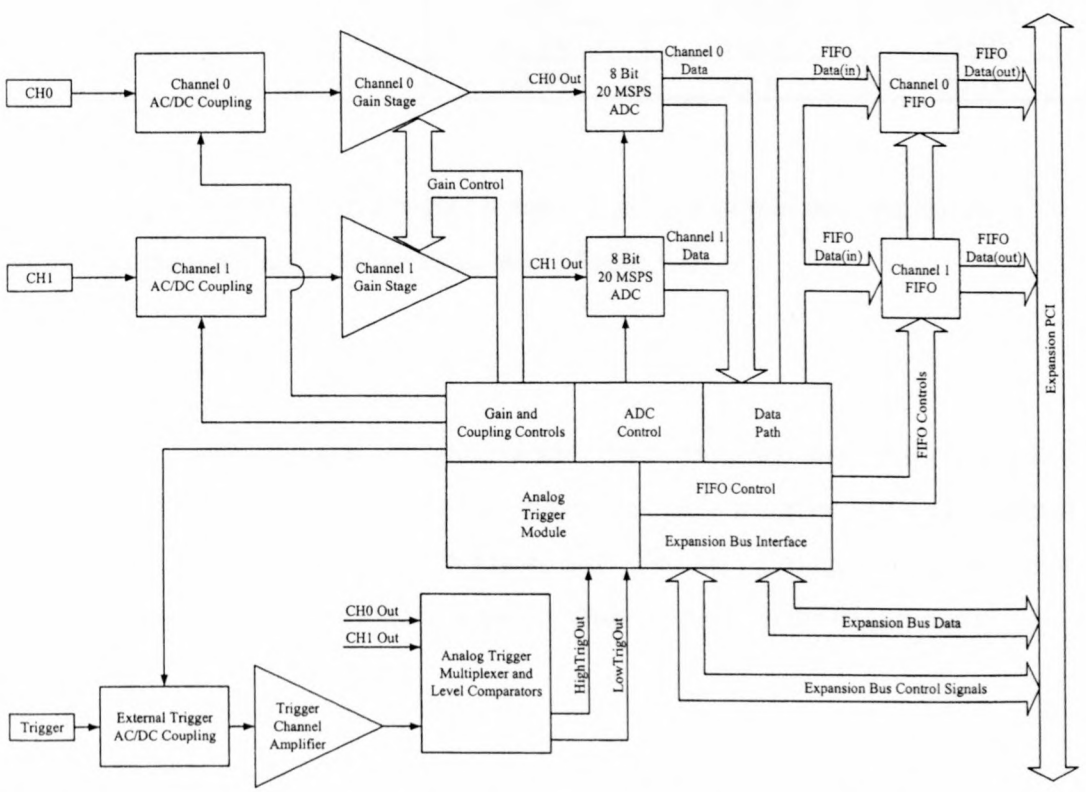

Figure A-1 Simplified block diagram of the NI 5102 Data Acquisition card.

A.2 Input Coupling and Gain Control

Figure A-1 shows that the NI 5102 has two analog input channels and an external trigger input. The coupling of each input channel and the trigger channel can be set to either DC or AC. Signals with a large DC and small AC component is difficult to measure using DC coupling. AC coupling removes the DC component from the signal leaving only the small AC component.

The gain stage for both analog input channels provides amplification in order to measure small signals. The available range of values for the gain stage is shown in the first column of Table A-1. The measurement of larger signals is possible with the use of voltage probes with various attenuation factors. The input ranges for different gains and probe attenuations is shown in Table A-1.

Table A-1 Table of analog input voltage ranges.

Gain	Input Range [V]			
	X1 Probe	X10 Probe	X100 Probe	X1000 probe
1 (Default)	+5V	+50V	+500V	+5000V
5	±1V	±10V	±100V	±1000V
20	±0.25V	±2.5V	±25V	±250V
100	±50mV	±0.5V	±5V	±50V

The gain stage for the external trigger input is fixed at a gain of one and results in the corresponding input range values as shown in Table A-1.

A.3 Triggering

The external trigger signal is multiplexed with both analog input signals to provide a selectable trigger source. The selected trigger source is compared to a pre defined high and low level value as shown in Figure A-2. The analog trigger circuit processes the high level and low level trigger outputs in order to produce the trigger signal.

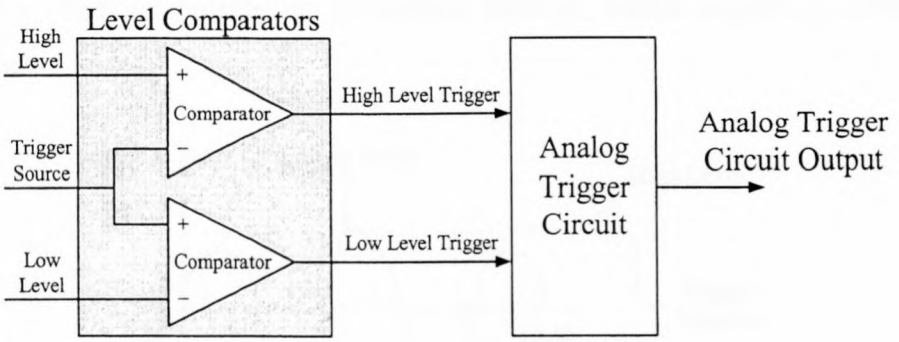

Figure A-2 Block diagram of the trigger generation.

There are three trigger modes in which the NI 5102 can operate namely edge, window and hysteresis. These modes are implemented in the analog trigger circuit as shown in Figure A-2.

The first trigger mode is edge triggering and is used to generate a trigger condition by the rising or falling edge of the trigger source past a predefined value. Figure A-3 shows an example waveform with negative-edge triggering. The analog trigger circuit monitors the high or low-level trigger outputs and generates a trigger if a valid edge is detected. This is typically used for the triggering of repetitive signals typically used in oscilloscopes.

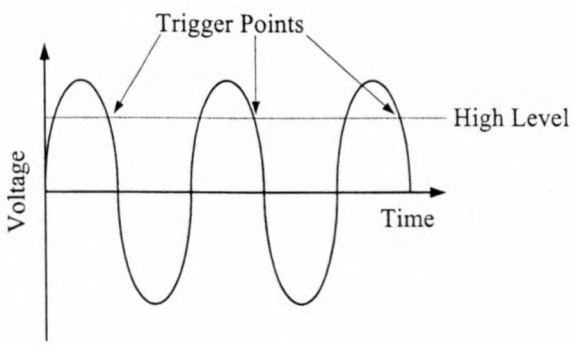

Figure A-3 Example waveform indicating falling-edge triggering.

The second trigger mode is window triggering and is used to detect signals leaving or entering a predefined window. This type of triggering is useful to detect isolated occurrences, which do not repeat at regular intervals. The window is constructed from the high- and low-level trigger values and a trigger condition is generated in the analog trigger circuit. The waveform shown in Figure A-4 exhibits an irregular

transient condition outside the predefined window, which triggers an acquisition sequence.

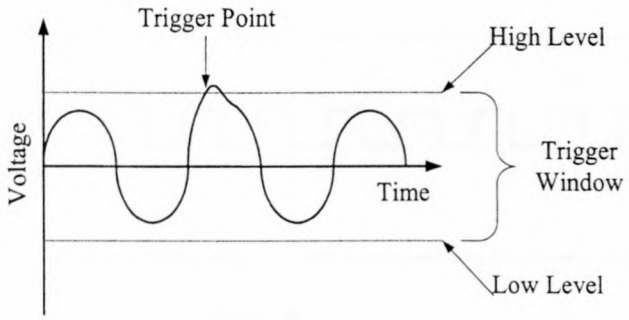

Figure A-4 Window triggering with the signal leaving the predefined window.

The third trigger mode is hysteresis triggering, which is generally used for noisy trigger sources to prevent false triggering. Hysteresis triggering is similar to edge-triggering with the only difference that in this topology the preset trigger value is shifted upon detection of a valid trigger condition in order to avoid triggering as result of rapid transitions in the vicinity of the trigger level. Figure A-5 shows that upon detecting a valid rising edge the trigger source signal is required to fall below a preset threshold value (represented by the low level trigger value) in order to be accepted as a valid rising edge. This topology is also applicable to falling-edge triggering.

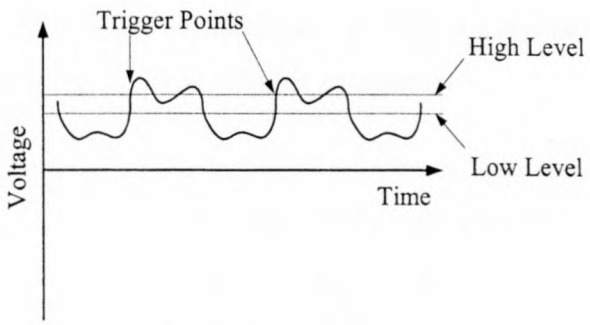

Figure A-5 Hysteresis triggering using the rising edge.

A.4 Data Acquisition Modes

The NI 5102 is capable of two acquisition modes namely, pre- and post-trigger acquisition, which is software selectable. Post-trigger acquisition acquires a predefined amount of samples after a trigger condition occurs. Figure A-6 shows the

internal signals used for post-trigger acquisition as implemented in the ADC control unit shown in Figure A-1. The amount of post-trigger data is eight samples.

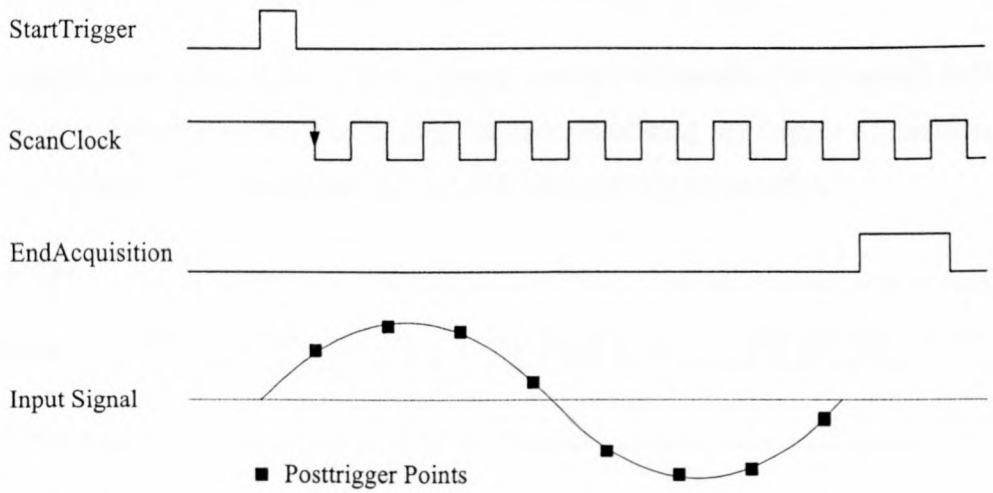

Figure A-6 Timing diagram describing post-trigger data acquisition.

The StartTrigger pulse initiates an acquisition sequence. This can be generated by software or CH0, CH1 and TRIG as indicated in Figure A-1. The ScanClock pulse causes the ADC to convert the input signal to digital data. The input data is sampled at 8-bit resolution. The ScanClock signal is generated internally by a 24-bit counter, which is clocked by a 20 MHz signal in order to generate pulses ranging from 20 MHz to 1.19 Hz. The EndAcquisition pulse signals the end of the acquisition sequence. The EndAcquisition signal is generated from a counter that keeps track of the amount of samples left in the acquisition sequence.

The data obtained from the analog to digital converters is stored in memory modules known as First-In-First-Out (FIFO) memory. The FIFO memory is controlled by the FIFO control module shown in Figure A-1 and enables real time data transfer between the NI 5102 and the computer memory via the PCI bus.

The amount of data that is sampled during an acquisition is not dependent on the on-board memory as data is transferred via the PCI bus to the computer memory in real time without losing data. The onboard FIFO memory is capable of storing 663000 data samples, which results in 331500 samples per channel. The real-time transfer of data via the PCI bus extends the acquisition length to 16 million samples per channel depending on available computer-memory.

The PCI bus is managed by the expansion PCI interface consisting of the expansion bus data and control lines as indicated in Figure A-1. The acquired data is interfaced to the computer PCI bus by means of the FIFO memory topology.

Pre-trigger acquisition requires that a preset amount of samples be acquired before and after a trigger occurs. The timing diagram describing pre-trigger acquisition is shown in Figure A-7 with six pre-trigger and four post-trigger samples.

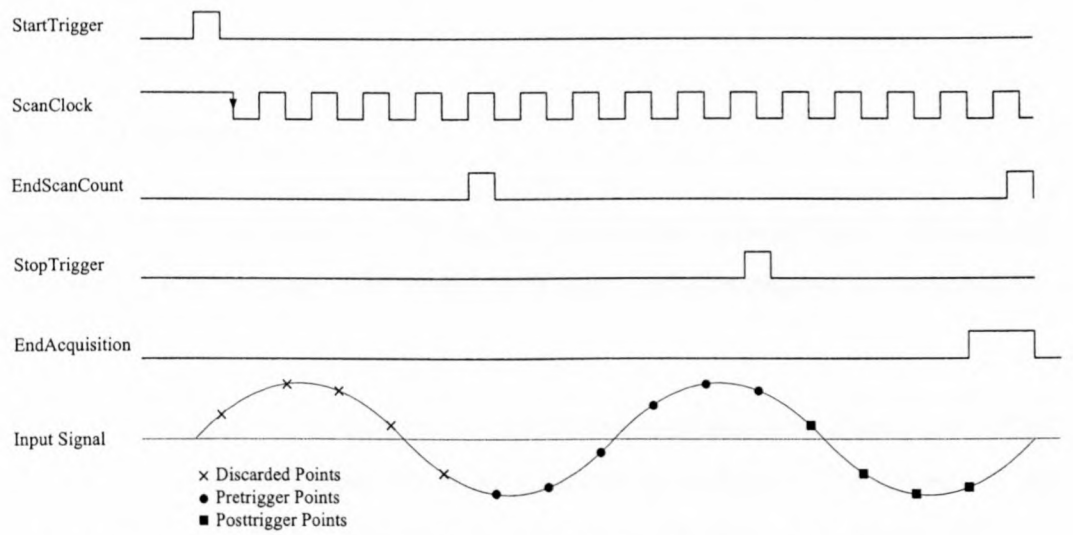

Figure A-7 Timing diagram describing pre-trigger data acquisition.

As shown in Figure A-7 the StartTrigger pulse enables the storage of the pre-trigger data in the FIFO memory. In pre-trigger mode the StartTrigger pulse can only be generated by software and not by CH0, CH1 or TRIG as is the case with post-trigger acquisition. The pre-trigger data is stored in a circular buffer in the onboard FIFO memory with the newest samples overwriting the oldest. The length of the circular data buffer is equal to the acquisition length for the pre-trigger data. The amount of pre-trigger data is limited to the size of the onboard memory. This implies that up to 663000 samples for one channel and 331500 samples for both channels can be stored. The ScanClock signal serves the same purpose as explained for post-trigger acquisition. EndScanCount is an internal signal, which pulses each time the pre-trigger sample count is met. The StopTrigger pulse stops the storage of pre-trigger data to onboard memory and starts to acquire the post-trigger data. The EndAcquisition pulse terminates the entire acquisition sequence.

Appendix B

LabVIEW

B.1 Overview

Appendix A introduced the NI 5102 digitiser device on hardware level. Appendix B describes the implementation of the NI 5102 using software created in the LabVIEW environment.

LabVIEW is a graphical design environment used to create control software for the various digitiser devices available from National Instruments. The control of the NI 5102 is accomplished through various software layers as shown in Figure B-1.

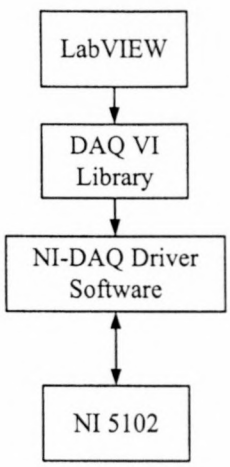

Figure B-1 Software layers for control of the NI 5102.

The NI-DAQ driver software contains all of the device drivers necessary to program and control the NI 5102 via the PCI bus. The NI-DAQ drivers are accessed by means of Virtual Instruments (VIs), which are the building blocks used to create the control software.

The NI 5102 is controlled programmatically by creating a specific application in LabVIEW or interactively by using the oscilloscope software NI-SCOPE, which is also created in LabVIEW and supplied by the manufacturer. NI-SCOPE is in essence a computer-based oscilloscope and supports various digitiser devices and standard oscilloscope functions. The use of NI-SCOPE for general applications is in order although specific tasks require tailor made software using the LabVIEW environment.

B.2 LabVIEW Design Environment

LabVIEW is a graphical programming environment used to create application-specific software to control various digitiser devices. The programming environment comprises two components namely the control and diagram window. The visual interface is designed in the control window and the operational implementation, which is not visible to the user in the diagram window. Figure B-2 shows an instance of the control window environment.

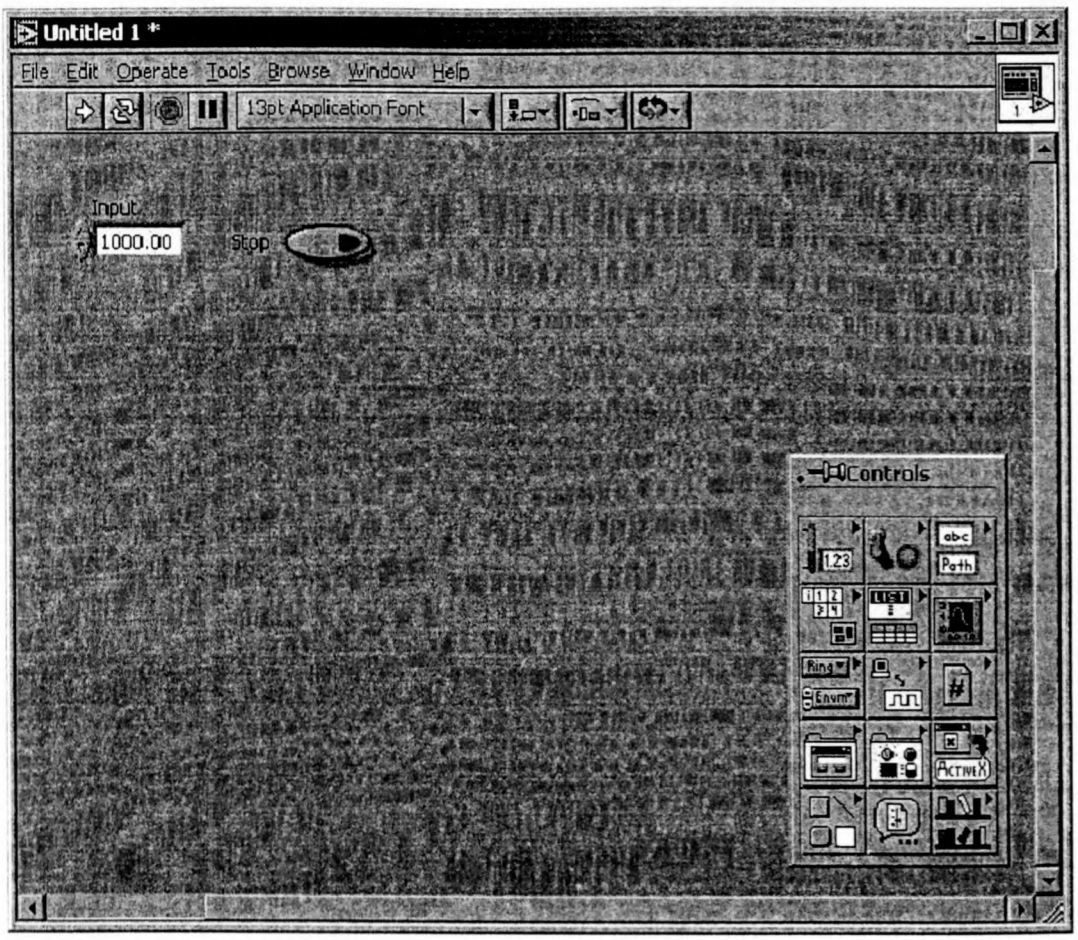

Figure B-2 Example of the Control window environment.

The control window environment creates the visual controls in order to control the digitiser device. These controls include buttons, dials, indicators and drop-down lists as shown in Figure B-2. The individual components are chosen from the control toolbar at the bottom right of Figure B-2 and placed in the working area. The button can be pressed by the mouse pointer and represents the feel of an actual instrument. The states that the button represents are relayed to the diagram window environment shown in Figure B-3.

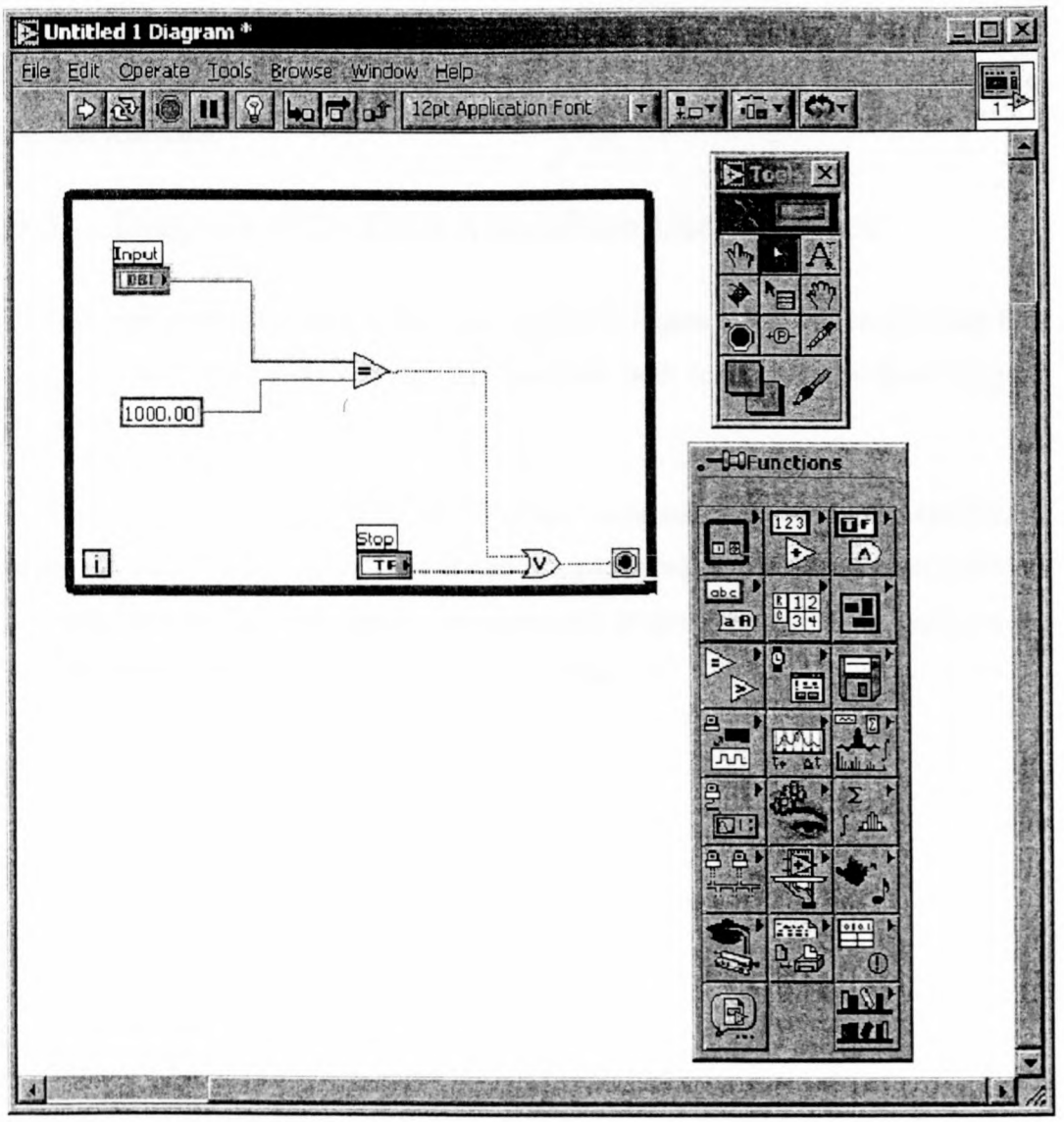

Figure B-3 Example of the diagram window environment.

Observation of Figure B-3 indicates a functions palette from which functional components are chosen which is not visible in the graphical user interface. These functions perform mathematical procedures, interact with data acquisition hardware

and provide network connectivity. Other functions exist which is dependable on the LabVIEW version.

The button named "input" shown in Figure B-2 represents a Boolean variable of either true or false which is used to change some of the parameters of the functional blocks not visible to the user. The functional blocks are known as virtual instruments (VI) and are chosen from the DAQ VI library. Figure B-3 shows an example of a simple VI, which continuously compares the input with 1000 and stops if the result is true. Pressing the Stop button also terminates the VI. These virtual instruments perform the actual operations and are set-up and controlled by the data retrieved from the user interface.

B.3 Diagram of the Data Acquisition User Interface

The diagram implementation of the control GUI of Figure 5-9 is shown in Figure B-4, which shows the operation of the user interface with respect to the block diagram shown in Figure 5-8.

Creating groups of functionality, which is known as sub-VIs reduces the complexity of the diagram. These sub-VIs are edited in separate windows and are represented by a single symbol with the appropriate input and output signals. This improves the readability and simplifies alteration of the diagram.

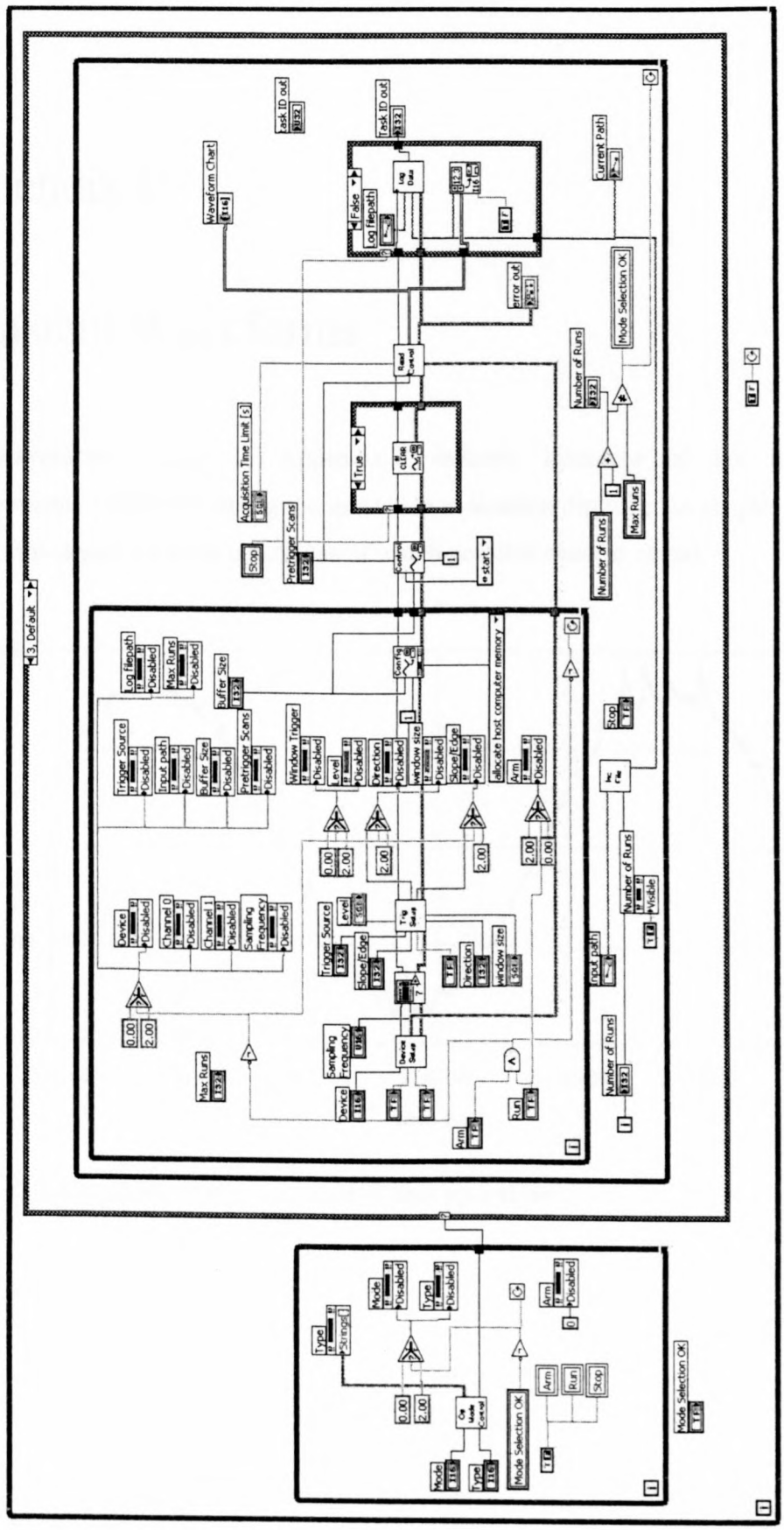

Figure B-4 LabVIEW diagram for the data acquisition user interface.

Appendix C

Transient Waveforms

The waveforms shown in Appendix C indicate instances of the transient measurements conducted during the substation evaluation discussed in chapter 7. The waveforms depict transient conditions of which possible cause is stated.

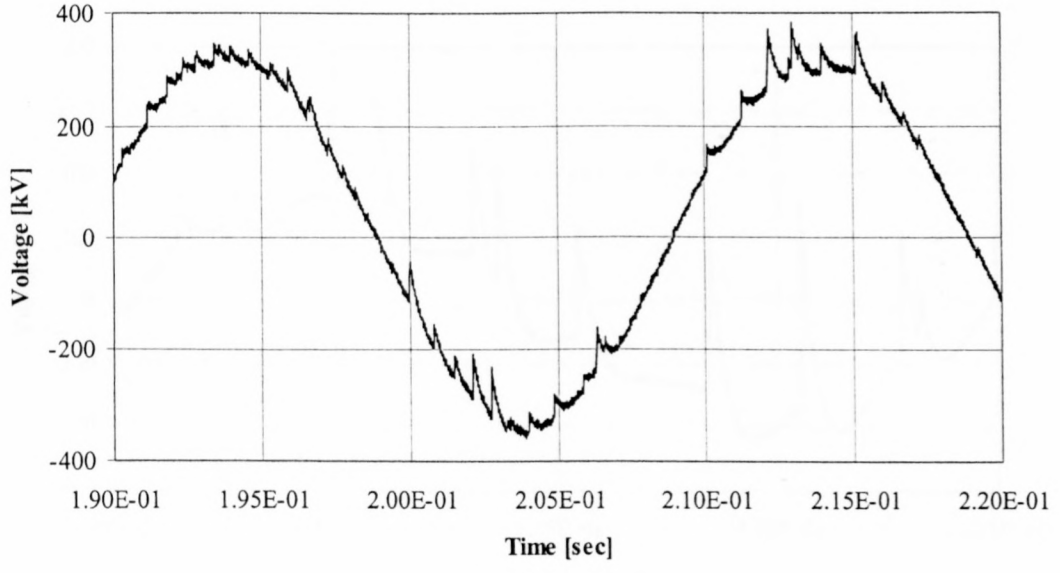

Figure C-1 Possible restrike as result of link operations.

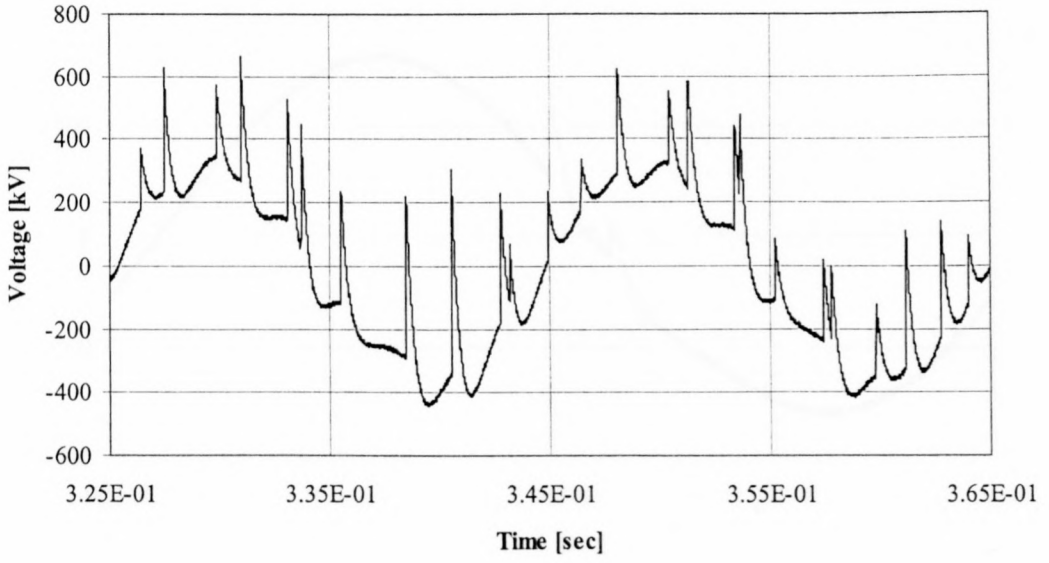

Figure C-2 Possible restrike as result of link operations.

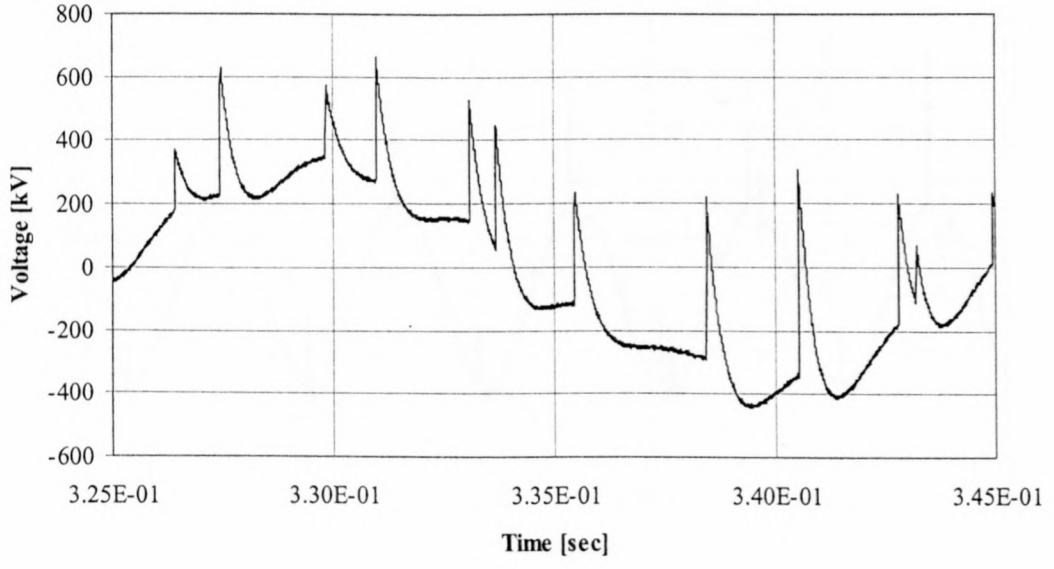

Figure C-3 Possible restrike as result of link operations.

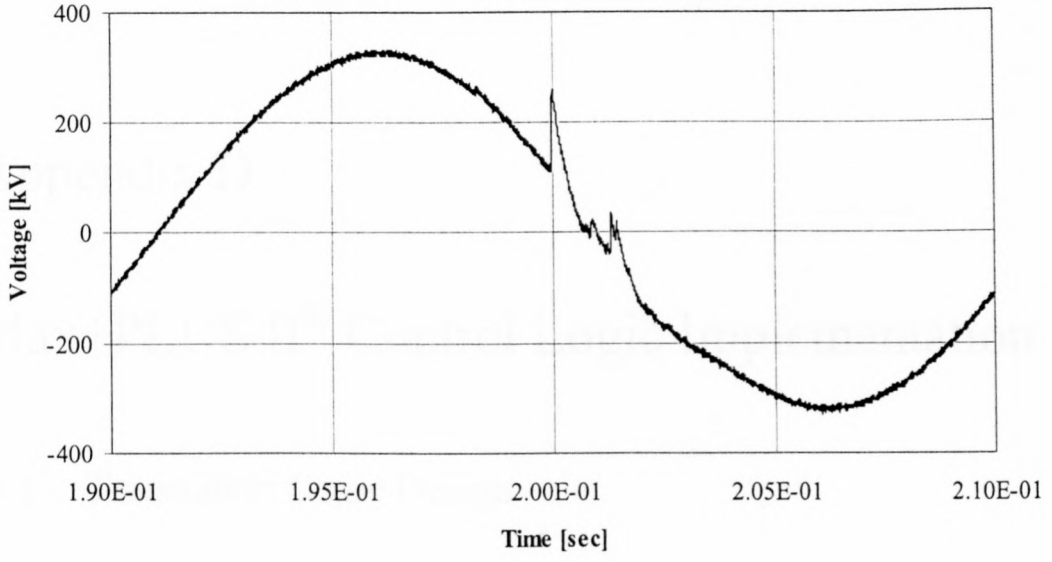

Figure C-4 Transient as result of possible breaker operation.

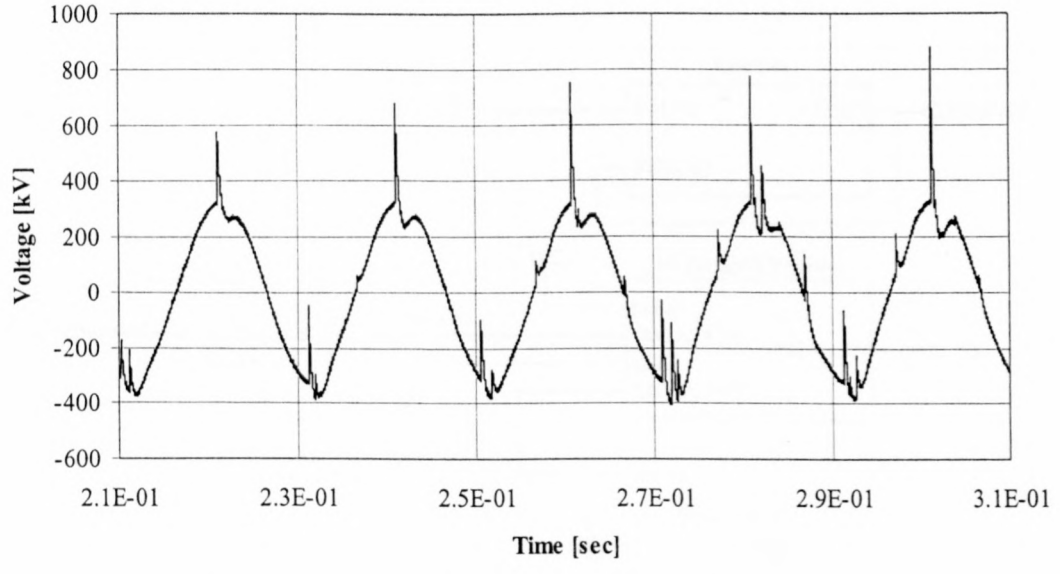

Figure C-5 Possible restrike as result of link operations.

Appendix D

Max+PLUS II® Control Logic Implementation

D.1 Transmitter Logic Design

This section presents the design of the transmitter unit control logic that includes the control for the ADC and the parallel to serial conversion. The main design diagram is shown in Figure D-1.

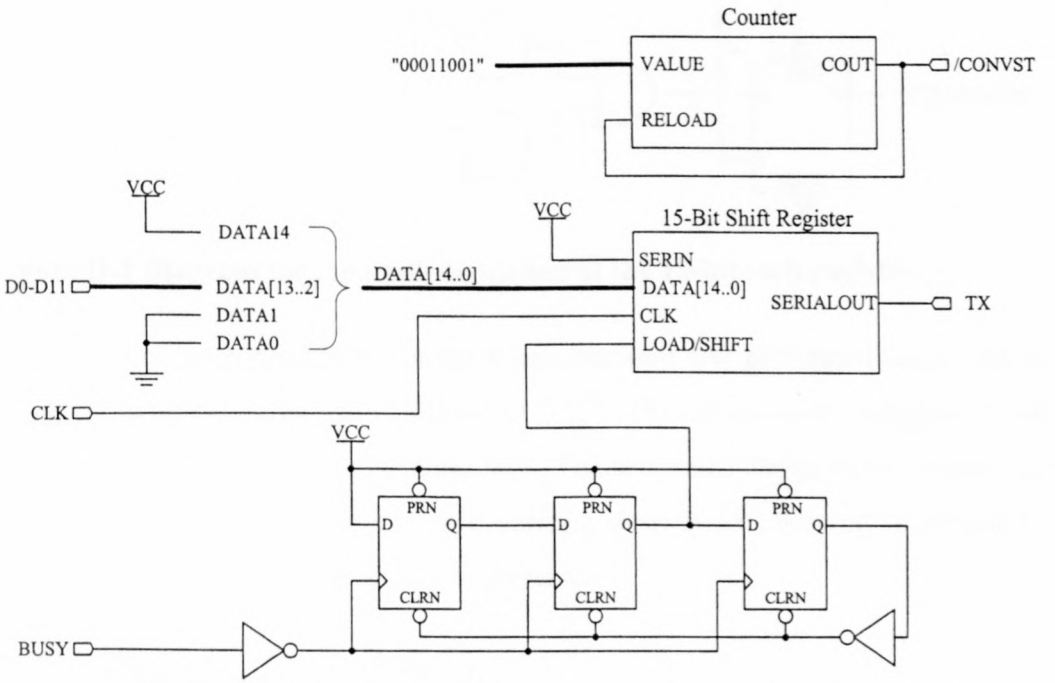

Figure D-1 Main design diagram of the control logic for the transmitter unit.

The implementation of the 15-bit shift register is shown in Figure D-2. The counter shown in Figure D-1 is a customisable component within the Max+PLUS II® environment.

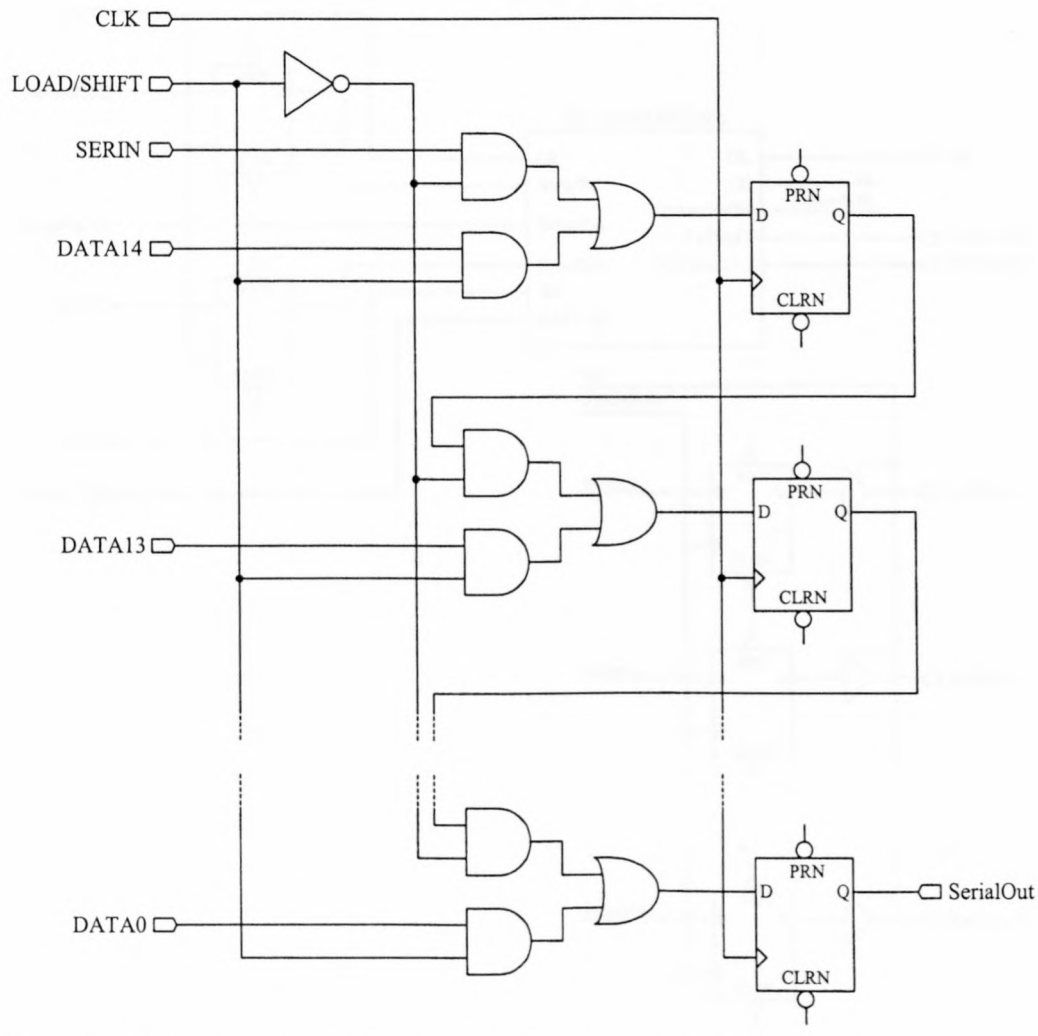

Figure D-2 Diagram for the implementation of the 15-bit shift register.

The design of the control logic for the transmitter unit was performed using only the graphical design environment of Max+PLUS II®. This is due to the simplicity of the design requirements for the transmitter unit. The text based design environment using VHDL is useful when creating more intricate designs as observed in section D.2 where the design of the receiver unit is presented.

D.2 Receiver Logic Design

This section presents the design of the control logic for the receiver unit. The design was created in both the graphical and VHDL environments. The main diagram of the receiver logic design is shown in Figure D-3.

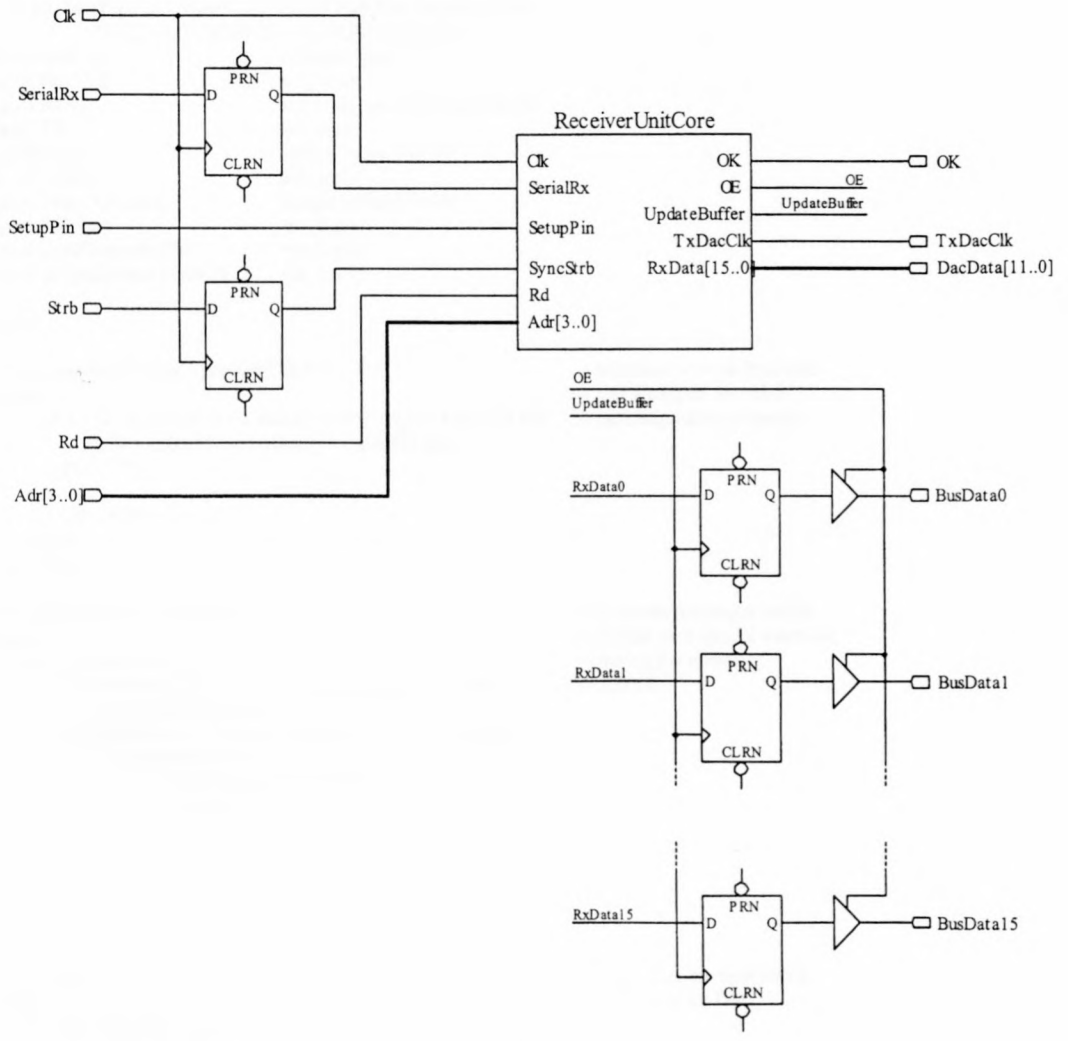

Figure D-3 Main design diagram of the receiver logic.

The Receiver Unit Core shown in Figure D-3 is implemented using VHDL instead of the graphical design environment, which is due to the increased complexity of the design. The VHDL code for the Receiver Unit Core is as follows:

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
entity RxProbeVer01_Core_Ch1 is
port (    Clk       :    in std_logic;                          -- Global Clock Input
     SerialRx       :    in std_logic;                          -- Synchronised Serial Data
     Rd        :    in std_logic;                              -- Data Bus Read Signal
     StrbSync       :    in std_logic;                          -- Synchronised Strb Signal
     UpdateBuffer   :    out std_logic;                         -- Update Buffer Signal
     Adr       :    in std_logic_vector(5 downto 0);           -- 4-bit Address bus
     SetupPin       :    in std_logic;                          -- Setup pin for startup
     Cslct          :    in std_logic_vector(3 downto 0);       -- Dipswitch Inputs
     OE        :    out std_logic;                             -- Data buffer Output Enable
     Ok        :    out std_logic;                             -- Serial data OK Signal
     TxDacClk       :    out std_logic;                         -- DAC Conversion signal
     RxData         :    out std_logic_vector(11 downto 0));    -- 12-bit Parallel data
end RxProbeVer01_Core_Ch1;

architecture RxProbeVer01_Core_Ch1_a of RxProbeVer01_Core_Ch1 is
```

```
Type RxStateType is  (StartBit1,StartBit2,Bit0,Bit1,Bit2,Bit3,Bit4,
            Bit5,Bit6,Bit7,Bit8,Bit9,Bit10,Bit11,StopBit);
signal RxState              :   RxStateType;
signal HoldOff              :   std_logic;
signal RxBuf                :   std_logic_vector(11 downto 0);
signal TB                   :   std_logic;
signal Count                :   integer range 0 to 39;
signal EndRx                :   std_logic;
signal TimeOutCount         :   integer range 0 to 49;
signal StrbSync             :   std_logic;
signal HoldOutputBuffer     :   std_logic;
signal OutputDataOnNextClk  :   std_logic;

begin

DataAcquisitionProcess : process(Clk,Rd)                    -- Monitors address lines and
begin                                                       -- and Rd signal for valid
    if (Rd = '0') and (Adr(3) = Cslct(3)) and (Adr(2) = Cslct(2)) and   -- data acquisition sequence
        (Adr(1) = Cslct(1)) and (Adr(0) = Cslct(0)) then
        OE <= '1';
    else
        OE <= '0';
    end if;
end process;

UpdateDataBuffer : process(Clk)                             -- Controls the output buffer
begin                                                       -- update with special attention
    if Clk'event and Clk = '1' then                         -- during the update of
        if (StrbSync = '0') and (HoldOutputBuffer = '1') then   -- RxBuf
            OutputDataOnNextClk <= '1';
        elsif (StrbSync = '0') and (HoldOutputBuffer = '0') then
            UpdateBuffer <= '1';
        elsif OutputDataOnNextClk = '1' then
            UpdateBuffer <= '1';
            OutputDataOnNextClk <= '0';
        else
            UpdateBuffer <= '0';
        end if;
end process;

TxDacClockProcess : process(Clk)                            -- Generates the conversion
begin                                                       -- signal for the DAC
    if Clk'event and Clk = '1' then
        if EndRx = '1' then
            TxDacClk <= '1';
        else
            TxDacClk <= '0';
        end if;
    end if;
end process;

HoldOffProcess : process(Clk)                               -- Implements the hold-off
begin                                                       -- feature during startup
    if Clk'event and Clk = '1' then                         -- or during break in
        if HoldOff = '1' then                               -- transmission
            if Count < 39 then
                Count <= Count + 1;
            else
                Count <= 0;
            end if;
        else
            Count <= 0;
        end if;
    end if;
end process;

DataReadProcess : process(Clk)                              -- Serial to parallel process
begin
    if Clk'event and Clk = '1' then
        if SetupPin = '1' then                              -- Internal registers initialised
            if HoldOff = '0' then                           -- Check for hold-off condition
                case RxState is
                    when StartBit1 =>                       -- Check state of serial data
                        if (TB = '0') and (SerialRx = '0') and (EndRx = '1') then -- First sample
                            TB <= '1';                      -- Proceed to second sample
```

```
            RxState <= StartBit1;
            TimeOutCount <= 0;
        elsif (TB = '1') and (SerialRx = '0') and (EndRx = '1') then -- Second Sample
            RxState <= StartBit2;                    -- Proceed to next bit
            TB <= '0';
            EndRx <= '1';
        else
            if TimeOutCount < 49 then                -- Check time-out of serial data
                TimeOutCount <= TimeOutCount + 1;
            else
                TimeOutCount <= 0;
                OK <= '0';
            end if;
            TB <= '0';
            EndRx <= '1';
            RxState <= StartBit1;
        end if;

    when StartBit2 =>
        if (TB = '0') and (SerialRx = '0') and (EndRx = '1') then
            TB <= '1';
            EndRx <= '1';
            RxState <= StartBit2;
        elsif (TB = '1') and (EndRx = '1') and (SerialRx = '0') then
            TB <= '0';
            EndRx <= '0';
            RxState <= Bit0;
        else
            TB <= '0';
            RxState <= StartBit1;
            EndRx <= '1';
        end if;

    when Bit0 =>
        if (TB = '0') and (EndRx = '0') then
            TB <= '1';
        elsif (TB = '1') and (EndRx = '0') then
            RxBuf(0) <= not SerialRx;
            TB <= '0';
            RxState <= Bit1;
        end if;

    when Bit1 =>
        if (TB = '0') and (EndRx = '0') then
            TB <= '1';
        elsif (TB = '1') and (EndRx = '0') then
            RxBuf(1) <= not SerialRx;                -- Transfer serial bit to RxBuf
            TB <= '0';
            RxState <= Bit2;                         -- Proceed to next bit
        end if;

    when Bit2 =>
        if (TB = '0') and (EndRx = '0') then
            TB <= '1';
        elsif (TB = '1') and (EndRx = '0') then
            RxBuf(2) <= not SerialRx;
            TB <= '0';
            RxState <= Bit3;
        end if;

    when Bit3 =>
        if (TB = '0') and (EndRx = '0') then
            TB <= '1';
        elsif (TB = '1') and (EndRx = '0') then
            RxBuf(3) <= not SerialRx;
            TB <= '0';
            RxState <= Bit4;
        end if;

    when Bit4 =>
        if (TB = '0') and (EndRx = '0') then
            TB <= '1';
        elsif (TB = '1') and (EndRx = '0') then
            RxBuf(4) <= not SerialRx;
            TB <= '0';
```

```
            RxState <= Bit5;
        end if;

    when Bit5 =>
        if (TB = '0') and (EndRx = '0') then
            TB <= '1';
        elsif (TB = '1') and (EndRx = '0') then
            RxBuf(5) <= not SerialRx;
            TB <= '0';
            RxState <= Bit6;
        end if;

    when Bit6 =>
        if (TB = '0') and (EndRx = '0') then
            TB <= '1';
        elsif (TB = '1') and (EndRx = '0') then
            RxBuf(6) <= not SerialRx;
            TB <= '0';
            RxState <= Bit7;
        end if;

    when Bit7 =>
        if (TB = '0') and (EndRx = '0') then
            TB <= '1';
        elsif (TB = '1') and (EndRx = '0') then
            RxBuf(7) <= not SerialRx;
            TB <= '0';
            RxState <= Bit8;
        end if;

    when Bit8 =>
        if (TB = '0') and (EndRx = '0') then
            TB <= '1';
        elsif (TB = '1') and (EndRx = '0') then
            RxBuf(8) <= not SerialRx;
            TB <= '0';
            RxState <= Bit9;
        end if;

    when Bit9 =>
        if (TB = '0') and (EndRx = '0') then
            TB <= '1';
        elsif (TB = '1') and (EndRx = '0') then
            RxBuf(9) <= not SerialRx;
            TB <= '0';
            RxState <= Bit10;
        end if;

    when Bit10 =>
        if (TB = '0') and (EndRx = '0') then
            TB <= '1';
        elsif (TB = '1') and (EndRx = '0') then
            RxBuf(10) <= not SerialRx;
            TB <= '0';
            RxState <= Bit11;
        end if;

    when Bit11 =>
        if (TB = '0') and (EndRx = '0') then
            TB <= '1';
        elsif (TB = '1') and (EndRx = '0') then
            RxBuf(11) <= not SerialRx;
            TB <= '0';
            RxState <= StopBit;
        end if;

    when StopBit =>
        if (TB = '0') and (EndRx = '0') then
            TB <= '1';
            HoldOutputBuffer <= '1';                    -- Disable update of the output buffer
        elsif (TB = '1') and (SerialRx = '1') and (EndRx = '0') then -- Check for valid stopbit
            RxData <= RxBuf;                            -- Update DAC data output
            TB <= '0';
            RxState <= StartBit1;
            EndRx <= '1';
```

```
                        Ok <= '1';
                        HoldOff <= '0';                    -- Disable holdoff
                        HoldOutputBuffer <= '0';           -- Enable update of output buffer
                    else
                        Ok <= '0';                         -- Indicate faulty transmission
                        HoldOff <= '1';                    -- Enable hold-off function
                        RxData <= "000000000000";          -- Zero to DAC output
                        RxState <= StartBit1;              -- Initialise to Startbit
                        TB <= '0';
                        EndRx <= '1';
                    end if;

                end case;
            else
                if Count = 39 then
                    HoldOff <= '0';
                end if;
            end if;
        else
            HoldOff <= '0';
            EndRx <= '1';
            RxState <= StartBit1;
            TB <= '0';
        end if;

    end if;
end process;

end RxProbeVer01_Core_Ch1_a;
```


siebrits_field_2003