Analysis and Synthesis of a 2 MVA Series-stacked Power-Quality Conditioner

Hendrik du Toit Mouton

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Supervisor: Prof. J.H.R. Enslin

Co-supervisor: Prof. H. Akagi

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Declaration

I, the undersigned, hereby declare that the work contained in this dissertation is my own original work, unless otherwise stated, and has not previously, in its entirety or in part, been submitted at any university for a degree.

H. du T. Mouton
December 4, 1999

Summary

This thesis describes the development of a power electronic converter for a 2 MVA series-injection power-quality device. The converter is designed to interface directly with superconducting magnetic energy storage devices and operates at a nominal DC-bus voltage of 2.4 kV.

In the first part of the thesis the viability of soft-switching for application to the 2 MVA converter is investigated. A new resonant turn-off snubber topology is introduced and a detailed theoretical study of the converter and snubber switching losses is carried out. An optimal snubber design procedure is derived. This is followed by a theoretical investigation of the effects of the different parasitic components on the snubber operation. In the final part of the investigation, a turn-on snubber is added to the turn-off snubber topology. An experimental evaluation of both the turn-off and combined turn-on and turn-off snubbers is carried out.

In order to obtain a DC-bus voltage of 2.4 kV, a series-stacked converter topology, for use in the 2 MVA series-injection device, is investigated. A detailed theoretical analysis of the DC-bus balancing mechanisms is conducted. This theoretical analysis makes use of fundamental results from the theory of systems of linear differential equations; in particular of Floquet theory.

In the final part of the thesis an experimental 700 kVA series-stacked phase-arm, operating at a 2.4 kV DC-bus voltage, is constructed. The operation of this converter is verified through a range of experiments and the measured results are compared with the theoretical predictions.

Opsomming

Hierdie proefskrif bespreek die ontwikkeling van 'n drywingselektroniese omsetter vir 'n 2 MVA serie-injeksie toevoerkwaliteittoestel. Die omsetter is ontwerp om direk aan 'n supergeleidende magnetiese energiestoor te koppel en werk by 'n nominale GS-busspanning van 2.4 kV.

In die eerste deel van die proefskrif word die moontlike toepassing van 'sagte skakeling' by hoë drywingsvlakke ondersoek. 'n Nuwe afskakelgapser word ondersoek en 'n deeglike teoretiese studie van die verliese in die gapser en omsetter word uitgevoer. Hierdie ondersoek gee aanleiding tot 'n optimale ontwerpprosedure. 'n Teoretiese analise van die effek van die verskillende parasitêre komponente op die werking van die gapser word gedoen. Laastens word getoon hoe 'n aanskakelgapser met die afskakelgapser geïntegreer kan word. Die werking van beide gapserbane word eksperimenteel bevestig.

Aangesien die serie-injeksie omsetter by 'n GS-busspanning van 2.4 kV moet werk, word 'n seriegeskakelde omsettertopologie ondersoek. 'n Breedvoerige teorie, wat die balansering van die GS-busspannings beskryf, word ontwikkel. Die teorie maak van basiese stellings uit die teorie van stelsels van linieêre differensiaalvergelykings gebruik; in die besonder van Floquet-teorie.

In die laaste deel van die proefskrif word die ontwerp van 'n eksperimentele 700 kVA seriegeskakelde fase-arm wat by 'n GS-busspanning van 2.4 kV werk, bespreek. Die werking van die omsetter word eksperimenteel geëvalueer en die gemete resultate word met die teorie vergelyk.

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Glossary

ARCP	Auxiliary Resonant Commutated Pole
c	Specific heat capacity
C_d	DC-bus capacitance
C_r	Snubber capacitance
δ	Skin depth
DSP	Digital Signal Processor
DVR	Dynamic Voltage Restorer
FPGA	Field Programmable Gate Array
f_r	Reference function
f_s	Half-bridge switching frequency (Hz)
ω_s	Half bridge angular switching frequency (rad/s)
GTO	Gate Turn-off Thyristor
IGBT	Insulated Gate Bipolar Transistor
i_o	Output current
L_r	Resonant inductance
Φ	Fundamental matrix
PWM	Pulse Width Modulation
R_b	Bus resistance
Re	Real part
s	Switching function
σ	Conductivity
STATCOM	Static Compensator
SVC	Static VAR Compensator
τ	Time constant
tr	trace of a matrix
T_s	Half-bridge switching period
UPS	Uninterruptible Power Supply
v_{ce}	Collector-emitter voltage
V_b	DC supply voltage
V_d	DC-bus voltage
v_o	Output voltage
v_s	Supply voltage
ω_r	Resonant frequency
W_{off}	IGBT turn-off losses
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Chapter 1

Power-quality problems and solutions

1.1 Power quality and reliability

Power-quality and reliability problems are abundant in power networks where the generation centers are concentrated in one area and power has to be delivered to areas far from this zone [28]. Power-quality problems also occur on strongly interconnected networks due to network switching. Dynamic or non-linear loads and interaction between the load and the network also give rise to a variety of power-quality problems.

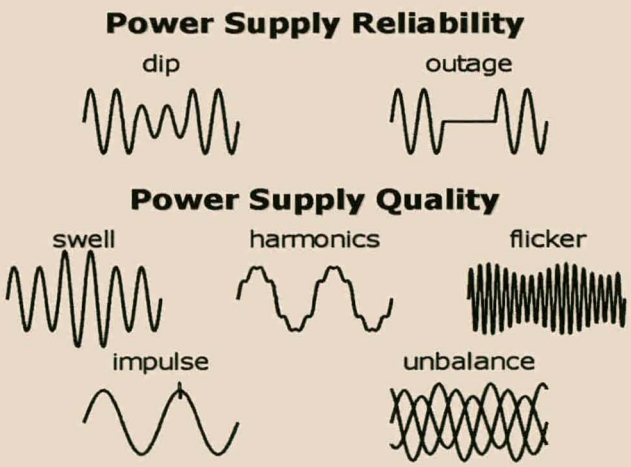


Figure 1.1: Different problems encountered with power quality and reliability.

Figure 1.1 shows some of the most common power-quality problems. The unwanted waveforms can be classified as those that lessen the reliability of the supply and those that degrade the quality.

The first group, power outages and brief voltage dips lasting from one cycle to a few seconds, is much more serious than the second group and can cause a large amount of damage [70], [6]. If

a dip exceeds even a few cycles, computer equipment, motors, servo-drives robots and machine tools cannot maintain control of the processes they power.

These reliability problems can be divided into two categories, namely those that originate on the facility itself (customer side) and those that originate on the utility side [33]. Customer side problems are mainly caused by plant startup or shutdown or electrical faults with the facility.

Utility side dips are caused by voltage depression as a result of abnormally large currents flowing through the power system impedance. These currents are mainly due to network faults and the starting of large motor or heating loads. Network faults are caused by lightning, cane fires, salt mist pollution, soil erosion and wash-away, fast-growing vegetation and sabotage [43], [101].

In South Africa and the USA voltage dips are by far the dominant and most costly power quality problem [101], [37], [39], [22].

Interruptions may last from a few seconds to days. Installing multiple feeders and more transformers reduces the occurrence of interruptions but increases the likelihood of dips due to the greater component count and the fact that more lines are exposed to lightning and fires.

The second group of power quality problems consists mainly of harmonic distortions, impulses and dynamic over-voltages that interfere with electronic circuits and may cause failure of equipment. Typical problems associated with harmonics are failure of commutation in thyristor rectifiers, overheating of equipment and trivial problems like fast running of digital clocks. Resonance at harmonic frequencies may result in the tripping of, or thermal damage to, shunt capacitor banks [101]. Loads that draw non-sinusoidal currents are the main cause of voltage harmonics. Typical sources of harmonics in power networks include variable speed drives, arc furnaces and rectifiers such as in aluminum smelters.

Voltage flicker is a fluctuation in the voltage supply that gives rise to perceptible fluctuations in light intensity. Fluctuating loads, like arc furnaces, are the main cause of flicker. The human eye is particularly sensitive to fluctuations of around 8 to 19 Hz. The effect of flicker on other types of equipment is not significant.

Asymmetry in the supply networks and the use of unbalanced (single-phase) loads are the main causes of voltage unbalance. Unbalanced supply voltages can cause overheating of motors, which is the single greatest load element in South Africa.

Power-quality-related problems have serious financial implications for industry. In South Africa it is estimated that the large industrial customers lose R1.2 billion per annum due to voltage dips [101]. In the USA industrial customers lose an estimated $50 billion due to dips and momentary outages. Both of these represent losses in excess of 10% of the value of electricity sales in the respective countries. It is roughly estimated that the potential market for dip and momentary outages mitigation is equal to one tenth of total worldwide electricity sales per

annum [101]. The other power-quality phenomena represent a potentially smaller market.

1.2 Power-quality solutions

A number of different approaches to a solution of these problems have been proposed. These solutions include both utility-side and customer-side approaches.

Shunt passive filters are widely used to suppress harmonics [1], [6], [9]. These filters provide a relatively inexpensive solution but can only compensate for a limited number of power-quality problems. They are also subject to a variety of other problems, including [17]:

- The source impedance strongly influences the filtering characteristics of the shunt passive filter. The fact that the source impedance is not accurately known and varies with the system configuration makes it difficult to design.
- The shunt passive filter acts as a sink to harmonic currents flowing from the source. In the worst case, the shunt passive filter may fall into series resonance with the supply impedance. This may result in overloading of the filter components.
- At a specific frequency parallel resonance occurs between the shunt passive filter and the supply impedance. This leads to so-called harmonic amplification.
- Shunt passive filters are subject to de-tuning as a result of aging of the filter components.

Due to the shortcomings of shunt passive filters and with the availability of new power electronic switches (like the IGBT) and high-speed digital signal processors, active power line conditioners have been developed in recent years. These devices are generally classified as shunt and series compensators. Although they are able to compensate for a wide variety of power quality problems, they also have a number of disadvantages. These include:

- Their initial and running costs are significantly higher than those of their passive counterparts [25]. The lifetime of some of the power electronic components, for instance the DC-bus capacitors, is limited. These have to be inspected and replaced on a regular basis.
- It has been wrongly believed that active filters are ideal harmonic compensators. As with passive filters the source and load impedances also influence their compensation characteristics [49].
- It is difficult and expensive to construct high-power converters with high bandwidth.

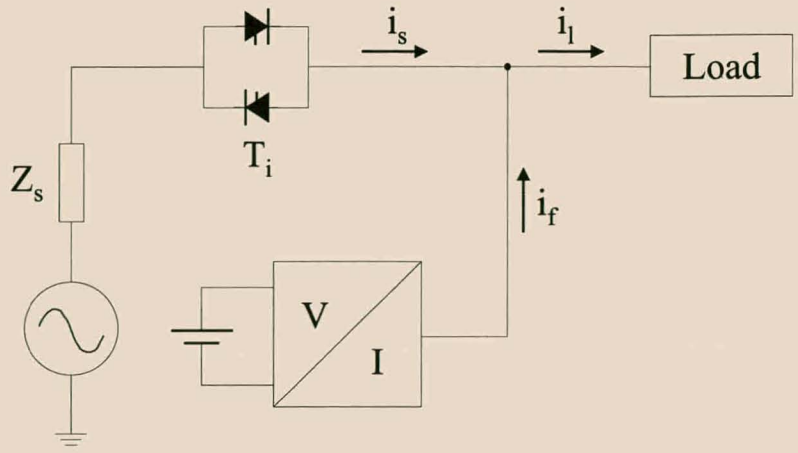


Figure 1.2: Shunt-injection power quality compensator.

Hybrid compensating devices, combing converters, thyristor controlled reactors (TCRs) and passive filters have been introduced to reduce the cost of active filters (see [97], [57], [98], [84], [62], [66], [80], [96] and [51]). One of the great advantages of this approach is a decrease in the required power rating of the high-performance converter. This results in decreased overall cost of the compensator.

1.2.1 Shunt compensation (STATCOM topology)

Figure 1.2 shows a shunt power quality compensator. It consists of a power electronic converter that is controlled to act as a current source, in shunt with the supply. Depending on the application, an optional energy storage element may be connected to the DC-bus.

When being used as an active filter, a compensating current i_f is injected to perform harmonic compensation for non-linear loads [27], [17], [83], thus canceling the load harmonics. The unwanted harmonic components flow only between the load and the compensator. This means that the supply current is sinusoidal. Its control is implemented through a detection and extraction circuit that provides a current reference consisting of the load harmonic current. One prerequisite for this device to function properly is that the load can be modeled as a current source (primarily inductive) [95], [49].

Apart from harmonic compensation this topology can also be used for power factor correction by injecting reactive power into the network. A small real power component is drawn to maintain the DC-bus at a constant value. This device can also compensate current unbalance between the three phases as well as for flicker.

The shunt device can be installed as a load current compensator (near the harmonic producing load) or as a harmonic damping device. Studies indicate that high levels of harmonics, during certain times of the day, can be caused by 'harmonic propagation' as a result of series/parallel

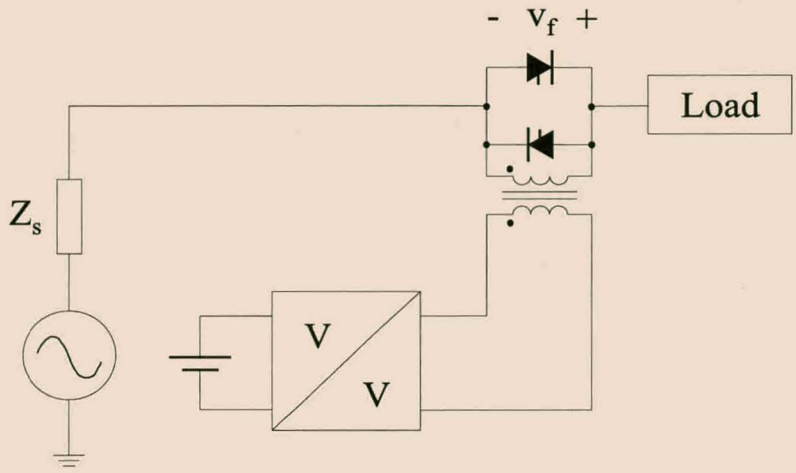


Figure 1.3: Series-injection power quality compensator.

resonance between the line inductance and shunt capacitors connected on the distribution network [62]. By providing a low impedance path through the shunt compensator, these harmonics can be damped.

By adding isolation thyristors T_i between the supply and the shunt-injection device, the device can be used as a UPS to provide power to the load during dips or outages. The thyristors are force commuted by the shunt compensator that takes over the full load current. By using this force-commutation technique the response time of the converter to voltage dips or outages is in the order of a few milliseconds. In this case an energy storage device, for instance batteries, flywheels or a superconducting energy storage device (SMES), supplies the energy [99].

One commercial device that operates on this principle is the DPQC-250 (Dynamic Power Quality Compensator) that has been developed at the University of Stellenbosch in association with ESKOM and APEC (AMS Power Electronic Converters). This multi-functional device makes use of battery energy storage for dip compensation and also provides active filtering and power factor correction.

1.2.2 Series compensation (DVR topology)

The series-injection topology is shown in Figure 1.3. It consists of a power electronic converter (controlled to act as a voltage source) in series, between the AC source and the load. A voltage v_f is injected in series with the supply voltage. Most of these devices make use of an injection transformer. Figure 1.3 also contains a thyristor bypass, which is used for protection purposes.

One of the applications of the series-injection device is as a harmonic isolator. In this application the device is controlled in such a way that it presents a high impedance to harmonic currents. In the process the source current is forced to be sinusoidal [95] [49]. In this mode of operation the device functions best if the load can be modeled as a voltage source, for instance, a diode

rectifier with smoothing capacitors [95]. A shunt passive filter may also be combined with the device to provide a low impedance path for harmonics.

The device may also be used as a dip compensator or to compensate for voltage unbalance by injecting a voltage component in series with the supply voltage. Recently some attempts have been made to eliminate the injection transformer in order to bring down the cost of the series-injection device [30], [100]. A transformerless dip compensator making use of a multilevel cascaded topology [49] is currently being developed at the University of Stellenbosch. A disadvantage of the transformerless series-injection topology is that energy cannot be exchanged between the DC-buses of the three converters (one per phase) and each phase requires its own individual energy storage device.

The main disadvantage of the series-injection topology is the fact that large fault currents will flow through the injection device under line fault conditions. Fault protection schemes for series active filters do exist [92], [108]. One way to protect the converter is to design the injection transformer in such a way that it saturates under fault currents. Another way is to provide a thyristor bypass with a high peak current rating. If the device is only operated as a dip compensator, the by-pass may be closed under normal operating conditions and opened when a dip is detected.

1.2.3 Unified series-shunt and shunt-series compensation

Figure 1.4 shows the series-shunt and shunt-series power quality devices which combine the benefits of both topologies [26], [62]. An optional energy storage device can be connected to the common DC-bus of the two converters.

Depending on the type of load (inductive or capacitive), either the series or the shunt device can be used to compensate for load harmonics. It is also possible to compensate for various other power quality problems, for instance, flicker, dips, poor power factor and current or voltage unbalance. The power ratings of the two units are not necessarily equal and depend on the required power quality solution.

In most applications the shunt device is responsible for regulating the DC-bus. The energy required for dip compensation can be provided through the energy storage element and the shunt unit. Table 1.1 summarizes the functions of the series, shunt and series-shunt devices.

The same converter topology is also applied to transmission system, where its purpose is quite different. In this context it is applied as a FACTS device and is referred to as a unified power flow controller (UPFC).

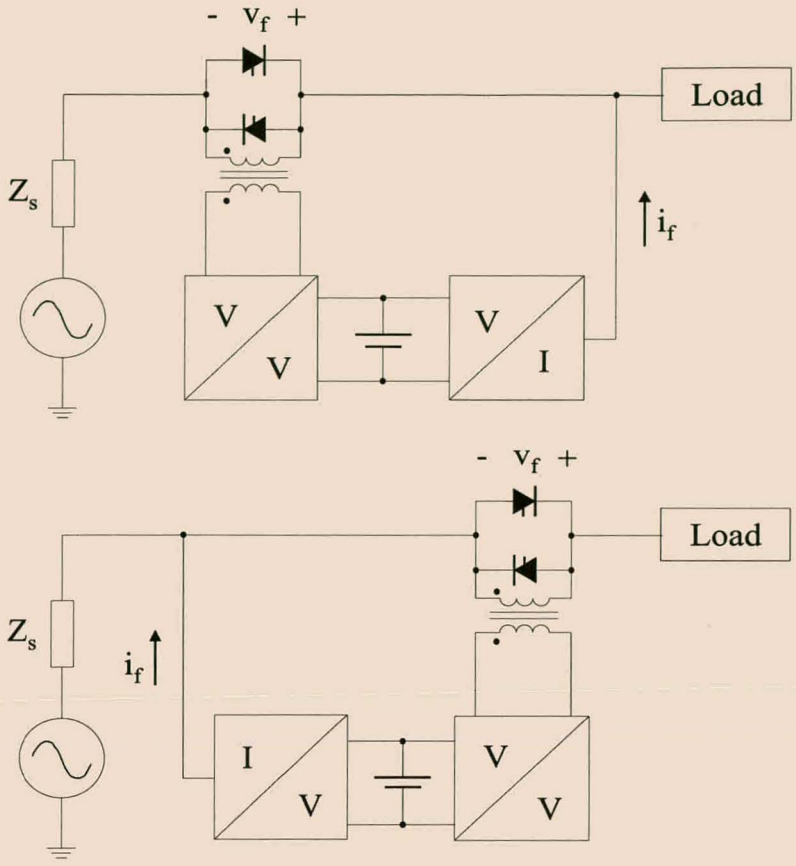


Figure 1.4: Series-shunt and shunt-series power quality compensators.

1.3 Project overview

The aim of this thesis is to study and develop the power electronic converter for a 2 MVA series-injection power quality device. This thesis formed part of a two-year research project for ESKOM on the development of a 2 MVA unified series-shunt power quality compensator. The main purpose of this device is to act as a dip compensator, although provision was made for multi-functionality in the design.

The overall ESKOM research project consisted of two main parts:

1. The development of a $\frac{1}{10}$th scale model (200 kVA) of a full three-phase series-shunt power quality compensator. This section of the project focused mainly on the closed-loop control of the power electronic converters of the series-shunt device [106].

2. The development of a single phase-arm (700 kVA) of a 2 MVA series-injection converter operating at a DC-bus voltage of 2.4 kV. This part of the project is reported in this thesis and it focused mainly on the converter technology.

Two of the main specifications laid down by ESKOM were:

Power Quality Problem	Series Device	Shunt Device	Series-shunt and Shunt-series
Harmonic isolation	Yes	No	Yes
Voltage dips	Yes	Yes (in UPS mode)	Yes
Power factor correction	No	Yes	Yes
Flicker	Yes	Yes	Yes
Current unbalance	No	Yes	Yes
Voltage unbalance	Yes	No	Yes
Voltage regulation	Yes	No	Yes
UPS operation	No	Yes	Yes

Table 1.1: Summary of the functions of the power quality compensator topologies.

1. The converter should be able to operate at a DC-bus voltage of between 2 and 2.5 kV. The main reason for this is that it must be able to interface with a superconducting magnetic energy storage device (SMES). This energy storage device provides a regulated DC-bus of 2.4 kV. Current dip compensators using superconducting magnetic energy storage devices are equipped with an extra GTO-based step-down converter to obtain an 800 V DC-bus. Eliminating this converter brings the overall system cost down and leads to an increase in efficiency.

2. The three phases of the converter should function independently. The three converters are connected to a common DC-bus, but the control of the three converters must be independent.

This thesis focuses on two of the aspects of high-power converter technology:

1. During the first part of the project soft-switching technology was developed and two new resonant snubber topologies were introduced. This research followed on the detailed investigation of the auxiliary resonant pole converter done in [105]. These new topologies were evaluated at a 70 kVA power level to determine their viability for use in the 700 kVA phase-arm.

2. The second part of the research focuses on high-voltage converter technology. By the time that the 700 kVA phase-arm was designed new high-voltage (2.5 kV, 3.3 kV and 4.5 kV) IGBTs were not yet commercially available. This meant that some form of series stacking of switching devices had to be used. A series-stacked converter topology was selected for this purpose. The second part of the research focused on the balancing and stability properties of this converter.

This thesis does not include a detailed investigation of the protection of this series device. More information on this important topic can be found in [108].

1.4 Soft-switching converters

The IGBT-based voltage source pulse-width modulated DC to AC converter has been the main choice in power electronic applications for the last number of years. This is due mainly to its simple drive circuit, low losses and effective protection circuitry. The switching frequency of very high power converters is, however, limited to a few kilohertz due to thermal limitations, as a result of switching losses, and EMI constraints.

Due to the fact that a relatively high bandwidth and a high quality of the output voltage waveform is required from the 2 MVA converter, a relatively high switching frequency has to be selected. Increasing the switching frequency also leads to smaller filter components, which results in a cost reduction as well as a reduction in the overall size of the converter. On the basis of these considerations it was decided to investigate the feasibility of soft switching for the 2 MVA phase-arm.

A wide variety of soft-switching topologies for DC to AC converters have been introduced over the years. These can broadly be classified as [18]:

1. *Load resonant DC-AC converters.* (See, for instance, [50], [38], [10], [52], [19], [24], [31], [21] and [32]) A resonant LC tank circuit is added to the load side of the converter. By utilizing the natural resonance of this circuit, zero voltage switch (ZVS) or zero current switch (ZCS) conditions can be produced for the switches of the converter bridge.

2. *Resonant transition DC-AC converters.* (See, for instance, [82], [29], [93], [75], [23], [85], [73], [36], [77] and [64]) In these topologies a resonant network is added to the main converter in order to create the ZVS or ZCS conditions. These may be passive networks, but in many topologies active switches are required to initiate the start of the resonant cycle.

3. *Resonant link DC-AC converters.* (See, for instance, [23], [35], [58], [78], [16], [65] and [69].) In this case the resonant network (active or passive) is connected between the input DC source and the converter bridge. The input bus oscillates in order to create the soft-switching conditions.

All of these topologies offer some advantages in terms of reduced switching losses and decreased $\frac{di}{dt}$ and $\frac{dv}{dt}$. Disadvantages of these topologies include complicated circuitry, limitations on the

control algorithms and increased current or voltage stresses on the main converter switches or auxiliary switches with high peak voltage or current ratings.

In [105] the auxiliary resonant pole converter (ARCP) was identified as being well suited to high power levels. This is mainly based on the fact that the resonant inductors carry large currents for only very small periods of time. A detailed investigation of this topology was carried out and an integrated module was developed. One of the problems identified with the ARCP is the high peak current rating of the auxiliary switches. This is typically between 120% and 180% of the maximum load current. Thyristors were used as auxiliary switches in [105]. However, due to their excessive turn-on losses when used above their rated current, the advantages of the ARCP were limited. IGBT devices may also be considered as auxiliary switches, but commercial IGBTs are designed to enter their linear region of operation (for protection purposes) if used significantly above their rated current.

In Chapter 2 a new resonant turn-off snubber that makes use of an auxiliary discharging circuit is introduced. The main advantage of this new topology is that the peak current rating of the auxiliary switches is small compared to that of the main switches. Later in Chapter 2 a turn-on snubber is integrated with the turn-off snubber in order to obtain the full benefit of reducing both the turn-on and turn-off losses.

1.5 Series-stacked converter topology

As mentioned above, at the time that the project was initiated a DC-bus voltage of 2.4 kV could not be obtained with single switching devices and some form of series stacking had to be applied.

Figure 1.5 shows a three-level series-stacked converter topology that was selected for this application. In [61] this topology was introduced for use in high-voltage DC and SVC applications. It is, however, believed that this topology has been published before, although the references could not be located.

The three-level series-stacked converter consists of three standard full-bridge converter modules with their DC-buses stacked in series. The outputs of the three converters are filtered and connected to three identical primaries of the injection transformer. Since the injection transformer is a non-standard transformer (based on ESKOM's range of transformers), the fact that it requires three individual primaries is not a serious disadvantage. Depending on the application the filter capacitors may be combined and placed on the secondary side of the transformer. In this case the leakage inductance of the transformer can be used as part of the filter inductor. When using the latter configuration, large ripple currents will flow through the windings of the transformer, leading to increased losses.

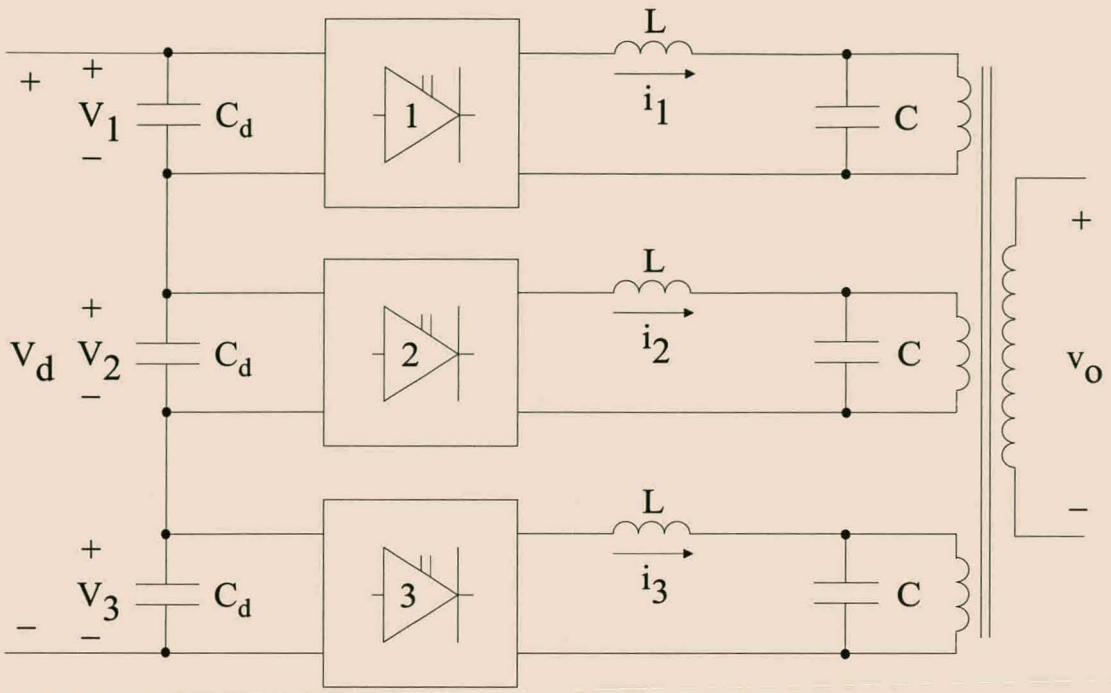


Figure 1.5: Three-level series-stacked converter.

Initially multilevel converters were investigated for the current application. As with the series-stacked converter topology these converters offer a high DC-bus voltage and reduced harmonic content of the output voltage waveform. Two of the best-known multilevel converter topologies are the diode clamped converter [46] and the flying capacitor multilevel converter [86]. In the current application the series-stacked converter topology offers some advantages over these two topologies. These include:

- It does not require extra components like clamping diodes and flying capacitors. It exploits the presence of the injection transformer, which is an integral part of the series-injection device.
- In a three-phase system the individual DC-bus capacitors banks of the respective full-bridge converters can be connected in parallel. Although this is possible with the diode-clamped topology, it cannot be achieved with the flying capacitor topology.
- It has excellent balancing properties. This will be proven formally in Chapter 3.
- The series-stacked converter topology can easily be reconfigured to operate at a lower (one-third) DC-bus voltage. This is achieved by connecting the DC-buses of all the full-bridge converters in parallel. In this case other energy storage devices, for instance batteries and flywheels, can be used. This option will, however, not be pursued in this thesis.

- It makes use of standard full-bridge converter building blocks that can be purchased from a number of manufacturers.

The stability analysis of the two- and three-level series-stacked converter topologies is the subject of Chapter 3. In Chapter 4 the construction of the laboratory prototype of the 700 kVA series-stacked phase-arm is discussed. This is followed by an experimental evaluation of its operation. Although the IGBT technology has since improved to the point where a 2.4 kV DC-bus voltage can be obtained using single devices, the basic principles laid down in this thesis can be applied to obtain higher rated converters with higher DC-bus voltages and increased total power rating.

1.6 Summary of the research contributions

The main focus of this thesis is on high-power converter technology for series-injection power quality compensators. A research contribution is made in two areas:

1. In Chapter 2 new snubber topologies suited to high-power voltage source converters are introduced. As a first step a new resonant turn-off snubber is developed. A study of the different converter and snubber losses is made. This gives rise to an optimal snubber design procedure that takes the effect of a number of parasitic components into account. This is followed by a detailed study of the effect of the different parasitic components on the snubber operation. An experimental version of the snubber is constructed and practical measurements of the switching behavior and efficiency are carried out. The aim is to evaluate the feasibility of this topology for use in the 700 kVA phase-arm. The measured results are compared with the theoretical results. In the final part of the chapter a turn-on snubber is added to the turn-off snubber topology. Its basic operating principles are described and an experimental prototype is constructed.

2. In Chapter 3 the DC-bus balancing properties of the series-stacked converter topology is studied. An extensive theory, describing the balancing mechanisms of the converter is developed for two- and three-level series-stacked converters. The operation and stability of these converters under two different modulation schemes are considered.

   As a first step the system of differential equations describing the operation of the converter is derived. So-called d and t parameters are introduced and the original circuit is transformed to an equivalent circuit that facilitates an understanding of the balancing mechanisms. Fundamental results from the theory of differential equations are applied. By using Liapunov's theorem the stability of the system is proved. This is followed by a

study of the dynamics of the balancing process by making use of Floquet theory. In the process effective ways of simulating the operation of the converter are derived.

In Chapter 4 the experimental 700 kVA phase-arm is constructed. This is followed by an experimental evaluation of the converter. The experimental evaluation confirms the balancing theory of Chapter 3 and proves that the converter operates effectively at its rated DC-bus voltage.

Chapter 2

A new resonant snubber

2.1 Introduction

This chapter introduces a new resonant snubber topology that is based on the auxiliary resonant pole converter. The main feature of this active snubber is that the peak current rating of the auxiliary switches is small compared to that of existing soft-switching circuits like the ARCP.

As a first step the effect of turn-off transients on IGBT converters is targeted by introducing a new turn-off snubber. Later a turn-on snubber is added to this topology to reduce the effects of both the turn-on and turn-off transients in high-power converters. This new topology forms part of the class of active resonant transition DC-AC converters (see p. 9).

Experimental versions of both the turn-off snubber and the combined turn-on/turn-off snubbers are constructed with the aim of evaluating the feasibility of these topologies at a 2 MVA power level.

2.2 A resonant turn-off snubber

In power bipolar transistor switching circuits, shunt capacitor turn-off snubbers were originally used to reduce the turn-off loss and prevent reverse-biased second breakdown (see [41]). Modern IGBT devices do not suffer from the problems associated with second breakdown. However, some modern devices, for instance, GTOs and new high-voltage IGBTs, do require turn-off snubbers to function properly. At high power levels adding snubber circuits becomes an attractive option to reduce switching loss and EMI; thereby extending the device ratings.

Some discrepancies appear in the literature concerning the ratio of turn-on to turn-off loss of modern high-power IGBT devices. Experimental results obtained in [71] and [72] showed that the turn-off loss in IGBT converters is significantly (3 times) greater than the turn-on loss.

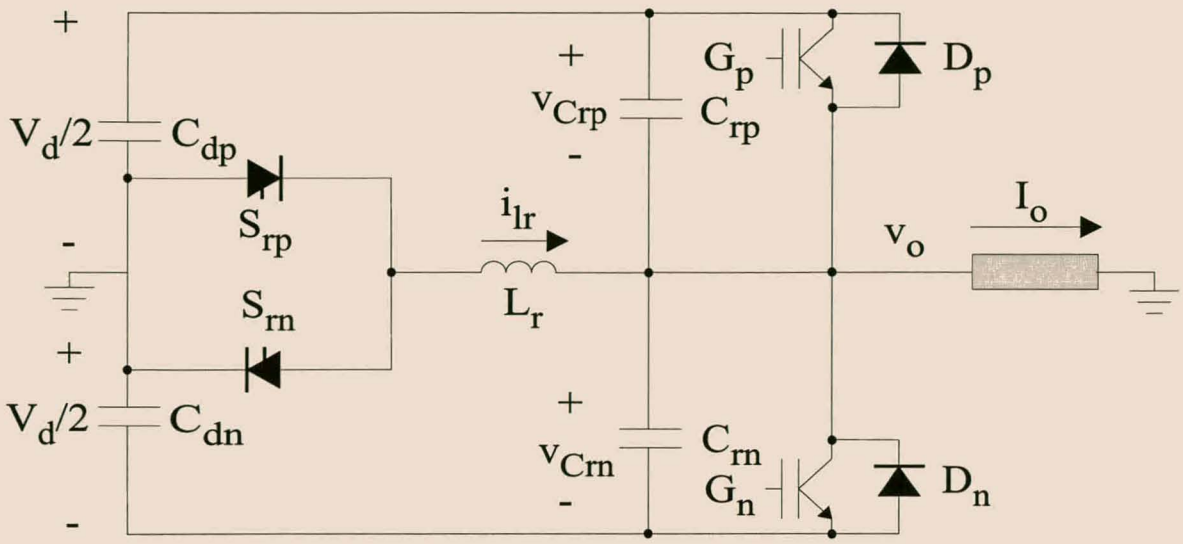


Figure 2.1: The auxiliary resonant commutated pole converter.

On the other hand [60] advocates the use of turn-on snubbers only. An oral communication with Prof J. Baliga, the inventor of the IGBT, revealed that it is possible to shape the ratio of turn-on to turn-off loss in the design process of the device. Device data sheets, for instance [102], show that the turn-off loss of integrated power modules is significantly greater than the turn-on loss at high currents and high temperatures. The turn-on loss is, however, influenced by the amount of parasitic inductance in the converter bus-bar structure and decreases with increasing parasitic inductance.

The aim of this section is to introduce a new resonant turn-off snubber (see [88]). As a first step a short overview of the ARCP is presented. The turn-off snubber circuit is introduced and its operating principles are discussed. This is followed by an investigation of the different loss components and an optimal snubber design procedure. A detailed investigation of the influence of the different parasitic components on the snubber operation is carried out. Finally, an experimental version of the snubber is constructed to evaluate its influence on the turn-off behavior of an integrated power module.

In the final part of the chapter a turn-on snubber will be combined with the new turn-off snubber, to achieve the full benefits of reducing the switching loss and EMI of both switching transients.

2.2.1 The auxiliary resonant commutated pole converter (ARCP)

This section provides a short overview of the operation of the ARCP converter. The aim is to show the evolution of the resonant turn-off snubber from the ARCP converter.

Figure 2.1 shows the ARCP converter topology (see, for instance, [74], [42] and [105]), while

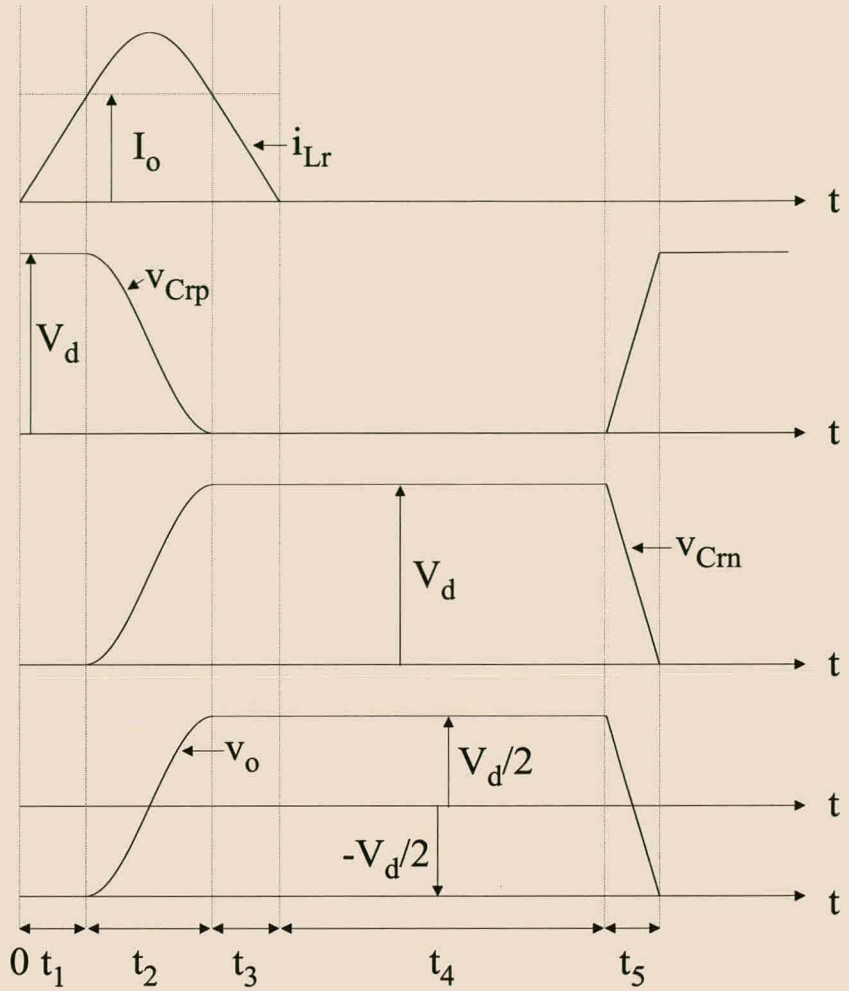


Figure 2.2: ARCP voltage and current waveforms.

Figure 2.2 shows the voltage and currents waveforms used in the following discussion. The main phase-arm is formed by IGBTs G_p and G_n and free-wheeling diodes D_p and D_n. Capacitors C_{dp} and C_{dn} form the DC-link capacitor bank, with the center point taken as the ground reference. The inductive load is modeled as a current source I_o. The auxiliary commutation circuit is formed by capacitors C_{rp} and C_{rn}, inductor L_r and auxiliary switches (thyristors) S_{rp} and S_{rn}. Capacitors C_{rp} and C_{rn} are equal in value and are denoted by C_r.

Consider the case where the load current I_o is positive. Prior to time 0 free-wheeling diode D_n is conducting the load current. At time 0 auxiliary switch S_{rp} is triggered. For $0 \leq t < t_1$ switch S_{rp} and inductor L_r start taking over the load current from D_n. During this period current i_{L_r} is given by

$$i_{L_r} = \frac{V_d}{2L_r}t. \tag{2.1}$$

At time $t_1 = \frac{2I_oL_r}{V_d}$ diode D_n turns off and inductor L_r starts to resonate with capacitors C_{rp} and C_{rn}. In the process C_{rp} is discharged, while C_{rn} is charged to voltage V_d. During this

period current i_{L_r} is given by

$$i_{L_r} = I_o + \frac{V_d}{2}\sqrt{\frac{2C_r}{L_r}}\sin(\omega_0(t - t_1)), \tag{2.2}$$

where $\omega_0 = \frac{1}{\sqrt{2L_rC_r}}$. Furthermore, voltages $v_{C_{rp}}$ and $v_{C_{rn}}$ are given by

$$v_{C_{rp}} = \frac{V_d}{2}(1 + \cos(\omega_0(t - t_1))) \tag{2.3}$$

and

$$v_{C_{rn}} = \frac{V_d}{2}(1 - \cos(\omega_0(t - t_1))). \tag{2.4}$$

At time $t_1 + t_2$ (with $t_2 = \frac{\pi}{\omega_0}$) voltage $v_{C_{rp}}$ reaches zero and main switch G_p is turned on. The voltages over C_{rp} and C_{rn} are now clamped by the combination of G_p and D_p. Note that G_p turns on at zero voltage and zero current. Furthermore, at time $t_1 + t_2$ current i_{L_r} is equal to the load current I_o and starts to decrease linearly at a rate of

$$\frac{di_{L_r}}{dt} = -\frac{V_d}{2L_r}. \tag{2.5}$$

At time $t_1 + t_2 + t_3$ (with $t_3 = \frac{2L_rI_o}{V_d}$) current i_{L_r} reaches zero and thyristor S_{rp} turns off. For the remainder of the period that G_p is on, current i_{L_r} is equal to zero, while the voltages over the snubber capacitors remain in their present states.

At time $t_1 + t_2 + t_3 + t_4$ main switch G_p is turned off. Capacitors C_{rp} and C_{rn} now take over the load current I_o from G_p, which turns off at zero voltage. The converter output voltage v_o decreases linearly with the gradient of the turn-off voltage slope given by

$$\frac{dv_o}{dt} = \frac{I_o}{2C_r}. \tag{2.6}$$

The total turn-off time t_5 is given by

$$t_5 = \frac{2V_dCr}{I_o}. \tag{2.7}$$

At the end of the turn-off cycle the output voltage v_o reaches $-\frac{V_d}{2}$. The process now starts over again.

When the load current I_o is relatively small capacitors C_{rp} and C_{rn} do not fully charge and discharge, respectively, before G_n is turned on. This results in excessive currents flowing through C_{rp}, C_{rn} and G_n. In this case auxiliary switch S_{rn} may be triggered to provide turn-off assistance. More details on this mode of operation can be found in [105].

Some observations concerning the operating principles of the ARCP can be made. These observations gives rise to the turn-off snubber topology of the following section.

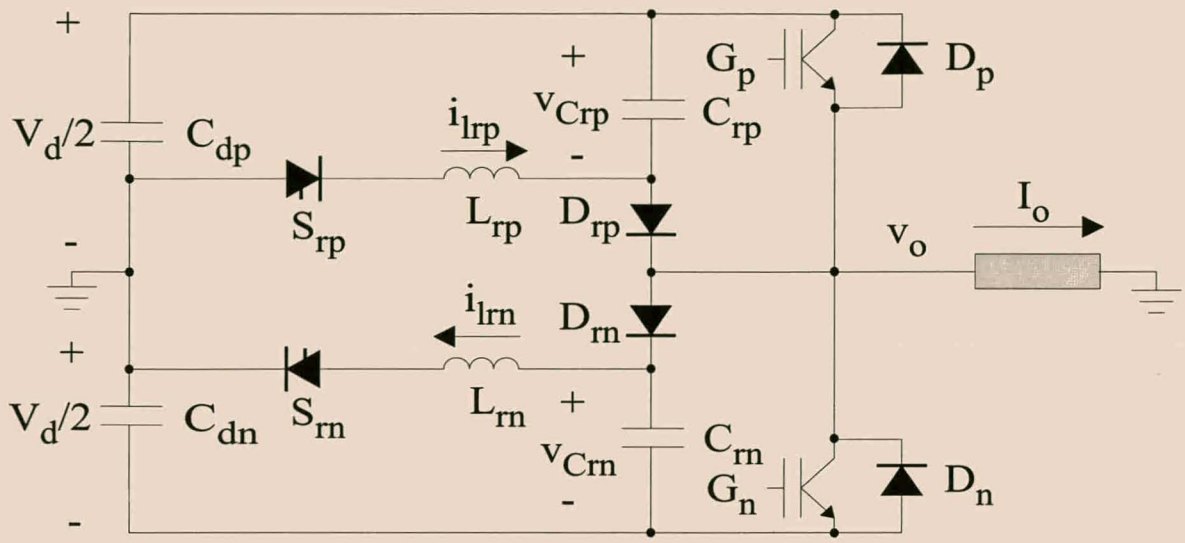


Figure 2.3: New resonant turn-off snubber topology.

1. The peak current rating of the auxiliary switches is given by

$$I_{L_{r(max)}} = I_o + \frac{V_d}{2}\sqrt{\frac{2C_r}{L_r}}. \tag{2.8}$$

   In practical converters this is substantially larger than the peak current rating of the main switches.

2. If it is possible to 'uncouple' the load from the snubber capacitors the I_o term in equation 2.8 disappears, which significantly reduces the peak current rating of the auxiliary switches.

3. A relatively high resonant frequency ω_0 has to be chosen. The time period $t_1 + t_2$ has to be shorter than the converter blanking time. This is another factor that leads to the high peak current rating of the auxiliary switches. Increasing the time available for the resonant cycle would lead to a decrease in the peak current rating of the auxiliary switches.

2.2.2 Basic turn-off snubber operation

Figure 2.3 shows the new resonant turn-off snubber topology. IGBTs G_p and G_n along with free-wheeling diodes D_p and D_n are a standard IGBT phase-arm. As in the previous section the inductive load is considered as a current source I_o. It is assumed that the load current is constant during the turn-off cycle of the phase-arm.

The resonant snubber consists of capacitors C_{rp} and C_{rn}, diodes D_{rp} and D_{rn}, inductors L_{rp} and L_{rn} and auxiliary switches S_{rp} and S_{rn}. Components C_{rp}, D_{rp}, L_{rp} and S_{rp} form the turn-off snubber for G_p, and S_{rp} is only triggered during periods of positive load current. Similarly, C_{rn},

D_{rn}, L_{rn} and S_{rn} form the turn-off snubber for G_n and S_{rn} is only triggered during periods of negative load current. In their most basic form thyristors can be used as auxiliary switches, but IGBTs, MOSFETs, GTOs and MTOs are also suitable. The auxiliary switches do, however, require a reverse blocking capability equal to $\frac{V_d}{2}$, which can be achieved by connecting a diode in series with the device. Capacitors C_{rp} and C_{rn} are equal in value and will be denoted by C_r, as are inductors L_{rp} and L_{rn}, which will be denoted by L_r. Essentially the snubber is a standard turn-off snubber (see, for instance, [10], p. 682) with a regenerative ARCP-based capacitor discharging circuit. The main advantage of this topology is that the peak current rating of the auxiliary switches is small compared to that of the standard ARCP converter and other resonant topologies, as will be shown shortly. The voltage rating of the auxiliary switches is half that of the main switches.

To explain the operation of the snubber the following assumptions are made in this section:

1. All the switching elements are ideal. This means that they have no conduction or switching losses and switch from one state to the other instantaneously. Furthermore, it is assumed that all the switches can block infinite voltages in the off state.

2. The passive components are ideal. They are assumed to be totally linear and have no losses.

3. The load current I_o is constant during the turn-off cycle of the main IGBT phase-arm.

4. The top and bottom DC-bus voltages do not drift and are fixed at $\frac{Vd}{2}$ and $-\frac{Vd}{2}$, respectively.

5. There are no parasitic inductances, capacitances or resistances in the circuit.

Refer to Figure 2.4 for an explanation of the snubber operation. Consider the case where the load current I_o is positive. Prior to time 0 diode D_n is conducting the load current. Capacitors C_{rp} and C_{rn} are fully charged with $v_{C_{rp}} = v_{C_{rn}} = V_d$. As the main switch G_p turns on, at time 0, the output voltage v_o swings from $-V_d/2$ to $V_d/2$ almost instantaneously. At the same instant thyristor S_{rp} is triggered and inductor L_{rp} starts to resonate with capacitor C_{rp}, discharging C_{rp} in the process. During the resonant cycle current $i_{L_{rp}}$, through the resonant inductor, is given by

$$i_{L_{rp}} = \frac{V_d}{2}\sqrt{\frac{C_r}{L_r}}\sin(\omega_0 t), \tag{2.9}$$

where $\omega_0 = \frac{1}{\sqrt{L_r C_r}}$. Voltage $v_{C_{rp}}$ over capacitor C_{rp} is given by

$$v_{C_{rp}} = \frac{V_d}{2}(1 + \cos(\omega_0 t)). \tag{2.10}$$

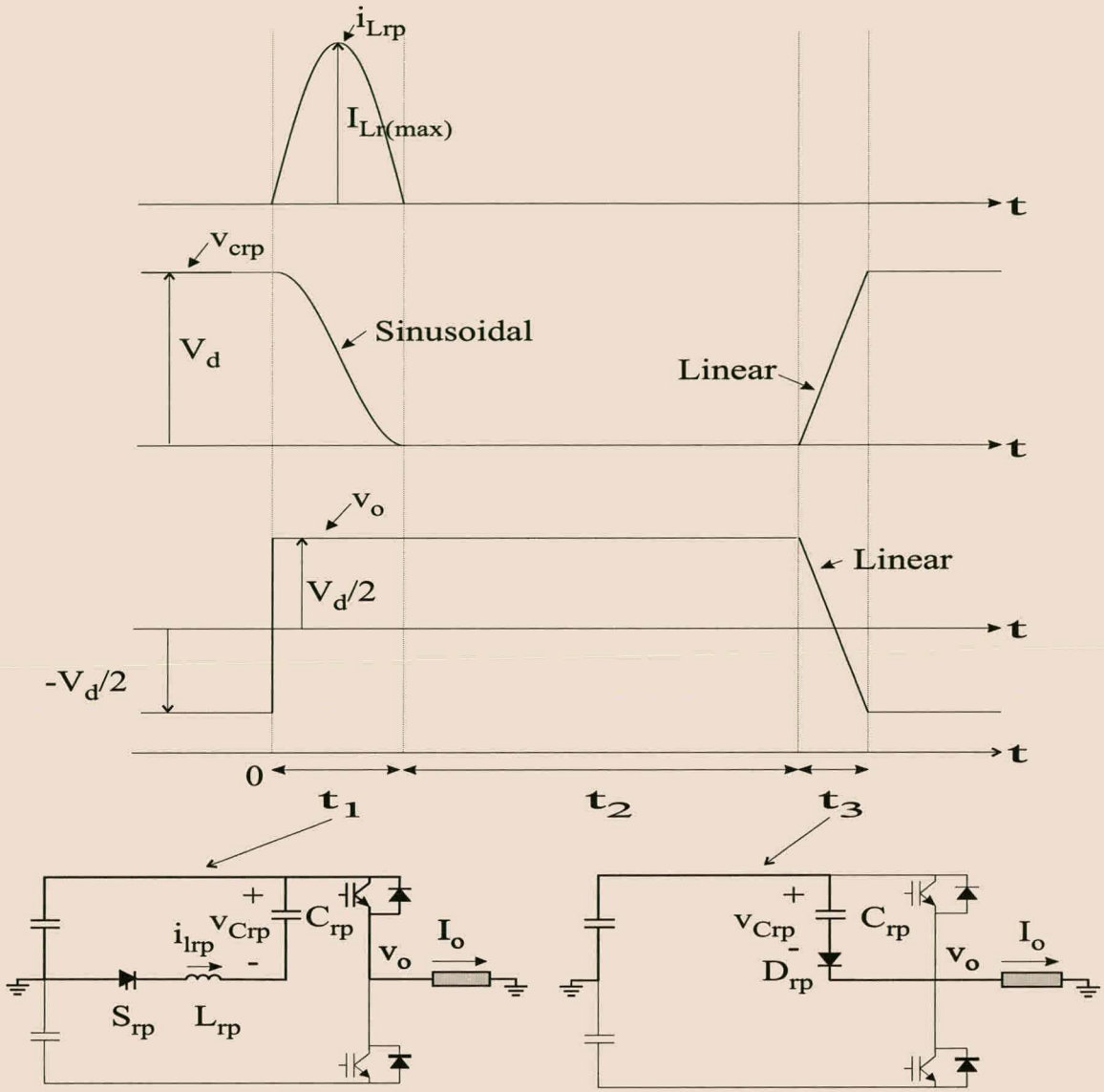


Figure 2.4: Turn-off snubber voltage and current waveforms.

At time $t_1 = \frac{\pi}{\omega_0}$ (after half a resonant cycle) $i_{L_{rp}}$ reaches zero and S_{rp} turns off as the voltage over C_{rp} reaches zero. Time t_1 will be referred to as the *capacitor discharge time*. The peak current through L_{rp} is given by

$$I_{L_{r(max)}} = \frac{V_d}{2}\sqrt{\frac{C_r}{L_r}}. \tag{2.11}$$

During the period $t_1 \leq t \leq t_1 + t_2$, G_p is conducting the load current and capacitor C_{rp} remains discharged.

At time $t_1 + t_2$ switch G_p is turned off and D_{rp} becomes forward biased. Diode D_{rp} and capacitor C_{rp} takes over the load current from G_p, which turns off at zero voltage. The converter output voltage v_o decreases linearly, with the gradient of the turn-off voltage slope given by

$$\frac{dv_o}{dt} = \frac{I_o}{C_r}. \tag{2.12}$$

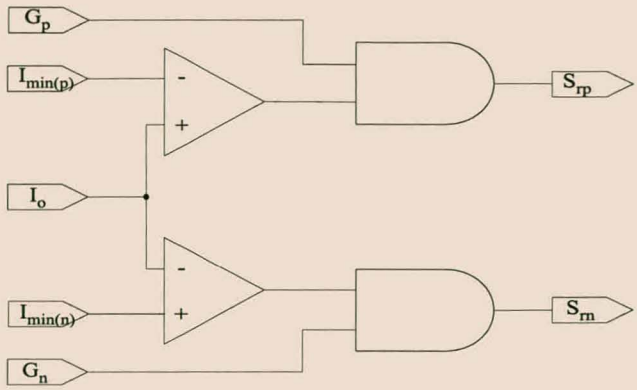


Figure 2.5: Turn-off snubber control circuit.

The total turn-off time t_3 is given by

$$t_3 = \frac{V_d C r}{I_o}. \tag{2.13}$$

At time $t_1 + t_2 + t_3$ the output voltage reaches $-\frac{V_d}{2}$ and the voltage over C_{rp} is equal to V_d. The cycle now starts over again.

It is important to note that the auxiliary switches turn on and off at zero current. Hence the auxiliary circuit is itself a soft-switching circuit. The operation of the snubber during periods of negative load current is totally symmetrical to that during periods of positive load current. When the load current is negative, auxiliary switch S_{rn} is triggered to initiate discharge of capacitor C_{rn}.

2.2.3 Implementation considerations

In this section some of the practical considerations of implementing the resonant turn-off snubber are discussed.

As the load current I_o decreases, the total turn-off time t_3 increases. If the total turn-off time exceeds the blanking time, t_b of the main module, switch G_n will turn-on before capacitor C_{rp} is fully charged. This will result in excessive current flowing through G_n, D_{rp} and C_{rp}, which may lead to the destruction of one or more of these devices. One solution to this problem is to measure the output current I_o and to cease operation of the snubber when

$$|I_o| < \frac{C_r V_d}{t_b}. \tag{2.14}$$

Figure 2.5 shows the snubber control circuit designed to accomplish this. The output current is measured and compared to reference currents $I_{min(p)}$ and $I_{min(n)}$ for the top and bottom IGBTs, respectively. If the measured output current is greater than the reference current $I_{min(p)}$, the gating signal of G_p is also applied to switch S_{rp}. On the other hand, if the output current is less than the reference current $I_{min(n)}$, the gating signal of G_n is also applied to S_{rn}.

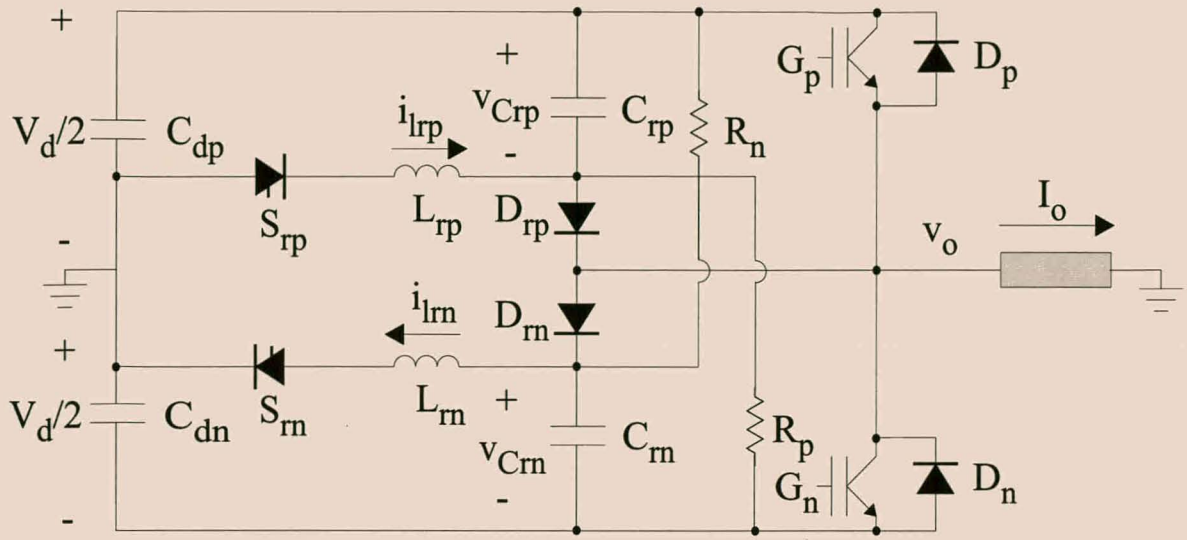


Figure 2.6: Turn-off snubber with charging resistors.

It is important to carefully consider the operation of the snubber when the output current changes sign. Consider the case where the output current I_o is positive at the beginning of the switching cycle, and changes sign during the particular cycle. At the end of the switching cycle diode D_p conducts the load current, which G_n takes over when turning on. If capacitor C_{rp} was discharged, based on the positive load current at the beginning of the switching cycle, large currents will flow through C_{rp}, D_{rp} and G_n. For this reason the magnitudes of $I_{min(p)}$ and $I_{min(n)}$ should be chosen greater than the maximum possible change (ripple) in the magnitude of the output current during one switching cycle.

Another important practical consideration is the fact that the snubber capacitors have to be charged before the converter is turned on to avoid excessive current when the main IGBTs turn on for the first time. For instance, if C_{rn} is not charged to V_d and G_p turns on, a large current will flow through G_p, D_{rn} and C_{rn}. Charging of the snubber capacitors can be achieved by slowly increasing the DC-bus voltage while the converter is switching. Another alternative is to connect resistors between the snubber capacitors and the DC-bus in order to charge the snubber capacitors before switching the main IGBT module as shown in Figure 2.6. Resistor R_p charges capacitor C_{rp} while R_n charges C_{rn} before the converter starts switching.

Some attention should also be given to the effect of the snubber on the DC-bus center point voltage. Again consider the case where the load current I_o is positive. The load current returns through the DC-bus center point. This will cause the voltage across the top DC-bus capacitor to decrease, while the voltage over the bottom capacitor increases. During periods of positive load current S_{rp} is triggered which results in current flowing out of the DC-bus center point. This will to a limited extent cancel the unwanted drifting effect caused by the load current returning through the center point. This shows that the snubber assist in a limited way with the balancing of the DC-bus center point. In full-bridge or three-phase converters the load

current does not necessarily return through the center point and careful consideration should be given to the effect of the snubber when designing the DC-bus capacitors.

When designing the snubber a compromise must be made between the main IGBT turn-off loss, peak current rating of the auxiliary switches and total discharge time of the snubber capacitor:

1. Increasing the size of the snubber capacitor C_r results in decreased turn-off loss in the main IGBT. This is at the expense of increased blanking time (especially at low output currents), greater peak current rating of the auxiliary switches and increased capacitor discharge times. It is important to note that the maximum (and minimum) duty cycle is limited by the capacitor discharge time.

2. Increasing the size of the resonant inductor L_r will result in lower peak ratings for the auxiliary switches at the expense of increased capacitor discharge time. It will also result in increased conduction loss in the resonant inductor.

Throughout this chapter examples will be used to illuminate the theoretical analysis of the snubber.

Example 2.1

The PM200DSA120 integrated IGBT module from Powerex (see [102], p. O-43) will be used as an example of the main IGBT module. This module was used in [105] as a basis for the evaluation of an ARCP converter. Table 2.1 summarizes the properties of this module. Based on this IGBT module, a turn-off snubber for a power electronic converter, meeting the

Parameter	Symbol	Value
Collector-Emitter Voltage	V_{CES}	1200 V
Collector Current	I_C	200 A
Peak Collector Current	I_{CP}	400 A
Supply Voltage	V_{CC}	900 V
Supply Voltage, Surge	$C_{CC(surge)}$	1000 V
Collector Dissipation	P_C	1140 W
Collector Turn-off Time	$t_{C(off)}$	600 ns

Table 2.1: Parameters of the Powerex PM200DSA120 IGBT module.

specifications of Table 2.2, must be designed. The base value C_{r_1} of the snubber capacitance is defined as

$$C_{r_1} = \frac{I_{o(max)} t_{C_{(off)}}}{V_d} = 150 \text{ nF}. \tag{2.15}$$

Parameter	Symbol	Value
Nominal DC-bus Voltage	V_d	800 V
Maximum Peak Output Current	$I_{o(max)}$	200 A
Switching Frequency	f_s	10 kHz
Blanking Time	t_b	5 μ s
Maximum Duty Cycle	d_{max}	0.85
Load Impedance	Z_o	3.4 Ω

Table 2.2: Design parameters for experimental converter with turn-off snubber.

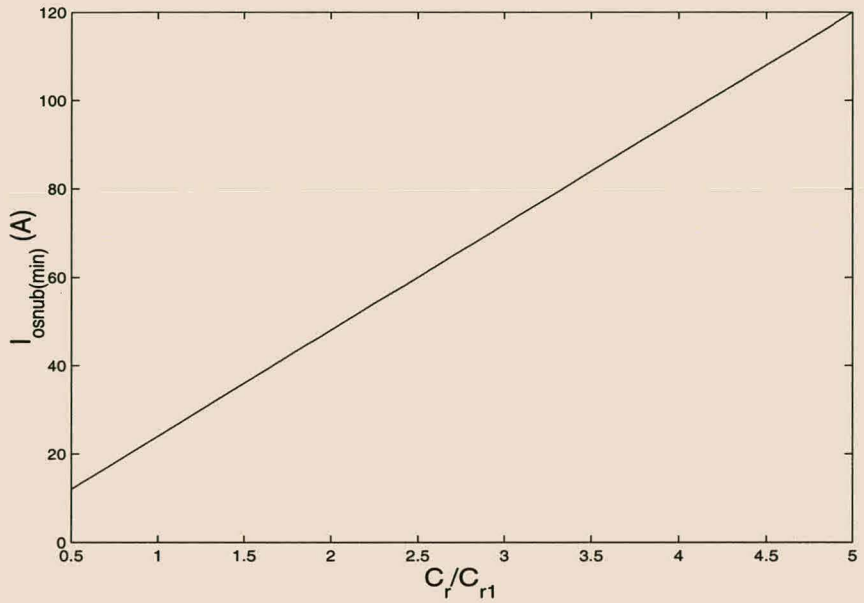


Figure 2.7: Minimum magnitude of output current at which snubber is triggered.

As mentioned earlier the minimum magnitude of the output current at which the snubber can be used is determined by the blanking time t_b and is given by equation 2.14. Figure 2.7 shows this minimum value $I_{osnub(min)}$ of the magnitude of the output current as a function of the size of the snubber capacitor C_r.

A capacitor discharge time t_1 of 10 μs is chosen in order to obtain the lowest possible peak current rating of the auxiliary switches with a maximum duty cycle of 0.85. From the fact that $t_1 = \frac{\pi}{\omega_0}$ it follows that the maximum value of the resonant inductor as a function of t_1 and C_r is given by

$$L_r = \frac{t_1^2}{\pi^2 C_r}. \tag{2.16}$$

Figure 2.8 shows the value of the resonant inductor L_r as a function of C_r based on this equation. It is important to note that the auxiliary inductor carries a very small average current.

From equations 2.11 and 2.16 the peak current rating $I_{L_r(max)}$ of the auxiliary switches is given

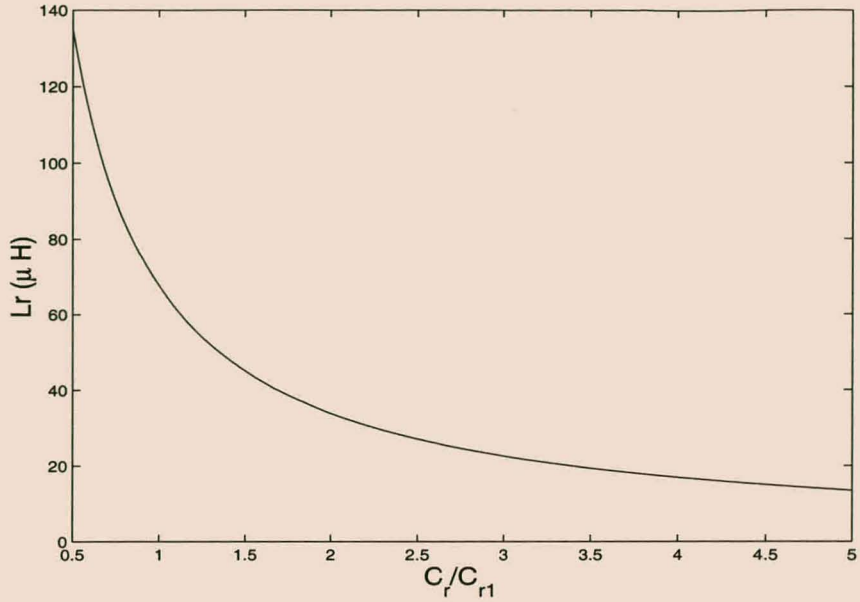


Figure 2.8: L_r as a function of C_r for a capacitor discharge time $t_1 = 10\mu$s.

by

$$I_{L_r(max)} = \frac{\pi V_d C_r}{2t_1} \tag{2.17}$$

and is shown in Figure 2.9. For $C_r = C_{r_1}$ the peak current rating of the auxiliary switch is approximately 20 A. This means that an IGBT with an average current rating of approximately 10 A can be used as an auxiliary switch. The rated voltage of the IGBT is 600 V. A 600 V diode has to be connected in series with the IGBT to provide the required reverse blocking capability. The total power rating of the auxiliary IGBT is only 3% of that of the main module. For the ARCP converter the peak current rating of the auxiliary switch is between 120% and 180% ([105] p. 106) of that of the main switches, with half the voltage rating of the main switches.

2.2.4 Evaluating the snubber losses

One of the key considerations when designing the turn-off snubber is to obtain the optimum balance between the reduction in turn-off loss in the main IGBT and the losses in the snubber circuit itself. In this section the different loss mechanisms are studied, including the losses in the resonant inductor, auxiliary switch and other parasitic components. Experience with ARCP-based converters [105] has shown that losses in the resonant inductor and auxiliary switches are significant compared to the reduction in switching loss in the main IGBT. It is important to have reasonable estimates of the losses in the different snubber components when designing these components.

It will later be shown that the snubber and main module parasitic inductances have a major influence on the snubber's effectiveness. The exact value of this inductance can only be measured

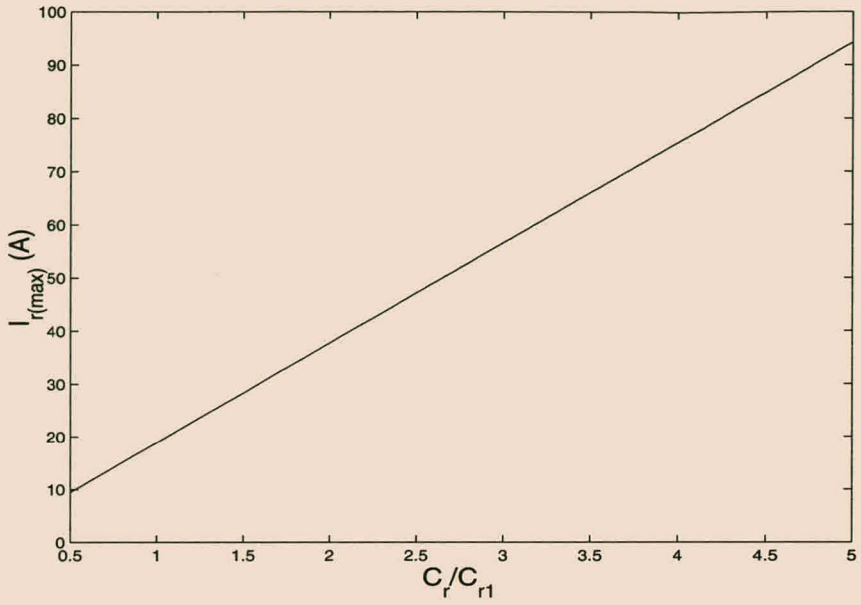


Figure 2.9: Peak current rating of the auxiliary switches as a function of C_r.

once the snubber has been constructed and is not taken into account in the initial evaluation of the total turn-off loss. Great care should be taken in the physical layout to keep this parasitic inductance as low as possible.

A number of studies on the switching behavior of IGBTs under soft-switched conditions can be found in the literature (see, for instance, [59], [56] and [55]). Detailed simulations are, however, complicated and require device parameters that are not readily available. The approach followed in this thesis is a 'first-order optimization process'. As a first step it is assumed that the snubber does not affect the switching behavior of the main IGBT. The design can then be iteratively refined by constructing the snubber, measuring its switching behavior and again applying the first-order optimization technique.

The final aim with the analysis of this section is to develop an optimal snubber design procedure which will result in a design that will minimize the total converter switching loss. Although the losses can be calculated through numerical simulation, this results in excessive calculation times when calculated over a full fundamental cycle of the output current for a variety of different snubber parameters. For this reason analytical expressions are developed for the different loss components. A more complete analysis of the snubber, taking the effect of the parasitic components on the snubber operation into account, will be made in the next section. This more complete model can be used to fine-tune the optimal design process.

Two different cycles of operation are studied, namely the main module turn-off cycle and the capacitor discharge cycle.

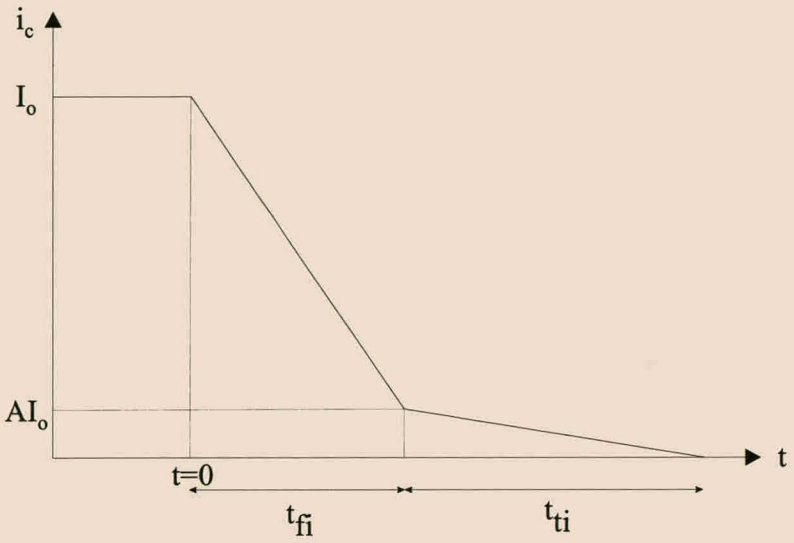


Figure 2.10: The turn-off tail current characteristic of an IGBT.

2.2.4.1 Main IGBT turn-off cycle

In the first part of this section the IGBT tail-forming characteristics are used to model the turn-off loss of an IGBT converter fitted with the resonant turn-off snubber. Figure 2.10 shows the turn-off tail current characteristic of an IGBT. The main difference between the IGBT turn-off behavior and that of a power MOSFET is the fact that the collector current waveform can be separated into two distinct time intervals. The rapid turn-off during t_{fi} is due to the MOSFET portion of the IGBT. The 'tailing' during the second interval t_{ti} is due to stored charge in the n^- drift region of the IGBT. During this period excess carriers are removed through recombination. When shortening time t_{ti}, the on-state voltage is increased, which results in increased conduction loss. As in a bipolar transistor, t_{ti} increases with increased temperature.

The approach followed in this section is based on that in [54]. Unlike in [54] the losses in a number of parasitic components are taken into account.

The following assumptions are made in the current analysis:

1. During turn-off the IGBT collector current declines to zero in two time-linear segments. The first segment is of duration t_{fi} (current fall time), while the second segment is of duration t_{ti} (current tail time). These two segments are described by the following equations:

$$i_c(t) = \begin{cases} I_o\left(1 + (A-1)\frac{t}{t_{fi}}\right) & \text{if } 0 \le t \le t_{fi} \\ AI_o\left(1 - \frac{t-t_{fi}}{t_{ti}}\right) & \text{if } t_{fi} \le t \le t_{fi} + t_{ti} \end{cases} \tag{2.18}$$

2. The turn-off current waveform of the IGBT is not affected by the snubber. That means

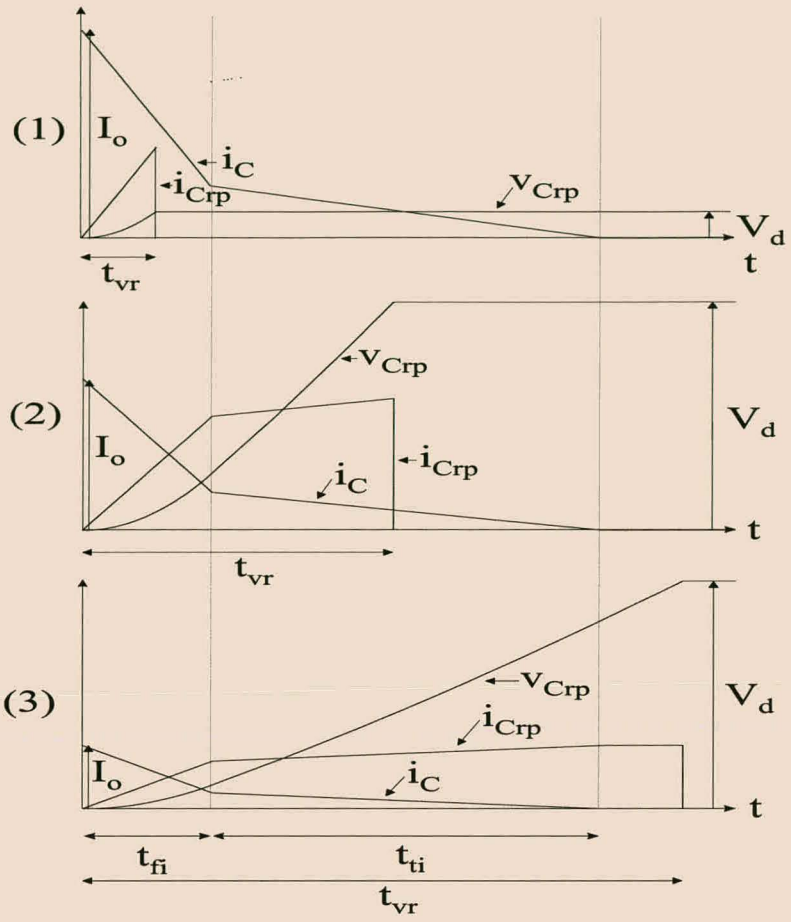


Figure 2.11: Three cases of snubber operation during main module turn-off.

that the current fall and tail times t_{fi} and t_{ti} are not functions of the snubber size. Furthermore, the knee-point current AI_o is only a function of the output current I_o and not of the snubber size.

3. The snubber diode is ideal. This means that it switches instantaneously from one state to the other and has no conduction loss.

4. There are no parasitic inductances in the snubber circuit.

5. The snubber capacitor is ideal. It is totally linear and has no equivalent series resistance (ESR).

Figure 2.11 shows three different cases of turn-off waveforms depending on the magnitude of the output current I_o and the size of the snubber capacitor C_r. Define the *voltage rise time* t_{vr} as the time when $v_{C_{rp}}$ reaches V_d.

1. In this case the capacitor voltage $v_{C_{rp}}$ reaches V_d at time less than or equal to t_{fi}. At this instant diode D_n becomes forward biased, starts conducting and clamps the voltage over

C_{rp} to V_d. For $0 \leq t \leq t_{vr}$ voltage $v_{C_{rp}}$ is given by

$$\begin{aligned} v_{C_{rp}} &= \frac{1}{C_r}\int_0^t i_{C_{rp}}(\tau)\,d\tau \\ &= \frac{I_o t^2(1-A)}{2C_r t_{fi}} \end{aligned} \tag{2.19}$$

and t_{vr} is given by

$$t_{vr} = \sqrt{\frac{2V_d C_r t_{fi}}{I_o\,(1-A)}}. \tag{2.20}$$

This also implies that, in terms of the load current, $t_{vr} \leq t_{fi}$ when

$$I_o \geq \frac{2V_d C_r}{t_{fi}(1-A)}. \tag{2.21}$$

The energy W_{off} dissipated in the main top IGBT during turn-off is given by

$$\begin{aligned} W_{off} &= \int_0^{t_{vr}} i_c v_{C_{rp}}\,dt + \int_{t_{vr}}^{t_{fi}+t_{ti}} i_c V_d\,dt \\ &= \frac{I_o^2}{2C_r t_{fi}}\left((1-A)\frac{t_{vr}^3}{3} - (1-A)^2\frac{t_{vr}^4}{4t_{fi}}\right) \\ &\quad + V_d I_o\left(t_{fi} - t_{vr} + (A-1)\frac{t_{fi}^2 - t_{vr}^2}{2t_{fi}}\right) + V_d A I_o \frac{t_{ti}}{2}. \end{aligned} \tag{2.22}$$

2. In this case $t_{fi} \leq t_{vr} \leq t_{fi} + t_{ti}$. For $0 \leq t \leq t_{fi}$ voltage $v_{C_{rp}}$ is given by equation 2.19, while for $t_{fi} \leq t \leq t_{vr}$

$$v_{C_{rp}} = \frac{I_o t_{fi}(1-A)}{2C_r} + \frac{I_o}{C_r}\left((t-t_{fi})(1-A) + A\frac{(t-t_{fi})^2}{2t_{ti}}\right) \tag{2.23}$$

and $v_{C_{rp}}$ reaches V_d when

$$t_{vr} = t_{fi} - \frac{1-A}{A}t_{ti} + \sqrt{\left(\frac{1-A}{A}t_{ti}\right)^2 - \frac{1-A}{A}t_{fi}t_{ti} + \frac{2C_r V_d t_{ti}}{I_o A}}. \tag{2.24}$$

In terms of the load current $t_{fi} \leq t_{vr} \leq t_{fi} + t_{ti}$ when

$$\frac{2V_d C_r}{t_{fi}(1-A)} \geq I_o \geq \frac{V_d C_r}{(1-A)\frac{t_{fi}}{2} + t_{ti} - \frac{A}{2}t_{ti}}. \tag{2.25}$$

The energy dissipated in the main IGBT during turn-off is given by

$$\begin{aligned} W_{off} &= \int_0^{t_{vr}} i_c v_{C_{rp}}\,dt + \int_{t_{vr}}^{t_{fi}+t_{ti}} i_c V_d\,dt \\ &= \frac{I_o^2}{2C_r}\left((1-A)\frac{t_{fi}^2}{3} - (1-A)^2\frac{t_{fi}^2}{4}\right) \\ &\quad + \frac{AI_o^2}{C_r}\left(t_{fi}\frac{1-A}{2}(t_{vr}-t_{fi}) + \frac{(1-A)}{2}(t_{vr}-t_{fi})^2 + A\frac{(t_{vr}-t_{fi})^3}{6t_{ti}}\right. \\ &\quad \left. - \frac{(1-A)t_{fi}}{4t_{ti}}(t_{vr}-t_{fi})^2 - \frac{1-A}{3t_{ti}}(t_{vr}-t_{fi})^3 - \frac{A}{8t_{ti}^2}(t_{vr}-t_{fi})^4\right) \\ &\quad + V_d A I_o\left(t_{fi} + t_{ti} - t_{vr} - \frac{t_{ti}}{2} + \frac{(t_{vr}-t_{fi})^2}{2t_{ti}}\right). \end{aligned} \tag{2.26}$$

3. In this case $t_{vr} \geq t_{fi} + t_{ti}$. The voltage over C_{rp} is given by equation 2.19 for $0 \leq t \leq t_{fi}$ and equation 2.23 for $t_{fi} \leq t \leq t_{fi} + t_{ti}$. For $t_{fi} + t_{ti} \leq t \leq t_{vr}$ voltage $v_{C_{rp}}$ is given by

$$v_{C_{rp}} = \frac{I_o t_{fi}(1-A)}{2C_r} + \frac{I_o}{C_r}\left(t_{ti}(1-A) + A\frac{t_{ti}}{2}\right) + \frac{I_o}{C_r}(t - t_{fi} - t_{ti}) \tag{2.27}$$

and $v_{C_{rp}}$ reaches V_d when

$$t_{vr} = \frac{C_r}{I_o}\left(V_d - \frac{I_o t_{fi}(1-A)}{2C_r} - \frac{I_o t_{ti}}{C_r}\left(1 - \frac{A}{2}\right)\right) + t_{ti} + t_{fi}. \tag{2.28}$$

In terms of the load current $t_{vr} \geq t_{fi} + t_{ti}$ when

$$I_o \leq \frac{V_d C_r}{(1-A)\frac{t_{fi}}{2} + t_{ti} - \frac{A}{2}t_{ti}}. \tag{2.29}$$

The energy dissipated in the main IGBT during turn-off is given by

$$\begin{aligned} W_{off} &= \int_0^{t_{fi}} i_c v_{C_{rp}}\, dt + \int_{t_{fi}}^{t_{fi}+t_{ti}} i_c v_{C_{rp}}\, dt \\ &= \frac{I_o^2 t_{fi}^2}{2C_r}\left(\frac{(1-A)}{3} - \frac{(1-A)^2}{4}\right) \\ &\quad + \frac{AI_o^2}{C_r}\left(\frac{t_{fi}t_{ti}(1-A)}{4} + \frac{t_{ti}^2(1-A)}{6} + \frac{t_{ti}^2 A}{24}\right). \end{aligned} \tag{2.30}$$

The remainder of the section is devoted to calculating the loss in snubber diode D_{rp} and snubber capacitor C_{rp}. Diode D_{rp} is modeled by its on-state voltage $V_{D_{rp}}$ in series with a resistor R_{D_r}. The forward recovery of diode D_{rp} is not taken into account. Furthermore, when diode D_{rp} turns off, the reverse voltage across it is small. Hence the diode's turn-off process is governed by recombination. For this reason the reverse recovery loss is not considered. Capacitor C_r is modeled as an ideal capacitor in series with its equivalent series resistance R_{C_r}.

Again three cases of the output current I_o have to be considered:

1. If $t_{vr} \leq t_{fi}$, the loss in diode D_{rp} is given by

$$\begin{aligned} W_{D_r} &= \int_0^{t_{vr}} V_{D_r} i_{C_{rp}}\, dt + \int_0^{t_{vr}} R_{D_r} i_{C_{rp}}^2\, dt \\ &= V_{D_R} I_o (1-A)\frac{t_{vr}^2}{2t_{fi}} + R_{D_r} I_o^2 (1-A)^2 \frac{t_{vr}^3}{3t_{fi}^2}, \end{aligned} \tag{2.31}$$

while the loss in capacitor C_{rp} is given by

$$\begin{aligned} W_{C_r} &= \int_0^{t_{vr}} R_{C_r} i_{C_{rp}}^2\, dt \\ &= R_{C_r} I_o^2 (1-A)^2 \frac{t_{vr}^3}{3t_{fi}^2}. \end{aligned} \tag{2.32}$$

2. In this case $t_{fi} \leq t_{vr} \leq t_{fi} + t_{ti}$. The loss in diode D_{rp} is given by

$$\begin{aligned} W_{D_r} &= \int_0^{t_{vr}} V_{D_r} i_{C_{rp}}\, dt + \int_0^{t_{vr}} R_{D_r} i_{C_{rp}}^2\, dt \\ &= V_{D_r} I_o (1-A)\frac{t_{fi}}{2} + R_{D_r} I_o^2 (1-A)^2 \frac{t_{fi}}{3} \\ &\quad + \frac{V_{D_r} I_o t_{ti}}{2A}\left(1 - A\left(1 - \frac{t_{vr}-t_{fi}}{t_{ti}}\right)^2 - (1-A)^2\right) \\ &\quad + \frac{R_{D_r} I_o^2 t_{ti}}{3A}\left(1 - A\left(1 - \frac{t_{vr}-t_{fi}}{t_{ti}}\right)^3 - (1-A)^3\right), \end{aligned} \tag{2.33}$$

while the loss in capacitor C_{rp} is given by

$$\begin{aligned} W_{C_r} &= \int_0^{t_{vr}} R_{C_r} i_{C_{rp}}^2\, dt \\ &= R_{C_r} I_o^2 (1-A)^2 \frac{t_{fi}}{3} \qquad (2.34) \\ &\quad + \frac{R_{C_r} I_o^2 t_{ti}}{3A}\left(\left(1 - A\left(1 - \frac{t_{vr}-t_{fi}}{t_{ti}}\right)\right)^3 - (1-A)^3\right). \qquad (2.35) \end{aligned}$$

3. Finally, if $t_{fi} + t_{ti} \leq t_{vr}$, the loss in D_{rp} is given by

$$\begin{aligned} W_{D_r} &= \int_0^{t_{vr}} V_{D_r} i_{C_{rp}}\, dt + \int_0^{t_{vr}} R_{D_r} i_{C_{rp}}^2\, dt \\ &= V_{D_r} I_o (1-A)\frac{t_{fi}}{2} + R_{D_r} I_o^2 (1-A)^2 \frac{t_{fi}}{3} \\ &\quad + V_{D_r} I_o \frac{t_{ti}}{2A}\left(1 - (1-A)^2\right) + R_{D_r} I_o^2 \frac{t_{ti}}{3A}\left(1 - (1-A)^3\right) \\ &\quad + V_{D_r} I_o (t_{vr} - t_{fi} - t_{ti}) + R_{D_r} I_o^2 (t_{vr} - t_{fi} - t_{ti}), \end{aligned} \tag{2.36}$$

and the loss in C_{rp} is given by

$$\begin{aligned} W_{C_r} &= \int_0^{t_{vr}} R_{C_r} i_{C_{rp}}^2\, dt \\ &= R_{C_r} I_o^2 (1-A)^2 \frac{t_{fi}}{3} + R_{C_r} I_o^2 \frac{t_{ti}}{3A}\left(1 - (1-A)^3\right) + R_{C_r} I_o^2 (t_{vr} - t_{fi} - t_{ti}). \end{aligned} \tag{2.37}$$

2.2.4.2 Auxiliary discharging cycle

In this section the losses in the auxiliary discharging circuit are analyzed. Figure 2.12 shows the auxiliary discharging circuit and its equivalent circuit used to analyze the conduction and switching losses during snubber capacitor discharge. Although the auxiliary switch S_{rp} consists of an IGBT in series with a diode (for reverse blocking purposes), the analysis is general and applies to thyristors, MOSFETs and GTOs.

The IGBT and series diode are modeled by their on-state voltages V_{sa} and V_{da} and on-state resistances R_{sa} and R_{da}, respectively. The conduction loss of the resonant inductor L_{rp} is

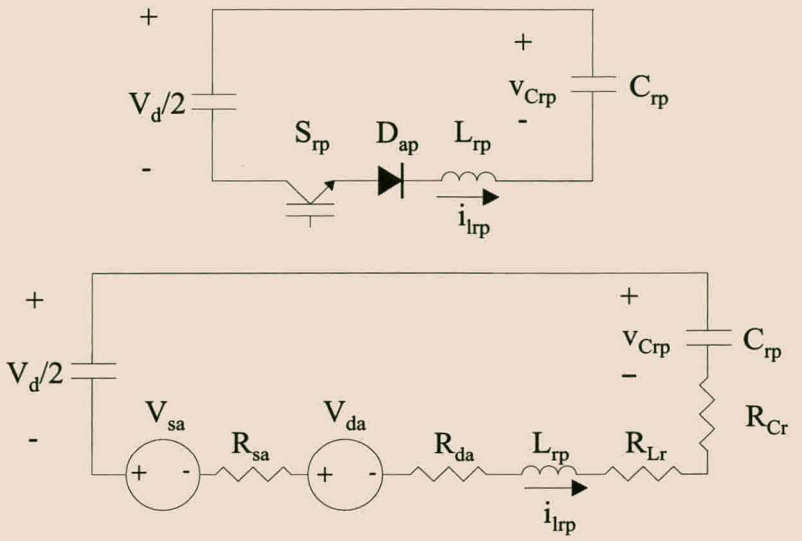


Figure 2.12: Auxiliary discharging circuit. Top: Auxiliary circuit. Bottom: Equivalent circuit.

modeled by a series resistor R_{L_r}. The loss in the snubber capacitor C_{rp} is presented by its equivalent series resistance R_{C_r}. Although these components will modify the behavior of the resonant circuit itself, the effect will not be taken into account in this section. The idealized equations of section 2.2.2 will be used for the voltage and current waveforms.

During the capacitor discharge cycle the conduction loss $W_{sa(cond)}$ in the auxiliary IGBT is given by

$$\begin{aligned} W_{sa(cond)} &= \int_0^{\frac{\pi}{\omega_0}} \left(i_{L_{rp}}^2 R_{sa} + i_{L_{rp}} V_{sa} \right) dt \\ &= \int_0^{\frac{\pi}{\omega_0}} \left(R_{sa} \left(\frac{V_d}{2} \sqrt{\frac{C_r}{L_r}} \sin(\omega_0 t) \right)^2 + \frac{V_{sa} V_d}{2} \sqrt{\frac{C_r}{L_r}} \sin(\omega_0 t) \right) dt \\ &= \frac{\pi R_{sa} V_d^2 C_r}{8} \sqrt{\frac{C_r}{L_r}} + V_{sa} V_d C_r, \end{aligned} \tag{2.38}$$

while the conduction loss in the series diode is given by

$$\begin{aligned} W_{da(cond)} &= \int_0^{\frac{\pi}{\omega_0}} \left(i_{L_{rp}}^2 R_{da} + i_{L_{rp}} V_{da} \right) dt \\ &= \int_0^{\frac{\pi}{\omega_0}} \left(R_{da} \left(\frac{V_d}{2} \sqrt{\frac{C_r}{L_r}} \sin(\omega_0 t) \right)^2 + \frac{V_{da} V_d}{2} \sqrt{\frac{C_r}{L_r}} \sin(\omega_0 t) \right) dt \\ &= \frac{\pi R_{da} V_d^2 C_r}{8} \sqrt{\frac{C_r}{L_r}} + V_{da} V_d C_r. \end{aligned} \tag{2.39}$$

The loss in the resonant inductor L_{rp} is given by

$$\begin{aligned} W_{L_r} &= \int_0^{\frac{\pi}{\omega_0}} i_{L_{rp}}^2 R_{L_r} \, dt \\ &= \int_0^{\frac{\pi}{\omega_0}} R_{L_r} \left(\frac{V_d}{2} \sqrt{\frac{C_r}{L_r}} \sin(\omega_0 t) \right)^2 dt \end{aligned}$$

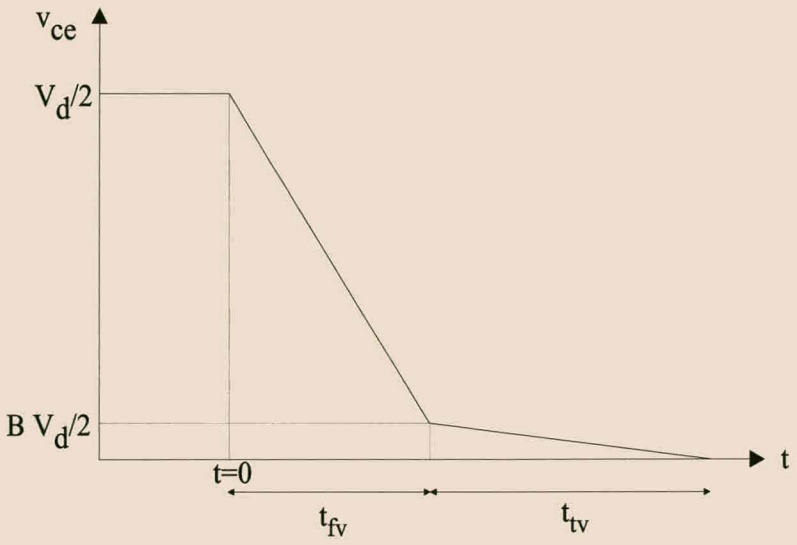


Figure 2.13: IGBT tail voltage characteristic.

$$= \frac{\pi R_{L_r} V_d^2 C_r}{8} \sqrt{\frac{C_r}{L_r}}. \tag{2.40}$$

Similarly the loss in the snubber capacitor C_{rp} is given by

$$\begin{aligned} W_{C_r} &= \int_0^{\frac{\pi}{\omega_0}} i_{L_{rp}}^2 R_{C_r}\, dt \\ &= \int_0^{\frac{\pi}{\omega_0}} R_{C_r} \left(\frac{V_d}{2} \sqrt{\frac{C_r}{L_r}} \sin(\omega_0 t) \right)^2 dt \\ &= \frac{\pi R_{C_r} V_d^2 C_r}{8} \sqrt{\frac{C_r}{L_r}}. \end{aligned} \tag{2.41}$$

In order to model the turn-on loss in the auxiliary switch, voltage tail-forming characteristics during turn-on are assumed. These characteristics are similar to the current tail forming characteristics described in section 2.2.4.1. Even though the tail voltage during turn-on is characteristic of an IGBT, the approach presented here can be applied to switching devices without voltage tails (like thyristors and MOSFETs) by taking t_{tv} equal to zero. The following assumptions are made during the analysis:

1. At the auxiliary switch turn-on instant the snubber capacitor C_{rp} is charged to voltage $v_{C_{rp}} = V_d$. Furthermore, it is assumed that the top and bottom DC-bus voltages are equal to $\frac{V_d}{2}$ and $-\frac{V_d}{2}$, respectively. This implies that the collector-emitter voltage across the resonant switch is equal to $\frac{V_d}{2}$ prior to turn-on.

2. During turn-on the voltage over the IGBT declines to zero in two time-linear segments. The first is of duration t_{fv} (voltage fall time), while the second is of duration t_{tv} (voltage tail time). These two segments are described by

$$v_{ce}(t) = \begin{cases} \frac{V_d}{2} \left(1 + (B-1) \frac{t}{t_{fv}} \right) & \text{if } 0 \le t \le t_{fv} \\ \frac{V_d}{2} B \left(1 - \frac{t - t_{fv}}{t_{tv}} \right) & \text{if } t_{fv} \le t \le t_{fv} + t_{tv}. \end{cases} \tag{2.42}$$

3. The turn-on voltage waveform of the IGBT is not affected by the snubber components. This means that the voltage fall and tail times t_{fv} and t_{tv} are not dependent on the snubber components C_{rp} and L_{rp}. Furthermore, the knee-voltage $B\frac{V_d}{2}$ is only a function of the total DC-bus voltage V_d.

4. The forward recovery and on-state voltage of the series diode is not taken into account in modeling the turn-on behavior of the auxiliary switch.

5. The time $t_1 = \frac{\pi}{\omega_0}$ taken to complete the resonant half cycle is significantly longer than the turn-on time of the auxiliary switch. Furthermore it is assumed that the voltage across C_{rp} is equal to V_d during the turn-on period of the auxiliary switch.

Under the above assumptions, current $i_{L_{rp}}$ during the auxiliary switch turn-on cycle is given by

$$i_{L_{rp}} = \begin{cases} \frac{V_d}{4L_r}(1-B)\frac{t^2}{t_{fv}} & \text{if } 0 \leq t \leq t_{fv} \\ \frac{V_d t_{fv}(1-B)}{4L_r} + \frac{V_d}{2L_r}\left((t-t_{fv})(1-B) + B\frac{(t-t_{fv})^2}{2t_{tv}}\right) & \text{if } t_{fv} \leq t \leq t_{fv}+t_{tv}, \end{cases} \tag{2.43}$$

while the switching loss in the auxiliary switch is given

$$\begin{aligned} W_{sa(switch)} &= \int_0^{t_{fv}} v_{ce} i_{L_{rp}}\, dt + \int_{t_{fv}}^{t_{fv}+t_{tv}} v_{ce} i_{L_{rp}}\, dt & (2.44) \\ &= \frac{V_d^2 t_{fv}^2}{8L_r}\left(\frac{(1-B)}{3} - \frac{(1-B)^2}{4}\right) \\ &\quad + \frac{BV_d^2}{4L_r}\left(\frac{t_{fv}t_{tv}(1-B)}{4} + \frac{t_{tv}^2(1-B)}{6} + \frac{t_{tv}^2 B}{24}\right). & (2.45) \end{aligned}$$

Finally, the reverse recovery loss in the series diode is evaluated. Based on Figure 2.14 (with $V_r = \frac{V_d}{2}$) the energy dissipated in the series diode due to reverse recovery can be roughly approximated by

$$W_{rr} \approx \frac{I_{rr} t_{rr} V_d}{8}. \tag{2.46}$$

Given the reverse recovery time, the peak reverse recovery current can be approximated by

$$I_{rr} \approx -\frac{di_R}{dt}\frac{t_{rr}}{2}. \tag{2.47}$$

Calculating $\frac{di_R}{dt}$ by making use of equation 2.9 results in

$$\frac{di_R}{dt} = -\frac{V_d}{2L_R}. \tag{2.48}$$

Hence

$$W_{da(rr)} \approx \frac{V_d^2 t_{rr}^2}{32L_R}. \tag{2.49}$$

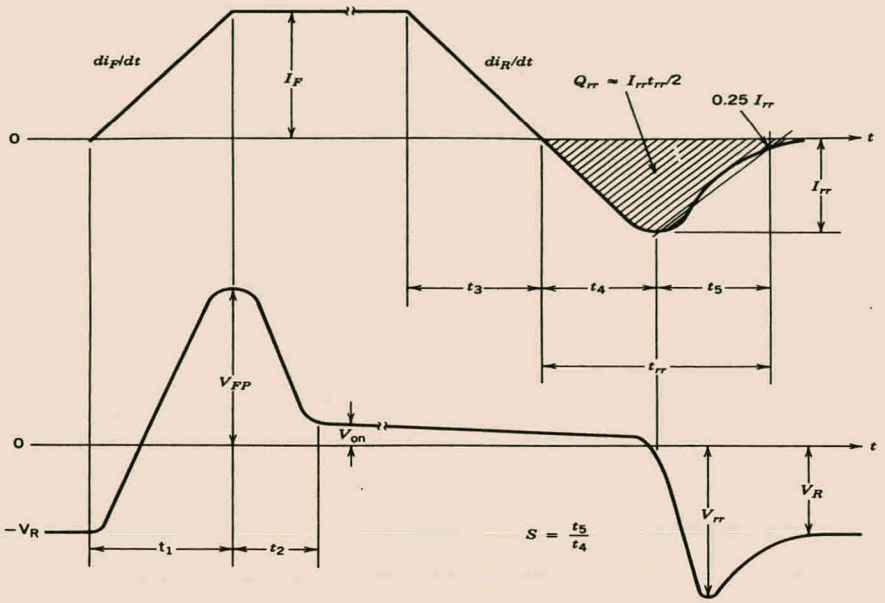


Figure 2.14: Diode forward and reverse recovery (taken from [10]).

2.2.5 Optimal snubber design

The aim of this section is to establish a design procedure in order to minimize the total turn-off (both the main IGBT turn-off and snubber circuit) losses of a phase-arm fitted with the resonant turn-off snubber.

A number of papers deal with optimal design of snubber and soft-switching circuits. In [40] optimal design procedures for non-regenerative RCD snubbers are presented. Some of the results of this paper can be found in standard text-books, for instance [10]. In [59] mixed mode simulation is used to study the behavior of IGBTs under soft-switched conditions. An optimal design process for non-linear turn-off snubbers is presented in [53]. As mentioned earlier, [54] contains optimal design methodologies for power electronic switches with both voltage and current tails. Most of the approaches mentioned do not consider the effect of the parasitic components in detail.

A number of decisions have to be made about the operation of the converter and the ratings of some of the snubber components before undertaking the optimal design procedure. These are:

1. The converter switching frequency f_s, maximum duty cycle d_{max} and blanking time t_b has to be selected. The blanking time places a limitation on the minimum load current I_o at which the snubber can be operated. As mentioned in section 2.2.2, turning the bottom IGBT on before snubber capacitor C_{r_p} is fully charged will result in excessive current

stress on the bottom IGBT, capacitor C_{r_p} and diode D_{r_p}. Hence auxiliary switch S_{r_p} is not triggered if

$$t_{vr} > t_b. \tag{2.50}$$

The maximum time available for the capacitor discharge cycle $t_{1(max)}$ is given by

$$t_{1(max)} = \frac{1 - d_{max}}{f_s} - t_b. \tag{2.51}$$

Since $t_1 = \frac{\pi}{\omega_0}$, the following limitation is placed on the maximum size of the resonant inductor

$$L_r \leq \frac{t_{1max}^2}{\pi^2 C_r}. \tag{2.52}$$

2. The peak current rating of the auxiliary switch $I_{r(max)}$ has to be selected. According to equation 2.11 this places a limitation on the minimum size of L_r

$$L_r \geq \frac{V_d^2 C_r}{4 I_{r(max)}^2}. \tag{2.53}$$

Together equations 2.52 and 2.53 give rise to the following limitation on the maximum value of C_r

$$C_r \leq \frac{2 t_{1(max)} I_{r(max)}}{\pi V_d}. \tag{2.54}$$

3. An estimate of the relationship between the inductance of the resonant inductor and its series resistance has to be made. In this section it will be assumed that the series resistance of the resonant inductor is given by

$$R_{L_r} = k_{R_{L_R}} L, \tag{2.55}$$

where $k_{R_{L_R}}$ is a constant. This approach is based on the following assumptions which give rise to equation 2.55:

   (a) A fixed diameter air core inductor consisting of a fixed volume V of copper is used to wind the inductor. The inductor is wound with Litz wire and hence the influence of the skin effect will be ignored in the optimal design procedure. Since a fixed volume of copper is used the series resistance increases linearly with l^2, where l is the length of the conductor used to wind the inductor.

   (b) The value of L_r increases linearly with l^2. This is the case if all the turns are of equal diameter.

The model of the losses in the resonant inductor will further be refined in section 2.2.7.4.

4. An estimate of the relationship between the value of C_r and its series resistance R_{C_r} has to be made. It is assumed that the required value of C_r can be achieved by stacking a number of small capacitors in parallel. Hence

$$R_{C_r} = \frac{k_{R_C}}{C_r}, \tag{2.56}$$

where k_{R_C} is a constant.

The optimal snubber design procedure is aimed at finding those values of C_r and L_r that will result in the least total turn-off losses (including the losses in the snubber circuit itself). The strategy is to calculate the total turn-off losses over one fundamental cycle of the output current for a range of different values of C_r and L_r. Those values of L_r and C_r that result in the minimum total losses over one fundamental cycle of the output current are selected as the optimal values. The details of the process are as follows:

1. The first step is to choose the range of values of C_r and L_r over which the optimization process will be performed. As a rough guideline the minimum value of C_r can be chosen as

$$C_{r(min)} = \frac{I_{o(max)} t_{fi}}{10 V_d}. \tag{2.57}$$

The maximum value of C_r is given by equation 2.54. The minimum and maximum values of L_r, for a specific value of C_r, are given by equations 2.53 and 2.52, respectively.

2. For each value of C_r and L_r the main IGBT turn-off loss and the losses in the auxiliary circuit are calculated over one cycle of the fundamental output current waveform, based on the loss equations of the previous section. In this chapter it is assumed that the output current contains relatively little ripple and is taken as constant over one switching cycle. If the details of the load and output filter are known the exact value of the output current at the switching instants can be used.

   Tables 2.3 and 2.4 summarize the equations used to calculate the individual loss components. If the voltage rise time of the snubber capacitor, t_{vr}, exceeds the blanking time t_b, operation of the discharge circuit is ceased. In this case the data sheet values of turn-off loss in the main IGBT are used, while the losses in the discharging circuit are taken as 0.

3. Those values of C_r and L_r which result in the lowest overall losses are selected as the optimum snubber parameters.

A Matlab program was written to perform the snubber optimization. This program is given in appendix A.

Parameter	Symbol	Equation number		
		Case 1 ($t_{vr} \leq t_{fi}$)	Case 2 ($t_{fi} \leq t_{vr} \leq t_{fi} + t_{ti}$)	Case 3 ($t_{vr} \geq t_{fi} + t_{ti}$)
Main Module Turn-off Loss	W_{off}	2.22	2.26	2.30
Snubber Diode Loss	W_{D_r}	2.31	2.33	2.36
Snubber Capacitor Loss	W_{C_r}	2.32	2.35	2.37

Table 2.3: Summary of loss equations during main module turn-off.

Parameter	Symbol	Equation number
Auxiliary Switch Conduction Loss	$W_{sa(cond)}$	2.38
Auxiliary Switch Switching Loss	$W_{sa(switch)}$	2.45
Auxiliary Diode Conduction Loss	$W_{da(cond)}$	2.39
Auxiliary Diode Reverse Recovery Loss	$W_{da(RR)}$	2.49
Resonant Inductor Loss	W_{L_r}	2.40
Snubber Capacitor Loss	W_{C_r}	2.41

Table 2.4: Summary of loss equations during the capacitor discharge cycle.

Example 2.2

In this example the optimal design procedure is applied to the example of section 2.2.3. Table 2.5 gives additional data on the PM200DSA IGBT module required in the optimization process. These values are taken from [105]. The snubber parameters are given in Table 2.6 and are based on data sheet values of typical components and typical inductor and capacitor characteristics from [105]. A 50 Hz sinusoidal output current waveform with a peak value of 200 A was used in the optimization process. The switching frequency f_s is 10 kHz.

Parameter	Symbol	Value
Current Fall Time	t_{fi}	250 ns
Current Tail Time	t_{ti}	500 ns
Tail Current Ratio	A	0.2
Turn-off Loss Coefficient	k_{Woff}	0.000 2 J/A

Table 2.5: Additional parameters of the Powerex PM200DSA120 IGBT module.

Figure 2.15 shows the sum of the turn-off and snubber losses as a function of the snubber capacitor C_r and snubber inductor L_r. The value of C_r ranges between 6 nF and 600 nF.

Parameter	Symbol	Value
Snubber Diode ESR	R_{D_r}	22 mΩ
Snubber Diode On-state Voltage	V_{D_r}	1.2 V
Snubber Capacitor ESR Coefficient	k_{R_C}	8×10^{-11} ΩF
Auxiliary Switch Peak Current Rating	$I_{r_{(max)}}$	75 A
Auxiliary Switch Voltage Fall Time	t_{fv}	250 ns
Auxiliary Switch Voltage Tail Time	t_{tv}	500 ns
Auxiliary Switch Tail Voltage Ratio	B	0.2
Auxiliary Switch ESR	R_{sa}	20 mΩ
Auxiliary Switch On-State Voltage	V_{sa}	1.2 V
Auxiliary Diode ESR	R_{da}	22 mΩ
Auxiliary Diode On-State Voltage	V_{da}	1.2 V
Auxiliary Diode Reverse Recovery Time	t_{rr}	100 ns
Resonant Inductor ESR Coefficient	k_{R_L}	20 000 Ω/H

Table 2.6: Snubber circuit parameters.

As C_R increases the allowable range of values of L_r shrinks. The optimal design value is at $C_r = 154$ nF and $L_r = 4.4$ μH, with the sum of the turn-off and snubber losses of the converter equal to 36.4 W.

Main IGBT Turn-off Loss	P_{off}	22.8 W
Snubber Diode Loss	P_{D_r}	4.5 W
Snubber Capacitor Loss	P_{C_r}	0.07 W
Resonant Inductor Loss	P_{L_r}	5.9 W
Auxiliary Switch Switching Loss	$P_{sa(switch)}$	0.006 W
Auxiliary Switch Conduction Loss	$P_{sa(cond)}$	2.7 W
Auxiliary Diode Reverse Recovery Loss	P_{rr}	0.42 W

Table 2.7: Losses in the main module IGBTs and snubber circuit calculated over one 50 Hz cycle.

Table 2.7 summarizes the losses in the individual components. The turn-off loss in the main IGBTs is 22.8 W and is the largest component of the total losses. The loss in the resonant inductor is the second largest component with a value of 5.9 W. Under hard-switched conditions the total converter turn-off loss is given by

$$\begin{aligned} P_{off(hs)} &= \frac{k_{Woff} f_s I_{o(peak)}}{\pi} \\ &= 127.3W. \end{aligned}$$

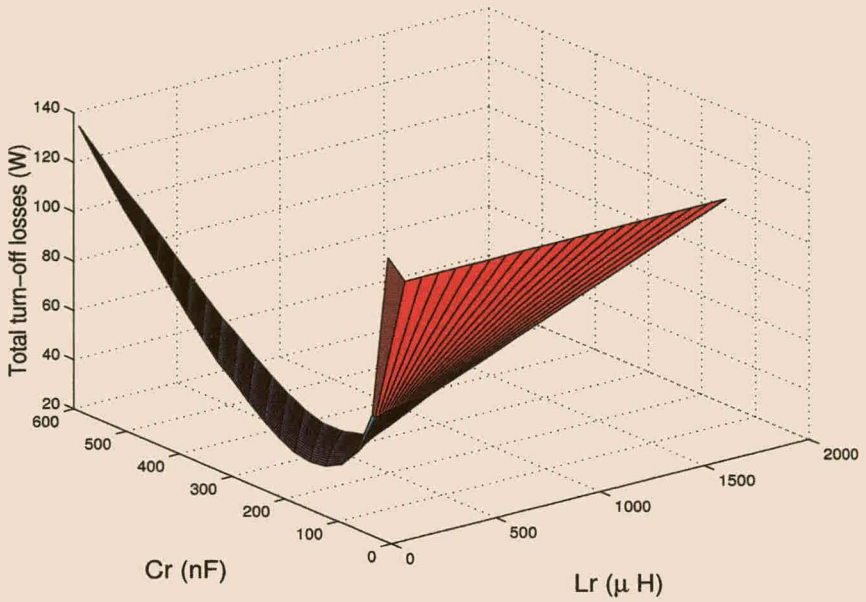


Figure 2.15: Sum of the turn-off and snubber losses of the converter for different values of C_r and L_r.

Hence, the snubber causes a decrease of 82% in the turn-off loss in the main IGBT and a decrease of 71% in the effective turn-off loss.

Parameter	Without Snubber	With snubber
Main Module Conduction Loss	229.2 W	229.2 W
Main Module Turn-on Loss	95.5 W	95.5 W
Turn-off Loss	127.3 W	22.8 W
Total Converter Loss	674.8 W	465.7 W
Converter Efficiency	98.0%	98.6%

Table 2.8: Summary of converter losses over one 50 Hz cycle with and without the snubber.

Table 2.8 summarizes the losses in the converter with and without the snubber. The addition of the snubber to the converter results in a decrease form 678.8 W to 465.6 W total converter loss. The converter efficiency increases from 98.0% to 98.6%.

2.2.6 Effect of the parasitic components

In this section the effects of parasitic components on the operation of the snubber, in particular the turn-off loss in the main IGBT module, are investigated in detail.

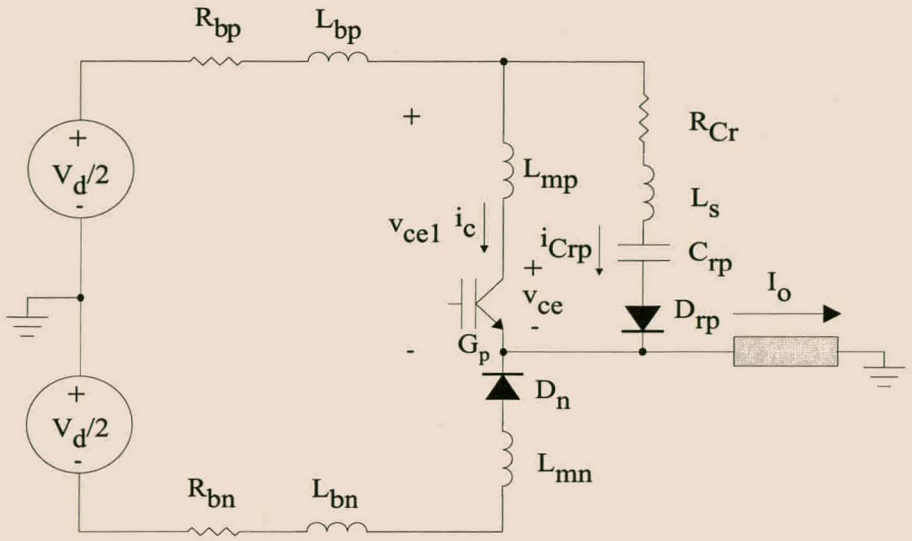


Figure 2.16: Parasitic components that influence the main IGBT turn-off cycle.

2.2.6.1 Main IGBT turn-off cycle

Figure 2.16 shows one half of the main IGBT module and turn-off snubber, including the parasitic components that influence the turn-off cycle. The DC-bus is considered as a perfect voltage source. The following parasitic components are included in the analysis:

1. The positive and negative rail bus-bar inductances L_{bp} and L_{bn}, and positive and negative rail bus-bar resistances R_{bp} and R_{bn}.

2. The parasitic inductance in the turn-off capacitor loop is represented by L_s. Resistor R_{C_r} represents the snubber capacitor ESR and any other resistance in the turn-off capacitor loop. In order to simplify the analysis the snubber diode resistance is included in R_{C_r}.

3. The internal inductance of the IGBT module is represented by inductances L_{mp} and L_{mn}.

Prior to the top IGBT G_p turning off, the load current I_o flows through R_{bp}, L_{bp}, L_{mp} and G_p. The IGBT tail-forming characteristics of section 2.2.4.1 are again used in this section to analyze the operation of the snubber during main-module turn-off. As G_p turns off, the current i_c through L_{mp} and G_p decreases as described by equation 2.18. Because the load current I_o is constant, the current through R_{C_r}, L_s, C_{rp} and D_{rp} increases. This results in an increase in v_{ce} given by

$$\Delta v_{ce} = -L_{mp}\frac{di_c}{dt} + L_s\frac{di_{C_{rp}}}{dt} + R_{C_r}i_{C_{rp}}, \tag{2.58}$$

compared to the idealized case of section 2.2.4.1. This increase in v_{ce} gives rise to increased turn-off loss in the main IGBT module.

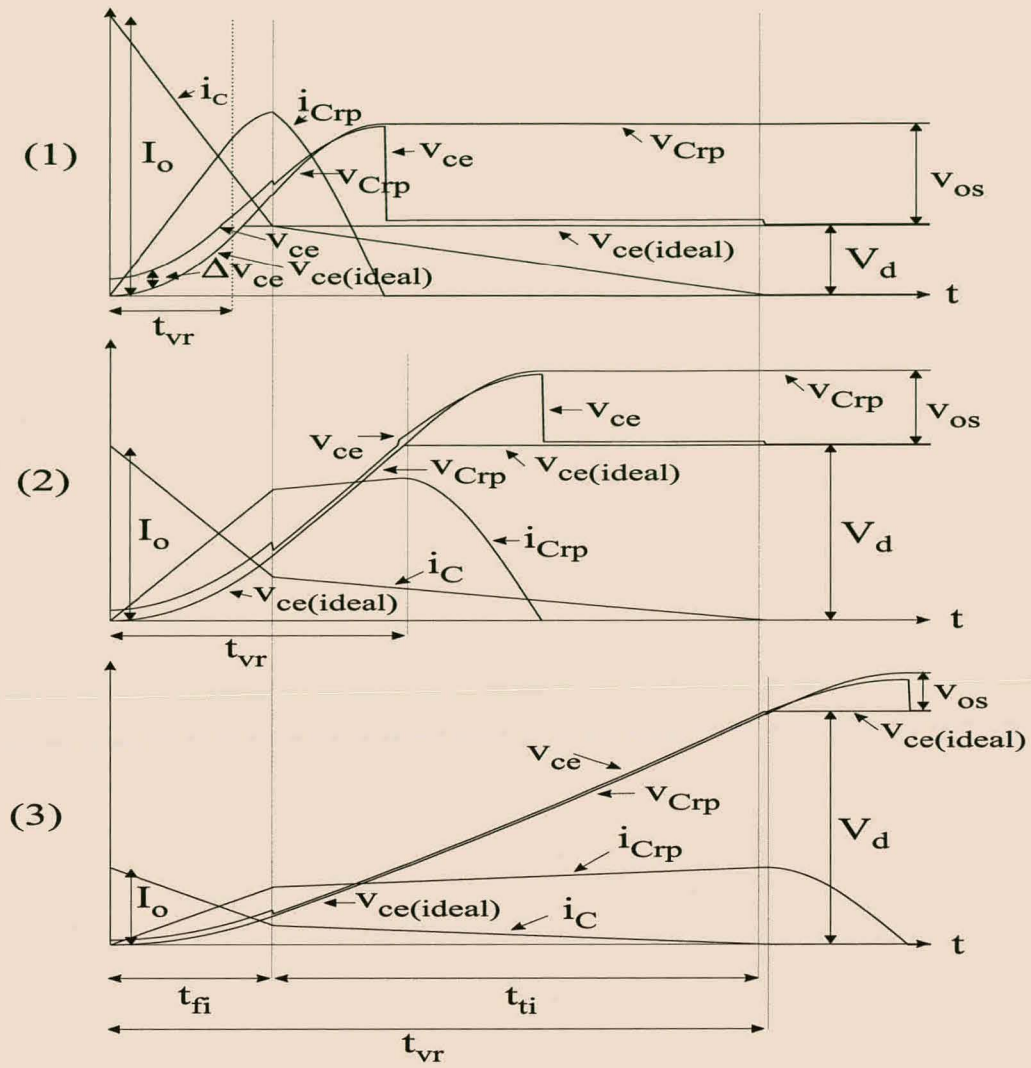


Figure 2.17: Effect of the parasitic components on the main IGBT turn-off waveforms.

In this section the voltage fall time t_{vr} is defined as the time when diode D_n becomes forward biased. As in section 2.2.4.1 three cases of the turn-off voltage waveforms can be identified as shown in Figure 2.17. This figure also shows the ideal v_{ce} waveform, without the presence of the parasitic components, which was derived in section 2.2.4.1. In case one $t_{vr} \leq t_{fi}$, while $t_{fi} \leq t_{vr} \leq t_{fi} + t_{ti}$ in case two, and $t_{vr} \geq t_{fi} + t_{ti}$ in case three. Voltage Δv_{ce} contains discontinuities at t_{fi} and $t_{fi} + t_{ti}$ as a result of the discontinuities of the derivatives of i_c and $i_{C_{rp}}$ in equation 2.58. Just before $i_{c_{rp}}$ reaches zero Δv_{ce} reverses sign as a result of the fact that the negative $\frac{di_{C_{rp}}}{dt}$ term dominates in equation 2.58.

When D_n turns on, at time t_{vr}, inductors L_{bp}, L_s, L_{mn}, L_{bn} and capacitor C_{rp} start to resonate, while L_{bn} takes over the load current I_o from L_{bp}. The result is a damped sinusoidal decrease in $i_{C_{rp}}$ to zero, combined with a voltage overshoot v_{os} in v_{ce} above its normal value of V_d. In the next section it will be shown that this is helpful during the capacitor discharging cycle. When $i_{C_{rp}}$ reaches zero, diode D_{rp} turns off.

The analytic solutions for voltages v_{crp}, v_{ce} and current $i_{C_{rp}}$ are mathematically involved and provide little insight into the snubber operation. These analytic expressions can be found in the Matlab program presented in Appendix A.

Both the increase in v_{ce} at the start of the turn-off cycle and the overshoot in v_{ce} near the end of the turn-off cycle leads to increased turn-off loss in the main IGBT module. The exact turn-off loss is in this case easiest to calculate through numerical integration.

Some attention should be given to the voltage overshoot v_{os} in case three. This is also the case of the greatest practical importance. The optimal snubber design typically results in a large enough value of C_r such that case three is valid throughout the largest part of the operating range of the snubber.

For $t_{fi} + t_{ti} \leq t \leq t_{vr}$ voltage v_{ce} is given by

$$v_{ce} = \frac{I_o t_{fi}(1-A)}{2C} + \frac{I_o}{C_r}\left(t_{ti}(1-A) + A\frac{t_{ti}}{2}\right) + \frac{I_o}{C_r}(t - t_{fi} - t_{ti}) + R_{C_r} I_o \tag{2.59}$$

and t_{vr} is given by

$$t_{vr} = t_{fi} + t_{ti} + \frac{C_r}{I_o}\left(V_d - \frac{I_o t_{fi}(1-A)}{2C_r} - \frac{I_o t_{ti}}{C_r}\left(1 - \frac{A}{2}\right) - R_{C_r} I_o\right). \tag{2.60}$$

The next step is to analyze the behavior of the circuit for $t \geq t_{vr}$. Let

$$\alpha = -\frac{R_{bp} + R_{C_r} + R_{bn}}{2(L_{bp} + L_s + L_{mn} + L_{bn})} \tag{2.61}$$

and

$$\beta = \sqrt{\frac{1}{C_r(L_{bp} + L_s + L_{mn} + L_{bn})} - \left(\frac{R_{bp} + R_{C_r} + R_{bn}}{2(L_{bp} + L_s + L_{mn} + L_{bn})}\right)^2}. \tag{2.62}$$

Then for $t \geq t_{vr}$

$$v_{C_{rp}} = e^{\alpha(t - t_{vr})}\left(a\cos\beta(t - t_{vr}) + b\sin\beta(t - t_{vr})\right) + V_d \tag{2.63}$$

and

$$i_{C_{rp}} = C_{rp} e^{\alpha(t - t_{vr})}\left((\alpha a + \beta b)\cos\beta(t - t_{vr}) + (\alpha b - \beta a)\sin\beta(t - t_{vr})\right) \tag{2.64}$$

where $a = -R_{C_r} I_o$ and $b = \frac{I_o}{\beta}(\frac{1}{C_r} - R_{C_r})$. Current $i_{C_{rp}}$ reaches zero (and D_{rp} turns off) when

$$t = t_z := t_{vr} + \frac{\arctan\left(\frac{\alpha a + \beta b}{\beta a - \alpha b}\right)}{\beta}. \tag{2.65}$$

Hence the maximum voltage overshoot $v_o s$ is given by

$$v_{os} = e^{\alpha(t_z - t_{vr})}\left(a\cos\beta(t_z - t_{vr}) + b\sin\beta(t_z - t_{vr})\right). \tag{2.66}$$

Example 2.3

In this example the effect of the parasitic components on the example of section 2.2.5 is investigated. Table 2.9 shows the parasitic component values. These values are based on typical measurements made in [105].

Parameter	Symbol	Value
Positive Bus-bar Inductance	L_{bp}	5 nH
Positive Bus-bar Resistance	R_{bp}	1 mΩ
Negative Bus-bar Inductance	L_{bn}	5 nH
Negative Bus-bar Resistance	R_{bn}	1 mΩ
IGBT Module Positive Stray Inductance	L_{mp}	50nH
IGBT Module Negative Stray Inductance	L_{mn}	50nH
Snubber Capacitance	C_r	150 nF
Snubber Capacitor ESR	R_{C_r}	22.5 mΩ

Table 2.9: Parasitic component values.

Figure 2.18 shows the effect of L_s on the main IGBT turn-off losses for different values of the output current I_o. The main module turn-off loss appears to increase linearly with increased parasitic inductance L_s. Table 2.10 shows the effect of the module stray inductance on the main IGBT turn-off loss for different values of the output current. For this calculation L_s was taken as zero. The module stray inductance alone accounts for an increase of approximately 30% in the main IGBT turn-off loss.

I_o A	Idealized turn-off loss (mJ per cycle)	Turn-off loss with parasitic components (mJ per cycle)
40	0.16	0.21
80	0.66	0.83
120	1.48	1.88
160	2.63	3.34
200	4.11	5.21

Table 2.10: Effect of module stray inductance on the main IGBT turn-off losses.

Figure 2.19 shows the effect of L_s on the voltage overshoot v_{os} (see equation 2.66) of the voltage across C_{rp} during main module turn-off for different values of the output current I_o.

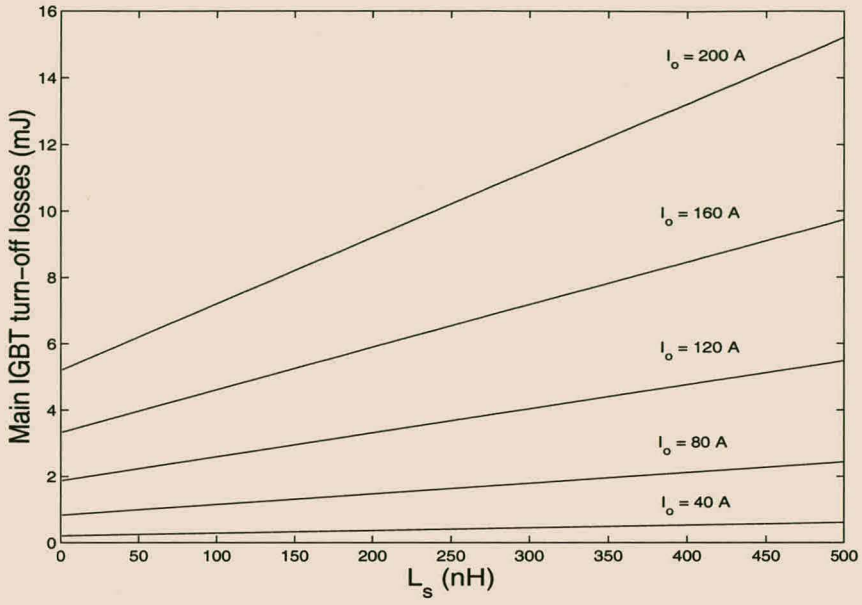


Figure 2.18: Main IGBT turn-off loss taking the effect of the parasitic components into account.

2.2.6.2 Capacitor discharge cycle

In this section the effect of the parasitic components on the capacitor discharge cycle is evaluated. Figure 2.20 shows the snubber circuit during the capacitor discharge cycle of the main top IGBT. The equivalent circuit used in the analysis of the circuit is also shown. The main aim of this analysis is to determine the effect of the losses in the circuit on the final capacitor voltage at the end of the resonant discharge cycle. Voltage source v_{ce} represents the voltage across the IGBT during switching. Resistors R_{L_r} and R_{C_r} represent the equivalent series resistance of inductor L_{rp} and capacitor C_{rp}, respectively. To simplify the analysis the series resistance of the auxiliary switch and diode are included in R_{L_r}.

The following assumptions are made in this section:

1. The positive and negative DC-bus voltages do not drift and are fixed at $V_d/2$ and $-V_d/2$, respectively. A simple adjustment of the value of $\frac{V_d}{2}$ can be made if it is necessary to model the imbalance in the DC-bus voltages.

2. Diode forward recovery is not considered.

3. During turn-on the voltage across the IGBT declines to zero in two time-linear segments as shown in Figure 2.13. These two segments are described by

$$v_{ce}(t) = \begin{cases} V_0\left(1 + (B-1)\frac{t}{t_{fv}}\right) & \text{if } 0 \leq t \leq t_{fv} \\ V_0 B\left(1 - \frac{t-t_{fv}}{t_{tv}}\right) & \text{if } t_{fv} \leq t \leq t_{fv} + t_{tv}, \end{cases} \tag{2.67}$$

where V_0 is the voltage across the IGBT at the start of the capacitor discharge cycle. Hence $V_0 = v_{os} + \frac{V_d}{2}$, where v_{os} was defined in the previous section.

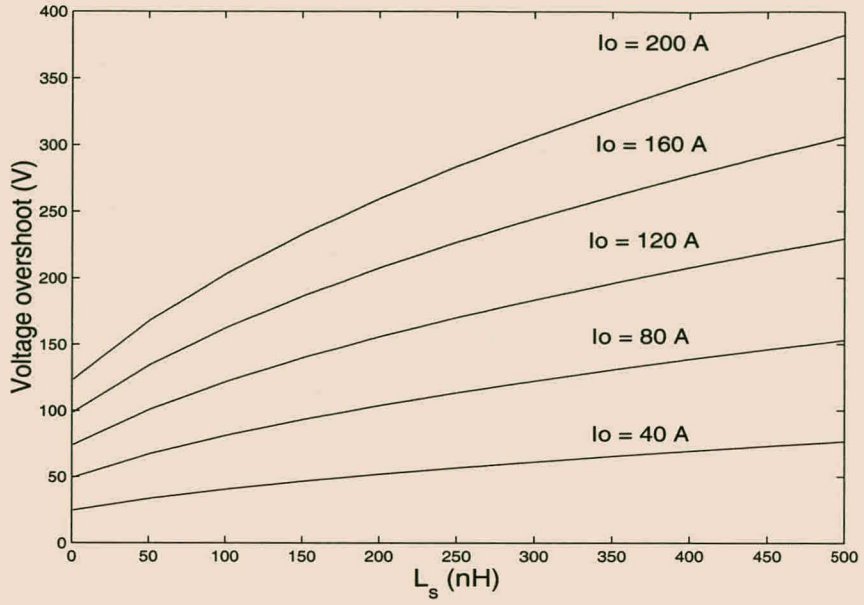


Figure 2.19: Turn-off voltage overshoot (v_{os}) as a result of the parasitic inductances.

4. The total duration of the capacitor discharge cycle is greater than the auxiliary switch turn-on time $t_{fv} + t_{tv}$.

5. The on-state voltages of the auxiliary IGBT and diodes are small compared to the DC-bus voltage and are not considered.

The next step in the analysis is to solve the differential equations for $i_{L_{rp}}$ and $v_{C_{rp}}$ during the discharge cycle. The discharge cycle can be divided into three distinct sub-cycles:

1. If $0 \leq t \leq t_{fv}$,

$$\begin{bmatrix} v_{C_{rp}} \\ i_{L_{rp}} \end{bmatrix} = A(t) \begin{bmatrix} k \\ \overline{k} \end{bmatrix} + \begin{bmatrix} \frac{V_d}{2} + v_{os} - R_{bp}I_o + V_0 \left(1 + (B-1)\left(\frac{t-(R_{bp}+R_{L_r}+R_{C_r})C_r}{t_{fv}}\right)\right) \\ -C_r V_0 \frac{B-1}{t_{fv}} \end{bmatrix}, \tag{2.68}$$

where

$$A(t) = \begin{bmatrix} e^{(\alpha+j\beta)t} & e^{(\alpha-j\beta)t} \\ -C_r(\alpha+j\beta)e^{(\alpha+j\beta)t} & -C_r(\alpha-j\beta)e^{(\alpha-j\beta)t} \end{bmatrix}, \tag{2.69}$$

$$\alpha = -\frac{R_{bp} + R_{L_r} + R_{C_r}}{2(L_{bp} + L_r)}, \tag{2.70}$$

and

$$\beta = \sqrt{\frac{1}{(L_{bp} + L_r)C_r} - \left(\frac{R_{bp} + R_{L_r} + R_{C_r}}{2(L_{bp} + C_r)}\right)^2}. \tag{2.71}$$

Furthermore,

$$\begin{bmatrix} k \\ \overline{k} \end{bmatrix} = A^{-1}(0) \begin{bmatrix} v_{os} + \frac{V_d}{2} + R_{bp}I_o - V_0 \left(1 + (B-1)\left(\frac{(R_{bp}+R_{L_r}+R_{C_r})C_{rp}}{t_{fv}}\right)\right) \\ C_r V_0 \frac{B-1}{t_{fv}} \end{bmatrix}. \tag{2.72}$$

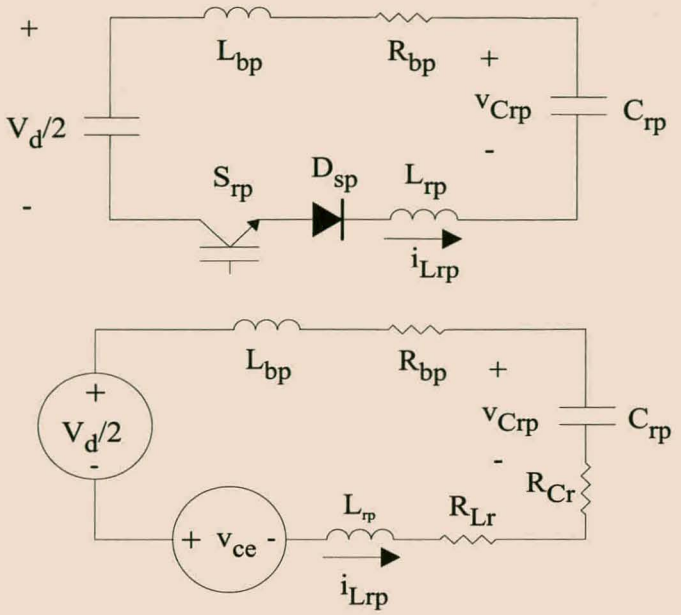


Figure 2.20: Parasitic components that influence the capacitor discharge cycle. Top: Actual circuit. Bottom: Equivalent circuit.

2. For $t_{fv} \leq t \leq t_{fv} + t_{tv}$,

$$\begin{bmatrix} v_{C_{rp}} \\ i_{L_{rp}} \end{bmatrix} = A(t) \begin{bmatrix} l \\ \bar{l} \end{bmatrix} + \begin{bmatrix} \frac{V_d}{2} - R_{bp}I_o + V_0 B \left(1 - \frac{t - t_{fv} + (R_{bp} + R_{Lr} + R_{Cr})C_r}{t_{tv}}\right) \\ C_r V_0 \frac{B}{t_{tv}} \end{bmatrix} \tag{2.73}$$

where

$$\begin{bmatrix} l \\ \bar{l} \end{bmatrix} = A^{-1}(t_{fv}) \begin{bmatrix} v_{C_{rp}}(t_{fv}) - \frac{V_d}{2} + R_{bp}I_o - V_o B \left(1 + \frac{(R_{bp} + R_{Lr} + R_{Cr})C_r}{t_{tv}}\right) \\ i_{L_{rp}}(t_{fv}) - C_r V_0 \frac{B}{t_{tv}} \end{bmatrix}. \tag{2.74}$$

Voltage $v_{C_{rp}}(t_{fv})$ and current $i_{L_{rp}}(t_{fv})$ are again the values of $v_{C_{rp}}$ and $i_{L_{rp}}$ at time t_{fv}, respectively.

3. Finally, for $t \geq t_{fv} + t_{tv}$

$$\begin{bmatrix} v_{C_{rp}} \\ i_{L_{rp}} \end{bmatrix} = A(t) \begin{bmatrix} m \\ \overline{m} \end{bmatrix} + \begin{bmatrix} \frac{V_d}{2} - R_{bp}I_o \\ 0 \end{bmatrix} \tag{2.75}$$

where

$$\begin{bmatrix} m \\ \overline{m} \end{bmatrix} = A^{-1}(t_{fv} + t_{tv}) \begin{bmatrix} v_{C_{rp}}(t_{fv} + t_{tv}) - \frac{V_d}{2} + R_{bp}I_o \\ i_{L_{rp}}(t_{fv} + t_{tv}) \end{bmatrix}. \tag{2.76}$$

Voltage $v_{C_{rp}}(t_{fv} + t_{tv})$ and current $i_{L_{rp}}(t_{fv} + t_{tv})$ are the values of $v_{C_{rp}}$ and $i_{L_{rp}}$, respectively at time $t_{fv} + t_{tv}$.

Figure 2.21 shows the effect of the parasitic components on the capacitor discharge cycle. The idealized waveforms based on equations 2.9 and 2.10 are also shown.

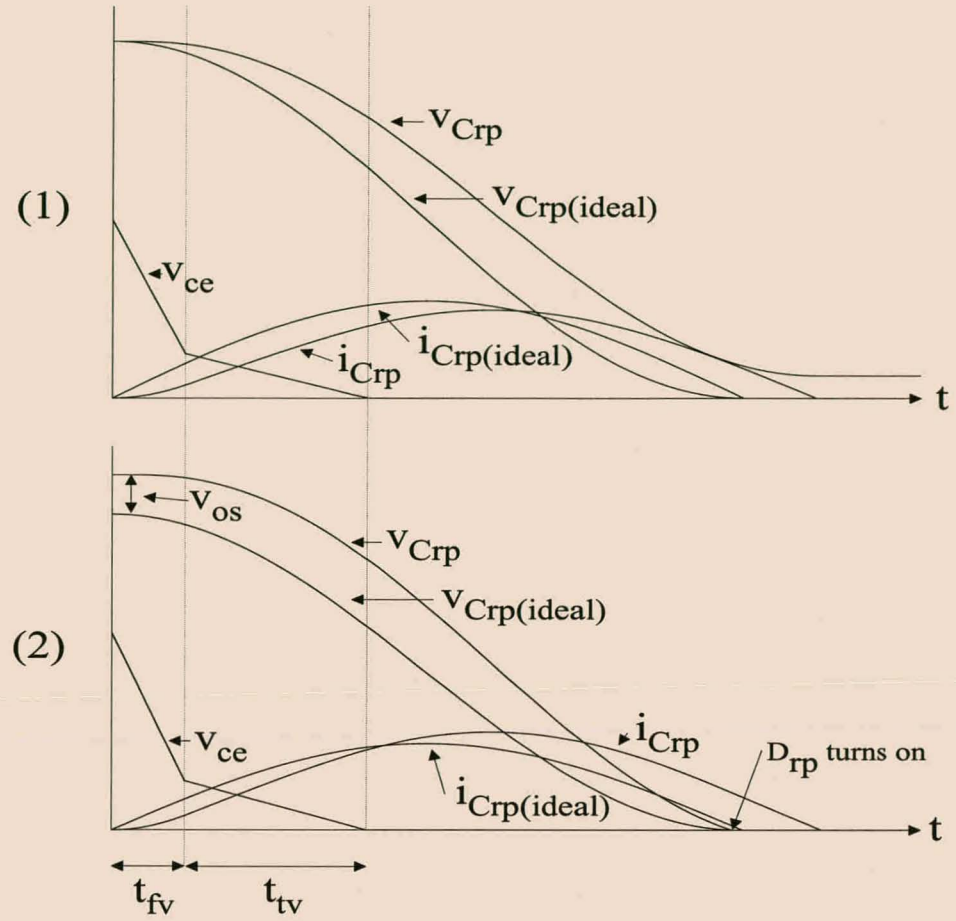


Figure 2.21: Effect of the parasitic components on the capacitor discharge cycle waveforms. Top: Without the effect of v_{os}. Bottom: With the effect of v_{os}.

The parasitic components and switch losses give rise to an increase in the duration of the resonant cycle. The most significant effect is that the snubber capacitor C_{rp} is not fully discharged if the voltage $v_{C_{rp}}$ across the resonant capacitor is equal to $\frac{V_d}{2}$ at the start of the discharge cycle. This phenomenon can, however, be negated by the voltage overshoot v_{os} across C_{rp} during the main IGBT turn-off cycle.

The next step in the analysis is to study the behavior of the circuit towards the end of the resonant half cycle. Depending on the value of $v_{C_{rp}}$ at the start of the capacitor discharge cycle, two different cases may arise (see Figure 2.21):

1. If v_{os} during the previous turn-off cycle is small, $v_{C_{rp}}$ does not reach zero before D_{sp} turns off. This will result in increased turn-off loss in the top main IGBT during the next turn-off cycle, as the voltage across the main IGBT will not be zero at turn-off.

2. For relatively large values of v_{os}, voltage $v_{C_{rp}}$ reaches zero before $i_{L_{rp}}$ reaches zero. In this case diode D_{rp} becomes forward biased, clamping the voltage across C_{rp} at zero. The excess energy stored in inductor L_{rp} is returned to the DC-bus. During this period the

current through L_{rp} is given by

$$i_{L_{rp}} = ne^{-\frac{t}{\tau}} + \frac{R_{bp}I_o - \frac{V_d}{2}}{R_{bp} + R_{L_r}}, \tag{2.77}$$

where

$$n = \frac{i_{L_{rp(don)}} - \frac{R_{bp}I_o - \frac{V_d}{2}}{R_{bp}+R_{L_r}}}{e^{\frac{t_{don}}{\tau}}} \tag{2.78}$$

and $i_{L_{rp(don)}}$ is the current through L_{rp} when D_{rp} turns on. Furthermore, time constant τ is given by

$$\tau = \frac{L_{bp} + L_r}{R_{bp} + R_{L_r}}. \tag{2.79}$$

Note that the snubber parasitic inductance L_s was not taken into account in this analysis. The effect of this inductance is visible in practical results but has very little influence on the operation of the snubber.

Example 2.4

In this example the effects of the parasitic components on the capacitor discharge cycle of the example of the previous section are investigated. Table 2.11 gives the additional snubber parameters used in this example. By making use of the equations above it was found that a minimum value of 40 V for v_{os} is required for the snubber capacitor to discharge fully. Taking $L_s = 100$ nH in Figure 2.19, full discharge of the snubber capacitor will be achieved for $I_o \geq 40$ A.

Parameter	Symbol	Value
Auxiliary Resonant Inductor	L_r	10.5 μH
Resonant Inductor ESR	R_{L_r}	250 mΩ
Voltage Overshoot at Turn-off	v_{os}	40 V

Table 2.11: Additional parasitic component values.

Figure 2.22 shows $v_{C_{rp}}$, v_{ce} and $i_{L_{rp}}$ for $v_{os} = 40$ V. The total capacitor discharge time is 4.2 μs which is well within the initial limits.

Figure 2.23 shows $v_{C_{rp}}$, v_{ce} and $i_{L_{rp}}$ for $v_{os} = 380$ V, which is the maximum overshoot of Figure 2.19. The capacitor discharge time is lengthened to 4.7 μs, while the peak current through L_{rp} increases from 75 A to 90 A. This shows that even a substantial increase in v_{os} does not increase the total capacitor discharge time or the peak rating of the auxiliary switch significantly. In fact, the original requirement of a maximum duty cycle of 85% can be increased to a maximum duty cycle of 90%.

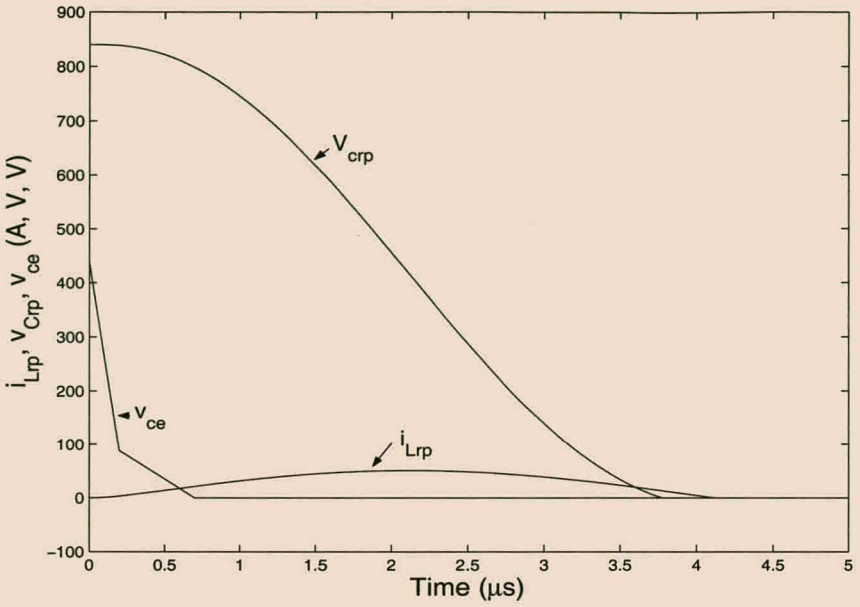


Figure 2.22: Example of the capacitor discharge cycle taking the effect of the parasitic components into account ($v_{os} = 40$ V).

2.2.7 Design of an experimental turn-off snubber

In this section the design of a 40 kVA single-phase converter, fitted with the resonant turn-off snubber, is described. The single-phase converter is based on the 200 A, 1200 V PM200DSA120 integrated power module from Powerex which has been used in the examples of this chapter. This module has a built in gate drive circuit with over-current and over-temperature protection. According to the data sheet the total module stray inductance is approximately 50 nH.

Recall that each phase arm of the 700 kVA three level series-stacked converter is a 120 kVA half-bridge converter. The experimental snubber is thus constructed at one third of the power level required in the final 2 MVA converter.

Altogether three different versions of the resonant turn-off snubber were constructed. Only the design and experimental results of the final version will be described here. Some of the experimental results taken on the second version of the snubber can be found in [88]. [The help of Mr. F.W. Combrink with the construction of the final snubber and experimental measurements is gratefully acknowledged. Mr. Combrink is currently pursuing a Masters degree on soft-switching topologies under the guidance of the author and the supervisor of this thesis.]

The design optimization of the resonant snubber was carried out in two steps:

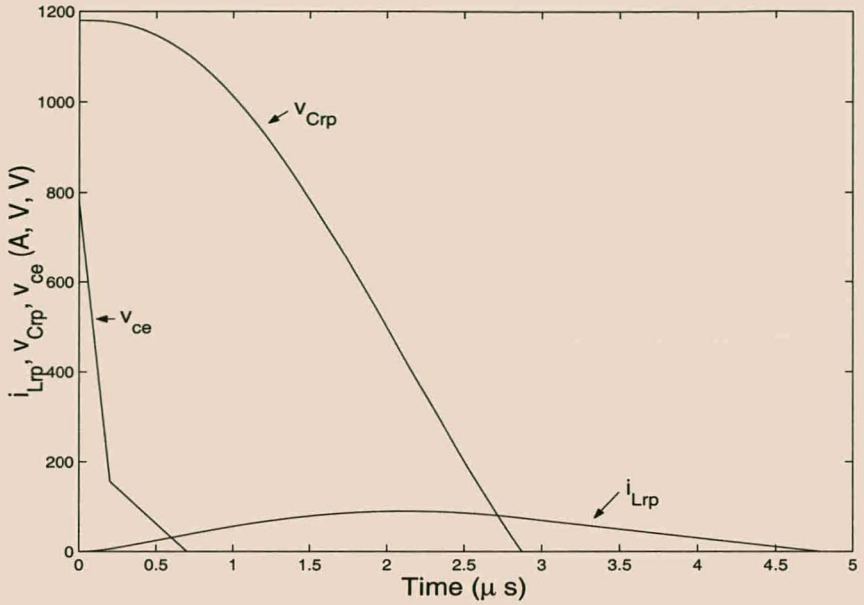


Figure 2.23: Example of the capacitor discharge cycle taking the effect of the parasitic components into account.

1. An initial selection of snubber components was made. An experimental version of the snubber was constructed based on the values of $L_r = 4.4$ μH and $C_r = 154$ nF of the optimal design example on p. 38. In the practical circuit C_r was chosen as 165 nF (5×33 nF). The main aim was to measure the turn-on behavior of the auxiliary IGBT under soft switching conditions. For the final snubber design an estimate of the resonant frequency $\omega_r = \frac{1}{\sqrt{C_r L_r}}$ had to be made. Based on the examples of this chapter this was estimated to lie between 100 and 200 kHz with an average value of 150 kHz.

2. After measuring the turn-on behavior of the auxiliary IGBT and improving the estimates of the resonant inductor loss, the optimal design procedure was again carried out. This resulted in a small modification to the size of the resonant inductor. The gain in efficiency by carrying out the second iteration was, however, limited.

The parameters of the inverter and snubber are listed in Table 2.12. The following paragraphs describe the different snubber components.

2.2.7.1 Snubber capacitors

Multi-layer ceramic capacitors and plastic film capacitors were considered as snubber capacitors. Ceramic capacitors have extremely low series inductance, but are not cost-effective at high voltage ratings. Plastic film capacitors are inexpensive and are supplied by a number of manufacturers. The most common plastic films used as dielectrics are polyester, polycarbonate and polypropylene. After comparing a number of commercially available capacitors, the R73

System Parameters		
Nominal DC-bus Voltage	V_d	800 V
Peak Output Current	$I_{o(peak)}$	200 A
Switching Frequency	f_s	10 kHz
Blanking Time	t_b	5 μs
Maximum Duty Cycle	d_{max}	0.85
DC-bus Capacitors	C_d	4 800 μF
Main IGBT Module (Powerex PM200DSA120)		
Current Fall Time	t_{fi}	250 ns
Current Tail Time	t_{ti}	500 ns
Tail Current Ratio	A	0.2
Total Module Stray Inductance	L_{stray}	50 nH
Snubber Diode (SEMIKRON SKR48F12)		
On-state Resistance	R_{D_r}	22 mΩ
On-state Voltage	V_{D_r}	1.2 V
Peak Voltage Rating	V_{rrm}	1200 V
Reverse Recovery Time	t_{rr}	80 ns
Peak Current Rating	I_{fsm}	500 A
Snubber Capacitor (Film-foil Polypropylene)		
Capacitance	C_r	5 $\times$ 33 nF
ESR Coefficient	k_{R_C}	$3.4 \times 10^{-12} \Omega F$
Auxiliary IGBT (Fuji 1MBH60D-090A)		
Voltage Fall Time	t_{fv}	17 ns
Voltage Tail Time	t_{tv}	40 ns
Tail Voltage Ratio	B	0.06
On-state Resistance	R_{sa}	0.017 Ω
On-state Voltage	V_{sa}	1.5 V
Peak Current Rating	$I_{r(max)}$	60 A
Peak Voltage Rating	$v_{ce_{max}}$	900 V
Auxiliary Diode (IXYS DSEI60)		
On-state Voltage	V_{da}	2 V
On-state Resistance	R_{da}	8.3 mΩ
Reverse Recovery Time	t_{rr}	40 ns
Peak Voltage Rating	V_{rrm}	1200 V
Peak Current Rating	I_{fsm}	540 A
Continuous Current Rating	I_{favm}	52 A
Resonant Inductor (Philips P30/19 3F3 Core)		
Inductance	L_r	12 μH
Core Loss Per Cycle	W_{core}	86.7 μJ
Copper Resistance	R_{cu}	21.8 mΩ

Table 2.12: Experimental turn-off snubber parameters.

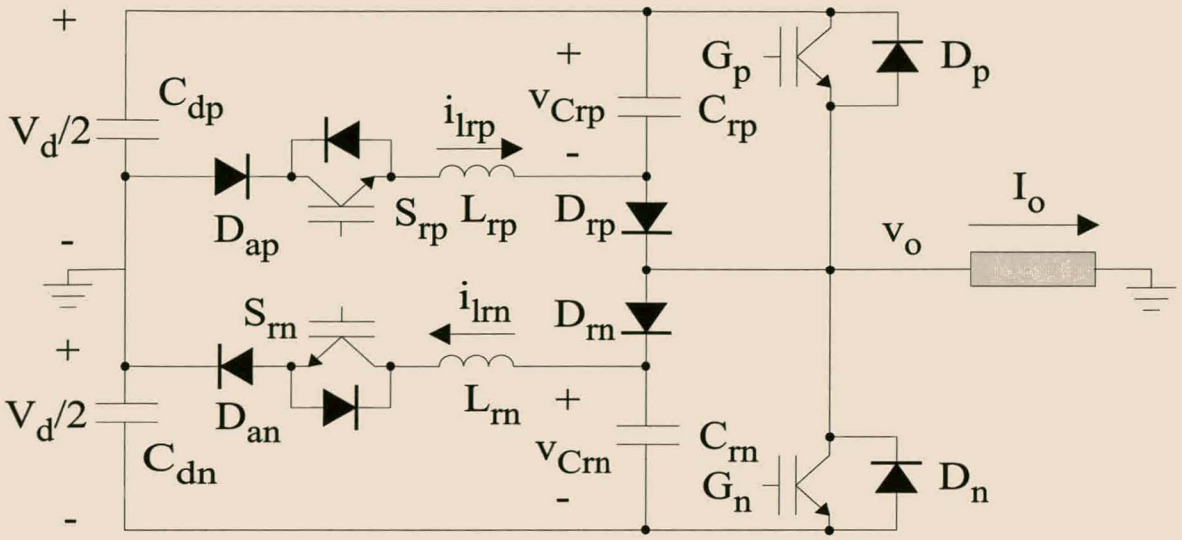


Figure 2.24: Experimental turn-off snubber.

KP range film-foil polypropylene capacitors from Arcotronics were selected due to their ability to handle high peak currents and their low cost. The 33 nF, 1000 V capacitor from this range was selected. By stacking a number of 33 nF capacitors in parallel a variety of different snubber capacitor values can be obtained. Each 33 nF capacitor has a peak $\frac{dv}{dt}$ rating of 11 000 V/μs. This implies that each capacitor can handle a peak current of 363 A, which is well above the peak converter output current of 200 A. According to the data sheet the equivalent self-inductance of each capacitor is approximately 18 nH. Based on the dissipation factor given in the data sheet ($\tan(\delta) \approx 50 \cdot 10^{-4}$), each capacitor has an approximate equivalent series resistance of $R_{C_r} = 104\ \mu\Omega$ at 100 kHz. Hence

$$k_{R_C} = R_{C_r} C_r = 3.4 \times 10^{-12}\ \Omega\text{F}. \tag{2.80}$$

2.2.7.2 Snubber diodes

The SKR48F12 fast recovery diode from SEMIKRON was chosen as snubber diode. Previous experience showed that this range of diodes has superior forward and soft reverse recovery properties. This diode has a voltage rating of 1200 V, a peak current rating of 500 A and a reverse recovery time of 80 ns. The on-state voltage and resistance that is shown in Table 2.12 are taken from the data sheet. No data on the diode stray inductance were available from the manufacturer.

2.2.7.3 Auxiliary switches

The 1MBH60D-090A IGBT from Fuji was chosen as the auxiliary switch. This relatively inexpensive IGBT (3% of the cost of the main IGBT) has a voltage rating of 900 V with

a continuous current rating of 60 A and a peak current rating of 120 A. This IGBT also contains an anti-parallel diode with a continuous current rating of 15 A. The on-state voltage and resistance of this auxiliary IGBT, which are presented in Table 2.12, are based on data sheet values. The turn-on behavior of the auxiliary IGBT was measured after the first iteration snubber was constructed.

A diode was connected in series with the auxiliary IGBT to obtain a reverse blocking capability. The DSEI60 diode from IXYS was chosen for this purpose. It has a voltage rating of 1200 V with an average current rating of 52 A and a peak current rating of 540 A. The on-state voltage and resistance are taken from the data sheet.

2.2.7.4 Resonant inductor

In the initial version of the turn-off snubber air-core resonant inductors were used. One of the problems with air-core inductors is the spreading of magnetic fields, which may result in interference with the control and other circuitry. To reduce this spreading of magnetic fields as well as the physical size of the inductors, it was decided to use ferrite core inductors in the final prototype. A Philips P30/19 3F3 P-core was selected due to the high performance-factor of the 3F3 magnetic material in the frequency range 100 kHz to 400 kHz (see [103], p. 39).

The losses in the inductor are due to core losses (mainly hysteresis loss) and conduction loss in the copper windings. A peak core flux density B_{max} of 300 mT was selected to prevent the core from saturating. To determine the hysteresis loss the core loss curves on p. 98 of [103] were used. These curves do not extend to 300 mT. Linearly extending the 100 kHz and 200 kHz curves to 300 mT yielded a value of $P_v = 1.2 \times 10^3$ kW/m^3 at 100 kHz and $P_v = 3 \times 10^3$ kW/m^3 at 200 kHz. Using an average value of $P_v = 2.1 \times 10^3$ kW/m^3 for 150 kHz and the fact that the core volume V_{core} is equal to 6190×10^{-9} m^3 results in core loss of

$$P_{core} = P_v V_{core} = 13.0 \text{ W} \tag{2.81}$$

for continuous operation at 150 kHz. Hence, the energy loss per cycle is given by

$$W_{core} = \frac{P_{core}}{150 \times 10^3} = 86.7 \ \mu\text{J}. \tag{2.82}$$

The next step is to calculate the conduction loss. The effective core cross-sectional area A_e is equal to 137 mm^2. Hence the peak magnetic flux $\hat{\phi}$ is given by

$$\hat{\phi} = A_e B_{max} = 41.1 \ \mu\text{Weber}. \tag{2.83}$$

The inductance L_r is given by

$$L_r = N \frac{\hat{\phi}}{I_{L_r(max)}}, \tag{2.84}$$

where N is the number of turns and $I_{Lr(max)}$ is the peak inductor current. This implies that

$$N = \frac{L_r I_{Lr(max)}}{\hat{\phi}}. \tag{2.85}$$

The core window area A_w (taking the bobbin into account) is 25 mm^2. Using a fill-factor of 0.35 (due to isolation requirements) gives an effective window area A_{we} of 8.75 mm^2. Hence the conductor cross-sectional area (per turn) is given by

$$A_{cond} = \frac{A_{we}}{N}. \tag{2.86}$$

The total length l_{cond} of the conductor is given by

$$l_{cond} = N\pi d_{turn}, \tag{2.87}$$

where d_{turn} is the average turn diameter. Based on the average bobbin diameter d_{turn} is equal to 18 mm.

The skin depth in copper at 150 kHz is given by (see [12], p. 151)

$$\delta = \frac{1}{\sqrt{\pi f \sigma \mu}} = 0.17 \text{ mm}, \tag{2.88}$$

where $\mu = 4\pi \times 10^{-7}$ H/m and $\sigma = 5.8 \times 10^7$ S/m. Based on this value of the skin depth, it was decided to wind the inductor using Litz wire. Each strand of the Litz wire was chosen to have a diameter of 0.17 mm. Working with thinner strands of wire proved to be impractical. Since the radius of the wire is equal to half the skin depth, the skin effect was not taken into account when calculating resistance R_{Lr}. The proximity effect was also not taken into account. Based on these simplifications, the winding resistance is given by

$$R_{cu} = \frac{l_{cond}}{\sigma A_{cond}}. \tag{2.89}$$

By making use of this more detailed analysis of the loss in the auxiliary inductors, the following modifications were made to the optimal design procedure of section 2.2.5:

1. For each value of L_r and C_r, the value of $I_{Lr(max)}$ was calculated by making use of equation 2.11. Resistance R_{cu} was then calculated by using the equations above. This value of R_{cu} was used to calculate the conduction loss in the resonant inductor from equation 2.40.

2. It is important to recall that for a particular choice of L_r and C_r the value of $I_{Lr(max)}$ depends only on the DC-bus voltage, which is fixed. As mentioned earlier the inductor will be designed in such a way that the peak flux density is equal to 300 mT. This means that the inductor core loss is fixed at 86.7 μJ per cycle. Hence, for each time that the auxiliary discharge circuit is triggered, 86.7 μJ is added to the total inductor loss.

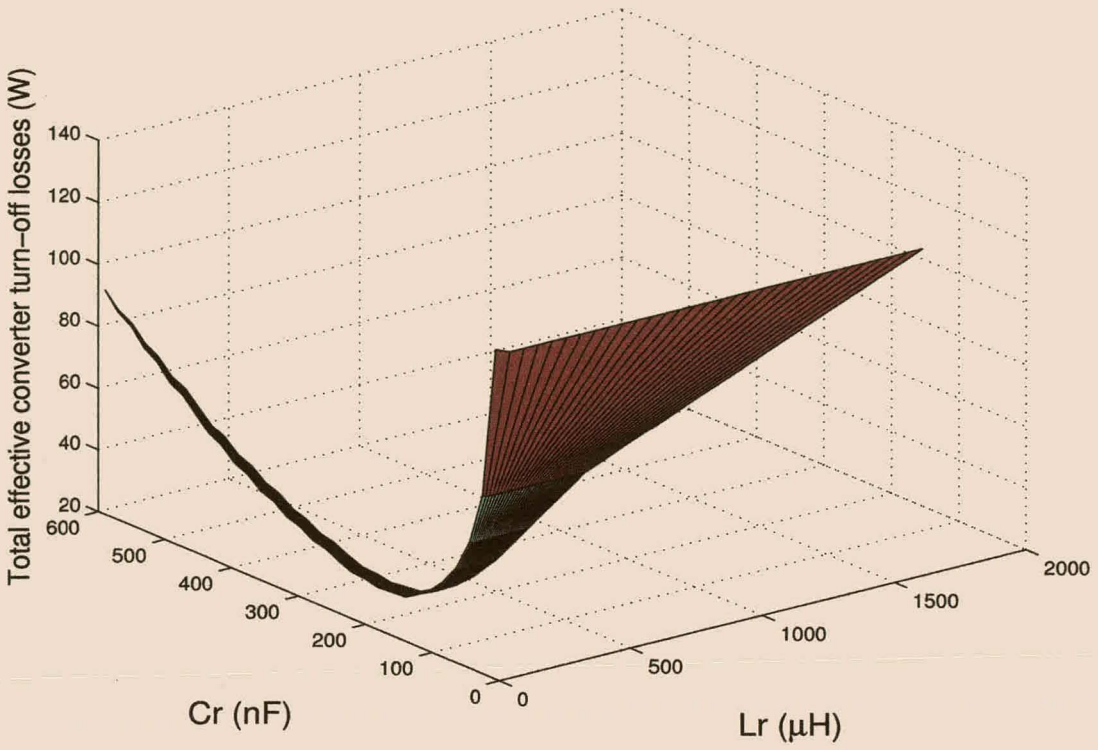


Figure 2.25: Total effective turn-off loss as a function of L_r and C_r.

After implementing this modification the optimal snubber design process was carried out for a 50 Hz sinusoidal output current with a peak value of 200 A. Figure 2.25 shows the result. The optimal values are $C_r = 183$ nF and $L_r = 14$ μH. The total effective converter turn-off loss is 33.1 W. Table 2.13 summarizes the losses in the main IGBTs and the snubber components. It was decided to use $L_r = 12$ μH and $C_r = 165$ nF in the practical circuit. The capacitor size has to be a multiple of 33 nF, while the inductor size was decreased to ensure that the snubber discharges fully during the minimum available discharge time. Recall that the losses and parasitic components increase the capacitor discharge time.

Main IGBT Turn-off Loss	P_{off}	21.4 W
Snubber Diode Loss	P_{D_r}	4.8 W
Snubber Capacitor Loss	P_{C_r}	0.003 W
Resonant Inductor Loss	P_{L_r}	1.8 W
Auxiliary Switch Switching Loss	$P_{sa(switch)}$	3.8×10^{-6} W
Auxiliary Switch Conduction Loss	$P_{sa(cond)}$	2.6 W
Auxiliary Diode Conduction Loss	$P_{da(cond)}$	2.8 W
Auxiliary Diode Reverse Recovery Loss	P_{rr}	0.024 W

Table 2.13: Theoretical losses in the converter and snubber circuit averaged over one 50 Hz cycle.

Knowing the value of the resonant inductor, its design can be finalized. By making use of equation 2.11 the peak inductor current is equal to

$$i_{L_{r(max)}} = \frac{V_d}{2}\sqrt{\frac{C_r}{L_r}} = 46.9 \text{ A}. \tag{2.90}$$

From equation 2.85 the number of turns is $N = 14$. To prevent core saturation an air gap is added. In the design of the air gap the fringing effect of the magnetic field is ignored. After construction small adjustments can be made to the length of the air gap to obtain the correct inductance value. By Ampere's law

$$Ni_{L_{r(max)}} = \oint (\hat{H}_{gap} + \hat{H}_{core})\, dl, \tag{2.91}$$

where $\hat{H}_{gap}$ is the peak magnetic field intensity in the air gap and $\hat{H}_{core}$ is the peak magnetic field intensity in the core. Since the permeability of the core is much greater than that of air ($\mu_r \approx 4000$ at 25°C [103], p. 118), the magnetic field is significantly smaller in the core and the contribution of $\hat{H}_{core}$ can be neglected. This implies that

$$Ni_{L_{r(max)}} = 2g\hat{H}_{gap}, \tag{2.92}$$

where g is the gap length. By making use of the fact that $B_{gap} = \mu_0 H_{gap}$ and the continuity of the magnetic flux density, it follows that

$$g = \frac{Ni_{L_{r(max)}}}{2\hat{H}_{gap}} = \frac{\mu_0 Ni_{L_{r(max)}}}{2B_{max}} = 1.38 \text{ mm}. \tag{2.93}$$

From equation 2.86 the conductor area A_{cond} is equal to 0.625 mm^2, which means that 27 strands of 0.17 mm diameter copper wire must be used to wind the inductor. The conductor length l_{cond} is 792 mm. Isolating tape (glass tape) was wound around the conductor to provide the isolation required. Finally, the copper resistance R_{cu} can be calculated by making use of equation 2.89, which yields a value of 21.8 mΩ. Practical measurements of the resonant frequency between the snubber capacitors and the resonant inductor yielded a value of 12.5 μH.

The snubber components were combined into a module, which also included the control circuit of Figure 2.5. This module consists of two printed circuit boards with one fitting on top of the other. A LEM module is used to measure output current that is fed back to the snubber controller. Figure 2.26 shows the printed circuit board containing the snubber control circuit as well as the auxiliary switches and diodes. The auxiliary switches are mounted at the back of the small heatsinks containing the auxiliary diodes. This module also contains the isolated power supply and gate-drive circuits for the auxiliary IGBTs. Both the main IGBTs as well as the snubber receive their control signals through optic fibers.

Figure 2.27 shows the printed circuit board containing the snubber diodes, snubber capacitors and resonant inductors. Small heatsinks were fitted to the snubber diodes. This module screws onto the main IGBT nodule, with the circuit of Figure 2.26 fitting on top of it.

A TMS 320C50 DSP was used to generate the PWM gating signals for the converter.

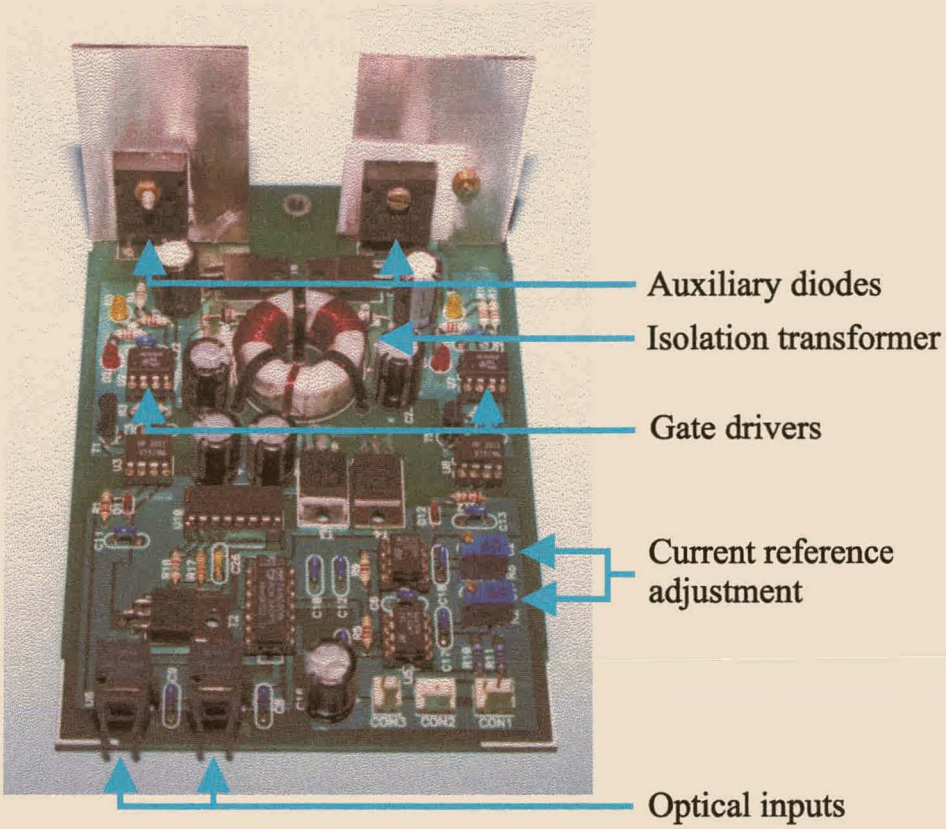


Figure 2.26: Snubber control circuit and auxiliary switches.

2.2.8 Experimental results

Experimental measurements on the practical system were made with a DC-bus voltage of 600 V. This value of V_d was chosen for comparison with the data sheet values of switching loss which are given for a 600 V DC-bus. In the first part of the experimental results a square wave output voltage waveform is used. In the second part efficiency measurements using a sine wave reference signal are made.

2.2.8.1 Square wave modulation

For the measurements of this section a square wave output voltage was used with an inductive load. Under these conditions each IGBT takes over load current from its free-wheeling diode, which results in the main IGBTs turning on at zero voltage. For this reason the turn-on loss can be ignored. This makes it easier to measure the effect of the snubber on the turn-off loss without having to take the turn-on loss into account.

2.2.8.1.1 Main IGBT turn-off cycle

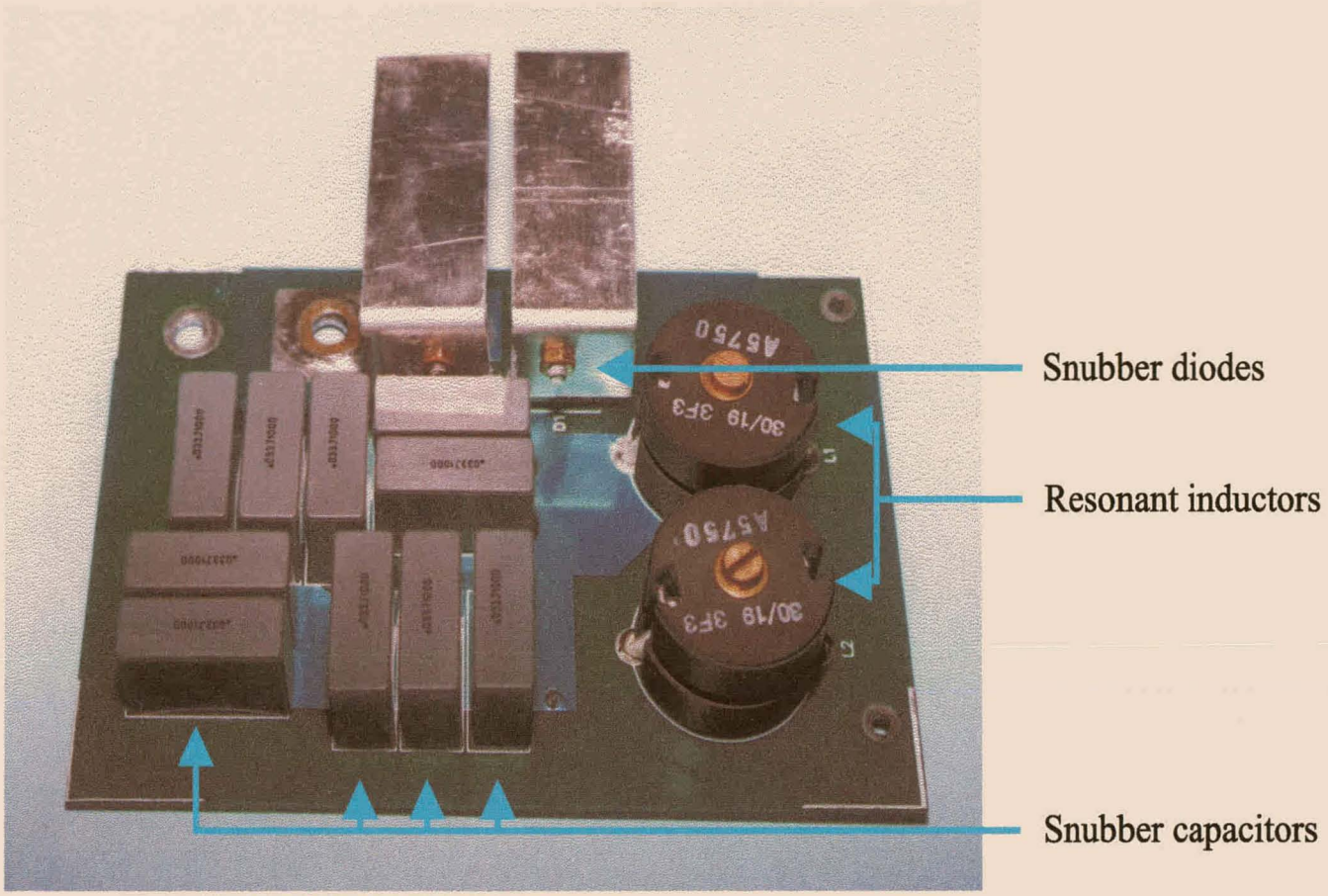


Figure 2.27: Experimental snubber circuit.

Figure 2.28 shows the main top IGBT turn-off voltage (v_{ce1}) for output currents between 25 A and 200 A. Recall that v_{ce1} is the collector emitter voltage plus the voltage over the module parasitic inductance as shown in Figure 2.16. The theoretical waveforms based on the analysis of section 2.2.6.1 are also shown. One of the problems with the analysis is to determine the value of the parasitic inductances. It was found that the parasitic resistances do not play a significant role. The value of R_{C_r} is dominated by the snubber diode on-state resistance, which is equal to 22 mΩ. The bus-bar resistances R_{bp} and R_{bn} were conservatively estimated at 1 mΩ.

In the following discussion it is assumed that the IGBT module and bus-bar are symmetrical in layout with $L_{bp} = L_{bn}$ and $L_{mp} = L_{mn}$. The analysis of section 2.2.6.1 is applied for the case $t \geq t_{vr}$. Taking typical values of $R_{bp} + R_{C_r} + R_{bn} = 23$ mΩ and $L_{bp} + L_s + L_{mn} + L_{bn} = 100$ nH showed that the $R_{bp} + R_{C_r} + R_{bn}$ has very little influence on the value of β in equation 2.62. Furthermore, the time constant $\tau = -\frac{1}{\alpha}$ is in the order of 10 microseconds. Based on these considerations the parasitic resistances are ignored in the following analysis. Taking $\alpha = 0$ and $\beta = \sqrt{\frac{1}{C_r(L_{bp}+L_s+L_{mn}+L_{bn})}}$ equations 2.63 and 2.64 can be rewritten as

$$v_{C_{rp}} = I_o\sqrt{\frac{(L_{bp} + L_s + L_{mn} + L_{bn})}{C_r}} \sin \beta(t - t_{vr}) + V_d \tag{2.94}$$

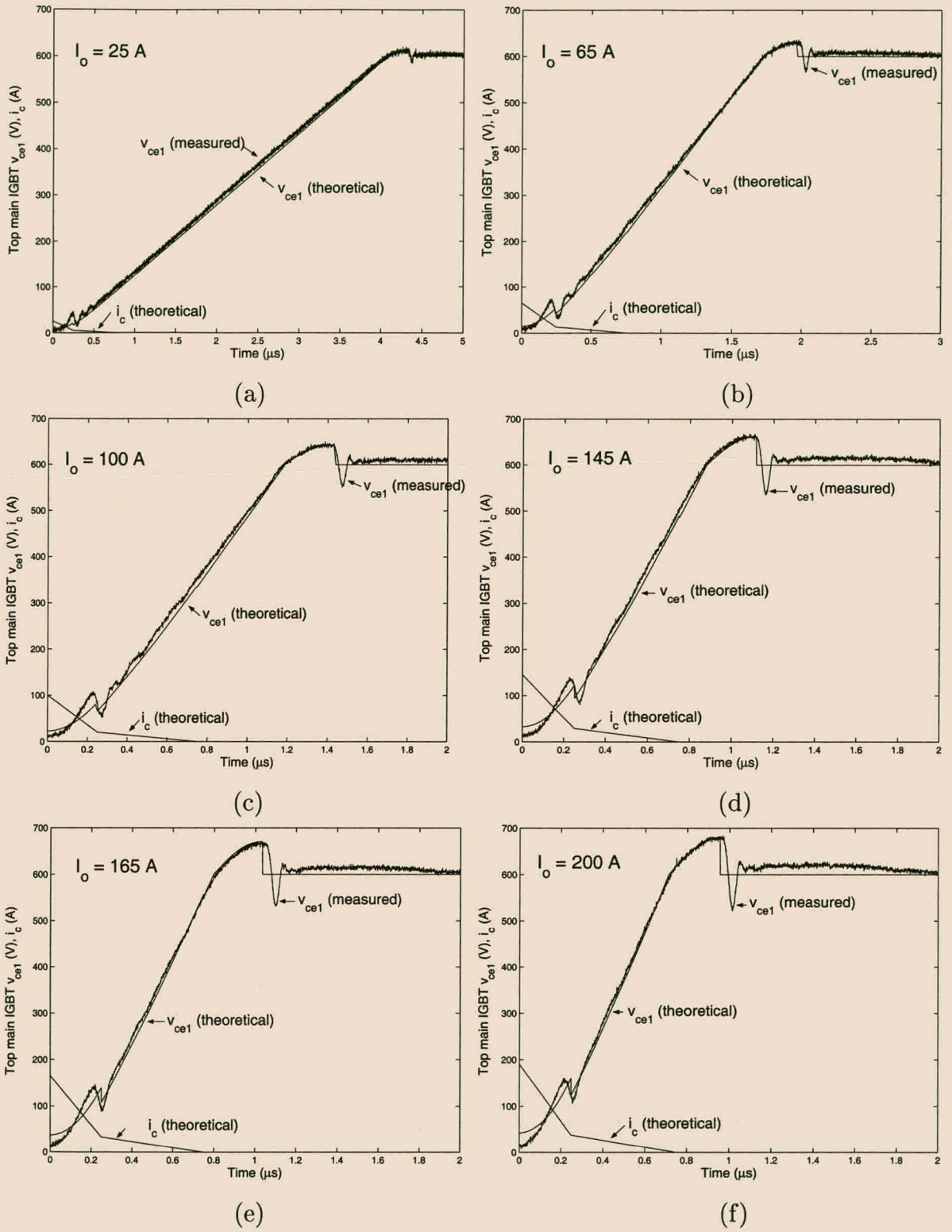


Figure 2.28: Main top IGBT collector-emitter voltage (v_{ce1}) during turn-off. Measured and theoretical results.

and

$$i_{Crp} = I_o \cos \beta(t - t_{vr}). \tag{2.95}$$

Hence, voltage v_{ce1} is given by

$$\begin{aligned} v_{ce1} &= v_{C_{rp}} + L_s \frac{di_{C_{rp}}}{dt} \\ &= I_o \left(\sqrt{\frac{(L_{bp} + L_s + L_{mn} + L_{bn})}{C_r}} - L_s \beta \right) \sin \beta(t - t_{vr}) + V_d. \end{aligned} \tag{2.96}$$

Based on these simplifications, estimates of the parasitic inductances can be obtained:

1. For the time period from t_{vr} (where D_n turns on) to the instant when D_{rp} turns off is a quarter resonant and cycle of resonant frequency β. From Figure 2.28(c), this is equal to 234 ns, from which it follows that $L_{bp} + L_s + L_{mn} + L_{bn} = 135$ nH. From the data sheet $L_{mp} \approx L_{mn} \approx 25$ nH, hence $L_{bp} + L_s + L_{bn} \approx 110$ nH.

2. From equation 2.96 the peak value of v_{ce1} is equal to

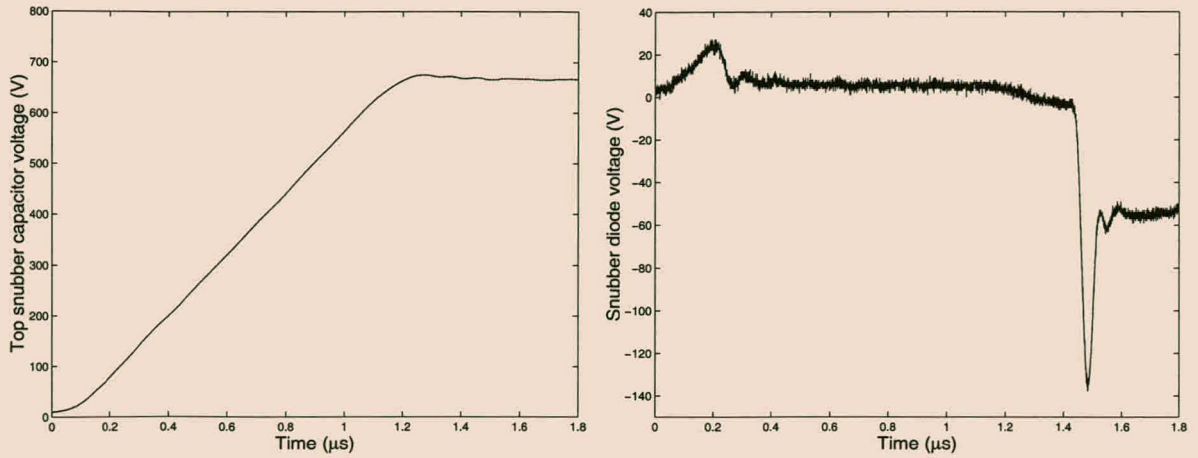
$$I_o \left(\sqrt{\frac{(L_{bp} + L_s + L_{mn} + L_{bn})}{C_r}} - L_s \beta \right) + V_d. \tag{2.97}$$

   Again, from Figure 2.28(c), this is equal to 642.5 V with $I_o = 100$ A. Solving L_s yields a value of $L_s = 72$ nH. Making use of the assumption that $L_{bp} = L_{bn}$ results in a value of $L_{bp} = L_{bn} = 19$ nH.

Parameter	Symbol	Value
Module Positive Stray Inductance	L_{mp}	25 nH
Module Negative Stray Inductance	L_{mn}	25 nH
Positive Bus-bar Inductance	L_{bp}	19 nH
Negative Bus-bar Inductance	L_{bn}	19 nH
Snubber Inductance	L_s	72 nH
Positive Bus-bar Resistance	R_{bp}	1 mΩ
Negative Bus-bar Resistance	R_{bn}	1 mΩ
Snubber Resistance	R_s	22 mΩ

Table 2.14: Values of parasitic components used in the theoretical waveforms of the experimental snubber.

Table 2.14 summarizes the parameters used in the theoretical analysis, the results of which are also shown in Figure 2.28. Although the measured and theoretical results compare well, some attention should be given to the differences between the two.



(a) (b)

Figure 2.29: Main module turn-off with $I_o = 100$ A. (a) Voltage across one of the snubber capacitors. (b) Snubber diode voltage.

The 'dip' in v_{ce1} near 250 ns is a result of the collector current i_c reaching its knee-point. The same dip could also be observed in ARCP converters, especially when the parasitic inductance was increased (see [105], p. 146). That rapid change in $\frac{di_c}{dt}$ is reflected in the voltages across parasitic inductors L_s and L_{mp}. This dip is, however, larger in the measured results than in the theoretical results. This can mainly be attributed to inaccurate modeling of the turn-off current of the main IGBT during the period $0 \leq t \leq t_{fi}$. The main IGBT collector current i_c initially decreases more slowly than predicted and then decreases more rapidly than predicted near t_{fi}. This is at least partly due to the effect of the snubber and module parasitic inductance on the turn-off current waveform of the main IGBT.

Figure 2.29 shows voltage $v_{C_{rp}}$, the measured voltage across one of the snubber capacitors, and the voltage across the snubber diode during main module turn-off. The output current I_o equals 100 A.

The voltage across the snubber diode increases to 25 V during the first part of the main IGBT turn-off cycle and then suddenly decreases to approximately 5 V around 250 ns. According to the theoretical turn-off tail current characteristic of the main IGBT, the jump in $\frac{di_{C_{rp}}}{dt}$ at $t =$ 250 ns is equal to 280×10^6 A/s^2. This would require a diode parasitic inductance of 71 nH (which seems unrealistically high) to achieve the decrease of 20 V at the 250 ns. This seems to imply that diode forward recovery plays some role in this phenomenon. As remarked above, the main IGBT collector current is incorrectly modeled near t_{fi}, which may account for the larger than expected jump in the diode voltage. A more accurate model of the diode turn-on behavior will be required to study this problem in detail.

It should also be noted that an expensive state-of-the-art differential measurement system is

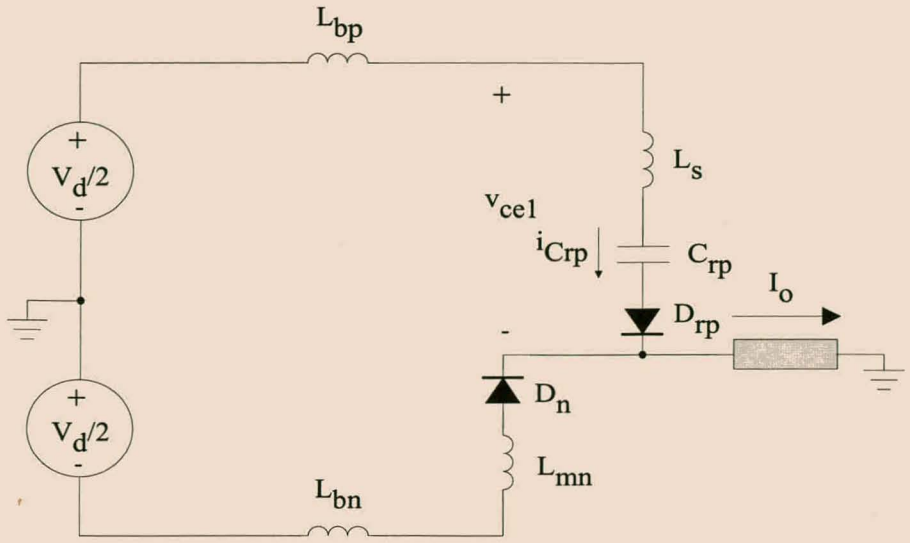


Figure 2.30: Parasitic components involved with the reverse recovery of D_{rp}.

required to obtain accurate high bandwidth measurements of the switching behavior of IGBTs and other power electronic switches. Since this type of equipment was not available, the results mentioned above should be interpreted with some caution. To gain a thorough understanding of the relation between the main module turn-off, the non-idealities of the snubber diode and capacitor and the snubber parasitic inductance would require more sophisticated measurement techniques as well as more accurate models of these components.

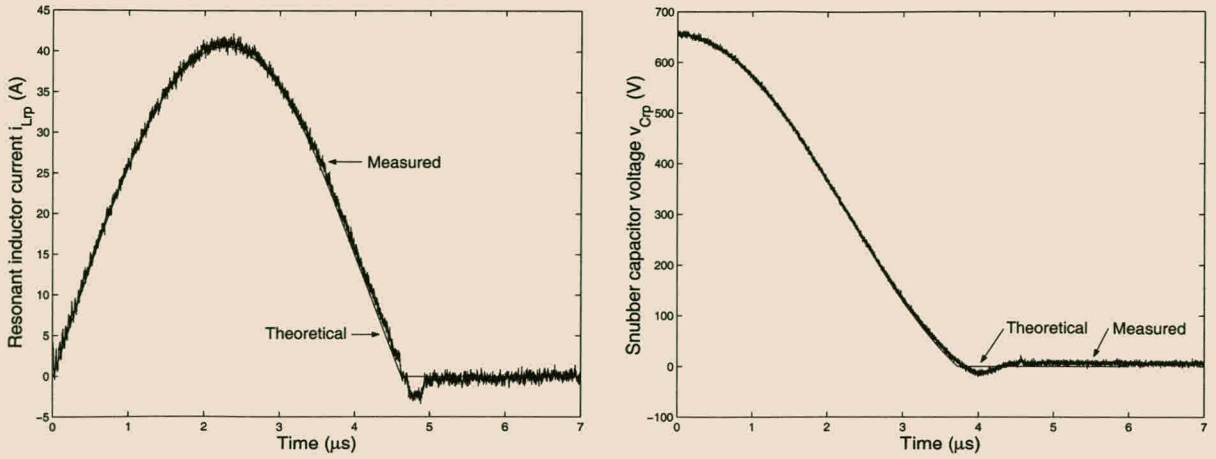
Despite several attempts to obtain measurement of the collector current using low inductance current shunts, reasonable results could not be obtained without introducing a significant amount of parasitic inductance into the circuit.

Another obvious difference between the measured and theoretical results is the negative going peak in v_{ce1} at the end of the turn-off cycle. This can be attributed to the reverse recovery of the snubber diode D_{rp}, which was not taken into account during the theoretical analysis. In all the experimental results of this section the current through the main IGBT is zero before diode D_{rp} turns off. Refer to Figure 2.30 for an explanation of the effect of the reverse recovery of D_{rp} on voltage v_{ce1}. Recall that the reverse recovery characteristics of a typical diode are shown in Figure 2.14. Since the reverse recovery time is small, the voltage across C_{rp} can be taken as constant during the reverse recovery period. During period t_5 (see Figure 2.14) the rate of change of current $\frac{di_{C_{rp}}}{dt}$ is positive, which results in a negative voltage peak

$$\Delta v_{D_{rp}} = V_{rr} - V_R \tag{2.98}$$

appearing across diode D_{rp}. The value of $\Delta v_{D_{rp}}$ is given by

$$\Delta v_{D_{rp}} = -(L_{bp} + L_s + L_{mn} + L_{bn})\frac{di_{C_{rp}}}{dt}. \tag{2.99}$$



(a) (b)

Figure 2.31: Capacitor discharge cycle. (a) Resonant inductor current; (b) Snubber capacitor voltage.

This causes a resulting negative voltage peak Δv_{ce1} given by

$$\Delta v_{ce1} = \Delta v_{D_{rp}} + L_s \frac{di_{Crp}}{dt} = -(L_{bp} + L_{mn} + L_{bn}) \frac{di_{C_{rp}}}{dt}. \tag{2.100}$$

2.2.8.1.2 Capacitor discharge cycle

Figure 2.31(a) shows current $i_{L_{rp}}$ through the top resonant inductor during capacitor discharge, while Figure 2.31(b) shows the voltage $v_{C_{rp}}$ over the snubber capacitor. The theoretical waveforms based on the analysis of section 2.2.6.2 are also shown.

The idealized theoretical discharge time $t_1 = \pi\sqrt{L_r C_r}$ equals 4.5 μs. In the practical circuit this is lengthened to approximately 4.7 μs due to the initial value of 655 V for the capacitor voltage and other non-idealities.

There are two noticeable differences between the theoretical and practical results. The first is the small (12 V) negative peak in $v_{C_{rp}}$ around 4 μs. This occurs just after D_{rp} turns on and can be attributed to the increase of current through the snubber parasitic inductance L_s. This was not taken into account in the theoretical analysis. The second difference is the reverse recovery current of diode D_{rp}. Recall that the auxiliary IGBT has an anti-parallel diode that provides a path for negative resonant inductor current. The effect of the reverse recovery of D_{rp} can be seen in Figure 2.31(a) and also gives rise to a small peak in voltage $v_{C_{rp}}$ around 4.7 μs.

2.2.8.1.3 Efficiency measurements

A calorimetric technique (similar to that in [94]) was used to determine the effect of the snubber

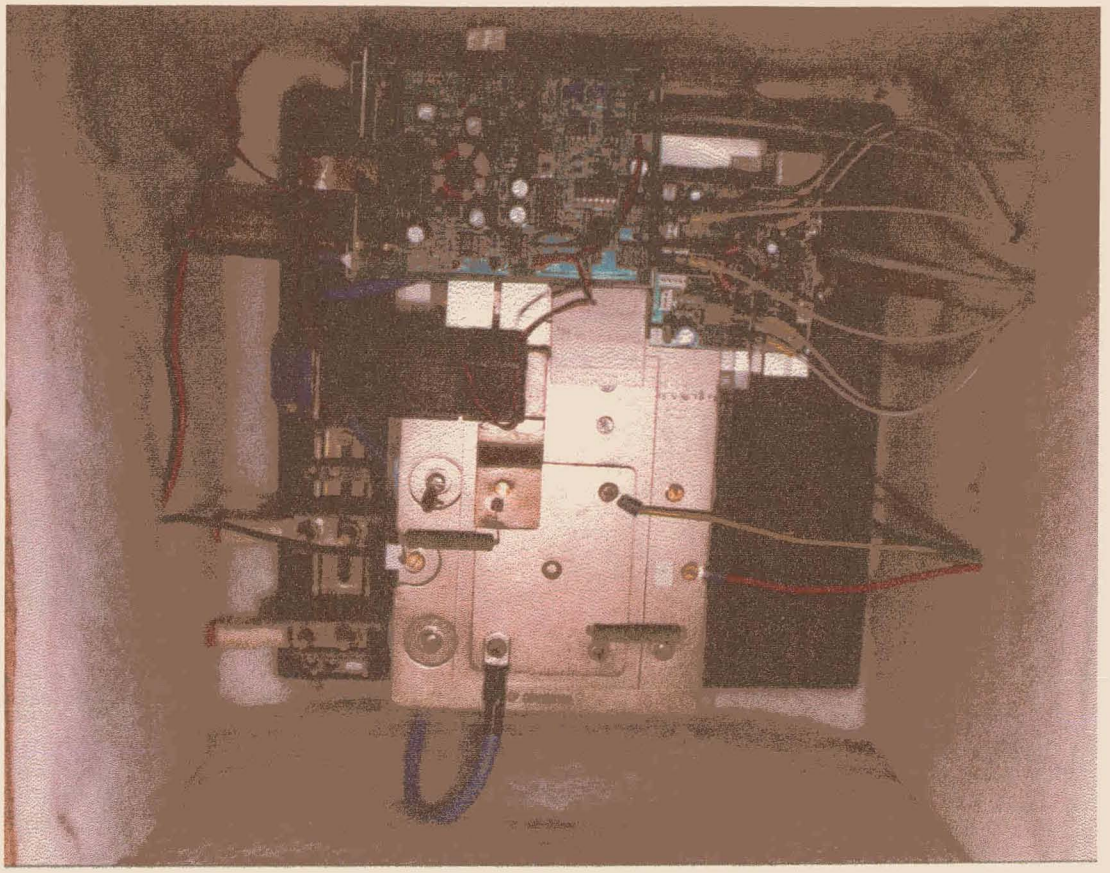


Figure 2.32: The converter fitted with the snubber inside the isolating box.

on the total converter losses. The main IGBT module was fitted on a water-cooled heatsink. The converter, with the snubber circuit, was placed in a closed isolated box. Water was circulated through the heatsink, with the flow rate controlled by a small electric pump. Figure 2.32 is a photograph of the converter in the isolated box.

Before determining the converter efficiency, the thermal characteristics of the isolated box were determined with no water flowing through the heatsink. A resistor was placed inside the box with a small electric fan circulating the air inside the box. The difference in the temperature of the air inside the box (denoted by T_b) and that outside the box (denoted by T_a) was measured. Table 2.15 shows the difference in air temperature inside and outside the box as a function of the amount of energy being dissipated in the resistor. After thermal equilibrium has been reached, the amount of energy dissipated in the resistor is equal to the amount of energy lost through the walls of the box. Based on the results of Table 2.15 the average thermal conductance σ_θ of the box is 1.7 W/K.

For the converter efficiency measurements the small electric fan was again used to circulate the air inside the box. The temperature of the water entering and leaving the box was measured electronically and logged. A two-hour period was allowed to ensure that the system reached thermal equilibrium. At the same time the temperature of the air inside the box was also

Power dissipated in resistor (W)	$T_b - T_a$ (K)	Thermal conductance σ_θ (W/K)
21	14.6	1.44
27	14.8	1.82
33	19.4	1.70
39	22.4	1.72
44	26.2	1.68

Table 2.15: Measured thermal characteristics of the isolating box.

measured. The total converter loss is given by

$$P_{loss(conv)} = c\frac{dm}{dt}\Delta T + P_{box}, \tag{2.101}$$

where c is the specific heat capacity of water (see [13], p. 308), $\frac{dm}{dt}$ is the flow rate (in $\frac{\text{kg}}{\text{s}}$) of the water through the box and ΔT is the temperature difference between the water entering the box and the water leaving the box. The value of c is equal to 4186 $\frac{\text{J}}{\text{kg K}}$ (see [13], p. 308). P_{box} is the amount of energy being lost through the walls of the box at the specific air temperature inside the box. Note that $P_{box} = \sigma_\theta(T_b - T_a)$. Since all the energy lost in the converter and snubber is accounted for in the measurement, the total converter efficiency is measured.

The total converter losses were measured, with a peak output current of 200 A at switching frequencies of 5 kHz and 10 kHz. Table 2.16 is a comparison of the calculated and measured converter losses. The main IGBT module turn-off loss was calculated by making use of the data sheet values for the hard-switched case. According to the data sheet the turn-off energy is approximately 25 mJ per cycle per IGBT. For the soft-switched case the theoretical voltage and current waveforms of Figure 2.28(f) were multiplied and integrated to calculate the main module turn-off loss.

The effect of the stray inductance resulted in almost double the turn-off loss in the main module compared to the idealized theoretical equations. The theoretical equations of section 2.2.4.1 yielded values of 26 W at 5 kHz and 52 W at 10 kHz, compared to 50 W at 5 kHz and 100 W at 10 kHz with the effect of the stray inductance included.

The main IGBT module conduction loss was calculated by making use of the data sheet values of the on-state voltages of the main IGBTs and free-wheeling diodes. A number of values of on-state voltage as a function of collector current were taken from the data sheets. A curve was fitted through these points and the losses were determined by numerically integrating the on-state voltage multiplied by the output current. The auxiliary circuit losses were calculated by making use of the idealized equations of section 2.2.4.2.

Finally, the equivalent series resistance of the DC-bus capacitors was used to calculate the

5 kHz Switching Frequency		
	Hard Switched	With Snubber
Main IGBT Turn-off Loss	250 W	40 W
Main IGBT Conduction Loss	202 W	202 W
Snubber Circuit Loss	0 W	9 W
DC-bus Capacitor Loss	137 W	137 W
Total	589 W	388 W
Measured	539 W	400 W
10 kHz Switching Frequency		
Main IGBT Turn-off Loss	500 W	80 W
Main IGBT Conduction Loss	202 W	202 W
Snubber Circuit Loss	0 W	18 W
DC-bus Capacitor Loss	137 W	137 W
Total	839 W	437 W
Measured	848 W	496 W

Table 2.16: Theoretical and measured converter losses with square wave output voltage.

conduction loss in the DC-link. According to the data sheet each of the four DC-bus capacitors has an equivalent series resistance of 41 mΩ and each capacitor carries a triangular current with a peak value of 50 A. This results in conduction loss of 137 W.

Given the inaccuracies involved in making efficiency measurements at high power levels, the theoretical and measured losses correspond well, with a maximum difference of 50 W (less than 15%).

For both values of the switching frequency the snubber reduced the turn-off loss in the main IGBT by 84%, while reducing the effective turn-off loss by 74%. Based on the data sheet values, on average the turn-on loss is approximately equal to the turn-off loss. However, at high current (200 A) and high temperature (125°C) the turn-off loss is equal to 3 times the turn-on loss. Depending on the temperature of the module and the output current, the addition of the snubber will lead to a reduction of approximately 37-50% in the main module switching loss, under sinusoidal PWM. Since the maximum switching frequency is in most applications limited by the switching loss, this implies that by adding the resonant snubber the switching frequency of the module can be increased by between 1.6 and 2 times. It should, however, be remembered that the maximum discharge time limits the maximum duty cycle at high switching frequencies. For the practical design of this section the maximum switching frequency is 15.9 kHz for a maximum duty cycle of 0.85.

Measurements of the effect of the snubber on the electric and magnetic fields close to the converter have been made. These can be found in [88] and will not be reported here because they were not performed according to an EMI standard.

2.2.8.2 Sinusoidal modulation

In this section the operation of the turn-off snubber using sinusoidal PWM is investigated. An average DC-bus voltage of 600 V is again used with an inductive load. The reference function is sinusoidal with a frequency of 100 Hz and a maximum duty cycle of 85%.

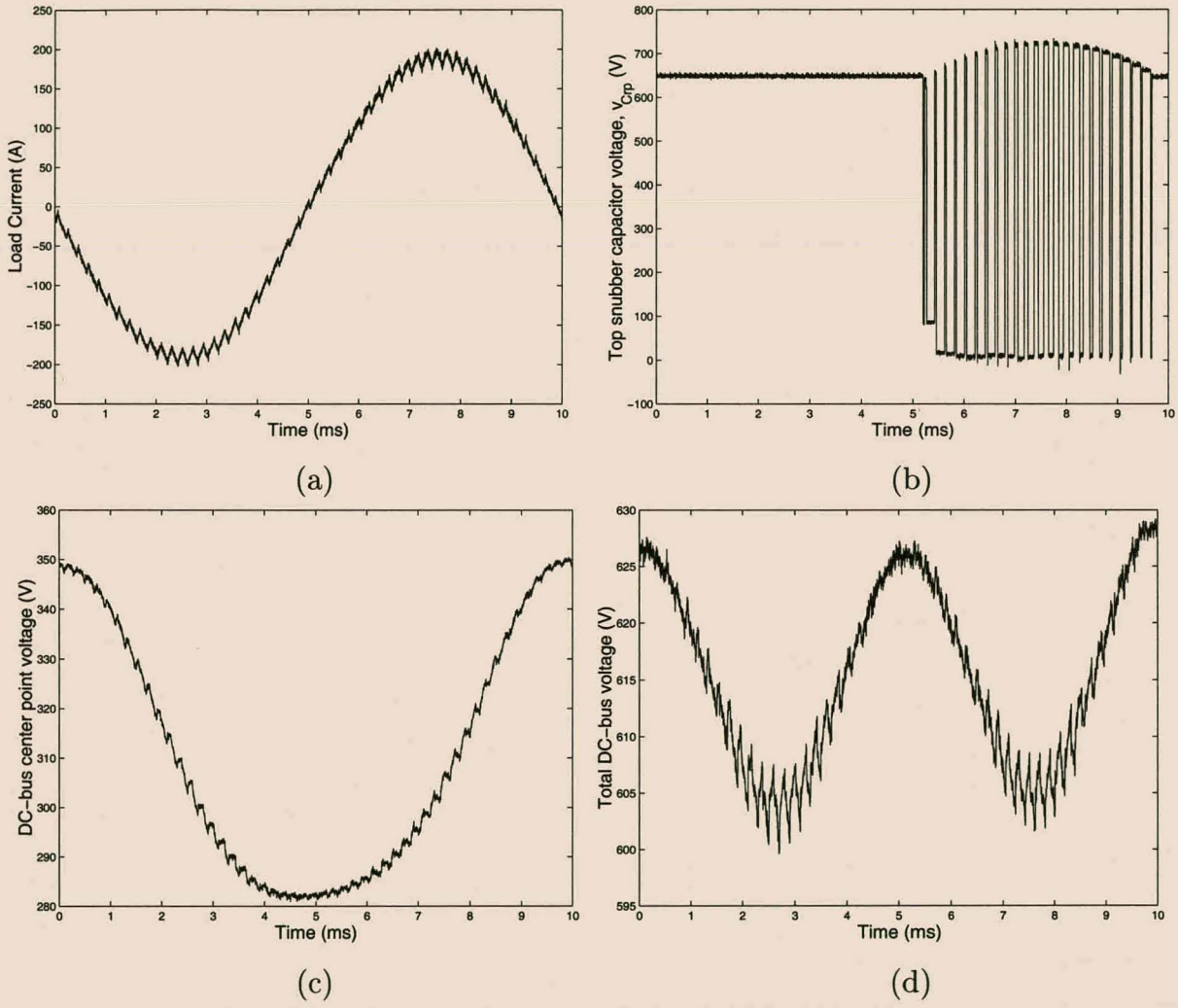


Figure 2.33: Operation of the turn-off snubber with sinusoidal modulation. (a) Load (output) current. (b) Voltage across the top snubber capacitor, $v_{C_{rp}}$. (c) DC-bus center point voltage. (d) Total DC-bus voltage.

Figure 2.33 shows the load current, voltage $v_{C_{rp}}$, the DC-bus center point voltage (with respect to the negative DC-bus terminal) and the total DC-bus voltage over one fundamental cycle.

Note that snubber capacitor C_{rp} does not fully discharge during the first two switching cycles

that the snubber circuit is triggered. This can be attributed to the fact that the DC-bus center point voltage has a value of approximately 280 V at this instant and the fact that the overshoot during main IGBT turn-off is small. This relatively small overshoot is a result of the small load current during this period. Also note the increase in the voltage overshoot at turn off as the load current increases.

2.3 Adding a turn-on snubber

In the final part of this chapter it is shown that a turn-on snubber can be combined with the turn-off snubber topology by intentionally increasing the bus inductance. Although this provides a method of reducing both the turn-on and turn-off losses, it does so at the expense of greater voltage stresses on the main and auxiliary IGBTs and increased current stresses on the auxiliary IGBTs. The design and control of the combined snubber are also more complicated than those of the turn-off snubber.

The aim of this section is to introduce the new combined turn-on and turn-off snubber and to explain its basic operating principles. The combined snubber will not be analyzed in as much detail as was done for the turn-on snubber. In the final part of this section the operation of the snubber is confirmed through experimental verfication.

2.3.1 Basic operation

Figure 2.34 shows the combined turn-on and turn-off snubber. It is the turn-off snubber topology with added bus inductance that acts as a turn-on snubber. The combination of inductors L_{bp} and L_{bn} forms the turn-on snubber for both the main switches. The energy stored in these inductors has to be absorbed by the turn-off snubber capacitor and will cause a voltage overshoot across the main switches at turn-off. This also leads to increased voltage and current stresses on the auxiliary switches. Inductors L_{bp} and L_{bn} are equal in value and will be denoted by L_b.

To explain the operation of the snubber, the case where the load current I_o is positive is considered. The operation of the snubber during periods of negative load current is totally symmetrical and will not be discussed in detail. The assumptions made in the analysis are the same as those made during the initial analysis of the turn-off snubber and can be found on p. 19.

Refer to Figures 2.35 and 2.36 for the explanation of the snubber operation. The operation of the snubber during the first part (till D_n turns on) of the turn-off cycle is identical to the operation of the turn-off snubber. For time $t < 0$ switch G_p conducts the load current I_o, which

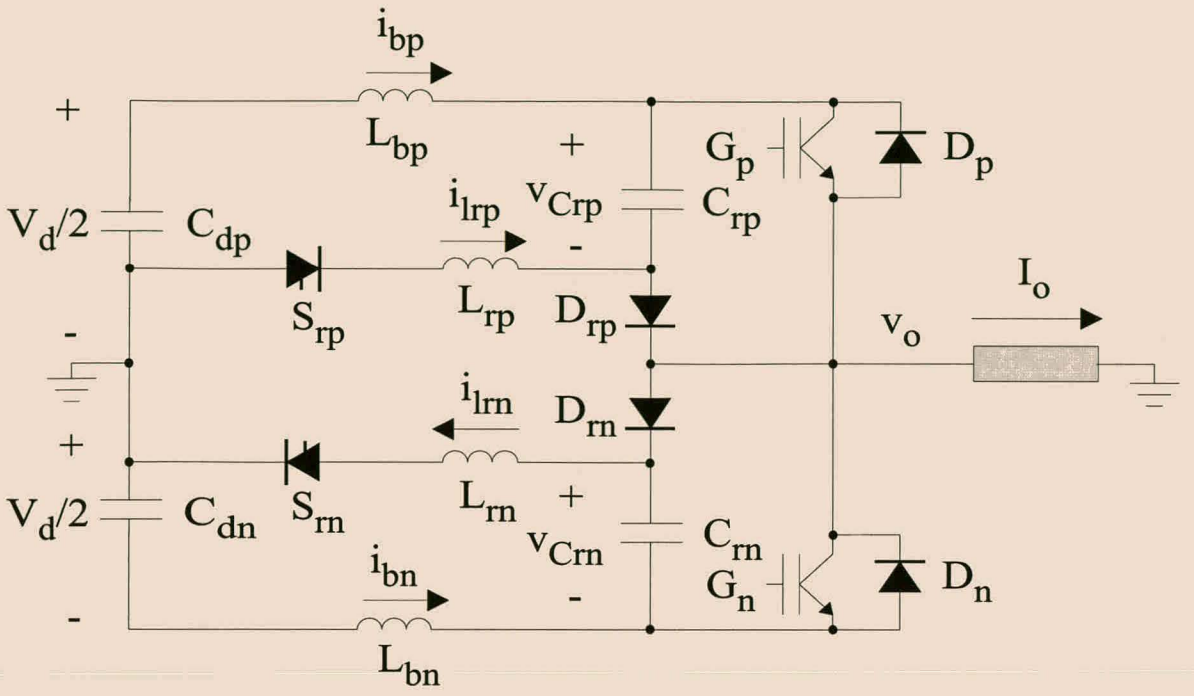


Figure 2.34: Combined turn-on and turn-off snubber.

also flows through inductor L_{bp}. Capacitor C_{rp} is totally discharged, with $v_{C_{rp}} = 0$. At $t = 0$ switch G_p is turned off and diode D_{rp} becomes forward biased. This results in G_p turning off at zero voltage. Capacitor C_{rp} and diode D_{rp} takes over the load current from G_p and C_{rp} charges at a rate

$$\frac{dv_{C_r}}{dt} = \frac{I_o}{C_r}. \tag{2.102}$$

At time $t_1 = \frac{C_r V_d}{I_o}$ the voltage across C_{rp} reaches V_d and D_n becomes forward biased. D_n and L_{bn} starts taking over the load current I_o from L_{bp}, while L_{bp} and L_{bn} resonates with C_{rp}. During this resonant cycle currents i_{bn} and i_{bp} are given by

$$i_{bn} = I_o(\cos\omega_0(t - t_1) - 1) \tag{2.103}$$

and

$$i_{bp} = I_o \cos\omega_0(t - t_1), \tag{2.104}$$

where $\omega_0 = \frac{1}{\sqrt{2L_b C_r}}$. Voltage $v_{C_{rp}}$ is given by

$$v_{C_{rp}} = I_o\sqrt{\frac{2L_b}{C_r}}\sin\omega_0(t - t_1) + V_d. \tag{2.105}$$

At time $t_2 = t_1 + \frac{\pi}{2\omega_0}$ diode D_{rp} turns off and voltage $v_{C_{rp}}$ reaches $V_d + I_o\sqrt{\frac{2L_b}{C_r}}$. Note that this voltage also appears across G_p. This means that an extra voltage overshoot equal to $I_o\sqrt{\frac{2L_b}{C_r}}$ appears across the main switch G_p during turn-off compared to ideal hard-switched conditions. It should, however, be noted that under hard-switched conditions the full voltage rating of the main switch can also not be utilized due to voltage overshoot caused by the steep turn-off

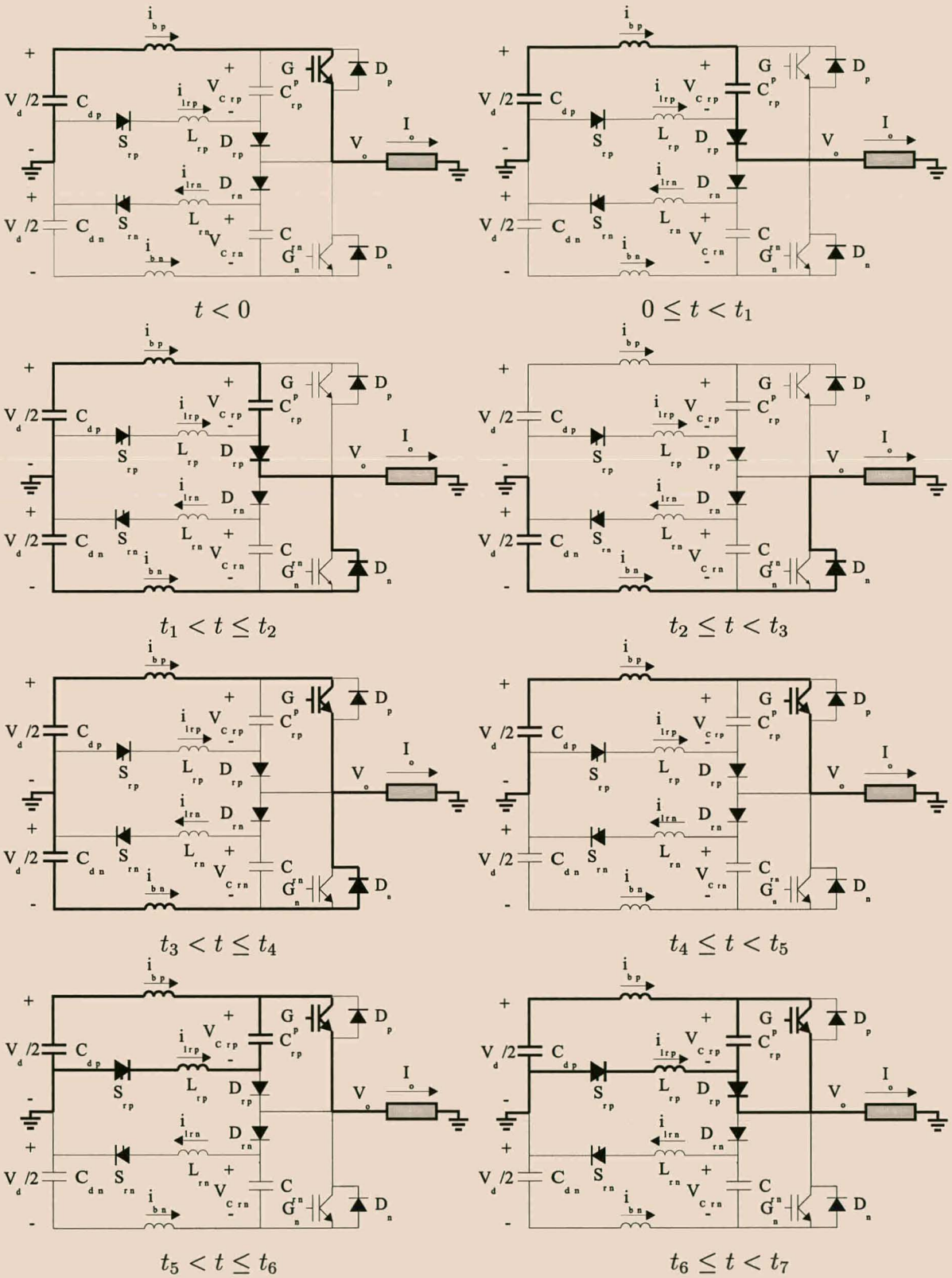


Figure 2.35: Different operating modes of the combined turn-on and turn-off snubber.

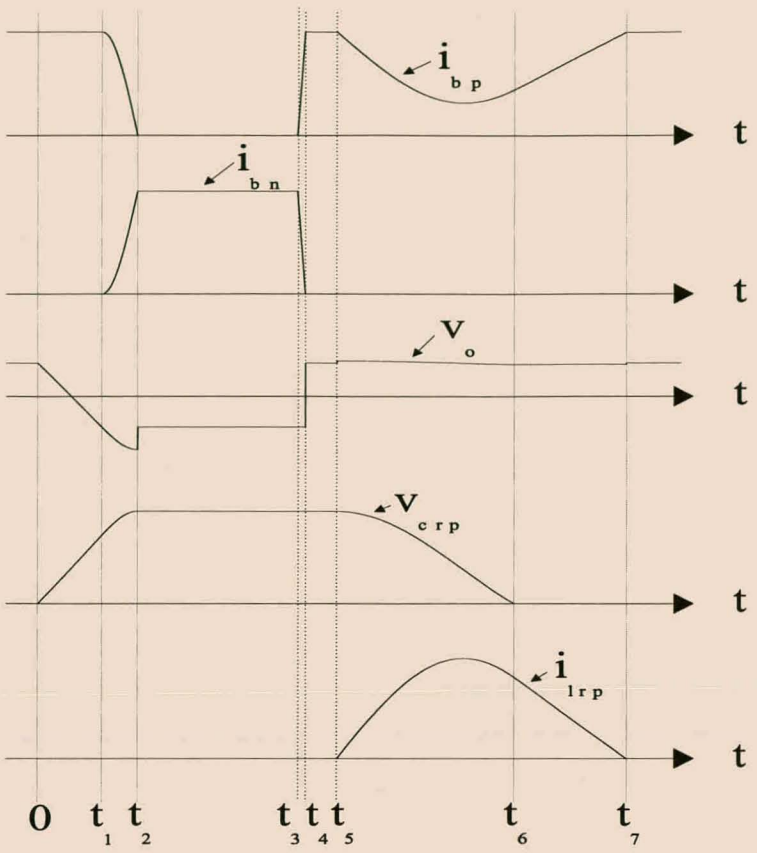


Figure 2.36: Combined turn-off and turn-on snubber voltage and current waveforms.

transients. Typically the maximum DC-bus voltage is not chosen greater than two thirds of the main switch peak voltage rating.

During the period $t_2 \leq t < t_3$ D_n and L_{bn} conducts the load current. Time $t_3 - t_2$ was deliberately chosen small in Figure 2.36 to illustrate the operation of the snubber. In practical converters this time will be large compared to the period of snubber operation. At time t_3 switch G_p is turned on (at zero current) and current i_{bp} increases at a rate of

$$\frac{di_{bp}}{dt} = \frac{V_d}{2L_b}. \tag{2.106}$$

At $t_4 = t_3 + \frac{2I_oL_b}{V_d}$ current i_{bp} reaches I_o and D_n turns off. The top main switch G_p now conducts the full load current. At time t_5 auxiliary switch S_{rp} is triggered. Inductors L_{bp} and L_{rp} resonate with C_{rp}. In the process capacitor C_{rp} is discharged and the stored energy is returned to the DC-bus capacitors. The current in the resonant inductor, $i_{L_{rp}}$, is given by

$$i_{L_{rp}} = \sqrt{\frac{C_r}{L_r + L_b}} \left(\frac{V_d}{2} + I_o \sqrt{\frac{2L_b}{C_r}} \right) \sin \omega_1 (t - t_5), \tag{2.107}$$

where $\omega_1 = \frac{1}{\sqrt{C_r(L_r+L_b)}}$. Voltage $v_{C_{rp}}$, across the resonant capacitor, is given by

$$v_{C_{rp}} = \left(\frac{V_d}{2} + I_o \sqrt{\frac{2L_b}{C_r}} \right) \cos \omega_1 (t - t_5) + \frac{V_d}{2}. \tag{2.108}$$

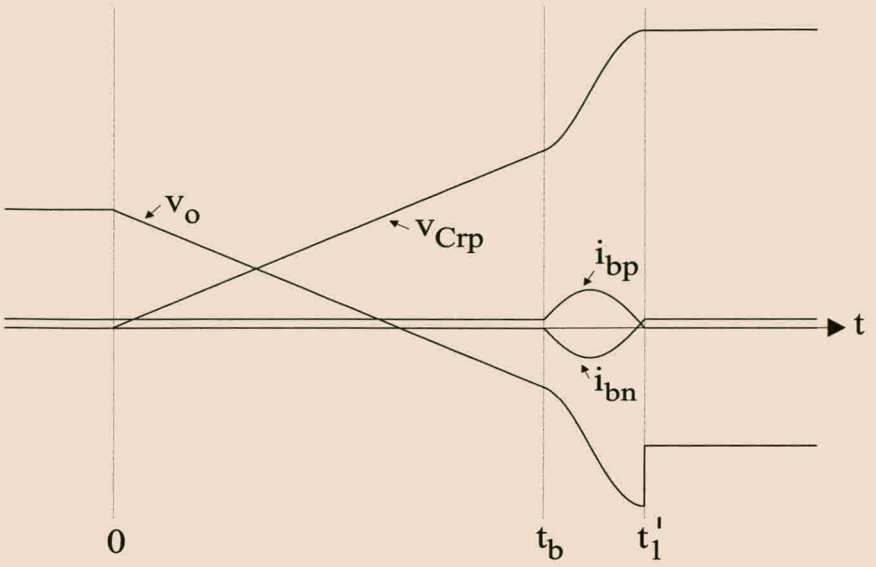


Figure 2.37: Combined snubber voltage and current waveforms under low output current.

At time $t_6 = t_5 + \frac{1}{\omega_1} \arccos\left(-\frac{V_d/2}{V_d/2+I_o\sqrt{\frac{2L_b}{C_r}}}\right)$ voltage $v_{C_{rp}}$ reaches zero and diode D_p turns on, clamping the voltage $v_{C_{rp}}$ at 0. Current $i_{L_{rp}}$ decreases at a rate of

$$\frac{di_{L_{rp}}}{dt} = -\frac{V_d}{2(L_b + L_r)}. \tag{2.109}$$

At time

$$t_7 = t_6 + 2\frac{L_b + L_r}{V_d}\sqrt{\frac{C_r}{L_r + L_b}}\left(\frac{V_d}{2} + I_o\sqrt{\frac{2L_b}{C_r}}\right)\sqrt{1 - \left(\frac{1}{1 + I_o\frac{2}{V_d}\sqrt{2\frac{L_b}{C_r}}}\right)^2} \tag{2.110}$$

switch S_{rp} turns off. G_p is now conducting the load current, while C_{rp} is fully discharged and the whole cycle starts over again.

To simplify the analysis it was assumed that the auxiliary switch S_{rp} was triggered some time after G_p is turned on. In practical systems the control is simplified if S_{rp} is triggered at the same time as G_p is turned on. This does not result in a significant modification of the snubber behavior.

As for the turn-off snubber some consideration has to be given to the discharge time of snubber capacitor C_{rp}. As the output current I_o decreases, the discharge time t_1 of this capacitor will start to exceed the converter blanking time t_b. This is the case if

$$I_o < C_r\frac{V_d}{t_b}. \tag{2.111}$$

Figure 2.37 shows the operation of the snubber in this case. At $t = 0$ G_p is turned off and the output voltage v_o starts decreasing. At time t_b, before $v_{C_{rp}}$ reaches V_d, the blanking time

expires and G_n turns on. During the period $t_b < t \leq t_1'$ voltage $v_{C_{rp}}$ is given by

$$v_{C_{rp}} = \left(\frac{I_o}{C_r}t_b - V_d\right)\cos\omega_0(t-t_b) + \frac{I_o}{C_r\omega_o}\sin\omega_0(t-t_b) + V_d, \tag{2.112}$$

while i_{bp} is given by

$$i_{bp} = I_o\cos\omega_0(t-t_b) - (I_o t_b - V_d C_r)\omega_0\sin\omega_0(t-t_b). \tag{2.113}$$

In the process currents i_{bp} and i_{bn} significantly increase in amplitude, as L_{bp} and L_{bn} resonates with C_{rp}. At time

$$t_1' = t_b + \frac{1}{\omega_0}\left(\pi + \arctan\left(\frac{I_o}{\omega_0(I_o t_b - V_d C_r)}\right)\right) \tag{2.114}$$

diode D_{rp} turns off as i_{bp} reaches zero. At this instant voltage $v_{C_{rp}}$ is given by

$$v_{C_{rp}}\text{max} = \frac{\frac{\omega_0}{C_r}(I_o t_b - V_d C_r)^2 + \frac{I_o^2}{C_r\omega_0}}{\sqrt{I_o^2 + (I_o t_b - V_d C_r)^2 w_0^2}} + V_d. \tag{2.115}$$

A similar situation occurs if the snubber capacitor is discharged and the output current changes sign during the switching cycle.

2.3.2 Implementation considerations

By carefully balancing the snubber components, the voltage stresses on the main switches as well as the peak current rating of the auxiliary switches can be optimized. The following considerations should be kept in mind during selection of the snubber components:

1. Care should be taken not to exceed the peak voltage rating of the main switches. If the output current I_o is large, the maximum voltage over the main switches is given by equation 2.105. It is important not to exceed the rated voltage of the main switches when turning off under short-circuit conditions. The addition of the turn-on inductance does, however, limit the rate of increase of the short-circuit current and allows for more time to detect short-circuit conditions through the use of a current sensor. By increasing the size of the snubber capacitor the maximum overshoot is decreased at the cost of longer turn-off times and increased current rating of the auxiliary switches. By decreasing the size of the turn-on inductors, the turn-off voltage overshoot is decreased at the expense of increased turn-on loss in the main switches.

2. If the output current is small, equation 2.115 gives the maximum voltage across the main switches. Proper selection of the blanking time is necessary not to exceed the main device voltage rating. Excessive blanking time does, however, limit the maximum obtainable duty cycle and introduces non-linearities in the control of the converter.

C_r	400 nF
L_b	450 nH
L_r	4 uH
V_d	235 V
I_o	75 A
Switching frequency	8 kHz

Table 2.17: System parameters used in the experimental evaluation of the combined turn-off and turn-on snubber.

3. The case where the output current changes sign should be carefully considered. One possible method of avoiding this problem is to cease discharging the snubber capacitors at low output currents. This is similar to the strategy followed for the turn-off snubber. Care should, however, be taken to ensure that the voltage over the snubber capacitors does not exceed the maximum allowable voltage of the main switches.

4. By increasing the size of the resonant inductors the peak current rating of the auxiliary switches is decreased (according to equation 2.107) at the expense of increased discharge times of the snubber capacitor. This discharge time in turn limits the minimum (and maximum) duty cycle of the converter. This was also true for the turn-off snubber.

An optimal design procedure, similar to that developed for the turn-off snubber is currently being developed by Mr. F.W. Combrink. Mr. Combrink is also studying the different implementation considerations, including those mentioned above.

2.3.3 Experimental Results

In this section the basic operating principles of the combined turn-on and turn-off snubber are illustrated experimentally. Recall that three different versions of the turn-off snubber were constructed and tested on the PDM200DSA120 integrated power module. The second experimental version of the turn-off snubber was modified for the purpose of evaluating the combined snubber by adding turn-on inductors. Table 2.17 summarizes the different component values used in this experimental snubber.

Figure 2.38 shows the turn-off voltage waveform of G_p with the snubber circuit. The voltage fall time (from $\frac{V_d}{2}$ to $-\frac{V_d}{2}$) is approximately 1.5 μs. The turn-off voltage waveform is essentially the same as for the turn-off snubber alone with extra overshoot at the end of the cycle due to the increased inductance. The ringing around 6 μs is a result of resonance between the load inductor and parasitic capacitance in the circuit, resulting in a voltage drop across L_{bn}.

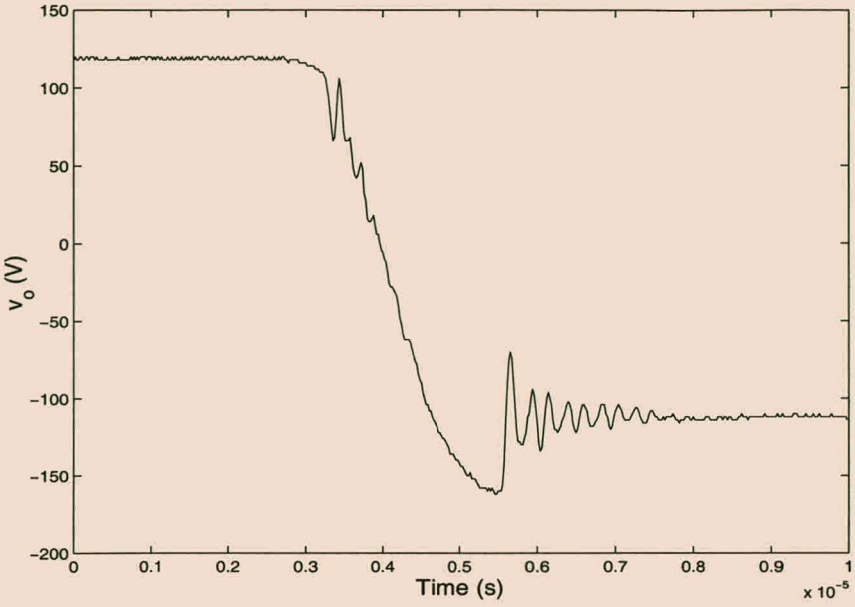


Figure 2.38: Converter output voltage waveform with the combined turn-on and turn-off snubber during main module turn-off.

Figure 2.39 shows the top IGBT collector emitter voltage and collector current during the turn-on cycle. The collector emitter voltage drops to approximately 25 V before the collector current starts to increase. This is in sharp contrast to the hard-switched case, where the collector current has to increase to I_o before v_{ce} will start to decrease. The ringing in i_{bp} is again a result of the load inductor resonating with parasitic capacitances in the circuit.

Figure 2.40 shows $v_{C_{rp}}$ and $i_{L_{rp}}$ during the capacitor discharge cycle. This is also essentially the same as for the turn-off snubber alone, except for the fact that extra energy has to be recovered due to the increased voltage overshoot at turn-off.

2.4 Summary

This chapter introduced a new resonant snubber topology based on the auxiliary resonant pole converter, but with much smaller peak current ratings for the auxiliary switches. As a first step a resonant turn-off snubber was introduced and its properties studied.

A detailed investigation into the different loss mechanisms was made by using simple models of the IGBT current and voltage tail-forming characteristics and by taking the effect of a number of parasitic components into account. Analytic expressions for the different loss components were derived. These expressions formed the basis for an optimal snubber design procedure.

The influence of the different parasitic components on the snubber operation was studied in detail. The snubber parasitic inductance has the most significant effect and gives rise to a

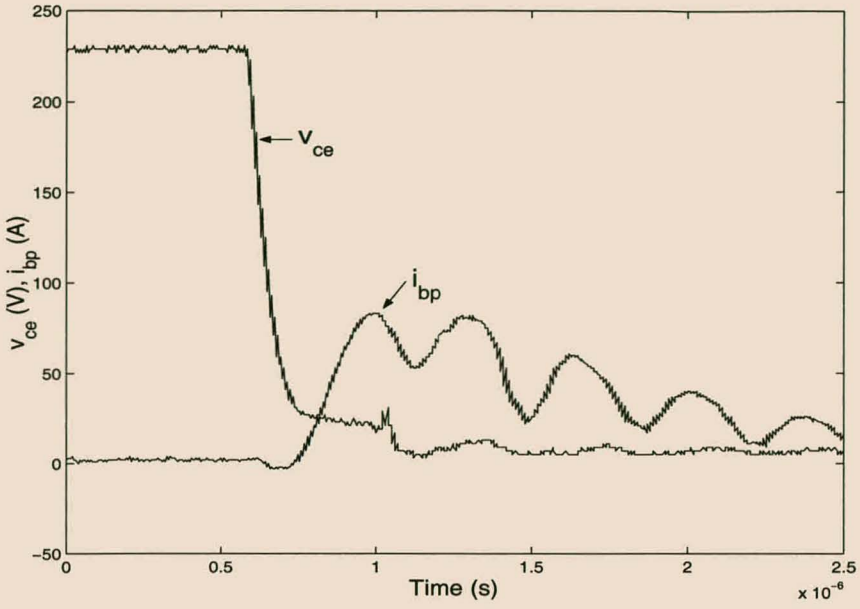


Figure 2.39: Top IGBT voltage and current waveforms during turn-on.

substantial decrease in the snubber efficiency (typically a 100% increase in the expected turn-off loss). One possibility for reducing the parasitic inductance is to integrate the main IGBT, snubber diode and snubber capacitor into a single module.

An experimental version of the turn-off snubber was constructed at one third of the power rating required for a full 2 MVA converter. The experimental results agreed closely with the theoretical predictions. However, it was shown that the simplified tail-forming models of the IGBT are not accurate, especially during the first part of the main IGBT turn-off cycle. This appears to be related to the influence of the snubber parasitic inductance on the main module turn-off behavior.

In the final part of the chapter turn-on inductance was added to the basic turn-off snubber topology. The benefits of the turn-on snubber come at the expense of larger voltage stresses on the main switches and larger voltage and current stresses on the auxiliary switches. Only the basic operating principles of the turn-on snubber were discussed and verified experimentally.

As mentioned earlier, the work on the new resonant topology is currently being continued at the University of Stellenbosch. Future research objectives include the following:

1. A detailed analysis and control strategy for the combined turn-on and turn-off snubber.
2. Operation and protection of the snubber under overcurrent conditions.
3. An optimal design procedure for this snubber.
4. An investigation of the effect of the snubber on the EMI generated by power electronic converters.

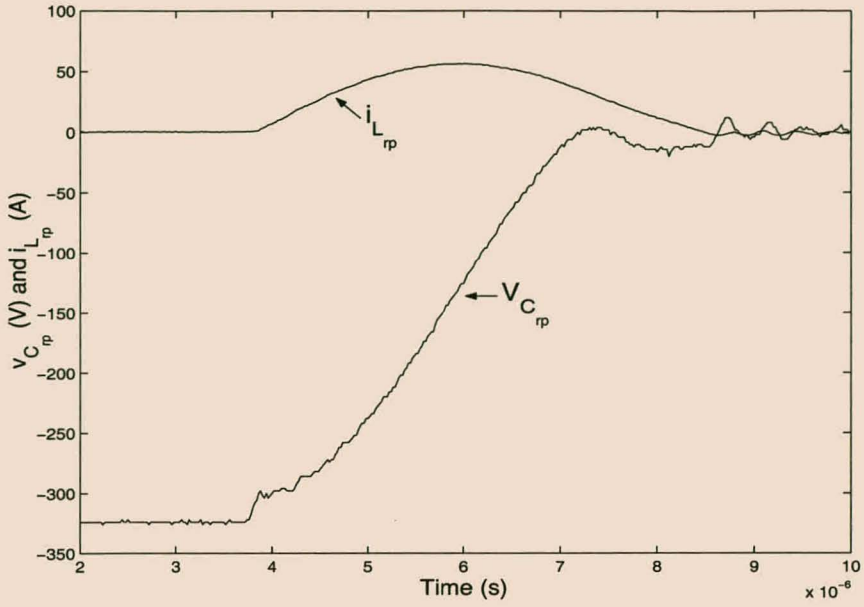


Figure 2.40: Capacitor discharge cycle for the combined turn-on and turn-off snubber.

5. A detailed experimental evaluation of the combined turn-on and turn-off snubber.

It was experimentally confirmed in this chapter that the new snubber topology effectively decreases switching losses. By decreasing the switching losses the switching frequency can be increased, which results in improved performance and smaller filter components. This comes at the expense of additional hardware and a more complicated system.

In the next chapter it will be shown that, for the application in mind, some of these benefits can be obtained in a totally different way without introducing extra hardware. By applying interleaved switching to the series-stacked converter, the effective switching frequency can be increased substantially. At the same time the power ratings of the individual converter building blocks add up to form a single high-power converter.

Based on these considerations, it was decided not to use soft switching in the experimental 2 MVA converter.

Chapter 3

Analysis of series-stacked converters

3.1 Introduction

One of the key considerations when designing series-stacked and multi-level converters is the balancing and stability of the different capacitor voltages. Power electronic switches are extremely sensitive to over-voltages and significant unbalance on one of the series-stacked DC-buses will almost certainly lead to destruction of one or more of the levels of the converter. On the other hand, to utilize the full power rating of the power electronic switches it is necessary to use the switching devices as close as possible to their peak voltage ratings. Based on these considerations, it is of vital importance to thoroughly understand the different DC-bus balancing mechanisms of the series-stacked converter. This is the subject of this chapter.

In general, the modeling of power electronic converters for design and control purposes is a difficult task. The systems consist of continuous elements (for instance, capacitors and inductors) and discrete switching elements. As mentioned in [44] this gives rise to two types of models, namely continuous and discrete. When using the first approach (see, for instance, [87]) the converter voltages and currents are averaged over one switching cycle. Although this technique is widely applied when designing closed loop controllers, it will be shown later in this chapter that the state space averaging technique destroys some of the vital information of the balancing process.

Although a number of references on the series-stacked converter topology can be found in the literature ([61], [34] and [47]), a detailed study of the DC capacitor voltage balancing mechanisms could not be found. The approach followed in this thesis is to use fundamental results from the theory of systems of linear differential equations to study the behavior of series-stacked converters. As a first step the system of differential equations describing the behavior of the converter is derived. These are then rewritten in a way that facilitates an understanding of the different balancing mechanisms. Basic theorems from the theory of systems of linear differential

equations and Floquet theory are then used to study the different balancing mechanisms. The two main objectives of this analysis are outlined below:

1. Any converter non-ideality can be seen as a perturbation of the original ideal system. The first objective is to prove that the system is stable and will return to its equilibrium point after a perturbation is removed.

2. The detailed properties and dynamics of the DC-bus balancing mechanisms will be studied. This includes determining the time constants involved with the balancing mechanisms.

In [44] a mathematical model capable of representing the self-balancing properties of multi-level converters is derived. The approach in this paper is to assume that the load time constants are significantly smaller than each switching period. Based on this assumption, the different voltages and currents of the converter and load are assumed to be in the steady-state after each switching cycle. Fourier techniques are then used to determine the different capacitor currents and to derive the change in capacitor voltage. Although the techniques of this paper provide interesting insights into the balancing mechanisms, they cannot be generalized to series-stacked converters. The main difficulty is that the assumption that the converter is in the steady-state after one switching cycle does not apply in general. Some of the methods of this chapter will however be based on the techniques of [44].

In this chapter it will be shown that two- and three-level series-stacked converters are stable and will balance naturally under a variety of operating conditions. As a first step the properties of these converters when the same gating signals are applied to all the levels (referred to as ordinary switching) are studied. It will be shown that, when applying ordinary switching, the DC capacitor voltages will balance under all operating conditions. As a second step the behavior of the converters under interleaved switching is analyzed. The main conclusion of this analysis is that as long as the converter switching frequency is chosen so as to be significantly higher than the highest frequency harmonic of its reference signal, the DC capacitor voltages will balance naturally. Although the possibility of forcing the DC-bus voltages to balance through active control does exist, it is found that due to natural balancing this is in general not necessary and will not be pursued further in this thesis.

3.2 Two-level series-stacked converters

Figure 3.1 shows the two-level series-stacked converter. It consists of two standard full-bridge converters with their DC-buses stacked in series. The outputs of the two converters are filtered and connected to two identical primaries of a series-injection transformer.

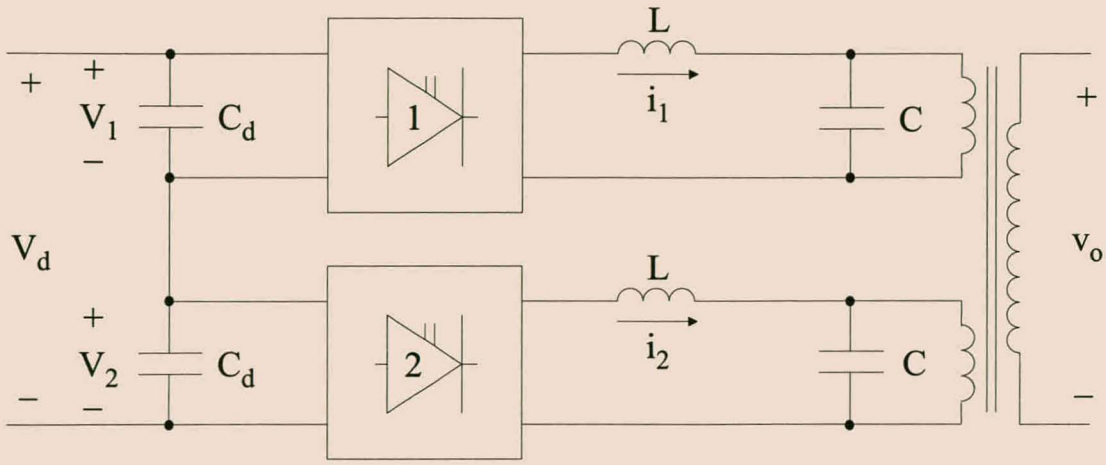


Figure 3.1: Two-level series-stacked converter.

3.2.1 Two-port switching circuits

Throughout this chapter the concept of a two-port switching circuit will be applied. It is a theoretical generalization of a full-bridge converter.

Figure 3.2 shows the basic two-port switching circuit which is controlled by a *switching function* s of t. The arrow points from port 1 to port 2. The relations between voltages v_1 and v_2 and currents i_1 and i_2 are given by

$$v_2 = sv_1 \quad \text{and} \quad i_1 = si_2. \tag{3.1}$$

The switching function s can assume any real value and the two-port switching circuit can be thought of as an 'ideal transformer' with time dependent 'winding ratio' s.

In the case of a full-bridge converter s is the converter switching state and assumes the values -1, 0 and 1.

3.2.2 Basic circuit analysis

In this section the differential equations describing the two-level series-stacked converter are derived. These differential equations are then rewritten in a way that facilitates the analysis of

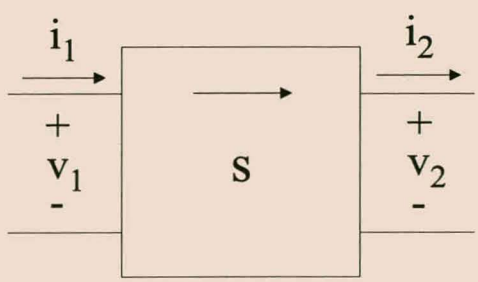


Figure 3.2: Two-port switching circuit.

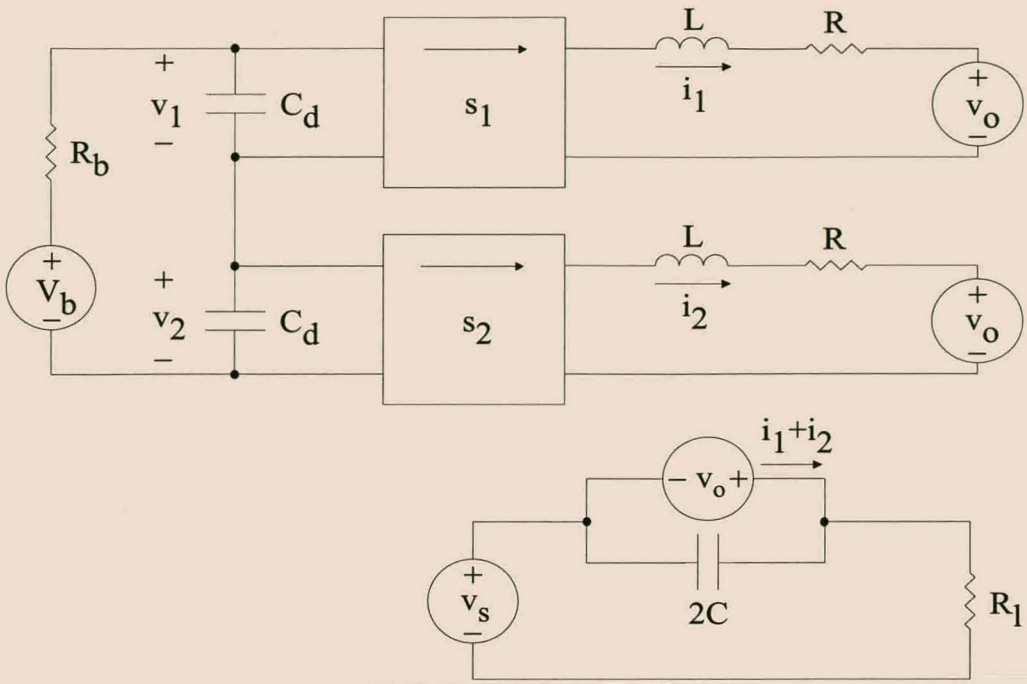


Figure 3.3: Equivalent circuit of the two-level series-stacked converter used in the analysis.

the balancing properties of the series-stacked converter.

Figure 3.3 shows the equivalent circuit of a two-level series-stacked converter topology applied as a series-injection power-quality device. Note that the filter capacitors have been referred across the injection transformer. In order to gain a basic understanding of the properties of the converter a number of simplifications are made. The load is modeled by a resistor R_l, while the supply is modeled as a voltage source v_s. The supply-side impedance is discarded for the sake of simplicity. In practical situations the load and supply will be much more complex. However, a more complete model of the full system increases the order of the differential equations and significantly complicates the process of gaining an understanding of the basic balancing mechanisms.

The following assumptions are made throughout this chapter:

1. The DC-bus is connected to a voltage source V_b with an equivalent source resistance of R_b.

2. The power electronic switches have no turn-on and turn-off delay and all four switches have identical switching behavior.

3. The passive components of the two full-bridge converters are identical. It is further assumed that all the passive components are totally linear.

4. The injection transformer is modeled as an ideal transformer with no leakage inductance and infinite magnetizing inductance. During the analysis it is also assumed that the

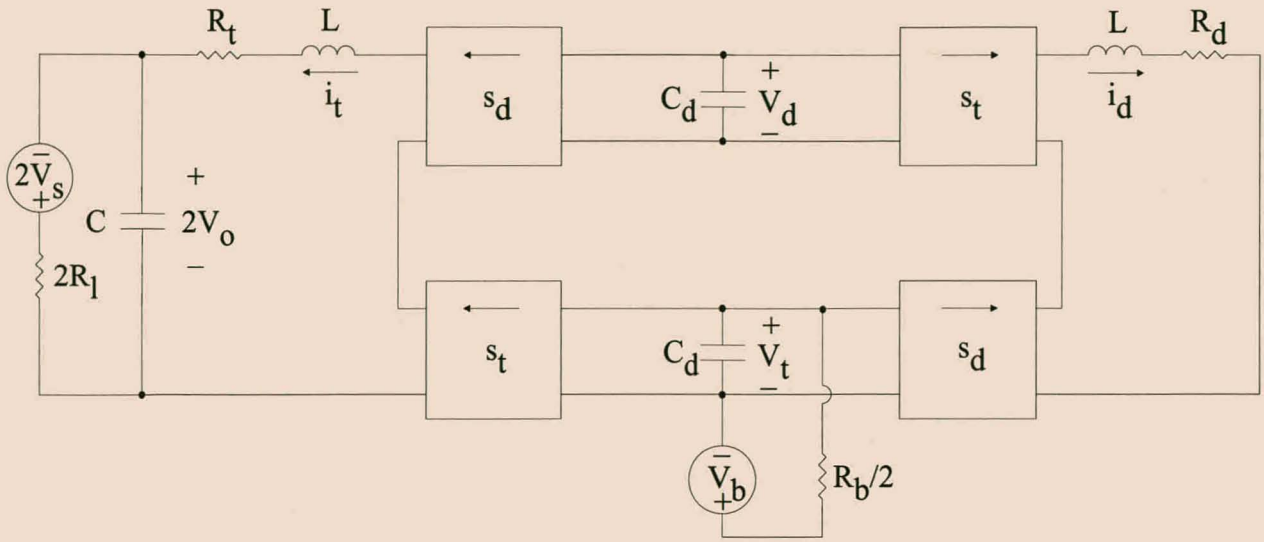


Figure 3.4: Two-level series-stacked converter in terms of d and t parameters.

transformer has a 1:1 turn ratio. This can be done without loss of generality since the secondary side circuit can be referred to the primary side.

5. For the moment it is assumed that the load is purely resistive.

6. The losses in the switching components, filter inductors and the primary side copper losses of the transformer are presented by resistor R.

7. Finally, it is assumed that both full-bridge converters will not remain in the zero state indefinitely.

Let s_1 be the switching function of the top converter and s_2 the switching function of the bottom converter. The behavior of the two-level series-stacked converter is described by the following system of differential equations:

$$\begin{bmatrix} \frac{di_1}{dt} \\ \frac{di_2}{dt} \\ \frac{dv_1}{dt} \\ \frac{dv_2}{dt} \\ \frac{dv_o}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 & \frac{s_1}{L} & 0 & -\frac{1}{L} \\ 0 & -\frac{R}{L} & 0 & \frac{s_2}{L} & -\frac{1}{L} \\ -\frac{s_1}{C_d} & 0 & -\frac{1}{R_b C_d} & -\frac{1}{R_b C_d} & 0 \\ 0 & -\frac{s_2}{C_d} & -\frac{1}{R_b C_d} & -\frac{1}{R_b C_d} & 0 \\ \frac{1}{2C} & \frac{1}{2C} & 0 & 0 & -\frac{1}{2R_l C} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ v_1 \\ v_2 \\ v_o \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \frac{V_b}{R_b C_d} \\ \frac{V_b}{R_b C_d} \\ -\frac{v_s}{2R_l C} \end{bmatrix} \tag{3.2}$$

As mentioned earlier, in general the load will be more complex. In this case all the capacitor voltages and inductor currents in the equivalent model of the load have to be included in this system of differential equations. This does, however, not result in any significant changes to the theory, other than increasing the order of the matrices.

In order to study the balancing of the system the following variables are introduced:

$$i_d := i_1 - i_2, \quad v_d := v_1 - v_2, \quad s_d := \frac{s_1 - s_2}{2} \tag{3.3}$$

and

$$i_t := i_1 + i_2, \quad v_t := v_1 + v_2, \quad s_t := \frac{s_1 + s_2}{2}. \tag{3.4}$$

Rewriting equation 3.2 in terms of the d and t currents and voltages results in

$$\begin{bmatrix} \frac{di_d}{dt} \\ \frac{dv_d}{dt} \\ \frac{di_t}{dt} \\ \frac{dv_t}{dt} \\ \frac{dv_o}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \frac{s_t}{L} & 0 & \frac{s_d}{L} & 0 \\ -\frac{s_t}{C_d} & 0 & -\frac{s_d}{C_d} & 0 & 0 \\ 0 & \frac{s_d}{L} & -\frac{R}{L} & \frac{s_t}{L} & -\frac{2}{L} \\ -\frac{s_d}{C_d} & 0 & -\frac{s_t}{C_d} & -\frac{2}{R_b C_d} & 0 \\ 0 & 0 & \frac{1}{2C} & 0 & -\frac{1}{2R_l C} \end{bmatrix} \begin{bmatrix} i_d \\ v_d \\ i_t \\ v_t \\ v_o \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ \frac{2V_b}{R_b C_d} \\ -\frac{v_s}{2R_l C} \end{bmatrix}. \tag{3.5}$$

Figure 3.4 shows the equivalent circuit associated with this system of differential equations. Resistors R_d and R_t are both equal in value to R. Each of the switching blocks is a two-port switching circuit with the arrow pointing from port 1 to port 2.

3.2.3 Ordinary switching

In this section it is assumed that the same switching functions are applied to both converters of the two-level series-stacked topology. This will be referred to as *ordinary switching*. Hence we assume that $s := s_1 = s_2$, from which it follows that $s_t = s$ and $s_d = 0$. This results in the following two independent systems of differential equations:

$$\dot{x}_d = A_d x_d, \tag{3.6}$$

where

$$x_d = \begin{bmatrix} i_d \\ v_d \end{bmatrix}, \quad A_d(s) = \begin{bmatrix} -\frac{R}{L} & \frac{s}{L} \\ -\frac{s}{C_d} & 0 \end{bmatrix}; \tag{3.7}$$

and

$$\dot{x}_t = A_t x_t + B_t, \tag{3.8}$$

where

$$x_t = \begin{bmatrix} i_t \\ v_t \\ v_o \end{bmatrix}, \quad A_t(s) = \begin{bmatrix} -\frac{R}{L} & \frac{s}{L} & -\frac{2}{L} \\ -\frac{s}{C_d} & -\frac{2}{R_b C_d} & 0 \\ \frac{1}{2C} & 0 & -\frac{1}{2R_L C} \end{bmatrix} \text{ and } B_t = \begin{bmatrix} 0 \\ \frac{2V_b}{R_b C_d} \\ -\frac{v_s}{2R_L C} \end{bmatrix}. \tag{3.9}$$

Figure 3.5 shows the two independent circuits associated with the d and t voltages and currents. These will be referred to as the d and t circuits. It is important to note that the voltages and currents of the two-level series-stacked converter are balanced when v_d and i_d are both zero. For this reason the d circuit is of particular interest, as its dynamic behavior determines the voltage and current balancing properties of the two-level series-stacked converter. Since the

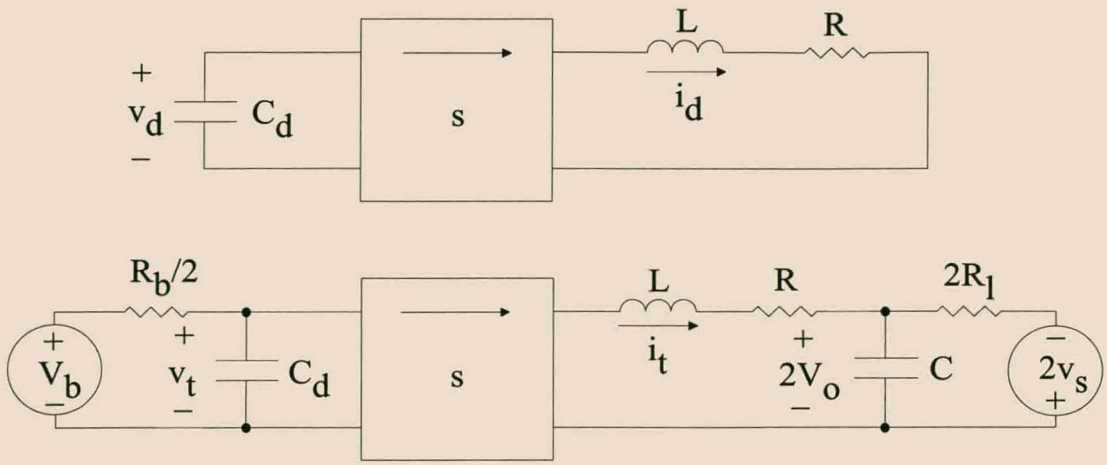


Figure 3.5: Ordinary switching d and t circuits.

d and t circuits are independent, voltage or current unbalance in the series-stacked converter does not affect the output voltage v_o in any way.

As a first step in the detailed analysis of the d circuit, Liapunov's theorem is used to prove its stability. The *equilibrium points* of 3.6 are defined as those values of x_d for which $\dot{x}_d = 0$. As mentioned earlier it is assumed that the converter is switching and that it does not remain in the zero state ($s = 0$) indefinitely. Hence it follows from 3.6 that $\dot{x}_d = 0$, for more than one switching cycle, if and only if $x_d = 0$. This shows that the only equilibrium point of 3.6 occurs where the voltages and currents of the series-stacked converter are balanced.

The stored energy W_d in the d circuit is given by

$$W_d = \frac{1}{2}C_d v_d^2 + \frac{1}{2}Li_d^2. \tag{3.10}$$

The rate of change in stored energy $\frac{dW_d}{dt}$ is equal to the power dissipated in resistor R and is given by

$$\frac{dW_d}{dt} = -i_d^2 R. \tag{3.11}$$

Furthermore, W_d satisfies the following two properties, which implies that W_d is a Liapunov function (see [7], p. 193):

1. $W_d = 0$ if $x_d = 0$ and $W_d > 0$ if $x_d \neq 0$.
2. $\frac{dW_d}{dt} \leq 0$ for all values of x_d.

Essentially these two properties state that the stored energy in the d circuit will be dissipated in resistor R. In the process the d circuit will return to the equilibrium point $x_d = 0$, of zero stored energy. This can be proven formally by making use of Liapunov's theorem ([7], p. 193) which states that, since W_d is a Liapunov function, the equilibrium point $x_d = 0$ of 3.6 is asymptotically stable. The following two conclusions can be made:

1. As long as the same switching functions are applied to both full-bridge converters of the two-level series-stacked converter, the DC-bus voltages and inductor currents will balance over time. The balancing mechanism is not influenced by the load or supply conditions and is governed by the losses in the d circuit.

2. The dynamics of the balancing process depend on the RMS value of the d circuit inductor current i_d. The larger the RMS value of i_d, the faster the system will rebalance after a perturbation. Current i_d can be separated into two components, namely a 'ripple current component', which depends highly on the switching frequency and a 'low frequency' component that depends on v_d and the reference signal. At lower switching frequencies the 'ripple current' component plays a significant role, resulting in faster rebalancing.

Having determined that the system is stable, the next step is to investigate the dynamics of the balancing process. For the remainder of this section the following assumptions are made:

1. A periodic reference signal (modulating function) $f_r(t)$ satisfying $-1 \leq f_r(t) \leq 1$ and of period T_r (and frequency $\omega_r = \frac{2\pi}{T_r}$) is applied to the pulse width modulator of the series-stacked converter.

2. The sequence of gating pulses is also periodic, with period T_r. More specifically, it is assumed that the interval $[0, T_r]$ can be divided into N sub-intervals $[t_0, t_1, t_2, \ldots, t_N]$, with $t_0 = 0$ and $t_N = T_r$. The value of the switching function s during the sub-interval $[t_{n-1}, t_n]$ is denoted by s_n.

3. Finally it is assumed that at high switching frequencies

$$\int_0^t s(\xi)\, d\xi \approx \int_0^t f_r(\xi)\, d\xi \tag{3.12}$$

and that

$$\int_0^{T_r} f_r(\xi)\, d\xi = 0. \tag{3.13}$$

It is thus assumed that the low-pass-filtered versions of the reference signal and switching function are equal, and that the reference signal has no DC-component.

In the remainder of this section the theory of systems of linear differential equations is applied to study the dynamic properties of the d circuit. The theory of systems of linear differential equations can be found in a number of textbooks (for instance [7], [8], [5] and [3]). Only a limited number of authors treat the theory in a general enough context to include switched circuits. The most general theory can be found in [8]. Under the assumptions above, the systems of differential equations that are studied have periodic coefficients and can be studied by making use of Floquet theory. Some of the results from Floquet theory (see [8], Chapter 8, [3], p. 95 and [5], p. 60) will be used in the process of analyzing the behavior of the d circuit.

The first step in the analysis is to apply one of the fundamental theorems of linear systems of differential equations with constant coefficients. If $x_d = x_{d_0}$ at time $t = 0$, then by applying [7], p. 90 it follows that

$$x_d = e^{A_d(s_1)t} x_{d_0} \tag{3.14}$$

for $0 \leq t < t_1$. By applying this theorem repeatedly, it follows that in general

$$x_d(t) = \Phi(t) x_{d_0}, \tag{3.15}$$

where

$$\Phi(t) = e^{A_d(s_n)t} e^{A_d(s_{n-1})t_{n-1}} \cdots e^{A_d(s_1)t_1}, \tag{3.16}$$

for $t_{n-1} \leq t < t_n$. Matrix $\Phi(t)$ is called the *fundamental matrix* of the d circuit and contains all the information to calculate the solution of 3.6 for any initial condition. Of particular importance is the matrix

$$M = \Phi(T_r) = e^{A_d(s_N)t_N} e^{A_d(s_{N-1})t_{N-1}} \cdots e^{A_d(s_1)t_1}, \tag{3.17}$$

since the value of x_d after one cycle of the reference function f_r is given by

$$x_d(T_r) = M x_{d_0}. \tag{3.18}$$

After k cycles of period T_r, the value of x_d is given by

$$x_d(kT_r) = M^k x_{d_0}. \tag{3.19}$$

There are two different approaches to studying the properties of M. The one approach is to calculate M numerically over one cycle of the reference signal f_r. The other approach is to study the properties of M analytically. Unfortunately no simple analytic expression for M could be found, even when the reference signal is sinusoidal in nature. However, a lot of important information can be obtained by studying the lossless case $R = 0$, which is the subject of the next section.

3.2.3.1 A special case

In this section it is assumed that resistors $R_t = R_d = 0$. Although this will not occur in practical converters, it provides important information about the general case. In a certain sense the voltage and current waveforms of the general case are just 'damped' versions of the waveforms of the lossless case. If $R = 0$, matrix $A_d(s)$ is given by

$$A_d(s) = s \begin{bmatrix} 0 & \frac{1}{L} \\ -\frac{1}{C_d} & 0 \end{bmatrix} \tag{3.20}$$

and has the following properties:

1. The different $A_d(s)$ matrices commute. This means that

$$A_d(s_i)A_d(s_j) = A_d(s_j)A_d(s_i) \tag{3.21}$$

for $s_i = -1, 0, 1$ and $s_j = -1, 0, 1$. This implies that (see [7], p. 85)

$$e^{A_d(s_i)t_i}e^{A_d(s_j)t_j} = e^{A_d(s_i)t_i + A_d(s_j)t_j}. \tag{3.22}$$

2. Matrix $e^{A_d(s)t}$ can be written in the form (see [7], p. 84, property (b))

$$e^{A_d(s)t} = P_1 e^{js\beta t} + P_2 e^{-js\beta t}, \tag{3.23}$$

where $\beta = \frac{1}{\sqrt{LC_d}}$,

$$P_1 = \begin{bmatrix} \frac{1}{2} & -\frac{j}{2}\sqrt{\frac{C_d}{L}} \\ \frac{j}{2}\sqrt{\frac{L}{C_d}} & \frac{1}{2} \end{bmatrix} \quad \text{and} \quad P_2 = \begin{bmatrix} \frac{1}{2} & \frac{j}{2}\sqrt{\frac{C_d}{L}} \\ -\frac{j}{2}\sqrt{\frac{L}{C_d}} & \frac{1}{2} \end{bmatrix}. \tag{3.24}$$

Based on these two properties, equation 3.15 for $t_{i-1} \leq t < t_i$ can in this case be rewritten as

$$x_d = \Phi(t)x_{d_0} = e^{A_d(s_n)t + A_d(s_{n-1})t_{n-1} + \cdots + A_d(s_1)t_1}x_{d_0}, \tag{3.25}$$

and M is given by

$$M = e^{A_d(s_N)t_N + A_d(s_{N-1})t_{N-1} + \cdots + A_d(s_1)t_1}. \tag{3.26}$$

From equation 3.20, 3.12 and 3.23 $\Phi(t)$ can be approximated by

$$\begin{aligned} \Phi(t) &= e^{(s_n t + s_{n-1}t_{n-1} + \cdots + s_1 t_1)A_d} && (3.27) \\ &\approx e^{\left(\int_0^t f_r(\xi)\,d\xi\right)A_d} && (3.28) \\ &= \left(P_1 e^{j\beta I_c(t)} + P_2 e^{-j\beta I_c(t)}\right) \\ &= \begin{bmatrix} \cos(\beta I_c(t)) & \sqrt{\frac{C_d}{L}}\sin(\beta I_c(t)) \\ -\sqrt{\frac{L}{C_d}}\sin(\beta I_c(t)) & \cos(\beta I_c(t)) \end{bmatrix}, && (3.29) \end{aligned}$$

where $I_c(t) = \int_0^t f_r(\xi)\,d\xi$. In particular, since $\int_0^{T_r} f_r(\xi)\,d\xi = 0$, it follows that

$$M = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}. \tag{3.30}$$

This implies that $x_d(t)$ is periodic with period T_r. As expected, it also shows that the series-stacked converter will not rebalance if $R = 0$.

A number of important conclusions about the behavior of x_d can be made in the lossless case:

1. In most practical systems the value of $\sqrt{\frac{L}{C_d}}$ is significantly less than 1 Ω. Hence the initial current i_{d_0} has relatively little influence on the behavior of v_d.

2. Of special interest is the case where $i_{d_0} = 0$ and a sinusoidal reference function of the form $f_r(t) = A\cos(\omega_r t)$ is applied to the converter. From the definition of $I_c(t)$,

$$\begin{aligned} I_c(t) &= \int_0^t A\cos(\omega_r \xi)\, d\xi \\ &= \frac{A}{\omega_r}(\sin(\omega_r t)). \end{aligned} \tag{3.31}$$

It follows from 3.29 that

$$i_d = v_{d_0}\sqrt{\frac{C_d}{L}}\sin\left(\frac{A\beta}{\omega_r}\sin(\omega_r t)\right) \tag{3.32}$$

and

$$v_d = v_{d_0}\cos\left(\frac{A\beta}{\omega_r}\sin(\omega_r t)\right). \tag{3.33}$$

Note that the argument of the cosine function in 3.33 varies between

$$-\frac{A\beta}{\omega_r} \leq \frac{A\beta}{\omega_r}\sin(\omega_r t) \leq \frac{A\beta}{\omega_r}. \tag{3.34}$$

This implies that v_d will not assume the full range of values $-v_{d_0} \leq v_d \leq v_{d_0}$ if and only if $\frac{A\beta}{\omega_r} \leq \pi$. Rewriting this inequality by making use of the definition of β results in

$$C_d \geq \frac{A^2}{L\omega_r^2\pi^2}. \tag{3.35}$$

If $A = 1$, then

$$C_d \geq \frac{1}{L\omega_r^2\pi^2}. \tag{3.36}$$

This introduces an important design guideline. It states that in order to limit the maximum variation in DC-bus voltage, with a sinusoidal reference signal f_r, the value of C_d must be chosen greater than $\frac{1}{L\omega_r^2\pi^2}$.

3. If the value of C_d is significantly larger than that given by equation 3.36, then $\beta I_c(t) << 1$ for $t \geq 0$. In this case

$$i_d \approx v_{d_0}\sqrt{\frac{C_d}{L}}\frac{A\beta}{\omega_r}\sin(\omega_r t) \tag{3.37}$$

and

$$v_d = v_{d_0}\cos(\beta I_c(t)) \approx v_{d_0}\left(1 - \frac{(\beta I_c(t))^2}{2}\right). \tag{3.38}$$

Example 3.1

In this example the d circuit voltages and currents of a lossless two-level series-stacked converter are studied for different reference signals. Table 3.1 gives the parameters used in the simulation. The switching frequency is assumed to be high enough that equation 3.12 holds.

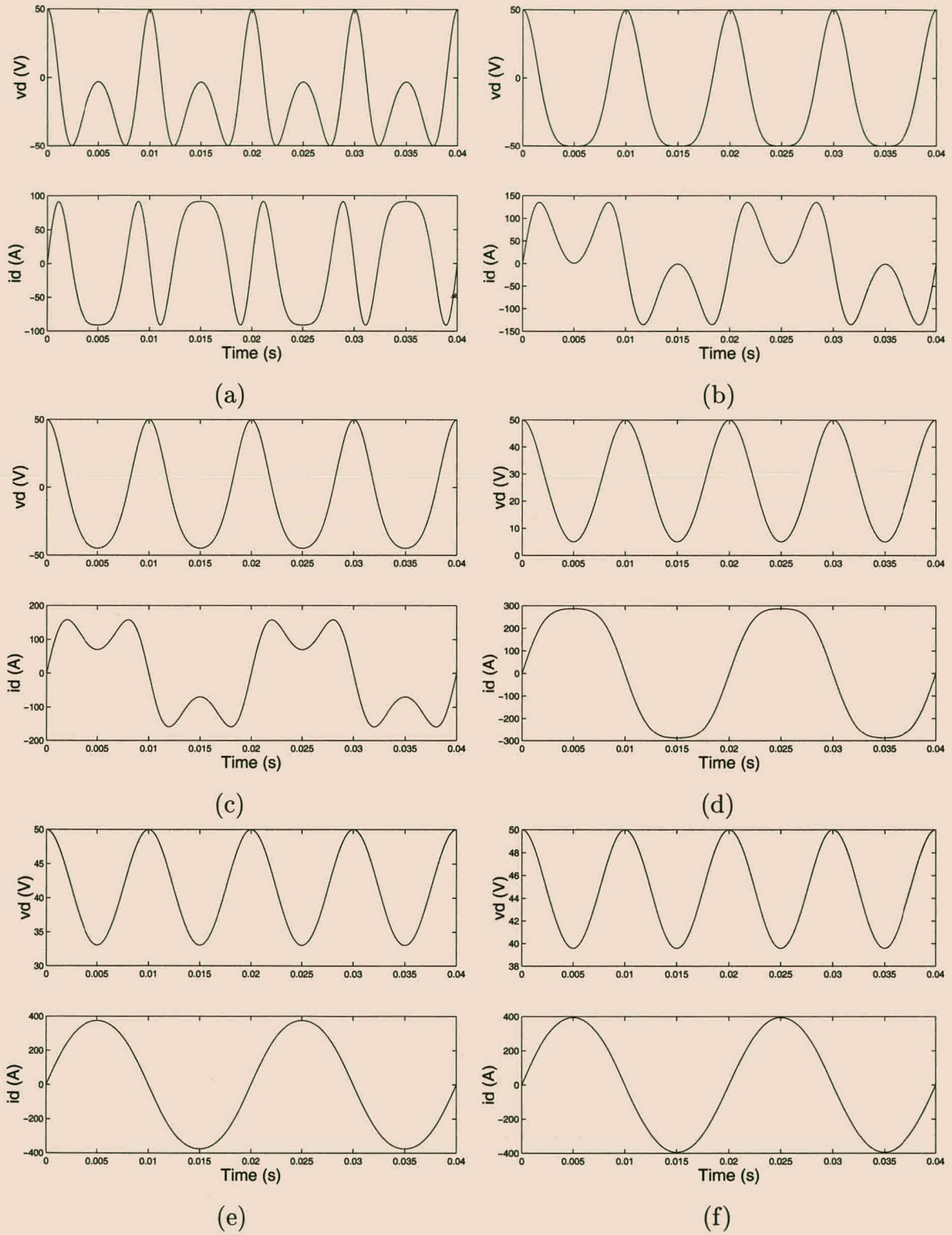


Figure 3.6: Voltage v_d and current i_d for the lossless two-level series-stacked converter. Case (a) $C_d = 1$ mF; (b) $C_d = 2.2$ mF; (c) $C_d = 3$ mF; (d) $C_d = 10$ mF; (e) $C_d = 30$ mF; (f) $C_d = 50$ mF.

Parameter	Symbol	Value
Filter Inductance	L	300 μH
Initial Inductor Current	i_{d_0}	0 A
Initial Capacitor Voltage	v_{d_0}	50 V

Table 3.1: Parameters of two-level lossless series-stacked converter.

1. In the first part of the example a sinusoidal reference signal

$$f_r(t) = 0.8\cos(2\pi \cdot 50t) \tag{3.39}$$

is applied to the converter. In this case

$$I_c(t) = \frac{0.8}{2\pi \cdot 50}\sin(2\pi \cdot 50t). \tag{3.40}$$

Figure 3.6 shows voltage v_d and current i_d for $C_d = 1$ mF, $C_d = 2.2$ mF, $C_d = 3$ mF, $C_d = 10$ mF, $C_d = 30$ mF and $C_d = 50$ mF. According to equation 3.36 values of C_d greater than 2.2 mF will lead to a reduction of the peak to peak magnitude of the oscillations of v_d. This can also be observed from results. For large values of C_d the oscillation in the DC-bus voltage becomes squared co-sinusoidal (as mentioned in remark 3 above), while current i_d becomes sinusoidal with a frequency of 50 Hz. The magnitude of i_d increases as C_d increases.

2. In this case a non-sinusoidal reference signal f_r of the form

$$f_r(t) = 0.5\cos(2\pi \cdot 50t) + 0.3\cos(2\pi \cdot 250t) + 0.1\cos(2\pi \cdot 350t) \tag{3.41}$$

is used. Function $I_c(t)$ is given by

$$I_c(t) = \frac{0.5}{2\pi \cdot 50}\sin(2\pi \cdot 50t) + \frac{0.3}{2\pi \cdot 250}\sin(2\pi \cdot 250t) + \frac{0.1}{2\pi \cdot 350}\sin(2\pi \cdot 350t). \tag{3.42}$$

Values of $C_d = 1$ mF, $C_d = 3$ mF, $C_d = 30$ mF and $C_d = 50$ mF are used. Figure 3.7 shows the results. Although the harmonics of the reference signal are now reflected in v_d and i_d, the basic tendencies are the same as in the previous case.

In the general case, where R is not necessarily equal to 0, equations 3.21 and 3.22 do not hold and a simple analytic solution for x_d could not be found. However, almost all the important information about the balancing properties are contained in M and in the solutions of the lossless case. When R is small, the solutions of the lossless case give a good approximation of the basic properties of the voltage and current waveforms on a per cycle basis. The information contained in M describes the 'damping' of these waveforms over time.

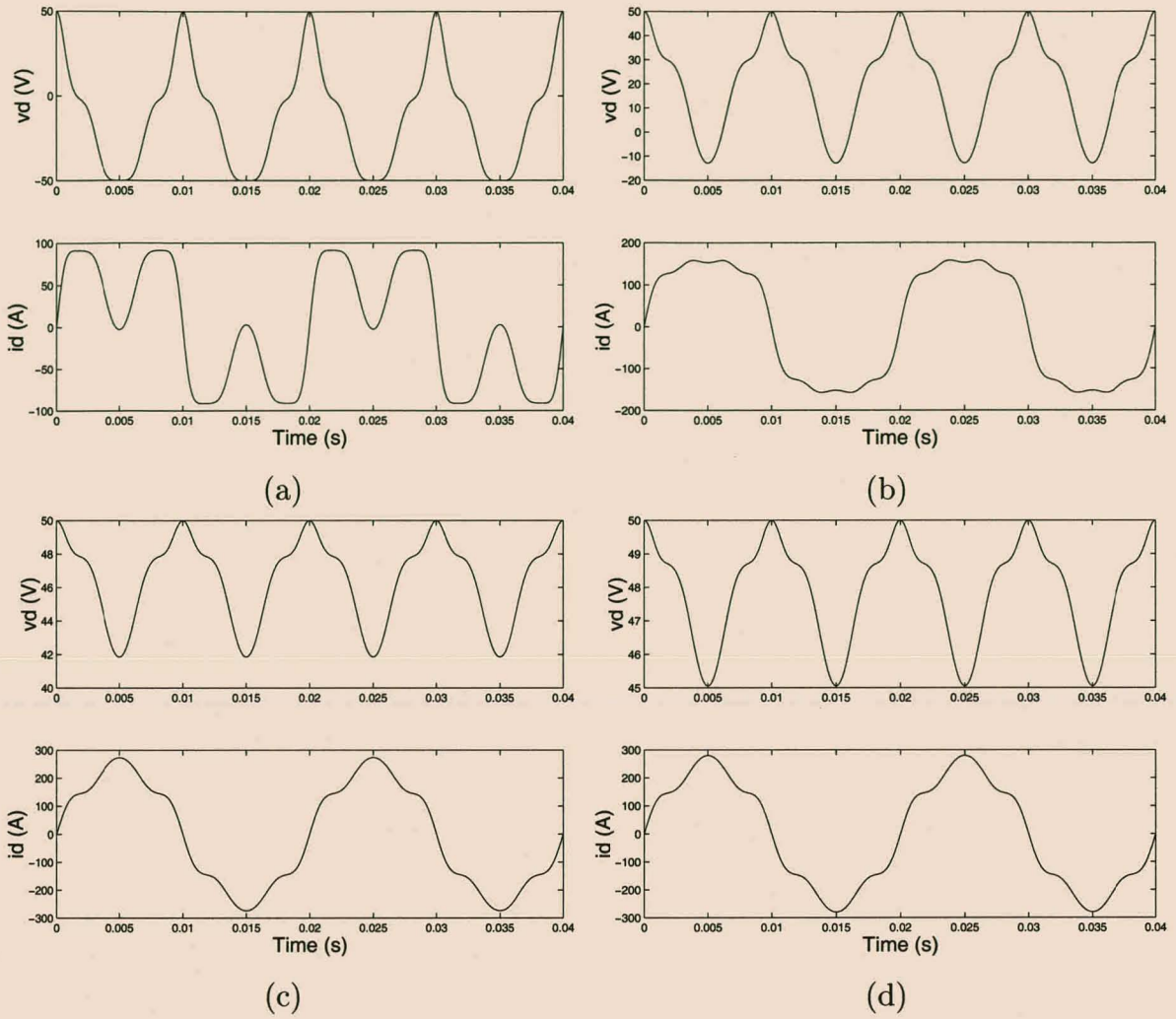


Figure 3.7: Voltage v_d and current i_d for a lossless two-level series-stacked converter with non-sinusoidal reference. Case (a) $C_d = 1$ mF; (b) $C_d = 3$ mF; (c) $C_d = 30$ mF; (d) $C_d = 50$ mF.

3.2.3.2 Quantitative analysis

In this section Floquet theory (see [8], Chapter 8) is used to study the properties of the d-circuit of the two-level series-stacked converter. Besides revealing important information about the time constants involved with the balancing process, it also provides a quick and easy way of numerically simulating the system. By calculating the fundamental matrix over one cycle of the reference function f_r, the behavior of the circuit for all $t \geq 0$ and all possible initial conditions can easily be predicted.

The fundamental matrix of the d circuit was defined in equation 3.16 as

$$\Phi(t) = e^{A_d(s_n)t} e^{A_d(s_{n-1})t_{n-1}} \cdots e^{A_d(s_1)t_1}, \tag{3.43}$$

for $t_{n-1} \leq t < t_n$. Matrix M was defined as

$$M = \Phi(T_r). \tag{3.44}$$

By [8], theorem 8.1.1, there exists a matrix C such that

$$M = e^{T_r C}. \tag{3.45}$$

Floquet's theorem ([8], theorem 8.1.1) states that $\Phi(t)$ can be factored in the form

$$\Phi(t) = P(t)e^{tC}, \tag{3.46}$$

where $P(t)$ is a periodic matrix valued function with period T_r.

Of particular importance are the real parts of the eigenvalues λ_1 and λ_2 of matrix C. These are called the *characteristic exponents* of the system. If σ_1 and σ_2 are the eigenvalues of M, then (see [8], remark 8.1.3)

$$\mathrm{Re}(\lambda_1) = \frac{\mathrm{Re}(\log \sigma_1)}{T_r} \quad \text{and} \quad \mathrm{Re}(\lambda_2) = \frac{\mathrm{Re}(\log \sigma_2)}{T_r}. \tag{3.47}$$

The two numbers

$$\tau_1 = -\frac{1}{\mathrm{Re}(\lambda_1)} = -\frac{T_r}{\mathrm{Re}(\log \sigma_1)} \quad \text{and} \quad \tau_2 = -\frac{1}{\mathrm{Re}(\lambda_2)} = -\frac{T_r}{\mathrm{Re}(\log \sigma_2)} \tag{3.48}$$

have a significant influence on the dynamics of the rebalancing process. They have the following properties:

1. τ_1 and τ_2 are the time constants of the balancing process (see [8] remarks 8.1.1 and 8.1.3), in the sense that any solution x_d of 3.6 is a linear combination of functions of the type

   $$\alpha(t)t^k e^{\lambda t}, \tag{3.49}$$

   where $0 \leq k \leq 1$ and $\lambda = \lambda_1$ or $\lambda = \lambda_2$.

2. The maximum of these two time constants $\tau := \max(\tau_1, \tau_2)$ gives a quantitative measure of the dynamics involved with the balancing process.

3. By making use of [7], theorem 9.5, it follows that

   $$\frac{1}{\tau_1} + \frac{1}{\tau_2} = -\mathrm{trace}(A_d(s)) = \frac{R}{L}. \tag{3.50}$$

   (Recall that the trace of a matrix is the sum of its diagonal elements.) This confirms the fact that the $\frac{L}{R}$ time constant plays an important role in the balancing of the system. Furthermore, it implies that $\tau \geq \frac{L}{R}$. The relation between τ_1 and τ_2 does, however, depend on the reference signal f_r. For instance, if $s = 0$ then $\tau = \infty$.

Parameter	Symbol	Value
Filter Inductance	L	300 μH
Parasitic Resistance	R	0.01 Ω
Switching Frequency	f_s	1000 Hz
Initial Inductor Current	i_{d_0}	0 A
Initial Capacitor Voltage	v_{d_0}	50 V

Table 3.2: Parameters of two-level series-stacked converter.

To calculate $\phi(t)$ and M the switching functions over one cycle of the reference signal has to be known. These can easily be calculated directly, or by using simulation software capable of generating PWM switching patterns. The approach followed in this thesis was to use a Matlab program to calculate the switching functions, $\phi(t)$, M, and τ_1 and τ_2.

The calculation of $\Phi(t)$ is relatively simple once the switching function $s(t)$ has been calculated over one cycle of the reference signal. By definition

$$\Phi(t) = e^{A_d(s_n)t} e^{A_d(s_{n-1})t_{n-1}} \cdots e^{A_d(s_1)t_1}, \tag{3.51}$$

The Matlab expm function is used to calculate the terms of the form $e^{A_d(s)t}$.

From this the following information can be obtained:

1. $\Phi(t)$ is used to simulate the exact behavior of the d circuit. The main advantage of this method is a significant decrease in simulation time. Essentially it means that simulating the system over one cycle of period T_r, for a particular reference signal f_r, provides all the information to simulate the behavior of the circuit for all $t \geq 0$ and all possible initial conditions.

2. Calculating the eigenvalues of M and subsequently $\tau = \max(\tau_1, \tau_2)$ provides the time constant of the rebalancing process for a particular reference signal f_r. One way of interpreting this time constant is to associate it with equivalent balancing resistors connected to the DC-buses of the full-bridge converters. This approach provides insight into the 'strength' of the balancing mechanism.

Example 3.2

In this example the reference signal

$$f_r(t) = 0.8\cos(2\pi \cdot 50t) \tag{3.52}$$

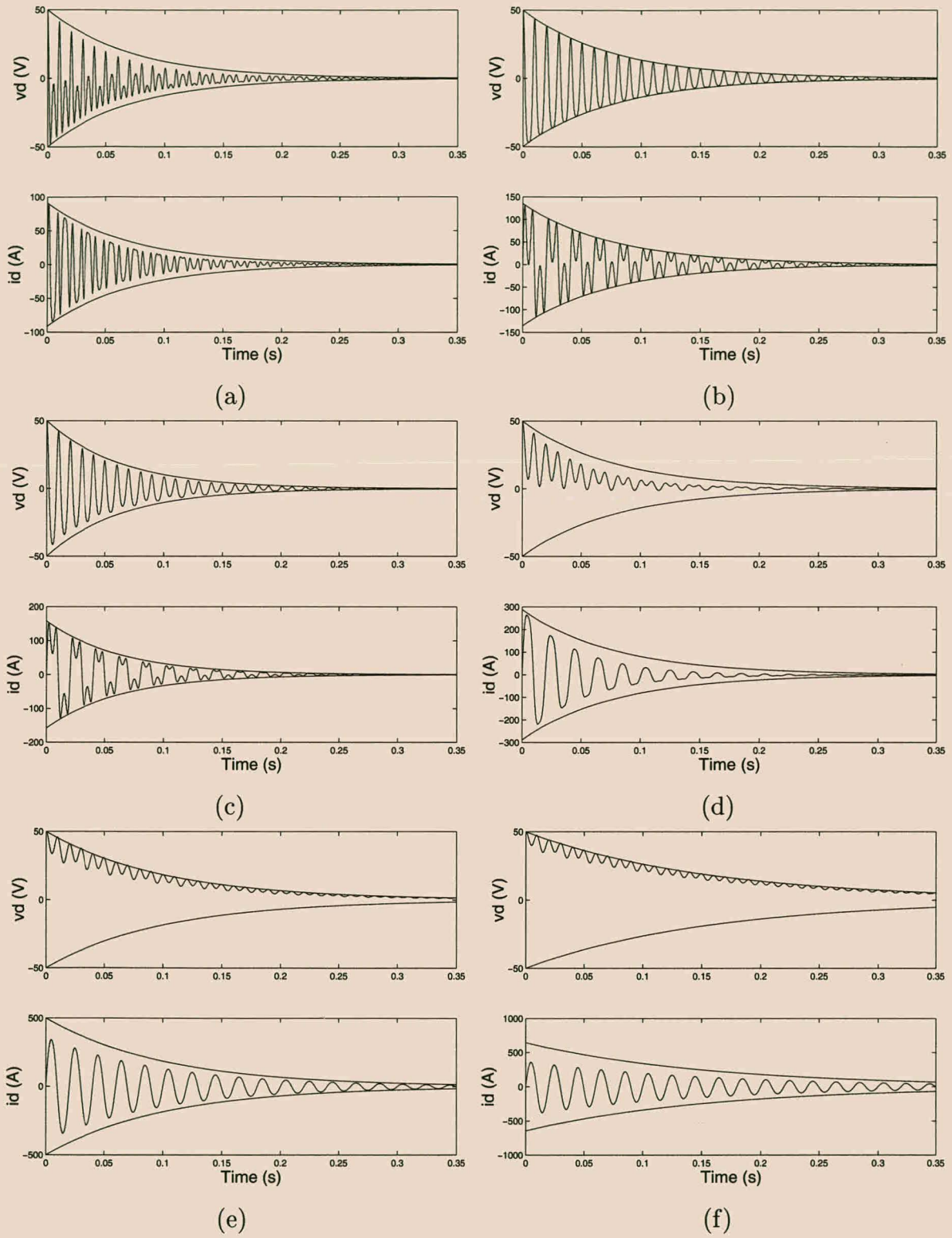


Figure 3.8: Voltage v_d and current i_d of the two-level series-stacked converter. Case (a) $C_d = 1$ mF; (b) $C_d = 2.2$ mF; (c) $C_d = 3$ mF; (d) $C_d = 10$ mF; (e) $C_d = 30$ mF; (f) $C_d = 50$ mF.

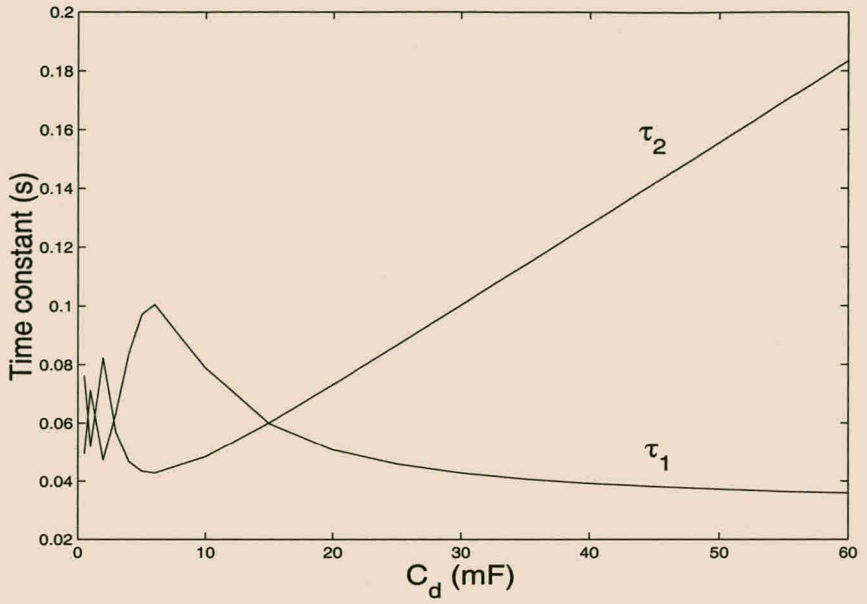


Figure 3.9: Time constants τ_1 and τ_2 as a function of C_d.

of equation 3.39 is applied to a two-level series-stacked converter with the same parameters as that of the previous example, but with the effect of the parasitic resistance R included. Table 3.2 summarizes the converter parameters. Figure 3.8 shows the results of the analysis for values of $C_d = 1$ mF, $C_d = 2.2$ mF, $C_d = 3$ mF, $C_d = 10$ mF, $C_d = 30$ mF and $C_d = 50$ mF, as in the previous example. Some of these results were checked against simulations performed on a two-level series-stacked converter with the Power System Blockset from Matlab. The results of the two methods were identical. A typical Matlab simulation ran for 8 hours, compared to 30 seconds for that based on the Floquet methods.

For each value of C_d voltage v_d and current i_d are shown. Along with v_d the envelope formed by

$$v_{d_0} e^{-\frac{t}{\tau}} \quad \text{and} \quad -v_{d_0} e^{-\frac{t}{\tau}} \tag{3.53}$$

is shown. For current i_d the envelope formed by

$$v_{d_0}\sqrt{\frac{C_d}{L}} e^{-\frac{t}{\tau}} \quad \text{and} \quad -v_{d_0}\sqrt{\frac{C_d}{L}} e^{-\frac{t}{\tau}} \tag{3.54}$$

is shown. This approximate relation between i_d and v_{d_0} is based on the observations made in the lossless case (see equation 3.29). A comparison with the results of the previous example confirms the fact that the waveforms inside the envelope correspond to those of the lossless case. It is also interesting to note that for values of C_d larger that the critical value of 2.2 mF the peak to peak value of the oscillations inside the envelope decreases as C_d increases.

Figure 3.9 shows the values of τ_1 and τ_2 as a function of C_d. Below the critical value of $C_d = 2.2$ mF these time constant shows some oscillations. For large values of C_d, τ_2 dominates and increases almost linearly with increasing C_d.

3.2.4 Interleaved switching

The main advantage of interleaved switching applied to a two-level series-stacked converter lies in the fact that it effectively doubles the switching frequency. Interleaved switching does, however, complicate the analysis of the converter and the possibility of unbalance in the DC-bus voltages under steady-state conditions arises. It will, however, be shown that as long as the converter switching frequency is chosen so as to be significantly higher than the maximum frequency content of the reference signal and supply voltage, this unbalance is not a major problem.

Throughout this section the following two assumptions are made:

1. Periodic gating signals, with frequency ω_r, are applied to the converter.
2. The supply voltage v_s is also periodic with frequency ω_r.

3.2.4.1 Harmonics of two-level unipolar PWM

In order to analyze the behavior of the two-level series-stacked converter under interleaved switching, some attention should be given to a study of the harmonics of PWM switching functions. The approach followed in this section is based on the use of double Fourier series which was originally taken from unpublished papers of W.R. Bennett by H.S. Black. Bennett originally applied the technique to study the spectra of rectified waves (see [2], Chapter 17). A number of applications of this method can be found in the literature (see, for instance, [20] and [79]).

Although the technique of interleaved switching is widely applied in power electronics, a detailed theoretical analysis of the harmonics of interleaved switching for non-sinusoidal reference signals could not be found in the literature. In [34] the harmonics of interleaved sinusoidal PWM are analyzed. Later, in [48], harmonic cancellation for non-sinusoidal reference signals is verified through simulation.

As a first step the frequency spectrum of the switching function $s(t)$ of a full-bridge converter is considered. Only unipolar switching with natural sampled double-edge modulations is analyzed. The techniques are, however, general and apply to a variety of different sampling methods and modulation strategies.

Figure 3.10 illustrates unipolar pulse width modulation as applied to a full-bridge converter. Although the figure only shows the first cycle of the reference signal $f_r(t)$, it continues periodically along the t axis for all $t \geq 0$. Function $f_c(t)$ is the triangular carrier signal with frequency ω_s. Frequency w_s is the switching frequency of each phase-arm of the series-stacked converter. It is assumed throughout the remainder of this chapter that w_s is an integer multiple of w_r. The

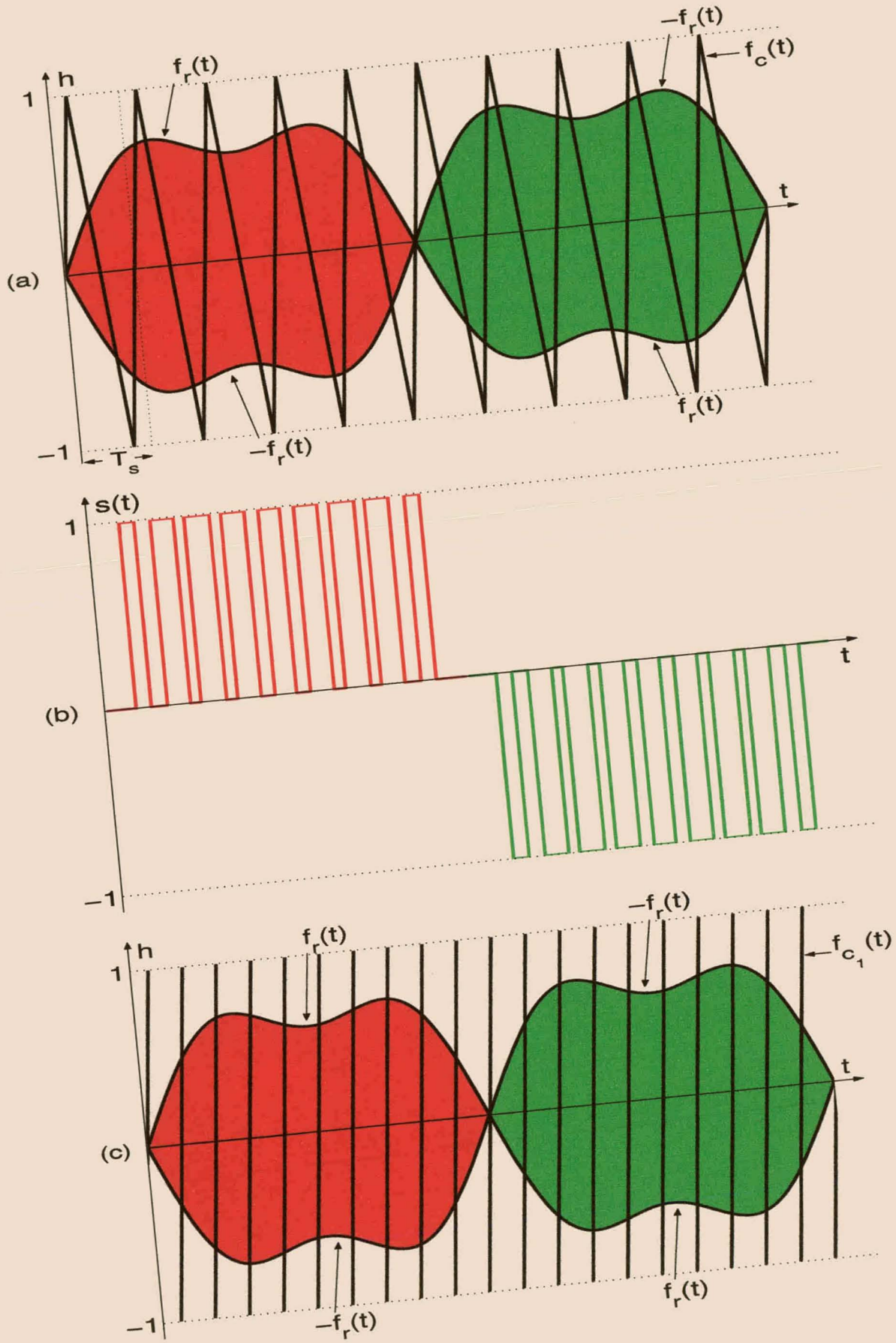


Figure 3.10: Unipolar modulation.

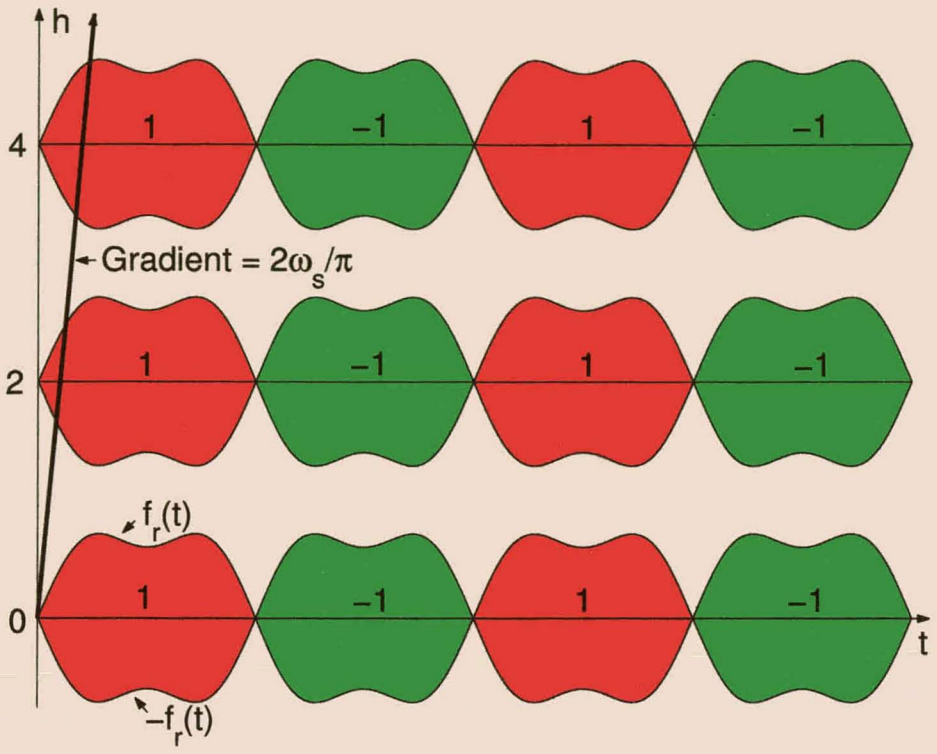


Figure 3.11: Three-dimensional representation of unipolar modulation.

theory of this section is, however, general and also applies when there is no relation between the switching frequency and that of the reference signal.

Figure 3.10(a) shows the carrier signal $f_c(t)$, $f_r(t)$ and $-f_r(t)$. The area between $f_r(t)$ and $-f_r(t)$ is colored red for $f_r(t) > 0$ and green for $f_r(t) < 0$. Figure 3.10(b) shows the resulting switching function $s(t)$, defined by

$$s(t) = \begin{cases} 1 & \text{if } -f_r(t) < f_c(t) \leq f_r(t) \\ -1 & \text{if } f_r(t) < f_c(t) \leq -f_r(t) \\ 0 & \text{elsewhere.} \end{cases} \tag{3.55}$$

It is important to note that replacing $f_c(t)$ by $-f_c(t)$ in 3.55 leads to exactly the same definition of $s(t)$. Based on this observation, $f_c(t)$ is replaced by $-f_c(t)$ during each second half of the switching period, giving rise to a new carrier signal $f_{c_1}(t)$, as shown in Figure 3.10(c). The gradient of each of the line segments of $f_{c_1}(t)$ is equal to $\frac{2\omega_s}{\pi}$. Define a function $F(h,t)$ of two variables by

$$F(h,t) = \begin{cases} 1 & \text{if } -f_r(t) < f_c(t) \leq f_r(t) \\ -1 & \text{if } f_r(t) < f_c(t) \leq -f_r(t) \\ 0 & \text{elsewhere.} \end{cases} \tag{3.56}$$

The switching function $s(t)$ can now be interpreted as the height of $F(h,t)$ when moving along the line segments mapped out by $(f_{c_1}(t), t)$ in the TOH plane.

The next step in the analysis is to extend $F(h,t)$ periodically along the t and h-axes as shown in Figure 3.11. The line segments of $f_{c_1}(t)$ line up to form straight lines in the TOH plane. Only the line passing through the origin has to be considered. Based on this observation, switching function $s(t)$ is now given by

$$s(t) = F\left(\frac{2\omega_s}{\pi}t, t\right). \tag{3.57}$$

Hence the value of $s(t)$ at time t is equal to $F(h,t)$, when moving along the line $(\frac{2\omega_s}{\pi}t, t)$ in the TOH plane.

Since $F(h,t)$ is periodic in t and h it can be presented by a two-dimensional Fourier series (see [2], p. 270), given by

$$\begin{aligned} F(h,t) &= \frac{1}{2}A_{00} + \sum_{n=1}^{\infty}(A_{0n}\cos n\omega_r t + B_{0n}\sin n\omega_r t) + \sum_{m=1}^{\infty}(A_{m0}\cos m\pi h + B_{m0}\sin m\pi h) \\ &\quad + \sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty}(A_{mn}\cos(m\pi h + n\omega_r t) + B_{mn}\sin(m\pi h + n\omega_r t)), \end{aligned} \tag{3.58}$$

where

$$A_{mn} + jB_{mn} = \frac{\omega_r}{2\pi}\int_0^{\frac{2\pi}{\omega_r}}\int_{-1}^{1} F(h,t)e^{j(m\pi h + n\omega_r t)}\,dh\,dt. \tag{3.59}$$

Substituting equation 3.57 into equation 3.58 results in

$$s(t) = F\left(\frac{2\omega_s}{\pi}t, t\right) \tag{3.60}$$

$$\begin{aligned} &= \frac{1}{2}A_{00} + \sum_{n=1}^{\infty}(A_{0n}\cos n\omega_r t + B_{0n}\sin n\omega_r t) + \sum_{m=1}^{\infty}(A_{m0}\cos 2m\omega_s t + B_{m0}\sin 2m\omega_s t) \\ &\quad + \sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty}(A_{mn}\cos(2m\omega_s t + n\omega_r t) + B_{mn}\sin(2m\omega_s t + n\omega_r t)). \end{aligned} \tag{3.61}$$

The first term $\frac{1}{2}A_{00}$ is the DC-component (average) of $F(h,t)$, which is equal to zero. The second term is the Fourier series coefficients of the reference signal $f_r(t)$ as will be shown shortly. The third term represents components at twice the switching frequency ω_s and harmonics thereof. The frequency components of the last term are harmonic side bands 'around' integer multiples of twice the switching frequency. The fact that only harmonics around multiples of twice the switching frequency occur is a result of interleaved switching, which effectively doubles the switching frequency.

The remainder of this section is devoted to studying some of the properties of the coefficients A_{mn} and B_{mn}. If $m \neq 0$ equation 3.59 can be rewritten as

$$\begin{aligned} A_{mn} + jB_{mn} &= \frac{\omega_r}{2\pi}\int_0^{\frac{2\pi}{\omega_r}}\int_{-f_r(t)}^{f_r(t)} e^{j(m\pi h + n\omega_r t)}\,dh\,dt \\ &= \frac{\omega_r}{2m\pi^2 j}\int_0^{\frac{2\pi}{\omega_r}}\left(e^{j(m\pi f_r(t) + n\omega_r t)} - e^{j(-m\pi f_r(t) + n\omega_r t)}\right)dt \\ &= \frac{\omega_r}{m\pi^2}\int_0^{\frac{2\pi}{\omega_r}} e^{jn\omega_r t}\sin(m\pi f_r(t))\,dt, \end{aligned} \tag{3.62}$$

while, if $m = 0$

$$\begin{aligned} A_{mn} + jB_{mn} &= \frac{\omega_r}{2\pi} \int_0^{\frac{2\pi}{\omega_r}} \int_{-f_r(t)}^{f_r(t)} e^{jn\omega_r t} dh\, dt \\ &= \frac{\omega_r}{\pi} \int_0^{\frac{2\pi}{\omega_r}} f_r(t) e^{jn\omega_r t}\, dt. \end{aligned} \tag{3.63}$$

A comparison with the definition of the Fourier series coefficients (see, for instance, [11], p. 740) of a periodic function proves that the second term of equation 3.61 is the Fourier series coefficients of the reference signal.

The following two properties play an important role in the analysis that follows.

1. If $m \neq 0$, then

$$|A_{mn} + jB_{mn}| = \left| \frac{\omega_r}{m\pi^2} \int_0^{\frac{2\pi}{\omega_r}} e^{jn\omega_r t} \sin(m\pi f_r(t))\, dt \right| \tag{3.64}$$

$$\leq \frac{\omega_r}{m\pi^2} \int_0^{\frac{2\pi}{\omega_r}} \left| e^{jn\omega_r t} \sin(m\pi f_r(t)) \right| dt$$

$$= \frac{\omega_r}{m\pi^2} \int_0^{\frac{2\pi}{\omega_r}} |\sin(m\pi f_r(t))|\, dt \tag{3.65}$$

$$\leq \frac{\omega_r}{m\pi^2} \cdot \frac{2\pi}{\omega_r}$$

$$= \frac{2}{m\pi}. \tag{3.66}$$

   This shows that $A_{mn} + jB_{mn} \to 0$ as $m \to \infty$.

2. If $m \neq 0$ and $n \neq 0$, then by using integration by parts

$$A_{mn} + jB_{mn} = \frac{\omega_r}{m\pi^2} \int_0^{\frac{2\pi}{\omega_r}} e^{jn\omega_r t} \sin(m\pi f_r(t))\, dt \tag{3.67}$$

$$= \frac{\omega_r}{m\pi^2} \left(\left[\frac{1}{jn\omega_r} e^{jn\omega_r t} \sin(m\pi f_r(t)) \right]_0^{\frac{2\pi}{\omega_r}} - \frac{1}{jn\omega_r} \int_0^{\frac{2\pi}{\omega_r}} e^{jn\omega_r t} \cos(m\pi f_r(t)) m\pi \frac{df_r(t)}{dt}\, dt \right). \tag{3.68}$$

   Since f_r is periodic with frequency ω_s, the first term is zero. Hence

$$|A_{mn} + jB_{mn}| = \left| \frac{1}{jmn\pi^2} \int_0^{\frac{2\pi}{\omega_r}} e^{jn\omega_r t} \cos(m\pi f_r(t)) m\pi \frac{df_r(t)}{dt}\, dt \right|$$

$$\leq \frac{1}{|n|\pi} \int_0^{\frac{2\pi}{\omega_r}} \left| \frac{df_r(t)}{dt} \right| dt. \tag{3.69}$$

   Since $\int_0^{\frac{2\pi}{\omega_r}} \left| \frac{df_r(t)}{dt} \right| dt$ is a fixed number, this shows that $|A_{mn} + jB_{mn}| \to 0$ if $n \to \infty$.

3. Combining these two properties results in

$$|A_{mn} + jB_{mn}| \leq \min \left(\frac{2}{m\pi}, \frac{1}{|n|\pi} \int_0^{\frac{2\pi}{\omega_r}} \left| \frac{df_r(t)}{dt} \right| dt \right). \tag{3.70}$$

The second property is important in the analysis that follows. Essentially it states that if the switching frequency is chosen significantly larger than the highest frequency harmonic of the reference function f_r, then the harmonics of the switching function s appear in clusters of side bands around integer multiples of $2m\omega_s$. For a particular value of $m > 0$ the cluster consists of harmonics at frequencies $n\omega_r + 2m\omega_s$, where $n = \pm 1, \pm 2, \ldots$. By property 2 above, these harmonics decrease in magnitude as $|n|$ increases. The magnitude of the harmonics is determined by $\int_0^{\frac{2\pi}{\omega_r}} \left|\frac{df_r(t)}{dt}\right| dt$. If the value of this integral is small, the side band harmonics of a particular cluster are quickly attenuated as $|n|$ increases and do not penetrate its surrounding clusters. For the remainder of this chapter it will be assumed that the switching frequency is high enough that harmonics of a particular cluster do not penetrate those of a neighboring cluster.

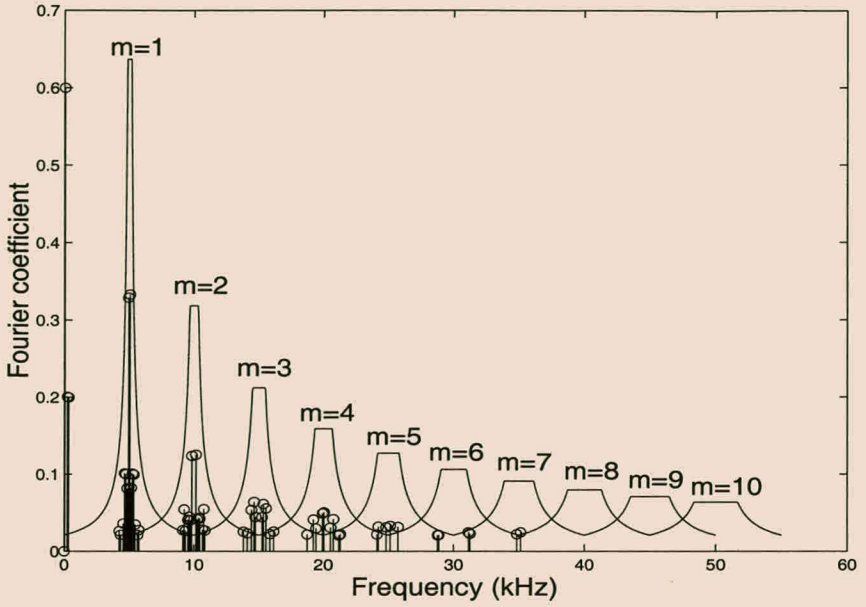


Figure 3.12: Example of the harmonics of unipolar switching.

Example 3.3

Consider the following reference function:

$$f_r(t) = 0.6\sin(2\pi \cdot 50t) + 0.2\sin(2\pi \cdot 250t) + 0.2\sin(2\pi \cdot 350t) \tag{3.71}$$

The switching frequency is 2.5 kHz. Figure 3.12 shows the magnitude of the Fourier series coefficient of $f_r(t)$ along with the estimate given by equation 3.70. These coefficients were calculated by numerically integrating equations 3.62 and 3.63. Only coefficients of magnitude greater than or equal to 0.02 are shown. As predicted by the theory the harmonics are clustered around multiples of twice the switching frequency.

3.2.4.2 Harmonics of interleaved switching

Now consider a two-level series-stacked converter under interleaved switching with s_1 the switching function of converter one and s_2 the switching function of converter two. Since unipolar switching effectively doubles the switching frequency, the carrier signals of the two converters differ by $\frac{\pi}{2}$ radians. Suppose that the carrier signal of converter two lags that of converter 1 by $\frac{\pi}{2}$ radians. The same arguments as applied in the previous section result in the following two lines in the TOH-plane

$$\left(\frac{2\omega_s}{\pi}t, t\right) \quad \text{and} \quad \left(\frac{2\omega_s}{\pi}t - 1, t\right) \tag{3.72}$$

to generate s_1 and s_2, respectively. These two lines are shown in Figure 3.13 and it follows that

$$s_1(t) = F\left(\frac{2\omega_s}{\pi}t, t\right) \quad \text{and} \quad s_2(t) = F\left(\frac{2\omega_s}{\pi}t - 1, t\right). \tag{3.73}$$

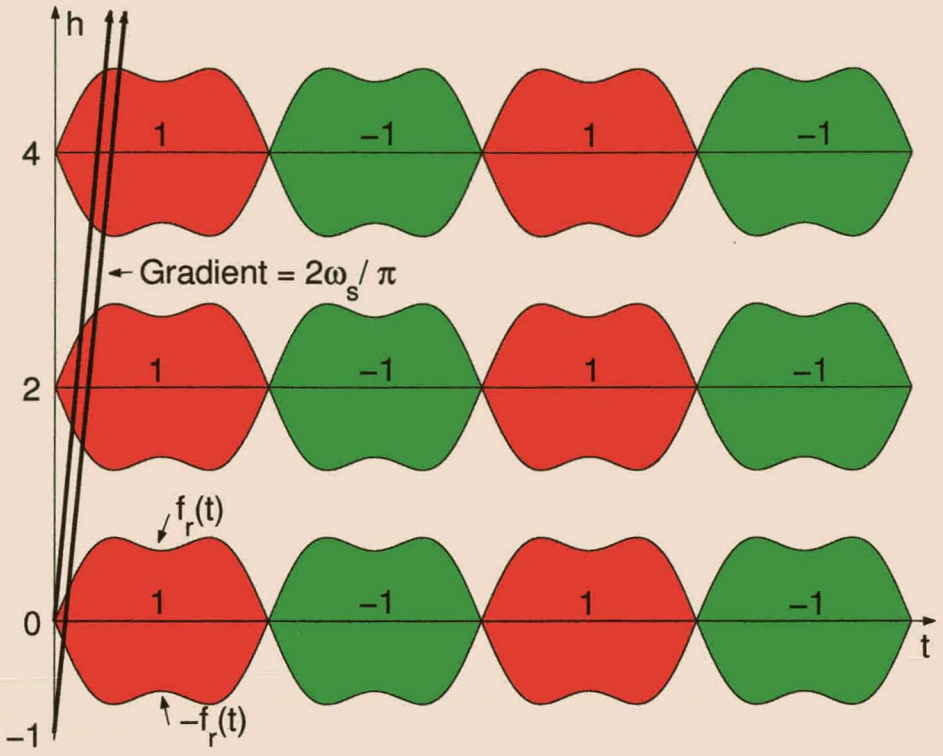


Figure 3.13: Interleaved switching with unipolar modulation.

Substituting these two equations into equation 3.58, results in

$$\begin{aligned} s_1(t) &= \frac{1}{2}A_{00} + \sum_{n=1}^{\infty}(A_{0n}\cos n\omega_r t + B_{0n}\sin n\omega_r t) + \sum_{m=1}^{\infty}(A_{m0}\cos 2m\omega_s t + B_{m0}\sin 2m\omega_s t) \\ &\quad + \sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty}(A_{mn}\cos(2m\omega_s t + n\omega_r t) + B_{mn}\sin(2m\omega_s t + n\omega_r t))\,. \end{aligned} \tag{3.74}$$

and

$$\begin{aligned} s_2(t) &= \frac{1}{2}A_{00} + \sum_{n=1}^{\infty}(A_{0n}\cos n\omega_r t + B_{0n}\sin n\omega_r t) \\ &\quad + \sum_{m=1}^{\infty}(A_{m0}\cos(2m\omega_s t - m\pi) + B_{m0}\sin(2m\omega_s t - m\pi)) \\ &\quad + \sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty}(A_{mn}\cos(2m\omega_s t - m\pi + n\omega_r t) + B_{mn}\sin(2m\omega_s t - m\pi + n\omega_r t)) \end{aligned} \tag{3.75}$$

Attention should be given to the third and fourth terms of these expressions for $s_1(t)$ and $s_2(t)$. Note that

$$\cos(2m\omega_s t - m\pi + n\omega_r t) = \begin{cases} \cos(2m\omega_s t + n\omega_r t) & \text{if } m \text{ is even} \\ -\cos(2m\omega_s t + n\omega_r t) & \text{if } m \text{ is odd} \end{cases} \tag{3.76}$$

and

$$\sin(2m\omega_s t - m\pi + n\omega_r t) = \begin{cases} \sin(2m\omega_s t + n\omega_r t) & \text{if } m \text{ is even} \\ -\sin(2m\omega_s t + n\omega_r t) & \text{if } m \text{ is odd} \end{cases}\,. \tag{3.77}$$

This shows that the Fourier series coefficients of s_1 and s_2 are equal in magnitude for all possible values of m. However, they are equal in phase around even multiples of twice the switching frequency, but differ by π radians in phase around odd multiples of twice the switching frequency. The following conclusions can be made:

1. Function $s_t = \frac{s_1+s_2}{2}$ contains harmonics around even multiples of twice the switching frequency, while the harmonics around odd multiples of the switching frequency cancel out. The non-zero harmonics are equal in magnitude and phase to those of s_1 around even multiples of twice the switching frequency. s_t also contains the frequency content of the reference signal f_r.

2. Function $s_d = \frac{s_1-s_2}{2}$ contains harmonics around odd multiples of twice the switching frequency, while the harmonics around even multiples of twice the switching frequency cancel out. In this case the non-zero harmonics are equal in phase and magnitude to those of s_1 around odd multiples of twice the switching frequency.

3. Based on the previous two properties, it follows that

$$|S_t(\omega)||S_d(\omega)| \approx 0. \tag{3.78}$$

   This property will play an important role in the following sections.

Example 3.4

In this example the reference signal

$$f_r(t) = 0.6\sin(2\pi \cdot 50t) + 0.2\sin(2\pi \cdot 250t) + 0.2\sin(2\pi \cdot 350t) \tag{3.79}$$

of equation 3.71 is again considered. The switching frequency is 2.5 kHz.

The Fourier series coefficients of s_1, s_t and s_d are shown in Figure 3.14. As predicted by the theory the frequency domain representation of s_t contains the Fourier series coefficients of s_1 around even multiples of twice the switching frequency. The Fourier series representation of s_d consists of the coefficients of s_1 around odd multiples of twice the switching frequency. It is also evident that $|S_t(\omega)||S_d(\omega)| \approx 0$.

3.2.4.3 Qualitative analysis

In this section the effects of interleaved switching on the balancing mechanisms of a two-level stacked converter are discussed.

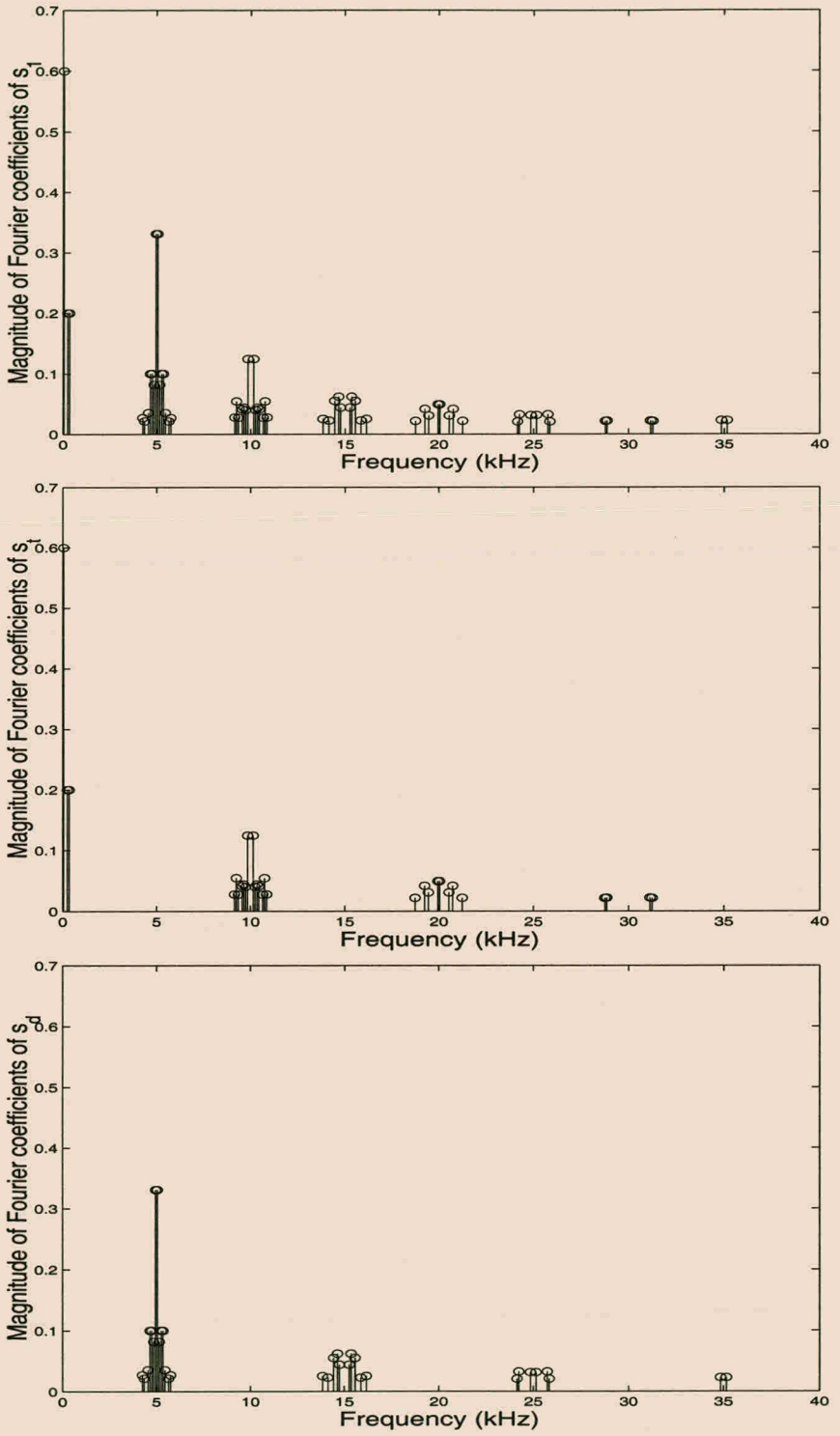


Figure 3.14: Harmonics of interleaved unipolar modulation.

As mentioned earlier, no simple analytic solution describing the behavior of the two-level series-stacked converter could be found and the problem becomes even more involved when applying interleaved switching. Although the precise behavior can only be determined through numerical simulation, a great deal of insight can be obtained by studying the balancing mechanisms for some special cases. Unlike in the case of ordinary switching, the d and t circuits can no longer be uncoupled when interleaved switching is used.

As mentioned in the previous section, for the remainder of this chapter it will be assumed that the switching frequency is high enough so that harmonics of a particular cluster do not penetrate those of a neighboring cluster.

For convenience equation 3.5 is rewritten as

$$\dot{x} = Ax + B, \tag{3.80}$$

where

$$x = \begin{bmatrix} i_d \\ v_d \\ i_t \\ v_t \\ v_o \end{bmatrix}, \quad A = \begin{bmatrix} -\frac{R}{L} & \frac{s_t}{L} & 0 & \frac{s_d}{L} & 0 \\ -\frac{s_t}{C_d} & 0 & -\frac{s_d}{C_d} & 0 & 0 \\ 0 & \frac{s_d}{L} & -\frac{R}{L} & \frac{s_t}{L} & -\frac{2}{L} \\ -\frac{s_d}{C_d} & 0 & -\frac{s_t}{C_d} & -\frac{2}{R_b C_d} & 0 \\ 0 & 0 & \frac{1}{2C} & 0 & -\frac{1}{2R_l C} \end{bmatrix} \quad \text{and} \quad B = \begin{bmatrix} 0 \\ 0 \\ 0 \\ \frac{2V_b}{R_b C_d} \\ -\frac{v_s}{2R_l C} \end{bmatrix}. \tag{3.81}$$

The equation

$$\dot{x} = Ax \tag{3.82}$$

is referred to as the homogeneous part of equation 3.80.

As a first step it is shown that the balancing properties of the two-level series-stacked converter under interleaved switching is essentially the same as that under ordinary switching, at relatively high switching frequencies.

First consider the homogeneous part of 3.80. The behavior of the circuit over one switching period $[NT_s, (N+1)T_s]$ is studied. Suppose that the converter assumes K different switching states during this period. Hence switching period $[NT_s, (N+1)T_s]$ can be divided into K sub-intervals $(t_0, t_1, \ldots, t_K)$ with $s(t) = s_i$ for $t_{i-1} \leq t < t_i$. In this case $s(t)$ is a vector consisting of switching functions s_t and s_d, given by

$$s(t) = \begin{bmatrix} s_t(t) \\ s_d(t) \end{bmatrix}. \tag{3.83}$$

By applying the same techniques as in section 3.2.3, vector x at the end of the switching period is given by

$$x((N+1)T_s) = e^{A(s_K)t_K} e^{A(s_{K-1})t_{K-1}} \cdots e^{A(s_1)t_1} x(NT_s). \tag{3.84}$$

Expanding the exponential terms results in

$$\begin{aligned} x((N+1)T_s) &= \left(1 + A(s_K)t_K + \frac{(A(s_K)t_K)^2}{2!} + \cdots\right) \cdots \\ &\left(1 + A(s_{K-1})t_{K-1} + \frac{(A(s_{K-1})t_{K-1})^2}{2!} + \cdots\right) \\ &\left(1 + A(s_1)t_1 + \frac{(A(s_1)t_1)^2}{2!} + \cdots\right) x(NT_s). \end{aligned} \tag{3.85}$$

At high switching frequencies the switching period T_s is small. Hence, multiplying out these terms and ignoring all second- and higher-order terms of time results in

$$x((N+1)T_s) = (1 + A(s_K)t_K + A(s_{K-1})t_{K-1} + \cdots + A(s_1)t_1)\, x(NT_s). \tag{3.86}$$

Furthermore, at high switching frequencies the reference signal $f_r(t)$ can be taken as constant over one switching period with $f_r(t) = f_r(NT_s)$, for $NT_s \leq t \leq (N+1)T_s$. Hence the average value of s_t taken over one switching period is equal to $f_r(NT_s)$ while the average value of s_d is equal to zero. This is true for both ordinary and interleaved switching. Hence, substituting the definition of A (equation 3.81) in equation 3.86 results in

$$x(N+1)T_s = \left(I + T_s \begin{bmatrix} -\frac{R}{L} & \frac{f_r(NT_s)}{L} & 0 & 0 & 0 \\ -\frac{f_r(NT_s)}{C_d} & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{R}{L} & \frac{f_r(NT_s)}{L} & -\frac{2}{L} \\ 0 & 0 & -\frac{f_r(NT_s)}{C_d} & -\frac{2}{R_b C_d} & 0 \\ 0 & 0 & \frac{1}{2C} & 0 & -\frac{1}{2R_l C} \end{bmatrix}\right) x(NT_s). \tag{3.87}$$

(In this case I is the identity 5×5 matrix.) By again making use of the fact that T_s is small at high switching frequencies

$$\begin{aligned} \dot{x} &\approx \frac{1}{T_s}\left(x((N+1)T_s) - x(NT_s)\right) \\ &= \begin{bmatrix} -\frac{R}{L} & \frac{f_r(NT_s)}{L} & 0 & 0 & 0 \\ -\frac{f_r(NT_s)}{C_d} & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{R}{L} & \frac{f_r(NT_s)}{L} & -\frac{2}{L} \\ 0 & 0 & -\frac{f_r(NT_s)}{C_d} & -\frac{2}{R_b C_d} & 0 \\ 0 & 0 & \frac{1}{2C} & 0 & -\frac{1}{2R_l C} \end{bmatrix} x(NT_s). \end{aligned} \tag{3.88}$$

Hence the following system of differential equations describes the two-level series-stacked converter at high switching frequencies, independent of the particular modulation strategy:

$$\dot{x} = \begin{bmatrix} -\frac{R}{L} & \frac{f_r(t)}{L} & 0 & 0 & 0 \\ -\frac{f_r(t)}{C_d} & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{R}{L} & \frac{f_r(t)}{L} & -\frac{2}{L} \\ 0 & 0 & -\frac{f_r(t)}{C_d} & -\frac{2}{R_b C_d} & 0 \\ 0 & 0 & \frac{1}{2C} & 0 & -\frac{1}{2R_l C} \end{bmatrix} x \tag{3.89}$$

This shows that if the switching frequency is high enough so that the reference signal can be taken as constant over one switching period, equation 3.80 becomes independent of the modulation method. Hence at high switching frequencies the behavior of the system is independent of the modulation method (ordinary or interleaved switching). Based on this observation, the results obtained for ordinary switching can be applied as a first approximation when studying the behavior of the converter under interleaved switching.

Numerical integration of 3.89 yielded results that closely approximated the results obtained by simulating the operation of the two-level series-stacked converter, particularly at high switching frequencies (typically at 5 kHz and above).

The above analysis gave rise to a state-space averaging of the system. Essentially both full-bridge converters of the two-level series-stacked converter can be seen as linear amplifiers at high switching frequencies. However, the averaging technique neglects the effect of ripple currents and voltages due to switching. This gives a clue to the difference between ordinary and interleaved switching. It will soon be shown that the difference lies in the effect of the 'switching harmonics' on the system.

Some basic conclusions about the properties of the two-level series-stacked converter under interleaved switching can be made by applying the theory of systems of linear differential equations with periodic coefficients (see [8], Chapter 8) to equation 3.80. As in section 3.2.3 a Liapunov argument can be used to show that the solution of the homogeneous part of 3.80 goes to zero as time goes to infinity, for all possible initial conditions. This implies that the homogeneous part of 3.80 has no non-zero periodic solutions and it follows from [8], theorem 8.3.2 that 3.80 has a periodic solution $x_p(t)$ with frequency w_r. Furthermore, from [8], theorem 6.5.1, it follows that given any initial condition x_0 the solution of equation 3.80 is of the form

$$x(t) = \Phi(t)x_0 + x_r(t), \tag{3.90}$$

where $\Phi(t)$ is the fundamental matrix of the homogeneous part and $x_r(t)$ is the particular solution of 3.5. This is an extension of the well-known results from linear circuit theory to switched systems.

Since $\Phi(t)x_0 \to 0$ as $t \to \infty$, the steady-state solution is given by $x_r(t)$, while $\Phi(t)$ describes the transient behavior. The particular solution $x_r(t)$ is equal to the sum of the periodic solution of the system and a homogeneous solution. Since the homogeneous solution goes to zero as time goes to infinity, the particular solution is itself periodic and equal to $x_p(t)$ in the steady state.

The response of the system to a perturbation from its steady-state condition is a solution of the homogeneous part. Hence to investigate the re-balancing of the system after a perturbation, it is only necessary to consider the homogeneous part. Although the variation of parameters

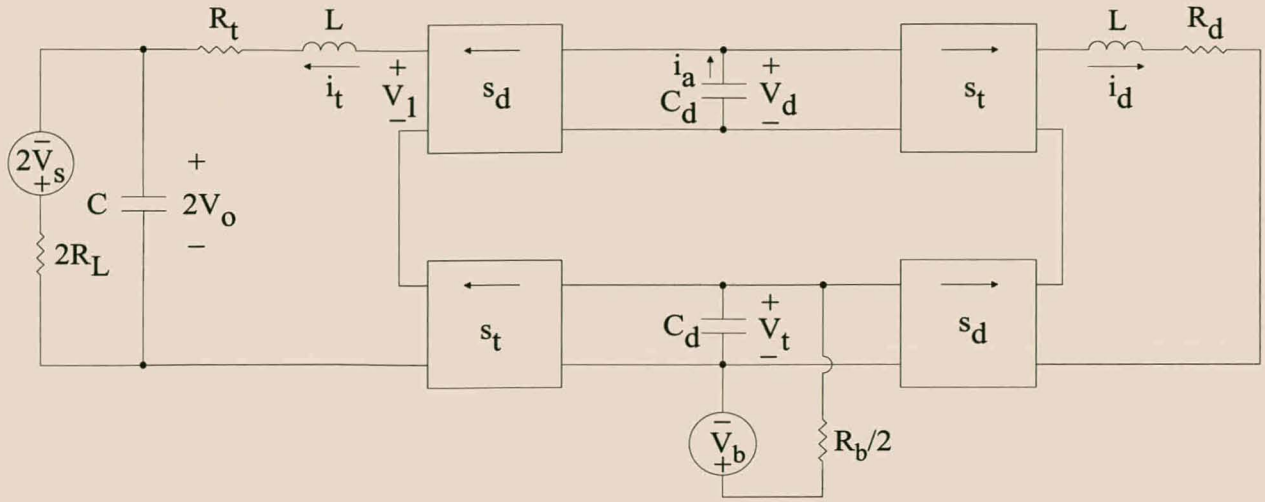


Figure 3.15: Equivalent circuit of the two-level series-stacked converter.

formula ([8], theorem 6.5.1)

$$x_r(t) = \Phi(t) \int_0^t \Phi^{-1}(\sigma) B(\sigma)\, d\sigma \tag{3.91}$$

can be used to calculate the particular solution $x_r(t)$, this proved impossible to implement analytically or numerically. By using the variation of parameters formula it is, however, possible to show that the principle of superposition can be applied to v_s and V_b. Hence the effect of these two sources on the converter can be studied separately.

Based on these considerations, the analysis of the two-level series-stacked converter under interleaved switching is divided into two sections:

1. The particular solution $x_p(t)$ is studied to obtain information about the steady-state behavior of the system.

2. The properties of the homogeneous part are studied to investigate the transient behavior, in particular the balancing mechanisms of the converter after a perturbation.

3.2.4.3.1 Steady-state analysis

It has been shown above that the steady-state solution $x_p(t)$ of 3.80 is periodic with period ω_r and hence Fourier analysis can be applied to study its properties. Throughout this section it is assumed that the DC-bus capacitor C_d is large in the sense that the two DC-bus voltages v_d and v_t can be considered as constant and that it contains only a DC-component in the steady-state with negligible high-frequency components.

By making use of the principle of superposition the effect of V_b and v_s on v_d can be studied separately. For the first part of the analysis it is assumed that the source voltage v_s is zero, while

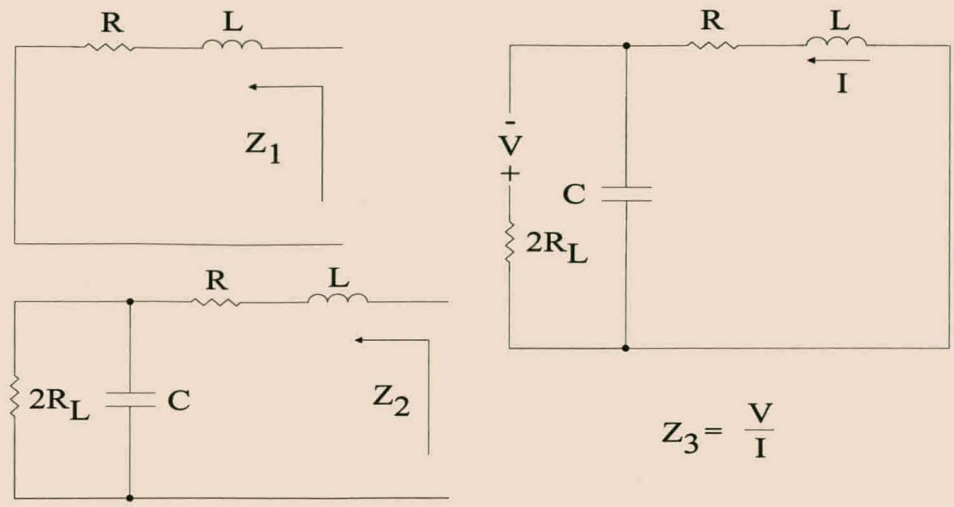


Figure 3.16: Definition of Z_1, Z_2 and Z_3 for the two-level series-stacked converter.

V_b is taken as zero for the second part. Refer to Figure 3.16 for the definition of impedances Z_1, Z_2 and Z_3 and current i_a.

Assuming that $v_s = 0$, the following relations hold in the frequency domain:

$$I_d(\omega) = \frac{V_d S_t(\omega) + V_t S_d(\omega)}{Z_1(\omega)} \tag{3.92}$$

$$I_t(\omega) = \frac{V_d S_d(\omega) + V_t S_t(\omega)}{Z_2(\omega)} \tag{3.93}$$

Since $i_a = i_d s_t + i_t s_d$, it follows that

$$\begin{aligned} I_a(\omega) &= I_d(\omega) \star S_t(\omega) + I_t(\omega) \star S_d(\omega) \\ &= V_d \left(\frac{S_t(\omega)}{Z_1(\omega)} \right) \star S_t(\omega) + V_t \left(\frac{S_d(\omega)}{Z_1(\omega)} \right) \star S_t(\omega) + \\ &\quad V_d \left(\frac{S_d(\omega)}{Z_2(\omega)} \right) \star S_d(\omega) + V_t \left(\frac{S_t(\omega)}{Z_2(\omega)} \right) \star S_d(\omega). \end{aligned} \tag{3.94}$$

($\star$ represents convolution in the frequency domain.) But in the steady-state the average value of i_a is equal to zero. Hence

$$\begin{aligned} & V_d \left(\left(\frac{S_t(\omega)}{Z_1(\omega)} \right) \star S_t(\omega) + \left(\frac{S_d(\omega)}{Z_2(\omega)} \right) \star S_d(\omega) \right) \Bigg|_{\omega=0} \\ = & - V_t \left(\left(\frac{S_d(\omega)}{Z_1(\omega)} \right) \star S_t(\omega) + \left(\frac{S_t(\omega)}{Z_2(\omega)} \right) \star S_d(\omega) \right) \Bigg|_{\omega=0}. \end{aligned} \tag{3.95}$$

Applying the definition of convolution integral and making use of the fact that both s_t and s_d are real valued results in

$$\frac{V_d}{V_t} = - \frac{\int_{-\infty}^{\infty} \left(\frac{S_d(\xi)\overline{S_t(\xi)}}{Z_1(\xi)} + \frac{S_t(\xi)\overline{S_d(\xi)}}{Z_2(\xi)} \right) d\xi}{\int_{-\infty}^{\infty} \left(\frac{|S_t(\xi)|^2}{Z_1(\xi)} + \frac{|S_d(\xi)|^2}{Z_2(\xi)} \right) d\xi}, \tag{3.96}$$

from which it follows that

$$\left|\frac{V_d}{V_t}\right| \leq \frac{\int_{-\infty}^{\infty}\left(\frac{|S_d(\xi)||S_t(\xi)|}{|Z_1(\xi)|}+\frac{|S_t(\xi)||S_d(\xi)|}{|Z_2(\xi)|}\right)d\xi}{\left|\int_{-\infty}^{\infty}\left(\frac{|S_t(\xi)|^2}{Z_1(\xi)}+\frac{|S_d(\xi)|^2}{Z_2(\xi)}\right)d\xi\right|}. \tag{3.97}$$

Under the assumption at the beginning of this section it follows that

$$\int_{-\infty}^{\infty}\left(\frac{|S_d(\xi)||S_t(\xi)|}{|Z_1(\xi)|}+\frac{|S_t(\xi)||S_d(\xi)|}{|Z_2(\xi)|}\right)d\xi << \left|\int_{-\infty}^{\infty}\left(\frac{|S_t(\xi)|^2}{Z_1(\xi)}+\frac{|S_d(\xi)|^2}{Z_2(\xi)}\right)d\xi\right|, \tag{3.98}$$

which implies that $V_d << V_t$.

In order to study the effect of the supply voltage on the average value of v_d assume that V_b is zero. In practical systems the bus resistance R_b is small and hence it can be assumed that $v_t = 0$. In this case

$$I_d(\omega) = \frac{V_d S_t(\omega)}{Z_1(\omega)} \tag{3.99}$$

$$I_t(\omega) = \frac{V_d S_d(\omega)}{Z_2(\omega)} + \frac{V_s(\omega)}{Z_3(\omega)}. \tag{3.100}$$

By again making use of the fact that $i_a = i_d s_t + i_t s_d$, it follows that

$$\begin{aligned} I_a(\omega) &= I_d(\omega) \star S_t(\omega) + I_t(\omega) \star S_d(\omega) \\ &= V_d\left(\frac{S_t(\omega)}{Z_1(\omega)}\right) \star S_t(\omega) + V_d\left(\frac{S_d(\omega)}{Z_2(\omega)}\right) \star S_d(\omega) + \left(\frac{V_s(\omega)}{Z_3(\omega)}\right) \star S_d(\omega). \end{aligned} \tag{3.101}$$

Again, from the fact that the average value of i_d is zero in the steady-state, it follows that

$$V_d\left(\left(\frac{S_t(\omega)}{Z_1(\omega)}\right) \star S_t(\omega) + \left(\frac{S_d(\omega)}{Z_2(\omega)}\right) \star S_d(\omega)\right)\Big|_{\omega=0} = -\left(\frac{V_s(\omega)}{Z_3(\omega)}\right) \star S_d(\omega)\Big|_{\omega=0}. \tag{3.102}$$

By applying the definition of the convolution of two functions and making use of the fact that s_d and s_t are real valued functions, it follows that

$$V_d = -\frac{\int_{-\infty}^{\infty}\frac{V_s(\xi)\overline{S_d(\xi)}}{Z_3(\xi)}d\xi}{\int_{-\infty}^{\infty}\left(\frac{|S_t(\xi)|^2}{Z_1(\omega)}+\frac{|S_d(\xi)|^2}{Z_2(\omega)}\right)d\xi}. \tag{3.103}$$

Hence

$$|V_d| \leq \frac{\int_{-\infty}^{\infty}\frac{|V_s(\xi)||S_d(\xi)|}{|Z_3(\xi)|}d\xi}{\left|\int_{-\infty}^{\infty}\left(\frac{|S_t(\xi)|^2}{Z_1(\omega)}+\frac{|S_d(\xi)|^2}{Z_2(\omega)}\right)d\xi\right|}. \tag{3.104}$$

Under the assumption at the beginning of this section the harmonics of s_d are concentrated around odd multiples of twice the switching frequency. Hence it is evident that

$$\int_{-\infty}^{\infty}\frac{V_s(\xi)\overline{S_d(\xi)}}{Z_3(\xi)}d\xi << \int_{-\infty}^{\infty}\left(\frac{|S_t(\xi)|^2}{Z_1(\omega)}+\frac{|S_d(\xi)|^2}{Z_2(\omega)}\right)d\xi \tag{3.105}$$

if the supply voltage v_s does not contain harmonics near odd multiples of twice the switching frequency.

To summarize, the DC-bus voltages v_1 and v_2 are balanced in the steady-state, if the following two conditions hold:

1. The switching frequency is chosen so as to be significantly higher than the highest frequency harmonic of the reference signal.

2. The supply voltage does not contain any harmonics near two times the switching frequency, or higher.

To date not a lot of attention has been devoted to non-linear loads. Many of the properties of non-linear loads can, however, be modeled by making use of the current theory. For instance, the harmonic currents drawn by non-linear loads can be modeled by adding a harmonic to the supply voltage.

3.2.4.3.2 Transient analysis

Simulations of the two-level series-stacked converter showed that it rebalanced faster under interleaved switching than under ordinary switching. In order to study the balancing properties, the solutions to the homogeneous part of 3.80 are analyzed. For this reason the voltage sources V_b and v_s are set to zero. Furthermore, since the bus resistance R_b is small in practical circuits, it is assumed that v_t is zero.

It was shown earlier that the fundamental difference between the operation of the converter when using ordinary switching as opposed to interleaved switching lies in the 'ripple' currents and voltages. As the dynamics of the balancing process are determined by the rate of decrease of the initial stored energy of the circuit, the effect of the difference in ripple currents and voltages on the loss mechanisms in the circuit is studied.

Only the case where C_d is 'large' is studied. It is thus assumed that voltage v_d can be seen as constant over a number of cycles of the reference signal f_r and is denoted by V_d. This analysis provides a great deal of insight into the losses associated with harmonic currents in the converter. The problem was also partly solved in the more general case where v_d is only assumed to be constant over one switching period. The solution is, however, mathematically involved and does not provide any significant new insight into the balancing mechanisms. For this reason it is not presented here.

The difference in the transient behavior between ordinary and interleaved switching is studied by comparing the losses in the converter in both cases.

In the case of ordinary switching $s_t = s_1$, while $s_d = 0$. By Parseval's identity the average power dissipated in resistor R_d is given by

$$\begin{aligned} P_{ord} &= \frac{R}{2\pi}\int_{-\infty}^{\infty} |I_d(\omega)|^2\, d\omega \\ &= \frac{RV_d^2}{2\pi}\int_{-\infty}^{\infty} \left|\frac{S_1(\omega)}{Z_1(\omega)}\right|^2 d\omega. \end{aligned} \tag{3.106}$$

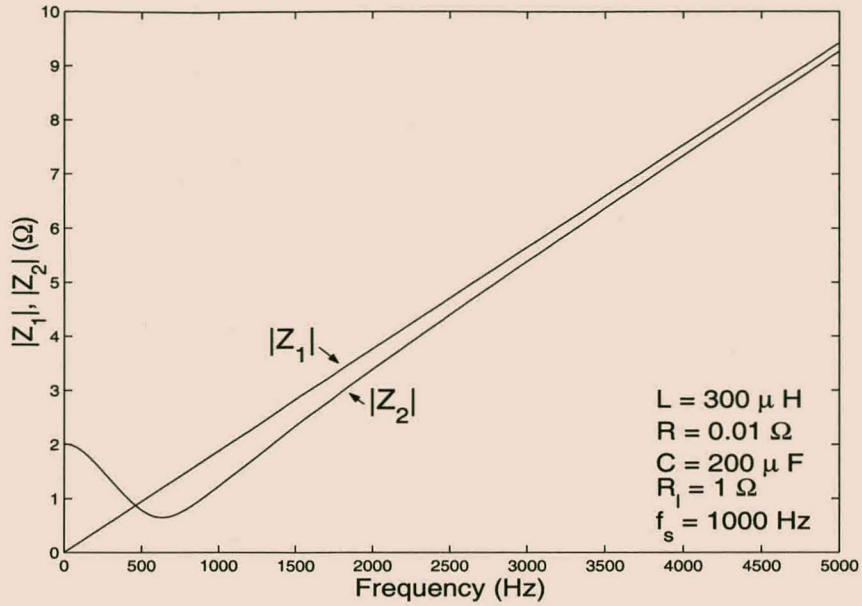


Figure 3.17: Typical graphs of $|Z_1|$ and $|Z_2|$ as functions of frequency.

When interleaved switching is applied, the losses in resistors R_d and R_t are given by

$$\begin{aligned} P_{intrl} &= \frac{R}{2\pi}\int_{-\infty}^{\infty}\left(|I_t(\omega)|^2 + |I_d(\omega)|^2\right)\,d\omega \\ &= \frac{RV_d^2}{2\pi}\int_{-\infty}^{\infty}\left(\left|\frac{S_t(\omega)}{Z_1(\omega)}\right|^2 + \left|\frac{S_d(\omega)}{Z_2(\omega)}\right|^2\right)\,d\omega. \end{aligned} \tag{3.107}$$

In practical converters the cutoff frequency of the output filter is chosen significantly lower than the converter switching frequency ω_s. Figure 3.17 shows the magnitudes of impedances Z_1 and Z_2 for a typical case, where a switching frequency of 1000 Hz was used. It is important to note that $|Z_2| \leq |Z_1|$ above the cutoff frequency. Since the harmonics of s_d are clustered around odd multiples of twice the switching frequency, we have

$$\left|\frac{S_d(\omega)}{Z_2(\omega)}\right| \geq \left|\frac{S_d(\omega)}{Z_1(\omega)}\right|. \tag{3.108}$$

This implies that

$$P_{intrl} \geq \frac{RV_d^2}{2\pi}\int_{-\infty}^{\infty}\left(\left|\frac{S_t(\omega)}{Z_1(\omega)}\right|^2 + \left|\frac{S_d(\omega)}{Z_1(\omega)}\right|^2\right)\,d\omega. \tag{3.109}$$

Furthermore, since $|S_d(\omega)||S_t(\omega)| \approx 0$, this equation can be rewritten as

$$\begin{aligned} P_{intrl} &\geq \frac{RV_d^2}{2\pi}\int_{-\infty}^{\infty}\frac{|S_t(\omega)|^2 + 2|S_t(\omega)||S_d(\omega)| + |S_d(\omega)|^2}{|Z_1(\omega)|^2}\,d\omega \\ &= \frac{RV_d^2}{2\pi}\int_{-\infty}^{\infty}\frac{\left(|S_t(\omega)| + |S_d(\omega)|\right)^2}{|Z_1(\omega)|^2}\,d\omega \\ &\geq \frac{RV_d^2}{2\pi}\int_{-\infty}^{\infty}\left|\frac{S_t(\omega) + S_d(\omega)}{Z_1(\omega)}\right|^2\,d\omega \end{aligned}$$

$$= \frac{RV_d^2}{2\pi}\int_{-\infty}^{\infty}\left|\frac{S_1(\omega)}{Z_1(\omega)}\right|^2 d\omega$$
$$= P_{ord}. \tag{3.110}$$

This argument shows that the losses due to ripple currents in R_t and R_d are in general greater with interleaved switching than with ordinary switching. Under interleaved switching the harmonics split into two, namely the harmonics of s_t and the harmonics of s_d. The essential ingredient in this argument is the fact that the impedance of the output filter Z_2 provides a lower impedance path for the harmonics of s_d. The resulting effective increase in ripple currents gives rise to increased losses, which cause the circuit to rebalance more quickly.

There are also other balancing mechanisms that play a role in rebalancing when interleaved switching is used. These losses may under certain conditions be even more significant than those studied above and include:

1. Losses in the bus resistance R_b due to ripple currents.
2. Losses in the load due to harmonics associated with s_d propagating to the load.

The influence of these mechanisms can in general only be studied through simulation, which is the subject of the next section.

3.2.4.4 Quantitative Analysis

3.2.4.4.1 Transient Analysis

In this section the Floquet techniques of section 3.2.3.2 are applied to study the transient behavior of the two-level series-stacked converter under interleaved switching. As in section 3.2.3.2 the time constant associated with the balancing process is obtained and a quick and easy method of simulating the behavior of the system is derived.

The analysis is almost identical to that of section 3.2.3.2, with a few minor modifications. The fundamental matrix $\Phi(t)$ is again defined by

$$\Phi(t) = e^{A(s_n)t}e^{A(s_{n-1})t_{n-1}}\cdots e^{A(s_1)t_1}, \tag{3.111}$$

for $t_{n-1} \leq t < t_n$. As mentioned earlier, in this case s_n is a vector containing the two switching states. Furthermore, matrix M is again defined as

$$M = \Phi(T_r). \tag{3.112}$$

Let $M = e^{T_r C}$. Then by Floquet's theorem there exists a periodic matrix valued function $P(t)$, such that

$$\Phi(t) = P(t)e^{tC}. \tag{3.113}$$

In this case C has five eigenvalues, denoted by $\lambda_1, \lambda_2, \ldots, \lambda_5$. If $\sigma_1, \sigma_2, \ldots, \sigma_5$ are the eigenvalues of M, then

$$\tau_i = -\frac{T_r}{\mathrm{Re}(\log(\sigma_i))}, \quad \text{for} \quad i = 1, \ldots, 5 \tag{3.114}$$

are the time constants associated with the system. In this case the five time constants also contain information on the load dynamics, bus bar resistance, bus capacitor dynamics, etc. It was established through simulation that in most practical converters the largest time constant is associated with the DC-bus rebalancing process. Hence

$$\tau = \max(\tau_1, \tau_2, \ldots, \tau_5) \tag{3.115}$$

is the time constant associated with the DC-bus rebalancing and provides essential information on the dynamics of the DC-bus rebalancing.

It is interesting to note that by [7], theorem 9.5

$$\frac{1}{\tau_1} + \frac{1}{\tau_2} + \cdots + \frac{1}{\tau_5} = -\mathrm{trace}(A(s)) = 2\frac{R}{L} + \frac{2}{R_b C_d} + \frac{1}{2R_l C}. \tag{3.116}$$

This confirms the fact that information about all the time constants of the system are contained in M.

Exactly the same steps as in section 3.2.3.2 are followed:

1. The switching functions s_t and s_d are first calculated over one cycle of f_r. Then $\Phi(t)$ is calculated over the same cycle by making use of equation 3.111 and the expm function of Matlab. $\Phi(t)$ is then used to simulate the behavior of the homogeneous part of the system over as many cycles as required.

2. The eigenvalues of $M = \Phi(T_r)$ and τ are then calculated.

3.2.4.4.2 Steady-state analysis

In this section a numerical method to obtain the steady-state behavior of the two-level series-stacked converter is derived. Simulations using the Power System Blockset from Matlab proved to be extremely time-consuming. The behavior of the converter typically has to be simulated over a number of seconds before it reaches its steady-state condition. Simulations using the personal edition of PSCAD V3.0 were also attempted. It was found that this package gave unreliable results in the steady-state. This resulted in simulation times from a number of hours to a few days (on a 450 MHz Pentium II processor) before meaningful results were obtained. Furthermore, to verify the stability properties of a specific design, its response to a number of different reference signals and different load conditions has to be studied. Based on these considerations, it was decided to derive a more time-effective simulation method.

To obtain the steady-state solution we start by simulating the behavior of the stacked converter over one cycle of f_r with initial condition $x(0) = x_0 = 0$. This can be done by using simulation software or by numerically integrating equation 3.80. The result is the solution $x(t)$ of 3.80 over only cycle of f_r with $x_0 = 0$.

It has been established in section 3.2.4.3 that 3.80 has a periodic solution $x_p(t)$. Hence $x(t)$ is of the form

$$x(t) = \Phi(t)x_a + x_p(t), \tag{3.117}$$

where x_a is determined by the values of $x_p(0)$ and x_0. Since $x(0) = 0$, we have

$$0 = \Phi(0)x_a + x_p(0), \tag{3.118}$$

and since $\Phi(0) = I$, it follows that $x_p(0) = -x_a$. Now consider equation 3.117 at time $t = T_r$:

$$x(T_r) = \Phi(T_r)x_a + x_p(T_r) \tag{3.119}$$

But $\Phi(T_r) = M$ and since $x_p(t)$ is periodic with period T_r, it follows that

$$x(T_r) = -Mx_p(0) + x_p(0). \tag{3.120}$$

Solving for $x_p(0)$ results in

$$x_p(0) = (I - M)^{-1}x(T_r). \tag{3.121}$$

By again making use of the fact that $x_p(0) = -x_a$, and substituting x_a back in equation 3.117, we obtain

$$x_p(t) = x(t) + \Phi(t)(I - M)^{-1}x(T_r). \tag{3.122}$$

Although this equation is of theoretical interest, it proved difficult to implement numerically. Since we know that $x_p(0)$ is the steady-state value of $x(t)$ at the start of each cycle of f_r, the steady solution can also be obtained by numerically integrating the system over one cycle of f_r, with $x_p(0)$ as initial condition.

To summarize, the steps to calculate the steady-state solution $x_p(t)$ are as follows:

1. The behavior of the system is simulated over one cycle with initial condition $x(0) = 0$. In practice this was done by numerically solving equation 3.80, using Euler's method. The solution is stored and the value of $x(T_r)$ is extracted.

2. At the same time the fundamental matrix $\Phi(t)$ is calculated by using the methods of the previous section. Vector $x_p(0)$ is then calculated by making use of equation 3.121. Using $x_p(0)$ as initial condition, equation 3.80 is then numerically solved over one cycle to obtain the steady-state solution.

Parameter	Symbol	Value
Bus Capacitance	C_d	30 mF
Filter Inductance	L	300 μH
Filter Capacitance	C	200 μF
Parasitic Resistance	R	0.01 Ω
Load Resistance	R_l	1 Ω
Bus bar Resistance	R_b	1 mΩ
Switching Frequency	f_s	1000 Hz
Bus Supply Voltage	V_b	1600 V
Supply Voltage	v_s	$300\cos(2\pi \cdot 50t)$

Table 3.3: Parameters of two-level series-stacked converter used in the simulations.

3.2.5 Simulation results

In this section the numerical techniques derived in the previous section are used to study the behavior of the two-level series-staked converter under a number of different conditions. First the transient behavior is studied. This is followed by a study of the steady-state analysis.

Table 3.3 gives the converter parameters that will be used throughout this section, unless stated otherwise.

3.2.5.1 Transient behavior

In this section a number of simulations of the transient behavior of the two-level series-stacked converter are carried out. Only the solutions of the homogeneous part of equation 3.80 are studied. For this reason V_b and v_s are taken as zero. The techniques of section 3.2.4.4.1 are applied and were implemented in a Matlab program, which is given in Appendix B.

Example 3.5

In this example the same reference function as in example 3.2.3.1 is used:

$$f_r(t) = 0.8\cos(2\pi \cdot 50t) \tag{3.123}$$

Figure 3.18 shows the voltage and current waveforms. For current i_d the envelope formed by $v_{d_o}\sqrt{\frac{C_d}{L}}e^{-\frac{t}{\tau}}$ and $-v_{d_o}\sqrt{\frac{C_d}{L}}e^{-\frac{t}{\tau}}$ is shown, while the envelope formed by $v_{d_o}e^{-\frac{t}{\tau}}$ and $-v_{d_o}e^{-\frac{t}{\tau}}$ is shown for v_d. A comparison with Figure 3.8(e) reveals that i_d and v_d show almost exact agreement with the case of ordinary switching. Unlike with ordinary switching i_t, v_t, v_o and i_b

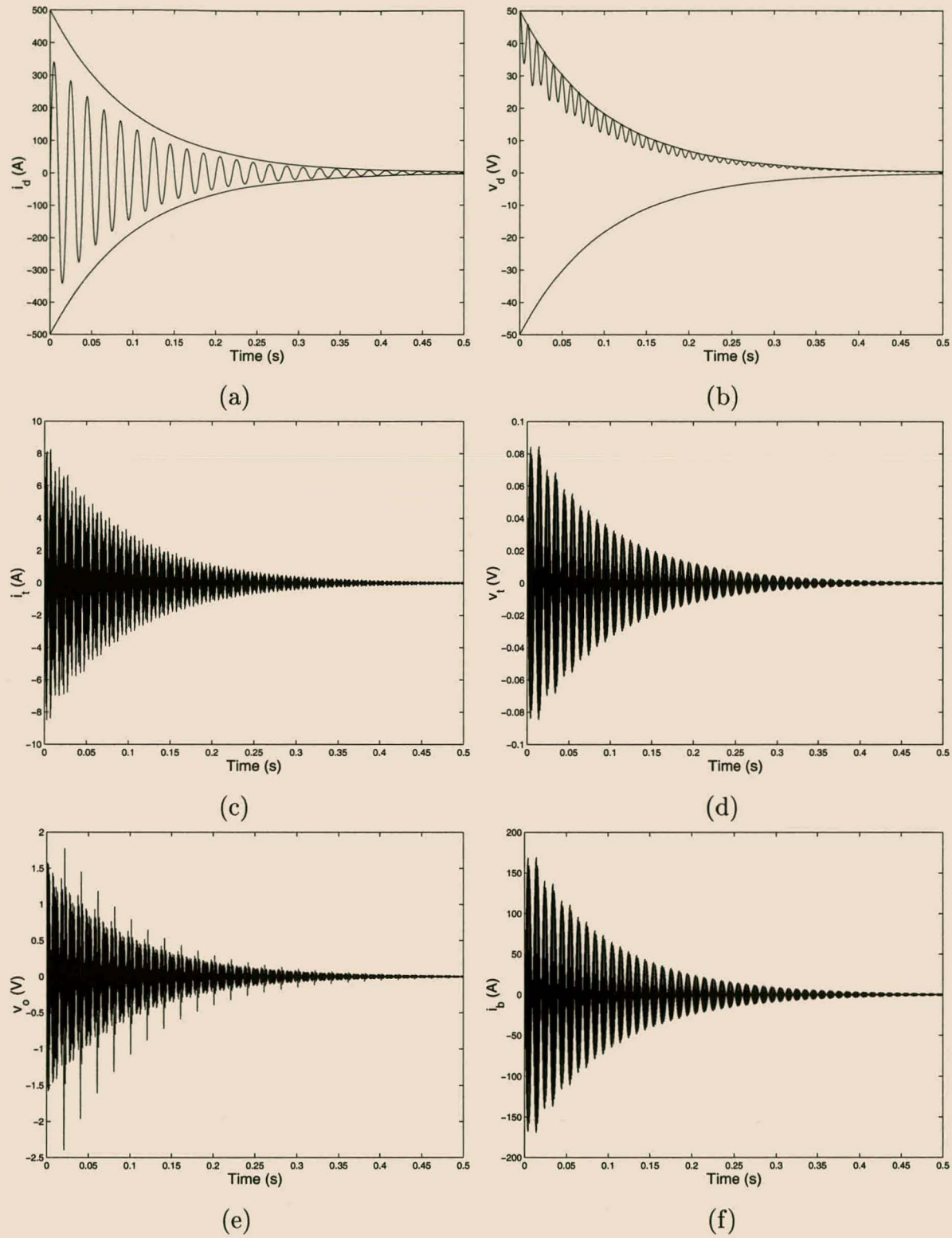


Figure 3.18: Voltage and current waveforms of a two-level series-stacked converter during re-balancing.

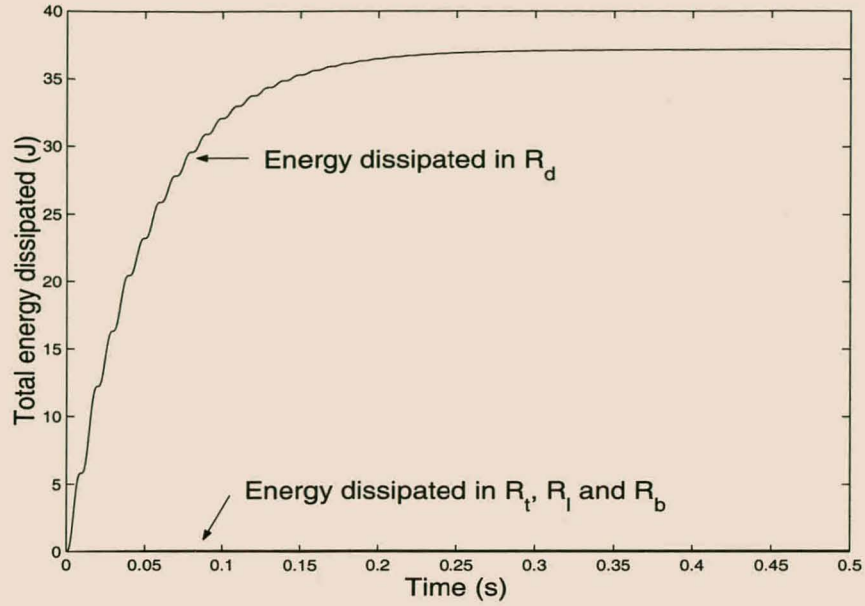


Figure 3.19: Energy dissipated in different resistors as functions of time.

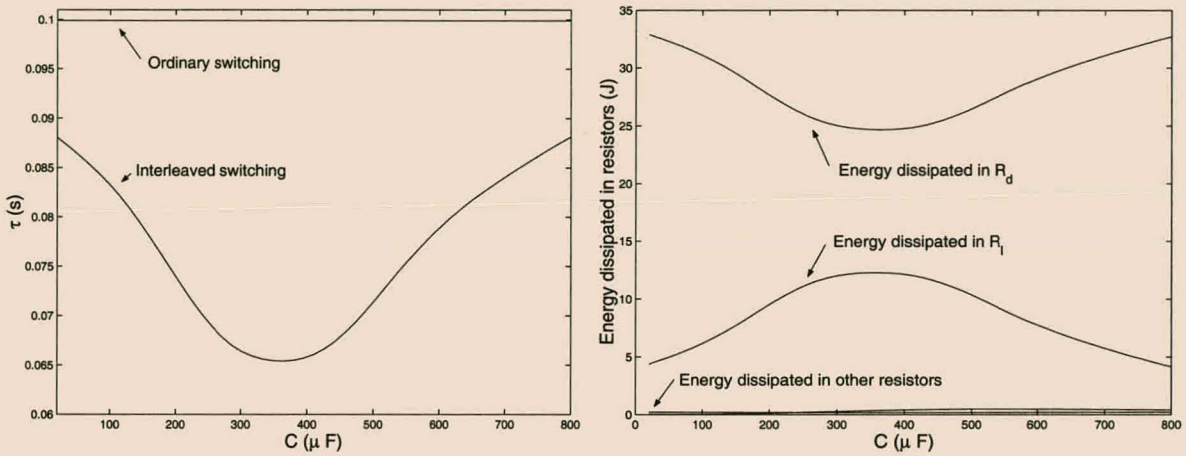
are no longer zero, but contain 'high-frequency' components as a result of the fact that s_t is no longer zero. Except for current i_b these high-frequency components are relatively small and have little effect on the steady-state values of the respective voltages and currents. Practical converters will have inductance between the DC-bus and voltage source V_b, which will further attenuate the high-frequency currents flowing through R_b.

One of the major differences between ordinary and interleaved switching is a slight decrease in the time constant τ, associated with the rebalancing process, in the case of interleaved switching. This is in agreement with the theory. Time constant τ equals 0.0996 s for interleaved switching, while τ equals 0.1004 s for ordinary switching. It will soon be shown that at lower switching frequencies this difference in time constants is more significant. The reason for this is that at lower switching frequencies the ripple currents play a more significant role in the balancing mechanisms.

Figure 3.19 shows the energy dissipated in the different resistors of the d and t circuit as a function of time. Table 3.4 shows the total energy dissipated in each of the resistors over the first 0.5 s and compares this with the initial energy stored in C_d. It is interesting to note that the second-most energy is dissipated in R_b. The fact that very little energy is dissipated in R_t shows that the ripple current through this resistor does not play a significant role in the balancing process. The main balancing mechanism is the 'low-frequency' current through R_d.

Parameter	Value
Total Energy Dissipated in R_d	37.17J
Total Energy Dissipated in R_t	00.001J
Total Energy Dissipated in R_l	0.04J
Total Energy Dissipated in R_b	0.12J
Total Energy Dissipated	37.3 J
Initial Stored Energy	37.5 J

Table 3.4: Energy dissipated in the different resistors during the first 0.5 s.



(a) (b)

Figure 3.20: Interleaved switching with $f_s = 250$Hz. (a) Time constant τ as a function of C; (b) Energy dissipated in the different resistors over the first 0.5 s as functions of C.

Example 3.6

In this example the switching frequency is reduced to 250 Hz to study the effect of interleaved switching, and its interaction with the output filter, on the rebalancing properties. Figure 3.20(a) shows time constant τ as a function of the filter capacitance C. For ordinary switching this time constant is independent of C and is equal to 0.0999 s. Figure 3.20(b) shows the energy dissipated in the different d and t circuit resistors over the first 0.5 s as a function of C. Only the energy dissipated in R_d and R_l play a significant role in this example.

Time constant τ reaches a minimum for C equal to 350μF. At twice the switching frequency (equal to 500 Hz) $|Z_2|$ is close to its minimum value (see Figure 3.21), while $\left|\frac{V_o(\omega)}{V_1(\omega)}\right|$ is close to its maximum value (refer to Figure 3.15 for the definition of v_1) . This implies that the maximum power is being transferred to resistors R_d and R_l. In this example the energy dissipated in

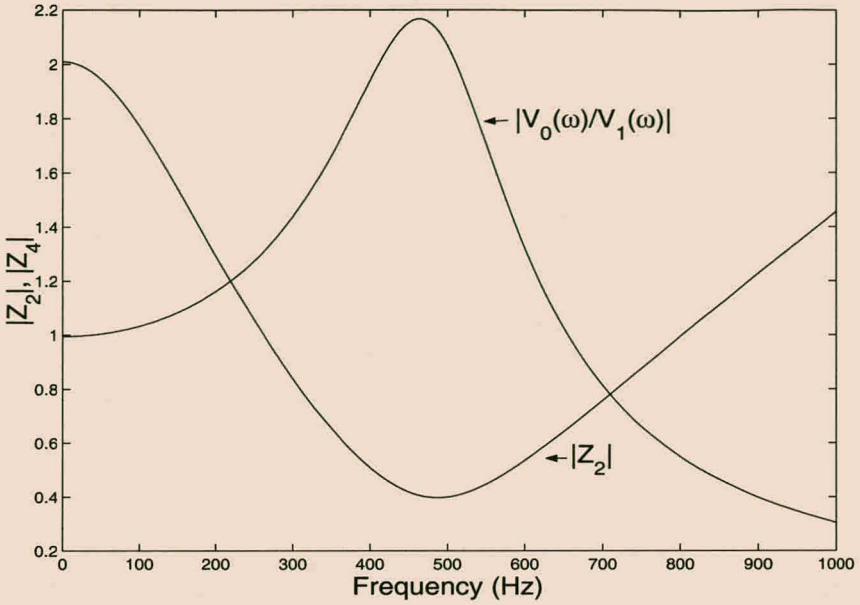


Figure 3.21: $|Z_2|$ and $\left|\frac{v_o(\omega)}{V_1(\omega)}\right|$ as functions of frequency for C=350μF.

R_d is the most important balancing mechanism, with energy dissipated in R_l the second-most important.

The undamped resonant frequency of L and C, with $C = 350$ μF, is

$$f_0 = \frac{1}{2\pi\sqrt{LC}} = 491 \text{ Hz}. \tag{3.124}$$

Figure 3.22 shows i_d and v_d for ordinary and interleaved switching. The switching frequency is 250 Hz and $C = 350$ μF. For ordinary switching time constant $\tau = 0.10$ s, while $\tau = 0.66$ s for interleaved switching. This difference in time constants can be observed in the results.

Example 3.7

In this example the non-sinusoidal reference function

$$f_r(t) = 0.5\cos(2\pi \cdot 50t) + 0.3\cos(2\pi \cdot 250t) + 0.1\cos(2\pi \cdot 350t) \tag{3.125}$$

of equation 3.41 is used. Figure 3.23 shows the results of the simulation. The main difference with the previous examples is a larger time constant τ which is equal to 0.2 s compared to 0.1 s and smaller in the previous examples. This increase in τ can be attributed to the smaller RMS value of the reference signal compared to the previous examples (0.35 compared to 0.64).

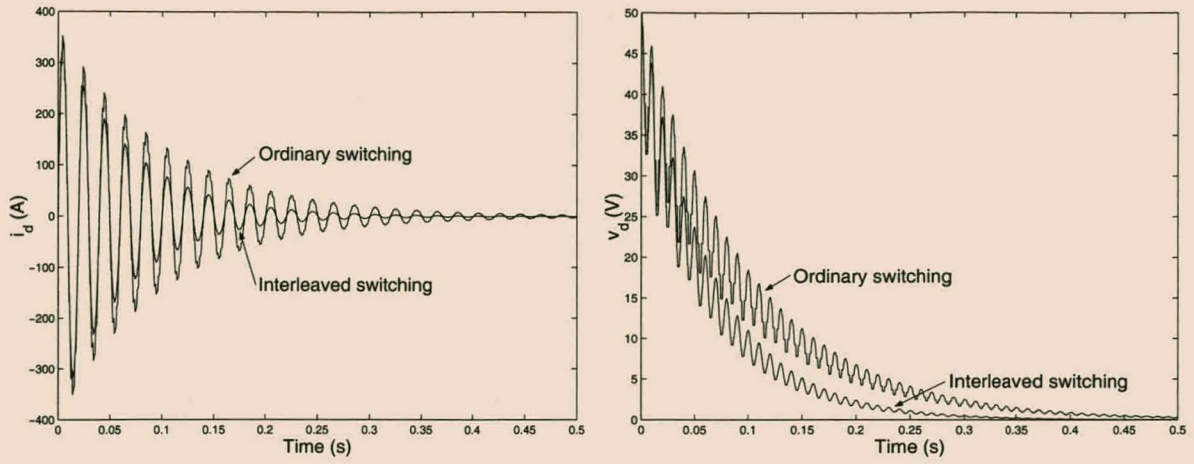


Figure 3.22: Voltage and current waveforms for ordinary and interleaved switching (C = 350 μF and f_s = 250 Hz).

3.2.5.2 Steady-state behavior

In this section the numerical simulations based on the methods of section 3.2.4.4.2 are used to analyze the steady-state behavior of the two-level series-stacked converter. A Matlab program to implement the algorithms is presented in Appendix B. Throughout this section the parameters of Table 3.3 are used. Unlike in the previous section the bus voltage V_b is not set to zero but is equal to 1600 V.

Example 3.8

In this example the reference function

$$f_r(t) = 0.8\cos(2\pi \cdot 50t) \tag{3.126}$$

is again used, while

$$v_s = 300\cos(2\pi \cdot 50t). \tag{3.127}$$

Figure 3.24 shows the results of the simulation over one 50 Hz cycle. All of the waveforms are periodic. Current i_d has a peak value of 300 A. The ripple in the DC-bus voltage v_t has a peak value of approximately 0.6 V, which is less than 0.01% of the total DC-bus voltage of 1600 V.

The average values of i_d and v_d are 0.5 A and -0.4 V, respectively. This is very small compared to the values of $V_b = 1600V$ and a peak output current i_t of 1000 A. These results are in agreement with the theory, which states that these average values should be approximately equal to zero.

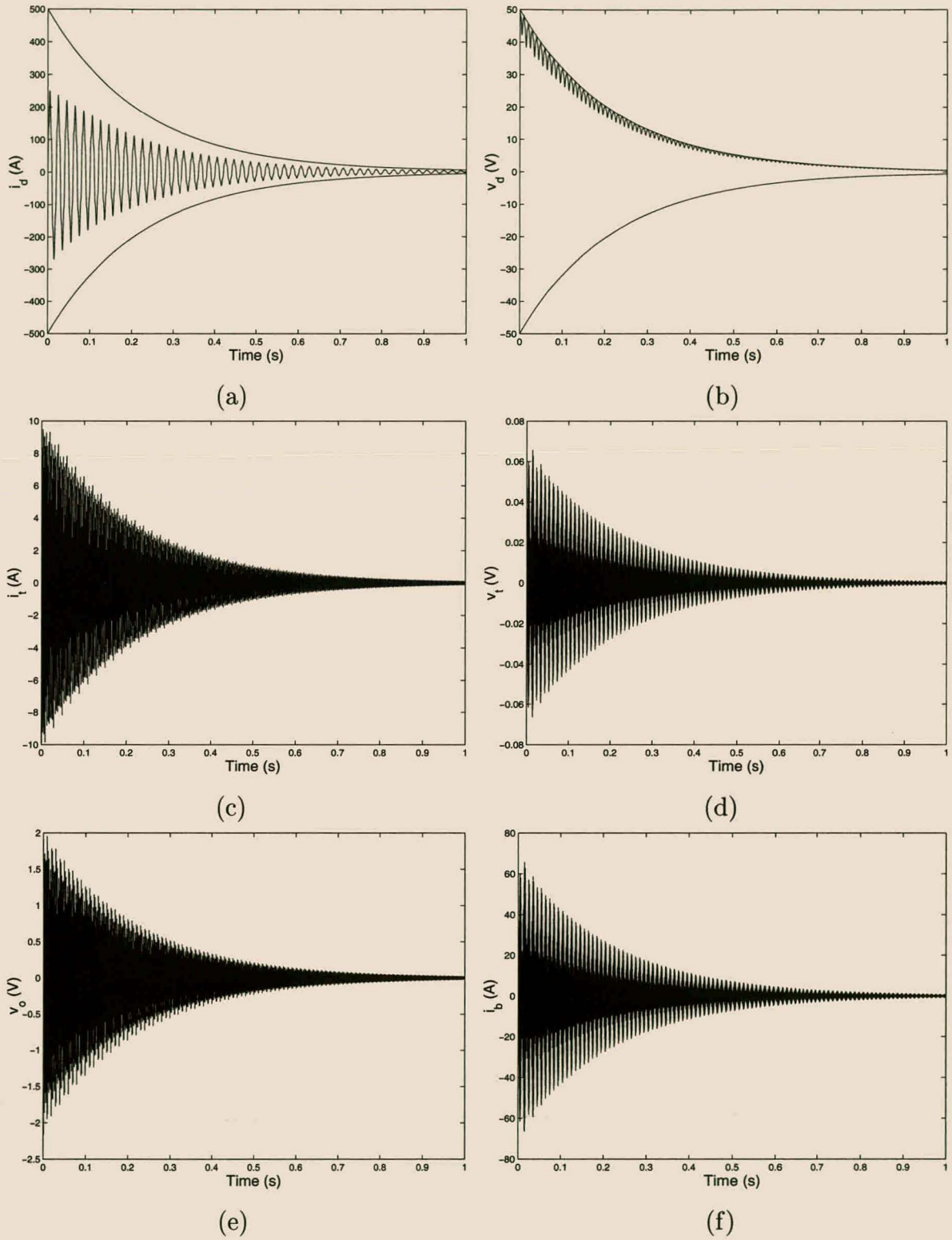


Figure 3.23: Voltage and current waveforms with non-sinusoidal reference.

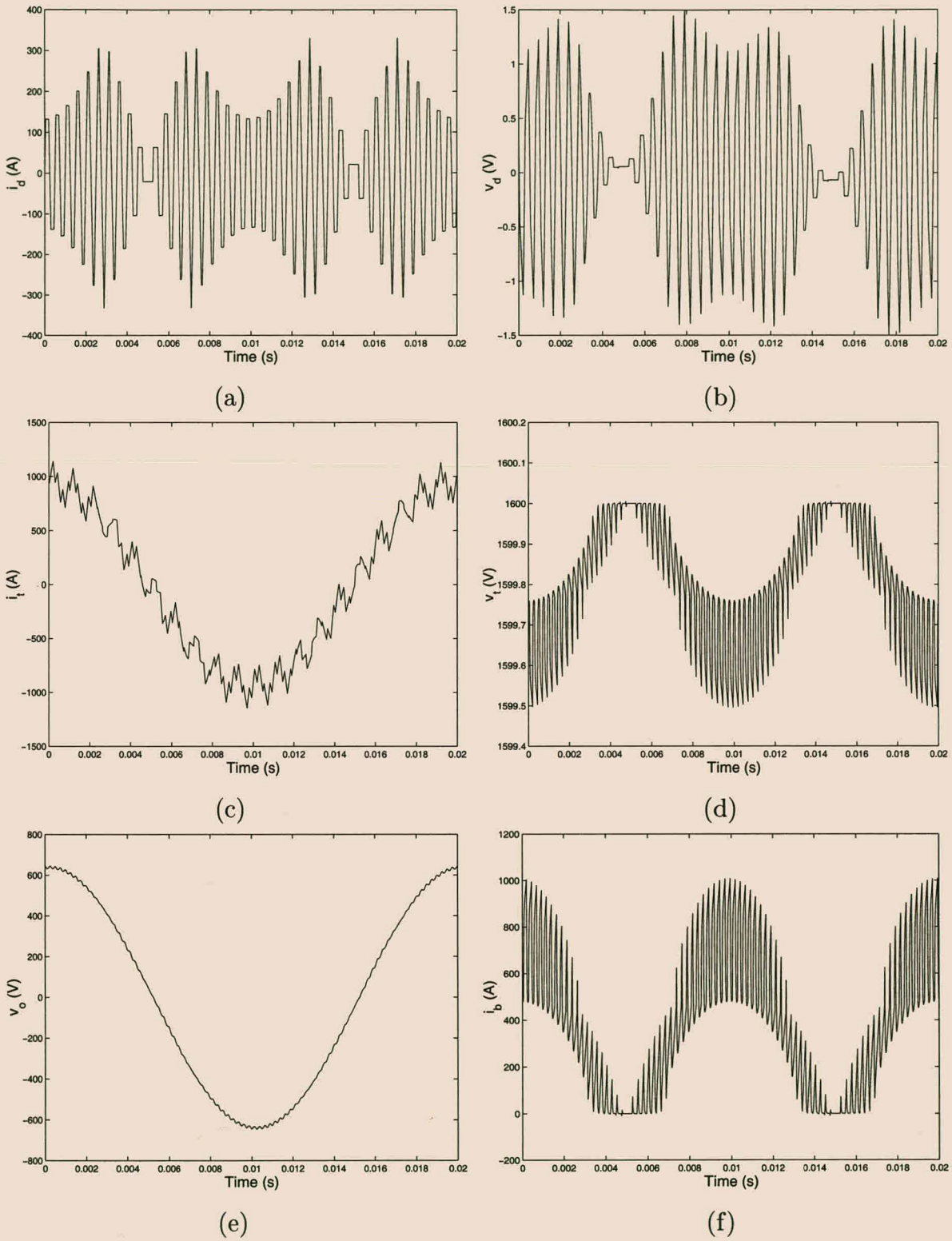


Figure 3.24: Steady-state voltage and current waveforms for a two-level series-stacked converter under interleaved switching.

Example 3.9

This example investigates the effect of high-frequency components of the reference signal on the steady-state behavior of the converter. The same parameters as in the previous example are used, but in this case the reference function contains a harmonic near twice the switching frequency. In this case f_r is given by

$$f_r(t) = 0.8\cos(2\pi \cdot 50t) + 0.1\cos(2\pi \cdot 2050t). \tag{3.128}$$

Figure 3.25 shows the results of the simulation.

The product $|S_d(\omega)S_t(\omega)|$ is shown in Figure 3.25 (d). The largest components of $|S_d(\omega)S_t(\omega)|$ are at 50 Hz and around 2 kHz. This product is the major contributor to the numerator of equation 3.97, which predicts the average value of v_d. The average value of v_d in Figure 3.25(b) is 165 V, while calculation of the average value of v_d by means of equation 3.97 yielded a value of 132 V. It should, however, be noted that v_d contains a 100 Hz component, as well as some higher-frequency components which were not taken into account in the development of the theory. The average values of all the other voltages and currents are zero. (The largest average value is that of i_d which is equal to -0.04A.)

It is interesting to note that the peak value of current i_d more than doubled as a result of the high-frequency term in the reference signal.

Example 3.10

In this final example the effect of a high-frequency component of the supply voltage on the steady-state behavior of the two-level series-stacked converter is evaluated. Due to the attenuation of high-frequency components of the supply current by the converter's output filter, a very large harmonic had to be used to see a significant effect on v_d. For this example $v_s(t)$ is given by

$$300\cos(2\pi \cdot 50t) + 2000\cos(2\pi \cdot 2050t). \tag{3.129}$$

Although this signal is most unlikely to occur in practical situations, it was chosen to demonstrate the theory. Figure 3.26 shows the results. The average value of v_d is 19.2 V. Calculation of the average value of v_d, by making use of equation 3.103, gave a value of 14.2 V. The difference can again be attributed to the fact that, during the theoretical analysis, it was assumed that v_d contained only a DC component.

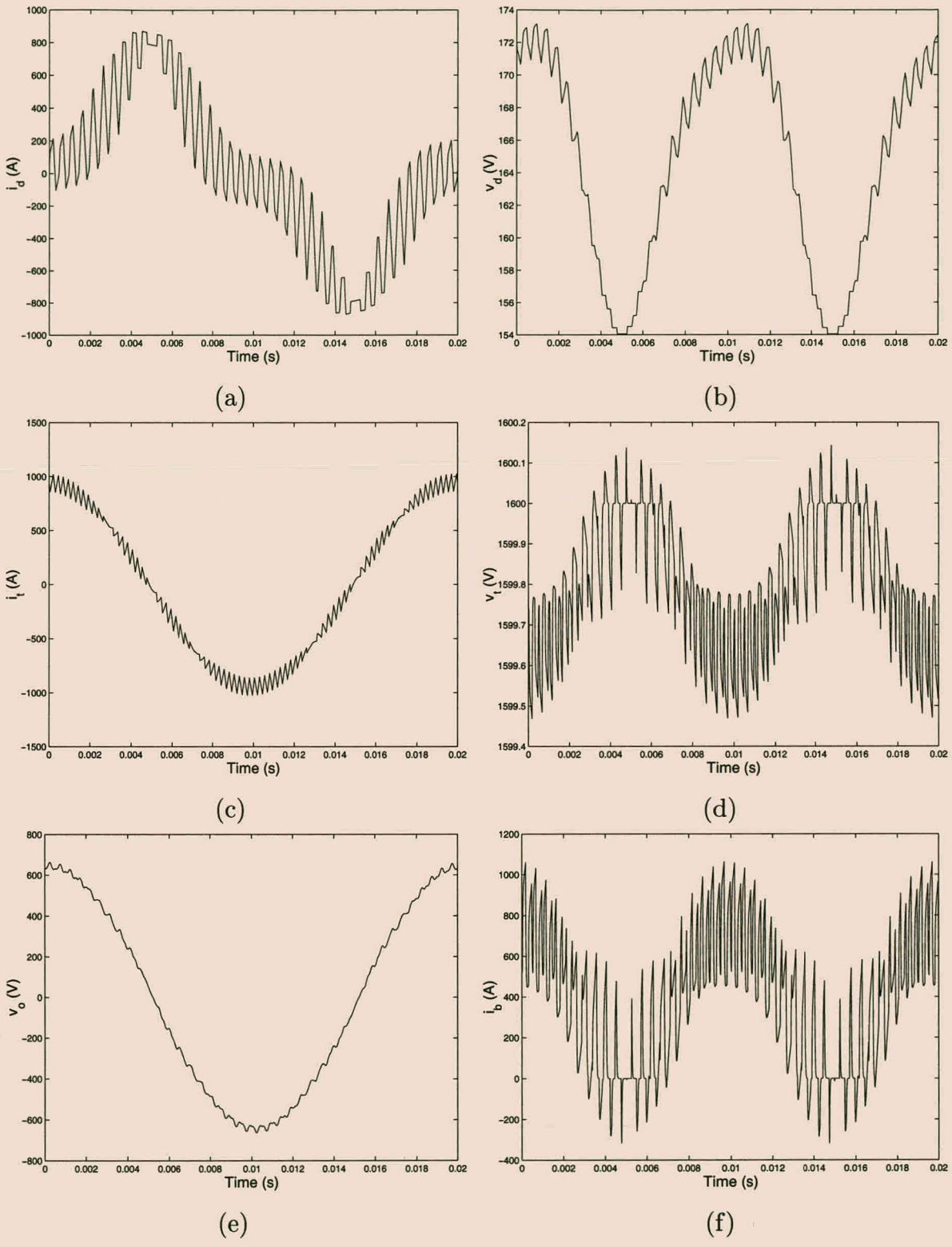


Figure 3.25: Steady-state voltage and current waveforms for a two-level series-stacked converter under interleaved switching.

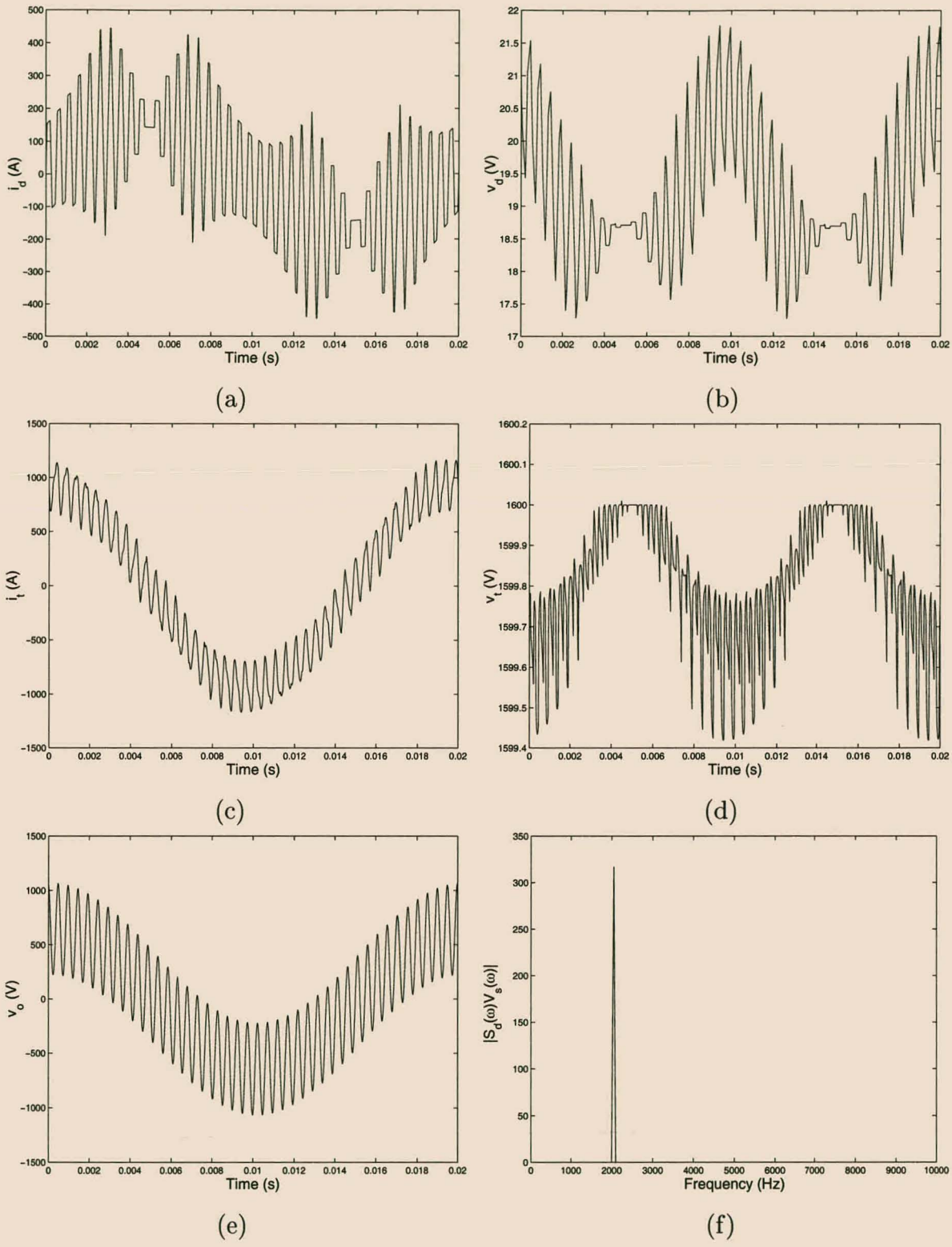


Figure 3.26: Steady-state voltage and current waveforms for a two-level series-stacked converter under interleaved switching.

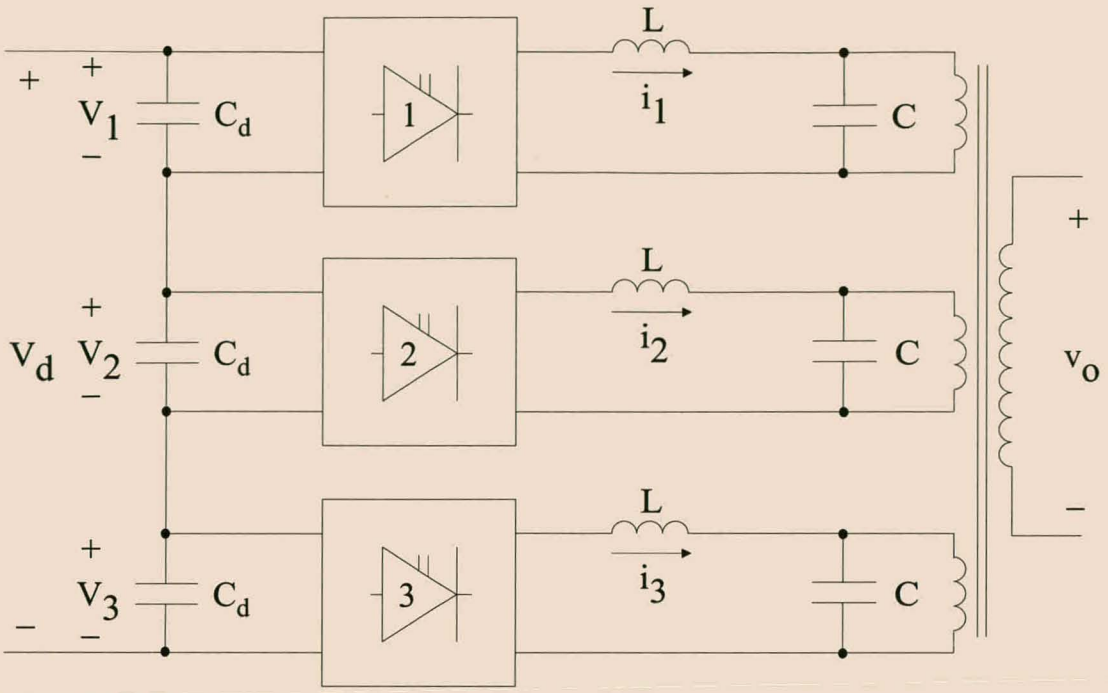


Figure 3.27: Three-level series-stacked converter.

3.3 Three-level series-stacked converters

Figure 3.27 shows the three-level series-stacked converter which was introduced in Chapter 2 and is repeated here for convenience. The converter topology is similar to that of the two-level series-stacked converter with the addition of an extra level.

3.3.1 Basic circuit analysis

In this section the differential equations describing the three-level series-stacked converter are derived. As in the case of the two-level series-stacked converter, d and t parameters are then introduced to study the balancing properties of the circuit.

Figure 3.28 shows the equivalent circuit of the three-level series-stacked converter. The same assumptions and simplifications as for the two-level series-stacked converter are made. Let s_1 be the switching function of the top converter, s_2 the switching function of the center converter and s_3 the switching function of the bottom converter. The three-level series-stacked converter is described by the following system of differential equations:

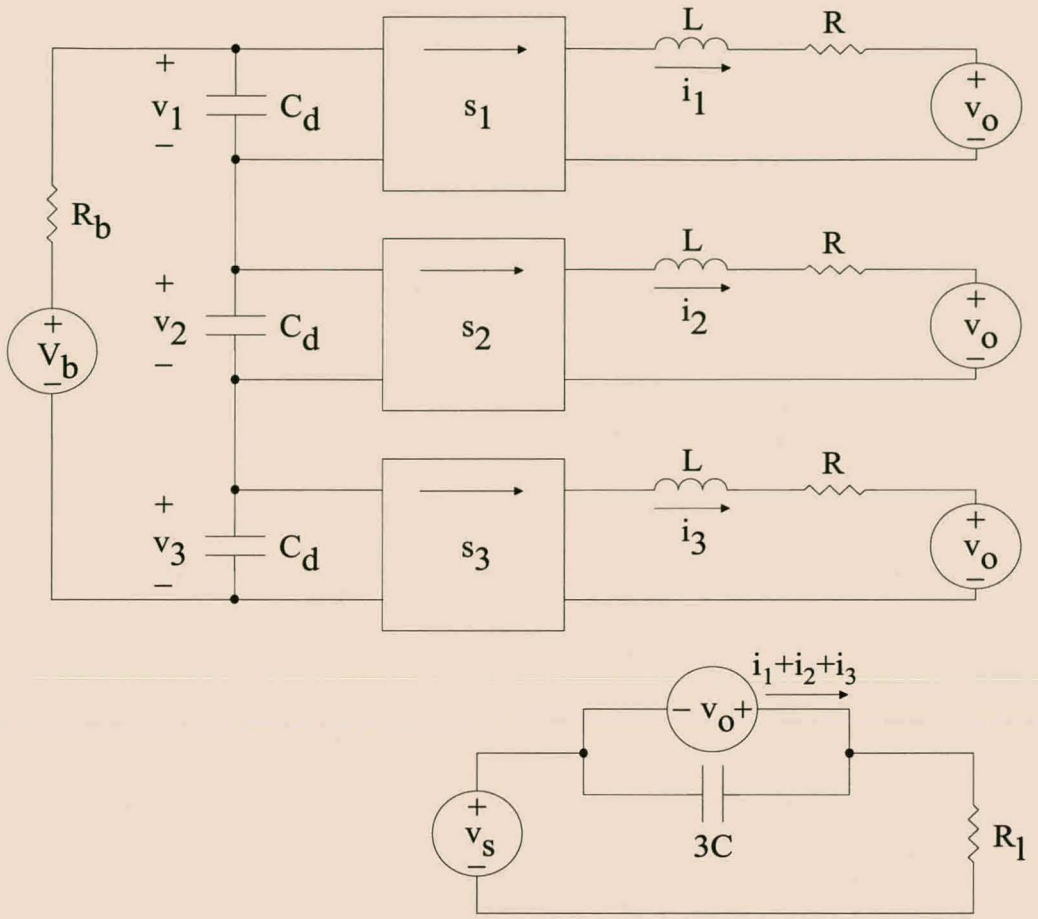


Figure 3.28: Equivalent circuit of the three-level series-stacked converter used in the analysis.

$$\begin{bmatrix} \frac{di_1}{dt} \\ \frac{di_2}{dt} \\ \frac{di_3}{dt} \\ \frac{dv_1}{dt} \\ \frac{dv_2}{dt} \\ \frac{dv_3}{dt} \\ \frac{dv_o}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 & 0 & \frac{s_1}{L} & 0 & 0 & -\frac{1}{L} \\ 0 & -\frac{R}{L} & 0 & 0 & \frac{s_2}{L} & 0 & -\frac{1}{L} \\ 0 & 0 & -\frac{R}{L} & 0 & 0 & \frac{s_3}{L} & -\frac{1}{L} \\ -\frac{s_1}{C_d} & 0 & 0 & -\frac{1}{R_bC_d} & -\frac{1}{R_bC_d} & -\frac{1}{R_bC_d} & 0 \\ 0 & -\frac{s_2}{C_d} & 0 & -\frac{1}{R_bC_d} & -\frac{1}{R_bC_d} & -\frac{1}{R_bC_d} & 0 \\ 0 & 0 & -\frac{s_3}{C_d} & -\frac{1}{R_bC_d} & -\frac{1}{R_bC_d} & -\frac{1}{R_bC_d} & 0 \\ \frac{1}{3C} & \frac{1}{3C} & \frac{1}{3C} & 0 & 0 & 0 & -\frac{1}{3R_lC} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_1 \\ v_2 \\ v_3 \\ v_o \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ \frac{V_b}{R_bC_d} \\ \frac{V_b}{R_bC_d} \\ \frac{V_b}{R_bC_d} \\ -\frac{v_s}{3R_lC} \end{bmatrix} \tag{3.130}$$

To transform the original circuit to d and t parameters the following transformation matrix is introduced:

$$D = \begin{bmatrix} \frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{1}{2} & -\frac{1}{2} \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix} \tag{3.131}$$

This definition states that current i_{d_1} and voltage v_{d_1} are equal to half of the difference between currents i_1 and i_2 and voltages v_1 and v_2, respectively. Similarly, current i_{d_2} and voltage v_{d_2} are equal to half of the difference between currents i_2 and i_3 and voltages v_2 and v_3, respectively.

Current i_t and voltage v_t are equal to one third of the sum of the three filter inductor currents and the three DC-bus capacitor voltages, respectively.

The inverse transformation D^{-1} is given by

$$D^{-1} = \frac{1}{3}\begin{bmatrix} 4 & 2 & 3 \\ -2 & 2 & 3 \\ -2 & -4 & 3 \end{bmatrix}. \tag{3.132}$$

The d and t switching functions, currents and voltages are given by

$$\begin{bmatrix} s_{d_1} \\ s_{d_2} \\ s_t \end{bmatrix} = D\begin{bmatrix} s_1 \\ s_2 \\ s_3 \end{bmatrix}, \quad \begin{bmatrix} i_{d_1} \\ i_{d_2} \\ i_t \end{bmatrix} = D\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \text{ and } \begin{bmatrix} v_{d_1} \\ v_{d_2} \\ v_t \end{bmatrix} = D\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix}. \tag{3.133}$$

Rewriting equation 3.130 in terms of the d and t parameters results in

$$\dot{x} = Ax + B, \tag{3.134}$$

where

$$A = \begin{bmatrix} -\frac{R}{L} & 0 & 0 & \frac{s_t+s_a}{L} & \frac{2s_{d_1}}{3L} & \frac{s_{d_1}}{L} & 0 \\ 0 & -\frac{R}{L} & 0 & -\frac{2s_{d_2}}{3L} & \frac{s_t-s_a}{L} & \frac{s_{d_2}}{L} & 0 \\ 0 & 0 & -\frac{R}{L} & \frac{8s_{d_1}+4s_{d_2}}{9L} & \frac{4s_{d_1}+8s_{d_2}}{9L} & \frac{s_t}{L} & -\frac{1}{L} \\ -\frac{s_t+s_a}{C_d} & -\frac{2s_{d_1}}{3C_d} & -\frac{s_{d_1}}{C_d} & 0 & 0 & 0 & 0 \\ \frac{2s_{d_2}}{3C_d} & -\frac{s_t-s_a}{C_d} & -\frac{s_{d_2}}{C_d} & 0 & 0 & 0 & 0 \\ -\frac{8s_{d_1}+4s_{d_2}}{9C_d} & -\frac{4s_{d_1}+8s_{d_2}}{9C_d} & -\frac{s_t}{C_d} & 0 & 0 & -\frac{3}{R_bC_d} & 0 \\ 0 & 0 & \frac{1}{C} & 0 & 0 & 0 & -\frac{1}{3R_lC} \end{bmatrix}; \tag{3.135}$$

and

$$s_a = \frac{2}{3}(s_{d_1} + s_{d_2}), \quad x = \begin{bmatrix} i_{d_1} \\ i_{d_2} \\ i_t \\ v_{d_1} \\ v_{d_2} \\ v_t \\ v_o \end{bmatrix} \text{ and } B = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ \frac{V_b}{R_bC_d} \\ -\frac{v_s}{3R_lC} \end{bmatrix}. \tag{3.136}$$

Figure 3.29 shows the equivalent circuit of the three-level series-stacked converter in terms of the d and t voltages, currents and switching functions. Unlike in the case of the two-level series-stacked converter, the equivalent circuit cannot be modeled by passive elements and two-port switching circuits only, but includes a number of controlled voltage and current sources. Despite several attempts, a linear transformation to d and t parameters that resulted in a simpler transformed equivalent circuit could not be found.

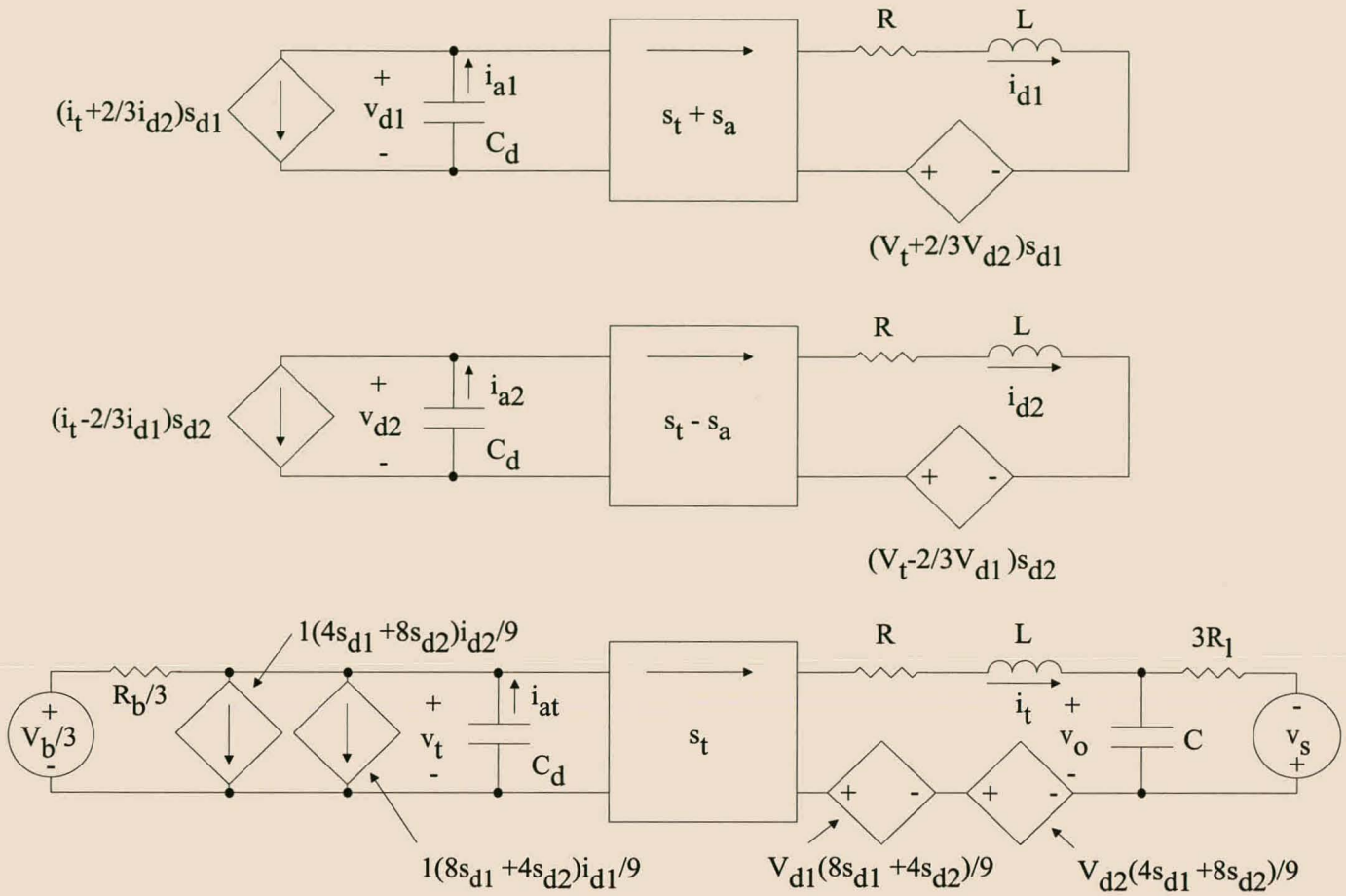


Figure 3.29: Three-level series-stacked converter in terms of d and t parameters.

3.3.2 Ordinary switching

Throughout this section it is assumed that the same switching functions are applied to all three levels of the three-level series-stacked converter. This means that $s := s_1 = s_2 = s_3$, which implies that $s_{d_1} = s_{d_2} = 0$ and $s_t = s$. As for the two-level series-stacked converter, this results in independent systems of differential equations, given by:

$$\dot{x}_{d_k} = A_d x_{d_k}, \tag{3.137}$$

where

$$x_{d_k} = \begin{bmatrix} i_{d_k} \\ v_{d_k} \end{bmatrix}, \quad A_d = \begin{bmatrix} -\frac{R}{L} & \frac{s}{L} \\ -\frac{s}{C_d} & 0 \end{bmatrix}, \tag{3.138}$$

for $k = 1, 2$; and

$$\dot{x}_t = A_t x_t + B_t, \tag{3.139}$$

where

$$x_t = \begin{bmatrix} i_t \\ v_t \\ v_o \end{bmatrix}, \quad A_t = \begin{bmatrix} -\frac{R}{L} & \frac{s}{L} & -\frac{1}{L} \\ -\frac{s}{C_d} & -\frac{3}{R_b C_d} & 0 \\ \frac{1}{C} & 0 & -\frac{1}{3R_L C} \end{bmatrix} \text{ and } B_t = \begin{bmatrix} 0 \\ \frac{V_b}{R_b C_d} \\ -\frac{v_s}{3R_L C} \end{bmatrix}. \tag{3.140}$$

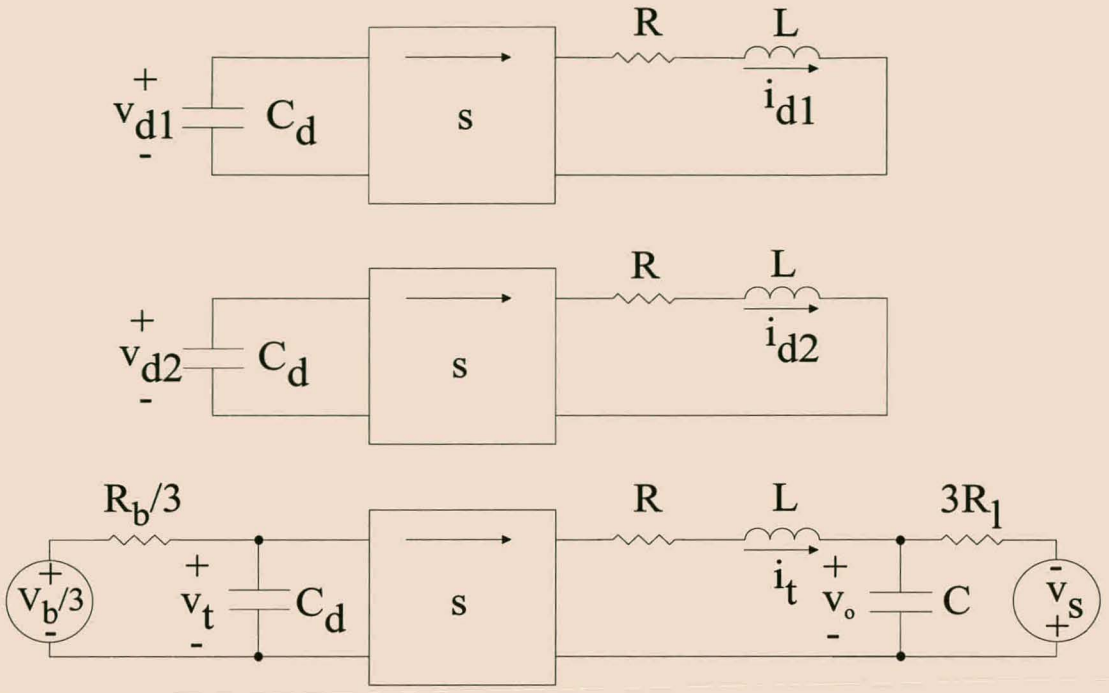


Figure 3.30: Three-level ordinary switching d and t circuits.

Figure 3.30 shows the three independent circuits. The voltages and currents of the three-level series-stacked converter are balanced when all the d voltages and currents are equal to zero. As for the two-level series-stacked converter under ordinary switching, the t circuit is independent of the d circuits. This implies that unbalance in the converter does not affect the output voltage or current waveforms, nor does the output voltage or current have an effect on the balancing properties of the converter.

The two d circuits are identical to the d circuit of the two-level series-stacked converter studied in section 3.2.3 and the theory developed in that case can be applied directly to the current analysis. The following is a short summary of the theory of section 3.2.3 as it applies to the three-level series-stacked converter:

1. A Liapunov argument shows that the two d circuits are stable and that the voltages and currents of the two d circuits are equal to zero in the steady state. The energy stored in a particular d circuit is dissipated in the parasitic resistor R of that circuit. The rate of rebalancing depends on the RMS value of the d circuit currents i_{d_1} and i_{d_2}. These currents can be split into two components namely a 'low-frequency' component and a 'ripple' component. The ripple component increases with decreasing switching frequency, while the low-frequency component depends mainly on the reference function f_r.

2. The exact behavior of the balancing mechanisms of each d circuit can be studied by making use of Floquet's theorem. The first step in applying this theory is to calculate

the d circuit fundamental matrix given by equation 3.16

$$\Phi(t) = e^{A_d(s_n)t} e^{A_d(s_{n-1})t_{n-1}} \cdots e^{A_d(s_1)t_1}. \tag{3.141}$$

The fundamental matrices of the two d circuits are identical. Hence, the balancing time constants of the two circuits are equal and independent of the initial conditions.

3. If σ_1 and σ_2 are the eigenvalues of $M = \Phi(T_r)$, then

$$\tau = \max\left(-\frac{T_r}{\mathrm{Re}(\log \sigma_1)}, -\frac{T_r}{\mathrm{Re}(\log \sigma_2)}\right) \tag{3.142}$$

is the time constant of the balancing process. The value of τ is highly dependent on the reference function f_r and τ may range from $\frac{L}{R}$ to infinity. In general τ decreases as the switching frequency decreases for a particular reference signal f_r.

4. The fundamental matrix $\Phi(t)$ can be used to simulate the exact behavior of the d circuits over time.

5. The design guideline

$$C_d \geq \frac{1}{L\omega_r^2\pi^2} \tag{3.143}$$

also applies in the case of the three-level series-stacked converter. Choosing the values of C_d and L according to this guideline will greatly reduce the oscillations in the DC-bus voltages following a perturbation.

Example 3.11

In this example the reference signal

$$f_r(t) = 0.7\cos(2\pi \cdot 50t) + 0.2\cos(2\pi \cdot 150t) + 0.1\cos(2\pi \cdot 550t) \tag{3.144}$$

is applied to a three-level series-stacked converter under ordinary unipolar switching. Table 3.5 gives the converter parameters.

For the results of Figure 3.31 $C_d = 30$ mF, while $C_d = 2$ mF for the results of Figure 3.32. Time constant $\tau = 0.12$ s for $C_d = 30$ mF, while $\tau = 0.06$ s for $C_d = 2$ mF. For Figure 3.31 the value of C_d is significantly larger than the value of 3.4 mF given by equation 3.143. The envelope formed by

$$v_{d_0} e^{-\frac{t}{\tau}} \quad \text{and} \quad -v_{d_0} e^{-\frac{t}{\tau}} \tag{3.145}$$

is shown for the d voltages.

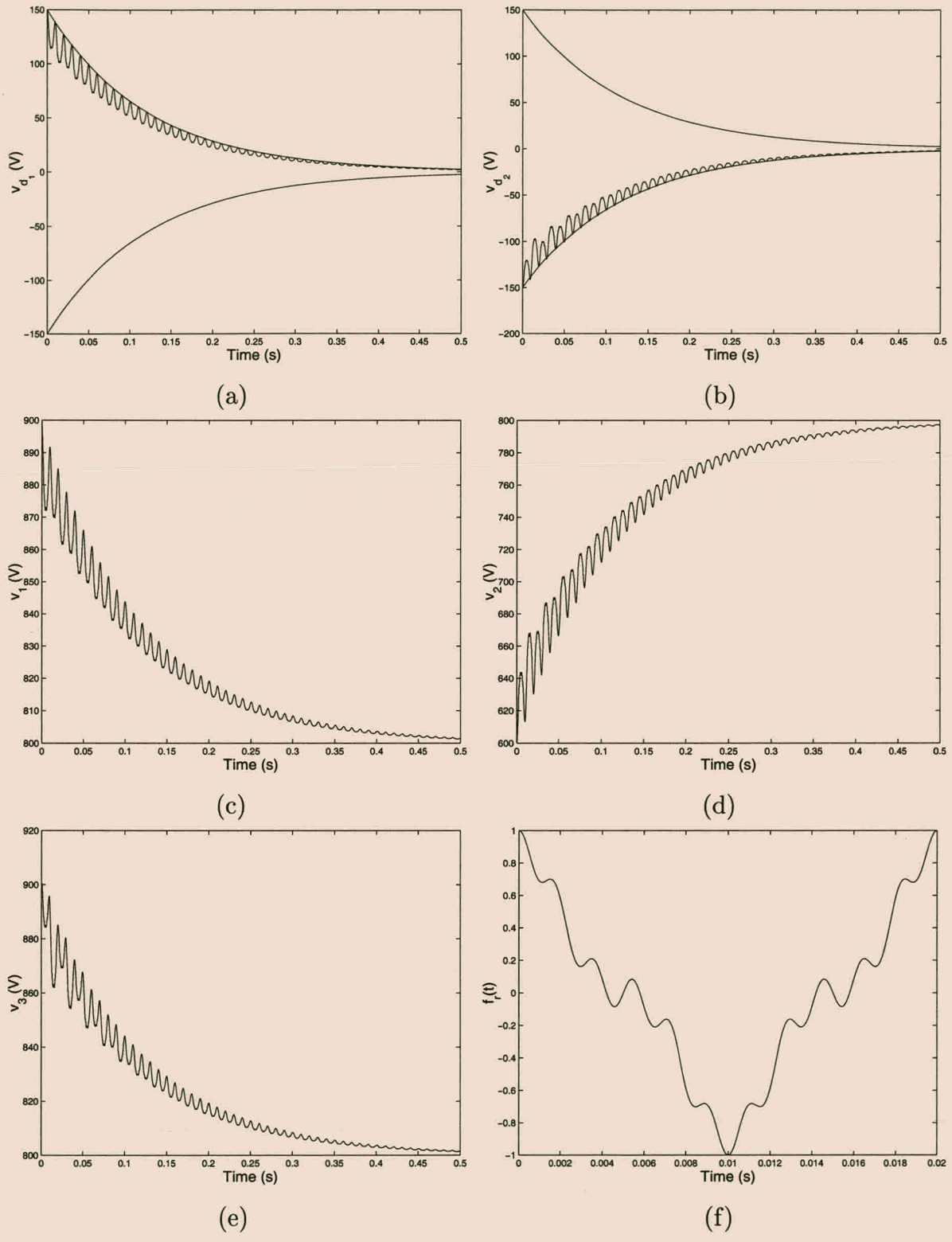


Figure 3.31: Voltage waveforms for a three-level series-stacked converter under ordinary unipolar switching with $C_d = 30$ mF.

Parameter	Symbol	Value
Filter Inductance	L	300 μH
Parasitic Resistance	R	0.01 Ω
Switching Frequency	f_s	1000 Hz
Initial Inductor Current 1	i_{d1_0}	1000 A
Initial Inductor Current 2	i_{d2_0}	900 A
Initial Inductor Current 3	i_{d3_0}	800 A
Initial Capacitor Voltage 1	v_{d1_0}	900 V
Initial Capacitor Voltage 2	v_{d2_0}	600 V
Initial Capacitor Voltage 3	v_{d3_0}	900 V
Total DC-bus Voltage	V_b	2 400 V

Table 3.5: Parameters of a three-level series-stacked converter.

The most important difference between the results of the two figures is the large oscillations in the DC-bus voltage for $C_d = 2$ mF. This leads to increased voltage stresses on the switches of converter 2. For $C_d = 30$ mF, the maximum bus voltage is equal to 900 V (for converters 1 and 3), while the maximum bus voltage increased to 960 V (for converter 2) when C_d was decreased to 2 mF.

3.3.3 Interleaved switching

In this section the effect of interleaved switching on the behavior of the three-level series-stacked converter is investigated. The state-space averaging technique at the beginning of section 3.2.4.3 can also be applied to the three-level series-stacked converter. The details of this process are identical to those followed in section 3.2.4.3 and will not be repeated here. The main conclusion of this analysis is that at high switching frequencies, the behavior of the three-level series-stacked converter under interleaved switching closely approximates its behavior under ordinary switching. It also gives an indication that the difference between ordinary and interleaved switching lies in the effect of the high-frequency ripple currents and voltages.

3.3.3.1 Harmonics of three-level interleaved PWM

In this section the techniques of sections 3.2.4.1 and 3.2.4.2 are adapted in order to study the harmonics of the switching functions for three-level interleaved switching. As in the case of the two-level series-stacked converter only unipolar switching with natural sampled double-edge modulation is considered. It is again assumed that the switching frequency ω_s is an integer

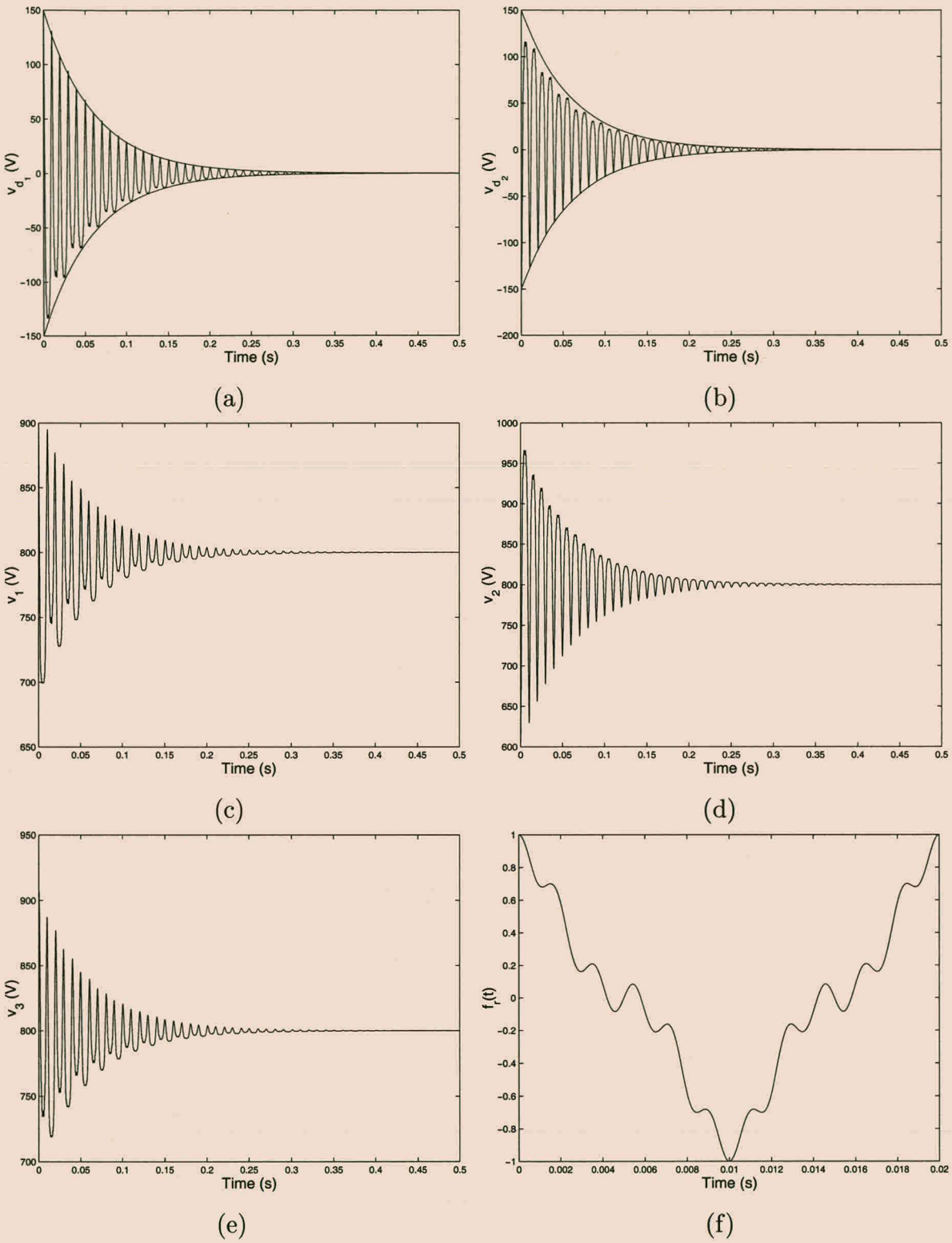


Figure 3.32: Voltage waveforms for a three-level series-stacked converter under ordinary unipolar switching with $C_d = 2$ mF.

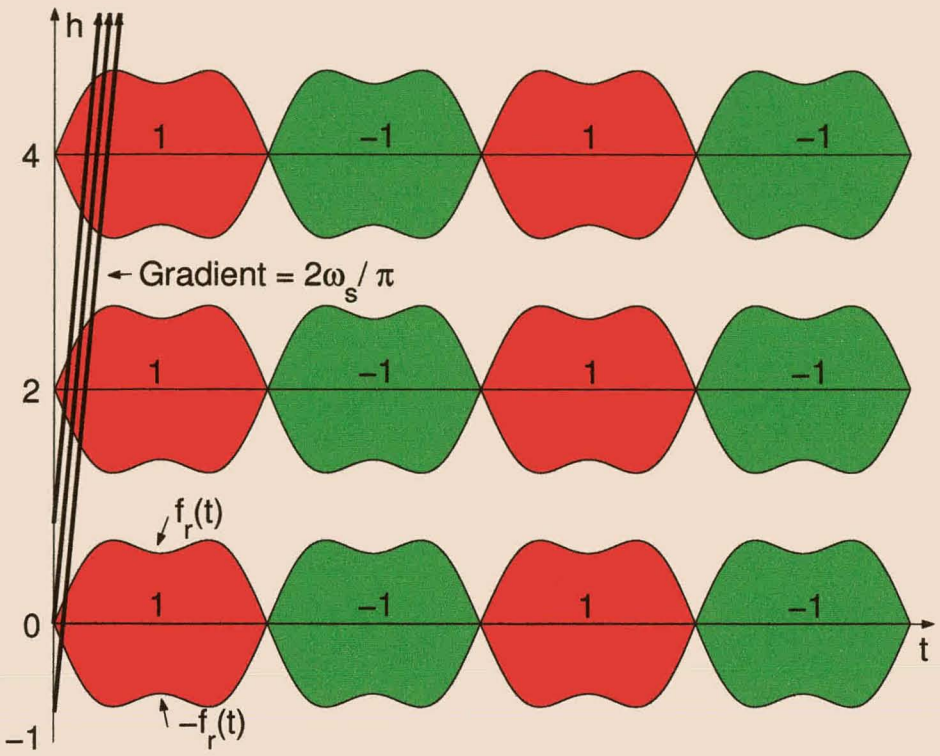


Figure 3.33: Three-dimensional representation of three-level interleaved switching with unipolar modulation.

multiple of the frequency ω_r of the reference signal.

For three-level interleaved switching the carrier signals of the three converters are phase shifted by $\frac{\pi}{3}$ radians. (Recall that unipolar modulation effectively doubles the switching frequency.) By adapting the arguments of section 3.2.4.2, this gives rise to three lines in the TOH-plane, given by

$$\left(\frac{2\omega_s}{\pi}t, t\right), \left(\frac{2\omega_s}{\pi}t - \frac{2}{3}, t\right) \text{ and } \left(\frac{2\omega_s}{\pi}t + \frac{2}{3}, t\right) \tag{3.146}$$

associated with switching functions s_1, s_2 and s_3 respectively. Figure 3.33 shows these three lines. Recall that Figure 3.33 extends periodically along the t and h axes.

The three switching functions s_1, s_2 and s_3 are given by

$$s_1(t) = F\left(\frac{2\omega_s}{\pi}t, t\right),\ s_2(t) = F\left(\frac{2\omega_s}{\pi}t - \frac{2}{3}, t\right) \text{ and } s_3(t) = F\left(\frac{2\omega_s}{\pi}t + \frac{2}{3}, t\right), \tag{3.147}$$

where function F was defined in equation 3.56.

Substituting these three equations into equation 3.58 results in

$$\begin{aligned} s_1(t) \;=\; & \frac{1}{2}A_{00} + \sum_{n=1}^{\infty}\left(A_{0n}\cos n\omega_r t + B_{0n}\sin n\omega_r t\right) + \sum_{m=1}^{\infty}\left(A_{m0}\cos 2m\omega_s t + B_{m0}\sin 2m\omega_s t\right) \\ & + \sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty}\left(A_{mn}\cos(2m\omega_s t + n\omega_r t) + B_{mn}\sin(2m\omega_s t + n\omega_r t)\right), \end{aligned} \tag{3.148}$$

$$
\begin{aligned}
s_2(t) &= \frac{1}{2}A_{00} + \sum_{n=1}^{\infty}(A_{0n}\cos n\omega_r t + B_{0n}\sin n\omega_r t) \\
&\quad + \sum_{m=1}^{\infty}\left(A_{m0}\cos(2m\omega_s t - \frac{2\pi}{3}m) + B_{m0}\sin(2m\omega_s t - \frac{2\pi}{3}m)\right) \\
&\quad + \sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty}\left(A_{mn}\cos(2m\omega_s t - \frac{2\pi}{3}m + n\omega_r t) + B_{mn}\sin(2m\omega_s t - \frac{2\pi}{3}m + n\omega_r t)\right)
\end{aligned}
\tag{3.149}
$$

and

$$
\begin{aligned}
s_3(t) &= \frac{1}{2}A_{00} + \sum_{n=1}^{\infty}(A_{0n}\cos n\omega_r t + B_{0n}\sin n\omega_r t) \\
&\quad + \sum_{m=1}^{\infty}\left(A_{m0}\cos(2m\omega_s t + \frac{2\pi}{3}m) + B_{m0}\sin(2m\omega_s t + \frac{2\pi}{3}m)\right) \\
&\quad + \sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty}\left(A_{mn}\cos(2m\omega_s t + \frac{2\pi}{3}m + n\omega_r t) + B_{mn}\sin(2m\omega_s t + \frac{2\pi}{3}m + n\omega_r t)\right).
\end{aligned}
\tag{3.150}
$$

It is important to note that

$$
\cos(2m\omega_s t - \frac{2\pi}{3}m + n\omega_r t) = \begin{cases} \cos(2m\omega_s t + n\omega_r t) & \text{if } m = 3k \\ \cos(2m\omega_s t - \frac{2\pi}{3} + n\omega_r t) & \text{if } m = 3k+1 \\ \cos(2m\omega_s t + \frac{2\pi}{3} + n\omega_r t) & \text{if } m = 3k+2 \end{cases} \tag{3.151}
$$

and

$$
\sin(2m\omega_s t - \frac{2\pi}{3}m + n\omega_r t) = \begin{cases} \sin(2m\omega_s t + n\omega_r t) & \text{if } m = 3k \\ \sin(2m\omega_s t - \frac{2\pi}{3} + n\omega_r t) & \text{if } m = 3k+1 \\ \sin(2m\omega_s t + \frac{2\pi}{3} + n\omega_r t) & \text{if } m = 3k+2, \end{cases} \tag{3.152}
$$

where $k = 0, 1, 2, \ldots$.

Furthermore, for these values of k,

$$
\cos(2m\omega_s t + \frac{2\pi}{3}m + n\omega_r t) = \begin{cases} \cos(2m\omega_s t + n\omega_r t) & \text{if } m = 3k \\ \cos(2m\omega_s t + \frac{2\pi}{3} + n\omega_r t) & \text{if } m = 3k+1 \\ \cos(2m\omega_s t - \frac{2\pi}{3} + n\omega_r t) & \text{if } m = 3k+2 \end{cases} \tag{3.153}
$$

and

$$
\sin(2m\omega_s t + \frac{2\pi}{3}m + n\omega_r t) = \begin{cases} \sin(2m\omega_s t + n\omega_r t) & \text{if } m = 3k \\ \sin(2m\omega_s t + \frac{2\pi}{3} + n\omega_r t) & \text{if } m = 3k+1 \\ \sin(2m\omega_s t - \frac{2\pi}{3} + n\omega_r t) & \text{if } m = 3k+2. \end{cases} \tag{3.154}
$$

Recall that it is assumed throughout this chapter that the switching frequency is chosen high enough with respect to the highest frequency component of the reference function f_r, that harmonics of the clusters associated with different values of m do not overlap.

Based on this assumption, the Fourier series components of $s_1(t)$, $s_2(t)$ and $s_3(t)$ can be separated into three groups consisting of different clusters of harmonics. Harmonics of *type zero*, of a particular switching function, are the set of all Fourier series components for which $m = 3k$. Similarly, harmonics of *type one* and *type two* are the set of Fourier series components for which $m = 3k + 1$ and $m = 3k + 2$, respectively.

Let $\omega = 2m\omega_s + n\omega_r \geq 0$ in the following discussion. The following observations concerning the Fourier series components and the Fourier transform of s_1, s_2 and s_2 can be made:

1. The harmonics of type zero of the three switching functions s_1, s_2 and s_3 are equal in magnitude and phase. In terms of the Fourier transform of s_1, s_2 and s_3, this implies that

$$S_1(\omega) = S_2(\omega) = S_3(\omega) \tag{3.155}$$

and

$$S_1(-\omega) = S_2(-\omega) = S_3(-\omega), \tag{3.156}$$

if $m = 3k$.

2. For harmonics of type one the Fourier series components of s_2 lag those of s_1 by $\frac{2\pi}{3}$ radians, while the Fourier series components of s_3 lead those of s_1 by $\frac{2\pi}{3}$ radians. In terms of the Fourier transform, this implies that

$$S_2(\omega) = S_1(\omega)e^{-\frac{2\pi}{3}j} \text{ and } S_3(\omega) = S_1(\omega)e^{\frac{2\pi}{3}j} \tag{3.157}$$

and

$$S_2(-\omega) = S_1(-\omega)e^{\frac{2\pi}{3}j} \text{ and } S_3(-\omega) = S_1(-\omega)e^{-\frac{2\pi}{3}j}, \tag{3.158}$$

if $m = 3k + 1$.

3. Finally, for the harmonics of type two the Fourier series components of s_2 lead those of s_1 by $\frac{2\pi}{3}$ radians, while the Fourier series components of s_3 lag those of s_1 by $\frac{2\pi}{3}$ radians. In terms of the Fourier transform, this implies that

$$S_2(\omega) = S_1(\omega)e^{\frac{2\pi}{3}j} \text{ and } S_3(\omega) = S_1(\omega)e^{-\frac{2\pi}{3}j}, \tag{3.159}$$

and

$$S_2(-\omega) = S_1(-\omega)e^{\frac{-2\pi}{3}j} \text{ and } S_3(-\omega) = S_1(-\omega)e^{\frac{2\pi}{3}j}, \tag{3.160}$$

if $m = 3k + 2$.

As a result of these observations, we deduce that the Fourier series components of the d and t switching functions have the following properties:

1. Switching function $s_t = \frac{1}{3}(s_1+s_2+s_3)$ contains only Fourier series components of type zero. The Fourier series components of s_t are equal to the type zero Fourier series components of s_1. This implies that s_t contains the frequency components of the reference function as well as the switching harmonics of s_1 around integer multiples of six times the switching frequency ω_s.

2. Switching functions $s_{d_1} = \frac{1}{2}(s_1 - s_2)$ and $s_{d_2} = \frac{1}{2}(s_2 - s_3)$ consist of harmonics of types one and two. Furthermore,

$$S_{d_2}(\omega) = \begin{cases} S_{d_1}(\omega)e^{-\frac{2\pi}{3}j} & \text{if m = 3k+1} \\ S_{d_1}(\omega)e^{\frac{2\pi}{3}j} & \text{if m = 3k+2} \end{cases} \tag{3.161}$$

and

$$S_{d_2}(-\omega) = \begin{cases} S_{d_1}(-\omega)e^{\frac{2\pi}{3}j} & \text{if m = 3k+1} \\ S_{d_1}(-\omega)e^{-\frac{2\pi}{3}j} & \text{if m = 3k+2.} \end{cases} \tag{3.162}$$

3.3.3.2 Qualitative analysis

In this section the same techniques as used in the qualitative analysis of the two-level series-stacked converter are applied to study the steady-state behavior of the three-level series-stacked converter. Although the underlying methods are the same, the theory becomes somewhat more involved.

3.3.3.2.1 Steady-state analysis

As for the two-level series-stacked converter, only the case where the bus capacitance C_d is 'large' is studied analytically. It is thus assumed that voltages v_{d_1}, v_{d_2} and v_t are constant and contain only DC components with negligible high-frequency components. These DC-bus voltages will be denoted by V_{d_1}, V_{d_2} and V_t, respectively.

To study the effect of V_t on V_{d_1} and V_{d_2} it is assumed that the supply voltage v_s is zero. Refer to Figure 3.34 for the definition of impedances Z_1, Z_2 and Z_3.

By making use of the d and t circuits of Figure 3.29, the following relations are derived:

$$\begin{bmatrix} I_{d_1}(\omega) \\ I_{d_2}(\omega) \\ I_t(\omega) \end{bmatrix} = \begin{bmatrix} \frac{S_t(\omega)+S_a(\omega)}{Z_1(\omega)} & \frac{2S_{d_1}(\omega)}{3Z_1(\omega)} & \frac{S_{d_1}(\omega)}{Z_1(\omega)} \\ \frac{-2S_{d_2}(\omega)}{3Z_1(\omega)} & \frac{S_t(\omega)-S_a(\omega)}{Z_1(\omega)} & \frac{S_{d_2}(\omega)}{Z_1(\omega)} \\ \frac{8S_{d_1}(\omega)+4S_{d_2}(\omega)}{9Z_2(\omega)} & \frac{4S_{d_1}(\omega)+8S_{d_2}(\omega)}{9Z_2(\omega)} & \frac{S_t(\omega)}{Z_2(\omega)} \end{bmatrix} \begin{bmatrix} V_{d_1} \\ V_{d_2} \\ V_t \end{bmatrix}. \tag{3.163}$$

The matrix in this expression can be factored in the following way:

$$\begin{bmatrix} \frac{S_t(\omega)+S_a(\omega)}{Z_1(\omega)} & \frac{2S_{d_1}(\omega)}{3Z_1(\omega)} & \frac{S_{d_1}(\omega)}{Z_1(\omega)} \\ \frac{-2S_{d_2}(\omega)}{3Z_1(\omega)} & \frac{S_t(\omega)-S_a(\omega)}{Z_1(\omega)} & \frac{S_{d_2}(\omega)}{Z_1(\omega)} \\ \frac{8S_{d_1}(\omega)+4S_{d_2}(\omega)}{9Z_2(\omega)} & \frac{4S_{d_1}(\omega)+8S_{d_2}(\omega)}{9Z_2(\omega)} & \frac{S_t(\omega)}{Z_2(\omega)} \end{bmatrix} = ZG, \tag{3.164}$$

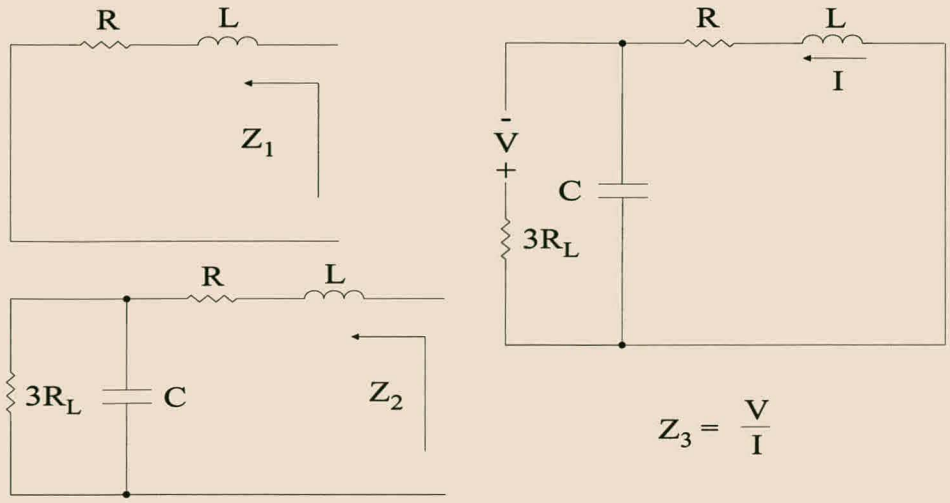


Figure 3.34: Definition of Z_1, Z_2 and Z_3 for the three-level series-stacked converter.

where Z and G are given by

$$Z = \begin{bmatrix} \frac{1}{Z_1(\omega)} & 0 & 0 \\ 0 & \frac{1}{Z_1(\omega)} & 0 \\ 0 & 0 & \frac{1}{Z_2(\omega)} \end{bmatrix} \text{ and } G = \begin{bmatrix} S_t(\omega) + S_a(\omega) & \frac{2S_{d_1}(\omega)}{3} & S_{d_1}(\omega) \\ \frac{-2S_{d_2}(\omega)}{3} & S_t(\omega) - S_a(\omega) & S_{d_2}(\omega) \\ \frac{8S_{d_1}(\omega)+4S_{d_2}(\omega)}{9} & \frac{4S_{d_1}(\omega)+8S_{d_2}(\omega)}{9} & S_t(\omega) \end{bmatrix}. \quad (3.165)$$

Furthermore, matrix Z can be written in the form

$$Z(\omega) = \frac{1}{Z_1(\omega)} L_1 + \frac{1}{Z_2(\omega)} L_2, \quad (3.166)$$

where

$$L_1 = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \text{ and } L_2 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix}. \quad (3.167)$$

The next step in the analysis is to split the switching functions of matrix G into different frequency components. Based on the remarks of the previous section, the Fourier transform $S_{d_1}(\omega)$, of switching function s_{d_1}, can be written in the form

$$S_{d_1}(\omega) = S_{d_{11}}(\omega) + S_{d_{12}}(\omega), \quad (3.168)$$

where $S_{d_{11}}(\omega)$ are the harmonic components of $S_{d_1}(\omega)$ of type one and $S_{d_{12}}(\omega)$ are the harmonic components of $S_{d_1}(\omega)$ of type two. Presenting $S_{d_2}(\omega)$ in the same way results in

$$S_{d_2}(\omega) = S_{d_{21}}(\omega) + S_{d_{22}}(\omega). \quad (3.169)$$

Furthermore, by equations 3.161 and 3.162

$$S_{d_{21}}(\omega) = \begin{cases} S_{d_{11}}(\omega) e^{-\frac{2\pi}{3}j} & \text{if } \omega \geq 0 \\ S_{d_{11}}(\omega) e^{\frac{2\pi}{3}j} & \text{if } \omega < 0 \end{cases} \quad (3.170)$$

and

$$S_{d_{22}}(\omega) = \begin{cases} S_{d_{12}}(\omega)e^{\frac{2\pi}{3}j} & \text{if } \omega \geq 0 \\ S_{d_{12}}(\omega)e^{-\frac{2\pi}{3}j} & \text{if } \omega < 0. \end{cases} \tag{3.171}$$

By making use of these decompositions of the switching functions and the fact that $S_a(\omega) = \frac{2}{3}\left(S_{d_1}(\omega) + S_{d_2}(\omega)\right)$, it follows that

$$G(w) = \begin{cases} NS_{d_{11}}(\omega) + \overline{N}S_{d_{12}}(\omega) + I_3S_t(\omega) & \text{if } \omega \geq 0 \\ \overline{N}S_{d_{11}}(\omega) + NS_{d_{12}}(\omega) + I_3S_t(\omega) & \text{if } \omega < 0, \end{cases} \tag{3.172}$$

where

$$N = \begin{bmatrix} \frac{2\left(1+e^{-\frac{2\pi j}{3}}\right)}{3} & \frac{2}{3} & 1 \\ -\frac{2e^{-\frac{2\pi j}{3}}}{3} & -\frac{2\left(1+e^{-\frac{2\pi j}{3}}\right)}{3} & e^{-\frac{2\pi j}{3}} \\ \frac{4\left(2+e^{-\frac{2\pi j}{3}}\right)}{9} & \frac{4\left(1+2e^{-\frac{2\pi j}{3}}\right)}{9} & 0 \end{bmatrix} \tag{3.173}$$

and I_3 is the identity 3×3 matrix.

The next step is to calculate currents $I_{a_1}(\omega)$, $I_{a_2}(\omega)$ and $I_{a_t}(\omega)$ (see Figure 3.29 for the definition of these currents.). By again making use of the d and t circuits of Figure 3.29, it follows that

$$\begin{bmatrix} I_{a_1}(\omega) \\ I_{a_2}(\omega) \\ I_{a_t}(\omega) \end{bmatrix} = \begin{bmatrix} S_t(\omega) + S_a(\omega) & \frac{2S_{d_1}(\omega)}{3} & S_{d_1}(\omega) \\ \frac{-2S_{d_2}(\omega)}{3} & S_t(\omega) - S_a(\omega) & S_{d_2}(\omega) \\ \frac{8S_{d_1}(\omega)+4S_{d_2}(\omega)}{9} & \frac{4S_{d_1}(\omega)+8S_{d_2}(\omega)}{9} & S_t(\omega) \end{bmatrix} \star \begin{bmatrix} I_{d_1}(\omega) \\ I_{d_2}(\omega) \\ I_t(\omega) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \frac{V_t - V_b}{R_b} \end{bmatrix}. \tag{3.174}$$

Note that multiplication has been replaced by frequency domain convolution in this equation. Equation 3.174 can be rewritten in the form

$$\begin{bmatrix} I_{a_1}(\omega) \\ I_{a_2}(\omega) \\ I_{a_t}(\omega) \end{bmatrix} = G \star \begin{bmatrix} I_{d_1}(\omega) \\ I_{d_2}(\omega) \\ I_t(\omega) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \frac{V_t - V_b}{R_b} \end{bmatrix}. \tag{3.175}$$

By making use of equations 3.163 and 3.164,

$$G \star \begin{bmatrix} I_{d_1}(\omega) \\ I_{d_2}(\omega) \\ I_t(\omega) \end{bmatrix} = G \star (ZG) \begin{bmatrix} V_{d_1} \\ V_{d_2} \\ V_t \end{bmatrix}. \tag{3.176}$$

By applying the definition of the convolution integral and making use of the fact that the switching functions have no DC components, it follows that

$$\begin{aligned} &(G \star (ZG))(\omega)|_{\omega=0} \\ &= \frac{1}{2\pi}\int_{-\infty}^{\infty} \overline{G(\xi)}Z(\xi)G(\xi)\,d\xi \\ &= \frac{1}{2\pi}\int_{0}^{\infty} \left(\overline{NS_{d_{11}}}(\xi) + N\overline{S_{d_{12}}}(\xi) + I_3\overline{S_t}(\xi)\right) Z(\xi) \left(NS_{d_{11}}(\xi) + \overline{N}S_{d_{12}}(\xi) + I_3S_t(\xi)\right) d\xi \\ &\quad + \frac{1}{2\pi}\int_{-\infty}^{0} \left(N\overline{S_{d_{11}}}(\xi) + \overline{NS_{d_{12}}}(\xi) + I_3\overline{S_t}(\xi)\right) Z(\xi) \left(\overline{N}S_{d_{11}}(\xi) + NS_{d_{12}}(\xi) + I_3S_t(\xi)\right) d\xi \end{aligned} \tag{3.177}$$

Based on the assumptions of the previous section, the contribution of all the following terms is negligible and will be ignored:

$$\begin{array}{ll}
\int_{-\infty}^{\infty} \overline{S_{d_{11}}(\xi)} S_{d_{12}}(\xi)\, d\xi & \int_{-\infty}^{\infty} \overline{S_{d_{11}}(\xi)} S_t(\xi)\, d\xi \\
\int_{-\infty}^{\infty} \overline{S_{d_{12}}(\xi)} S_{d_{11}}(\xi)\, d\xi & \int_{-\infty}^{\infty} \overline{S_{d_{12}}(\xi)} S_t(\xi)\, d\xi \\
\int_{-\infty}^{\infty} \overline{S_t(\xi)} S_{d_{11}}(\xi)\, d\xi & \int_{-\infty}^{\infty} \overline{S_t(\xi)} S_{d_{12}}(\xi)\, d\xi \\
\int_{-\infty}^{\infty} S_{d_{11}}(\xi) \overline{S_{d_{12}}}(\xi)\, d\xi & \int_{-\infty}^{\infty} S_{d_{11}}(\xi) \overline{S_t}(\xi)\, d\xi \\
\int_{-\infty}^{\infty} S_{d_{12}}(\xi) \overline{S_{d_{11}}}(\xi)\, d\xi & \int_{-\infty}^{\infty} S_{d_{12}}(\xi) \overline{S_t}(\xi)\, d\xi \\
\int_{-\infty}^{\infty} S_t(\xi) \overline{S_{d_{11}}}(\xi)\, d\xi & \int_{-\infty}^{\infty} S_t(\xi) \overline{S_{d_{12}}}(\xi)\, d\xi.
\end{array} \tag{3.178}$$

By making use of this observation, equation 3.177 can be written as

$$\begin{aligned}
(G \star (ZG))(\omega)|_{\omega=0} &= \frac{1}{2\pi} \int_0^{\infty} \left(\overline{N} Z(\xi) N \left| S_{d_{11}}(\xi) \right|^2 + N Z(\xi) \overline{N} \left| S_{d_{12}}(\xi) \right|^2 + Z(\xi) \left| S_t(\xi) \right|^2 \right) d\xi \\
&\quad + \frac{1}{2\pi} \int_{-\infty}^{0} \left(N Z(\xi) \overline{N} \left| S_{d_{11}}(\xi) \right|^2 + \overline{N} Z(\xi) N \left| S_{d_{12}}(\xi) \right|^2 + Z(\xi) \left| S_t(\xi) \right|^2 \right) d\xi.
\end{aligned} \tag{3.179}$$

Based on equation 3.166, $Z(\xi)$ can be decomposed in terms of L_1 and L_2, resulting in

$$\begin{aligned}
(G \star (ZG))(\omega)|_{\omega=0} &= \frac{1}{2\pi} \int_0^{\infty} \left(\frac{\left| S_{d_{11}}(\xi) \right|^2}{Z_1(\xi)} \overline{N} L_1 N + \frac{\left| S_{d_{11}}(\xi) \right|^2}{Z_2(\xi)} \overline{N} L_2 N \right) d\xi \\
&\quad + \frac{1}{2\pi} \int_0^{\infty} \left(\frac{\left| S_{d_{12}}(\xi) \right|^2}{Z_1(\xi)} N L_1 \overline{N} + \frac{\left| S_{d_{12}}(\xi) \right|^2}{Z_2(\xi)} N L_2 \overline{N} \right) d\xi \\
&\quad + \frac{1}{2\pi} \int_0^{\infty} \left(\frac{\left| S_t(\xi) \right|^2}{Z_1(\xi)} L_1 + \frac{\left| S_t(\xi) \right|^2}{Z_2(\xi)} L_2 \right) d\xi \\
&\quad + \frac{1}{2\pi} \int_{-\infty}^{0} \left(\frac{\left| S_{d_{11}}(\xi) \right|^2}{Z_1(\xi)} N L_1 \overline{N} + \frac{\left| S_{d_{11}}(\xi) \right|^2}{Z_2(\xi)} N L_2 \overline{N} \right) d\xi \\
&\quad + \frac{1}{2\pi} \int_{-\infty}^{0} \left(\frac{\left| S_{d_{12}}(\xi) \right|^2}{Z_1(\xi)} \overline{N} L_1 N + \frac{\left| S_{d_{12}}(\xi) \right|^2}{Z_2(\xi)} \overline{N} L_2 N \right) d\xi \\
&\quad + \frac{1}{2\pi} \int_{-\infty}^{0} \left(\frac{\left| S_t(\xi) \right|^2}{Z_1(\xi)} L_1 + \frac{\left| S_t(\xi) \right|^2}{Z_2(\xi)} L_2 \right) d\xi.
\end{aligned} \tag{3.180}$$

Calculating the different matrices in the above expression results in

$$\overline{N} L_1 N = \begin{bmatrix} \frac{2}{3}\left(1 + \frac{j}{\sqrt{3}}\right) & \frac{4}{3\sqrt{3}} j & 0 \\ -\frac{4}{3\sqrt{3}} j & \frac{2}{3}\left(1 - \frac{j}{\sqrt{3}}\right) & 0 \\ 0 & 0 & \frac{4}{3} \end{bmatrix}, \tag{3.181}$$

$$N L_2 \overline{N} = \begin{bmatrix} \frac{2}{3}\left(1 + \frac{j}{\sqrt{3}}\right) & \frac{4}{3\sqrt{3}} j & 0 \\ -\frac{4}{3\sqrt{3}} j & \frac{2}{3}\left(1 - \frac{j}{\sqrt{3}}\right) & 0 \\ 0 & 0 & 0 \end{bmatrix}, \tag{3.182}$$

$$\overline{N} L_2 N = \begin{bmatrix} \frac{2}{3}\left(1 - \frac{j}{\sqrt{3}}\right) & -\frac{4}{3\sqrt{3}} j & 0 \\ \frac{4}{3\sqrt{3}} j & \frac{2}{3}\left(1 + \frac{j}{\sqrt{3}}\right) & 0 \\ 0 & 0 & 0 \end{bmatrix}, \tag{3.183}$$

and

$$NL_1\overline{N} = \begin{bmatrix} \frac{2}{3}\left(1-\frac{j}{\sqrt{3}}\right) & -\frac{4}{3\sqrt{3}}j & 0 \\ \frac{4}{3\sqrt{3}}j & \frac{2}{3}\left(1+\frac{j}{\sqrt{3}}\right) & 0 \\ 0 & 0 & \frac{4}{3} \end{bmatrix}. \tag{3.184}$$

Define matrix P by

$$P = \begin{bmatrix} \frac{2}{3}\left(1+\frac{j}{\sqrt{3}}\right) & \frac{4}{3\sqrt{3}}j \\ -\frac{4}{3\sqrt{3}}j & \frac{2}{3}\left(1-\frac{j}{\sqrt{3}}\right) \end{bmatrix}. \tag{3.185}$$

Then $\overline{P}$ is given by

$$\overline{P} = \begin{bmatrix} \frac{2}{3}\left(1-\frac{j}{\sqrt{3}}\right) & -\frac{4}{3\sqrt{3}}j \\ \frac{4}{3\sqrt{3}}j & \frac{2}{3}\left(1+\frac{j}{\sqrt{3}}\right) \end{bmatrix}. \tag{3.186}$$

From equations 3.175 and 3.176 and the fact that the average values of i_{a_1} and i_{a_2} are zero in the steady state, it follows that

$$\begin{bmatrix} 0 \\ 0 \end{bmatrix} = \left(kP + \overline{kP} + lL_1\right) \begin{bmatrix} V_{d_1} \\ V_{d_2} \end{bmatrix}, \tag{3.187}$$

where constants k and l are given by

$$\begin{aligned} k &= \frac{1}{2\pi}\int_0^\infty \left(\frac{|S_{d_{11}}(\xi)|^2}{Z_1(\xi)} + \frac{|S_{d_{12}}(\xi)|^2}{Z_2(\xi)}\right) d\xi + \int_{-\infty}^0 \left(\frac{|S_{d_{11}}(\xi)|^2}{Z_2(\xi)} + \frac{|S_{d_{12}}(\xi)|^2}{Z_1(\xi)}\right) d\xi \\ &= \frac{1}{2\pi}\int_0^\infty \left(\frac{|S_{d_{11}}(\xi)|^2}{Z_1(\xi)} + \frac{|S_{d_{12}}(\xi)|^2}{Z_2(\xi)} + \frac{|S_{d_{11}}(\xi)|^2}{\overline{Z_2}(\xi)} + \frac{|S_{d_{12}}(\xi)|^2}{\overline{Z_1}(\xi)}\right) d\xi \end{aligned} \tag{3.188}$$

and

$$l = \frac{1}{2\pi}\int_{-\infty}^\infty \frac{|S_t(\xi)|^2}{Z_1(\xi)}\, d\xi. \tag{3.189}$$

Note that since the real parts of impedances Z_1 and Z_2 are positive, the real part of k is positive. Also note that constant l is real and positive.

Define the complex number $\alpha + j\beta$ by

$$e^{\alpha+j\beta} = \frac{k}{l}. \tag{3.190}$$

According to equation 3.187

$$\left(e^{\alpha+j\beta}P + e^{\alpha-j\beta}\overline{P} + L_1\right) \begin{bmatrix} V_{d_1} \\ V_{d_2} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}. \tag{3.191}$$

After some trigonometric manipulations, this gives rise to the following set of equations:

$$V_{d_1}\sin\beta + \frac{\sqrt{3}}{2}V_{d_2}\cos\beta + \frac{1}{2}V_{d_2}\sin\beta + \frac{3\sqrt{3}}{8e^\alpha}V_{d_2} = 0 \tag{3.192}$$

$$\frac{\sqrt{3}}{2}V_{d_1}\cos\beta - \frac{1}{2}V_{d_1}\sin\beta - V_{d_2}\sin\beta + \frac{3\sqrt{3}}{8e^\alpha}V_{d_1} = 0. \tag{3.193}$$

Multiplying equation 3.192 by V_{d_1}, equation 3.193 by V_{d_2} and subtracting the two, results in

$$V_{d_1}V_{d_2}\sin\beta + V_{d_2}^2\sin\beta + V_{d_1}^2\sin\beta = 0. \tag{3.194}$$

The following two possibilities have to be considered:

1. If $\sin\beta \neq 0$ then

$$V_{d_1}^2 + V_{d_2}^2 + V_{d_1}V_{d_2} = 0. \tag{3.195}$$

   The only solution of this equation for which both V_{d_1} and V_{d_2} are real is $V_{d_1} = V_{d_2} = 0$.

2. If $\sin\beta = 0$, then since $\cos\beta$ is positive (according to the remarks above), it follows from equation 3.193 that $V_{d_1} = 0$, while it follows from 3.192 that $V_{d_2} = 0$.

This proves that the DC-bus voltages are balanced in the steady state, under the assumptions of the previous section.

In the remainder of this section the effect of the supply voltage on the steady-state bus voltages are studied. It is assumed that the supply voltage is also periodic with frequency ω_r. This leads to the following small modifications to the theory developed so far in this section:

1. When taking the effect of $V_s(\omega)$ into account, equation 3.163 is replaced by

$$\begin{bmatrix} I_{d_1}(\omega) \\ I_{d_2}(\omega) \\ I_t(\omega) \end{bmatrix} = \begin{bmatrix} \frac{S_t(\omega)+S_a(\omega)}{Z_1(\omega)} & \frac{2S_{d_1}(\omega)}{3Z_1(\omega)} & \frac{S_{d_1}(\omega)}{Z_1(\omega)} \\ \frac{-2S_{d_2}(\omega)}{3Z_1(\omega)} & \frac{S_t(\omega)-S_a(\omega)}{Z_1(\omega)} & \frac{S_{d_2}(\omega)}{Z_1(\omega)} \\ \frac{8S_{d_1}(\omega)+4S_{d_2}(\omega)}{9Z_2(\omega)} & \frac{4S_{d_1}(\omega)+8S_{d_2}(\omega)}{9Z_2(\omega)} & \frac{S_t(\omega)}{Z_2(\omega)} \end{bmatrix} \begin{bmatrix} V_{d_1} \\ V_{d_2} \\ V_t \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \frac{V_s(\omega)}{Z_3(\omega)} \end{bmatrix}. \tag{3.196}$$

2. This leads to the following modification to equation 3.176:

$$G\star\begin{bmatrix} I_{d_1}(\omega) \\ I_{d_2}(\omega) \\ I_t(\omega) \end{bmatrix} = G\star(ZG)\begin{bmatrix} V_{d_1} \\ V_{d_2} \\ V_t \end{bmatrix} + G\star\begin{bmatrix} 0 \\ 0 \\ \frac{V_s(\omega)}{Z_3(\omega)} \end{bmatrix}. \tag{3.197}$$

   Furthermore, for $\omega = 0$,

$$G\star\begin{bmatrix} 0 \\ 0 \\ \frac{V_s(\omega)}{Z_3(\omega)} \end{bmatrix} = \begin{bmatrix} \frac{1}{2\pi}\int_{-\infty}^{\infty}\frac{\overline{V_s(\xi)}}{\overline{Z_3(\xi)}}S_{d_1}(\xi)\,d\xi \\ \frac{1}{2\pi}\int_{-\infty}^{\infty}\frac{\overline{V_s(\xi)}}{\overline{Z_3(\xi)}}S_{d_2}(\xi)\,d\xi \\ \frac{1}{2\pi}\int_{-\infty}^{\infty}\frac{\overline{V_s(\xi)}}{\overline{Z_3(\xi)}}S_t(\xi)\,d\xi \end{bmatrix}. \tag{3.198}$$

   If all the harmonic components of the supply voltage v_s are significantly lower in frequency than twice the switching frequency, then only the $I_{a_t}(\omega)$ term in equation 3.175 is affected. Since this term plays no further role in the development of the theory, it is evident that $V_{d_1} = V_{d_2} = 0$ in this case as well.

To summarize: the DC-bus voltages of the three-level series-stacked converter will balance in the steady state if the following two conditions are satisfied:

1. The switching frequency is chosen so as to be significantly higher than the highest frequency harmonic of the reference function.

2. The supply voltage does not contain any harmonics near two times the switching frequency or higher.

These are exactly the same steady-state balancing requirements as for the two-level series-stacked converter. It should, however, be noted that these are sufficient conditions for the bus voltage to balance. It is possible to find special situations where the DC-bus voltages will balance even though one or both of these conditions are violated.

3.3.3.2.2 Transient analysis

The aim of this section is to show that the three-level series-stacked converter rebalances faster under interleaved switching than under ordinary switching following a perturbation. As for the two-level series-stacked converter, only the case where the bus capacitance C_d is 'large' is studied. It is thus assumed that DC-bus voltages v_{d_1}, v_{d_2} and v_t are constant over a number of cycles of the reference signal f_r. Moreover, it is assumed that the bus voltages change so slowly, compared to the dynamics of the system, that the converter voltages and currents are essentially in the steady state.

Since only the homogeneous part of equation 3.134 is studied for voltage sources, V_b and v_s are taken as zero. In practical converters the bus resistance R_b is small and hence it is assumed that v_t is equal to zero. Furthermore, since the principle of superposition applies to the solution of the homogeneous part of 3.134, the initial value of v_{d_2} is taken as zero, while the decay of v_{d_1} is studied. Based on the fact that at high switching frequencies the behavior of the converter under interleaved switching closely approximates that under ordinary switching, it is assumed that v_{d_2} is small throughout the rebalancing process. For this reason it is assumed that $v_{d_2} = 0$. This assumption will later be confirmed through simulation.

The steps followed in the analysis are essentially the same as for the two-level series-stacked converter. The details of the analysis are, however, somewhat more complicated. As a first step, the losses in the parasitic resistors under ordinary switching are studied. In the case of ordinary switching $s_t = s_1$, while $s_{d_1} = s_{d_2} = 0$. Recall that under ordinary switching the voltages and currents in the d_2 and t circuits remain zero. By Parseval's identity the average power dissipated in resistor R of the d_1 circuit is given by

$$P_{ord} = \frac{R}{2\pi} \int_{-\infty}^{\infty} |I_{d_1}(\omega)|^2 \, d\omega$$

$$= \frac{RV_{d_1}^2}{2\pi}\int_{-\infty}^{\infty}\left|\frac{S_1(\omega)}{Z_1(\omega)}\right|^2 d\omega. \tag{3.199}$$

The next step is to calculate the total losses in the parasitic resistances under interleaved switching. These are given by

$$P_{intrl} = \frac{R}{2\pi}\int_{-\infty}^{\infty}\left(|I_{d_1}(\omega)|^2 + |I_{d_2}(\omega)|^2 + |I_t(\omega)|^2\right) d\omega. \tag{3.200}$$

Since $V_{d_2} = 0$ and $V_t = 0$, it follows from equation 3.163 that

$$I_{d_1}(\omega) = \frac{S_t(\omega) + S_a(\omega)}{Z_1(\omega)}V_{d_1} \tag{3.201}$$

$$I_{d_2}(\omega) = -\frac{2S_{d_2}(\omega)}{3Z_1(\omega)}V_{d_1} \tag{3.202}$$

$$I_t(\omega) = \frac{8S_{d_1}(\omega) + 4S_{d_2}(\omega)}{9Z_2(\omega)}V_{d_1}. \tag{3.203}$$

By making use of the frequency domain decompositions of the previous section, it follows that

$$I_{d_1}(\omega) = \frac{1}{Z_1(\omega)}\left(\frac{2\left(1+e^{-\frac{2\pi j}{3}}\right)}{3}S_{d_{11}}(\omega) + \frac{2\left(1+e^{\frac{2\pi j}{3}}\right)}{3}S_{d_{12}}(\omega) + S_t(\omega)\right)V_{d_1} \tag{3.204}$$

$$I_{d_2}(\omega) = \frac{1}{Z_1(\omega)}\left(-\frac{2e^{-\frac{2\pi j}{3}}}{3}S_{d_{11}}(\omega) - \frac{2e^{\frac{2\pi j}{3}}}{3}S_{d_{12}}(\omega)\right)V_{d_1} \tag{3.205}$$

$$I_t(\omega) = \frac{1}{Z_2(\omega)}\left(\frac{4\left(2+e^{-\frac{2\pi j}{3}}\right)}{9}S_{d_{11}}(\omega) + \frac{4\left(2+e^{\frac{2\pi j}{3}}\right)}{9}S_{d_{12}}(\omega)\right)V_{d_1} \tag{3.206}$$

if $\omega \geq 0$, while

$$I_{d_1}(\omega) = \frac{1}{Z_1(\omega)}\left(\frac{2\left(1+e^{\frac{2\pi j}{3}}\right)}{3}S_{d_{11}}(\omega) + \frac{2\left(1+e^{-\frac{2\pi j}{3}}\right)}{3}S_{d_{12}}(\omega) + S_t(\omega)\right)V_{d_1} \tag{3.207}$$

$$I_{d_2}(\omega) = \frac{1}{Z_1(\omega)}\left(-\frac{2e^{\frac{2\pi j}{3}}}{3}S_{d_{11}}(\omega) - \frac{2e^{-\frac{2\pi j}{3}}}{3}S_{d_{12}}(\omega)\right)V_{d_1} \tag{3.208}$$

$$I_t(\omega) = \frac{1}{Z_2(\omega)}\left(\frac{4\left(2+e^{\frac{2\pi j}{3}}\right)}{9}S_{d_{11}}(\omega) + \frac{4\left(2+e^{-\frac{2\pi j}{3}}\right)}{9}S_{d_{12}}(\omega)\right)V_{d_1} \tag{3.209}$$

if $\omega < 0$.

From equation 3.200 and by neglecting terms from 3.178, it follows that

$$\begin{aligned} P_{intrl} &= \frac{RV_{d1}^2}{2\pi}\int_{-\infty}^{\infty}\left(\overline{I_{d_1}(\omega)}I_{d_1}(\omega) + \overline{I_{d_2}(\omega)}I_{d_2}(\omega) + \overline{I_t(\omega)}I_t(\omega)\right) d\omega \\ &= \frac{RV_{d1}^2}{2\pi}\int_{-\infty}^{\infty}\frac{1}{|Z_1(\omega)|^2}\left(\frac{8}{9}|S_{d_{11}}|^2 + \frac{8}{9}|S_{d_{12}}|^2 + |S_t|^2\right) d\omega \\ &\quad + \frac{16}{27}\frac{RV_{d1}^2}{2\pi}\int_{-\infty}^{\infty}\frac{1}{|Z_2(\omega)|^2}\left(|S_{d_{11}}|^2 + |S_{d_{12}}|^2\right) d\omega. \end{aligned} \tag{3.210}$$

The Fourier transform $S_1(\omega)$, of switching function s_1, can also be written in the form

$$S_1(\omega) = S_{11}(\omega) + S_{12}(\omega) + S_t(\omega), \tag{3.211}$$

where $S_{11}(\omega)$ are the harmonic components of type one and $S_{12}(\omega)$ are the harmonic components of type two. Furthermore,

$$S_{d_{11}}(\omega) = \frac{1}{2}\left(S_{11}(\omega) - S_{21}(\omega)\right) \tag{3.212}$$

and by equations 3.157 and 3.158

$$S_{21}(\omega) = \begin{cases} S_{11}(\omega)e^{\frac{-2\pi j}{3}} & \text{if } \omega \geq 0 \\ S_{11}(\omega)e^{\frac{2\pi j}{3}} & \text{if } \omega < 0, \end{cases} \tag{3.213}$$

from which it follows that

$$|S_{d_{11}}(\omega)|^2 = \frac{1}{4}\left|1 - e^{\pm j\frac{2\pi}{3}}\right|^2 |S_{11}(\omega)|^2 = \frac{3}{4}|S_{11}(\omega)|^2. \tag{3.214}$$

By the same argument

$$|S_{d_{12}}(\omega)|^2 = \frac{3}{4}|S_{12}(\omega)|^2. \tag{3.215}$$

It now follows from equation 3.210 that

$$\begin{aligned} P_{intrl} &= \frac{RV_{d1}^2}{2\pi}\int_{-\infty}^{\infty}\frac{1}{|Z_1(\omega)|^2}\left(\frac{2}{3}|S_{11}(\omega)|^2 + \frac{2}{3}|S_{12}(\omega)|^2 + |S_t(\omega)|^2\right)d\omega \\ &\quad + \frac{RV_{d1}^2}{2\pi}\frac{4}{9}\int_{-\infty}^{\infty}\frac{1}{|Z_2(\omega)|^2}\left(|S_{11}(\omega)|^2 + |S_{12}(\omega)|^2\right)d\omega. \end{aligned} \tag{3.216}$$

As in the case of the two-level series-stacked converter $|Z_2(\omega)| \leq |Z_1(\omega)|$ over the frequency domain in question (see Figure 3.17). This implies that

$$\begin{aligned} P_{intrl} &\geq \frac{RV_{d1}^2}{2\pi}\int_{-\infty}^{\infty}\frac{1}{|Z_1(\omega)|^2}\left(\frac{2}{3}|S_{11}(\omega)|^2 + \frac{2}{3}|S_{12}(\omega)|^2 + |S_t(\omega)|^2\right)d\omega \\ &\quad + \frac{RV_{d1}^2}{2\pi}\frac{4}{9}\int_{-\infty}^{\infty}\frac{1}{|Z_1(\omega)|^2}\left(|S_{11}(\omega)|^2 + |S_{12}(\omega)|^2\right)d\omega \\ &= \frac{RV_{d1}^2}{2\pi}\int_{-\infty}^{\infty}\frac{1}{|Z_1(\omega)|^2}\left(\frac{10}{9}|S_{11}(\omega)|^2 + \frac{10}{9}|S_{12}(\omega)|^2 + |S_t(\omega)|^2\right)d\omega \\ &\geq \frac{RV_{d1}^2}{2\pi}\int_{-\infty}^{\infty}\frac{1}{|Z_1(\omega)|^2}\left(|S_{11}(\omega)|^2 + |S_{12}(\omega)|^2 + |S_t(\omega)|^2\right)d\omega. \end{aligned} \tag{3.217}$$

Finally, by again neglecting the orthogonal terms, it follows that

$$\begin{aligned} \int_{-\infty}^{\infty}\frac{1}{|Z_1(\omega)|^2}\left(|S_{11}(\omega)|^2 + |S_{12}(\omega)|^2 + |S_t(\omega)|^2\right)d\omega &\geq \int_{-\infty}^{\infty}\frac{1}{|Z_1(\omega)|^2}|S_{11}(\omega) + S_{12}(\omega) + S_t(\omega)|^2\,d\omega \\ &= \int_{-\infty}^{\infty}\frac{1}{|Z_1(\omega)|^2}|S_1(\omega)|^2\,d\omega, \end{aligned} \tag{3.218}$$

which proves that $P_{intrl} \geq P_{ord}$.

This shows that the DC-bus voltages of the three-level series-stacked converter rebalances more quickly under interleaved switching than under ordinary switching.

As for the two-level series-stacked converter there are also other balancing mechanisms that play a role in rebalancing when interleaved switching is applied. Recall that these include:

1. Losses in the bus resistance R_b due to ripple currents;
2. Losses in the load due to harmonics associated with s_{d_1} and s_{d_2} propagating to the load.

3.3.4 Quantitative analysis

The quantitative analysis of the three-level series-stacked converter is almost identical to that of the two-level series-stacked converter presented in section 3.2.4.4. One difference is that for the three-level series-stacked converter matrix M (see equation 3.112) has seven eigenvalues $\sigma_1, \sigma_2, \ldots \sigma_7$. For most practical three-level series-stacked converters the time constant associated with the DC-bus rebalancing is the largest. Hence

$$\tau = \max\left(\tau_1, \tau_2, \ldots, \tau_7\right), \tag{3.219}$$

where

$$\tau_i = -\frac{T_r}{\mathrm{Re}(\log(\sigma_i)}, \quad \text{for} \quad i = 1, \ldots, 7 \tag{3.220}$$

is the time constant associated with the DC-bus rebalancing process. Recall that T_r is the period of the reference function. Furthermore, by [7], theorem 9.5,

$$\frac{1}{\tau_1} + \frac{1}{\tau_2} + \cdots + \frac{1}{\tau_7} = -\mathrm{trace}\,(A) = 3\frac{R}{L} + \frac{3}{R_b C_d} + \frac{1}{3R_l C}. \tag{3.221}$$

For the steady-state analysis exactly the same steps as given in section 3.2.4.4 are followed. To summarize:

1. The behavior of the three-level series-stacked converter is simulated over one cycle of the reference function with initial condition $x(0) = 0$. The solution is stored and the value of $x(T_r)$ is extracted.
2. At the same time the fundamental matrix $\Phi(t)$ is calculated. Vector $x_p(0)$ is then calculated by making use of equation 3.121. Using $x_p(0)$ as initial condition, equation 3.80 is solved numerically over one cycle of $f_r(t)$ to obtain the steady-state solution.

Parameter	Symbol	Value
Bus Capacitance	C_d	30 mF
Filter Inductance	L	300 μH
Filter Capacitance	C	200 μF
Parasitic Resistance	R	0.01 Ω
Load Resistance	R_l	1 Ω
Bus bar Resistance	R_b	1 mΩ
Switching Frequency	f_s	1000 Hz
DC-bus Supply Voltage	V_b	2400 V
Supply Voltage	v_s	$300\cos(2\pi \cdot 50t)$

Table 3.6: Parameters of the three-level series-stacked converter used in the simulations.

3.3.5 Simulation results

In this section numerical simulations are used to study the behavior of the three-level series-stacked converter under interleaved switching. All the simulations are based on the numerical techniques derived in this chapter.

The converter parameters are given in Table 3.6. Unless stated otherwise these converter parameters will be used throughout the remainder of this chapter. They are almost identical to those of the two-level series-stacked converter given in Table 3.3. The only difference is that for the three-level series-stacked converter the total DC-bus voltage V_b is increased from 1600 V to 2400 V. The reference function

$$f_r(t) = 0.7\cos(2\pi \cdot 50t) + 0.2\cos(2\pi \cdot 150t) \tag{3.222}$$

is used throughout.

As a first step the transient behavior of the three-level series-stacked converter is analyzed. It is shown that the converter rebalances faster under interleaved switching than under ordinary switching, as predicted by the theory. It is further shown that the time constant τ associated with the balancing process decreases with decreasing switching frequency.

In the second part of this section the steady-state behavior of the three-level series-stacked converter is studied. It is shown that the different capacitor voltages and inductor currents balance in the steady state if the theoretical balancing conditions are adhered to. Finally, some of the implications of using a digital controller to generate the PWM switching functions are studied through simulation.

Parameter	Symbol	Value
Initial Inductor Current 1	$i_{d_1}(0)$	50 A
Initial Inductor Current 2	$i_{d_2}(0)$	0 A
Initial Inductor Current 3	$i_t(0)$	0 A
Initial Capacitor Voltage 1	$v_{d_1}(0)$	100 V
Initial Capacitor Voltage 2	$v_{d_2}(0)$	50 V
Initial Capacitor Voltage 3	$v_t(0)$	0 V
Initial Output Voltage	$v_0(0)$	0 V

Table 3.7: Initial conditions used in the simulations.

3.3.5.1 Transient analysis

In this section the transient behavior of the three-level series-stacked converter under interleaved switching is studied. Recall that only solutions of the homogeneous part of equation 3.134 are studied and that V_b and v_s are taken as zero.

Example 3.12

In this example the rebalancing process of the three-level series-stacked converter under interleaved switching is studied. Table 3.7 gives the initial conditions.

Figure 3.35 shows currents i_{d_1}, i_{d_2} and i_t and voltages v_{d_1}, v_{d_2} and v_t. The theoretical envelopes associated with the rebalancing process are shown for voltages v_{d_1} and v_{d_2}. Time constant τ associated with the rebalancing process equals 0.12 s. Note that current i_t and voltage v_o are relatively small compared to i_{d_1}, i_{d_2}, v_{d_1} and v_{d_2}. Recall that these waveforms can be seen as the effect of unbalance on the steady-state values of i_t and v_o.

Example 3.13

In this example the rebalancing of the three-level series-stacked converter under interleaved switching is compared to that under ordinary switching. The same parameters as in the previous example are used, but the switching frequency is decreased to 250 Hz. At a switching frequency of 1 kHz the difference between the rebalancing properties of the two cases is very small.

Figure 3.36 shows the results of the simulation. Time constant τ is equal to 0.12 s for ordinary switching and decreases to 0.10 s for interleaved switching. This decrease in time constant can

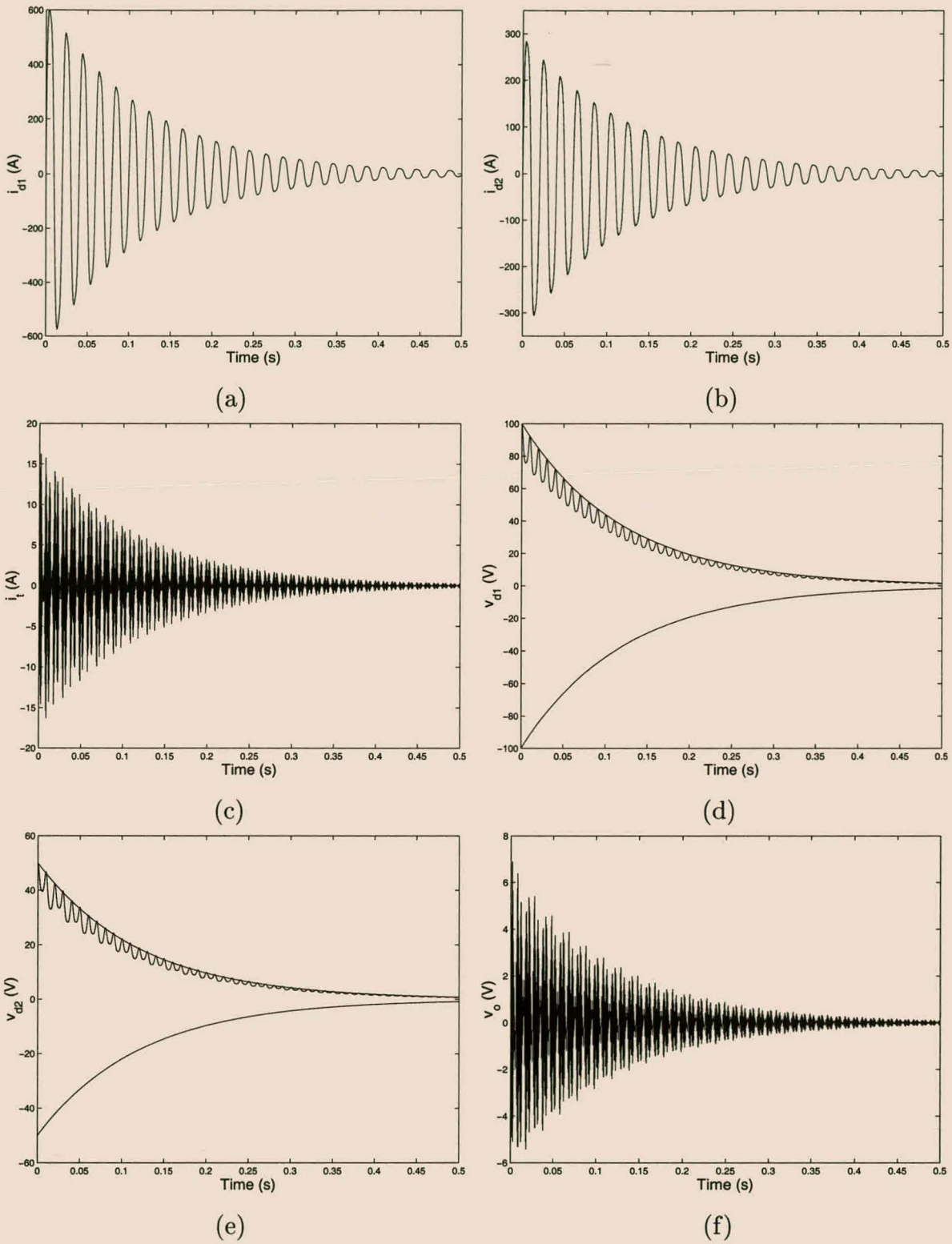


Figure 3.35: Voltage and current waveforms of a three-level series-stacked converter during rebalancing.

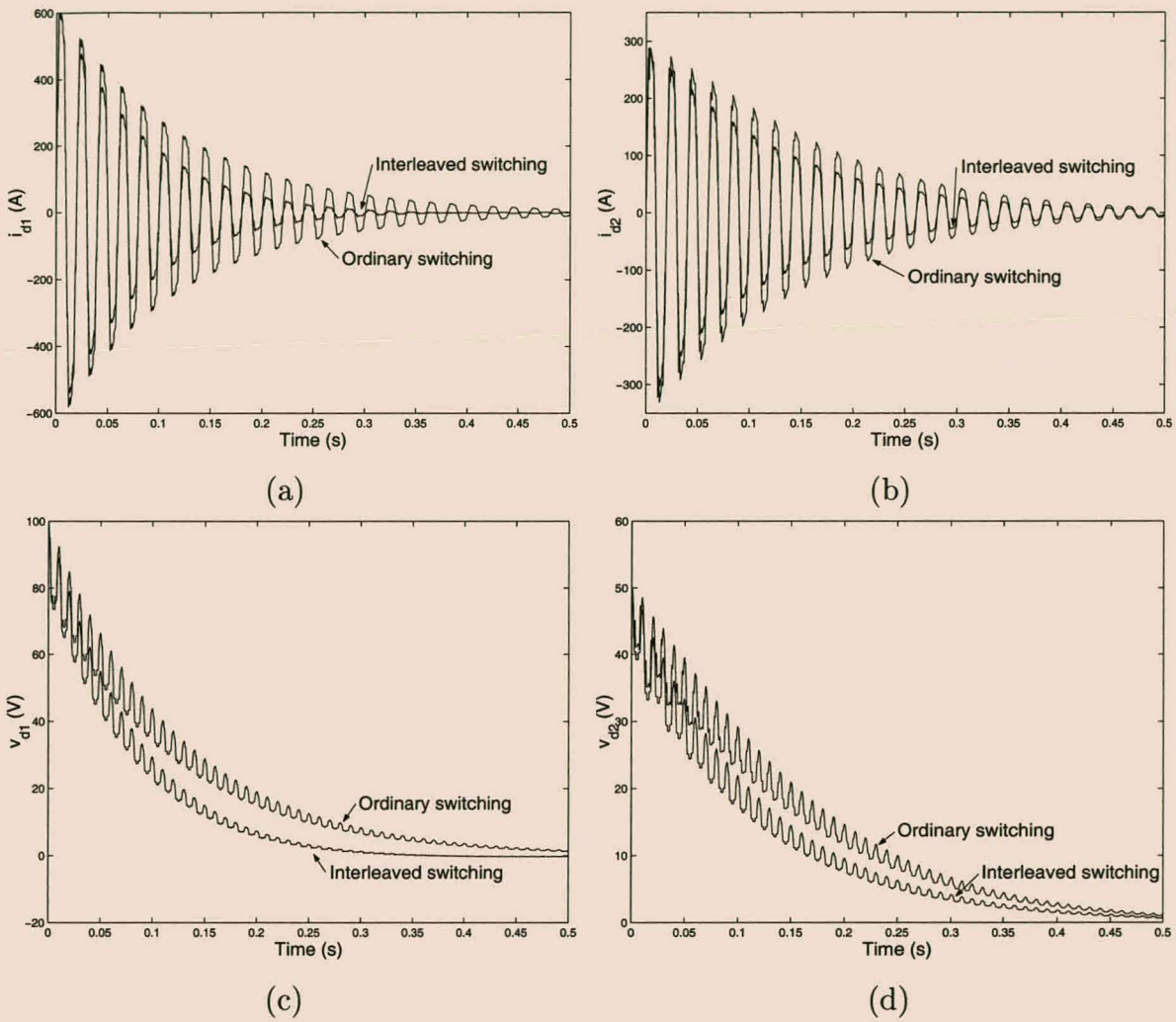


Figure 3.36: Comparison of the rebalancing of a three-level series-stacked converter under ordinary and interleaved switching.

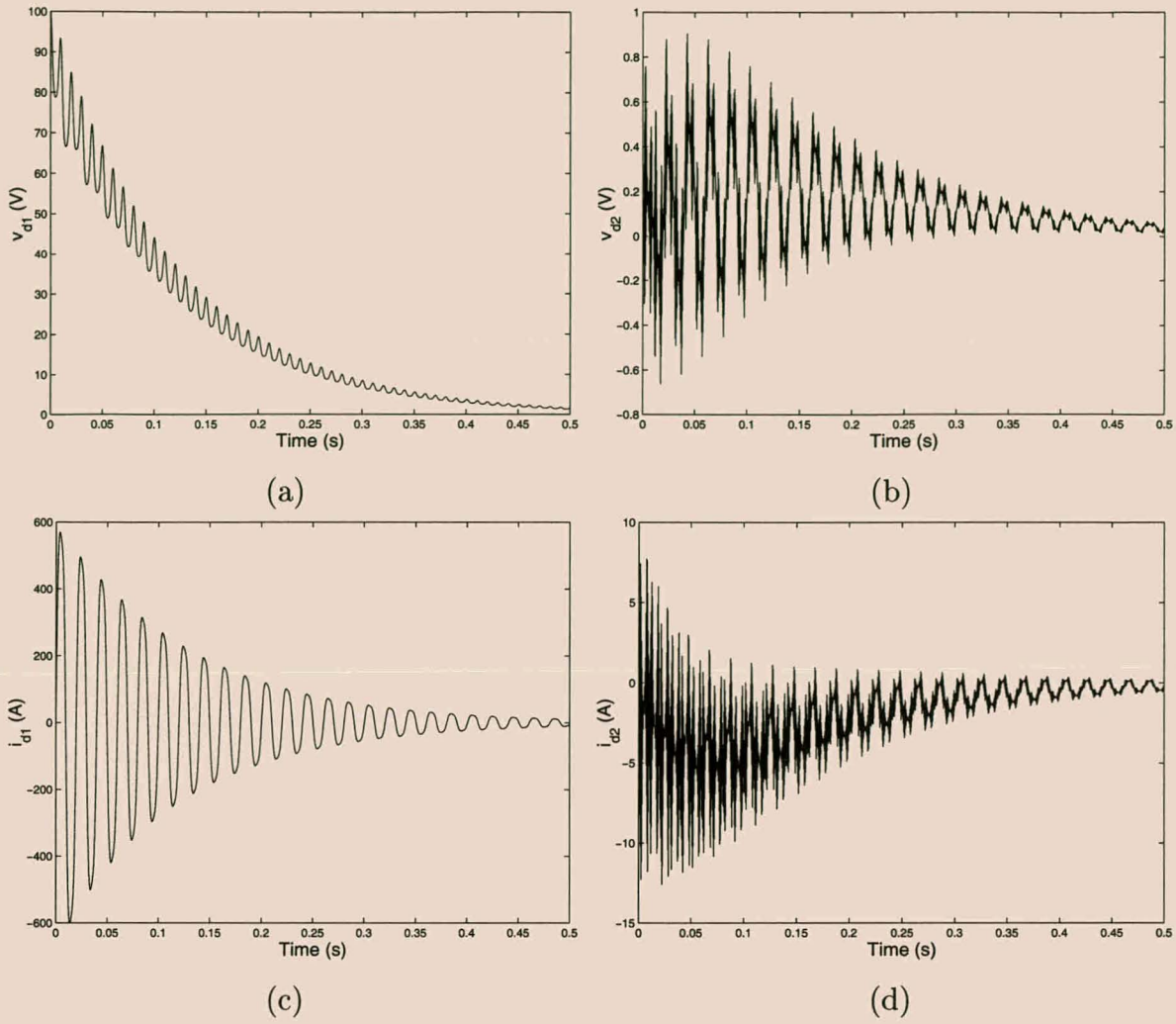


Figure 3.37: Effect of v_{d_1} on v_{d_2} and i_{d_2} during the rebalancing process.

mainly be attributed to energy being dissipated in the load resistance. Also note that, compared to the previous example, τ decreased from 0.12 s to 0.10 s under interleaved switching due to the decrease in switching frequency from 1000 Hz to 250 Hz.

Example 3.14

In this example it is shown that voltage v_{d_1} has little effect on v_{d_2} and i_{d_2} during the rebalancing process. This was mentioned in the theoretical analysis of section 3.3.3.2.2 and requires verification.

The same converter parameters as in the first example of this section are used, but with different initial conditions. In this example all initial conditions are zero except for voltage v_{d_1} which is equal to 100 V.

Figure 3.37 shows the results of the simulation. The peak magnitude of current i_{d_2} is 12.5 A, compared to 600 A for i_{d_1}, while the peak magnitude of v_{d_2} is 0.9 V compared to 100 V for v_{d_1}. This confirms the assumptions made in the theoretical analysis.

3.3.5.2 Steady-state analysis

Example 3.15

The aim of this example is to show that the DC-bus voltages of the three-level series-stacked converter are balanced in the steady state if the reference function and the supply voltage do not contain any frequency components near or above the switching frequency. The simulation parameters are the same as mentioned at the beginning of this section.

Figure 3.38 shows the results of the simulation. Note that voltages v_{d_1} and v_{d_2} are small compared to currents i_{d_1} and i_{d_2}. This is a result of the phase difference in the ripple currents of the three filter inductors. The average values of all the voltages and currents shown in Figure 3.38 are small. The largest average value is that of i_{d_1} which is equal to -1.2 A. This can be attributed to inaccuracies associated with the numerical integration process.

Example 3.16

At high power levels the total cost of the converter, filter components and injection transformer justifies the use of a high-performance digital controller. In this example some of the consequences of using a digital controller are studied.

The converter control algorithm typically consists of an inner-loop current controller and an outer-loop voltage controller. The output of the control algorithm is a reference signal that is used as input for a pulse width modulator. This pulse width modulator may be implemented through standard analog circuitry or through the use of high-frequency digital counters. One of the key features of the digital controller is the fact that this reference function can only be updated at discrete time intervals. The duration of these time intervals is limited by the speed of the controller and the complexity of the control algorithm. To prevent multiple crossings between the carrier and reference functions, the reference function is usually updated once or twice per switching period.

A simplified model of the digital modulation strategy that will be applied to the practical converter (see Chapter 4) is shown in Figure 3.39. To simplify the analysis the output of the control algorithm is modeled as a continuous reference function $f_r(t)$, which is sampled at discrete time intervals. The reference function $f_r(t)$ is applied to three sample and hold registers. The output of each sample and hold register serves as input to a pulse width modulator. Based on the theory of section 3.3.3.1, the three triangular carrier functions of the three PWM

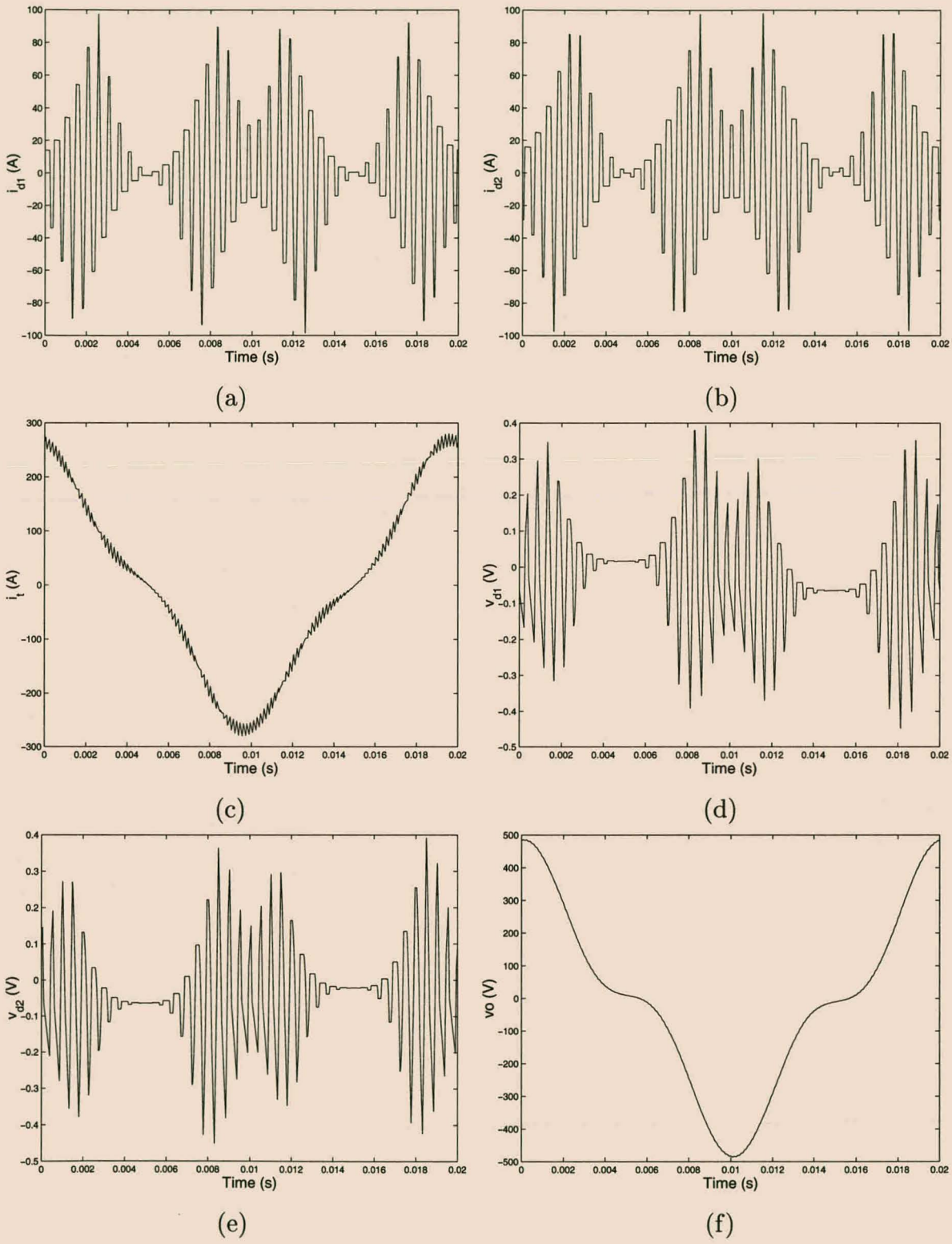


Figure 3.38: Steady-state voltage and current waveforms of the three-level series-stacked converter.

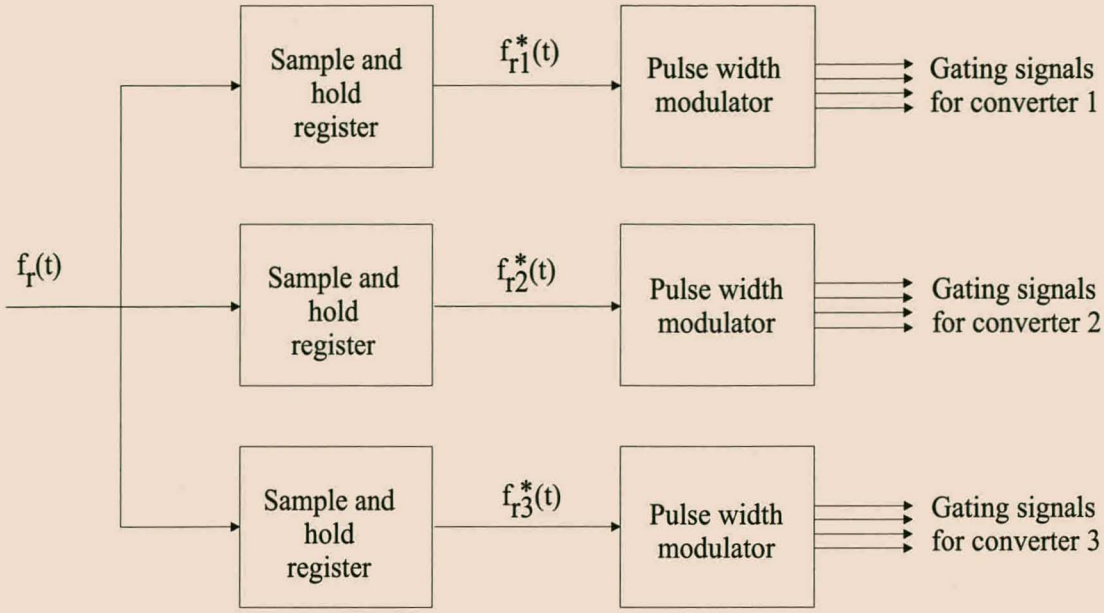


Figure 3.39: Simplified model of digital pulse width modulation.

modulators are phase shifted by $\frac{\pi}{3}$ radians. The sample and hold register associated with a particular PWM modulator is synchronized to its triangular carrier and $f_r(t)$ is sampled at every zero crossing of the carrier signal. It is well-known that the sample and hold register introduces harmonics around integer multiples of the sampling frequency which is equal to twice the switching frequency.

Figure 3.40 shows the Fourier transforms of the different switching functions resulting from this modulation strategy. The following observations concerning the Fourier transforms of the switching functions can be made from these results:

1. The magnitudes of $S_1(\omega)$, $S_2(\omega)$ and $S_3(\omega)$ are equal and contain harmonics of type zero, one and two.

2. The magnitudes of $S_{d_1}(\omega)$ and $S_{d_2}(\omega)$ are also equal and contain harmonics of type one and two, but not of type zero.

3. $S_t(\omega)$ contains only harmonics of type zero.

According to the theory these three properties guarantee balanced capacitor voltages in the steady state.

Although these properties were formally proven for a continuous reference function applied to an analog PWM modulator, it is important to note that they also hold in this example. A formal proof that these properties are in general true when using the digital modulation strategy could not be found. The properties were, however, verified for a number of different reference functions and are believed to be true in general.

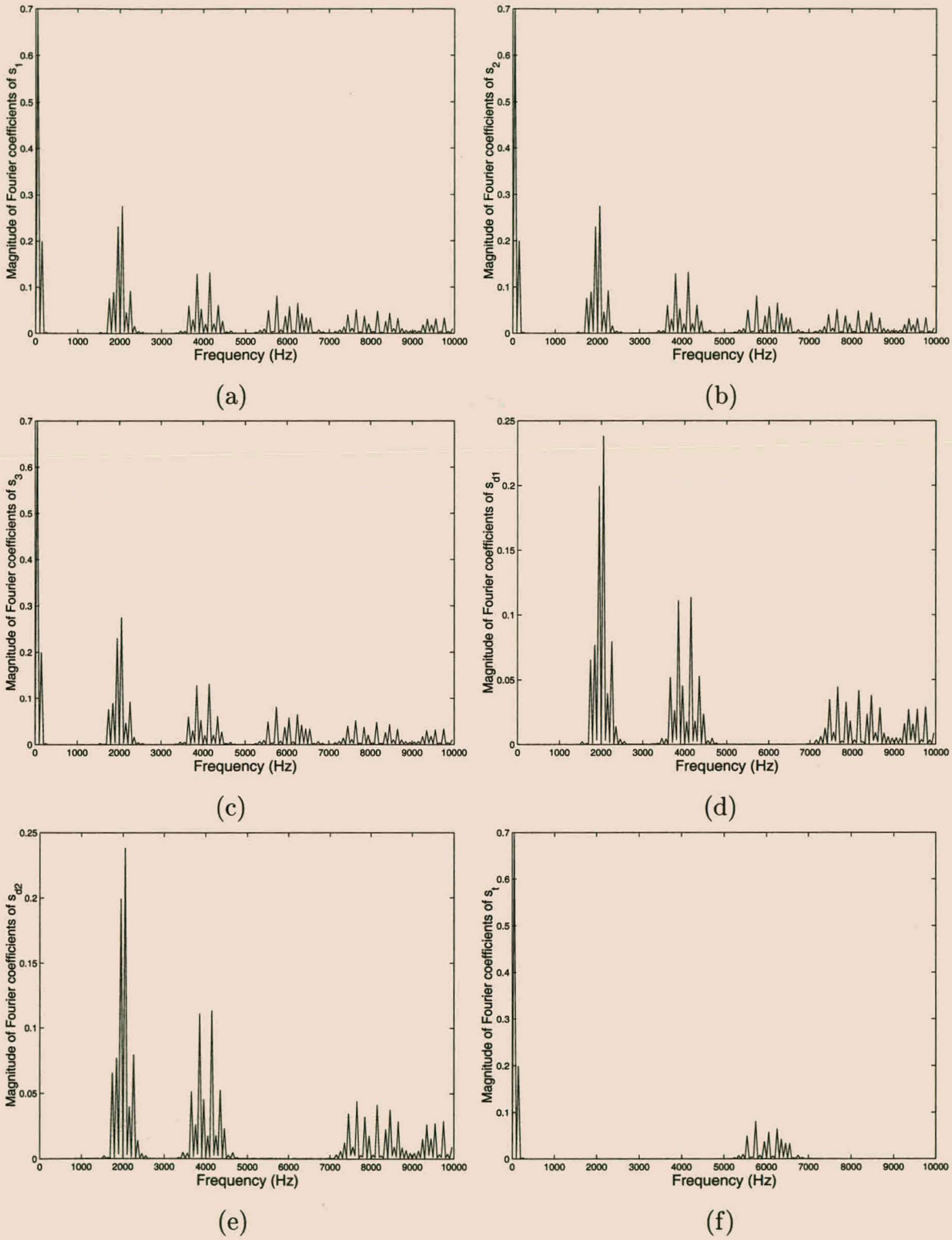


Figure 3.40: Harmonics of the different switching functions.

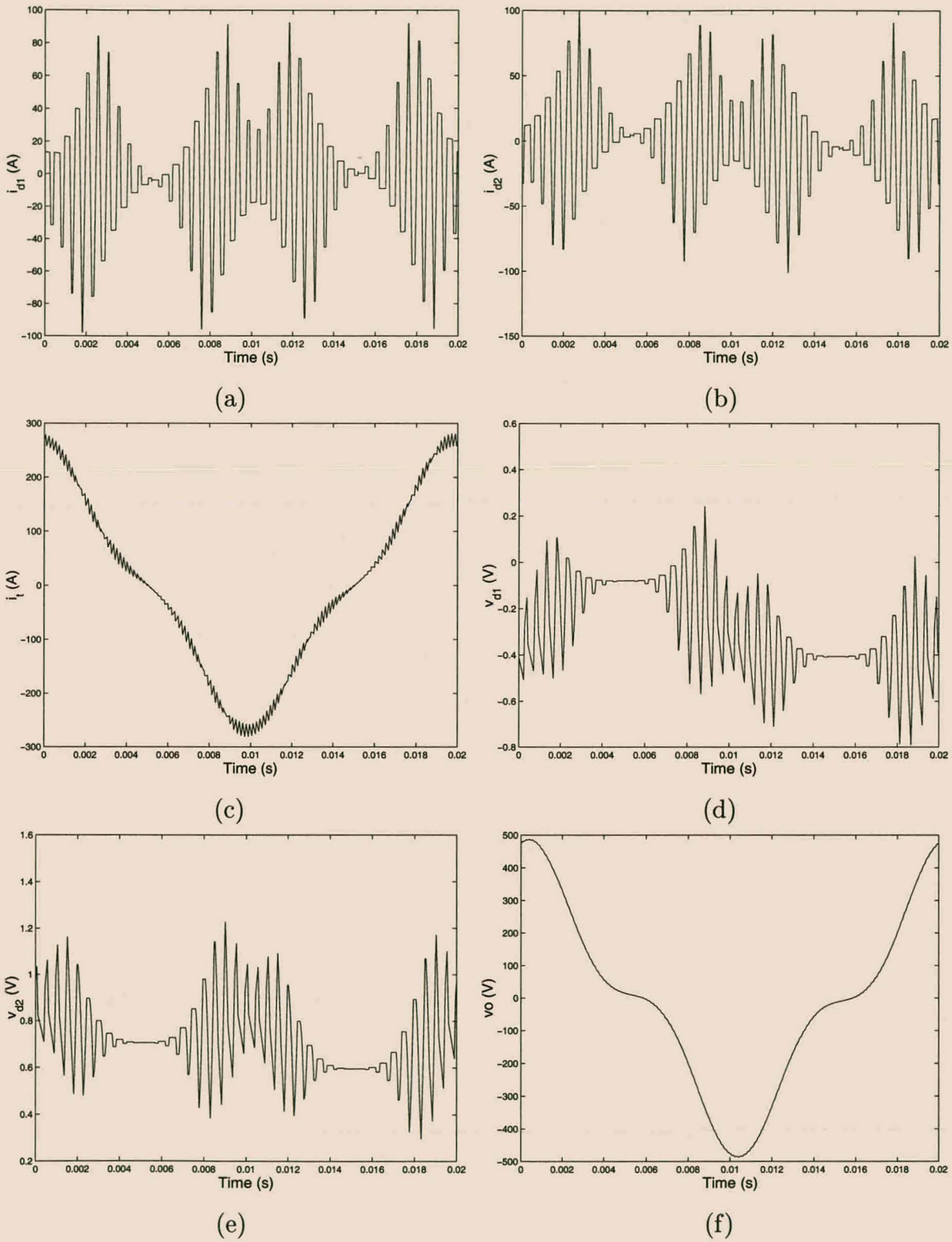


Figure 3.41: Steady-state voltage and current waveforms of a three-level series-stacked converter with a digital controller.

Figure 3.41 shows the steady-state voltage and current waveforms. These agree almost exactly with the results of Figure 3.38, which shows that the digital controller has little effect on the steady-state behavior of the three-level series-stacked converter.

3.4 Summary

The aim of this chapter was to study the balancing properties of two and three-level series-stacked converters by making use of basic circuit theory and the theory of systems of linear differential equations. The original circuits were transformed to the so-called d and t circuits. This facilitates the analysis of the balancing properties.

In the first part of the analysis the behavior of the series-stacked converter under ordinary switching was studied. By making use of a Liapunov function it was shown that the converter is stable under all operating conditions. The DC-bus balancing is due to energy being dissipated through parasitic losses. These losses can be separated in two different components:

1. Losses due to the 'low-frequency fundamental' currents in the d circuit. This component depends mainly on the reference signal.

2. Losses due to ripple current. This component depends on the switching frequency. In most cases the system will rebalance more quickly at lower switching frequencies.

After a perturbation the converter will return to its equilibrium point of balanced capacitor voltages and inductor currents. The time constant of this rebalancing is obtained by making use of Floquet theory. By studying the lossless case an important design guideline was derived to reduce oscillations of the DC-bus voltages. A time effective numerical method for studying the rebalancing mechanisms was derived.

In the second part of the analysis the rebalancing mechanisms when applying interleaved switching were studied. The harmonic spectrums of the d and t switching functions are studied for reference signals that are not necessarily sinusoidal. It is then shown that at relatively high switching frequencies the behavior of the two and three-level series-stacked converters is insensitive to the modulation method (interleaved or ordinary switching).

It is shown that the first of the two rebalancing mechanisms is unaffected by interleaved switching. However, when using interleaved switching, harmonics will propagate to the load and through the DC supply. This leads to an increase in the dissipation of energy associated with the balancing process and gives rise to a reduction in the balancing time constant.

Although the converters recover more quickly under interleaved switching, the DC-bus voltages may be unbalanced in the steady state if one or more of the following two conditions are satisfied:

1. The harmonic spectra of the d switching functions overlap with the spectrum of the t switching function in the frequency domain.

2. The harmonic spectra of the d switching functions and the spectrum of the supply voltage v_s overlap in the frequency domain.

The key to avoiding both these conditions is to choose the switching frequency significantly higher than the highest frequency harmonic of the converter reference signal f_r and of the supply voltage v_s. Harmonic currents drawn by non-linear loads can also be modeled as high-frequency components of the supply voltage.

Finally numerical methods were derived to study both the transient and steady-state behavior of the two and three-level series-stacked converters. These methods were then applied to a number of examples.

Chapter 4

An experimental series-stacked converter

4.1 Introduction

This chapter describes the design and experimental evaluation of a 700 kVA three-level series stacked phase-arm, intended for use as a series-injection power quality compensator. In the first part of the chapter the design of the converter is discussed. The aim is to provide a 'system level' design overview without describing the finer details of all the system components.

In the second part of the chapter an experimental evaluation of the converter is carried out. The main focus of this evaluation is to verify the theory of Chapter 3. Both the transient and steady-state balancing properties are evaluated and compared with the theoretical analysis.

4.2 System overview

This section provides an overview of the 700 kVA phase-arm and its control and measurement system. As mentioned in Chapter 1, the phase-arm is intended for use as a series-injection power quality device. It is designed to interface with a superconducting magnetic energy storage device, which provides a regulated DC-bus at 2.4 kV. This voltage rating is achieved by stacking three standard 800 V full-bridge converters in series. The experimental version of the phase-arm is designed to operate under both ordinary and interleaved switching.

Although the power electronic converters of the phase-arm were designed for the full 700 kVA rating, it was decided to use an injection transformer with a 70 kVA rating. This decision was based purely on financial considerations. However, when used as a dip compensator, the thermal rating of the full-scale injection transformer may be reduced. The availability of suitable loads

Parameter	Value
Nominal DC-bus Voltage	2 400 V
Maximum DC-bus Voltage	2 700 V
Control Bandwidth	650 Hz
Output Voltage	230 V (RMS)
Output Current	3043 A (RMS)
Output Current Laboratory Prototype	304 A (RMS)
Switching Frequency	2500 Hz
Maximum Duty Cycle	85%
Maximum Ambient Temperature	40°C

Table 4.1: Design parameters of the 700 kVA phase-arm.

and a step-up transformer to provide the 2.4 kV DC-link (at 700 kVA) also proved to be a problem. It will, however, be shown experimentally that the phase-arm can operate at its rated voltage. Each of the three full-bridge converters was tested at its rated current before assembling the stacked converter.

Table 4.1 summarizes the design parameters for the experimental 700 kVA phase-arm. The output voltage and load current ratings of 230 V (RMS) and 3043 A (RMS) are for sinusoidal 50 Hz voltage and current waveforms. The phase-arm is designed to inject voltage components up to the 13th harmonic. Hence the 'control bandwidth' is specified as 650 Hz. In terms of the design criteria of Chapter 3, the effective switching frequency (twice the switching frequency) must be chosen significantly greater than the highest frequency harmonic of the reference function. It was thus decided to choose a switching frequency of 2 500 Hz. The design of the system is based on a maximum duty cycle of 85%.

Each of the three full-bridge converters of the series-stacked phase-arm provides one third of the total converter VA rating of 700 kVA. Hence each full-bridge converter has a rating of 233 kVA and operates at a nominal DC-bus voltage of 800 V. Since the maximum duty cycle is 85% the nominal sinusoidal output voltage of each full-bridge converter is 480 V (RMS). Hence each full-bridge converter has a nominal sinusoidal current rating of 485 A (RMS). The experimental 700 kVA phase-arm is designed for a maximum ambient temperature of 40°C. Designing for higher ambient temperatures resulted in a marked increase in the cost of the system.

Figure 4.1 is a block diagram of the 700 kVA phase-arm with its control and measurement system. An electrically isolated voltage and current measurement system was developed to prevent problems associated with EMI. This measurement system was also used on the $\frac{1}{10}$th scale model of the full series-shunt compensator. A PEC-31 controller (see [63]) serves as the primary controller for the phase-arm. This controller was developed at the University of

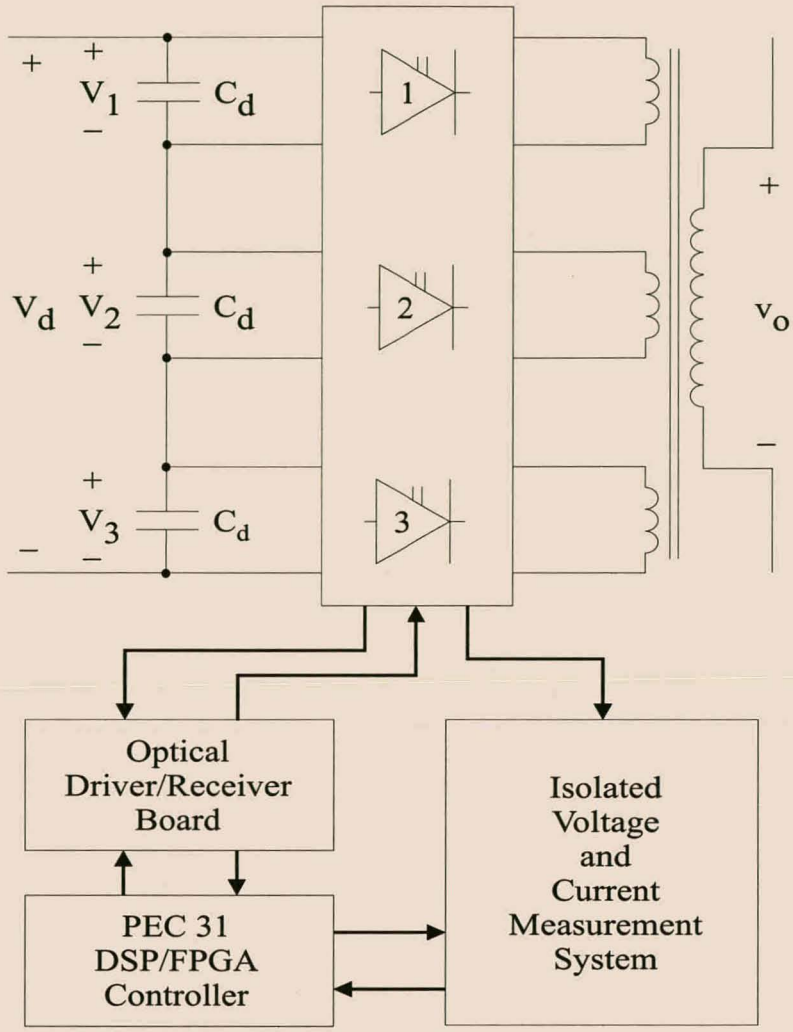


Figure 4.1: Block diagram of the phase-arm with the controller and measurement system.

Stellenbosch and contains a TMS320C31 floating point DSP as well as an 81500 series FPGA from ALTERA. The FPGA is used as a PWM generator while the control algorithms are implemented in the DSP.

An optical driver and receiver board was developed to act as interface between the FPGA and the optically isolated gate-drive circuits of the three full-bridge converters. The controller, measurement system and optical driver and receiver board were designed to accommodate a full three-phase converter based on three individual three-level series-stacked phase-arms.

4.3 Design and description of the system components

In this section the individual system components are described. These include the injection transformer, the full-bridge converter building blocks, the output filter, the measurement system and the optical driver and receiver board.

Parameter	Value
Number of Primaries	3
Primary Voltage Rating	480 V (RMS)
Current Rating per Primary	486 A (RMS)
Secondary Voltage Rating	230 V
Secondary Current	3043 A

Table 4.2: Design parameters of the full-scale injection transformer.

4.3.1 The injection transformer

In this section the properties of the injection transformer are discussed. As a first step the voltage and current ratings of the full-scale injection transformer are presented. This is followed by a discussion of parameters of the $\frac{1}{10}$th scale model injection transformer.

Table 4.2 summarizes the properties of the full-scale series-injection transformer. A number of factors should be kept in mind when designing the injection transformer:

1. The winding ratio of the transformer should be designed to meet the specific application. If the device is designed to act as an active filter or compensate for dips of limited depth, the winding ratio may be increased. For the experimental phase-arm the secondary voltage rating was chosen to be equal to the nominal line to neutral voltage of the system it is intended for. It was also decided to incorporate a 115 V tap on the secondary.

2. The thermal rating of the transformer depends on the application. If the series-injection device is equipped with a bypass switch, which only opens when a dip is detected, the thermal rating of the transformer can be reduced. However, care should be taken to keep the leakage inductance small. Excessive leakage inductance will lead to a voltage drop across the transformer, which can only be compensated for by increasing the rating of the power electronic converter.

3. In some applications the leakage inductance of the injection transformer may also be used as the filter inductance of the power electronic converter. In this case the leakage inductance should be chosen and designed carefully. This will give rise to high-frequency ripple currents flowing through the windings of the transformer. These ripple currents will lead to increased losses.

4. The isolation of the transformer should be designed to handle the high voltage transients associated with the switching of the power electronic converters. If ordinary switching is applied, these rapid changes in voltage occur between ground and each of the primary

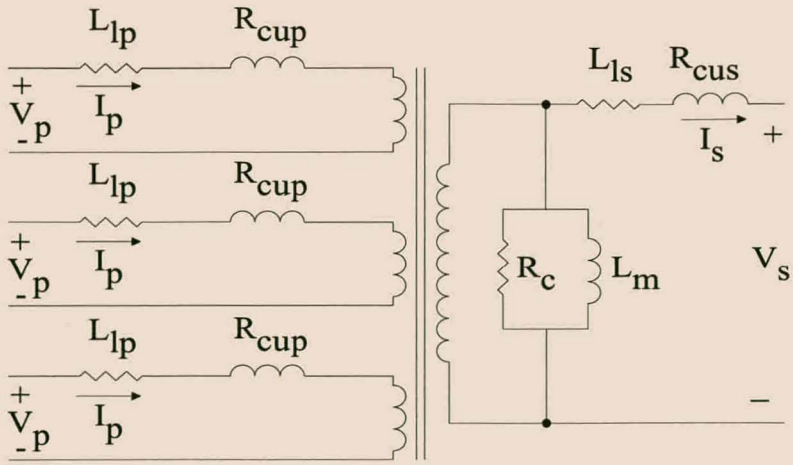


Figure 4.2: Equivalent circuit of the injection transformer.

Parameter	Symbol	Value
Voltage Rating per Primary	V_p	480 V (RMS)
Current Rating per Primary	I_p	49 A (RMS)
Voltage Rating of Secondary	V_s	230 V (RMS)
Current Rating of Secondary	I_s	304 A (RMS)
Leakage Inductance per Primary	L_{lp}	62 μH
Leakage Inductance of Secondary	L_{ls}	89 μH
Copper Resistance per Primary	R_{cup}	0.21 Ω
Copper Resistance of Secondary	R_{cus}	11.48 $m\Omega$
Magnetizing Inductance (viewed from secondary side)	L_m	144 mH
Core Loss Resistance (viewed from secondary side)	R_c	289 Ω

Table 4.3: Parameters of the scale model injection transformer.

windings. On the other hand, if interleaved switching is applied, the rapid changes in voltage occur between the different primary windings as well as with respect to ground.

As mentioned in section 4.2, the magnetic components of the experimental phase-arm were designed at a reduced power rating to save cost. The injection transformer of the scale model has the same voltage ratings as those of the full-scale injection transformer presented in Table 4.2, but with one tenth of the current ratings. It was, however, found that this transformer could handle one and a half times its rated current for short periods of time.

After the transformer had been constructed, standard short-circuit and open-circuit tests (see, for instance, [14], p. 54) were performed to determine its parameters. These are presented in Table 4.3, while Figure 4.2 shows the equivalent circuit of the injection transformer.

For a full-scale injection transformer the leakage inductances, magnetizing inductance and

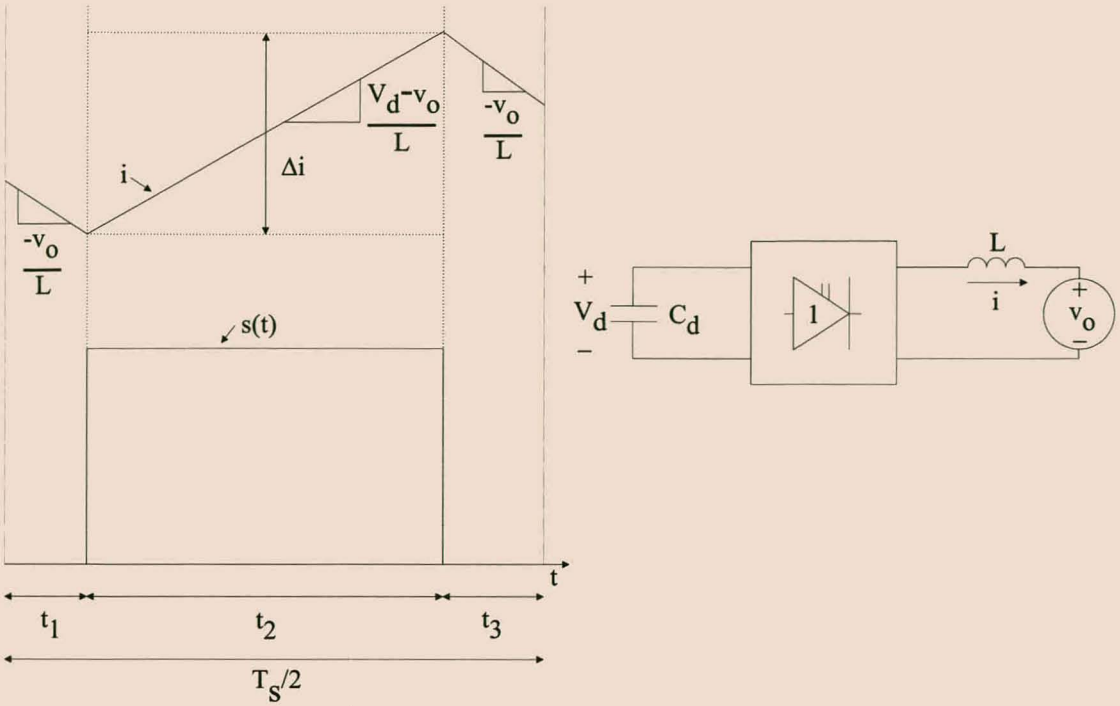


Figure 4.3: Inductor current over half a switching cycle.

copper resistance are expected to be significantly smaller than for the scale-model.

4.3.2 Output filter

In this section the design of the low-pass output filter of each full-bridge converter is discussed. Recall that the three-level series-stacked converter must be designed to operate under both ordinary and interleaved switching.

4.3.2.1 Filter inductors

As a first step the design of the filter inductors is discussed. To simplify the design it is assumed that the filter capacitor voltage v_o stays constant over half a switching cycle.

Figure 4.3 shows the inductor current over half a switching cycle. Although only the case where the switching function $s(t)$ is positive is considered in Figure 4.3, the details of the analysis are identical for negative values of $s(t)$. At relatively high switching frequencies, the ripple current Δi can be approximated by

$$\Delta i = \frac{(V_d - v_o)t_2}{L} = \frac{(V_d - v_o)\overline{f_r}T_s}{2L}, \tag{4.1}$$

where $\overline{f_r}$ is the average value of the reference function f_r over the half switching period and V_d is the DC-bus voltage of the full-bridge converter building block.

Assuming that the output voltage v_o closely approximates the reference function, it follows that

$$v_o \approx V_d \overline{f_r}, \tag{4.2}$$

which implies that

$$\Delta i \approx \frac{V_d(1-\overline{f_r})\overline{f_r}T_s}{2L}. \tag{4.3}$$

Furthermore, Δi reaches its maximum value when $\overline{f_r} = \frac{1}{2}$. This implies that

$$\Delta i_{max} \approx \frac{V_d T_s}{8L}. \tag{4.4}$$

Choosing Δi_{max} equal to 200 A (approximately 30% of the peak output current) yields a value of $L = 200$ μH.

Another important consideration is the maximum possible rate of increase in the inductor current. In [89] and [45] an optimal on-line tuning predictive current regulator was presented. When using an inner-loop current regulator of this type, it is important to ensure that

$$\left|\frac{di}{dt}\right| \geq \left|\frac{di_r}{dt}\right|, \tag{4.5}$$

where i_r is the current reference applied to the current regulator. As mentioned in the specifications, the converter is designed to be able to inject voltage harmonics up to 650 Hz. The criterion that will be used in this thesis is as follows: it is required that the inductor current must be able to follow current references of magnitude up to half the rated current when the output voltage v_o is at two thirds of its rated value. Hence the inductor current must be able to follow a reference of the form

$$i_r(t) = \frac{486\sqrt{2}}{2}\cos(2\pi \cdot 650t) \text{ A} \tag{4.6}$$

when the voltage over the filter inductor is equal to $800 - \frac{2}{3} \cdot 480 \cdot \sqrt{2} = 348$ V. This implies that

$$\frac{di_r}{dt} \leq \frac{486\sqrt{2} \cdot 2\pi \cdot 650}{2} = 1.404 \text{ A}/\mu\text{s}, \tag{4.7}$$

from which it follows that $L \leq 248$ μH. This condition is satisfied with the choice of $L = 200$ μH.

In the experimental 700 kVA series-stacked phase-arm an air-core inductor was used. This inductor was wound with 'welding cable' from Alvern cables [110]. This cable has a cross-sectional area of 50 mm^2. A single-layer cylindrical-shaped inductor was designed using the method of [4], p. 162. This method results in the shortest possible length of conductor to obtain a specified inductance. Based on these calculations, the diameter of the inductor is 617 mm and its height is 251 mm. It has 17 turns and the total length of the conductor is 32.48 m. The DC resistance of the inductor is 11.2 mΩ. The conductor is made up of strands with a diameter of 0.28 mm. This is substantially less that the skin depth (equal to 0.9 mm) in copper at 5 kHz.

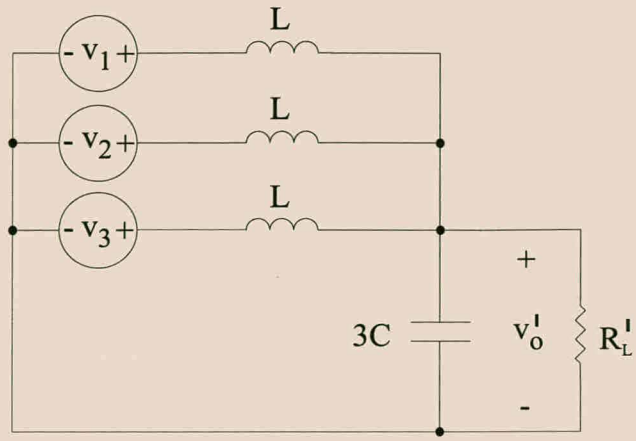


Figure 4.4: Simplified equivalent circuit of the output filter.

4.3.2.2 Filter capacitors

The next step in the design of the output filter is to determine the size of the filter capacitors. In the initial design of the filter capacitors the injection transformer is assumed to be ideal. It is further assumed that the load R_L is purely resistive and equal to 330 mΩ when referred to the primary side of the injection transformer. The load resistance referred to the primary side of the transformer is denoted by R'_L.

Consider the equivalent circuit of the output filter shown in Figure 4.4. The transfer function of the output filter is given by

$$V'_o(s) = \frac{R'_L}{3R'_L + Ls + 3R'_L CLs^2} \left(V_1(s) + V_2(s) + V_3(s)\right). \tag{4.8}$$

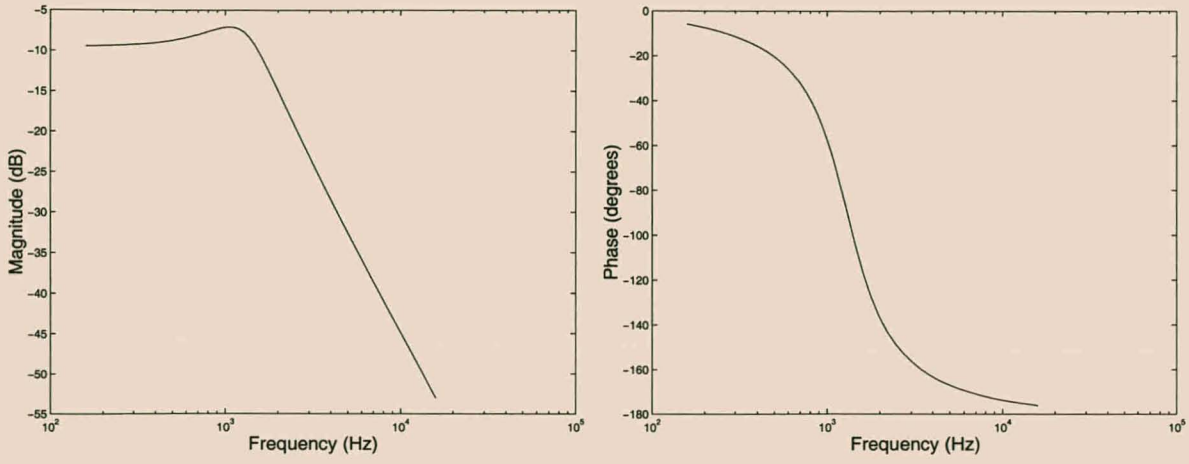
Choosing $C = 150$ μF results in an undamped natural frequency ω_0 given by

$$\omega_0 = \frac{1}{\sqrt{LC}} = 919 \text{ Hz}, \tag{4.9}$$

and a damping coefficient ζ of

$$\zeta = \frac{1}{6R'_L}\sqrt{\frac{L}{C}} = 0.583. \tag{4.10}$$

Figure 4.5 is a bode plot of the transfer function of the output filter. The transfer function shows a peak in magnitude at 1055 Hz. This peak increases in magnitude as the load resistance increases. The phase of the output filter transfer function is equal to $-29°$ at 650 Hz. A well-designed closed-loop controller will, however, compensate for both the phase lag and the resonance peak. Furthermore, since the experimental version of the phase-arm was constructed to operate under both ordinary and interleaved switching, the cut-off frequency of the output filter had to be chosen to be relatively low. In a final version of the phase-arm it may be decided to operate only under interleaved switching. In this case the cut-off frequency of the output filter can be increased significantly, leading to smaller filter components and improved bandwidth.



(a) (b)

Figure 4.5: Frequency response of the output filter using an ideal injection transformer.

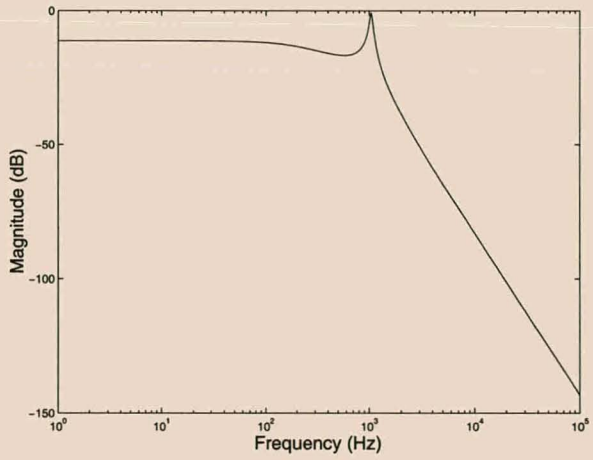


Figure 4.6: Frequency response of the output filter including the equivalent circuit of the injection transformer.

Figure 4.6 shows the frequency response of the output filter taking the equivalent circuit of the injection transformer into account. This figure was produced by using the evaluation version of PSpice version 8 from MicroSim. The injection transformer gives rise to an increase in the magnitude of the peak near 1 kHz as well as a more rapid decline of the magnitude of the frequency response above 1 kHz.

Some attention should be given to the current rating of the filter capacitors. In the worst case all the filter inductor ripple current flows through the filter capacitor. The exact RMS value of the filter capacitor current is dependent on the particular application and operating conditions. Once these conditions are known, it can only be accurately determined through simulation.

A very rough estimate of the worst-case RMS ripple current can be made based on the current waveform of Figure 4.3. Observing that the worst case ripple current component can be ap-

Parameter	Value
Nominal DC-bus Voltage	800 V
Peak DC-bus Voltage	900 V
Maximum Duty Cycle	85%
Maximum Sinusoidal Output Current	486 A (RMS)
Peak Output Current	687 A
Switching Frequency	2.5 kHz

Table 4.4: Design parameters of the full-bridge converter building blocks.

proximated by a triangular waveform, the RMS value of the ripple current calculated over the switching cycle of Figure 4.3 can be approximated by

$$I_{C(ripple)} \approx \frac{\Delta i_{max}}{2\sqrt{3}} = 58 \text{ A}. \tag{4.11}$$

The next step is to calculate the RMS value of the low frequency component of the filter capacitor current. For the rated sinusoidal output voltage, this is given by

$$I_{Cf} = 2\pi \cdot 50 \cdot 150 \cdot 10^{-6} \cdot 480 = 23 \text{ A}. \tag{4.12}$$

Hence, the worst-case RMS filter capacitor current can be approximated by

$$I_C \approx I_{C(ripple)} + I_{Cf} = 81 \text{ A}. \tag{4.13}$$

The 440 V (RMS), 50 μF C.V.T. range capacitor from Afcap [109] was selected as filter capacitor. A stack of twelve of these capacitors forms each of the three filter capacitor banks. Two capacitors are connected in series to obtain the required voltage rating. Each filter capacitor stack consists of six of these series strings connected in parallel to obtain the required 150 μF. Each 50 μF capacitor has a continuous current rating of 16 A (RMS) and a peak current rating of 1000 A. This implies that each filter capacitor stack has a continuous current rating of 96 A (RMS). This is larger than the worst-case value of 81 A calculated above.

According to the data sheet, the ESR of each 50 μF capacitor is equal to 10 mΩ. This implies that the ESR of each stack is equal to 3.3 mΩ.

4.3.3 Full-bridge converter building blocks

This section describes the design of the full-bridge converter building blocks of the experimental 700 kVA phase-arm. Table 4.4 summarizes the design parameters of the full-bridge converters.

One of the first choices made in the design of the full-bridge converter building blocks was to identify suitable switching devices. Given the high power rating, the choice lay between

IGBTs and GTOs. New switching devices like high-voltage IGBTs (3.3 kV and 4.5 kV) and IGCTs were not commercially available at the time that the converter design was carried out. Although GTOs are suited to very high power levels, their relatively low switching frequencies, snubbing requirements and complicated gate drives made them a less attractive option than IGBTs.

After considering IGBT devices from Powerex, Toshiba and Semikron, it was found that the SKiiP (Semikron integrated intelligent power pack) provided the most economical solution at that time. These integrated power modules (see [104]) contain an integrated gate drive with an isolated power supply, current measurement and over-current and over-temperature protection. The driver circuits can be ordered with an optional optical interface. The integrated modules are fitted on the heatsink by the manufacturer to ensure low thermal resistance.

Based on the specifications of Table 4.4 the SKiiP 1212 GB 120 (see [104], p. 796) half-bridge with the 402 driver was recommended by the manufacturer. This driver receives its gating signals through an optic fiber interface. It also provides an optical error signal that is activated under over-current or over-temperature conditions.

Each half-bridge module consists of four phase-arms connected in parallel to obtain the required current rating. Table 4.5 gives the essential data of the SKiiP 1212 GB 120 module. Each full-bridge converter is formed by connecting two of these modules to a common DC-bus capacitor bank.

One of the most important considerations when designing the converter building blocks is to ensure that the maximum junction temperature of the semiconductor devices is not exceeded.

The first step is to calculate the total converter losses per switching cycle. In the following analysis the effect of the ripple current on the converter losses will not be taken into account and it is assumed that the filter inductor current remains constant over one switching period. One of the main effects of the ripple current on the converter losses is the fact that the magnitude of IGBT collector current at turn-on differs from that at turn-off. Because the manufacturer did not provide separate data on the turn-on and turn-off loss, this cannot be taken into account in the loss calculations.

In the following discussion the half-bridge output current is denoted by I_o (with the same sign convention as in Chapter 2). Based on the comments above it is assumed that I_o is constant over one switching cycle. Under these conditions one of the IGBTs and one of the diodes, of each half-bridge, turn on and off exactly once per switching cycle.

The IGBT switching losses per switching cycle is given by (see [104], p. A-56)

$$W_{isc} = (E_{on} + E_{off})\frac{V_d}{600}\frac{|I_o|}{1200}, \tag{4.14}$$

where V_d is the DC-bus voltage of the full-bridge converter and $E_{on} + E_{off}$ is the sum of the

Module Characteristics		
Parameter	Symbol	Value
Maximum DC-link Voltage	V_{CC}	900 V
Isolation Voltage (to Heatsink)	V_{isol}	3000 V (RMS)
Driver Supply Voltage (Unregulated)	V_{S2}	24 V
Maximum Switching Frequency	f_{swmax}	7 kHz
Over-Temperature Protection Threshold	T_{tp}	115°C
Thermal Resistance Heatsink to Ambient (With fan)	R_{thha}	0.02 K/W
Blanking Time	t_b	5 μs
IGBT Section		
Maximum Collector Emitter Voltage	V_{CES}	1 200 V
Maximum Collector Current (Continuous)	I_C	1 200 A
Peak Collector Current	I_{CM}	2 400 A
Collector Emitter Saturation Voltage at 25°C	V_{CEsat}	2.75 V
Collector Emitter Saturation Voltage at 125°C	V_{CEsat}	3.6 V
Turn-on + Turn-off Energy (at 125°C)	$E_{on} + E_{off}$	360 mJ
Thermal Resistance Junction to Heatsink (Per IGBT)	R_{thjh}	0.02 K/W
Maximum Junction Temperature	T_{jmax}	125°C
Diode Section		
Maximum Forward Current (Continuous)	I_F	990 A
Peak Forward Current	I_M	2400 A
On-state Voltage at 25°C	V_F	2.0 V
On-state Voltage at 125°C	V_F	1.8 V
Turn-on + Turn-off Energy (at 125°C)	$E_{on} + E_{off}$	48 mJ
Thermal Resistance Junction to Heatsink (Per diode)	R_{thjh}	0.07 K/W
Maximum Junction Temperature	T_{jmax}	125°C

Table 4.5: Parameters of the SKiiP 1212 GB 120 half-bridge integrated IGBT module.

turn-on and turn-off energies of the IGBT (see Table 4.5). Similarly, the diode switching losses per cycle is given by

$$W_{dsc} = (E_{on} + E_{off})\frac{V_d}{600}\frac{|I_o|}{1200}. \tag{4.15}$$

[Some confusion may arise concerning the use of $E_{on} + E_{off}$. In equation 4.14 $E_{on} + E_{off}$ denotes the sum of the turn-on and turn-off energy of the IGBT, while $E_{on} + E_{off}$ is the sum of the turn-on and turn-off energy of the diode in 4.15. This choice of symbols is based on those used in the data sheet. The meaning should, however, be clear from the context.]

Assuming that the output current has half-wave symmetry, the average IGBT switching losses are shared evenly by the two IGBTs of the half-bridge. Similarly the diode switching losses are shared evenly between the two diodes of the half-bridge.

The IGBT conduction loss per switching cycle is given by

$$W_{icc} = \begin{cases} V_{CEsat} I_o d T_s & \text{if } I_o \geq 0 \\ V_{CEsat} I_o (d-1) T_s & \text{if } I_o < 0, \end{cases} \tag{4.16}$$

where $0 \leq d \leq 1$ is the duty cycle of the phase-arm and $T_s = \frac{1}{f_s}$ is the switching period of the half-bridge. Similarly, the diode conduction loss per cycle is given by

$$W_{dcc} = \begin{cases} V_F I_o (1-d) T_s & \text{if } I_o \geq 0 \\ -V_F I_o d T_s & \text{if } I_o < 0. \end{cases} \tag{4.17}$$

The average IGBT and diode conduction losses are also shared evenly by the two IGBTs and diodes of the phase-arm.

Two distinct cases are considered in the thermal analysis of the full-bridge converter building blocks. In the first case the operation of the series-injection device as a dip compensator is considered. In this case the output voltage is assumed to be sinusoidal. Figure 4.7 shows the worst case (maximum on state voltages were used) steady-state losses at rated sinusoidal (480 V (RMS)) output voltage and a DC-bus voltage of 800 V. The output current used in this analysis is also sinusoidal and ranges from 0 A to rated output current of 486 A (RMS). In Figure 4.7 (a) to (c) the output voltage is in phase with the output current.

The losses increase linearly with output current. At rated output current the IGBT junction temperature rises to 98°C, which is within the thermal limits of the device.

Figure 4.7(d) shows the heatsink and junction temperatures as functions of the phase angle between output voltage and the output current at rated voltage and rated current. The different junction temperatures stay almost constant as the phase angle ranges from $-40°$ to $40°$. It is also interesting to note that the maximum total converter losses occur at a phase angle of $0°$.

In the second case the operation of the series device at zero output voltage is considered. This closely approximates the operation of the converter when it injects only a small voltage

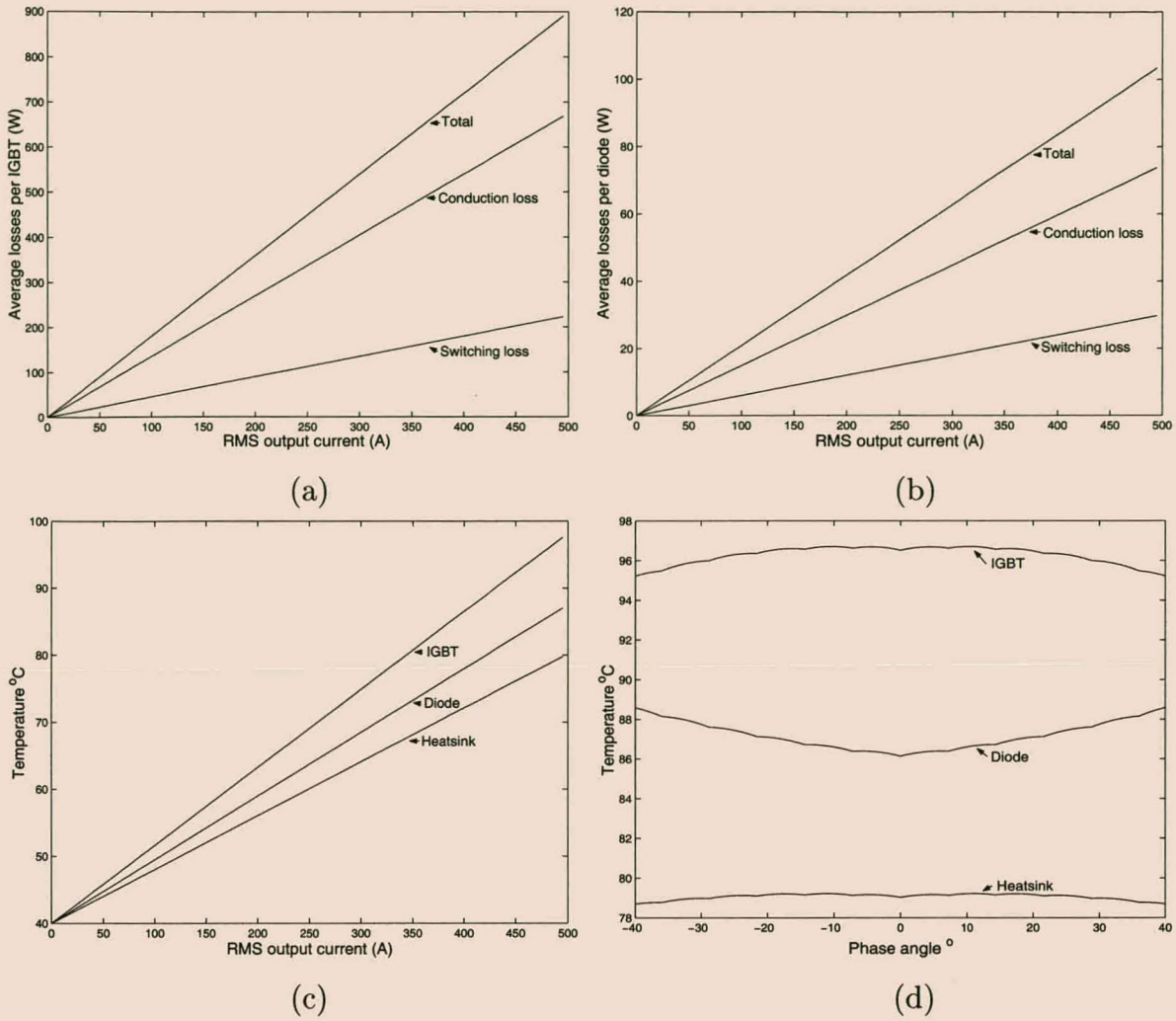


Figure 4.7: Worst-case steady-state half-bridge losses at rated output voltage: (a) IGBT losses, (b) diode losses, (c) junction and heatsink temperatures, (d) temperatures as functions of phase angle.

component. In this mode of operation the diodes and IGBTs of each phase-arm conduct for equal periods of time during each switching cycle. It is again assumed that the output current is sinusoidal and the losses are evaluated for the output current ranging from 0 A to rated current.

Figure 4.8(a) shows the average losses per IGBT, while Figure 4.8(b) shows the losses per diode. The total losses per half-bridge are shown in Figure 4.8(c). Although the IGBT losses decreased the diode losses increased compared with the previous case.

Figure 4.8(d) shows the steady-state junction and heatsink temperatures as a function of the RMS output current. In this case the diode junction temperature is the highest with a value of 93°C at rated output current. This is within the thermal limits. The total converter loss is smaller than in the previous case as reflected in the lower steady-state heatsink temperature.

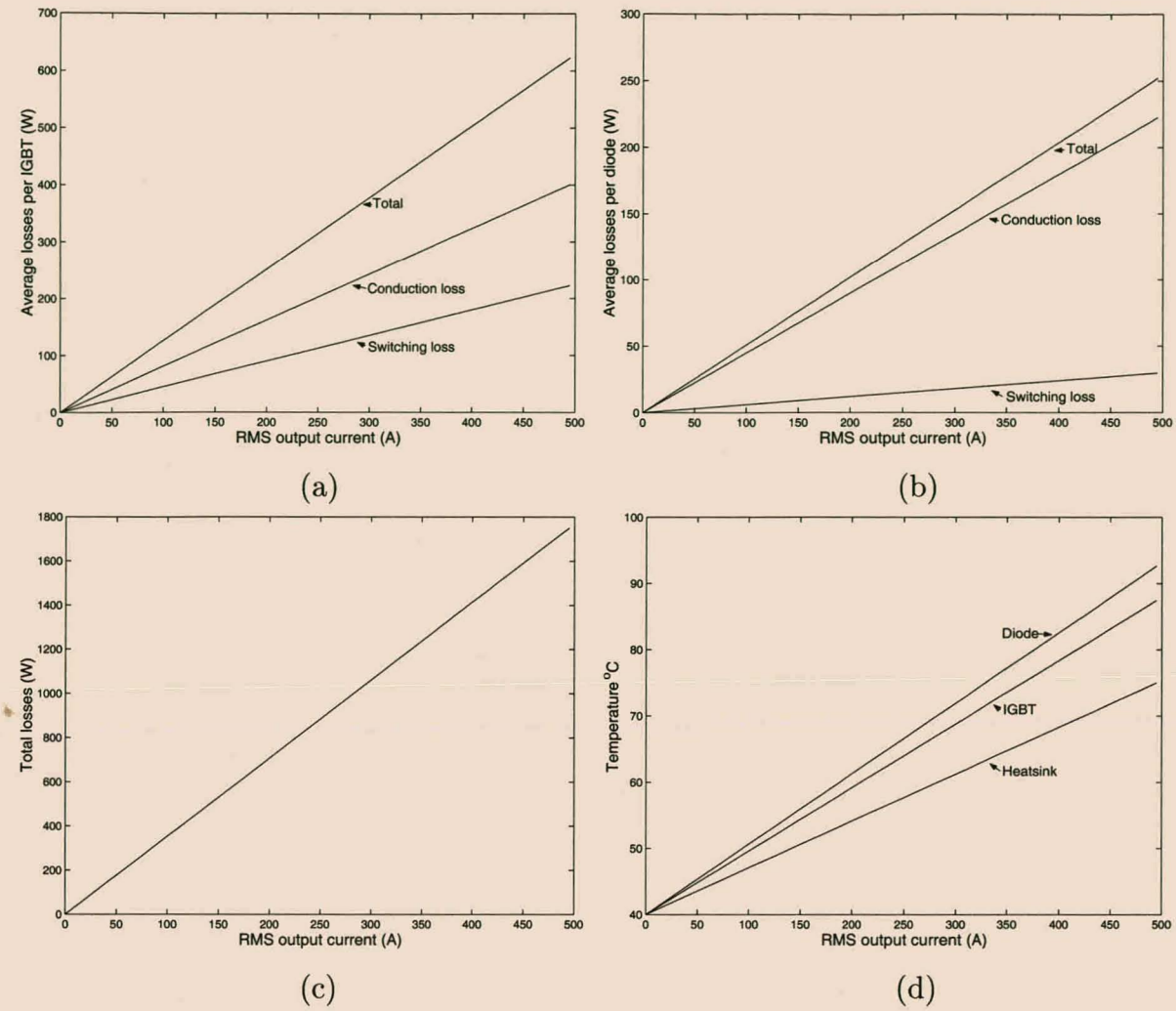


Figure 4.8: Worst-case steady-state half-bridge losses at zero output voltage. (a) IGBT losses, (b) diode losses, (c) total loss, (d) junction and heatsink temperatures as functions of output current.

The next step in the design of the full-bridge converter building blocks is the selection of the DC-bus capacitor bank of each full-bridge converter. As mentioned in the introduction the energy storage device supplies a well-regulated DC-bus. Hence, the main criterion for the design of the filter capacitors is given by equation 3.36 which states that

$$C_d \geq \frac{1}{L\omega_r^2\pi^2} = 5.1 \text{ mF}, \tag{4.18}$$

where $\omega_r = 2\pi \cdot 50$. In order to ensure that the DC-bus voltages of the three-level series-stacked converter do not oscillate following a perturbation, it was decided to choose C_d equal to 26.4 mF. This is approximately five times larger than the minimum value suggested by equation 4.18.

Attention should also be given to the RMS current rating of the DC-bus capacitors. The DC-bus capacitor ripple current is dependent on the output impedance of the DC source. As mentioned earlier, the superconducting magnetic energy storage device provides a well-regulated DC-bus.

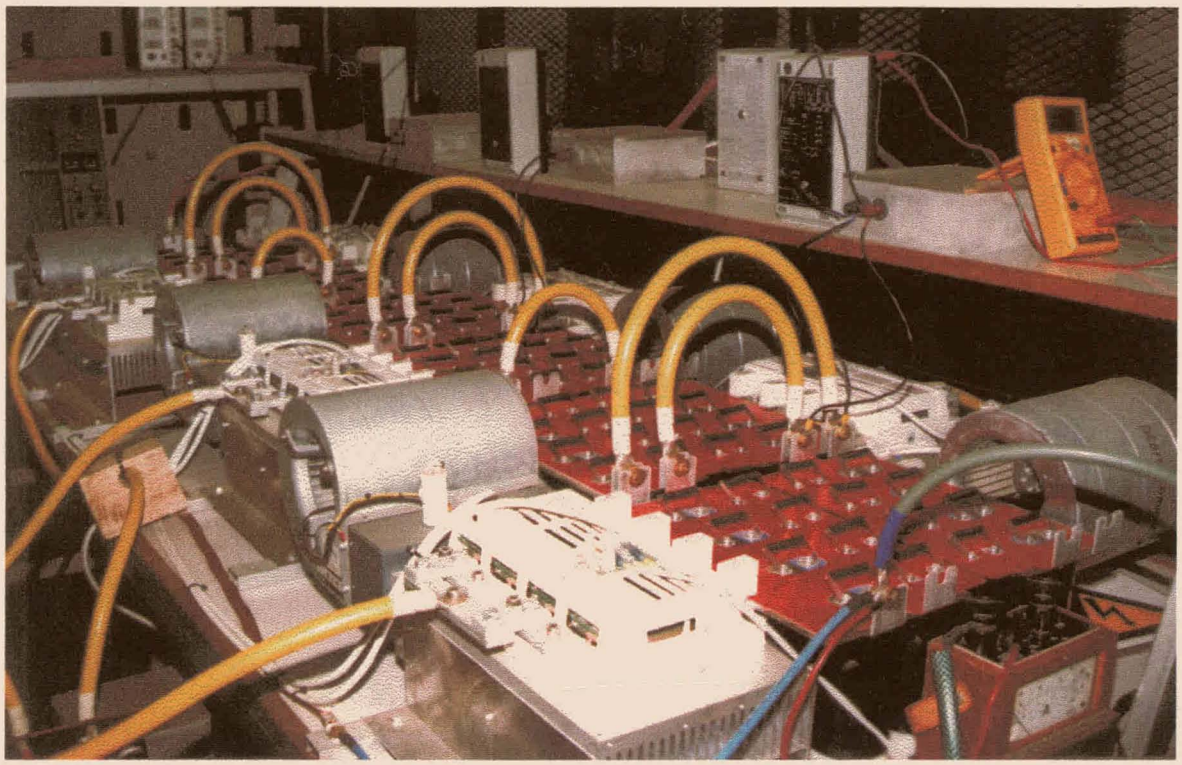


Figure 4.9: Photograph of the three-level series-stacked converter.

Based on this information the DC voltage source is considered as a perfect voltage source. It is further assumed that the impedance between the DC-source and the DC-bus of the three-level series-stacked phase-arm is small and can be neglected.

Refer to Figure 4.10 for the definitions of the currents that will be used in the following analysis. It follows from Figure 4.10 that:

$$i_{c_1} = i_b - i_{b_1} \tag{4.19}$$

$$i_{c_2} = i_b - i_{b_2} \tag{4.20}$$

$$i_{c_3} = i_b - i_{b_3}. \tag{4.21}$$

Furthermore, since the total DC-bus voltage V_b is constant, it follows that

$$i_{c_1} + i_{c_2} + i_{c_3} = 0. \tag{4.22}$$

Solving i_{c_1}, i_{c_2} and i_{c_3} results in

$$i_{c_1} = \frac{1}{3}\left(-2i_{b_1} + i_{b_2} + i_{b_3}\right) \tag{4.23}$$

$$i_{c_2} = \frac{1}{3}\left(i_{b_1} - 2i_{b_2} + i_{b_3}\right) \tag{4.24}$$

$$i_{c_3} = \frac{1}{3}\left(i_{b_1} + i_{b_2} - 2i_{b_3}\right). \tag{4.25}$$

In the steady-state the 'low-frequency' components of i_{b_1}, i_{b_2} and i_{b_3}, associated with the reference function, are identical. Hence, only the ripple components of these currents have to be taken into account.

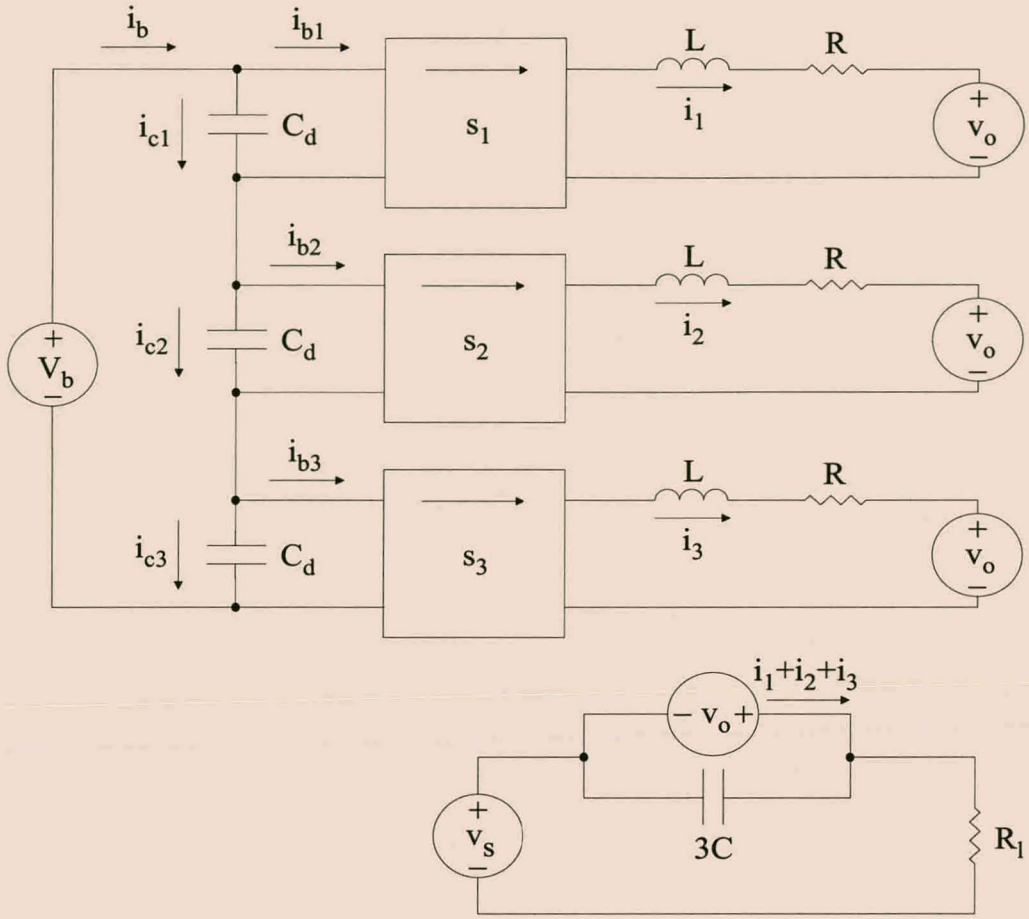


Figure 4.10: Equivalent circuit of the three-level series-stacked converter with zero bus impedance.

The next step is to obtain an estimate for the RMS values of the ripple components of i_{b_1}, i_{b_2} and i_{b_3}. Based on the analysis of Chapter 3, we know that

$$i_{b_1} = i_1 s_1 \tag{4.26}$$

$$i_{b_2} = i_2 s_2 \tag{4.27}$$

$$i_{b_3} = i_3 s_3. \tag{4.28}$$

Hence, based on Figure 4.3 the following approximate relations hold for the worst-case RMS ripple currents

$$I_{b_1(ripple)} \leq \frac{\Delta_{imax}}{2\sqrt{3}} \tag{4.29}$$

$$I_{b_2(ripple)} \leq \frac{\Delta_{imax}}{2\sqrt{3}} \tag{4.30}$$

$$I_{b_3(ripple)} \leq \frac{\Delta_{imax}}{2\sqrt{3}}. \tag{4.31}$$

From equations 4.23 to 4.25, it follows that the worst-case values of the RMS ripple components of i_{c_1}, i_{c_2} and i_{c_3} are given by

$$I_{c_1(ripple)} \leq \frac{1}{3}\left(2I_{b_1(ripple)} + I_{b_2(ripple)} + I_{b_3(ripple)}\right) \leq 77 \text{ A} \tag{4.32}$$

$$I_{c2(ripple)} \leq \frac{1}{3}\left(I_{b1(ripple)} + 2I_{b2(ripple)} + I_{b3(ripple)}\right) \leq 77 \text{ A} \quad (4.33)$$

$$I_{c3(ripple)} \leq \frac{1}{3}\left(I_{b1(ripple)} + I_{b2(ripple)} + 2I_{b3(ripple)}\right) \leq 77 \text{ A}. \quad (4.34)$$

Another case that requires some consideration is where the impedance between the DC-source and the converter bus is relatively large. In this case i_b contains a relatively small ripple component. This implies that each individual DC-bus has to supply the full ripple current drawn by its converter. In this case the RMS high-frequency ripple current is also less than or equal to 58 A.

The 3 300 μF 83 series 450 V capacitors from Felsic were selected based on their long lifetime and ability to handle relatively high ripple currents. The DC-bus capacitor bank of each full-bridge converter consists of 32 of these capacitors. Two capacitor banks of 16 capacitors each were connected in series to obtain the required voltage rating. Each capacitor has an RMS ripple current rating of 12.6 A, which means that the DC-bus of each full-bridge converter can handle 202 A (RMS) of ripple current. This is well above the value calculated above.

According to the data sheet each capacitor has an ESR of 40 mΩ. Hence the DC-bus capacitor bank of each full-bridge converter has an ESR of 5 mΩ. A 22 kΩ bleeding resistor was fitted to each of the capacitors. The time constant associated with the DC-bus capacitor bank and its bleeding resistors is equal to 72.6 s.

4.3.4 Measurement system

In the experimental version of the 700 kVA series-stacked converter seven voltage measurements and three current measurements are required. The three DC-bus voltages, three filter capacitor voltages and secondary side transformer voltage are measured. The three filter inductor currents are also measured. In a final industrialized version of the phase-arm the number of measurements may be reduced. The bus voltage measurements may, for instance, be replaced by over-voltage sensors that are only used for protection purposes.

Based on the high DC-bus voltage and to avoid problems associated with EMI it was decided to develop an optically isolated voltage measurement system. The voltage measurement system consists of seven isolated transmitters as well as an optical receiver board. The optical receiver board interfaces with the DSP/FPGA-based controller. The Hewlett Packard HFBR1521/2521 series of optical transmitters and receivers were used to form the optical data link.

Figure 4.11 is a block diagram of the isolated voltage measurement transmitter, while Figure 4.12 is a photograph of one of the units. Each voltage measurement transmitter consists of three separate printed circuit boards that are mounted in separate compartments of a cast aluminum box. The first of these boards is an isolated power supply that provides 5 V and $\pm$15 V to

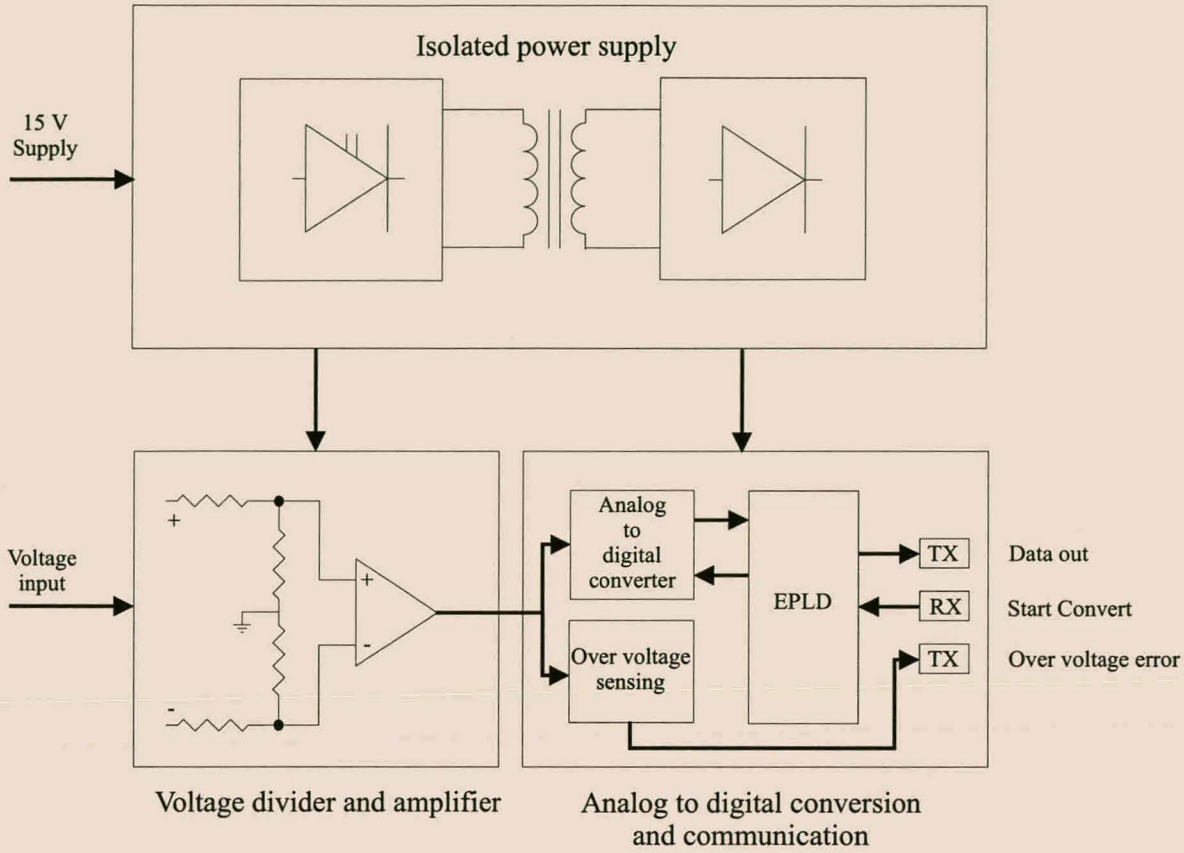


Figure 4.11: Block diagram of the isolated voltage measurement system transmitter [106].

power the analog and digital circuitry of the voltage measurement transmitter. The power supply consists of a small power electronic converter, switching at 150 kHz, a small isolation transformer with three secondaries, three separate rectifiers and three voltage regulators. The isolation transformer was wound on a toroid covered with 'glass tape'. A similar transformer was tested in the high-voltage laboratory at the University of Stellenbosch. Its isolation broke through at 20 kV.

The second board is a differential voltage divider and instrumentation amplifier. Special 10 MΩ resistors with good linearity over the required voltage range were selected for this purpose. Offset adjustment as well as compensation for the parasitic capacitances of the 10 MΩ resistors was included. An AD620 instrumentation amplifier from analog devices [112] provides gain adjustment and amplifies the measured voltage to suitable levels for analog to digital conversion.

The third board of the voltage measurement transmitter is responsible for the conversion of the measured voltage to an optical data stream. It also makes provision for over-voltage sensing. The operation of this board is controlled by an EPM7064SLC-44-10 in circuit programmable EPLD (Erasable Programmable Logic Device) from ALTERA [111]. The main function of this device is to take care of the communication between the receiver board and the voltage measurement transmitter. It receives a start conversion pulse from the transmitter, initiates

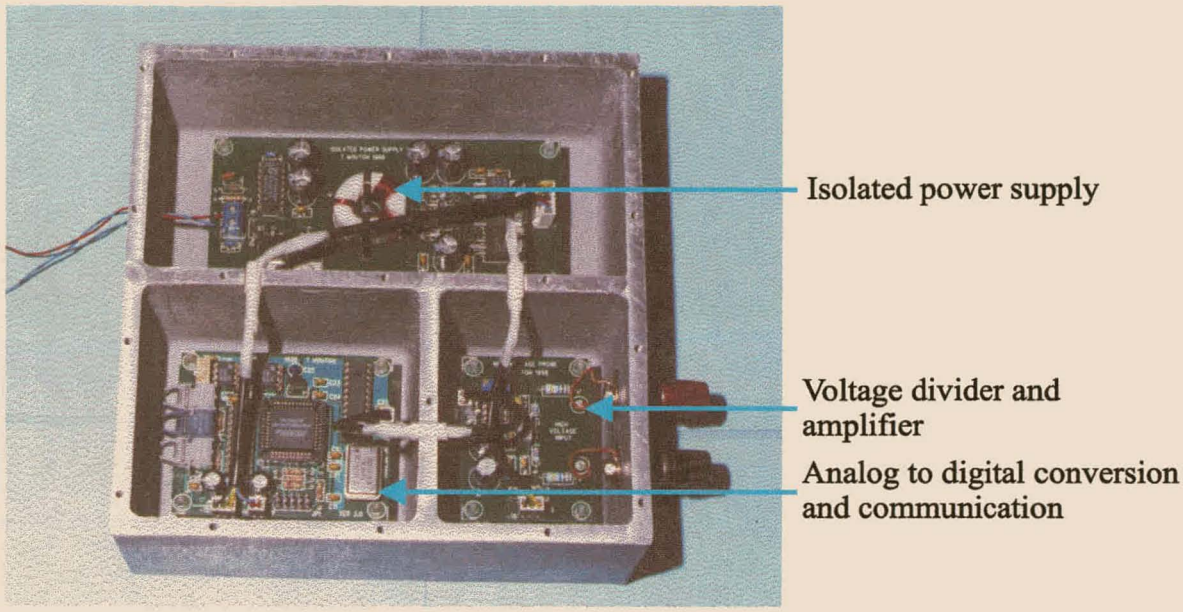


Figure 4.12: Photograph of the isolated voltage measurement system transmitter.

the analog to digital conversion process and transmits the digital value of the measured voltage as a serial bit stream. A twelve-bit AD7892AN-1 [112] analog to digital converter from Analog Devices was used to convert the output of the instrumentation amplifier to a digital data word. This analog to digital converter has a conversion time of 1.47 μs. The measured data is transmitted at 1 MBaud (Mega bits per second) over the optical interface. Hence the total effective conversion time (as seen by the DSP-based controller) is equal to 14 μs.

Over-voltage sensing is carried out by comparing a reference voltage to the measured voltage using a standard LM311 voltage comparator. The output of the comparator is used to trigger an optical fiber transmitter.

Figure 4.13 is a photograph of the isolated voltage measurement receiver board. The purpose of this board is to act as interface between the DSP/FPGA controller and the optically isolated voltage measurement transmitters. This board is designed for a full three-phase system and contains 30 optical transmitters and receivers as well as an EPM81500 FPGA from ALTERA. The main function of the FPGA is to convert the serial bit stream to a parallel data word that is read by the DSP/FPGA-based controller. It also provides a start conversion signal for the individual voltage measurement transmitters. The software for both the transmitter EPLD and the receiver FPGA was written in VHDL using Maxplus II version 8.3 from ALTERA.

The three filter inductor currents were measured by using an LT1005-S current sensor from LEM [113]. This sensor has an RMS current rating of 1200 A. The signals from these sensors are converted to a differential signal and transmitted to the controller by making use of unshielded twisted pair cable. The differential signals are connected to the DSP/FPGA-based controller.

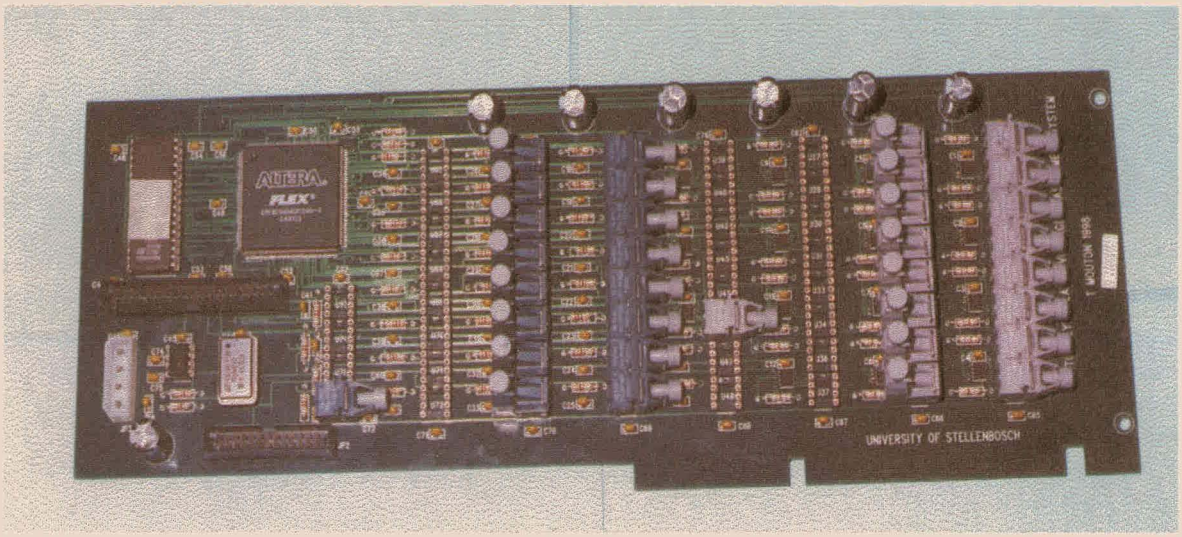


Figure 4.13: Photograph of the isolated voltage measurement receiver board.

4.3.5 DSP/FPGA-based controller

Figure 4.14 is a block diagram of the PEC31 DSP/FPGA controller (see [106] and [76]). Mr. D.D. Bester developed this controller as part of his M.Sc.(Eng) project under the guidance of the supervisor and the author of this thesis.

Table 4.6 summarizes the features and specifications of the PEC31 controller. Its main components are the TMS320C31 floating-point digital signal processor and an EPM81500 FPGA from ALTERA [111]. The DSP is typically used to implement high-level control algorithms, while the FPGA is used for low-level, high-speed processing. In the current application the FPGA is used as a digital pulse width modulator. The FPGA is also used to 'and' the different error signals from the IGBT modules and voltage measurement system. It automatically shuts the converter down when a fault condition is detected. Possible fault conditions include over-voltage on one of the DC-buses and over-current or over-temperature on one of the IGBT modules. The PEC31 board also contains high-speed analog to digital converters with differential receivers that are used to convert the output of the LEM current sensors to a digital format.

The main purpose of this controller is to generate the PWM gating signals for the different full-bridge converters of the three-level series-stacked phase-arm. C-programs were written that sets up the lookup tables containing the applicable reference functions. A number of different reference functions were used during the experimental evaluation of the phase-arm.

Apart from generating the switching functions, the FPGA also generates an interrupt near the end of each half switching cycle. This informs the DSP that it is ready to receive the next value of the reference function (duty cycle). An RS232 port was also implemented in the FPGA to enable communication with a personal computer.

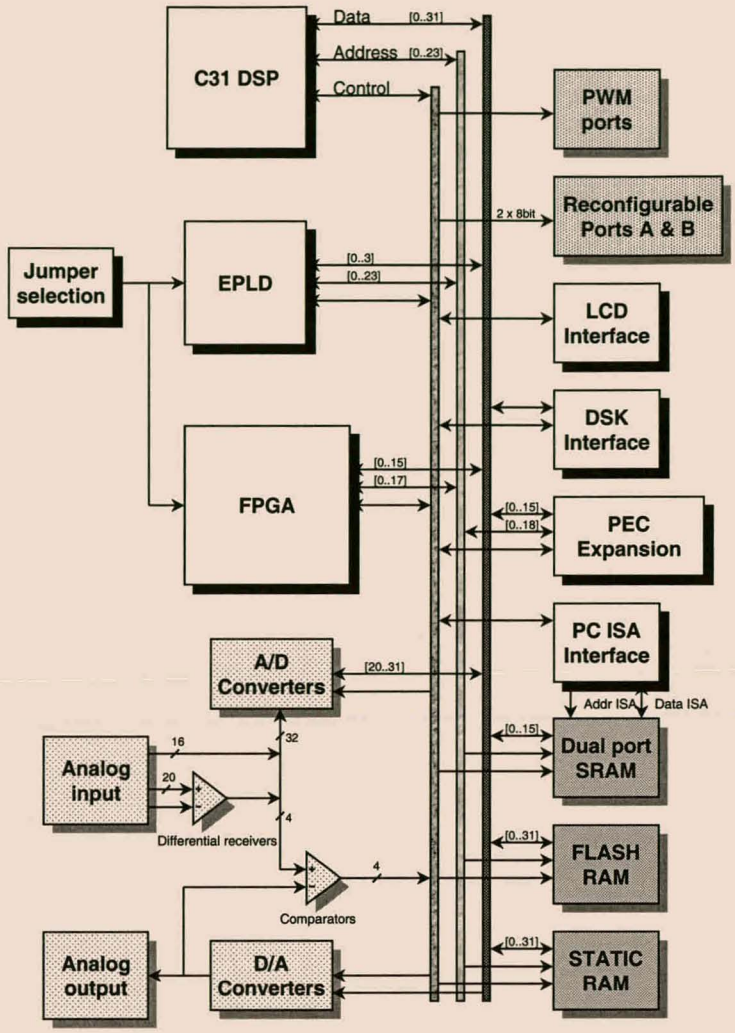


Figure 4.14: Block diagram of the PEC31 DSP/FPGA-based controller [106].

Figure 4.15 is a photograph of the optical driver and receiver board. The purpose of this board is to convert the electrical gating signals generated by the FPGA to optical signals. It also receives error signals from the different IGBT modules and voltage measurement systems. The different error signals are converted to a single error signal using four 20V8 GALs from Lattice. As for the other components of the controller and measurement system the optical driver and receiver board is also designed for a full three-phase system. It makes provision for 36 optical outputs and 27 optical inputs. It also contains a row of 27 surface-mount LEDs that shows the state of the different error signals received by the board.

4.4 Experimental results

This section describes the experimental results obtained with the 700 kVA phase-arm. The aim of the experimental work is twofold:

Digital specifications
TMS320C31 floating-point DSP from Texas Instruments (33 MHz)
60 ns single-cycle instruction execution time
33.3 MFLOPS (million floating-point operations per second)
16.7 MIPS (million instructions per second)
EPM81500 FPGA from ALTERA Corp
SRAM-based architecture
Low standby power and in-circuit reconfiguration
EPF7128s EPLD from ALTERA Corp
High speed and stability with non-volatile configuration
In circuit programmable for easy software modification
Texas Instruments C31 DSK (DSP Starter Kit) parallel port interface
ISA bus connection to enable PC supervision through 2k x 16 bit Dual Port RAM
512k x 32 FLASH memory
32k x 32 single wait state SRAM
Analog specifications
Four 8-channel 12-bit analog to digital converters (A/D) with 1.6 μs conversion time
Four channel 12-bit digital to analog converter (D/A) with a settling time of 6 s
Five 4-channel differential-input ports for high noise immunity
Four 4-channel, single-ended, analog input ports

Table 4.6: Specifications of the PEC31 DSP/FPGA controller.

1. The main aim is to verify the theory of Chapter 3 by showing that the three-level series-stacked converter is stable under a variety of different reference functions. Both the results of the transient and steady-state analysis of Chapter 3 are verified experimentally.

2. The second objective with the experimental work is to show that the converter functions properly at its rated DC-bus voltage.

4.4.1 The experimental setup

Figure 4.16 is a block diagram of the experimental setup that is used throughout the remainder of this chapter. The main components are the three-level series-stacked phase-arm along with its measurement and control system. The experimental setup also consists of a personal computer, isolation contactor, step-up transformer, thyristor controlled rectifier and an inductive load.

The PEC31 controller and its measurement system were described in sections 4.3.4 and 4.3.5. In the current application the main function of this controller is to generate the PWM gating

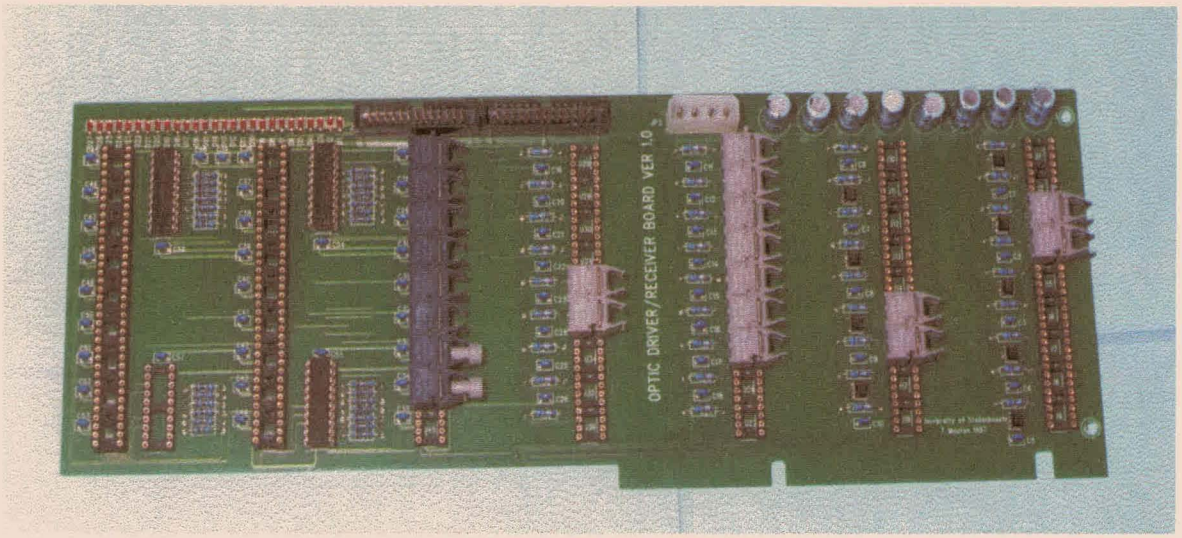


Figure 4.15: Photograph of the optical driver and receiver board.

signals for the three-level series-stacked phase-arm. The pulse width modulator is contained in the FPGA of the PEC31 controller. It consists of triangle generators and digital comparators. Two sets of VHDL code were developed, one for ordinary switching and one for interleaved switching. The reference functions are generated in the DSP by making use of lookup tables. Different C programs for ordinary and interleaved switching were developed. The main difference between the two programs is that the reference function is sampled at 5 kHz for ordinary switching and at 15 kHz for interleaved switching.

A standard 66 MHz 80486 personal computer is used as user interface to the system. This computer communicates with the PEC31 controller through an optical RS232 port. A small RSR232 to optical fiber interface board was developed for this purpose. The PEC31 receives commands from the PC through this port. In particular, it receives commands to close or open the contactor and to start or stop the modulation (switching) process. The PEC31 transmits the average and RMS values of the voltage and current measurements through the RS232 port to the PC, where it is displayed.

A 400 V (line to line), 1 MVA three-phase supply serves as energy source for the system and is isolated through a contactor. The contactor is controlled through an optic fiber connection with the PEC31 controller and opens automatically if a fault condition is detected. A step-up transformer is used to obtain the required voltage rating. This transformer has a continuous power rating of 20 kVA with a peak rating of 200 kVA. The primary has a voltage rating of 380 V line to line. A number of taps are available on the secondary. The tap with the highest voltage rating of 1670 V (line to line) is used. This leads to a maximum DC-bus voltage of 2.36 kV if no DC-current is drawn.

A high-voltage thyristor-controlled rectifier is used to rectify the output of the step-up trans-

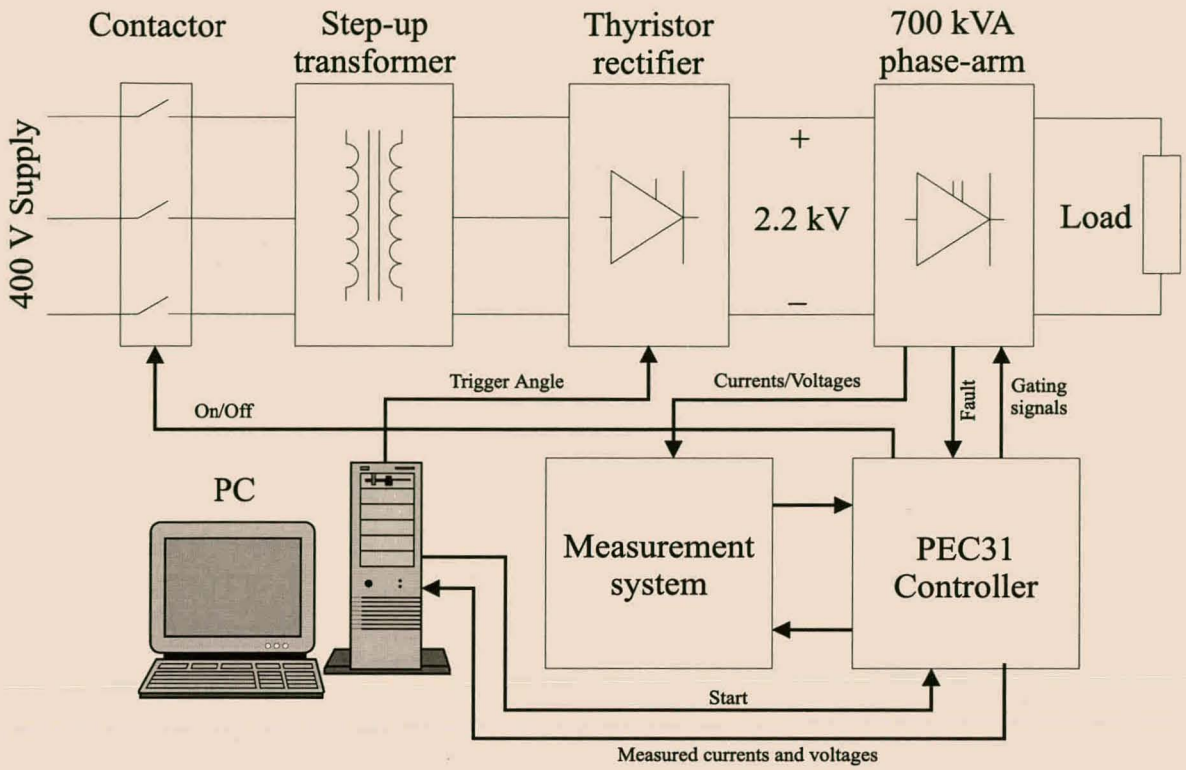


Figure 4.16: Block diagram of the experimental setup.

former. This rectifier was developed by the author as part of the research project. Eight 1 600 V, 75 A thyristors are stacked in series (per phase) to obtain the required voltage rating. Snubbers are used to ensure voltage sharing and to prevent over-voltages arising from the supply and transformer inductance. Each thyristor is mounted on a separate heatsink and is equipped with an over-voltage and over-temperature sensor. The thyristor-controlled rectifier automatically shuts down if one or more of these conditions occur. Its gating pulses are isolated through a low-cost optically isolated gate-drive circuit. This gate drive makes use of inexpensive infrared transmitters and receivers. An 8051-based digital controller is used to generate the gating signals for the individual thyristors. The controller is equipped with an optical RS232 interface that receives triggering angle information from the PC. By adjusting the triggering angle, a variable DC-bus voltage is obtained. The thyristor-controlled rectifier is also used to 'soft start' the DC-bus during converter startup.

The load consists of a 3 mH inductor in parallel with a 1.7 mH inductor. Hence the effective load inductance is equal to 1.1 mH, which has an impedance of 341 jmΩ at 50 Hz. Both inductors have an RMS current rating of 500 A.

All the measurements of this section were made using a Tektronix TDS3000 four-channel digital phosphor oscilloscope.

Parameter	Symbol	Value
Filter Inductance	L	262 μH
Filter Capacitance	C	150 μF
DC-bus Capacitance	C_d	28 mF
Parasitic Resistance	R	0.22 Ω
Load Resistance	R_L	10 kΩ
Bus Resistance	R_b	0.1 Ω

Table 4.7: Simulation parameters of the experimental 700 kVA phase-arm.

4.4.2 Balancing properties

In this section the balancing properties of the three-level series-stacked phase-arm are evaluated experimentally. In the first set of experiments the transient behavior is studied, while the steady-state behavior is studied in the second set of experiments.

All the measurements were carried out with a total DC-bus voltage of approximately 600 V. This voltage is substantially lower than the maximum DC-bus voltage of each individual full-bridge converter. Using a bus voltage of 600 V significantly reduces the risk of destruction of one of the converters, even under conditions of severe unbalance. Another advantage of this bus voltage is that the step-up transformer, with its large leakage inductance, was not required and the thyristor rectifier was connected directly to the 400 V supply.

4.4.2.1 Transient behavior

In this section the transient behavior of the three-level series-stacked converter is evaluated experimentally and compared with the theoretical predictions.

In order to obtain the simulation results, based on the theory of Chapter 3, the system parameters have to be known. Table 4.7 shows the parameters used in the simulations. The following is a discussion of how the component values of Table 4.7 were obtained and how the differences between the theoretical model and the practical system are likely to affect the results.

1. The primary side transformer leakage inductance L_{lp} (of 62 μH) was not taken into account in the theoretical analysis of Chapter 3. Although this can be included separately in the theoretical model, it increases the order and complexity of the model without providing a significant amount of extra insight into the balancing mechanisms.

   Figure 4.17 shows an ordinary switching d circuit, including the effect of the transformer primary side leakage inductance as well as the other relevant parasitic components. This circuit was derived by adapting the theoretical techniques of section 3.3. Resistor R_{lf} is

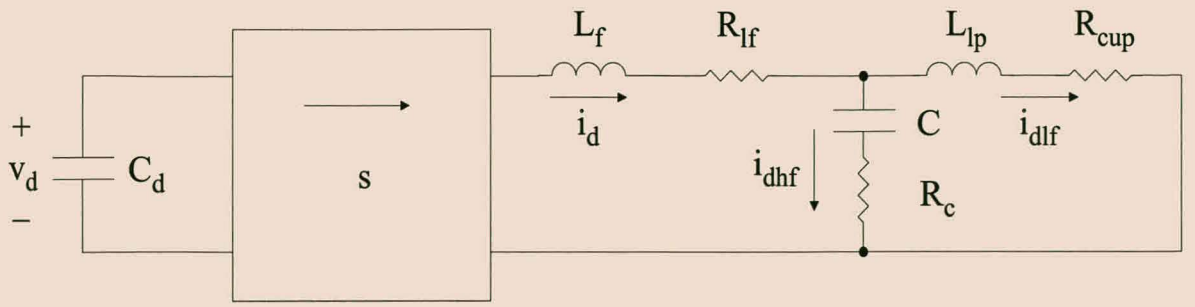


Figure 4.17: Modified d circuit including the transformer leakage inductance.

the filter inductor ESR which is equal to 11.2 mΩ (see p. 170). The ESR of the filter capacitor is denoted by R_c and is equal to 3.3 mΩ (see p. 173). As mentioned previously, R_{cup} is the primary side copper resistance of the injection transformer and is equal to 0.21 Ω (see Table 4.3).

Some attention should be given to the magnitudes of the different impedances playing a role in the d circuit. At a frequency of 50 Hz

$$\left|R_c + \frac{1}{2\pi \cdot 50 \cdot Cj}\right| = 21\ \Omega \quad \text{and} \quad |R_{cup} + 2\pi \cdot 50 \cdot L_{lp}j| = 0.22\ \Omega, \tag{4.35}$$

while at 5 kHz (the effective switching frequency)

$$\left|R_c + \frac{1}{2\pi \cdot 5\,000 \cdot Cj}\right| = 0.21\ \Omega \quad \text{and} \quad |R_{cup} + 2\pi \cdot 5\,000 \cdot L_{lp}j| = 2.0\ \Omega. \tag{4.36}$$

This implies that the largest part of the high-frequency ripple current component i_{dhf} of i_d will flow through the filter capacitor, while most of the low-frequency component i_{dlf} of i_d will flow through the primary side of the injection transformer. Simple estimates of the magnitudes of the ripple current component of i_d versus its low-frequency component show that the ripple current component is smaller than the low-frequency component for the experimental cases considered. Since $R_{lf} + R_c = 14.5$ mΩ is significantly smaller than $R_{lf} + R_{cup} = 0.22\ \Omega$, the losses associated with the ripple current component of i_d can be ignored. For this reason the effect of the filter capacitor can be ignored in Figure 4.17.

2. Some attention should be given to the influence of the skin effect on the ESR of the filter inductors. The skin depth in copper equals 9.3 mm at 50 Hz and 0.93 mm at 5 kHz. As mentioned on p. 170 the conductor used to wind the filter inductors consists of strands with a diameter of 0.28 mm. Hence the influence of the skin effect on the ESR of the filter inductor is not taken into account. The primary side of the injection transformer is wound with solid-core copper conductor with a diameter of 5 mm. By remark 1 above, mainly low-frequency current components flow through the injection transformer. For this reason the skin effect is also not taken into account in the copper resistance R_{cup} of the injection transformer. Furthermore, since the magnetic flux path associated with the

leakage inductance is mainly in air, the effect of the transformer core losses on R_{cup} can be ignored.

3. The effects of the converter losses and blanking time are not taken into account in the theoretical model. A model including the effect of the converter losses was partially derived for ordinary switching. Some of the problems associated with deriving such a model are:

   (a) The on-state voltages and on-state resistances of the IGBTs and the free-wheeling diodes differ.

   (b) The on-state voltages of these devices are in effect non-linear resistors. At high currents their equivalent resistance is small and increases as the current decreases.

   (c) The switching losses depend on both the filter inductor current and the DC-bus voltage.

   (d) To take the effect of blanking time on the d circuits into account, all the actual filter inductor currents have to be known. Hence the d circuits no longer function independently of the t circuit, even with ordinary switching.

   It will soon be shown that the results of the theoretical model and the practical results agree closely when the reference function is relatively large (in other words for a modulation index approaching 1). For small values of the reference function, the two sets of results differ. Initial investigations show that this may mainly be due to the effect of the blanking time. For a reference function with an amplitude of 0.1 the maximum time that each full-bridge converter is not in the zero state is 20 μs, while the blanking time is 5 μs.

   Although the factors discussed here do result in differences between the experimental and theoretical results, they have no serious implications concerning the operation and the stability of the converter. Moreover, this does not imply any significant changes to the basic understanding of the balancing mechanisms gained in Chapter 3.

4. Based on the previous remarks, the value of the filter inductance L used in the simulations is given by $L = L_f + L_{lp} = 262$ μH. The value of the total parasitic resistance R is given by $R = R_{lf} + R_{cup} = 220$ mΩ.

5. The theory of Chapter 3 gives upper and lower bounds for the time constant associated with the DC-bus recovery in the case of ordinary switching. By remark 3 on p. 93 the minimum time constant for ordinary switching τ_{min} is equal to $\frac{L}{R} = 1.2$ ms. The maximum time constant of recovery τ_{max} is equal to the time constant associated with the DC-bus capacitors and their bleeding resistors of 72.6 s (see p. 181).

6. In the practical system an inductive load is used as opposed to the resistive load of the theoretical model. Recall from Chapter 3 that when interleaved switching is applied, high-frequency d circuit ripple currents (associated with twice the switching frequency) flow through the load. The losses associated with these currents form part of the balancing mechanism. However, given the relatively large impedance of the load (equal to 35 jΩ), at the effective switching frequency, the effect of these currents will be small compared to the other balancing mechanisms and their effect can be ignored. For this reason the load resistance is set to 10 kΩ in the theoretical model, forcing the load current to be small enough that it can be ignored.

7. The theoretical model only makes provision for a bus resistance R_b. As was shown in Chapter 3, R_b has little influence on the balancing mechanisms at relatively high switching frequencies. For the simulations of this chapter the bus resistance R_b is chosen arbitrarily as 0.1 Ω.

8. The theoretical value of the DC-bus capacitance C_d of each full-bridge converter is 26.4 mF (see p. 178). These capacitors have a tolerance of -10% to $+30\%$. Measurements of the actual DC-bus capacitances were carried out by discharging the individual DC-bus capacitor banks into a resistor and measuring the time constants. This yielded an average value of 28 mF as shown in Table 4.7.

As a first step in the experimental evaluation of the balancing properties a sinusoidal reference function was applied to the PWM modulator. This is followed by a study of the transient balancing properties using a non-sinusoidal reference function.

At the start of each experiment the IGBT switches of all three converters were turned off and the DC-bus capacitors were charged by slowly decreasing the triggering angle of the thyristor-controlled rectifier. A 180 Ω resistor was connected to the DC-bus of the bottom converter (converter 3 of Figure 3.28) in order to create unbalance in the three DC-bus voltages. After the DC-bus voltages had stabilized the 180 Ω resistor was switched out and the modulation process was started.

Both interleaved and ordinary switching were applied and the three DC-bus voltages were measured during the rebalancing process. The ground of the oscilloscope was connected to the negative DC-bus terminal of the bottom converter (converter 3), with probes connected to the positive terminals of the DC-buses of each of the three full-bridge converters. Due to the distances between the three full-bridge converters and the EMI generated by the converters and the isolated gate-drive circuits, some noise can be observed on the measured results. The three DC-bus voltages v_1, v_2 (see Figure 4.10) and v_3 were calculated from the measured results. (Measurements of v_3, $v_3 + v_2$ and $v_3 + v_2 + v_1$ were available.) The d and t voltages were calculated from the measured results by making use of equation 3.131.

A	Ordinary Switching			Interleaved Switching		
	Figure	τ_t (s)	τ_m (s)	Figure	τ_t (s)	τ_m (s)
0.85	4.18	0.020	0.02	4.19	0.020	0.02
0.6	4.20	0.040	0.04	4.21	0.040	0.04
0.3	4.22	0.160	0.2	4.23	0.160	0.2
0.1	4.24	1.433	2.8	4.25	1.433	2.8

Table 4.8: Transient behavior theoretical and experimental results.

The three filter inductor currents could not be measured accurately over the rebalancing period due to aliasing problems resulting from the high-frequency ripple currents.

In the first set of measurements a 50 Hz sinusoidal reference function of the form

$$f_r(t) = A\sin(2\pi \cdot 50t) \tag{4.37}$$

with A equal to 0.85, 0.6, 0.3 and 0.1 was used.

Simulations were carried out by making use of the techniques of Chapter 3 and the parameters of Table 4.7. The initial voltages used in the simulation were calculated from the initial measured values of the three DC-bus voltages. The initial currents were zero. Equation 3.132 was used to calculate v_1, v_2 and v_3 from the d and t voltages. Recall from Chapter 3 that all voltage sources were set to zero for the transient analysis. However, when calculating v_1, v_2 and v_3, the initial value of v_t (which is equal to the total DC-bus voltage divided by 3) is used. It should, however, be noted that the actual value of v_t decreased during the measurement period due to the effect of the supply impedance. This introduced some deviations between the measured and theoretical values of v_1, v_2 and v_t.

Table 4.8 summarizes the amplitude of the reference functions, measured and theoretical time constants and the figure numbers where the results appear. The theoretical time constants are denoted by τ_t, while the measured time constants are denoted by τ_m. The measured time constants were read from these figures and are subject to some inaccuracy.

A number of remarks concerning the measured and theoretical results can be made:

1. As mentioned above the measured results contain some noise due to the geometry of the physical setup and the electromagnetically noisy environment. These are most visible in voltages v_{d_1} and v_t due to the voltage scale of the figures.

2. Little difference can be observed between the results for ordinary and interleaved switching in both the measured and theoretical results. This is in agreement with the theory for relatively high switching frequencies. The main difference between the two is that v_{d_1}

remains at its initial condition of -2 V for ordinary switching, while it goes to 0 V for interleaved switching. In order to study the difference between interleaved and ordinary switching further, the switching frequency was lowered to 500 Hz and the experiments were repeated. No significant difference could be measured between the recovery time constants for ordinary and interleaved switching, both in the experimental and simulated results. The reason for this seems to be the relatively large copper resistance of the injection transformer primary windings. When using a full-scale injection transformer the differences in the time constants for ordinary and interleaved switching may be more significant.

3. The differences between the measured and theoretical values of v_t, v_1, v_2 and v_3 towards the end of the recovery period are due to the fact that the initial value of v_t was used in the theoretical results. As explained above the actual value of v_t decreased during the recovery period.

4. The experimental and theoretical values of v_{d_2} agree closely for the first three cases ($A = 0.85$, $A = 0.6$ and $A = 0.3$). Both the rate of decrease and the basic waveforms of the results agree. Some differences arise towards the end of the recovery period.

5. For the amplitude of the reference function equal to 0.1 the differences between the measured and theoretical results are more significant. The theoretical time constant is 1.433 s, while the measured time constant is 2.8 s. This can be attributed to the fact that the converter losses and blanking time were not taken into account in the theoretical model, as remarked above. Given the fact that the blanking time is large compared to the maximum duty cycle it is suspected that the difference is mainly due to this non-ideality. A more detailed investigation will be required to fully understand and evaluate this phenomenon.

In the final part of this section the transient balancing properties of the three-level series-stacked converter with a non-sinusoidal reference function are evaluated. At the same time the effect of the load on the balancing properties is evaluated. The experimental setup and measurement procedures are the same as in the previous section, with the load inductors disconnected for some of the experiments.

The reference function

$$f_r(t) = 0.5\sin(2\pi \cdot 50t) + 0.2\cos(2\pi \cdot 250t) + 0.1\cos(2\pi \cdot 650t) \tag{4.38}$$

is used.

Figure 4.26 (a) and (b) shows the measured and theoretical waveforms of voltage v_{d_2} for ordinary switching. Case (a) has the inductive load connected, while case (b) has the load inductor

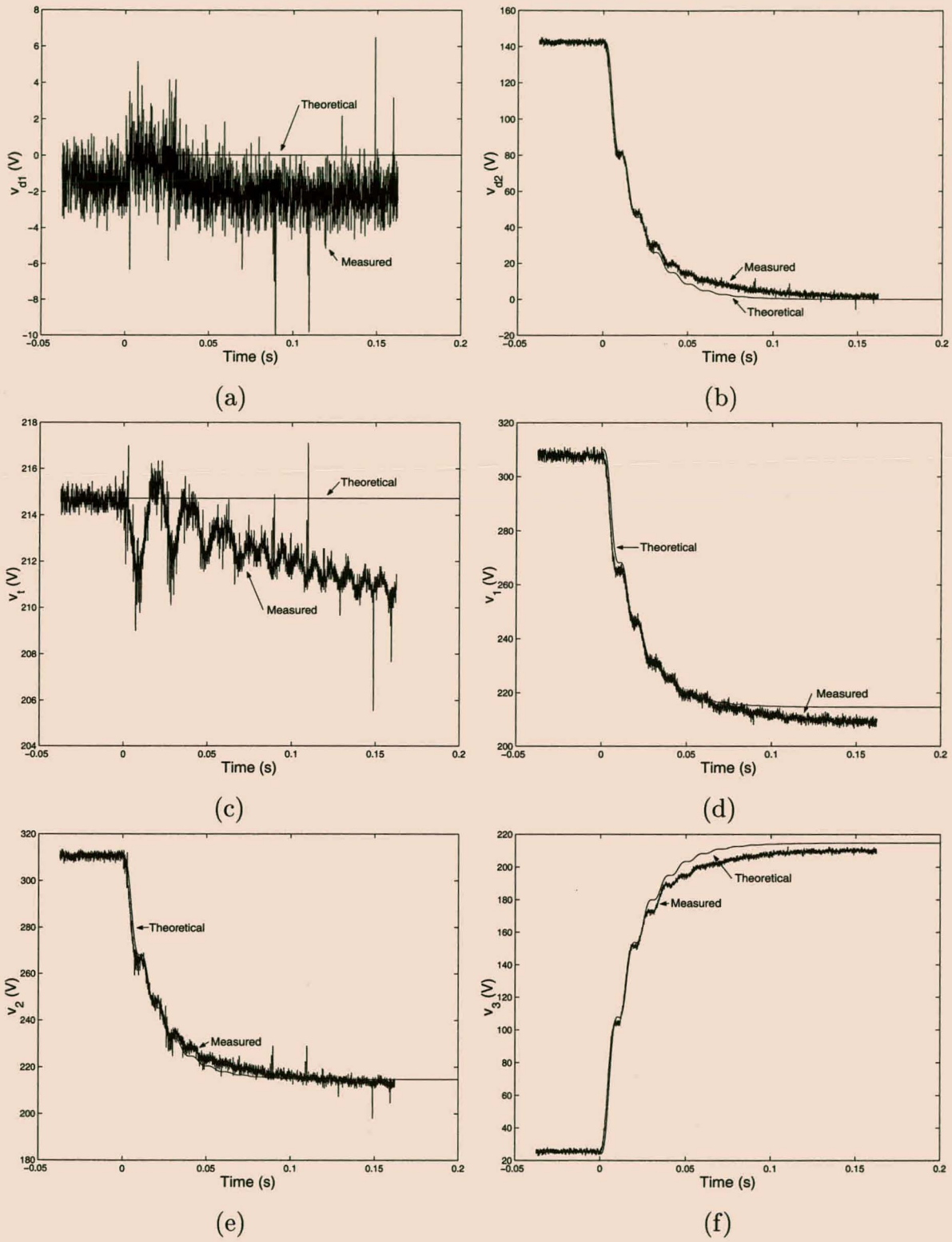


Figure 4.18: Ordinary switching measured and theoretical DC-bus voltage waveforms with a sinusoidal reference and $A = 0.85$.

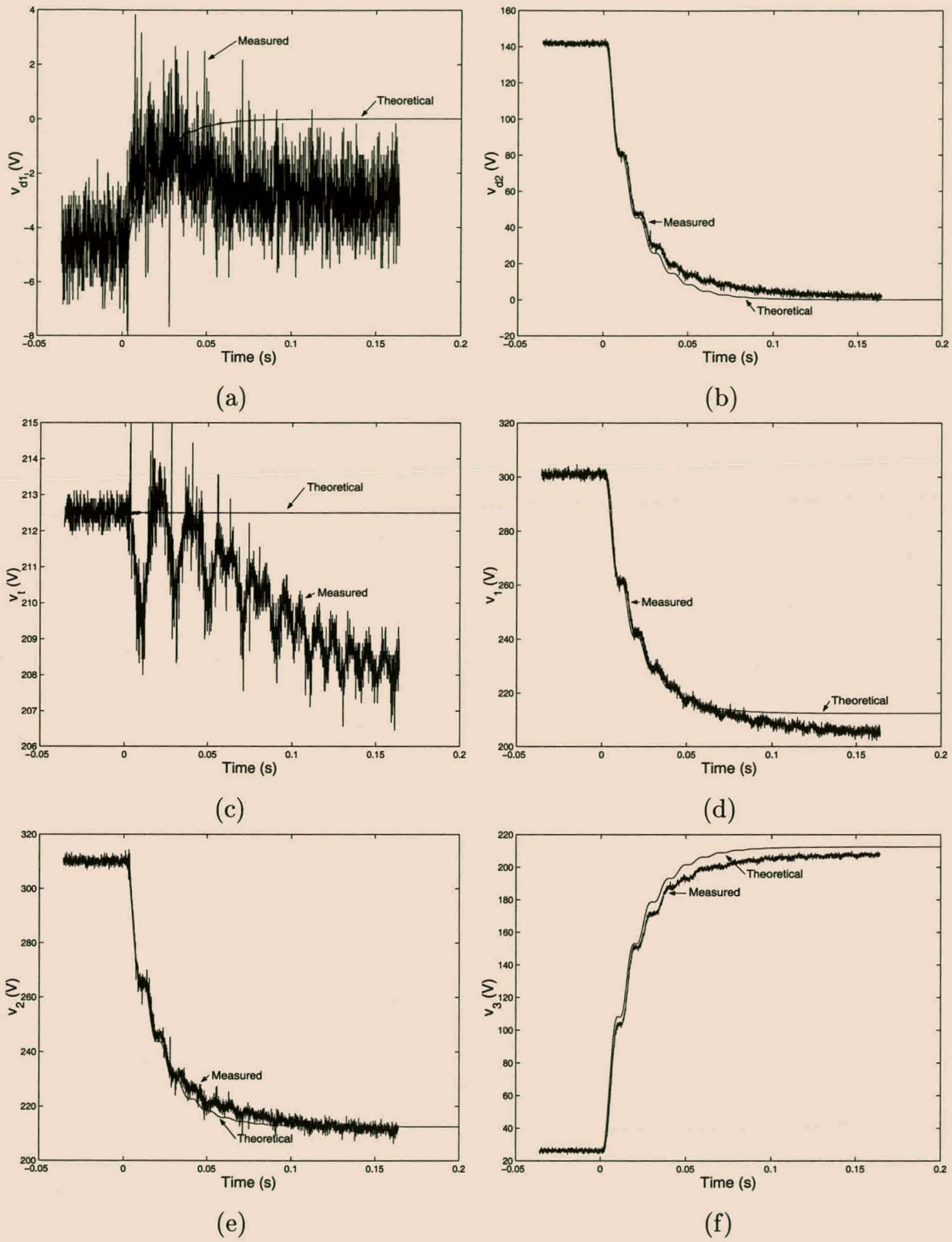


Figure 4.19: Interleaved switching measured and theoretical DC-bus voltage waveforms with a sinusoidal reference and $A = 0.85$.

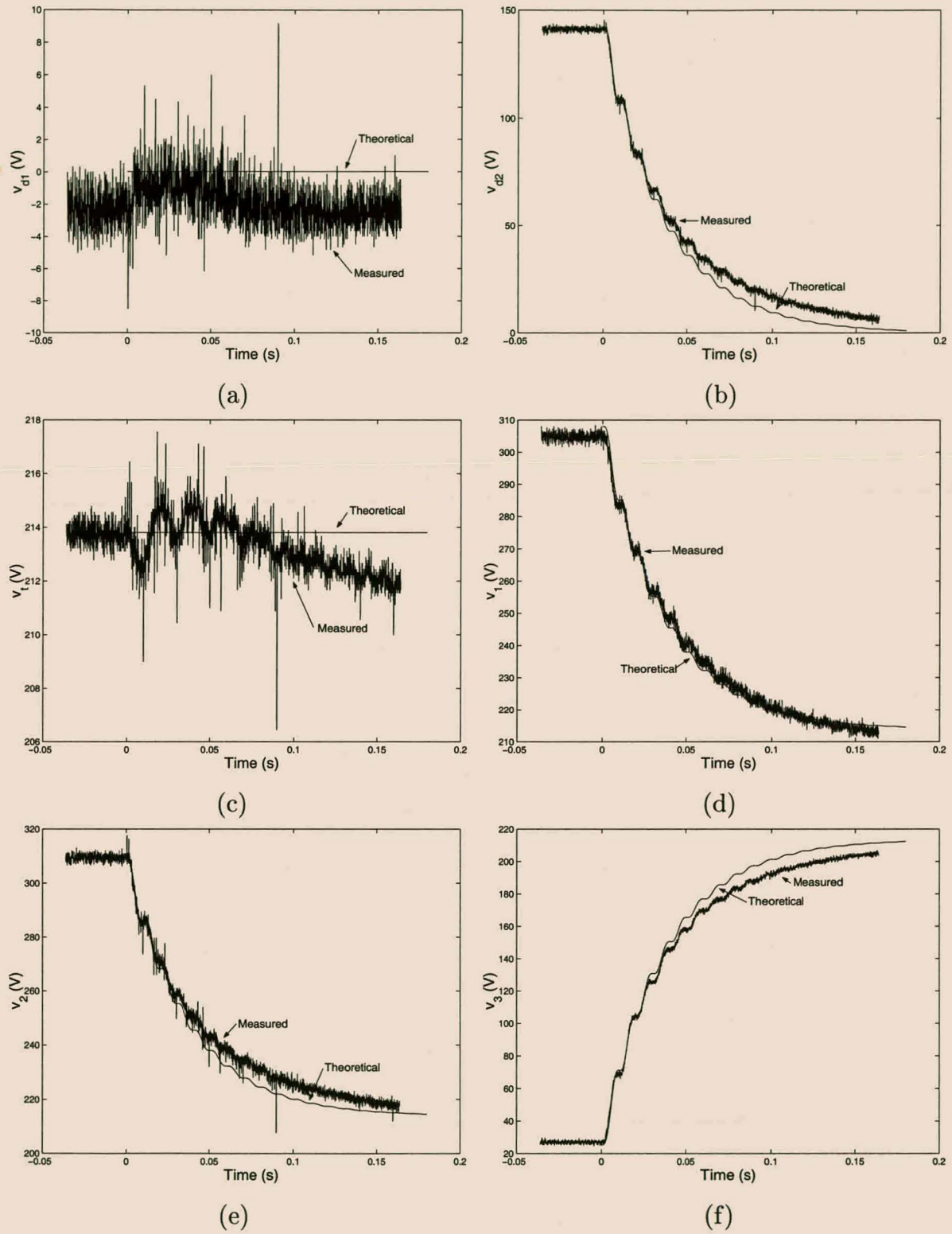


Figure 4.20: Ordinary switching measured and theoretical DC-bus voltage waveforms with a sinusoidal reference and $A = 0.6$.

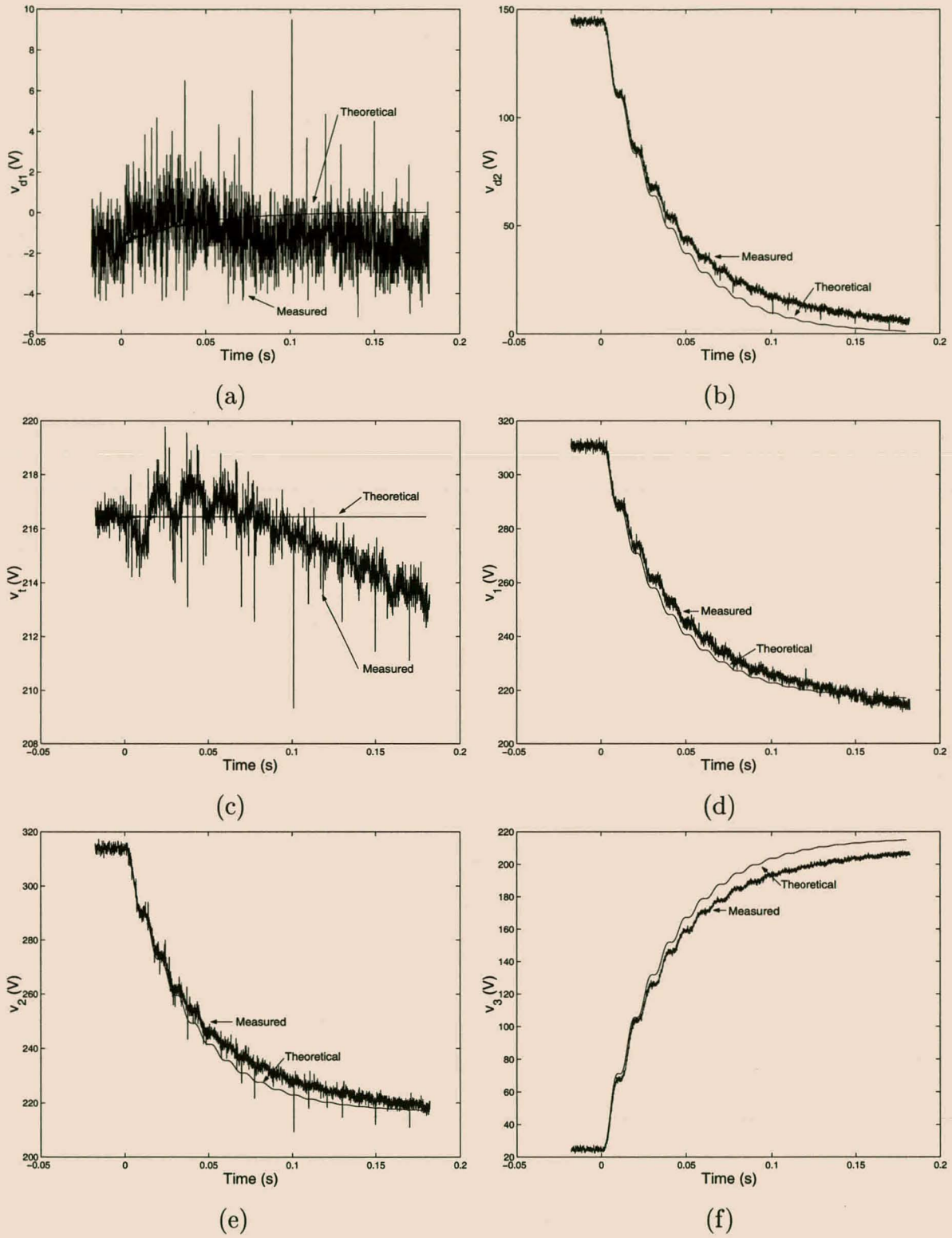


Figure 4.21: Interleaved switching measured and theoretical DC-bus voltage waveforms with a sinusoidal reference and $A = 0.6$.

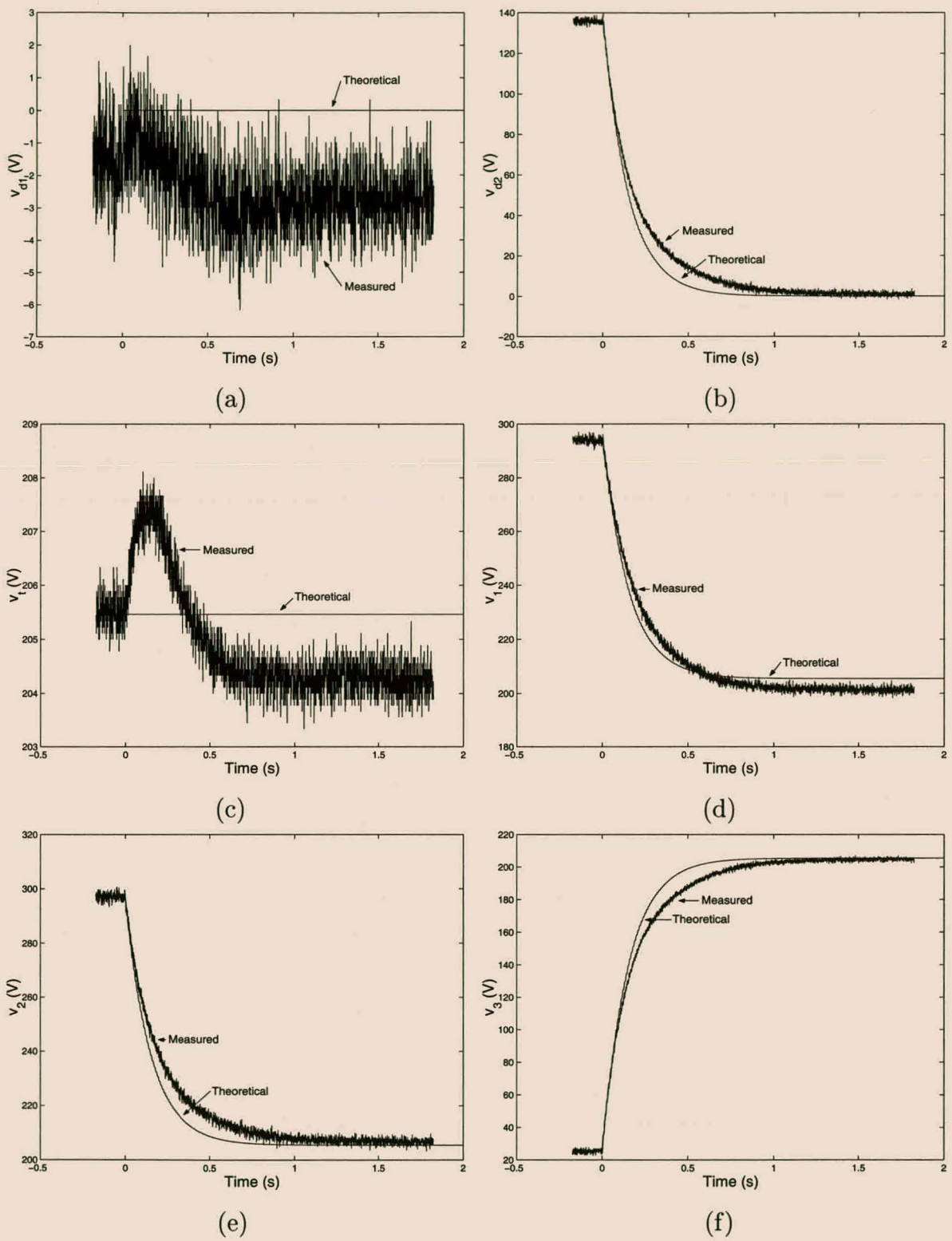


Figure 4.22: Ordinary switching measured and theoretical DC-bus voltage waveforms with a sinusoidal reference and $A = 0.3$.

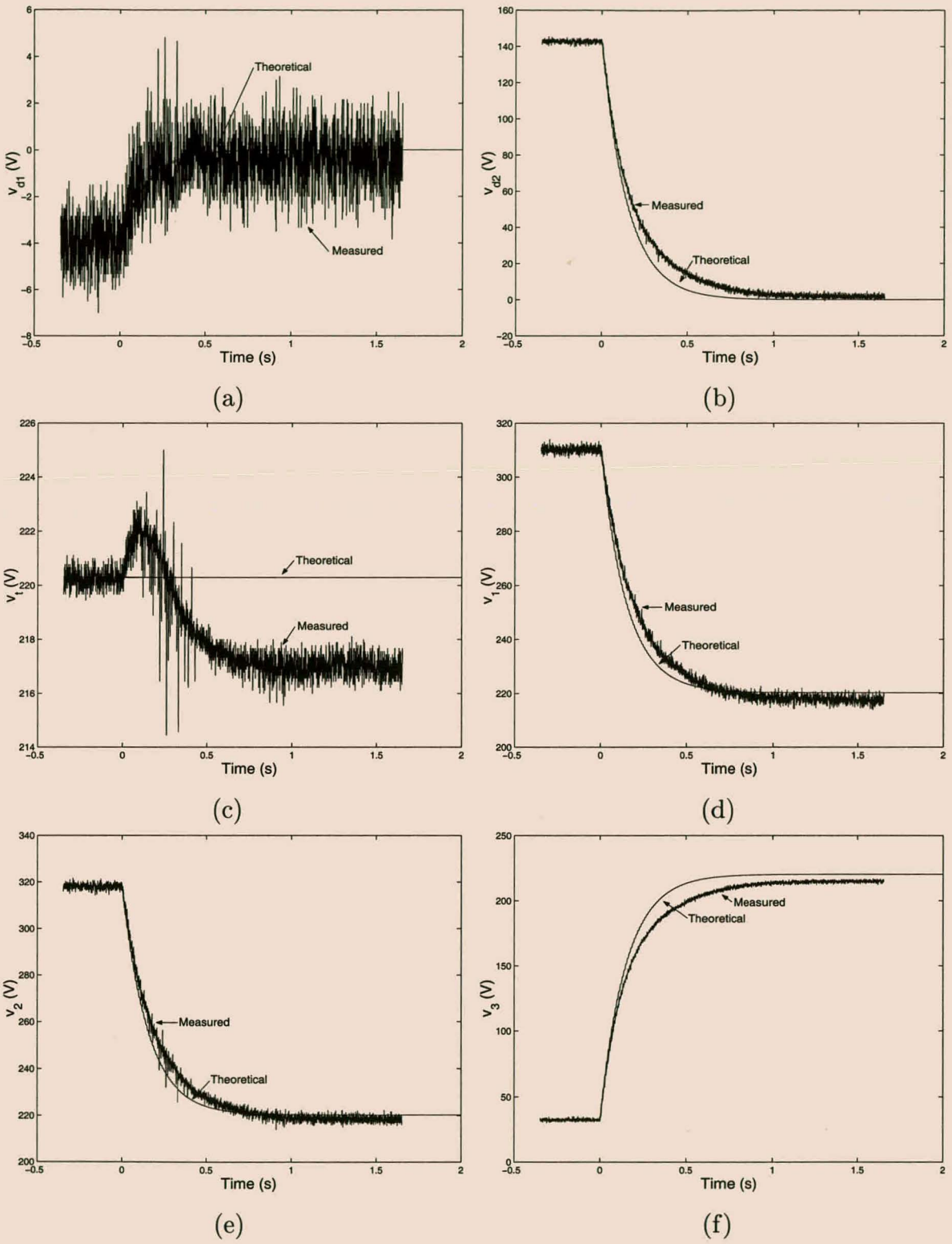


Figure 4.23: Interleaved switching measured and theoretical DC-bus voltage waveforms with a sinusoidal reference and $A = 0.3$.

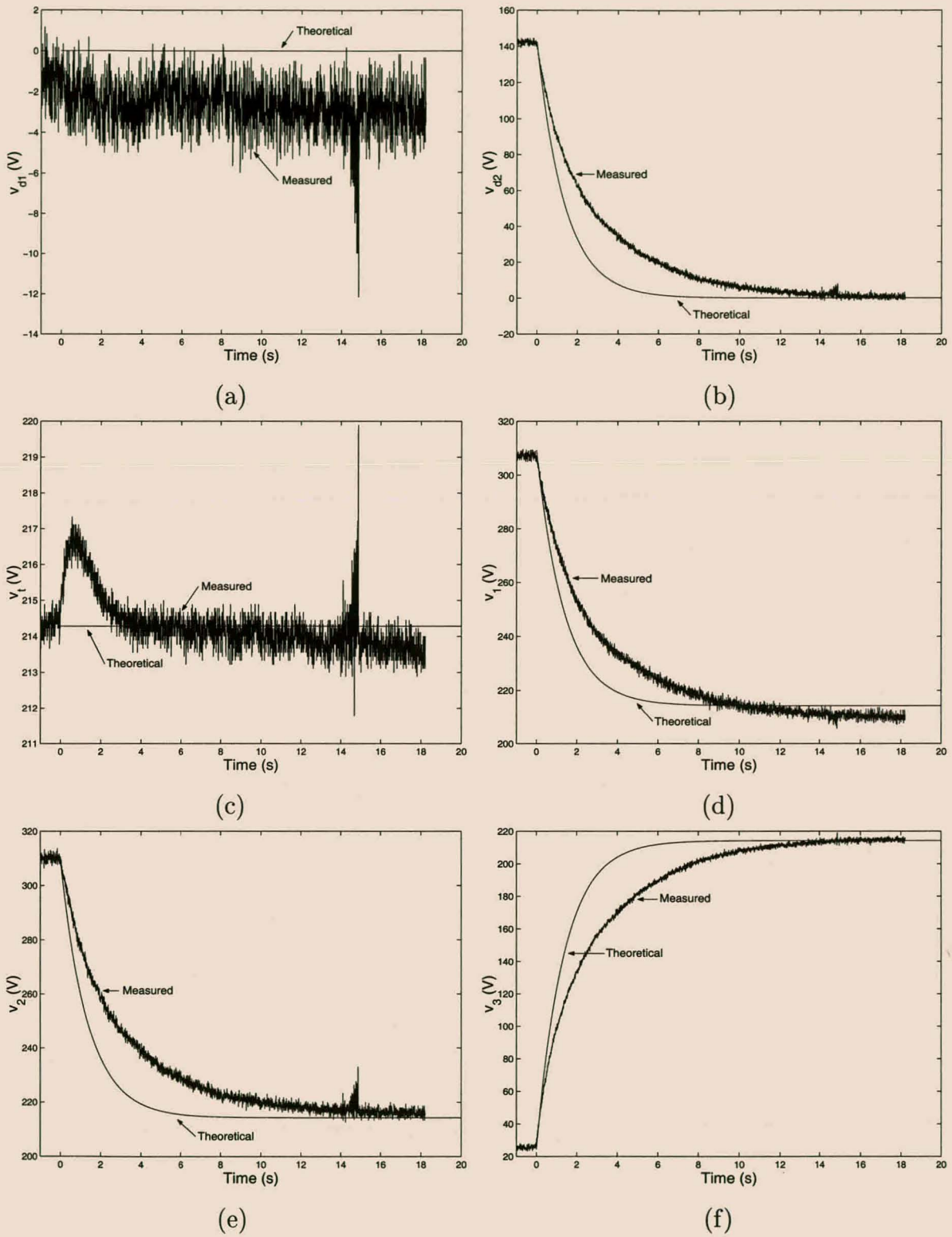


Figure 4.24: Ordinary switching measured and theoretical DC-bus voltage waveforms with a sinusoidal reference and $A = 0.1$.

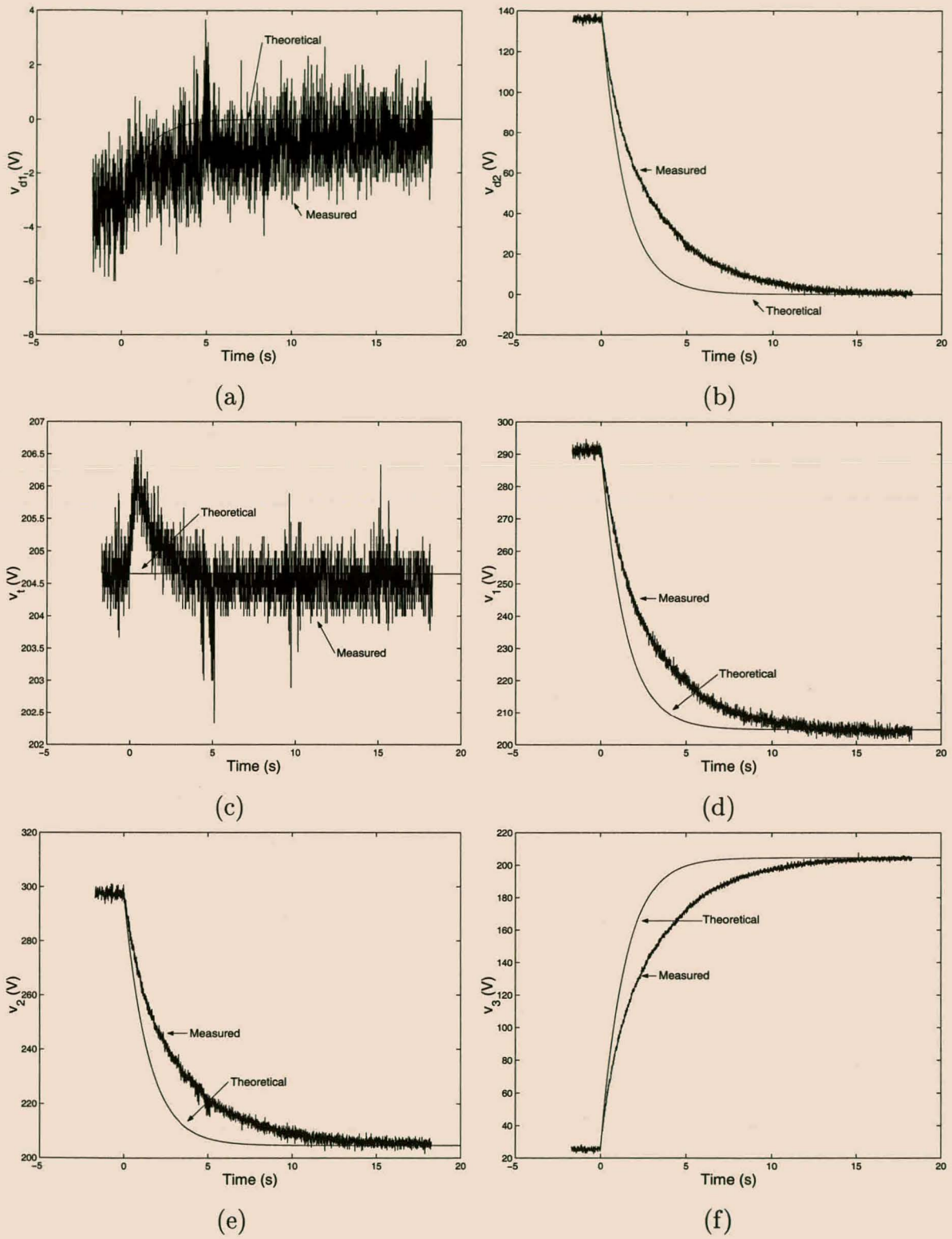


Figure 4.25: Interleaved switching measured and theoretical DC-bus voltage waveforms with a sinusoidal reference and $A = 0.1$.

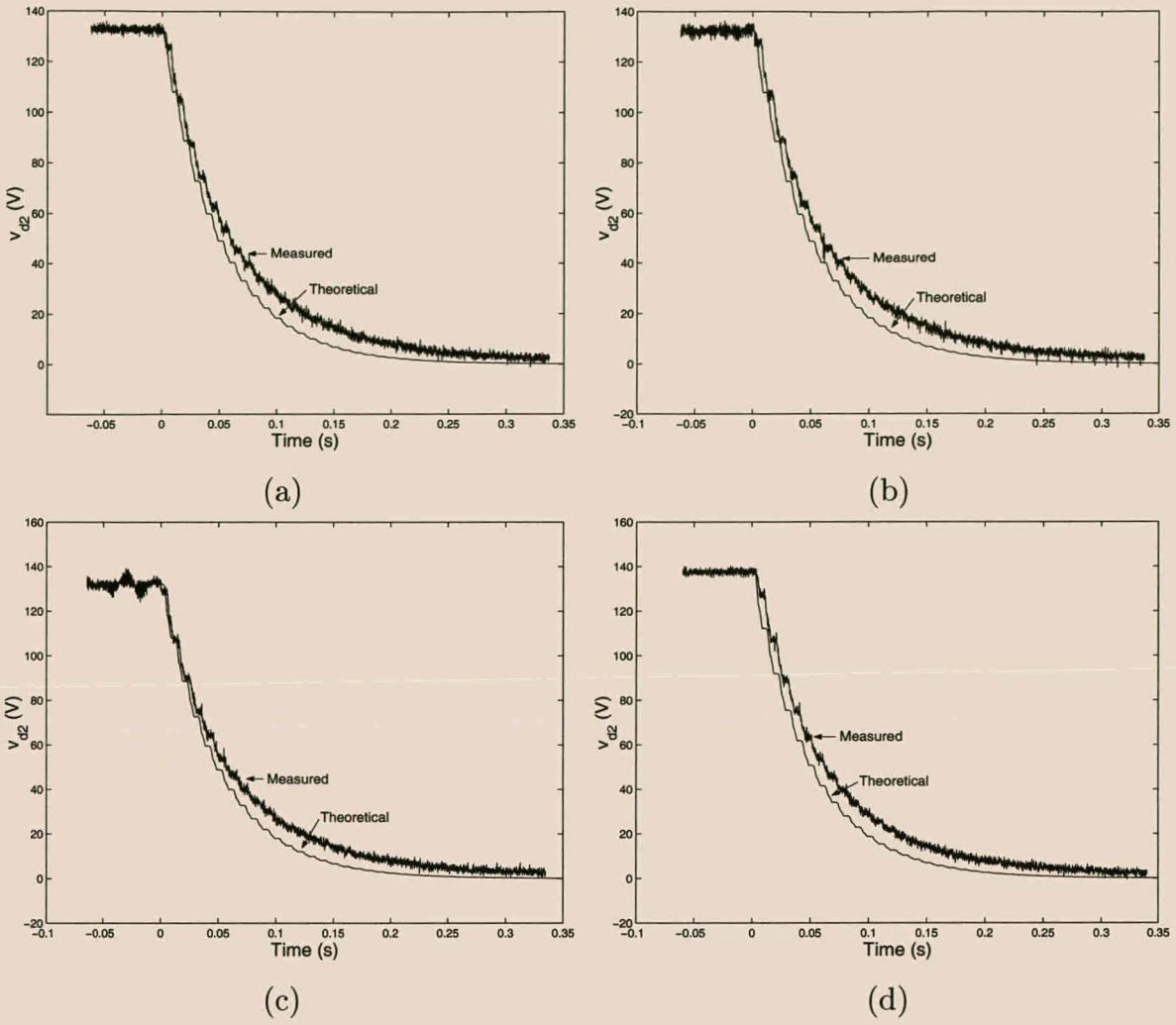


Figure 4.26: DC-bus balancing with a non-sinusoidal reference function.

disconnected. Cases (c) and (d) of this figure show the results for interleaved switching. Case (c) has the load connected, while the load is disconnected in case (d). Very little difference can be observed between the four sets of results. Although it appears that the recovery of v_{d_2} may be slightly faster for interleaved switching, this is not confirmed by the simulations. For both interleaved and ordinary switching the theoretical time constant is equal to 0.51 s. These results confirm the fact that the load has little effect on the balancing mechanisms, especially at relatively high switching frequencies. This is in agreement with the theory of Chapter 3.

4.4.2.2 Steady-state results

In this section the steady-state DC-bus balancing properties of the experimental series-stacked phase-arm are evaluated. The experimental setup is the same as in the previous section. Throughout this section the LEM current sensors of the converter's measurement system are used to obtain the measured results. The three filter inductor currents i_1, i_2 and i_3 are measured.

Figure	Ordinary Switching			Interleaved Switching		
	V_1 (V)	V_2 (V)	V_3 (V)	V_1 (V)	V_2 (V)	V_3 (V)
$f_r(t) = 0.85\sin(2\pi \cdot 50t)$						
4.27	193	192	193	195	192	194
$f_r(t) = 0.5\sin(2\pi \cdot 50t) + 0.2\sin(2\pi \cdot 250t) + 0.1\cos(2\pi \cdot 550t) + 0.1\sin(2\pi \cdot 650t)$						
4.28	197	195	198	192	190	191
$f_r(t) = 0.3\sin(2\pi \cdot 50t) + 0.2\cos(2\pi \cdot 550t) + 0.3\sin(2\pi \cdot 5500t)$						
4.29	190	192	193	104	283	135

Table 4.9: Steady-state behavior theoretical and experimental results.

From these measured results i_{d_1}, i_{d_2} and i_t are calculated by making use of equation 3.131. The average values of the DC-bus voltages are measured by making use of the isolated voltage measurement system of the converter.

Unlike in the previous section the measured results are not compared with theoretical simulations. As mentioned earlier, the theoretical model does not make provision for the inductive load. The steady-state DC-balancing properties are evaluated with a number of different reference functions.

Table 4.9 summarizes the different reference functions used, figure numbers where the results appear and average measured DC-bus voltages. Refer to Figure 3.27 of p. 129 for the definition of voltages V_1, V_2 and V_3.

In the first set of results a 50 Hz sinusoidal reference function is used, while a reference function containing harmonics up to the thirteenth harmonic is used for the second set. In the final experiment a deliberate attempt is made to create unbalance in the three DC-bus voltages by introducing a harmonic near the effective switching frequency into the reference function.

Some remarks concerning the experimental results for the first two reference functions (Figures 4.27 and 4.28) can be made:

1. The output voltage waveform contains a number of irregularities. This can be attributed to the effect of blanking time and other non-idealities like the difference in diode and IGBT on-state voltages on the operation of the converter. Observe that as a result of the relatively large ripple current components, i_1, i_2 and i_3 have zero crossings during almost every switching period. This is due to the fact that the total converter output current is small compared to its rated current, for which the filter inductors were designed.

2. As expected, the ripple in the output voltage is smaller for interleaved switching than for

ordinary switching.

3. The d circuit currents are relatively small for ordinary switching, while the t circuit current contains a large ripple current component.

4. In the case of interleaved switching, the d circuit currents consist of high-frequency components, while the t circuit current has a significantly smaller ripple component than in the case of ordinary switching.

5. The unbalance in the three DC-bus voltages is negligible for both ordinary and interleaved switching.

In the third experiment a harmonic near twice the switching frequency is included in the reference function. The presence of this harmonic causes severe unbalance in the three DC-bus voltages when interleaved switching is used, as predicted by the theory of Chapter 3. The largest unbalance is between v_1 and v_2, with a difference of 179 V. This is equal to 34% of the total DC-bus voltage.

The unbalance in the three DC-bus voltages also gives rise to relatively large low-frequency d circuit currents. This can be interpreted as an attempt of the natural balancing mechanisms to correct the unbalance. Further confirmation of this fact can be found by observing that a marked increase in the converter DC supply current was measured when interleaved switching was applied. The supply current increased from 5 A for ordinary switching to 10 A for interleaved switching. This gives rise to a drop in the total DC-bus voltage from 575 V to 552 V.

For ordinary switching the bus voltages and filter inductor currents are balanced, as predicted by the theory.

An important question that has not yet been addressed is the effect of parameter sensitivity on the balancing properties of the three-level series-stacked converter. No special attempt was made to ensure that the three sets of DC-bus capacitors, filter inductors and filter capacitors were balanced. However, the steady-state balancing properties of the experimental system were better than originally expected. To further study this question some of the DC-bus filter capacitors were removed and extra inductance was added to one of the levels. This had almost no influence on the steady-state average values of the three DC-bus voltages.

These preliminary findings should, however, be treated with a certain amount of caution. A more complete experimental evaluation, backed by a theoretical model, should be carried out. The fact that, for the current set of experiments, the converter supplies mainly reactive power to the load should also be kept in mind.

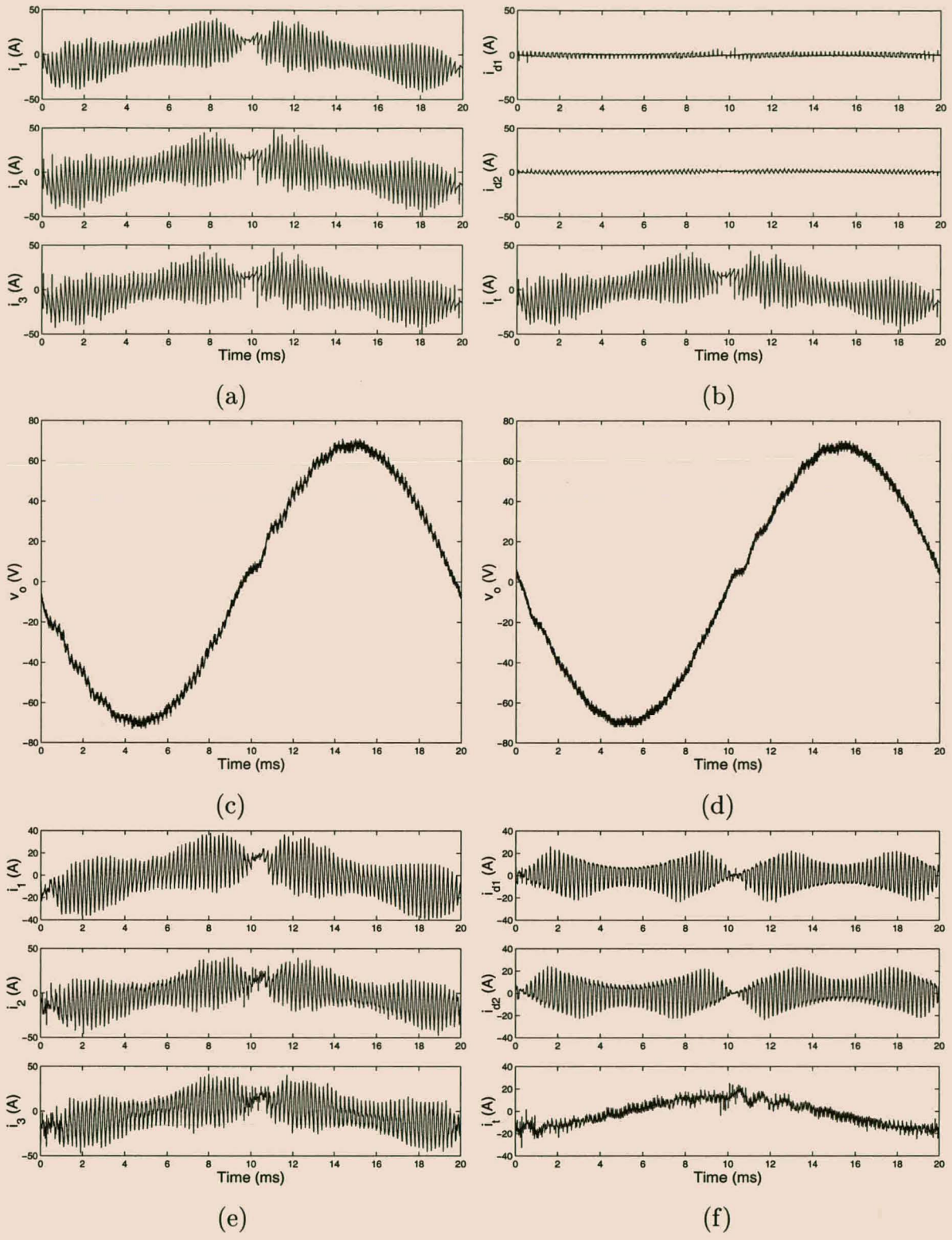


Figure 4.27: Steady-state current waveforms for $f_r(t) = 0.85\sin(2\pi \cdot 50t)$. (a)-(c): ordinary switching, (d)-(f): interleaved switching.

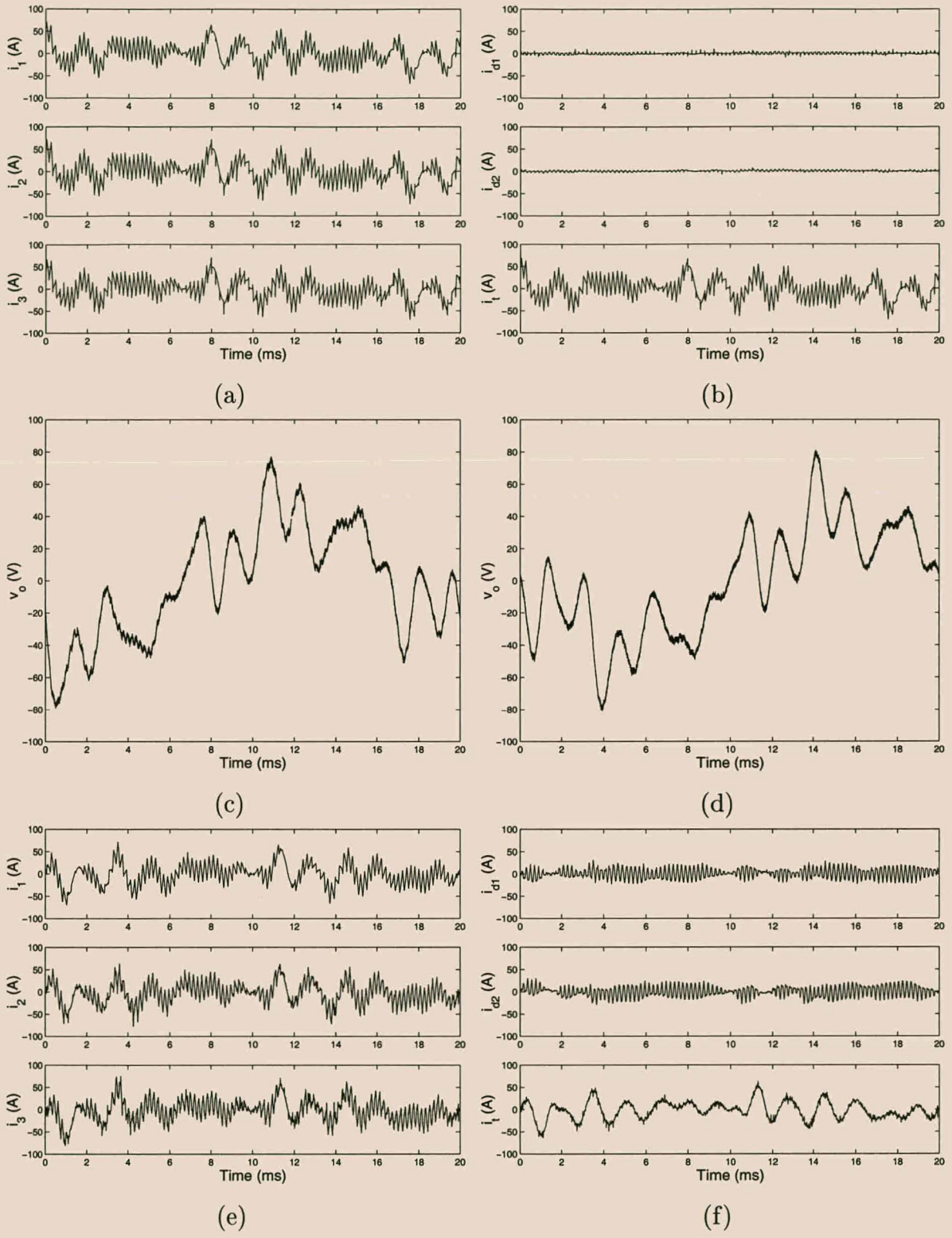


Figure 4.28: Steady-state current waveforms for $f_r(t) = 0.5\sin(2\pi \cdot 50t) + 0.2\sin(2\pi \cdot 250t) + 0.1\cos(2\pi \cdot 550t) + 0.1\sin(2\pi \cdot 650t)$. (a)-(c): ordinary switching, (d)-(f): interleaved switching.

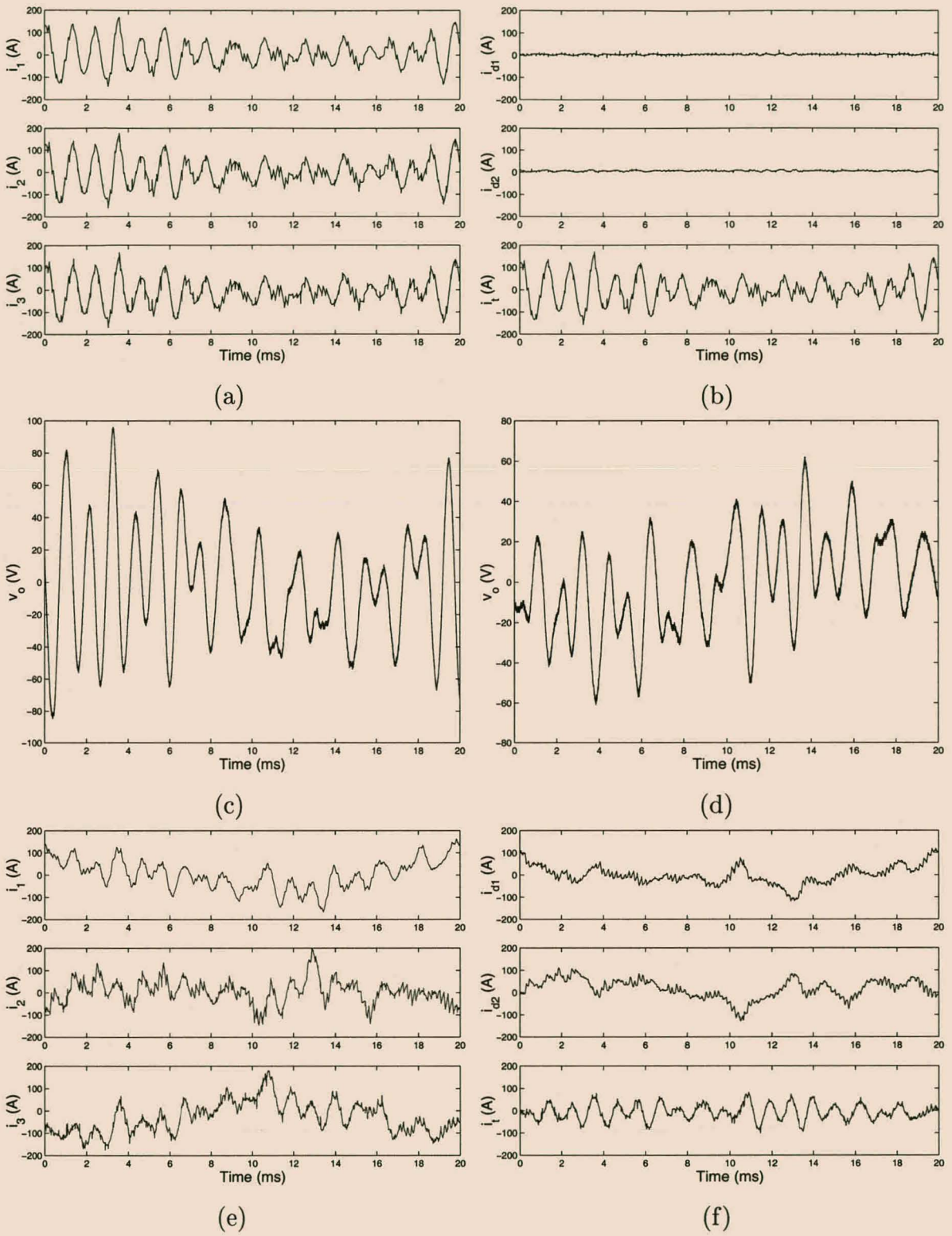


Figure 4.29: Steady-state current waveforms for $f_r(t) = 0.3\sin(2\pi \cdot 50t) + 0.2\cos(2\pi \cdot 550t) + 0.3\sin(2\pi \cdot 5500t)$. (a)-(c): ordinary switching, (d)-(f): interleaved switching.

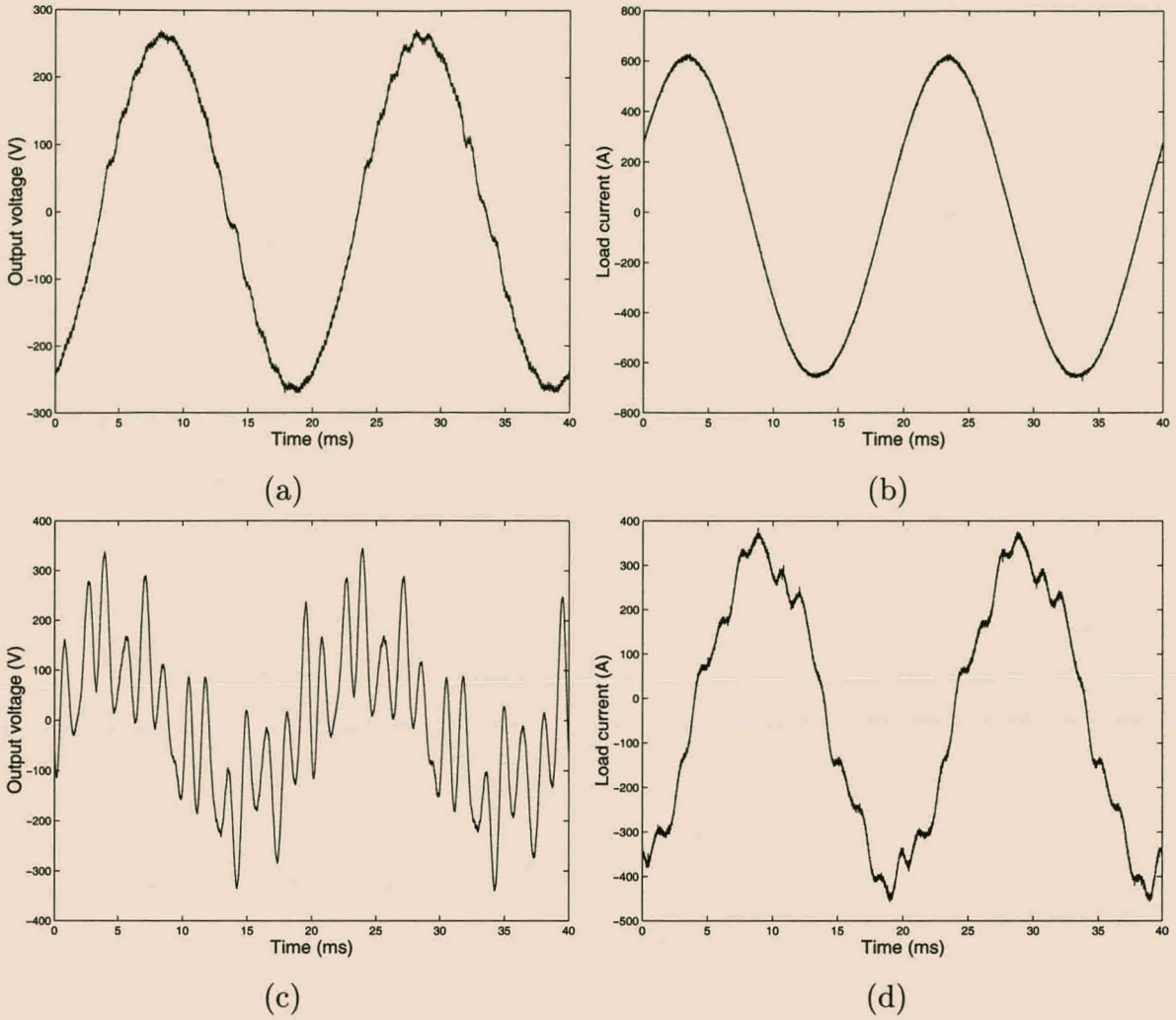


Figure 4.30: Output voltage and load current at a DC-bus voltage of 2.2 kV.

4.4.3 High DC-bus voltage results

In the final set of experimental results the operation of the three-level series-stacked phase-arm is evaluated at a DC-bus voltage of 2.2 kV. This is within 10% of the nominal value and is the highest bus voltage that could be obtained with the current step-up transformer. Interleaved switching is used for all the experimental results of this section.

In the first experiment the reference function

$$f_r(t) = 0.85 \sin(2\pi \cdot 50t) \tag{4.39}$$

is again used. The output voltage (secondary side transformer voltage) v_o is shown in Figure 4.30(a), while Figure 4.30(b) shows the load current. The effect of the converter non-idealities, in particular the blanking time, is again clearly visible on the output voltage. Note that the peak value of the output current is equal to 640 A, with an RMS value of 453 A. This is 1.5 times the rated output current of the injection transformer. This accounts for a larger than

expected voltage drop across the transformer. The three DC-bus voltages were again almost perfectly balanced with $V_1 = 738$ V, $V_2 = 735$ V and $V_3 = 736$ V.

In the final experiment a non-sinusoidal reference function of the form

$$f_r(t) = 0.5\sin(2\pi \cdot 50t) + 0.2\sin(2\pi \cdot 250t) + 0.2\sin(2\pi \cdot 650t) \tag{4.40}$$

is used. The results are shown in Figure 4.30. The average steady-state DC-bus voltages were: $V_1 = 744$ V, $V_2 = 739$ V and $V_3 = 740$ V.

4.5 Summary

This chapter described the design and experimental evaluation of an experimental 700 kVA three-level series-stacked phase-arm. While the power electronic converters were designed for the full 700 kVA rating, the injection transformer was designed for a 70 kVA rating. A design overview of the different components was presented followed by an experimental evaluation of the system.

The design of the following components was discussed:

- The injection transformer.
- The output filters.
- The full-bridge converter building-blocks.
- The controller and measurement system.

In the first part of the experimental evaluation the transient balancing properties of the phase-arm were evaluated and compared with the theory of Chapter 3. Both sinusoidal and non-sinusoidal references were applied. It was found that the simulation and measured results correspond well when the amplitude of the reference function (modulation index) is relatively large. For smaller values of the reference function some differences between the two sets of results can be observed. This can be attributed to converter non-idealities, for instance, the effect of blanking time.

In the second part of the experimental evaluation the steady-state balancing properties are evaluated. In general the DC-bus voltages are well balanced with only 2 or 3 V difference between them. The only exception is the case where a harmonic near twice the switching frequency is added to the reference function. This results in severe unbalance in the case of interleaved switching, as predicted by the theory of Chapter 3.

Finally the operation of the converter at rated bus voltage is illustrated.

Chapter 5

Summary and conclusions

This final chapter summarizes the research contribution and the main conclusions from this thesis. Possible future research questions as a result of the research are identified.

5.1 Contributions of and conclusions from this study

- In the first part of Chapter 2 a new resonant turn-off snubber topology was introduced. This snubber topology is derived from the ARCP. Its main feature is the fact that the peak current rating of the auxiliary switches is small compared to the current rating of the main switches. The following aspects of the new snubber circuit were investigated:

  1. The basic theory, describing the snubbers operating principles, was derived.
  2. A detailed analysis of the different losses involved in the main IGBT and snubber circuit was carried out by using simple tail-forming models of IGBT switching behavior. The losses in a number of different parasitic components were included in this analysis.
  3. Based on the loss calculations, an optimal snubber design procedure was developed. The aim is to find those values of the snubber capacitor and resonant inductor that result in the least total converter losses.
  4. The effect of the different parasitic components on the operation and efficiency of the snubber was investigated. It was found that the snubber and module parasitic inductance has a significant effect on the effectiveness of the snubber.
  5. An experimental version of the turn-off snubber was constructed at a 40 kVA level. The experimental turn-off voltage waveforms agreed well with the results from the theoretical model. It was, however, found that the simple tail-current model of the IGBT is not accurate during the first part (current fall time) of the turn-off cycle.

This inaccuracy in the model appears to be related to the snubber and main module parasitic inductance as well as the forward recovery of the snubber diode.

6. A calorimetric technique was used to measure the total converter losses with and without the snubber. The measured and theoretical results agreed well with a maximum difference of 15% between the two.

7. Based on these loss measurements and the data sheet values of the main module losses it is estimated that the snubber reduces the total converter switching losses by between 37% and 50% under sinusoidal modulation.

- In the final part of Chapter 2 a turn-on snubber was added to the turn-off snubber topology. This combined snubber targets the effects of both the turn-on and turn-off transients at the expense of increased voltage stresses on the main switches. The following aspects of the combined snubber were investigated:

  1. The basic theory describing the snubbers operating principles was derived. The different compromises involved in the snubber design were discussed. This involves balancing the reduction in switching losses against the rating of the auxiliary switches and the increased voltage stresses on the main switches.

  2. An experimental version of the snubber was constructed and the basic operating principles of the snubber were experimentally verified.

- Although soft-switching provides benefits in terms of reduction in switching losses and decreased $\frac{di}{dt}$ and $\frac{dv}{dt}$, it increases the component count, complexity and cost of the system. Based on these considerations it was decided not to apply soft-switching techniques in the experimental 700 kVA series-injection converter.

- The series-stacked converter topology provides some of the benefits associated with soft switching. By applying interleaved switching the harmonic content of the output voltage waveform is reduced. In this sense the technique of interleaved switching increases the effective switching frequency.

- The series stacked converter topology leads to a high-voltage DC-bus by stacking standard full-bridge converters in series. A DC-bus voltage of 2.4 kV is required for the converter to interface directly with superconducting energy storage devices. One of the advantages of this topology is that the converter can easily be reconfigured by stacking the full-bridge converters in parallel. This opens the possibility of interfacing with other energy storage devices that requires a 800 V DC-bus. Examples of such devices are flywheels and battery banks.

- A detailed balancing theory was developed for the two- and three-level series stacked converters under ordinary and interleaved switching. The following is a summary of the key steps of this analysis:

  1. The system of differential equations describing the operation of the converter is derived.
  2. This system of differential equations is transformed by introducing d and t parameters. The use of these parameters leads to an understanding of the balancing mechanisms.
  3. Fundamental theory for systems of linear differential equations are used to study the balancing mechanisms. As a first step Liapunov's theorem is used to prove that the two- and three-level series stacked converters are stable under ordinary switching. It also shows that the losses in the system are responsible for the balancing of the DC-bus voltages and filter inductor currents.
  4. The next step in the analysis is to study the lossless case for ordinary switching. Even though a lossless converter is not practically possible, this theoretical analysis provides insight into the balancing mechanisms. In this case analytic solutions can be found for the d and t voltages and currents. An important design guideline is derived, relating the size of the DC-bus capacitor banks to that of the filter inductors.
  5. In the general case Floquet's theorem is used to determine the time constant associated with the blanking process. One way of interpreting this time constant is to associate it with equivalent balancing resistors connected to the DC-buses of the full-bridge converters. This approach provides insight into the 'strength' of the balancing mechanism.
  6. The Floquet techniques also provides a simple and time-efficient technique for numerically simulating the balancing process.
  7. A detailed study of the harmonics of ordinary and interleaved switching is carried out by making use of three-dimensional presentations of the switching functions and the theory of double Fourier series. The theory is general and applies to reference functions that are not necessarily sinusoidal.
  8. In the final part of the analysis the steady-state behavior of the two- and three-level series-stacked converters are studied. It is proven formally that the DC-bus voltages of the two- and three-level series-stacked converters will balance in the steady state if the switching frequency is chosen high enough that the following two conditions hold:

     (a) The spectra of the d switching functions and that of the reference function do not overlap in the frequency domain.

(b) The spectra of the d switching functions and that of the supply voltage do not overlap in the frequency domain.

These two conditions are satisfied if the highest frequency at which significant harmonics occur in the reference function or the supply voltage is significantly less than twice the switching frequency. (The same applies for harmonic currents as a result of nonlinear loads.)

9. A numerical method is derived for simulating the steady-state behavior of the series-stacked converter. A number of simulations are carried out to confirm the theory and to gain an understanding of the operation of the two- and three-level series stacked converters.

10. Finally it is shown that when a digital controller is used to generate the gating signals for the three-level series-stacked converter (under interleaved switching) the reference function should be updated at six times the switching frequency or faster.

- In the final part of the thesis the design and experimental evaluation of the 700 kVA three-level series-stacked phase-arm is discussed. Apart from the power electronic converter, the following hardware was developed:

  1. An optically isolated voltage measurement system. The system is designed for a full three-phase series-injection power quality device.
  2. An optical driver and receiver board. This board also makes provision for a full three-phase system.
  3. In order to obtain the required DC-bus voltage a high-voltage thyristor rectifier with a digital controller was developed. This rectifier receives a triggering angle command through an optical serial port.

- Both the transient and steady-state balancing properties of the converter were studied experimentally and compared to the theoretical predictions. In general, the experimental results agree closely with the theoretical results although converter non-idealities (like blanking time) gives rise to some differences.

- In the final part of the experimental evaluation it is shown that the converter operates successfully at its rated DC-bus voltage for both sinusoidal and non-sinusoidal reference functions.

5.2 Possibilities for future study

This study gave rise to a number of interesting new research possibilities. Some of these are currently being further pursued at the University of Stellenbosch. The following are some of the most important future research problems:

- A more detailed analysis and optimization of the turn-off snubber topology, based on more accurate device models. A detailed study of the relation between the turn-off behavior of the main IGBT, the snubber diode forward recovery and the parasitic inductance of the main module and snubber circuit should be carried out.
- Attention should be given to minimizing the parasitic inductance. One option is to integrate the main switch, snubber diode and snubber capacitor into a single module.
- The effect of the turn-off snubber on the EMI generated by a converter should be studied. This requires measurement equipment and facilities that are not currently available at the University of Stellenbosch.
- A more detailed investigation of the combined turn-on and turn-off snubber is currently being carried out under the guidance of the author. This involves the following:
    1. The operation of the combined snubber when the output current is relatively small.
    2. A detailed analysis and investigation of the converter and snubber losses.
    3. An optimal snubber design procedure.
    4. A full experimental evaluation of the topology.
    5. The development of a three-phase soft-switched converter based on this topology.
    6. An investigation of the possibility of combining the critical snubber components into a module in order to reduce the parasitic inductance.
- The balancing theory developed in Chapter 3 should be extended to three-phase converters.
- The possibility of extending this theory to diode-clamped and flying-capacitor multilevel converters should be investigated.
- A unified theory, describing the balancing properties of an arbitrary number of levels should be developed. Initial investigations point to possible differences in the theory when the number of levels is not prime.
- The effect of converter non-idealities on the balancing properties should be studied further. A theoretical analysis of the effect of parameter sensitivity should be carried out.

- It was assumed throughout this thesis that the switching frequency is an integer multiple of the frequency of the reference function. In order to avoid this assumption a Floquet theory relative to two variables is required. The possibility of extending the Floquet theory will be investigated in the near future.

- The experimental three-level series-stacked converter should be connected to a SMES device and evaluated under a variety of different operating conditions. These include field trials.

- The possibility of cost-effective transformerless dip compensators is currently being investigated under the guidance of the author.

- The converter technology described in this thesis should be industrialized. A possible industrialization of the device (in cooperation with ESKOM) is currently being considered.

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Appendix A

Resonant snubber Matlab programs

In this chapter two of the Matlab programs used in Chapter 2 are presented. The first of these programs implements the resonant turn-off snubber optimization program. It was used to produce Figure 2.25.

The second program plots the voltage and current waveforms during main module turn off taking the effect of the parasitic components into account. It was used to plot the theoretical waveforms of Figure 2.28(c).

```
% Program to implement optimal snubber design for experimental turn-off snubber
% T Mouton
% June 1998

clear all;

% System parameters

Vd = 800;                % DC-bus voltage
Iomax = 200              % Peak output current
fs = 10000;              % Converter switching frequency
tb = 5e-6;               % Blanking time
t1max = 10e-6;           % Discharge time
ffundamental = 50;       % Fundamental frequency of output current

% Main IGBT

tfi = 250e-9;            % Current fall time
tti = 500e-9;            % Current tail time
```

```
A = 1/5;                % Tail current ratio

% Snubber diode

trr = 80e-9;            % Reverse recovery time
VDr = 1.2;              % On-state voltage
RDr = 22e-3;            % On-state resistance

% Snubber capacitor

kRC = 3.42e-12;         % ESR coefficient

% Auxiliary IGBT

tfv = 17e-9;            % Voltage fall time
ttv = 40e-9;            % Voltage tail time
B = 0.06;               % Tail voltage ratio
Rsa = 0.017;            % On-state resistance
Vsa = 1.5;              % On-state voltage
Irmax = 75;             % Maximum peak current through auxiliary switch

% Auxiliary diode

Rda = 8.3e-3;           % On-state resistance
Vda = 2;                % On-state voltage

% Resonant inductor

Wcore = 87.6e-6;        % Core loss per cycle
phipeak = 41.1e-6;      % Peak flux
Awe = 8.5e-6;           % Effective core area
Dturn = 18e-3;          % Average turn diameter
sigma = 5.8e7;          % Resistivity of copper

% Initialize variables

Crmin = Iomax*tfi/(10*Vd);      % Minimum value of Cr
Crmax = 2*t1max*Irmax/(pi*Vd);  % Maximum value of Cr
```

```
Wmin = inf;                          % Total loss
d=1;                                 % Counter


% Simulation

for Cr = Crmin:(Crmax-Crmin)/30:Crmax;          % Step range of values of Cr
   c = 1;                                       % Counter
   Lrmin = Vd^2/4*Cr/(Irmax^2);                 % Minimum value of Lr
   Lrmax = t1max^2/(pi^2*Cr);                   % Maximum value of Lr
   for Lr = Lrmin:(Lrmax-Lrmin)/30:Lrmax;       % Step range of values of Lr
      RCr = kRC/Cr;                             % Calculate RCr

      % Initialize sum of loss components over 1/4 cycle
      Woffcycle = 0;
      WDrpcycle = 0;
      WCrpcycle = 0;
      Wsacondcycle = 0;
      Wdacondcycle = 0;
      WLrcycle = 0;
      WCrcycle = 0;
      Wsaswitchcycle = 0;
      Wrrcycle = 0;

      % Determine losses  over 1/4 of a 50 Hz cycle
      for t = 0:1/fs:1/(4*ffundamental);
         Io = Iomax*sin(2*pi*ffundamental*t);
         % Main IGBT turn-off cycle

         % Case 1
         if (Io > 2*Vd*Cr/(tfi*(1-A)))
            tvr = sqrt(2*Vd*Cr*tfi/(Io*(1-A)));
            Woff = Io^2/(2*Cr*tfi)*((1-A)*tvr^3/3 - (1-A)^2*tvr^4/(4*tfi))
                   + Vd*Io*(tfi-tvr+(A-1)*(tfi^2-tvr^2)/(2*tfi)) + Vd*A*Io*tti/2;
            WDrp = VDr*Io*(1-A)*tvr^2/(2*tfi)+RDr*Io^2*(1-A)^2*tvr^3/(3*tfi^2);
            WCrp = RCr*Io^2*(1-A)^2*tvr^3/(3*tfi^2);
         % Case 2
         elseif (Io > Vd*Cr/((1-A)*tfi/2+tti-A/2*tti))
```

```
        tvr = tfi - (1-A)/A*tti + sqrt(((1-A)/A*tti)^2 -
              (1-A)/A*tfi*tti + 2*Cr*Vd*tti/(Io*A));
        Woff = Io^2/(2*Cr)*((1-A)*tfi^2/3-(1-A)^2*tfi^2/4)
               + A*Io^2/Cr*(tfi*(1-A)/2*(tvr-tfi)+(1-A)/2
               *(tvr-tfi)^2+A*(tvr-tfi)^3/(6*tti)
               -tfi*(1-A)/(4*tti)*(tvr-tfi)^2-(1-A)/(3*tti)
               *(tvr-tfi)^3-A/(8*tti^2)*(tvr-tti)^4)
               + Vd*A*Io*(tfi+tti/2-tvr+(tvr-tfi)^2/(2*tti));
        WDrp = VDr*Io*(1-A)*tfi/2+RDr*Io^2*(1-A)^2*tfi/3+VDr*Io*tti/(2*A)
               *((1-A*(1-(tvr-tfi)/tti))^2 - (1-A)^2)
               + RDr*Io^2/(3*A)*tti*((1-A*(1-(tvr-tfi)/tti))^3-(1-A)^3);
        WCrp = RCr*Io^2*(1-A)^2*tfi/3+RCr*Io^2*tti/(3*A)
               *((1-A*(1-((tvr-tfi)/tti)))^3-(1-A)^3);
      % Case 3
else
          tvr = Cr/Io*(Vd-Io*tfi*(1-A)/(2*Cr)-Io*tti/Cr*(1-A/2))+tti+tfi;
          % Check if capacitor will discharge in blaking time
          if (tvr < tb)
            Woff = Io^2*tfi^2/(2*Cr)*((1-A)/3-(1-A)^2/4)
                   + A*Io^2/Cr*(tfi*tti*(1-A)/4+tti^2*(1-A)/6+tti^2*A/24);
            WDrp = VDr*Io*(1-A)*tfi/2+RDr*Io^2*(1-A)^2*tfi/3+VDr*Io*tti/(2*A)
                   *(1-(1-A)^2)+RDr*Io^2*tti/(3*A)*(1-(1-A)^3)
                   + VDr*Io*(tvr-tfi-tti)+RDr*Io^2*(tvr-tfi-tti);
    WCrp = RCr*Io^2*tti/(3*A)*(1-(1-A)^3) + RCr*Io^2*(tvr-tfi-tti);
   else
          % Use data sheet losses
      Woff = 0.04/200*Io;
      WDrp = 0;
      WCrp = 0;
   end;
end;

        % Auxiliary discharging cicuit losses
         if (tvr < tb)       % Check if snubber will discharge capacitor
            Wsacond = pi*Rsa*Vd^2*Cr/8*sqrt(Cr/Lr)+Vsa*Vd*Cr;
            Wdacond = pi*Rda*Vd^2*Cr/8*sqrt(Cr/Lr)+Vda*Vd*Cr;
            WCr = pi*RCr*Vd^2*Cr/8*sqrt(Cr/Lr);
            Wsaswitch = Vd^2*tfv^2/(8*Lr)*((1-B)/3-(1-B)^2/4)
```

```
                    + B*Vd^2/(4*Lr)*(tfv*ttv*(1-B)/4
                    + ttv^2*(1-B)/6 + ttv^2*B/24);
        Wrr = Vd^2*trr^2/(32*Lr);

        % Caluculate inductor copper resistance
        Ipeak = Vd/2*sqrt(Cr/Lr);
        N = Lr*Ipeak/phipeak;
        Acond = Awe/N;
        lcond = N*pi*Dturn;
        RLr = lcond/(sigma*Acond);
        % Calculate Wlr;
        WLr = pi*RLr*Vd^2*Cr/8*sqrt(Cr/Lr)+Wcore;
    else              % If snubber not active, auxiliary losses equals 0
      Wsacond = 0;
      Wdacond = 0;
      WLr = 0;
      WCr = 0;
      Wsaswitch = 0;
      Wrr = 0;
   end;

   % Add losses
   Woffcycle = Woffcycle+Woff;
   WDrpcycle = WDrpcycle+WDrp;
   WCrpcycle = WCrpcycle+WCrp;
   Wsacondcycle = Wsacondcycle+Wsacond;
   Wdacondcycle = Wdacondcycle+Wdacond;
   WLrcycle = WLrcycle+WLr;
   WCrcycle = WCrcycle+WCr;
   Wsaswitchcycle = Wsaswitchcycle+Wsaswitch;
   Wrrcycle = Wrrcycle+Wrr;
end;

% Add components to obtain total converter effective turn-off losses
% Multiply by 4*ffundamental because losses were calculated over 1/4 cycle
% Each IGBT turns off for 1/2 a fundamental cycle

Wtot = (Woffcycle+WDrpcycle+WCrpcycle+Wsacondcycle
```

```
                +Wdacondcycle+WLrcycle+WCrcycle
                +Wsaswitchcycle+Wrrcycle)*4*ffundamental;

        % Store variables for plotting

        Wtotrec(c, d) = Wtot;
        Lrrec(c, d) = Lr;
        Crrec(c, d) = Cr;

        c = c + 1;      % Increment counter

        % Search for minimum value of total effective turn-off losses
        if(Wtot < Wmin)
           Lropt = Lr;
           Cropt = Cr;
           Wmin = Wtot;
         end;
   end;

d = d + 1;              % Increment counter
end;

% Plot data

surf(Lrrec*1e6, Crrec*1e9, Wtotrec);
xlabel('Lr ({\mu}H)');
ylabel('Cr (nF)');
zlabel('Total effective converter turn-off losses (W)');

% Write results
Lropt
Cropt
Wmin
```

```
% Program to simulate effect of parasitic components during turn-off cycle
% T Mouton
% July 1998

clear all;

% System parameters

Vd = 600;                       % DC-bus voltage
Rbp = 1e-3;                     % Positive bus resistance
Rbn = 1e-3;                     % Negative bus resistance
Lbp = 19e-9;                    % Positive bus inductance
Lbn = 19e-9;                    % Negative bus inductance
Lmp = 25e-9;                    % Module stray inductance
Lmn = 25e-9;                    % Module stray inductance
Ls = 72e-9;                     % Snubber parasitic inductance
Cs = 165e-9;                    % Snubber capacitance
Rs = 0.022;                     % Snubber resistance
Io = 100;                       % Output current
tfi = 250e-9;                   % Main module current fall time
tti = 500e-9;                   % Main module current tail time
A = 0.2;                        % Main module tail current ratio
dt = 1e-8;                      % Plotting time step
tend = 2.0e-6;                  % Duration of simulation

% Calculate constants required in the equations

Rt = Rbp+Rbn+Rs;
Rb = Rbn+Rbp;
Lt = Lbp+Lbn+Lmn+Ls;
alpha = -Rt/(2*Lt);
beta = sqrt(4*Lt*Cs-Rt^2*Cs^2)/(2*Lt*Cs);

% Initialize variables

i = 1;                          % Counter
diodenon = 0;                   % 1 if Dn on
```

```
diodeson = 1;                    % 1 if Drp on
case2calc = 0;                   % 1 if case 2 initial conditions calculated
case3calc = 0;                   % 1 if case 3 initial conditions calculated

% Calculate waveforms

for t = 0 : dt : tend;
   % Case 1
   if t >= 0 & t < tfi;
      ic = Io*(1+(A-1)*t/tfi);
      vceideal = Io*t^2*(1-A)/(2*Cs*tfi);
      if diodenon == 0;
         ils = Io*(1-A)*t/tfi;
         vcs = Io*t^2*(1-A)/(2*Cs*tfi);
         vce = vcs + Io*Rs*(1-A)*t/tfi +(Ls+Lmp)*Io*(1-A)/tfi;
         vce1 = vcs + Io*Rs*(1-A)*t/tfi +(Ls)*Io*(1-A)/tfi;
         vdn = Vd - Io*Rbp - vce - Lmp*(1-A)/tfi;
      else
         if diodeson == 1;
            Am = [exp((alpha+j*beta)*t),exp((alpha-j*beta)*t); Cs*(alpha+j*beta)
                *exp((alpha+j*beta)*t), Cs*(alpha-j*beta)*exp((alpha-j*beta)*t)];
            vcsp = Vd-Io*(A-1)/tfi*(Lbp+Lbn+Lmn+Rb*t+Rt*Rb*Cs)-Rb*Io;
            ilsp = Cs*Io*Rb*(1-A)/tfi;
            temp = Am*k + [vcsp; ilsp];
            vcs = temp(1);
            ils = temp(2);
            vce = vcs + Rs*ils + Lmp*Io*(1-A)/tfi + Ls*(ils-ilsprev)/dt;
            vce1 = vcs + Rs*ils + Ls*(ils-ilsprev)/dt;
         else
            vce = Vd - Rbp*ic-Rbn*(ic-Io)-(Lbn+Lbp)*Io*(1-A)/tfi;
            vce1 = vce;
         end;
         ilsprev = ils;
      end;
   end;

   % Case 2
   if t >= tfi & t < tfi+tti;
```

```
   ic = A*Io*(1- (t-tfi)/tti);
   vceideal = Io*tfi*(1-A)/(2*Cs) + Io/Cs*((t-tfi)*(1-A) + A*(t-tfi)^2/(2*tti));
   if diodenon == 0;
      ils = Io*(1-A*(1-(t-tfi)/tti));
      vcs = Io*tfi*(1-A)/(2*Cs) + Io/Cs*((t-tfi)*(1-A) + A*(t-tfi)^2/(2*tti));
      vce = vcs + Io*Rs*(1-A*(1-(t-tfi)/tti))+(Ls+Lmp)*Io*A/tti;
      vce1 = vcs + Io*Rs*(1-A*(1-(t-tfi)/tti))+(Ls)*Io*A/tti;
      vdn = Vd - Io*Rbp - vce - Lmp*A/tti;
   else
      if diodeson == 1;
         Am = [exp((alpha+j*beta)*t),exp((alpha-j*beta)*t); Cs*(alpha+j*beta)
             *exp((alpha+j*beta)*t), Cs*(alpha-j*beta)*exp((alpha-j*beta)*t)];
         vcsp = Vd+Io*A*((Lbp+Lbn+Lmn)/tti-Rb*(t-tti)/tfi+Rt*Rb*Cs/tti);
         ilsp = Cs*Io*Rb/tti;
         if case2calc == 0;
           k = inv(Am)*[vcs-vcsp;ils-ilsp];
           case2calc = 1;
         end;
         temp = Am*k + [vcsp; ilsp];
         vcs = temp(1);
         ils = temp(2);
         vce = vcs + Io*Rs + Lmp*Io*(1-A)/tfi + Ls*(ils-ilsprev)/dt;
         vce1 = vcs + Io*Rs + Ls*(ils-ilsprev)/dt;
         ilsprev = ils;
      else
         vce = Vd - Rbp*ic-Rbn*(ic-Io)-(Lbn+Lbp)*Io*A*(-1)/tti;
         vce1 = vce;
      end;
   end;
end;

% Case 3
if t >= (tfi+tti);
   ic = 0;
   vceideal = Io*tfi*(1-A)/(2*Cs) + Io/Cs*(tti*(1-A) + A*tti/2)+Io/Cs*(t-tfi-tti);
   if diodenon == 0;
      vcs = Io*tfi*(1-A)/(2*Cs) + Io/Cs*(tti*(1-A) + A*tti/2)+Io/Cs*(t-tfi-tti);
      vce = vcs+Rs*Io;
```

```
      vce1 = vce;
      ic = 0;
      ils = Io;
      vdn = Vd - Io*Rbp - vce;
   else
      if diodeson == 1;
        Am = [exp((alpha+j*beta)*t),exp((alpha-j*beta)*t); Cs*(alpha+j*beta)
             *exp((alpha+j*beta)*t), Cs*(alpha-j*beta)*exp((alpha-j*beta)*t)];
       vcsp = Vd;
        ilsp = 0;
        if case3calc == 0;
        k = inv(Am)*[vcs-vcsp;ils-ilsp];
        case3calc = 1;
      end;
        temp = Am*k + [vcsp; ilsp];
        vcs = temp(1);
        ils = temp(2);
        vce = vcs + Rs*ils + Ls*(ils-ilsprev)/dt;
        vce1 = vce;
        ilsprev = ils;
      else
         vce = Vd - Rbp*ic-Rbn*(-Io);
         vce1 = vce;
      end;
   end;
end;

% Test for Dn turning on and calculate constants
if (vdn <= 0) & (diodenon == 0);
   diodenon = 1;
   Am = [exp((alpha+j*beta)*t),exp((alpha-j*beta)*t); Cs*(alpha+j*beta)
        *exp((alpha+j*beta)*t), Cs*(alpha-j*beta)*exp((alpha-j*beta)*t)];
   if t < tfi;
      vcsp = Vd-Io*(A-1)/tfi*(Lbp+Lbn+Lmn+Rb*t+Rt*Rb*Cs)-Rb*Io;
      ilsp = Cs*Io*Rb*(1-A)/tfi;
   end;
   if (t >= tfi & t < tfi+tti);
      vcsp = Vd+Io*A*((Lbp+Lbn+Lmn)/tti-Rb*(t-tti)/tfi+Rt*Rb*Cs/tti);
```

```
            ilsp = Cs*Io*Rb/tti;
            case2calc = 1;
        end;
        if (t >= tfi+tti);
            vcsp = Vd;
            ilsp = 0;
            case3calc = 1;
        end;
        k = inv(Am)*[vcs-vcsp;ils-ilsp];
        vcsprev = vcs;
    end;
    if ils < 0;
        diodeson = 0;
    end;

    % Store variables

    icrec(i) = ic;
    ilsrec(i) = ils;
    ilsprev = ils;
    trec(i) = t;
    vce1rec(i) = vce1;
    vcsrec(i) = vcs;
    vdnrec(i) = vdn;

    i = i + 1;    % Increment counter
end;

% Plot results

plot(trec*1e6, icrec, trec*1e6, vce1rec);
xlabel('Time ({\mu}s)', 'FontSize', 14);
ylabel('Top main IGBT v_{ce1} (V)', 'FontSize', 14)'
```

Appendix B

Series-stacked converter Matlab programs

In this appendix Matlab programs used to simulate the behavior of the two-level series-stacked converter are presented. The first program calculates the homogenous solution and was used to produce the results of the example on p. 118 is presented. The second program calculates the steady-state solution and was used to produce the results on p. 125. All the other simulations of Chapter 3 were produced by applying the same techniques as presented in these programs.

```
% M-file to simulate series-stacked converter under interleaved switching
% Homogenous part
% T Mouton
% June 1999

clear all;

% System parameters

Cd = 30e-3;             % Bus capacitance
L = 300e-6;             % Filter inductance
C = 200e-6;             % Filter capacitance
R = 0.01;               % Parasitic resistance
Rl = 1;                 % Load resistance
Rb = 0.001;             % Bus resistance
fs = 1000;              % Switching frequency
fr = 50;                % Reference frequency
dt = 1e-7;              % Time step
```

```
tend = 0.5;              % Stop time

% Set initial conditions

id0 = 0;
vd0 = 50;
it0 = 0;
vt0 = 0;
v00 = 0;

x0 = [id0; vd0; it0; vt0; v00];

% Calculate parameters

Ts = 1/fs;
Tr = 1/fr;
wr = 2*pi*fr;

% Initialize total energy dissipated in different resistances

ERd = 0;
ERt = 0;
ERl = 0;
ERb = 0;

% Generate switching functions

tcycle = 0;
k = 1;

for t = 0:dt:Tr;
   % Reference signal
   fr = 0.8*cos(wr*t);

   % Carrier signal for converter 1
   if tcycle <= Ts/4;
      fc1 = 4/Ts*tcycle;
   elseif tcycle < 3*Ts/4;
```

```
      fc1 = 1-4/Ts*(tcycle-Ts/4);
   else
      fc1 = -1+4/Ts*(tcycle-3*Ts/4);
   end;
   % Carrier signal for converter 2
   if tcycle <= Ts/2;
      fc2 = -1+4/Ts*tcycle;
   else
      fc2 = 1-4/Ts*(tcycle-Ts/2);
   end;
% Incerement tcycle
   if tcycle >= Ts;
      tcycle = 0;
   else
      tcycle = tcycle+dt;
   end;
   % Calculate s1 and s2
   if (fc1 <= fr & fc1 >= -fr)
      s1 = 1;
   elseif (fc1 <= -fr & fc1 >= fr)
      s1 = -1;
   else
      s1 = 0;
   end;
   if (fc2 <= fr & fc2 >= -fr)
      s2 = 1;
   elseif (fc2 <= -fr & fc2 >= fr)
      s2 = -1;
   else
      s2 = 0;
   end;

   % Calculate st and sd and store values
   st(k) = (s1+s2)/2;
   sd(k) = (s1-s2)/2;
   k=k+1;
end;
```

```
% Calculate Phi
k = 1;
Phiprev = [1, 0, 0, 0, 0; 0, 1, 0, 0, 0;
          0, 0, 1, 0, 0; 0, 0, 0, 1, 0; 0, 0, 0, 0, 1];

for t = 0:dt:Tr;
   A = [-R/L, st(k)/L, 0, sd(k)/L, 0; -st(k)/Cd, 0,
       -sd(k)/Cd, 0, 0; 0, sd(k)/L, -R/L, st(k)/L, -2/L;
       -sd(k)/Cd, 0, -st(k)/Cd, -2/(Rb*Cd), 0;
       0, 0, 1/(2*C), 0, -1/(2*Rl*C)];
   Phinew = expm(A*dt)*Phiprev;
   Phi(:,:,k) = Phiprev;
   Phiprev = Phinew;
   k = k + 1;
end;


% Calculate homogonous solution
k = 1;
l=1;
len = length(Phi);
step = 10;
for t = 0:step*dt:tend;
   x = Phi(:,:,k)*x0;
   if k < len;
      k=k+step;
   else;
      k=1;
      x0 = x;
   end;
   % Calculate energy dissipated in different resistors
   ERd = ERd + R*x(1).^2*dt*step;
   ERt = ERt + R*x(3).^2*dt*step;
   ERl = ERl + (x(5).^2)*2/Rl*dt*step;
   ERb = ERb + x(4).^2/(Rb/2)*dt*step;
   % Store values
   xrec(:,l)=x;
   trec(l) = t;
```

```
   ERdrec(l) = ERd;
   ERtrec(l) = ERt;
ERlrec(l) = ERl;
   ERbrec(l) = ERb;
   l=l+1;
end;

% Calculate time constants

M = Phi(:,:,len);
E = eig(M);
tauvect = -Tr./(real(log(E)));
tau = max(tauvect)

% Plot Results

plot(trec, xrec(1,:), trec, sqrt(Cd/L)*vd0*exp(-trec/tau),
     trec, -sqrt(Cd/L)*vd0*exp(-trec/tau));
ylabel('i_d (A)', 'FontSize', 16);
xlabel('Time (s)', 'FontSize', 16);

figure;
plot(trec, xrec(2,:), trec, vd0*exp(-trec/tau), trec, -vd0*exp(-trec/tau));
ylabel('v_d (V)', 'FontSize', 16);
xlabel('Time (s)', 'FontSize', 16);

figure;
plot(trec, xrec(3,:));
ylabel('i_t (A)', 'FontSize', 16);
xlabel('Time (s)', 'FontSize', 16);

figure;
plot(trec, xrec(4,:));
ylabel('v_t (V)', 'FontSize', 16);
xlabel('Time (s)', 'FontSize', 16);

figure;
plot(trec, xrec(5,:));
```

```
ylabel('v_o (V)', 'FontSize', 16);
xlabel('Time (s)', 'FontSize', 16);

figure;
plot(trec, xrec(4,:)./(Rb/2));
ylabel('i_b (A)', 'FontSize', 16);
xlabel('Time (s)', 'FontSize', 16);

figure;
plot(trec, ERdrec, trec, ERtrec, trec, ERlrec, trec, ERbrec);
ylabel('Total energy dissipated (J)', 'FontSize', 16);
xlabel('Time (s)', 'FontSize', 16);
```

```
% M-file to simulate series-stacked converter under interleaved switching
% Steady state solution
% T Mouton
% June 1999

clear all;

% System parameters

Cd = 30e-3;              % Bus capacitance
L = 300e-6;              % Filter inductance
C = 200e-6;              % Filter capacitance
R = 0.01;                % Parasitic resistance
Rl = 1;                  % Load resistance
Rb = 0.001;              % Bus resistance
Vb = 1600;               % Dc-bus voltage

fs = 1000;               % Switching frequency
fr = 50;                 % Reference frequency
dt = 1e-9;               % Time step

% Initial conditions

id0 = 0;
vd0 = 0;
it0 = 0;
vt0 = 0;
v00 = 0;

x0 = [id0; vd0; it0; vt0; v00];

step = 20;

% Calculate parameters

Ts = 1/fs;
Tr = 1/fr;
wr = 2*pi*fr;
```

```
% Generate switching functions

tcycle = 0;
k = 1;

Imat = [1, 0, 0, 0, 0; 0, 1, 0, 0, 0;
        0, 0, 1, 0, 0; 0, 0, 0, 1, 0; 0, 0, 0, 0, 1];
Phi = Imat;
x = x0;

for t = 0:dt:Tr;
   % Reference signal
   fr = 0.8*cos(wr*t);

   % Carrier signal for converter 1
   if tcycle <= Ts/4;
      fc1 = 4/Ts*tcycle;
   elseif tcycle < 3*Ts/4;
      fc1 = 1-4/Ts*(tcycle-Ts/4);
   else
      fc1 = -1+4/Ts*(tcycle-3*Ts/4);
   end;
   % Carrier signal for converter 2
   if tcycle <= Ts/2;
      fc2 = -1+4/Ts*tcycle;
   else
      fc2 = 1-4/Ts*(tcycle-Ts/2);
   end;
% Incerement tcycle
   if tcycle >= Ts;
      tcycle = 0;
   else
      tcycle = tcycle+dt;
   end;
   % Calculate s1 and s2
   if (fc1 <= fr & fc1 >= -fr)
      s1 = 1;
```

```
    elseif (fc1 <= -fr & fc1 >= fr)
       s1 = -1;
    else
       s1 = 0;
    end;
    if (fc2 <= fr & fc2 >= -fr)
       s2 = 1;
    elseif (fc2 <= -fr & fc2 >= fr)
       s2 = -1;
    else
       s2 = 0;
    end;
% Calculate st and sd and store values
    st = (s1+s2)/2;
    sd = (s1-s2)/2;

    % Calculate M
    A = [-R/L, st/L, 0, sd/L, 0; -st/Cd, 0, -sd/Cd, 0, 0;
        0, sd/L, -R/L, st/L, -2/L; -sd/Cd, 0, -st/Cd,
        -2/(Rb*Cd), 0; 0, 0, 1/(2*C), 0, -1/(2*Rl*C)];
    Phi = expm(A*dt)*Phi;

    % Integrate system numerically
    vs = 300*cos(wr*t);
    B = [0; 0; 0; 2*Vb/(Rb*Cd); -vs/(2*Rl*C)];
    x = x+(A*x+B)*dt;

end;

M = Phi;
x1 = inv(Imat-M)*x
tcycle = 0;

% Integrate system numerically again with x1 as initial condition
k = 1;
l=1;
x = x1;
for t = 0:dt:Tr;
```

```
% Reference signal
fr = 0.8*cos(wr*t);
% Carrier signal for converter 1
if tcycle <= Ts/4;
   fc1 = 4/Ts*tcycle;
elseif tcycle < 3*Ts/4;
   fc1 = 1-4/Ts*(tcycle-Ts/4);
else
   fc1 = -1+4/Ts*(tcycle-3*Ts/4);
end;
% Carrier signal for converter 2
if tcycle <= Ts/2;
   fc2 = -1+4/Ts*tcycle;
else
   fc2 = 1-4/Ts*(tcycle-Ts/2);
end;
% Incerement tcycle
if tcycle >= Ts;
   tcycle = 0;
else
   tcycle = tcycle+dt;
end;
% Calculate s1 and s2
if (fc1 <= fr & fc1 >= -fr)
   s1 = 1;
elseif (fc1 <= -fr & fc1 >= fr)
   s1 = -1;
else
   s1 = 0;
end;
if (fc2 <= fr & fc2 >= -fr)
   s2 = 1;
elseif (fc2 <= -fr & fc2 >= fr)
   s2 = -1;
else
   s2 = 0;
end;
% Calculate st and sd and store values
```

```
    st = (s1+s2)/2;
    sd = (s1-s2)/2;

    vs = 300*cos(wr*t);
    B = [0; 0; 0; 2*Vb/(Rb*Cd); -vs/(2*Rl*C)];
    A = [-R/L, st/L, 0, sd/L, 0;
        -st/Cd, 0, -sd/Cd, 0, 0;
        0, sd/L, -R/L, st/L, -2/L;
        -sd/Cd, 0, -st/Cd, -2/(Rb*Cd), 0;
        0, 0, 1/(2*C), 0, -1/(2*Rl*C)];
    x = x+(A*x+B)*dt;
    if mod(k, 20) == 0;
    xrec(:,l) = x;
   trec(l) = t;
    l=l+1;
    end;
    k=k+1;
end;

% Plot results

plot(trec, xrec(1,:));
ylabel('i_d (A)', 'FontSize', 16);
xlabel('Time (s)', 'FontSize', 16);

figure;
plot(trec, xrec(2,:));
ylabel('v_d (V)', 'FontSize', 16);
xlabel('Time (s)', 'FontSize', 16);

figure;
plot(trec, xrec(3,:));
ylabel('i_t (A)', 'FontSize', 16);
xlabel('Time (s)', 'FontSize', 16);

figure;
plot(trec, xrec(4,:));
ylabel('v_t (V)', 'FontSize', 16);
```

```
xlabel('Time (s)', 'FontSize', 16);

figure;
plot(trec, xrec(5,:));
ylabel('v_o (V)', 'FontSize', 16);
xlabel('Time (s)', 'FontSize', 16);

figure;
plot(trec, (Vb-xrec(4,:))*2/Rb);
ylabel('i_b (A)', 'FontSize', 16);
xlabel('Time (s)', 'FontSize', 16);
```