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**An Autonomous,
Omnidirectional, Digital,
Borehole Imaging System**

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UNIVERSITY

Timothy G. Sindle

Study Leaders: Prof J.H. Cloete and Prof K.D. Palmer

Thesis submitted in partial fulfilment of the requirements for the degree of Masters of Engineering in the department Electrical and Electronic Engineering at the University of Stellenbosch.

Declaration

I, the undersigned, hereby declare that the work contained in this thesis is my own original work, except where indicated. It has not been submitted before, in its entirety or in part, for any degree or examination at any other University.

Timothy Grant Sindle

Abstract

This thesis documents the research, design, implementation and successful testing of a prototype camera probe to survey the inside of hard rock boreholes. Rock core images are intended to aid mine geologists in recording the borehole rock layers. The system consists of a wide-angle fisheye lens mounted onto a CMOS digital image sensor. The image data is read in and processed by an FPGA, then stored on a removable SD flash memory card. All of the aforementioned components are mounted inside a watertight Perspex tube. Application specific PC software is used to process the data to form strip images of the borehole wall. Using mathematical correlation, these images are stitched together into a virtual core that is a flattened representation of the rock inside the borehole. The probe contains its own power and light source which enables it to be deployed easily with no external wires needed for operation. The storage capacity, image quality, and lighting design can be improved in future design revisions.

Opsomming

Die inhoud van hierdie tesis behels die navorsing, ontwerp, implementering, en suksesvolle toetsing van 'n prototipe kameraprobe wat dit moontlik maak om die binnewand van boorgate in harde rots te besigtig. Beelde van die rotskern vergemaklik die taak van myngeoloë wat die rotslae, waardeur die boorgat strek, moet opteken. Die stelsel behels 'n wyehoek lens wat op 'n CMOS digitale sensor gemonteer is. Die data gewerf vir die vorming van die beeld word deur 'n FPGA ingelees en verwerk, waarna dit op 'n verwyderbare SD flits geheuekaart gestoor word. Die bogenoemde komponente word alles binne 'n waterdigte Perspexbuis monteer. Gebruikerspesifieke sagteware vir persoonlik rekenaars word gebruik om die data te verwerk en sodoende strookbeelde van die binnewand van die boorgat te vorm. Met gebruik van wiskundige korrelasie word hierdie beelde aan mekaar gelas om 'n virtuele kern te vorm, wat 'n voorstelling is van die rots binne die boorgat. Die probe bevat self krag en ligbronne, wat toelaat dat dit maklik bruikbaar is sonder enige eksterne bedrading. Toekomstige hersienings van die ontwerp sal verbeterde data geheue, beeldgehalte en beligting kan bewerkstellig.

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Abbreviations

ADC	Analogue to digital converter
BRAM	Block random accesses memory
CID	Card identification register
CLB	Configurable logic block
CMOS	Complementary metal oxide semiconductor
CRC	Cyclical redundancy check
DLL	Delay-locked loop (FPGA)
DLL	Dynamic link library (USB PC Code)
DOS	Disk operating system
DSP	Digital signal processor
FAT32	32-bit File allocation table
FIFO	First in first out
FPGA	Field programmable gate array
FPS	Frames per second
I ² C	Inter-integrated circuit
IO	Input output
IOB	Input output block
JTAG	Joint test action group
LC	Logic cell
LUT	Look up table
mcd	Millicandela
MMC	Multimedia card
PC	Personal computer
PCB	Printed circuit board
PGA	Programmable gain array
PROM	Programmable read only memory
RAM	Random access memory
RGB	Red, green, blue
SD	Secure digital
USB	Universal serial bus

Table of Contents

Declaration	II
Abstract	III
Opsomming	IV
Acknowledgements	V
Abbreviations	VI
Table of Contents	VII
Table of Figures	IX
Table of Equations	XI
Table of Tables	XI
An Early Omnidirectional Imaging System	XII
Chapter 1 Introduction	1
1.1 Background Study.....	1
1.2 Initial System Specification	4
1.3 Design Overview.....	5
1.4 Thesis Overview.....	5
Chapter 2 System Level Design	6
2.1 Existing Systems and Related Patents.....	6
2.1.1 Existing Systems	6
2.1.2 Related Patents	8
2.2 System Innovations	9
2.3 Complete System Description.....	10
2.3.1 Omnidirectional Optics System	11
2.3.2 Camera and Lighting.....	11
2.3.3 FPGA Data Processing.....	12
2.3.4 Flash Memory Storage	12
Chapter 3 Hardware Design	13
3.1 Hardware Overview	13
3.2 Image Sensor.....	13
3.2.1 Image Sensor Requirements.....	13
3.2.2 Image Sensor Technology.....	16
3.2.3 CMOS Image Sensor.....	17
3.3 Processing Power	19
3.3.1 Processing Requirements	19
3.3.2 FPGA Technology	20
3.3.3 Xilinx Virtex FPGA	21
3.4 Flash Memory	23
3.4.1 Memory Storage Requirements.....	23
3.4.2 Flash Technology	24
3.4.3 Secure Digital Card.....	26
3.5 USB Communication	27
3.6 LED Lighting Circuitry.....	29

Chapter 4	Optical Design.....	30
4.1	Optics Overview.....	30
4.1.1	Spherical, Hyperboloidal, and Paraboloidal Mirrors	32
4.1.2	Conical Mirror.....	33
4.2	Conical Mirror Optical Setup.....	34
4.3	Fisheye Lens.....	41
Chapter 5	Firmware Design	43
5.1	Firmware Overview	43
5.2	Camera Controller.....	45
5.2.1	Initialize Process	45
5.2.2	Read Data Process.....	48
5.3	SD Flash Controller.....	49
5.3.1	Write Block Process.....	52
5.4	FIFO Memory Block.....	55
5.5	Timer and Clock Generation.....	56
Chapter 6	Image Processing.....	58
6.1	Bayer's Array to RGB, Methods and Implementation.....	58
6.2	Polar to Cartesian Conversion.....	60
6.3	Correlation Based Merge and Distance Calculation	63
Chapter 7	Testing and Results	65
7.1	Prototype Packaging.....	65
7.2	Lighting Modifications.....	66
7.3	CMOS Sensor Gain Variation Test.....	67
7.4	Test Borehole Results	71
7.4.1	Conical Mirror.....	71
7.4.2	Fisheye Lens.....	72
7.5	Resolution Test Chart.....	74
7.6	Water Borehole Test	75
7.7	Rock Borehole Results.....	78
7.8	Power Usage.....	84
7.9	System Cost.....	84
Chapter 8	Recommendations and Conclusions	85
8.1	Recommendations	85
8.1.1	Hardware	85
8.1.2	Optics	86
8.1.3	Firmware	87
8.1.4	Image Processing Software	89
8.1.5	Packaging	89
8.2	Future Developments	90
8.2.1	Real-Time Test Mode	90
8.2.2	Wireless Downloading.....	90
8.2.3	Linking with Orientation Sensor.....	90
8.3	System Specification.....	91
8.4	Conclusion.....	92
Chapter 9	References	93

Table of Figures

Figure 1-1 Borehole drill rig and operator [1].	1
Figure 1-2 A core yard at Finsch diamond mine.	2
Figure 1-3 Intended process for using this project.	3
Figure 1-4 Broad system design.	5
Figure 2-1 Raax BIPS (left) and ALT setup (right).	7
Figure 2-2 Annotated picture of RockEye probe.	10
Figure 2-3 Schematic elements of RockEye system.	11
Figure 3-1 CMOS sensor showing desired annular region in grey.	14
Figure 3-2 Illustration of the workings of a rolling shutter.	15
Figure 3-3 A picture of a moving bus taken with a rolling shutter CMOS sensor [7].	15
Figure 3-4 Camera board with Micron MT9V403 sensor front, back unpopulated. ...	18
Figure 3-5 Micron MT9V403 frequency response [8].	18
Figure 3-6 Test board, FPGA and PROM highlighted.	20
Figure 3-7 Virtex architecture [9].	21
Figure 3-8 Two slice vertex CLB [9].	22
Figure 3-9 SanDisk Ultra II SD flash card.	25
Figure 3-10 Secure Digital flash card inner workings [10].	26
Figure 3-11 USB module including FTDI245BM microchip [11].	28
Figure 3-12 First picture from the camera, downloaded through USB port.	28
Figure 3-13 LED driver circuit.	29
Figure 4-1 General optics setup.	31
Figure 4-2 Mirror field of view, image from [14].	32
Figure 4-3 Cone mirror setup as suggested by Lin and Bajcsy [15].	34
Figure 4-4 Gaussian simple lens setup.	35
Figure 4-5 Test mirrors (14, 10, 5 mm) and clear mounting tube.	36
Figure 4-6 Conical mirror test setup.	37
Figure 4-7 Concentric or radial lines in focus.	37
Figure 4-8 Images in the concentric and radial focal planes, modified from [12].	39
Figure 4-9 Fisheye lens.	41
Figure 4-10 Fisheye lens internal optics [19].	42
Figure 5-1 FPGA internal process overview showing internal modules.	43
Figure 5-2 Firmware dataflow.	44
Figure 5-3 Camera module processes.	45
Figure 5-4 Exposure setting control loop.	47
Figure 5-5 Step response for exposure control.	47
Figure 5-6 Read data process flow.	48
Figure 5-7 Frame and row synchronisation waveforms [8].	49
Figure 5-8 SD card module, initialize process.	51
Figure 5-9 Block data packet format [10].	52
Figure 5-10 CRC 16-bit shift register [10].	53
Figure 5-11 Simulink CRC generator simulation.	53
Figure 5-12 Write block process.	54
Figure 5-13 FIFO memory buffer address decoding.	55
Figure 5-14 System clock and double rate clock.	56
Figure 5-15 Clock generation.	57
Figure 6-1 Pixel colour filters, image modified from [21].	58
Figure 6-2 Bayer's pattern.	59
Figure 6-3 Interpolation implementation example.	59

Figure 6-4 Two methods of unwrapping the annular ring.	61
Figure 6-5 Sub-pixel anti-aliasing.....	62
Figure 6-6 Effect of anti-aliasing on unwrapped test image.	62
Figure 6-7 Example of the correlation process.	64
Figure 7-1 Packaged probe.....	65
Figure 7-2 Lighting evolutions (current setup shown on the right).	66
Figure 7-3 Image sensor analogue signal path [8].	67
Figure 7-4 Graph showing variation of exposure time versus gain.	68
Figure 7-5 Graph showing the change in SNR with gain.	69
Figure 7-6 Noise versus gain pictures.....	70
Figure 7-7 Conic mirror in test borehole using 8 mm lens.	71
Figure 7-8 Picture of the test borehole grid pattern using fisheye lens.....	72
Figure 7-9 Unwrapped test grid.	73
Figure 7-10 Relationship between pixel position and borehole distance.....	73
Figure 7-11 Geometrically correct unwrapped test grid.	74
Figure 7-12 Resolution test chart image.	74
Figure 7-13 Water borehole test image.	75
Figure 7-14 Dry test borehole.	76
Figure 7-15 Water filled test borehole.	76
Figure 7-16 Optics in air and water.....	77
Figure 7-17 Granite block with holes of 113, 76, 58, 50, 40 mm diameter.	78
Figure 7-18 Inside of tombstone picture.	79
Figure 7-19 Unwrapped section of frame 1.	79
Figure 7-20 Unwrapped section of frame 2.	79
Figure 7-21 Correlation of one row from frame 2 with all rows from frame 1.	80
Figure 7-22 Correlating every row in frame 1 with every row in frame 2.....	81
Figure 7-23 Pixel offset between frames.	82
Figure 7-24 Virtual core.....	83

Table of Equations

Equation 4-1 Gaussian thin lens formula.....	35
Equation 4-2 Focal distance formula [17].....	40
Equation 5-1 Row time formula.....	46
Equation 5-2 Frame time formula.....	46
Equation 5-3 16-bit CRC generator polynomial.....	52
Equation 6-1 Rectangular to polar transformation.....	60
Equation 6-2 Polar to rectangular transformation.....	61
Equation 6-3 Correlation formula used in MATLAB.....	63
Equation 7-1 Signal to noise ratio formula.....	68
Equation 7-2 Snell's Law [23].....	77

Table of Tables

Table 2-1 Existing optical borehole imaging systems.....	6
Table 3-1 Flash card comparisons.....	25
Table 3-2 Data rates of various communications protocols.....	27
Table 5-1 Camera register setup values.....	46
Table 5-2 Clock frequencies for different modules.....	57
Table 7-1 Cost estimate for critical components.....	84
Table 8-1 Final system specification.....	91

An Early Omnidirectional Imaging System



“Hand with reflecting Sphere”, 1935 M.C. Escher

"The picture shows a spherical mirror, resting on a left hand. But as a print is the reverse of the original drawing on stone, it was my right hand that you see depicted. (Being left-handed, I needed my left hand to make the drawing.) Such a globe reflection collects almost one's whole surroundings in one disk-shaped image. The whole room, four walls, the floor, and the ceiling, everything, albeit distorted, is compressed into that one small circle. Your own head, or more exactly the point between your eyes, is the absolute center. No matter how you turn or twist yourself, you can't get out of that central point. You are immovably the focus, the unshakable core, of your world." - M. C. Escher

Chapter 1 Introduction

This chapter begins with a background study that leads to the formulation of this project idea and includes the initial system specification.

1.1 Background Study

The mining industry is one of South Africa's most important economic activities contributing around 6.5% to the national gross domestic product. This 52 billion rand industry is kept running by numerous mines spread around the country, excavating South Africa's wealth of mineral resources. Before excavation can begin, boreholes are drilled to prospect the rock and determine the underlying strata that the mine will be entering into.

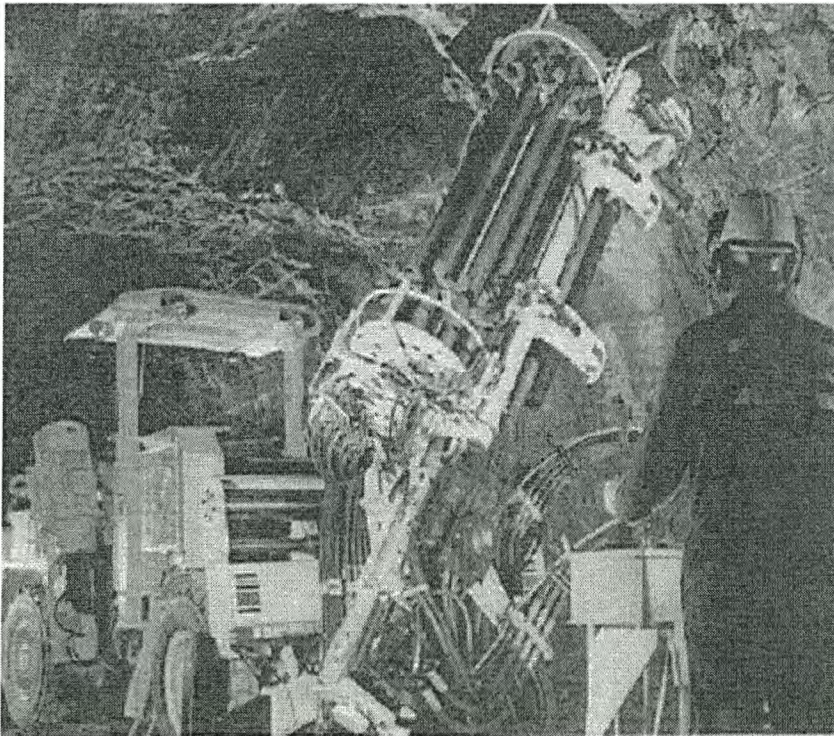


Figure 1-1 Borehole drill rig and operator [1].

Most exploration hard rock boreholes are drilled using diamond tipped drill bits that flush out a circular rock core. The often fractured core samples are collected and stacked in order for later examination by the mine geologist. However, these samples may be stacked incorrectly in the core trays, inaccurately logged against distance, or simply lost. If the cores reach the surface in good condition, the geologist may not have the time to visit the core yard and go through the laborious task of documenting it. In 2003 Anglo Platinum alone drilled 630 km of boreholes, at an average cost of R200 – R1000 per meter. This represents an approximate investment of R200 million – and this for only one of the many mining companies in SA.

The idea behind this project is to design an electronic borehole imager system that will record pictures of the entire borehole wall. The result should be an image of a virtual core, accurately logged against the distance into the borehole, which the geologist and mine planners can peruse back in their office. This will greatly increase the return on investment for the mines for every metre of borehole drilled.



Figure 1-2 A core yard at Finsch diamond mine.

There are existing borehole camera systems that are not widely used – mainly due to their high cost and complexity. They need skilled operators and a setup consisting of screens, computers, winches, optical fibres, and shaft encoders.

This project was designed to work in conjunction with a MSc. Eng. project currently being completed by Stefan van der Walt. His project aims to design an automatic rock classifier based on wavelet pattern recognition technology. It is intended for this design to produce the images that are then processed to form a virtual core. This image is then automatically interpreted as far as is possible before being passed on to the mine geologist who checks the results and uses the information for future mine planning. These steps are shown in Figure 1-3.

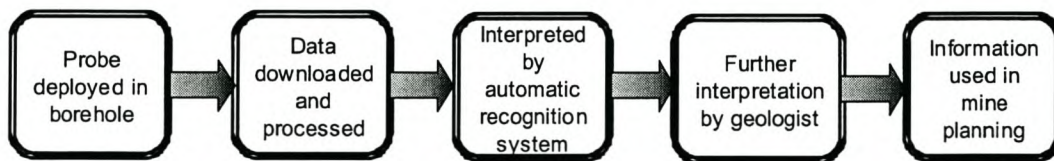


Figure 1-3 Intended process for using this project.

1.2 Initial System Specification

From the end-product described in the previous section, an initial system specification was drawn up. The aim of this project is to produce an imaging system, which is easy to deploy by unskilled miners, to capture visual pictures of the entire wall of the inside of hard rock boreholes. The specifications are:

- Capable of taking high resolution colour pictures.
- Should be able to discern features of width 0.5 mm in a 48 – 75 mm borehole.
- Give a full 360° side-on view of the borehole wall.
- Be able to focus on the 48 mm (and wider) diameter of the borehole wall.
- Camera frame rate should not put too many constraints on deployment speed.
- Store all images onboard on some form of memory.
- Autonomous operation (no attachment wires needed).
- Have enough battery capacity to complete a full survey¹.
- Illuminate the borehole wall.
- Attempt to design for wireless (Bluetooth) download.
- Download data to a PC or handheld device at a reasonably fast rate.
- Work and fit into the physical constraints of a 48 mm diameter borehole.
- Compact design lengthwise.
- Work in air and water filled boreholes.

¹ Borehole radar surveys typically consist of logging a 150-200 m borehole takes approximately 40min. Average deployment rate 0.1 m/sec.

1.3 Design Overview

Using the problem statement, the previous specifications, and many hours of research, a system was designed using the latest available technology. A prototype named the RockEye was built to test the concept. It includes optics, a camera, a processing unit, and a storage medium as shown in Figure 1-4. Post processing software was also developed to present the images in a visually useful format. The RockEye system aims to be the first borehole camera system to save all data onboard and allow complete autonomous operation. Hopefully this will revolutionise the use of borehole cameras in the mining industry.

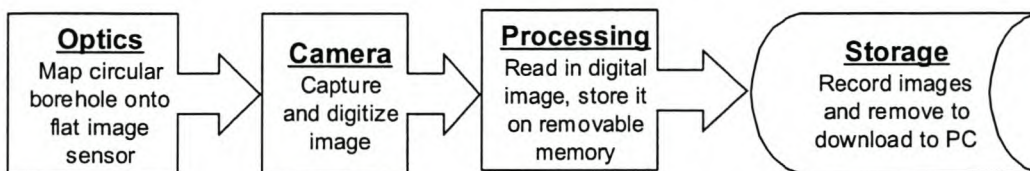


Figure 1-4 Broad system design.

1.4 Thesis Overview

The rest of this thesis details the research, design, implementation and testing of a digital borehole camera. Chapter 2 details the system as a whole - with the following chapters exploring each part of the system in detail. Hardware is discussed in Chapter 3, optics in Chapter 4, firmware in Chapter 5 and image processing in Chapter 6. Chapter 7 shows testing and results before recommendations and conclusions are made in Chapter 8. Chapters 2, 3 and 4 begin with a literature study of available technology to fulfil the specific system needs, then go on to justify the choices made and document the design.

Chapter 2 System Level Design

This chapter initially looks at the existing commercially available borehole camera systems and related patents. The following Section 2.2, describes how this design differs from previous systems. Section 2.3 details the complete design and functioning of this unique device.

2.1 Existing Systems and Related Patents

2.1.1 Existing Systems

There are a number of available borehole imagers that form a good starting point for designing this system. Some of the main market players; the Japanese company Raax; Advanced Logic Technology (ALT) from Luxembourg and Robertson Geologging (RG) originally based in the UK. The main specifications, where available, for the probes from these companies are shown in Table 2-1.

	RAAX BIPS ³	RG OPTV ²	ALT OBI 40 ⁴
Diameter	50 mm (42/32 option)	50 mm	40 mm
Length	1 m	1.43 m	1.7 m
Weight			7 kg
Maximum Depth	500 m (50 bar)	1500 m (150 bar)	2000 m (200 bar)
Max Temperature	45°C		50°C
Logging Speed	0.9 m/min	1 to 2.5 m/min	Variable depending on resolution
Sensor Type	CCD camera	CCD camera 768x494	CCD camera
Sensor Azimuth Resolution	360 or 720 pixels / 360°	720 pixels / 360°	720 pixels / 360°
Sensor Vertical Resolution	0.25 mm	1 / 2 mm	Up to 0.5 mm
Optics	Fisheye / rotating Mirror / 45 degree cone mirror	Hyperbolic mirror	Polycarbonate conic prism
Price			US \$ 25 000

Table 2-1 Existing optical borehole imaging systems.

² <http://www.geologging.com>

However, all of these systems are modified TV cameras housed in protective tubes attached to long cables. The cable normally supplies power and delivers the image signal to the surface where it is attached to a computer or television video recorder combination. In addition to the probe the entire system setup for these systems can comprise of: a length of fibre optic or coaxial cable including up to 7 wires; a shaft encoder to log the length of cable entered into the hole; and a specialised 486 PC including additional PC cards to complete the specific tasks and read in image data. Together, these elements form a complex and costly setup. The Raax and ALT setups are shown in Figure 2-1.

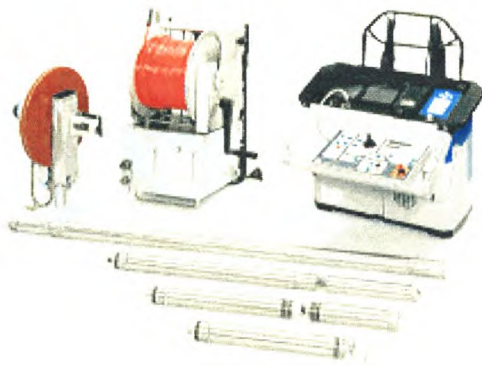


Figure 2-1 Raax BIPS³ (left) and ALT⁴ setup (right).

³ <http://www.raax.co.jp>

⁴ <http://www.alt.lu>

2.1.2 Related Patents

There are a number of patents relating to the field of borehole imaging. Schlumberger seem to have filed the first one in 1986, which consists of a hemispherical mirror being imaged by photodiodes housed in a vacuum chamber to stop them being influenced by the heat in the boreholes [2]. However, since then, RAAX seem to be the most prolific patent filers. Initially in 1992 they patented a modified conic mirror and associated imaging probe [3]. The modified conic mirror had the tip cut off and replaced by a plane 45° mirror used for high resolution detailed borehole inspection. Since then they have patented various minor advancement on this theme. Additionally, in 1996 they patented a 3D borehole imaging system [4]. It is based on a conic mirror and two Fresnel prisms. The system generates two images, one for each eye, allowing the borehole to be viewed in 3D.

Jeffrey Beckstead of Interscience based in New York, patented another modification on the conic mirror in 1998 – this time with a transparent centre, so in addition to being able view sideways it can view forward images as well [5].

In 2002 Brad Meltzer from the US company DHV International patented a method of lighting for borehole cameras [6]. Their design has a light shining on an ellipsoidal mirror. At the focus point of the elliptical mirror a fibre optics bundle takes the light and shines it out radially. They claim the increased efficiency allows the probe to contain its own battery pack and thus reduce the size of the wires attached to the probe – allowing it to go into narrower boreholes.

This patent search showed that borehole camera advancements are actively being filed. Additionally it seems conical mirrors are regularly used for borehole inspection. There may be more patents published that were not found as performing a full patent search is an arduous and expensive task.

2.2 System Innovations

The RockEye aims to be the first completely autonomous borehole imaging system with all data stored on board, as well as having its own power and light source. After deployment and once out of the mine, the captured images can be downloaded using a standard PC. This design takes advantage of the very latest trends in semiconductor camera and memory technology – the camera chip used was released in November 2003 and the flash memory card has been on the market for less than a year. The hardware of the system was designed to be simple, with all the processing completed by one FPGA. There are no moving parts, which increases the reliability of the probe. While other systems log the distance into the borehole by measuring the number of rotations of the winch deploying it, this system aims to calculate distance using post processing correlation based software working on the calibrated images taken in the borehole.

These advances in technology enable this device, consisting of only a probe, to compete with existing entire systems. Hopefully, with the increase in simplicity of this system, coupled with its ease of use, the mines will adopt borehole cameras for every day service.

2.3 Complete System Description

The prototype probe shown in Figure 2-2 has been designed with a maximum width of 38 mm to fit inside a 40 mm Perspex tube. Rightmost in Figure 2-2 is a fisheye lens to capture a view of the entire circumference of the borehole in one camera shot. Next, the borehole wall is lit using a ring of eight ultra bright LEDs. Behind the LEDs is the camera sensor and associated support circuitry, mounted facing forward. The digital output from the camera is captured and processed by the FPGA before being written to the removable flash disk memory storage. There are three LEDs to show the current probe mode. A voltage regulator ensures a steady 5V is supplied to the electronics. The LED controller handles the high current drawn by the lighting diodes. A magnetic switch enables the probe's mode to be changed while the device is sealed in a watertight package. Finally, the battery pack supplies power to the entire device enabling it to run without any wires.

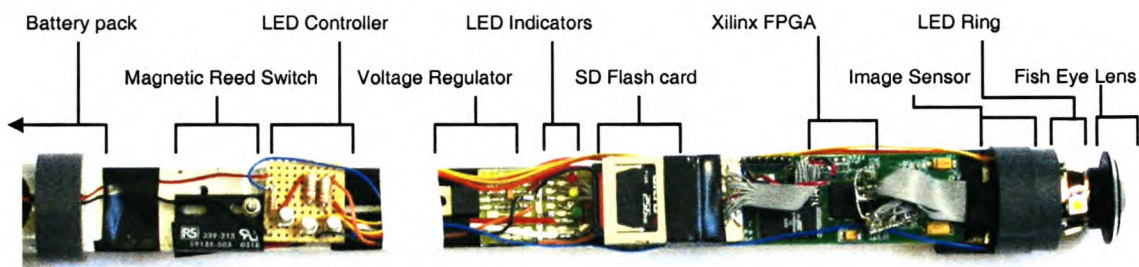


Figure 2-2 Annotated picture of RockEye probe.

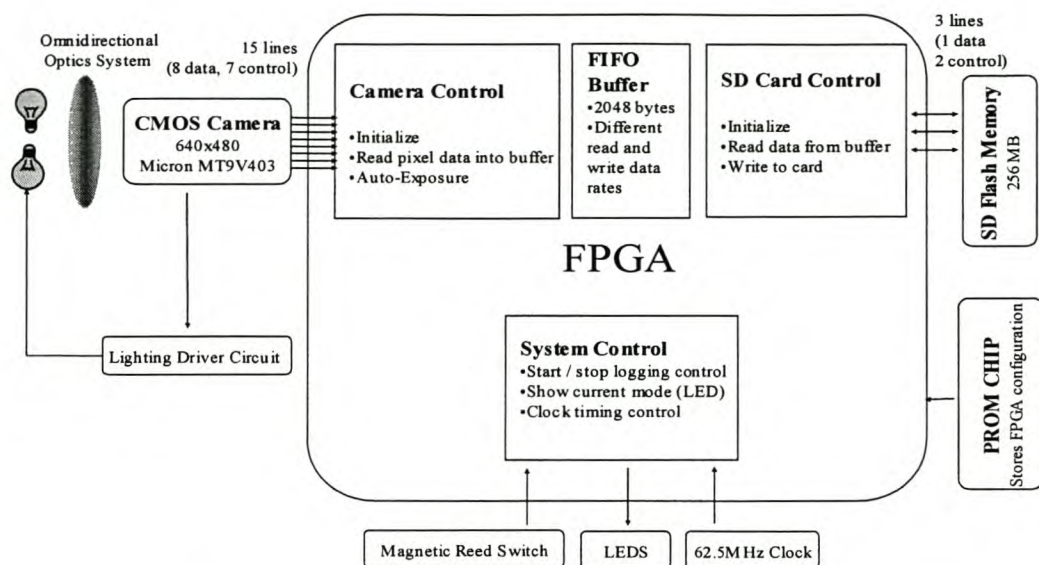


Figure 2-3 Schematic elements of RockEye system.

The various element of this design are shown schematically in Figure 2-3. They are discussed in more detail in the following subsections.

2.3.1 Omnidirectional Optics System

Although the prototype contains a fisheye lens, lens-mirror combinations were also investigated, specifically the conical mirror. The fisheye lens has a field of view of 180° enabling it to see forward as well as to the side, effectively mapping the circumference of the borehole onto the flat plane of the image sensor. The optics of this project are discussed in detail in Chapter 4.

2.3.2 Camera and Lighting

The full colour 640 by 480 pixel image sensor is capable of running at up to 200 frames per second (fps) but for this application it need only run at 10 fps. It has an internal digital shutter that eliminates the need for an external mechanical shutter. Inside the camera, the analogue values read from the light sensitive pixels are transformed into digital values by an internal 10-bit analogue to digital converter (ADC). The most significant 8 bits are read into the FPGA along with digital control lines indicating when the row and frames are valid. There is also a two wire serial interface to the camera to set internal registers such as the exposure time. The camera

and the control thereof is described in more detail in the hardware and firmware chapters.

The borehole wall is lit using eight Osram Golden Dragon LEDs. These LEDs are extremely bright over a wide viewing range. However, they use a lot of power and generate heat. To cut down on their power use, the lights are only turned on when the camera is taking a picture. There is a digital output from the camera that goes high whenever it is exposing a picture. This expose line is connected through a transistor driver circuit to the LEDs. These circuits are explained in Section 3.6.

2.3.3 FPGA Data Processing

Upon power up, the FPGA configures itself from an external programmable read only memory chip (PROM). The FPGA then initializes the camera and memory card, setting internal registers and ensuring that they are both in the correct modes to start recording picture information when the magnetic switch is activated. The FPGA is clocked using a 62.5MHz external crystal oscillator – all the internal clock rates are generated from this frequency. Three external LEDs show the current mode of the probe and if there are any faults. They were also used extensively during development for debugging purposes. From the CMOS sensor, the image data is read into an internal buffer on the FPGA and then read out and stored on the flash memory card. The firmware is described in more detail in Chapter 5 and the FPGA itself within the hardware chapter in Section 3.3.2 .

2.3.4 Flash Memory Storage

A Secure Digital (SD) flash card is used to store the images. Flash memory is a nonvolatile memory storage type, so when the power is switched off, the data remains. This flash disk has a capacity of 256MB allowing storage of 1070 images. It is controlled by a command line, a clock line, and a data line. Once the images have been recorded on the card, it can be removed from its holder and downloaded on any PC with an SD card reader and some specialized software. The methods used to write to the card are outlined in Section 5.3 and the card itself is described in Section 3.4.

Chapter 3 Hardware Design

This chapter examines each of the hardware elements in detail. Firstly, examining the available technology, and then justifying the choices made for this design.

3.1 Hardware Overview

The hardware in this system is split into four functional groups: data capture, data processing, data storage and data download. Each of these functional groups is examined in the rest of this chapter under the sub-sections: image sensor, processing power, flash storage, and USB communications. Although USB communications have not been built into the current prototype, they were tested successfully during development and it is envisaged that a final system may include USB download capabilities.

3.2 Image Sensor

3.2.1 Image Sensor Requirements

For this application the image sensor has the following requirements:

Resolution

The image sensor's resolution is determined by the desired azimuth resolution on the borehole wall. The vertical resolution is set by the optics. One of the initial specifications was that the system should be able to discern features that are 0.5 mm in width in a 48 mm diameter (150.7 mm circumference) borehole. To meet this criterion, the image sensor should have an azimuth resolution of approximately 0.2 mm per pixel. A 640x480 pixel standard size will achieve this as it has a maximum ring circumference of roughly 1507 pixels ($480 \times \pi$), resulting in a resolution of 0.1 mm per pixel for the outer ring. The minimum diameter in number of pixels to achieve a

0.2 mm resolution is 240, where the circumference is 754. Thus, we can have an annular ring that is up to 120 pixels wide.

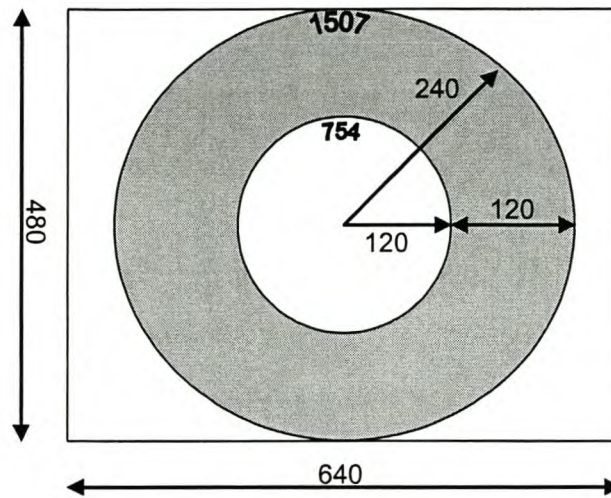


Figure 3-1 CMOS sensor showing desired annular region in grey.

Colour

The final graphic representation of the core should look like it does if one was viewing it with one's own eyes. For this, we need a full colour picture with at least 8 bits per colour – forming a 24-bit red, green and blue (RGB) image.

Frame Rate

Suppose, the probe is deployed at 100 mm per second and each picture scans a region of approximately 24 mm (120 pixels times 0.2 mm per pixel). Thus the minimum frame rate is 5 fps. Eventually the individual frame images should be stitched together and some overlap must be allowed so the eventual frame rate will be higher than 5 fps.

Electronic Shutter

Most image sensors employ a form of rolling shutter where a narrow band of the sensor is exposed sequentially. The width of the band is determined by the exposure settings. This process is shown in Figure 3-2. In this system, the probe is moving while taking pictures of the nearby borehole wall. A rolling shutter will result in a distorted image similar to the picture of a bus in Figure 3-3. Another option is to include a mechanical shutter, but this adds unwanted moving parts to the design and

size issues may be a problem. In this system an internal electronic full frame shutter is desired.

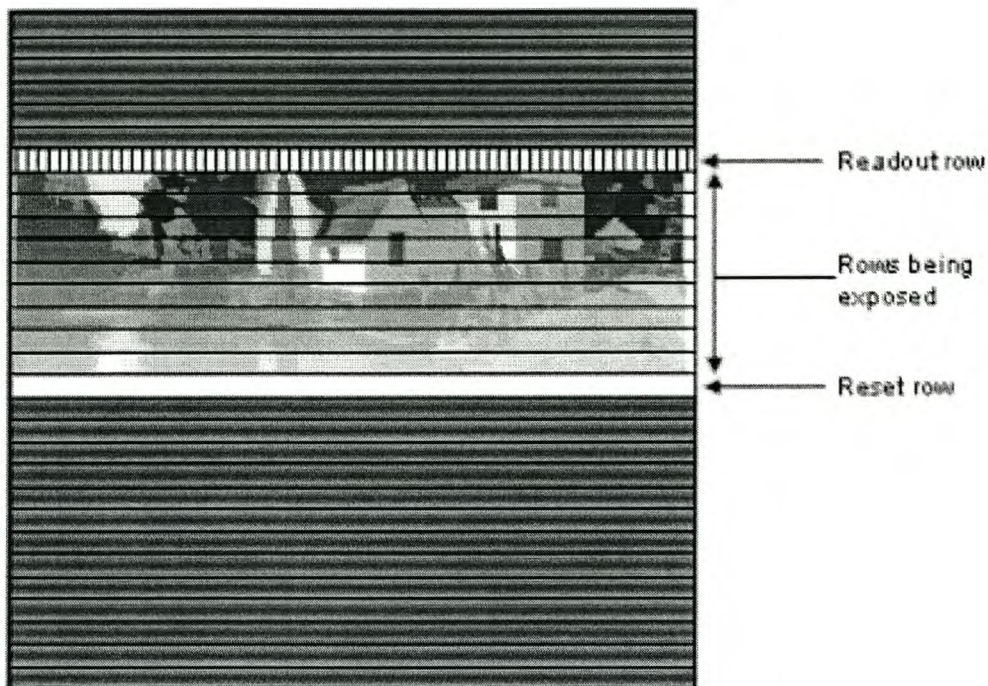


Figure 3-2 Illustration of the workings of a rolling shutter.



Figure 3-3 A picture of a moving bus taken with a rolling shutter CMOS sensor [7].

Light Sensitivity

Again, as the probe is moving while taking pictures, the exposure time has to be kept to a minimum to combat blurring. A combination of a sensitive camera and a bright light will have to be used.

3.2.2 Image Sensor Technology

With the recent boom in the digital camera market there are numerous image-sensing microchips available. Two competing technologies in this arena are Complementary Metal Oxide Semiconductor (CMOS) sensors and Charge Coupled Devices (CCD). The most significant differences between the two relate to how electrons are transferred from the sensor and the fact that CMOS can incorporate more processing functions on the chip. Initially, both CMOS and CCDs were invented as solid-state memory storage devices and neither had anything to do with digital photography.

In the 1960s various scientists discovered that CMOS could be made photosensitive. Around the same time, developments in the Bell Labs found CCDs to have impressive charge transfer capabilities that would make them ideal for image sensing. The first commercially available CCD image sensor was produced in 1973.

CCDs are specialized chips, used only for image capture manufactured by only a handful of very specialized fabrication facilities such as those owned by Sony, Philips, Kodak, Matsushita, Fuji, and Sharp. CMOS however, used in many more kinds of devices, including the vast majority of consumer electronic devices, are produced using standard processes in high volume facilities. Economics of mass production are such that CMOS image sensors are considerably less expensive to manufacture.

Other factors add to CMOS image sensors cost effectiveness. They can include image processing and analogue-to-digital converters (ADC) on-chip. This makes CMOS sensors significantly less expensive to build and buy, as well as physically smaller. CMOS image sensors also require less energy than CCDs so they need less battery capacity. They are a digital camera one chip solution and normally require only additional decoupling capacitors.

In recent years, CMOS imagers have improved in picture quality significantly and now come close to rivalling CCDs. However, in systems for which image quality is the most important factor, a CCD is still superior. It has greater sensitivity to light, better dynamic range and less noise.

For this project, a CMOS imager was chosen for the above reasons and the fact that although important, absolute image quality is not the highest design priority. The image quality is likely to be limited by external factors, such as unclear water or dirt in the harsh mine environment, rather than image sensor technology itself.

3.2.3 CMOS Image Sensor

Most of the ready built camera modules are physically too large to fit inside the Perspex pipe. It is thus necessary to build up an image sensor from the basic building blocks including the CMOS chip and all associated circuitry on a custom built PCB. This also allows us to choose the best suited image sensor for this application.

There are a vast array of CMOS image sensors on the market at the moment. The main industry players are Kodak, OmniVision, Mitsubishi, ST-Microelectronics, and Micron. The full frame electronic shutter constraint is the most limiting factor as most sensors have the more common rolling shutter described in Figure 3-2. Kodak and Micron have sensors with these capabilities. However, the Kodak sensor's freeze frame only works when in single picture mode, which will not work for this application. The Micron MT9V403 image sensor, Figure 3-4, was released in November 2003. It has an array of 659x494 pixels and incorporates TrueSNAP™ full freeze frame shutter technology. The chip is capable of running at speeds of up to 200fps which is faster than will ever be required in this application. There is an onboard 10-bit ADC connected to the 10 line parallel digital output pins.

Micron is one of the leading CMOS chip manufactures worldwide. Historically they concentrated on manufacturing memory chips for PCs. Recently in 2001, they bought out Photobit, the CMOS image sensor manufacturers. Photobit were originally a spin-off company selling the image sensing technology developed by the NASA Jet Propulsion Laboratories.

The MT9V403 sensor also incorporates a two wire serial interface used to set various internal registers. These control different aspects of the sensor including exposure time, image window size, pixel gain factors, etc. Each pixel measures 9.9 by 9.9 μm

which is fairly large in comparison to most sensors on the market. The large size increases the light sensitivity and decreases the noise present. From the frequency response shown in Figure 3-5 it is clear that the sensor is sensitive to near infrared light. Either an infrared filter must be used or the lighting must not emit infrared light.

External circuitry needed to run this sensor is limited to an array of decoupling capacitors and two potentiometers for setting external voltages. A PCB was designed, then manufactured by TRAX⁵ and populated by ELPROM⁶.

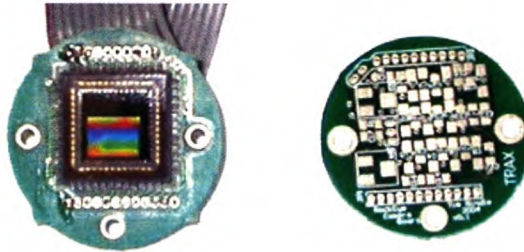


Figure 3-4 Camera board with Micron MT9V403 sensor front, back unpopulated.

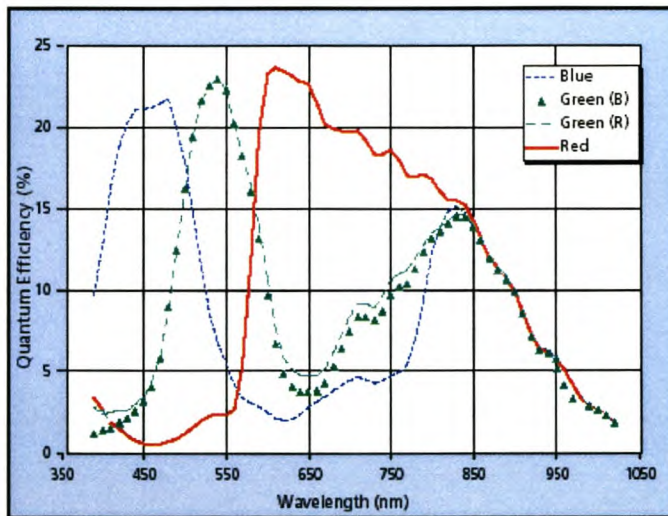


Figure 3-5 Micron MT9V403 frequency response [8].

⁵ <http://www.trax.co.za/>

⁶ <http://www.elprom.co.za/>

3.3 Processing Power

3.3.1 Processing Requirements

There are many different options available to solve the processing needs for this system. The quest is to find the solution that will perform all the desired functions with a fair amount of configurability, without compromising the complexity or price of the end product.

For the high speed and accurate timing needed to get data from the CMOS imager to the flash memory, an FPGA is the optimal solution.

A DSP is the best option for the onboard image processing tasks including image scaling and unwrapping of the annular ring. However, this processing would be better done on a PC with a fast CPU and plenty of RAM rather than on an embedded processor. External data processing would mean extraneous data has to be stored in the onboard memory and a larger capacity for data storage will be needed.

The dedicated camera processors made by Texas Instruments and others are specialised and not highly configurable, although they do contain some nice features like built in JPEG encoders and USB connectivity.

The initialization procedures for the camera and flash card are easiest to perform on a microprocessor. However one can also implement simple processors on an FPGA like the Pico-Blaze 8-bit processor offered free by Xilinx.

The most common solution to the camera processing requirements is a combination of an FPGA and a small microprocessor. The FPGA is used to shift the vast amounts of data around within the strict timing constraints and the processor is used to initialize the various components as well as communicate with the outside world. However, in this design, the bold choice was made to go with just a single FPGA. At the cost of extra time and difficulty during programming, the benefits of a single chip design will pay off if this design goes into small scale production.

3.3.2 FPGA Technology

There are a multitude of FPGAs on the market today. The two main chip manufactures, Xilinx and Altera dominate the market, with some competition now coming from Actel. FPGAs within the various ranges are characterized by:

- Number of system gates
- Number of IO pins
- Amount of internal RAM
- Package size

Development of the VHDL code began before the chip was chosen leading to the conclusion that one of the smaller entry level chips would suffice for this design. There was not much difference between the devices offered by Xilinx and Altera, however the embedded block memory feature of the Xilinx Virtex series finally swung the decision in their favour – even the smallest Virtex FPGA has 4 KB of internal block ram.

The major benefit of this choice is that programming for the prototype could start immediately using an FPGA test board designed by J Hargreaves⁷. It incorporates the smallest Xilinx in the Virtex range, the XCV50. A few board modifications were needed to access the FPGA IO pins. The test board incorporates some other ICs, however, the only ones used in the prototype were: the FPGA and associated PROM chip (highlighted in Figure 3-6): a 62.5 MHz clock, and the 3.3 V and 2.5 V power supplies.

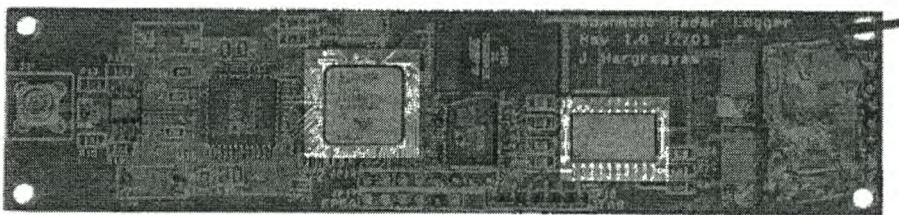


Figure 3-6 Test board, FPGA and PROM highlighted.

⁷ Dr J Hargreaves works for Geomole and the University of Sydney.

3.3.3 Xilinx Virtex FPGA

Xilinx Virtex devices feature a flexible architecture that consists of an array of configurable logic blocks (CLB) surrounded by programmable input/output blocks (IOB), all interconnected by versatile routing resources shown in Figure 3-7. Virtex FPGAs are volatile RAM-based, and are customized by loading configuration data into internal memory cells. When the power is cycled the configuration is lost. For this design a Programmable ROM (PROM) chip is connected to the FPGA so that whenever the power is switched on, the FPGA automatically configures itself from the PROM. The PROM is loaded with setup data through a JTAG port from a PC using the Xilinx software and download cable.

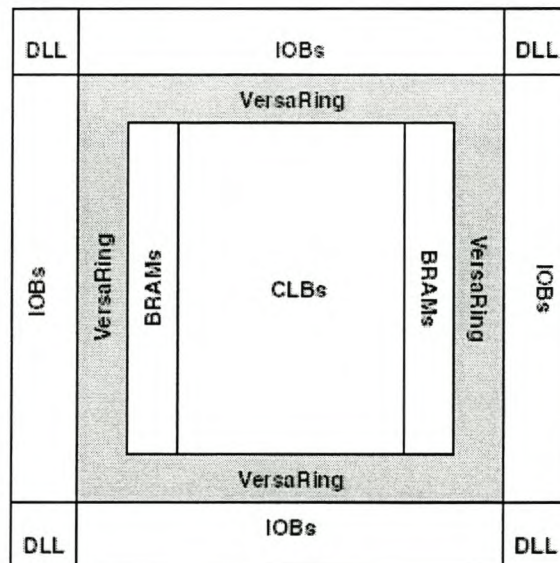


Figure 3-7 Virtex architecture [9].

The Xilinx XCV50 has 57,960 logic gates and is packaged in the CS144 (12x12 mm) package allowing it to have a maximum of 94 IO pins. It contains four delay-locked loops (DLL) that are used to eliminate clock-distribution delays and provide phase shifted versions of the source clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

The basic building block of the Virtex CLB is the logic cell (LC). A LC includes a 4-input look up table (LUT) function generator, carry logic, and a storage element. Each Virtex CLB contains four LCs organized in two similar slices, as shown in Figure 3-8. These simple building blocks are routed together to form complex logic capable of executing the desired processing tasks.

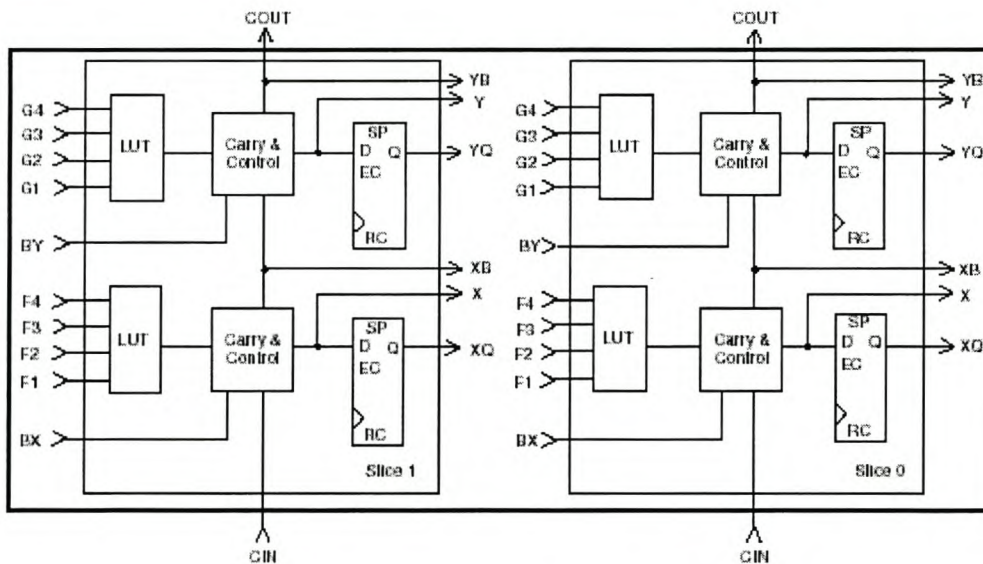


Figure 3-8 Two slice vertex CLB [9].

3.4 Flash Memory

3.4.1 Memory Storage Requirements

The recent developments in the field of mass storage flash solutions is the main enabling technology that allows this autonomous device to be built, permitting the RockEye to break away from the conventional TV camera on a wire devices.

Previously, the forms of non-volatile memory included EEPROM, DataFlash™, and magnetic storage media. These old technologies are too bulky, too slow, or do not have enough storage capacity for this application. Flash memory is so called because entire sections of the microchip can be erased at once, or flashed. Most high end flash memory is based on NAND gate technology.

The storage capacity for this system can be accessed from an area perspective. For a 150 m borehole of 48 mm diameter (150.7 mm circumference) the borehole picture area is 22.619 m². A resolution of 0.2 mm per pixel in both directions, gives 25 million pixels per square metre. This works out to 565 million pixels, with 8 bits per pixel a total storage capacity of 565 MB of data is needed.

These calculations are for a perfect system, however currently there is no means for the probe to accurately measure the distance into the hole. Thus the frame rate and size of the picture will have to be accurately matched to the deployment speed with an additional overlap. The overlap must be able to cover for the variations in speed to ensure that no image information is lost. The average percentage overlap is directly proportional to the increase in data. Additionally, all parts of the image are not taken at the same resolution as shown in Figure 3-1, resulting in an added increase in data. However, flash technology is developing at a rapid rate and there are currently up to 1 GB flash cards on the market.

Another constraint on the storage medium is the burst and sustained write speeds. Burst write speed is defined as the maximum speed at which data can be written to the flash device. The sustained rate is the average write rate, taking into account the time

between write operations when the microchip is busy. To calculate the maximum data rate needed for this application – assume 10 fps and that the entire image square image (480x480 pixels) is stored for each frame. Each frame then contains 230400 bytes of data resulting in a required maximum data rate of 2.3 MB/s.

3.4.2 Flash Technology

Two different approaches can be taken when deciding on which flash technology to use. One option is to use the basic flash microchip. These are simply bulk storage devices with no additional internal circuitry. However, flash memory is not completely reliable, two different types of errors present themselves, bad blocks from manufacturing faults and erroneous bits appearing during operation. Initial bad blocks have to be scanned for and mapped out by the firmware before any writing operations can take place. The error bits that appear from time to time can be corrected by developing error correcting codes. Developing this firmware would be time consuming and it is currently the subject of an MSc thesis⁸ here at Stellenbosch University.

The other option is to use one of the pre-packaged flash cards as used in digital cameras and hand held PCs. Most of these cards include sophisticated controllers that handle the transfer of data to the flash memory, as well as powerful error correcting codes. For example the SD card has a data reliability rating of less than one non-recoverable error in 10^{14} bits read. This means that there should be less than one bit error for every 12 500 gigabytes of data read. Table 3-1 documents the specifications of some of the more popular flash cards on the market at the moment.

⁸ Ian Horsburgh, “The Analysis of NAND Flash Memory for a Mass Memory Unit on a Micro-Satellite”, Electronic System Laboratory.

	SD	MMC	Compact Flash	Smart Media	Memory Stick
Power Ratings					
Sleep	150 μ A	150 μ A	200 μ A	20 μ A	1.5 mA
Read	40 mA	35 mA	35 mA	10 mA	65 mA
Write	45 mA	45 mA	35 mA	10 mA	100 mA
Typical speeds ⁹					
Burst [MB/s]	10	2.5	16	8	10
Read [MB/s]	3 – 10	1.4	3.3 – 5.9	3.5	10
Write [MB/s]	0.8 - 9	1.2	1.5 – 4.8	3.5	1.875
Physical size					
Length [mm]	32	32	36.4	45	50
Width [mm]	24	24	42.8	37	21.5
Thickness [mm]	2.1	1.4	3.30	0.76	2.8
Capacity [MB]	16 -1000	32 - 128	64 - 4000	8 - 128	128 - 2000
Temp Rating [°C]	-25 – 85	-25 – 85	0 – 60	0 – 55	-25 – 85

Table 3-1 Flash card comparisons.

The borehole probe size constraint excludes use of the Compact Flash and Smart Media cards. It is notoriously difficult to get hold of the technical data regarding operating the Sony memory stick and for this reason it was excluded. The two cards left, the Multimedia card (MMC) and its successor, the Secure Digital (SD) card are physically almost the same size and compatible in some devices. However the MMC is not produced in large capacities (greater than 128 MB) and has slow read and write speeds. SD cards contain newer technology and are being aggressively developed as well as adopted in many new products including a range of Nokia phones. There is also an Ultra II range of SanDisk SD cards that have a guaranteed sustained read and write speed of above 9 MB/s. For the prototype RockEye a 256 MB SanDisk Ultra II SD card was used.



Figure 3-9 SanDisk Ultra II SD flash card.

⁹ The write and read speed vary considerably from one brand of card to another. Speeds also vary considerably between different capacity cards from the same manufacturers. Speeds based on results from <http://www.digit-life.com/articles2/flashcard-test/flashcard-test-p2.html>

3.4.3 Secure Digital Card

The SD Card specifications were originally defined by Matsushita Electric Company, Toshiba Corporation and SanDisk Corporation. Currently, the specifications are controlled by the Secure Digital Association (SDA)¹⁰. The SanDisk SD Card [10] was designed to be compatible with the SD Card Physical and Protocol Specification as set out by the SDA.

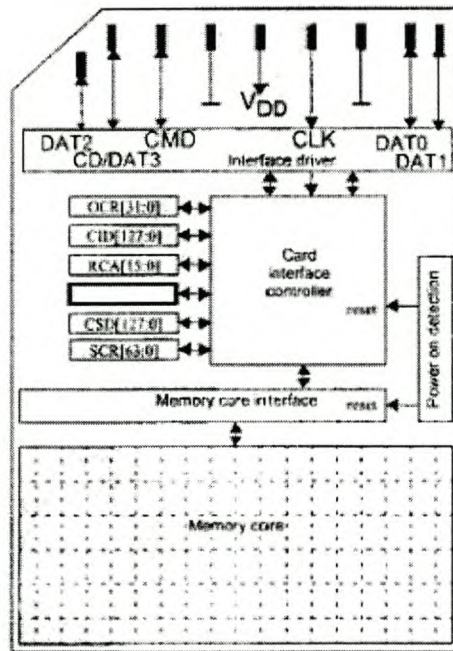


Figure 3-10 Secure Digital flash card inner workings [10].

The SD card has nine external lines: four data lines, a clock line, a command line, a power line and two grounds. The card can be used in either one or four data wire mode. With one wire the maximum data rate is 3.125 MB/s and with four it is 12.5 MB/s, however, this is the burst speed whereas this system is still limited by the overall sustained transfer rate of the card. Figure 3-10 shows a representation of the internals of an SD card. The flash memory core is controlled through the memory core interface by the card interface controller. The smallest amount of data that can be read or written is 512 bytes. There are also various registers and card addresses that can be read. A complex initialization procedure must be followed, which is described in more detail in Chapter 5.

¹⁰ <http://www.sdcard.org>

3.5 USB Communication

From the initial specifications the Bluetooth protocol for wireless downloads was investigated. Currently, there is a good implementation for serial RS232 to Bluetooth connectivity using Bluewave technology. However, this would be a laboriously slow process as the current serial download speed is 57 600 bits per second. Approximate download times for two different sized files are shown in Table 3-2 for different communication protocols. Firewire, also known as IEEE 1394, is not included as it is very similar to USB 2.0 in speed.

Protocol	Speed [kB/s]	Speed [kB/s]	90 MB file download time [h:m:s]	512 MB file download time [h:m:s]
RS-232	57.6	7.2	3:30:00	19:45:00
Bluetooth	723	90.125	0:16:00	1:34:00
USB1.1	1500	187.5	0:08:00	0:47:00
USB1.1- Full Speed	12 000	1500	0:01:00	0:06:00
USB 2.0 ¹¹	480 000	60 000	0:00:02	0:00:09

Table 3-2 Data rates of various communications protocols.

From Table 3-2 it is clear that for a reasonable download time the minimum acceptable protocol is USB 1.1. There is a very useful chip made by FTDI, the FT245BM. This IC accepts 8-bits data and handles all USB communications with a host PC, in a first in first out (FIFO) manner. It includes a 384 byte transmit buffer and a 128 byte receive buffer which ensures maximum data transfer rate. There are free dynamic link libraries (Dlls), provided by the manufacturer to aid in Windows™ USB direct communications development. Data can be transferred at up to 1 MB/s using these USB Dlls. This chip is also available as part of a ready built module, as shown in Figure 3-11, including the necessary external circuitry and USB connector – very handy for development work.

¹¹ Assuming the flash memory could be read at this speed, which is not possible.

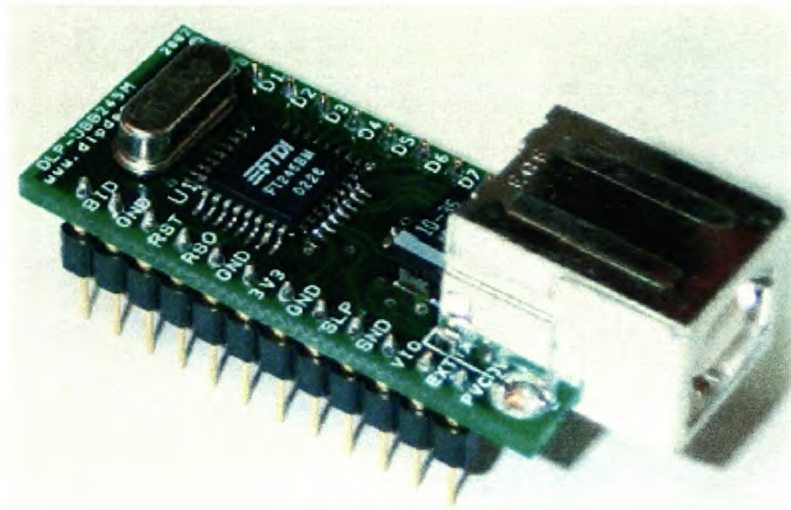


Figure 3-11 USB module including FTDI245BM microchip [11].

The USB chip is fairly easy to operate. Data is placed on the 8 parallel input lines and the write line (WR) is clocked from high to low. The transmit allow (TXE#) line should also be monitored to check when the internal buffer is full. On the PC side an application is written using Borland C++ Builder to communicate through the FTDI Dlls with the USB port. The received data is then saved directly to file. Before the SD card was up and running, this USB module was used extensively and the first pictures from the camera were downloaded through it. This was an important step in the development of the entire system as it proved the camera and FPGA were working correctly before the memory card was added.

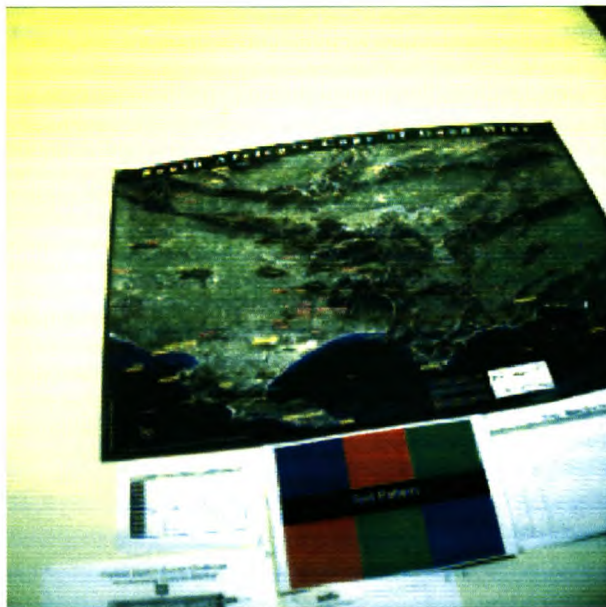


Figure 3-12 First picture from the camera, downloaded through USB port.

3.6 LED Lighting Circuitry

The Golden Dragon™ LEDs made by OSRAM draw 350mA each and have a forward voltage of 3.2 – 3.6 V. Their spectral emission does not extend past the visual range so no infrared filters are necessary for the camera. They are capable of emitting 10,000 mcd with a viewing angle of 120°. During operation they need to dissipate one watt of power which is only possible if special considerations and materials are taken into account when designing and manufacturing their mountings. To save power and eliminate the need for this costly thermal management, the LEDs are only turned on when the camera is in the expose mode. The digital expose pin output from the MT9V403 image sensor goes high whenever the sensor is taking a picture. This pin can only drive 0.2 mA and is thus connected through a modified Darlington pair transistor circuit to drive the high power LEDs directly from the 7.6 V battery pack. The LEDs cannot be connected directly in parallel as their forward voltages differ and are therefore connected as four sets of two LEDs in series each with a resistor. Figure 3-13 shows this circuit. A high power TIP41C transistor is used to switch on the LEDs handling a peak current of 1.4 A. A large capacitor is added in parallel to handle the current surges.

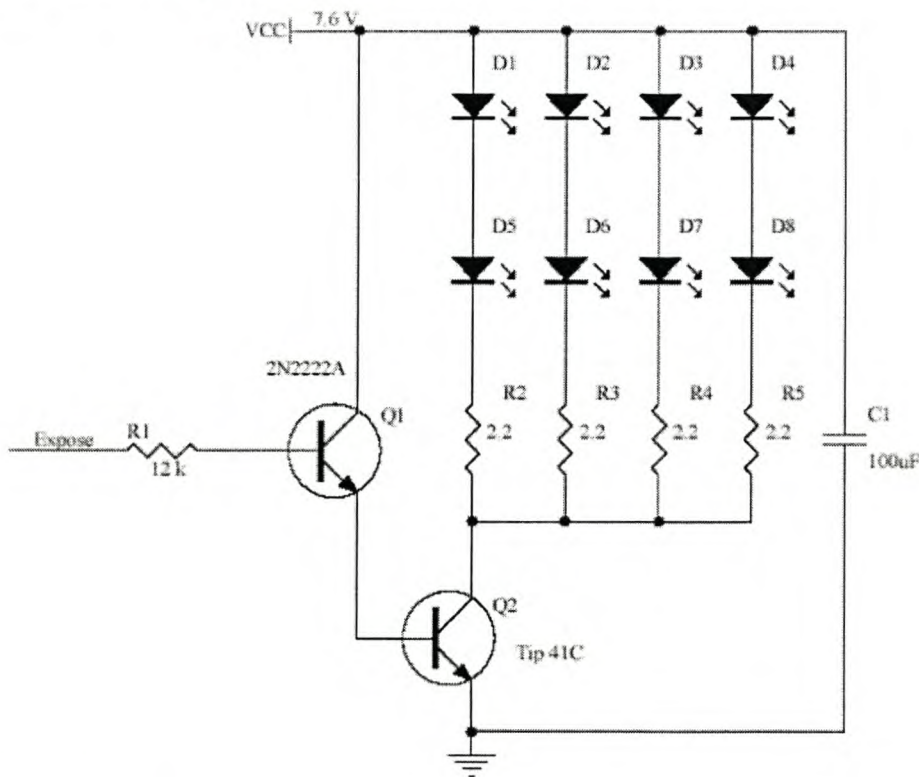


Figure 3-13 LED driver circuit.

Chapter 4 Optical Design

This chapter presents the design and implementation of the optics part of the RockEye system. The goals for the optics are first described, followed by an in-depth study. Two different optical solutions, the conic mirror and the fisheye lens, are presented.

4.1 Optics Overview

The objective for the optics in this system is to map an image of the circular borehole onto the flat CMOS sensor. There are various ways to acquire an omnidirectional (360°) view using a single camera as presented in patents, available literature, and existing systems, including:

- Hyperbolic mirrors
- Paraboloidal mirrors
- Spherical mirrors
- Conical mirrors
- Fisheye lenses

With the exception of the fisheye lens, which will be dealt with later, the above omnidirectional sensors consist of a combination of lenses and mirrors. These are known as catadioptric systems. Dioptrics is the science of lens refracting elements, and catoptrics the science of mirror reflecting surfaces [12]. The combination of refracting and reflecting elements is therefore referred to as catadioptrics.

The most common catadioptric setup includes a convex mirror placed in front of a lens and aligned with the centre of the lens system on the optical axis. The mirror collects light from 360 degrees around the device, reflecting it through the lens system, which focuses it to provide a sharp picture on the CMOS sensor. The generalised setup is shown in Figure 4-1. Instead of using mirrors, prisms could also have been used, where the shape of the mirror is cut from a suitable transparent medium, based on the total internal reflection criteria. A prism system has to be well designed to stop chromatic aberrations causing the various colours of the spectrum to

be refracted at slightly different angles. Before describing each of the omnidirectional mirror setups in more detail, some constraints are introduced.

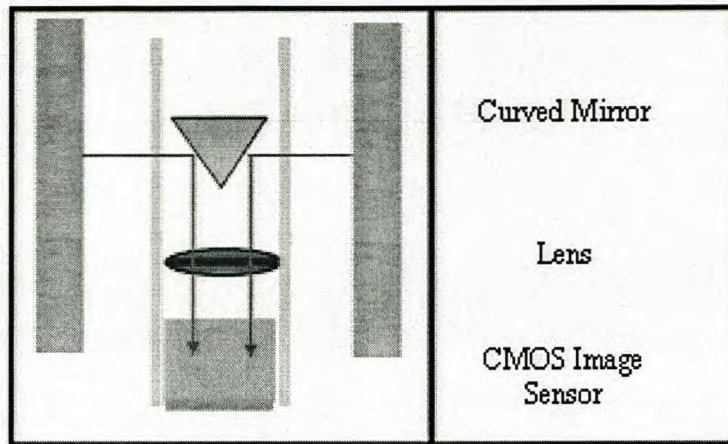


Figure 4-1 General optics setup.

One of the constraints often cited in omnidirectional literature is the single view point constraint. Under the single viewpoint constraint, every pixel in the sensed image measures the irradiance of the light passing through the viewpoint in one particular direction. A single viewpoint is desirable as it is a requirement for the generation of geometrically correct perspective images as well as panoramic ones from the images captured by the catadioptric cameras. However, although it is optically beneficial, it is not an absolute necessity for this system to have a single viewpoint in order to produce useful images.

The other constraints are of a more practical nature – the optics for this system should be small to fit inside the borehole. The mirror must be physically easy to manufacture or commercially available – custom optics are often prohibitively expensive, with long lead times for manufacture. It is more preferable to be able to use off the shelf components.

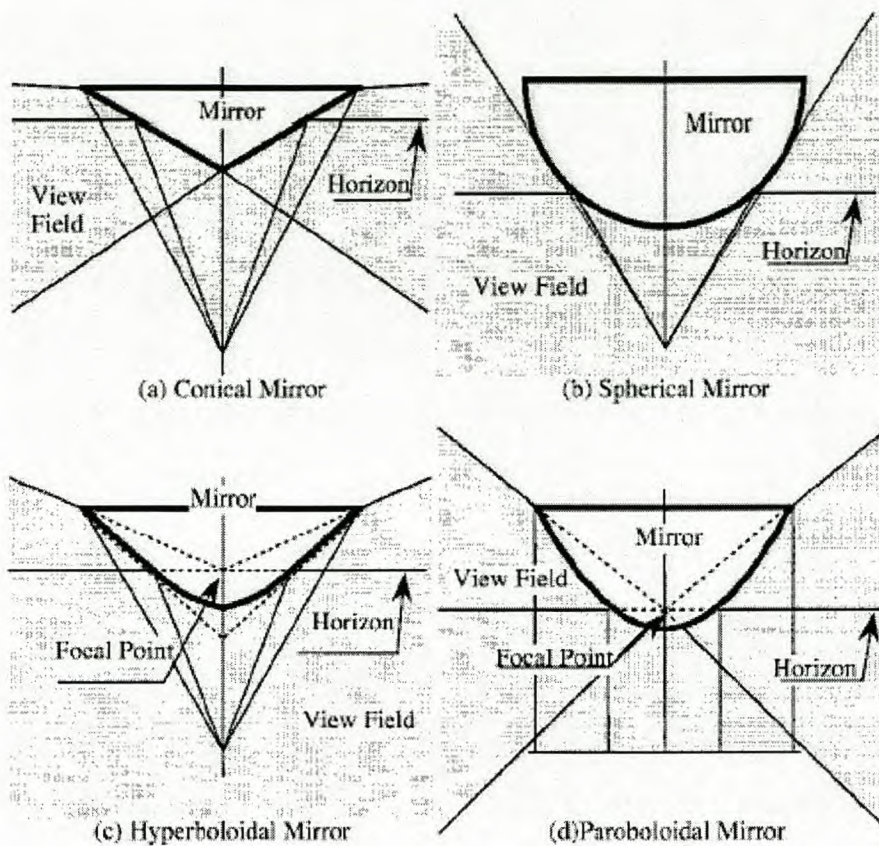


Figure 4-2 Mirror field of view, image from [14].

4.1.1 Spherical, Hyperboloidal, and Paraboloidal Mirrors

These three mirrors shown in Figure 4-2b, c and d are fairly similar in nature. They all have a large angular field of view – which is not necessary for this application as the camera is only viewing a thin band of the rock wall. The spherical mirror has the largest field of view and has good central resolution but poor peripheral resolution. According to Baker and Nayar [13], the spherical mirror satisfies the single viewpoint constraint only when the effective pinhole is placed at the base of the sphere – in which case the observer will only be able to see itself as the point of the sphere is flat. Hyperboloidal and paraboloidal mirrors do conform to the single viewpoint constraint and have better peripheral resolution due to the narrower field of view.

4.1.2 Conical Mirror

The cone mirror or conic section can be thought of as an angled plane mirror rotated about the optical axis. The cone mirror is the only system that can get a perfect image vertically when you use a perfect lens system as it is a plane mirror in the vertical direction. All other curved mirrors introduce defocus blurs in the vertical direction as they are curved longitudinally [13]. So even with a perfect lens system you can not get a perfect vertical image in those mirrors. In the concentric direction, all omnimirrors are curved with the same horizontal cross-section shape – circles.

Baker and Nayar [13] as well as Yagi [14] suggest that the conical mirror has a single view point, but as it is located at the tip of the cone it is a degenerative case and not of any practical value. However, Lin and Bajcsy [15], argue that if true geometric Gaussian optics are used in place of the simplified pin-hole optics, used by Baker and Nayar, there are two effective pinholes in the system – one at the tip of the cone, the other a distance f away. Where f is the front focal length of the thin lens used. Lin and Bajcsy built a successful prototype system to prove their theory.

The conical mirror configuration also gives a linear compression of the image towards the centre of the cone – this should make the unwrapping algorithm easier. Conical mirrors are also commercially available off the shelf from Edmund Scientific¹². They stock a range of micro lenses with 10, 5, and 3 mm diameters costing about US \$175 each.

Due to the positive reviews in Lin and Bajcsy's article and their commercial availability, initial test went ahead with the conic mirror setup. However, as described in Section 4.2, problems were encountered and a fisheye lens was also investigated, described in Section 4.3.

¹² <http://www.edmundoptics.com>

4.2 Conical Mirror Optical Setup

The setup for an omnidirectional imaging system using a conical mirror as suggested by Lin and Bajcsy is shown in Figure 4-3. The setup consists of a mirror, a thin lens and an image sensor. The point of the conical mirror is placed a distance f away from the lens at the front focal point. Point B is the imaged point on the borehole wall; b is the virtual point as seen when looking at the mirror from the top; β is the corresponding point on the image plane, sensed on the CMOS imager. Various rays are traced between B and β to give some insight as to what is happening with the optics.

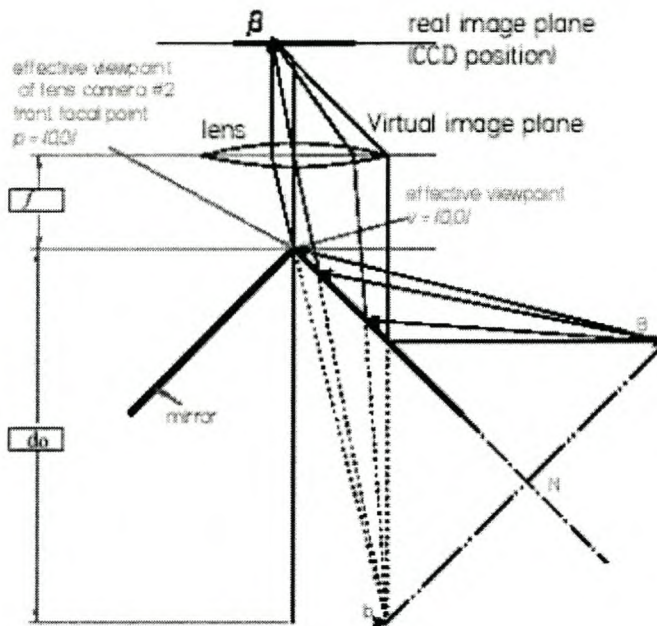


Figure 4-3 Cone mirror setup as suggested by Lin and Bajcsy [15].

The system can then be focussed according to Gaussian optic lens laws, ignoring the lens and just calculating the total path length. Where d_o is the total ray distance to the object being imaged; d_i , the distance from the virtual image plane to the image sensor; and f the lens's focal length.

Gaussian optics was developed for paraxial¹³ rays. It states that all rays that come from the same object point in the world and enter the focused optical system, converge at the same point. Using this, any two rays can be traced from a world point to find its image point. Normally the two most easily traced rays are used.

- The ray that passes through the front focal point is refracted by the lens and then proceeds parallel to the optical axis.
- The ray that passes through the centre of the lens is not affected and carries on travelling in its original direction.

This is illustrated in Figure 4-4. Equation 4-1, the standard thin lens formula, can be derived from similar triangles. The magnification (m) can also be worked out from the relationship between d_i and d_o .

$$\frac{1}{d_o} + \frac{1}{d_i} = \frac{1}{f}$$

$$m = \frac{d_i}{d_o}$$

Equation 4-1 Gaussian thin lens formula.

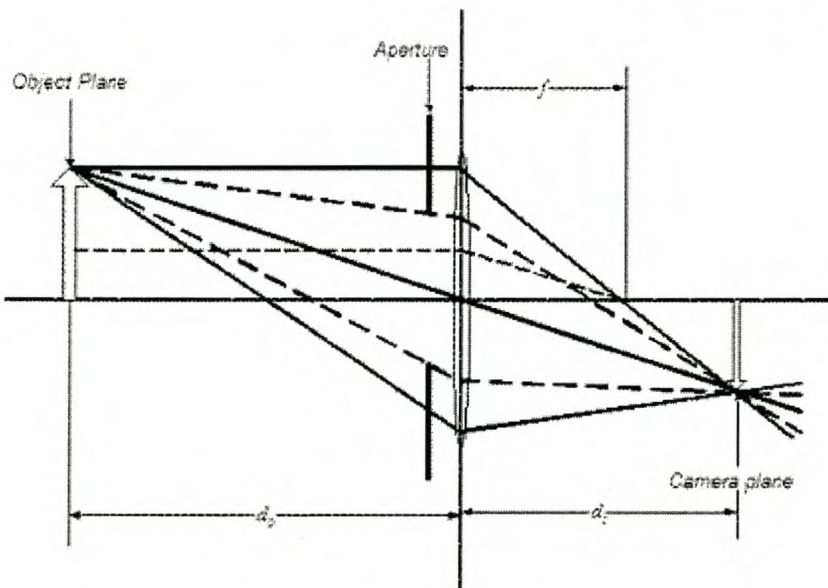


Figure 4-4 Gaussian simple lens setup¹⁴.

¹³ Rays that arrive at the lens at shallow angles with respect to the optical axis, i.e. almost parallel to the axis.

¹⁴ Image from http://www.high-techdigital.com/integration/optics_t_2.htm

Armed with the theoretical knowledge of the accepted setup of an omnidirectional catadioptric sensor, a test setup was built. Three conical 45° mirrors were sourced. Two, a 10 mm and a 5mm, come from Edmund Scientific in the U.S and one, a 14 mm, from MIT (Measurement Instrumentation Technology) in Johannesburg. The 14 mm glass cone was not coated originally and it was kindly coated with reflective aluminium by METGLO in Brakenfell. The mirrors were then mounted into the threaded PVC holders shown in Figure 4-5.

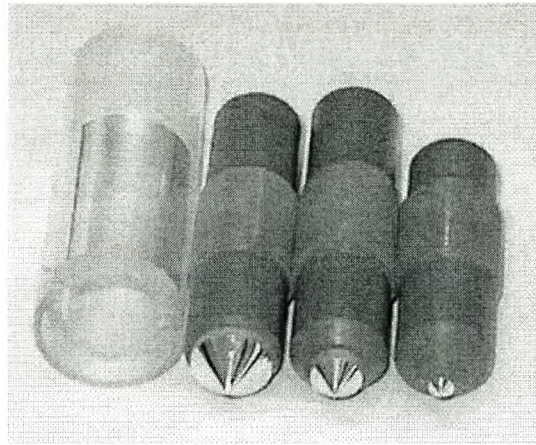


Figure 4-5 Test mirrors (14, 10, 5 mm) and clear mounting tube.

These PVC holders screw into a clear Perspex tube into which the camera is mounted on the opposite side. A section of 66 mm PVC pipe was cut and used as a test borehole, shown in Figure 4-6. Different printed test patterns were placed inside, in Figure 4-6 it contains a grid pattern. A circular aluminium disk was machined to hold the Perspex pipe in the centre of the test borehole.

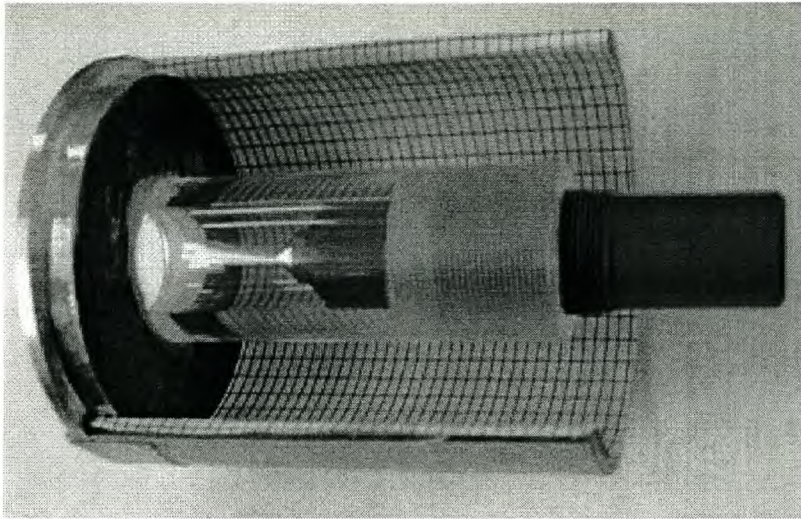


Figure 4-6 Conical mirror test setup.

A standard PCB mount lens holder with a micro-lens was mounted onto the camera board and connected to the Perspex tube. It was soon found that the standard micro lenses are more complicated than they seem. Further investigation by Robin Starke [16], revealed that these seemingly simple lenses actually consist of three to four internal lens elements and are remarkably complex for such standard, inexpensive lenses. They also have different front and back focus planes that are not well defined – which makes focussing by any means other than educated trial an error impractical.

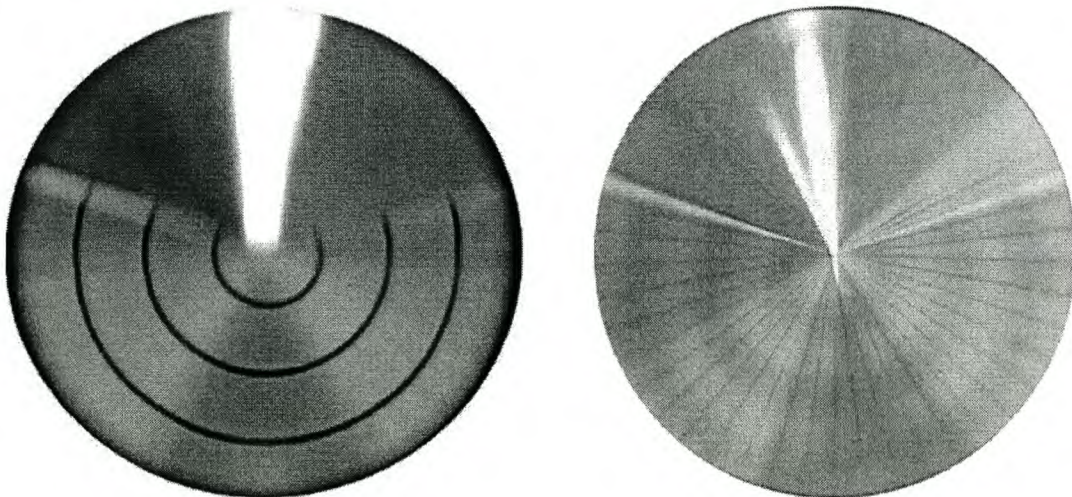


Figure 4-7 Concentric or radial lines in focus¹⁵.

¹⁵ These photos were taken using a Nikon Coolpix digital camera.

The photos in Figure 4-7 are taken using the test setup shown in Figure 4-6, photographing the mirror in the test setup viewing the grid pattern. Due to the time consuming processes involved in taking pictures, and the difficulty in changing the focus of the RockEye camera while connected in the test setup, a standard digital camera was used to take the above pictures. By varying the focus settings it is possible to either get the concentric ring (left-hand picture) or the radial lines (right-hand pictures) in focus. This unexpected result was confusing at first but was clarified by looking through Hecht's chapter on aberrations [12]. Figure 4-7 exhibiting the effects of the astigmatism aberrations, introduced by the conical mirror.

Astigmatism in classic optics is a defect in the surface of a lens or mirror where the focus of a light beam varies depending on how far off centre the light beam hits the lens or mirror. For example, light hitting the centre of an astigmatic lens might focus at 20 cm while light hitting the outside of the lens would focus at 20.5 cm. The actual focus of the lens would then vary from 20 to 20.5 cm, with no perfect focus. However, in this case the astigmatism is caused by the curvature of the conical mirror.

If a plane of light aligned with the optical axis hits the conical mirror, it encounters a plane mirror and is reflected accordingly. However, if a plane of light perpendicular to the optical axis hits the cone it encounters a mirror circular in shape – this causes the light to diverge more than it would when hitting a plane. The end result of this phenomenon is that the concentric focal length differs from the radial one. In omnidirectional literature this effect is commonly referred to as defocus blur and is common to all catadioptric sensors. This effect seen in the test images of Figure 4-7 is demonstrated in Figure 4-8 from Hecht [12].

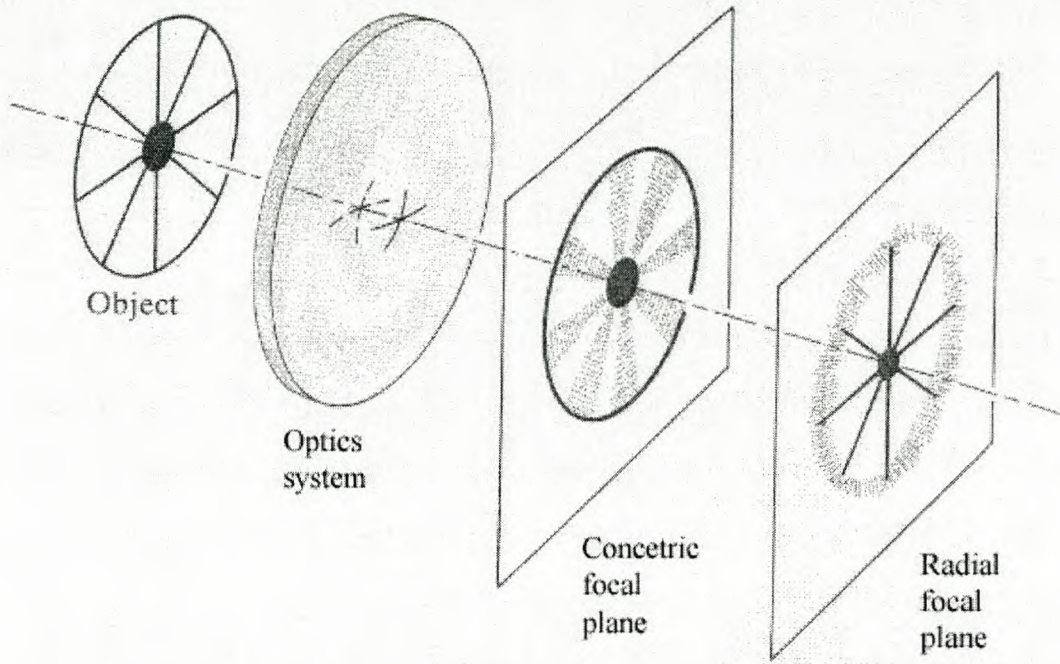


Figure 4-8 Images in the concentric and radial focal planes, modified from [12].

The question of how to correct this astigmatic defocus problem now presents itself, with two suggested solutions:

- Increase the depth of field
- Add a corrective lens or mirror

An optical system can be designed with a large depth of field to include both focal planes. The depth of field is the distance, measured along the optical axis, for which the image is sufficiently sharp, i.e. an image can have a depth of field of between two and three meters meaning that objects between two and three meters away are in focus. To tell if a scene is sufficiently sharp a point source is imaged and the blur region, known as the 'circle of confusion', is measured on the CMOS sensor. To be 'in focus' the circle of confusion should be less than the sensors pixel size – in this case $9.9\mu\text{m}$

$$d = \frac{s}{1 \pm ac \frac{s-f}{f^2}}$$

s — the subject distance (measured from the lens entrance pupil)

f — lens focal length

a — aperture (or F -stop), e.g., 2.8

c — the diameter of the acceptable circle of confusion.

A '+' in the denominator is used for the near, and a '-' for the far value. Negative results for the far limit (i.e., with a '-' in the denominator) mean that the focus reaches to infinity.

Equation 4-2 Focal distance formula [17].

One way to achieve a large depth of field is to stop down the aperture of the camera. The aperture limits the amount of light rays entering the camera, and this is proportional to the size of the circle of confusion. Therefore, decreasing the size of the aperture decreases the circle of confusion and increase the depth of field. The near and far distance values of depth of field can be calculated from Equation 4-2. However, narrowing the aperture has the adverse side effect of allowing less light to the sensor – which is already in short demand in the borehole environment. From Equation 4-2 it is also clear that a short focal length, wide angle, lens has the effect of increasing the depth of field.

The other method for solving the astigmatism problems is to create a corrective lens or mirror in the shape of a rotated cylindrical lens. The goal of the lens would be to move the two focal planes together. This is a similar idea to the glasses worn by people who have astigmatic eye problems.

4.3 Fisheye Lens

During testing of the conical mirror, the edge of the picture was found to capture the test grid pattern directly. These imaged grids were sharp and more useable than those reflected off the mirror. It was then decided to investigate a wide angle lens. The most extreme wide angle lens is called a fisheye lens. The name fish-eye was coined by R.W. Wood to refer to any lens capable of imaging the entire hemisphere in object space onto a finite circle in the focal plane. He chose this name because a fish looking upward at the surface of the water will see the whole sky imaged as a finite circle this way, [18].

An inexpensive lens (R180) was sourced from Eagle Electronics in Cape Town. It has the following specifications:

- Focal Length: 1.78 mm.
- Aperture: F3 (5 mm diameter).
- View Angle (Half): 90 - 108° (depending on sensor array size).
- Dimensions: 31 x 24.3 mm.
- Board lens mounting thread.

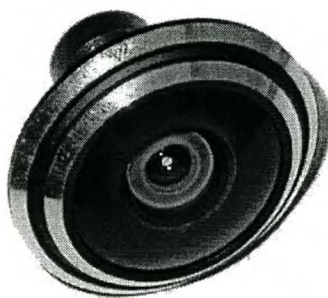


Figure 4-9 Fisheye lens.

Fisheye lenses are known to introduce distortion, but for imaging the inside of a cylindrical hole over a small distance, it should be possible to achieve high-quality pictures. This lens consists of an array of many internal lenses, each refracting the light to achieve the desired omnidirectional vision. An example of the internals of a fisheye lens is shown in Figure 4-10. Three different rays are also traced through the lenses to the image plane.

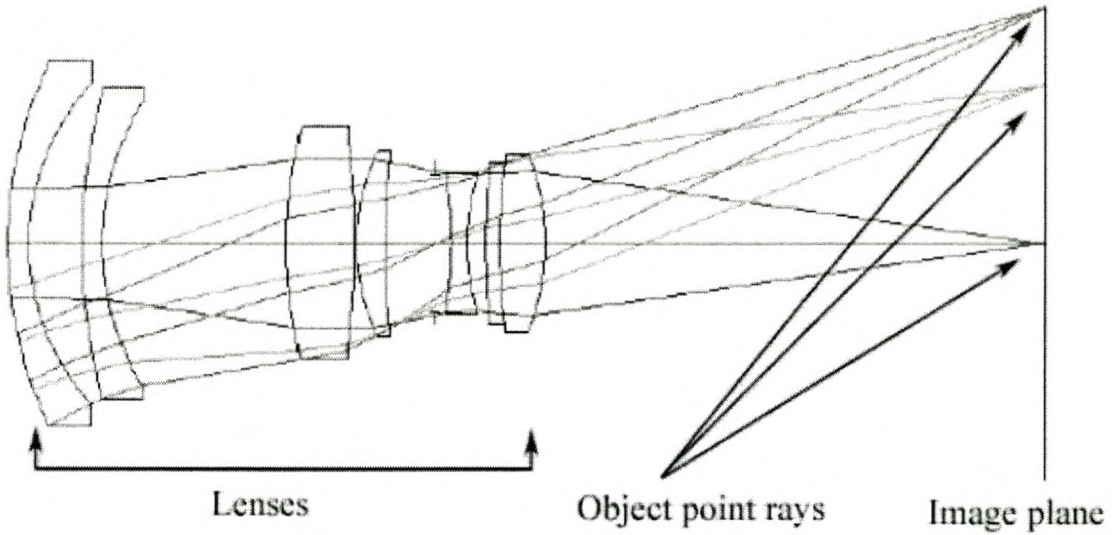


Figure 4-10 Fisheye lens internal optics [19].

Chapter 5 Firmware Design

The processing in the RockEye is controlled by an FPGA. Although it is not ideal for some of the complex interfacing and control protocols of the image sensor and flash card, it is well suited for quickly moving the large amount of picture data around. The VHDL¹⁶ firmware code used to program the FPGA was developed in the Xilinx ISE 5.1 environment, using ModelSim XE II for simulations. In VHDL hardware programming [20], tasks are completed by implementing logic based state machines. State machines are processes that have defined states that are changed depending on internal and external conditions. Various related processes are often grouped into a module. The compiled code is then downloaded onto the PROM chip and every time the board is powered up, the SRAM based FPGA is loaded with this code.

5.1 Firmware Overview

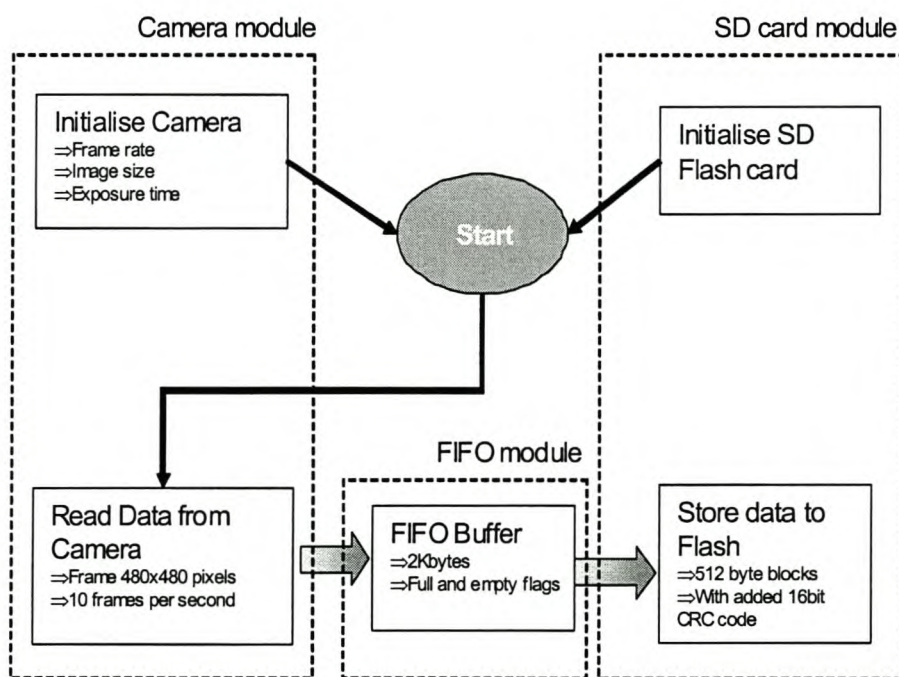


Figure 5-1 FPGA internal process overview showing internal modules.

¹⁶ VHDL is a compressed acronym and stands for Very High Speed Integrated Circuit Hardware Description Language.

Upon power up, the FPGA initializes the image sensor setting the picture size, exposure time and frame rate. Preliminary commands are sent to the SD Flash to get it into the correct state, ready to receive the write command. Moving a magnet close to the reed switch starts the image recording. The writing process involves reading digital pixel data in a row-by-row manner from the CMOS camera. Data is then written one byte at a time into an internal FIFO (first in first out) memory buffer. The SD card process reads out the data from this buffer at its own rate and writes to the flash memory card in a serial fashion. This entire process and the various VHDL modules are illustrated in Figure 5-1.

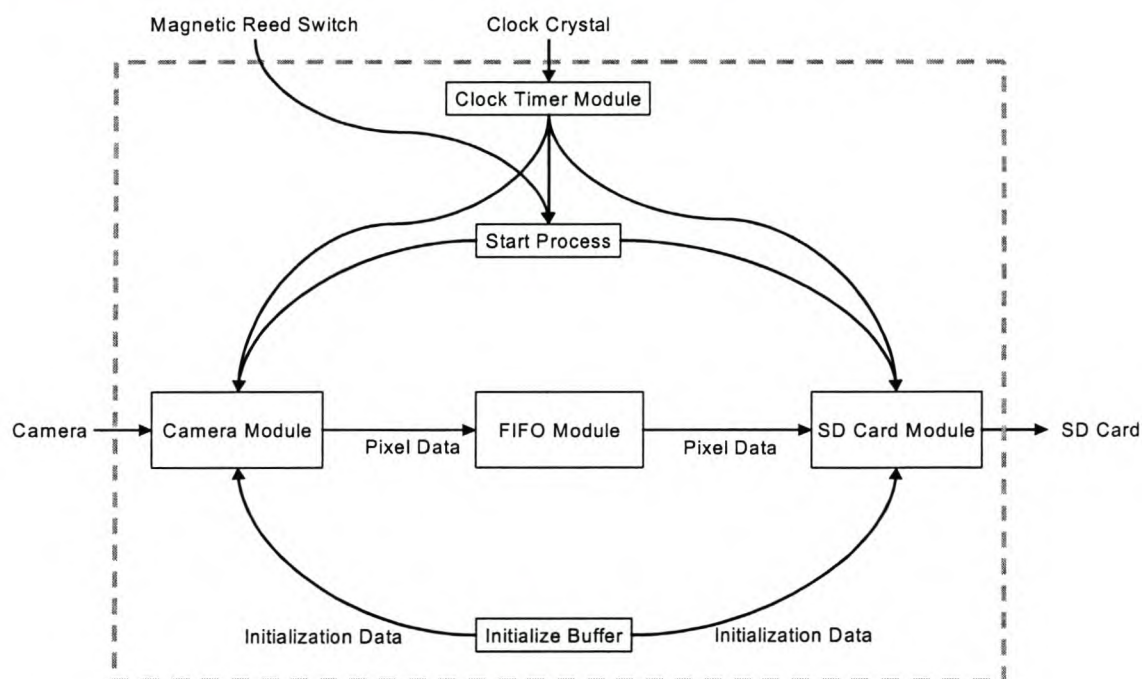


Figure 5-2 Firmware dataflow.

Figure 5-2 shows a simplified view of the general data flow within the system. Both the camera module and the SD card module get their initialization data from a common initialization buffer. Other external influences come from the 62.5MHz crystal, which goes through the clock timer module before being distributed to the various modules. The magnetic reed switch is connected to a start process that controls when the probe starts and stops logging pictures. The rest of this chapter deals with each of the VHDL modules, camera, SD card, FIFO and clock generation in more detail examining the various processes and program flow.

5.2 Camera Controller

The camera module has the job of controlling the Micron MT9V403 image sensor. This module consists of three sub-processes shown in Figure 5-3. The first simply gives a reset pulse to the sensor, which initiates internal ADC calibration and sets the sensor running. Next, the initialize process sets up the camera, before the read data process starts.

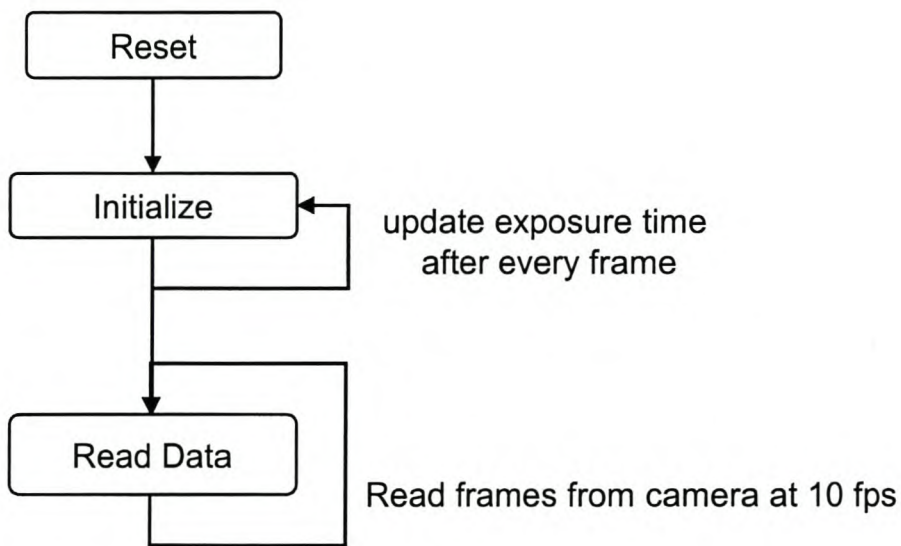


Figure 5-3 Camera module processes.

5.2.1 Initialize Process

The initialize process begins once the sensor has been reset. This process has the task of serially loading the internal registers of the MT9V403 with values specific for this application. These registers set variables such as the camera mode, start column, start row, ADC gain, exposure time, etc. The serial interface is based on the two wire I²C protocol. All the registers set are shown in Table 5-1. The frame rate for the sensor is set indirectly by adjusting applied clock frequency and then fine tuned by setting the number of horizontal and vertical blanks. Horizontal blanking (HB) and vertical blanking (VB) are essentially variable delays. The frame rate can be calculated using

Equation 5-1 and Equation 5-2, taking the values for HB and VB from Table 5-1. N is the number of rows, 480. The clock rate f_{sysclk} is 4MHz.

$$RT = (671 + HB) \times \frac{1}{f_{sysclk}}$$

Equation 5-1 Row time formula.

$$FT = (N + VB) \times RT$$

Equation 5-2 Frame time formula.

Register Number	Register Value Hex : (Dec)	Register Description
1	00 0B (11)	Start row
2	00 6E (110)	Start column
3	01 EB (491)	Stop row
4	02 4D (589)	Stop column
5	00 8E (142)	Number of horizontal blanking pixels (HB)
6	00 0A (10)	Number of vertical blanking pixels (VB)
9	00 64 (100)	Exposure time (in multiples of the row time)

Table 5-1 Camera register setup values.

The exposure time register value is in multiples of the row time, currently 208.6 μ s. With a minimum value of two and maximum of 255, the exposure can therefore vary between 417.2 μ s and 53ms. All these initial register values are set at compile time and stored as the initial values of one of the Xilinx's 512 byte memory blocks.

Once the initialize process is finished loading the register values it then goes into a loop continually updating only the exposure register after every frame of data has been read from the camera. If the picture is too dark the exposure value is increased, too light and it is decreased. The goal of the control loop is to achieve a mean value of 128 out of a maximum of 255 for the pixels. The mean value is calculated by summing the pixel values for the entire image and dividing by the number of pixels in

the image (230 400). However, in the FPGA it is easier to divide by multiples of two and the closest multiple is 2^{18} (262 144). Additionally, the image from the fisheye lens does not fill the corners of the image and they are always black with a value of zero. To compensate for both of these factors, the desired mean of the picture is set to 88 with a small dead band (84 to 92). Figure 5-4 shows this process.

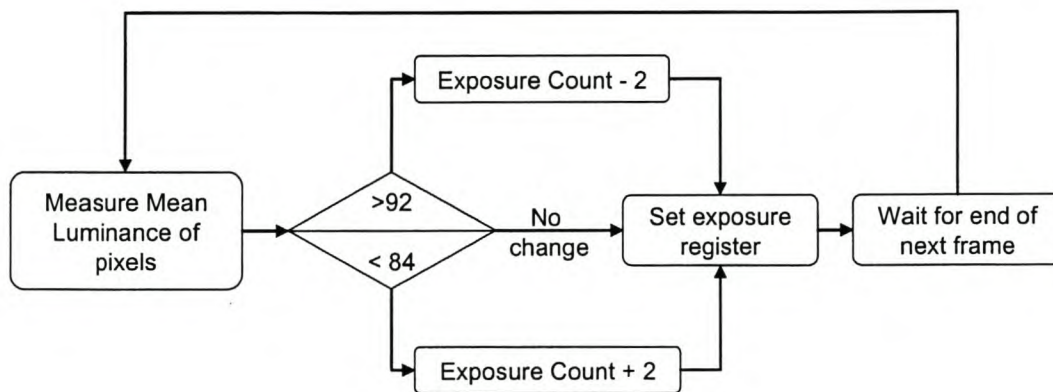


Figure 5-4 Exposure setting control loop.

A step response test, Figure 5-5, was conducted by running the camera indoors and then pointing it at a sunlit scene outdoors. The frame mean shoots up to 220 as the image saturates, but returns to normal as the exposure time decrease. The maximum time that it could take the control system to settle is 12.5 seconds, going from minimum to maximum exposure time.

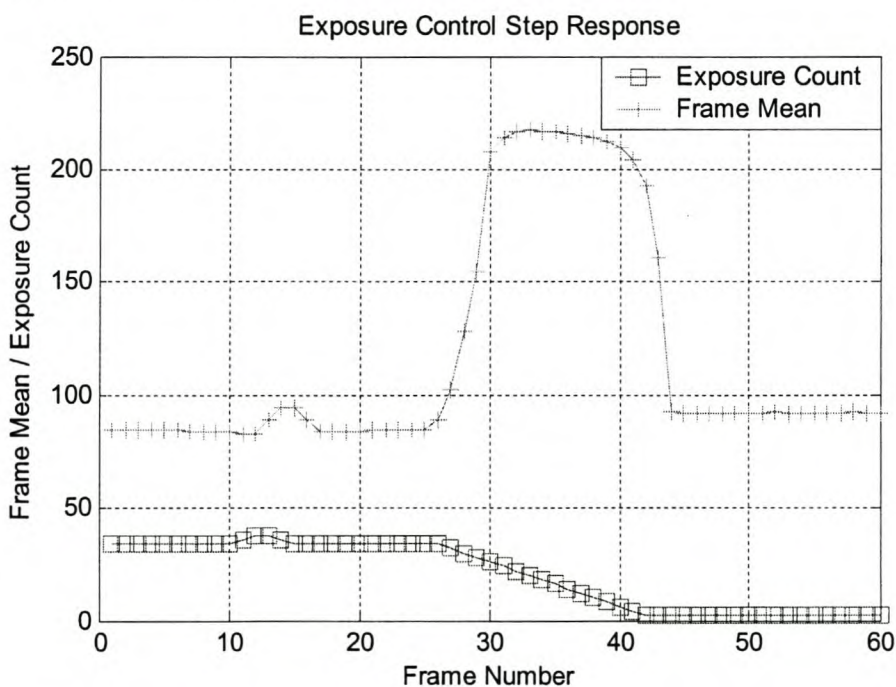


Figure 5-5 Step response for exposure control.

5.2.2 Read Data Process

The third process running in the camera module is responsible for reading in the pixel data from the camera, one frame at a time and writing it to the FIFO memory buffer. This process runs continually once the initialize process is complete. However, if the start signal has not been activated the process runs as normal but does not write data to the FIFO buffer. This ensures that when recording is started the exposure settings are already correct. Before every frame is written to memory a frame header is stored. The frame header contains useful information including:

1. Synchronisation code – 4 bytes.
2. Mean luminescence of previous frame – 1 byte.
3. Exposure time of current frame – 1 byte.
4. Frame number – 2 bytes.

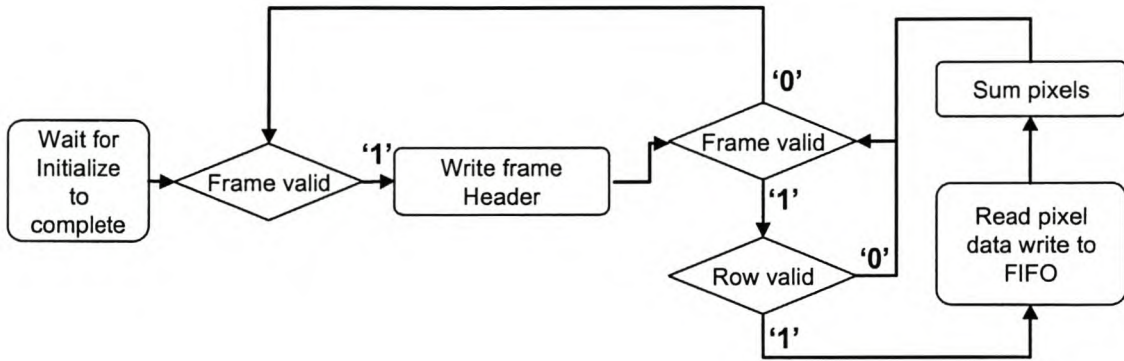


Figure 5-6 Read data process flow.

Figure 5-6 shows the internal states of the read data process. “Frame valid” and “row valid” are digital outputs from the camera module read into the FPGA. “Frame valid” goes high (‘1’) when frame data is available to be read out. “Row valid” goes high for every row of pixel data that is read out. These signals are illustrated graphically in Figure 5-7. While row valid and frame valid are high, on the falling edge of the system clock, pixel data is read from the camera. The pixels are also summed to calculate the mean for the entire frame – this value is then used in the exposure control loop.

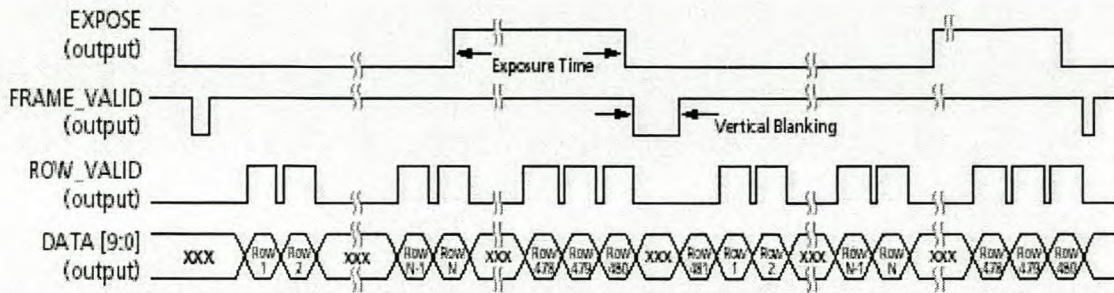


Figure 5-7 Frame and row synchronisation waveforms [8].

5.3 SD Flash Controller

The Secure Digital flash card has a six wire interface. Four of the wires are dedicated for data transfer; additionally there is a clock and a command line. For this application the speed of only one data wire is sufficient. The SD card VHDL module handles the initialization and writing of data to the flash card. To ensure compatibility amongst the various devices that uses SD flash cards, there is a fairly lengthy process involved in setting them up. The SD card manual is an extensive document and implementation of the protocol requires a good understanding of the majority of this document [10]. This subsection contains a simplified overview of the processes involved.

There are two processes involved in the SD card module. The first process controls the initialization of the card and all subsequent communications on the command line. The other process handles writing the image data from the FIFO memory buffer to the SD card on the data line.

Communication over the SD bus is based on commands sent to the card, and responses received from the card. There are two classes of commands, normal (CMD) and application specific (ACMD).

The card initially starts up in the idle state and takes a variable amount of time before it is ready to receive commands. During this time the card is repeatedly sent ACMD41 and the response is examined to see if the busy flag is set. Also contained in the response are the card's possible operation voltages. Once the busy flag has been cleared the card goes into the ready state. CMD 2 is then sent, requesting the card to send its card identification (CID) register. None of the CID information is actually used but it is part of the mandatory initialize procedure. CMD 3 then asks the SD card to publish a relative address; the reply is then used in the next step to select the card, CMD 7. Now the card is finally in the transfer state. The process waits here for the start sequence to be executed by the probe user. Once the internal start variable goes high, ACMD 23 is issued to pre-erase the entire card. This substantially speeds up the writing of multiple blocks. Next the multiple block write command, CMD 25, is issued. After receiving this command the SD card expects multiple blocks of 512 bytes to be sent to it until a stop transfer command, CMD 12, is issued. At this point the initialize process halts and calls the write block process. The write process writes a single block of data and then returns to the initialize process to check if the data has been received correctly. The stop command is issued either when the probe user terminates the image recording, causing the start variable to return to zero, or if an error is encountered while writing a block. This entire process is illustrated in Figure 5-8.

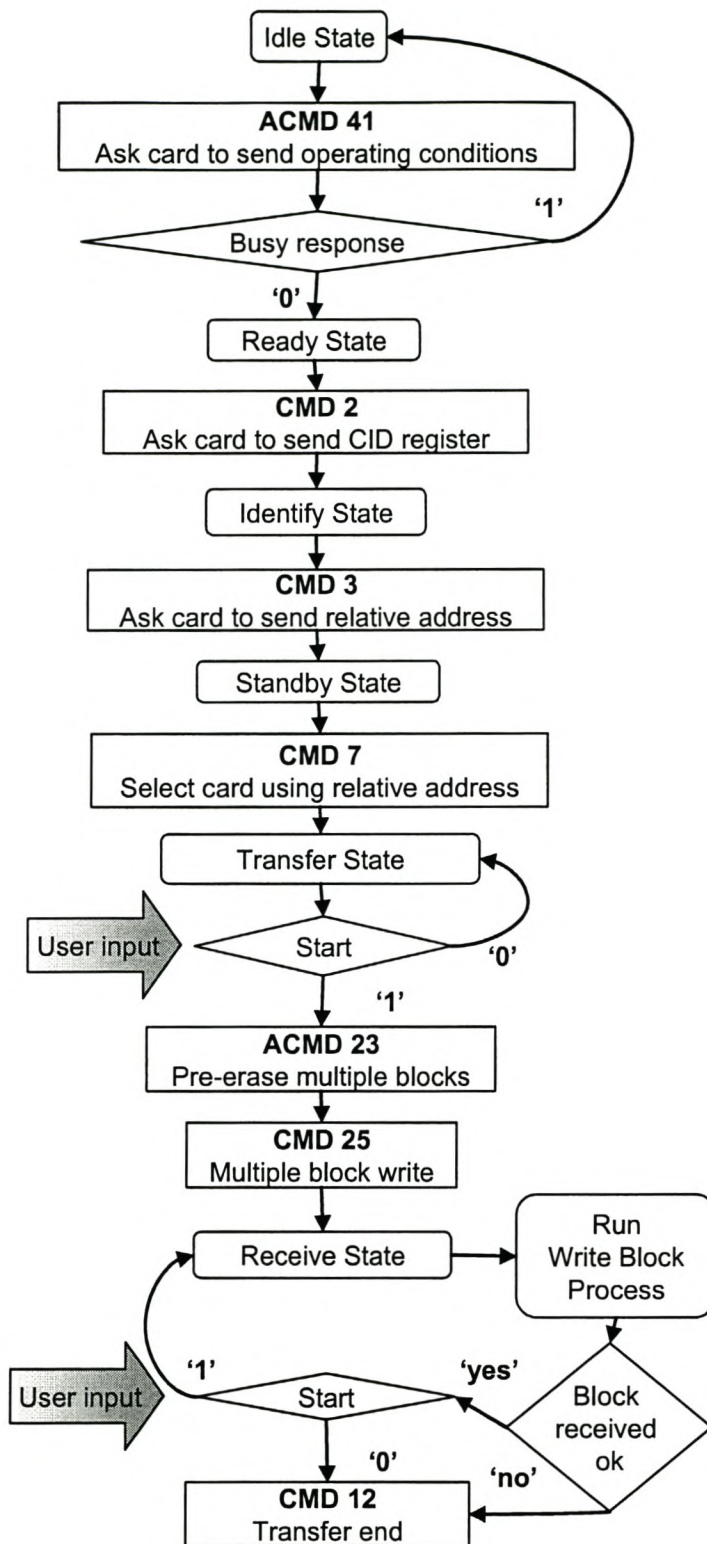


Figure 5-8 SD card module, initialize process.

5.3.1 Write Block Process

The write block process is run for every block that is transferred to the SD card. It is started from within the initialize process once the magnetic switch has been triggered. After every execution it returns to the initialize process. The write block process has the task of reading 512 bytes from the FIFO memory buffer, serializing them into a string of 4096 bits, appending a CRC code and sending the data to the flash card. The format of the block data packet is shown in Figure 5-9.

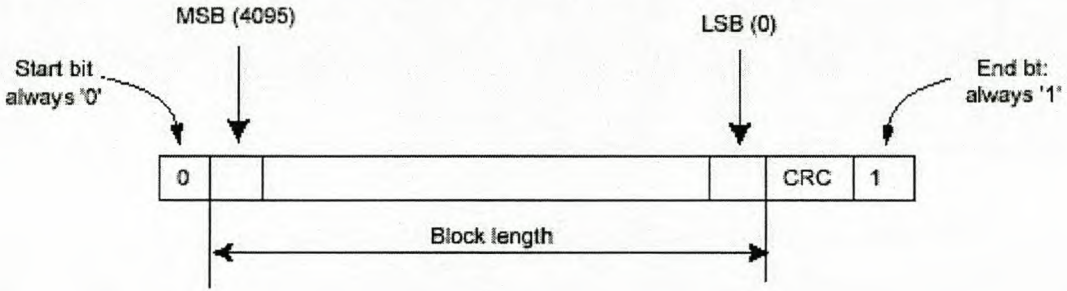


Figure 5-9 Block data packet format [10].

The SD card protocol requires that every block of data is followed by a 16-bit cyclical redundancy code (CRC) generated using the polynomial in Equation 5-3. The CRC ensures the data integrity between the FPGA and the SD card.

$$G(x) = x^{16} + x^{12} + x^5 + 1$$

Equation 5-3 16-bit CRC generator polynomial.

The CRC function is implemented as a shift register where data is shifted in at the left one bit of a time. In Figure 5-10, the \oplus symbol is an XOR block, and the rectangle (\square) a storage element within the shift register. Data is XORed into the shift register at various places corresponding to the CRC polynomial in Equation 5-3.

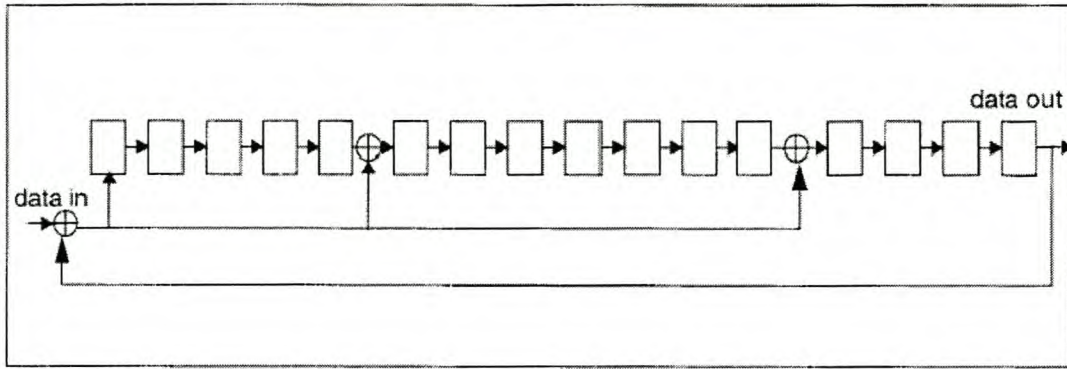


Figure 5-10 CRC 16-bit shift register [10].

It was imperative that the CRC code was generated correctly for the SD card to accept the image data. To get the CRC working, the VHDL code was first simulated in ModelSim. These simulated results were then compared to Simulink simulations created in MATLAB using the communication toolbox, shown in Figure 5-11. Using an oscilloscope, the Simulink and ModelSim simulations were then compared to the actual signal output from the FPGA and the correct implementation was achieved.

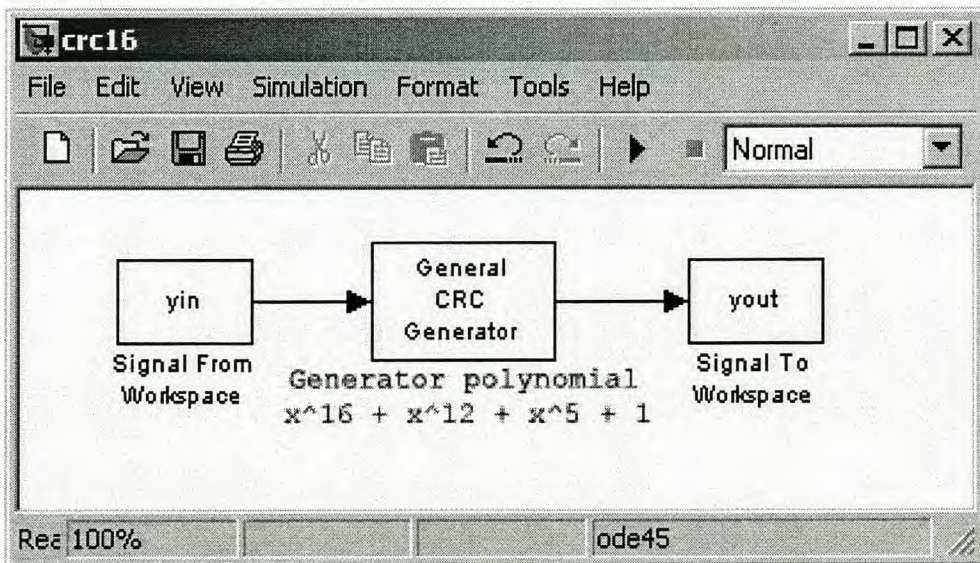


Figure 5-11 Simulink CRC generator simulation.

Figure 5-12 shows a flow diagram for the write process. Once started the process only begins sending data to the flash card when there are at least 512 bytes of data in the FIFO memory block. This ensures the process of writing a block runs smoothly and is not interrupted due to a lack of data. Bytes are read from the FIFO buffer and then the bits of each byte are sent out one at a time to the SD card. At the same time they are shifted through the CRC shift register. After a block of 512 bytes has been completed, the 16 bits of the CRC shift register are sent.

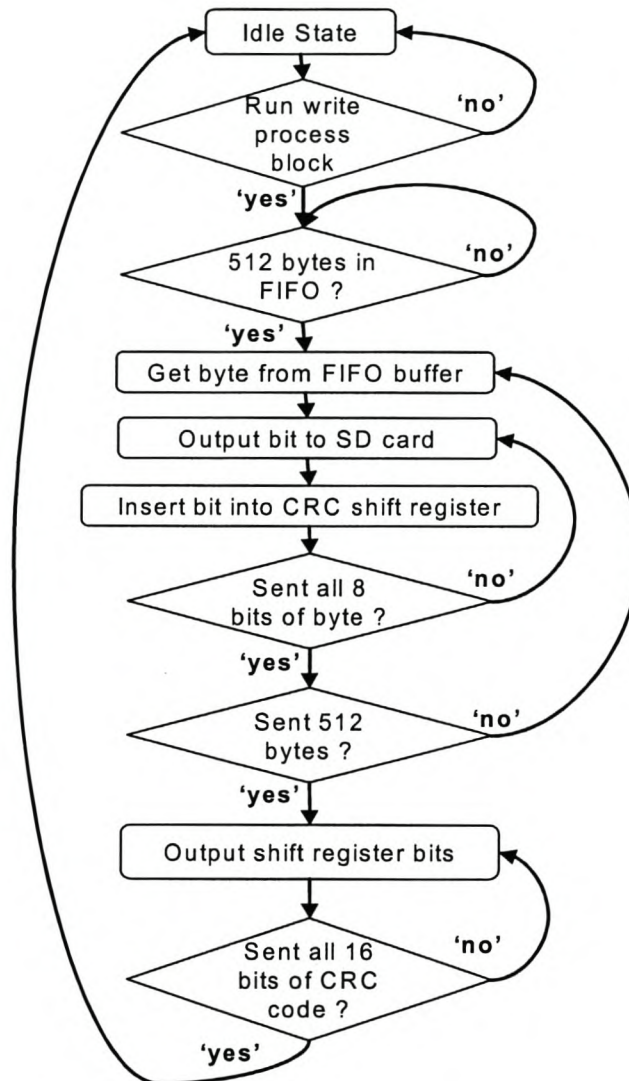


Figure 5-12 Write block process.

5.4 FIFO Memory Block

The FIFO memory module is a buffer to eliminate any problems between the rate of data output from the camera and the rate of data written to the SD flash card. This buffer is created from four 512 byte block rams inside the Xilinx FPGA, making up a total of 2048 bytes. The FIFO block is actually quite simple in operation. There is a read and a write address. The write address is incremented every time a byte is written into the buffer; similarly the read address is incremented when a byte is read. The address counters are 11 bits in length allowing addressing of all 2048 bytes. The most significant 2 bits of the address are used to decide which block ram to write to through a 2-to-4 decoder. The remaining 9 bits address the bytes within the separate 512 byte block rams. When the address counters reach 2048 the addresses automatically wrap around and continue writing to byte zero. There is additional logic to provide external signals for when the buffer is full, empty or contains more than 512 bytes. The four separate blocks, how they are linked, as well as the address decoding is shown in Figure 5-13.

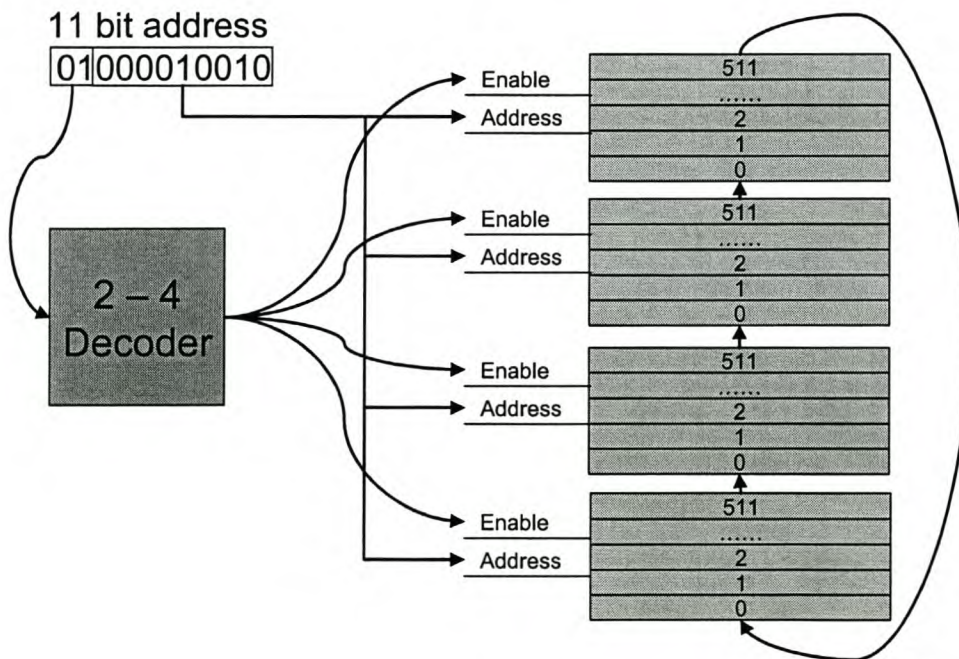


Figure 5-13 FIFO memory buffer address decoding.

5.5 Timer and Clock Generation

The test board that was used to develop the prototype RockEye has one external clock – a 62.5 MHz crystal. This design includes a number of modules, each requiring their own data rate and subsequently their own clock signal. Additionally several of the processes require a double rate control clock.

The double rate clock is necessary as some of the processes controlling the camera and SD card require events to occur on both the rising edge and falling edges of the system clock signal. The VHDL language does not allow for processes to be executed on both edges of the clock. Thus a work around has to be employed where the process is controlled by a clock signal at twice the frequency. This double rate clock now has a rising edge for both the edges of the system clock, shown in Figure 5-14.

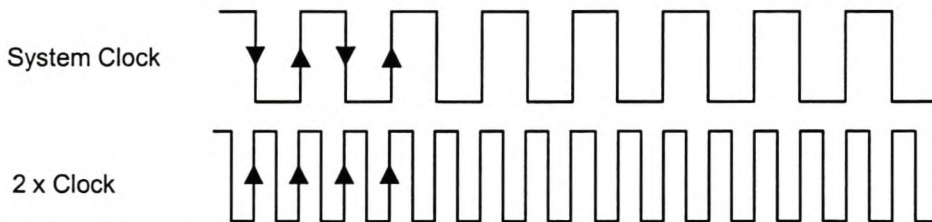


Figure 5-14 System clock and double rate clock.

The Xilinx FPGA has some very useful dedicated clock management blocks including delay lock loops and frequency dividers. A clock module was designed that makes use of the internal clock blocks as well as binary counters that act as clock dividers. It is generally accepted that creating ones own clock signals using logic on the FPGA is not a good digital design principle as glitches can occur on the signals causing errors that are hard to track down. However for this prototype design the chance of glitches was seen as an acceptable risk when the alternative was major hardware revisions. Table 5-2 shows the different frequency clocks used by each module. The generation of these clock rates is shown in Figure 5-15.

Camera module	SD card module	Start switch
4 MHz	40 MHz	1 kHz
60 kHz	20 MHz	
30 kHz		
1 kHz		

Table 5-2 Clock frequencies for different modules.

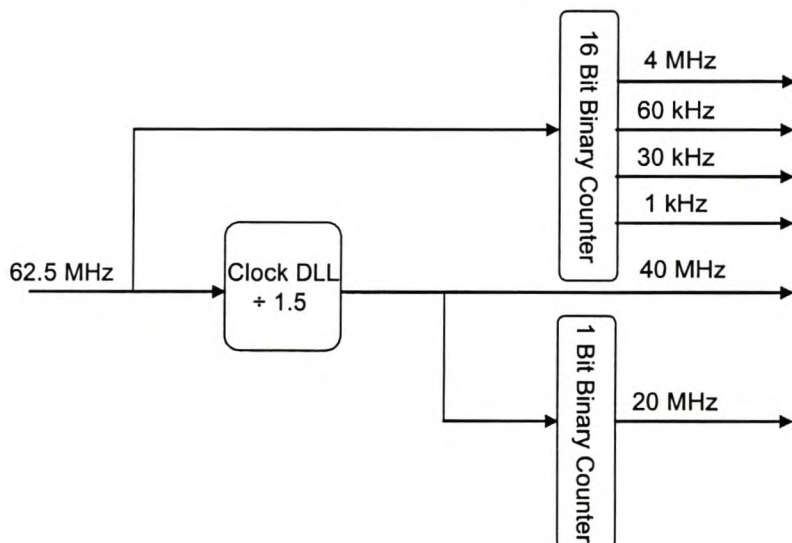


Figure 5-15 Clock generation.

Chapter 6 Image Processing

The previous two chapters describe how the firmware and hardware writes image data from the camera onto the removable flash card. This chapter centres on what happens to the data once the flash disk has been removed from the probe and downloaded onto a PC. There is a fair amount of processing involved in getting from the raw image data to a viewable virtual core that can be presented to a mine geologist.

The first section of the chapter describes the steps for transforming the raw pixel data to a viewable image. This image can then be processed using the techniques in Section 6.2 to create a strip view of the inside of the borehole. The distance into the borehole can then be calculated and the strip images stitched together by the theory presented in Section 6.3.

6.1 Bayer's Array to RGB, Methods and Implementation

The Micron image sensor consists of a group of light sensitive pixels. During manufacturing a colour array of red, green and blue filters are placed above the pixels enabling us to obtain a colour picture, illustrated in Figure 6-1.

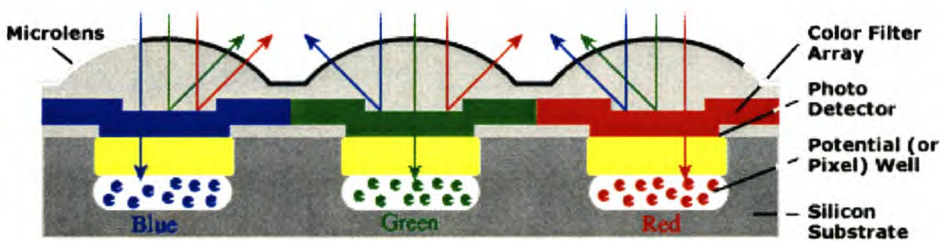


Figure 6-1 Pixel colour filters, image modified from [21].

The filter array used on this sensor is the Bayer's pattern¹⁷ shown in Figure 6-2. Alternate rows switch between green–red–green and blue–green–blue. This means there are twice as many green pixels as red or blue. The pattern was designed this way as the eye's frequency response is most sensitive to green light.

¹⁷ Named after Dr Bryce Bayer who worked for KODAK.

4	B	G	B	G
3	G	R	G	R
2	B	G	B	G
1	G	R	G	R
	1	2	3	4

Figure 6-2 Bayer’s pattern.

The data that is read out of the image sensor and stored on the flash card is in Bayer’s format. The data needs to be processed using interpolation to generate a red, green, and blue (RGB) value for each pixel location. This process is done using code written in MATLAB. The raw data is read in, the frame header removed and an interpolation algorithm implemented. There are various algorithms available as described in Ramanath, Snyder and Bilbro’s article on demosaicing algorithms [22]. Different algorithms perform better for different types of pictures – images with sharp high contrast lines are the most challenging. However, the difference between the best and worst implementations is minor and for this prototype application a simple average algorithm was chosen. Figure 6-3 shows how this algorithm works. If the RGB values are needed for the middle pixel, the red value is its own value (18); green is the mean of (12, 20, 26, and 10) which is 17; blue is the mean of (4, 5, 3, and 8) which is 5. This algorithm is then repeated for every pixel in the image. Instead of the mean, the median can be used – this is supposedly less disturbed by noise but the visual change between the two is not noticeable. The resulting image can now be displayed, saved or combined with other images to form a movie clip. Further image processing as described in 6.2 can now take place.

B = 4	G = 12	B = 5
G = 26	R = 18 G = 17 B = 5	G = 20
B = 3	G = 10	B = 8

Figure 6-3 Interpolation implementation example.

6.2 Polar to Cartesian Conversion

The pictures taken through the fisheye lens, or of the cone mirror, are in the form of a forward looking square picture with the useful section of the image in an annular ring. This ring needs to be unwrapped into straight strips that can be patched together to form a complete virtual core.

One way to unwrap the image is to take the original image and for every x and y pixel coordinate work out the polar coordinates, in r and θ . Then plot r versus θ in a normal Cartesian coordinate system. Values for θ and r are calculated using Equation 6-1. Where nx and ny are the original coordinates centred at the middle of the image; k is a constant that determines the final image width; $atan2()$ is a MATLAB function similar to $arctan$ but giving a full four quadrant result ($-\pi$ to π). This process and the results of its implementation on a test image is shown as method A in Figure 6-4. However, as can be seen from the resulting unwrapped image a rather patchy image is created. This is due to scaling and rounding errors resulting in missing pixels that will have to be interpolated.

$$r = \sqrt{nx^2 + ny^2}$$

$$\theta = k \times a \tan 2(ny, nx)$$

Equation 6-1 Rectangular to polar transformation.

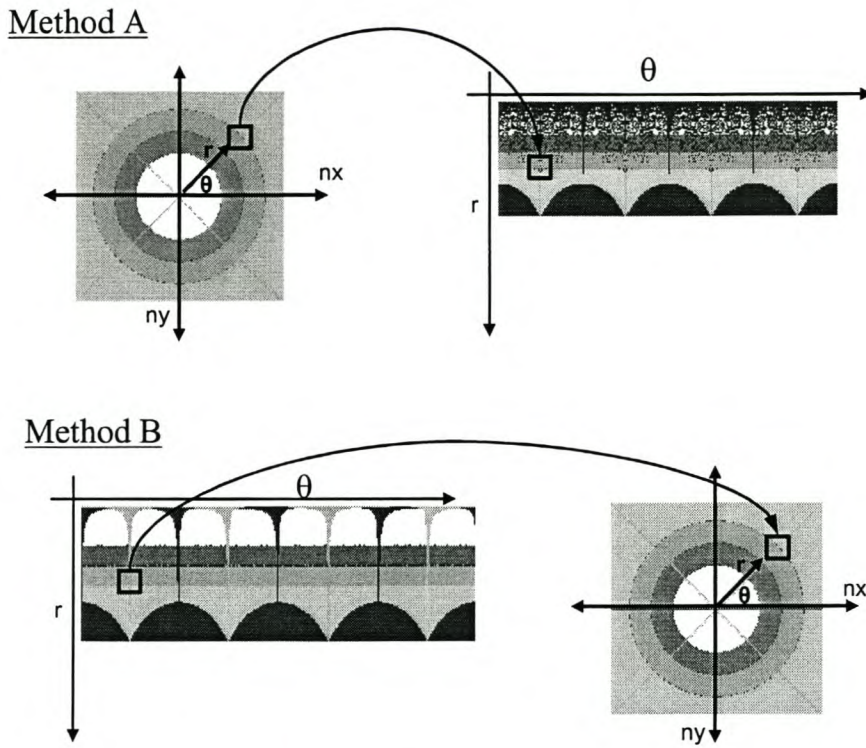


Figure 6-4 Two methods of unwrapping the annular ring.

A solution to the problems of method A is to approach this coordinate transformation in reverse, shown in Figure 6-4 as method B. Instead of taking the original pixels and placing them on the unwrapped image, take the unwrapped (r, θ) image and for every set of coordinates calculate where they map back onto the original image. Then copy the pixel values from this location back to the (r, θ) image. This process forms a complete image with no interpolation necessary. Equation 6-2 is then used for this transformation.

$$nx = r \cos\left(2\pi \frac{\theta}{\theta_{\max}} + \frac{\pi}{2}\right)$$

$$ny = r \sin\left(2\pi \frac{\theta}{\theta_{\max}} + \frac{\pi}{2}\right)$$

Equation 6-2 Polar to rectangular transformation.

The next refinement for this process is to work on the sub-pixel level and consider the decimal point, a technique called anti-aliasing. For example if we are looking for a pixel with x, y coordinates of (20.75, 10.2) rather than rounding to the nearest integer value – take an average of pixels (20, 10), (20, 11), (21, 10) and (21, 11). These pixels are then weighted according to the original fraction of a pixel i.e. pixel (20, 11) is weighted 0.25 times 0.80 giving 20%. Weighting is calculated for all four pixels, meaning that every pixel in the unwrapped image is the result of a weighted average of four original pixels. This produces a smoother, more accurate image at the end of the process. Figure 6-5 shows this graphically where the grey square is the exact requested coordinates (20.75, 10.2). Figure 6-6 shows an example of the effect of this anti-aliasing process on the resultant picture – the lines are smoother without the jagged appearance.

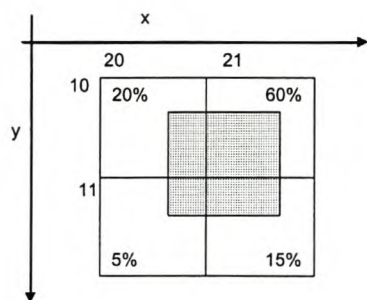


Figure 6-5 Sub-pixel anti-aliasing.

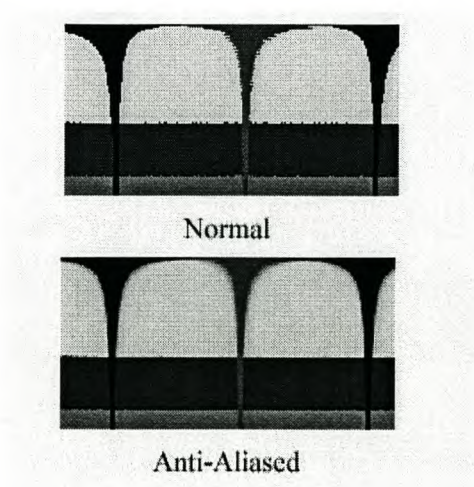


Figure 6-6 Effect of anti-aliasing on unwrapped test image.

6.3 Correlation Based Merge and Distance Calculation

The RockEye prototype system takes pictures at a constant rate of 10 fps. These pictures are then unwrapped using the algorithm developed in Section 6.2. The images then have to be stitched together at the correct position to form a seamless virtual core. If the optics of the system are analysed, a coefficient of pixels per millimetre can be calculated and the core can then be accurately logged against distance.

The process of working out when to stitch two unwrapped frames together works as follows. A row from the current frame is taken and it is correlated with every row of the next frame. The correlation formula (Equation 6-3) determines statistically how alike two vectors are, with a normalised maximum value of one. The maximum value of the correlation corresponds to the position at which the two frames should be stitched together.

$$r = \frac{\sum_m \sum_n (A_{mn} - \bar{A})(B_{mn} - \bar{B})}{\sqrt{\left(\sum_m \sum_n (A_{mn} - \bar{A})^2\right) \left(\sum_m \sum_n (B_{mn} - \bar{B})^2\right)}}$$

where $\bar{A} = \text{mean2}(A)$, and $\bar{B} = \text{mean2}(B)$.

Equation 6-3 Correlation formula used in MATLAB¹⁸.

¹⁸ Formula from MATLAB help file.

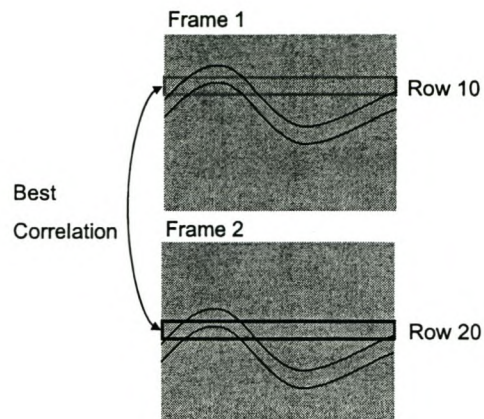


Figure 6-7 Example of the correlation process.

Figure 6-7 gives an illustration of correlating procedure. The sinusoidal shape in the image is a rock feature that is displaced further down the image in frame 2 than in frame 1. In this example it was found that row 10 of frame 1 correlates best with row 20 of frame 2 – meaning that between frames the probe has been displaced 10 rows, ± 2 mm. The two frames would then be stitched together at this point. This entire process would then continue again for frame 3 until a virtual core has been produced for the entire borehole.

Chapter 7 Testing and Results

This chapter begins by describing the packaging of this design into a robust probe that can be tested. The development of the various lighting systems is then described in Section 7.2. Camera internal gain tests were conducted and are explained in Section 7.3. Test borehole images are shown in Section 7.4. Section 7.5 details a brief resolution test and Section 7.6 a water filled borehole test. Rock borehole images and the post processing thereof are graphically displayed in Section 7.7. The power requirements and system cost analysis form the last two sections of this chapter.

7.1 Prototype Packaging

In order to test the entire system the electronics were mounted on a machined aluminium base and packaged inside a 40 mm clear Perspex tube. The base houses a pack of six NiCad rechargeable batteries supplying 7.2V with an energy rating of 2000 mAh. The ends of the tube are closed with machined PVC plugs including rubber O-rings to make the probe watertight. Plastic strips are attached onto the exterior of the pipe with zip ties. When pushed together they centre the device in the borehole, ensuring a non-distorted picture. The probe is shown in Figure 7-1.

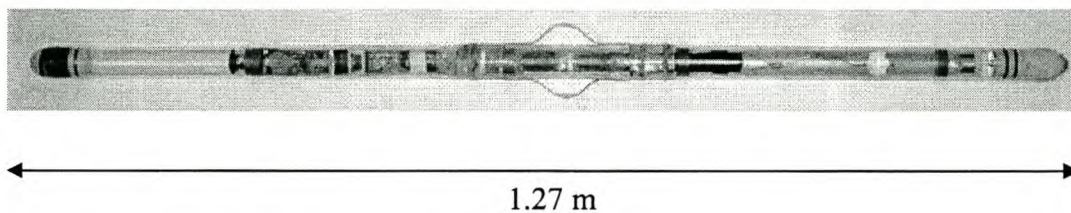


Figure 7-1 Packaged probe.

This packaging was tested at the Finsch diamond mine, near Kimberley. The probe was deployed down an almost vertical water filled hole to a depth of 10 m and it remained watertight. The plastic spacers were found too be brittle and bend too easily.

7.2 Lighting Modifications

Through the development of the probe, three different LED lighting arrangements were tested. They are shown in Figure 7-2. From the left of the figure, the first two configurations were found not to be bright enough. The second one was tested at the Finsch diamond mine with disappointing results. The problem with this configuration was that the four LEDs were mounted at an angle behind the fisheye lens and the rim of the fisheye blocked the light from reaching the rock wall. The latest setup (far right) is mounted around the outside of the fisheye lens. For this to be possible the rim of the fisheye had to be machined to reduce the diameter of the aluminium casing from 31 to 29 mm. Eight LEDs are included in this setup, which doubles the amount of available light. For the trials in the rock borehole in Section 7.7, the average exposure time was 10 ms, where with the previous 4 LED setup it had been 53 ms.

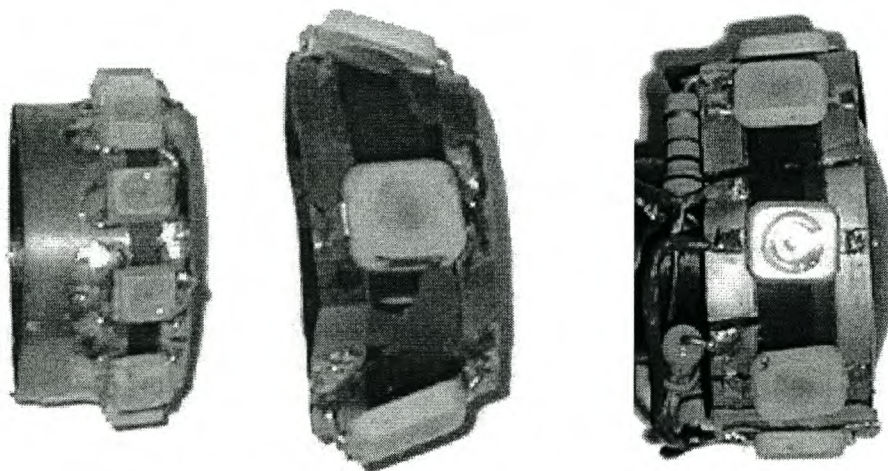


Figure 7-2 Lighting evolutions (current setup shown on the right).

7.3 CMOS Sensor Gain Variation Test

There are three ways to vary the brightness of a photograph: change the lighting; increase or decrease the exposure time; or vary the pixel gain. The pixel gain is a programmable value set through the image sensor's internal registers. Varying the internal registers affects the gain on the analogue signal path before it is read into the ADC, labelled as PGA in Figure 7-3. The default value of this gain is 2 but it can be changed from 0.5 to 18.

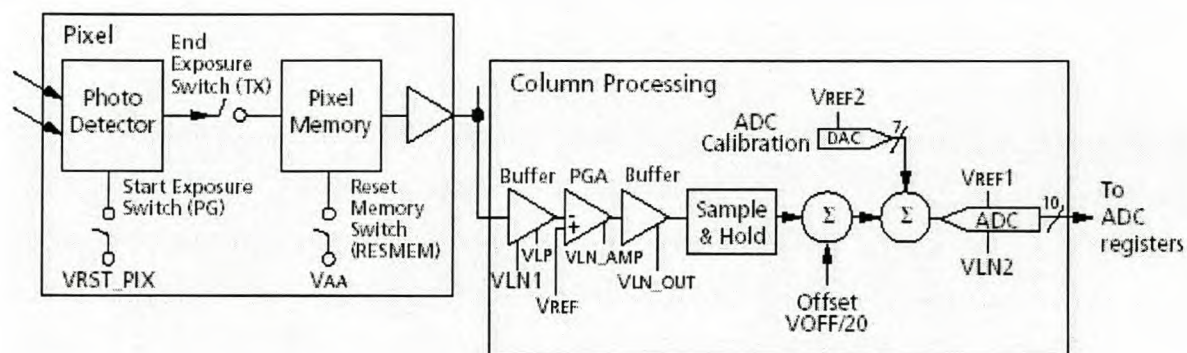


Figure 7-3 Image sensor analogue signal path [8].

For this test, the camera was mounted in a stationary position and eleven pictures were taken for four different gain settings (1, 2, 4 and 10). Figure 7-4 shows how the exposure time varies as the gain is changed. The internal control loop designed in the VHDL camera firmware strives to achieve a mean actual luminescence of between 92 and 102. This was achieved for gain values of 2, 4 and 10. When the gain was set to 1 the exposure time increased to the maximum allowed value corresponding to 53 ms and then the mean luminescence was still below the desired levels. Looking at the relationship between gain and exposure time with only a few data points measured, it is hard to tell but it looks like an inverse (x^{-1}) relation.

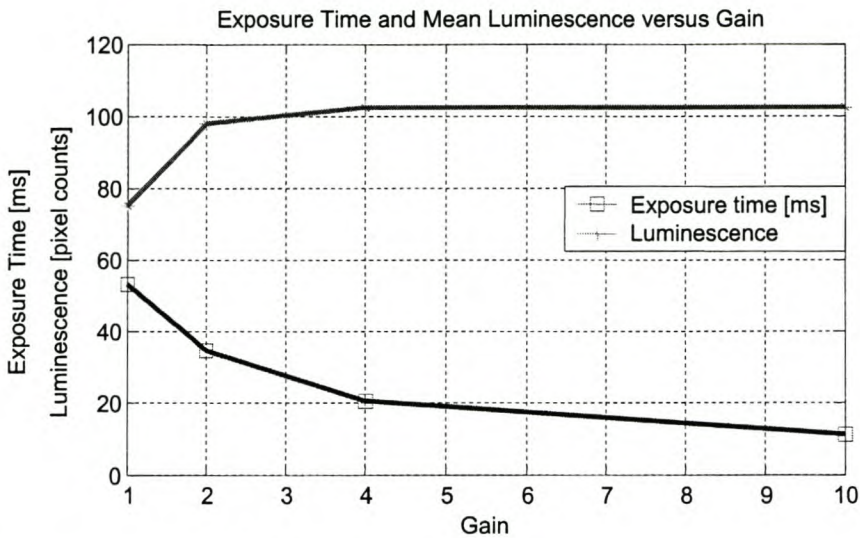


Figure 7-4 Graph showing variation of exposure time versus gain.

The main reason for doing these gain variation tests was to check the effect that changing the gain has on the noise present in the images. As seen in Figure 7-6, it is clear that there is an increase in noise as the gain is raised above two. The noise is seen as horizontal lines imposed upon the images. On close inspection the image with the gain set to one also displays more noise than with the default value of two. Quantitatively this effect was confirmed by calculating a signal to noise ratio (SNR) type merit number for each of the gain settings. The SNR for each gain setting was calculated by first subtracting successive pictures from each other. The difference between these pictures was then taken to be the noise image, as in Equation 7-1. The mean of the entire image was then divided by the mean of the absolute value of the noise image. The SNR is then plotted in Figure 7-5 against the various gains. The results here correspond well to the visual inferences made by looking at the pictures in Figure 7-6.

$$SNR = \frac{\text{mean}(image)}{\text{mean}(abs(\text{noise image}))}$$

Equation 7-1 Signal to noise ratio formula.

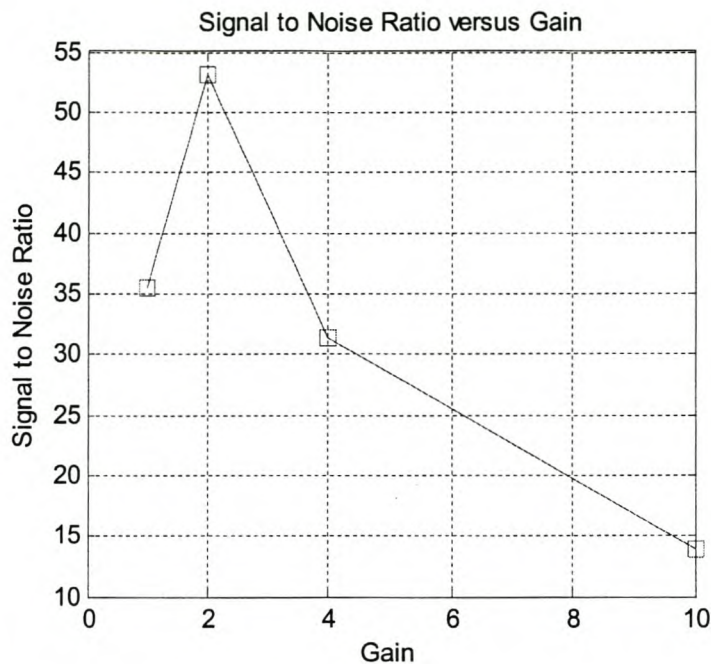


Figure 7-5 Graph showing the change in SNR with gain.

From these results it is possible to infer that there may be two sources of noise within the system. There is noise, of a constant level, that becomes more evident as the gain is increased and correspondingly the magnitude of the actual pixel signal decreases. There is also noise that decreases with gain. This could be as a result of the amplifier. Programmable gain amplifiers often work by switching in resistor networks to decrease the gain. This causes most of the noise to be present when the gain is lowest as each additional resistor that is added in creates thermal noise. The sum of the two noise sources results in the effect shown Figure 7-5 – where a gain of two gives the lowest noise. A portion of the noise looks synchronous rather than random. Better design of the camera PCB may decrease these noise levels.



Gain = 1



Gain = 2



Gain = 4



Gain = 10

Figure 7-6 Noise versus gain pictures.

To conclude this investigation into varying the gain, instead of there being three ways to vary the brightness of an image, there are only two, exposure and lighting – the gain setting should be left at its default value of two unless the user is prepared to accept a degraded picture.

7.4 Test Borehole Results

Using the test borehole setup shown in Figure 4-6, the pictures in Figure 7-7 and Figure 7-8 were taken by the conical mirror and fisheye lens respectively. A grid pattern was pasted inside the test borehole for the following tests.

7.4.1 Conical Mirror



Figure 7-7 Conic mirror in test borehole using 8 mm lens.

This picture was the best image taken using the RockEye system incorporating the conical mirror. The astigmatic effects described in Section 4.2 are prevalent here with only the concentric rings in focus. Further investigations into getting a fully focused image were conducted by Robin Starke [16]. Starke used four different lenses (2.97, 6, 8, and 12 mm) and it was still not possible to achieve a well focused image.

7.4.2 Fisheye Lens

The fisheye lens performed better than the conical mirror lens combination. Figure 7-8 is an image taken using the test borehole setup. The visible circle represents a 180° degree viewing angle. At the edges the image is slightly blurred and not useable. A little way in, the picture is clear and useable. The depth of field is good due to the short focal length (1.78 mm) and relatively small aperture of 5mm (F3.0).

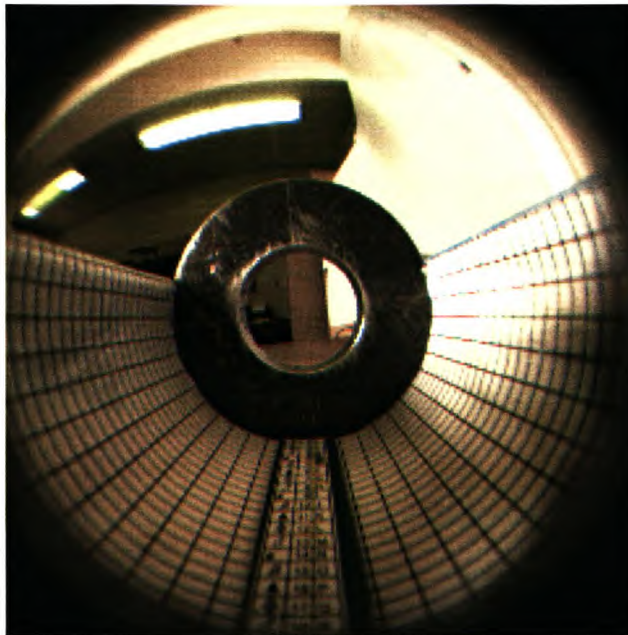


Figure 7-8 Picture of the test borehole grid pattern using fisheye lens.

Figure 7-8 is then processed by the polar to Cartesian coordinate transform software that was explained and developed in Section 6.2. The unwrapped image is shown in Figure 7-9. The software works well and the grid pattern is only minimally distorted compared to the original grid. The bottom of the image has better resolution as it was mapped onto the outside of the CMOS image sensor. The lines on the grid paper are 0.2 mm wide, they are clearly visible and occupy 2 to 3 pixels in this 66 mm diameter “borehole”. The usable Section is at least 70 pixels high which maps to 13 mm on the test borehole. The resolution is limited by the vertical compression, which shrinks the grid lines towards the top of the image. This is to be expected with a lens system as opposed to a catadioptric setup. Imagine looking along a borehole – it would not be possible to see very far into it.

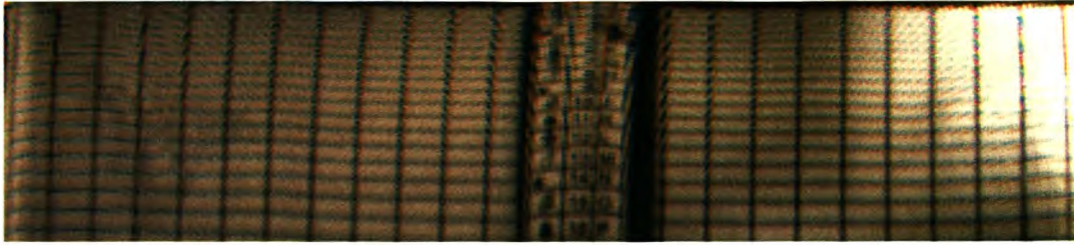


Figure 7-9 Unwrapped test grid.

The unwrap process was modified to combat the vertical compression shown in Figure 7-9. By manually counting the number of pixels between grid lines, which are spaced at 2.25 mm intervals, a relationship between pixels and distance on the borehole wall can be determined. Using the least squares approximation method a quadratic polynomial can be calculated that fits the measured data points over a narrow region. The measured data and fitted quadratic polynomial are shown in Figure 7-10. The polynomial equation is then used in the MATLAB unwrap algorithm to create geometrically correct images.

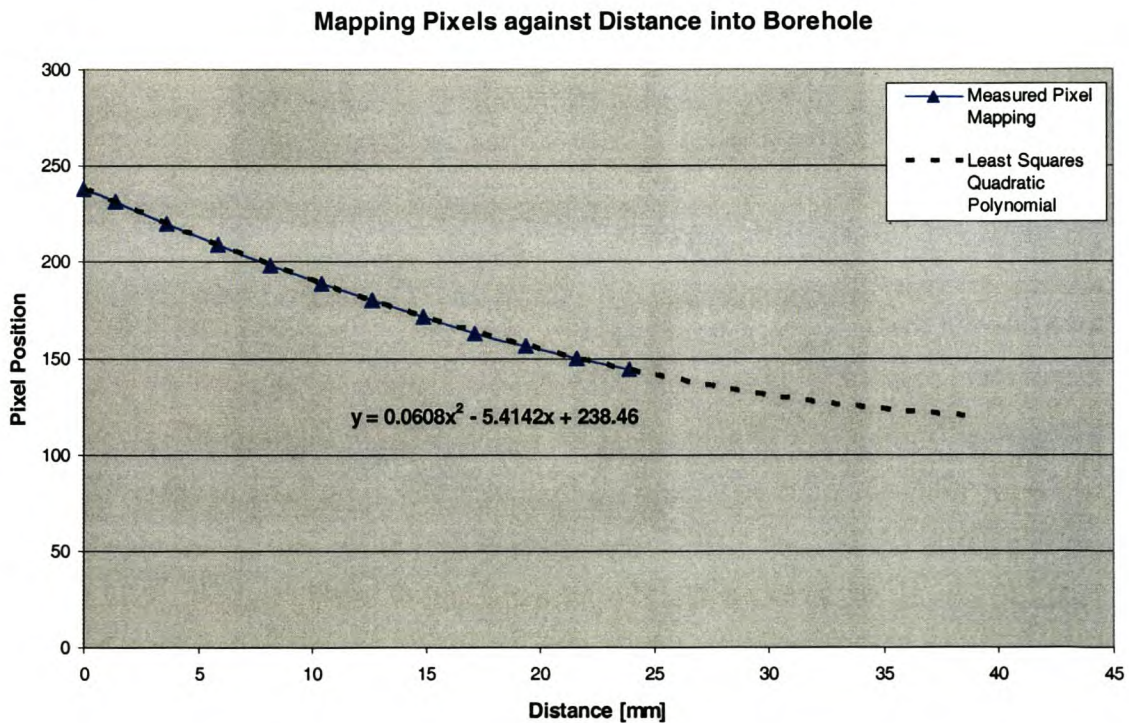


Figure 7-10 Relationship between pixel position and borehole distance.

The geometrically correct unwrapped image of the test grid is shown in Figure 7-11. This image is plotted at a constant resolution of 0.2 mm per pixel in both directions. Now, instead of compressing the lines at the top of the image, the lines become blurred where the resolution is limited. However, the lower half of the image is sharp and geometrically correct.

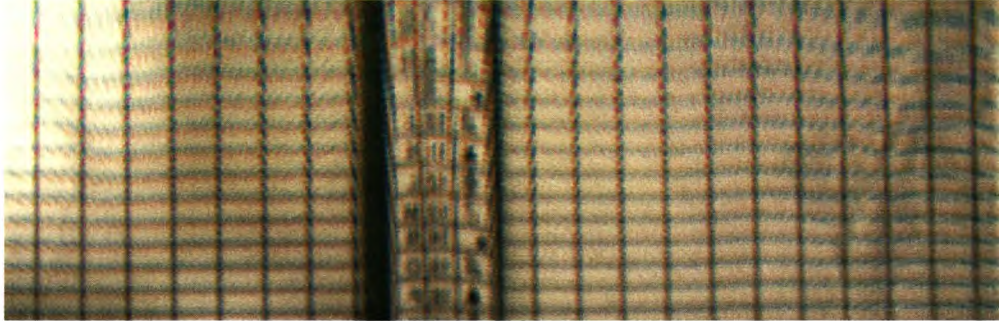


Figure 7-11 Geometrically correct unwrapped test grid.

7.5 Resolution Test Chart

A United States Air Force resolution chart from Edmund Optics¹² was used to test the resolution of the system. The resolution test chart was placed inside the 66 mm test borehole and imaged with the fisheye lens. The test chart has multiple groups, each containing three horizontal and three vertical lines. As these groups get progressively smaller the resolution is taken to be the limit at which it is not possible to discern two adjacent lines. For this system, the top right line group of Figure 7-12 is the limit. In this group the lines are 0.5 mm wide, separated by a gap of 0.5 mm. The initially specified resolution requirement was that the system should be able to discern features of width 0.5 mm in a 48 mm borehole. This system meets and exceeds the desired resolution as the test borehole is wider than the specified 48 mm one.

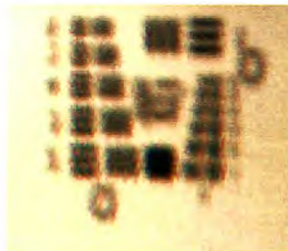


Figure 7-12 Resolution test chart image.

7.6 Water Borehole Test

One of the initial specifications was that the probe should work in water and air filled boreholes. A water filled test borehole was setup to ascertain how the camera's focus and image quality is affected by water. A 66 mm PVC tube was used as a test borehole. It contained the laminated test image, shown in Figure 7-13. The probe was placed in the borehole and water was added. Images were captured in the dry hole (Figure 7-14) and the water filled hole (Figure 7-15).

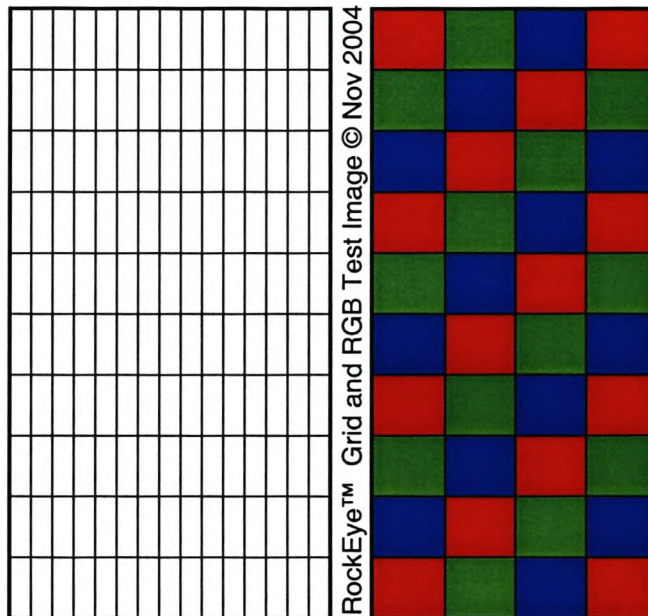


Figure 7-13 Water borehole test image.

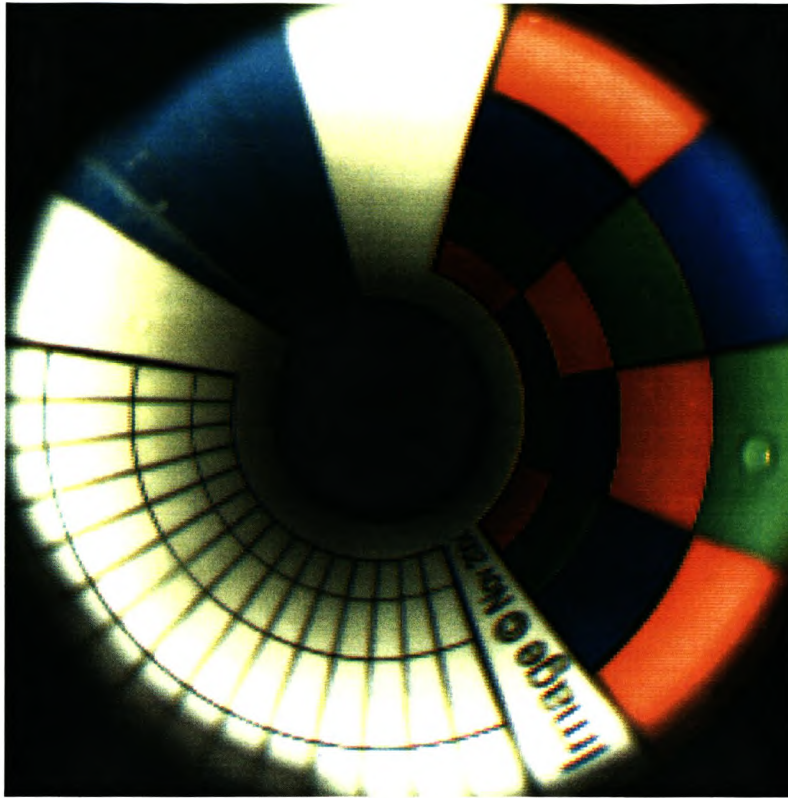


Figure 7-14 Dry test borehole.

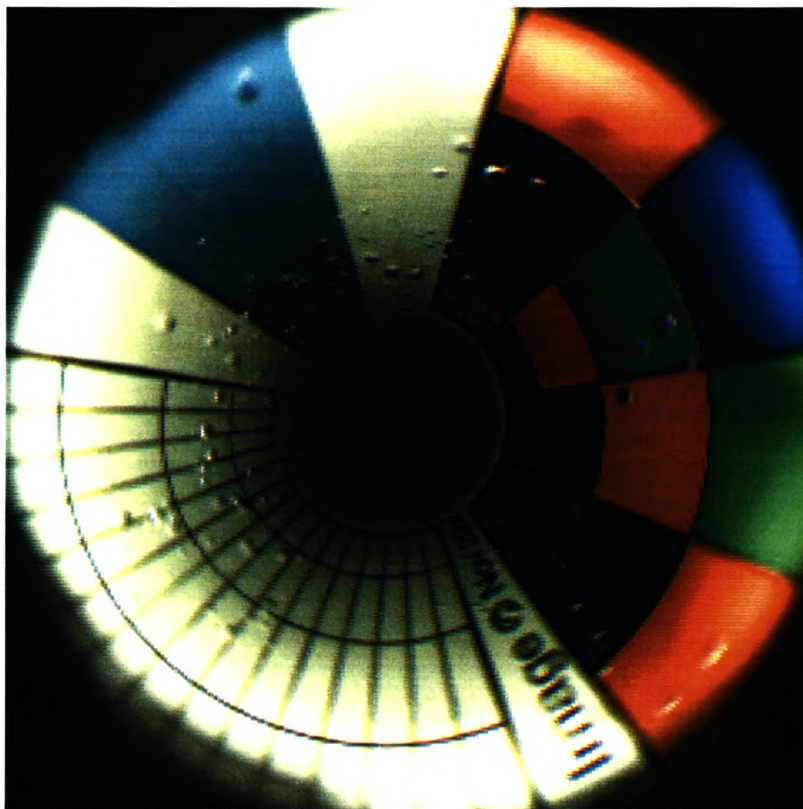


Figure 7-15 Water filled test borehole.

Apart from the bubbles in the water test, the images are sharp and well focused in both instances. The water changes the optics of the system. However, the extremely high depth of field of the fisheye enables both cases to be imaged clearly. The light rays are refracted by the interface between the air in the probe, and the water in the borehole. The angle that the ray is refracted is calculated using Snell's Law, Equation 7-2, with the relative refractive index (n) of water equal to 1.33. The optical setup is shown in Figure 7-16, where D is a position on the wall in a dry borehole and W the corresponding position in a wet borehole. The effect of the refraction is that it is possible to see further down a dry borehole than a water filled one.

$$\sin(i) = n \sin(r)$$

Equation 7-2 Snell's Law [23].

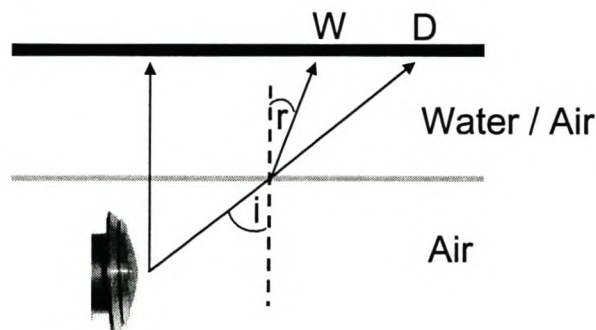


Figure 7-16 Optics in air and water.

7.7 Rock Borehole Results

The borehole radar group has a block of granite with five differently sized holes drilled into it, ranging in diameter from 40 to 113 mm. This block of rock¹⁹ provides an excellent opportunity to test the RockEye in a borehole environment.

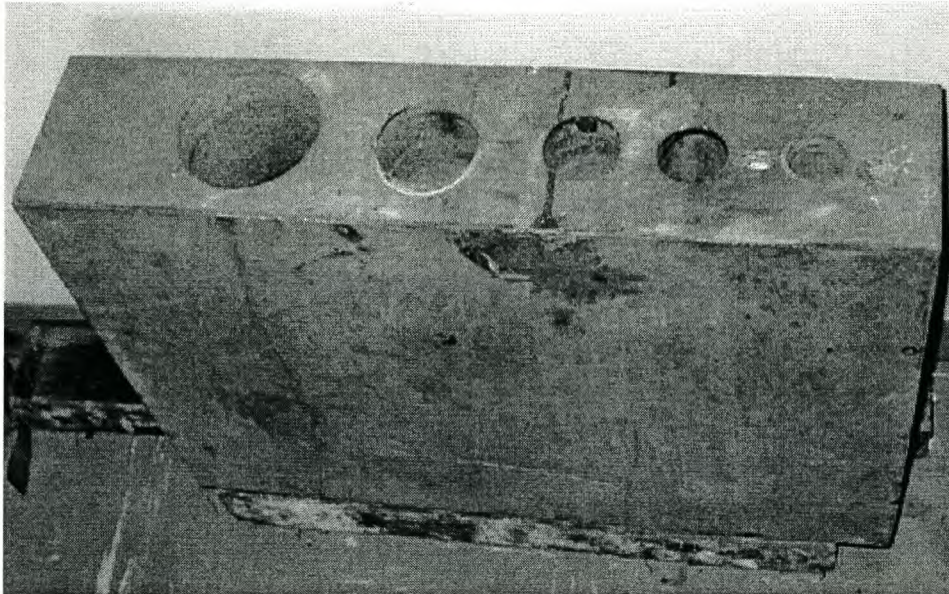


Figure 7-17 Granite block with holes of 113, 76, 58, 50, 40 mm diameter.

The probe was deployed down the 76 mm hole, whilst inside the Perspex tube with the plastic centring attachments. The probe was moved down the hole whilst logging the pictures to flash memory. One of the pictures taken is shown in Figure 7-18. Accurate rock detail can be seen in the photo and the hole is lit a fair way down. Striation marks made by the drill can clearly be seen on the sidewall. The lighting is still not evenly spread causing saturated (white) pixels around the edges.

¹⁹ Affectionately known as the tombstone.

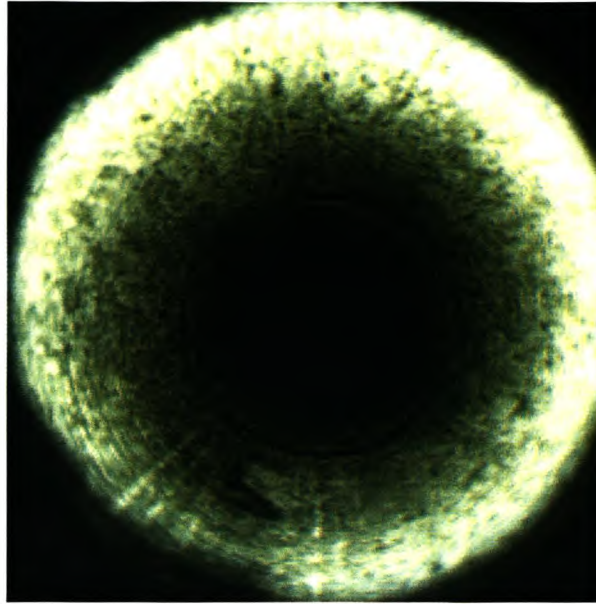


Figure 7-18 Inside of tombstone picture.

Two frames (1 and 2) were taken from the deployment test and unwrapped using the algorithm described in Section 6.3. A polynomial fitting equation was also generated for this hole by imaging a tape measure placed on the sidewall and counting the number of pixels between graduations. The best lit regions were removed from these geometrically correct unwrapped images and are shown in Figure 7-19 and Figure 7-20.

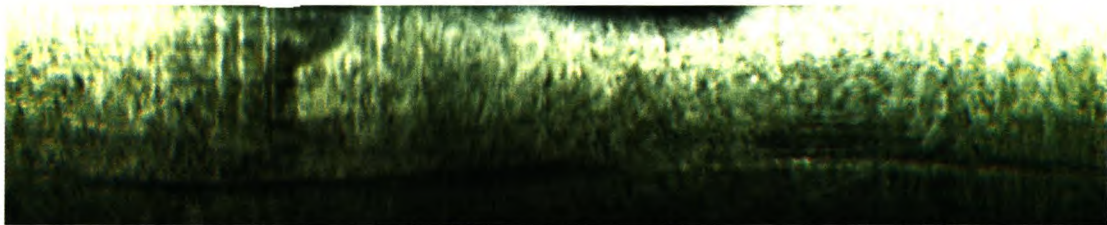


Figure 7-19 Unwrapped section of frame 1.

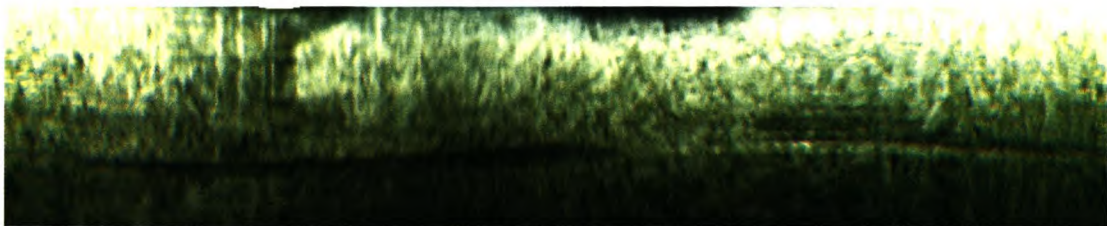


Figure 7-20 Unwrapped section of frame 2.

These two colour images were then run through the correlation process. Colour images such as the ones above consist of a red, green, and blue value for each pixel. The correlation process for every row was tested using an array of all three colours at once.

The centre row (50) was chosen from frame 2 and it was correlated with every row from frame 1. The correlation values for each row are shown in Figure 7-21. There is a clear well defined peak with a correlation coefficient of 0.94 at row 68. Meaning that between frames the probe has moved 18 pixels.



Figure 7-21 Correlation of one row from frame 2 with all rows from frame 1.

One might argue that this is a lucky or contrived result. However, Figure 7-22 shows the correlation coefficients calculated by correlating every row of frame 1 with every row of frame 2. There is a clearly defined watershed running linearly across the plot.

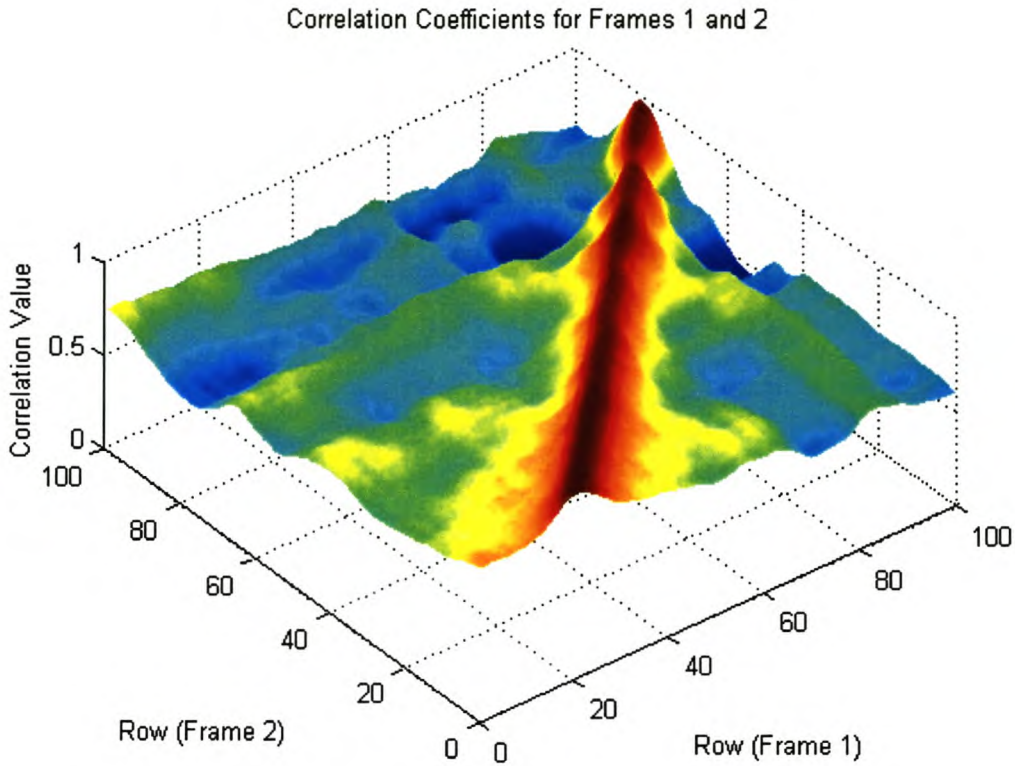


Figure 7-22 Correlating every row in frame 1 with every row in frame 2.

Carefully looking at Figure 7-22, one notices that the best correlation straight line has a gradient of close to one. Investigating this further, Figure 7-23 was plotted. This graph shows the displacement in pixels against the rows of frame 2. Ideally this should be a straight line showing that every row in frame 2 has moved the same number of pixels with respect to frame 1. This would prove that the geometrically correct unwrapping algorithm is working correctly. However, there are some variations in the offsets, between a maximum of 20 and a minimum of 17. The pixel variations are due to inaccurate distance pixel mapping as well as blurring caused by both the moving probe and the Bayer's colour interpolation algorithm. However, for the first 38 rows, where there is maximum resolution, the variation in offsets is only one pixel. It can thus be calculated that between frames 1 and 2 the probe moved 3.9 mm (19.5 pixels times 0.2 mm per pixel).

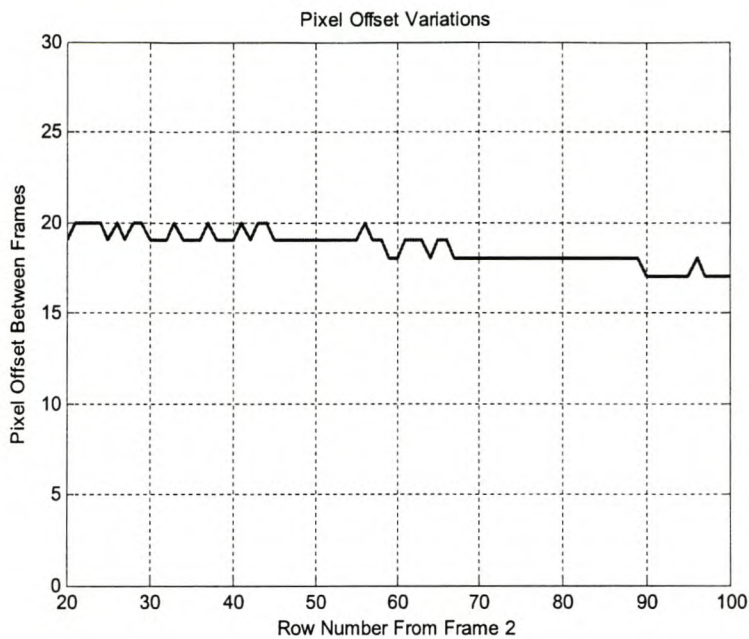


Figure 7-23 Pixel offset between frames.

MATLAB code was written to take the individual strips and stitch them together based on the results from the correlation formula. Figure 7-24 shows this virtual core. It is the result of 40 image frames being stitched together and represents approximately 160 mm of the borehole with a resolution of 0.2 mm per pixel. Although the virtual core is detailed and some features clearly run across strip transitions, there are problems:

- Variable lighting makes the top of each strip brighter than the bottom. This makes the individual strips clearly visible.
- There is some inaccurate stitching due to the pixel offset variations discussed previously.
- Due to the short length of the rock test borehole and the inadequate plastic centring spacers, the probe angle tilts slightly between images causing distortion.

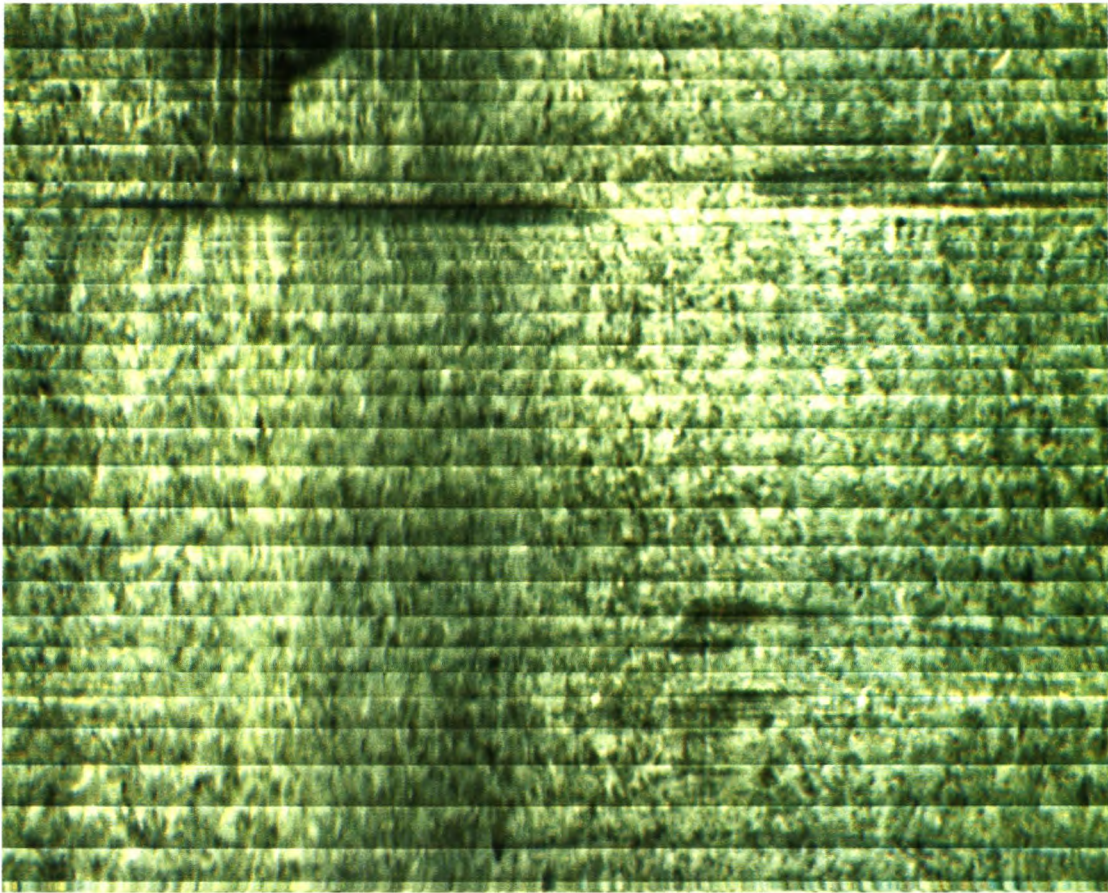


Figure 7-24 Virtual core.

7.8 Power Usage

The majority of the power used by the RockEye probe is used for the LED lighting. Without the lighting the rest of the electronic use 128 mA when not logging and 160 mA whilst logging images. The current used by the lighting depends on the exposure time. With the exposure at the maximum setting, the LEDs add on an extra 600 mA, and with it at its minimum only an extra 2 mA. Even with maximum exposure the probe should be able to record for two and a half hours when using the current 2000 mAh battery pack.

7.9 System Cost

Table 7-1 shows the cost of the critical components used in this design. As this is a prototype, the packaging and PCBs are not finalised and not included in this estimate.

Quantity	Component	Price Each
1	Xilinx XCV50 FPGA	R 150
1	256MB Ultra II SD flash card	R 950
8	Osram Golden Dragon LED	R 43
1	Micron MT9V403 image sensor	R 1500
1	Fisheye lens	R 180
	Total cost	R 3124

Table 7-1 Cost estimate for critical components.

Chapter 8 Recommendations and Conclusions

This final chapter evaluates the prototype design and makes recommendations for improvements in future designs. The system specification is tabled before the final conclusion describes what has been achieved in terms of the initial objectives.

8.1 Recommendations

8.1.1 Hardware

Camera

The camera performed well and met the desired colour, resolution and frame rate specifications. The layout of the PCB could do with a few modifications. The component spacing is really tight and difficult to populate – smaller capacitor package sizes should be used. The wire connectors to the camera board are simply soldered into the board, which is messy and time consuming – a small form connector should rather be used.

During development, a vast amount of time was spent getting the camera's serial interface to work. The fault was eventually found to be an electromagnetic compatibility problem caused by a combination of capacitive and inductive coupling. The sharp rise time (2ns) of the system clock driven by the FPGA was coupling voltage spikes onto the serial clock line. This led to unpredictable errors when attempting to program the internal camera registers through the serial interface. The eventual solution was to rewire the digital lines to the camera with a separating ground line in-between each line. A new revision of the camera board should include these separating ground lines. Additionally, the PCB should be expanded from a two layer board to a four layer board with a dedicated ground plane. Additional power supply smoothing should also be included – it is envisaged that these steps will reduce noise on the images.

SD Card

The SD card performed reliably and the system was not limited by the read or write speeds. It was very useful in the mine environment to be able to simply remove the flash card for post processing. The 256 MB SD card used in the prototype model can only store 100 seconds worth of images and this is not practical. If the firmware is upgraded to store only the useful annular ring from the image, this will halve the data rate from 2.3 to 1.2 MB/s. Then, with a 1 GB flash card, it will be possible to store over 13 minutes of data, which is close to a realistic figure. If needs be, multiple flash disks could also easily be added.

FPGA

The FPGA enabled all the processing tasks be performed admirably. It took a little longer to write some of the initialization code than it would have on a microprocessor, but the hardware design, with just an FPGA, is much simpler and still highly configurable. Currently 60% of the hardware resources of the XCV50 FPGA are used in this design. With the additional functionality envisaged to be included in future systems it may be wise to upgrade to the XC100 with double the amount of hardware resources. These two FPGAs are available in the same package, so upgrading would simply be a drop in replacement.

Lighting

A number of different lighting setups were tried and tested as shown in the testing Section 7.2. The problem is that optimally, the lighting should come from in front of the lens, but it is not possible to get the power to the lights without putting wires in front of the lens.

8.1.2 Optics

From the conic mirror testing and further investigations completed by Robin Starke [16], it seems that implementing a conic mirror in a small macro type setup is extremely tricky. Starke used four different lenses varying in focal length from 2.97

to 12 mm, and a real time webcam to immediately evaluate results, which were never as good as with the fisheye lens. One further option to test is with the biggest mirror possible in the given packaging. A larger mirror is less curved, which could lead to less blurring of the concentric parts of the image.

The fisheye lens outperformed the conic mirror pictures, however it does exhibit non-linear compression towards the centre of the image – this was taken care of using software scaling. There are a few board mount fisheye lenses on the market, some of them very well characterized and costing ten times more than the current one [24]. These could be tested to ascertain if they improve the picture quality and resolution.

8.1.3 Firmware

The VHDL code, implemented in logic on the FPGA, reliably performs the diverse jobs of initialization as well as bulk data transfer. Some of the benefits of working with programmable hardware are that different tasks can be implemented in parallel and the timing of data transfer can be rigorously defined in terms of clock cycles.

There are currently two faults with the system and some scope for improvement. The first fault is that sometimes when switching to recording mode the system freezes and has to be restarted – this problem does not occur frequently and has to do with the fact that the switch is asynchronous with respect to the frame timing and will be fixed with a little investigation.

The second fault is more serious and has to do with the system design. The symptom of this fault is that while writing image data to the SD card, one or two frames are lost in every seventy. This is caused by the SD card going into a busy mode approximately every seven seconds. While in this mode no further writing is possible for a variable amount of time, normally 10 ms. Consequently parts of two image frames are lost. Although described in the SD specification, the timing and duration of the busy signal is not quantified anywhere and varies from one card brand to the next.

To rectify the problem the FIFO memory buffer must be enlarged from 2 kB to around 500 kB (0.5 MB). This will enable the card to store the two frames that have to be written while the card is in busy mode and write them at a later stage with no loss of data. None of the Xilinx FPGAs contain this amount of internal memory so external RAM must be added to the board and interfaced by the FPGA.

Once the optics have been further tested and the desired annular ring is accurately known, it can be selected on the FPGA resulting in a huge space saving on the memory card.

The image sensor output pixel data is in 10-bit format, currently only the most significant 8-bits are used as these can be stored more effectively on the SD card and PC. Rather than just selecting eight of the ten bits, a formula can be used to compress the higher valued numbers in a non-linear manner. This will give the sensor better dynamic range – meaning that it is more difficult to saturate or under expose the image.

Instead of writing data to the SD card in raw image format, the data should be written in the DOS FAT32 format. This would involve writing a file allocation table and a directory structure. The additional overhead would be worth the effort as then instead of having to download the flash card using specialised software the data can be downloaded using built in Windows™ file handling software.

Currently all the needed clock frequencies are generated from the one external clock. As mentioned in Section 5.5, this is bad practice. Future designs should include multiple clocks, minimising the need to generate internal clocks.

The auto exposure algorithm works as intended, but there is a problem in its logic. If the camera is taking a picture of black rock the eventual picture should be dark, yet the rock texture should be visible. An intelligent algorithm should be developed to test if there is sufficient texture in a photograph as opposed to simply measuring the mean luminescence of the image.

8.1.4 Image Processing Software

The post processing software completes its own individual tasks well. However they are implemented in MATLAB code which is slow – it currently takes about 12 hours to transform 1000 images into colour. The entire process from reading in the file to producing a virtual core should be automated into a single process requiring minimal user input. The code should be written in a compiled language like C++, this will improve the speed considerably.

To improve image quality, various different Bayer's pattern demosaic algorithms can be tested to decide which one is best suited for this application. Another step that has not been implemented in this thesis is white balance. Human vision is remarkable as our eyes adjust the colours we see according to the colour of the light with which it is illuminated. This means that white always looks white no matter what colour light is shined on it. In a camera system this is accomplished by testing the illuminating light shining on a standard grey background and generating a colour correction matrix.

The correlation distance measurement gives encouraging results, however the successful lab tests will have to be validated by rigorous field testing. Various image processing techniques will have to be developed to achieve the best possible accuracy for the system.

8.1.5 Packaging

The plastic that the centring devices were made from was not rigid enough and too brittle. In future versions they should be made from sprung steel, adjustable for various sized boreholes. The packing was watertight, but would have to be modified if it was going to be deployed to great depths.

The probe diameter could easily be reduced from 40 mm to 30 mm, to fit into smaller holes. All of the critical components were chosen to be able to fit inside a 28 mm pipe. The lighting would then have to be redesigned.

8.2 Future Developments

8.2.1 Real-Time Test Mode

Adding the external RAM needed to correct the buffering problem will also enable a testing camera mode to be implemented. In this mode real time video will be stored onto the memory and downloaded via the USB port to a PC. Although this functionality is not desired for the final product, it is extremely useful to have real-time pictures to view when focussing or experimenting with the probe.

8.2.2 Wireless Downloading

Downloading the image data using conventional means such as Bluetooth will take too long as shown in Table 3-2. A new standard for wireless download called WiFi²⁰ or IEEE 802.11 is available offering download speeds of up to 10 MB/s. SanDisk make a WiFi card in the same form as an SD card that can be communicated with using the already developed SD card protocol.

8.2.3 Linking with Orientation Sensor

Knowing the orientation of the probe is important when the probe intersect a new layer of rock strata. The geologist would want to know at what angle the borehole intersects the layer. If the probe rotates while being deployed down the borehole, there is no way of knowing its orientation. A device has been developed within the borehole radar group called the Sindlehead²¹ navigator. The navigator can be used to log the trajectory of a borehole as well as the roll angle of the probe. It could be linked to the RockEye to form a more intelligent borehole camera while simultaneously logging the trajectory of the hole.

²⁰ <http://www.wi-fi.org/>.

²¹ Developed by Tim Sindle, Charles Whitehead, and Wessel van Brakel.

8.3 System Specification

RockEye System Specification²²	
Physical	
Length	1.27 m
Diameter	40 mm
Weight	2 kg
Optics	
Lens	1.78 mm fisheye lens
Resolution	0.5 mm
Lighting	8 LEDs 10,000 mcd each
Power	
Current usage ²³	160 mA to 760 mA
Operating time	2.5 hours to 12.5 hours
System	
Frame rate	10 frames per second
Image resolution	480 by 480 pixels
Colour	RGB Bayer's pattern
Image size	230 400 bytes
256MB SD flash card actual capacity	246 768 400 bytes
Images per 256MB card	1070
Time to fill card at current rate	1 minute 45 seconds
Data storage rate	2.3 MB per second

Table 8-1 Final system specification.

²² This can be compared with the existing borehole imaging systems on page 6.

²³ Current usage depends on the lighting needed to effectively capture the texture of the rock.

8.4 Conclusion

The objective of this project was to design a working prototype of a complete borehole imaging system. The RockEye probe was the first successful implementation of a completely autonomous borehole imager. All of the initial specifications for the system were met or exceeded barring wireless download. Clear accurate pictures were taken of test grids and rock boreholes. The quality of the rock images acquired does not reflect the true potential of the system. Accurate focussing and effective lighting should improve these pictures considerably. Images were successfully unwrapped to form geometrically correct strips that were stitched together using correlation techniques to form a virtual core. Attention will have to be paid to reducing the amount of data stored on the flash disk as the current limit is not practical. Overall the system design is sound, however, there are incremental improvements to be made and a substantial amount of testing still to complete.

Chapter 9 References

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