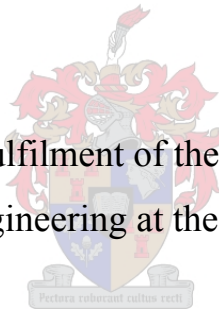


# **Electronic voltage regulator technology for rural electrification**

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Thesis presented in partial fulfilment of the requirements for the degree  
of Master of Science in Engineering at the University of Stellenbosch



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March 2008

# DECLARATION

I, the undersigned, hereby declare that the work contained in this thesis is my own original work and that I have not previously in its entirety or in part submitted it at any university for a degree.

Signature:

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## Summary

This thesis discusses the development of a 5 kVA single phase AC voltage regulator, specifically designed to assist in the reduction of electrification costs in sparsely populated rural areas. The voltage regulator is based on a solid state auto-transformer tap changer, designed to be robust and maintenance free.

Electrification cost savings can be realized if the length of the LV network can be extended to reach more households. To accomplish this, a voltage regulator can be installed onto the extended LV feeder at the point where the LV voltage will drop below the minimum valid voltage, thereby boosting the voltage downstream and enabling more customers to be connected.

A variety of voltage regulator topologies were investigated to obtain the best topology for the application. The voltage regulator design is discussed in detail with careful attention given to the power loss incurred, surge voltage protection requirements, protection coordination with the existing LV network and the thermal design requirements. An electronic controller based on a digital signal processor together with an appropriate power supply is designed and built. The software to control the voltage regulator is developed, integrated with the hardware and debugged. The complete voltage regulator is evaluated through extensive laboratory testing and field trials are performed to verify the performance of the device.

## Opsomming

Hierdie tesis bespreek die ontwikkeling van 'n 5 kVA, enkelfase, wisselstroom spannings reguleerder, spesifiek ontwerp om koste besparings te bewerkstellig in die elektrifisering van yl bevolkte landelike gemeenskappe. Die spannings reguleerder se ontwerp is gebaseer op 'n outo-transformator tap wisselaar met vaste toestand skakelaars, om sodoende robuust en instandhoudings vry te funksioneer.

Elektrifiserings koste besparings is moontlik indien die laag spannings distribusie kabel verleng kan word, om sodoende elektrisiteit aan meer huishoudings te voorsien. Om dit moontlik te maak kan 'n spannings reguleerder geïnstalleer word op die punt waar die kabel spanning onder die minimum toegelate spanning daal. Sodoende word die spanning weer verhoog aan al die huishoudings wat aan die verlengde gedeelte van die kabel verbind is.

'n Verskeidenheid uiteenlopende spannings reguleerder topologieë is ondersoek om die beste topologie vir die toepassing te identifiseer. Die ontwerp van die spannings reguleerder is baie deeglik bespreek en spesifieke aandag is gegee aan die verliese, spits opwelling spannings beveiliging, sinkronisasie met die huidige laag spannings netwerk se beveiligings meganismes en die termiese ontwerp van die stelsel. 'n Elektroniese beheerder, gebaseer op 'n digitale sein verwerker, tesame met 'n toepaslike kragbron is ontwerp en gebou. Die nodige sagteware om die spannings reguleerder te beheer is ontwikkel, geïntegreer met die hardeware en ontfout. Die volledige spannings reguleerder is ontleed deur intensiewe toetse in die laboratorium en toets installasies op laag spannings netwerke, om sodoende die nakoming van die werks verrigting vereistes van die toestel te bevestig.

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# Glossary

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## Abbreviations

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ABC	Arial Bundle Conductor
AC	Alternating Current
AD	Analog to Digital
ADC	Analog to Digital Converter
ADMD	After Diversity Maximum Demand
CT	Current Transformer
CVT	Constant Voltage Transformer
DA	Digital to Analog
DARAM	Dual Access Random Access Memory
DC	Direct Current
DMC	Dough Mould Compound
DSP	Digital System Processor
EVR	Electronic Voltage Regulator
FLASH	Non volatile memory type
GRP	Glass Reinforced Polyester
HV	High Voltage
IC	Integrated Circuit
IP	Ingress Protection
IPC	Insulation Piercing Connector
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LV	Low Voltage
MIPS	Millions of Instructions Per Second
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MOV	Metal Oxide Varistor

MV	Medium Voltage
NTC	Negative Temperature Coefficient
PC	Personal Computer
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
RMS	Root Mean Square
SARAM	Single Access Random Access Memory
SCI	Serial Communication Interface
SPI	Serial Peripheral Interface
SWER	Single Wire Earth Return
TF	Transformer
UV	Ultra Violet

---

### **Circuit symbols**

---

C	Capacitor
CB	Circuit breaker
CT	Current transformer
L	Inductor
R	Resistor
S	Switch
SA	Surge arrestor

---

### **Units**

---

°C	Degrees Celsius
A	Ampere
cm	Centimeter

Hz	Hertz
J	Joule
kg	Kilogram
m	Meter
min	Minute
mm	Millimeter
s, sec	Second
T	Tesla
V	Volt
VA	Volt ampere
W	Watt
$\Omega$	Ohm

---

# **Chapter 1**

Introduction

---

# 1 Introduction

## 1.1 *Electrification initiative*

To improve the living conditions of all South Africans, the government in conjunction with the electricity utility (ESKOM) has started a national initiative in the early 1990's to provide basic electricity to all South Africans by 2012. Through this drive 3.3 million households has been electrified by ESKOM up to the end of 2006 [5].

South Africa's household distribution can be categorized as urban, peri-urban, rural and deep rural settlements according to population density. Nationally, 8 % of urban / peri-urban households are still without electricity compared to 18 % of rural / deep rural households.

From a technical point of view, the cost per connection for grid extension is determined mainly by the following factors:

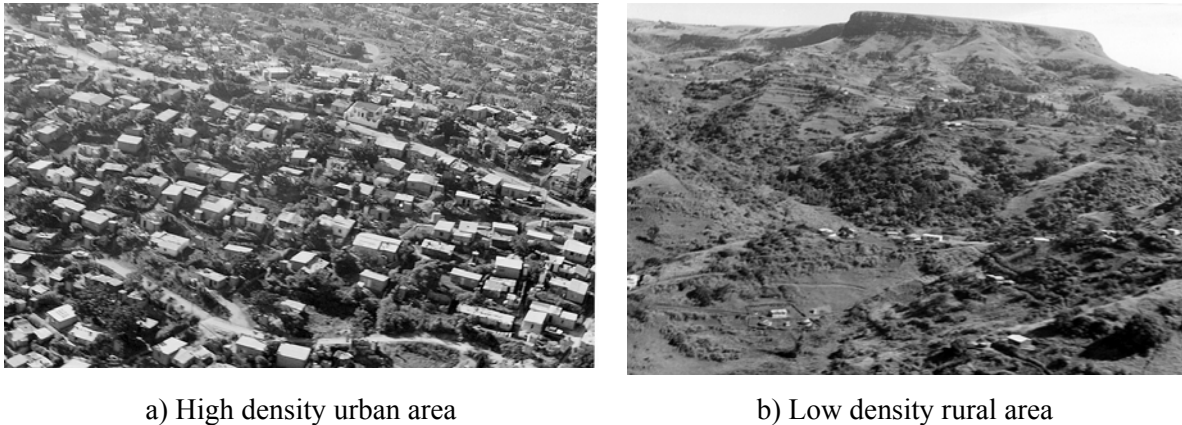
- Distance of the settlement from an existing supply grid
- Settlement density
- Projected load

To reduce the capital and operating costs involved in the electrification program, innovative approaches to supply technologies was made [1] [6], which includes:

- Single wire earth return (SWER) feeders which:
  - Allow longer spans lengths
  - Requires less line hardware (e.g. insulators, cross arms, conductor ties etc.)
- Phase-phase medium voltage (MV) networks
- Dual phase low voltage (LV) networks
- Pole mounted transformers
- Aerial bundle conductors (ABC)
- Optimized after diversity maximum demand (ADMD)
- Large scale introduction of pre-payment metering

Even with these new innovative technologies, rural electrification still poses a challenge [6] [7]. These communities are generally further away from the existing grid which makes electrification more expensive. The costs are escalated even further due to the sparsely populated, low density distribution typical of rural areas versus that of urban areas as shown in

Figure 1-1. The only positive factor reducing the costs of rural electrification is that the projected load is typically very low, allowing initial capital costs savings to be made.



**Figure 1-1: Housing density**

To illustrate the difference between the average cost per connection in urban as opposed to rural and deep rural areas, the following cost per connection per area class in the Eastern Region (for the year 2004) is shown in Table 1-1 [10]. The major component contributing to the high cost in rural areas are the settlement MV and LV cost per connection.

**Table 1-1: Eastern region - Cost per connection (2004)**

	Urban	Rural	Deep rural
Settlement MV and LV	R 2,017	R 3,055	R4,735
Total cost including bulk MV line and bulk high voltage (HV)/MV strengthening per connection	R 2,687	R 4,533	R6,812

These figures show a electrification cost difference of more than 100 % between the urban and deep rural areas, mainly due to fewer connections per transformer zone in the low density areas. These high rural electrification costs are posing challenges to the electrification program and new approaches need to be considered.

## **1.2 Supporting rural electrification**

To reduce rural electrification costs (in conjunction with the innovations already mentioned in the previous section) the possibility of increasing the number of connections per transformer zone is proposed [8] [9]. This can be accomplished by allowing the LV line to be extended over longer distances, thus reaching more households. This does however lead to voltage regulation

problems for the customers connected to the extended portion of the line, due to the additional voltage drop across the extended feeder.

To compensate for this voltage drop, the voltage can be regulated at the point where the voltage reaches the minimum allowable level of 10 % below nominal, with an appropriate voltage regulation device. This regulator boosts the voltage back to the maximum allowable level of nominal plus 10 %, thus enabling the line reach to double (assuming that the load on the transformer is low enough to accommodate the additional connections on the extended line). Doubling the length of the line increases the area that can be covered by a factor of four. In practice the benefit is however not as large, since communities are not evenly dispersed over the area. The absolute low-end estimate would be a 50 % increase in the households when regulating the feeder at a single point per feeder. In this way, LV regulation saves one transformer zone MV line and transformer per two installed zones.

### **1.3 Thesis objectives**

The objective of this thesis is to develop a single phase AC voltage regulator, suitable for use in LV reticulation networks. The operation of the voltage regulator must be proven through laboratory evaluation and field trials.

The voltage regulator must adhere to the following basic requirements:

- Automatic voltage regulation
- Substantial overload capability
- High efficiency
- Minimum maintenance requirements (i.e. no moving parts)
- Protect customers against sustained over voltage (i.e. neutral connection failures)
- Pole mountable
- Reliable
- Low cost

### **1.4 Structure of the report**

This chapter introduced the challenges facing the electrification drive in South Africa, especially for rural settlements. To assist in cost effective rural electrification, the concept of using a voltage regulator in conjunction with extended LV feeders was introduced. The objectives of the thesis were set out and the required characteristics of the voltage regulator were introduced.



Chapter 2 presents an overview of the concept of voltage regulation applied to the reticulation network. A background study on a number of different voltage regulator topologies is completed. The operation of each topology is described and their major advantages and disadvantages are listed. Using the voltage regulator requirements set out in this chapter, the different topologies are then compared to select the most suitable topology for the application

Chapter 3 provides an overview of the voltage regulator developed in this thesis, by describing the features, technical specifications, construction and basic operation of the device. All the protection modes and means of identifying a specific error through the status indicators are highlighted. Detailed design information and results are presented in the following chapters.

Chapter 4 presents a detailed design of the power circuit, together with comprehensive power loss calculations and a complete thermal design of the enclosure. Careful attention is given to the surge voltage and coordinated protection issues, to ensure the reliability of the EVR.

Chapter 5 focuses on the design of the controller and its power supply, to enable control of the power circuit. Various topologies to be used in the power supply are evaluated and the preferred topology is designed in detail. A description of the controller together with its measurement circuitry and thyristor drive circuits is provided.

Chapter 6 describes the development of the software code that controls the functionality and behaviour of the EVR. The software consists of a number of files, all linked together. A brief overview of the function of each file is given, before a detailed description of the parameters that can be used to fine tune the behaviour of the EVR is given. This is followed by flow diagrams, explaining the main program code.

Chapter 7 discusses the results obtained from tests performed on the EVR in a laboratory environment. These tests verify the electrical and thermal design of the EVR as well as the correct operation of the software code. Results obtained from a field trial installation are also presented.

Chapter 8 gives a brief overview of the voltage regulator designed in this thesis and discusses the performance of the device and future work regarding improvements to the system and the long term evaluation of the device.

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## **Chapter 2**

### Voltage regulation

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## 2 Voltage regulation

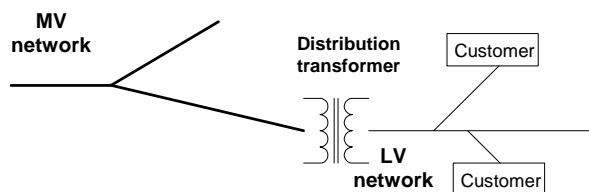
This chapter presents an overview of the concept of voltage regulation on the reticulation network. A background study on a number of different voltage regulator topologies is completed. The operation of each topology is described and their major advantages and disadvantages are listed. Using the voltage regulator requirements set out in the previous chapter, the different topologies are then compared to select the most suitable topology for the application.

### 2.1 Reticulation network

The key objective of the medium voltage (MV) and low voltage (LV) distribution network is to provide customers with power at voltage levels for which appliances and equipment will operate with acceptable levels of performance and efficiency [11]. As stipulated in the South African Electricity Act and NRS 048 the nominal LV voltage for new customers is 230 V with an allowable voltage variation of  $\pm 10\%$ .

A typical MV / LV reticulation network is shown in Figure 2-1. The LV voltage supplied to the end user depends on the following factors:

- MV sending voltage and voltage control philosophy
- MV network voltage drop
- MV to LV distribution transformer secondary rated voltage (220 V, 230 V, 240 V) and tap setting
- Distribution transformer voltage drop
- LV network voltage drop



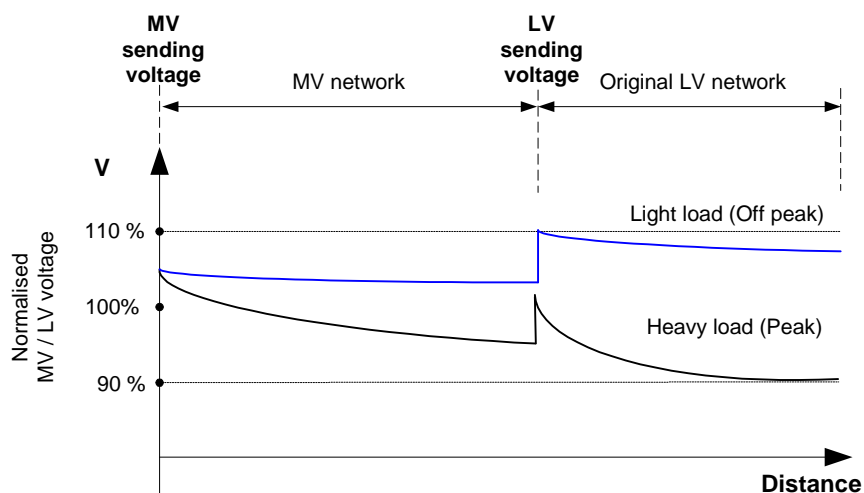
**Figure 2-1: MV / LV reticulation network**

To keep the voltage supplied to the end customer within the required minimum and maximum limits careful attention must be given to the design of the MV and LV networks, their interaction, and the loading on the network. A typical MV / LV network voltage profile during

light loading (off peak times) and heavy loading (peak times) is shown in Figure 2-2. (The voltage drop and transformer tap boost percentages are given for illustration purposes and not necessarily representative of a real network.)

Under light loading conditions, the MV voltage decrease from 105 % to 104 % at the distribution transformer. With a tap boost setting of 6 % at the distribution transformer, the LV sending voltage is increased to the maximum allowed 110 %, decreasing to 107 % at the end of the LV line. Under heavy loading, the MV voltage decrease from 105 % to 95 % at the distribution transformer. Adding a 6 % transformer boost increase the LV sending voltage to 101 %, which decrease to the minimum allowed voltage of 90 % at the end of the LV line.

(The MV profile is drawn with fixed MV voltage control resulting in the same MV sending voltage under light and heavy load conditions. Through use of line drop compensation or voltage compounding techniques the MV sending voltage can be decreased during light loading, allowing higher boosting ratios at the distribution transformer to be used.)



**Figure 2-2: MV / LV voltage profile**

To extend the reach of the LV feeder, thereby increasing the number of customers that can be connected to the line, a voltage regulator (VR) can be installed close to the location where the original LV network voltage drops to 90 %. This is shown in Figure 2-3.

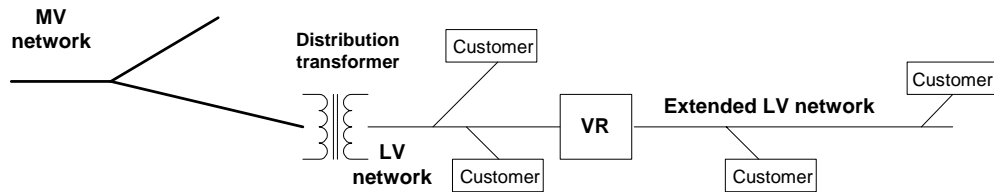


Figure 2-3: MV / LV network with LV voltage regulator

The new voltage profile can be seen in Figure 2-4, where the voltage regulator boost the voltage under light or heavy loading conditions to close to 110 %, allowing extension of LV network.

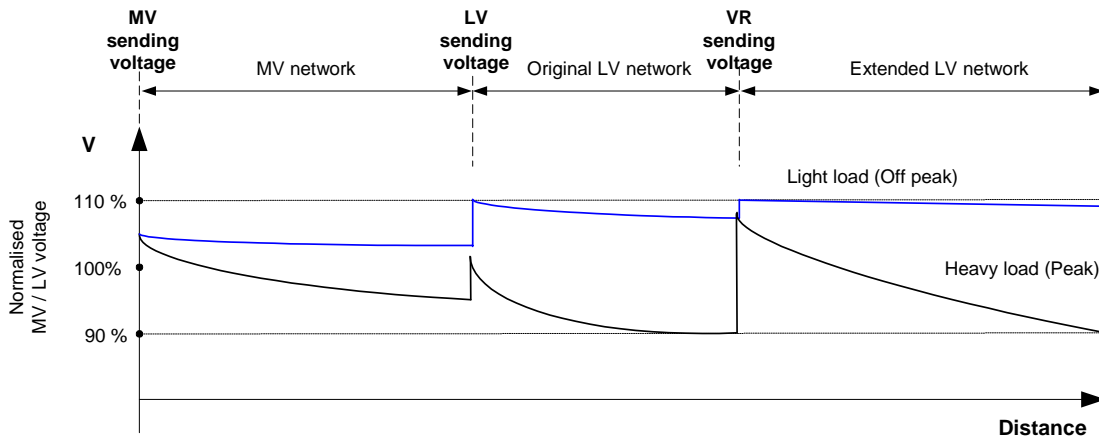


Figure 2-4: MV / LV voltage profile with LV voltage regulator

## 2.2 Circuit topologies

There are numerous different circuit topologies and technologies suitable for use in voltage regulator devices, each with its own advantages and disadvantages which make them suitable for specific applications [2] [12] [13] [14]. The voltage regulators can be classified into the following types:

- Tap changers (both discrete step and constant control)
- Saturable reactors
- Ferro resonant transformers
- Power-electronic voltage regulators

The voltage regulators are mainly suited for voltage regulation on LV networks, except for the tap changers which can also be used in MV applications. All the regulators can be used in either single phase or three phase circuits.

## 2.2.1 Tap changers

Various types of tap changers are available as shown in Figure 2-5. They operate by selecting different taps on either the primary or secondary side of a isolating or auto-transformer, thereby changing the transformer winding ratio and consequently the output voltage. The tap positions can be selected such that the supply voltage is either increased or decreased as required by the specific application.

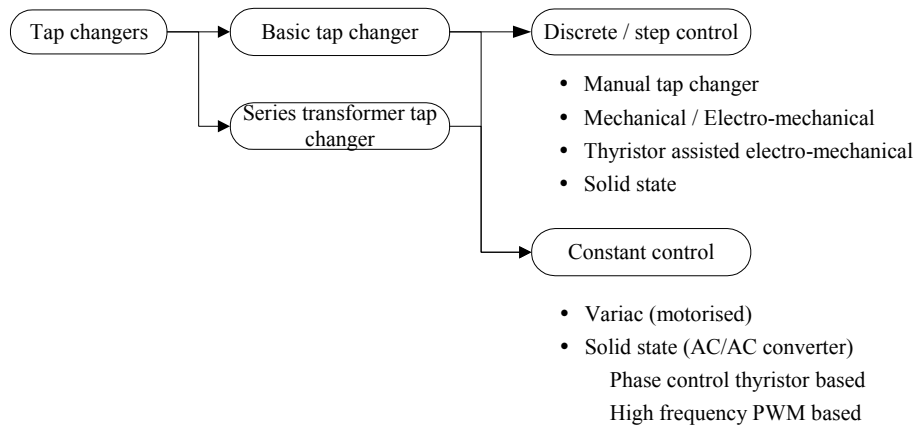


Figure 2-5: Tap changer types

Selection of either an isolating transformer or auto-transformer tap changer depends on the specific application in which the tap changer will be used. Consider the diagram in Figure 2-6 where a portion of a MV line, distribution transformer and LV line is shown. If the tap changer is to be used at the distribution transformer (point A) where the MV voltage is stepped down to the LV reticulation voltage, an isolation transformer will be a more appropriate choice due to the high step down ratio and probable voltage isolation requirement. If the tap changer is connected in line in either the MV or LV network to obtain a small (less than 50 %) change in voltage (point B and C), no voltage isolation is required and cost savings can be made using an auto-transformer based tap changer.

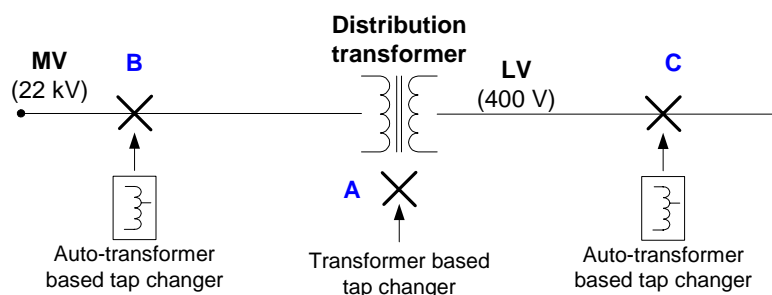


Figure 2-6: Tap changer location

Placement of the taps on either the primary or secondary side of the transformer depends on the type of technology used in the tap switches, and the nature of the application. If the tap changer is to be used in a step down transformer configuration, the currents on the primary side will be lower than those on the secondary side. Placing the taps on the primary side will thus enable lower rated current switches to be used, which depending on the type of tap switch can lead to lower costs. The tap switches must however be capable of withstanding the higher voltage on the primary side.

The circuit topology of the “basic tap changer” and “series transformer tap changer” will be described in the following sections, together with the different types of switching elements that can be used in the tap switches. For illustration purposes, all circuit configurations shown employ an isolating transformer with taps on the secondary side. The type of transformer (isolating versus auto-transformer) and placement of the taps (primary versus secondary side) can however be changed to suit the requirements of the particular application in which the voltage regulator will be used.

### 2.2.1.A Basic tap changer

The basic tap changer circuit configuration, with the taps placed on the secondary side of an isolation transformer, is shown in Figure 2-7. Changes in the input supply voltage are monitored using an electronic circuit, which then selects and activates the appropriate tap switch ( $S_0$  to  $S_n$ ) in order to control the output voltage.

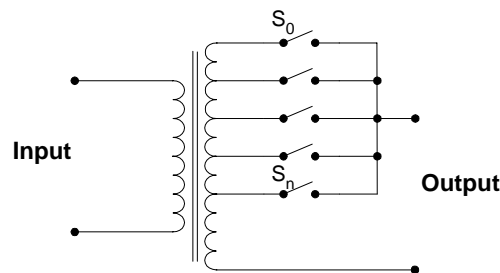
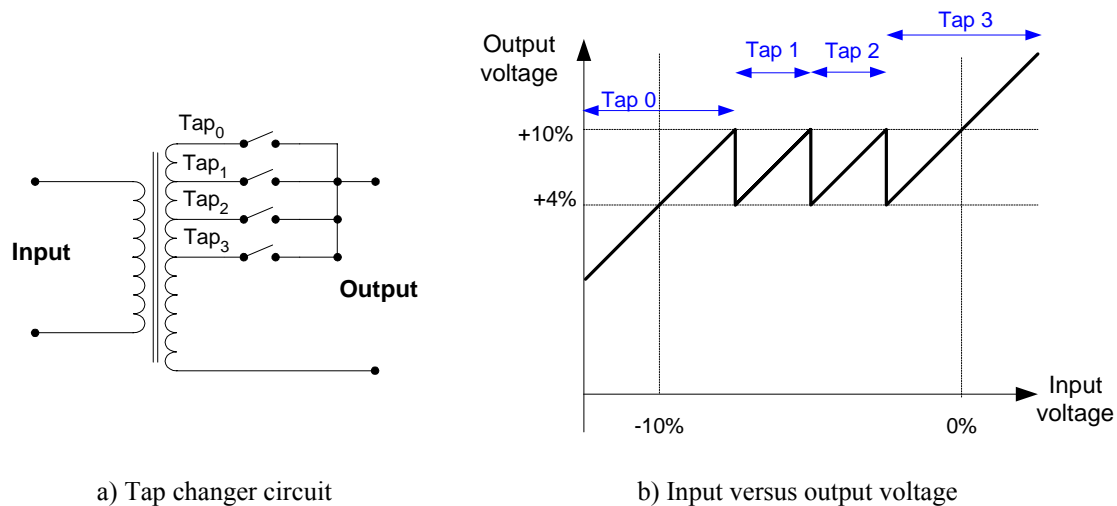


Figure 2-7: Basic tap changer

### 2.2.1.B Discrete / step control

Discrete / step control implies that the output voltage will change in steps [14]. The step size is determined by the number of taps used and the input voltage range over which regulation is required. A typical output voltage obtained from such a tap changer is shown in Figure 2-8. This specific tap changer has 4 tap positions, each boosting the input voltage such that the output voltage is maintained within a certain band.



**Figure 2-8: Step voltage control**

The tap switches can be realized physically through a number of different technologies, each with certain advantages and disadvantages. These are:

- Manual
- Mechanical / electro-mechanical
- Thyristor assisted mechanical / electro-mechanical
- Solid state

### **Manual**

This is the simplest type of tap changer and essentially consists of a tapped transformer. The tap connections are available through bushings mounted onto the transformer tank and are changed manually. The manual tap changer is only feasible to be used in applications where the supply voltage is expected to remain constant over very long time periods (in excess of a year).

The main advantages are:

- Low cost
- No control circuitry necessary
- High efficiency - determined by the efficiency of the transformer.

The main disadvantages are:

- Offline tap changing process, implying that the supply is interrupted during a tap change
- Response time to voltage variations is extremely slow since it depends on physical disconnection of the output from the tap and reconnecting it to a different tap
- Poor line transient suppression.



### Mechanical / Electro-mechanical

The tap switches used in these regulators can consist of electro-mechanical devices (relays), contacts operated by a spring loaded mechanism or contacts operated by a motorized slider as shown in Figure 2-9 [14] [15] [16]. During tap changes, the tap slider should move from one tap to the other as quickly as possible.

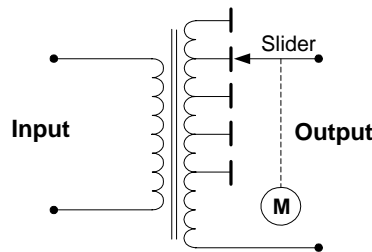


Figure 2-9: Basic tap changer with slider and electrical contacts

Two implementations of the tap slider are possible. One implementation utilizes a slider with one finger (resulting in a break before make operation), while the other preferred implementation utilizes a three finger slider (resulting in a make before break operation).

The operation of the “one finger tap changer” tap changing sequence can be described by referring to Figure 2-10 (a, b, c and d).

- The tap slider is connected to tap 1 ( $T_1$ ), and must move to tap 2 ( $T_2$ ).
- As the tap finger separates from tap 1 an arc is drawn, leading to contact wear.
- To prevent the arc from being drawn across tap 1 and tap 2, thereby shorting the portion of winding between the taps, the slider must operate slow enough to allow the arc to extinguish. This introduces a temporary open circuit, which is unacceptable in most applications.
- Tap changing operation is completed and the slider is connected to tap 2.

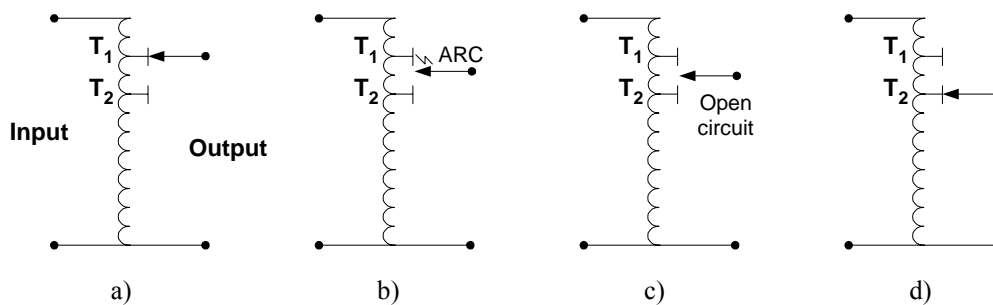
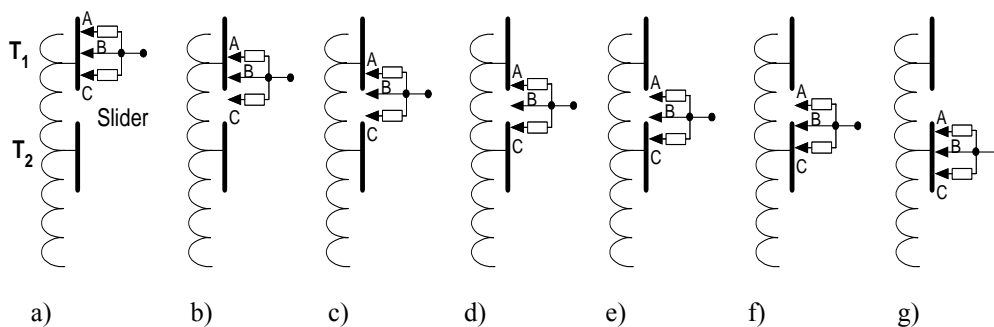


Figure 2-10: Tap changeover – Slider with 1 finger

To prevent the momentary disconnection of the load during tap changing, the preferred tap switching mechanism should operate on a make before break principle. This can be accomplished through incorporation of a bridging contact, implemented with a three finger slider. To limit the circulating current that will flow when the slider bridges two taps, impedance is added to the two outer slider fingers.

The tap changeover sequence for the three finger slider can be explained by referring to Figure 2-11 (a to g), where the fingers are marked as A, B and C. (Finger A and C has some series impedance added, while finger B has a very low impedance.)

- a) On load tap changer connected to tap 1, with load current supported by finger B.
- b) Tap change initiated and slider starts to move from tap 1 to tap 2. Finger C breaks with no arcing because entire load current is still supported by finger B.
- c) Arcing occurs as finger B breaks contact and the entire load current transfers to finger A.
- d) Arcing occurs as finger C makes contact with tap 2. Finger C and A bridges tap 1 and tap 2, thereby shorting out a section of the transformer winding. Due to the impedance of finger C and A, the circulating current is however limited.
- e) Finger A disconnects from tap 1 with arcing. The load is now connected to tap 2, with the entire load current supported by finger C.
- f) Finger B makes contact, shunting away all the current from finger C.
- g) Finger A makes contact completing the tap change.



**Figure 2-11: Tap changeover - Slider with 3 fingers**

The main advantages are:

- High efficiency in excess of 98 %
- Can handle large surge currents

The main disadvantages are:

- Moving parts that require maintenance / replacement
- Poor line transient suppression

### **Thyristor assisted mechanical / electro-mechanical**

This configuration is based on the electro-mechanical type of tap changers, with back to back thyristors added to assist in arc reduction during the tap changing process [17].

The main advantages are:

- Less maintenance required than in mechanical / electro-mechanical tap changer
- High efficiency in excess of 98 %

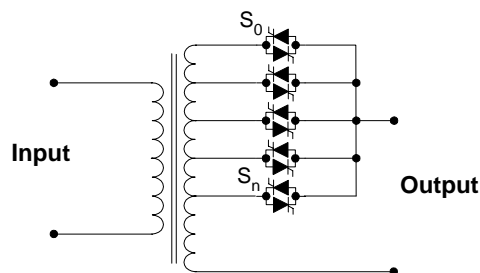
The main disadvantages are:

- More expensive than mechanical / electro-mechanical tap changer
- Poor line transient suppression

### **Solid state**

In the solid state tap changer, the tap contacts / switches are replaced with electronic devices such as thyristors or IGBTs [12] [14].

Thyristors are less expensive, have lower losses and higher surge current capability when compared to IGBTs. They are therefore the preferred choice in most applications where slow switching is used. However, because IGBTs are still in the early stages of their technology development future improvements could make them a strong competitor. In Figure 2-12 a basic tap changer with thyristors employed as switches is shown. Because thyristors can only conduct in one direction, back to back thyristors are used to realize each switch.



**Figure 2-12: Basic tap changer with thyristor switches**

The main advantages are:

- No moving parts

- High response speed between 1 to 2 cycles
- High efficiency in excess of 98 %, although lower than electro-mechanical switches due to power loss in solid state switches.

The main disadvantages are:

- More expensive than mechanical / electro-mechanical switches
- Surge current handling capability lower than mechanical / electro-mechanical switches
- Poor line transient suppression.

### 2.2.1.C Constant control

Constant control implies that the output voltage remain constant as the input voltage varies [14]. This is similar to a discrete / step control regulator with an infinite number of taps. The output voltage obtained from such a regulator designed to boost a supply voltage of nominal - 10 % to a nominal value is shown in Figure 2-13.

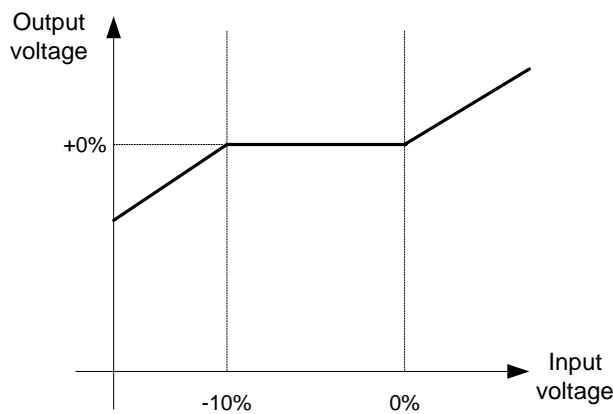


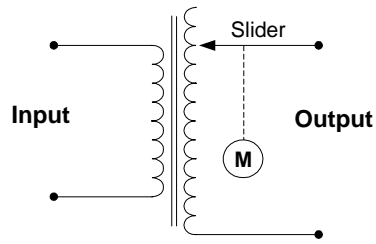
Figure 2-13: Constant voltage control

A constant voltage tap changer can be implemented with the following topologies:

- Variac with motorized slider
- Solid state AC-AC converter

#### Variac (motorized)

This voltage regulator uses a motor operated brush slider to select the appropriate position on the secondary winding, which will lead to the required output voltage as shown in Figure 2-14.



**Figure 2-14: Variac (motorized)**

The main advantages are:

- Constant output voltage
- High efficiency in excess of 98 %
- Can handle large surge currents.

The main disadvantages are:

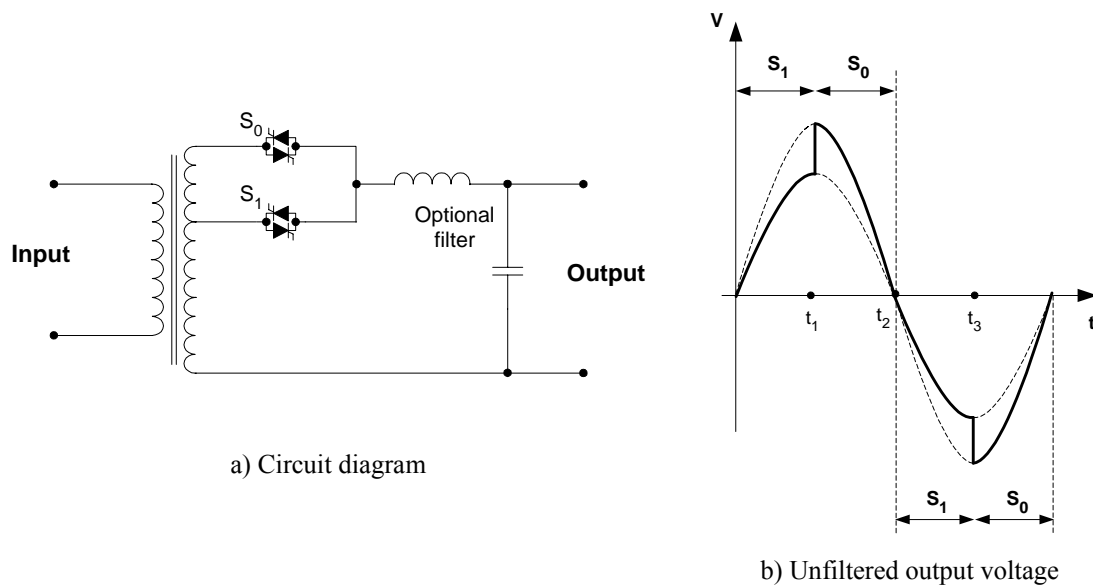
- Moving parts that require maintenance
- Slow response speed (30 V/second)
- Poor line transient suppression.

**Solid state (AC-AC converter)**

This type of voltage regulator uses semiconductor switches to switch between two different tap settings. The method of switching depends on the type of semiconductor switch used. If thyristors are used, which are difficult to commutate at instants other than the natural current zero crossing, phase control are normally implemented. If IGBTs are used, which can be operated at high frequency and turned off at any time instant, high frequency PWM techniques are used to switch between the two taps. The output voltage with both types of switching are not purely sinusoidal and an optional filter can be used to improve the output voltage waveform.

- Phase control thyristor tap changer

The phase control thyristor tap changer is shown in Figure 2-15, together with the unfiltered output voltage waveform [18]. The tap changer consists of two taps with back to back thyristor switches ( $S_0$  and  $S_1$ ) connected to each tap. An optional LC filter is used to improve to output voltage waveform by removing the unwanted harmonics.



**Figure 2-15: Phase control thyristor tap changer**

To evaluate the circuit the unfiltered output voltage is investigated. Initially switch  $S_1$  is on, connecting the output to the lower tap. At time  $t_1$ , switch  $S_0$  is turned on. Because  $S_0$  is connected to the higher tap, it will shunt away the current from  $S_1$ , allowing  $S_1$  to commutate and turn off. At time  $t_2$ ,  $S_0$  will naturally commutate (assuming a resistive load) and  $S_1$  can once again be turned on, connecting the load to the lower tap. The same sequence is repeated for the negative half cycle. Through varying the time instant  $t_1$  and  $t_3$  when  $S_0$  takes over from  $S_1$ , the output voltage magnitude can be held constant at any level between the lower and higher tap setting.

The main advantages are:

- Constant output voltage
- Low number of taps and tap switches required, resulting in cost saving.

The main disadvantages are:

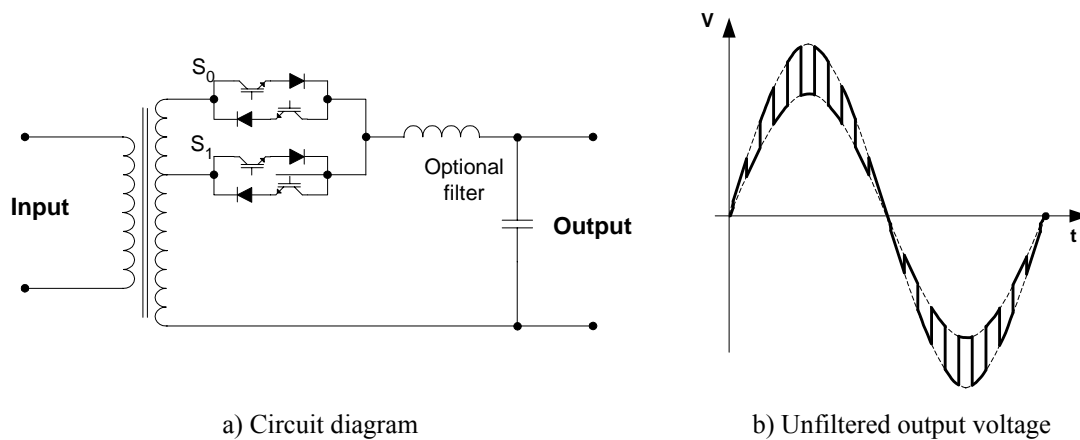
- Harmonics created in the output (without the optional LC filter)
- High output impedance and reduced efficiency (with the use of the optional LC filter)
- Large filter elements required to remove the low frequency harmonics
- Improved line transient suppression (with use of the LC filter).

- High frequency PWM controlled IGBT tap changer

The high frequency IGBT based tap changer is shown in Figure 2-16 together with the unfiltered output voltage [2] [18]. The circuit configuration is identical to that of the phase

control thyristor tap changer, except that the back to back thyristors are replaced with IGBTs switches.

Because the IGBTs are incapable of blocking a reverse voltage, series diodes must be added for reverse blocking purposes. At any instant two devices (one IGBT and one diode) are conducting, leading to an increase in losses compared to the phase control thyristor tap changer. Switching at high frequency between the two taps, the chopped output voltage waveform shown in Figure 2-16 (b) is created. Due to the high switching frequency the size of the optional LC filter, used to remove the high frequency harmonics from the output waveform, can be reduced considerably.



**Figure 2-16: High frequency PWM controlled IGBT tap changer**

The main advantages are:

- Constant output voltage
- High switching frequency introduces less distortion in the output voltage, leading to smaller filter to remove unwanted harmonics.

The main disadvantages are:

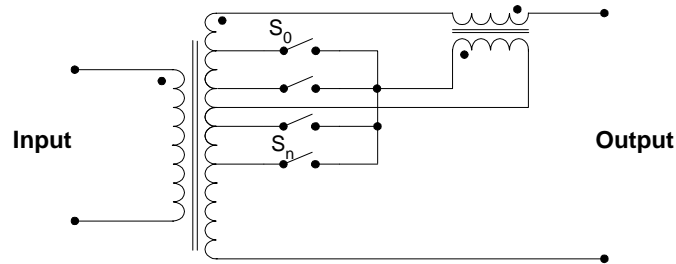
- Harmonics created in the output (without the optional LC filter)
- Higher losses than in phase control thyristor tap changer due to losses in both IGBT and series diode and additional switching losses
- High output impedance and reduced efficiency (with the use of the optional LC filter)
- Improved line transient suppression (with use of the LC filter).

### 2.2.1.D Series transformer tap changer

A variation on the basic tap changer can be obtained by adding an extra series injection transformer as shown in Figure 2-17. The total secondary winding of the main transformer is

connected to the load through the series injection transformer. By selecting an appropriate tap setting, an additional voltage can be added or subtracted to the load voltage through the injection transformer.

All of the tap changers discussed under the step control and constant control sections can be modified to incorporate the series injection topology.



**Figure 2-17: Tap changer with injection transformer**

With this topology the tap switches operate at a lower power rating, since it only adds or subtract the voltage magnitude needed to regulate the output voltage. The amount of power required depends on the input voltage range over which the voltage regulator is designed to operate.

The addition of the injection transformer could potentially lead to a more costly and less efficient regulator design, depending upon the specific application and type of switching devices used in the tap switches. Careful attention must also be given to the protection of the tap switches during excessive load current conditions. Depending on the relevant impedances in the supply line, main transformer and injection transformer high voltages might be developed across the injection transformer under short circuit conditions, which could damage the tap switches especially if the switches are solid state devices.

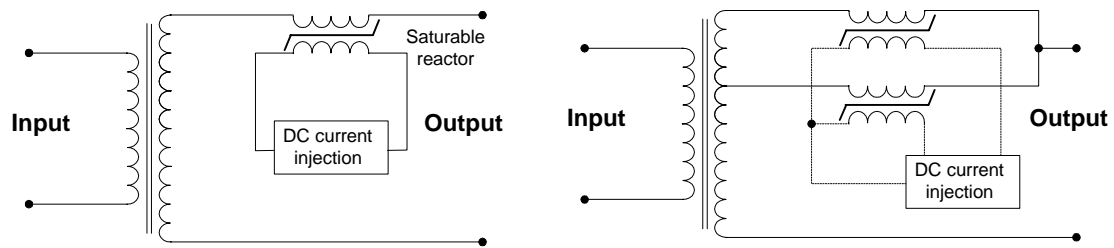
## **2.2.2 Saturable reactors**

The saturable reactor regulator controls the output voltage by varying the impedance of a reactor [12] [14]. This is accomplished by injecting a variable dc current into the reactor to control the saturation level of the core.

Two variations of the saturable type regulator are shown in Figure 2-18. In the first type a single saturable reactor is used, allowing output voltage control only if a load is present. (If no load is present, controlling the impedance of the reactor will have no influence on the output voltage.) To enable the circuit to regulate the output voltage independent of the load current, a



dual saturable reactor configuration is used, with each reactor connected to a tap on the transformer. Each reactor's saturation level and consequently their impedance is controlled individually, allowing the output voltage to be set at any level between the two tap voltages.



a) Single saturable reactor

b) Dual saturable reactor on two taps

**Figure 2-18: Saturable reactor regulator**

The main advantages are:

- Constant / smooth output voltage
- Low maintenance
- Good line transient suppression.

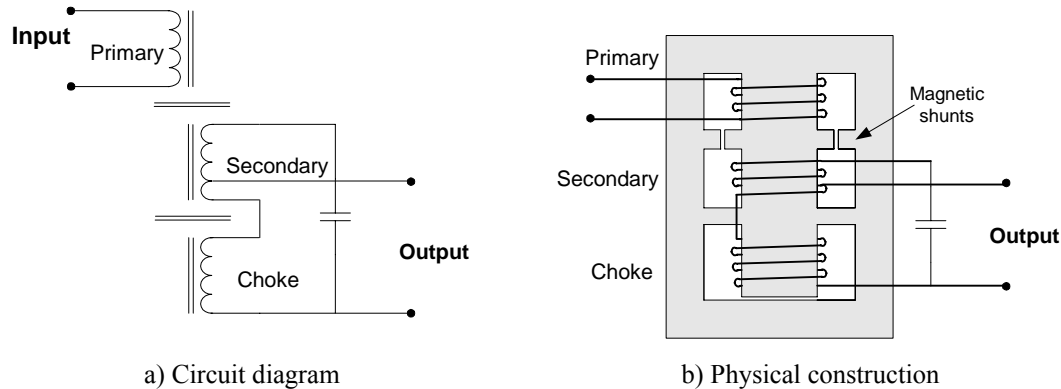
The main disadvantages are:

- Large size and weight
- Slow response time (10 cycles)
- High output impedance (as much as 30 % of load impedance), causing non sinusoidal output voltage when used with non linear loads
- Lower efficiency compared to tap changers
- Audible humming noise present
- High intensity magnetic fields can interfere with nearby sensitive equipment
- Output voltage depends on load power factor

### 2.2.3 Ferro-resonant transformer

Ferro-resonant transformers or constant voltage transformers (CVT) are essentially a special kind of transformer in which a portion of the transformer core is designed to operate in saturation. Any changes in input voltage will therefore have little effect on the core's magnetic flux density, which implies that the secondary output voltage will remain constant despite variations in the supply voltage. Because the core is operated in saturation, the output voltage is not sinusoidal and needs to be filtered.

Different topologies for CVT's can be found in literature, all of which operate on the same principle [13] [14] [19] [20] [21]. In Figure 2-19 the circuit diagram and physical construction of a CVT is shown. It consists of a primary winding, secondary winding (usually tapped), a capacitor and a choke winding (which forms part of the filter circuit).



**Figure 2-19: CVT**

The primary winding establishes the main flux in the core. To achieve a constant output voltage the core must be saturated, which implies that a large primary current will be required. To prevent this, the core is constructed using magnetic shunts such that the primary and secondary magnetic paths are separated from each other. Using a resonant circuit formed by connecting a capacitor in parallel with the secondary winding, this portion of the core can be saturated, while the primary magnetic path remains unsaturated. Connecting the choke winding in series with the capacitor provides a filter to remove unwanted harmonics and create a pure sinusoidal output.

The main advantages are:

- Constant / smooth sinusoidal output voltage
- Fast response (1-2 cycles)
- Inherent short circuit protection
- Excellent line transient suppression
- Low maintenance.

The main disadvantages are:

- Large size and weight
- High output impedance (up to 30 % of load impedance)
- Low efficiency especially under light / no load conditions (85 % under full load, 60 % with light load, up to 20 % no-load losses)

- Output voltage collapse if overloaded above 150 %. Can be over rated to handle overloads, but efficiency will decrease further
- Audible humming noise present
- High intensity magnetic fields created can interfere with nearby sensitive equipment.

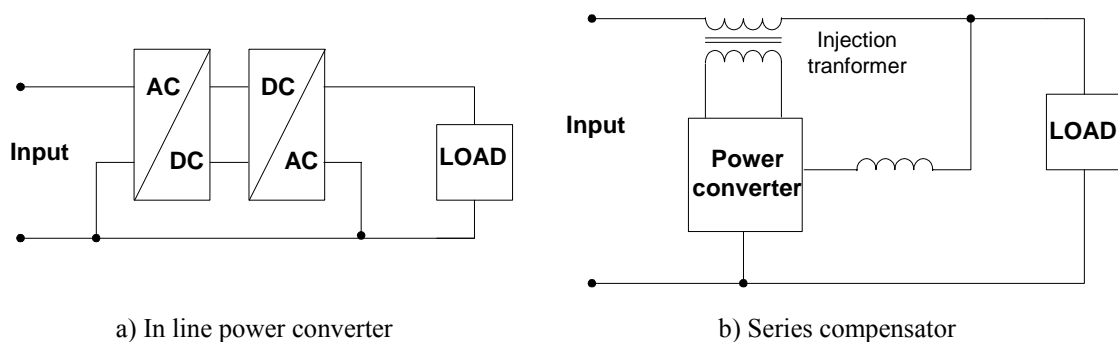
## 2.2.4 Power-electronic voltage converters

With advances in power-electronic devices and new converter developments, new circuit topologies capable of providing constant / continuous voltage regulation are being developed [3].

The following types of power converters will be discussed:

- In line AC-to-DC-to-AC power converters
- Series compensators

The in line converter shown in Figure 2-20 (a) must support the entire load current. Due to the relative high cost of power semiconductors it makes in line converters an expensive solution at the present time. The series type of compensators shown in Figure 2-20 (b) is a hybrid configuration of active and passive components. Using a power converter together with a series injection transformer provides a more cost effective solution since only a portion of the load power is processed by the power converter.

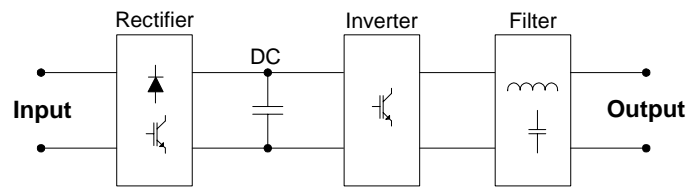


**Figure 2-20: Power-electronic voltage regulators**

### In line AC-to-DC-to-AC converter

This regulator consists of a dual conversion process with an energy storage device connecting the two stages as shown in Figure 2-21. The AC input is rectified and together with the capacitor provides a constant DC voltage. This DC voltage is converted back into AC using an inverter and a passive LC filter is used to remove the unwanted high frequency harmonics generated by the inverter. The capacitor provides the further benefit that its stored energy can be used to provide a constant output during short interruptions on the AC supply. An electronic

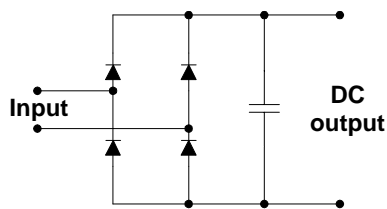
controller measures the system voltages and implements the necessary control algorithms to keep a constant output voltage with very fast response times.



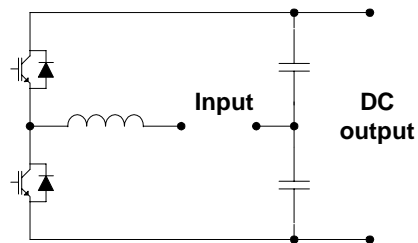
**Figure 2-21: AC-DC-AC converter**

Various circuit topologies can be used for the rectification and inverting processes. All the topologies that are discussed below apply to single phase circuits only, but they can be extended to three phase circuits.

The simplest form of rectification consists of a passive diode bridge rectifier as shown in Figure 2-22 (a). This has the disadvantage that highly distorted currents are drawn from the supply and power can only flow from the input to the output. Through use of high speed IGBT switches the bridge rectifier topology can be improved to allow for sinusoidal control of the supply current and the ability to have bi-directional power flow. The new topology is shown in Figure 2-22 (b).



a) Diode bridge rectifier

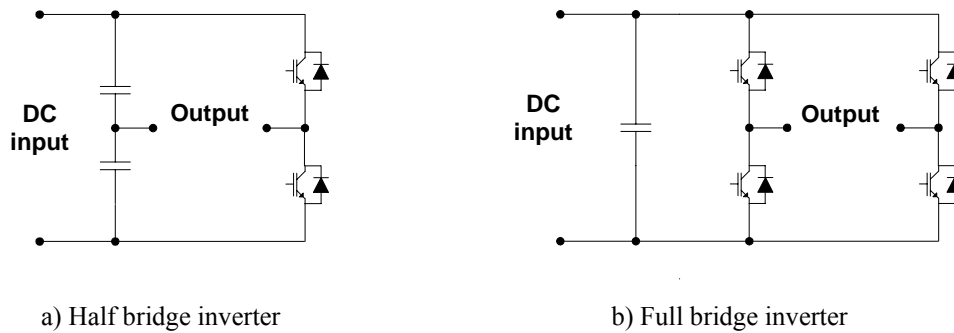


b) IGBT based active rectifier

**Figure 2-22: Rectification topologies**

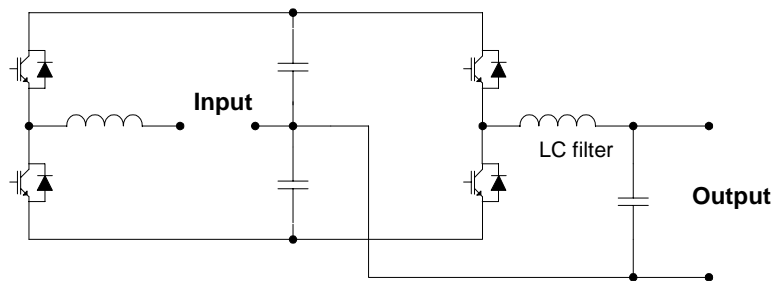
The preferred device to use in the inverter topologies (with DC input voltages in excess of 300 V) is the IGBT, because of its high switching speed and ease of control. To reconstruct an AC voltage from the DC input, the IGBT switches are controlled with high frequency pulse width modulated (PWM) switching algorithms. With further passive LC filtering a pure sinusoidal output can be created. For the inverter half bridge, full bridge or resonant topologies can be used [3] [12].

The half bridge and full bridge inverter topologies are shown in Figure 2-23 (a) and (b). In the half bridge converter only one device (IGBT or associated diode) will be conducting at any instant in time as opposed to the full bridge inverter where two devices will conduct at any instant. Due to the cost savings on the amount of IGBTs needed and the lower losses, the half bridge inverter is the preferred choice for voltage regulator applications. Resonant converters allow considerable reductions in the switching losses incurred in the IGBTs to be made, but are however fairly complex and will not be discussed further.



**Figure 2-23: Inverter topologies**

The complete in line AC-to-DC-to-AC voltage regulator converter can now be constructed by connecting the IGBT based active rectifier, half bridge inverter and LC filter together as shown in Figure 2-24 [9].



**Figure 2-24: AC-DC-AC converter topology**

The main advantages are:

- Constant / smooth sinusoidal output voltage
- Fast response (less than 1 cycle)
- No moving parts (only if no cooling fans are required)
- Can compensate for power quality problems in addition to voltage regulation
- Can present a unity power factor load to the supply independent of the load power factor.

The main disadvantages are:

- Complex circuitry and control
- Low efficiency due to double conversion process (85 %)
- Expensive
- Low overload capability to reduce system costs
- High frequency audible noise present if switching frequency is below 16 kHz.

### Series compensators

The series compensator topology is repeated in Figure 2-25 for reference [12] [14] [22]. The power converter can deliver power to a buck / boost injection transformer, which is either in phase or out of phase with the supply. Voltage can thus be added or subtracted from the supply voltage to maintain a constant load voltage. The type of power converter used can be similar to that described in the AC-DC-AC converter, with the added advantage of a reduced power rating, since the power converter supplies only a portion of the load power.

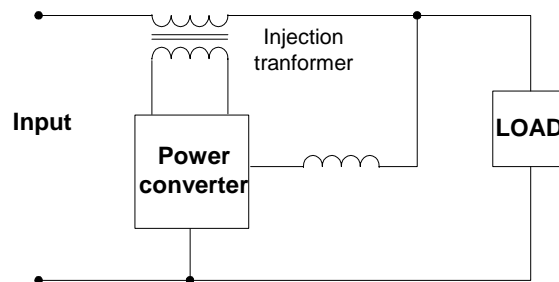


Figure 2-25: Series compensator

The main advantages are:

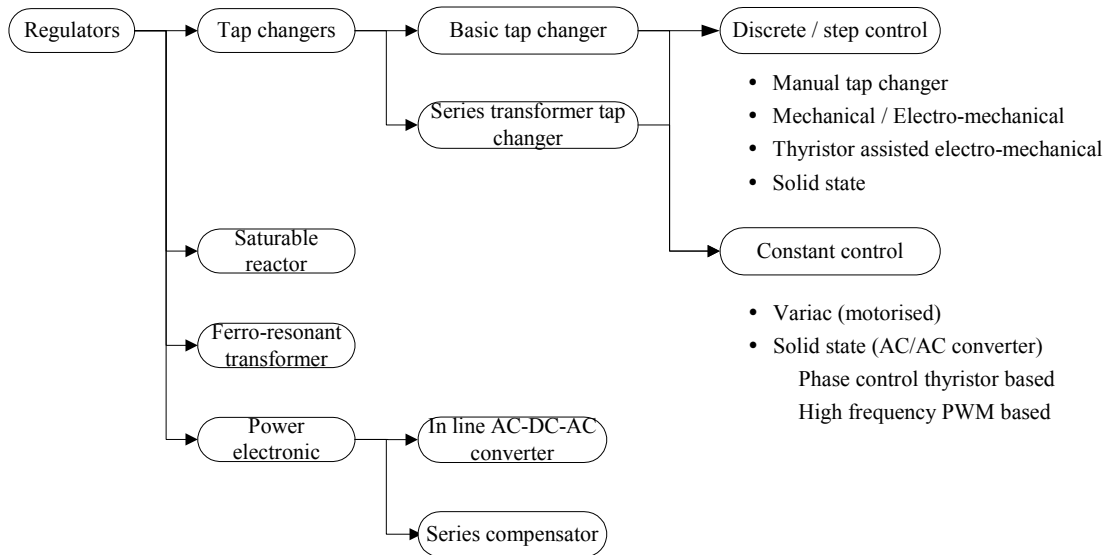
- Constant / smooth sinusoidal output voltage
- Fast response (less than 1 cycle)
- Higher efficiency than in line converters since only a portion of the load power is processed
- No moving parts (only if no cooling fans are required)
- Can compensate for power quality problems in addition to voltage regulation
- Can present a unity power factor load to the supply independent of the load power factor.

The main disadvantages are:

- Complex circuitry and control
- Expensive, but less so than in line converters
- High frequency audible noise present if switching frequency is below 16 kHz.

## 2.2.5 Summary

A number of different voltage regulator topologies were investigated and their major advantages and disadvantages compared. The different types of regulators are shown in Figure 2-26 for reference.



**Figure 2-26: Voltage regulator types**

To identify the most suitable voltage regulator topology for the intended application the following requirements / specifications must be adhered to:

- Automatic voltage regulator required
- No moving parts to minimize maintenance
- High efficiency
- Low cost and substantial overload capability

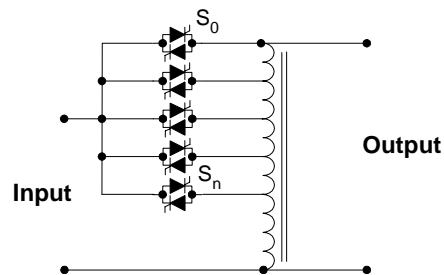
Application of these specifications results in two possible topologies that can be used:

- Basic tap changer → Step voltage control → Solid state regulator
- Series transformer tap changer → Step voltage control → Solid state regulator

With the series transformer tap changer, thyristor switches with a lower current rating can be used because only a portion of the load power needs to be injected in series with the load. The cost of the control circuitry and number of thyristor would remain identical to that used in the basic tap changer, although the thyristor commutation detection will be more difficult.

Deciding on the best solution therefore involves evaluating the losses and costs associated with the additional series transformer and lower rated thyristors, with that of the higher rated thyristors used in the basic tap changer.

After careful consideration of these factors, the basic auto-transformer based tap changer, with solid state tap switches on the primary side (as shown in Figure 2-27) was selected as the preferred topology for the application. Placing the tap switches on the primary side, allows the transformer to be disconnected entirely from the supply during periods of sustained over voltage on the supply. The inrush current magnitude at turn on can also be minimized by controlling the turn on instant.



**Figure 2-27: Auto-transformer solid state tap changer**



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## **Chapter 3**

EVR specification

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## 3 EVR specification

This chapter provides an overview of the electronic voltage regulator (EVR) developed in this thesis, by describing the features, technical specifications, construction and basic operation of the device. All the protection modes and means of identifying a specific error through the status indicator lights are highlighted. Detailed design information and results are presented in the following chapters.

### 3.1 Overview

The EVR is a 5 kVA, single phase, solid state, auto-transformer based tap changer designed for voltage regulation on long LV reticulation networks with a nominal voltage of 230 V / 240 V. Thyristors are used as tap switches due to their high overload capability compared to more modern power semiconductor switches. The device does not have any impact on the normal configuration of the LV feeder, since it is designed and programmed such that existing protection coordination is maintained.

The device is ideal in applications where slow or fast load changes induce large voltage drops on long LV feeder. The output voltage is controlled within a specified voltage band as the input voltage varies over a large voltage range. Three units can be star connected in three-phase applications and two units in dual-phase applications.

### 3.2 Features

Some of the more important features of the EVR include:

- Real-time output voltage regulation
- Field reprogrammable system
- Automatic restart procedure
- Protection against:
  - Supply over current
  - Short circuit current (coordinated)
  - Supply under voltage
  - Supply over voltage
  - Transformer over temperature
  - Thyristor over temperature
  - Lightning surges

- Overload capability – With EVR fully functional
- Extended overload capability – With EVR operating in temperature limiting mode
- Sustained supply over voltage handled without damage
- Minimal voltage distortion introduced (input & output)
- Status LED indicators
- No audible noise
- No moving parts to minimize maintenance requirements
- Environmentally sealed and protected enclosure (IP 43)
- Pole mountable enclosure
- Easy, simple installation

### 3.3 Specifications

The specifications for the EVR are listed in Table 3-1.

**Table 3-1: EVR specifications**

---

<b>Input</b>	
Supply power	5.1 kVA
Supply voltage	230 V (+/- 10 %)
Supply current	24.6 A (@ 230 V – 10 %)
Sustained over voltage	460 V
Peak current	1200 A (10 ms)
Maximum fault level (protection coordination)	500 A
Protection coordination (with 50 A, curve 1 CB)	150 A to 500 A
Voltage distortion introduced	None during normal operation Very low during tap change
Line current surges	40 kA (8/20 $\mu$ s)
<b>Output</b>	
Load apparent power	5 kVA
Load voltage	230 V (+ 4 to + 10 %)
Load current	19.8 A (@ 230 V + 10%)
Voltage step change (max)	6 %
Load power factor	0.2-1

**Overload capability<sup>1,2</sup> (cold start<sup>3</sup>) < 25 °C ambient**

400 % rated power	40 seconds
200 % rated power	Continuously (1 hour fully functional)
150 % rated power	Continuously

**Overload capability<sup>1,2</sup> (cold start<sup>3</sup>) < 45 °C ambient**

400 % rated power	40 seconds
200 % rated power	Continuously (40 minutes fully functional)
150 % rated power	Continuously (4 hours fully functional)

**Losses**

No load losses	25 W
Efficiency (Rated power @ minimum supply voltage)	98.5 %

**Dimensions**

Height including heat sink	450 mm
Width	410 mm
Depth including pole bracket	210 mm

<b>Weight</b>	32 kg
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## Notes:

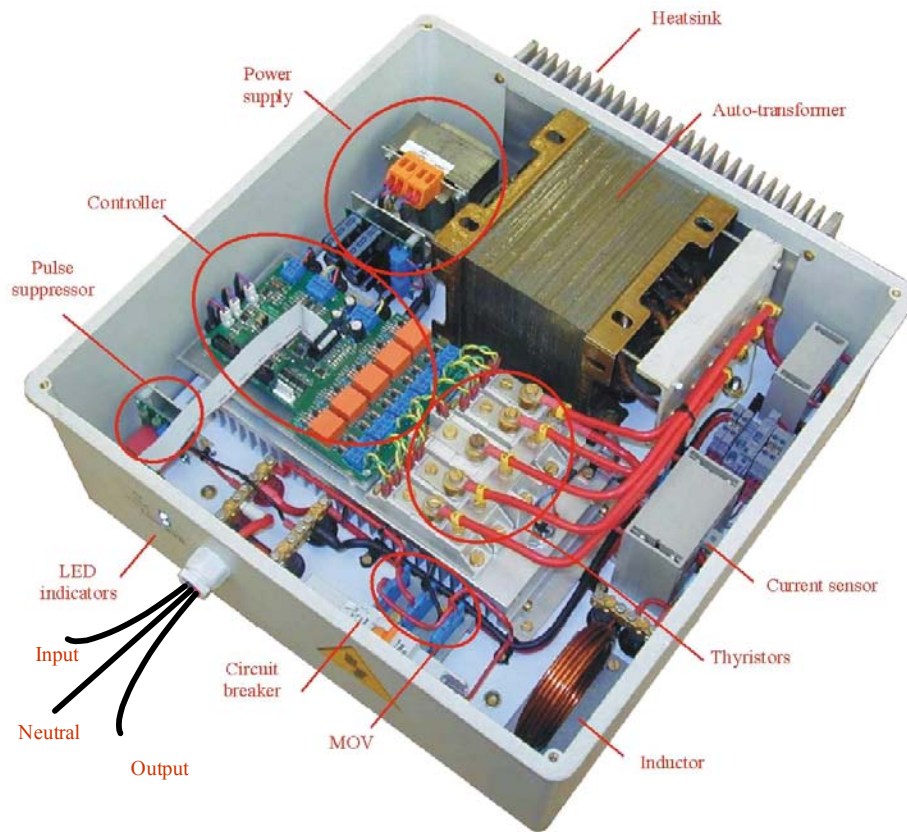
1. During overloading the EVR initially remains fully functional (implying the output voltage is kept within specification) until the transformer temperature rises too high. To extend the operating time, the transformer losses are then reduced by switching to a lower tap, implying a reduced output voltage. The EVR is now operating in temperature limiting mode and will remain in this mode until the tap switch temperature goes too high, forcing the EVR to turn off.
2. Because the output voltage is reduced while the EVR is operating in temperature limiting mode, the load power is also reduced. The EVR is thus operating at a somewhat lower power level than the indicated overload figure, while operating in temperature limiting mode.
3. Cold start implies that the EVR was turned on with the initial EVR temperature equal to the ambient temperature.

### **3.4 Construction**

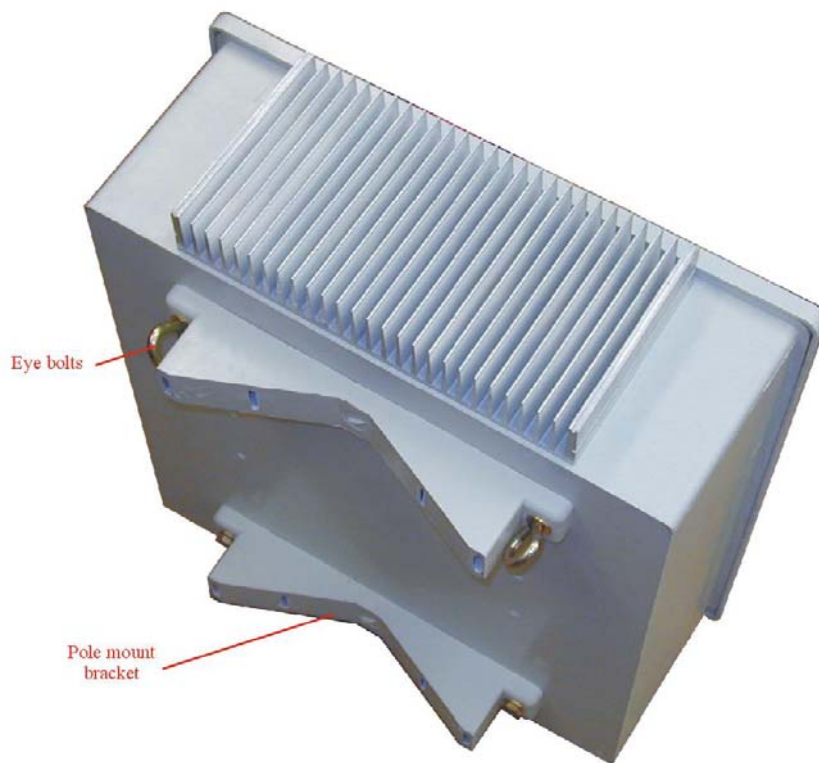
The enclosure has no ventilation holes to ensure maximum environmental protection. An external heat sink mounted on top of the enclosure is used to extract heat generated by the auto-transformer, the main source of losses, from the enclosure as shown in Figure 3-1.

The EVR is equipped with pole mount brackets on the back, enabling mounting onto a pole as shown in Figure 3-2. Two eye-bolts are provided so that the unit can be pulled up a pole and fastened.

To avoid opening of the EVR enclosure during installation (both from a tampering point of view and to ensure that the lid sealing remains optimal), input, output and neutral fly-leads are provided. These fly-leads should be connected with insulation piercing connectors (IPCs) to the feeder.



**Figure 3-1: EVR front view (cover removed)**



**Figure 3-2: EVR back view**

### 3.5 Basic operation

When the EVR is turned on, the controller evaluates the supply voltage to see if the supply voltage conforms to a predefined valid voltage range. This is indicated by turning the “OK” light emitting diode (LED) on and off repeatedly.

If the supply voltage is valid the “OK” LED will remain on and the EVR output activates, otherwise the ‘OK” LED will continue to flash until a valid supply voltage is detected. The output voltage will be regulated through tap switching by evaluating the load voltage and sequentially tapping up or down to force the output voltage to be within the specified limits.

If an error occurs during operation, the EVR will turn off all the tap switches, and remain inactive for a preset time (determined by the type of fault that has occurred). It will then automatically restart itself provided that the supply voltage is valid.

To distinguish between different error events, the “FAULT” LED on the display panel will turn on and off according to an error sequence code as shown in Figure 3-3. By counting the number of times the LED turns on / off within the sequence the error can be identified. After the sequence is completed, a 1 second delay will follow, before the sequence will repeat itself. This will continue until the restart counter associated with the particular error event clears the event and restarts the EVR.

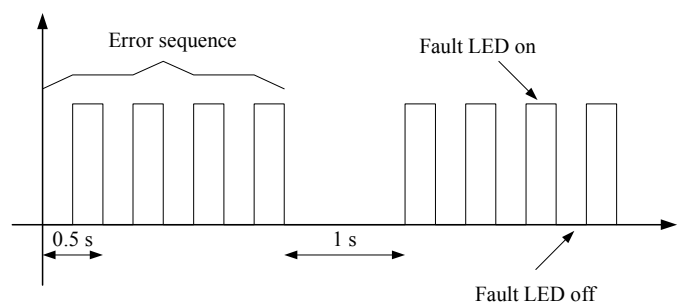


Figure 3-3: Error sequence

Overloading the EVR, above rated but below 200 % rated power, causes the transformer temperature to increase up to the point where it goes into the temperature limiting mode. In temperature limiting mode the output voltage regulation will be “relaxed” to prevent the EVR from turning off due to too high transformer temperatures. Overloading above 200 % rated power will eventually cause the EVR to turn off and restart after an appropriate time delay.

Table 3-2 shows the different operational states that can occur and how they can be identified from the LED display indicators, while Table 3-3 show all the non-operational or error states. (Operational state implies that the EVR output is active, while non-operational implies no output.)

**Table 3-2: EVR operational states**

State	State caused by	State cleared by	LED Indicators	
			OK	Fault
Normal operation			On	Off
Temperature limit mode	Transformer winding temperature above 135 °C	Transformer winding temperature below 130 °C	On	On
Thyristor heat sink temperature sensor failed <sup>1</sup>	Temperature sensor sensed as open or short circuit	SERVICING REQUIRED	On	Flashing 12x
TF temperature sensor failed <sup>1</sup>	Temperature sensor sensed as open or short circuit	SERVICING REQUIRED	On	Flashing 13x
Tap failure <sup>2</sup>	Tap other than nominal tap failed to turn on	SERVICING REQUIRED  (State automatically cleared after 20 hours)	On	Flashing 14x

Notes:

1. If the temperature sensor is not functioning, the transformer / thyristors may be damaged due to overloading. To prevent this, the over current trip level reverts to the nominal rating of 5 kVA should a sensor failure be detected.
2. If a tap other than the nominal tap fails to turn on, the nominal tap will be activated. Failure of the nominal tap will cause the unit to go into a non-operational state.



**Table 3-3: EVR non-operational states**

State	State caused by	State cleared by	LED indicators	
			OK	Fault
Supply voltage not within valid range <sup>1</sup>	Initial power-on OR Supply voltage out of range (Below 115 V or above 265 V)	Supply within range for more than 10 sec <sup>1</sup>	Flash	Off
Coordinated tripping not possible	Thyristor heat sink temperature too high to sustain fault current	*Auto-restart after 3 min	Off	Flashing 1x
Supply over current	Average supply current over a 80 sec interval is above 49 A	*Auto-restart after 30 sec	Off	Flashing 2x
Excessive fault current	Average supply current over a 10 ms interval is above 500 A	*Auto-restart after 30 sec	Off	Flashing 3x
Supply under voltage	Average supply voltage over a 10 sec interval is below 115 V	*Auto-restart after 15 sec	Off	Flashing 4x
Supply over voltage	Average supply voltage over a 10 sec interval is above 265 V	*Auto-restart after 15 sec	Off	Flashing 5x
Thyristor over temperature	Thyristor heat sink temperature is above 97 °C	*Auto-restart after 10 min	Off	Flashing 7x
Transformer over temperature	Transformer winding temperature is above 150 °C	*Auto-restart after 10 min	Off	Flashing 8x
Repetitive short circuit	Short circuit condition occurs within 20 sec of previous short circuit	*Auto-restart after 1 min	Off	Flashing 9x

State	State caused by	State cleared by	LED indicators	
			OK	Fault
Nominal tap failure	Nominal tap failed to turn on	SERVICING REQUIRED  (Auto restart at 20 min intervals)	Off	Flashing  10x
Tap shorted	Thyristor failure	SERVICING REQUIRED  (Auto restart at 2 min intervals)	Off	Flashing  11x

Notes:

1. “Within range”, indicates that the supply voltage is higher than the under voltage trip level, but lower than the over voltage trip level.

If the supply voltage is close to the under voltage trip level with the output in the off state, an under voltage error may be generated the instant that the output is activated, due to the voltage drop across the feeder. To prevent this, the supply voltage must be 5 % above the under voltage trip level, before the system will activate itself.

- \*. The EVR will only restart if the supply voltage is within the valid range

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## **Chapter 4**

### Power circuit design

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## 4 Power circuit design

The previous chapter gave an overview of the EVR to gain insight into its operation and the hardware requirements. This chapter presents a detailed design of the power circuit, together with comprehensive power loss calculations and a complete thermal design of the enclosure. Careful attention is given to the surge voltage and coordinated protection issues, to ensure the reliability of the EVR.

### 4.1 Overview

The power circuit is shown in Figure 4-1 and consists of the following components:

- Circuit breaker ( $CB_1$ )
- Surge protection ( $SA_1$ ,  $SA_2$ ,  $SA_3$ , and  $L_1$ )
- Auto-transformer ( $T_1$ )
- Thyristor switches ( $S_0$  to  $S_4$ )
- Pulse suppressor ( $R_1$ ,  $R_2$ ,  $C_1$ )
- Measurement sensors ( $Th_1$ ,  $Th_2$ ,  $CT_1$  and  $CT_2$ )

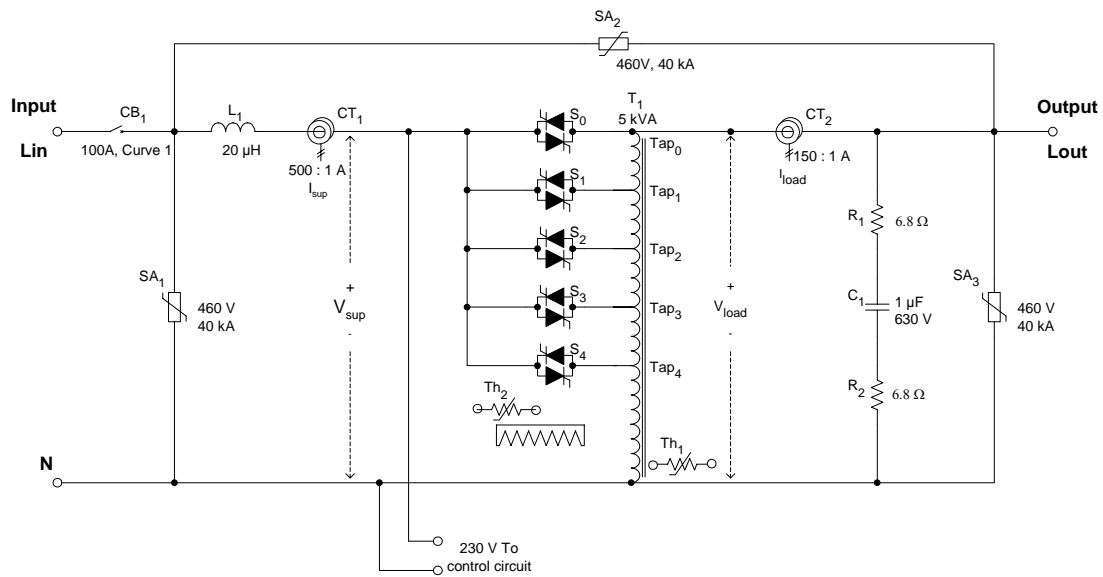


Figure 4-1: EVR power circuit

The circuit breaker on the input ( $CB_1$ ) protects the upstream line in the event of the EVR either failing to protect itself, or cannot due to too high fault currents. The circuit breaker has a slow tripping curve and a 100 A rating, which is needed to prevent the circuit breaker from interfering with the protection coordinated tripping scheme implemented in the EVR controller.

The input inductor ( $L_1$ ) operates together with surge arrestors ( $SA_1, SA_2, SA_3$ ) to protect the EVR against surge voltages. The input inductor has an air core, to prevent it from saturating. The surge arrestors are rated at  $460 V_{rms}$  and can withstand a surge current with a 40 kA magnitude (8 / 20  $\mu s$  waveform).

The auto-transformer ( $T_1$ ) has 5 tap settings on the primary and a nominal power rating of 5 kVA. All the tap settings, except for  $tap_0$ , are positioned such that the output voltage at terminal  $L_{out}$  is higher than input voltage at terminal  $L_{in}$ , i.e. the supply voltage is boosted. At  $tap_0$  (nominal tap setting) the output voltage will be equal to the input voltage, because the transformer is essentially bypassed. The auto-transformer can be overloaded to 10 kVA for extended time periods. The time period depends on the winding temperature, which is monitored by a thermistor ( $Th_1$ ) placed in-between the transformer windings. If the winding temperature is too high, the system will enter a temperature limiting mode. In this mode the controller will try to reduce the temperature in the windings by disallowing certain taps from being used, thereby lowering the losses.

To activate the transformer taps, back-to-back thyristor switches ( $S_0$  to  $S_4$ ) are used to connect the auto-transformer to the input. Due to the high current magnitudes during short circuit conditions and the need to provide coordinated tripping with other elements in the network the thyristor switches are oversized with respect to the system's rated current. To minimize the cost implication, only  $tap_0$  is oversized to such an extent, that it can sustain the load current long enough to implement coordinated tripping. Whenever a short circuit or severe overload condition arises,  $tap_0$  is automatically selected, thereby allowing the other thyristor switches to have a lower current rating.

All the thyristors are mounted onto a heat sink for cooling purposes, together with a thermistor ( $Th_2$ ) that provides over temperature protection.

A current transformer ( $CT_1$ ) on the input measures the supply current to protect the unit against overloading and implement the coordinated tripping scheme.

Due to the way in which the thyristor switches are activated, a short interruption / glitch of a few micro seconds might be present on the output voltage during each current zero crossing, especially when large inductive loads are present on the output. These glitches are caused because a small delay might exist from the time one thyristor in the back to back thyristor set

commutates, till the next thyristor is turned on. To minimize the magnitude of these glitches the glitch suppressor circuit consisting of  $R_1$ ,  $R_2$  and  $C_1$  is used.

## **4.2 Circuit breaker**

The circuit breaker (CB) on the input of the EVR protects the upstream line in the event of the EVR either failing to protect itself, or cannot due to the presence of too high fault currents.

### **4.2.1 Selection**

The EVR is allowed to operate at 10 kVA (two times rated power) for extended time periods, depending upon the auto-transformer winding temperature. The circuit breaker should therefore have a continuous rated current of at least 48.4 A. In addition to this the EVR circuit breaker should not interfere with the coordinated protection implemented in the EVR software.

During short circuits the EVR controller must keep the thyristor tap switches on long enough to trip the power utility's 50 A curve 1 circuit breaker, fitted inside the pole top box. The circuit breaker used inside the EVR must therefore not trip during this time.

To select a circuit breaker the time versus current tripping curve of the power utility's pole top circuit breaker is plotted in Figure 4-2 ("50A Curve 1" graph). The circuit breaker has a defined minimum and maximum tripping time and can trip anywhere in between these two boundaries. To guarantee that the protection coordination will operate correctly, the circuit breaker inside the EVR must remain on long enough so that the pole top box circuit breaker will trip. The tripping curve for the EVR circuit breaker should therefore not overlap with that of the 50 A circuit breaker.

Plotting the minimum and maximum tripping time curves for various circuit breakers reveals that a 100 A curve 1 circuit breaker should be used in the EVR to prevent overlapping of the tripping bands, as shown in Figure 4-2.

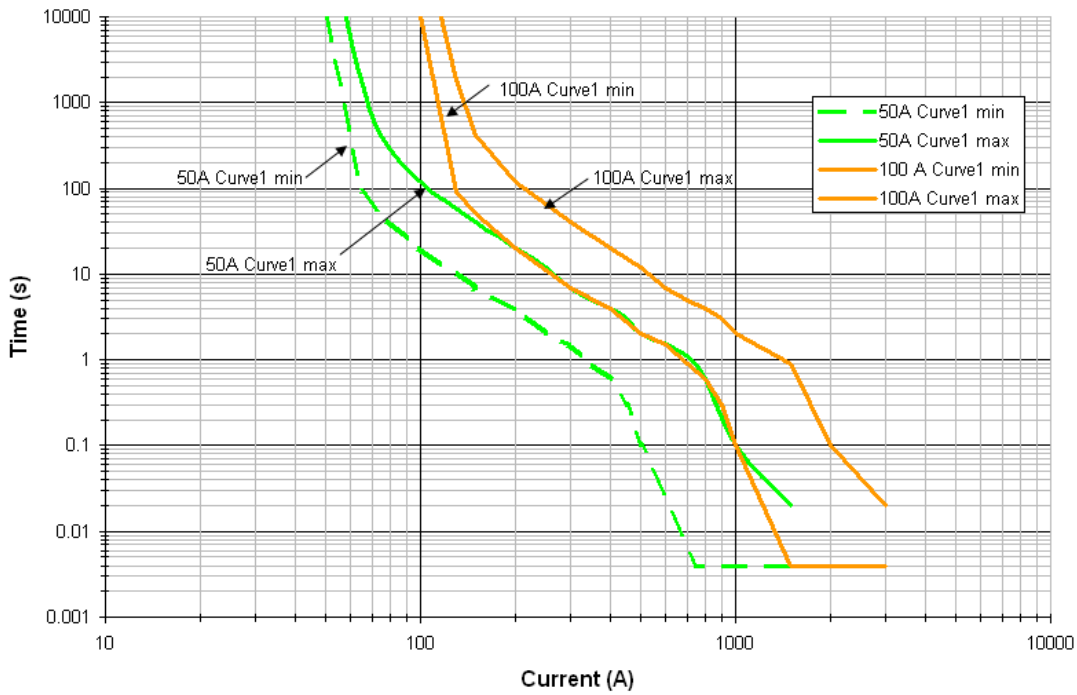
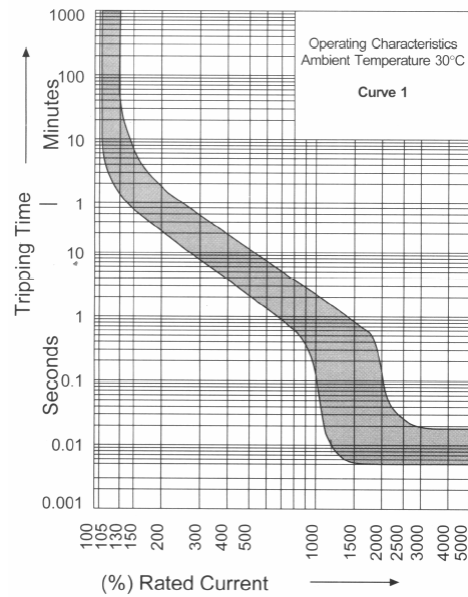


Figure 4-2: Circuit breaker tripping curves

#### 4.2.2 Fault current limitation

During an excessive fault current the controller turns off the thyristors by removing the gate pulses driving the thyristors. The thyristors will however continue to conduct until it commutates naturally, which could take up to 10 ms. If the circuit breaker cannot conduct the fault current for 10 ms it will trip.

From the normalized circuit breaker tripping characteristic in Figure 4-3, it can be seen that a circuit breaker tripping time in excess of 10 ms can only be guaranteed if the current is less than 12x the rated current of the circuit breaker.



**Figure 4-3: Circuit breaker tripping characteristic (normalized)**

Since a 100 A circuit breaker is selected for the EVR, the maximum fault current that will not trip the circuit breaker within 10 ms is 1200 A.

If the EVR is thus installed in a system with a fault level between 1.2 kA and 1.9 kA (10ms thyristor current handling ability), the circuit breaker might trip before the thyristors can commutate. This will not damage the unit, but will require an operator to reset the circuit breaker inside the EVR manually.

The situation can be overcome by installing more expensive and bulky circuit breakers with a longer tripping time characteristic, or by even removing the circuit breaker altogether. However, since the EVR is designed to be used in networks with a fault current level below 500 A, this situation should never occur, and can be ignored.

### **4.3 Auto-transformer**

Since no electrical isolation is required between the input and output of the EVR, major size, cost, weight and efficiency improvements can be gained by using an auto-transformer versus a normal isolating transformer.

#### **4.3.1 Specifications**

To specify the auto-transformer, the following points need attention:

- Tap switch location
- Power rating and number of taps



### 4.3.1.A Tap switch location

The thyristor tap switches can be placed either on the input side of the auto-transformer or on the output side. Placing the taps on the input side enables control of the transformer inrush current at turn on and enables isolation of the transformer during severe over voltage conditions.

#### Inrush current control

If the tap switches are placed on the output side of the auto-transformer, the transformer will be magnetized the instant the supply is turned on. Depending on the position in the AC cycle where the supply is turned on, a huge inrush current can develop due to core saturation. This can be explained as follow [23]:

The flux ( $\phi$ ) and therefore flux density ( $B$ ) in a coil is, according to Faraday's law, proportional to the integral of the voltage applied to it.

---

$$\phi = \frac{1}{N} \int v(t) dt$$

Where

$N =$  Number of windings

$v =$  Voltage (V)

---

When a transformer is turned on at the supply voltage peak, the maximum flux will be proportional to a quarter voltage cycle integral, as illustrated in Figure 4-4(a). If it is turned on at zero voltage, the maximum flux will be proportional to a half voltage cycle integral, illustrated in Figure 4-4(b). In the latter case the maximum flux will be double that of the flux for turn on at peak voltage.

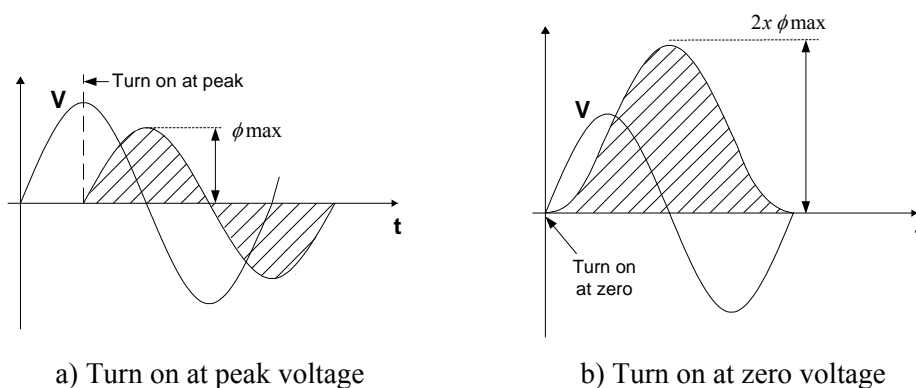


Figure 4-4: Transformer flux at turn on

The relationship between flux and current can be obtained from the non-linear B-H curve characteristic of the magnetic material used in the core construction.

By considering the following equations, it can be seen that the axis of the B-H curve is directly proportional to flux and current.

$$B = \frac{\phi}{A}$$

and

$$H = \frac{N \times I}{l}$$

**Where**

$B$  = Flux density (Tesla)

$\phi$  = Flux (Gauss)

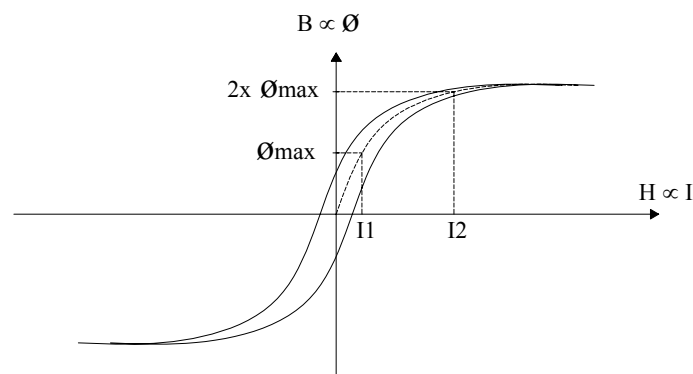
$A$  = Cross section area ( $m^2$ )

$N$  = Number of windings

$I$  = Current (A)

$l$  = Magnetic path length (m)

From Figure 4-5 it can be seen that if the flux increases beyond the linear portion of the B-H curve, it will result in a much higher current flow. This effect is called saturation of the core. If the core is driven completely into saturation, the current magnitude will only be limited by the DC resistance of the transformer windings.



**Figure 4-5: B-H curve**

The magnitude of the inrush current can be 10 to 40 times the steady state current of the transformer and cause high thermal and mechanical stress in the transformer windings and core. It can be minimized by turning the supply on near the peak of the supply voltage waveform.

If there is any remnant magnetism in the core, the saturation effect could be even worse. (Remnant magnetism refers to the nature of the core to retain some of magnetism after the magnetizing voltage has been removed.) If the remnant magnetism is positive and a voltage that causes the flux to increase in the positive direction energizes the transformer, a much smaller increase in flux will cause the transformer to go into saturation.

Placing the taps and thyristor switches on the input side allows the EVR to control the instant of turn on, thereby preventing saturation of the core.

### **Transformer isolation during supply over voltage**

If a severe supply over voltage condition exists, the auto-transformer might saturate, causing a large supply current to flow. If the thyristor switches are connected to the output side of the transformer, this current cannot be interrupted, leading to possible damage during long duration over voltage conditions. Placing the thyristor switches on the input side allows the auto-transformer to be disconnected entirely from the supply, thereby preventing any damage.

#### **4.3.1.B Power rating and number of taps**

A 5 kVA auto-transformer was used in the EVR design. Overloading of 10 kVA is allowed for extended time periods, with the time period limited through monitoring of the winding temperature. In calculating the required number of taps and their position, the following points must be considered:

- **Supply voltage range**

The larger the supply voltage range, the more taps would be required for an identical voltage step size between taps.

- **Output voltage regulation**

The tighter the output voltage regulation required, the more taps would be needed. Output voltage regulation is also directly linked to the rapid voltage change.

- **Rapid voltage change**

When the EVR changes from one tap to another, the load will experience a step in voltage. This voltage step could introduce stresses in customer appliances as well as high light intensity changes in lighting equipment. To minimize this effect the voltage step size should be as low as possible.

- **Voltage flicker**

If the load voltage is close to the maximum or minimum allowed voltage, a small increase or decrease in supply voltage will cause a tap change to occur. A small amount of flicker on the supply voltage could therefore cause the system to continuously change between two taps thereby in effect magnifying the amount of flicker the load will experience. To minimize the possibility of this occurrence, each tap position should include some margin of overlap with the previous tap position.

- **Cost**

The more taps, the more thyristor switches would be required that significantly increases the cost.

As a trade-off between the cost, output voltage regulation and rapid voltage change allowed it was decided to use 5 taps on the EVR. The nominal tap (tap 0) connects the input directly to the output with no boosting. This ensures that no steady state over voltage can occur at the customer load, as long as the supply voltage is kept within the electricity utility’s specification of 230 V + 10 %.

Using 5 taps causes a rapid voltage change of 6 % during tap changes. To minimize the frequency of tap changes, a voltage overlap or hysteresis band of 1.5 V to 2 V between tap positions is included in the design. (A detailed analysis of the tap positions and the resultant output voltage of the transformer are given in Appendix A)

#### 4.3.1.C Summary

The specifications for the auto-transformer are summarized in Table 4-1.

**Table 4-1: Auto-transformer specifications**

<b>Type:</b>	Single phase
<b>Cooling:</b>	Air
<b>Rating:</b>	5.1 kVA (With 100 W allowed for transformer losses)
<b>Voltage:</b>	Variable, 207 V <sub>rms</sub> to 253 V <sub>rms</sub>
<b>Taps:</b>	
Tap 0	253 V <sub>rms</sub>
Tap 1	242.8 V <sub>rms</sub>
Tap 2	232.5 V <sub>rms</sub>
Tap 3	223.3 V <sub>rms</sub>
Tap 4	212.1 V <sub>rms</sub>
<b>Additional:</b>	NTC thermistor used as temperature sensor to be inserted into TF windings.

### 4.3.2 Analyses

The specifications created for the auto-transformer were given to a transformer manufacturer for design and manufacturing. The manufactured transformer as shown in Figure 4-6 is analyzed below to calculate the power loss in the transformer.

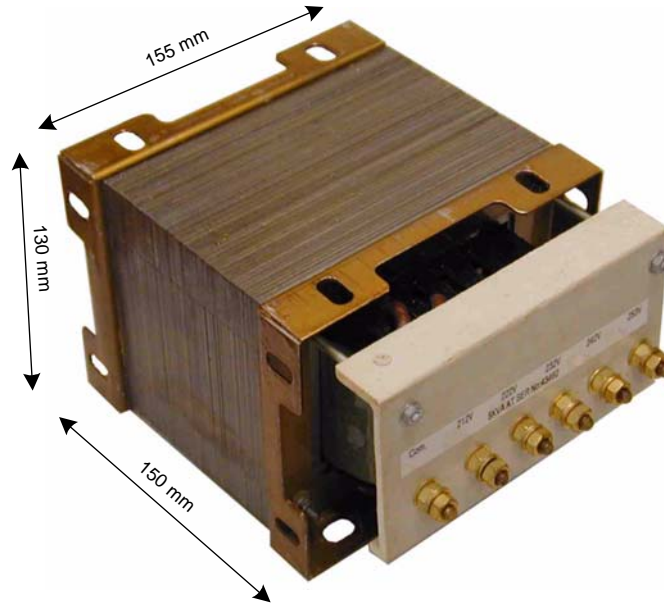


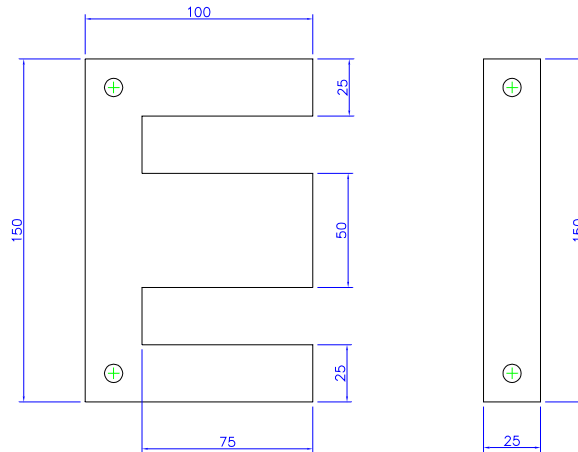
Figure 4-6: 5 kVA Auto-transformer

#### 4.3.2.A Core

The transformer core is constructed by interleaved stacking of EI laminations (named after their physical resemblance of the letters E and I) to minimize fringe flux. Each lamination has a thin non-conductive coating on both sides to minimize eddy current loss. About 200 laminations are used, each 0.5 mm thick giving a core width of approximately 102 mm. The material properties for the laminations are given in Table 4-2, while the physical dimensions are shown in Figure 4-7.

Table 4-2: Lamination material properties

Material type	Thickness	Density	Core loss at 50Hz with flux density of:		Stack weight (EI 150)
			1 T	1.5 T	
Non grain orientated silicon steel	0.5 mm	7.65 g/cm <sup>3</sup>	1.5 W/kg	3.5 W/kg	1.09 kg/cm



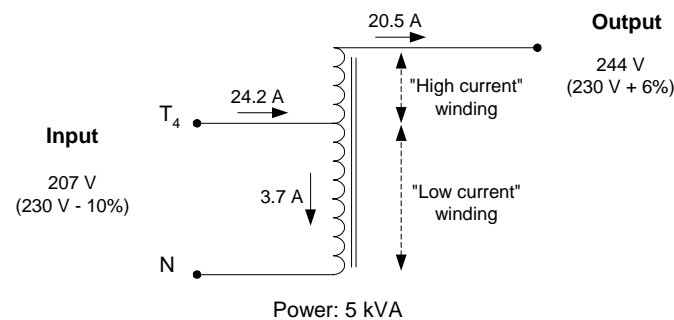
**Figure 4-7: EI lamination dimensions (in mm)**

### 4.3.2.B Windings

In an auto-transformer only a portion of the power is transformed via the magnetic flux in the core. This leads to a smaller physical size and lower losses compared to an isolation transformer.

In the EVR the taps on the auto-transformer is arranged such that the supply voltage is normally stepped up, excluding tap 0 that essentially bypasses the transformer. The basic working of the auto-transformer is illustrated in Figure 4-8, where the minimum supply voltage of 207 V is applied to tap 4 and boosted to 244 V at the output.

For the nominal 5 kVA power rating, the currents flowing through the different sections of the auto-transformer are indicated. The section of winding between tap 4 and neutral conducts a small magnetizing current of 3.7 A, while the winding between tap 4 and the output conducts 20.5 A.



**Figure 4-8: Auto-transformer**

The low current part of the transformer winding (between the tap 4 and neutral) consists of 174 windings; wound using a circular, enameled coated, copper conductor with a diameter of 1.5 mm. This leads to a current density of 2.1 A/mm<sup>2</sup> and an estimated winding length of 64 m.

The high current part of the winding (between tap 4 and the output) consists of 34 windings; wound using a rectangular copper conductor with a cross section dimension of 5.6 x 2.24 mm. The current density in this winding is 1.64 A/mm<sup>2</sup>, with an estimated winding length of 16 m.

The low and high current winding properties are summarized in Table 4-3.

**Table 4-3: Auto-transformer winding data**

Winding	Conductor	Cross section area	Turns	Estimated length	Current density	
					5 kVA	10 kVA
Low current winding	1.5 mm diameter Round	1.77 mm <sup>2</sup>	174	64 m	2.1 A/mm <sup>2</sup>	4.4 A/mm <sup>2</sup>
High current winding	5.6 x 2.24 mm Rectangular	12.54 mm <sup>2</sup>	34	16 m	1.64 A/mm <sup>2</sup>	3.22 A/mm <sup>2</sup>

### 4.3.2.C Losses

The losses in the auto-transformer are primarily due to:

- Core losses – Caused by the hysteresis and eddy currents
- Copper losses – Caused by the electrical resistance of the windings

#### Core loss

The core loss consists of the hysteresis and eddy current losses, both caused by the varying magnetic flux inside the core and strongly dependent on the material used in the laminations, the flux density in the core and to a lesser extent the core temperature. The core loss is largely independent of the load on the auto-transformer. Loading can however lead to an indirect change in core loss, because the magnetic properties of the core material will change with a change in core temperature, caused by the losses in the transformer core and windings.

The hysteresis loss can be reduced by using laminations made from a higher quality material with a narrower BH curve, for example grain orientated silicon steel. This is however more expensive. Eddy current losses, which depends on the electrical conduction properties of the material used, can be reduced through material choice as well as using thinner laminations.

The core loss for the material used in the auto-transformer can be calculated using the lamination material properties in Table 4-2 if the flux density in the core is known. To calculate the flux density, Faraday's law can be used.

Faraday's law states that a voltage will be induced in a winding if it is placed in a time varying magnetic field.

---

$e = N \frac{d\Phi}{dt}$	<p><b>Where</b> <span style="float: right;">(4-1)</span></p> <p><i>e</i> = Induced voltage (V)  <i>N</i> = Number of windings  <i>Φ</i> = Flux (Gauss)  <i>t</i> = Time (s)</p>
--------------------------	---

---

Assuming that the flux inside the transformer will be sinusoidal, the flux can be written as:

---

$\Phi = \Phi_{\max} \sin(2\pi ft)$	<p><b>Where</b> <span style="float: right;">(4-2)</span></p> <p><i>Φ<sub>max</sub></i> = Maximum flux (Gauss)  <i>f</i> = Frequency (Hz)</p>
------------------------------------	--

---

The relationship between flux and magnetic flux density is given by:

---

$B = \frac{\Phi}{A}$	<p><b>Where</b> <span style="float: right;">(4-3)</span></p> <p><i>B</i> = Flux density (T)  <i>Φ</i> = Flux (Gauss)  <i>A</i> = Area (m<sup>2</sup>)</p>
----------------------	---

---

Substituting the flux obtained from using Equation (4-2) into Equation (4-1), and noting the relationship between flux and flux density from Equation (4-3), Faraday's law can be rewritten as follow.



---


$$E = 4.44 f N A B_{\max} \quad \text{Where} \quad (4-4)$$

$E = \text{RMS induced voltage (V)}$

$f = \text{Frequency (Hz)}$

$N = \text{Number of windings}$

$A = \text{Core cross section area (m}^2\text{)}$

$B_{\max} = \text{Maximum flux density (T)}$

---

Through rewriting this equation  $B_{\max}$  can be obtained.

---


$$B_{\max} = \frac{E}{4.44 f N A} \quad (4-5)$$


---

With the given transformer, the flux density inside the core is thus dependent on the supply voltage magnitude and frequency. Since the frequency in the EVR is fixed at 50 Hz, the flux density will only be influenced by the supply voltage magnitude.

The maximum flux density, leading to the maximum core loss, will occur at the maximum supply voltage of 253 V. However, at the maximum supply voltage the EVR will be using tap 0, effectively bypassing the transformer, leading to minimal copper loss. For the entire transformer the maximum loss will thus occur at the highest supply voltage that will result in tap 0 being selected, which is 215 V (refer to Appendix A on page 229). Using Equation (4-5) the flux density can be calculated as:

---


$$B_{\max} = 1.09 \text{ Tesla}$$

**With**

$E = 215 \text{ V}$

$f = 50 \text{ Hz}$

$N = 174 \text{ windings}$

$A = 0.0051 \text{ m}^2 \text{ (} 50 \times 102 \text{ mm)}$

---

With the aid of the lamination material properties in Table 4-2, the core loss can be calculated by first calculating the core mass and then multiplying it with the “loss per weight” constant in the table at the appropriate flux density.

Noting that the core used in the EVR has a width of 102 mm, the core mass can be calculated using the indicated mass figure of 1.09 kg/cm, which gives a total mass of 11.12 kg. The core loss at a flux density of 1.09 Tesla is linearly approximated from the indicated losses at 1 Tesla and 1.5 Tesla to be 1.86 W/kg. Multiplying this with the core mass gives core losses of 20.7 W.

## Copper loss

The copper loss is caused by the electrical resistance of the copper conductors used in the windings and is proportional to the square of the current through the winding. Since the resistance of copper increases with an increase in temperature, the losses are higher at higher temperatures.

To calculate the copper loss, the resistance of each section of the winding will be calculated at a temperature of 20 °C. The resistance values will then be adjusted since the temperature in the windings will be much higher than 20 °C once the transformer is loaded. Because the actual winding temperature under load is not known, an estimated temperature value will be used. The new resistance value, based on the estimated winding temperature, will then be used to calculate the losses.

The DC resistance of an electrical conductor is given by:

---

$$R = \frac{l\rho}{A}$$
$$= \frac{l\left(\frac{1}{\sigma}\right)}{A}$$

**Where** (4-6)

$R$  = Resistance ( $\Omega$ )  
 $l$  = Length of conductor (m)  
 $\rho$  = Resistivity ( $\Omega m$ )  
 $A$  = Cross section area ( $m^2$ )  
 $\sigma$  = Conductivity (S/m)

---

The conductivity of copper depends strongly on impurities in the metal and is approximately  $59.6 \times 10^6$  S/m at 20 °C. Since conductivity is the inverse of resistivity, the resistance for each winding at 20 °C can be calculated from Equation (4-6) using the winding data supplied in Table 4-3.

To adjust the resistance to account for the higher winding temperature the following relationship can be used.

---

$$R = R_0[1 + \alpha(T - T_0)]$$

**Where** (4-7)

$R$  = Resistance at temperature  $T$   
 $R_0$  = Resistance at temperature  $T_0$   
 $\alpha$  = Temperature coefficient of resistance  
 $T$  = Temperature (°C)

---

The temperature coefficient of resistance ( $\alpha$ ) is not a constant, but depends on the temperature and type of material as shown below.

$$\alpha = \frac{1}{234.5 + T} \quad \text{Where} \quad (4-8)$$

$\alpha =$  Temperature coefficient of resistance at temperature  $T$   
 $T =$  Temperature ( $^{\circ}\text{C}$ )

(The factor 234.5 applies only to copper)

Because  $\alpha$  is not constant, an iterative approach is followed to calculate the winding resistance at a higher temperature. With the resistance at 20  $^{\circ}\text{C}$  calculated from Equation (4-6), the resistance at a higher temperature is calculated by increasing the temperature in small steps. At each step, a new  $\alpha$  factor is calculated, which is used in Equation (4-7) to obtain the new resistance at this temperature.

The resistance values for the windings (calculated using this iterative approach) and their losses at 5 kVA and 10 kVA power levels are summarized in Table 4-4, assuming a winding temperature of 90  $^{\circ}\text{C}$  and 130  $^{\circ}\text{C}$  at the respective power levels.

**Table 4-4: Auto-transformer winding resistance & loss**

Winding	Resistance 20 $^{\circ}\text{C}$	5 kVA			10 kVA		
		Resistance 90 $^{\circ}\text{C}$	Current	Power loss	Resistance 130 $^{\circ}\text{C}$	Current	Power loss
Low current winding	607.71 m $\Omega$	774.2 m $\Omega$	3.7 A	10.6 W	869.3 m $\Omega$	7.4 A	47.6 W
High current winding	21.41 m $\Omega$	27.3 m $\Omega$	20.5 A	11.5 W	30.6 m $\Omega$	41 A	51.4 W
Total				22.1 W			99 W

## Total loss

By adding the core loss and copper loss together, the total loss in the auto-transformer at 5 kVA and 10 kVA can be calculated as given in Table 4-5.

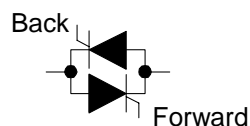
**Table 4-5: Auto-transformer losses**

	@ 5 kVA	@ 10 kVA
<b>Core loss</b>	20.7 W	20.7 W
<b>Copper loss</b>	22.1 W	99 W
<b>Total loss</b>	42.8 W	119.7 W

This gives the auto-transformer an efficiency of 99.1 % at the rated power level of 5 kVA and 98.8 % at 10 kVA.

## 4.4 Tap switches

Due to the robust nature of thyristors, they were chosen as the technology to implement in the tap switches. Since a thyristor can conduct in one direction only, back-to-back thyristors are used to realize each tap switch as shown in Figure 4-9. One thyristor will conduct in the positive AC half cycle, while the other will conduct in the negative half cycle.



**Figure 4-9: Back-to-back thyristor switch**

In selecting and designing the thyristor tap switches the following aspects are discussed:

- Thyristor selection
- Cooling design
- Over temperature protection
- Overloading capability

## 4.4.1 Selection

### Package

Power thyristors are available in stud and module packages as shown in Figure 4-10 [25].



**Figure 4-10: Thyristor packages**

Although stud mount thyristors are generally less expensive than modules, they introduce voltage isolation problems since their outer metal casing is at a live electrical potential (either connected to the anode or cathode of the thyristor). This requires a number of electrically isolated heat sinks to be used for cooling, since the thyristor casings will be at different electric potentials.

Thyristor modules (containing two thyristors per modules) have an electrically isolated base plate, enabling all the thyristors to be mounted onto a single heat sink. Since only one thyristor module is conducting at any instant in time, the entire heat sink surface is available to cool any of the modules.

In the case of stud mount thyristors, electrically isolating the heat sinks from each other also introduces thermal isolation between them. Each thyristor heat sink would therefore need to be approximately half the size (only one thyristor, therefore half the losses) of the heat sink that will be needed if thyristor modules are used. In total a considerable bigger heat sink would thus be required if stud mount thyristors are used. Based on this, thyristor modules are considered to be a better choice.

### Current rating & losses

The thyristors must be capable of conducting a continuous current of 48.4 A (10 kVA power level), and have enough capacity to implement a coordinated protection scheme with the power utility's pole top box circuit breaker.

To minimize the cost implication, only tap 0 is oversized to such an extent that it can sustain the load current long enough to implement the required coordinated tripping. Whenever a short circuit or severe overload condition arises, tap 0 is automatically selected, thereby allowing the other thyristor switches to have a lower current rating.

Selection of the thyristor is based on the design parameters shown in Table 4-6:

**Table 4-6: Thyristor switch design parameters**

	<b>Tap 0</b>	<b>Tap 1, 2, 3 &amp; 4</b>
<b>Continuous power</b>	10 kVA	10 kVA
<b>Supply voltage: Min</b>	207 V (230 V - 10%)	207 V (230 V - 10%)
<b>Max</b>	253 V (230 V + 10%)	253 V (230 V + 10%)
<b>Current</b>	48.4 A	48.4 A
<b>Short circuit current</b>	As high as possible	As high as possible
<b>Protection coordination</b> (with 50 A curve 1 circuit breaker)	YES	NO
<b>Cooling</b>	Natural cooling only	Natural cooling only
<b>Cost</b>	Minimum	Minimum

The 10 kVA continuous overload capability required from the EVR, relate to a required thyristor current of 48.4 A<sub>rms</sub> at the minimum supply voltage of 207 V<sub>rms</sub>.

Considering all the design parameters above, it was decided to use the SKKT 162/12E and SKKT 106/12E dual thyristor modules from SEMIKRON [25] for tap 0 and taps 1 to 4 respectively.

The thyristor modules have a RMS current rating of 250 A and 180 A respectively, which might seem excessive. These ratings are however only applicable to a system with optimum forced air cooling, unlike the EVR which utilizes natural cooling in an enclosed space.

Both modules have a reverse blocking voltage of  $1200 V_{peak}$ , which again seems to be excessive. Using thyristors with a higher reverse blocking voltage does however lead to a higher  $dv/dt$  commutation capability which can simplify or altogether prevent the use of commutation snubbers in the design.

The conduction losses can be obtained directly from the datasheets as shown in Figure 4-11, where the SKKT 106/12E thyristor module together with its losses at various RMS currents is shown. With a RMS current of 48.4 A, the losses will be approximately 45 W.

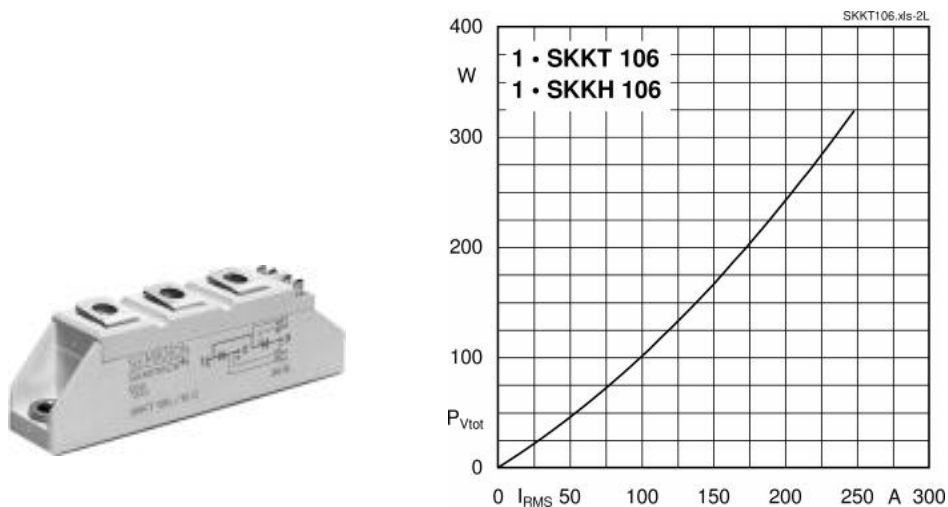


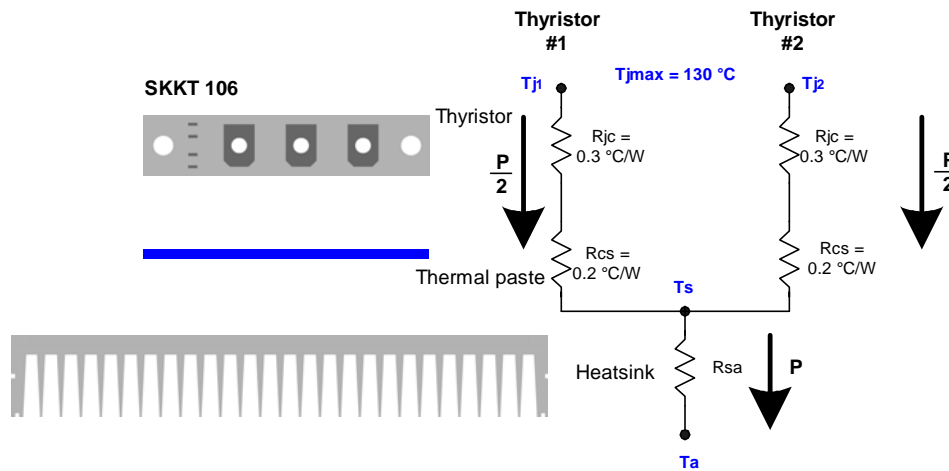
Figure 4-11: SKKT 106/12E Thyristor module – Losses

#### 4.4.2 Cooling

Since only one tap switch is on at any instant in time, the steady state thermal design of the heat sink is fairly simple and based only on conduction losses. (Due to the low frequency of operation, switching losses can be ignored). Additional loss of approximately 0.25 W is introduced in the gate by the gate drive circuitry.

Both types of thyristor modules used are subjected to the same steady state operating currents. Since the SKKT106 have a lower rated current, it would be sufficient to do the steady state heat sink design for this thyristor module alone.

To perform a thermal analysis, a thermal model for the thyristor module is needed. This thermal model is shown in Figure 4-12, where “thyristor #1” and “thyristor #2” represents the two thyristors contained within the thyristor module.



**Figure 4-12: Thyristor cooling - thermal model (SKKT 106)**

To design the heat sink, the ambient temperature ( $T_a$ ) inside the EVR is needed. The internal ambient temperature depends on the amount of losses inside the EVR (mainly caused by the auto-transformer and thyristors) and the rate at which the losses can escape through the enclosure. As this process is quite complex the internal temperature was estimated with the help of practical tests to be a maximum of 85 °C.

The relationship between power and temperature can be expressed as:

$$\Delta T = PR_{th}$$

**Where** (4-9)

$\Delta T$  = Change in temperature (°C)

$P$  = Power dissipated (W)

$R_{th}$  = Thermal resistance (°C/W)

Using this relationship and noting that the total conduction losses for the SKKT106 thyristor module operating at two times rated power (48.4 A) is equal to 45 W, the required heat sink thermal resistance ( $R_{sa}$ ) can be calculated using the thermal model. Since only one thyristor inside the thyristor module is conducting at any instant in time, the model can be evaluated by looking at only one thyristor switch. The required thermal resistance can therefore be calculated as follow:



---


$$R_{sa} = \left( \frac{T_{j2} - T_a}{P} \right) - \frac{(R_{jc} + R_{cs})}{2} \quad \text{Where} \quad (4-10)$$

$$= 0.75 \text{ } ^\circ\text{C/W}$$

$$T_{j2} = T_{jmax} = 130 \text{ } ^\circ\text{C}$$

$$T_a = 85 \text{ } ^\circ\text{C}$$

$$P = 45 \text{ W (2x Rated power)}$$

$$R_{jc} = 0.3 \text{ } ^\circ\text{C/W}$$

$$R_{cs} = 0.2 \text{ } ^\circ\text{C/W}$$


---

Using a HE4 heat sink from SEMIKRON with a length of 130 mm (long enough to provide mounting space for all 5 thyristor modules) a thermal resistance of 0.5 °C/W can be obtained for natural cooling. Since this thermal resistance is better than the required 0.75 °C/W, the maximum junction temperature can be recalculated using Equation (4-10) to be 118.8 °C.

### 4.4.3 Over temperature protection

To protect the thyristors against destruction during severe and extended overloading, a thermistor is mounted onto the heat sink to measure the heat sink temperature. The output from the thermistor is monitored by the controller, thereby enabling the controller to protect the thyristors.

During steady state overloading, the heat sink temperature ( $T_s$ ) can be calculated from the thyristor thermal model in Figure 4-12 as follows:

---


$$T_s = T_a + (P \times R_{sa}) \quad \text{Where} \quad (4-11)$$

$$= 107.5 \text{ } ^\circ\text{C}$$

$$T_a = 85 \text{ } ^\circ\text{C}$$

$$P = 45 \text{ W}$$

$$R_{sa} = 0.5 \text{ } ^\circ\text{C/W}$$

$$(Actual \text{ heat sink used})$$


---

The heat sink temperature of 107.5 °C represents the temperature directly underneath the thyristor chip that is conducting. Since it is impossible to mount the thermistor directly underneath the thyristor chip, the temperature at the thermistor location will be different from the value calculated above. Allowing for a 10 % difference in temperature between these two locations implies a trip level setting of 96.8 °C.

### 4.4.4 Overload capability

During overload / short circuit conditions the EVR will switch to tap 0, which is equipped with the more powerful SKKT 162 thyristors. To implement the coordinated protection scheme, the current versus time capability of the thyristors during short duration overloads is needed. To

obtain this, the power dissipated, current junction temperature, thyristor and heat sink transient thermal impedance, and the duration of the overload are needed.

#### 4.4.4.A Power dissipation

Since the thyristor loss graph given in the datasheets does not extend far enough, the thyristor loss at high current magnitudes are calculated based on the forward conduction characteristic of the thyristor as shown in Figure 4-13 and Equation (4-12).

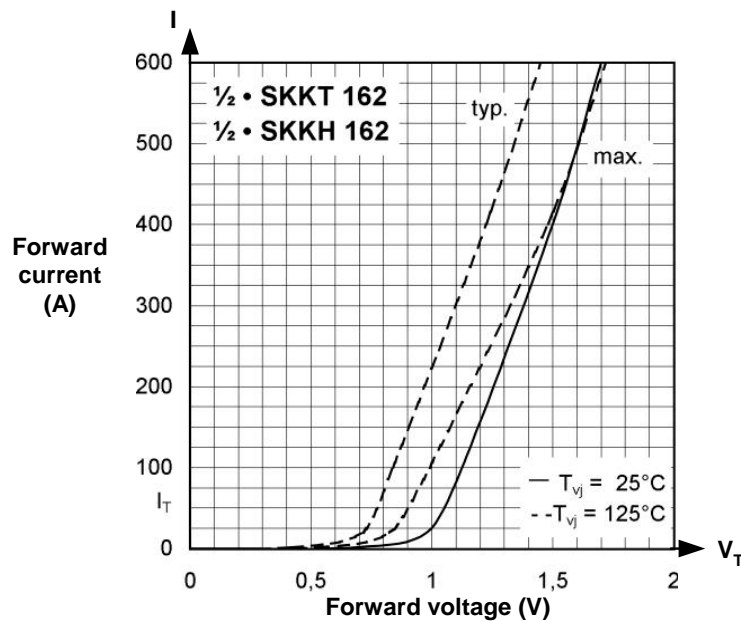


Figure 4-13: Thyristor forward characteristic (SKKT 162)

$$P = V_T I$$

Where

(4-12)

$P$  = Power (W)

$V_T$  = Thyristor forward voltage (V)

$I$  = Thyristor current (A)

#### 4.4.4.B Current junction temperature

The thyristor overload capability at a specific time instant will depend on the difference between the current junction temperature and the maximum allowable junction temperature. The current junction temperature in turn depends on the current operating conditions (thyristor current and internal ambient temperature) and will therefore vary over time. To calculate the junction temperature, a thermal model identical to that used in designing the thyristor heat sink is used. The model is repeated in Figure 4-14 with the new parameters for the SKKT 162 thyristor included.

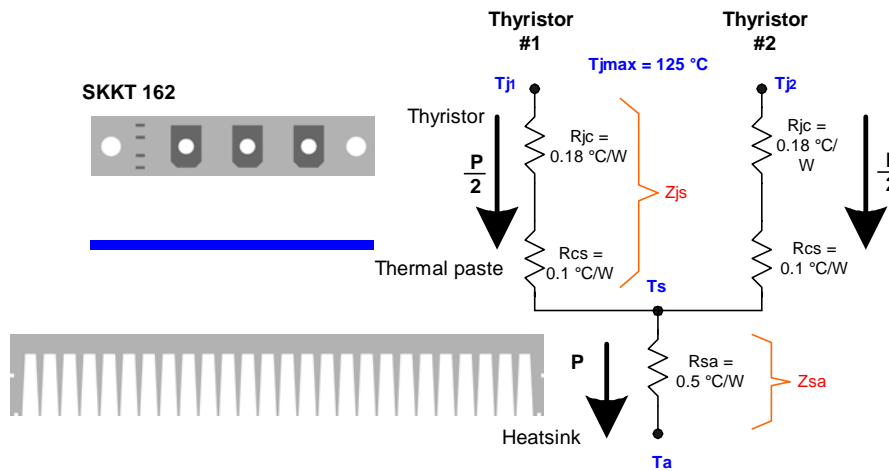


Figure 4-14: Thyristor cooling - thermal model (SKKT 162)

#### 4.4.4.C Thyristor transient thermal impedance

The transient thermal impedance defines how the junction to heat sink or junction to case thermal impedance varies with regard to the time duration of a power pulse applied to the thyristor. For short time power pulses, the thyristor can conduct much higher currents before the maximum junction temperature will be exceeded.

In Figure 4-15 both the junction to heat sink ( $Z_{th(j-s)}$ ) and junction to case ( $Z_{th(j-c)}$ ) transient thermal impedances for the SKKT 162 thyristor module are shown.

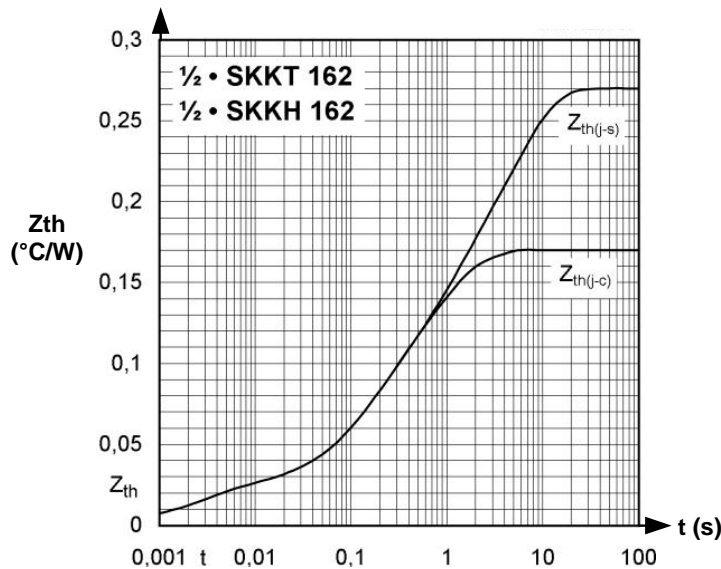


Figure 4-15: Transient thermal impedance (SKKT 162)

#### 4.4.4.D Heat sink transient thermal impedance

For short time power pulses the thermal resistance of the heat sink onto which the thyristors are mounted also varies from the steady state thermal resistance. Because no data is available on the transient thermal impedance of the heat sink the temperature increase due to a power pulse is estimated by using the specific heat capacity of the heat sink. Assuming that none of the heat absorbed by the heat sink is transferred from the heat sink to the surrounding air, a conservative estimation of the heat sink temperature is made.

The specific heat capacity ( $c$ ) of a material is the quantity of energy ( $Q$ ) needed to change the temperature ( $T$ ) of 1 kg of the material by 1 °C. Using this definition Equation (4-13) can be written, which shows the relationship between the temperature change in a material with a specific mass after a certain amount of energy has been absorbed.

---

$\Delta T = \frac{Q}{mc}$	<b>Where</b>	
And noting that $P = \frac{Q}{t}$	$\Delta T = \text{Change in temperature } (^{\circ}\text{C})$	(4-13)
$\Delta T = \frac{Pt}{mc}$	$m = \text{Material mass (kg)}$	
	$c = \text{Specific heat capacity (Jkg}^{-1}\text{^{\circ}C}^{-1}\text{)}$	
	$P = \text{Power (W)}$	
	$t = \text{time (s)}$	

---

For aluminium the specific heat capacity is 900 Jkg<sup>-1</sup>°C<sup>-1</sup>, while the mass of the HE4 heat sink used is 1.898 kg.

#### 4.4.4.E Thyristor overload capability

To calculate the thyristor overload capability, the first step involves calculating the current junction temperature ( $T_j$ ) under the specified operating conditions (that is at the time instant before the overload is experienced). This is done by using the thyristor thermal model in Figure 4-14. The difference between the maximum allowable junction temperature ( $T_{j\text{max}}$ ) and the current junction temperature represents the margin with which the temperature across the thyristor and heat sink may increase during the overload.

Subsequently, the transient thermal impedance of the thyristor corresponding with the specified overload duration is determined from Figure 4-15. Using this together with the junction temperature, the amount of power that can be dissipated can be calculated as shown in Equation (4-14).

---

Define

$$\Delta T = (T_{j\max} - T_j)$$

Then from Figure 4-14:

$$\begin{aligned}\Delta T &= \frac{P}{2}(Z_{js}) + P(Z_{sa}) \\ &= \frac{P}{2}(Z_{js}) + \frac{Pt}{mc}\end{aligned}$$

Thus

$$\therefore P = \frac{(T_{j\max} - T_j)}{\frac{Z_{js}}{2} + \frac{t}{mc}}$$

Where

$T_{j\max}$  = Max junction temperature ( $^{\circ}\text{C}$ )

$T_j$  = Current junction temperature ( $^{\circ}\text{C}$ )

$P$  = Power dissipated ( $\text{W}$ )

$Z_{js}$  = Thyristor transient thermal impedance ( $^{\circ}\text{C}/\text{W}$ )

$Z_{sa}$  = Heat sink transient thermal impedance ( $^{\circ}\text{C}/\text{W}$ )

$t$  = Time duration of overload ( $\text{s}$ )

$m$  = Mass of HE4 heat sink (1.898 kg)

$c$  = Specific heat capacity of aluminium ( $900 \text{ Jkg}^{-1}\text{C}^{-1}$ )

(4-14)

---

To obtain the fault current that can be handled for the specified time duration, the thyristor forward conduction characteristics in Figure 4-13 together with Equation (4-12) can be used to relate the fault current to the calculated power.

Using the principles as described above, the thyristor overload capability (subject to an internal ambient temperature of  $45^{\circ}\text{C}$  and a thyristor current of 25 A and 50 A prior to the overload occurring) is calculated as shown in Figure 4-16.

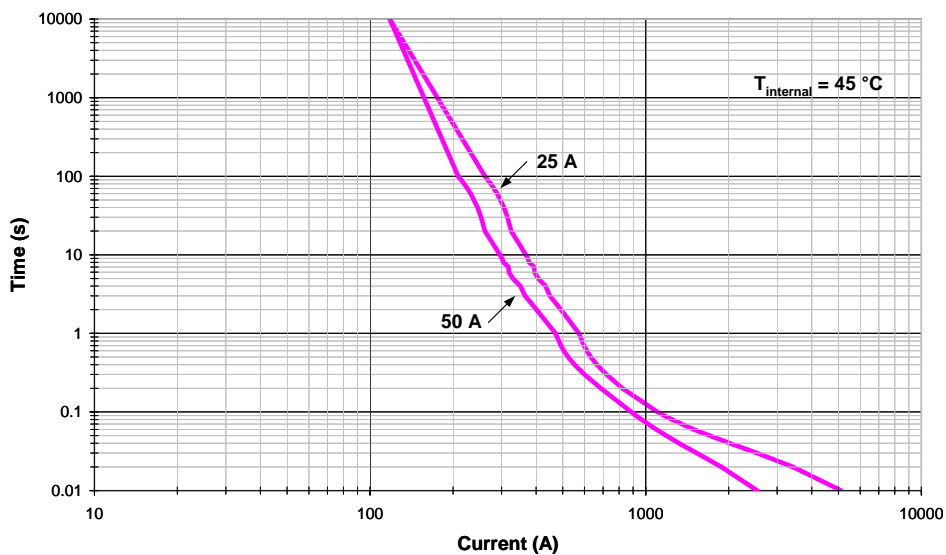


Figure 4-16: Thyristor overload capability (SKKT 162)

## 4.5 Surge / lightning protection

### 4.5.1 Surge characteristics

To protect the EVR against surge voltages, an understanding of the magnitude and characteristics of these surges are necessary.

The most common cause of surges in deep rural areas that will affect the EVR is lightning strikes. These lightning strikes can propagate to the EVR due to:

- Direct strikes to the LV feeder
- Induced surges to the LV feeder
- Direct strikes to the MV feeder
- Induced surges to the MV feeder

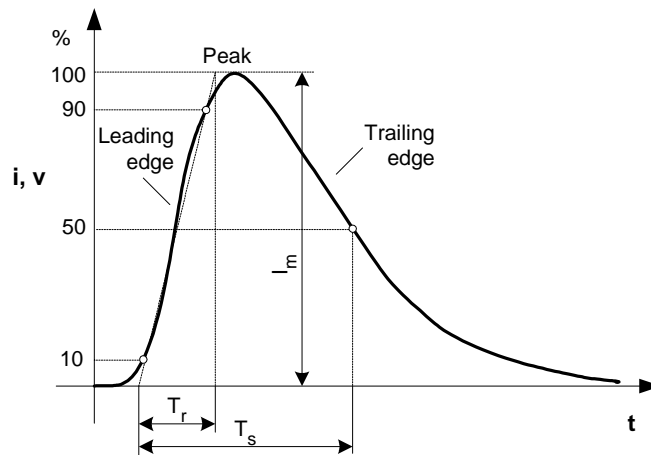
**Table 4-7: Lightning surge characteristics**

Location (LV or MV)	Type	Magnitude	Frequency
LV	Direct	Very high	1 in 3 years
LV	Induced	Moderate to low	Several per year
MV	Direct	High	Several per year
MV	Induced	Low	Many

Since the exact waveform shape and magnitude of lightning induced surges vary, a standard procedure to test the susceptibility of components to lightning surges is required.

A standard model to evaluate a system, with regards to surge susceptibility, is by applying voltage and current surge impulses. These impulses have certain characteristic rise and decay times that are used to specify the waveform. Current impulses applied are normally 8/20  $\mu$ s (rise time 8  $\mu$ s, with a decay time to half of the peak value equal to 20  $\mu$ s) or 4/10  $\mu$ s, while voltage impulses are (1.2/50  $\mu$ s).

The characteristic surge impulse waveform is shown in Figure 4-17, where  $T_r$  represents the surge rise time and  $T_s$  the surge duration until the surge decayed to half of the peak value.

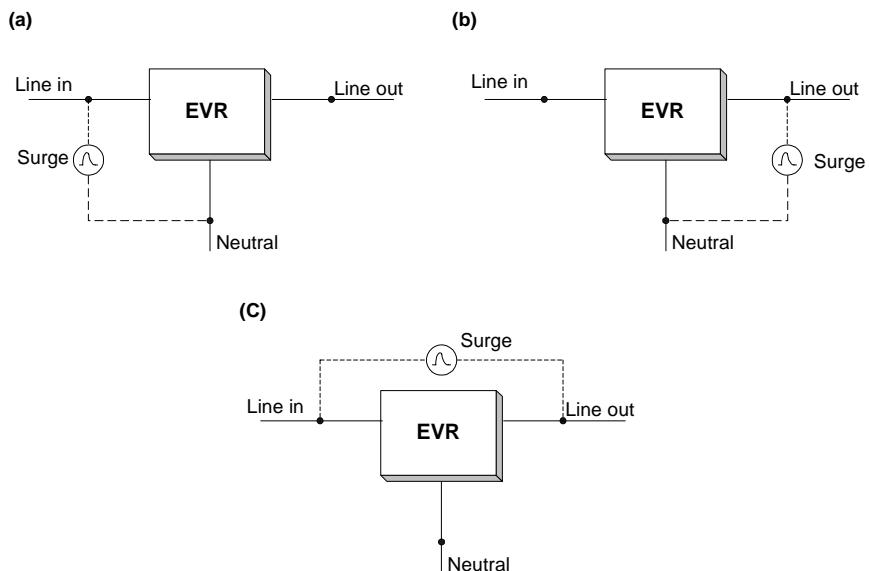


**Figure 4-17: Surge impulse waveform**

The magnitude of the surge voltage and current expected at the EVR terminals in the field installation is very difficult to predict. From past experience gained by the electricity utility company the surge current magnitude on the LV feeders where the EVR will be installed, can be assumed to be less than 20 kA.

### 4.5.2 EVR protection

The EVR can be seen as a three terminal device, the three terminals being line in, line out and neutral. A surge either due to lightning or other source can occur between any of these terminals as illustrated in Figure 4-18 (a, b, c).

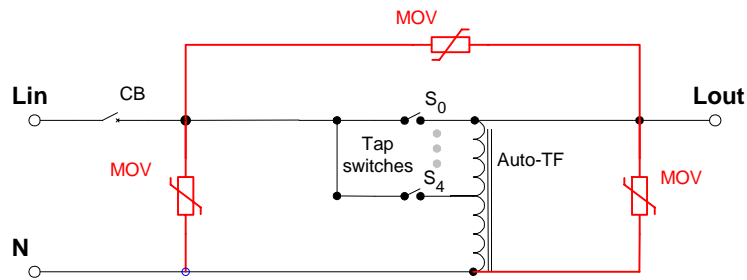


**Figure 4-18: Surge voltage location**

To protect the EVR against surge voltages the EVR is evaluated in non-operational (all the EVR taps are turned off) and operational mode.

In non-operational mode, the EVR presents a relative high impedance to surge voltages, because all the thyristor tap switches are open (see Figure 4-19). Applying a high surge voltage could however lead to a low impedance if any of the components fail due to isolation breakdown. The resulting surge current could destroy the component.

Using metal oxide varistors (MOVs), connected between all three terminals, the surge voltage can be clamped to a much lower level, thereby preventing isolation breakdown. The clamped voltage will depend on the amount of energy present in the surge and the characteristic of the MOV used. The resulting surge current will flow primarily through the MOV, which has a low impedance at high voltage, and not the EVR with its relative high impedance (assuming no isolation breakdown occurs).



**Figure 4-19: Surge protection - Non operational mode**

In operational mode (especially with the nominal tap,  $S_0$ , turned on), there will be a low impedance connection between the “line in” and “line out” terminals (see Figure 4-20). If a surge voltage is introduced, the resulting surge current flowing through the thyristors might damage the thyristor. To prevent this, an inductor is added in series with the “line in” terminal, thereby increasing the impedance. Since the voltage surge will be of short duration, the inductor will serve to limit the current magnitude by limiting the rate of rise of the current, thereby protecting the thyristors.



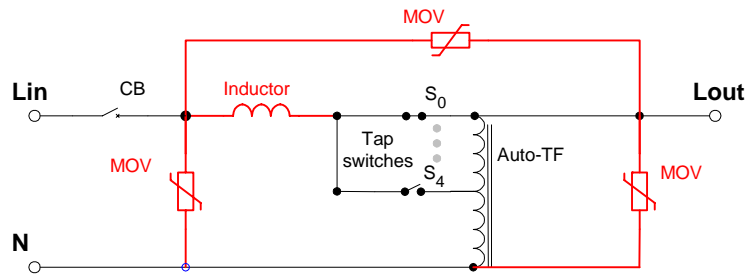


Figure 4-20: Surge protection - Operational mode

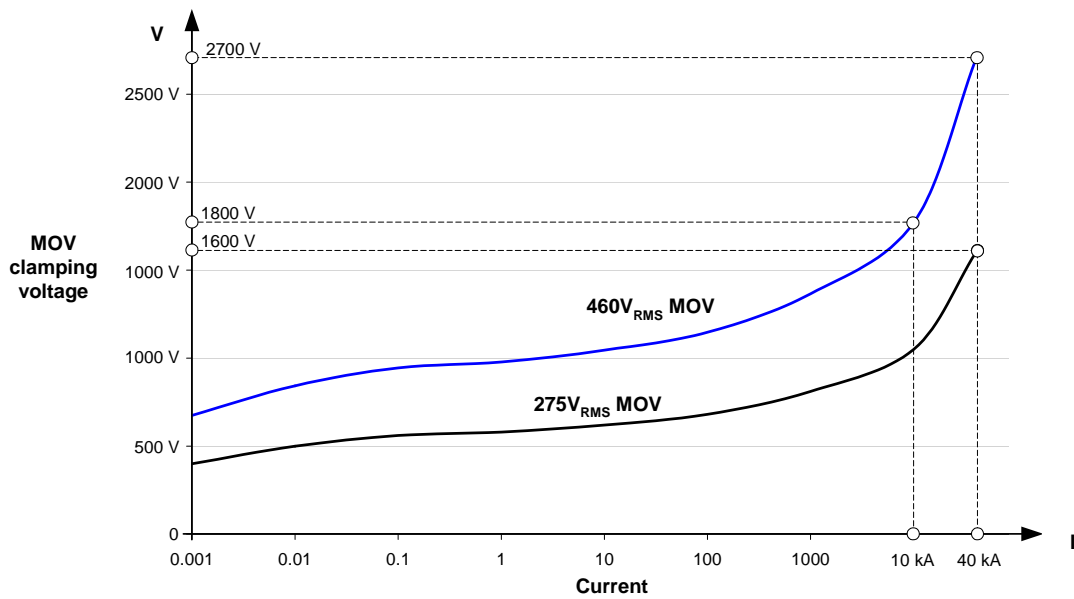
### MOV specification

Following recommendations made by the electricity utility company, MOVs with a surge current capability of at least 20 kA (8/20  $\mu$ s waveform) should be used for protection. Since 40 kA MOVs are more robust and available at a reasonable price, they are used in the design.

MOVs are essentially symmetrical, non-linear, voltage dependent resistors whose resistance decreases with an increase in voltage. The lower the MOV voltage rating, the lower the clamping voltage will be for the same current magnitude. To provide optimum protection the MOV rated voltage should therefore be chosen to just exceed the maximum RMS voltage expected at the EVR terminals.

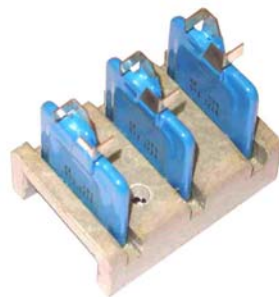
Under normal conditions the maximum voltage at the EVR input and output terminals will be  $253 V_{rms}$  ( $230 V + 10\%$ ), therefore a MOV rated at  $275 V_{rms}$  should be suitable. During certain line fault conditions the voltage at the input terminals could however be substantially higher. If for example the neutral connection on a three phase star connected distribution transformer fails, the line to line voltage could change depending on the amount of imbalance on the transformer. In a worst case scenario this voltage could increase to  $440 V$  ( $400 V + 10\%$ ) causing a MOV rated at  $275 V_{rms}$  to fail. Consequently MOVs rated at  $460 V_{rms}$  are used.

The current versus clamping voltage relationship for both the 460 V and 275 V MOV is shown in Figure 4-21. As can be seen the relationship is highly non-linear. With a surge current of 40 kA the clamping voltage across the 460 V and 275 V MOV is respectively 2700 and  $1600 V_{peak}$ .



**Figure 4-21: MOV V/I characteristic (Peak values shown)**

Figure 4-22 shows a picture of the MOV devices as used in the EVR. All three MOVs are mounted together onto a glass fiber base with short leads to the line in, line out and neutral connection points. The short leads minimize unwanted electromagnetic coupling caused by the high surge currents, from affecting the EVR controller.



**Figure 4-22: MOV assembly**

### Inductor specification

To design the surge current limiting inductor, the magnitude of current that can be conducted through the thyristors during a typical 8/20  $\mu$ s current waveform need to be obtained. The thyristor datasheet only specifies that the thyristor can handle a surge current with a magnitude of 2.25 kA for a 10 ms period. To obtain information regarding the 8/20  $\mu$ s surge current capability, the thyristors were tested physically.

Surge current withstand tests were performed on two SKKT106/12 thyristor modules (four thyristors in total) in a high voltage test facility at a South African university. The weakest thyristor could withstand a 12 kA surge current before failing, while others were able to withstand currents in excess of 16 kA. (See section 7.1.6.A on page 204 for more details on the surge current tests.) Because such a small number of samples were tested a 10 kA surge current, which is below the level at which the weakest thyristor failed, is selected as a safe surge withstand current for the thyristors.

The surge current limiting inductor operates when a voltage surge is encountered while the EVR is in operational mode (refer to Figure 4-20). If a voltage surge occurs on the supply, the MOV on the supply side will start to conduct. Due to the presence of the inductor which limits the  $di/dt$  into the rest of the EVR, most of the surge current will be shunted through the MOV, raising its clamping voltage according to the MOVs characteristic. As the clamping voltage increases with time, the current through the inductor will slowly increase.

As a first iteration, assume that the surge current through the MOV has a value of 10 kA peak, which according to electric utility company is a typical expected value at the point in the network where the EVR will be installed. From the MOV characteristic in Figure 4-21, this surge current will lead to a clamping voltage of approximately 1800 V. With an 8/20  $\mu$ s current waveform, the inductance needed to limit the surge current is then estimated from Equation (4-15):

---

$v = L \frac{di}{dt}$ $\therefore L = v \frac{dt}{di}$ $= 3.6 \mu H$	<p style="text-align: right;"><b>Where</b> (4-15)</p> <p><i>L = Inductance</i></p> <p><i>v = MOV clamping voltage (1800 V)</i></p> <p><i>di = Maximum surge current (10 kA)</i></p> <p><i>dt = ~ Surge duration for 8/20 <math>\mu</math>s waveform (20 <math>\mu</math>s)</i></p>
--	--

---

If the surge current through the MOV increases to 40 kA, which is the maximum value that the MOV can tolerate, the clamping voltage will be 2700 V. Recalculating the inductance needed to limit the surge current through the inductor to 10 kA, leads to a value of 5.4  $\mu$ H.

Being overly cautious due to the unpredictable nature of lightning surges, an inductor value of 20  $\mu$ H was chosen. This will limit the surge current to well below the thyristor's current withstand capability, which was obtained through limited experimental testing.

Since the inductor must be able to withstand high surge currents without saturating, an air core inductor was designed. Due to space restriction and the fact that only a few turns would be needed to construct the inductor, a high current density is allowed in the inductor. This minimizes the inductor size, at the expense of an increase in the copper losses.

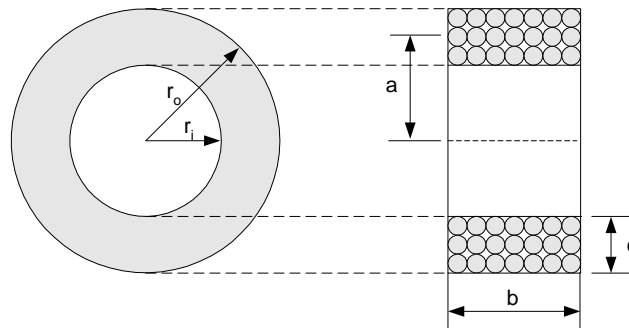
Calculating the precise inductance of an air core inductor can be very complex, especially if multiple layers are used. To estimate the inductance, Wheelers formula for multi-layer coils shown in Equation (4-16) can be used. This formula is based primarily on empirical measurements as opposed to theory and accurate to within a few percent. The geometry of such a multilayer coil is shown in Figure 4-23.

---


$$L = \left( \frac{1}{25.4 \times 1000} \right) \left( \frac{0.8 N^2 a^2}{6a + 9b + 10c} \right) \quad \text{Where} \quad (4-16)$$

$L = \text{Inductance (H)}$   
 $a = \text{Average radius of coil (m)}$   
 $\quad (r_i + r_o)/2$   
 $b = \text{Length of coil (m)}$   
 $c = \text{Thickness of coil (m)}$   
 $N = \text{Number of windings}$

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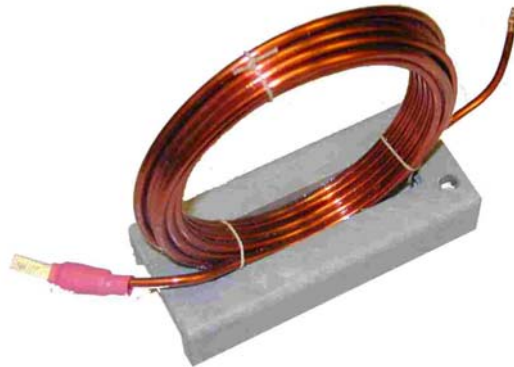


**Figure 4-23: Coil geometry**

To use Wheelers formula to obtain the number of windings an iterative process must be followed since the formula uses the coil geometry, which is unknown until the number of windings is known. Instead of describing this iterative process, the constructed inductor will be evaluated through Wheelers formula, to illustrate the formula's accuracy.

The inductor is wound using 3 mm enameled copper wire with 14 turns. The turns are distributed across 3 layers with an inner diameter of 75 mm and an outer diameter of approximately 94 mm. Its inductance is measured as 21.2  $\mu$ H. To facilitate mounting and

provide thermal and electrical isolation the inductor is mounted in a glass fiber base as shown in Figure 4-24.



**Figure 4-24: Inductor assembly**

Substituting the core geometry and winding data into Equation (4-16) gives:

---


$$L = 22.8 \mu H$$

*With*

$$a = 42.25 \times 10^{-3} m$$

$$b = 15 \times 10^{-3} m$$

$$c = 9.5 \times 10^{-3} m$$

$$N = 14$$


---

This calculated inductance corresponds well with the measured inductance of 21.2  $\mu H$ , verifying the accuracy of Wheelers formula. The inductor wiring data is summarized in Table 4-8, together with the current density at 5 kVA and 10 kVA power levels.

**Table 4-8: Inductor wiring data**

Conductor	Cross section	Turns	Estimated length	Current density	
				5 kVA	10 kVA
3mm Diameter Round	7.07 mm <sup>2</sup>	14 (3 Layers)	4 m	3.42 A/mm <sup>2</sup>	6.84 A/mm <sup>2</sup>

To estimate the losses in the inductor the same equations and principle that was used to calculate the copper loss in the transformer is used (see section 4.3.2.C on page 51). The copper

resistance is first calculated at 20 °C using Equation (4-6) and then modified using Equation (4-7) and (4-8) to calculate the resistance at higher copper temperatures.

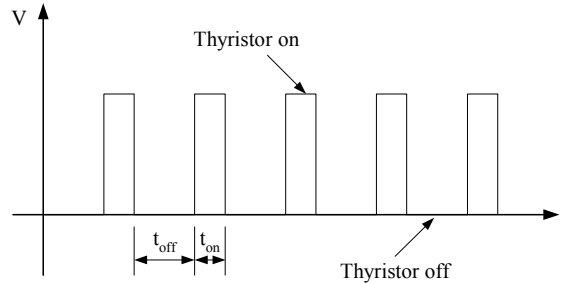
For the calculations at 5 kVA and 10 kVA power levels, the copper temperature is assumed to be 100 °C and 150 °C respectively. The results are tabulated in Table 4-9.

**Table 4-9: Inductor winding resistance & loss**

Resistance 20 °C	5 kVA			10 kVA		
	Resistance 100 °C	Current	Power loss	Resistance 150 °C	Current	Power loss
9.49 mΩ	12.5 mΩ	24.2 A	7.3 W	14.3 mΩ	48.4 A	33.5 W

#### 4.6 Glitch suppressor

Each tap switch consists of a back-to-back set of thyristors. To make sure that the thyristors turn on, pulses are applied to the thyristor's gate as illustrated in Figure 4-25.



**Figure 4-25: Thyristor pulses**

These pulses are applied continuously to both thyristor gates. As the supply current changes from the positive to negative AC cycle or vice versa, the corresponding thyristor in the set takes over the current flow.

If the transition in the AC cycle takes place just after time  $t_{on}$  has elapsed, the thyristor taking over the current flow will have to wait for time  $t_{off}$  before it will receive a positive gate pulse, turning it on. During the time  $t_{off}$  it is therefore possible that no thyristor will conduct, leading to a glitch in the output voltage. With a pulse frequency of 20 kHz and 30 % duty cycle used,  $t_{off}$  could be up to 35  $\mu$ s in length.

The glitch in the output voltage is only noticeable for highly inductive loads. This is due to two reasons:

- **Voltage at thyristor changeover point**

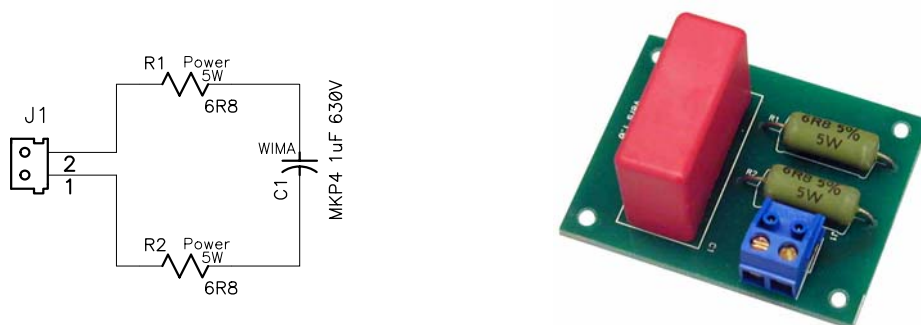
For purely resistive loads the load current and voltage will be in phase. The voltage will therefore be close to zero as one thyristor commutates and the other one starts to conduct, thereby preventing the glitch from being noticed. With highly inductive loads the current changeover point occurs at a high voltage and the glitch becomes noticeable.

- **Transformer flux**

The transformer flux and voltage is phase shifted by  $90^\circ$  from each other. With a purely resistive load, the transformer flux at the current crossover point is therefore at a maximum and could help support the load. For highly inductive loads, the transformer flux at the changeover point will be low and cannot help to support the load. A glitch will therefore be present in the output voltage.

To remove the glitch, the gate pulses need to be synchronized with the zero crossing point of the supply current so that the gate drive can be applied the instant the current crossover point is reached. Detecting the crossover point accurately and fast enough at very low power levels is however extremely difficult. It was therefore decided to rather connect a small capacitor across the load, storing enough energy to support the load voltage during crossover period. This circuit can be seen in Figure 4-26 together with a picture of the glitch suppressor.

The series resistance is added to limit the charge / discharge current through the capacitor. Inclusion of this glitch suppression circuit effectively prevents the occurrence of the glitches.



**Figure 4-26: Glitch suppressor**

## 4.7 Thyristor snubber

A thyristor can turn on falsely if its anode to cathode voltage is positive and the rate in voltage rise ( $dv/dt$ ) limitation is exceeded [24], even though the gate is not turned on. Depending on the application and type of thyristor used, additional protection measures might be needed to prevent false turn on. These protection measures typically consist of a resistor and capacitor connected across the thyristor (RC snubber), which limits the  $dv/dt$  across the thyristor. Snubber circuits are not required for all applications, as snubber design depend on the load characteristic, type of thyristor used and circuit configuration.

### 4.7.1 False turn on of thyristors

After a thyristor has been turned off, it takes a long time for the remaining excess carriers in one of the p-n regions of the device to recombine and swept out by the rise in voltage. The device should therefore be kept in the off state for a minimum time. In this application the thyristor is turned on at most once per cycle and there is therefore enough time for recombination to occur. However, the same effect can occur when the rate in voltage rise ( $dv/dt$ ) causes a displacement current through the p-n junction capacitance of the device. This current has the same effect as a gate trigger current in that it produces carriers that grows until the device is in its on state. Two types of  $dv/dt$  can be identified:

#### Static $dv/dt$

Static  $dv/dt$  or  $(dv/dt)_s$ , is a measure of ability of the thyristor to remain in a blocking state under the influence of a voltage transient which causes a rise in forward voltage. If the thyristor turns on due to the presence of high  $(dv/dt)_s$ , it will automatically turn off after a half cycle of conduction, if no further  $(dv/dt)$  disturbances are present.

In Figure 4-27 (a) a simple thyristor circuit diagram is shown together with two output waveforms in Figure 4-27 (b). In the top waveform the thyristor experiences a high  $dv/dt$  as the supply is turned on at time  $t_1$  and it starts to conduct until it commutates naturally at time  $t_2$ . In the bottom waveform, a surge present on the supply causes a high  $dv/dt$  that turns the thyristor on at time  $t_1$ . The thyristor will once again commutate naturally at time  $t_2$ .



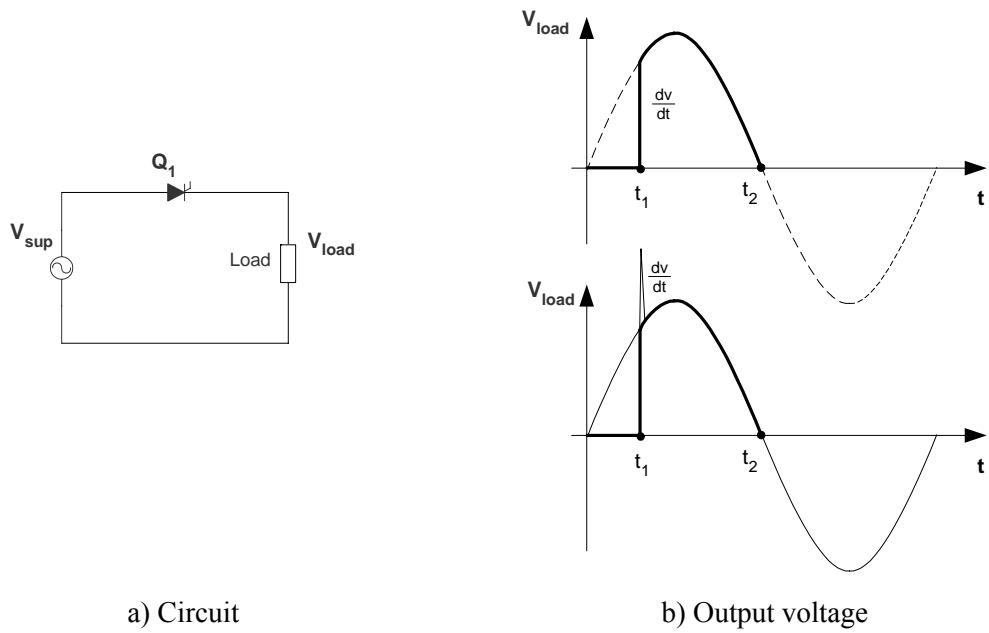


Figure 4-27: Static  $dv/dt$

### Commutating $dv/dt$

Commutating  $dv/dt$  or  $(dv/dt)_c$ , is applicable when the device was in the on-state and is turned off. This is illustrated in Figure 4-28, where an inductive / resistive load is supplied by back to back connected thyristors. Initially thyristor  $Q_1$  is turned on by applying a gate signal. At the current zero crossover point ( $t_1$ ),  $Q_1$  can commute. Due to the lag between the current and voltage a large  $dv/dt$  will be experienced by the forward biased thyristor  $Q_2$ , the instant  $Q_1$  turns off, forcing it to falsely turn on. This process will be repeated at every current zero crossing and the thyristors could potentially never turn off.

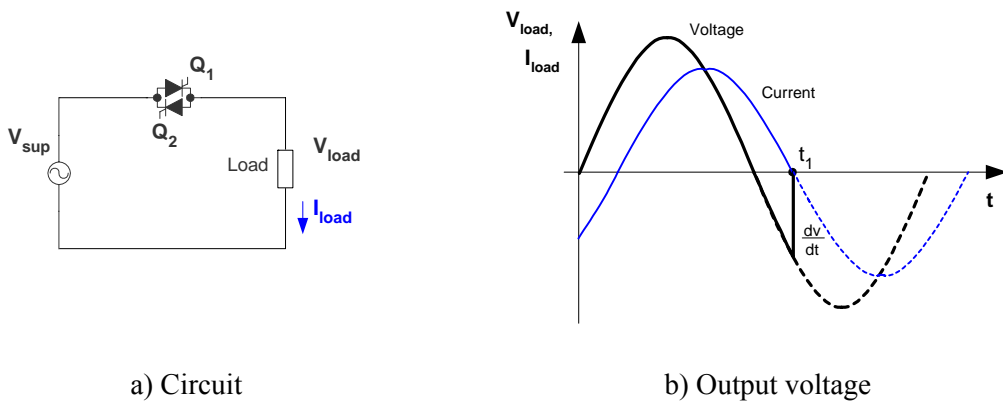


Figure 4-28: Commutating  $dv/dt$

## 4.7.2 Impact on EVR

Adding snubbers to the EVR introduces additional components that could negatively influence the reliability of the EVR. Snubber design is normally performed for specific load conditions, leading to less optimal and even possible thyristor damage if the load characteristics are changed significantly [24]. It is thus prudent to investigate whether or not snubber circuits are indeed required in the EVR. This depends on the specific thyristors used and the nature of the EVR load.

The thyristors used in the EVR have a very high  $dv/dt$  rating of  $1000 \text{ V}/\mu\text{s}$ . Due to the exponential rating method of  $dv/dt$  withstand capability [24], a higher rated voltage device guarantees increased  $dv/dt$  capability at lower voltages. The thyristors used in the EVR have a reverse voltage blocking capability of  $1200 \text{ V}$ , yet they are used in an application with a peak voltage of  $360 \text{ V}$  ( $253 \text{ V}_{\text{RMS}}$ ). The actual  $dv/dt$  withstand capability at  $360 \text{ V}$  is therefore substantially higher (at least  $2000 \text{ V}/\mu\text{s}$ ).

The EVR as applied in rural electrification will typically be subjected to mostly resistive loads, typically lighting and heating appliances.

### Impact of static $dv/dt$

To bring some perspective to the high  $dv/dt$  rating of the thyristor, the expected  $dv/dt$  caused by surge voltages needs to be quantified. During surge voltage protection tests, a typical voltage impulse with a characteristic waveform of  $1.2/50 \mu\text{s}$  is applied. Assuming that  $1.2 \mu\text{s}$  is a typical expected voltage surge rise time, the expected  $dv/dt$  can be calculated as  $1500 \text{ V}/\mu\text{s}$ , assuming that the MOVs on the EVR limits the surge voltage to  $1800 \text{ V}$ . This is lower than the  $dv/dt$  withstanding capability of the thyristors.

If the static  $dv/dt$  rating is indeed exceeded, the thyristors will automatically commutate within half a cycle. Although a portion of the tap winding would be shorted during this period, the resulting circulating current will not cause damage to the transformer or thyristors. This was verified experimentally in section 7.1.7, and the rise in transformer winding temperature calculated theoretically.

### Impact of commutated $dv/dt$

As already stated, the EVR will be subjected to mostly resistive loads. The amount of lag between the current and voltage will therefore be very small, minimizing the possibility of the

commutating  $dv/dt$  phenomenon. If the EVR is indeed subjected to a large inductive load, the glitch suppressor in conjunction with the decreasing flux in the transformer will maintain the output voltage, causing it to slowly decrease. The commutating  $dv/dt$  is thus limited, preventing loss of control over the thyristors.

This can be explained by reference to Figure 4-29 (a), where a simplified EVR model is shown together with the glitch suppressor circuit ( $R_g$ ,  $C_g$ ) and a resistive-inductive load. Thyristor  $Q_1$  is initially turned on. At the current zero crossover point ( $t_1$ ),  $Q_1$  will commute. Due to the decaying flux inside the transformer and the RC time constant of the glitch suppressor circuit the output voltage will not decrease to zero instantly, but will decrease exponentially as shown in Figure 4-29 (b). The  $dv/dt$  experienced by  $Q_2$  will therefore be low, preventing it from turning on.

(The slowly decaying output voltage is confirmed through practical measurements – refer to Figure 7-5)

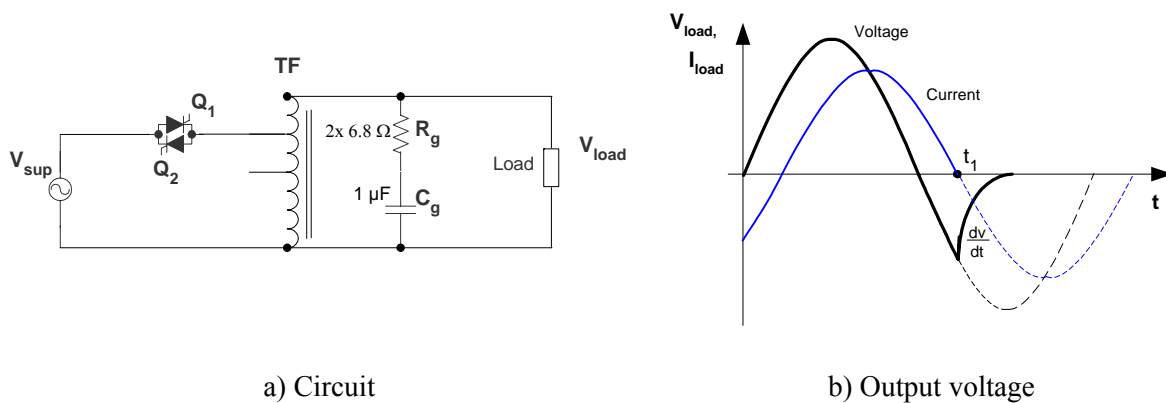


Figure 4-29: Simplified EVR with glitch suppressor aiding in  $dv/dt$  limiting

## Conclusion

Although not proven theoretically, snubbers are not expected to be required in the EVR. This was verified through practical experimentation in which the EVR was subjected to highly inductive loads.

## 4.8 Wiring losses

To obtain the losses in the EVR, the wiring loss must also be considered. Due to the negligible power loss in all the control and low power wiring harnesses, only the losses incurred in high current wiring consisting of the main power path and fly-leads are considered.

The main power path inside the EVR consists of the wiring from the input to the auto-transformer and back again to the output. The path is approximately 1.5 m long and consists mainly of 10 mm<sup>2</sup> copper wiring.

The EVR is equipped with three fly-leads (line-in, line-out and neutral) which are used to connect to the EVR to the power network. Each of these wires is approximately 2.5 m long and has a cross section area of 10 mm<sup>2</sup>. Because these fly-leads are an integral part of the EVR, their losses are included in the total power loss of the EVR. Because the current through the neutral fly-lead is small, only the losses in the input and output fly-lead is considered.

The internal and external wiring that contributes significantly to the wiring losses are summarized in Table 4-10.

**Table 4-10: Enclosure wiring**

<b>Location</b>	<b>Conductor</b>	<b>Cross section</b>	<b>Estimated length</b>
Internal	Main power wiring (input to output)	10 mm <sup>2</sup>	1.5 m
External	Fly-lead (input back to output)	10 mm <sup>2</sup>	5 m

To calculate the loss in the internal and the external wiring, the same equations and principles that were used to calculate the copper loss in the transformer (see section 4.3.2.C on page 51) is used. The copper resistance at 20 °C is first calculated using Equation (4-6) and then modified using Equation (4-7) and (4-8) to calculate the resistance at the higher temperature.

To calculate the copper loss at 5 kVA and 10 kVA power levels, the internal wiring copper temperature is estimated to be 70 °C and 85 °C respectively. The external wiring temperature is assumed to be 50 °C and 65 °C at the two power levels.

**Table 4-11: Enclosure wiring resistance & loss**

	Resistance 20 °C	5 kVA			10 kVA		
		Resistance	Current	Power loss	Resistance	Current	Power loss
Internal wiring	2.52 mΩ	2.8 mΩ (@ 70 °C)	24.2 A	1.6 W	3 mΩ (@ 85 °C)	48.4 A	7 W
External wiring	8.39 mΩ	10 mΩ (@ 50 °C)	24.2 A	5.9 W	10.5 mΩ (@ 65 °C)	48.4 A	24.6 W

## 4.9 Enclosure

The EVR is installed outdoors and should therefore be designed to be able to withstand harsh weather conditions.

An essential requirement of the EVR design is that the components used should require no maintenance. This requirement complicates the thermal cooling design of the EVR since it implies that no moving parts i.e. fans may be used.

Since the EVR will be used outdoors, water penetration and condensation inside the EVR must be prevented. This necessitates that the EVR enclosure should be totally sealed, thereby effectively trapping the heat generated inside and introducing further complications to the thermal design.

Selection criteria for the enclosure includes size, cost, ingress protection (IP) rating, ultraviolet (UV) withstand capability and corrosion resistance. Based on these criteria, an enclosure made from glass fiber reinforced polyester (GRP) dough mould compound (DMC) with an IP rating of 65 was selected. DMC basically consists of a thermosetting polyester plastic with added calcium carbonates to improve stiffness, aluminium hydroxides to improve fire retardency and glass fibers to improve mechanical strength. An IP rating of 65 implies total protection against dust and protection against powerful water jets all round. It should be noted that this IP rating only applies to the enclosure before any holes for cable entry and LED status indicators are

made. Addition of these holes changes the IP rating of the enclosure to 43 which mean that solid objects larger than 1 mm cannot penetrate the enclosure, neither can rain.

To verify if adequate cooling is present in the sealed enclosure, a thermal design must be completed. Due to the complex nature of the thermal interaction between the various components and the heat distribution within the enclosure a simplified design procedure is followed to estimate the cooling requirements. This procedure can be described as follows.

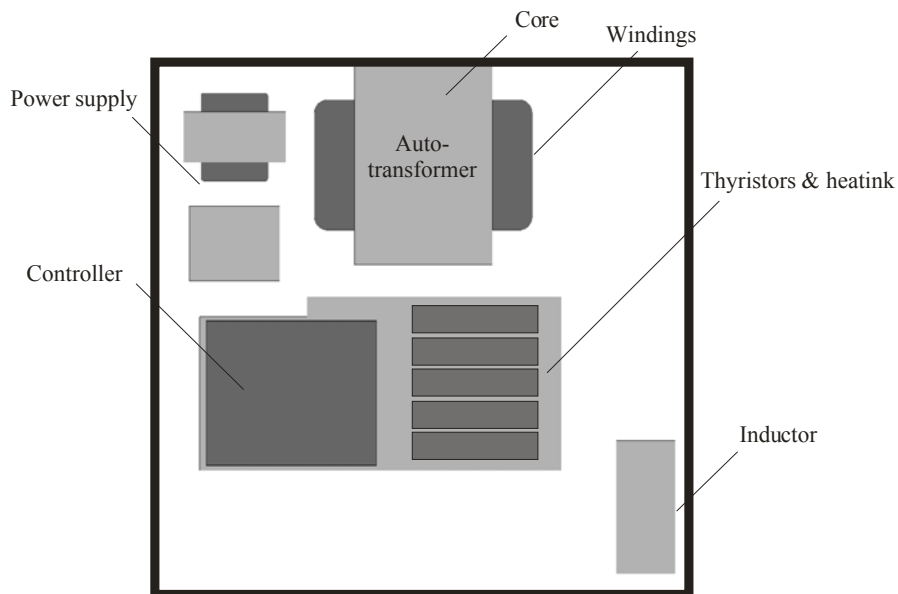
All the major sources of heat and their specific location inside the enclosure are identified and their expected losses at 5 kVA and 10 kVA are summarized. Experimental data is then obtained for the temperature inside the enclosure at various points with a heat source equivalent to the losses at 5 kVA and 10 kVA. The results of these experiments will show that enough heat cannot be transferred through the enclosure's surface alone while maintaining an acceptable internal ambient temperature. To improve the cooling the addition of an external heat sink is then investigated and its required thermal resistance is calculated based on the internal ambient temperatures obtained during the experiments.

#### **4.9.1 Component location and losses**

A summary of the expected losses inside the EVR (excluding the external wiring) at the rated power of 5 kVA and at 10 kVA overload are given in Table 4-12. The physical position for each of the components inside the enclosure is illustrated in Figure 4-30.

**Table 4-12 : Component losses (excluding external wiring)**

Component	Power loss	
	@ 5 kVA	@ 10 kVA
Auto transformer - Core	20.7 W	20.7 W
Windings	22.1 W	99 W
Thyristors	22 W	45 W
Surge protection inductor	7.3 W	33.5 W
Electronics		
Power supply & controller	5 W (estimate)	5 W (estimate)
Wiring - Internal	1.6 W	7 W
External	---	---
<b>Total loss</b>	<b>78.7 W</b>	<b>210.2 W</b>



**Figure 4-30: Component position**

## 4.9.2 Enclosure thermal evaluation

Since only limited information on the thermal properties of the enclosure could be obtained, the enclosure is evaluated through a set of practical experiments. The aim of these experiments is to determine how much of the heat would be able to be transferred through the enclosure surface to the outside while the internal ambient temperature stays at an acceptable level. To quantify the acceptable internal ambient temperature, the most critical components that can fail or stop functioning under high temperatures need to be identified. These are the auto-transformer, thyristors and electronic components.

The auto-transformer core and windings can withstand high temperatures (up to 150 °C internally) although this accelerates degrading of the isolation on the windings, leading to a lower life expectancy. Temperature protection has been included in the auto-transformer through addition of a temperature sensor that monitors the winding temperature. If the winding temperature exceeds 135 °C, the controller reduces the losses in the transformer by selecting a tap setting with lower losses.

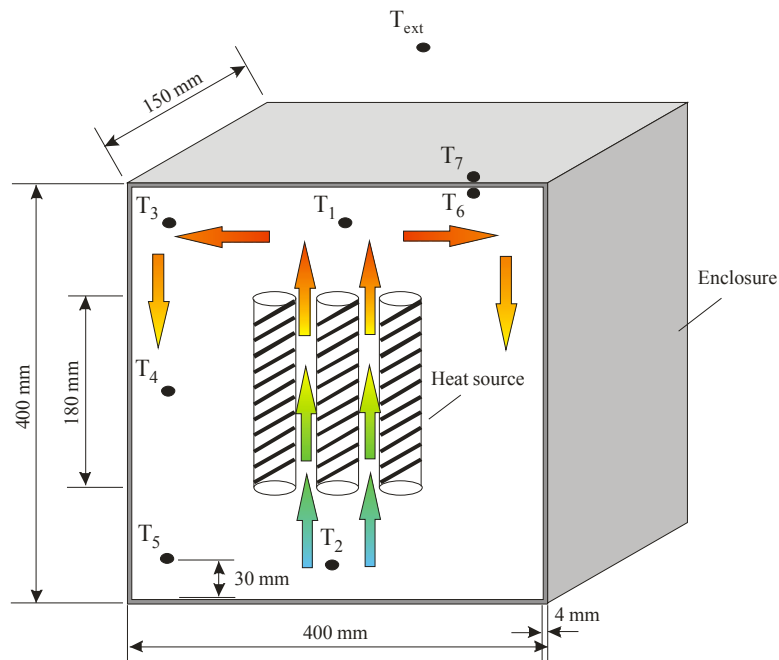
The thyristors are mounted onto a heat sink and are protected against temperature related failures with a temperature sensor mounted onto the heat sink. In designing the thyristor heat sink a maximum ambient temperature of 85 °C was assumed so the EVR will remain functional up to this temperature.

Lastly, the electronic components used in the power supply and controller are commercial grade components that are only specified to operate reliably at an ambient temperature up to 85 °C.

Consequently the maximum acceptable internal ambient temperature is selected as 85 °C.

To evaluate the enclosure a heat source was placed in the center of the enclosure, since most of the EVR losses are concentrated in this area. Temperature measurements were made at various points inside the enclosure as shown in Figure 4-31. Temperature measurement points  $T_1$  to  $T_5$  were located 30 mm from the inner surface of the enclosure, while points  $T_6$  and  $T_7$  measure the temperature on the inner and outer surface on the enclosure.





**Figure 4-31: Temperature measurements inside enclosure**

The measurements were done with a heat source of 100 W and 200 W, which are comparable to the expected losses at 5 kVA and 10 kVA respectively. The steady state temperatures obtained are summarized in Table 4-13. For both experiments the thermal time constant was approximately 20 minutes, which means that steady temperatures were reached in approximately 100 minutes. Steady state implies that the rate at which heat is produced by the heat source is equal to the heat flow rate through the enclosure surface.

**Table 4-13: Internal enclosure temperatures**

Location	Temperature @	
	100 W	200 W
T <sub>ext</sub> - External	20 °C	20 °C
T <sub>1</sub> – Top center	84 °C	120 °C
T <sub>2</sub> – Bottom center	34 °C	47 °C
T <sub>3</sub> – Top left	68 °C	101 °C
T <sub>4</sub> – Middle left	57 °C	86 °C
T <sub>5</sub> – Bottom left	32 °C	41 °C
T <sub>6</sub> – Inner surface	61 °C	91 °C
T <sub>7</sub> – Outer surface	43 °C	62 °C

*Note: Add 25 °C to measurements to obtain temperatures equivalent to 45 °C external ambient conditions.*

From the temperature measurements it can be seen that the temperature at the top of the enclosure is much warmer than at the bottom (T<sub>1</sub> versus T<sub>2</sub>). Furthermore the temperature at the center is also much warmer than the temperature at the left (T<sub>1</sub> versus T<sub>3</sub>). This non-uniform temperature distribution can be explained as follows, with reference to Figure 4-31.

As the air around the heat source is heated, it becomes less dense and rises to the top of the enclosure through convection. Conduction between the hot air and enclosure surface allows heat to be extracted from the air. As it cools slightly, its density decreases and it moves sideways and down, allowing it to be replaced by new warm air, thereby creating the heat distribution as observed. Because air is such a poor conductor of heat, conduction plays a minimal role in the temperature distribution.

Since the experiments were done indoors with an ambient temperature of 20 °C, a further 25 °C will be added to all the measurements if the EVR operates outdoors in a 45 °C environment.

The temperature in the vicinity of the electronic components ( $T_4$ ) will now be 82 °C and 111 °C respectively with 100 W and 200 W being dissipated.

Due to the maximum internal operating temperature of 85 °C for the electronic components it can be seen that the thermal cooling of the enclosure is insufficient for the EVR operating at 10 kVA. Consequently another method must be devised to extract heat from the enclosure to aid the losses through the enclosure's surface.

### **4.9.3 Improved thermal cooling**

Due to the shape, location and amount of heat produced by the auto-transformer, an aluminium heat sink can be mounted externally onto the auto-transformer to extract heat from the enclosure. Since the auto-transformer is responsible for approximately 50 % of the losses in the EVR, this greatly reduces the internal ambient temperatures.

To obtain optimum thermal contact with the auto-transformer, a large rectangular hole is made in the top of the enclosure, through which the heat sink base protrudes. Since the assembled laminated core does not provide a very even surface a thick layer of thermal conduction paste is applied between the core and heat sink to ensure adequate thermal coupling. To maintain the tight coupling the transformer core is tightened to the heat sink using two screws attached the core frame.

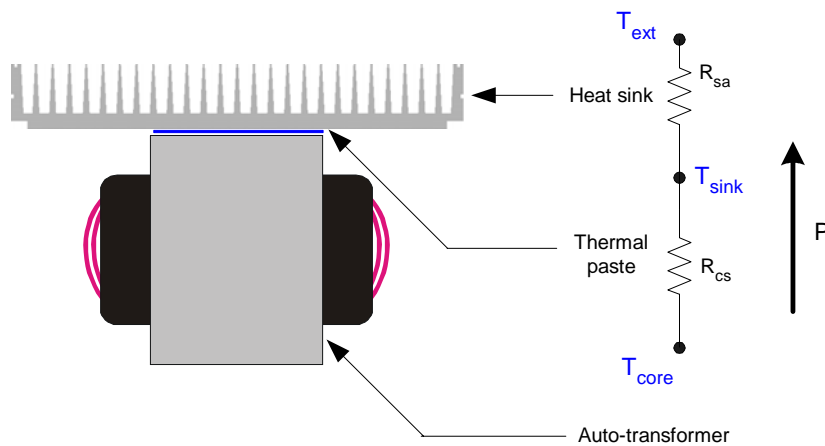
To calculate the required thermal resistance of the heat sink is quite complex. All of the losses generated by the auto-transformer windings will not couple directly with the core because of the poor thermal coupling between the windings and core. In addition, heat generated in other components may be absorbed by the auto-transformer and extracted through the heat sink. Obtaining the amount of heat available in the transformer core for extraction is therefore very difficult and a simplified approach was taken to estimate the heat sink requirements.

From the experimental data obtained for the enclosure (refer to Table 4-13) the ambient temperature in the vicinity of the electronic components will be 82 °C with 100 W being dissipated (under 45 °C external ambient conditions). Since this temperature is still below the limit of 85 °C, the amount of power that can be dissipated by the enclosure can be increased to 108.1 W (assuming a linear relationship between power and temperature).

Through the addition of the heat sink the surface area of the enclosure itself will be reduced, which leads to a slight decrease in the amount of power that can be dissipated through the

enclosure surface alone. Assuming that only the top half of the enclosure surface contributes significantly to the cooling due to the non uniform temperature distribution, the surface area available for cooling is reduced by a factor of 0.95 (from 0.28 m<sup>2</sup> to 0.266 m<sup>2</sup>). This loss in surface area reduces the amount of losses that can be extracted through the enclosure itself to 102.3 W.

To calculate the required thermal resistance of the heat sink a simplified thermal model consisting of the auto-transformer, thermal paste and heat sink (as shown in Figure 4-32) is used.



**Figure 4-32: Cooling thermal model**

Using the relationship between power and temperature as stated in Equation (4-9), the heat sink thermal resistance ( $R_{sa}$ ) can be calculated as follows:

$$R_{sa} = \frac{(T_{core} - T_{ext})}{P} - R_{cs} \quad \text{Where} \quad (4-17)$$

$R_{sa}$  = Heat sink to ambient thermal resistance ( $^{\circ}C/W$ )

$R_{cs}$  = Core to heat sink thermal resistance ( $^{\circ}C/W$ )

$T_{core}$  = Core temperature ( $^{\circ}C$ )

$T_{ext}$  = External ambient temperature ( $^{\circ}C$ )

$P$  = Power ( $W$ )

To solve the equation above, two unknown parameters must be estimated or calculated. These are the core temperature ( $T_{core}$ ) and the core to heat sink thermal resistance ( $R_{cs}$ ).

The amount of heat that can be extracted through the enclosure was calculated to be 102.3 W. With the EVR operating at 10 kVA (210.2 W of losses) in a 45 °C external environment 107.9 W must therefore be extracted through the heat sink (assuming that these losses will be present at the core for extraction).

Dissipation of the 102.3 W of losses will be responsible for an increase in the air temperature inside the enclosure comparable to that of the 100 W thermal experiment. The air temperature in the vicinity of the core ( $T_1$ ) can thus be estimated to be close to 109 °C by referring to Table 4-13. If the actual core temperature is lower than this, additional heat will be extracted from the air into the core and dissipated through the heat sink. As a first iteration it can be assumed that the core temperature is equal to the air temperature in the vicinity of the core.

The thermal paste used between the core and heat sink is specified by its thermal conductivity ( $k$ ). To relate the thermal conductivity to the thermal resistance of the layer of heat sink paste ( $R_{cs}$ ) the definition of thermal conductivity can be used.

Thermal conductivity ( $k$ ) can be defined as the rate ( $Q/t$ ) at which heat is transferred through a medium with a cross section area of ( $A$ ) over a distance ( $L$ ) due to a temperature difference ( $\Delta T$ ) across the medium as shown in Equation (4-18).

---

$k = \left( \frac{Q}{t} \right) \frac{L}{A \Delta T}$	<p><b>Where</b> <span style="float: right;">(4-18)</span></p> <p><math>k</math> = Thermal conductivity (W/m.K)</p> <p><math>Q</math> = Quantity of heat (J)</p> <p><math>t</math> = time (s)</p> <p><math>L</math> = Length / distance (m)</p> <p><math>A</math> = Area (<math>m^2</math>)</p> <p><math>\Delta T</math> = Temperature difference (°C)</p>
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Recognizing that the rate at which heat is transferred ( $Q/t$ ) is equal to power; the equation can be rewritten as follow:

---

$\Delta T = \left( \frac{Q}{t} \right) \left( \frac{L}{k A} \right)$ $= P \left( \frac{L}{k A} \right)$	<p>(4-19)</p>
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By comparing Equation (4-19) with Equation (4-9) it can be seen that  $\frac{L}{kA}$  represents the thermal resistance. To obtain the thermal resistance of the thermal paste layer, the thermal conductivity (k), the thickness of the applied paste (L) and the area (A) the paste is applied to is needed.

The thermal conductivity of the paste used is specified as 0.55 W/(m.K). Due to the uneven assembly of the core laminations the paste is applied in layer with a thickness of approximately 1 mm. The core surface area onto which the paste is applied measures 120 x 102 mm. Using these values, the thermal resistance of the heat sink paste layer can be calculated as:

---

$R_{cs} = \frac{L}{kA}$ $= 0.149 \text{ } ^\circ\text{C/W}$	<p><b>Where</b></p> $L = 1 \times 10^{-3} \text{ m}$ $A = 0.0122 \text{ m}^2$ $k = 0.55 \text{ W/(m.K)}$	(4-20)
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All the parameters in Equation (4-17) are now quantified and the required thermal resistance of the heat sink can be calculated from the cooling thermal model as:

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$R_{sa} = \frac{(T_{core} - T_{ext})}{P} - R_{cs}$ $= 0.44 \text{ } ^\circ\text{C/W}$	<p><b>Where</b></p> $R_{cs} = 0.149 \text{ } ^\circ\text{C/W}$ $T_{core} = 109 \text{ } ^\circ\text{C}$ $T_{ext} = 45 \text{ } ^\circ\text{C}$ $P = 107.9 \text{ W}$	(4-21)
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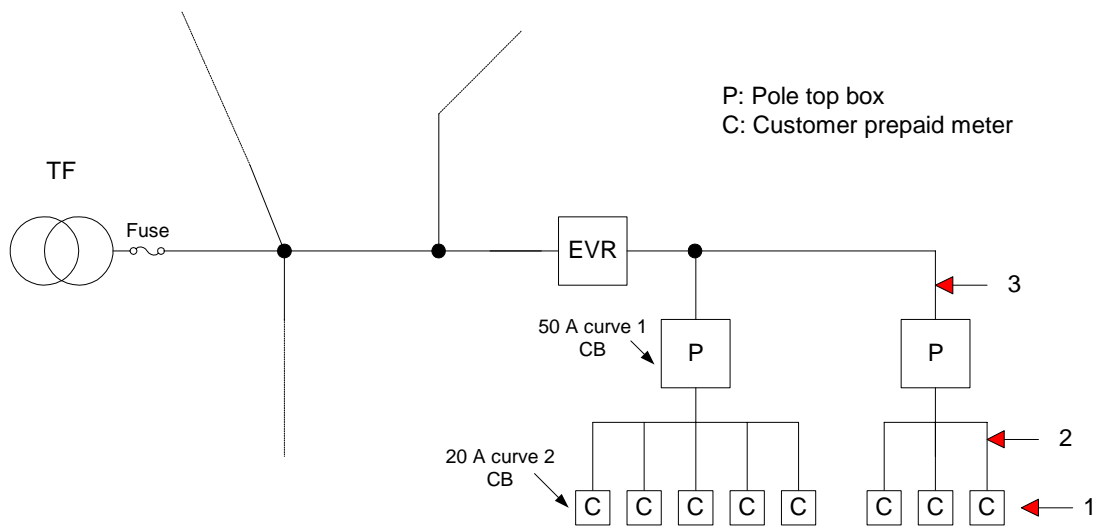
The most suitable commercially available heat sink to fit in the required space with minimal machining requirements is a HE4. With a length selected as 140 mm, the specified thermal resistance is 0.34 °C/W for natural air cooling. Since this is better than the requirement, the core temperature using this heat sink will be lower. Using Equation (4-17) the core temperature can be recalculated to be 98.5 °C. Since the core temperature is lower than the surrounding air temperature of 109 °C, additional heat will be absorbed from the air and extracted, leading to an internal temperature less than 85 °C.

## 4.10 Protection coordination

### Background

Installing an EVR on the low voltage reticulation network could influence optimal operation if its protection is not properly coordinated with the other elements in the network.

To investigate this, consider the diagram in Figure 4-33, where a section of a LV reticulation network is illustrated. One EVR is shown, feeding the last section of the line onto which two pole top boxes (service connection points) are connected. Each pole top box is equipped with a 50 A curve 1 circuit breaker, supplying a number of customers. Each customer is assumed to be connected through a prepaid electricity meter inside his house, equipped with a 20 A curve 2 circuit breaker.



**Figure 4-33: Typical LV feeder configuration**

Depending on the location of the fault the following should occur:

**Case 1:** Customer at point “1” has a faulty appliance inside his house, causing a short circuit.

The customer’s 20 A curve 2 circuit breaker inside his prepaid meter should trip, before the 50 A curve 1 circuit breaker in the pole top box or the EVR.

**Case 2:** Fault on the service line at point “2” between the pole top box and customer’s prepaid meter.

The 50 A pole top box circuit breaker should trip, before the EVR trips. The EVR should therefore be capable of sustaining the fault current long enough to trip the pole top box circuit breaker. This also ensures that the power supply to the five customers on the other pole top box feeding from the EVR would not be interrupted.

If the EVRs protection is not coordinated with the pole top box, the fault could result in the EVR turning off, thereby also unnecessarily disrupting the power supply to the other pole top

box.. To determine the location of the fault would now be more difficult as no indication is given to the location of the fault other than it is somewhere downstream from the EVR.

**Case 3:** Fault on the line at point “3” between the EVR and pole top box

The EVR should protect itself and turn off before the transformer fuse blows. Assuming that the pole top box circuit breakers are in working order, it narrows the fault finding to the line between EVR and pole top boxes.

#### 4.10.1 Fault current magnitude

To evaluate if the desired protection coordination can be implemented in the EVR, the maximum expected fault current magnitude is needed. To calculate the fault current, a typical LV network consisting of a transformer and feeder cable is evaluated. Using the cable and transformer properties a simple network model is constructed. This model is used to identify a suitable location where the EVR can be installed, based on the minimum acceptable customer voltage of 230 V – 10 %. The fault current at this position is then calculated. (To simplify the analyses the voltage drop across the service connection from the feeder to the customer is ignored.)

#### Cable

The EVR is to be installed on low density rural LV feeders equipped with aerial bundled conductors (ABC). In these networks ABC feeders with a cross section of 35 mm<sup>2</sup> and 70 mm<sup>2</sup> is most commonly used. Some of the electrical properties of these cables are given in Table 4-14.

**Table 4-14: ABC cable properties**

	35 mm <sup>2</sup>	70 mm <sup>2</sup>
Resistance (@ 20°C)	0.868 Ω/km	0.443 Ω/km
Reactance	0.09 Ω/km	0.083 Ω/km
Rated current (in free air)	138 A	213 A

To obtain a more accurate network model, the cable resistance which is specified at 20 °C needs to be adjusted for a higher operating temperature. In adjusting the resistance the same principles used in calculating the copper wire resistance at higher temperatures can be used. - Refer to



Equation (4-7) for more information. Assuming a feeder temperature of 60 °C, the new resistance can be estimated to be 1.004 Ω/km and 0.512 Ω/km for the 35 mm<sup>2</sup> and 70 mm<sup>2</sup> cables respectively.

## Transformer

The transformers used in the LV rural networks are typically 16 kVA single phase or 32 kVA dual phase, with an impedance voltage drop of approximately 4.5 %. Data supplied by the transformer manufacturer indicate that the copper losses in a typical 16 kVA (22 kV / 240 V) transformer is approximately 400 W.

To be able to calculate the fault currents on the network, consisting of the transformer and feeder cable, the transformers' resistance and reactance must be calculated. The resistance can be obtained from the copper loss, shown in Equation (4-22).

---

$P_{CL} = I_{TFR}^2 R_{TF}$	<b>Where</b>	(4-22)
	$P_{CL} = \text{Copper loss (400 W)}$	
$\therefore R_{TF} = 0.09 \Omega$	$I_{TFR} = \text{Rated TF secondary current (66.67 A)}$	
	$R_{TF} = \text{Transformer resistance } (\Omega)$	

---

To calculate the reactance, the relationship between impedance, resistance and reactance is used, as stated in Equation (4-23). Because impedance is a complex quantity (contains both magnitude and phase information), the relationship between impedance, resistance and reactance is not linear. Using the formula below, the reactance can be calculated from the specified impedance and calculated resistance.

---

$\hat{Z} = R + jX$	<b>Where</b>	
and	$Z = \text{Complex impedance } (\Omega)$	
$ \hat{Z}  = \sqrt{R^2 + X^2}$	$R = \text{Resistance } (\Omega)$	(4-23)
	$X = \text{Reactance (positive or negative) } (\Omega)$	
	$ Z  = \text{Magnitude of complex impedance } (\Omega)$	

---

To obtain an ohmic value for the impedance, the percentage voltage drop over the impedance at rated current is used as shown in Equation (7-2).

$$V_Z = I_{TFR} Z_{TF} \quad \text{Where} \quad (4-24)$$

$$\therefore Z_{TF} = 0.162 \Omega$$

$V_Z = TF$  voltage drop (4.5% of 240 V)

$I_{TFR} =$  Rated TF secondary current (66.67 A)

$Z_{TF} =$  TF impedance ( $\Omega$ )

Using the impedance and resistance, the reactance can now be calculated from Equation (4-23) as shown below.

$$|\hat{Z}_{TF}| = \sqrt{R_{TF}^2 + X_{TF}^2}$$

$$\therefore X_{TF} = 0.135 \Omega$$

With

$$Z_{TF} = 0.162 \Omega$$

$$R_{TF} = 0.09 \Omega$$

## Network model

Using the transformer and ABC feeder properties, the simple network model shown in Figure 4-34 is constructed. This model is used to evaluate the voltage along the feeder and the fault current magnitude at the end of the feeder for different feeder lengths.

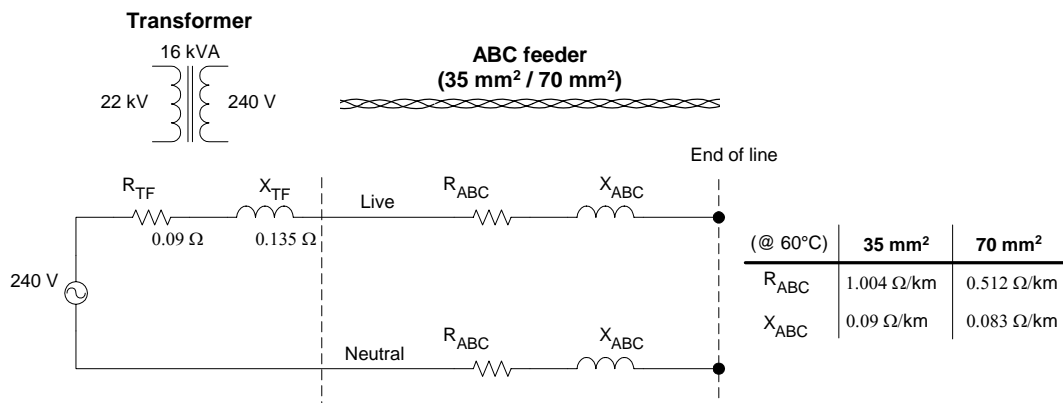


Figure 4-34: Network model

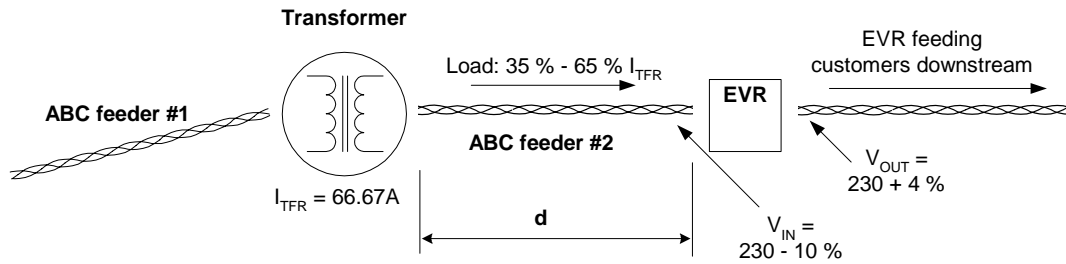
## Fault current

To evaluate the fault currents, the probable location of the EVR on the feeder needs to be identified. This is done based on the voltage along the feeder. Consider the diagram in Figure 4-35, where a single phase transformer is placed centrally to two feeders.

If the system is perfectly balanced, 50 % of the transformer current would flow in either feeder. In practice the loads on both feeders would seldom be equal. This is because of the

diversification in electricity use by the customers and due to the addition of new households onto the feeder that disrupts the original balanced design.

Assuming that the amount of balance between the feeders is such that the load current expected in any of the feeders varies between 35 % and 65 % of the rated transformer current ( $I_{TFR}$ ), the distance ( $d$ ) at which the feeder voltage drops to 230 V – 10 % can be calculated. This is the point where an EVR can be installed, boosting the voltage to the downstream customers.



**Figure 4-35: EVR position**

Using the constructed network model, the voltage at different positions along the 35 mm<sup>2</sup> and 70 mm<sup>2</sup> feeders can be calculated for feeder currents equal to 35 % and 65 % of the rated transformer current, as shown by Equation (4-25).

$$V = V_R - IZ$$

**Where**

$V$  = Feeder end voltage ( $V$ )

$V_R$  = Rated transformer voltage (240 V)

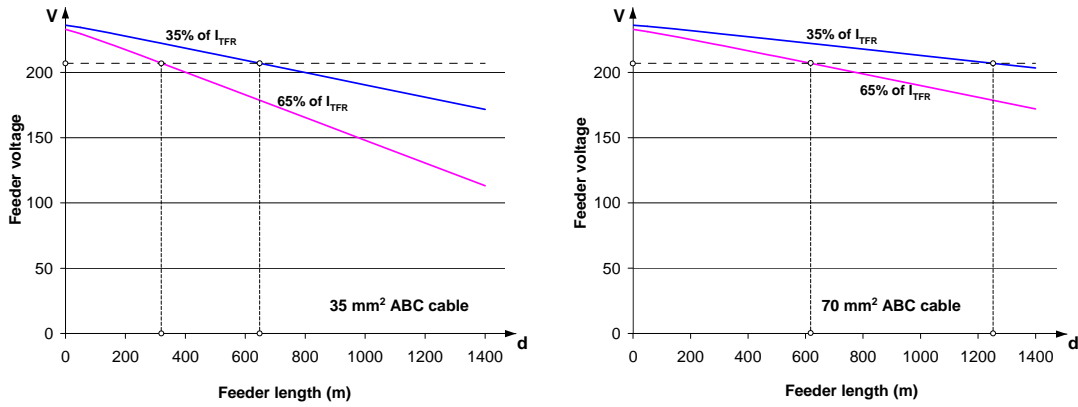
$I$  = Feeder current (35 % - 65 % of  $I_{TFR}$ )

$Z$  = Network impedance

$d$  = Feeder length / distance

$$= V_R - I \sqrt{\left( R_{TF} + 2R_{ABC} \frac{d}{1000} \right)^2 + \left( X_{TF} + 2X_{ABC} \frac{d}{1000} \right)^2} \quad (4-25)$$

The feeder voltage versus distance obtained from Equation (4-25) is plotted in Figure 4-36, with the distances at which the feeder voltage reaches 230 V – 10 % indicated.



**Figure 4-36: Feeder voltage versus length (MV line at rated voltage)**

The fault level currents corresponding to the distance at which the feeder voltage falls to 230 V – 10 %, can now be calculated from Equation (4-26).

$$I_{SC} = \frac{V_R}{Z}$$

**Where**

$I_{SC}$  = Fault level current (A)

$V_R$  = Rated transformer voltage (240 V)

$Z$  = Network impedance

$d$  = Feeder length / distance

$$= \frac{V_R}{\sqrt{\left(R_{TF} + 2R_{ABC} \frac{d}{1000}\right)^2 + \left(X_{TF} + 2X_{ABC} \frac{d}{1000}\right)^2}} \quad (4-26)$$

The feeder lengths corresponding to the 230 V – 10 % feeder voltage is summarized Table 4-15 together with the fault currents. The influence of a  $\pm 5\%$  MV line voltage variation on the feeder length is also included in the table.

**Table 4-15: Feeder length & fault current (MV line at rated voltage  $\pm 5\%$ )**

Feeder current	MV voltage	Feeder length (d)		Fault current ( $I_{SC}$ )
		35 mm <sup>2</sup> Cable	70 mm <sup>2</sup> Cable	
35 % $I_{TFR}$	95 %	392 m	754 m	253 A
	100 %	649 m	1253 m	170 A
	105 %	905 m	1750 m	131 A
65 % $I_{TFR}$	95 %	182 m	347 m	469 A
	100 %	323 m	619 m	314 A
	105 %	461 m	889 m	243 A

From these values it can be seen that the most suitable position to install the EVR onto the feeder is influenced significantly by the expected MV line voltage and the feeder current.

If the MV voltage at a specific site is unknown, the EVR position is selected according to an assumed MV voltage of 100 %. The fault currents will thus deviate  $\pm 5\%$  from the indicated values of 170 A and 314 A with an MV voltage change of  $\pm 5\%$ .

On the other hand, if the MV voltage at a particular site is known to be either low or high, a more suitable / appropriate position for the EVR can be selected, based on the MV voltage. This will result in fault currents between 131 A and 469 A at respectively 105 % and 95 % of the rated MV voltage,

The maximum expected fault current will thus vary between 131 A and 469 A, depending on the position of the EVR along the feeder. The minimum fault current will depend on the length of the feeder downstream of the EVR, which is not discussed at this point. Consequently the EVR protection coordination is designed to operate up to a maximum fault level of 500 A.

#### **4.10.2 Implementation**

Due to the relative high power losses inside power semiconductors they cannot be compared with traditional network components such as circuit breakers and feeders with regard to the magnitude and duration of fault currents that can be sustained. Implementing coordinated

protection thus requires that the thyristors used in the tap switches be over rated at the expense of higher system cost.

To minimize this cost implication, only one thyristor switch is over rated to such an extent that coordinated protection can be implemented. Whenever an excessive load current is detected (in excess of the minimum expected fault current), this thyristor switch (SKKT162 thyristor module) is turned on until the fault is cleared.

#### 4.10.2.A Protection curves

In Figure 4-37 the current versus time capability of the thyristor switch (“SKKT162 thyristor”) is plotted together with the tripping curves for the various circuit breakers in the EVR (“100A Curve1”), pole top box (“50A curve1”) and customer meter (“20A curve2”).

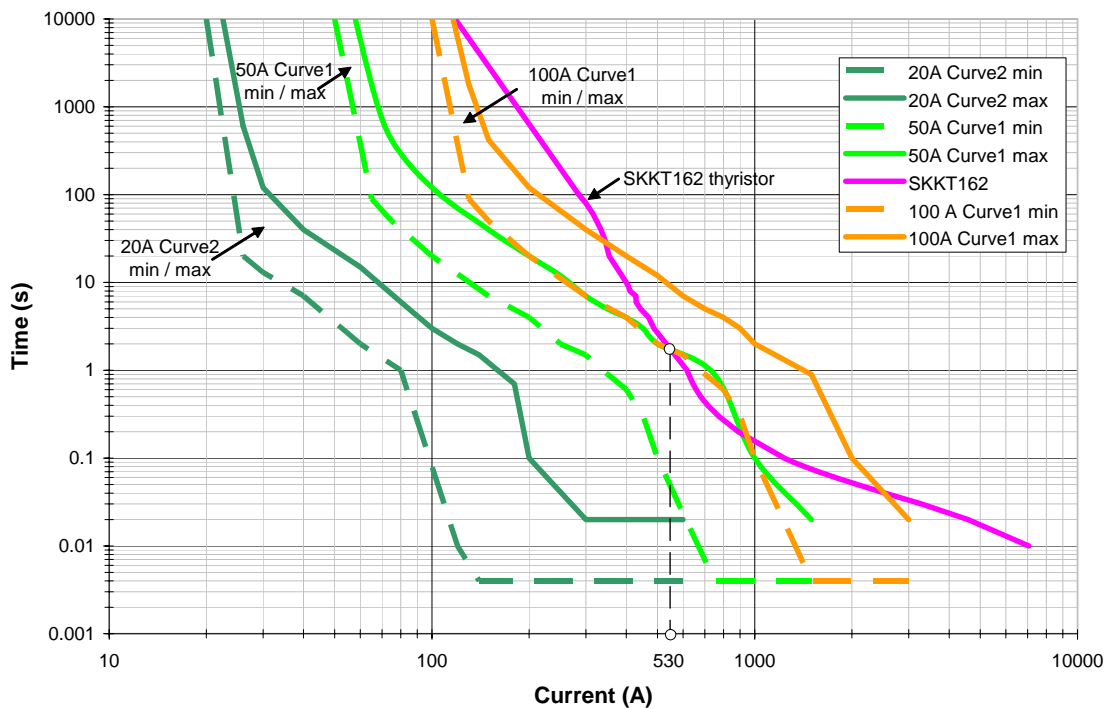


Figure 4-37: Protection curves (EVR load = 2.5 kVA,  $T_{\text{internal}} = 45\text{ }^{\circ}\text{C}$ )

The thyristor current handling capability is determined by the difference between the thyristor’s maximum allowable junction temperature and the junction temperature at the time instant just preceding the short circuit. The junction temperature in turn, depends on the thyristor heat sink temperature and the thyristor current. The curve “SKKT162 thyristor” is calculated with the EVR operating with a thyristor current of 12.5 A (~2.5 kVA) and a heat sink temperature of 50 °C (equivalent to an internal ambient temperature of 45 °C).

Protection coordination requires that the thyristor should be able to conduct the fault current for longer than the 50 A curve 1 maximum tripping time. As can be seen from Figure 4-37 the thyristor is capable of doing this up to a current magnitude of 530 A, which is in excess of the maximum expected fault current of 500 A.

#### 4.10.2.B Digital implementation

Since the EVR is controlled by a digital controller, implementing this continuous time current tripping curve necessitate it to be broken up into discrete steps. This leads to the staircase curve “EVR trip – no restrictions” in Figure 4-38. The greater the number of steps, the closer the staircase curve will approach the actual thyristor capability. Due to memory and processing time constraints within the controller a compromise must however be made between resource usage and the accuracy / resolution of the staircase tripping curve.

Imposing the 500 A maximum fault level restriction on this curve and preventing the thyristor from staying on so long that it would trip the EVRs own 100 A CB, the curve “EVR trip curve” is derived. This curve is implemented in the controller and controls the EVRs tripping time.

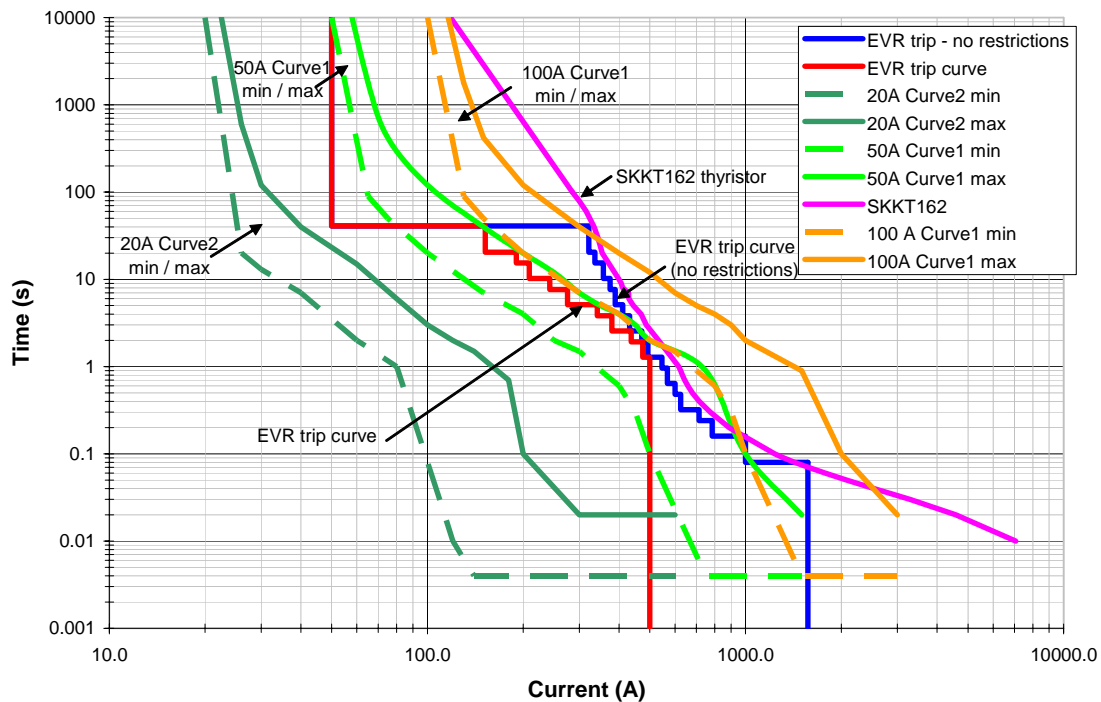
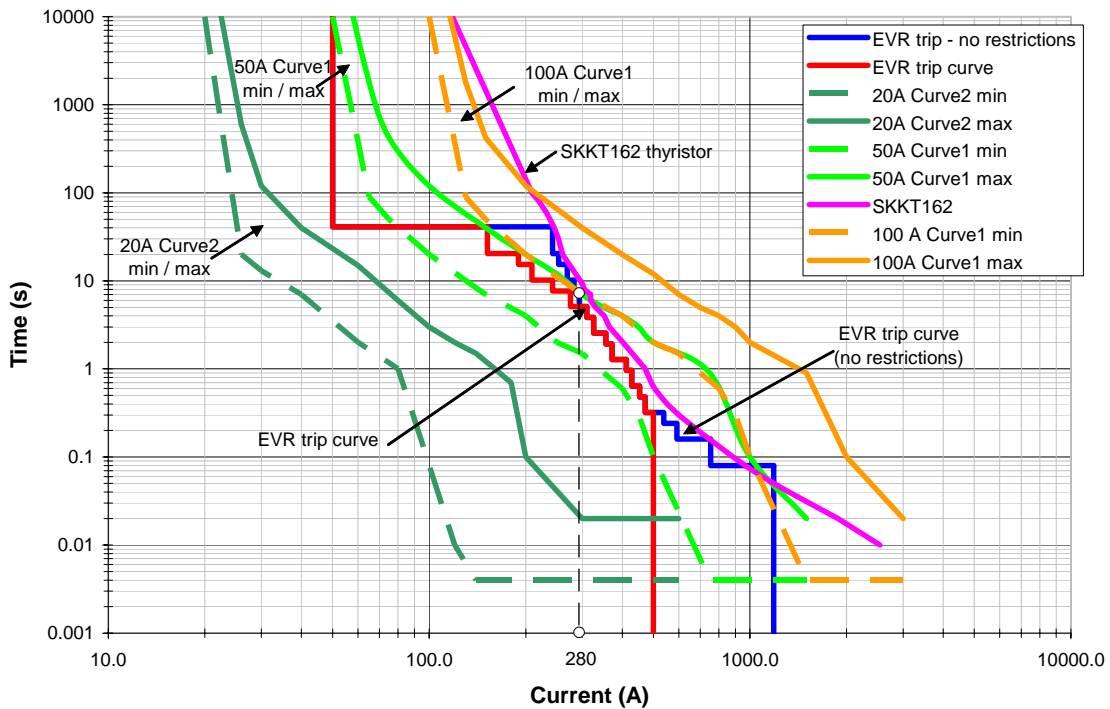


Figure 4-38: Protection coordination curve (EVR load = 2.5 kVA,  $T_{\text{internal}} = 45\text{ }^{\circ}\text{C}$ )

With varying loads the thyristor current versus time tripping curve must be modified to reflect the changes in the operating conditions (load current and heat sink temperature). The conditions / parameters are measured by the controller and are used to obtain a new current versus time

curve that will protect the EVR from self destruction during short circuits. To illustrate the effect of these parameters, the thyristor current handling capability curve with a thyristor current of 50 A (~10 kVA) and a heat sink temperature of 62 °C (corresponding to an internal ambient temperature of 45 °C), is shown in Figure 4-39.



**Figure 4-39: Protection coordination curve (EVR load = 10 kVA,  $T_{\text{internal}} = 45 \text{ }^{\circ}\text{C}$ )**

Under these operating conditions the EVRs tripping curve cannot be maintained close to the maximum tripping curve of the 50 A CB for the entire fault current range (150 A to 500 A). It does however stay above the minimum CB tripping curve, which implies that coordinated protection might be possible, but cannot be guaranteed.

If the EVR is unable to sustain the fault current (coordinated protection is not possible), it will turn off for a preset time period, during which it will cool slightly. When the EVR restarts itself a new tripping curve will be calculated based on the slightly lower heat sink temperature and an operating current of 0 A. This will allow for a much improved thyristor current capability, capable of successfully tripping the circuit breaker.



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## **Chapter 5**

Control circuit design

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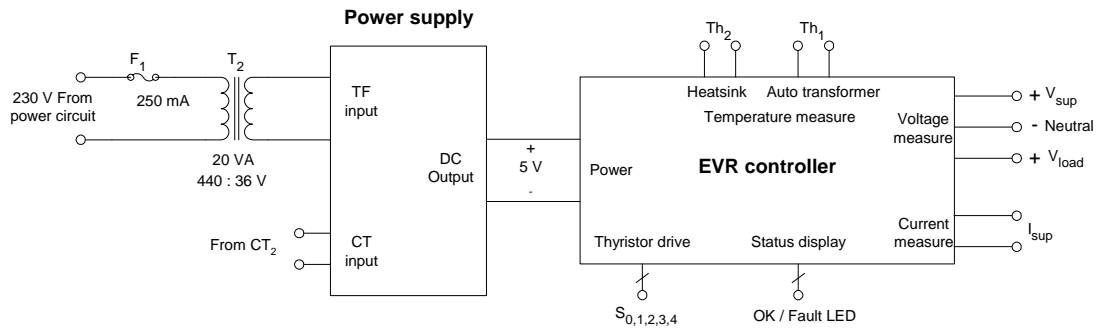
## 5 Control circuit design

The previous chapter described the hardware used in the power circuit of the EVR. This chapter focuses on the design of the controller and its power supply, to enable control of the hardware. Various topologies to be used in the power supply are evaluated and the preferred topology is designed in detail. A description of the controller together with its measurement circuitry and thyristor drive circuits is provided.

### 5.1 Overview

The control circuitry of the EVR consists of the following components as shown in the circuit diagram in Figure 5-1:

- Power supply
- EVR controller



**Figure 5-1: EVR control circuit**

The power supply provides the necessary low voltage DC power to the controller board. Two power sources feed the power supply board, a primary source and a secondary source. The primary source is obtained from the low power step down transformer ( $T_2$ ), which is connected to the EVR's supply input via a fuse ( $F_1$ ). The secondary source is obtained from  $CT_2$ , which measures the output current of the EVR. During short circuit conditions (which could last for several seconds), the EVR controller needs power to implement the coordinated tripping scheme. As the supply voltage will be close to zero during short circuits, the necessary power is obtained from the secondary source.

The EVR controller is responsible for controlling the entire system. This consists of processing all the measurements, implementing the protection measures and controlling the tap switching of the auto-transformer.

## **5.2 Power supply**

To enable the EVR controller to function, a low voltage DC power supply is needed. In designing the power supply, three possible power supply topologies were considered:

- Line powered switch mode power supply
- Transformer with a linear power supply
- Transformer with a low voltage switch mode power supply

The relative complex circuitry associated with a line powered switch mode power supply operating from a high input voltage could lead to reliability problems and long development times. A transformer based power supply is therefore seen as a more viable alternative even though it is less compact. In the transformer based power supply, the high voltage is stepped down to a lower level, before being processed by either linear or switch mode regulators. As the expected supply voltage varies over a huge span, linear regulators would lead to excessive power dissipation. Consequently a low power switch mode regulator is the preferred choice.

### **5.2.1 Requirements**

To minimize the costs involved in the power supply board, the EVR controller is designed to operate from only positive power supply rails. The controller accepts two supply rails; one powers the DSP and associated circuitry, while the other provides power to the thyristor driving circuitry. Both rails are operated from +5 V to decrease the component count and reduce the cost on the power supply board. Although the controller's current requirement at +5 V is only 300 mA (see the controller power requirement on page 128), additional capacity should be provided for future additions.

Under normal circumstances the supply voltage to the power supply transformer will be  $230\text{ V} \pm 10\%$ . The transformer must however be capable to provide sufficient power over a wide input voltage range, to account for abnormally high or low supply voltage that might occur. Under certain conditions, loss of a neutral connection can cause the supply voltage to increase to 440 V ( $400\text{ V} + 10\%$ ). On the other hand, due to transformer overloading, supply voltages as low as 115 V might occur. The transformer input range is therefore defined between 115 V up to 440 V. However, during short circuit conditions the supply voltage will collapse and could drop as low as 0 V, depending on the feeder impedance between the EVR and the location of the fault. The power supply transformer would therefore be incapable of delivering any power to the system and an alternative power source must be used.

## 5.2.2 Design

The topology chosen is a transformer based low voltage switch mode power supply with an input supply voltage range of 115 V to 440 V<sub>rms</sub>. During normal operation most of the power is obtained from the transformer. To provide power during short circuits, the output from a current transformer (measuring the output current) is used to obtain the necessary power. Noting that the total controller power consumption is equal to 1.5 W, the current transformer should be capable of providing at least this amount of power.

To enable future modifications / additions to be made to the EVR, without redesigning the power supply, the power supply is designed to provide 1.2 A. One such addition is the EVR logger. This is an optional addition to the system, used to log the input and output voltages and currents to enable monitoring of the system performance.

### 5.2.2.A Overview

A block diagram of the power supply is shown in Figure 5-2. The supply voltage is stepped down through the power supply transformer, to provide a low voltage AC power supply to the power supply board. The power supply board consists of a front end circuit and the switch mode regulator circuit. The front end accepts the incoming AC voltage and the CT output current and rectifies it to provide a DC link voltage. The switch mode regulator circuit uses the DC link voltage to create a regulated DC output. The regulated output is independent of variations on the DC link caused by a varying transformer supply voltage or a varying output current from the current transformer.

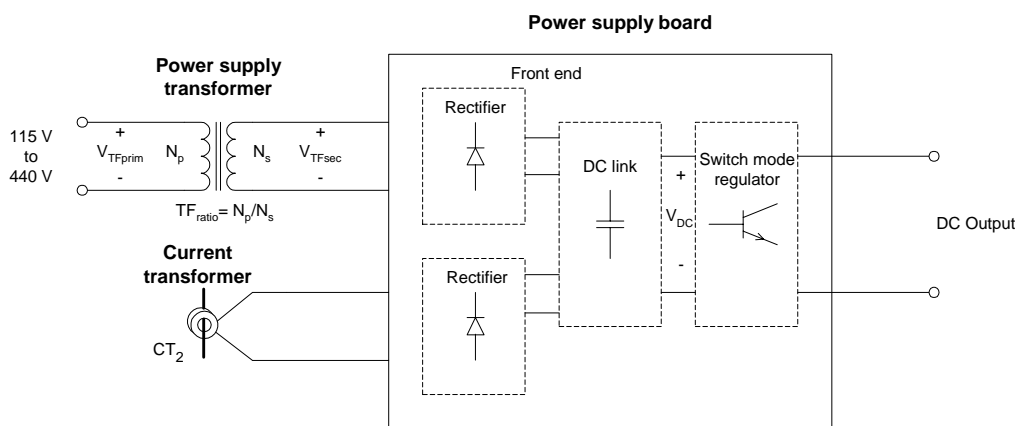
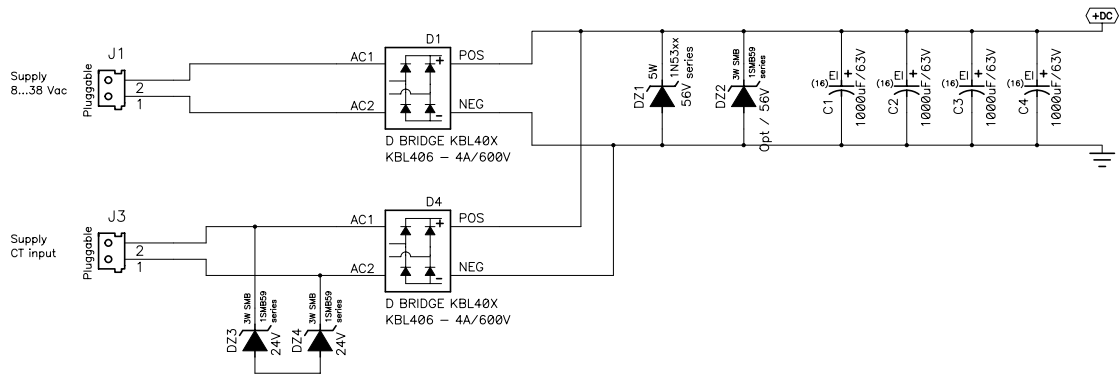


Figure 5-2: Power supply block diagram

### 5.2.2.B Power supply board

The switch mode regulator front end circuit is shown in Figure 5-3. The power supply board accepts AC power from the power supply transformer and the current transformer that powers

the board during short circuits. Two 24 V back-to-back zener diodes are connected across the CT terminals to ensure that the CT is never unloaded. The AC input is rectified by a full bridge rectifier and filtered by a capacitor bank to create a DC link voltage. A 56 V zener diode is connected across the DC link to protect the switch mode regulator against over voltages.



**Figure 5-3: Switch mode regulator circuit - front end**

The switch mode regulator itself consists of a buck regulator operating at a frequency of 150 kHz, along with its associated circuitry as shown in Figure 5-4.

The regulator IC (LM2592HVS) can operate from a DC link voltage as low as the required output plus 1.2 V, up to 60V. To allow a safety margin for the operation of the 56 V DC link over voltage protection zener diode used in the front end, a maximum DC link voltage of 55 V is however used. The output voltage can be adjusted through resistance  $R1$ ,  $R3$  and  $R2$ . The regulator adjusts its output voltage in such a manner that the feedback voltage at “pin 4” equals 1.23 V. Additional filtering is provided with the inclusion of  $L5$  and  $C7$ , to minimize the output voltage ripple. The efficiency of the switch mode regulator is in excess of 70 %.

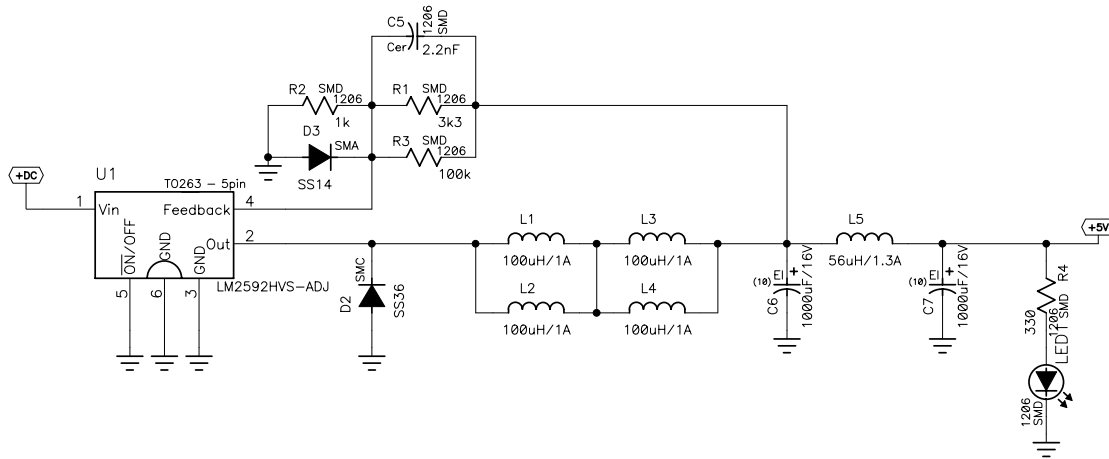


Figure 5-4: Switch mode regulator circuit

### 5.2.2.C Power supply transformer

To specify the transformer, the winding ratio is calculated based on the supply voltage to the transformer and the DC input voltage range of the power supply board. The transformer power rating is then estimated based on the power requirements of the power supply board and an assumed transformer efficiency. The influence of the transformer voltage regulation on the DC link voltage is then investigated and modifications made regarding the transformer size.

#### Winding ratio

To calculate the winding ratio of the transformer ( $TF_{ratio}$ ) the supply voltage range to the transformer input (115 V to 440 V<sub>rms</sub>) and the DC voltage range from which the switch mode converter can operate (6.2 V to 55 V<sub>dc</sub>) is used. Using the power supply block diagram in Figure 5-2, the relationship between the DC link voltage and transformer input voltage under no load conditions can be derived as shown in Equation (5-1).

$$V_{DC} = \frac{\sqrt{2} \times V_{TF_{prim}}}{TF_{ratio}} - 2V_{diode} \quad \text{Where} \quad (5-1)$$

$V_{DC}$  = DC link voltage (V)

$V_{TF_{prim}}$  = TF input voltage (V)

$TF_{ratio}$  = TF winding ratio (Prim:Sec)

$V_{diode}$  = Diode voltage drop (V)

Solving Equation (5-1) for the transformer winding ratio with the maximum supply voltage present leads to:

$$TF_{ratio} = 11$$

**With**

$$V_{DCmax} = 55 \text{ V}$$

$$V_{TFprim} = 440 \text{ V}$$

$$V_{diode} = 0.7 \text{ V}$$

To verify that the calculated transformer winding ratio will satisfy the minimum DC input voltage required by the switch mode regulator, Equation (5-1) is evaluated with the minimum supply voltage. This results in a DC link voltage of 13.39 V, which is higher than the required 6.2 V.

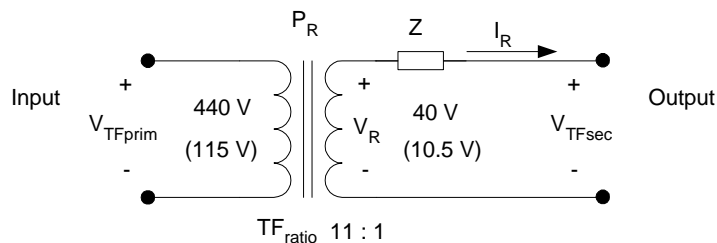
### Power rating

The power requirement of the power supply board supplying a load with 1.2 A at +5 V and operating with an assumed efficiency of 70 % is equal to 8.6 W. Assuming an efficiency of 80 % for the transformer, the required transformer VA rating is calculated to be at least 10.8 VA (ignoring the power factor introduced by the power supply board).

At 10.8 VA, the current drawn by the transformer's primary winding will be 94 mA and 25 mA at 115 V and 440 V respectively. The conductors used in the primary winding must therefore be rated for 94 mA, resulting in a transformer power rating of 41.4 VA at 440 V (even though only 10.8 VA will be drawn).

### Voltage regulation

Due to the poor voltage regulation of transformers with a low VA rating (caused by the high impedance of the thin conductors used in the windings), the influence of the voltage drop across the transformer on the DC link voltage needs to be examined. The voltage drop across the windings is made worse if non sinusoidal currents with high peak values are drawn, such as that drawn by the diode capacitor front end of the power supply. A simple model of the power supply transformer used to evaluate the voltage regulation, is shown in Figure 5-5.



**Figure 5-5: Power supply transformer model**

From the transformer model in Figure 5-5, the following relationship can be found between the impedance ( $Z$ ) and the voltage regulation ( $r$ ).

---


$$Z = \frac{V_R \left( \frac{r}{100} \right)}{I_R} = \frac{V_R^2 \left( \frac{r}{100} \right)}{P_R} \quad \text{Where} \quad (5-2)$$

$Z =$  Transformer impedance ( $\Omega$ )  
 $r =$  Transformer voltage regulation  
 $V_R =$  Rated transformer secondary voltage ( $V$ )  
 $I_R =$  Rated transformer secondary current ( $I$ )  
 $P_R =$  Rated transformer power ( $W$ )

---

Assuming a typical voltage regulation figure of 10 % for a 40 VA transformer, the transformer impedance at 440 V can be calculated using Equation (5-2) as shown below.

---


$$Z_{440V} = \frac{V_R^2 \left( \frac{r_{440V}}{100} \right)}{P_R} = 4 \Omega \quad \text{Where}$$

$r_{440V} =$  Voltage regulation at 440 V (10 %)  
 $V_R = 440 V$   
 $P_R = 40 W$

---

The impedance of the windings is fixed at 4  $\Omega$ . If the supply voltage is now reduced by a factor of approximately 4 (440 V to 115 V), the voltage regulation that can be achieved at this voltage with the fixed impedance can be calculated from rewriting Equation (5-2) as follow.

---


$$r = \frac{Z P_R}{V_R^2} 100 \quad (5-3)$$


---

The voltage regulation at 440 V and 115 V is thus:



---


$$r_{440V} = \frac{Z_{440} P_R}{V_R^2} 100$$

and

$$r_{115V} = \frac{Z_{440V} P_R}{\left(\frac{1}{4} V_R\right)^2} 100$$

$$= 16 \frac{Z_{440V} P_R}{V_R^2} 100$$

$$= 16 r_{440V}$$

**Where**

$r_{440V}$  = Transformer voltage regulation at 440 V

$r_{115V}$  = Transformer voltage regulation at 115 V

$Z_{440V}$  = Transformer impedance at 440 V ( $\Omega$ )

(5-4)

---

The voltage regulation at 115 V is 16 times worse than the voltage regulation at 440 V, which will lead to an unacceptable output voltage. Noting that the power supply board will only use 10.8 VA, which is approximately a quarter of the rated transformer power; a new voltage regulation figure can be calculated at 115 V from Equation (5-4).

---


$$r_{115V}^{10VA} = 16 \frac{Z_{440V} \frac{P_R}{4}}{V_R^2} 100$$

$$= 4 \frac{Z_{440V} P_R}{V_R^2} 100$$

$$= 4 r_{440V}$$

**Where**

$r_{115V}^{10VA}$  = Transformer voltage regulation at 115 V, 10VA

(5-5)

---

The voltage regulation at 115 V, with 10 VA drawn from the transformer has been improved by a factor of four compared to the voltage regulation with a load of 40 VA. With the original 10 % voltage regulation at 440 V, the voltage regulation at 115 V is thus 40 %.

To include the effect of the voltage regulation on the DC link voltage, Equation (5-2) which shows the relationship between the DC link voltage and the transformer input voltage under no load condition is modified as shown in Equation (5-8).

---


$$V_{DC} = \frac{\sqrt{2} \times V_{TF_{prim}} \left(1 - \frac{r}{100}\right)}{TF_{ratio}} - 2V_{diode} \quad \text{Where} \quad (5-6)$$

$r = \text{Voltage regulation}$   
 $V_{TF_{prim}} = \text{TF input voltage (V)}$   
 $TF_{ratio} = \text{TF winding ratio}$   
 $V_{diode} = \text{Diode voltage drop (V)}$

---

To determine if the voltage regulation at 115 V, will deliver a high enough DC link voltage for the power supply board to function, Equation (5-6) is evaluated, which leads to:

---


$$V_{DC} = 6.87 \text{ V} \quad \text{Where} \quad (5-7)$$

$r = 40$   
 $V_{TF_{prim}} = 115 \text{ V}$   
 $TF_{ratio} = 11$   
 $V_{diode} = 1 \text{ V}$

---

Although this voltage is marginally higher than the minimum input of 6.2 V required, it should be noted that the actual voltage will be reduced further due to:

- **Non sinusoidal load currents**

The peak transformer output voltage will be reduced due to the high peak current pulses drawn by the switch mode regulator front end. The magnitude of the voltage reduction depends on the current form factor, which is defined by the impedance of the transformer and the power supply board.

(The current form factor is the ratio of the RMS value of the current divided by its average value. It can typically vary between 1.11 (for sinusoidal currents) and 5.)

- **Ripple on the DC link**

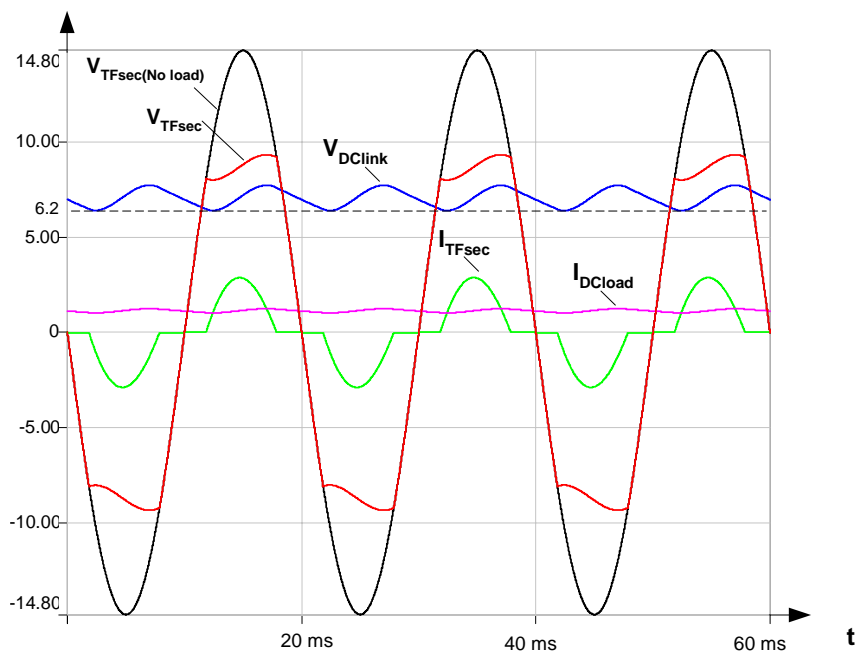
A certain amount of ripple will be present on the DC link. Near the peak value of the rectified AC voltage the capacitors will be charged with a short pulse current. As the sinusoidal AC voltage decreases naturally, the capacitor voltage will decrease slowly while they are discharged into the load. The capacitors will discharge until the rectified AC voltage is again larger than the DC voltage. The minimum value of the DC link will determine if the output voltage can be maintained.

- **Assumed efficiency**

In determining the power needed from the transformer, a transformer efficiency of 80 % was assumed. Due to the high transformer impedance at 115 V, this assumption is not valid at 115 V. Consequently the amount of power required from the transformer at 115 V will increase, leading to a poorer voltage regulation and lower DC link voltage.

Considering all the factors above, it is clear that the minimum DC link voltage requirement will not be fulfilled. A transformer with reduced copper losses, leading to a much better voltage regulation is thus required.

Using a computer simulation with the transformer connected to the switch mode power supply front end and an 8.6 W load, it is established that a transformer impedance of approximately  $2.1 \Omega$  is needed to fulfill the minimum DC link requirement. The simulation is shown in Figure 5-6, with the transformer secondary voltage and load and current ( $V_{TFsec(No\ load)}$ ,  $V_{TFsec}$ ,  $I_{TFsec}$ ) and the DC link voltage ( $V_{DClink}$ ) and DC load current ( $I_{DCload}$ ). The current pulses drawn from the transformer are not sinusoidal as expected and a 1.76 V ripple is present on the DC link.



**Figure 5-6: Power supply simulation** (TF primary voltage of 115  $V_{RMS}$ )

To manufacture the transformer, the required specifications (input voltage range, winding ratio, impedance required and power rating at the minimum supply voltage) were given to a transformer manufacturer to manufacture.

### 5.2.2.D Current Transformer

To supply power to the power supply board during short circuit conditions a current transformer (CT) measuring the load current is employed. Because the expected fault current varies between 150 A and 500 A, a 150:1 current ratio was selected. The power rating of a typical commercially available CT is too low to supply enough power to operate the power supply board at its full rating. Noting that the power supply board is over designed and that the EVR controller will only require 1.5 W (see controller power requirements in Table 5-4 on page 129), a CT with a power rating of 2.5 VA is chosen.

### 5.2.2.E Summary

A summary of the power supply characteristics is given in Table 5-1, together with a picture of the power supply board and transformer in Figure 5-7.

**Table 5-1: Power supply characteristic**

---

<b>Transformer</b>		
Input voltage		115 to 440 V <sub>rms</sub>
Rating: Power		20 VA at 115 V
Impedance		Less than 2.1 Ω
Winding ratio		11 : 1 (Primary : Secondary)
<b>Power supply board</b>		
Input: Transformer		10.5 to 40 V <sub>rms</sub>
Current transformer		2.5 VA, Ratio 150:1 A
Output: Voltage		+5 V <sub>DC</sub>
Current		1.2 A

---



a) Power supply board

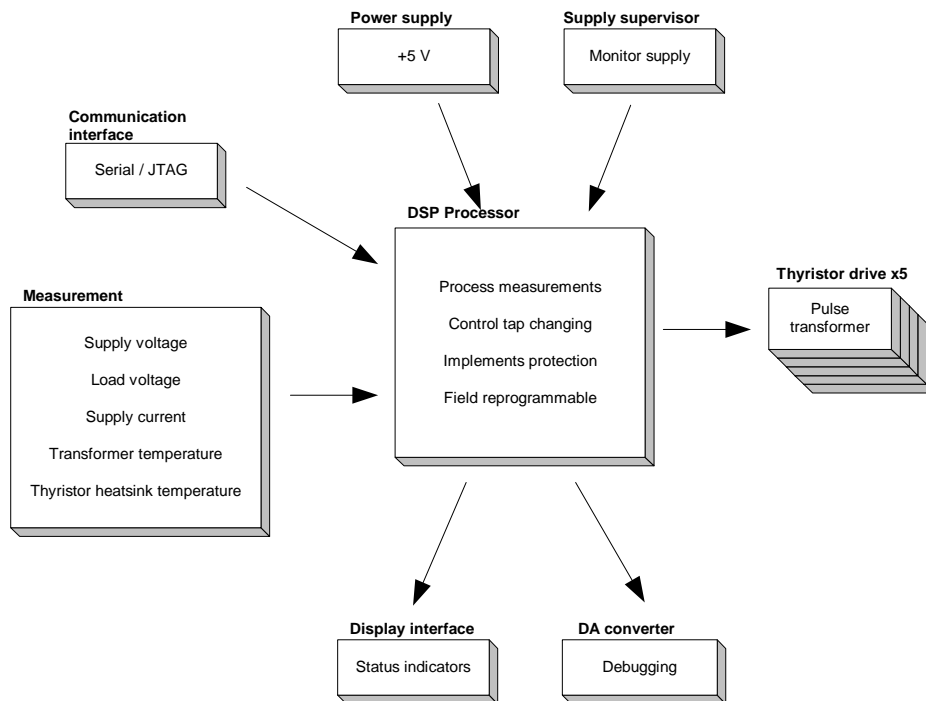


b) Power supply transformer

**Figure 5-7: Power supply board & transformer**

### 5.3 EVR Controller

The EVR controller is based on a digital signal processor (DSP) to which all the necessary measurements are relayed. A block diagram of the controller is shown in Figure 5-8.

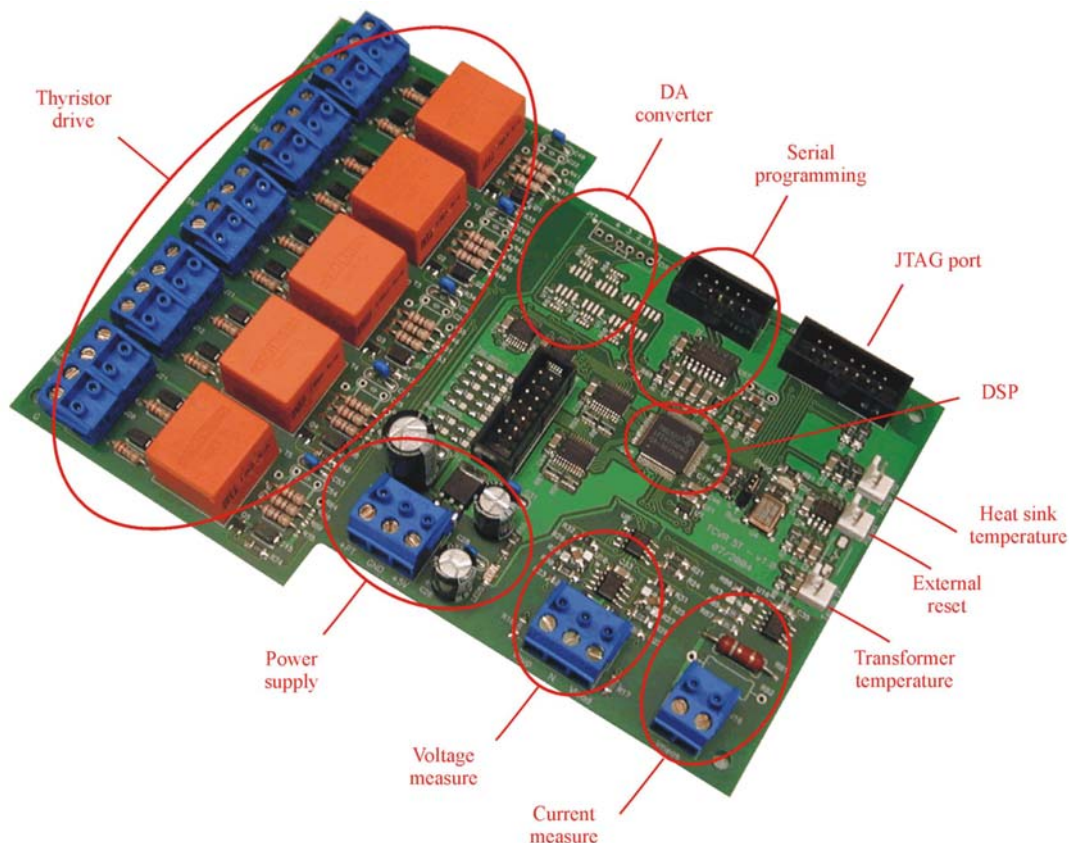


**Figure 5-8: Controller block diagram**

The DSP forms the core of the controller and performs all the calculations and processing of measurements needed for tap changing and protection of the EVR. To ensure reliable operation a supply supervisor monitors the supply voltage and reset the DSP if the supply voltage is too low. The DSP is field reprogrammable through either a serial or a JTAG interface and can be password protected to prevent unauthorized access / tampering to the DSP code. Measurements include the supply and load voltage, supply current and auto-transformer winding and thyristor heat sink temperature.

The controller makes provision for a number of LED indicators to aid in code development purposes and also provide monitoring of the EVRs operational and error states. A digital to analog converter, exclusively used in code development / debugging purposes, is also included in the system. To activate the thyristors used in the tap switches, pulse transformers are employed to provide the necessary isolation

A picture of the controller is shown in Figure 5-9. To minimize production costs, the controller layout was done utilizing only a double-sided printed circuit board (PCB).



**Figure 5-9: Controller picture**

In the next sections, each of the fundamental blocks in the controller is described.

### 5.3.1 DSP processor

The DSP processor used is the TMS320F2403A from Texas Instruments. This processor is a 16 bit fixed point processor with a performance of 40 million instructions per second (MIPS).

The processor has a number of on-chip features that simplifies the controller design, which include:

- On chip memory:
  - FLASH - 16 kWord
  - SARAM – 512 Word
  - DARAM – 544 Word
- ADC - 10 bit, 8 channel with 500ns conversion time
- SCI port
- SPI port
- Digital I/O pins
- Timers – 2 x 16 bit
- PWM generation

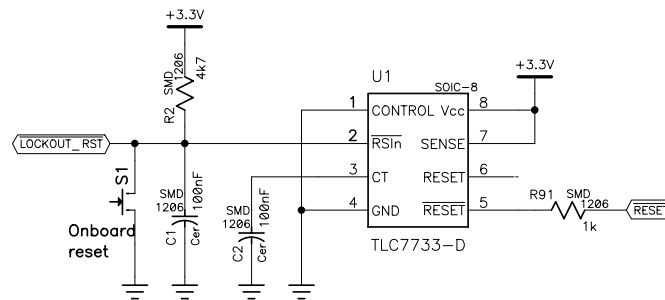
### 5.3.2 Supply supervisor

To enable the DSP to operate in a predictable manner, the supply voltage to the DSP must remain within certain limits. If the supply voltage falls too low, the DSP will not function correctly and the system needs to be informed and act on this. This also applies to the power-up state, during which the supply voltage will rise from 0 to 3.3V within a finite time.

Accomplishing predictable behaviour necessitate the use of a supply supervisor circuitry as shown in Figure 5-10. During the power-up state the supply supervisor activates the DSP “/RESET” pin, thus keeping the DSP from performing any instructions. Once a valid supply is detected, the “/RESET” signal is deactivated, and the DSP can start executing code.

The supply supervisor continues to monitor the supply voltage after the power-up state. If the supply voltage goes below a lower threshold, the “/RESET” signal will once again be activated, to force the DSP into a known operation state.

Provision was also made for an onboard manual reset, through activating the reset pushbutton “SI” and an external reset “/LOCKOUT\_RST”. Both these reset sources can be omitted from future designs, as they were used for development purposes only.



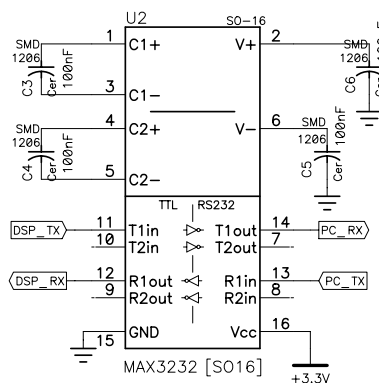
**Figure 5-10: Supply supervisor circuit**

### 5.3.3 Communication interface

Communication with the DSP can be accomplished either by using a serial link interface through the SCI or through the JTAG interface.

The serial interface is based on the RS232 serial interface, which enables the DSP to be connected to a PC through a simple serial cable. Since the signal levels on the DSP is not compatible with that of the RS232 specification, a level translator circuitry is used as shown in Figure 5-11.

Through use of the serial interface the FLASH memory containing the program code can be programmed. Information can also be exchanged between the DSP and PC with the appropriate software.

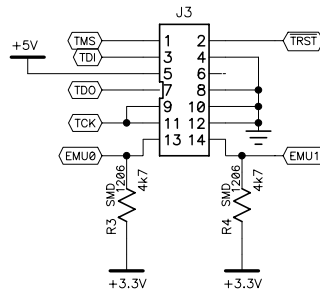


**Figure 5-11: RS232 interface circuit**

The JTAG interface seen in Figure 5-12, enables communication between a PC and the DSP through the use of a JTAG emulator. This emulator is expensive but has the benefit of not only



being capable the program the FLASH memory with the program code, but to read the memory and registers in the DSP to facilitate in the development and debugging of the software code.



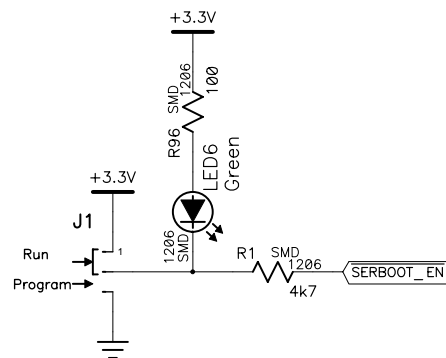
**Figure 5-12: JTAG interface circuit**

### 5.3.4 DSP programming

The DSP can be programmed either through the serial interface or JTAG port. Programming the DSP using the serial interface requires a jumper setting to be made on the controller.

Setting the jumper “J1” (Figure 5-13) to the “PROG” position, will activate the serial boot-loader code on the DSP. This code sets up the SCI on the DSP, to enable communication with the PC through the serial link.

The controller ground is connected to neutral through the voltage measurement connections. To prevent damage to the PC’s serial port, care must be taken to ensure that either the PC ground is floating, or that the voltage measurement connector plug are unplugged, before the serial link connection is made.



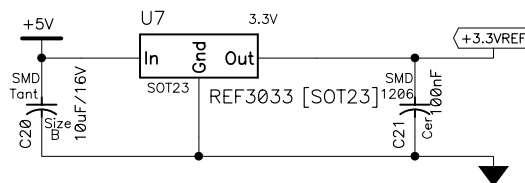
**Figure 5-13: Serial programming circuit**

## 5.3.5 Measurements

### 5.3.5.A Analog to digital converter

The DSP is equipped with a single onboard analog to digital (AD) converter capable of accepting 8 analog input channels through a multiplexer. The multiplexer connects the AD converter to a specific input channel which then samples and converts the voltage on the channel to an equivalent digital representation. The input channels can only accept positive voltages between a lower (minimum of 0 V) and upper (maximum of 3.3 V) reference and produce an output code with a 10 bit resolution ranging between 0 and 1023.

To utilize the full input range of the AD converter, the lower and upper reference is connected to 0 and 3.3 V respectively. In the digital controller substantial noise can be generated onto the 3.3 V power supply rails. To prevent this noise from interfering with the accuracy of the AD converter a precision 3.3 V band gap reference IC with an accuracy of 0.2 % accuracy is used to generate a separate 3.3 V reference as shown in Figure 5-14. The AD converter's upper reference is connected to this 3.3 V reference, instead of connecting it directly to the noisy 3.3 V power supply rail.



**Figure 5-14: Analog reference circuit**

To further improve the accuracy of the AD converter due to noise present on the ground power rail, a separate analog ground power rail is created, connected to the digital ground at one point only. This analog ground is connected to the lower reference input of the AD.

Because the EVR is used in an AC system, voltage and current measurements will be of an AC nature (swinging both positive and negative with respect to neutral / ground). Since the AD converter can only accept positive voltages an offset needs to be added to these signals before they can be connected to the AD converter. To obtain maximum swing, an offset voltage of 1.65 V needs to be added to all the AC measurements. This offset voltage is derived from the 3.3 V band gap reference.

### 5.3.5.B Voltage measurement

#### Requirement

The supply voltage to the EVR under normal conditions is a maximum of  $253 V_{\text{rms}}$  ( $230 V_{\text{rms}} + 10\%$ ). Since the system must be able to detect over voltage conditions, the measurement circuit should be designed with some extra margin. Provision is therefore made to measure voltages up to  $264.5 V_{\text{rms}}$  ( $230 V_{\text{rms}} + 15\%$ ).

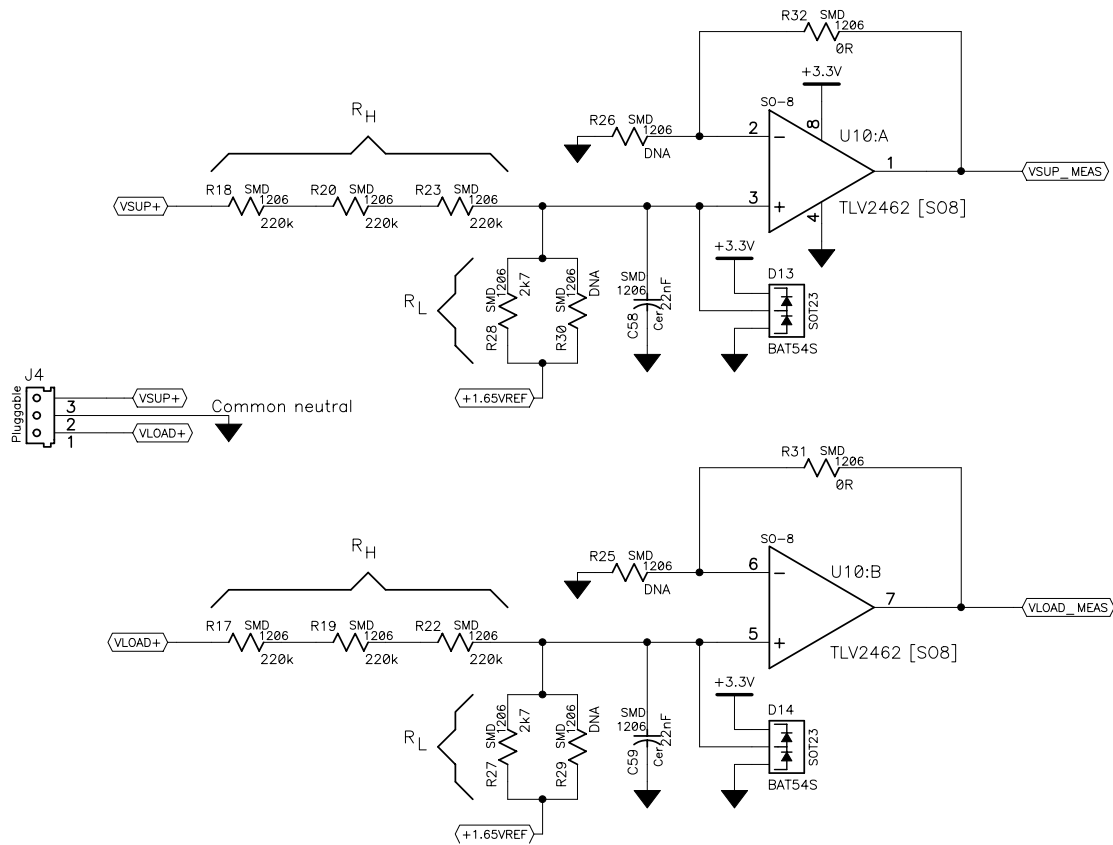
Measurement of the supply / load voltages involves transforming these signals to be compatible with the input range of the AD converter. Since the AD converter can only accept voltages in the range of 0 to 3.3 V, the supply / load voltage must be scaled down to a lower magnitude and due to their AC nature, an offset voltage also needs to be added.

#### Measurement circuitry

Since the supply and load voltages are of the same magnitude, an identical measurement circuit is used for both as shown in Figure 5-15. Because no electrical isolation exists between the input and output of the EVR, due to the auto-transformer being used, both the supply and load share a common neutral connection. To simplify the measurement circuitry, neutral is also connected to the power supply ground.

Although rail to rail operation amplifiers are used in the design, their current sink / source capability with an output voltage close to the power supply rails are limited. To prevent this from affecting the accuracy of the measurements the circuit is designed for a voltage swing of 3.05 V instead of 3.3 V, limiting the voltage swing to 125 mV from the supply rails.

The supply / load voltage are scaled down to 3.05 V peak to peak, using a resistive divider circuit consisting of  $R_H$  and  $R_L$ . Addition of the 1.65 V reference allows the measured signal to swing around approximately 1.65 V. (The measurement circuitry does not provide an output swing that is 100% symmetrical around the 1.65 V offset voltage. A slight DC offset error is introduced through the addition of the 1.65 V reference. This offset is very small and can be removed through coding in the DSP software.) Due to the high impedance of the measurement circuit, the measured signal must be buffered to provide enough current sink / source capability to drive the AD converter input. Clamping diodes *D13*, *D14* prevent over voltage conditions from damaging the amplifier.



**Figure 5-15: Voltage measurement circuit**

Relating the supply / load voltage to the measurement output voltage for the circuit in Figure 5-15, leads to Equation (5-8):

$$V_{meas} = \left[ \frac{(V_{inRMS} \sqrt{2}) - 1.65}{R_H + R_L} \times R_L \right] + 1.65 \quad \text{Where} \quad (5-8)$$

$V_{meas}$  = Measured voltage (V)  
 $V_{inRMS}$  = Supply / load voltage ( $V_{rms}$ )

With the measured voltage swing restriction of 1.525 V peak and the magnitude of the supply / load voltage that needs to be measured, values for the unknown parameters ( $R_H$  and  $R_L$ ) can be calculated from Equation (5-8). Changing these values slightly to obtain practical resistor values gives:  $R_H = 660 \text{ k}\Omega$ ;  $R_L = 2.7 \text{ k}\Omega$

Substituting these values back into Equation (5-8), lead to the following relationship between the supply / load voltage and the output of the measurement circuit.

$$V_{meas} = 4.074 \times 10^{-3} (V_{inRMS} \sqrt{2} - 1.65) + 1.65 \quad \text{With} \quad (5-9)$$

$$R_H = 660 \text{ k}\Omega$$

$$R_L = 2.7 \text{ k}\Omega$$

To obtain the DC offset error introduced through the addition of the 1.65 V reference, the equation above needs to be evaluated with an input voltage of 0 V. This gives an offset error of -6.722 mV on top of the required 1.65 V offset. To remove this offset error from the measurements the digital equivalent of this voltage must be added to the measurement in the DSP software.

The characteristics of the voltage measurement circuit are summarized in Table 5-2.

**Table 5-2: Voltage measurement summary**

<b>Circuit parameters</b>	$R_H: 660 \text{ k}\Omega$ $R_L: 2.7 \text{ k}\Omega$	
<b>Input range</b>	0 - 264.69 V <sub>rms</sub>	
<b>Output</b>	$V_{meas} = 4.074 \times 10^{-3} (V_{inRMS} \sqrt{2} - 1.65) + 1.65$	
With $V_{inRMS} = 0 \text{ V}$	1.643 V	
264.69 V <sub>rms</sub>	1.643 + 1.525 V	
-264.69 V <sub>rms</sub>	1.643 - 1.525 V	

### 5.3.5.C Current measurement

#### Requirement

The EVR is rated at 5 kVA with a 10 kVA extended overload rating. With a minimum input voltage of 207 V (230 V - 10 %) the current at 10 kVA is 48.4 A. To implement a protection coordination scheme with upstream circuit breakers, the EVR must be capable of measuring

substantially higher currents for short time periods. To fulfill this requirement the maximum supply current to be measured is increased to the maximum expected fault current of 500 A.

### Measurement circuitry

To measure the supply current a current transformer (CT) with a current transfer ratio of 500:1 is used. The output from the current sensor is then interfaced with the current measurement circuit shown in Figure 5-16.

The output current from the CT is terminated in a resistor ( $R_{burden}$ ) in the measurement circuitry to produce a voltage signal. To protect the operational amplifier against high voltages that could be generated across the resistor during excessive fault currents, back to back connected zener diodes are used to clamp the voltage. The voltage across the resistor is scaled and a 1.65 V offset added, before being sent to the ADC on the DSP.

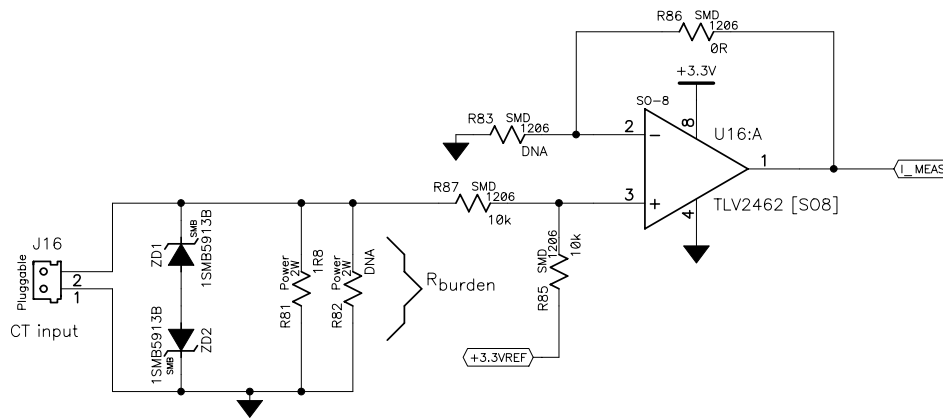


Figure 5-16: Current measurement circuit

Relating the supply current to the measurement output voltage for the circuit in Figure 5-16, leads to Equation (5-10):

$$I_{meas} = \frac{\left[ \frac{I_{SupRMS}}{CT_{ratio}} \sqrt{2} \times R_{burden} \right]}{2} + 1.65 \quad \text{Where} \quad (5-10)$$

$I_{meas}$  = Measured current (V)  
 $I_{SupRMS}$  = Supply current (A)  
 $CT_{ratio}$  = CT winding ratio  
 $R_{burden}$  = Terminating resistor  
 (Ω)

The rail-to-rail amplifier loading necessitates the restriction of the output voltage swing to 1.525 V<sub>peak</sub>. To calculate the value of the terminating resistor the first term of Equation (5-10) which is equal to the voltage swing can be used as shown in Equation (5-11).

---


$$I_{meas\_swing} = \frac{\left[ \frac{I_{SupRMS}}{CT_{ratio}} \sqrt{2} \times R_{burden} \right]}{2}$$

**With**

$$I_{meas\_swing} = 1.525 \text{ V}$$

$$I_{SupRMS} = 500 \text{ A}$$

$$CT_{ratio} = 500$$
(5-11)

$$\therefore R_{burden} = \frac{2I_{meas\_swing} CT_{ratio}}{I_{SupRMS} \sqrt{2}}$$

$$= 2.16 \Omega$$


---

Changing the calculated resistance value to obtain a practical resistor, gives  $R_{burden}$  equal to  $1.8 \Omega$ . By substituting this value back into Equation (5-10), the following relationship exists between the supply current and the measurement.

---


$$I_{meas} = 2.546 \times 10^{-3} I_{SupRMS} + 1.65$$

**With**

$$I_{SupRMS} = 500 \text{ A}$$

$$CT_{ratio} = 500$$

$$R_{burden} = 1.8 \Omega$$
(5-12)


---

The characteristics of the current measurement circuit are summarized in Table 5-3.

**Table 5-3: Current measurement summary**

<b>Circuit parameters</b>	$R_{burden}: 1.8 \Omega$	
<b>Input range</b>	$0 - 599 \text{ A}_{rms}$	
<b>Output</b>	$I_{meas} = 2.546 \times 10^{-3} I_{SupRMS} + 1.65$	
With $I_{SupRMS} = 0 \text{ A}$	$1.65 \text{ V}$	
$599 \text{ A}_{rms}$	$1.65 + 1.525 \text{ V}$	
$-599 \text{ A}_{rms}$	$1.65 - 1.525 \text{ V}$	

---

### 5.3.5.D Transformer temperature measurement

To enable the EVR to be operated at higher than nominal ratings for extended periods of time, the transformer winding temperature is monitored. This is accomplished by using a 5 k $\Omega$  negative temperature coefficient (NTC) thermistor. The resistance of the thermistor varies non-linearly with temperature as shown in Figure 5-17.

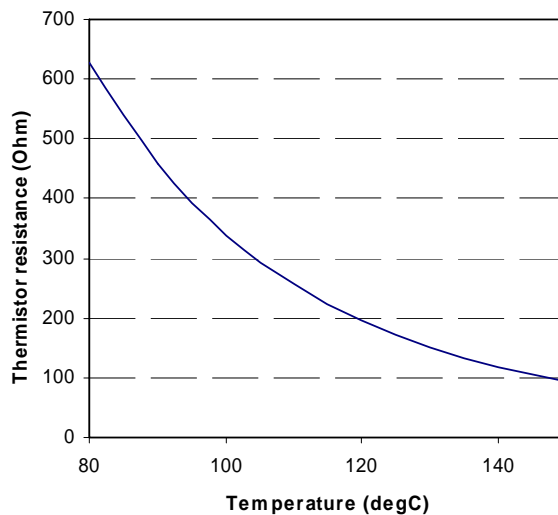


Figure 5-17: Thermistor resistance (80 – 150 °C)

A simple circuit to monitor the temperature is shown in Figure 5-18. The circuit applies a constant voltage to the series connection of  $R94$  and the thermistor and measures the voltage developed across the thermistor. This voltage is relayed to the AD converter for processing by the DSP. The 5 k $\Omega$  thermistor's voltage versus temperature characteristic, with the specific circuit values used, is shown beside the circuit diagram.



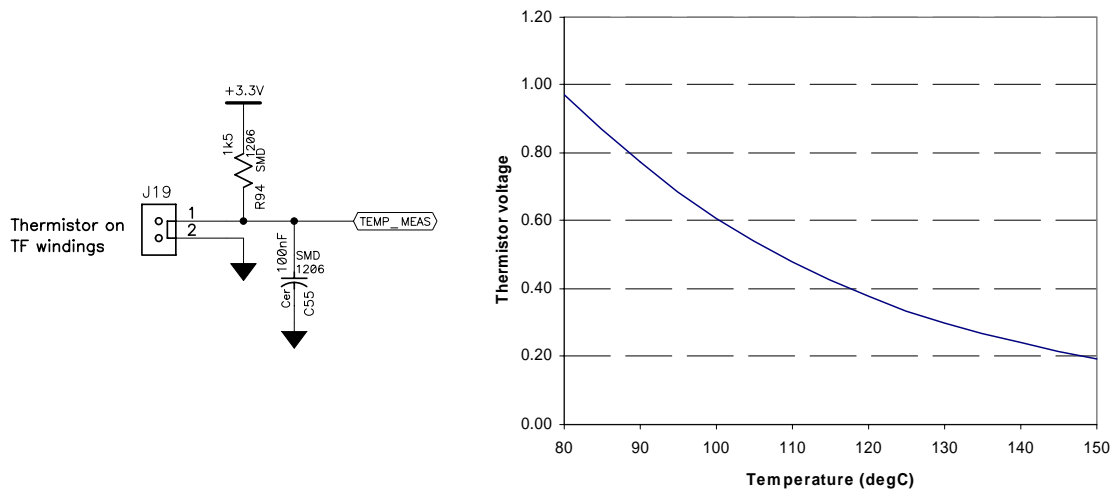


Figure 5-18: Transformer temperature measurement circuit & thermistor output

### 5.3.5.E Thyristor heat sink temperature measurement

A 10 kΩ NTC thermistor is mounted onto the thyristor heat sink to protect the thyristors against over temperature.

The circuitry used to interface with the sensor is identical to that of the transformer temperature sensor. The circuit is shown in Figure 5-19, together with the thermistor's voltage versus temperature characteristic with the specific circuit values used.

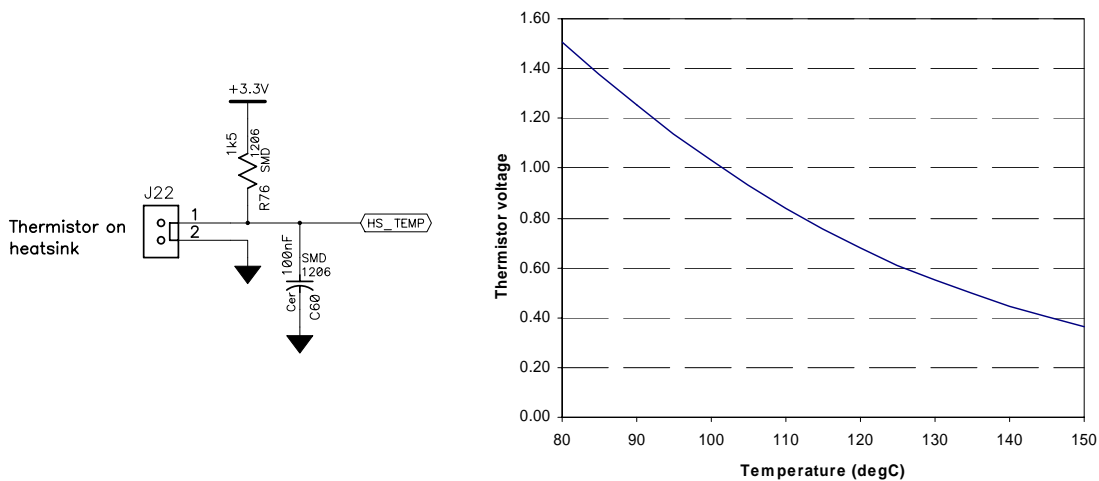


Figure 5-19: Heat sink temperature measurement circuitry & thermistor output

### 5.3.6 Thyristor drive

The thyristors are controlled using pulse transformers as shown in Figure 5-20. The pulse transformers provide the necessary electrical isolation and provide the gate power to turn the thyristors on.

To turn on a specific tap, a high frequency pulse-train signal with a specific duty cycle is applied to the gate of MOSFET *Q3*. This will cause the pulse transformer primary winding to be energized through current limiting resistors  $R_p$ . (A higher peak energizing current can be obtained at turn on by populating *R55* and *C24* if necessary.) The flux produced by the rising input current, will induce a voltage in both secondary windings, thereby driving the forward and reverse thyristor gate. Although both thyristor gates are driven, only the thyristor with a forward based anode-cathode will turn on.

To prevent saturation of the pulse transformer, the duty cycle must be chosen low enough to provide enough time for the pulse transformer to de-energize itself through diode *D7* and *ZD5*.

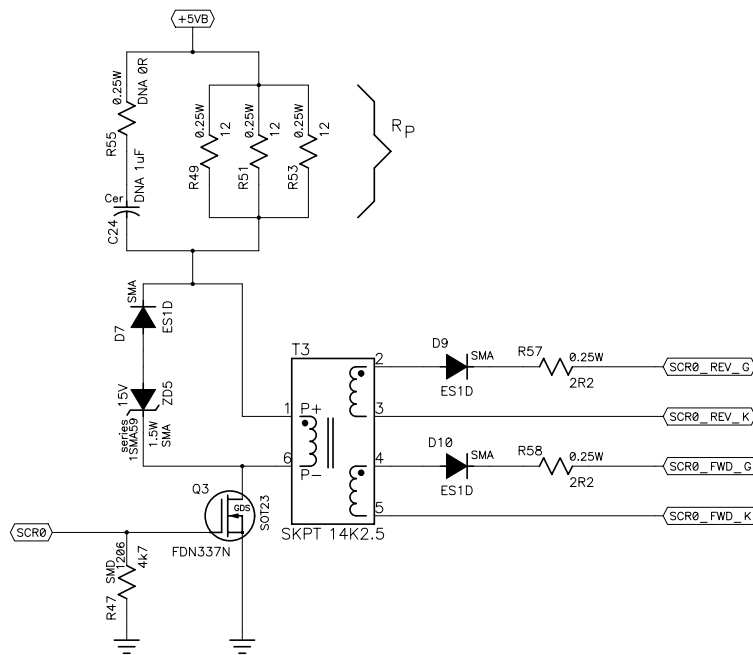


Figure 5-20: Thyristor drive circuit

The gate pulses supplied to the pulse transformers has a duty cycle of 30 % and frequency of 20 kHz. Both the frequency and duty cycle are entirely under software control. The driving circuitry is designed to supply 250 mA to the thyristor gate.

### 5.3.7 Power supply stabilizing

The EVR power supply supplies +5 V to the controller onto two separate pins, thus providing two supply rails. The one rail provides power to the DSP and related circuitry, while the other rail is dedicated for use by the pulse transformers.

The pulse transformers are operated with a high frequency pulse-train as described in section 5.3.6. This causes high frequency current pulses of 500 mA peak to be drawn, which introduce disturbances onto the +5 V supply.

To isolate these disturbances from the rest of the circuitry and minimize their influence a localized power supply is created for the pulse transformers. This power supply is obtained by “buffering” the pulse transformer supply (“+5VB”) from the incoming +5 V through series resistance and capacitor storage as shown in Figure 5-21.

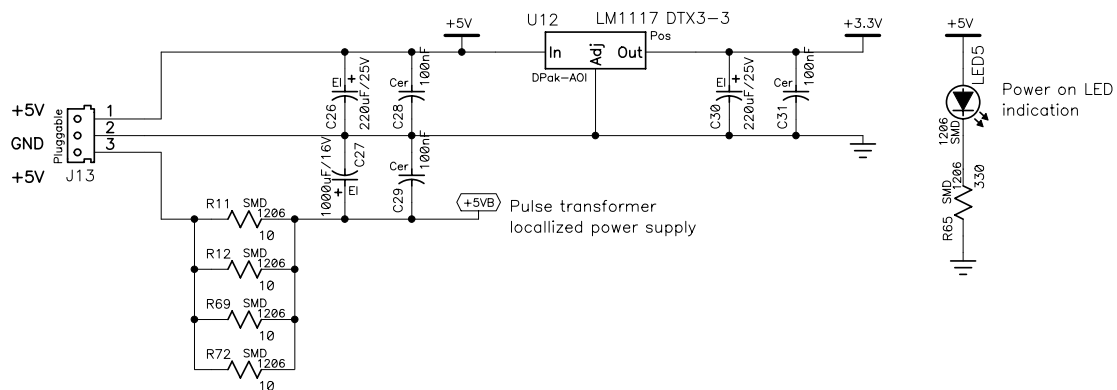


Figure 5-21: Power supply circuit

The DSP and most of the digital circuitry on the controller needs 3.3 V to operate. This voltage is obtained through the use of a linear voltage regulator connected to the +5 V supply.

### 5.3.8 DA converter

To simplify the debugging of code an external digital to analog (DA) converter was included in the design for code development purposes. (The DA converter and its associated amplifiers are only used during code development and testing and need not be populated in the final product.)

The DA converter, shown in Figure 5-22, consists of a quad 8-bit converter with a serial interface. This serial interface connects to the serial peripheral port (SPI) on the DSP, thereby enabling the DSP to write debugging values to a specific channel for monitoring purposes. Conversion speed is relatively slow, because the DA allows a maximum clock input of 1 MHz.

All the output channels are buffered and scaled to a maximum of 3.3 V using rail-to-rail amplifiers (not shown here).

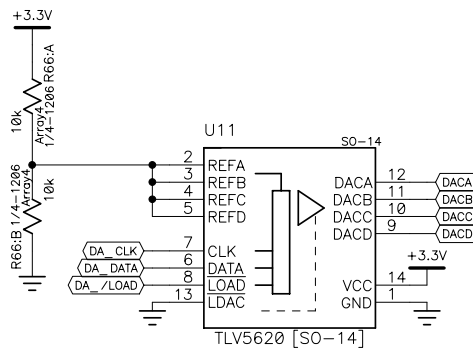


Figure 5-22: DA converter circuit

### 5.3.9 Display interface

Provision is made for the connection of external light emitting diode (LED) indicators to provide visual information on the EVR operating condition to the user. The information that can be displayed includes:

- Active tap setting
- 5x Status indicators

To keep the EVR operation simple and minimize confusion from the user’s perspective, only two indicators (“*Status\_LED5*” and “*Status\_LED1*”) are presently used. They function as the “OK” and “Fault” status indicators on the EVR. None of the tap settings are displayed.

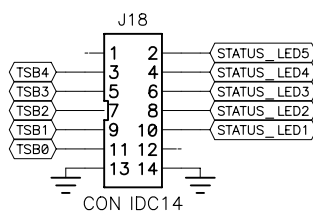


Figure 5-23: Display interface circuit

### 5.3.10 Power requirement

To design the power supply, the controller’s power requirements are needed. The power consumption of the controller is measured both in non-operational (thyristors are turned off) and operational mode as shown in Table 5-4. The total current consumed in operational mode at +5 V is 300 mA, resulting in a power requirement of 1.5 W.

**Table 5-4: Controller power requirement**

<b>Mode</b>	<b>Current @ 5V</b>		<b>Total</b>	
	<b>DSP circuitry</b>	<b>Thyristor drive</b>	<b>Current</b>	<b>Power</b>
Non-operational	130 mA	0 mA	130 mA	0.65 W
Operational	170 mA	130 mA	300 mA	1.5 W

---

## **Chapter 6**

Software development

---

## 6 Software development

The previous chapters have described the hardware and controller used in the EVR. In this chapter the development of the software code that controls the functionality and behaviour of the EVR is discussed. The software consists of a number of files, all linked together. A brief overview of the function of each file is given, before a detailed description of the parameters that can be used to fine tune the behaviour of the EVR is given. This is followed by flow diagrams, explaining the main program code.

### 6.1 Overview

The EVR software is written in c language and compiled using Texas Instruments code composer studio 3.1. The code follows a procedural or top down approach and consists of the following header and source files:

---

#### Header files

---

user_par.h	Contains user parameters to control the behaviour of EVR  Parameters are specified in “real world” quantities e.g. volts and ampere.
convert_par.h	Convert the parameters defined in user_par.h to their corresponding fixed point DSP representation where applicable.
main.h	Declares most of the variables and structures used in the code.
init.h	Declare functions present in init.c source file.
regs240x.h	Declare all register addresses for the TMS320LF2403 DSP processor.

---

---

#### Source files

---

init.c	Contain some initialization functions used to initialize the processor and peripherals.
TCVR_5Tap.c	Main program code

---

## 6.2 User parameters

The user parameters reside in the header file “user\_param.h” and contain user changeable parameters to fine tune the EVRs behaviour. The parameters can be grouped into the following sections which will be discussed below.

1. System settings
2. Thyristor settings
3. Tap threshold voltages
4. Line impedance
5. Valid supply voltage range
6. Valid load voltage range
7. Supply current range
8. Coordinated tripping
9. Cycle transition detection
10. Voltage averaging times
11. Tap change intervals
12. Tap failing
13. Auto restart time
14. Auto reset time
15. Successive error detection
16. Transformer temperature
17. Thyristor heat sink temperature
18. Error codes

### 6.2.1 System settings

These parameters specify the clock frequency of the DSP processor and the frequency of the main control loop.

---

<code>_clock</code>	DSP clock frequency	40 MHz
<code>_loopFreq</code>	Main control loop frequency	12.5 kHz

---

### 6.2.2 Thyristor settings

To drive the thyristor switches, consecutive pulses are applied to the gate. The frequency and duration of these pulses can be changed.



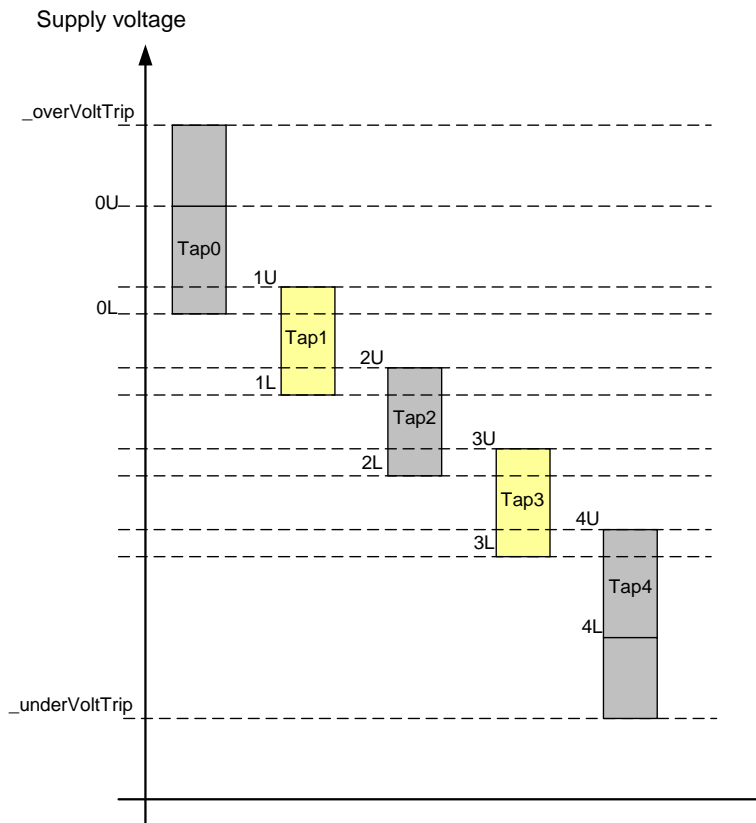
_fPulseTrain	Thyristor pulsetrain frequency	20 kHz
_duty	Thyristor pulse duty cycle	30 %

### 6.2.3 Tap threshold voltages

When the EVR turns on initially, it could either start with tap 0 activated (no voltage boosting) and then gradually switch through the taps until the required output voltage is obtained, or it can use the supply voltage measurement to select the correct tap at startup.

To select the correct startup tap, the following table is used.

_tap4L_rms	Tap4 lower voltage (set equal to under voltage trip level)	115 V
_tap4U_rms	Tap4 upper voltage	213 V
_tap3L_rms	Tap3 lower voltage	212 V
_tap3U_rms	Tap3 upper voltage	223 V
_tap2L_rms	Tap2 lower voltage	221 V
_tap2U_rms	Tap2 upper voltage	233 V
_tap1L_rms	Tap1 lower voltage	230 V
_tap1U_rms	Tap1 upper voltage	243 V
_tap0L_rms	Tap0 lower voltage	240 V
_tap0U_rms	Tap0 upper voltage (set equal to over voltage trip level)	265 V



### 6.2.4 Line impedance

The line impedance is used at startup to estimate the amount of voltage drop that will occur as soon as the EVR turns on (assume a load of 50% of EVR rating). This voltage drop is taken into account when the initial tap is selected.

---

<code>_lImpedanceP</code>	Line impedance percentage	5 %
---------------------------	---------------------------	-----

---

### 6.2.5 Valid supply voltage range

The EVR will only function if the supply voltage measurement is within a valid range, defined by the over voltage and under voltage trip levels. The measurement is not instantaneous, but a moving average of the supply voltage over a time period of 10.24 seconds (see section 6.2.10). If the supply voltage goes beyond these trip levels the EVR will turn off.

Depending on the EVR loading, the line voltage drop might cause the supply voltage to drop below the under voltage trip level at startup causing the EVR to trip repeatedly. To prevent this,

the supply voltage needs to exceed the under voltage trip level by a certain margin, before the system will turn on. This is specified by the under voltage boost constant.

---

<code>_overVoltTrip_rms</code>	Over voltage trip level	265 V
<code>_underVoltTrip_rms</code>	Under voltage trip level	115 V
<code>_underVoltBoost_rms</code>		10 V

---

### 6.2.6 Valid load voltage range

The EVR output voltage will be regulated to fall within the range set by the maximum and minimum static load voltage parameters. These “static” voltage limits are compared against a slow (long time span) moving average voltage measurement calculated over 5 seconds (see section 6.2.10). If the voltage measurement exceeds the max static voltage level, the EVR will change taps to reduce the output voltage. Similarly if the output falls below the minimum static voltage level, a tap adjustment will be made to increase the voltage.

To improve the response speed of the system against load over voltage, a maximum dynamic load voltage level is used. If the load voltage over a 20 ms period exceeds this level, a tap change will be made to prevent an over voltage condition at the load.

---

<code>_vLoadMaxStatic_rms</code>	Maximum load voltage (230 V + 10%)	253 V
<code>_vLoadMinStatic_rms</code>	Minimum load voltage (230 V + 4%)	239 V
<code>_vLoadMaxDynamic_rms</code>	Maximum load voltage over 20 ms period (230 V + 11.5%)	256 V

---

### 6.2.7 Supply current range

Although the EVR is rated for 25 A it can handle a substantial overload as can be seen from the coordinated tripping parameters (section 6.2.8). It can handle a sustained overload of 50 A for a

couple of hours depending on the transformer and heat sink temperature. Overloads larger than 50 A will cause the EVR to trip in 81.92 seconds.

The EVR only reverts to the rated supply current as a trip level if either the heat sink or transformer temperature sensor fails.

---

<code>_iNom_rms</code>	Rated EVR supply current	25 A
------------------------	--------------------------	------

---

### 6.2.8 Coordinated tripping

A short circuit will be recognized by the EVR as a 10 ms supply current magnitude in excess of 150 A. Current levels above 500 A will instantly trip the EVR.

---

<code>_iSCTrigLevel_rms</code>	Short circuit trigger level	150 A
	A supply current above this level causes the EVR to change state to short circuit mode.	
<code>_iTripHCycle_rms</code>	10 ms Trip level	500 A

---

The EVR should be capable of tripping a 50 A curve 1 circuit breaker only if it can do so safely, that is, without destroying itself. As the time period that the EVR can be kept on during a short circuit not only depends on the magnitude of the short circuit, but also the state of the thyristor heat sink temperature and steady state current magnitude before the short circuit occurred, a safe tripping curve needs to be calculated. This tripping curve is recalculated inside the EVR as conditions change.

**Step 1:** *Obtain thyristor tripping curve*

To obtain this curve, the maximum current / time characteristic was calculated for the SKKT162 thyristor module, with the ambient temperature equal to 20 °C. As the tripping curve is implemented digitally a limited number of points were evaluated. To speed up calculations in the fixed point DSP processor time intervals were chosen to be multiples of 2. The shortest time interval over which the current is evaluated is 80 ms, the next 160ms and so on up to 81.92 s.

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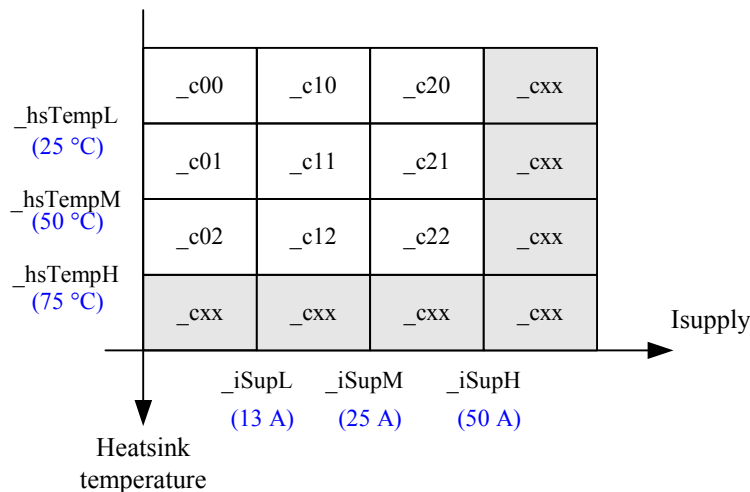
**Thyristor tripping curve**

<code>_iThyrisCurveP1</code>	Thyristor tripping curve: Point #0 - 0.08 sec	2200 A
...		
<code>_iThyrisCurveP9</code>	Thyristor tripping curve: Point #9 – 1.92 sec	690 A
...		
<code>_iThyrisCurveP18</code>	Thyristor tripping curve: Point #18 - 81.92 sec	50 A

---

***Step 2: Scale thyristor tripping curve***

Next the thyristor tripping curve needs to be adjusted to account for the actual heat sink temperature and steady state current. Due to possible calculation time constraints in the DSP, a table was constructed from which a scaling factor is chosen to apply to the thyristor curve depending on the system state.



For example, if the heat sink temperature is between 25 and 50 °C and the steady state supply current is smaller than 13 A, “`_c01`” will be the scaling percentage applied to the thyristor tripping curve.

If the supply current is higher than 50 A, or if the thyristor heat sink temperature is higher than 75 °C, a scaling factor capable of tripping a 20 A curve 2 circuit breaker is selected. This ensures that the EVR will at least be capable of tripping a customer breaker if it is too hot to trip the pole top box circuit breaker.

---

**Curve scaling percentage**

_c00_perc	Scaling percentage	87.39 %
_c01_perc	Scaling percentage	67.59 %
_c02_perc	Scaling percentage	45.99 %
...		
_c10_perc	Scaling percentage	86.08 %
_c11_perc	Scaling percentage	66.01 %
_c12_perc	Scaling percentage	41.07 %
_c20_perc	Scaling percentage	83.78 %
_c21_perc	Scaling percentage	64.03 %
_c22_perc	Scaling percentage	39.58 %
_cxx_perc	Scaling percentage outside table	25 %

---

***Step 3: Obtain circuit breaker tripping curve***

The EVR is fitted with a 100 A curve 1 circuit breaker. This circuit breaker was used as its minimum tripping characteristic is just larger than the maximum tripping characteristic of a 50 A curve 1 circuit breaker. This guarantees that the EVRs circuit breaker will never trip before the pole top box circuit breaker.

The characteristic of the circuit breaker was obtained over the same time intervals as that of the thyristor tripping curve. An additional safety factor was also added, scaling the circuit breaker tripping curve by 95 %.

---

### **100A Circuit breaker tripping curve**

<code>_i100CurveP1</code>	Circuit breaker tripping curve: Point #0 - 0.08 sec	1000 A
...		
<code>_i100CurveP9</code>	Circuit breaker tripping curve: Point #9 – 1.92 sec	500 A
...		
<code>_i100CurveP18</code>	Circuit breaker tripping curve: Point #18 – 81.92 sec	130 A
<code>_i100Scale</code>	Circuit breaker tripping curve scaling factor	95 %

---

#### ***Step 4: Impose constraints on scaled thyristor tripping curve***

To obtain the final thyristor tripping curve, the following must be combined:

- Scaled thyristor tripping curve
- Circuit breaker tripping curve
  - The thyristor cannot be kept on longer than the time allowed by the circuit breaker tripping curve; otherwise the EVR will turn itself off.
- Maximum fault level
  - A maximum fault level of 500 A is anticipated. Therefore the EVR tripping curve will be limited at 500 A.

---

### **Tripping curve limits**

<code>_iTripCurveMax_rms</code>	Maximum fault current that the EVR can handle	500 A
<code>_iTripCurveMin_rms</code>	Steady state overload level	50 A

---

## **6.2.9 Cycle transition detection**

The EVR code relies on detecting the supply voltage cycle transition for various purposes. This is done by sampling the voltage and checking if it is positive or negative. To provide some noise immunity the average over a number of samples is used in detecting the cycle transition. (Samples are taken every 80  $\mu$ s.)

---

_filtSize	Number of samples over which the supply voltage is filtered.	4
-----------	--	---

---

### 6.2.10 Voltage averaging times

On startup, the EVR will monitor the supply voltage over a number of half cycles. The EVR will not turn on until the supply voltage stays within the valid range (see section 6.2.5) for 1000 consecutive half cycle periods.

Both the supply and load voltage measurements are averaged over a short and longer period. The short or fast average is calculated as the average over a specified number of half cycles. The longer average is a moving average calculated from a specified number of fast averages.

The supply moving average is used to detect over and under voltage conditions on the supply, while the load fast and moving average is used to determine whether tap changes are needed.

---

#### **Supply voltage**

_vSupValidPer	Number of half cycles during which supply voltage must stay valid, before system will turn on	1000 (10 sec)
_vSupFAvgSize	Number of half cycles in fast average	32 (320 ms)
_vSupMAvgSize	Number of fast averages used to calculate moving average	32 (10.24 sec)

#### **Load voltage**

_vLoadFAvgSize	Number of half cycles in fast average	25 (250 ms)
_vLoadMAvgSize	Number of fast averages used to calculate moving average	20 (5 sec)

---



## 6.2.11 Tap change intervals

To minimize the number of tap changes, tap changes are only allowed at certain time periods, or under certain conditions.

On startup, an initial tap will be selected according to the supply voltage. Thereafter enough time needs to pass for the load voltage to be averaged, before the first tap change can be made. Tap changes will now be allowed according to the normal tap change period parameter. If an over voltage condition arises at the load, the time between tap changes will be shortened to quickly reduce the load voltage.

---

__tapChangePerNormal	Normal number of half cycles between tap changes	$\_vLoadFAvgSize + 1$ (26)
__tapChangePerOvervolt	Number of half cycles between tap changes during a load dynamic overvoltage condition	2
__tapChangePerStartup	Number of half cycles from startup to first tap change	$\_vLoadFAvgSize * 2$ (50)
__tapChangePerTapFail	Number of half cycles between successive retries of a specific tap, if systems detects that the tap failed to turn on	5

---

## 6.2.12 Tap failing

If the EVR turns on a specific tap, and no output voltage is measured a possible tap failure event is registered. To verify that the tap did indeed fail, a number of retries are allowed.

Once a possible tap failure is recognized, the corresponding thyristor's control signal will be removed and reapplied after 5 half cycles (see section 6.2.10) has passed. This process will be repeated 8 times or until an output voltage is measured. If no output voltage is measured after the last retry the tap will be flagged as failed. This will prevent any further use of this tap and any tap tap lower than it for the next 20 hours (see section 6.2.13).

---

__tapFailNumRetries	Number of times system will try to activate a specific tap before flagging it as failed	8
__tapFailWindowSize	Window period (in half cycles) for detection of tap failure	$(\_tapFailNumRetries + 2) \times \_tapChangePerTapFail$ (50)

---

### 6.2.13 Auto restart times

Following an error event, the EVR will restart itself after a certain time period associated with the specific error event has passed. The restart times could also be extended if too many errors occur within a certain time period (see section 6.2.15).

---

_tRestartOverCur	Restart time for overload event	30 sec
_tRestartOverCurInst	Restart time for excessive short circuit > 500 A over 10 ms period	30 sec
_tRestartCoordinationFail	Restart time after coordination failure trip.	180 sec
_tRestartRepShortCircuit	Restart time after successive short circuits	60 sec
_tRestartOverTemp	Over temperature restart time	600 sec
_tRestartOverVolt	Over voltage restart time	15 sec
_tRestartTap0Fail	Nominal tap failure restart time	1200 sec
_tRestartTapShorted	Tap shorted restart time	120 sec

---

A tap flagged as failed will be allowed to be reused after a 20 hour time interval has expired.

---

_tRestartTapFail	Clear tap fail flag	20 hours
------------------	---------------------	----------

---

### 6.2.14 Auto reset time

To minimize possible inconvenience to the customer due to software bugs, the EVR has the ability to reset itself after a certain time period if it encounters an unexpected condition.

---

<code>_tResetNoOutputNoErr</code>	Resets EVR if there is no error condition present, and no output voltage is measured.	300 sec
<code>_tResetNoOutput</code>	Resets the EVR if no output voltage is measured for longer than the indicated time.	1800 sec

---

### 6.2.15 Successive error detection

The restart times following an error event is made as short as possible to minimize inconvenience to the customer. Should errors occur repetitively, the short restart times will lead to stress in the system components. To prevent this restart times are extended by a certain factor if repetitive errors occur.

---

<code>_maxNumErrors</code>	Maximum number of errors that can occur over the window period	3
<code>_repErrWindow</code>	Window period for detecting repetitive errors	123 sec
<code>_restartExtendFactor</code>	Restart time multiplication factor	4
<code>_tmaxRestartExtendApply</code>	Restart extension will only be applied to restart times smaller than this value	120 sec

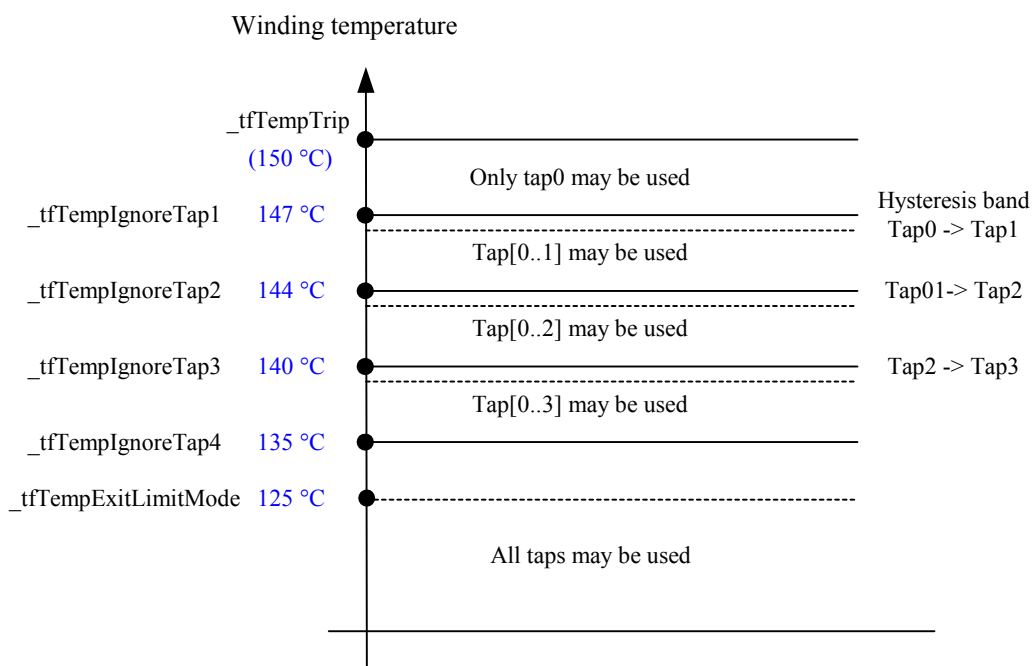
---

### 6.2.16 Transformer temperature

To protect the transformer the internal winding temperature is measured. If the winding temperature is too high, the EVR will go into temperature limiting mode. In this mode the EVR will try to lower the losses in the transformer by switching to a higher tap setting.

The winding temperatures above which a particular tap setting will not be allowed is given below.

_tfTempTrip_degC	Temperature trip level	150 °C
_tfTempIgnoreT1_degC	Only tap 0 may be used	147 °C
_tfTempIgnoreT2_degC	Only tap 0 and 1 may be used	144 °C
_tfTempIgnoreT3_degC	Only tap 0, 1 and 2 may be used	140 °C
_tfTempIgnoreT4_degC	Only tap 0, 1,2 and 3 may be used	135 °C
_tfTempExitLimitMode_degC	If temperature falls below this level, temperature limit mode can be exited and all taps used	125 °C
_tfTempHystBand	Hysteresis band percentage	75 %



## 6.2.17 Thyristor heat sink temperature

The thyristor heat sink trip parameter protects the thyristor modules against over temperature.

_hsTempTrip_degC	Temperature above which EVR will trip	97 °C
------------------	---------------------------------------	-------

## 6.2.18 Error codes

To enable the operator to identify on which fault the EVR tripped, the fault LED will repeatedly flash a specific error code. By counting the number of flashes in this error code, the fault can be identified.

Both high priority error codes and low priority error codes are displayed on the fault LED. Low priority errors indicate that there is a problem with the EVR, but the severity of error is not high enough to warrant the EVR to turn off - the EVR can continue to operate although at some reduced power / functionality level. High priority errors necessitates that the EVR be turned off, to prevent damage to the EVR or the customer.

Since only one error indicator is used on the EVR, a high priority error will override a low priority error that is being displayed on the fault LED.

---

**High priority errors**

_errCode_coordinationFail	Coordinated tripping was not possible	1
_errCode_overCur	Overloading occurred	2
_errCode_overCurInst	Supply current in excess of 500 A over ar 10 ms period	3
_errCode_underVolt	Supply under voltage	4
_errCode_overVolt	Supply over voltage	5
_errCode_hsTemp	Thyristor heat sink over temperature	7
_errCode_tfTemp	Transformer winding over temperature	8
_errCode_repShortCircuit	Short circuits occurred less than 20 seconds after previous short circuit was cleared	9
_errCode_tap0Failed	Nominal tap failed to turn on	10
_errCode_tapShorted	A tap switch is shorted – on when it should be off	11

**Low priority errors**

_errCodeLP_hsSensor	Heat sink temperature sensor failed	12
_errCodeLP_tfSensor	Transformer winding temperature sensor failed	13
_errCodeLP_tapFailed	A tap, other than tap 0, failed to turn on	14

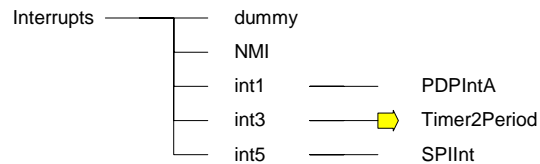
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### 6.3 Software flowchart

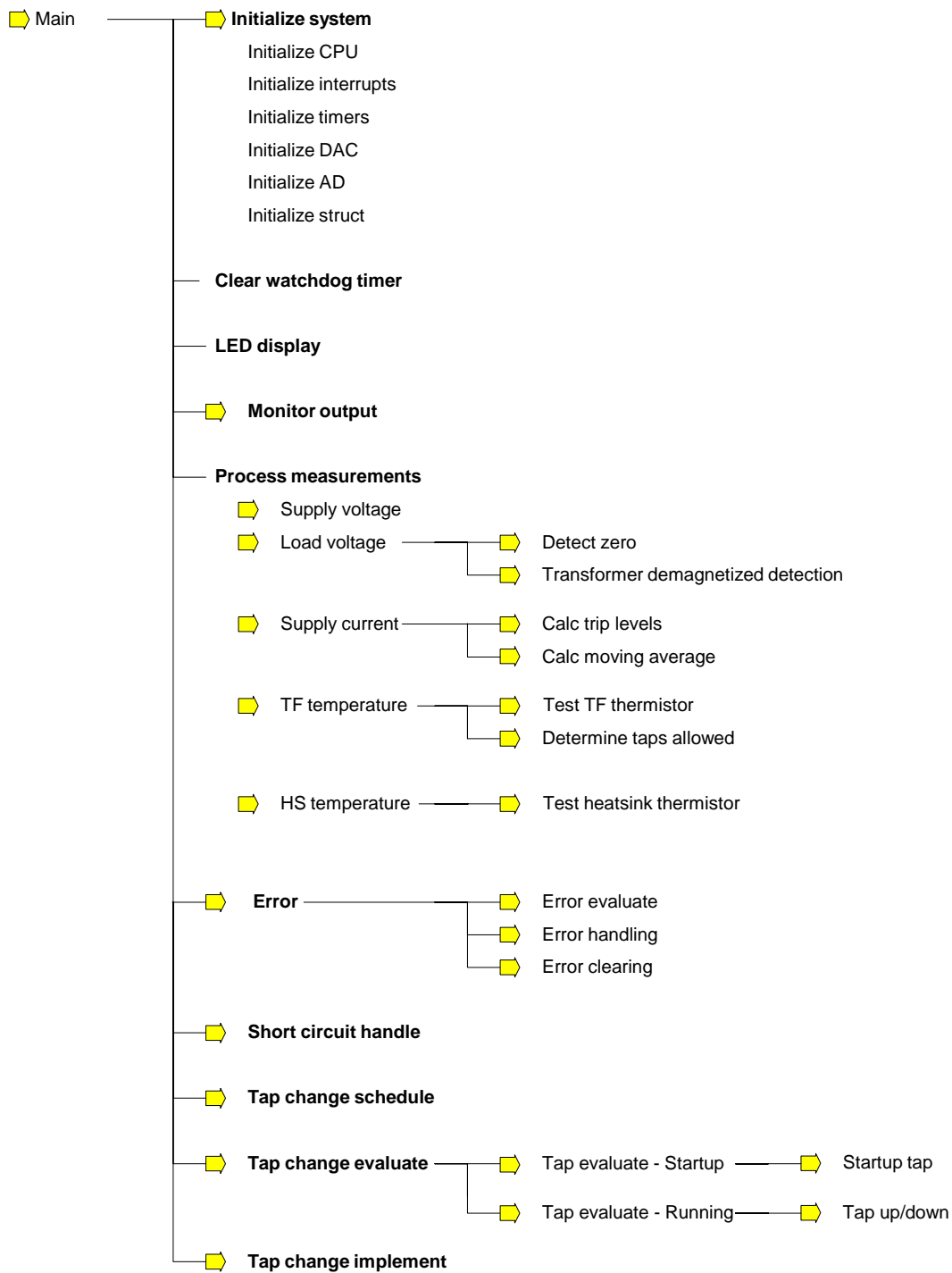
The system operation is controlled by the main procedure, assisted by a number of the sub procedures called from the main procedure.

A few interrupts runs in parallel with the main program, performing the necessary real time timing and synchronizing through updating of various counters.

A tree view outlining the different procedures in the software is shown in Figure 6-1 and Figure 6-2 for the interrupt and main procedures respectively. Each procedure marked with a “⇔” has a flowchart associated with it which will be discussed in the following sections.



**Figure 6-1: Flowchart - Interrupts procedure tree view**



**Figure 6-2: Flowchart - “Main” procedure tree view**

Note: Not all the procedures showed here exits explicitly in the DSP code. As some DSP procedures translated to multiple page flowchart diagrams, they were broken down into smaller logical units, to simplify flowchart reading.



### 6.3.1 Timer2Period

---

Interrupts    ⇒    Int3    ⇒    Timer2Period    ⇒

---

This interrupt service routine is called when timer2 period expires, which occurs every 80 us. The routine updates various counters to enable the main and sub procedures to synchronize their activities in real time.

At the start of the routine, the “timeSliceExp” flag set. This is used to signal to the main procedure that the main control loop can re-execute. The “tSlice” counter counts the number of 80 us intervals that have expired, to enable the system to detect 10 ms and 20 ms time intervals.

The 10 ms interval is used to set flags linked to various procedures. These flags enable the procedures to perform certain operations once the 10 ms period has expired.

The 20 ms interval is used to enable the flashing of the error LED at the required frequency and updating of the automatic restart and time between error counter.

At the end of the routine the analog to digital converter is restarted to obtain the new measurement samples. The digital to analog conversion sequence is also started, to enable code debugging values to be monitored.

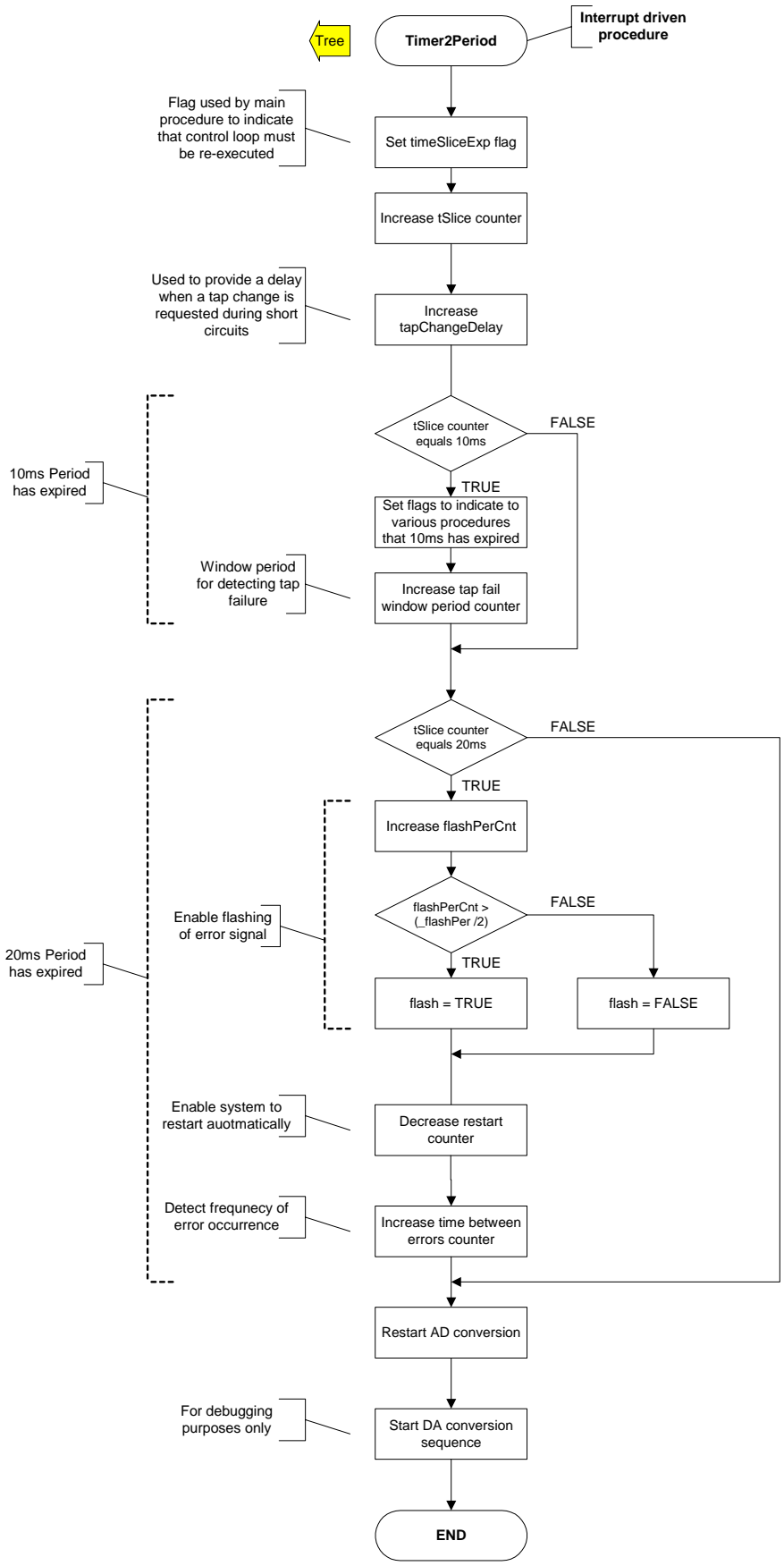


Figure 6-3: "Timer2Period" procedure

### 6.3.2 Main

---

Main      ⇨                      ⇨                      ⇨

---

When the EVR is turned on, the DSP initializes itself, setting up all the peripherals and initializing all the structures. The system then enters the main control loop, which will be executed repeatedly every 80  $\mu$ s.

At the start of the main control loop the system watchdog will be cleared and the current system status will be displayed on the LED display. The measurements obtained in the previous 80  $\mu$ s interval are then processed and average values calculated. The processed measurement values are then compared against pre-set threshold values to detect if any errors have occurred.

If the system is not in an error state, the controller will check whether it is allowed to evaluate the system for a possible tap change. (The time period allowed between successive tap changes are scheduled to reduce voltage flicker at the customer due to frequent tap changes.) The system taps will then be evaluated and a new tap setting obtained and activated if necessary.

Finally new measurement samples will be obtained after which the controller will wait for the start of the next control loop.

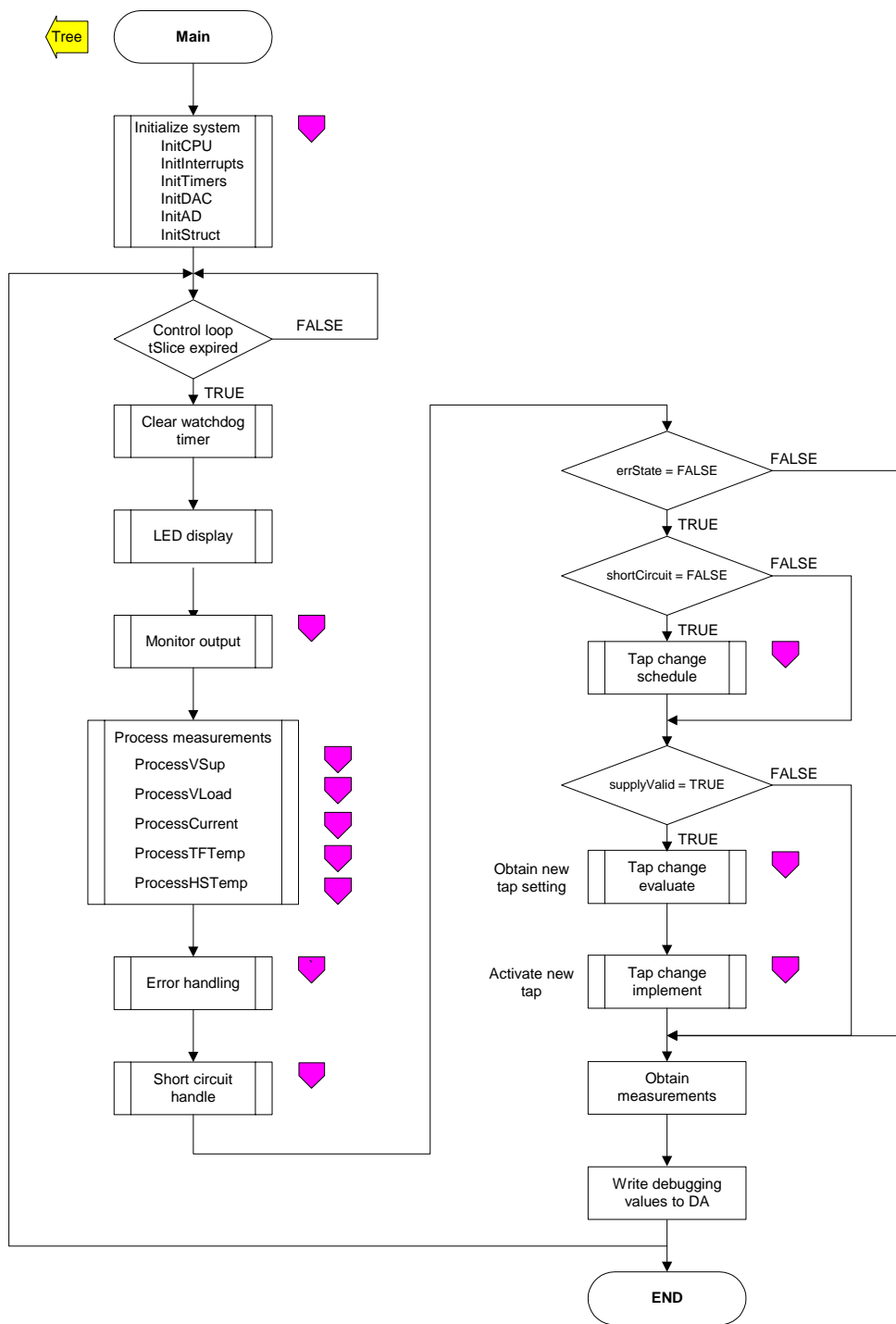


Figure 6-4: “Main” procedure

### 6.3.2.A Initialize system

These procedures initialize the DSP processor, configure the DSP peripherals and initialize the structures and variables used in the code.

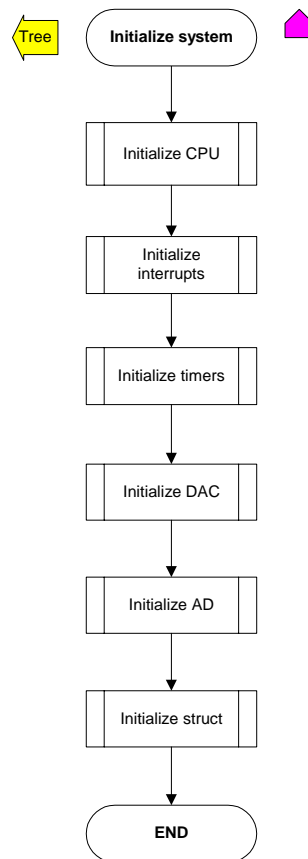


Figure 6-5: "Initialize system" procedures

### 6.3.2.B Monitor output

Main ⇒ Monitor output ⇒

This procedure is included to minimize possible customer inconvenience should an unknown bug exists in the code. It causes the system to reset the processor if the output voltage remains low for a preset time period.

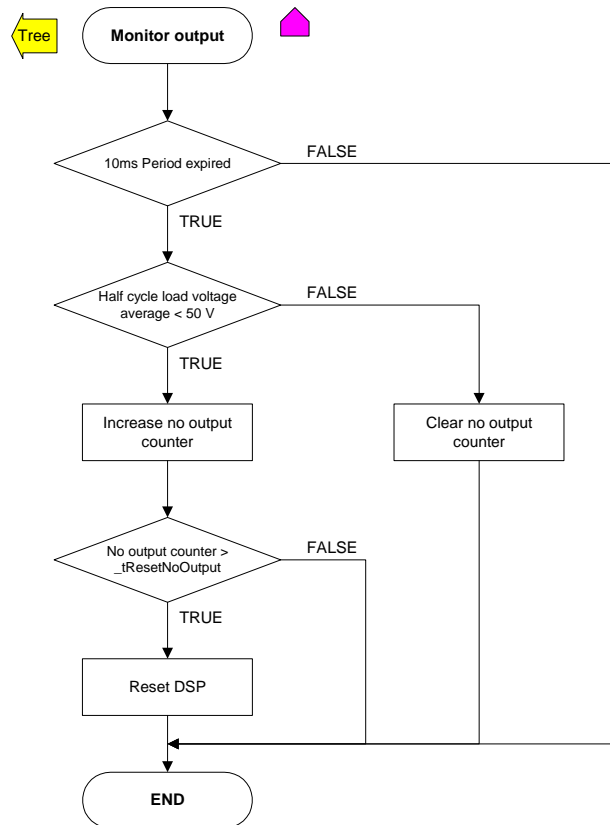


Figure 6-6: "Monitor output" procedure



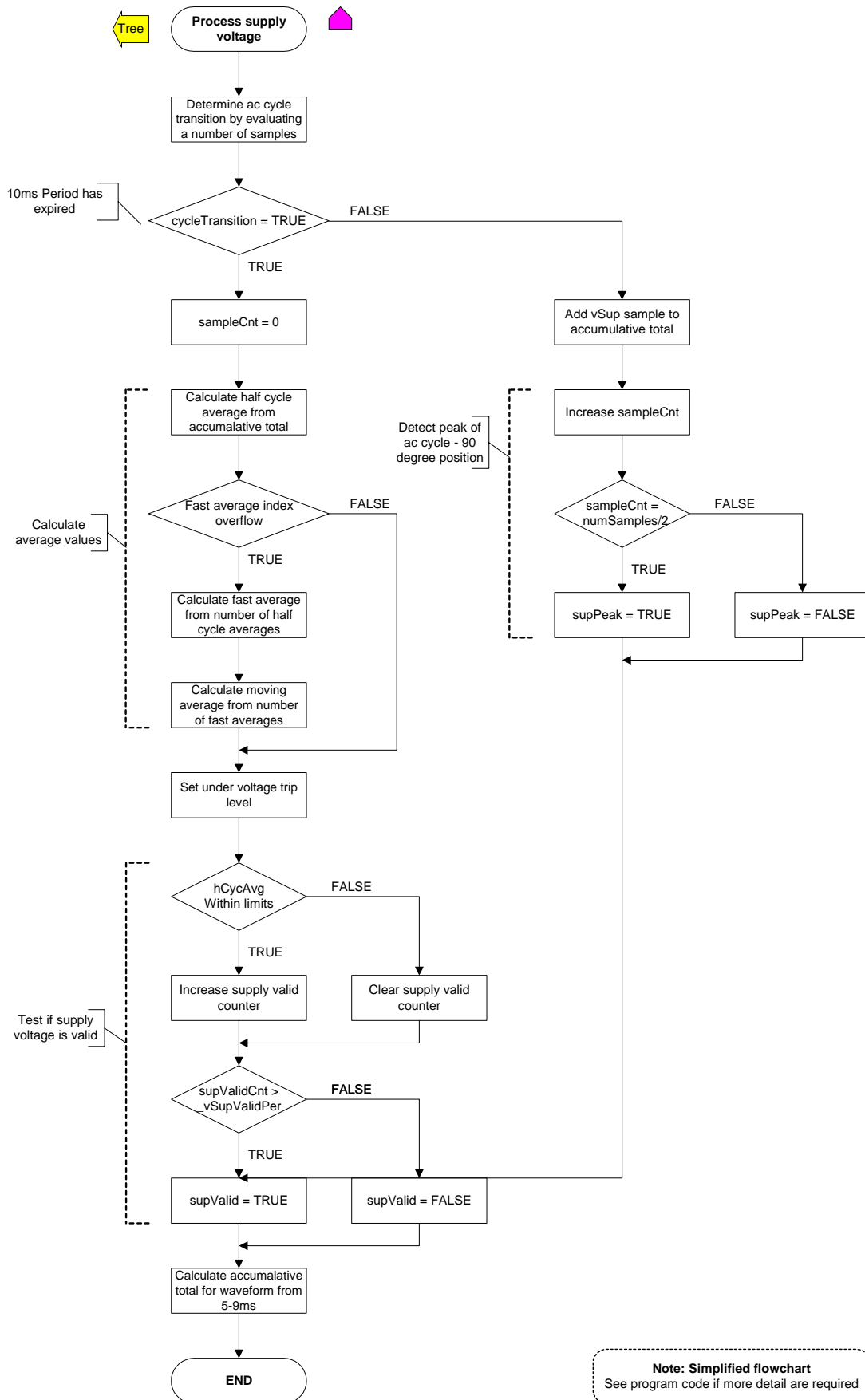


Figure 6-7: “Process supply voltage” procedure





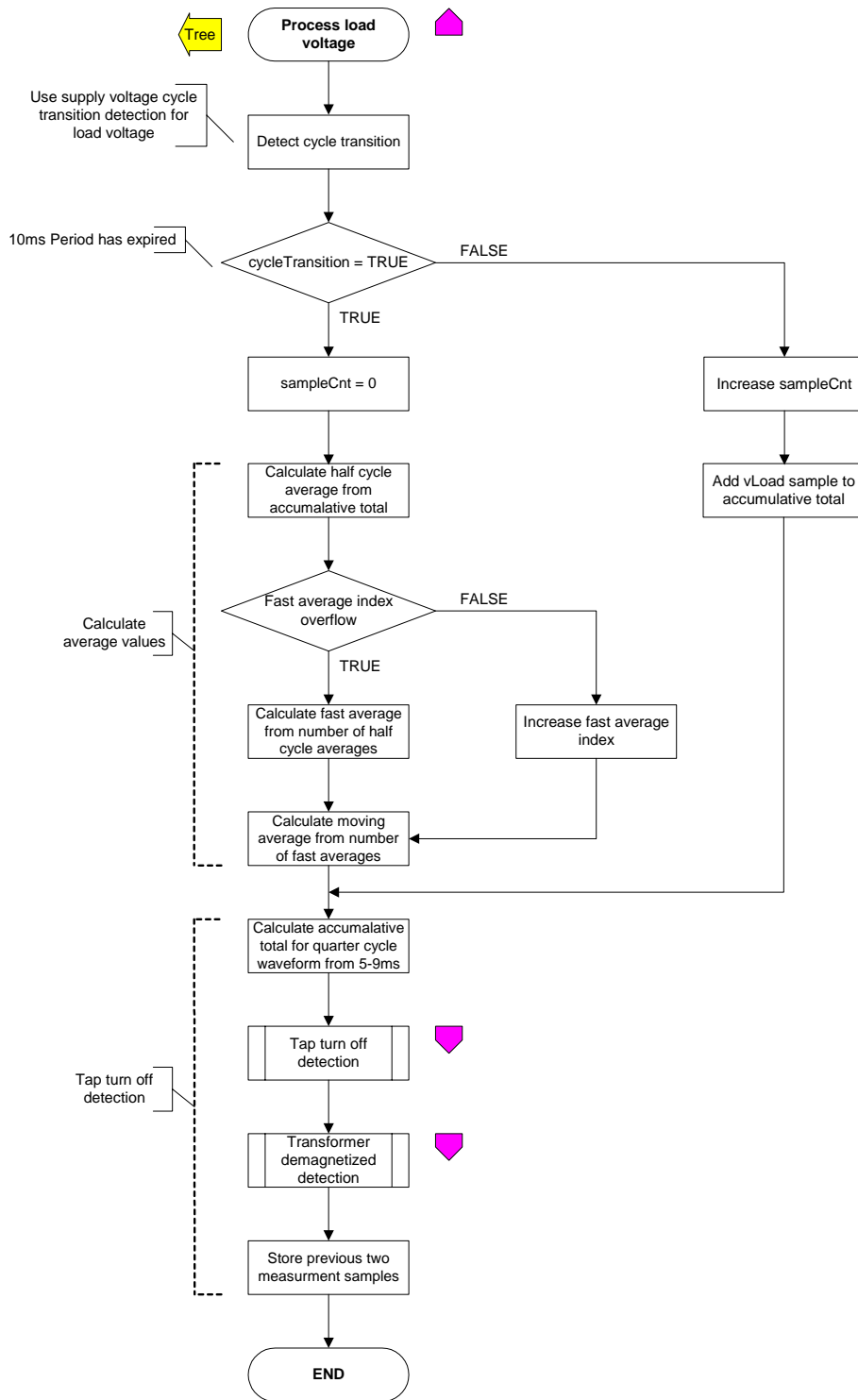


Figure 6-8: "Process load voltage" procedure

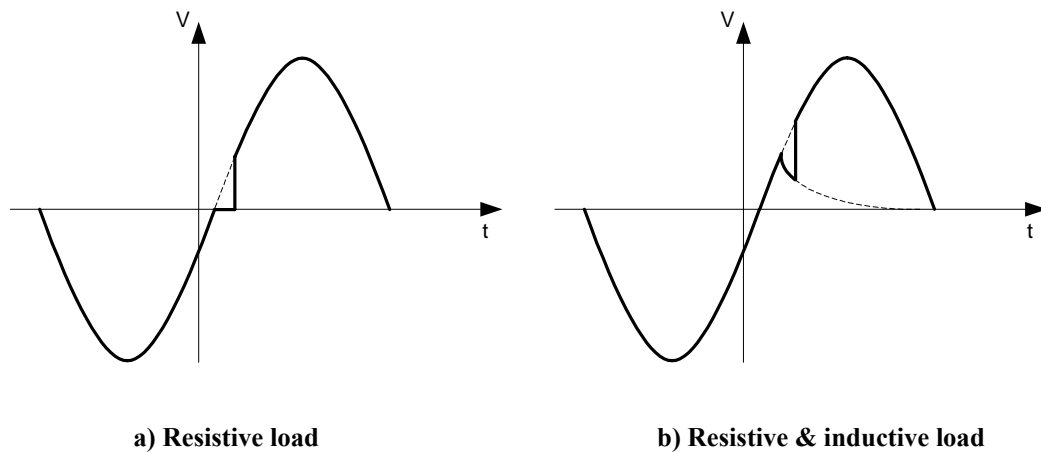
### 6.3.2.D.i *Detect tap turn off*

---

Main       $\Rightarrow$       Process load       $\Rightarrow$       Detect tap turn off       $\Rightarrow$   
voltage

---

To detect when a tap turns off or commutates, the load voltage samples are inspected to recognize a specific pattern. This pattern depends on the load power factor as can be seen in Figure 6-9.



**Figure 6-9: Load voltage during tap turn off**

For a purely resistive load the voltage and supply current are in phase. Tap commutation would therefore take place at the voltage zero crossing. To detect this, the load voltage is inspected for the existence of a constant low level, present for a certain time period.

For a combination of resistive and inductive load the supply current will lag the voltage. Tap commutation would therefore take place with the voltage at some point on the rising slope of the sine wave. Once the tap commutates, the load voltage will start to decrease. Detecting this decreasing voltage on the normally rising voltage slope indicates that the tap has commutated.

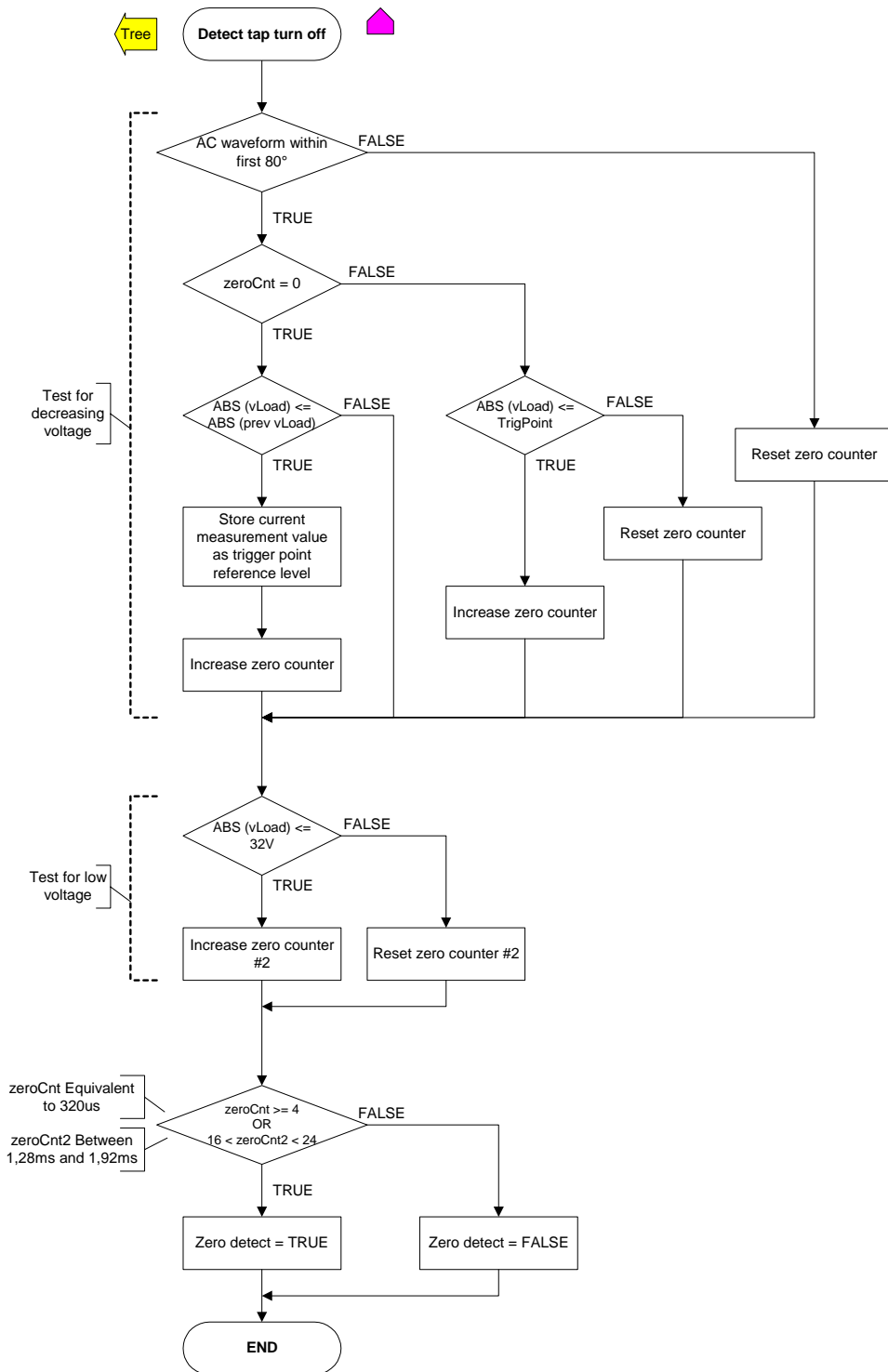
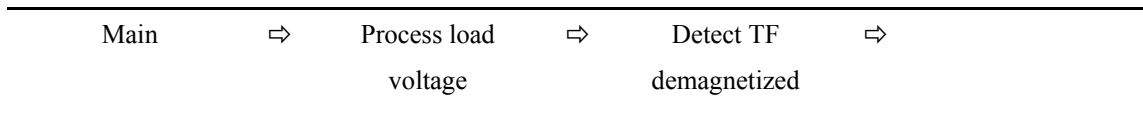


Figure 6-10: "Detect tap turn off" procedure

### 6.3.2.D.ii *Detect TF demagnetized*



If the transformer is demagnetized, the supply needs to be turned on at the peak of the AC waveform to avoid huge inrush currents into the transformer.

To detect if the transformer is demagnetized the load voltage is monitored over a 3 ms period. If the load voltage stays low during this period, the transformer is assumed to be demagnetized.

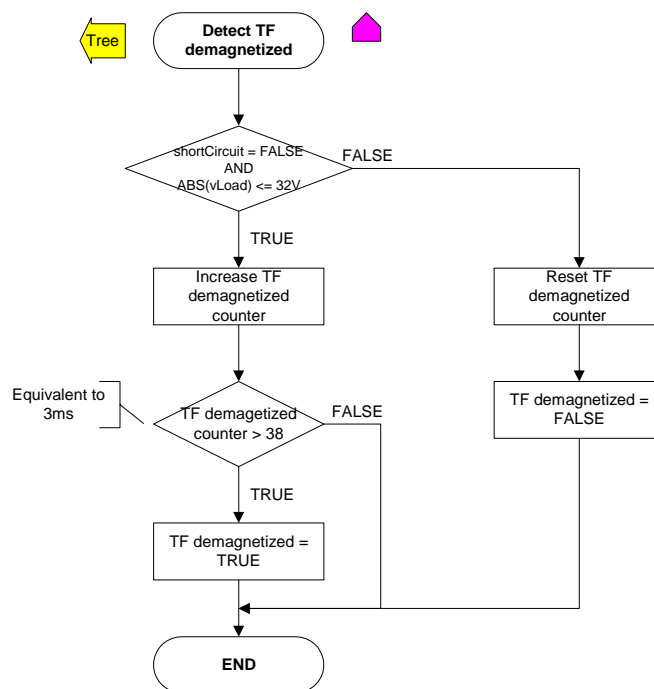


Figure 6-11: "Detect TF demagnetized" procedure

### 6.3.2.E Process supply current

---

Main ⇒ Process supply ⇒  
current

---

To protect the system against self destruction and to implement a synchronized tripping curve a tripping curve and the average current at each point on the tripping curve is required. To obtain this, the following functions are performed by the procedure:

- Calculates the average supply current over:
  - 32 samples / 2.56 ms  
Moving average for detecting tap turn off during short circuit conditions.
  - 10 ms / Half cycle average  
(This average is not synchronized with the AC waveform zero crossing)
  - 80 ms / Fast moving average - Based on a number of half cycle averages.
  - tripping curve points / Tripping curve moving averages - Based on a number of 80 ms moving averages.
- Calculates a safe tripping curve for the thyristor taking into account the current heat sink temperature and load.
- Calculates the moving average at each point on the tripping curve.
- Test for over current at each point on tripping curve.

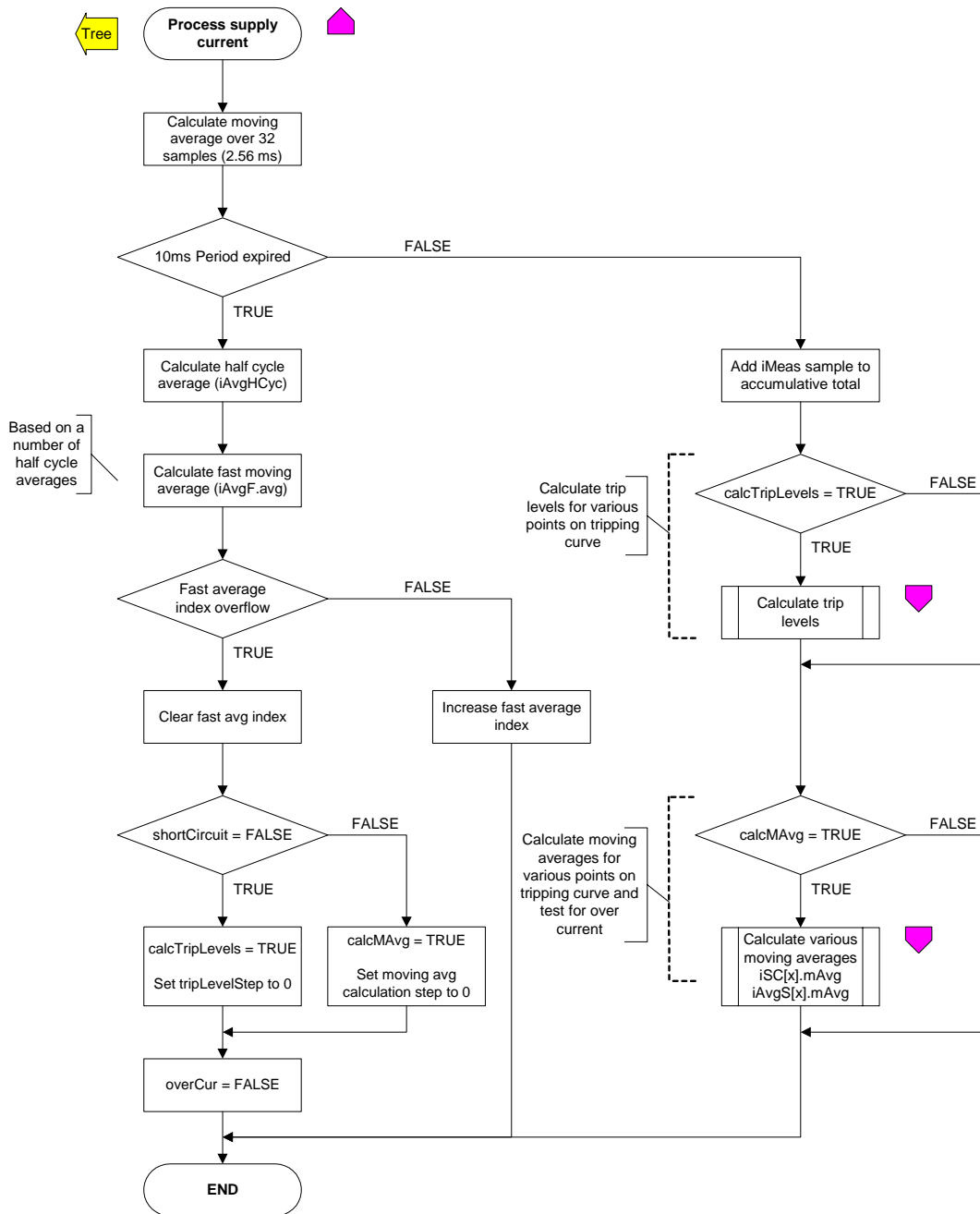
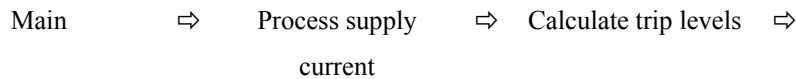


Figure 6-12: "Process supply current" procedure

### 6.3.2.E.i *Calculate trip levels*



This code will be executed once the “calcTripLevels” flag has been set, which occurs as soon as the latest 80 ms moving average has been calculated. As there are 20 trip level points to be calculated they are calculated in successive 80 μs time slices rather than in a single time slice, thereby reducing the burden on a single 80 μs interval.

The first step is to obtain the curve scaling factor. Then in the following 80 μs time slices the thyristor tripping curve is scaled at each point by this scaling factor and restrictions/limits applied to the point.

When the new tripping curve has been calculated, the “calcMAvg” flag is set to enable the calculation of the moving average current at each point of the tripping curve.



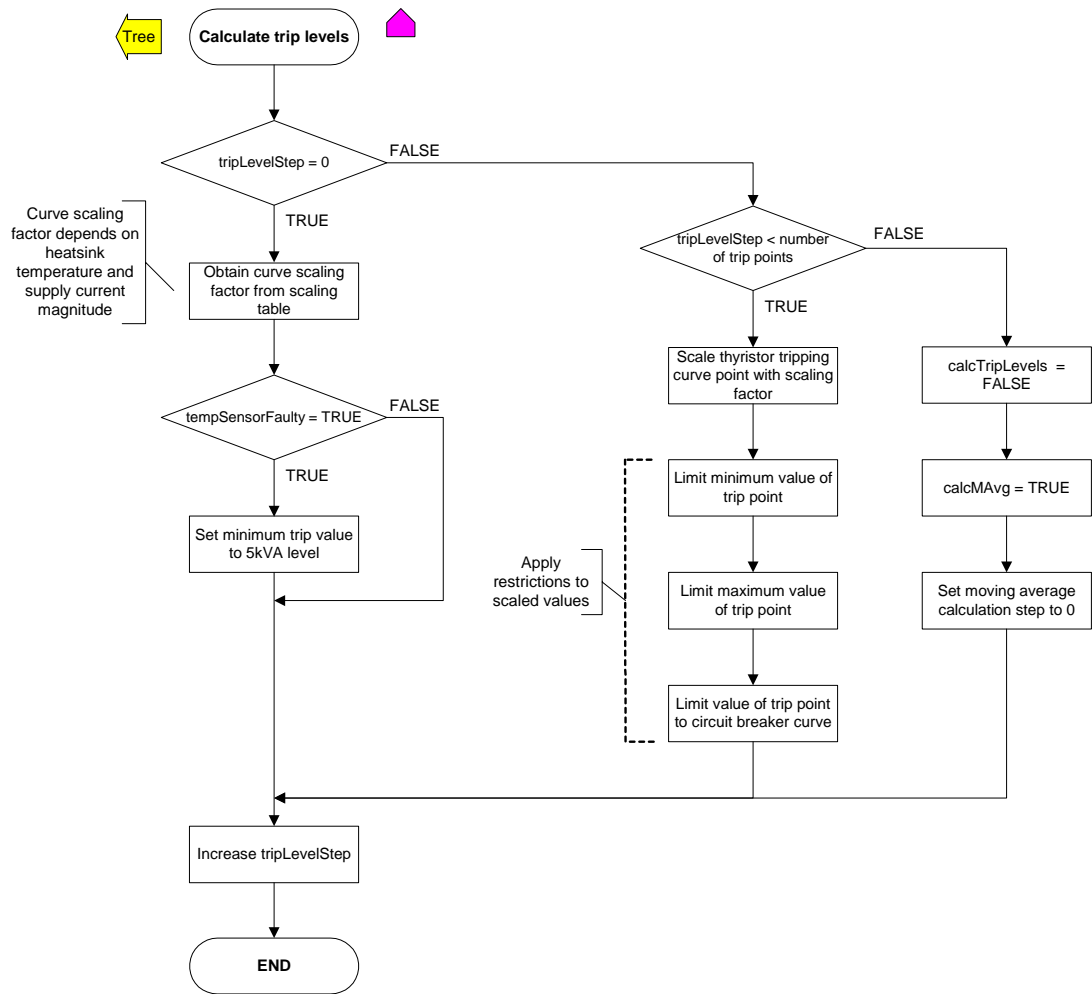
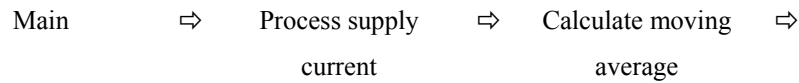


Figure 6-13: "Calculate trip levels" procedure

### 6.3.2.E.ii *Calculate moving averages*



This code calculates the moving averages at the various points on the thyristor tripping curve and test each point for an over current error. It will be executed once the “calcMAvg” flag has been set. As there are 20 moving averages to be calculated they are calculated in successive 80  $\mu$ s time slices rather than in a single time slice, thereby reducing the burden on a single 80  $\mu$ s interval.

The moving averages are calculated from a circular array storing 80 ms averages. By combining a different number of values from this array, the moving averages for the various time intervals corresponding to the tripping curve points are calculated. Once each moving average is calculated, it is compared to the tripping curve to test for an over current condition.

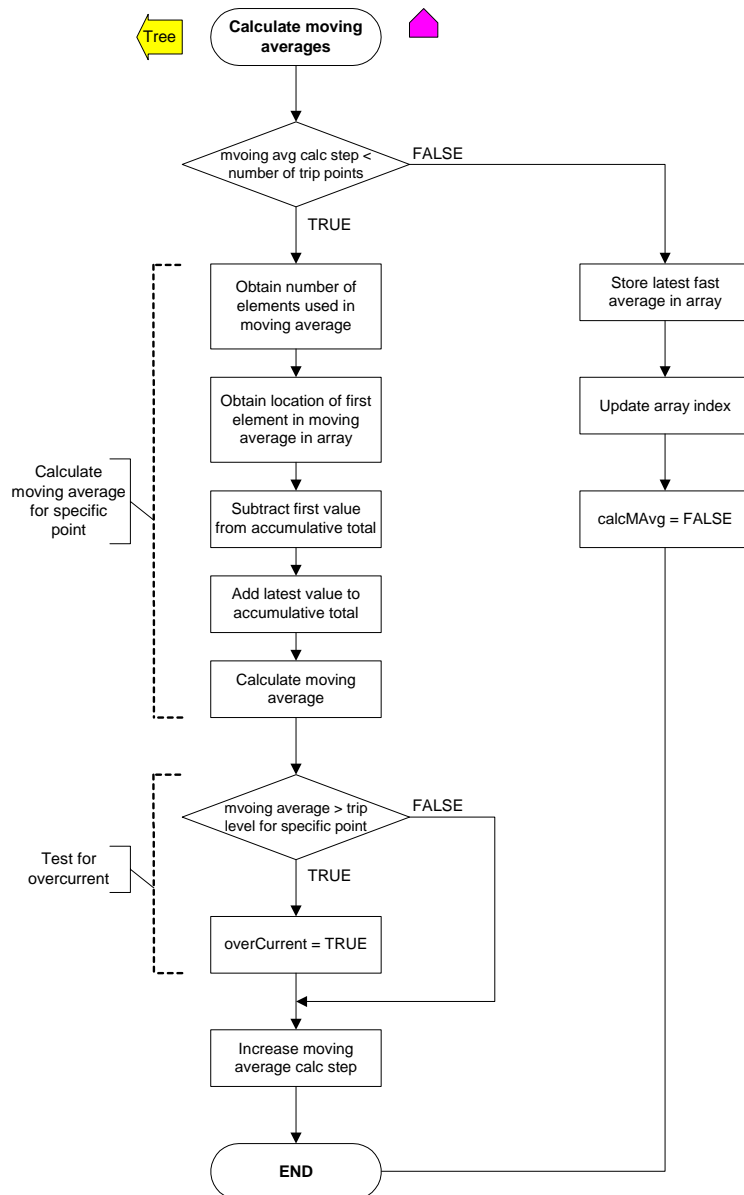


Figure 6-14: "Calculate moving averages" procedure

### 6.3.2.F Process transformer temperature

Main ⇒ Process transformer ⇒  
temperature

The average transformer winding temperature is calculated, and used to determine if the thermistor sensor is operational and whether or not the system should go into temperature limiting mode.

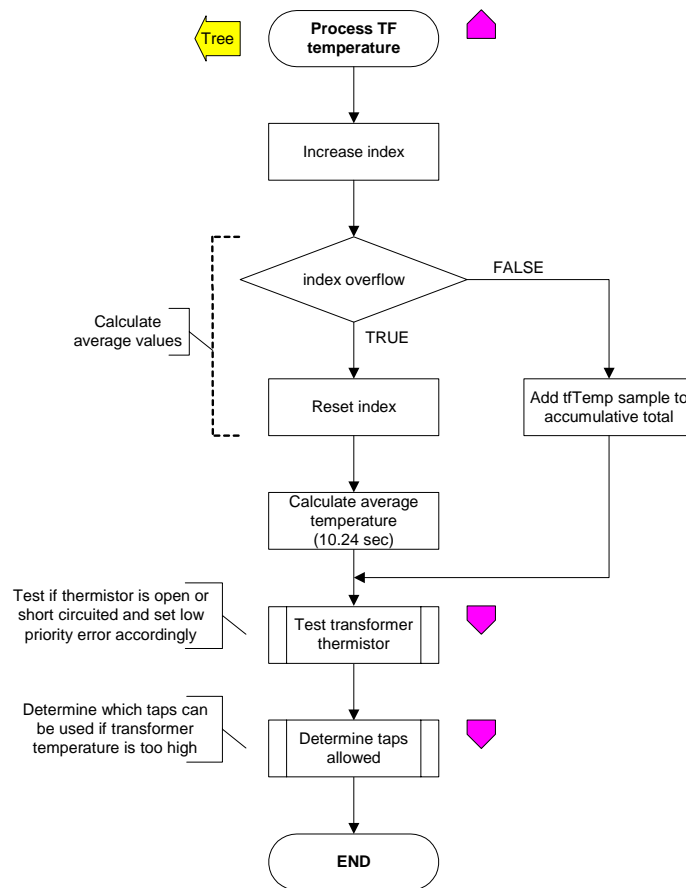


Figure 6-15: "Process transformer temperature" procedure



### 6.3.2.F.ii *Determine taps allowed*

---

Main	⇒	Process transformer temperature	⇒	Determine taps allowed	⇒
------	---	------------------------------------	---	---------------------------	---

---

The transformer is designed for a 5 kVA. Since a substantial overload rating is required the transformer winding temperature is measured to protect the windings. If the temperature goes too high, the temperature limiting mode will be entered, thereby disabling high boost taps to reduce the current through the transformer. If no other errors (low or high priority) are present, the error LED will be turned on to indicate that the system is operating in temperature limit mode.

(If the transformer temperature sensor fails, the current trip levels will be set to that of a 5 kVA system. As the transformer can operate safely at these currents all the taps can be used if the sensor has failed.)

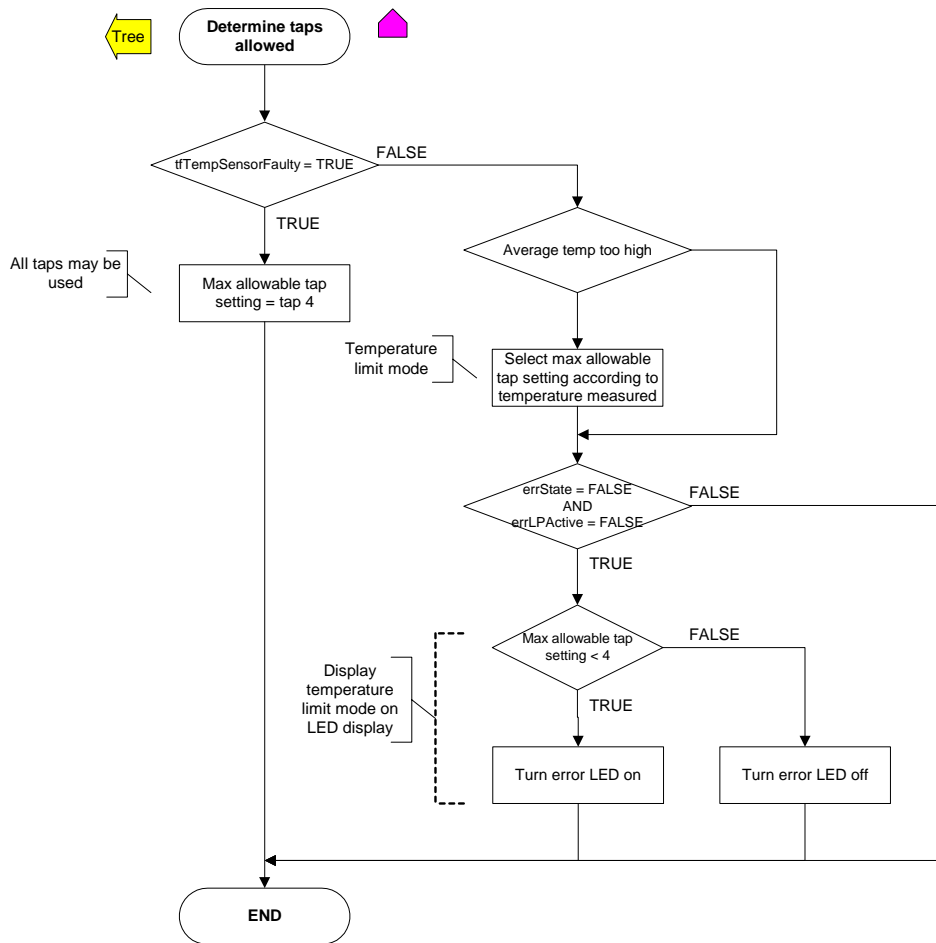


Figure 6-17: "Determine taps allowed" procedure







### 6.3.2.H Error

Main      ⇨      Error      ⇨      ⇨

The procedure detects, handle restart the system if an error has occurred.

and

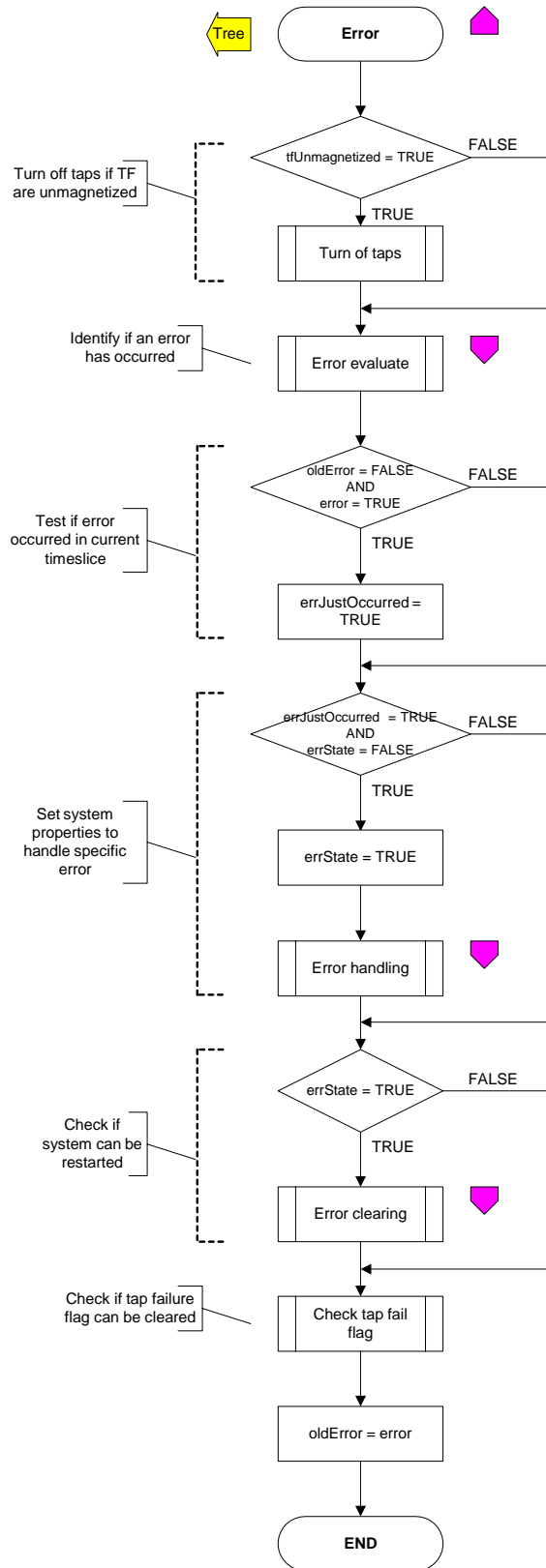


Figure 6-20: "Error" procedure

### 6.3.2.H.i *Error evaluate*

---

Main      ⇒      Error      ⇒      Error evaluate      ⇒

---

Most errors are tested for in this procedure, which include:

- Instantaneous over current  
10 ms Average of the supply current exceeds the threshold value.
- Under and over voltage  
10.24 s Moving average of the supply voltage exceeds the threshold values.

During a short circuit condition, the supply voltage will fall to a low value. To prevent the system from detecting this as an under voltage error and turning the system off, the voltage checking is disabled during the short circuit and for a certain time period after the short circuit has been cleared. This is needed as the supply voltage moving average measurement will slowly increase once the short circuit has been cleared.

For the same reason the voltage checking is disabled during system startup, thereby providing sufficient time for the moving average to increase.

- Heat sink over temperature
- Transformer over temperature

Some errors are detected in other procedures, which include:

- Over current error - Detected for each individual point on the tripping curve
- Nominal tap failure - Nominal tap failed to turn on
- Tap shorted – Tap is on without being turned on
- Repetitive short circuit – Frequency of short circuits is too rapid

All of these errors are then combined into a single error flag.

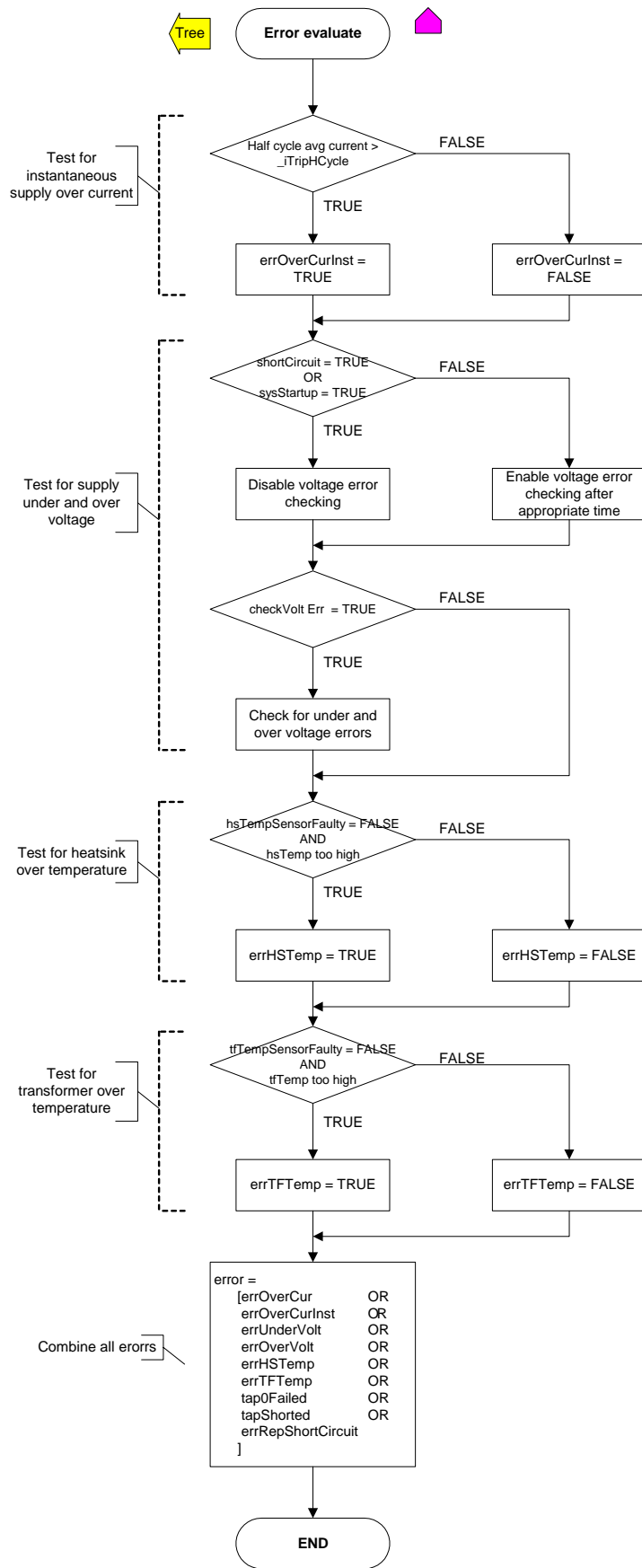


Figure 6-21: "Error evaluate" procedure

### 6.3.2.H.ii *Error handling*

---

Main      ⇒      Error      ⇒      Error handling      ⇒

---

When an error is recognized, all the taps are turned off and the error processed.

Each error has an error code (number of flashes on the error LED) and an automatic restart period associated with it. To process the error the error code and restart timer values associated with the particular error are loaded.

To minimize the electricity interruption period, the restart times associated with each error has been selected to be as short as possible. If errors occur in rapid succession, it could lead to unnecessary stress in the system components. To avoid this, the time between successive errors are monitored. If too many errors occur within a certain window period a repetitive error state will be recognized. The normal restart times associated with each error will now be multiplied by a certain factor to minimize stress in the components.

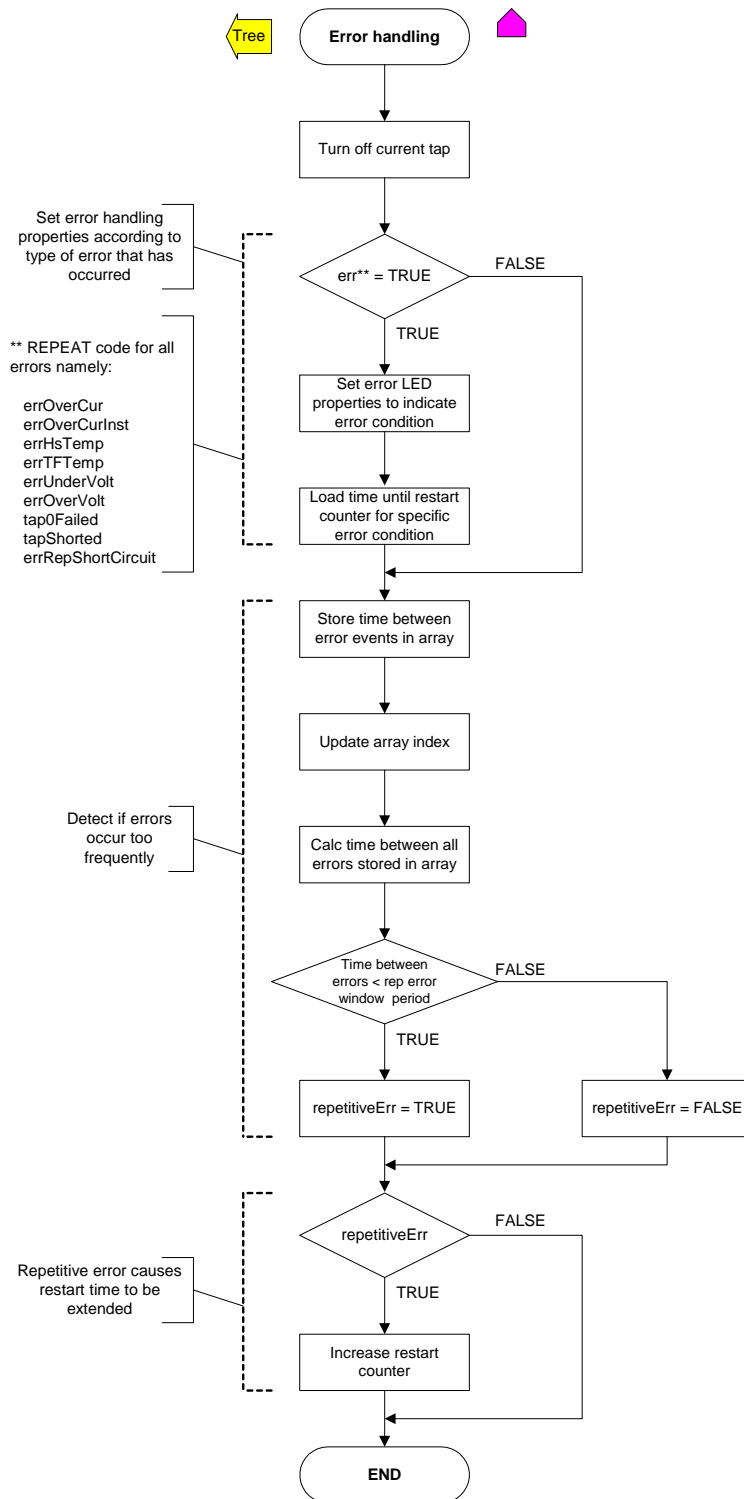


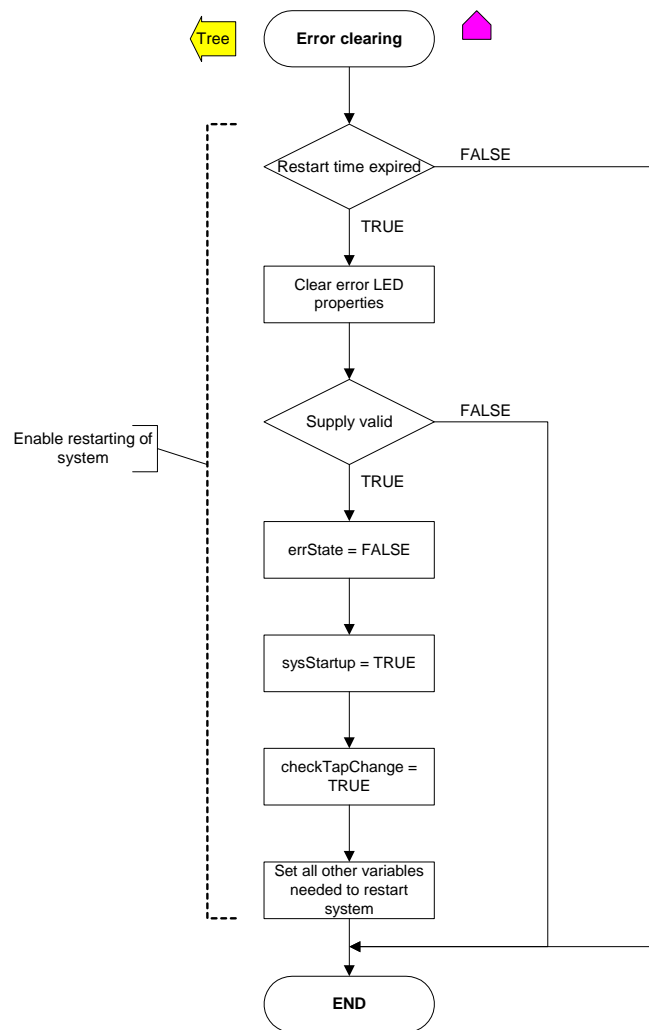
Figure 6-22: "Error handling" procedure

### 6.3.2.H.iii *Error clearing*

Main ⇒ Error ⇒ Error clearing ⇒

Once the restart time period has expired the system can be configured to reactivate itself.

The error LED properties, displaying the error code, is cleared. If the supply voltage is not valid, the system will not turn on. If however the supply voltage is valid the system variables are configured allow the system to restart itself.



**Figure 6-23: "Error clearing" procedure**

### 6.3.2.I Short circuit handle

---

Main      ⇨   Short circuit handle   ⇨      ⇨

---

This procedure detects and clears the short circuit state.

A short circuit is detected if the 10 ms supply current average exceeds the set threshold value. Once a short circuit is recognized the system variables must be set up to enable the system to change to the nominal tap, which has a higher power rating than the other taps.

Once the average current falls below a certain level, the short circuit state can be cleared, but only if the average current remains below this level for more than 20 seconds. If the current increases above this level during the 20 second interval, the system will issue a repetitive short circuit error. This will cause the system to turn off to avoid unnecessary stress to the system components.



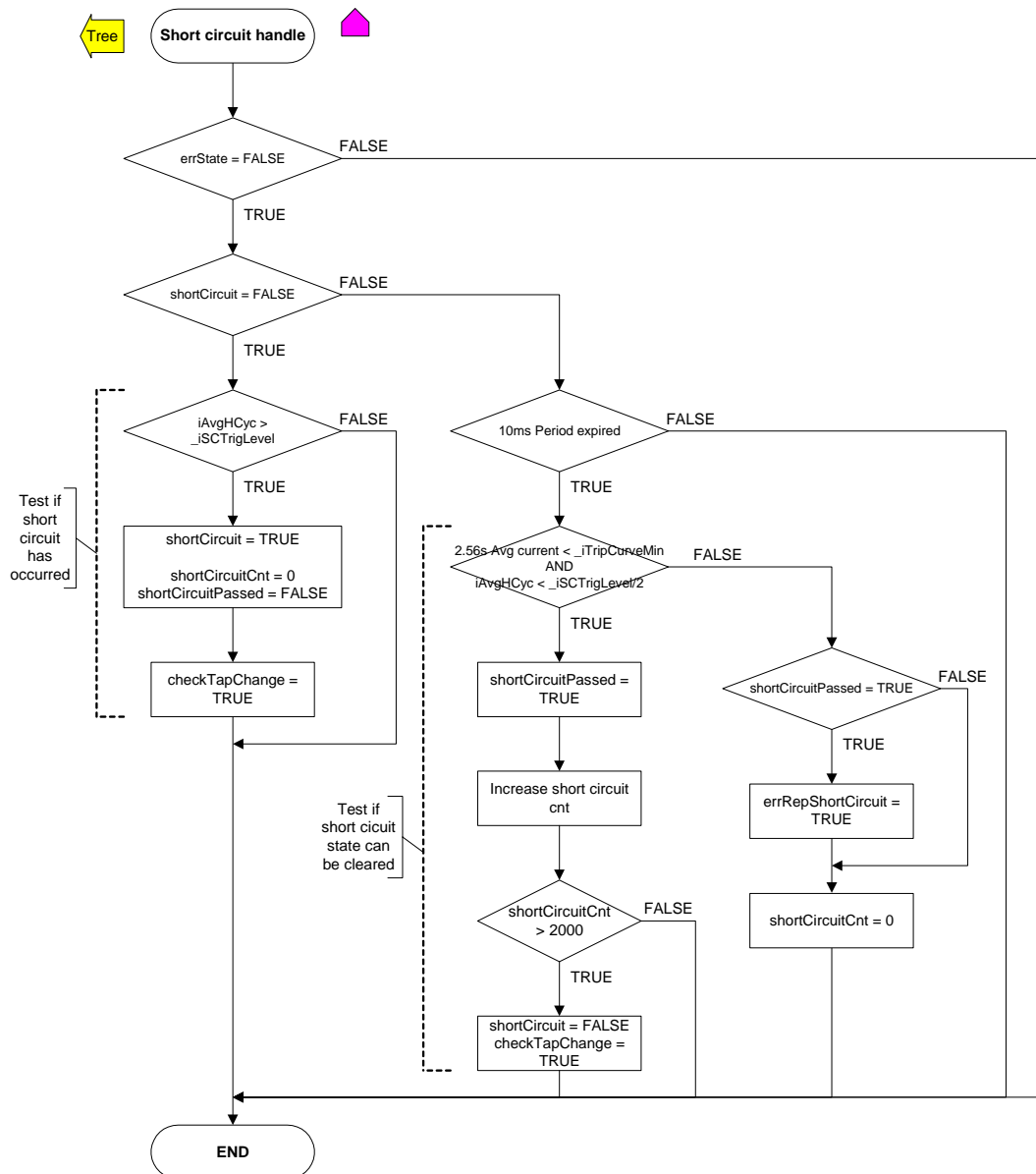
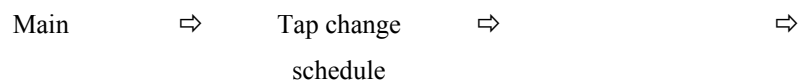


Figure 6-24: "Short circuit handling" procedure

## Tap change schedule



During a tap change the load will see a rapid change in voltage, which might cause a flicker in the intensity of a light bulb. To minimize this flicker, the number of tap changes is controlled by allowing the system to check for tap changes only at certain scheduled time intervals.

Exceptions to this normal interval period are allowed during:

- Over voltage  
Tap change intervals are set short, to quickly reduce the over voltage.
- Start up  
Tap changes can only be allowed after the system had sufficient time to calculate all voltage averages.
- Transformer demagnetization

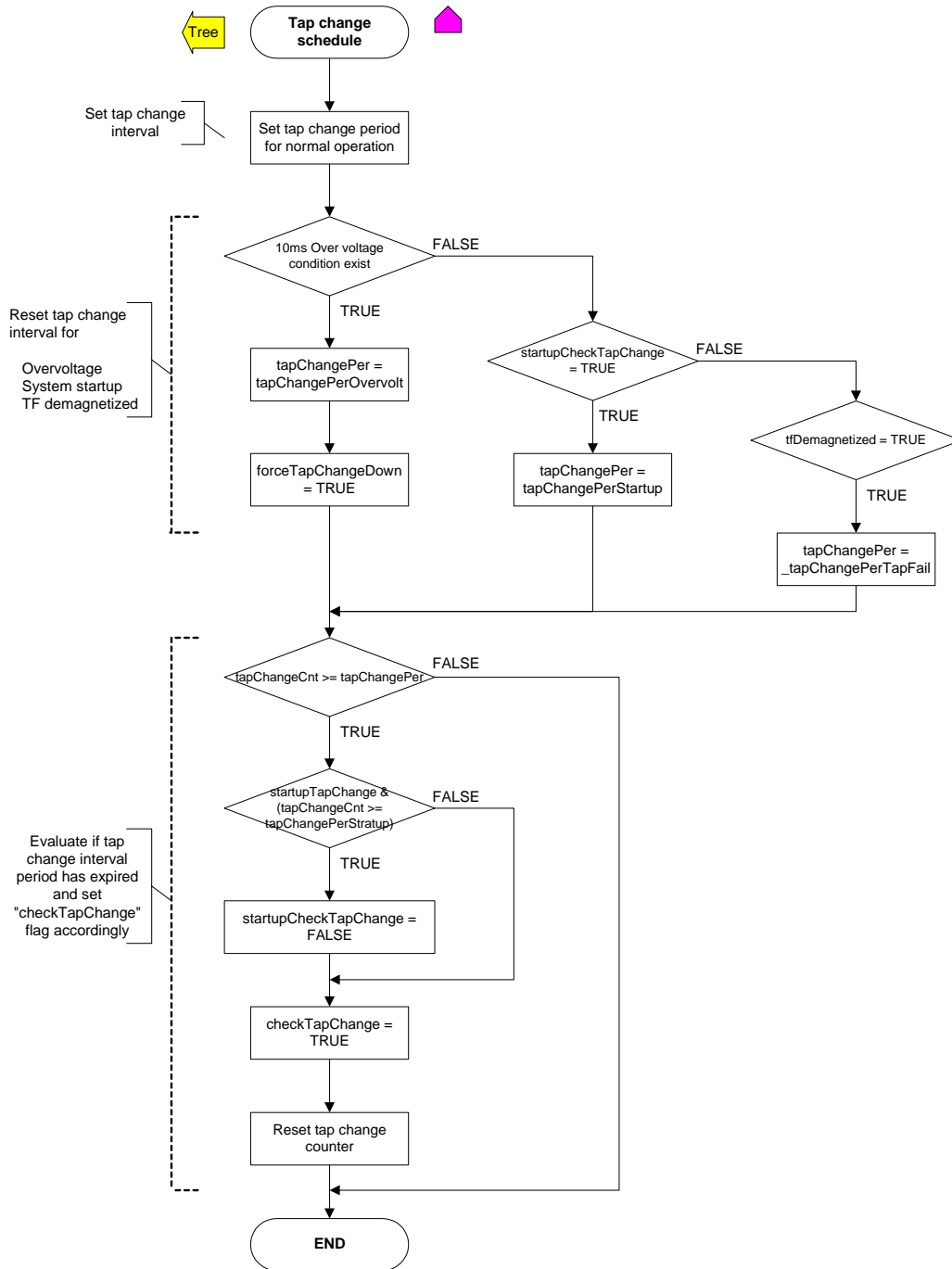


Figure 6-25: "Tap change schedule" procedure

### 6.3.2.J Tap change evaluate

Main      ⇨      Tap change      ⇨      ⇨  
   evaluate

If the tap scheduling procedure has set the “checkTapChange” flag, the system can evaluate the system to see if a tap change needs to be made.

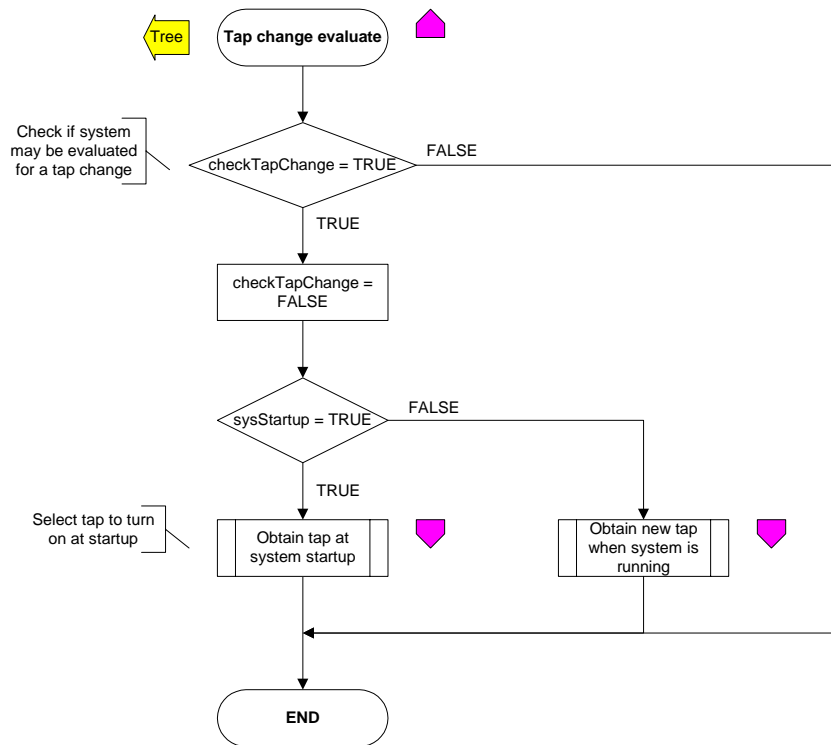


Figure 6-26: "Tap change evaluate" procedure

### 6.3.2.J.i *Tap eval - startup*

Main ⇒ Tap change ⇒ Tap eval - startup ⇒ evaluate

A demagnetized transformer implies that no voltage is present on the load side of the transformer. If the transformer is not demagnetized at startup a load voltage is present, implying that one of the taps is already turned on, even though the controller has not yet turned on any taps. One of the taps is therefore internally shorted and the tap shorted error is set.

If the transformer is demagnetized, the system can obtain the required tap to be turned on at startup and set the “tapChangeRequest” flag, to indicate that a tap change needs to be made.

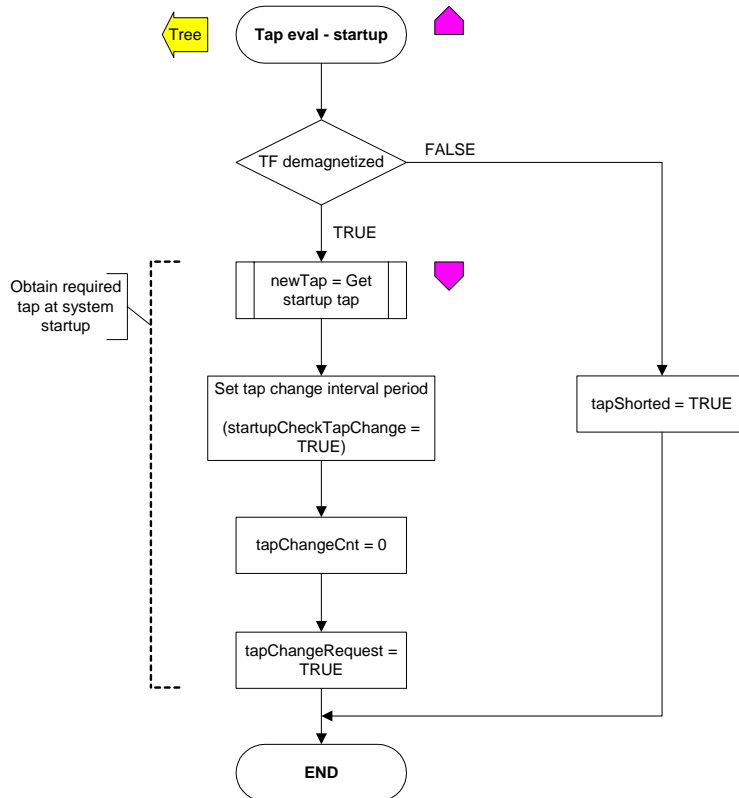
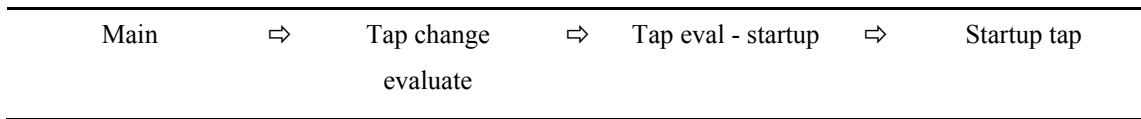


Figure 6-27: "Tap eval - startup" procedure

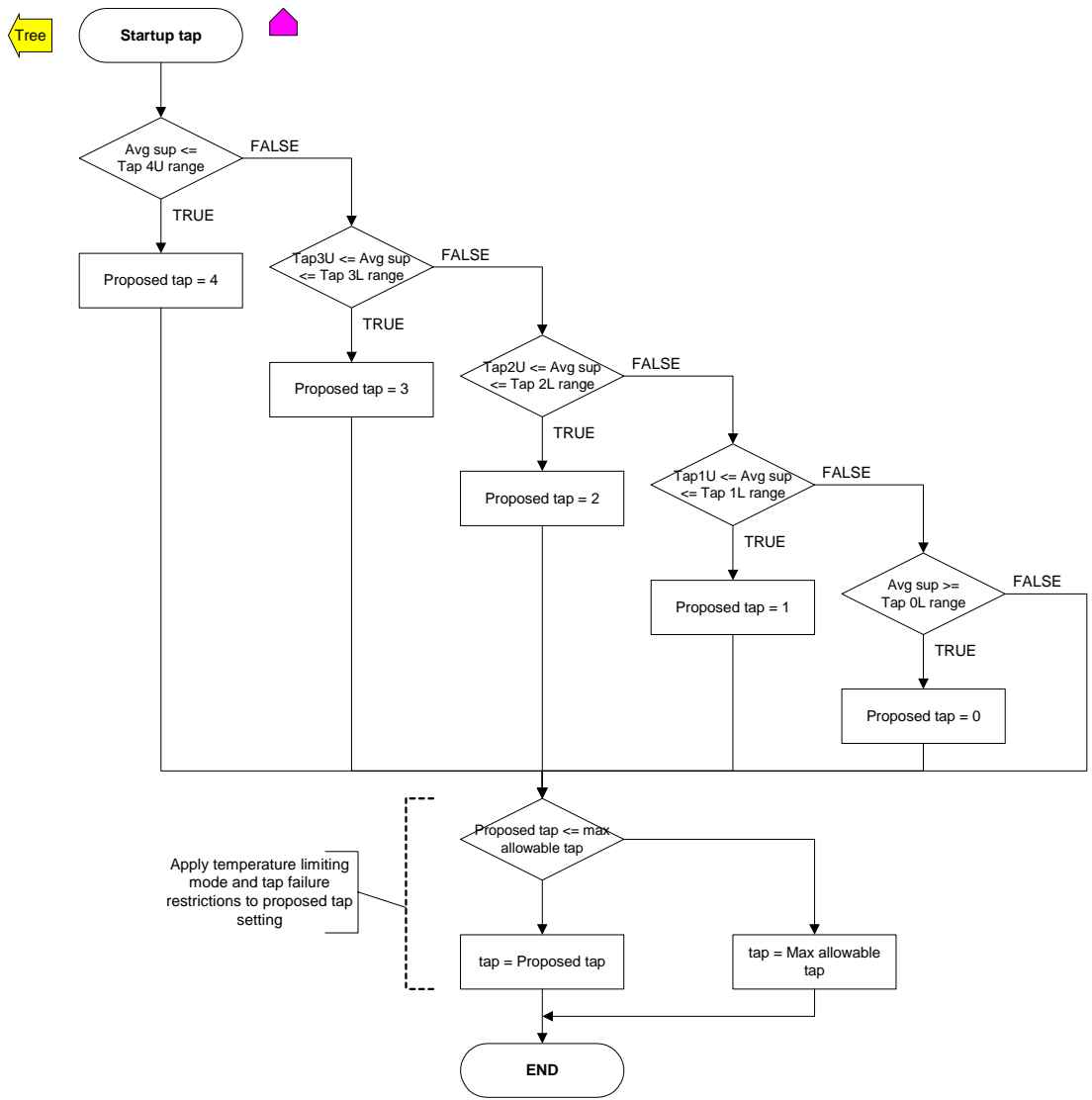
### *Startup tap*



Because no load voltage is present at startup to guide the system to tap up or down, the startup tap is selected based on the magnitude of the supply voltage.

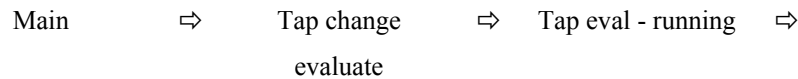
If the system startup has been caused by an automatic startup (following an error occurrence) it might be possible that the transformer was operating in temperature limiting mode and that certain taps are not allowed to be used.

The initial tap chosen can therefore be adjusted if the system was operating in the temperature limiting mode.



**Figure 6-28: "Startup tap" procedure**

### 6.3.2.J.ii *Tap eval - running*



This procedure applies if the system is already operating and a new tap selection must be made. Four scenarios exist:

- Tap failure has occurred

If the transformer is demagnetized when a new tap selection must be made, the current tap has failed to turn on. To verify that the tap does indeed not turn on, the tap will be reactivated a number of times. If it still fails to turn on, it will be marked as failed.

If this failure occurs at the nominal tap, the nominal tap failure error will be set and the system will turn off. If another tap has failed, this tap and all the taps boosting the voltage by a bigger margin will be disabled.

- Short circuit state is present - The nominal tap must be selected as the new tap setting.
- Over voltage state is present – The load voltage must be reduced, therefore the new tap setting should provide less voltage boost.
- Normal state – The tap selection will be either up or down depending on the load voltage magnitude.

Once the new tap has been selected a tap change request is issued to allow the system to implement the tap change and the current tap is turned off.



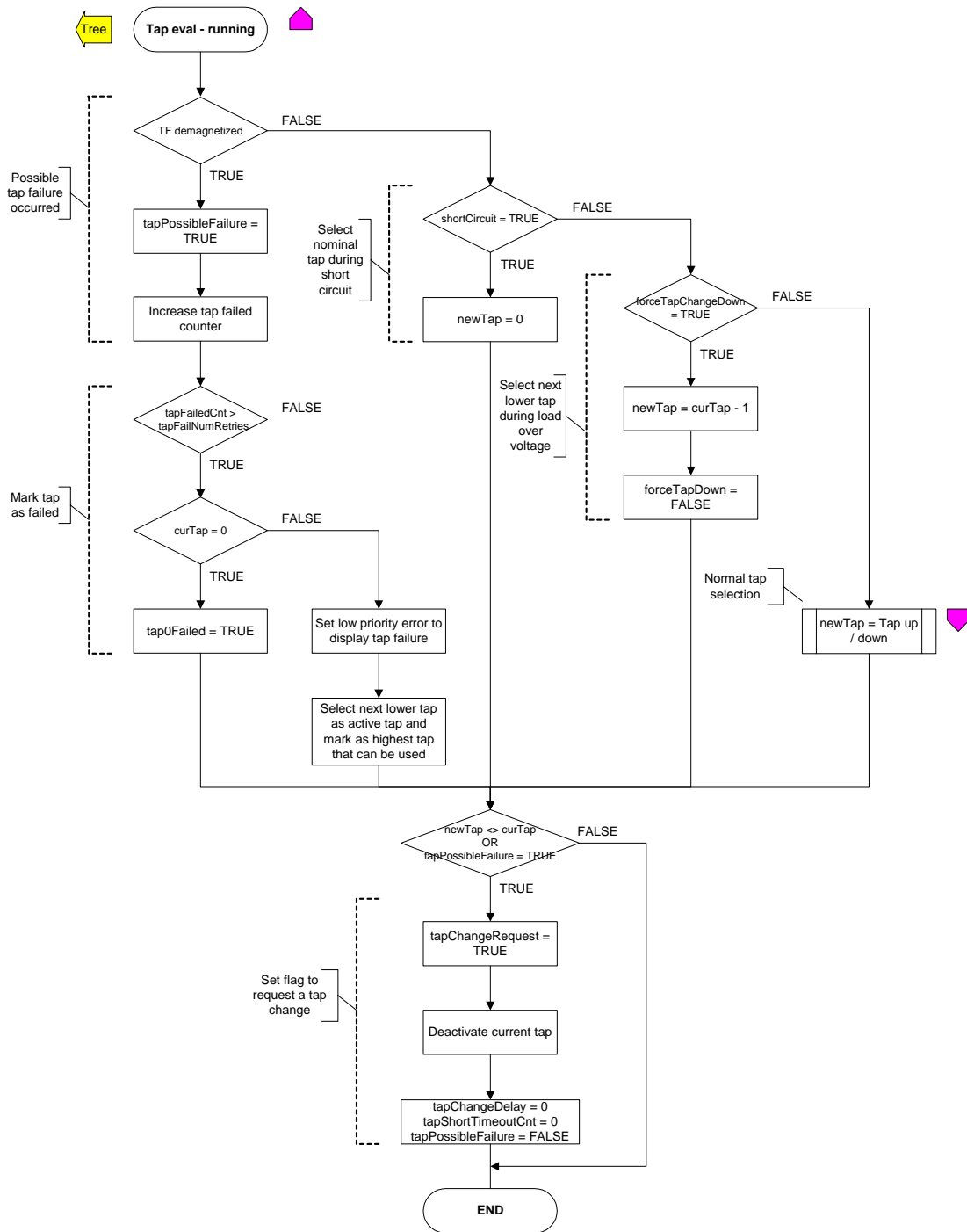


Figure 6-29: "Tap eval - running" procedure

## Tap up / down

Main ⇒ Tap change ⇒ Tap eval - running ⇒ Tap up / down evaluate

Tap selection during normal operation is made by sequentially tapping up or down.

If the average load voltage is too high, the new tap must be selected that will cause the load voltage to decrease. On the other hand, if the load voltage is too low a new tap must be selected to increase the load voltage.

These tap selections can be modified to take into account that the system is operating in temperature limit mode, or that some taps have failed. (In both cases only certain taps will be allowed to be used.)

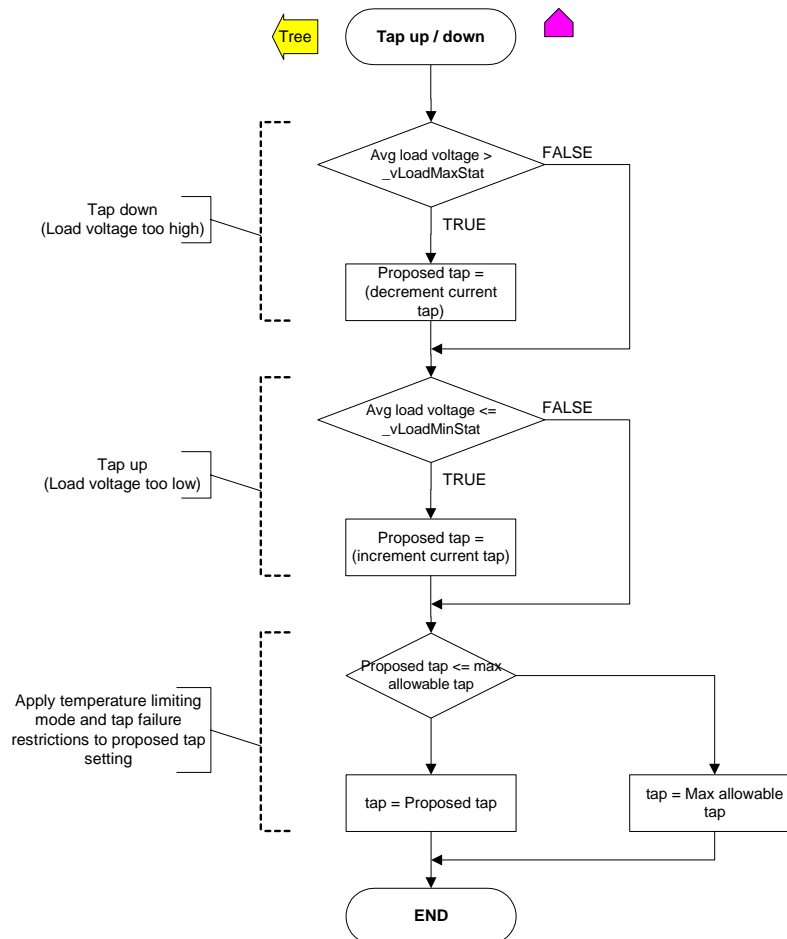


Figure 6-30: "Tap up / down" procedure

### 6.3.2.K Tap change implement

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Main	⇒	Tap change implement	⇒	⇒
------	---	-------------------------	---	---

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This procedure implements / activates the new tap that has been selected. (The current tap has already been issued to turn off, but the turn off still needs to be recognized to activate the new tap selection.)

If a tap change request has been made and more than 40 ms has passed since the request was issued, the system recognizes a tap shorted error. This is because the tap has been requested to turn off, but has never turned off, as no tap turn off detection mechanism has picked up the turn off or commutation of the tap.

To implement the tap change, three scenarios exist:

- Short circuit state is present - During a short circuit, the load voltage will be close to zero and the tap commutation cannot be reliably detected from the load voltage. The magnitude of the supply current is therefore used to detect when the tap has commutated.

As soon as the tap turn off is recognized, the new tap is turned on.

- Transformer is demagnetized - If the transformer is demagnetized the new tap should only be activated at the peak of the supply voltage. This is to prevent a large inrush current from flowing into the transformer.

As soon as the peak of the AC voltage is recognized, the new tap is turned on.

- Normal state - The system will wait for the tap commutation to be detected. Once this is recognized, the new tap will be turned on.

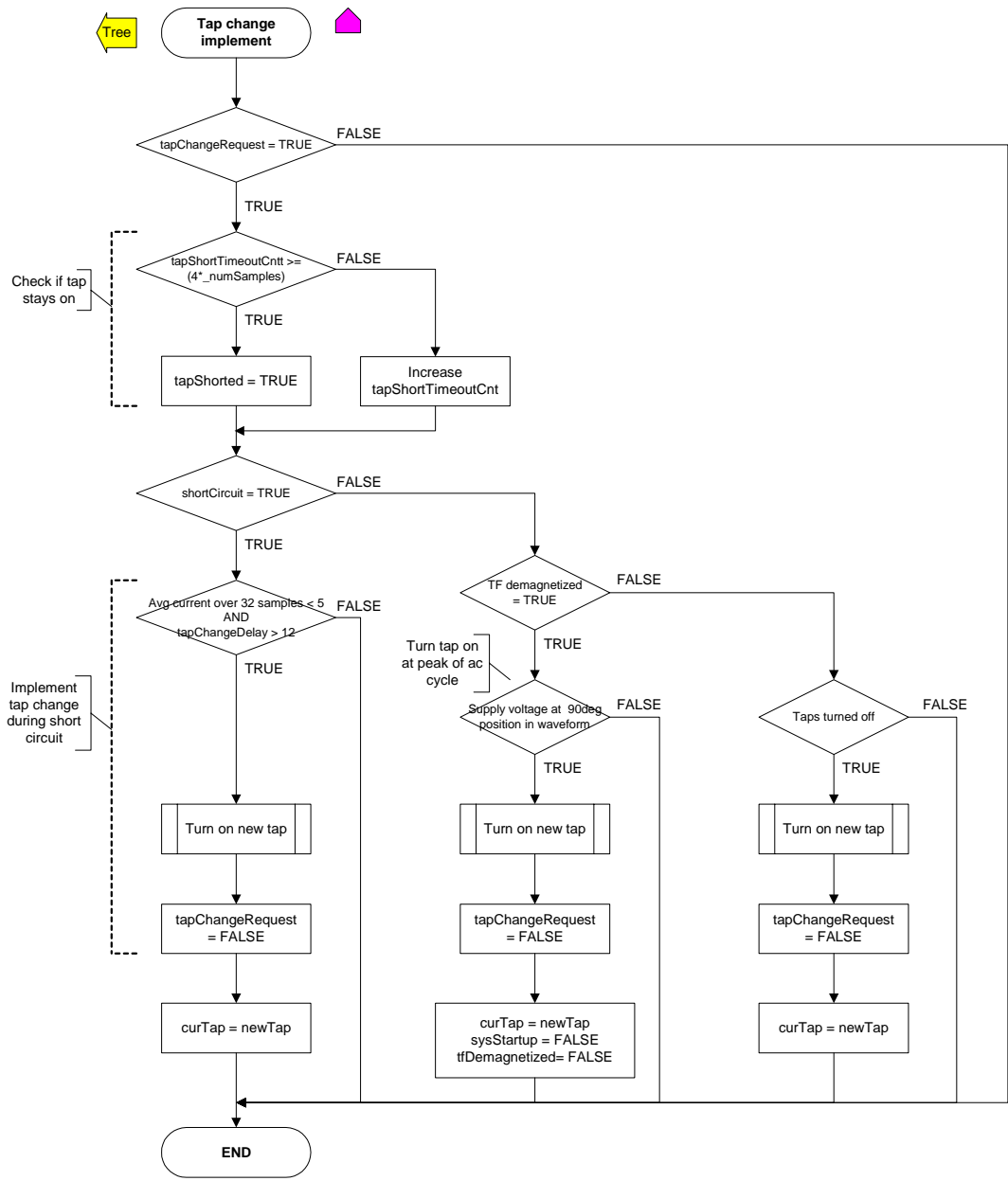


Figure 6-31: "Tap change implement" procedure

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# **Chapter 7**

## Results

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## 7 Results

This chapter discusses the results obtained from tests performed on the EVR in a laboratory environment. These tests verify the electrical and thermal design of the EVR as well as the correct operation of the software code. Results obtained from a field trial installation are also presented.

### 7.1 Laboratory results

The laboratory results obtained include the following:

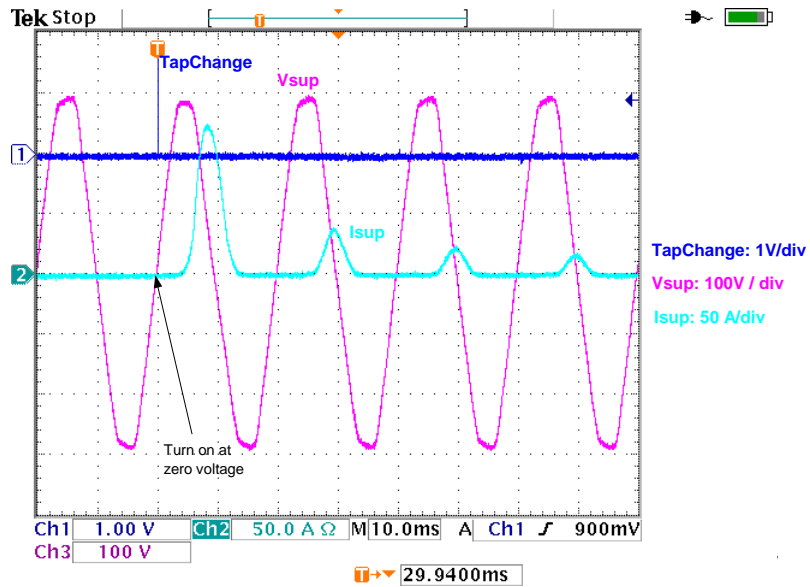
- Core saturation waveforms
- Tap changing waveforms
- Output glitch suppressor operation
- Response time
- Voltage surge test
- Temperature measurements
- Power loss / efficiency measurements

#### 7.1.1 Core saturation

The time instant at which the EVR turns on need to be controlled to prevent large inrush currents being drawn from the supply due to transformer core saturation. To illustrate this experimentally, the EVR is turned on close to the zero and peak value of the AC supply voltage. In each case no loads are connected to the EVR.

##### 7.1.1.A Turn on at zero voltage

In Figure 7-1 the transformer is turned on near the supply voltage zero crossing. The “*TapChange*” signal in the figure is a control signal generated inside the controller and is used as a trigger event to capture the waveforms. A high to low transition on “*TapChange*” indicates the time instant where the system is turned on / tap is activated.

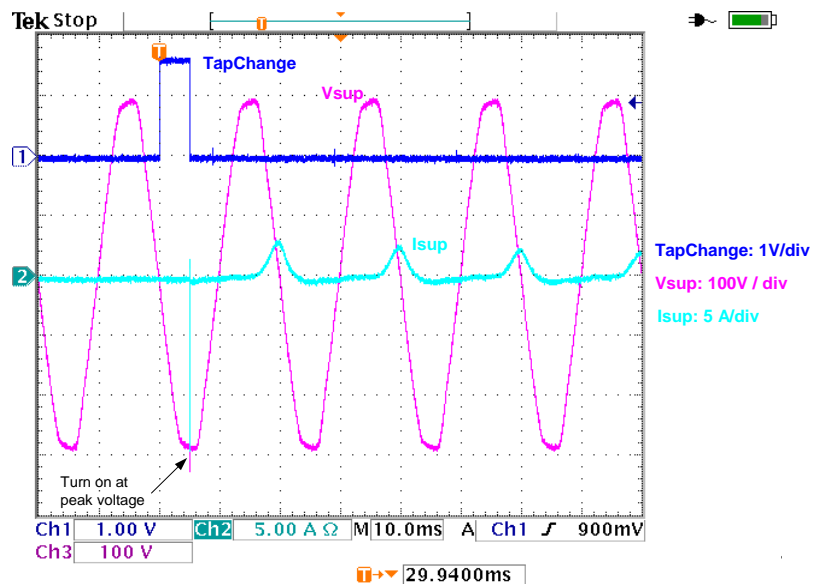


**Figure 7-1: Turn on at zero crossing of supply voltage**

Turning the transformer on at the supply voltage zero crossing point, causes a first cycle saturation current of 125 A peak to flow. This current decays rapidly within 4 cycles.

### 7.1.1.B Turn on at peak voltage

In Figure 7-2 the transformer is turned on at the peak of the supply voltage. The resulting supply current is now only 3 A peak.



**Figure 7-2: Turn on at peak of supply voltage**

The 17 A pulse current at turn on is due to the charging of the output pulse suppression capacitor.

### 7.1.1.C Conclusion

From the foregoing discussion, it can be seen that turning a transformer on at zero voltage should be avoided due to the large inrush currents that can occur. These inrush currents cause unnecessary thermal and mechanical stresses in the transformer, which could lead to premature failures.

### 7.1.2 Tap changing

The transitions that occur during tap changing are shown here, both with resistive and inductive loads connected to the EVR.

#### 7.1.2.A Resistive load

##### Stepping down

Figure 7-3 illustrates tap changing (tap 4 to tap 3) for a 10 kVA, resistive load. The output voltage is reduced / stepped down, by changing from tap 4 to tap 3.

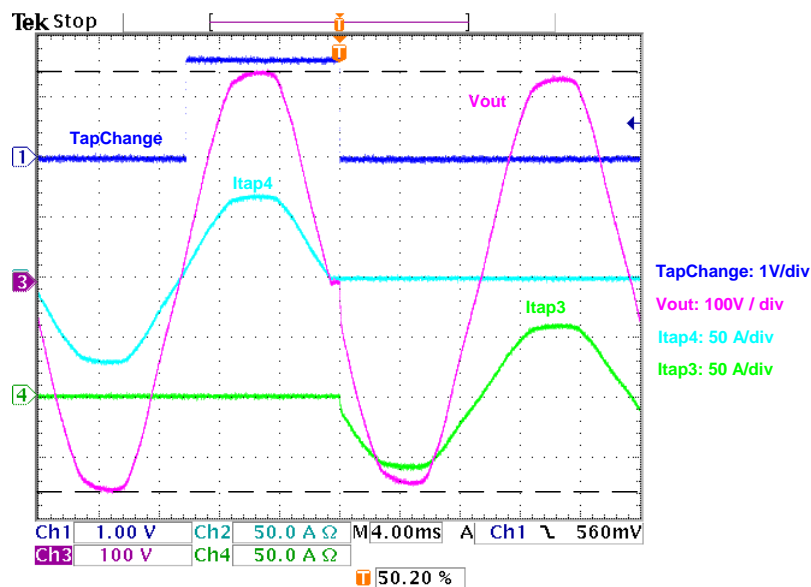


Figure 7-3: Tap changing - Stepping down - 10 kVA resistive load

A low to high transition on the “TapChange” control signal indicates that the controller decided that a tap change is necessary, due to the load voltage magnitude being out of range. At this



point tap 4 is instructed to turn off by discontinuing the thyristor gate pulses. The system now waits for the thyristor on tap 4 to commutate, to enable a safe changeover of taps.

At the instant in time when tap 4 commutates, the output voltage should remain zero because no thyristors are turned on (the auto transformer is therefore disconnected from the supply) and the load is purely resistive. The controller monitors the output voltage to detect the zero output voltage condition. Once detected, it is safe to turn on tap 3, indicated by the high to low transition of the “TapChange” signal. To safely detect the commutation instant through monitoring of the output voltage, a 600  $\mu$ s time period during which the output remains off is introduced.

### Stepping up

For reference Figure 7-4 shows the tap transition, switching from tap 3 to tap 4, thereby stepping up / increasing the output voltage. Detection of the commutation once again introduces a disruption in the output voltage with duration of 600  $\mu$ s.

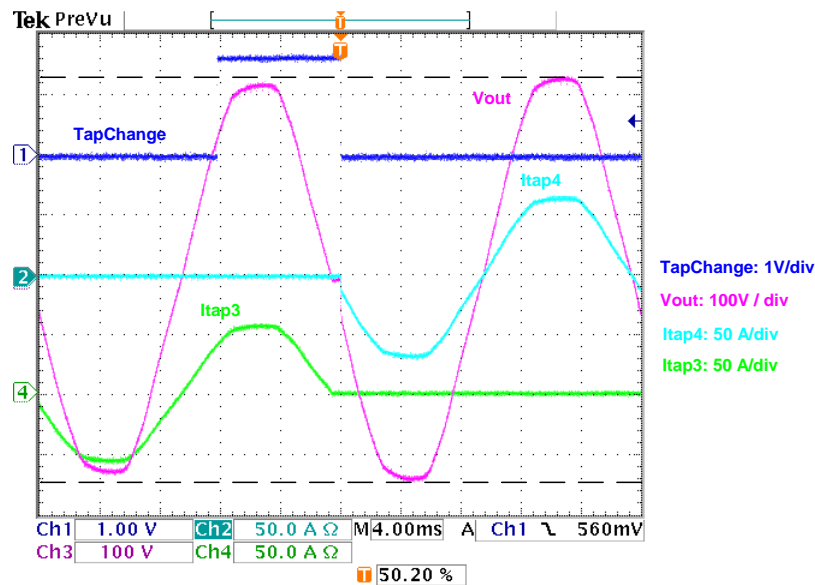
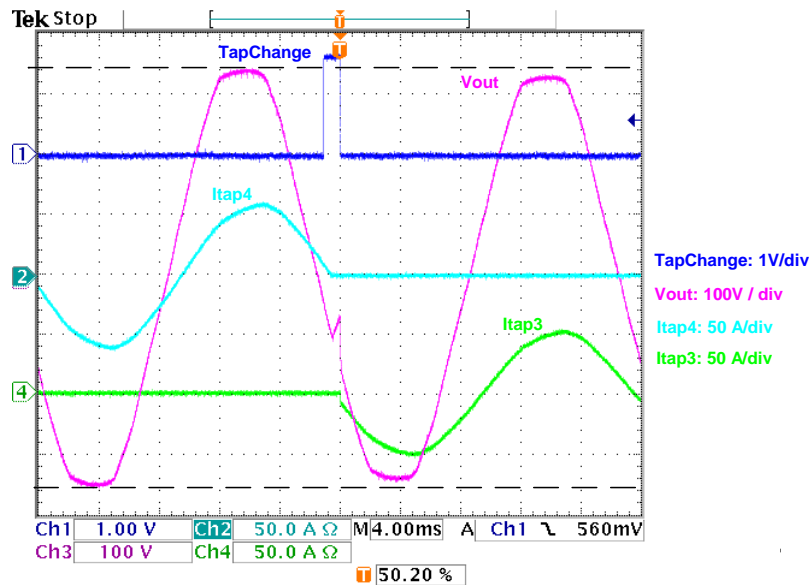


Figure 7-4: Tap changing – Stepping up - 10 kVA resistive load

### 7.1.2.B Resistive / inductive load

Figure 7-5 illustrates tap changing (tap 4 to tap 3) for a resistive-inductive (RL) load. The output voltage is decreased / stepped down, by changing from tap 4 to tap 3.



**Figure 7-5: Tap changing – Stepping down - RL load**

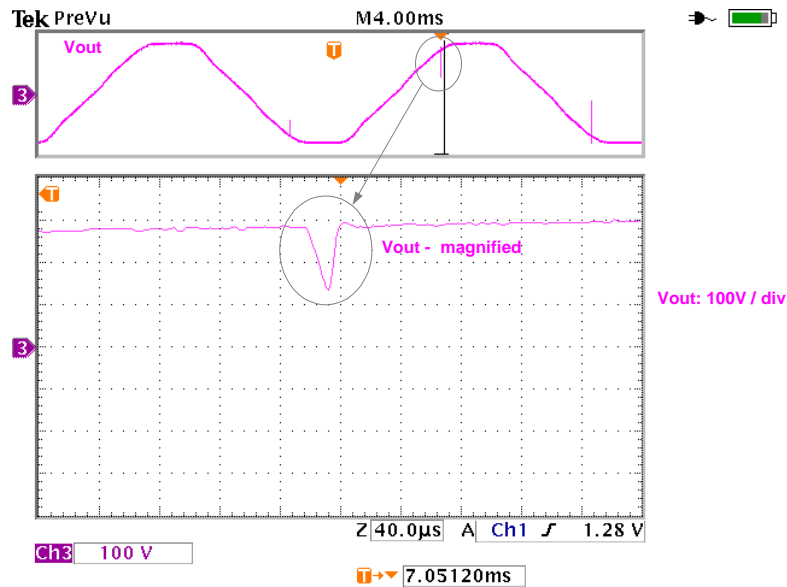
A low to high transition on the “TapChange” signal shows where the gate signal to tap 4 was turned off, while the high to low transition on “TapChange” shows where tap 3 was turned on.

When the thyristor on tap 4 commutates, the load voltage starts to decrease. It does however not drop to zero instantly, because the decaying transformer flux supports the output voltage. The controller monitors the output voltage to detect this drop in voltage, thereby indicating that the current tap has commutated and the new tap can be activated. The changeover of current between the two taps occurs smoothly, except for the discontinuation in the output voltage of approximately 600  $\mu$ s, due to time taken to detect the thyristors commutation.

### 7.1.3 Output glitch suppression

As discussed on page 74, the interaction between the AC supply current zero crossing and the instant the thyristors are triggered, can cause a glitch in the output voltage.

To illustrate this, the EVR is operated without the glitch suppressor circuitry and an inductive load. The results are shown Figure 7-6. With a specific tap active, a short glitch is present at each current zero crossing due to the thyristor control signal being generated a couple of microseconds after the other the thyristor in the tap switch has commutated.



**Figure 7-6: Load voltage with no pulse suppressor present**

With the inclusion of the pulse suppressor circuitry, the glitches are removed.

### 7.1.4 Response time

The EVR regulates the load voltage between an upper and lower boundary level through measurement of the load voltage. The time taken to react and correct the output voltage due to boundary transgressions is adjustable through software parameters. This enables customizing of the system to a specific line to minimize the occurrence of frequent tap changes. As tap changing introduces a step change in the customer voltage, frequent tap changes can lead to flickering in lights, which could be a source of irritation to the customer.

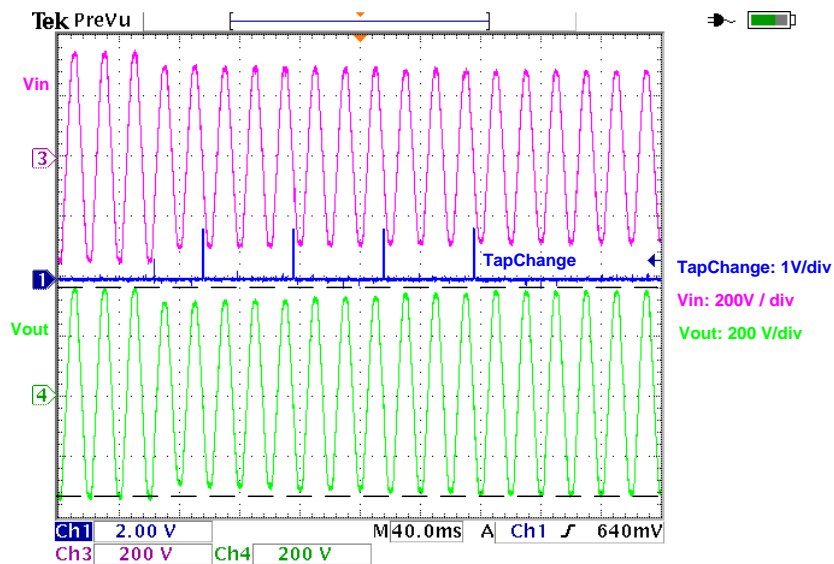
To enable the system to react faster to over voltage conditions (which could damage customer appliances), separate response times can be selected for under and over voltage conditions.

To illustrate the effect of different response time settings, two examples are provided.

#### 7.1.4.A Fast response time

In this case, the EVR is set to evaluate the load voltage based on a 60 ms average. If a sudden step in supply voltage occurs, the EVR will aim to correct the output voltage by sequentially tapping up or down, until the load voltage is within its boundaries. The times between tap changes for both under and over voltage conditions has been set to 60 ms. Figure 7-7 shows how the load voltage reacts to a sudden decrease in the supply voltage.

As the supply voltage drops instantly from 250 V to 210 V, the load voltage drops with the same percentage, as the EVR has not yet recognized the voltage drop. About 60 ms later the system recognizes that the load voltage is below the lower boundary and a tap change takes place to increase the voltage. After a further 60 ms period the load voltage is still below the lower boundary and another tap change occurs. This sequence repeats until the load voltage falls between the upper and lower boundary levels specified.



**Figure 7-7: Response time - fast**

It is important to note that the 60 ms response time can lead to a substantial over voltage if the supply voltage suddenly changes from a low to a high value.

If the EVR is operating from a supply voltage of 207 V and the supply instantly changes to 253 V, the EVR will continue to operate on the lowest tap for the next 60 ms. Consequently the output voltage will be boosted by a factor of 1.19 (calculated from the transformer winding ratio), resulting in an output voltage of 300 V. The over voltage will be reduced in successive 60 ms intervals, until it falls within the normal required output voltage range.

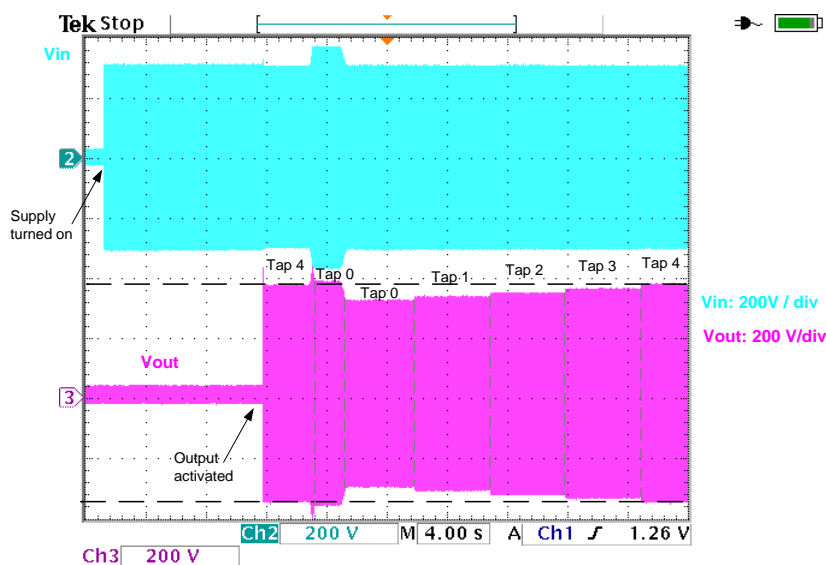
#### **7.1.4.B Slow response time**

Response time to an over voltage condition has been set to 20 ms (based on 10 ms load voltage averages), while under voltage response time is set to 5 seconds (based on 1 s load voltage averages). Tap changes due to an under voltage condition is thus allowed once every 5 seconds, while over voltage tap changes can occur every 20 ms.

As can be seen in Figure 7-8 the EVR is initially turned on with tap 4 activated, as the supply voltage is low. A sudden increase in supply voltage caused a rapid response from the EVR. Taps were changed sequentially from tap 4 to tap 0 in 80 ms, thereby preventing a long duration voltage overload to the customer.

On the contrary, a rapid decrease in the supply voltage does not lead to a similar fast response. This is because the EVR is only allowed to change a tap setting once every 5 seconds on load under voltage conditions. Consequently the load voltage slowly increases every 5 seconds as the EVR sequentially changes taps to tap 4.

If a high frequency voltage variation is present on the supply line, the slow tap changing will provide some means of immunity against frequent tap changing.



**Figure 7-8: Response time – slow**

### 7.1.5 Coordinated protection

Due to the coordinated protection scheme implemented, a short circuit might last tens of seconds before the EVR either turns off, or the fault is cleared. During this time the power supply transformer which normally supplies power to the controller will not be able to deliver any power as the supply voltage will be close to zero. Power will therefore be obtained from the CT measuring the load current. Results obtained at both the minimum and the maximum expected fault currents if the output of the EVR was shorted close to the point where it was installed are discussed below.

### 7.1.5.A Low fault level

Figure 7-10 shows the supply voltage and supply current to the EVR together with the DC link voltage of the power supply during a short circuit with a magnitude of 155 A.

Referring to the coordinated protection section (specifically Figure 4-38) it can be seen that the 50 A pole top box CB tripping time at this current magnitude falls in a huge range (between 7 and 40 seconds). The EVR must therefore be capable of staying on for at least 40 seconds, to allow enough time the 50 A pole top box circuit breaker to operate.

In this specific test, the circuit breaker took 30 seconds to open. Notice that even though the supply voltage was close to zero during the entire 30 seconds period, the DC link voltage of the power supply did not drop, indicating that the CT was capable of delivering enough power to power the controller.

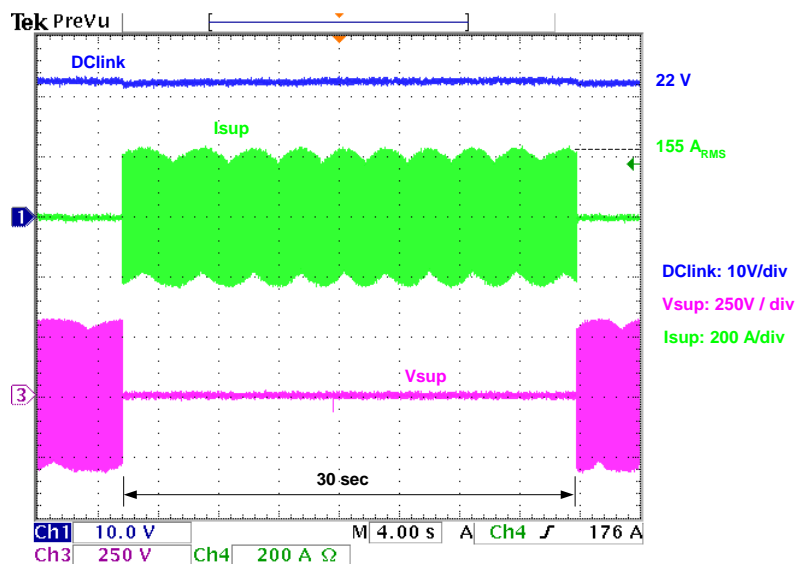


Figure 7-9: Coordinated protection (155 A fault current)

(The “waves” present on the current and supply voltage waveforms are not present in reality. They are caused by the interaction of the sampling rate of the oscilloscope together with the long time division setting used.)

### 7.1.5.B High fault level

Figure 7-10 shows the supply voltage and supply current to the EVR together with the DC link voltage of the power supply during a short circuit with a magnitude of 495 A. This is close to the maximum expected fault current of 500 A that the EVR will be subjected to.

Referring to the coordinated protection section (specifically Figure 4-38) it can be seen that the 50 A pole top box CB can take between 0.1 and 2 seconds to trip, during which time the EVR must stay active. In this specific test, the 50 A CB took 1.8 seconds before it tripped. During this time the power supply's DC link voltage did not drop, but actually increased because of the amount of power generated by the high fault current through the CT.

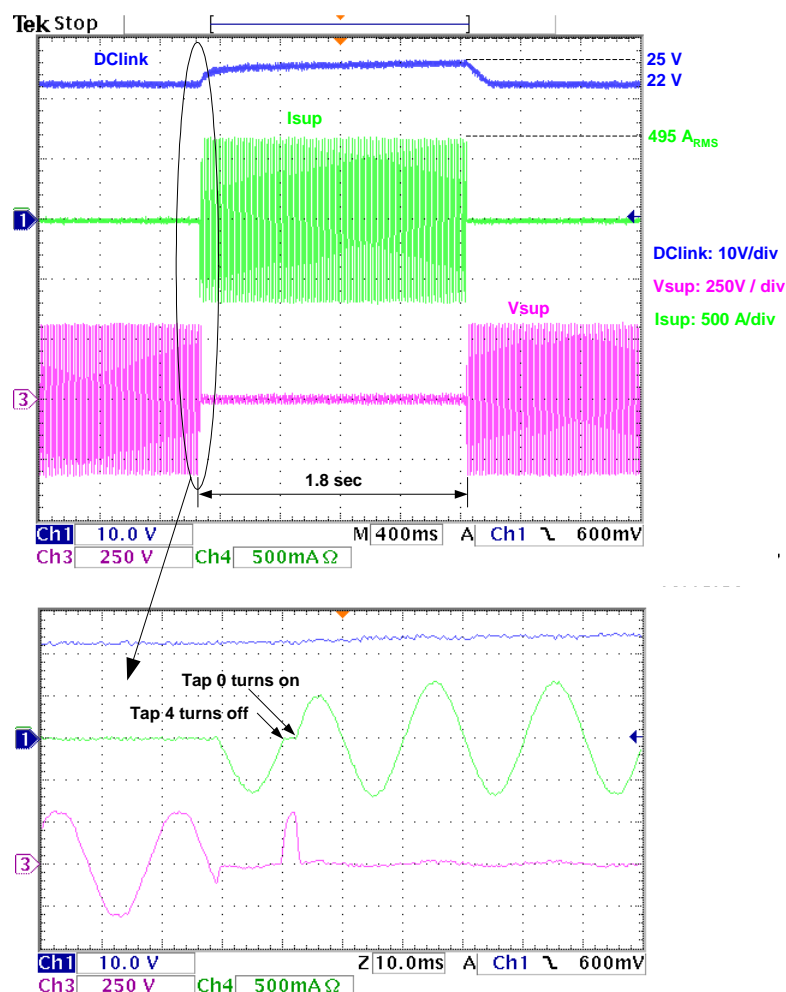


Figure 7-10: Coordinated protection (495 A fault current)

Magnifying the time scale at the start of the fault current (as shown in the bottom part of Figure 7-10), the tap change from the active tap (tap 4) to the nominal tap (tap 0) can be seen. It shows

that the EVR recognized the fault current condition, and successfully changed over to the nominal tap which has the higher fault current withstand capability.

### 7.1.6 Surge voltage tests

Surge voltage tests were done on the thyristor modules used in the EVR as well as on two complete EVR units to verify their operation in the presence of lightning surges. These tests were outsourced, because of a lack of the necessary equipment to perform the tests.

#### 7.1.6.A Thyristor module impulse test

Two thyristor modules (each containing two thyristors) are tested with current impulses of 8/20  $\mu$ s wave shape. These impulses started with peak amplitude of 2 kA, increasing in 2 kA steps up to 16 kA.

The impulses are applied using a combination wave generator capable of delivering voltage pulses with a 1.2/50  $\mu$ s wave and current pulses with a 8/20  $\mu$ s wave shape. The generator can however only deliver this combined waveform up to a peak current magnitude of 8 kA. Beyond this level only current impulses can be delivered, i.e. the open circuit voltage cannot be applied simultaneously.

Two thyristors withstood the impulse tests up to 16 kA level, while one failed at 15.6 kA and the other one at 14 kA. Figure 7-11 shows the application of a 16 kA surge current to one of the thyristor under test.

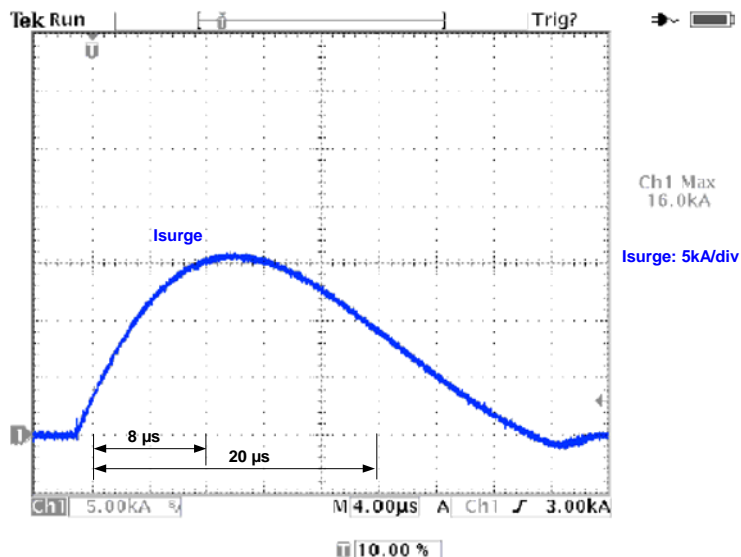


Figure 7-11: 16 kA, 8/20  $\mu$ s Surge current applied to thyristor



### 7.1.6.B EVR impulse test

During the early stages of the EVR development, two EVR prototype units (“EVR A” and “EVR B”) were tested for surge susceptibility, equipped with different MOV protection devices.

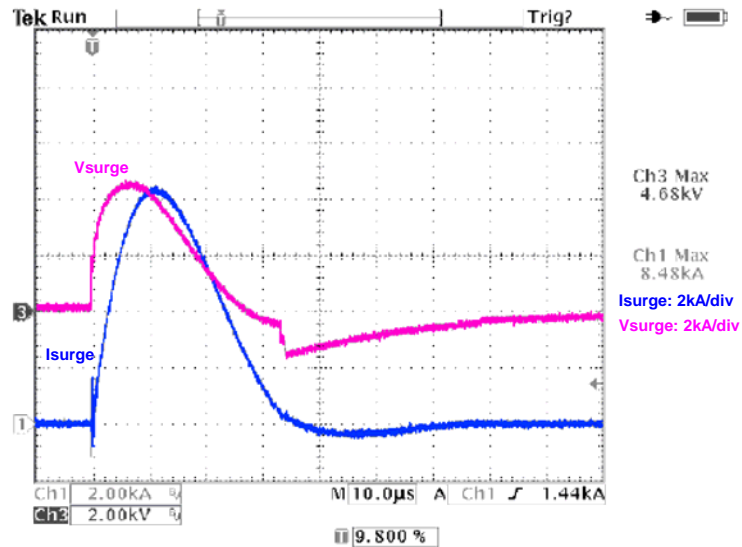
“EVR A” is equipped with 460 V PCB mounted MOVs, capable of handling a surge of 8 kA for a typical 8/20  $\mu$ s current waveform, while “EVR B” is equipped with 275 V DIN rail mounted MOVs, capable of handling a surge of 40 kA for a typical 8/20  $\mu$ s current waveform.

Both EVR units were tested using a standard combination impulse. The generator delivering this impulse applied a 1.2/50  $\mu$ s open circuit voltage impulse or an 8/20  $\mu$ s short circuit current impulse, depending on the load connected across its output terminals. Surges were applied to the two units between the following terminals:

- Supply in and neutral
- Supply in and load out
- Load out and neutral

In each case three impulses of each polarity were applied, i.e. a total of six impulses were applied in each of the above configurations.

The generator capacitor charging voltage for each impulse was set at 19.8 kV, giving a peak open circuit voltage of approximately 19.6 kV and a peak short circuit current of approximately 9.4 kA. Figure 7-12 shows the applied impulse voltage and current flowing into the unit during one of the test.



**Figure 7-12: EVR impulse test**

Both “EVR A” and “EVR B” passed all the tests. On “EVR A” equipped with the PCB mounted MOVs there was signs of flashover on the PCB with nearly every impulse applied.

Due to the flashovers experienced on “EVR A” containing the PCB mounted MOVs and their limited current capability (8 kA), these MOVs and the PCB layout configuration is regarded as not suitable for use in the EVR.

The 40 kA DIN rail mounted surge arrestors used in “EVR B” proved to be effective, but due to their packaging they are too expensive for use in the EVR. Using identical MOVs but instead using a different packaging technique, costs can be reduced enough to justify their use in the EVR. (The packaging technique entails mounting of the MOVs in a glass fiber base with a strong epoxy resin.)

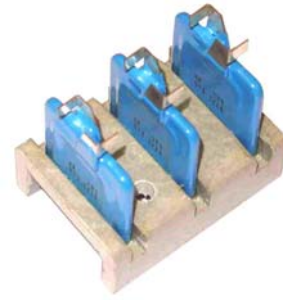
The different surge arrestor variants; PCB mounted MOVs, DIN rail mounted MOVs and glass fiber mounted MOVs are shown in Figure 7-13.



(a) 8 kA, PCB mount



(b) 40 kA, DIN rail mount



(c) 40 kA, Glass fiber mount

**Figure 7-13: Surge arrestors used during EVR development**

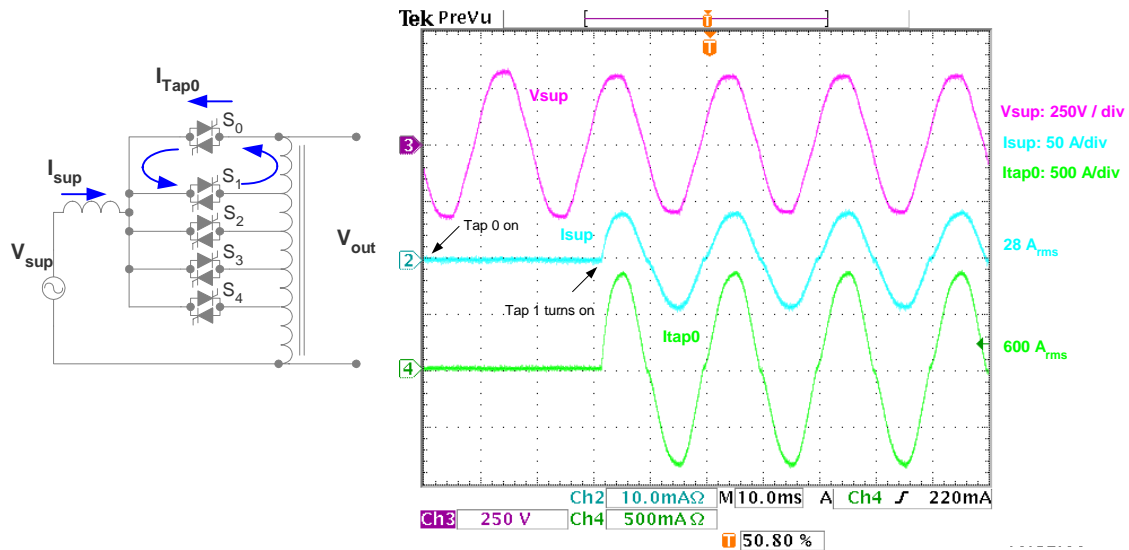
### 7.1.7 Tap winding shorted

In theory it is possible for the thyristor tap switches to turn on in the presence of external line surge transients which exceed the static  $dv/dt$  rating of the thyristors. Although the surge protection added to the EVR will minimize the possibility of such an event it is still prudent to investigate the effect of such an incident.

Exceeding the static  $dv/dt$  rating of the thyristors will cause one or more tap switches to latch on, thereby shorting a portion of the transformer winding. Because the tap switches will automatically commutate at the next current zero crossing in the absence of any further line transients (with no gate signal being applied), a large circulating current will flow between the two taps for a maximum time period of 10 ms. The magnitude of the circulating current will be limited mainly by the resistance of the tap winding.

To verify that the EVR would not be damaged if this were to occur, two taps were turned on simultaneously by applying a gate signal to both tap switches as shown in Figure 7-14 (a). The resulting supply current and circulating tap current were measured as shown in Figure 7-14 (b).

Initially  $S_0$  is turned on, resulting in a negligible supply current because no load is present.  $S_1$  is then also turned on, causing a circulating current with a magnitude of  $600 A_{rms}$  to flow through the shorted portion of the transformer winding and the tap switches. The supply current increases to  $28 A_{rms}$  to supply the power being dissipated in the shorted winding, the tap switches, the interconnecting wires and contact resistances. It can be seen that the auto-transformer winding and tap switches can survive this unlikely occurrence for multiple supply cycles without any visible effects of damage to the winding.



a) Test circuit diagram

b) Waveforms

**Figure 7-14: Tap winding shorted**

To investigate if the high circulating current in the transformer winding will not lead to an unacceptable high temperature rise in the winding, a more detailed investigation is performed.

Because the taps are distributed linearly along the high current portion of the tap winding, the resistance of the shorted portion of the tap winding is approximately a quarter of the total high current winding resistance (refer to Table 4-4) which equals 5.35 mΩ at 20 °C. The resulting  $I^2R$  power loss in this portion of the winding will thus be equal to 1926 W. To calculate the temperature rise in the winding Equation (4-13) can be used, repeated below for reference. This states that the temperature rise in the winding ( $\Delta T$ ) will be equal to the energy absorbed in the winding divided by the mass of the winding and the specific heat capacity of copper.

$$\Delta T = \frac{Pt}{mc}$$

**Where**

$\Delta T$  = Change in temperature (°C)

$m$  = Material mass (kg)

$c$  = Specific heat capacity ( $Jkg^{-1}^{\circ}C^{-1}$ )

$P$  = Power (W)

$t$  = time (s)

For a worst case scenario it will be assumed that during the tap short condition, all the energy will be absorbed into the copper winding and none of the absorbed energy will be conducted away from the portion of winding. By reference to the auto-transformer winding data in Table 4-3 the mass of the portion of copper winding can be calculated as 0.05 kg, assuming a copper

density of  $8.96 \text{ g/cm}^3$ . The temperature rise in the copper winding during a 10 ms period can now be calculated as:

$$\Delta T = \frac{Pt}{mc}$$

$$= 1 \text{ }^\circ\text{C}$$

**Where**

$$m = 0.05 \text{ kg}$$

$$c = 385 \text{ Jkg}^{-1}\text{ }^\circ\text{C}^{-1}$$

$$P = 1926 \text{ W}$$

$$t = 10 \text{ ms}$$

This verifies that the high circulating current will not cause any damage to the winding, during its brief existence. The temperature rise if this current were to flow for 1 second will be approximately  $100 \text{ }^\circ\text{C}$ , which would still not damage the windings.

### 7.1.8 Temperature measurements

All the temperature measurements were done using a HP34970A data acquisition unit made by HP / Agilent as shown in Figure 7-15. Type K thermocouples were used for all the measurements, done at 30 second intervals.



**Figure 7-15: HP34970A data acquisition unit**

Temperatures are recorded at various points within the EVR to verify the accuracy of the design. These points include:

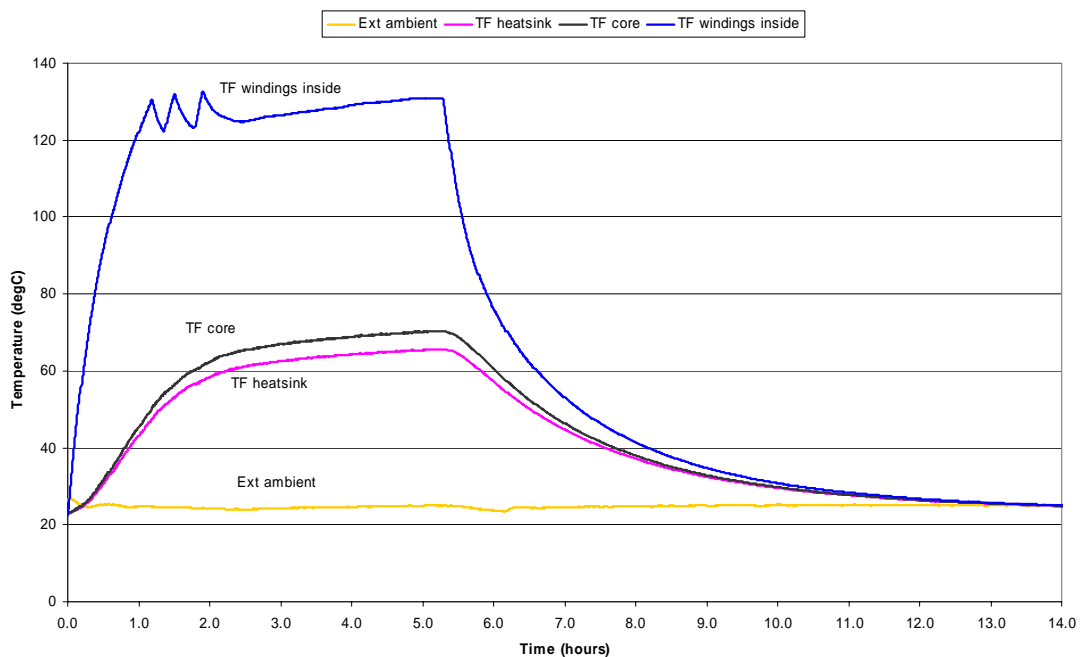
- Ext ambient                      Ambient temperature outside the EVR
- Int ambient                      Temperature inside the EVR enclosure
- TF heat sink                      Auto-transformer heat sink temperature

- TF core                      Auto-transformer outer core temperature
- TF windings inside        Auto-transformer inner winding temperature
- Thyristor heat sink        Temperature on thyristor heat sink

For the purpose of the tests, the EVR is operated at 10 kVA (200 % rated power) for a period of 5½ hours, where after it is switched off and the cooling down response is obtained. To generate the most losses, the supply voltage to the EVR is adjusted so that tap 4 is the active tap. During the measurements the external ambient temperature is approximately constant at 25 °C.

### 7.1.8.A Transformer temperature

In Figure 7-16 the transformer internal winding temperature together with the core, transformer heat sink and external ambient temperature is shown.



**Figure 7-16: Transformer temperature (25 °C ext ambient)**

By referring to Figure 7-16, the transformer winding, core and heat sink temperatures are discussed below.

## **Transformer winding temperature**

The internal transformer winding temperature rises rapidly from an initial value of 25 °C to 130 °C in approximately 60 minutes. At this point, the over temperature protection recognizes that the transformer temperature is too high, and the EVR goes into temperature limiting mode to protect the transformer windings. (Entering temperature limiting mode implies that the output voltage regulation control will be relaxed, to allow the usage of a tap setting that will lead to lower losses.)

Tap 4 is therefore turned off and tap 3 activated, which has a lower winding impedance and therefore less losses. In addition to this, tap 3 also provides less voltage boost, causing a reduction in output voltage and output power, which reduces the losses further. The winding temperature should therefore increase at a slower rate, or decrease, as is the case here.

After the temperature has decreased to 125 °C the temperature limiting mode is exited and tap 4 is activated once again, leading to higher losses and an increase in the winding temperature.

After 5½ hours the EVR is turned off, to obtain details of the cooling characteristic. As can be seen the transformer takes approximately 6 hours to cool down completely.

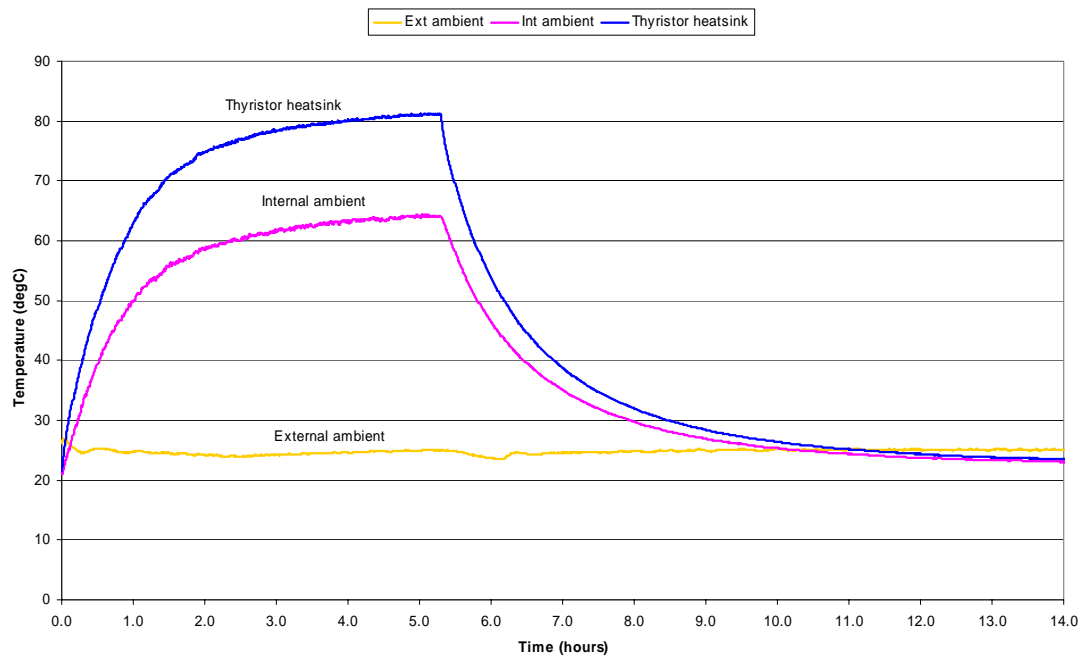
## **Transformer core / heat sink temperature**

A huge temperature differential exists between the transformer windings and core. This is due to the poor thermal coupling between the windings and the core caused by the physical construction of the transformer in which the windings are wound around a bobbin, which fits loosely over the transformer core.

A much closer resemblance can be seen between the core and heat sink temperature, due to better thermal coupling. The core and heat sink temperature reaches a value of 71 °C and 65 °C respectively after 5½ hours. The expected core temperature calculated in the enclosure design section is 98.5 °C with an external ambient temperature of 45 °C. This compares favorable with the measured value of 71 °C if the difference of 20 °C in ambient temperature is taken into account.

### **7.1.8.B Thyristor heat sink / internal ambient temperature**

Figure 7-17 shows the thyristor heat sink temperature together with the internal and external ambient temperatures.



**Figure 7-17: Thyristor heat sink temperature (25 °C ext ambient)**

### **Thyristor heat sink temperature**

The thyristor heat sink temperature increased steadily over a period of 5½ hours from 25 °C to 83 °C at which point the EVR was turned off. Comparing the heat sink temperature with the expected / calculated value of 107.5 °C (at an external ambient temperature of 45 °C) shows a favorable comparison if the 20 °C difference in the external temperature is taken into consideration.

### **Internal ambient temperature**

The internal temperature measured in the vicinity of the controller increased to 65 °C, which could lead to accelerated aging of the EVR components. As it is anticipated that the EVR will only be subjected to short periods of overload, mainly during morning and afternoon peak times, the high internal ambient temperature will not be present for long periods of time and the influence on the component lifetime should be lessened. Comparing the measured internal ambient temperature to the required maximum ambient temperature that was designed for (85 °C at an external ambient of 45 °C) reveal a good correspondence.



## 7.1.9 Power loss / efficiency

### 7.1.9.A Power analyzer

To verify the calculated losses in the EVR a “NORMA 5000” power analyzer (shown in Figure 7-18) is used. This is a high precision instrument with accuracy of 0.1 %, capable of measuring signals from DC to a few MHz.

Six isolated voltage and current channels are available for use. The voltage channels are capable of accepting a voltage up to 1000 V, while the current channels accepts either a current input up to 10 A or a voltage input up to 10 V. For the measurement of large currents external current sensors must be utilized. These can be CT's interfaced with the current input, or resistive shunts that interface with the voltage input of the current channel.



Figure 7-18: Norma 5000 power analyzer

For the power loss measurements two resistive shunts (for input and output current) rated at 60 A are used. To maintain high accuracy these shunts were calibrated with the power analyzer. For calibration a 10 A<sub>rms</sub> current signal is passed through the series connection of the shunt and the current sensor on one of the current channels of the power analyzer. The shunts voltage output is measured using another current channel and compared with the internal sensor's reading to calibrate it.

To obtain the worst case accuracy in the measured power, the effect of a worst case voltage and current accuracy is investigated.

---


$$P = V(\pm d\%)I(\pm d\%) \quad \text{Where} \quad (7-1)$$

Worst case – both channels has either a positive or negative accuracy of  $d\%$

$P = \text{Power (W)}$   
 $V = \text{Voltage (V)}$   
 $I = \text{Current (A)}$   
 $d = \text{Accuracy of voltage \& current measurement (\%)}$

$$\begin{aligned} P &= V(+d\%)I(+d\%) \\ &= V\left(1 + \frac{d}{100}\right)I\left(1 + \frac{d}{100}\right) \\ &= VI\left(1 + \frac{d}{100}\right)^2 \end{aligned}$$


---

Investigating the influence of the percentage of accuracy in the voltage and current ( $d\%$ ) to the percentage of accuracy in the calculated power ( $d_p\%$ ) give:

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$$P(\pm d_p) = VI\left(1 + \frac{d_p}{100}\right) \quad \text{Where} \quad (7-2)$$

Thus

$$\therefore VI\left(1 + \frac{d_p}{100}\right) = VI\left(1 + \frac{d}{100}\right)^2$$

$d_p = \text{Accuracy of power measurement (\%)}$   
 $d = \text{Accuracy of voltage \& current measurement (\%)}$

$$\begin{aligned} \therefore d_p &= \left[\left(1 + \frac{d}{100}\right)^2 - 1\right]100 \\ &= \frac{d^2}{100} + 2d \end{aligned}$$


---

With an accuracy of 0.1 % in the voltage and current measurements, the worst case accuracy of the power measurement is thus +0.2001 % or -0.1999%. On 5 kW this amounts to +10.005 W or -9.995W.

### 7.1.9.B Losses

To verify and minimize any error in the calibration of the shunts, the power loss is evaluated with the shunts connected to the input and output, and also with the shunts interchanged. The power loss measured at 5 kVA and 10 kVA with both shunt configurations is shown in Table 7-1.

During all the tests sufficient time is allowed for the system to reach its steady state operating temperature, to ensure that the copper losses at the higher operating temperatures are measured. The external ambient temperature during the measurements is approximately 20 °C.

**Table 7-1: Measured power loss** (External ambient = 20 °C)

	<b>Power loss</b>	
	<b>@ 5 kVA</b>	<b>@ 10 kVA</b>
Shunts on input and output	78 W	229 W
Shunts interchanged	75 W	223 W
<b>Average</b>	<b>76.5 W</b>	<b>226 W</b>

A small difference in the measured power loss is obtained through interchanging of the shunts. At the 5 kVA power level, the change in power loss after interchanging the shunts is 3 W, which is equal to an error of 0.06 %.

Comparing the measured losses with the calculated losses shown in Table 7-2 reveals a very good correspondence. At 5 kVA the error made in the estimation is 7.6 W, while at 10 kVA the error is 8.3 W. Noting that with the worst case accuracy in the power analyzers measurements, a deviation of 10 W can be expected at 5 kVA, the estimated losses are assumed to be accurate.

Furthermore, the measured losses are obtained with an external ambient temperature of 20 °C, while the calculated losses are obtained assuming an external ambient temperature of 45 °C. The difference in ambient temperature implies that the calculated losses will be slightly higher than the measured losses, due to higher winding / copper resistance at higher temperature.

**Table 7-2: Calculated power loss**

<b>Component</b>	<b>Power loss</b>	
	<b>@ 5 kVA</b>	<b>@ 10 kVA</b>
Auto-transformer - Core	20.2 W	20.2 W
Windings	22.1 W	99 W
Thyristors	22 W	45 W
Surge protection inductor	7.3 W	33.5 W
Electronics		
Power supply & controller	5 W (estimate)	5 W (estimate)
Wiring – Internal	1.6 W	7 W
External	5.9 W	24.6 W
<b>Total loss</b>	<b>84.1 W</b>	<b>234.3 W</b>

### **7.1.9.C Efficiency**

From the measured losses in Table 7-1 the efficiency of the EVR operating at 5 kVA and 10 kVA are calculated as 98.5 % and 97.8 % respectively.

## **7.2 Field results**

A number of EVR units were installed in field trials, mostly in Kwazulu-Natal and Eastern Cape. A picture of the first prototype installed in North West is shown in Figure 7-19. To install the EVR, it is hoisted up the pole using a rope and pulley system attached to the eyebolts on the back of the EVR. The unit is then strapped onto the pole using bandit straps. The input, output and neutral connections are made using IPC connectors. (For a complete reference on the installation procedure, refer to Appendix B.)



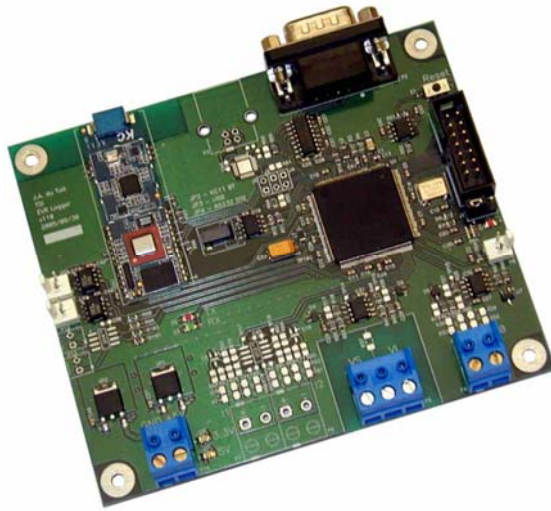
**Figure 7-19: EVR installation**

To monitor the performance of the EVR during field installations, a logger designed at the University of Stellenbosch is used to measure the relevant voltages and currents.

### **7.2.1 Data logger**

The data logger shown in Figure 7-20, is designed specifically for the EVR and measures and records the input and output voltages and input current of the EVR.

The data logger is equipped with 2 Mbyte of FLASH memory, to enable a large amount of data to be recorded. Each recorded measurement represents the RMS value of the parameter as accumulated over a period of 10 minutes. A real time clock with battery backup is used to time stamp all the recorded measurements. With 10 minute intervals between each recorded measurement, the logger is capable of storing data for more than a year before the FLASH memory's capacity is reached. To download the recorded information and clear the memory a Bluetooth link with a maximum range of 100 m is utilized.



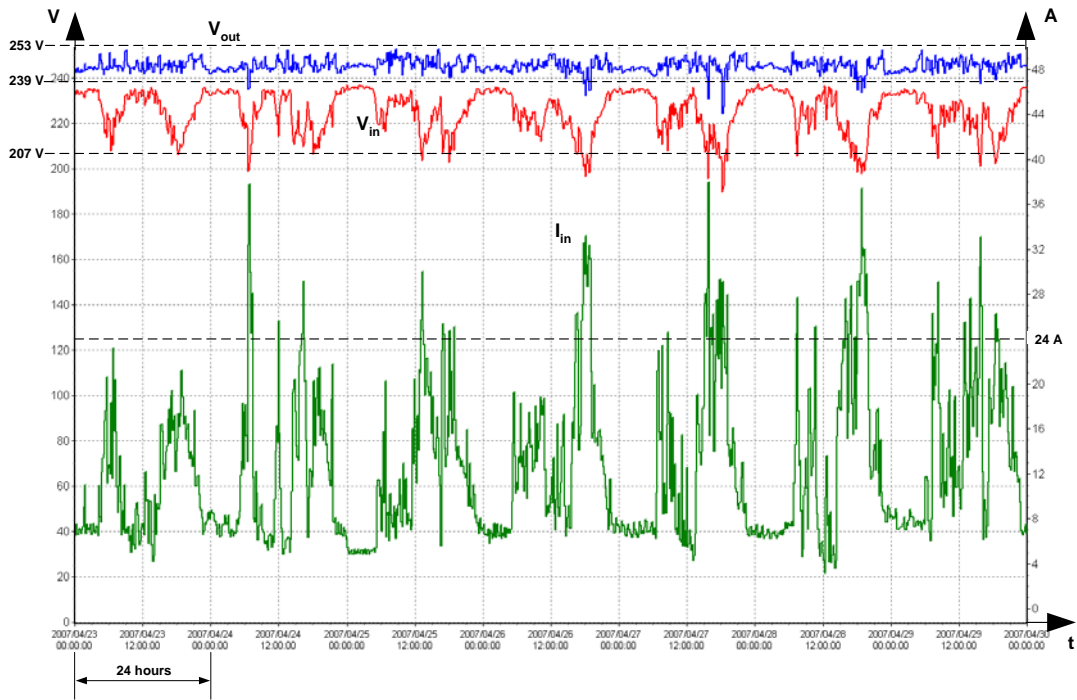
**Figure 7-20: EVR logger**

## 7.2.2 Results

A number of EVR units are installed in field trials. A typical result obtained from one of the field trials is shown in Figure 7-21 for a period of one week. This specific EVR is installed on one phase of a 32 kVA dual phase transformer equipped with 35 mm<sup>2</sup> ABC feeders. The EVR is located approximately 530 m downstream from the transformer and supplies 7 customers with electricity. The input / output voltages and the input current to the EVR are displayed as recorded over a period of one week.

The EVR is designed to boost an input voltage that varies between 230 V  $\pm$  10 % (207 V to 253 V) to an output that varies between 230 V + 4 % (239.2 V) and 230 V + 10 % (253 V). From the recorded  $V_{in}$  and  $V_{out}$  graphs it can be seen that the desired output voltage range is maintained as long as the input voltage remains above the minimum level of 207 V. Due to the 10 minute recording intervals used in the logger, the tap switching instants can unfortunately not be identified.

At a 5 kVA power level with an input voltage of 207 V, the EVR is rated for an input current of 24 A. From the  $I_{in}$  graph it can be seen that the EVR regularly exceeds the 24 A / 5 kVA level, normally during the morning and / or evening peak times when everybody is at home preparing meals. The duration of the time interval during which the 24 A level is exceeded varies between 30 minutes and 3 hours. The EVR never exceeds the 10 kVA (48 A) level, which would cause the EVR to turn off to protect itself against excessive overloading.



**Figure 7-21: EVR field results**

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# **Chapter 8**

## Conclusions

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## 8 Conclusions

This chapter gives a brief overview of the voltage regulator developed in this thesis. The performance of the device is discussed and comments regarding future improvements and the long term evaluation of the device are made.

### 8.1 Overview

The possibility of using a voltage regulator to provide cost savings in rural electrification projects through allowing extension of the LV feeder was outlined. Various types of voltage regulator topologies were evaluated to obtain the optimal solution for the specific application where reliability, maintenance free operation and low losses are the main criteria. The voltage regulator was designed and built and put through extensive tests to verify its operation. A number of field installations were completed successfully to illustrate the operation of the voltage regulator.

- **Hardware**

A detailed design of the power circuit was presented, together with comprehensive steady state power loss calculations for both the auto-transformer and thyristor tap switches. In addition, transient thermal analyses on the thyristor tap switches were performed to obtain their short time overload capabilities. To ensure robust and reliable operation in the field, careful attention was given to the surge voltage protection design and implementation. A complete but simplified approach to the thermal analyses and design of the enclosure was done to ensure that the EVR would perform to its maximum capability. To ensure seamless integration of the EVR with the existing LV network, detailed attention was given to the implementation of the coordinated protection scheme. This involved evaluation of a small network model to obtain the probable position of the EVR on the LV network to enable calculation of the expected fault current magnitudes.

- **Controller**

A digital signal processor based controller together with a suitable power supply was designed and constructed to enable control of the hardware. Various topologies to be used in the power supply were evaluated due to the high supply voltage requirement. A detailed design of the power supply was performed to ensure that it would remain operational over a large supply voltage input range. An innovative approach to obtain power during short circuit conditions was made, through using a current transformer as a power source and interfacing it with the power supply board. Extracts of relevant portions of the controller

circuit diagram were used to describe the implementation of various features of the controller, including the measurement circuitry and the thyristor drive circuits.

- **Software**

The development of the software code that controls the functionality and behaviour of the EVR was discussed. A brief overview of the function of each of the source files was given and a detailed description of the user configurable parameters, used to fine tune the behaviour of the EVR, was given. Using flow diagrams, the functioning of the most crucial parts of the program code was described.

## **8.2 Practical results**

Extensive tests were performed in a laboratory environment to verify that the electrical and thermal design does indeed function as required and to validate the operation of the software code. The practical tests illustrated / verified the following design concepts:

- Core saturation at turn on and how to prevent it in accordance with the theoretical description.
- Tap changing as applied to both resistive and inductive loads confirming that the control strategy implemented to prevent two tap switches from turning on simultaneously is working correctly.
- Operation of the EVR with and without the glitch suppressor circuit, used to remove voltage glitches from the output during thyristor commutation.
- The effect of fast and slow voltage regulation to understand the influence on the output voltage.
- Correct functioning of the coordinated protection scheme through short circuit tests.  
Ability of the CT to deliver the necessary control power during short circuits.  
Ability of the thyristors to turn off under high fault currents.
- Surge voltage withstand capability were confirmed by voltage impulse tests done at a local university on individual thyristors and complete EVR units.
- Ability of the transformer and thyristors to withstand the high circulating currents generated if two taps switches are turned on simultaneously, thereby short circuiting a portion of the transformer winding.
- Conformance with the theoretical thermal design.

- Regulation of the transformer temperature by relaxing the voltage regulation requirement to prevent an overloaded EVR from disconnecting the customers it supplies.
- Power loss measurements verify the theoretical loss calculations.
- Results obtained from field trials verify the correct operation of the voltage regulation capability of the EVR and prove that it is suitable for use on outdoor LV reticulation networks.

### **8.3 Conclusions**

The design objectives of this project as set out in section 1.3 have been reached and the following conclusions can be made:

- The topology best suited for the particular application has been selected.
- The required hardware / power circuitry was designed and constructed.
- The control circuitry was designed and constructed and integrated with the hardware.
- The software to control the device and implement all the features and protection requirements was developed, debugged and implemented.
- The entire system was tested and evaluated both in the laboratory and in the field. The system performed exceptionally well and fulfilled the design objectives.

### **8.4 Future work**

- **Data logger**

Improved communication between the EVR controller and the data logger and larger storage capability on the data logger could prove to be helpful in the future. Some technical issues with the current Bluetooth modules, causing them to stop functioning if frequent power interruptions are experienced, must also be resolved.

Due to the lack of a proper communication channel between the controller and data logger, no information on the tap settings and frequency of tap changes are available. This can be corrected either by redesigning both boards to include a proper communication channel, or integrating both the controller and data logger into one unit. Due to storage limitations, the data logger is only capable of storing a year's information at 10 minutes intervals. To obtain improved resolution, the storage capability either needs to be extended, or more frequent site visits needs to be performed to download the information.

- **Field evaluation**

A long term evaluation of the field performance of the EVR needs to be performed, both from a technical point of view and the end customer's perception of the performance of the device. This entails field visits every six months to download the recorded voltage / current profiles and error logs stored inside the data logger. These logs should be evaluated to identify any potential problems in the performance of the EVR. A customer survey also needs to be completed to ascertain that they experience an improvement in the quality of the supply. For rural communities this would most probable be an improvement in the lighting intensity during peak times and faster cooking times. It should also be confirmed that the step voltage control implementation does not lead to a noticeable / disturbing voltage flicker, especially visible in lighting fixtures.

- **Power rating**

Based on the field results obtained, a detailed study must be done in identifying the optimal power rating / tap settings for the EVR and the number of customers that can be connected to the EVR. Attention must also be given to the impact of future load growth on the performance of the EVR. If the load growth exceeds the power capability of the EVR, the EVR will disconnect the load to protect itself. Because this will most frequently occur during morning and evening peak times it could lead to annoyance and frustration amongst the customers, damaging the perception of the EVR.

Correcting an overloaded EVR installation entails one of the following options, each involving considerable manual labour, which should therefore be avoided through proper initial planning:

- Removal of the EVR to a location further downstream. This would unfortunately leave some of the upstream customers with a supply that does not conform to the minimum voltage requirement.
- Adding another ABC bundle in parallel with the existing bundle on the opposite side of the pole together with an additional EVR.
- Replacing the EVR with a higher capacity model.

- **Reliability**

Through data obtained from the field trials, the reliability of the device must be evaluated to ascertain its economic viability.

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# **Appendix A**

Tap positions

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## A EVR Tap positions

The parameters used in the calculation of the tap position are shown in Table A-1. The required tap positions are indicated at the end of the table.

**Table A-1: Tap position calculations**

Line based EVR					
			=User adjustable parameters		
<b>Parameters</b>					
<b>Vsupply</b>					
nom	230				
min	207.0	= $V_{sup\ nom} -$	10	%	
max	253.0	= $V_{sup\ nom} +$	10	%	
<b>Vout</b>					
min	239.2	= $V_{sup\ nom} +$	4	%	
max	253.0	= $V_{sup\ max}$			
<b>Taps</b>	5	<i>(Includes nominal tap)</i>			
<b>Tap size</b>	4.45	<i>%(Based on nominal supply voltage)</i>			
<b>Transformer</b>					
TF impedance	1.5				
Tap number		0	1	2	3 4
Tap impedance %		0.00	0.38	0.75	1.13 1.50
Tap position		253.0	242.8	232.5	222.3 212.1

Based on the tap positions above, a table evaluating the output voltage with a varying supply voltage can be constructed. Table A-2 shows the active tap for a given supply voltage magnitude and the amount of voltage overlap that will exist between taps - for output loading of both 0 % and 100 % of rated current.

**Table A-2: Output voltage**

<b>(a) Load 0%</b>						<b>(b) Load 100%</b>					
<b>Vsup</b>	<b>Vout - @ TAP#</b>					<b>Vsup</b>	<b>Vout - @ TAP#</b>				
	<b>0</b>	<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>		<b>0</b>	<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>
253.0	253.0					253.0	253.0				
252	252.0					252	252.0				
251	251.0					251	251.0				
250	250.0					250	250.0				
249	249.0					249	249.0				
248	248.0					248	248.0				
247	247.0					247	247.0				
246	246.0					246	246.0				
245	245.0					245	245.0				
244	244.0					244	244.0				
243	243.0					243	243.0	252.3			
242	242.0	252.2				242	242.0	251.3			
241	241.0	251.2				241	241.0	250.2			
240	240.0	250.1				240	240.0	249.2			
239		249.1				239		248.1			
238		248.0				238		247.1			
237		247.0				237		246.1			
236		245.9				236		245.0			
235		244.9				235		244.0			
234		243.9				234		243.0	252.7		
233		242.8				233		241.9	251.6		
232		241.8	252.4			232		240.9	250.5		
231		240.7	251.3			231		239.8	249.5		
230		239.7	250.2			230			248.4		
229			249.2			229			247.3		
228			248.1			228			246.2		
227			247.0			227			245.1		
226			245.9			226			244.1		
225			244.8			225			243.0		
224			243.7			224			241.9	252.1	
223			242.6			223			240.8	250.9	
222			241.5	252.7		222			239.7	249.8	
221			240.5	251.5		221				248.7	
220			239.4	250.4		220				247.6	
219				249.2		219				246.4	
218				248.1		218				245.3	
217				247.0		217				244.2	
216				245.8		216				243.1	
215				244.7		215				241.9	252.7
214				243.6		214				240.8	251.5
213				242.4		213				239.7	250.3
212				241.3	252.9	212					249.1
211				240.1	251.7	211					248.0
210					250.5	210					246.8
209					249.3	209					245.6
208					248.2	208					244.4
207					247.0	207					243.3

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## **Appendix B**

### EVR installation guide

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## **B EVR installation guide**

### **Transport and Unpacking**

Each EVR is delivered to the depot inside a special chipboard container. Always transport the unit enclosed in this container to protect it from damage. Open the lid by unfastening four Philips-head screws. To avoid electrical shock or equipment damage, do not open the EVR enclosure. Unpack the two Bandit straps with fittings for pole mounting. The EVR is equipped with three black fly leads each marked with an identification cable tie.

### **Marking**

The three fly leads are marked as follows:

---

<b>Identification</b>	<b>Description</b>
1 Input	Refers to the lead that is connected to the unregulated side of the network supplied from the transformer or another source.
2 Output	Refers to the lead that is connected to the regulated side of the network that supplies the load further down the network.
3 Neutral	Refers to the lead that is connected to the neutral of the network and is common to the input and the output.

---

### **Tools and working procedures**

Standard tools and safe working procedures used by field services personnel is required for the installation of the EVR. The applicable tools are:

<b>Description</b>	
1	Phillips screwdriver
2	Cable cutter
3	Ladder
4	Lever hoist
5	13-mm tube spanner with T-bar or a 6-sided (hexagon) socket to be used with a ratchet
6	Double leg sling
7	Bandit strap tool
8	Harness and protective clothing

## **Fittings**

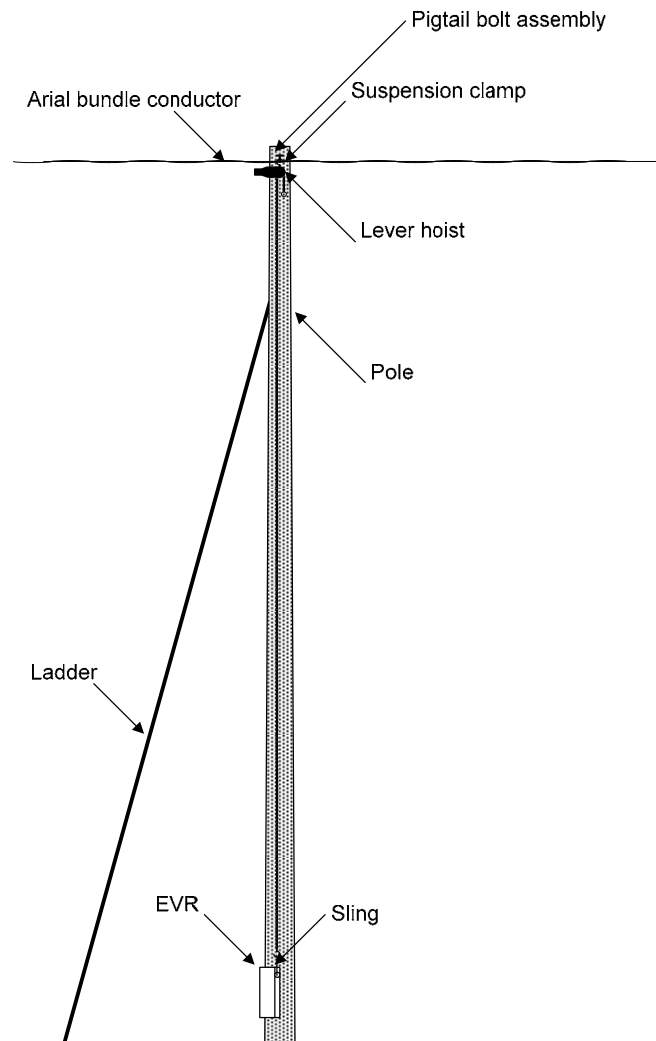
The fittings required for the installation of the EVR shall meet the requirements of the Eskom standard for fittings for aerial bundled conductors [1]. The fittings required per EVR installation are:

<b>Description</b>	<b>NSN</b>	<b>STD DWG SPEC D-DT--</b>
1 IPC 35-95/IPC 6-25 (BLACK) ABC INS PHASE/SERVICE INS PHASE	5935-70-009-6936	3039 SH1 NRS018-5
2 PG 35-50/IPC 6-25 (BLUE) BARE NEUT (PG)/SERV (IPC)	5935-70-010-0246	3039 SH3 NRS018-5
3 LOOSE END CAP 35-95 MM <sup>2</sup>	5975-70-007-7452	3079 NRS018-5
4 CABLE TIE 9 X 270	5975-70-009-2555	3075 NRS020

## **Mounting**

To limit supply interruption time it is recommended that the EVR is mounted to the pole prior opening the feeder links while maintaining low voltage live work practices [2]. The EVR shall

be installed with a minimum clearance of 3 m to ground as stated in the low voltage reticulation standard [3]. Since the mass of the EVR is 32 kg, a lever hoist hooked to the pigtail bolt assembly should be used to lift the EVR and keep it in position while strapping it to the pole as depicted in Figure B-1.

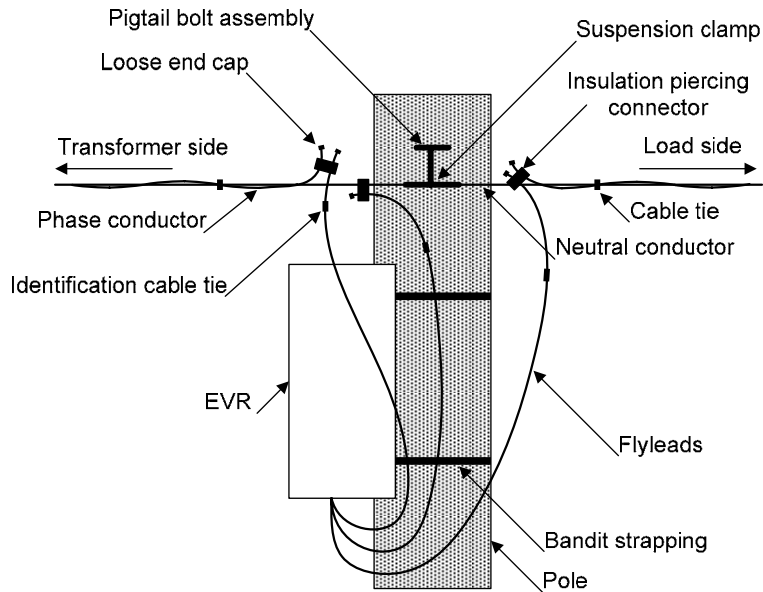


**Figure B-1: Arrangement for lifting the EVR to its position on the pole**

## Connections

After mounting of the EVR on the pole, the feeder link should be opened at the transformer for the safe connection of the cables. Figure B-2 shows the connection diagram of the EVR.

The phase conductor is strapped to the neutral conductor on the transformer side and load side of the pole before it is cut. The fly lead marked “Input” is connected to the transformer side of the network, the fly lead marked “Neutral” is connected to the neutral conductor and the fly lead marked “Output” is connected to the load side of the network. The appropriate insulation piercing connectors (IPC) are used for this purpose.



**Figure B-2: EVR connection diagram**

The following practices should be followed when connecting up the EVR [4]:

- IPCs shall be spaced in the following manner:
  1. The distance between any two phase IPCs shall be spaced between 200 mm and 300 mm.
  2. The neutral IPCs should be positioned closest to the pole and then the phase IPCs shall follow.
- All IPCs shall be positioned in such a manner that the tightening bolt is in a vertical position, with the torque-shear nut on top. This ensures that the grease, enhancing water-tightness, does not run out.
- As far as is practically possible the ABC bare neutral conductor should be positioned in such a way that it does not lie adjacent to the mouth of the phase IPC.
- Cable Ties are applied in the following manner:
  1. The EVR neutral cable shall not be cable tied to the ABC.
  2. Phase service distribution box cables shall be cable tied, to that specific ABC phase conductor to which it is connected, only. These cable ties shall be positioned in the centre point between adjacent phase IPCs.
  3. No cable ties shall be allowed between the two neutral IPCs.

4. Cable ties around all phases and neutral conductors of the ABC shall only be used after the last IPC; at a distance of  $\geq 300$ mm away from the last IPC.
- During installation of IPCs it shall be ensured that the IPC is held securely in order to prevent it from twisting. A standard 24-sided 13 mm ring spanner shall not be used, but a 13-mm tube spanner with T-bar or a 6-sided (hexagon) socket, to be used with a ratchet shall be used.

## References

- [1] Eskom SCSSCAAL4:1997, *Fittings for bare neutral aerial bundled conductor*.
- [2] Eskom SCSPVABL7:2001, *Low voltage live work: livening up a pole-mounted service box*.
- [3] Eskom SCSASAAM2:1998, *Distribution standard: Low voltage reticulation-LV overhead reticulation*.
- [4] J. Maudu, "Review of current practices on low voltage ABC networks," in *Distribution technical bulletin*, vol. 00TB-036, 2005.