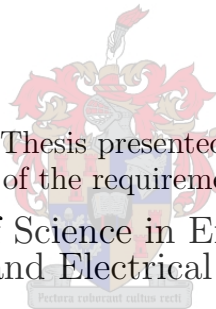


# Design and Implementation of a Modular Converter with Application to a Solid State Transformer

by

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# Declaration

By submitting this dissertation electronically, I declare that the entirety of the work contained therein is my own, original work, that I am the owner of the copyright thereof (unless to the extent explicitly otherwise stated) and that I have not previously in its entirety or in part submitted it for obtaining any qualification.

December 2009

# Abstract

The purpose of a solid state transformer (SST) is to use power electronic converters to mimic the operation of the conventional distribution transformer. These power electronic converters are proposed to overcome the disadvantages of the conventional distribution transformer. The advantages of a SST include near perfect voltage regulation and harmonic isolation between the primary and secondary windings of the transformer.

This thesis discusses the design and development of the different converters in a solid state transformer (SST). A prototype modular back-to-back converter is developed for the input and isolation stage of the SST. The isolation stage consists of a high voltage DC-DC converter, which transfers power across the isolation barrier of the SST. This stage is evaluated in the laboratory with special attention being paid to the efficiency of the converter.

The second aspect that this thesis addresses is the output stage of the SST, namely a three phase inverter. The discussion of the output stage focuses on the losses occurring in the inverter. The switching device losses are calculated by means of an adapted numerical method as opposed to using conventional analytical methods. The presented numerical method is compared to the existing analytical method and the findings are discussed.

A double loop control strategy is implemented for the output stage inverter. The inner current loop utilizes a predictive control strategy. The control analysis of the double loop controller is discussed and evaluated in the laboratory. All the converters that are discussed in this thesis are evaluated in the laboratory and the relevant measurements are included.

# Opsomming

Die doel van 'n drywingselektroniese transformator (DET) is om drywingselektroniese omsetters te gebruik om die werking van die konvensionele distribusietransformator na te boots. Hierdie drywingselektroniese omsetters word voorgestel ten einde die nadele van die konvensionele distribusietransformator te bowe te kom. Die voordele van 'n DET sluit in: feitlik perfekte regulering van spanning en harmoniese isolasie tussen die primêre en sekondêre windings van die transformator.

Hierdie tesis bespreek die ontwerp en ontwikkeling van die verskillende omsetters in 'n drywingselektroniese transformator (DET). 'n Prototipe modulêre rug-aan-rug-omsetter word ontwikkel vir die intree- en isolasiefase van die DET. Die isolasiefase bestaan uit 'n hoogspanning-GS-GS omsetter, wat drywing oor die isolasiegrens van die DET heen oordra. Hierdie omsetter word in die laboratorium geëvalueer met besondere aandag aan die doeltreffendheid van die omsetter.

Die tweede aspek waarna in hierdie tesis gekyk word, is die uittreefase van die DET, naamlik 'n driefaseomsetter. Die bespreking van die uittreefase fokus egter op die verliese wat in die omsetter voorkom. Die verliese van die skakelaars word bereken deur middel van 'n aangepaste numeriese metode teenoor die gebruik van konvensionele analitiese metodes. Die numeriese metode wat aangebied word, word vergelyk met die bestaande analitiese metode en die bevindings word bespreek.

'n Dubbellus-beheerstrategie word vir die uittreefase-omsetter geïmplementeer. Die binneste stroomlus word geïmplementeer deur van 'n voorspelbare beheerstrategie gebruik te maak. Die beheeranalise van die dubbellusbeheerder word bespreek en in die laboratorium geëvalueer. Al die omsetters wat in hierdie tesis bespreek word, word in die laboratorium geëvalueer en die relevante metings word ingesluit.

# List of Publications

- **SAUPEC 2008**

- **A Low Computational Double-Loop Control Strategy for DC-AC Inverters**

- In this paper an average current mode control method is presented. The control method is based on the change in inductor ripple over the different states of operation. The controller developed forms the inner loop of a double loop control strategy. The current controller is rigorously tested and implemented in a DC-AC inverter. Emphasis is placed on the low computational requirements of the control method.

- **IEEE AFRICON 2009**

- **An Investigation of Switching and Conduction Losses in Inverters Under Varying Inductor Ripple Current**

- This paper presents an accurate method of calculating the switching device losses in a half bridge DC-AC inverter. The analysis is based on an existing numerical method of calculating the inductor ripple current. The losses are calculated by replicating the exact current waveform flowing through the switching devices. This method allows for a more accurate loss calculation compared to the well known existing analytical methods. The different methods are discussed and the results are compared.

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# Nomenclature

AC	- Alternating Current
ADC	- Analogue to Digital Converter
DC	- Direct Current
DEPWM	- Double Edge Pulse Width Modulation
DSP	- Digital Signal Processor
EMI	- Electro Magnetic Interference
ESR	- Equivalent Series Resistance
FFT	- Fast Fourier Transform
FPGA	- Field Programmable Gate Array
GPIO	- General Purpose Input Output
IGBT	- Insulated Gate Bi-Polar Transistor
LPF	- Low Pass Filter
MV	- Medium Voltage
OVS	- Over Voltage Snubber
p.u.	- Per Unit
PCB	- Printed Circuit Board
PWM	- Pulse Width Modulation
rms	- Root Mean Square
SEPWM	- Single Edge Pulse Width Modulation
SST	- Solid State Transformer
THD	- Total Harmonic Distortion
ZVS	- Zero Voltage Switching
ZCS	- Zero Current Switching



# Chapter 1

## Introduction

The purpose of the entire process from generation to distribution is to provide power to paying customers. The quality of supply is therefore defined from a customer perspective. This definition follows from [14], which refers to “Any power problem manifested in voltage, current or frequency deviations that result in failure or mis-operation of customer equipment”. Thus, it is the utility, which is responsible for maintaining the quality of supply. This is done by adding active and passive components into the network. Examples of these components are voltage regulators, harmonic filters and solid state tap-changers. The network therefore consists of multiple additional components, which improve the quality of supply.

Conventional distribution transformers are reliable and efficient devices. These transformers do, however, have disadvantages, such as non-perfect voltage regulation and high inrush currents. Nonetheless, the transformer in general is not responsible for power quality degradation. The main disadvantage of transformers in the network is that disturbances propagate directly through the transformer. For example, a dip on the primary voltage is reflected to the secondary voltage of the transformer. Harmonics drawn on the secondary of the transformer are also reflected to the primary. A method or device that would prevent these disturbances from crossing the isolation barrier of a transformer would offer great benefits to the network.

Research is currently under way to develop such a component, namely the solid state transformer (SST). The concept of a SST is illustrated in Figure 1.1. The purpose of the SST is to mimic a conventional distribution transformer and to improve the power quality of the supply. Active converters are used on the primary and secondary of the SST, thus it is possible to improve the power quality of the supply. The SST is therefore proposed to replace voltage regulators, tap changers and conventional components of improving power quality.

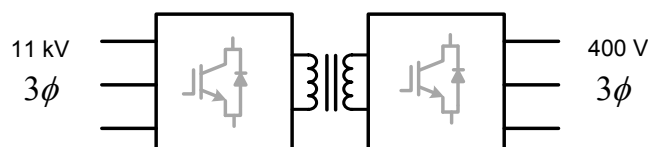


Figure 1.1: Solid state transformer

The advantages of the SST therefore include near perfect voltage regulation of the secondary voltage, and harmonic isolation between the primary and secondary windings. Other advantages include short circuit protection and the fact that a short circuit on the secondary of the SST is not reflected to the primary, as opposed to what happens in conventional transformers. Dip compensation can also be achieved in the SST by using a form of energy storage in the output stage of the SST. The SST can also adapt to different primary and secondary supply frequencies, for example 50 Hz on the primary and 60 Hz on the secondary of the SST.

The SST does however have many disadvantages, such as cost, size and reliability. The SST is presently in the research stage and has not been successfully operated at distribution voltage levels. The main obstacle encountered in implementing the SST concept is the high primary voltage that the input converters are required to withstand. Semiconductors that can operate at these voltage ratings are not available, hence multilevel converters are required for the input stage of the SST.

The series stacked SST is chosen for the prototype [2], because this converter uses modular cells that divide the high primary voltage equally among the cells. A cell is defined as a modular back-to-back converter consisting of an active rectifier and an isolation stage. The isolation stage utilizes a high voltage DC-DC converter to transfer power across the isolation transformer of the cell. The proposed frequency of this converter is required to be between 25 kHz and 50 kHz, which is necessary to reduce the size of the transformer. The output stage of the SST consists of an actively controlled three phase DC-AC inverter. This stage therefore provides the sinusoidal output voltage which is connected to the load.

The design and implementation of the modular cell as well as of the output stage of the SST are discussed in this thesis. The next section briefly describes the objectives of the thesis.

## 1.1 Thesis Objectives

The first objective of this thesis is to design and build a prototype of the modular cell. The modular cell is required to have an active rectifier, as well as a full bridge DC-DC converter. Laboratory evaluations of the DC-DC converter are required at the rated specifications of the series stacked converter. The requirements of the modular cell are:

- To research possible topologies that could be used for the modular cell.
- To design the modular cell.
- To evaluate the DC-DC converter at the rated specifications of the series stacked converter.
- To prove the concept of the series stacked converter by stacking the modular cells in series.

The second objective of this thesis is to design and implement the output stage of the SST, namely a three phase inverter. The following objectives are required for the output stage of the SST:

- To analyze extensively the losses occurring in the inverter.

- To design the inverter based on the loss analysis.
- To research possible control strategies that could be used for the inverter.
- To implement the chosen control strategy and evaluate the method.

## 1.2 Thesis Outline

This section gives a brief overview regarding the chapters in this thesis.

**Chapter 2** discusses the relevant literature regarding conventional distribution transformers. The advantages and disadvantages of these transformers are discussed and the SST is introduced as a solution to improving the power quality of the supply. The advantages and disadvantages of the SST are highlighted and the possible topologies of implementing a SST are discussed. The existing SST prototypes found in the literature are mentioned. The relevant research regarding the chosen SST is also included.

**Chapter 3** describes the operation of the chosen SST, namely the series stacked converter. The specifications of the modular cell are defined and the relevant stages of the back-to-back converter are discussed. A step by step design of the back-to-back converter is presented. This chapter describes the power circuit as well as the auxiliary circuits of the back-to-back converter. The mechanical construction of the cell is also explained with regard to the high voltages present in the cell.

**Chapter 4** discusses the DC-DC converter, which is used in the isolation stage of the modular cell. The topologies of the DC-DC converter are discussed and the phase shifted full bridge converter is chosen for the converter. The converter operation is described in depth with special attention being paid to the soft switching transitions. The operation of the secondary rectifier is described, with an emphasis on the diode ringing voltage. The description of the snubber circuit is also included.

**Chapter 5** focuses on the design of the three phase inverter, with emphasis on the losses occurring in the inverter. This chapter presents an alternative method of calculating the switching device losses in a half bridge inverter, using an existing inductor current model. This method takes into account the inductor ripple current, unlike other methods in the literature. The presented numerical method is compared to the existing analytical method and the findings are discussed.

**Chapter 6** focuses on the control strategy of the three phase inverter. The control method is based on a double loop control strategy. The inner loop control strategy is based on an existing control method used in a full bridge converter. This method is extended to a half bridge converter and the relevant control analysis is discussed. A comparison is included using different sampling times and carrier waveforms to achieve a faster transient response. The design of the outer voltage loop is included and implemented in the double loop control strategy.

**Chapter 7** evaluates the DC-DC converter of the modular cell, highlighting the advantages and shortcomings of the first prototype. This chapter discusses the voltage overshoot occurring across the IGBTs as well as a method of reducing this overshoot. The efficiency of the DC-

DC converter is calculated and compared to the measured efficiency. The concept of the series stacked SST is partially proven in this chapter, by connecting two modular cells in series. The balancing mechanism occurring in the series stacked converter is also discussed.

## Chapter 2

# Literature Review

### 2.1 The Transformer

Thomas Edison presented major breakthroughs in the previous century with respect to the electrical world; for example, Edison invented the light bulb in 1878 and then later Edison's famous Pearl Street Station was built in 1882 [15]. Pearl Street Station was situated in New York and used steam engines to power dynamos. This station eventually supplied lighting to 59 customers, a demonstration of a distribution system using direct current (DC). The implementation of this DC distribution method grew at a rapid pace, although problems began to arise due to the large voltage drop that occurred along the transmission lines.

In 1886, William Stanley used a transformer to demonstrate the more practical alternating current (AC) transmission system, as we know it today. He did this by transmitting power across a distance of 4 000 feet, by first stepping up the voltage to 3 000 V and then down again to 500 V. This stepped down voltage was then suitable for residential applications [1].

The early networks operated at various frequencies ranging from 25-60 Hz; the Americans eventually stabilized at 60 Hz and the Europeans at 50 Hz. The main advantage of the 60 Hz system was that the transformers and rotating machines were smaller than the ones with the same rating in the 50 Hz system. The main advantage of the 50 Hz system was that the transformers and transmission lines had smaller reactances than the corresponding 60 Hz system.

The invention of the transformer later became the basis for moving away from DC reticulation systems, due to the high transmission losses occurring at low voltage transmission. Today electricity is transmitted over thousands of kilometres, and this is commercially viable due to the high voltage used in AC transmission systems. The AC transmission voltages also increased gradually from 132 kV to 400 kV. Presently AC transmission voltages are in excess of 765 kV.

After moving along the transmission line, the transmission voltages are stepped down and supplied to a wide variety of loads. These transmission voltages are further stepped down and then classified as distribution voltages. Distribution transformers then step down these distribution voltages to the even lower voltages that are required for residential loads. In this way, the transformer has become an integral part of the power network.

## 2.2 Distribution Transformers

A transformer is a static device that consists of two or more magnetically coupled coils, and it transfers power from one coil to another, usually at different voltages and currents. Distribution transformers are power transformers with power ratings between 25 kVA and 1250 kVA. These transformers are used to supply a whole network of residential loads or perhaps even a small industrial load. According to the South African standards concerning distribution transformers, namely the SANS780, a distribution transformer is classified as a transformer with a maximum voltage that does not exceed 36 kV [12]. However, typical distribution voltages in South Africa are 11 kV and 22 kV.

Distribution transformers can be either a dry type or the windings can be submerged in mineral oil. Dry type transformers are used for relatively small loads and where cost is a factor. The commonly used oil filled distribution transformer uses mineral oil for cooling and for insulation between the windings. Natural convection of the oil is used to cool distribution transformers depending on their power ratings.

Distribution transformers are usually designed to work at 200% overload for several hours, and have a life expectancy of up to 40 years. Distribution transformers between 15 kVA and 100 kVA are either pole mounted, or placed in a minisub on the ground. A photo of a 50 kVA pole mounted distribution transformer is shown in Figure 2.1 [13]. A 100 kVA transformer can supply between 8 and 15 residential loads depending on the social economic area. These transformers have a minimum protection of primary fuses. The information in this section was obtained from [1; 15]



Figure 2.1: 50 kVA three phase pole-mounted distribution transformer

### 2.2.1 Transformer Model

There are three main categories of losses in a transformer, namely copper losses, hysteresis and eddy current losses. Copper losses are the losses occurring in the windings, namely the  $I^2R$  loss. Hysteresis losses are caused by the energy required to magnetize the core first in one direction

and then in the other, due to the periodic reversal of the primary voltage. Lastly, eddy current losses are caused by induced currents that flow in the core due to the magnetic fields present.

An equivalent circuit diagram of the transformer is shown in Figure 2.2; this model is widely used and is based on the losses occurring in the transformer. The series resistances  $r_1$  and  $r_2$  are the resistances of the respective windings, these resistances reflect the copper losses of the transformer. The impedances  $x_1$  and  $x_2$  are defined as the leakage reactances, and they represent the loss in flux linkage between the primary and secondary windings. The parallel resistance  $R_m$  represents the eddy current and hysteresis losses. The parallel reactance  $X_m$  reflects the magnetization current that flows through the transformer.

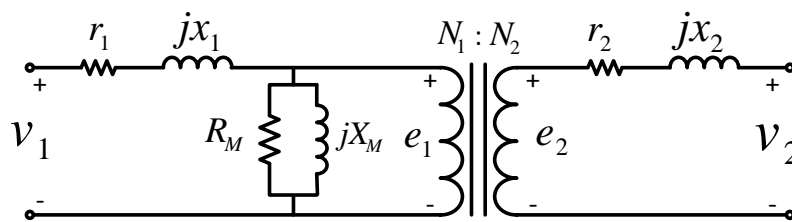


Figure 2.2: Transformer equivalent circuit

For larger power transformers the core and winding losses are much smaller than the effect of the leakage inductances. For this reason, a simplified network model is usually used with a single leakage reactance, which takes into account the primary and secondary flux losses. However, for smaller distribution transformers these losses are not negligible, and the full equivalent circuit is generally used. The information in this section was obtained from [1; 15].

### 2.2.2 Disadvantages of the Distribution Transformer

In general transformers are reliable and efficient devices. A well-designed transformer can obtain an efficiency of greater than 98%, making it one of the most efficient electrical devices ever invented. The transformer does however have disadvantages, such as voltage regulation and high inrush currents. Spectral distortion of the transformer output voltage is also caused by the non-linear magnetization current that flows in the primary. These disadvantages are briefly discussed below.

#### Voltage Regulation

As expected, transformers in general do not have perfect voltage regulation, and thus, depending on the size of the load, the secondary voltage fluctuates. This has a significant impact on the power quality of the network. Tap changers are therefore used to keep the voltage within the tolerance stipulated by the national standards (NRS-048).

A tap changer is an electro-mechanical switch that is built into the primary of the transformer. This device either adds or removes windings of the primary, which in effect alters the turns ratio of the transformer. Currently, tap changers are available in manual or automatic

versions to control the output voltage. However, research is underway to develop solid state tap changers, which use instantaneous voltage control [16]. These tap changers are proposed to adjust the secondary voltage by  $\pm 5\%$ .

### Inrush Currents

When a transformer is energized an inrush current of approximately 16 p.u. flows in the primary; this current is the initial magnetization current of the transformer [1]. The core generally saturates, which causes these large inrush currents. This inrush current is caused by the reactances of the transformer being abnormally small, as the transformer core saturates. The components in the network are therefore designed to withstand these initial inrush currents.

### Spectral Distortion

The B-H curve is relatively linear near the origin, but it becomes non-linear at higher values of magnetic flux density B and magnetic field strength H. Transformers are designed to fully utilize the B-H curve to minimize the amount of core material, thus the non-linear properties of the core are inevitable.

The flux  $\phi$  in the core lags the primary voltage by  $90^\circ$ ; the magnetization current  $i_m$  therefore becomes non-linear to force a sinusoidal flux  $\phi$  in the core. This is due to the non-linearity of the B-H curve; this concept is illustrated in Figure 2.3. The magnetization current  $i_m$  is shown to be rich in harmonics and this can distort the output voltage of the transformer. This effect is very small however, as the magnetization current  $i_m$  is between 1% and 5% of the full load current. The information in this section was obtained from [1].

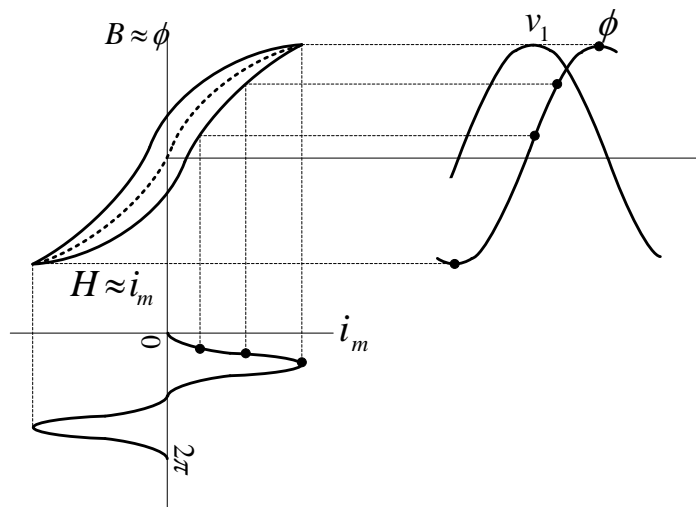


Figure 2.3: Non-linear magnetization current taken from [1]



## 2.3 Power Quality

The purpose of the entire process from generation to distribution is to provide power to paying customers, and therefore the customer has the most say with respect to power quality. The definition of power quality is thus defined from a customer perspective. The definition follows from [14] and refers to “any power problem manifested in voltage, current or frequency deviations that results in failure or mis-operation of customer equipment”. The main factors that deteriorate power quality in a network are listed below from [14; 17]:

- Harmonics
- Over voltages
- Voltage swell
- Voltage surges
- Network transients
- Flicker
- Long-term interruptions

These factors and their allowable tolerances stipulated by the NRS-048 are discussed in Appendix D.

A significant amount of research is currently under way to improve the quality of the electricity supply. Additional components are being added into the network to improve the quality of supply. These components may be active or passive components, such as harmonic filters, power factor correction devices and solid state tap changers. These components are added into the network depending on the sensitivity of the load.

The adverse effect of the non-linear magnetization current that is drawn by the primary of the conventional transformer is relatively small. The magnetization current only accounts for a small percentage of the full load current. The voltage regulation is improved with the use of tap-changers, thus the voltage regulation is not of a major concern. The protection devices in the network also take into account the large inrush current of the transformer. Thus the current distribution transformer is not responsible for major power quality degradation.

The transformer does however allow these occurrences to propagate directly through it. For example, should a dip occur on the primary of the transformer, the secondary will also reflect this. Another example of this is that if a specific load is drawing a large number of harmonics, these harmonics are directly applied to the network through the transformer. The main disadvantage of the transformer is therefore that these disturbances propagate directly across the isolation barrier of the transformer.

Research is currently under way to implement all of these additional components, which will improve the power quality of the network, by consolidating them into one component, namely the Solid State Transformer (SST). Thus, in the future it is proposed that the SST will

take the place of active filters, tap changers and power factor correction devices. One of the main advantages of the SST is that the power qualities on the primary and secondary of the transformer are independent of each other. A form of energy storage is thus required in the SST. Consequently, the improvement of power quality using a SST has opened up a large field of research.

## 2.4 Introduction to the Solid State Transformer

The SST is a device that mimics the standard operation of the distribution transformer using semiconductors. The principle of the SST is therefore to transform high voltage AC to low voltage AC, for example, 11 kV to 400 V. Figure 2.4 depicts the concept of the SST. Switching converters are placed on both sides of the isolation barrier, with the primary and secondary network voltages remaining unchanged.

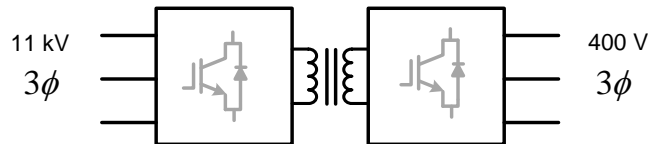


Figure 2.4: Concept of the SST

The SST consists of multiple back-to-back converters depending on the topology. Three main converters are required in the SST, namely an input stage converter, isolation stage converter and an output stage converter. The input stage comprises an active rectifier, which controls the primary current. This stage forces the input current to be sinusoidal, regardless of the secondary current. The isolation stage consists of a DC-DC converter, which transfers power across the isolation barrier. The output converter consists of a three phase DC-AC inverter, thus the three output voltages are instantaneously controlled. Energy storage is also added to the bus capacitance of the output stage. This is done to obtain dip compensation and to prevent harmonics from propagating through the SST.

The isolation stage of the SST converts power across the isolation barrier at a much higher frequency than the fundamental of 50 Hz. Thus, by increasing the switching frequency, the volt-time integral of the transformer is reduced which results in a smaller transformer core. Depending on the topology of the SST, either a single transformer or multiple smaller transformers are utilized. The goal is that these transformers use natural cooling, without submerging the transformer in oil. These transformers are smaller but the entire SST will by no means be smaller than the conventional distribution transformer. This is due to the additional components such as heatsinks, bus capacitors and a large number of printed circuit boards. The maximum allowable sizes and the costs of conventional transformers are shown in Table 2-I. A photograph of an existing single phase SST can be found in [6].

With reference to Section 2.2, not much can be done to improve the efficiency, lifetime or reliability of the conventional distribution transformer. The cost of the SST would also be much

higher than that of the conventional distribution transformer. The cost of the SST can be favourably compared to the total system cost, however, if tap changers, measurement apparatus and protection devices are included in calculating the costs. Investors might be prepared to pay several times the amount of a conventional distribution transformer, but then would also expect to receive a far superior functionality. The design goal of the SST is to improve the power quality of the secondary supply. The cost of the SST would moreover be reduced through mass production and due to the current trend of semi-conductors becoming cheaper.

Table 2-I: Conventional distribution transformer information (11 kV-400 V) [12; 13]

kVA	Cost	Maximum size
50	R 40 000	1.1m × 0.95m
100	R 52 000	1.3m × 1m
150	R 80 000	–
315	R 159 000	1.4m × 1.1m
500	R 204 000	1.8m × 1.2m
800	R 314 000	2m × 1.4m
1 000	R 391 000	–

### 2.4.1 Advantages of the SST

The major benefits of the SST in comparison with the conventional distribution transformer are listed below:

- **Input power factor correction:** This is obtained by using an active rectifier to control the input current that is drawn from the medium voltage (MV) supply. The input current can be set to be in phase, leading or lagging with the supply voltage. Consequently, the SST can be a resistive, capacitive or inductive load, as seen from the network side. Reactive power compensation can thus be achieved, although the effect on the network is dependent on the power rating of the SST.
- **Near perfect output voltage regulation:** The three phase output voltage is obtained with an actively controlled DC-AC inverter. This converter controls the output voltage instantaneously, which means that near perfect voltage regulation can be obtained.
- **Harmonic filtering:** Harmonics are prevented from flowing from the primary to the secondary of the transformer and vice versa. This is achieved by adding storage capacitance on the DC bus of the three phase DC-AC inverter. This isolates the harmonics, and prevents them propagating through the system.
- **Output short circuit protection:** The active control of the inverter limits the output current in a fault condition. The primary current is therefore not a reflection of the secondary fault current.

- **Voltage dip and swell compensation:** Depending on the size of the storage capacitance used in the SST, the output voltage can be kept at a constant rms value.
- **Single phase or three phase operation:** The SST can operate from either a single phase or a three phase connection; this is possible because each phase converts its energy into the same storage capacitance on the secondary of the SST.
- **Supply frequency variation:** The primary and secondary sides of the SST are actively controlled, thus the SST can operate at different frequencies. The SST can therefore operate at 50 Hz or 60 Hz on either the primary or secondary of the SST. This could possibly be used in a harbour to supply ships with either 50 Hz or 60 Hz supply frequencies.
- **Capable of supplying a DC voltage:** A high voltage DC or low voltage DC supply is available if required.
- **Operation under a fault condition:** Depending on the type of fault, the SST can still deliver power to the load. For example, if the SST is supplying power to residential loads and one of the phases is short circuited, the actively controlled DC-AC inverter can maintain the supply of the other two phases and limit the current of the faulty phase. This would keep  $\frac{2}{3}$  of the residential loads on until the fault is resolved by personnel [18].

For more advantages and the interaction of the SST with the network refer to [18].

## 2.5 Existing SST Research

The switching frequency across the isolation transformer is therefore required to be much higher than the fundamental of 50 Hz supply; this is done in order to reduce the size of the transformer. A comparison was done in [19] to prove the concept of a high frequency power transformer. A steel cored transformer designed at a frequency of 1 kHz can process three times more power than the identical transformer operating at 60 Hz. The 60 Hz measurement was done by reducing the primary voltage to prevent the core from saturating. The losses were compared, as expected, it was found that the core losses were the limiting factor of the transformer operating at 1 kHz. The limiting factor of the transformer operating at 60 Hz, however, was the maximum flux density.

To reduce the size of the transformer further, the switching frequency must be increased. A higher switching frequency also decreases the size of the passive filter components. The feasibility of the SST is greatly dependent on the switching frequency, thus it is proposed that the switching frequency of the isolation stage should be between 25 kHz and 50 kHz.

The SST has not yet been successfully operated at 11 kV, and, in fact, the entire concept of the SST is still in the research phase. The high input voltage of the primary is one of the major problems hindering the successful implementation of the SST. This is mainly due to the existing blocking voltages of the switching devices, such as insulated gate bi-polar transistors (IGBT). Currently, IGBTs can block voltages of up to 6 kV; however, they are only able to do so at a

switching frequency in the order of 1-2 kHz. Their switching frequency is thus far below the required SST switching frequency.

Existing research regarding silicon-carbide (SiC) IGBTs predicts that the blocking voltage could be improved by a factor 10 with respect to the conventional IGBT. The switching times of these SiC IGBTs are also expected to improve, with switching frequencies in the order of tens of kilohertz being expected. Nevertheless, SiC IGBTs have not yet been produced commercially due to problems regarding the crystal-lattice. Thus, it is doubtful that these devices will become generally available in the next 10 years, if at all.

Regardless, even if the SiC IGBT were able to block voltages in excess of 10 kV at higher switching frequencies, many other problems would occur. For instance, the switching losses would be very high due to the high voltage that is applied to the device. Thus, depending on the power rating of the device, the switching frequency would have to be reduced. The electro-magnetic interference (EMI) at these  $\frac{dv}{dt}$  ratings would also be problematic. Another issue concerns the isolation requirements of the gate drive circuitry. The required isolation would have to be in excess of 10 kV. The availability of bus capacitors at this high voltage is also a great concern. The SST is therefore not been designed on the hope of increased blocking voltages in the future.

Working prototypes of power electronic transformers have been built, albeit not at rated distribution levels. The highest incoming AC voltage connected to a SST was 3.6 kV in [6]. This prototype, however, achieved excellent results, such as harmonic filtering, power factor correction etc. The principle of the SST has thus been proven, although not at the required distribution voltages. The next milestone, therefore, involves connecting the SST to an 11 kV supply voltage.

As the main emphasis of the SST is based on the high voltage primary side of the SST, the topologies must be selected accordingly. The following subsections briefly describe the different topologies that have been implemented and discussed in the literature. These topologies include the AC-AC converter, the multi-level diode clamped converter, the flying capacitor multi-level converter and the series stacked converter.

### 2.5.1 AC-AC Converters

The AC-AC buck converter was first proposed in 1980 by Brooks, this was a method of stepping down the voltage by means of using series tied switches. The major drawback of the proposed converter was the use of these series tied switches. These switches would have had to endure not only the high input voltages but also the full load current. Furthermore, this proposed converter did not provide magnetic isolation, and this meant it was not feasible to use it for a SST. The information regarding this converter was obtained from [6].

Another attempt to design an AC-AC transformer was implemented in [19]; Figure 2.5 illustrates the schematic of this converter. This converter modulates the high AC input voltage to a high frequency square wave. The secondary side converter synchronously demodulates the switched waveform back to the fundamental frequency at a lower voltage. The main advantage of this converter with regard to the previous design lay in the addition of galvanic isolation.

The size of the transformer was also reduced with respect to the conventional distribution transformer. These AC-AC converters are moreover able to regulate the output voltage.

However, these prototypes were tested at voltages much lower than that required at distribution levels. The possibilities of increasing this voltage level are discussed in [19]; this is done by connecting two of these AC-AC converters in series. In this case, the individual voltage of each converter is clamped by capacitors similar to that in a half bridge converter. However, such AC-AC topologies do not add additional benefits, such as power factor control, energy storage and harmonic filtering. These converters also use series tied switches, which is a disadvantage. Thus the feasibility of the AC-AC converter in a SST application is questionable.

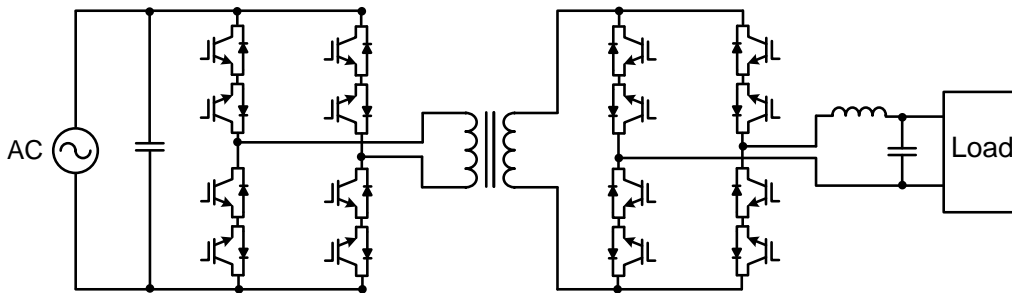


Figure 2.5: AC-AC transformer

### 2.5.2 Multilevel Converters

In order to overcome the short comings of the AC-AC transformer, such as power factor correction and energy storage, multiple back-to-back converters are required. Figure 2.6 shows a block diagram format of such a back-to-back converter. The first converter is an active rectifier connected to the 11 kV incoming supply voltage, whereas the second converter is a high voltage inverter, which transfers the power across the isolation barrier. The third active converter is a three phase DC-AC inverter on the low voltage side of the SST.

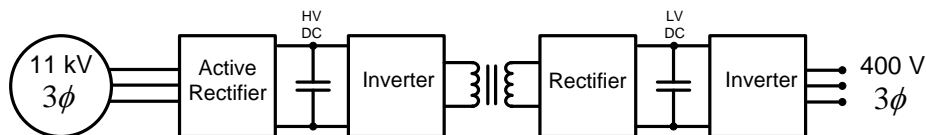


Figure 2.6: An SST design using back-to-back converters

It is possible to build the SST to achieve bi-directional power flow; however, this complicates the design, as an additional active converter is required on the secondary of the SST. This converter acts either as a rectifier or as an inverter, depending on the direction of the power flow. Bi-directional power flow is however not required in conventional distribution transformers. The converter discussions that follow are therefore based on a uni-directional power flow. This allows the use of a passive rectifier on the secondary, which simplifies the topology.

The active rectifier is therefore connected directly to the 11 kV incoming supply; it is proposed that this high voltage be broken down, using a multilevel converter phase arm [3]. Multilevel converters are used to clamp the voltage across each switch, thereby allowing multiple IGBTs of a smaller blocking voltage to be used. The blocking voltage of each switch in a multilevel converter is given as  $\frac{V_{DC}}{N-1}$ , with  $N$  defined as the number of levels. Phase arms of the diode clamped converter and of the flying capacitor multilevel converters are shown in Figure 2.7 [2; 3].

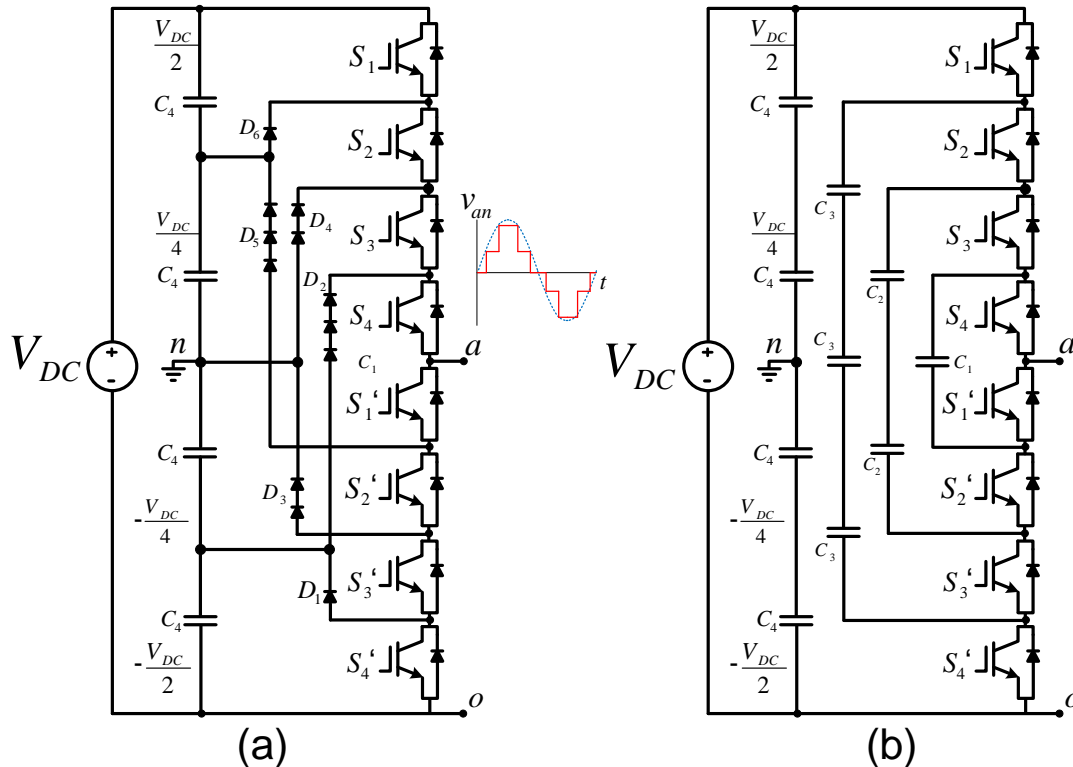


Figure 2.7: (a) 5 level diode clamped converter taken from [2] (b) 5 level flying capacitor converter taken from [3]

The diode clamped converter shown in Figure 2.7 (a) is a multilevel converter, but for demonstration purposes only 5 levels are shown. The 5 level converter has five possible output voltages, hence the name "5 level"; the output voltage  $v_{an}$  can be  $\frac{V_{DC}}{2}, \frac{V_{DC}}{4}, 0, -\frac{V_{DC}}{4}, -\frac{V_{DC}}{2}$ .

As the number of levels increase, the diode clamped converter can be applied to high input voltages. This is possible because the diodes equally balance the voltage over the IGBTs. The converter operates as follows: Assume that  $S_1, S_2, S_3, S_4$  are on, the voltage at point  $a$  with respect to neutral  $n$  is therefore  $\frac{V_{DC}}{2}$ . The voltage between  $a$  and  $o$  is  $V_{DC}$ . Diode  $D_1$  blocks  $\frac{V_{DC}}{4}$  and diode  $D_2$  blocks  $\frac{3V_{DC}}{4}$ , hence three diodes in series are used, assuming that the diode voltage rating is identical to that of each bus capacitor. Diodes  $D_3$  and  $D_4$  each block  $\frac{V_{DC}}{2}$ . Diode  $D_5$  blocks  $\frac{3V_{DC}}{4}$  whereas diode  $D_6$  blocks  $\frac{V_{DC}}{4}$ . These diodes therefore allow each switch in the off state to have a voltage rating of  $\frac{V_{DC}}{4}$ . The  $N$  levels of the output voltage  $v_{an}$  are therefore obtained by different switching configurations of the IGBTs.

The flying capacitor multi-level converter shown in Figure 2.7 (b) is another option of implementing a SST. This converter differs from the diode clamped converter as the capacitors clamp the voltage instead of the diodes. The possible output voltages are identical to those of the diode clamped converter, but switches  $S_1$  and  $S_1'$  are switched as alternate pairs.

The number of levels  $N$  required in the multilevel converter is dependent on the incoming voltage of the supply. The number of levels in the converter would be reduced if the SST were connected in a star configuration. The converter would therefore be connected to the phase voltage, which is smaller than the line voltage. This is not possible, though as there is no fixed neutral connection on a delta supply, and thus the voltage would not balance equally among the phase arms. The SST is therefore connected in a delta configuration, resulting in an increased number of levels for each multilevel converter.

Different configurations of these multilevel converters are proposed in [2]. Two multilevel converters could be used per phase, i.e. one for the active rectifier and the other for the high voltage inverter. Thus six multilevel converters are required for the SST. The blocking voltage of each multilevel converter in this configuration is given as 21 560 V, thus 23 levels would be required if 1 200 V IGBTs are used. These voltage levels would increase, however, if there would not be a stable neutral connection.

The number of multilevel converters could be reduced to four, if a three phase converter is built. This topology is similar to a three phase active rectifier using 3 half bridge converters and using space vector modulation. Thus, three multilevel converters are used for the active rectifier, one for each phase, while the fourth multilevel converter is used for the high voltage inverter. The blocking voltage of each multilevel converter in this configuration is given as  $1.2V_{LL}\sqrt{2} = 18670 V$ , if a 20% boost factor is used. This configuration has two advantages over the configuration discussed above; Firstly, the blocking voltage is reduced, which means that fewer levels are required. Secondly, four phase arms are required as opposed to six, which reduces the total number of components.

The main disadvantage of these multilevel converters lies in the number of components required and the fact that the converter is not modular. The input voltage is fixed, as is the power rating of the converter. The number of components for both multilevel converters assuming 20 levels and 4 phase arms is tabulated in Table 2-II from [2].

Table 2-II: Component count for multilevel SSTs

Component	Diode Clamped	Flying Capacitor
IGBTs (1200 V)	152	152
Bus capacitors (450 V)	45	45
Flying capacitors (450 V)	–	29640
Diodes (1200 V)	1292	–

Analysis of this data depicts the large number of components that are required for these converters and this data excludes gate drivers, isolated supplies and so on. The large number of



diodes needed in the diode clamped converter can be attributed to the series stringing of these devices, as the levels  $N$  of the converter increase.

The large number of capacitors in the flying capacitor converter is also caused by series stringing of these devices, as three 450 V capacitors are connected in series to match the blocking voltage of one switching device. Every time a series string is formed an identical capacitor is connected in parallel [2]. This is done to obtain uniform values of capacitance between the flying capacitors branches. The number of capacitors is thus a quadratic function of the number of levels. Due to the cost of these capacitors, this converter is therefore not feasible for the implementation of a SST.

Another disadvantage of these converters lies in the passive snubber circuits, which are required to balance the voltages equally across the diodes and capacitors. The reverse recovery present in the diodes of the diode clamp converter also complicates this topology. Advanced snubber circuits have however been designed to reduce the losses dissipated in the snubber circuitry, making the multilevel converter more efficient. These snubber circuits are based on an Undeland snubber, and they utilize fewer components than the conventional RCD/RLD snubber circuits [20]. A 20 level converter would nonetheless require a large number of additional components for the snubber circuitry. These losses would increase considerably as the number of levels increases.

The mechanical construction of a diode clamped converter is relatively simple, but as the number of levels increases many design challenges are introduced. These difficulties include the mechanical construction of the entire converter to reduce stray inductances between the device connections. The mechanical connections of the snubber circuitry and methods of cooling them are also of a concern. Thus the feasibility of the multilevel converter is questionable in distribution applications. The information in this section was obtained from [2–4; 21].

### **Existing Prototypes of the Multilevel Based SST**

The diode clamped converter is converted into a SST in [4] and is shown in Figure 2.8. This SST is a 20 kVA single phase prototype with a 2.4 kV input voltage and a split rail output voltage of 240 V or 120 V. The SST shown is created by connecting a back-to-back multi-level converter on the primary of the SST. The first multilevel converter is an active rectifier with the second acting as an inverter. Four high voltage transformers of 5 kVA each are connected in series on the primary and in parallel on the secondary. This is done to enable the voltage handling capability on the primary and the current carrying capability on the secondary. The rectifiers on the secondary are passive full bridge rectifiers.

This multilevel SST was fully tested and excellent results were obtained regarding voltage sag, load disturbances and harmonic filtering. The converter was a 3 level converter using custom packaged IGBTs. The input voltage was however only connected to 2.4 kV AC which is far below distribution voltage levels. The switching frequency obtained in the isolation stage was 20 kHz. An 11 kV prototype of the SST built in Figure 2.8 would require 3 phase arms per phase of 20 levels each. The numerous diodes that would be required in the 9 phase arms would make this diode clamped topology impractical for use in a SST.

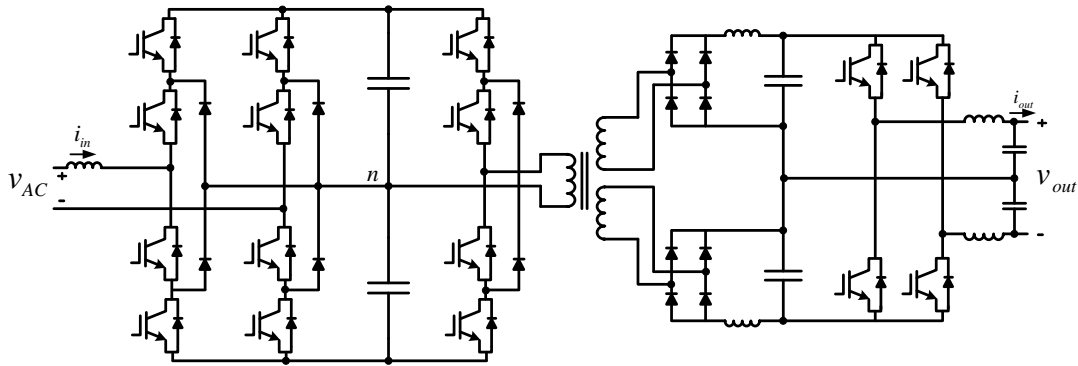


Figure 2.8: Single phase diode clamped SST built in [4]

### 2.5.3 Series Stacked SST

The third possible topology is the series stacked converter, which is in effect a series to parallel converter with cascaded inputs. This converter consists of multiple modular cells, with a cell defined as a single modular back-to-back converter. A single phase of the converter is shown in Figure 2.9. The high primary voltage is divided equally up among the cells, which forms the main voltage reduction. Each cell transfers power across the isolation barrier of which the secondary of all the cells are connected in parallel.

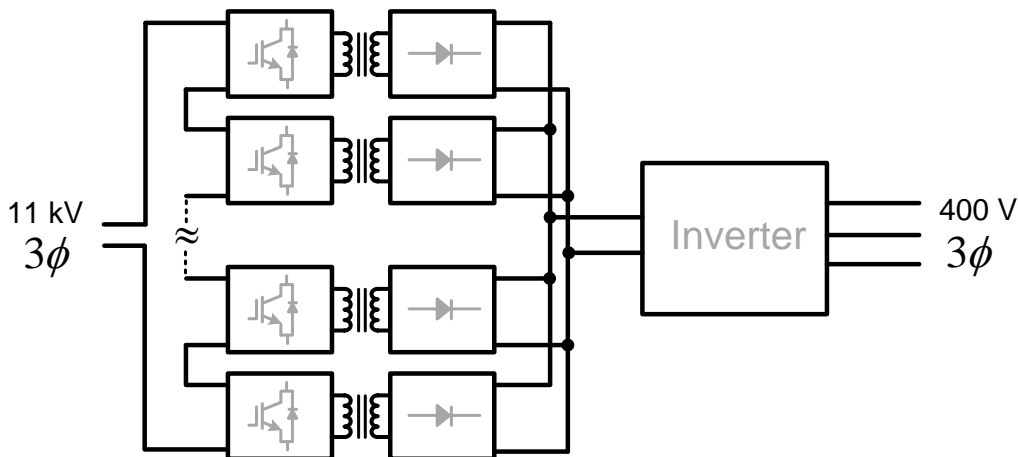


Figure 2.9: One phase of the series stacked SST

The input stage of the cell is comprised of a back-to-back converter. The first converter acts as an active rectifier, while the second acts as an inverter that transfers the power across the isolation barrier. A passive rectifier is used to rectify the secondary voltage of the transformer. The final stage of the series stacked SST is a 3 phase DC-AC inverter.

#### Advantages of the Series Stacked SST

The main advantage of this topology is its modularity, as cells can be added or removed depending on the primary voltage connected to the SST. The series stacked SST can therefore adjust to

the primary voltage, unlike the multilevel converter, which is fixed due to the number of levels in the initial design. The power rating of the SST could also be altered by adding additional cells in parallel.

The concept of modularity is adequately explained in [5] with regard to the overhead supply voltages for locomotives. France utilizes 25 kV at 50 Hz for their railway supply voltages whereas Italy uses 3 kV DC. The most commonly used supply is, however, 15 kV at a frequency of  $16\frac{2}{3}$  Hz. The transformers are large because of these low frequencies, thus power electronic converters are utilized to reduce the weight of the locomotive. It is therefore proposed to use configurable multi-chain converters to adapt to these various incoming supplies.

Figure 2.10 illustrates the concept of these converters. The primary connection of the cells is interchangeable with the aid of thyristors  $sw1 - sw4$ . Thyristors  $sw1$  and  $sw4$  are closed, while  $sw2$  and  $sw3$  are open for a series connection in the event of a high primary voltage. In the case of a lower incoming voltage, the cells are connected in parallel, and thus  $sw1, sw2$  and  $sw3$  are closed, while  $sw4$  is left open. This example highlights the modularity of the cell structure by altering the front end of the converter.

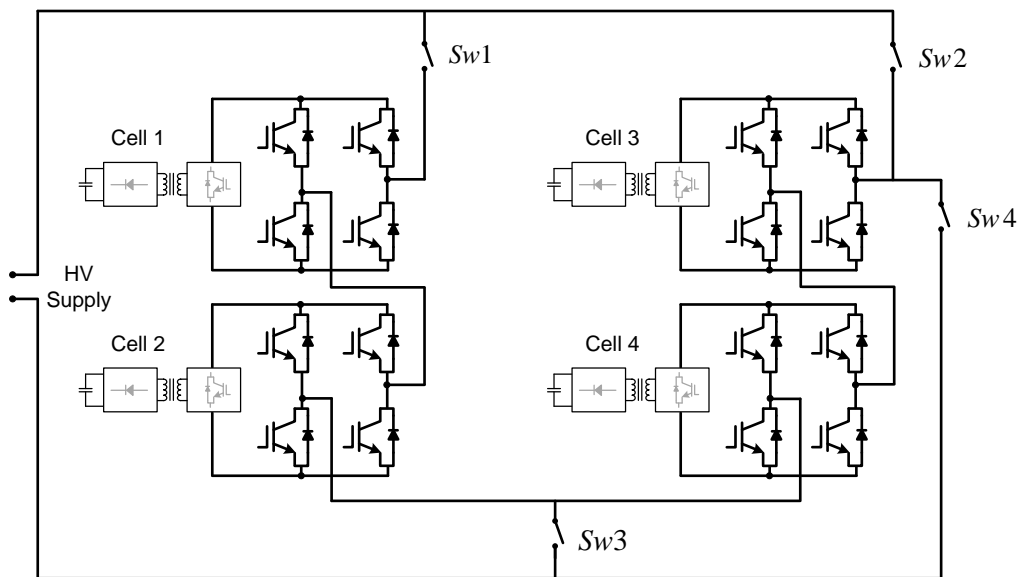


Figure 2.10: The concept of configurable multi-cell converters [5]

This modularity also applies to the SST, thus the number of cells added is a function of the primary voltage. Parallel connected cells would not typically be used, as  $N$  number of cells should then be connected in parallel to ensure voltage balancing. Thus, the power rating of each cell would typically be increased instead of connecting  $N$  parallel cells. The modularity of the cells also brings major benefits with respect to the cost of manufacturing, because a large quantity of identical cells are produced which reduces the costs. It is thus very likely that the series stacked SST will become more cost effective in the near future. The cost of the series stacked SST is comparable to the cost of the diode clamped converter [2].

The series stacked SST can also bypass a faulty cell, thus allowing normal operation of the SST to continue. Each cell voltage is merely increased proportionally. The power transferred across each isolation transformer in the series stacked converter is also reduced with respect to the single transformer in a multilevel converter. Stringing the transformer primaries in series to handle the high primary voltage is also avoided in this topology. This is due to each phase having  $N$  transformers, with  $N$  defined as the number of series stacked cells. Thus each transformer has to handle a voltage of  $\frac{1.2\sqrt{2}V_{LL}}{N} = 1.24$  kV, if 15 cells are utilized. The insulation requirements between the transformer windings is therefore reduced, compared to those of the single transformer in the multilevel converter. The reduced power requirements of each transformer in the series stacked converter enhance the possibility of using natural cooling for the transformers.

All the possible topologies of the SST require a high voltage inductor which is connected in series with the high voltage supply. The active rectifier requires this boost inductor to maintain a sinusoidal input current. The series stringed topology allows the switching signals of the active rectifier to be interleaved, resulting in a converter switching frequency of  $N \cdot f_s$ . This increased frequency reduces the inductance required by a factor of  $N$ . This is a significant advantage, as it is difficult to manufacture an inductor with a 11 kV insulation between windings. This boost inductor can also be separated into  $N$  inductors, thus one inductor on each cell, which increases the modularity of the SST. Multilevel converters also have the property of reducing the inductor size due to an increase in switching frequency.

The series stacked SST as well as the multilevel topologies allow the SST to operate with a single phase supply on the high voltage side. This is because each phase supplies power into the same low voltage DC bus of the 3 phase DC-AC inverter. However, the power transmitted to the load would be reduced to a third of the rated power.

### Disadvantages of the Series Stacked SST

The series stringed topology also has numerous disadvantages, the main being that the high primary voltage is shared equally among the cells. Active control of these cell voltages is proposed in [2; 3], but this would add complexity to the control of the entire SST. Advanced control methods and the sensing of many operating conditions on each cell would be required. Research also proposes the use of varistors or voltage clamping circuits to clamp each cell voltage; however, the power dissipated in these circuits is of concern. The series stringed SST was built in [6] with varistors connected across each cell.

The future of the series stringed SST was therefore bleak because of problems associated with the voltage balancing of each cell. The voltage balancing dilemma was recently solved in [22], this study gives the formal derivation of the voltage balancing mechanism in a series stringed back-to-back converter. In terms of the reported findings, the voltage over each cell balances in the steady state operation and rebalances if external perturbations are present. Thus, the active control of each individual cell voltage is not required if the cells are given a similar duty cycle command, resulting in a simplified control circuit of the SST.

Other disadvantages of the series stringed SST include the sensing of the individual cell

operating conditions and the transfer of this data to the main controller. This topology also requires a large number of components due to the existence of multiple cells. The number of cells required to connect the SST to distribution voltages is in the order of 15. Three phase operation of the SST would therefore require 45 cells. The primary of each cell requires 8 IGBTs, thus 360 high voltage IGBTs would be required for the two back-to-back converters alone. Nonetheless, the cost of the series stringed SST is comparable to that of the diode clamped converter [2]. The information in this section was obtained from [2; 3; 6; 23].

### Existing Prototypes of the Series Stacked SST

The series stacked topology was researched and built in [6; 23] with a power rating of 10 kVA at 7.2 kV primary voltage. Referring to Figure 2.9, each input module rectifies the incoming AC voltage and provides input harmonic filtering by means of a single switch boost converter, as shown in Figure 2.11.

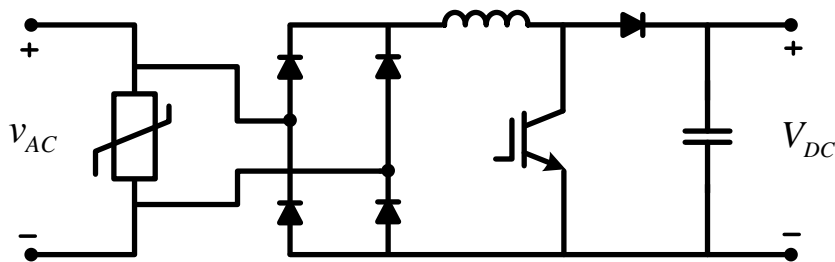


Figure 2.11: Input module used in [6]

The second converter is the high frequency DC-DC converter, which transforms the power over to the secondary of the SST. The switching frequency achieved was 10.8 kHz, and air cooled isolation transformers were utilized. A passive rectifier is utilized on the secondary of each isolation stage, namely, a full bridge center tapped rectifier. The output stage consisted of a split rail full bridge inverter.

The prototype was only able to operate at 50% of its design voltage, namely at 3.6 kV. The reason for this was the large amount of electromagnetic interference (EMI) present. The input voltage and current waveforms were distorted, which was caused by the impedances of the variable voltage sources. The output single phase inverter however kept the voltage constant under load disturbances. The problems encountered regarding the EMI and input distortion of the input waveforms were identified and are currently being improved in a second iteration prototype.

## 2.6 Chosen Topology

The size, cost and efficiency of the conventional transformer are still far superior to those of any SST. The emphasis is therefore not improving on these factors but rather to build a working prototype of an SST that operates at the required distribution voltage level.

The topologies mentioned in the previous sections all require a large number of components. Each of the topologies also requires extensive digital control and communication throughout the entire SST. Weighing up the advantages and disadvantages between the various topologies, the series stacked SST was found to be the most favourable [2]. This research was based on an extensive comparison between the possible topologies regarding cost, functionality and integration of a SST in future networks.

## 2.7 Future Research

The series stacked SST is therefore chosen for the prototype, and thus a modular approach is followed. The series stacked SST requires 15 modular cells per phase if 1200 V IGBTs are used, which means that three phases require 45 cells. The scope of this thesis is based on the isolation stage as well as on the three phase inverter. A block diagram of the modular cell connected to the three phase inverter is shown in Figure 2.12. The stages that are highlighted in black are discussed in this thesis.

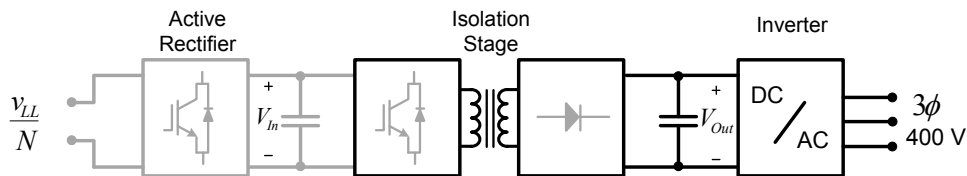


Figure 2.12: Block diagram of the modular cell connected to the inverter

The next section briefly discusses the relevant literature regarding the isolation stage as well as the three phase inverter. This literature is however explained in even greater depth in the relevant chapters, for further discussions see Chapters 4, 6 and 5.

### 2.7.1 Isolation Stage

The isolation stage includes a high voltage DC-DC converter. The switching frequency of this stage is required to lie between 25 kHz and 50 kHz. This transformer is therefore dependent on the switching frequency of the isolation stage. The possible configurations of this DC-DC converter are between the half bridge and the full bridge converters. The disadvantage of the half bridge converter is that the full primary current flows through the bus capacitors. A substantial bus capacitance is therefore required to reduce the bus ripple voltage. Series stringed electrolytic capacitors would typically be used as these capacitors have larger capacitance values than those of polypropylene capacitors.

The size of the modular cell is largely dependent on the bus capacitors, and thus the full bridge converter is considered. This topology requires less bus capacitance, as the primary current flows mainly through the semiconductors. The trade-off is therefore made between bus capacitance versus the use of silicon. The full bridge converter requires two more IGBTs, but polypropylene bus capacitors can be used. The advantage of these is their self-healing ability

and their increased life expectancy as opposed to that of the electrolytic capacitors. The full bridge converter is therefore chosen for the isolation stage of the SST.

A remarkable amount of literature is available regarding full bridge DC-DC converters, and thus only journal publications are considered in this research. The articles that are considered propose methods of achieving soft switching in full bridge converters [24–27]. Soft switching is achieved in these converters by using zero voltage switching (ZVS), zero current switching (ZCS) or a combination of the two namely ZVZCS. The emphasis of these converters is to maintain soft switching for an increased load region. These soft switching techniques do however bring a large degree of complexity into the circuit. An example of these topologies is an active switching circuit on the secondary, and an auxiliary winding on the transformer or series connected transformers on the primary. These topologies are discussed in greater detail in Chapter 4.

A trade-off is therefore required between the switching losses and the additional complexity of the DC-DC converter. The switching losses of semiconductors are gradually being reduced due to continuous improvements of the switching devices. The switching losses are proportional to the switching frequency as well as to the switching times of the device. Currently there are 1 700 V IGBTs available that have switching times in the order of 60 ns. The switching times of 1 200 V IGBTs are currently in the order of 40 ns. The switching losses are therefore reduced due to these minute switching times. The switching losses are therefore taken into account, thus the additional complexity is not considered for the isolation stage of the SST.

The chosen DC-DC converter is the conventional phase shifted full bridge. This converter does however have soft switching characteristics due to the inherent ringing waveforms of the parasitic components in the circuit. The soft switching of this converter is mainly dependent on the amount of energy that can be stored in the leakage inductance. The soft switching of this converter is therefore dependent on the load. At lighter loads, the soft switching is lost, but the switching losses are proportionally reduced because the current is less. The converter is therefore operated to obtain the maximum amount of soft switching, and as the soft switching is lost, the switching losses are taken into account.

### 2.7.2 Three Phase DC-AC Inverter

A three phase half bridge inverter is chosen for the output stage of the SST, because the neutral of the low voltage supply can be connected between the bus capacitors. The literature regarding the design of the inverter as well as the control strategy is briefly discussed below.

#### **Inverter Design**

The design of the inverter is based on the current and voltage waveforms flowing in the respective components. The losses in the inverter are an integral part of the design, as this determines the size of the heatsink and cooling fan. The size of the inverter is largely dependent on the size of the heatsink. Thus, an accurate method of calculating the losses is required.

The losses in inverters consist of passive component losses as well as switching component losses. Passive losses mainly include the conduction losses occurring in the inductors and capac-

itors. Switching component losses are the losses dissipated in the diodes and IGBTs. Switching component losses are further subdivided into switching and conduction losses. The most accurate way of determining the losses is to measure them physically. Two main methods are used for this, namely electrical and calorimetric methods [28]. Loss measurements can however only be done on an existing inverter, thus a theoretical loss calculation is required for the design phase. Optimization of the external heatsink and fan is dependent on the accuracy of the loss calculations.

A few methods showing how losses were calculated in the past are described in [8; 29–31]. Analytical methods of calculating switching device losses are available in the literature, but these methods do not take into account the inductor ripple current. Large inverters in the range of hundreds of kVA are commonly operated under large inductor ripple current conditions. This is done to limit the physical size of the inductors. The required inductance could however be halved by using uni-polar switching in a full bridge converter, as this effectively doubles the frequency of the inductor current. The half bridge converter unfortunately does not have this property.

Thus, it is uncertain how this large inductor ripple current affects the losses in the inverter. The effect of the carrier waveform on the losses is also not known. These two uncertainties are therefore discussed in this thesis.

### **Inverter Control Strategies**

In the past, inverters were controlled with a relatively slow outer voltage loop, with a reaction time in the order of a few cycles of the fundamental output voltage. This type of control rarely included feed-forward parameters, thus the response to disturbances was relatively slow and non-linear loads distorted the output voltage [32]. Later this was improved by using instantaneous control, which improved the transient response and the THD of the output voltage. These controllers were implemented using a single outer voltage loop. The advantage of this method was that it had a simple design but a relatively slow transient response.

A double loop control strategy consisting of an inner current loop and outer voltage loop was therefore introduced to ensure a faster transient response. This method effectively separates the second order system of the filter into two first order systems, thus simplifying the design of the outer voltage loop.

Digital control, as opposed to analogue control, is the preferred option in most controllers today. The factors that limit the implementation of inverter control algorithms in digital signal processors (DSP) are the processing speed and ADC conversion times. Multiple digital control strategies have been developed in recent literature, for example predictive control has been implemented to shape the load spectrum in [33]. Predictive controllers have also been presented in [34] and robust predictive controllers in [10]. A low computational predictive control strategy was presented in [35] by using the superposition of the inductor current.

A dead beat controller was implemented in [36] and load decoupling and hysteresis control was discussed in [37]. Hysteresis control and average current mode control are effective control methods for the inner current loop, but they are best implemented using analogue electronics.



Digital implementation of these methods requires multiple samples per cycle at very high sampling rates. A double loop state-space control strategy is presented in [36]; this method makes use of a dead beat controller to improve the dynamic response of the system. This strategy is unique to digital controllers due to the specific pole placements of the system. This controller in effect increases the response time of the system. An output voltage decoupling mechanism is also implemented to increase the performance of the inner current loop.

A state-space observer was developed in [32] to control inverters using a double loop strategy. Different forms of load decoupling are also discussed with regard to this controller. Excellent results were obtained with these state space controllers, although their control algorithms are complex.

The above literature was revised and the relevant controllers methods were identified as [10; 35]. The robust predictive control in [10] describes a method of increasing the robustness of the controller to mismatch in filter inductance. An alternative sampling strategy is also employed to increase the accuracy of the predicted current. The control algorithm is however based on a grid connected inverter, thus an alternative control algorithm is required.

A predictive control algorithm was developed in [35] for a full bridge inverter using uni-polar switching. This method uses the superposition of the inductor current in the different states of the converter operation. The control algorithm requires very little computational time in the DSP, thus it is possible to implement this algorithm in a fixed point DSP.

The control method developed in this thesis is based on the sampling strategy in [10], and the control algorithm of [35] is extended to a half bridge inverter.

## 2.8 Conclusion

The operation of the conventional distribution transformer was briefly discussed and the advantages and disadvantages of this transformer were highlighted. The concept of a solid state transformer (SST) was introduced to overcome the disadvantages of the conventional transformer and to improve the quality of the low voltage supply. Different topologies of realizing such an SST were discussed and the series stacked SST was chosen for the SST prototype. The main reason for choosing this topology was that it is modular, which means that this converter can be implemented in power distribution and multiple other fields. A three phase 11 kV prototype SST was proposed, with 15 series stacked cells per phase resulting in 45 modular cells in the three phase SST. The existing literature regarding the modular cell and the output stage converter was discussed.

## Chapter 3

# Solid State Transformer Overview

The various topologies of the SST are discussed in Chapter 2; they range from the AC-AC converter to the series stacked SST. The series stacked SST is chosen for the prototype due to the modularity of the design [2], which makes it adaptable to the amplitude of the incoming supply voltage. This chapter discusses the operation of the series stacked SST and the design of the modular cell.

The SST prototype is rated at 80 kVA at an incoming distribution voltage of 11 kV. The SST consists of three branches of series stacked converters, one for each phase. Each series stacked converter consists of  $N$  modular cells connected in series. The block diagram of the series stacked cell is depicted in Figure 3.1, which shows that the cell consists of an active rectification stage as well as an isolation stage.

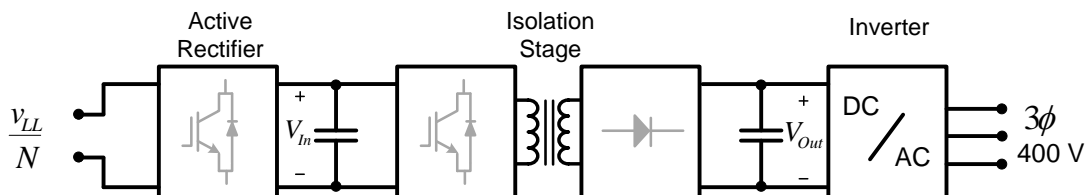


Figure 3.1: The back-to-back converter in each cell, which is connected to the DC-AC inverter

The topology of the three phase SST is shown in Figure 3.2. The 11 kV feeder is connected in delta, thus the line voltage  $V_{LL}$  is connected to each series stacked converter. Each converter consists of  $N$  number of series connected cells which reduce the individual cell voltage to  $\frac{V_{LL}}{N}$ .

This AC voltage, namely  $\frac{V_{LL}}{N}$ , is then rectified using an active rectifier in each cell. This active rectifier acts as a boost converter and thus the output DC voltage of the rectifier, namely  $V_{In}$  is always higher than the peak of the incoming sinusoid. If this voltage  $V_{In}$  is not higher, the converter acts as a passive full bridge rectifier, resulting in a distorted current drawn from the medium voltage supply. The boost factor is typically 20% greater than the peak value of the incoming sinusoidal voltage, namely  $V_{In} = 1.2\sqrt{2}\frac{V_{LL}}{N}$ .

The second stage of the cell is the isolation stage, in which the power is transferred across the isolation barrier utilizing a high voltage DC-DC converter. It is proposed that the switching

frequency of this section should operate at 50 kHz.

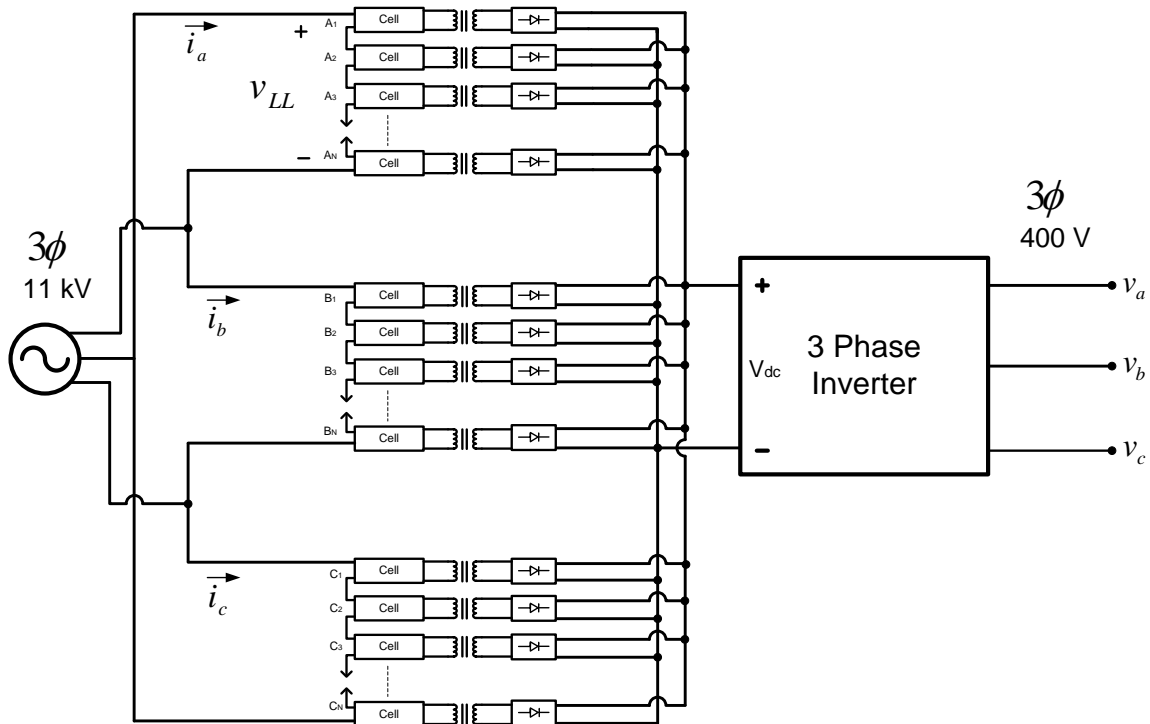


Figure 3.2: Topology of the three phase SST

The final stage of the SST shown in Figure 3.2 is the three phase inverter. The DC bus of the inverter is fed by the  $3 \cdot N$  isolation stages, which are connected in parallel. The entire SST is controlled by a global controller, and two way communication is thus present between the controller and each stage of the SST.

### 3.1 Series Stacked Converter Design

The active rectifier and DC-DC converter in the cell are comprised of a back-to-back full bridge converter. The reason why a full bridge converter was chosen is discussed in Chapter 4. The current flowing through the IGBTs on the primary of the SST is relatively small. As a result, the high bus voltage  $V_{In}$  of each cell is the rating factor of the IGBTs. The switching devices used are 1 700 V IGBTs, thus the bus voltage  $V_{In}$  at which these devices can operate is optimistically rated at 1 300 V.

This approximation is made to determine the number of series stacked cells required in each phase arm. The advantage of the modular design is that, if the bus voltage  $V_{In}$  is not reached, extra cells could be added in series, which would reduce the individual bus voltage  $V_{In}$  of each cell.

The total bus voltage is equal to  $V_{DC(Total)} = 1.2\sqrt{2}V_{LL}$ ; using this, the number of series stacked cells is given by:

$$\begin{aligned} N &= \frac{1.2\sqrt{2}V_{LL}}{V_{In}} & (3.1) \\ &= \frac{1.2 \cdot 11000 \cdot \sqrt{2}}{1300} \\ &= 15 \text{ cells} \end{aligned}$$

Each branch of the SST therefore requires a minimum of 15 cells, resulting in 45 cells for the three phase SST. Referring to Figure 3.2, the rms current flowing through the series linked cells namely  $I_{a(rms)}$  is calculated using fundamental 3 phase analysis:

$$\begin{aligned} I_{a(rms)} &= \frac{80 \text{ kVA}}{3 \cdot 11 \text{ kV}} & (3.2) \\ &= 2.42 \text{ A} \end{aligned}$$

The power that is transmitted through each cell is given as:

$$\begin{aligned} P_{Cell} &= \frac{80 \text{ kW}}{3 \cdot 15} & (3.3) \\ &= 1.8 \text{ kW} \end{aligned}$$

The SST is not designed with lengthy overload capabilities opposed to the conventional distribution transformer. Generally semiconductor based converters do not allow lengthy overloading periods. This is due to the design criteria of operating semiconductors very close to their maximum junction temperature  $T_{jmax}$ , thus reducing the size of the heatsink. Overload capabilities are however obtained if the converter is designed to operate at the overload level continuously. The cost of such a converter is greatly increased and the semiconductor devices are underutilized under nominal load conditions.

## 3.2 Cell Description and Design

The modular cell is a back-to-back full bridge converter. The first H-Bridge has the purpose of forcing the input current to be sinusoidal and regulating the bus voltage  $V_{In}$ . This converter is an active rectifier with a double loop control strategy, in which the inner loop controls the inductor current and the outer loop controls the bus voltage  $V_{In}$ . The network will therefore see a purely resistive load if the input current is purely sinusoidal and in phase with the input voltage. The basic schematic of the cell is shown in Figure 3.3.

The active rectifier is switched in a boost converter configuration. This converter is switched at a high frequency which results in a smaller inductor ripple current. The size of the boost inductor  $L_B$  is inversely proportional to the switching frequency  $f_s$ .

The second H-Bridge is a DC-DC converter, which transfers the power across the isolation barrier at a high switching frequency. The frequency of the DC-DC converter is limited by the

switching losses as well as by the parasitic inductances in the circuit. The feasibility of the SST is highly dependent on this switching frequency, as this determines the transformer size.

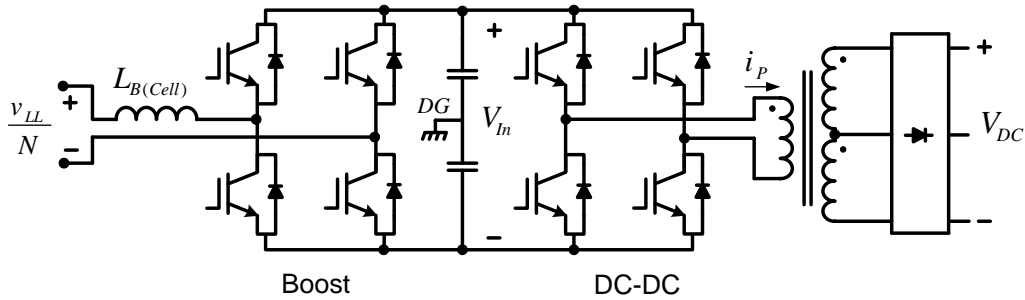


Figure 3.3: Cell schematic

The flux density  $B$  of the transformer is the factor that determines the size of the core, from Faraday's Law [11]:

$$e = N \frac{d\phi}{dt} \quad (3.4)$$

The flux is equal to  $\phi = A_e B$ , with the effective area of the core as  $A_e$ . Rearranging Equation 3.4, the change in flux density  $dB$  is given as:

$$dB = \frac{e \cdot dt}{N \cdot A_e} \quad (3.5)$$

Referring to Equation 3.5, the volt time integral is reduced as the switching frequency increases. The size of the core is therefore reduced as the change in flux density  $dB$  is reduced.

The second factor that determines the size of the transformer is the required isolation between the primary and secondary windings. The secondary of each isolation stage is connected in parallel, thus the 45 transformer secondary's are at the same static voltage potential. However, the primary winding of each transformer is at a different potential. The static potential of each primary winding is at  $nV_{In}$ , with  $n$  ranging from 0 to  $N$ . Each transformer therefore requires a different isolation level depending on its primary potential.

The concept of a modular cell requires each cell to be identical, thus all the transformers are designed to have an identical isolation rating. The minimum isolation between the primary and secondary of each transformer is expressed as  $NV_{In}$ . The size of this isolation level furthermore increases the size of the transformer as the windings are no longer placed on top of each other. The conventional distribution transformer, however, requires an isolation of 75 kV between the primary and secondary windings [12]. The purpose of this is to protect the downstream feeders from lightning, the 75 kV rating is therefore an impulse withstand rating.

The secondary of the transformer is rectified using a full bridge passive rectifier. This rectifier provides a center point connection, which is connected to the neutral of the LV supply. The DC-AC inverter is a 3 phase arm half bridge inverter. The 45 isolation stages which source power

to the inverter are interleaved and therefore supply the bulk of the current. The advantage of this is that the bus capacitors do not require large current ratings.

The following sections discuss the design and implementation of the modular cell. The design of the passive components as well as of the auxiliary circuits required to operate the back-to-back converter is discussed. The mechanical construction of the cell is also explained at the end of this chapter.

### 3.2.1 Magnetic Components

The magnetic components in the cell consist of three inductors and one transformer. The three inductors are used for the boost inductor and the two filter inductors. The following subsection briefly describes the design of the magnetic components.

#### Boost Inductor

The series linked active rectifiers require an inductor to be connected in series with the medium voltage supply to boost the incoming voltage. The design of this inductor is dependent on the voltage, current and switching frequency of the converter. The analysis of the boost inductor  $L_B$  is done with a single full bridge converter, this is equivalent to  $N$  series connected active rectifiers using synchronized switching. The block diagram of the active rectifier is shown in Figure 3.4. The bus voltage is defined as  $V_{DC(Total)}$ , the incoming voltage and inductor voltage are defined as  $v_{LL}$  and  $v_{L_B}$  respectively. The voltage  $v_P$  is defined as the switching voltage of the full bridge active rectifier.

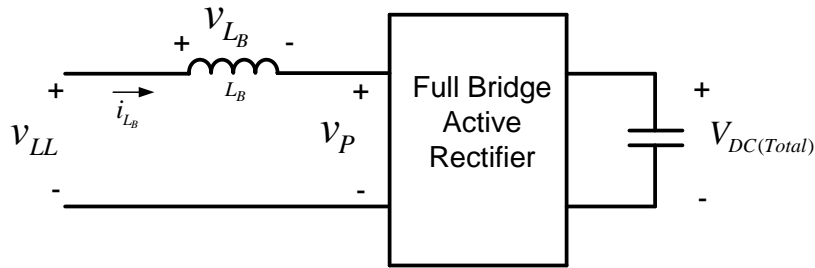


Figure 3.4: Single phase series connected active rectifier

The inductance value of the boost inductor  $L_B$  is calculated using the differential equation of an inductor:

$$v_{L_B} = L_B \frac{di}{dt} \quad (3.6)$$

The derivation of the respective parameters of Equation 3.6 is explained below. In Figure 3.4, the inductor voltage  $v_{L_B}$  is given as:

$$v_{L_B} = v_{LL} - v_P \quad (3.7)$$

The switching voltage  $v_P$  is dependent on the type of modulation used in the converter; bipolar and unipolar PWM are considered for the converter. The possible amplitudes of the switching voltage  $v_P$  using bipolar PWM are either  $V_{DC(Total)}$  or  $-V_{DC(Total)}$ . Unipolar switching allows  $v_P$  to have three voltage levels, namely  $V_{DC(Total)}$ ,  $0 V$  and  $-V_{DC(Total)}$ . Unipolar PWM effectively doubles the switching frequency  $f_s$  and the voltage across the boost inductor is reduced with respect to that of bipolar PWM.

The simulated waveforms of the active rectifier using unipolar PWM are shown in Figure 3.5. The incoming line voltage is set to 11kV and the bus voltage  $V_{DC(Total)}$  is charged to 18.8 kV. The peak inductor voltage  $V_{L_B}$  occurs when the incoming line voltage  $v_{LL}$  crosses through zero. The duty cycle  $d$  of both legs is equal of 50% as  $v_{LL} = 0 V$ .

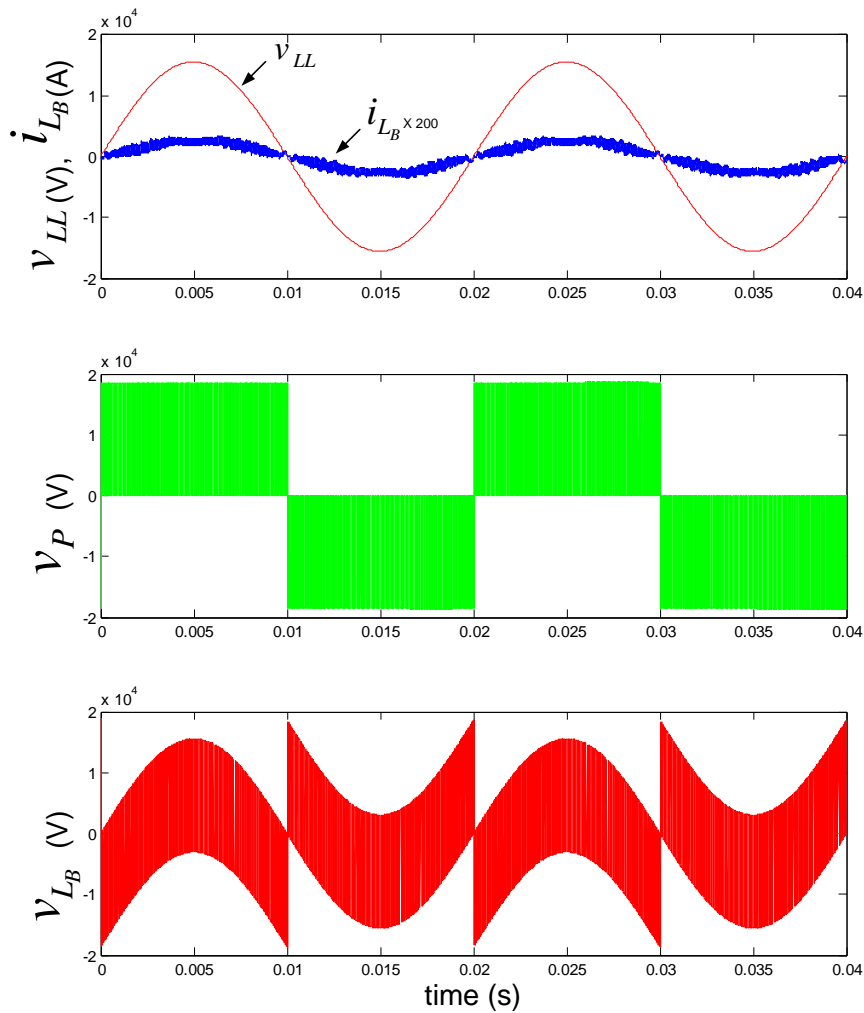


Figure 3.5: Simulated waveforms of the active rectifier using unipolar PWM

The peak inductor voltage  $V_{LB}$  is equal to the bus voltage  $V_{DC(Total)}$  and is given as:

$$\begin{aligned} V_{LB} &= V_{DC(Total)} \\ &= 1.2\sqrt{2}V_{LL} \\ &= 18670 \text{ V} \end{aligned} \quad (3.8)$$

The amplitude of the ripple current  $di$  is designed to be 10% of the peak input current, namely  $I_{a(Peak)}$ . This current  $I_{a(Peak)}$  is obtained using Equation 3.2 and is equal to  $I_{a(Peak)} = \sqrt{2} \cdot I_{a(rms)}$ . The amplitude of the ripple current  $di$  is given as:

$$\begin{aligned} di &= \sqrt{2} \cdot I_{a(rms)} \cdot 10\% \\ &= 342 \text{ mA} \end{aligned} \quad (3.9)$$

The time increment  $dt$  in Equation 3.6 is dependent on the switching frequency  $f_s$  and the duty cycle  $d$  of the active rectifier. The switching frequency is assumed to be 25 kHz and a duty cycle equal to 50% is used as this is where the peak inductor voltage  $V_{LB}$  occurs. The time increment  $dt$  is therefore equal to  $d\frac{T_s}{2}$  because the switching frequency  $f_s$  is effectively doubled with unipolar PWM.

Rearranging the terms in Equation 3.6 and substituting Equation 3.8 and 3.9 into Equation 3.6, the inductance  $L_B$  is approximated as:

$$\begin{aligned} L_B &= \frac{V_{LB} dt}{di} \\ &= \frac{1.2\sqrt{2}V_{LL} \cdot d\frac{T_s}{2}}{\sqrt{2} \cdot I_{a(rms)} \cdot 0.1} \end{aligned} \quad (3.10)$$

The inductance  $L_B$  can further be reduced by using interleaved switching, as this effectively increases the switching frequency  $f_s$  by a factor  $N$ . The required inductance  $L_B$  using interleaved switching is given as:

$$L_B = \frac{1.2\sqrt{2}V_{LL} \cdot d\frac{T_s}{2}}{N\sqrt{2} \cdot I_{a(rms)} \cdot 0.1} \quad (3.11)$$

The boost inductor  $L_B$  is divided into  $N$  smaller inductors, namely  $L_{B(cell)}$ . This is done to reduce the voltage over each inductor, which in turn reduces the insulation requirements. The inductance required for each cell inductor  $L_{B(cell)}$  is given as:

$$\begin{aligned} L_{B(cell)} &= \frac{1.2\sqrt{2}V_{LL} \cdot d\frac{T_s}{2}}{N^2\sqrt{2} \cdot I_{a(rms)} \cdot 0.1} \\ &= 2.13 \text{ mH} \end{aligned} \quad (3.12)$$

The  $N^2$  term in the denominator of Equation 3.12 greatly reduces the size of the inductance required. The first  $N$  multiplication term is due to the cells, which are interleaved. The second  $N$  multiplication term is obtained as  $N$  series stringed inductors are utilized, one on each cell.



### Transformer

The first iteration of the transformer is designed with the input and output voltages of the converter as 1 350 V and 800 V respectively. The transformer is optimistically designed as it is not sure if the 1 700 V IGBTs are able to switch at this bus voltage  $V_{In}$ . The power specification of the transformer was 2.2 kW.

The transformer is designed to operate at a variable frequency ranging between 25 kHz and 50 kHz. This is done as the optimal switching frequency is not yet known. The lower frequency determines the number of windings required on the primary of the transformer, as the flux density  $dB$  is inversely proportional to the switching frequency  $f_s$ . The higher frequency, determines the number of parallel conductors required in each winding with regard to the skin effect. The higher the frequency, the thinner the parallel conductors must be. The design parameters are shown in Table 3-I

Table 3-I: Magnetic variables

Magnetic design specifications		
$V_{In} = 1350 \text{ V}$	$V_{Out} = 800 \text{ V}$	$P_{Load} = 2.2 \text{ kW}$
$f_s = 25 - 50 \text{ kHz}$	$d = 45 \%$	$B_{Sat} = 400 \text{ mT}$
$dB = 2 \cdot 80\% \cdot B_{Sat}$	$A_e = 535 \text{ mm}^2$	$Core = E65$

The number of windings on the primary is determined by Faraday's Law and using the specifications in Table 3-I:

$$\begin{aligned} N_1 &= \frac{V_{In} \cdot dt}{A_e \cdot dB} \\ &= 71 \text{ turns} \end{aligned} \quad (3.13)$$

Referring to Figure 3.6 and Appendix A, the transfer function of the full bridge converter is derived using first principles and given as:

$$\frac{V_{Out}}{V_{In}} = 4 \times \frac{N_2}{N_1} d \quad (3.14)$$

The turns ratio using Equation 3.14 is equal to  $\frac{N_2}{N_1} = 0.33$ . The transformer core used was the E65 core from EPCOS. This core has a sufficiently large winding area; the primary windings were increased to 85 turns, whereas 29 windings were wound on the secondary.

The rms current flowing through the primary and secondary conductors is calculated as 1.63 A and 2.75 A respectively. The required surface area in the primary and secondary conductors at a current density of  $J = 4 \text{ A/mm}^2$  is  $0.408 \text{ mm}^2$  and  $0.69 \text{ mm}^2$  respectively. The skin depth at 50 kHz is  $0.295 \text{ mm}$ , thus any conductor thicker than 0.6 mm in diameter is not used at this frequency. The primary winding consists of two parallel conductors of 0.6 mm in diameter, whereas the secondary winding consists of three parallel conductors of 0.6 mm in diameter.

### Filter inductors

The center tap full bridge rectifier requires two filter inductors, namely  $L_1$  and  $L_2$ . The schematic of the circuit is shown in Figure 3.6.

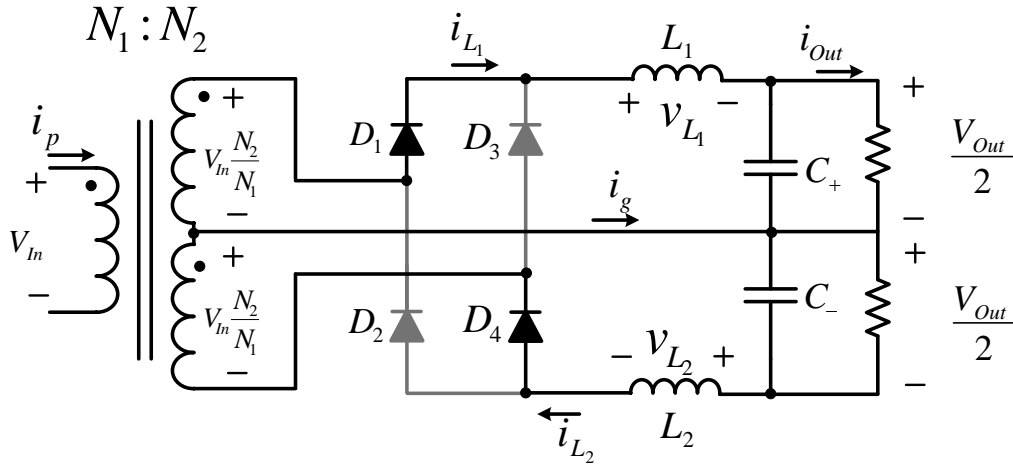


Figure 3.6: Full bridge center tap rectifier

The filter inductors combined with the bus capacitors form a low pass LC filter. The inductors however mainly reduce the amplitude of the ripple current  $\Delta i_L$ . The inductance of the filter inductors is calculated according to the allowable percentage ripple current with respect to the output current  $I_{Out}$ . The inductor ripple current  $\Delta i_{L_1}$  is derived from first principles and given as:

$$\Delta i_{L_1} = \frac{\left( V_{In} \cdot \frac{N_2}{N_1} - \frac{V_{Out}}{2} \right)}{L_1} \times dT_S \quad (3.15)$$

The inductor ripple current  $\Delta i_{L_1}$  is designed to be 20% of the load current  $I_{Out}$ . The load current  $I_{Out}$  is given as 3 A, and the switching frequency  $f_s$  as 35 kHz. Utilizing Equation 3.15, a filter inductor of 1.29 mH is required at a 45% duty cycle  $d$ .

The selection process for the inductor core is between distributed air gapped cores and gapped ferrite cores. The distributed air gap cores have a much higher saturation density, namely in the order of 10 500 Gauss. The advantage is that more energy is stored in the core as opposed to the gapped ferrite core, thus the size of the core is reduced. Another advantage of the distributed air gapped core is that no fringing flux occurs as opposed to what happens in the gapped ferrite core.

The distributed air gapped core is chosen for the design because it is smaller than the gapped ferrite core. The chosen core is the K4022E26u from Magnetics [38]. This material has a nominal inductance of  $104 \frac{nH}{turn^2}$ , thus the calculation of the reluctance of the core is not required. The inductance is simply determined by the number of turns.

The number of turns required to wind a 1.29 mH inductor is calculated to be 112 turns. The number of turns is however increased to 132 turns, this is done because of the roll off of the

initial permeability as the amplitude of the current increases. The cross sectional area of the conductor is chosen to be  $0.9 \text{ mm}^2$ . The skin effect of the conductors is taken into account at a switching frequency of 35 kHz. The information regarding the distributed air gapped core is obtained from [39].

### 3.2.2 Bus Capacitor Design

The bus capacitors form the link between the two full bridge converters in the cell. The active rectifier draws a sinusoidal current from the supply and then feeds this rectified current  $i_{AR}$  into the bus capacitor and load. The load is defined as the second full bridge DC-DC converter, for the purpose of this analysis this load is defined as a DC current source  $I_S$ . This approximation is made as the frequency of the DC-DC converter is much higher than the frequency of the current entering the bus capacitors. Figure 3.7 shows the active rectifier with a current source as load.

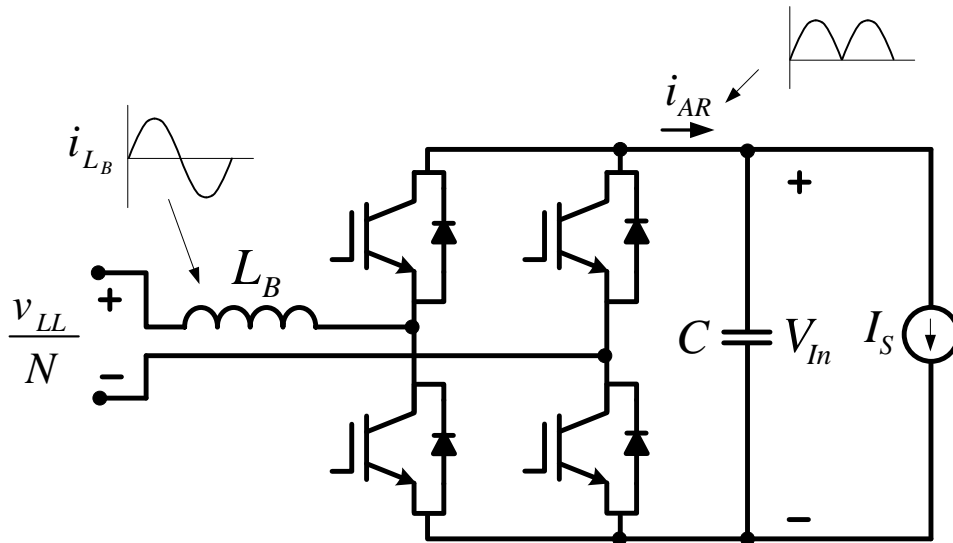


Figure 3.7: The active rectifier connected to a current source load

The active rectifier draws a sinusoidal current from the supply at the supply frequency, namely 50 Hz. The output current of the active rectifier  $i_{AR}$  is therefore at twice this frequency, namely 100 Hz. The shape of this current waveform is of the form  $I_p |\sin(\omega_1 t)|$ . The frequency of the current in rad/s is defined as  $\omega_1$ . At maximum power, the rms current  $I_{a(rms)}$  flowing into the rectifier amounts to 2.42 A from Equation 3.2. The peak current  $I_p$  is therefore equal to  $I_p = \sqrt{2} I_{a(rms)}$  at this rating, which is equal to 3.42 A. The DC current source  $I_s$  is assumed to have an amplitude of 2.2 A.

The switching frequency harmonic is also superimposed on this current waveform  $i_{AR}$ . The switching frequency  $f_s$  is however much higher than the fundamental and thus is ignored for the design of the bus capacitors. The bus capacitor  $C$  is designed according to the allowable ripple voltage on the bus voltage  $V_{In}$ . The design specifications of the bus ripple voltage, namely  $\Delta V_o$ , was limited to 100 V.

In the steady state, the change in voltage  $\Delta V_o$  of the bus capacitors is given as [8]:

$$\Delta V_o = \frac{\Delta Q}{C} \quad (3.16)$$

The integral of the capacitor current  $i_c$  is equal to the change in charge of the capacitor, namely  $\Delta Q$ . Referring to Figure 3.8, the change in charge  $\Delta Q$  is calculated by obtaining the area between  $i_{AR}$  and  $I_s$ .

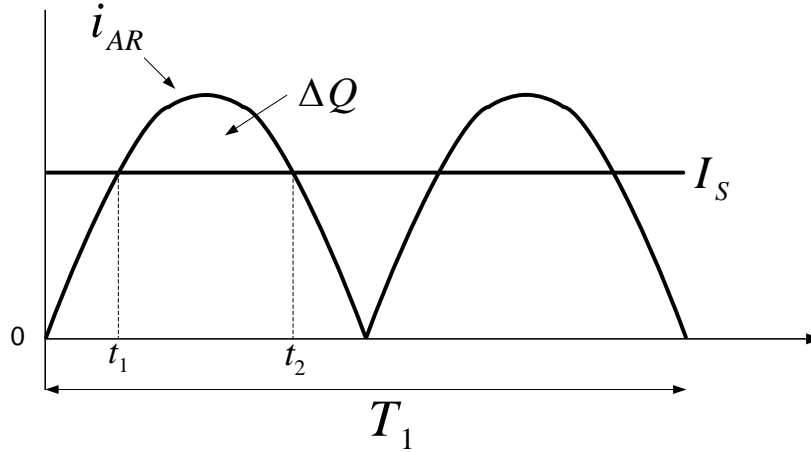


Figure 3.8: Calculation of  $\Delta Q$  of the bus capacitor  $C$

The period of the supply voltage is defined as  $T_1$ , and thus the time intervals  $t_1$  and  $t_2$  are given as:

$$t_1 = \frac{\arcsin\left(\frac{I_s}{I_p}\right)}{\omega_1} \quad (3.17)$$

$$t_2 = \frac{T_1}{2} - t_1 \quad (3.18)$$

The change in charge of the bus capacitor  $C$  is given as:

$$\begin{aligned} \Delta Q &= \int_{t_1}^{t_2} I_p \sin(\omega_1 t) dt - \int_{t_1}^{t_2} I_s dt \\ &= \int_{2.3m}^{7.7m} 3.42 \sin(\omega_1 t) dt - \int_{2.3m}^{7.7m} 2.2 dt \\ &= 4.405 \text{ mC} \end{aligned} \quad (3.19)$$

The bus capacitance  $C$  is calculated by substituting Equation 3.19 into Equation 3.16 and noting that the maximum ripple voltage  $\Delta V_o$  is designed as 100 V. The minimum capacitance required for the bus capacitors is given as:

$$\begin{aligned} C &> \frac{\Delta Q}{\Delta V_o} \\ &> 44.05 \text{ uF} \end{aligned} \quad (3.20)$$

The bus capacitance is therefore chosen as 50  $\mu\text{F}$ ; the bus is comprised of four 50  $\mu\text{F}$  900 V capacitors. Two capacitors are connected in series, thus the capacitance drops to 25  $\mu\text{F}$ , another series string is therefore connected in parallel to increase the bus capacitance to 50  $\mu\text{F}$ .

The maximum ripple voltage  $\Delta V_o$  is calculated for a 50  $\mu\text{F}$  capacitor using Equation 3.19, and it amounts to  $\Delta V_o = 88.11$  V. A Simpler simulation was run to justify the size of the bus capacitors. This simulation utilized a sinusoidal input current  $i_{AR}$  of the shape  $I_p |\sin(\omega_1 t)|$  and a DC current source, namely  $I_s$ . Figure 3.9 illustrates the model used in the simulation.

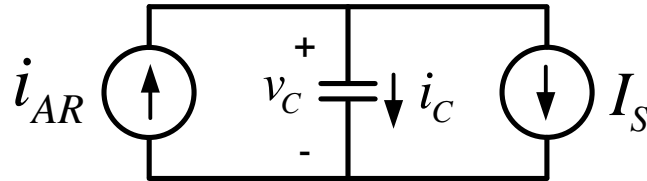


Figure 3.9: Simulation model

Figure 3.10 shows the superimposed voltage ripple  $v_c$  on the bus capacitor  $C$  as well as the capacitor current  $i_c$ . The simulation depicts a ripple voltage  $\Delta V_o$  of 89 V, which concurs with the theoretical prediction.

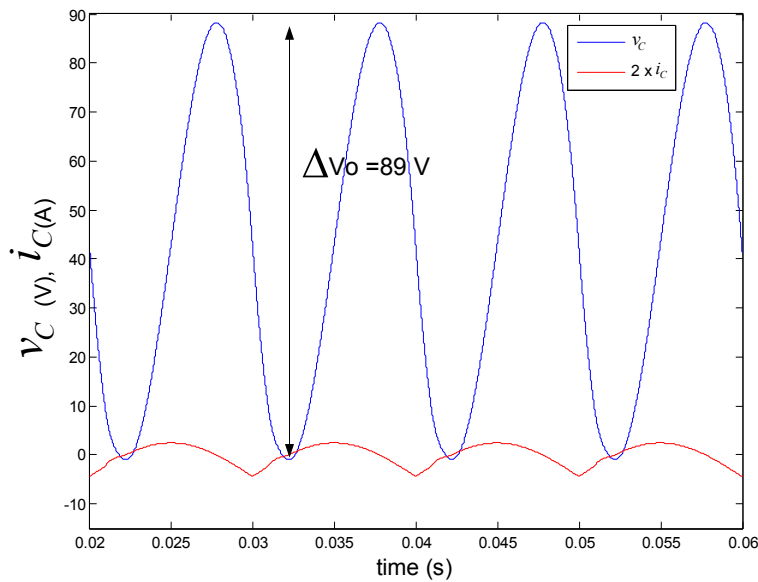


Figure 3.10: Ripple voltage across the bus capacitor

### 3.3 Auxiliary Circuits

The modular cell requires auxiliary circuitry for the cell to function; these circuits include the gate driver circuitry and the FPGA controller. These auxiliary circuits require power to function

and therefore a power supply is required for each cell. Referring to Figure 3.3, the auxiliary circuit is grounded between the two bus capacitors and is defined as the digital ground  $DG$ . Thus, each cell's  $DG$  is roughly 1.3 kV from the next  $DG$  of the following series stacked cell. A self-sustaining power supply is therefore required for each cell due to the different voltage potentials. The reliability of this power supply is of extreme importance in order to keep the SST functioning correctly. The status and control of the cell are lost if the power supply fails, and this would require the whole SST to shut down immediately.

There are many methods of building such a power supply, but the reliability of these converters is questionable. This supply can be achieved by adding an auxiliary winding on each transformer for the power supply. The duty cycle of the main DC-DC converter is therefore not allowed to operate at a 0% duty cycle. Other options exist, which reduce the bus voltage  $V_{In}$  with series resistors, this option is however extremely inefficient and bulky to implement in practice.

The proposed solution is to build an independent DC-DC converter that uses a custom built isolation transformer. This transformer has a single primary winding and 15 secondary windings, one secondary winding for each cell. This transformer therefore requires a large isolation barrier between windings. The LV grid voltage is proposed to power the converter, thus its start-up condition is of no concern. The auxiliary supply is however beyond the scope of this thesis, thus, each cell is temporarily powered by batteries which float at the relevant potentials. The main auxiliary circuits are described below.

### 3.3.1 The Controller

The main controller of the SST comprises three field programmable gate array (FPGA) devices, each of which controls a phase arm of the SST. The main controller communicates with each individual cell regarding the status and control of the cell. Fibre optic transmitter and receiver pairs are utilized to communicate between the cell and the main controller. The main controller is also responsible for the start-up control sequence of the SST.

Each individual cell is controlled by an FPGA device, which measures the operating conditions and is responsible for the control of the cell. The cell controller block diagram is shown in Figure 3.11.

The controller transmits 16 PWM gate signals to the gate drive circuit, in other words, two signals per IGBT. The status of the cell is obtained by measuring the bus voltage  $V_{In}$ , the primary current  $i_P$  and the heatsink temperature  $t_h$ . The bus voltage is measured differentially and the primary current is measured with a LEM sensor, as this sensor provides sufficient galvanic isolation.

These analogue measurements are converted to a digital value using multiple analogue to digital converters (ADC). The duty cycles of the active rectifier as well as the DC-DC converter are received from the main controller. The general status of the cell is sent back to the main controller, thus establishing a two way communication protocol. The FPGA also has control over the heatsink cooling fan, and it switches of the fan under light load conditions, thereby increasing the efficiency of the SST. The controller discussed above was designed by Francois Breet.

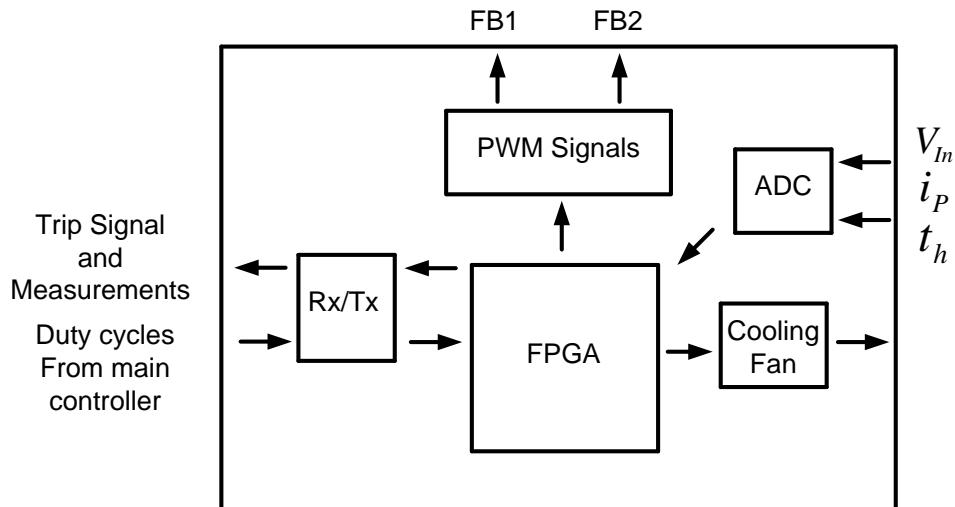


Figure 3.11: FPGA controller

### 3.3.2 Fault Condition and Monitoring

Three main fault conditions can occur in the cell; an over voltage can occur on the bus voltage, a short circuit can occur on the secondary side of the transformer, or there can be shoot through of the IGBTs in either half of the full bridge. An over voltage of the bus voltage  $V_{In}$  causes the voltage margin of the IGBTs to decrease, thus the IGBTs no longer operate in their safe operating area (SOA). The double loop control strategy is proposed to hold the bus voltage relatively constant in steady state operation. A DC dump circuit is however proposed in the second iteration of the cell to prevent the occurrence of an over voltage.

In the case of a short circuit on the secondary of the transformer, this will increase the primary current  $i_P$  significantly. The impedance of the reflected secondary circuit is therefore reduced to the single leakage reactance  $L_\sigma$  of the transformer. This current  $i_P$  is a measured operating condition, thus should a short circuit occur, then the gate signals of the IGBTs are switched off. The time required to stop the fault current is mainly dependent on the bandwidth of the current sensor. An analogue trip circuit is also used in parallel with the controller in the case of a short circuit [40]. This is done because the analogue circuit reacts faster than the analogue to digital converter and controller combined.

The third type of fault is the possible shoot through of the switches; in other words, both high side and low side switches are on, thereby causing a short circuit. The impedance that the fault current observes is the stray inductance of the tracks, and this impedance is much smaller than the leakage inductance  $L_\sigma$ . The bus voltage  $V_{In}$  is therefore shorted, causing large currents to flow through the IGBTs.

The current flowing through a conducting IGBT is proportional to the on-state forward voltage across the device. Thus, by measuring the  $v_{ce}$  voltage of the IGBT while the device is conducting, the amplitude of the collector current is known. This method is known as desaturation protection. The IGBT is therefore turned off if the  $v_{CE}$  voltage increases beyond the specific limits.

The additional circuitry for de-saturation protection consists of an external diode, which is required to have a voltage rating of the bus voltage  $V_{In}$ . The physical routing of this circuitry adds complexity to the design, as all three IGBT terminals are routed to the gate driver PCB. This routing is problematic at such high voltage levels and the limited availability of fast switching 1 700 V diodes is of concern. This additional circuitry is therefore not feasible for the two full bridges of the cell. Consequently, alternative methods are used in the gate driver circuit to prevent shoot through of the IGBTs.

### 3.3.3 Gate Driver Circuitry

Inexpensive off-the-shelf gate drivers for 1 700 V IGBT modules are not available, although gate drivers for 1 200 V IGBT modules are; as a result, it was necessary to custom build the gate drivers. Two options of gate driver circuits are considered, namely the bootstrap gate driver and the isolated gate driver using optocouplers. The bootstrap circuit is relatively simple and easy to implement although no isolation is offered. The bootstrap circuit is also largely dependent on the quality, cost and availability of the 1 700 V fast reacting diode. This circuit is furthermore not isolated thus if the diode fails, the probability of destroying all the electronic circuitry is high. The bootstrap circuit is therefore not viable at these voltage ratings.

The isolated gate driver circuit operates optically with the use of optocouplers that have adequate isolation ratings. Optocouplers have two grounds, namely the digital ground  $DG$ , which is connected to the controller and the floating ground  $FG$ , which is isolated from the  $DG$ . The disadvantage of using these devices is that an isolated supply voltage is required for each optocoupler. Nonetheless, it was decided to use optocouplers due to the isolation they offered, regardless of the extra complexity.

The gate signal of each IGBT is required to be 15 V higher than its emitter voltage, and so a floating potential is required to switch each IGBT. The digital ground  $DG$  can be connected to the negative of the bus voltage  $V_{In}$ , and the low side drivers would thus not require any isolation. However, the high side drivers would require an isolation barrier equal to the bus voltage  $V_{In}$ .

The direct connection between the low side gate signal and the FPGA is not considered due to the voltage levels present in the system. Thus, both high and low side drivers are isolated from the controller. Referring to Figure 3.12, the digital ground  $DG$  is chosen to be between the bus capacitors. This allows equal isolation requirements between the high and low side drivers, namely  $\frac{V_{In}}{2}$ .

The gate signals are optically transmitted over this isolation barrier with optical gate drivers. The implemented gate driver, in this case the ACNWN130 from Avago, has a continuous isolation rating of 1.4 kV [41]. The gate signal circuitry is shown in Figure 3.13; note that the digital ground  $DG$  is separated from the floating ground  $FG$ .

The utilization of de-saturation protection is not used in this setup, thus the gate driver circuit is designed to prevent the occurrence of shoot through of the IGBTs. Furthermore, sufficient noise rejection is required to avoid false triggering of the IGBTs. The LED of the optocoupler is operated differentially, thus two signals are required for each IGBT. Differential signals are used due to the noise present in the converter. The main noise component in the converter is caused



by the high  $\frac{dv}{dt}$  ratings. The gate drive signals are therefore routed differentially to increase the noise rejection.

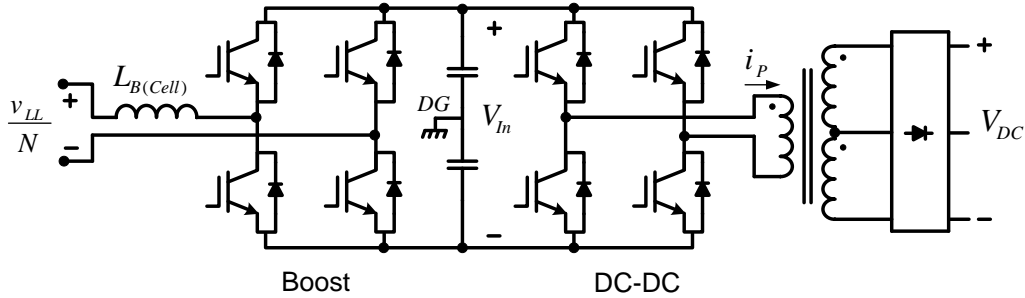


Figure 3.12: Cell schematic

The noise is present on both signals, and thus the difference of the two signals rejects the noise and the expected signal is obtained. A ribbon cable is used to transfer the signals from the controller to the gate driver PCB. These differential signals are wired with a ground connection between the signals, in order to minimize inductive and capacitive coupling. Noise is also created by large  $\frac{di}{dt}$  ratings, which induces a voltage in any loop; this is similar to the operation of a transformer. In this way, possible loops are avoided or minimized.

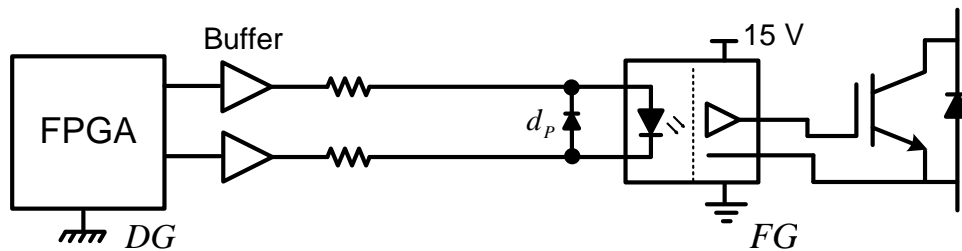


Figure 3.13: Differential gate signals

The differential configuration also solves the uncertainty of the general purpose input output pins (GPIO) while the FPGA boots. As the device is booting, both GPIOs will be at the same potential, and thus no current will flow through the LED. The code of the FPGA is also written in such a manner that the high and low side drivers are not enabled on initialization of the FPGA. This is seen in Figure 3.14, where the device starts operating at  $t = 32 \mu s$ . The figure shows that the high and low side gate signals are not on simultaneously when the FPGA starts to operate. The dead time is also seen to be in operation immediately.

The gate drive circuitry is also designed in such a way that the LED is reverse biased when the signal is required to be off, which is the function of the anti-parallel diode  $d_P$  over the LED. This improves the noise margin, as the voltage over the LED is negative in the off state.

The buffer circuit has an enable pin, which is pulled high while the FPGA boots. This buffer is only enabled after the FPGA booting process is complete. The dead time between the IGBTs is also set large enough to prevent shoot through of the high and low side IGBTs. The

length of the dead time is determined by the propagation delays in the circuitry as well as by the switching times of the IGBTs. These precautionary measures are taken because there is no current protection in the event of shoot through of the IGBTs.

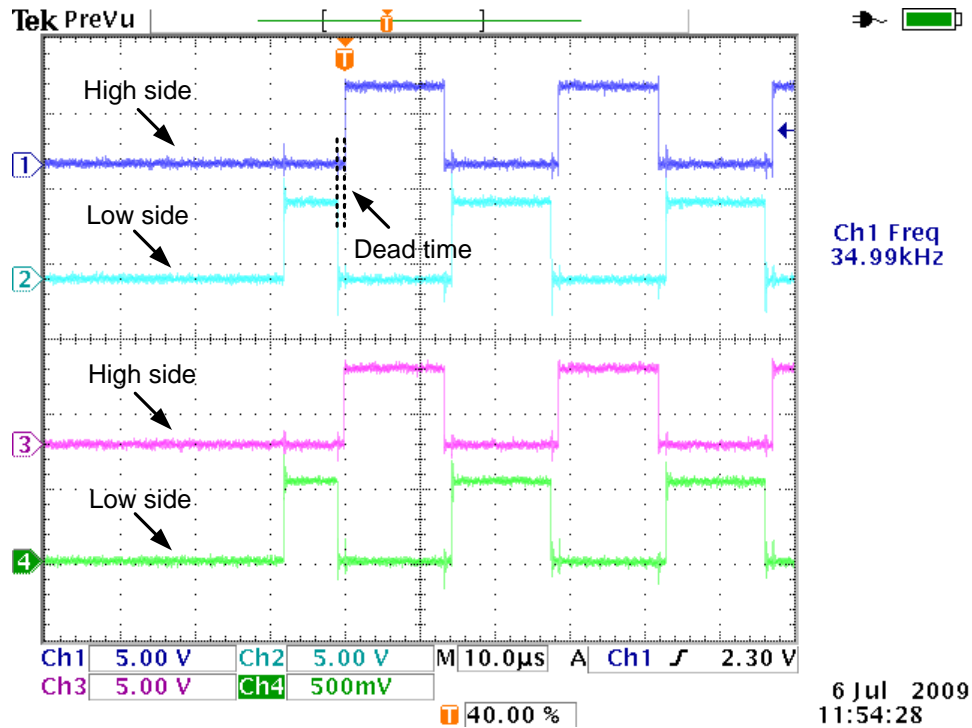


Figure 3.14: The gate signals after the FPGA has finished booting

### 3.3.4 Isolated Power Supply

The gate driver circuit is built using an optocoupler, moreover, a floating supply is required for each optocoupler. These isolated supplies can be purchasable in a single package, but they are expensive and often the isolation is not rated at a continuous operation voltage. Eight of these supplies would be required for the two full bridges in the cell. These devices are PCB mounted, and so the development costs of the PCB would need to be incorporated too. To reduce the costs and to ensure adequate galvanic isolation, it is decided to design and implement the eight isolated supplies onto a single PCB by using a custom built DC-DC converter.

The options that are considered are the push-pull converter, the flyback converter and the half bridge converter. The main design specifications of these supplies are their reliability and their ease of manufacturing. The cost of these supplies is also a consideration, because 8 supplies are required per cell; 45 cells would therefore require 360 isolated supplies. Lastly, the time required to wind the toroids is the greatest labour concern.

The flyback converter requires an airgap in the core, which means that a gapped ferrite core or a distributed core is required. The gapped ferrite core would need to be implemented using an E-core, which would require the windings to be wound on top of each other. Adequate isolation

would furthermore be required between the windings, and thus the safer option would be to use a distributed core. The distributed core is available in a toroidal form, thus the windings can be placed next to each other, thus facilitating greater isolation. However, the windings on a flyback transformer have a specific polarity, which complicates the manufacturing process.

The push-pull converter has a complex winding on the primary, as two windings are joined together to form the primary. Moreover, the windings also have a specific polarity, the winding thereof is time consuming. The advantage of this converter is that the gate signals are obtained without a bootstrap circuit. Nonetheless, a more complicated driver chip is however required to prevent the saturation of the core.

The half bridge converter however does not saturate due to the balancing mechanism provided by the bus capacitors. This converter requires a single winding on the primary and one on the secondary if a full bridge rectifier is used on the secondary. The polarity of the winding in this configuration is also irrelevant, which simplifies the manufacturing process. However, this converter however does require the full primary current to flow through the bus capacitors, which is not the case in the other types of converters. The half bridge converter requires the least number of windings per isolated supply, and so more isolated supplies can be wound on the same toroid. In view of the above, this converter is chosen for the isolated supply.

The half bridge driver circuit is designed in such a way that the amount of external components required is reduced. The cost and complexity of the PCB design is furthermore reduced as the number components on the PCB are decreased. The IR2184 from International Rectifier is chosen for the gate driver, as it has a built-in bootstrap diode and only requires three external components [42]. The concept of the isolated supplies is shown in Figure 3.15. The transformer is shown to have five windings, one primary and four secondary's. All the isolation supplies for one full bridge are wound on one toroid. A photo of the isolated supply is shown in Figure 3.18.

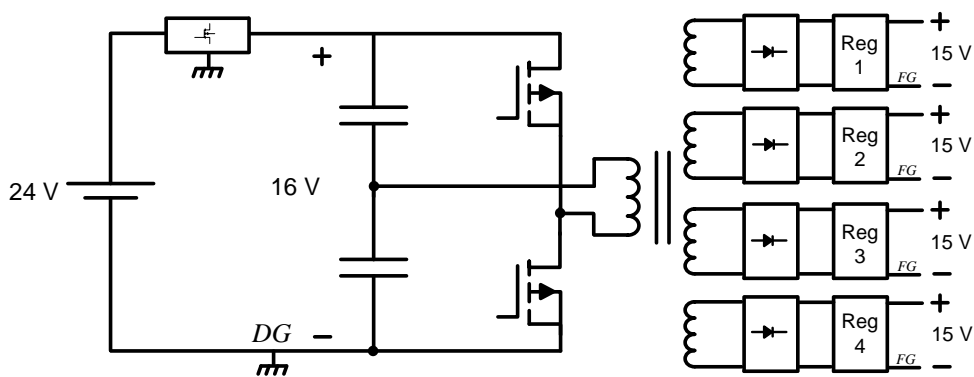


Figure 3.15: Isolated supply

The isolated supply obtains its power from a 24 V battery; this voltage is stepped down to 16 V using a switching regulator. This is done to maintain a stable voltage over the bus capacitors with regard to the battery voltage. The half bridge converter operates at a switching frequency of 80 kHz, with a constant duty cycle of 49%. The input and output voltages of the

half bridge converter are 16 V and 20 V respectively. The output voltage of the half bridge converter is therefore fed through a 15 V linear regulator to obtain the 15 V supply.

The transformer is designed in the same manner as the transformer in Section 3.2.1. An r25 toroid is used with N27 core material, the effective area of the core is  $51.26 \text{ mm}^2$ . The number of turns on the primary and secondary windings is calculated as 5 and 14 respectively.

### 3.4 Mechanical Design of the Cell

Figure 3.16 depicts the first iteration of the modular cell. The structure on the left of the transformer is the section containing the back-to-back converter. Eight IGBTs are mounted on the heatsink, in other words, four for each full bridge. The IGBTs are mounted in a staggered configuration, as shown in Figure 3.17. The purpose of this is to allow the heat to conduct equally across the heatsink. An off-the-shelf heatsink is used, namely the HE-5 from Semikron.

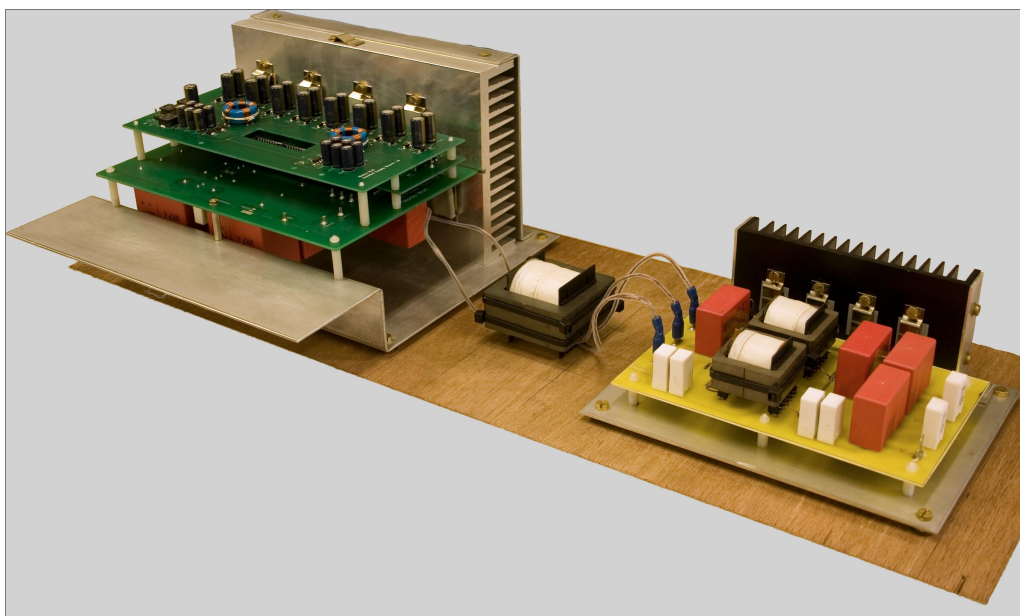


Figure 3.16: The first iteration of the cell, which was built by the author

The three PCBs are staggered above one another in a piggy back configuration. The bottom PCB is the power plane where the IGBTs, bus capacitors and current sensor are placed. The PCB directly above it is the gate driver circuit, while the PCB on top is the isolated supply. This configuration improves the clearances between the different PCBs, due to the high voltages present in the system. The routing is simplified with this configuration as the auxiliary circuits are separated from the power plane. The following subsections describe the specific components in Figure 3.16.

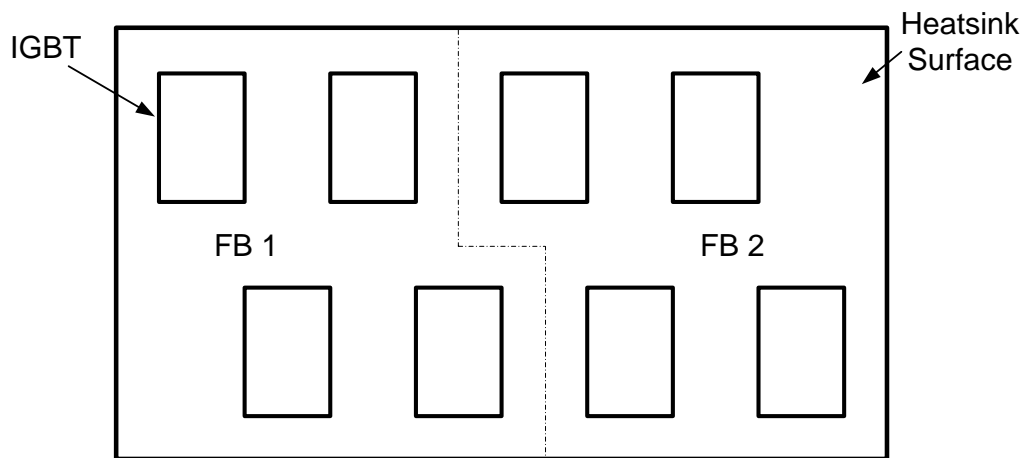


Figure 3.17: IGBT placement on the heatsink

### Isolated Supply PCB

The isolated supply PCB consists of two half bridge converters with each half bridge converter producing four isolated power supplies. Figure 3.18 depicts the isolated supply PCB, and a clear distinction can be seen between the digital and floating grounds. The windings on the toroid are also spaced equally apart for isolation purposes. The continuous isolation between windings is in the order of 2.5 kV. The isolated supply voltages are transferred to the gate driver PCB using pins and receptacles, which are custom made for piggy back applications.

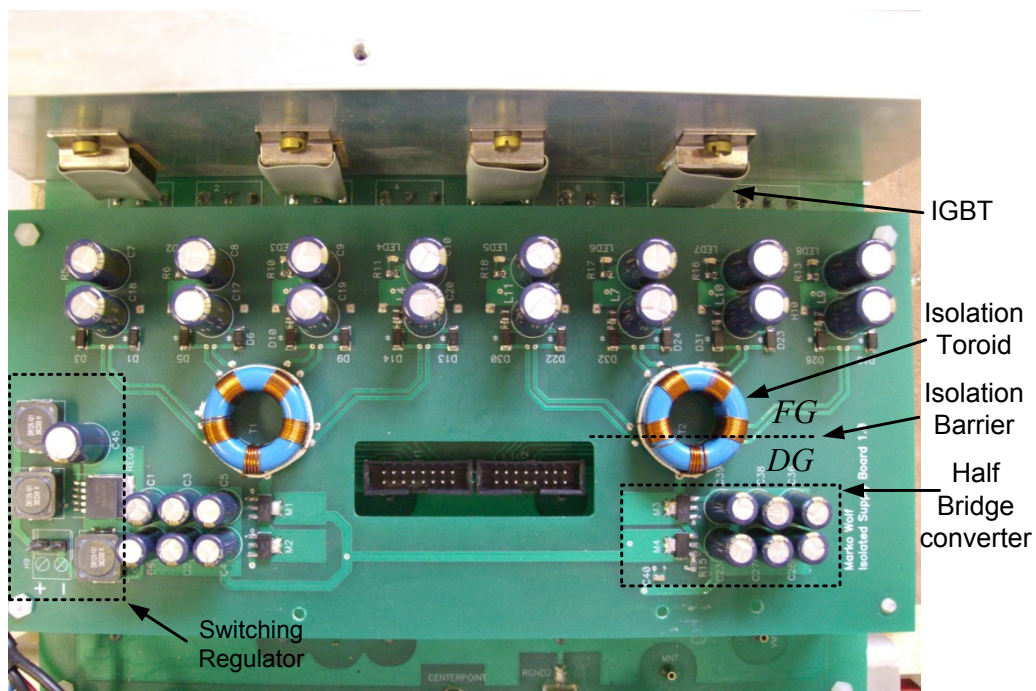


Figure 3.18: Isolated supply PCB

### Gate Driver PCB

The gate driver PCB is shown in Figure 3.19. Two 16 pin box headers are used to receive the PWM signals from the FPGA. These signals are then differentially routed between the box header and the optocouplers. The digital and floating grounds are separated at the optocouplers. The receptacles into which the pins are inserted, from the isolated supply PCB are also seen in the figure.

The output of the gate driver is placed in series with two anti-parallel diodes and gate resistors. This allows for the turn-on and turn-off switching times to be altered independently because two gate resistors are used. The gate signals are also transferred to the power plane using pins and receptacles.

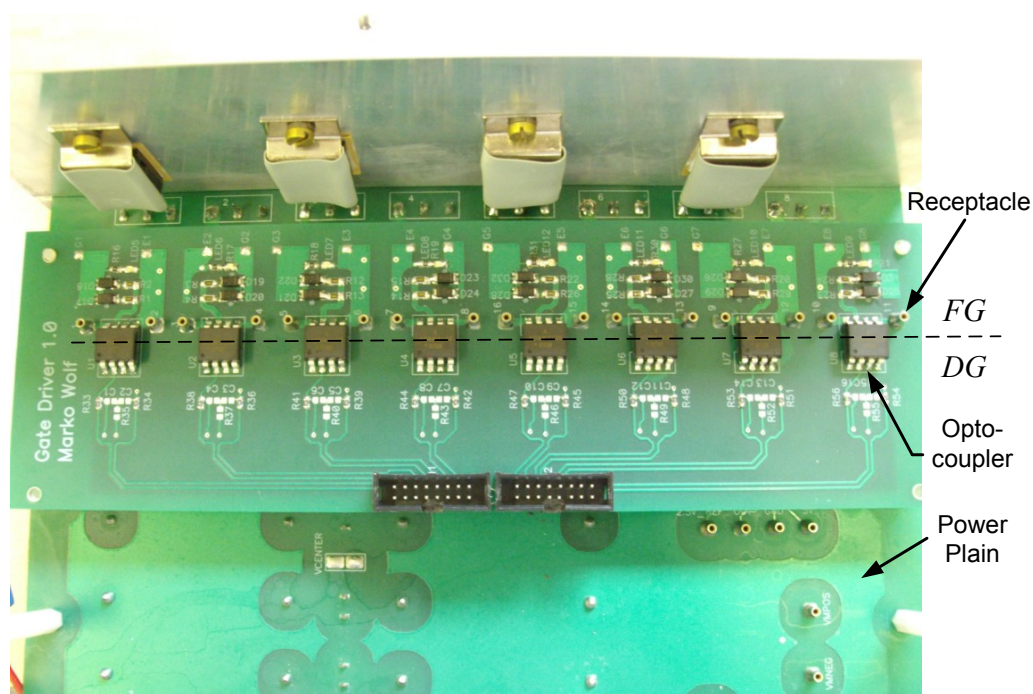


Figure 3.19: Gate driver PCB

### Power Plane PCB

A section of the power plane is shown in Figure 3.19. The large clearances between connections are visible. The ground layer polygon has a clearance of 5 mm near the bus capacitors and 3.5 mm near the IGBTs. This clearance is reduced due to the density of tracks near the IGBTs. The bus capacitors and other components are mounted on the bottom of the power plane PCB, this is seen in Figure 3.16. This is done because the mechanical clearance between the power plane and gate driver is insufficient.

The tracks between IGBTs are kept as short as possible to reduce the parasitic inductance between connections. Snubber capacitors are placed as close as possible to the IGBTs to counter this stray inductance. Four  $0.22 \mu\text{F}$  2000 V snubber capacitors are used, two for each full bridge.

### 3.5. CONCLUSION

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The four bus capacitors are placed directly behind the snubber capacitors. The bus capacitors on the power plane are comprised of series linked 900 V 50  $\mu$ F polypropylene capacitors.

All the PCBs of the cell are built using two layer boards, in order to save on costs. The modular cell is therefore built keeping costs into consideration, as a large number of these cells need to be manufactured. The two layer board complicated the routing of the power plane, as a separate ground and Vcc plane were not available. The signals as well as the polygon planes were therefore optimized onto a two layer board.

#### **The Transformer**

The transformer seen in Figure 3.16 is an E65 transformer set from EPCOS. This transformer is wound using enamel insulated copper windings, which are insulated from each other using Kapton tape. The isolation breakthrough voltage between the primary and secondary windings was measured; it broke through at 10.5 kV. As this is a prototype transformer, it is not designed to have an isolation of 75 kV. The connections between the transformer and both PCBs are done using blades and female shrouded connectors.

#### **Rectifier PCB**

The portion to the right of Figure 3.16 is the full bridge center tapped rectifier. The four 1200 V rectifier diodes are mounted onto the heatsink. The bus capacitors are noted on the right of the rectifier (red Wima), whereas the Wima capacitors on the left are the 470 nF snubber capacitors. The two cores seen on the rectifier are the two filter inductors made using distributed air gapped cores. These inductors have an inductance of 1.3 mH at a current rating of 3.3 A.

A second iteration of the rectifier PCB was built, to improve the operation of the snubber circuit. The optimized snubber circuit is a conventional over voltage snubber with a resistor connected in series with the snubber capacitor. The mechanical construction of the PCB is similar, the only difference is that the bleeding resistors are mounted onto the heatsink for cooling purposes.

## **3.5 Conclusion**

The different stages of the SST were discussed, specifically the input stage, the isolation stage and the output stage of the SST. Special attention was paid to the design of the back-to-back converter used in the modular cell. The design of the individual components in the cell was discussed; these components included the high voltage transformer, the boost inductor and the bus capacitors. The mechanical construction of the back-to-back converter was explained and photographs of the modular cell were given.

## Chapter 4

# Isolation Stage

The isolation stage of the cell is defined as the section that transfers power across the isolation barrier. This stage is comprised of a high voltage DC-DC converter, which includes a step-down isolation transformer and a passive rectifier on the secondary of the transformer. Figure 4.1 depicts the isolation stage highlighted in black, whereas the rest of the cell is depicted in gray. The DC-DC converter converts the voltage from 1 200 V to 800 V, the primary bus voltage is obtained from the active rectifier and the output voltage is fed into the 3-phase DC-AC inverter.

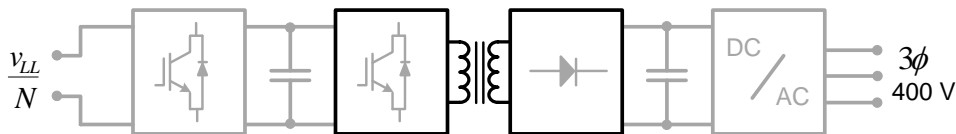


Figure 4.1: Isolation stage of the cell

The frequency of the DC-DC converter is the factor that makes the whole SST feasible; simply put the higher the frequency, the smaller the transformer. This high switching frequency has many disadvantages for the converter, such as switching losses, overshoot on the primary switches and the skin effect of the conductors. The maximum switching frequency is determined by the trade-off between these factors as well as by the allowable switching frequency of the switches.

The possible topologies of the DC-DC converter were either the half bridge or the full bridge converter. The advantage of the half bridge converter is that no DC offset occurs in the transformer primary voltage, but the full current flows through the bus capacitors. These capacitors therefore require a large capacitance to keep the center point voltage constant. As a result series stringed electrolytic capacitors would typically be required due to the high voltage and capacitance requirements.

The full bridge converter requires less bus capacitance, thus polypropylene capacitors could be used. These capacitors have notable advantages over electrolytic capacitors due to their lifetime and self-healing ability. The full bridge converter could however cause the transformer to saturate, due to a DC offset caused by unbalanced leg voltages. However, this problem can



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be resolved by adding an additional control loop to alter the DC offset. In view of the aforesaid, the trade-off was made between the bus capacitors vs silicon, and the full bridge topology was chosen for the design.

The switches used in this converter are 1 700 V IGBTs, these devices are chosen because mosfets are unfortunately not available at this voltage range. The IGBTs are chosen according to their blocking voltage, switching frequency and package size. The current that is required to flow through the device is relatively small, and thus is not a major concern in influencing the selection of a suitable IGBT. The switching losses are also reduced due to the IGBTs' fast rise time of 60 ns. The chosen 1 700 V IGBT is furthermore available in a T0-247 package. This is an advantage, as the size of the full bridge is reduced, as opposed to using bulky IGBT modules.

Multiple topologies of full bridge DC-DC converters are available in the literature. These converters offer favourable operation conditions, such as soft switching and satisfactory efficiencies. Soft switching is obtained by turning the switches on or off under zero voltage (ZVS) or under zero current (ZCS) conditions. This allows converters to achieve much higher switching frequencies, as the losses are reduced. Zero volt switching is typically achieved by the interaction between the parasitic switch capacitances and the leakage inductance of the converter. Zero current switching is realized by allowing the leakage inductor to discharge fully or to reset this current actively by using clamping circuits or saturable inductors [24].

Zero current switching of all the switches over the full load region is realized in a DC-DC converter built in [25]. This is achieved by using a circuit on the secondary side of the transformer; this contains an active switch that resets the primary current to zero before commutation. This topology also allows soft commutation of the rectifier diodes, which is a notable advantage. This converter has excellent properties, but the addition of an active circuit on the transformer secondary complicates the topology considerably. The converter built in [26] utilizes the magnetization current of the transformer to aid the ZVS mechanism. The load region where ZVS switching occurs is therefore increased. This is done by using two transformers, connected in series, on the primary side of the converter.

Other researchers obtain soft switching using ZVS, ZCS or a combination of the two, namely ZVZCS [24; 27]. However, these converters do not ensure soft switching over the entire load region, which means that soft switching is lost at lighter loads. Although these topologies utilize different configurations, similar efficiencies are however obtained.

These topologies often include additional auxiliary windings and active switches on the secondary side of the transformer. The isolation transformer in each cell of the SST is required to have an isolation of 75 kV [12], and thus adding an active switch on the secondary side of the transformer would complicate the topology. This switch would typically be controlled optically, which means that an increased number of components would be required, which is a disadvantage in a modular design.

These topologies maintain soft switching as the load varies, however, the additional circuitry is complex. In selecting the most suitable topology, this complexity is weighed up against the switching losses. Should soft switching be lost at lighter loads, then the switching losses would also be reduced, as the current is less. The conduction losses are almost more substantial than

the switching losses due to the high forward voltage  $V_{on}$  of the 1 700 V IGBTs. The additional circuit complexity is therefore not viable, if the switching losses are taken into account.

Consequently the simplest and most reliable DC-DC converter topology is chosen, namely the phase shifted full bridge (PSFB). This converter requires no active switches or auxiliary windings to obtain soft switching. The mechanical construction of the PSFB is identical to that of the bipolar switched full bridge converter. The PSFB utilizes phase control, as opposed to the duty cycle control used in bipolar PWM converters. The specific converter utilizes a step-down center tap transformer, which has one primary winding and two secondary windings. Furthermore, the two secondary windings are connected in series, with the connection point of the two windings defined as the center point. The two halves of the secondary rectifier are therefore symmetrically separated due to this center point.

This converter utilizes the inherent transformer leakage inductance  $L_\sigma$  to obtain ZVS. The energy stored in the leakage inductance  $L_\sigma$  discharges the voltage across the switches on all the turn-on transitions. This soft switching is however only obtained if sufficient energy is stored in the leakage inductance  $L_\sigma$ . The energy in this inductance is proportional to the square of the current, and thus ZVS switching is lost at lighter loads. As the primary current decreases, the soft switching of the right leg is lost first, followed by that of the left leg. The legs of the full bridge are shown in Figure 4.2.

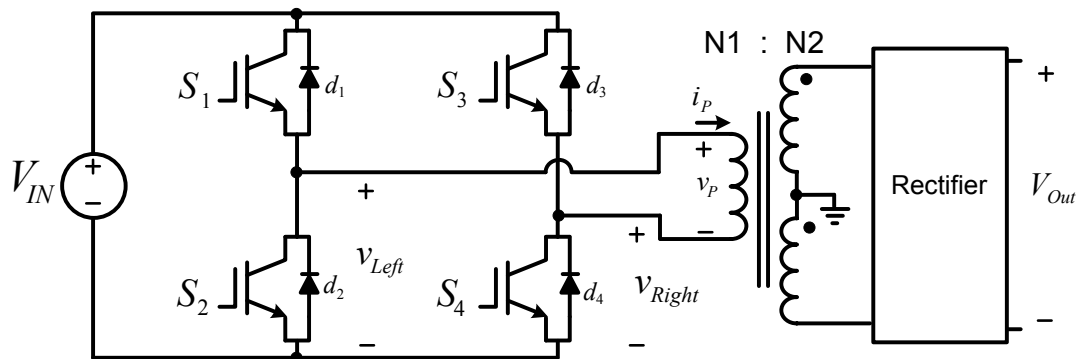


Figure 4.2: Ideal circuit diagram of the PSFB

These soft switching transitions are also dependent on the amount of time between transitions; thus, if the dead time is set too large, then ZVS switching cannot be obtained. The converter does not have over current protection against shoot through in either of the legs of the full bridge, thus the dead time is set within limits to prevent such an occurrence happening. The dead time is therefore set in such a manner as to obtain ZVS of the left leg and ZCS of the right leg. Zero current switching is obtained by allowing the leakage inductance to discharge fully before the right leg switches are commutated. These soft switching transitions are explained in further detail as the chapter commences.

## 4.1 PSFB Converter Operation

The output voltage of the PSFB converter is phase controlled, thus the duty cycle is proportional to the phase angle  $\theta$ . The PSFB operates on the principle of switching the left and right leg switches at a 50% duty cycle. With reference to Figure 4.2, the left leg switches are defined as  $S_1$  and  $S_2$ , with  $S_3$  and  $S_4$  being the right leg switches. The phase angle  $\theta$  between the two leg voltages is proportional to the primary transformer voltage  $v_P$ . Figure 4.3 depicts the ideal leg voltages as well as the transformer primary voltage  $v_P$  at a specific value of  $\theta$ . The transformer voltage  $v_P$  is the difference between the two leg voltages, thus the effective duty cycle increases as the phase angle  $\theta$  increases. These leg voltages are shown by ignoring the effects of the parasitic components present in the circuit.

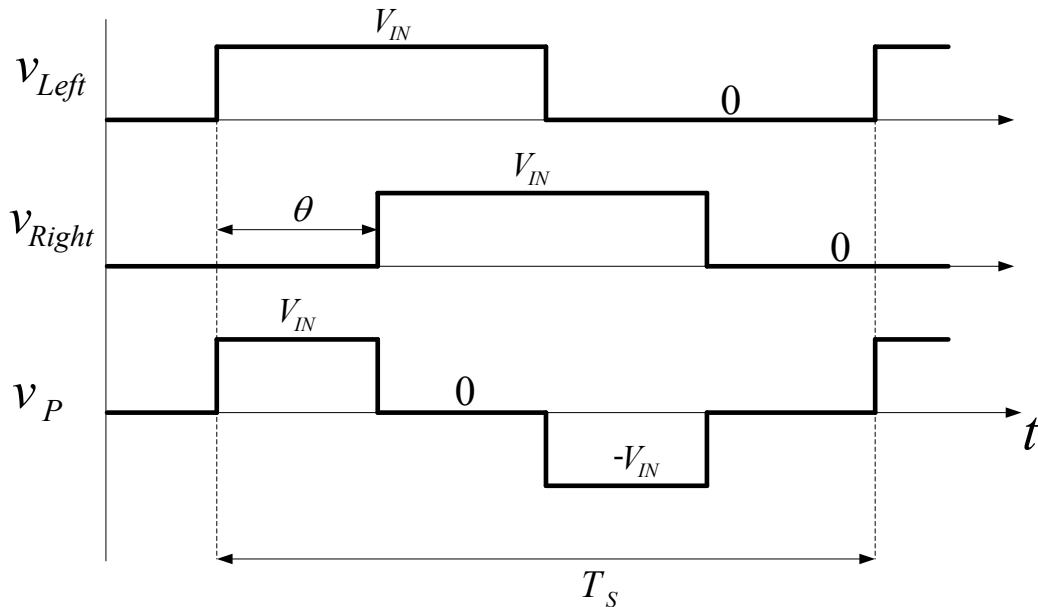


Figure 4.3: Ideal operation of the PSFB

The range of  $\theta$  is defined from  $0$  to  $180^\circ$  and the effective duty cycle is given by:

$$d_{DC-DC} = \frac{50 \cdot \theta}{180} \% \quad (4.1)$$

The transfer function of the converter using a full bridge rectifier is given as:

$$\frac{V_{Out}}{V_{In}} = 4 \cdot \frac{N_2}{N_1} \cdot d_{DC-DC}$$

The measured transformer voltage  $v_p$  and the primary current  $i_P$  waveforms for a complete cycle are shown in Figure 4.4. These waveforms are different to the ideal waveforms in Figure 4.3 due to the interaction between the parasitic capacitances of the switches and the leakage inductance  $L_\sigma$  of the transformer. The interaction between these components allows the PSFB

to obtain ZVS. The magnetization inductance is ignored in this section, as its effect is only noticeable at lighter loads.

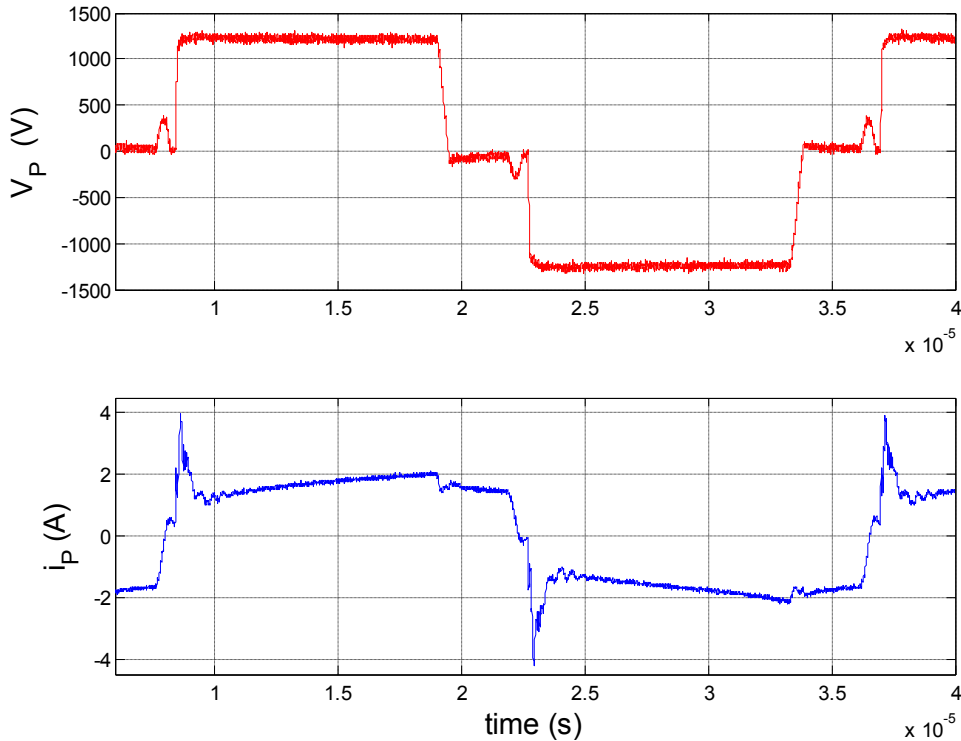


Figure 4.4: Transformer voltage and current at a bus voltage of 1.3 kV

A detailed description of these switching transitions, based on [43] is given in section 4.1.1-4.1.6 of this chapter, refer to this citation for a more comprehensive analysis of the waveforms, which occur in the converter. To assist in describing these transitions, the switching period  $T_s$  is separated into ten specific zones. These zones are defined in Figure 4.5. The gate signals of  $S_1 - S_4$ , as well as the transformer primary voltage  $v_P$  and current  $i_P$ , are included.

The converter operation is briefly summarised in the following paragraph,(see Figures 4.5 and 4.6 for the component classifications). In zones 2 and 7, the power is transferred across the isolation barrier to the load. Zone 3 is the left leg transition, and the energy in the leakage inductance  $L_\sigma$  discharges the left leg voltage  $v_{Left}$ , allowing soft switching of  $S_2$ . Zone 4 involves the freewheeling of the primary current, and thus the primary current  $i_P$  flows through  $S_4$  and  $d_2$ .

The right leg transition occurs in zone 5, and it is initiated when  $S_4$  is switched off. The energy remaining in the leakage inductance  $L_\sigma$  charges the right leg voltage  $v_{Right}$ . ZVS is obtained if  $v_{Right}$  is charged to the bus voltage  $V_{In}$  before  $S_3$  is switched on. This is generally not obtained due to the energy in the leakage inductance  $L_\sigma$  being insufficient, thus the primary current  $i_P$  discharges to zero in zone 5. Figure 4.5 depicts the primary current discharged to zero before  $S_3$  is switched on, thus an incomplete transition is shown and ZVS of  $S_3$  is not obtained.

Zone 6 is where the primary current ramps negatively which is followed by the second power transfer zone, namely zone 7. Zones 6 to 10 are identical to zones 1 to 5 only mirrored about the time axis, therefore these zones are not described in this chapter. The rectifier is also analysed in the respective zones that form the basis of the snubber design at the end of this chapter. The results of the snubber circuit are also included at the end of this chapter.

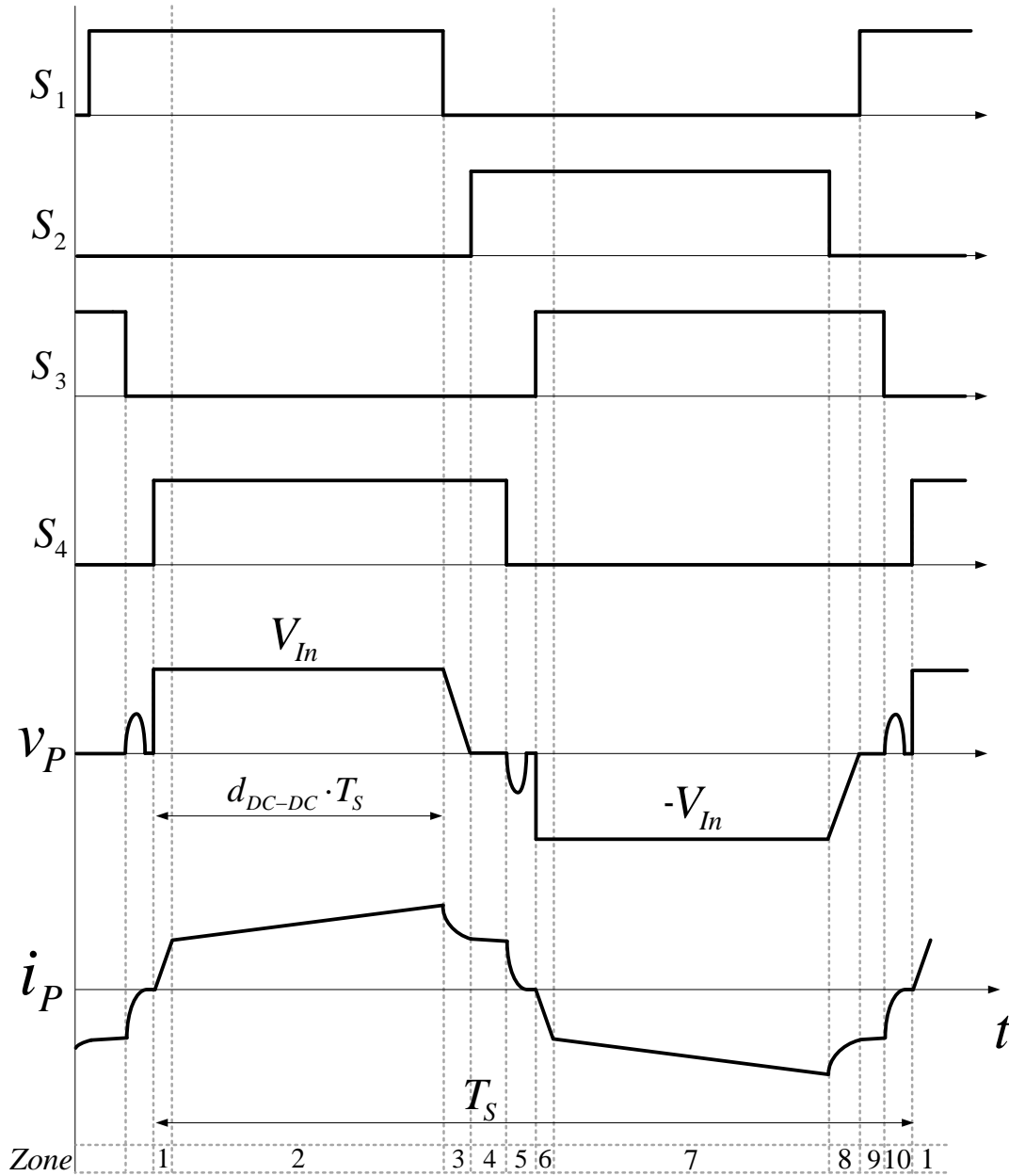


Figure 4.5: PSFB zones of operation

### 4.1.1 Full Bridge - Zone 1

Zone 1 is initialized by  $S_4$  switching on; note that  $S_1$  is already on. The primary current  $i_P$  is initially zero, as the leakage inductance is fully discharged in zone 10. Figure 4.6 depicts the current flow in the circuit at the beginning of zone 1. Initially all four diodes of the rectifier conduct the full secondary current, as the converter operates in continuous conduction mode.

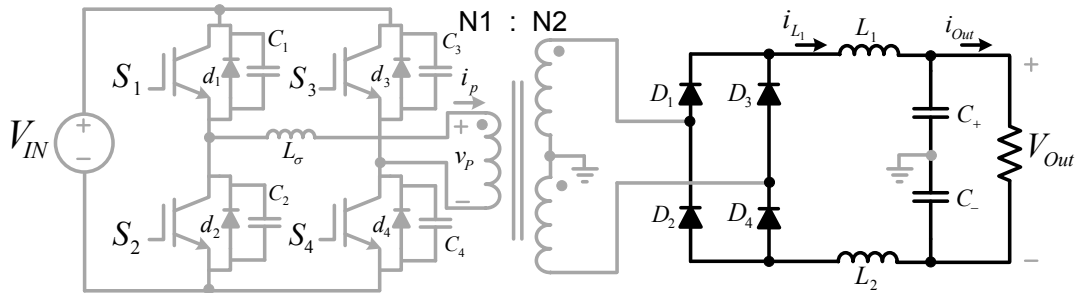


Figure 4.6: Initial current direction in zone 1

The transformer voltage is clamped to  $V_{In}$  due to  $S_1$  and  $S_4$  conducting, which causes the primary current  $i_P$  to increase rapidly. This current increases from zero until it reaches the positive reflected current of the filter inductor  $L_1$ , namely  $i_{L1} \frac{N_1}{N_2}$ . The gradient of the primary current  $i_P$  in this zone is characterized by  $\frac{V_{In}}{L_\sigma}$ . The direction of the primary current  $i_P$  as it starts to ramp up is shown in Figure 4.7. This figure depicts the primary current  $i_P$  before it reaches the reflected secondary current of the filter inductor  $L_1$ ; note that, until it reaches this point all four diodes continue to conduct.

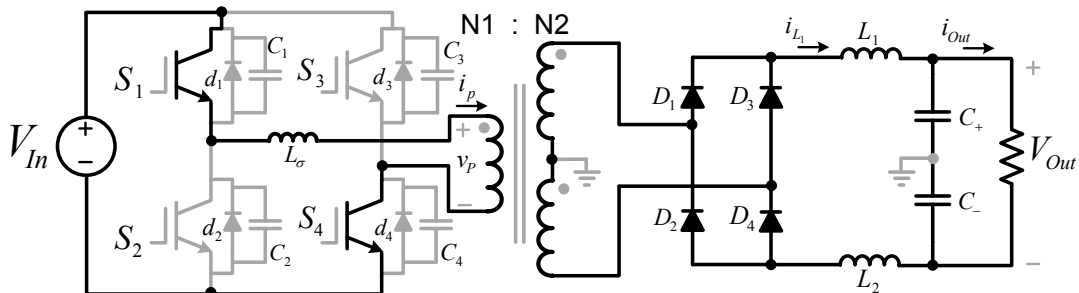


Figure 4.7: Current direction in zone 1 as the primary current  $i_P$  ramps positively

The end of zone 1 occurs when the primary current reaches the reflected secondary current of the filter inductor  $L_1$ . Diodes  $D_2$  and  $D_3$  are reverse biased as soon as the primary voltage  $v_P$  is clamped to  $V_{In}$ , which means that the diodes switch off and allow the full current to flow through  $D_1$  and  $D_4$ . The excessive ringing voltage of the diodes occurs at the end of this zone, which is described in the snubber design at the end of this chapter.

### 4.1.2 Full Bridge - Zone 2

This zone is initiated as the primary current  $i_P$  reaches the reflected secondary current of  $i_{L_1}$ . Power is transferred from the primary to the secondary side and the positive gradient of the primary current is given by:

$$\frac{di_P}{dt} = \frac{N_2}{N_1} \cdot \frac{V_{In} \cdot \frac{N_2}{N_1} - \frac{V_{Out}}{2}}{L_1} \quad (4.2)$$

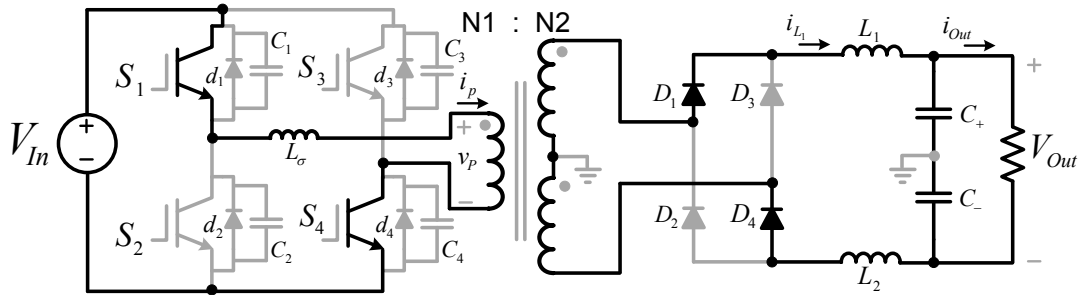


Figure 4.8: Current direction in zone 2

The maximum current flowing in the primary is obtained in this zone. Figure 4.8 depicts the respective current flow.

### 4.1.3 Full Bridge - Zone 3

Zone 3 is initiated when  $S_1$  is switched off,  $S_1$  switches off hard. The rectifier diodes  $D_3$  and  $D_4$  switch on as soon as the primary current falls below the reflected value of the filter inductor current  $i_{L_1}$ . These diodes switch on almost instantaneously at the beginning of zone 3.

The primary current  $i_P$  continues to flow in the same direction due to the energy stored in the leakage inductance  $L_\sigma$ . This stored energy is proportional to the square of the current at the instant when  $S_1$  switches off. This energy is transferred to the parasitic output capacitances of the IGBTs, namely  $C_1$  and  $C_2$ . Figure 4.9 depicts the direction of the primary current  $i_P$ .

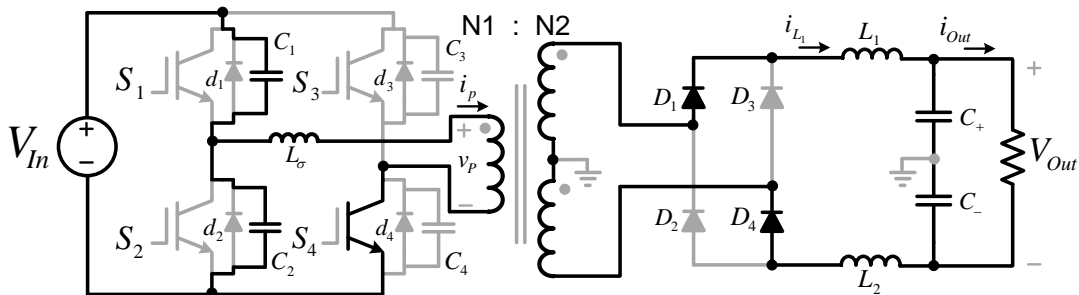


Figure 4.9: Current direction in zone 3

The small signal circuit consists of the leakage inductance  $L_\sigma$  in series with the parallel combination of  $C_1$  and  $C_2$ . Capacitor  $C_2$  is discharged, while  $C_1$  charges to the bus voltage  $V_{In}$ . The current in  $L_\sigma$  at the beginning and end of zone 3 is defined as  $i_{(3initial)}$  and  $i_{(3final)}$  respectively.

For  $S_2$  to switch on under zero voltage switching (ZVS) conditions the voltage across  $C_2$  should be fully discharged. Soft switching of  $S_2$  is then ensured if the energy stored in the  $L_\sigma$  is greater than the energy required to discharge  $C_2$  and charge  $C_1$ . This condition is stated mathematically as:

$$\frac{1}{2}L_\sigma(i_{(3initial)}^2 - i_{(3final)}^2) > C_1V_{In}^2 \quad (4.3)$$

The minimum value of  $L_\sigma$  to obtain soft switching of  $S_2$  in zone 3 is given by:

$$L_{\sigma(min)} > \frac{2 \cdot C_1 \cdot V_{In}^2}{i_{(3initial)}^2 - i_{(3final)}^2} \quad (4.4)$$

The leakage current  $i_P$  at the end of zone 3, namely  $i_{(3final)}$ , is therefore zero if this criterion is met. Ideally, the leakage inductance  $L_\sigma$  should be larger than  $L_{\sigma(min)}$  if ZVS of  $S_3$  is required in zone 6.

The ringing transition occurring in zone 3 at a bus voltage  $V_{In}$  equal to 1.3 kV is measured and shown in Figure 4.10. The plot depicts the  $v_{CE}$  voltage of  $S_2$ , namely  $v_{CE(S_2)}$ , the primary current  $i_P$  and the gate voltage of  $S_2$ , namely  $v_{ge(S_2)}$ . As the voltage over  $S_2$  rings down to zero, a clear decrease in the primary current  $i_P$  is observed. This decrease in current is due to the energy lost in  $L_\sigma$ , which discharge  $C_2$  and charges  $C_1$ . The final value of the primary current  $i_P$  is greater than zero, thus diode  $d_2$  conducts the primary current  $i_P$ . The leakage inductance  $L_\sigma$  is therefore larger than  $L_{\sigma(min)}$ . The gate signal of  $S_2$  is switched on after the voltage over  $S_2$  has rung down to zero, thus ZVS of  $S_2$  is achieved.

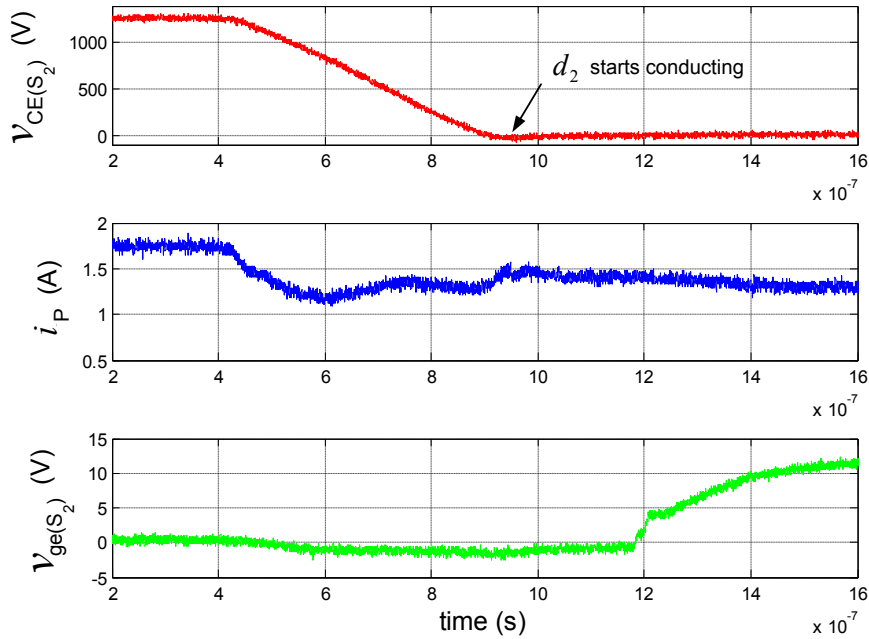


Figure 4.10: Measured soft switching of  $S_2$  in zone 3



This measurement is taken in order to be certain that ZVS occurs in this transition; the voltages were measured by using two  $100\times$  probes and a differential voltage probe. The differential probe was used to measure the gate signal of  $S_2$ , as this voltage is at a floating potential with respect to the center point of the bus capacitors. The  $100\times$  voltage probes were used to measure the negative terminal of the bus voltage  $V_{In}$  and the left leg voltage  $v_{Left}$  with respect to the center point. The difference of these two measurements is equivalent to the voltage over  $S_2$ .

The voltage probe connected to the left leg voltage  $v_{Left}$  has an effect on the measurement, as the output capacitance of this probe is in the order of 2.75 pF. This capacitance is small compared to the output capacitance of  $C_2$  which is 120 pF. The parasitic capacitance of the voltage probe adds to the output capacitance of the IGBTs, thus increasing the total capacitance that should be either discharged or charged. Thus, more energy is withdrawn from the leakage inductance  $L_\sigma$ . Figure 4.10 shows that ZVS is easily obtained due to the remaining amount of primary current  $i_P$  after this transition, thus the additional value of the probe capacitance is ignored.

#### 4.1.4 Full Bridge - Zone 4

The current flow in zone 4 is dependent on the amount of energy remaining in the leakage inductance  $L_\sigma$  after zone 3. Assuming that there is still sufficient energy remaining in  $L_\sigma$  after zone 3, diode  $d_2$  will become forward biased and start conducting the primary current  $i_P$ . IGBT  $S_2$  is then switched on under ZVS, because the diode forward voltage  $v_f$  is approximately zero with respect to the bus voltage  $V_{In}$ .

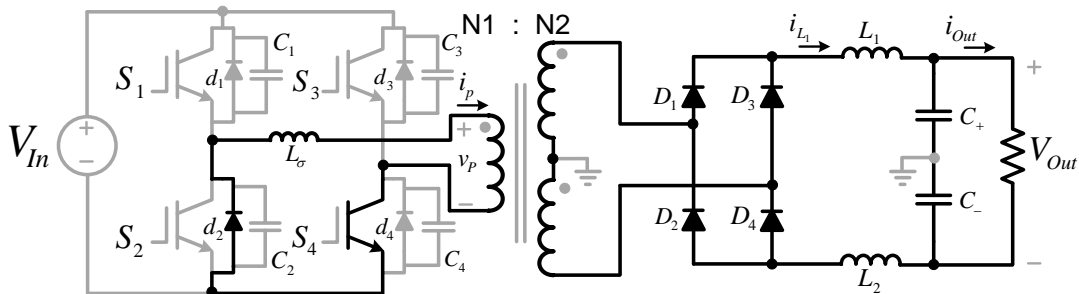


Figure 4.11: Current direction in zone 4

The voltage over the primary winding  $v_p$  is clamped to:

$$\begin{aligned} v_p &= -[V_{CE(SAT)} + V_f] \\ &\approx 0V \end{aligned} \tag{4.5}$$

As the primary voltage  $v_p$  is clamped, an LR circuit is formed, with  $L_\sigma$  in series with the equivalent resistance in the conduction path. The LR time constant is large, thus the leakage current  $i_p$  remains virtually constant during this time interval [44].

### 4.1.5 Full Bridge - Zone 5

Zone 5 is initiated when IGBT  $S_4$  is switched off; this transition is hard-off. The primary current  $i_p$  continues to flow through  $d_2$  due to the remaining energy in the leakage inductance  $L_\sigma$ . The right leg voltage is no longer clamped, thus the primary current  $i_p$  charges  $C_4$  and discharges  $C_3$ . This transition takes much longer than the left leg transition, as most of the energy in  $L_\sigma$  is lost in zone 3.

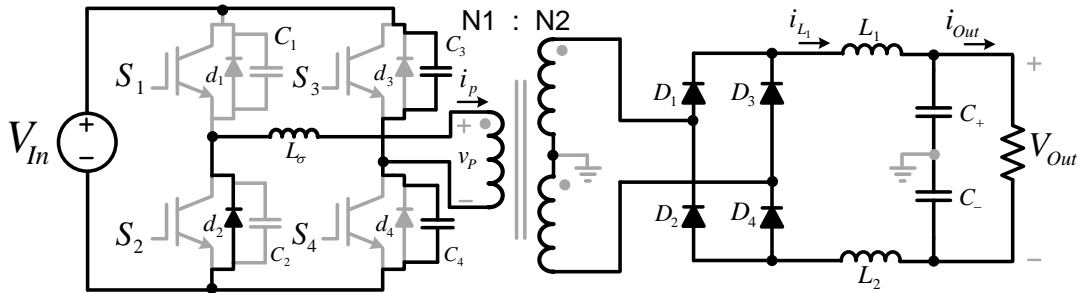


Figure 4.12: Current direction in zone 5

IGBT  $S_3$  is switched on under ZVS if  $C_3$  is fully discharged; however, if the energy in the leakage inductance is insufficient, ZVS is not obtained. The amount of energy required at the start of zone 5 to discharge  $C_3$  fully is mathematically stated as:

$$\frac{1}{2}L_\sigma i_{(5initial)}^2 > C_3 V_{In}^2 \quad (4.6)$$

The primary current in the converter is relatively low, thus the energy stored in  $L_\sigma$  is mostly insufficient for a complete transition. Figure 4.13 shows the measured voltage transition over  $S_3$  in zone 5. The dead time was set to show the full transition of the ringing voltage. Capacitor  $C_3$  is shown to ring towards zero and  $C_4$  charges toward  $V_{In}$ . The amplitude of the ringing voltage shows that the energy in  $L_\sigma$  is insufficient to discharge  $C_3$  entirely. To minimize the switching losses  $S_3$  should be switched on at the peak of the ringing voltage.

After the peak of the ringing voltage,  $C_3$  charges to  $V_{In}$  and  $C_4$  discharges to zero. As the primary current stops flowing, diode  $d_2$  switches off softly because the voltage over it is clamped to zero. These excess carriers naturally recombine, thus no reverse current is required to sweep them out of the drift region [11].

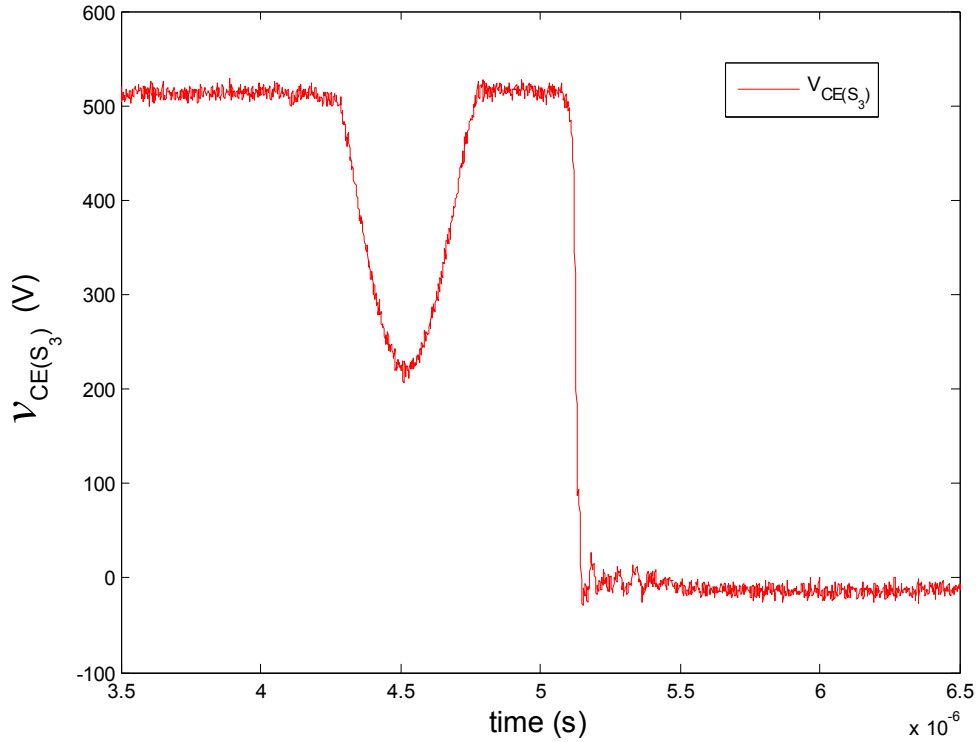


Figure 4.13: Measured voltage over  $S_3$  in zone 5

#### 4.1.6 Full Bridge - Zone 6

Zone 6 is initiated as IGBT  $S_3$  is switched on. The switching transition of  $S_3$  is dependent on the energy stored in the leakage inductance  $L_\sigma$ . There are three possible options with regard to the switching transition: the first option is that there is sufficient energy left in  $L_\sigma$  so that  $C_3$  is totally discharged and  $S_3$  switches on under ZVS. The energy is proportional to the square of the current, thus ZVS will not be obtained at lighter loads.

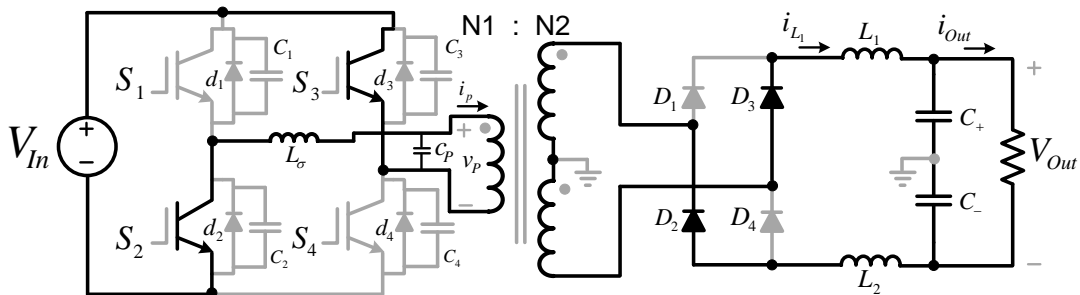


Figure 4.14: Current direction in zone 6

The second option is that an incomplete transition occurs and that  $C_3$  is not fully discharged, which means that  $S_3$  is switched on at a reduced voltage. Zero voltage switching is however attainable by adding extra inductance into the primary winding; the disadvantage of this is

that the rectifier snubber has to absorb this additional energy. A trade-off is made between the switching losses in the IGBTs and the rectifier snubber circuit that has to absorb this additional energy. For practical purposes, this option was not chosen, because ZVS for this transition is not reliable under varying load conditions.

The third option is to set the dead-time occurring in zone 5 so that it is large enough for the leakage inductance  $L_\sigma$  to discharge fully, hence reducing the primary current  $i_P$  to zero. This allows IGBT  $S_3$  to be switched on at a current amplitude of zero. Figure 4.15 illustrates the turn-on transition of  $S_3$  at a bus voltage  $V_{In}$  equal to 1.3 kV. This figure depicts the  $v_{CE}$  voltage of  $S_3$ , namely  $v_{CE(S_3)}$  and the primary current  $i_P$ . It can be seen from the figure that the voltage transition of zone 5 is incomplete, therefore discharging the leakage inductance  $L_\sigma$ . The primary current  $i_P$  reduces to zero at the same instant as the right leg ringing transition completes. IGBT  $S_3$  then switches on after the primary current  $i_P$  has been reduced to zero. The rise time  $t_{on}$  was measured to be 97 ns. The bandwidth of the voltage and current probes is 100 MHz and 50 MHz respectively.

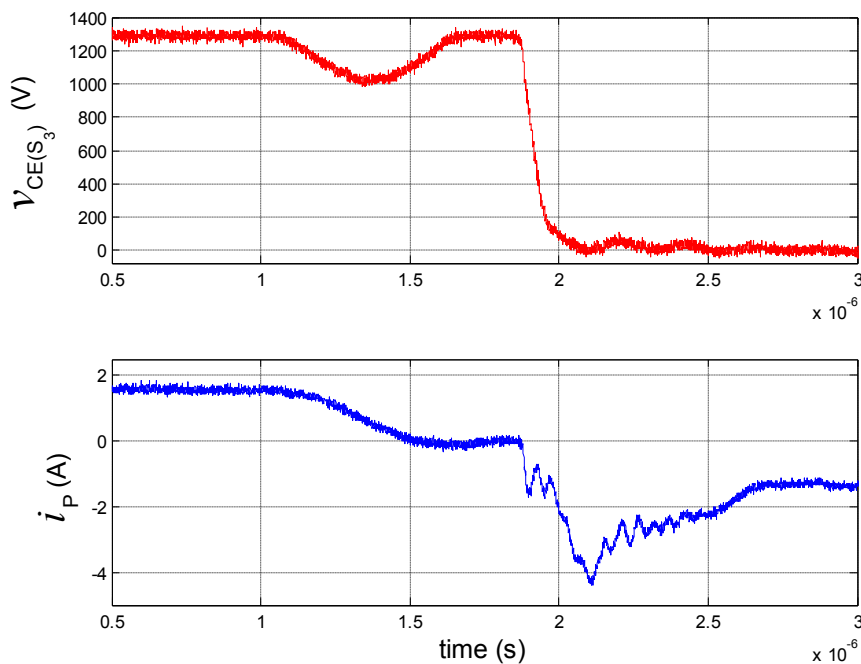


Figure 4.15: Zero current switching of  $S_3$

The ringing that is noticed on  $i_P$  as  $S_3$  is switched on is caused by the parasitic capacitances of the IGBTs and the transformer capacitance  $C_P$ . As IGBT  $S_3$  is switched on, capacitor  $C_4$  is charged to  $V_{In}$ , thus discharging  $C_3$ . The transformer parasitic capacitance  $C_P$  is also charged to  $V_{In}$ . The oscillatory current flowing through  $S_3$  at switch-on is comprised of the current flowing into the right leg through  $C_4$  and the current flowing into the transformer through  $C_P$ .

The method used to calculate the switching losses used in [11] cannot be utilized for this transition, as the current is not constant. This is due to the small value of the leakage induc-

tance  $L_\sigma$ . The switching losses of  $S_3$  are obtained from first principles by calculating the power dissipated in the transition:

$$\begin{aligned} P_{S_3(on)} &= \frac{1}{T_s} \int_0^{t_{on}} v_{CE}(t) \cdot [i_{C_4}(t) + i_{C_P}(t)] dt \\ &= \frac{1}{T_s} \int_0^{t_{on}} v_{CE}(t) \cdot [C_4 v'(t) + C_P v'(t)] dt \end{aligned} \quad (4.7)$$

Solving this equation analytically is impractical, as the instantaneous voltages are required, as well as the exact value of  $C_P$ . The transformer parasitic capacitance  $C_P$  is not known and the calculation thereof is based on assumptions, thus leading to an inaccurate result.

The partial switching losses of  $S_3$ , are however numerically calculated by measuring the instantaneous waveforms of the primary current  $i_P$  and the IGBT  $v_{CE}$  voltage. These losses were 1.7 W at a switching frequency of 35 kHz. The minute rise time  $t_{on}$  of 97 ns is the main factor why these losses are negligible. These measurements and numerical results shown in Figure 4.15 prove that the switching losses of  $S_3$  are negligible. After this oscillation has settled the primary current  $i_p$  ramps negatively at a gradient of  $\frac{-V_{In}}{L_\sigma}$ .

## 4.2 Rectifier

The alternating waveform on the secondary of the transformer is passed through a rectifier, to obtain the DC voltage required for the three phase inverter. The rectifier selection is based between an active or a passive rectifier. The main disadvantage of the active rectifier is the additional cost involved, because this option requires 4 additional IGBTs as well as the additional gate drive circuitry. Another disadvantage is the required isolation between the primary and secondary windings of the transformer. These additional IGBTs would generally be controlled optically, as pulse transformers do not have the required isolation. The cost of these optic transmitters for 48 cells would add unwanted costs to the SST.

The passive rectifier utilizes diodes, thus no control circuitry is required; however, this option only allows uni-directional power flow. The active rectifier, in contrast allows bi-directional power flow. Bi-directional power flow in distribution transformers is rarely required, as these devices step down the voltage from 11 kV to 400V, rather than stepping it up from 400 V to 11 kV.

The rectifier chosen is a passive full bridge center-tapped rectifier, the rectifier is shown in Figure 4.16. This rectifier is chosen because it provides a center point connection which is required for the 3 phase DC-AC inverter.

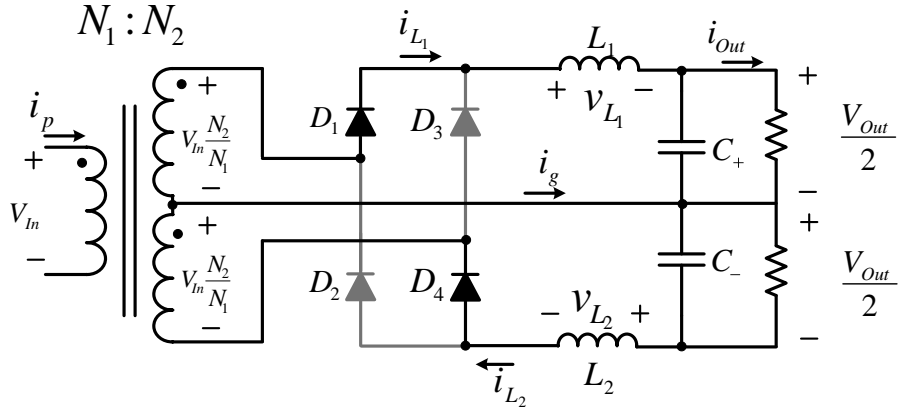


Figure 4.16: Rectifier

The rectifier is separated into two halves if the center point current  $i_g$  is zero. For the center point current  $i_g$  to be zero, the secondary currents  $i_{L_1}$  and  $i_{L_2}$  must be identical. These currents are identical if the voltages across the filter inductors, namely  $v_{L_1}$  and  $v_{L_2}$  are the same. Referring to Figure 4.16, the inductor voltages are given as:

$$v_{L_1} = \frac{V_{In} \cdot \frac{N_2}{N_1} - \frac{V_{Out}}{2}}{L_1} \quad (4.8)$$

$$v_{L_2} = \frac{V_{In} \cdot \frac{N_2}{N_1} - \frac{V_{Out}}{2}}{L_2} \quad (4.9)$$

These voltages are identical if the value of the inductors, namely  $L_1$  and  $L_2$  are identical.  $L_1$  and  $L_2$  are chosen so that both have a value of 1.1 mH, and thus the center point current  $i_g$  is ignored. The primary vs secondary current relation is therefore given as:

$$N_1 i_p = N_2 i_{L_1} + N_2 i_{L_2} \quad (4.10)$$

$$N_1 i_p = 2N_2 i_{L_1}$$

$$i_{L_1} = \frac{N_1}{N_2} \cdot \frac{i_p}{2}$$

Ignoring the center point current  $i_g$  in the steady state analysis greatly simplifies the analysis of the rectifier. It allows the top half and the bottom half of the rectifier to be split up with respect to the center point. The rectifier operation is explained from zone 2 to 6, forming a basis of the snubber design (refer to Figure 4.5).

#### 4.2.1 Rectifier - Zone 2

In zone 2, the secondary voltage is positive, forcing diodes  $D_1$  and  $D_4$  into conduction. The current in the filter inductor  $i_{L_1}$  is considered as a current source due the large inductance of  $L_1$ , as compared to the referred leakage inductance  $L'_\sigma$ . Figure 4.17 depicts the parasitic capacitances of each rectifier diode, as well as the referred transformer capacitance  $C'$ . Zone 3 is ignored in the analysis of the rectifier, as the time required to forward bias  $d_2$  is negligible.

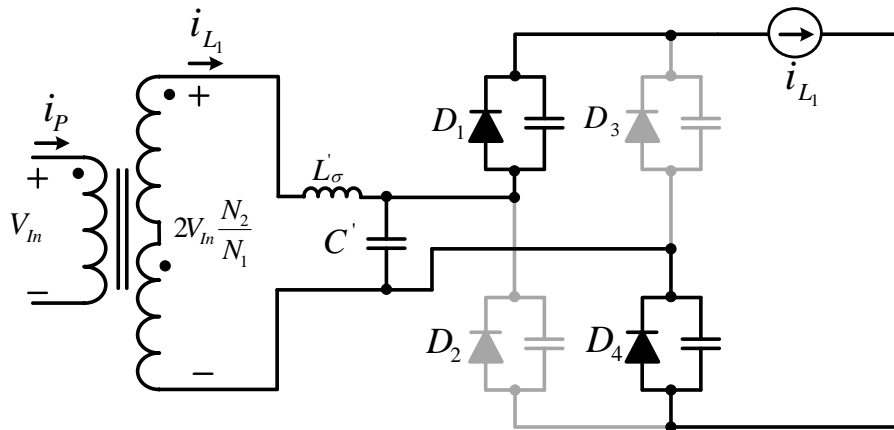


Figure 4.17: Rectifier zone 2

#### 4.2.2 Rectifier - Zone 4

The full bridge in zone 4 clamps the primary voltage  $v_P$  to the conduction drop that occurs in the freewheeling period as explained in Section 4.1.4. The primary voltage  $v_P$  is virtually zero with respect to the bus voltage  $V_{In}$ . The remaining energy in the leakage inductance  $L_\sigma$  however still allows the primary current  $i_P$  to flow. The secondary current  $i'_P$  continues to flow in the positive direction through  $D_1$  and  $D_4$  due to the leakage inductance  $L_\sigma$ . As the secondary current  $i'_P$  falls below the filter inductor current  $i_{L1}$ , diodes  $D_3$  and  $D_4$  switch on. The filter inductor current is equally shared between the four diodes as soon as the leakage inductance  $L_\sigma$  is fully discharged.

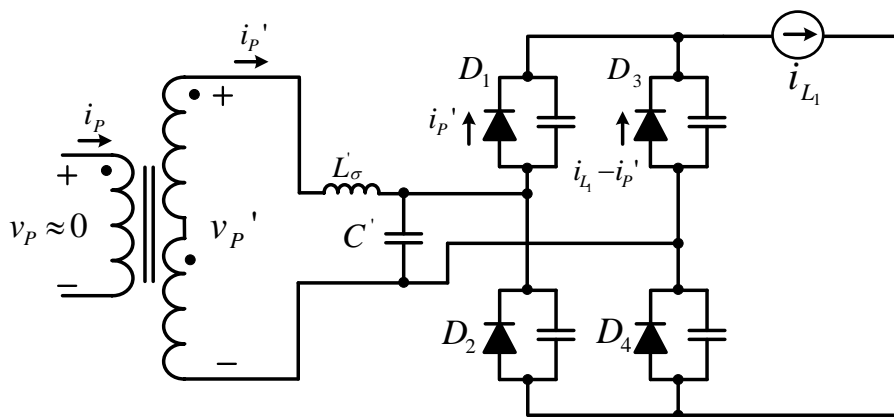


Figure 4.18: Rectifier zone 4

Zone 5 is the right leg transition, the direction of the current flow is not different from that of zone 4. The amplitude of the primary current  $i_p$  is however reduced, this zone is therefore not of importance with regard to the snubber analysis.

### 4.2.3 Rectifier - Zone 6

In zone 6, the primary voltage  $v_P$  reverses and diodes  $D_1$  and  $D_4$  become reverse biased. The current in these diodes is now drastically reduced at a gradient of  $\frac{di_{rr}}{dt}$ . This rate of current change is dependent on many circuit parameters; such as the circuit inductance, the voltages of the circuit and the characteristics of the diode. The current flowing through the diode eventually becomes negative and is defined as the reverse recovery current  $i_{rr}$ . This current becomes negative to sweep the excess carriers out of the drift region in order for the metallurgical junctions to become reverse biased [11]. This reverse current is shown in the form of a current source in Figure 4.19.

As the reverse recovery current snaps off, the stored energy in the leakage inductance  $L'_\sigma$  reacts with the stray capacitances of the circuit. This forms an under-damped LC circuit. A simplified circuit is obtained by shorting out  $D_2$  and  $D_3$  and is shown in Figure 4.20 [7]. At snap-off the amplitude of the current flowing through the secondary winding namely  $i'_P$  is equal to:

$$i'_P = i_{LL} + 2i_{rr} \quad (4.11)$$

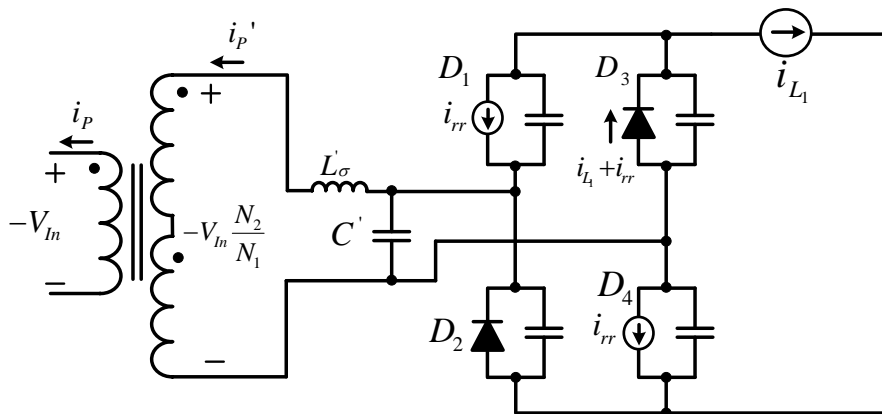


Figure 4.19: Rectifier zone 6

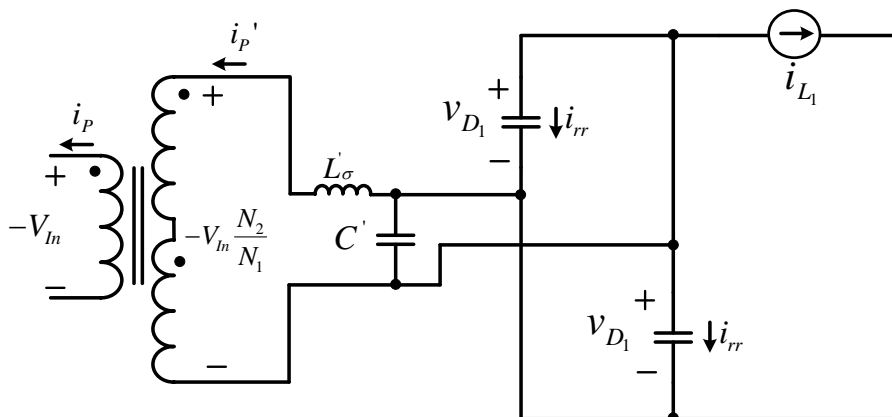


Figure 4.20: Reduced circuit of zone 6 obtained from [7]



The small signal circuit of Figure 4.20 is shown in Figure 4.21, with the voltage  $v_{D_1}$  being the actual ringing voltage across the diode.

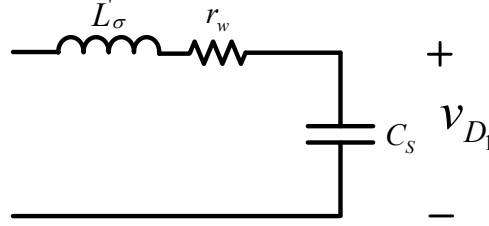


Figure 4.21: Small signal of zone 6

The resistance  $r_w$  is the transformer winding resistance, whereas  $C_d$  is the capacitance of diodes  $D_1$  and  $D_2$  added in parallel. The total secondary capacitance is defined as  $C_S = C_d + C'$ . The transfer function of the circuit is given by:

$$H(s) = \frac{1}{L'_\sigma C_S}{s^2 + s \frac{r_w}{L'_\sigma} + \frac{1}{L'_\sigma C_S}} \quad (4.12)$$

Analysing Equation 4.12, the natural frequency and damping of the system are respectively given by:

$$f_r = \frac{1}{2\pi \sqrt{L'_\sigma C_S}} \quad (4.13)$$

$$\zeta = \frac{r_w}{2L'_\sigma \sqrt{L'_\sigma C_S}} \quad (4.14)$$

The natural ringing voltage of the diodes is shown in Figure 4.22, thus no snubber circuit was included. Due to the excessive ringing voltage this measurement was taken at a lower bus voltage  $V_{Out}$  to protect the diodes. The overshoot is seen to be 240%. This measurement was taken to obtain the natural ringing frequency  $f_r$  that occurs on the diode ringing voltage. This frequency  $f_r$  was measured to be 3.3 MHz; from this the secondary capacitance  $C_S$  is calculated to be 72.7 pF using Equation 4.13. The referred leakage inductance  $L'_\sigma$  was measured to be 31.6  $\mu$ H.

The natural damping caused by the resistance  $r_w$  is also seen in Figure 4.22. The winding resistance  $r_w$  is measured to be 200 m $\Omega$ , however this resistance is in the order of a few hundred ohm at  $f_r$  due to the skin effect (refer to [43] for the relevant calculation of this resistance).

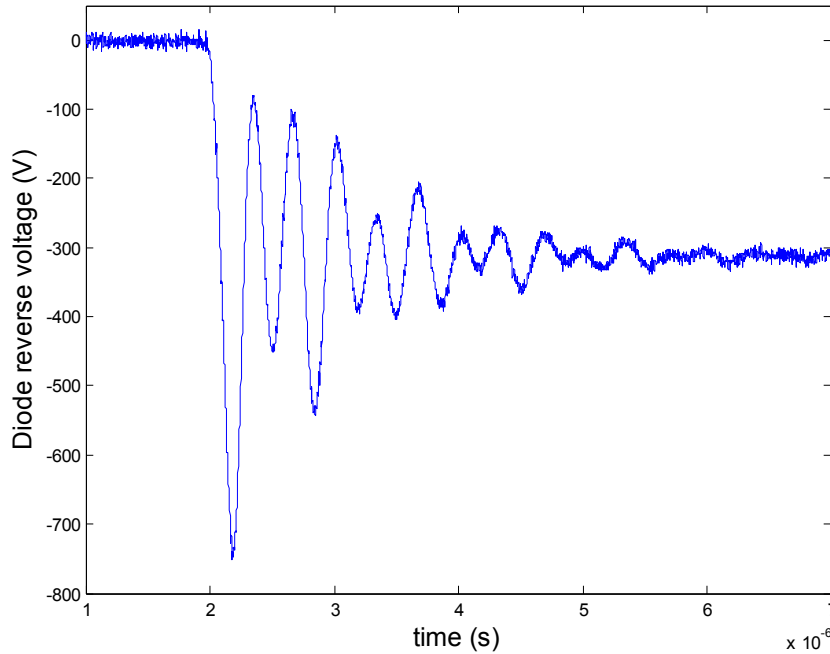


Figure 4.22: Measured ringing voltage of the rectifier diodes

#### 4.2.4 Snubber Design

The design of the snubber is done by adding additional circuitry onto the small signal circuit of Figure 4.21 to damp the circuit optimally. This additional circuitry is designed to absorb the high frequency components and to improve the damping of the system.

The impedance of the snubber circuit must be much lower for the high frequency components, than the impedance of the parasitic elements in the system. The design in this section is based on [7]. The capacitance value of the snubber circuit is typically ten times larger than  $C_S$ , thus providing a low impedance path for the high frequency components. The addition of a series resistance is added for damping, the RC snubber circuit described is shown in Figure 4.23.

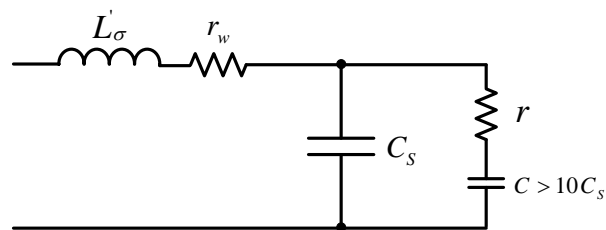


Figure 4.23: Basic snubber circuit

This circuit is reduced to an RLC circuit if the assumption is made that  $C_S$  is much smaller than the snubber capacitance  $C$ , thus  $C_S$  is omitted. The RLC circuit is then easily analysed using the standard second order transfer function available in most control system textbooks.

Thus  $L$  is fixed,  $C$  is chosen and  $R$  is calculated to obtain an optimal damping value of  $\zeta = \frac{1}{\sqrt{2}}$ . The main aim in the design of any snubber is to obtain the best damping with the least power dissipated in the snubber circuit. The power losses are the most restrictive factor in the design.

There are two main snubber circuits that are considered for this rectifier namely the RC snubber and the over voltage snubber. The RC snubber would have a capacitance of  $10 \cdot C_S$ , which is roughly 1 nF. The power loss in the RC circuit would amount to  $P_{Snub} = 2f_s C V_{Out}^2$  which is equal to 44.8 W. These losses are however reduced by placing two identical snubber circuits in series and connecting the center point between them. The advantage of this is that the voltage of each snubber circuit is brought down from 800 V to 400 V, which means that the total losses of both snubbers would amount to 22.4 W.

A disadvantage of the RC snubber is that the peak value of the diode ringing voltage is not directly controllable. The RC snubber was thus not chosen for the design, as it is not certain whether this voltage margin is suitable for the 1200 V diodes.

The over voltage snubber (OVS) shown in Figure 4.24, however, has a controllable threshold voltage. The threshold voltage is defined by the voltage of  $C_{OV}$ , as Diode  $D_{OV}$  must be forward biased to bring  $D_{OV}$  into conduction. Figure 4.24 only shows one OVS; however there is an identical OVS connected between the center point and the negative bus.

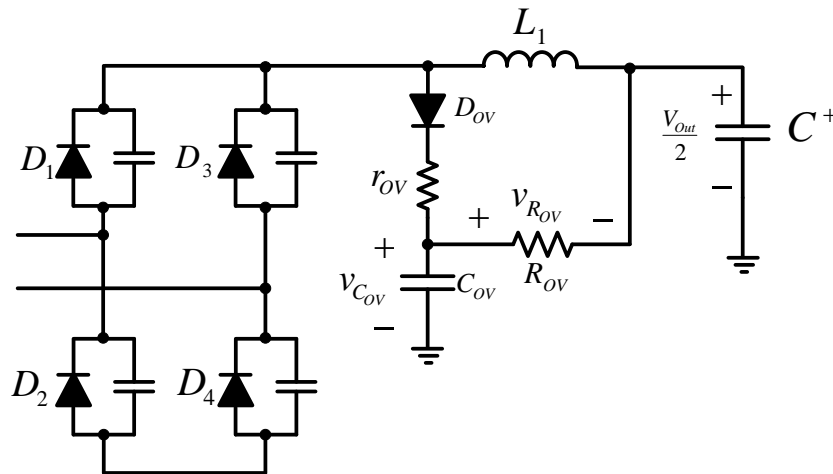


Figure 4.24: Over voltage snubber

The advantage of this snubber is that it is only in the circuit for a limited amount of time, as opposed to the RC snubber, which is continuously in circuit. For this reason, the capacitance of the snubber circuit can be increased extensively opposed to the RC snubber. As the diode voltage rings above  $V_{C_{OV}}$ , then diode  $D_{OV}$  becomes forward biased and the circuit operates as a conventional RC snubber.

The main disadvantage is that, once diode  $D_{OV}$  is reverse biased, the high frequency ringing carries on naturally. This remaining ring will not have a large amplitude, though, as most of the energy is removed by the initial absorption of the RC snubber.

The resistance value of  $R_{OV}$  is chosen to set the threshold of the capacitor voltage  $C_{OV}$  optimally. The threshold voltage should be set to absorb the ringing voltage but when the ringing is complete, then diode  $D_{OV}$  should become reverse biased and remove the RC snubber from the circuit. The remaining time where  $D_{OV}$  is reverse biased allows for  $C_{OV}$  to discharge into the bus capacitor  $C^+$ .

The amount of energy entering the snubber circuit is mainly dependent on the threshold voltage  $v_{C_{OV}}$ . This energy entering the circuit is not a linear function of  $R_{OV}$ , as the threshold is set regardless of the diode ringing waveform. This non-linear effect is shown in Figure 4.25, as the threshold is altered. The area below the threshold voltages  $V_1$  or  $V_2$  and the ringing waveform is where the snubber circuit is in operation. The energy entering the snubber circuit while the threshold is equal to  $V_1$  is much more than that at threshold  $V_2$ . The more energy that enters the snubber circuit, the higher the threshold voltage is because capacitor  $C_{OV}$  is charged. The higher this voltage, the less effective the snubber circuit becomes.

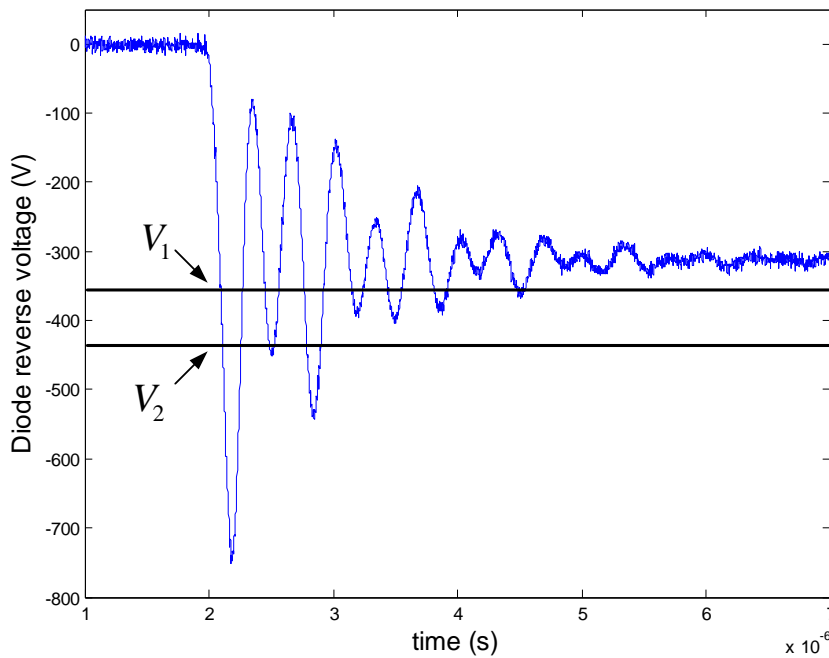


Figure 4.25: Threshold voltages

The value of  $R_{OV}$  is estimated by calculating the amount of power entering the snubber circuit from the energy stored in the referred leakage inductance  $L'_\sigma$ . This method described below is a rough estimate to obtain an initial value for  $R_{OV}$ . The assumption is made that the power entering the snubber circuit is fully dissipated in  $R_{OV}$ , which is mathematically stated as:

$$E_{L'_\sigma} \cdot 2f_s = \frac{V_{R_{OV}}^2}{R_{OV}} \quad (4.15)$$

$$\begin{aligned} \frac{1}{2}L'_\sigma I_{rr}^2 \cdot 2f_s &= \frac{(V_{COV} - \frac{V_{Out}}{2})^2}{R_{OV}} \\ R_{OV} &= \frac{(550 - 400)^2}{31.7\mu H \cdot 2.75^2 \cdot 35000} \\ &= 2.68 \text{ k}\Omega \end{aligned}$$

The energy stored in  $L'_\sigma$  is multiplied by twice the switching frequency to calculate the power entering the circuit. The reverse recovery current  $I_{rr}$  used in Equation 4.15 is the current amplitude at the instance of snap-off. The power entering the circuit is assumed to be constant, as is the voltage over  $R_{OV}$ . The voltage over  $R_{OV}$  is chosen to be 150 V, thus the threshold voltage is set to 150 V above the bus voltage  $\frac{V_{Out}}{2}$ .

The initial value of  $R_{OV}$  was calculated to be 2.68 k $\Omega$ ; this was obtained by rearranging the terms in Equation 4.15. The values of the following parameters are given as  $L'_\sigma = 31.7$   $\mu$ H,  $f_s = 35$  kHz and  $I_{rr} = 2.75$  A. This method of obtaining  $R_{OV}$  was used initially, before a range of measurements were taken to clarify the assumptions made regarding the unknown parameters. The bus voltage  $\frac{V_{Out}}{2}$  versus  $V_{ROV}$  were measured at different resistance values and are shown in Figure 4.26.

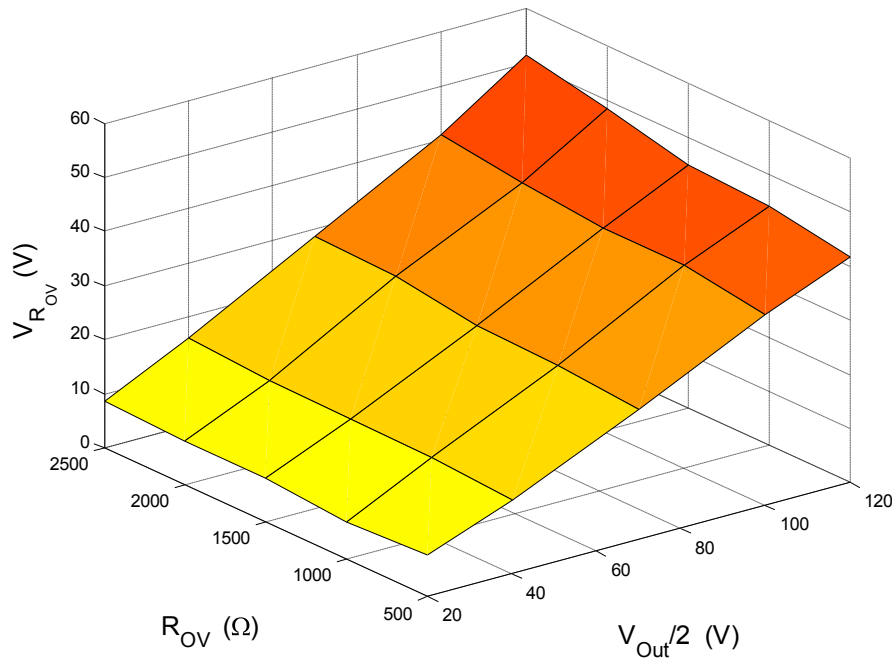


Figure 4.26: Measured voltages at a constant  $r_{OV} = 25 \Omega$

The plot shows that the gradient of  $m = \frac{V_{ROV}}{V_{OUT}/2}$  is not constant as  $R_{OV}$  is altered. Figure 4.26 depicts the increase in the gradient  $m$  as  $R_{OV}$  increases. The voltage  $V_{ROV}$  increases as the resistance increases, thus reducing the effect of the snubber circuit. Decreasing the value of  $R_{OV}$  improves the effect of the snubber; at the same time, however, the losses in  $R_{OV}$  increase. This means that the energy entering the snubber circuit varies as the threshold voltage varies.

However the plot in Figure 4.26 shows that the gradient  $m$  is constant at a fixed value of  $R_{OV}$ . This has an advantage, as the voltages can be extrapolated to the rated bus voltage  $V_{Out}$  for a constant resistance of  $R_{OV}$ .

An optimal value of  $R_{OV}$  is chosen by taking into account the allowable threshold voltage and power dissipation. However, the value of  $R_{OV}$  is not reduced to such an extent that it effects the operation of the filter inductor  $L_1$ . The data of Figure 4.26 is extrapolated and the power dissipated in  $R_{OV}$  is shown in Figure 4.27. The power dissipated in  $R_{OV}$  is a quadratic function of the voltage  $V_{R_{OV}}$ .

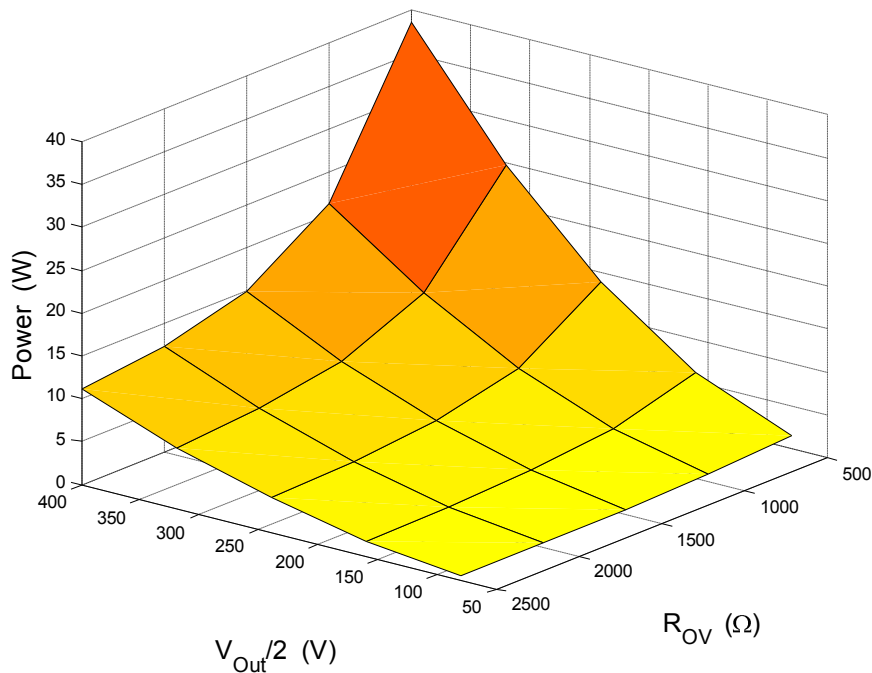


Figure 4.27: Extrapolated power dissipation in  $R_{OV}$  at a constant  $r_{OV} = 25 \Omega$

It is visible from the plot that, as  $R_{OV}$  increases the dissipated power decreases. The value of  $R_{OV}$  is chosen to be  $1500 \Omega$ , thus the losses amount to  $15 \text{ W}$ , thus for both over voltage snubbers the losses amount to  $30 \text{ W}$ . This is under  $1.5\%$  of the total power of the system. At this resistance value, it is predicted that the threshold voltage of  $V_{C_{OV}}$  is  $550 \text{ V}$ .

The effect of the snubber circuit is measured as the leakage inductance  $L_\sigma$  is altered. This was done by adding additional inductance in series with the transformer primary winding. According to Equation 4.15, as the leakage inductance is increased the energy entering the snubber circuit is increased. Thus the voltage over  $R_{OV}$  is expected to increase as the leakage inductance increases. The measured results are depicted in Figure 4.28, which concurs with the theory.

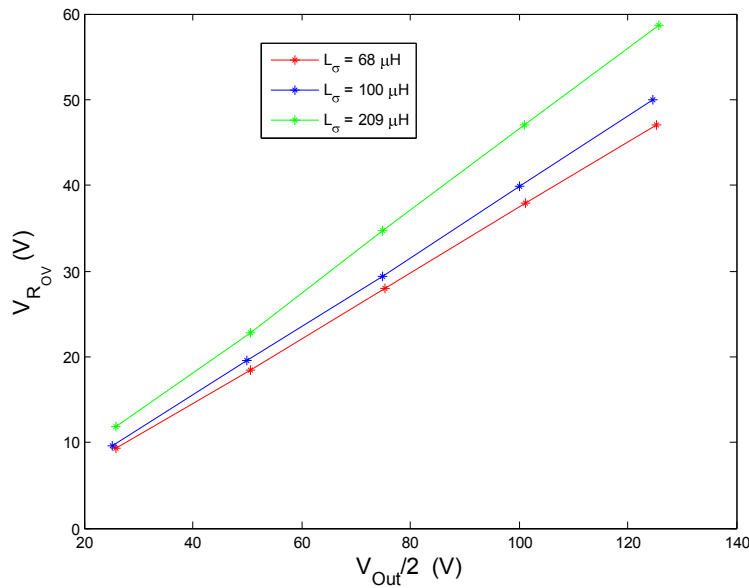


Figure 4.28: Voltage over  $R_{OV}$  as  $L_\sigma$  is altered

The overshoot and damping of the system were also measured as the leakage inductance was varied. This was done in order to verify that the snubber circuit's operation is still satisfactory in the event of additional leakage inductance  $L_\sigma$  being added. These results are shown in Figure 4.29, from which it is seen that the settling time of the ringing voltage increases as  $L_\sigma$  increases. This is due to the additional energy entering the snubber circuit. The ringing frequency is clearly shown to decrease as the leakage inductance  $L_\sigma$  is increased, thus the ringing frequency equation is justified, namely Equation 4.13. It can be deduced that the effect of the snubber circuit remains satisfactory as the leakage inductance  $L_\sigma$  increases.

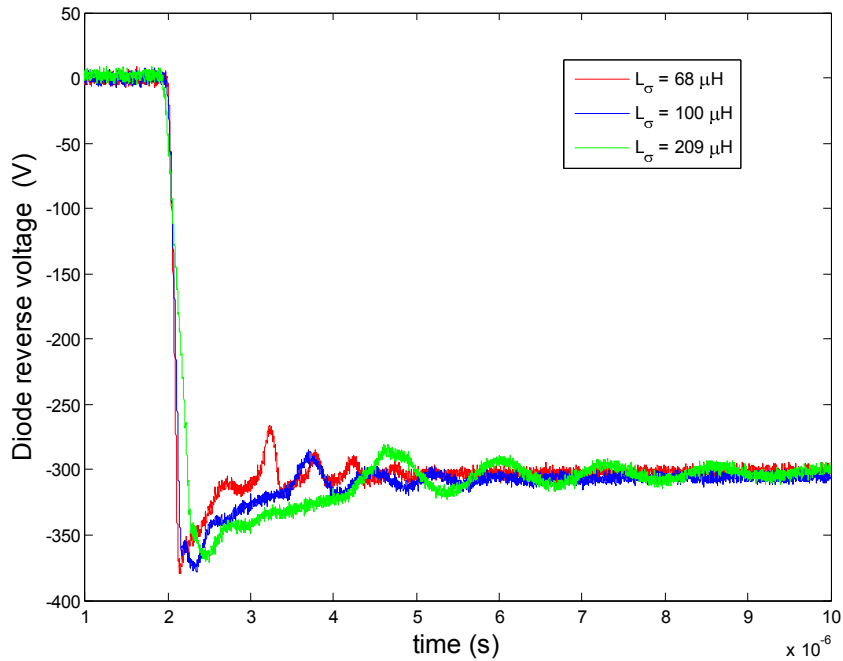


Figure 4.29: Diode reverse voltage as  $L_\sigma$  is altered

In Figure 4.30, the value of the series resistance  $r_{OV}$  is chosen with  $R_{OV}$  fixed. This resistance is chosen to damp the ringing voltage of the system optimally. The addition of this series resistance  $r_{OV}$  increases the peak value of the ringing voltage. This is caused by the voltage drop that occurs across  $r_{OV}$  while diode  $D_{OV}$  conducts. The increased overshoot is negligible with respect to the benefits that  $r_{OV}$  adds to the dampening of the system.

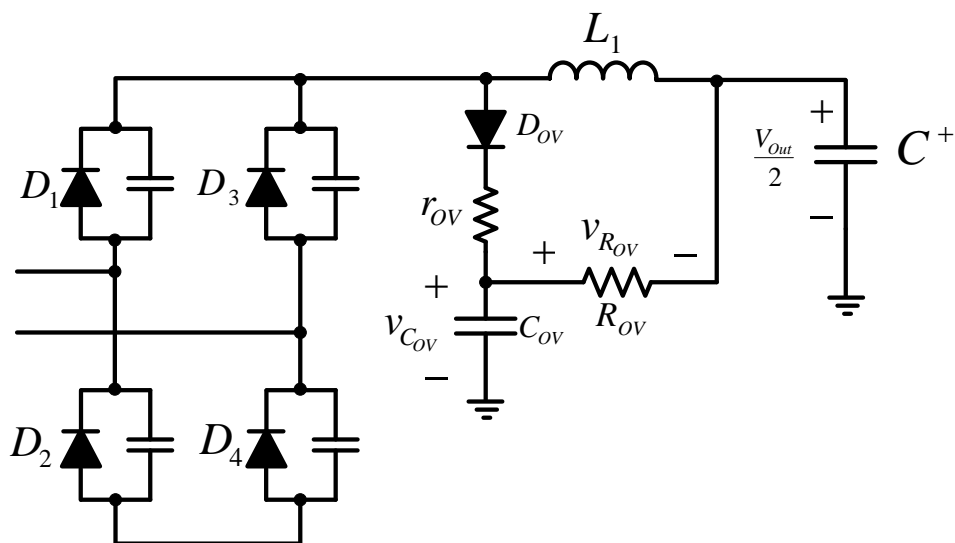


Figure 4.30: Over voltage snubber



When the over voltage snubber is in circuit, the small signal circuit is identical to that of Figure 4.23. The secondary capacitance  $C_S$  is ignored, and the snubber capacitor  $C_{OV}$  is chosen to be 470 nF. The referred leakage inductance  $L'_\sigma$  is fixed, thus  $r_{OV}$  is calculated to obtain optimal damping:

$$\zeta = \frac{r_{OV}}{2L'_\sigma \sqrt{\frac{1}{L'_\sigma C_{OV}}}} \quad (4.16)$$

$$r_{OV} = \zeta \cdot 2L'_\sigma \sqrt{\frac{1}{L'_\sigma C_{OV}}}$$

$$= 11.6 \Omega$$

The effect of the snubber circuit is shown in Figure 4.31, with  $R_{OV} = 1500 \Omega$  and  $r_{OV} = 12 \Omega$ . The overshoot of the ringing voltage is reduced from 240% to 18%.

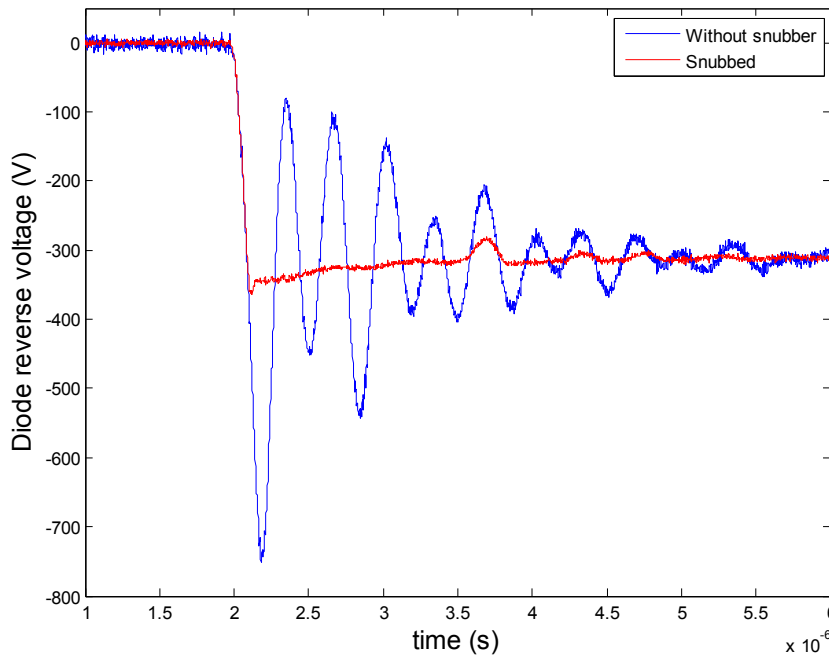
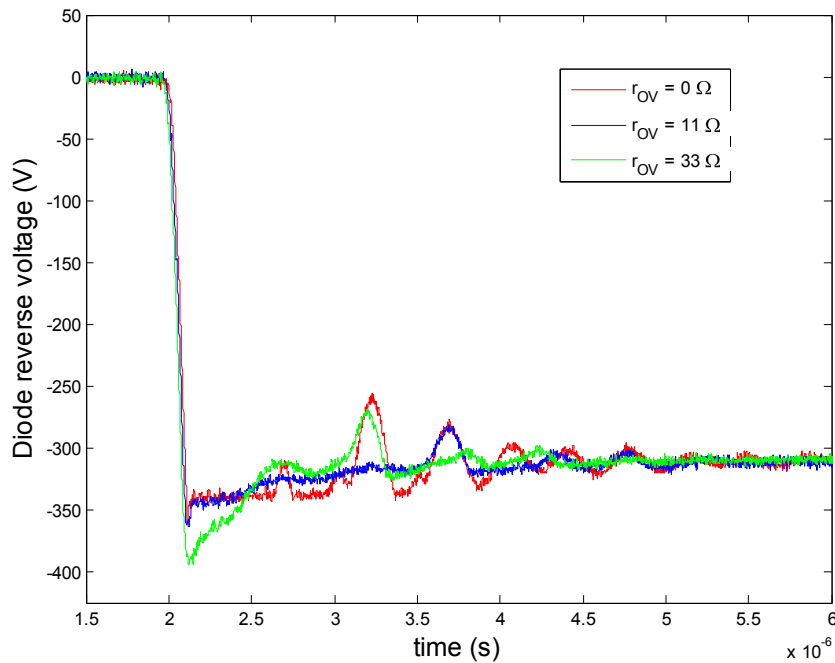


Figure 4.31: Diode reverse voltage with and without the snubber circuit

Figure 4.32 depicts the ringing voltage at different values of  $r_{OV}$ . It can be seen that the optimal damping of the system is obtained at  $r_{OV} = 11\Omega$ , which is the same as the theoretical value.

Figure 4.32: Diode reverse voltage at  $R_{OV} = 1500 \Omega$ 

### 4.3 Conclusion

The topology selection of the high voltage DC-DC converter was discussed, and it was explained why the phase shifted full bridge (PSFB) converter was chosen. The operation of the converter was described, and the soft switching transitions were investigated. The left leg switches were commutated under ZVS, whereas the right leg switches were commutated under ZCS. The relevant soft switching measurements at a rated bus voltage of 1.3 kV were included. The operation of the secondary rectifier was discussed and it was shown why a modified over voltage snubber was used. This snubber circuit reduced the diode ringing voltage from 240% to 18%, as was verified by the relevant measurements.

## Chapter 5

# Three Phase Inverter

The output stage of the cell is defined as the section that converts the low voltage DC to three phase AC. The low voltage DC bus is fed from the parallel connected isolation stages of the series stacked SST. Figure 5.1 depicts the output stage highlighted in black, whereas the rest of the cell is depicted in gray.

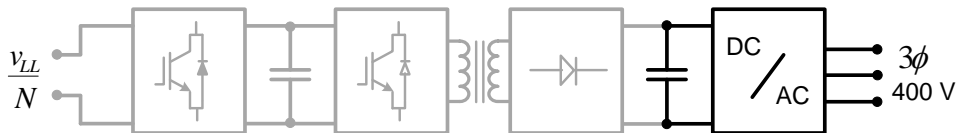


Figure 5.1: The output stage of the cell

The output stage of the SST is implemented by using a 3 phase DC-AC inverter; the converter is shown in Figure 5.2. The half bridge topology is chosen for the converter, as it can be connected to provide a neutral point at the load. The neutral of the load is therefore connected between the bus capacitors. The secondary configuration is therefore identical to that of the conventional distribution transformer.

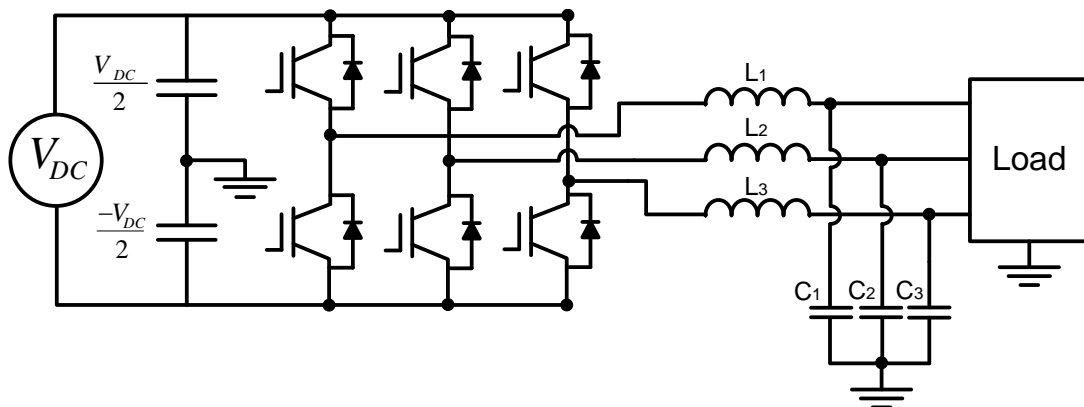


Figure 5.2: Three phase inverter

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This chapter describes the design of the inverter in detail; the emphasis of this design is on the losses present in the system. These losses are comprised of passive component losses as well as switching component losses. The former mainly include the conduction losses occurring in the inductors and capacitors. The latter are the losses dissipated in the diodes and insulated gate bipolar transistors (IGBT). These losses are further subdivided into switching and conduction losses.

The most accurate way of determining the losses is to physically measure them. Two main methods are used for this, namely electrical and calorimetric methods [28]. Electrical methods measure the current that flows through a device and the voltage across it, whereas the instantaneous power is obtained by multiplying these two values. Measuring the losses electrically is much easier and quicker than the lengthy calorimetric methods. Analogue measuring devices have a very low bandwidth, thus these measurements are only suitable for DC or low frequency AC measurements. Although digital measuring devices have a greater bandwidth, they are more susceptible to noise. A phase lag is also introduced with these measuring devices, thereby resulting in inaccurate measurements.

Calorimetric methods require the device being tested to be placed in a temperature controlled environment, and thus the change in temperature is proportional to the losses emitted in the system. These measurements are lengthy procedures, although their results are more accurate than electrical methods.

Loss measurements can, however, only be done on an existing inverter. Thus it is necessary to do a theoretical loss calculation for the design phase. Optimization of the external heatsink and cooling fan is dependent on the accuracy of the loss calculations. A few methods of how loss calculations have been done in the past are described in [8; 29–31]. Analytical methods of calculating switching device losses are available in the literature, although these methods do not take into account the inductor ripple current. Thus it is unknown what the effect of the inductor ripple current has on the switching device losses. This chapter therefore focuses on the IGBT and diode losses as the inductor ripple current increases. The findings of this chapter were published in [45].

Two methods of calculating the switching device losses are discussed, namely analytical and numerical methods. The existing analytical method is based on obtaining the average current flowing through the switching devices and calculating the losses using averaged values. The proposed numerical method calculates the exact current flowing through the switching devices, thus taking into account the inductor ripple current. This method is based on an existing method of calculating the inductor ripple current. This current is then subdivided into the respective IGBT and diode currents.

The losses occurring in the switching devices are also dependent on the type of modulation used. The main modulation methods of controlling inverters are space-vector modulation and sinusoidal modulation; this analysis focuses on the latter. The losses are calculated numerically for two sinusoidal pulse width modulation (SPWM) techniques, namely single edge (SEPWM) and double edge PWM (DEPWM).

## 5.1 System Specifications

As the SST is rated at 80 kVA, the DC-AC converter is rated identically. The output of the converter is coupled in a three phase four wire configuration. At unity power factor the line current is equal to 115 A rms, which is identical to the phase current. The amplitude of the peak current flowing through the load is therefore  $\sqrt{2} \times 115$  A, namely 163 A.

The currents flowing through the filter inductors are therefore the fundamental current of 163 A with a 10 kHz ripple current super-imposed thereon. The ripple current is chosen as 30% of the fundamental; this large ripple current is taken into account in order to limit the physical size of the inductors. This however presents difficulties in the control stability as well as resulting in an increase in switching losses. The main reason for limiting the inductor size is to build the entire SST as small as possible, which enhances the feasibility of the SST.

A segment of the inductor current flows through the IGBTs, thus the current rating of the IGBTs should be greater than the current flowing through the filter inductors. The current rating of the IGBTs should therefore be greater than 187 A. The IGBTs chosen are the soft punch-through devices from Semikron, namely the SEMiX 352GB128Ds. These IGBTs have a voltage rating of 1 200 V and a 270 A nominal current rating. These devices also have exceptionally fast switching times, hence reducing the switching losses.

The respective losses and their calculation is dependent on a thorough understanding of the current flowing in the inverter. Figure 5.3 and Figure 5.4 illustrate the current flow in the inverter for the positive inductor current scenario. More specifically, Figure 5.3 depicts the current flow when the top IGBT  $S_A$  is conducting. In contrast, Figure 5.4 depicts the current flow when IGBT  $S_A$  is off, and the current is still positive; it thus conducts through diode  $D_B$ . The negative inductor current scenario is similar, resulting in IGBT  $S_B$  and diode  $D_A$  conducting the current.

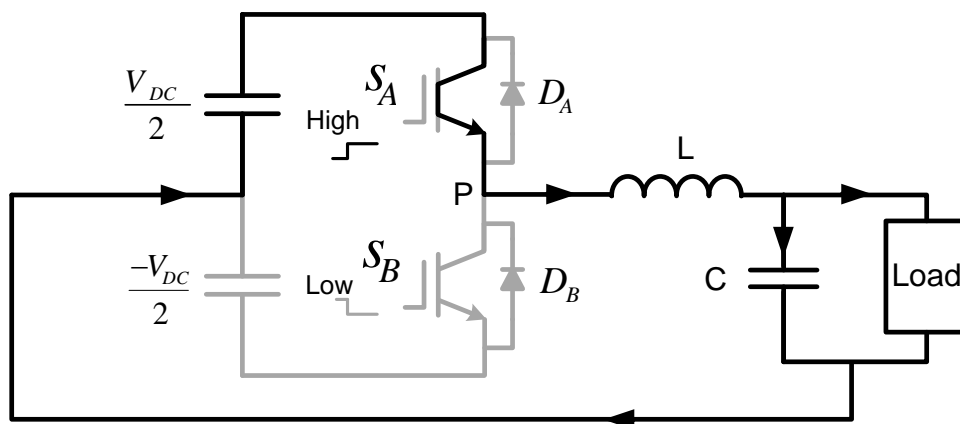


Figure 5.3: Positive inductor current with IGBT  $S_A$  on

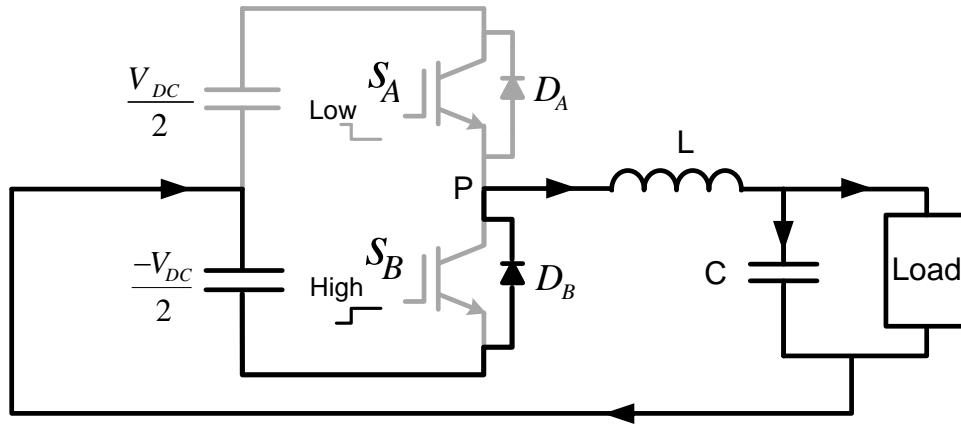


Figure 5.4: Positive inductor current with IGBT  $S_A$  off

The losses are calculated for the half bridge topology shown in Fig. 5.5. The DC bus voltage in Figure 5.5, namely  $V_{DC}$ , is identical to the output voltage  $V_{Out}$  described in Chapter 4. This voltage is renamed in this chapter for the sake of clarity. The load current is defined as  $i_o$  and the peak value of the load current as  $I_o$ . The filter capacitor  $C$  is fixed, while the filter inductance  $L$  is varied.

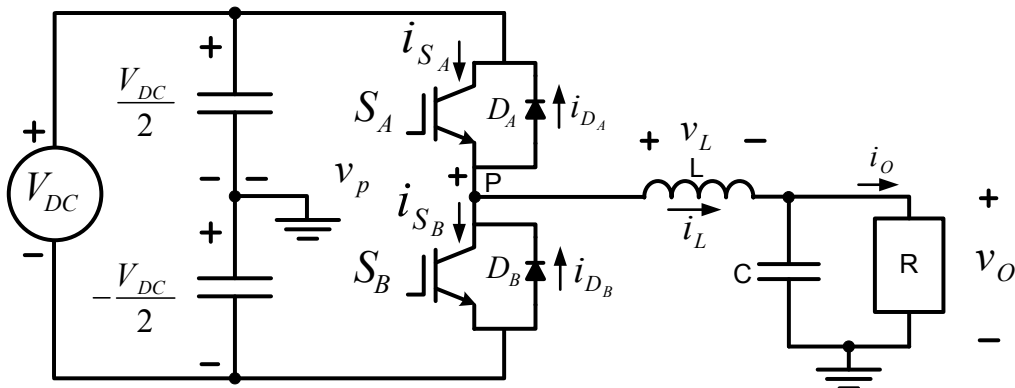


Figure 5.5: Half bridge topology

Referring to Figure 5.6, the carrier wave is defined as  $c(t)$  and the reference wave as  $m(t) = m_a \sin(\omega_1 t)$ , with  $m_a$  being the modulation index. The period of  $m(t)$  and  $c(t)$  is defined as  $T_1 = \frac{1}{f_1}$  and  $T_s = \frac{1}{f_s}$ , respectively.

Table 5-I tabulates the specifications of the inverter and Table 5-II lists the specifications of the IGBT.

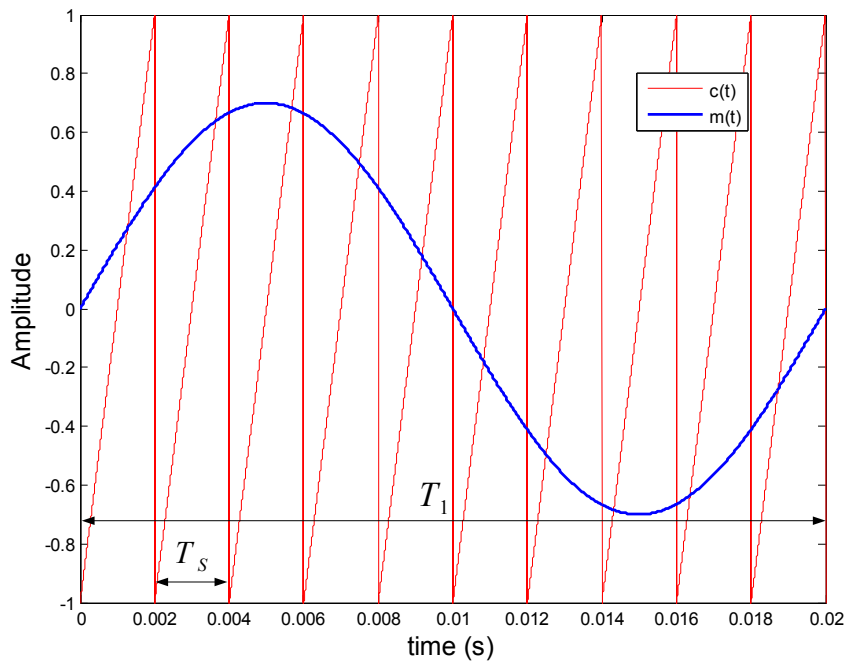


Figure 5.6: Sinusoidal modulation using a sawtooth carrier

Table 5-I: Inverter specifications

Parameters	
$I_{o(rms)} = 115 \text{ A}$	$I_o = I_{o(rms)} \cdot \sqrt{2} \text{ A}$
$V_{DC} = 800 \text{ V}$	$m_a = 0.8$
$L = \text{various}$	$C = 100 \mu\text{F}$
$f_s = 10 \text{ kHz}$	$f_1 = 50 \text{ Hz}$

Table 5-II: IGBT specifications

Parameters	
$V_{CE(max)} = 1200 \text{ V}$	$I_C = 270 \text{ A}$
$V_{on} = 0.6 \text{ V}$	$V_{f(diode)} = 2 \text{ V}$
$t_{on} = 55 \text{ ns}$	$t_{off} = 90 \text{ ns}$
$E_{RRmax} = 10.6 \text{ mJ}$	$r_{ce} = 7.5 \text{ m}\Omega$

## 5.2 Method 1

The switching and conduction losses are analytically calculated in this section using well-known existing models. This method, which is obtained in [8], assumes the load current to be purely sinusoidal, thus ignoring the inductor ripple current.

### 5.2.1 Switching Losses

The switching transitions in a half bridge inverter are hard-on and hard-off transitions, which means that there are no soft switching transitions. These transitions are shown in Figure 5.7, which gives a brief overview of the switching transitions in a half bridge inverter. The gate signals of IGBT  $S_A$  and IGBT  $S_B$  are defined as  $G_A$  and  $G_B$  respectively. The collector-emitter voltages of these IGBTs are defined as  $v_{ce(S_A)}$  and  $v_{ce(S_B)}$  respectively and the dead time is defined as  $t_{dt}$ . The switching transitions occur at the beginning and end of zone 3.

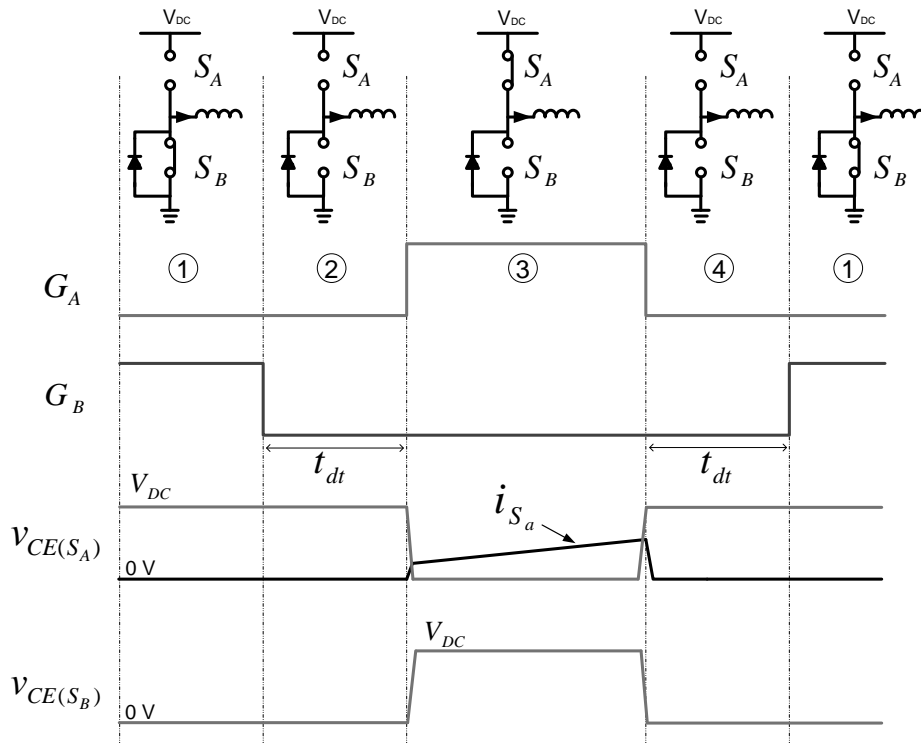


Figure 5.7: Half bridge inverter switching transients

This section uses a well-known model, which appears in most power electronics text books [11], to approximate the switching losses occurring in IGBTs. The basis of the model is to calculate the energy dissipated in the switch-on and switch-off transitions. The energy dissipated in each transition is shown in Equations 5.1 and 5.2, where  $i_C$  is the collector current.



The rise and fall times are defined as  $t_{on}$  and  $t_{off}$  respectively.

$$W_{turn(On)} = \frac{1}{2}V_{DC}i_C t_{on} \quad (5.1)$$

$$W_{turn(Off)} = \frac{1}{2}V_{DC}i_C t_{off} \quad (5.2)$$

Defining the inductor current as  $i_L = I_o \sin(\omega_1 t - \phi)$  with  $\phi$  the phase angle between the load voltage and load current. An assumption is made that the turn-on and turn-off transitions occur at the same current amplitude in each switching cycle  $T_s$ .

The sum of the switching energies over  $T_1$  is converted into a Riemann sum. This is done to obtain the average switching losses. The average switching losses of IGBT  $S_A$  over  $T_1$  are given by [8]:

$$\begin{aligned} P_{switch} &= \frac{1}{T_1} \sum_{i=1}^N \frac{1}{2} V_{DC} I_o \sin(\omega_1 t_i - \phi) (t_{on} + t_{off}) \quad (5.3) \\ &= \frac{1}{2T_1 T_s} V_{DC} I_o (t_{on} + t_{off}) \sum_{i=1}^N \sin(\omega_1 t_i - \phi) T_s \\ &\approx \frac{1}{2T_1 T_s} V_{DC} I_o (t_{on} + t_{off}) \int_{\frac{\phi}{\omega_1}}^{\frac{T_1}{2} + \frac{\phi}{\omega_1}} \sin(\omega_1 t - \phi) dt \\ &= \frac{f_s}{2\pi} V_{DC} I_o (t_{on} + t_{off}) \\ &= 30.02W \end{aligned}$$

The result of Equation 5.3 and all the analytical results that follow are obtained from the specifications in Section 5.1. The switching losses are independent of the phase angle  $\phi$ .

### 5.2.2 Conduction Losses

The basic model of a conducting IGBT is modelled by a resistance  $r_{ce}$  in series with a constant on voltage  $V_{on}$ . The conduction loss in IGBT  $S_A$  is given by:

$$P_{cond}(IGBT) = V_{on} \cdot I_{S_A} + I_{S_A(rms)}^2 \cdot r_{ce} \quad (5.4)$$

The average current through IGBT  $S_A$  is defined as  $I_{S_A}$ , whereas  $I_{S_A(rms)}$  is the rms current through the IGBT. Figure 5.8 shows the current through IGBT  $S_A$  for a section of the positive half cycle. The energy dissipated in the  $i^{th}$  pulse is approximated by:

$$\begin{aligned} E_{i(cond)} &\approx V_{on} \cdot dT_s \cdot I_o \sin(\omega_1 t_i) \quad (5.5) \\ &= V_{on} \cdot \frac{1}{2} (1 + m_a \sin(\omega_1 t_i)) I_o \sin(\omega_1 t_i) T_s \end{aligned}$$

with the duty cycle of IGBT  $S_A$  defined as  $d = \frac{1}{2}(1 + m_a \sin \omega_1 t)$ . The middle of the switching period is defined as  $t_i$  and the range of  $i$  is defined as  $1 \leq i \leq N$ .

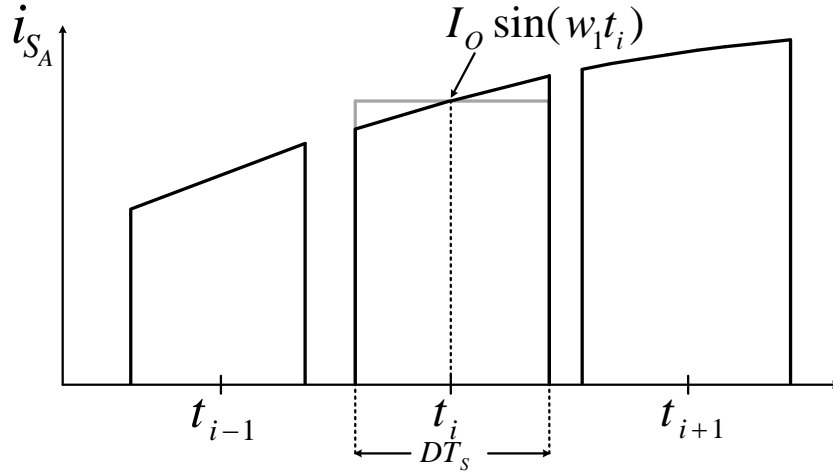


Figure 5.8: Average current approximation taken from [8]

The first term in Equation 5.4 is obtained by adding all of these pulses together and dividing by  $T_1$ . A Riemann sum is then used to approximate the average current through IGBT  $S_A$  [8]:

$$\begin{aligned}
 V_{on} \cdot I_{S_A} &= \frac{1}{T_1} \sum_{i=1}^N E_{i(cond)} & (5.6) \\
 &= \frac{1}{T_1} \sum_{i=1}^N \frac{1}{2} V_{on} (1 + m_a \sin(\omega_1 t_i)) I_o \sin(\omega_1 t_i) T_s \\
 &\approx \frac{V_{on}}{2T_1} \int_0^{\frac{T_1}{2}} (1 + m_a \sin(\omega_1 t)) I_o \sin(\omega_1 t) dt \\
 &= V_{on} \left( \frac{I_o}{2\pi} + \frac{m_a I_o}{8} \right) \\
 &= 25.28 \text{ W}
 \end{aligned}$$

The rms current  $I_{S_A(rms)}$  is obtained similarly to Equation 5.6 by first squaring all the pulses in Figure 5.8.

$$\begin{aligned}
 I_{S_A(rms)}^2 &= \frac{1}{T_1} \sum_{i=1}^N I_o^2 \sin^2(\omega_1 t_i) \cdot DT_s & (5.7) \\
 &= \frac{I_o^2}{2T_1} \sum_{i=1}^N \sin^2(\omega_1 t_i) \left( 1 + m_a \sin(\omega_1 t_i) \right) \cdot T_s \\
 &\approx \frac{I_o^2}{2T_1} \int_0^{\frac{T_1}{2}} \left[ \sin^2(\omega_1 t) + m_a \sin^3(\omega_1 t) \right] dt \\
 &= I_o^2 \left[ \frac{1}{8} + \frac{m_a}{3\pi} \right] \\
 &= 5551 \text{ A}^2
 \end{aligned}$$

The result of Equation 5.4 using Equations 5.6 and 5.7 is 67 W.

Figure 5.9 depicts the current waveforms in the respective components at a phase angle of  $40^\circ$ .

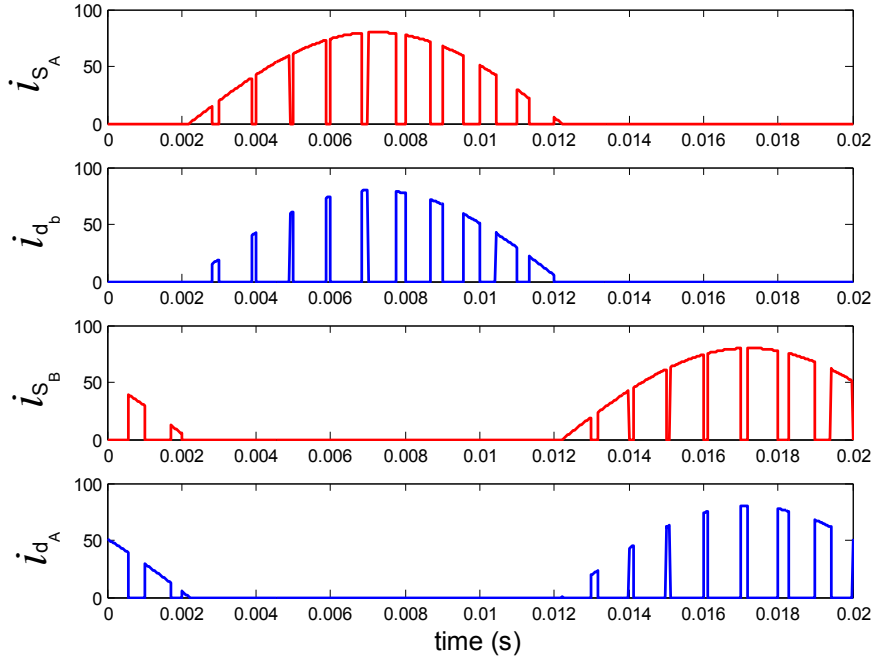


Figure 5.9: Respective current waveforms at  $\phi = 40^\circ$ , taken from [8]

An extension of Equation 5.6 is used to calculate the average IGBT current at a specific power factor. The phase angle  $\phi$  is inserted into the duty cycle term in Equation 5.8, as this term does not become negative opposed to the load current. This is done intuitively, as the current through the IGBT is unidirectional.

$$\begin{aligned}
 V_{on} \cdot I_{SA} &= \frac{1}{T_1} \sum_{i=1}^N E_{i(cond)} & (5.8) \\
 &\approx \frac{V_{on}}{2T_1} \int_0^{\frac{T_1}{2}} \left[ (1 + m_a \sin(\omega_1 t - \phi)) \right. \\
 &\quad \left. \times I_o \sin(\omega_1 t) dt \right] \\
 &= \frac{V_{on} I_o}{2T_1} \left[ \int_0^{\frac{T_1}{2}} \sin(\omega_1 t) dt \right. \\
 &\quad \left. + \int_0^{\frac{T_1}{2}} m_a \sin(\omega_1 t) \cdot \sin(\omega_1 t - \phi) dt \right] \\
 &= V_{on} I_o \left( \frac{1}{2\pi} + \frac{m_a \cos(\phi)}{8} \right)
 \end{aligned}$$

The equations in this section for calculating the conduction losses are also found in [31].

The average current of IGBT  $S_A$  vs  $\phi$  from Equation 5.8 is shown in Figure 5.10. The average current flowing through diode  $D_B$  is also plotted on the same axis; this result is obtained from Section 5.2.3. The converter operates in an inverter mode between the angles  $-90 \leq \phi \leq 90$  and acts as a rectifier outside those limits.

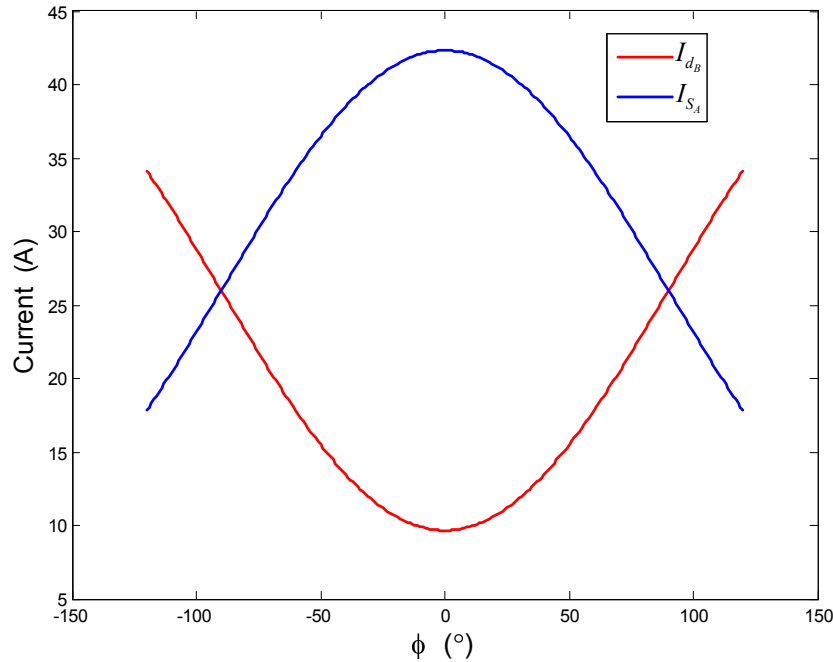


Figure 5.10: Average current versus phase angle  $\phi$

### 5.2.3 Diode Losses

The average current flowing through diode  $D_B$  is calculated by taking the difference between the average inductor current  $I_L$  and the average current through IGBT  $S_A$ . The average diode current  $I_{D_B}$  over one period is defined as [8]:

$$\begin{aligned}
 I_{D_B} &= I_L - I_{S_A} & (5.9) \\
 &= \frac{1}{T_1} \int_0^{T_1/2} I_o \sin(\omega_1 t) dt - I_{S_A} \\
 &= \frac{I_o}{\pi} - \left( \frac{I_o}{2\pi} + \frac{m_a I_o}{8} \right) \\
 &= 9.62 \text{ A}
 \end{aligned}$$

The conduction losses in diode  $D_B$  are found by simply multiplying  $I_{D_B}$  by the forward voltage  $V_{f(diode)}$ .

The reverse recovery losses  $P_{RR}$  in the diodes are difficult to calculate because it requires so many approximations. These approximations include the snappiness factor  $S$ , and the time

rate of change of the reverse current  $\frac{di_R}{dt}$ . The reverse recovery time  $t_{rr}$  is also required in the calculation [11]. To further complicate the calculation, the turn-off stored charge  $Q_r$  is dependent on the on-state forward current at the instant of turn-off [46]. This presents a problem, as the duty cycle and switching current vary over  $T_1$  due to the modulation index  $m_a$ .

For the purpose of this thesis a rough assumption is made in Equation 5.10 in order to calculate the  $P_{RR}$  by using the diode reverse recovery energy  $E_{RRmax}$ . The current through the diode is sinusoidal over  $\frac{T_1}{2}$ , thus the average of  $E_{RRmax}$  is derived similarly to Equation 5.3.

$$\begin{aligned} P_{RR} &\approx \frac{E_{RRmax}}{\pi} f_s \\ &\approx 33.7W \end{aligned} \quad (5.10)$$

Switch-on losses in modern day fast recovery diodes can be ignored [47], thus only the reverse recovery losses are approximated.

## 5.3 Method 2

Method 2 is a more accurate method of obtaining the losses in the switching components. This numerical method utilizes the exact current flowing through the IGBT to calculate the losses, thus increasing the accuracy of the result.

### 5.3.1 Inductor Ripple Current

The inductor ripple current  $\Delta i_L$  is parsed as a parameter to compare the results between the two methods. The ripple current is altered by changing the size of the filter inductor  $L$ . An equation for  $\Delta i_L$  is given in Equation 5.11, with the duty cycle equal to  $d = \frac{1}{2}(1 + m_a \sin(\omega_1 t))$  [48].

$$\Delta i_L = \frac{V_{DC}}{L f_s} (d - d^2) \quad (5.11)$$

The maximum ripple current is obtained by differentiating Equation 5.11 to obtain the maximum point. The filter inductance  $L$  at  $\Delta i_{L(Max)}$  is equal to:

$$L = \frac{V_{DC}}{4 f_s \Delta i_{L(Max)}} \quad (5.12)$$

### 5.3.2 Numerical Analysis

The numerical analysis of the switching and conduction losses is based on the accurate calculation of the intersections of the carrier  $c(t)$  and the reference wave  $m(t)$ .

The intersections are obtained in this section using the method derived in [48; 49]. The times at which the intersections occur are determined by means of the Newton-Raphson method. The general form of this method for calculating the roots of a function  $f(t)$  is given by:

$$t_{n+1} = t_n - \frac{f(t_n)}{f'(t_n)} \quad (5.13)$$

The intersection point between  $m(t)$  and  $c(t)$  is iteratively calculated by:

$$t_{n+1} = t_n - \frac{m(t_n) - c(t_n)}{m'(t_n) - c'(t_n)} \quad (5.14)$$

### 5.3.3 Double Edge PWM

Double edge PWM (DEPWM) has two intersections per switching period  $T_S$ ; these intersections are shown in Figure 5.11.

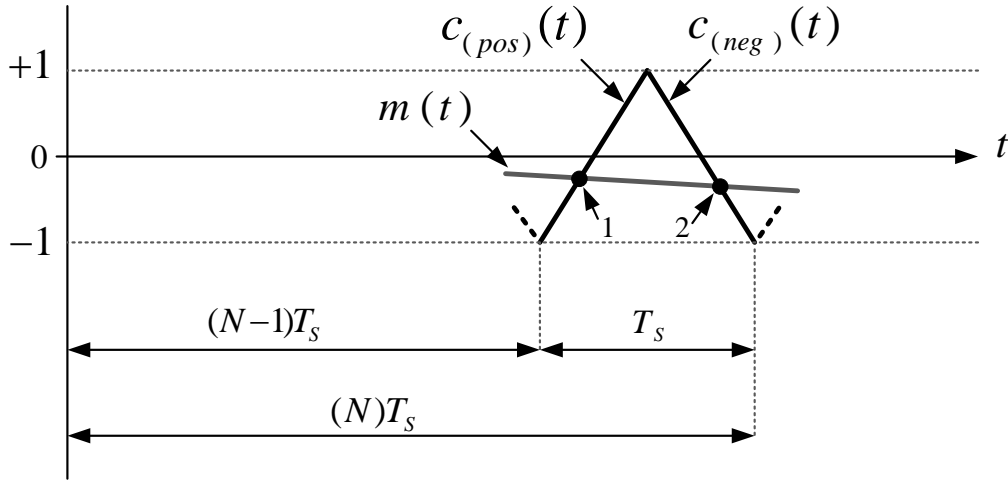


Figure 5.11: Intersection approximation of DEPWM

The respective line segments from Figure 5.11, namely  $c_{(pos)}(t)$  and  $c_{(neg)}(t)$  are given as:

$$c_{(pos)}(t) = \frac{4}{T_S}t - [4(N-1) + 1] \quad (5.15)$$

$$c_{(neg)}(t) = -\frac{4}{T_S}t + (4N-1) \quad (5.16)$$

For the respective regions:

$$(N-1)T_S < t < NT_S - \frac{T_S}{2} \quad (5.17)$$

$$NT_S - \frac{T_S}{2} < t < NT_S \quad (5.18)$$

The first intersection  $t_{n1}$  of the specific switching period  $N$  is found by substituting Equation 5.15 into 5.14. The point in time where the intersection occurs is calculated through iteration of the equation:

$$t_{n1+1} = t_{n1} - \frac{m_a \sin(w_1 t_{n1}) - \frac{4}{T_S} t_{n1} + [4(N-1) + 1]}{m_a w_1 \cos(w_1 t_{n1}) - \frac{4}{T_S}} \quad (5.19)$$

The second intersection  $t_{n2}$  of switching period (N) is found by substituting Equation 5.16

into 5.14 and iteratively calculated by:

$$t_{n2+1} = t_{n2} - \frac{m_a \sin(w_1 t_{n2}) + \frac{4}{T_s} t_{n2} - (4N - 1)}{m_a w_1 \cos(w_1 t_{n2}) + \frac{4}{T_s}} \quad (5.20)$$

### 5.3.4 Single Edge PWM

Single edge PWM (SEPWM) has a fixed starting point, namely at the beginning of each switching period. Thus, only one intersection is required per  $T_s$ .

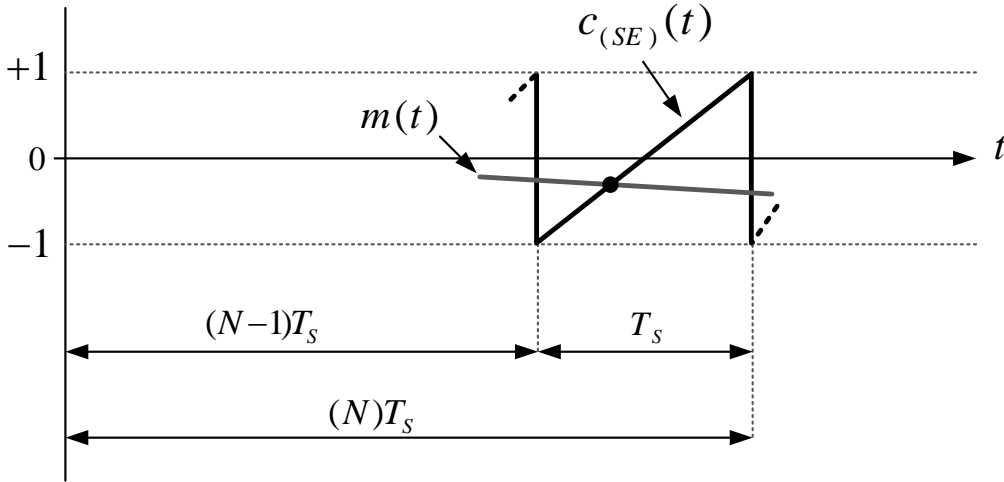


Figure 5.12: Intersection approximation of SEPWM

In the region between  $(N - 1)T_s < t < NT_s$ ,  $C_{(SE)}(t)$  is given as:

$$C_{(SE)}(t) = \frac{2}{T_s}t - (2N - 1) \quad (5.21)$$

The point in time where the intersection occurs is obtained similarly to that of the DEPWM and is found through iteration of:

$$t_{n+1} = t_n - \frac{m_a \sin(w_1 t_n) - \frac{2}{T_s}t_n + (2N - 1)}{m_a w_1 \cos(w_1 t_n) - \frac{2}{T_s}} \quad (5.22)$$

### 5.3.5 Current Waveforms

The intersections defined in the previous section determine the upper and lower envelopes of the inductor current. The respective equations are defined by:

$$i_{upper}(t_i) = I_o \sin(w_1 t_i) + \frac{\Delta i_L(t_i)}{2} \quad (5.23)$$

$$i_{lower}(t_i) = I_o \sin(w_1 t_i) - \frac{\Delta i_L(t_i)}{2} \quad (5.24)$$

The inductor current is plotted in Figure 5.13 at a switching frequency of 2 kHz. This waveform is plotted with the assumption that the voltage across the inductor namely  $v_L$  is constant over  $DT_S$  and  $(1 - D)T_S$ . Thus the gradient of the inductor current  $i_L$  is constant in these two regions.

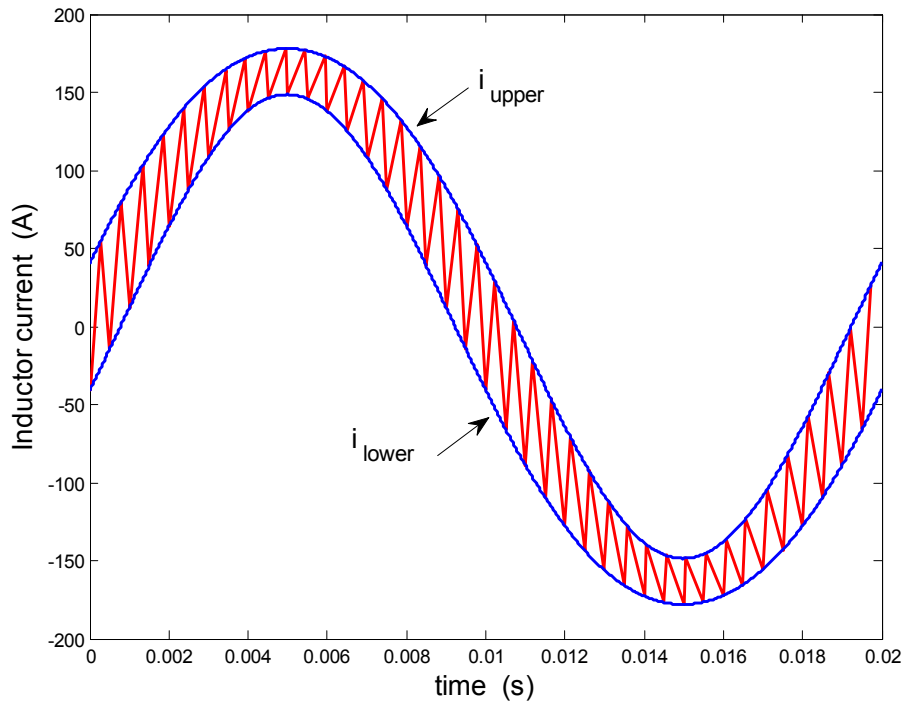


Figure 5.13: Inductor current at  $\Delta i_L = 50\%$

The inductor current  $i_L$  is the total current that flows out of point  $P$  in Fig. 5.14. The inductor current  $i_L$  is therefore separated into the respective components, namely  $i_{S_A}$ ,  $i_{S_B}$ ,  $i_{D_A}$  and  $i_{D_B}$  for waveform analysis.

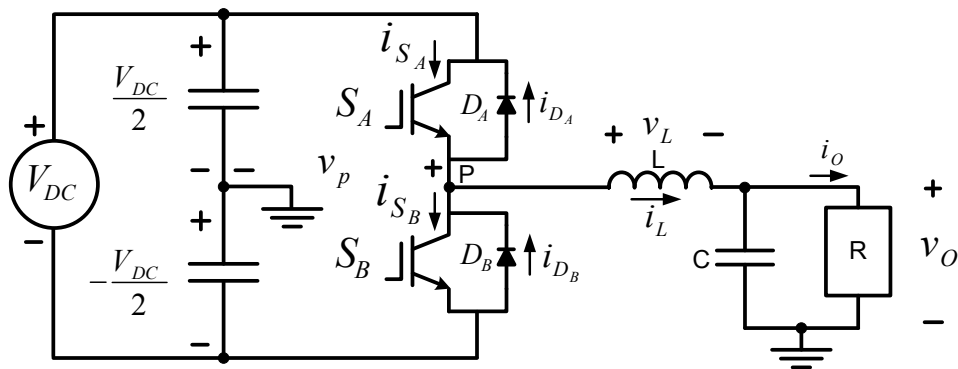


Figure 5.14: Half bridge topology



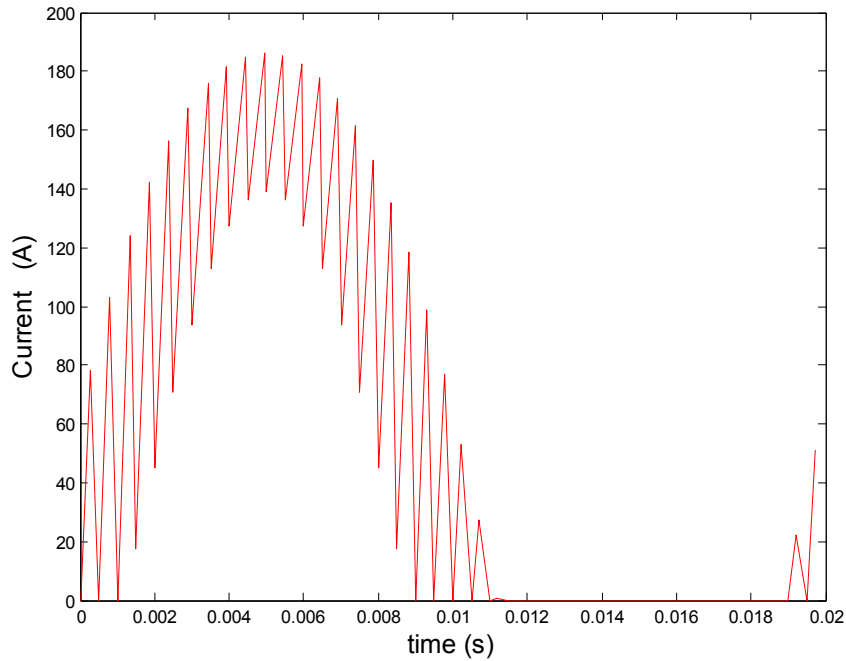


Figure 5.15: Partial inductor current, which flows through IGBT  $S_A$  and diode  $D_B$

The positive inductor current flowing through IGBT  $S_A$  and diode  $D_B$  is shown in Figure 5.15: IGBT  $S_A$  conducts when the gradient of  $i_L$  is positive, whereas diode  $D_B$  conducts when the gradient is negative. This figure is plotted at a switching frequency  $f_s$  equal to 2 kHz and at a large  $\Delta i_L$  for easier visualisation. The average current flowing through IGBT  $S_A$  and diode  $D_B$  is calculated by obtaining the area under the respective line segments with respect to the x-axis. The switching losses of IGBT  $S_A$  are calculated by using the exact current amplitudes on the inductor current  $i_L$ , when IGBT  $S_A$  switches either on or off. IGBT  $S_A$  switches on at the lower envelope of the inductor current  $i_L$  and switches off at the upper envelope amplitudes.

Figure 5.16 shows the simulation strategy of calculating the losses occurring in the switching devices. This flow chart shows that:

1. The system parameters are defined.
2. The intersections of DEPWM and SEPWM are calculated.
3. The inductor current  $i_L$  is separated into the respective components currents.
4. The conduction and switching losses are calculated for both modulation techniques.
5. Steps 3 and 4 are completed as the inductor ripple current  $\Delta i_L$  is iteratively increased.

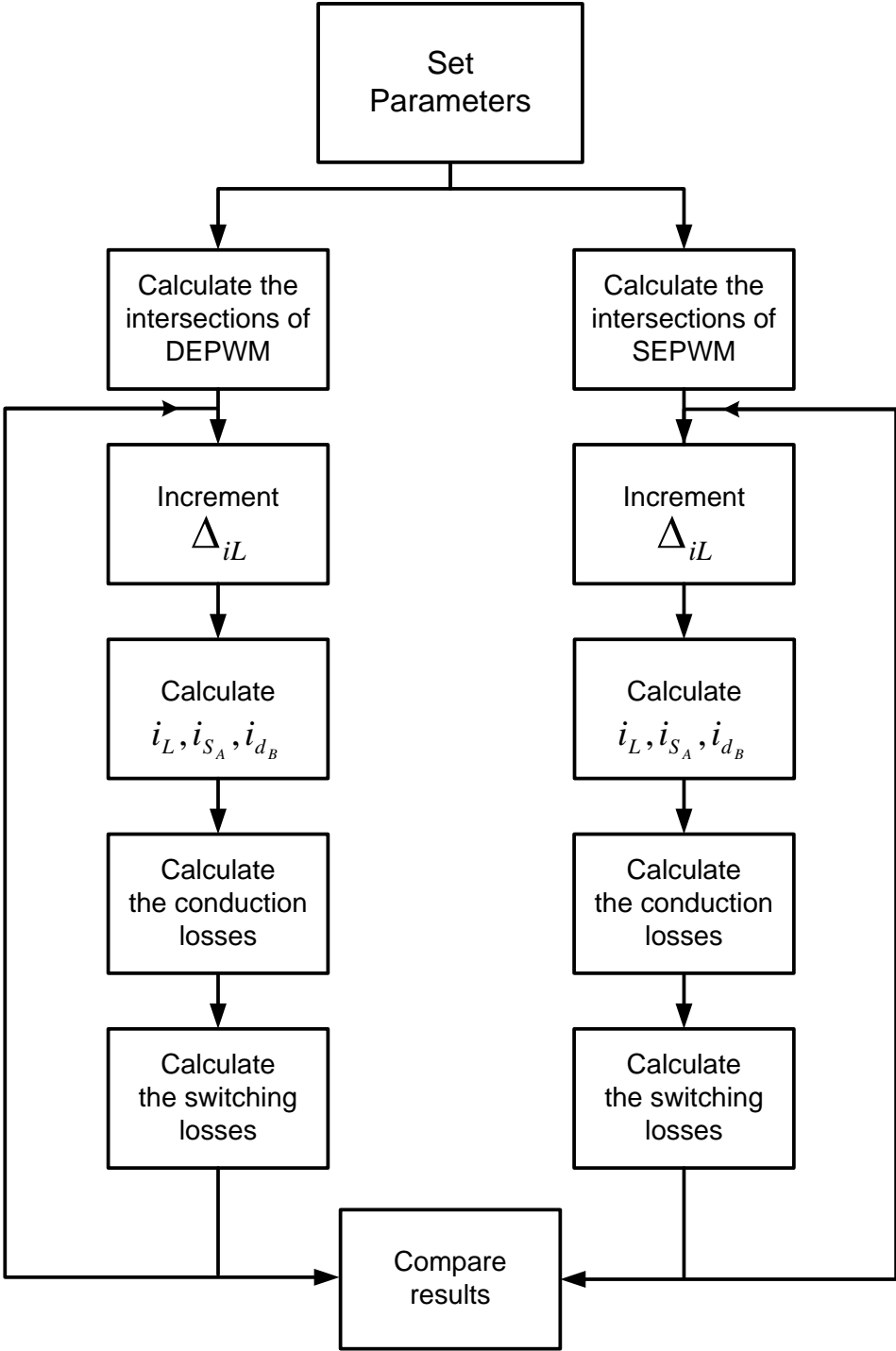


Figure 5.16: The simulation strategy of calculating the losses

### 5.3.6 Switching Losses

The switching losses of IGBT  $S_A$  are calculated numerically by using Equation 5.1 and 5.2, with  $i_C$  being the exact current magnitude on the upper and lower envelopes of  $i_L$ . The turn-off and turn-on transitions of IGBT  $S_A$  occur in the first half cycle of  $i_L$ , on the upper and lower envelopes respectively.

The average value of the lower envelope decreases as  $\Delta i_L$  increases. Thus the turn-on losses decrease as  $\Delta i_L$  increases. The average value of the upper envelope increases as  $\Delta i_L$  increases, and therefore the turn-off losses increase with an increase in  $\Delta i_L$ . The results of the individual switching losses used in the simulation are shown in Figure 5.17. These results demonstrate that the turn-on losses decrease and that the turn-off losses increase as  $\Delta i_L$  is increased.

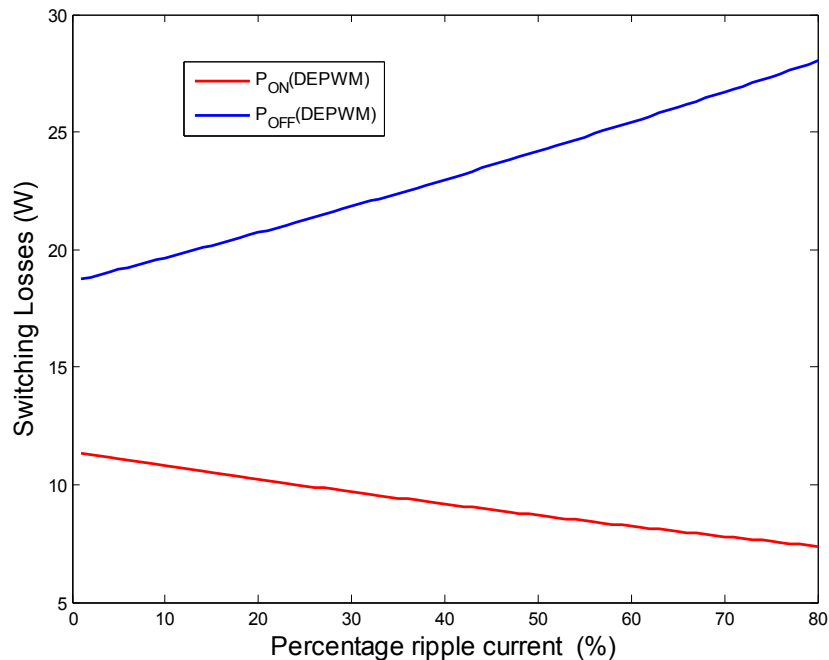


Figure 5.17: Individual switching losses using the numerical method

Figure 5.18 shows the numerical and analytical results of the combined switching losses as  $\Delta i_L$  increases. It can be deduced from these results that the switching losses are identical between the two PWM methods, namely SEPWM and DEPWM. The numerical methods converge to the analytical method as  $\Delta i_L \rightarrow 0$ . Simpler simulations are not included in Fig. 5.18 due to the small time steps that would be required.

The switching losses increase linearly with  $\Delta i_L$ , thus it is necessary to take into account the inductor ripple current  $\Delta i_L$ . A 7% error is made between the two methods at a  $\Delta i_L$  of 40%. This error is therefore substantial for inverters that have large power ratings and that operate under large inductor ripple current  $\Delta i_L$  conditions.

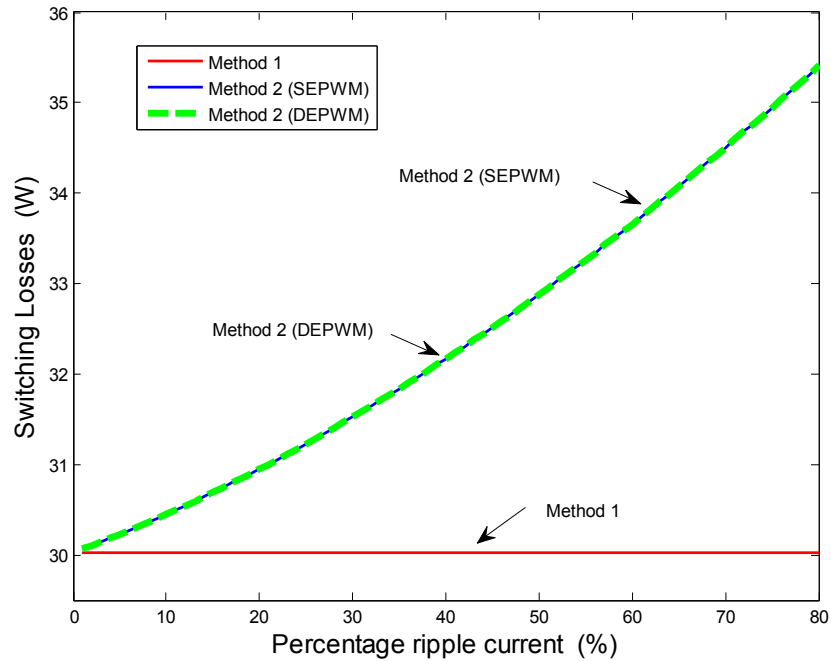


Figure 5.18: Combined switching losses using the numerical method

### 5.3.7 Conduction Losses

Method 1 uses a rectangular pulse train to calculate the conduction losses, as shown in Figure 5.19. The area approximation of each pulse involves taking the rectangular area as being equal to  $I_o \sin(w_1 t_i) \cdot dT_s$ . As a result area  $A_1$  is added and area  $A_2$  is ignored.

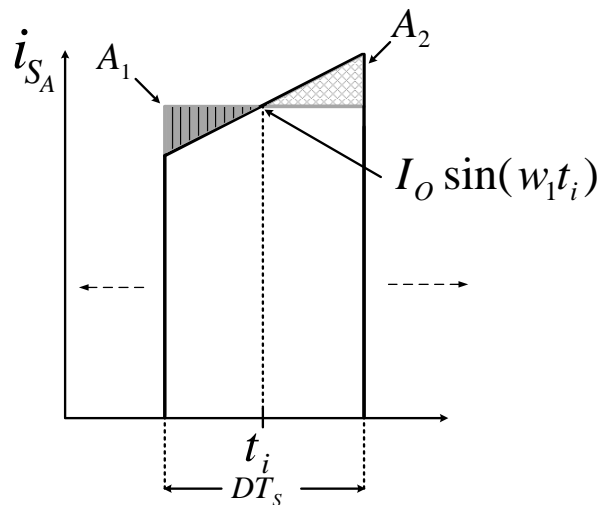


Figure 5.19: Average current approximation

The numerical method calculates the true area under  $i_{S_A}$ , namely  $A_{S_A}$ . This is done to make it possible to compare the results of the two methods.

Figure 5.20 illustrates the area that is calculated to obtain the average current  $I_{S_A}$ . The area approximations include a triangular area when  $i_{lower} < 0$  and a trapezoidal area when  $i_{lower} > 0$ . The unshaded area in Figure 5.20 that is neither triangular nor trapezoidal is ignored. This approximation is made, because this area will eventually enter the triangular area as  $\Delta i_L$  increases.

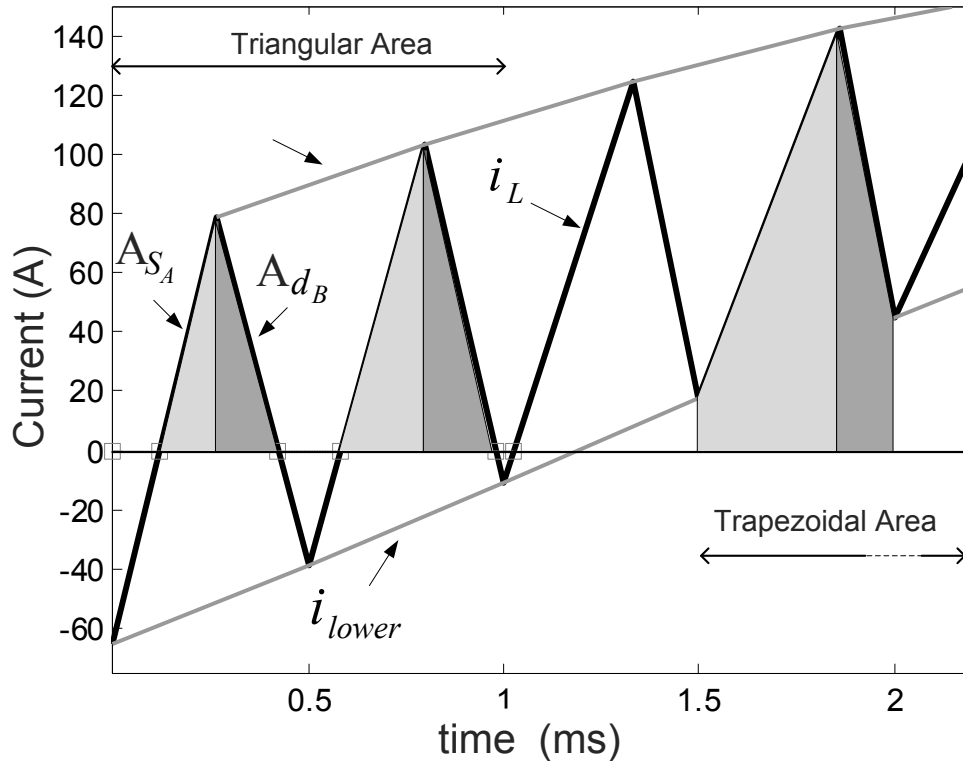


Figure 5.20: Area calculations

Figure 5.21 depicts the results of methods 1 and 2 as well as the Simpler simulation of the average current  $I_{S_A}$ . An increase in  $I_{S_A}$  is noted as  $\Delta i_L$  increases. The ripple in the numerical result is caused by the ignored area eventually being taken into account as  $\Delta i_L$  increases. The difference in amplitude between the two methods is under 1% at a  $\Delta i_L$  of 40%, which means that the approximations of the area in Figure 5.19 are accurate. These results demonstrate that the analytical method is accurate and easy to calculate opposed to the lengthy simulation of the numerical method.

The average diode current  $I_{D_B}$  is similarly calculated by summation of the areas under the diode current  $i_{D_B}$ , namely  $A_{D_B}$ . The results are shown in Fig. 5.22.

The average current  $I_{S_A}$  was calculated using a constant  $\Delta i_L$  of 40% over a range of frequencies. This is done to test the accuracy of the Riemann sum approximation in Equation 5.6 at lower switching frequencies. Fig. 5.23 depicts a negligible error made between the numerical and analytical methods as the switching frequency increases. The inductor ripple current  $\Delta i_L$  and switching frequency  $f_s$  have negligible effects on the analytical methods used in Section 5.2.2.

5.3. METHOD 2

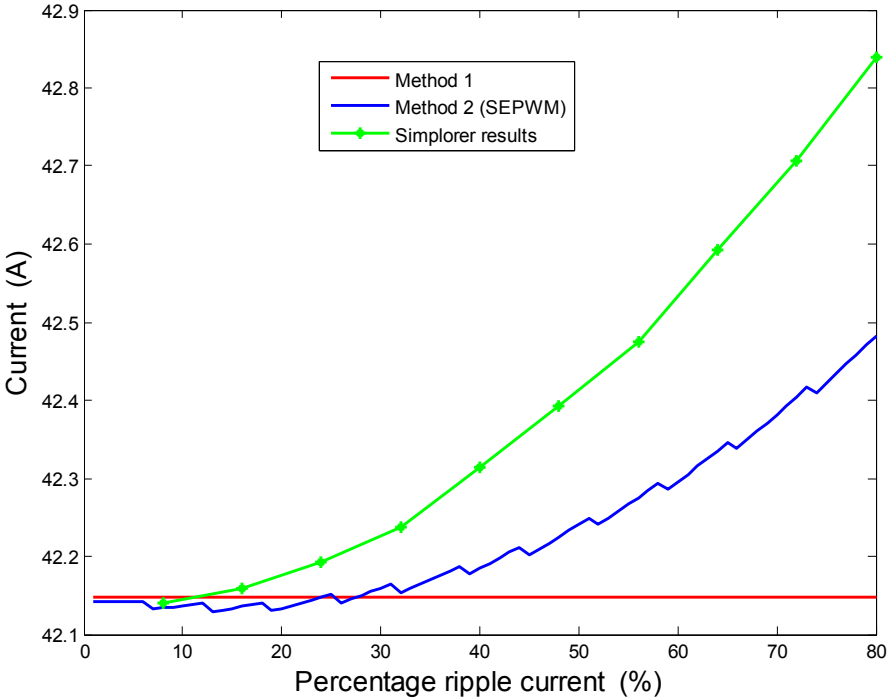


Figure 5.21: Average current through IGBT  $S_A$

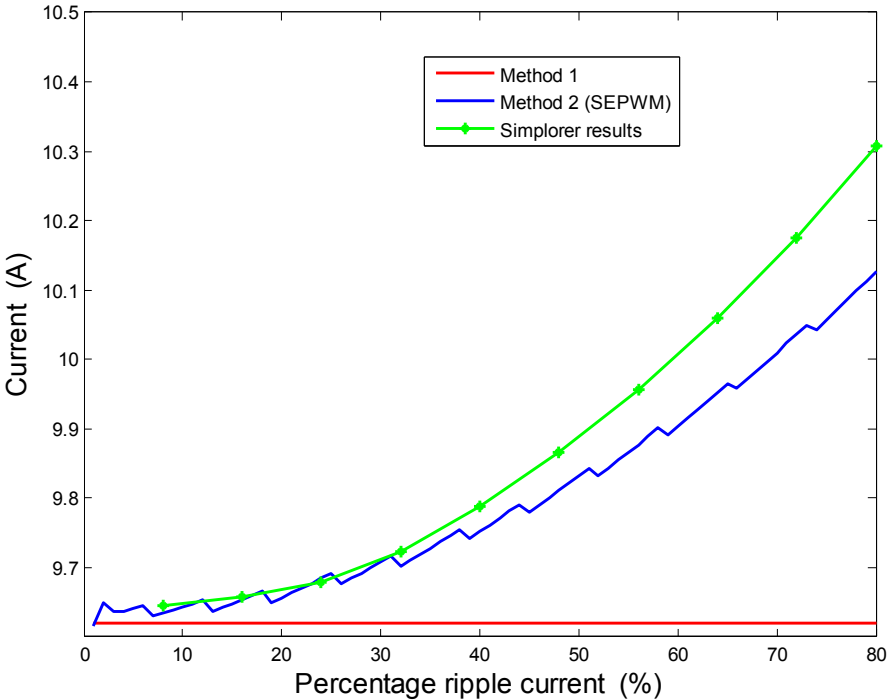


Figure 5.22: Average current through diode  $D_B$

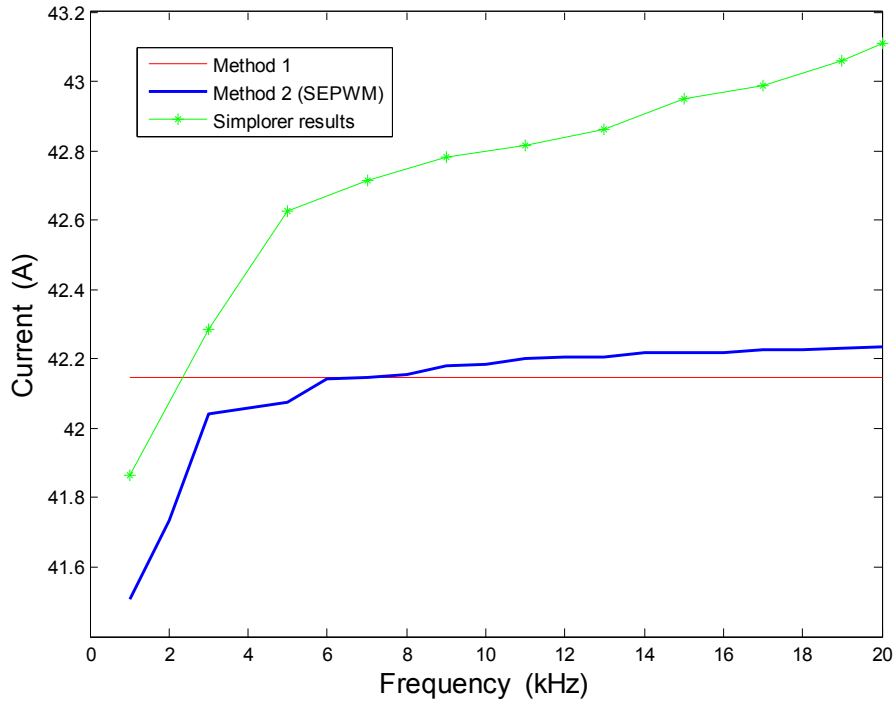


Figure 5.23: Average current through IGBT  $S_A$  vs frequency

### 5.3.8 Conclusion of Section 5.2 and 5.3

To summarize the previous sections, an alternative method is presented to calculate the switching and conduction losses in a half bridge inverter. The numerical loss analysis used an existing inductor current model to determine the exact current flowing through the switches. A comparison was made between the proposed numerical and the existing analytical methods. The numerical results show that the total losses increase as the inductor ripple current increases. The calculation of the losses using the numerical method does not greatly improve the accuracy of the result with regard to the conduction losses. This concluded that the analytical method is accurate for calculating the conduction losses occurring in the switching devices.

The switching losses however increase linearly with the increase in inductor ripple current  $\Delta i_L$ . In other words the turn-on losses decrease and the turn-off losses increase; the combined switching losses, however, increase with  $\Delta i_L$ . A 7% error is made between the two methods at a 40%  $\Delta i_L$ . Thus, it is beneficial to use the numerical method for calculating the switching losses. The information presented in this section was published in [45].

## 5.4 Heatsink Design

From the results obtained in Section 5.2 and 5.3, the individual power losses are calculated in this section. The conduction losses are obtained from the analytical method, as the error between the two methods is negligible in this regard. The switching losses, in contrast, are obtained from the numerical analysis as the error between the two methods was sufficiently significant. These results are summarized in Figure 5.18. The losses are calculated based on a unity power factor using a star connected load.

The single phase component losses at an inductor ripple current of 30% are depicted in Table 5-III. The thermal resistances parameters are also tabulated. The exploded heatsink diagram is shown in Figure 5.24 with the total single phase IGBT and Diode losses given as:

$$P_{IGBT} = P_{Switch(IGBT)} + P_{Cond(IGBT)} \quad (5.25)$$

$$P_{Diode} = P_{Switch(Diode)} + P_{Cond(Diode)} \quad (5.26)$$

The specific temperature drops are also included with a reference ambient temperature of 40°C. Each module consists of two IGBTs and two free-wheeling diodes, thus 3 separate modules are mounted on the same heatsink. The junction temperature of each module is calculated to be 90°C. The maximum safe operating temperature of the junction is 115°C, this temperature margin allows the inverter to be overloaded for short periods.

Table 5-III: Heatsink specifications

Parameters	
$P_{Switch(IGBT)} = 31.6 \text{ W}$	$P_{Cond(IGBT)} = 67 \text{ W}$
$P_{Switch(Diode)} = 33.7 \text{ W}$	$P_{Cond(Diode)} = 11.54 \text{ W}$
$\theta_{J/C}(IGBT) = 0.083 \frac{^{\circ}\text{C}}{\text{W}}$	$\theta_{J/C}(Diode) = 0.15 \frac{^{\circ}\text{C}}{\text{W}}$
$\theta_{C/S}(Module) = 0.045 \frac{^{\circ}\text{C}}{\text{W}}$	$\theta_{S/A}(SEU16) = 0.033 \frac{^{\circ}\text{C}}{\text{W}}$



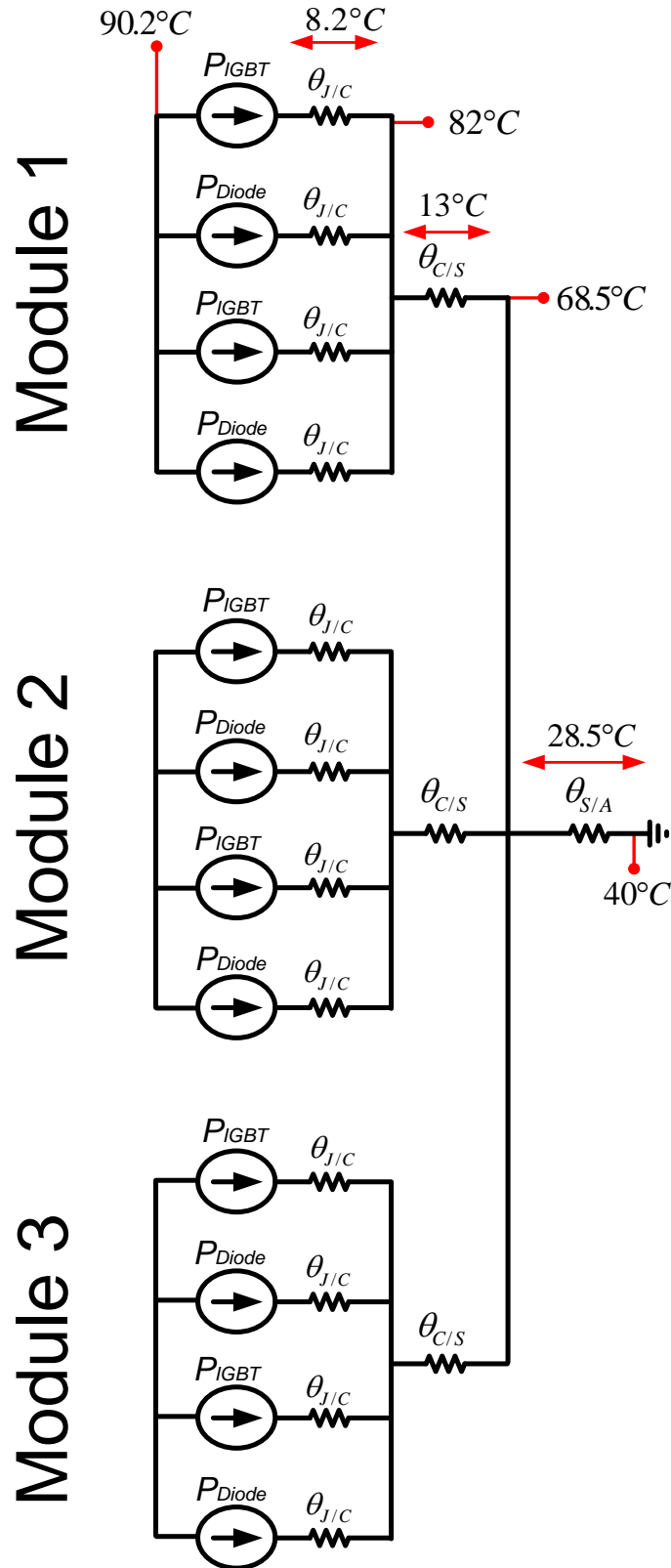


Figure 5.24: Heatsink representation

## 5.5 Bus Capacitor Design

The DC bus voltage  $V_{DC}$  is obtained from 45 DC-DC converters of the SST, the secondary's of these converters are all connected in parallel. Each DC-DC converter utilizes a center point rectifier, and thus a center point connection is provided for the DC-AC inverter. The switching signals of the DC-DC converters are also interleaved, thus the assumption is made that the 50 Hz current flows through the IGBTs and returns via the center point connection to the rectifiers. The interleaved output rectifiers therefore allow less current to flow through the bus capacitors.

However, the ripple current from the phase currents will be sourced/absorbed by the bus capacitors. The amplitude of the maximum ripple current is obtained from Equation 5.12 and amounts to 48.7 A. This current is therefore the same current that flows through the filter capacitors. The maximum rms current entering the filter capacitors is calculated by assuming that the current entering the capacitors is triangular. This triangular waveform is also assumed to have a continuous amplitude of 48.7 A. The rms value of the current that flows through the filter capacitors is calculated by [50]:

$$\begin{aligned} I_{rms(C1)} &= \frac{I_{Peak}}{2\sqrt{3}} \\ &= 14.5A \end{aligned} \quad (5.27)$$

The worst case scenario of the current flowing in the bus capacitors is three times this value due to the three phase currents. This assumes that no current will be cancelled between phases, and the varying sinusoidal ripple current is assumed to have a constant amplitude. The bus capacitors therefore do not need very high current ratings; rather, they need a high capacitance for energy storage. The larger the energy storage, the more effective the SST will be in isolating voltage dips entering the primary of the transformer.

For this prototype, a 14.1 mF bus capacitance is used, thus 6 parallel rows of series linked electrolytic capacitors with a value of 4700  $\mu$ F. The national voltage requirements from the NRS-048 state that the voltage should be within a 6% tolerance, thus the minimum peak output voltage  $V_{O(peak)}$  should be greater than 306 V. The output voltage is proportional to:

$$V_{O(peak)} = m_a \frac{V_{DC}}{2} \quad (5.28)$$

Defining the modulation index  $m_a$  to be 0.95, the minimum bus voltage  $V_{DC}$  is given by:

$$\begin{aligned} V_{DC} &= \frac{2V_{O(peak)}}{m_a} \\ &= 644V \end{aligned} \quad (5.29)$$

The power that the inverter delivers is 80 kW, thus the time that the bus capacitors will be able to keep the output voltage within the specified tolerance is given by:

$$time = \frac{Energy}{Power} \quad (5.30)$$

$$\begin{aligned}
 &= \frac{\frac{1}{2} \cdot 14.1mF \cdot (800^2 - 644^2)}{80000} \\
 &= 19.85 \text{ ms}
 \end{aligned}$$

Thus should a dip occur on the 11 kV supply, the SST would be able to keep the output voltage within specifications for almost a complete cycle of the 50 Hz waveform.

## 5.6 Efficiency

The total losses of the system are comprised of both the switching device losses and the passive losses. Based on Section 5.4, the total switching device losses are calculated to be 863 W. The passive component losses consist of the losses in the filter inductors, the filter capacitors and the bus capacitors.

In the previous section the worst case rms current flowing through the filter capacitors was calculated to be 14.5 A. The equivalent series resistance (ESR) of the filter capacitor  $r_{C1}$  is obtained from the data sheet, and it amounted to 2.5 mΩ. The losses in the filter capacitors  $C_1$ ,  $C_2$  and  $C_3$  are therefore approximated as:

$$\begin{aligned}
 P_{FilterCap} &\approx 3 \cdot I_{rms}^2 \cdot r_{C1} & (5.31) \\
 &= 3 \cdot 14.5^2 \cdot 2.5 \text{ m}\Omega \\
 &= 1.57 \text{ W}
 \end{aligned}$$

The losses in the bus capacitors are approximated by taking three times the filter capacitor current squared and multiplied with the equivalent resistance  $r_{Bus}$ :

$$\begin{aligned}
 P_{BusCap} &\approx I_{rms}^2 \cdot r_{Bus} & (5.32) \\
 &= 43.5^2 \cdot 4.05 \text{ m}\Omega \\
 &= 7.6 \text{ W}
 \end{aligned}$$

The power loss of the bleeding resistors across the bus capacitors amounted to 58.2 W. The losses in the inductors are calculated similarly, by first obtaining the rms current. The rms current flowing through the filter inductor  $L_1$  is equal to the load current, namely  $I_{o(rms)}$ . The ESR of the inductors were measured to be 2.27 mΩ, thus the conduction losses are given by:

$$\begin{aligned}
 P_{L1} &= 3 \cdot I_{o(rms)}^2 \cdot r_L & (5.33) \\
 &= 3 \cdot 115^2 \cdot 2.27 \text{ m}\Omega \\
 &= 90.06 \text{ W}
 \end{aligned}$$

The inductors were bought and no data is available regarding the core losses or skin effect of the conductors. Thus, the losses in the inductors are expected to be larger than predicted in Equation 5.33. The ESR was measured using a resistance meter capable of measuring very small resistances; this device injects a DC current and measures the voltage across the device

being tested. The skin effect is therefore not taken into account by the resistance meter.

The total efficiency of the inverter is given by:

$$\begin{aligned} \eta &= \frac{P_{Out}}{P_{Out} + P_{Losses}} \\ &= \frac{80 \text{ kW}}{80 \text{ kW} + 963 \text{ W}} \\ &= 98.8\% \end{aligned} \tag{5.34}$$

The efficiency of the inverter has not been tested, as a 80 kW DC source was not available in the laboratory. However, the inverter was tested at full voltage and full current in [9]; this was done by shorting out the output capacitors and reducing the modulation index. This configuration allows minimal current to be drawn from the supply, as the energy in the inductors and bus capacitors is continuously exchanged. This measurement is mainly done to test the ratings of the semiconductors. The temperature of the heatsink was measured in this configuration, and is shown below [9; 51]:

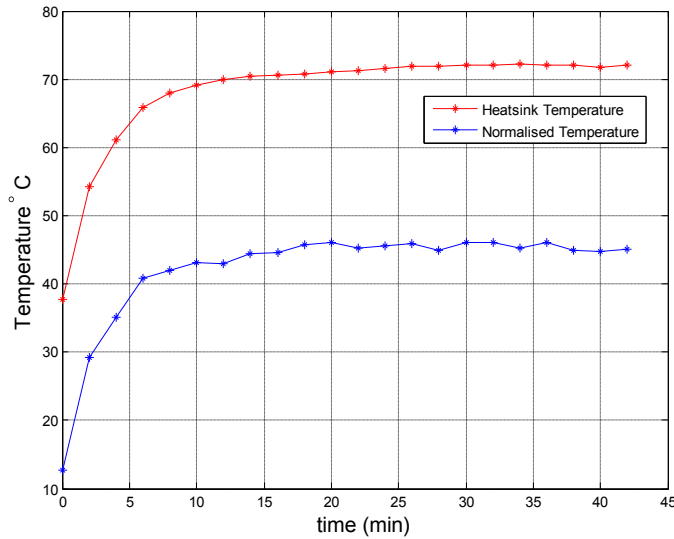


Figure 5.25: Heatsink temperature taken from [9]

Figure 5.25 depicts the measured heatsink temperature as well as the normalised temperature with respect to the ambient temperature. These results show that a 45 °C drop occurred across the heatsink as the temperature stabilized. Thus the total power  $P_{total}$  that is emitted in the heatsink is given by:

$$\begin{aligned} P_{total} &= \frac{\text{temperature}}{\theta_{S/A}(SEU16)} \\ &= \frac{45^\circ C}{0.033 \frac{^\circ C}{W}} \\ &= 1363 \text{ W} \end{aligned} \tag{5.35}$$

The power  $P_{total}$  is not a conclusive comparison to the theoretical prediction as the test setups vary, due to the modulation index and output voltage. It is possible to conclude from the temperature measurement, however, that the maximum junction temperature is not exceeded.

The measured efficiency will be compared to the theoretical calculations in the future with the 45 cells connected as a source. The inverter's modulation index as well as load will be set identical to the theoretical specifications.

## 5.7 Conclusion

The chosen topology for the three phase inverter was the half bridge converter, as it provides a center point connection between its bus capacitors. The operation of this type of inverter was briefly described; it forms the basis of the loss calculations discussed in this chapter. An alternative method was implemented to calculate the switching and conduction losses in a half bridge inverter. The numerical loss analysis was done using an existing inductor current model. The aim of this was to determine accurately the current flowing through the switches. A comparison was made between the proposed numerical method and the existing analytical method. The already existing analytical results were therefore used as a basis for comparison with the findings of the numerical method. The findings of this chapter were published in [45]. The design of the inverter was included herein, based on the results of the loss analysis. Lastly, the efficiency of the three phase inverter was also discussed.

## Chapter 6

# Inverter Control Strategy

The main purpose of the SST is to improve the characteristics of the conventional distribution transformer, the improvement of power quality is thus critical. As the power rating of the SST is relatively small, the advantages that it can offer to the supply grid are limited. The main advantages of the SST relate to the low voltage output stage, this stage is required to provide near perfect regulation and undistorted output voltages regardless of the load.

The main technical challenge of the SST, however, is still based on the high voltage series stacked converter, due to the complexity of this converter. However, the output stage is just as important in the SST concept with regard to power quality improvement. This chapter focuses on the control of the DC-AC inverter, the block diagram of this stage is shown in Figure 6.1.

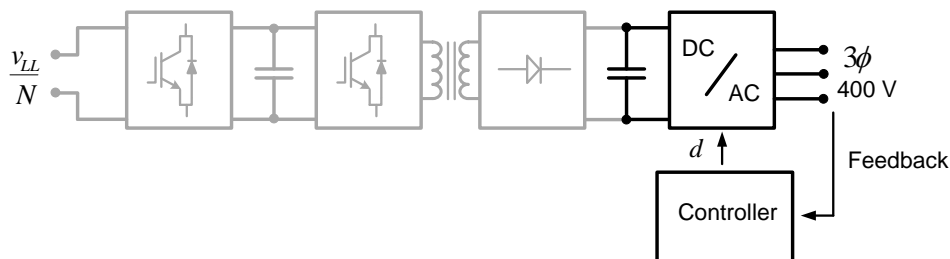


Figure 6.1: Output stage of the SST

As the SST is currently in the research phase, the specific load requirements are not yet known; for example, the SST could simply be connected to a load that is disconnected from the grid. Alternatively, the SST could be connected to the grid, in which case the output stage would act as a grid source inverter. As a grid source inverter injects current into the network, thus the output voltage of the grid is not controlled. The control techniques of the output stage should therefore be designed by taking the above into consideration. To mimic the conventional distribution transformer, the output voltages of the inverter are required to adhere to the specifications of the South African voltage standards, namely the NRS-048. To increase the feasibility of the SST, the tolerances of the output voltages should fall well within these standards. The control techniques of the output stage should therefore be chosen carefully in order to improve the quality of the supply voltage on the output of the SST.

## 6.1 Control of DC-AC Inverters

There is a significant amount of research available regarding the control of DC-AC inverters. For the purpose of researching the control strategy, the focus was mainly on journal publications. This section therefore gives a detailed summary and explanation of the relevant literature regarding the control of DC-AC inverters.

In general, controllers can be implemented using either analogue circuitry or a digital processor is used. The main benefit that analogue controllers have over digital controllers is that their feedback parameters are kept in the continuous domain. Simply put, the controller has continuous knowledge of the feedback parameters. An example of an analogue inverter control strategy, namely one-cycle control, is presented in [52]. This method utilizes an analogue integrator circuit with flip flops and comparators. The control strategy operates by integrating the half leg voltage until the result is equal to the reference signal, thereby achieving a form of average voltage control. This method provides many benefits to audio amplifiers, although the concept can also be extended to high power inverters.

Nonetheless, analogue control techniques do have many disadvantages over digital controllers. The main disadvantage is that the design of analogue controllers is difficult and that small alterations involve lengthy and tedious procedures. In addition, the parameters of the passive components used to realize the poles and zeros of the controller vary with temperature and age. Digital controllers have the following advantages over analogue controllers [35]:

- Digital controllers can be re-programmed which greatly reduces the design time.
- Improving or tweaking the controller design does not increase the size of the hardware.
- Digital controllers are not affected by temperature, humidity or other atmospheric conditions.
- Eventual mass production of the controller is cheaper as no components need to be tweaked.

In view of the above, a digital controller is chosen for the DC-AC inverter. Digital controllers operate with a finite sampling time, thus limiting the feedback parameters to a periodic informative stream. Digital control strategies can thus be implemented by discretizing the continuous domain signals. Factors that limit the implementation of inverter control systems are the DSP's processing speed and the ADC conversion times. These factors of the DSP have greatly improved, which enables instantaneous control instead of RMS based control, as used in the past.

Inverters were previously controlled using a single outer voltage loop, the advantage of that method was that it had a simple design but a relatively slow response. Such a single loop controller is depicted in Figure 6.2. A faster response can be obtained by increasing the gain of the PI controller but this has an adverse affect on the noise entering the system.

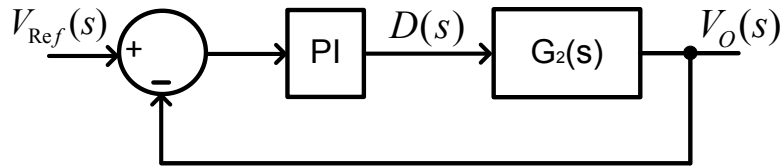


Figure 6.2: Single loop strategy

A double loop strategy consisting of an inner current loop and outer voltage loop is introduced for a faster response. This method effectively splits the output filter into two single order systems, simplifying the design of the outer loop. The outer voltage loop is fed by a unity gain current source. The inner loop controls the inductor current, while the outer loop controls the load voltage. Figure 6.3 depicts the double loop control strategy.

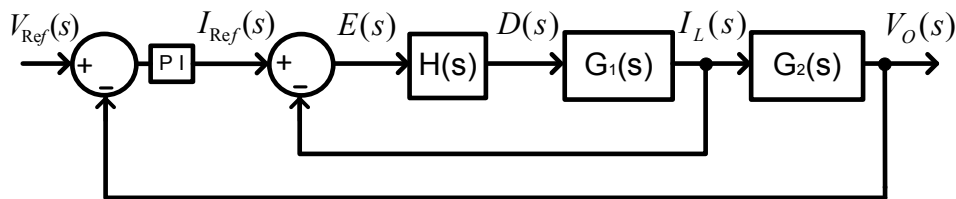


Figure 6.3: Double loop control strategy

The second order system of the LC output filter can be broken up into two single order systems, if the bandwidth of the inner current loop is much higher than the bandwidth of the outer loop. The separation of the poles has an advantage, as the inner loop is modelled as a unity gain with respect to the bandwidth of the outer loop. The outer voltage loop design is therefore only dependent on the filter capacitor and the load impedance. The transfer function of the outer voltage loop has a current input with a voltage output.

Due to the uncertainty of the load of the SST, a single or double loop control strategy could be required for the output stage. In the event of the inverter being connected to the grid, only the inner current loop is required to inject current into the network. Should the inverter act as a voltage source inverter, a double loop control strategy would be required. The double loop control strategy is however chosen for the output stage of the SST. This is done as the outer voltage loop can simply be removed, depending on the required use. The inner current loop is therefore required to operate in both working environments, namely connected to the grid or disconnected from the grid.

## 6.2 Chosen Inner Loop Controller

A remarkable amount of literature is available concerning control strategies for inverters. These strategies range from hysteresis control to ramp control. Other strategies include state space control, observer control and predictive control. Refer to Chapter 2 for the discussion regarding



these control strategies. The predictive control route is chosen for the control strategy in this project, based on the literature given in [10; 35]. This decision is based on the computational time required to implement the respective algorithms in a fixed point DSP. A fixed point DSP is chosen for the controller, namely the TMS320F2808 from Texas Instruments. This device is chosen due to the reduced cost with respect to FPGA and floating point DSPs. The relevant literature regarding the control algorithms is briefly discussed below.

Conventional predictive control is done by calculating the voltages in the inverter and using this to force the inductor current to follow the reference current. The concept of this strategy is shown in Figure 6.4, where the sampling points are referred to as  $SP$  and the controlling points are referred to as  $CP$ . Conventional predictive controllers sample at  $SP(N - 1)$  and predict what the current and voltage will be at  $CP(N - 1)$ . The duty cycle is therefore set at  $CP(N - 1)$  by using the samples obtained at  $SP(N - 1)$ . The target of this control strategy is therefore to set the duty cycle that the inductor current matches the reference current at the beginning of the next switching period.

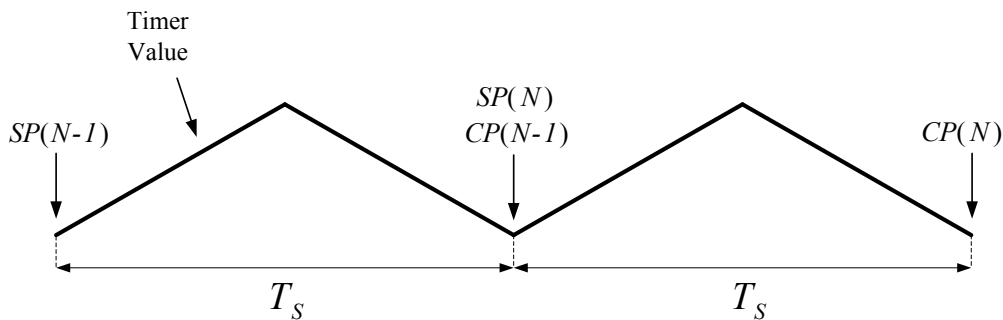


Figure 6.4: Concept of conventional predictive control taken from [10]

However, this method has poor robustness to mismatches in the system parameters, especially in the value of the filter inductor. Due to the increased computational ability of DSPs, a robust predictive controller could be developed. The concept of this is shown in Figure 6.5; here the sampling time is shown to be shifted  $\Delta$  before the start of the switching period. The time interval  $\Delta$  is defined as the time taken to sample and complete the computation of the duty cycle. The voltages and currents are predicted using the samples taken at  $SP(N)$ , while the duty cycle is set at  $CP(N)$ . This shifted sampling time improves the response of the system. The information regarding the sampling times in [10] is therefore used to implement the predictive control strategy.

The duty cycle algorithm is obtained using an alternative method, namely the superposition of the inductor current. This method was used in [35] for the control of a full bridge converter using unipolar switching. The controller described in this chapter utilizes this technique and extends the control algorithm to a half bridge converter. The extension of this method was published in [53]. The next section discusses the presented controller.

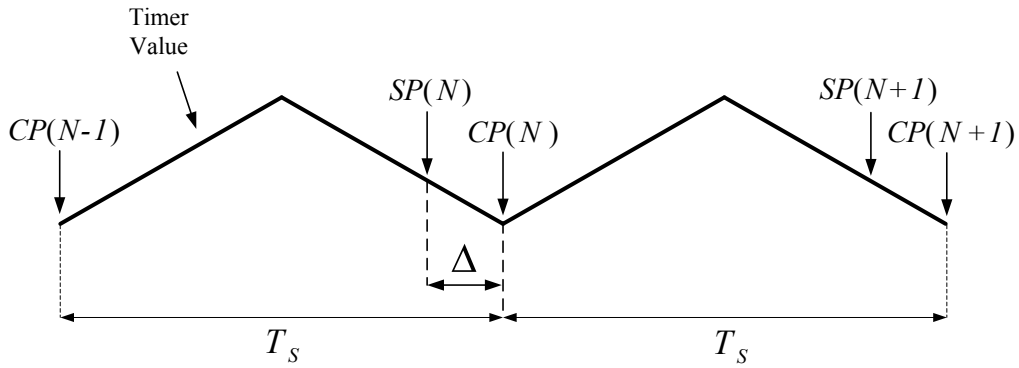


Figure 6.5: Concept of robust predictive control taken from [10]

### 6.3 Inner Loop Current Controller

The control strategy is based on the single phase inverter shown in Figure 6.6. The DC bus voltage is defined as  $V_{DC}$  with  $L$  and  $C$  given as the filter components. The inductor current is defined as  $i_L$  and the load voltage is given as  $v_o$ .

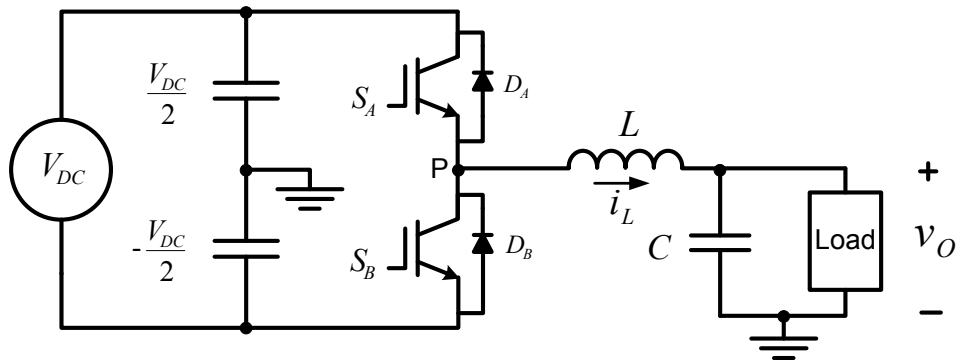


Figure 6.6: Single phase half bridge inverter

The principle of superposition of the inductor current  $i_L$  is based on the inductor ripple current  $\Delta i_L$  over the switching period  $T_s$ . The half bridge inverter has only one of two states, as opposed to the four states in a uni-polar full bridge converter. The first state is defined as the time interval where the half leg voltage is equal to  $\frac{V_{DC}}{2}$ . In this state, the inductor current flows through either IGBT  $S_A$  or diode  $D_B$  for a positive inductor current  $i_L$ . The second state is defined as the time interval where the half leg voltage is equal to  $\frac{-V_{DC}}{2}$ . The two states are shown in Figure 6.7. The changes in inductor current of state 1 and 2 are defined as  $\Delta i_{L1}$  and  $\Delta i_{L2}$  respectively.

The change in amplitude of the inductor ripple current  $\Delta i_L$  from one cycle to the next is therefore defined as  $\Delta i_L = \Delta i_{L1} + \Delta i_{L2}$ . For example, assuming that  $\Delta i_{L1} = 10$  A and  $\Delta i_{L2} = -4$  A, then the total change in inductor current  $\Delta i_L$  for that switching period  $T_s$  is calculated as 6 A. Thus, if the duty cycle  $d$  is set accordingly, the change in inductor current  $\Delta i_L$  in each switching period  $T_s$  can be set to follow the reference current  $i_{ref}$  cycle by cycle.

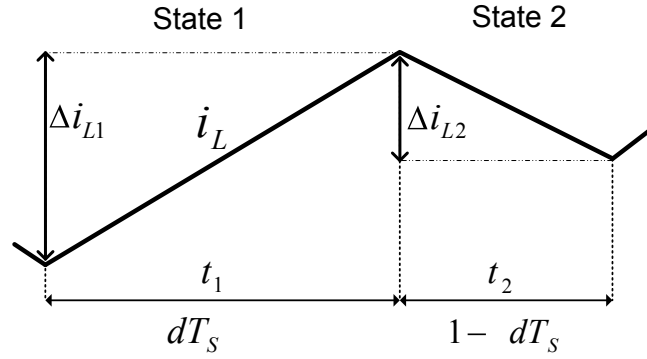


Figure 6.7: State definitions

### 6.3.1 Derivation of the Predictive Controller

The derivation of the controller in this section assumes that all components are ideal and that the output voltage  $v_o$  remains constant throughout the switching period  $T_s$ . This assumption is accurate, as the switching period  $T_s$  is equal to  $100 \mu\text{s}$ ; this time is negligible, compared to the  $20 \text{ ms}$  period of the output voltage  $v_o$ .

The inductor ripple current of each state is obtained by referring to Figures 6.6 and 6.7. The change in inductor current  $\Delta i_{L1}$  in State 1, is given by:

$$\Delta i_{L1} = \frac{\frac{V_{DC}}{2} - v_o}{L} \times t_1 \quad (6.1)$$

The change in inductor current  $\Delta i_{L2}$  in State 2, is given by:

$$\Delta i_{L2} = \frac{\frac{-V_{DC}}{2} - v_o}{L} \times t_2 \quad (6.2)$$

During one switching period both states occur, and the time interval of each state is dependent on the duty cycle  $d$ . The aim is therefore to obtain an equation for the duty cycle  $d$  to force the inductor current error to zero by the start of the next switching period  $T_s$ . Thus  $\Delta i_L$  is defined as the difference in current between the reference current and the measured current. Using superposition of these two expressions over one switching period:

$$\begin{aligned} \Delta i_L &= \Delta i_{L1} + \Delta i_{L2} \\ &= \left( \frac{\frac{V_{DC}}{2} - v_o}{L} \times t_1 \right) + \left( \frac{\frac{-V_{DC}}{2} - v_o}{L} \times t_2 \right) \end{aligned} \quad (6.3)$$

Noting that the switching period  $T_s$  is equal to:

$$T_s = t_1 + t_2 \quad (6.4)$$

Substituting Equation 6.4 into Equation 6.3:

$$\Delta i_L = \left( \frac{V_{DC}}{2} - v_o \right) \times \frac{t_1}{L} + \left( \frac{-V_{DC}}{2} - v_o \right) \times \frac{(T_s - t_1)}{L} \quad (6.5)$$

Defining  $d = \frac{t_1}{T_s}$  and rearranging terms in Equation 6.5, the duty cycle of IGBT  $S_A$  is obtained as:

$$d = \left( \Delta i_L \times \frac{L}{V_{DC} \cdot T_s} \right) + \frac{1}{2} + \frac{v_o}{V_{DC}} \quad (6.6)$$

The duty cycle  $d$  is related to the change in inductor current over one switching period, thus providing a method of controlling the inductor current. Inserting the reference  $i_{ref}$  and inductor current  $i_L$ , Equation 6.6 is therefore given as:

$$d = \left( (i_{ref} - i_L) \times \frac{L}{V_{DC} \cdot T_s} \right) + \frac{1}{2} + \frac{v_o}{V_{DC}} \quad (6.7)$$

According to Equation 6.7, only three parameters are sampled once per switching period  $T_s$ , namely  $V_{DC}$ ,  $v_o$  and  $i_L$ . Thus, highlighting the low computational requirements for calculating the algorithm in the DSP. Refer to Appendix C for the schematic of the measurement PCB.

Figure 6.8 is a graphical analysis of the controller. The required samples are first taken at  $(T_s(N) - \Delta)$  and then  $d(N)$  is set to eliminate  $\Delta i_L(N)$ . As depicted in Figure 6.8, the actual current is always one cycle behind the reference. The time increment that is required for the computation of the duty cycle, from sampling the parameters to setting the duty cycle register, is defined as  $\Delta$ .

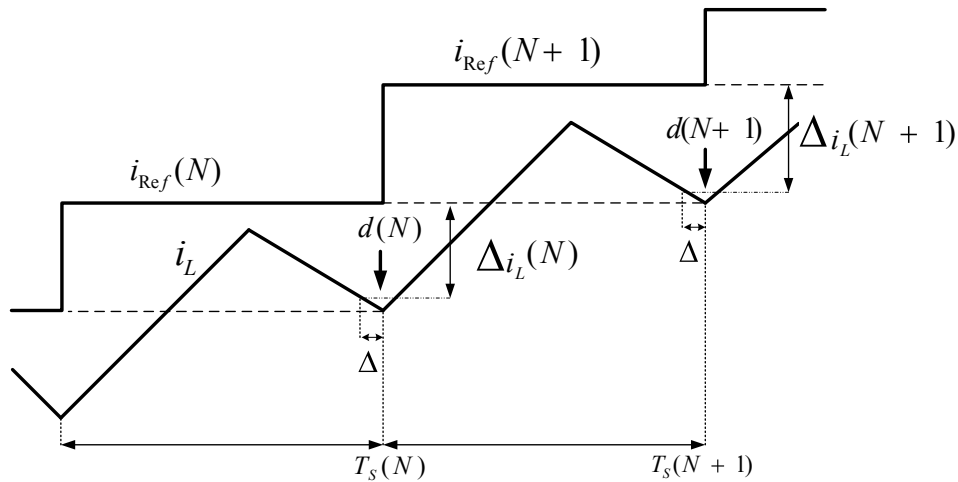


Figure 6.8: Timing strategy of the predictive control method

An error is introduced in the duty cycle  $d(N)$ , because the inductor current  $i_L$  is sampled at  $(T_s(N) - \Delta)$  instead of at  $T_s(N)$ . Compensation for the extra delay should be taken into account, depending on the length of  $\Delta$ . Other methods in the literature predict the inductor current  $i_L$  at  $T_s(N)$  by using linear extrapolation. The duty cycle  $d$  is then calculated with

these predicted values. Ignoring the computational delay in the control design could lead to an under-damped response, depending on the length of the computational delay  $\Delta$  [54].

Figure 6.9 illustrates the DSP implementation of Figure 6.8. A sawtooth carrier waveform is used and defined as single edge pulse width modulation (SEPWM).

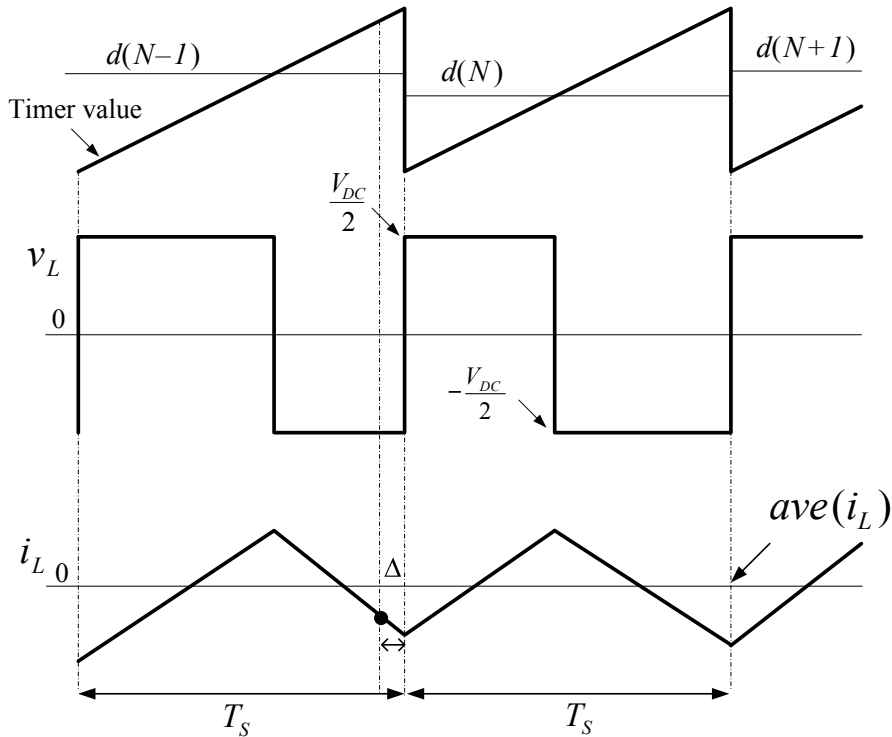


Figure 6.9: DSP implementation of the SEPWM carrier waveform

The computational time  $\Delta$  taken in the DSP to calculate the control algorithm, namely that of Equation 6.7, was initially measured as  $20 \mu\text{s}$ . This lengthy delay was caused by the algorithm being calculated using floating point variables in a fixed point DSP. The transient response of the inner loop current controller was therefore poor due to this large delay. The time delay  $\Delta$  was however reduced to  $3.4 \mu\text{s}$  by calculating the duty cycle with the use of 32-bit integers. It is worth mentioning that the computational delay  $\Delta$  obtained in [10] was measured as  $10 \mu\text{s}$ . This improvement in  $\Delta$  therefore makes this implementation viable in a fixed point DSP.

The computational time of  $\Delta = 3.4 \mu\text{s}$  with respect to the switching period of  $T_s = 100 \mu\text{s}$  is very small. Due to this improvement in the computational time  $\Delta$ , it was decided to use the measured values at time  $(T_s(N) - \Delta)$  instead of predicting the inductor current  $i_L$  at  $T_s(N)$ .

The emphasis in the literature with regard to predictive current control is to reduce the current error within one switching period  $T_s$ . In reality this is extremely difficult to achieve. Control stability can also be lost by increasing the gain of the system out of proportion, in order to reduce this error within one switching period  $T_s$ . If the current error is settled within two or three switching periods  $T_s$ , the transient response is still acceptable with respect to the supply frequency of 50 Hz. Thus, the current controller for the output stage of the SST is focused on

stability and the transient response is considered thereafter. The analysis of the control system is discussed in the next section.

### 6.3.2 Inner Loop Control Analysis

The control analysis of the inner loop is based on Equation 6.7, with the third term considered constant throughout  $T_s$ . The first term therefore results in the most significant change in inductor current  $i_L$ . A continuous domain proportional feedback loop is formed and depicted in Figure 6.10.

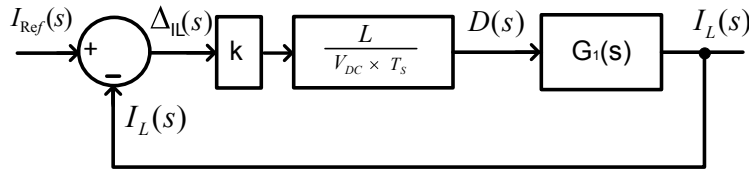


Figure 6.10: Inductor control loop

Defining the open loop gain as follows:

$$k \times k_2 = k \times \frac{L}{V_{DC} T_s} \quad (6.8)$$

The transfer function of the inner current loop is defined as  $G_1(s) = \frac{I_L(s)}{D(s)}$  and is derived using the state space averaging method of Middlebrook and Cúk. The transfer function  $G_1(s)$  is given as:

$$G_1(s) = \frac{V_{DC} \cdot \left( \frac{s}{L} + \frac{1}{LC(R_L + r_C)} \right)}{s^2 + s \left( \frac{L + R_L C(r_L + r_C)}{LC(R_L + r_C)} \right) + \frac{R_L^2 + R_L(r_L + r_C)}{LC(R_L + r_C)^2}} \quad (6.9)$$

The inductance  $L$  is  $500 \mu H$  and is designed on the basis of the permissible ripple current. The equivalent series resistances of the passive components are defined as  $r_L$  and  $r_C$ . The load resistance  $R_L$  and the other parameters are tabulated in Table 6-I.

Table 6-I: Inverter parameters

Parameters	
$V_{DC} = 800 \text{ V}$	$T_s = 100 \mu s$
$L = 500 \mu H$	$C = 100 \mu F$
$R_L = 5.4 \Omega$	$r_C = 33 \text{ m}\Omega$
$r_L = 30 \text{ m}\Omega$	

The controller is designed by means of direct digital methods, thus  $G_1(s)$  is transformed directly to the  $z$  domain. This is done using a zero order hold transformation, because this takes into account the sample and hold effect of the ADC. The  $z$ -domain transfer function is given as:

$$k.k_2.G_1(z) = \frac{k \times k_2 (154z - 127.8)}{z^2 - 1.64z + 0.8215} \quad (6.10)$$

The root locus plot of Equation 6.10 is shown in Figure 6.11. The root locus depicts the closed loop poles as the gain  $k$  is altered.

Interpretation of the root locus plot reveals that the gain can vary from 0 to 2, before exiting the unit circle and causing the system to become unstable. The gain may never be zero for obvious reasons, which means that  $L$  and  $V_{DC}$  may not be zero. The proportional gain  $k$  can therefore be increased to obtain a faster response time. A proportional gain of  $k = 1$  was used in the control system, because the measured response time was acceptable at this gain. Increasing this gain  $k$  above 1 diminishes the current error faster, however, the system overshoot increases. The next section discusses the results of the inner loop controller.

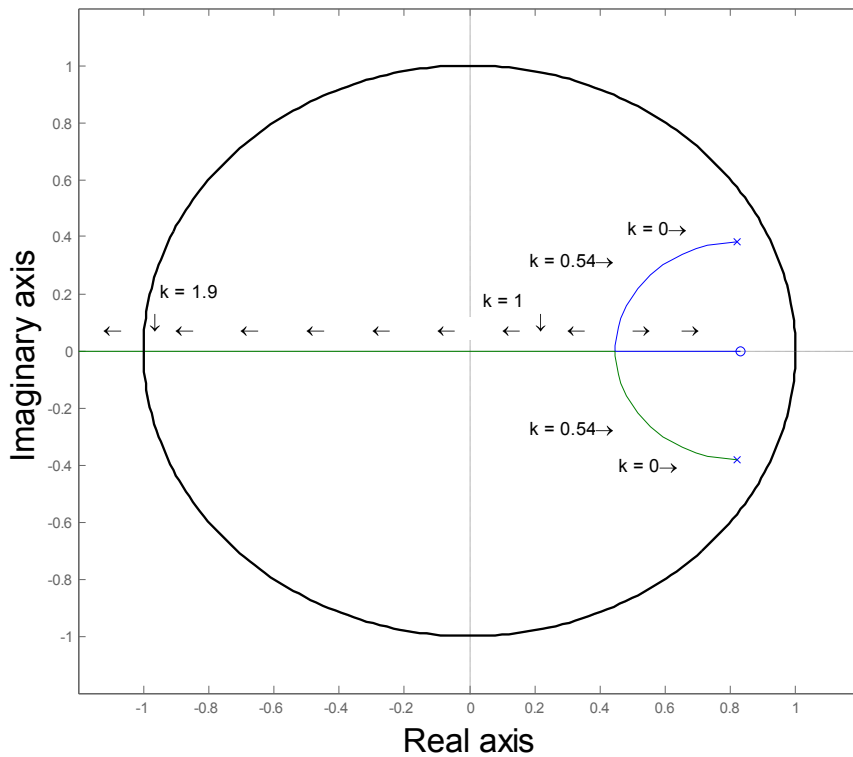


Figure 6.11: Root locus of Equation 6.10

### 6.3.3 Current Controller Results and Analysis

This section discusses the simulations and results of the inner loop current controller. The simulation package Simpler 7 was used to simulate the inner loop current controller. The DSP controller samples the parameters once per switching period  $T_s$ , and the simulations were thus implemented using the same technique. This was done by using dummy interrupts, which sampled the variables, thereafter the variables were held constant throughout the switching period  $T_s$  exactly as would be done in the DSP. This was done to obtain an accurate comparison between the simulated and measured results.

Figures 6.13 and 6.14 depict the simulated and measured inductor current  $i_L$ , set to follow a 25 A sinusoidal reference waveform  $i_{ref}$  (figures on next page). It can be seen from the figures that the measured and simulated results are similar. Ideally, the average of the inductor current  $i_L$  should follow the 25 A reference signal. This is not the case, though, as both the simulated and measured results depict an offset between the inductor current  $i_L$  and the reference waveform  $i_{ref}$ . Thus, the inner loop controller gives relatively poor results. Further analysis of this problem showed that the offset was caused by taking the samples at the incorrect time.

In terms of Figure 6.12, the inductor current is sampled at  $(T_s - \Delta)$  and not at the mean value of the inductor current  $i_L$ . To measure the mean value of the inductor current  $i_L$  the time delay  $\Delta$  would have to be shifted back considerably. This time increment  $\Delta$  would also not be fixed due to the variation of the duty cycle  $d$ , and the sampling point would thus have to be adjusted every cycle. This method would increase the computational requirements and the system will become unstable if  $\Delta$  increases considerably.

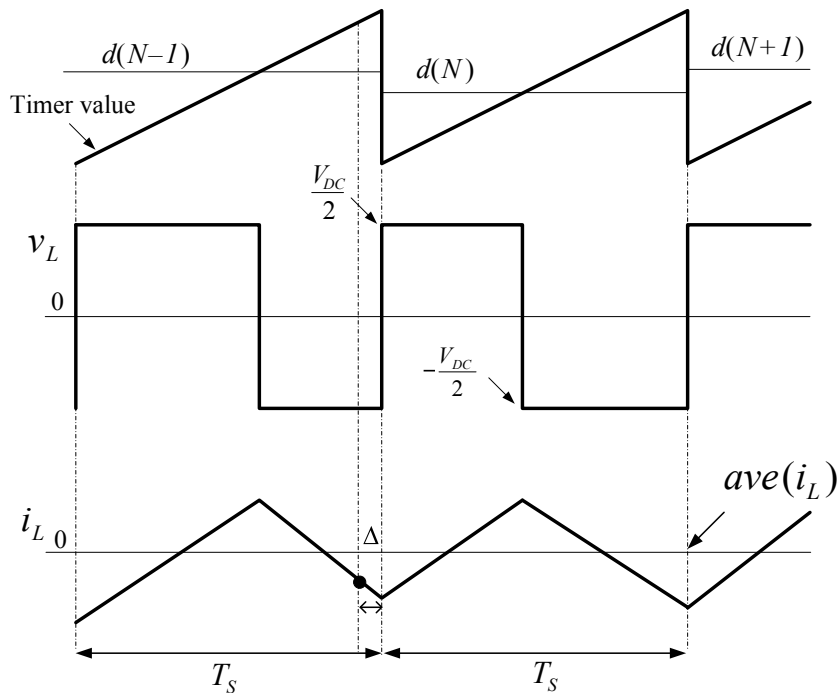


Figure 6.12: DSP implementation of the SEPWM carrier waveform



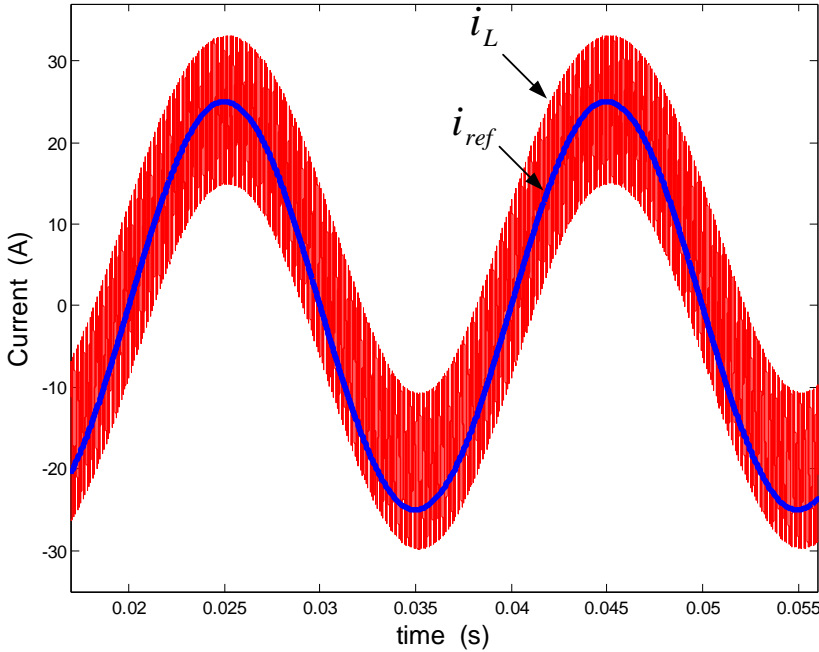


Figure 6.13: Simulated inductor current  $i_L$  using SEPWM

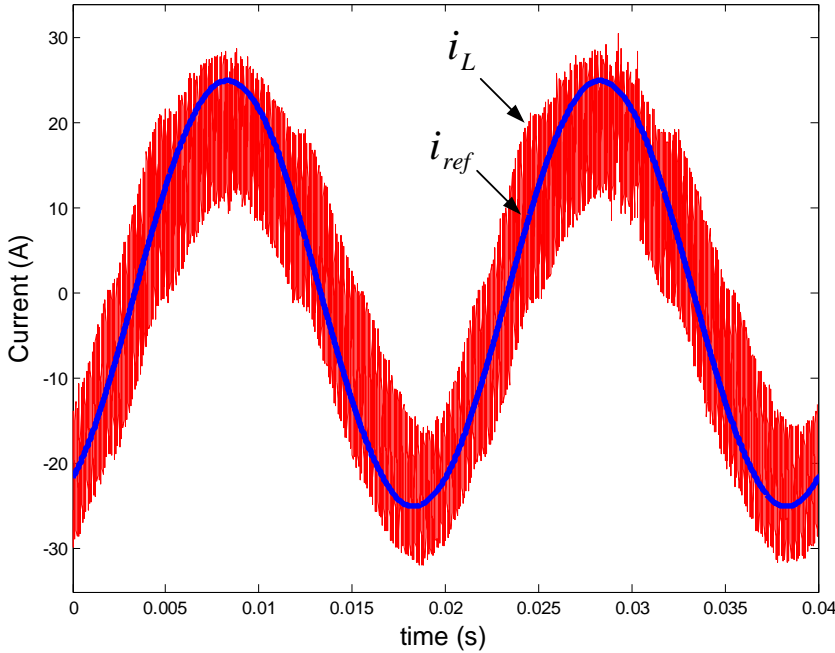


Figure 6.14: Measured inductor current  $i_L$  using SEPWM

The average of the inductor current  $i_L$  can, however, be measured if double edged PWM (DEPWM) is used, in other words if a triangular carrier wave is used. The respective waveforms of DEPWM are shown in Figure 6.15. Sampling the mean value of the inductor current  $i_L$  is achieved by using DEPWM and sampling at  $(\frac{T_s}{2} - \Delta)$ . The duty cycle  $d(N)$  is therefore set at  $\frac{T_s}{2}$ , thus the length of the computational delay  $\Delta$  remains unchanged from that in Figure 6.8. This sampling position is therefore achieved much more simply than the method proposed with SEPWM.

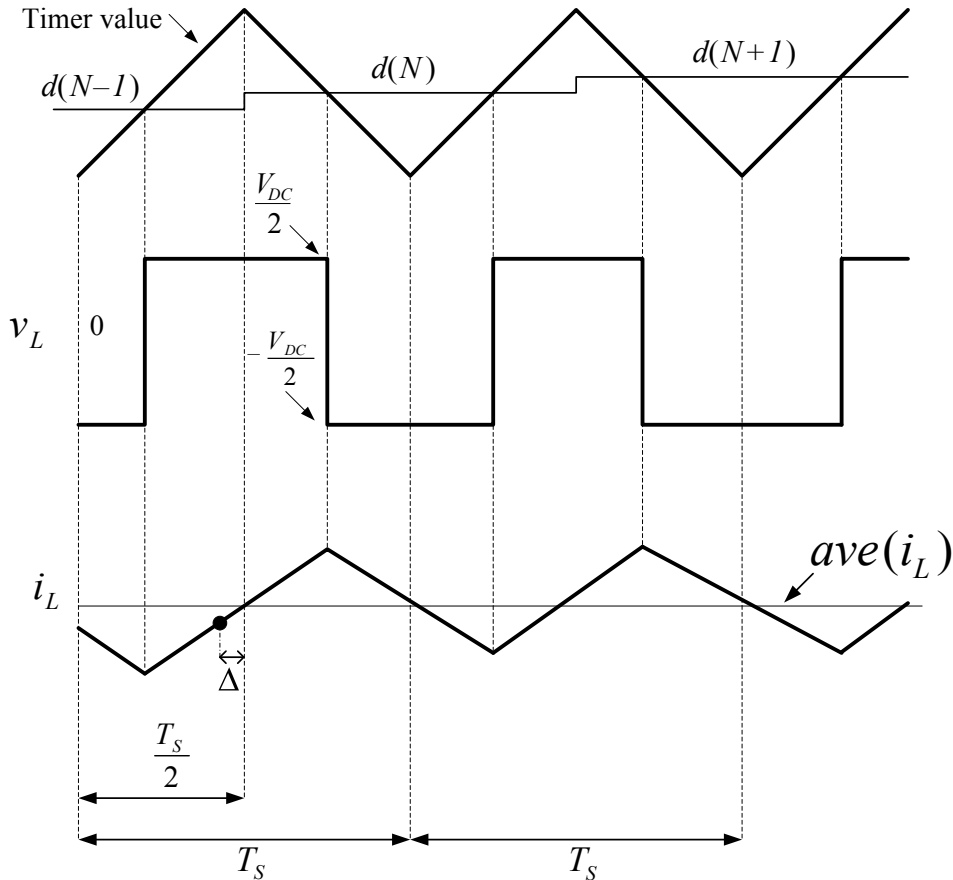


Figure 6.15: Sampling the mean of the inductor current  $i_L$  using DEPWM

Figures 6.16 and 6.17 illustrate the simulated and measured inductor current  $i_L$  by using DEPWM and sampling at  $(\frac{T_s}{2} - \Delta)$ . The results obtained by means of the simulation and the measurements are almost identical. It is shown that the measured inductor current  $i_L$  accurately follows the reference waveform  $i_{ref}$ . Digital average current mode control is therefore achieved using DEPWM and optimally sampling the inductor current.

The effects of the sampling times of SEPWM and DEPWM are shown in Figure 6.18. It can be clearly seen that, unlike the SEPWM carrier, DEPWM samples the mean of the inductor current  $i_L$ .

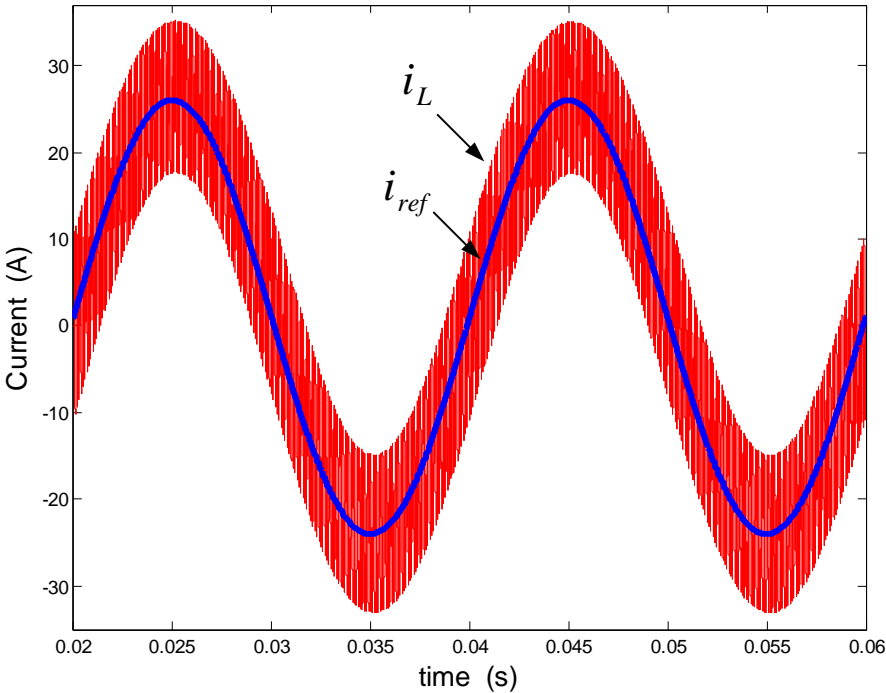


Figure 6.16: Simulated inductor current  $i_L$  using DEPWM

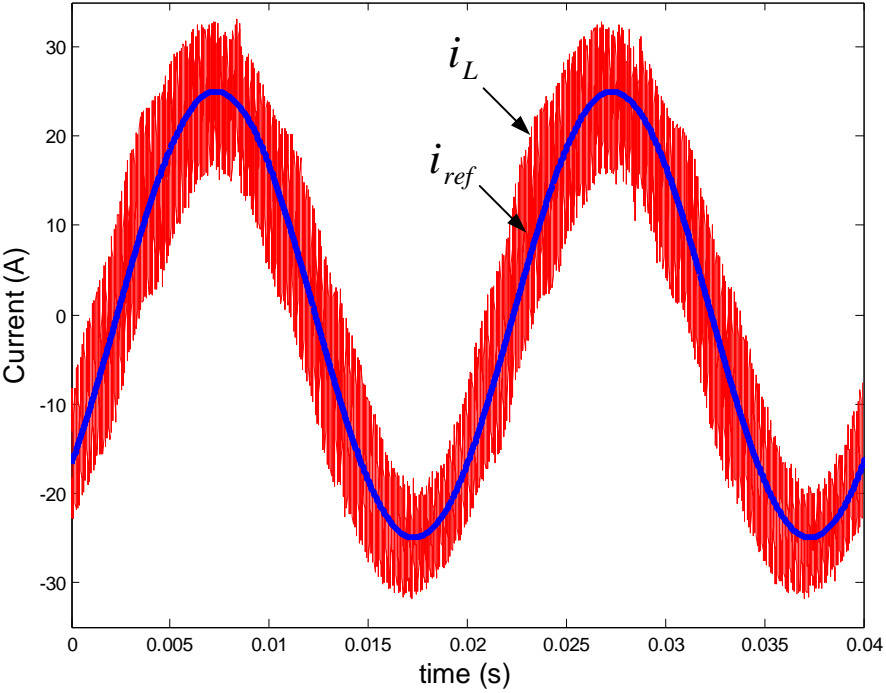


Figure 6.17: Measured inductor current  $i_L$  using DEPWM

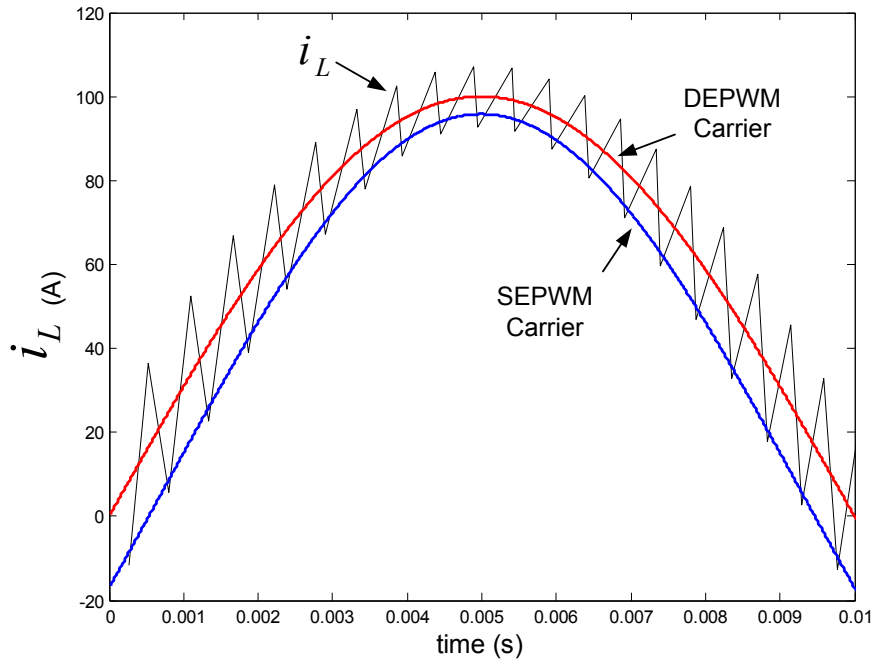


Figure 6.18: Sampling time comparison between SEPWM and DEPWM

Figure 6.19 depicts the inductor current  $i_L$  that is set to follow a 25 A square wave reference. The output voltage  $v_o$  is also shown in the figure. The output voltage  $v_o$  is initially seen to be zero, which was done intentionally by short circuiting the load. The inductor ripple current  $\Delta i_L$  is therefore much larger due to the shorted output voltage  $v_o$ . This measurement confirms that the inner current loop remains stable under large inductor ripple current  $\Delta i_L$  values.

At time  $t \approx 30$  ms, the short circuit is removed from the load by means of a circuit breaker. The circuit breaker removes the short circuit across the load, thus at  $t \approx 30$  ms a resistive load is connected into the circuit. It can clearly be seen that the output voltage  $v_o$  increases as the current is injected into the resistive load. The inductor ripple current  $\Delta i_L$  is also shown to decrease as the load voltage  $v_o$  increases. The amplitude of the ripple current in the steady state is approximated as:

$$\Delta i_{L1} = abs \left( \frac{\frac{V_{DC}}{2} - v_o}{L} \times t_1 \right) \quad (6.11)$$

Referring to Equation 6.11 and assuming that  $t_1$  is constant, it can be seen that at a zero output voltage  $v_o$ , the ripple current will be at its maximum. Thus, as the output voltage  $v_o$  increases the ripple current  $\Delta i_L$  decreases. This explanation is justified by the results in Figure 6.19. It is also noted that, in the steady state, the inductor current  $i_L$  follows the square wave in an acceptable fashion. This measurement was also done using a sinusoidal reference wave, and similar results were obtained.

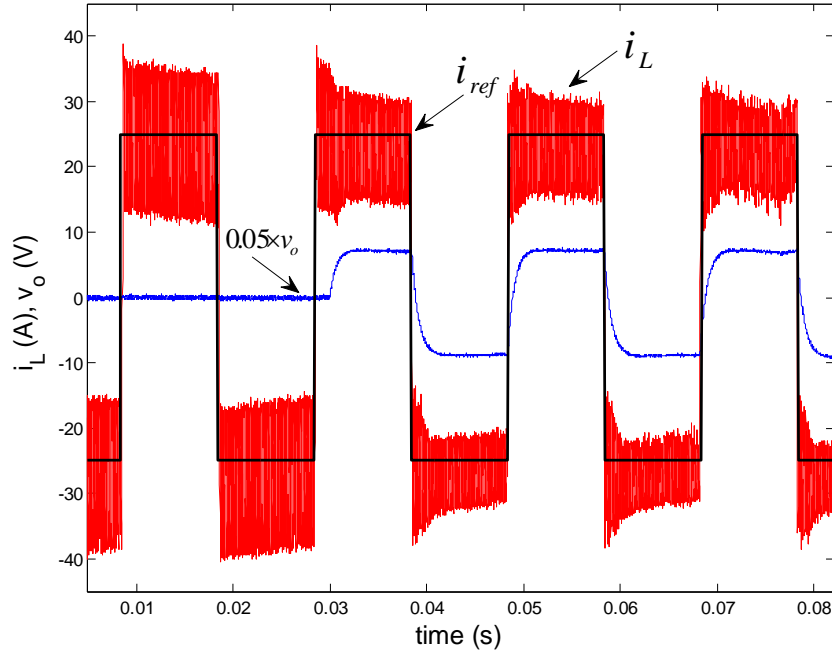


Figure 6.19: Measured step response following a step wave reference

### 6.3.4 Bandwidth

The bandwidth of the current loop is approximated by comparing the step response of Figure 6.19, to a second order linearised transfer function, namely  $M(s)$ . The second order transfer function is obtained by measuring the peak time and overshoot, and by using the following formulas from [55], pages 229-234:

$$M_p = e^{\left(\frac{-\zeta}{\sqrt{1-\zeta^2}}\right)\pi} \quad (6.12)$$

$$t_p = \frac{\pi}{W_d} \quad (6.13)$$

Where  $M_p$  is the percentage overshoot,  $t_p$  the time where the response peaks and  $\zeta$  the damping ratio. The model transfer function  $M(s)$  is shown below:

$$M(s) = \frac{1.309 \times 10^9}{s^2 + 4.993 \times 10^4 s + 1.309 \times 10^9} \quad (6.14)$$

Analysing  $M(s)$ , the 3 dB bandwidth of the system is calculated to be 5 757 Hz, which is roughly 18 times the bandwidth of the outer voltage loop. The bandwidth measurement is dependent on the output voltage  $v_o$  and filter inductance  $L$ , as this determines the rate of current increase  $\frac{di}{dt}$ . Thus the bandwidth stated will differ if the filter inductor is altered. The step response of  $M(s)$  is plotted against the measured step response and the similarities can be seen in Figure 6.20.

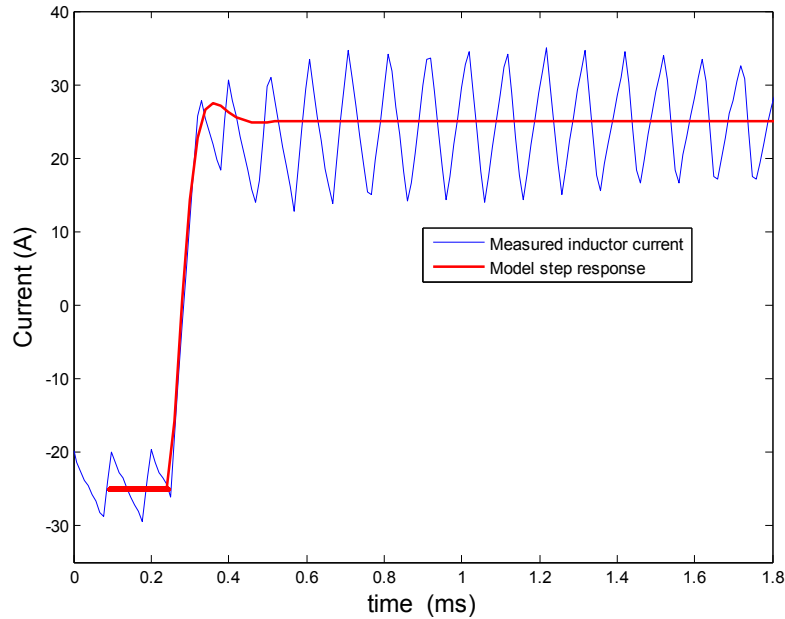


Figure 6.20: Second order model approximation

### 6.3.5 Conclusion of the Inner Current Loop

The control algorithm was successfully implemented in a fixed point DSP, due to the low computational requirements of this algorithm. The results were initially unsatisfactory as result of the poor transient tracking ability. The problem was identified as the use of the incorrect sampling times of the inductor current, which was resolved by using another carrier waveform. A comparison was made between a sawtooth carrier and a triangular carrier. The results showed that the former produced a form of peak current mode control. However, the preferred average mode current control was obtained by using the triangular carrier and optimally setting the sampling time. The inner current loop was fully tested and the relevant measurements were discussed.

## 6.4 Outer Voltage Loop

A suitable outer voltage loop should react quickly to load transients but not to high frequency noise. Thus, the bandwidth of the outer voltage loop is in the order of 300 - 350 Hz. Figure 6.21 depicts the model of the outer voltage loop. A current source is used as input to the outer voltage loop due to the high bandwidth of the inner loop. Consequently, the second order output filter has been split into two single order systems.

The transfer function of the outer voltage loop, namely  $Y(S) = \frac{V_o(S)}{I_{in}(S)}$  is derived using nodal

voltage analysis and given as:

$$Y(s) = \frac{s \left( \frac{r_C R_L}{r_C + R_L} \right) + \frac{R_L}{C[R_L + r_C]}}{s + \frac{1}{C[R_L + r_C]}} \quad (6.15)$$

With  $R_L$  being the load resistance,  $C$  the filter capacitance and  $r_C$  the ESR of the capacitor. The design of the voltage loop is carried out using a  $25 \Omega$  resistive load and a filter capacitor of  $100 \mu\text{F}$ .

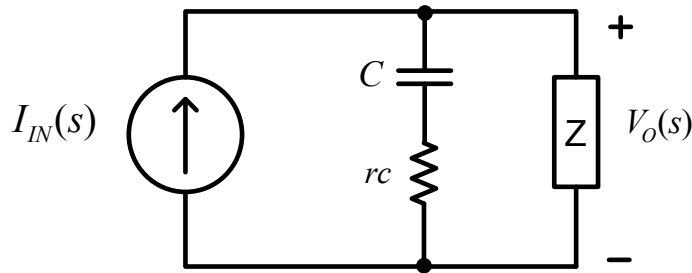


Figure 6.21: Simplified control model

A  $PI$  controller is chosen for the control of the outer voltage loop; these types of controllers are dependent on the load parameters. This means that they are susceptible to unstable operation under major load variations. The  $PI$  controller is therefore designed in such a way that it has a sub-optimal response, although guarantees stability.  $PI$  control is used in this double loop strategy regardless of the disadvantages mentioned, as the emphasis of this control strategy is on the inner loop current controller. A block diagram representation of  $PI(s)$  is shown in Figure 6.22.

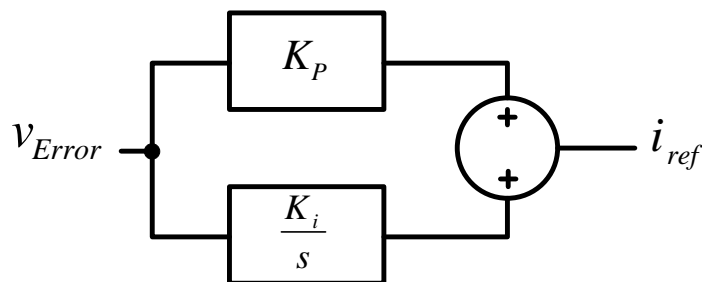


Figure 6.22: PI controller

There are many options of designing the outer voltage loop. For example, the design can be done in the  $s$ -domain and directly placed in the discrete domain by using emulation techniques. However, this method requires the sampling frequency  $f_s$  to be 30 times higher than the bandwidth of the system. Another option is to design the controller in the  $s$ -domain and transform it to the  $z$ -domain using  $z$ -transformations. In this case, the pre-requisite of the former method

regarding the sampling frequency is not met. Thus, the design of the controller is done directly in the  $s$ -domain and transformed to the  $z$ -domain.

The  $PI$  controller in the  $s$ -domain contains a pole at the origin and a zero placed on the real axis at a specific frequency. The controller is therefore designed iteratively in Matlab to obtain an acceptable response. The controller was designed by placing a zero at 4 000 rad/s and a pole at the origin. The  $s$ -domain controller is given as:

$$PI(s) = \frac{k(s + 4000)}{s} \quad (6.16)$$

The dampening  $\zeta$  and the natural frequency  $w_n$  of the system are increased as the gain  $k$  is increased. The gain is therefore set to have an improved dampening  $\zeta$ , but the natural frequency  $w_n$  should not exceed  $2\pi 500$  rad/s. At a gain  $k = 0.2$ , a dampening  $\zeta = 0.42$  is obtained and the natural frequency  $w_n$  of the system is equal to 2 800 rad/s. The root locus of  $PI(s)Y(s)$  is shown in Figure 6.23

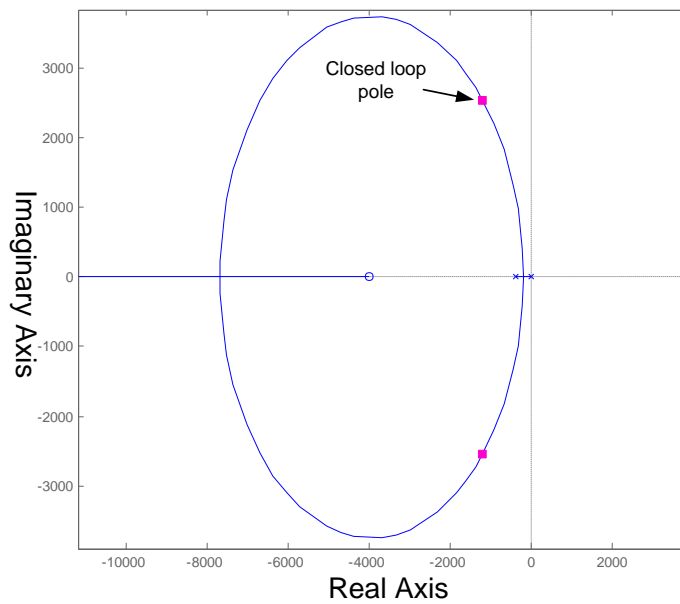


Figure 6.23: Root locus of  $PI(s)Y(s)$

Mapping the controller to the  $z$ -domain by using a zero order hold transform,  $PI(z)$  is given as:

$$PI(z) = \frac{0.2z - 0.12}{z - 1} \quad (6.17)$$

This controller  $PI(z)$  is directly implemented into the discrete domain by using first principles. The controller is therefore defined as  $PI(k)$ . The gain  $k$  of the controller was furthermore tweaked to obtain an optimum response. The next section discusses the results of the outer voltage loop.



### 6.4.1 Outer Voltage Loop Results

The double loop control strategy is tested in this section with the main emphasis being on the outer voltage loop. The design of the outer loop controller is based on a resistive load  $R_L$ , hence the tests that follow are done with a resistive load. The controller is not optimally designed for connecting another load to the system, for example an RL load. The load dependence on the PI controller is therefore a major disadvantage. A resistive load is therefore used to illustrate the concept of the double loop strategy. The measurements of the double loop controller are discussed in the following section.

#### Transient Response of the Double Loop Controller

The double loop control strategy was tested by applying load steps to the system in order to analyze the transient responses. This was done by means of a circuit breaker that connects an extra load into the circuit. A base case was formed to compare the open loop and closed loop responses, thus the system parameters were kept constant for both tests.

The step responses of both the closed and open loop systems are shown in Figures 6.24 and 6.25. The output voltage  $v_o$  of the open loop system, is shown to have an underdamped response as the load step is introduced. The closed loop system, however, reacts much faster and no oscillations are present on the output voltage. These measurements show that the transient response of the closed system is far superior to that of the open loop system.

#### Spectral Analysis

A spectral analysis is done on the output voltage  $v_o$  of both the open loop as well as the closed loop systems. This is done to see whether the voltages fall within the specifications of the South African standards (NRS-048). The NRS-048 specifies that the THD should be below 8% up to and including the 40<sup>th</sup> harmonic. The FFT of each output voltage  $v_o$  was obtained with the inherent function of the oscilloscope. The open loop output voltage  $v_o$  is the voltage that is generated using sinusoidal modulation, at a modulation index  $m_a = 0.8$ . The carrier method used was SEPWM.

The output voltage spectra of the open and closed loop systems are shown in Figures 6.26 and 6.27 respectively. As expected, the spectrum of the open loop system depicts large odd harmonics. The spectrum of the closed loop output voltage  $v_o$  depicts a 12 dB improvement in the third harmonic. The 5<sup>th</sup>, 7<sup>th</sup>, 9<sup>th</sup> and 11<sup>th</sup> harmonics are also improved with regard to the open loop system. A degradation in the second harmonic is seen in the closed loop system, but this harmonic is -37 dB smaller than the fundamental. The second harmonic is not noted on  $v_o$  in Figure 6.25, due to the gain of -37 dB.

The THD of the output voltage was calculated by taking into account the first 10 harmonics as well as the harmonics at the switching frequency  $f_s$ . The THD of the closed loop system was in fact worse than that of the open loop system, although it was still within the specifications of the NRS 048-2:2004. This deteriorated THD of the closed loop voltage can be attributed to the large second harmonic present in the spectrum. The accuracy of the THD calculation on

the scope is limited, thus to improve the accuracy of the THD calculation a spectral analyser should be used.

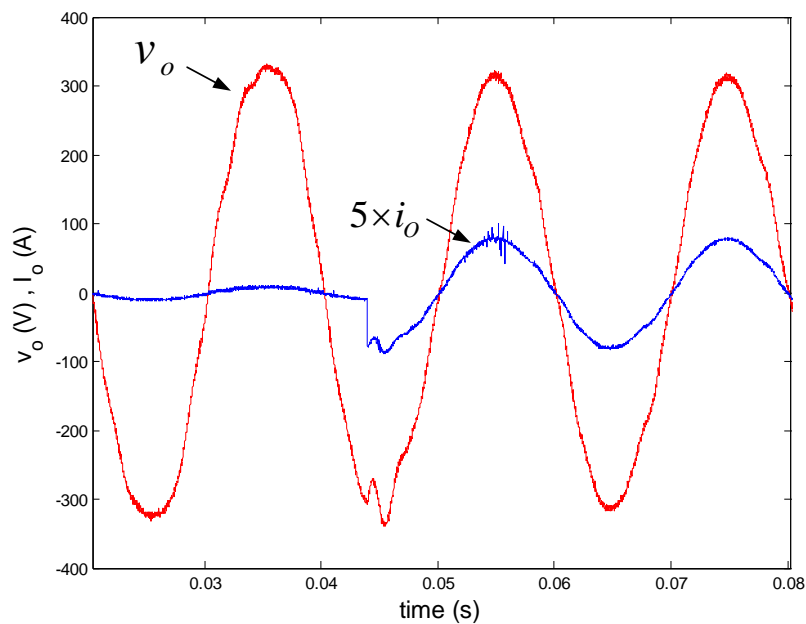


Figure 6.24: Open loop response under a load step condition

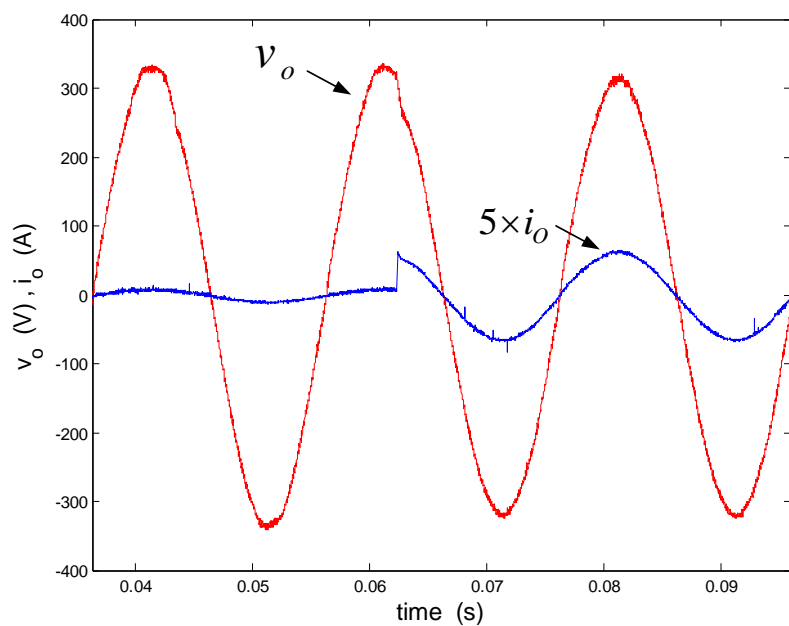


Figure 6.25: Closed loop response under a load step condition

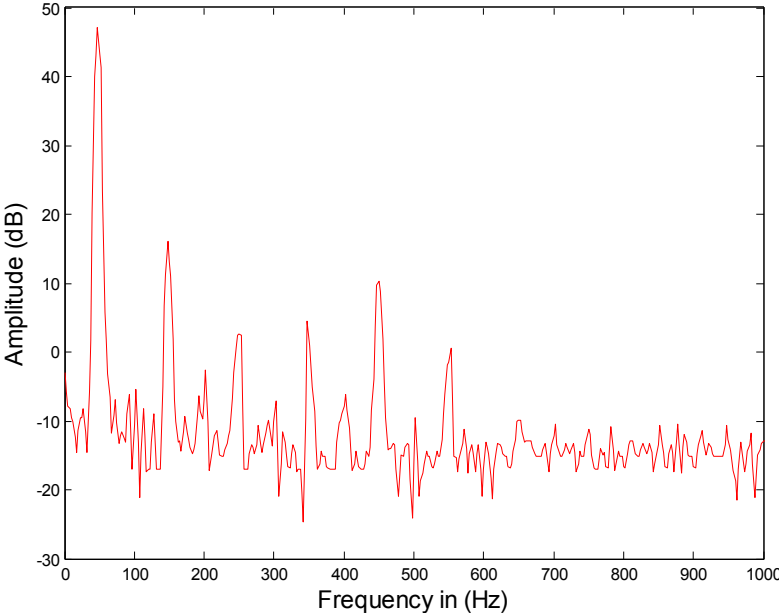


Figure 6.26: Open loop voltage spectra. THD = 3.39%

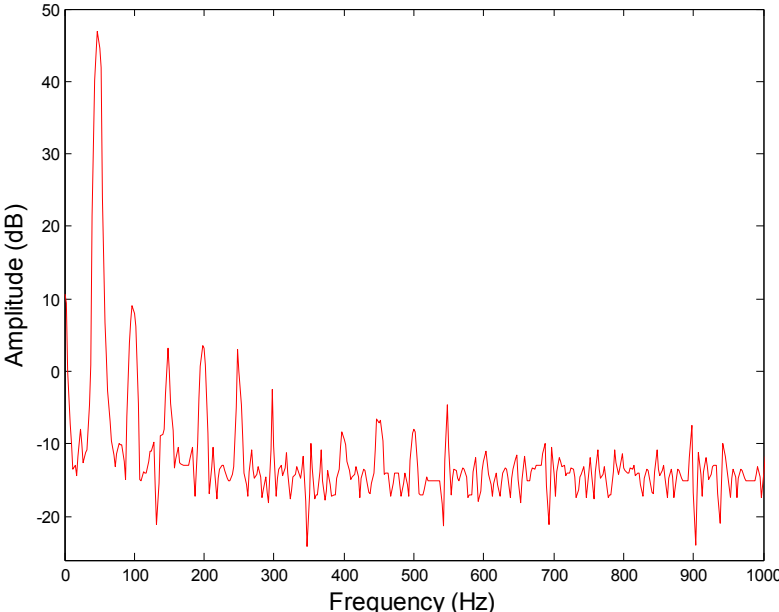


Figure 6.27: Closed loop voltage spectra. THD = 3.47%

### 6.4.2 Outer Voltage loop Conclusion

The outer voltage loop was designed using a conventional PI controller. The transient response of the double loop control system was tested under load step conditions. This was done to clarify whether the double loop strategy improves the transient response of the system. These transient responses were compared to the open loop response and acceptable results were obtained.

The THD of the steady state output voltage was found to be within the specifications of the NRS-048. Unlike the open loop system, the closed loop output voltage manifested even harmonics on the frequency spectrum. Thus, the positive and negative waveforms depicted a form of asymmetry. A slight DC offset is also present in the output voltage. This led to the conclusion that the integrator in the PI controller did not eliminate the steady state error in the voltage loop. Further investigation is therefore proposed to improve the THD of the output voltage.

## 6.5 Conclusion

The relevant research regarding predictive control strategies was briefly discussed and a double loop controller was chosen. The inner loop control method discussed in this chapter is based on an existing control technique used in a full bridge converter. This method was extended to a half bridge converter and evaluated in the laboratory. An investigation was done with regard to different carrier waveforms and the effect thereof on the system response. The outer voltage loop was implemented by means of a PI control strategy and the results of the double loop control technique were discussed. The findings of this chapter were published in [53].

# Chapter 7

## Experimental System Analysis

The practical results obtained in this thesis are discussed in this chapter, ranging from the three phase DC-AC inverter to the back-to-back converter in the modular cell. The results of the three phase inverter are only briefly discussed in this chapter, as they are discussed in detail in previous chapters.

The main emphasis of this chapter is on the operation of the high voltage DC-DC converter, which is described in, Chapters 3 and 4. The converter is fully tested and the problems occurring in the modular cell are discussed. The concept of the series stacked SST is partially tested in this chapter by connecting two of the cells in series and their outputs in parallel. The voltage balancing occurring on the primary of the converter is also investigated.

### 7.1 Three Phase Inverter

This section briefly explains the results obtained with regard to the output stage of the SST. A loss analysis was done with regard to the components in the inverter using two different methods. These methods are briefly described and compared. The control algorithms developed in Chapter 6 are discussed and the results of the double loop control strategy are highlighted.

#### 7.1.1 Loss Analysis of the Switching Devices in the Inverter

Chapter 5 presented an in-depth analysis of the switching device losses present in a half bridge inverter. This analysis was based on the comparison between existing analytical methods and the presented numerical method. The analytical methods focus on calculating the average current flowing through the semiconductors, which is why the inductor ripple current is ignored. This method calculates the switching and conduction losses using an averaging technique [8]. The numerical method calculates the exact current waveforms flowing through the individual components and then averages them. The benefit of the numerical method is that the inductor ripple current is taken into account.

These current waveforms are obtained by using an existing inductor current model [48]. The amplitudes of the inductor current  $i_L$  are obtained by inserting the intersection times into the inductor current model. These intersections times occur between the carrier waveform  $c(t)$  and

the reference waveform  $m(t)$  [49]. This method therefore calculates the switching and conduction losses by using the exact current amplitudes.

These two methods were used to calculate the switching and conduction losses occurring in a single phase inverter. The purpose of this was to facilitate a comparison between the two methods as the inductor ripple current increased. The difference between these two methods with regard to the conduction losses was negligible. The switching losses, however, resulted in different results between the two methods. The switching losses were shown to increase linearly with regard to an increase in the inductor ripple current. The analytical methods were calculated using two modulation techniques, namely SEPWM and DEPWM, and identical results were obtained between the carrier waveforms. A comparison of these methods was published in [45].

### 7.1.2 Inverter Control Algorithms

Multiple control strategies were considered for the control of the three phase half bridge inverter. This topology simplifies the control by means of an available neutral point between the bus capacitors. The required control algorithms are identical for all three phases, although the reference signals are phase shifted by  $120^\circ$ . A double loop control strategy is chosen for the three phase half bridge inverter; in other words there is an inner current loop and an outer voltage loop. The successful operation of the double loop control strategy is dependent on the bandwidth of the inner current loop. The greater the bandwidth of the inner loop, the faster the reaction time of the outer voltage loop.

Possible methods of controlling the inner current loop were considered, namely proportional control, predictive control and state space control. The computational requirements of each method differ, and the decision to use the control method was dependent on the digital controller. The digital controller available was a 32 bit fixed point DSP. The computational ability of this controller is far inferior to an FPGA, but the software implementation of the control algorithms is simpler than that on an FPGA. Predictive control of the inner current loop is chosen for the inner current loop. The control method used in the half bridge inverter is based on the research of superposition of the inductor current obtained in [35]. This method was implemented in a full bridge inverter using unipolar switching. This method was therefore extended to a half bridge inverter based on the same principle. The extension of this method was published in [53].

The control algorithm of the inner current loop resulted in:

$$D = \left( \Delta i_L \times \frac{L}{V_{DC} \cdot T_S} \right) + \frac{1}{2} + \frac{v_o}{V_{DC}} \quad (7.1)$$

This equation and the derivation thereof is discussed in Chapter 6. The control algorithm was successfully implemented in the fixed point DSP due to the low computational requirements of this algorithm. The computational time required for the algorithm was reduced to  $3.4 \mu s$  by using 32-bit integers, as opposed to floating point variables. The low computational time of this control method was therefore highlighted. The duty cycle result obtained in Equation 7.1 is compared to a carrier waveform to obtain the switching signals for the IGBTs. The comparison between a sawtooth carrier and triangular carrier was investigated. The results showed that

the sawtooth carrier produced peak current mode control. The preferred average mode current control was obtained by using the triangular carrier and setting the sampling time optimally. The inner current loop was fully tested and acceptable results were obtained. The inner current loop obtained a bandwidth of 5.7 kHz, which is sufficient for the outer voltage loop.

The purpose of the outer voltage loop is to provide a reference for the inner current loop. The outer voltage loop is designed using a conventional PI controller. The transient response of the double loop control system was tested under load step conditions. This was done to clarify that the double loop strategy improves the transient response of the system. These transient responses were compared to the open loop response and acceptable results were obtained.

The THD of the steady state output voltage was found to be within the specifications of the NRS-048. In contrast with the open loop system, the closed loop output voltage depicted even harmonics on the frequency spectrum. Thus, the positive and negative waveforms have a form of asymmetry. The second harmonic was however -37 dB smaller than the fundamental. A slight DC offset is also present in the output voltage. This led to the conclusion that the integrator in the PI controller did not eliminate the steady state error in the voltage loop. Further investigation is therefore proposed to improve the THD of the output voltage.

## 7.2 High Voltage Source for the DC-DC Converter

The DC-DC converter is tested with the high voltage (HV) source shown in Figure 7.1. A three phase variable AC source ranging from 0 to 400 V is used on the primary of the step-up transformer. Variable tap settings are available on the primary of the transformer in order to alter the turns ratio. The primary of the transformer is connected in delta, giving rise to three phase operation on the low voltage (LV) side. The secondary of the transformer however utilizes 6 phases, these additional phases are obtained by phase shifting the respective primary waveforms.

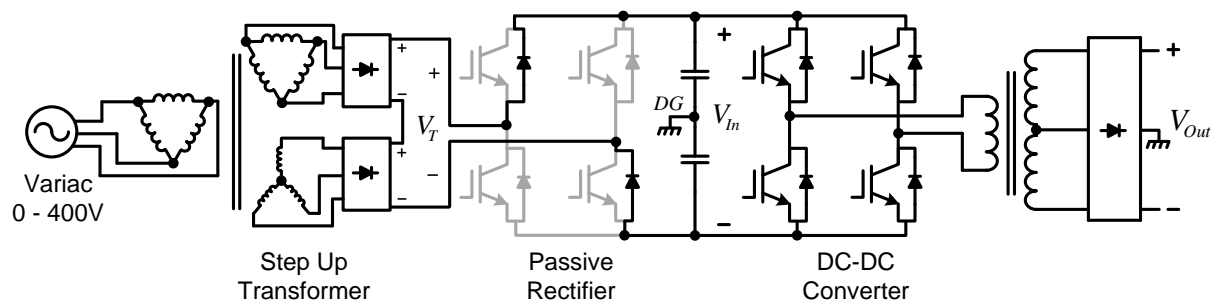


Figure 7.1: The schematic of the system setup

The 6 phases on the HV side are separated into two 3 phase connections; the phases of the secondary are connected in delta and star respectively. The output of each delta and star connected secondary is fed into a six pulse passive rectifier. A series connection is formed between the two rectifiers to increase the output DC voltage. This DC voltage is stabilized with a 4700  $\mu\text{F}$  capacitor bank. The amount of energy stored in these capacitors is proportional to

the voltage squared; this energy is therefore substantial due to the high bus voltage. In the event of a short circuit occurring in the cell, the energy stored in the bus capacitors would discharge into the cell and cause further damage. To prevent this, a custom built DC fuse is connected in series with the cell input. The connection of the fuse is shown in Figure 7.2.

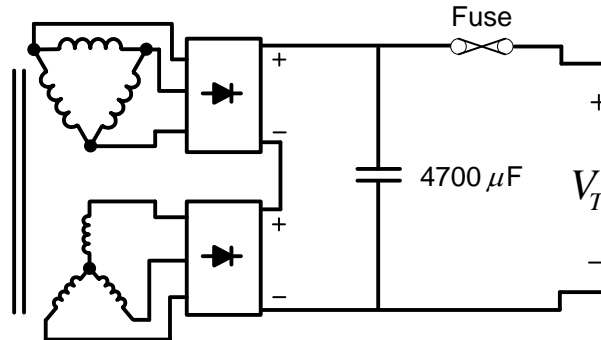


Figure 7.2: High voltage source

The high voltage source with an output voltage  $V_T$ , ranges from 0 to 3.3 kV, depending on the tap settings of the primary. This voltage  $V_T$  is connected between the IGBTs of the active rectifier. The IGBTs of the active rectifier are disabled, and the converter therefore acts as a passive full bridge rectifier. Figure 7.1 shows that only two diodes conduct the current due to the DC input voltage.

The ground connection between the bus capacitors namely  $DG$  is connected to the earth connection of the LV supply; this can be done as the primary and secondary of the step-up transformer are galvanically isolated. The full bridge rectifier on the secondary of the high frequency transformer has three connections, namely  $\frac{V_{Out}}{2}$ ,  $-\frac{V_{Out}}{2}$  and a ground connection. This ground connection is also connected to the earth of the LV supply. The  $DG$  between the bus capacitors of the full bridge converter is therefore the same as the ground on the output of the rectifier. These additional grounds are connected to the earth of the LV supply to prevent floating potentials.

### 7.3 Evaluation of the DC-DC Converter

The initial testing of the DC-DC converter was done at relatively low voltages to test the general operation of the converter. These voltages were systematically increased until the rated value of the converter was achieved. The DC-DC converter was successfully tested up to a bus voltage  $V_{In}$  of 1.3 kV. However, as the load was increased the IGBTs failed irregularly. The IGBTs started to fail as the collector current was increased above 3 A, even though this current was far below the rated current of the IGBTs. The continuous collector current of the chosen IGBT is rated at 16 A and the maximum blocking voltage is given as 1 700 V. IGBT failure in general is caused by over voltages or when the maximum junction temperature  $T_{J(max)}$  is exceeded. The probable causes of the IGBT failure in the DC-DC converter are discussed in the sections that follow.



## 7.4 Voltage Overshoot

Voltage overshoot usually occurs when the IGBT is turned off and is a strong function of the stray inductances  $L_s$  of the circuit. The change in collector current  $\frac{di_c}{dt}$  also influences the voltage overshoot. The amplitude of the collector emitter voltage  $v_{CE}$  occurring across an IGBT as the device is switched off is given as [8]:

$$v_{CE} = V_{In} + L_s \frac{di_c}{dt} \quad (7.2)$$

The voltage that the IGBT is required to block therefore increases as the stray inductance  $L_s$  increases. The fall time  $dt$  is also inversely proportional to the overshoot voltage  $v_{CE}$ . Reduction of the overshoot voltage is therefore obtained by improving the circuit layout which reduces the stray inductance  $L_s$ . The turn-off times of the IGBT can also be increased, although this increases the switching losses.

The overshoot occurring across the IGBTs is therefore analysed using Equation 7.2, hence the current amplitudes at which these devices turn-off are required. The current amplitude that is interrupted by the left leg switches is greater than that of the right leg switches. The amplitude of the current that is interrupted by  $S_1$  in the left leg is defined as  $i_{(3initial)}$ . The left and right leg switches of the full bridge are shown in Figure 7.3. Refer to Section 4.1.3, in Chapter 4 for further information regarding these amplitudes.

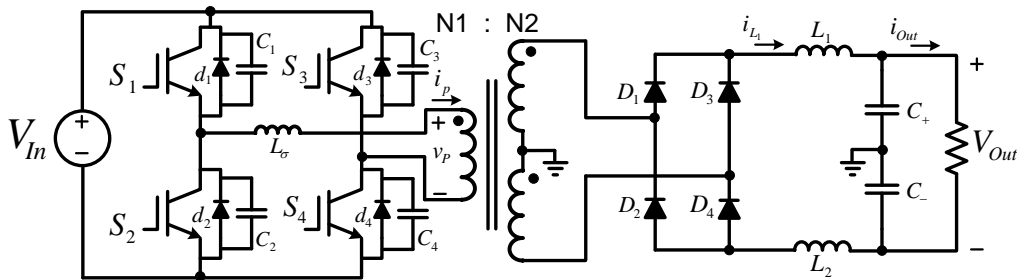


Figure 7.3: DC-DC converter schematic

The voltage overshoot across all the IGBTs was measured, and it was found that the maximum overshoot occurs across  $S_1$  and  $S_2$ . This is justified by Equation 7.2, as the initial current is greater in the left leg IGBTs. Thus, the left leg IGBTs  $S_1$  and  $S_2$  are most likely to fail due to voltage overshoot. Consequently, the voltage overshoot analysis that follows is based on IGBT  $S_1$ .

Figure 7.4 depicts the overshoot occurring across  $S_1$  at a bus voltage  $V_{In}$  equal to 1 000 V. The overshoot across IGBT  $S_1$  is measured as 115 V, which is an overshoot of 11% . It is clearly seen that the overvoltage occurs on the turn-off transient. The overshoot measurements in this section are measured with a differential probe directly on the terminals of the IGBT. The measurement shown in Figure 7.4 is unfiltered, but the overshoot measurements that follow in this section are digitally filtered to reduce the amount of noise on the measurement. Thus,

a comparison can be made between this figure and the figures that follow with respect to the filtered measurements. These measurements are filtered to improve the clarity of the result.

According to Equation 7.2, the overshoot voltage is therefore reduced by one of two methods: In the first method, it is reduced by increasing the fall time  $t_f$  of the IGBT. In the second method the stray inductance  $L_s$  of the circuit is reduced. The latter method would furthermore require the PCB to be rerouted, and the certainty of the overshoot improvement is not guaranteed. The fall time  $t_f$  of the IGBT can be altered, however, by adjusting the gate resistors, which is discussed in the next section.

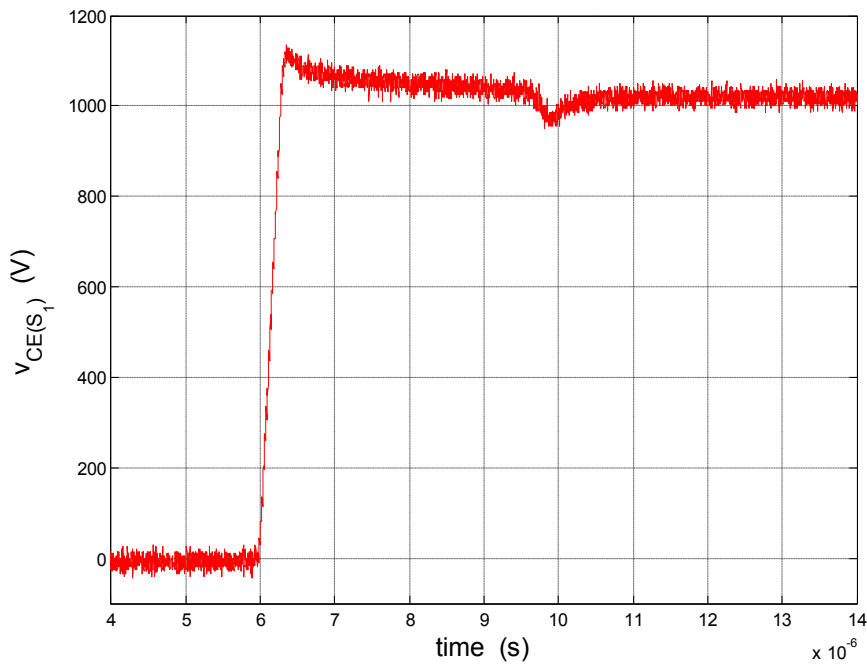


Figure 7.4: Voltage overshoot across IGBT  $S_1$

### 7.4.1 Gate Resistor Optimization

The switching times of the IGBTs are altered by changing the size of the gate resistors. The gate driver circuit either charges or discharges the gate capacitance  $c_{GE}$  through a gate resistor  $r_{gate}$ . This forms a first order RC circuit, thus the switching times are increased by increasing gate resistance  $r_{gate}$ . Referring to Equation 7.2, the voltage overshoot is reduced by increasing the fall time  $t_f$ . The overshoot is therefore analysed as the switching times are altered.

The gate resistances were altered and the overshoot results are shown in Figure 7.5. The parameters of the DC-DC converter were kept constant for this measurement, in order to create a base case to enable a comparison of the results. The bus voltage was set to  $V_{In} = 800 \text{ V}$ , and the load current was also kept constant at  $I_{Out} = 3 \text{ A}$ . The gate resistors were altered from  $22 \Omega$  to  $47 \Omega$ .

Figure 7.5 shows that the difference in overshoot is negligible as the gate resistances are changed. The zoomed-in overshoot voltages are also shown at the peak of the overshoot. These amplitudes concur with Equation 7.2, as the fall times  $t_f$  are increased. The difference in overshoot is roughly 10 V as the gate resistors are altered.

Due to the small change in voltage overshoot as the fall time  $t_f$  is altered, the assumption is made that stray inductance  $L_s$  in the circuit is relatively small. This assumption can be justified, because the length of the tracks between the IGBTs in either leg of the full bridge and the snubber capacitors is less than 10 cm. The width of the tracks between IGBTs is also routed as thick as possible to reduce the stray inductance  $L_s$ . Thus if the stray inductance  $L_s$  is relatively small, the voltage overshoot should be negligible according to Equation 7.2. This is not the case, though, as the voltage overshoot is still present.

It can therefore be observed that the voltage overshoot is not greatly dependent on the stray inductance of the circuit. The gate resistances  $r_{gate}$  are therefore set to  $33 \Omega$ , as the variation of resistance did not reduce the voltage overshoot sufficiently.

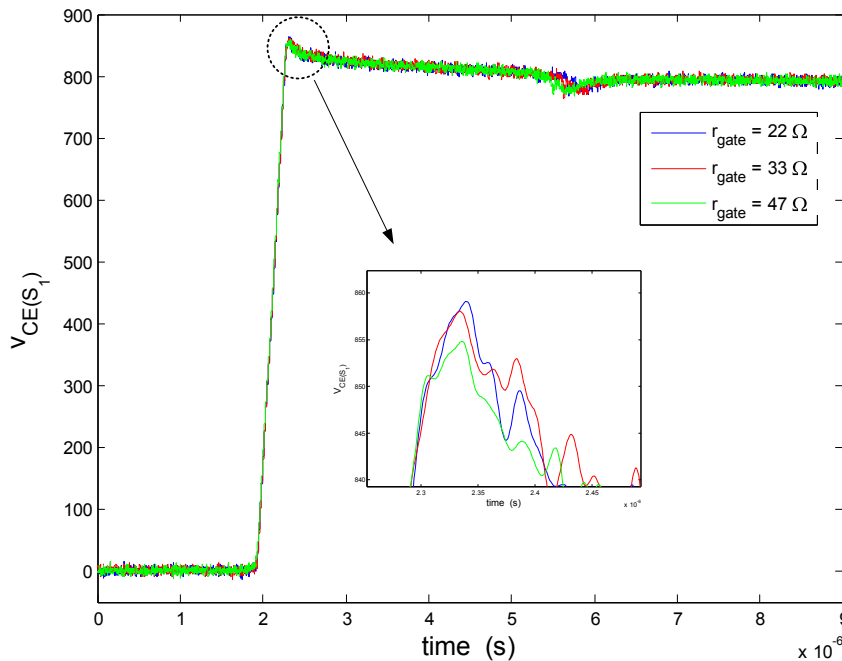


Figure 7.5: Overshoot voltage of IGBT  $S_1$  as the  $r_{gate}$  is altered

### 7.4.2 Voltage Overshoot: Further Investigation

In view of the findings above, further investigation was done with regard to the overshoot of the IGBTs. The overshoot voltage was measured as the bus voltage  $V_{In}$  and the current interrupted by  $S_1$ , namely  $i_{(3initial)}$ , was altered. This is seen in Figure 7.6. The results show that the overshoot is strongly dependent on the current  $i_{(3initial)}$ , and that the larger this current is

the larger is the overshoot voltage. The amplitude of the overshoot voltage also increases as the bus voltage increases. The circuit is therefore analysed in detail at the instant when the overshoot occurs, namely in zones 2-4. The following section is a brief summary of Section 4.1.4, in Chapter 4.

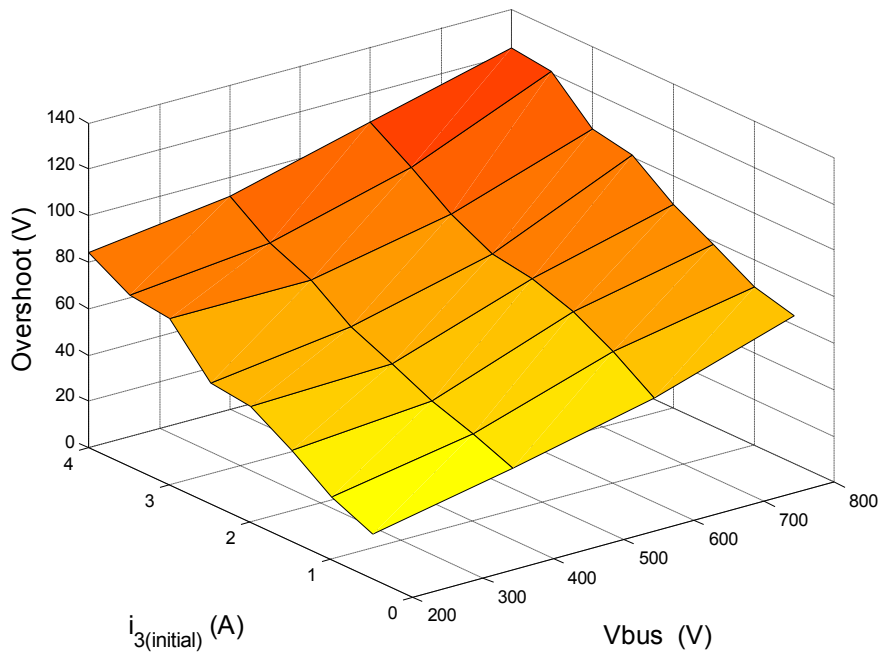


Figure 7.6: Overshoot voltage of  $S_1$  under variation of the system parameters

### 7.4.3 Brief Overview of Zones 2-4

The direction of the primary current  $i_p$  in Zone 2 is shown in Figure 7.7; here, the current conducts through  $S_1$  and  $S_2$ , which is defined as the power transfer stage. Zone 3 is depicted in Figure 7.8; this zone is initialized by IGBT  $S_1$  switching off. The primary current  $i_p$  remains flowing in the positive direction due to the remaining energy left in the leakage inductance  $L_\sigma$ . This current flow therefore discharges capacitor  $c_2$  and charges  $c_1$ , with the voltage across  $c_1$  being equivalent to the  $v_{CE}$  voltage of IGBT  $S_1$ . The voltage overshoot of  $S_1$  therefore occurs at the end of this zone.

Zone 4 is defined as the freewheeling period where the primary current  $i_p$  flows through diode  $d_2$  and IGBT  $S_4$ . This zone is initialized as soon as capacitor  $c_2$  is discharged below the forward voltage of the freewheeling diode  $d_2$ . The primary current  $i_p$  is therefore forced to conduct through diode  $d_2$ .

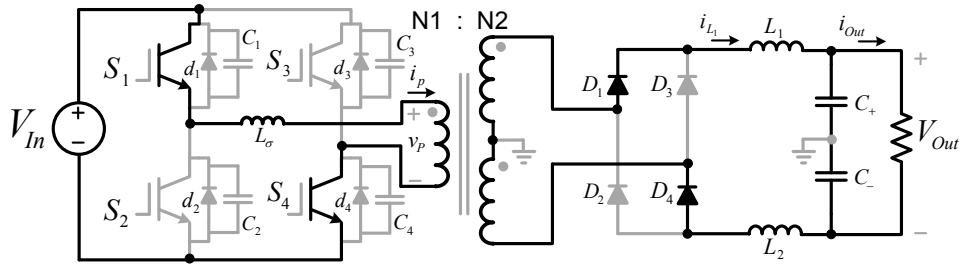


Figure 7.7: Primary current  $i_p$  direction of Zone 2

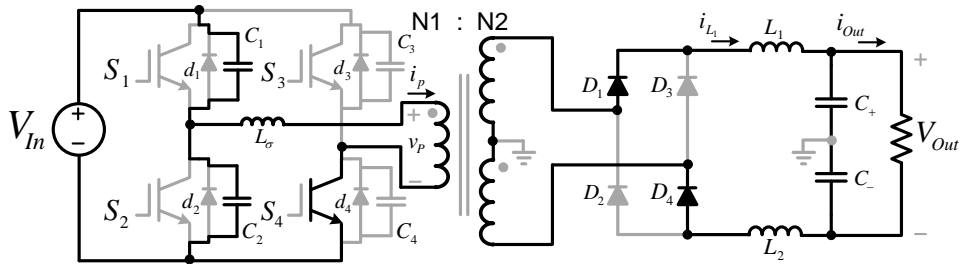


Figure 7.8: Primary current  $i_p$  direction of Zone 3

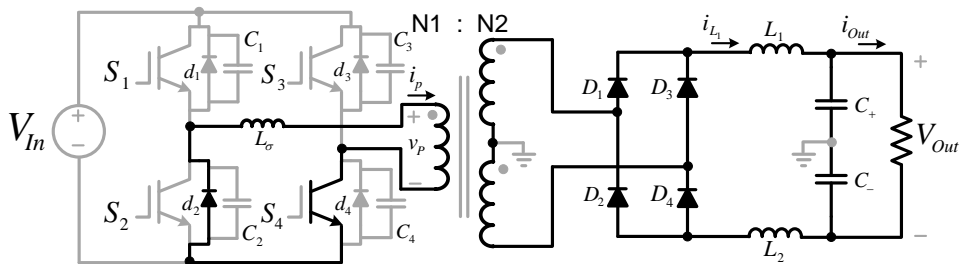


Figure 7.9: Primary current  $i_p$  direction of Zone 4

#### 7.4.4 Diode Forward Recovery in Power Diodes

Analysis of the system waveforms reveals that the voltage overshoot across IGBT  $S_1$  occurs as diode  $d_2$  turns on [7]. Modern day power diodes rarely have forward recovery losses, so this occurrence is therefore unexpected. This section briefly explains the forward recovery occurring in power diodes and this information is utilized in the specific analysis of  $d_2$  in Figure 7.9.

The turn-on transient of a power diode is shown in Figure 7.10; here the forward current is defined as  $i_d$  and the diode voltage as  $v_d$ . It is seen that the forward voltage of the diode has a large overshoot, as the device turns on, namely  $v_{dp}$ . The waveforms are split up into two time segments, namely  $t_1$  and  $t_2$ . During time interval  $t_1$ , the space charge stored in the depletion region, which is caused by the high reverse voltage  $V_R$ , is discharged by the growth of the forward current  $i_d$ . Thus a large voltage drop occurs across the drift region as the forward current grows. The stray inductances present in the circuit also add to this voltage drop if large  $\frac{di_F}{dt}$  values are applied to the device. This time interval  $t_1$  is in the order of hundreds of nanoseconds for high voltage diodes.

As the second interval  $t_2$  commences, the excess carrier distribution grows towards the steady state value of the diode. The forward voltage of the diode starts to become smaller as the forward current  $i_d$  eventually stabilizes. The nominal on state voltage  $v_{f(diode)}$  is reached as interval  $t_2$  is completed. The time interval  $t_2$  is in the order of microseconds in high voltage power diodes.

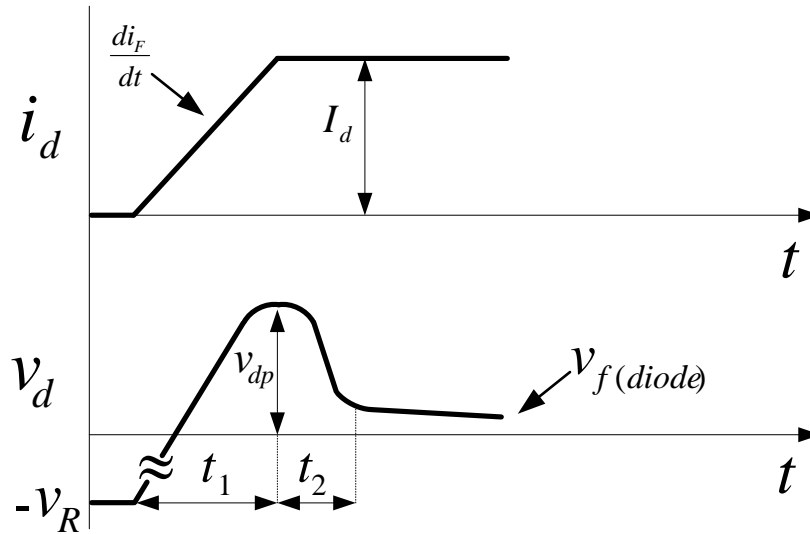


Figure 7.10: Diode forward recovery taken from [11]

The space charge is discharged more rapidly as the value of  $\frac{di_F}{dt}$  increases, but a large value of  $I_d$  increases the time interval of  $t_2$ . Simply put, the forward recovery of the diode is dependent on the forward current  $I_d$  flowing through the diode. This information regarding the diode turn-on transition is obtained in [11].

### 7.4.5 Diode Forward Recovery Occurring in the Full Bridge

The forward recovery of diode  $d_2$  in zone 4, is therefore responsible for the voltage overshoot across IGBT  $S_1$ . This is justified by the measurement shown in Figure 7.11, in which the measured voltages of both  $S_1$  and  $S_2$  are shown and defined as  $v_{M_1}$  and  $v_{M_2}$  respectively.

It can be seen in Figure 7.11 that the voltage across  $S_2$  is negative as the overshoot occurs across  $S_1$ . This suggests that the forward recovery occurring in diode  $d_2$  causes a large forward voltage to occur across the device, hence the voltage across  $S_2$ , namely  $v_{M_2}$  is negative. Using a Kirchoffs voltage loop it can be shown that the voltage across  $S_1$ , namely  $v_{M_1}$  is given as:

$$v_{M_1} = V_{In} - v_{M_2} \quad (7.3)$$

At the beginning of zone 4, the voltage  $v_{M_2}$  is equal to the forward voltage of diode  $d_2$ , namely  $v_{d_2}$ . The polarity of the diode voltage  $v_{d_2}$  is however reversed with respect to  $v_{M_2}$ , hence:

$$v_{M_1} = V_{In} + v_{d_2} \quad (7.4)$$

Equation 7.4 shows that the blocking voltage of  $S_1$ , namely  $v_{M_1}$ , is a function of the forward overshoot voltage of diode  $d_2$ . The required blocking voltage of  $S_1$  is therefore increased due to the forward recovery of diode  $d_2$ .

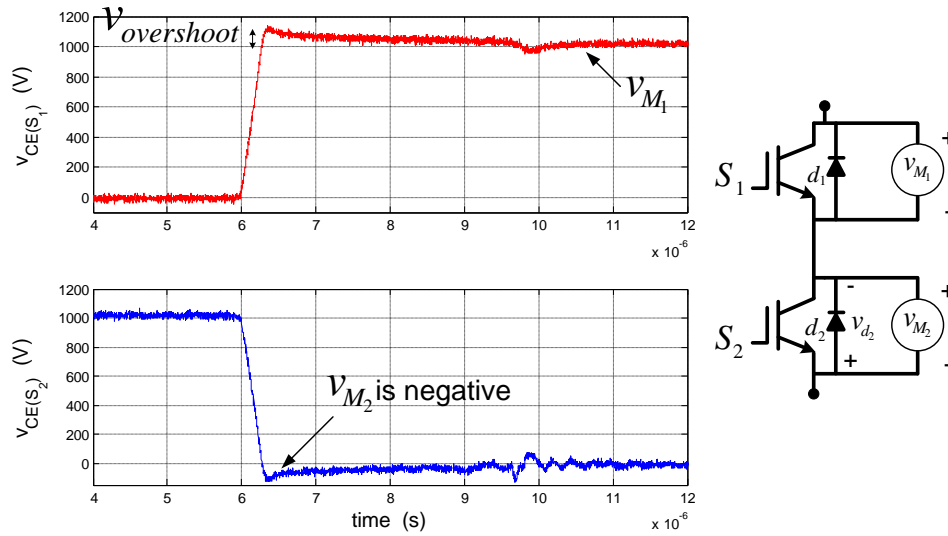


Figure 7.11: Overshoot analysis

The anti-parallel diode of the 1700 V IGBTs is connected internally, thus there is not much that can be done to improve the forward recovery of the device. Placing an additional diode in parallel across the existing diode is not good practice. This is because thermal runaway of the devices could occur due to the diodes not sharing the forward current equally. A measurement is, however, taken with 1 200 V diodes connected in parallel to the existing diodes. This is done to prove that the forward recovery of the left leg diodes increases the overshoot across the respective IGBTs. The bus voltage  $V_{In}$  is reduced to 800 V to ensure that the parallel diodes are operating in their safe operating area SOA. This measurement is shown in Figure 7.12.

The figure shows that the overshoot is reduced with the additional diodes connected in parallel to the existing diodes. The voltage peak is reduced by 35 V, which is a 4.3% reduction of the previous overshoot. The voltage waveform of the externally connected diode measurement is distinctly different to that of the unconnected diode measurement. The voltage overshoot of the circuit without the external diodes clearly shows the forward recovery of the diode voltage superimposed on the voltage across IGBT  $S_1$ . This forward recovery voltage is almost identical to that shown in Figure 7.10.

The voltage waveform, including the parallel connected diodes, depicts no forward recovery voltage superimposed on the bus voltage  $V_{In}$ . Simply put, the overshoot voltage is seen to be constant as diode  $d_2$  turns on.

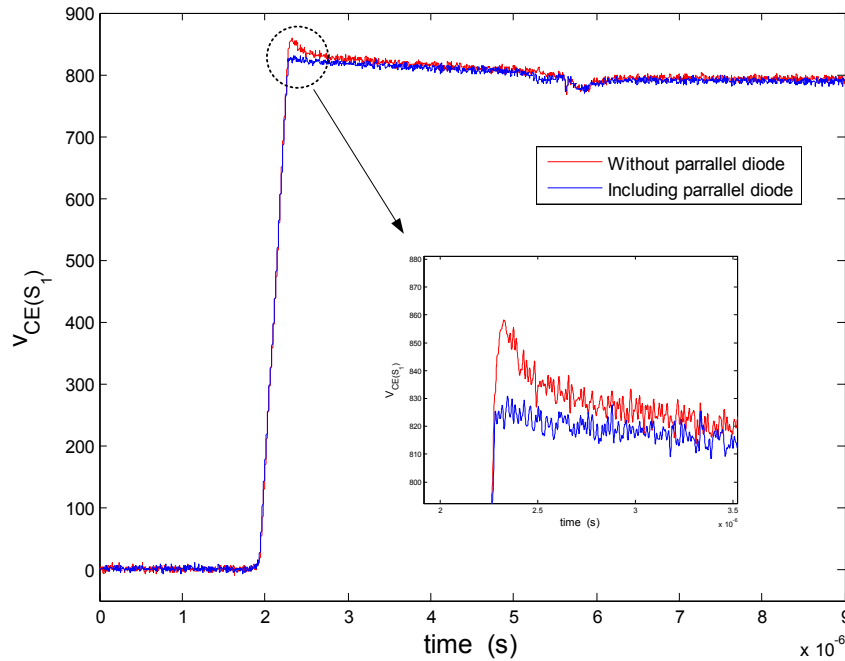


Figure 7.12: Overshoot comparison with and without parallel freewheeling diodes

#### 7.4.6 Conclusion with regard to Voltage Overshoot

The voltage overshoot occurring across the IGBTs is the limiting factor that explains why the bus voltage  $V_{In}$  cannot be increased to the required voltages. The bus voltage  $V_{In}$  is therefore limited to a value under 1 100 V to keep the IGBTs operating within their safe operating conditions. This reduced voltage is a major disadvantage for the SST, as the number of cells  $N$  must be increased to connect the SST to the required distribution voltage levels. Nine extra cells are therefore required in the SST if the bus voltage  $V_{In}$  is reduced to 1 100 V.

Further investigation to increase the bus voltage  $V_{In}$  of each cell is therefore beneficial to the SST concept. The possible solutions are to purchase the 1700 V IGBT without the internal diode and to connect a superior diode externally. However, this will bring unwanted stray inductance  $L_s$  into the circuit. Other options would be to purchase another type of IGBT that has improved characteristics. Currently other 1 700 V IGBTs are only available in larger modules, as opposed to the T0-247 Package. The allowable switching frequencies of these devices are also inferior to those of the existing IGBT. A trade-off between a higher bus voltage, package size and switching frequency is therefore required in the second iteration of the modular cell.

## 7.5 DC-DC Efficiency

The efficiency of the DC-DC converter was tested using the setup described in Section 7.2. The bus voltage  $V_{In}$  was set to 1 000 V and the load was systematically increased. The incoming voltage  $V_T$  was reduced to 1 000 V, to avoid the possibility of the cell failing due to voltage



overshoot. The voltage regulation of the high voltage source is relatively poor, because the input voltage  $V_T$  dropped by 85 V as the load was increased to 2.2 kW. Nonetheless, this was not a serious concern, as the power was measured on the input as well as the output of the cell.

Digital multimeters were used to measure the voltages and currents of the system to ascertain the efficiency of the converter. Multimeters were used, because the voltages and currents of the system are DC, and thus high frequency information was not required. The efficiency was measured using four Fluke digital multimeters, and due to the high voltage of  $V_{In}$ , the primary voltage was divided down using a resistive divider circuit. The thevenin equivalent of the resistive divider was therefore calculated to obtain the true measured voltage.

The other three multimeters were used to measure the input current  $I_{In}$ , the output current  $I_{Out}$  and the output voltage  $V_{Out}$ . The accuracy of the multimeter voltage and current measurements is given as 0.1% and 0.05% respectively, which is obtained from the datasheet of the respective multimeter. Although there are more accurate methods of measuring the efficiency, the accuracy of this method is sufficient for the scope of this thesis.

The modular cell is required to process 1.8 kW in the SST, but this cell was designed to operate at 2.2 kW. Figure 7.13 shows the measured efficiencies, as the power is increased to 2.08 kW. The maximum power of 2.2 kW was not obtained, because the IGBTs failed at this power level. The reason for this is explained later in this section.

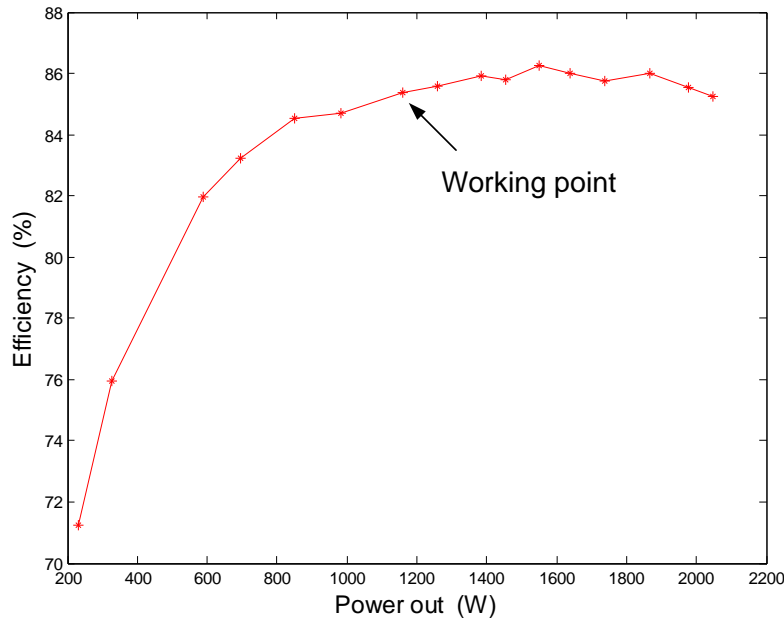


Figure 7.13: DC-DC converter efficiency

From Figure 7.13, the maximum efficiency obtained is shown to be 86%; this efficiency is surprisingly low. The total losses in the cell are measured as 338 W at the maximum output power level of 2.08 kW. These losses are much higher than expected, thus it was initially unknown where these additional losses were being generated. The possible areas where these losses could

occur are in the IGBTs, the high frequency transformer or the passive rectifier. The explanation below explains the steps taken to clarify where these additional losses occur.

The heatsink of the two full bridge converters is designed by using the theoretical value of the losses. Due to the excessive losses, it is possible that the thermal dissipation characteristics of the heatsink are insufficient at this power level. The tests that follow are therefore conducted at a reduced power level, namely 1.2 kW. This is done to ensure that the maximum junction temperature  $T_{J(max)}$ , of the IGBTs is not exceeded. This working point is shown in Figure 7.13.

The efficiency is recalculated at this working point to obtain a more accurate classification of the losses. The theoretical efficiency amounted to 93.1%, the in-depth calculation of the losses is discussed in Appendix A. The error between the predicted losses and measured losses is 230%. Thus the individual losses of the converter are measured to clarify the differences between the theoretical and measured losses.

An indication of the losses emitted by the IGBTs is obtained by measuring the steady state temperature of the heatsink. A comparison between the measured and theoretical losses of the IGBTs can therefore be obtained. The temperature of the heatsink and the transformer core were therefore measured at the specified working point, with the results being shown in Figure 7.14.

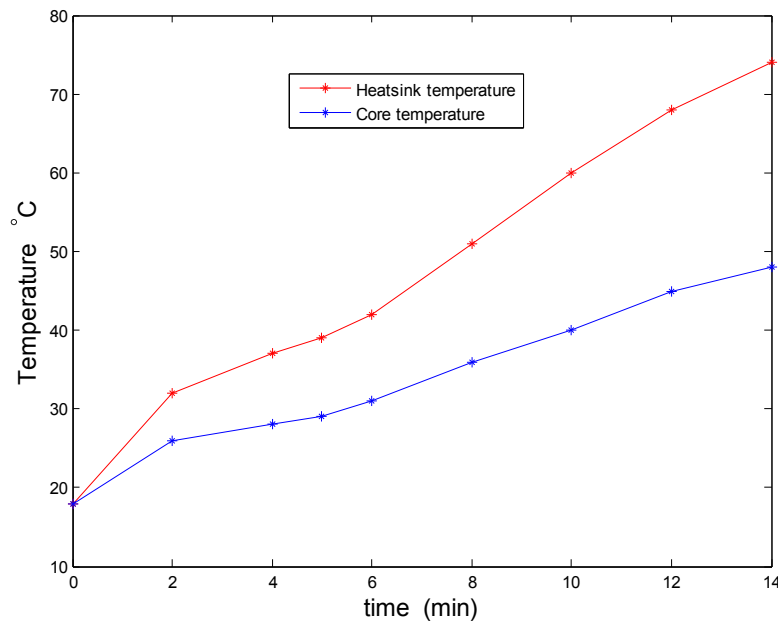


Figure 7.14: Temperature measurements of the cell

It can be seen in the figure that the temperature of the transformer core increased, but the core temperature was still in its safe operating area. The heatsink temperature, however, increased rapidly. The heatsink temperature rose above 70°C within 14 minutes. This temperature also exceeded the theoretically predicted temperature. As a result, the test was interrupted to protect the IGBTs. Clearly, the power emitted by the IGBTs is one of the areas where the

additional losses are being generated. The steady state temperature was not reached, thus the amount of losses occurring in the IGBTs could not be determined. This measurement did prove, however that the IGBTs are emitting much greater losses than expected.

The specific 1 700 V IGBT is not rated at a specific switching frequency, neither is anything stated about tail currents. A tail current refers to the small amplitude of the collector current that remains flowing for a considerable amount of time after the IGBT has switched off. The amplitude of this current is relatively small, although the full blocking voltage is across the IGBT, hence large losses are dissipated in the device. This is the most probable cause of these additional losses occurring in the IGBTs. Thus, the waveforms of the current and voltage of the respective IGBTs must be measured to clarify whether tail currents are present.

The next step was to find out if the transformer and rectifier were also emitting more losses than expected. This was done by means of an infra red image taken of the cell at a main heatsink temperature of  $70^{\circ}C$ . This image is shown in Figure 7.15.

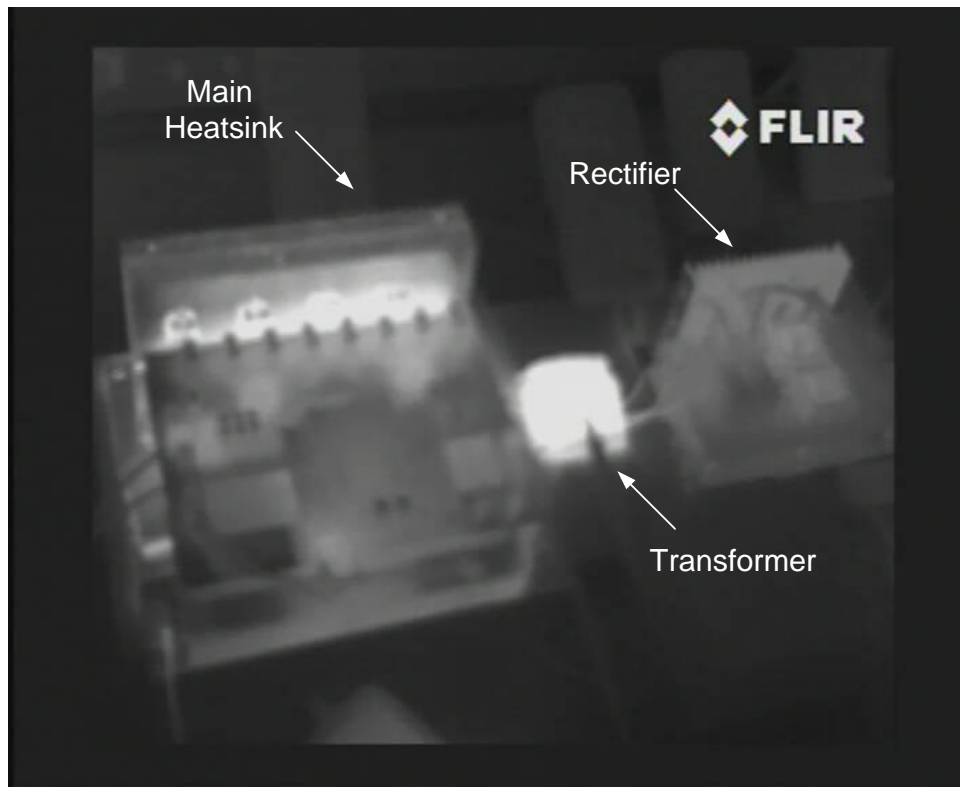


Figure 7.15: Infra red image of the modular cell

The image shows that the main hotspots of the cell are on the main heatsink as well as in the transformer. The excessive heat of the heatsink was expected, though not that of the transformer. The temperature of the transformer core is shown in Figure 7.14; it resulted in an acceptable temperature, although the temperature of the windings was not included in this measurement. The transformer windings were designed to operate at a switching frequency of 50 kHz, hence the diameter  $d$  of the conductors was chosen as  $d = 2\delta$ , with  $\delta$  defined as the skin

depth. The primary winding consisted of two litz wires, whereas three litz wires were used on the secondary winding. The excessive temperature of the windings is therefore caused by the proximity effect and possibly that of the skin effect.

The proximity effect refers to eddy currents which are induced in conductors, or in a layer of windings, due to other current carrying conductors in proximity to the conductor [11]. The proximity effect is especially noticeable at higher frequencies and as the number of winding layers increase. This causes the effective resistance of the winding to increase, which causes additional losses. The transformer was designed and built by ignoring the proximity effect. The three windings of the transformer were wound directly on top of each other, and hence the proximity effect should of been taken into account.

The proximity effect is reduced by adding additional litz wires in parallel and twisting them in a twisted pair configuration. This reduces the proximity effect, as the induced voltages cancel each other out. The multiple litz wires twisted in parallel moreover increase the geometric radius of the conductor; this is a disadvantage because fewer windings can be placed onto a bobbin.

Regarding the skin effect of the conductors, the frequency components flowing in the primary winding are obtained by taking the FFT of the primary current  $i_p$ . This was done to ascertain whether the upper limit design frequency of 50 kHz was sufficient. This is seen in Figure 7.16.

The figure shows that a large number of odd harmonics are present above the switching frequency of 35 kHz. The THD of the waveform until the 20<sup>th</sup> harmonic is calculated as 42%, which means that 42% of the current components are above 35 kHz. Thus, it is evident that the upper limit frequency of 50 Khz was insufficient in the conductor design. The second iteration of the transformer should therefore be designed at a higher frequency, and thus more parallel connected litz wires are required in each winding. The information regarding the proximity effect was obtained from [11].

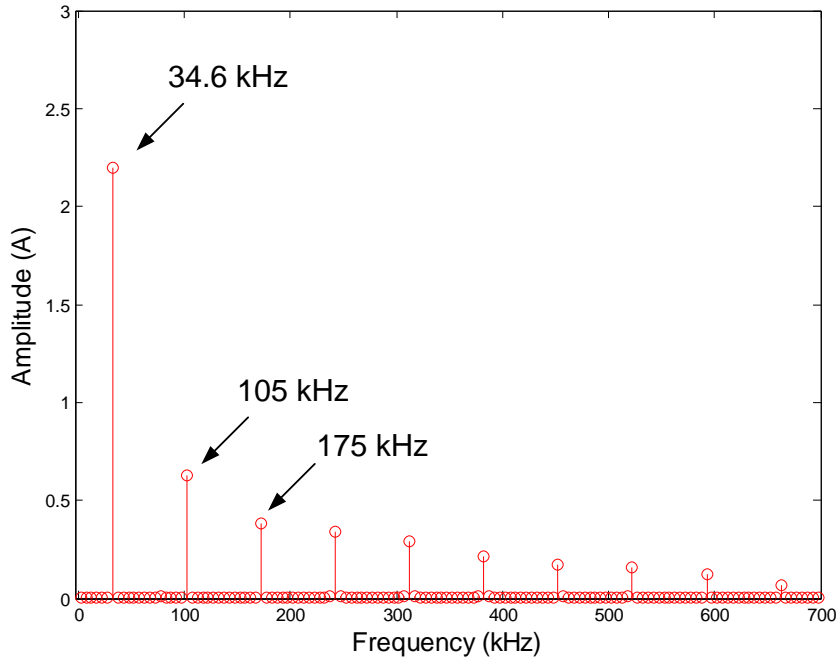


Figure 7.16: FFT of the primary current  $i_p$

### 7.5.1 Efficiency Conclusion

The efficiency of the first iteration of the modular cell was far below the designed specifications, and thus the losses in the converter were investigated. It was found that the IGBTs in the full bridge converter were emitting far greater losses than expected. The IGBTs failed on two occasions, because their maximum junction temperature  $T_{J(max)}$  was exceeded. The modular cell therefore never achieved its designed power rating for a sustained period of time.

The theoretical switching and conduction losses of the IGBTs are far below the devices' maximum ratings. The presence of tail currents in the IGBT is the most probable clarification of these additional losses. The modular cell was however built so compactly that a current probe could not be inserted over the IGBT leads. Thus, the physical voltage and current waveforms of the IGBTs have not been measured. It is possible, though, to break the circuit of the IGBTs and to connect a conductor in series with the circuit, which would allow the use of a current probe. However, this method would introduce a large amount of stray inductance into the circuit. Nonetheless, this method would make it possible to determine the losses occurring in the IGBTs because the voltage and current of the IGBT can be measured simultaneously. This measurement is proposed for future work on the modular cell. Unfortunately, not much can be done about tail currents in the present converter; but if it is found that tail currents are indeed present, then other IGBTs will have to be purchased.

The infra red image taken of the cell showed that the transformer windings were becoming excessively hot. The main losses occurring in the windings were caused by the proximity effect between the stacked winding layers. It was also noted that the upper limit frequency of 50 kHz

should be increased to reduce the skin effect of the conductors. The efficiency of the transformer can be improved if these factors are taken into account when designing the second iteration of the transformer.

### 7.5.2 Conclusion with regard to the Modular Cell

The first iteration of the modular cell was built and tested during the research for this thesis. The two full bridges as well as all the auxiliary circuitry functioned correctly. The IGBTs in the full bridge converters, however, did fail on numerous occasions throughout the testing phase. The source of these failures was investigated. The two main reasons for the IGBT failure were found to be the voltage overshoot across the devices and the excessive junction temperatures.

The voltage overshoot occurring across the IGBTs was investigated and it was found that the cause of this was the forward recovery of the internal freewheeling diodes. This was discussed and justified by improving the overshoot by 4%. The relevant measurements were shown. The bus voltage  $V_{In}$  of each cell can therefore be increased by using alternative freewheeling diodes.

A bus voltage  $V_{In}$  of greater than 1 100 V cannot be obtained in the cell, even at lighter loads, because the IGBTs fail continuously. It was found that the specific IGBT was unable to operate at the required specifications of the DC-DC converter. It is proposed that lower voltage IGBTs, which can operate at the required switching frequency, should be used in the second iteration of the cell. The cell is designed in such a way that alternative IGBTs can simply be inserted without any hardware alterations. The modular cell is therefore suitable for the second iteration of the prototype using different IGBTs.

## 7.6 Analysis of the Series Stacked Converter

The partial concept of the series stacked SST is discussed in this section. Two modular cells are connected in series with their outputs connected in parallel, thereby forming a series stacked converter. The active rectifiers of the modular cell are disabled, and hence the converter is classified as a series input parallel output (SIPO) converter. The high voltage source described in Section 7.2, namely  $V_T$ , is used to test the SIPO converter. The connection diagram of the converter is shown in Figure 7.17. The individual DC cell voltages are defined as  $V_1$  and  $V_2$  respectively.

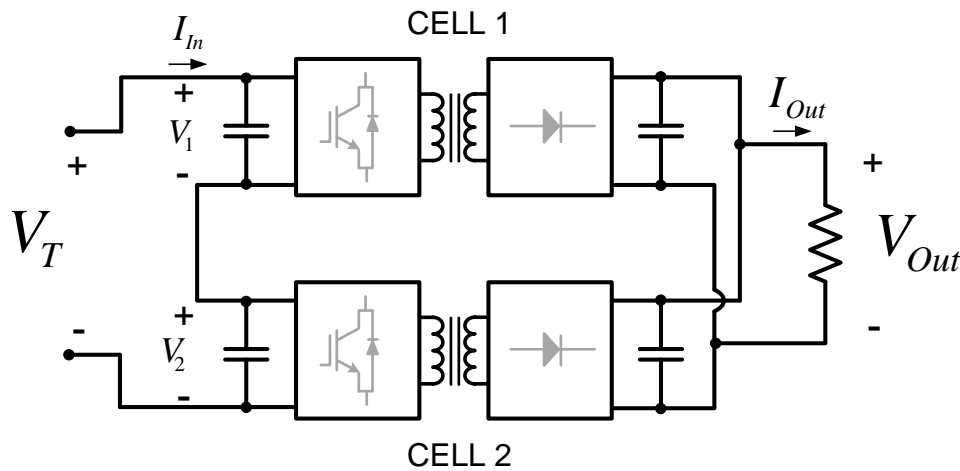


Figure 7.17: Series connection of the two cells

The benefit of using the SIPO converter is that the switching signals can be interleaved. Interleaving of the switching signals reduces the ripple current that is superimposed on the load current  $I_{Out}$ . This can be achieved as the switching frequency  $f_s$  effectively becomes  $N \cdot f_s$ . The concept of interleaving is shown in Figure 7.18 and 7.19, with the transformer primary voltages defined as  $v_{P_1}$  and  $v_{P_2}$ . The intervals where power is transferred to the load are defined as  $p_L$ . It can therefore be seen that by shifting the phase  $\phi$  optimally between the transformer primary voltages, the frequency of  $p_L$  is doubled. The cell controllers are therefore synchronized to obtain the interleaved switching signals. This was achieved by using the fibre optic communication links on each cell controller [40]. Simply put, the two clocks of the PWM generators are synchronized.

The integral part of this converter is that the input voltages balance equally among the cells. The voltage balancing of this converter is dependent on the duty cycle of each cell, namely  $D_1$  and  $D_2$ . The relation of the input voltages with respect to the duty cycle is given as:

$$V_1 D_1 = k \quad (7.5)$$

$$V_2 D_2 = k \quad (7.6)$$

The constant  $k$ , which appears in both Equations 7.5 and 7.6, is identical, thus the relation of

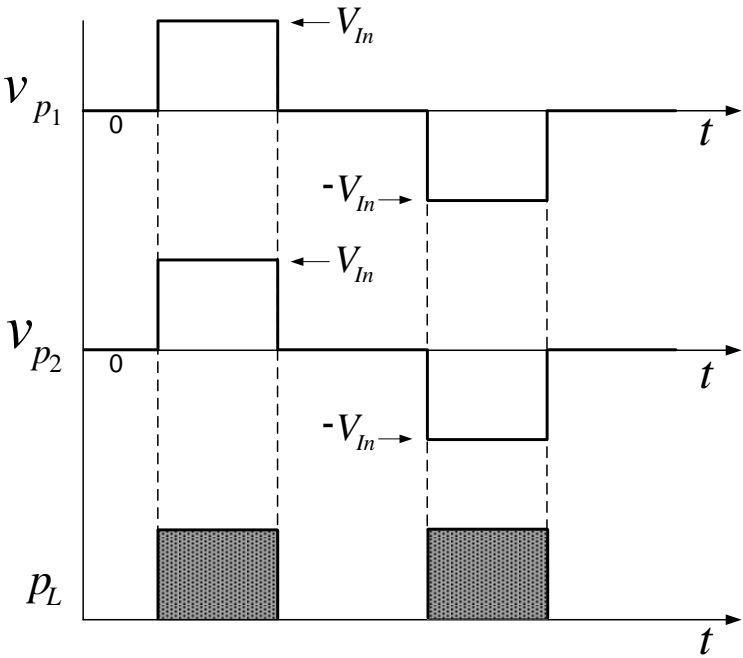


Figure 7.18: Non-interleaved switching signals

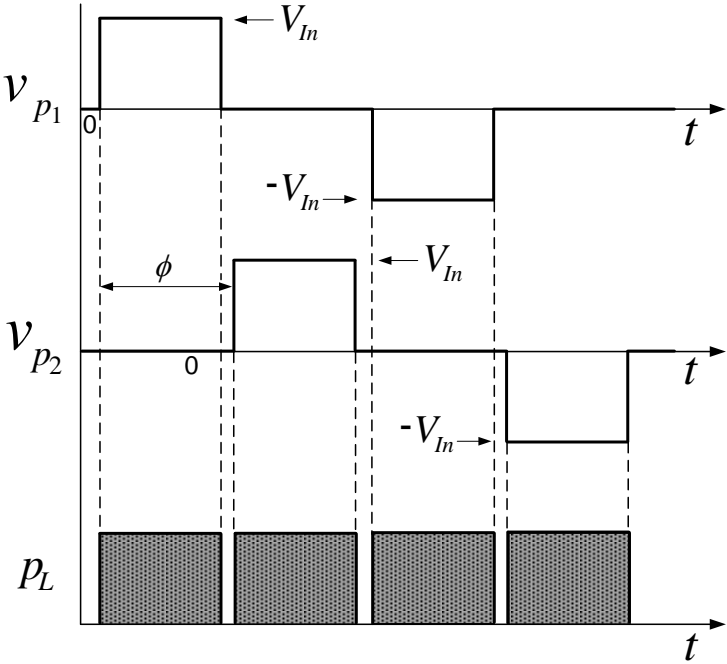


Figure 7.19: Interleaved switching signals



the cell voltages is simplified to:

$$V_1 D_1 = V_2 D_2 \quad (7.7)$$

Thus if both duty cycles are equal, then the individual cell voltages will be identical, namely  $V_1 = V_2$ . Further information regarding the actual parameters that govern the natural balancing mechanism is available in [22; 56].

The validity of Equation 7.7 was tested using the setup shown in Figure 7.17. The incoming voltage  $V_T$  was set to 1.55 kV and the duty cycle of both cells were kept at a constant duty cycle of 40%. The incoming voltage  $V_T$  was set to an amplitude that is greater than the rated value of one individual cell, namely 1.55 kV. This was done to prove the voltage balancing concept; for example, if the voltage does not balance correctly, the incoming voltage  $V_T$  would exceed the voltage rating of either cell. This would lead to the failure of the converter. The voltage balancing results are shown in Figure 7.20.

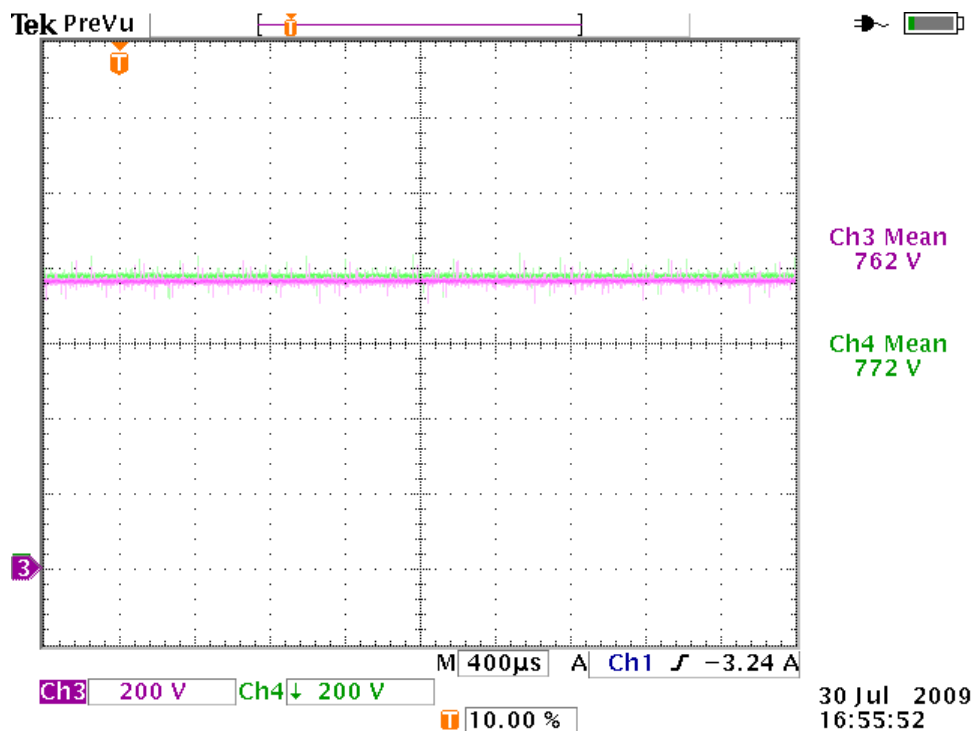


Figure 7.20: Voltages  $V_1$  and  $V_2$  at a total bus voltage of 1.5 kV

It can be seen in the figure that the cell's voltages balanced evenly, whereas the scope trace depicts that there is a 10 V difference between  $V_1$  and  $V_2$ . These voltages were measured with additional multimeters and balanced to an accuracy of 1 V. This voltage difference is caused by the DC offset of the voltage probes. Nonetheless, it is shown that the results concur with Equation 7.7. The output power was set to 1.7 kW for this measurement and an efficiency of 87.5% was obtained. This efficiency is similar to the results obtained for the single DC-DC converter in Section 7.5. A photograph of the system setup is shown in Figure 7.21.

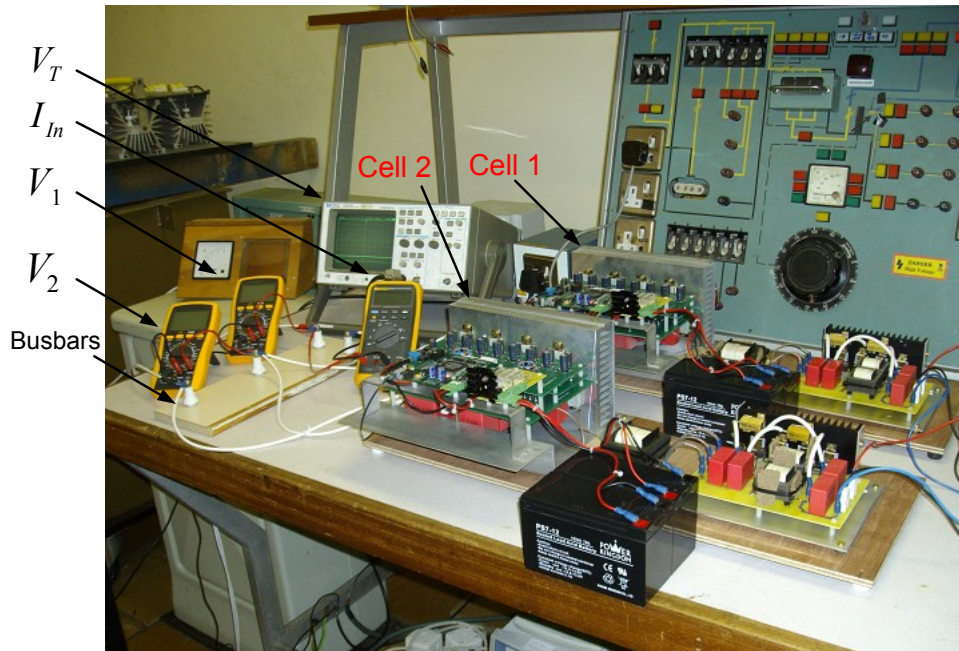


Figure 7.21: Photograph of the SIPO converter

The voltage balancing theory was further tested by forcing an imbalance between the cell voltages. This was done by altering the second cell's duty cycle to  $D_2 = 35\%$ , while  $D_1$  remained constant at  $40\%$ . This imbalance in duty cycle is kept for a specific time interval and thereafter both duty cycles are reset to  $40\%$ . This measurement was taken at an incoming voltage  $V_T = 800$  V. This measurement is shown in Figure 7.22.

It can be seen in the figure that the two cell voltages are initially not balanced because  $D_1 = 40\%$  and  $D_2 = 35\%$ . At time  $t = 35$  ms, duty cycle  $D_2$  is reset to  $40\%$  and the cell voltages balance equally to  $V_1 = V_2 = 405$  V. Before the balancing occurs, the amplitude of the cell voltages are measured as  $V_1 = 375$  V and  $V_2 = 435$  V. These amplitudes concur with Equation 7.7.

The time constant  $\tau$  which is shown in Figure 7.22, is defined as the time interval between the maximum value of  $V_2$ , namely  $V_{2(max)}$  and  $(V_{2(max)} - 0.367V_{2(max)})$ . This time constant  $\tau$  is therefore a specified time interval as the cell voltages are rebalancing. The time constant  $\tau$  was measured at different power levels, which set out to investigate if  $\tau$  was dependent on the load. These measurements were done using non-interleaved switching signals as well as interleaved switching signals. The cell voltages were measured on the bus bars of the high voltage setup, which were placed relatively far away from the converter. Thus, a large amount of noise was present on the measurements. The cell voltages were digitally filtered, and the results are shown in Figure 7.23.

The figure shows that the time constant  $\tau$  remains constant as the output power is increased. No difference occurs in  $\tau$  with either interleaved or non-interleaved switching signals, the average value of  $\tau$  amounted to 1.12 ms.

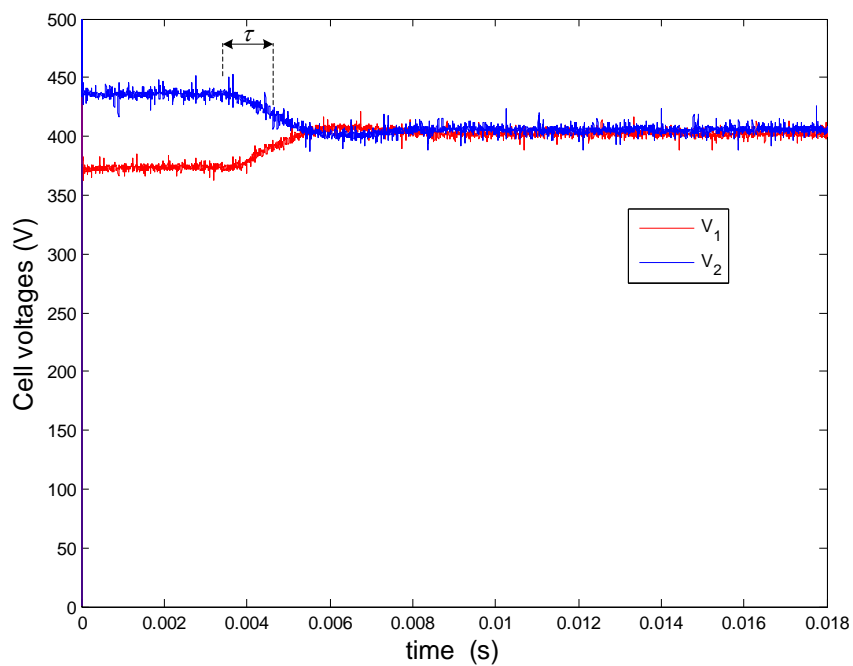


Figure 7.22: Cell voltages under imbalance

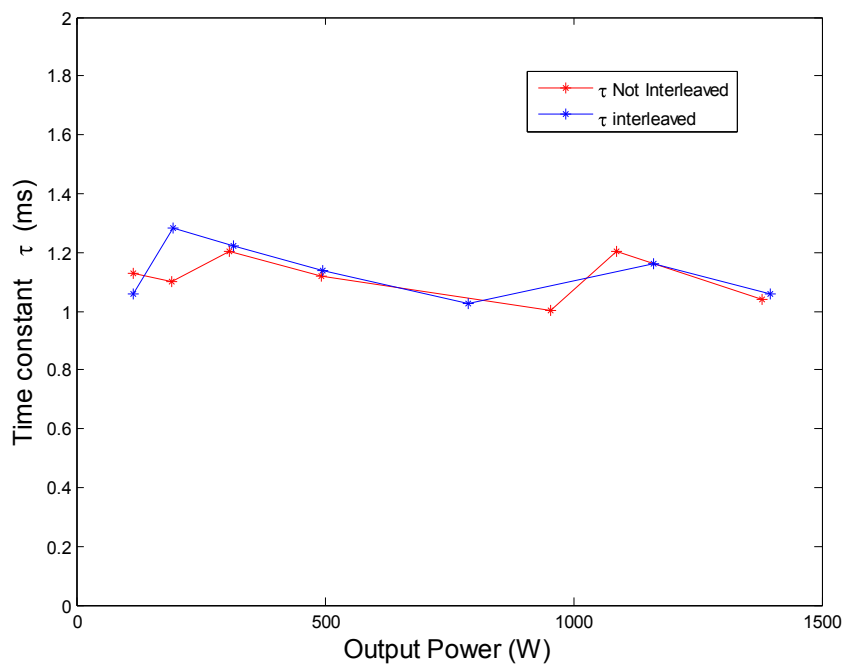


Figure 7.23:  $\tau$  versus load using interleaved and non-interleaved switching

## 7.7 Transient Analysis

The transformer primary currents, namely  $i_{p1}$  and  $i_{p2}$ , are shown in Figure 7.24 as the cell voltages rebalance. Only the envelopes of the currents are shown due to the large time scale of the measurement. The transformer primary currents are seen to differ as the duty cycle  $D_2$  is reset to 40%, at time  $t \approx 3.6$  ms. However, the DC input current  $I_{In}$ , of each cell remains the same because the converter is connected in series. The cell voltage  $V_2$  is initially higher than that of  $V_1$  due to the imbalance of the duty cycle. At  $t \approx 3.6$  ms both duty cycles are reset to 40%, but the cell voltages do not change immediately. Thus in the transient state cell 1 transmits less power to the load than cell 2. This is seen by the amplitude of the respective cell voltages and current envelopes.

Each cell has a passive rectifier on the secondary of the transformer, which means that the current and voltages on the secondary side do not aid the voltage balancing that occurs on the primary of the converter. This however becomes possible if an active rectifier is used. Simply put, the output secondary current in cell 2 can flow through the active rectifier of cell 1 and pass through the transformer of cell 1. This reflected current would therefore influence the primary current of cell 1. However, the analysis of this phenomenon is beyond the scope of this thesis.

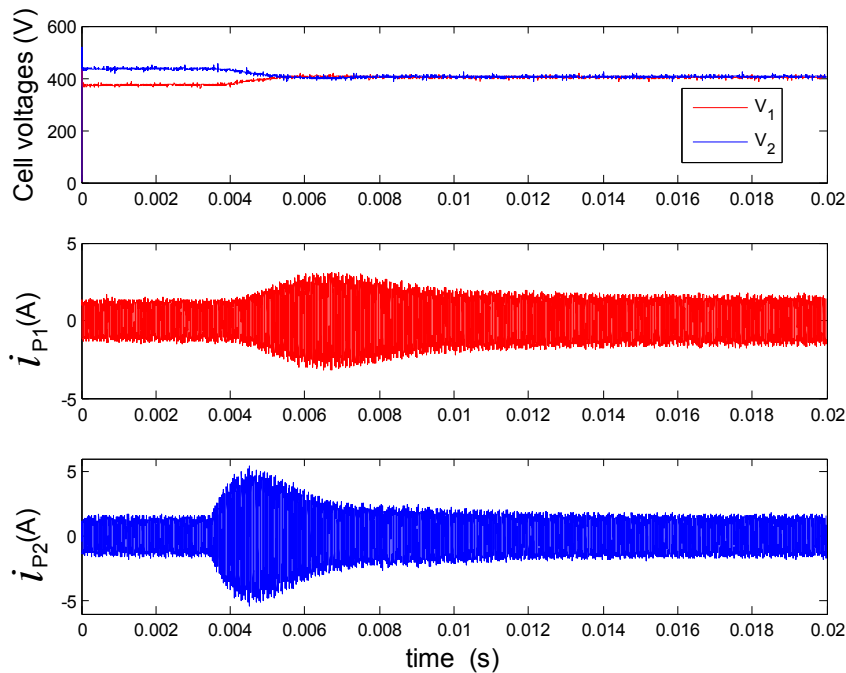


Figure 7.24: Transformer currents  $i_{p1}$  and  $i_{p2}$  as the cell voltages rebalance

The input and output currents, namely  $I_{In}$  and  $I_{Out}$ , were measured as the voltages of the cells rebalance. These results are shown in Figure 7.25. It shows that the output current  $I_{Out}$  remains fairly constant as the cell voltages rebalance. A resistive load is connected to the converter, thus the output voltage  $V_{Out}$  will also remain more or less constant. However, a large

peak is noted on the DC input current  $I_{In}$ , which has the same shape as the current envelope of  $i_{p2}$  in Figure 7.24. The in-depth analysis of these current waveforms with regard to the voltage balancing is beyond the scope of this thesis, but these results are included nonetheless to explain that the maximum current ratings of the semiconductors are not exceeded.

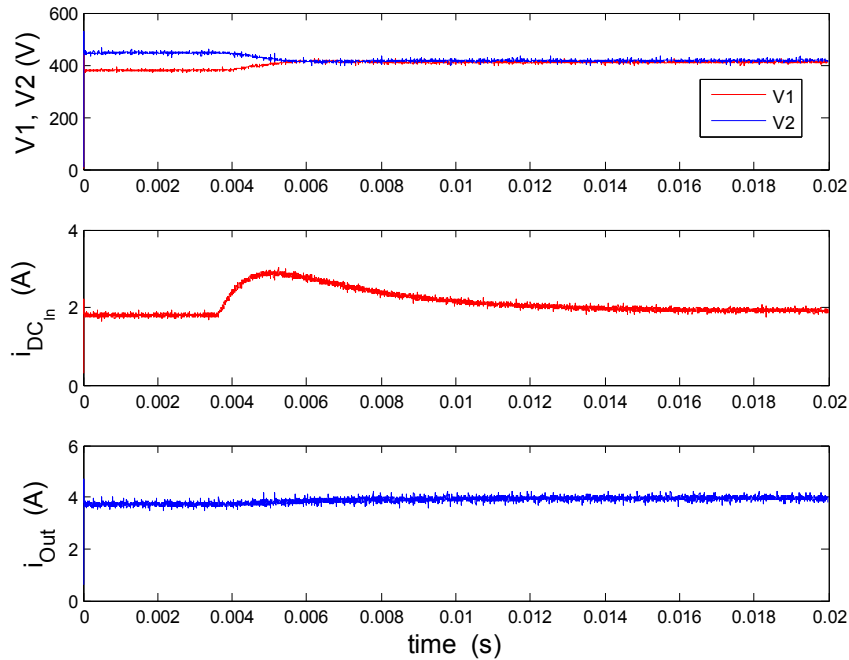


Figure 7.25: Measurement of the input and output currents as the cell voltages rebalance

### 7.7.1 Conclusion with regard to the SIPO Converter

The SIPO converter was constructed and tested with emphasis being placed on balancing the input cell voltages. Two series stacked cells were used with the active rectifier disabled, hence this stage acted as a passive rectifier. The primaries of the cells were connected in series with their outputs in parallel. The cell voltages were also forced into imbalance by altering the duty cycles of the cells. This was done to verify that the cell voltages rebalance as the duty cycles return to their steady state value. The input cell voltages balanced, and the relevant measurements were shown.

## 7.8 Conclusion

The results obtained in respect of all the converters that had been designed and built in this thesis were discussed in this chapter. Particular emphasis was placed on the findings of the three phase inverter and the high voltage DC-DC converter. The high voltage DC-DC converter was evaluated with special attention to the efficiency of the converter. The advantages and

7.8. CONCLUSION

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shortcomings of the converter were discussed. Two modular cells were connected in series and the concept of the series stacked converter was shown. Lastly, the relevant measurements regarding the voltage balancing and efficiency of the converter were included.

# Chapter 8

## Thesis Conclusion

### 8.1 Introduction

This chapter summarizes the findings of each chapter. The future work and possible improvements are also highlighted.

### 8.2 Research Findings

#### 8.2.1 Chapter 1

The solid state transformer was briefly introduced in this chapter and the objectives of this thesis were discussed.

#### 8.2.2 Chapter 2

The characteristics of the conventional distribution transformer were briefly described. The advantages and disadvantages of the transformer were highlighted and existing solutions were mentioned to overcome these disadvantages. Power quality disturbances were briefly summarized and the effect of the conventional transformer when experiencing such disturbances was discussed. The solid state transformer (SST) was introduced to improve on the disadvantages of the conventional distribution transformer. Possible topologies of the SST were discussed, ranging from the AC-AC converter to the series stacked converter. The feasibility of each converter was highlighted and a brief description of their operation was given. The series stacked converter was chosen for the SST prototype due to its modularity. The literature regarding the modular cell and the three phase inverter used in the SST was also discussed.

#### 8.2.3 Chapter 3

The series stacked converter was proposed as the most feasible form of SST due to its modular design [2]. The topology of this converter was discussed and the modular cell was introduced. The detailed design of the modular cell was described, with an emphasis on the power and auxiliary circuits. The design of the magnetic components was discussed with special attention

being paid to the design of the high voltage transformer and the boost inductor. The design of the bus capacitors used in the back-to-back converter was also explained. The cell was constructed using a modular manufacturing approach, which reduces the cost of the individual components. The mechanical design and implementation of the cell was discussed and photographs of the working prototype were included.

#### 8.2.4 Chapter 4

The isolation stage of the modular cell, namely the high voltage DC-DC converter, was discussed in this chapter. The topology selection of the DC-DC converter was briefly explained with regard to the implementation of a modular cell. The DC-DC converter chosen was the phase shifted full bridge converter (PSFB), because of its simplicity with regard to other more complex topologies. The operation of the converter was discussed with an emphasis on the inherent soft switching mechanisms in the PSFB based on [43]. The switching analysis showed that ZVS of the left leg was obtained and that virtually no switching losses occurred on the right leg due to ZCS. The relevant measurements were shown at a bus voltage of 1.3 kV.

The secondary rectifier chosen for the converter was the full bridge center-tapped rectifier. The operation of this rectifier was discussed as well as the ringing voltage that occurred on the secondary rectifier diodes. A modification to the conventional over voltage snubber was introduced and implemented. The snubber circuit reduced the diode ringing voltage from 240% to 18%.

#### 8.2.5 Chapter 5

The operation of the three phase inverter was briefly described with regard to the SST concept. An alternative numerical method was implemented to calculate the switching and conduction losses in a half bridge inverter. The numerical loss analysis was done using an existing inductor current model. The inductor ripple current was calculated by means of this method, as opposed to the analytical method. A comparison was made between the proposed numerical method and the existing analytical method.

The comparison of the two methods showed that there were negligible differences at small values of inductor ripple current. It was found that the conduction losses remained more or less constant, as the inductor ripple current increased. The switching losses, however, increase in a linear fashion as the inductor ripple current increases. The losses of the passive components were also described and the total efficiency of the converter was calculated. The findings of this chapter were published in [45].

#### 8.2.6 Chapter 6

This chapter discussed the design and implementation of a double loop control strategy for a DC-AC inverter. The inner loop control strategy was based on an existing control method used in a full bridge converter. This method was extended to a half bridge converter and the relevant control analysis was discussed. A comparison was done using different carrier waveforms to



improve the response of the inner current loop. Average current mode control was achieved by using a DEPWM carrier waveform and setting the sampling times optimally. The control of the outer voltage loop was implemented by means of a PI controller. The double loop control strategy was tested and an acceptable transient response was obtained. The findings of this chapter were published in [53].

### 8.2.7 Chapter 7

The results of the modular cell and the three phase inverter were described in this chapter. The high voltage DC-DC converter of the modular cell was evaluated, highlighting the advantages and short comings of the first prototype. This chapter discussed the voltage overshoot occurring across the IGBTs as well as presenting a method to reduce the overshoot. The efficiency of the DC-DC converter was calculated and compared with the measured efficiency. The concept of the series stacked SST was partially proven by connecting two modular cells in series. The balancing mechanism occurring in the series stacked converter was investigated. This chapter summarizes the results of all the converters built and tested in this thesis.

## 8.3 General Thesis Conclusion

The concept of a SST was discussed with special attention to the advantages that could be added to the existing network. The existing research regarding solid state transformers was discussed with special attention to the different available topologies. The most feasible topology was chosen namely the series stacked SST based on [2]. The advantages of this topology as opposed to other topologies was also discussed. The main objectives of this thesis were to design and evaluate the different components in the series stacked SST. The design and implementation of the modular cell and that of the output stage of the SST were discussed. The following sections briefly summarise the two main aspects of this thesis:

### 8.3.1 Output Stage of the SST

The half bridge inverter was chosen for the output stage of the SST and the reasons for this were discussed. An extended loss analysis was done on the switching devices of the half bridge inverter. This numerical analysis was based on the use of an existing inductor current model in order to accurately calculate inductor current. The switching device losses were therefore calculated as the inductor ripple current varied. The numerical analysis resulted in a beneficial result with regard to the switching losses in an inverter. The results of this analysis were used to design the 80 kW three phase inverter.

The second aspect of the output stage was based on the control strategy. A double loop control strategy was developed and thoroughly discussed. The inner loop predictive controller was designed using the superposition of the different states which occur in the inverter. The inner loop controller was evaluated and successful results were obtained. A PI controller was developed for the outer voltage loop. The inner current loop was therefore inserted into a double

loop control strategy consisting of the outer voltage loop. The double loop control strategy was tested and compared to that of the open loop system. The results of the closed loop system depicted a large improvement with regard to the transient response of the system.

### 8.3.2 The Modular Full Bridge Converter

The different available topologies that could be used for a modular converter were discussed and the full bridge back-to-back converter was chosen. This decision was based on the trade-off between the additional switching devices as opposed to the large bus capacitors which would be required for a half bridge converter. The design of the modular converter was based on the size, cost and ease of manufacturing with regard to the SST concept. The thesis discussed the in-depth design and manufacturing process of the modular converter.

The emphasis of the modular converter with regard to the thesis was based on the evaluation of the high voltage DC-DC converter. The DC-DC converter was implemented using a phase shifted modulation technique based on [43]. The modulation technique offered inherent soft switching transitions which increased the efficiency of the converter. These soft switching transitions were discussed and measured at a bus voltage of 1.3 kV.

The IGBTs did however fail at a bus voltage of 1.3 kV and the reasons for this were analysed and relevant solutions were found. The characteristics of the free-wheeling diode and the large IGBT tail current were found to be the cause of the IGBT failure. The relevant tail current and other additional measurements are included in Appendix B.

The concept of the SST was partially proven by connecting two of the modular cells in series on their inputs and in parallel on their outputs. This SIPO converter demonstrated that the individual cell voltages balanced equally among the cells. The SIPO converter was also connected to the three phase inverter which demonstrated the concept of the SST.

## 8.4 Improvements and Future Work

### 8.4.1 Modular Cell

It is proposed that the IGBTs' collector current and the voltage across the IGBTs be measured simultaneously. This will make it possible to determine the exact losses occurring in the IGBTs, thereby facilitating the implementation of a more conclusive thermal analysis. It is assumed that the voltage overshoot and the heat dissipation of the current IGBTs are the main causes of failure in the cell. Thus it is suggested that other 1 700 V IGBTs be used, however, these proposed devices are only available in larger IGBT modules. The advantage of these modules is that their thermal dissipation is better than that of the existing IGBTs. The allowable switching frequency of these IGBTs is also less than the required switching frequency of the isolation stage, which is a disadvantage. Thus in order to maintain the same bus voltage by using the proposed new IGBTs, the switching frequency would have to be reduced.

The second option is to de-rate the bus voltage of each cell and to use 1 200 V IGBTs; this would allow the switching frequency of 35 kHz to be maintained. At the same time, though, this

would increase the number of cells required for each series stacked converter. Thus, a trade-off is required between the switching frequency and the amplitude of the bus voltage.

#### **8.4.2 Three Phase Inverter**

The operation of the inductor current loop was found to be acceptable. Additional research is required in respect of the outer voltage loop with regard to the THD of the output voltage. An alternative control strategy, other than the PI controller, is proposed. This is necessary because the PI controller is dependent on the load, thus as the load changes, so does the response of the outer voltage loop.

### **8.5 Summary**

The MSc project was thoroughly enjoyed and it was a pleasure to work in the power electronics group (PEG) laboratory. A considerable amount was learned from the supervisors of this project, namely Professor T. Mouton and Mr. W. van der Merwe.

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## Appendix A

# Efficiency of the DC-DC Converter

The efficiency of the DC-DC converter is calculated in this section and compared to the measured efficiency. The working point used is shown in Figure 7.13. The measured parameters of the DC-DC converter at this working point are shown in Table A-I.

Table A-I: Parameter descriptions

Parameters		
$V_{In} = 948.2 \text{ V}$	$V_{Out} = 470.92 \text{ V}$	$P_{Load} = 1160.8 \text{ W}$
$I_{In} = 1.435 \text{ A}$	$I_{Out} = 2.465 \text{ A}$	$\frac{N_2}{N_1} = \frac{29}{85}$
$V_f = 2.2 \text{ V}$	$V_{f(IGBT)} = 1.515 \text{ V}$	$V_{CE(sat)} = V_{(on)} = 1.975 \text{ V}$
$C_{(1;2;3;4)} = 110 \text{ pF}$	$f_s = 35 \text{ kHz}$	$L_\sigma = 67.86 \text{ uH}$
$L_1 = L_2 = 1.1 \text{ mH}$	$D = 40 \%$	

The losses are calculated in this section by firstly obtaining the transfer function of the converter, followed by the inductor ripple current of the filter inductors. This is required as the inductor current  $i_{L_1}$  is reflected across the transformer, to obtain the amplitude of the current at which the IGBTs switch. The conduction losses in the passive as well as active components are calculated. The switching losses are calculated with regard to the soft switching transitions described in Chapter 4.

### A.1 Converter Transfer Function

The transfer function of the converter is derived from first principles by setting the average of the inductor voltage  $v_{L_1}$  equal to zero. The voltages and current waveforms used to calculate the transfer function are those of zone 2 in Chapter 4:

$$\left[ \left( \frac{N_2}{N_1} \cdot V_{In} \right) - \frac{V_{Out}}{2} \right] \times dT_S = -\frac{V_{Out}}{2} \times \left( \frac{1}{2} - d \right) T_S \quad (\text{A.1})$$

$$\frac{V_{Out}}{V_{In}} = 4 \times \frac{N_2}{N_1} d$$



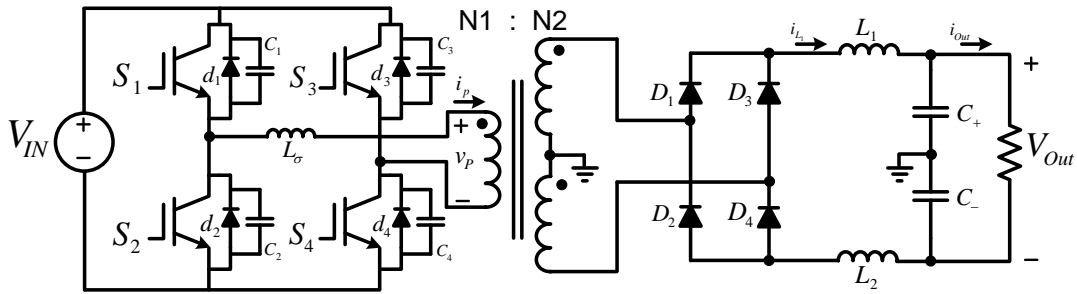


Figure A.1: Schematic diagram of the DC-DC converter

The inductor ripple current  $\Delta i_{L_1}$  is calculated by obtaining the gradient of the inductor current  $\frac{di_{L_1}}{dt}$  in zone 2. Noting that the frequency of the inductor current is twice that of  $f_s$  due to the rectifier configuration. The amplitude of inductor ripple current  $\Delta i_{L_1}$  is derived using first principles and using Figure A.2:

$$\Delta i_{L_1} = \frac{\left( V_{In} \cdot \frac{N_2}{N_1} - \frac{V_{Out}}{2} \right)}{L_1} \times dT_S \quad (\text{A.2})$$

The output current  $I_{Out}$  is equal to 2.465 A, this value is obtained from Table A-I. The voltage drops occurring in the system are disregarded for the inductor ripple current calculation, hence the output voltage is fixed and this value is used in equation A.1. Simply put, the measured output voltage  $V_{Out}$  is therefore inserted into Equation A.1 to obtain the input voltage  $V_{In}$ . The maximum amplitude of the current in  $L_1$  namely  $i_{L_1}(max)$  is obtained by:

$$\begin{aligned} i_{L_1}(max) &= I_{Out} + \frac{\Delta i_{L_1}}{2} \\ &= 2.465 + 0.304 \text{ A} \\ &= 2.769 \text{ A} \end{aligned} \quad (\text{A.3})$$

The minimum inductor current of  $L_1$  namely  $i_{L_1}(min)$  is obtained similarly to Equation A.3 and amounted to 2.161 A.

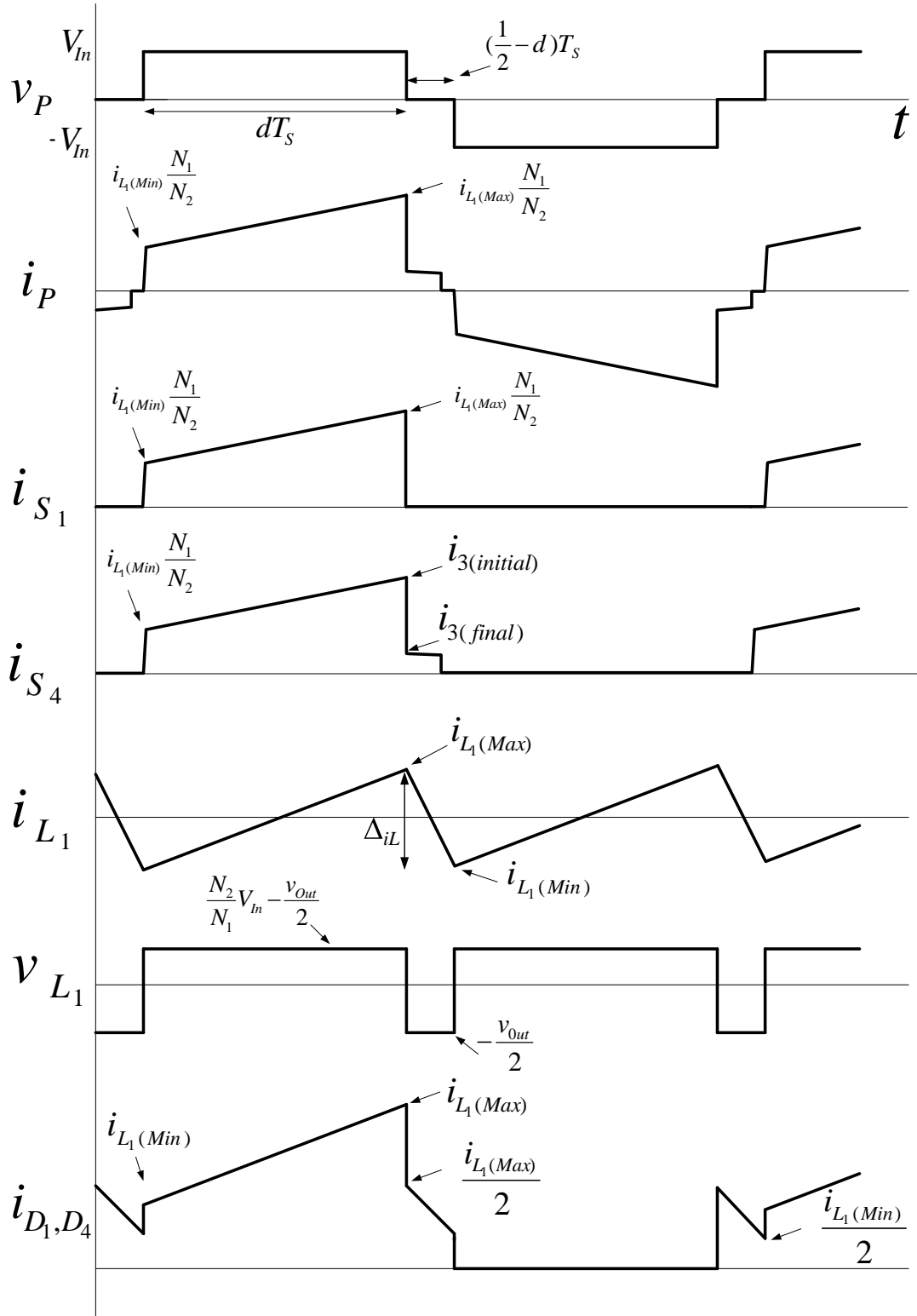


Figure A.2: Ideal waveforms of the respective components

### A.1.1 IGBT Switching Losses

Figure A.3 depicts the primary current  $i_P$  of zones 3-6. IGBT  $S_1$  switches off at  $i_{(3initial)}$  in zone 3 and  $S_2$  switches off at the same amplitude in zone 8. The switching off, of  $S_1$  and  $S_2$  are hard off transitions.

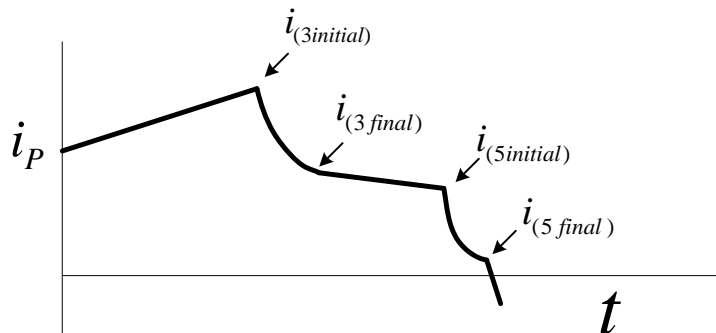


Figure A.3: Expanded primary current  $i_P$

The amplitude of the current in IGBT's  $S_1$  and  $S_2$  at switch-off is calculated by transferring the inductor current across the transformer, and is given as:

$$\begin{aligned} i_{S_1;S_2}(off) &= 2 \cdot i_{L_1}(max) \cdot \frac{N_2}{N_1} \\ &= 1.89 \text{ A} \end{aligned} \quad (\text{A.4})$$

The leakage inductance was measured by shorting out the secondary of the rectifier and applying a reduced voltage on the primary converter. The duty cycle was reduced to 3% and the ripple current  $i_p$  and transformer primary voltage  $v_p$  were used to obtain the leakage inductance  $L_\sigma$ . This inductance  $L_\sigma$  amounted to 67.8  $\mu\text{H}$ . IGBT  $S_1$  and  $S_2$  switch on softly as explained in zone 4 and 9 as the criteria of Equation 4.3 is satisfied.

Referring to Figure A.3, the amplitude at which  $S_4$  switches off at is namely  $i_{(5initial)}$ . The assumption is made that  $i_{(3final)}$  is equal to  $i_{(5initial)}$  at higher duty-cycles. The current amplitude where  $S_4$  switches off is then found by using Equation 4.3 and solving for  $i_{(3final)}$ :

$$\begin{aligned} i_{(3final)} &= \sqrt{i_{(3initial)}^2 - \frac{2 \cdot C_2 \cdot V_{In}^2}{L_\sigma}} \\ &= 1.07 \text{ A} \end{aligned} \quad (\text{A.5})$$

The drop in primary current  $i_P$  to charge  $C_1$  and discharge  $C_2$  is therefore 820 mA.

The limited amount of energy which the leakage inductance  $L_\sigma$  is capable of storing can be improved by adding an additional inductance in series with the primary winding. This would provide for soft on transitions of all the IGBT's if Equations 4.3 and 4.4 are satisfied. The addition of leakage inductance in the converter is however not implemented due to the adverse affects of the ringing voltage on the secondary diodes. Zero volt switching is not achieved for

$S_3$  and  $S_4$  however if the leakage inductance is fully discharged before the beginning of zone 6 zero current switching is achieved.

The amplitude of the incomplete ringing transition of the right leg is given as:

$$\begin{aligned} V_{ring} &= \sqrt{\frac{L_\sigma \cdot i_{(3final)}}{2 \cdot C_4}} \\ &= 578 \text{ V} \end{aligned} \quad (\text{A.6})$$

Thus even if the dead time was set appropriately the amplitude of the ringing voltage would not allow soft switching, as this value is less than the bus voltage  $V_{In}$ . The energy remaining in the leakage inductance  $L_\sigma$  is therefore not sufficient to provide soft switching of IGBT's  $S_3$  and  $S_4$ . ZVS of the right leg switches is therefore hindered by setting dead time large enough to discharge the primary current  $i_p$  to zero. This is done to ensure ZCS of the right leg switches. This increased dead time is advantages for the converter as short circuit protection is not provided. The dead time is therefore set to protect the IGBT's instead of obtaining soft switching.

The primary current  $i_{(5final)}$  is therefore discharged fully before the right leg switches are commutated. The ZCS switching transition is described in Chapter 4, Section 4.1.6. This section explained that switching losses do occur but that these losses are negligible. The losses resulted in 1.7 W per IGBT. This has a major advantage as soft switching is obtained without adding additional leakage inductance  $L_\sigma$ . The dead time is therefore increased to ensure that the leakage inductor is fully discharged before zone 6.

The switching transitions of  $S_1 - S_4$  are tabulated in Table A-II.

Table A-II: Switching transitions

Transition	IGBT	Zone	$v_{CE}$	$i_{CE}$	transition
<b>turn-on</b>	$S_1$	9	0 V	0 A	Soft-on
	$S_2$	4	0 V	0 A	Soft-on
	$S_3$	6	$V_{in}$	$\approx 0 \text{ A}$	$\approx$ Soft-on
	$S_4$	1	$V_{in}$	$\approx 0 \text{ A}$	$\approx$ Soft-on
<b>turn-off</b>	$S_1$	3	$V_{in}$	$i_{(3initial)}$	Hard-off
	$S_2$	8	$V_{in}$	$i_{(3initial)}$	Hard-off
	$S_3$	10	$V_{in}$	$i_{(3final)}$	Hard-off
	$S_4$	5	$V_{in}$	$i_{(3final)}$	Hard-off

The switching loss of each IGBT is calculated using [11]:

$$P_{off} = \frac{f_s}{2} \cdot V_{In} \cdot i_C \cdot t_f \quad (\text{A.7})$$

The total switching losses of the IGBT's are calculated using Table A-II, the measured value of the bus voltage  $V_{In}$  is used for this calculation, Namely  $V_{In} = 948 \text{ V}$ . The rise and fall times

are given as  $t_r = 97 \text{ ns}$  and  $t_f = 150 \text{ ns}$  respectively. The total switching losses are given as:

$$\begin{aligned} P_{off(S_1-S_4)} &= f_s \cdot V_{In} \cdot t_f (i_{(3initial)} + i_{(3final)}) \\ &= 14.73 \text{ W} \end{aligned} \quad (\text{A.8})$$

## A.2 IGBT Conduction Losses

The individual conduction losses are calculated in this section. The average current flowing through each device is calculated using piece wise integration. The conduction losses in rectifier diodes are calculated using the same principle. The conduction losses of  $S_4$  are calculated using piecewise integration of  $i_{S_4}$  in Figure A.2, and given as:

$$\begin{aligned} P_{cond(S_4)} &= \frac{1}{T_s} \int_0^{T_s} V_{(on)} \cdot i_{S_4}(t) \\ &= \frac{V_{(on)}}{T_s} \left[ \int_0^{t_1} \frac{V_{In}}{L_\sigma} \cdot t dt + \int_{t_1}^{t_2^-} \left( i_{S_4}(t_1) + \frac{\frac{N_2}{N_1} \cdot V_{In} - \frac{V_{Out}}{2}}{L_1} \cdot \frac{N_2}{N_1} \cdot (t - t_1) \right) dt \right. \\ &\quad \left. + \int_{t_2^+}^{t_3} \left( i_{S_4}(t_2^+) + \frac{v_{p(zone\ 4)}}{L_\sigma} \cdot (t - (t_2^+)) \right) dt \right] \\ &= V_{on} \cdot 725 \text{ mA} \\ &= 1.432 \text{ W} \end{aligned} \quad (\text{A.9})$$

Referring to Figure A.2 the conduction losses of  $S_1$  are calculated by:

$$\begin{aligned} P_{cond(S_1)} &= \frac{1}{T_s} \int_0^{T_s} V_{(on)} \cdot i_{S_1}(t) \\ &= \frac{V_{(on)}}{T_s} \left[ \int_0^{t_1} \frac{V_{In}}{L_\sigma} \cdot t dt + \int_{t_1}^{t_2} \left( i_{S_1}(t_1) + \frac{\frac{N_2}{N_1} \cdot V_{In} - \frac{V_{Out}}{2}}{L_1} \cdot \frac{N_2}{N_1} \cdot (t - t_1) \right) dt \right] \\ &= V_{on} \cdot 672 \text{ mA} \\ &= 1.32 \text{ W} \end{aligned} \quad (\text{A.10})$$

The conduction losses of  $S_3$  and  $S_4$  are identical and those of  $S_1$  and  $S_2$  are identical. The losses in the free-wheeling diode  $d_2$  are negligibly small and are omitted in the efficiency calculation. The conduction losses for the four IGBTs amount to 5.518 W.

### A.2.1 Rectifier Conduction Losses

The Rectifier diode conduction losses are calculated as follows:

$$\begin{aligned} P_{cond(D_1)} &= \frac{1}{T_s} \int_0^{T_s} V_f \cdot i_{D_1}(t) \\ &= \frac{V_f}{T_s} \left[ \int_{t_0}^{t_1} \left( i_{L_1(min)} + \frac{V_{In} \frac{N_2}{N_1} - \frac{V_{Out}}{2}}{L_1} \cdot (t - t_0) \right) dt \right. \\ &\quad \left. + 2 \int_{t_1}^{t_2} \left( \frac{i_{L_1(max)}}{2} - \frac{V_{Out}}{L_1} \cdot (t - t_1) \right) dt \right] \end{aligned} \quad (\text{A.11})$$

## A.3. MAGNETIC LOSSES

$$\begin{aligned}
&= V_f \cdot 1.124 \text{ A} \\
&= 2.47 \text{ W}
\end{aligned}$$

The average current flowing in diode pairs  $D_1$  and  $D_4$  is the same as that of  $D_2$  and  $D_3$ , thus the conduction losses in the rectifier diodes amounts to 9.89 W. The snubber losses were designed to be 15 W per over-voltage snubber, this for both snubber circuits the losses are approximated as 30 W.

### A.3 Magnetic Losses

The average current flowing inductors  $L_1$  and  $L_2$  is equal to the load current  $I_{Out}$ . The resistance of the inductor namely  $r_{L_1}$  was measured to be 365 m $\Omega$ . The conduction losses in the inductor  $L_1$  ignoring the skin effect is given by:

$$\begin{aligned}
P_{cond(L_1)} &= I_{Out}^2 \cdot r_{L_1} \\
&= 2.217 \text{ W}
\end{aligned} \tag{A.12}$$

This both filter inductors conduction losses amounted to 4.43 W. The transformer conduction losses is also calculated on the same principle and amounted to 1.7 W. The core losses of each filter inductors amounted to 363 mW. This was obtained from the datasheet of the k4022e-26 core [39]. The total core losses of the inductor is therefore given as 726 mW.

The transformer core losses are obtained from the data sheet of the N27 material, however The flux density  $B$  and switching frequency  $f_s$  are required. The flux density  $B$  is calculated using Faradays law:

$$E = N \cdot A_e \frac{dB}{dt} \tag{A.13}$$

$$\begin{aligned}
dB &= \frac{V_{In} \cdot dt}{N_1 \cdot A_e} \\
dB &= 240 \text{ mT}
\end{aligned} \tag{A.14}$$

Using  $dB$  in the datasheet and noting that the core volume is 78600  $mm^3$  the core power losses were obtained as 14.2 W.

### A.4 Active Rectifier Losses

The active rectifier is disabled, however the converter acts as a passive full bridge rectifier. Thus two freewheeling diodes are continuously on, hence losses occur in these devices. The losses of the two freewheeling diodes is given as:

$$P_{diodes} = 2 \cdot v_f \cdot I_{In} \tag{A.15}$$

$$= 4.34 \text{ W} \tag{A.16}$$

### A.5 Efficiency of The DC-DC Converter

The total efficiency of the DC-DC converter is therefore given as:

$$\eta = \frac{P_{Out}}{P_{Out} + P_{Losses}} \tag{A.17}$$

$$\begin{aligned} &= \frac{1160 \text{ W}}{1160 \text{ W} + 85.52 \text{ W}} \\ &= 93.1\% \end{aligned}$$

# Appendix B

## Additional Measurements

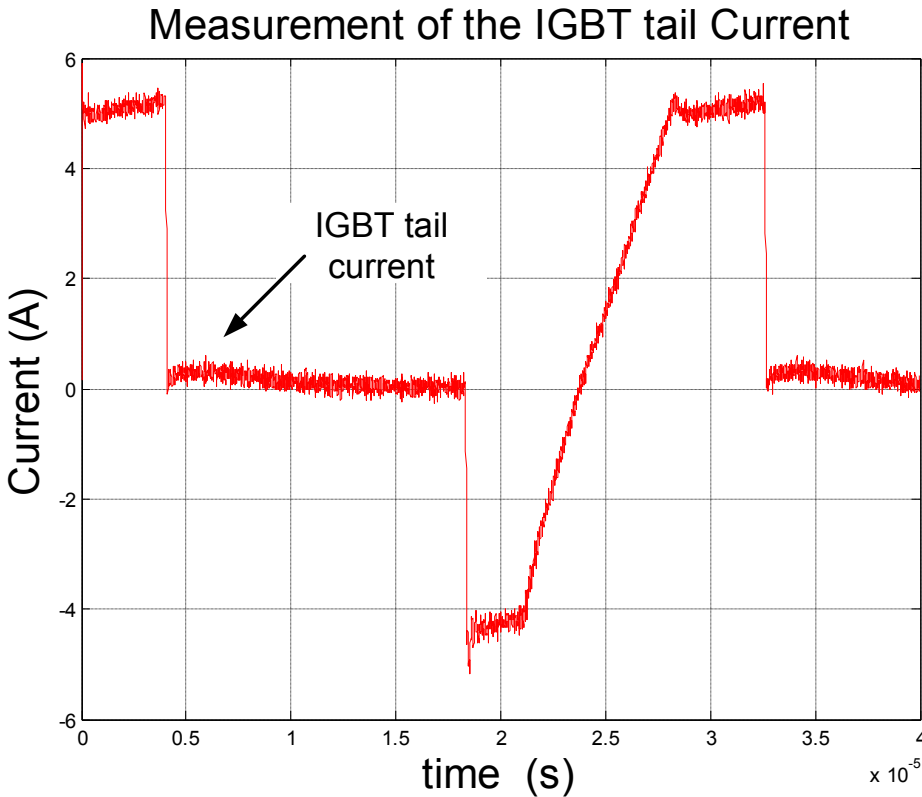


Figure B.1: IGBT tail currents at  $V_{IN} = 200$  V



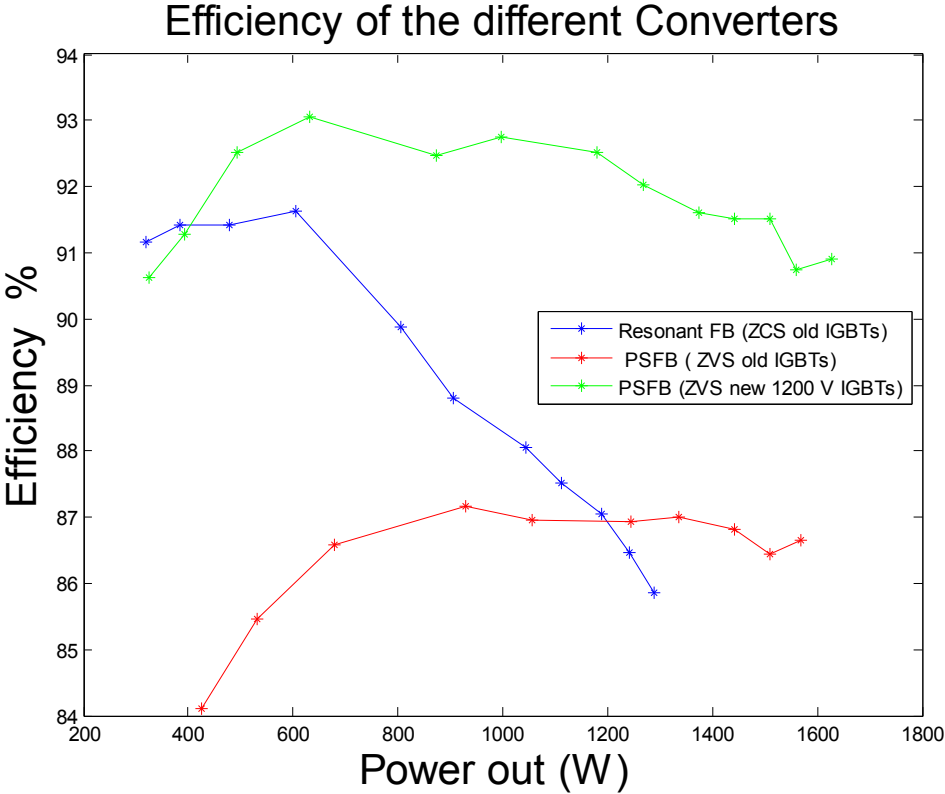


Figure B.2: Efficiency comparison of the different converters: (PSFB 1700 V IGBTs, series resonant converter 1 700 V IGBTs, PSFB 1 200 V IGBTs)

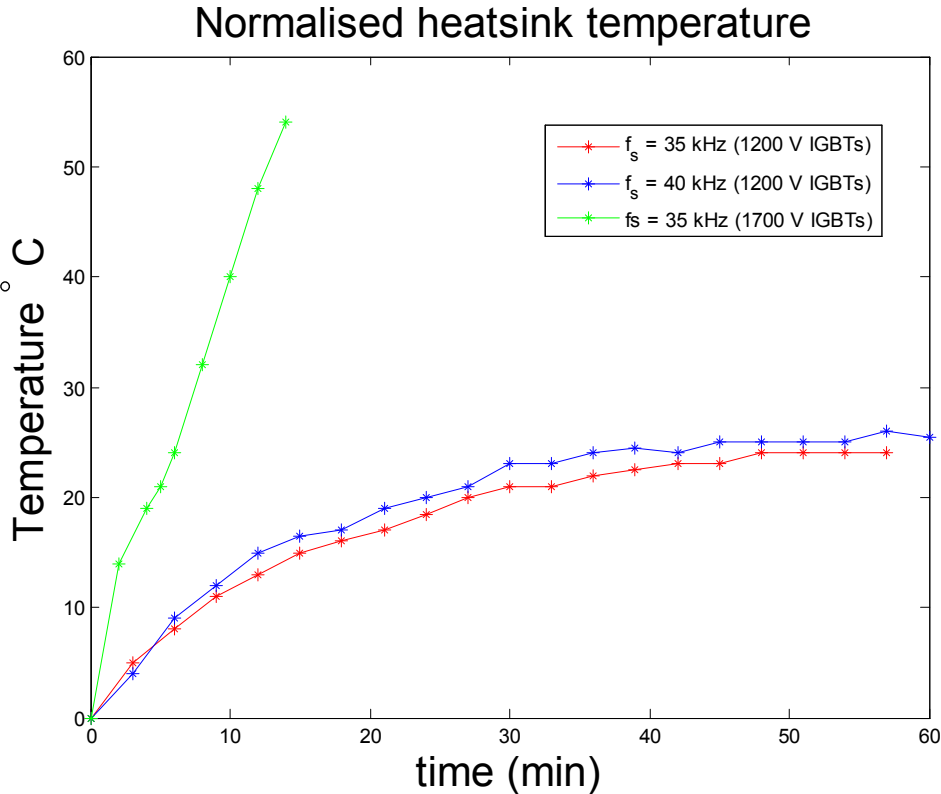


Figure B.3: Comparison of the heatsink temperature with 1 700 V and 1 200 V IGBTs

# Appendix C

## Schematics

### C.1 Inverter Schematics

### C.2 Modular Cell Schematics

The schematics in this section are those of the modular cell. The circuits on these PCBs are repetitive, hence the component descriptions are only included for one circuit due to space requirements. The errors on the PCBs were:

- The isolated supply PCB: Pin 6 of the IR2153d should be connected to the source of Mosfet *M4*. this connection is also required on the other half bridge converter.

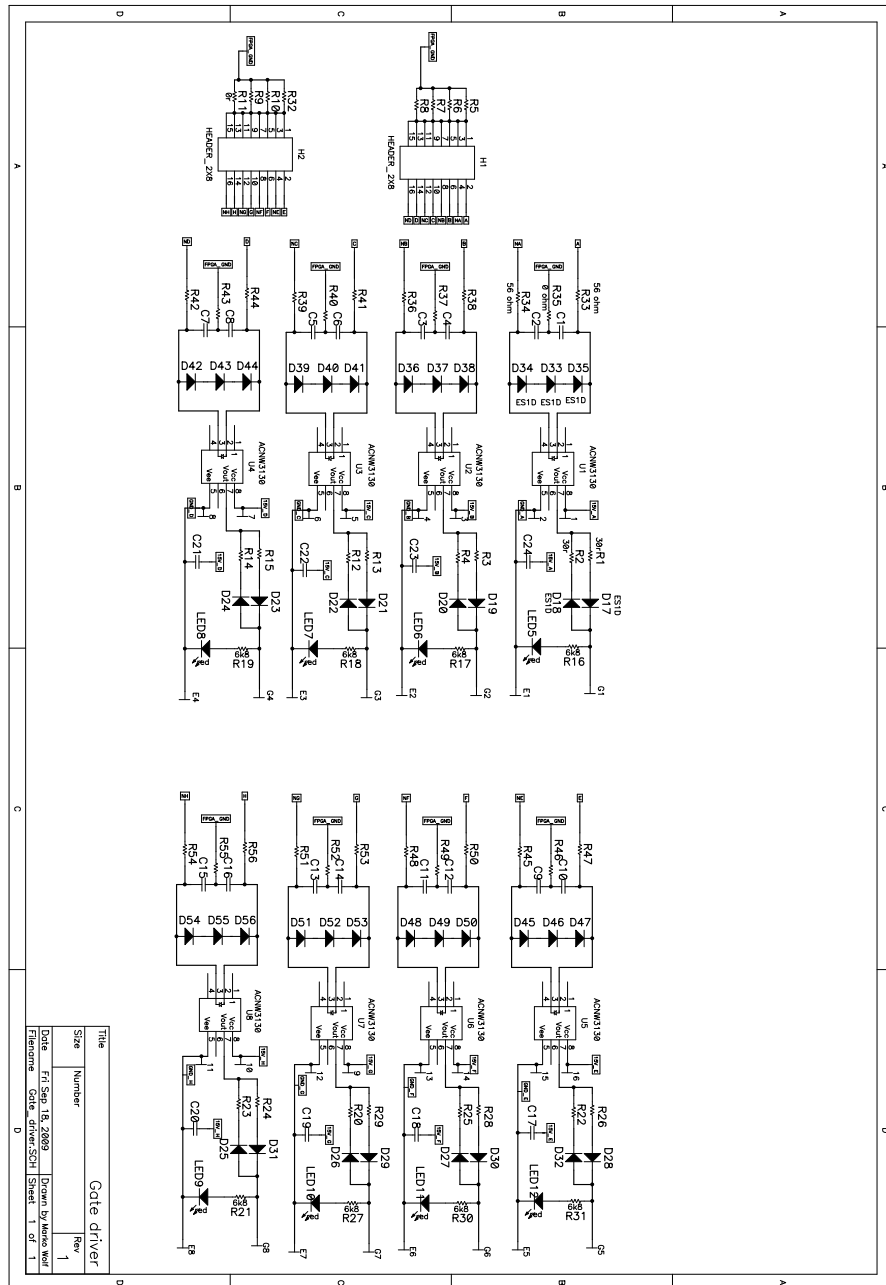


Figure C.1: Gate driver schematic

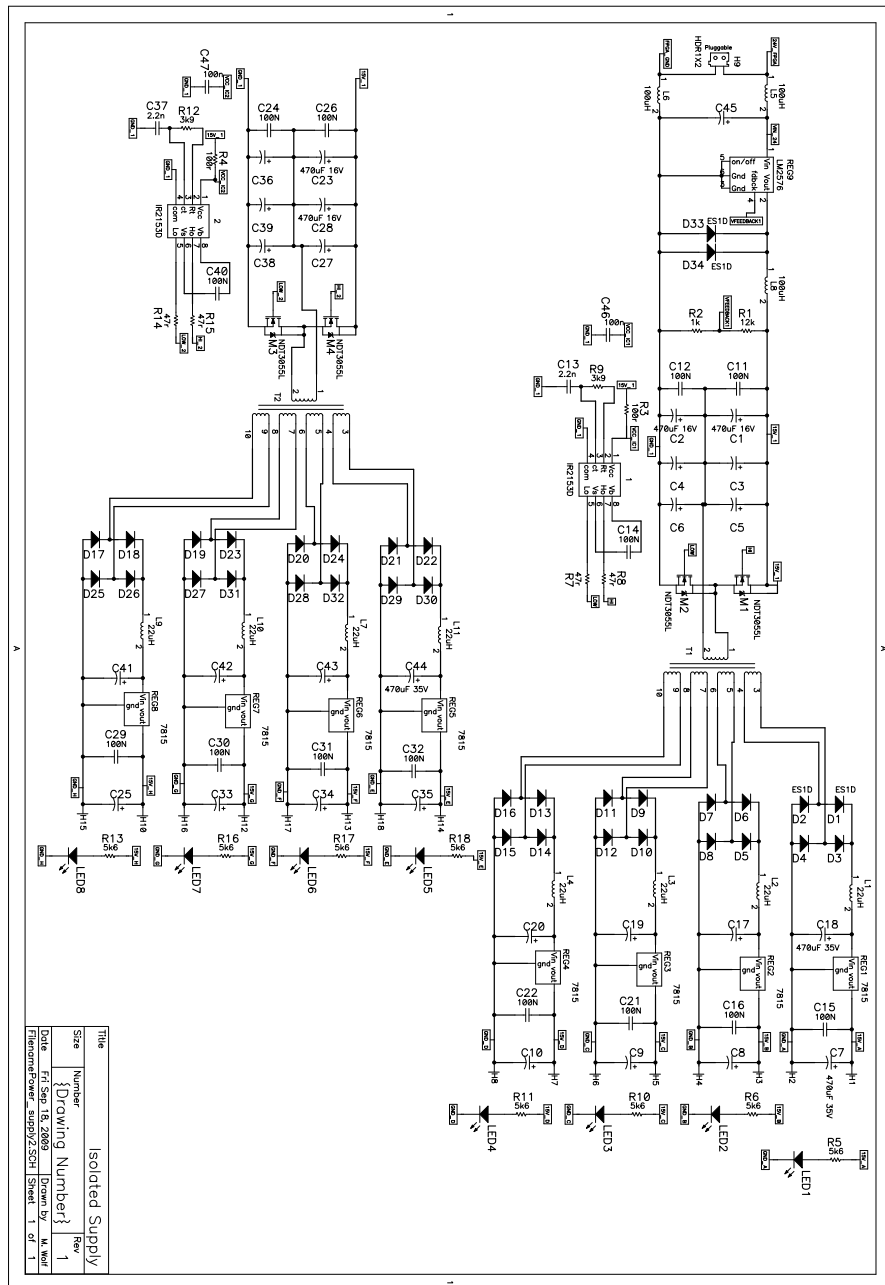


Figure C.2: Isolated supply schematic

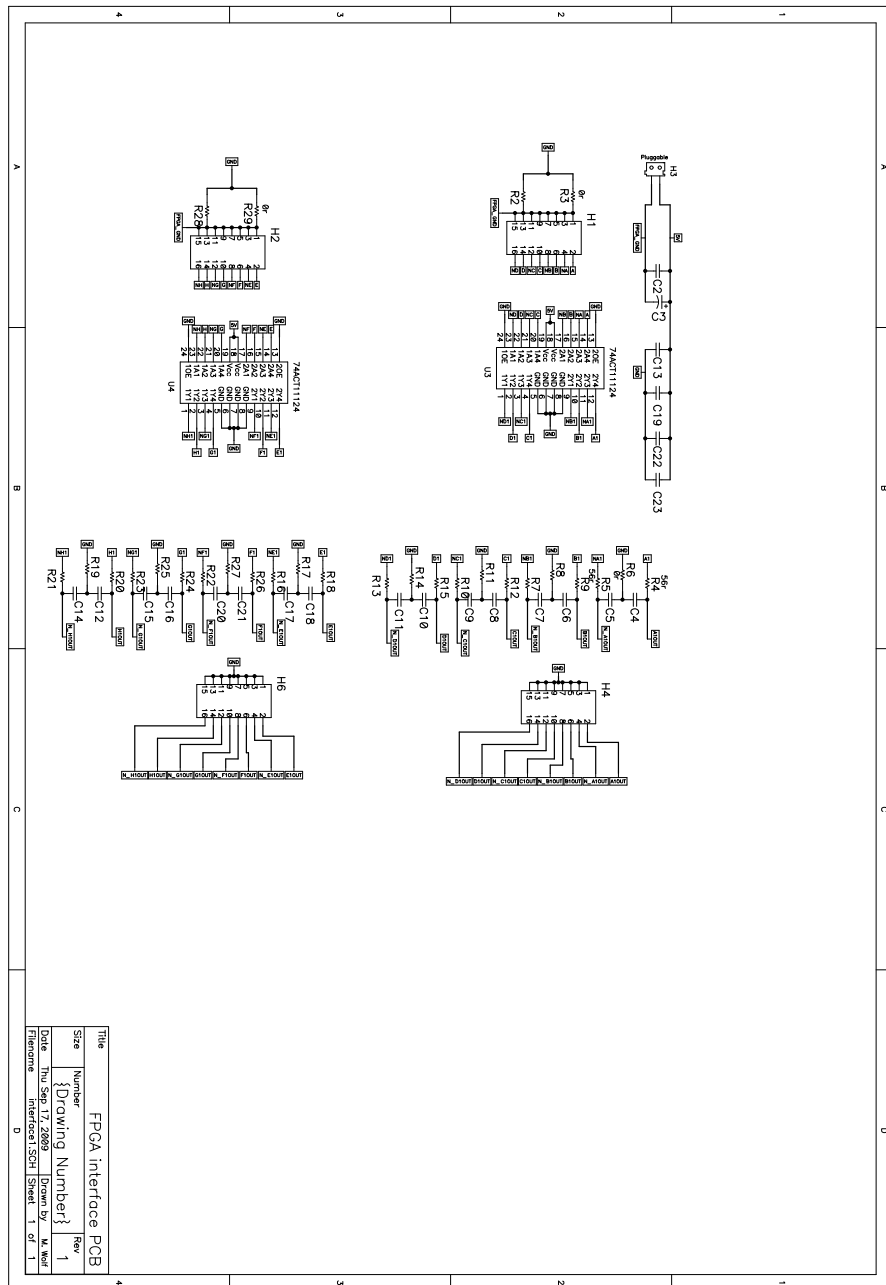


Figure C.3: FPGA interface schematic

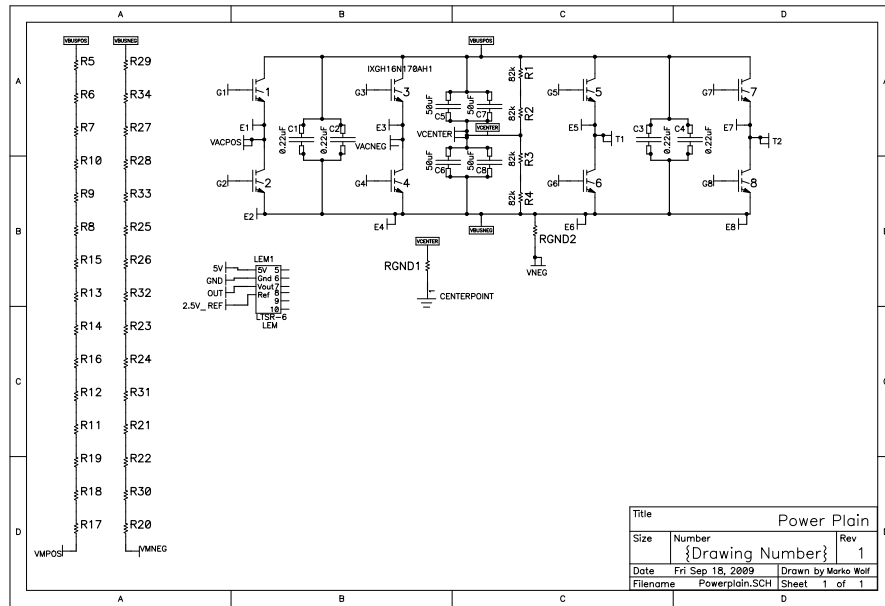


Figure C.4: Power plain schematic

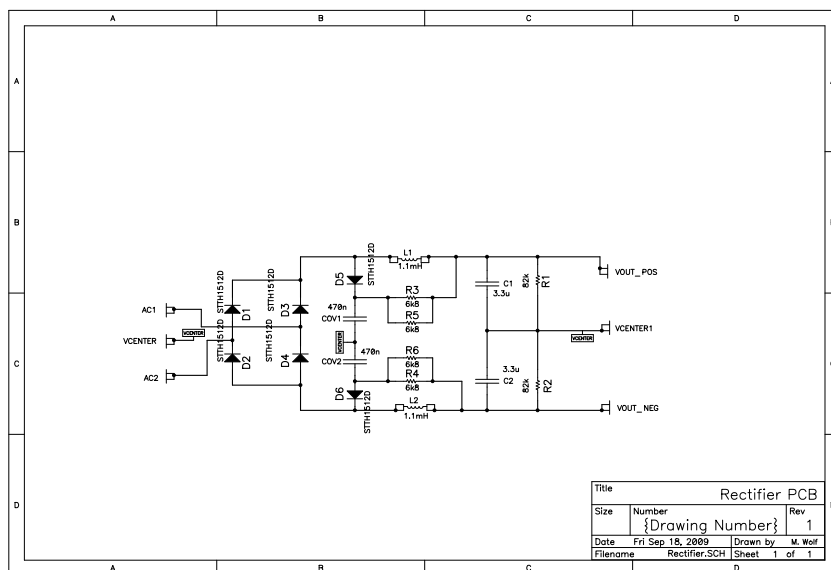


Figure C.5: Rectifier schematic (Revision 1)

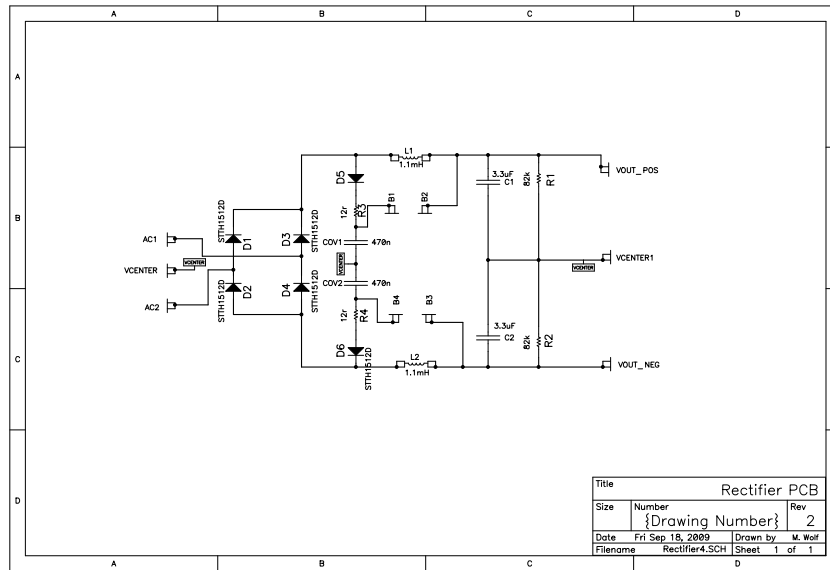


Figure C.6: Rectifier schematic (Revision 2)

### C.2.1 Measurement Board for the DC-AC Inverter

The schematic of the measurement PCB used in the three phase DC-AC inverter is shown in Figure C.7. The measurements that were required for this PCB are as follows:

- 3 phase voltages, namely  $v_a, v_b, v_c$
- 3 inductor currents, namely  $i_{L_a}, i_{L_b}, i_{L_c}$
- 2  $\frac{V_{DC}}{2}$  measurements of the bus voltage

A photograph of the measurement PCB is shown in Figure C.8, the relevant measurement parameters are also indicated on this photograph. The errors of this PCB were:

- Instrumentation opamp U14, pin no 8 is required to be connected to the 15 V supply.

The ICs, namely U6, U8, U10, U12, U13 are instrumentation opamps (INA 128). The ICs, namely U1-U5, U7, U9, U11 and U14 are standard dual rail operational amplifiers (LF353).



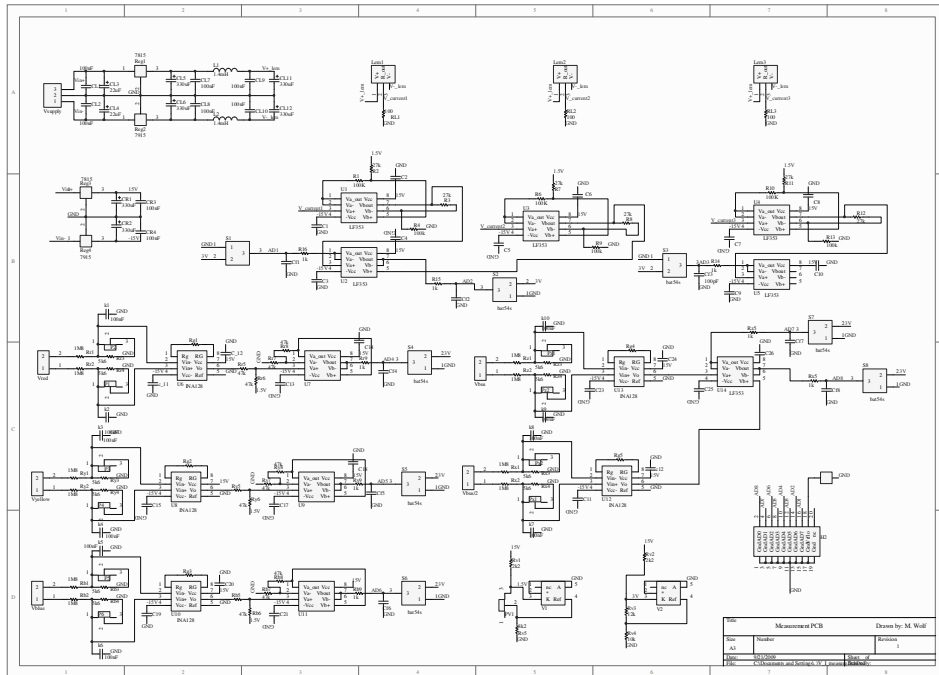


Figure C.7: Measurement PCB schematic

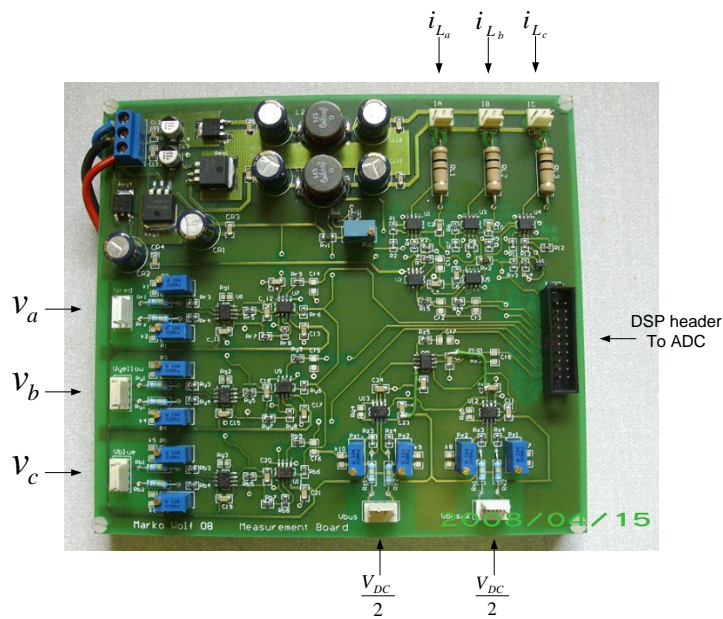


Figure C.8: Photo of the measurement board

### C.2.2 Optic Driver Circuit for the DC-AC inverter

The schematic of the optic gate driver circuit is shown in Figure C.9. A photograph of this PCB is shown in Figure C.10. The PCB consists of 6 TX signals which are used for the PWM gate signals. Six Rx fault signals are included for the IGBT fault signals. The mosfets used on this PCB were the 2N7000. The optic transmitters and receivers were the HFBR1521 and HFBR2521 respectively.

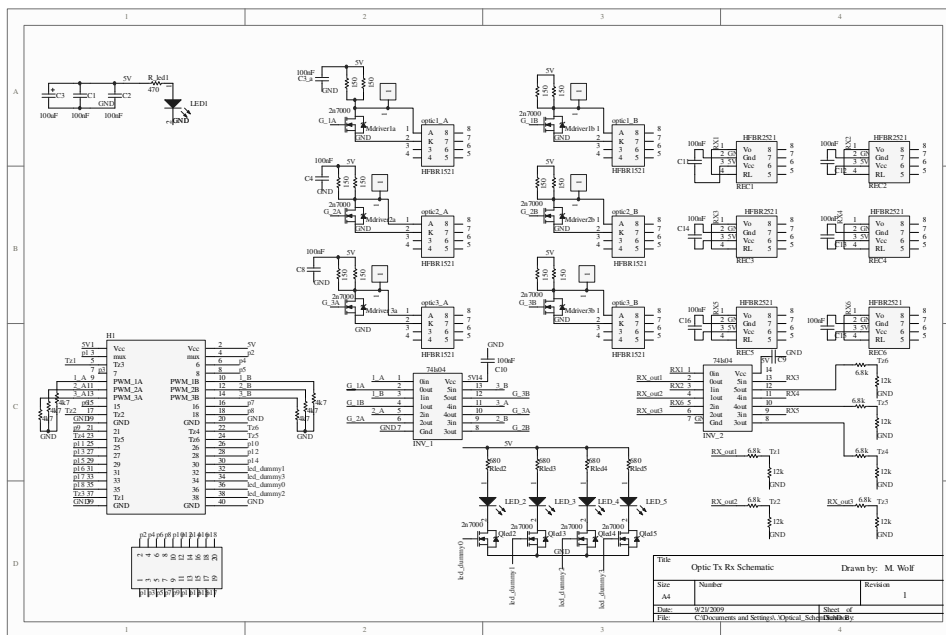


Figure C.9: Optic driver schematic

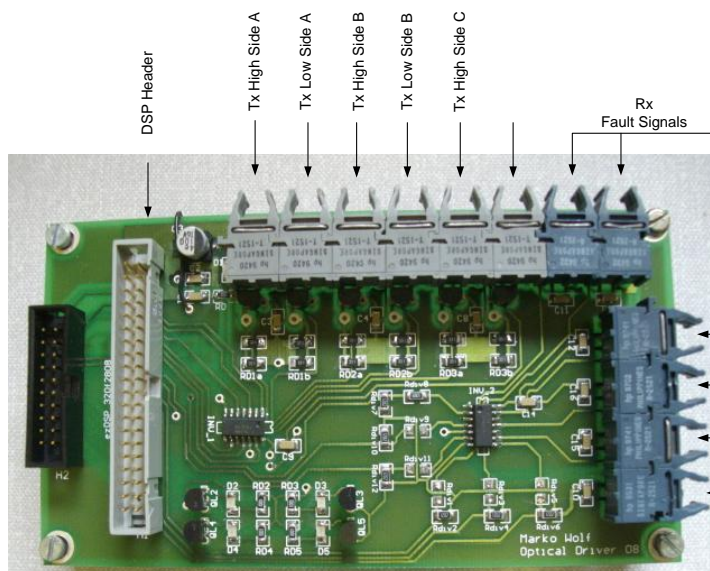


Figure C.10: Optic driver photograph

# Appendix D

## Power Quality

This appendix briefly discusses the components in the system that cause the power quality to deteriorate. This information is obtained from [14; 17]

### D.1 Harmonics

Through the study of heat flow in a rod, the French mathematician Joseph Fourier discovered that a periodic function can be written as a trigonometric series [50]. Thus through using the Fourier series any voltage or current waveform is separated into the specific harmonics.

Non-sinusoidal currents that are drawn from any load produces a non-sinusoidal voltage drop across the impedances of the system. This in effect distorts the voltage of the system. Harmonics cause additional losses and in effect increase the temperature of certain components. Thus harmonics should be taken into account when designing a power system, for example cables should be de-rated and maximum device temperature should be considered.

Power systems are affected by harmonics because the skin effect increases the impedances of the system at higher frequencies. The  $I^2R$  losses occurring in a transformer make up 75-85% of the total losses, of these losses roughly 75% are frequency independent. The remainder is proportional to the frequency squared. The no-load losses are therefore 15-25% of the total losses and increase as the frequency increases to a factor between  $f^{1.5} - f^3$ , depending on the flux in the core.

The NRS 048-2:2004 is a document that specifies voltage quality parameters and specific compatibility levels of the supply voltage in South Africa. This document specifies that the total harmonic distortion (THD) up to the 40<sup>th</sup> harmonic, should not exceed 8% in medium or low voltage supplies.

### D.2 Over Voltages

Over voltages are caused when the rms AC voltage is over the 1.15 p.u. Over voltages could be caused by capacitor banks being switched on, or large loads being switched off or the unlikely event of a transformer tap setting being set incorrectly.

### D.3 Voltage Swell

A swell is an increase of the system voltage for a few cycles, causes of this is a possible load being switched off or a capacitor bank being energized. Another possibility of a swell is the single phase to ground fault

where the other two phases voltages increase until the protection devices operate. Voltage dip is the exact opposite of a swell.

## D.4 Voltage Surges

Surges are an increase in the voltage for a small duration of a cycle, in the order of milli-seconds. The NRS-048 describes these as rapid voltage changes. These surges can be caused from a switching transient for example the magnetization winding in a transformer. Should the transformer supply be interrupted, the magnetization current is therefore forced to zero. The voltage would be proportional to:

$$v = L \frac{di}{dt} \tag{D.1}$$

## D.5 Network Transients

Undesired network transients are normally oscillatory conditions on a power system that will eventually stabilize. These faults are therefore classified as temporary faults. Transients can be caused by a large number of occurrences, for example lightning striking a transmission line which causes a temporary over-voltage, or a large load being switched on causing a voltage dip.

## D.6 Flicker

The amount of disturbances the human eye notices by irregular flashing of light is described as flicker. The fluctuation in lumen is caused by voltage fluctuations appearing across the lights, these disturbances usually are in the order of 6-8 Hz. This frequency is noticeable and irritating to the human eye. Flicker is caused by continuous or random voltage changes, the output voltage is modulated by a lower frequency that is perceptible to the human eye. Loads that change quickly and continuously can be the cause of flicker, an example of this is the electric arc furnace.

## D.7 Long-term Interruptions

Long term interruptions are caused by significant faults in the system. These faults are then isolated from the network by the protection devices in the network. The NRS-048 specifies the type of interruption depending on the voltage level. For example in the case of HV/LV systems a momentary interruption is when the supply is interrupted for more than 3 seconds but less than 5 minutes. Sustained interruptions are those that persist longer than 5 minutes.

## D.8 Spectral Distortion

Distortion is classified as the deviation of the output waveform from a pure sinusoidal waveform at the specific frequency. Distortion can be caused by harmonics, noise or a possible DC offset. A DC offset is detrimental to a power system as this introduces a DC offset into the B-H curve of all the transformers. The transformer core could eventually saturate depending on the severity of the DC offset. This occurs because the flux density drifts further and further away from the origin of the BH curve [14]. The saturation of the core however prevents the continuous saturation as the BH curve eventually stabilizes. Simply put, the flux density can not increase to infinity.

## D.9 Power Frequency Variations

The deviation in frequency from the required frequency namely 50 Hz is considered as a power frequency variation. This phenomena is caused by instability between the generators and the load. The mechanical power  $P_m$  is equal to the electrical power  $P_e$  in the steady state operation of a generator. Should a large load suddenly be disconnected from the generator due to a fault on the transmission feeder, the electrical power  $P_e$  decreases. The mechanical power and the inertia of the rotor cannot change instantaneously, therefore the rotor will start to accelerate. This causes the electrical frequency of the generator to increase. The NRS-048 specifies that the frequency compatibility level should be within  $\pm 2\%$ , which is a fluctuation of 1Hz.

# Appendix E

## Cell Manufacturing Information

### E.1 Filter Inductor Manufacturing

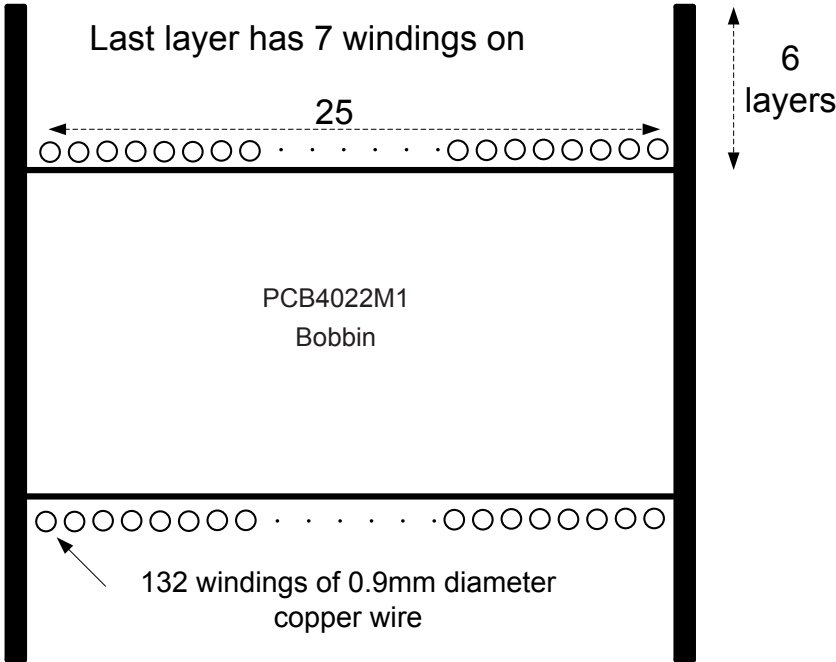


Figure E.1: Filter inductor winding layout

### E.2 Cell Construction

In the event of replacing the IGBTs:

1. Remove back-to-back converter from the wooden base plat.
2. Loosen the fan cover.
3. Remove the FPGA PCB, isolated supply PCB and gate driver PCB.
4. Loosen the heatsink from the aluminium base plate.

5. Loosen the bottom IGBT mounting plates as well as the top IGBT mounting plates.
6. Separate the heatsink from the power plane PCB.
7. Replace the IGBTs: Apply heatsink paste as well as the back washers of the IGBTs, **note do not solder the IGBTs at this stage.**
8. Loosen IGBT mountings sufficiently that they can rotate.
9. Place power plane PCB with IGBTs to the left of the IGBT mountings, see Figure E.2.
10. Shift the power plane as well as the IGBTs to the right, the IGBT mounting plates will shift over the IGBTs.
11. Fasten the bottom IGBT mounting plates and then the top IGBT mounting plates.
12. Solder the IGBTs on the top side of the power plane PCB.
13. Re-assemble the back-to-back converter.

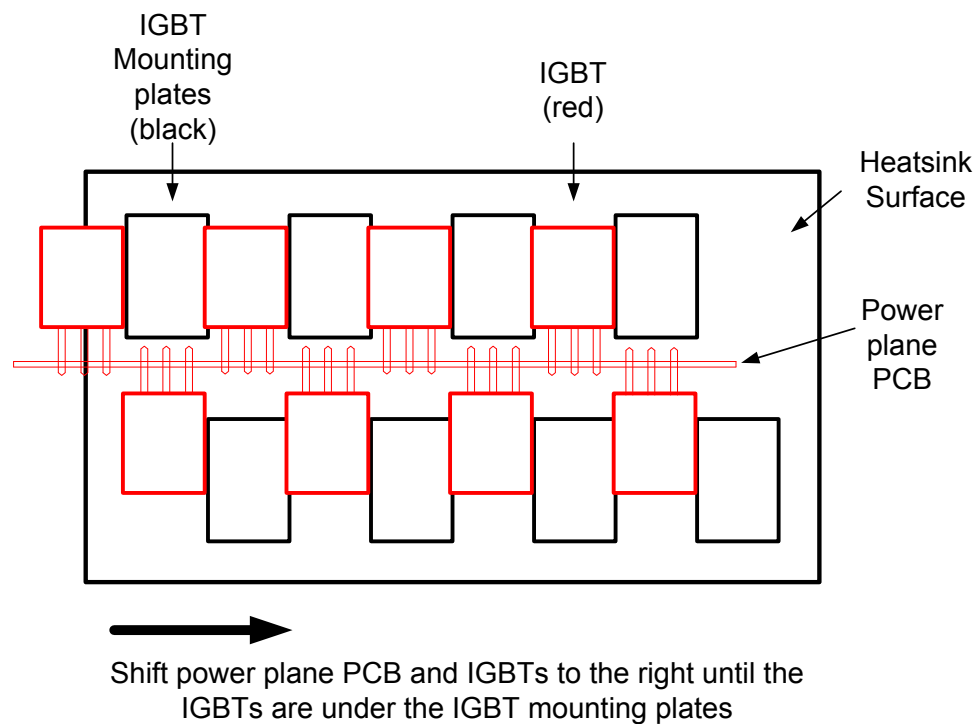


Figure E.2: IGBT mounting procedure