

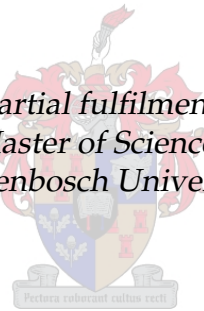


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A Low Noise PLL-Based Frequency Synthesiser For X-Band Radar

Henderikus Jan Moes

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for the degree of Master of Science in Engineering at
Stellenbosch University*



Supervisors:

Prof. J.B. de Swardt Prof. P.W. van der Walt

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Declaration

I, the undersigned, hereby declare that the work contained in this thesis is my own original work and that I have not previously in its entirety or in part submitted it at any university for a degree.

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H.J. Moes

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Abstract

This thesis discusses the design, development and measured results of a phase-locked loop based frequency synthesiser for X-band Doppler radar. The objective is to obtain phase noise comparable or lower than that typically achieved with direct analogue frequency synthesis techniques. To meet this objective, a theoretical study of the noise contributions of individual components of the synthesiser and their effect on the total phase noise within and outside the loop bandwidth of the PLL is performed. The effect of different phase margins on the closed-loop frequency response of the PLL, and hence the total phase noise, is investigated. Based on the results, an optimal phase-frequency detector reference frequency, loop bandwidth, adequate phase margin, and suitable components are chosen for optimal phase noise performance. The total phase noise at the output of the synthesiser is calculated and it is shown that the phase noise specification can be met.

A significant part of this thesis is devoted to the design, modelling and characterisation of a frequency multiplier, as well as to a combine and interdigital bandpass filter required for the frequency synthesiser. In the first case, a piecewise linear circuit model is used to model the behaviour of the nonlinear multiplier circuit. Fourier theory is used to calculate the large-signal driving point input and output impedances of the nonlinear circuit, enabling the computation of the circuit elements for the input and output matching networks. The measured response of the frequency multiplier under various different operating conditions is presented and discussed. The design of the microwave bandpass filters is based on the theory of coupling and external quality factors. To aid in the verification and optimisation of the design, a software simulation tool is used. The presented S-parameter measurements of the filters show how well the theory matches with what is obtained in practice.

The measured spectral and phase noise response of various components comprising the synthesiser, are discussed. These measurements provide insight into the response of individual components under different operating conditions and show the behaviour of important subsystems of the synthesiser. The thesis culminates in the presentation of the measured phase noise of the complete synthesiser. It is shown how well the measured phase noise correlates with the calculated phase noise. In addition, the measured spectral content and transient behaviour of the synthesiser are investigated and discussed. High power spurious components at some output frequencies are identified and reduced. The feasibility of using the developed prototype phase-locked loop based frequency synthesiser for coherent X-band Doppler radar is discussed and demonstrated.

Opsomming

Die ontwerp, ontwikkeling en gemete resultate van 'n fasesluitlus gebaseerde frekwensie sintetiseerder vir X-band Doppler radar, word bespreek. Die doelstelling is om faseruis wat vergelykend of laer is as wat tipies met direkte analoog frekwensie sintese behaal word, te verkry. Vir hierdie doel word 'n teoretiese studie van al die ruis bydraes van verskillende komponente van die sintetiseerder, en die invloed van elkeen binne en buite die lusbandwydte van die fasesluitlus, gedoen. Die effek van verskillende fasegrense op die geslotelus frekwensie weergawe van die fasesluitlus en gevolglik op die totale faseruis, word ondersoek. Op grond van die resultate word 'n optimale fase-frekwensie detektor vergelykings frekwensie, lusbandwydte, geskikte fasegrens en komponente gekies vir optimale faseruis gedrag. Die totale faseruis by die uittree van die sintetiseerder word bereken en daar word aangetoon dat die faseruis spesifikasie behaal kan word.

'n Beduidende deel van die tesis is gewy aan die ontwerp, modellering en karakterisering van 'n frekwensie vermenigvuldiger en aan 'n kamlyn en interdigitaal banddeurlaat filter wat vir die sintetiseerder benodig word. Vir die vermenigvuldiger word 'n stuksgewys lineêre stroombaan model gebruik om die nie-lineêre gedrag van die vermenigvuldiger te modelleer. Fourier teorie word gebruik om die grootsein in- en uittree impedansies van die nie-lineêre baan te bereken, wat gevolglik die berekening van die stroombaan elemente van die aanpassingsnetwerke toelaat. Die gemete resultate van die vermenigvuldiger onder 'n aantal verskillende kondisies word gegee en bespreek. Die ontwerp van die mikrogolf banddeurlaat filters is gebaseer op die teorie van koppeling en eksterne kwaliteits faktore. 'n Sigteware pakket word gebruik om die ontwerp te verifieer en te optimaliseer. Die gemete S-parameters van die filters word bespreek en daar word aangetoon hoe goed die teorie met die praktyk vergelyk.

Die gemete spektrale en faseruis resultate van 'n verskeidenheid komponente van die sintetiseerder word bespreek. Die metings gee insig in die gedrag van individuele komponente onder verskillende kondisies en dui die gedrag van belangrike substelsels van die sintetiseerder aan. Die tesis bereik sy hoogtepunt met die aanbieding van die totale gemete faseruis van die sintetiseerder. Daar word aangetoon hoe goed die teoretiese voorspelling met die gemete faseruis ooreenstem. Die spektrale en tydgebied gedrag van die sintetiseerder word ook ondersoek en bespreek. Hoë drywing stuurseine by sommige uittree frekwensies word identifiseer en verminder. Die geskiktheid van die ontwikkelde prototipe sintetiseerder vir koherente X-band Doppler radar word bespreek en aangetoon.

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List of Abbreviations

AC	Alternating Current
AM	Amplitude Modulation
BER	Bit Error Rate
CP	Charge Pump
DAC	Digital-to-Analogue Converter
DC	Direct Current
DDS	Direct Digital Synthesis(er)
DUT	Device Under Test
FET	Field-Effect Transistor
FM	Frequency Modulation
FTW	Frequency Tuning Word
IC	Integrated Circuit
IM	Intermodulation
LO	Local Oscillator
LSB	Lower Sideband
OCXO	Oven-Controlled Crystal Oscillator
PCB	Printed Circuit Board
PFD	Phase-Frequency Detector

PLL	Phase-Locked Loop
PM	Phase Modulation
RADAR	Radio Detection and Ranging
RBW	Resolution Bandwidth
RF	Radio Frequency
RMS	Root Mean Square
SFDR	Spurious-Free Dynamic Range
SMA	SubMiniature Version A
SRD	Step-Recovery Diode
SSB	Single-Sideband
TEM	Transverse Electromagnetic
USB	Upper Sideband
VBW	Video Bandwidth
VCO	Voltage-Controlled Oscillator
VNA	Vector Network Analyser

Chapter 1

Introduction

1.1 A Brief Overview of Frequency Synthesis and Phase-Locked Loops

Frequency synthesis, especially the digital part of it, has experienced major advancement and growth during the last couple of years. In the not too distant past, the use of frequency synthesis was limited to the more complex and demanding applications [1]. Today, frequency synthesis is ubiquitous and it is utilised in a large number of applications ranging from medical imaging, radar and test instrumentation, to virtually every type of communications and storage device. A large driving force behind its widespread use was the early demand for communication within a limited bandwidth which has led to rapid development in the field [2].

Kroupa defines frequency synthesis as the frequency changing process whereby a new frequency is derived from a given fundamental frequency by combinations of several additions, subtractions, multiplications and divisions [3]. The term was invented during the early 1940s when the first measurement devices were developed. The variable output frequency of these measurement instruments was harmonically related to a submultiple of the reference frequency [4].

The development in the field of frequency synthesis has led to the three main frequency synthesis methods we know today namely, direct digital synthesis (DDS), direct (analogue) frequency synthesis, and indirect or phase-locked frequency synthesis [1, 5, 6].

The concept of the phase-locked loop (PLL) can be traced back to as early as 1919. Vincent and Appleton experimented and analysed, respectively, the practical synchronisation of oscillators [7, 8]. After these initial papers, research and development continued until the 1940s. Around that time, the initial interest in synchronisation was for a local oscillator in frequency modulation (FM) demodulation and the exciter for an atomic particle accelerator amplifier [9]. An early description of phase-lock was published by French scientist de Bellescize in 1932 [10].

The first widespread use of PLLs was in the synchronisation of horizontal and vertical scan in television receivers [11]. Colour television would not have been possible without the advancement in PLL technology. In 1954, Richman published a paper in which he developed equations describing the acquisition time for a first-order PLL used in colour television [12]. Spaceflight requirements also inspired intensive application of phase-lock methods and space use of PLLs began with the launching of the first American artificial satellites [10].

The first divide-by-N PLL synthesiser became practical with the advent of small-scale digital integrated circuits (ICs) in the middle 1960s [2]. The availability of PLL ICs facilitated the rapid introduction of PLLs into consumer products. Today, PLLs are used in applications such as frequency synthesis, data and clock recovery, and frequency demodulation. The list is not nearly all inclusive.

Frequency synthesis is still going through an evolutionary period today. It has received much attention from IC manufacturers, and a great variety of PLL and DDS ICs have been available for several years. The continuous improvement of these ICs enables the designer to develop high quality frequency synthesisers that comply with the most stringent requirements of modern systems.

1.2 Project Background and Motivation

The rapid development in PLL and DDS technology has opened doors in terms of frequency synthesiser design. As a result of this advancement, many complex synthesisers can now be replaced with smaller, simpler, lower power frequency synthesisers at a fraction of the cost.

Direct (analogue) synthesisers, which still find use in many radars today, employ multiplication, mixing, division and filtering to generate a desired signal frequency from a single reference, and do not make use of feedback as compared to PLL synthesisers [5]. Direct synthesisers offer great advantages such as fast switching speed and low phase noise. On the other hand however, they tend to be complex and expensive, especially when wide frequency coverage with fine resolution is required [6]. The recent advancement in PLL technology has made it possible that indirect synthesisers can in many instances be developed with comparable phase noise performance to that of direct synthesisers, at the same time reducing size, simplifying the architecture, driving down cost and power consumption.

A major breakthrough in low noise PLL synthesiser design came with the recent appearance of the HMC439QS16G low noise phase-frequency detector (PFD) from *Hittite*. The PFD is able to operate with input reference frequencies up to 1.3 GHz, greatly reducing the required frequency divider value in the feedback path of the PLL, in turn reducing the in-band phase noise of the frequency synthesiser. The effect of the PFD and the frequency divider on the phase noise of a PLL is discussed in the next chapter.

Another *Hittite* component which contributes in simplifying the architecture of the synthesiser discussed in this text, is the HMC586LC4B voltage-controlled oscillator (VCO) which appeared on the market quite recently. It offers low phase noise, wide tuning range and high frequency of operation, eliminating the need of using additional frequency multipliers to obtain the desired output frequency.

This thesis focuses on the exploitation of recent advancement in PLL and DDS technology to design, develop and test a PLL-based frequency synthesiser that can be used as a local oscillator (LO) stage for coherent X-band Doppler radar. Since coherent Doppler radar requires very phase stable LOs, the primary objective is to obtain phase noise comparable or lower than that typically achieved with current direct frequency synthesis techniques.

Table 1.1 shows a typical electrical specification of an LO used for X-band Doppler radar.

Table 1.1: Typical local oscillator specification.

Parameter	Specification	
Output Frequency	5.47 - 7.47 GHz	
Output Power	10 dBm \pm 2.5 dB	
Frequency Resolution	\leq 1 MHz	
Switching Speed	\leq 1 μ s	
Spurious Outputs	-50 dBc Maximum	
Harmonics	-50 dBc Maximum	
Single-Sideband Phase Noise	100 Hz	\leq -80 dBc/Hz
	1 kHz	\leq -105 dBc/Hz
	10 kHz	\leq -118 dBc/Hz
	100 kHz	\leq -118 dBc/Hz
	1 MHz	\leq -118 dBc/Hz
	10 MHz	\leq -130 dBc/Hz

The goal of this study project is to investigate and demonstrate the possibility of meeting the phase noise specification with a PLL-based frequency synthesiser. In addition, the other specifications listed in Table 1.1 are also investigated and evaluated.

1.3 Organisation of Thesis

For all the chapters following Chapter 2, preliminary theoretical knowledge of basic noise and PLLs is assumed. For this reason, Chapter 2 is a theoretical chapter devoted to a discussion of relevant noise and PLL theory, covering all the concepts required to understand the application in the rest of this thesis. Chapter 3 serves as an introduction to the proposed indirect frequency synthesiser which is given in block diagram form. The synthesiser architecture is discussed in detail and the reasoning behind some of the choices of components is explained and motivated.

Chapter 4 describes the design and measured response of a step-recovery diode (SRD) frequency multiplier which is used to increase the frequency of the reference oscillator used for the synthesiser.

Chapter 5 outlines the theory, design, software modelling, optimisation and measured response of two microwave bandpass filters required for the frequency synthesiser.

Chapter 6 describes the design of the synthesiser for optimal phase noise performance. Numerous transfer functions required for the calculation of the phase noise, are derived. These transfer functions, together with the noise information of the individual components of the frequency synthesiser, are then used to compute the total phase noise at the output of the synthesiser. In the final part of the chapter, the estimated power levels at several stages of the synthesiser are given.

The measured response of several components of the synthesiser is discussed in Chapter 7. Chapter 8 is dedicated to a discussion of the measured phase noise, spectral purity, and transient response of the synthesiser. The measured phase noise is compared to the phase noise calculated in Chapter 6 and it is shown how well theory matches with what is obtained in practice. Chapter 9 concludes this thesis by objectively reflecting on the completed work and by presenting suggestions for future development.

Chapter 2

Background Theory

2.1 Introduction

This chapter covers background theory required for understanding the application of numerous theoretical concepts in the chapters that follow. The chapter starts off with a discussion of noise theory relevant to this thesis. The final part of this chapter is devoted to a discussion of basic PLL theory.

2.2 Types of Noise

Noise, as broadly defined by Motchenbacher *et al.*, is any unwanted disturbance that obscures or interferes with a desired signal. The effect of noise, which is inherent to all electrical systems, is critically important in the performance of most RF and microwave communications, radar and remote sensing systems, because it sets a limit on the dynamic range of a system. System noise is a result of internally generated noise, as well as noise entering the system from external sources. In either case, the noise level places a limit on the minimum signal power that can be detected [13, 14, 15].

2.2.1 Thermal Noise

Thermal noise, also known as Johnson or Nyquist noise, is the most commonly encountered noise and is caused by the random motion of charge carriers in a conducting medium whose temperature is above absolute zero [6, 15, 16].

A resistor is a source of thermal noise, and can be represented by either equivalent noise circuits shown in Figure 2.1. The electrons in the resistor are in random motion, with a kinetic energy proportional to the temperature. The random motion of these charge carriers produces small voltage fluctuations across its terminals. The mean value of this voltage is zero, but the nonzero *root mean*

square (RMS) noise voltage is given by [6, 15, 16]

$$V_n = \sqrt{4kTB R} \quad (2.1)$$

where

$k = 1.38 \times 10^{-23} \text{ J/}^\circ\text{K}$ is Boltzmann's constant

T is the temperature, in degrees Kelvin (K)

B is the bandwidth in Hz

R is the resistance in Ω

Equation 2.1 is known as the *Rayleigh-Jeans* approximation, and is the expression most commonly used in microwave work [13]. It follows that the mean-squared noise voltage, expressed in per unit of bandwidth, is given by

$$S(f) = \frac{V_n^2}{B} = 4kTR \quad \left[\text{V}^2/\text{Hz} \right] \quad (2.2)$$

which has units V^2/Hz . Equation 2.2 represents the spectral density of thermal noise. The spectral density has a flat frequency response, that is, it is frequency independent. For this reason, thermal noise is often referred to as white noise, which is in analogy with white light which is composed of all colours of the visible light spectrum [15].

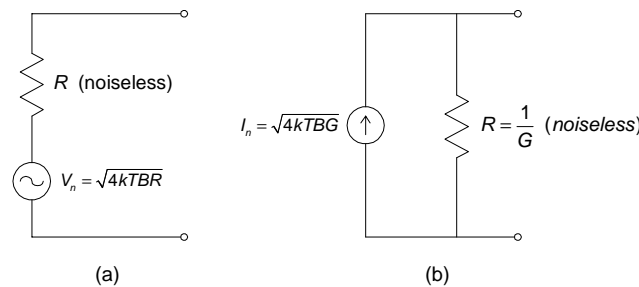


Figure 2.1: Equivalent (a) Thevenin and (b) Norton circuits representing thermal noise in a resistor.

When a load resistor R is connected to the circuit shown in Figure 2.1(a), maximum power transfer occurs. In this case, the power delivered to the load is equal to

$$P_n = \left(\frac{V_n}{2} \right)^2 \frac{1}{R} = kTB \quad (2.3)$$

where the $\frac{1}{2}$ term is a result of voltage division between the source and load resistance. Note that the noise power is independent of R . It is also interesting to note that the noise power decreases as the bandwidth and temperature decreases. Thus, although thermal noise cannot be eliminated, it can be minimised [13].

The available noise power from a resistor in a 1 Hz bandwidth at room temperature (290°K), is calculated as

$$10 \log_{10}(kTB) = 10 \log_{10}(1.38 \times 10^{-23} (290) 1) = -203.98 \text{ dB} = -173.98 \text{ dBm} \quad (2.4)$$

When sinusoidal signal voltage sources of the same amplitude and frequency are connected in series, the resultant signal amplitude is twice that of one individual source, given that they are in phase. Combined, they can deliver four times the power of one source. If, on the other hand, the sources are 180° out of phase, the net voltage and power is zero. For other phase relationships, they may be combined using the rules of phasor algebra [15].

When two sinusoidal signal voltage sources of different frequencies with RMS amplitudes V_1 and V_2 are connected in series, the resultant RMS voltage is equal to $V_R = \sqrt{V_1^2 + V_2^2}$. It follows that the mean-squared amplitude of the resultant signal is equal to

$$V_R^2 = V_1^2 + V_2^2 \quad (2.5)$$

When independent or uncorrelated noise sources are connected in series, the output power is the sum of the separate source powers. Consequently, it is valid to combine such sources so that the resultant mean-square voltage is equal to the sum of the mean-square voltages of the individual sources. White noise sources are uncorrelated by definition and can be treated similarly [14, 15].

2.2.2 Shot Noise

Shot noise is observed in diodes, transistors and tubes, and is associated with current flow across a potential barrier. Such a barrier exists at every *pn*-junction in semiconductor devices and at the cathode surface in a vacuum tube. The current flow in these devices is not smooth and continuous, but rather is the sum of pulses of current caused by the random emission of charge carriers from the cathode or emitter region, fluctuating statistically from instant to instant [15, 16].

In 1918, Schottky showed that the mean-square current fluctuation is given by [14, 17]

$$i_n^2 = 2qI_{DC}B \quad (2.6)$$

where

q is the electron charge (1.6×10^{-19} C)

I_{DC} is the DC current in A

B is the bandwidth in Hz

Therefore, the spectral density of shot noise can be expressed as

$$S(f) = \frac{i_n^2}{B} = 2qI_{DC} \quad \left[\text{A}^2/\text{Hz} \right] \quad (2.7)$$

As with thermal noise, the amplitude distribution of shot noise is Gaussian, while the spectral distribution is independent of frequency [17].

2.2.3 Flicker Noise

A third commonly observed Gaussian amplitude distribution noise is flicker noise, also referred to as excess, contact or $1/f$ noise. It is observed in vacuum tubes, transistors, diodes, and resistors, but is also present in thermistors, carbon microphones, thin films and light sources [15].

Flicker noise is characterised by a spectral density that increases with decreasing frequency. The spectral density is of the form

$$S(f) = \frac{c}{f^\alpha} \quad 0.8 \leq \alpha \leq 1.5 \quad (2.8)$$

where c is a constant. The physical mechanism that gives rise to flicker noise is not well understood, but it is associated with contact and surface irregularities in semiconductors and appears to be caused by fluctuations in the conductivity of the medium [14, 17].

2.2.4 Phase Noise

The concept of having perfect periodic sinusoidal signals is convenient for modelling and analysis, but is erroneous in principle since in practice no deterministic signals exist. Recall from Fourier theory that a sinusoidal signal, $A \sin(2\pi f_0 t)$, is represented by an impulse function in the frequency domain. Thus, when such a signal is displayed on a spectrum analyser, one would expect to see a single tone at f_0 . In practice however, the spectral line has finite width, and noise power appears as a continuous distribution localised around the carrier frequency f_0 . The spread of noise power around the carrier is a result of both amplitude and phase noise modulating the signal in a random fashion, creating what can be considered a large number of sidebands. A sinusoidal signal with phase noise, as seen on a spectrum analyser, typically takes the form of that depicted in Figure 2.2 [1, 18].

Phase noise is a means of characterising the short-term stability of a signal. Short-term stability extends between a fraction of a second to 1 s, or in some cases up to 1 minute. For longer time scales, stability is referred to as aging or long-term stability [19].

Phase noise is often specified as an integrated number in RMS degrees or radians, or given as the ratio of the single-sideband (SSB) noise power in a 1 Hz bandwidth, to the total signal power, plotted versus the offset frequency from the carrier. This is illustrated in Figure 2.3. The related phenomenon of phase noise observed in the time domain is commonly referred to as *jitter*, and describes the

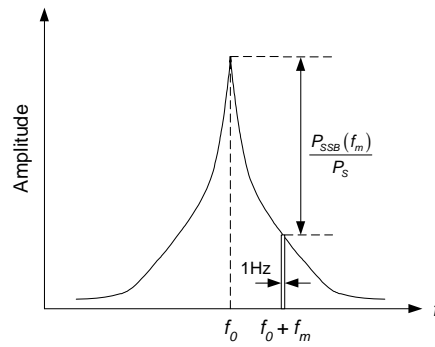


Figure 2.2: Spectrum analyser display of phase noise.

variation in the zero crossings of a signal [17, 18, 19].

Phase noise is very important in communications and radar systems. It causes problems such as reciprocal mixing, requiring the need for increased channel spacings, and causes increased bit error rates (BERs) and synchronisation problems in digital systems. Phase noise furthermore causes an error in the Doppler frequency of Doppler radars, resulting in radial velocity errors of moving targets. The problem becomes more pronounced for targets that have slow radial velocities, producing small Doppler shifts [20].

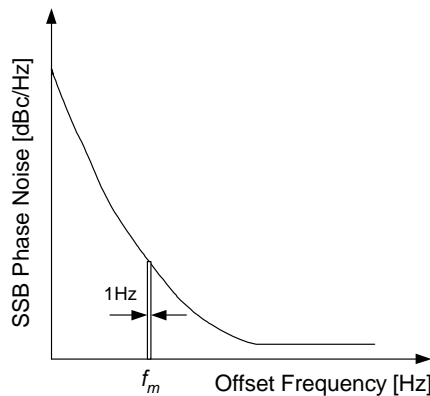


Figure 2.3: SSB phase noise as a function of offset frequency from the carrier.

A more realistic description of real life sinusoidal signals, is given by

$$v(t) = A'(t) \cos(\phi(t)) = A(1 + a(t)) \cos(\omega_c t + \theta(t)) \tag{2.9}$$

where A is a constant, $a(t)$ is the amplitude noise, and $\theta(t)$ is the phase fluctuation noise, also referred to as phase noise. The phase variations may be discrete, resulting in discrete spurious components, or random in nature, creating a continuous frequency spectrum as shown in Figure 2.3. The signal has an instantaneous frequency of $\frac{d\phi(t)}{dt}$, with an average value of ω_c known as the carrier or centre frequency. Note however that the instantaneous frequency varies with time [17, 19].

In most synthesisers, amplitude noise is much lower than phase noise. In addition, amplitude noise generally has less impact on system performance, and can generally be well controlled or mitigated. Thus, in most practical cases, the amplitude of the signal can be considered constant. In this case, all noise is due to $\theta(t)$ [1, 13, 18].

Consider a frequency modulated carrier, with an instantaneous frequency deviation of

$$f(t) = \Delta f \cos(\omega_m t) \quad (2.10)$$

Phase is the time integral of frequency. Therefore, the instantaneous phase deviation is equal to

$$\theta(t) = \int 2\pi f(t) dt = \frac{\Delta f}{f_m} \sin(\omega_m t) = \theta_p \sin(\omega_m t) \quad (2.11)$$

Thus, frequency modulation (FM), with a peak frequency deviation of Δf and modulation frequency f_m , implies phase modulation (PM) at the same modulating frequency with a peak phase deviation of $\theta_p = \frac{\Delta f}{f_m}$ radians [5, 17, 18].

Returning to Equation 2.9, let $a(t) = 0$, and $\theta(t) = \theta_p \sin(\omega_m t) = \frac{\Delta f}{f_m} \sin(\omega_m t)$. For simplicity and without any loss of generality, let $A = 1$. In this case, Equation 2.9 reduces to

$$v(t) = \cos(\omega_c t + \theta_p \sin(\omega_m t)) \quad (2.12)$$

Expanding Equation 2.12 yields

$$v(t) = \cos(\omega_c t) \cos(\theta_p \sin(\omega_m t)) - \sin(\omega_c t) \sin(\theta_p \sin(\omega_m t)) \quad (2.13)$$

Frequency modulation (FM) with small modulation indices (small θ_p) is known as *narrowband FM*. If the peak phase deviation is much less than one ($\theta_p \ll 1$), it follows that

$$\cos(\theta_p \sin(\omega_m t)) \approx 1 \quad (2.14)$$

and

$$\sin(\theta_p \sin(\omega_m t)) \approx \theta_p \sin(\omega_m t) \quad (2.15)$$

Thus for narrowband FM, Equation 2.13 can be approximated as

$$\begin{aligned} v(t) &= \cos(\omega_c t) - \theta_p \sin(\omega_c t) \sin(\omega_m t) \\ &= \cos(\omega_c t) + \frac{\theta_p}{2} \cos((\omega_c + \omega_m)t) - \frac{\theta_p}{2} \cos((\omega_c - \omega_m)t) \end{aligned} \quad (2.16)$$

Note that, for small peak phase deviations, the spectrum consists of two sidebands with peak amplitudes equal to $\frac{\theta_p}{2}$. The single-sideband amplitude spectrum and phasor representation of narrowband FM is pictorially shown in Figure 2.4 [5, 17, 18, 19].

The frequency distribution of a narrowband FM signal is useful for interpreting a signal's spectral

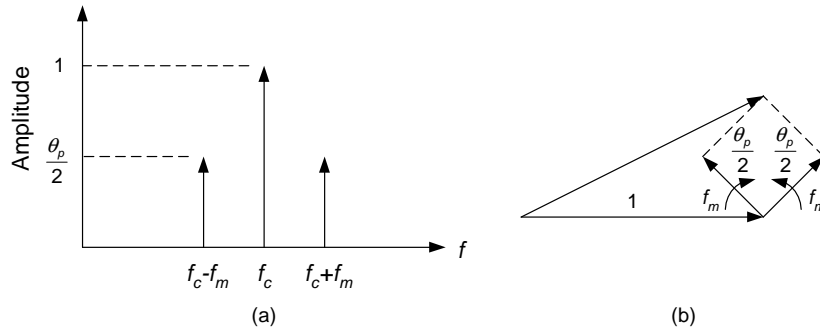


Figure 2.4: (a) SSB amplitude spectrum of a narrowband FM signal (b) Equivalent phasor representation.

density due to phase noise. Although the noise distribution on each side of the carrier of Figure 2.2 is continuous, the spectrum can be divided into a large number of 1 Hz strips, as shown in Figure 2.3. The energy in the 1 Hz band at f_m can then be viewed as being caused by a sinusoidal frequency modulated signal with a deviation proportional to the amplitude of the spectrum at f_m [17].

Phase noise is most commonly expressed as the ratio of the single-sideband noise power in a 1 Hz bandwidth f_m hertz away from the carrier, to the total signal power [5, 13, 18, 19]. Mathematically

$$\mathcal{L}(f_m) = \frac{P_{SSB}(f_m)}{P_S} \quad [1/\text{Hz}] \quad \text{or} \quad \mathcal{L}(f_m) = 10 \log_{10} \left(\frac{P_{SSB}(f_m)}{P_S} \right) \quad [\text{dBc}/\text{Hz}] \quad (2.17)$$

Applying this definition to the waveform of Equation 2.16, results in SSB phase noise equal to

$$\mathcal{L}(f_m) = \frac{\frac{1}{2} \left(\frac{\theta_p}{2} \right)^2}{\frac{1}{2} (1^2)} = \frac{\theta_p^2}{4} = \frac{\theta_{RMS}^2}{2} \quad [1/\text{Hz}] \quad (2.18)$$

where $\theta_{RMS} = \frac{\theta_p}{\sqrt{2}}$ is the RMS value of the phase deviation [13, 19]. Expressed in dBc/Hz, the phase noise is [17, 19]

$$\mathcal{L}(f_m) = 10 \log_{10} \left(\frac{\theta_p}{2} \right)^2 = 20 \log_{10} \left(\frac{\theta_p}{2} \right) \quad [\text{dBc}/\text{Hz}] \quad (2.19)$$

The one-sided spectral density of phase fluctuations is defined as

$$S_\theta(f_m) = \frac{\theta_{RMS}^2(f_m)}{B} \quad [\text{rad}^2/\text{Hz}] \quad (2.20)$$

where B is the measurement bandwidth of θ_{RMS} . The phase spectral density S_θ can also be expressed in dB/Hz, that is, decibels relative to 1 rad^2/Hz [5]. From Equation 2.12, it follows that

$$\theta_{RMS}^2(f_m) = \overline{\theta(t)^2} = \overline{(\theta_p \sin(\omega_m t))^2} = \frac{\theta_p^2}{2} - \frac{\theta_p^2 \cos(2\omega_m t)}{2} = \frac{\theta_p^2}{2} \quad (2.21)$$

where the overbar signifies time average. Substituting Equation 2.21 into Equation 2.20 with $B =$

1 Hz, yields

$$S_{\theta}(f_m) = \frac{\theta_p^2}{2} \left[\text{rad}^2/\text{Hz} \right] \quad (2.22)$$

Comparing Equation 2.18 to Equation 2.22 shows that

$$\mathcal{L}(f_m) = \frac{S_{\theta}(f_m)}{2} \quad (2.23)$$

Equation 2.23 shows that \mathcal{L} in dBc/Hz is 3 dB lower than S_{θ} in dB_r/Hz, which holds only when amplitude noise is negligible, and when the total RMS phase deviation is much smaller than 1 rad [5, 13, 18, 19].

The RMS phase deviation in a frequency band ($B = f_2 - f_1$) can be found by taking the square root of the area under the phase spectral density curve [18, 19]. In mathematical terms,

$$\theta_{RMS} = \sqrt{\int_{f_1}^{f_2} S_{\theta}(f_m) df_m} = \sqrt{\int_{f_1}^{f_2} 2\mathcal{L}(f_m) df_m} \quad [\text{rad}] \quad (2.24)$$

2.3 Decomposition of SSB components into AM and FM

In many frequency synthesis cases, a combination of a carrier signal and a spurious component is encountered. In such a case, the smaller SSB component can be decomposed into amplitude modulation (AM) and FM [5]. To explain this concept, consider an amplitude modulated carrier signal of the form

$$v(t) = (1 + M \cos(\omega_m t)) \cos(\omega_c t) \quad (2.25)$$

where Equation 2.9 has been used, with $\theta(t) = 0$, $a(t) = M \cos(\omega_m t)$, and $A = 1$. For AM, M is known as the modulation index. Expanding Equation 2.25 yields

$$v(t) = \cos(\omega_c t) + \frac{M}{2} \cos((\omega_c + \omega_m) t) + \frac{M}{2} \cos((\omega_c - \omega_m) t) \quad (2.26)$$

Equation 2.26 shows that amplitude modulation with a sinusoid produces a carrier and two sidebands at $f_c + f_m$ and $f_c - f_m$. The ratio of the amplitude of each sideband to that of the carrier is $\frac{M}{2}$ [17, 18].

Figure 2.5(a) shows the single-sided amplitude spectrum of an amplitude modulated signal. The phasor diagram is depicted in Figure 2.5(b). Comparing Figure 2.5 to Figure 2.4 shows that the difference between AM and narrowband FM with a sinusoidal modulating signal lies in the fact that the phasor resulting from the lower sideband (LSB) and upper sideband (USB) phasors adds to the carrier for AM, but is in phase quadrature with the carrier for FM. The difference results from the minus sign in the LSB component of FM [14].

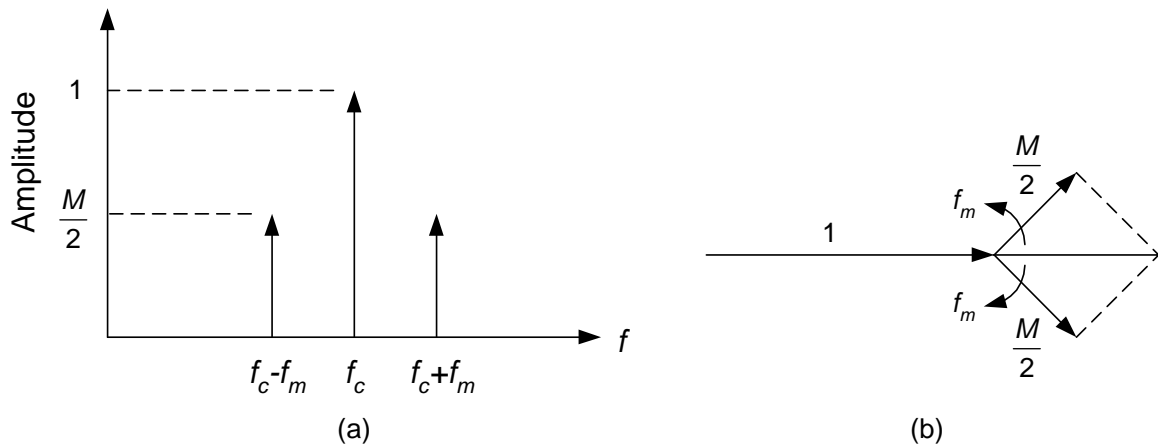


Figure 2.5: (a) SSB amplitude spectrum of an AM signal (b) Equivalent phasor diagram representation.

Figure 2.6 shows the equivalent Fourier and phasor representations of a SSB component with peak amplitude equal to N_o , decomposed into AM and FM [5].

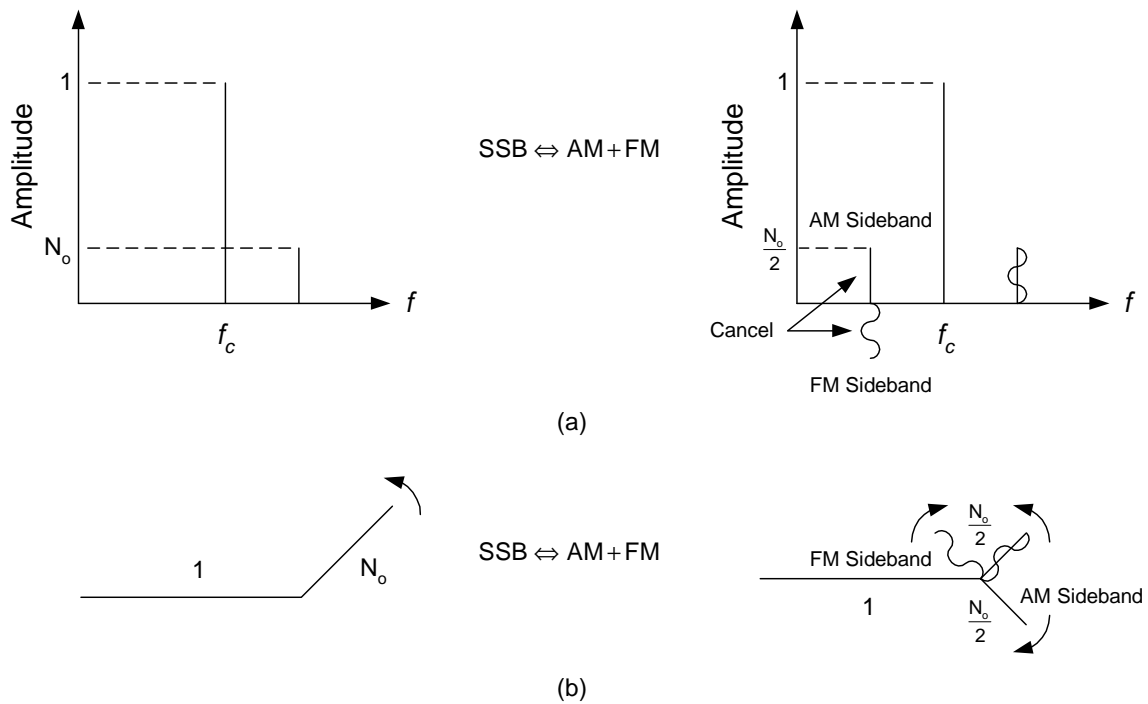


Figure 2.6: (a) Fourier and (b) phasor representation of a SSB component decomposed into AM and FM.

Comparing Equation 2.26 to Equation 2.16 shows that, for AM and FM with a modulation index of N_o , the LSB component of FM cancels with the LSB of AM to produce the equivalent SSB component. This is shown in Figure 2.6. The power in the SSB component is

$$P_{SSB} = \left(\frac{N_o}{\sqrt{2}} \right)^2 = \frac{N_o^2}{2} \tag{2.27}$$

Similarly, the power in each sideband is equal to

$$P_{Sideband} = \left(\frac{N_o}{2\sqrt{2}} \right)^2 = \frac{N_o^2}{8} = \frac{P_{SSB}}{4} \quad (2.28)$$

Equation 2.28 shows that the power of the original SSB component is shared equally between the four sidebands. Thus, half the power is converted to AM and half is converted to FM. If the signal is stripped of AM by a perfect limiter, half the power is absorbed and only FM sidebands with power $P_{FM} = \frac{N_o^2}{8} = P_{SSB} \text{ [dB]} - 6.02 \text{ dB}$ in each sideband, remain [5, 18].

To illustrate this concept further, consider the following example. A 0 dBm signal at 10 MHz, and a -50 dBm spurious signal at 11 MHz enter a perfect limiter. What is the expected amplitudes of the components at the output?

The first step in finding the solution is to decompose the SSB component into AM and FM. This is shown in Figure 2.7. The power level of each sideband is -56.02 dBm, forming a total power level of -50 dBm. The limiter removes the AM sidebands, leaving only FM sidebands. Therefore, the amplitude of the spurious FM components at 9 MHz and 11 MHz is equal to -56.02 dBm. Note that the spurious-free dynamic range (SFDR) has improved by 6.02 dB.

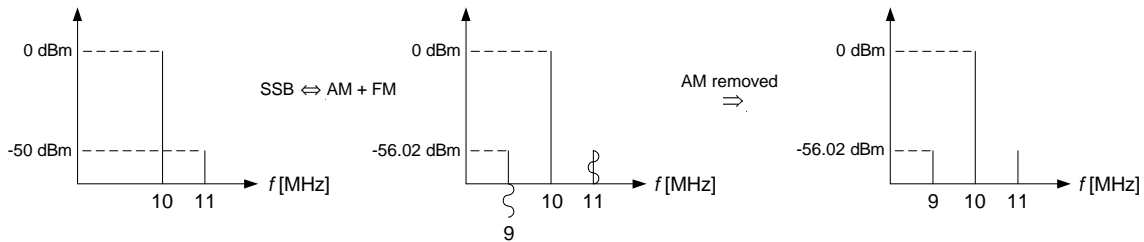


Figure 2.7: SSB decomposition example.

2.4 The Effect of Frequency Multiplication on Phase Noise

When a carrier with phase noise is subjected to frequency multiplication, the signal at the output of the multiplier can be written as

$$v(t) = \cos(n\omega_c t + n\theta(t)) = \cos(n\omega_c t + n\theta_p \sin(\omega_m t)) \quad (2.29)$$

where n is the multiplication factor. Revisiting the narrowband FM theory of Section 2.2.4 shows that the FM sidebands increase by the multiplication factor. The phase noise at the output of the multiplier, with the aid of Equation 2.19, is equal to

$$\mathcal{L}(f_m) = 10 \log_{10} \left(\frac{n\theta_p}{2} / 1 \right)^2 = 20 \log_{10}(n) + 20 \log_{10} \left(\frac{\theta_p}{2} \right) \quad \left[\text{dBc/Hz} \right] \quad (2.30)$$

Equation 2.30 shows that the phase noise is degraded by $20 \log_{10}(n)$ dB. Note that the modulation frequency f_m is not altered by the frequency multiplication process, preserving the frequency spacing between the carrier and the FM sidebands [5, 17, 18, 19].

The same line of reasoning can be extended for the case of frequency division. For frequency division, the phase noise improves by $20 \log_{10}(n)$ dB, where n is the value of the the frequency divider [5, 19].

2.5 Basic PLL Theory

A basic form of a PLL, consisting of a phase detector, loop filter, and voltage-controlled oscillator (VCO), is shown in Figure 2.8.

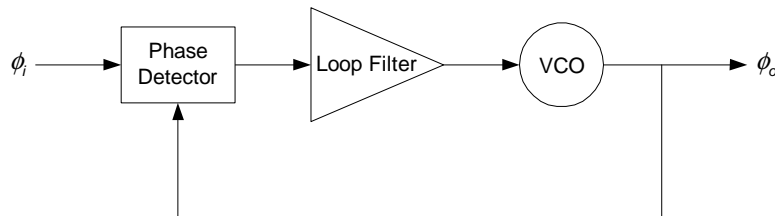


Figure 2.8: Basic PLL structure.

A PLL tracks phase differences between the input and fed back signal from the VCO. The phase detector produces a voltage which is proportional to the phase difference between its two inputs. This error voltage is filtered by the loop filter and applied to the VCO, changing the VCO frequency such that the phase difference between the two phase detector input signals becomes constant, or reduces to zero, depending on the type of phase detector used. When this happens, the loop is said to be *locked*. In the locked condition, the output frequency is equal to the average frequency of the input signal [10, 19].

PLLs are actually narrowband tracking filters. These two features account for the major uses of PLL receivers. Because of the narrow bandwidth of the PLL, it is able to reject large amounts of noise power, enabling a PLL to recover signals that are deeply embedded in noise [10].

2.5.1 PLL Transfer Functions

PLLs are nonlinear feedback control systems, since phase detectors are nonlinear devices. In the locked state however, it can be treated as a linear system. Figure 2.9 shows a linearised model of a digital PLL in Laplace notation, where $s = j\omega = j2\pi f$ is the Laplace transform variable. The noise sources of various components are also shown in the figure. A digital PLL differs from an analogue PLL in that both the the phase-frequency detector (PFD) and frequency divider are manufactured from digital components [19].

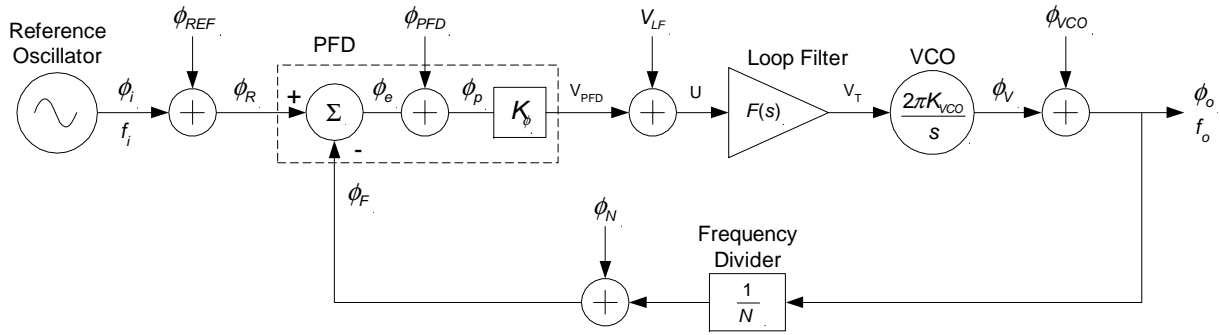


Figure 2.9: Linearised model of a digital PLL.

When the phase difference between the two inputs of the PFD is small, the PFD acts as a linear device. In this case, the output voltage is proportional to the phase difference between its two inputs [10, 19]. Expressed mathematically,

$$V_{PFD}(s) = K_{\phi} (\phi_R(s) - \phi_F(s)) \quad (2.31)$$

where K_{ϕ} is the PFD gain factor, measured in units of volts per radian.

A VCO is a frequency modulator since the frequency deviation $\frac{d\phi_v(t)}{dt}$ at the VCO output is proportional to voltage applied to the control port [14]. In mathematical terms

$$\frac{d\phi_v(t)}{dt} = 2\pi K_{VCO} v_t(t) \quad (2.32)$$

where K_{VCO} represents the tuning sensitivity of the VCO, in MHz/V. In Laplace notation, Equation 2.32 becomes

$$\mathcal{L} \left\{ \frac{d\phi_v(t)}{dt} \right\} = s\phi_V(s) = 2\pi K_{VCO} V_T(s) \quad (2.33)$$

where $\mathcal{L} \{ \}$ denotes the Laplace transform. Rearranging terms yields

$$\frac{\phi_V(s)}{V_T(s)} = \frac{2\pi K_{VCO}}{s} \quad (2.34)$$

The forward gain of the PLL is equal to the product of the transfer functions in the forward path. It can be written as

$$G(s) = \frac{K_{\phi} F(s) 2\pi K_{VCO}}{s} \quad (2.35)$$

The open loop transfer function, also sometimes referred to as the loop gain, is equal to the product of the forward gain transfer function and the feedback transfer function, that is,

$$L(s) = G(s)H(s) = \frac{K_{\phi} F(s) 2\pi K_{VCO}}{Ns} \quad (2.36)$$

where $H(s) = \frac{1}{N}$.

The closed-loop transfer function, relating $\phi_i(s)$ and $\phi_o(s)$, can be written as [5, 10, 17, 19]

$$H_{CL}(s) = \frac{\phi_o(s)}{\phi_i(s)} = \frac{G(s)}{1 + G(s)H(s)} = \frac{\frac{K_\phi F(s)2\pi K_{VCO}}{s}}{1 + \frac{K_\phi F(s)2\pi K_{VCO}}{Ns}} = \frac{NK_\phi F(s)2\pi K_{VCO}}{Ns + K_\phi F(s)2\pi K_{VCO}} \quad (2.37)$$

The transfer characteristic of the reference oscillator noise source to the output, can be found by setting all other noise sources to zero and by writing the output phase as

$$\phi_o(s) = \frac{\phi_e(s)K_\phi F(s)2\pi K_{VCO}}{s} \quad (2.38)$$

where

$$\phi_e(s) = \phi_{REF}(s) - \phi_F(s) = \phi_{REF}(s) - \frac{\phi_o(s)}{N} \quad (2.39)$$

Substituting Equation 2.39 into Equation 2.38 and rearranging terms, yields

$$H_{REF}(s) = \frac{\phi_o(s)}{\phi_{REF}(s)} = \frac{\frac{K_\phi F(s)2\pi K_{VCO}}{s}}{1 + \frac{K_\phi F(s)2\pi K_{VCO}}{Ns}} = \frac{NK_\phi F(s)2\pi K_{VCO}}{Ns + K_\phi F(s)2\pi K_{VCO}} \quad (2.40)$$

For the frequency divider noise, the error function is equal to

$$\phi_e(s) = - \left(\phi_N(s) + \frac{\phi_o(s)}{N} \right) \quad (2.41)$$

Substituting Equation 2.41 into Equation 2.38, yields

$$H_N(s) = \frac{\phi_o(s)}{\phi_N(s)} = \frac{-\frac{K_\phi F(s)2\pi K_{VCO}}{s}}{1 + \frac{K_\phi F(s)2\pi K_{VCO}}{Ns}} = \frac{-NK_\phi F(s)2\pi K_{VCO}}{Ns + K_\phi F(s)2\pi K_{VCO}} \quad (2.42)$$

The transfer function relating the input referred PFD noise to the output phase, can be found by writing the output phase as

$$\phi_o(s) = \frac{\phi_p(s)K_\phi F(s)2\pi K_{VCO}}{s} \quad (2.43)$$

where

$$\phi_p(s) = \phi_{PFD}(s) + \phi_e(s) = \phi_{PFD}(s) - \frac{\phi_o(s)}{N} \quad (2.44)$$

Therefore

$$H_{PFD}(s) = \frac{\phi_o(s)}{\phi_{PFD}(s)} = \frac{\frac{K_\phi F(s)2\pi K_{VCO}}{s}}{1 + \frac{K_\phi F(s)2\pi K_{VCO}}{Ns}} = \frac{NK_\phi F(s)2\pi K_{VCO}}{Ns + K_\phi F(s)2\pi K_{VCO}} \quad (2.45)$$

Note that all the transfer functions derived thus far are equal in magnitude to the closed-loop transfer function of the PLL, that is, $|H_{CL}(s)| = |H_{REF}(s)| = |H_N(s)| = |H_{PFD}(s)|$.

The transfer function shaping the loop filter noise to the output can be found by writing

$$\phi_o(s) = \frac{U(s)F(s)2\pi K_{VCO}}{s} \quad (2.46)$$

where

$$U(s) = V_{LF}(s) + \phi_p(s)K_\phi = V_{LF}(s) - \frac{\phi_o(s)K_\phi}{N} \quad (2.47)$$

Therefore

$$H_{LF}(s) = \frac{\phi_o(s)}{V_{LF}(s)} = \frac{\frac{F(s)2\pi K_{VCO}}{s}}{1 + \frac{K_\phi F(s)2\pi K_{VCO}}{Ns}} = \frac{NF(s)2\pi K_{VCO}}{Ns + K_\phi F(s)2\pi K_{VCO}} \quad (2.48)$$

Note that $H_{LF}(s)$ is a factor K_ϕ smaller than the closed-loop transfer function of the PLL. The loop filter transfer function can be expressed as

$$H_{LF}(s) = \frac{1}{K_\phi} \frac{NK_\phi F(s)2\pi K_{VCO}}{Ns + K_\phi F(s)2\pi K_{VCO}} = \frac{1}{K_\phi} H_{CL}(s) \quad (2.49)$$

The transfer function for the VCO noise is

$$\phi_o(s) = \phi_{VCO}(s) + \frac{\phi_e(s)K_\phi F(s)2\pi K_{VCO}}{s} \quad (2.50)$$

where

$$\phi_e(s) = -\frac{\phi_o(s)}{N} \quad (2.51)$$

Substituting Equation 2.51 into Equation 2.50 yields

$$H_{VCO}(s) = \frac{\phi_o(s)}{\phi_{VCO}(s)} = \frac{1}{1 + \frac{K_\phi F(s)2\pi K_{VCO}}{Ns}} \quad (2.52)$$

which is smaller than the closed-loop transfer function by the forward gain.

2.5.2 PLL Noise Analysis

For a linear time-invariant system with transfer function $H(s)$, the spectral density at the output of the system, is related to the spectral density at the input by [6, 14]

$$S_o(f) = |H(f)|^2 S_i(f) \quad (2.53)$$

The total phase spectral density at the output of the PLL can be found by adding all the uncorrelated noise sources, that is,

$$S_\phi(f) = \left(S_{REF}(f) + S_{PFD}(f) + S_N(f) + \frac{S_{LF}(f)}{K_\phi^2} \right) |H_{CL}(f)|^2 + S_{VCO}(f) |H_{VCO}(f)|^2 \quad (2.54)$$

Note that the reference oscillator, PFD, frequency divider, and loop filter noise all scale to the output of the synthesiser by the magnitude of the closed-loop transfer function, given by

$$|H_{CL}(s)| = \left| \frac{\frac{K_\phi F(s)2\pi K_{VCO}}{s}}{1 + \frac{K_\phi F(s)2\pi K_{VCO}}{Ns}} \right| \quad (2.55)$$

The loop filter $F(s)$ is of lowpass form. Therefore, at low frequencies well within the loop bandwidth of the PLL,

$$|L(s)| = \left| \frac{K_\phi F(s) 2\pi K_{VCO}}{Ns} \right| \gg 1 \quad (\omega \ll \omega_c) \quad (2.56)$$

where the crossover frequency of the loop, is defined as the frequency point where [21]

$$|L(j\omega_c)| = 1 \quad (2.57)$$

The crossover frequency ω_c of the open loop transfer function is closely related to the closed-loop 3 dB bandwidth of the PLL. For underdamped systems, the closed-loop bandwidth is typically somewhat greater than ω_c , though usually less than $2\omega_c$ [21]. In this text, ω_c will be referred to as the loop bandwidth or cutoff frequency of the loop.

For low frequencies, the closed-loop transfer function reduces to

$$|H_{CL}(s)| \approx \left| \frac{\frac{K_\phi F(s) 2\pi K_{VCO}}{s}}{\frac{K_\phi F(s) 2\pi K_{VCO}}{Ns}} \right| = |N| \quad (\omega \ll \omega_c) \quad (2.58)$$

Expressed in decibels,

$$20 \log_{10} |H_{CL}(s)| = 20 \log_{10} N \quad (\omega \ll \omega_c) \quad (2.59)$$

Note that, for low frequencies within the loop bandwidth of the PLL, the transfer function of the VCO becomes

$$|H_{VCO}(s)| = \left| \frac{1}{1 + L(s)} \right| \approx \left| \frac{1}{G(s)H(s)} \right| = \left| \frac{N}{G(s)} \right| \approx 0 \quad (\omega \ll \omega_c) \quad (2.60)$$

Therefore, for low offset frequencies, the phase spectral density at the output of the PLL reduces to

$$S_\phi(f) \approx \left(S_{REF}(f) + S_{PFD}(f) + S_N(f) + \frac{S_{LF}(f)}{K_\phi^2} \right) |H_{CL}(f)|^2 \quad (\omega \ll \omega_c) \quad (2.61)$$

Equation 2.61 shows that the reference oscillator, PFD, frequency divider, and loop filter are the major contributors of in-band phase noise, while the in-band phase noise contribution of the VCO is essentially negligible. The PLL thus acts as a lowpass filter to reference oscillator, PFD, frequency divider and loop filter noise.

For very low offset frequencies, the reference oscillator phase noise usually dominates the other in-band noise contributors. In this case, Equation 2.61 becomes

$$S_\phi(f) = S_{REF}(f) |H_{CL}(f)|^2 = S_{REF}(f) N^2 \quad (2.62)$$

which shows that the phase noise of the reference oscillator essentially determines the in-band phase noise at low offset frequencies [19]. Note that the in-band phase noise increases by $20 \log_{10} N$. Therefore, to obtain low in-band phase noise requires choosing N as low as possible.

For frequencies much higher than the loop bandwidth, the open loop transfer function is

$$|L(s)| \ll 1 \quad (\omega \gg \omega_c) \quad (2.63)$$

In this case, the closed-loop transfer function can be approximated as

$$|H_{CL}(s)| \approx |G(s)| = \left| \frac{K_\phi F(s) 2\pi K_{VCO}}{s} \right| \quad (\omega \gg \omega_c) \quad (2.64)$$

The transfer function of the VCO can be approximated as

$$|H_{VCO}(s)| \approx 1 \quad (\omega \gg \omega_c) \quad (2.65)$$

The forward gain transfer function $G(s)$ is a monotonically decreasing function, and is small at frequencies much higher than the loop bandwidth. Thus, outside the loop bandwidth, the VCO is the main contributor of phase noise. The loop thus acts as a highpass filter to VCO noise.

For offset frequencies outside the loop bandwidth of the PLL, the total phase spectral density at the output of the PLL can be approximated as

$$S_\phi(f) \approx S_{VCO}(f) |H_{VCO}(f)|^2 \approx S_{VCO}(f) \quad (\omega \gg \omega_c) \quad (2.66)$$

Equation 2.66 shows that outside the loop bandwidth of the PLL, the overall phase noise is essentially equal to the free-running VCO phase noise.

The loop bandwidth for optimal phase noise performance is equal to the frequency point where the VCO phase noise intersects with the total phase noise of all the in-band phase noise contributors. This is illustrated in Figure 2.10. Above the loop bandwidth frequency f_c , $(S_{REF}(f) + S_{PFD}(f) + S_N(f) + \frac{S_{LF}(f)}{K_\phi^2}) |N|^2$ is attenuated where it is greater than the free-running VCO phase noise. For frequencies lower than f_c , S_{VCO} is attenuated by the response of the loop where it is greater compared to the total phase noise of the in-band contributors.

It has been shown that the in-band phase noise scales by $20 \log_{10} N$. Therefore, to minimise the phase noise within the loop bandwidth, requires choosing N as low as possible. In the locked state, the output frequency is related to the input reference frequency by

$$f_o = N f_i \quad (2.67)$$

From Equation 2.67 it is clear that lowering N , requires increasing the reference frequency to obtain the same output frequency. Thus, if N is halved, the reference frequency needs to be doubled to keep the output frequency constant. Therefore, to obtain the same output frequency, the overall or net frequency multiplication factor (N_{net}) from the input to output must stay constant, regardless of whether N is reduced or increased.

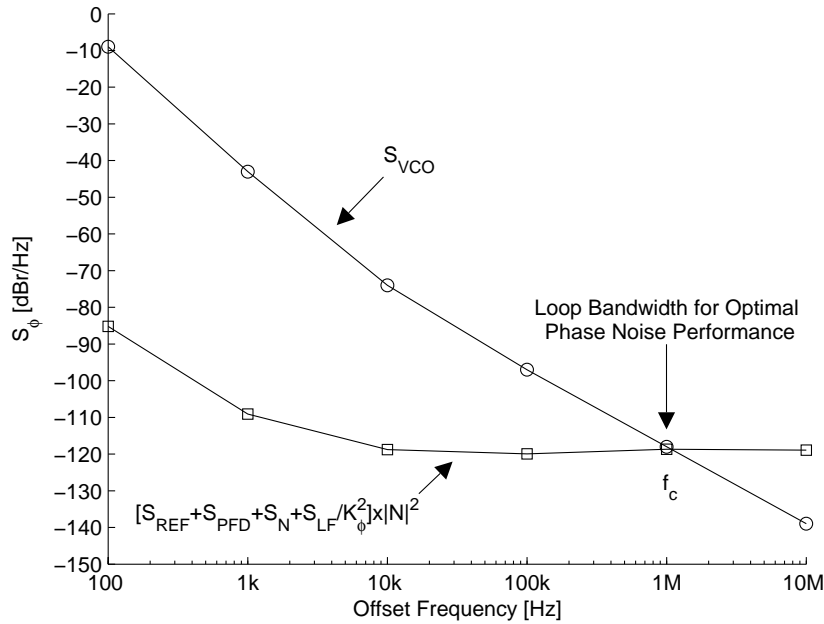


Figure 2.10: Choosing the loop bandwidth for optimal phase noise performance.

The phase noise of the reference oscillator degrades by $20 \log_{10} N_{net}$ from the input to output. Therefore, lowering N and increasing the reference frequency does not lower the phase noise contribution of the reference oscillator, since the overall multiplication factor to the output stays the same. However, for the PFD used for the synthesiser discussed in this thesis, lowering N does improve the in-band phase noise contribution of the PFD.

To understand this, consider the SSB phase noise of the HMC439QS16G PFD from *Hittite* listed in Table 2.1 for two different operating input reference frequencies.

Table 2.1: HMC439QS16G PFD SSB phase noise.

Offset Frequency	Hz	100	1k	10k	100k	1M	10M
$f_{r1} = 100 \text{ MHz}$	dBc/Hz	-144	-153	-153	-153	-151	-150
$f_{r2} = 1280 \text{ MHz}$	dBc/Hz	-129	-140	-143	-143	-139	-141
$\sigma \log_{10} \left(\frac{f_{r2}}{f_{r1}} \right) = PN_{f_{r2}} - PN_{f_{r1}}$	σ	13.55	11.74	9.03	9.03	10.84	8.13

Table 2.1 shows that the PFD phase noise scales by $\sigma \log_{10}(f_r)$, where f_r is the reference frequency of the PFD. Thus, in terms of the in-band PFD phase noise contribution, lowering N causes a $20 \log_{10} N$ decrease in phase noise, while the corresponding increase in reference frequency causes the PFD phase noise to increase only by $\sigma \log_{10}(f_r)$. Thus for every doubling in reference frequency, a reduction of about 3 dB ($\sigma \approx 10$) PFD phase noise contribution is obtained. For this reason, choosing N as low as possible and the reference frequency as high as possible, reduces the PFD phase noise contribution to the overall phase noise of the PLL.

2.5.3 Loop Type, Order and Frequency Response

Consider a passive RC loop filter of the form

$$F(s) = \frac{s\tau_1 + 1}{s\tau_2 + 1} \quad (2.68)$$

where τ_1 and τ_2 are constants. Substituting Equation 2.68 into the open loop transfer function given by Equation 2.36, yields

$$L(s) = \frac{K_\phi (s\tau_1 + 1) 2\pi K_{VCO}}{Ns (s\tau_2 + 1)} \quad (2.69)$$

Figure 2.11 shows a Bode plot of the open loop frequency response given by Equation 2.69, with $\tau_1 \gg \tau_2$. The *phase margin*, which gives an indication of the stability of the loop, is defined as

$$\text{Phase Margin} = 180^\circ + \angle L(j\omega_c) \quad (2.70)$$

where ω_c is the crossover frequency of the open loop transfer function. In this example, the phase margin is 145° . For a stable system, the phase margin is typically larger than or equal to 30° [17]. Note that the combination of the zero and the pole of the loop filter has the effect of maximising the phase at the crossover frequency of the loop, improving the phase margin.

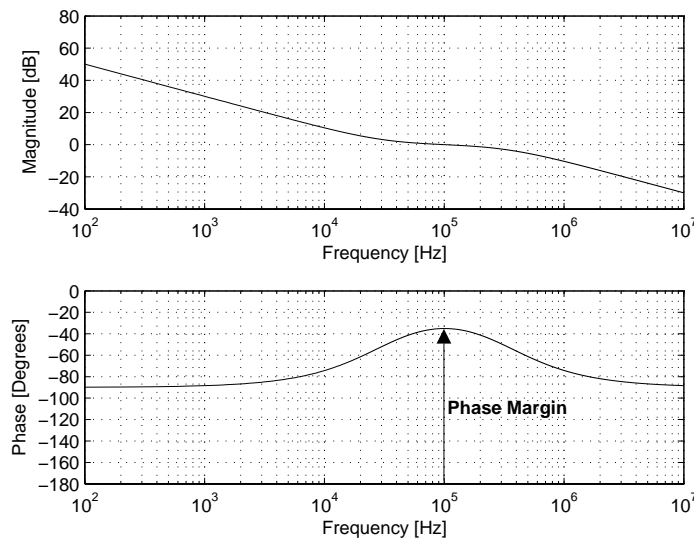


Figure 2.11: Typical open loop frequency response.

The *type* of a loop refers to the number of poles at the origin of the open loop transfer function. Any PLL is at least a Type 1 loop because of the integrator in the VCO transfer function. Thus, since the loop filter given by Equation 2.68 has no poles at the origin, the PLL is a Type 1 loop. If the loop filter contains one pole at the origin, the open loop transfer function has two poles at the origin, and the PLL is classified as a Type 2 loop [10, 19].

To see how the loop type influences the steady-state error of the PLL, that is, the error remaining when all transients have died out, consider the error response transfer function, given by

$$\frac{\phi_e(s)}{\phi_i(s)} = \frac{\phi_i(s) - \phi_F(s)}{\phi_i(s)} = 1 - \frac{\phi_F(s)}{\phi_i(s)} = 1 - \frac{\phi_e(s)K_\phi F(s)2\pi K_{VCO}}{\phi_i(s)Ns} \quad (2.71)$$

Rearranging terms yields

$$\frac{\phi_e(s)}{\phi_i(s)} = \frac{1}{1 + \frac{K_\phi F(s)2\pi K_{VCO}}{Ns}} = \frac{1}{1 + G(s)H(s)} = \frac{1}{1 + L(s)} \quad (2.72)$$

which in turn can be written as

$$\phi_e(s) = \frac{\phi_i(s)Ns}{Ns + K_\phi F(s)2\pi K_{VCO}} \quad (2.73)$$

To find the steady-state error for various driving input functions, the *Final Value Theorem* is applied to the error function, that is,

$$\lim_{t \rightarrow \infty} \phi_e(t) = \lim_{s \rightarrow 0} s\phi_e(s) \quad (2.74)$$

where $\phi_e(s)$ is the Laplace transform of $\phi_e(t)$ [10, 19, 21]. It is customary to analyse the performance of the loop for three different conditions, namely [17, 19]

1. A step input.
2. A ramp input.
3. A parabolic input.

The steady-state error for a step input in phase $\phi_i(t) = 1(t)$, is equal to

$$\varepsilon_{ss} = \lim_{s \rightarrow 0} s\phi_e(s) = \lim_{s \rightarrow 0} \left[s \frac{Ns}{Ns + K_\phi F(s)2\pi K_{VCO}} \frac{1}{s} \right] = \lim_{s \rightarrow 0} \left[\frac{Ns}{Ns + K_\phi F(s)2\pi K_{VCO}} \right] = 0 \quad (2.75)$$

where $\mathcal{L} = \{1(t)\} = \frac{1}{s}$. The steady-state error resulting from a ramp of input phase (step in frequency) $\phi_i(t) = t1(t)$, is equal to

$$\varepsilon_{ss} = \lim_{s \rightarrow 0} s\phi_e(s) = \lim_{s \rightarrow 0} \left[s \frac{Ns}{Ns + K_\phi F(s)2\pi K_{VCO}} \frac{1}{s^2} \right] = \frac{N}{K_\phi 2\pi K_{VCO}} \quad (2.76)$$

For the third case, consider a parabolic phase input (frequency ramp) of the form $\phi_i(t) = \frac{1}{2}t^2 1(t)$. The steady-state error is found to be

$$\varepsilon_{ss} = \lim_{s \rightarrow 0} s\phi_e(s) = \lim_{s \rightarrow 0} \left[s \frac{Ns}{Ns + K_\phi F(s)2\pi K_{VCO}} \frac{1}{s^3} \right] = \lim_{s \rightarrow 0} \left[\frac{N}{Ns^2 + sK_\phi F(s)2\pi K_{VCO}} \right] = \infty \quad (2.77)$$

It is apparent from the last three equations that a Type 1 loop can track out a step change in phase, and will follow a step in frequency with a constant error. Equation 2.77 shows that the loop is not

very attractive for frequency tracking, as above some critical value of rate of change of reference frequency the loop will no longer stay locked [17, 19].

Performing the same analysis on other loop types, yields the steady-state errors for different input driving functions as listed in Table 2.2 [17].

Table 2.2: Steady-state errors for different loop types and various input driving functions.

Type of System	ε_{ss} for step input	ε_{ss} for ramp input	ε_{ss} for parabolic input
0	Constant	∞	∞
1	0	Constant	∞
2	0	0	Constant

Table 2.2 shows that a Type 2 loop can track a frequency ramp with a constant error. The PLL considered in this thesis is a Type 2 loop, since the loop filter has one pole at the origin.

Substituting the transfer function of the loop filter given by Equation 2.68 into the closed-loop transfer function of the PLL, yields

$$H_{CL}(s) = \frac{\frac{K_\phi(s\tau_1+1)2\pi K_{VCO}}{(s\tau_2+1)s}}{1 + \frac{K_\phi(s\tau_1+1)2\pi K_{VCO}}{(s\tau_2+1)Ns}} = \frac{NK_\phi(s\tau_1+1)2\pi K_{VCO}}{s^2N\tau_2 + s(N + 2\pi K_{VCO}K_\phi\tau_1) + 2\pi K_{VCO}K_\phi} \quad (2.78)$$

Since the highest power of s in the denominator of the closed-loop transfer function is equal to 2, the loop is classified as a second-order loop [10, 17, 19].

The closed-loop transfer function can be written in the form

$$H_{CL}(s) = \frac{\frac{NK}{\tau_2}(s\tau_1+1)}{s^2 + s\frac{1}{\tau_2}(1 + K\tau_1) + \frac{K}{\tau_2}} = \frac{sN\left(2\zeta\omega_n - \frac{\omega_n^2}{K}\right) + N\omega_n^2}{s^2 + 2\zeta\omega_ns + \omega_n^2} \quad (2.79)$$

where

$$\omega_n = \sqrt{\frac{K}{\tau_2}} \quad (2.80)$$

and

$$\zeta = \frac{1}{2\sqrt{K\tau_2}}(1 + K\tau_1) \quad (2.81)$$

and where $K = \frac{2\pi K_{VCO}K_\phi}{N}$. In analogy with servo terminology, ω_n is known as the *natural frequency* of the loop and ζ is known as the *damping factor*. Note that both the natural frequency and damping factor can be set independently by the two constants of the loop filter [10].

Figure 2.12 shows the magnitude of the closed-loop frequency response of the system given by Equation 2.79, for various different damping factors. Note that the closed-loop frequency response is of lowpass form, as expected. The closed-loop response exhibits peaking in the vicinity of the closed-

loop bandwidth of the loop. The maximum value of the frequency response magnitude is referred to as the *resonant peak* [21].

It can be shown that the phase margin is closely related to the damping factor [21]. In fact, choosing a higher phase margin has the same effect as increasing the damping factor. Equation 2.54 shows that the total phase noise spectral density at the output of the PLL is proportional to the magnitude squared of the closed-loop transfer function. Thus, from Figure 2.12, it is clear that for optimal phase noise performance, a high phase margin or damping factor should be chosen to minimise the resonant peak in the vicinity of the cutoff frequency of the loop.

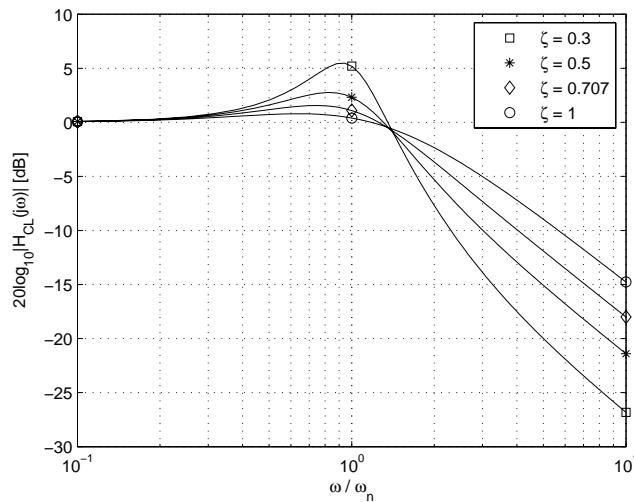


Figure 2.12: Closed-loop frequency response of a second-order loop as a function of ζ .

2.6 Conclusion

This chapter covered some basic noise and PLL theory, laying the foundation for the rest of the chapters of this thesis. In the first part of this chapter, various types of noise were discussed. The concept of phase noise was explained with the aid of FM theory, and the effect of frequency multiplication and division on phase noise, was investigated.

In the latter part of this chapter, the influence of phase noise of individual components of the PLL on the overall phase noise within and outside the loop bandwidth of the PLL, was investigated. It was shown that the reference oscillator, PFD, frequency divider, and loop filter are the major contributors of in-band phase noise, while the phase noise of the PLL outside the loop bandwidth is essentially determined by the phase noise of the VCO. The concept of choosing the loop bandwidth and PFD reference frequency for optimal PLL phase noise performance, was illustrated. Finally, the effect of different damping factor values on the closed-loop frequency response, and hence the overall phase noise of the PLL, was investigated.

Chapter 3

An Introduction to the Indirect Frequency Synthesiser

3.1 Introduction

This chapter presents a discussion of the proposed indirect frequency synthesiser architecture which is introduced in block diagram form in the next section. The roles of the synthesiser components are explained and the reasoning behind some choices of components is motivated. This chapter serves as a qualitative description of the synthesiser. Mathematical formulas are used only in cases where it aids in illustrating a concept more clearly. The analytical design is the topic of Chapter 6.

3.2 Frequency Synthesiser Block Diagram and Description

Figure 3.1 shows a simplified block diagram representation of the indirect frequency synthesiser. In its simplest form, the frequency synthesiser comprises a reference frequency source, a PLL and a direct digital synthesiser (DDS) which, in conjunction with the PLL, is used to enable the output to cover the required 2 GHz LO frequency range as specified in Table 1.1. For the purpose of the discussion that follows, the block diagram is divided into two parts.

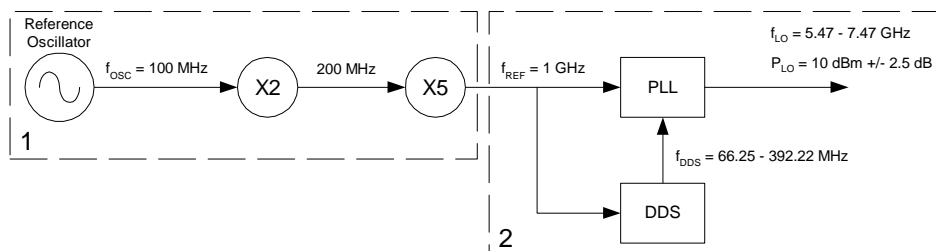


Figure 3.1: Simplified block diagram representation of the indirect frequency synthesiser.

3.2.1 Multiplier Chain

The section of the block diagram which shows how the 100 MHz fundamental reference frequency is multiplied to 1 GHz, is depicted in more detail in Figure 3.2.

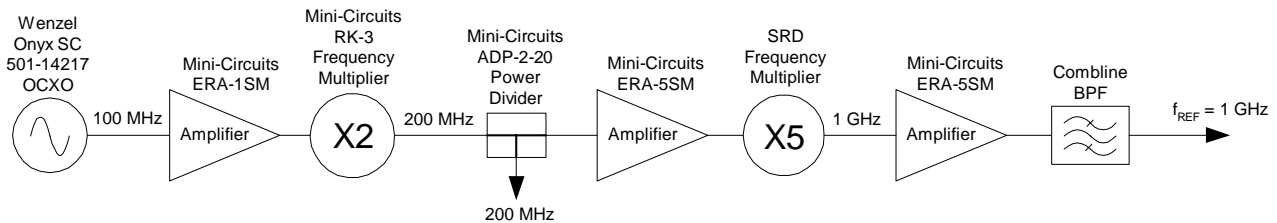


Figure 3.2: Block diagram representation of the multiplier chain.

At the heart of the frequency synthesiser is a low noise 100 MHz oven-controlled crystal oscillator (OCXO) which is used as the fundamental reference frequency source. The built-in oven of the oscillator keeps the crystal and internal critical circuitry at a constant temperature, mitigating the effect of temperature induced frequency variations.

The previous chapter showed that the phase noise within the loop bandwidth of a PLL depends partly on the phase noise of the reference oscillator. Especially at offset frequencies close to the carrier, the reference oscillator is usually the dominant source of phase noise. This is due to the levels of phase noise which, in comparison with other in-band phase noise contributors, are generally significantly higher. A high performance reference oscillator is essential for low noise PLL design and should be chosen according to the specific in-band phase noise requirements. The phase noise calculations of Chapter 6 show that the high quality oscillator from *Wenzel Associates* is a suitable candidate for the synthesiser.

Figure 3.3 shows the single-sideband (SSB) phase noise of the oscillator. The squares on the figure are connected with straight lines and indicate the phase noise as given by the manufacturer. At 10 Hz offset, the phase noise is already as low as -90 dBc/Hz, decreasing rapidly with increasing offset frequency, reaching the noise floor at 10 kHz frequency offset from the carrier.

The ERA-1SM *Mini-Circuits* amplifier shown in Figure 3.2 is driven slightly into saturation to reduce any output power variation of the OCXO. In addition, it provides isolation between the frequency doubler and the OCXO. ERA amplifiers were chosen for all the gain stages of the synthesiser since they require minimal external circuitry, can be designed for a wide range of bias voltages, and have relatively low noise figures, minimising the degradation of the noise floor.

A passive diode frequency doubler from *Mini-Circuits* is used to increase the fundamental reference frequency to 200 MHz. The frequency multiplication process causes the phase noise of the signal being multiplied to degrade by $20 \log_{10}(2) = 6.02$ dB. The phase noise of the output signal is furthermore degraded by noise inherent to the multiplier, but it is usually much less compared to the

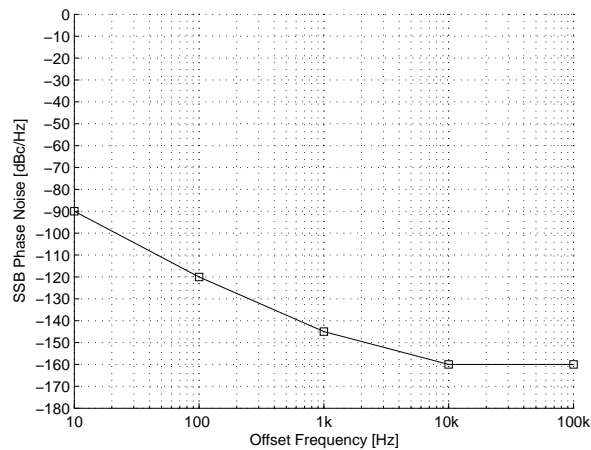


Figure 3.3: SSB phase noise of the OCXO used for the synthesiser.

degradation caused by the multiplication process, and can for all practical purposes be neglected. Note that any spurious components at the input of the doubler also increase by 6.02 dB.

Besides the desired second harmonic, the nonlinear behaviour of the multiplier also produces higher order harmonics, each spaced 100 MHz apart. The fundamental input signal frequency also appears in the output spectrum, but both the fundamental and unwanted harmonic components are considerably lower in power compared to the wanted second harmonic. The frequency content at the output of the doubler is presented in Chapter 7.

Further frequency multiplication by means of a custom designed step-recovery diode (SRD) multiplier is employed, increasing the 200 MHz signal frequency by a factor five to yield a reference frequency of 1 GHz. The anti-parallel configuration of SRDs used in the circuit ensure high levels of even-order harmonic suppression. An SRD-based multiplier was chosen since SRDs are low noise devices and the inevitable $20 \log_{10}(5) = 13.98$ dB degradation in phase noise invariably dominates any noise introduced by the device itself [13, 22]. The design and measured frequency response of this multiplier are outlined in the next chapter.

The amplifier at the input of the SRD multiplier compensates for the conversion loss of the RK-3 frequency doubler and the 3 dB decrease in power caused by the power divider. It provides the required gain to set the SRD multiplier to a practical operating point. Additional amplification at the output of the SRD multiplier is required to provide the necessary power at the 1 GHz output.

A Chebyshev combline bandpass filter with a centre frequency of 1 GHz and a ripple bandwidth of 3% is used to suppress undesired frequency components generated during the multiplication process. The narrow bandwidth of the filter ensures a spectrally clean reference and clock signal for the PFD and DDS, respectively. The design and measured frequency response of this filter are discussed in Chapter 5.

3.2.2 PLL and DDS Description

Figure 3.4 shows the rest of the synthesiser architecture required to produce the synthesised LO signal. With the exception of the quadrature modulator used in the feedback path, the typical PLL architecture discussed in Chapter 2 is clearly recognisable.

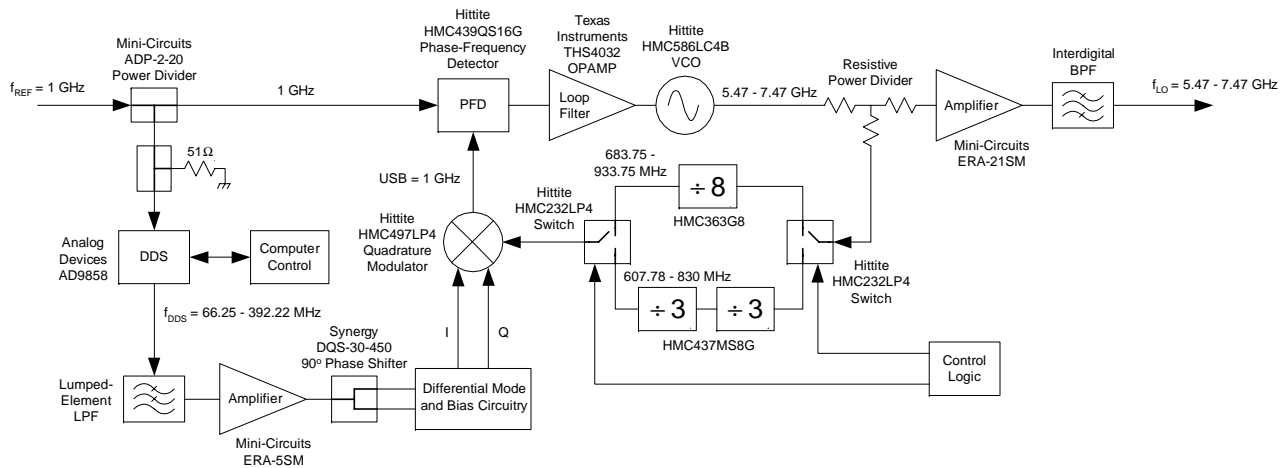


Figure 3.4: Block diagram representation of the PLL and DDS.

The frequency synthesiser is designed to be tunable over a 2 GHz frequency range. Frequency agility is enabled with the computer-controlled DDS which is used to generate a sinusoidal signal in the 66.25 MHz to 392.22 MHz frequency range.

A DDS is a device used to produce a phase and frequency-tunable analogue waveform referenced to a fixed-frequency clock source. The DDS core generates a time-varying signal in digital form and then performs a digital-to-analogue conversion to produce the analogue signal. Direct digital synthesisers are known for their fine frequency resolution, good spurious performance, low phase noise and extremely fast frequency hopping capabilities.

Figure 3.5 shows the internal architecture of the AD9858 DDS, as given in the datasheet. At the heart of the DDS core is a frequency tuning word (FTW), a 32-bit phase accumulator, a phase-to-amplitude converter and a 10-bit digital-to-analogue converter (DAC) operating up to a maximum frequency of 1 GHz. The AD9858 features an on-chip divide-by-2 circuit, allowing the external clock input to be as high as 2 GHz. Although not used, the AD9858 DDS also offers an analogue mixer capable of operating up to 2 GHz, a PFD and a programmable charge pump (CP) with advanced fast-lock capability.

The FTW and other control registers of the AD9858 DDS can either be programmed in serial or parallel mode. For use with the synthesiser, a computer was used to load the registers in parallel mode.

To understand the functioning of the DDS, visualise the generated sinusoidal signal as a vector rotating around a phase wheel, as shown in Figure 3.6. The number of discrete points contained in

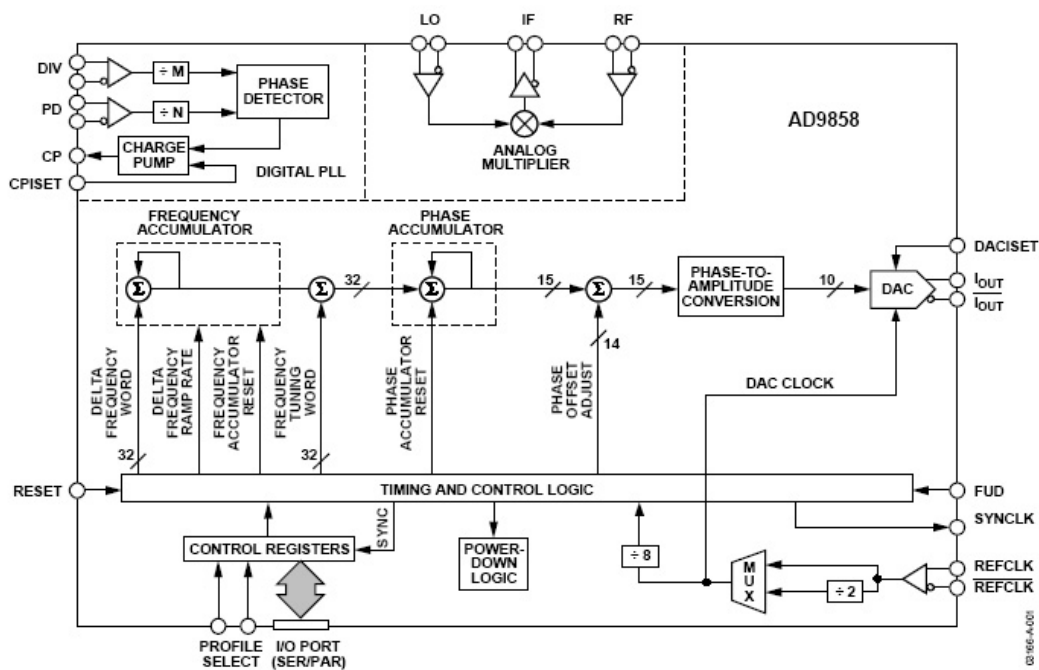


Figure 3.5: Functional block diagram of the AD9858 DDS.

the wheel is determined by the resolution, N , of the phase accumulator. For the AD9858, $N = 32$, resulting in $2^{32} = 4294967296$ discrete points. Each point on the phase wheel maps to an equivalent point on the cycle of a sinusoid. A complete cycle of the sinusoid is generated when the vector makes a complete revolution around the phase wheel.

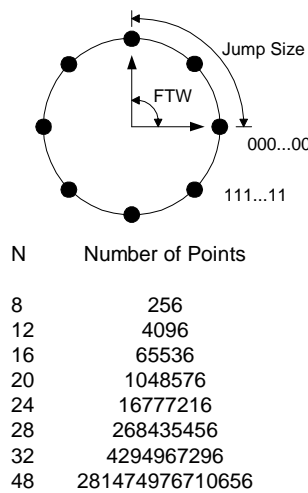


Figure 3.6: Digital phase wheel.

The output of the phase accumulator cannot directly be used to generate a sinewave, since its output is linear. For this reason, a phase-to-amplitude lookup table is used to convert the phase accumulator’s instantaneous output value into sinewave amplitude information. The output of the phase-to-amplitude converter represents a digital sinewave which the DAC converts to an analogue signal.

The phase accumulator is a counter that increments its stored value every time it receives a clock pulse. The magnitude of the increment is determined by the FTW. The FTW determines how many points to skip around the phase wheel. The larger the jump size, the faster the phase accumulator overflows and completes its equivalent sinewave cycle, resulting in a higher frequency being generated. Changing the FTW results in an almost instantaneous change in output frequency.

From the preceding paragraphs, it is clear that the output frequency is directly proportional to the value of the FTW and the system clock, and inversely proportional to the resolution of the phase accumulator. In mathematical form, the output frequency can be written as

$$f_o = \frac{FTW \times f_{clk}}{2^N} \quad [\text{Hz}] \quad (3.1)$$

where FTW is the decimal number of the frequency tuning word, f_{clk} is the system clock frequency (or equivalently, the sampling rate), and N is the length of the phase accumulator in bits.

The smallest frequency change occurs when the FTW changes by one. This determines the frequency resolution of the DDS for a given system clock frequency. Figure 3.4 shows that the input clock frequency to the DDS is equal to 1 GHz. Thus, if FTW changes by one, the output frequency changes by

$$\Delta f_o = \frac{\Delta FTW \times f_{clk}}{2^N} = \frac{1 \times 1 \times 10^9}{2^{32}} = 0.233 \text{ Hz} \quad (3.2)$$

The minimum value of the frequency divider in the feedback path of the PLL is equal to 8. Therefore, the frequency resolution of the synthesiser is equal to $0.233 \times 8 = 1.864 \text{ Hz}$, which is far within the maximum allowable frequency resolution of 1 MHz given in Table 1.1.

The DDS is fundamentally a sampled system. The sampling frequency of the DAC puts an upper limit on the highest output frequency that can be generated. The sampling theorem states that, to avoid the effect of aliasing, the sampling frequency should at least be twice the bandwidth of the signal that needs to be reconstructed [23].

The spectrum at the output of a DDS is illustrated in Figure 3.7. In this case the system clock frequency is $f_{clk} = 1 \text{ GHz}$, and the fundamental output frequency is equal to $f_{out} = 250 \text{ MHz}$. All other sources of spurious signals have been ignored for clarity.

The *sinc* function shaping the envelope of the spectrum is a result of the zero-order hold circuitry forming part of the DAC at the output of the DDS.

The DDS produces undesired frequency components at

$$f = kf_{clk} \pm f_{out} \quad k = 1, 2, 3, \dots \quad (3.3)$$

The output of a DDS is usually followed by a lowpass filter to remove all the unwanted frequency components present in the output spectrum. The frequency component closest to the desired output is located at $f = f_{clk} - f_{out} = 1 - 0.25 \text{ GHz} = 0.75 \text{ GHz}$. As the fundamental output frequency

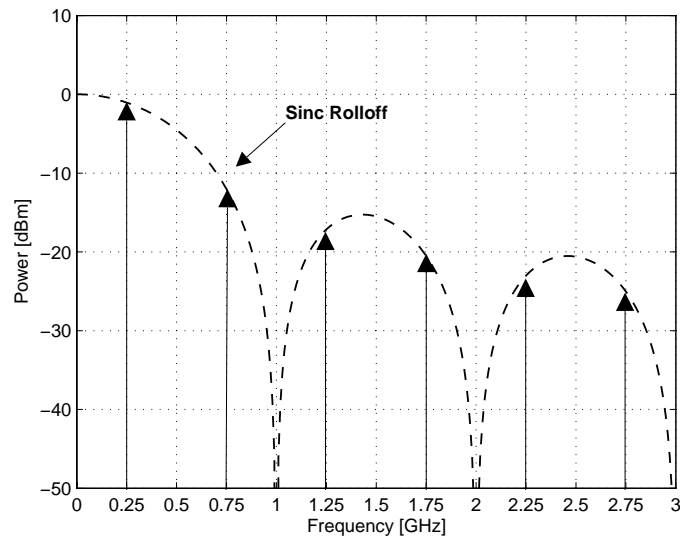


Figure 3.7: A typical DDS spectrum.

increases, the relative frequency difference between these two components decreases. The result is that it becomes increasingly more difficult to suppress the unwanted component significantly with lowpass filtering. For this reason, the output frequency of the DDS is generally limited to about 40% of the system clock frequency. The highest DDS output frequency required is 392.22 MHz, less than 40% of the DDS clock frequency.

Figure 3.4 shows that the DDS output is amplified and filtered with a fifth-order Chebyshev lowpass filter. The filtered signal is presented to a wideband 90° phase shifter which creates the quadrature channels required for the HMC497LP4 quadrature modulator. The *I* and *Q* ports of the modulator are driven differentially, and the bias circuitry adds the necessary direct current (DC) offset required for each channel.

The internal architecture of the HMC497LP4 quadrature modulator, as given in the datasheet, is shown in Figure 3.8.

If perfect quadrature sinusoidal input signals are assumed, and if the LO limiting amplifiers are ignored, the output signal $m(t)$ can be written as

$$\begin{aligned}
 m(t) &= \cos(\omega_{LO}t)I(t) + \sin(\omega_{LO}t)Q(t) \\
 &= \cos(\omega_{LO}t)\cos(\omega_Bt) + \sin(\omega_{LO}t)\cos(\omega_Bt \pm \pi/2) \\
 &= \cos((\omega_{LO} \pm \omega_B)t)
 \end{aligned} \tag{3.4}$$

where $\omega_{LO} + \omega_B$ is known as the upper sideband (USB), and $\omega_{LO} - \omega_B$ is known as the lower sideband (LSB). Thus, depending on the 90° phase relationship between the *I* and *Q* channels, either sideband can be obtained. The use of the quadrature modulator thus eliminates the need of filtering out the undesired sideband obtained with conventional mixing.

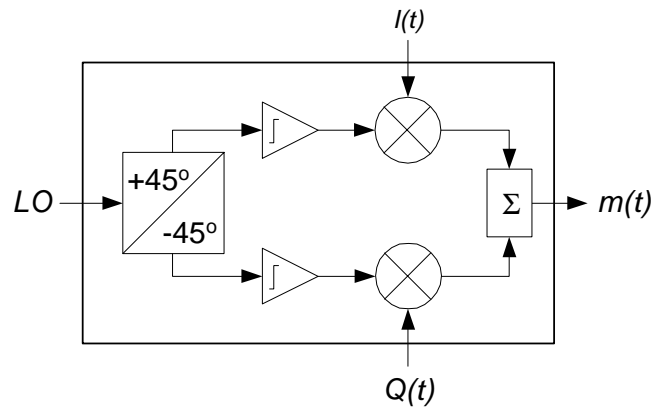


Figure 3.8: Internal architecture of the HMC497LP4 quadrature modulator.

In reality the spectrum consists of many more frequency components than just the one given by Equation 3.4. In general, the frequency spectrum consists of intermodulation (IM) products of the form

$$m\omega_{LO} + n\omega_B \quad (3.5)$$

where $m, n = 0, \pm 1, \pm 2, \pm 3, \dots$. The order of a given product is defined as $|m| + |n|$ [13].

Equation 3.5 shows that both a USB (or sum frequency) and LSB (or difference frequency) component are present in the output spectrum. For an ideal quadrature modulator this is not the case, but imperfections in the modulator, and inaccuracies introduced externally, cause the undesired sideband to be generated. The difference in decibels between the desired sideband power and the undesired sideband power, is known as *sideband suppression*. The sideband suppression of the HMC497LP4 quadrature modulator is presented in Chapter 7.

Chapter 2 showed that the noise contribution of the HMC439QS16G PFD is minimised by using the highest possible reference frequency input to the PFD. For this reason, a PFD reference frequency of 1 GHz was chosen which lies safely within the maximum operating frequency of the PFD, and at the same time, is equal to the maximum sampling rate of the DDS. The high DDS clock frequency enables the DDS to produce the high frequency output signals required.

Either one of the two frequency dividers in the feedback path of the PLL is selected by using two digitally controlled switches. The choice between the two dividers gives a degree of freedom with regard to managing undesired mixing products obtained at the output of the quadrature modulator. Mixing products that lie far outside the loop bandwidth of the PLL are suppressed significantly by the frequency response of the PLL and are not usually of any concern. However, those within the loop bandwidth are actually phase amplified to the output of the PLL and may in certain cases exceed the acceptable spurious-free dynamic range (SFDR) .

Switching between the dividers changes the offset frequencies in the loop, causing a different set of mixing products to be generated. In certain cases, switching between the dividers causes higher-order, and hence generally lower level, mixing products to be generated for the same output fre-

quency. In such a case, choosing the divider that yields higher order products generally leads to lower level spurious products in the output spectrum.

Figure 3.9 shows the loop filter used in conjunction with the differential output of the HMC439QS16G PFD.

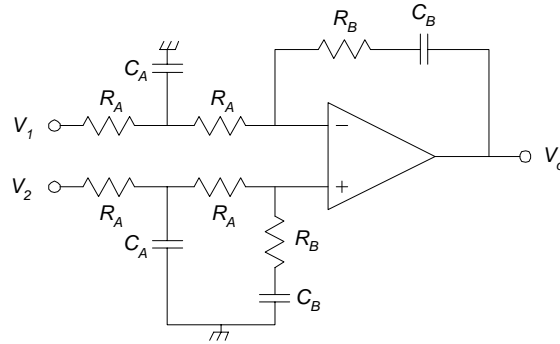


Figure 3.9: Circuit diagram of the loop filter used for the synthesiser.

The transfer function of the loop filter, which is derived in Chapter 6, takes the form of that given in Equation 3.6.

$$F(s) = \frac{V_o}{V_2 - V_1} = \frac{s(R_B C_B) + 1}{s(2R_A C_B) \left(s \left(\frac{R_A C_A}{2} \right) + 1 \right)} \quad (3.6)$$

Since all the parameters of the PLL are fixed and specific to the components used, the loop filter is the only component that gives a degree of freedom with regard to the design of the PLL. The values of R_A , R_B , C_A and C_B ultimately set the loop bandwidth and phase margin of the PLL and are computed in Chapter 6 for optimal phase noise performance.

The low noise *Hittite* VCO shown in Figure 3.4 is tunable over a frequency range of approximately 4 – 8 GHz, covering the total frequency range required for the LO. It has an internal buffer amplifier providing isolation between the VCO and the rest of the circuit.

The previous chapter showed that the VCO is the major contributor of phase noise outside the loop bandwidth of the PLL. A VCO with low phase noise is critical for low noise PLL design, since the free-running phase noise of the VCO influences the optimal loop bandwidth of the PLL. If the PLL is designed for optimal phase noise performance, a VCO with high phase noise requires a wide loop bandwidth. Although this results in faster transient response, it degrades phase noise performance.

A resistive power divider, consisting of three 16 Ω resistors, is used as an equal power splitter at the output of the VCO. The inherent wideband characteristic of this power divider is ideal for the $\frac{7.47-5.47}{6.47} \times 100 = 30.91\%$ of bandwidth required.

Two stages of amplification are required at the output of the synthesiser to obtain the desired output power. Out-of-band spurious signals and VCO harmonics at the output of PLL are suppressed with a fifth-order interdigital Chebyshev filter.

3.3 Conclusion

This chapter presented a qualitative description of the indirect frequency synthesiser which was introduced in block diagram form. The roles of some important components of the synthesiser were explained, and the reasoning behind some choices of components was motivated.

The next step is to design and characterise the components required for the frequency synthesiser that are not purchased off-the-shelf. This is the topic of Chapter 4 and Chapter 5 which are dedicated to the design and characterisation of the multiplier and microwave filters, respectively.

To conclude this chapter, the complete block diagram of the frequency synthesiser is depicted in Figure 3.10.

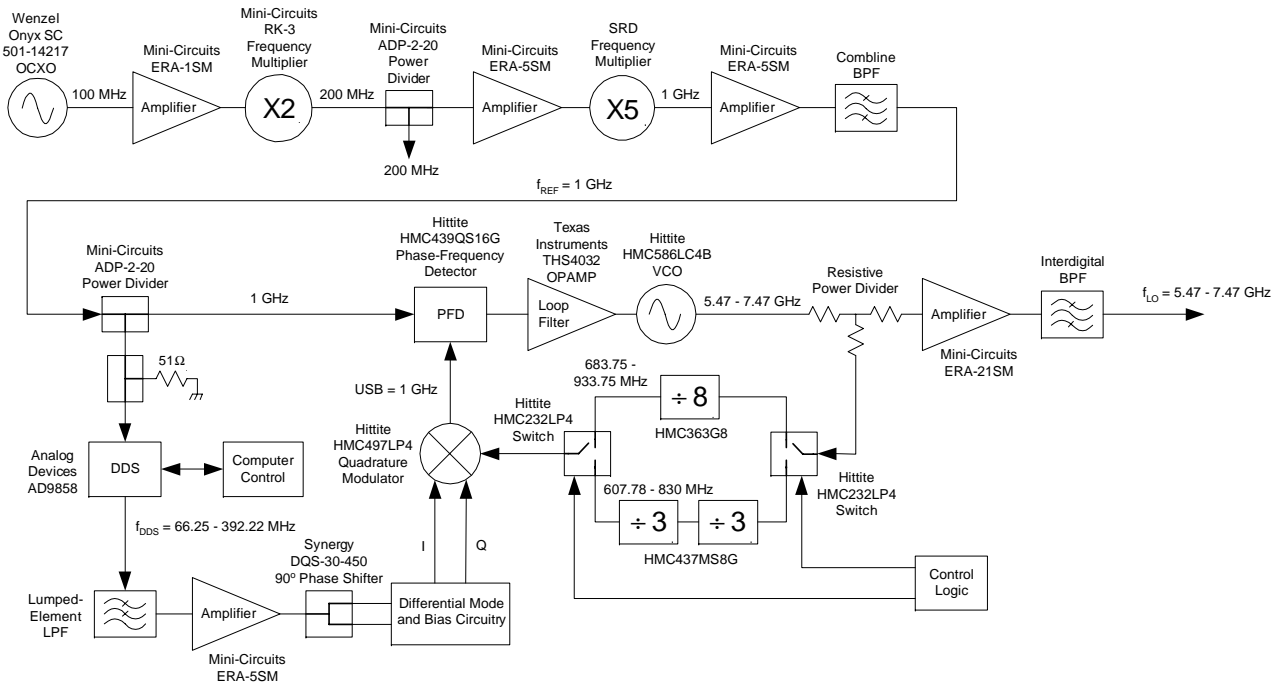


Figure 3.10: Block diagram representation of the complete indirect frequency synthesiser.

Chapter 4

Design and Measured Response of an SRD Frequency Multiplier

4.1 Introduction

A frequency multiplier, as defined by the IEEE standard dictionary of electrical and electronics terms, is a device for delivering output power at a frequency that is an exact positive integer (except 0 and 1) multiple of an input frequency [24].

Frequency multipliers can be realised with both active and passive devices. Active multipliers, in contrast to passive multipliers, offer wide bandwidth and can achieve conversion gain. In addition, they require low input drive levels and have improved isolation between ports [25, 26, 27]. The greatest disadvantages of active multipliers compared to reactive, passive multipliers are, higher noise, and the difficulty in the generation of high or odd-order harmonics [22, 28].

Harmonic generation with active FET multipliers is usually obtained by some form of drain current clipping. This can be achieved by biasing a FET below pinch-off. The sinusoidal input signal, which is applied to the gate, turns the transistor on over a part of its cycle, creating a drain current waveform that is rich in harmonics. The desired harmonic is filtered at the output. Bipolar transistors can also be used for frequency multiplication, with the capacitance of the collector-base junction providing the necessary nonlinearity [25, 29].

Passive multipliers on the other hand are known for their simple circuit topologies and their ability to operate at high frequencies. Although passive multipliers cannot achieve conversion gain, it is partly compensated for by low or zero DC power consumption [29].

Passive diode frequency multipliers can be classified as resistive and reactive types [25, 29]. Resistive frequency multipliers generally exploit the nonlinear I/V characteristic of a forward biased Schottky-barrier diode to distort the input sinusoidal signal, leading to the generation of harmon-

ics [22]. Resistive multipliers are significantly less efficient compared to reactive multipliers and are rarely used for generating harmonics greater than the second. This is due to their efficiency which decreases rapidly as the harmonic number increases. Page proved that the optimum efficiency of a resistive frequency multiplier can be no greater than $1/n^2$, where n is the harmonic number [30]. A resistive frequency doubler will therefore exhibit conversion loss of at least $\left|10 \log_{10} \left(\frac{1}{2^2}\right)\right| = 6.02$ dB. In reality, resistive doublers rarely have conversion loss below about 10 dB [22].

Resistive multipliers have one significant advantage in that they can be made very broadband. This characteristic is inherent to the non frequency-dependent nature of the resistive nonlinearities (I/V) that are employed in the generation of the harmonics. Usually, the bandwidth of resistive multipliers is limited primarily by external circuitry such as matching networks, not by the diodes themselves [25, 29].

Reactive frequency multipliers use the nonlinear reactance of varactors¹ or step-recovery diodes (SRDs) to generate harmonics of the input signal. Most varactors are *pn*-junction devices, but Schottky-barrier diodes having metal-to-semiconductor junctions are occasionally used as well [22]. In both cases, the nonlinear reactance is the depletion capacitance under reverse bias. This nonlinearity is not very strong, and for this reason, varactors are used primarily for low-order multiplication, rarely over four times the source frequency. This is in contrast with SRDs, which exhibit very strong C/V nonlinearities, making them ideal for high-order frequency multiplication [22, 25, 31].

The reactive nature of varactors and SRDs make them inherently narrowband. Reactive multipliers, in contrast with resistive multipliers, are extremely sensitive to circuit parameters such as tuning reactances, bias voltage and input power, and have a well deserved reputation of being difficult to optimise [25, 29].

The major advantage of reactive multipliers compared to other frequency multipliers is that, because it is a reactive device, it generates very little noise. This is particularly valuable in cases where low phase noise is desired, such as in local oscillator sources for radar applications [25]. This advantage in itself may be reason enough for using a reactive multiplier, rather than any other type. Reactive frequency multipliers are furthermore preferably used in cases where odd harmonics are needed, or where very high harmonics must be generated from a low-frequency source [22]. In the latter case, the SRD is ideal. One of the most outstanding characteristics of the SRD is the high conversion efficiency with high frequency multiplication order [32].

This chapter outlines the design and measured response of a reactive, SRD frequency multiplier that forms part of the multiplier chain shown in Figure 3.2. The narrow bandwidth, low noise, and the high, odd-order of multiplication required, favors the use of the SRD. Also, since the SRD is essentially a reactive device, low conversion loss can be expected. Section 4.2 briefly describes the SRD behaviour and introduces the circuit model used for the design of the multiplier in Section 4.3. The penultimate section shows and discusses the measured response of the reactive multiplier.

¹The term is derived from the words *variable* and *reactor*. A varactor is a voltage-variable reactance.

4.2 Step-Recovery Diode Behaviour and Circuit Model

The SRD, which is to first-order an ideal nonlinear capacitor, is a device which has found application in waveshaping, harmonic generation, division, switching, sampling, and up-conversion. As a recognised semiconductor device, it has only been in existence since the late 1950s. In 1959, Leenov and Uhler first discussed the possibility of efficient harmonic generation using ideal nonlinear capacitors. During the same time Boff empirically discovered the step-recovery effect in a circuit designed to produce high-order harmonics that exceeded any of the then existing theories. Since the 1960s when the devices became readily available, numerous papers were published discussing the step-recovery phenomenon and its related circuit applications [33, 34].

The SRD, also occasionally referred to as the snap-off or charge-storage diode, is a pn -junction device with a thin, essentially intrinsic² (i) layer centered between the heavily doped p and n semiconductors, forming a pin device [32, 33, 36].

When the SRD is forward biased, majority carrier electrons³ from the n -region and majority carrier holes from the p -region diffuse into the i -layer. Almost any amount of charge can be stored at constant voltage [25, 33, 36]. The electrons and holes are stored in the i -region for a mean time equal to the *minority carrier lifetime* (t_1), after which electrons and holes start to recombine in a process known as *electron-hole recombination*. The minority carrier lifetime of SRDs is usually specified by the manufacturer. For times considerably shorter than the minority carrier lifetime, the quantity of stored charge at virtually constant voltage is associated with a large capacitance ($C = \frac{Q}{V}$), known as the *diffusion capacitance* [25, 33, 36]. For a reverse voltage to be possible, the stored charge must first be removed by reverse current. If the minority carrier lifetime is long compared to the inverse of the excitation frequency, essentially no charge recombines and virtually all the stored charge is recoverable [25, 31, 33].

Under reverse bias, the stored minority carriers that do not recombine are depleted until all the charge stored in the i -layer has been removed. At this stage, the SRD switches very abruptly from the diffusion capacitance state to a small depletion capacitance state which is essentially independent of reverse voltage [25, 36]. Since the diffusion capacitance under forward bias is a result of having a large number of free carriers in a finite volume, the transition from the diffusion to the depletion capacitance state cannot be expected to be instantaneous. Moll and Hamilton have empirically found that the switching time (t_t) can be approximated by accounting 10 ps for every micron width of the i -layer [33]. SRDs have typical i -layer widths in the range of 0.5 to 4 microns, thus having switching times in the order of 5 ps to 40 ps.

From the preceding two paragraphs, it is clear that the SRD can in the ideal case be modelled as a nonlinear, two-state capacitor of large (effectively infinite) diffusion capacitance under forward

²An intrinsic semiconductor is a single-crystal semiconductor material with no other types of atoms within the crystal. This is in contrast with extrinsic semiconductors that contain impurity atoms, i.e. p -type and n -type semiconductors [35].

³In a n -type semiconductor, electrons are called the *majority carriers* because they far outnumber the holes, which are termed the *minority carriers* [35].

bias, and a small, depletion capacitance under reverse bias, with zero switching time between states [25, 33, 36]. The ideal model of the SRD is shown in Figure 4.1, where V_λ is the contact potential. The extent to which the ideal model is an accurate representation depends strongly on the minority carrier lifetime (t_l), the switching time (t_s), and the lowest and highest operating frequencies in the circuit associated with the SRD. According to Moll and Hamilton, the model in Figure 4.1 is valid in the frequency range of $1/t_l < f < 1/t_s$. For frequencies lower than $1/t_l$, one must take into account the finite recombination effects and at frequencies higher than $1/t_s$, the effects of finite switching time [33]. The ideal model assumes that the SRD has

- Infinite capacitance under forward bias.
- Constant depletion capacitance under reverse bias.
- Negligible series resistance.
- Negligible parasitic elements.

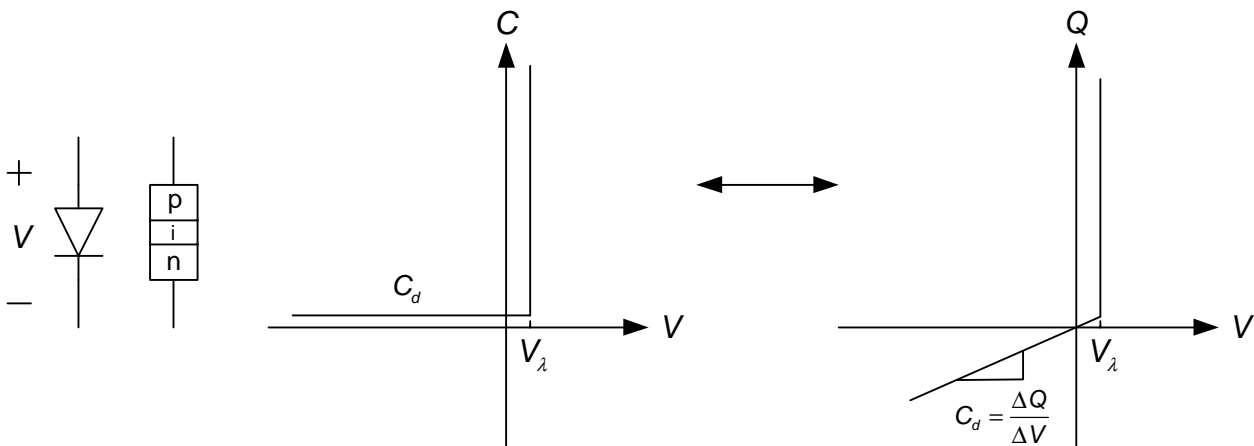


Figure 4.1: Ideal SRD circuit model.

Analysis of resonant and nonresonant circuit performance using the piecewise linear model shown in Figure 4.1 describe the first-order diode behaviour very well [33].

While a conventional pn -junction varactor only makes modest use of charge-storage capacitance, the SRD uses it almost exclusively, in fact, this is the main difference between these two devices [22]. Schottky-barrier diodes do not store charge at all. The current in a pn -junction and SRD is controlled by the diffusion of minority carriers, while the current of a Schottky-barrier diode results from the flow of majority carriers across the metallurgical junction, that is, the interface where the metal and the moderately doped n -type semiconductor makes contact. This means that there is no minority carrier storage in a Schottky diode, so the switching time from forward bias to reverse bias is very short compared to that of an SRD or pn -junction diode [35].

4.3 Frequency Multiplier Design

The design of the frequency multiplier discussed in this section follows the same general approach as described in the paper by Johnston and Boothroyd [37]. The theory presented by them, which only considers one ideal nonlinear charge-storage element for frequency multiplication, is extended in this chapter to the case where two SRDs in anti-parallel are considered. The anti-parallel combination of diodes suppresses even-order harmonics ensuring a more spectrally clean output, thereby alleviating the combline filter specification at the output of the multiplier chain. The analysis of the multiplier in Johnston and Boothroyd's paper is furthermore limited to finding only the real parts of the large-signal input and output impedances of the nonlinear circuit. In the design of the frequency multiplier outlined in this chapter, both the resistance and reactance of the input and output impedances are taken into consideration. This allows optimal input and output impedance matching, minimising conversion loss.

Figure 4.2 shows a photo of the BAT18 *pin* diode from *Philips* used for the multiplier design. Although the BAT18 diode is not an SRD, it behaves like one at the operating frequencies considered here and serves as an inexpensive and suitable alternative to a real SRD.

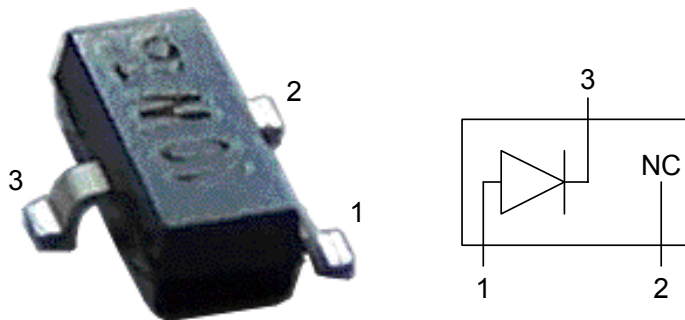


Figure 4.2: The BAT18 *pin* diode in the SOT23 package type.

The BAT18 diode has a minority carrier lifetime (t_l) of 120 ns and an *i*-layer width of 3 μm , therefore having a switching time (t_t) in the order of $3 \times 10 \text{ ps} = 30 \text{ ps}$ according to Moll and Hamilton's empirical approximation. The frequency band over which the idealised model of Figure 4.1 is a very good description of the BAT18 behaviour, is shown in Figure 4.3 [33]. Note that the input and output frequencies of the frequency multiplier (200 MHz and 1 GHz, respectively) designed in this chapter lie safely within the frequency band depicted in Figure 4.3.

Figure 4.4 shows the circuit topology of the multiplier. The fundamental input signal which is applied to the nonlinear circuit, results in the generation of harmonics. The matching networks matches the large-signal impedances of the nonlinear circuit at the fundamental frequency and fifth harmonic to the source and load impedances, respectively.

Collectively, the nonlinear part of the circuit is comprised of the two anti-parallel SRDs, the DC voltage source and the linear capacitor C_p which appears in parallel with the SRDs. The characteristic

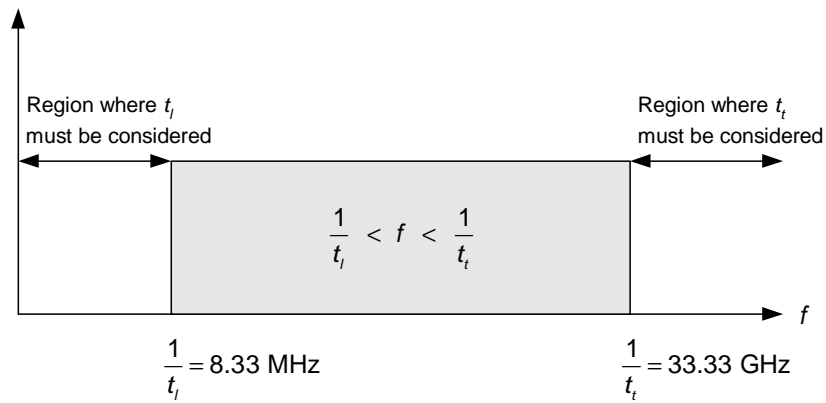


Figure 4.3: Frequency band over which the nonlinear SRD model of Figure 4.1 is valid for the BAT18 diode.

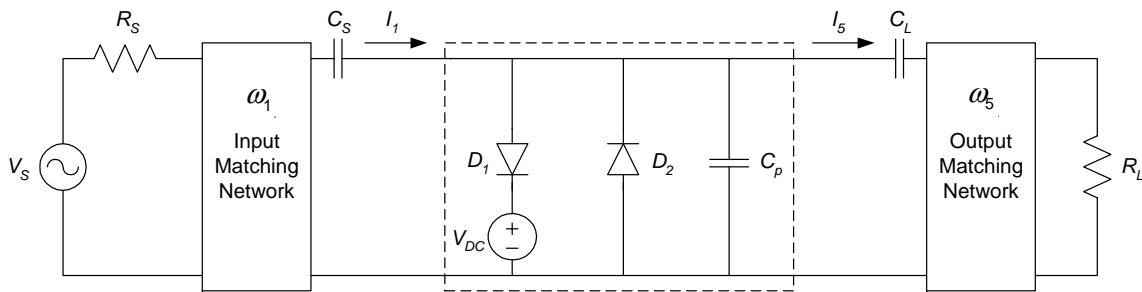


Figure 4.4: SRD frequency multiplier circuit topology.

Q/V line of the nonlinear circuit is shown in Figure 4.5, where V_λ is the contact potential of the SRDs, and C_d is the depletion capacitance of the SRDs.

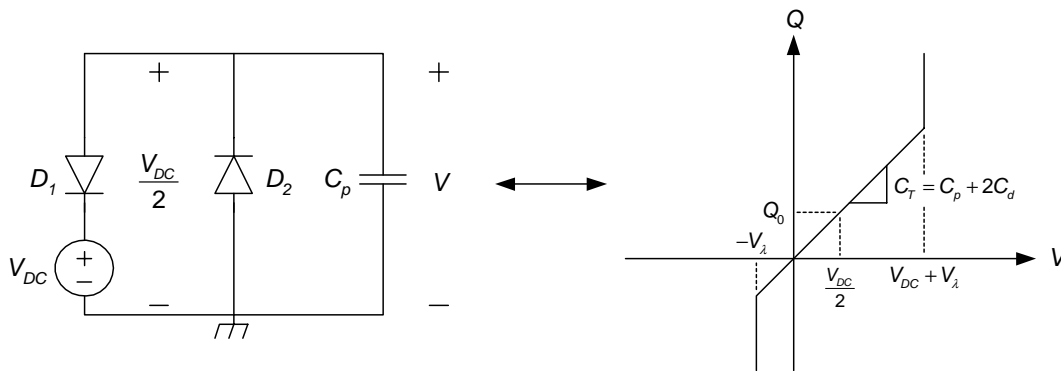


Figure 4.5: Piecewise linear model of the nonlinear circuit.

Within the voltage range of $-V_\lambda < V < V_{DC} + V_\lambda$, both SRDs are reverse biased and the depletion capacitance C_d of each SRD adds to the linear capacitor (C_p) in parallel with the SRDs. The linear capacitor C_p gives some control over the slope of the characteristic Q/V line, and has an effect on the large-signal input and output impedances of the nonlinear circuit. When $V > V_{DC} + V_\lambda$, D_1 switches to the diffusion capacitance state under which any quantity of charge can be stored at constant voltage. The same is true for $V < -V_\lambda$, when D_2 becomes forward biased.

Performing a DC analysis on the circuit of Figure 4.4 shows that the SRDs are connected in series. The DC voltage V_{DC} divides equally between the two SRDs, resulting in $V_{DC}/2$ across each diode. Note that this point lies exactly in the middle of the characteristic Q/V line, as shown in Figure 4.5. As a result, the time-varying voltage and charge waveforms swing symmetrically around the centre point. Thus, from an AC perspective, the centre point of the characteristic Q/V line can be shifted to the origin of the axis, as shown in Figure 4.6. This is done to simplify the analysis.

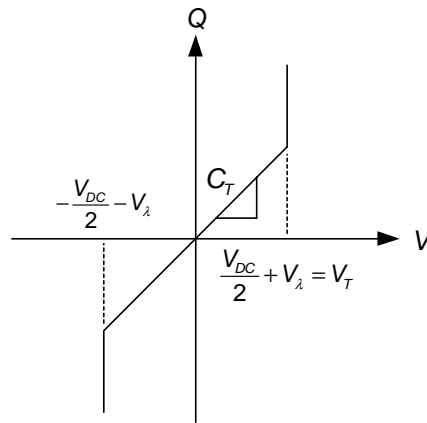


Figure 4.6: Centre point of the characteristic Q/V line moved to the origin.

The voltage, as a function of charge, can be expressed as

$$v = \begin{cases} V_T & \cdots & q \geq C_T V_T \\ \frac{q}{C_T} & \cdots & -C_T V_T < q < C_T V_T \\ -V_T & \cdots & q \leq -C_T V_T \end{cases} \quad (4.1)$$

In order to simplify the design of the frequency multiplier, it is assumed that only the fundamental and fifth harmonic current components are applied to the nonlinear circuit (see Figure 4.4). This may seem like an oversimplification, as other harmonics besides the fifth are also generated by the nonlinear circuit. However, as a result of the anti-parallel combination of SRDs, all even-order harmonic currents circulate only between the diodes, ideally never reaching the source or load. Of course in practice, due to the slight difference between diodes and imperfect balance in the circuit, some even-harmonic power will reach the load, but compared to the desired harmonic output, is insignificant. The input and output matching circuits furthermore present a relatively high impedance to unwanted odd-order harmonics of significance, preventing large undesired odd-order harmonic currents to flow to the source and load. The assumption that only the fundamental and fifth harmonic currents are applied to the nonlinear circuit, is thus fairly accurate.

To start the analysis of the multiplier, assume that the charge waveform of the nonlinear circuit, takes the form of Equation 4.2,

$$q(t) = Q_1 \cos(\omega t) + Q_n \sin(n\omega t) \quad (4.2)$$

where n is the multiplication factor, $\omega = 2\pi f$, and Q_1 and Q_n are constants. Note that the harmonic charge component is 90° out of phase with respect to the fundamental component. The implications of this relationship will become clear after some further analysis.

The current is found by taking the time-derivative of the charge, that is

$$i(t) = \frac{dq(t)}{dt} = -Q_1\omega \sin(\omega t) + n\omega Q_n \cos(n\omega t) = I_1 \sin(\omega t) + I_n \cos(n\omega t) \quad (4.3)$$

where

$$I_1 = -Q_1\omega \quad \text{and} \quad I_n = n\omega Q_n \quad (4.4)$$

Solving Equation 4.4 for Q_1 and Q_n and substituting back into Equation 4.2, yields

$$q(t) = \left(\frac{-I_1}{\omega}\right) \cos(\omega t) + \left(\frac{I_n}{n\omega}\right) \sin(n\omega t) \quad (4.5)$$

In this analysis, it is assumed that the SRDs only change state (depletion to diffusion capacitance state or vice versa) when the harmonic charge component is zero, and that each SRD changes state only twice per fundamental cycle. The harmonic charge component is zero when

$$\begin{aligned} n\omega t &= m\pi & m &= \pm 0, 1, 2, \dots \\ \therefore t &= \frac{m\pi}{\omega n} \end{aligned} \quad (4.6)$$

Figure 4.6 shows that for either SRD to change state, the charge at $t = \frac{m\pi}{\omega n}$ must be equal to

$$q\left(t = \frac{m\pi}{\omega n}\right) = \left(\frac{-I_1}{\omega}\right) \cos\left(\frac{m\pi}{n}\right) = \pm C_T V_T \quad (4.7)$$

Rearranging terms in Equation 4.7 yields

$$I_1 = \pm \frac{C_T V_T \omega}{\cos\left(\frac{m\pi}{n}\right)} \quad (4.8)$$

To ensure that each SRD does not change state more than twice per fundamental cycle, it is required that the absolute value of the slope of the harmonic charge component at $t = \frac{m\pi}{\omega n}$ must not be greater than the absolute value of the slope of the fundamental charge at the same time instant. Expressed mathematically,

$$\begin{aligned}
 \left| \frac{dq_n}{dt} \right|_{t=\frac{m\pi}{\omega n}} &\leq \left| \frac{dq_1}{dt} \right|_{t=\frac{m\pi}{\omega n}} \\
 \therefore |I_n \cos(m\pi)| &\leq \left| I_1 \sin\left(\frac{m\pi}{n}\right) \right| \\
 \therefore |I_n| |\cos(m\pi)| &\leq |I_1| \left| \sin\left(\frac{m\pi}{n}\right) \right| \\
 \therefore \frac{|I_n|}{|I_1|} &\leq \sin\left(\frac{m\pi}{n}\right) \quad 0 < m < n \\
 \therefore \frac{|I_n|}{|I_1|} &\leq \sin\left(\frac{m\pi}{n}\right) \quad 0 < m < n \\
 \therefore I_n &\leq I_1 \sin\left(\frac{m\pi}{n}\right) \quad 0 < m < n
 \end{aligned} \tag{4.9}$$

To illustrate the effect of different I_n magnitudes on the voltage waveform and the way the SRDs switch between states, three cases are investigated,

1. $I_n < I_1 \sin\left(\frac{m\pi}{n}\right)$
2. $I_n = I_1 \sin\left(\frac{m\pi}{n}\right)$
3. $I_n > I_1 \sin\left(\frac{m\pi}{n}\right)$

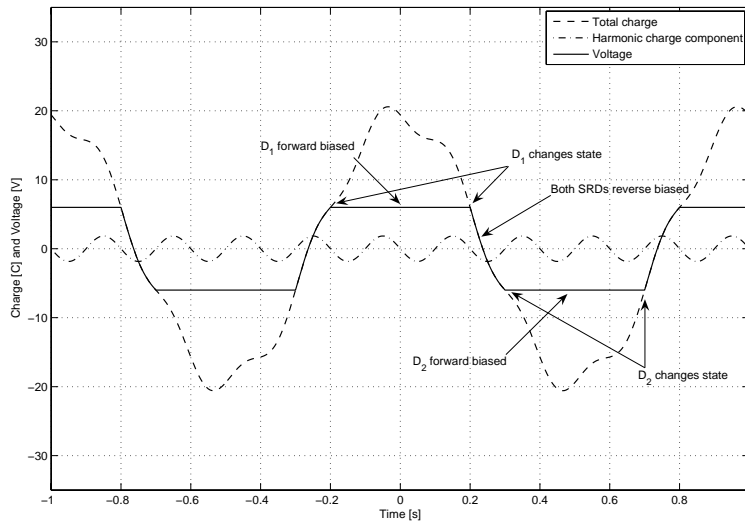


Figure 4.7: Nonlinear circuit charge and voltage waveforms as a function of time ($I_n = 0.5I_1 \sin\left(\frac{m\pi}{n}\right)$).

For the first case, $I_n = 0.5I_1 \sin\left(\frac{m\pi}{n}\right)$. Figure 4.7 shows the charge and voltage waveforms of the nonlinear circuit as a function of time. The voltage is defined by Equation 4.1. For all three cases considered, $f = 1$ Hz, $V_T = 6$ V, $C_T = 1$ F, $m = 2$, $n = 5$ and $I_1 = -\frac{C_T V_T \omega}{\cos\left(\frac{m\pi}{n}\right)}$. Note that, as expected,

each SRD only switches state twice per fundamental cycle. Also note that each SRD only changes state when the harmonic charge component is zero.

For the second case, $I_n = I_1 \sin\left(\frac{m\pi}{n}\right)$. This is the maximum permissible value of I_n according to Equation 4.9, as a larger value of I_n will result in the SRDs to switch more than twice per fundamental cycle. Figure 4.8 shows the corresponding waveforms. The total current is also shown, and for this example has been decreased by a factor 10 to fit nicely onto the figure.

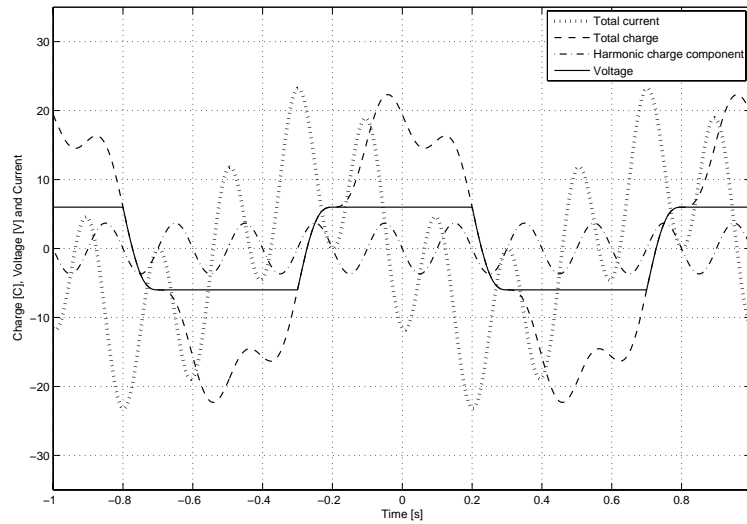


Figure 4.8: Nonlinear circuit charge, current and voltage waveforms with $I_n = I_1 \sin\left(\frac{m\pi}{n}\right)$.

A lot of insight can be gained from Figure 4.7 and Figure 4.8. According to Equation 4.5, a larger harmonic current constant (I_n) results in a larger harmonic charge component. Comparing Figure 4.7 to Figure 4.8 shows that a larger harmonic charge component which adds to the even fundamental charge component causes the total charge function, and hence the corresponding voltage waveform, to become a more odd function. The fundamental input power is directly proportional to the product of the fundamental voltage component in-phase with the fundamental *sin* current component (see Equation 4.3). For this reason, a larger harmonic charge component yields more real input power, or a larger real value of nonlinear circuit input impedance. For the case where $I_n = 0$ (no harmonic generation), the fundamental frequency voltage and current components are orthogonal. In this case, the nonlinear circuit appears reactive at the fundamental input frequency and no real power is delivered to the nonlinear circuit.

The 90° phase relationship between the fundamental charge and harmonic charge component can now also be understood. One might argue that a harmonic charge component $Q_n \cos(n\omega t)$ could also have been chosen, but closer investigation shows that this would result in an even charge function (the sum of two even functions is even [38]), and hence an even voltage waveform, in quadrature with the fundamental current (*sin*) component.

The charge-storage property of the SRD under forward bias is clearly illustrated in Figure 4.8. Note for example that when D_1 is in the diffusion capacitance state ($t = -0.2$ s to $t = 0.2$ s), the total charge increases and decreases under constant voltage, and the voltage stays constant even for short durations of negative current. This is the fundamental difference between an ideal rectifying diode and the SRD. The voltage of an ideal rectifier changes at the instant the applied current polarity changes. The SRD only switches from the diffusion capacitance state to the depletion state when all the stored charge is removed by reverse current. Only then is a reverse voltage across the diode possible.

For the final case $I_n = 1.5I_1 \sin\left(\frac{m\pi}{n}\right)$. Figure 4.9 shows the waveforms. Note that both SRDs change state more than twice per fundamental cycle, as expected. This mode of operation will not be considered and it will be assumed that I_n always obeys Equation 4.9.

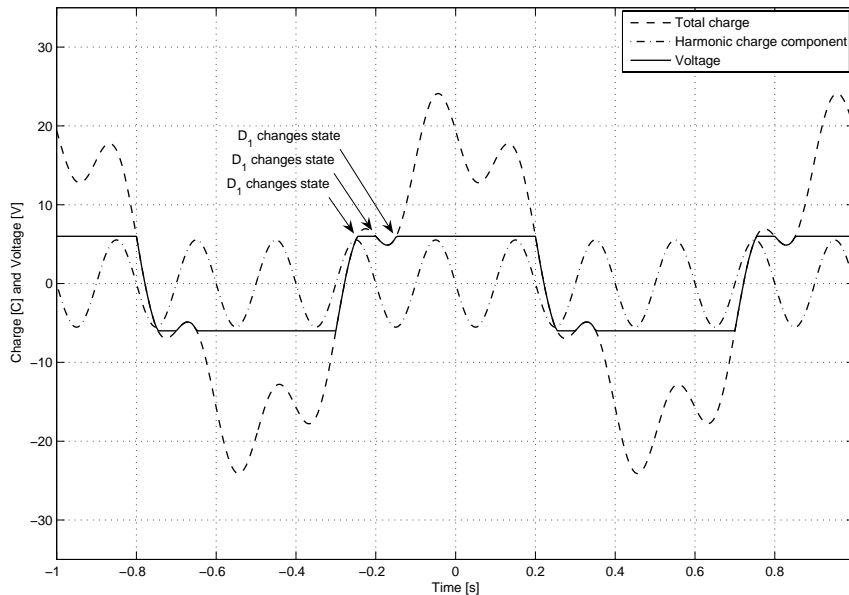


Figure 4.9: Nonlinear circuit charge and voltage waveforms with $I_n = 1.5I_1 \sin\left(\frac{m\pi}{n}\right)$.

In the foregoing analysis it was assumed that the SRDs only change state when the harmonic charge component becomes zero. Since the value of m determines at which zero crossing the state of the SRD changes, the duration of time each SRD is forward biased is also dependent on the value of m . In fact, the duration of time each SRD is forward biased is double that given by Equation 4.6, that is,

$$t_c = 2 \left(\frac{m\pi}{\omega n} \right) = 2 \left(\frac{m\pi}{2\pi f n} \right) = \frac{mT}{n} \quad \text{for } m = 1, 2 \quad (4.10)$$

Thus for the previous example with $f = 1$ Hz, $m = 2$, $n = 5$ and $I_n \leq I_1 \sin\left(\frac{m\pi}{n}\right)$, $t_c = \frac{2 \times 1}{5} = 0.4$ s. The duration of time both SRDs are in the depletion state is 0.1 s, half the period of the fifth harmonic.

Figure 4.10 shows the case for which $m = 1$ and $I_n = I_1 \sin\left(\frac{m\pi}{n}\right)$. All the other parameters are the same. In this case, each SRD is forward biased for $t_c = \frac{1}{5} = 0.2$ s.

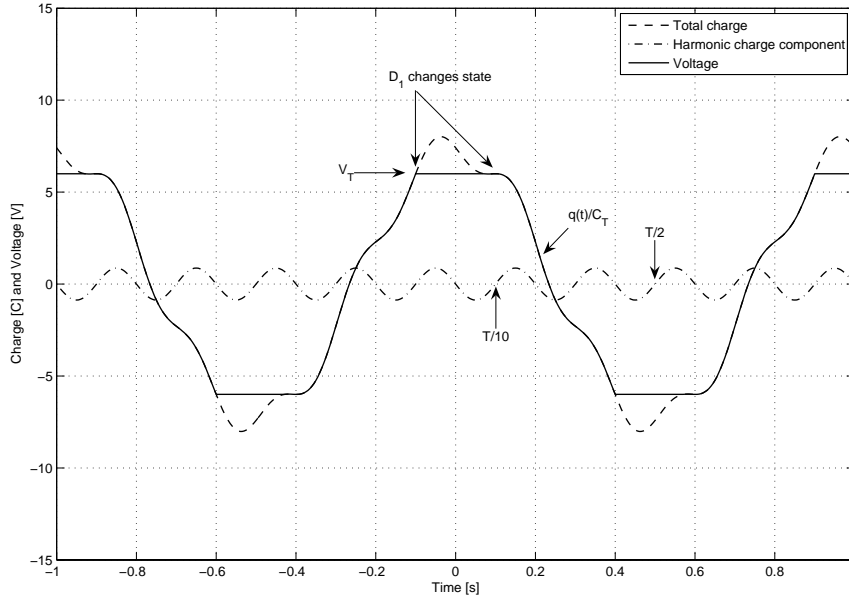


Figure 4.10: Nonlinear circuit charge and voltage waveforms ($m = 1$ and $I_n = I_1 \sin\left(\frac{m\pi}{n}\right)$).

In order to match the nonlinear circuit to the source and load, the large-signal driving point impedances need to be calculated. It is defined in a similar manner as a linear impedance, i.e. [25],

$$Z(\omega) = \frac{V(\omega)}{I(\omega)} \quad (4.11)$$

The voltage components in-phase and quadrature with the fundamental and harmonic current can be found with Fourier analysis. For a periodic function $f(t)$ with fundamental frequency $f = \frac{1}{T}$, Fourier showed that $f(t)$ can be expressed as

$$f(t) = \frac{a_0}{2} + \sum_{k=1}^{\infty} (a_k \cos(k\omega t) + b_k \sin(k\omega t))$$

where

$$a_k = \frac{2}{T} \int_{t_0}^{t_0+T} f(t) \cos(k\omega t) dt$$

$$b_k = \frac{2}{T} \int_{t_0}^{t_0+T} f(t) \sin(k\omega t) dt \quad (4.12)$$

Note that the voltage waveforms shown in Figure 4.7, Figure 4.8 and Figure 4.10 all exhibit half-wave symmetry, that is

$$f(t) = -f(t - T/2) \quad (4.13)$$

For a periodic function with half-wave symmetry, the Fourier coefficients reduce to

$$\begin{aligned}
 a_0 &= 0 \\
 a_k &= b_k = 0 && \text{for } k \text{ even} \\
 a_k &= \frac{4}{T} \int_0^{T/2} f(t) \cos(k\omega t) dt && \text{for } k \text{ odd} \\
 b_k &= \frac{4}{T} \int_0^{T/2} f(t) \sin(k\omega t) dt && \text{for } k \text{ odd}
 \end{aligned} \tag{4.14}$$

Note that, as a result of the anti-parallel SRDs, the voltage waveform contains no even-order Fourier coefficients.

The current applied to the nonlinear network is given by Equation 4.3, and is given again below

$$i(t) = I_1 \sin(\omega t) + I_n \cos(n\omega t) \tag{4.15}$$

The large-signal input and output impedances are expressed as

$$Z_1 = \frac{|b_1| - j|a_1|}{|I_1|} \tag{4.16}$$

and

$$Z_n = \frac{|a_n| - j|b_n|}{|I_n|} \tag{4.17}$$

Thus in general, with Figure 4.10 as a reference and $I_1 = -\frac{C_T V_T \omega}{\cos(\frac{m\pi}{n})}$ (Equation 4.8), and I_n given by Equation 4.9, the fundamental voltage component in phase with the fundamental current is given by

$$\begin{aligned}
 b_1 &= \frac{4}{T} \int_0^{T/2} v(t) \sin(\omega t) dt \\
 &= \frac{4}{T} \int_0^{\frac{mT}{2n}} V_T \sin(\omega t) dt + \frac{4}{T} \int_{\frac{mT}{2n}}^{\frac{T}{2} - \frac{mT}{2n}} \frac{q(t)}{C_T} \sin(\omega t) dt + \frac{4}{T} \int_{\frac{T}{2} - \frac{mT}{2n}}^{\frac{T}{2}} -V_T \sin(\omega t) dt
 \end{aligned} \tag{4.18}$$

which is valid for $m = 1, 2$. Although a closed form solution exists for b_1 and the other Fourier coefficients, it requires a lot of tedious mathematics. Instead, *Matlab* is used for evaluating the integrals numerically.

Table 4.1 shows the input and output impedances calculated with *Matlab* for two different conduction angles m , and two different magnitudes of I_n . The *Matlab* code can be found in Appendix B. The multiplier parameters are, $f = 200$ MHz, $n = 5$, $V_T = 6$ V, $C_T = 4$ pF, and $I_1 = -\frac{C_T V_T \omega}{\cos(\frac{m\pi}{n})}$.

Substituting different values of V_T into the integrals reveals that the input and output impedances

are independent of V_T , as long as Equation 4.8 holds. However, since V_T is directly proportional to I_1 , increasing or decreasing V_T requires more or less fundamental input power, respectively.

The depletion capacitance of the BAT18 diode is approximately 1 pF. Therefore, C_p is chosen as 2 pF to make up the total capacitance of $C_T = 4$ pF. Increasing the value of C_p results in decreased values of input and output resistance. Since the resistances are already quite low, a larger value of C_p is not desirable.

Table 4.1: Large-signal driving input and output impedances of the nonlinear circuit.

m	$I_n = kI_1 \sin\left(\frac{m\pi}{n}\right)$	Z_1 [Ω]	Z_5 [Ω]
1	$k = 0.5$	$1.82 - j179.59$	$21.11 - j23.87$
1	$k = 1$	$3.65 - j179.59$	$10.55 - j23.87$
2	$k = 0.5$	$4.77 - j77.01$	$21.11 - j7.96$
2	$k = 1$	$9.55 - j77.01$	$10.55 - j7.96$

It is clear from Table 4.1 that a conduction angle of $m = 2$ and maximum harmonic current are preferable. This leads to a real part of input impedance that is most practical to match to the source impedance of 50Ω . Note that according to Equation 4.9, $m = 3$ and $m = 4$ are also valid. However, evaluation of the integrals leads to the same impedance levels as for $m = 2$ and $m = 1$, respectively.

The nonlinear frequency multiplier can thus be divided into two linear circuits as depicted in Figure 4.11.

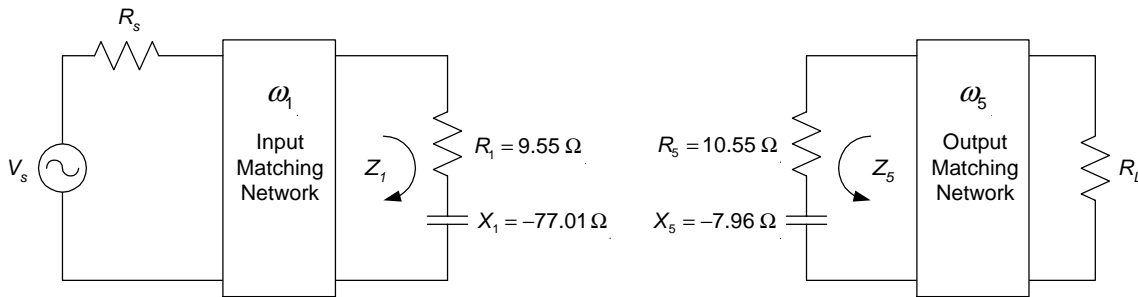


Figure 4.11: Nonlinear multiplier circuit divided into two linear circuits.

The first element of the input matching network is a shunt capacitor which appears in parallel with the source impedance, R_S .

The parallel circuit can be transformed to an equivalent series circuit. The 50Ω source impedance is transformed to be equal in value to the input resistance of the nonlinear circuit. The corresponding quality factor (Q) factor is found to be

$$Q = \pm \sqrt{\frac{R_S}{R_1} - 1} = \pm \sqrt{\frac{50}{9.55} - 1} = \pm 2.06 \quad (4.19)$$

The reader is referred to Appendix A for the derivation of Equation 4.19. Since the quality factor is equal for both the parallel and series circuit, the reactance and equivalent capacitance of the parallel capacitor is calculated as

$$X = \frac{R_S}{Q} = \frac{50}{-2.06} = -24.27 \Omega \quad (4.20)$$

$$C = \frac{-1}{\omega X} = \frac{-1}{2\pi(200 \times 10^6)(-24.27)} = 32.79 \text{ pF} \quad (4.21)$$

The series reactance is found to be

$$X_S = QR_1 = -2.06(9.55) = -19.67 \Omega \quad (4.22)$$

For the source to be matched to the input impedance of the nonlinear circuit, the total reactance must be zero at 200 MHz. A series inductor is added cancel the reactance,

$$L_S = \frac{|X_T|}{\omega} = \frac{|X_S + X_1|}{\omega} = \frac{|-19.67 + (-77.01)|}{2\pi(200 \times 10^6)} = 76.94 \text{ nH} \quad (4.23)$$

The complete input matching circuit is depicted in Figure 4.12.

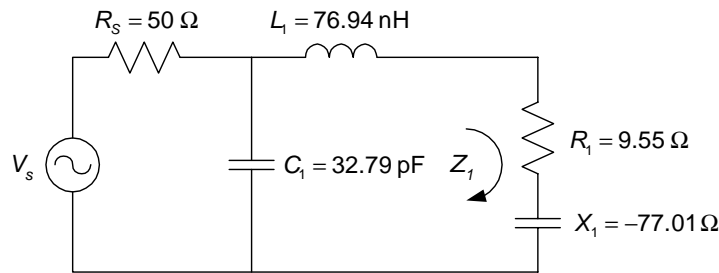


Figure 4.12: Input matching circuit.

Figure 4.13 shows a plot of the impedance seen looking back from the nonlinear circuit into the matching network. Note that the impedance at 200 MHz is equal to the conjugate of Z_1 , as expected. Also note that the impedance increases with increasing frequency, preventing higher-order currents generated by the nonlinear circuit from flowing. Although the impedance is not that large at 600 MHz, the matching network presents a relatively high reactive impedance to the third harmonic. The same is true for the fifth harmonic.

The output matching circuit takes the form of that shown in Figure 4.14. Besides providing the required impedance match, the π -resonator which consists of the inductor and the two shunt capacitors, acts as a bandpass filter. This is ideal since it rejects undesired harmonics. The two series capacitors determine the amount of coupling and should be kept small to maximise the loaded Q factor.

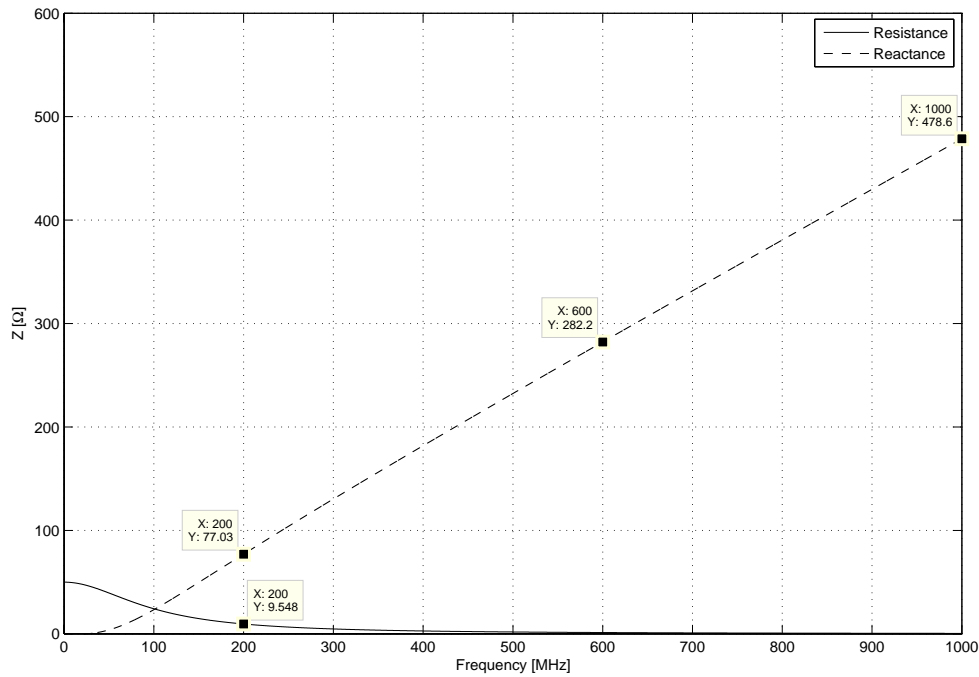


Figure 4.13: Impedance seen looking back from the nonlinear circuit to the source.

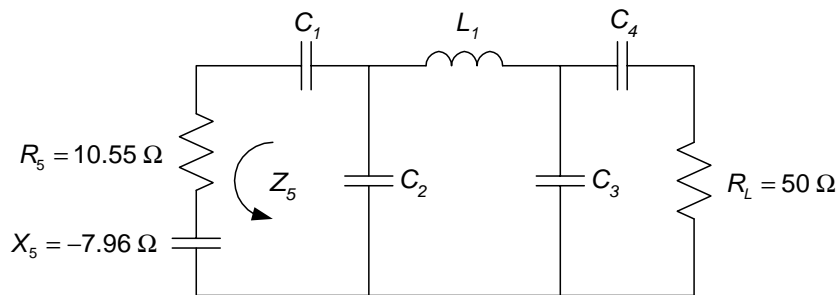


Figure 4.14: Proposed output matching circuit topology.

With $C_4 = 1 \text{ pF}$, the series combination of C_4 and $R_L = 50 \text{ } \Omega$ transforms to an equivalent parallel circuit with values

$$R_{pL} = R_L (1 + Q_L^2) \tag{4.24}$$

$$R_{pL} = 50 \left(1 + \left(\frac{-159.15}{50} \right)^2 \right) = 556.57 \text{ } \Omega \tag{4.25}$$

and

$$X_{pL} = \frac{R_{pL}}{Q_L} = \frac{556.57}{-3.18} = -175.02 \text{ } \Omega \tag{4.26}$$

The π -resonator requires the same impedance loading on both sides. Thus, R_5 needs to be trans-

formed to 556.57Ω . The required Q factor is found to be

$$Q_S = \pm \sqrt{\frac{R_{pS}}{R_5} - 1} = \pm \sqrt{\frac{556.57}{10.55} - 1} = \pm 7.19 \quad (4.27)$$

The equivalent series and parallel reactance corresponding to Q_S is equal to

$$X_S = R_5 Q_S = 10.55(-7.19) = -75.85 \Omega \quad (4.28)$$

and

$$X_{pS} = \frac{R_{pS}}{Q_S} = \frac{556.57}{-7.19} = -77.4 \Omega \quad (4.29)$$

The total series reactance X_S is comprised of X_5 and the reactance of C_1 . The reactance and capacitance of C_1 are calculated as

$$X_1 = X_S - X_5 = -75.85 - (-7.96) = -67.89 \Omega \quad (4.30)$$

$$C_1 = \frac{-1}{\omega X_1} = \frac{-1}{2\pi(1 \times 10^9)(-67.89)} = 2.34 \text{ pF} \quad (4.31)$$

The circuit values calculated thus far, and the corresponding transformations are shown in Figure 4.15.

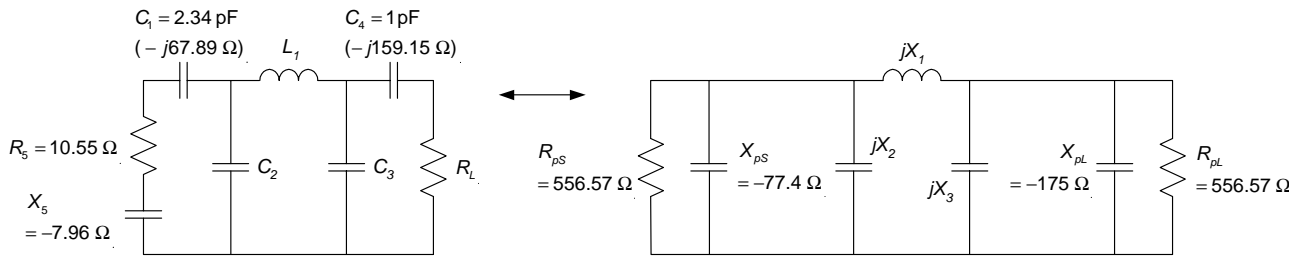


Figure 4.15: Output matching circuit with series-to-parallel transformations.

The resonant frequency of the π -resonator is given by

$$f_0 = \frac{1}{2\pi \sqrt{\frac{L_1 C}{2}}} \quad (4.32)$$

where $C = \frac{-1}{\omega(X_{pS} || X_2)} = \frac{-1}{\omega(X_{pL} || X_3)}$. Rearranging terms in Equation 4.32 yields

$$C = \frac{2}{\omega^2 L_1} = \frac{-1}{\omega X_c} \quad (4.33)$$

$|X_c|$ cannot be larger than $|X_{pS}|$, since $|X_{pS} || X_2| \leq |X_{pS}|$. Choosing L_1 equal to 10 nH yields a

capacitance and equivalent reactance of

$$C = \frac{2}{\omega^2 L_1} = \frac{2}{(2\pi(1 \times 10^9))^2 10 \times 10^{-9}} = 5.07 \text{ pF} \quad (4.34)$$

$$X_c = \frac{-1}{\omega C} = \frac{-1}{2\pi(1 \times 10^9)5.07 \times 10^{-12}} = -31.39 \Omega \quad (4.35)$$

Solving for X_2 and X_3 and calculating the equivalent capacitances yields

$$\begin{aligned} X_2 &= -52.89 \Omega \\ \therefore C_2 &= \frac{-1}{\omega X_2} = \frac{-1}{2\pi(1 \times 10^9)(-52.89)} = 3 \text{ pF} \end{aligned} \quad (4.36)$$

and

$$\begin{aligned} X_3 &= -38.3 \Omega \\ \therefore C_3 &= \frac{-1}{\omega X_3} = \frac{-1}{2\pi(1 \times 10^9)(-38.3)} = 4.16 \text{ pF} \end{aligned} \quad (4.37)$$

Figure 4.16 shows the impedance seen looking towards the load. Note that the input impedance at 1 GHz is essentially equal to the conjugate of Z_5 , thus ensuring maximum power transfer to the load. The matching network presents a moderately high reactive impedance at the third harmonic, causing most of the third-order current that does flow to be reflected back towards the nonlinear circuit where it mixes again with other harmonics to produce other frequency components.

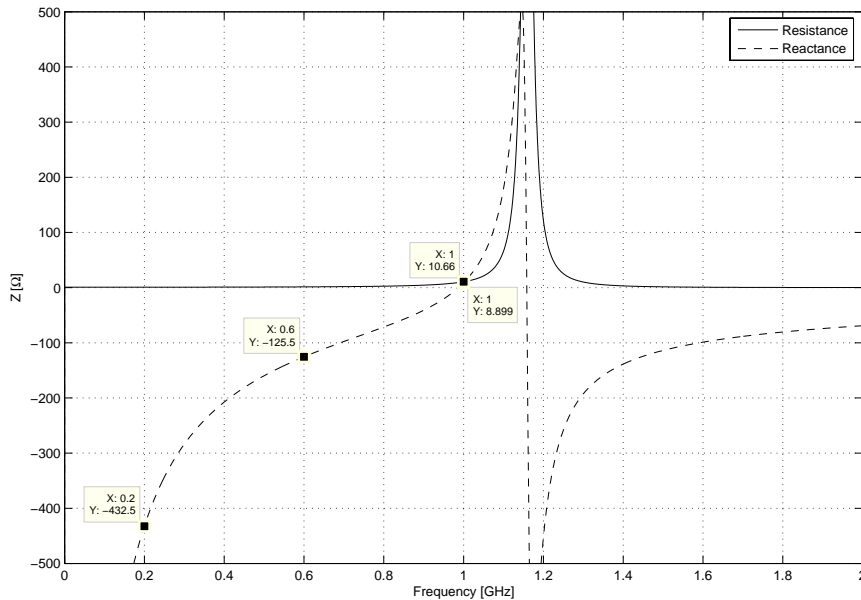


Figure 4.16: Impedance seen looking from the output of the nonlinear circuit towards the load.

Figure 4.17 shows a photo of the frequency multiplier, built-up on *GIL-MC3D* ($\epsilon_r = 3.86$, $h =$

0.787 mm) substrate. A few vias connecting the top and bottom ground planes were manually soldered through the substrate to ensure good RF ground. Surface mount 0603 capacitors and chip inductors were used. The characteristic impedance of the input and output transmission lines is 50Ω .

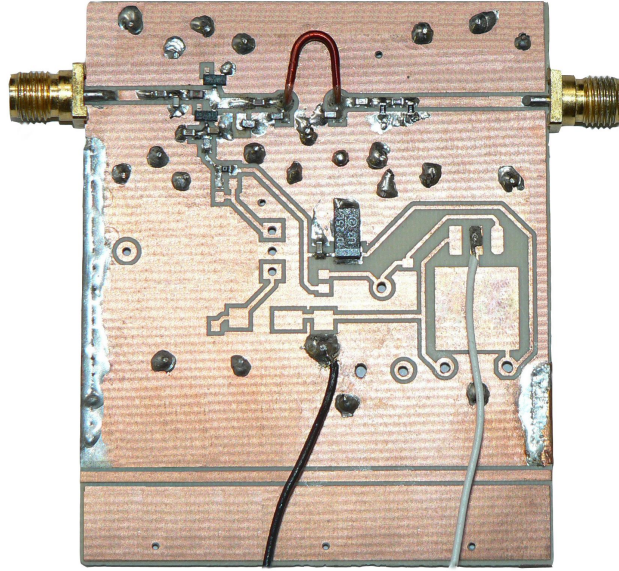


Figure 4.17: A photo of the frequency multiplier.

The 10 nH inductor of the output matching circuit is realised by using a short piece of copper wire orientated horizontally above the ground plane, as shown in the photo. The inductance can be varied by physically adjusting the height of the wire above the ground plane. By varying the inductance, the output matching network can be optimised for minimal conversion loss.

The required line length can be calculated. It can be shown that, due to the symmetrical loading and relatively high loaded Q factor of the π -resonator, there exists a virtual ground in the middle of the inductor. Thus, when looking into the resonant circuit, the inductor appears as a short-circuited piece of transmission line of length $\ell = \ell_t/2$, where ℓ_t is the total length of the line. The input impedance of a short-circuited transmission line is given by

$$Z_{in} = jZ_0 \tan(\beta\ell) \quad (4.38)$$

where Z_0 is the characteristic impedance of the transmission line and $\beta = \frac{2\pi}{\lambda}$ [13]. The characteristic impedance of a horizontal line above ground, is given by [39]

$$Z_0 = \frac{138}{\sqrt{\epsilon_r}} \log_{10} \left(\frac{4h}{d} \right) \quad \text{for} \quad d \ll h \quad (4.39)$$

where d is the diameter of the line and h is the distance from the ground plane to the centre of the transmission line. Substituting Equation 4.39 into Equation 4.38 yields

$$Z_{in} = j \frac{138}{\sqrt{\epsilon_r}} \log_{10} \left(\frac{4h}{d} \right) \tan(\beta\ell) = j\omega \frac{L}{2} \quad (4.40)$$

Equation 4.40 shows that a change in h causes a change in inductance. Solving Equation 4.40 for the length of the line, yields

$$\ell = \frac{\lambda}{2\pi} \tan^{-1} \left(\frac{Z_{in}}{j \frac{138}{\sqrt{\epsilon_r}} \log_{10} \left(\frac{4h}{d} \right)} \right) \quad (4.41)$$

With $h = 2.5$ mm, $d = 1$ mm, $\epsilon_r = 1$ and $Z_{in} = j\omega \frac{L}{2} = j2\pi(1 \times 10^9) \frac{(10 \times 10^{-9})}{2}$, ℓ is found to be

$$\ell = 10.68 \text{ mm} \quad (4.42)$$

The total length of the line is thus equal to

$$\ell_t = 2 \times \ell = 2 \times 10.68 = 21.36 \text{ mm} \quad (4.43)$$

4.4 Simulated and Measured Response

Figure 4.18 shows the schematic circuit diagram of the complete frequency multiplier implemented in *Microwave Office (MWO)*. The component values shown in the figure are practical values chosen closest to that calculated in the previous section, with the exception of the 1.8 pF capacitor in the output matching network which has been optimised slightly through practical experimentation.

The DC threshold voltage of 11 V is supplied through a 10 k Ω resistor. The required input power for $V_T = \frac{11}{2} + 0.8 = 6.3$ V, $C_T = 4$ pF, $m = 2$, $n = 5$ and $f = 200$ MHz, is

$$P_{in} = 10 \log_{10} \left(\left(\frac{I_1}{\sqrt{2}} \right)^2 R_1 \right) + 30 = 10 \log_{10} \left(\left(\frac{-0.102}{\sqrt{2}} \right)^2 9.55 \right) + 30 = 17 \text{ dBm} \quad (4.44)$$

where Equation 4.8 has been used. The circuit is simulated with P_{in} equal to 18 dBm, for comparison to the measured response.

The parallel combination of the 180 pF and 680 pF capacitors provides a low impedance path to ground for AC signals. The 680 pF capacitor at the input of the multiplier serves as a DC blocking capacitor. Note that the output matching network is inherently AC coupled. A 3 dB π -attenuator is added to the output to improve the output return loss by 6 dB.

A 1.8 pF capacitor is added in parallel with the diodes. Together with the depletion capacitance of each diode under reverse bias, it forms a total parallel capacitance of $C_T = 3.8$ pF. In practice, parasitic and stray capacitance associated with each diode also add to C_T . There is some uncertainty

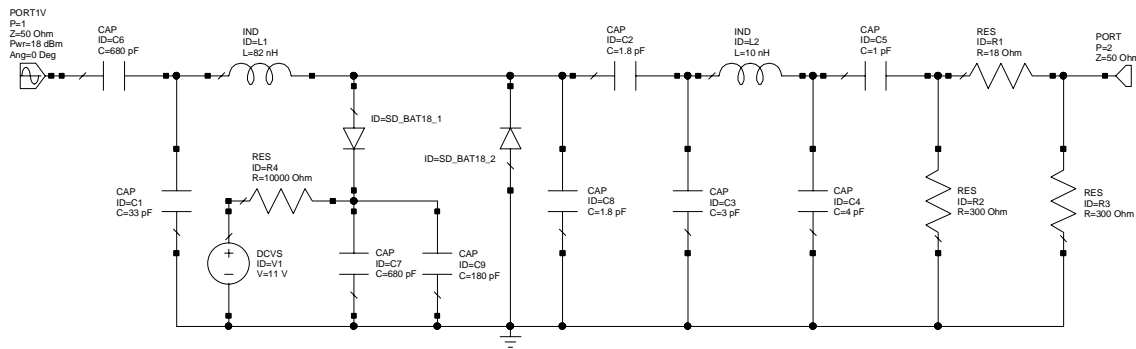


Figure 4.18: Frequency multiplier circuit diagram.

as to the exact value of this capacitance, and its effect was investigated through measurement. It is estimated that each diode contributes in the order of 1 pF. For this reason, the multiplier was designed for $C_T = 4$ pF. If the total parasitic and stray capacitance are indeed in the order of 2 pF, C_p can simply be made zero. In this case, total shunt capacitance C_T is still equal to 4 pF. The parallel capacitor C_p thus gives some control over the total shunt capacitance and is a parameter that is best optimised through trial and error.

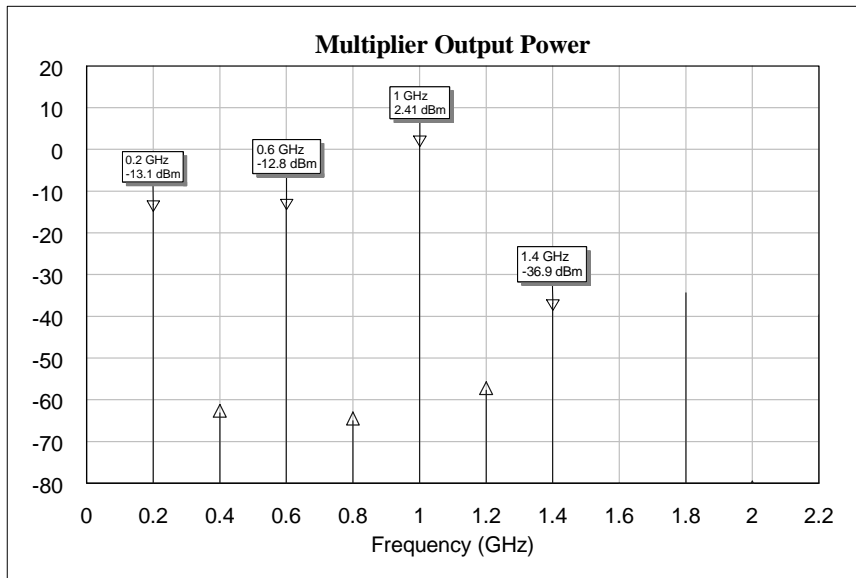


Figure 4.19: Predicted frequency content at the output of the SRD multiplier.

Harmonic-balance analysis of SRD multipliers can be troublesome due to the strong nonlinearity of SRDs, the large number of harmonics involved, especially in high-order multipliers, and possible instability, making convergence precarious. The high sensitivity of reactive multipliers to parameter variations further complicate matters [25, 32]. Despite this, an attempt was made to simulate the multiplier using the harmonic-balance solver of MWO. The number of harmonics was set to 20, four times the highest harmonic of interest.

Figure 4.19 shows the predicted harmonic output power of the circuit shown in Figure 4.18. If the 3 dB attenuator at the output of the multiplier is taken into account, the conversion loss, which is the difference in fundamental input and desired harmonic output power, is equal to $18 - (2.41 + 3) = 12.59$ dB.

The multiplier shown in Figure 4.17 was measured on an HP8562A spectrum analyser. A Rohde & Schwarz SML03 signal generator was used to supply the input signal. A photo of the measurement setup is shown in Figure 4.20.

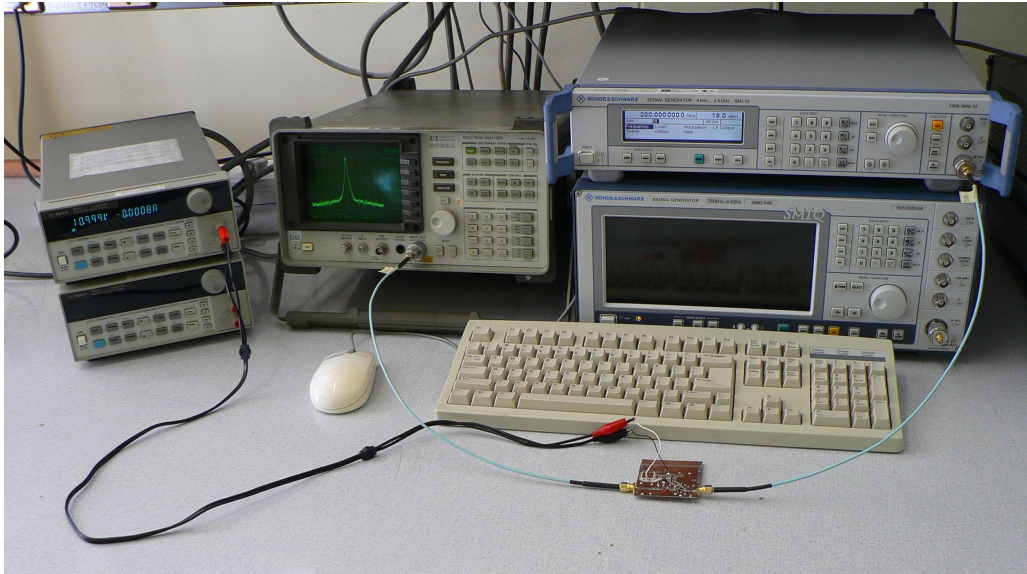


Figure 4.20: Measurement setup for characterisation of the frequency multiplier.

Figure 4.21 shows the measured frequency content at the output of the frequency multiplier. P_{in} refers to the power at the output port of the signal generator. The loss in the two cables has not been calibrated out, but is basically negligible. The interested reader is referred to Appendix C which shows a plot of the loss of the cables as a function of frequency. In each of the measurements, RBW refers to the resolution bandwidth, VBW indicates the video bandwidth, and Att denotes the attenuator of the spectrum analyser. The measured fundamental and third harmonic power is very close to that obtained with the MWO model. The fifth harmonic power is however 6.74 dB lower than expected, but increased significantly when C_p was made smaller. The highest output power was obtained when C_p was removed. According to these observations, it seems that the parasitic and stray capacitance are not negligible, causing an increase in the total parallel capacitance.

Figure 4.22 shows the measured frequency content with C_p removed. Note the similarity in the measured frequency response and that simulated under the same conditions. The fundamental component and third and fifth harmonic all lie within 0.7 dB of the simulated values.

The anti-parallel diodes yield good levels of even-order harmonic suppression. All even-order harmonics are at least 30 dB lower in power compared to the desired fifth harmonic. Besides the desired

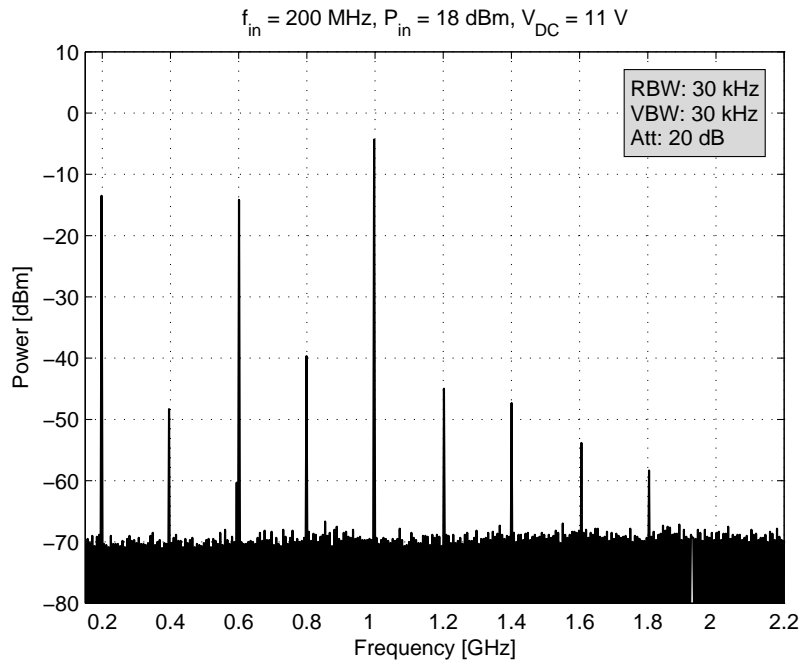


Figure 4.21: Measured output frequency spectrum with $C_p = 1.8 \text{ pF}$.

fifth harmonic, the fundamental and third harmonic also appear at the output. The fundamental frequency component at 200 MHz is 15 dB lower compared to the fifth harmonic at 1 GHz, and has decreased by approximately 31 dB from the input to the output.

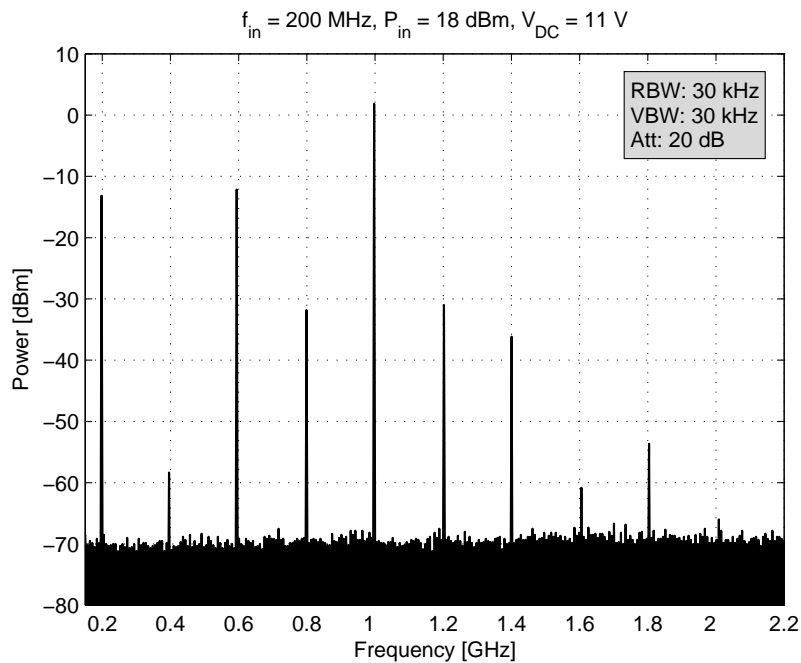


Figure 4.22: Multiplier output frequency spectrum with C_p removed.

A valid question that may be raised at this point is why the conversion loss of the multiplier is not equal to 0 dB. The lossless nonlinear capacitor model shown in Figure 4.1 suggests that all input power must be converted to output power. There are several reasons why this is not the case. In reality, not all the input power is converted to the desired harmonic. Figure 4.22 shows that, due to diode mismatch and nonideal embedding networks, some fundamental input power is also spread to other harmonics besides the fifth. The ideal nonlinear circuit model also assumes zero series resistance. In practice, there is some loss associated with the series resistance of the diodes. In addition, there is also some associated loss in the matching networks due to the finite quality factors of the circuit elements used. Also, although the carrier lifetime is long compared to the inverse of the fundamental input frequency, some charge recombines and does not contribute to output power. The finite switching time of the diodes also results in the attenuation of high-order harmonics [31].

Figure 4.23 shows a plot of the power in the fifth harmonic, as a function of V_{DC} . All four curves exhibit hysteresis. That is, in a specific region, increasing V_{DC} produces different fifth harmonic output power values from those where V_{DC} is decreasing. This measured data is very unique and to the author's knowledge, similar observations have not been published in any other literature discussing the same topic.

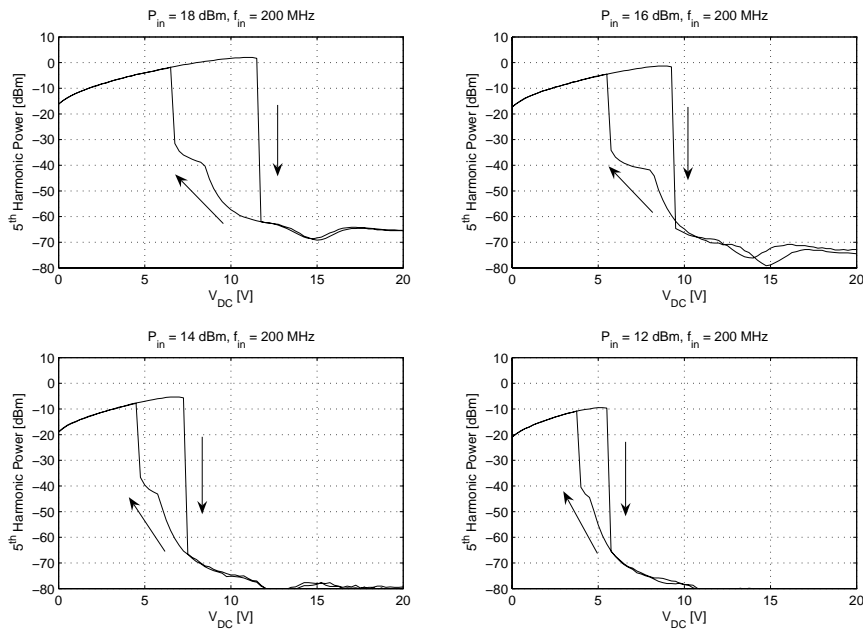


Figure 4.23: Output power in the fifth harmonic as a function of voltage.

Recall that the value of V_{DC} , and hence V_T , affects the amount of required fundamental input power. If the peak value of fundamental current (I_1) is given by Equation 4.8, the input impedance Z_1 is independent of V_T , and with the parameters of the multiplier designed in this chapter, is given by the last entry in Table 4.1. However, whenever I_1 and hence P_{in} is not related to V_T by Equation 4.8 and are changed independently, Z_1 changes accordingly.

Thus, when P_{in} is held fixed and V_{DC} increases from 0 V, Z_1 changes. For low values of V_{DC} , the input power is large enough to switch both diodes, even when the input impedance is not perfectly matched to the 50 Ω source. As V_{DC} increases, Z_1 changes from being poorly matched to a point where it is perfectly matched to the source. At this point, I_1 is given by Equation 4.8, and in this state of resonance, maximum fundamental input power is converted to fifth harmonic power. Figure 4.23 shows that for $P_{in} = 18$ dBm, this corresponds to about $V_{DC} = 11$ V. Theory predicts this point to be at $V_{DC} = 12.5$ V, but is calculated with the assumption that the input matching circuit is lossless. In reality, there is some loss associated with the input matching network and cable used at the input of the multiplier.

If V_{DC} increases beyond the optimal voltage, it reaches a point where the fixed fundamental input power is not large enough to forward bias the diodes. When this happens, both diodes become reverse biased and the operation of the multiplier is limited to the linear depletion portion of the characteristic Q/V line shown in Figure 4.6. In this linear region, no harmonics are created. Figure 4.23 shows that the power in the fifth harmonic drops very abruptly to very low values.

When V_{DC} decreases from a point for which both diodes are initially reverse biased, the input impedance changes again. In this case however, the input impedance is such that the input power is too small to switch the diodes, even for values of V_{DC} under which they switched when it was increased. Only when the voltage decreases significantly, the input power becomes large enough to start switching the diodes. At this point there is a sudden increase in fifth harmonic power and the circuit changes to a impedance state similar to when V_{DC} increased.

Note that the value of V_{DC} for which the diodes become reversed biased decreases as the input power is decreased. As a result, it causes the overall area of hysteresis to decrease.

From a practical point of view, it is impractical to operate the multiplier under conditions of minimal conversion loss. Figure 4.23 shows that if the multiplier is operated with $P_{in} = 18$ dBm and $V_{DC} = 11$ V, a small increase in DC voltage will force the multiplier to the linear mode of operation, causing no harmonics to be generated. For this reason, it is recommended to operate the multiplier at a point outside the area of hysteresis, sacrificing conversion loss for stable operation.

Figure 4.24 shows the conversion loss of the multiplier as a function of input power. The curves also exhibit hysteresis for the same reasons discussed in the previous paragraphs. In this case, V_{DC} is held constant and P_{in} is varied. With the 3 dB attenuation at the output taken into account, the minimum conversion loss is equal to 13 dB, and occurs for $V_{DC} = 11$ V and $P_{in} = 18$ dBm. When V_{DC} decreases, the area of hysteresis moves towards values of lower input power, as expected.

Figure 4.25 shows a plot of the fifth harmonic power as a function of frequency. The measurement was performed with the *max hold* function of the HP8562A spectrum analyser. According to both Figure 4.23 and Figure 4.24, $P_{in} = 18$ dBm and $P_{in} = 16$ dBm lie outside the area of hysteresis for the case where $V_{DC} = 5$ V.

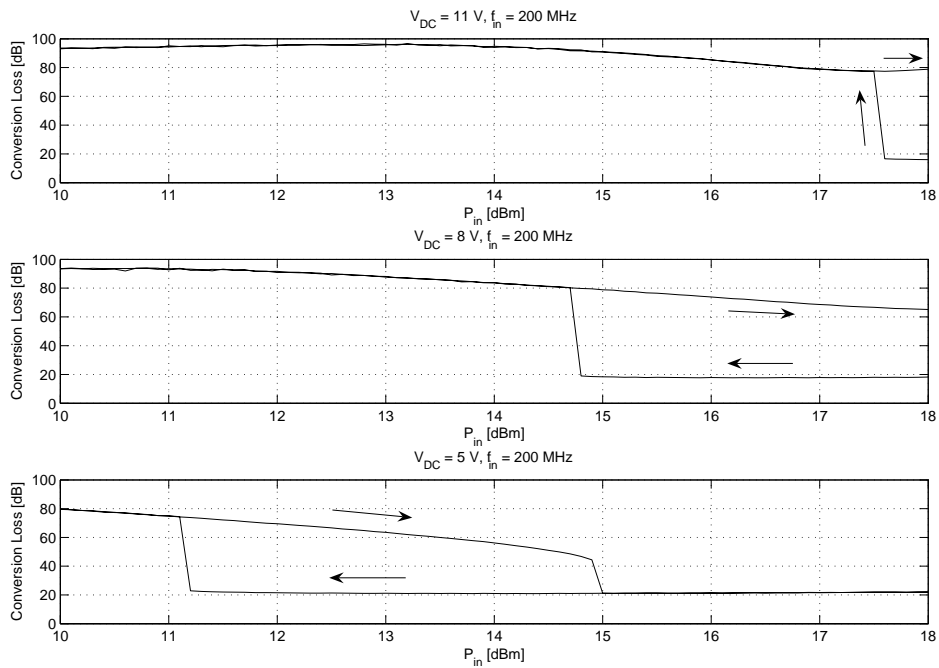


Figure 4.24: Conversion loss as a function of input power.

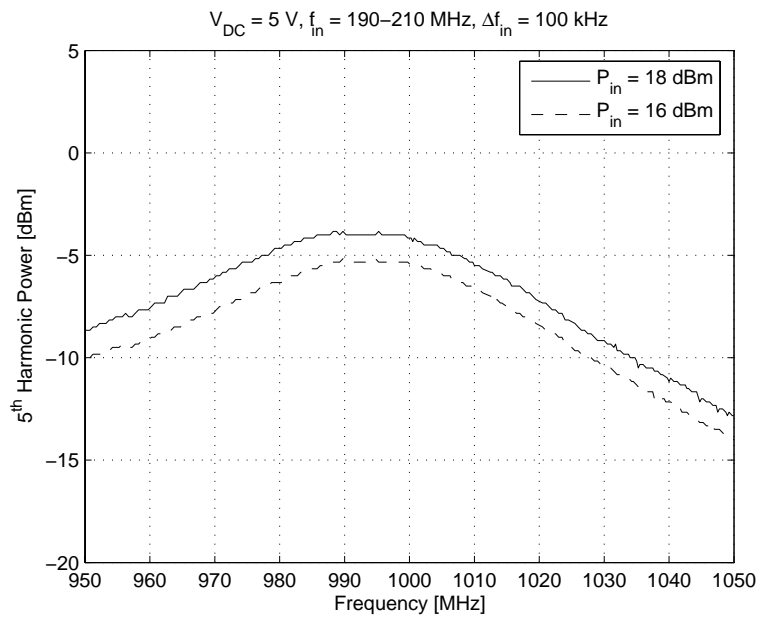


Figure 4.25: Fifth harmonic power as a function of frequency.

The power in the fifth harmonic was optimised by adjusting the height of the inductor in the output matching network above the ground plane for the case where $V_{DC} = 11$ V and $P_{in} = 18$ dBm. The maximum fifth harmonic power occurs at 995 MHz for the case where $V_{DC} = 5$ V. The 3 dB bandwidth for both $P_{in} = 18$ dBm and 16 dBm is in the order of 5.5%.

Due to the relatively weak C/V nonlinearity of varactor diodes, they do not efficiently generate harmonics greater than the second. To increase the conversion efficiency of varactor multipliers with multiplication factors greater than 2, an *idler* is often used. An idler is a series resonator that is placed in parallel with the nonlinear element, tuned to an intermediate harmonic, also known as the *idler* frequency. The resonator creates a path for an intermediate harmonic current, allowing it to re-circulate through the nonlinear circuit where it mixes again with other frequency components, producing higher harmonic components. In a tripler for example, an idler with a resonant frequency at the second harmonic presents a short circuit to the generated second harmonic current, causing it to re-circulate through the nonlinear circuit and mix with the fundamental, producing the desired third harmonic. Although the strong C/V nonlinearity of SRDs generally do not require the use of idlers, both theory and experimental evidence indicate that idlers can improve the efficiency of reactive multipliers, even those using SRDs [25].

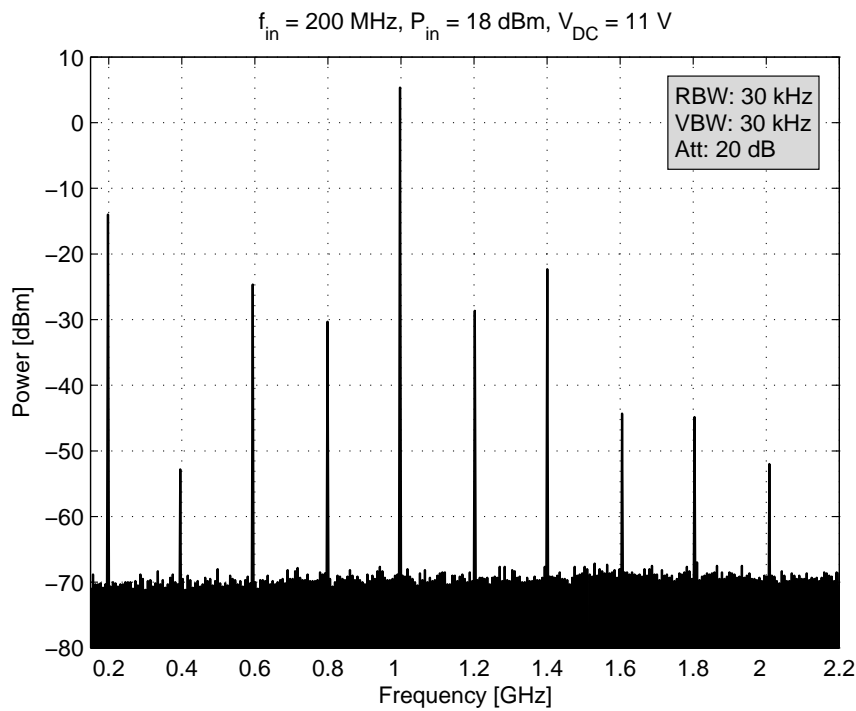


Figure 4.26: Frequency response of the multiplier with a third harmonic idler in place.

An idler with a resonant frequency at the third harmonic was inserted into the multiplier circuit. The idler consists of a series combination of $L = 22$ nH and $C = 3.3$ pF in parallel with both diodes. The resonant frequency of the idler is equal to

$$f_r = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{(22 \times 10^{-9})(3.3 \times 10^{-12})}} = 590.68 \text{ MHz} \quad (4.45)$$

which was found to be close enough to 600 MHz. Both L and C were implemented with 0603 surface mount components.

It is important to note that the design of the multiplier assumed only the fundamental and fifth harmonic currents to be applied to the nonlinear circuit. With the idler in place, a path for the third harmonic current exists, resulting in an additional current component to be applied to the nonlinear circuit. The design of the multiplier discussed in the previous section, is thus not valid for the case where an idler is present. To design a multiplier with an idler present, a total of three currents must be considered. The design with an idler present was not performed, but the effect of the idler on the designed circuit was investigated.

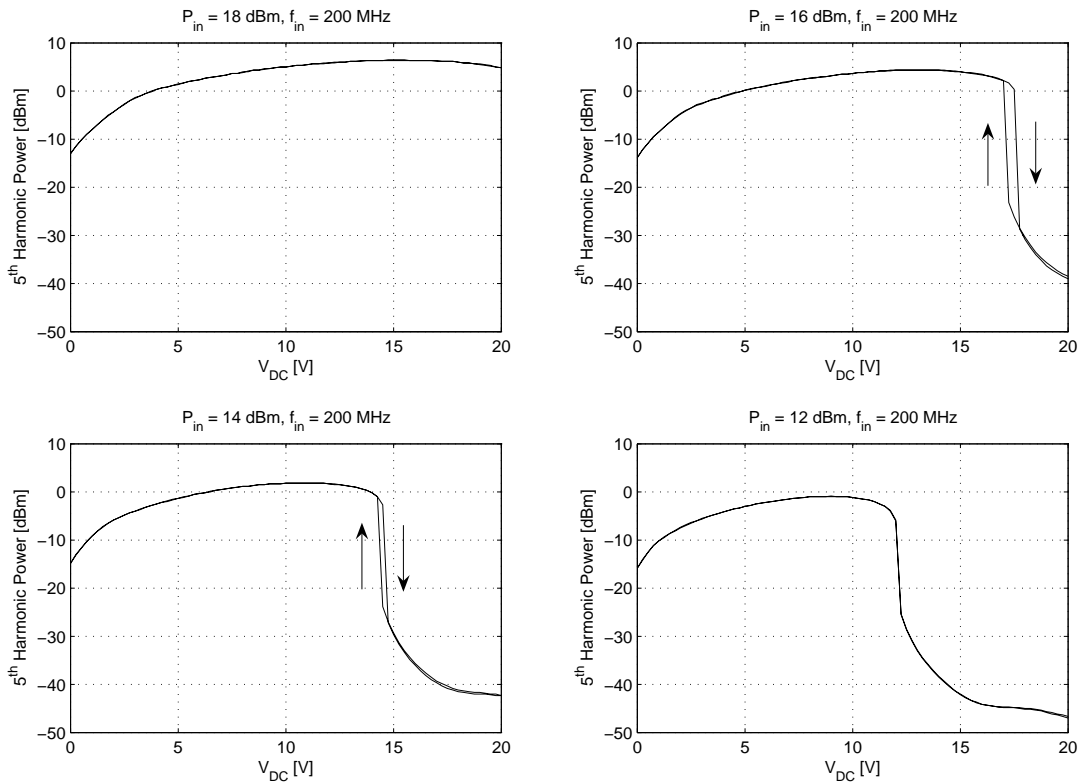


Figure 4.27: Fifth harmonic power as a function of V_{DC} with the idler present.

Figure 4.26 shows the frequency content with the idler present, measured with $V_{DC} = 11$ V. Comparing Figure 4.26 to Figure 4.22 shows that the power in the fifth harmonic has increased by 3.5 dB. Also note that the third harmonic power has decreased by 12.5 dB. The idler thus has the desired effect of converting third harmonic power to the fifth harmonic. As a result of the idler, the power in harmonics beyond the fifth has also increased somewhat.

Figure 4.27 shows the power in the fifth harmonic as a function of V_{DC} . Note the astonishing effect the idler has on the output power. Compared to the multiplier circuit without the idler, it has decreased the area of hysteresis significantly. In fact, the hysteresis is essentially eliminated by the idler. Also note that the multiplier with the idler is able to operate up to much higher DC voltage levels.

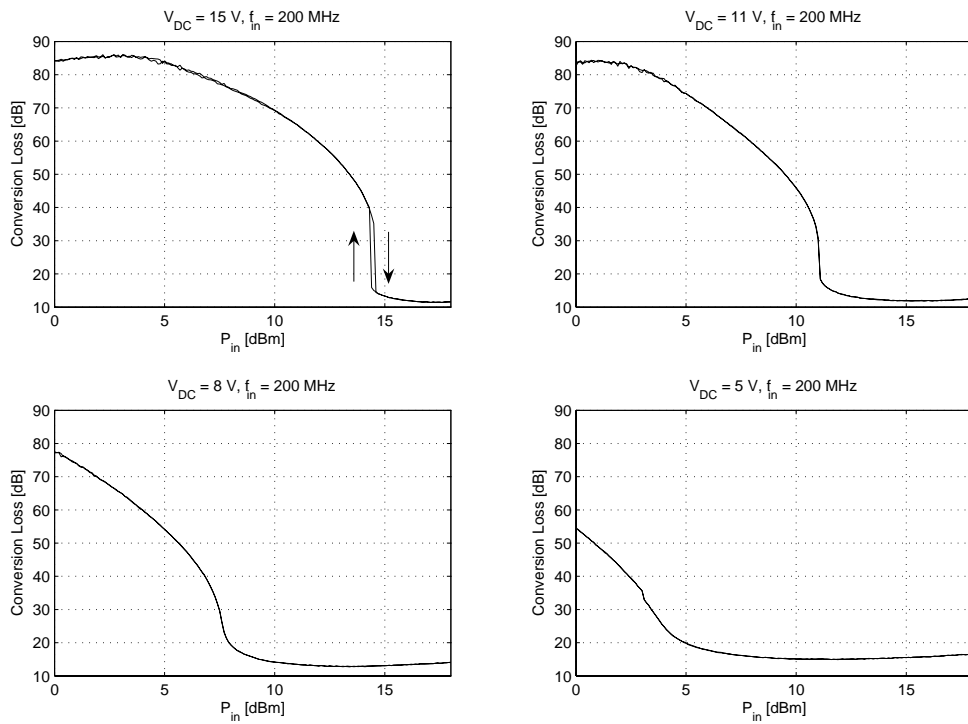


Figure 4.28: Conversion loss of the multiplier with a third harmonic idler in place.

Figure 4.28 shows a plot of the conversion loss. The minimum conversion loss is observed when $V_{DC} = 15$ V and $P_{in} = 18$ dBm. If the 3 dB attenuator at the output is taken into account, the minimum conversion loss is approximately 8.5 dB. Comparing Figure 4.28 to Figure 4.24 shows that the idler increases the effective operating region of the frequency multiplier. For the same values of V_{DC} , the multiplier with the idler is able to operate efficiently for lower input power levels.

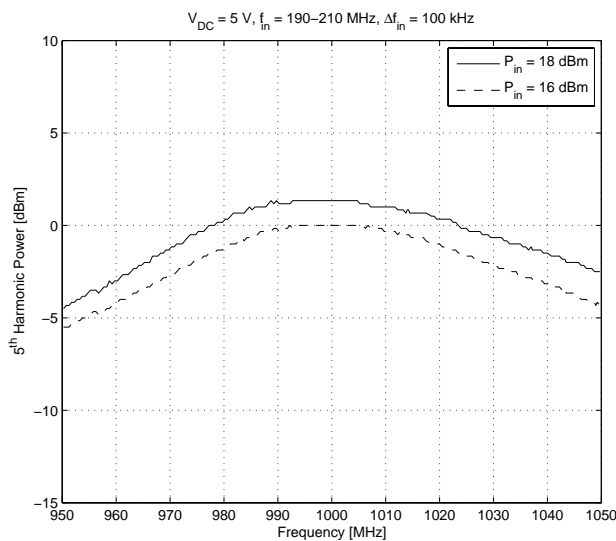


Figure 4.29: Fifth harmonic power as a function of frequency with the idler present.

Figure 4.29 shows the power in the fifth harmonic as a function of frequency, with $P_{in} = 18$ dBm and $P_{in} = 16$ dBm. The bandwidth for the two cases is 7.3% and 6.93%, respectively. This is slightly more compared to the case where no idler was present.

It is clear that the idler, besides decreasing conversion loss, improves the overall performance of the multiplier. Although the multiplier with the idler can be operated under optimal conditions, that is, $P_{in} = 18$ dBm and $V_{DC} = 15$ V, it requires high input power. Figure 4.28 shows that the multiplier is still very efficient for lower values of V_{DC} and input power. For $V_{DC} = 5$ V, the input power can be anything between 5 dBm to 18 dBm with relative good levels of efficiency.

4.5 Conclusion

This chapter discussed the detailed design of an SRD frequency multiplier with the aid of the simple piecewise linear model introduced in Section 4.2. With a choice of suitable parameters, the large-signal input and output impedances were found by computing the Fourier coefficients of the voltage waveform in phase and quadrature with the applied current.

The measured response of the multiplier without the idler yielded good even-order harmonic suppression, and with C_p removed, a minimum conversion loss of 13 dB was achieved. The sensitivity of the multiplier to circuit parameters was also seen, limiting the use of the multiplier without an idler, to low values of V_{DC} .

The idler improved the multiplier in almost every aspect. It minimised conversion loss, essentially removed the effect of hysteresis, increased the 3 dB bandwidth slightly, and broadened the effective region of operation considerably. For these reasons, it was decided to implement an idler in the multiplier circuit used for the frequency synthesiser.

Chapter 5

Narrow and Moderate Bandwidth Microwave Bandpass Filters

5.1 Introduction

This chapter describes the theory, design, software modelling, optimisation and measured response of the combline and interdigital bandpass filters that form part of the frequency synthesiser. The microwave filters discussed in this chapter are comprised of a combination of both lumped and distributed elements. The high unloaded quality factors of the distributed elements ensure minimum insertion loss for a given fractional bandwidth. Chebyshev filter responses were chosen for the filters because of the sharper cutoff rate compared to Butterworth filters of the same order [40].

The outline of this chapter is as follows. In Section 5.2, a generalised bandpass circuit for filters of narrow to moderate bandwidth is derived from a well-known lowpass *LC*-ladder prototype filter circuit. The bandpass circuit topology is general and practical for implementation at microwave frequencies as it accommodates for the use of lumped elements, distributed elements or a combination thereof. Along with the derivation of the bandpass circuit, expressions are found that relate the coupling coefficients and external quality factors to the known lowpass prototype element values. The coupling coefficients and external quality factors form the basis of the design [40].

In Section 5.3, it is shown that the equivalent electrical circuit of the combline and interdigital filters can be transformed into a form similar to that derived in Section 5.2. The coupling coefficients and external quality factors of both types of filters are found and are used for the design in Section 5.4 and Section 5.5.

Section 5.4 and 5.5 cover the design, software modelling and optimisation of the combline and interdigital filters, respectively. The measured frequency response of the filters is presented and compared to the theoretical specification and the results obtained with software simulation.

5.2 Coupling and External Quality Factors of the Prototype Bandpass Filter

The bandpass filters considered in this chapter derive its response from the well-known lumped element lowpass filter prototype circuit depicted in Figure 5.1(a). Its dual is shown in (b). Both prototype topologies give identical responses [40].

Figure 5.2(a) shows a typical lowpass Chebyshev (equal ripple) response that can be obtained with the circuits of Figure 5.1. The corresponding bandpass filter response shown in Figure 5.2(b) is obtained by applying a lowpass-to-bandpass transformation on the lowpass prototype circuit. Note that the bandpass filter response is also of Chebyshev form.

A lowpass prototype filter with n reactive elements leads to a bandpass filter with n resonators. The multiple resonances inherent to transmission line or cavity resonators generally cause additional passbands at higher frequencies, as illustrated in Figure 5.2(b). This is not the case when lumped elements are used [40, 41].

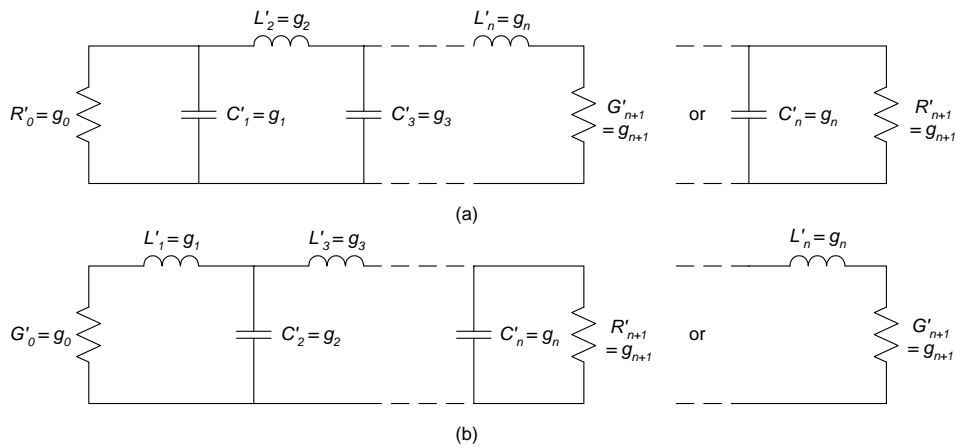


Figure 5.1: Lowpass prototype filter and its corresponding dual circuit shown in (b).

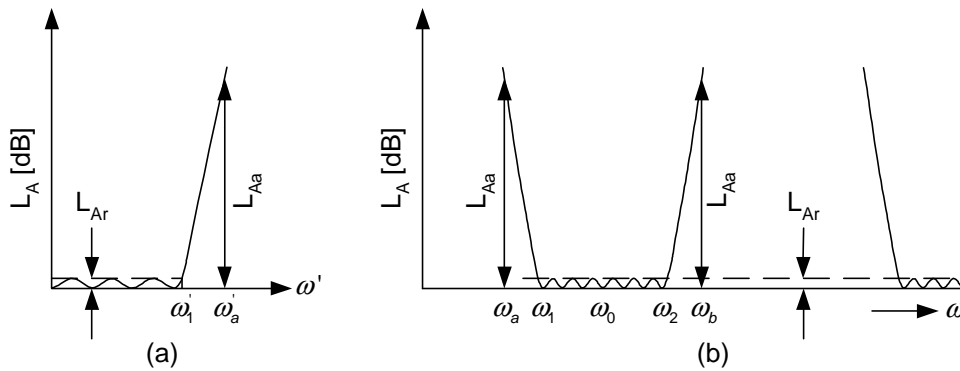


Figure 5.2: (a) Lowpass prototype response and corresponding (b) bandpass filter response.

The normalised lowpass prototype filter element values, for a Chebyshev response with L_{Ar} dB pass-band ripple, $g_0 = 1$, and a ripple bandwidth of $\omega'_1 = 1$, are given by [40, 42]

$$g_1 = \frac{2a_1}{\gamma} \quad (5.1)$$

$$g_k = \frac{4a_{k-1}a_k}{b_{k-1}g_{k-1}} \quad k = 2, 3, \dots, n \quad (5.2)$$

$$g_{n+1} = 1 \quad \text{for } n \text{ odd} \quad (5.3)$$

$$= \coth^2\left(\frac{\beta}{4}\right) \quad \text{for } n \text{ even} \quad (5.4)$$

where

$$\beta = \ln\left(\coth\left(\frac{L_{Ar}}{17.37}\right)\right) \quad (5.5)$$

$$\gamma = \sinh\left(\frac{\beta}{2n}\right) \quad (5.6)$$

$$a_k = \sin\left[\frac{(2k-1)\pi}{2n}\right] \quad k = 1, 2, \dots, n \quad (5.7)$$

$$b_k = \gamma^2 + \sin^2\left(\frac{k\pi}{n}\right) \quad k = 1, 2, \dots, n \quad (5.8)$$

Note that the lowpass prototype circuit contains both series and shunt reactive elements. As a result, the bandpass circuit obtained by performing a lowpass-to-bandpass transformation, is comprised of both series and shunt resonators. This kind of arrangement is difficult to achieve in a practical microwave structure. It is much more practical to realise microwave filters with resonators of the same type [40].

Therefore, to obtain a generalised bandpass prototype circuit practical for implementation at microwave frequencies, the lowpass prototype circuit is first converted into an equivalent lowpass form that consists of only one type of reactive element. This is achieved by the use of admittance or impedance inverters (collectively immittance inverters). The proposed circuit is depicted in Figure 5.3. Note that the transformed lowpass circuit consists of only shunt capacitors. The rectangular blocks represent admittance inverters. The derivation of the equations shown in Figure 5.3 follows after a brief discussion of admittance inverters. The values of G_A , G_B and C_{ak} in Figure 5.3 may be chosen arbitrarily. The response will be identical to that of the original prototype circuit, provided that the admittance parameters J are specified by the equations given in Figure 5.3 [40].

An ideal admittance inverter is a two port network that exhibits such a property at all frequency that if an admittance Y_2 is connected to one of its ports, the admittance Y_1 seen looking into the other port is

$$Y_1 = \frac{J^2}{Y_2} \quad (5.9)$$

where J is real and known as the *characteristic admittance* of the inverter. Admittance inverters are

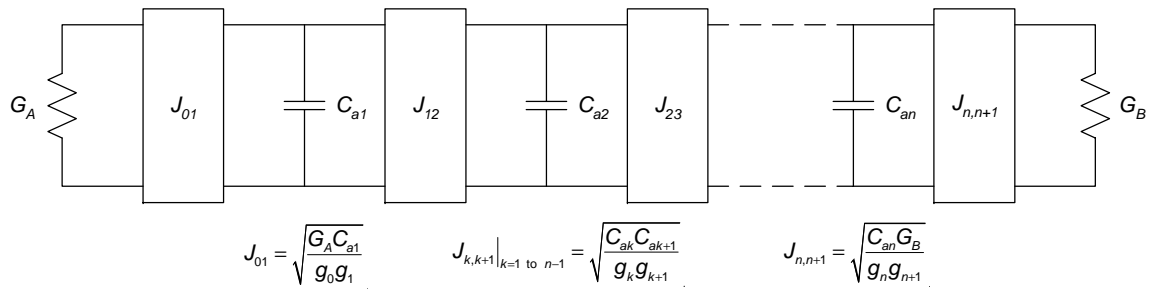


Figure 5.3: Modified lowpass prototype filter using admittance inverters.

also referred to as J -inverters. In general, ideal admittance inverters have the $ABCD$ matrix [42]

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 0 & \pm \frac{1}{jJ} \\ \mp jJ & 0 \end{bmatrix} \quad (5.10)$$

Admittance inverters can be realised in various ways. One of the simplest forms of admittance inverters is a quarter-wavelength transmission line. Recall that the input impedance seen looking into a quarter-wavelength line connected to a load Z_L , is given by

$$Z_{in} = \frac{Z_0^2}{Z_L} \quad (5.11)$$

$$\therefore Y_{in} = \frac{Y_0^2}{Y_L} \quad (5.12)$$

where Z_0 (Y_0) is the characteristic impedance (admittance) of the line. Comparing Equation 5.12 to Equation 5.9 shows that a quarter-wavelength transmission line acts as an admittance inverter, if $J = Y_0$. The inverting property of a quarter-wavelength line is narrowband in nature and can therefore only be used effectively for filters of relatively narrow bandwidth. However, good results can in some cases be obtained for bandwidths approaching 40% [40].

Besides a quarter-wavelength transmission line, there are numerous other circuits that operate as inverters. The type of admittance inverter used for the combline filter consists of transmission lines of positive and negative characteristic admittance, and has the form shown in Figure 5.4 [40, 41]. The negative admittances are in practice absorbed into adjacent lines of positive characteristic admittance.

The derivation of the equations shown in Figure 5.3 is considered briefly. It is analogous to the dual case found in [40].

The circuit configuration, and the corresponding equations shown in Figure 5.3 are found by using the concept of duality. The inverting property of an inverter as indicated by Equation 5.9, makes a series inductance with an inverter on each side look like a shunt capacitance from its exterior terminals. In a similar fashion a shunt capacitance with an inverter on both sides appears as a series inductance from its exterior terminals. Thus, a given circuit as seen through an inverter looks like the dual of that given circuit [40]. Thus, with reference to Figure 5.3 and Figure 5.1, the admittances

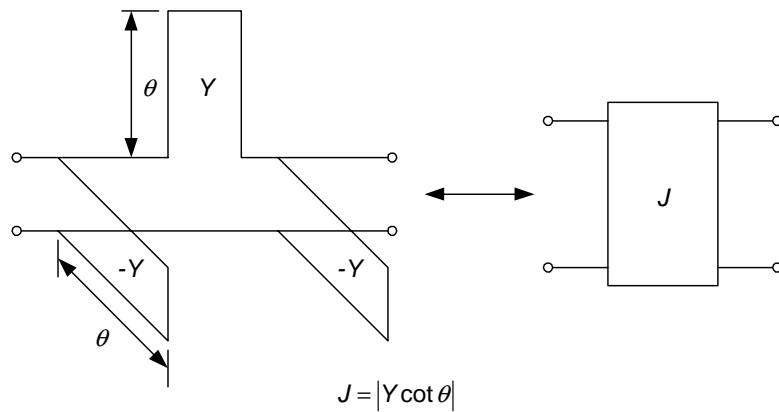


Figure 5.4: An admittance inverter formed from stubs of electrical length θ .

seen from capacitor C_{n1} are the same as those seen from capacitor C'_1 , except for a possible admittance scaling factor. Similarly, the admittances seen from C_{n2} are identical to those seen from C'_2 , except for a possible admittance scale change.

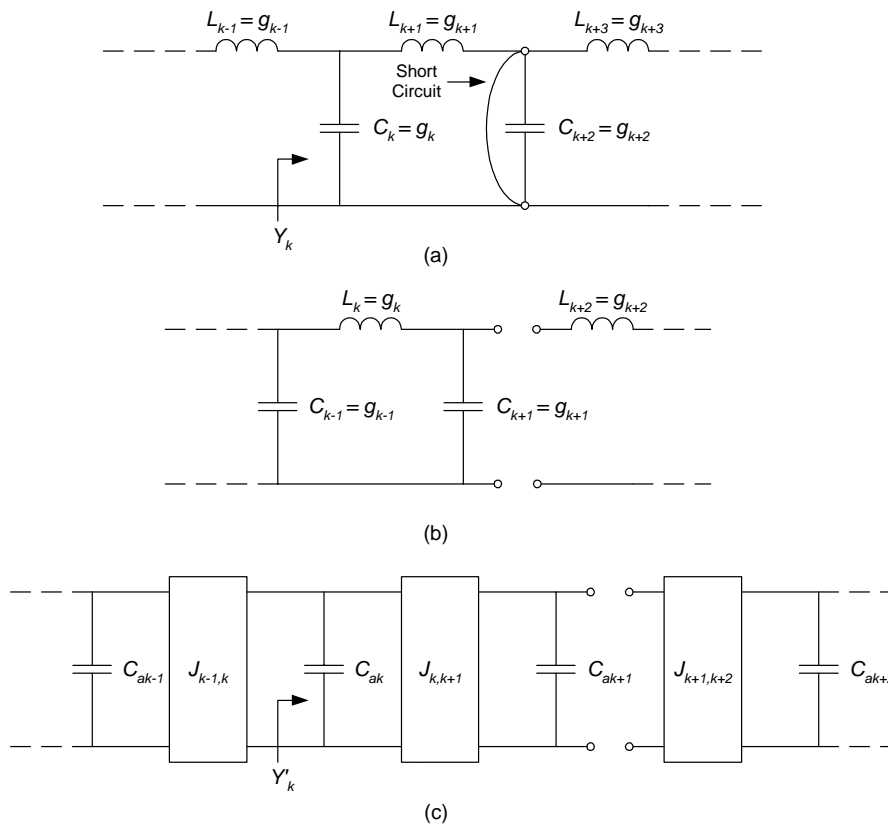


Figure 5.5: A section of the lowpass prototype is shown in (a), and its dual in (b). The analogous J -inverter form of these two circuits is shown in (c).

Figure 5.5(a) shows a section of the original lowpass prototype circuit that has been short circuited behind the inductor L_{k+1} . The short circuit is introduced merely to simplify the analysis. The dual of the circuit is shown in Figure 5.5(b). Note that the short circuit becomes an open circuit in the dual

case. The series inductors transform to shunt capacitors and shunt capacitors transform to series inductors. The circuit shown in Figure 5.5(c) is similar to that of Figure 5.3 and is found by replacing each series inductor in (b) with a shunt capacitor and an admittance inverter on each side.

Since the two circuit representations shown in Figure 5.5(a) and (c) are equivalent, the admittance at any two equivalent points can be compared. The admittance Y_k is equal to

$$Y_k = j\omega C_k + \frac{1}{j\omega L_{k+1}} \quad (5.13)$$

and from Figure 5.5(c)

$$Y'_k = j\omega C_{ak} + \frac{J_{k,k+1}^2}{j\omega C_{ak+1}} \quad (5.14)$$

where Equation 5.9 has been used. The admittance Y_k must be identical to Y'_k , except for an admittance scale factor of C_{ak}/C_k . Therefore

$$Y'_k = \frac{C_{ak}}{C_k} Y_k = j\omega C_{ak} + \frac{C_{ak}}{C_k} \frac{1}{j\omega L_{k+1}} \quad (5.15)$$

Equating the second terms of Equation 5.14 and Equation 5.15 gives, after some rearrangement,

$$J_{k,k+1} = \sqrt{\frac{C_{ak}C_{ak+1}}{C_k L_{k+1}}} = \sqrt{\frac{C_{ak}C_{ak+1}}{g_k g_{k+1}}} \quad (5.16)$$

which is equal to that given in Figure 5.3. Inspection shows that the same procedure applies for calculation of the other inverter parameters, except those at the ends. Hence, Equation 5.16 is valid for $k = 1, 2, \dots, n - 1$.

To calculate $J_{n,n+1}$, consider Figure 5.6. Figure 5.6(a) shows the end section of the lowpass prototype circuit, and (b) shows an equivalent form with a J -inverter.

The admittance Y_n is equal to

$$Y_n = j\omega C_n + \frac{1}{R_{n+1}} \quad (5.17)$$

Similarly

$$Y'_n = j\omega C_{an} + \frac{J_{n,n+1}^2}{G_B} \quad (5.18)$$

Since Y'_n must be equal to Y_n within a scale factor of C_{an}/C_n , that is,

$$Y'_n = \frac{C_{an}}{C_n} Y_n = j\omega C_{an} + \frac{C_{an}}{C_n} \frac{1}{R_{n+1}} \quad (5.19)$$

Equating the second terms in Equation 5.18 and Equation 5.19, yields

$$J_{n,n+1} = \sqrt{\frac{C_{an}G_B}{C_n R_{n+1}}} = \sqrt{\frac{C_{an}G_B}{g_n g_{n+1}}} \quad (5.20)$$

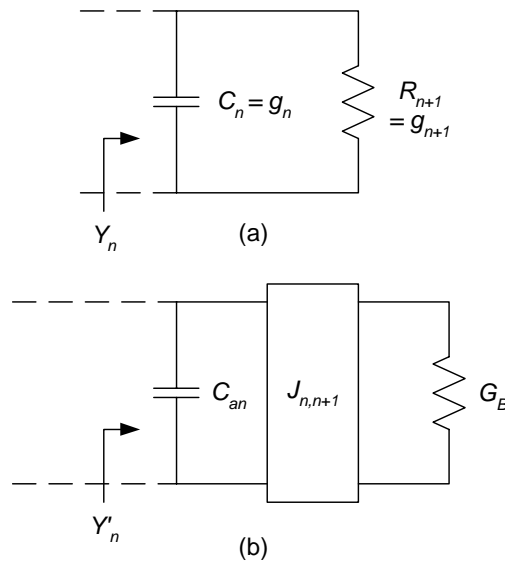


Figure 5.6: End section of the lowpass prototype circuit is shown in (a) and the corresponding end section of Figure 5.3 is shown in (b).

which is equal to the equation shown in Figure 5.3. Following exactly the same procedure, it can be shown that

$$J_{01} = \sqrt{\frac{G_A C_{a1}}{g_0 g_1}} \quad (5.21)$$

Now that the equations given in Figure 5.3 have been derived, the next step is to transform the lowpass circuit to an equivalent bandpass form. This is accomplished by using the lowpass-to-bandpass mapping [40, 42]

$$\omega' = \frac{\omega_1'}{B} \left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right) \quad (5.22)$$

where B is the fractional bandwidth, defined as

$$B = \frac{\omega_2 - \omega_1}{\omega_0} \quad (5.23)$$

and ω_0 is the centre frequency equal to the geometric mean of the passband edges, that is,

$$\omega_0 = \sqrt{\omega_2 \omega_1} \quad (5.24)$$

If the lowpass-to-bandpass transformation is applied to a capacitor with admittance $Y = sC = j\omega' C$, the admittance becomes

$$\begin{aligned} Y_p &= j\omega' C = j \frac{\omega_1'}{B} \left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right) C = j \frac{\omega_1' \omega C}{B \omega_0} - j \frac{\omega_1' \omega_0 C}{B \omega} \\ \therefore Y_p &= j\omega \left(\frac{\omega_1' C}{B \omega_0} \right) + \frac{1}{j\omega \left(\frac{B}{\omega_1' \omega_0 C} \right)} = j\omega C_p + \frac{1}{j\omega L_p} \end{aligned} \quad (5.25)$$

which has the form of a parallel LC combination. The element transformation is shown in Figure 5.7.

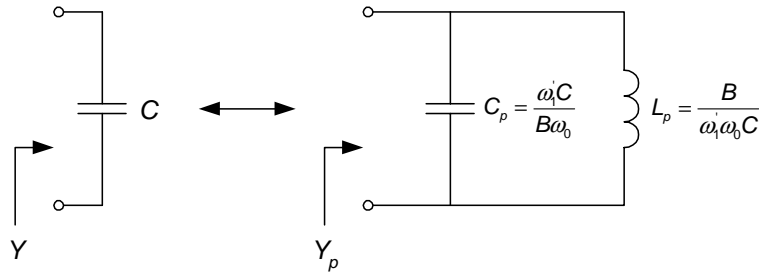


Figure 5.7: Basic lowpass-to-bandpass element transformation.

Figure 5.8 shows the bandpass transformation applied to the lowpass filter of Figure 5.3. Note that in the ideal case, the admittance inverters are independent of frequency, and are therefore left unchanged by the transformation. The same holds for the source and load conductances.

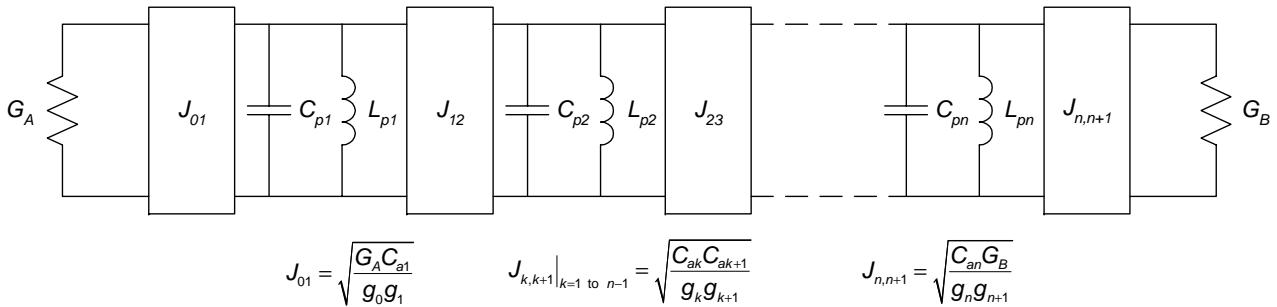


Figure 5.8: Lowpass filter circuit transformed to a bandpass filter.

The filter of Figure 5.8 consists of lumped element resonators. At microwave frequencies, it becomes increasingly more difficult to realise lumped elements. Resonators at high frequencies are often realised with distributed elements, or a combination of both lumped and distributed elements.

As a basis for establishing the resonance properties of shunt resonators regardless of its form, it is convenient to define a susceptance slope parameter [40, 42]

$$b = \frac{\omega_0}{2} \left. \frac{dB(\omega)}{d\omega} \right|_{\omega=\omega_0} \tag{5.26}$$

where $B(\omega)$ is the susceptance of the resonator.

Consider the shunt LC resonator shown in Figure 5.9. The admittance seen looking into the resonator is equal to

$$Y = j\omega C + \frac{1}{j\omega L} = j \left(\omega C - \frac{1}{\omega L} \right) = jB(\omega) \tag{5.27}$$

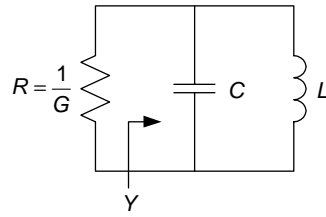


Figure 5.9: Lumped element shunt resonator.

The susceptance slope parameter is calculated as

$$b = \frac{\omega_0}{2} \left. \frac{dB(\omega)}{d\omega} \right|_{\omega=\omega_0} = \frac{\omega_0}{2} \left(C + \frac{1}{\omega_0^2 L} \right) = \frac{\omega_0}{2} (2C) = \omega_0 C \quad (5.28)$$

Rearranging terms in Equation 5.28 yields

$$C = \frac{1}{2} \left. \frac{dB(\omega)}{d\omega} \right|_{\omega=\omega_0} \quad (5.29)$$

The loaded quality factor of the shunt resonator is equal to

$$Q = \frac{R}{X} = \frac{R}{\left(\frac{1}{\omega_0 C} \right)} = R\omega_0 C \quad (5.30)$$

Expressed in terms of the susceptance slope parameter, it becomes

$$Q = R\omega_0 C = R\omega_0 \left(\frac{1}{2} \left. \frac{dB(\omega)}{d\omega} \right|_{\omega=\omega_0} \right) = Rb = \frac{b}{G} \quad (5.31)$$

Returning to Figure 5.8, the circuit can be generalised to accommodate for any type of resonator. From Equation 5.28,

$$b_k = \omega_0 C_{pk} \quad (5.32)$$

where $k = 1, 2, \dots, n - 1$. Substituting the value of C_p shown in Figure 5.7 into Equation 5.32 and rearranging terms, yields

$$b_k = \omega_0 C_{pk} = \omega_0 \left(\frac{\omega'_1 C_{ak}}{B\omega_0} \right) = \frac{\omega'_1 C_{ak}}{B} \quad (5.33)$$

$$\therefore C_{ak} = \frac{b_k B}{\omega'_1} \quad (5.34)$$

Similarly

$$b_{k+1} = \omega_0 C_{pk+1} = \omega_0 \left(\frac{\omega'_1 C_{ak+1}}{B \omega_0} \right) = \frac{\omega'_1 C_{ak+1}}{B} \quad (5.35)$$

$$\therefore C_{ak+1} = \frac{b_{k+1} B}{\omega'_1} \quad (5.36)$$

Substituting Equation 5.34 and Equation 5.36 into Equation 5.16, yields

$$J_{k,k+1}|_{k=1 \text{ to } n-1} = \sqrt{\frac{C_{ak} C_{ak+1}}{g_k g_{k+1}}} = \sqrt{\frac{\left(\frac{b_k B}{\omega'_1} \right) \left(\frac{b_{k+1} B}{\omega'_1} \right)}{g_k g_{k+1}}} = \frac{B}{\omega'_1} \sqrt{\frac{b_k b_{k+1}}{g_k g_{k+1}}} \quad (5.37)$$

Repeating the same process for J_{01} and $J_{n,n+1}$, yields

$$J_{01} = \sqrt{\frac{G_A C_{a1}}{g_0 g_1}} = \sqrt{\frac{G_A b_1 B}{\omega'_1 g_0 g_1}} \quad (5.38)$$

and

$$J_{n,n+1} = \sqrt{\frac{C_{an} G_B}{g_n g_{n+1}}} = \sqrt{\frac{b_n B G_B}{\omega'_1 g_n g_{n+1}}} \quad (5.39)$$

The coupling coefficient is defined as

$$k_{k,k+1}|_{k=1 \text{ to } k=n-1} = \frac{J_{k,k+1}}{\sqrt{b_k b_{k+1}}} \quad (5.40)$$

which is a generalisation of the usual definition of the coupling coefficient. For lumped element resonators with inductive couplings, $k_{k,k+1} = M_{k,k+1} / \sqrt{L_k L_{k+1}}$, where L_k and L_{k+1} are self inductances and $M_{k,k+1}$ is the mutual inductance [40].

Substituting Equation 5.37 into Equation 5.40 yields

$$k_{k,k+1}|_{k=1 \text{ to } k=n-1} = \frac{\frac{B}{\omega'_1} \sqrt{\frac{b_k b_{k+1}}{g_k g_{k+1}}}}{\sqrt{b_k b_{k+1}}} = \frac{B}{\omega'_1 \sqrt{g_k g_{k+1}}} \quad (5.41)$$

The external quality factor at the source side, is the quality factor of the first resonator $B_1(\omega)$, coupled by the inverter J_{01} to the source impedance G_A . It is equal to

$$Q_A = \frac{b_1}{(J_{01}^2 / G_A)} = \frac{g_0 g_1 \omega'_1}{B} \quad (5.42)$$

In a similar fashion the external quality factor at the load side is found to be

$$Q_B = \frac{b_n}{\left(J_{n,n+1}^2 / G_B\right)} = \frac{g_n g_{n+1} \omega_1'}{B} \tag{5.43}$$

where Equation 5.9, Equation 5.31, Equation 5.38 and Equation 5.39 have been used.

Figure 5.10 shows the generalised bandpass filter form and equations for the external quality factors and coupling coefficients that are valid for any type of resonator.

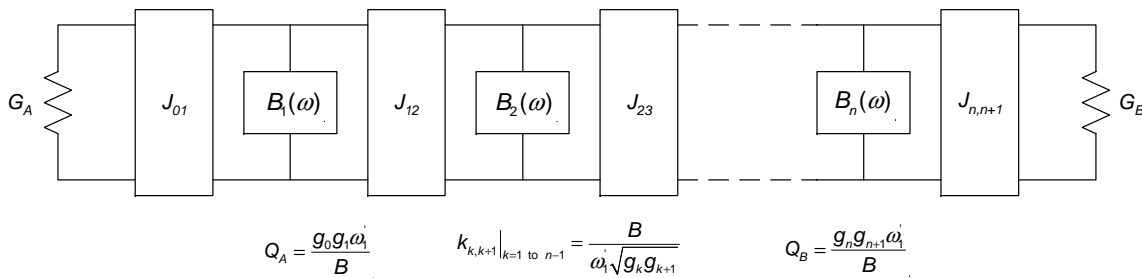


Figure 5.10: Generalised bandpass filter circuit comprised of admittance inverters and shunt resonators.

5.3 Equivalent Electrical Circuit, Coupling Coefficients and External Quality Factors of the Comblines and Interdigital Filters

The previous section derived a generalised bandpass filter circuit from a lowpass prototype circuit. Just how well this bandpass filter response reflects the original lumped element lowpass prototype response, depends on how well the susceptances of the distributed or mixed element resonators approximate the susceptances of the lumped element resonators. Ideally, they should be equal at all frequencies, but in practice the susceptances are only equal close to resonance, limiting the accuracy of the equations to bandpass filters of narrow to moderate bandwidth.

The external quality factors and coupling coefficients of the prototype bandpass filter were derived and are given in terms of the lowpass prototype element values in Equations 5.41 - 5.43. These equations are all that is required to set the desired response of the bandpass filter.

In the next section, the physical structure of the combline filter is transformed into an equivalent bandpass form like that shown in Figure 5.10. The aim of Section 5.3.1 is to derive equations for the coupling coefficients and external quality factors of the combline bandpass filter. Section 5.3.2 repeats the process for the interdigital filter.

5.3.1 Comblines Filter

Figure 5.11 shows the physical structure of an n^{th} -order combline filter in stripline form. The resonators in this type of filter consist of transverse electromagnetic (TEM) mode transmission line elements that are short-circuited at one end and have a lumped capacitance, C_k ($k = 1$ to n), between the other end of each resonator line element and ground. Lines 0 and $n + 1$ are impedance transforming sections. With the capacitors C_k present, the resonator lines will be less than $\lambda_0/4$ long at resonance, where λ_0 is the wavelength in the medium of propagation at midband [41].

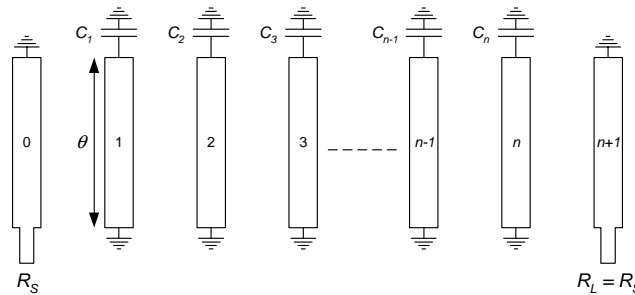


Figure 5.11: Physical representation of the combline filter.

The equivalent electrical circuit of the combline filter can be found by using the transformations found in references such as [40, 41], relating TEM circuits to the open-wire line circuits that are electrically equivalent. The two transformations used are given in Table 5.1.

Table 5.1: Equivalent open-wire line circuits for two TEM networks.

TEM Circuit	Equivalent Open-Wire Line Circuit
<p>Diagram of a TEM circuit with two parallel strips, labeled 'a' and 'b', of length θ. Strip 'a' is connected to port 1 and has admittances Y_{oo}^a, Y_{oe}^a. Strip 'b' is connected to port 2 and has admittances Y_{oo}^b, Y_{oe}^b.</p>	<p>Diagram of the equivalent open-wire line circuit. It consists of two parallel strips of length θ. The admittance between the strips is $Y_{ab} = vC_{ab} = \frac{Y_{oo}^a - Y_{oe}^a}{2}$. The admittance of strip 'a' is $Y_a = vC_a = Y_{oe}^a$. The admittance of strip 'b' is $Y_b = vC_b = Y_{oe}^b$.</p>
<p>Diagram of a TEM circuit with two parallel strips, labeled 'a' and 'b', of length θ. Strip 'a' is connected to port 1 and has admittances Y_{oo}^a, Y_{oe}^a. Strip 'b' is connected to port 2 and has admittances Y_{oo}^b, Y_{oe}^b.</p>	<p>Diagram of the equivalent open-wire line circuit. It consists of two parallel strips of length θ. The admittance between the strips is $Y_{ab} = vC_{ab}$. The admittance of strip 'a' is $Y_a = vC_a = Y_{oe}^a$. The admittance of strip 'b' is $Y_b = vC_b = Y_{oe}^b$.</p>

In Table 5.1, Y_{oo}^a and Y_{oe}^a are the odd and even mode admittances for strip a , respectively. Y_{oo}^b and Y_{oe}^b are the odd and even mode admittances for strip b . C_a and C_b are the self capacitances, that

is, the capacitances per unit length between strip a and ground and between strip b and ground, respectively. C_{ab} is the mutual capacitance, that is, the capacitance per unit length between strips.

The characteristic admittance of a lossless uniform transmission line operated in the TEM mode, is related to its shunt capacitance by

$$Y_0 = vC = \frac{\sqrt{\epsilon_r}C}{\eta_0\epsilon} = \frac{\sqrt{\epsilon_r}C'}{\eta_0} \quad (5.44)$$

where

- v is the speed of propagation along the line
- ϵ_r is the relative dielectric constant of the medium
- ϵ is the permittivity of the medium
- η_0 is the impedance of free space

The dimensionless ratio $C' = \frac{C}{\epsilon}$ simplifies the symbols and can be used directly with the equations given by Perlow to obtain physical dimensions of the filters [43]. This is discussed in more detail in later sections.

Figure 5.12(a) shows the equivalent electrical circuit of a third-order combline filter, where the transformations of Table 5.1 have been used. The circuit in (b) is obtained in two steps. The first step is to apply the Kuroda identity shown in Figure 5.13 at the source and load side of the circuit. The second step is adding lines of negative mutual admittance in parallel with the resonator lines to obtain admittance inverters of the form shown in Figure 5.4.

To further transform the circuit of Figure 5.12(b), recall that the input impedance of a short-circuited transmission line of length ℓ and characteristic impedance Z_0 is, in terms of Richards' variable, given by

$$Z_{sh} = jZ_0 \tan(\beta\ell) = Z_0 j \tan(\theta) = SZ_0 \quad (5.45)$$

where Richards' variable is defined as

$$S|_{s=j\omega} = \Sigma + j\Omega|_{s=j\omega} = \tanh(sT)|_{s=j\omega} = \tanh(j\omega T) = j \tan(\omega T) = j \tan\left(\omega \frac{\ell}{v}\right) = j \tan(\theta) \quad (5.46)$$

and where $\beta = \frac{2\pi}{\lambda}$ [13].

Equation 5.45 shows that a short-circuited transmission line, in terms of S , behaves like a lumped inductor of value $L = Z_0$. The circuit of Figure 5.12(c) is found by replacing the short-circuited transmission lines with S -plane inductors, and by bringing all the circuitry connected to the exterior terminals of the transformers across to the other side.

The circuit shown in Figure 5.12(c) has a similar form compared to that shown in Figure 5.10, that is, it consists of shunt resonators and admittance inverters only.

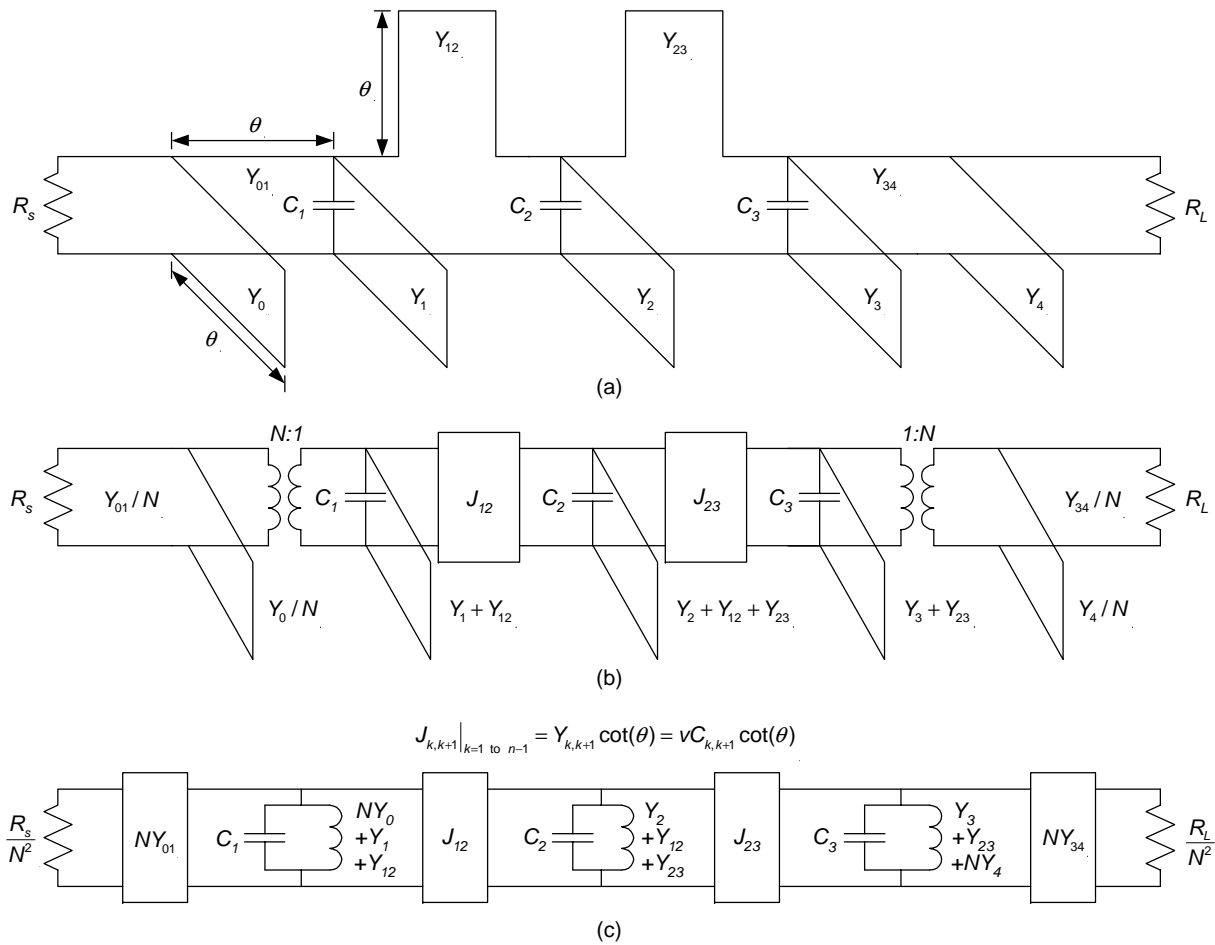


Figure 5.12: Equivalent electrical circuit of the combline filter.

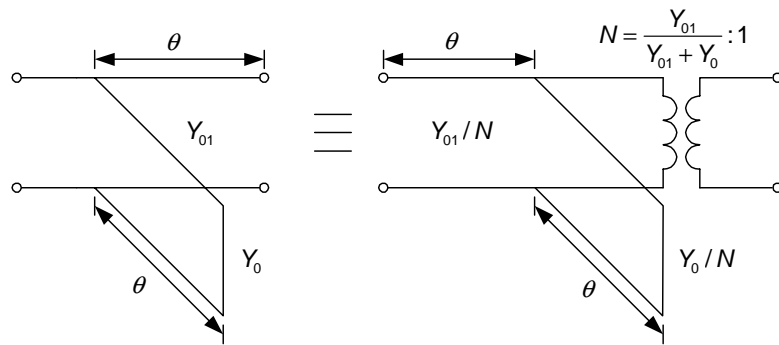


Figure 5.13: One of Kuroda's identities.

To find the external quality factor at the source side, recall that the input impedance Z_{in} seen looking into a line with characteristic impedance Z_0 and length ℓ , is given by

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan(\beta\ell)}{Z_0 + jZ_L \tan(\beta\ell)} \tag{5.47}$$

where Z_L is the load connected at the end of the transmission line. To calculate the external quality

factor at the source side, consider the part of the filter circuit up to the first resonator, as shown in Figure 5.14.

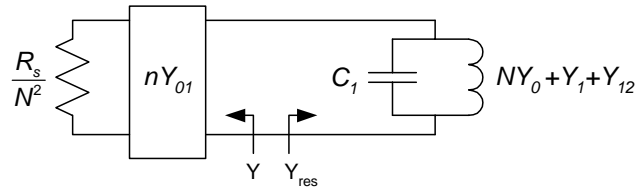


Figure 5.14: A section of the combline filter circuit up to the first resonator.

By rearranging Equation 5.47, the admittance Y , as indicated in Figure 5.14, is equal to

$$Y = \frac{NY_{01} \left[\frac{N^2}{R_s} + jNY_{01} \tan(\theta) \right]}{NY_{01} + j\frac{N^2}{R_s} \tan(\theta)} = NY_{01} \frac{\frac{N}{R_s} + jY_{01} \tan(\theta)}{Y_{01} + j\frac{N}{R_s} \tan(\theta)} = g_s + jb_s \quad (5.48)$$

Ideally, b_s should be equal to zero. This occurs when

$$R_s = \frac{1}{Y_{01} + Y_0} \quad (5.49)$$

Small values of b_s can be accommodated for by adjusting C_1 . Practical means of changing C_1 is discussed in Section 5.4.

From Equation 5.31 and Equation 5.48, the external quality factor at the source can be written as

$$Q_s = \frac{b_1}{G} = \frac{b_1}{g_s} = \frac{\frac{\omega_0}{2} \left. \frac{dB_1(\omega)}{d\omega} \right|_{\omega=\omega_0}}{g_s} \quad (5.50)$$

For the resonator under investigation

$$Y_{res} = j\omega C_1 - j(NY_0 + Y_1 + Y_{12}) \cot(\theta) = jB_1(\omega) \quad (5.51)$$

At the resonant frequency, $B_1(\omega_0) = 0$. Thus

$$\omega_0 C_1 = (NY_0 + Y_1 + Y_{12}) \cot(\theta_0) \quad (5.52)$$

where $\theta_0 = \frac{\omega_0 \ell}{v}$ is the electrical length of the lines at the centre frequency. With the help of Equation 5.51 and Equation 5.52, the susceptance slope parameter is found to be

$$b_1 = \frac{\omega_0 C_1}{2} + \frac{(NY_0 + Y_1 + Y_{12}) \omega_0 \ell}{2 \sin^2 \left(\frac{\omega_0 \ell}{v} \right) v} = (NY_0 + Y_1 + Y_{12}) \left[\frac{\cot(\theta_0)}{2} + \frac{\theta_0}{2 \sin^2(\theta_0)} \right] \quad (5.53)$$

Substituting Equation 5.53 into Equation 5.50 yields the external quality factor at the source

$$Q_S = \frac{\frac{\omega_0}{2} \left. \frac{dB_1(\omega)}{d\omega} \right|_{\omega=\omega_0}}{g_S} = \frac{(NY_0 + Y_1 + Y_{12})}{g_S} \left[\frac{\cot(\theta_0)}{2} + \frac{\theta_0}{2 \sin^2(\theta_0)} \right] \quad (5.54)$$

The external quality factor, expressed in terms of the self and mutual static capacitances, becomes

$$Q_S = \frac{\sqrt{\epsilon_r} (NC'_0 + C'_1 + C'_{12})}{\eta_0 g_S} \left[\frac{\cot(\theta_0)}{2} + \frac{\theta_0}{2 \sin^2(\theta_0)} \right] \quad (5.55)$$

where Equation 5.44 has been used. In a similar fashion, the external quality factor at the load side can be written as

$$Q_L = \frac{\frac{\omega_0}{2} \left. \frac{dB_3(\omega)}{d\omega} \right|_{\omega=\omega_0}}{g_L} = \frac{\sqrt{\epsilon_r} (NC'_4 + C'_3 + C'_{23})}{\eta_0 g_L} \left[\frac{\cot(\theta_0)}{2} + \frac{\theta_0}{2 \sin^2(\theta_0)} \right] \quad (5.56)$$

where

$$g_L = \text{Re} \left[NY_{34} \frac{\frac{N}{R_L} + jY_{34} \tan(\theta)}{Y_{34} + j\frac{N}{R_L} \tan(\theta)} \right] \quad (5.57)$$

The coupling coefficients are, with the help of Equation 5.40, expressed as

$$\begin{aligned} k_{12} &= \frac{J_{12}}{\sqrt{b_1 b_2}} = \frac{Y_{12} \cot(\theta_0)}{\sqrt{(NY_0 + Y_1 + Y_{12})(Y_{12} + Y_2 + Y_{23})} \left[\frac{\cot(\theta_0)}{2} + \frac{\theta_0}{2 \sin^2(\theta_0)} \right]} \\ &= \frac{C'_{12} \cot(\theta_0)}{\sqrt{(NC'_0 + C'_1 + C'_{12})(C'_{12} + C'_2 + C'_{23})} \left[\frac{\cot(\theta_0)}{2} + \frac{\theta_0}{2 \sin^2(\theta_0)} \right]} \end{aligned} \quad (5.58)$$

and

$$\begin{aligned} k_{23} &= \frac{J_{23}}{\sqrt{b_2 b_3}} = \frac{Y_{23} \cot(\theta_0)}{\sqrt{(Y_{12} + Y_2 + Y_{23})(NY_4 + Y_3 + Y_{23})} \left[\frac{\cot(\theta_0)}{2} + \frac{\theta_0}{2 \sin^2(\theta_0)} \right]} \\ &= \frac{C'_{23} \cot(\theta_0)}{\sqrt{(C'_{12} + C'_2 + C'_{23})(NC'_4 + C'_3 + C'_{23})} \left[\frac{\cot(\theta_0)}{2} + \frac{\theta_0}{2 \sin^2(\theta_0)} \right]} \end{aligned} \quad (5.59)$$

The coupling coefficients between the inner resonators of an n^{th} -order filter, can in general be written as

$$\begin{aligned} k_{n,n+1} &= \frac{J_{n,n+1}}{\sqrt{b_n b_{n+1}}} \\ &= \frac{C'_{n,n+1} \cot(\theta_0)}{\sqrt{(C'_{n-1,n} + C'_n + C'_{n,n+1})(C'_{n,n+1} + C'_{n+1} + C'_{n+1,n+2})} \left[\frac{\cot(\theta_0)}{2} + \frac{\theta_0}{2 \sin^2(\theta_0)} \right]} \end{aligned} \quad (5.60)$$

5.3.2 Interdigital Filter

Figure 5.15 shows the physical structure of an n^{th} -order interdigital filter.

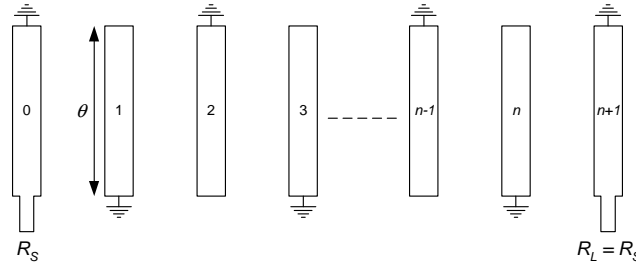


Figure 5.15: Physical structure of an interdigital filter.

The structure depicted in Figure 5.15 consists of TEM mode resonators in stripline form. Each resonator element is a quarter-wavelength long at the midband frequency and is short-circuited at one end and open-circuited at the other end. As with the combline filter, the input and output lines serve as impedance matching elements.

The equivalent electrical circuit of the interdigital filter can be found by using the transformation shown in Table 5.1, and by using Kuroda's identity as given in Figure 5.13. The equivalent circuit of a fifth-order interdigital filter is depicted in Figure 5.16. In this case, each quarter wavelength transmission line acts as an admittance inverter, with $J = Y_0$. The short-circuited transmission lines that appear as S-plane inductors in Figure 5.16(c), act as the resonators.

The external quality factor at the source side, can be found by evaluating the part of the circuit up to the first admittance inverter. The equivalent circuit is depicted in Figure 5.17.

The admittance Y_{res} , is equal to

$$Y_{res} = -j(NY_0 + Y_1 + Y_{12}) \cot(\theta) = -j(NY_0 + Y_1 + Y_{12}) \cot\left(\frac{\omega\ell}{v}\right) = jB_1(\omega) \quad (5.61)$$

The derivative of $B_1(\omega)$ with respect to frequency, is equal to

$$\frac{dB_1(\omega)}{d\omega} = \frac{(NY_0 + Y_1 + Y_{12})\ell}{v \sin^2\left(\frac{\omega\ell}{v}\right)} \quad (5.62)$$

The external quality factor at the source side is equal to

$$Q_S = \frac{b_1}{G} = \frac{\frac{\omega_0}{2} \left. \frac{dB_1(\omega)}{d\omega} \right|_{\omega=\omega_0}}{Y_{01}^2 R_S} = \frac{(NY_0 + Y_1 + Y_{12})\theta_0}{2Y_{01}^2 R_S \sin^2(\theta_0)} \quad (5.63)$$

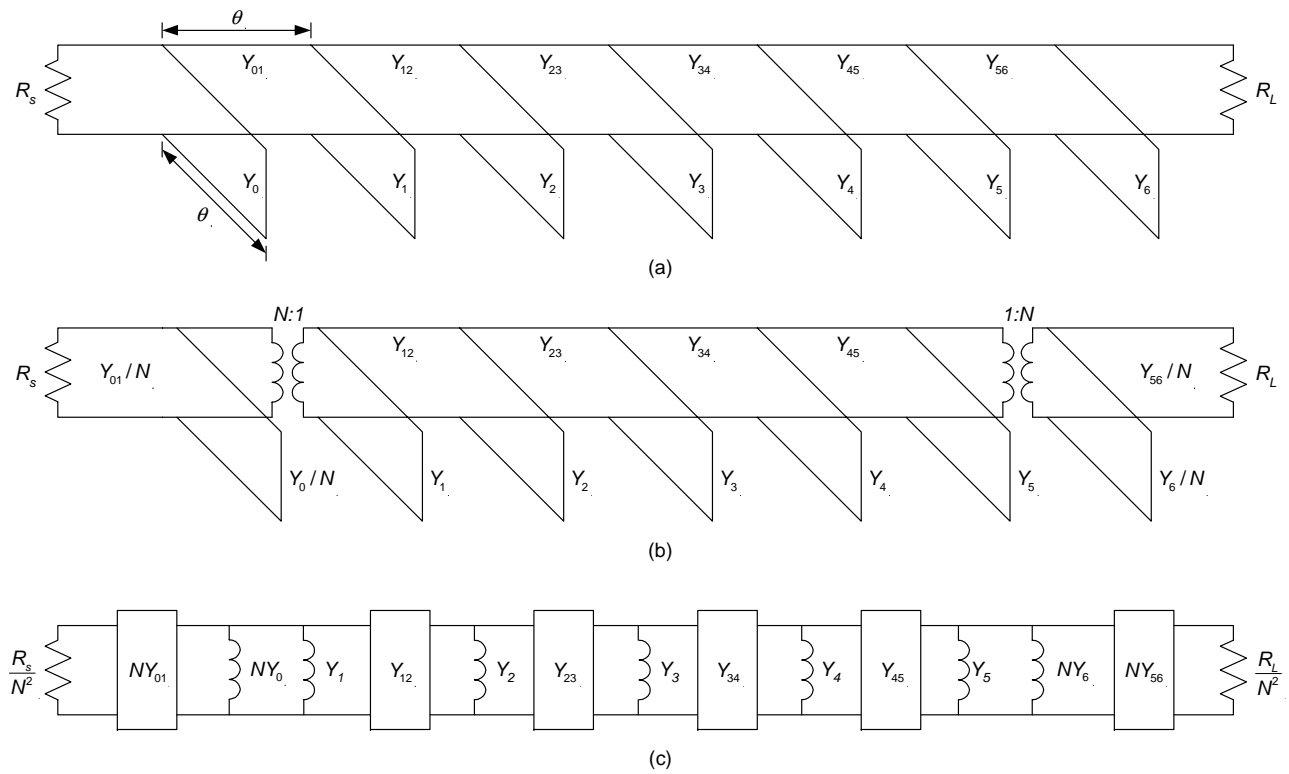


Figure 5.16: Equivalent electrical circuit of a fifth-order interdigital filter.

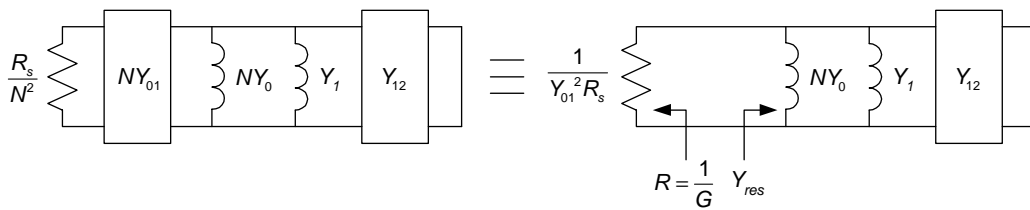


Figure 5.17: Equivalent circuit to determine the loaded quality factor at the source.

For an interdigital filter $\theta_0 = \frac{\pi}{2}$. Therefore, Equation 5.63 reduces to

$$Q_S = \frac{(NY_0 + Y_1 + Y_{12}) (\pi/2)}{2Y_{01}^2 R_S \sin^2 (\frac{\pi}{2})} = \frac{\pi (NY_0 + Y_1 + Y_{12})}{4Y_{01}^2 R_S} \tag{5.64}$$

Writing Equation 5.64 in terms of its self and mutual capacitances, yields

$$Q_S = \frac{\pi \eta_0 (NC'_0 + C'_1 + C'_{12})}{4\sqrt{\epsilon_r} C_{01}'^2 R_S} \tag{5.65}$$

The external quality factor at the load can be found in a similar way, and is given by

$$Q_L = \frac{\pi \eta_0 (NC'_6 + C'_5 + C'_{45})}{4\sqrt{\epsilon_r} C_{56}'^2 R_L} \tag{5.66}$$

From the definition of the coupling coefficient given by Equation 5.40, the coupling coefficient between the first and second resonators, can be written as

$$\begin{aligned} k_{12} &= \frac{J_{12}}{\sqrt{b_1 b_2}} = \frac{Y_{12}}{\sqrt{\left(\frac{(NY_0 + Y_1 + Y_{12})\theta_0}{2\sin^2(\theta_0)}\right) \left(\frac{(Y_{12} + Y_2 + Y_{23})\theta_0}{2\sin^2(\theta_0)}\right)}} \\ &= \frac{4C'_{12}}{\pi\sqrt{(NC'_0 + C'_1 + C'_{12})(C'_{12} + C'_2 + C'_{23})}} \end{aligned} \quad (5.67)$$

Similarly, the coupling coefficient between the fourth and fifth resonator is given by

$$k_{45} = \frac{J_{45}}{\sqrt{b_4 b_5}} = \frac{4C'_{45}}{\pi\sqrt{(NC'_6 + C'_5 + C'_{45})(C'_{45} + C'_4 + C'_{34})}} \quad (5.68)$$

The coupling coefficients for the inner resonators are in general given by

$$k_{n,n+1} = \frac{J_{n,n+1}}{\sqrt{b_n b_{n+1}}} = \frac{4C'_{n,n+1}}{\pi\sqrt{(C'_{n-1,n} + C'_n + C'_{n,n+1})(C'_{n,n+1} + C'_{n+1} + C'_{n+1,n+2})}} \quad (5.69)$$

These equations show that calculation of the external quality factors and coupling coefficients reduces to calculation of the self and mutual capacitances.

5.4 Combine Filter Design, Simulated and Measured Response

The previous two sections derived the external quality factors and coupling coefficients of the combline and interdigital filters. These parameters ensure the desired response of the filters. The response of the bandpass prototype filter of Figure 5.10 may be chosen arbitrarily by choosing the desired filter order, centre frequency, bandwidth and passband ripple in the case of a Chebyshev design. In order for the combline or interdigital filter to have the same desired response as that of the prototype circuit, the external quality factors and coupling coefficients of the combline or interdigital filter should be made equal to that of the prototype circuit.

The combline bandpass filter discussed in this section is used at the output of the multiplier chain as shown in Figure 3.2. A third-order filter with a narrow ripple bandwidth of 3% was found to be adequate. The unwanted frequency components closest to the desired 1 GHz signal, are spaced 100 MHz away. The third-order response predicts about 40 dB of attenuation at 100 MHz offset frequency from the centre frequency, significantly suppressing any unwanted spectral components obtained by the multiplication process. Undesired frequency components are furthermore suppressed by the frequency response of the PLL, ensuring a spectrally clean output.

A combline filter type was chosen for this application since they are more compact compared to interdigital filters and are capable of a broader stopband above the primary passband. Furthermore, combline filters can usually be fabricated without the use of dielectric support materials so that dielectric losses can be minimised [41].

The physical form of the combline filter designed in this chapter consists of a coupled line array of rectangular bars between parallel ground planes. The dielectric medium is air. Rectangular bars were specifically chosen so that the filter could be manufactured out of one piece of material (except for the top and bottom cover plates), ensuring a stronger physical structure and an uniform thermal expansion coefficient. Round rods could also have been used, but in this case the choice would have been limited to rods of specific diameter. In addition, the filter would also have consisted of various separate mechanical parts put together.

Figure 5.18 shows a cross section of the filter. The corresponding self and mutual capacitances of each line are shown in the figure. It will be assumed in this discussion that the thicknesses of all the bars in the array are the same and that the coupling between nonadjacent bars is negligible or so insignificant that it can easily be adjusted for.

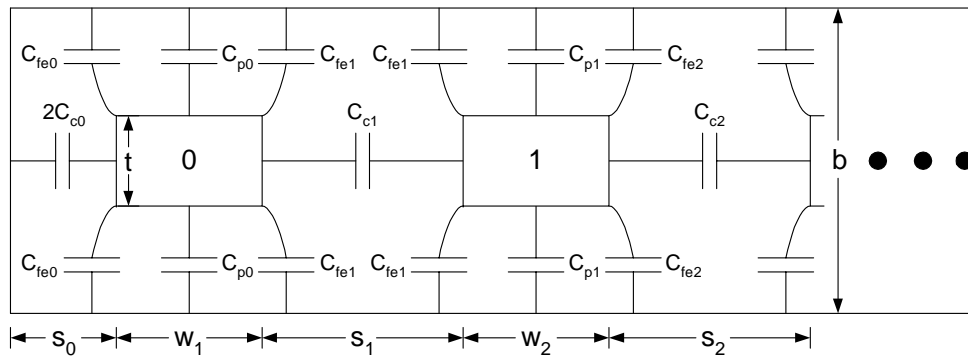


Figure 5.18: A cross section of the combline filter showing the line capacitances associated with each bar.

The total shunt capacitance of the input line is equal to

$$C_0 = 2C_{c0} + 2(C_{fe0} + C_{p0} + C_{fe1}) \tag{5.70}$$

The interior lines have two even mode fringing capacitance components and a parallel plate component. The total self or even mode capacitance is thus equal to

$$C_k = 2(C_{fek} + C_{pk} + C_{fe(k+1)}) \quad k = 1, 2, \dots, n \tag{5.71}$$

In Perlow’s paper, equations are given to calculate each of the capacitive components shown in Figure 5.18. These equations are implemented in the *Matlab* design code of the combline filter which can be found in Appendix B. The values of the line capacitances depend on the physical dimensions of the bars, the separation between them and the ground plane spacing.

The design of the combline filter reduces to equating the external quality factors and coupling coefficients of the combline filter to that of the generalised bandpass filter shown in Figure 5.10. Equation 5.55 to Equation 5.56 and Equation 5.58 to Equation 5.60 show that the external quality factors and coupling coefficients can be altered and subsequently made equal to the equations shown in Figure 5.10 by changing the line capacitances. The change in line capacitances is obtained by adjusting the separation between the bars, while keeping all the other dimensions fixed. An iterative process can be performed whereby the separation between the bars is adjusted such that the difference between different coupling coefficients and external quality factors reduces to zero.

The execution of such an iterative process can best be performed by a computer, and also forms part of the filter design code given in Appendix B. Table 5.2 shows a list of the input parameters required from the designer.

Table 5.2: Required input parameters for the combline filter design.

Parameter	Value
Filter order (n)	3
Electrical length of the resonator lines at resonance	60°
Maximum passband reflection coefficient	−20 dB
Centre frequency	1000 MHz
Ripple bandwidth	30 MHz
Earth plane spacing (b)	12.5 mm
Bar thickness (t)	5 mm
Inner resonator bar width (w_2 to w_{n+1})	5 mm
Input and output line bar width (w_1 and w_{n+2})	5 mm
End bar spacing from side wall (s_0)	3 mm

The values listed in Table 5.2 are the actual values used for the combline filter design. The choice of electrical length, the dimensions of the lines and the sidewall spacing yielded practical bar spacings. The bar spacings returned from the design code are given in Table 5.3, where S_1 to S_4 are the bar spacings as defined in Figure 5.18. The resonator capacitances (C_1 , C_2 , and C_3 in Figure 5.12) are found by using Equation 5.52, while for the inner resonators, the capacitance is calculated using

$$C_k = \frac{\sqrt{\epsilon_r} \left(C'_{k-1,k} + C'_k + C'_{k,k+1} \right) \cot(\theta_0)}{2\pi f_0 \eta_0} \quad k = 2, 3, \dots, n-1 \quad (5.72)$$

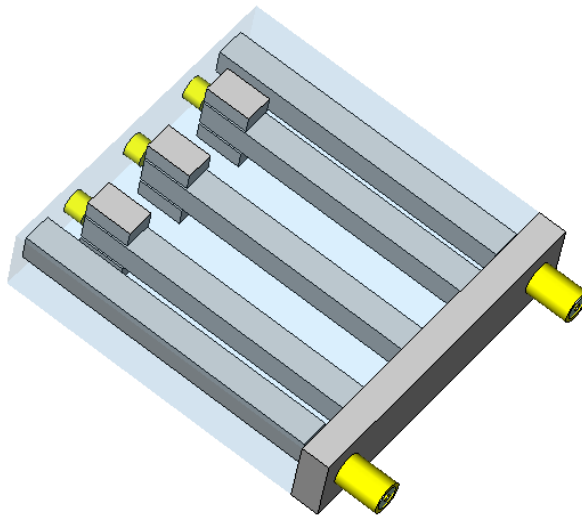
The values of the resonator capacitances obtained with the design code are also given in Table 5.3.

To verify and optimise the design, the filter is modelled in *Computer Simulation Technology (CST)*. Figure 5.19 shows a model of the combline filter implemented in *CST*.

The resonator capacitances that appear in parallel with the resonator lines, are each comprised of a fixed and variable capacitance. The fixed part of the capacitance consists of the capacitance that exists between the end section of each resonator line and the small rectangular blocks located on the top and bottom cover plates of the filter. This is also visible in the *CST* model. Care was taken not

Table 5.3: Combine bar spacings and resonator capacitances returned from the *Matlab* design code.

Parameter	Value
S1	4.1 mm
S2	9.06 mm
S3	9.06 mm
S4	4.1 mm
C1	1.6 pF
C2	1.57 pF
C3	1.6 pF

**Figure 5.19:** CST model of the combline filter.

to perturb the line capacitances of the resonator lines too much by making the rectangular blocks too long.

The capacitance between two parallel surfaces is given by

$$C = \frac{\epsilon A}{d} = \frac{\epsilon_0 \epsilon_r A}{d} \quad (5.73)$$

where A is the area of the surface in square meters, and d is the distance in meters between the surfaces. The fixed portion of the capacitance, is found to be

$$C = \frac{\epsilon A}{d} = 2 \left(\frac{8.854 \times 10^{-12} (8 \times 10^{-3} \times 5 \times 10^{-3})}{0.5 \times 10^{-3}} \right) = 1.42 \text{ pF} \quad (5.74)$$

The variable capacitance is obtained by using *Temex* tuning screws at the end of each resonator line. Figure 5.20 shows a picture of the tuning element used for the combline filter. The tuning elements are also visible in the CST model.

The tuning element consists of a threaded mounting bushing and a self locking rotor screw. By

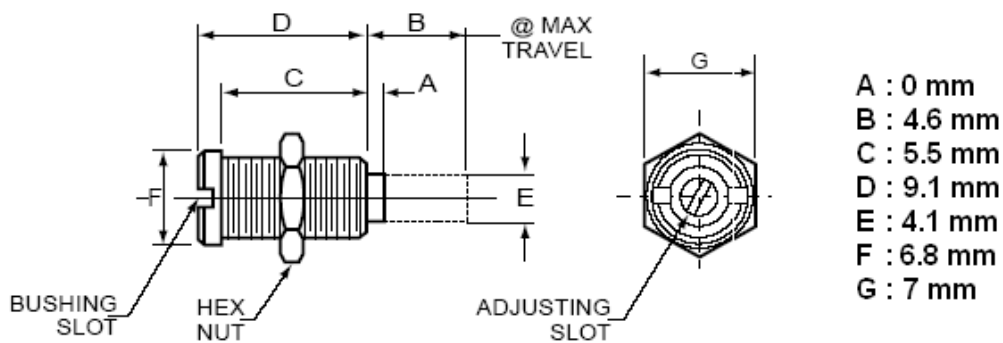


Figure 5.20: Temex AT6926-10SL tuning element.

adjusting the length of the tuning screw, the gap size between the resonator line and tuning screw is varied, in turn varying the capacitance.

To make manufacturing possible, a minimum gap size of 4 mm between the end of each resonator line and the vertical back wall of the filter was required, forcing the input and output lines to be 4 mm longer than what was designed for. Although the theory does not account for this, the solution obtained with *CST* shows that it has no significant influence on the response of the filter.

The SMA connectors are also modelled in *CST*. The physical dimensions were obtained from the manufacturer. At the transition from the SMA connectors to the transmission lines, there is an associated discontinuity. The SMA to transmission line transition is depicted in Figure 5.21.

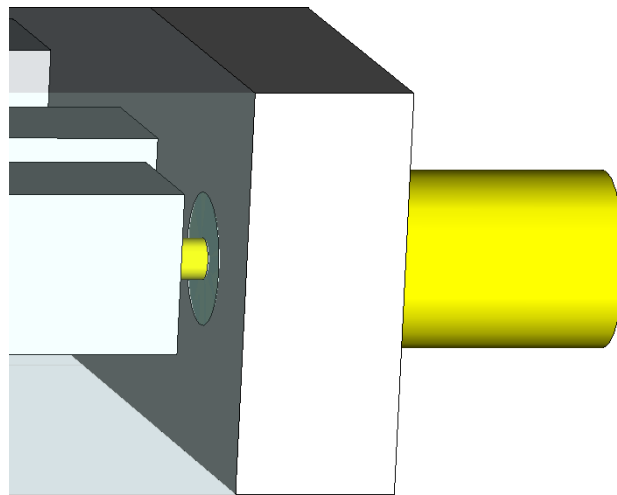


Figure 5.21: SMA to transmission line transition.

In practice, a hole with a diameter a fraction larger than the SMA centre pin diameter was drilled into the lines to accommodate for a short piece of the SMA centre pin. Conductive epoxy was used to ensure a high quality electrical connection between the SMA centre pin and transmission line.

The gap size between the vertical front wall of the filter and the input and output transmission lines influences the effect of the transition. The transition was investigated and optimised by modelling the problem in *CST*. Through iteration, a gap size of 1.3 mm was found to be sufficient.

Figure 5.22 shows the simulated response of the combline filter. Both the *Eigenmode* and *Transient* solvers of *CST* yielded similar results. The number of mesh cells was increased to the point where a further increase did not change the solution obtained, ensuring accurate results.

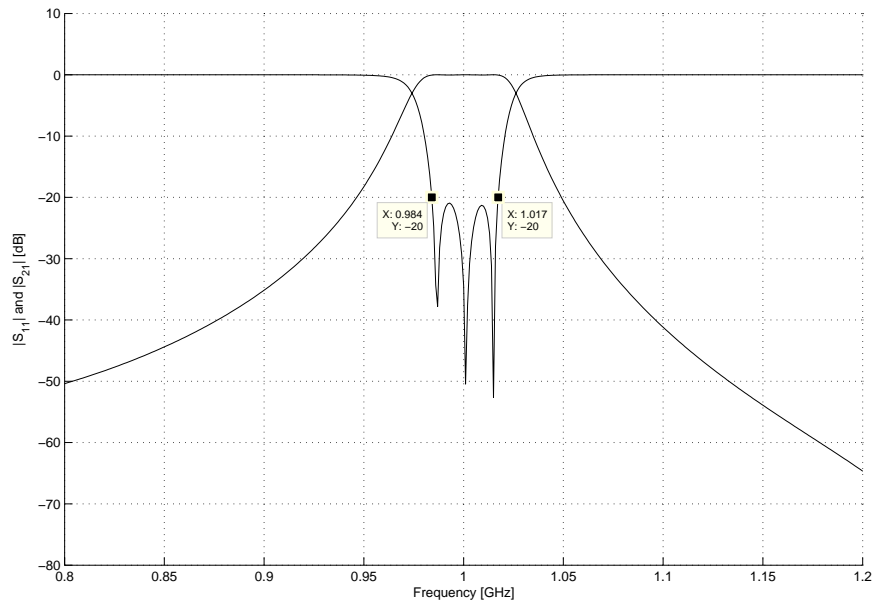


Figure 5.22: Simulated combline filter response obtained with *CST*.

The predicted filter response obtained with *CST* is very close to the design specifications. Note that the centre frequency is indeed 1 GHz. The Chebyshev response is clearly noticeable by the characteristic equal ripple visible in $|S_{11}|$. The ripple bandwidth is equal to 3.3%, slightly larger than the specification of 3%. Note that, as required by the design specification, the reflection coefficient in the passband does not exceed -20 dB.

Hardly any change in bar spacings obtained with the *Matlab* design code was necessary to obtain the desired filter response, illustrating the accuracy by which the filter can be described mathematically. Through *CST* optimisation, the most significant modification was the change of $S1 = S4 = 4.1$ mm to $S1 = S4 = 3.85$ mm, representing a 6.09% change. The final optimised *CST* filter dimensions used for manufacturing are given in Appendix D.

Figure 5.23 shows a photo of the manufactured filter. The combline filter was measured on a *Rohde & Schwarz* ZVB vector network analyser (VNA). Figure 5.24 shows a photo of the measurement setup.

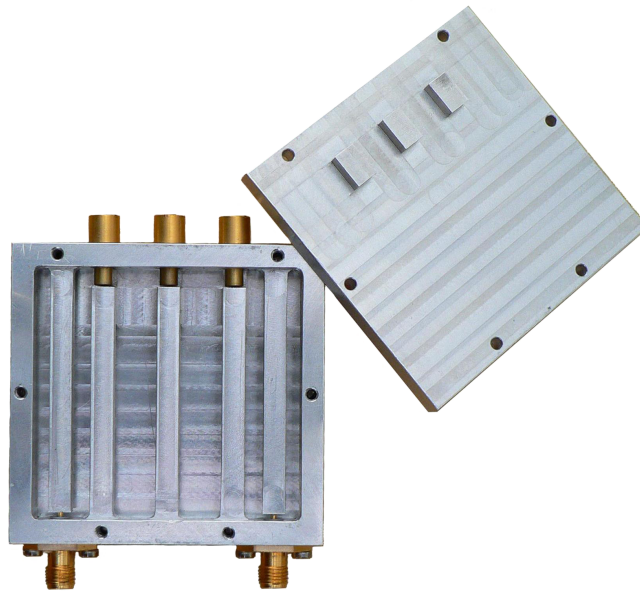


Figure 5.23: A photo of the manufactured combline filter.

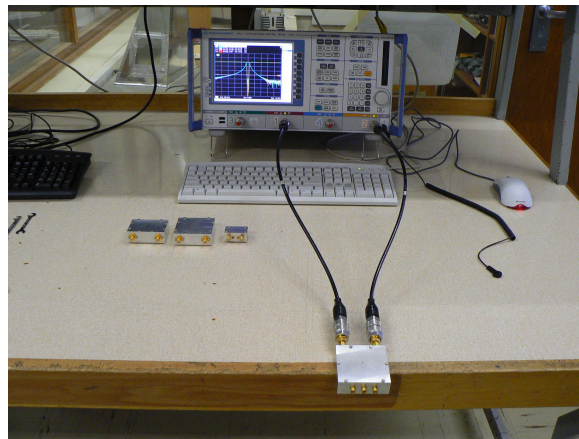


Figure 5.24: Combline filter measurement setup.

Figure 5.25 shows the measured narrow and wideband frequency response of the combline filter obtained with the VNA. The CST solution is superimposed onto the narrowband measurement for comparison.

Note the excellent agreement between the simulated and measured response. The maximum measured passband reflection coefficient exceeds -20 dB only marginally. The attenuation of the filter at 900 MHz and 1.1 GHz is equal to 36 dB and 41 dB, respectively. This is close to the predicted attenuation of about 40 dB at 100 MHz offset from the centre frequency. The ripple bandwidth is equal to 3.54%, which is very close to the simulated 3.3% obtained with CST. The maximum insertion loss in the passband is equal to 0.74 dB. Note the second passband of the filter which is centered around 3.77 GHz. This secondary passband is inherent to the periodicity encountered in transmission line resonators.

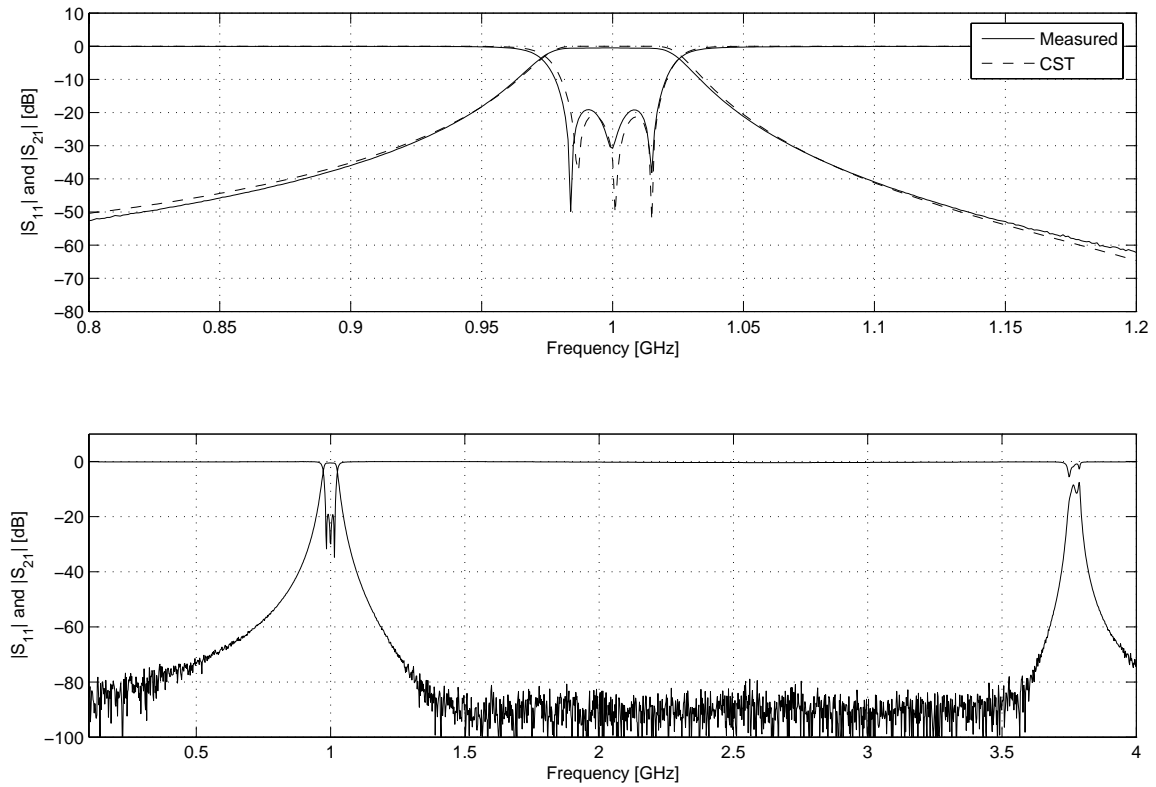


Figure 5.25: Measured and simulated frequency response of the combline filter.

5.5 Interdigital Filter Design, Simulated and Measured Response

The design of the interdigital filter follows essentially the same procedure as described in the previous section. The interdigital bandpass filter is used at the output of the frequency synthesiser, as shown in Figure 3.4. A fifth-order filter was found to be adequate, giving about 40 dB attenuation at an offset frequency of 2 GHz from the centre frequency. Since the frequency synthesiser produces signals in a 2 GHz band, the ripple bandwidth of the filter needs to be at least 2 GHz. A ripple bandwidth of 2.1 GHz was chosen.

The design of the interdigital filter again reduces to computing the external quality factors and coupling coefficients from the physical dimensions and equating them to the equations shown in Figure 5.10. The design code which performs this iterative process is given in Appendix B. It is essentially the same as the combline filter design code, except that different equations are used for the calculation of the external quality factors and coupling coefficients. These equations were derived in Section 5.3.2.

Table 5.4 shows the input parameters that are required from the designer. The values shown are the actual values used for the design, and were found to result in the most practical bar spacings. A lower limit of 2 mm was placed on the thicknesses and widths of the bars to minimise the risk of mechanical failure during the manufacturing process.

Table 5.4: Required input parameters for the interdigital filter design.

Parameter	Value
Filter order	5
Maximum passband reflection coefficient	−20 dB
Centre frequency	6470 MHz
Ripple bandwidth	2100 MHz
Earth plane spacing (b)	6.5 mm
Bar thickness (t)	2 mm
Inner resonator bar width (w_2 to w_{n+1})	2 mm
Input and output line bar width (w_1 and w_{n+2})	2 mm
End bar spacing from side wall (s_0)	2.2 mm

Table 5.5: Interdigital filter bar spacings.

Parameter	Theoretical Value	Optimised CST Value
S1	0.78 mm	0.8 mm
S2	1.87 mm	2.23 mm
S3	2.54 mm	2.83 mm
S4	2.54 mm	2.83 mm
S5	1.87 mm	2.23 mm
S6	0.78 mm	0.8 mm

The bar spacings returned from the *Matlab* code are listed in Table 5.5, where S_1 to S_6 are the bar spacings as defined in Figure 5.18. Also shown in the table are the optimised spacings obtained with *CST*.

Figure 5.26 shows the *CST* model of the filter. The total length of the cavity is equal to 11.58 mm ($\theta = 90^\circ$). Note that the one end of each resonator line needs to be open-circuited. Practically this requires the resonator lines to be somewhat shorter than $\theta = 90^\circ$. Since this change in length alters the line capacitances of the resonators lines, a tuning element is inserted at the end of the each line to gain control over the line capacitances of the lines. A resonator electrical length of 80° was chosen. *Temex AT6925-2 SL* tuning elements were used for tuning purposes. The tuning screw has a diameter of 1.6 mm.

Due to the decrease in resonator line length, the coupling between lines is different from that assumed in theory. Figure 5.15 shows that the theoretical model assumes coupling over the whole length (90°) of the lines. In the *CST* model and in practice, the lines are not aligned over the complete length of the lines, causing the coupling between lines to be slightly different from that calculated with theory. The same holds for the transition from the SMA connector to the input and output lines which also causes the coupling between lines to be different from theory.

The relatively wide bandwidth of the filter requires strong coupling between resonators which in turn yields small bar spacings. The smallest theoretical bar spacing is equal to 0.78 mm. This spacing is very hard to obtain accurately in practice. Due to the small spacings required, the filter had to be manufactured out of two pieces of aluminium, excluding the top and bottom cover plates.

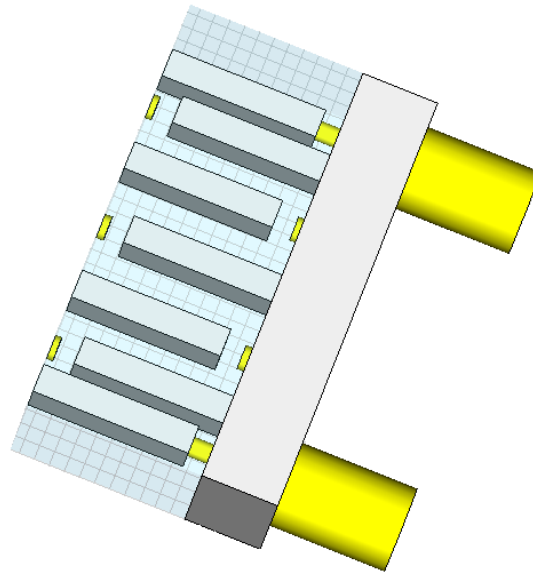


Figure 5.26: CST model of the interdigital filter.

Due to the narrow spacings between bars, there is more cross coupling between nonadjacent lines, compared to a filter of narrow bandwidth, which have larger bar spacings. Recall that the theory assumes no cross coupling between nonadjacent bars. The *CST* model is important in this regard as it takes cross coupling into account.

It should be noted that the theory assumes perfect admittance inverters over the frequency band of interest. This does not pose a problem for filters of narrow bandwidth like the combline filter discussed in the previous section. However, when the bandwidth becomes moderate as in the case of the interdigital filter, the practical admittance inverters only approximate the response of the theoretical admittance inverters close to resonance. Further away from resonance, the response of the inverters deviate from that of the ideal theoretical inverters.

For all the above mentioned reasons, it is fair to expect some difference between the theoretical and optimised simulated dimensions.

The final optimised filter dimensions obtained with *CST* were found through extensive iteration. A gap size of 1.3mm between the front wall of the filter and the input and output lines was again found to be optimal. The dimensions used for manufacturing can be found in Appendix D.

Figure 5.27 shows the simulated response of the filter. The reflection coefficient in the passband is smaller than or equal to -20 dB, as required.

A closer view of the passband ripple is shown in Figure 5.28. The five equal ripples visible in the passband are distinctive of the fifth-order Chebyshev response. Through *CST* optimisation, the ripple bandwidth has decreased to about 2006 MHz, representing a 4.48% decrease in bandwidth.

Figure 5.29 shows a photo of the manufactured interdigital filter with the top cover removed. The

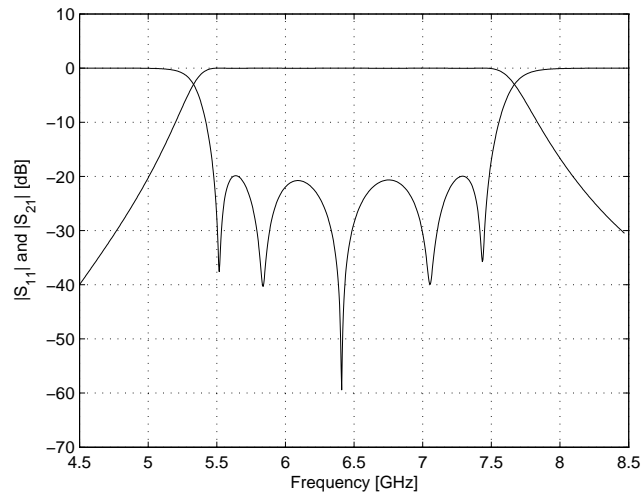


Figure 5.27: Simulated frequency response of interdigital filter obtained with CST.

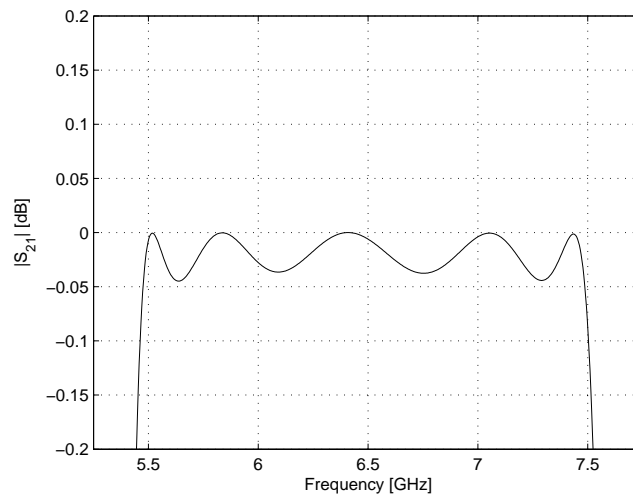


Figure 5.28: Close-up view of the interdigital filter passband ripple.

ruler in the photo gives an indication of the scale of the filter.

Figure 5.30 shows the measured S-parameters of the filter, measured on a *Rohde & Schwarz* VNA which is able to measure up to a maximum frequency of 8 GHz. The CST response is superimposed onto the measured result for comparison.

If manufacturing tolerances are taken into account, and the difficulty in constructing such a filter is appreciated, the similarity between the simulated and measured response is quite good. The difference in simulated and measured frequency response can largely be ascribed to manufacturing tolerances. The bar spacings were finely adjusted under a microscope to obtain the optimal response.

The measured reflection coefficient conforms to the maximum allowable -20 dB specification in the

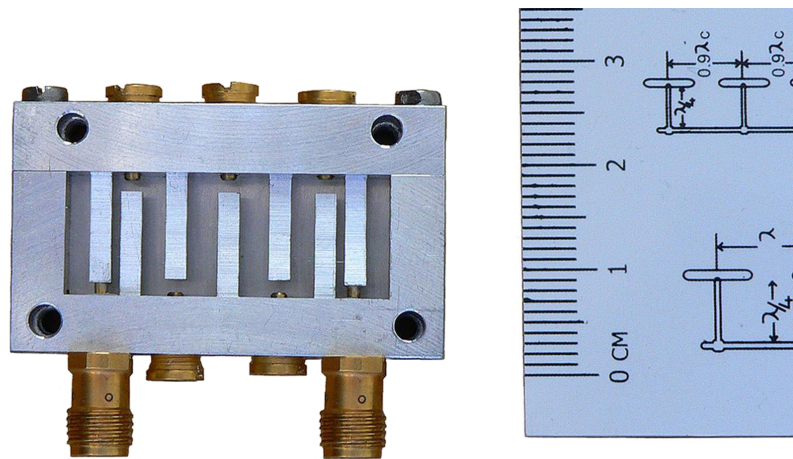


Figure 5.29: A photo of the manufactured interdigital filter with the top cover plate removed.

centre of the passband. It exceeds the specification close to the passband edges, but is nonetheless lower than -16.6 dB. The maximum insertion loss in the $5.47 - 7.47$ GHz frequency band occurs at the low frequency end, and is equal to 1.35 dB.

Figure 5.31 shows a wideband measurement performed on an HP8510 VNA. As with the combline filter, the interdigital filter has a secondary passband centered at about 19 GHz.

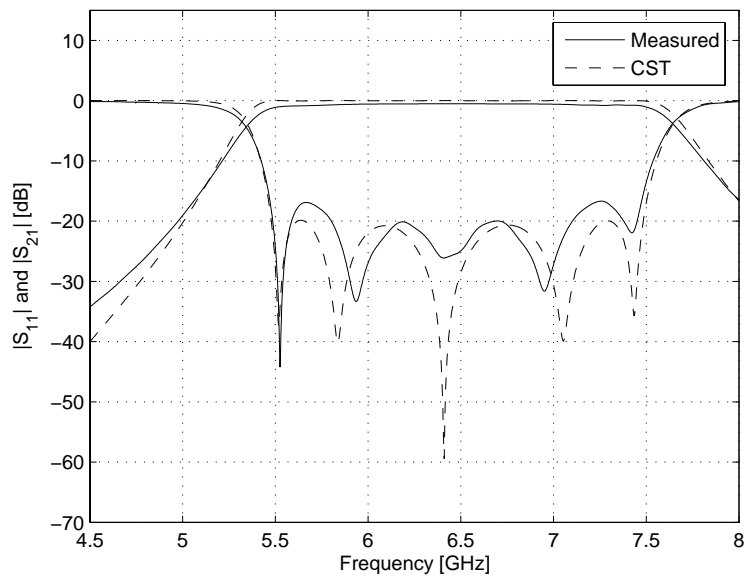


Figure 5.30: Measured frequency response of the interdigital filter.

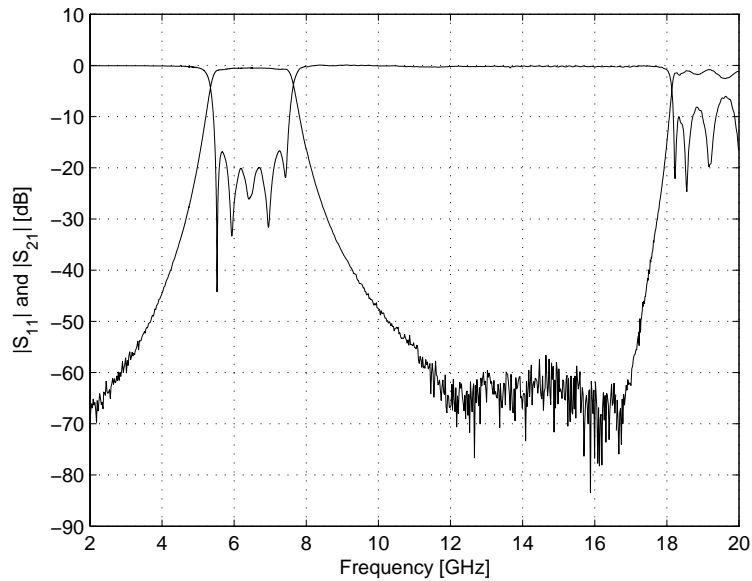


Figure 5.31: Wideband frequency response of the interdigital filter.

5.6 Conclusion

This chapter discussed the theory, design, modelling, optimisation and measured response of two microwave filters required for the frequency synthesiser. In the first section of this chapter a general bandpass circuit topology that could accommodate the use of both lumped and distributed element resonators was found. Equations were derived that related the coupling and external quality factors to the original lowpass prototype circuit elements.

Section 5.3 was devoted to finding equations for the coupling and external quality factors of the combline and interdigital filters. It was shown that the physical structures of both filters could be transformed into a form similar to that of the general bandpass filter circuit.

CST was used to verify and optimise the design of the filters. Care was taken to model all the practical aspects of the filters not taken into account by theory. Excellent agreement between the simulated, measured and theoretical response was obtained for the combline filter. For the interdigital filter, good agreement between the simulated and measured response was obtained. It was seen that, due to the small size and moderate bandwidth of the filter, some optimisation of the bar spacings was required to account for a number of practical aspects not taken into account by theory.

Chapter 6

Frequency Synthesiser Phase Noise and Power Level Design

6.1 Introduction

The first part of this chapter outlines the design of the frequency synthesiser for optimal phase noise performance. In order to compute the overall phase noise at the output of the synthesiser, various transfer functions need to be derived. This is the topic of the next section. In Section 6.3, the loop bandwidth for optimal synthesiser phase noise is calculated, in turn enabling the loop filter element values to be found. The derived transfer functions, together with the noise information of each component, are then used to calculate the overall phase noise at the output of the synthesiser. In the final section of the chapter, the estimated power levels at various stages of the synthesiser are shown.

6.2 Derivation of Transfer Functions

Figure 6.1 shows the linearised model of the PLL-based frequency synthesiser in Laplace notation. The noise sources of the various components are also shown in the figure. The synthesiser model is in many respects very similar to the PLL model discussed in Chapter 2.

The closed-loop transfer function relating $\phi_i(s)$ and $\phi_o(s)$, can be written as

$$H(s) = \frac{\phi_o(s)}{\phi_i(s)} = \frac{\text{Forward Gain}}{1 + \text{Loop Gain}} = \frac{\frac{K_\phi F(s) 2\pi K_{VCO}}{s}}{1 + \frac{K_\phi F(s) 2\pi K_{VCO}}{Ns}} = \frac{NK_\phi F(s) 2\pi K_{VCO}}{Ns + K_\phi F(s) 2\pi K_{VCO}} \quad (6.1)$$

where $K_\phi = \frac{1}{\pi}$ V/rad is the PFD gain factor, $F(s)$ is the transfer function of the loop filter, and $K_{VCO} \approx 300$ MHz/V is the tuning sensitivity of the HMC586LC4B VCO.

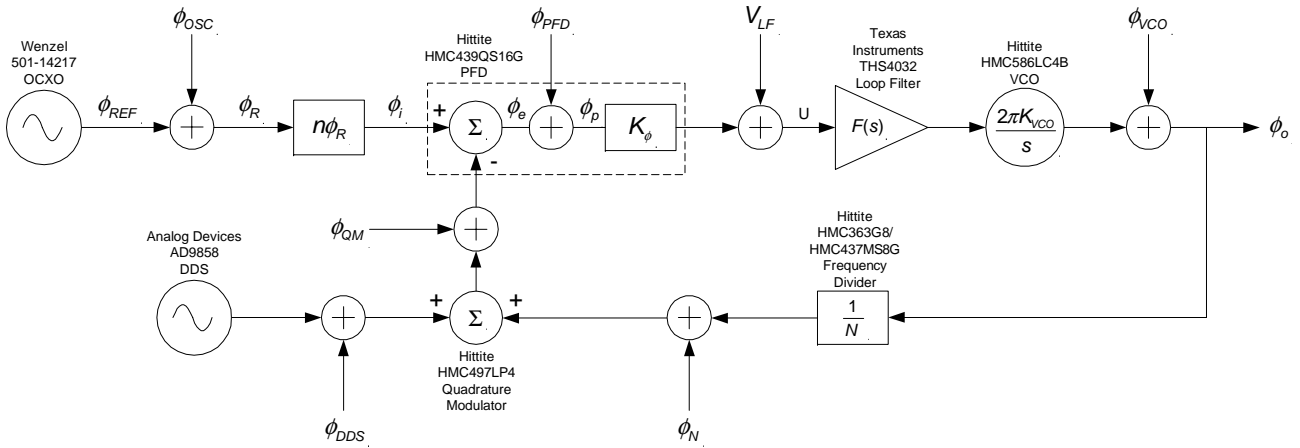


Figure 6.1: Linear model of the PLL-based frequency synthesiser in Laplace notation.

The transfer functions relating the PFD, frequency divider, loop filter and VCO noise to the output of the PLL, are exactly the same as that derived in Chapter 2. They are given by

$$H_{PFD}(s) = \frac{\phi_o(s)}{\phi_{PFD}(s)} = \frac{\frac{K_\phi F(s) 2\pi K_{VCO}}{s}}{1 + \frac{K_\phi F(s) 2\pi K_{VCO}}{Ns}} = \frac{NK_\phi F(s) 2\pi K_{VCO}}{Ns + K_\phi F(s) 2\pi K_{VCO}} \quad (6.2)$$

and

$$H_N(s) = \frac{\phi_o(s)}{\phi_N(s)} = \frac{-\frac{K_\phi F(s) 2\pi K_{VCO}}{s}}{1 + \frac{K_\phi F(s) 2\pi K_{VCO}}{Ns}} = \frac{-NK_\phi F(s) 2\pi K_{VCO}}{Ns + K_\phi F(s) 2\pi K_{VCO}} \quad (6.3)$$

and

$$H_{LF}(s) = \frac{\phi_o(s)}{V_{LF}(s)} = \frac{\frac{F(s) 2\pi K_{VCO}}{s}}{1 + \frac{K_\phi F(s) 2\pi K_{VCO}}{Ns}} = \frac{NF(s) 2\pi K_{VCO}}{Ns + K_\phi F(s) 2\pi K_{VCO}} \quad (6.4)$$

and

$$H_{VCO}(s) = \frac{\phi_o(s)}{\phi_{VCO}(s)} = \frac{1}{1 + \frac{K_\phi F(s) 2\pi K_{VCO}}{Ns}} \quad (6.5)$$

The transfer function relating the DDS noise to the output of the synthesiser, can be found by setting all other noise sources to zero. The output phase can be written as

$$\phi_o(s) = \frac{\phi_e(s) K_\phi F(s) 2\pi K_{VCO}}{s} \quad (6.6)$$

where

$$\phi_e(s) = - \left(\phi_{DDS}(s) + \frac{\phi_o(s)}{N} \right) \quad (6.7)$$

Substituting Equation 6.7 into Equation 6.6 and rearranging terms, yields

$$H_{DDS}(s) = \frac{\phi_o(s)}{\phi_{DDS}(s)} = \frac{-\frac{K_\phi F(s) 2\pi K_{VCO}}{s}}{1 + \frac{K_\phi F(s) 2\pi K_{VCO}}{Ns}} = \frac{-NK_\phi F(s) 2\pi K_{VCO}}{Ns + K_\phi F(s) 2\pi K_{VCO}} \quad (6.8)$$

In a similar fashion it can be shown that

$$H_{QM}(s) = \frac{\phi_o(s)}{\phi_{QM}(s)} = \frac{-\frac{K_\phi F(s)2\pi K_{VCO}}{s}}{1 + \frac{K_\phi F(s)2\pi K_{VCO}}{Ns}} = \frac{-NK_\phi F(s)2\pi K_{VCO}}{Ns + K_\phi F(s)2\pi K_{VCO}} \quad (6.9)$$

Note that $|H(s)| = |H_{PFD}(s)| = |H_N(s)| = |H_{DDS}(s)| = |H_{QM}(s)|$.

Figure 6.2 shows the loop filter circuit used in conjunction with the differential output of the PFD. The derivation of the loop filter transfer function follows next.

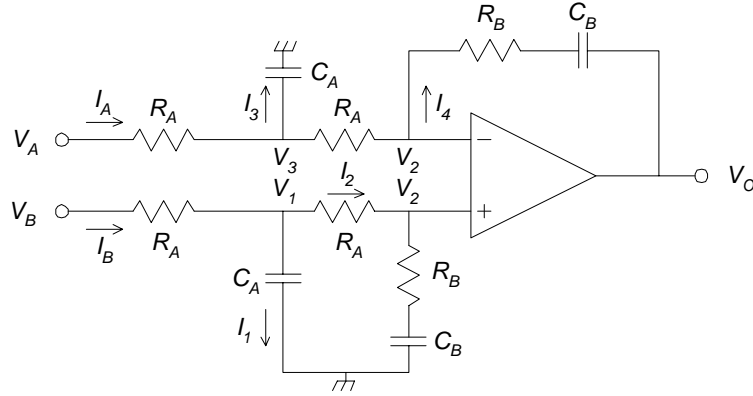


Figure 6.2: Active loop filter circuit.

The voltage at the noninverting input of the operational amplifier can be written as

$$V_2 = I_2 \left(R_B + \frac{1}{sC_B} \right) \quad (6.10)$$

Similarly

$$V_1 = I_2 \left(R_A + R_B + \frac{1}{sC_B} \right) \quad (6.11)$$

Eliminating I_2 yields

$$V_1 = \frac{V_2 (sC_B (R_A + R_B) + 1)}{sR_B C_B + 1} \quad (6.12)$$

The current I_B is equal to the sum of I_1 and I_2 , that is

$$I_B = I_1 + I_2 \quad (6.13)$$

Therefore

$$\begin{aligned} \frac{V_B - V_1}{R_A} &= V_1 sC_A + \frac{V_1}{R_A + R_B + \frac{1}{sC_B}} \\ \therefore V_B &= V_1 \left(1 + sR_A C_A + \frac{sR_A C_B}{sC_B (R_A + R_B) + 1} \right) \end{aligned} \quad (6.14)$$

Substituting Equation 6.12 into Equation 6.14 and rearranging terms, yields

$$V_2 = V_B \left(\frac{sR_B C_B + 1}{(sC_B (R_A + R_B) + 1) (sR_A C_A + 1) + sR_A C_B} \right) \quad (6.15)$$

Applying Kirchhoff's current law at node V_3 yields

$$\begin{aligned} I_A &= I_3 + I_4 \\ \therefore \frac{V_A - V_3}{R_A} &= V_3 sC_A + \frac{V_3 - V_o}{R_A + R_B + \frac{1}{sC_B}} \\ \therefore V_A &= V_3 \left(1 + sR_A C_A + \frac{sR_A C_B}{sC_B (R_A + R_B) + 1} \right) - \frac{V_o sR_A C_B}{sC_B (R_A + R_B) + 1} \end{aligned} \quad (6.16)$$

V_3 can be written as

$$\begin{aligned} V_3 &= V_2 + I_4 R_A \\ \therefore V_3 &= V_2 + \frac{(V_3 - V_o) R_A}{R_A + R_B + \frac{1}{sC_B}} \\ \therefore V_3 (sC_B (R_A + R_B) + 1) &= V_2 (sC_B (R_A + R_B) + 1) + sR_A C_B (V_3 - V_o) \\ \therefore V_3 (sR_B C_B + 1) &= V_2 (sC_B (R_A + R_B) + 1) - V_o sR_A C_B \\ \therefore V_3 &= \frac{V_2 (sC_B (R_A + R_B) + 1) - V_o sR_A C_B}{sR_B C_B + 1} \end{aligned} \quad (6.17)$$

Substituting Equation 6.17 into Equation 6.16 yields

$$\begin{aligned} V_A (sC_B (R_A + R_B) + 1) &= (V_2 (sC_B (R_A + R_B) + 1) - V_o sR_A C_B) \dots \\ &\times \left(\frac{(sC_B (R_A + R_B) + 1) (sR_A C_A + 1) + sR_A C_B}{sR_B C_B + 1} \right) - V_o sR_A C_B \end{aligned} \quad (6.18)$$

Substituting Equation 6.15 into Equation 6.18 yields

$$\begin{aligned} V_A (sC_B (R_A + R_B) + 1) &= V_B (sC_B (R_A + R_B) + 1) \dots \\ &- V_o sR_A C_B \left(\frac{(sC_B (R_A + R_B) + 1) (sR_A C_A + 1) + sR_A C_B}{sR_B C_B + 1} + 1 \right) \end{aligned} \quad (6.19)$$

Dividing Equation 6.19 by $sC_B (R_A + R_B) + 1$ and rearranging terms, yields

$$\begin{aligned} V_A &= V_B - V_o sR_A C_B \left(\frac{sR_A C_A + 2}{sR_B C_B + 1} \right) \\ \therefore F(s) &= \frac{V_o}{V_B - V_A} = \frac{sR_B C_B + 1}{s (2R_A C_B) \left(s \left(\frac{R_A C_A}{2} \right) + 1 \right)} \end{aligned} \quad (6.20)$$

The noise source V_{LF} is comprised of the thermal noise voltage generated by the resistors of the loop filter and the noise from the operational amplifier. The noise arising from the operational amplifier can be modelled by a combination of a voltage source v_n and a current source i_n at the input, as

shown in Figure 6.3. Usually it is assumed that v_n and i_n are uncorrelated. The values of current and voltage noise versus frequency are normally given by the manufacturer [15, 16].

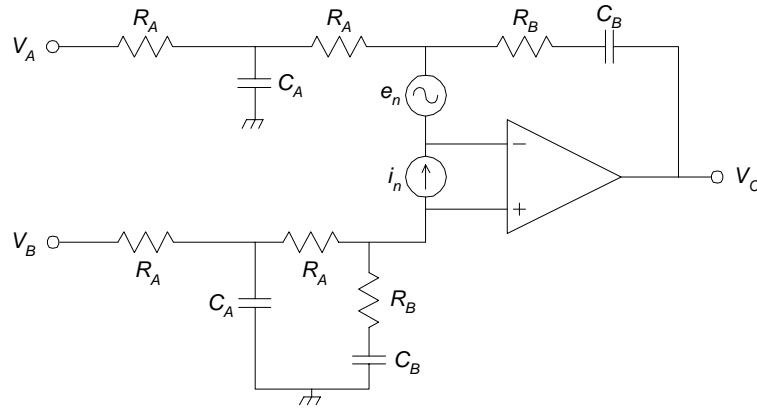


Figure 6.3: Equivalent operational amplifier noise circuit.

The transfer function relating the noise voltage to the output of the operational amplifier, can be found by setting V_A and V_B to zero. The equivalent circuit is shown in Figure 6.4.

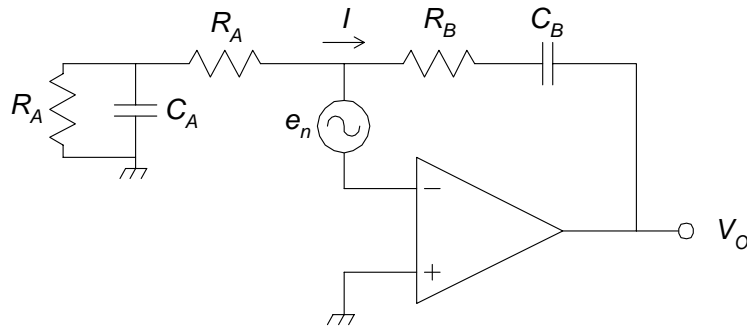


Figure 6.4: Equivalent noise voltage circuit.

Applying Kirhhoff's voltage law yields

$$e_n = -I \left(\frac{R_A}{1 + sR_A C_A} + R_A \right) \tag{6.21}$$

The current can be expressed as

$$I = \frac{e_n - V_o}{R_B + \frac{1}{sC_B}} = \frac{sC_B (e_n - V_o)}{sR_B C_B + 1} \tag{6.22}$$

Substituting Equation 6.22 into Equation 6.21 yields

$$e_n = \frac{-sC_B (e_n - V_o)}{sR_B C_B + 1} \left(\frac{R_A}{sR_A C_A + 1} + R_A \right) \tag{6.23}$$

Rearranging terms yields

$$\frac{sC_B V_o}{sR_B C_B + 1} \left(\frac{R_A}{sR_A C_A + 1} + R_A \right) = e_n \left(1 + \frac{sC_B}{sR_B C_B + 1} \left(\frac{R_A}{sR_A C_A + 1} + R_A \right) \right) \quad (6.24)$$

Further simplification yields

$$\begin{aligned} \frac{V_o}{e_n} &= \frac{\left(\frac{sR_B C_B + 1}{sR_A C_B} + \frac{1}{sR_A C_A + 1} + 1 \right)}{\frac{1}{sR_A C_A + 1} + 1} \\ \therefore \frac{V_o}{e_n} &= \frac{(sR_B C_B + 1)(sR_A C_A + 1) + sR_A C_B (sR_A C_A + 1) + sR_A C_B}{sR_A C_B (sR_A C_A + 1) + sR_A C_B} \\ \therefore F_e(s) &= \frac{V_o}{e_n} = \frac{s^2 R_A C_A C_B (R_A + R_B) + s(R_A C_A + C_B (2R_A + R_B)) + 1}{s^2 R_A C_B \left(s \left(\frac{R_A C_A}{2} \right) + 1 \right)} \end{aligned} \quad (6.25)$$

The voltage noise contribution of the operational amplifier to the overall phase noise of the synthesiser is accounted for by substituting $F_e(s)$ for $F(s)$ in the forward gain path of the transfer function of Equation 6.4, that is

$$H_e(s) = \frac{\phi_o(s)}{V_{LF}(s)} = \frac{\frac{F_e(s)2\pi K_{VCO}}{s}}{1 + \frac{K_\phi F(s)2\pi K_{VCO}}{Ns}} = \frac{NF_e(s)2\pi K_{VCO}}{Ns + K_\phi F(s)2\pi K_{VCO}} \quad (6.26)$$

The equivalent circuit modelling the current and resistor noise, is depicted in Figure 6.5.

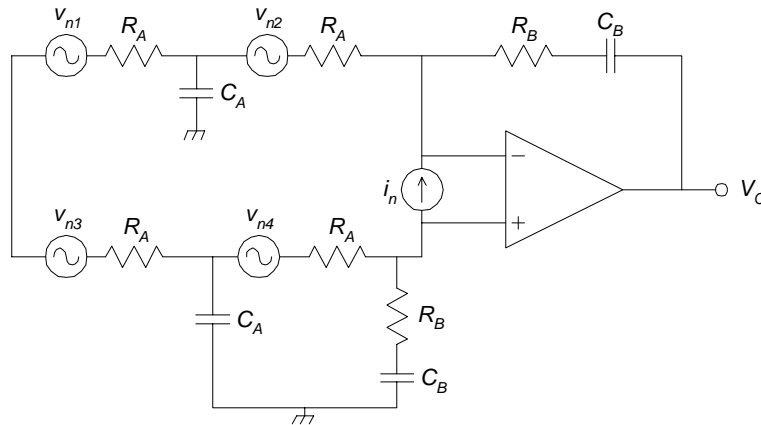


Figure 6.5: Equivalent circuit for modelling the current and resistor noise.

In the next section, it is shown that the value of R_B is small in comparison to R_A . Therefore, R_A is the dominant source of thermal noise and R_B is not taken into account in the noise analysis. Capacitors are reactive devices and generate very little noise. For this reason they are not considered in the noise analysis either. The thermal noise of the resistors and the current noise of the operational amplifier, are scaled to the output of the synthesiser using Equation 6.4.

6.3 PLL Loop Bandwidth and Loop Filter Component Values

Now that the various transfer functions relating the noise sources to the output of the synthesiser have been derived, the loop bandwidth for optimal phase noise performance can be computed. In Chapter 2 it was shown that, for optimal PLL phase noise performance, the loop bandwidth should be chosen equal to the frequency point where the VCO phase noise intersects with the total phase noise of the in-band phase noise contributors.

Table 6.1 shows the *Excel* spreadsheet used for determining the optimal PLL loop bandwidth. The calculations are performed for a synthesiser output frequency of 5.47 GHz and a PLL frequency divider value of $N = 8$. In Section 6.4, the overall phase noise of the synthesiser at both the lowest and highest output frequencies are computed.

Table 6.1: Spreadsheet to determine the loop bandwidth for optimal synthesiser phase noise performance.

Element	Comment	Units	Frequency	Frequency Offset					
			MHz	100 Hz	1 kHz	10 kHz	100 kHz	1 MHz	10 MHz
Wenzel OCOXO (501-14217)	Phase Noise	dBc/Hz	100	-120.00	-145.00	-160.00	-160.00	-160.00	-160.00
	Phase Noise at Output of PLL	dBc/Hz	5470	-85.24	-110.24	-125.24	-125.24	-125.24	-125.24
	Phase Noise at Input of PFD	dBc/Hz	683.75	-103.30	-128.30	-143.30	-143.30	-143.30	-143.30
AD9858 DDS	Phase Noise	dBc/Hz	103	-139.00	-148.00	-152.00	-152.00	-152.00	-150.00
	Phase Noise	dBc/Hz	403	-123.00	-132.00	-137.00	-140.00	-140.00	-139.00
	Interpolated Phase Noise	dBc/Hz	316.25	-125.84	-134.84	-139.67	-142.13	-142.13	-140.95
HMC497LP4 Quadrature Modulator	Noise Floor Relative To -5dBm Output	dBc/Hz		-156.00	-156.00	-156.00	-156.00	-156.00	-156.00
HMC363G8 Frequency Divider (/8)	Phase Noise	dBc/Hz		-133.00	-143.00	-150.00	-152.00	-153.00	-153.00
HMC439QS16G PFD	Phase Noise	dBc/Hz	100	-144.00	-153.00	-153.00	-153.00	-151.00	-150.00
	Phase Noise	dBc/Hz	1280	-129.00	-140.00	-143.00	-143.00	-139.00	-141.00
	Interpolated Phase Noise	dBc/Hz	1000	-130.45	-141.26	-143.97	-143.97	-140.16	-141.87
	Total Phase Noise at PFD Input H(s)	dBc/Hz dB		-103.26 18.06	-127.14 18.06	-136.83 18.06	-138.04 18.06	-136.74 18.06	-137.00 18.06
Phase Noise at Output of PLL			dBc/Hz	-85.20	-109.07	-118.77	-119.98	-118.68	-118.94
Loop Filter Resistor Noise (4xR _n)	4kTR	V ² /Hz		1.28E-17	1.28E-17	1.28E-17	1.28E-17	1.28E-17	1.28E-17
	H _{Lr} (s) , Factor Kphi Smaller Than H(s)	dB		28.01	28.01	28.01	28.01	28.01	28.01
	Phase Noise at Output of PLL	rad ² /Hz		8.09E-15	8.09E-15	8.09E-15	8.09E-15	8.09E-15	8.09E-15
Phase Noise at Output of PLL			dBc/Hz	-143.93	-143.93	-143.93	-143.93	-143.93	-143.93
THS4032 Operational Amplifier	Current Noise Density	pA/sqrt(Hz)		3.60	1.60	1.25	1.20	1.20	1.20
	Equivalent Thevenin Voltage Noise Density	nV/sqrt(Hz)		2.88	1.28	1.00	0.96	0.96	0.96
	H _{Lr} (s) , Factor Kphi Smaller Than H(s)	dB		28.01	28.01	28.01	28.01	28.01	28.01
	Phase Noise at Output of PLL	rad ² /Hz		5.24E-15	1.03E-15	6.32E-16	5.82E-16	5.82E-16	5.82E-16
Phase Noise at Output of PLL			dBc/Hz	-145.82	-152.86	-155.01	-155.36	-155.36	-155.36
Total LPF Phase Noise at Output of PLL			dBc/Hz	-85.20	-109.07	-118.76	-119.96	-118.66	-118.92
HMC586LC4B VCO	VCO Phase Noise	dBc/Hz		-9.00	-43.00	-74.00	-97.00	-118.00	-139.00

The phase noise values of the various components shown in the spreadsheet are taken directly from the datasheets. The values highlighted in grey are estimated values not given by the manufacturer. In each case, sensible values have been assumed. In the case of the *Wenzel* oscillator for example, the phase noise reaches the noise floor of -160 dBc/Hz at 10 kHz offset from the carrier. When the noise floor is reached, the phase noise curve for higher offset frequencies is flat. This is evident from the phase noise specified at 100 kHz, which is also equal to -160 dBc/Hz. For this reason, it is fair to take the phase noise at 1 MHz and 10 MHz offset as -160 dBc/Hz.

The spreadsheet shows that the phase noise contribution arising from the current noise of the operational amplifier is insignificant compared to other sources of phase noise. The estimated current noise values at 1 MHz and 10 MHz offset therefore do not have any significant influence in determining the loop bandwidth. An approximation of the phase noise of the VCO at 10 MHz offset was found by extrapolation of the VCO phase noise curve.

The frequency of the *Wenzel* oscillator is multiplied by the frequency multipliers, internally divided by the DDS, summed in the quadrature modulator and further multiplied to the output of the synthesiser. Since all these operations are linear on the phase, and since the phase noise of the oscillator at these various mathematical operators is perfectly correlated, the output phase is as if it is obtained by straight multiplication by the ratio of output to reference frequencies [5]. For an output frequency of 5.47 GHz, the net frequency multiplication factor is equal to

$$N_{net} = \frac{f_o}{f_{REF}} = \frac{5.47 \times 10^9}{100 \times 10^6} = 54.7 \quad (6.27)$$

The spreadsheet shows the phase noise of the reference oscillator for an output frequency of 5.47 GHz. The phase noise of the oscillator referenced to the input of the PLL is $20 \log_{10}(N)$ lower compared to the phase noise at the output, where N is the value of the frequency divider in the feedback path of the PLL.

The residual phase noise of the DDS is given at 103 MHz and 403 MHz. For an output frequency of 5.47 GHz, the DDS frequency is equal to 316.25 MHz. To find the phase noise of the DDS at 316.25 MHz, interpolation is required. Equation 3.1 shows that the DDS is essentially a frequency multiplier, as it multiplies the DDS system clock frequency by the ratio $\frac{FTW}{2^{32}}$. Thus, for ideal frequency multiplication, the phase noise from 103 MHz to 403 MHz is expected to increase by $20 \log_{10}\left(\frac{403}{103}\right) = 11.85$ dB. In reality, the DDS phase noise scales somewhat differently. If a phase noise scaling formula of $\eta \log_{10}\left(\frac{f_2}{f_1}\right)$ is assumed (η is a constant), the data from the manufacturer indicates that the phase noise from 103 MHz to 403 MHz at 100 Hz and 1 kHz offset increases by 16 dB, corresponding to $\eta = 27$. At 1 MHz and 10 MHz frequency offset, $\eta = 20.25$ and $\eta = 18.57$, respectively. The interpolated phase noise at 316.25 MHz is shown in the spreadsheet. The same approach is used to find the interpolated phase noise of the PFD at 1 GHz.

For use in the synthesiser, the quadrature modulator is operated such that the output power of the 1 GHz upper sideband (USB) is in the order of -5 dBm. The noise floor of the modulator is specified as -161 dBm/Hz. Thus, relative to -5 dBm, the noise floor is -156 dBc/Hz.

Recall from Chapter 2 that the spectral density at the output of a linear time-invariant system is related to the spectral density at the input by

$$S_o(f) = |H(f)|^2 S_i(f) \quad (6.28)$$

where $H(f)$ is the transfer function of the system.

The DDS, quadrature modulator, frequency divider, PFD and reference oscillator phase noise specified at the input of the PLL scale to the output of the synthesiser by the magnitude-squared of the closed-loop transfer function of the PLL. From Equation 6.1, the magnitude of the closed-loop transfer function is given by

$$|H(s)| = \left| \frac{\frac{K_\phi F(s) 2\pi K_{VCO}}{s}}{1 + \frac{K_\phi F(s) 2\pi K_{VCO}}{Ns}} \right| \quad (6.29)$$

The loop filter transfer function derived in the previous section is of lowpass form and contains a pole at the origin. Thus, at low frequencies, $\frac{K_\phi F(s) 2\pi K_{VCO}}{Ns} \gg 1$. Therefore, for frequencies much lower than the cutoff frequency of the loop, the magnitude of the closed-loop transfer function reduces to

$$|H(s)| = \left| \frac{\frac{K_\phi F(s) 2\pi K_{VCO}}{s}}{1 + \frac{K_\phi F(s) 2\pi K_{VCO}}{Ns}} \right| \approx \left| \frac{\frac{K_\phi F(s) 2\pi K_{VCO}}{s}}{\frac{K_\phi F(s) 2\pi K_{VCO}}{Ns}} \right| = |N| \quad (\omega \ll \omega_c) \quad (6.30)$$

where ω_c is the cutoff frequency of the loop. The magnitude of the closed-loop transfer function in dB, and the total phase noise of the reference oscillator, DDS, quadrature modulator, frequency divider and PFD at the output of the PLL, are shown in the spreadsheet.

The datasheet of the PFD specifies that, to obtain a PFD gain factor of $K_\phi = \frac{1}{\pi}$ V/rad, R_A is required to be 200 Ω . From Chapter 2, the thermal noise generated by R_A , expressed in RMS voltage-squared per unit of bandwidth, is equal to

$$S(f) = \frac{V_n^2}{B} = 4kTR \quad \left[\frac{\text{V}^2}{\text{Hz}} \right] \quad (6.31)$$

The voltage noise density is scaled to the output of the PLL using the transfer function given by Equation 6.4, resulting in units of rad^2/Hz . The peak phase deviation is converted to dBc/Hz using Equation 2.19. The operational amplifier current noise is transformed into an equivalent Thevenin voltage source and scaled to the output of the PLL in a similar fashion. The transfer function $|H_e(s)|$ required to scale the voltage noise density of the operational amplifier to the output of the PLL, depends on the unknown values C_A , C_B and R_B . For this reason, its noise contribution is neglected in the calculations for determining the loop bandwidth.

All the different noise sources of the synthesiser are uncorrelated. Therefore, the total lowpass filtered phase noise at the output of the PLL is found by adding all the individual phase noise spectral densities. Figure 6.6 shows a graphical representation of the total lowpass filtered phase noise and the free-running VCO phase noise plotted on the same graph. The phase noise values are taken from the spreadsheet.

The two curves meet at an offset frequency of 1 MHz. Choosing the loop bandwidth of the PLL equal to 1 MHz results in optimal frequency synthesiser phase noise performance. Inside the loop bandwidth, the PLL suppresses VCO phase noise and passes all other sources of phase noise. Outside the loop bandwidth, the VCO phase noise is passed while all other sources of phase noise are suppressed by the frequency response of the PLL.

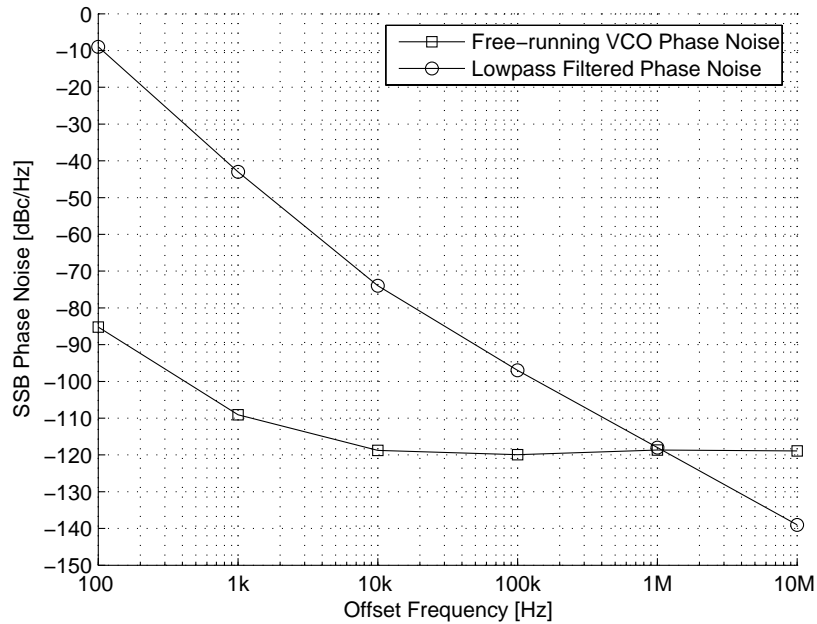


Figure 6.6: Graphical representation for determining the loop bandwidth for minimal phase noise.

6.3.1 Loop Filter Component Values

The transfer function of the loop filter can be expressed as

$$F(s) = \frac{sR_B C_B + 1}{s(2R_A C_B) \left(s \left(\frac{R_A C_A}{2} \right) + 1 \right)} = \frac{R_B \left(s + \frac{1}{R_B C_B} \right)}{s R_A^2 C_A \left(s + \frac{2}{R_A C_A} \right)} \tag{6.32}$$

which is of the form

$$F(j\omega) = \frac{K(j\omega + z)}{j\omega(j\omega + p)} \tag{6.33}$$

The phase of the transfer function can be written as

$$\phi = \angle F(j\omega) = \tan^{-1} \left(\frac{\omega}{z} \right) - \tan^{-1} \left(\frac{\omega}{p} \right) - \frac{\pi}{2} \tag{6.34}$$

The derivative of the phase with respect to frequency is equal to

$$\frac{d\phi}{d\omega} = \frac{1/z}{1 + (\omega/z)^2} - \frac{1/p}{1 + (\omega/p)^2} \tag{6.35}$$

Setting $\frac{d\phi}{d\omega} = 0$, and solving for ω yields

$$\omega = \frac{z - p}{\frac{1}{p} - \frac{1}{z}} = \sqrt{zp} \tag{6.36}$$

Equation 6.36 shows that the frequency point of the maximum phase is equal to the geometric mean of the zero and pole. The maximum phase at this point can be found by substituting Equation 6.36 into Equation 6.34

$$\phi_{max} = \tan^{-1} \left(\sqrt{\frac{p}{z}} \right) - \tan^{-1} \left(\sqrt{\frac{z}{p}} \right) - \frac{\pi}{2} \quad (6.37)$$

Let the pole-to-zero ratio be given by c , so that $p = cz$. The maximum phase, expressed in terms of c , is equal to

$$\phi_{max} = \tan^{-1} (\sqrt{c}) - \tan^{-1} \left(\frac{1}{\sqrt{c}} \right) - \frac{\pi}{2} \quad (6.38)$$

It is evident from Equation 6.38 that the pole-to-zero ratio c determines the maximum phase of the loop filter. The aim of the loop filter design is to obtain an adequate loop phase margin, ensuring good system stability and a low resonant peak in the vicinity of the cutoff frequency of the loop. The open loop transfer function of the PLL can be expressed as

$$L(s) = \frac{K_\phi 2\pi K_{VCO} F(s)}{Ns} = \left(\frac{K_\phi 2\pi K_{VCO}}{Ns} \right) \left(\frac{sR_B C_B + 1}{s(2R_A C_B) \left(s \left(\frac{R_A C_A}{2} \right) + 1 \right)} \right) \quad (6.39)$$

Note that the phase of $L(s)$, and hence the phase margin of the loop, is effectively controlled by the phase of the loop filter. The two integrators in the denominator of the open loop transfer function each account for -90° of phase, resulting in a total of -180° . The combination of the zero and the pole of the loop filter has the desired effect of maximising the phase at the selected frequency point.

Choosing $c = 30$ yields a maximum loop filter phase of

$$\phi = \tan^{-1} (\sqrt{30}) - \tan^{-1} \left(\frac{1}{\sqrt{30}} \right) - \frac{\pi}{2} = -20.69^\circ \quad (6.40)$$

The choice of c will become clear shortly. To maximise the phase margin of the PLL, the maximum phase of the loop filter should be set to the frequency point where $L(s)$ crosses the 0 dB axis. If this is the case, the phase margin of the loop is equal to

$$\text{Phase Margin} = 180^\circ + \angle L(j\omega_c) = 180^\circ + (-90^\circ - 20.69^\circ) = 69.31^\circ \quad (6.41)$$

From Equation 6.32 and Equation 6.33, the pole is related to R_A and C_A by

$$\begin{aligned} p &= \frac{2}{R_A C_A} \\ \therefore C_A &= \frac{2}{p R_A} \end{aligned} \quad (6.42)$$

The maximum phase of the loop filter should occur at 1 MHz, the intended loop bandwidth of the

PLL. From Equation 6.36

$$\begin{aligned}\omega &= \sqrt{zp} = \sqrt{cz^2} \\ \therefore z &= \frac{\omega}{\sqrt{c}} = \frac{2\pi f}{\sqrt{c}} = \frac{2\pi (1 \times 10^6)}{\sqrt{30}} = 1.147 \times 10^6\end{aligned}\quad (6.43)$$

Therefore

$$p = cz = 30 (1.147 \times 10^6) = 34.414 \times 10^6 \quad (6.44)$$

Substituting Equation 6.44 into Equation 6.42, yields

$$C_A = \frac{2}{pR_A} = \frac{2}{34.414 \times 10^6 (200)} = 290.57 \text{ pF} \quad (6.45)$$

The value of R_B can be found by setting $|L(j2\pi \times 10^6)| = 1$, that is

$$|L(j\omega_c)| = \frac{K_\phi 2\pi K_{VCO} R_B \sqrt{\omega_c^2 + z^2}}{N\omega_c^2 R_A^2 C_A \sqrt{\omega_c^2 + p^2}} = 1 \quad (6.46)$$

Solving for R_B , with $\omega_c = 2\pi(1 \times 10^6)$, yields

$$R_B = \frac{N\omega_c^2 R_A^2 C_A \sqrt{\omega_c^2 + p^2}}{K_\phi 2\pi K_{VCO} \sqrt{\omega_c^2 + z^2}} = 33.51 \ \Omega \quad (6.47)$$

Note that R_B is much smaller compared to R_A . With the help of Equation 6.32 and Equation 6.33, C_B is found to be

$$C_B = \frac{1}{R_B z} = \frac{1}{33.51 (1.147 \times 10^6)} = 26 \text{ nF} \quad (6.48)$$

The frequency response of the loop filter is depicted in Figure 6.7. Note that the phase of the loop filter peaks at 1 MHz, where it is equal to -20.69° as expected. The integrator in the transfer function of the loop filter accounts for a constant -90° of phase lag in the phase response. The combination of the zero and the pole causes the phase to increase and decrease around 1 MHz. The integrator in the loop filter transfer function also causes the 20 dB/decade rolloff in amplitude observed at low frequencies.

Figure 6.8 shows the Bode diagram of the open loop transfer function. Note that $L(s)$ is a monotonically decreasing function, and that $|L(s)| \gg 1$ for frequencies much lower than the crossover frequency. The phase margin is indicated in the figure and is equal to 69.31° as expected.

Figure 6.9 shows the effect of the phase margin on the closed-loop response of the PLL. Note that the resonant peak in the vicinity of the loop bandwidth increases as the phase margin decreases. This is in line with what was discussed in Chapter 2. In cases where low phase noise is very important, this characteristic is undesired, since peaking in the closed-loop response results in peaking to be observed in the output phase noise of the PLL. A phase margin of 69.31° was found to be adequate, yielding a moderate resonant peak and practical loop filter element values.

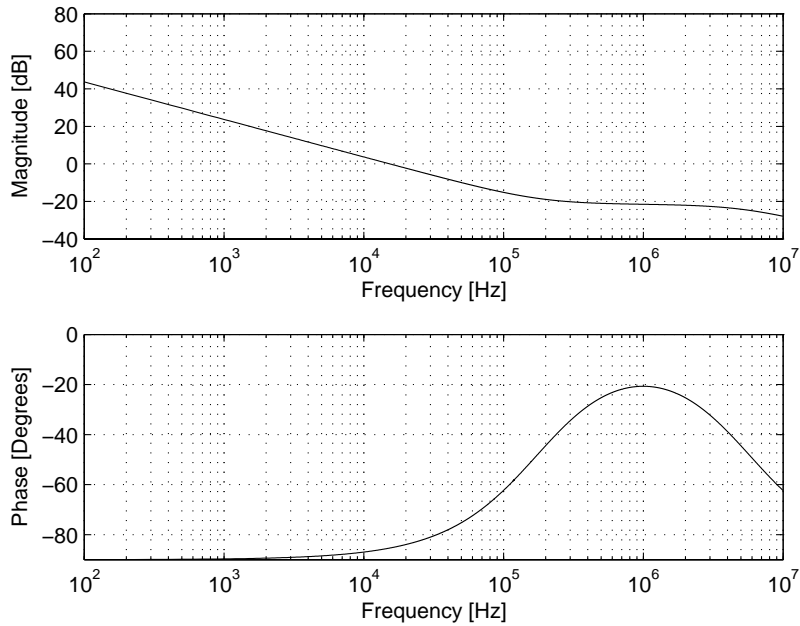


Figure 6.7: Loop filter Bode diagram.

Figure 6.9 also shows that the 3 dB bandwidth is slightly different from the designed cutoff frequency. The actual 3 dB loop bandwidth for a phase margin of 69.31° , is approximately equal to 1.4 MHz. Note that the 3 dB closed-loop bandwidth approaches the designed loop bandwidth (crossover frequency) of 1 MHz for the case where the phase margin approaches 90° .

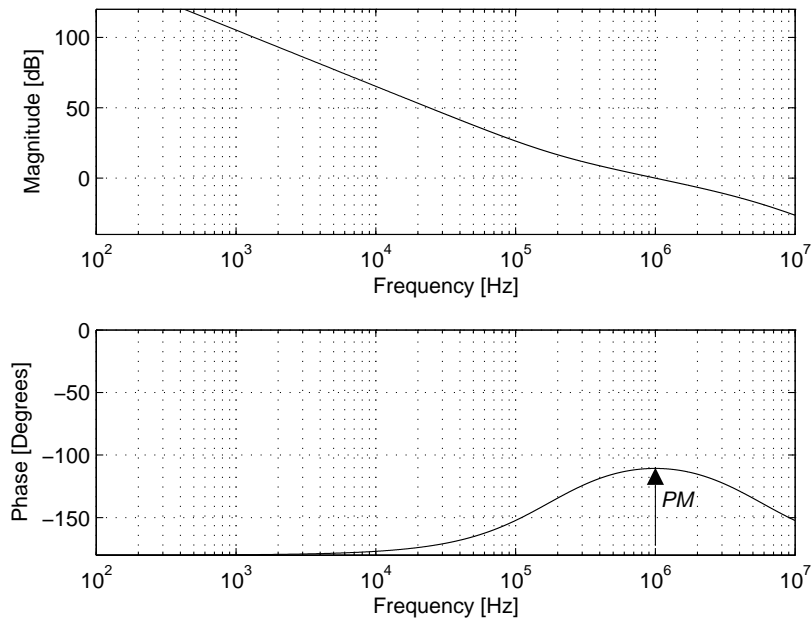


Figure 6.8: Open loop frequency response.

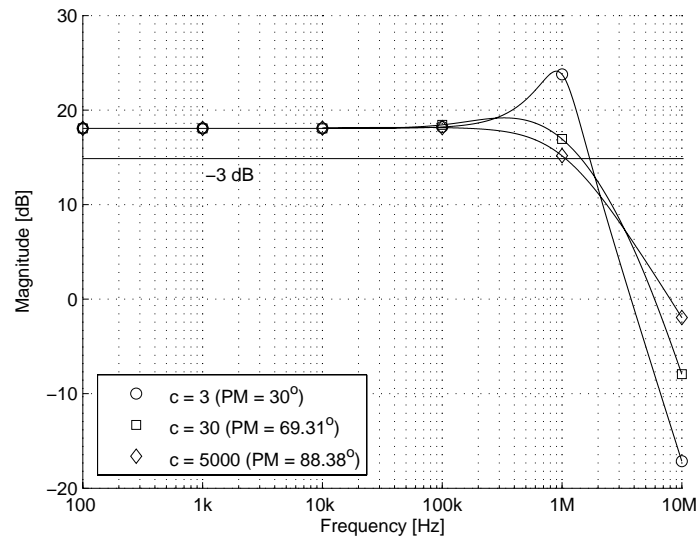


Figure 6.9: The effect of various phase margins on the closed-loop response of the PLL.

6.4 Overall Synthesiser Phase Noise

In this section, the overall phase noise of the synthesiser is calculated. Figure 6.10 shows a magnitude plot of the various transfer functions derived in Section 6.1. Note the lowpass and highpass frequency response of $|H(s)|$ and $|H_{VCO}(s)|$, respectively. The numerical magnitude values of the transfer functions at various frequencies, are given in Table 6.2. These are the values required for the phase noise calculations. Other parameters required for the phase noise calculations are given in Table 6.3. Practical loop filter component values closest to that calculated in the previous section were used. The PFD gain factor and VCO tuning sensitivity are taken from the datasheets.

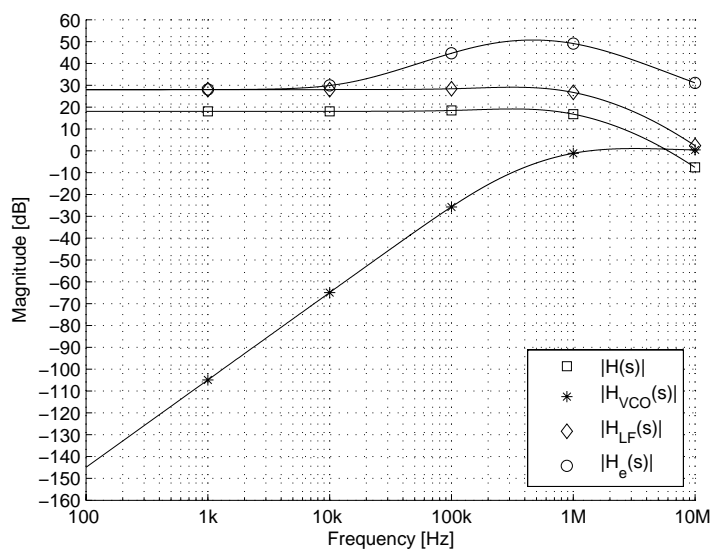


Figure 6.10: Magnitude plot of the various transfer functions derived in Section 6.1.

Table 6.2: Magnitude values of various transfer functions required for calculating the synthesiser phase noise.

Frequency [Hz]	100	1k	10k	100k	1M	10M
$ H(s) $ [dB]	18.06	18.06	18.07	18.45	16.78	-7.57
$ H_{LF}(s) $ [dB]	28.01	28.01	28.01	28.39	26.72	2.37
$ H_e(s) $ [dB]	28.01	28.03	29.88	44.63	49.11	31.1
$ H_{VCO}(s) $ [dB]	-144.91	-104.91	-64.91	-25.7	-1.16	0.38

Table 6.3: Parameter values used in the phase noise calculations.

Parameter	Value
K_ϕ	$\frac{1}{\pi}$ V/rad
K_{VCO}	300 MHz/V
R_A	200 Ω
C_A	270 pF
R_B	33 Ω
C_B	27 nF

Table 6.4 and Table 6.5 show the *Excel* spreadsheets for determining the overall phase noise at the output of the synthesiser at the lowest and highest output frequencies, respectively. The calculations follow the same outline as discussed previously. The *Excel* spreadsheets for determining the synthesiser phase noise with $N = 9$, are given in Appendix A.

Table 6.4: Spreadsheet for calculating the synthesiser phase noise at 5.47 GHz.

Element	Comment	Units	Frequency MHz	Frequency Offset							
				100 Hz	1 kHz	10 kHz	100 kHz	1 MHz	10 MHz		
Wenzel OCXO (501-14217)	Phase Noise	dBc/Hz	100	-120.00	-145.00	-160.00	-160.00	-160.00	-160.00		
	Phase Noise at Output of PLL	dBc/Hz	5470	-85.24	-110.24	-125.24	-125.24	-125.24	-125.24		
	Phase Noise at Input of PFD	dBc/Hz	683.75	-103.30	-128.30	-143.30	-143.30	-143.30	-143.30		
AD9858 DDS	Phase Noise	dBc/Hz	103	-139.00	-148.00	-152.00	-152.00	-152.00	-150.00		
	Phase Noise	dBc/Hz	403	-123.00	-132.00	-137.00	-140.00	-140.00	-139.00		
	Interpolated Phase Noise	dBc/Hz	316.25	-125.84	-134.84	-139.87	-142.13	-142.13	-140.95		
HMC497LP4 Quadrature Modulator	Noise Floor Relative To -5dBm Output	dBc/Hz		-156.00	-156.00	-156.00	-156.00	-156.00	-156.00		
HMC363G8 Frequency Divider (/8)	Phase Noise	dBc/Hz		-133.00	-143.00	-150.00	-152.00	-153.00	-153.00		
HMC439QS16G PFD	Phase Noise	dBc/Hz	100	-144.00	-153.00	-153.00	-153.00	-151.00	-150.00		
	Phase Noise	dBc/Hz	1280	-129.00	-140.00	-143.00	-143.00	-139.00	-141.00		
	Interpolated Phase Noise	dBc/Hz	1000	-130.45	-141.26	-143.97	-143.97	-140.16	-141.87		
	Total Phase Noise at PFD Input $ H(s) $	dBc/Hz dB		-103.26 18.06	-127.14 18.06	-136.83 18.07	-138.04 18.45	-136.74 16.78	-137.00 -7.57		
Phase Noise at Output of PLL				dBc/Hz		-85.20	-109.07	-118.76	-119.59	-119.96	-144.57
Loop Filter Resistor Noise ($4xR_A$)	$4kTR$	V^2/Hz		1.28E-17	1.28E-17	1.28E-17	1.28E-17	1.28E-17	1.28E-17		
	$ H_{LF}(s) $, Factor Kphi Smaller Than $ H(s) $	dB		28.01	28.01	28.01	28.39	26.72	2.37		
	Phase Noise at Output of PLL	rad^2/Hz		8.09E-15	8.09E-15	8.11E-15	8.85E-15	6.02E-15	2.21E-17		
Phase Noise at Output of PLL				dBc/Hz		-143.93	-143.93	-143.92	-143.54	-145.21	-169.56
THS4032 Operational Amplifier	Current Noise Density	pA/sqrt(Hz)		3.60	1.60	1.25	1.20	1.20	1.20		
	Equivalent Thevenin Voltage Noise Density $ H_{LF}(s) $, Factor Kphi Smaller Than $ H(s) $	nV/sqrt(Hz) dB		2.88 28.01	1.28 28.01	1.00 28.01	0.96 28.39	0.96 26.72	0.96 2.37		
	Voltage Noise Density $ H_e(s) $	nV/sqrt(Hz) dB		3.62 28.01	1.90 28.03	1.50 29.88	1.40 44.63	1.35 49.11	1.35 31.10		
	Phase Noise at Output of PLL	rad^2/Hz		1.35E-14	1.03E-15	6.33E-16	6.37E-16	4.33E-16	1.59E-18		
	Phase Noise at Output of PLL				dBc/Hz		-141.70	-152.86	-155.00	-154.97	-156.64
HMC586LC4B VCO	Phase Noise	dBc/Hz		-9.00	-43.00	-74.00	-97.00	-118.00	-139.00		
	$ H_{VCO}(s) $	dB		-144.91	-104.91	-64.91	-25.70	-1.16	0.38		
Phase Noise at Output of PLL				dBc/Hz		-153.91	-147.91	-138.91	-122.70	-119.16	-138.62
Total Phase Noise at Output of PLL				dBc/Hz	5470	-85.20	-109.07	-118.71	-117.85	-116.53	-137.63

Table 6.5: Spreadsheet for calculating the synthesiser phase noise at 7.47 GHz.

Element	Comment	Units	Frequency MHz	Frequency Offset							
				100 Hz	1 kHz	10 kHz	100 kHz	1 MHz	10 MHz		
Wenzel OCXO (501-14217)	Phase Noise	dBc/Hz	100	-120.00	-145.00	-160.00	-160.00	-160.00	-160.00		
	Phase Noise at Output of PLL	dBc/Hz	7470	-82.53	-107.53	-122.53	-122.53	-122.53	-122.53		
	Phase Noise at Input of PFD	dBc/Hz	933.75	-100.60	-125.60	-140.60	-140.60	-140.60	-140.60		
AD9858 DDS	Phase Noise	dBc/Hz	103	-139.00	-148.00	-152.00	-152.00	-152.00	-150.00		
	Phase Noise	dBc/Hz	403	-123.00	-132.00	-137.00	-140.00	-140.00	-139.00		
	Interpolated Phase Noise	dBc/Hz	66.25	-144.18	-153.18	-156.85	-155.88	-155.88	-153.56		
HMC497LP4 Quadrature Modulator	Noise Floor Relative To -5dBm Output	dBc/Hz		-156.00	-156.00	-156.00	-156.00	-156.00	-156.00		
HMC363G8 Frequency Divider (/8)	Phase Noise	dBc/Hz		-133.00	-143.00	-150.00	-152.00	-153.00	-153.00		
HMC439QS16G PFD	Phase Noise	dBc/Hz	100	-144.00	-153.00	-153.00	-153.00	-151.00	-150.00		
	Phase Noise	dBc/Hz	1280	-129.00	-140.00	-143.00	-143.00	-139.00	-139.00		
	Interpolated Phase Noise	dBc/Hz	1000	-130.45	-141.26	-143.97	-143.97	-140.16	-141.87		
	Total Phase Noise at PFD Input H(s)	dBc/Hz dB		-100.59 18.06	-125.39 18.06	-138.48 18.07	-138.58 18.45	-137.13 16.78	-137.85 -7.57		
Phase Noise at Output of PLL				dBc/Hz		-82.53	-107.33	-120.41	-120.13	-120.35	-145.42
Loop Filter Resistor Noise (4xR _L)	4kTR	V ² /Hz		1.28E-17	1.28E-17	1.28E-17	1.28E-17	1.28E-17	1.28E-17		
	H _L (s) , Factor Kphi Smaller Than H(s)	dB		28.01	28.01	28.01	28.39	26.72	2.37		
	Phase Noise at Output of PLL	rad ² /Hz		8.09E-15	8.09E-15	8.11E-15	8.85E-15	6.02E-15	2.21E-17		
Phase Noise at Output of PLL				dBc/Hz		-143.93	-143.93	-143.92	-143.54	-145.21	-169.56
THS4032 Operational Amplifier	Current Noise Density	pA/sqrt(Hz)		3.60	1.60	1.25	1.20	1.20	1.20		
	Equivalent Thevenin Voltage Noise Density	nV/sqrt(Hz)		2.88	1.28	1.00	0.96	0.96	0.96		
	H _L (s) , Factor Kphi Smaller Than H(s)	dB		28.01	28.01	28.01	28.39	26.72	2.37		
	Voltage Noise Density	nV/sqrt(Hz)		3.62	1.90	1.50	1.40	1.35	1.35		
	H _a (s)	dB		28.01	28.03	29.88	44.63	49.11	31.10		
	Phase Noise at Output of PLL	rad ² /Hz		1.35E-14	1.03E-15	6.33E-16	6.37E-16	4.33E-16	1.59E-18		
Phase Noise at Output of PLL				dBc/Hz		-141.70	-152.86	-155.00	-154.97	-156.64	-180.99
HMC586LC4B VCO	Phase Noise	dBc/Hz		-9.00	-43.00	-74.00	-97.00	-118.00	-139.00		
	H _{VCO} (s)	dB		-144.91	-104.91	-64.91	-25.70	-1.16	0.38		
Phase Noise at Output of PLL				dBc/Hz		-153.91	-147.91	-138.91	-122.70	-119.16	-138.62
Total Phase Noise at Output of PLL				dBc/Hz	7470	-82.53	-107.33	-120.33	-118.20	-116.70	-137.79

From the spreadsheet it is clear that the overall phase noise does not depend significantly on the estimated current and voltage noise values of the operational amplifier at 1 MHz and 10 MHz offset. The operational amplifier noise at these offset frequencies is very low compared to other phase noise contributors. On the other hand however, the estimated VCO phase noise value at 10 MHz offset

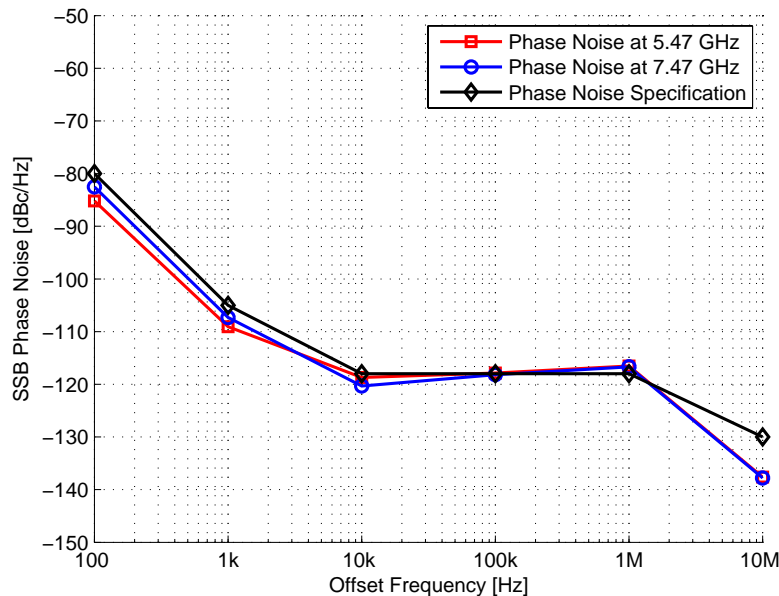


Figure 6.11: Overall synthesiser phase noise at the lowest and highest output frequencies.

has a large impact on the calculated output phase noise, and any difference in estimated and actual phase noise will show when the measured phase noise is compared to the calculated phase noise.

Figure 6.11 shows the graphical representation of the calculated phase noise at both output frequencies. The phase noise specification of Table 1.1 is also shown in the graph. Note that the calculated phase noise is lower than the specification across most offset frequencies, except at 1 MHz offset where it is marginally higher. Improved phase noise response at 1 MHz offset can be obtained by choosing a higher phase margin. However, the slightly exceeding calculated phase noise at 1 MHz offset is largely outweighed by the lower phase noise obtained at nearly all other frequency offsets.

For offset frequencies below about 3 kHz, the reference oscillator is the dominant source of phase noise, while the VCO dominates for offset frequencies above 1 MHz. It is interesting to see the effect of the net frequency multiplication factor on the phase noise of the reference oscillator. Note that, at offset frequencies below about 3 kHz where the reference oscillator phase noise dominates, the overall phase noise is slightly higher at 7.47 GHz compared to that at 5.47 GHz. This is expected, since the net multiplication factor changes from $N_{net} = \frac{5470}{100} = 54.7$ to $N_{net} = \frac{7470}{100} = 74.7$, representing a 2.71 dB increase in reference oscillator phase noise. The increase in reference oscillator phase noise is directly visible in the overall phase noise of the synthesiser for offset frequencies below about 3 kHz.

6.5 Frequency Synthesiser Power Level Design

This section briefly investigates the power level design of the frequency synthesiser. Power level design is usually an approximate but important design step, and reduces to considering the gain or loss of the various components that comprise a system. Power level design is important in ensuring adequate component operation and in obtaining desired output power.

Rather than arguing the need of amplifiers at several stages of the synthesiser, the estimated power levels with the amplifiers in place, are shown. In doing so, the power level design becomes self explanatory.

Figure 6.12 shows a block diagram of the frequency synthesiser with the estimated power levels at various stages. The gain or loss of the different components were taken from the datasheets. The *select-on-test* (SOT) attenuators are optional and not required by default.

The values shown serve only as an estimate to expected power levels, and some tolerance should be expected. The reason for this is because, in many cases, the output power, gain or loss of components under the specific operating conditions of the synthesiser is not exactly known. Consider the *Mini-Circuits* frequency doubler for example. The conversion loss window is specified as 11.5 – 15 dB, and depends on the input frequency and input power. The conversion loss of the doubler under the operating conditions of the synthesiser is not specifically given however. An average conversion loss of 13 dB has been assumed.

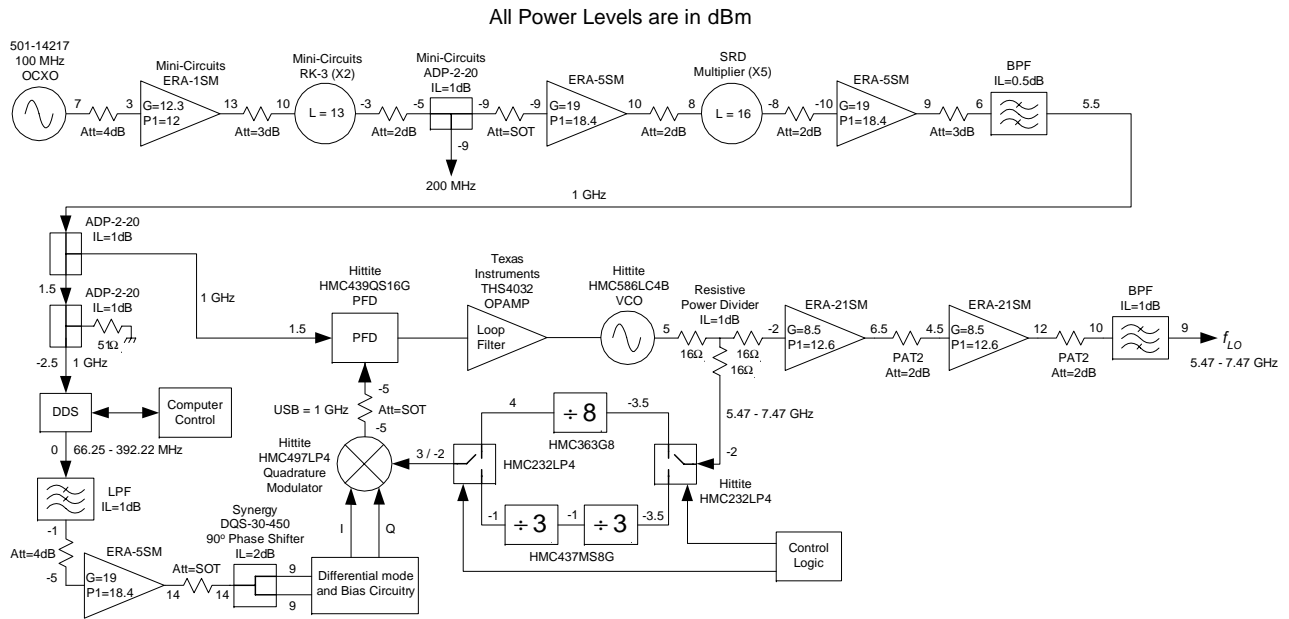


Figure 6.12: Approximated power levels at various stages of the frequency synthesiser.

A number of components of the synthesiser operate over a range of frequencies. In such cases, the output power, gain or loss of that component varies over frequency. Average values have each case been assumed. Mismatch between components and gain compression can also cause slightly different power levels to be observed.

6.6 Conclusion

This chapter discussed the design of the frequency synthesiser for optimal phase noise performance. In the first part of this chapter the various transfer functions required for calculation of the loop bandwidth and overall phase noise of the synthesiser, were derived. In Section 6.3 the loop bandwidth for optimal phase noise performance was found and the effect of different phase margins on the closed-loop frequency response of the loop was investigated. In Section 6.4 the overall phase noise of the synthesiser at the lowest and highest output frequencies was calculated. It was shown how well a PLL-based frequency synthesiser could match the phase noise specification of Table 1.1. The final section of this chapter briefly considered the power levels at various stages of the synthesiser.

Chapter 7

Measured Results of Various Synthesiser Components

7.1 Introduction

This chapter discusses the measured results of various components of the synthesiser. In the first part of this chapter the measurements of the reference oscillator and multiplier chain are presented and discussed. Measurements of the DDS are given and briefly discussed in Section 7.3. In the final section of this chapter, the measured response of the quadrature modulator under various operating conditions is presented and investigated.

7.2 Reference Oscillator and Multiplier Chain

Figure 7.1 shows the frequency content of the *Wenzel* OCXO, measured on a *Rohde & Schwarz* FSEK30 spectrum analyser. The fundamental output power of 5.41 dBm is within the output power window of $7 \text{ dBm} \pm 2 \text{ dB}$ specified in the datasheet. The second harmonic is more than 35 dB lower compared to the fundamental frequency component, and higher order harmonics decay rapidly.

Figure 7.2 shows a photo of the developed multiplier chain circuit. The circuit provides SMA connector outputs at 200 MHz and 1 GHz that are positioned on the back of the printed circuit board (PCB). Only the centre pins of the connectors are visible in the photo. *GIL-MC3D* ($h = 0.787 \text{ mm}$, $\epsilon_r = 3.86$) substrate was used. The reader is referred to Appendix E for the multiplier chain circuit diagram.

Figure 7.3 shows a measurement of the wideband frequency spectrum at the 200 MHz output. The spectrum is rich in harmonic content. The output power in the 200 MHz component is equal to -10.62 dBm , 1.62 dB lower than the predicted power shown in Figure 6.12. Note that the fundamental frequency component of 100 MHz is also present in the output spectrum. The nonlinear

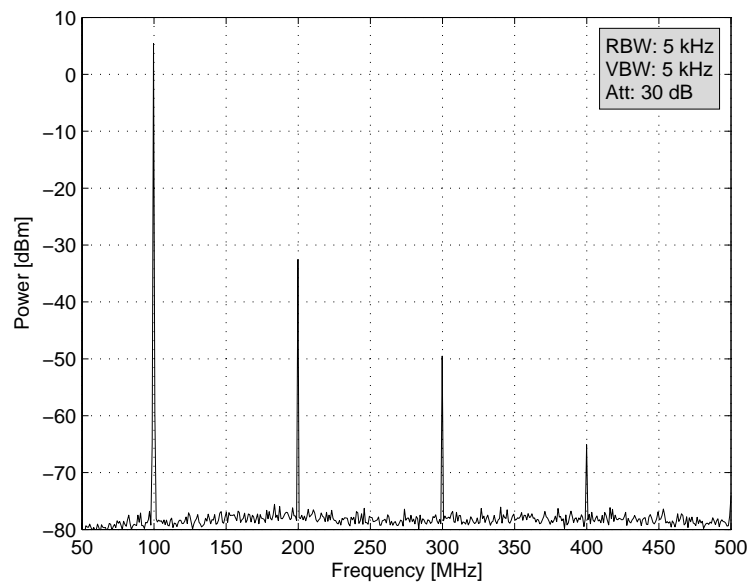


Figure 7.1: Measured frequency content of the *Wenzel* OCXO.

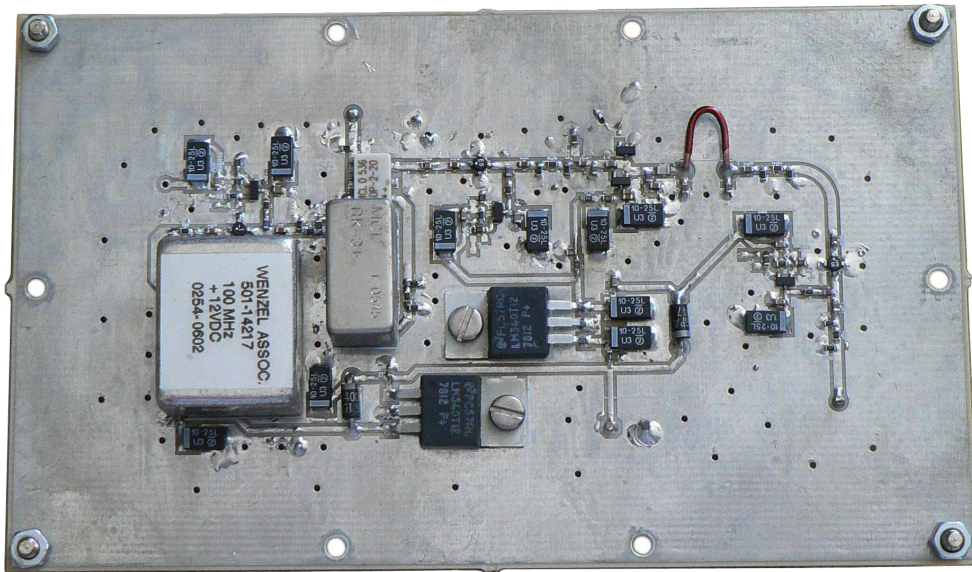


Figure 7.2: A photo of the developed multiplier chain.

behaviour of the doubler also produces higher order components. It is interesting to note that a low power 1 GHz component is already present in the spectrum.

The relative difference in power between the desired 200 MHz component and the fundamental and third harmonic components is not that high as expected. The datasheet of the doubler specifies the fundamental and third harmonic components to be at least 20 dB below the carrier. Figure 7.3 shows that the fundamental and third harmonic components are only about -16 dBc and -10.5 dBc, respectively. Despite the high levels of power in undesired components, no filtering at the output of the doubler deemed necessary.

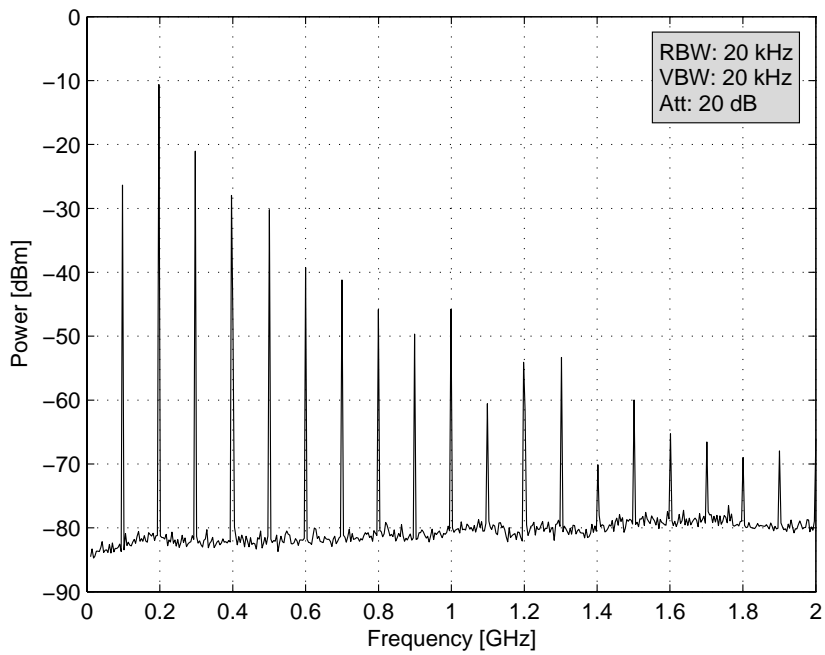


Figure 7.3: Frequency content at the 200 MHz output.

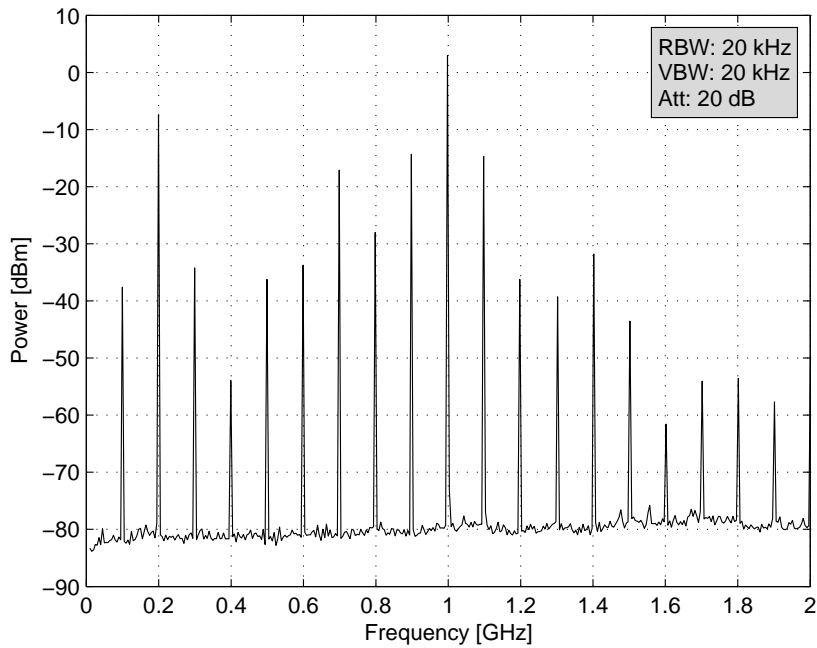


Figure 7.4: Unfiltered frequency spectrum at the 1 GHz output.

Figure 7.4 shows a plot of the unfiltered frequency spectrum measured at the 1 GHz output of the multiplier chain. The frequency components are all spaced 100 MHz apart. The two components closest to the desired component at 1 GHz are of most concern and are about -17 dBc. The cutoff rate of the combline filter determines how well these undesired components are suppressed.

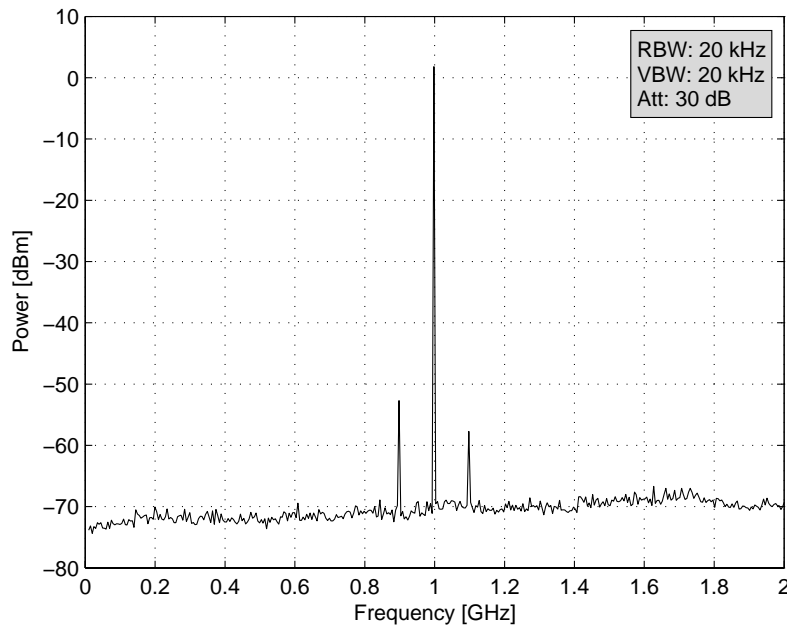


Figure 7.5: Filtered frequency spectrum at the 1 GHz output.

Figure 7.5 shows the same measurement, but with the combline filter added to the output. Note how well the filter cleans the spectrum from unwanted frequency components. The only undesired frequency components left are those at 900 MHz and 1.1 GHz. Comparing Figure 7.4 to Figure 7.5 shows that the power in these two components has been reduced by the rate of attenuation of the filter, as expected. From Chapter 5, the insertion loss of the combline filter at 900 MHz is equal to 36 dB. This is very close to the difference of $-14.32 \text{ dBm} - (-52.71 \text{ dBm}) = 38.39 \text{ dB}$ in power observed at 900 MHz. The extra bit of attenuation is largely the result of the cables used to connect the filter to the output of the multiplier chain and spectrum analyser.

The output power at 1 GHz is equal to 1.79 dBm, and includes the loss of the two cables used. The cables account for about 1 dB of loss. If this loss is taken into account, the actual output power is 2.71 dB lower than that estimated in Chapter 6. The lower output power is not of any concern since the low-end input sensitivity of the DDS and PFD is equal to -20 dBm and -10 dBm , respectively. The actual measured output power of the multiplier chain is safely above these minimum values.

Figure 7.6 shows the measured phase noise of the 1 GHz signal. The phase noise was measured on an *Aeroflex PN9000B* phase noise measurement instrument, using the reference phase locking method. The noise floor of the instrument as specified in the manual is also shown in the graph. Note that the measured phase noise is mostly that of the *Aeroflex* instrument, since the measured phase noise lies on the instrument noise floor for most offset frequencies. For these offset frequencies, no useful information regarding the phase noise of the device under test (DUT) can be obtained, except that the phase noise of the DUT is at least 3 dB less than that of the instrument noise floor. Only for offset frequencies below 100 Hz and above about 300 kHz, the measured phase noise is that of the 1 GHz signal.

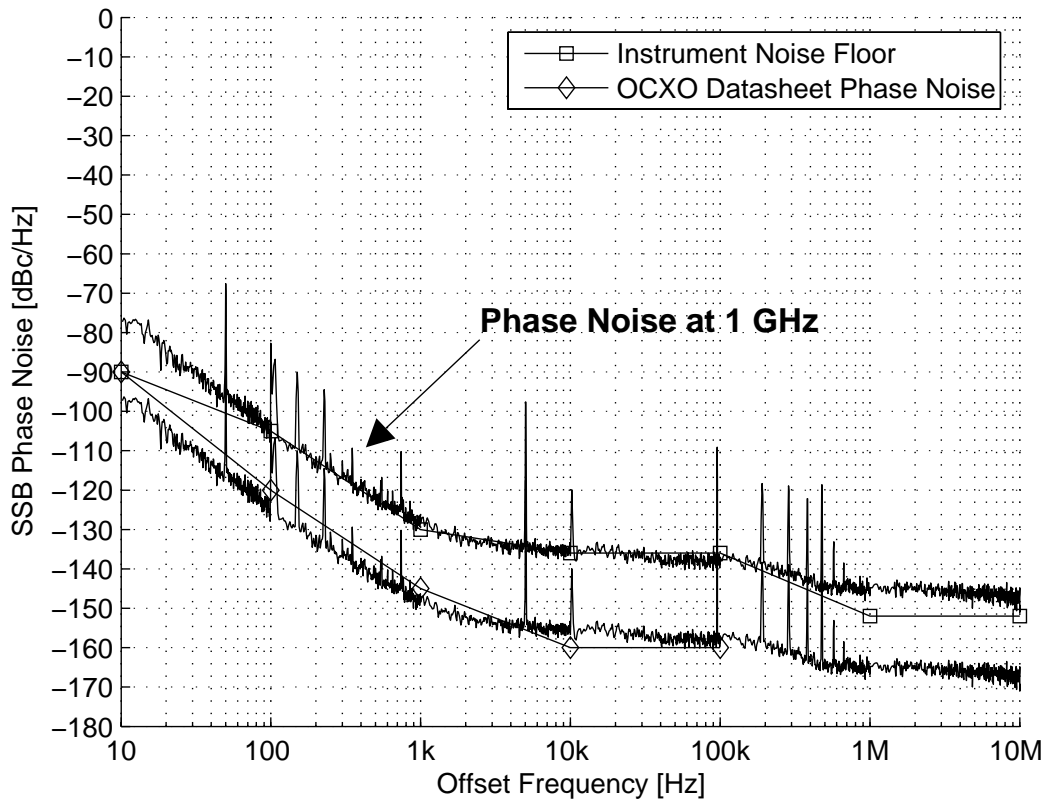


Figure 7.6: Measured phase noise of the 1 GHz signal.

An upper bound on the phase noise of the 100 MHz OCXO can be found by subtracting $20 \log_{10}(10) = 20$ dB from the measured phase noise of the 1 GHz signal. Figure 7.6 shows the upper bound for the OCXO phase noise. When compared to the phase noise of the datasheet, it is surprising to see that the upper bound at offset frequencies lower than 4 kHz is less than the oscillator phase noise specified in the datasheet. The measured phase noise thus suggests that the actual phase noise of the OCXO is somewhat lower than that given by the datasheet for offset frequencies lower than 4 kHz. This should be kept in mind when the phase noise of the complete synthesiser is presented in the next chapter.

7.3 DDS Measurements

A DDS evaluation board is used for the synthesiser. Figure 7.7 shows the measurement setup for investigation of the spectral behaviour of the DDS. The DDS is programmed using the parallel port of a computer not visible in the photo.

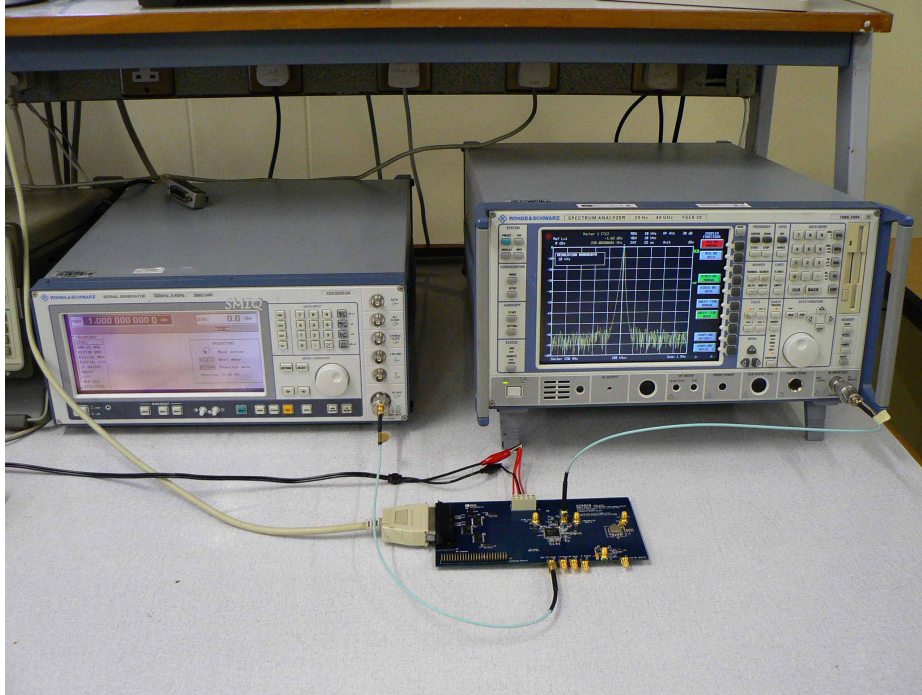


Figure 7.7: Measurement setup for characterisation of the DDS.

Figure 7.8(a) shows a measurement of the Nyquist frequency band (DC - 500 MHz), with the DDS programmed to an output frequency of 250 MHz. The spurious-free dynamic range (SFDR) for this specific output frequency is greater than 70 dB. Figure 7.8(b) shows the spectrum at offset frequencies close to the carrier. No spurious components are noticeable. The output power, without a filter connected to the output, is equal to -1.34 dBm.

Figure 7.9(a) shows an unfiltered wideband measurement of the DDS frequency spectrum. Note the various unwanted frequency components that are present in the spectrum.

Recall from Chapter 3 that as a result of the sampling process of the DAC, undesired frequency components are present at

$$f = kf_{clk} \pm f_{out} \quad k = 1, 2, 3, \dots \quad (7.1)$$

where f_{clk} is the DDS clock frequency of 1 GHz. Also note the *sinc* amplitude rolloff in the spectrum. Harmonics of the output frequency are a result of DAC nonlinearity, and are also visible in the spectrum. Note that the DDS clock frequency leaks through to the output port of the DDS. This is known as *clock feedthrough*.

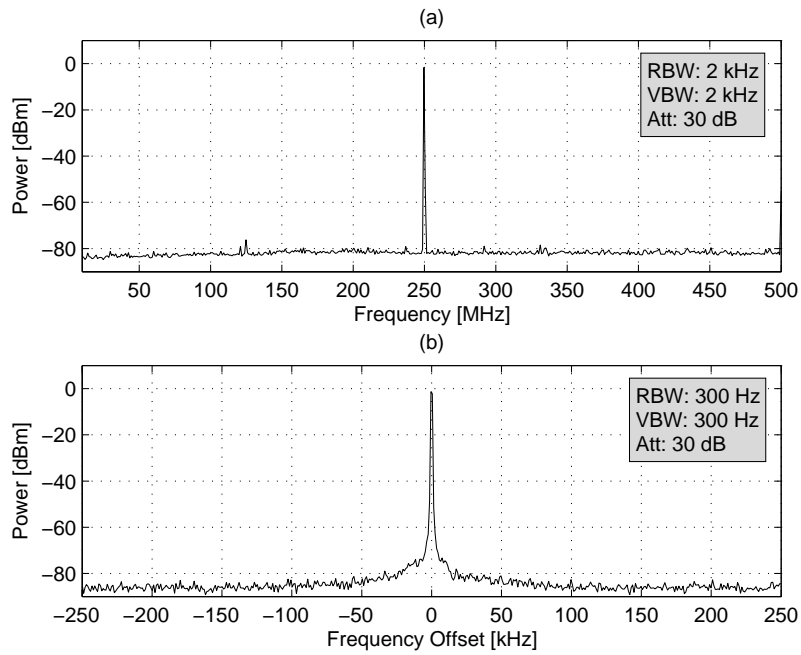


Figure 7.8: (a) Nyquist frequency band and (b) close-in frequency spectrum.

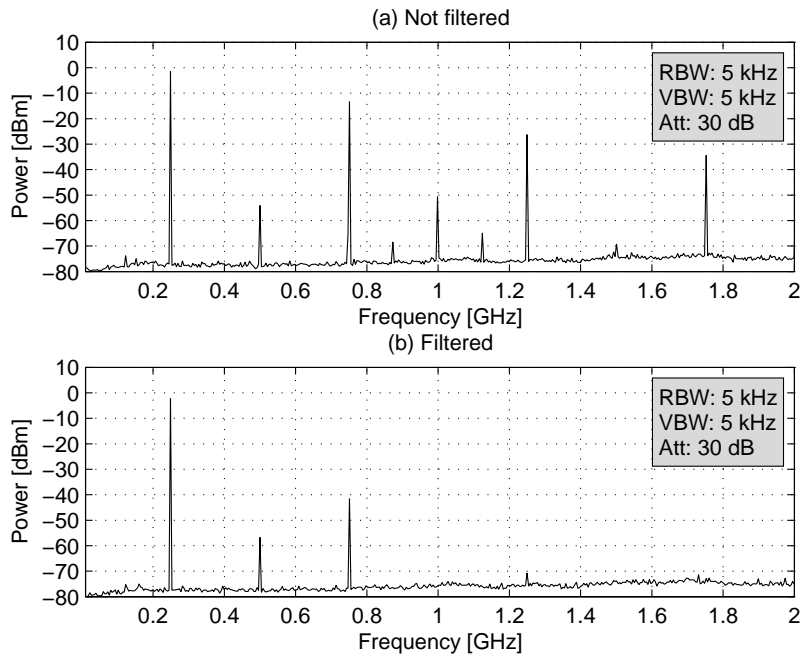


Figure 7.9: (a) Unfiltered wideband frequency spectrum (b) Filtered spectrum.

Figure 7.9(b) shows the frequency spectrum with a fifth-order Chebyshev lowpass filter attached to the output port of the DDS. The measured frequency response of the filter is shown in Appendix C. The lowpass filter has the desired effect of significantly suppressing undesired frequency components.

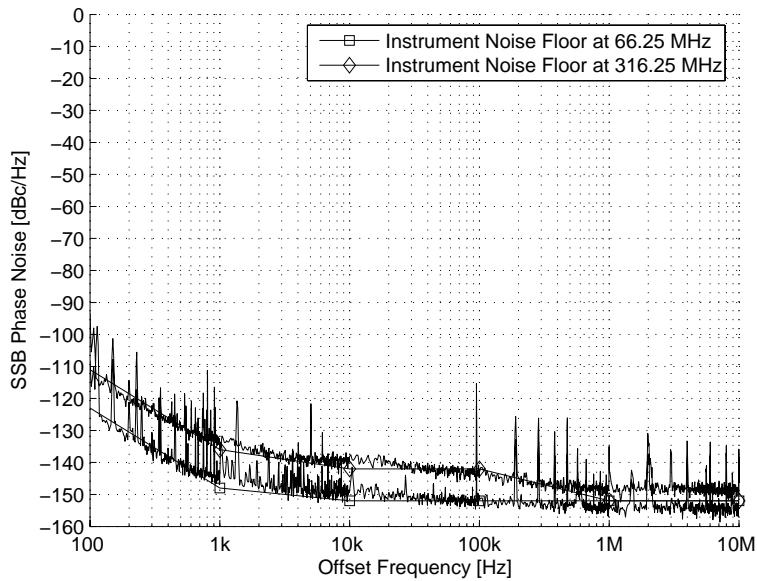


Figure 7.10: DDS phase noise measured at two different output frequencies.

Figure 7.10 shows the measured phase noise of the DDS at 66.25 MHz and 316.25 MHz, where the reference phase locking method of the *Aeroflex* instrument has been used. The 1 GHz signal at the output of the multiplier chain was used for the DDS clock. The phase noise measurement again results in measurement of the instrument noise floor and yields no information regarding the phase noise of the DDS itself. The measurement shows that the DDS phase noise is not significantly higher than expected.

7.4 Quadrature Modulator Measurements

The quadrature modulator directly affects the spurious performance of the synthesiser. Intermodulation (IM) products generated by the modulator are scaled to the output of the synthesiser by the closed-loop transfer function of the PLL. If the IM products are located at offset frequencies well within the loop bandwidth of the PLL, they are scaled to the output of the synthesiser by $20 \log_{10}(N)$ dB, where N is the frequency divider value of the PLL. IM products located at offset frequencies far outside the loop bandwidth of the PLL are attenuated by the lowpass frequency response of the loop. It is the IM products that are produced at offset frequencies close to the carrier that are of concern and should be investigated.

The HMC497LP4 quadrature modulator from *Hittite* can be operated in single-ended or differential mode. Both modes are investigated. For characterisation purposes, an evaluation board of the quadrature modulator was used. Figure 7.11 shows a photo of the evaluation board. Note the differential inputs of the I , Q and LO channels. The RF output port is single-ended. The LO port is driven in single-ended mode, that is, the LO signal is applied to the LO^+ port, while the LO^- port is terminated in a 50Ω load.

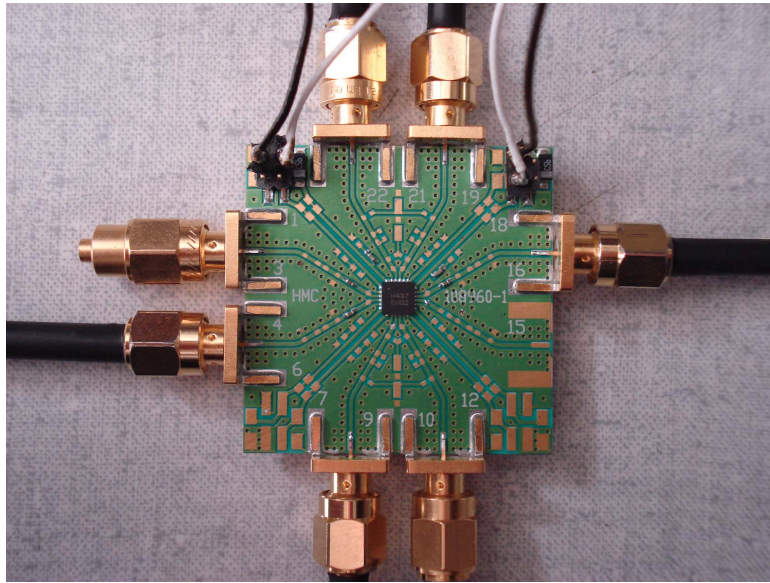


Figure 7.11: A photo of the HMC497LP4 evaluation board.

There are an endless number of possible mixing frequencies that can be investigated. Recall from Chapter 3 that in general, the quadrature modulator produces spectral components at

$$f = mf_{IQ} + nf_{LO} \quad m, n = 0, \pm 1, \pm 2, \dots \quad (7.2)$$

For evaluation purposes, a baseband and local oscillator frequency of $f_{IQ} = 248.75$ MHz and $f_{LO} = 1000 - 248.75 = 751.25$ MHz were chosen, respectively. The combination of these two input frequencies produces IM products close to the carrier.

To obtain quadrature phase signals at a baseband frequency of 248.75 MHz, an equal power divider is used to split the input signal into two channels of equal amplitude. The power divider is followed by two cables of different length, introducing the 90° of relative phase shift required. The calculations for finding the physical lengths of the transmission lines required to obtain the relative 90° phase shift, can be found in Appendix A.

7.4.1 Single-Ended Operation

In the single-ended mode the I^- and Q^- ports are terminated in 47Ω resistors. The quadrature RF signals are applied to the I^+ and Q^+ ports that are also terminated in 47Ω resistors. A recommended DC voltage of 1.5 V is applied to both I and Q channels.

Figure 7.12 shows the measurement setup for the single-ended mode of operation. The power divider that is used to split the input signal into two separate channels can be seen in the photo. The black cable connected to one of the output ports of the power divider is the cable that was specially made to obtain quadrature phase channels. A PCB connected in between the modulator and power divider

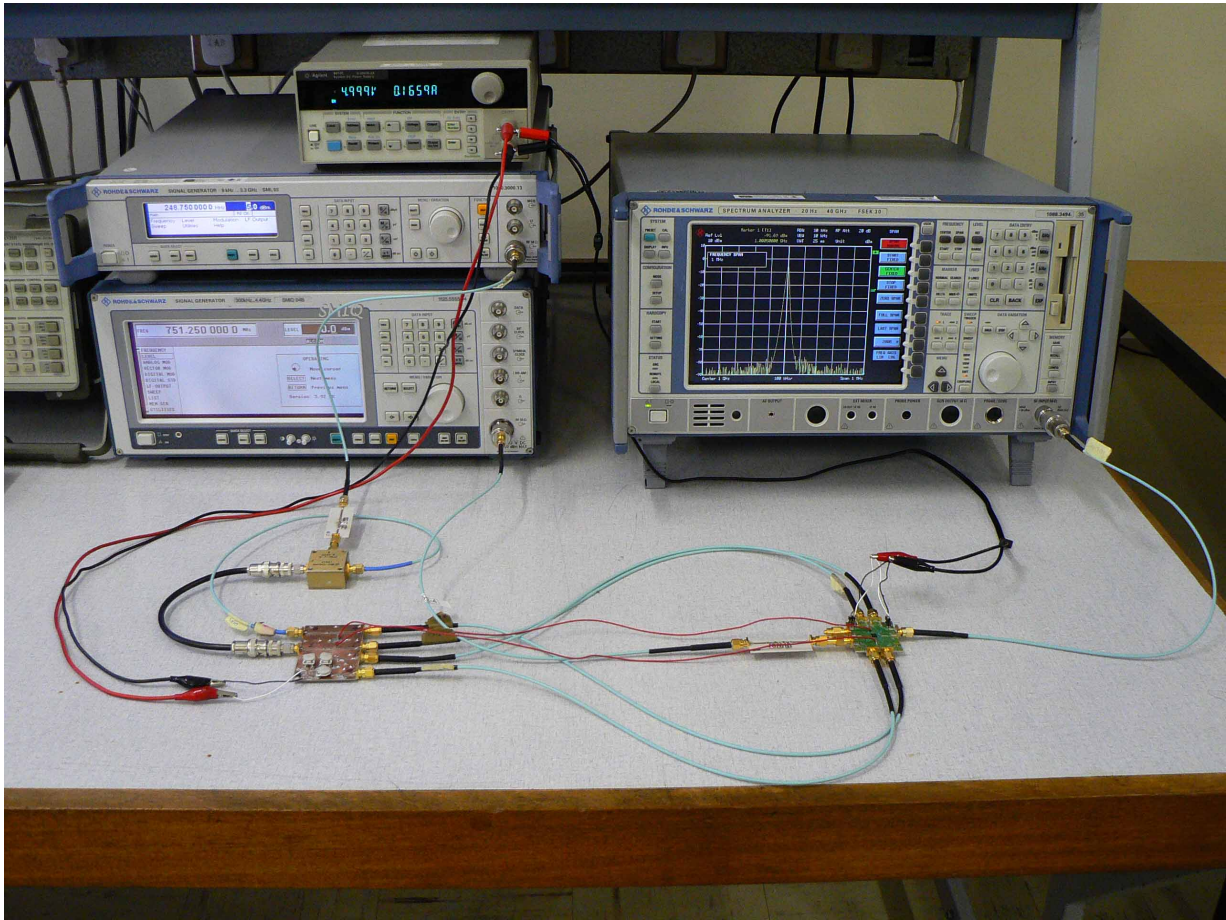


Figure 7.12: A photo of the single-ended measurement setup.

provides finely adjustable DC voltages required for both the I and Q channels. Care was taken to use lines of equal length between the PCB and modulator to preserve the 90° phase difference. To verify the line length calculations and actual phase difference between channels, the I and Q channels at the point where it enters the evaluation board, were measured on an HP54750A sampling oscilloscope. The result is shown in Appendix C. The measurement shows that the phase difference for an input of frequency of 248.75 MHz is essentially 90° .

Figure 7.13 shows the spectral components obtained at the RF output port for the conditions shown. Note the various spectral components that are present in the spectrum. Most of the power is contained in the desired upper sideband (USB) component at $f_{LO} + f_{IQ}$. The sideband suppression, which is the difference in power between the USB and LSB, is about 35 dB.

Sideband suppression depends on the amplitude and phase match of the I and Q channels. To understand this, consider an I channel that is slightly different in amplitude compared to the Q channel. Mathematically

$$\begin{aligned} I(t) &= (A + \varepsilon) \cos(\omega_{IQ}t) \\ Q(t) &= -A \sin(\omega_{IQ}t) \end{aligned} \quad (7.3)$$

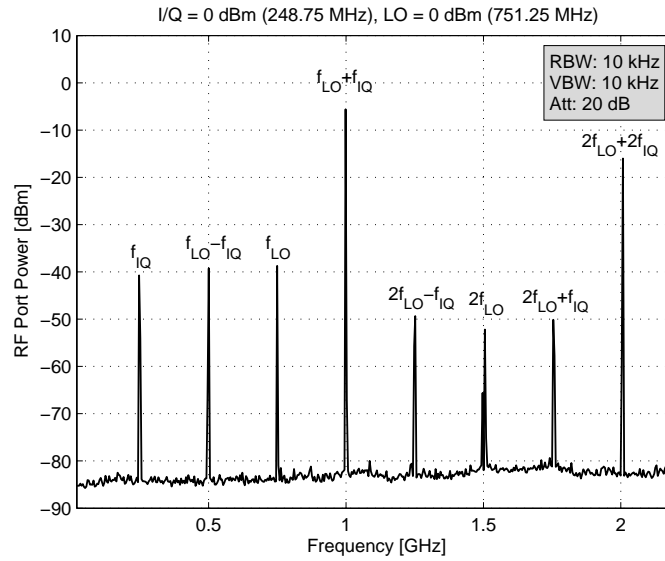


Figure 7.13: Frequency content at the RF output port.

With reference to Equation 3.4, it follows that the modulated signal $m(t)$ can be written as

$$\begin{aligned}
 m(t) &= (A + \varepsilon) \cos(\omega_{LO}t) \cos(\omega_{IQ}t) - A \sin(\omega_{LO}t) \sin(\omega_{IQ}t) \\
 \therefore m(t) &= \varepsilon \cos(\omega_{LO}t) \cos(\omega_{IQ}t) + A \cos(\omega_{LO}t) \cos(\omega_{IQ}t) - A \sin(\omega_{LO}t) \sin(\omega_{IQ}t) \\
 \therefore m(t) &= \frac{\varepsilon}{2} (\cos((\omega_{LO} - \omega_{IQ})t) + \cos((\omega_{LO} + \omega_{IQ})t)) + A \cos((\omega_{LO} + \omega_{IQ})t) \\
 \therefore m(t) &= \left(A + \frac{\varepsilon}{2}\right) \cos((\omega_{LO} + \omega_{IQ})t) + \frac{\varepsilon}{2} \cos((\omega_{LO} - \omega_{IQ})t) \quad (7.4)
 \end{aligned}$$

Equation 7.4 shows that due to the amplitude mismatch, a LSB component at $f_{LO} - f_{IQ}$ is present. For I and Q channels that are not perfectly phase quadrature,

$$\begin{aligned}
 I(t) &= A \cos(\omega_{IQ}t) \\
 Q(t) &= -A \sin(\omega_{IQ}t - \phi) \quad (7.5)
 \end{aligned}$$

The modulated signal can be expressed as

$$\begin{aligned}
 m(t) &= A \cos(\omega_{LO}t) \cos(\omega_{IQ}t) - A \sin(\omega_{LO}t) \sin(\omega_{IQ}t - \phi) \\
 \therefore m(t) &= A \cos(\omega_{LO}t) \cos(\omega_{IQ}t) - A \sin(\omega_{LO}t) (\sin(\omega_{IQ}t) \cos(\phi) - \cos(\omega_{IQ}t) \sin(\phi))
 \end{aligned}$$

For small phase errors $\cos(\phi) \approx 1$, and $\sin(\phi) \approx \phi$. The modulated signal reduces to

$$\begin{aligned}
 m(t) &= A \cos(\omega_{LO}t) \cos(\omega_{IQ}t) - A \sin(\omega_{LO}t) (\sin(\omega_{IQ}t) - \cos(\omega_{IQ}t) \phi) \\
 \therefore m(t) &= A \cos((\omega_{LO} + \omega_{IQ})t) + A\phi \sin(\omega_{LO}t) \cos(\omega_{IQ}t) \\
 \therefore m(t) &= A \cos((\omega_{LO} + \omega_{IQ})t) + \frac{A\phi}{2} \sin((\omega_{LO} - \omega_{IQ})t) + \frac{A\phi}{2} \sin((\omega_{LO} + \omega_{IQ})t) \quad (7.6)
 \end{aligned}$$

which again results in a LSB with amplitude proportional to the phase error being present in the

spectrum. Both equations suggest that if a LSB is present due to errors introduced in the modulator, it can be compensated for externally.

Figure 7.13 shows that both the I/Q baseband and LO signals leak through to the RF output port. Various other IM products are also visible. The IM product at 2 GHz is about 10 dB lower compared to the USB, but lies outside the maximum operating bandwidth of the PFD of 1.3 GHz. All the undesired frequency components lie far outside the loop bandwidth of the PLL, and are attenuated by the response of the loop.

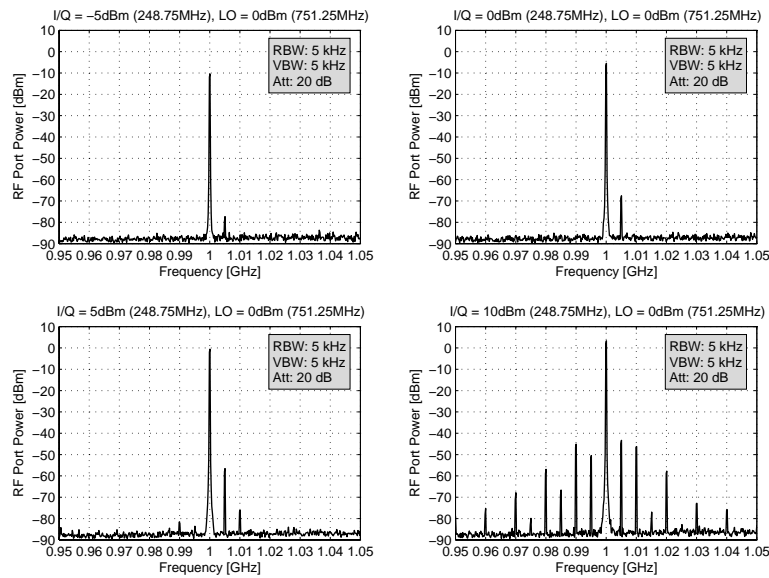


Figure 7.14: Frequency spectrum close to the carrier as a function of I/Q channel power.

At offset frequencies close to the carrier, other IM products are present. Figure 7.14 shows a plot of the frequency spectrum close to the carrier as a function of I/Q power. For the single-ended mode of operation, the I/Q power is the actual input power to the evaluation board. Note the rapid increase in IM product power as the I/Q power increases.

It is evident from the graph that lowering the I/Q power improves the SFDR of the modulator, since the power in the unwanted high-order IM products decreases more rapidly compared to the USB. However, the I/Q power should not decrease beyond the point where the USB power is lower than the minimum input sensitivity of the PFD, which is given as -10 dBm. Figure 7.14 shows that to obtain an USB power of at least -10 dBm, requires the I/Q channel power to be larger than -5 dBm. For use in the synthesiser, an I/Q channel power of 0 dBm was chosen.

For $I/Q = 0$ dBm, the fourth-order spur ($m = -2, n = 2$) at 1005 MHz is -62 dBc. Decomposition of the SSB spur into AM and FM results in AM and FM sidebands equal to $-62 - 6 = -68$ dBc. The PFD typically converts the input signals to digital signals by passing them through a limiting high gain differential amplifier, removing the AM sidebands. The remaining FM sidebands are scaled to the output of the synthesiser by the magnitude of the closed-loop transfer function. Figure 6.10

shows that the magnitude of $H(s)$ is 2 dB at 5 MHz. The expected levels of the spurious components at the output of the synthesiser, relative to the carrier, are therefore equal to $-68 + 2 = -66$ dBc.

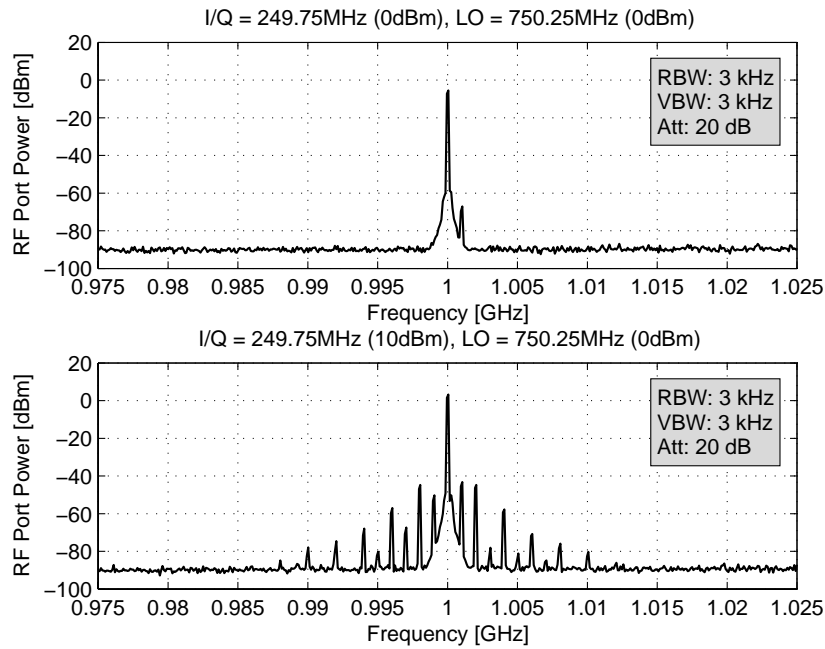


Figure 7.15: IM products for another combination of input frequencies.

Figure 7.15 shows the measured frequency spectrum for another combination of input frequencies producing fourth-order spurious components at offset frequencies 1 MHz from the carrier. The spur at 1001 MHz ($m = -2, n = 2$) for an I/Q input power of 0 dBm, is again -62 dBc. This shows that the SFDR for the same order IM products is comparable, even for different sets of input frequencies. In this case, the magnitude of the closed-loop transfer function $H(s)$ at 1 MHz is equal to 16.78 dB. Therefore, the expected spurious levels at the output of the synthesiser is equal to $-62 - 6 + 16.78 = -51.22$ dBc. According to Table 1.1 this is close to the maximum spurious levels that can be tolerated.

The power in the IM products as a function of I/Q power, is depicted in Figure 7.16. The spurs at 995 MHz and 1005 MHz are fourth-order products, while those at 990 MHz and 1010 MHz are eighth-order IM products.

Figure 7.17 shows the USB power plotted versus I/Q power. The 1 dB compression point occurs at an USB output power of 3 dBm. It is interesting to observe that the USB power is independent of LO power.

Figure 7.18 shows the uncalibrated and calibrated carrier feedthrough. Ideally no carrier should be present in the spectrum. The carrier feedthrough is calibrated by slightly adjusting the DC voltages between the I/Q channels. The calibration was performed for an I/Q power of 0 dBm. Note that for the calibrated case, the carrier power decreases rapidly when the I/Q power approaches 0 dBm.

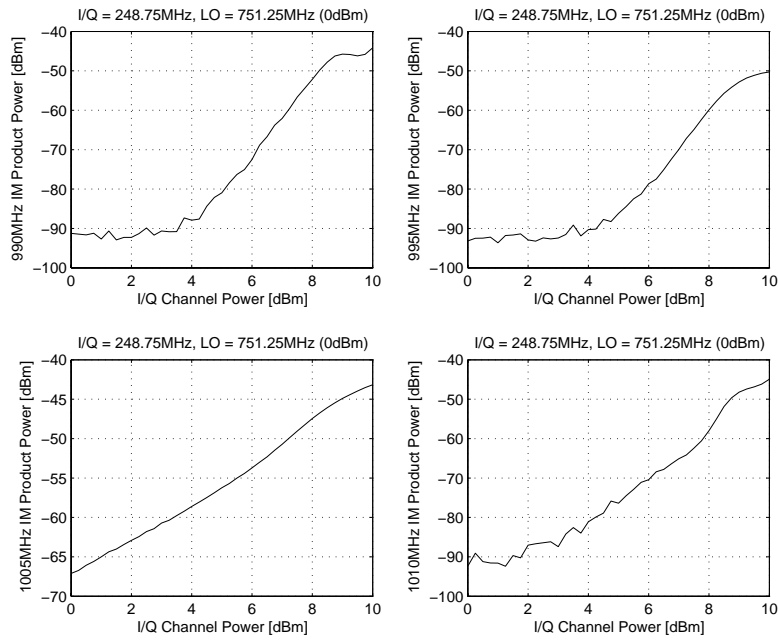


Figure 7.16: IM products as a function of I/Q channel power.

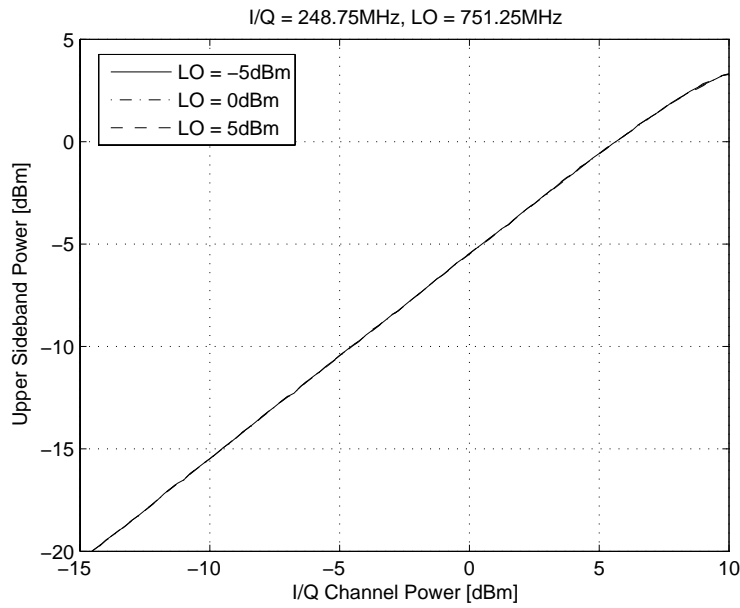


Figure 7.17: USB power as a function of I/Q power.

To understand why the carrier feedthrough is influenced by DC offset levels between channels, consider

$$\begin{aligned}
 I(t) &= A \cos(\omega_{IQ}t) + \epsilon \\
 Q(t) &= -A \sin(\omega_{IQ}t)
 \end{aligned}
 \tag{7.7}$$

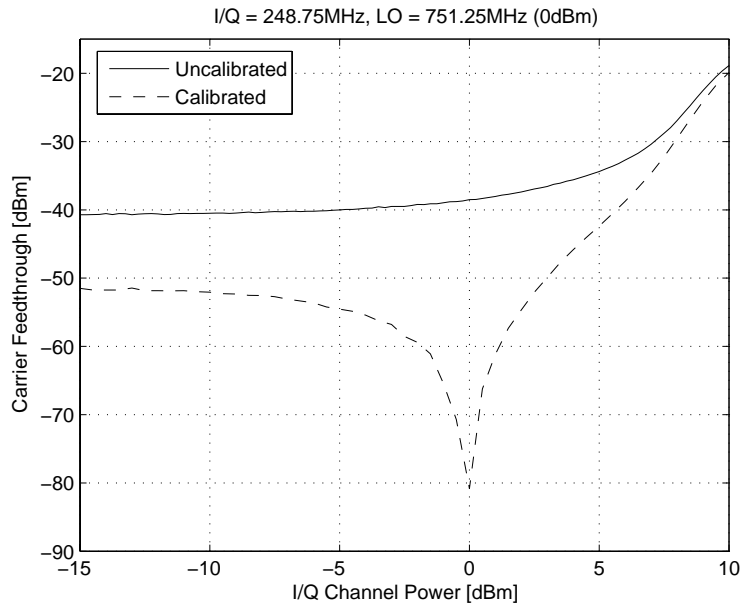


Figure 7.18: Uncalibrated and calibrated carrier feedthrough.

It follows that the modulated signal $m(t)$, is equal to

$$\begin{aligned} m(t) &= \cos(\omega_{LO}t) (A \cos(\omega_{IQ}t) + \varepsilon) - A \sin(\omega_{LO}t) \sin(\omega_{IQ}t) \\ \therefore m(t) &= A \cos((\omega_{LO} + \omega_{IQ})t) + \varepsilon \cos(\omega_{LO}t) \end{aligned} \quad (7.8)$$

Thus, besides the desired USB, the unwanted carrier signal is also present.

7.4.2 Differential Operation

In this mode of operation, transformers are used to produce the differential inputs for the I and Q channels. The I^+/Q^+ and I^-/Q^- ports are again terminated in 47Ω resistors soldered onto the evaluation board.

The PCB that was developed for evaluation of the modulator in differential mode, is shown in Figure 7.19. *Mini-Circuits* ADTT1-1 transformers with an impedance ratio of 1 were used. Two adjustable voltage dividers are used to set the DC levels of each channel.

Figure 7.20 shows a plot of the frequency content close to the USB as a function of I/Q power. For the differential mode of operation, the I/Q power is the input power to the PCB. The insertion loss of the transformers is specified as 3 dB. Therefore, the actual I/Q power entering the modulator evaluation board is about 3 dB lower compared to the single-ended mode of operation. Comparing Figure 7.20 to Figure 7.14 shows that some of the spurs at high offset frequencies are no longer present. The power in spurs at low offset frequencies has also decreased. Although the I/Q channel power at the input of the modulator is about 3 dB less compared to the single-ended case, the output power of the

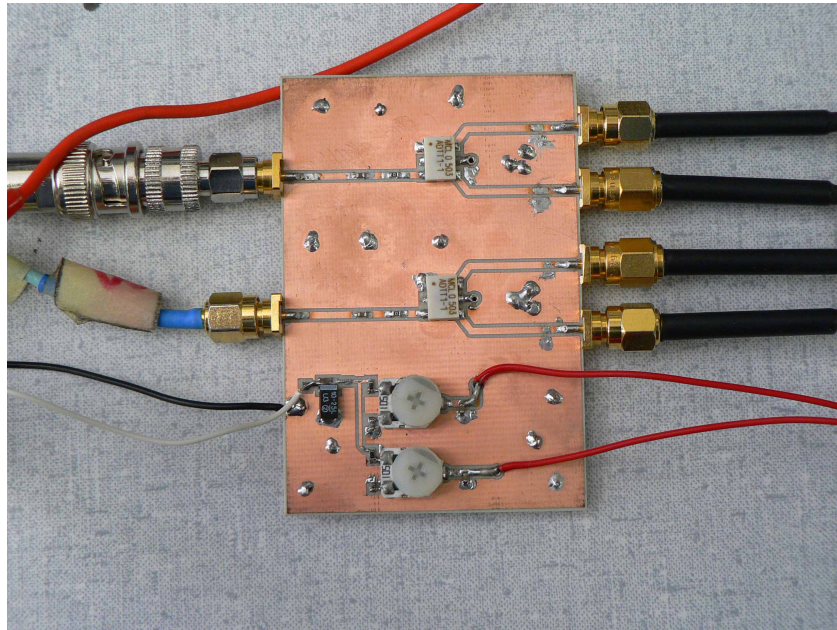


Figure 7.19: PCB used for differential mode evaluation.

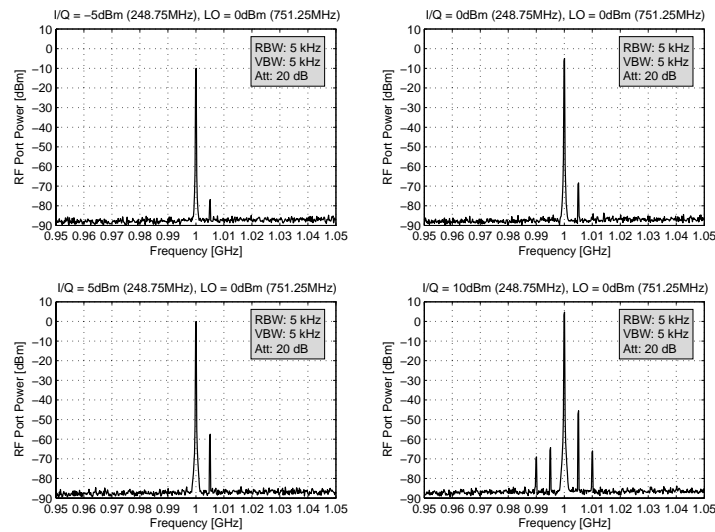


Figure 7.20: Frequency content close to the carrier as a function of I/Q power.

USB is still the same as compared to the single-ended case. Operating the modulator in differential mode therefore yields improved SFDR.

To see the difference in undesired IM product power more clearly, Figure 7.21 compares the power in the four closest IM products for the single-ended and differential modes of operation. From the graph it can be seen that operating the modulator in differential mode results in improved SFDR.

Figure 7.22 shows a plot of the power in the LSB as a function of relative phase difference between the I and Q channels. The phase between channels was varied by inserting adaptors of different length to each of the channels. Note that as expected, the sideband suppression is optimal for phase

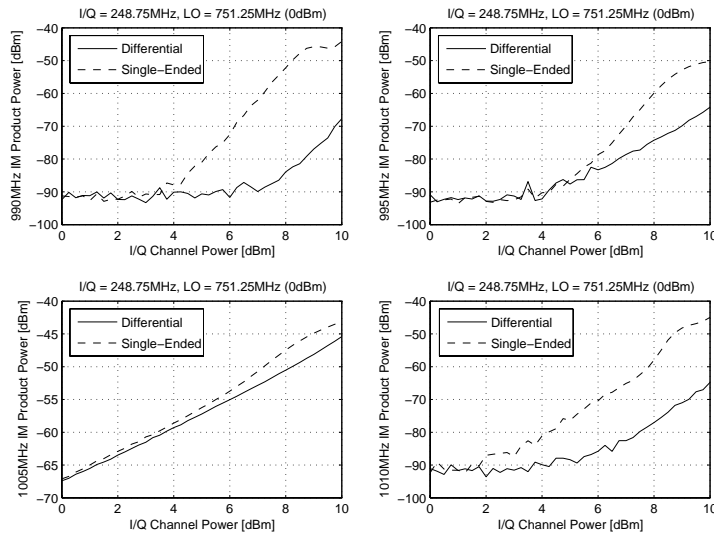


Figure 7.21: Comparison between IM products for the single-ended and differential modes of operation.

differences close to 90° . Any deviation from 90° results in the undesired sideband power to increase. The differential mode of operation yields slightly better sideband suppression.

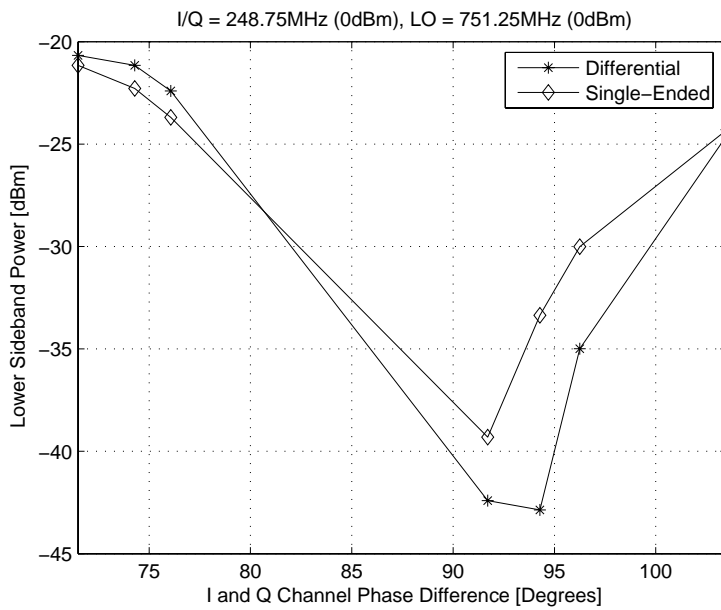


Figure 7.22: LSB power as a function of relative *I* and *Q* channel phase difference.

Figure 7.23 shows a plot of the USB power versus *I/Q* power. The 1 dB compression point exceeds $USB = 5$ dBm which is more compared to the 1 dB compression point of 3 dBm of the single-ended mode of operation.

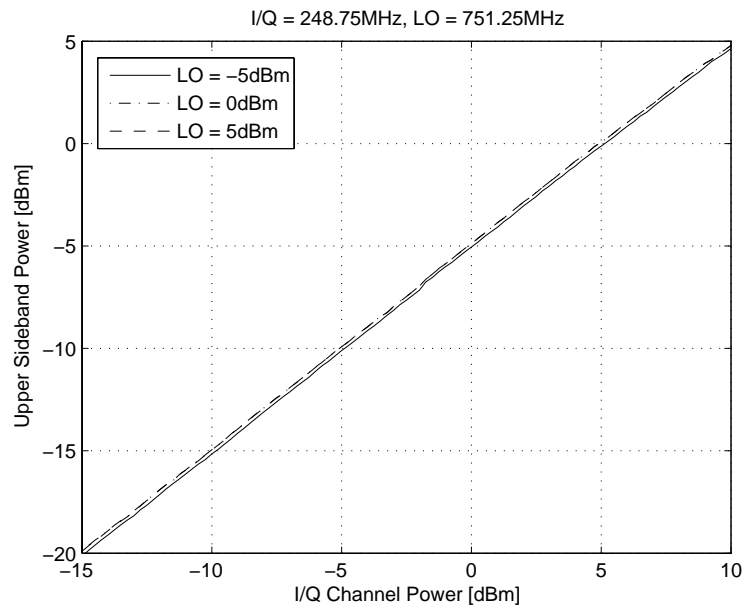


Figure 7.23: Upper sideband power as a function of I/Q power.

7.5 Conclusion

This chapter presented and discussed various measurements of components that are used for the frequency synthesiser. In the first part of the chapter the reference oscillator and multiplier chain measurements were discussed. It was seen that the frequency doubler produced a frequency spectrum rich in harmonic content. Despite the high power in undesired harmonics, the sharp cutoff rate of the combline filter ensured an SFDR in excess of 50 dB at the output of the multiplier chain. Phase noise measurements indicated that the phase noise of the multiplier chain lies below the noise floor of the *Aeroflex* instrument. Therefore, only an upper bound on the multiplier chain and OCXO phase noise could be found.

The DDS showed good wideband and close-in SFDR. The sources of various wideband spectral components were identified, and a lowpass filter was used to suppress most of the undesired components. An attempt to measure the phase noise of the DDS again resulted in the measurement of the instrument noise floor.

The quadrature modulator was investigated in both single-ended and differential modes of operation. The differential mode of operation revealed improved SFDR and sideband suppression. Based upon these observations, it was decided to use the quadrature modulator in the differential mode for use in the synthesiser.

Chapter 8

Frequency Synthesiser Phase Noise, Spectral Purity and Transient Response

8.1 Introduction

In this chapter various measurements of the complete frequency synthesiser are presented and discussed. In the first section the measured phase noise at the lowest and highest output frequencies are presented. It is shown how well the measured phase noise correlates with the phase noise calculated in Chapter 6. The chapter continues by investigating the spurious performance of the synthesiser in Section 8.3. A variety of narrow and wideband measurements at different output frequencies are presented and discussed. In the final section of this chapter, the transient response of the synthesiser is briefly considered.

A photo of the developed PLL circuit of Figure 3.4 is depicted in Figure 8.1. The complete circuit diagram can be found in Appendix E. The PCB consists of FR-4 ($h = 0.5$ mm, $\epsilon_r \approx 4.3$) and Rogers 4003C ($h = 0.508$ mm, $\epsilon_r = 3.38$) substrate pressed together, forming a four-layer PCB. The ground plane is a solid layer located between the two substrates, providing good RF ground. Electronic components on the RF layer are shielded from external noise sources with an aluminium cavity that encloses the whole RF layer. The cavity which is visible in Figure 8.2 also serves as a heat sink.

8.2 Measured Frequency Synthesiser Phase Noise

The phase noise of the frequency synthesiser was measured on an *Aeroflex* PN9000B phase noise measurement instrument using the microwave downconverter and built-in RF synthesiser. Figure 8.2 shows a photo of the measurement setup. The aluminium cavities used for the multiplier chain and PLL circuit are visible in the photo.

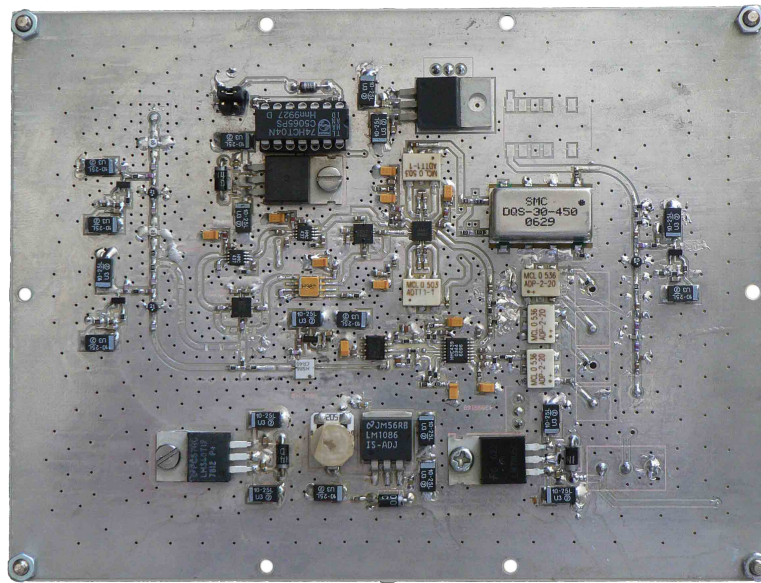


Figure 8.1: A photo of the PLL printed circuit board.

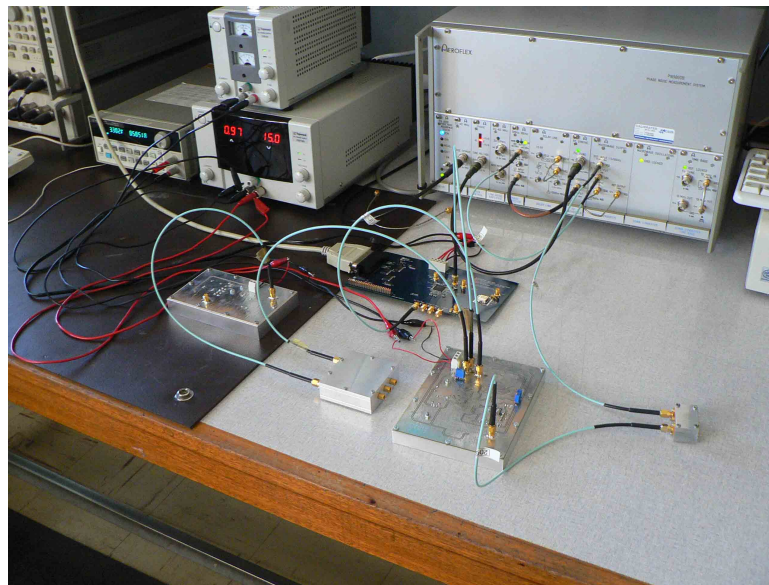


Figure 8.2: Frequency synthesiser phase noise measurement setup.

Figure 8.3 shows the measured phase noise at 5.47 GHz, with $N = 8$. The calculated phase noise of Chapter 6 is superimposed on the graph. The reader is referred to Appendix C for phase noise measurements with $N = 9$.

Note how well the calculated phase noise compares to the measured phase noise. At offset frequencies below about 10 kHz the measured phase noise is somewhat lower than that predicted by theory. Recall from the previous chapter that an upper bound on the phase noise of the 100 MHz reference OCXO was found. It was seen that the upper bound was lower compared to the phase noise given by the manufacturer, suggesting that the actual OCXO phase noise is lower than that specified in the

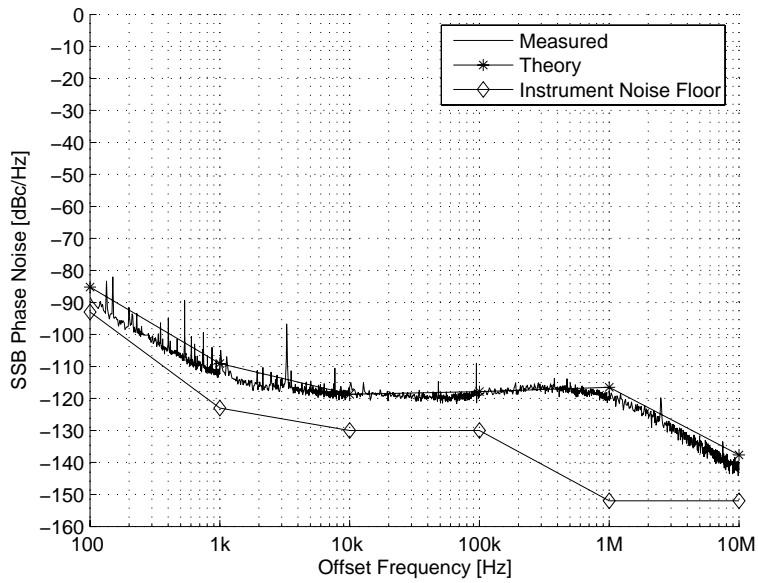


Figure 8.3: Complete synthesiser phase noise at 5.47 GHz, with $N = 8$.

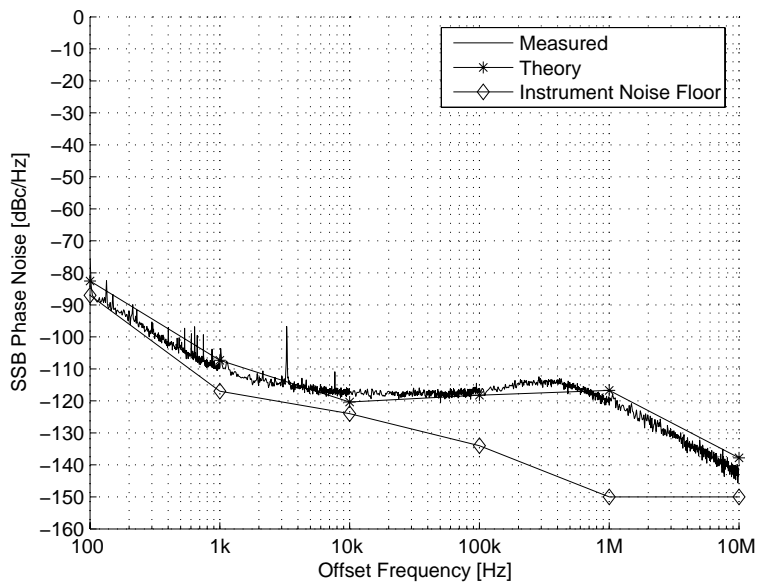


Figure 8.4: Complete synthesiser phase noise at 7.47 GHz, with $N = 8$.

datasheet. From the measurement, it indeed seems that the actual OCXO phase noise is somewhat lower than that given in the datasheet.

At offset frequencies from 10 kHz to 1 MHz the predicted phase noise is essentially equal to the measured phase noise. The slight difference in predicted and measured phase noise at 10 MHz offset can be ascribed to the estimated theoretical value of the VCO phase noise at 10 MHz offset. Note that the estimated VCO phase noise of -139 dBc/Hz at 10 MHz offset is somewhat conservative. The actual phase noise is slightly lower.

Figure 8.4 shows the measured phase noise at 7.47 GHz. The phase noise at 10 MHz offset and offset frequencies lower than 4 kHz is again slightly lower than that calculated for the same reasons discussed in the previous paragraphs.

Figure 8.5 shows the synthesiser phase noise at the lowest and highest output frequencies plotted on the same graph. The phase noise specification of Table 1.1 is also shown. Note that the measured phase noise is lower than or equal to the discrete specification points that are connected with straight lines. The primary objective of meeting the phase noise specification with a PLL-based synthesiser is thus achieved.

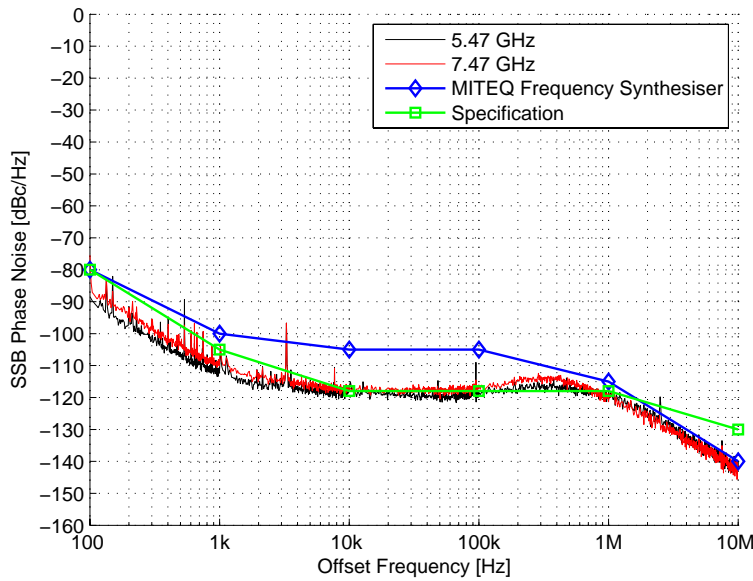


Figure 8.5: Synthesiser phase noise at 5.47 GHz and 7.47 GHz, with $N = 8$.

Figure 8.5 shows that the phase noise for both output frequencies is essentially equal at offset frequencies higher than 1 MHz. This is to be expected, since the phase noise outside the loop bandwidth of the PLL is essentially determined by the phase noise of the VCO. The datasheet of the VCO shows that the VCO phase noise is virtually independent of the tuning voltage and hence output frequency of the VCO. At offset frequencies below about 4 kHz, the measured phase noise at 7.47 GHz is slightly higher compared to that at 5.47 GHz. The reason for this is because the net multiplication factor increases from $\frac{5470}{100} = 54.7$ to $\frac{7470}{100} = 74.7$, resulting in a higher reference oscillator phase noise contribution.

At offset frequencies between about 5 kHz and 1 MHz, the phase noise at 7.47 GHz is expected to be slightly lower compared to the phase noise at 5.47 GHz (see Figure 6.11). The reason for this is because the DDS frequency changes from 316.25 MHz to 66.25 MHz, resulting in a smaller phase noise contribution to the overall phase noise of the synthesiser. The measured phase noise indicates however that the decrease in DDS phase noise is slightly dominated by the increase in reference

oscillator phase noise. The overall result is a slight increase in phase noise at the higher output frequency.

To appreciate the levels of phase noise achieved, the phase noise of the developed frequency synthesiser is compared to a *MITEQ* LNS60806580 frequency synthesiser. *MITEQ* offers high quality frequency synthesiser solutions for military and satellite applications. The LNS series of synthesisers are specifically designed for applications where low phase noise performance is critical. The electrical specification of the *MITEQ* synthesiser is listed in Table 8.1. Note that the synthesiser discussed in this thesis offers broader bandwidth, finer step size and as will be shown, faster switching speed and higher harmonic suppression compared to that of the *MITEQ* synthesiser.

The phase noise is compared in Figure 8.5. The phase noise of the developed frequency synthesiser at both output frequencies is lower compared to that of the *MITEQ* frequency synthesiser at all offset frequencies.

Table 8.1: *MITEQ* LNS frequency synthesiser specification.

Parameter	Specification	
Output Frequency	6.08 - 6.58 GHz	
Output Power	≥ 13 dBm ± 1.5 dB	
Frequency Resolution	Down to 1 kHz	
Switching Speed	10 ms Typical	
Spurious-Free Dynamic Range	-49 dBc Maximum	
Harmonics	-20 dBc Typical	
Phase Noise	100 Hz	-80 dBc/Hz
	1 kHz	-100 dBc/Hz
	10 kHz	-105 dBc/Hz
	100 kHz	-105 dBc/Hz
	1 MHz	-115 dBc/Hz
	10 MHz	-140 dBc/Hz

8.3 Frequency Synthesiser Spectral Purity

Figure 8.6 shows a photo of the measurement setup used for investigation of the spectral performance of the synthesiser. The interdigital filter at the output of the synthesiser is only inserted for out-of-band spectral measurements.

Figure 8.7 shows a narrowband plot of the frequency synthesiser spectrum at the lowest, centre, and highest output frequencies. The DDS frequency and divider value N are in each case displayed at the top of the figure. The SFDR is more than 50 dB for all three output frequencies. It is interesting to note that spurious components close to the carrier are generally higher in power due to weaker suppression of the loop at frequencies close to the carrier.

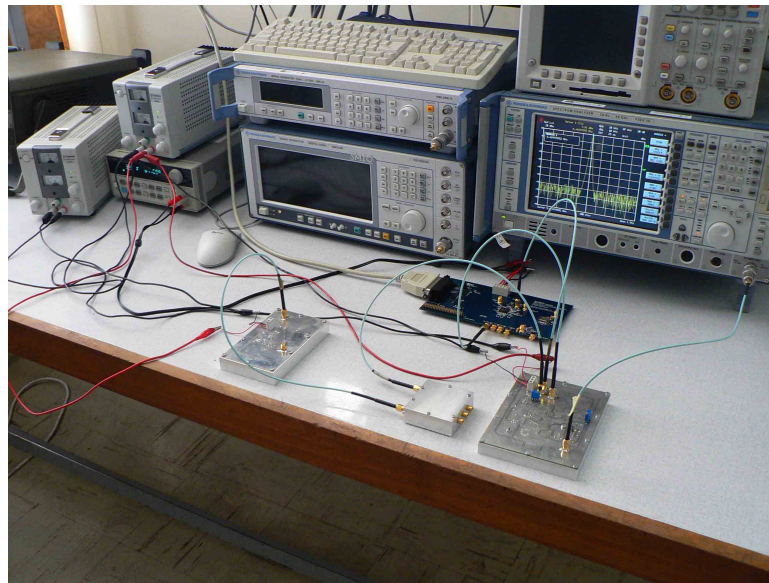


Figure 8.6: Measurement setup for investigating the spurious performance of the synthesiser.

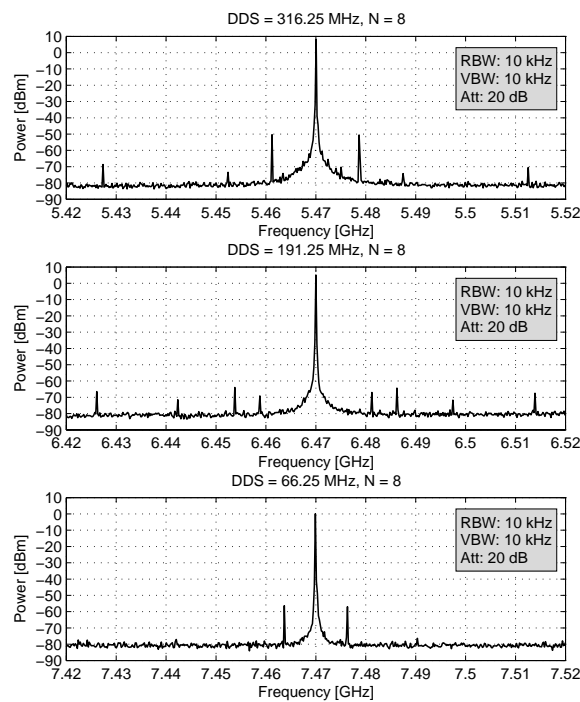


Figure 8.7: Narrowband spectrum of the frequency synthesiser at the lowest, highest and centre frequency.

At 5.47 GHz the output power including cable loss, is equal to 8.1 dBm. The typical loss of a cable similar to that used at the output of the synthesiser is shown in Appendix C. At 5.47 GHz, the cable loss is 1.8 dB. If the loss of the cable is taken into account, the actual output power is approximately 9.9 dBm which is within the specification of 10 dBm \pm 2.5 dB. Note however that at 7.47 GHz, the output power has dropped to 0.1 dBm. The cable accounts for about 2.1 dB of loss, so the actual output power is in the order of 2.2 dBm.

The slope in power observed can largely be ascribed to the *Mini-Circuits* PAT-2 attenuators and ERA-21SM amplifiers used at the output. The attenuators are only rated up to a maximum operating frequency of 7 GHz and at that time were chosen due to the lack of a better available choice. Quite recently *Mini-Circuits* released graphs showing the frequency response of the attenuators and ERA-21SM amplifiers. From these graphs, the slope from 5.47 GHz to 7.47 GHz of both the ERA-21SM and attenuators accounts for about 4 dB of relative difference in power obtained at the lowest and highest output frequencies. If the response of both these components was flat over frequency, the output power would have been approximately $2.2 + 4 = 6.2$ dBm, just 1.3 dB short of the minimum required output power. Some part of the slope in power is also a result of the increase in insertion loss of the resistive power divider and transition from coplanar waveguide to the SMA connector. The transition at the output was modelled and optimised with *CST*. The *CST* model and simulated S-parameters of the transition can be found in Appendix F. It is perhaps worth mentioning that *Mini-Circuits* now have attenuators available that are rated up to a maximum frequency of 8 GHz.

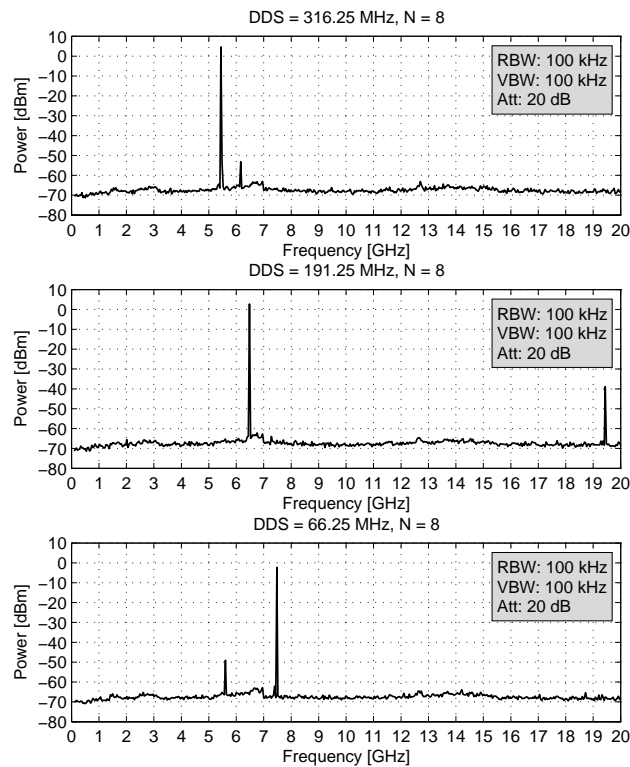


Figure 8.8: Wideband frequency spectrum of the synthesiser at 5.47 GHz, 6.47 GHz, and 7.47 GHz.

Figure 8.8 shows the wideband spurious performance for the same output frequencies. For this measurement, the filter was included. Two cables with loss similar to that given in Appendix C were used to connect the filter and spectrum analyser to the output of the synthesiser.

The wideband SFDR is quite good. For an output frequency of 7.47 GHz the SFDR is just less than 50 dB. The second harmonics are well suppressed by the output filter and are well within specification. Note however that for an output frequency of 6.47 GHz, the third harmonic at 19.41 GHz falls

into the secondary passband of the interdigital filter and is about 42 dB below the carrier. In reality, the suppression is somewhat less due to the increase in loss of the cables at higher frequencies.

Spectral measurements at various other output frequencies were performed. In general, both the close-in and wideband spurious performance was found to be within specification. The reader is referred to Appendix C for a variety of other spectral measurements.

At some output frequencies within the 5.47 – 7.47 GHz band however, spurious components close to the carrier were found to be unacceptably high. Figure 8.9 shows the frequency synthesiser programmed to 6.01 GHz with $N = 8$. The DDS frequency is equal to 248.75 MHz which is the same as that used for evaluation of the quadrature modulator in Chapter 7. These high levels of spurs are unsuspected. Recall from Chapter 7 that the spurs at 5 MHz offset for $I/Q = 0$ dBm was predicted to be 66 dB lower than the carrier. Figure 8.9 shows that the spurs at 5 MHz offset are only -15.59 dBc.

To determine the cause of the high levels of spurious components observed, an open loop investigation was performed. Figure 8.10 shows the spectrum measured at the output of the quadrature modulator. The VCO was set to 6.01 GHz using a DC source. The output power in the USB is -3.62 dBm, close to -5 dBm as expected for an I/Q channel power of 0 dBm. The spur at 5 MHz offset is 60.98 dB below the carrier, close to the -62 dBc obtained in the previous chapter.

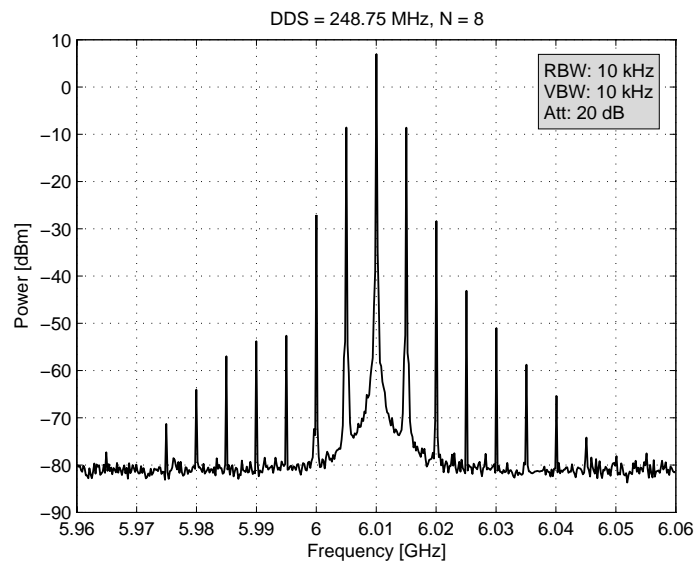


Figure 8.9: Spurious performance for an output frequency of 6.01 GHz, with $N = 8$.

Figure 8.11 shows a wideband measurement for the same conditions. The expected IM products similar to that of Chapter 7 can again be identified. The most significant IM product is the LSB at $751.25 - 248.75 = 502.5$ MHz, which is 14.08 dB lower compared to the USB. Although the frequency spectrum contains a lot of undesired spurs, they lie far outside the loop bandwidth of the PLL and are suppressed to the output by the response of the loop.

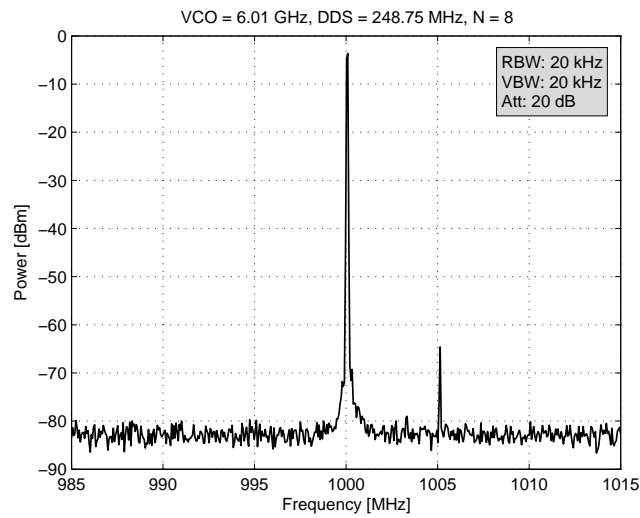


Figure 8.10: Frequency content measured at the output of the quadrature modulator.

To investigate whether spurs outside the loop bandwidth of the PLL influence the overall close-in spurious performance of the synthesiser, a bandpass filter was inserted between the quadrature modulator and PFD. A *Mini-Circuits* lowpass filter and custom built highpass filter were cascaded to obtain a bandpass filter response. The frequency response of this bandpass filter measured on a *Rohde & Schwarz ZVB* vector network analyser is shown in Appendix C. The return loss in the passband is not very good, but for the purpose of the investigation was found to be adequate.

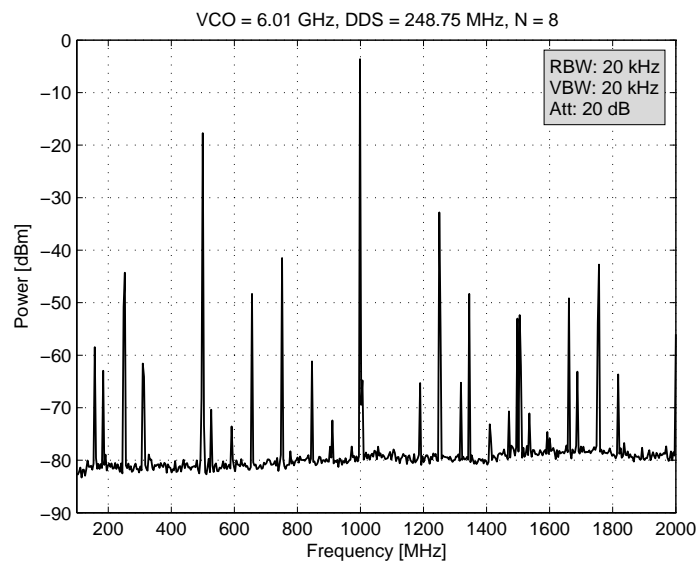


Figure 8.11: Wideband frequency content measured at the output of the quadrature modulator.

Figure 8.12 shows the spurious performance with the filter in place. Comparing Figure 8.9 to Figure 8.12 shows a major improvement in SFDR. The spurious components at 5 MHz offset are 62.38 dB below the carrier which is close the -66 dBc predicted in Chapter 7.

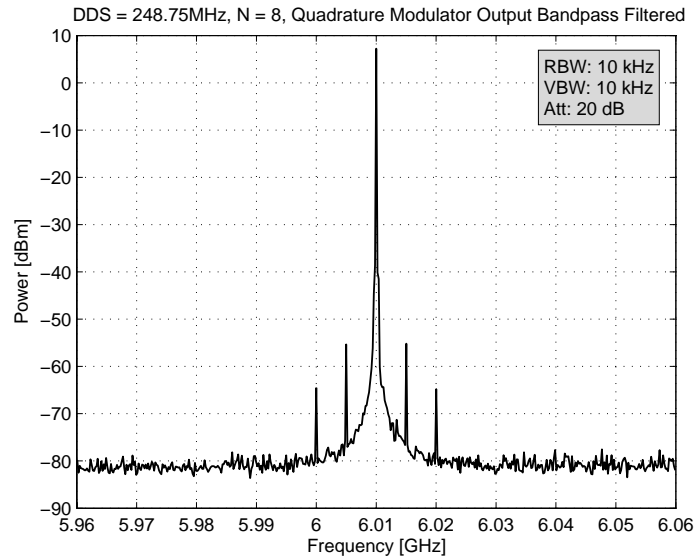


Figure 8.12: Close-in frequency content with the modulator output bandpass filtered.

From these measurements it is clear that spurs outside the loop bandwidth of the PLL affect the SFDR of the synthesiser at offset frequencies close to the carrier. Therefore, for future development, the addition of a bandpass filter between the modulator and PFD should be considered.

8.4 Frequency Synthesiser Transient Response

The transient response of the frequency synthesiser for a frequency jump from 5.47 GHz to 7.47 GHz is shown in Figure 8.13. The measurement was performed with an oscilloscope connected to the tuning port of the VCO.

The switching speed of the synthesiser is approximately $250 \mu\text{s}$ for $N = 8$, and about $300 \mu\text{s}$ for $N = 9$. This is much longer than the switching speed specification of $1 \mu\text{s}$. The long switching time is a result of the narrow loop bandwidth of the PLL which was chosen for optimal phase noise performance, not minimal switching speed.

8.5 Conclusion

In this chapter, measurements of the complete frequency synthesiser were presented and discussed. In the first section of the chapter the measured phase noise at both output frequencies was presented. The close correlation between the calculated and measured phase noise was shown and the primary objective of meeting the phase noise specification of Table 1.1 was achieved.

The SFDR of the synthesiser was found to be within specification for most output frequencies. How-

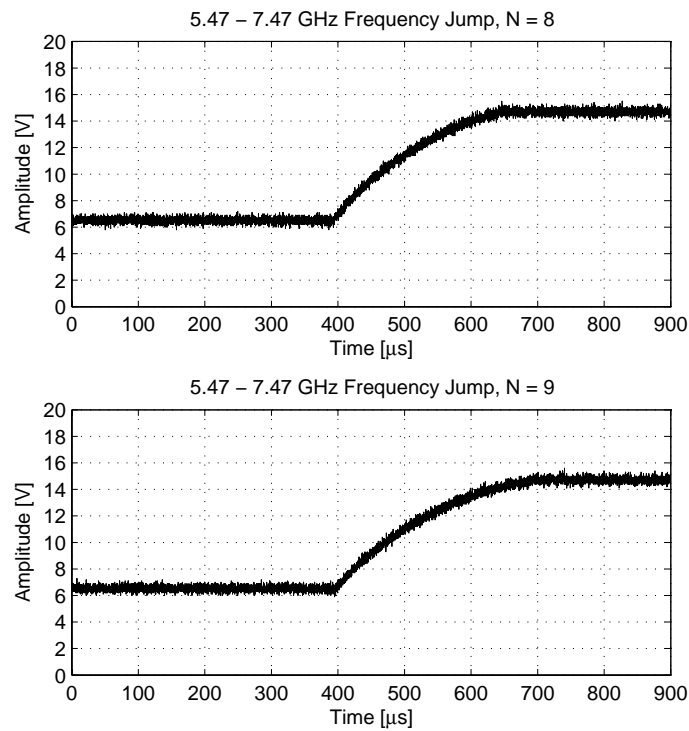


Figure 8.13: Transient response of the synthesiser for a frequency jump from 5.47 – 7.47 GHz.

ever, at some output frequencies spurious components were found to be unacceptably high. The cause of these high power spurs was investigated and it was found that the insertion of a bandpass filter between the modulator and PFD increased the SFDR to within specification.

In the final part of this chapter, the switching speed of the synthesiser was measured. Due to the narrow loop bandwidth of the PLL which was chosen for optimal phase noise performance, the switching speed was found to be out of specification.

Chapter 9

Conclusion and Recommendations

This thesis discussed the detail design, development and measured results of a low-noise PLL-based frequency synthesiser for coherent X-band Doppler radar. The primary objective of this research project was to exploit the recent advancement in PLL and DDS technology to design an indirect frequency synthesiser that could meet the phase noise specification of Table 1.1. This goal was achieved and measured phase noise levels equal to or lower than the specification were obtained.

In order to obtain optimal frequency synthesiser phase noise performance, a theoretical study of the noise contributions of individual components of the synthesiser and their effect on the total phase noise within and outside the loop bandwidth of the PLL, was conducted. The effect of different phase margins on the closed-loop frequency response of the PLL, and hence the overall phase noise of the synthesiser, was investigated. Based on the results, an optimal PFD reference frequency of 1 GHz, loop bandwidth of 1 MHz, adequate phase margin close to 70° and suitable components were chosen for optimal phase noise performance.

A significant part of this thesis was dedicated to the design, modelling and characterisation of a frequency multiplier and two bandpass filters required for the synthesiser. The design of the frequency multiplier was based on a piecewise linear SRD model. The theory presented by Johnston and Boothroyd was extended to the case where two SRDs in anti-parallel were considered. The large-signal driving point impedances of the nonlinear network were found using Fourier analysis and were matched to the source and load impedances using lumped element networks. It was seen that the anti-parallel combination of diodes yielded even-order harmonic suppression in excess of 30 dB. Through practical experimentation it was found that the addition of an idler at the third harmonic improved the response of the multiplier quite significantly, and conversion loss as low as 8.5 dB was obtained.

The theory of coupling coefficients and external quality factors was used for the design of the combine and interdigital bandpass filters. To aid in the verification and optimisation of the design, both filters were modelled in *CST*. The *CST* models proved useful for modelling practical aspects of the filters

not taken into account by theory. Excellent agreement between the simulated and measured response was obtained for the combline filter and hardly any change in bar spacings calculated with the *Matlab* design code was found necessary. For the interdigital bandpass filter, good agreement between the simulated and measured response was obtained. It was seen that some optimisation of the bar spacings in *CST* was required to obtain the desired frequency response.

The thesis culminated in the presentation of the measured phase noise of the complete frequency synthesiser in Chapter 8. Excellent agreement between the calculated and measured phase noise was obtained and it was shown that the phase noise specification of Table 1.1 could be met.

The close-in and wideband SFDR of the synthesiser was investigated and was found to be within specification for most of the evaluated output frequencies. In some cases however, high levels of spurious components close to the carrier were obtained. Closer investigation revealed that the inclusion of a bandpass filter between the output of the quadrature modulator and PFD input improved the SFDR to levels well within specification, proving that spurious components outside the loop bandwidth of the PLL has a direct influence on the close-in SFDR of the synthesiser. For future development, the inclusion of a bandpass filter between the quadrature modulator and PFD should be considered.

A considerable drop in the output power of the synthesiser was observed with increasing output frequency. The components causing the observed slope were identified and should for future use be replaced with components that have a flat frequency response over the band of interest. The design of the power divider used at the output of the VCO can be improved. Although the resistive power divider is inherently broadband, it offers no isolation between ports. For future development, the use of a Wilkinson power divider can be considered.

In total perspective, with the exception of the switching speed of the synthesiser, the PLL-based frequency synthesiser appears to be a feasible and suitable option for effectively operating as a low noise LO for coherent X-band Doppler radar.

Appendices

Appendix A

Mathematical Derivations and Computations

A.1 Series to Parallel Circuit Transformations

$$\begin{aligned} Y &= \frac{1}{Z} = \frac{1}{R_s + jX_s} \\ \therefore Y &= \frac{R_s - jX_s}{R_s^2 + X_s^2} = \frac{R_s}{R_s^2 + X_s^2} - j \frac{X_s}{R_s^2 + X_s^2} = G_p + jB_p \\ \therefore R_p &= \frac{1}{G_p} = \frac{R_s^2 + X_s^2}{R_s} = R_s \left(1 + \left(\frac{X_s}{R_s} \right)^2 \right) = R_s (1 + Q^2) \\ \therefore Q &= \pm \sqrt{\frac{R_p}{R_s} - 1} \end{aligned} \tag{A.1}$$

A.2 Calculating the Line Length for Phase Quadrature I and Q Channels

An arbitrary cable for the quadrature modulator measurements was chosen. Its length was measured as $\ell_1 = 51.5$ cm. To obtain a phase difference of 90° between this cable and another cable with length ℓ_2 , requires

$$\beta \ell_1 - \beta \ell_2 = \frac{2\pi \ell_1}{\lambda_2} - \frac{2\pi \ell_2}{\lambda_2} = \pm \frac{\pi}{2} \tag{A.2}$$

The wavelength in the medium of propagation, is related to the free-space wavelength and dielectric constant of the medium by

$$\lambda = \frac{\lambda_0}{\sqrt{\epsilon_r}} = \frac{c}{f \sqrt{\epsilon_r}} \tag{A.3}$$

Therefore, Equation A.2 can be expressed as

$$\frac{\ell_1}{\lambda_1} - \frac{\ell_2}{\lambda_2} = \frac{\ell_1 f \sqrt{\epsilon_{r1}}}{c} - \frac{\ell_2 f \sqrt{\epsilon_{r2}}}{c} = \pm \frac{1}{4} \tag{A.4}$$

Rearranging terms yields

$$\ell_2 = \pm \frac{c}{4f\sqrt{\epsilon_{r2}}} + \frac{\ell_1\sqrt{\epsilon_{r1}}}{\sqrt{\epsilon_{r2}}} \tag{A.5}$$

Substituting the values of $c = 2.997 \times 10^8 \text{ m/s}$, $f = 248.75 \text{ MHz}$, $\epsilon_{r1} = 2.08$, and $\epsilon_{r2} = 2.3$ into Equation A.5, yields

$$\ell_2 = 29.11 \text{ cm} \quad \text{or} \quad \ell_2 = 68.84 \text{ cm} \tag{A.6}$$

Note that the dielectric constant of the two cables differs.

A.3 Frequency Synthesiser Phase Noise with $N = 9$

Table A.1: Spreadsheet for calculating the overall phase noise at 5.47 GHz, with $N = 9$.

Element	Comment	Units	Frequency	Frequency Offset					
			MHz	100 Hz	1 kHz	10 kHz	100 kHz	1 MHz	10 MHz
Wenzel OCXO (501-14217)	Phase Noise	dBc/Hz	100	-120.00	-145.00	-160.00	-160.00	-160.00	-160.00
	Phase Noise at Output of PLL	dBc/Hz	5470	-85.24	-110.24	-125.24	-125.24	-125.24	-125.24
	Phase Noise at Input of PFD	dBc/Hz	683.75	-103.30	-128.30	-143.30	-143.30	-143.30	-143.30
AD9858 DDS	Phase Noise	dBc/Hz	103	-139.00	-148.00	-152.00	-152.00	-152.00	-150.00
	Phase Noise	dBc/Hz	403	-123.00	-132.00	-137.00	-140.00	-140.00	-139.00
	Interpolated Phase Noise	dBc/Hz	316.25	-125.84	-134.84	-139.67	-142.13	-142.13	-140.95
HMC497LP4 Quadrature Modulator	Noise Floor Relative To -5dBm Output	dBc/Hz		-156.00	-156.00	-156.00	-156.00	-156.00	-156.00
HMC437MS8G Frequency Divider (/3)	Phase Noise	dBc/Hz		-138.00	-146.00	-150.00	-152.00	-153.00	-153.00
HMC439QS16G PFD	Phase Noise	dBc/Hz	100	-144.00	-153.00	-153.00	-153.00	-151.00	-150.00
	Phase Noise	dBc/Hz	1280	-129.00	-140.00	-143.00	-143.00	-139.00	-141.00
	Interpolated Phase Noise	dBc/Hz	1000	-130.45	-141.26	-143.97	-143.97	-140.16	-141.87
	Total Phase Noise at PFD Input H(s)	dBc/Hz dB		-103.27 19.09	-127.19 19.09	-136.83 19.09	-138.04 19.52	-136.74 17.24	-137.00 -7.62
Phase Noise at Output of PLL		dBc/Hz		-84.18	-108.10	-117.74	-118.52	-119.50	-144.62
Loop Filter Resistor Noise (4xR _n)	4KTR	V ² /Hz		1.28E-17	1.28E-17	1.28E-17	1.28E-17	1.28E-17	1.28E-17
	H _{LF} (s) , Factor Kphi Smaller Than H(s)	dB		29.03	29.03	29.03	29.46	27.18	2.32
	Phase Noise at Output of PLL	rad ² /Hz		1.03E-14	1.03E-14	1.03E-14	1.13E-14	6.70E-15	2.19E-17
Phase Noise at Output of PLL		dBc/Hz		-142.90	-142.90	-142.90	-142.47	-144.75	-169.61
THS4032 Operational Amplifier	Current Noise Density	pA/sqrt(Hz)		3.60	1.60	1.25	1.20	1.20	1.20
	Equivalent Thevenin Voltage Noise Density	nV/sqrt(Hz)		2.88	1.28	1.00	0.96	0.96	0.96
	H _{LF} (s) , Factor Kphi Smaller Than H(s)	dB		29.03	29.03	29.03	29.46	27.18	2.32
	Voltage Noise Density	nV/sqrt(Hz)		3.62	1.90	1.50	1.40	1.35	1.35
	H _e (s)	dB		29.03	29.05	30.90	45.70	49.57	31.06
Phase Noise at Output of PLL	rad ² /Hz		1.71E-14	1.31E-15	8.00E-16	8.14E-16	4.82E-16	1.57E-18	
Phase Noise at Output of PLL		dBc/Hz		-140.68	-151.83	-153.98	-153.90	-156.18	-181.04
HMC586LC4B VCO	Phase Noise	dBc/Hz		-9.00	-43.00	-74.00	-97.00	-118.00	-139.00
	H _{VCO} (s)	dB		-143.88	-103.88	-63.89	-24.63	-0.70	0.34
Phase Noise at Output of PLL		dBc/Hz		-152.88	-146.88	-137.89	-121.63	-118.70	-138.66
Total Phase Noise at Output of PLL		dBc/Hz	5470	-84.18	-108.10	-117.69	-116.78	-116.07	-137.68

Table A.2: Spreadsheet for calculating the overall phase noise at 7.47 GHz, with $N = 9$.

Element	Comment	Units	Frequency MHz	Frequency Offset					
				100 Hz	1 kHz	10 kHz	100 kHz	1 MHz	10 MHz
Wenzel OCXO (501-14217)	Phase Noise	dBc/Hz	100	-120.00	-145.00	-160.00	-160.00	-160.00	-160.00
	Phase Noise at Output of PLL	dBc/Hz	7470	-82.53	-107.53	-122.53	-122.53	-122.53	-122.53
	Phase Noise at Input of PFD	dBc/Hz	933.75	-100.60	-125.60	-140.60	-140.60	-140.60	-140.60
AD9858 DDS	Phase Noise	dBc/Hz	103	-139.00	-148.00	-152.00	-152.00	-152.00	-150.00
	Phase Noise	dBc/Hz	403	-123.00	-132.00	-137.00	-140.00	-140.00	-139.00
	Interpolated Phase Noise	dBc/Hz	66.25	-144.18	-153.18	-156.85	-155.88	-155.88	-153.56
HMC497LP4 Quadrature Modulator	Noise Floor Relative To -5dBm Output	dBc/Hz		-156.00	-156.00	-156.00	-156.00	-156.00	-156.00
HMC437MS8G Frequency Divider (/3)	Phase Noise	dBc/Hz		-138.00	-146.00	-150.00	-152.00	-153.00	-153.00
HMC439QS16G PFD	Phase Noise	dBc/Hz	100	-144.00	-153.00	-153.00	-153.00	-151.00	-150.00
	Phase Noise	dBc/Hz	1280	-129.00	-140.00	-143.00	-143.00	-139.00	-141.00
	Interpolated Phase Noise	dBc/Hz	1000	-130.45	-141.26	-143.97	-143.97	-140.16	-141.87
	Total Phase Noise at PFD Input H(s)	dBc/Hz dB		-100.59 19.09	-125.43 19.09	-138.48 19.09	-138.58 19.52	-137.13 17.24	-137.85 -7.62
Phase Noise at Output of PLL		dBc/Hz		-81.50	-106.34	-119.39	-119.06	-119.89	-145.47
Loop Filter Resistor Noise (4xR_n)	4kTR	V ² /Hz		1.28E-17	1.28E-17	1.28E-17	1.28E-17	1.28E-17	1.28E-17
	H _{LF} (s) , Factor Kphi Smaller Than H(s)	dB		29.03	29.03	29.03	29.46	27.18	2.32
	Phase Noise at Output of PLL	rad ² /Hz		1.03E-14	1.03E-14	1.03E-14	1.13E-14	6.70E-15	2.19E-17
Phase Noise at Output of PLL		dBc/Hz		-142.90	-142.90	-142.90	-142.47	-144.75	-169.61
THS4032 Operational Amplifier	Current Noise Density	pA/sqrt(Hz)		3.60	1.60	1.25	1.20	1.20	1.20
	Equivalent Thevenin Voltage Noise Density	nV/sqrt(Hz)		2.88	1.28	1.00	0.96	0.96	0.96
	H _{LF} (s) , Factor Kphi Smaller Than H(s)	dB		29.03	29.03	29.03	29.46	27.18	2.32
	Voltage Noise Density	nV/sqrt(Hz)		3.62	1.90	1.50	1.40	1.35	1.35
	H _e (s)	dB		29.03	29.05	30.90	45.70	49.57	31.06
Phase Noise at Output of PLL	rad ² /Hz			1.71E-14	1.31E-15	8.00E-16	8.14E-16	4.82E-16	1.57E-18
Phase Noise at Output of PLL		dBc/Hz		-140.68	-151.83	-153.98	-153.90	-156.18	-181.04
HMC586LC4B VCO	Phase Noise	dBc/Hz		-9.00	-43.00	-74.00	-97.00	-118.00	-139.00
	H _{VCO} (s)	dB		-143.88	-103.88	-63.89	-24.63	-0.70	0.34
Phase Noise at Output of PLL		dBc/Hz		-152.88	-146.88	-137.89	-121.63	-118.70	-138.66
Total Phase Noise at Output of PLL		dBc/Hz	7470	-81.50	-106.34	-119.31	-117.13	-116.24	-137.83

Appendix B

Matlab Code

B.1 Frequency Multiplier Design Code

```
close all
clear all
clc

f=200e6;
T=1/f;
w=2*pi*f;

m=2;
n=5;
VDC=10.4;
Vlam=0.8;
VT=VDC/2+Vlam;
Cp=2e-12;
Cd=1e-12;
CT=Cp+2*Cd;
k=1;
%Integral boundaries valid for m=1 and m=2.
l0=0;
l1=(m*T)/(2*n);
l2=T/2-(m*T)/(2*n);
l3=T/2;
%
syms t
```

```

I1=(-VT*CT*w)/cos(m*pi/n);
In=k*I1*sin(m*pi/n);
i=I1*sin(w*t)+In*cos(n*w*t);
q=(-I1/w)*cos(w*t)+(In/(n*w))*sin(n*w*t);

V1I=(4/T)*(int(VT*sin(w*t),t,l0,l1)+int((q/CT)*sin(w*t),t,l1,l2)+...
    int(-VT*sin(w*t),t,l2,l3))
V1Q=(4/T)*(int(VT*cos(w*t),t,l0,l1)+int((q/CT)*cos(w*t),t,l1,l2)+...
    int(-VT*cos(w*t),t,l2,l3))

VnI=(4/T)*(int(VT*cos(n*w*t),t,l0,l1)+int((q/CT)*cos(n*w*t),t,l1,l2)+...
    int(-VT*cos(n*w*t),t,l2,l3))
VnQ=(4/T)*(int(VT*sin(n*w*t),t,l0,l1)+int((q/CT)*sin(n*w*t),t,l1,l2)+...
    int(-VT*sin(n*w*t),t,l2,l3))

R1=abs(V1I/I1)
X1=-abs(V1Q/I1)

Rn=abs(VnI/In)
Xn=-abs(VnQ/In)

```

B.2 Comblin Filter Design Code

```

close all;
clear all;
clc;

n = input('Low pass prototype order: ');
th_0 = input('Electrical length of resonators at resonance (degrees): ');
s11 = input('Maximum passband reflection coefficient (dB): ');

if s11 >= 0
s11 = -s11;
end

f0 = input('Centre frequency of bandpass filter (MHz): ');
bandwidth = input('Ripple bandwidth of bandpass filter (MHz): ');
ep_spacing = input('Earth plane spacing (mm): ');

```



```

t = input('Bar thickness (mm): ');
w = input('Inner resonator bar width (mm): ');

Widths = ones(1,n+2)*w;
w = input('Input line bar width (mm): ');
Widths(1) = w; Widths(n+2) = w;
x_end = input('End bar (input line) spacing from sidewall (mm): ');

QKQ = chebkq(n,s11);
QKQ(1) = (QKQ(1)*f0)/bandwidth;
QKQ(n+1) = QKQ(1);

for i = 2:n
QKQ(i) = (QKQ(i)*bandwidth)/f0;
end

S = Widths(2)*linspace(1,1,n+1);
S(1) = S(1)/3;
S(n+1) = S(n+1)/3;

QKQFil = CalcKQ_CL(n,S,t,Widths,ep_spacing,x_end,th_0);
inv_grad = (1.05*S-.95*S)./...
(CalcKQ_CL(n,1.05*S,t,Widths,ep_spacing,x_end,th_0)-...
CalcKQ_CL(n,.95*S,t,Widths,ep_spacing,x_end,th_0));
DeltaS = inv_grad.*(QKQ-QKQFil);
NormStep = sqrt(DeltaS*DeltaS');
S = S+0.3*DeltaS;
count=0;

while NormStep > ep_spacing/10000
count = count+1;
QKQFil = CalcKQ_CL(n,S,t,Widths,ep_spacing,x_end,th_0);
inv_grad = (1.05*S - .95*S)./...
(CalcKQ_CL(n,1.05*S,t,Widths,ep_spacing,x_end,th_0)-...
CalcKQ_CL(n,.95*S,t,Widths,ep_spacing,x_end,th_0));
DeltaS = inv_grad.*(QKQ-QKQFil);
NormStep = sqrt(DeltaS*DeltaS');
S = S + DeltaS;
end

```

```

disp('-----*****-----')
disp(['Dimensions determined after ',num2str(count),' refinements'])
disp('Spacing between bars (mm)')
S
S1 = S;
ok = input('Do you want to round the spacings? y to round, n to finish '...
    , 's');
while ok == 'y'
for i = 1:n+1
disp(['S(',num2str(i),') = ',num2str(S(i))])
S1(i) = input('Input rounded value: ')
end
QKQrounded = CalcKQ_CL(n,S1,t,Widths,ep_spacing,x_end,th_0);
Error = 100*(QKQrounded-QKQ)./QKQ;
disp('Percentage errors after rounding, Q1, K12, K23...Qn')
Error
ok = input('Not satisfied? y to round again, n to end ', 's');
end
disp('Bar capacitances (Farads):')
Cmat = CalcC(n,S1,t,Widths,ep_spacing,x_end)
disp('Bar transmission line characteristic impedances (Ohm):')
Z = 376.7*(Cmat.^-1)
TuneCaps = TCaps(50,n,Cmat,th_0,f0);
disp('Tuning capacitors (Farads):')
TuneCaps
FilterInnerWidth = sum(Widths)+2*x_end+sum(S1);
disp('Filter inner width (mm):')
FilterInnerWidth
CavityLength = (75000/f0)*(th_0/90);
disp('Cavity length (mm):')
CavityLength
%-----

% Reference: G.L. Matthaei, L. Young, E.M.T. Jones,
% "Microwave Filters, Impedance Matching Networks and Coupling Structures",
% McGraw-Hill, Inc., 1964, pp 99
function kq = chebkq(n,MaxRef1)
    S11=10^(MaxRef1/20);
    Lar=-10*log10(1-S11^2);
    Beta=log(coth(Lar/17.37));
    Sigma=sinh(Beta/(2*n));

```

```

g0=1;
for i=1:n+1
    ak=sin(((2*i-1)*pi)/(2*n));
    bk=Sigma^2+sin(i*pi/n)^2;
    if i==1
        g(i)=2*ak/Sigma;
    elseif (i~=1)&(i~=n+1)
        g(i)=(4*akmin1*ak)/(bkmin1*gkmin1);
    else
        if mod(n,2)==0
            g(i)=coth(Beta/4)^2;
        else
            g(i)=1;
        end
    end
    end
    akmin1=ak;
    bkmin1=bk;
    gkmin1=g(i);
end

g=[g0,g];

for i=1:n+1
    if (i==1)
        kq(i)=g(i+1);
    elseif(i==n+1)
        kq(i)=kq(1);
    else
        kq(i)=1/sqrt(g(i)*g(i+1));
    end
end
end
%-----

% Function to calculate combine K & Q values from physical data
function QKQ = CalcKQ_CL(n,S,t,W,b,x_end,th_0);
% S contains the n+1 spacings between the n+2 bars
% C contains n+2 rows of data, cl, cg, cr for each bar.
C=[];
C = cBar(W(1),t,b,2*x_end,S(1));

```

```

for i = 2:n+1
C = [C;cBar(W(i),t,b,S(i-1),S(i))];
end
C = [C;cBar(W(n+2),t,b,S(n+1),2*x_end)];
QKQ = [1:n+1];
QKQ(1) = Qext_CL(50,2*C(1,1)+C(1,2),C(1,3),C(2,2),C(2,3),th_0);
QKQ(n+1) =QKQ(1);
QKQ(2) = K12_CL(n,50,2*C(1,1)+C(1,2),C(1,3),C(2,2),C(2,3),C(3,2),...
          C(3,3),th_0);
QKQ(n) = QKQ(2);
for i = 3:n-1
QKQ(i) = Kmn_CL(C(i,1),C(i,2),C(i,3),C(i+1,2),C(i+1,3),th_0);
end
end
%-----

% Calculates the capacitances (C/eps values) for parallel coupled bars
% Reference: S.M. Perlow, "Analysis of Edge-Coupled Shielded
% Strip and Slabline Structures",
% IEEE Transactions on Microwave Theory and Techniques
% vol. 35, no. 5, pp 522 - 529, May 1987.
function C = cBar(w, t, b, sl, sr)
if ((nargin < 5) || (nargin > 5))
error ('usage: cBar(w, t, b, sl, sr)');
end

cpar = Cp(w,t,b);
cfel = Cfe(sl,t,b);
cfer = Cfe(sr,t,b);
C = [];
C(1) = Cc(sl,t,b);
C(2) = 2*(cpar+cfel+cfer);
C(3) = Cc(sr,t,b);
end

function a = A(s,t,b)
if (s/b) < 0.30
a = 1.0+2.13507*(t/b)*exp(-0.57518*log(s/b));
else
a = 1.0+3.89531*(t/b)*exp(-0.11467*log(s/b));

```

```

    end
end

function b = B(s,t,b)
if ((t/b) <= 0.5636)
if ((s/b) < 0.08)
b = -(0.2933+3.333*s/b)*t/b;
else
b = -(0.56)*t/b;
    end
else
if ((s/b) < 0.08)
b = -0.1653-5.6814*(s/b)+6.7475*(s/b)*(t/b);
else
b = -0.62+0.54*(t/b);
    end
    end
end

function c = Cp(w,t,b)
wc0 = 2*log(2)/pi+(w/b)-1/((2/pi)*log(abs(2*coth(pi*w/(4*b)))));
if ~(((w*t)/(b*b)) > 0.015) | (w/b > 0.4)
weff = w-b*(wc0*(1.0-Sqrt(w*t/(b*b)/0.015))^2)
else
weff = w;
    end
    c = 2*weff/(b-t);
end

function c = Cc(s,t,b)
c = 2*A(s,t,b)*log(coth(pi*s/(2*b)))/pi;
end

function c = Cfe(s,t,b)
cfeo = A(s,t,b)*(s/b-2*log(cosh(pi*s/(2*b)))/pi)+B(s,t,b);
if s/b > 1
cfeo = (Cf(t,b)-cfeo)*(1-exp(-4*(s/b-1)))+cfeo;
    end
c = cfeo;
end

```

```

function c = Cf(t,b)
tb = 1/(1-t/b);
c = (2*tb*log(tb+1)-(tb-1)*log((tb)^2-1))/pi;
end
%-----

% Computes the external quality factors of the first (and last) resonators
function Q = Qext_CL(Rg,c0,c01,c1,c12,th_0)
n = c01/(c01+c0);
yterm = (n*c01/376.7)*(c01/376.7*j*tan(th_0*pi/180)+(n/Rg))/...
        (c01/376.7+j*tan(th_0*pi/180)*n/Rg);
gt = real(yterm);
bt = imag(yterm);
slopefactor = (cot(th_0*pi/180)+th_0*(pi/180)/sin(th_0*pi/180)^2)/2;
Q = slopefactor*1/gt*((n*c0+c1+c12)/376.7);
end
%-----

% Evaluates the coupling between first and second resonators
function k = K12_CL(n,Rg,c0,c01,c1,c12,c2,c23,th_0)
n1 = c01/(c0+c01);
slopefactor = (cot(th_0*pi/180)+th_0*(pi/180)/sin(th_0*pi/180)^2)/2;
if n > 2
    k = (1/slopefactor)*c12*cot(th_0*pi/180)/...
        sqrt((n1*c0+c1+c12)*(c12+c2+c23));
else
k = (1/slopefactor)*c12*cot(th_0*pi/180)/(n1*c0+c1+c12);
end
end
%-----

% Calculates the coupling coefficients between inner lines
function k = Kmn_CL(cml,cm,cmn,cn,cnr,th_0)
slopefactor = (cot(th_0*pi/180)+(th_0*pi/180)/sin(th_0*pi/180)^2)/2;
k = (1/slopefactor)*cmn*cot(th_0*pi/180)/...
    sqrt((cml+cm+cmn)*(cmn+cn+cnr));
end
%-----

% Calculates the bar capacitances of n+2 parallel bars

```

```

function C = CalcC(n,S,t,W,b,x_end)
C=[];
C = cBar(W(1),t,b,2*x_end,S(1));
for i = 2:n+1
C = [C;cBar(W(i),t,b,S(i-1),S(i))];
end
C = [C;cBar(W(n+2),t,b,S(n+1),2*x_end)];
C(1,2) = C(1,2)+2*C(1,1);
C(1,1) = 0;
C(n+2,2) = C(n+2,2)+2*C(n+2,3);
C(n+2,3) = 0;
end
%-----

% Function to calculate the tuning capacitors
function TC = TCaps(Rg,n,C,th_0,f0);
    n1 = C(1,3)/(C(1,2) + C(1,3));
yterm = n1*C(1,3)/376.7*(C(1,3)/376.7*j*tan(th_0*pi/180)+n1/Rg)/...
(C(1,3)/376.7+j*tan(th_0*pi/180)*n1/Rg);
gt = real(yterm);
bt = imag(yterm);
disp(['Redundant input line characteristic impedance: ',...
    num2str(376.7*n1/C(1,3)), ' Ohm'])
disp(['Transformed load admittance: ',num2str(gt),' + j ',...
    num2str(bt),' S'])
TC = [1:n];
TC(1) = (((n1*C(1,2)+C(2,2)+C(2,3))/376.7)*...
    cot(th_0*pi/180)-bt)/(2*pi*f0*10^6);
for i = 3:n
TC(i-1) = (C(i,1)+C(i,2)+C(i,3))*...
    cot(th_0*pi/180)/(376.7*2*pi*f0*10^6);
    end
TC(n) = TC(1);
end

```

B.3 Interdigital Filter Design Code

```

close all
clear all
clc

n = input('Low pass prototype order: ');
s11 = input('Max passband reflection coefficient (dB): ');

if s11 >= 0
s11 = -s11;
end

f0 = input('Centre frequency of bandpass filter (MHz): ');
bandwidth = input('Ripple bandwidth of bandpass filter (MHz): ');
ep_spacing = input('Earth plane spacing (mm): ');
t = input('Bar thickness (mm): ');
w = input('Inner resonator bar widths (mm): ');

Widths = ones(1,n+2)*w;
w = input('Input line bar widths (mm): ');
Widths(1) = w; Widths(n+2) = w;
x_end = input('End bar (input line) spacing from sidewall (mm): ');

QKQ = chebkq(n,s11);
QKQ(1) = QKQ(1)*f0/bandwidth;
QKQ(n+1) = QKQ(1);

for i = 2:n
QKQ(i) = QKQ(i)*bandwidth/f0;
end

S = Widths(2)*linspace(1,1,n+1);
S(1) = S(1)/3;
S(n+1) = S(n+1)/3;
QKQFil = CalcKQ(n,S,t,Widths,ep_spacing,x_end);

inv_grad = (1.05*S - .95*S)./...
(CalcKQ(n,1.05*S,t,Widths,ep_spacing,x_end)-CalcKQ(n,.95*S,t,Widths,...
ep_spacing,x_end));

```



```

DeltaS = inv_grad.*(QKQ-QKQFil);
NormStep = sqrt(DeltaS*DeltaS');
S = S + 0.3*DeltaS;
count=0;

while NormStep > ep_spacing/10000
count = count + 1;
QKQFil = CalcKQ(n,S,t,Widths,ep_spacing,x_end);
inv_grad = (1.05*S - .95*S)./...
(CalcKQ(n,1.05*S,t,Widths,ep_spacing,x_end)-...
CalcKQ(n,.95*S,t,Widths,ep_spacing,x_end));
DeltaS = inv_grad.*(QKQ-QKQFil);
NormStep = sqrt(DeltaS*DeltaS');
S = S + DeltaS;
end

disp('-----*****-----')
disp(['Dimensions determined after ',num2str(count),' refinements'])
disp('Spacing between bars ')
S
S1 = S;
ok = input('Do you want to round the spacings? y to round, n to finish '...
,'s');

while ok == 'y'
for i = 1:n+1
disp(['S(',num2str(i),') = ',num2str(S(i))])
S1(i) = input('Input rounded value: ')
end

QKQrounded = CalcKQ(n,S1,t,Widths,ep_spacing,x_end);
Error = 100*(QKQrounded-QKQ)./QKQ;
disp('Percentage errors after rounding, Q1, K12, K23...Qn')
Error
ok = input('Not satisfied? y to round again, n to end ', 's');
end

FilterInnerWidth = sum(Widths) + 2*x_end + sum(S1)
CavityLength = 75000/f0
C = CalcC(n,S1,t,Widths,ep_spacing,x_end);

```

```

disp('Bar capacitances')
C
disp('Bar characteristic impedances')
Z = 376.7*(C.^-1)
%-----

% Reference: G.L. Matthaei, L. Young, E.M.T. Jones,
% "Microwave Filters, Impedance Matching Networks and Coupling Structures",
% McGraw-Hill, Inc., 1964, pp 99
function kq = chebkq(n,MaxRefl)
    S11=10^(MaxRefl/20);
    Lar=-10*log10(1-S11^2);
    Beta=log(coth(Lar/17.37));
    Sigma=sinh(Beta/(2*n));

    g0=1;
    for i=1:n+1
        ak=sin(((2*i-1)*pi)/(2*n));
        bk=Sigma^2+sin(i*pi/n)^2;
        if i==1
            g(i)=2*ak/Sigma;
        elseif (i~=1)&(i~=n+1)
            g(i)=(4*akmin1*ak)/(bkmin1*gkmin1);
        else
            if mod(n,2)==0
                g(i)=coth(Beta/4)^2;
            else
                g(i)=1;
            end
        end
        akmin1=ak;
        bkmin1=bk;
        gkmin1=g(i);
    end

    g=[g0,g];

    for i=1:n+1
        if (i==1)
            kq(i)=g(i+1);
        elseif(i==n+1)

```

```

        kq(i)=kq(1);
    else
        kq(i)=1/sqrt(g(i)*g(i+1));
    end
end
end
%-----

function QKQ = CalcKQ(n,S,t,W,b,x_end);
% S contains the n+1 spacings between the n+2 bars
% C contains n+2 rows of data, cl, cg, cr for each bar.
C=[];
C = cBar(W(1),t,b,2*x_end,S(1));
for i = 2:n+1
C = [C;cBar(W(i),t,b,S(i-1),S(i))];
end
C = [C;cBar(W(n+2),t,b,S(n+1),2*x_end)];
QKQ = [1:n+1];
QKQ(1) = Qext(50,2*C(1,1)+C(1,2),C(1,3),C(2,2),C(2,3));
QKQ(n+1) =QKQ(1);
QKQ(2) = K12(n,2*C(1,1)+C(1,2),C(1,3),C(2,2),C(2,3),C(3,2),C(3,3));
QKQ(n) = QKQ(2);
for i = 3:n-1
QKQ(i) = Kmn(C(i,1),C(i,2),C(i,3),C(i+1,2),C(i+1,3));
    end
end
%-----

% Calculates the capacitances (C/eps values) for parallel coupled bars
% Reference: S.M. Perlow, "Analysis of Edge-Coupled Shielded
% Strip and Slabline Structures",
% IEEE Transactions on Microwave Theory and Techniques
% vol. 35, no. 5, pp 522 - 529, May 1987.
function C = cBar(w,t,b,sl,sr)

if ((nargin < 5) || (nargin > 5))
error ('usage: cBar(w, t, b, sl, sr)');
    end

```

```

cpar = Cp(w,t,b);
cfel = Cfe(sl,t,b);
cfer = Cfe(sr,t,b);
C = [];
C(1) = Cc(sl,t,b);
C(2) = 2*(cpar+cfel+cfer);
C(3) = Cc(sr,t,b);
end

```

```

function a = A(s,t,b)
if (s/b) < 0.30
a = 1.0+2.13507*(t/b)*exp(-0.57518*log(s/b));
else
a = 1.0+3.89531*(t/b)*exp(-0.11467*log(s/b));
end
end

```

```

function b = B(s,t,b)
if ((t/b) <= 0.5636)
if ((s/b) < 0.08)
b = -(0.2933+3.333*s/b)*t/b;
else
b = -(0.56)*t/b;
end
else
if ((s/b) < 0.08)
b = -0.1653-5.6814*(s/b)+6.7475*(s/b)*(t/b);
else
b = -0.62+0.54*(t/b);
end
end
end

```

```

function c = Cp(w,t,b)
wc0 = 2*log(2)/pi+(w/b)-1/((2/pi)*log(abs(2*coth(pi*w/(4*b)))));
if ~(((w*t)/(b*b))>0.015)|(w/b>0.4)
weff = w-b*(wc0*(1.0-Sqrt(w*t/(b*b)/0.015))^2)
else
weff = w;
end

```

```
c = 2*weff/(b-t);
end
```

```
function c = Cc(s,t,b)
c = 2*A(s,t,b)*log(coth(pi*s/(2*b)))/(pi);
end
```

```
function c = Cfe(s,t,b)
```

```
cfeo = A(s,t,b)*(s/b-2*log(cosh(pi*s/(2*b)))/pi)+B(s,t,b);
if s/b > 1
cfeo = (Cf(t,b)-cfeo)*(1-exp(-4*(s/b-1)))+cfeo;
    end
c = cfeo;
end
```

```
function c = Cf(t,b)
tb = 1/(1-t/b);
c = (2*tb*log(tb+1)-(tb-1)*log((tb)^2-1))/pi;
end
```

```
%-----
```

```
% Computes the external quality factors
function Q = Qext(Rg,C_0,C_01,C_1,C_12)
n = C_01/(C_01+C_0);
Q = (pi*376.7*(n*C_0+C_1+C_12))/(4*Rg*C_01^2);
end
%-----
```

```
% Evaluates the coupling coefficients between first and second resonators
```

```
function k = K12(n,c0,c01,c1,c12,c2,c23)
n1 = c01/(c0+c01);
if n>2
    k = (4/pi)*c12/sqrt((n1*c0+c1+c12)*(c12+c2+c23));
else
k = (4/pi)*c12/(n1*c0+c1+c12);
end
end
%-----
```

```
% Calculates the coupling coefficients between inner lines
```

```

function k = Kmn(cml,cm,cmn,cn,cnr)
k = (4/pi)*cmn/sqrt((cml+cm+cmn)*(cmn+cn+cnr));
end
%-----

% Calculate the bar capacitances of n+2 parallel bars
function C = CalcC(n,S,t,W,b,x_end)
C=[];
C = cBar(W(1),t,b,2*x_end,S(1));
for i = 2:n+1
C = [C;cBar(W(i),t,b,S(i-1),S(i))];
end
C = [C;cBar(W(n+2),t,b,S(n+1),2*x_end)];
C(1,2) = C(1,2)+2*C(1,1);
C(1,1) = 0;
C(n+2,2) = C(n+2,2)+2*C(n+2,3);
C(n+2,3) = 0;
end
%-----

```

Appendix C

Various Measured Results

C.1 Loss of the Cables Used for the Frequency Multiplier

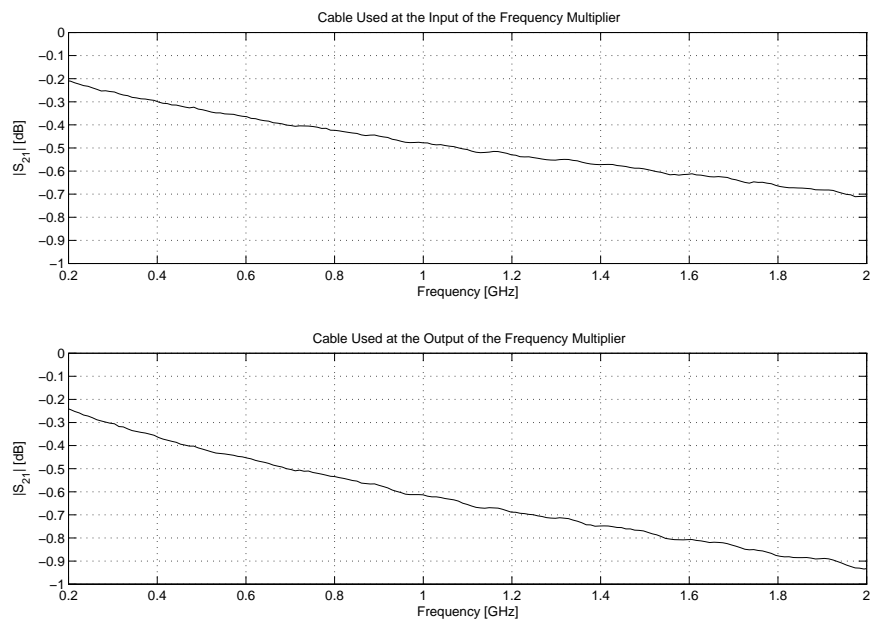


Figure C.1: Loss of the cables used for the frequency multiplier.

C.2 DDS Lowpass Filter Frequency Response

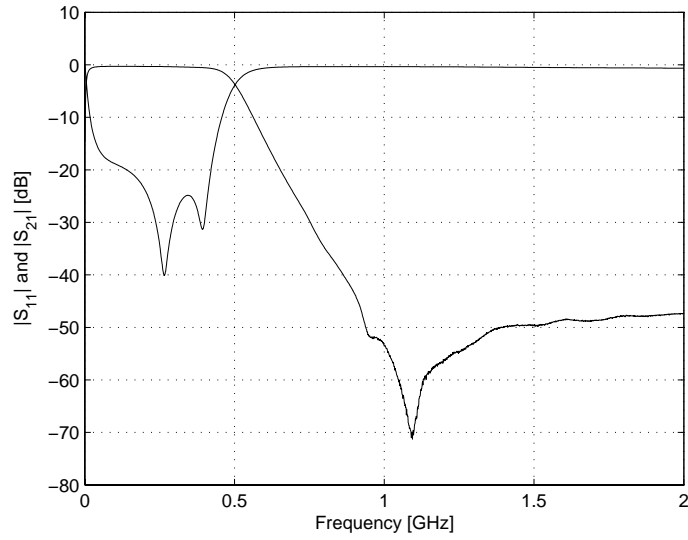


Figure C.2: S-parameters of the lowpass filter connected to the output of the DDS.

C.3 I and Q Channel Phase Relationship

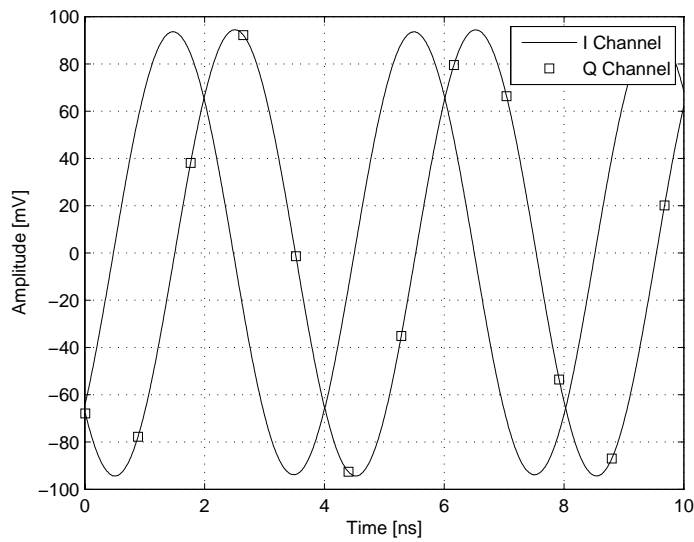


Figure C.3: Actual measured phase relationship between the I and Q channels.

C.4 Frequency Synthesiser Phase Noise

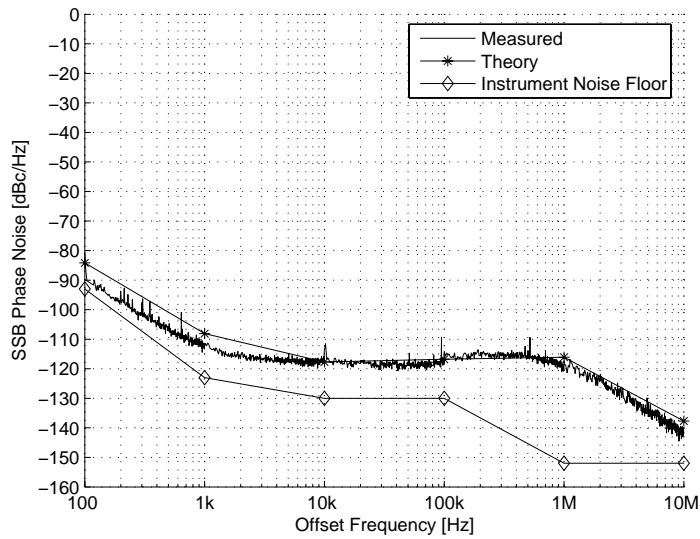


Figure C.4: Complete synthesiser phase noise at 5.47 GHz, with $N = 9$.

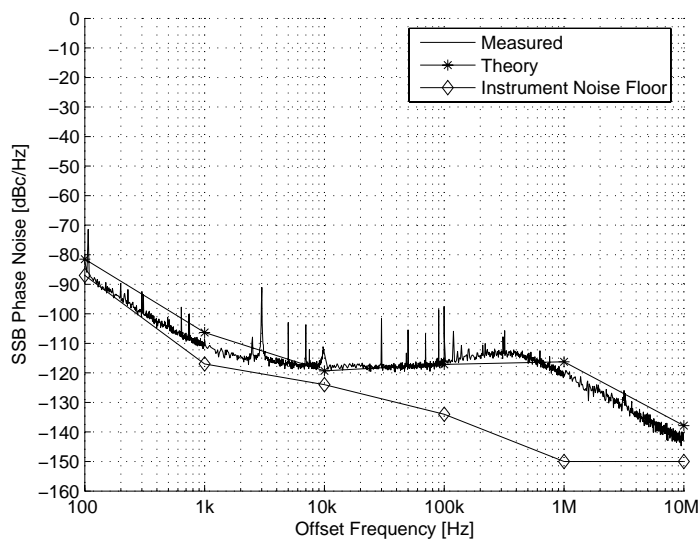


Figure C.5: Complete synthesiser phase noise at 7.47 GHz, with $N = 9$.

C.5 Loss of a Cable Similar to that Used at the Output of the Synthesiser

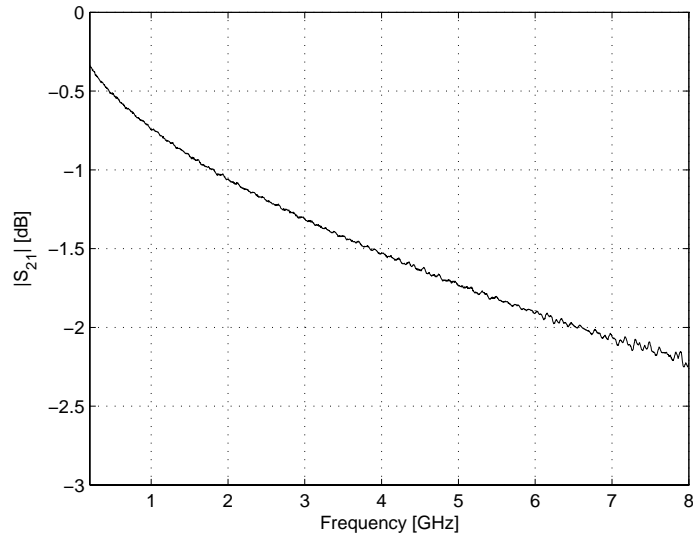


Figure C.6: Typical cable loss of a cable similar to that used to connect the synthesiser to the spectrum analyser.

C.6 Various Frequency Synthesiser SFDR Measurements

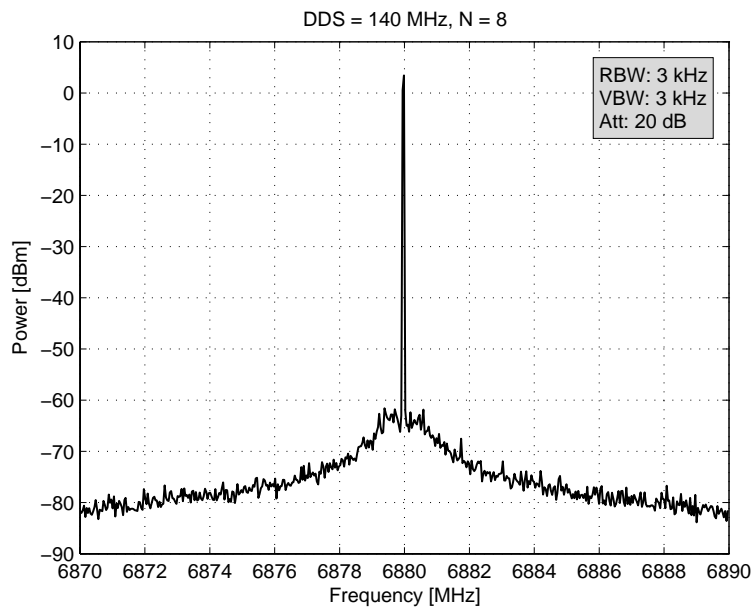


Figure C.7: Close-in frequency spectrum, with DDS = 140 MHz and N = 8.

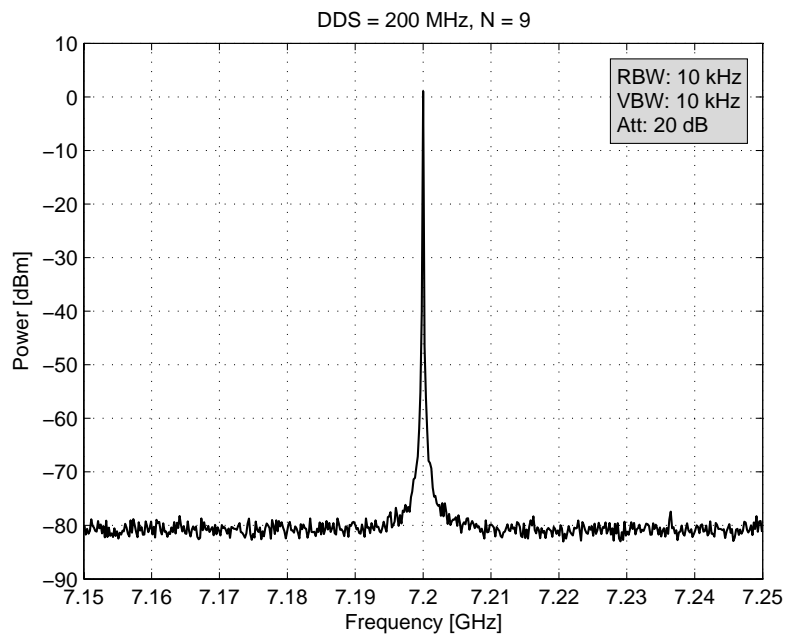


Figure C.8: Close-in frequency spectrum, with DDS = 200 MHz and $N = 9$.

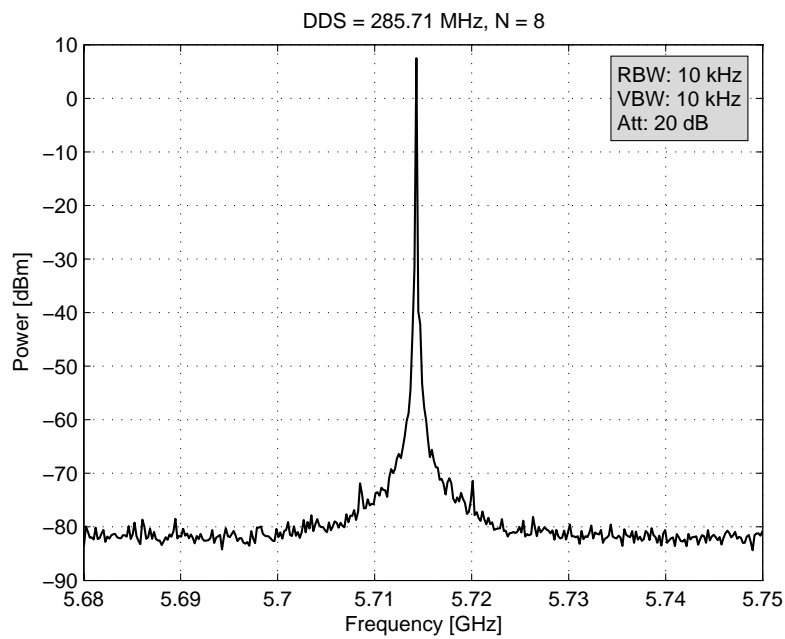


Figure C.9: Close-in frequency spectrum, with DDS = 285.71 MHz and $N = 8$.

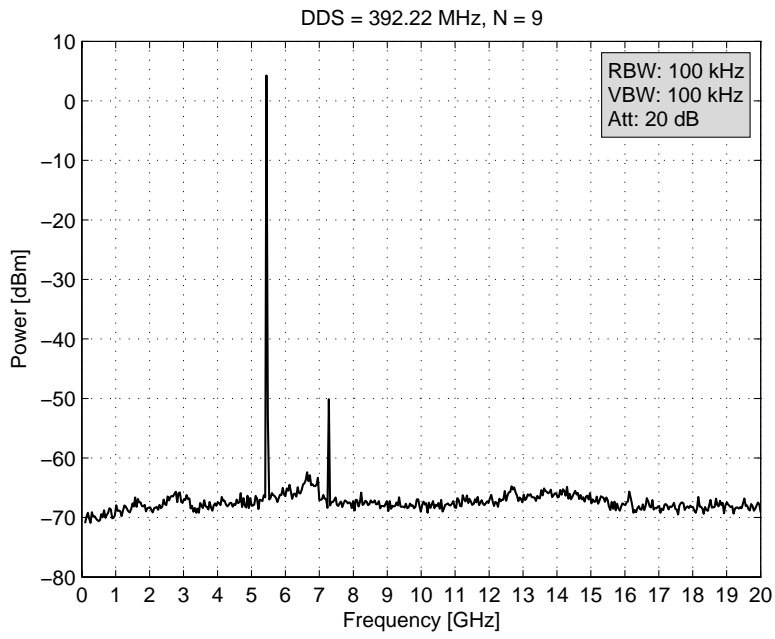


Figure C.10: Wideband frequency spectrum, with DDS = 392.22 MHz and $N = 9$.

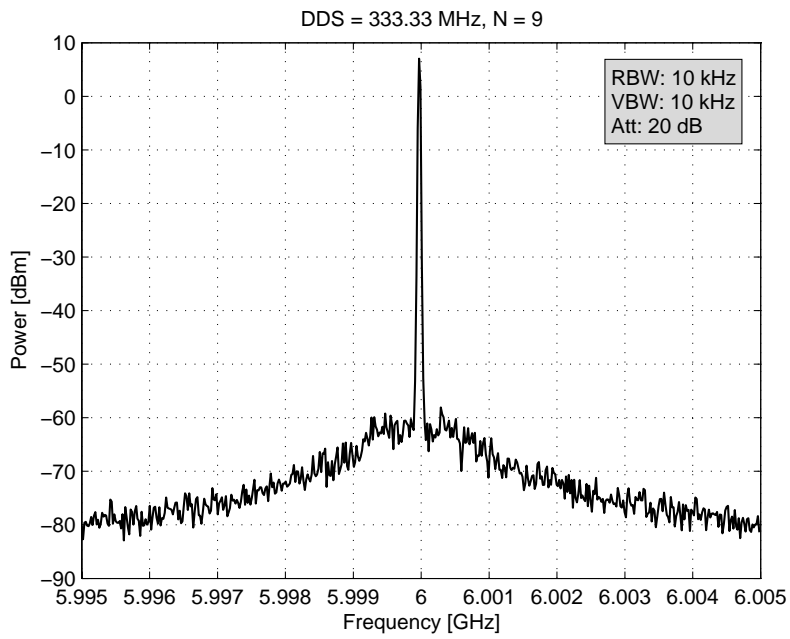


Figure C.11: Close-in frequency spectrum, with DDS = 333.33 MHz and $N = 9$.

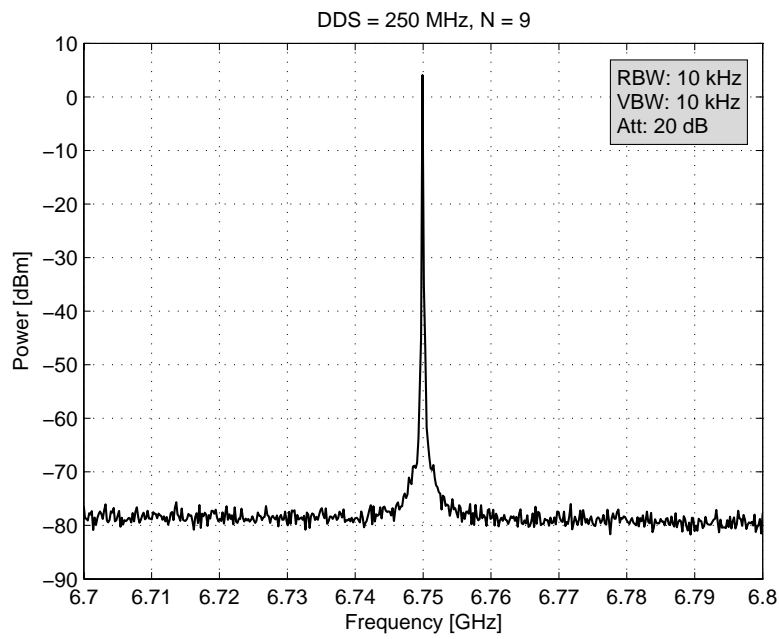


Figure C.12: Close-in frequency spectrum, with DDS = 250 MHz and $N = 9$.

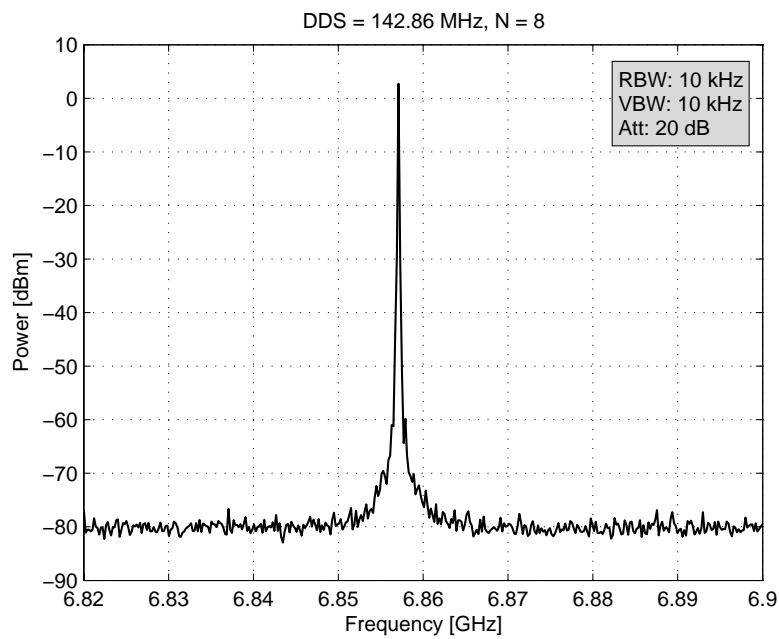


Figure C.13: Close-in frequency spectrum, with DDS = 142.86 MHz and $N = 8$.

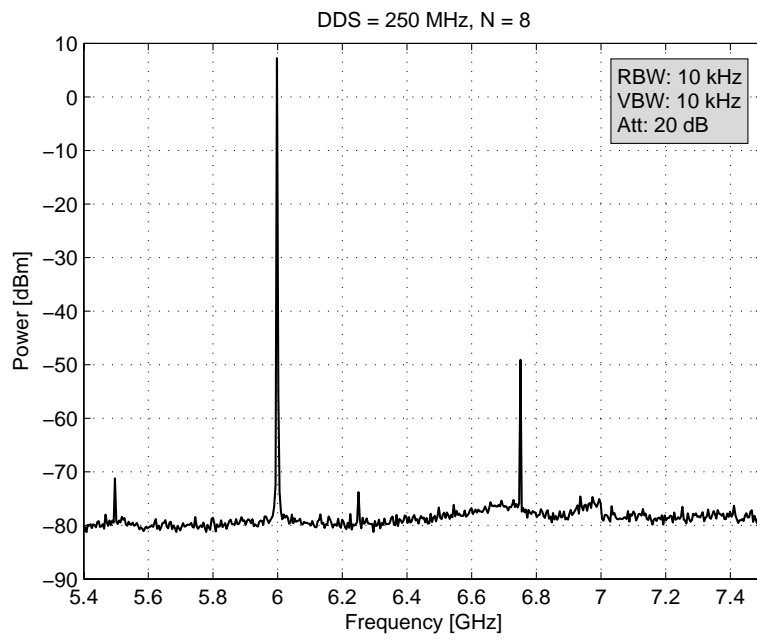


Figure C.14: Wideband frequency spectrum, with DDS = 250 MHz and $N = 8$.

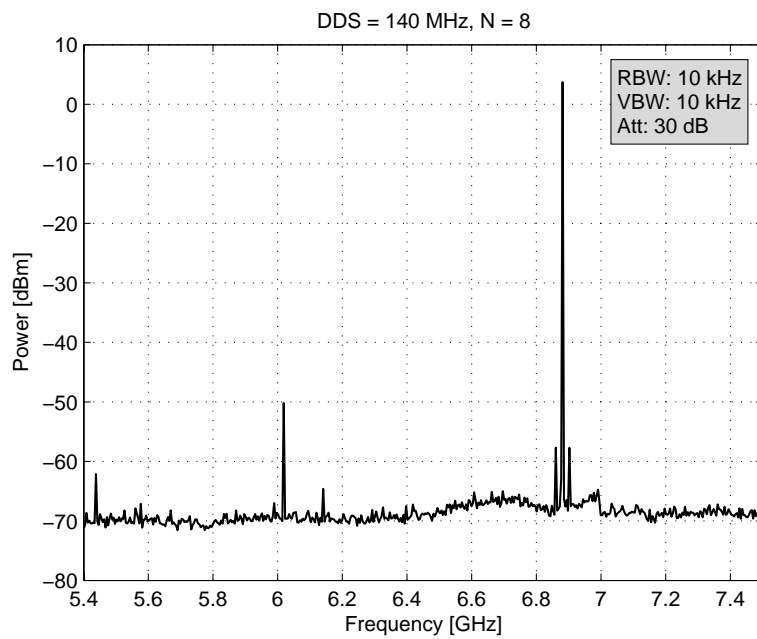


Figure C.15: Wideband frequency spectrum, with DDS = 140 MHz and $N = 8$.

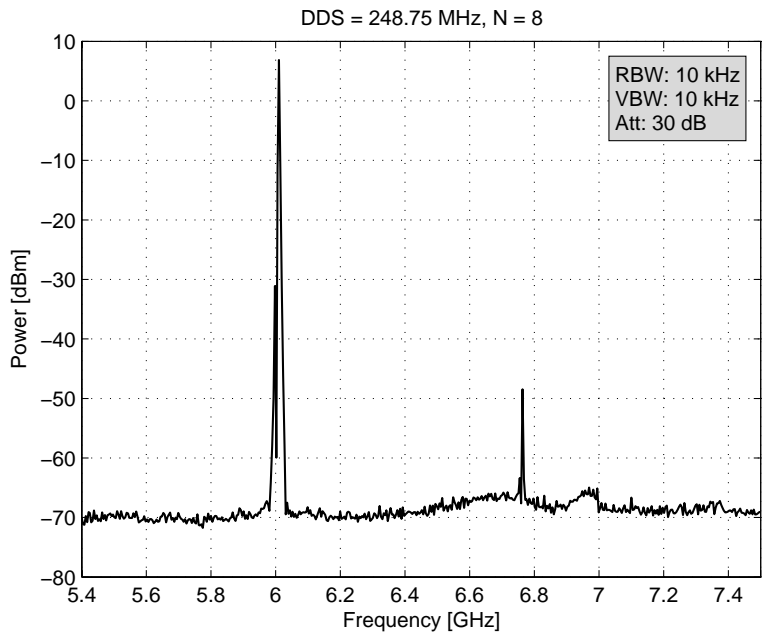


Figure C.16: Wideband frequency spectrum, with DDS = 248.75 MHz and $N = 8$.

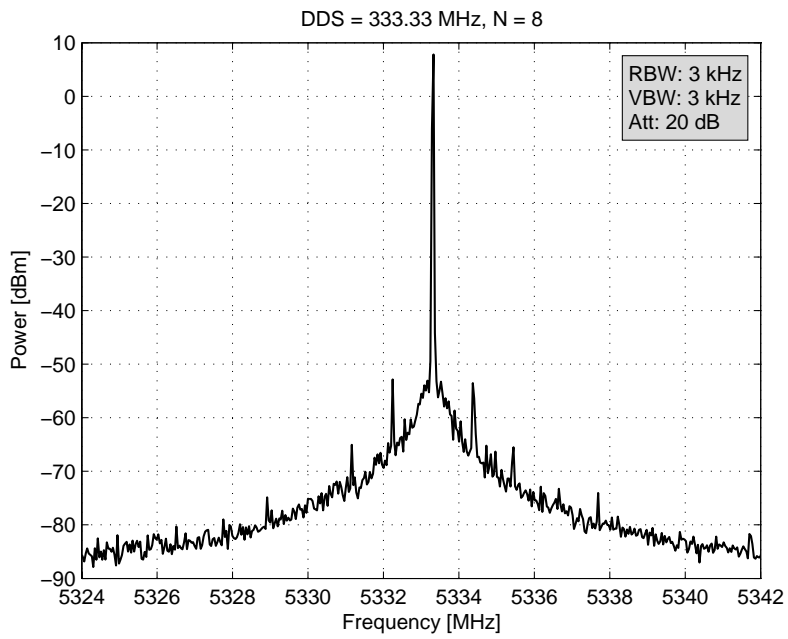


Figure C.17: Close-in frequency spectrum, with DDS = 333.33 MHz and $N = 8$.

C.7 Bandpass Filter Used for Spurious Performance Investigation

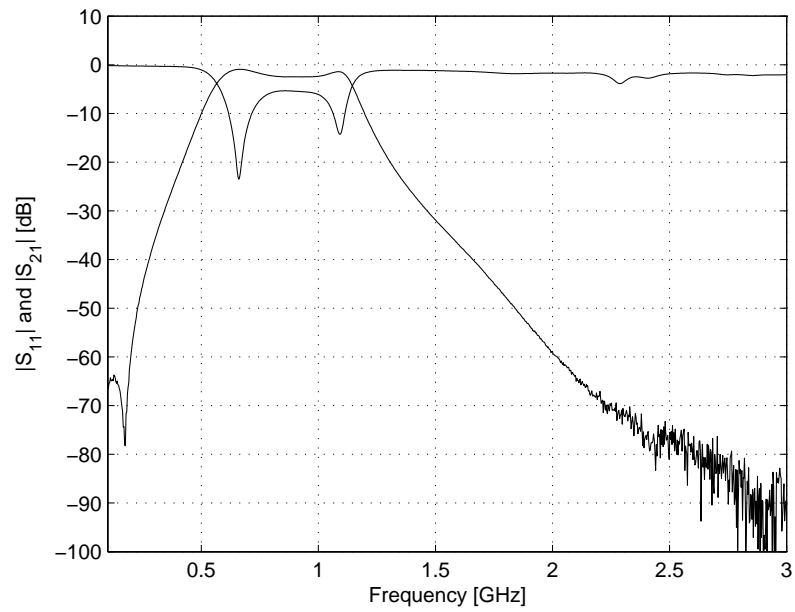


Figure C.18: Frequency response of the bandpass filter.

Appendix D

Comblines and Interdigital Filter Dimensions

D.1 Comblines Filter Dimensions

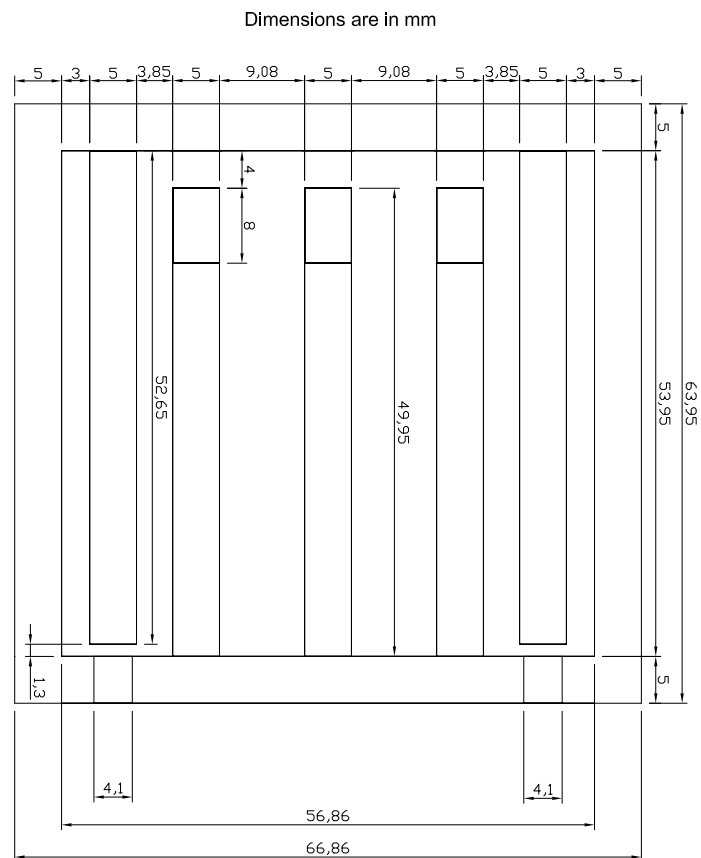


Figure D.1: Top view of the combline filter.

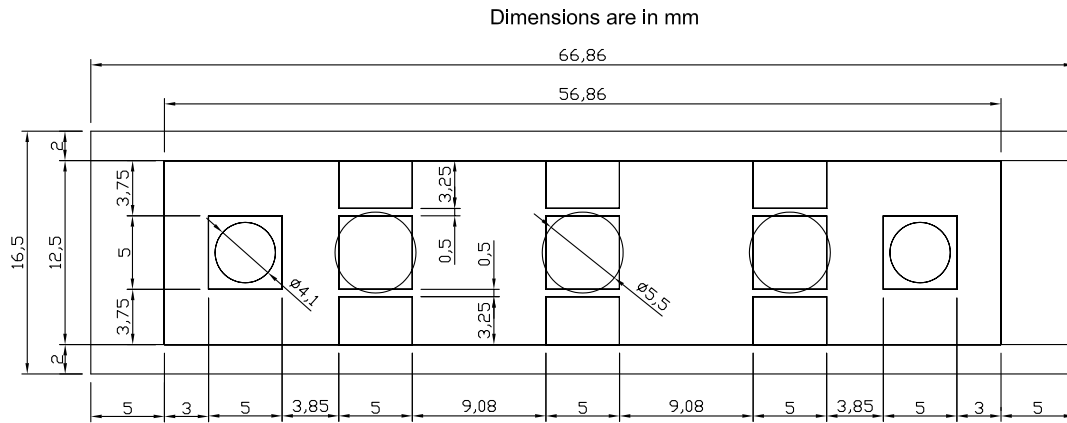


Figure D.2: Cross section of the combline filter.

D.2 Interdigital Filter Dimensions

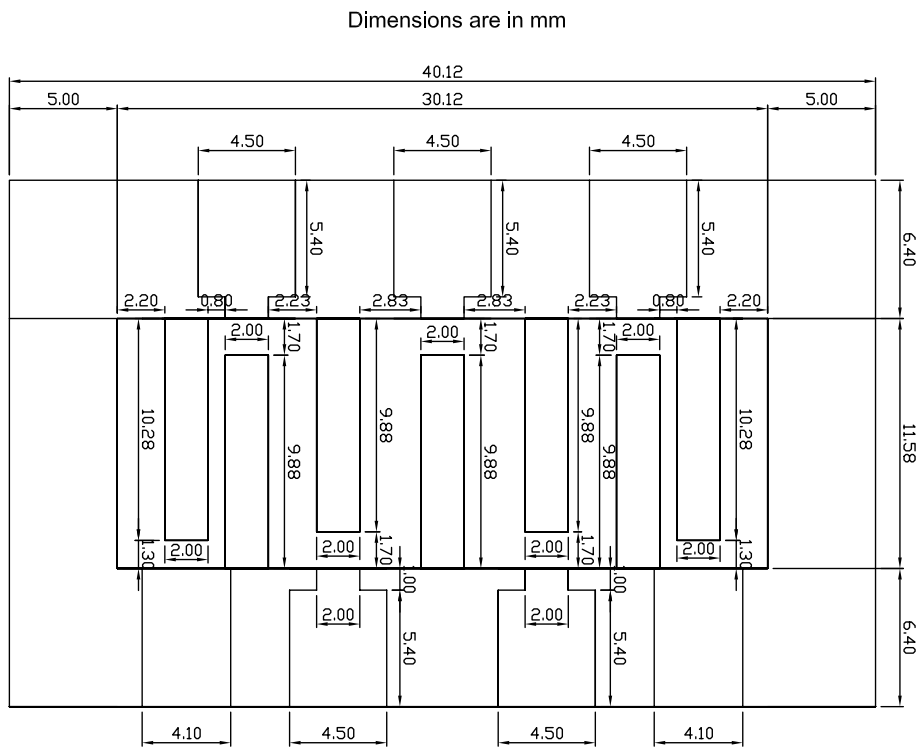


Figure D.3: Top view of the interdigital filter.

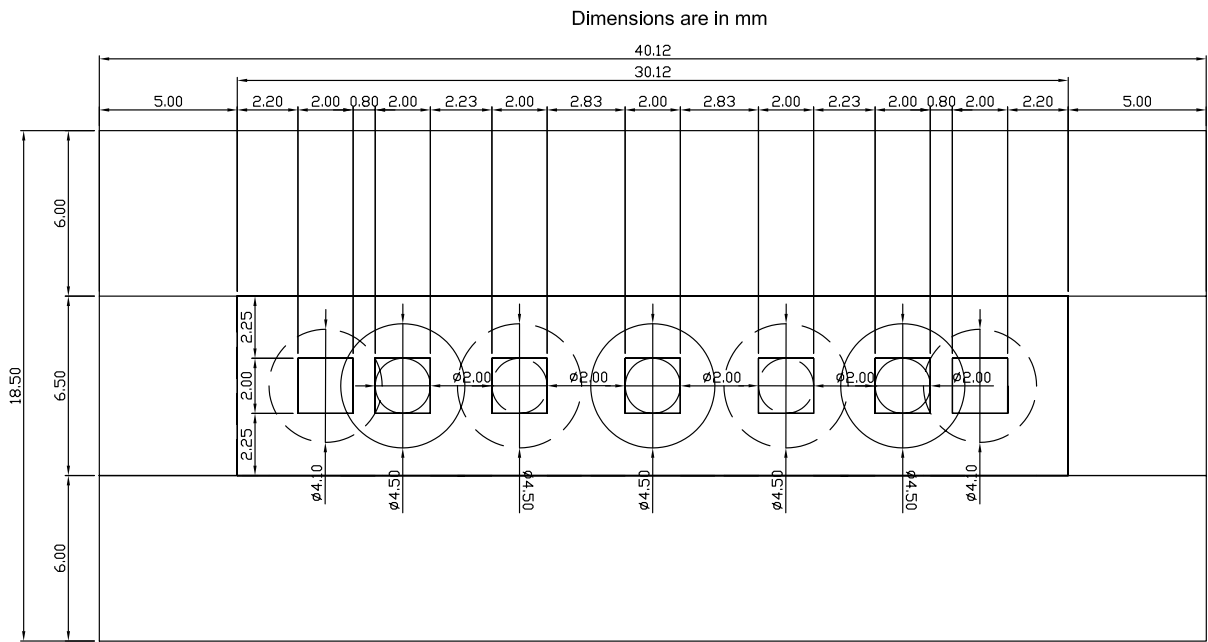


Figure D.4: Cross section of the interdigital filter.

Appendix E

Frequency Synthesiser Circuit Diagrams

E.1 Multiplier Chain Circuit Diagram

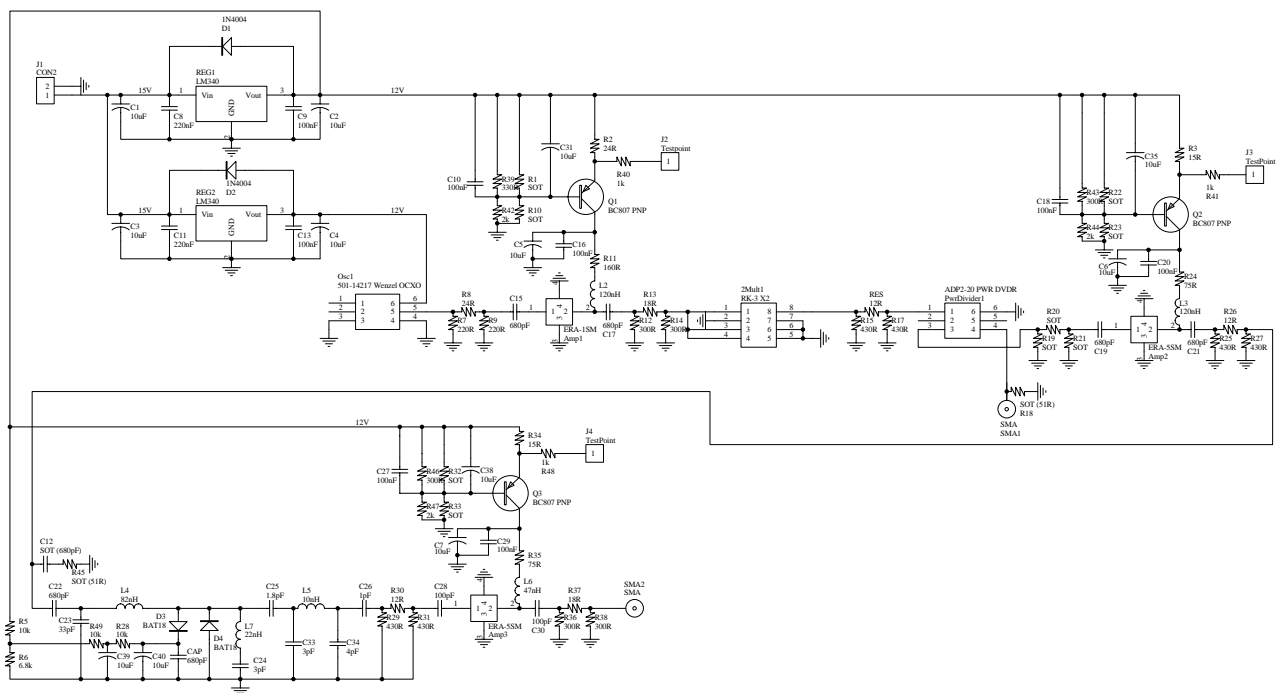


Figure E.1: Multiplier chain circuit diagram.

E.2 PLL Circuit Diagram

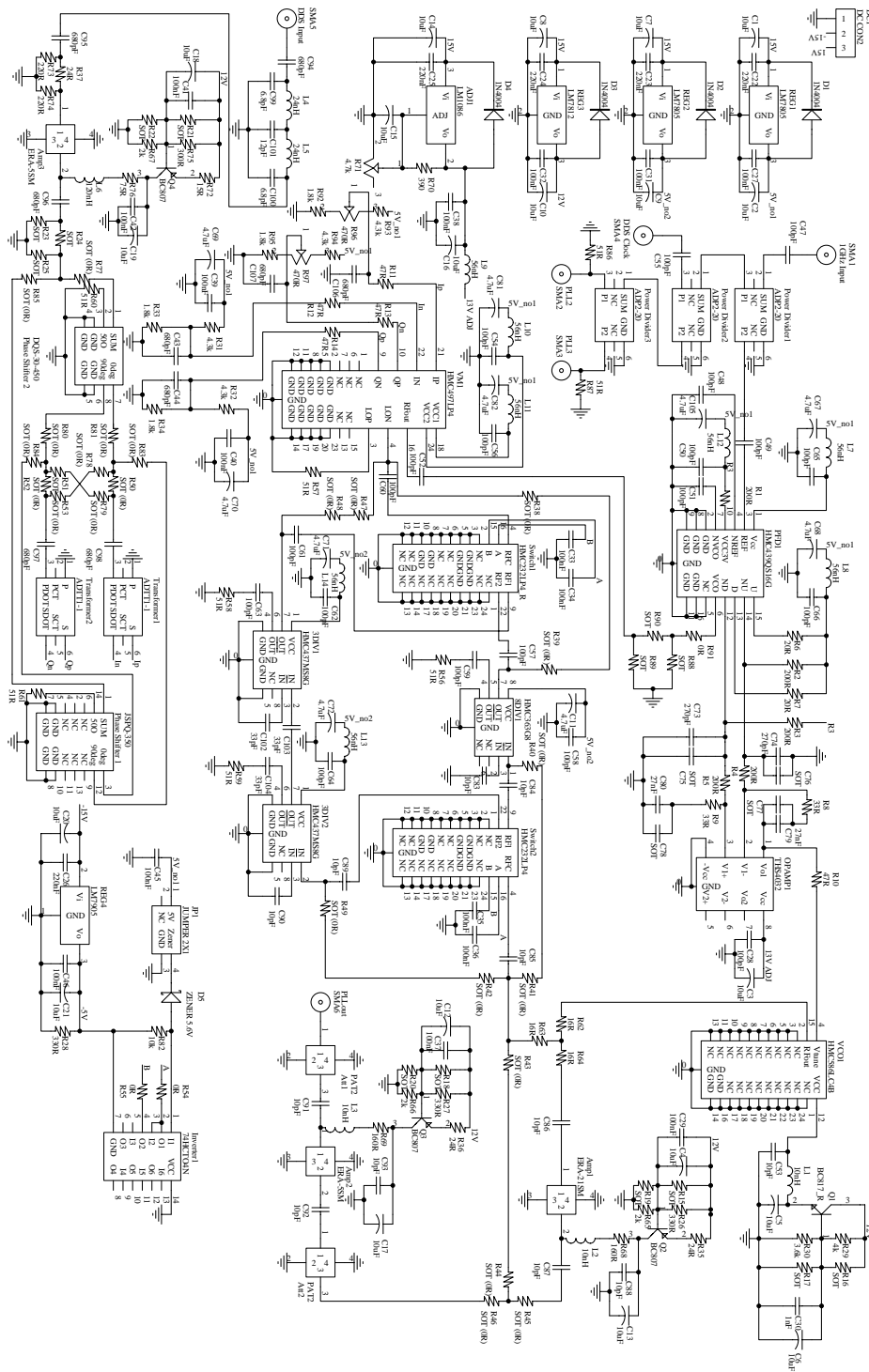


Figure E.2: PLL schematic circuit diagram.

Appendix F

CST Models and Simulation Results

F.1 Frequency Synthesiser Output Transition

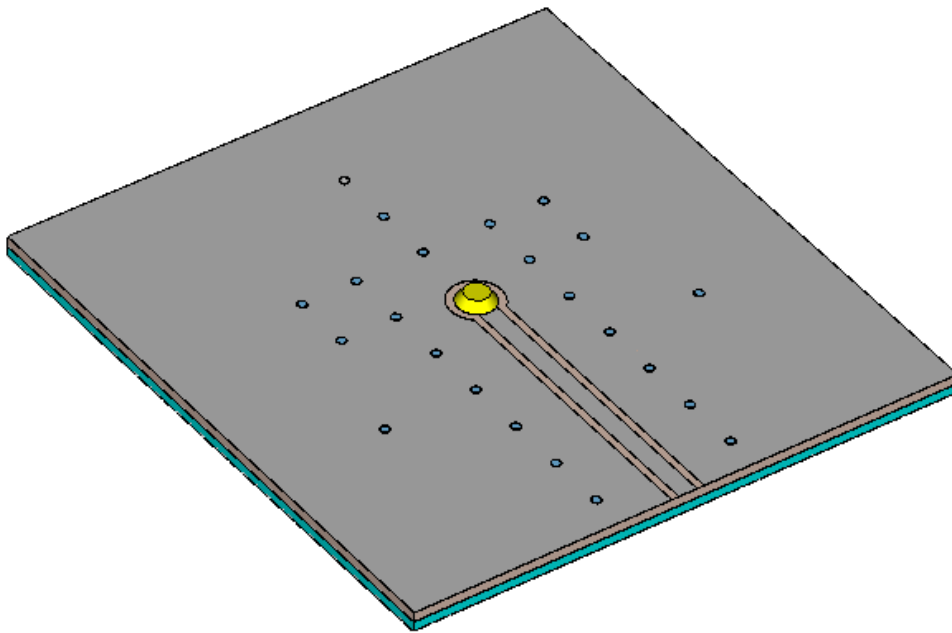


Figure F.1: Top view of the *CST* coplanar waveguide to SMA connector transition model.

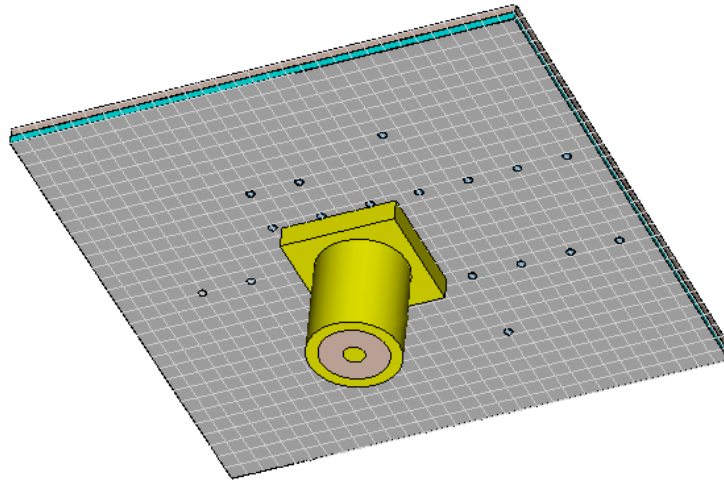


Figure F.2: Bottom view of the CST coplanar waveguide to SMA connector transition model.

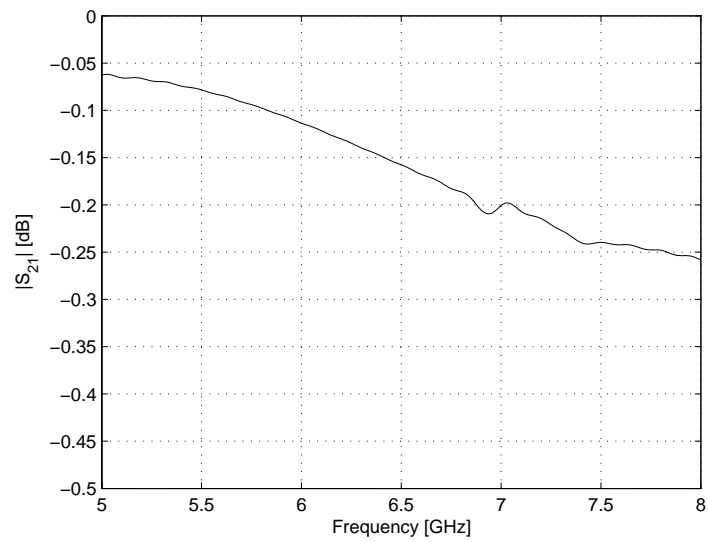


Figure F.3: $|S_{21}|$ of the coplanar waveguide to SMA connector transition.

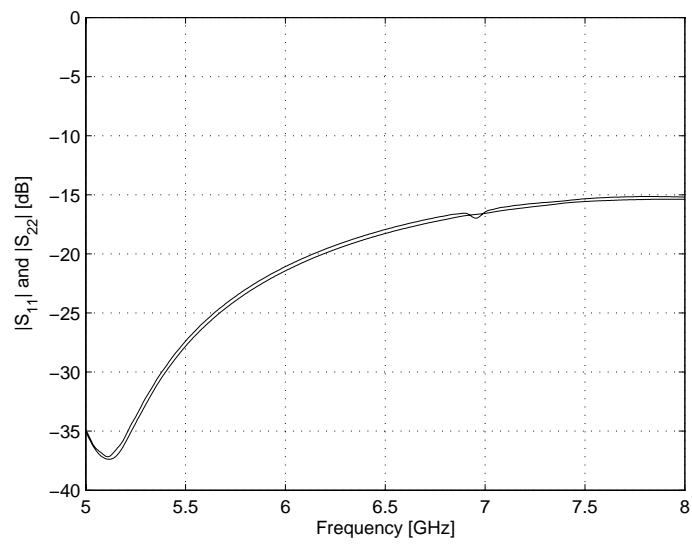


Figure F.4: $|S_{11}|$ and $|S_{22}|$ of the coplanar waveguide to SMA connector transition.

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