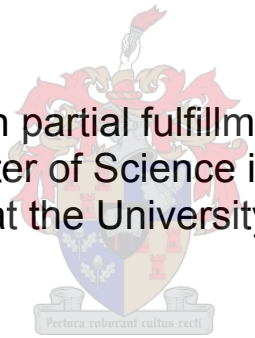
Control of a 1.5 MW active power filter and regeneration converter for a Spoornet DC traction substation

Pieter Hendrik Henning



Thesis presented in partial fulfillment of the requirements
for the degree of Master of Science in Electrical and Electronic Engineering at the University of Stellenbosch.

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Co Supervisor: A. D. le Roux

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Declaration

I, the undersigned, hereby declare that the work contained in the thesis is my own original work, unless otherwise stated, and has not previously, in its entirety or in part, been submitted at any university for a degree.

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P.H. Henning Date

Opsomming

Die generator werking van treine se elektriese motors word al vir ‘n geruime tyd gebruik om te rem. Die herwinde energie is egter verkwis in weerstande en gaan dus verlore. Die onlangse vordering op die gebied van drywings elektroniese skakel komponente wat vinniger skakel en ‘n hoër drywing vermoens het, maak dit moontlik om die hergenereerde elektriese energie van GS na WS te verander, wat dan in die Eskom netwerk geinjekteer kan word.

‘n 1.5 MW vol skaal prototype stelsel is gebou, geïnstaleer en getoets in ‘n Spoornet DC substasie. Die stelsel maak gebruik van 'n sewe vlak serie-gekoppelde omsetter topologie. Die topologie vereis ‘n spesiaal ontwerpte “injeksie” transformator waarmee die sewe vlak serie-gekoppelde omsetter topologie aan die ses-fase toevoer koppel word . Die PEC 33 beheerder, wat by die Universiteit van Stellenbosch ontwikkel is, word gebruik om die stelsel te beheer. Die stelsel is ontwerp om twee funksies te verrig, eerstens as ‘n hergenereerde energie omsetter en tweedens as ‘n aktiewe krag filter.

Die stelsel se werking as hergenererende omsetter word beheer deur ‘n naloop beheerder, wat ontwerp is om die DC-bus spanning te reguleer. Die oombliklike reaktiewe drywings teorie [1] word gebruik om die stelsel se aktiewe krag filter the beheer. Beide hierdie beheer algoritmes word in ‘n DSP gebaseerde beheerder geimplimenteer. Die vervlegte skakelseine word deur ‘n eksterne PWM bord opgewek wat die seine dan na die omsetter stuur.

Heinrich Fuchs was verantwoordelik vir die ontwerp van die meetstelsel as ook vir die konstruksie van die omsetter stelsel [6][31]. Die vol skaal prototype stelsel is geinstaleer in ‘n GS substasie waar beide funsies suksesvol geimplimenteer en getoets is.

Hierdie tesis bespreek die beheerstrategie wat gebruik is om die stelsel te beheer, as ook die implimenteering van die beheer strategie in ‘n DSP beheerder. Die resultate verkry van toetse wat met die geïnstaleerde stelsel gedoen is word ook bespreek

Summary

Although regenerative braking has been in used in railway systems for a long time already, the energy generated was dissipated in resistor banks. The rapid advances in the power electronics field, accompanied by the development of faster and higher power switching devices in recent years, now make it possible to convert the regenerated electrical energy from DC to AC, which can then be injected into the Eskom grid.

A 1.5 MW full scale prototype system was built, installed and tested in a Spoornet DC traction substation. A seven level series-stacked converter topology was used along with a specially designed injection transformer. The system was controlled by the PEC 33 controller board, which was developed at the University of Stellenbosch. The primary function of the system is to function as a regeneration converter and as a secondary function act as an active power filter.

The regeneration functionality of the system is governed by a Lag compensator, designed to regulate the DC-bus voltage at a fixed level. The filtering operation of the converter is based on the Instantaneous reactive power theory, introduced by H. Akagi [1]. Both these controllers are implemented in a DSP based controller and run continuously. The interleaved gating signals, to switch the converter, are generated on a separate expansion board.

Heinrich Fuchs was responsible for the design of the measuring system as well as the assembly of the physical converter system [6][31]. The full scale system was installed in a DC substation and worked successfully as both a regeneration converter and as an active power filter.

This thesis presents the control strategies to govern the converter, as well as the implementation of the control strategies in a DSP controller. The results obtained in the tests done using the prototype converter system are also discussed.

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Last but in no means least, The Lord, for the opportunities and grace I have received.

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I. List of Abbreviations

AC	Alternating current
AC-VMB	AC voltage measuring board
ADC	Analog-to-digital converter
AnEn	Address-not-Enable
APF	Active power filter
CPU	Central processing unit
DC	Direct current
DC-VMB	DC voltage measuring board
DSP	Digital signal processor
DAC	Digital-to-analog converter
DnEn	Data-not-Enable
EERPOM	Electrically erasable programmable read only memory
EMI	Electro magnetic interference
EPLD	Erasable programmable logic device
ExBus	External Bus
fmax	Maximum clock frequency
FPGA	Field programmable gate array
IGBT	Isolated gate bipolar transistor
IMB	Current measurement boards
INT3	DSP external interrupt 3
IRPT	Instantaneous reactive power theory
JTAG	Joint test action group
LCD	Liquid crystal display
nACK	not-Acknowledge
MFLOPS	Million floating point operations per second
MIPS	Million instructions per second
NPC	Neutral point clamped
ODB	Optical driver boards
OP-AMP	Operational amplifier
PEC 33	Power Electronic controller
PC	Personal computer
PCB	Printed circuit board

PLD	Programmable logic devices
RnW	Read-not-write
RMS	Root mean square
PWM	Pulse width modulation
PWM-EB	PWM Expansion Board
ROM	Read only Memory
RTC	Real time clock
SRAM	Static random access memory
TINT0	DSP internal timer interrupt 0
VMB	Voltage measuring board
VHDL	Very high speed hardware description language

II. List of symbols

X_a	Phase A of entity X
X_b	Phase B of entity X
X_c	Phase C of entity X
X_α	Phase α of entity X
X_β	Phase β of entity X
X_{AC}	AC component of entity X
X_{DC}	DC component of entity X
X_{ref}	reference for entity X
X_{RMS}	RMS value for component X
$\hat{X}$	Peak value for component X
C_{eq}	Equivalent DC-bus capacitance
C_{inv}	A single level's DC-bus capacitance
d_x	Duty cycle for the voltage vector $\mathbf{V_x}$
D_x	Duty cycle for phase x
I_x	Current in phase x
$\hat{I}(k)$	peak compensation current for the DC-bus regulator
L, L_f	Filter inductance
N	Winding ratio of the injection transformer
p_x	Real power, active power of phase x
$\bar{p}$	DC component of the active power
$\tilde{p}$	AC component of the active power
$P_{3\phi}$	Power calculated on the three-phase side
$P_{6\phi}$	Power calculated on the six-phase side
P_{DC}	Power calculated on the DC side
q_x	imaginary power, reactive power of phase x
$\bar{q}$	DC component of the reactive power
$\tilde{q}$	AC component of the reactive power
t_{sw}	Switching period
$\mathbf{V_x}$	Space vector state x voltage vector

V_x	Voltages of phase X
V_{dc}	DC working point of the DC-bus voltage
$\tilde{V}_{dc}$	AC variation around V_{dc}
V_e	voltage difference between the reference and measured DC-bus voltage
V_{LL}	Line-to-line voltage
V_{LN}	Line-to-neutral voltage
V_{pLL}	Primary side lint-to-line voltage
V_{sLL}	Secondary side line-to-line voltage
Z_{Load}	Load impedance
Z_{supply}	Supply impedance

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1. Introduction

1.1. Overview of the Spoornet project

South Africa's major railway company, Spoornet, uses 3 kV DC to power part of their railway network. The 3 kV DC is supplied by DC traction substations. Although the topologies of these substations vary, they all use diode rectifiers to rectify the AC supply.

Under normal operating conditions a train acts as a load, drawing current from the AC grid via a DC traction substation. These AC currents have a high harmonic content as result of the diode rectifiers. These harmonics do not pose a problem for the DC traction substation, but the line impedance of the supply network causes distortion of the supply voltages. The introduction of various standards regarding power quality at the point of common coupling, such as IEEE 519 [26] and NRS 048 [30], introduced by South Africa's National Electricity Regulator, are forcing companies like Spoornet to look for ways of reducing the amount of harmonics they cause.

The maintenance cost on mechanical breaks makes it economically unfeasible for electric trains to rely solely on their mechanical brakes to slow the trains [6]. Particularly on downhill tracks, the trains use their electric motors to brake. The kinetic energy of the train is converted to electrical energy by the motor, working as a generator. This regenerated energy can be used by another train on the same section of track, but the majority of energy is currently dissipated in resistor banks.

Figure 1.1 shows a diagram of a DC traction substation and the shunt converter system, developed primarily as a regeneration converter with a secondary role as an active power filter. When a passing train slows down, using regenerative braking, the voltage of the DC-line rises. The converter system is to convert the DC to AC and feed the energy back into the Eskom gird. While the train is drawing current from the AC grid, the system is to act as an active power filter (APF), by injecting harmonic current components complementary to those drawn by the DC substation and thus reducing the harmonic content of the current drawn from the AC grid. Japan has

been using inverting DC traction substations since the late seventies [32] and combining the inverter functioning with active power filtering was introduced in the mid nineties [33].

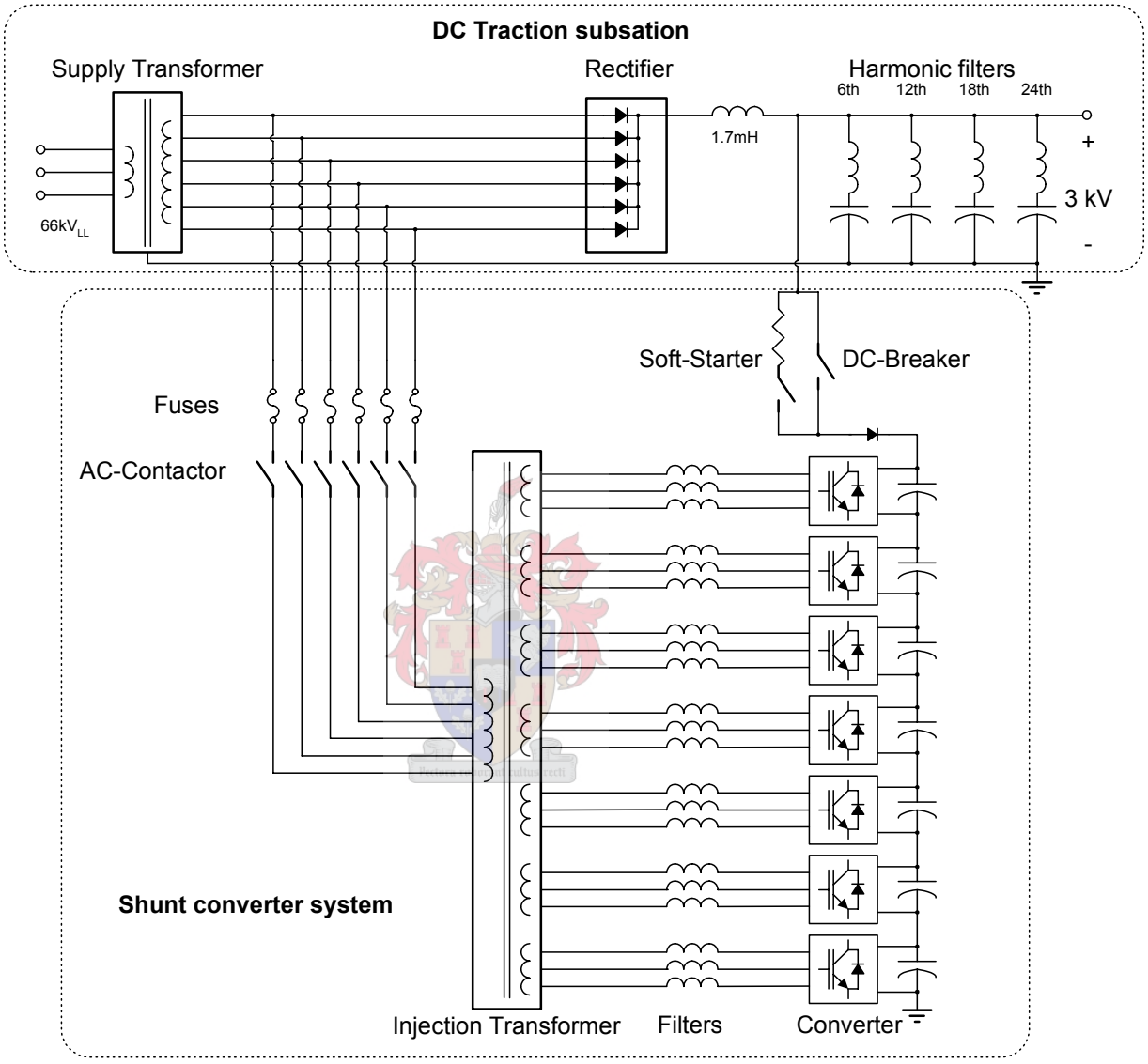


Figure 1.1 Block diagram of the overall system

The system is required to invert 1,5 MW continuous energy into the supply network. For the intended installation site the 3 kV DC supply will be inverted to a 2420 V, 6 phase 50 Hz AC system which feeds into the main traction transformer.

1.2. Overview of this thesis

Chapter 2 starts by introducing the reader to the DC traction station setup and basic converter topologies, before discussing the seven level series-stacked converter along with its connections to the existing systems within the DC substation. The chapter concludes with an overview of the control strategy and an introduction to the controller hardware used to control the converter system.

The control strategy is discussed in detail in chapter 3, starting with the active power filtering scheme, based on the Instantaneous reactive power theory [1]. The DC-bus controller, which is also responsible for the regeneration functioning of the system, is discussed next. This is followed by the PWM duty cycle generation, by means of space vector PWM.

Chapter 4 discusses the simulations done to examine the converter topology and the control strategies which were to be implemented. First the six-phase system, including the main injection transformer and the rectifier, is investigated. The next set of simulations investigates the differences between the non-interleaved and the two interleaved switching schemes. This is followed by the simulations to examine the APF control strategy, based on the Instantaneous reactive power theory [1], where after the behaviour of the Lag compensator [5] is investigated. The chapter concludes with a simulation combining the different control aspects, including the transitions between the regeneration and the APF modes.

The practical implementation of the system and the control there of is discussed in chapter 5. This includes a discussion of the DSP based controller, the measuring system, the generation of the interleaved gating signals, the DSP code and the operation of the system. The chapter concludes with practical results and a discussion there of.

Chapter 6 presents the conclusions and recommendations for future work on the Spoornet system.

2. The Spoornet system

2.1. The DC traction substation

A Spoornet DC traction substation at Wolesely was chosen as the test site, since passing trains regularly use regenerative braking on the section of track, supplied by the substation. Although regenerative braking is used on this section (of the track), the excessive amount of regenerated energy (i.e. not being used by another train) is dissipater in resistor banks in the substation and thus wasting the regenerated energy.

The substation connects to a three-phase 66 kV feed from the Eskom network. The supply is stepped down to 2420 V and transformed to a six-phase voltage system. The output of the transformer is rectified by a six-phase half bridge rectifier to power the 3 kV DC-line. To smooth the DC voltage, four passive filters are connected to the output of the rectifier. These are tuned to reduce the 6^{th}, 12^{th}, 18^{th} and 24^{th} order harmonics. The substation houses two of these six-phase half bridge rectifier bays, each one having its own traction transformer. These two rectifiers work in parallel under normal circumstances. When viewed from the supply side the substation resembles a twelve pulse rectified load since the primary windings of the one traction transformer has a star connection and the other has a delta connection.

The injection transformer was designed to mirror the traction transformer with the star connected primary. The vector diagram of the traction transformer is shown in Figure 2.1, with its star connected primary windings and the triple star connection of the secondary windings.

The configuration of the transformer results in a line-to-neutral voltage equal to one of the line-to-line voltages on the secondary side as shown in Figure 2.1. A further characteristic is that the amplitude relationship between the primary line-to-neutral voltage and the voltage on the secondary differs with a factor of $\sqrt{3}$ when we ignore the winding ratio. The voltage equivalences between the primary line-to-neutral, secondary line-to-neutral and the line-to-line voltages on the secondary are listed in Table 2.1.

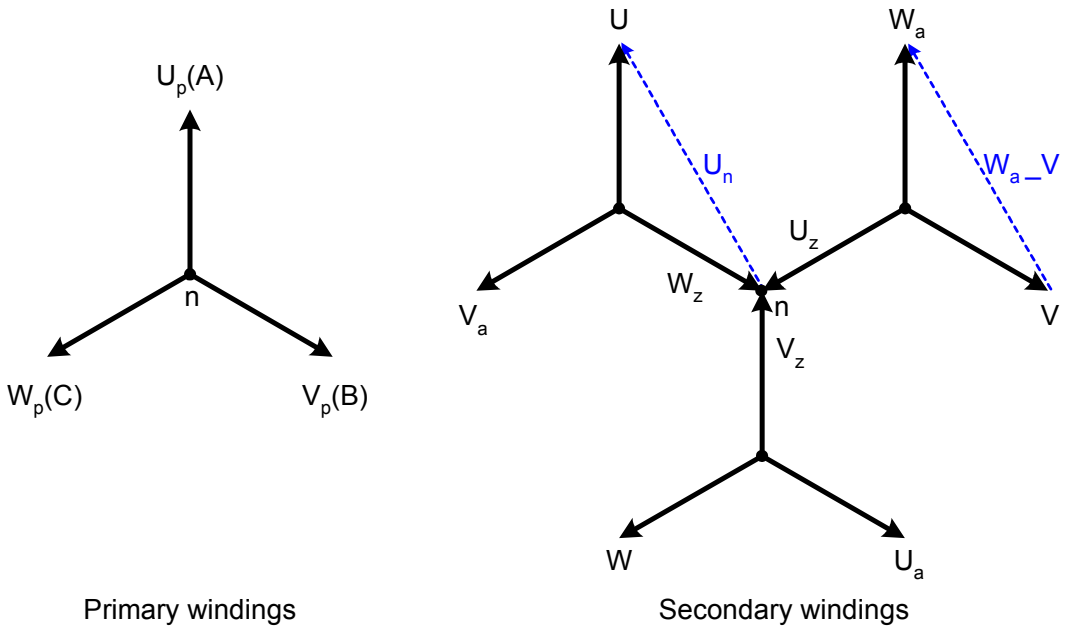


Figure 2.1 The vector polarity diagram of the supply transformer

Table 2.1 Table of voltage equivalencies for the main traction transformer

Primary V_{Ln}	Secondary V_{Ln}	Secondary V_{LL}
$\frac{U}{\sqrt{3}}\angle 30^{o}$	V_{Un}	V_{wa_V}
$\frac{U}{\sqrt{3}}\angle -30^{o}$	V_{Wan}	V_{u_Va}
$\frac{V}{\sqrt{3}}\angle 30^{o}$	V_{Vn}	V_{Ua_W}
$\frac{V}{\sqrt{3}}\angle -30^{o}$	V_{Uan}	V_{V_Wa}
$\frac{W}{\sqrt{3}}\angle 30^{o}$	V_{Wn}	V_{Va_U}
$\frac{W}{\sqrt{3}}\angle -30^{o}$	V_{Van}	V_{W_Ua}

The six-phase line-to-line supply voltages and the six-phase line currents are measured between the diode rectifier and the injection point of the inverter. The DSP

based control algorithms uses a three-phase current and voltage domain, thus the six-phase voltage and current measurements have to be transformed to their equivalent three-phase quantities. The relationship between the six-phase line-to-line voltages and their equivalent three-phase line-to-neutral voltages are illustrated in Figure 2.2.

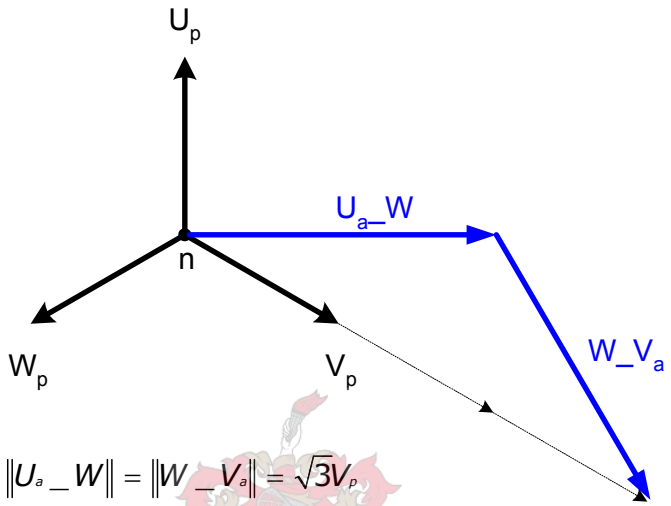


Figure 2.2 Calculating the equivalent three-phase voltages

The steady state relationship between the six-phase and three-phase voltages are given by

$$v_a = \frac{V_{W\_Va} + V_{Va\_U}}{-3} \tag{2.1}$$

$$v_b = \frac{V_{V\_Ua} + V_{Ua\_W}}{-3} \tag{2.2}$$

$$v_c = \frac{V_{U\_Wa} + V_{Wa\_V}}{-3} \tag{2.3}$$

Similarly the six-phase current measurements have to be transformed to their three-phase equivalent values. Their relationship is illustrated in Figure 2.3 where W_z as shown in Figure 2.1 is the negative of $V_a + U$.

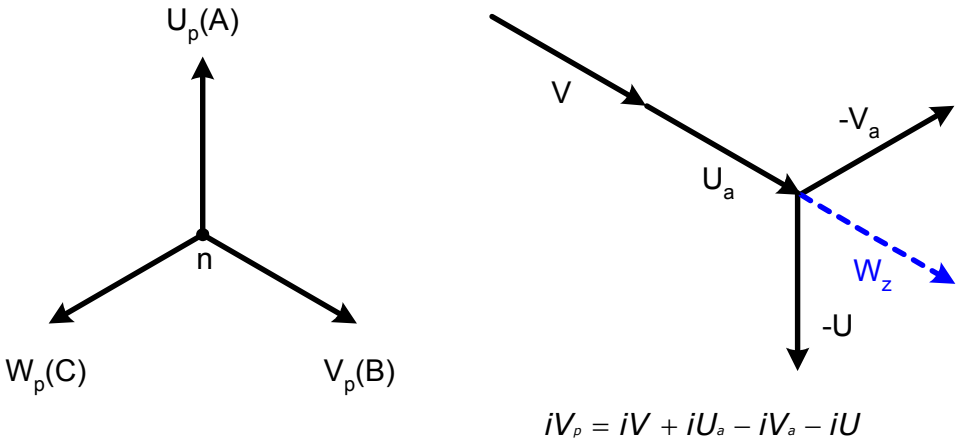


Figure 2.3 Calculating the equivalent three-phase currents

The steady state relationship between the six-phase and three-phase currents are:

$$i_{Up} = i_U + i_{Wa} - i_{Ua} - i_W \tag{2.4}$$

$$i_{Wp} = i_W + i_{Va} - i_{Wa} - i_V \tag{2.5}$$

$$i_{Vp} = i_V + i_{Ua} - i_{Va} - i_U \tag{2.6}$$

2.2. The basic compensator topologies

The performance of a compensator topology depends greatly on the load profile and the nature of the power quality compensation that is required. This section outlines the three main converter topologies and their properties.

2.2.1. The shunt compensator

Figure 2.4 shows a block diagram of a shunt compensator system. The voltage source inverter is connected in parallel with the supply and is controlled to act as a controlled current source [3][13][16][18]. In order to function properly the load has to be inductive or be modelled as a current source.

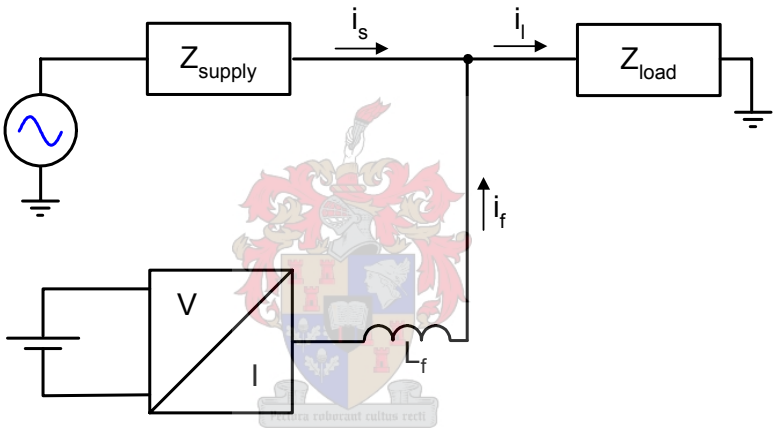


Figure 2.4 Block diagram of a shunt compensator

This converter topology can be used as an APF by injecting current harmonics complementary to the harmonics drawn by the load, resulting in harmonic cancellation. By injecting reactive power into the network the converter can also be used for power factor correction, while a small amount of real power is drawn to sustain a constant DC-bus voltage [3][13][16][18]. It is also possible to compensate for voltage flicker and current unbalance in a three-phase system.

2.2.2. The series compensator

A block diagram of a series compensator or series-injection device is shown in Figure 2.5. The converter is controlled as a voltage source. A compensating voltage is inserted in series into the supply line via the injection transformer. This type of device functions correctly if load is capacitive or can be modelled as a voltage source.

This topology lends itself to voltage dip compensation, voltage unbalance compensation and harmonic isolation. By further controlling the equivalent impedance of the injection transformer line reactance compensation and series resonant damping can be achieved. The topology can however not be used for power factor correction [3][13][16][18].

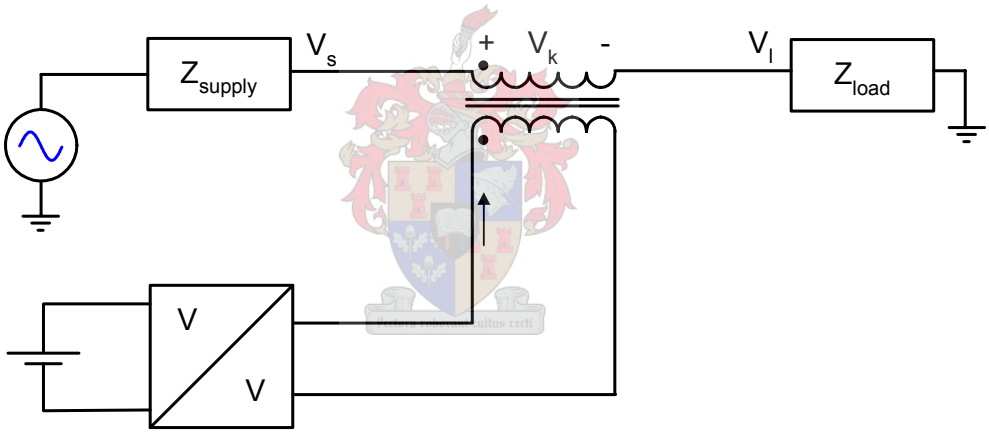


Figure 2.5 A block diagram of a series compensator

A major disadvantage of this topology is that large fault currents will flow through the converter when a line fault occurs on the load side, since the converter is in series with the supply. It is possible to minimize the effect of the fault current by designing the injection transformer to saturate or by including a solid state bypass to carry the fault current.

2.2.3. The series-shunt compensator

Figure 2.6 shows a block diagram of the series-shunt converter topology which combines the benefits of the series and shunt compensators. Compensation can be done by either the series or the shunt compensator, depending on the type of load, inductive or capacitive.

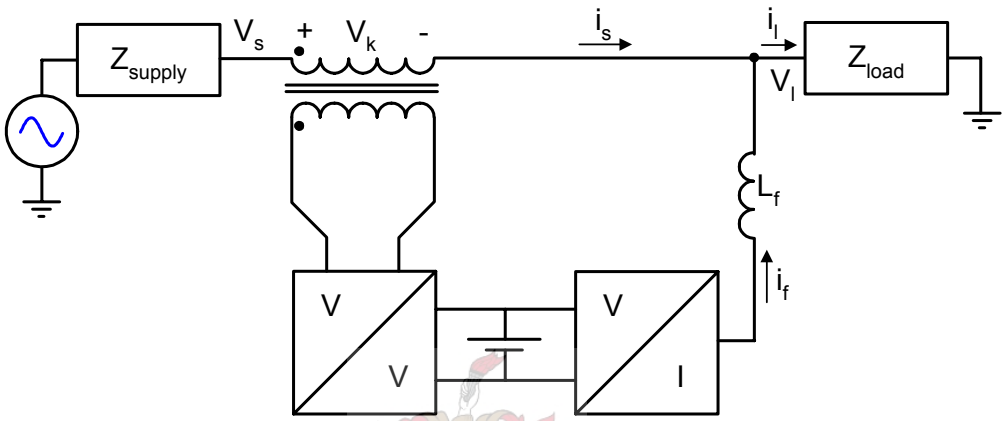


Figure 2.6 The Series-shunt converter topology

This converter topology can compensate for voltage flicker, voltage unbalance in a three-phase system, voltage dips, current unbalance in a three-phase system, reactive power and unwanted harmonics [3][13][18].

This converter topology allows an energy storage device to be connected to the common DC-bus of the two converters while the shunt converter regulates the DC-bus voltage.

2.3. The basic converter topologies

Over the past few years the need for higher rated power equipment has given rise to a number of multilevel converters. These topologies allows the converter system to have a higher DC-bus voltage rating while using switching devices with lower ratings [4][7][10][13][29]. A further feature of a multilevel converter is that it produces lower output harmonic levels than a single level system does [7][10]. This section will discuss the four most common multilevel topologies.

2.3.1. Three-phase full bridge converter

The three-phase full bridge inverter topology is shown in Figure 2.7. The inverter is made up of three phase arms connected to a common DC-bus. The pole of each phase arm is connected to a filter inductor.

With the three-phase outputs coupled, a change in one phase will directly influence the output of the other two phases. This topology does not allow a zero phase sequence current to flow, since the sum of the output currents must be zero.

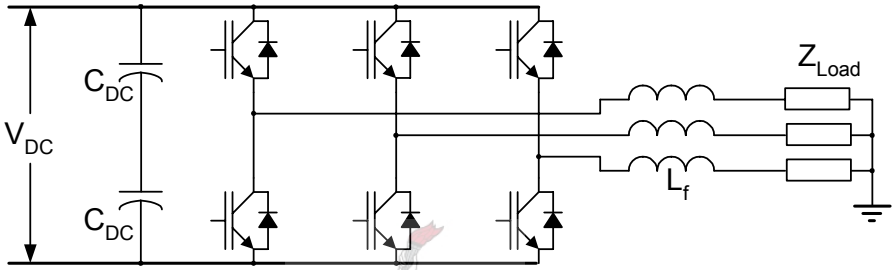


Figure 2.7 Three-phase inverter with coupled outputs

Switching the two IGBTs on a phase arm complementary, the converter has eight valid states, of which two are called zero states. This is discussed in detail in section 3.4.2 and the output voltages are listed in Table 3.1

2.3.2. Series-stacked multilevel inverter

As shown in Figure 2.8, the series-stacked inverter is made up out of a number of full bridge inverters with their DC-busses connected in series. This allows the inverter system to have a high DC-bus voltage rating while using switching devices with lower ratings [4][7][10][13][29]. In addition a multi level topology produces lower output harmonic levels than a single level system [7][10].

The DC-busses of the inverters are connected in series and their outputs are connected to matching primaries of the output transformer. By connecting the full bridge inverters with their DC-busses in series the rating of each inverter only needs to be equal to the total system rating divided by the number of levels. This includes

the rating for the switches and the capacitors. The output transformer does however need to handle the full rating of the system. The total power rating of the converter system is equal to the sum of the power ratings for the seven individual full-bridge inverters. Although the topology is simple and does not require additional clamping diodes or capacitors, the transformer has to be specially designed with a predetermined number of levels.

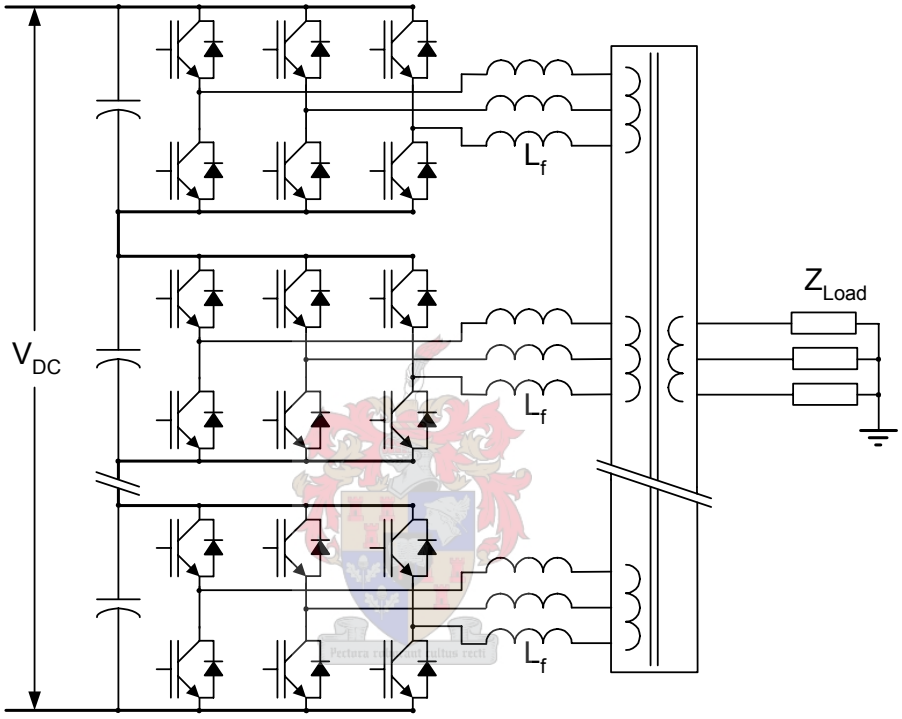


Figure 2.8 Series-stacked multi level inverter

Filter capacitors can be added to the primary or secondary side of the output transformer. By moving the filter capacitors to the secondary of the transformer the number of filter capacitors are reduced. This does cause larger ripple currents to flow through the output transformer, but the leakage inductance of the transformer can be used as a part of the filter inductor.

A further advantage of the series-stacked topology is that the DC-bus has excellent balancing characteristics under steady state conditions [13], whether the system in switched in an interleaved or non-interleaved manner. By using interleaved switching

the equivalent switching frequency on the load side is multiplied by the number of converter levels [29].

2.3.3. Cascade multilevel converter

The three-phase cascade converter topology is shown in Figure 2.9. Each phase of the three-phase cascade converter is made up out of a number of single-phase, full bridge inverters with their outputs connected in series [4][8][10][19]. Each level can generate three output voltages, $+V_{DC}$, 0 and $-V_{DC}$ [8][19]. The multilevel inverter output is thus synthesized by adding the output voltages of the different levels together. The staircase construction of the output voltage leads to reduced electro magnetic interference (EMI) [9].

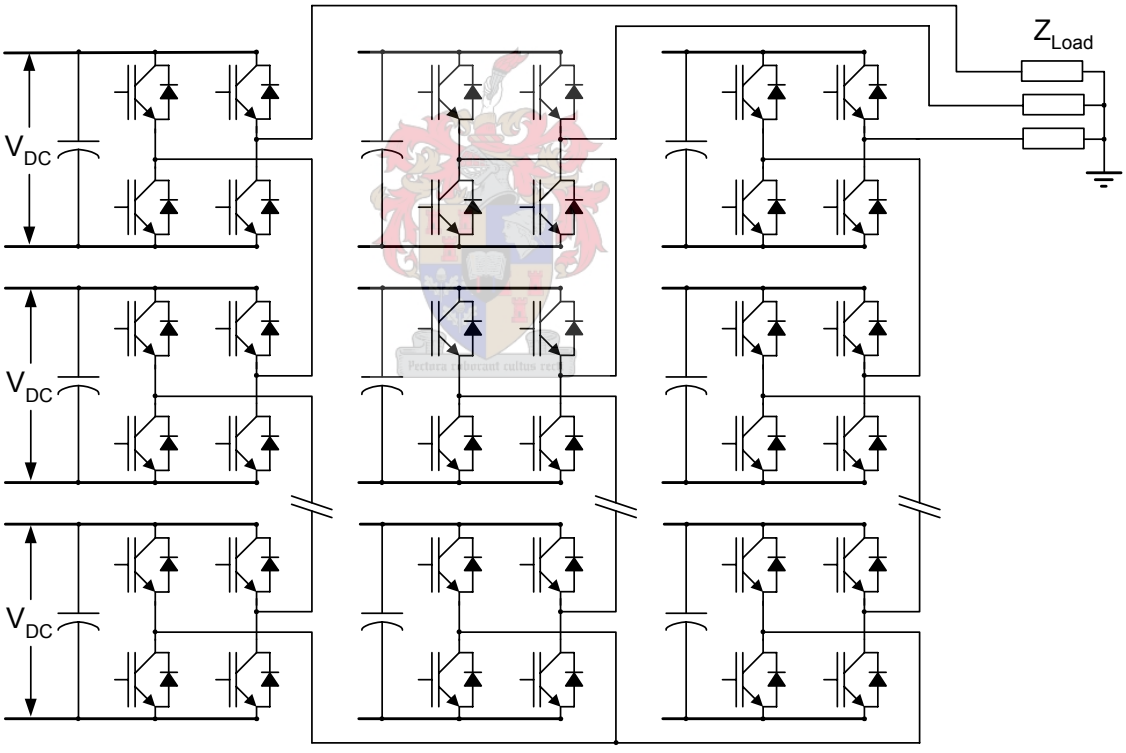


Figure 2.9 The three-phase cascade converter topology

A disadvantage of this topology is that it needs isolated DC-bus supplies. Unles the converter is used purely for reactive power compensator, when capacitors can be used as the DC-bus energy source [4][8][10]. Among the advantages are that it requires the least amount of components to achieve the same number of output

voltage levels as other multilevel converters [8]. Since topology is modular and does not require other components like clamping diodes [8][10] there is thus no penalty involved in implementing a large number of level [20].

2.3.4. Neutral-point-clamped converter

The neutral-point-clamped (NPC) or diode-clamped converter topology is shown in Figure 2.10.

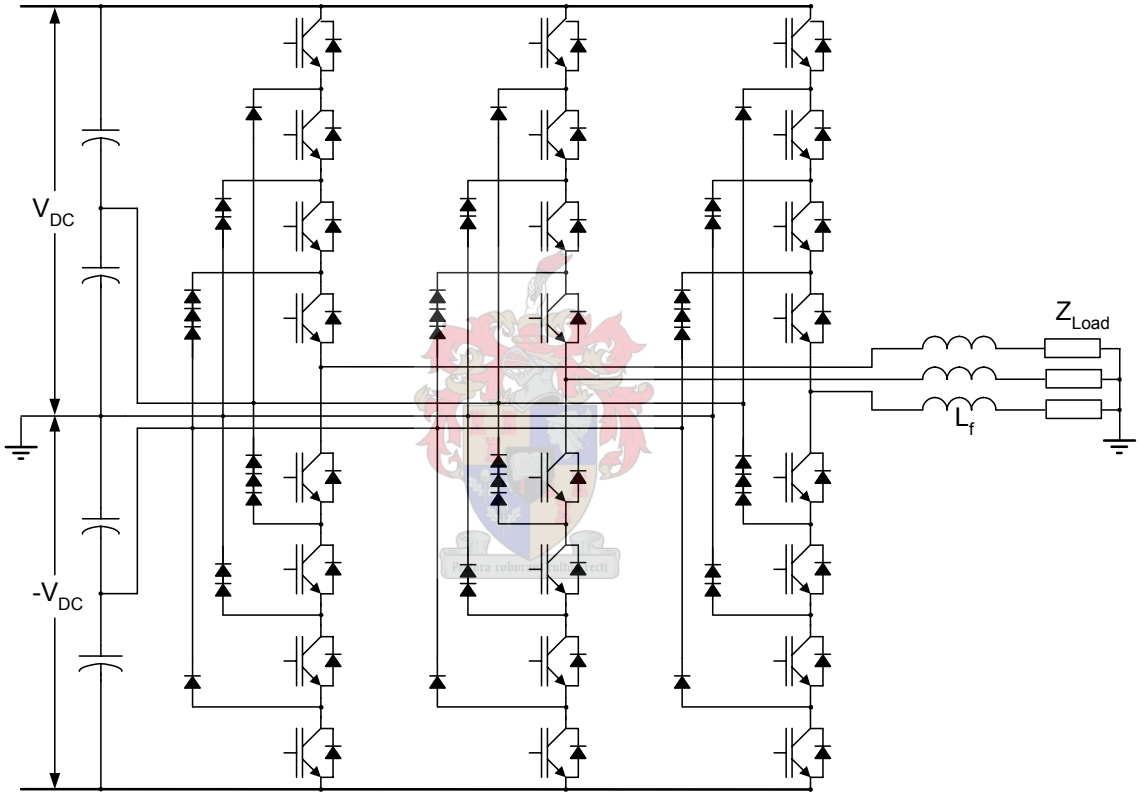


Figure 2.10 The neutral-point-clamped multilevel converter topology

The NPC converter uses a single DC-bus that is divided by a string of series capacitors into a number of voltage levels. The arrangement of the switching devices and clamping diodes allows any of the voltage levels to be switched to the converter's output [10].

Although each of the switching devices is only required to block a voltage level equal to $\frac{V_{DC}}{n-1}$, where n is the number of output voltage levels, the clamping diodes need different reverse blocking voltage ratings. In general, clamping diodes with the same rating as the switching devices are used. The diodes are then connected in series to achieve the required blocking voltage rating. The number of clamping diodes for each phase will be $(n-1)\times(n-2)$, which represents a quadratic increase in the number of clamping diodes needed [8][19][20]. This makes the physical layout and cost of the system impractical when requiring a large number of output voltage levels [20][8][19].

In applications where in real power needs to be converted from DC to AC or AC to DC, the capacitors charge and discharge unevenly which results in capacitor voltage unbalance. To solve the problem a more intricate control strategy, including redundant switching states, has to be implemented increasing the systems complexity [8][10].

2.3.5. Flying-capacitor multilevel converter

Figure 2.11 shows the three-phase flying-capacitor multilevel converter topology, also known as the capacitor-clamped converter. All three phase legs share the same DC link capacitor bank [8][11]. The flying-capacitor converter offers more flexibility with regard to the synthesis of the output voltages than the NPC converter does [19].

Similar to the NPC converter, an n-level flying-capacitor converter has n output voltage levels. Assuming that the voltage rating of each capacitor is equal to the voltage rating of the switching devices, an n-level flying-capacitor will require $\frac{(n-1)(n-2)}{2}$ clamping diodes per phase arm and $(n-1)$ main DC-bus capacitors [8][19].

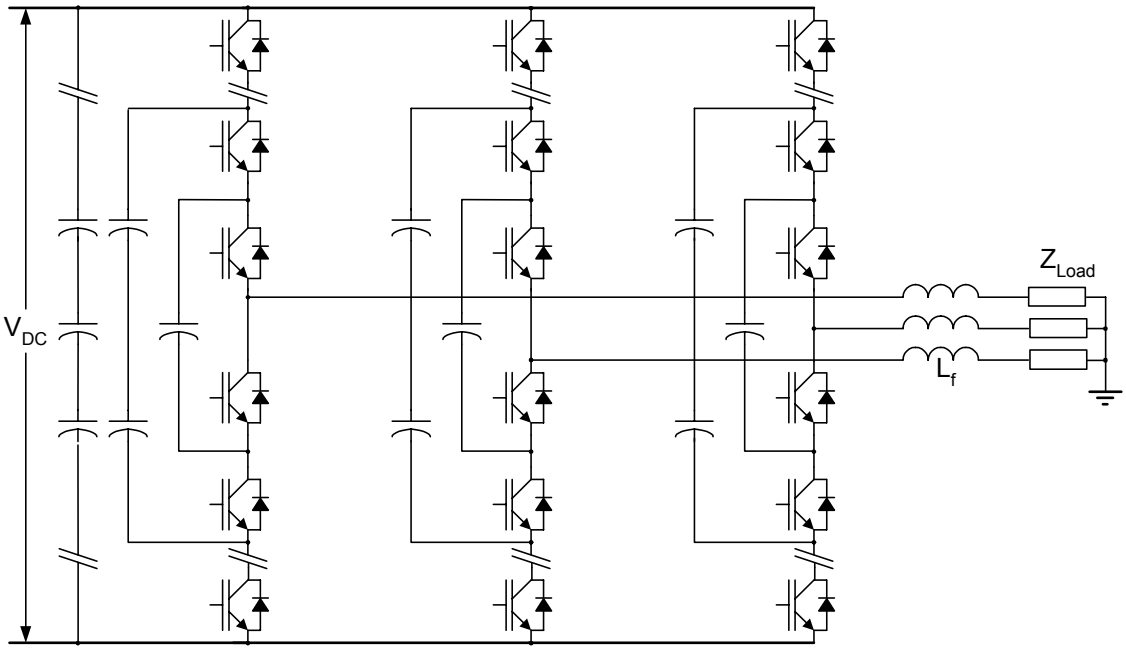


Figure 2.11 The flying-capacitor multilevel inverter topology

This topology allows both real and reactive power flow to be controlled, but difficulty occurs in balancing the capacitor voltages during real power conversion and the large number of storage capacitors count against the topology [8][19].

2.4. The seven level series-stacked converter system

The series-stacked multilevel converter topology was chosen for the Spoornet project. The topology allows standard full bridge three-phase inverters to be connected with their DC-busses in series which results in a high DC-bus rating [14][15]. The multilevel topology also reduces the level of output harmonics produced by the converter [7][10][14][15]. By connecting the standard three-phase inverter's DC-busses in series, no extra components like clamping diodes or capacitors are needed. Another characteristic which favoured the choice of the series-stacked converter topology is its excellent natural balancing properties [13][14][15]. Although the topology does require a specialised injection transformer, the transformer properties are exploited, for example, the leakage inductance is used along with the filter inductance to filter the output. The series-stacked multilevel converter lends itself to interleaving the switching signals. This reduces the output current ripple and increases the equivalent switching frequency [13].

The series-stacked converter is made out of seven three-phase full bridge inverters with their DC-busses connected in series. Figure 2.12 shows one of the three-phase full bride inverters. Each inverter level has a DC voltage rating of 800 V, giving the system a total DC-bus voltage rating of 5.4 kV. The operating specifications set by Spoornet is summarized in Table 2.2

Table 2.2 Operating specifications for the system

Altitude	0 to 1800 m above sea level
Ambient Temperature	-10ºC to 50ºC
Relative Humidity	10% to 90% non-condensing
Lightning conditions	11 ground flashes / km^2 / year
DC voltage	2.3 kV to 3.9 kV
Harmonics caused by substation	300 Hz to 1200 Hz
Auxiliary power supply	88 V to 118 $V_{DC,}$ nominal 110 V_{DC}
Regeneration rating	1.5 MW
DC-bus rating	4 kV

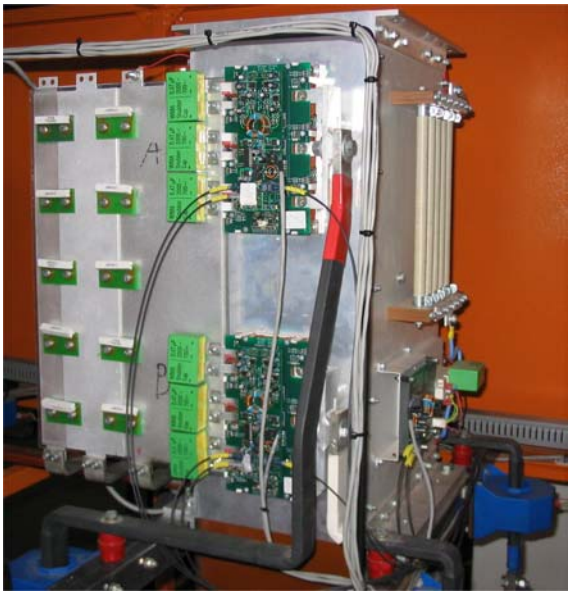


Figure 2.12 One of the seven three-phase full bridge inverters

The seven level series-stacked-converter is shown in Figure 2.13 and its specifications are summarized in Table 2.3.

Figure 2.13 The full seven level series-stacked system

Table 2.3 The seven level series-stacked converter specifications

Number of full bridge converters	7
Total number of IGBTs	42 x 3 (3 in parallel per switch)
Maximum DC voltage rating of IGBT	800 V_{DC}
Maximum output current of IGBT	500 A_{RMS}
Maximum total DC-bus voltage	5.4 kV_{DC}
Six-phase voltages on secondary of injection transformer	2420 V_{RMS}
Three-phase voltage on primary of injection transformer	242 V_{RMS}
Size of filter inductors	150 µH
Switching frequency of the IGBTs	5 kHz
Equivalent switching frequency of the interleaved system	35 kHz
AC protection	Two 3 kV AC contactors Six 400 A fuses Two three-phase zorg suppressors
DC protection	Two blocking diodes 700 A DC contactor seven DC dump switches
AC measurements	21 converter currents 6 six-phase load currents 6 six-phase supply voltages
DC measurements	Eight DC-bus voltages DC current between DC-bus and 3 kV DC-line

2.5. DC circuit connection and Soft-starter

The DC-bus of the converter is connected to the 3 kV DC-line as shown in Figure 2.14. It was decided to soft start the system from the DC side and thus avoiding the inrush current caused by the converter's free wheeling diodes. The blocking diode makes it possible to regulate the converters DC-bus voltage to a level higher than 3 kV without current flowing back to the Spoornet system.

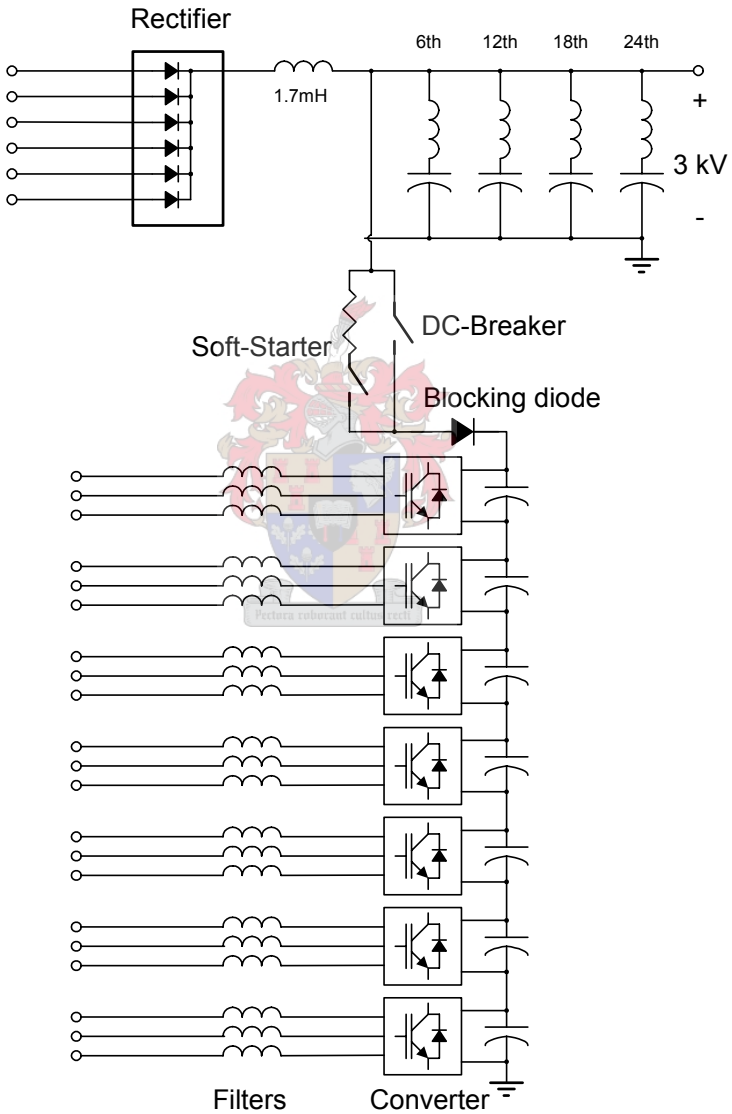


Figure 2.14 Diagram of the DC side connection

The soft-starter consists of a 407 Ω resistor in series with a small DC contactor. The soft start resistor limits the initial current when the soft-starter is switched on to 8.12 A. The DC-bus takes approximately 4 s to charge up to 3 kV. When the DC voltage of the converter reaches 3 kV, the main DC contactor is closed, where after the soft start contactor is opened.

The soft start sequence is controlled by the DSP controller and takes 4 s to complete. Once the DC-bus is charged and the main DC contactor is closed, the controller enables the PWM outputs and runs the controller algorithm.

2.6. The injection transformer and filter inductor

As can be seen in Figure 1.1, a special transformer is needed for the system. The secondary of the injection transformer mirrors the secondary of the main traction transformer. Thus for the installation at the Wolseley substation, a triple star connected, six-phase secondary winding is required. The primary of the injection transformer consists of seven three-phase windings, one three-phase winding for each converter level.

Figure 2.15 The Injection transformer

The transformer is designed with 21 inputs on the primary and six outputs on the secondary. The primary connects via the filter inductors to the seven level series-stacked inverter and the secondary to the 2420 V (line-to-line) supply lines. The three phase line-to-line and line-to-neutral voltages has the following relationship

$$V_{LL} = \sqrt{3} V_{LN} \tag{2.7}$$

While in the six-phase system the relationship is given by

$$V_{LL} = V_{LN} \tag{2.8}$$

The voltage relationship between the primary and the secondary of the transformer is thus given by (the injection transformer winding ratio, N = 10)

$$\begin{aligned} NV_{pLL} &= V_{sLL} \\ V_{pLL} &= \frac{V_{sLL}}{N} \\ V_{pLn} &= \frac{V_{sLL}}{\sqrt{3}N} \end{aligned} \tag{2.9}$$

The relationship between the 21 input and six output currents for the transformer for a resistive load is

$$I_s = \frac{7 I_p}{2\sqrt{3}N} \tag{2.10}$$

For a nonlinear load the current relationship changes to

$$I_s = \frac{I_p}{3N} \tag{2.11}$$

The 21 filter inductors are each 150 μH inductors and are connected directly to the injection transformer. No filter capacitors are used which means that the leakage inductance of the injection transformer is also used as part of the filter.

2.7. The AC circuit connection and measuring system

The seven three-phase outputs of the converter are summed through the injection transformer. The seven primary windings are isolated from each other since, each converter level has a different DC offset.

The secondary of the injection transformer has a six-phase output which connects to the six-phase supply feeding the rectifier as shown in Figure 2.16.

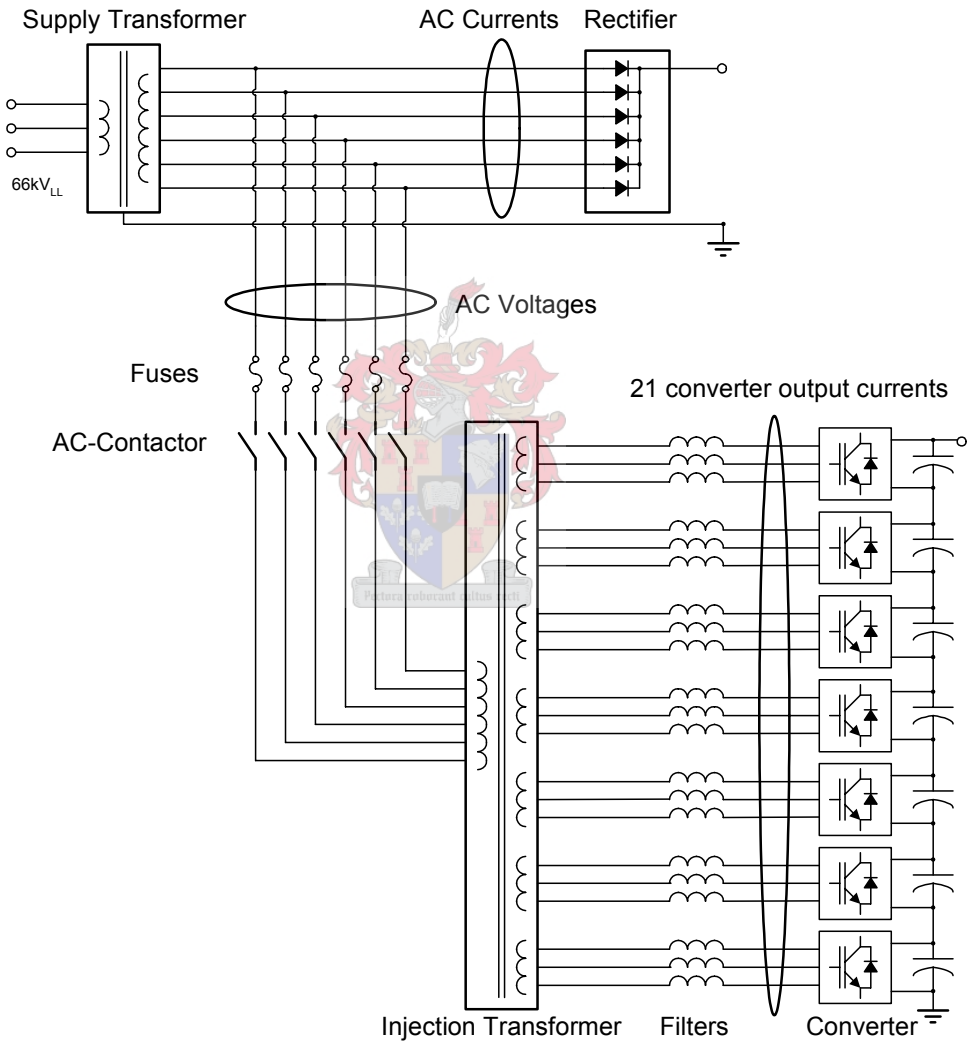


Figure 2.16 Diagram of the AC side connection and position of the measuring system.

The connection of the injection transformer's secondary to the six-phase supply is made via two three-phase AC contactors. The AC contactors are closed after the DC-bus of the converter has been connected to the 3 kV line. This is to avoid charging the capacitors from the AC side through the converter's free wheeling diodes. The six 400 A fuses are used as a last line of protection and are situated between the six-phase supply and the secondary of the transformer.

The AC measuring system and protection was designed by Heinrich Fuchs and is shown in Figure 2.16. On the supply side, the six currents feeding the rectifier are measured using Lem current probes [31]. The six line-to-line voltages are measured with high voltage Lem voltage probes. On the converter side, all 21 converter output currents are measured with Lem current probes. A Lem current probe also measures the DC current between the rectifier output and the systems DC-bus. The total DC-bus voltage as well as the DC voltages over the seven converter levels are measured.

2.8. The digital controller board

In order to control the system, a number of voltage and current measurements are taken and used to calculate the switching signals for the converter. The PEC 33 controller board used for the project was designed as a general purpose power electronic controller [23] and is shown in Figure 2.17. The analog current measurements and digital voltage measurements are read into the digital signal processor, DSP on the board. The DSP then runs through the control algorithm and computes the three-phase duty cycles for the converter.

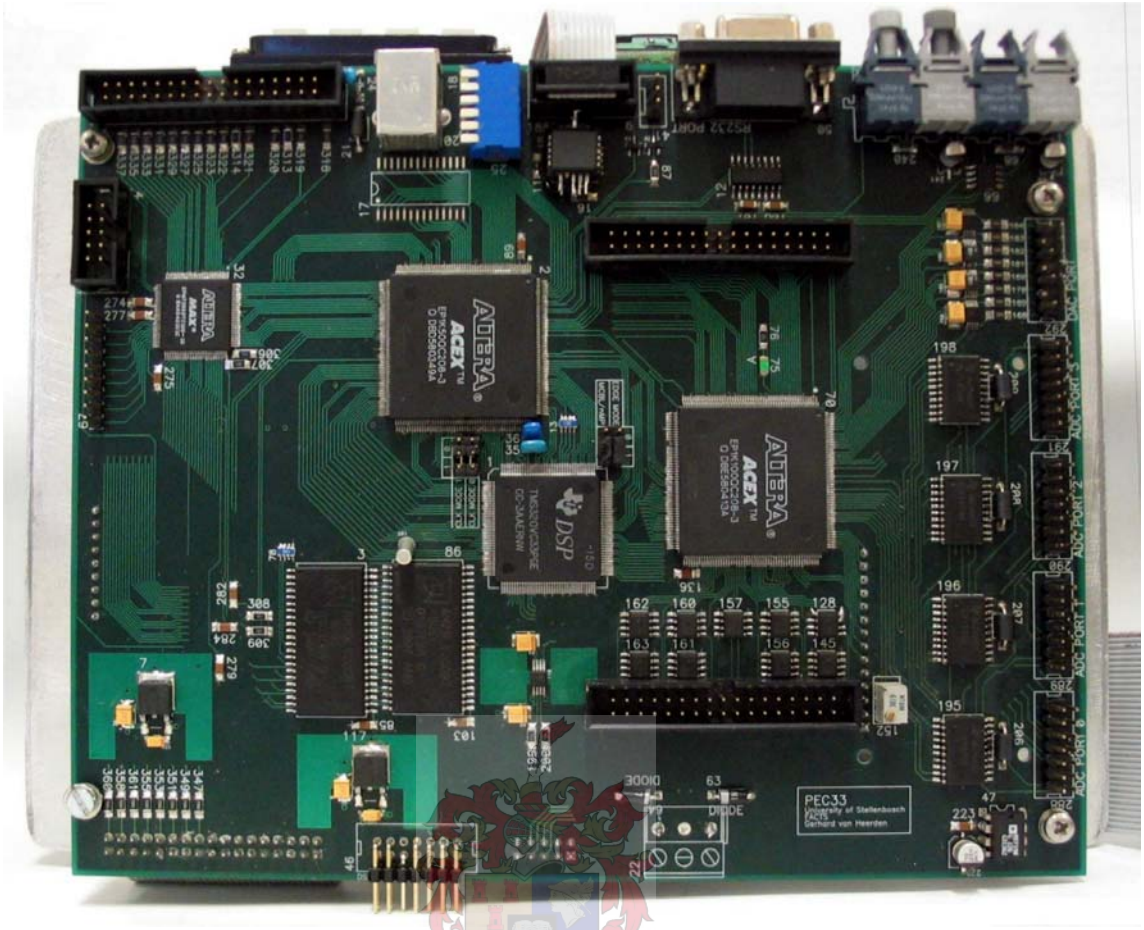


Figure 2.17 The PEC 33 controller board

The seven cells are switched in an interleaved fashion, to reduce harmonic content of the output voltage, which in turn reduces the strain on the injection transformer. The resulting equivalent switching frequency is 35 kHz. This means that although the individual cells only switch at frequency of 5 kHz, the duty cycles have to be computed every 28.57 µs instead of every 200 µs.

2.9. The PWM expansion board

The seven level series-stacked converter has a total of 42 switches that need to be controlled individually. Since the controller board does not have enough space in its FPGA or enough PWM outputs to address all the switches, the PWM expansion board and optical driver boards were developed.

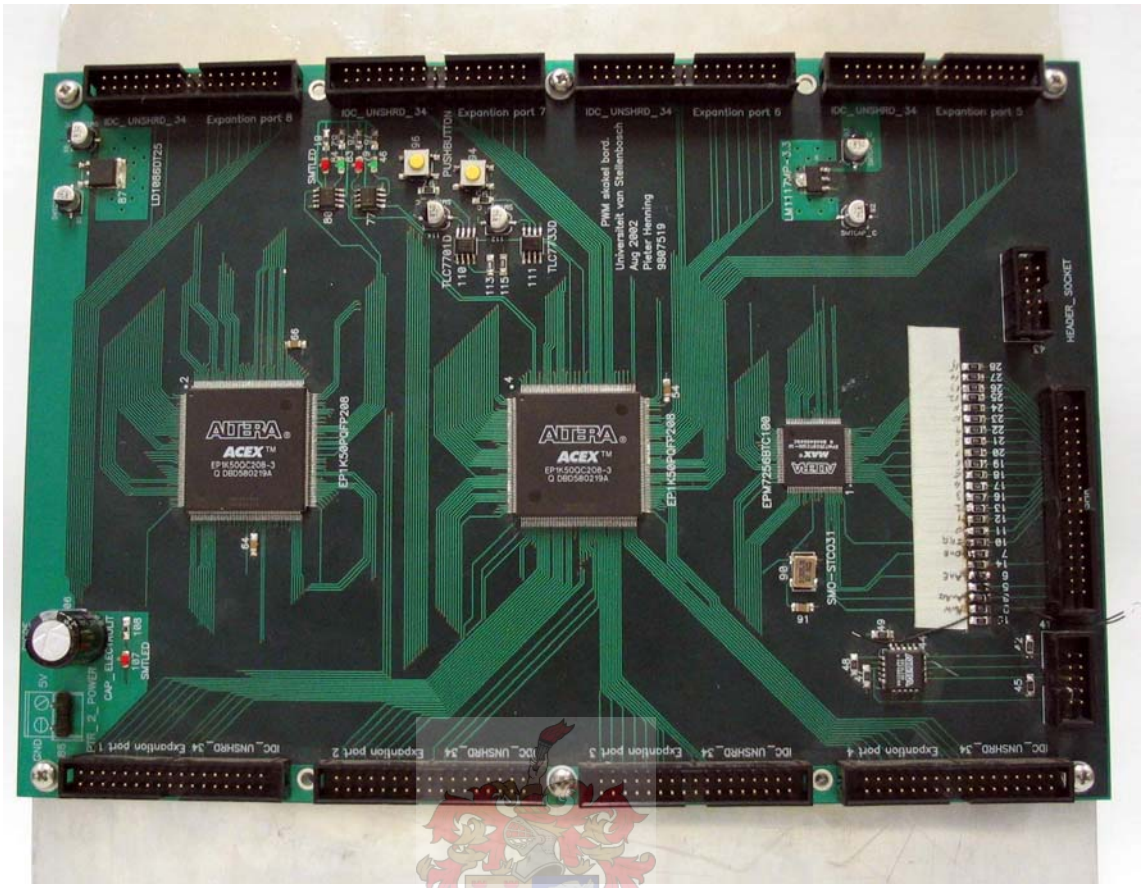


Figure 2.18 PWM expansion board

The expansion board receives the duty cycles calculated by the DSP, and then generates the PWM switching signals for the converters. Interleaving of the switching signals are also done by the expansion board. In addition the expansion board generates the switching signals for the AC contactor and DC contactor, the soft-starter, the cooling fans and the DC dump switches. The various error signals that need to be checked are also handled by the expansion board.

To keep the optical fibres that carry the switching and error signals manageable, eight optical driver boards connect to the PWM expansion board. Each driver board has enough optical drivers and receivers to control one converter level. The eighth driver board switches the contactors and relays that are not associated with an individual cell.

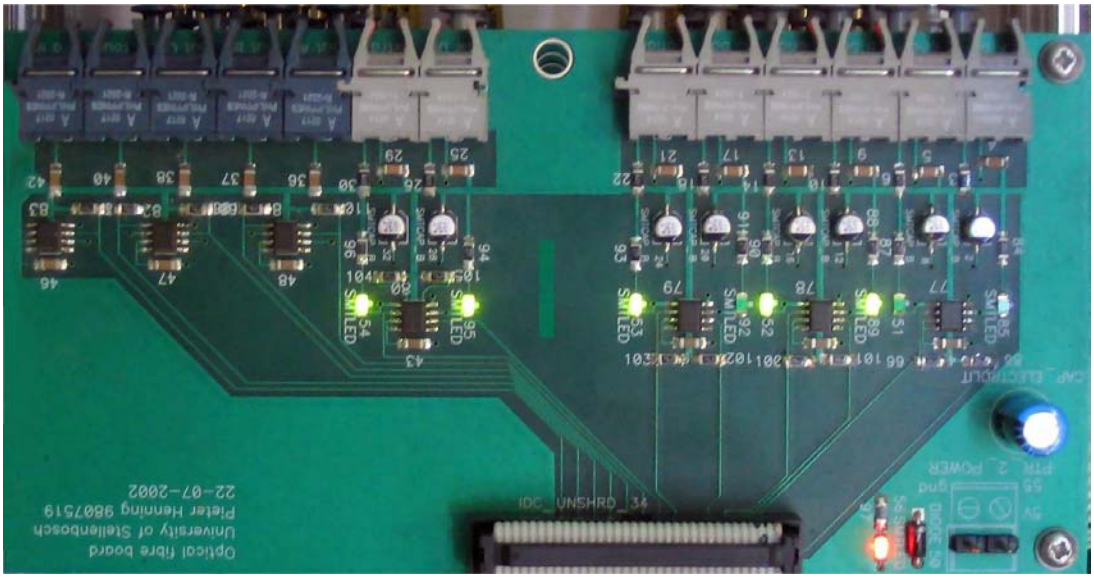


Figure 2.19 Optical driver board

2.10. An overview of the control strategy

In [24] various simulations were done to investigate the seven level series-stacked converter as well as different control strategies. Both the Instantaneous reactive power theory, introduced by H Akagi [1], and the Synchronous reference frame were evaluated as APF controllers. The Instantaneous reactive power theory was also investigated as APF controller in DC traction substation power conditioner in [2].

The control algorithm used for the Spoornet project consists of two parts that run simultaneously. The APF controller is based on the Instantaneous reactive power theory, while the second controller is a Lag compensator [5] that controls the converter's DC-bus voltage. The Lag compensator also generates the reference currents for the regeneration mode.

The transition between regeneration and active power filtering mode occurs automatically. When a train uses regenerative braking, the voltage on the 3 kV line rises and cause the rectifiers diodes to stop conducting. The AC current drawn from the supply becomes zero. Which cause the APF current references to become zero, thus leaving the control of the system to the Lag compensator.

3. The control strategy

This chapter introduces the Instantaneous reactive power theory and explains how it is used to control the active power filtering function of the system. The next section deals with the modelling of the converter system and the design of the Lag compensator, to control the DC-bus voltage. The chapter concludes with the calculation of the reference voltages and the use of space vector modulation, to generate the switching signals.

3.1. The active power filter control

The system is to function as an APF under normal conditions, which is when power is drawn from the Eskom supply through the diode rectifiers to power the 3kV DC-line. This filtering requires that the converter injects a current into the supply side, which would ideally neutralize the harmonic content of the current drawn by the rectifier.

The elementary operation of an APF is shown in Figure 3.1 where a compensation current is added to the uncompensated supply current which results in the filterd supply current.

By reducing the harmonic current component of the supply less strain is put on the power network. A reduction in the harmonic content of the supply current also decreases the electro magnetic interference (EMI) that is generated. High frequency harmonics in the supply current causes electromagnetic emissions that may interfere with sensitive equipment. As yet, there is no legislation that restricts the degree of distortion that a client is permitted to cause on the supply current. In [26], standards to limit the distortion that may be caused is proposed and this, or an adaptation on this, will likely be implemented in the near future. If such legislation is approved, active power filters would be indispensable to industry, especially to applications where passive rectifiers are used.

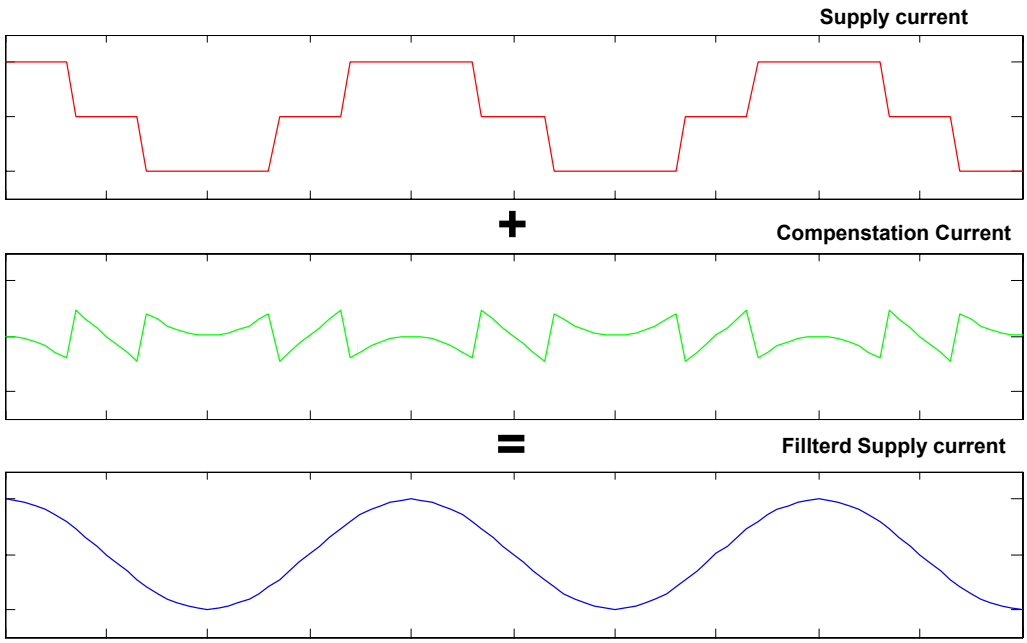


Figure 3.1 Basic APF functioning

3.1.1. Instantaneous reactive power compensation theory

The instantaneous reactive power theory was developed by H. Akagi et al. [1]. It is defined on the basis of the instantaneous values of arbitrary voltage and current waveforms in a three-phase system. The theory does not require an undistorted voltage (sinusoidal voltage) measurements or having a balanced system. [17]

This theory introduces instantaneous imaginary power (this is not the conventional imaginary power). Using this, the instantaneous reactive power can be uniquely defined for arbitrary three-phase voltage and current waveforms. In turn this is used to calculate the switching reference to compensate for the harmonic current.

The instantaneous three-phase voltage and current values are represented as instantaneous space vectors. These three-phase (a-b-c) voltages and currents are represented in a three-axis two-dimensional plane as shown in Figure 3.2, where the a, b and c axis are situated at 120° with respect to each other.

The three-phase equivalent instantaneous voltage vectors are calculated from the six-phase instantaneous voltage measurements as described in section 1.3.1.

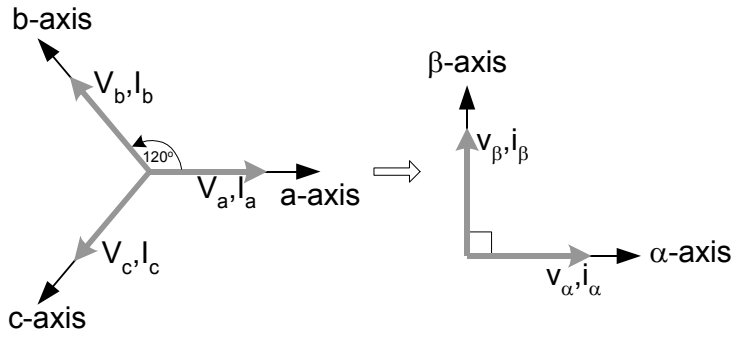


Figure 3.2 The instantaneous space vectors

Using the Clarke transform [17][34][35] these three-phase vectors are transformed to the orthogonal α-β-0 coordinate system.

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{3.1}$$

$$\begin{bmatrix} I_\alpha \\ I_\beta \\ I_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{3.2}$$

Since the load is balanced, and there is no neutral line, the system does not have a zero-sequence, V_0 and I_0 are thus equal to zero and the system equations simplify to

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{3.3}$$

$$\begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{3.4}$$

The conventional instantaneous power in a three-phase system is equal to the power the scalar or dot product of the vectors calculated in the α-β system.

$$p = v_\alpha \bullet i_\alpha + v_\beta \bullet i_\beta \qquad [W] \tag{3.5}$$

The instantaneous imaginary power is then introduced [1] as the cross product of the vectors. The result of the cross product is a vector perpendicular to the α-β plane. A third dimension, the imaginary axis, is added perpendicular to the α-β plane. This new instantaneous imaginary power is shown in Figure 3.3 and is defined by

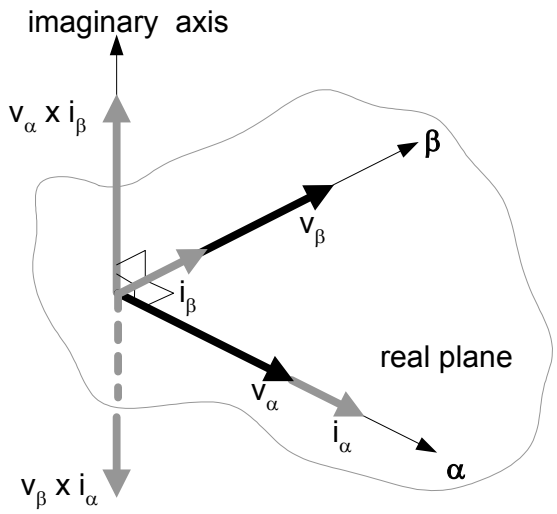


Figure 3.3 The introduced imaginary axis

$$q = v_\alpha \times i_\beta + v_\beta \times i_\alpha \tag{3.6}$$

equations (3.5) and (3.6) witch are written in matrix form as shown in equation (3.7). p is the conventional real power, with dimension [W]. Since q is defined as the product of an instantaneous voltage and current, that are not in the same axis it does not have a conventional dimension like W, VA or VAR.

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{3.7}$$

Equation (3.7) is inverted and manipulated to express the α and β currents in terms of their active and reactive components.

The α-axis instantaneous active current as

$$i_{\alpha p} = \frac{v_\alpha}{v_\alpha{}^2 + v_\beta{}^2} p \tag{3.8}$$

The α-axis instantaneous reactive current as

$$i_{\alpha q} = \frac{-v_\beta}{v_\alpha{}^2 + v_\beta{}^2} q \tag{3.9}$$

The β-axis instantaneous active current as

$$i_{\beta p} = \frac{v_\beta}{v_\alpha{}^2 + v_\beta{}^2} p \tag{3.10}$$

and the β-axis instantaneous reactive current as

$$i_{\beta q} = \frac{v_\alpha}{v_\alpha{}^2 + v_\beta{}^2} q \tag{3.11}$$

Using these representations of the α and β currents, the instantaneous power on the α and β axes can be written as

$$\begin{bmatrix} p_\alpha \\ p_\beta \end{bmatrix} = \begin{bmatrix} v_\alpha i_{\alpha p} \\ v_\beta i_{\beta p} \end{bmatrix} + \begin{bmatrix} v_\alpha i_{\alpha q} \\ v_\beta i_{\beta q} \end{bmatrix} \tag{3.12}$$

The sum of p_α and p_β is equal to the conventional instantaneous real power, p in a three-phase system.

$$\begin{aligned} p = p_\alpha + p_\beta = \frac{v_\alpha{}^2}{v_\alpha{}^2 + v_\beta{}^2} p + \frac{v_\beta{}^2}{v_\alpha{}^2 + v_\beta{}^2} p \\ + \frac{-v_\alpha v_\beta}{v_\alpha{}^2 + v_\beta{}^2} q + \frac{v_\alpha v_\beta}{v_\alpha{}^2 + v_\beta{}^2} q \end{aligned} \tag{3.13}$$

In equation (3.13) it can be seen that the third and fourth terms always sum to zero, thus instantaneous active powers, $p_{\alpha q}$ and $p_{\beta q}$ makes no contribution to the power flow between the source and the load. This means that the instantaneous real power in a three-phase system coincides with the sum of the instantaneous active powers, $p_{\alpha p}$ and $p_{\beta p}$

3.1.2. The control strategy

The active and reactive powers as calculated in equation (3.7) can be split into DC and AC values and written as

$$p = \bar{p} + \tilde{p} \tag{3.14}$$

and

$$q = \bar{q} + \tilde{q} \tag{3.15}$$

Where $\bar{p}$ and $\bar{q}$ are the DC active and reactive power while $\tilde{p}$ and $\tilde{q}$ are the AC active and reactive power [1].

Since the system has to compensate for the harmonic and reactive power drawn by the load, it has to eliminate the instantaneous reactive power, $\bar{q}$ and $\tilde{q}$ as well as the AC component of the instantaneous real power, $\tilde{p}$ [17].

The reference currents that are needed to achieve the required compensation are calculated by

$$\begin{bmatrix} i_{\alpha ref} \\ i_{\beta ref} \end{bmatrix} = \frac{1}{\left(v_\alpha{}^2 + v_\beta{}^2\right)} \begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} \tilde{p} \\ \bar{q} + \tilde{q} \end{bmatrix} \tag{3.16}$$

The α and β reference currents that the converter is required to realize are given by:

$$i_{\alpha ref} = \frac{v_\alpha}{v_\alpha{}^2 + v_\beta{}^2}\tilde{p} - \frac{v_\beta}{v_\alpha{}^2 + v_\beta{}^2}\bar{q} - \frac{v_\beta}{v_\alpha{}^2 + v_\beta{}^2}\tilde{q} \tag{3.17}$$

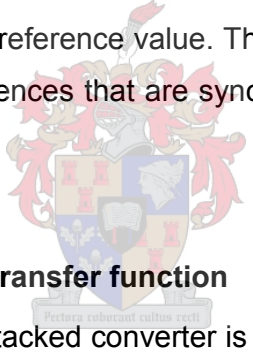
$$i_{\beta ref} = \frac{v_\beta}{v_\alpha{}^2 + v_\beta{}^2}\tilde{p} + \frac{v_\alpha}{v_\alpha{}^2 + v_\beta{}^2}\bar{q} + \frac{v_\alpha}{v_\alpha{}^2 + v_\beta{}^2}\tilde{q} \tag{3.18}$$

In both equations (3.17) and (3.18) the second term is the value of the conventional DC reactive current component, while the first and third terms are the AC component for the active and reactive components respectively.

3.2. The DC-bus voltage control

During the system operation, it is necessary to keep the DC-bus voltage at a predefined value. Reactive harmonic compensation and the interchange of the active harmonic currents do not require energy storage devices [1]. However, losses in the converter and the passive elements lead to power dissipation for which the capacitor banks provide the energy. This combined with the continuous charging and discharging of the capacitor banks due to calculation errors caused by time delays necessitates a DC-bus voltage controller.

To control the DC-bus voltage, a sinusoidal current component is added to APF reference current. The amplitude of the sinusoidal component is determined by using a Lag compensator. The compensator calculates a compensation current using a model of the system and the difference between the actual DC voltage that is measured and the predefined reference value. This compensation value is then used to scale three sinusoidal references that are synchronized with the three-phase line-to-neutral supply voltages.



3.2.1. Modeling the system transfer function

Since the seven level series-stacked converter is quite complicated to model, several simplifications and assumptions are made on the way to deriving a system transfer function.

Firstly the seven level of the series-stacked converter is assumed to be lossless. Thus the behavior of the system is comparable to that of a capacitor. The transfer function for a capacitor is given by

$$I_{DC} = C\frac{dV_{DC}}{dt} \tag{3.19}$$

Where C is the equivalent compensator capacitance, I_{DC} is the current through the capacitor and V_{DC} the voltage over the capacitor. Next an equivalent capacitor value

is calculated for the seven capacitor banks in series, each of which has a capacitance of 24mF. The equivalent capacitance is then

$$C_{eq} = \frac{C_{inv}}{7} = 3.43mF \tag{3.20}$$

As a lossless system, the input power must be equal to the output power, which leads to the average DC power being equal to the average AC power. The different power equations and system transformations are shown in Figure 3.4.

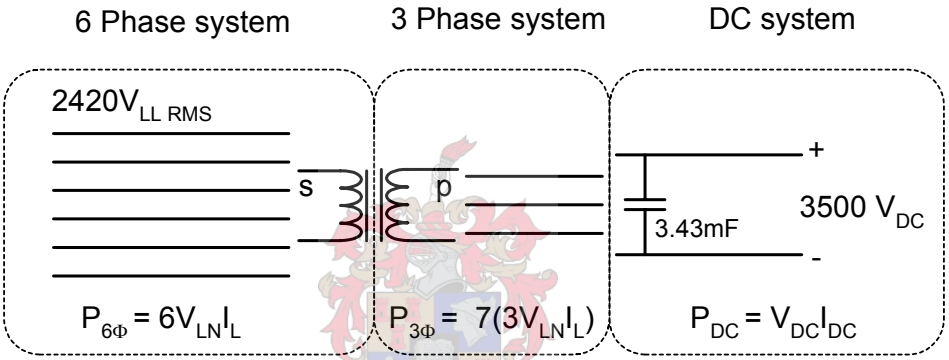


Figure 3.4 Power relationship between the different systems

The AC side is approximated for a six-phase sinusoidal supply with a unity power factor as

$$P_{6\phi} = 6V_{LNRMS}I_{LRMS} \tag{3.21}$$

And rewritten as in terms of peak line current as

$$P_{6\phi} = \frac{6V_{sLNRMS}\hat{I}_{sL}}{\sqrt{2}} \tag{3.22}$$

The subscript s indicates the currents and voltages on the secondary side of the injection transformer. The power equation on the DC side of the system is written as

$$\begin{aligned} P_{DC} &= V_{DC} I_{DC} \\ &= V_{DC} C_{eq} \frac{dV_{DC}}{dt} \end{aligned} \tag{3.23}$$

where V_{DC} is the sum of V_{dc}, the DC working point and $\tilde{V}_{dc}$, the small variance around the working point as shown in equation (3.24).

$$V_{DC} = V_{dc} + \tilde{V}_{dc} \tag{3.24}$$

Since the AC power must be equal to the DC power, equation (3.22) and (3.23) combined and rewritten as

$$\begin{aligned} V_{DC} C_{eq} \frac{dV_{DC}}{dt} &= \frac{6 V_{sLNRMS} \hat{I}_{sL}}{\sqrt{2}} \\ \frac{d\left(V_{dc} + \tilde{V}_{dc}\right)}{dt} &= \frac{6 V_{sLNRMS} \hat{I}_{sL}}{\sqrt{2}\left(V_{dc} + \tilde{V}_{dc}\right) C_{eq}} \end{aligned} \tag{3.25}$$

Where V_{sLNRMS} and $\hat{I}_{sL}$ are the RMS value of the six-phase AC supply, line-to-neutral voltage and the peak value of the line current respectively. Since $V_{dc} \gg \tilde{V}_{dc}$ and the working point, V_{dc}, is a constant, equation (3.25) becomes.

$$\frac{d\tilde{V}_{dc}}{dt} = \frac{6 V_{sLNRMS}}{\sqrt{2} C_{eq} V_{dc}} \hat{I}_{sL} \tag{3.26}$$

And this is then written in the Laplace domain as

$$\tilde{V}_{dc} = \frac{6 V_{sLNRMS}}{\sqrt{2} s C_{eq} V_{dc}} \hat{I}_{sL} \tag{3.27}$$

The final step in determining the transfer function of the system is to write the equation in terms of a single-phase line current magnitude on the primary of the injection transformer. In other words, a single-phase line current output of the inverter. This is done since the DC compensation current is calculated every 28.57μs

along with the APF reference current, which is then combined to form the switching reference for a single inerter level. The current relationship between the secondary and the primary of the injection transformer is given in equation (2.10), thus equation (3.27) becomes

$$\tilde{V}_{dc} = \frac{6V_{sLNRMS}}{4.83\sqrt{2}sC_{eq}V_{dc}}\hat{I}_{pL} \tag{3.28}$$

With V_{sLNRMS} = 2420V and V_{dc} = 3500V transfer function of the system is

$$\tilde{V}_{dc} = \frac{172.9}{s}\hat{I}_{pL} \tag{3.29}$$

3.2.2. Designing a Lag compensator

The main characteristics that are required from the compensator is that it increases the low frequency gain, thus reducing the steady state error, while not changing the high frequency behavior and thus not interfering with the filtering operation of the converter.

A Lag compensator was chosen to control the DC-bus voltage because of its suitable characteristics [5]. A block diagram of the closed loop system including the Lag compensator is shown in Figure 3.5

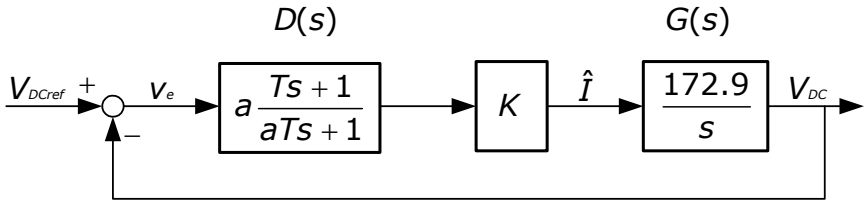


Figure 3.5 Block diagram of the Lag compensator and the converter system

The gain K is chosen so that the bandwidth is set to 100 Hz, which is low enough not to interfere with the converter's filtering operation.

The transfer function of the Lag compensator is given by

$$D(s) = \left(a \frac{Ts + 1}{aTs + 1} \right) K \tag{3.30}$$

To ensure sufficient low-frequency gain, the pole of the compensator must have a lower break-point than the zero. To do this, the value of a must be greater than 1. Further, T is chosen so that the corner frequency is a decade lower than the minimum frequency component on the DC system, ω_{min} = 30 Hz. The design is done using Matlab, first the bode plot of the system is drawn, then a constant gain K is added so that the crossover frequency is at 100 Hz or 628.3 rads^{-1}. The open loop bode plots of the system with and without the gain K = 3.7 is shown in Figure 3.6

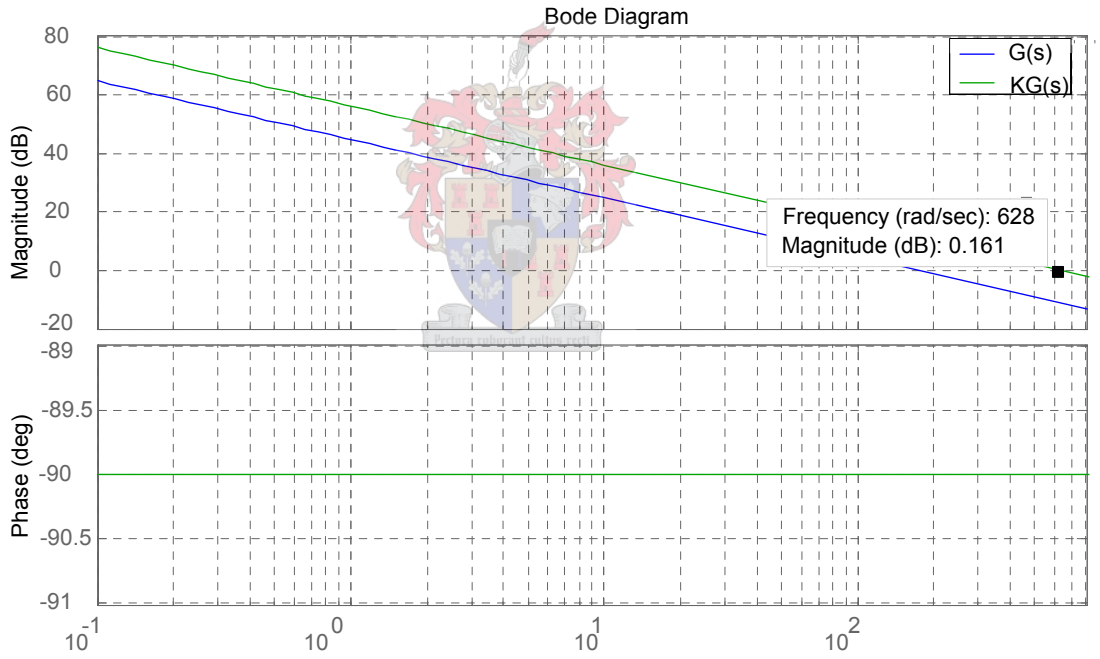


Figure 3.6 The open loop bode plot for the system with and without K

The bode plots of the original system, the system with a constant gain K and the system with the Lag compensator is shown in Figure 3.7.

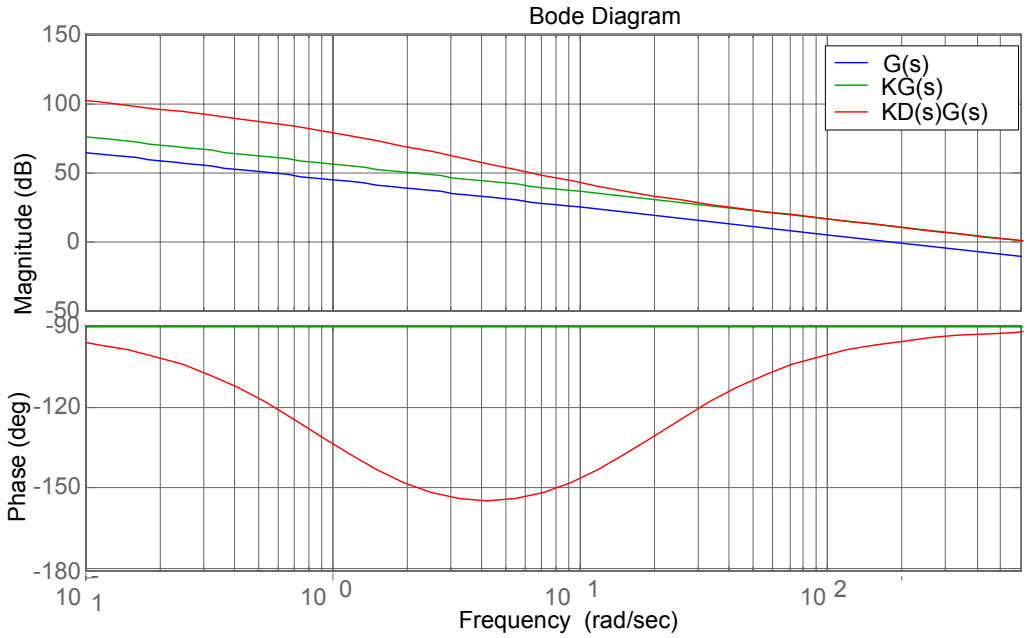


Figure 3.7 The bode plot of the system with the Lag compensator

The resulting closed loop step response of the system with and without the compensator is shown in Figure 3.8

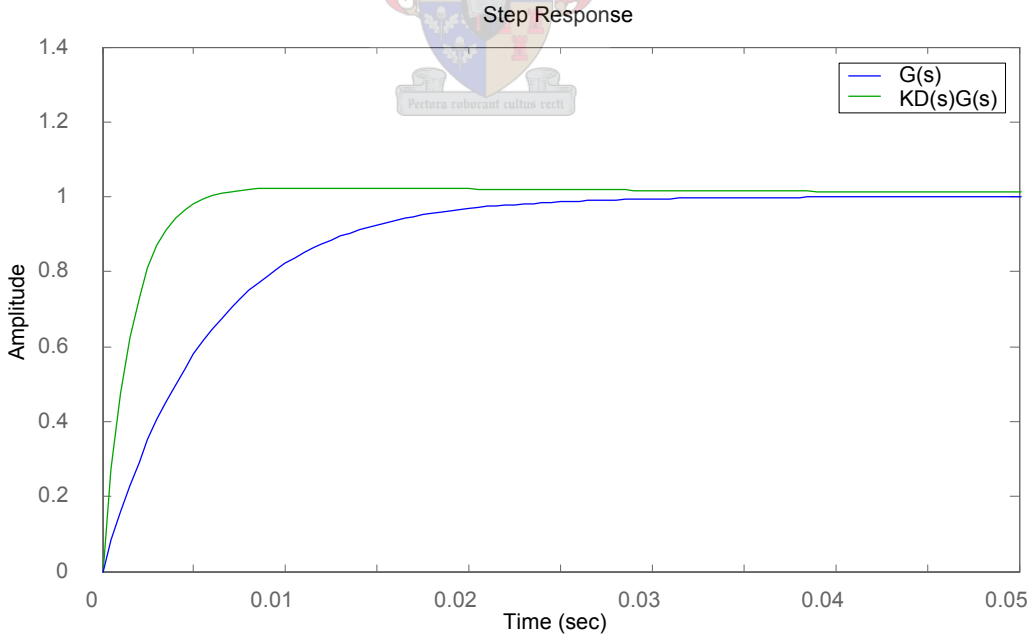


Figure 3.8 The step response for the system with and without the Lag compensator

To obtain adequately low-frequency gain and leave a sufficient phase margin at the desired crossover frequency of the system $T = \frac{10}{\omega_{\min}}$, a is set to 20.

The resulting Lag compensator is thus given by equation (3.31) as

$$KD(s) = \left(\frac{3.926s + 74}{1.061s+1} \right) \tag{3.31}$$

Since the control is to be implemented in a DSP, equation (3.31) is transformed to the discrete z domain.

$$\frac{\hat{I}}{V_e} = \frac{3.707 - 3.693z^{-1}}{1 - 0.9998z^{-1}} \tag{3.32}$$

where V_e is the error between the reference and measured voltage. Equation (3.32) is then rewritten in terms of sampled values as

$$\hat{I}(k) = 0.9998\hat{I}(k-1) + 3.707V_e(k) - 3.693V_e(k-1) \tag{3.33}$$

This reference current, $\hat{I}(k)$, is the amplitude of the current that the converter needs to switch in order to regulate the DC-bus voltage. This current amplitude is multiplied with three unity sinusoidal phase references to give the AC current reference that the converter must generate to regulate the DC-bus voltage.

3.3. Extracting the sinusoidal synchronization reference signals

Three sinusoidal synchronization reference currents have to be used in order to complete the DC-bus control algorithm. These sinusoidal references are extracted from the AC voltage measurements, using a Fourier based method rather than a zero-cross detection method. The latter method is prone to cause false synchronization since the technique is very sensitive to disturbances especially with small measurement values. [12] In general the Fourier series is given by

$$f(t) = \frac{A_0}{2} + \sum_{n=0}^{\infty} [A_n \cos((2\pi f)nt) + B_n \sin((2\pi f)nt)] \tag{3.34}$$

Where f is the frequency, t is time, and A_n and B_n are the Fourier coefficients calculated using Euler's formulas, given here for a fixed integration window [25].

$$A_n(t) = \frac{2}{T} \int_{t-T}^{t} f(x)\cos(\omega_n x)dx \tag{3.35}$$

$$B_n(t) = \frac{2}{T} \int_{t-T}^{t} f(x)\cos(\omega_n x)dx \tag{3.36}$$

Since we are only interested in the 50 Hz frequency component, the length of the integration window, T, is set to one 50 Hz cycle as shown in Figure 3.9

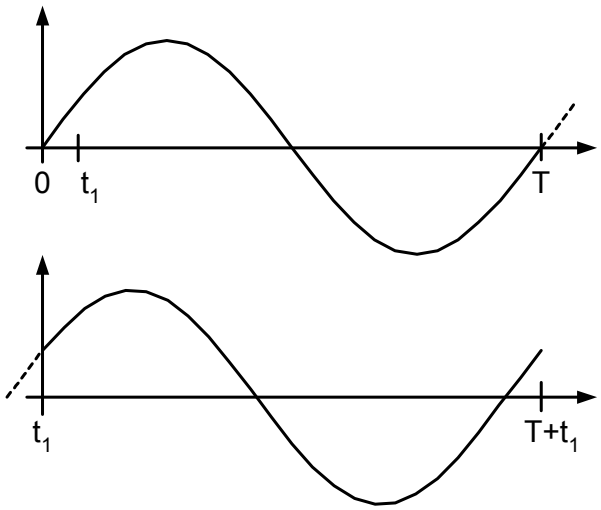


Figure 3.9 Diagram to illustrate how the Fourier coefficients are updated

Keeping in mind that the integration window length is fixed, we consider a time change, where t is replaced with $t+t_1$.

$$\begin{aligned} A_n(t+t_1) &= \frac{2}{T}\int_{t+t_1-T}^{t+t_1} f(x)\cos(\omega_n x)dx \\ &= -\frac{2}{T}\int_{t-T}^{t+t_1-T} f(x)\cos(\omega_n x)dx + \frac{2}{T}\int_{t-T}^{t} f(x)\cos(\omega_n x)dx \\ &\quad + \frac{2}{T}\int_{t}^{t+t_1} f(x)\cos(\omega_n x)dx \\ &= -\frac{2}{T}\int_{t-t_1-T}^{t-T} f(x)\cos(\omega_n x)dx + A_n(t) + \frac{2}{T}\int_{t}^{t+t_1} f(x)\cos(\omega_n x)dx \end{aligned} \tag{3.37}$$

As shown in equation (3.37) and illustrated in Figure 3.9, the Fourier constants can be updated over a short interval. This is done by subtracting the interval shown by the dotted line, which falls outside the integration bracket from the Fourier coefficient and adding the contribution made by the interval shown from time T, to $T+t_1$. In a digital implementation, a single sampling period would correspond to this integration interval.

Since the Fourier coefficients are only summed over one cycle, the window within which the fundamental is extracted is “broad”. This makes it possible for the system to synchronize to the supply voltages even if the supply frequency varies slightly.

The Fourier based synchronization method is implemented in the DSP. During one 50 Hz cycle, the procedure calculating the references is called seven hundred times, since the procedure is called every 28.57 µs. Thus each array in the look up table consists of seven hundred elements and is set up in such a manner that it loops back to the first one once the end of the array is reached. There are the A and B Fourier coefficient arrays, which are initialized as zeros. The 50 Hz sine and cosine arrays for each of the three-phase voltages are defined, where the phase A waveforms lead that of phase B by 120º and the waveform of phase C by 240º. The sine and cosine waveforms are initiated when the DSP starts up and says fixed.

Since the voltage measurements available are of the six-phase line-to-line voltages they are transformed to their equivalent three-phase line-to-neutral voltages using equations (1.1),(1.2) and (1.3). The calculations are simplified by combining the three-phase voltage measurements, to give weighted average Fourier constant, for a balanced three-phase system. The result yields the maximum power factor for the balanced three-phase system. The contribution made by a single integration interval is now

$$\begin{aligned} A(t+t_1) &= V_a\cos(\omega_a t)+V_b\cos(\omega_b t)+V_c\cos(\omega_c t) \\ B(t+t_1) &= V_a\sin(\omega_a t)+V_b\sin(\omega_b t)+V_c\sin(\omega_c t) \end{aligned} \tag{3.38}$$

Since the extracted sinusoids are normalized, the constant multiplication factor can be ignored. The three synchronization reference signals are then constructed as

$$A_{Sync} = A(t)\cos(\omega_a t)+B(t)\sin(\omega_a t) \tag{3.39}$$

$$B_{Sync} = A(t)\cos(\omega_b t)+B(t)\sin(\omega_b t) \tag{3.40}$$

$$C_{Sync} = A(t)\cos(\omega_c t)+B(t)\sin(\omega_c t) \tag{3.41}$$

and normalized before being scaled by the DC-bus control reference calculated by the Lag compensator.

3.4. The Implementation of the control strategies

Before the duty cycles needed to switch the converter can be calculated, the two reference currents have to be combined. The combined current is then used to calculate the voltage that has to be produced by the converter in order to realize the current references.

3.3.1. Combining the reference currents

The reference currents, calculated to do the filtering, are scaled by the injection transformer's winding ratios. The scaled values are then divided by seven to give the current that has to be switched by each converter. The reference currents for the DC-bus control are then subtracted from the scaled APF currents. The resulting currents are used to compute the reference voltages.

3.4.1. Determining the reference voltages

For the converter to track the current reference, a voltage reference has to be computed. This is done in the α-β plane, by calculating the voltage induced over the filter inductor by a changing current.

$$V_{ref} = L\frac{di_{ref}}{dt} \tag{3.42}$$

The differential part of equation (3.42) is done by subtracting the measured current through the inductor from the required current value and then dividing that by the switching time, as shown in Figure 3.10. The resulting voltage is added to the supply voltage, which is scaled by the injection transformer's winding ratios.

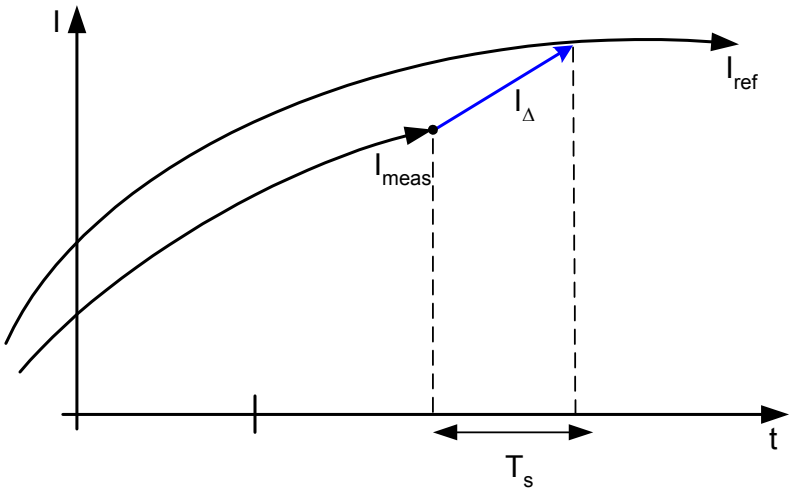


Figure 3.10 Figure showing the calculation of $\frac{di}{dt}$

$$V_{ref} = L\frac{i_{ref} - i_{meas}}{t_{sw}} + V_{emf} \tag{3.43}$$

The resulting α and β reference voltages, $V_{\alpha ref}$ and $V_{\beta ref}$ are then used in the space vector modulation technique to calculate the most efficient switching sequence.

3.4.2. Generating the Space Vector PWM duty cycles

Since the controller is implemented in a DSP, digital references are calculated, thus implementing a digital pulse width modulator is made straightforward. The FPGA implements symmetrical PWM to generate the switching signals. Symmetrical and asymmetrical PWM methods also known as sample and hold modulation as well as natural or analog PWM is are illustrated in Figure 3.11. [7][21]

Although asymmetric PWM reduces low order harmonics to a greater extent than symmetric PWM [21], the controller needs to update the reference twice in each switching cycle. Since calculation time is extremely limited, having to compute seven references during the 5 kHz period, symmetric PWM had to be implemented.

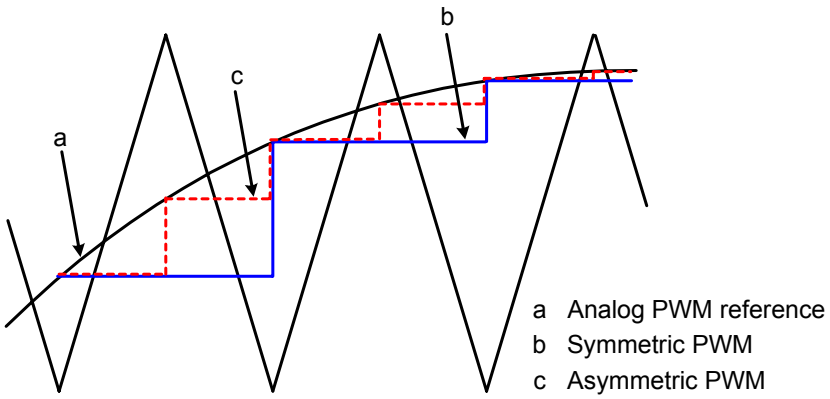


Figure 3.11 An illustration of the differences between symmetric and Asymmetric PWM

The PWM which is implemented in the FPGA, which ultimately generates the gating signals for the IGBTs. The duty cycles used for the symmetrical PWM in the FPGA is constructed using space vector PWM in order to optimise the IGBT switching sequence.

Optimum pulse width modulation is expected when the deviation of the current vector for several switching states is minimal and cycle times as short as possible. This is achieved if only the four switching states adjacent to the reference vector are used and the reference vector is constructed out of successive switching states [22]. The DSP uses the α-β reference voltages and space vector modulation to optimise the switching states.

A three-phase converter has eight valid switching combinations, when the top and bottom IGBTs are switched complementary [4][22]. In other words the top and bottom IGBT of a phase are never both on or both off. These states are shown in Table 3.1, where a 1 indicates that the top IGBT is on and the bottom IGBT is off, while a 0 indicates that the top IGBT is off and the bottom IGBT is conducting.

Table 3.1 The eight switching states

Switching state	Voltage vector	Phase		
		A	B	C
0	$\mathbf{V_0}$	0	0	0
1	$\mathbf{V_1}$	1	0	0
2	$\mathbf{V_2}$	1	1	0
3	$\mathbf{V_3}$	0	1	0
4	$\mathbf{V_4}$	0	1	1
5	$\mathbf{V_5}$	0	0	1
6	$\mathbf{V_6}$	1	0	1
7	$\mathbf{V_7}$	1	1	1

When the voltages that result are transformed to the α-β plane it translates into two zero voltage vectors and six voltage vectors of finite length.

$$\begin{aligned} &\left|\bar{V}_1\right| = \left|\bar{V}_2\right| = \left|\bar{V}_3\right| = \left|\bar{V}_4\right| = \left|\bar{V}_5\right| = \left|\bar{V}_6\right| = \sqrt{\frac{2}{3}} V_{DC} \\ &\left|\bar{V}_0\right| = \left|\bar{V}_7\right| = 0V \end{aligned} \tag{3.44}$$

These space vectors divide the α-β plane into six sectors as shown in Figure 3.12. A reference voltage lying inside any sector can be made up out of the two vectors, defining the sector's boundaries and the two zero voltage vectors. Reference vectors which extend past the circular border of a sector, shown in Figure 3.12, are scaled down to lie on the edge of the circle. The circle shows region wherein the converter is always capable of producing the required output voltage.

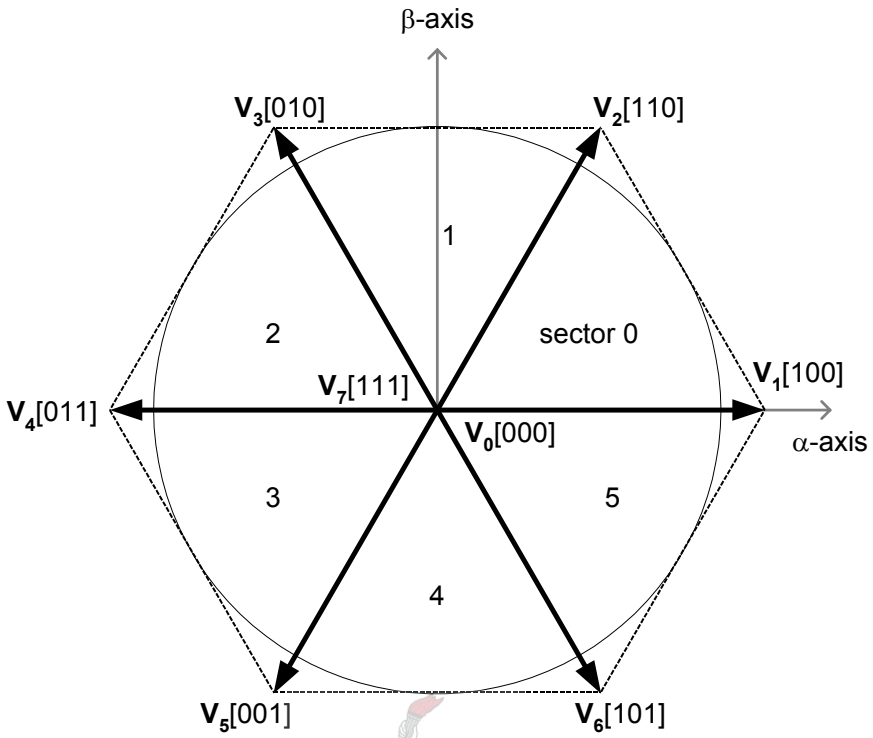


Figure 3.12 The eight voltage vectors and the 6 sectors

The radius of the circle is calculated using equation (3.48) witch is derived from Figure 3.13, which shows that the shortest vector that lies inside the sector is found 30º above the α-axis.

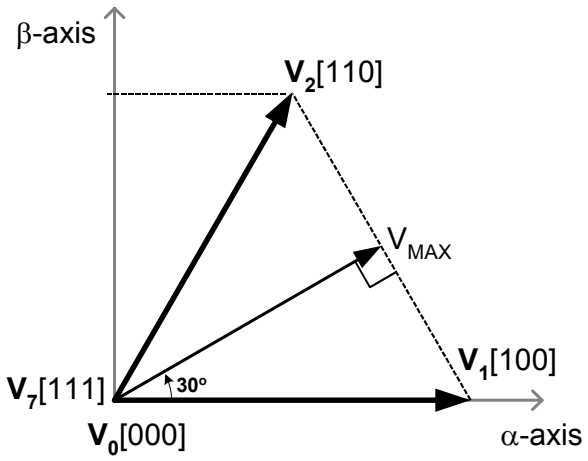


Figure 3.13 Calculating the maximum output voltage

$$
\begin{aligned}
V_{max} &= V_1 \cos(30°) \\
&= \sqrt{\frac{2}{3}} V_{DC} \cos(30°) \\
&= \frac{1}{\sqrt{2}} V_{DC}
\end{aligned}
\tag{3.45}
$$

Bearing the above mentioned constraints in mind, the sector wherein the required voltage reference lies, has to be established in order to determine the necessary switching sequence. With the reference vector, $V_{\alpha ref}$ and $V_{\beta ref}$ known, it is simple to determine in which sector the resultant vector lies, as shown in Figure 3.14

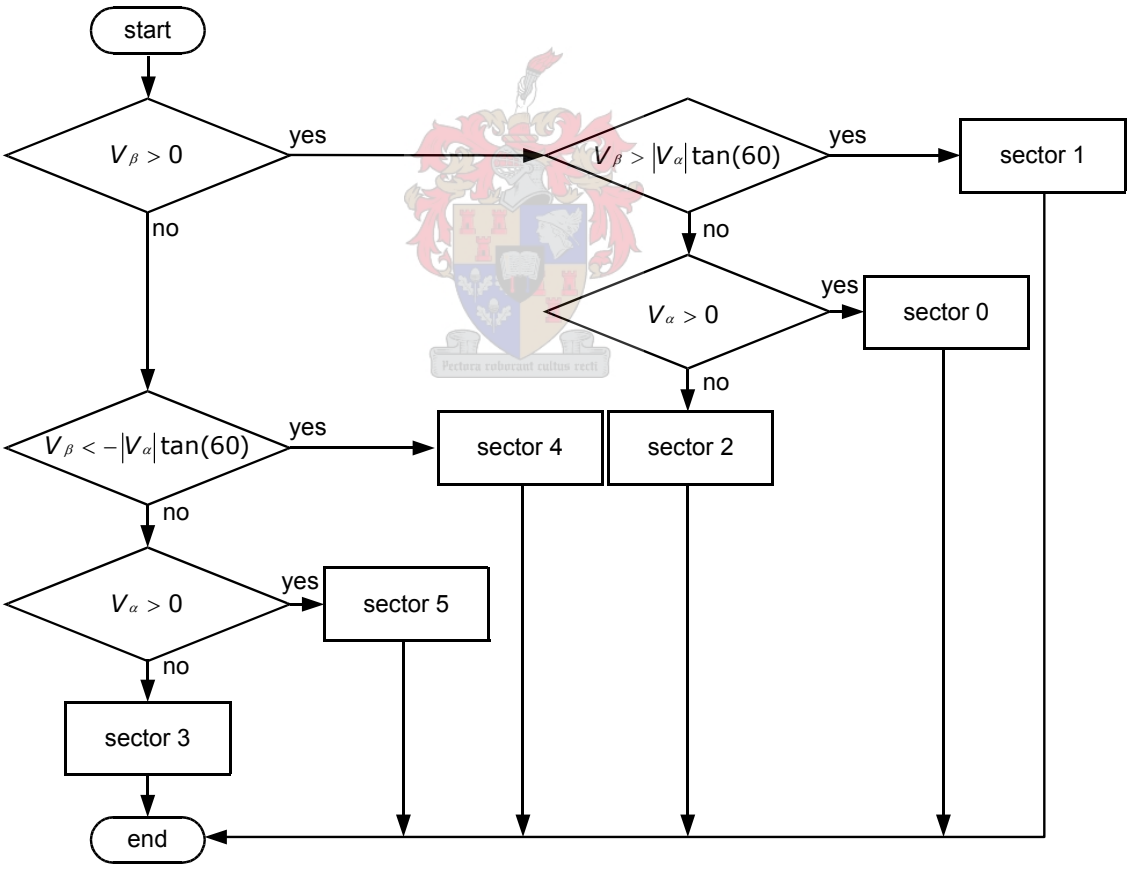


Figure 3.14 Flow diagram of how switching sectors are determined

Having determined in which sector the reference lies, the duty cycles can be calculated. For each voltage vector, $\mathbf{V}_x$ a duty cycle d_x is assigned and calculated. Figure 3.15 shows how the duty cycles are computed for a resultant voltage vector that lies in sector 0.

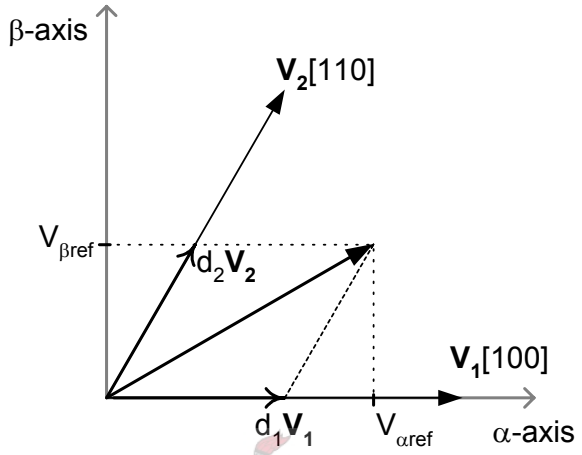


Figure 3.15 Calculating the duty cycles in sector 0

The boundaries of sector 0 are defined by $\mathbf{V}_1$ and $\mathbf{V}_2$, thus while V_{ref}, lies in sector 0, it can be made up out of $\mathbf{V}_1$, $\mathbf{V}_2$ and the two zero vectors $\mathbf{V}_0$ and $\mathbf{V}_7$.

From Figure 3.15:

$$d_1\|V_1\| = V_{\alpha ref} - \frac{V_{\beta ref}}{\tan(60°)} \tag{3.46}$$

and

$$d_2\|V_2\| = \frac{V_{\beta ref}}{\sin(60°)} \tag{3.47}$$

With the voltage vector lengths as given in equation(3.45), d_1 in equation (3.46) reduces to

$$d_1 = \frac{\sqrt{\frac{2}{3}}V_{\alpha ref} - \frac{1}{\sqrt{2}}V_{\beta ref}}{V_{DC}} \tag{3.48}$$

and similarly from equation (3.48) d_2 is reduced to

$$d_2 = \sqrt{2}\frac{V_{\beta ref}}{V_{DC}} \tag{3.49}$$

Next d_1 and d_2 are added together, and if the result is greater than one, the duty cycles are scaled so that the scaled values add to one. If the sum is less than one, the two zero vectors are introduced to make up the difference.

Table 3.2 Duty cycle relationships for sector 0

Duty cycle	Voltage vector	Phase		
		A	B	C
$\frac{d_0}{2}$	$\mathbf{V}_0$	0	0	0
d_1	$\mathbf{V}_1$	1	0	0
d_2	$\mathbf{V}_2$	1	1	0
$\frac{d_0}{2}$	$\mathbf{V}_7$	1	1	1

Using Table 3.2, the duty cycles for the each phase of the three-phase inverters are constructed as the sum of the duty cycles that has a 1 in the corresponding column of the phase in question. The duty cycles for sector 0 are thus:

$$\begin{aligned} D_A &= d_1 + d_2 + \frac{d_0}{2} \\ D_B &= d_2 + \frac{d_0}{2} \\ D_C &= \frac{d_0}{2} \end{aligned} \tag{3.50}$$

In a similar way, the duty cycles are calculatged for the other five sectors. By constructing the duty cycles in this way, the optimal switching sequences can be exploited as shown in Figure 3.16. As can be seen, only one switching transition is made at a time. Further more, a switching state will only change to an adjacent state.

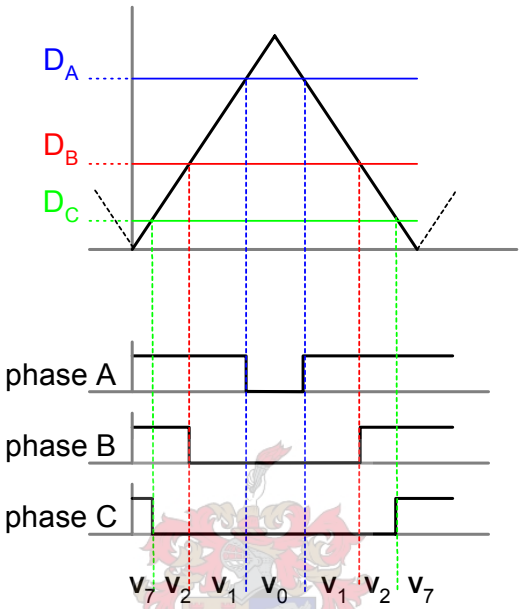


Figure 3.16 Diagram showing the PWM output and resulting voltage vector sequence.

Similar to the way equations (3.48) and (3.49) are derived for sector 0, the corresponding duty cycle equations for the other five sectors are calculated and listed in Table 3.3

Table 3.3 The duty cycles for the different sectors

Sector 1:	$d_2 = \frac{\frac{V_{\beta ref}}{\sqrt{2}} + \sqrt{\frac{3}{2}} V_{\alpha ref}}{V_{DC}}$	(3.51)
	$d_3 = \frac{\frac{V_{\beta ref}}{\sqrt{2}} - \sqrt{\frac{3}{2}} V_{\alpha ref}}{V_{DC}}$	(3.52)
Sector 2:	$d_3 = \frac{\sqrt{2} V_{\beta ref}}{V_{DC}}$	(3.53)
	$d_4 = \frac{-\sqrt{\frac{3}{2}} V_{\alpha ref} - \frac{V_{\beta ref}}{\sqrt{2}}}{V_{DC}}$	(3.54)
Sector 3:	$d_5 = \frac{-\sqrt{2} V_{\beta ref}}{V_{DC}}$	(3.55)
	$d_4 = \frac{-\sqrt{\frac{3}{2}} V_{\alpha ref} + \frac{V_{\beta ref}}{\sqrt{2}}}{V_{DC}}$	(3.56)
Sector 4:	$d_5 = \frac{\frac{-V_{\beta ref}}{\sqrt{2}} - \sqrt{\frac{3}{2}} V_{\alpha ref}}{V_{DC}}$	(3.57)
	$d_6 = \frac{\frac{-V_{\beta ref}}{\sqrt{2}} + \sqrt{\frac{3}{2}} V_{\alpha ref}}{V_{DC}}$	(3.58)
Sector 5:	$d_1 = \frac{\sqrt{\frac{3}{2}} V_{\alpha ref} + \frac{V_{\beta ref}}{\sqrt{2}}}{V_{DC}}$	(3.59)
	$d_6 = \frac{-\sqrt{2} V_{\beta ref}}{V_{DC}}$	(3.60)

For each of the six sectors, their corresponding three-phase duty cycles are constructed in the same way as shown for sector 0 and are listed in Table 3.4

Table 3.4 The three-phase duty cycle relationships for each sector

Sector 1:	$D_A = d_2 + \frac{d_0}{2}$ $D_B = d_2 + d_3 + \frac{d_0}{2}$ $D_C = \frac{d_0}{2}$	(3.61)
Sector 2:	$D_A = \frac{d_0}{2}$ $D_B = d_3 + d_4 + \frac{d_0}{2}$ $D_C = d_4 + \frac{d_0}{2}$	(3.62)
Sector 3:	$D_A = \frac{d_0}{2}$ $D_B = d_4 + \frac{d_0}{2}$ $D_C = d_4 + d_5 + \frac{d_0}{2}$	(3.63)
Sector 4:	$D_A = d_6 + \frac{d_0}{2}$ $D_B = \frac{d_0}{2}$ $D_C = d_5 + d_6 + \frac{d_0}{2}$	(3.64)
Sector 5:	$D_A = d_6 + \frac{d_0}{2}$ $D_B = \frac{d_0}{2}$ $D_C = d_5 + d_6 + \frac{d_0}{2}$	(3.65)

The resulting voltage vector switching sequences are listed in Table 3.5 for each of the six sectors.

Table 3.5 Optimal switching sequences for the six sectors

Sector	Switching sequence
0	...0127210...
1	...0327230...
2	...0347430...
3	...0547450...
4	...0567650...
5	...0167610...

3.4.3. Generating the interleaved switching signals

The system consists of seven three-phase converters with their DC-busses connected in series, thus forming a series-stacked converter. The simplest way to generate the switching signals, is to send the same switching signal to all seven converter levels. An alternative way is to generate individual switching signals, shifted in time, for each of the seven converter levels. This is referred to as interleaved switching.

The method used to generate interleaved switching signals is shown for a single-phase of a three level converter in Figure 3.17. Each of the three levels has its own triangular carrier, which is compared with a duty cycle reference. These triangular carriers are equally spaced in time and the duty cycle for a level is updated each time the triangular carrier of the corresponding level reaches zero.

Figure 3.17 shows that while the duty cycle, D_A, is greater than the triangular carrier, the top IGBT of the corresponding level will be switched on. Similarly, while the duty cycle is less than the triangular carrier, the bottom IGBT of the corresponding level will be switched on.

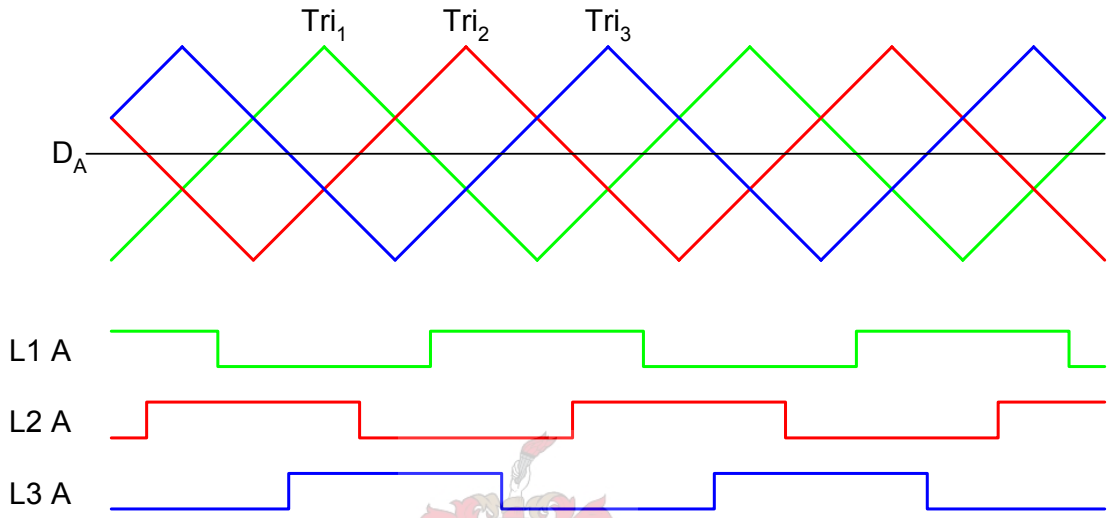


Figure 3.17 Diagram showing three interleaved PWM outputs

In the Spoornet system, seven converters are switched using interleaved switching. Thus seven triangular carriers, each having a frequency of 5 kHz and shifted in time by 28.57 µs are generated,

The PWM is done by a FPGA on the expansion board that connects to the PEC 33 controller via the external data bus. The FPGA contains 21 PWM blocks, one block for each phase arm on a converter. Thus there are three PWM blocks for each converter level. For a specific inverter level, each of the three PWM bocks, receives an unique duty cycle which is compared to the appropriate triangular carrier. The duty cycles for a particular level are updated each time the triangular carrier for that level reaches zero.

4. Simulations

This chapter discusses the computer aided simulations done, in order to investigate the converter topology, control strategy and evaluate three different switching approaches.

The simulation setup is shown in Figure 4.1. The system consists of a seven level series-stacked converter which is made of seven three-phase inverters, with their DC-busses connected in series. The seven three-phase outputs are summed through an injection transformer having 21 primary windings and six secondary windings. Each of the 21 converter outputs has a 150 μH filter inductor. The secondary of the injection transformer is connected to the low voltage, six-phase side of the main traction transformer at the substation.

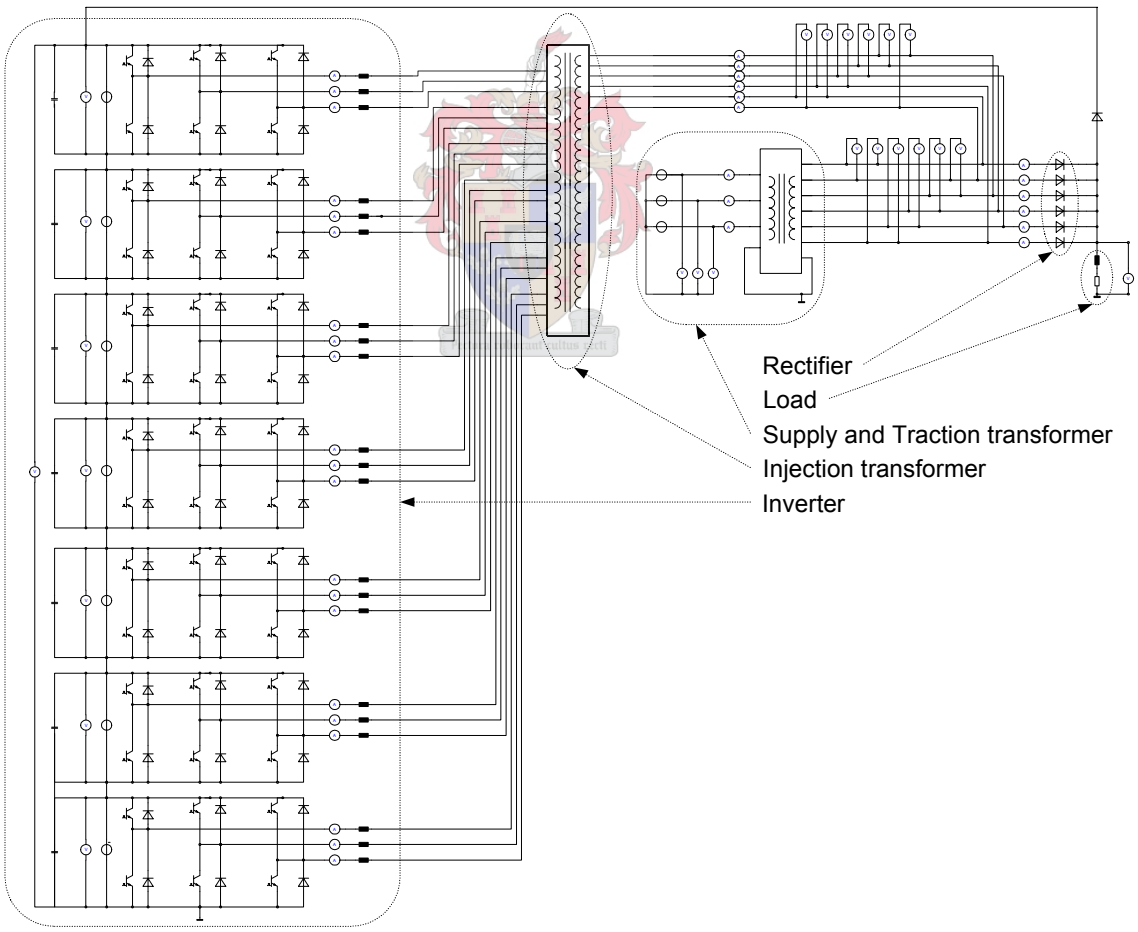


Figure 4.1 The simulation setup

The DC substation and 3 kV line were modelled as a six-phase half bridge rectifier with a series connected resistor and inductor. The Escom supply was modelled by a three-phase 66 kV_{RMS} voltage source, while the main traction transformer's model was created in Simplorer according to the nameplate information of the actual transformer. This was done to insure an accurate representation of the interaction between the converter system and the substation. To prevent uneven magnetization of the transformers, the three-phase supply voltages are ramped from zero to 66 kV_{RMS} during the first 20 ms of the simulations.

The simulations were done using Simplorer, with idealized components and no switching dead time. The time delays due to sampling and calculations were however taken into account. Table 4.1 lists the parameters used during the simulations.

Table 4.1 Simulation parameters

Total DC-bus voltage of converter	3.5 kV
Three-phase Supply voltage	66 kV_{RMS}
Six-phase voltages	2420 V_{RMS}
Filter inductance	150 µH
Capacitance of single DC-bus capacitor bank	24 mF
Passive DC-load	2 Ω + 1 mH
Current source as DC-load	+ 500 A to -1500 A
Number of switches	42
Switching frequency	5 kHz
Non-interleaved calculation frequency	5 kHz
Interleaved calculation frequency	35 kHz
Simulation time step	2 µs

The simulations and their results are discussed in five parts. To start off with, the behaviour of the six-phase system and rectifier is investigated. The next section examines the three switching strategies and compares them with each other. Then the functionality of the system is simulated in two parts, first the APF operation and then the DC-bus regulation, which is also responsible for the regeneration process. The final simulation is of the whole system, including the transition between operating modes.

4.1. The six-phase system and rectifier

Although the series-stacked converter and the control there of is done as for a three-phase system, the load and measurement system on the DC substation side is that of a six-phase system. Since it is easier to conceptualize and understand the interactions in a three-phase system, most simulation results are transformed to their three-phase equivalent forms, however it is necessary to keep in mind that the physical system is a six-phase one. This section is intended to clarify the interaction between the secondary of the main traction transformer and the six-pulse rectifier load and highlight the difference between the three-phase and six-phase systems.

Figure 4.2 is a simplified diagram showing the three-phase Eskom supply, the main traction transformer, the six-phase half bridge rectifier, as well as the inverter system and its connection to the six-phase system.

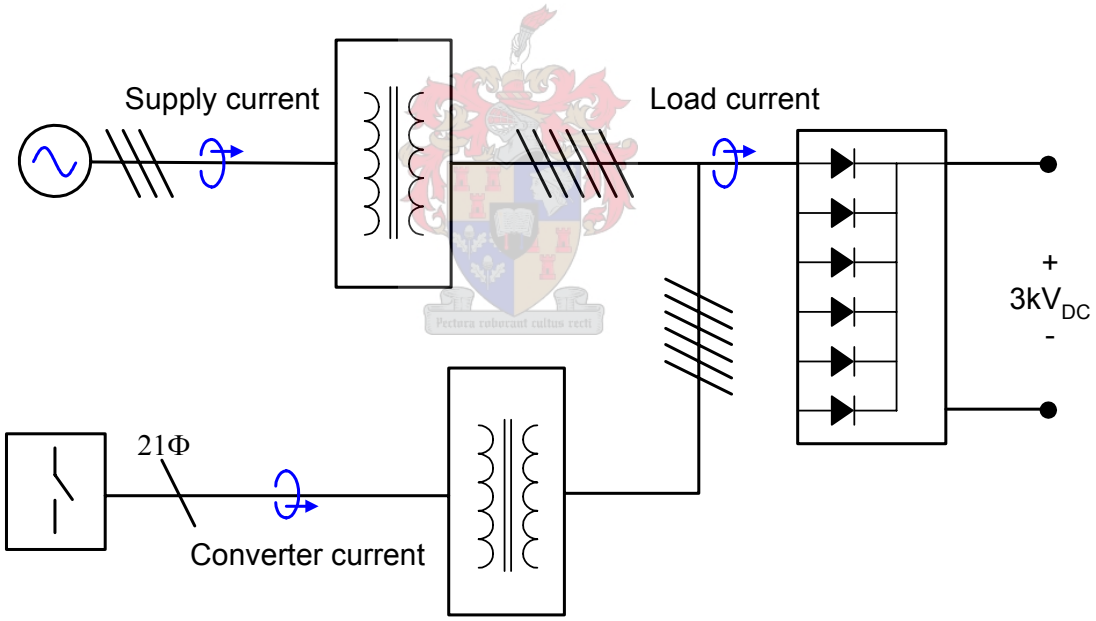


Figure 4.2 Simplified diagram of the substation and converter system

Since the six-phase half bridge rectifier is equivalent to a three-phase full bridge rectifier and if the 21 three-phase outputs of the converter can be superimposed to result in a single three-phase output, the system shown in Figure 4.2 can be viewed as a simplified three-phase system shown in Figure 4.3.

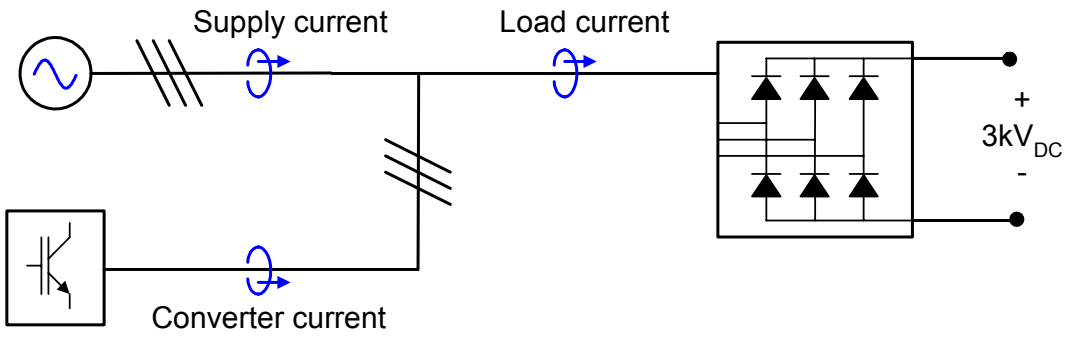


Figure 4.3 The simplified three-phase equivalent system

Figure 4.4 is a diagram showing the connection between the secondary of the main injection transformer and the six-phase half bridge rectifier. A diode is connected to each of the six transformer outputs and the cathodes of the six diodes are connected to the load.

Since a diode only conducts when the line-to-neutral voltage that it sees is higher than the other five line-to-neutral voltages and the voltage over the load, only one of the six-phase supply lines carries the load current at any point in time.

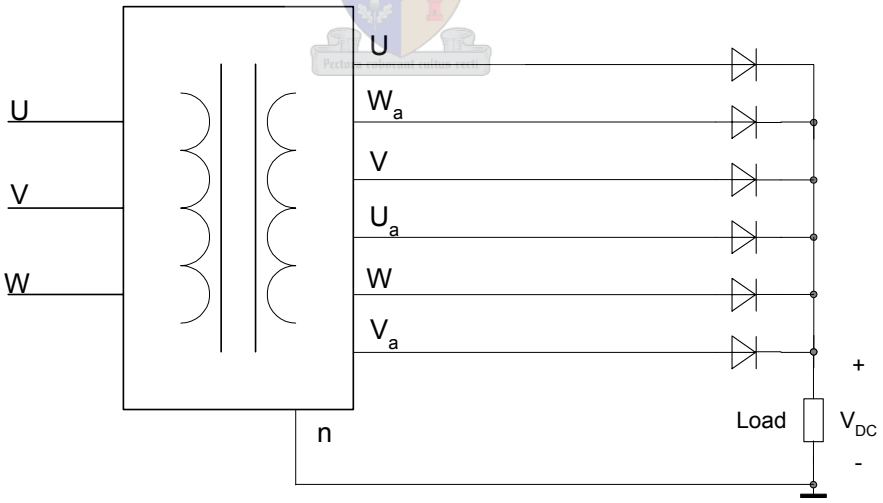


Figure 4.4 The six-phase and rectifier system

Since the six voltages on the secondary side are 60º out of phase with regard to each other, the output voltage V_{DC} is made up out of the top parts of the six sinusoidal voltages as shown in Figure 4.5

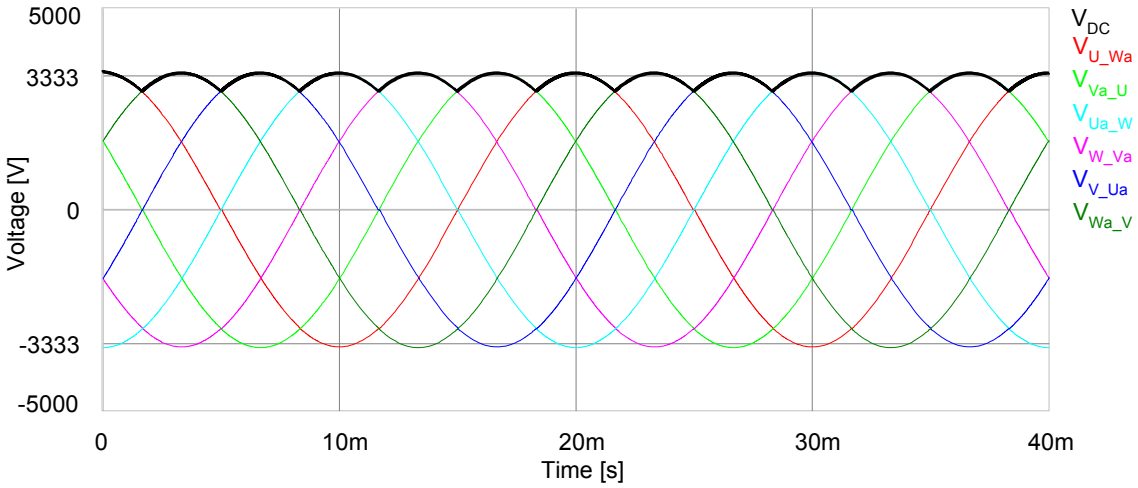


Figure 4.5 The six-phase voltages and rectified load voltage

The current drawn by the rectifier is supplied exclusively by the diode which has the highest voltage over it at a given moment. The resulting current drawn from the transformer for a 50 Hz cycle is shown in Figure 4.6. The amplitude of the load current during the simulations was 1500 A.

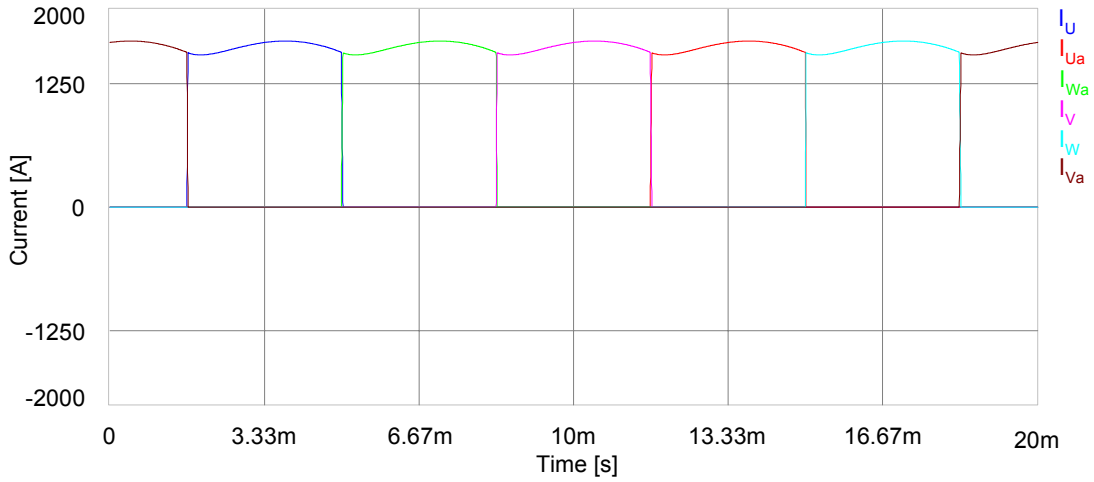


Figure 4.6 The six phase load currents

The current drawn by a single phase, phase U, is shown in Figure 4.7. It is noted that the average current drawn per phase over a 50 Hz period has a DC value unlike the load current feeding a three-phase rectifier shown in Figure 4.8.

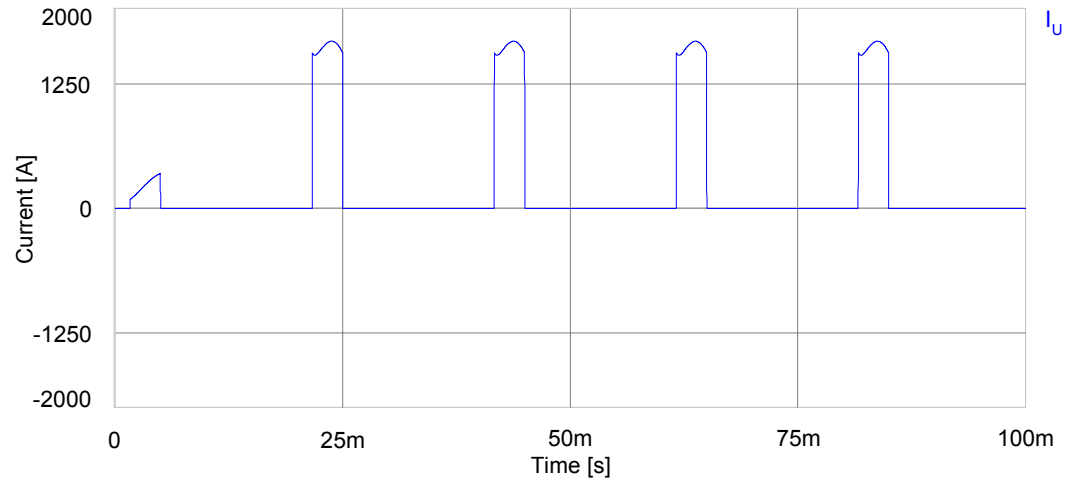


Figure 4.7 The load current drawn by phase U

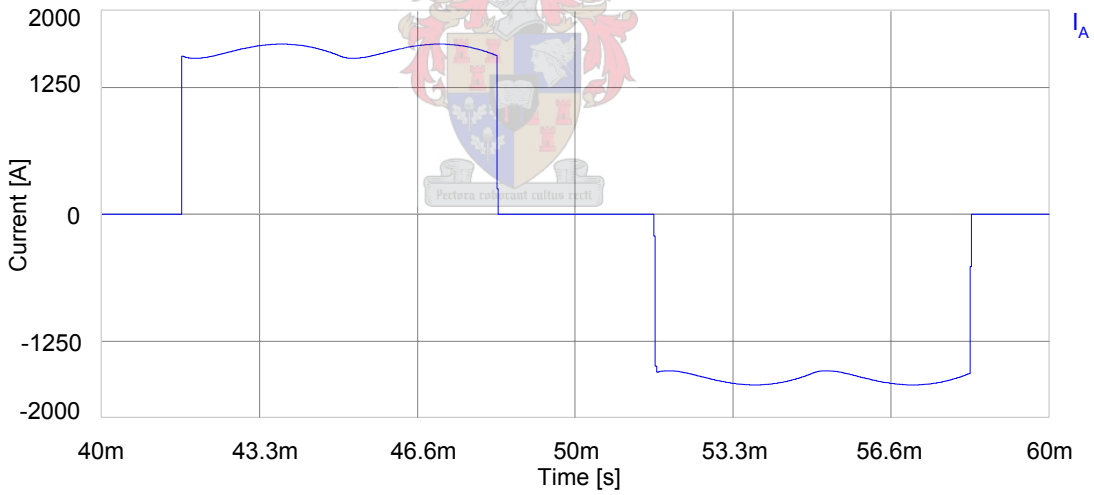


Figure 4.8 The load current drawn by a three-phase rectifier

Looking back to Figure 4.6 it can be seen that the average current drawn from the secondary of the transformer has a DC value. This DC current circulates via the neutral point of the transformer's secondary and through the diode that is conducting at that moment in time, and does not exist at the primary side of the transformer.

This DC current in the secondary may cause confusion when examining the compensated six-phase current, shown in Figure 4.9

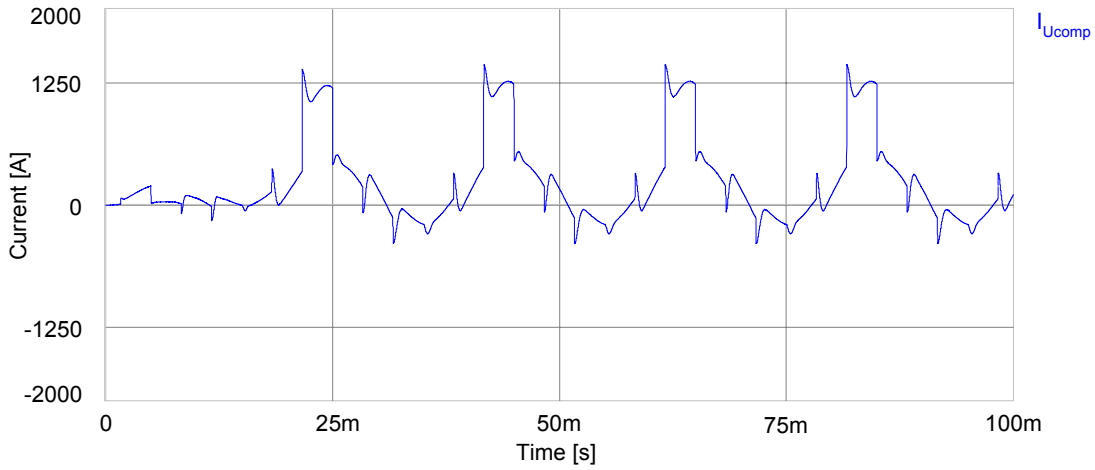


Figure 4.9 A compensated six-phase line current

One would expect the compensated current to be a purely sinusoidal, which is not the case as shown in Figure 4.9. To make sense of the current one must take the DC current that flows in the secondary into account. The DC current is added to the sinusoidal current to give the compensated current shown in Figure 4.9. The current drawn from the primary is however purely sinusoidal and compensated as one would expect, since the DC current component does not pass over the transformer.

4.2. The interleaved and non-interleaved simulations

The interleaved and non-interleaved switching schemes were simulated using identical converter and load setups. The simulation setup was that of a shunt active power filter, so that the systems response to step changes in the switching reference could be evaluated along with the effects of switching into an opposing voltage. The DC-bus is connected to a 3.5 kV DC voltage source and the DC-busses of the converters were not regulated. The voltages over the seven converter levels initially divide equally, but with the absence of parasitic components and voltage regulators the individual DC-bus voltages diverge as the simulations progress.[13]

To work as an active power filter, the output of the series-stacked converter is connected via the injection transformer to the six-phase AC link between the main traction transformer and the rectifier. The same filter inductor, having a value of 150 μH, was used in al three simulations. A model of the injection transformer is used to sum the 21 converter outputs into the six-phase system.

Instantaneous reactive power theory as described in section 3.1 is used to generate the current references. Space vector PWM as set out in section 3.4 then calculates the switching duty cycles.

For the non-interleaved system, the seven PWM blocks used the same 5 kHz triangular carrier and the switching duty cycles were calculated every time the triangular wave reached zero. The switching reference and duty cycles were thus updated every 200 μs. For the interleaved system, the seven triangular carriers were phase shifted by 51.43º and the current references and duty cycles for a specific PWM block was calculated every time the corresponding triangular carrier reached zero. This meant that the current references and duty cycles were calculated every 28.56 μs, although each PWM block kept its reference for 200 μs.

Figure 4.10 shows the seven phase A output currents and the current reference for phase A of the system, using the non-interleaved switching scheme. As was expected, all seven of the converter levels, output the exact same current.

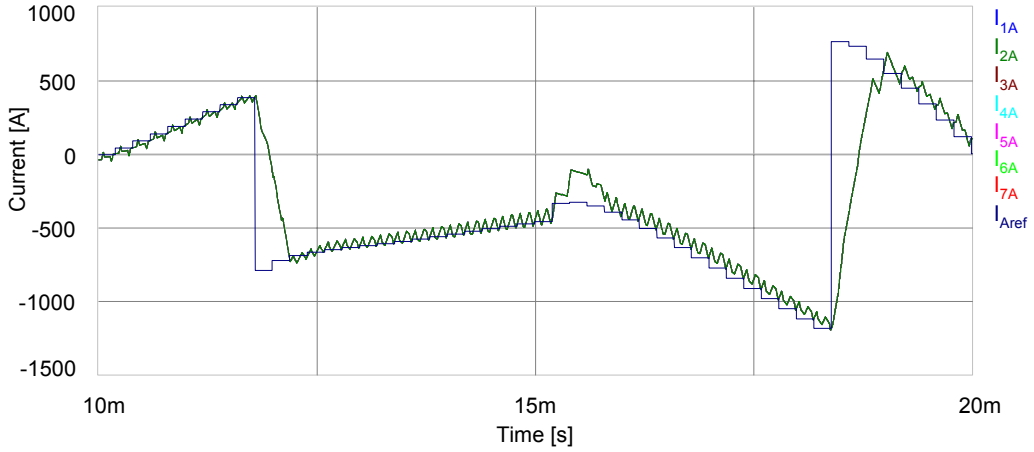


Figure 4.10 The non-interleaved output currents

The non-interleaved current reference shows large step changes, compared to that of the natural balancing interleaved and atypical interleaved systems shown in Figure 4.11 and Figure 4.12 respectively. This is because the frequency with which the interleaved switching references are updated, is seven times higher than for the non-interleaved system.

By calculating the switching references and duty cycles for each level, taking the status of the whole system into account, the natural balancing mechanism that balances the DC-bus can operate [13]. The system's response as a whole follows the reference current quite closely as shown in Figure 4.15. Using the status of the system as a whole implies that the total DC-bus voltage is measured, along with all 21 of the converters output currents. The output currents are summed to obtain the converter's output, as a whole. The individual inverter levels are presumed to share the DC-bus voltage as well as the over all output current equally. These averaged measurements are then used to calculate the switching references and duty cycles for an individual inverter level.

The output currents generated when the natural balancing switching scheme is used is shown in Figure 4.11. Inherent to this strategy, the individual output currents tend to sit at different DC offsets.

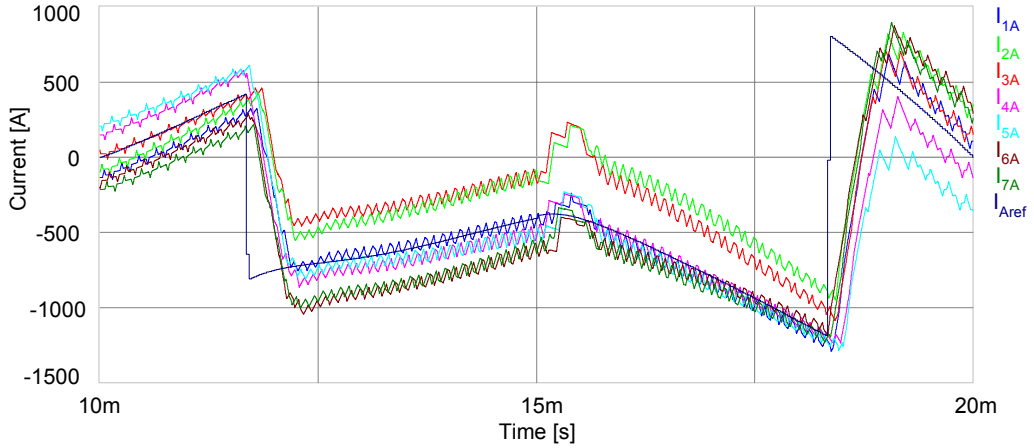


Figure 4.11 The natural balancing interleaved output currents

To eliminate the drift between the different converter currents and the reference current, the switching duty cycles can be calculated for each level using only the output current measurements and DC-bus voltage over the converter level in question. The simulated results obtained using this, the "atypical interleaved" switching scheme, are shown in Figure 4.12. Controlling the system in this manner does however imply that the natural balancing mechanism for the DC-bus voltages of a series-stacked converter is suppressed. To solve this problem the DC-bus voltages for each of the converter levels have to be regulated separately.

By doing this each level can be exactly controlled taking its status into account, as apposed to the natural balancing switching scheme, which relies on the assumption that all the DC-bus voltages and per phase output currents divide equally between the converter levels.

As seen in Figure 4.12, the individual output currents follow the reference current very closely. The individual output currents also lie on top of each other, showing the characteristic overlapping, as result of the interleaved switching.

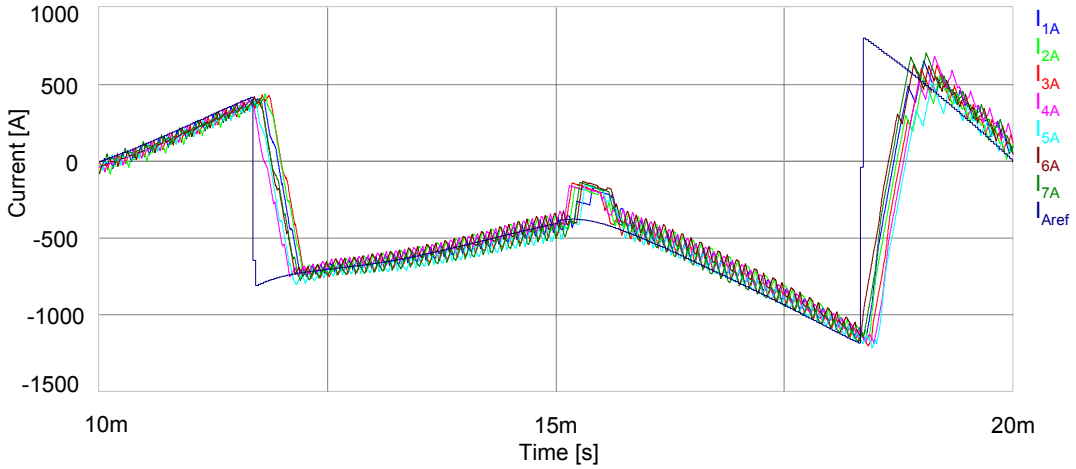


Figure 4.12 The output currents generated by atypical interleaved switching

Figure 4.13 and Figure 4.14 takes a closer look at the overlapping output current ripples as result of the natural balancing interleaved and atypical interleaved switching scheme respectively.

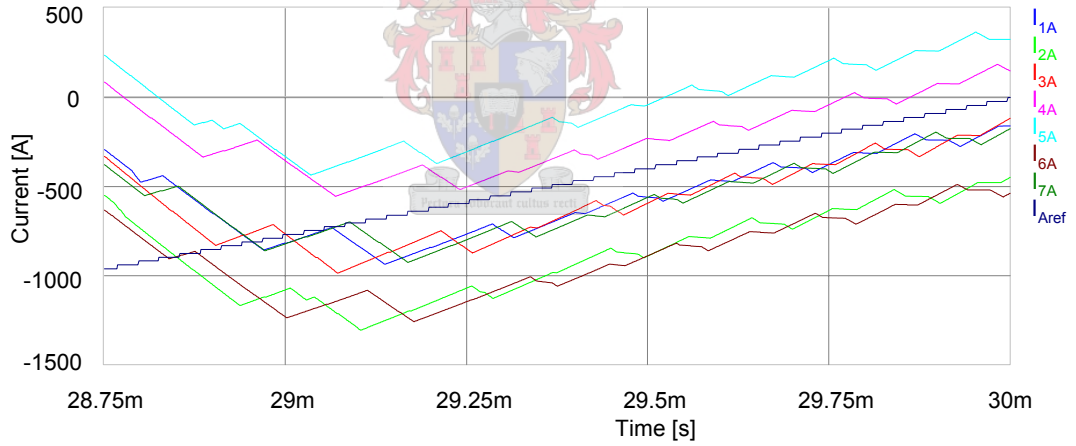


Figure 4.13 The overlapping ripple caused by the natural balancing interleaved switching scheme

Using the atypical switching scheme, the individual output currents follow the current reference much closer than the results obtained using the natural balancing interleaved switching scheme.

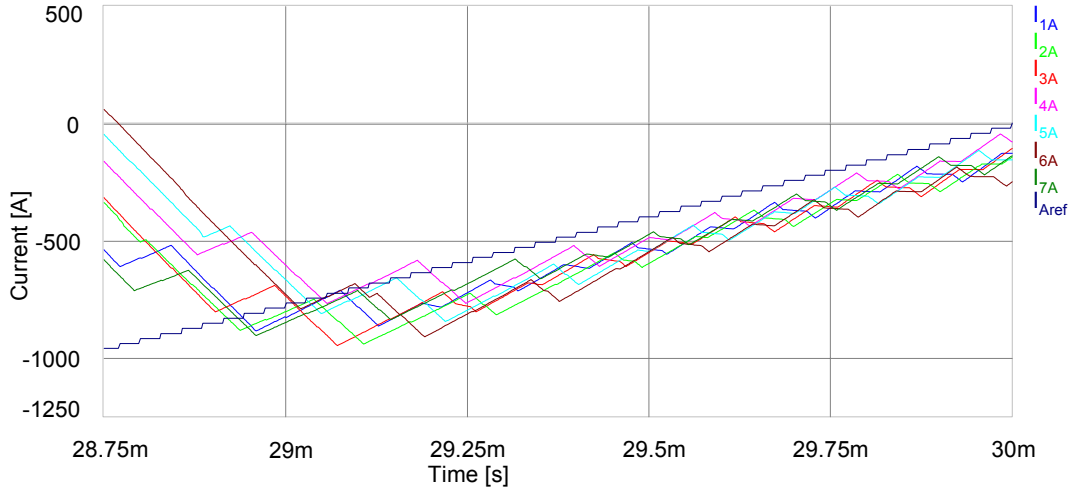


Figure 4.14 The overlapping ripple caused by the atypical interleaved switching scheme

The switching references for the three schemes and their resulting output currents are shown in Figure 4.15. When the two interleaved switching schemes are compared with regard to their overall output current, the difference is indistinguishable.

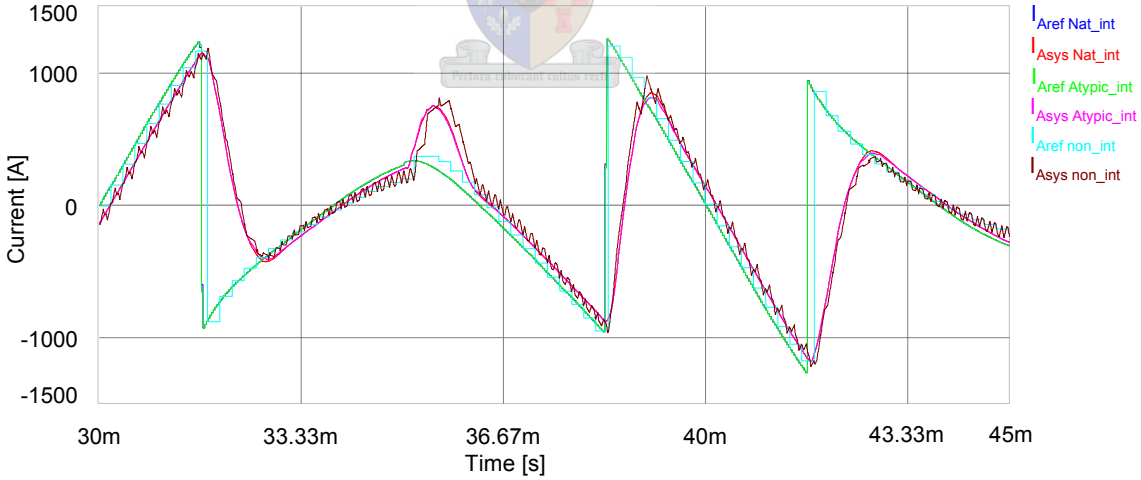


Figure 4.15 The reference and output currents for the three switching schemes

Since the same size filter inductor was used in the three simulations, the three switching strategies take the same amount of time to regain the required output current after a step change in the reference. The main difference between the

interleaved and non-interleaved systems is the amount of switching ripple present in their output currents. A closer look at the difference in the output current ripple is given in Figure 4.16. The two interleaved switching schemes clearly have a much reduced current ripple when compared to the non-interleaved switching scheme. The frequency of the ripple in the output is also seven times higher than the ripple frequency of the non-interleaved output current.

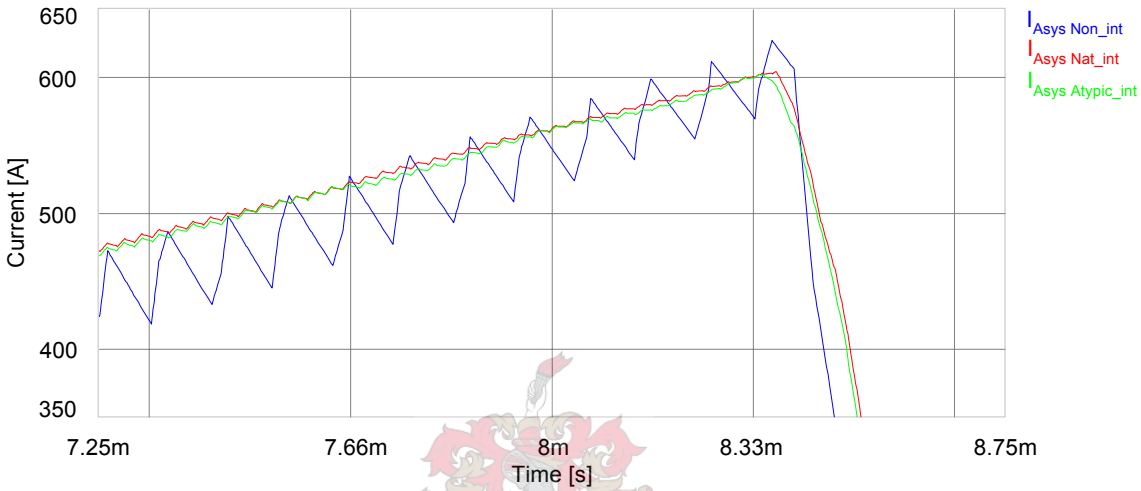


Figure 4.16 The current ripple for the three strategies

The current ripple caused by the non-interleaved switching can be reduced by enlarging the filter inductors. This would however slow the systems ability to react on a step change in the switching reference, and thus reduces the systems performance.

The main advantage gained by interleaving the switching signals is the reduction in the output current ripple, without opting for a lager filter inductance and thus a slower system response. Interleaved switching would also result in a reduced amount of transformer core losses caused by changing flux density, thus putting less strain on the injection transformer. By interleaving the converters the voltage steps that are summed by the injection transformer is smaller than it would be in the non-interleaved case. Since magnetic flux in a transformer's core is proportional to the integral of the voltage over the windings, a smaller voltage variation would cause less losses.

4.3. The APF functioning of the system

The simulation setup to evaluate the systems performance as an active power filter is the same as used for the interleaved switching schemes discussed in 4.1. Time delays, as expected in the physical system were introduced in the simulations. These delays approximate the time taken to sample the measurements and compute the switching references. Again note that the DC-bus is connected to a 3.5 kV DC voltage source and the converter's DC-busses were not regulated. Since the two interleaved switching schemes reacts almost identically when the system is observed as a whole, the results discussed in this section are from the atypic interleaved switching scheme. Distinctions between the two interleaved switching schemes are made when the behaviour of the DC-bus voltages are looked at though. A quantitative comparison with regard to the filtering performance of the three switching strategies ends this section.

Since the interaction in a three-phase system is simpler to understand and easier to visualize, most of the APF simulations are viewed from a three-phase perspective. A quick look will be taken at the actual six-phase currents at the end of this section.

The three-phase load currents are calculated out of the six-phase current measurements and do not actually exist in the physical system. The three-phase supply currents are however measured on the primary side of the main traction transformer. In the simulation results they are scaled by the transformer's winding ratio, in order to be compared with the three-phase equivalent load current, calculated on the six-phase side.

The reference currents used to control the APF functioning is calculated as described in section 3.1, using the Instantaneous reactive power theory. Since interleaved switching is used, the current references and duty cycles are calculated every 28.57 µs. Figure 4.17 shows the filtering current reference for the phase A currents and the system's attempt to follow the reference for phase A.

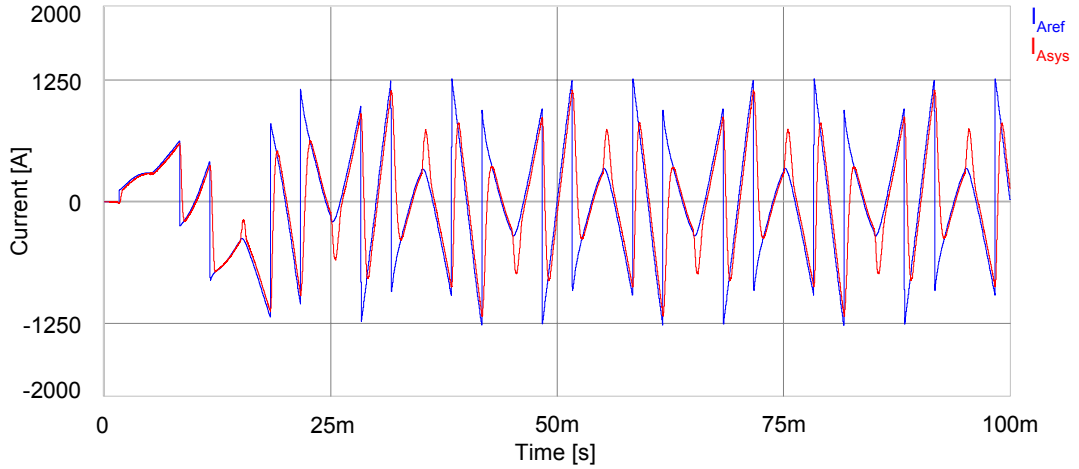


Figure 4.17 The phase A reference and converter currents

A closer look at the current reference and the system's output current are shown in Figure 4.18.

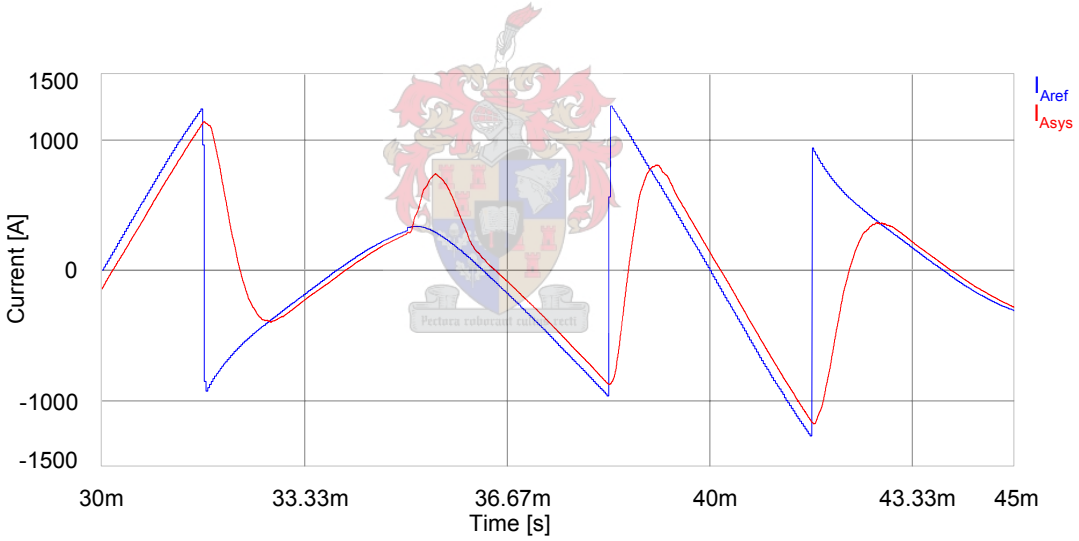


Figure 4.18 A closer look at the current reference and the system's output

In Figure 4.18 it can be seen that the reference is followed quite closely except where a sharp transition has to be made, which is attributed to the output voltage of the converter saturating. The output current of the system can only achieve a damped gradient, as apposed to the infinite gradient at the step changes in the reference current. At 35 ms the output current of the system swerves away from the reference, this corresponds to the time where the references for phase B and C makes a step

change. This point also coincides with the time that two of the six-phase currents commutate.

The phase A load current and the compensated supply current are shown in Figure 4.19. The compensated supply current looks notably more sinusoidal than the load current. The occurrence of the spikes on the compensated current corresponds to the commutation of the rectifier diodes. The spikes occur because the step changes in the reference current can not be followed closely enough.

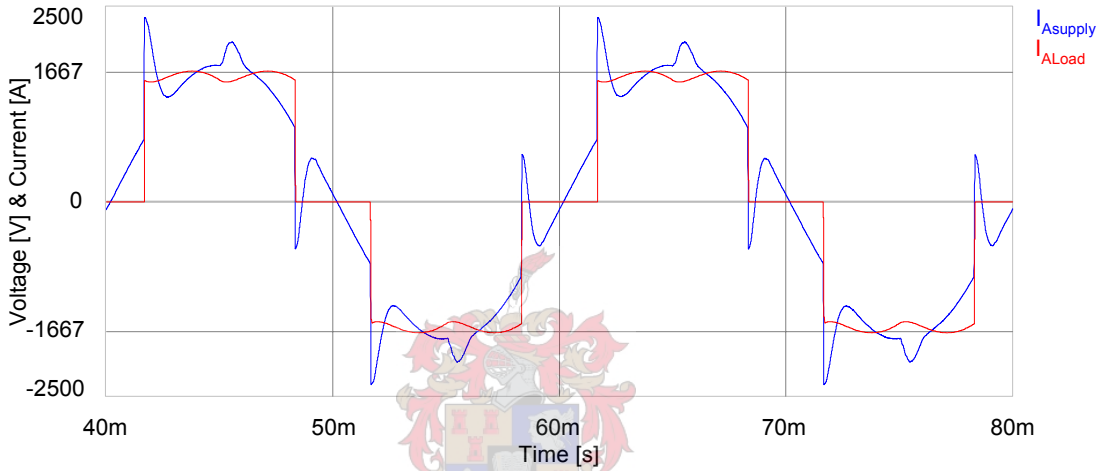


Figure 4.19 The load and compensated supply currents for phase A

The effect of the simultaneous step change in the phase A and B reference currents on the phase A output current, causes the kinks observed at the peaks of the compensated supply current. The same effects occur on the other two compensated supply current phases. The interaction becomes even more complex when observed out of the six-phase point of view.

The equivalent phase A voltage, calculated out of the six-phase line-to-line voltage measurements and the compensated phase A supply current is shown in Figure 4.20. The supply voltages and compensated supplies current are in phase with each other, thus indicating that power is being drawn from the supply. During regeneration the supply voltages and currents are 180º out of phase, indicating that power is delivered to the supply.

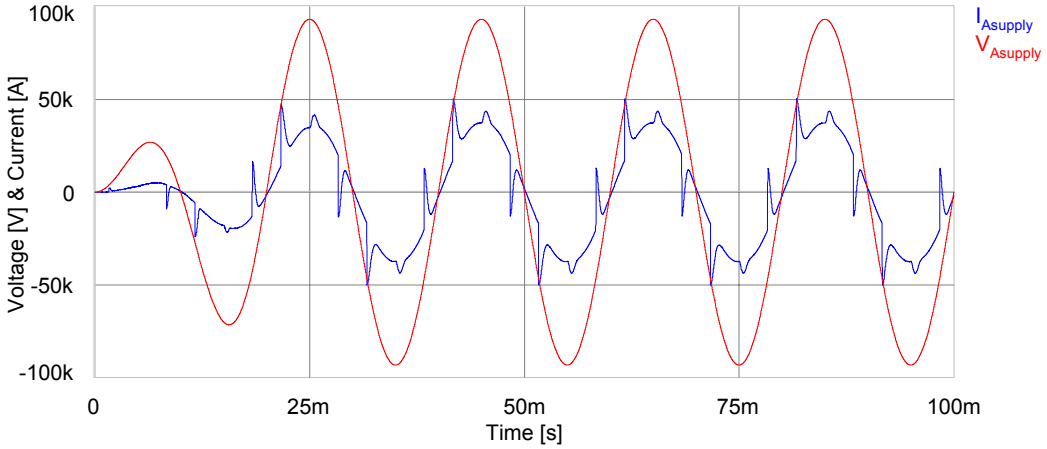


Figure 4.20 The Supply voltage and compensated supply current for phase A

The only noticeable difference between the APF simulations for the natural balancing and atypic interleaved switching schemes are in the behaviour of their capacitor voltages. During the APF simulation the DC-bus voltages of the seven converters were not controlled and the simulation starts with the total DC-bus voltage sharing equally over the seven converter levels.

Figure 4.21 shows the seven DC-bus voltages for the natural balancing interleaved switching scheme.

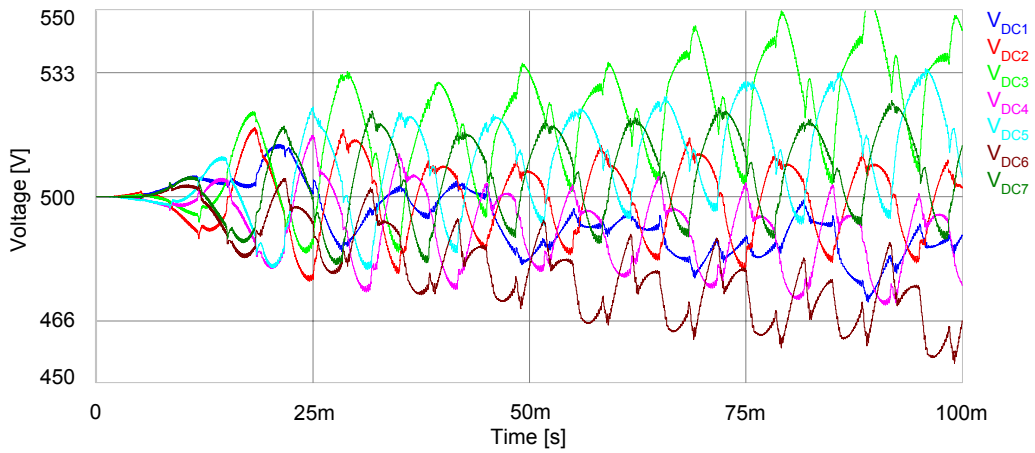


Figure 4.21 The seven capacitor voltages for the natural balancing interleaved switching scheme

Two balancing mechanisms have been identified, one associated with losses in the system and one related to the load impedance [13][14][15]. The lack of losses and the idealization of components in the simulation suppresses the natural balancing mechanism and the seven capacitor voltages diverge slowly. Since the different individual levels switch at different points in time, the energy drawn from their respective capacitor banks differ, while the current flowing through all the capacitors remain equal, thus causing the oscillations visible in the capacitor voltages.

The seven capacitor voltages resulting from the atypical interleaved switching scheme are shown in Figure 4.22. Similarly to the natural balancing interleaved switching scheme, the individual converters levels switch at different points in time, however the duty cycles are calculated using the DC-bus voltage of the converter level in question, thus disrupting the capacitor voltage interaction describes for the natural balancing system. Again the absence of losses and the idealization of components in the simulation cause the capacitor voltages diverge slowly.

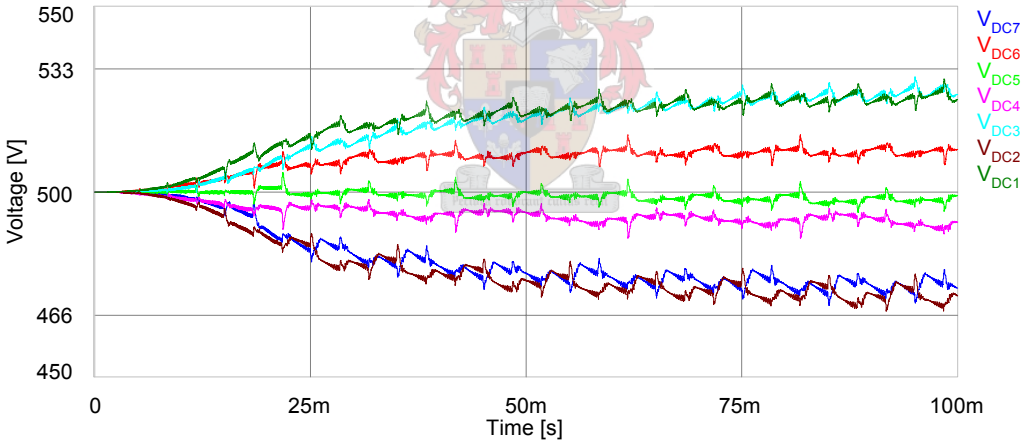


Figure 4.22 The seven capacitor voltages for the atypical switching scheme

The simulations done for the non-interleaved switching scheme confirmed that even without losses, the DC-bus voltages of the non-interleaved system balances perfectly. This is because the mechanism for unbalance has no source of energy and if unbalance was to occur, the switching and copper losses in the system would dissipate the energy [13][14][15].

The simulations were repeated with losses included in the simulations. A 0.01 Ω resistor was added in series with the DC supply voltage. To emulate switching and copper losses 0.01 Ω resistors were also added in series with each filter inductor. No changes were made to the six-phase connection and rectifier load.

Figure 4.23 shows the seven capacitor voltages for the natural balancing interleaved system. Similar to the results shown in Figure 4.21 the oscillations are still present but the important part to note is that the voltages do not diverge as time progresses.

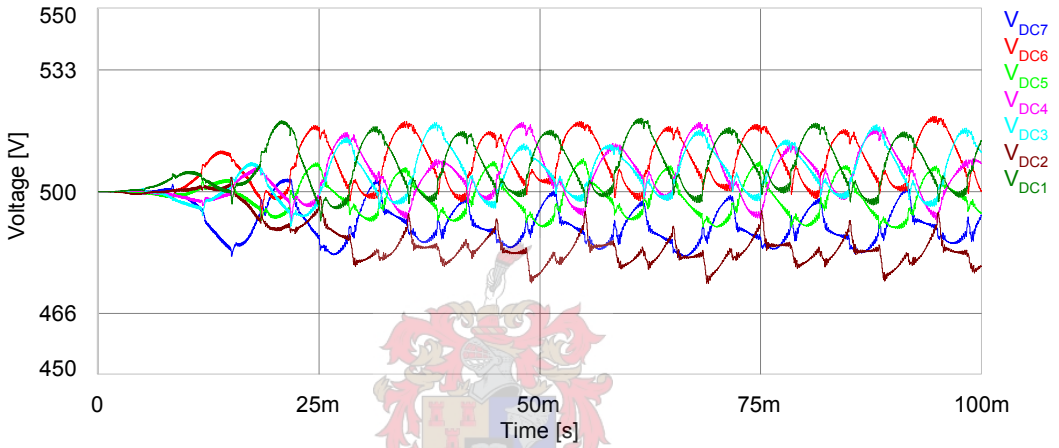


Figure 4.23 The individual capacitor voltages for a system with losses taken into account

The results obtained for the atypic interleaved scheme does not differ from those shown in Figure 4.22 which supports the assumption that atypic switching suppresses the natural balancing mechanisms which exists in a series-stacked converter.

To conclude the APF simulations, a look was taken at what happens in the physical six-phase system. Figure 4.24 shows the relationship between one of the six-phase load currents and the three-phase equivalent load current for phase A. Looking at the three-phase load current and noting that the average load current over a period is zero, it is easy to accept that the compensated three-phase current would be sinusoidal as shown in Figure 4.19.

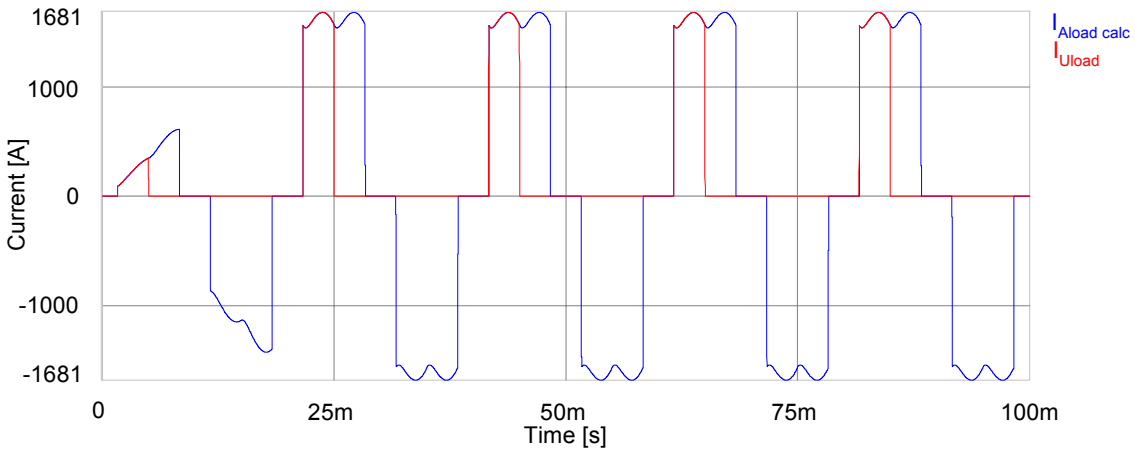


Figure 4.24 six-phase and three-phase rectified load currents

As discussed in section 4.1, the time average load current has a DC component which circulates through the neutral point of the transformer and out via the line which is conducting at that moment in time. A compensated six-phase current would thus have a sinusoidal component which is proportional to the current drawn by the primary of the transformer. In addition to the sinusoidal element, the six-phase load current would also have to carry the DC current component at the appropriate space in time. A six-phase load current and the compensated version of that current is shown in Figure 4.25.

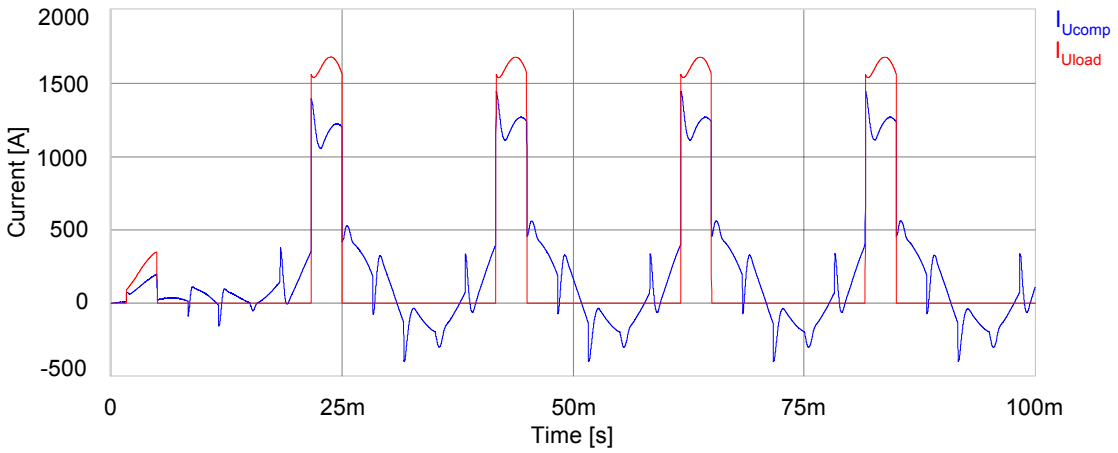


Figure 4.25 The compensated and uncompensated six-phase load current

The three-phase primary side of the transformer does not have a DC current component and the relationship between the primary and the secondary currents of the transformer is shown in Figure 4.26.

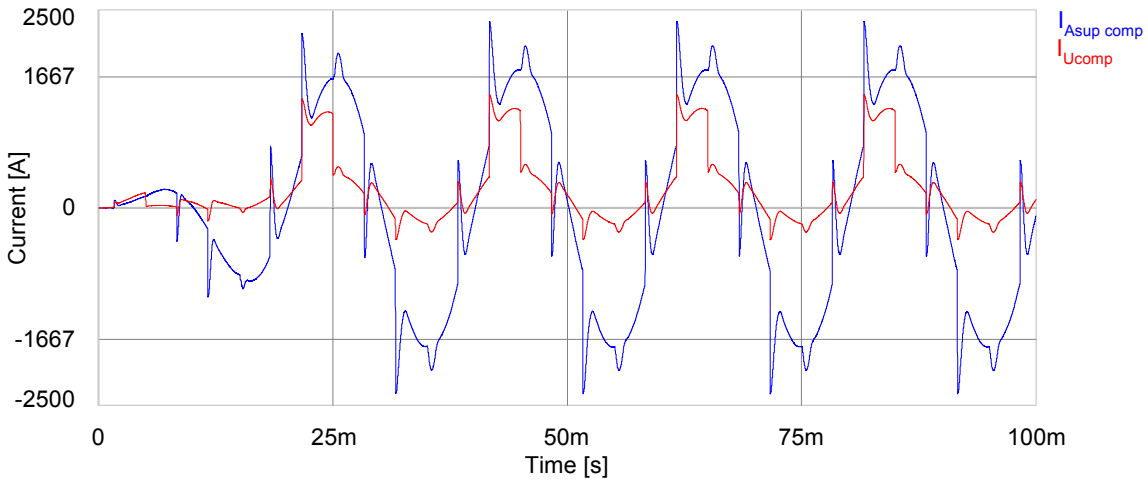


Figure 4.26 a three-phase primary and a six-phase secondary transformer current

For the power quality issues, we are only interested in the three-phase currents drawn by the primary of the traction transformer and there is thus no need to further investigate the behaviour of the six-phase system.

To do a quantitative comparison between the different switching strategies, the degree of harmonic distortion is calculated and compared. The total harmonic distortion, THD is calculated using all the harmonics up to the 50th.

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} \hat{i}_h^2}}{\hat{i}_1} \cdot 100 \qquad (4.1)$$

The THD of the three-phase supply currents for the three switching strategies and the uncompensated case were calculated using equation(4.1) and listed in Table 4.2.

Table 4.2 THDs of the uncompensated and compensated supply current by the three switching strategies

	THD of the filtered supply current
Uncompensated supply	30.17%
Non-interleaved switching	26.17%
Natural balancing interleaved switching	26.26%
Atypical interleaved switching	25.98%

Although the simulated wave forms look quite good, the THDs calculated suggest that the system performs poorly as an active power filter. This is mainly due to the time delay is the simulation, although the lack of parasitic elements is the simulations also contribute to the poor simulated performance. In the practical system, the parasitic components, like the injection transformers leakage inductance, is used as a part of the filter inductance, while losses in the system results in a more damped system response.

As was expected the atypic switching scheme shows the best result. Unfortunately a 4.09% reduction in THD is not sufficient. To evaluate the effectiveness of the instantaneous reactive power theory as applied in the simulations the calculated current reference was added to the measured load current and a 14.84% reduction in THD could be achieved if the reference could be followed exactly. Around 10% of the filtering capability of the system is lost due to the simulation setup.

In Table 4.3 the size of the major harmonic components in the load current is given as a percentage of the fundamental harmonic component for an uncompensated supply current and for the three switching strategies.

Table 4.3 The major harmonic component as a percentage of the fundamental harmonic

	5	7	11	13	17	19
Uncompensated	21.46	12.73	8.84	7.21	5.65	4.99
Non-interleaved	14.08	7.79	12.27	6.3	8.69	5.31
Natural balanced interleaved	13.08	9.39	12.08	6.89	8.77	5.44
Atypic interleaved	13.09	9.4	11.72	6.9	8.44	5.41

The most significant reduction in the size of a harmonic component is for the 5^{th} harmonic, although the 7^{th} and 13^{th} harmonics are also reduced. The 11^{th}, 17^{th} and 19^{th} harmonics are however slightly lager in the cases where compensation was attempted.

Since there are no standards set with regard to the harmonic contents of current drawn by a consumer in South Africa, the APF functioning of the system will be evaluated by comparing the THD of the supply voltage before and after filtering.

A line inductance was added on the primary of the main traction transformer. The current harmonics drawn by the load will thus cause distortion of the supply voltages. Since the line inductance is unknown, the leakage inductance of the main traction transformer is approximated as 5% of the traction transformer's inductance (L_{leak} = 139.39 mH) and used as the line inductance value in the simulation.

The THD of a medium voltage supply, counting all harmonics up to the 40th order, has to be less than 8% [30]. Figure 4.27 shows the distortion of the 66 kV supply after harmonic compensation.

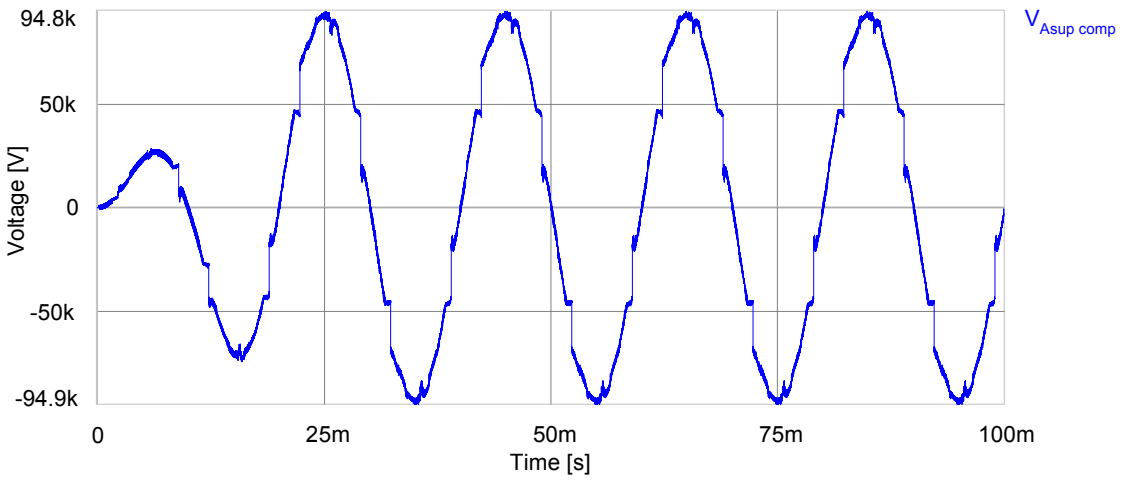


Figure 4.27 The distortion on the supply voltage as result of line inductance and the harmonic content of the supply current

The THD was reduced from 6.53% for the uncompensated system to 5.19% for the compensated system, suggesting that there is no need for filtering.

4.4. DC-bus controller

The next step was to simulate the DC-bus voltage controller which is also responsible for the regeneration functioning of the system. To avoid behaviour that may arise as a result of the APF functioning, the switching references and duty cycles were calculated using only the DC-bus controller. The reference voltage for total DC-bus voltage was set to 3.5 kV, which meant that each converter level would ideally have 500 V over it. The DC-bus capacitors are given an initial voltage of 471 V, which is the voltage over each converter level after the system has been soft started. This is to eliminate the effect of the DC-bus charging via the free-wheeling diodes when the AC voltages are connected.

Since the major difference between the two interleaved switching schemes are the behaviour of their DC-bus voltages, the DC-bus controllers for both schemes are looked at in this section. In both schemes a Lag compensator is used to regulate the DC-bus voltages. The compensator discussed in section 3.2.2 is designed for the natural balancing interleaved system. Using the same design path, a Lag compensator was designed for the atypical interleaved system as well. The difference lies in that for the natural balancing system only one controller is used and the system transfer function is modelled as a whole. While for the atypic system the controller is designed using the transfer function of a single converter level, thus requiring seven identical controllers to control all the DC-busses.

Figure 4.28 shows the seven capacitor voltages for the atypical interleaved switching scheme. No initial currents or compensator values are defined at the start of the simulation. As a result the systems DC-bus voltages drop right after the simulation starts. After the dip, the voltage increases sharply and overshoots the reference value, where after the voltages then decrease until they reach their desired values.

As was expected for the atypic system, all seven DC voltages reaches and stays at the 500 V mark.

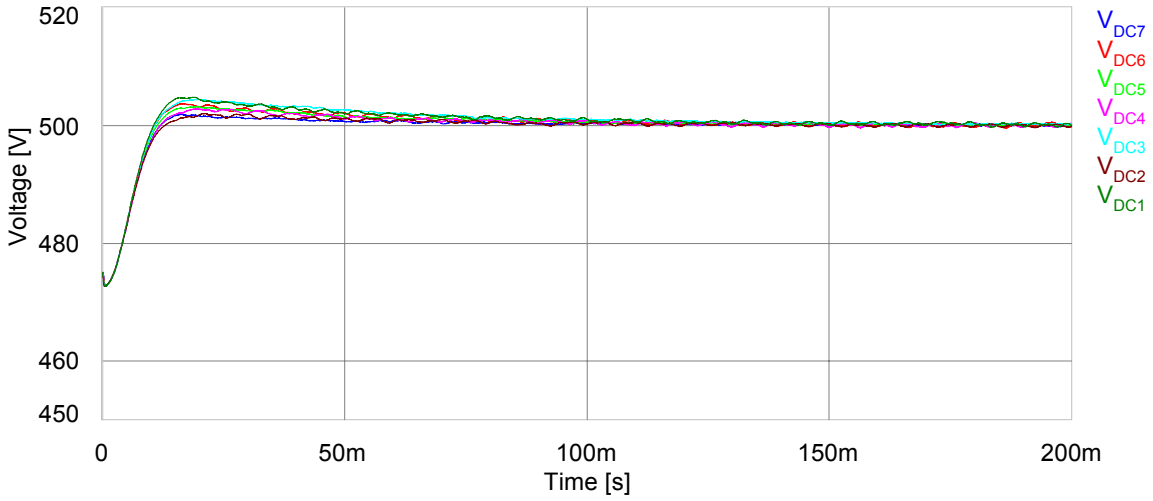


Figure 4.28 The individual capacitor bank voltages

This results in a steady state total DC-bus voltage of 3.5 kV, as shown in Figure 4.29. The rise time in response to the regulator starting is identical to the rise time of the individual converter busses and is around 10 ms which corresponds quite well with the step response plotted for the controller in Figure 3.8.

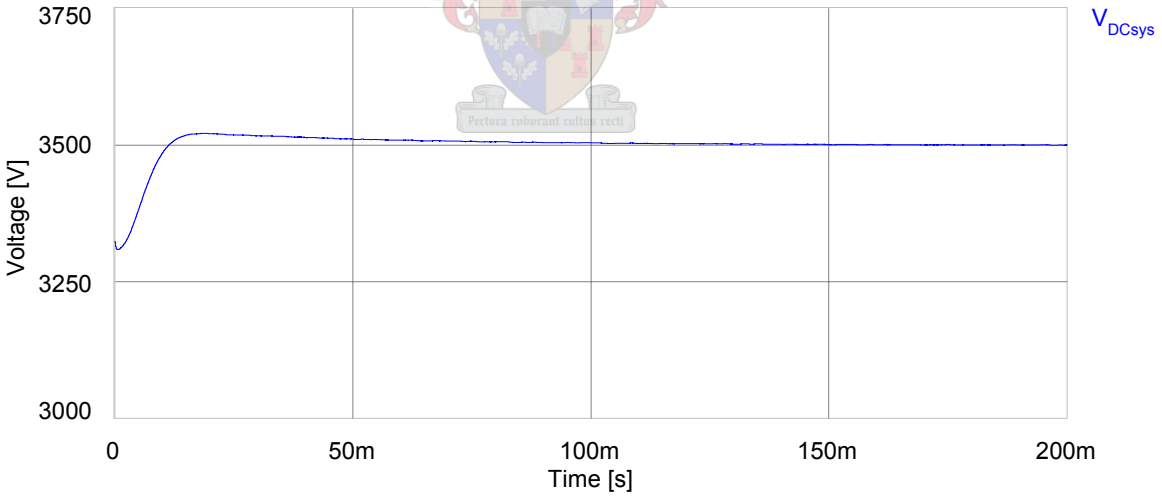


Figure 4.29 The total DC-bus Voltage

The Lag compensator uses the error between the reference voltage and the measured voltages along with previous error measurements and compensator outputs to generate a current reference. The voltage errors used to do the

calculations are shown in Figure 4.30. Each level has its own compensator, thus the seven voltage errors and compensator reference currents are calculated separately.

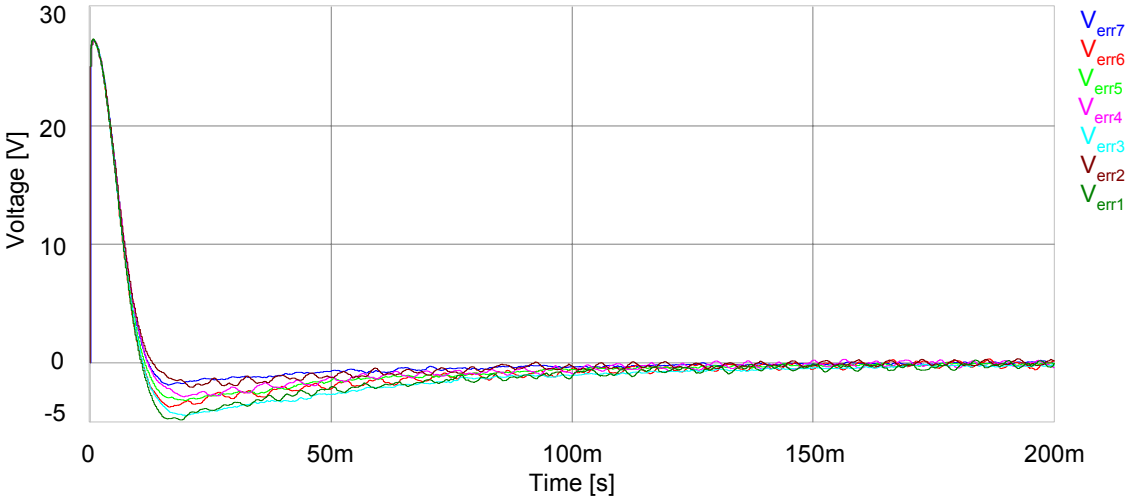


Figure 4.30 The error between the reference and the measured DC-bus voltages

Each converter level's voltage is measured separately and for the atypic switching case the voltage error and the DC-bus compensation current reference shown in Figure 4.31 are thus updated at a frequency of 5 kH, the frequency with which each converter levels reference is updated as well.

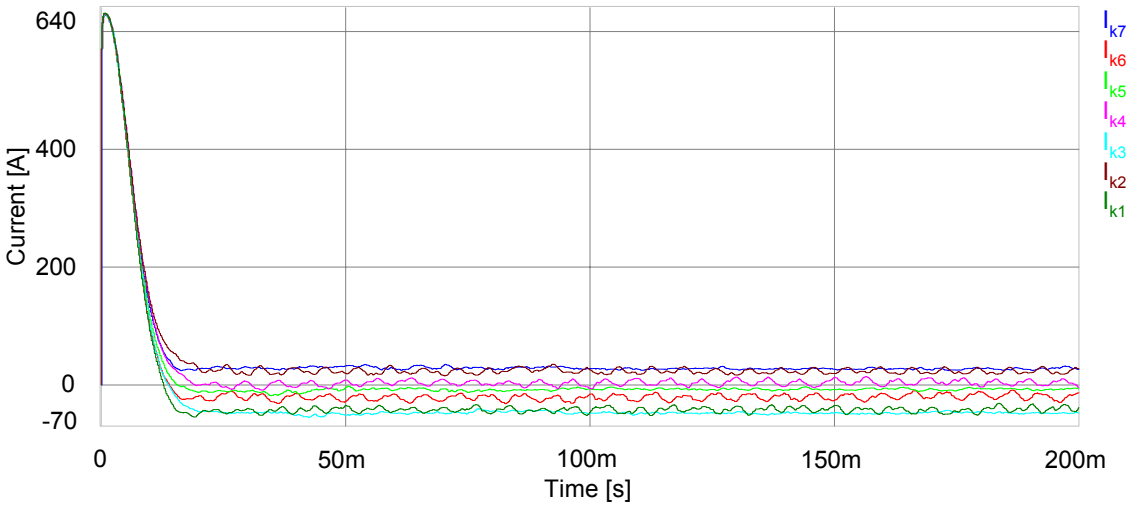


Figure 4.31 The reference currents generated by the DC-bus controller

The control of the natural balancing system works in much the same way, the difference being that the seven level system is modelled as a single converter and the Lag compensator was designed to control the equivalent system. A single voltage error, shown in Figure 4.32, is calculated with the reference voltage set to 3.5 kV and using the total DC-bus voltage measurement.

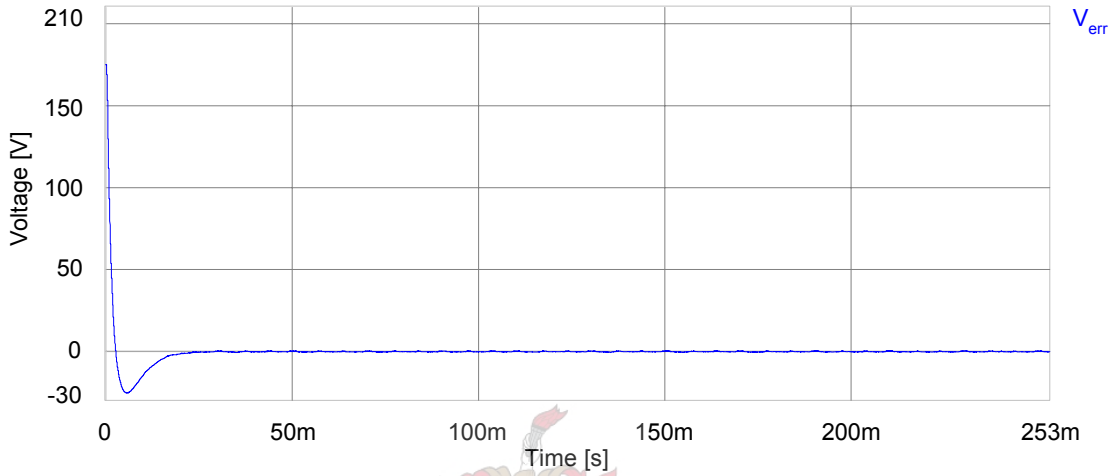


Figure 4.32 The voltage error for the natural balancing DC-bus controller

The DC-bus compensation current reference is shown in Figure 4.33, the voltage error and compensation current references are updated at 35 kHz, each time a switching reference is calculated.

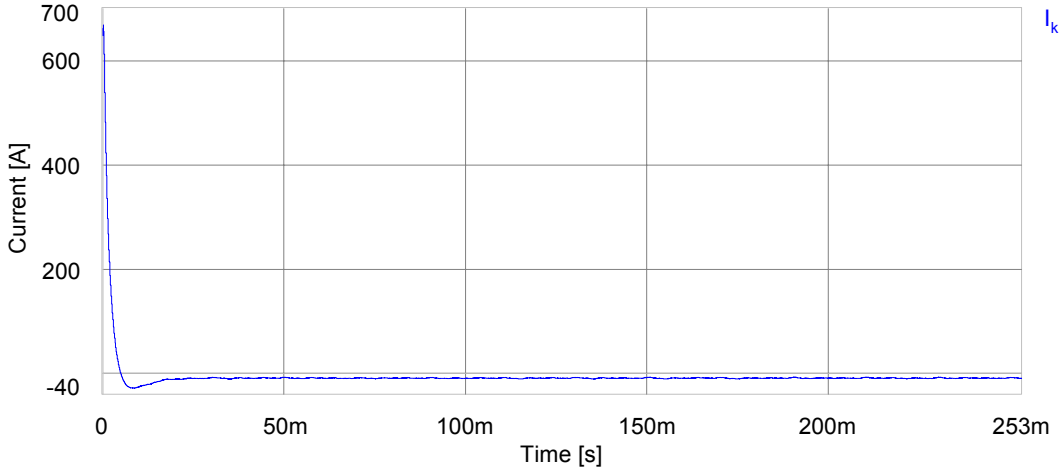


Figure 4.33 The current reference for the natural balancing switching scheme

As shown in Figure 4.34 the total DC-bus voltage reaches the reference quite quickly with a small amount of overshoot. Although the controller for the natural balancing cases has a faster response than the one used in the atypical case, the focus of this investigation is on the steady state behaviour of the individual DC-bus voltages.

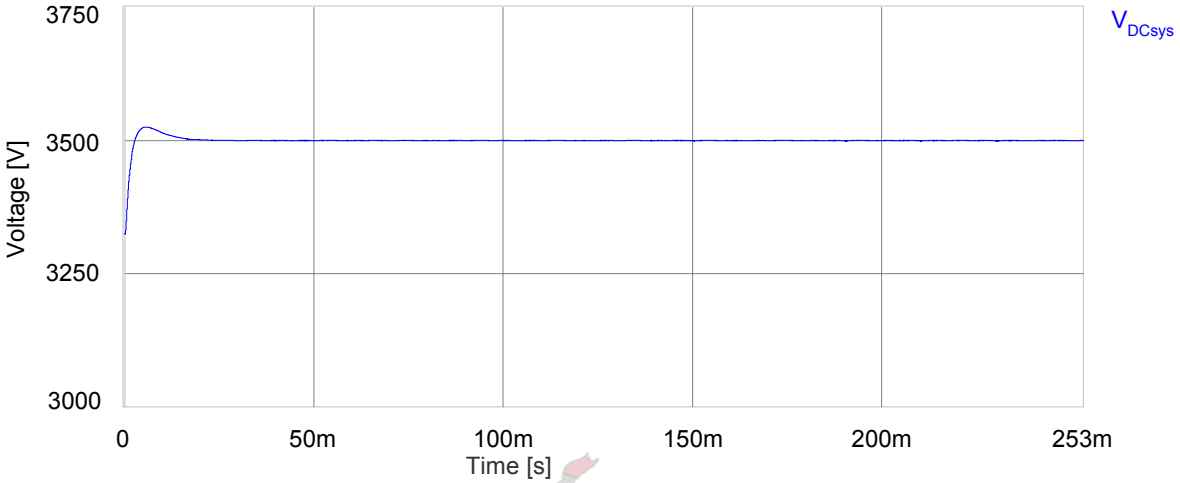


Figure 4.34 The total DC-bus voltage for the natural balancing switching scheme

The seven individual DC-bus voltages of the system are shown in Figure 4.35. With a total DC-bus voltage of 3.5 kV one would ideally see that each of the seven DC-bus

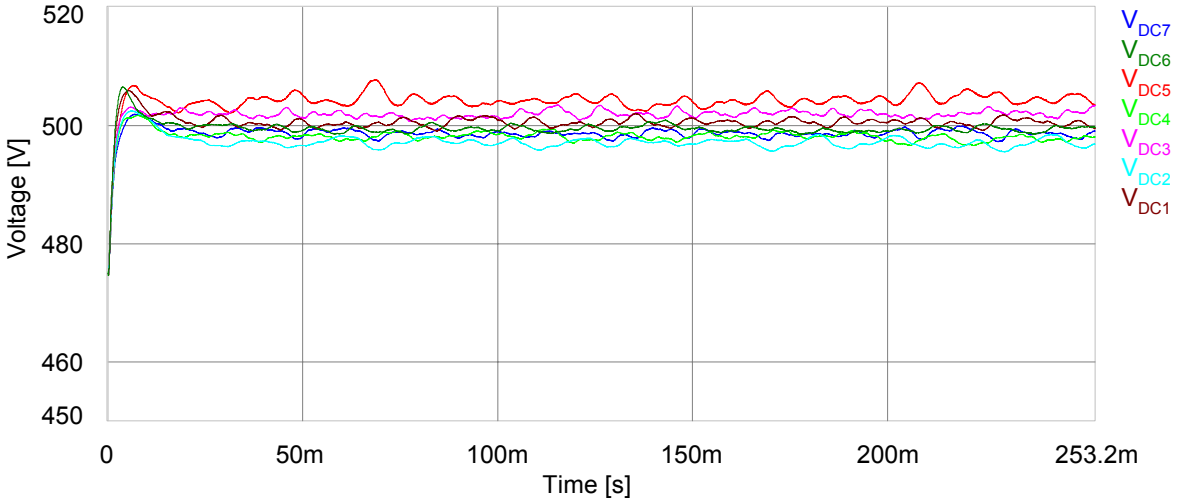


Figure 4.35 The individual DC-bus voltages for the natural balancing scheme

voltages would be equal to 500 V. Figure 4.35 shows that that is not the case, the seven voltages arrange themselves around the 500 V mark while still summing to 3500V. Unlike the individual DC-bus voltages seen in the atypic simulation results, the voltages for the natural balancing scheme has an AC component. The ripple that is visible on the voltages are due to the controller trying to regulate the total DC-bus voltage using the averaged DC-bus and output current measurements. This means that the duty cycle and switching reference that is calculated, is not exclusively tailored for the converter level receiving the gating signals, but rather the reference that would best serve the system as a whole.

4.5. The integrated simulation

The final simulation incorporates both the APF and regenerating functions of the system. The simulation results discussed here were obtained using the natural balancing interleaved switching scheme. The simulation setup was the same as for the other simulations discussed in this section, except that the DC-load, which was a series connected 2 Ω resistor and 1 mH inductor, was replaced with a current source.

With an externally controlled current source as load, the behaviour of a train on the 3 kV DC-line could be modelled. While a train is braking (regenerating electrical energy) the load current was set to 500 A. While the train is running normally, the load current is -1500 A which is drawn through the rectifier from the main traction transformer.

The simulation starts off in regeneration mode with the DC-bus charged to 3.3 kV, which is the DC-bus voltage after the soft start sequence has finished and the DC contactor has closed. The system stays in regeneration mode for 85 ms before the load current direction is changed. Between 100 ms and 200 ms, the system is required to perform filtering in full load condition. After 200 ms the current direction changes again and from 215 ms the system is back to regenerating at full rating.

At the start of the simulation no initial values were given to the controller and no initial output currents were defined in the system. The simulation was done using the natural balancing interleaved switching scheme, witch means that the reference currents and switching duty cycles were calculated at a frequency of 35 kHz, taking the condition of the whole system into account for each reference calculated.

Figure 4.36 shows the load current profile during the simulations, the system is in regeneration mode when the load current is greater than zero and in APF mode when the load current is negative. Since the 3 kV DC-line has a large inductive nature, the load current would not change instantaneously, the load current in the simulation is thus ramped between the full regeneration current to full load current over a period of 20 ms.

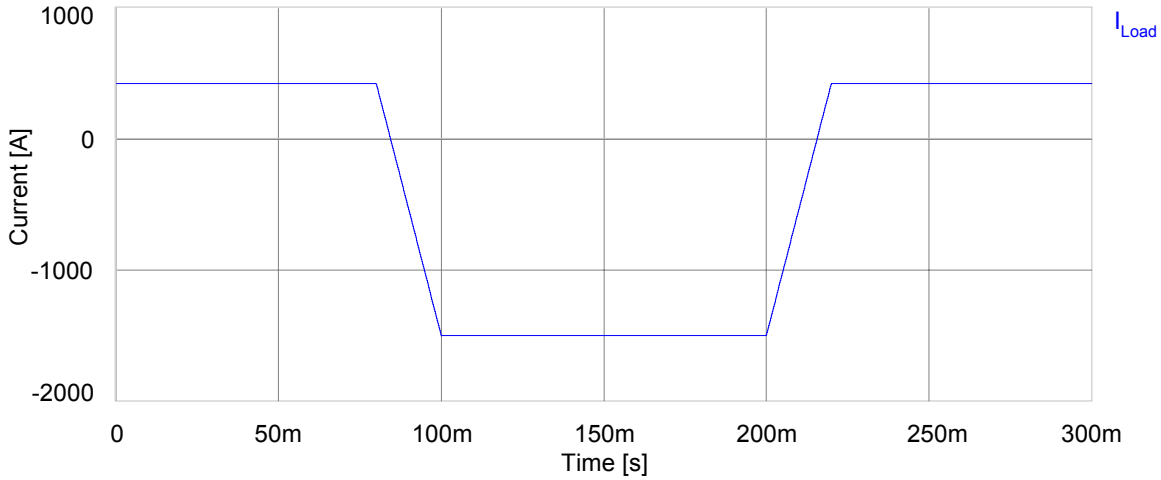


Figure 4.36 The load current

Since no initial values are given to the DC-bus controller, the DC-bus voltage initially overshoots the reference mark before settling at its intended value as shown in Figure 4.37.

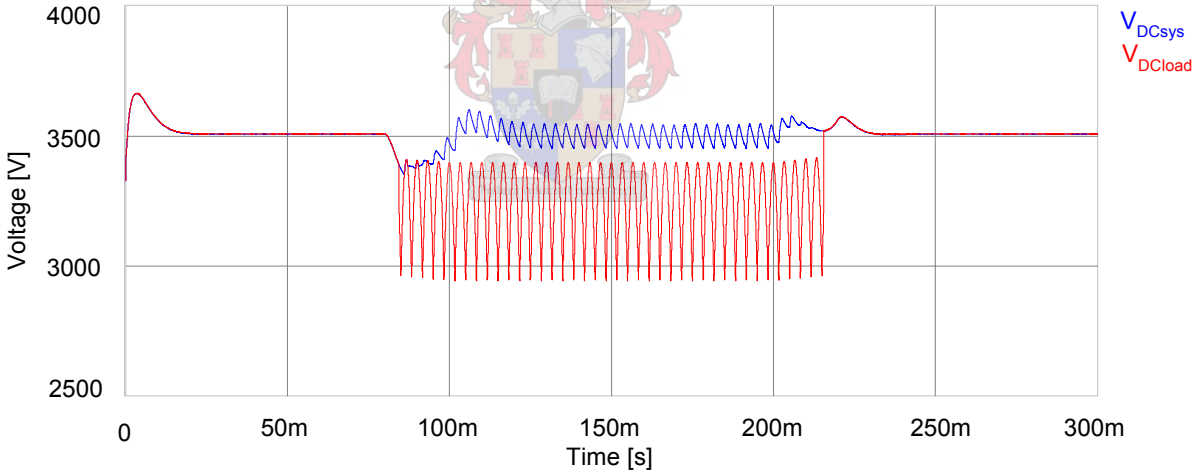


Figure 4.37 The DC-bus voltages of the System and the load

In the regeneration mode, the DC-bus of the system along with the DC voltage of the 3 kV line is kept at 3.5 kV. During the APF mode the 3 kV DC-line voltage drops to the rectified output voltage of the six-phase supply, while the systems DC-bus is kept at 3.5 kV.

A 300 Hz ripple is visible on both the of the voltage measurements during APF mode. The ripple on the 3 kV line is the direct effect of the six-phase supply voltages as shown in Figure 4.5. The ripple on the DC-bus of the system is due to the attempt of the system to compensate for the AC component of the real power drawn by the load.

The system enters regeneration mode again and after a small overshoot both voltages settle at 3.5 kV once again. The error between the reference voltage and the total DC-bus voltage measurement of the system as used to calculate the current reference for the DC-bus controller is shown in Figure 4.38.

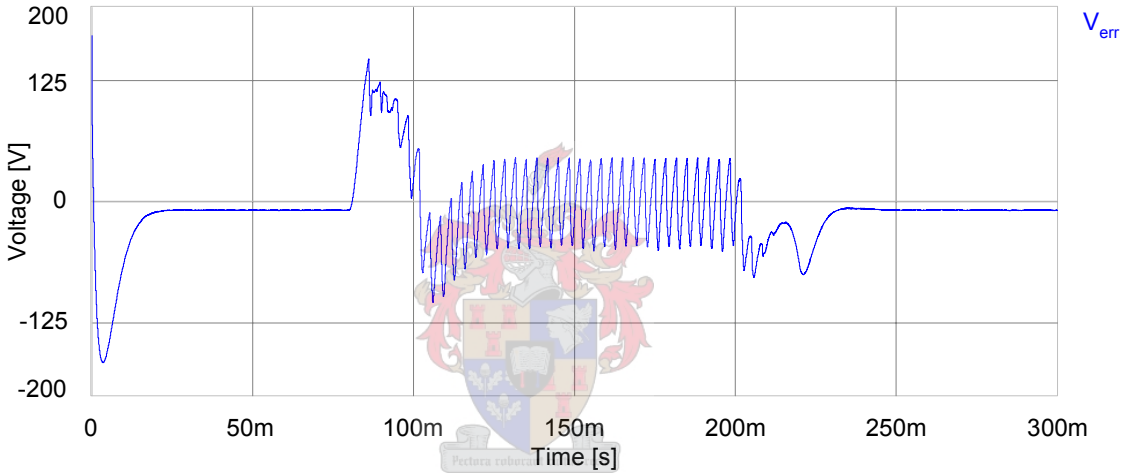


Figure 4.38 The error between the reference and total DC-bus voltage

During steady state, the voltage error can be reduced by increasing the low frequency gain of the Lag compensator by choosing a larger value for a, as described in 3.2.2. Since the error is ± 10 V (0.29%) it was not needed to compromise phase margin in favour of a smaller steady state error.

The voltage error along with the previous value of the voltage error is used by the digital implementation of the Lag compensator to calculate the reference current to regulate the DC-bus voltage of the system. This reference current, as shown in Figure 4.39, serves as the amplitude reference to the sinusoidal currents that the system has to output to regulate the DC-bus voltage.

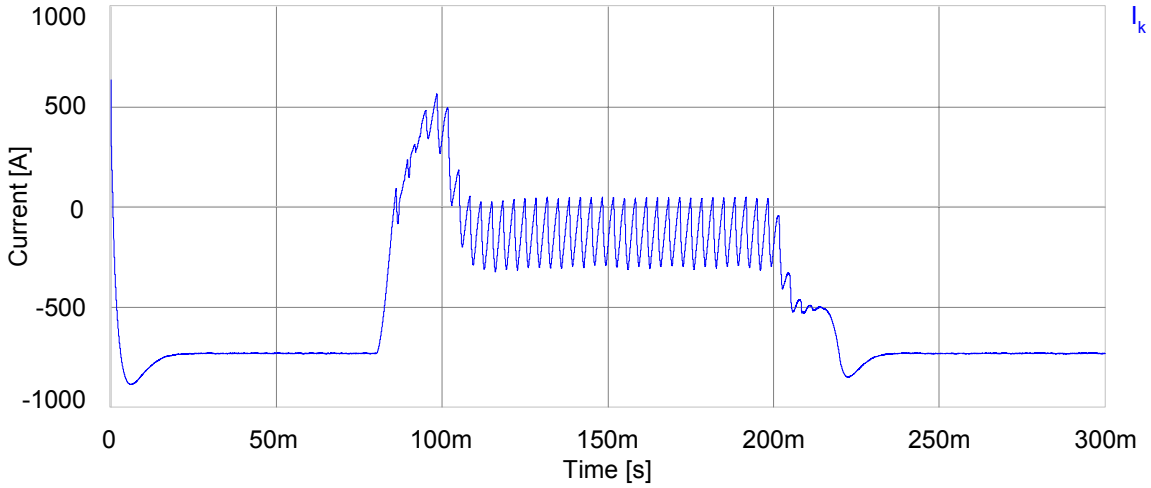


Figure 4.39 The DC-bus controller's reference current

Since the simulations were done for the natural balancing interleaved switching strategy, the individual DC-bus voltages are not regulated and the system relies fully on the natural balancing properties of the series-stacked converter to regulate the voltage sharing of the converter levels. Figure 4.40 shows that even without losses, the voltages over the seven converter levels share quite well. During APF mode though, the voltages start to diverge slowly. The divergence is however recalled when the system enters regeneration mode again.

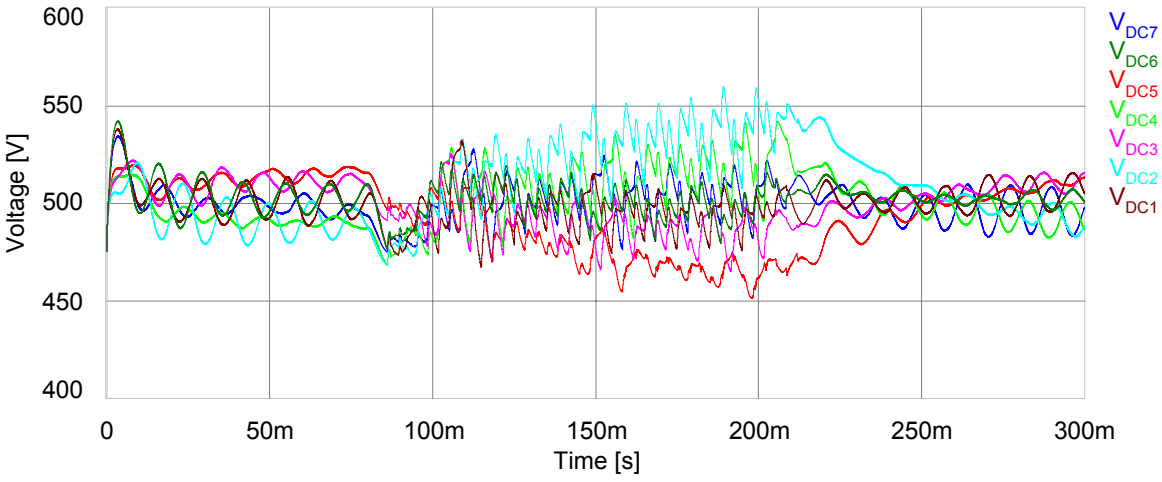


Figure 4.40 The individual DC-bus voltages

Since one of the natural balancing mechanism relies on the losses and parasitic elements [13] which were not included in this simulation, the DC-bus unbalance seen in Figure 4.40 would not cause complications.

The supply voltage and current for phase A is shown in Figure 4.41. From the simulation result one can distinguish between the filtering and regeneration mode of the system. In regeneration mode the supply current is 180º out of phase with the supply voltage, as can be seen for the time before 80 ms and the period after 220 ms.

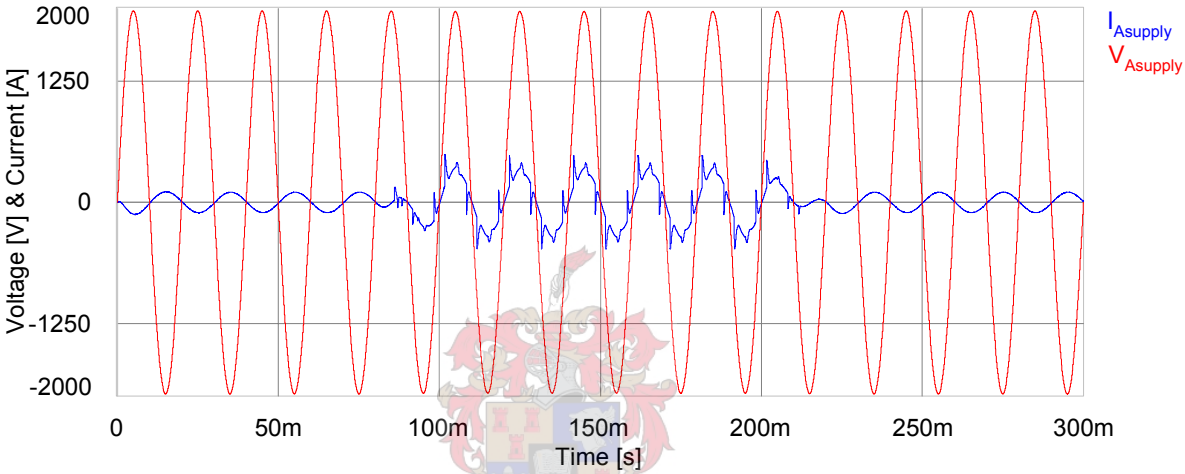


Figure 4.41 The phase A supply voltage and current

During regeneration mode, the diode rectifier is blocking, thus drawing no current from six-phase supply, and the series-stacked converter outputs a sinusoidal three-phase current which is injected into the supply. While the supply current is 180º out of phase with the supply voltage the utility network is supplying negative power, which in fact indicated that energy is absorbed by the utility network during regeneration mode.

The diode rectifier switches on once the 3 kV DC-line voltage drops below the peak voltage value of the six-phase supply. The current and voltage supplied by the utility network is in phase thus indicating that power is being drawn by the DC substation.

In Figure 4.41 the filtered supply current stays sinusoidal through the APF region of the simulation. Figure 4.42 takes a closer look at the behaviour of the phase A load

and supply currents, during the APF period. Using a current source as a load during the simulation, the load current profile becomes squarer than the wave from shown in Figure 4.8. The compensated supply current however looks much more sinusoidal and displays the characteristic glitches where the load current has an infinite gradient.

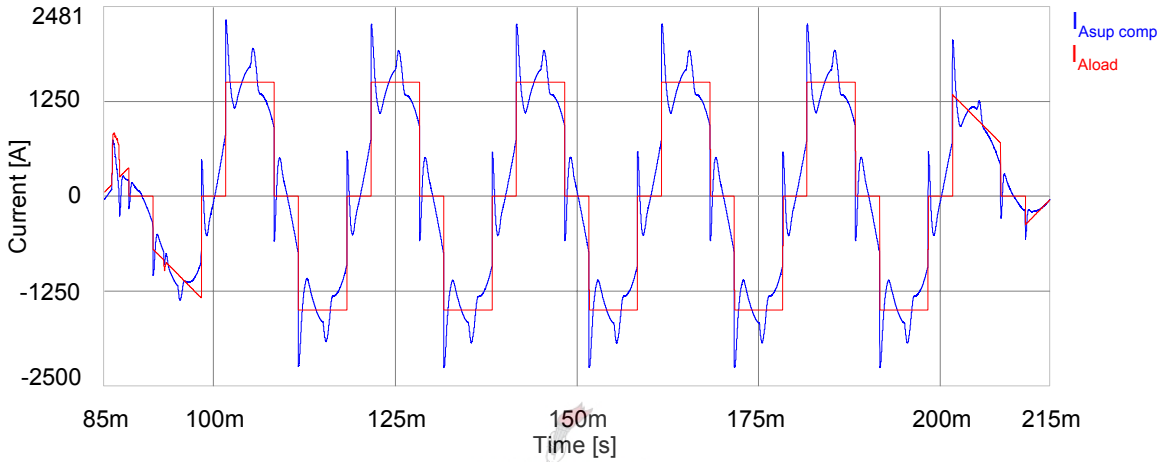


Figure 4.42 The load current and the filtered supply current

The phase A current reference and the output current of the system is shown in Figure 4.43, once again the regeneration mode and APF mode can be clearly distinguished.

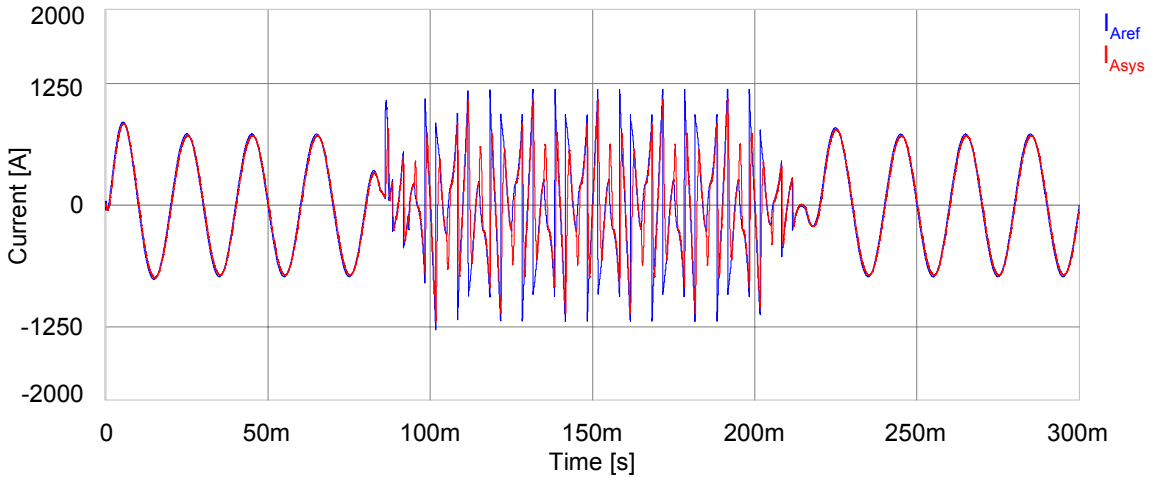


Figure 4.43 The reference current and the systems output current

To give a better account of what happens, a closer look is taken at the reference and the system's output currents during the transition between regeneration and AFP modes in Figure 4.44.

During the regeneration period the output current of the system follows the reference closely. The reference during the regeneration period is purely sinusoidal and is generated only by the DC-bus controller. As soon as the diode rectifier switches on, the system enters APF mode and the reference current is a combination of the DC-bus controller's output and the harmonic current reference required to filter the supply current.

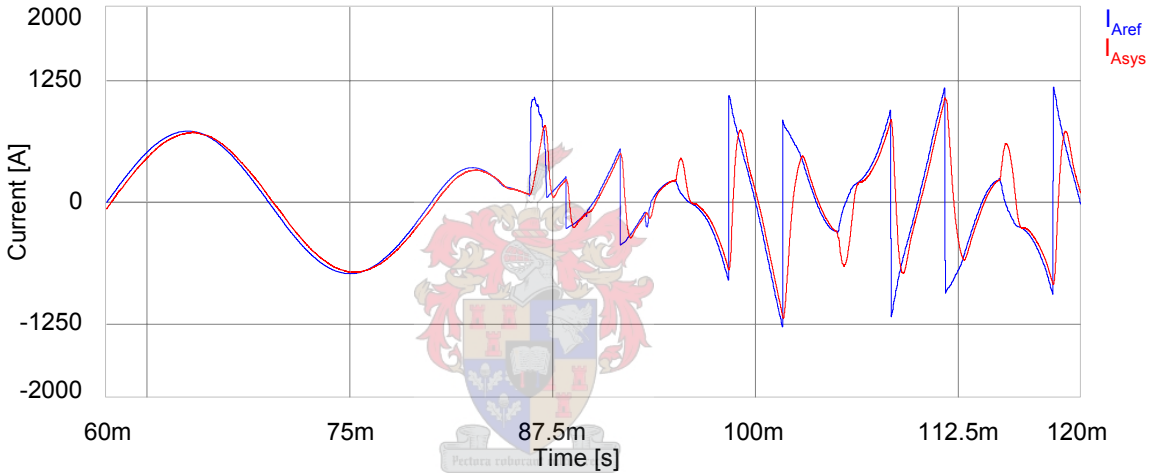


Figure 4.44 The current reference and systems response to the change from regenerating mode to APF mode

In the APF mode, the current reference seizes to be sinusoidal and exhibit regular step changes. The output current of the system continues to follow the reference current, but lags behind each time a step change occurs. Looking back to Figure 4.18 the effect of the DC-bus controller on the reference current can be seen, the ability of the system to follow the reference however stays the same. Despite the system's output current not following the reference exactly, the over all result is satisfactory.

To end off the simulations a look is taken at how the six-phase system reacts. In Figure 4.45 one of the six-phase load currents and the corresponding compensated supply current is shown.

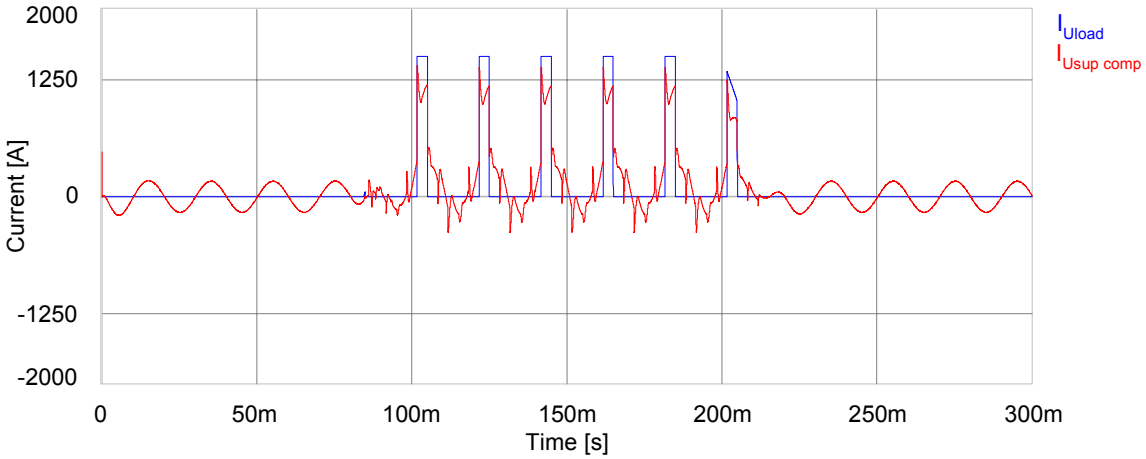


Figure 4.45 Six-phase load end supply current

As is in the three-phase case, a purely sinusoidal current is generated during the regeneration mode. This current is also 180º out of phase with its related supply voltage. Since the diode rectifier is off during the regeneration period, the load current is zero. Once the rectifier switches on, the load current takes on the profile of the six-phase rectified current. The load current (as result of the current source, as a load) is squarer than the load current for a resistive load as shown in Figure 4.7.

Since the load currents in the six-phase system has a DC component, the compensated six-phase supply currents cannot be purely sinusoidal. The compensated six-phase supply current is a combination of the DC component of the load current that circulates only through the secondary of the traction transformer and the 50 Hz sinusoidal component drawn from the three-phase primary of the traction transformer.

The compensated six-phase supply current can be better seen in Figure 4.46. Note that the load current is drawn between 30º and 90º and is not centred around the peaks of the compensated supply current. As a result of the converter compensating for the AC component of the real power the peak amplitude of the compensated six-

phase supply current is less than the peak current drawn by the load. The difference is thus supplied by the converter system.

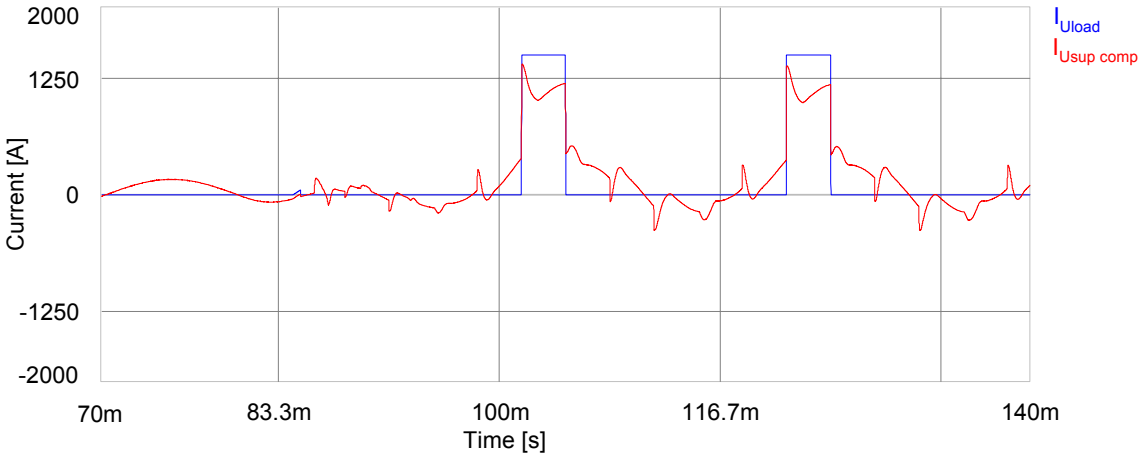


Figure 4.46 The transition from the regenerating mode to APF mode from the six-phase perspective.

The simulations confirm that the system topology as well as the control strategy to run the system does in fact perform the desired functions. Aspects such as the natural balancing of the DC-bus and the influence of losses and parasitic elements were further investigated in the physical system.

At the onset of planning it was thought that only one of the two rectifier bays in the substation would be active at any time. It was later discovered that the two rectifier systems run in parallel and since they have different topologies for their traction transformers, the utility network sees the substation as a twelve pulse rectified system. Since only one of the two rectifier bays are connected, only half of the supply current to the substation would be compensated. In addition the simulations show that the APF functionality has a mediocre performance, the significance of system thus relies on its performance as a power regeneration converter.

5. Implementing the control strategy in the prototype system

The converter system is controlled using a DSP based controller. The controller board calculates a set of three switching duty cycles every 28.57µs. The set of duty cycles is sent to the PWM Expansion board (PWM-EB), which in turn generates the interleaved gating signals for the 42 IGBTs. A block diagram showing the controller's connection to the converter system is shown in Figure 5.1.

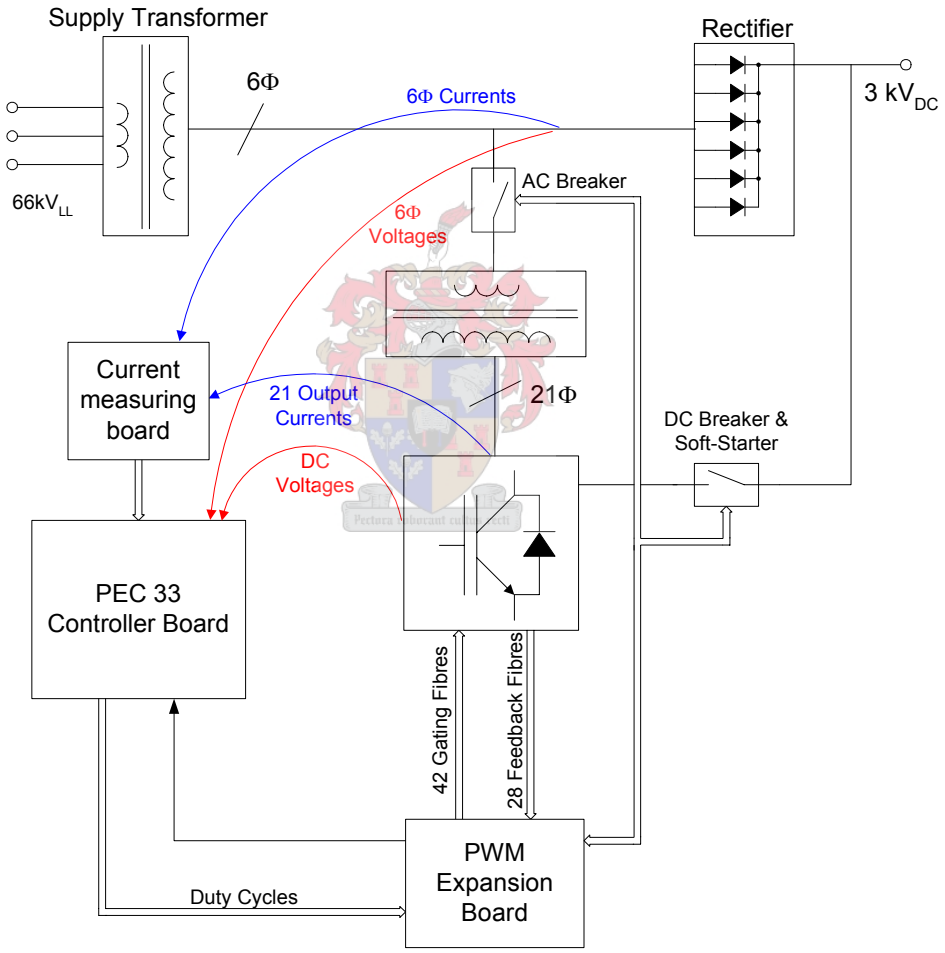


Figure 5.1 Block diagram the controller's connections

Along with the duty cycles, the PWM-EB also relays the control signals for the system. These include switching the AC breaker, DC breaker, Soft-starter, DC dump and cooling fans. As part of the system protection, the PWM-EB monitors the 33 error

and feedback signals generated by the system. The gating signals, control signals and their feedback signals are sent via eight identical optical driver boards that connect to the PWM-EB.

To calculate the duty cycles and control the system several, measurements are required. These include the DC-bus voltages and output currents of the converter of the system are measured as well as the AC voltages and currents on the six phase supply side. The voltage measurements are digitally encoded and connect through the PWM port of the PEC 33 controller board. The current measurements are analog and are made via four current measurement boards that connect to analog to digital converters (ADC) on the PEC 33 controller.

5.1. The PEC 33 digital signal processing board

The PEC 33 controller, which was designed as a reconfigurable general purpose power electronic controller [23], is used to control the system. The controller is based around a 32 bit floating point DSP (TMS320VC33 manufactured by Texas Instruments). The processor features internal dual-access SRAM and parallel floating point operations. This allows the processor to perform 150 million floating point operations per second (MFLOPS) and to execute 75 million instructions per second (MIPS) [28].

A block diagram of the PEC 33 controller board is shown in Figure 5.2. The DSP interfaces with the peripheral devices on the PEC 33 controller via two FPGAs. The peripheral devices include four dual channel DAC, four eight channel ADC, PWM in and output ports, LCD port, keypad port, two pairs of optical senders and receivers, RS232 serial port, a real time clock (RTC), Flash RAM and two external bus controllers.

FPGA-Main receives 24 address lines from the DSP, the four most significant bits are used to generate chip select (CS) signals for FPGA-Analog, Flash RAM 0, Flash RAM 1, External Bus 0 and External Bus 1. The memory map for the controller board is given in Appendix D1. The serial port, RTC and Flash RAM controllers are implemented in FPGA-Main. The onboard optical sender and receiver interface is also implemented by FPGA-Main. All the peripherals command and data registers are mapped as memory locations in FPGA-Main and are listed in Appendix D3.

FPGA-Analog accommodates the ADC, DAC, LCD, keypad and PWM port controllers. These peripheral devises are controlled by the DSP, by writing an instruction to the command registers in FPGA-analog. Data from the 32 ADC channels, 18 PWM input ports and the keypad are stored in individual data registers, in FPGA-Analog and are accessed by the DSP as external memory locations. The command registers and memory locations for FPGA-Analog are given in Appendix D4.

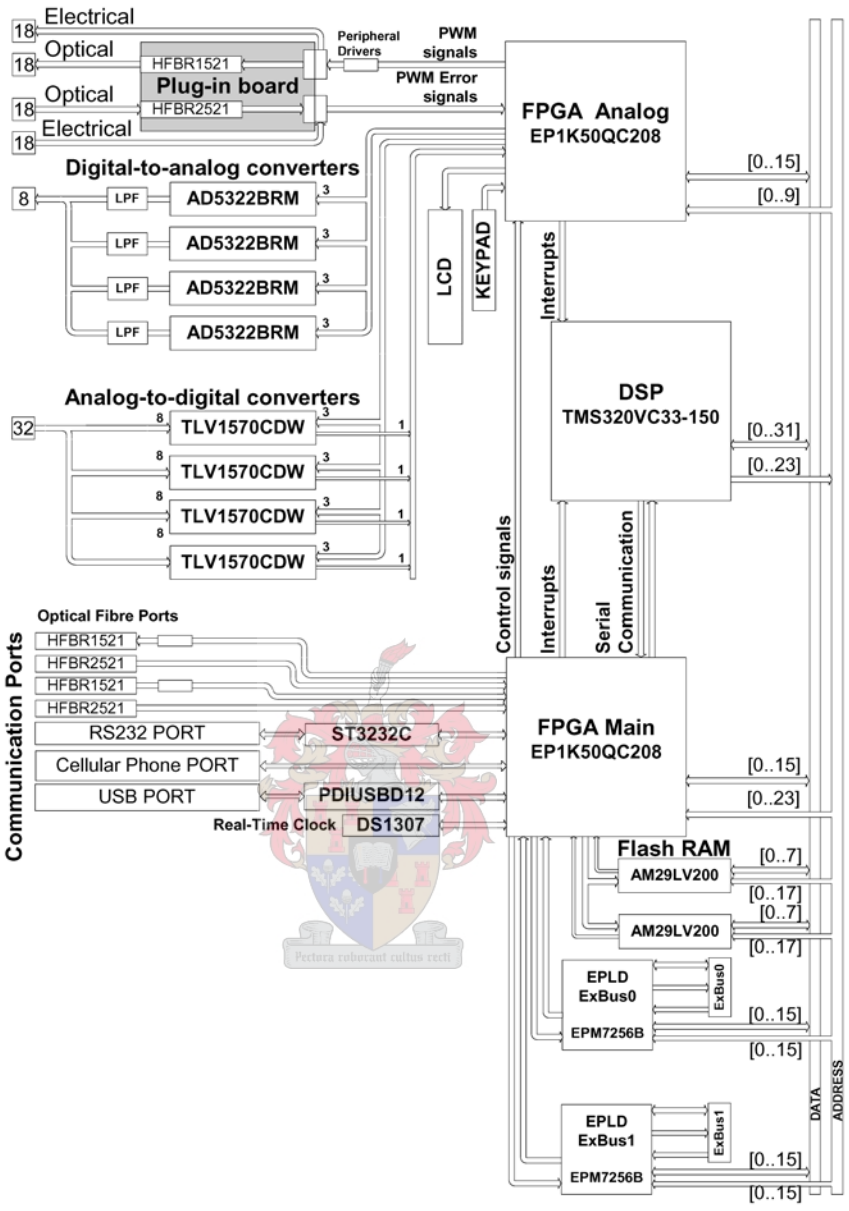


Figure 5.2 Block diagram of the PEC 33 controller board

The external data busses are also mapped as memory locations, each controlled by an EPLD. The EPLD acts as a buffer, receiving data directly from the DSP and then sending the data to an external board using a handshaking protocol. Data is read from the external board to the EPLD and then the DSP using a similar handshaking protocol.

The internal memory of the DSP and the two FPGAs are volatile, which means that once power is removed from the chips, they lose their data. This implies that each time the system is powered up, the DSP and FPGAs have to boot from a non-volatile source. The DSP can be booted from three sources, directly from a personal computer (PC) via the serial port, from the on board Flash RAM or from a PC using, a DSP emulator, connected to the JTAG port on the PEC 33. The FPGAs are booted from an EPC2LC20 configuration device on the PEC 33 controller board.

The controller is required to send new duty cycles to the PWM-EB every 28.57 µs. In order to calculate the switching duty cycles the DSP reads in eight DC voltages, six AC voltage, one DC current, six AC currents and 21 converter output currents. At the same time the DSP does the necessary safety checks. The safety checks are to protect the system against over voltage and over current. The eight DC voltage measurements are used to check for over voltage on the total DC-bus and on each inverter level. The over current checks are done on all 21 converter output currents.

5.1.1. Modifications to the PEC 33 controller

Since the VHDL code translates to a physical circuit, the Quartus II compiler calculates the maximum clock frequency (fmax) at which the circuitry would function correctly. The original firmware did not meet the speed requirements imposed by the 30 MHz and 75 MHz clock signals, routed to the FPGAs. Thus the firmware for both FPGAs and the external bus controller were rewritten. H.D Fuchs wrote the code to decode the digital voltage measurements, A.D le Roux contributed code for the LCD controller and N. van Greunen modified the serial communication controller.

In addition to meeting the required fmax for the new firmware an effort was made optimizing certain controllers. In particular the ADC, data and address controllers were streamlined. Using the new data and address controllers. The external memory access time for the DSP was reduced from requiring six wait states to three wait states, while the time required to sample all 32 ADC channels was reduced from more than 17.07 µs to 9.73 µs.

The PWM port of the PEC 33 controller was reconfigured as ports for the digital voltage measurement. The voltage measurements are digitally encoded by the voltage measuring board (VMB) and sent via optical fibres to the PEC 33 controller board. The PWM port has 18 pairs of senders and receivers which are routed to FPGA-Analog.

The original PEC 33 controller board used the EP1K50QC208-3 FPGA for both FPGA-Main and FPGA-Analog. Although only 37% of the logic cells in FPGA-Main are used, FPGA-Analog could not accommodate the code for the digital voltage measurement decoding along with all the other controllers assigned to it.

It was decided to use an EP1K100QC208-3 for FPGA-Analog. This device has double the amount of logic cells available, while retaining the same pin-outs. Even with the new chip, the firmware for FPGA analog used 97% of the logic cells. Using a larger FPGA for FPGA-Analog meant that the EPC2LC20 configuration device could not initiate both FPGAs. Since there are no pin compatible configuration devices that could program both FPGAs, a second EPC2LC20 chip was mounted on top of the original and their pins connected as described in Appendix C. The new firmware for the PLDs on the PEC 33 controller board is given on the CD accompanying this thesis.

5.1.2. The analog current measurements

The system measures the 21 converter output currents, six AC supply currents and the DC current into the DC-Bus. The 21 converter output currents are measured using LT 505-S LEM current probes, while the DC and six AC currents are measured using LT 2005-S LEM current probes [31]. The current probes generate current output signals, which are less susceptible to EMI than voltage signals. The LEM probes also provide electrical isolation between the controller and measured currents. Since the AC currents, especially the 21 converter output currents, have high order harmonic components, the current measuring system needs as high a band width as possible. This is achieved by keeping the current measurement in analog form and digitizing them in the PEC 33 controller board.

The ADCs on the PEC 33 controller board requires a buffered voltage input signal between 0 V and 4.096 V. The TLV1570 is a 10-bit ADC that has eight analog input channels and uses a four wire serial interface to FPGA-Analog [27]. An external reference voltage of 4.096V is supplied to the ADC as well as the current measurement boards (IMB). The 4.096 V is supplied by the REF198 reference voltage chip.

Since the ADCs on the PEC33 controller board require voltage input signals between 0 V and 4.096 V, the current measurement boards (IMB) was developed by H.D. Fuchs. The IMB receives the current output signals from the LEM probes and converts them to voltage signals [31]. The resulting voltage signals are inverted, which is compensated for in the DSP. The voltage signals are then level shifted and centred at 2.048 V. The level shifted voltage signal is then buffered by an operational amplifier, with a 5 V rail to protect the ADC against voltage spikes.

The 21 converter output current measurements are calibrated to measure a peak value of 800 A and the six-phase AC current measurements are calibrated to measure a peak current of 2000 A. The ADCs convert the input voltage signals to digital values between 0 and 1024, where 0 V corresponds to 0 and 4.096 V to 1024. The digitized current measurements are sent serially to FPGA-Analog from where the DSP can read them.

Each ADC connects to FPGA-Analog through a 4-wire serial interface. The ADCs requires a 16-bit configuration data set to initiate each analog to digital data conversion. Note that since the data is transmitted serially a configuration will only take effect on the next cycle. While the new configuration is sent to the ADC the sampled value invoked by the previous configuration is returned as shown in Figure 5.3 [27]. To minimize time spent configuring the ADC, the sampling sequence was hard-coded in FPGA-Analog. This meant that the DSP would only give one sample command to initiate the sampling sequence in all four ADCs.

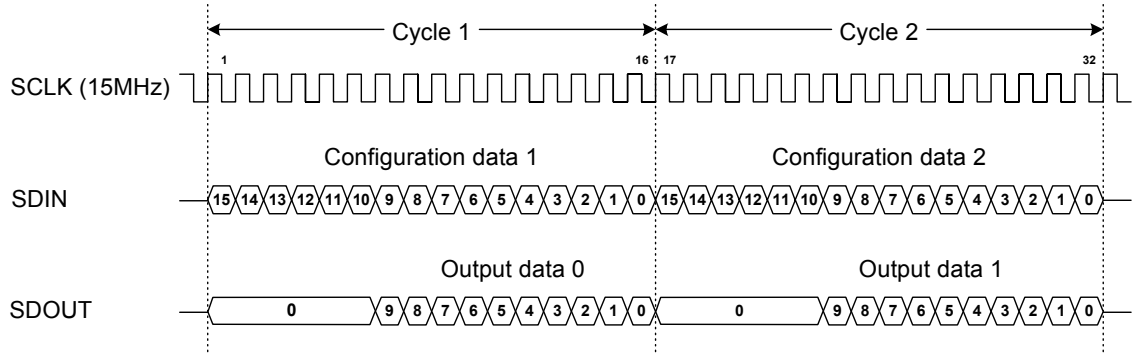


Figure 5.3 ADC configuration and data timing diagram

When the DSP reads a current measurement from FPGA-Analog, the value is read out of the FPGA as an integer. Although the DSP can read a 32-bit data bus, the FPGAs are only connected to a 16-bit data bus. Since the ADC only returns 10-bit data the most significant 22-bits of the 32-bit register is zeroed. The DSP then subtracts 512 from the register, this is done to shift the measured value back around zero. The last step is to type cast the register to a floating point value and multiply with the appropriate scaling factor to obtain the actual measured value.

5.1.3. The Digital voltage measurements

To provide electrical isolation between the controller and the voltage measurement equipment, the measured data is sent through optical fibres. The six AC voltage measurements are made with CV 4-5000 LEM voltage probes, which connect to the AC voltage measuring boards (AC-VMBs). The same probe and measuring board is used to measure the total DC-bus voltage. The seven DC-bus voltages of the individual inverter levels are measured using a resistive voltage divider on the DC-VMBs [31].

The output of the voltage probes are connected to a Voltage Measurement Board (VMB). The VMB digitizes the voltage measurements with a 12-bit ADC. The ADC then passes the data to an EPLD, which encodes the data end sends it serially via the optical fibre to the controller. Before digitalisation, the calibration adjustment is done using an AD620AN instrumentation amplifier [31]. The AC and total DC-bus voltage measurements were calibrated for a peak value of 4 kV, while the seven individual DC-bus voltage measurements were calibrated for a peak value of 600 V.

Since the CV 4-5000 voltage probes pick up a lot of noise, a RC filter is connected to its output, before the instrumentation amplifier. The filter was designed to have a cut off frequency of 312 Hz [31]. Although the filter only attenuates the 50 Hz component by 2% it introduces a phase shift of 9.1º.

The digitized data is sent serially, via optical fibres, to the controller board. To minimize errors during data transfer, the data is encoded. An EPLD on the VMB read the digitized measurement, encodes it and controls the data transmission. The basic component of the encode data is called a chip. Each chip has a duration of 200 ns (six 30 MHz periods). The data is related to logic transitions from high to low or low to high. Three different pulses are defined, an S-pulse, 1-pulse and a 0-pulse which are shown in Figure 5.4.

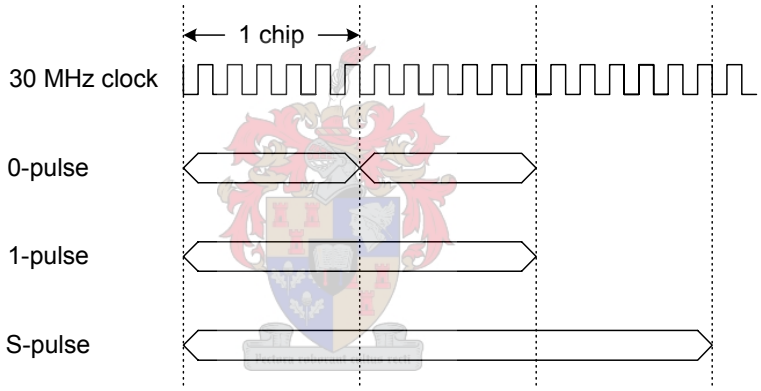


Figure 5.4 Diagram of the voltage data encoding

The S-pulse is used to synchronize the data transition and is sent while data is not being sent. The controller reacts to the synchronization pulses by sending a request pulse to the VMB, this initiates the data transfer sequence. A S-pulse is made up out of three chips having a constant level (either high or low). A 0-pulse represents a logic low and consists of two chips with a level change between them. The 1-pulse represents a logic high and is made up of two chips without a level change [31].

Using the 5 MBd optical senders, each data bit has a duration of 400 ns. The ADC under control of the EPLD has a conversion tome of 1.6 µs. This results in a 8 µs delay between a data request and a complete data transition. The delay is

insignificant, since the 50 Hz supply voltage level does not change much in the time between data requests every 28.57 µs (35 kHz).

On the PEC 33 controller, the optical fibres carrying the voltage measurements plug in on the “PWM error port”. The “PWM output port” is used to send data request signals to the VMBs. The data reaches the controllers serially and is decoded by FPGA-Analog, as the data is received. Of the 16 data bits received, the least significant 12 data bits represent the signed voltage measurement, while the four most significant bits are used as parity bits. If data is lost or corrupted during transmission, the last valid measurement received, is kept in the output register. To minimize the effect of clock drift between the clock on the VMB and the clock on the PEC 33 controller board, the sampling clock of the decoder synchronises on every falling edge of the received data.

The DSP reads the voltage measurements as integers into 32-bit registers. The data is then bit-shifted to the left, 20 times, to move the sign bit from bit 12 to bit 32. The register is then shifted right 20 times, to return the voltage measurement to the 11 least significant bits. The registers are then type cast to floating point values and scaled to obtain the actual measured voltages.

5.1.4. The External Bus communication

Since the PEC 33 controller board does not have enough PWM output ports to switch the converter system, the PWM-EB was developed. The DSP calculates a set of duty cycles. The duty cycles are then sent via the external data bus to the PWM-EB. The PWM-EB then use the duty cycles to generate the 42 interleaved PWM gating signals.

The PEC 33 controller board has two external data bus (ExBus) communication ports. The ExBus ports are mapped through two EPLDs, which implements the ExBus controllers. In effect they functions as a buffer between the DSP and the external data bus, buffering data and then sending it over the ExBus, while the DSP continues with is operations. A block diagram of the external data bus is shown in Figure 5.5, including the control lines.

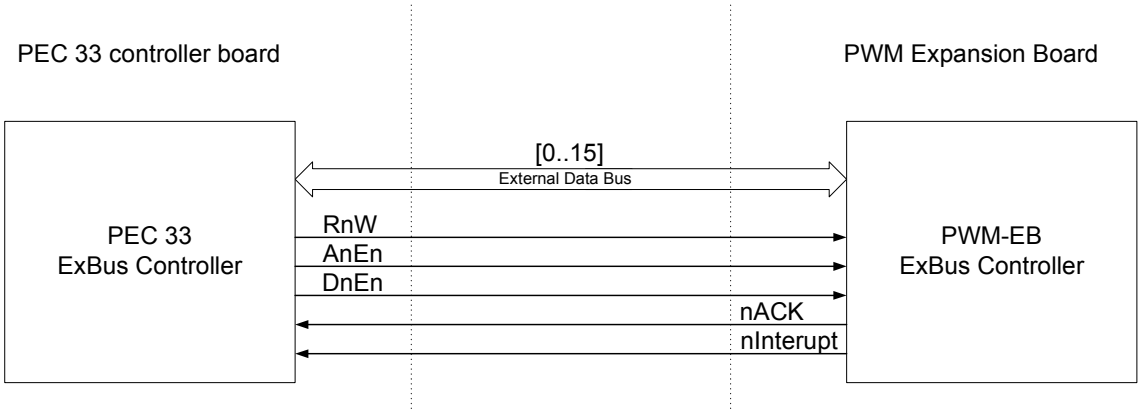


Figure 5.5 Block diagram of the External Data Bus connection

Using the control lines; Address-not-Enable (AnEn), Data-not-Enable (DnEn), Read-not-write (RnW), not-acknowledge (nACK) and a not-Interrupt line, communication across the external data bus is implemented using a handshaking protocol. The not-Interrupt line is routed from the EPLD through FPGA-Main to the DSP as an external interrupt port. Figure 5.6 shows the basic functioning of the protocol for a write cycle.

The super-script numbers in this paragraph correspond to the points in time shown in Figure 5.6. The ExBus EPLD on the PEC 33 buffers the address and data that the DSP writes to the external data bus. The PEC 33 ExBus controller first sets the RnW[1] to the appropriate level, then puts the address on the data bus[2] and pulls AnEn low[3]. The PWM-EB ExBus controller latches the address once AnEn is low[3] and pulls the nACK line low[4]. On seeing the nACK line pulled low[4] the PEC 33 ExBus controller resets the AnEn line[5]. Once the AnEn line has been reset[5], the PWM-EB ExBus controller resets the nACK line[6]. The PEC 33 ExBus controller puts the data on the external data bus and pulls DnEn low[7]. The PWM-EB ExBus controller latches the data and pulls the nACK line low agian[8]. The PEC 33 ExBus controller resets DnEn[9] once nACK is low[8] which signals that the data transfer has been completed, the RnW line is reset[10] and the data bus is tri-stated.

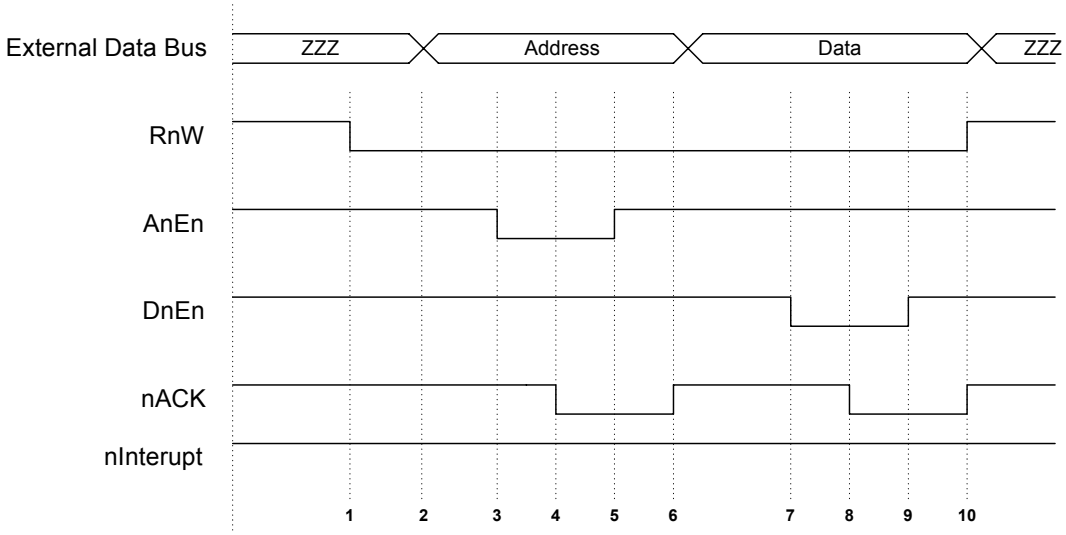


Figure 5.6 Diagram showing the handshaking data transfer protocol

The DSP reads data from the ExBus using the same handshaking protocol. The DSP does however have to perform two read operations to receive the data from the external bus. During the first read operation, the address that is being read from is buffered in the ExBus controller and the read operation to the specified address is done across the external data bus. The ExBus controller makes the data received from the external bus, during the previous read cycle, available to the DSP. Thus the DSP has to perform a second read operation to receive the newly requested data.

Since a set of duty cycles have to be calculated and transmitted to the PWM-EB every 28.57 µs, timing requirements on the PEC 33 controller board are extremely tight. It was decided to combine the address and data that is transferred, in order to reduce the duration of the external data bus read and write cycles. Since the PWM duty cycles are represented as a 10-bit value, there are 6-bits, allowing 64 memory locations to be addressed by the external data bus. Of the 64 memory locations the PWM-EB only uses ten, as listed in Appendix D.5 (The memory map for the PWM Expansion Board). The new ExBus data transmission protocol is thus concluded when the nACK resets[6].

5.2. The PWM Expansion Board

The PWM-EB was developed to generate the interleaved gating signals. A bock diagram of the PWM-EB is shown in Figure 5.7. Two FPGAs had to be used to provide enough input and output pins to control and monitor the converter system. In addition to the FPGAs, the PWM-EB has an EPLD to control the external data bus communication and route the data to the appropriate FPGA.

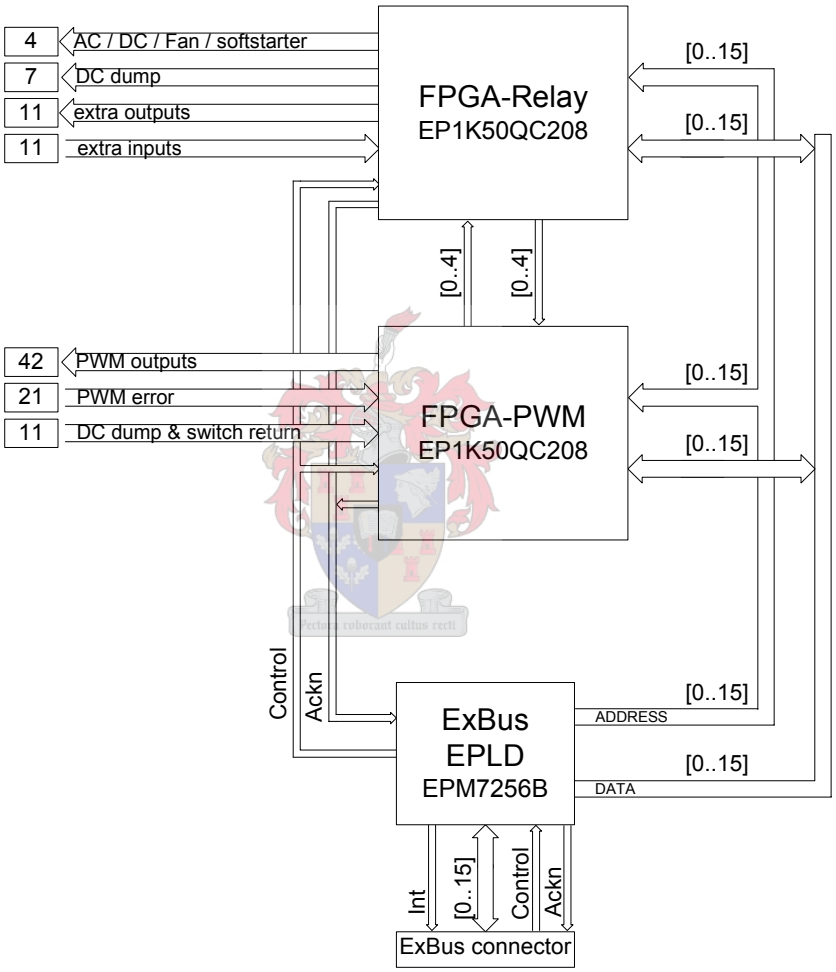


Figure 5.7 Block diagram of the PWM Expansion Board

FPGA-PWM generates the interleaved gating signals to switch the 42 IGBTs and monitors the 21 error and 11 status return signals from the converter system, as well as governs the timing of duty cycle requests. A set of three duty cycles are requested from the PEC 33 controller, by sending an interrupt signal via the ExBus to the DSP.

The other switching signals are handled by Relay-FPGA. These switching signals are for the AC breaker, DC breaker, the cooling Fans, the Soft-starter contactor and the seven DC dump IGBTs. A number of extra input and output ports were defined and routed to the various optical driver board ports. The schematics and PCB layout for the PWM-EB are given in Appendix A1 and Appendix A2 respectively.

The gating signals, generated by the PWM-EB and the return signals, from the converter system are sent via optical fibre, which provides electrical isolation between the controller and the converter system. To keep the 85 optical fibres that connect to the PWM-EB manageable, the optical senders and receivers were put on eight identical optical driver boards (ODB). The ODB connects to the PWM-EB through eight separate, 34-pin, ribbon cable connector. Each ODB has eight optical senders and five optical receivers. The schematics and PCB layout for the ODBs are given in Appendix B1 and Appendix B2 respectively.

The IGBT driver boards are configured so that an IGBT switches on when the optical fibre transmits light. This prevents the IGBTs from being switched if a fibre breaks or comes loose. The IGBT driver boards are set up so that the error and return signals transmit light while there are no errors. Thus the PWM-EB will pick up an error if an optical fibre is broken as well as when an error signal is transmitted. To reduce the amount of optical fibres needed to monitor the converter system, it was decided to combine the error feedback of the top and bottom IGBTs on each phase arm in the converter. The IGBT diver boards also make it possible to distinguish between a short circuit and an over temperature error.

To protect the system, FPGA-PWM monitors all the error feedback signals and implements a watchdog timer. The watchdog timer signals an error if the requested duty cycle data does not arrive within a specified in time. All gating signals are disabled as soon as an error is detected. The error is logged in an error register, which is read by the DSP as soon as the shut down sequence has been completed. The error codes are listed in Appendix D6.

5.3. Interleaving the PWM gating signals

21 separate PWM blocks are implemented in FPGA-PWM, one for each converter IGBT phase arm. The PWM blocks compares 10-bit duty cycle values with triangular carriers generated in the FPGA, to generate the gating signals. While the duty cycle is greater than the value of the triangular carrier, the top IGBT of the phase in question is on and while the duty cycle has a smaller value than the carrier the bottom switch is on, as shown Figure 5.8. The PWM block ads 5 µs dead time to the gating signals to ensure that the top and bottom switches on a phase arm are not on at the same time.

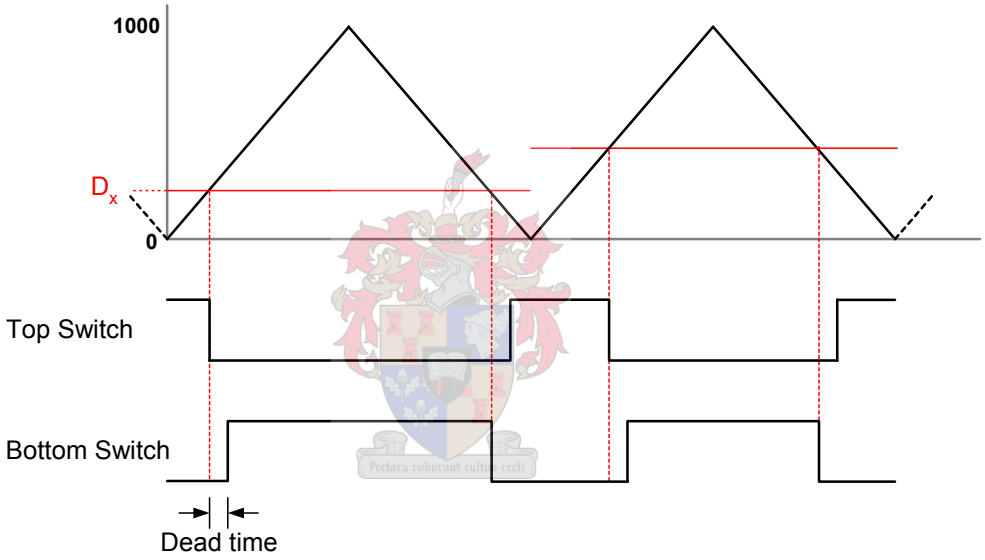


Figure 5.8 Diagram of the PWM generation, including dead time

A 10-bit counter is used to construct the triangular carrier. The counter stats at 0, increments every 100 ns until it reaches 1000. The counter then decrements every 100 ns, thus constructing a 5 kHz triangular carrier. When the descending counter reaches 280, an interrupt signal is generated. This leaves 28 µs between the generation of the interrupt signal and the counter reaching zero. The interrupt signal is sent to the DSP via the ExBus to request a set of duty cycles for the inverter level in question.

To start switching the converter system, the DSP sends the “PWM enable” command to the PWM-EB. FPGA-PWM starts the first counter and 28.57 µs later the next one and so on, until all seven counters are running. 172 µs after the first counter starts, it generates the first interrupt signal, requesting a set of duty cycles for level 1 of the converter system. The DSP subsequently receives interrupt signals every 28.57 µs. The firmware run in the PWM-EB is included on the CD accompanying this thesis.

When the DSP receives an external interrupt from the PWM-EB, it reads in all the measurements and calculates the switching duty cycles, which it then sends to the PWM-EB. FPGA-PWM routes the received duty cycles to the relevant PWM block. The new duty cycles reach the PWM block before the counter reaches zero. The new duty cycles are latched, and as soon as the counter reaches zero the new duty cycles are used to generate the gating signals for the next cycle. The DSP takes between 21 µs and 26 µs to calculate and send the requested duty cycles. Since the request is made 28 µs before the counter reaches zero, the new data arrives 2 µs to 7 µs before it is used. The controller does not compensate for the effect due to the duty cycles being calculated 28 µs before they are used. This causes a slightly under damped system response.

If the new duty cycles do not arrive in time the system stops and shuts down, opening the contactors and discharges the DC-bus. The operator is able to view the error message and restart the system.

5.4. Controlling the system

The DSP controller boots from Flash RAM on the PEC 33 controller board, when the system powers up and works as a stand alone control system. Although the controller does have a LCD display and Keypad as user interface, the operator in the substation does not have access to them, since the controller is mounted in an EMI shielded housing. The whole system is controlled from a single On / Off switch (SW), mounted on the DC breaker control panel. This switch, like all the other external components has an optical fibre link to the controller.

The only time an operator would work directly with the controller is when data that has been logged is downloaded to a PC or new code is loaded into the Flash RAM. Both of these operations require a PC to be connected to the PEC 33 controller through the RS 232 serial port.

The DSP code is written in C and is based on a cooperative multi-threading structure. Functions like writing to information the LCD, retrieving the value of a pressed key, read and writing to the Flash RAM, reading the real time clock and navigating the user menus are based on a multi-threading structure. This entails monitoring the status of a process, and only executing the instructions if that process does not indicate a busy status. If the process does indicate that it is still busy, the code skips to the next process, instead of waiting for the other process to finish first. The time critical part of the DSP code is situated in an externally triggered interrupt procedure. The external interrupt is generated by the PWM-EB when the system is running and a new set of duty cycles is requested. While the system is running (switching) a watchdog timer is implemented using one of the DSP's internal timers, along with a timer interrupt procedure. If the watchdog timer runs out the system is shut down and waits in "safe state" until the system is restarted. The DSP's code is available on the CD accompanying this thesis.

The overall system control is done using a state based algorithm, with states defined as shown in Figure 5.9. When the system powers up, the DSP is booted from the Flash RAM and the code starts executing. During the "Initialize" state the DSP and PEC 33 controller board's peripheral devices are configured. For the DSP this

includes the primary bus control register, the internal timers, disabling all interrupts and calculating the Fourier lookup tables which are used to synchronize to the utility network. On the PEC 33 controller board the DACs are configured and the LCD is initialized.

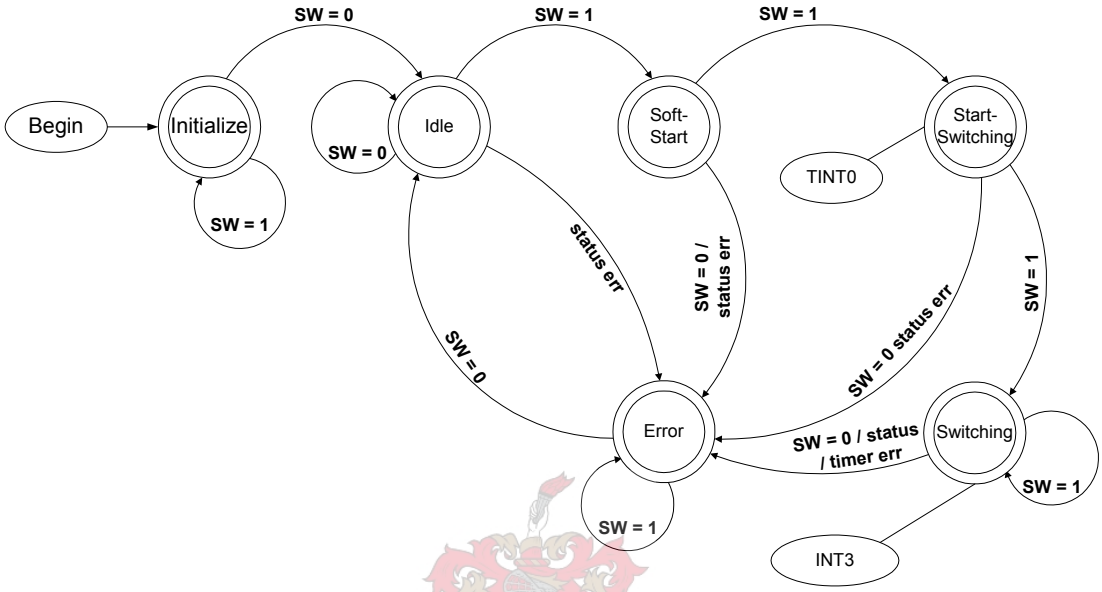


Figure 5.9 State flow diagram for the DSP code

After the DSP and PEC 33 controller board has been initialized, the converter system is initialized and in a safe state before the "Idle" state is entered. This involves switching the soft-starter off, opening the DC and AC breakers and switching DC dump on. The controller then waits until the On / Off switch is switched off before entering the "Idle" state. In the state flow diagrams the On / Off switch is referred to as SW, where SW = 0 indicates off and SW = 1 indicates on. During the "Soft-start", "Start-Switching" and "Running" states the system can be stopped by the operator, simply by turning the On / Off switch off. The controller sees SW = 0 and goes to the "Error" state.

During the "Idle" state the system is in a safe condition, all the contactors are open and the DC bus is discharged (DC Dump is on). The "Idle" state checks the status of the Soft-starter, AC contactor and DC contactor. If an error is detected from one of the status the system enters the "Error" state. From the "Idle" state the system moves to the "Soft-start" state when SW = 1.

The “Soft-start” state controls the charging of the DC-bus from the 3 kV DC side as well as closing the DC and AC breakers once the DC-bus has been charged. A flow diagram showing the “Soft-start” state is shown in Figure 5.10.

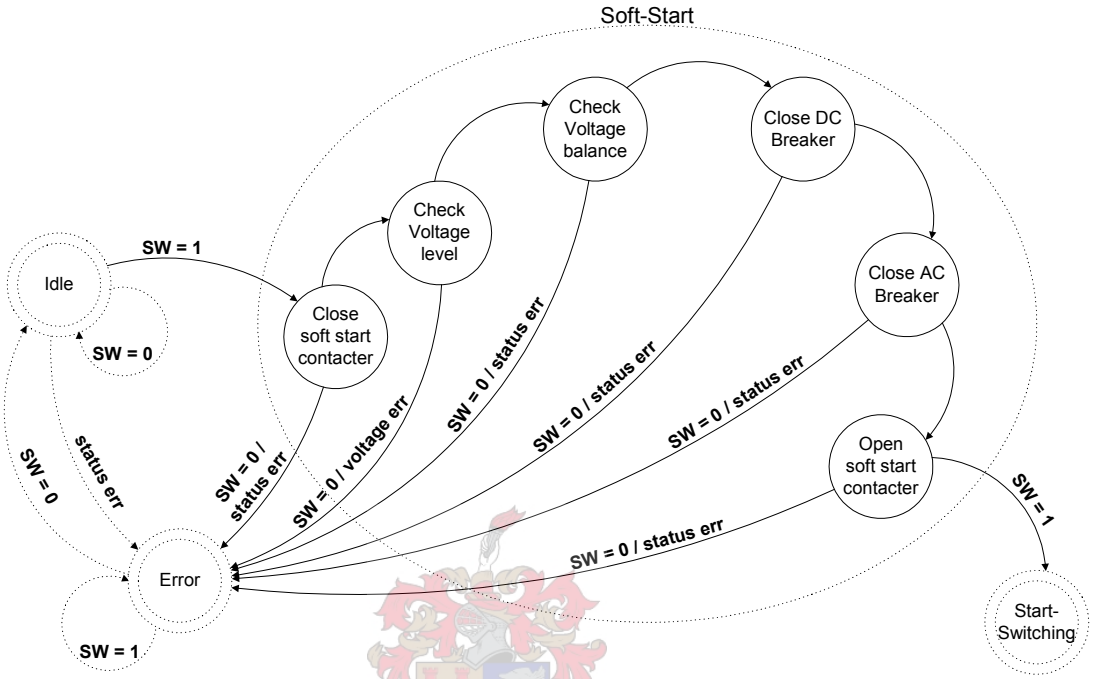


Figure 5.10 Flow diagram of the "Soft-Start" state

The soft-start sequence starts by switching the DC Dump off and switching the soft-starter on. The DC-bus then charges from the 3 kV DC-line through a set of resistors. This takes approximately 4 s. While the converter system’s DC-bus charges, the controller monitors the total DC-bus voltage as well as the voltage across each inverter level. At this stage the controller checks for over voltage. As soon as the DC-bus voltage reaches 3 kV, the controller checks the voltage balancing between the seven inverter levels. If everything is fine the DC breaker is closed. The DC breaker takes approximately 4 s to close, as soon as the DC breaker is closed the soft-starter switches off. The AC contactor then closes and the controller goes the “Start switching” state. If at any stage in the “Soft-start” state an error is picked up or SW = 0, the controller goes to the “Error” state.

The PWM-EB starts the triangular carriers and start requesting duty cycles after it receives the PWM enable command. The “Start-Switching” state gives the PWM enable command and enables the DSP’s interrupts, used by the system while the converter is switching. Figure 5.11 shows the flow diagram for the “Start-Switching” state.

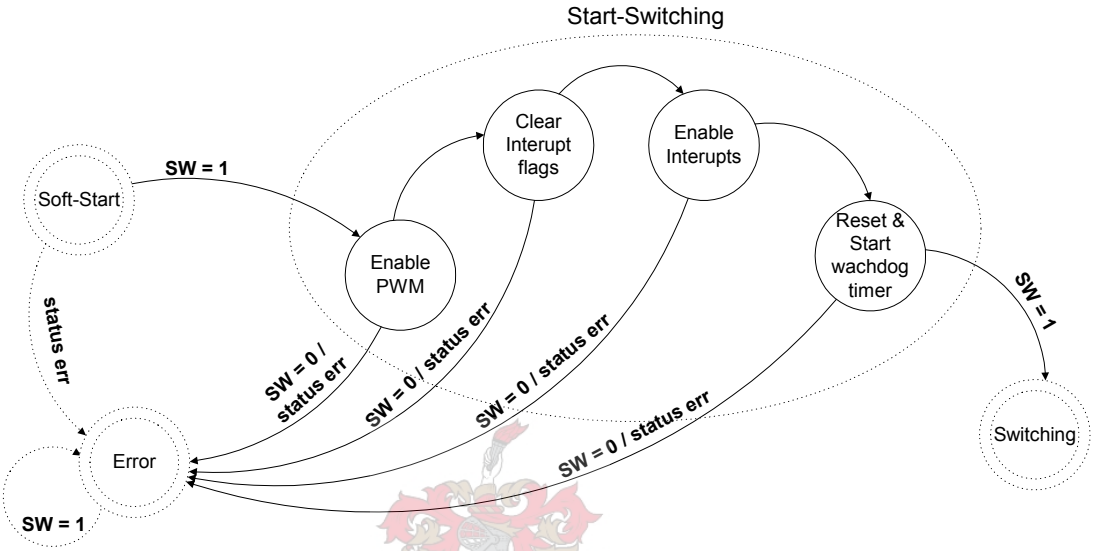


Figure 5.11 Flow diagram of the "Start-Switching" state

In the “Start-Switching” state, the DSP writes the enable command to the PWM enable register on the PWM-EB. All interrupt flags are cleared before the internal timer 0 (TINT0) and the external interrupt 3 (INT3) are enabled. The period for timer 0 is set and timer 0 is started, where after the “Switching” state is entered.

INT3 is triggered by the PWM-EB when a set of duty cycles is requested. TINT0 is used as a watchdog timer, to check that data requests occur within an acceptable time period. When the timer runs out the PWM disable command is sent to the PWM-EB. The state machine enters the error state and shuts down the system.

Since the first INT3 is generated 172 µs after the PWM enable command is given, the period for timer 0 is set to 220 µs in the “Start-Switching” state. Once the first INT3 has been received, INT3 is generated each 28.57 µs, for which the period of timer 0, the watchdog timer is to 40µs.

During the “Switching-state” the DSP processing is mostly interrupt driven. Tasks such as writing to the LCD, reading keystrokes and writing to the Flash RAM have low priorities and thus take place in the free time between interrupt calls. In the “Switching” state the controller checks the status of the contactors as well as the value of SW. While the system is running INT3 is triggered every 28.57 µs. The interrupt procedure is used to calculate the new switching duty cycles. Figure 5.12 shows the flow diagram for the “Switching” state as well as for INT3.

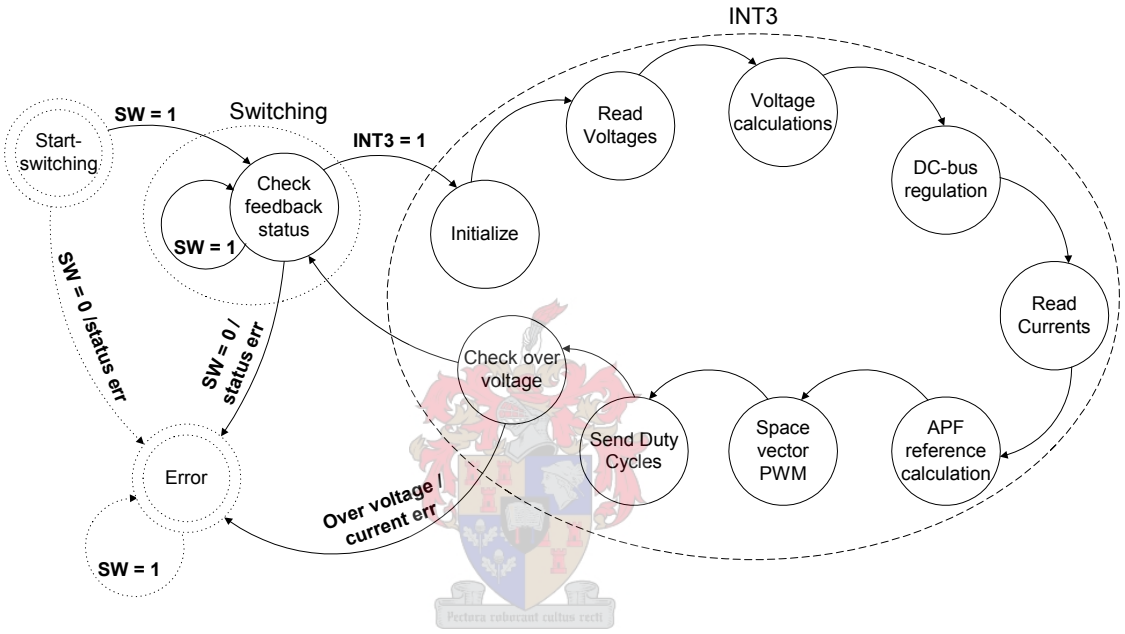


Figure 5.12 Flow diagram of the "Switching" state and the external interrupt three procedure

Only while the controller is in the “Switching” state will INT3 be enabled. When INT3 is called it first resets the timer 0 and gives the ADC sample command. While the ADCs are sampling the currents, the voltage measurements are read into the DSP. The DC voltage measurements are filtered, using an infinite response digital filter, to remove noise on the measurements. The six AC voltage measurements are used to compute the three-phase equivalent voltages. The synchronization calculations are also performed at this time. After the synchronization signals have been computed, the DC-bus regulator’s reference is calculated.

The 21 converter currents, the DC and the six AC currents are then read in. As the currents are read, the DSP checks for over current on the 21 converter current measurements. The next step is to calculate the reference currents for the APF functioning of the converter. The reference currents are combined and the α-β reference voltages are calculated. Space vector PWM is then used to construct the three-phase duty cycles. The three duty cycles are then sent to the PWM-EB via the ExBus. The interrupt procedure then checks for over voltage on the DC-bus voltage measurements before exiting.

The system is can be stopped at any time by the operator, by switching SW to 0. The system will then enter the "Error" state, which shuts down the whole converter system. If any error is detected, over voltage, over current or converter status error the "Error" state is also entered into. Figure 5.13 shows the flow diagram for the "Error" state.

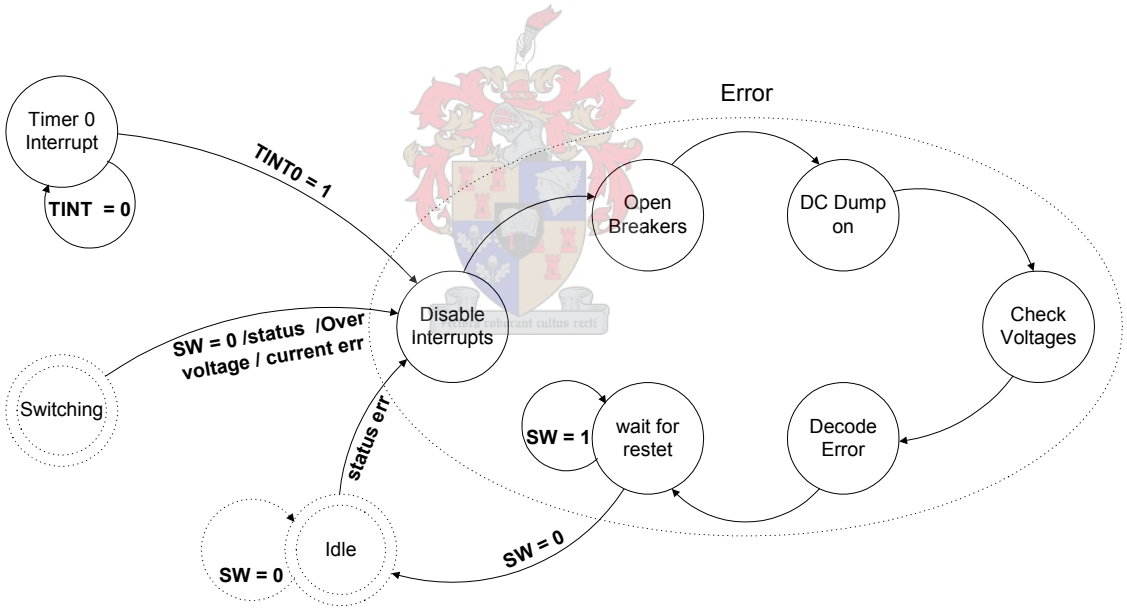


Figure 5.13 Flow diagram of the Error state

The "Error" state shuts down the converter system and waits for a manual reset by the operator. The PWM disable command is written to the PWM-EB to stop the generation of gating signals. The interrupts, TINT0 and INT3 are disabled. Next the DC breaker, soft-start contactor and AC breakers are opened. As soon as the system is disconnected from the AC and DC supplies the DC dump is switched on. The DSP

then reads in the DC-bus voltage measurements, to check whether all the DC-busses have discharged. The DSP then reads the error codes from the PWM-EB and checks the internal error register. The error is decoded and displayed on the LCD. The system then waits for the manual reset by the operator. When the operator switches the main switch off, the system returns to the “Idle” state, where it waits for the main switch to be turned on again.

The system keeps a log of the total DC-bus voltage and DC current during the time that the system is regenerating energy. The time is read from the RTC and logged when the system starts to regenerate energy. The voltage and current measurement is logged every 10 s during the regeneration period. Due to the limited memory available in the Flash RAM a different protocol for data logging will be implemented during long term tests. During these long term test, the start and stop times of each regeneration period will be logged, along with the average power, regenerated power and the peak value of the regenerated power during each regeneration period.

5.5. Practical results

Preliminary tests were done at the University of Stellenbosch. Because of the limited power supply to the laboratory and the size of the system, each level was tested separately at full rating. The full system was first tested with the outputs of each converter level's filter inductors shorted. The full system tests were performed using DC-bus voltages up to 3.5 kV. The high DC-bus voltages did however restrict the amount of current that could be switched. The main objective with these tests were to test the controller and the measuring system.

The final tests at the laboratory were done with the system's outputs connected to a scale model of the injection transformer. During these tests the seven levels were switched using interleaving PWM. Due to the high power rating of the system and the six phase output of the injection transformer the system could not be tested in the laboratory with a load.

This meant that the system had to be installed in a DC substation before it could be tested in full. The major disadvantage of testing in the substation is that the system has to be connected and tested at full rating, while not having any control over the tests conditions. Since the system has so many measurements and the individual inverter levels sit at different off set voltages, most of the test results were monitored via the DAC converters on the PEC 33 controller board.

Preliminary tests at the substation repeated the tests done at the university, this time however, the six-phase current and voltage measurements were used to calculate the switching references. The six-phase to three-phase transformations were also tested to verify their validity. Since the control strategy is based on a three-phase system, the six-phase measurements are converted to their three-phase equivalent values. The seven three-phase output currents of the converter system are also combined to give an equivalent three-phase system. This is used to calculate the natural balancing interleaved reference signals.

The APF reference current, calculated using the six-phase measurements, the reference current for phase A and the three-phase output of the converter system is shown in Figure 5.14.

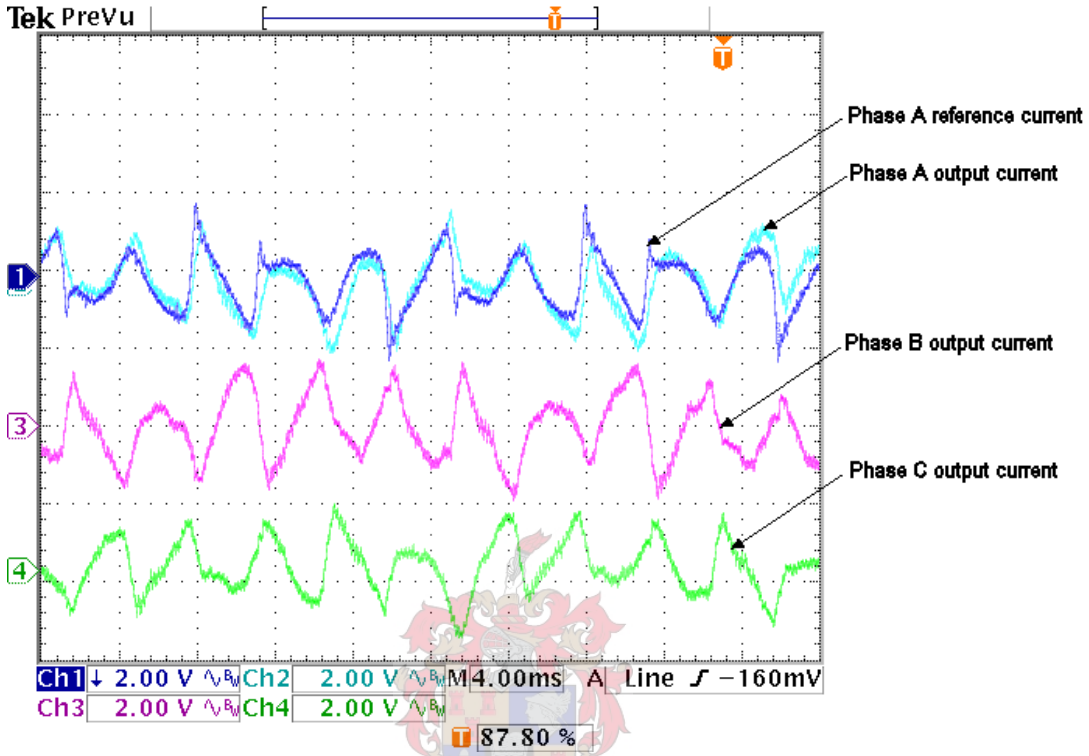


Figure 5.14 The reference current for phase A and the converter output currents for phase A, B and C

The three-phase output of the converter is the sum of the output currents of the seven inverter levels. Figure 5.14 shows that the reference current is followed quite closely.

In Figure 5.15 the APF reference current for phase A and the phase A output current of the converter system are shown (note that channel 1 is on a 1 V scale while channel 2 is on a 500 mV scale). Phase A of the equivalent three-phase load current is shown on channel 3 (the load current is calculated from the six-phase current measurements, assuming a star connected three-phase primary). Channel 4 shows the predicted compensated supply current for phase A. The predicted current is calculated by subtracting the measured converter output current, shown on channel 2, from the three-phase load current, shown on channel 3.

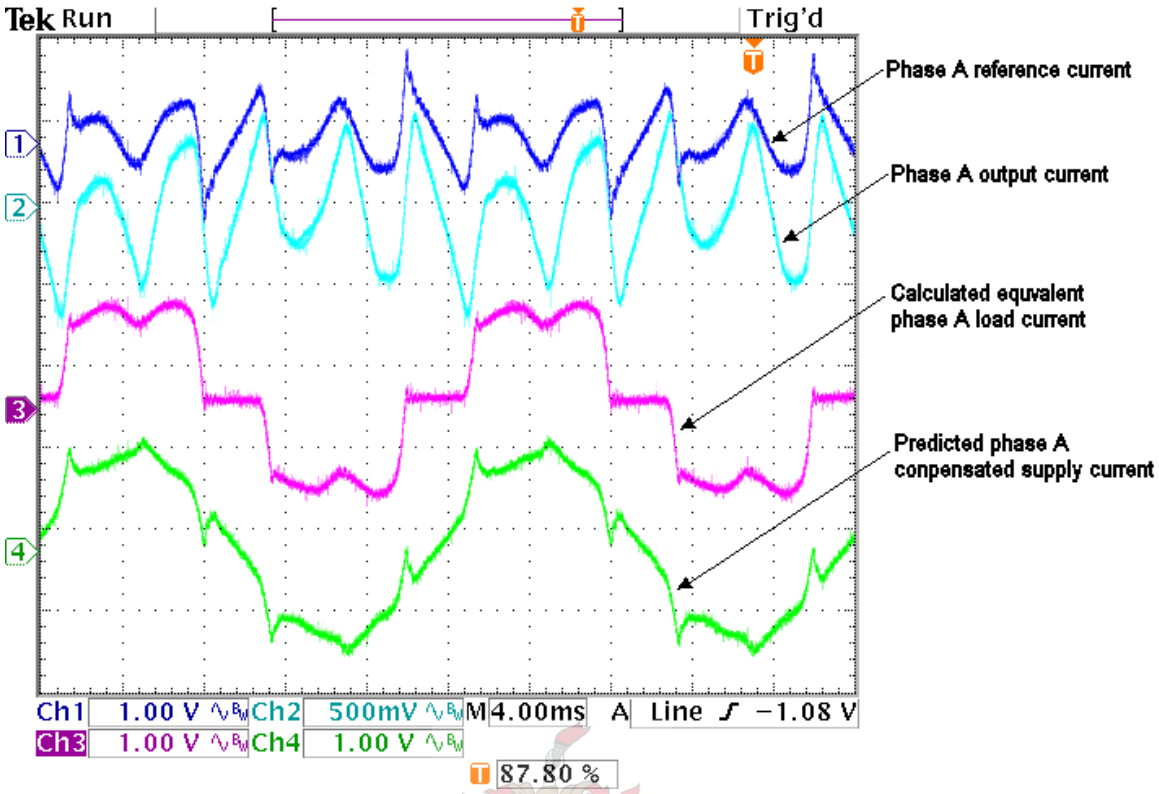


Figure 5.15 The phase A reference and converter output current, the calculated load current and the predicted supply currents after compensation

The predicted result of the active power filtering is visibly more sinusoidal than the load current. The DAC outputs shown on channel 3 and channel 4 were saved in a csv file and analyzed using Matlab. The THD of the load current was calculated to be 31.2%. The predicted compensated supply current's THD was calculated to be 13%.

It is not possible to measure the six-phase supply currents, but the two CTs on the primary side of the main traction transformer makes it possible the measure the current that is drawn from the Eskom network.

Figure 5.16 shows two phases of the uncompensated supply current that is drawn on the 66 kV side of the main traction transformer. Note that the wave form of the supply current is that of a three-phase to six-phase transformer with a delta connected three-phase primary winding. At the time of this test the train was drawing approximately 550 A. The CTs have a conversion ratio of 1:10, which means that a peak current of approximately 20 A was drawn when the screenshot was taken.

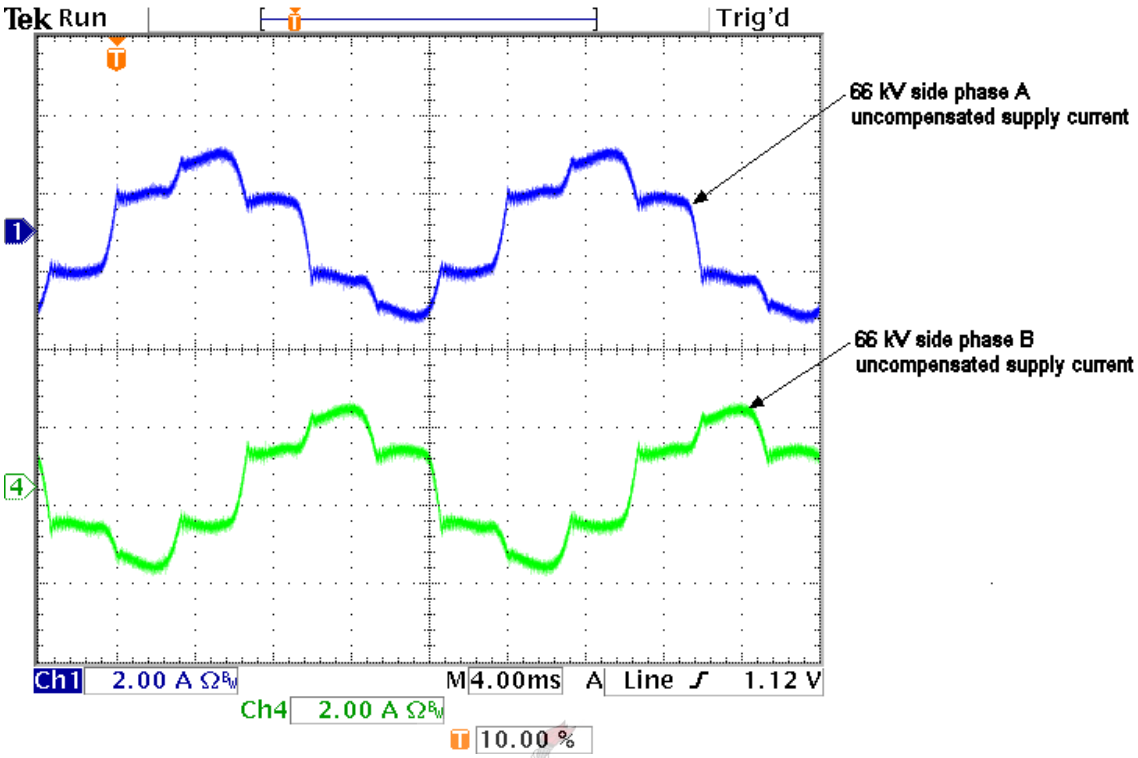


Figure 5.16 The uncompensated supply current measured on the 66 kV side of the main transformer

Although the injection transformer was designed to mirror the main traction transformer having a star connected three-phase primary. The controller converts the six-phase measurements into a three-phase system assuming a star connected primary for the main traction transformer as shown in Figure 5.15. The delta connected primary of the main traction transformer does not cause complications since the injection transformer prescribes how the six to three-phase conversions are to be done.

The compensated supply current measured on the 66 kV side by the CTs are shown in Figure 5.17. The compensated supply current is visibly more sinusoidal than the uncompensated current and is similar to the predicted compensation current shown in Figure 5.15.

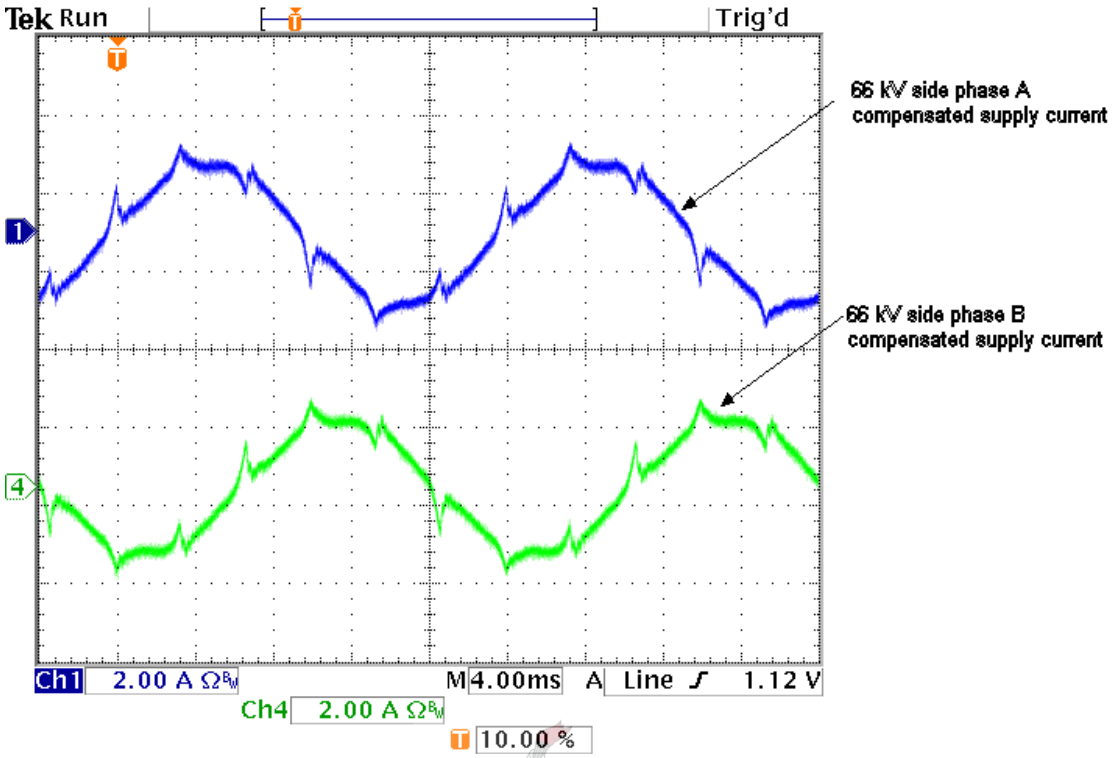


Figure 5.17 The compensated supply current measured on the 66 kV side of the main transformer

Figure 5.18 shows the harmonic components of the uncompensated supply current, measured on the 66 kV side, expressed as a percentage of the fundamental frequency. As expected, the 5th, 7th, 11th and 13th are quite large. The harmonic components of the compensated supply current, measured on the 66 kV side and expressed as a percentage of the fundamental frequency are shown in Figure 5.19. The major harmonics, the 5th, 7th, 11th and 13th are reduced along with several other harmonic components. The 2nd, 3rd and 23rd harmonics components are however are enlarged when the system is working as in AFP mode. THDs for the uncompensated and compensated supply current on the 66 kV side was calculated. The uncompensated supply current had a THD of 24.93% which was reduced to 15.55% for the compensated supply current.

The converter system is only able to perform APF while the train is drawing 1.5 MW (500 A_{DC}) or less. When more power is drawn the filter inductors of the converter begin to overheat. The current limit imposed by the controller to protect the system causes the compensated supply current to distort once the limit is reached.

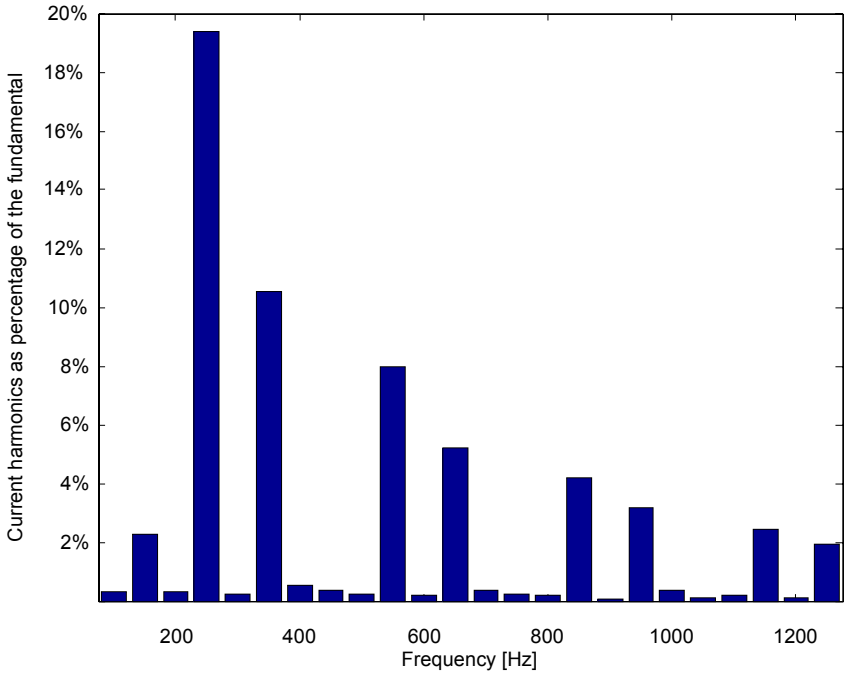


Figure 5.18 The harmonics of the uncompensated supply current

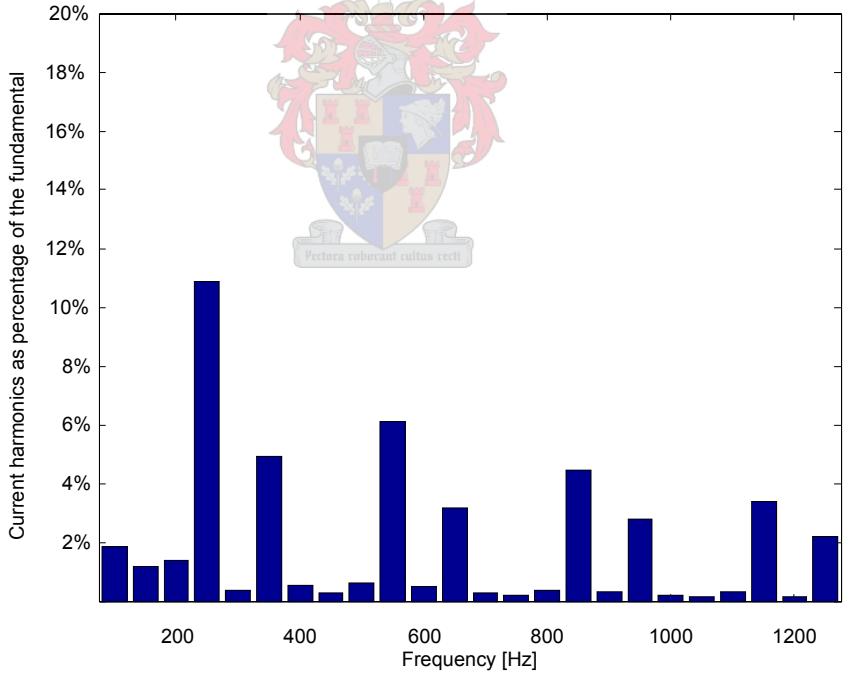


Figure 5.19 The harmonics of the compensated supply currents

The controller uses the natural balancing interleaving switching scheme to calculate the reference currents. This scheme makes it possible to exploit the excellent natural balancing properties of the series-stacked converter topology. The system is

controlled as a whole, by taking the whole system's status into account although each level's duty cycles are calculated individually. This is the same for the DC-bus regulator. The total DC-bus voltage is regulated, leaving the individual inverter levels to balance the voltage between them naturally.

Figure 5.20 shows the voltage profile of the total DC-bus voltages as well as the voltages measured on inverter level 1, level 2 and level 3. The total DC-bus voltage was scaled so that 1 V equals 1 mV on the oscilloscope screen while the individual DC-bus voltage measurements were scaled so that 1 V is equal to 3 mV on the oscilloscope screen.

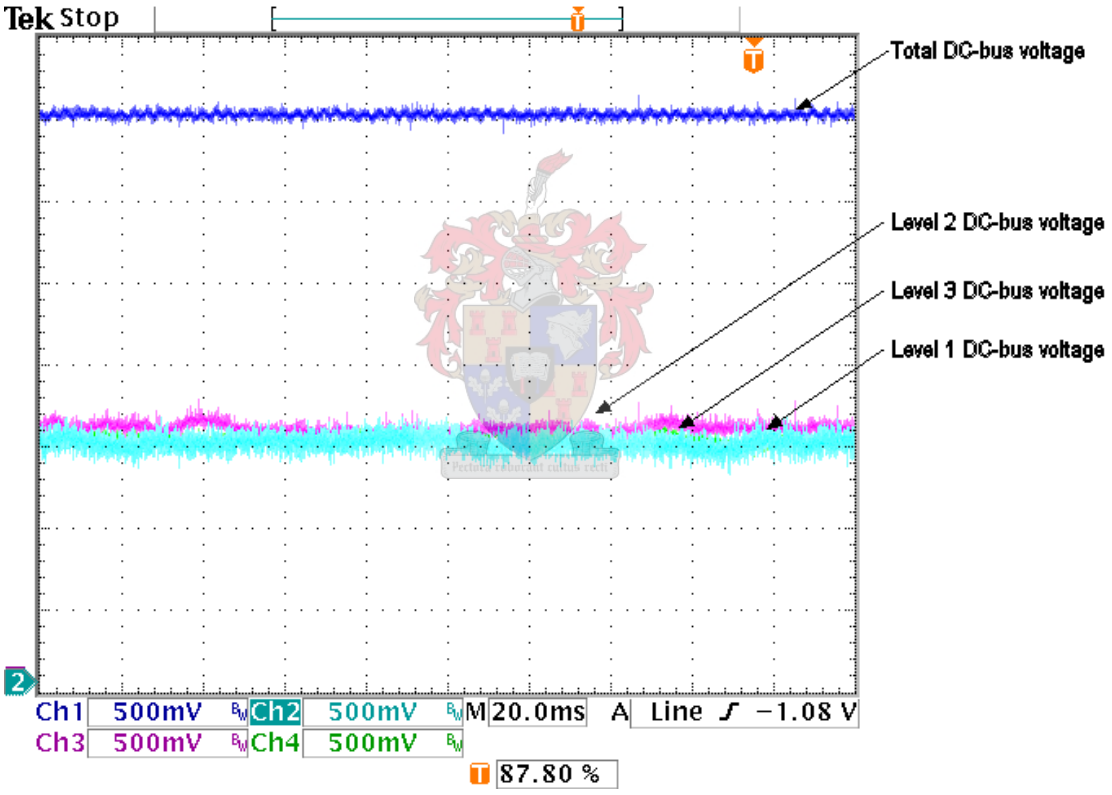


Figure 5.20 The voltage measurements for the total DC-bus, level 1, level 2 and level 3 during APF functioning

Although it is only possible to display four measurements at a time, the other four inverter level's DC-bus voltages were similar to those measured on level 1, level 3 and level 3.

The Lag compensator controls the DC-bus voltage and power regeneration done by the converter system. The Lag compensator calculates a peak amplitude value which is then used to scale three sinusoidal phase references. This gives the AC current references that the converter must generate to regulate the DC bus voltage.

When the system is switched on, the DC-bus is charged from the 3 kV DC-line through the soft-start resistors. Once the DC-bus voltage has reached the 3 kV mark, the DC breaker is closed, soft-starter switched off and the AC breaker is closed. This is done to prevent the systems DC-bus from charging up from the AC side through the free wheeling diodes. Figure 5.21 shows a screen shot of the total DC-bus voltage during the soft-start procedure.

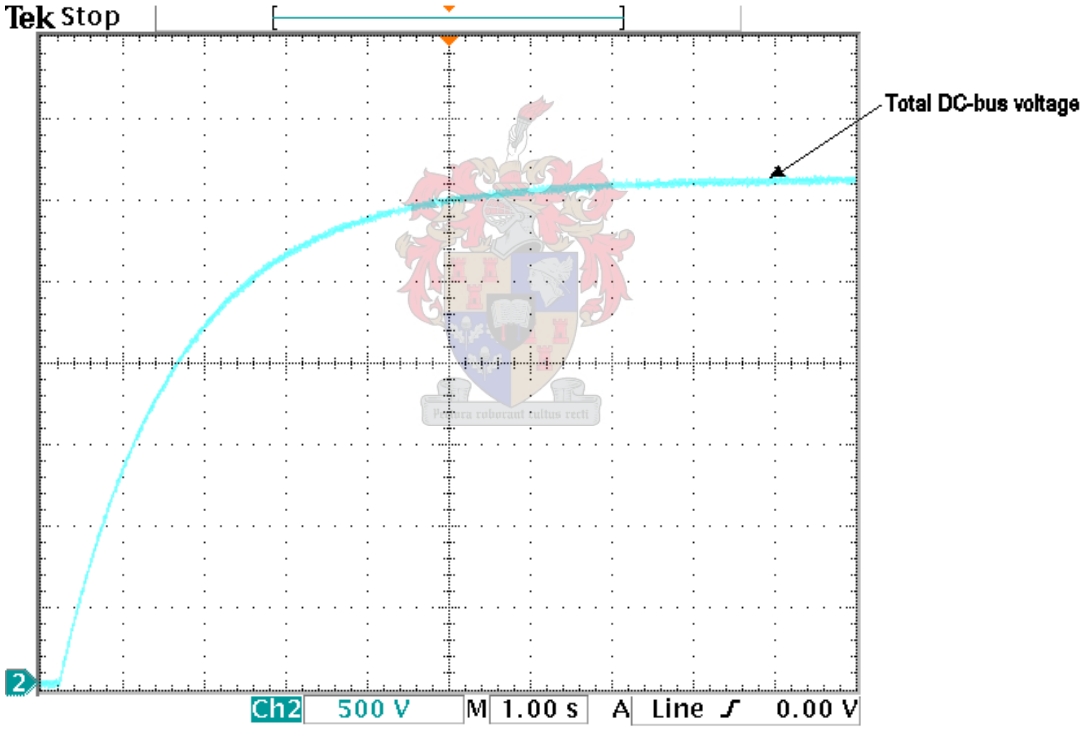


Figure 5.21 The total DC-bus voltage during the soft-start procedure

Only once the DC-bus has been charged to 3 kV and the AC breakers has been closed, does the converter system stat switching. The Lag compensator is then responsible to regulate the DC-bus voltage at the 3.5 kV reference value. This means

that as soon as the converter system starts switching, the DC-bus voltage is charged up from 3 kV to 3.5 kV where it is kept while the system is running.

Figure 5.22 shows the DC-bus regulator's reference current for phase A, the phase A output current of the converter and the phase A supply voltage. The amplitudes of the reference and output currents are very high when the system is switched on causing the DAC's outputs flip over. As the DC-bus voltage approaches the reference value the reference current, stabilizes.

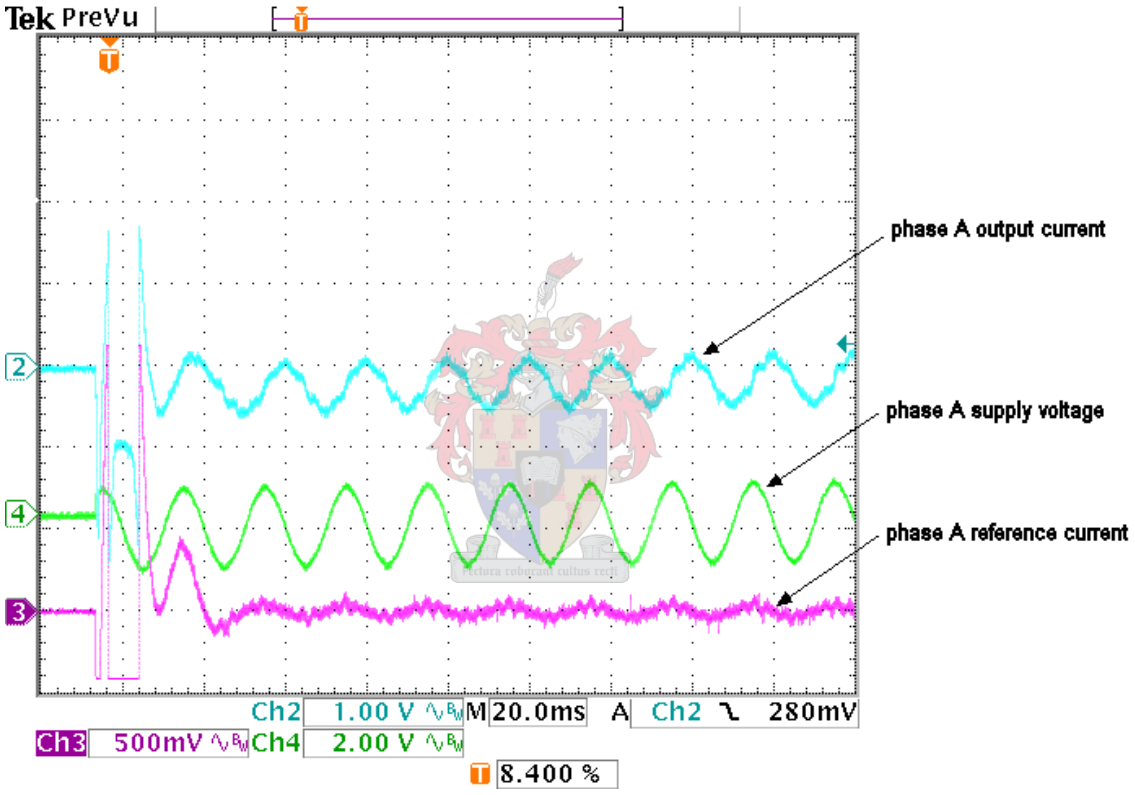


Figure 5.22 Phase A output current, phase A supply voltage and phase A reference current during DC-bus regulation test

Figure 5.23 shows the total DC-bus voltage. The tests starts with the DC-bus voltage charged to 3 kV through the soft-starter. As soon as the DC-bus regulator is switched on the DC-bus voltage dips down before the voltage starts to rise and settles at the reference value. Even though the reference current is limited the DC-bus voltage reaches the reference value of 3.5 kV in approximately 40 ms. Other than slowing the

response time of the system the limited reference current is also responsible for the voltage dip just after the regulator is stated.

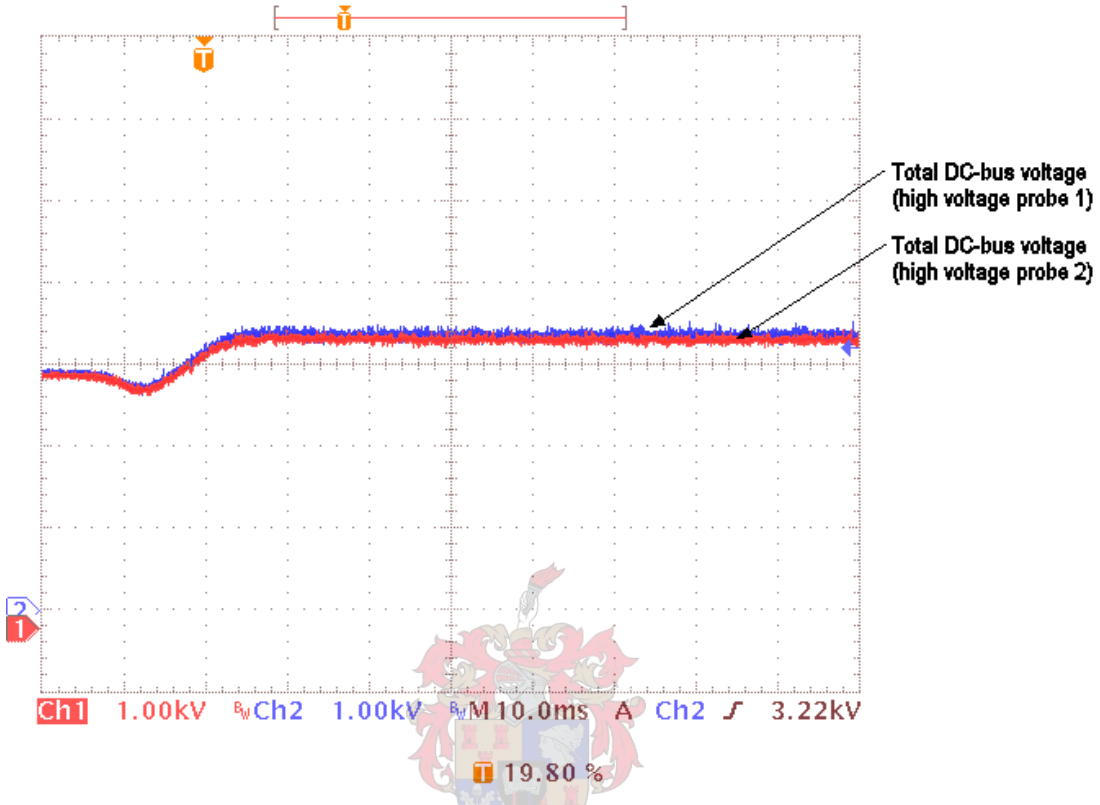


Figure 5.23 The Total DC-bus voltage response to the DC-bus regulator

Although the reference currents that are calculated by the DC-bus regulator is limited to 600 A, the initial reference value and the subsequent converter output current are on the limit. It was thus decided to ramp the reference current from 0 A up to the full reference value over a period of one second. This would cause less stress on the inverters since the IGBTs would not have to switch the maximum allowed current as soon as the system is switched on.

Figure 5.24 shows the DC-bus regulator's peak amplitude reference value, the phase A reference current, the phase A output current of the converter and the phase A supply voltage, using the ramped reference signal. On channel 1 the peak amplitude value calculated by the DC-bus regulator is shown (0 A corresponds to 2.048 V on the DAC's output). During the first 80 ms the peak value is at its 600 A limit. The switching reference current for phase A is shown on channel 3. Although the DC-bus

regulators reference is stuck at 600 A, the effect of ramping the switching reference allows a more controlled charging of the DC-bus. Channel 2 shows the phase A converter output current.

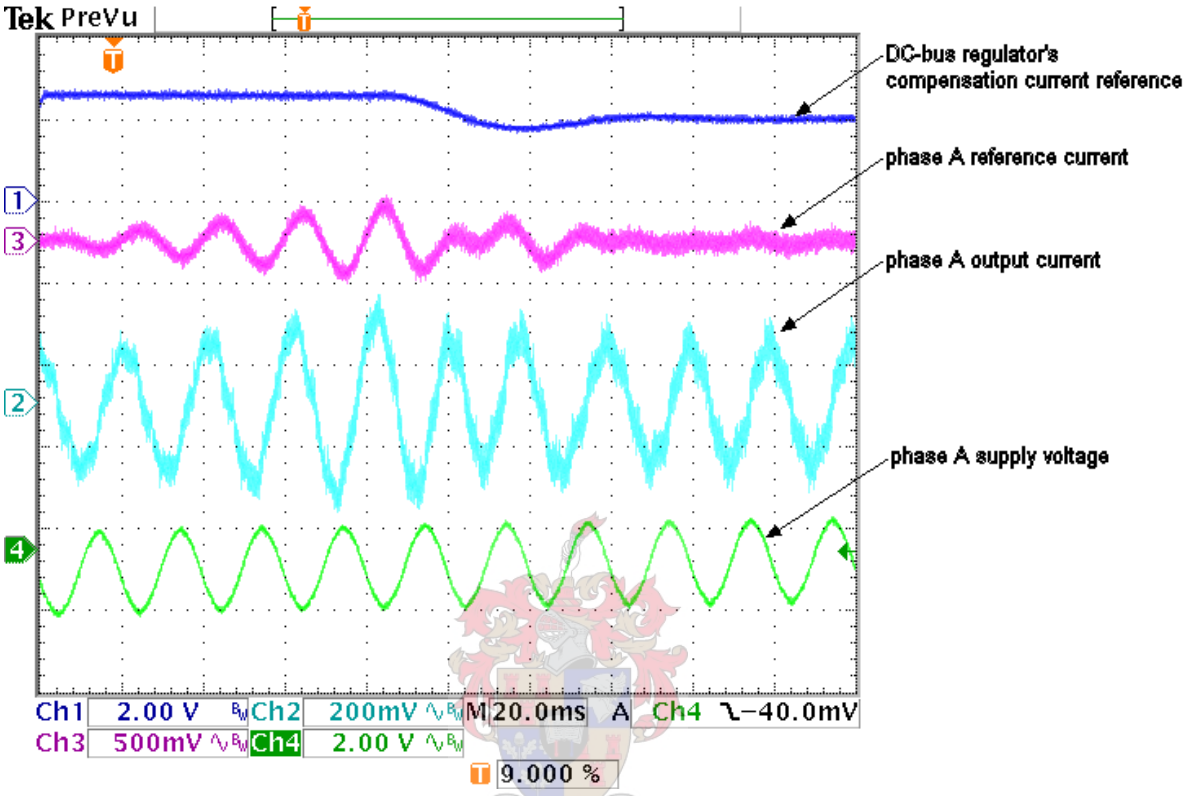


Figure 5.24 The DC-bus compensator's reference current, phase A reference and output current and the phase A supply voltage during DC-bus regulator start up with reference limiting

At approximately 100 ms the DC-bus regulators output reference reaches zero. This corresponds to the time when the DC-bus voltage reaches the 3.5 kV reference value for the first time. The DC-bus voltage overshoots slightly, causing the DC-bus regulator's reference to become negative. After 140 ms the DC-bus reaches its steady state value of 3.5 kV. Although the DC-bus regulators reference is almost zero after 140 ms the converters output current does not reach zero. This is due to the time delay present in the voltage measurements.

The total DC-bus voltage measurement for the ramped switching scheme is shown in Figure 5.25. The DC-bus regulator is switched on at t = 40 ms, the DC bus charges

up and reaches the 3.5 kV mark approximately 96 ms later. The DC-bus voltage overshoots the reference value and reaches steady state 140 ms after the DC-bus regulator had started.

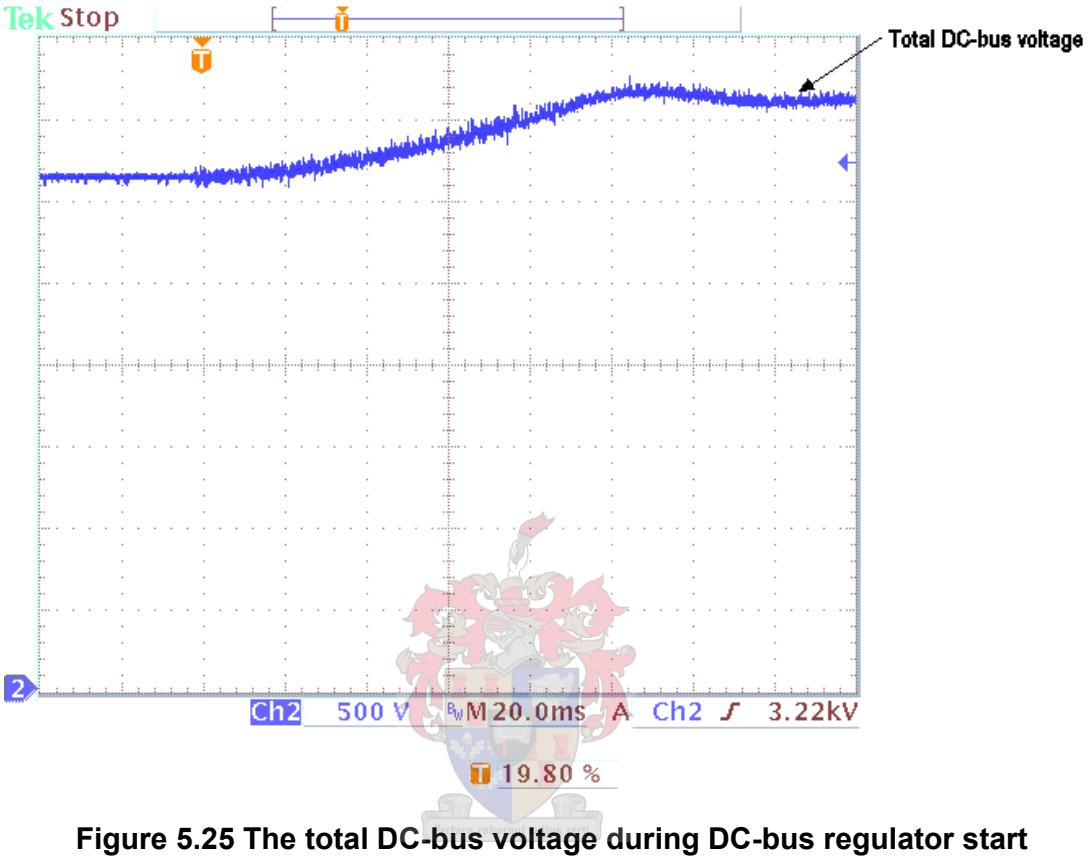


Figure 5.25 The total DC-bus voltage during DC-bus regulator start up with reference limiting

By ramping the switching current reference, the DC-bus regulator's start up response is impaired. As soon as the switching references have been ramped to its full value, only the 600 A current limit will interfere with the DC-bus regulator.

During normal operation the system regulates its DC-bus at a level of 3.5 kV while the 3 kV DC line varies between 3 kV and 3.3 kV. The DC-bus voltage can rise up to 3.9 kV when a passing train uses regenerative braking to slow down. The train driver slows the train by increasing the current that is regenerated. If the regenerated energy is not extracted from the over head DC-line the DC voltage of the line starts to climb. The train driver is able to monitor the DC-line voltage and decreases the amount of regenerated current if the voltage approaches 3.9 kV.

The converter starts injecting energy into the utility network as soon as the DC-line voltage passes the 3.5 kV point. Since there is not a regular running schedule for the freight trains and it is not possible to communicate with the train driver, there was no way to control the test conditions. To protect the system the DC-bus regulator's current limit for the first test was set to 600 A. The system was started up and left to run while the DC-bus voltage and DC current into the converter system is logged continually.

Figure 5.26 shows the measured total DC-bus voltage and the DC current into the converter system during the first regeneration period

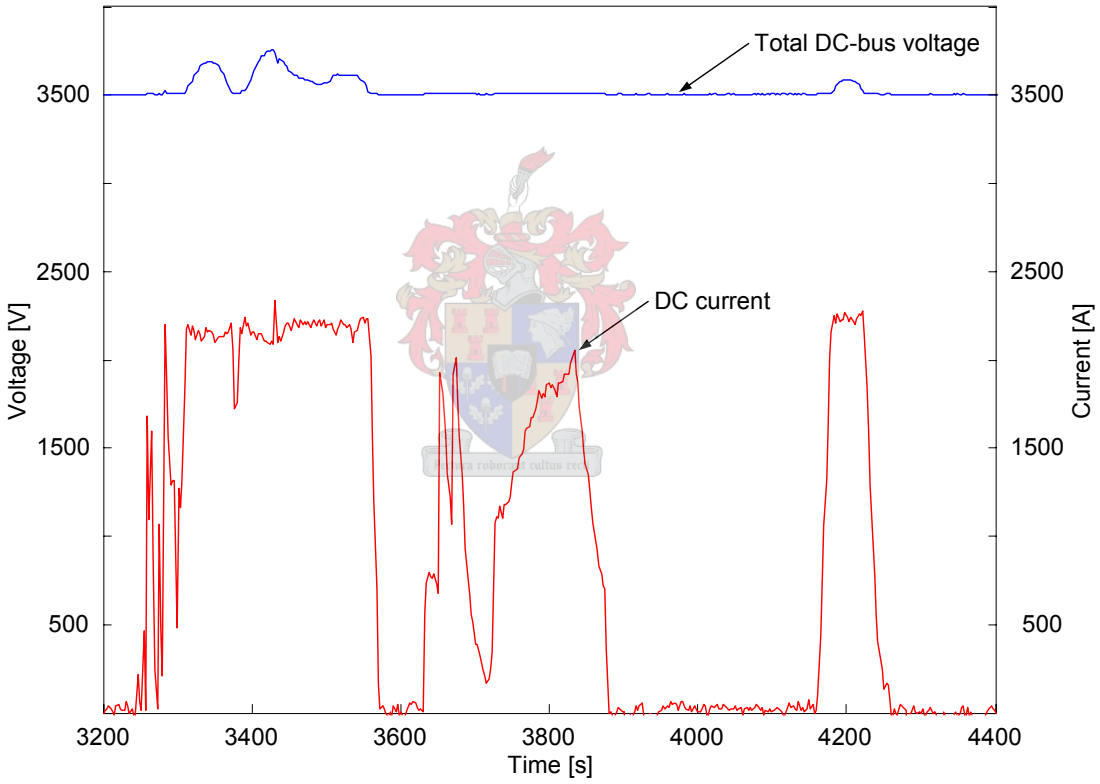


Figure 5.26 The Total DC-bus voltage and DC current measurments during the first regeneration period

The DC-bus voltage is held at 3.5 kV until the current limit is reached. When the system starts limiting the current, the DC bus voltage starts to climb. The train driver responds to the rising voltage by lowering the regenerated current which in turn causes the DC-line voltage to decrease. During the first test, regeneration started at

3 250 s. The current rises and at 3 310 s the current reaches the current limit. At this point the voltage starts to climb. The driver responds by lowering the regenerated current and keeps the regenerated power relatively constant until regeneration is stopped at 3570 s. The first regeneration period lasted for 260 s. At 3 630 s the next regeneration period started and lasted 250 s, the current profile is however more jaggerd. The third regeneration period started at 4 160 s and lasted a 100 s.

The power regenerated during the first test is shown in Figure 5.27. With the current limit at 600 A for the first test the regenerated power is limited to 800 kW.

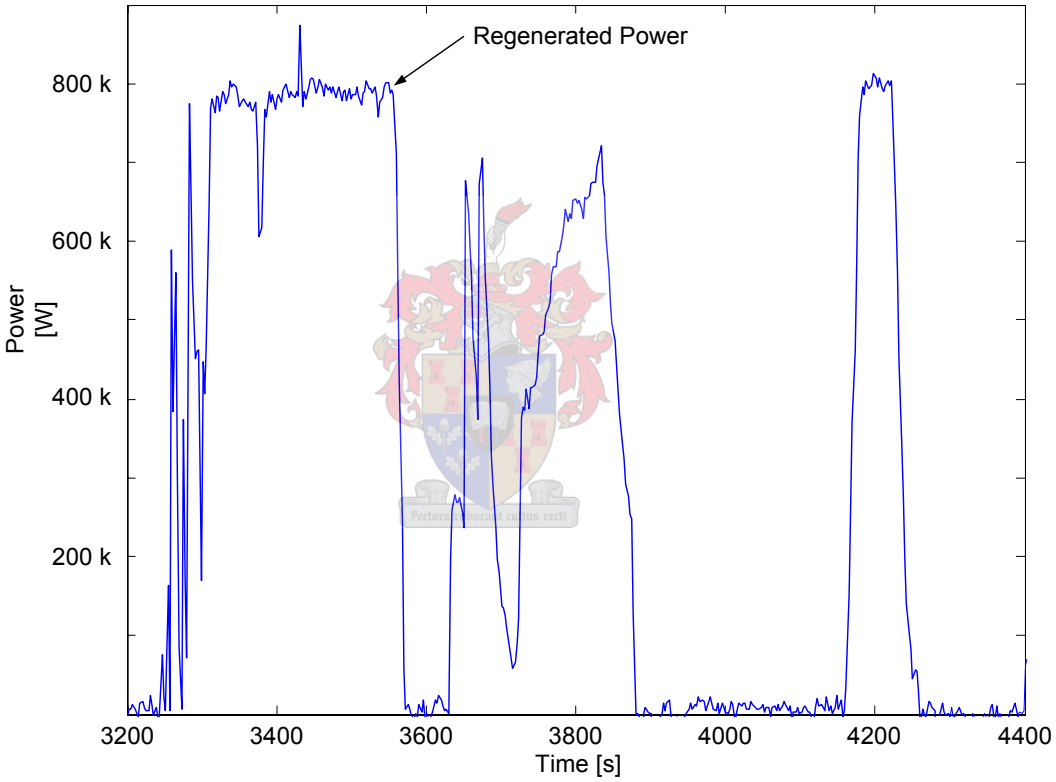


Figure 5.27 A graph of the power regenerated during the first regeneration period

The first regeneration period resulted in a relatively constant near 800 kW for 260 s. The second regeneration period has a more jaggerd regenerated power profile but lasts for 240 s. The third period again reaches the limit and is constant at 800 kW for a 100 s.

During the second regeneration tests the current limit for the DC-bus regulator was raised to 900 A, the combined reference current limit was raised to 800 A per phase. The total DC bus voltage and DC current logged during the second regeneration test is shown in Figure 5.28.

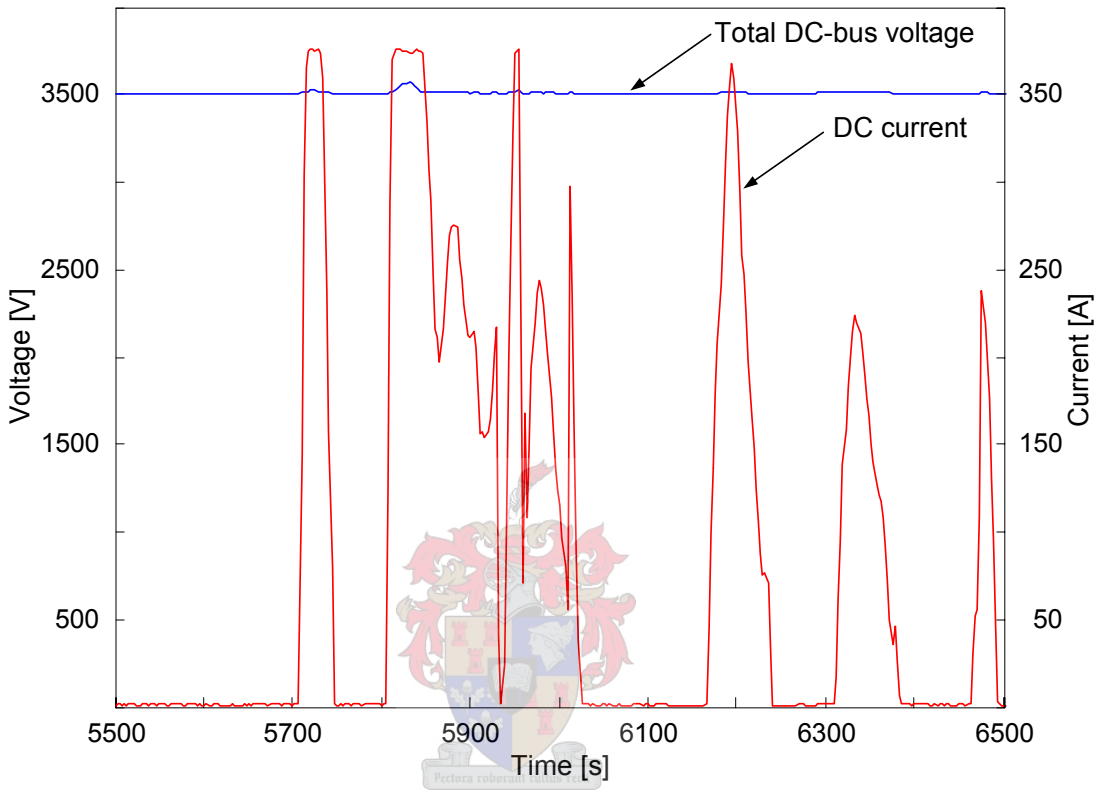


Figure 5.28 The Total DC-bus voltage and DC current measurments during the second regeneration period

The second test had a less uniform regeneration profile than the first test. During the second tests five regeneration periods can be identified and it is easy to see that the system reaches the current limit on three occasions. The first regeneration period started at 5 707 s and lasted 43 s. The second period stated at 5 806 s and lasted 225 s. The system reaches the current limit twice in the second regeneration period although the current also fluctuates considerably. The third, fourth and fifth regeneration periods lasted 75 s, 75 s and 34 s respectively.

The regenerated power during the second regeneration test period is shown in Figure 5.29. With the increased current limit the regenerated power is limited to 1.3 MW. The regeneration limit was reached three times during the second test.

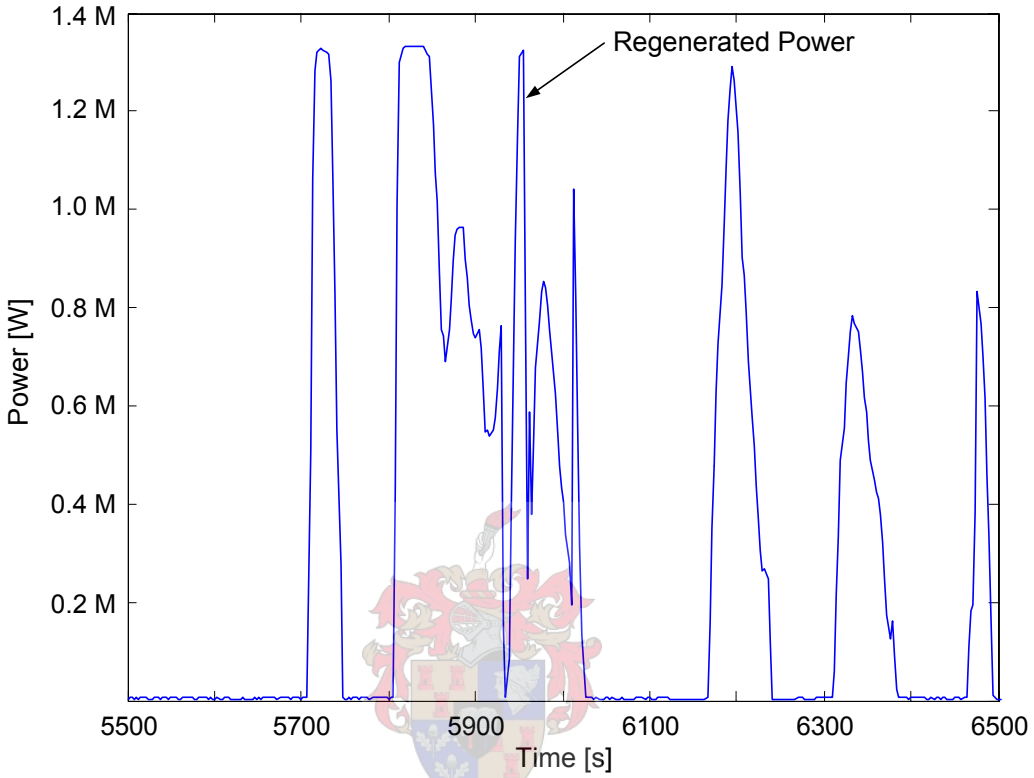


Figure 5.29 A graph of the power regenerated during the second regeneration period

The second regeneration period lasted 225 s and although the regenerated power reached its limit twice the average power regenerated overt the period is 760 kW. As can be seen from Figure 5.29 and Figure 5.27 the regenerated current and thus power fluctuates considerably and is dependant on the train's load as well as on the driver.

The test results confirm that the seven level series-staked converter is successfully controlled by the PEC33 controller board. The algorithms controlling the regeneration and APF functioning of the converter work correctly while exploiting the natural balancing properties of the series stacked converter. While the interleaving the switching signals produces reduced output harmonics in the injected current.

6. Conclusion and Recommendations

A full scale 1.5 MW series-stacked converter was built and installed in a Spoornet DC traction substation. The converter was developed to perform two functions; to act as an active power filter and to operate as a regeneration converter. Both of these functions were successfully implemented and tested.

The system regenerates when a passing train slows using its electric motor, which generates electrical energy. The regenerated energy causes the voltage on the 3 kV DC-line to rise. When the voltage on the DC-line reaches 3.5 kV the system starts injecting the regenerated energy into the Eskom grid. The system performs its APF functioning when a passing train draws power via the DC substation from the supply network. The current drawn from the AC supply through the diode rectifier has a high harmonic content. The system injects harmonic current components complementary to those the rectifier draws. The harmonic current drawn from the supply network is thus reduced.

The peak power regenerated during tests was logged as 1.3 MW. The maximum power regenerated was limited to this level by the limit imposed on the reference currents. A power limit of 1.5 MW will be reached if the current limit is raised from 800 A to 900 A. Due to a limited time schedule the tests with the higher current limit has not yet been performed.

During the APF tests the total harmonic distortion, measured on the 66 kV supply side of the main traction transformer was reduced from 24.93 to 15.55%. The system is however only capable of performing the active power filtering while the train does not draw more than 1.5 MW from the supply network. With the current control strategy and converter setup the filter inductors start to overheat when the power drawn by the train reaches 1.5 MW.

6.1 The converter system

A seven level series-stacked converter was designed, built and installed as a shunt compensator system in a Spoornet DC traction substation. The converter is constructed by connecting the DC-busses of seven three-phase inverters in series with each other. The converter has a total DC bus rating of 5.6 kV, normally operating with a DC voltage of 3.5 kV. Being a seven level series-stacked converter, the seven three-phase outputs were combined in a specially made injection transformer. The secondary of the transformer consisted of a triple star six-phase winding which was connected to the six-phase supply lines connected to the diode rectifier.

A multilevel converter topology reduces the level of output harmonics produced by the converter. The series-stacked topology does not require extra components like clamping diodes or capacitors. While the natural balancing properties of the DC-bus makes it possible to use a number of levels without complicating the control strategy. Although the topology does require a specialised injection transformer, the transformer properties like the leakage inductance and inherent isolation is exploited. The series-stacked multilevel converter lends itself to interleaving the switching signals, which further reduces the output current ripple and increases the equivalent switching frequency of the converter system.

The converter system for the Spoornet project was built up using seven three-phase full bridge inverters. The system has 42 IGBTs, each switched individually. A total of 28 current and 14 voltage measurements are taken to control the system. The system connects to the six-phase AC supply though six fuses and two three-phase contactors. The DC-bus connects to the 3 kV DC-line through two DC contactors in parallel, the one used as the soft-starter has a resistor network in series with it.

6.2 The controller and measuring system

The system is controlled by a PEC 33 controller board. A few modifications had to be made to the controller board and firmware, to increase its speed and capacity. A PWM expansion board was developed to provide enough PWM outputs and feedback ports. The control and feedback signals are transmitted through optical fibres to provide electrical isolation between the controller and converter system.

The voltage measurements are digitized and encoded by voltage measuring boards. To provide isolation between the measuring boards and the controller, the encoded voltage measurements are sent through optical fibres. Since a higher bandwidth is required for the current measurements, they are kept in analog form and digitized on the PEC 33 controller board. The current probes provide the required isolation between the controller and converter system. The current probes output's current signals, which are converted to voltage signals by current measurement boards. These voltage signals are then sampled by the ADCs on the PEC 33 controller.

The DSP on the PEC 33 controller calculates and outputs a set of three-phase duty cycles every 28.57 µs. This involves reading in all the voltage and current measurements, determining the current references for the DC-bus controller and active power filtering and then constructing the three-phase duty cycles through space vector PWM. The duty cycles are transmitted to the PWM expansion board. The PWM expansion board then generates the interleaved switching signals. While in regeneration mode, the DSP logs the duration, average power, and peak power of the regeneration period.

To protect the system the DSP checks for over voltage and over current on the converter system. The DSP also checks whether the contactors are in the correct states as well as implementing a watchdog timer. The PWM expansion board also implements a watchdog timer as well as monitoring the converter's feedback signals.

6.3 The control strategy

A Lag compensator was used to regulate the DC-bus voltage of the converter. The primary function of the system, to work as a regeneration converter is also controled by the Lag compensator. The DC-bus voltage is regulated at 3.5 kV and as soon as the DC-bus rises above the reference voltage the converter starts injecting the excess energy into the utility network.

The secondary role of the converter is to work as an active power filter. The compensation current reference is calculated using the Instantaneous reactive power theory, introduced by H. Akagi. The APF current reference, calculated from the Instantaneous reactive power theory, attempts to compensate for all harmonic current components.

The system is controlled using the natural balancing interleaved switching scheme. This involves using the status of the system as a whole to calculate the switching duty cycles, although the references are only used to switch a single converter level. In other words, all the output currents are measured and combined, then together with the average DC-bus voltage over a converter level is used to calculate the switching duty cycles.

During the preliminary tests, power levels of up to 1.3 MW have been reached during regeneration. The 1.5 MW mark will be reached once the current limit of the combined reference currents is increased to 900 A. During the APF tests the converter system reduced the measured THD of the supply current from 24.93% to 15.55%. The system is however only capable of working as an APF while the train draws less than 1.5 MW from the supply. This is mainly due to the filter inductors that overheat. The excessive heating of the filter inductors are due to core losses, as result of the high frequency current components.

6.4 Recommendations and future work

Since this system is the first full scale prototype developed and installed, there are many elements that require further attention. These elements fall into two groups; the controller hardware and control strategy.

As a regeneration converter, the control strategy does not need obvious changes. One aspect worthwhile evaluating is controlling the system using the atypical interleaved switching scheme as apposed to the natural balancing switching scheme. The atypic switching scheme involves only measuring the output currents and the DC-bus voltage of a single inverter level, to calculate the switching duty cycles for the level in question.

Although the APF functioning is only of secondary concern for Spoornet, using synchronous reference frame to calculate the APF reference currents could be considered. Using the synchronous reference frame it is possible to target discrete current harmonics. Thus it is possible to compensate only for the fifth harmonic, seventh harmonic, eleventh harmonic and so on. In this manner it might be possible to reduce the heating of the filter inductors and it may thus be possible to perform compensation even though the train is drawing more that 1.5 MW (the performance of the converter will still be subject to limits on the current references).

Although not essential, changes that should be considered on the hardware side are; a redesign or follow up to the PEC 33 controller will improve reliability and add more flexibility. To improve reliability a larger FPGA and configuration device would eliminate the need for modifications to the controller board. Single channel ADCs would decrease time lost during sampling and improve the systems overall response time. A redesign of the PWM expansion board and a more efficient external data bus communication protocol would also reduce time lost during data transmission.

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A. PWM Expansion Board

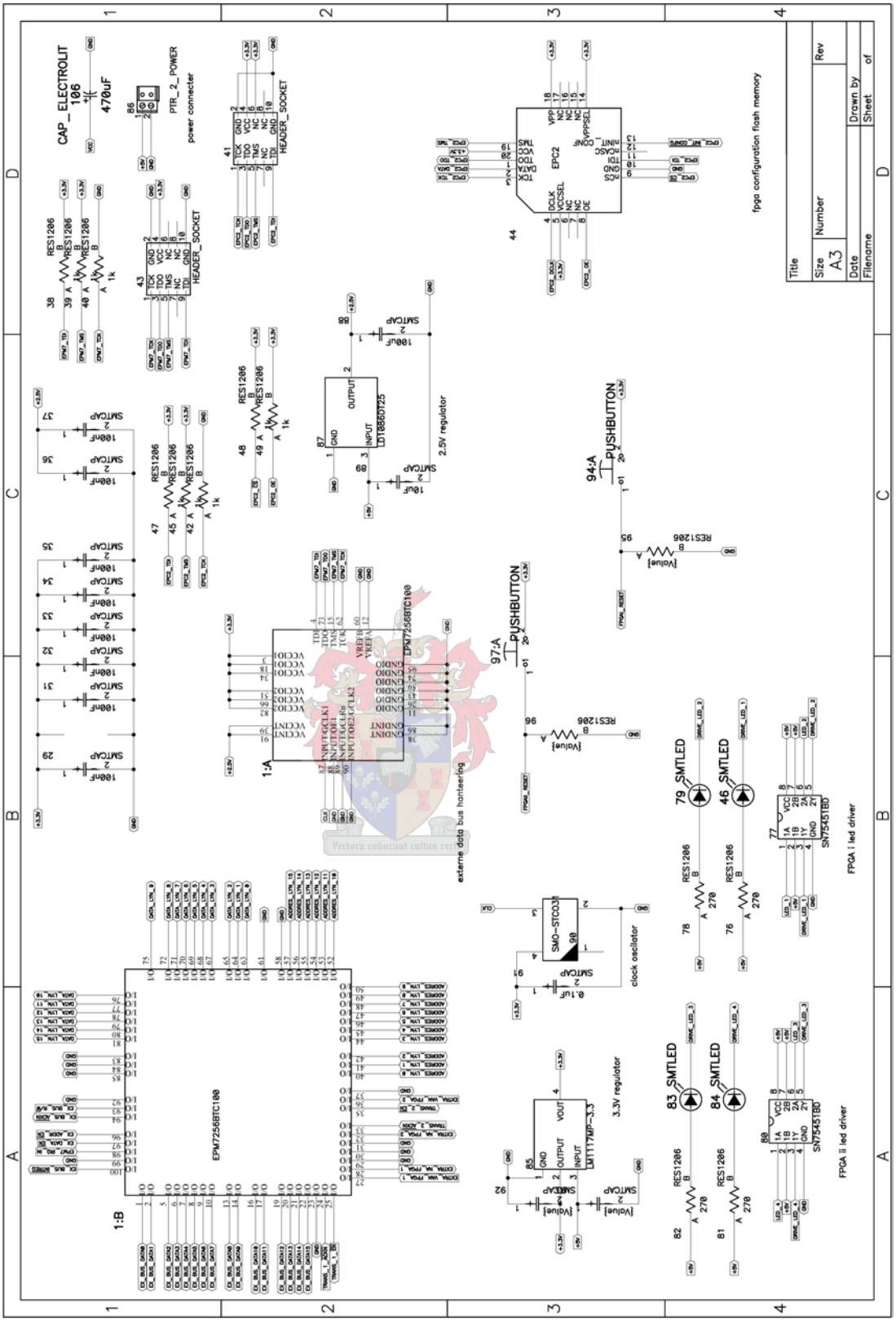

Figure A-1 Schematic of EPLD and small components

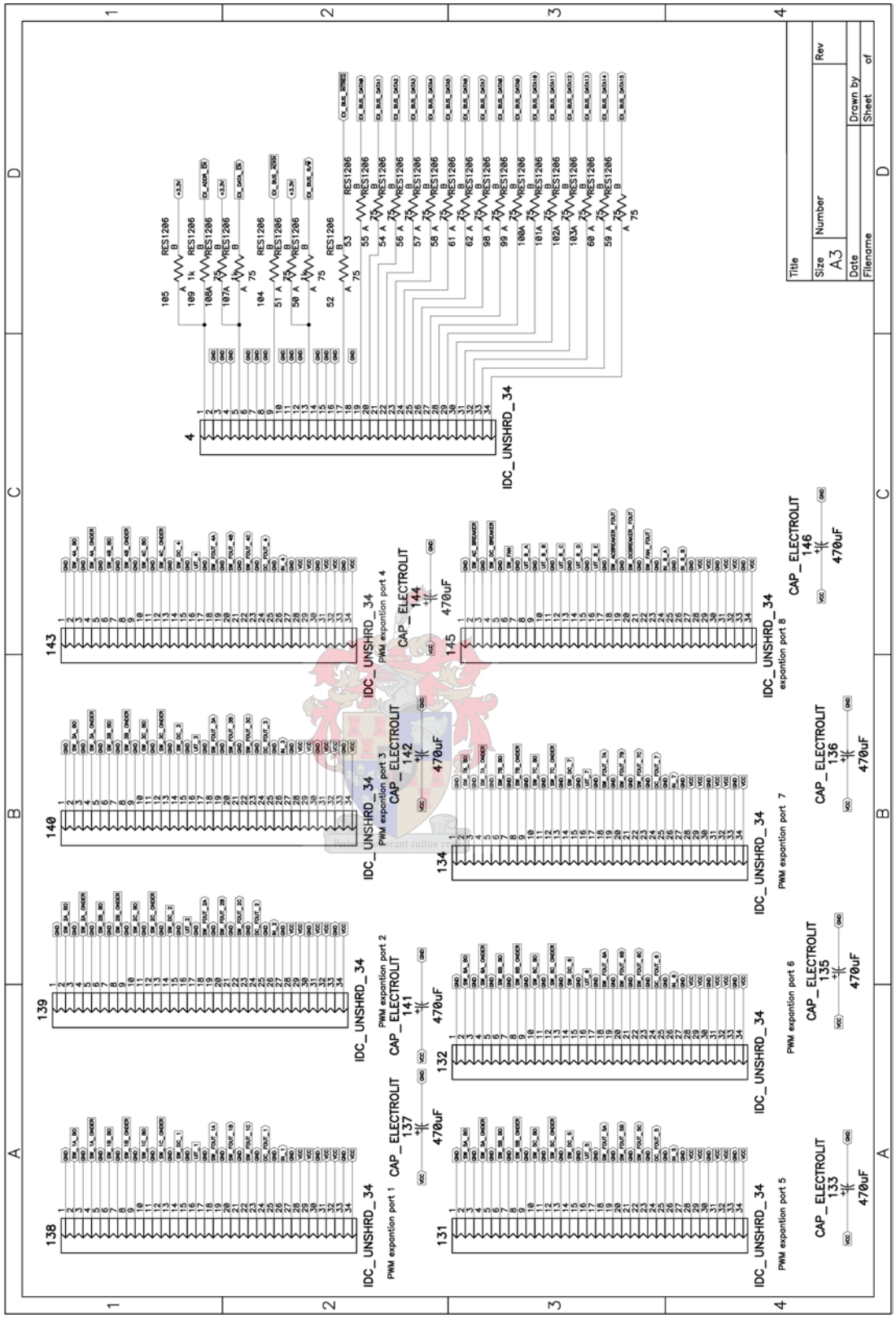

Figure A-2 Schematic of ports

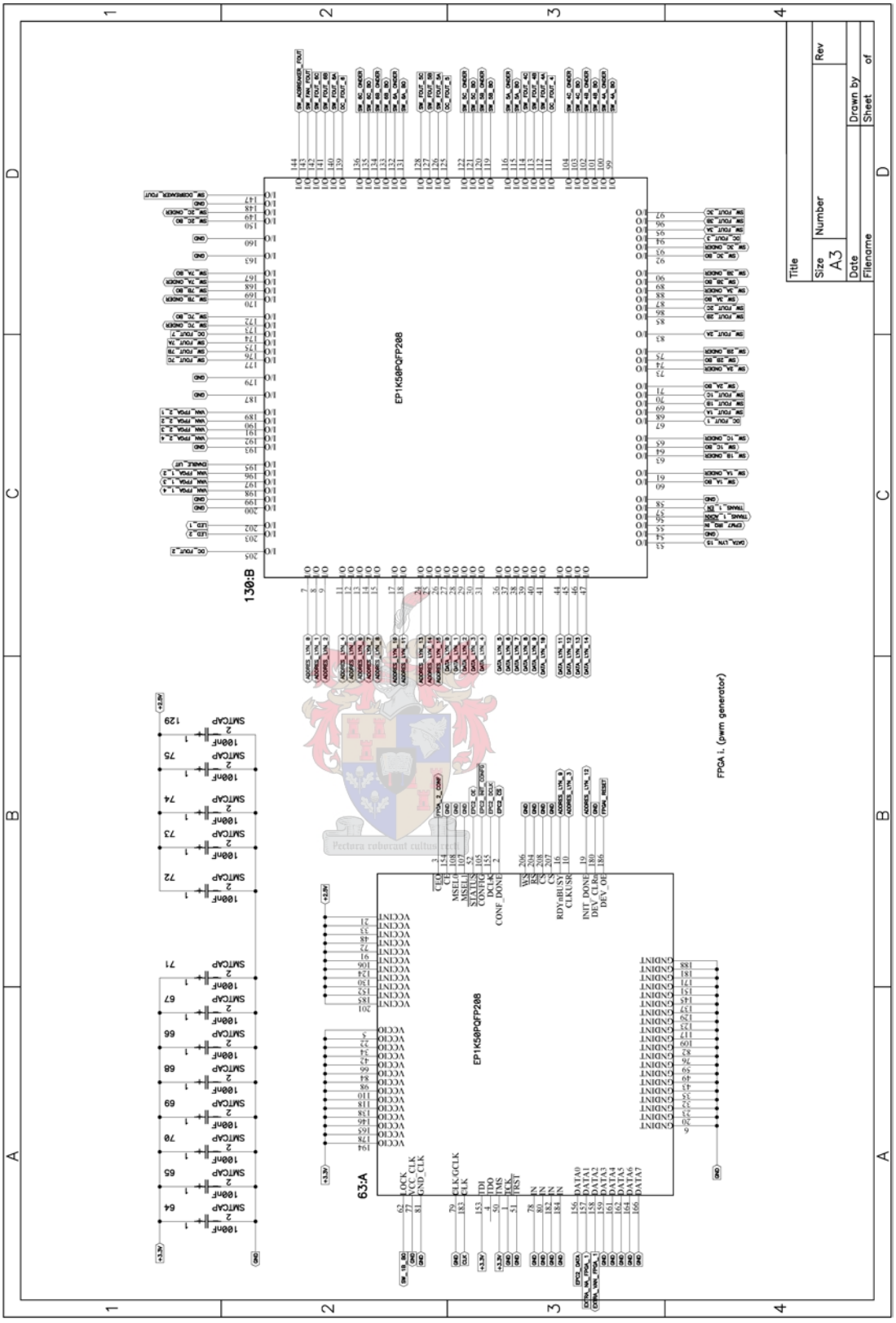

Figure A-3 Schematic of PWM FPGA

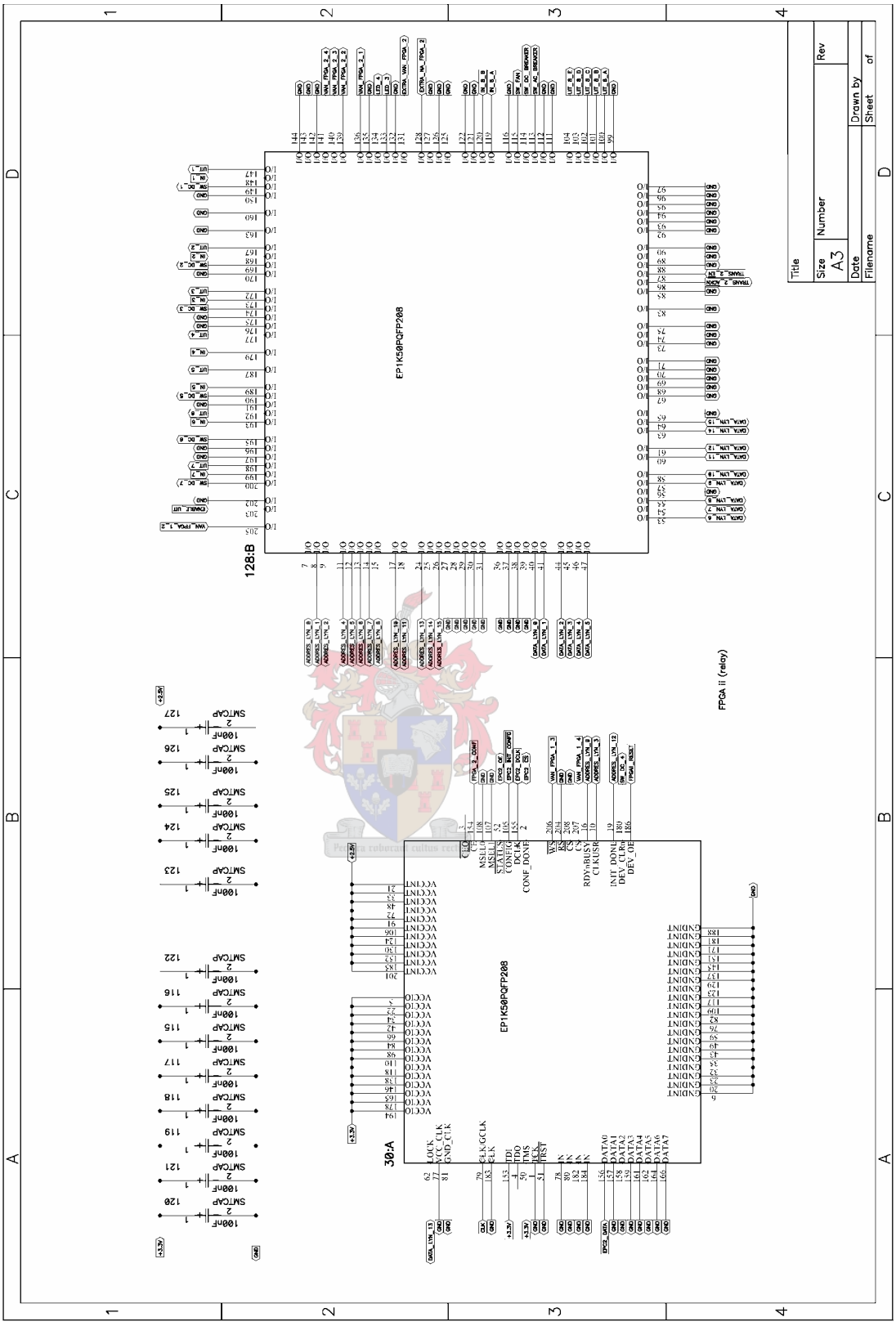

Figure A-4 A4 Schematic of relay FPGA

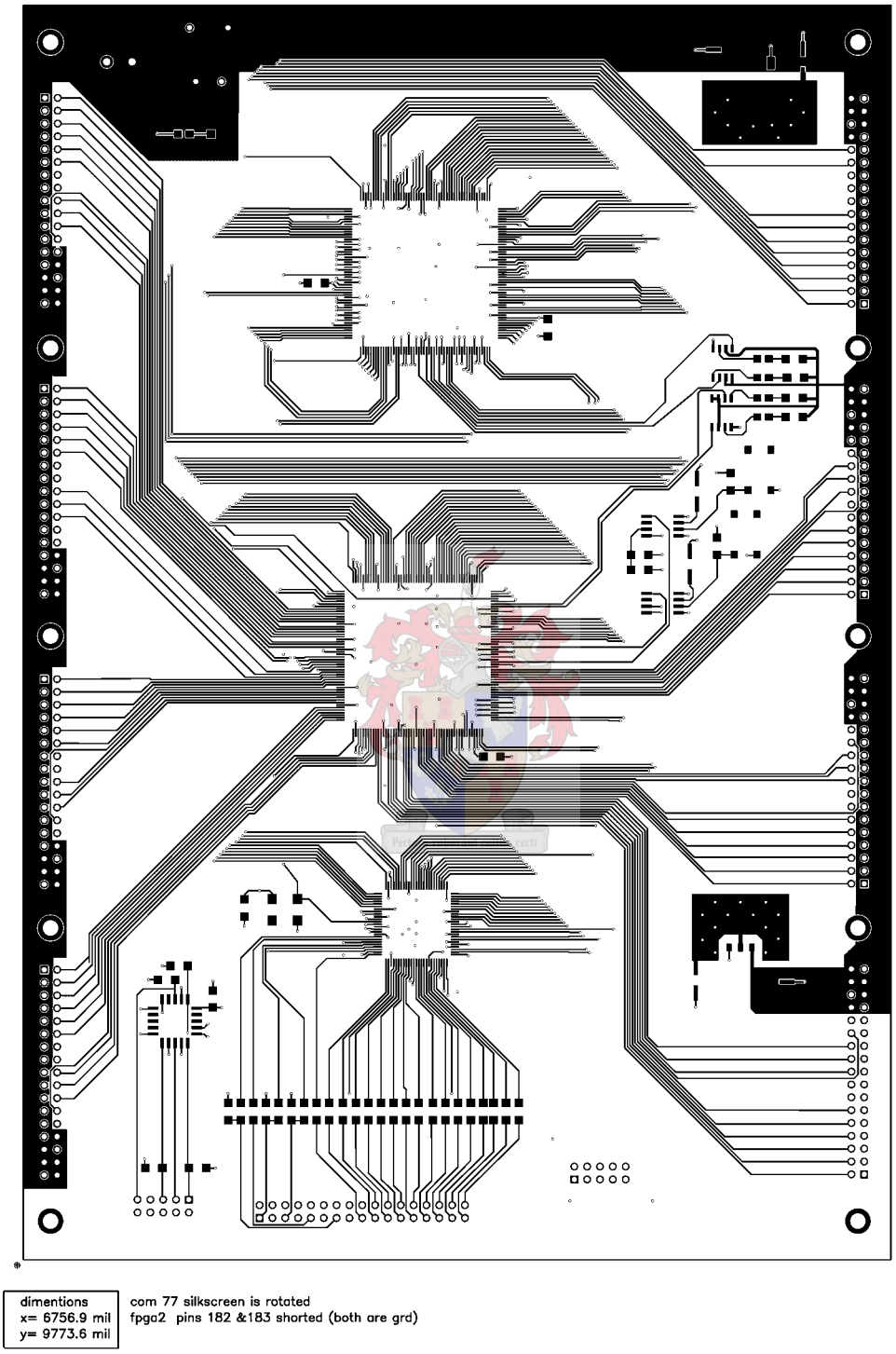

Figure A-5 PCB layout of PWM Expansion Board TOP layer

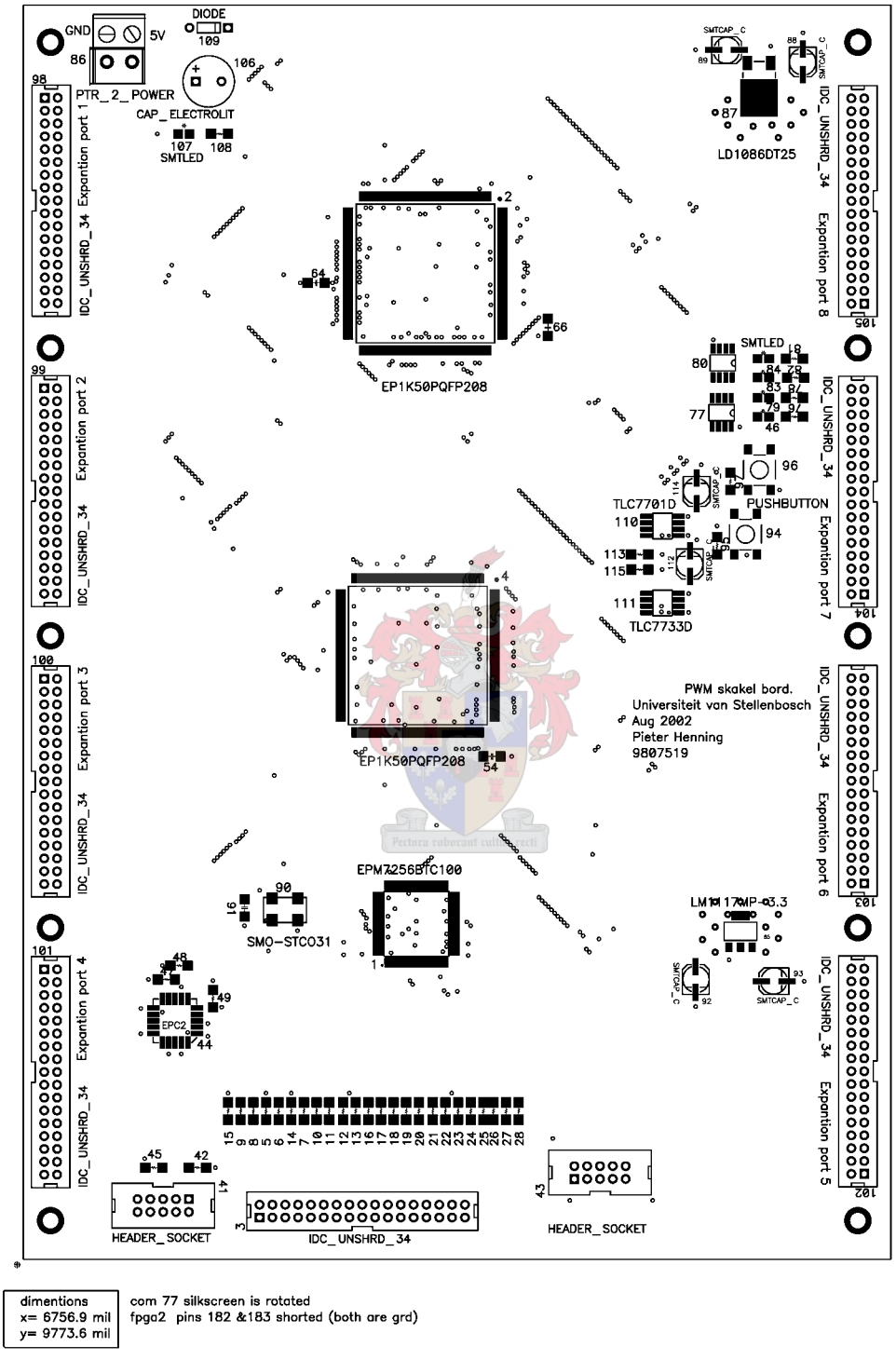

Figure A-6 PCB layout of PWM Expansion Board TOP silkscreen and pads

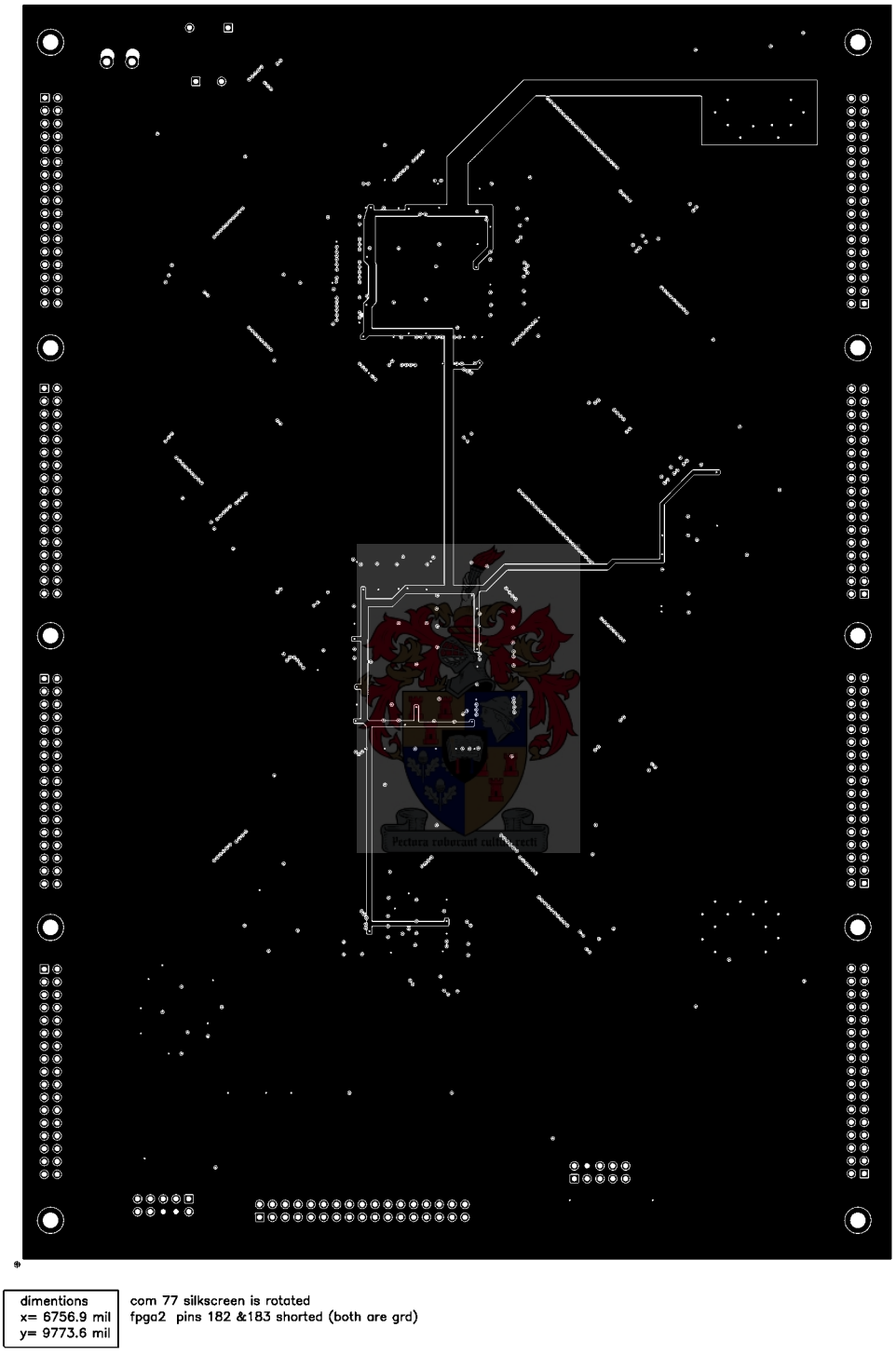

Figure A-7 PCB layout of PWM Expansion Board Power layer

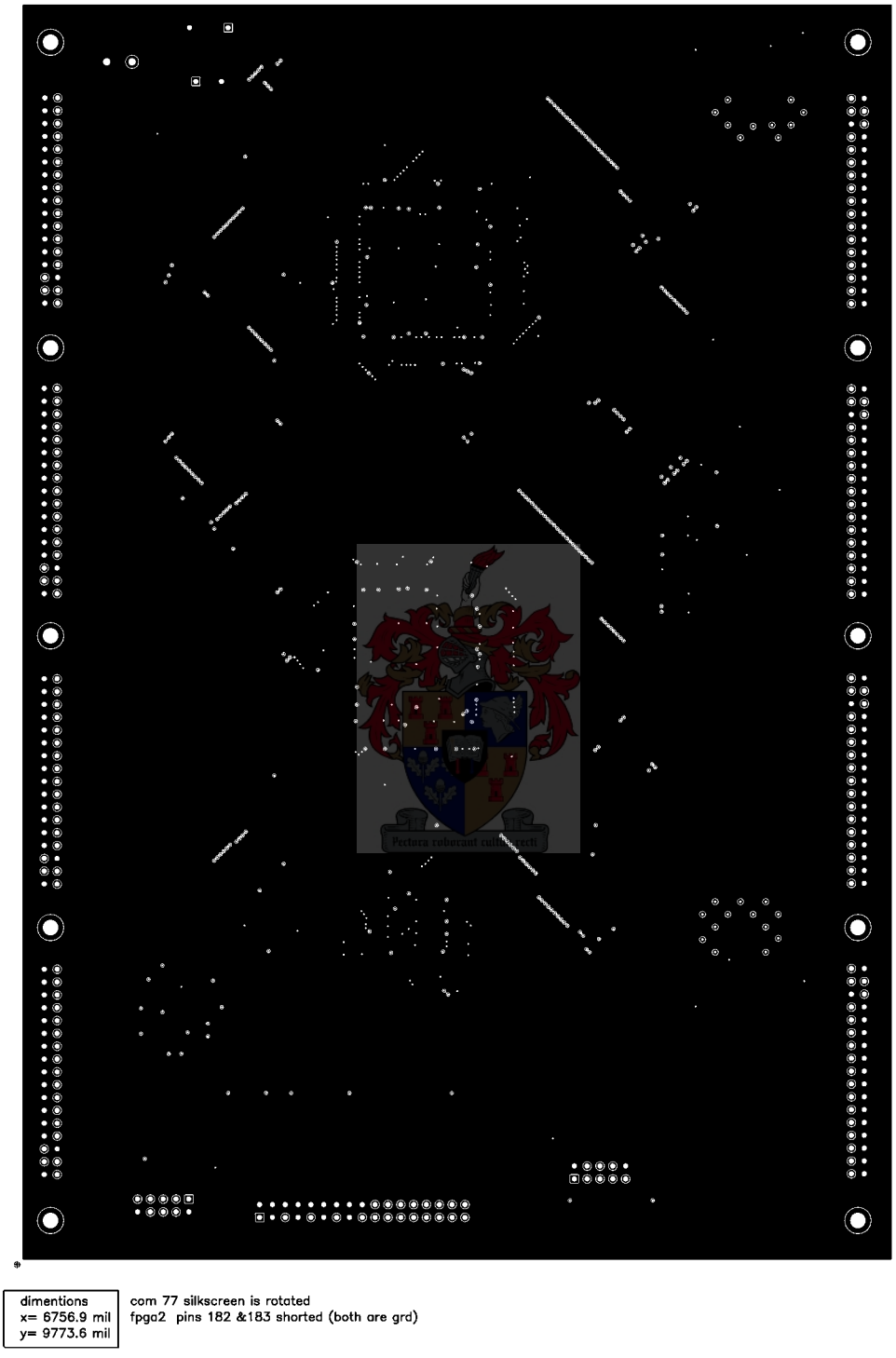

Figure A-8 PCB layout of PWM Expansion Board Ground layer

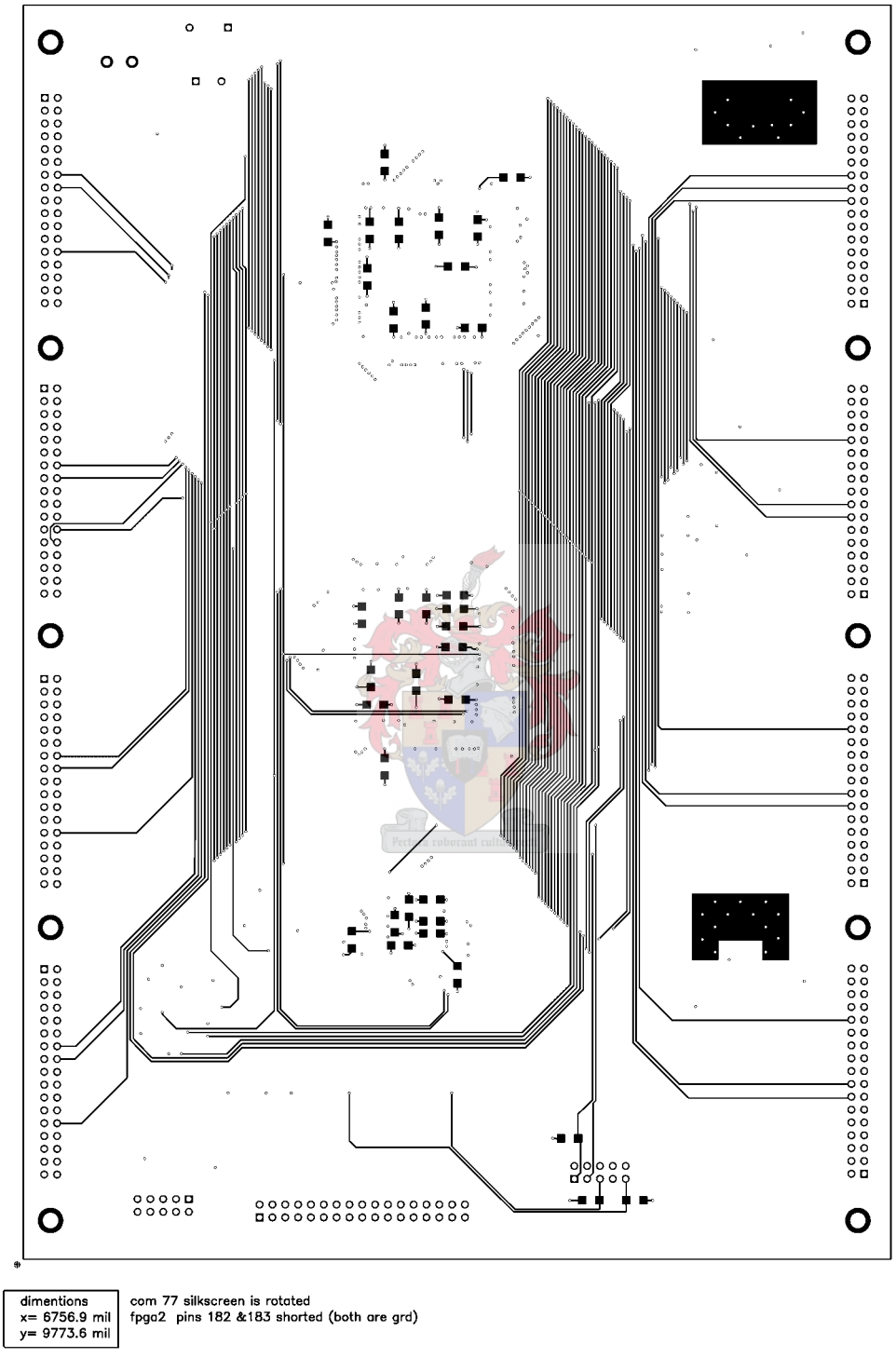

Figure A-9 PCB layout of PWM Expansion Board BOTTOM layer

B. Optical Driver Boards

B1 Schematics of the Optical Driver Boards

B2 Printed circuit board layout of the Optical Driver Boards

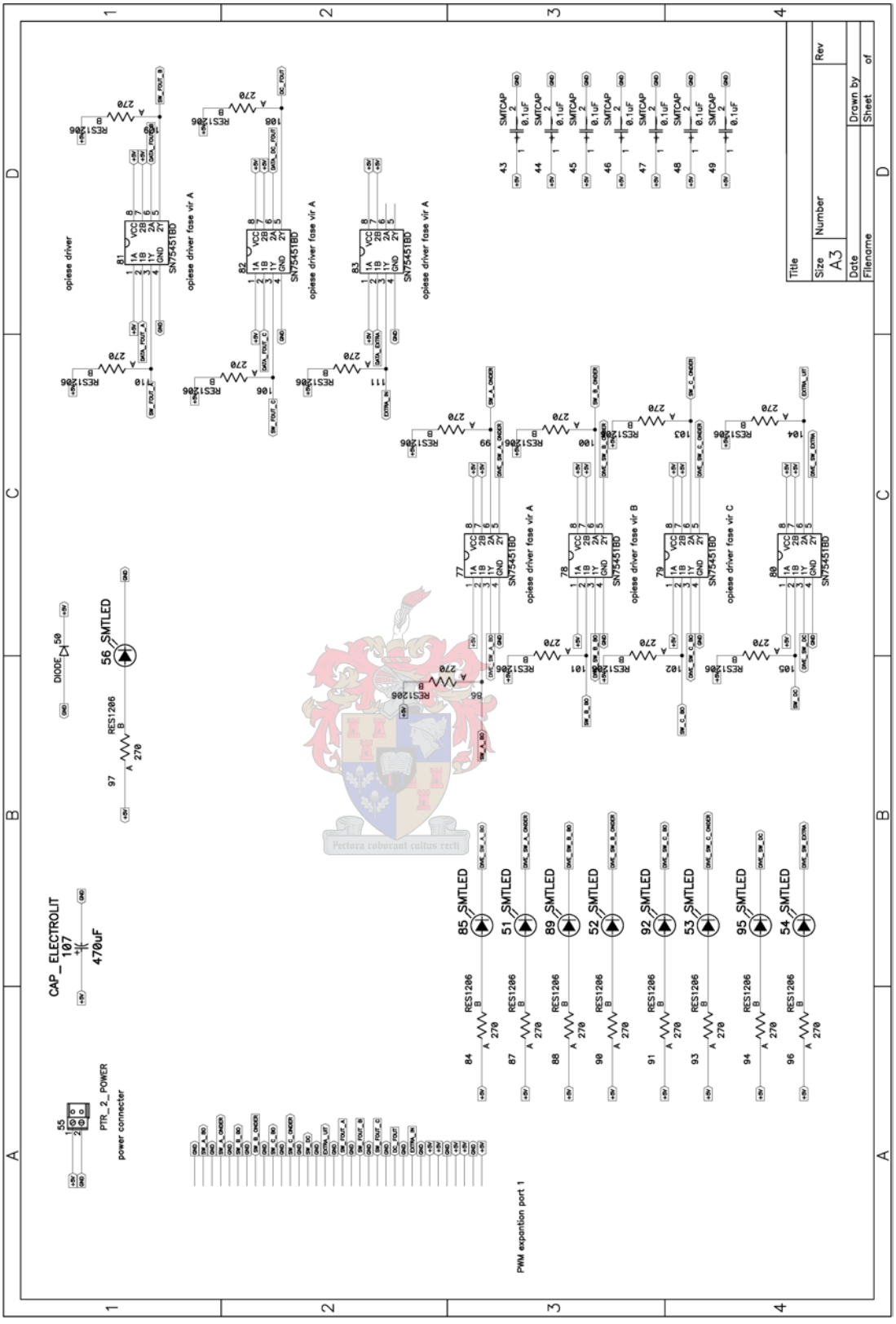

Figure B-1 Schematic of port and driver chips

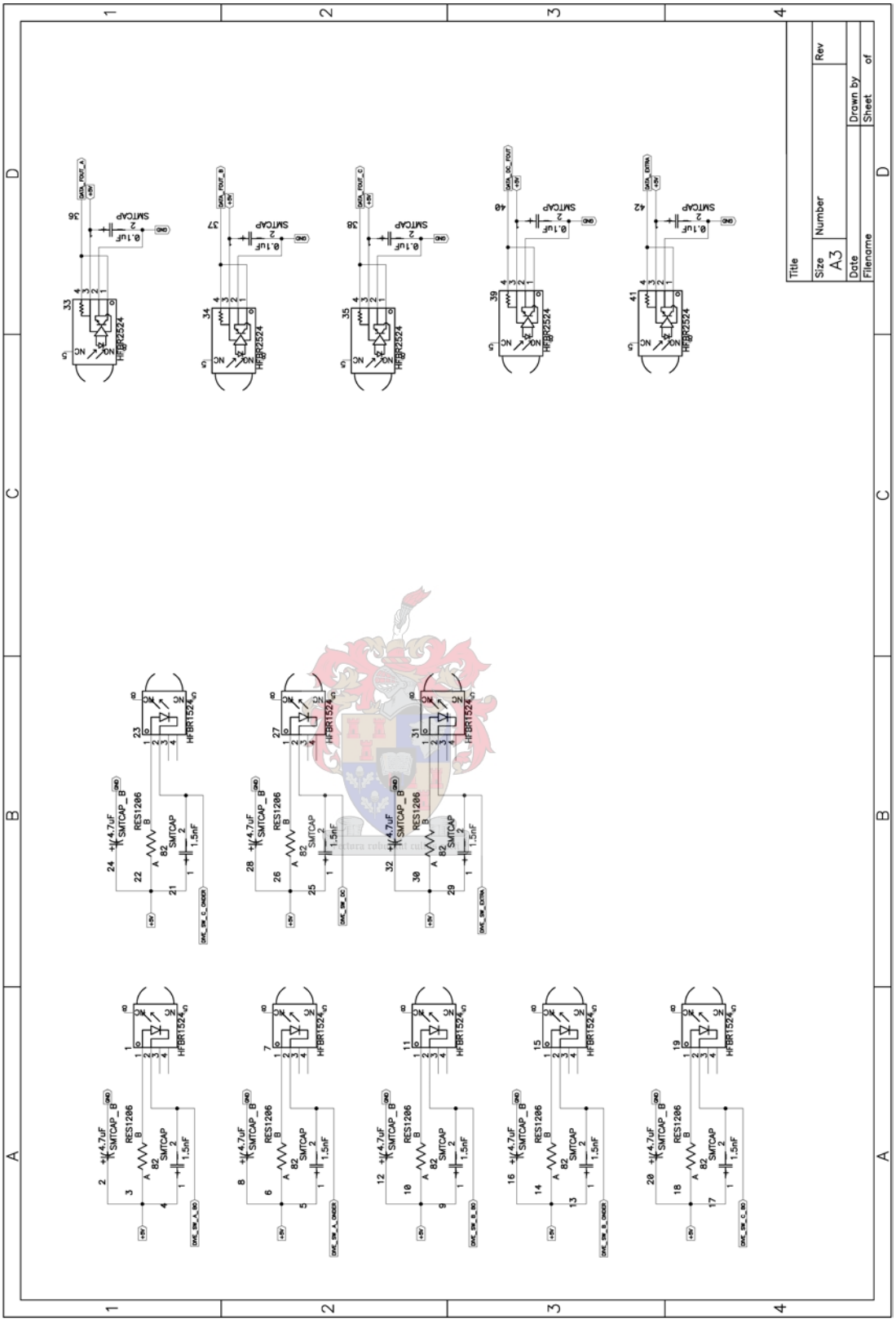

Figure B-2 Schematic of optical sender and receivers

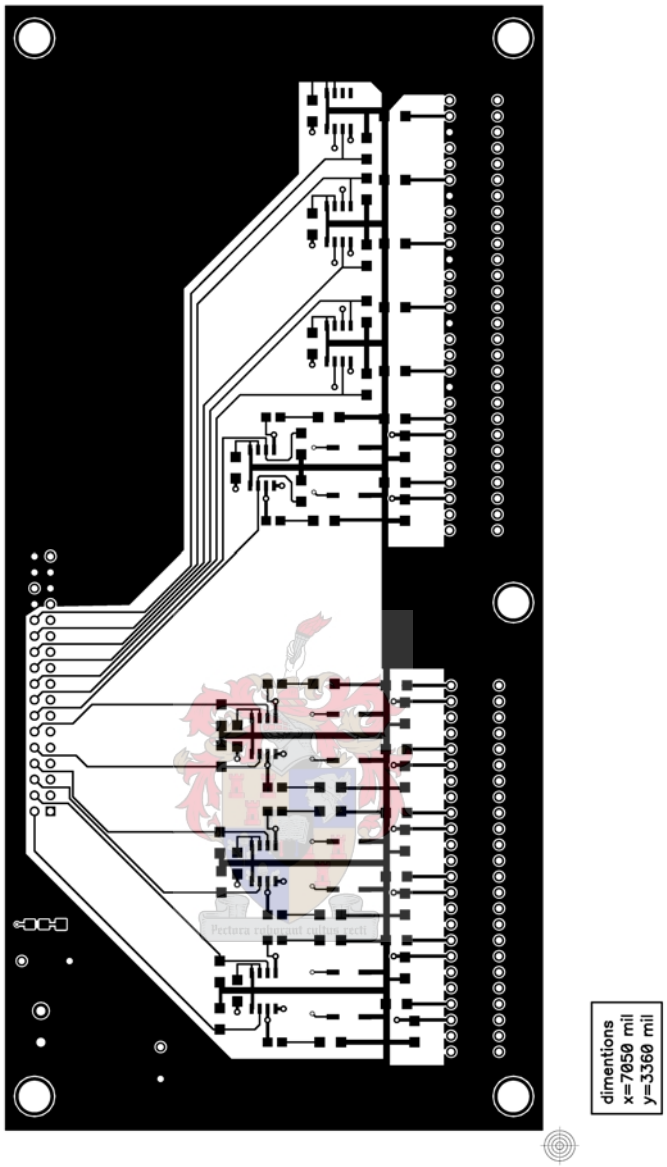

Figure B-3 PCB layout of Optical Driver Board TOP layer

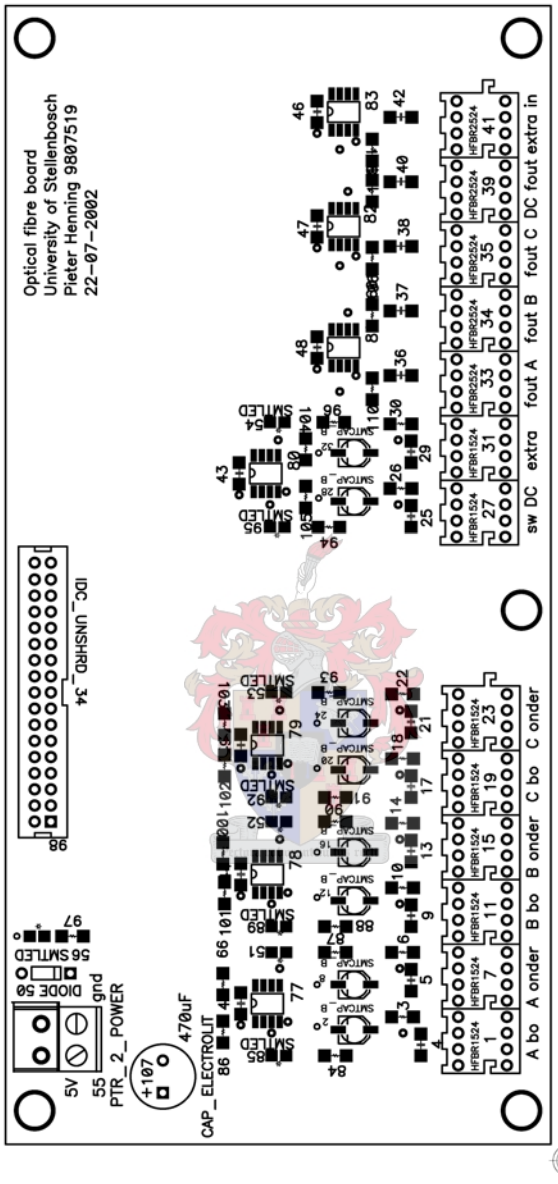

Figure B-4 PCB layout of Optical Driver Board TOP silkscreen and pads

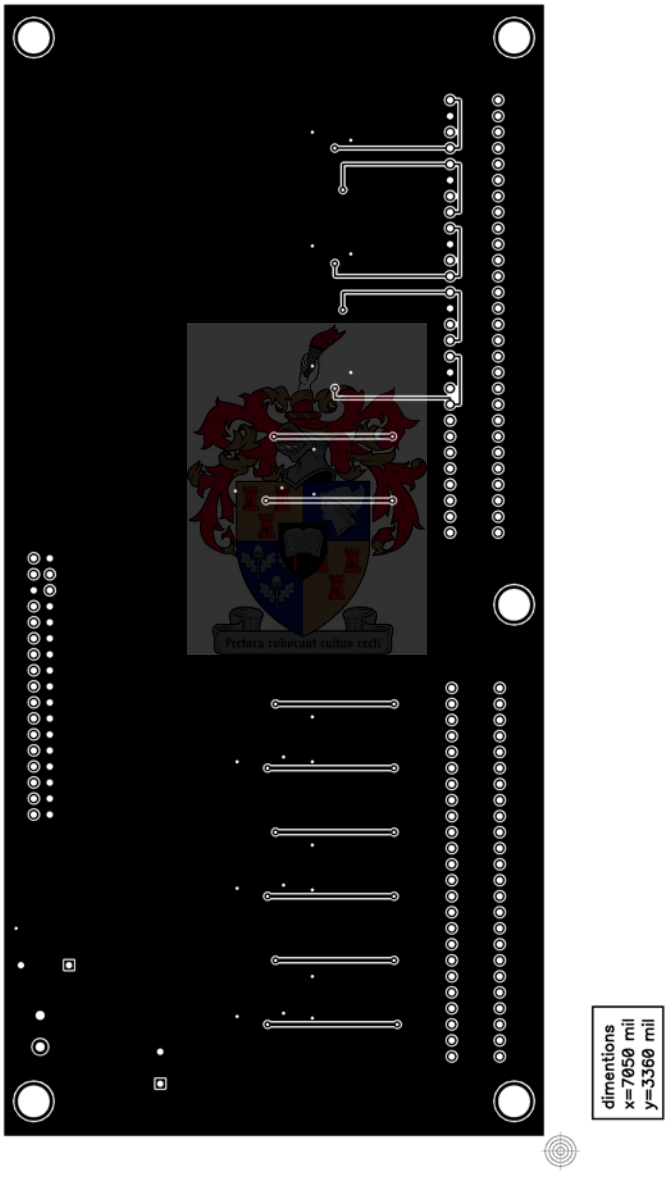

Figure B-5 PCB layout of Optical Driver Board BOTTOM layer

C. EPC2 Modification

C1 EPC2 Modification

Figure C1 shows A diagram of the connection between the PCB pads of the PEC 33 controller board, and the pins of the two EPC2LC20 configuration devices. The pads of the PCB is shown on the outside. The first (BOTTOM) EPC2 is drawn inside the pads and the second (TOP) EPC2 is drawn inside the first EPC2. Most of the pins connect directly to each other. Special connections are from pin 1 of the TOP EPC2 to pin 3 (TDO) of the EPC2 configuration header. Pin 9 of the TOP EPC2 is connected to pin 12 of the BOTTOM EPC2. Pin 11 of the TOP EPC2 is connected to pin 1 of the BOTTOM EPC2. Note that pin 1 of the BOTTOM EPC2 must not be connected to pad 1 (TOD) of the PEC 33 PCB.

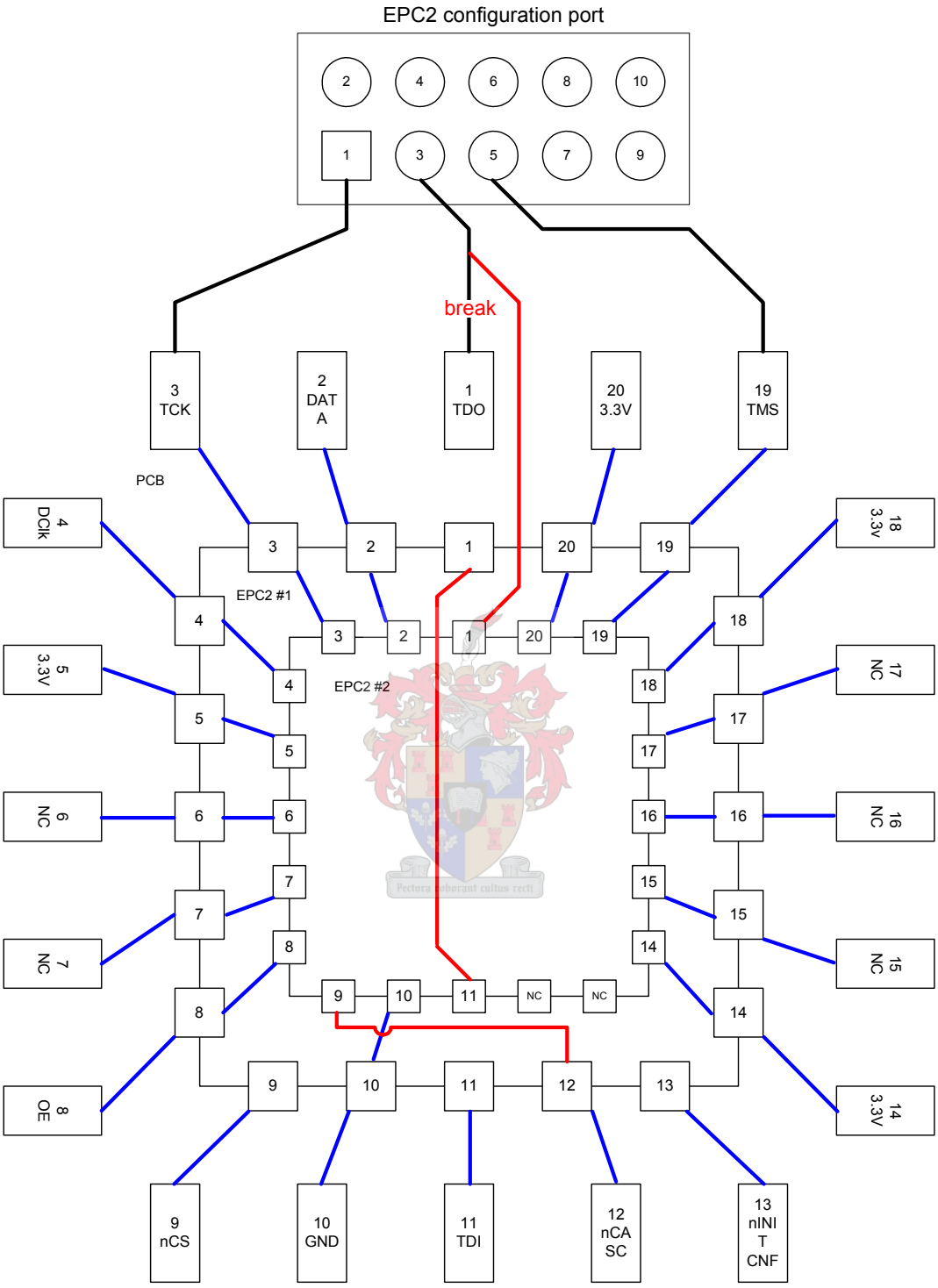

Figure C-1 Diagram showing the connection of the two EPC2 chips and the PEC 33 PCB

D. Memory Allocations & Error code definitions

Table D-1 Memory map of the PEC 33 controller

Address Range	Device allocation
000000 h – 000FFF h	Boot loader
400000 h – 43FFFF h	Flash RAM 0
500000 h – 600000 h	FPGA-Main
600000 h – 60FFFF h	FPGA-Analog
800000 h – 809FFF h	DSP Internal memory
A00000 h – A0FFFF h	External Bus 0
B00000 h – B0FFFF h	External Bus 1
C00000 h – C0FFFF h	Flash RAM 1

Table D-2 Internal memory map of the DSP

Address Range	DSP Internal Allocation
800000 h – 801FFF h	Expansion bus MSTRB active (8K words)
802000 h – 803FFF h	Reserved (8K words)
804000 h – 805FFF h	Expansion bus IOSTRB active (8K words)
806000 h – 807FFF h	Reserved (8K words)
808000 h – 8097FF h	Peripheral bus memory-mapped registers (6K words internal)
809800 h – 809BFF h	RAM block 0 (1K words internal)
809C00 h – 809FFF h	RAM block 1 (1K words internal)

Table D-3 Register definitions in FPGA-Main

Address	Width	Read / Write	Description
000 h	8	W	RS-232 Transmit data
001 h	8	R	RS-232 Receive data
002 h	1	R	RS 232 Transmit status
003 h	3	W	RS 232 Baud rate
008 h	1	R	Flash RAM status
010 h	1	R	RTC Status
011 h	8	W	RTC Write address
012 h	8	W	RTC Write data
013 h	8	R	RTC Read data (seconds)
014 h	8	R	RTC Read data (minutes)
015 h	8	R	RTC Read data (hours)
016 h	8	R	RTC Read data (day)
017 h	8	R	RTC Read data (date)
018 h	8	R	RTC Read data (month)
019 h	8	R	RTC Read data (year)
01A h	8	R	RTC Read data (control)
068 h	1	R	Optical receiver 0 status
069 h	1	W	Optical transmitter 0 data
06A h	1	R	Optical receiver 1 status
06B h	1	W	Optical transmitter 1 data

Table D-3 continued: Register definitions in FPGA-Main

Address	Width	Read / Write	Description
070 h	8	W	RTC write data (seconds)
071 h	8	W	RTC write data (minutes)
072 h	8	W	RTC write data (hour)
073 h	8	W	RTC write data (day)
074 h	8	W	RTC write data (date)
075 h	8	W	RTC write data (month)
076 h	8	W	RTC write data (year)
077 h	8	W	RTC write data (control)

Table D-4 Register definitions for FPGA-Analog

Address	Width	Read / Write	Description
000 h	3	R	DAC 0 configuration data
001 h	12	R	DAC 0 channel A data
002 h	12	R	DAC 0 channel B data
003 h	1	R	DAC 0 load command
004 h	3	R	DAC 1 configuration data
005 h	12	R	DAC 1 channel A data
006 h	12	R	DAC 0 channel B data
007 h	1	R	DAC 0 load command
008 h	3	R	DAC 0 configuration data
009 h	12	R	DAC 0 channel A data
00A h	12	R	DAC 0 channel B data
00B h	1	R	DAC 0 load command
00C h	3	R	DAC 0 configuration data
00D h	12	R	DAC 0 channel A data
00E h	12	R	DAC 0 channel B data
00F h	1	R	DAC 0 load command

Table D-4 continued: Register definitions for FPGA-Analog

Address	Width	Read / Write	Description
010 h	16	W	ADC 0 configuration data (reserved)
011 h	10	R	ADC 0 Channel 0 data
012 h	10	R	ADC 0 Channel 1 data
013 h	10	R	ADC 0 Channel 2 data
014 h	10	R	ADC 0 Channel 3 data
015 h	10	R	ADC 0 Channel 4 data
016 h	10	R	ADC 0 Channel 5 data
017 h	10	R	ADC 0 Channel 6 data
018 h	10	R	ADC 0 Channel 7 data
019 h	16	W	ADC 1 configuration data (reserved)
01A h	10	R	ADC 1 Channel 0 data
01B h	10	R	ADC 1 Channel 1 data
01C h	10	R	ADC 1 Channel 2 data
01D h	10	R	ADC 1 Channel 3 data
01E h	10	R	ADC 1 Channel 4 data
01F h	10	R	ADC 1 Channel 5 data
020 h	10	R	ADC 1 Channel 6 data
021 h	10	R	ADC 0 Channel 7 data

Table D-4 continued: Register definitions for FPGA-Analog

Address	Width	Read / Write	Description
022 h	16	W	ADC 2 configuration data (reserved)
023 h	10	R	ADC 2 Channel 0 data
024 h	10	R	ADC 2 Channel 1 data
025 h	10	R	ADC 2 Channel 2 data
026 h	10	R	ADC 2 Channel 3 data
027 h	10	R	ADC 2 Channel 4 data
028 h	10	R	ADC 2 Channel 5 data
029 h	10	R	ADC 2 Channel 6 data
02A h	10	R	ADC 2 Channel 7 data
02B h	16	W	ADC 3 configuration data (reserved)
02C h	10	R	ADC 3 Channel 0 data
02D h	10	R	ADC 3 Channel 1 data
02E h	10	R	ADC 3 Channel 2 data
02F h	10	R	ADC 3 Channel 3 data
030 h	10	R	ADC 3 Channel 4 data
031 h	10	R	ADC 3 Channel 5 data
032 h	10	R	ADC 3 Channel 6 data
033 h	10	R	ADC 3 Channel 7 data
034 h	1	W	ADC sample command
035 h	9	W	LCD Load Data

Table D-4 continued: Register definitions for FPGA-Analog

Address	Width	Read / Write	Description
036 h	13	R	Digital Voltage register Vac 0
037 h	13	R	Digital Voltage register Vac 1
038 h	13	R	Digital Voltage register Vac 2
039 h	13	R	Digital Voltage register Vac 3
03A h	13	R	Digital Voltage register Vac 4
03B h	13	R	Digital Voltage register Vac 5
03C h	13	R	Digital Voltage register Vac 6
03D h	13	R	Digital Voltage register Vdc 1
03E h	13	R	Digital Voltage register Vdc 2
03F h	13	R	Digital Voltage register Vdc 3
040 h	13	R	Digital Voltage register Vdc 4
041 h	13	R	Digital Voltage register Vdc 5
042 h	13	R	Digital Voltage register Vdc 6
023 h	13	R	Digital Voltage register Vdc 7
044 h	13	R	Digital Voltage register Vdc total
045 h	4	R	Keypad data
048 h	1	R	LCD Ready-not-Busy
050 h	1	R	Soft Starter Status
051 h	1	R	AC Breaker Status
052 h	1	R	DC Breaker Status

Table D-5 Register definitions for External Bus 1 (PWM Expansion Board)

Address	Width	Read / Write	Description
000 h	1	W	PWM Enable command
001 h	10	W	PWM Duty Cycle phase A
002 h	10	W	PWM Duty Cycle phase B
003 h	10	W	PWM Duty Cycle phase C
004 h	1	W	Switch cooling fans
005 h	1	W	Switch DC Breaker
006 h	1	W	Switch AC Breaker
007 h	7	W	Switch DC Dump
008 h	8	W	Switch Soft starter
009 h	10	R	Read Error Data

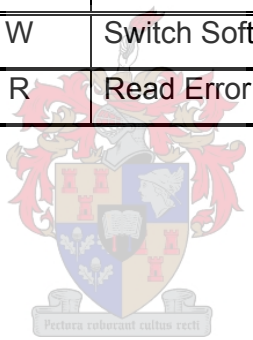

Table D-6 Error code definitions for the PWM Expansion Board

Error Code	Description
1	DC Dump 1 Error
2	DC Dump 2 Error
3	DC Dump 3 Error
4	DC Dump 4 Error
5	DC Dump 5 Error
6	DC Dump 6 Error
7	DC Dump 7 Error
8	AC Breaker open
9	DC Breaker open
12	Level 1 A error
13	Level 1 B error
14	Level 1 C error
15	Level 2 A error
16	Level 2 B error
17	Level 2 C error
18	Level 3 A error
19	Level 3 B error
20	Level 3 C error
21	Level 4 A error
22	Level 4 B error
23	Level 4 C error
24	Level 5 A error
25	Level 5 B error
26	Level 5 C error

Table D-6 continued: Error code definitions for the PWM Expansion Board

Error Code	Description
27	Level 6 A error
28	Level 6 B error
29	Level 6 C error
30	Level 7 A error
31	Level 7 B error
32	Level 7 C error
111	PWM disabled
110	Time error receiving Duty cycle A
220	Time error receiving Duty cycle B
330	Time error receiving Duty cycle C