The Applications of Superconductors in Cellular Network Base Stations

by

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Thesis presented in partial fulfilment of the requirements for the degree of Master of Science in Engineering at the University of Stellenbosch

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Declaration

I, the undersigned, hereby declare that the work contained in this thesis is my own original work and that I have not previously in its entirety or in part submitted it at any university for a degree.

Signature: .....
R. Du Toit

Date: .....

Abstract

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Thesis: MScEng (E&E)

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Wireless communications have increasingly become part of our world. The growth of radio frequency (RF) wireless communications has led to an increasing demand for frequency spectrum licenses, increased system capacity and larger user bandwidths. These demands lead to frequent improvements on the physical and higher layers of wireless communication protocols. Changes in the physical layer are frequently followed by the need for replacement of dedicated hardware components. The need therefore exists for a more general and programmable physical layer. A more general and programmable radio architecture implies increased radio front-end performance without losing programmability.

The contribution of this thesis is the analysis of how superconductor electronics (SCE) using Rapid Single Flux Quantum (RSFQ) logic may advance wireless radio front-ends by providing a general-purpose programmable radio architecture. Superconductor analogue to digital converters (ADCs) are employed as high performance, programmable digitization structures. Once a received signal is digitized, SCE can be used to rapidly do recursive operations such as synchronization and multi-path delay estimation. These operations are based on correlation, and for evaluation of such operations with SCE the popular CDMA multiplexing method is studied along with the WCDMA protocol used in the 3G UMTS standard.

Two delta-type oversampling superconductor ADC modulator designs are presented and evaluated along with a hybrid decimation filter design, using both the benefits of

SCE and room temperature electronics. A fast RSFQ correlator design is also presented and evaluated for use in a multi-path estimation structure. A rapid multi-path delay estimation architecture based on fast RSFQ circular data buffers and correlators is presented. The architecture uses the fast speeds of RSFQ logic to obtain accurate path delay estimates in a rapidly changing wireless environment.

It is concluded that RSFQ-based wireless receiver components offer promising new options for data conversion, correlation and multi-path delay estimation implementations.

Samevatting

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Draadlose kommunikasie word al hoe meer deel van ons wêreld. Groei in radiofrekwensietipe kommunikasie het gelei tot 'n toenemende aanvraag na frekwensiespektrum lisensies, vergrote stelselkapasiteit en groter gebruikerbandwydtes. Hierdie aanvrae lei tot gereelde en spoedige verbeteringe op die fisiese en hoër lae van huidige draadlose kommunikasieprotokol. Veranderinge in die fisiese laag vereis gewoonlik dat toegewyde hardewarde komponente vervang word. Die behoefte bestaan dus vir 'n meer algemene, programmeerbare fisiese laag. Dit vereis dus 'n verbetering in die radio-ontvanger se komponente naaste aan die antenna sonder om programmeerbaarheid te verloor.

Die bydrae van hierdie tesis is hoofsaaklik die analise van hoe supergeleierelektronika wat van *Rapid Single Flux Quantum* (RSFQ) logika gebruik maak, huidige draadlose sellulêre basisstasies se fisiese laag kan verbeter deur 'n meer algemene en programmeerbare radio-argitektuur op te lewer. Supergeleier analoog-na-syfer omsetters (ADCs) word bestudeer as moontlike programmeerbare versyferingstrukture wat steeds hoë werkverrigting lewer. Wanneer 'n ontvangde sein in digitale vorm omgesit is, kan supergeleierelektronika gebruik word om vinnig rekursiewe operasies uit te voer. Voorbeelde van sulke operasies is sinkronisasie en die waardebepaling van die vertraging van verskillende paaie wat 'n sein volg na die ontvanger. Hierdie spesifieke operasies se werking is gebaseer op korrelasie, en vir die evaluasie van sulke operasies met supergeleierelektronika is die gewilde

Code Division Multiple Access (CDMA) seinsamestellingsmetode bestudeer saam met die wyeband-CDMA (WCDMA) protokol wat gebruik word in die 3G UMTS-standaard.

Twee supergeleier-delta-tipe oorversyferings-ADC-moduleerderontwerpe word voorgelê en evaluasie word daarop gedoen saam met 'n hibriede desimasiefilterontwerp wat gebruik maak van beide die voordele van supergeleierelektronika en kamertemperatuurelektronika. 'n Vinnige RSFQ-korreleerder word ook voorgelê en evaluasie word daarop gedoen vir gebruik binne 'n multi-padvertraging-waardebepalerstruktuur. Hierdie struktuur wat gebaseer is op RSFQ sirkulêre buffers en korreleerders, word voorgelê. Die waardebepaler maak gebruik van die spoed van RSFQ-logika om akkurate multi-padvertragingswaardes te bepaal in 'n vinnig veranderende draadlose omgewing.

Die gevolgtrekking word gemaak dat RSFQ-gebaseerde draadlose ontvangerkomponente groot voordele in versyfering-, korreleerder- en multi-padvertragingsbepaler-toepassings bied.

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- Psitek for their funding and interest in our research.
- Our God, for His love, wonderful creation and His supply of joy, peace, hope and strength.

Contents

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List of Abbreviations

2G	2nd Generation
3G	3rd Generation
3GPP	3rd Generation Partnership Project
ADM	Asynchronous-based Delta Modulator
AWGN	Additive White Gaussian Noise
BER	Bit error rate
BPF	Band-Pass Filter
BS	Base Station
BSC	Base Station Controller
BSS	Base Station Subsystem
BTS	Base Transceiver Station
CDMA	Code Division Multiple Access
DC	Direct Current
DM	Delta Modulator
DPDCH	Dedicated Physical Data Channel
DPCCH	Dedicated Physical Control Channel
DR	Dynamic Range
DRO	Destructive Readout Register

DSP	Digital Signal Processing
EDGE	Enhanced Data rate for GSM Evolution
ENOB	Effective Number Of Bits
FDMA	Frequency Division Multiple Access
FFT	Fast Fourier Transform
FIFO	First-In-First-Out
FIR	Finite Impulse Response
GSM	Global System for Mobile communications
HDL	Hardware Description Language
HTS	High-Temperature Superconductor
HUFFLE	Hybrid Unlatched Flip-Flop Element
IC	Integrated Circuit
IF	Intermediate Frequency
JJ	Josephson Junction
JTL	Josephson Transmission Line
LPF	Low-Pass Filter
LNA	Low Noise Amplifier
LSB	Least Significant Bit
LTS	Low-Temperature Superconductor
NRZ	Non-Return-to-Zero
MAI	Multiple Access Interference
MRC	Maximum Ratio Combining
Mbps	Megabits per second

MSB	Most Significant Bit
MS/s	Mega Samples per second
OVSF	Orthogonal Variable Spreading Factor
PG	Processing Gain
PMD	Phase Modulation-Demodulation
PN	Pseudo-random Number
RAT	Radio Access Technology
RCSJ	Resistive Capacitive Shunted Junction
RF	Radio Frequency
RNC	Radio Network Controller
RSFQ	Rapid Single Flux Quantum
QoS	Quality of Service
SCE	Superconductor Electronics
SDR	Software Defined Radio
SF	Spreading Factor
SFDR	Spurious Free Dynamic Range
SFQ	Single Flux Quantum
SINAD	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
SQUID	Superconductor Quantum Interference Device
SS	Spread Spectrum
SWR	Software Radio
TDMA	Time Division Multiple Access

TFF	Toggle Flip-Flop
UE	User Equipment
UMTS	Universal Mobile Telecommunications System
UTRAN	UMTS Terrestrial Radio Access Network
WCDMA	Wideband CDMA
YBCO	Yttrium Barium Copper Oxide

List of Symbols

Constants:

p	pico, scale constant, 1×10^{-12}
n	nano, scale constant, 1×10^{-9}
μ	micro, scale constant, 1×10^{-6}
m	milli, scale constant, 1×10^{-3}
k	kilo, scale constant, 1×10^{3}
M	mega, scale constant, 1×10^{6}
G	giga, scale constant, 1×10^{9}
T	tera, scale constant, 1×10^{12}
π	Pi $\backsimeq 3.14159$
e	The Magnitude of electron charge $\backsimeq 1.602 \times 10^{-19}$ C
h	The Planck constant $\backsimeq 6.626 \times 10^{-34}$ Js
Φ_0	Magnetic flux quantum $\backsimeq 2.0678 \times 10^{-15}$ Wb

Units of Measure:

A	Ampère
C	Coulomb
dB	Decibel
F	Farad
H	Henry
Hz	Hertz
J	Joule
K	Kelvin
Ω	Ohm

s	Seconds
V	Volt
W	Watt
Wb	Weber

Chapter 1

Introduction

1.1 Motivation

Superconductors have interesting properties with promising potential applications. The aim in this thesis is to explore some of the possible applications of these conductors in a fast evolving wireless world, rich in opportunity for improvements. Previous work on superconductor applications in wireless systems led to many questions about the specifics of implementation. This thesis aims to answer some of these questions, building on the ideas proposed elsewhere on how to apply this high-potential technology. In addition to this, exploration is done in this field to find new ideas for cellular network base station improvement.

A leading method of multiplexing in current third generation (3G) cellular systems is code division multiple access (CDMA). In this thesis there is a strong focus on this widely used multiple access method because of its popularity and potential for capacity improvements.

Only cellular network base station applications are considered because of the specialized cooling requirements of superconductors.

1.2 Cellular technology trends and requirements

In modern wireless communications the transition from narrowband data to wideband data has created an increasing need for channel selection and signal processing in the digital domain. First generation wireless technologies such as AMPS, had a dedicated 30kHz band per user. The second generation delivered standards such as GSM with a shared 200kHz band using TDMA for 8 user slots. Third generation (3G) technology give us

5 MHz bands which are shared among numerous users. Such wideband technologies decrease the need for multiple expensive analogue components including mixers, amplifiers, filters and data converters. This results in the cost per resource in continuous use (cost per Erlang) to be much lower for 3G than 2G [1]. Although wideband communications require much higher digital processing power, the advances as predicted by Moore's law have allowed the necessary DSP drive to enable 3G technologies [1].

As the cellular standards develop and improve, the need arises for a more flexible architecture. Such architecture should offer a system which can be updated and expanded in a cost-efficient way. A solution to the above mentioned rapid changes in wireless technology is to shift all operations to the digital domain - a fully digital RF system also known as the Software Radio (SWR) or Digital RF radio as seen in Fig. 1.1 (a). Such a system eliminates the need for expensive and precise analogue components by shifting the ADC as close to the antenna as possible. The SWR digitizes the whole RF-band of interest directly after the antenna. To implement this architecture an ADC needs to deliver 14 to 16 bits resolution with a bandwidth of about 1.4 GHz (800 MHz - 2.2 GHz). This is impractical for a single receiver because of high required SNRs, high required LNA performance and future ADC performance projections [2, 3, 4]. In order to realize such a system, the band of interest could be divided into sub-bands and digitized by multiple wideband bandpass ADCs [5, 2] as seen in Fig. 1.1 (b). Data is then processed by DSP units to give different services. A more practical receiver realization of

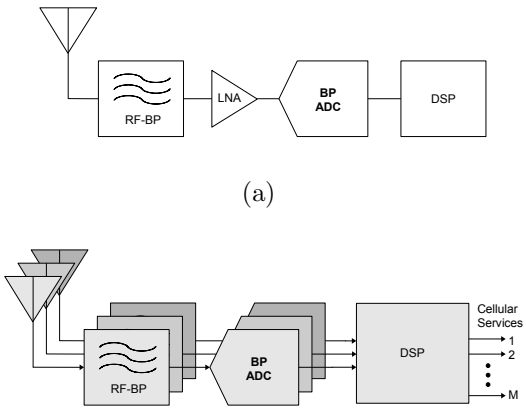


Figure 1.1: (a) Digital RF radio with direct digital downconversion and (b) a practical architecture to cover the whole RF band of interest

the SWR (due to ADC technology restrictions) is the Software-Defined Radio (SDR) where the front-end is a typical superheterodyne RF receiver architecture as seen in

Fig. 1.2. Analogue to digital conversion is done at IF or baseband frequencies, allowing less stringent ADC requirements. Such a receiver will then use software procedures for demodulation, digital filtering, channelization and other required radio functions. It is important to note that when changing the frequency to IF or baseband (by analogue mixing), phase information is distorted. Many digital encoding technologies make use of phase information, making IF or baseband sampling systems less ideal than direct sampling systems. In order to implement these flexible architectures, faster ADCs offering

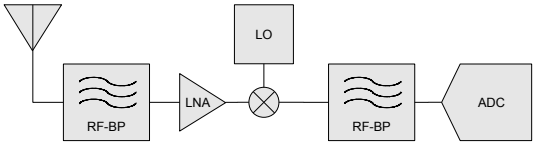


Figure 1.2: Digital IF or baseband radio front-end for SDR, using the classic superheterodyne architecture

more resolution is needed. Semiconductor technology is showing slow progress in this field [5] and therefore other technologies are being considered. Microcircuit manufacturers are looking into parallelization and multi-core technologies to keep up the pace, but some problems are serial by nature and require rapid execution. One of the most promising technologies for superior ADCs is RSFQ superconducting electronics. These electronics show much potential for implementation of very fast serial operations. Superconductors have many other useful applications in wireless communications which are discussed in following sections.

1.3 RSFQ Superconducting Electronics

As most semiconductor electronic device circuit speeds reach their limit, superconducting electronics are still in very early stages of growth. These superconducting electronics (SCE) offer very fast operating speeds and are still far from reaching their physical limits. These circuits work by means of pulse-based logic (not voltage state) called Rapid Single Flux Quantum (RSFQ) logic. In RSFQ logic, operations with quantum accuracy are made possible, offering extremely linear circuits. For more information on how RFSQ logic works, see Section 3.1.

Currently SCE circuits are mostly manufactured with low-temperature superconductor metals such as Niobium. These circuits operate at cryogenic temperatures below 4 Kelvin which are easily obtained by expensive modern cryogenic coolers. High temperature

superconductors (such as YBCO) are mostly used for sharp and effective linear analogue filtering, but digital circuits are also possible. Problems are currently experienced in the effective fabrication of such digital circuits. YBCO circuits are generally operated at temperatures of about 60 Kelvin which can be obtained by much smaller and less expensive cryogenic coolers.

1.4 Superconductors in Wireless applications

One of the biggest advantages that superconductors have to offer in wireless applications is the implementation of a superconducting ADC. This follows from superconducting and RSFQ circuit characteristics that are uniquely suitable for analogue-to-digital conversion in a wireless environment (see Section 4.3). Superconducting electronics also offer ADC architectures that are dynamically programmable. This allows a trade off between resolution and bandwidth which is particularly favourable where quality of service (QoS) varies between standards. This flexibility is not available in similar high performance semiconductor ADCs which are generally designed for a single operating frequency [2]. All these advantages make superconductor electronics favourable for the implementation of SDR.

As mentioned in Section 1.3, HTS filters can be used for effective analogue filtering. Using these small high-order filters with low insertion loss yield substantial receiver improvements in sensitivity and selectivity. These filters especially offer significant improvements in CDMA systems [6] through their high selectivity (see next section for more).

These improvements in base station sensitivity, selectivity and resolution extends its range (area of service) and also fulfils the desire to keep the complexity in the base station and therefore allowing handsets to be simple and low-power.

1.5 Superconductors in Spread Spectrum Systems

One of the key technologies used in Third-Generation (3G) wireless communications is Code-Division Multiple Access (CDMA). Instead of giving users access by individual timeslots or frequency bands, access is gained by certain codes, known by the user equipment (UE) and base station (BS). In this way the information of many users are spread over the same wide frequency band. Such systems are termed spread spectrum (SS) systems and are explained in more detail in Chapter 2. The ability of a SS system to recover information depends on the orthogonality between spread signals. In asynchronous SS

systems the information recovery also depends on the synchronization of despreading codes with spread signals. The number of users capable of using a certain frequency band is determined by various factors. The Shannon-Hartley law [7] states that channel capacity is limited by channel bandwidth and signal-to-noise ratio (SNR) as follows:

$$C = B\log(1 + \frac{S}{N}). \tag{1.1}$$

Here C is the maximum channel capacity (in $bits/second$), B is the channel bandwidth (in Hz), S is the signal power and N the noise power (both S and N are in watts). Capacity can therefore be increased linearly by using larger bandwidths. It is only increased logarithmically by increasing S and decreasing N.

Some of the factors influencing the maximum number of users (N_u) in a SS system are as follows:

- The ratio of code bandwidth f_c to the user information bandwidth f_b.
- The signal-to-interference ratio, defined as the energy per information bit to the interference spectral density (E_0/I_0). Interference I_0 is used here to collectively represent the noise floor, in-band interference and out-of-band interference. Any interference degrades synchronization ability and orthogonality between spread signals. The maximum number of users per channel (N_u) can therefore be expressed proportional to these two factors as follows:

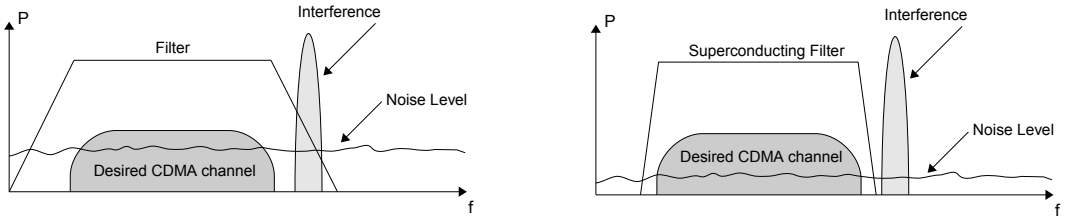
$$N_u \propto \frac{f_c}{f_b} \times \frac{E_0}{I_0} \tag{1.2}$$

With superconducting digital circuits, much higher code frequencies (f_c) are possible. This allows for despreading operations (correlations) at RF frequencies, directly on the sampled RF waveform, which eliminates the need for down-conversion in order to despread a signal [8]. Using SCE also lowers the noise floor and offer capacity improvements as it would to all other multiple access techniques.

In conventional CDMA detectors only user specific sequences are used along with the received signal for signal restoration while other user signals are regarded as noise. An alternate method is called multi-user CDMA detection where spread user signal restoration is aided by information about other user signals in the same frequency band. Parallel interference cancellation algorithms [9] is a method for achieving such multi-user detection by means of channel parameter estimation. To support these algorithms in real-time for a commercially interesting number of users, digital signal processing requirements lie far beyond what is currently possible in semiconductor technologies. Here superconducting

electronics can be used in such detectors to make them practical for a large number of users. Studies show capacity improvements of 35 % compared to conventional receivers [10].

HTS filters have general benefits for wireless systems because of their sensitivity. Combined with a cooled LNA, such a receiver effectively lowers the noise level as seen in Fig. 1.3. These filters offer great advantages to interference limited systems such as CDMA because of their selectivity. With excellent out-of-band interference rejection as shown in Fig. 1.3, studies done by S.C. Bundy [6] show that HTS filters can significantly improve CDMA system capacity. Numerous opportunities therefore exist to optimise spread spec-



(a) Conventional Receiver (b) Cryogenic Receiver

Figure 1.3: Advantages of using HTS filters with a cryogenic LNA

trum channel capacity by lowering noise and interference levels. According to Eq. 1.1 this has the effect of a lower noise power, leading to increased maximum channel capacity.

In asynchronous spread spectrum systems, the synchronization and multi-path estimation processes require fast execution in rapidly varying wireless environment. Superconducting electronics can be used in a synchronizer or estimator to perform very fast correlations along with fast threshold decision making. Little research has been done in this field with regards to SCE and some designs and implementations are presented in Chapter 5. More about the principles of synchronization and path estimation can be found in Section 2.2.

1.6 Competing and Complementing Technologies

Technologies that may complement or compete with SCE are considered. These may have the ability to bring significant improvements or solve certain problems experienced with SCE. Such technologies are mentioned to keep perspective on SCE advantages.

Recently a new switching speed record was set by researchers from IBM and Georgia Tech for semiconductor electronics [11, 12]. They were successful in demonstrating

silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) operation at more than 500 GHz. The circuit was liquid helium cooled at a temperature of 4.5 Kelvin. Their simulations show that speeds of up to 1 THz are possible. Similar experiments demonstrate room temperature SiGe HBT operation at 350 GHz. Although the technology may compete with some superconducting applications, it may remain inferior in applications that rely on some unique RSFQ circuit advantages like sensitivity and natural quantization. Technologies such as this may fill the gap that RSFQ circuits have in terms of an electronic switch (transistor). While conventional semiconductors may fail in very low temperature environments, these SiGe chips can run in the same cryogenic environment as RSFQ circuits - further broadening the possibility for integration of the two technologies.

1.7 Research approach

From the sections mentioned above it is clear that superconductors have a wide range of applications in wireless systems and spread spectrum technology (CDMA). The challenge is to design system components showing advantages that SCE offer in wireless systems and specifically cellular network base stations using CDMA technology. This is achieved by first evaluating physical layer components of modern wireless spread spectrum systems. Models are produced for physical layer components and CDMA user signals. These models create a foundation according to which SCE components are designed. For the scope of this thesis, two main areas for SCE applications are identified:

1. Sampling: Analogue to digital conversion using SCE.
2. Multiple signal path delay estimation using a combination of SCE and room temperature electronics.

The sampling and path delay estimation are discussed independent of each other. The sampling concepts are independent of CDMA technology, while path delay estimation is strongly dependent on the CDMA communication signals and protocol. The proposed ADC and path estimator can function together (directly connected to one another), but independent use of the components are also possible.

Fig. 1.4 gives an overview of the typical components in the uplink physical layer of a modern CDMA based wireless cellular system. The components identified for SCE implementation are shown along with their respective arrangement in the uplink architecture. All modelled structures in this thesis are also indicated.

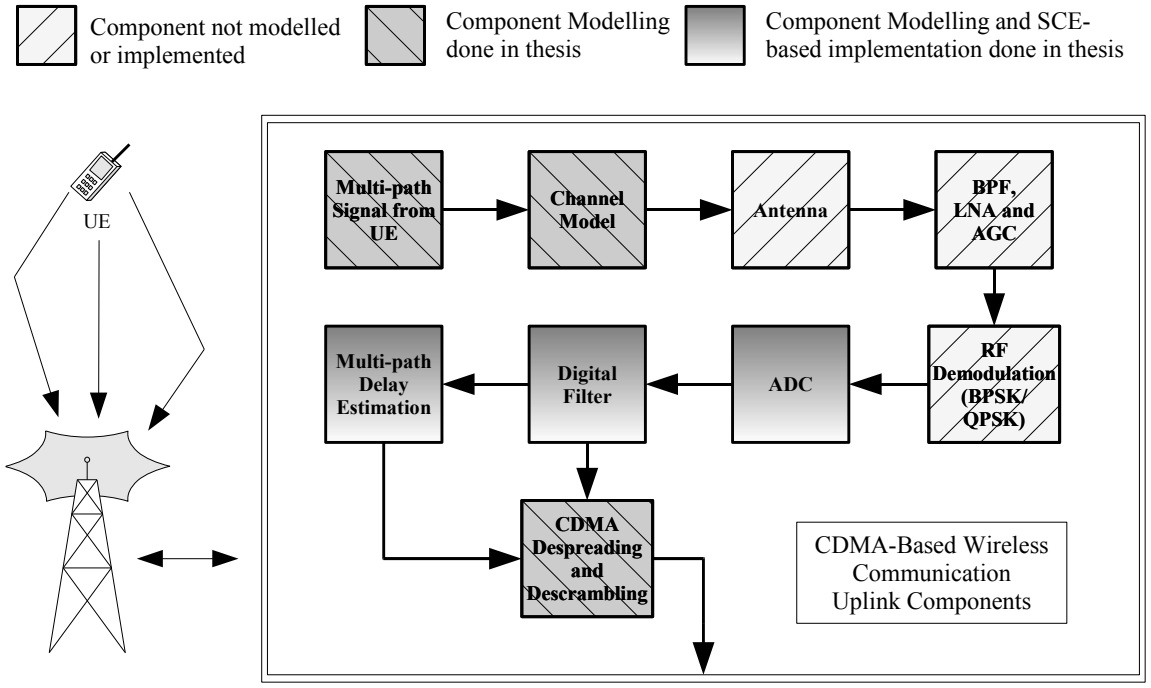


Figure 1.4: Components identified for SCE implementation in the uplink of a wireless cellular communication system.

1.8 Overview of Thesis

- In Chapter 2 various concepts surrounding spread spectrum systems are introduced. The physical layer components of a CDMA uplink channel are also discussed and modelled for the use with other component models in this thesis.

- After basic concepts of wireless spread spectrum systems have been introduced along with motivations for SCE implementation of some components, RSFQ SCE are introduced in Chapter 3. The Josephson Junction circuit model is introduced along with the RSFQ cell library.

- Chapter 4 covers general sampling concepts along with how SCE circuits are used for sampling and specifically oversampling architectures. A few RSFQ analogue to digital converters are discussed while in-depth evaluations and modelling is done for two variations of the SCE delta oversampling modulator. A decimation structure is then proposed for the increase of ADC dynamic range and lowering of output sample rate. The decimation filter is modelled in order to compare the ADC output dynamic range of different oversampling modulators.

- Chapter 5 is dedicated to the design, modelling and simulation of a rapid multi-path delay estimation architecture using RSFQ SCE. Firstly an RSFQ correlator design is presented along with a technique for the comparison of different correlators. A rapid data repeater design is presented for use with the RSFQ correlator to form an important part of the RSFQ rapid multi-path delay estimator. The complete estimator design is then presented along with circuit layout considerations.
- Chapter 6 presents conclusions that are obtained from the work presented in this thesis. The contributed work is summarized and conclusions are drawn. Future research opportunities are also discussed in the light of conclusions made in this thesis.

1.9 Contributions

The following is a summary of the main contributions of this thesis:

- Contributions in RSFQ Superconductor Electronics (SCE)
  - Detailed analysis of the WRspice JJ model including the equations necessary to adapt the model for a specific fabrication process.
  - A specific Toggle Flip-Flop cell (T2FF) which is derived from other TFFs. A T2FF with destructive readout is also contributed along with a T2FF with destructive readout and 2 inputs.
  - A DC-enabled JTL cell for blocking or passing SFQ pulses.
- Superconductor ADC contributions
  - Detailed specifications of superconductor ADC input waveform frequency and amplitude depending on certain parameters.
  - Two different superconductor delta-type ADC modulator designs. One of these designs include a new oversampling technique.
  - A MATLAB model for each of the designed modulators that simplify the quantum effects.
  - A simplified superconductor based decimation filter design for small layout size.
  - A MATLAB model of the decimation filter.

  - Dynamic range evaluations that lead to conclusions about how modulator slew-rate and sensitivity relate to the dynamic range of the modulator.

- Contributions in CDMA-based communications

  - A CDMA channel model incorporating random user data, scrambling codes (Gold codes), multiple path delays and AWGN.
  - A multi-path delay estimation model.

- Path delay estimation contributions

  - A comparison method for different correlator configurations.
  - An RSFQ-based correlator model.
  - An RSFQ correlator circuit design based on an ideal correlator model.
  - A rapid data supply model based on a dual function circular FIFO buffer that is controlled by data and clock switching components.
  - An RSFQ circuit implementation of the rapid data supply model.

For more details about the contributions see Section 6.2.

Chapter 2

Spread Spectrum Systems

As the frequency spectrum becomes increasingly populated, spread spectrum (SS) systems are gaining popularity. These systems are much more complex and expensive, but are proven to use the spectrum more efficiently. In addition to this SS systems offer excellent interference rejection and signal security. Some conventional systems try to put as much information in as small a bandwidth as possible. This makes them much more prone to jamming signals or interference. SS systems avoid jamming by spreading the information across a much higher bandwidth than the user information. Pseudo-Noise (PN) spreading codes can also provide security which makes it extremely difficult to eavesdrop on a conversation or data transmission.

Some of the popular spread spectrum techniques are direct spread (DS), frequency hopping and time hopping. In this thesis CDMA is used as method for allowing multiple users in the same bandwidth and only DS SS systems are considered.

This chapter starts with a basic introduction to spread spectrum systems and CDMA. Techniques used for CDMA user signal detection are then discussed. In the asynchronous CDMA environment generally used for cellular systems, synchronization is necessary. Synchronization refers to a process of phase difference detection in such an environment. Phase difference detection in a CDMA environment is presented and discussed. This is followed by a look into the properties of different SS system code types. Typical code usage in modern SS systems is then presented. At the end of this section a simplified WCDMA model is presented along with path estimation and bit error rate (BER) evaluations.

2.1 Code-Division-Multiple-Access data transmission

The CDMA concept is first explained from a time-domain point of view by way of two users, each with their own data, which they want to transmit to a single receiver. User data is defined in Fig. 2.1 as *A data* and *B data*. As mentioned in previous sections, each user obtains a special code, containing much higher frequencies than their data, whereby they will communicate. Assigned codes are shown as *A code* and *B code*. Each user's data is then mixed with the code, forming a signal that contains information about the user data. These users will then transmit these waveforms with some form of modulation. These signals, using the same frequency band, will then be superimposed as represented in Fig. 2.1 by the composite signal $A + B$. A receiver can then recover one of the

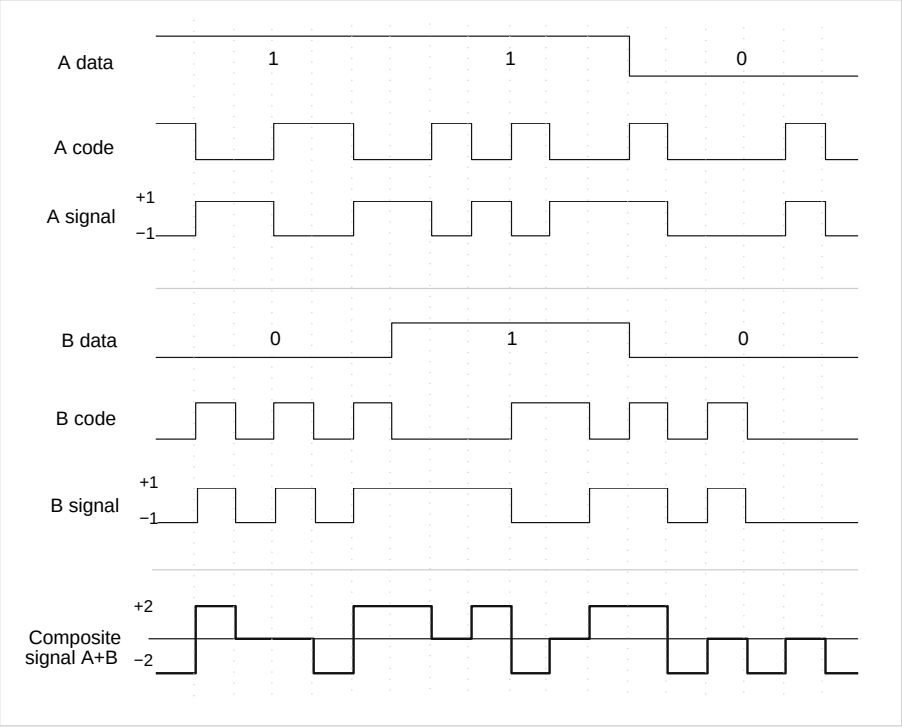


Figure 2.1: Creation of a simple CDMA signal containing information of two users

two users' data, depending on the code used for the operation. A simple despreading scenario is shown in Fig. 2.2 where user A's data is recovered. Note that the integrator combined with the comparator alleviates the effects of additive noise and the recovered data is inverted. In the same way user B's data can be recovered by mixing the composite

signal with *B code*. If another code is used (one that was not used for encoding data) to decode the composite signal, a low amplitude noise signal would result. From a frequency

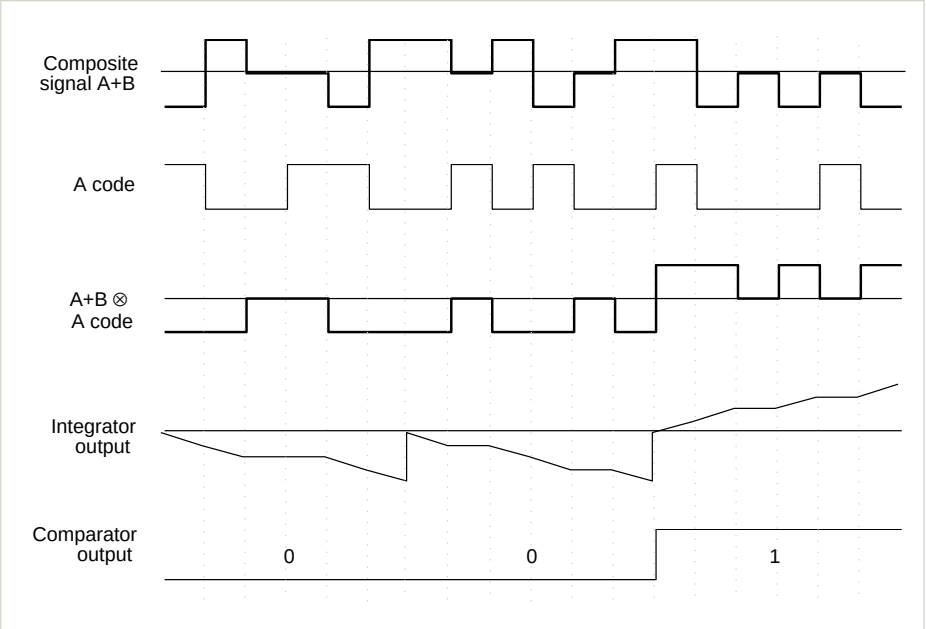
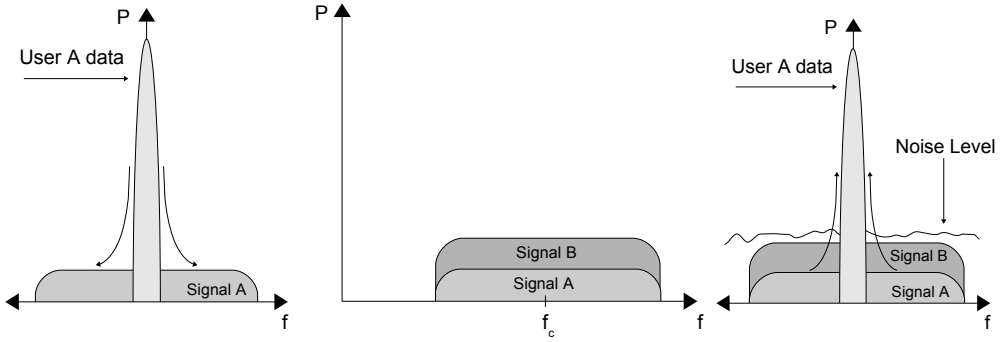


Figure 2.2: Despreading for user A, using signal created in Fig. 2.1

point-of-view the terms "spreading" and "despreading" become more apparent (as seen in Fig. 2.3). High-frequency codes (if long enough), look similar to band limited white noise. When the narrow band user data is mixed with this code, the narrow band data is spread over the bandwidth of the code as seen in Fig. 2.3(a). This signal now contains information about the user data. Shown in Fig. 2.3(b) are two superimposed user signals that are mixed to RF (modulated signals). After demodulating to baseband, the user code is mixed with this signal which causes information about the user data to appear out of the noise. Passing this signal through integrate- and compare-functions cuts off unwanted noise- and high-frequency components. A reconstruction of the user data is then produced. As seen in Fig. 2.3(c) the integration causes the user data to be recognizable above the noise level. The more users or noise in the CDMA system, the higher this noise level will be. System capacity will be limited by this noise level, depending on the acceptable bit error rate (BER).



(a) spreading (b) RF Signal (c) Despreading

Figure 2.3: A Frequency-domain representation of CDMA communication

2.2 CDMA Signal Detection

Any received signal in a CDMA system is spread according to some signature signal. Therefore, because they are spread according to some signal, they have similarity with the specific signature signal. In a system where these signature signals are designed to have little similarity among them, correlation functions are performed using a specific spreading signal to detect a specific user signal. The correlation function output is then evaluated by threshold detection (as seen in Fig. 2.2) to recover the user signal. The correlation serves a two-fold purpose by first attempting to increase the wanted signal SNR and then by filtering out noise. Some of the most basic correlators are the sliding correlator and the matched filter correlator.

Correlation

Firstly, the mathematical formula for the correlation of two time-domain signals is defined as:

$$R_{xy}(t) = \int_{\tau \to -\infty}^{\tau \to \infty} x(\tau) y^*(t+\tau) d\tau, \tag{2.1}$$

with t being the lagging time shift of one of the signals. This equation tells us that for correlation, both signals needs to be evaluated at τ, multiplied and averaged. Here it is important to note that the correlation output will differ with the varying time shift t. For user signal recovery, the maximum values of R_{xy} are of interest.

The sliding correlator is a very direct implementation of the last mentioned correlation equation, where other techniques essentially do the same in a more subtle manner. As seen in Fig. 2.4 two discrete single-bit sequences can be multiplied together by converting

the binary sequences to non-return-to-zero (NRZ) or bi-polar values ($0 \rightarrow 1$ and $1 \rightarrow -1$), as defined in the 3GPP specification [13]. The multiplication results are all accumulated into some register so that this accumulation result will increase where bits in a sequence are the same and decrease where the bits differ. As a correlation result, an averaged value is dumped by the accumulator when all bits in a sequence have been multiplied together.

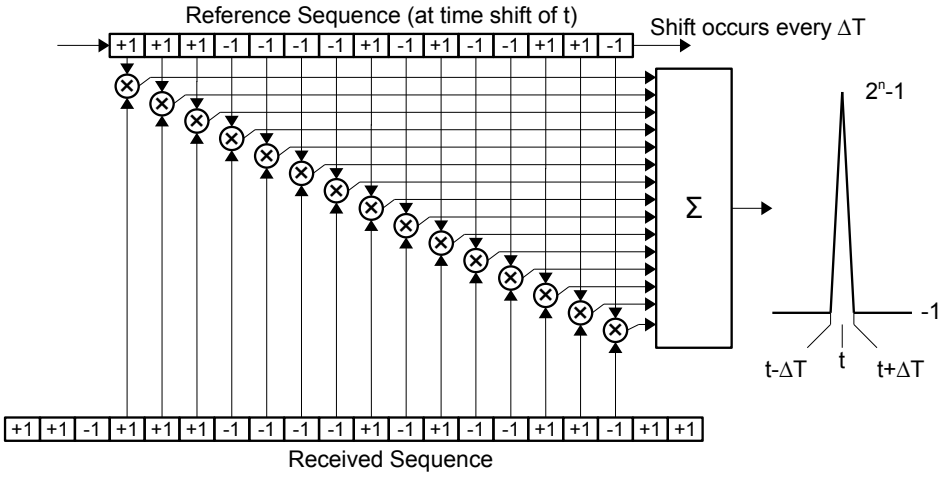


Figure 2.4: Correlation method generally used for the correlation of two single-bit sequences. The correlation is done for a sequence with good auto-correlation properties.

The matched filter is a digital filter implementation where filter coefficients are set to match an expected incoming signal. The filter output is a comparison of the received signal with filter coefficients. This output is then accumulated and evaluated in a way similar to the sliding correlator. With a matched filter $h(t)$ it is possible to implement the filter response as a time-shifted (T) and time-reversed ($-t$) version of a template signal (ϕ) as

$$h(t) = \phi(T - t).$$

Correlation is then performed between the filter response function and received signal (x) as follows:

$$R_{x\phi}(t) = \int_{\tau \rightarrow -\infty}^{\tau \rightarrow \infty} x(\tau)\phi^*(T - t + \tau)d\tau, \tag{2.2}$$

where aligned correlation is possible via shifted filter coefficients so that $t = T$ and

$$R_{x\phi}(T) = \int_{\tau \to -\infty}^{\tau \to \infty} x(\tau)\phi^*(\tau)d\tau. \tag{2.3}$$

Here $R_{x\phi}$ is expected to have its maximum value.

Synchronization (Phase Detection)

Typical wireless cellular environments have stationary transceivers and mobile devices. Mobile devices generally vary their position relative to the stationary transceivers and direct communication occurs between stationary transceivers and mobile devices. When using CDMA methods in communication, a synchronized environment is desired to minimize interference in such an interference limited system. Although synchronized transmission signals are transmitted from the stationary transceiver to mobile devices (downlink), added interference is caused by multiple path signal reflections and signals from nearby stationary transceivers. In the uplink, mobile devices may attempt to gain access to the wireless cellular network at any time and these devices may transmit data at any time. Therefore, a signal transmitted from the stationary transceiver requires synchronization at the mobile device and signals transmitted by the mobile device require synchronization at the stationary transceiver.

In Fig. 2.1 and Fig. 2.2 the different codes are regarded as in-sync with the user signals. If the user signal or code is delayed in relation to the other, the despreading operation will have a totally different outcome. The despreading will only deliver the desired output signal when the code and user signal are in synchronization. In SS systems the receiver should therefore be able to estimate these time differences of incoming user signals in relation to codes stored at the receiver. This synchronization process is also often referred to as phase acquisition.

In general, synchronization is partially performed by correlation of an incoming signal with a stored code (see Section 2.2). Correlation allows us to determine, with a high degree of accuracy, whether the code and signal are aligned. Correlation is followed by threshold detection to determine the degree of signal similarity. The process is repeated with the same code that is shifted in relation to the incoming signal, until the code and signal are aligned (in correlation).

The correlator design is often the determining factor of how fast a system can acquire a signal and how much interference a system can tolerate. Basic correlators can be used, but more advanced synchronization algorithms deliver more complex solutions to speed up the synchronization process [14].

Rake Receivers

Generally transmitted signals follow various paths towards a receiver because of signal reflections. This causes multiple signals from a single source to be received at different time instances.

To maximize received signal SNR, these multiple paths are also utilised as opposed to using only the strongest signal path or first acquired signal path. In a correlation function output, relatively large values are considered and generally referred to as "fingers". A receiver that detects multiples of these fingers and performs combined correlation is known as a rake receiver. Such a receiver performs delay acquisition for different fingers and incorporates them to produce a maximum SNR for threshold detection. The rake receiver therefore needs to synchronize the significant multiple signal paths to the codes stored at the receiver. This process is also commonly referred to as channel estimation. A typical rake receiver is presented in Fig. 2.5. Chapter 5 of this thesis is dedicated towards the

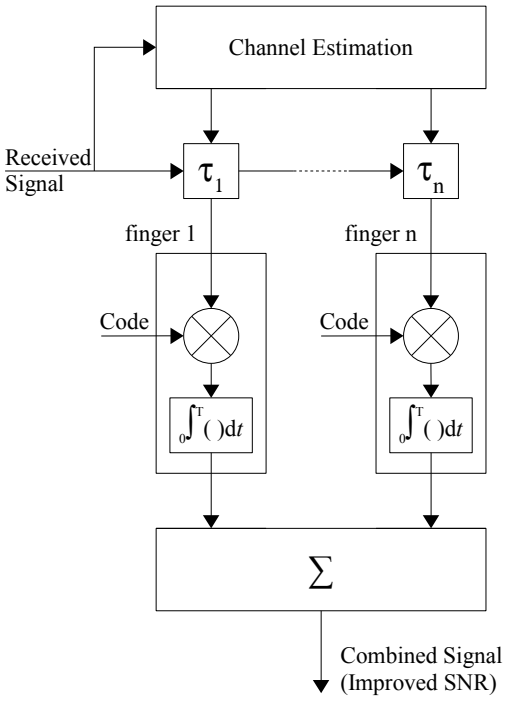


Figure 2.5: Rake receiver structure

design of an RSFQ system that rapidly detects all possible multiple signal paths. The rake receiver then uses the strongest signal paths according a programmed threshold algorithm with maximum ratio combining (MRC), generally referred to as the "searcher" [15].

2.3 CDMA Code Sequences

Wireless cellular CDMA systems all make use of both PN and orthogonal code sequences. These sequences are used to spread a data signal to a wider bandwidth and inherit the properties of the sequences. Spreading is done by simply mixing the data signal with the code sequence. The data signal can be fully recovered by mixing a spread signal with the same sequences, followed by integration (as mentioned in Section 2.1). When multiple data signals are spread (each with an unique sequence or sequence combination) and superimposed in the same frequency band, data can be recovered as mentioned, but here the relation between the different codes will influence the recovered data integrity. This is because the multiple spread signals interfere with each other when superimposed (interference because of non-orthogonality between signals). This is generally referred to as multiple access interference (MAI). The amount of this interference can be kept to a minimum by using sets of codes with certain properties. Two types of codes are discussed, each having their advantages and disadvantages for use in SS systems. In CDMA systems it is desired for codes to have good auto-correlation and cross-correlation properties. As shown in Eq. 2.1 for continuous time signals, cross-correlation R between two fixed length discrete signals x and y can be defined as [16]:

$$R_{xy}(j) = \sum_{n=0}^{N} x(n)y(n-j) \tag{2.4}$$

With N equal to the sequence length and j the lagging time shift of one of the sequences. Auto-correlation is defined in Eq. 2.5 and can also be defined as the cross-correlation of the sequence with a time shifted version of itself.

$$R_{xx}(j) = \sum_{n=0}^{N} x(n)x(n-j) \tag{2.5}$$

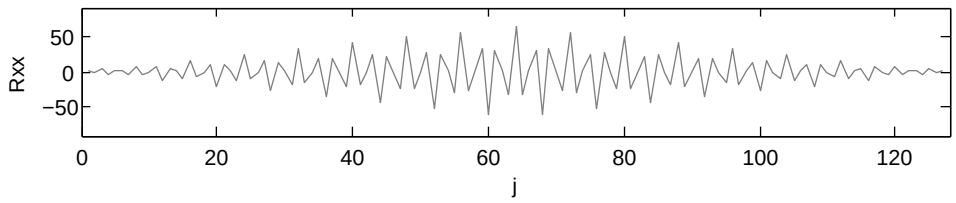
Ideal correlation properties for a set of codes used in a CDMA systems are that R_{xy} should be zero for all values of $j \in \{0..2N\}$ and all combinations of codes in the set except where $x = y$. In addition to this R_{xx} should be zero for all values of $j \in \{0..N-1, N+1..2N\}$ with a high peak at $j = N$ (where $x(n)$ is in correlation with the time shifted). These cross-correlation properties are to minimize interference between users and the sharp peak in auto-correlations is desired for effective signal phase detection in asynchronous CDMA systems.

CDMA system codes are generally defined as either orthogonal or non-orthogonal. Different types of codes were evaluated along with code usage in modern communication

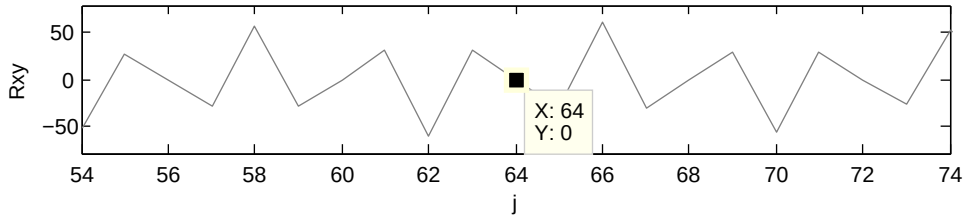
systems.

2.3.1 Orthogonal Codes

Orthogonal codes have the property that for a given set, all cross-correlations R_{xy} are zero at $j = N$, except when $x = y$. Walsh codes are an example of orthogonal codes. Orthogonal variable spreading factor (OVSF) codes (based on Walsh codes) are an example of a set of varying length orthogonal codes that are widely used in modern communication systems [15]. These codes have relatively high R_{xy} values for $j \neq N$ and lack a single sharp peak in R_{xx} values (as seen in Fig. 2.6(a)). They are an excellent choice to provide channel insulation in a CDMA environment, but when used in an asynchronous system, synchronization is very difficult because of auto-correlation properties. Cross-correlation properties clearly show that codes are only orthogonal to each other when in synchronization with each other. For this reason, all users using a specific set of Walsh codes in a CDMA system first have to be synchronized by some other means before communication can be established. There is also a very limited set of Walsh codes available for certain spreading factors. Examples of auto- and cross-correlations are given in Fig. 2.6. Note that for two Walsh code sequences of 64 bits they have zero cross-correlation at $j = 64$. This is true for all combinations of any two Walsh sequences. Fig. 2.6(b) shows a single case of cross-correlation with relatively large values.



(a)



(b)

Figure 2.6: Typical Walsh code (a) auto-correlation and (b) cross-correlation properties

2.3.2 Non-Orthogonal Codes

A wide variety of non-orthogonal codes with varying auto- and cross-correlation properties have been developed for communication purposes. Gold codes are an example of such codes. They are formed by the combination of two maximum length sequences (M-sequences). Gold codes show good, but non-ideal cross-correlation properties. They show single and sharp R_{xx} peaks which are required for synchronization. Fig. 2.7 shows the typical auto- and cross-correlations from a set of 129 gold codes each with a length of 128. Simulations also showed that second highest R_{xx} values are well below the sharp peaks found in the R_{xx} of each code The maximum R_{xy} values of all possible combinations between two codes from the set of 129 are seen in Fig. 2.7(c) and show that cross-correlations are more-or-less stable with no large variations in maximum values. This implies that a synchronization process should not suffer drastically from peaks produced by cross-correlations.

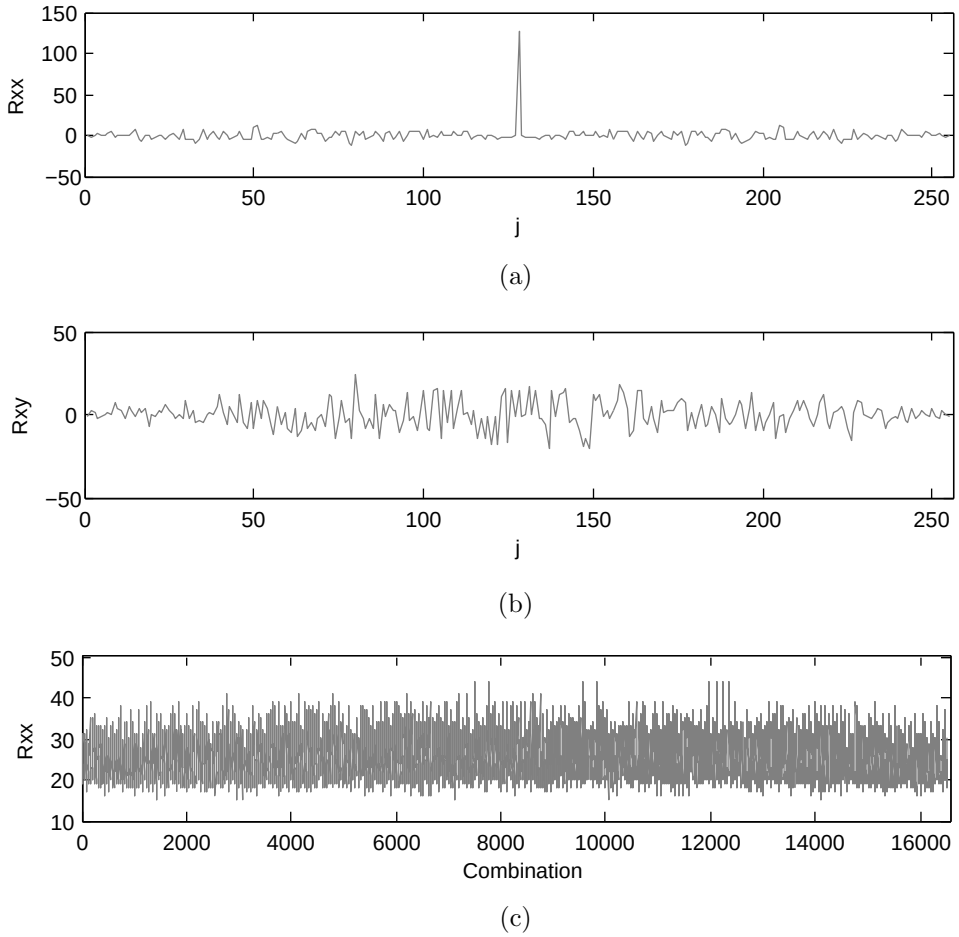


Figure 2.7: Typical Gold code (a) auto-correlation and (b) cross-correlation properties

2.4 Modern CDMA based Standards

When designing a CDMA system, typical modern CDMA protocols and standards are examined first. 3G mobile telecommunications consist mainly out of two standards, namely Universal Mobile Telephone System (UMTS) and CDMA2000. Fig. 2.8 shows these standards along with the radio access technology (RAT) they each use. UMTS is a 2G/3G

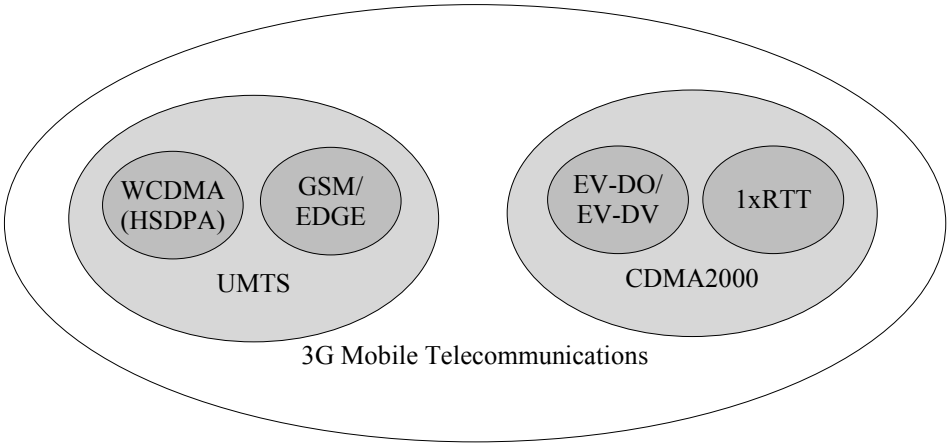


Figure 2.8: 3G Mobile Telecommunication Standards and RAT

protocol of mobile telecommunication standards that is widely used in European countries and South Africa [17]. Deployments can also be found in North America and some Asian and Pacific countries [17]. In UMTS there are two different types of RAT. The first is the Wideband-CDMA (WCDMA) 3G standard. The second is an enhanced 2G GSM system referred to as GSM/EDGE radio access network. CDMA2000 is a similar protocol widely used most Asian, Pacific, African and American countries [18]. CDMA2000 use CDMA based standards like 1xRTT, EV-DO and EV-DV that are in many ways similar but incompatible with WCDMA.

In this thesis a basic understanding of the UMTS WCDMA RAT is obtained and a simplified CDMA communications model is produced, incorporating only some parts of the WCDMA standard which are relevant to this research. Aspects like power control, soft-handovers and RF modulation techniques are outside the scope of the thesis.

2.4.1 Basic UMTS Network Description

In the UMTS network, 2G and 3G type transceivers and controllers are different and link to the core of the cellular network. Different terms are therefore used to describe each

of these components. Fig. 2.9 show these components and different ways to access the

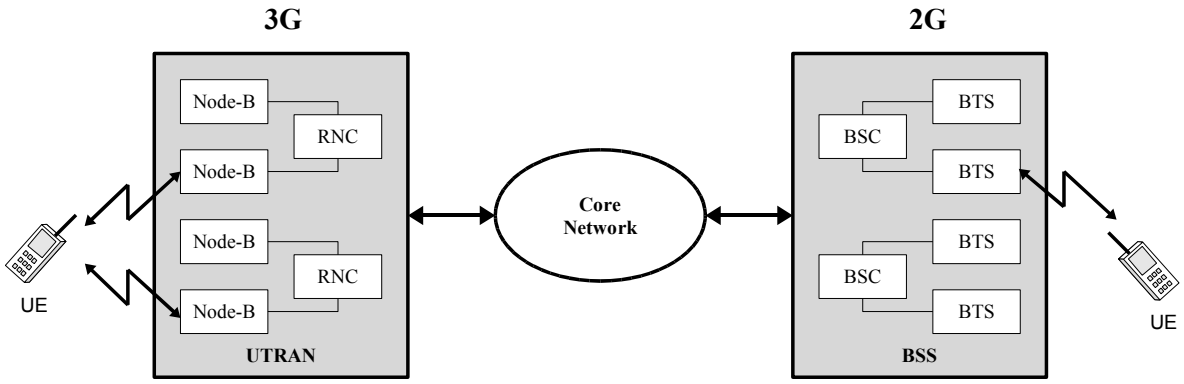


Figure 2.9: UMTS network architecture

core network. In 2G implementations a base station subsystem (BSS) consists of multiple base station controllers (BSCs) that each control a number of base transceiver stations (BTSs). In the same way the UMTS terrestrial radio access network (UTRAN) describes the 3G link between user equipment (UE) and the core network. Multiple radio network controllers (RNCs) each control a number of 3G transceivers, termed Node-B.

In a WCDMA system, all channels have a rate of 3.84 Mbps after spreading and scrambling. These channels are multiplexed onto channels with a 5 MHz bandwidth. To allow for filter roll-off and therefore lower inter-channel interference, not the whole channel bandwidth is used.

In general, the uplink refers to the telecommunication link from the mobile device (UE) to the stationary base station (BTS or Node-B). The downlink refers to the link from the base station to the mobile device.

2.4.2 Code Usage

Orthogonal and non-orthogonal codes both have unique properties that are required for effective asynchronous CDMA communications. These codes are therefore generally used together to gain the benefits of both. The orthogonal codes are used to separate channels from each other and are termed channelization codes. Orthogonal code sets are limited and code reuse is desired. Orthogonal code reuse is achieved by using non-orthogonal codes (scrambling codes) to scramble sets of channels that are channelized by orthogonal codes. These non-orthogonal codes then also provide a means for synchronization (phase acquisition).

Two terms are important for the mixing of codes with user data. These are:

1. The spreading factor (SF) - A term that determines the data transmission rate. This factor is determined by the channelization code length used per user data bit.

2. The processing gain (PG) - This figure defines the scrambling code length used per user data bit.

In the older IS-95 CDMA systems, $SF = PG$, but in more advanced CDMA standards like WCDMA, $SF \leq PG$. The lower SFs are made possible by the OVSF code set and enable variable data rates that can be adjusted according to user need or system load.

Typical downlink channelization and scrambling operations [13] are shown in Fig. 2.10. The operations are only shown for dedicated physical data and control channels

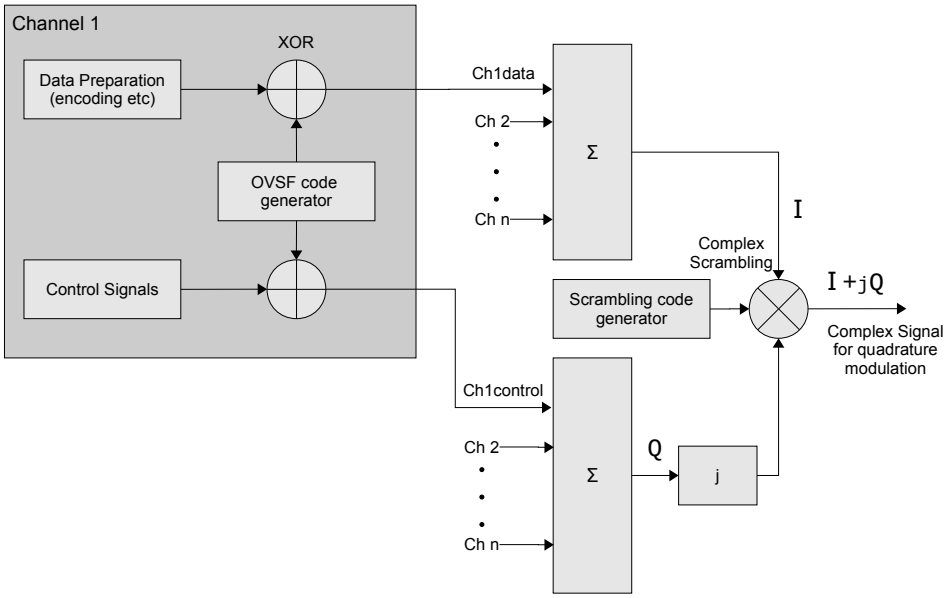


Figure 2.10: Channelization and scrambling of WCDMA user data and control channels

(DPDCHs and DPCCHs). Many other channels exist, each with specific purpose and characteristics [15]. In this thesis the focus is directed towards dedicated physical data channels. The proposed areas of superconductor application (discussed in Chapter 5) are applicable to all channels that require correlation and phase acquisition.

A code allocation example is shown in Fig. 2.11. Here it is seen how a set of channelization codes (OVSF codes) can be spread by the same scrambling code (SC) in the downlink, because all channelization codes are in synchronization. SCs therefore differ in the downlink of separate Nodes-B to allow code reuse. In the uplink, channelization codes of separate UE are not in synchronization. Therefore, different UE use the same channelization codes in the uplink, but different SCs. An example of Node-B downlink

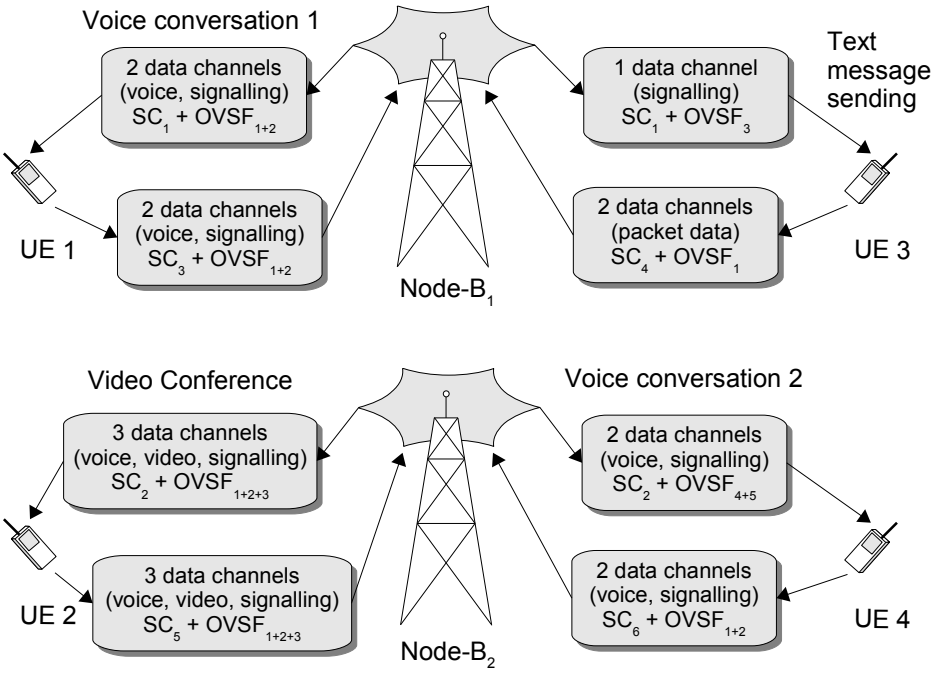


Figure 2.11: An example of WCDMA code allocations

SC assignments by the RNC is shown in Fig. 2.12. Different SC sets are used in the uplink and downlink [13].

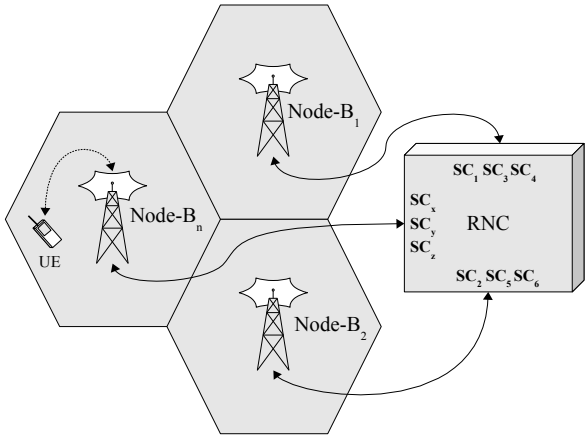


Figure 2.12: Example of RNC assigned Node-B scrambling codes

2.5 Modelling of a simplified WCDMA Channel

For this study of superconductor applications in a wireless cellular environment, the focus is on the uplink channel where the receiver is implemented in the BS. A simplified baseband channel model is presented along with models for signal detection and channel estimation.

2.5.1 Uplink signal generation

The signal input to the uplink WCDMA Node-B receiver is modelled as follows:

- User data from higher WCDMA layers consist of user data along with error correction coding. This data is modelled using random binary numbers generated by the Bernoulli distribution.

- Multiple data and control channels of a single user are separated by the use of OVSF codes in the uplink [13]. These channels are then all scrambled by a specific scrambling code given to each user. The model simplifies the coding implementation by implementing a single data channel per user that is only scrambled (and therefore also spread) by the unique scrambling code given to each user.

- According to specifications [13], either long or short scrambling sequences may be used for the scrambling of a physical data channel. By using long scrambling sequences the scrambling code changes with each symbol (different phase of the long scrambling sequence) and different initial phase offsets are assigned to users so that no users will use the same phase of the scrambling sequence. With short scrambling sequences, each user is assigned a fixed code with a length of 256. The configuration of such long and short code generation can be seen in the 3GPP technical specification [13]. Long scrambling sequences are used in this model. These long sequences are Gold sequences using m-sequences with the polynomials: $X_{25}+X_3+1$ and $X_{25}+X_3+X_2+X+1$. This results in a long sequence with 16777232 chips, where a *chip* is defined as a single symbol of the scrambling code.

- 8 data channels are present in this model. These channels all have arbitrary time delays as UE may transmit to the BS at any given time. UE signals may follow multiple paths to the receiver, therefore a single user signal is also modelled as multiple channels with different delays using the same data and scrambling code. The channels are organized as follows:

  - One channel uses a data sequence of only 1's. All other channels use random data as described.
  - One channel is used to produce three paths each with a different delay. This is to simulate multi-path propagation for one of the users
  - Six other user channels are added for the addition of multiple access interference (MAI) into the model.

- Additive White Gaussian Noise (AWGN) is added to the model for different SNR and BER evaluations. This models the MAI in the system.

The model for the different channels is shown in Fig. 2.13. Channels 3 to 8 have the same structure, therefore only channels 1 to 3 is shown. AWGN is also omitted in the figure.

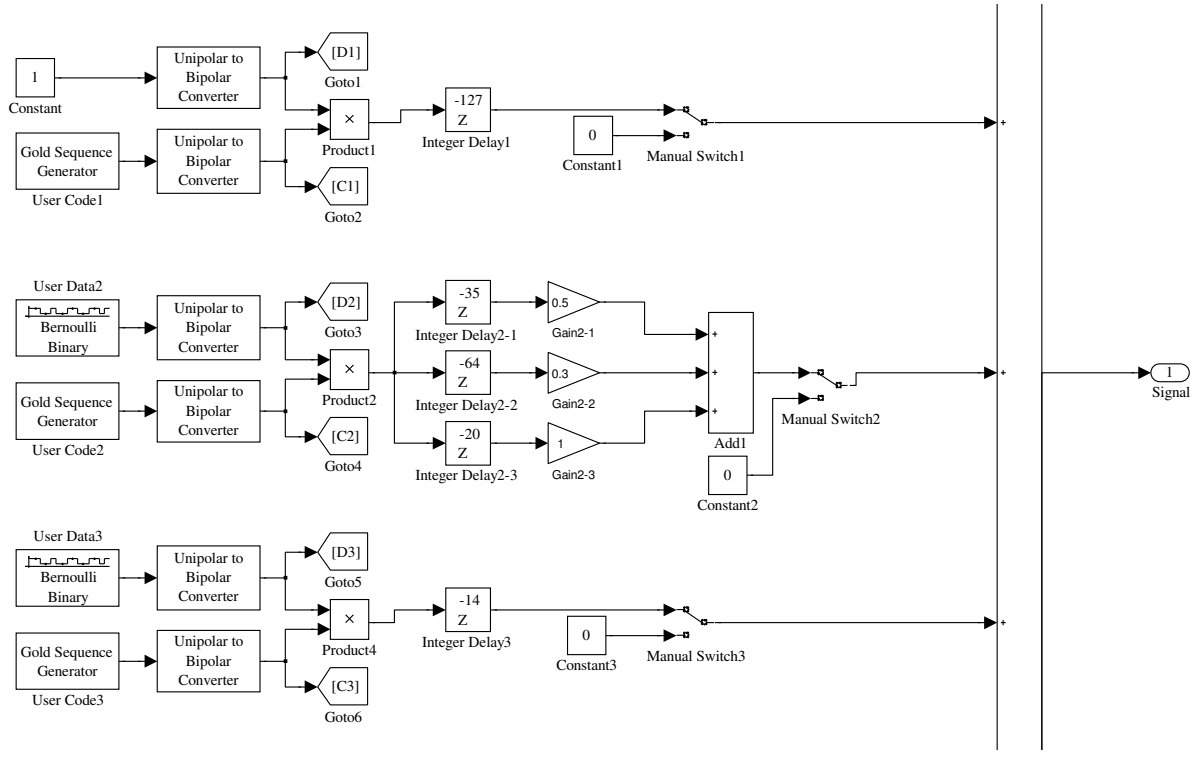


Figure 2.13: Model for WCDMA signal generation

2.5.2 Path Estimation

Correlation is used to determine phase differences between user signals and stored code. The estimation model is set to determine the delays added to the user channels as seen

in Fig. 2.13. The estimation model is presented in Fig. 2.14 and consists of the following components:

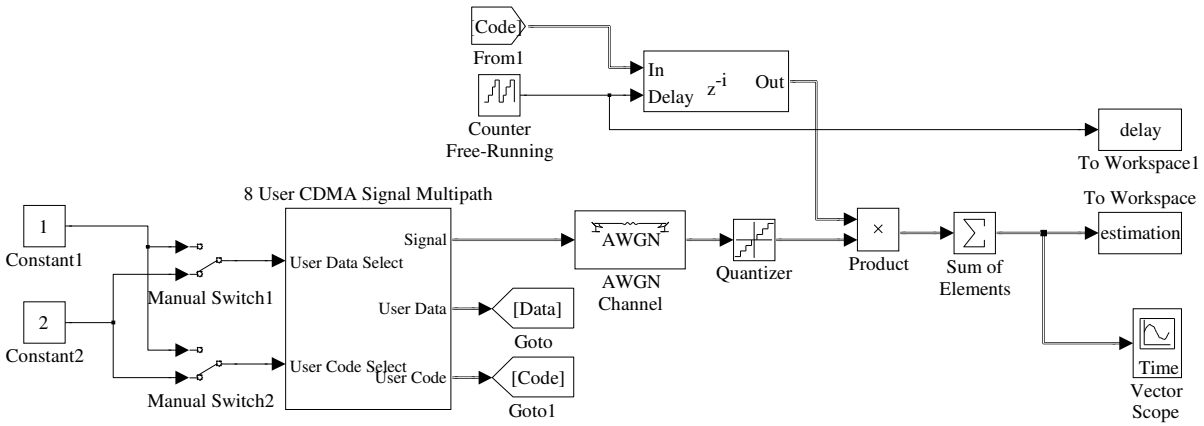


Figure 2.14: A simple CDMA channel estimation model

- Selection switches to obtain specific user data and code
- Signal generation model with added noise (AWGN) and quantizer
- A multiplier used for the first step of correlation. The bi-polar input signal is multiplied by the NRZ despreading code. This code is an inversion of the spreading code in order to produce positive correlation peaks for binary ones (user data before spreading) and negative peaks for binary zeros.
- A variable delay, incremented each time a correlation is completed for a specific code delay. This delay cycles through all possible phase shifts between code and incoming data. One cycle therefore leads to a complete correlation result, revealing all possible signal path components and other interfering components.
- An accumulation function (Sum of Elements) which accumulates all data in a predefined frame. The frame contains one scrambled symbol. The accumulation effectively increases the SNR of the spread signal, revealing a result dependent on the input data symbol. With the retained code shifting, the accumulator results are used to obtain 'pictures' of correlation component magnitudes in relation to code delays.

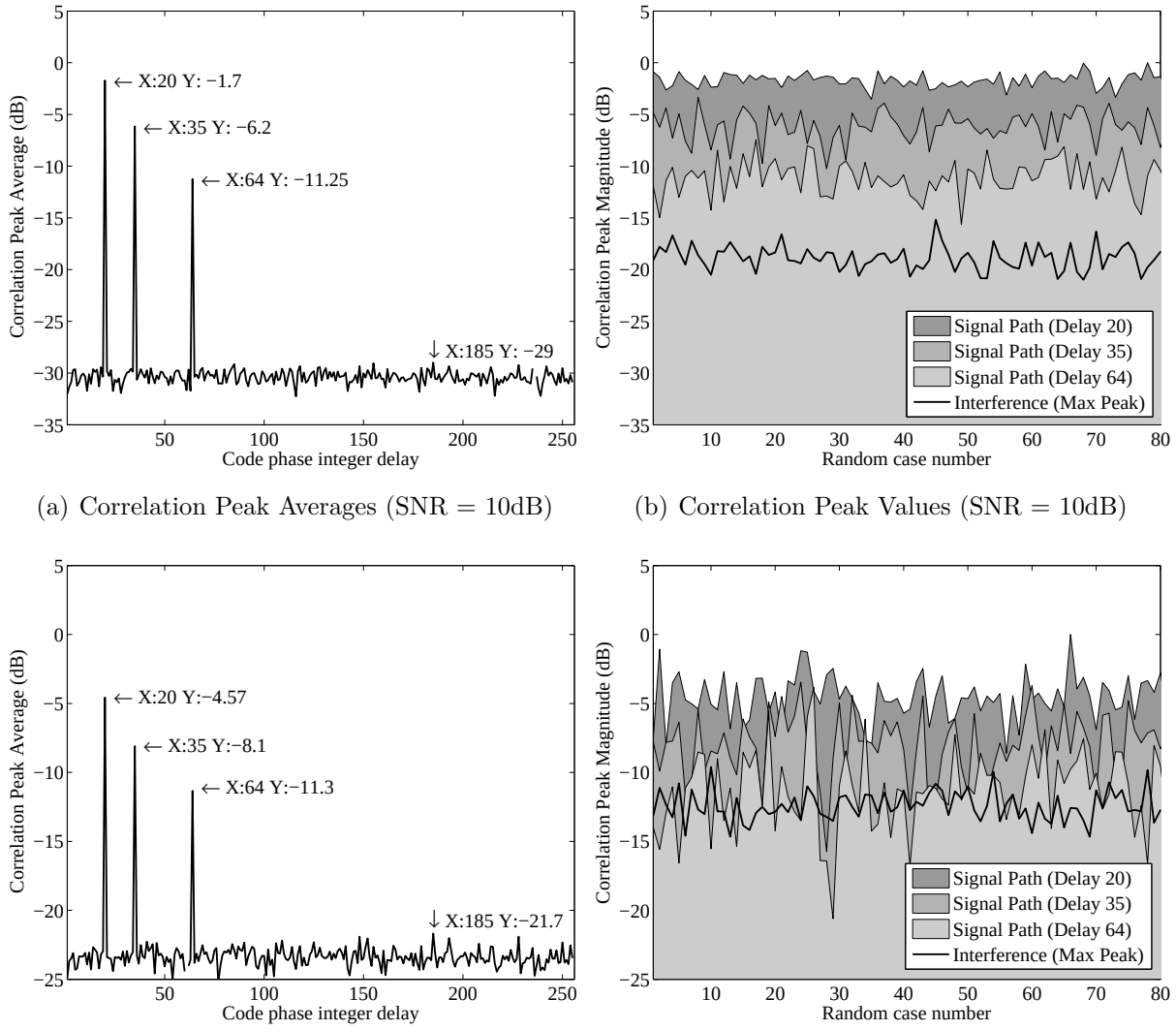
To demonstrate estimation of multiple path signal component delays, the model is set to use a single user signal with multiple paths. As a basic evaluation of the estimator

model Fig. 2.15 is presented to show how correlation produces detectable multiple path components at different delays. In Fig. 2.15 (a) and (c), the average values of correlation components are produced at each possible phase shift of the despreading code. These averages are computed for 80 different cases where different spreading codes are used for each case. Fig. 2.15 (b) and (d) show the specific correlation values produced for each of the different cases. These values are produced for each multi-path component and in addition maximum interference correlation values of each case are added. These figures show signal path components related to interference in the system. These figures are produced having different SNR values (by changing the AWGN component) to demonstrate how estimation is affected by MAI. The three multi-path components are clearly marked at delays of 20, 35 and 64 respectively. A single level threshold is used to to detect if correlation components are classified as a signal path component or interference component. According to dynamic range requirements for such a single level detector (as discussed in Appendix A.1), the signal path correlation component is desired to be at least 6.02 dB above the highest interference component. In Fig. 2.15 it can be seen that high SNRs in a multi-path environment meet such requirements. As SNR deteriorates, some signal path components can not be distinguished from maximum interference components.

In a rake receiver it is desired to combine multiple signal paths to produce a larger SNR than when using only one signal path. When signal path components are close to interference components, the addition of such components could actually introduce more noise into the system than signal power. Therefore, not all signal path components are beneficial when a rake receiver is used and path selection is an important aspect in such a receiver. In Chapter 5 multiple path identification with superconductor electronics are covered. Signal path and threshold selection techniques are not within the scope of this thesis

2.5.3 Despreading and Data Recovery

After multiple data paths are detected, data recovery can be done via the despreading process. For the evaluation of the CDMA system performance in the presence of MAI, a data recovery model is presented with AWGN and additional user signals added. The data recovery model is similar to the estimation model and is presented in Fig. 2.16. Here time delays for the despreading code are kept at the estimated phase shifts and the correlation output is simply tested according to its sign (negative correlation output values imply zeros and positive correlation values imply ones). Added to the model is an error rate calculation component, used for BER analysis. The recovered user data BER is evaluated



(a) Correlation Peak Averages (SNR = 10dB)

(b) Correlation Peak Values (SNR = 10dB)

(c) Correlation Peak Averages (SNR = -10dB)

(d) Correlation Peak Values (SNR = -10dB)

Figure 2.15: Simulation results for an estimation model where multiple signal path components are evaluated in relation to interfering correlation components.

by varying the amount of MAI. A Monte Carlo analysis is performed for each level of interference. The BER is averages calculated for 10^5 random user data and spreading code combinations. The BER is therefore limited to 10^{-5}. The BER results are presented in Fig. 2.17 and show how user data can be recovered from an environment where noise levels (MAI) are much greater than the spread user signal. BER curves are calculated for a 8-user system and 16-user system to evaluate the performance degradation caused by added users. The performance of CDMA clearly degrades when more users are added to the system. When the amount of AWGN is reduced (SNR increased), the BER increase per user can be obtained.

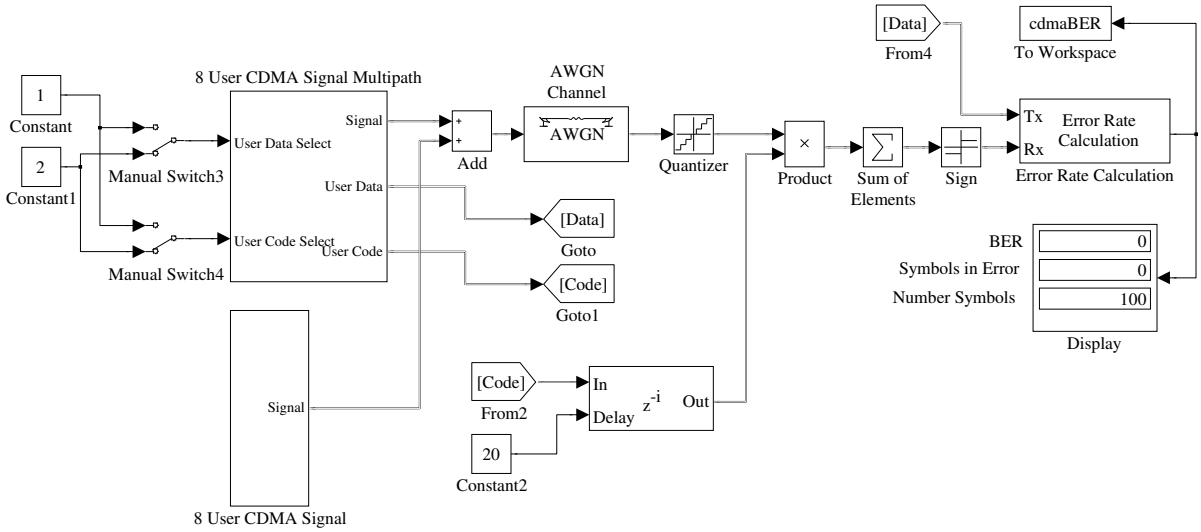


Figure 2.16: Model diagram for simple WCDMA system data recovery and analysis

2.6 Conclusions

This chapter introduced basic CDMA concepts and techniques. Some of the popular CDMA-based standards and architectures were presented and discussed. The popular WCDMA RAT was then explored on the physical layer before a simplified WCDMA model was presented and evaluated to study the estimation of multiple signal paths and effects of MAI.

With the basic understanding of modern wireless cellular network components and CDMA based communications, the basics of RSFQ superconducting electronics are presented in the following chapter before discussing the applications of superconductors in wireless systems.

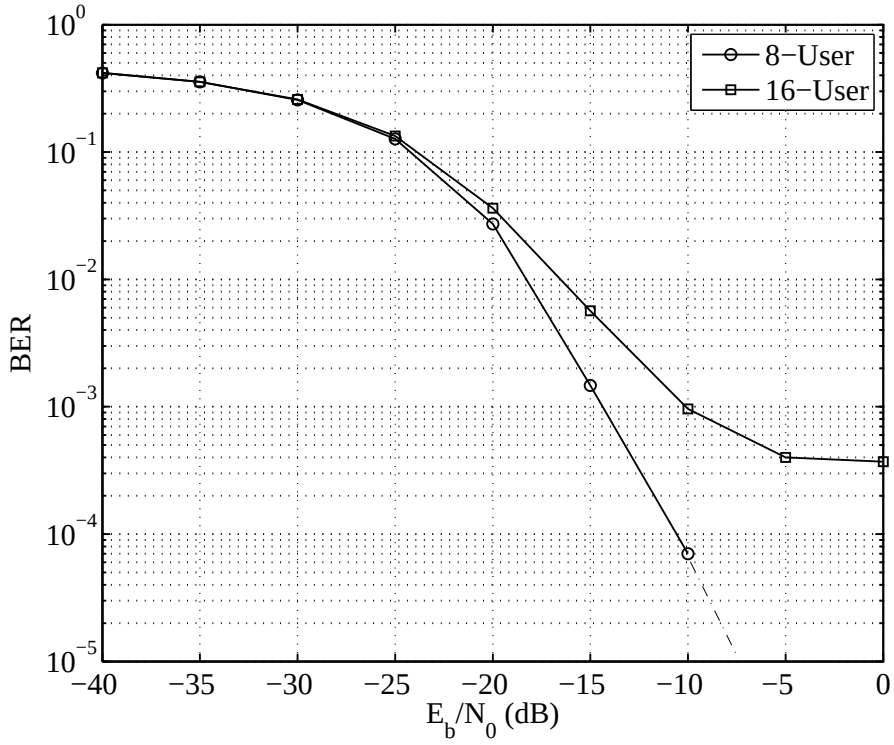


Figure 2.17: BER results for a simple WCDMA based multiple access model with PG=256

Chapter 3

RSFQ Circuit Building Blocks

3.1 Introduction

All superconducting components in this thesis are designed for low-temperature superconductor (LTS) implementation using RSFQ logic. This is done to explore the advantages of a rapidly pulsed logic in wireless communication systems.

The RSFQ logic family was introduced in 1985 [19] and since then developments on these circuits have increased considerably. There are numerous research opportunities in different RSFQ applications and an increasing number of companies are utilizing the benefits that these applications have. The logic is based on the use of a Josephson junction with a resistive element in parallel [20]. Such a resistively shunted junction can then produce a voltage pulse because of the Josephson Effect [20]. RSFQ circuits operate with current pulses. Such a pulse is known as an SFQ pulse, has a width of a few picoseconds and has an area (voltage integrated over time) of a single magnetic flux quantum (Φ_0). In RSFQ circuits these pulses are generated, memorized, passed and reproduced. The presence of an SFQ pulse within a certain clock period would represent the binary 1 while the absence of such a pulse represents a 0.

This chapter contains details of how the junction model is derived for a certain fabrication process along with the evaluation of existing RSFQ cells and presentation of new RSFQ cells. A few useful configurations of cells are also presented. All electrical circuit simulations are done with WRspice [21].

3.2 Josephson Junction Model

Josephson junctions are superconductive devices that show non-linear behaviour. They act as an inductive conductor with zero resistance when operated in a certain region and mainly as a resistive element when operated in another region. This is explained by first introducing a JJ model generally used for RSFQ logic circuits [20]. This model is known as the resistive capacitive shunted junction (RCSJ) model, shown in Fig. 3.1. The current

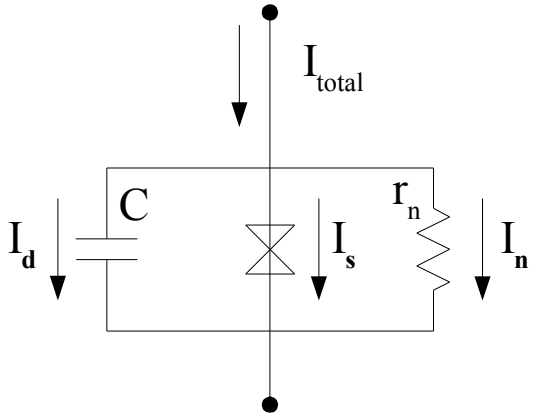


Figure 3.1: Schematic circuit of the RCSJ JJ model

contributions to the total current flowing through such a junction can be expressed as:

$$I_{total} = I_s + I_n + I_d \tag{3.1}$$

Where I_s is the lossless DC current that can flow through the JJ itself. This current is limited to the critical current of the junction (I_c) and is also dependent on the voltage over the JJ (see [20] for mathematical details). I_c is determined by the critical current density (J_c) and the area (A_J) of the junction so that:

$$I_c = J_c A_J \tag{3.2}$$

When using a commercial fabrication process, J_c is obtained from the process specifications. In the layout procedure, only the area of the junction is changed to get different junction I_c values. JJs are also inherently inductive. This inductance is modelled as a linear inductor where $I_s \ll I_c$, as seen in Eq. 3.3. Closer to I_c the inductance has a dependence on the change in flux through the junction [20].

$$L_{J0} = \frac{\Phi_0}{2\pi I_c} \tag{3.3}$$

The I_n current in Eq. 3.1 is associated with the normal current flow in a JJ. Commercial fabrication processes specify a constant voltage ($V_n = I_c R_n$) [22] whereby shunt resistance values vary depending on I_c.

Parasitic capacitance in a JJ structure is generally unavoidable. This effect is represented in the RCSJ model by a shunt capacitance. Current flowing in this branch is referred to as the displacement current ($I_d = C_d \frac{dV}{dT}$). This capacitance affects the switching speed of RSFQ logic circuits.

Josephson junctions have a few important parameters that vary with the use of different superconductors and different fabrication processes. Here the JJ model is discussed on which all circuit simulations in this thesis are based. Presented in Table 3.1 are the junction parameters of Hypres' 4.5kA/cm^2 Nb/AlO$_x$/Nb fabrication process. Table 3.2

Table 3.1: Typical junction parameters of Hypres' 4.5kA/cm^2 fabrication process

Parameter	Value
Gap voltage (V_g)	$2.5 \pm 0.1mV$
Normal Resistance Product ($I_c R_n$)	$1.3 \pm 0.2mV$
V_m	$13 \pm 2mV$
R_{sg}/R_n	10 ± 1

presents the WRspice model parameters with a description of each. The values in Table 3.1 are then used to create a WRspice JJ model for a specific fabrication process. This model is named "jj45". Here I_c is scaled according to Eq. 3.2. Parasitic capacitance C_d is calculated according to Eq. 3.4 and Eq. 3.5 as seen in the Hypres design rules [23].

$$C_s = \frac{1}{21.5 - 4.3 log_{10} J_c} \quad (pF/\mu m^2) \tag{3.4}$$

$$C_d = \frac{I_c}{J_c} C_s \tag{3.5}$$

Table 3.2: WRspice JJ Model Parameters - The parameters marked with an asterisk in the "Area" column scale with the area parameter given in the device line in WRspice

Name	Area	Parameter	Units	4.5 kA junction (jj45)
icrit	*	Junction critical current (I_c)	A	1.0×10^{-3}
cap	*	Junction capacitance (C_d)	F	1.5333×10^{-12}
rn	*	Normal state resistance (R_n)	Ω	1.3
r0	*	Subgap resistance (R_{sg})	Ω	13
vg		Gap voltage (V_g)	V	2.5
delv		Gap voltage spread	V	0.1×10^{-3}
rtype		Quasiparticle branch model	-	1 (Std. PWL Model)
cct		Critical current model	-	1 (Fixed Critical Current)

3.3 Josephson Junction Shunt Resistance Calculations

Josephson junctions form a response similar to that of an LCR resonator [20] with a resonant frequency of

$$\omega_0 = 2\pi f_0 = \frac{1}{(L_{J0}C_d)^{1/2}}, \tag{3.6}$$

and bandwidth (BW) related to the RC time constant, resonant frequency and quality factor (Q) as follows:

$$BW = \frac{1}{RC} = \frac{\omega_0}{Q}. \tag{3.7}$$

The quality factor can be expressed as

$$Q = \omega_0 R_n C_d = \frac{R_n^2 C_d}{L_{J0}}. \tag{3.8}$$

The Stewart-McCumber parameter (β_c) is more generally used in RSFQ circuit design instead of Q and is defined as follows:

$$\beta_c = Q^2 = \frac{2\pi I_c C_d R_n^2}{\Phi_0} \tag{3.9}$$

In RSFQ, junction response is desired to be as quick as possible without suffering from the negative effects of hysteresis. For this it is desired that the junction is critically damped ($\beta_c = 1$). For $\beta_c > 1$ the junction is underdamped and with $\beta_c < 1$ the junction is overdamped [20]. Recent studies have shown that higher β_c values increase the junction switching speed without having a significant effect on circuit operating margins and yield

[24]. According to Eq. 3.9 the shunt resistance value has to increase significantly for small increases in β_c. Simulations have shown small gate delay decreases for an increasing β_c. Minor gains in potential clock speeds are acquired by using underdamped junctions [24]. In order to reduce layout size and keep layout simple, junctions are chosen to be critically damped with a $\beta_c \approx 1$. As seen in Table 3.1 the junctions made by this process have an intrinsic shunt resistance of

$$R_n = \frac{1.3mV}{I_c} \tag{3.10}$$

For these shunt resistance values, junctions are still well underdamped with a $\beta_c \approx 8$. Decrease in β_c is obtained by adding external shunt resistances. Fig. 3.2 shows the intrinsic shunt resistance values (R_n) along with the external shunt resistances required to get certain β_c values. Calculations can be seen in Appendix B.1. For this thesis all junctions are externally shunted to be critically damped according to Fig. 3.2.

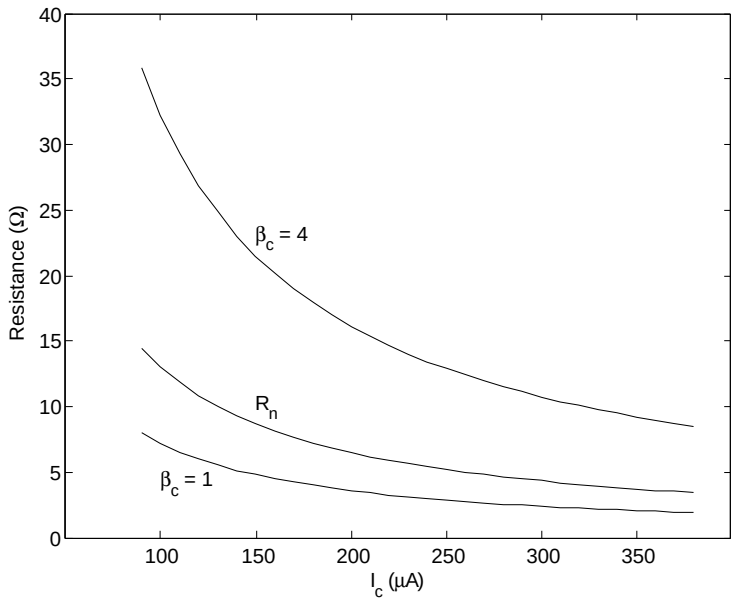


Figure 3.2: Intrinsic shunt resistance values (R_n) with the required external shunt resistances for $\beta_c = 1$ and $\beta_c = 4$. Values shown are all a function of I_c and specific for the HYPRES 4.5kA/cm^2 fabrication process.

3.4 RSFQ Cell library

All RSFQ cells used in this thesis are presented, described and analysed in this section. Basic circuit diagrams are shown along with their simulated circuit responses. Some existing cells from the University of Stellenbosch RSFQ cell library [25] and some new cells were implemented using Josephson junction models for the Hypres 4.5 kA/cm^2 [23] fabrication process. Cells in the library were originally designed for the Hypres 1 kA/cm^2 fabrication process and some changes in circuit components were necessary. This change in process mainly affects external shunt resistance values because of a change in junction characteristics. The inherently faster junction switching speeds have a minor but not negligible effect, since RSFQ pulses have different shapes and maximum amplitudes over inductive interconnects.

The expected yield of some new cells are calculated via Monte Carlo analysis as described by Fourie [25]. The yield of a circuit is defined as a percentage of the ratio y, where

$$y = \frac{N_{correct}}{N_{manufactured}}.$$

Here $N_{manufactured}$ indicates the number of circuits manufactured and $N_{correct}$ the number of manufactured circuits that show correct operation. The yield analysis method is based on the variation of all circuit elements that may result from a specific fabrication process. In a Monte Carlo analysis, the expected presence of an SFQ pulse is tested for in windowed periods of 20 ps. The expected absence of SFQ pulses are tested for in arbitrary window periods. Changes in circuit Monte Carlo yield figures for existing cells (by Fourie [25]) can be attributed to the difference in circuit speed or RSFQ pulse shapes. Examples of Monte Carlo analysis circuit files are presented in Appendix D.

The cell library description is started with the Josephson Transmission Line (JTL) followed by the DC-to-SFQ converter, Pulse Merger and Pulse Splitter. These are all asynchronous RSFQ components that are used for RSFQ pulse routing and RSFQ circuit interface. Logic cells used in this thesis are then presented. These are the inverter, AND gate and XOR gate. The Destructive Readout register (DRO) and asynchronous toggle flip-flops are then introduced and demonstrated. New toggle flip-flop variations that are required in this thesis are presented. The design of a DC-enabled JTL which allows RSFQ pulses to be passed or blocked depending on the input DC current polarity is also shown.

Detailed circuits which include all circuit elements along with parasitic inductances and damping resistances are shown in Appendix C.

3.4.1 SFQ Pulse Interface and Routing Cells

Josephson Transmission Line (JTL)

The Josephson transmission line is one of the fundamental circuits in RSFQ logic. It is generally used to connect other RSFQ cells while performing sharpening of RSFQ pulses [26]. The JTL is also used as a standard load for the optimization and testing of RSFQ circuits[25]. Simulation results for a series of interconnected JTLs are shown in Fig. 3.3. The simulation result is obtained by using the following circuit component values:

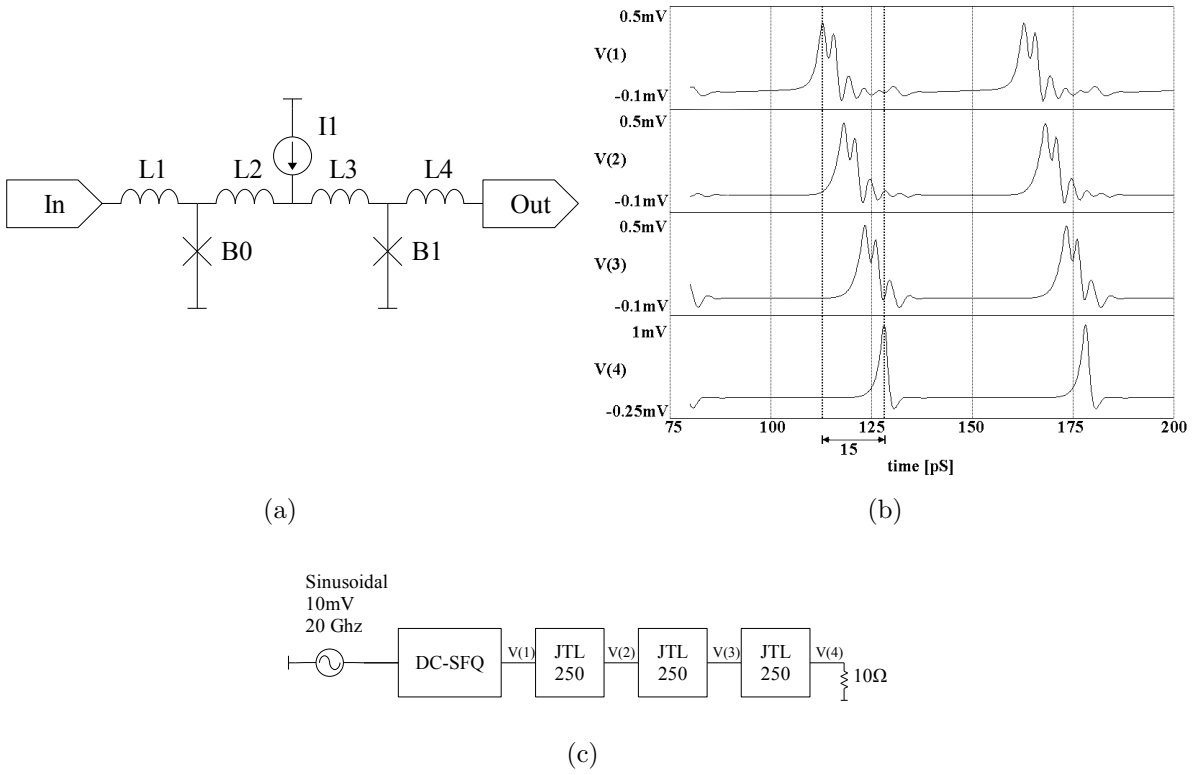


Figure 3.3: JTL (a) circuit details, (b) simulated responses and (c) simulation test setup

$B_{0,1} = 250\,\mu A$, $L_{1,2,3,4} = 1.98\,pH$ and $I_1 = 351\,\mu A$. This JTL is generally termed a $250\,\mu A$-JTL or a $250\,\mu A$-to-$250\,\mu A$-out JTL.

The simulation voltage pulses V(1) - V(3) in Fig. 3.3 may appear underdamped, but this is simply the effect of measuring voltages between the input and output inductances of the JTL. When observing current pulses through these inductances it is clear that the pulses are damped [25].

When connecting cells where the output/input JJ(I_{c1}) of the one cell differs from the input/output JJ(I_{c2}) of the other cell, junction overload may occur. This condition causes

SFQ pulse distortion and could lead to the input JJ not switching when a pulse arrives. Junction overload is considered below critical when $I_{c2} \lesssim I_{c1} \times \sqrt{2}$ and $I_{c2} > I_{c1}$[26]. Some cells with large input or output JJ I_c values therefore require that the $\sqrt{2}$ factor is brought under consideration. Therefore a special JTL is needed between cells where $I_{c2} > I_{c1} \times \sqrt{2}$. This JTL is designed for below-critical JJ overload with $I_{c2} = 250\,\mu A \times \sqrt{2} \approx 355\,\mu A$. Such JTL is termed a $250\,\mu A$-to-$355\,\mu A$ JTL. For the circuit shown Fig. 3.3 the component values are then as follows: $B_0 = 250\,\mu A$, $B_1 = 355\,\mu A$, $L_{1,2} = 1.98\,pH$, $L_3 = 1.16\,pH$, $L_3 = 0.82\,pH$ and $I_1 = 424\,\mu A$.

The complete JTL circuits with parasitic inductances and damping resistances are shown in Appendix C.

DC-to-SFQ Converter

The DC-to-SFQ converter serves as an link between room-temperature electronics and RSFQ logic circuits. These cells are used to provide clock pulses and data input pulses to an RSFQ circuit. This important cell produces an RSFQ pulse each time the input signal current rises above a certain level. It is reset when the current decreases below a certain threshold. For a sine wave input this cell produces a periodic train of SFQ pulses. The input specifications (10 mV into 28 Ω) are defined for a specific practical setup [25] and may need adjustment depending on the signal source. The circuit is shown in Fig. 3.4. The simulation result is obtained using the following circuit component values: $B_{0,3} = 171\,\mu A$, $B_1 = 245\,\mu A$, $B_2 = 148\,\mu A$, $L_1 = 3.35\,pH$, $L_2 = 1.29\,pH$, $L_3 = 1.13\,pH$, $L_4 = 1.74\,pH$, $L_5 = 2.11\,pH$, $L_6 = 1.27\,pH$, $L_7 = 3.59\,pH$, $L_{p1} = 0.69\,pH$, $L_{p2} = 0.29\,pH$ and $I_0 = 406\,\mu A$.

In relation to a positive input current (rising sine wave) through L_1, B_0 and B_2 are negatively biased by I_0 while B_3 is positively biased. The input current is also distributed between the branches containing B_0, B_2 and L_7, making the switching of B_0 and B_2 less likely with a rising input. When the input current rises above a certain level, the positively biased B_3 switches, producing an SFQ pulse that has little effect on B_0 and B_2, but causes B_1 to switch, producing an output pulse. Some of the bias current from B_3 is now diverted to the superconducting loop between B_0 and B_2. In this state the input is allowed to be noisy or inexact within about 0.5mA without switching any junctions in the circuit [25].

In relation to a negative input current through L_2, B_0 and B_2 are now positively biased by I_0 while the biasing current through B_3 is decreased as current is extracted from the circuit through the input. When the input current is below a certain threshold, B_0 and

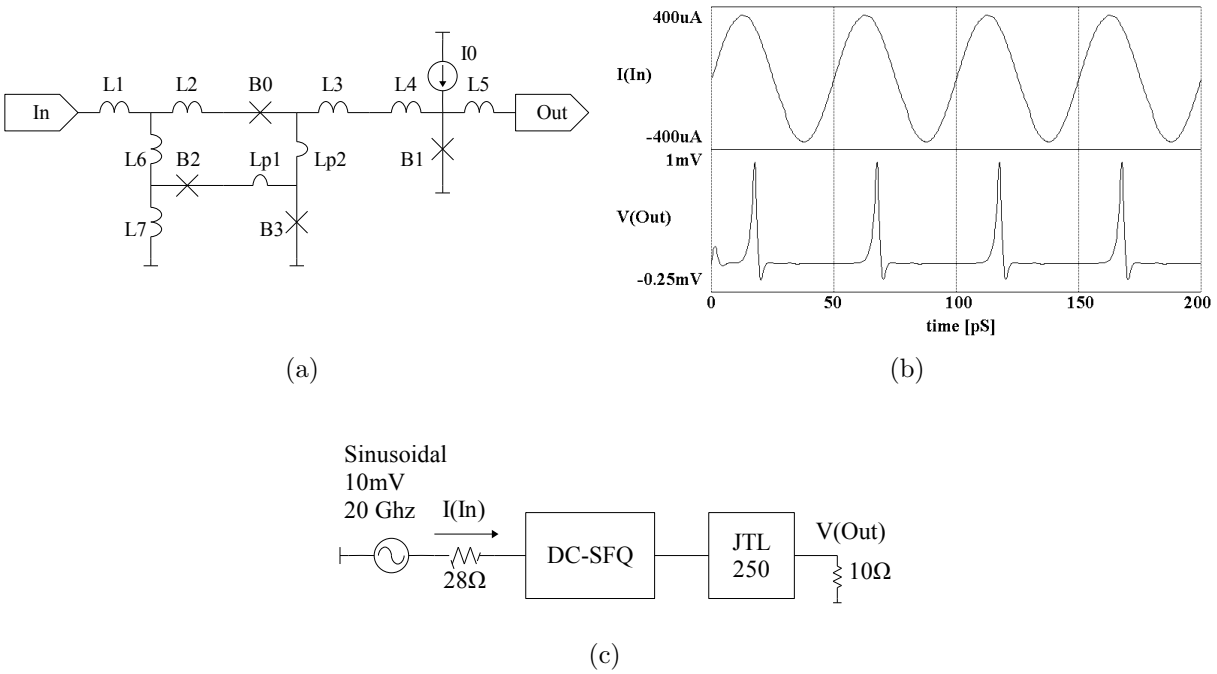


Figure 3.4: DC-to-SFQ converter (a) circuit details, (b) simulated responses and (c) simulation test setup

B_2 switch, resetting the circuit.

Pulse Merger

The SFQ pulse merger is a circuit that enables SFQ pulses from 2 different sources to be merged into a single output. The circuit is presented in Fig. 3.5. The simulation result is obtained using the following circuit component values: $B_{0,3,4} = 250\,\mu A$, $B_{1,2} = 225\,\mu A$, $L_{1,3} = 1.97\,pH$, $L_{2,4} = 0.66\,pH$, $L_5 = 2.64\,pH$, $L_6 = 2\,pH$, $L_{p1} = 0.21\,pH$ and $I_0 = 513\,\mu A$.

The pulse merger demonstrates the buffering function of serial junctions that are not connected to ground. These are also referred to as auxiliary junctions. All junctions in this circuit are biased by I_0. An input pulse at B_0 produces a rapid current increase in B_0 and switches the junction. This causes a current pulse to rapidly increase current through B_1, B_2, B_3 and B_4. Because of the bias current directions and JJ I_c values, B_3 switches instead of B_1, and B_3 switches before B_4. This prevents SFQ pulse from being reproduced from one input to the other. This operation clearly shows the buffering function of serial junctions B_1 and B_2.

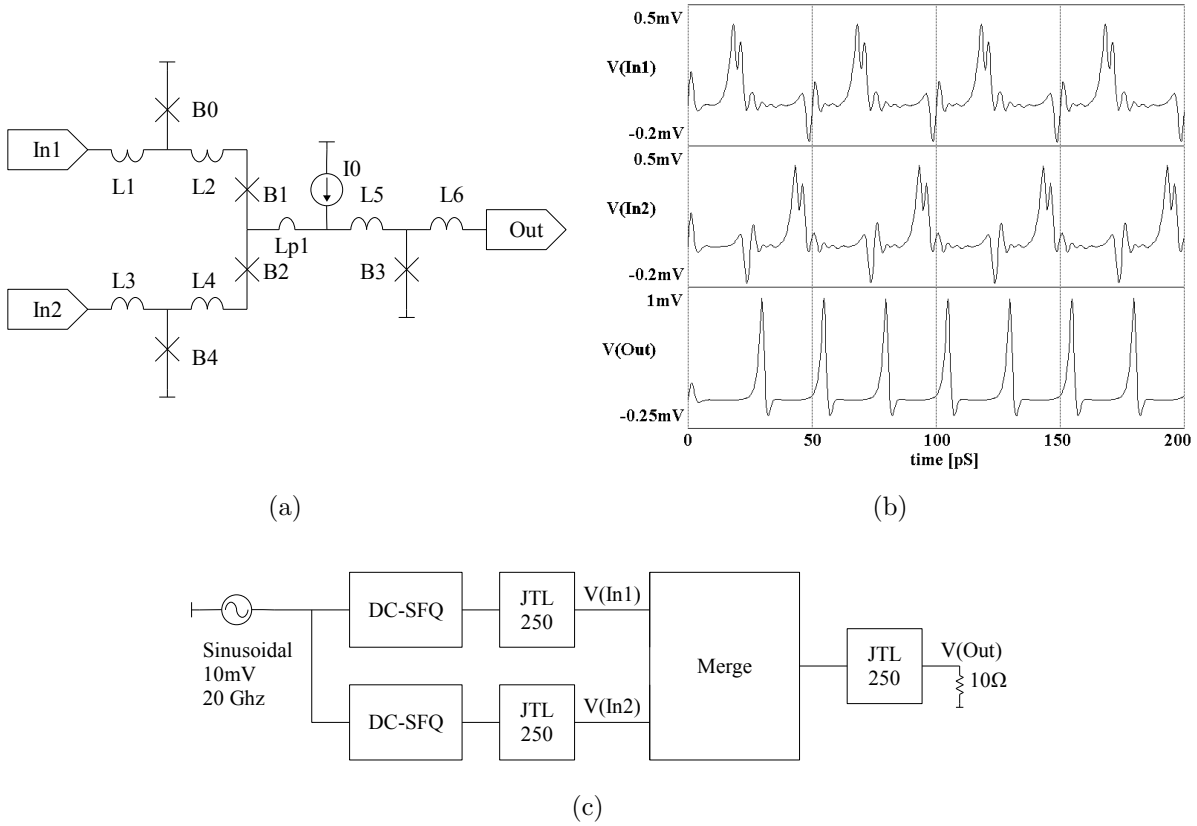


Figure 3.5: Pulse merger (a) circuit details, (b) simulated responses and (c) simulation test setup

Pulse Splitter

RSFQ is a current based logic and pulse energy is divided when pukA/cm^{2}lses are simply split over multiple inductive paths. Pulses have to be reproduced to ensure signal integrity. The SFQ pulse splitter is an important circuit for the distribution of clock or data pulses to various RSFQ cells. The circuit is shown in Fig. 3.6. The simulation result is obtained using the following circuit component values: $B_{0,2} = 251\,\mu A$, $B_1 = 355\,\mu A$, $L_{1,5} = 1.64\,pH$, $L_{2,6} = 1.98\,pH$, $L_3 = 0.82\,pH$, $L_4 = 1.16\,pH$ and $I_0 = 598\,\mu A$.

An input pulse at B_1 causes the junction to switch which creates a pulse that is divided between B_0 and B_2. Both these junctions then effectively reproduce the lower energy input pulses.

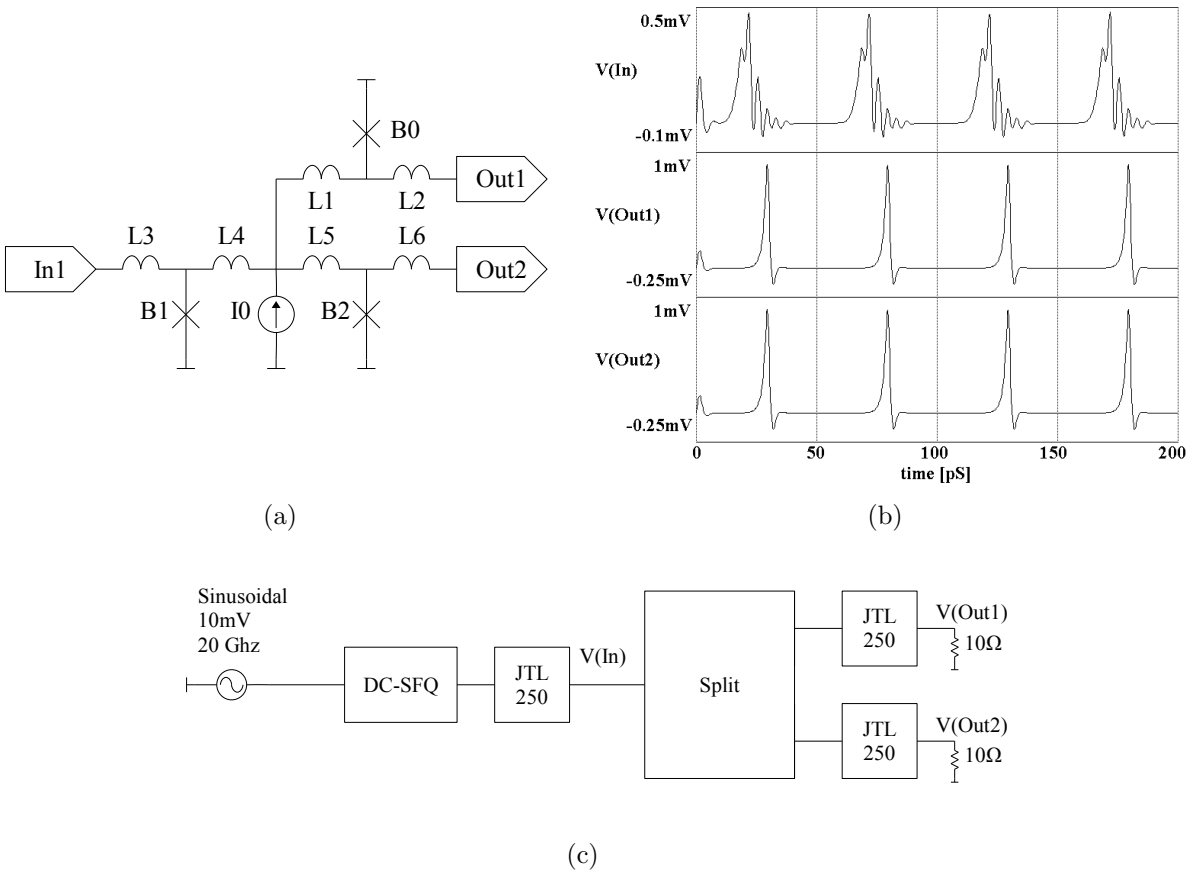


Figure 3.6: Pulse splitter (a) circuit details, (b) simulated responses and (c) simulation test setup

3.4.2 Logic Gates

Inverter (NOT)

The inverter cell is configured to accept an input within a certain period and then after receiving a clock pulse, produce the inversion of the input. When a pulse is received within the input period, no pulse is produced when the circuit is clocked. When no pulse is received during the input period, a pulse is produced at the output when the circuit is clocked. The simulation result is obtained using the following circuit component values: $B_0 = 355\,\mu A$, $B_1 = 140\,\mu A$, $B_2 = 250\,\mu A$, $B_3 = 310\,\mu A$, $B_4 = 175\,\mu A$, $B_5 = B_6 = 294\,\mu A$, $B_7 = 264\,\mu A$, $L_1 = 0.79\,pH$, $L_2 = 1\,pH$, $L_3 = 1.79\,pH$, $L_4 = 1.03\,pH$, $L_5 = 0.98\,pH$, $L_6 = 0.97\,pH$, $L_7 = 5.89\,pH$, $L_8 = 1.3\,pH$, $L_9 = 1.05\,pH$, $L_{10} = 0.887\,pH$, $L_{11} = 1.71\,pH$, $L_{12} = 1.12\,pH$, $L_{13} = 2.38\,pH$, $L_{p1} = 0.33\,pH$, $L_{p2} = 0.57\,pH$, $I_0 = 251\,\mu A$, $I_1 = 240\,\mu A$, $I_2 = 155\,\mu A$ and $I_3 = 185\,\mu A$.

The inverter operation is mainly performed by the 2-junction SQUID [20] formed by

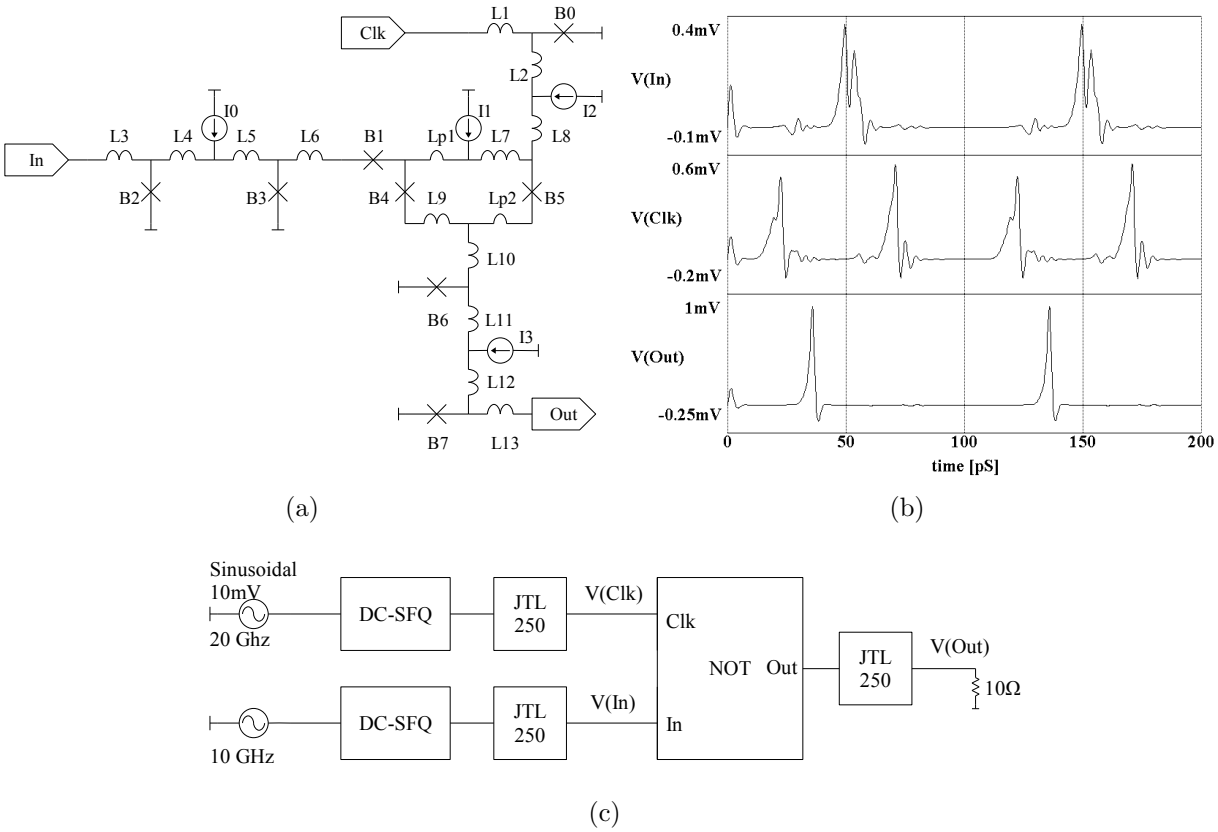


Figure 3.7: NOT (a) circuit details, (b) simulated responses and (c) simulation test setup

B_4, B_5, L_7 and L_9. In addition, pulse shaping occurs in the input JTL formed by B_2, B_3 and L_{3-6}, the output JTL formed by B_6, B_7 and L_{10-13} and the clock input pulse shaper formed by B_0 and $L_{1,2,8}$. The auxiliary junction B_1 prevents any clock pulses coming through L_8 and L_7 from switching B_3.

The amount of current through B_5 will determine whether a clock pulse coming through L_8 will propagate to the output JTL or not. In the initial unset state, the bias current will follow the path of least inductance through B_4 and L_9. An input pulse at the input JTL will switch the biased B_4 and cause the current coming from I_0 to flow through L_7 and B_5. In this stable state, an input clock pulse through L_8 will switch B_5 before switching B_6 and therefore produce no output when an input pulse is applied. The switching of B_5 redirects the bias current to flow through B_4 and the circuit is reset.

When no input pulse arrives, B_5 remains unbiased and an input clock pulse through L_8 causes B_6 to switch and therefore a pulse is propagated through the output JTL, effectively inverting the input.

AND Gate

When clocked, the AND logic gate produces an output SFQ pulse only when both of the two inputs have received an input SFQ pulse during the clock period. The circuit is shown in Fig. 3.8 along with simulation test setup and simulated response. The simulation result

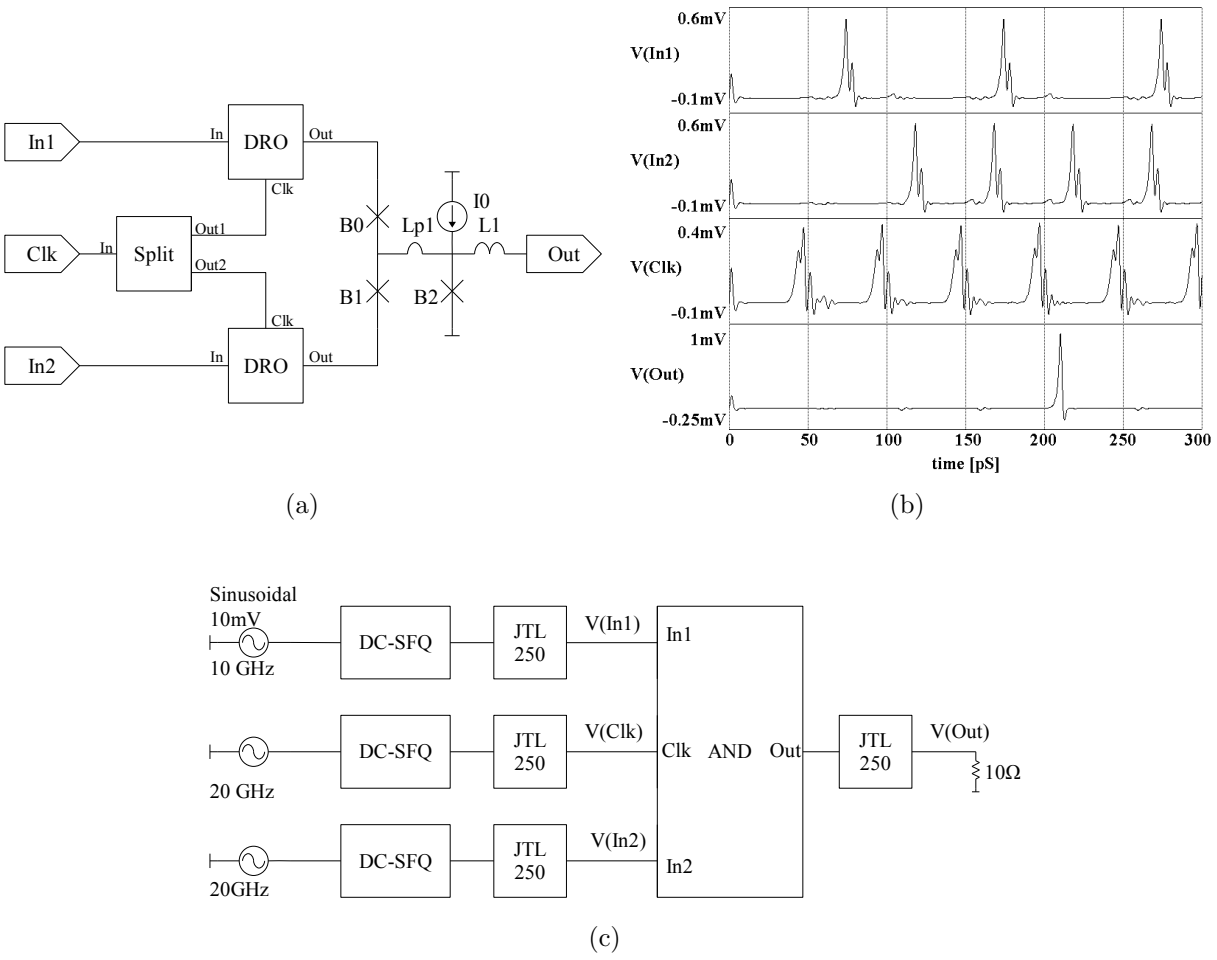


Figure 3.8: AND gate (a) circuit details, (b) simulated responses and (c) simulation test setup

is obtained using the following circuit component values: $B_{0,1} = 170\,\mu A$, $B_2 = 410\,\mu A$, $L_1 = 2\,pH$, $L_{p1} = 0.2\,pH$ and $I_0 = 279\,\mu A$.

The AND gate output is based on the current through B_2 when the gate is clocked. When only one input receives an SFQ pulse into a DRO during the clock period (see Section 3.4.3 for DRO operation), the current increase though B_2 is not enough for B_2 to switch when the gate is clocked. In this case B_0 or B_1 would switch depending on the DRO where the pulse arrived. When the gate is clocked and an input pulse arrived at each of the two inputs during the clock period, current through B_2 increases rapidly

above the threshold of B_2, causing it to switch before B_0 and B_1. In all cases the gate is reset as result of DRO properties.

The effective operation of this AND gate configuration is dependent on the simultaneous arrival of current pulses at B_2 as well as the threshold of B_2. The arrival times of these pulses as well as the sensitive threshold of B_2 are highly subject to the circuit parameter variations during fabrication. The gate presented delivers low Monte Carlo yield values. A large improvement of the circuit yield is obtained by Fourie [25], producing a more dependable, but relatively large circuit. The design of a more effective AND gate configuration is desired, but not presented in this thesis. Before attempting to design an improved AND gate circuit, it is recommended to study the XOR gate configuration which is dependent on the switching of DC currents through a single junction. Such configuration might lead to a much smaller and more dependable AND gate configuration.

XOR Gate

The XOR cell produces an output pulse when only one of the two inputs receives an SFQ pulse within the clock period. The circuit resets when both inputs receive a pulse or when a clock pulse is applied to produce an output depending on the state of the cell. The circuit is shown in Fig. 3.9 along with simulation test setup and simulated response. The simulation result is obtained using the following circuit component values: $B_{0,6} = 245\,\mu A$, $B_{1,2,3,5,8} = 171\,\mu A$, $B_4 = 193\,\mu A$, $B_7 = 221\,\mu A$, $L_{0,1} = 5.07\,pH$, $L_{2,3} = 2.63\,pH$, $L_4 = 1.05\,pH$, $L_5 = 4.75\,pH$, $L_{p1} = 0.4\,pH$ and $I_{0,1} = 86.7\,\mu A$.

The XOR cell operation depends on a 2-junction SQUID for each of the two inputs. The SQUIDs are formed by the loops that contain $B_{3,1,4,8}$ and $B_{5,2,4,8}$ respectively. It is clear that these loops share B_4 and B_8. The XOR operation is based on the amount of current flowing through these junctions. When the current exceeds a certain threshold, B_4 will switch and reset the circuit. Otherwise, a clock pulse will produce an output depending on the current flowing through B_8. An input pulse at *In1* causes B_3 and B_2 to switch. The bias current is therefore diverted through L_0 and flows through B_4 and B_8 effectively producing a stable set state. The same occurs for an input at *In2*, but when both inputs receive a pulse before the clock resets the circuit, B_4 will switch before B_8.

3.4.3 Destructive-ReadOut (DRO) Register

The DRO is a simple memory structure where an input pulse can be stored until a clock signal resets the register and produces a representation of the stored input in the form of an RSFQ pulse or the absence thereof. The circuit is presented in Fig. 3.10. The simulation

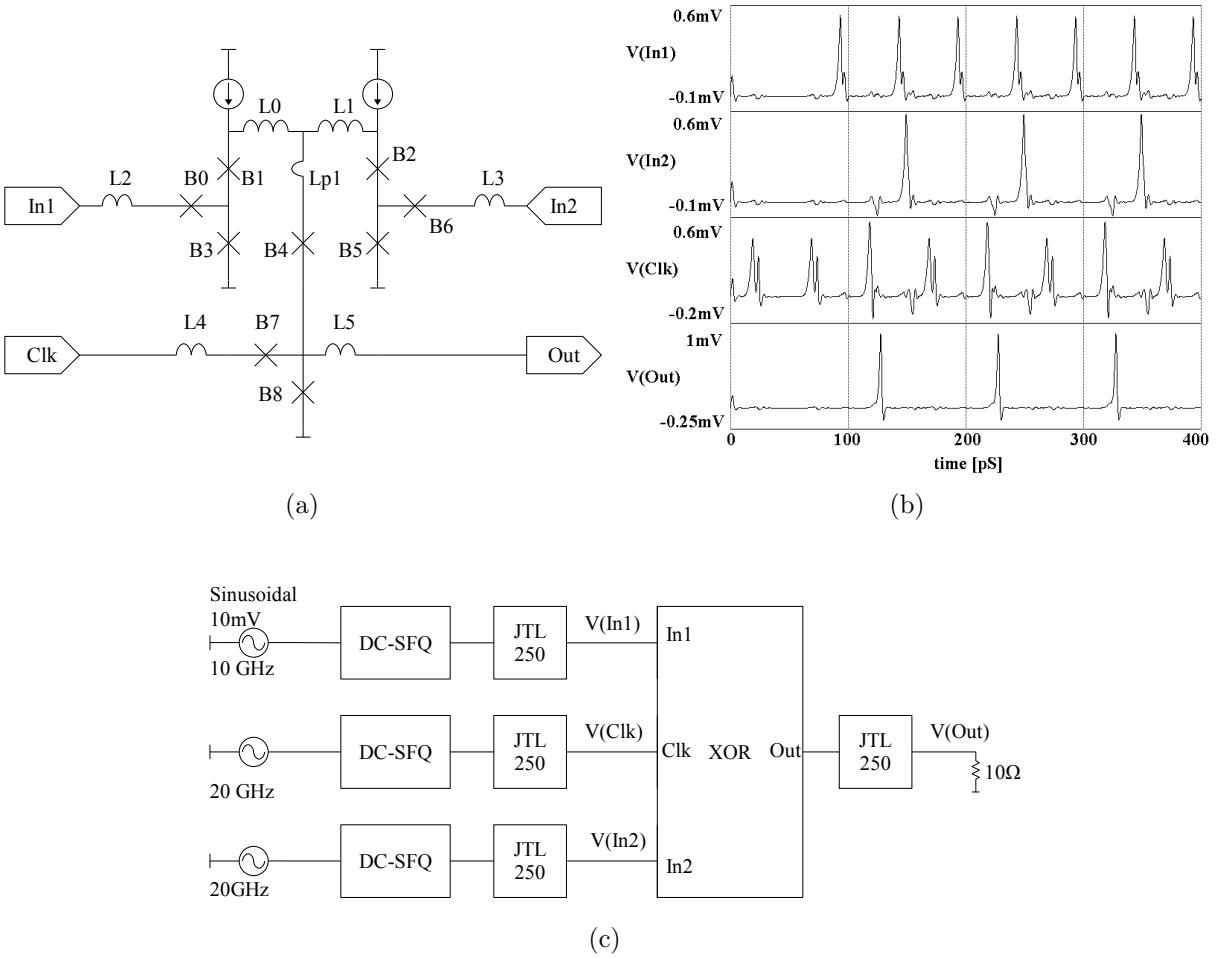


Figure 3.9: XOR (a) circuit details, (b) simulated responses and (c) simulation test setup

result is obtained using the following circuit component values: $B_{0,3} = 270\,\mu A$, $B_{1,2} = 245\,\mu A$, $L_0 = 1.58\,pH$, $L_1 = 2.77\,pH$, $L_2 = 8.474\,pH$, $L_3 = 3.17\,pH$ and $I_0 = 167\,\mu A$.

In the DRO the bias current is designed to mainly flow through B_2 when the circuit is in the unset state. When a pulse arrives at B_1 and B_2, B_2 switches before B_1 because of the strong bias current through B_2. The switching of B_2 causes the bias current to follow alternate routes to ground of which the predominant route is through L_2 and B_3. The relatively large value of L_2 prevents the bias current from being redirected through B_2 after it has switched. This enables a stable set state. When a pulse is now applied through the *read* input at L_0, B_3 is found to be biased through L_2 and therefore switches before the unbiased B_0, causing a pulse at the output. When B_3 switches the bias current is forced to follow an alternate path of least inductance. The current is therefore reset to the original path which is through B_2. After such a destructive read operation, the circuit is therefore ready to store a following input pulse.

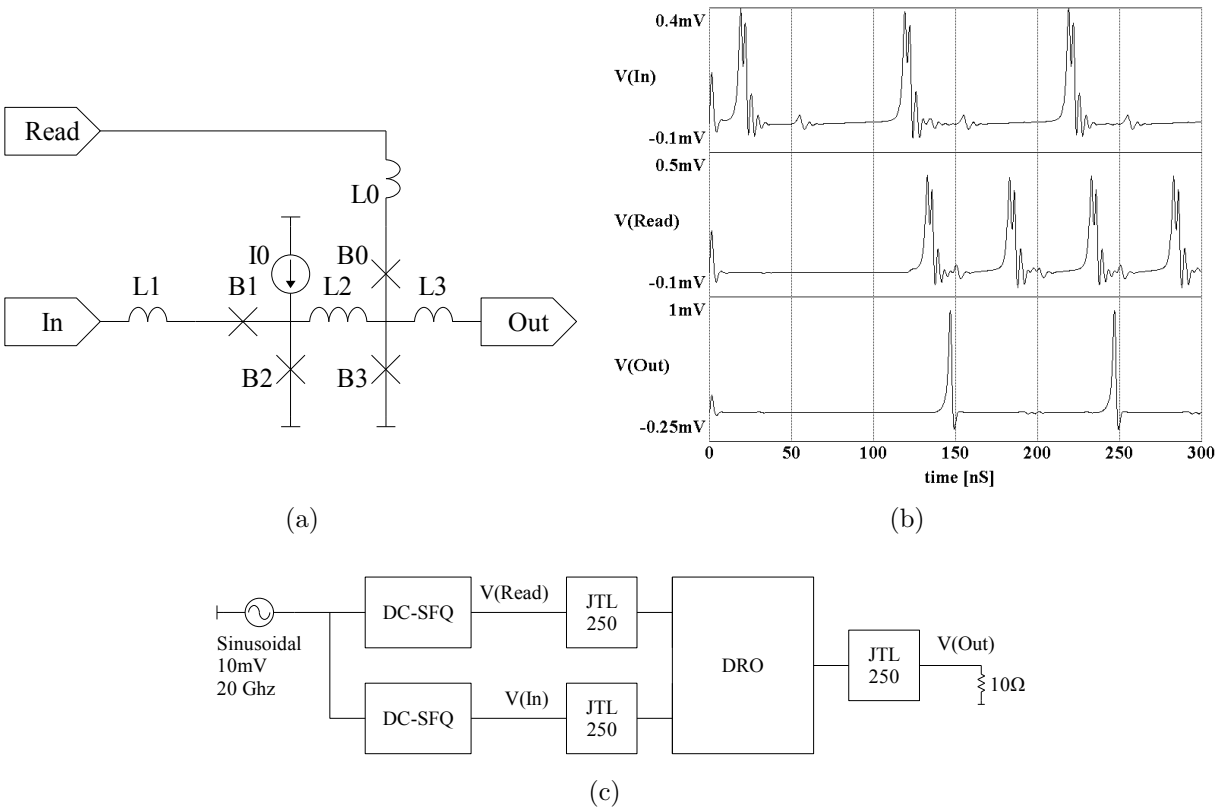


Figure 3.10: DRO (a) circuit details, (b) simulated responses and (c) simulation test setup

3.4.4 Toggle Flip-Flops (TFFs)

The TFF is a cell with two possible states. Triggered by an input pulse, the cell is switched from one state to the other. In the RSFQ versions of the TFF, one state is related to the storage of an input pulse and the other is related to the release of a stored pulse. An output pulse is produced in the latter state, and none for the former. A certain TFF configuration also allows for the synchronous acquisition of the TFF state in a destructive way. Different TFF configurations are proposed depending on the input, output and state acquisition requirements. The TFF can be configured to start at any one of the two possible states. Each of these configurations has its own advantages for specific applications. These different configurations will be referred to as the T1FF and T2FF. The T1FF will start in the state where an output pulse is produced for the first input pulse. The T2FF will start in the state where an input pulse is stored before producing an output pulse when the next input pulse arrives.

These TFFs produce one output pulse for two consecutive input pulses and are therefore useful as frequency dividers or binary counters.

The basic T1FF and T2FF are presented first before looking at a T2FF with destruc-

tive readout and 2 inputs (DT2FF). The latter is required for binary counters with a multiple bit input and synchronous readout. Some useful TFF configurations are also presented.

T1FF circuit

The T1FF circuit diagram, simulation test setup and simulation results for the T1FF is presented in Fig. 3.11. The operation of the T1FF is demonstrated by cascading 2 of these cells. The simulation result is obtained using the following circuit component values:

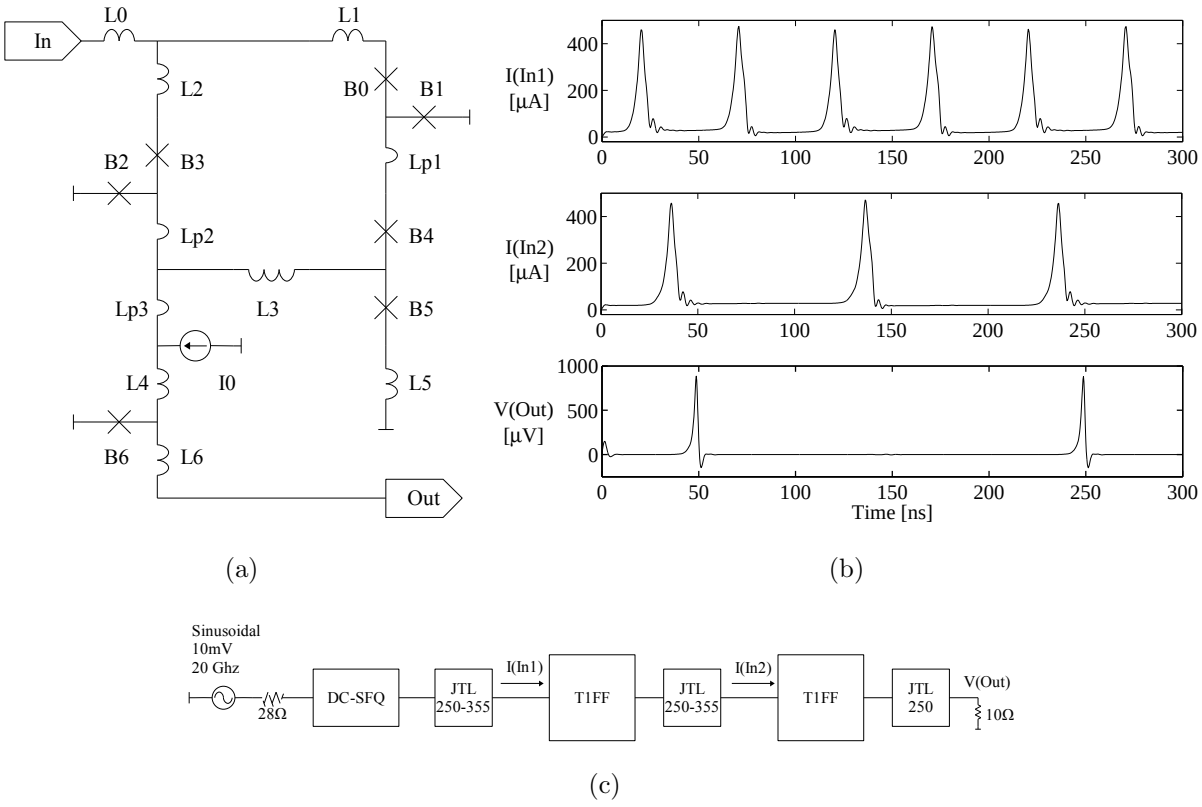


Figure 3.11: T1FF (a) circuit details, (b) simulated responses and (c) simulation test setup

$B_0 = 204\,\mu A$, $B_1 = 250\,\mu A$, $B_2 = 211\,\mu A$, $B_3 = 206\,\mu A$, $B_4 = 190\,\mu A$, $B_5 = 253\,\mu A$, $B_6 = 237\,\mu A$, $L_0 = 0.836\,pH$, $L_1 = 0.868\,pH$, $L_2 = 1.5\,pH$, $L_3 = 4.05\,pH$,$L_4 = 2.49\,pH$, $L_5 = 3\,pH$, $L_6 = 3.29\,pH$, $L_{p1} = 0.594\,pH$, $L_{p2} = 0.526\,pH$, $L_{p3} = 0.55\,pH$ and $I_0 = 412.5\,\mu A$.

In the circuit, junctions B_2 and B_6 are initially biased by I_0, while junctions B_1 and B_5 are not implicitly biased. With an input SFQ pulse through L_1 and L_2, the biased junction B_2 then switches before B_3 and B_0 switches before B_1. This causes B_6 to switch

and produces an output SFQ pulse. With the switching of B_1 and B_6, most of the current from I_0 is now diverted through L_3 and this effectively biases junctions B_1 and B_5. A following input pulse through L_1 and L_2 now finds B_1 biased and causes B_1 and B_3 to switch. The switching of B_1 causes B_5 to switch producing an output pulse between L_3, B_5 and B_4. This pulse produced by B_5 also causes B_4 to switch, forcing the current thought L_3 to divert to the path of least inductance through B_2 and B_6. In this way the circuit is reset to the initial state.

The simulation test setup in Fig. 3.11 (c) shows the configuration for a simple frequency divider where $f_{out} = f_{in}/4$. All frequency dividers used in this thesis are a similar configuration of cascaded T1FFs where the number of T1FFs used (n) is related to the division factor as follows:

$$f_{out} = \frac{f_{in}}{2^n}$$

T2FF circuit

The T2FF circuit is derived from a TFF circuit with non-destructive readout proposed by Filipov *et al.* [27]. The readout circuit is removed and a few component values are changed to allow output only from the second received input pulse. The T2FF circuit diagram, simulation test setup and simulation results for the T2FF is presented in Fig. 3.12. The operation of the T2FF is demonstrated by cascading 2 of these cells. The simulation result is obtained using the following circuit component values: $B_0 = 325\,\mu A$, $B_1 = 237\,\mu A$, $B_{2,3} = 212\,\mu A$, $B_4 = 237\,\mu A$, $B_{5,6} = 250\,\mu A$, $L_0 = 1.97\,pH$, $L_1 = 1.44\,pH$, $L_{2,3} = 0.92\,pH$, $L_{4,5} = 1.3\,pH$, $L_6 = 2.1\,pH$, $L_7 = 4.73\,pH$, $L_8 = 4.1\,pH$, $I_0 = 275\,\mu A$ and $I_1 = 231\,\mu A$.

In this circuit an input pulse at L_0 causes the pulse to be sharpened by B_0. This pulse is then divided between L_2 and L_3. Junctions B_4 and B_5 are biased by I_1 while B_2 and B_6 are not implicitly biased. In this state an input pulse causes B_4 to switch before B_3 and causes B_1 to switch before B_2. A pulse is produced by B_4, causing B_5 to switch. In this way, most of the I_0 current is diverted through L_7, effectively biasing junctions B_2 and B_6. A following input pulse now causes B_3, B_2 and B_6 to switch, producing an output pulse through L_8. This also causes the current through L_7 to be diverted back to its original path of least inductance mainly through B_4 and B_5, effectively resetting the circuit to its original state.

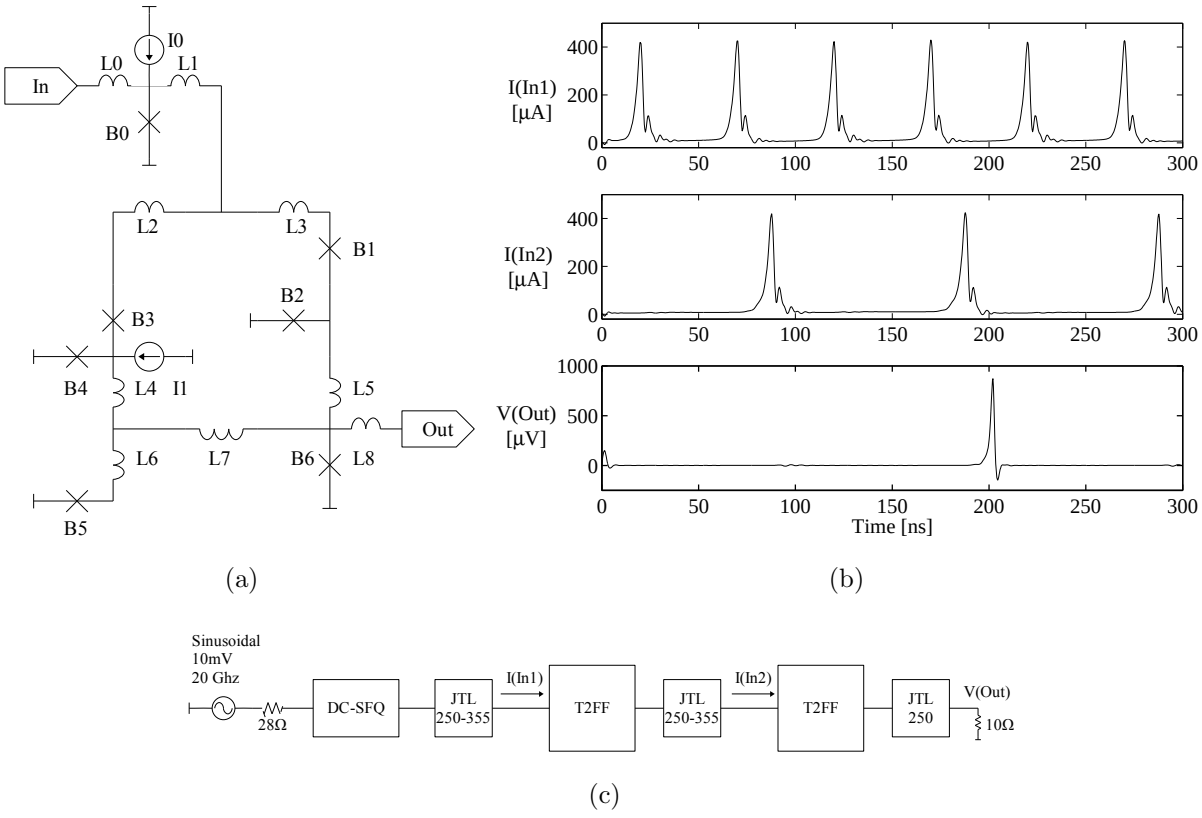


Figure 3.12: T2FF (a) circuit details, (b) simulated responses and (c) simulation test setup

DT2FF circuit

The circuit for a T2FF with 2 inputs and destructive readout ability (DT2FF) is derived from the basic T2FF. The circuit diagram, simulation test setup and simulation results are presented in Fig. 3.13. The circuit component values used for simulation are as follows: $B_{0,1} = 325\,\mu A$, $B_{2,3} = 237\,\mu A$, $B_{4,5,8} = 212\,\mu A$, $B_{6,7} = 237\,\mu A$, $B_{9,10} = 250\,\mu A$, $B_{11,12} = 194\,\mu A$, $L_{0,1,8} = 1.97\,pH$, $L_{2,3} = 0.92\,pH$, $L_{4,5} = 1.3\,pH$, $L_6 = 2.1\,pH$, $L_7 = 4.73\,pH$, $L_9 = 3.42\,pH$, $L_{p1,p2} = 0.02\,pH$, $L_{p3} = 0.418\,pH$, $I_0 = 520\,\mu A$, $I_1 = 65\,\mu A$ and $I_2 = 225\,\mu A$.

The circuit operation is much the same as the basic T2FF. With this circuit the possibility now exists for one of two inputs to switch the circuit state and a destructive readout is possible that resets the circuit. In the reset state an input pulse at L_0 or L_1 causes $B_{5,6,10}$ to switch, diverting the current through L_7 to bias B_7 and B_{12}. When B_{12} is biased, an input clock pulse through B_{11} switches B_{12}, producing an output pulse through L_9. This pulse causes B_9 and then B_8 to switch, resetting the circuit to its original state. When the circuit is in the set state, a second input pulse at L_0 or L_1 causes $B_{4,7}$ to switch, producing an output pulse at L_8.

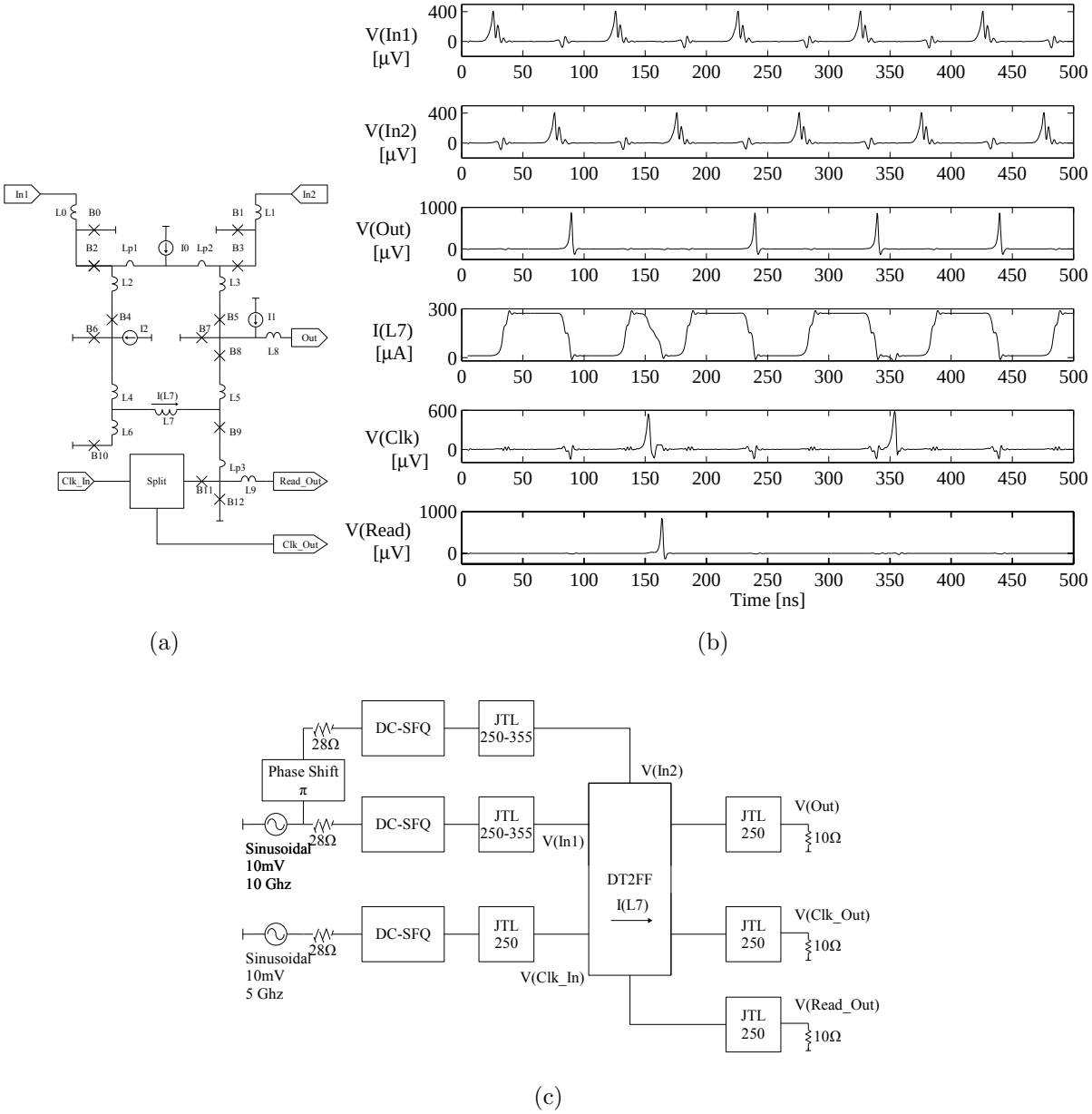


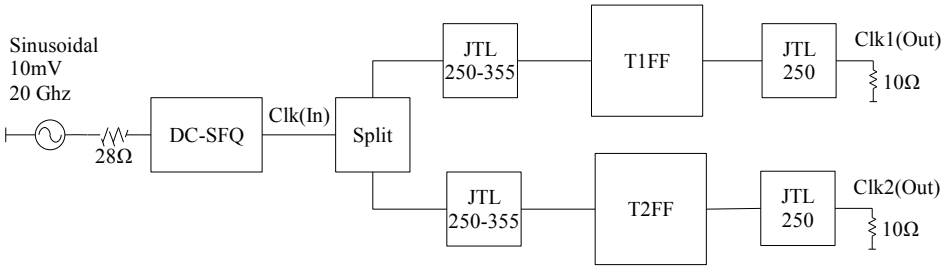
Figure 3.13: DT2FF (a) circuit details, (b) simulated responses and (c) simulation test setup

T2FF-based circuit Monte Carlo Analysis

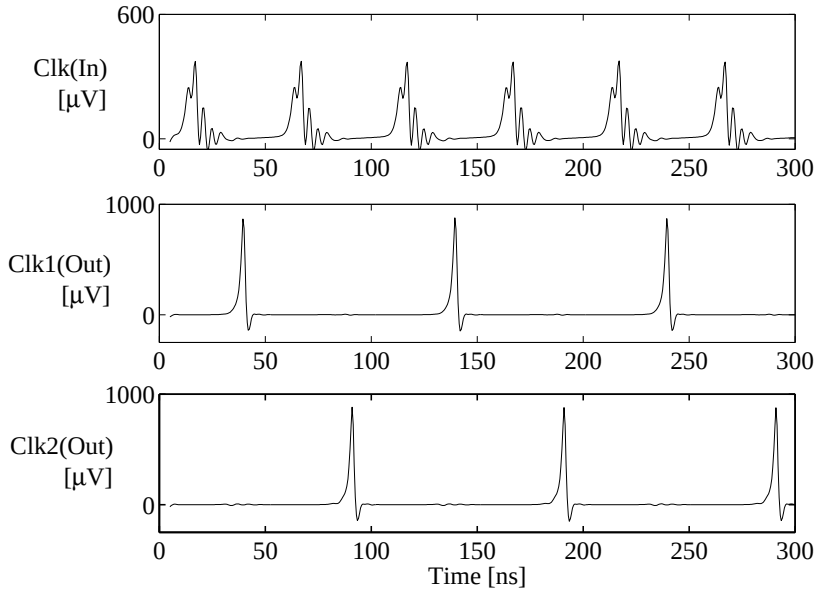
A Monte Carlo yield analysis revealed a T2FF yield of 96.69 % and DT2FF yield of about 80.16 %. Both circuits were analyzed for 10 GHz input signals and the DT2FF was tested with a readout clock of 4 GHz. No optimization was done and is recommended for these non-optimal circuits. The yield of the DT2FF is considered very low, but when analysing the simple operation of this circuit, it is assumed that a large yield is possible by optimizing the circuit components.

TFF-based two-phase clock

Some applications require for the clock signal to have a certain phase difference in different circuit components. This can be achieved by using cascaded JTLs that provide an arbitrary latency. A clock phase difference can also be created by the combined use of a T1FF and T2FF. The proposed configuration and simulation results for a two-phase clock generator is presented in Fig. 3.14. The disadvantage of this method is the implied frequency division by TFF circuits.



(a)



(b)

Figure 3.14: A two-phase clock generator. Shown in (a) is the simulation test setup and (b) simulated responses.

3.4.5 DC-enabled JTL

The DC-enabled JTL (DCE-JTL) is simply a JTL that allows input pulses to be passed or blocked depending on an external DC current that switches polarity. The circuit for a DCE-JTL is presented in Fig. 3.15. The circuit component values used for simulation

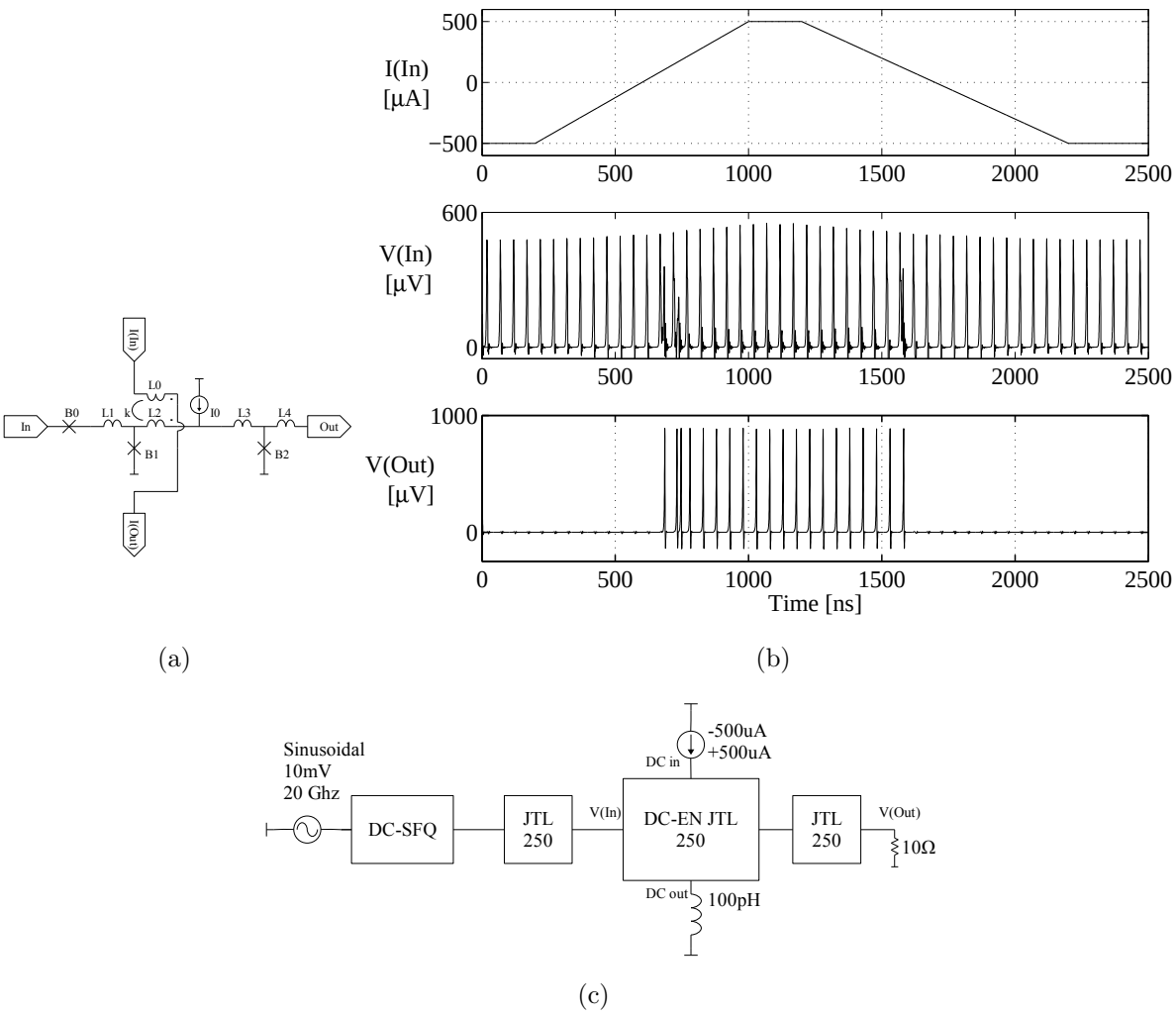


Figure 3.15: DCE-JTL (a) circuit details, (b) simulated responses and (c) simulation test setup

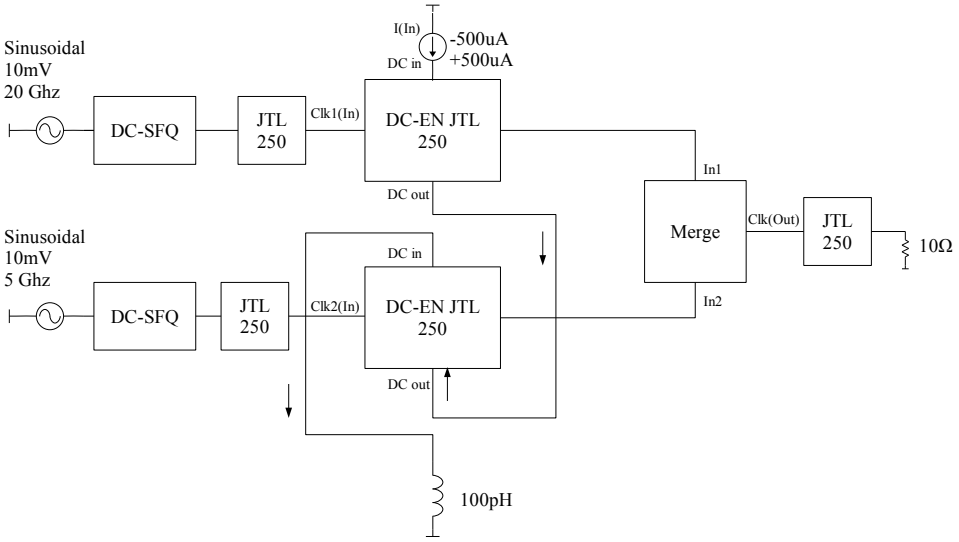
are as follows: $B_0 = 150\,\mu A$, $B_1 = 280\,\mu A$, $B_2 = 250\,\mu A$, $L_0 = 2\,pH$, $L_1 = 1\,pH$, $L_{2,3,4} = 1.98\,pH$ and $I_0 = 351\,\mu A$.

In the DCE-JTL, a bi-polar DC signal biases or unbiases the input junction to the JTL, depending on the polarity. When B_1 is properly biased, the cell functions like a normal JTL. When B_1 is unbiased, an input pulse at B_0 will cause B_0 to switch before

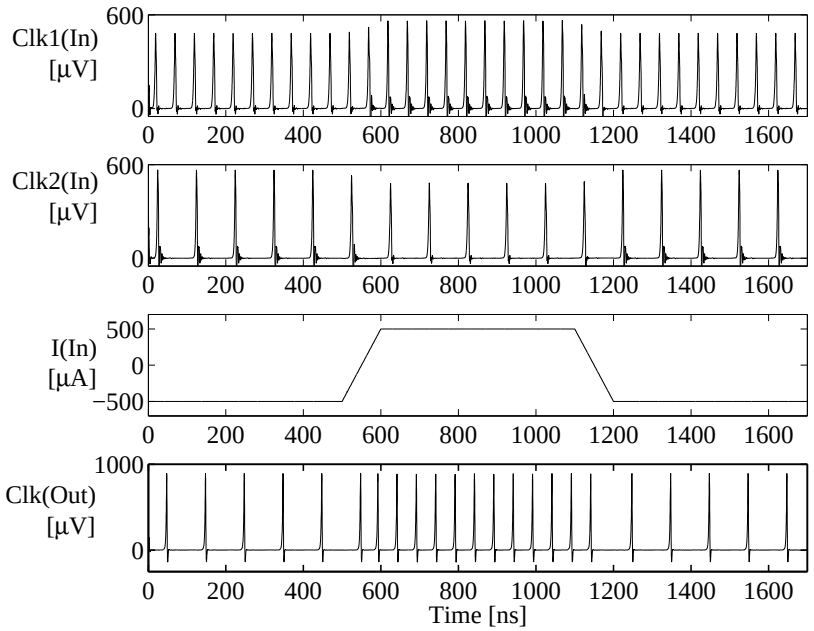
B_1, effectively blocking input pulses from being reproduced at the output. This cell is designed to be controlled by either external or internal signal. Transient effects when switching DC signal polarity may cause circuit yield to be low, although the circuit is still useful for certain applications that cope with such transient effects. Such an application is discussed in Chapter 5.

The non-optimized DCE-JTL circuit delivers a yield of 99.17 %. The yield analysis details can be seen in Appendix D.

The DCE-JTL is mostly used for the switching of different clock signals to a single clock distribution circuit. Such application requires two DCE-JTLs configured as seen in Fig. 3.16. The circuit simulation result is also shown in Fig. 3.16 where it is clear how the switching between two different clock signals occur.



(a)



(b)

Figure 3.16: DCE-JTL switch configuration for clock distribution. Shown in (a) is the simulation test setup and (b) simulated responses.

Chapter 4

Analogue-to-Digital Conversion

4.1 Introduction

One of the most important elements in a digital communications receiver system is the analogue-to-digital converter (ADC). These converters have a large influence on the receiver performance and therefore form an important part in studies on the improvement of wireless receiver systems. This chapter covers basic ADC theory, superconductor ADC advantages, discussions on different ADC types and implementation of some ADC types.

Firstly some important concepts that influence ADC performance are discussed. The advantages of superconductor ADCs are then discussed, followed by the demonstration of general superconductor ADC circuits. Variations of these circuits, using the same concepts, are commonly used for ADC modulator quantization and feedback. Different types of superconductor ADCs are then covered with the main focus on oversampling ADCs. This is followed by a discussion on the increase of oversampling superconductor ADC dynamic range. The design and evaluation of two delta-type modulators are then presented along with the general specifications of ADC input waveforms. The design of a simplified decimation filter structure for superconductor implementation is then discussed and presented. The two proposed oversampling modulators are evaluated along with the decimation filter to produce simulated ADC dynamic range results by which the two modulators can be compared.

4.2 ADC Background

Analogue-to-digital converters (ADCs) convert analogue input signals to digital output codes. ADCs have many different sources of inaccuracy. Here some important noise and

distortion sources for ADCs with dynamically changing input (communication signals) are briefly discussed. Performance specifications that are generally given for specific ADCs, quantify the errors caused by an ADC. The main errors produced by ADCs are identified as quantization errors, errors due to aliasing and errors due to distortion caused by the non-linearity of the ADC.

4.2.1 Quantization Errors

Quantization errors are inevitable when representing analogue signals with digital numbers. When an analogue signal is digitized, a decision has to be made according to a certain threshold and therefore information is lost, sometimes causing errors. In an ideal digitization system, quantization errors will appear as the noise floor in a spectrum evaluation of a digitized analogue signal. As explained in Appendix A.1, the theoretical SNR of an ideal ADC is

$$SNR_{ADC}(dB) = 6.02N + 1.76\,dB \tag{4.1}$$

where N is the number of bits (resolution). As example, an ideal 14-bit ADC would have an SNR of about $86\,dB$.

4.2.2 Aliasing

Sampling produces replicas of the input signal at multiples of the sampling frequency as seen in Fig. 4.1. These replicas form in such a way that input frequencies are mirrored around multiples of the sampling frequency. Sampling at frequencies much larger than the input signal bandwidth produce replicated signals that do not overlap with the input signal frequencies as shown in Fig. 4.1. When sampling at a frequency lower than twice the input signal bandwidth (lower than the Nyquist frequency), the replicated signal overlaps with the input signal frequency band, causing distortion as seen in Fig. 4.2. In this way unwanted frequencies are introduced in the band of interest and can not be filtered out without losing valuable information. This effect is known as aliasing. ADCs are usually preceded by anti-aliasing filters that limit the input signal bandwidth by suppressing frequencies that are out of the band of interest. The result of aliasing would influence the ADC performance if frequencies are not suppressed below the noise floor of the ADC. Aliasing is likely to occur at the decimation stage of an oversampling ADC. Aliasing in the decimation filter is discussed in Section 4.8.

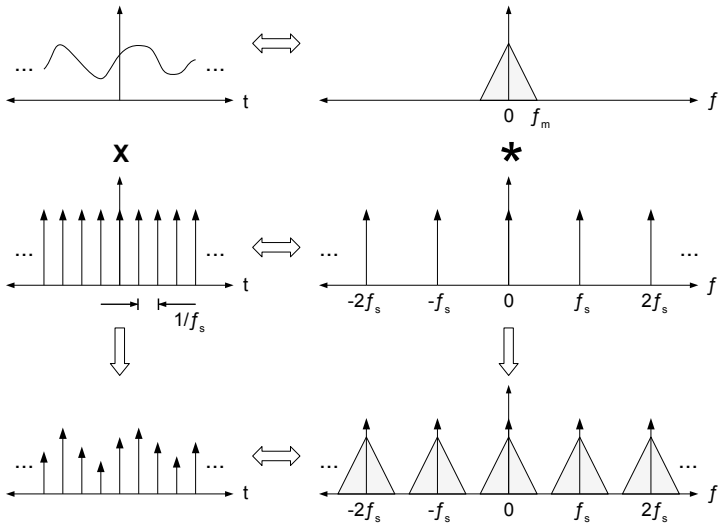


Figure 4.1: An example of how sampled time signals are translated to the frequency domain.

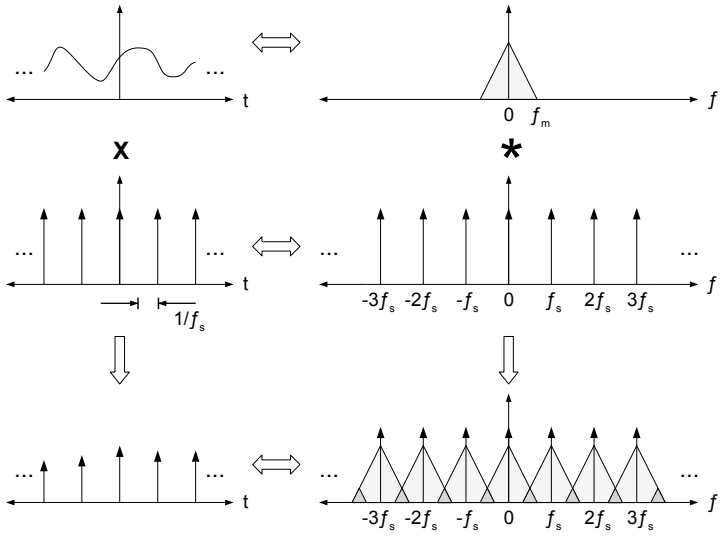


Figure 4.2: An example of how aliasing occurs with time to frequency domain translations

4.2.3 Dynamic Range

In simple terms dynamic range (DR) can be described as an indication of the range between the biggest signal and smallest signal that can be recognized in a system. It is always a figure for a certain bandwidth. In communication systems it is important to maximize this figure in order to communicate as effectively as possible. Dynamic range figures include figures such as the signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SINAD), spurious-free dynamic range (SFDR) and the effective number

of bits (ENOB). For more about these figures, see Appendix A.1.

There are many ways to increase the dynamic range of an ADC. One of these is to increase the number of quantization levels. This produces an increased number of output bits at the quantizer and therefore increases signal resolution, allowing a larger difference between the smallest and biggest input signal. Another method used in oversampling ADC modulators is to increase the modulator order. This generally suppresses quantization noise, leading to improved small signal recognition and therefore increased DR. It is important to note that some modulators (Sigma-Delta types) shape the quantization noise. In such modulators noise is suppressed at lower frequencies but enhanced at higher frequencies. In higher-order Sigma-Delta type modulators noise is suppressed more at lower frequencies, but enhanced more at higher frequencies.

4.3 Superconductor ADC advantages

Superconducting and RSFQ circuits have characteristics that are uniquely suitable for analogue-to-digital conversion. RSFQ circuits have the inherent property of flux quantization which means that in a closed loop made from superconducting material, magnetic flux can only exist in discrete quantized amounts. These amounts are multiples of the fundamental physical constant, the magnetic flux quantum (Φ_0), defined as

$$\Phi_0 = \frac{h}{2e} \approx 2.07 \times 10^{-15},$$

where h is Planck's constant and e is the electron charge. Such circuits can convert analogue signals to the digital domain with exceptional linearity. With relatively crude fabrication technology ($3\,\mu m$), very high speed circuits have been demonstrated [28]. Recent improvements in the commercial fabrication process [29] have led to medium-scale ICs working at about 80 GHz. Using an experimental $0.3\,\mu m$ fabrication, RSFQ technology has been demonstrated to operate at 770 GHz for a digital frequency divider [30]. Oversampling ADCs operating at such high speeds may offer a commercially interesting output bandwidth with sufficient resolution, especially for SDR application. Currently popular RSFQ circuits (based on Niobium) operate at a temperature of $4K$ where there are very low thermal noise levels. This allows more sensitive detectors and may even eliminate the need for an LNA before analogue-to-digital conversion. Low switching energy of junctions used in RSFQ circuits (about 10^{-18} Joules) allow for more tightly packed circuits (smaller fabrication), higher switching speeds and thus faster ADCs.

Superconductors therefore have attractive properties for the implementation of ADCs

and particularly the implementation of oversampling ADCs.

4.4 Superconductor ADC building blocks

4.4.1 Quantizer and feedback

A single Josephson junction (JJ) is the most integral part of any superconductor quantizer. Such a junction has the characteristic of becoming resistive when current through the junction exceeds the critical current (I_c) of the junction. RSFQ logic uses resistively shunted junctions to produce a short voltage pulse when the current through it exceeds I_c [20]. Therefore, when the input current goes above I_c, a pulse is produced. When the input current is below I_c, no output pulse is produced.

When a junction switches, an inherent feedback effect occurs. This is demonstrated by a superconducting loop consisting of an inductance coupled to an input source and connected to a quantizer (Shunted JJ) as seen in Fig. 4.3.

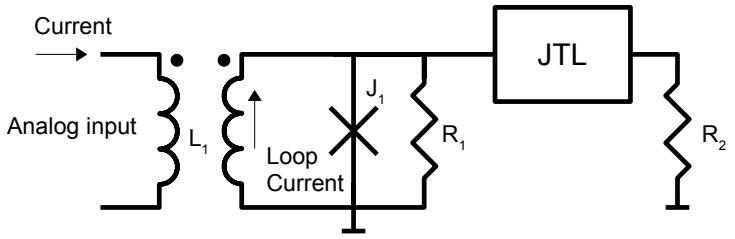


Figure 4.3: A simple quantizer circuit to demonstrate inherent feedback in RSFQ circuits. Here $L_1 = 500\,pH$, $J_1 = 250\,\mu A$, $R_1 = 2.88\,\Omega$ and $R_2 = 10\,\Omega$.

The output of the quantizer is connected to a JTL and output SFQ pulses are produced across R_2. The feedback effect can clearly be seen by applying a constant current as input to the circuit shown in Fig. 4.3. The result is that an exact amount of current is repeatedly subtracted from the loop current until it is below the I_c value of the junction. The amount of current subtracted ($\triangle I_{loop}$) is related to magnetic flux as follows:

$$\triangle I_{loop} = \Phi_0 / L_{loop} \tag{4.2}$$

Without accounting for parasitic inductances, $\triangle I_{loop}$ in this example should be approximately $\Phi_0/500pH \approx 4.14\,\mu A$. This is confirmed in simulation as indicated in Fig. 4.4. Junction switching properties cause a magnetic flux quantum (Φ_0) to be consumed

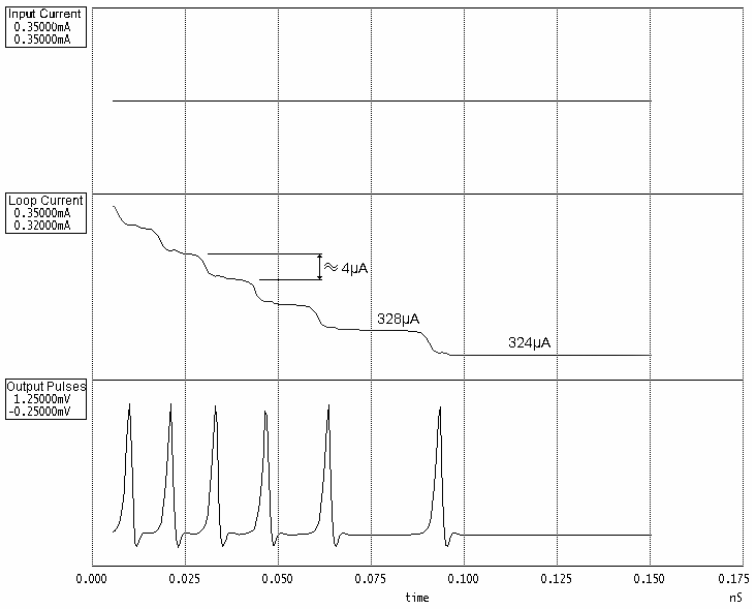


Figure 4.4: Simulated response for the circuit presented in Fig. 4.3

mainly by the shunt resistance (R_1) over the junction. This consumption leads to the reduction of current in the loop.

As seen in Fig. 4.4 the loop-current reductions are immediate, occurring within about $5-10\,ps$ which is much faster than the average sampling clock. In a synchronous quantizer this effect is modelled by the subtraction of an exact amount of current, delayed by one sampling period. The delay is introduced because the subtracted current only influences the next sampling operation.

4.4.2 Filters

The most commonly used filter function in superconductor ADC modulators is the integrator. To date, there is no known way to make high performance superconducting analogue integrators [31]. Low-pass filters (LPFs) are generally used in superconducting electronics as analogue integrators, because their frequency response is similar to that of an integrator. The most basic LPF in superconducting electronics is the first-order R-L filter. These filters integrate SFQ pulses to sustained amounts of current, shown in Fig. 4.5. The LPF is formed by L_1 and R_1 and the filter induces current into L_2. This is a typical setup for LPF use in a superconducting ADC. The cut-off frequency for R-L filters are:

$$f_c = \frac{R_1}{2\pi L_1} \tag{4.3}$$

The voltage based transfer function (H_v) of the circuit in Fig. 4.5 is calculated as

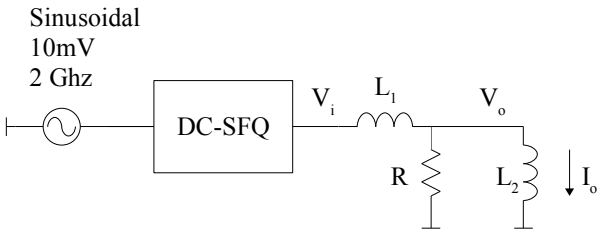


Figure 4.5: A first order R-L superconductor filter circuit to demonstrate the integration effect. Here $L_1 = 100\,pH$, $L_2 = 400\,pH$ and $R_1 = 2\,\Omega$

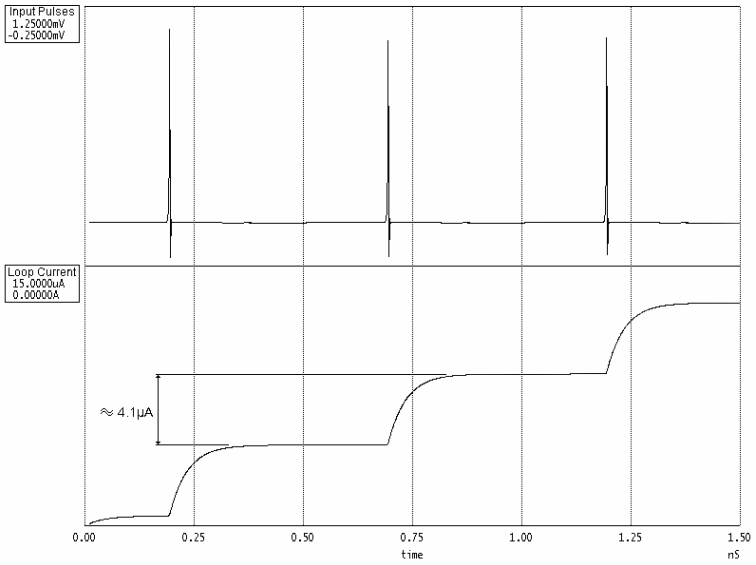


Figure 4.6: Simulated response for the circuit presented in Fig. 4.5.

$$H_v(s) = \frac{V_o(s)}{V_i(s)} = \frac{R/L_1}{s + (R/L_2 + R/L_1)}.$$

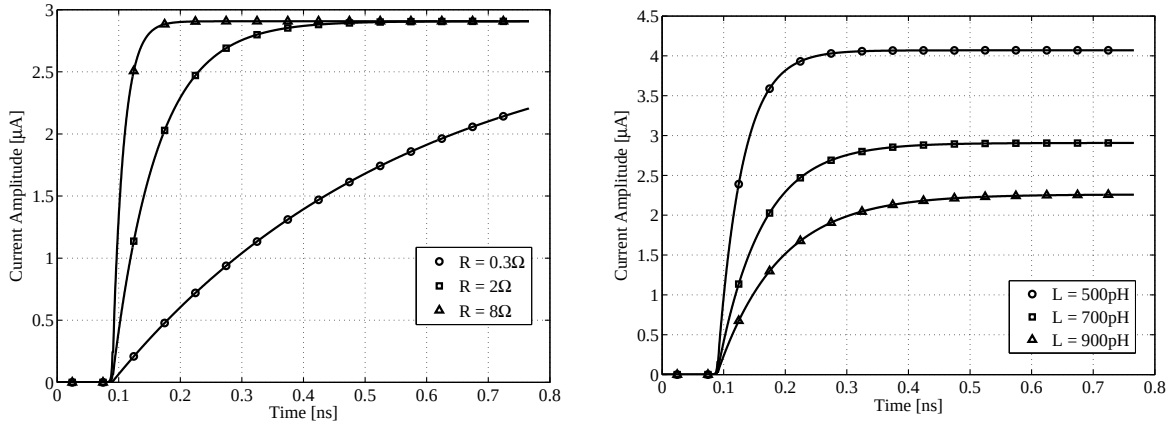
The output current I_o in the model is obtained along with the current based transfer function (H_i) as follows:

$$H_i(s) = H_v(s)\frac{1}{sL_1},$$

so that

$$I_o(s) = V_i(s)H_i(s).$$

The model is excited with RSFQ pulses that consist of sampled points obtained through WRspice circuit simulations. The simulated output currents for differing values of resistance (R_1) and inductance ($L = L_1 + L_2$) is shown in Fig. 4.7. To produce an accurate



(a) Varying resistance, L=700pH

(b) Varying inductance, R=2

Figure 4.7: Modelled RL-filter output current for different filter inductance and resistance values.

response, RSFQ pulses are sampled each 0.5ps in the WRspice simulation. The modelled output current of the filter is therefore also produced at this rate, giving sufficient output definition. ADC oversampling modulators sample at a rate much lower than this and therefore the simplification of the filter effect on a superconducting modulator is investigated for simplified superconductor ADC modelling.

For the modelling of an ADC modulator, the filter model can be simplified by choosing the filter component values ($L_{1,2}$ and R_1) optimally. The values are chosen according to the filter effect on the modulator quantization noise and response time. The filter optimization is discussed along with the evaluated ADC modulators in Section 4.7.

4.5 ADC types for superconductor implementation

Numerous types of ADCs exist and many of them are suitable for implementation in superconducting electronics [28]. They can be divided into two main categories, namely Nyquist rate and oversampling converters.

Nyquist rate converters sample at a rate equal to or greater than the Nyquist rate for a desired input bandwidth. The direct conversion (flash type) ADC is an example of a Nyquist rate converter. This converter generally uses a large comparator structure

which directly produces a binary output according to the input voltage level. A structure with 2^n comparators is required for an n-bit converter. Fabrication processes cause slight mismatches in comparator components and decrease the dynamic range of the converter.

Oversampling converters sample at a rate much larger than the Nyquist rate for a desired input bandwidth. These converters then produce a low resolution output stream that can be converted to a higher resolution with lower bandwidth. The conversion from a high bandwidth, low resolution signal to a low bandwidth, high resolution signal, is done by a decimation filter (discussed in Section 4.8).

The delta and sigma-delta modulators can be used in oversampling converters to produce a low resolution, high bandwidth output. The delta modulator (DM) utilizes a quantizer and feedback with an integrator to determine if a signal is busy rising or falling (hence the term "delta"). In effect the modulator delivers the derivative of the input signal. It has been theoretically verified that delta-type modulators have an inherent stability [32], always attempting to track an input signal. A block diagram of this modulator type is shown in Fig. 4.8. In Fig. 4.8 and in the rest of this chapter $x(t)$ refers to

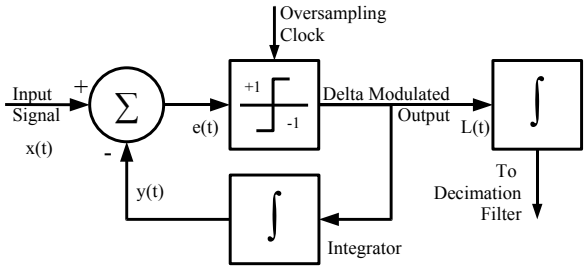


Figure 4.8: Delta modulator system

the input waveform, $y(t)$ to the estimated input signal, $e(t)$ the error signal and $L(t)$ the digital output. At the output stage integration is necessary along with an averaging filter (decimation) to obtain increased resolution. The sigma-delta modulator (SDM) is in effect a delta modulator with the output integrator shifted to the input and therefore the modulator function is the same. This allows a simplified modulator where the input signal combined with feedback can be integrated by the same component.

The sigma-delta modulators therefore have increased robustness because they are less dependent on the performance of integrators. Delta modulators are generally less popular because close-to-perfect integration is required in the feedback loop in order to obtain acceptable converter linearity [33]. Such integrators are difficult to realize in semiconductor technology [28]. Superconductors offer close-to-perfect integrators, because of natural

flux quantization, enabling practical superconductor delta modulators.

Other ADC types have been developed using superconductor electronics that have modulators that are similar to either the DM or the SDM [28]. They include the counting ADC based on a voltage-to-frequency converter [34], the counting ADC based on flux quantization [35] and the Phase-Modulation-Demodulation (PMD) delta ADC [36]. Some superconductor DMs and SDMs use synchronous quantizers while other similar architectures separate the quantization and sampling process.

To date, the most successful oversampling superconducting ADCs are the PMD type. Many ADCs have been developed and successfully tested using the PMD technique [36, 37, 38, 39]. With the PMD type modulator (basic block diagram is presented in Fig. 4.9), a constant flow of flux is added to the quantizer current loop. The phase of the constant input flux is modulated by the input signal according to its derivative (delta modulation). The quantizer is followed by a synchronizer where the sampling process takes place. The synchronizer determines the presence or absence of a pulse within a certain sampling period. This effectively increases the number of quantization levels.

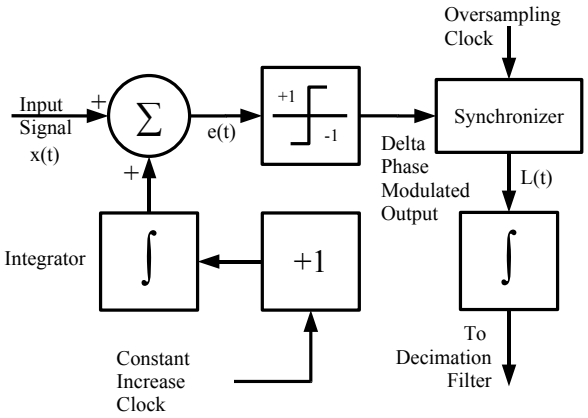


Figure 4.9: A PMD delta modulator system

4.6 Increasing Modulator Dynamic Range

Superconductor oversampling ADC dynamic range (DR) is affected by the oversampling rate, modulator order and number of quantization levels. With significant increases in the oversampling rate of a first-order ADC with single level quantizer, the modulator DR is increased by much less significant amounts. Therefore many techniques have been developed to increase modulator order and quantization levels. Semiconductor technology

offer numerous techniques that are much more complex to implement with superconductor technology. Some specific architectures produce results with increased performance. The PMD modulator is probably the most successful superconducting oversampling modulator to date because of a multi-channel synchronizer method that effectively increases the number of quantization levels [38]. Attempts to increase the superconductor sigma-delta modulator order [40] have revealed a great increase in complexity because of losses in R-L filters used for integration. Such a second order modulator requires large amounts of feedback gain in a short period of time [40]. Similarly, increasing the quantization levels in the delta modulator by incorporating a simple flash-type ADC as quantizer would greatly increase the modulator feedback complexity because of current amplification requirements. The delta modulator order can effectively be increased by SFQ pulse multiplication in the feedback loop (relates to current amplification) [41].

4.7 Modulator Evaluations

A simple delta modulator is evaluated first before an advanced SFQ-counting delta modulator is presented and evaluated. Firstly maximum input waveform characteristics are defined according to specified ADC requirements. The defined waveform is then used in all circuit models and device level models to allow for effective comparison. Device level simulations are done with MATLAB [42] and circuit simulations are done using WRSpice [21]. All device level simulations use quantizer and feedback models as defined in Section 4.4.1 and 4.4.2.

4.7.1 Modulator Input Signal Specification

An input signal frequency and amplitude relationship is defined for ADC operation in the linear region (ADC not overloaded with input signal). Both the classic delta and advanced delta modulator produce a binary coded derivative of the input signal at the output. The maximum range of both modulators is therefore determined by the signal slope (slew rate).

Modulator quantization levels (N_q) are also taken into account. Assuming perfect integration, the feedback of the modulator causes increases or decreases of a fixed amount (γ) per sampling clock (f_s) period. Increase in N_q increases the number of γ-feedbacks possible. The maximum rate of the feedback signal (also the output signal) is therefore

$$\zeta = \gamma N_q / T_s = \gamma N_q f_s \tag{4.4}$$

For an input waveform ($x(t)$) with amplitude (A_m), frequency (f_m) and phase shift ($\phi(t)$),

$$x(t) = A_m sin(2\pi f_m t + \phi(t)) \ .$$

For the input waveform with a derivative of

$$x'(t) = A_m[2\pi f_m + \phi'(t)]cos(2\pi f_m t + \phi(t))$$

and $\phi'(t) = 0$, the condition of slope overload is generally avoided when

$$A_m 2\pi f_m \leq \gamma N_q f_s$$

so that the maximum slope of the input signal ($A_m 2\pi f_m$) is smaller than the required maximum rate of input signal change stated in Equation 4.4. The superconductor modulators are operated at a sampling frequency (f_s) of 20 GHz and feedback occurs in quantized amounts of $\gamma = \Phi_0/L_{loop}$ as explained in Section 4.4.1. Slope overload in a superconducting delta modulator with a specific loop inductance (L_{loop}), is therefore prevented when

$$A_m \leq \frac{\Phi_0 N_q f_s}{2\pi f_m L_{loop}} \tag{4.5}$$

In sampling systems, according to the Nyquist-Shannon sampling theorem, the output sample rate must be greater than the Nyquist rate ($2f_m$) for perfect input signal reconstruction (without aliasing components). Here f_m represents the maximum frequency component of a certain bandwidth, therefore f_m also refers to the input signal bandwidth. At ADC output sample rates above, but close to the Nyquist rate, the reconstructed waveform amplitude is dependent on the relative phase of the input waveform. This results in unreliable signal reconstruction. For reliable reconstruction of the input, the modulator and ADC models are designed for $f_m$but input signals are only tested up to $f_{sig} = f_m/2$. Although designed for f_m, the full potential of these modulators are explored by allowing input waveform amplitudes (A_{sig}) with f_{sig} as presented in Fig 4.11.

For the ADC to produce the digitized input waveform at a rate larger that the Nyquist rate (decimated), the resolution of the ADC is limited because only a limited number of γ-steps are possible to count within an output sample period. The ADC maximum output resolution (after decimation) is limited by f_s, f_m and the number of modulator quantization levels (N_q). In the oversampled converter the following number of N_q-bit

samples (N_s) are produced per input waveform period:

$$N_s = \frac{f_s}{f_m}$$

As seen in Fig. 4.10 the maximum peak-to-peak rising change in a triangular input waveform (no slope overload) produces the following number of output pulses (B_{out}):

$$B_{out} = \frac{N_s}{2} \times 2^{N_q - 1}$$

For the maximum input sine waveform the effective number of output pulses are cosine

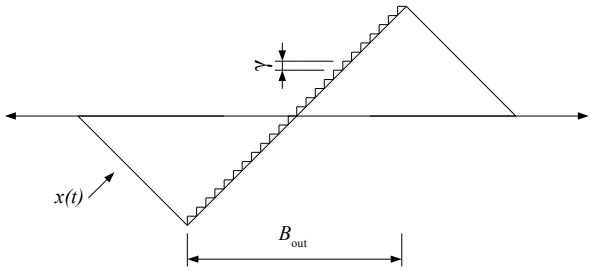


Figure 4.10: ADC modulator maximum number of quantizations for triangular input waveform

dependent. For a sine waveform the number of output pulses (B_{out}) for a maximum peak-to-peak rise is:

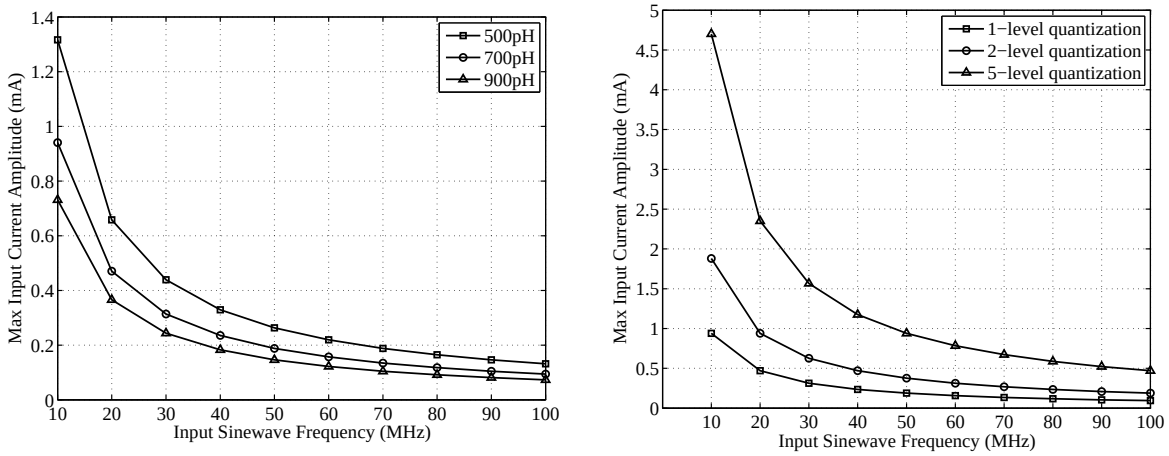
$$B_{out} = 2^{N_q - 1} \times \sum_{k=0}^{N_s/2} \mid cos(2\pi f_m k T_s) \mid \tag{4.6}$$

Therefore, the maximum resolution is limited by the maximum number of output pulses and modulator quantization levels. The number of output pulses are converted to resolution as follows:

$$n = log_2(B_{out}) \tag{4.7}$$

At this stage it is important to note that increased ADC output resolutions are possible when the input waveform frequency is much lower than the input frequency that the modulator is designed for (eg. at $f_{sig} = f_m/2$). The number n then refers to the maximum resolution of output signal change per output signal sample. The larger input amplitude (A_{sig}) is possible when using a digital integrator at the output with a larger output resolution than n. The maximum allowed resolution for a sine waveform of frequency f_{sig} is as shown in Fig. 4.12.

The design of an oversampling superconductor delta ADC operated at 20 GHz with single- or multi-level quantization is aided by Eq. 4.5, Eq. 4.6 and Eq. 4.7. Eq. 4.5 is used to produce Fig. 4.11, where the relationship between the input waveform frequency and maximum modulator input current is shown for different values of L_{loop} and N_q. Fig.



(a) Nq = 1 (b) L = 700pH

Figure 4.11: Delta ADC modulator input waveform frequency in relation to the maximum allowed input current amplitude

4.12 is produced by Eq. 4.6 and Eq. 4.7. The figure shows maximum ADC output resolution in relation to the input waveform frequency for different quantization levels (N_q). The input signal to the ADC is selected according to the results produced in Fig.

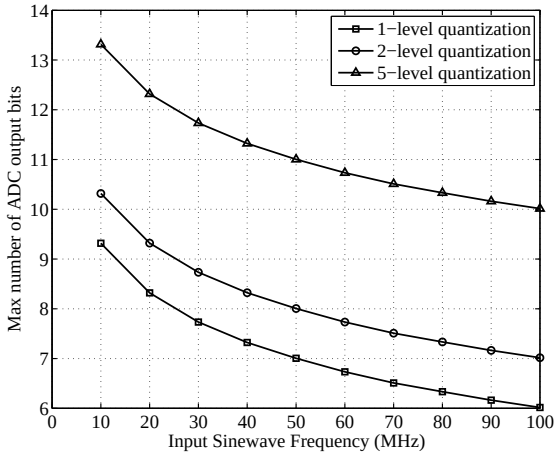


Figure 4.12: Delta ADC modulator input waveform frequency in relation to maximum output resolution of the ADC (L_{loop}=700pH)

4.11 and Fig. 4.12. In order to limit circuit simulation times, all WRspice circuit models are designed for $f_m = 100$ MHz and supplied with an input sine waveform of $f_{sig} \leq f_m/2$ with a maximum input current amplitude as shown in Fig. 4.11. In MATLAB, model evaluations are done for various input waveforms (mostly at maximum slew rate).

Superconducting ADC modulators obtain input waveforms through an inductively coupled structure which is matched to a 50 Ω input impedance for input from an LNA or directly from an antenna. All input amplitudes are designed for an inductively coupled structure with ideal coupling ($k = 1$). For a lossy inductive coupling the maximum input amplitude is allowed to be $\frac{1}{k}$ times the specified input current value.

In the modulator evaluations all input signals are converted to and compared in dBm. Input signal current amplitudes are converted to power figures in relation to a 50 Ω load. Eq. 4.8 and 4.9 is used for the conversions.

$$P_{mW} = \frac{I^2}{50\,\Omega} \times 10^3\, mW \tag{4.8}$$

$$P_{dBm} = 10 log_{10}(P_{mW}) \tag{4.9}$$

The average power per ohm for a sinusoidal waveform is $A^2/2$ where A is the zero-to-peak amplitude of the waveform [7].

4.7.2 Delta Modulator Implementation

Basic Idea

The delta modulator design is based on the early Pulse Delta Modulator (PDM) [43], SFQ-counting ADC [44] and the feedback concepts demonstrated in Sections 4.4.1 and 4.4.2. A diagram of a first-order delta modulator was given in Fig. 4.8 and an equivalent superconductor circuit of such a modulator containing all necessary feedback effects, is given in Fig. 4.13. This superconducting delta modulator will, with the rise of an incoming analogue signal produce an SFQ pulse at the output of the synchronous comparator formed by J_1 and J_2. This "switching" action of the junction is followed by the natural reduction of current in the superconducting loop, as discussed in Section 4.4.1. This reduction always occurs in exact, quantized amounts of Φ_0/L, where L is the total loop inductance. This occurrence corresponds to the feedback, integration and subtraction required in a delta modulator when a rising input signal is applied. The loop is formed by J_1 , L_{p1} , L_2 , L_F and the input inductance and JJ of JTL_1. When omitting the relatively small inductance of JJs and parasitic elements, the loop inductance is roughly equal to $L_F + L_2$. With a

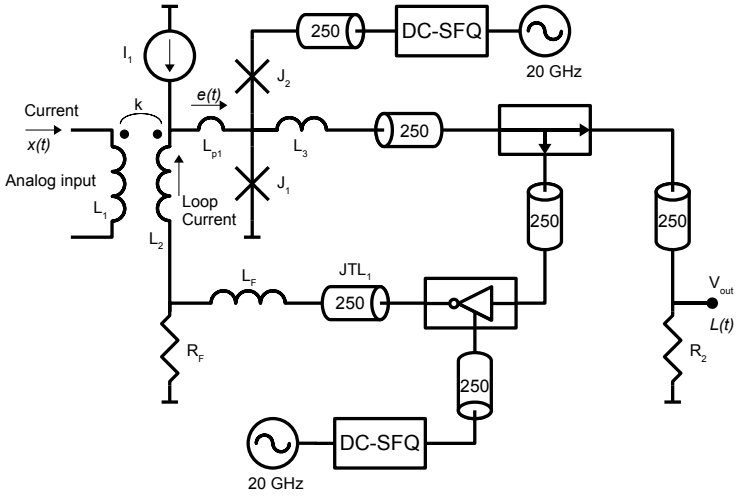


Figure 4.13: Circuit details of a superconducting delta ADC. Parameter values are as follows: $J_1 = J_2 = 250\,\mu A$, $L_1 = 1.2\,nH$, $L_2 = 500\,pH$, $k = 0.5$, $L_3 = 3\,pH$, $L_F = 200\,pH$, $R_F = 2\,\Omega$, $R_2 = 10\,\Omega$ and $I_1 = 40\,\mu A$.

decreasing input signal, the current in the superconducting loop is increased. In this case, the comparator does not produce an output SFQ pulse and an inverting circuit is used to produce a pulse that is integrated into the modulator loop by a first-order R-L LPF, increasing the current as demonstrated in Section 4.4.2. When a DC signal is applied, this modulator will repeatedly increase and decrease the loop current around the comparator threshold, clearly showing quantization noise. By the process of precise current increase and decrease through SFQ pulses, linear analogue to digital modulation is made possible.

When current levels are above the quantizer threshold, the superconductor comparator instantaneously decreases current in the superconducting loop and is used as part of the feedback in a delta modulator. Optimally increasing the current when no pulses are produced at the comparator is a more complex and difficult task, because the feedback parameters influence the modulator dynamic range. The low-pass filter and feedback delay must therefore be optimized for maximum modulator dynamic range. The resistive (R_F) and inductive (L_F) elements of the LPF influence the modulator in different ways. The loop inductance ($L_{loop} = L_2 + L_F$) is chosen so that the quantizer is unresponsive to thermal noise, but responsive to the smallest possible signals in order to keep receiver amplification minimal. The loop inductance also determines the ADC maximum input current characteristics as described in Section 4.7.1. The resistance is then primarily used to shift the filter cut-off frequency to an optimal position. If the filter response is too fast, quantization noise is increased as result of feedback latency. Slow filter response can lead to distortion because of hysteresis. The ideal LPF is one causing minimal hysteresis

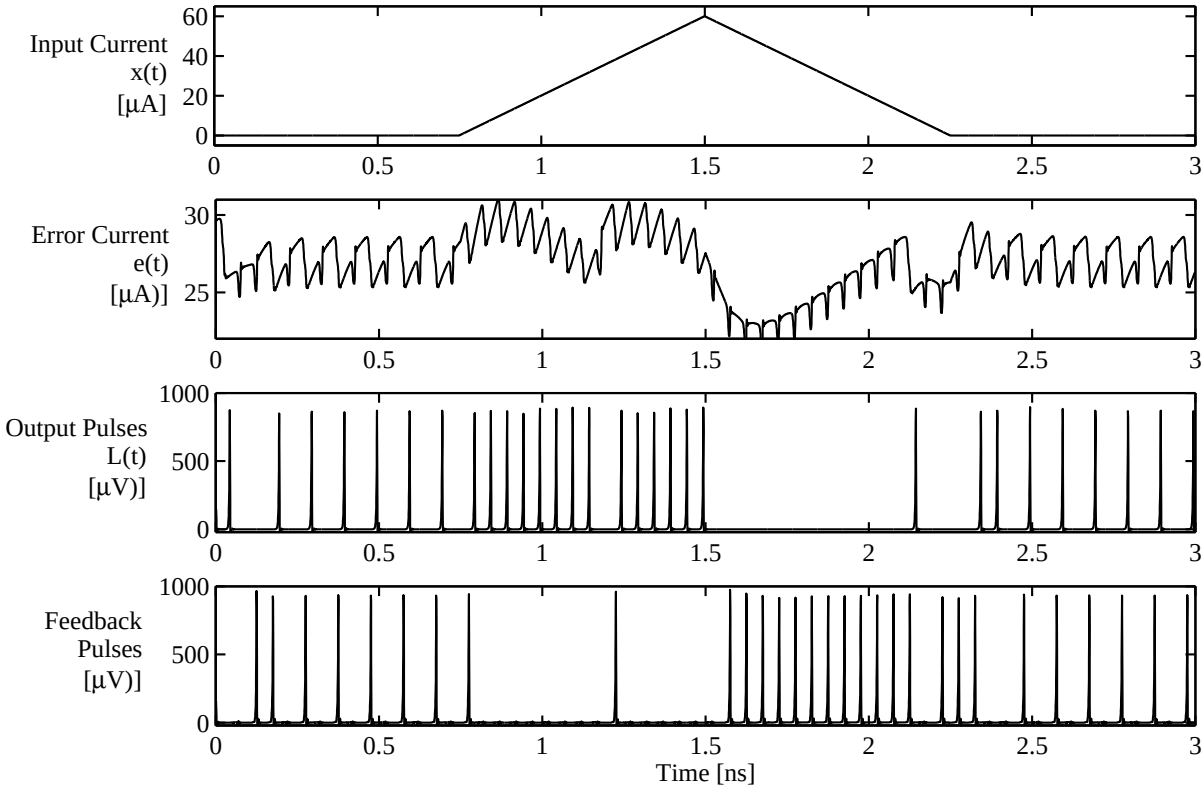


Figure 4.14: Circuit responses of the delta modulator simulation.

while optimizing quantization noise. Dynamic range evaluations and filter optimization are done in Section 4.7.2 using the filter model from Section 4.4.2 and a device level model of the modulator.

Circuit Simulation

Shown in Fig. 4.14 is the circuit simulation results of the delta modulator seen in Fig. 4.13. Note that the $e(t)$ error current remains stable when no input signal is applied. An increase in the input signal causes the increases in the amount of loop current subtractions and an increase in SFQ-pulses at the modulator output. A reduction in the applied input signal then causes the slower current increases seen in the loop current. The increase in feedback pulses are clearly seen, along with the decrease of output pulses. This result is produced to demonstrate the operation of the circuit with ideal quantization noise ($\pm\gamma$).

With the circuit sensitivity fixed (L_2 and L_F fixed) a quantization noise evaluation is done for different values of R_F. In Fig. 4.15 the steady state $e(t)$ results are shown for different R_F values when no input current is applied. From these evaluations it clear that lower R_F values produce a more constant feedback current slope. Each current

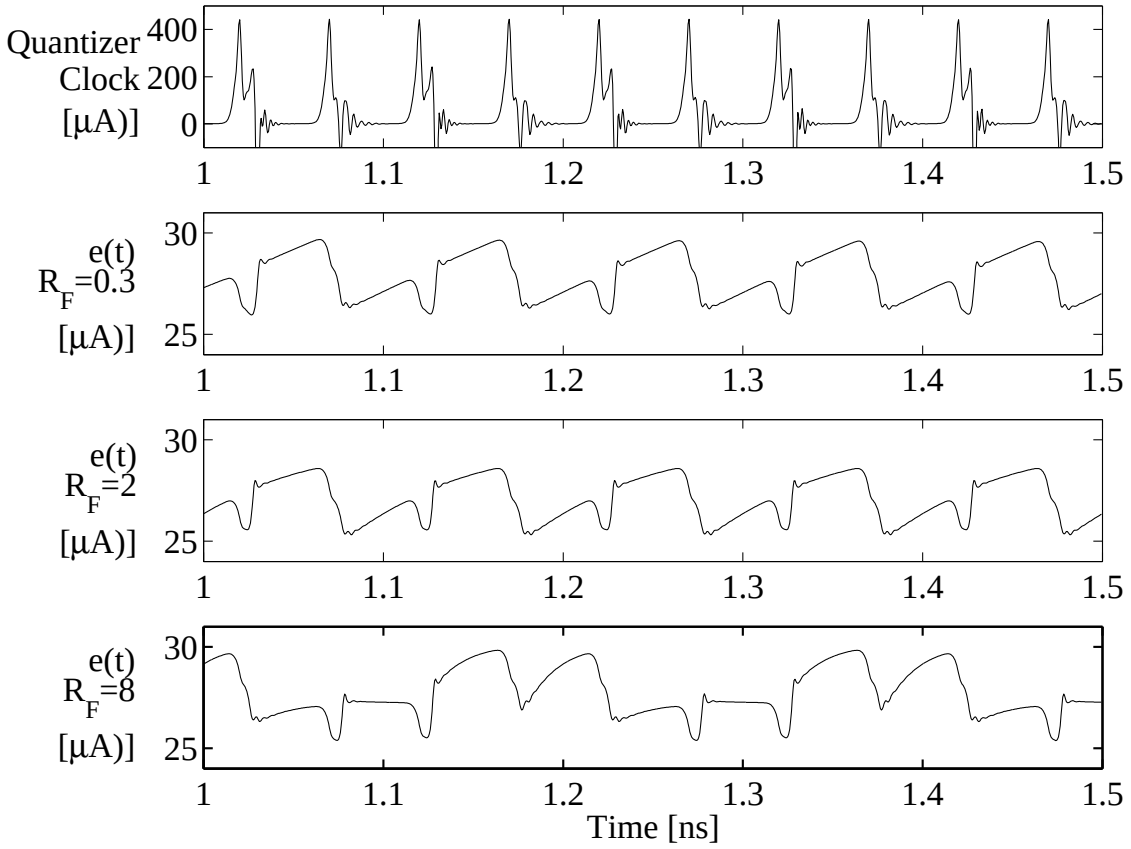


Figure 4.15: Circuit responses for the delta modulator at steady state with no input current and different LPF resistance values.

decrease related to the immediate decrease of γ. Each current increase is subject to circuit latency and it is difficult to rapidly increase the loop current at the correct instances as shown with $R_F = 8\,\Omega$. For minimum quantization noise, a constant injection of $\gamma/2$ per clock period is therefore considered optimal. With $R_F = 0.3\,\Omega$ this optimal condition is obtained, but further circuit evaluations show current build-up (hysteresis) when the input current has fallen at maximum slew rate. This hysteresis effect influences the modulator output for up to 500ps after the input is restored to have no input current. The effect is therefore considered a source of distortion. With larger resistance values such as $R_F = 2\,\Omega$ an improved hysteresis to current injection combination is obtained, allowing optimal quantization noise with minimal hysteresis.

Modelling and Dynamic Range Evaluations

A model of the delta modulator is presented in Fig. 4.16. This model is compared with the WRspice circuit simulation results when using similar sampling and component values.

The model consists out of the following:

- Quantizer - Detects whether $e(t)$ is above the pre-defined quantization level. This level is dependent on JJ area, JJ biasing current and quantizer clock pulse characteristics. The level is constant for the ideal circuit model. Bias current fluctuations and quantizer clock pulse characteristics should be considered in a more realistic model. JJ area variations would only influence the quantizer level value and does not influence modulator performance. The quantizer level selected is determined by the circuit simulation. The quantizer delivers an output serial stream of binary values $L(k)$.
- The implicit reduction of loop current when $e(t)$ is above the quantizer level is modelled as explained in Section 4.4.1.
- When the output bit from the quantizer is zero, a comparator produces a binary 'one' ($\overline{L(k)}$). This comparator output is then converted to feedback current $y(t)$ which is an estimate of the input current. The feedback current is implemented as $\gamma/2$ ($0.5\Phi_0/L$) increases per clock period as described for the ideal LPF filter in Section 4.7.2.

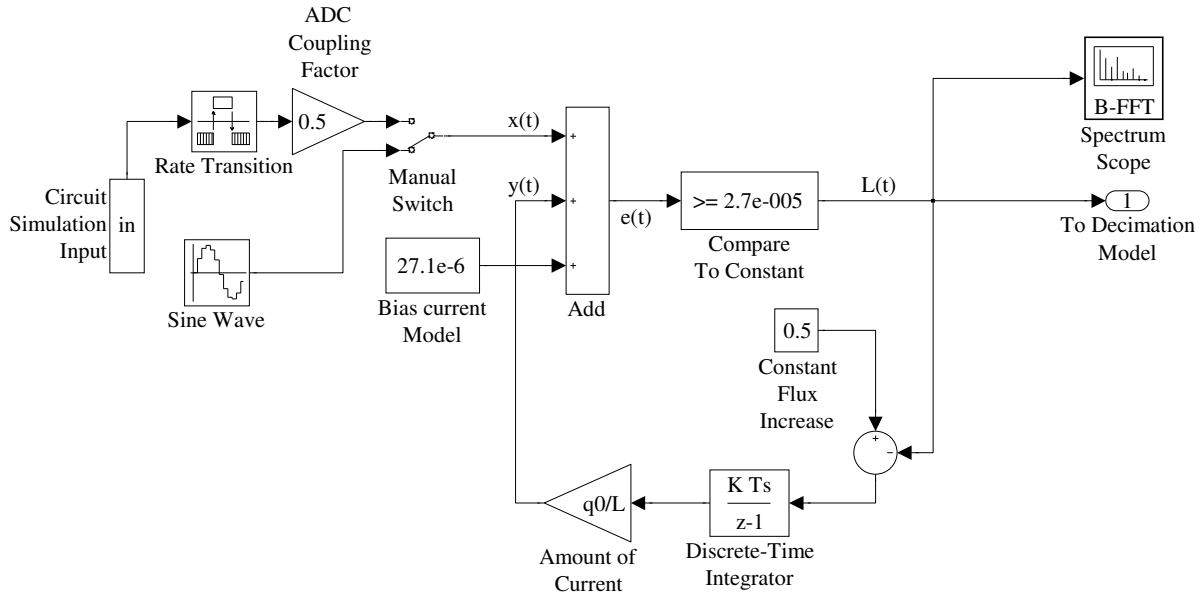


Figure 4.16: MATLAB model diagram of the Delta modulator

The input $x(t)$, error signal $e(t)$ and binary outputs $L(k)$ are compared between the circuit simulations and model simulations. These are shown in Fig. 4.17 and Fig. 4.18. The $e(t)$

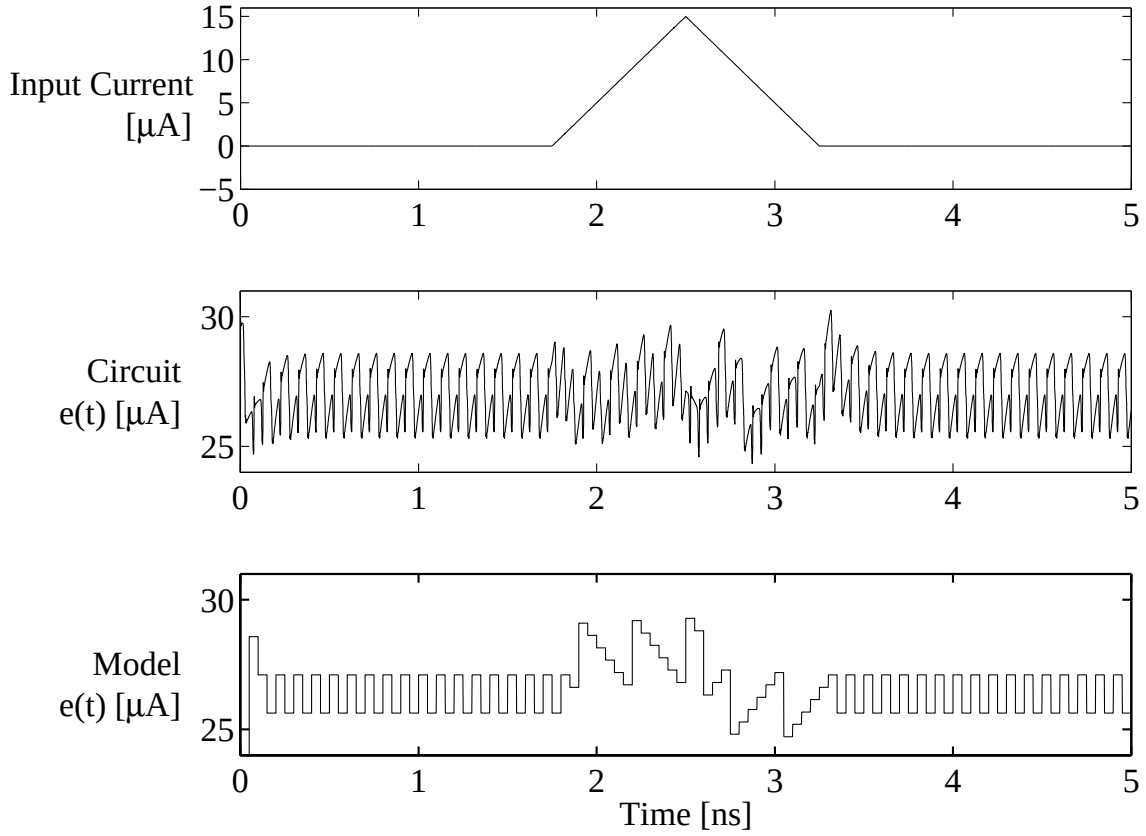


Figure 4.17: Delta modulator circuit and model comparison of $e(t)$currents

waveform for the model is smaller than the waveform for the circuit. This is attributed to the difference between a continuous time system and a discrete time model. In the discrete model, increases and decreases are simultaneously calculated at each sample while in the circuit simulation results in-between current changes are clearly seen.

From the comparison it is clear that the model output closely approximates the circuit simulation output. Differences in the output are attributed to the non-ideal filter loading curves of the circuit as shown in Fig. 4.15. The model can therefore be used for optimization purposes and dynamic range evaluations. Non-ideal superconductor DM effects such as filter characteristics can also be added to the model.

The spectrum of the model output for an input waveform of 9.55 MHz at maximum slew rate is presented in Fig. 4.19. The maximum slew rate is found to occur for a sine input current at about $I_{max} = 963\,\mu A_{pk-pk}$, which closely relates to the specifications in Section 4.7.1 and Fig. 4.11. The average input waveform power per 50 Ω is then $-53.18\,dBm$. An averaged spectrum is calculated from 7 consecutive 32768-point FFT results. In the figure the low frequency component of the input waveform is visible along

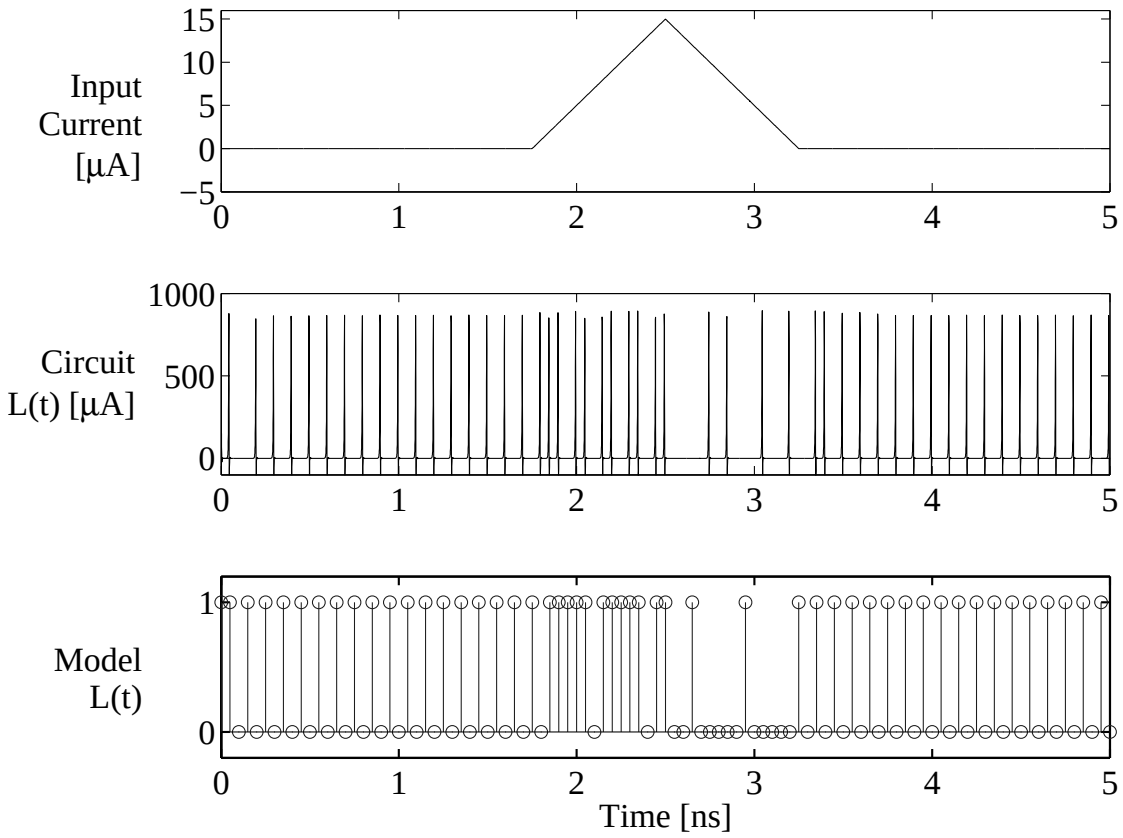


Figure 4.18: Delta modulator circuit and model comparison of $L(t)$ binary output

with the high frequency noise from the modulator. The SNR of low frequency components can be increased by the use of a decimation filter.

4.7.3 An Advanced SFQ-counting Delta Modulator Implementation

Basic Idea

The advanced SFQ-counting delta modulator is based on an asynchronous quantizer and is therefore termed an asynchronous delta modulator (ADM). The ADM is based on the old asynchronous pulse delta modulator (PDM) [43]. In the PDM seen in Fig. 4.20, an output voltage pulse is produced when the input to the quantizer rises above a certain level. An RC filter is used to filter the voltage pulse and in effect subtract a fixed amount of current via a feedback loop. Capacitor C is charged with a voltage representing an estimation of the input signal. C constantly discharges, resulting in a constant increase at $e(t)$. The superconductor ADM differs from the asynchronous PDM in that fixed

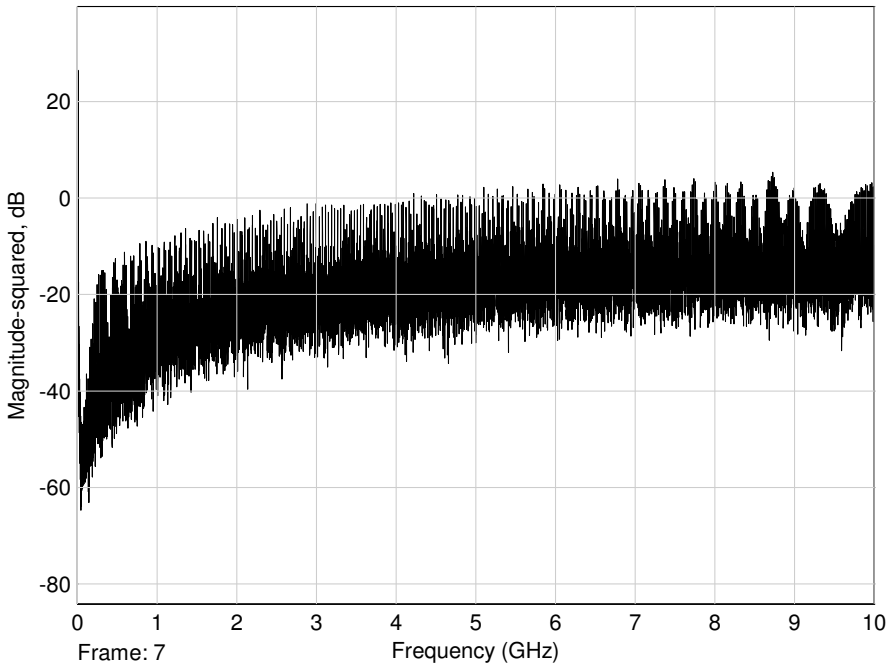


Figure 4.19: The simulated spectrum of the DM model output for a 9.55 MHz input waveform at maximum slew rate.

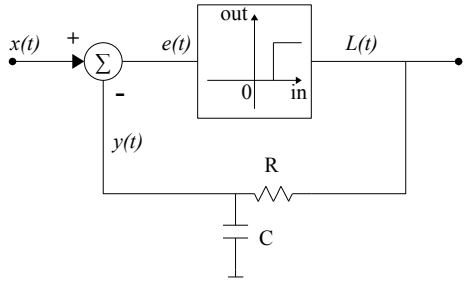


Figure 4.20: Asynchronous PDM system

amount of current decreases are implicit with a JJ quantizer as explained in Section 4.4.1. Therefore, no additional feedback loop is required. Current increases at $e(t)$ are achieved by flux injection at a fixed rate. Such constant addition of flux is similar to the PDMs constant capacitor voltage level decreases that lead to $e(t)$ increases. Output pulses from this superconductor ADM can then be synchronized by a DRO and counted (integrated) in a similar way as with the classic synchronous delta modulator.

With the ADM the amount of flux produced by the quantizer is not limited as in the synchronous quantizer from the DM in Section 4.7.2. Flux exceeding Φ_0 can therefore be produced within a single clock period. The amount of flux is quantized ($m\Phi_0$) and

can be counted in an m-channel synchronizer. Fig. 4.21 shows a 2-channel synchronizer architecture, proposed for the ADM. The values of the circuit components shown in Fig.

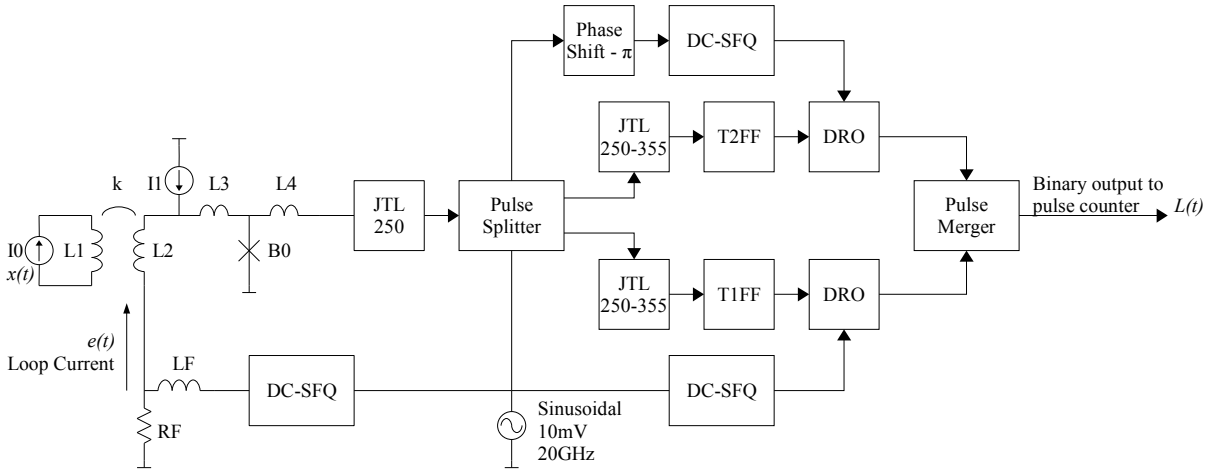


Figure 4.21: The proposed ADM architecture

4.21 are as follows: $B_0 = 250\,\mu A$, $L_1 = 1.2\,nH$, $L_2 = 500\,pH$, $k = 0.5$, $L_3 = 1\,pH$, $L_4 = 3\,pH$, $L_F = 200\,pH$, $R_F = 2\,\Omega$, and $I_1 = 290\,\mu A$. The ADM can receive SFQ pulses at a rate exceeding the clock frequency of the circuit. In the 2-channel synchronizer, a T1FF and T2FF is used to determine the number of pulses from the quantizer. These TFFs are asynchronous and are both accompanied by a DRO to obtain synchronous outputs. The DROs are clocked with a phase difference (π) to allow effective operation of the fast pulse splitter and binary counter. The two-phase clocking structure effectively results in a modulator with 2 quantization threshold levels, where output values are binary representations of the numbers 0, 1 or 2. Outputs containing only 1's indicate that the input signal is not changing. When containing only 0's the input signal is estimated to decrease at maximum rate and when containing only 2's the input signal is estimated to be rising at maximum rate.

Circuit Simulation

From the circuit simulation results in Fig. 4.22 it is clear how different outputs are produced for different slopes of an input signal. For the input, chosen to be at approximately maximum slew rate, it is seen that the $e(t)$ current is within the ideal range of $\pm\gamma$ around the JJ threshold. Here $\gamma = \pm\Phi_0/(L_F + L_2) \approx 2.96\,\mu A$.

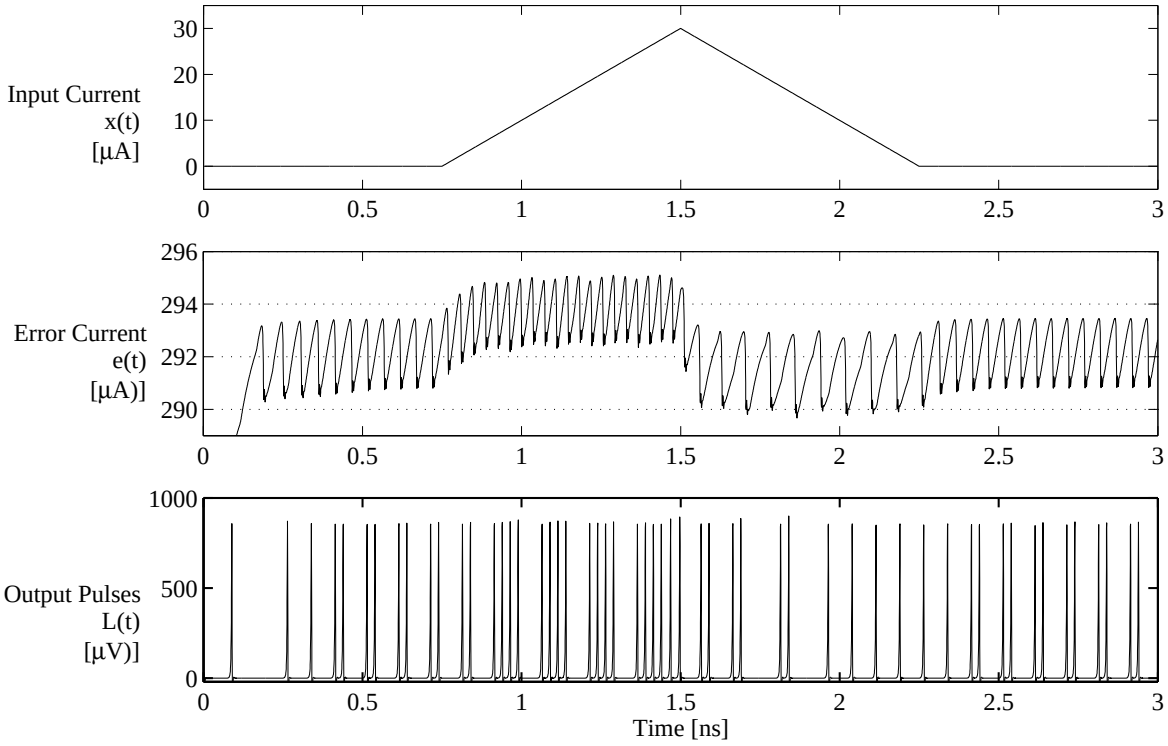


Figure 4.22: ADM modulator circuit simulation results for a simple input waveform.

Modelling and Dynamic Range Evaluations

Accurate modelling of an asynchronous modulator is a difficult task because the quantizer produces SFQ pulses at arbitrary time instances depending on JJ characteristics. A simplified model is therefore presented for comparison with the circuit simulation results. The simplified model components are as follows:

- Quantizer: The total amount of flux increase or decrease from the input waveform is taken into account along with the flux that is synchronously added through the LPF. The amount of current is periodically quantized (multiples of Φ_0/L) and the remainder of current is used in the next quantification.

- Synchronizer: Flux in the proposed quantizer model is periodically quantized and therefore the synchronizer model is greatly simplified. An excess of flux occurs when overloading the modulator with an input waveform that exceeds the maximum slew rate. The synchronizer prevents excess flux from being sent to the ADC pulse counter. This is done by allowing a maximum modulator output of 2 SFQ pulses for the two channel synchronizer. The redundant pulses cause the T1FF and T2FF to alternately produce an output, but these pulses are consumed when the DRO is

already set. This effect is modelled by the saturation of the number of input pulses from the quantizer. Saturation causes signal distortion and is monitored in the DR evaluations.

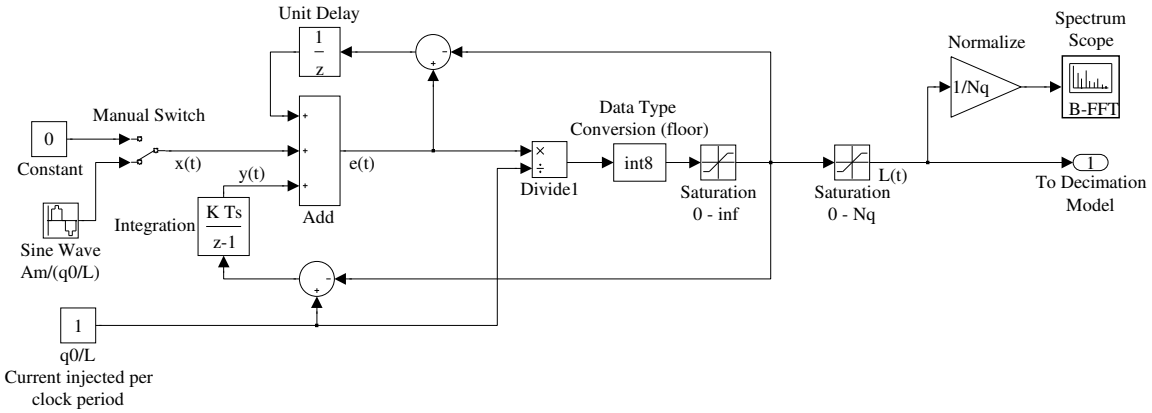


Figure 4.23: A model for the superconductor ADM modulator

The model is presented in Fig. 4.23. The quantizer parameters are all normalized by quantized units of current (Φ_0/L). Simulation results showing the number of output SFQ pulses before saturation for an input waveform at maximum slew rate is shown in Fig. 4.24. A normalized input waveform is also added to this figure as reference. The spectrum

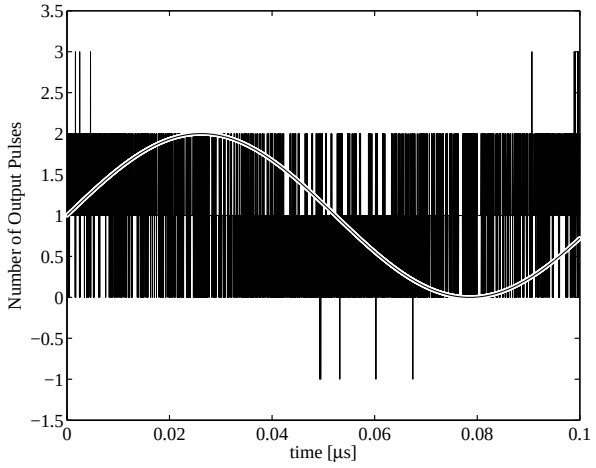
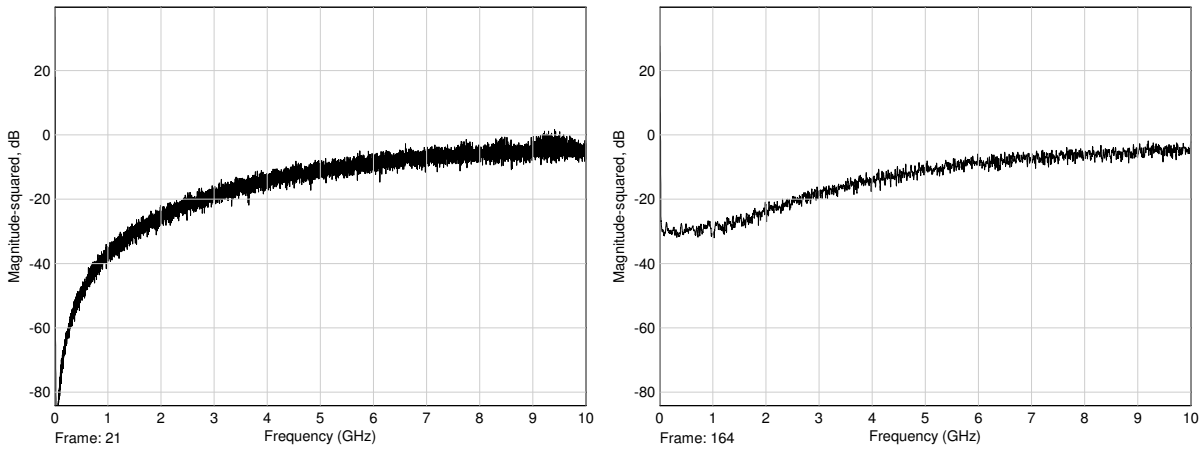


Figure 4.24: The ADM quantizer model showing the number of output SFQ pulses for an input waveform at maximum slew rate

of the unsaturated model output for an input waveform of 9.55 MHz at maximum slew rate is presented in Fig. 4.25. The maximum slew rate is found to occur for a sine input

current at about $I_{max} = 481\,\mu A_{pk-pk}$. The average input waveform power per 50 Ω load is then $-59.37\,dBm$. Small excessive flux bursts were observed from very small input signal powers. These bursts are observed in time domain analysis (see Fig. 4.24) when no model saturation effects are applied. The inherent saturation effects of the ADM design limits the DR of this modulator. The averaged spectrum output for both the saturated and non-saturated modulator is calculated from 16 consecutive 32768-point FFT results, using a 'Blackman' window. In the figure the low frequency component of the input waveform is visible along with the high frequency noise from the modulator. The excessive flux bursts



(a) Without saturation (b) With saturation

Figure 4.25: The simulated spectrum of the ADM model output for a 9.55 MHz input waveform at maximum slew rate.

seen in Fig. 4.24 may seem insignificant, but DR evaluations show that the saturation of such excess flux has a large influence on the DR of the modulator. The SNR of low frequency components can be increased by the use of a decimation filter.

4.7.4 DM and ADM Comparison

The ADM modulator and classic delta modulator evaluations deliver results that can be compared. Each of the modulators have its own advantages and disadvantages. A few modulator characteristics are compared:

- Sensitivity: The ADM shows increased sensitivity because of the high constant current increase in the asynchronous quantizer. This sensitivity along with the asynchronous quantizer easily produces increased bursts that cause saturation in the synchronizers. This limits the DR of the ADM and neutralises the advantages

of the increased sensitivity. The DM shows less sensitivity, but improved DR at the lower frequencies of the output spectrum.

- Circuit Complexity: The DM is a relatively simple circuit allowing fast and reliable implementations. Performance degradation of the DM is caused by the build-up of flux that causes output signal distortion. Although the ADM has increased sensitivity over the DM, the circuit is more complex. The ADM linearity for a certain input signal range is subject to the complexity of the multi-channel synchronizer.

- Quantizer levels: Both modulators have single-level quantizers, but the ADM delivers an 2-bit output.

4.8 Decimation filter

Basic Idea

As decimation filters can become relatively large structures [45], superconductors need to be used as effective as possible in order to produce acceptably sized structures. Particularly with current commercial fabrication processes, space and distance are limiting factors in superconducting integrated circuits (ICs). The process of decimation is examined to provide a simplified superconductor decimation architecture that occupies less space on the chip.

The modulated bit-stream from the delta-modulator needs to be demodulated via integration, because differential signals are given by the delta modulator. Along with integration, the signal must be averaged to provide the ADC resolution. As seen in Fig. 4.26(a), conventional decimators perform integration at the oversampling rate and an averaging FIR filter follows. This is done in order to take advantage of the frequency rejection properties of digital filters to prevent aliasing, especially when using programmable decimation architecture to selectively obtain different frequency channels (as indicated in Fig. 4.26(a) by the numbers 1 to 3). Generally, first-order Sinc filters (also known as rectangular filters) are used for the signal averaging (filtering) process [28]. In such architectures, analogue wideband anti-aliasing filters are implemented before the oversampling modulator [46]. This is generally a low-pass filter with a cut-off frequency above the Nyquist rate of $f_s/2$, where f_s is the oversampling frequency (see Fig. 4.26(a)). To save space and keep complexity low on superconductor chips, the filtering function of the digital decimation structure can be shifted to the analogue anti-aliasing pre-filter (as shown in Fig. 4.26(b)). This reduces programmability and possible sample rates of the ADC, but greatly simplifies

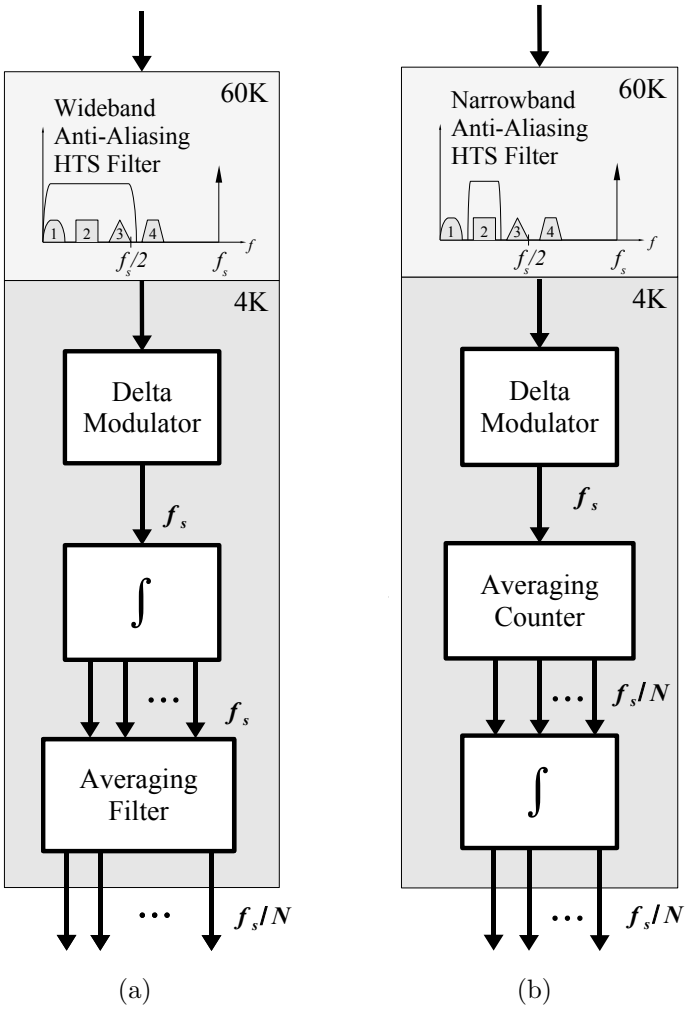


Figure 4.26: The (a) conventional and (b) proposed, simplified decimation filter architecture. Both are shown with anti-aliasing pre-filters.

the design for applications where wide bandwidth channels at fixed frequencies are to be digitized. Such an analogue filter requires a relatively narrow bandwidth (relative to the oversampling frequency) and good out-of-band frequency rejection. Oversampling ADC modulators for wireless communications may have dynamic ranges greater than 100 dB [47] and therefore analogue filters of high order are required to suppress the out-of-band frequencies enough to prevent aliasing. High temperature superconducting (HTS) analogue filters are capable of meeting these requirements [6] with high selectivity, excellent out-of-band frequency rejection and low insertion loss. These filters outperform conventional filters of similar order, and because superconducting ADCs require a cryogenic environment, operating temperatures for HTS filters are readily available. The proposed decimation filter is therefore built around the advantages that HTS analogue filters offer.

With the HTS filter suppressing the frequency components that could cause aliasing, samples from the delta modulator can now simply be accumulated to form a differential average as shown in Fig. 4.26(b). Following the accumulation is the integration of those values, implemented as the addition and subtraction of averages. Firstly, the accumulation process (averaging) and integration process are described separately before the complete RSFQ decimator design is presented, modelled and simulated.

Accumulation of output from ADC modulator

The serial or low resolution output bit stream from a delta modulator is accumulated to produce an average value that is integrated in order to complete the design of a delta ADC. For the accumulation, a ripple adder, consisting of RSFQ T2FF elements, is used to average the fast changing input bits. The accumulated values are then used to indicate the magnitude by which the input waveform is increasing or decreasing. The values contained in the accumulation register are therefore mapped to represent signed values. The mapping for a 6-bit accumulation register is shown in Fig. 4.27. According to the

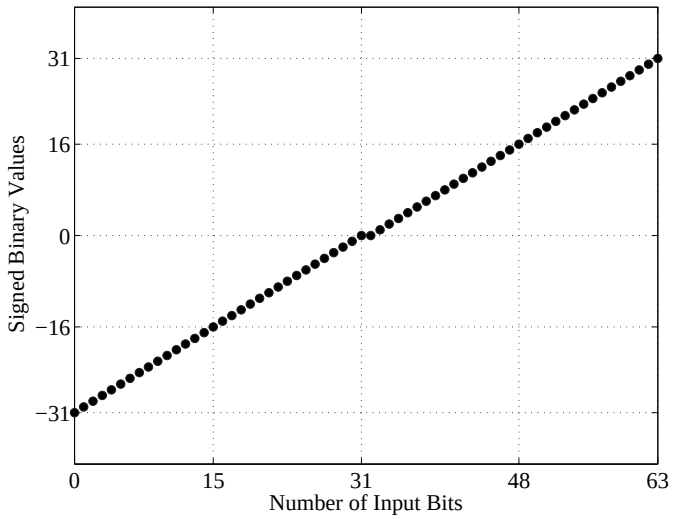


Figure 4.27: The binary number representation for the acquired number of accumulator bits

mapped values, the accumulator output is similar to the one's complement form with only the MSB being a bit inversion of the standard form MSB. This number representation allows for simple addition of signed binary numbers with equal length [48]. These numbers can simply be added through normal binary addition. Whenever overflow occurs, the overflow bit is simply added to the LSB. Examples are shown in Fig. 4.28.

(+5)	0101	(-5)	1010
+ (+2)	+ 0010	+ (+2)	+ 0010
(+7)	0111	(-3)	1100
(+5)	0101	(-5)	1010
+ (-2)	+ 1101	+ (-2)	+ 1101
(+3)	1 0010	(-7)	1 0111
	↪ 1		↪ 1
	0011		1000

Figure 4.28: Examples of one's complement addition

Integration of the averaged ADC output

Averaged values from the accumulator are clocked at a much slower speed than the modulator output rate, depending on the accumulation register readout clock. The slower operation speed allows for the integration of accumulator values in either superconductor electronics or conventional semiconductor electronics.

The ADC accumulator is designed to produce averages with a resolution relating to the Nyquist frequency of the input signal bandwidth. Signal components that have a much lower frequency than the Nyquist frequency are therefore able to produce an output with a much higher resolution when the signal component is at maximum slew rate. This implies that the integration register should be larger than the accumulation register to obtain increased ADC output resolution for frequency components well below the Nyquist frequency.

The mismatch in accumulation and integration register size leads to a more complex integration structure. This is because extra bits are required when integrating negative values. These bits are therefore dependent on the inverse of the sign bit in the accumulation register. An example of such an insertion of bits is shown in Fig. 4.29. It is important to note that these operations are done with one's complement values with an inverted sign bit. In addition, the integration register is assumed to be unsigned (ADC output samples are not required to be signed). This allows for a simpler integration structure because the unsigned integration register is always positive. The integration register complexity is also further increased by the need for overflow and underflow control. Added logic is needed to detect such cases and cause the register to saturate at zero or the largest possible register value.

After evaluating the above considerations for the implementation of the decimation integrator structure, it was decided not to implement the integrator in superconductor electronics. The main reasons are as follows:

(+32)	100000		
+ (-7)	+ **0**0000	(16)	010000
	↪ **111**000	+ (7)	+ **1**111
(+25)	1 011000		↪ **000**111
	↪ 1	(23)	010111
	011001		

Figure 4.29: Example of bit insertion when adding a signed number to an unsigned number

- The ADC output sample rate is within the range of semiconductor electronics. The accumulation output is at the same rate and within range as well.
- The accumulation register size is always less than or equal to the size of the integrator register. When the integration register is larger, more bits are required over the cryogenic-to-room-temperature interface. In addition, any bit errors over this interface influence the ADC performance. The integrator output consists of more significant bits and errors to these bits may cause more degradation to the ADC performance than bit errors from the accumulation register output.
- The added complexity of a superconductor integrator is not justified for this specific lower-speed application.

Hybrid ADC architecture is therefore proposed where oversampling, modulation and averaging is done in superconductor electronics and integration in semiconductor electronics.

Decimator Modelling

A model of the simplified decimation structure is presented in Fig. 4.30. This model is designed to be connected to the output of the DM or ADM for decimated output spectrum analysis.

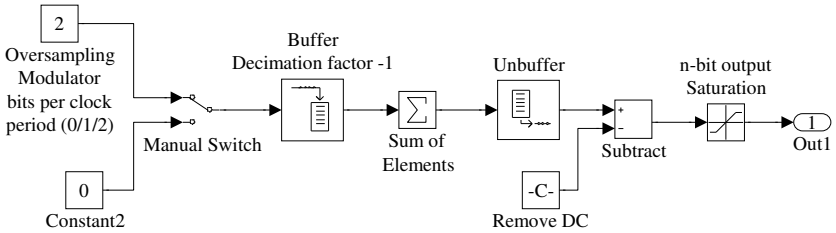


Figure 4.30: The simplified decimation filter model

4.9 ADC Dynamic Range Evaluations

Both the DM and ADM modulators are connected to the decimation filter for ADC output DR evaluations. The evaluations are done by connecting the ADC modulator models to the decimation filter model. The spectra of the ADCs are then evaluated for different input signals. Firstly DR evaluations for the two modulator designs are done with full-scale input signals. Both these designs are oversampled at 20 GHz, tested with a 9.55 MHz input sine waveform, decimated by a factor of 64 giving an output sample rate of 312.5 MS/s. The ADC output spectrum is evaluated with an FFT analysis using 'Blackman' windowing on 8192-point data acquisitions. FFT averaging for 4 sets of data is done.

Firstly an ADC using the DM is evaluated. This ADC is designed to receive signals with a maximum input power of $-53.18\,dBm$ (after coupling). The simulated output spectrum of a DM oversampling ADC with maximum input waveform is presented in Fig. 4.31. A SFDR of about 70 dB is obtained for the DM-based ADC simulation. The

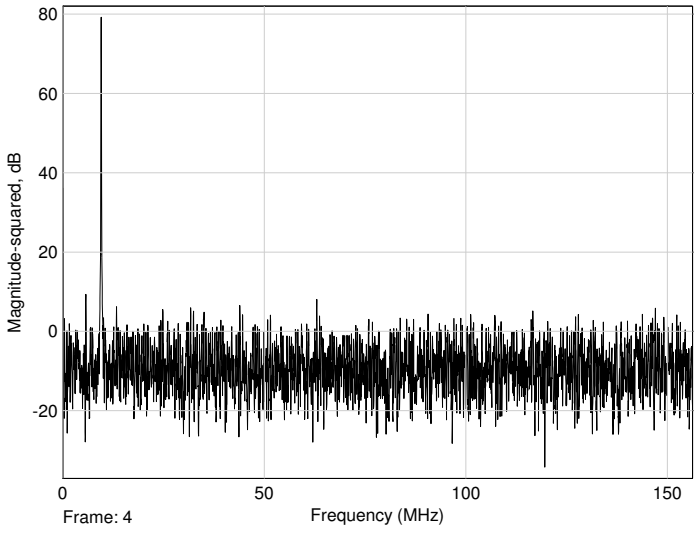


Figure 4.31: Simulated spectrum of DM-based ADC output (1:64 Decimation, 9.55 MHz input)

ADM ADC is designed to receive signals with a maximum input power $-59.37\,dBm$ (after coupling). The simulated output spectrum of a ADM oversampling ADC with maximum input waveform (value designed for) is presented Fig. 4.32. A SFDR of about 40 dB is obtained for the ADM-based ADC. As discussed in Section 4.7.4, the excess flux that is saturated by the 2-channel ADM modulator leads to a significant decrease in dynamic range with an increase harmonic distortion components.

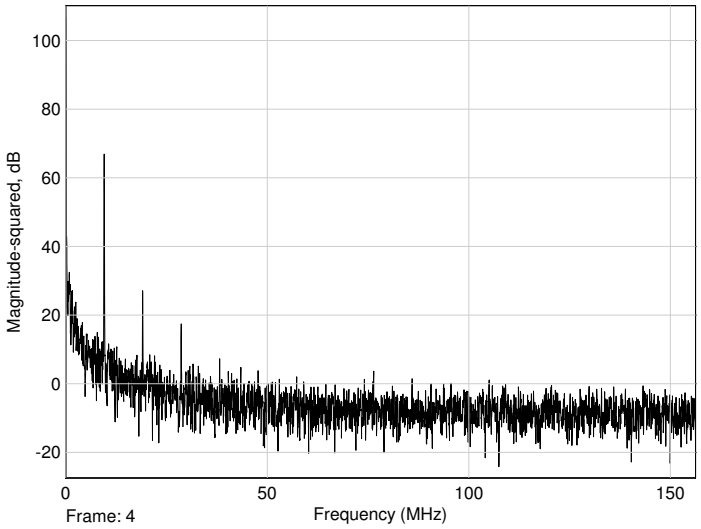


Figure 4.32: Simulated spectrum of ADM-based ADC output with 1:64 Decimation and 9.55 MHz input signal.

When compared to the SFDR results of other superconductor oversampling ADCs, it was discovered that the modulators presented in this chapter are very sensitive. To illustrate this, some of the results published by Mukhanov *et al.* [49] are compared to the results of the DM-based ADC model. The ADC by Mukhanov *et al.* is an oversampling PMD-type ADC and the results used is from a modulator clocked at 11.2 GHz, output sampling rate of 175MS/s (1:64 decimation ratio) and 10 MHz input sine wave. Acquisition of SFDR figures are done by varying input signal power to the ADC models. In Fig. 4.33 the increased sensitivity of the presented delta modulator is clearly seen. The specific DM-based modulator is able to digitize much weaker signals at acceptable dynamic ranges.

4.10 Conclusion

In this chapter several fundamentals of superconductor ADCs were covered. Basic sampling concepts were discussed before looking at superconductor ADC sampling concepts. Superconducting ADC advantages were discussed along with ADC architectures that are suitable for superconductor implementation. The main focus of the chapter is on oversampling superconductor ADCs and more specifically oversampling ADC modulators. An in-depth look was taken at the quantization and modulation in delta-type modulators. Detailed analysis of required input signals for these modulators was presented. The sen-

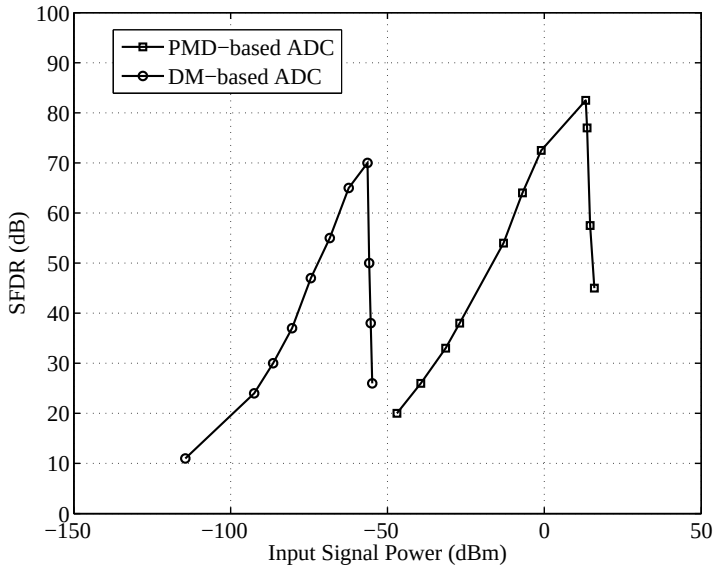


Figure 4.33: Comparison of SFDR values from spectrum evaluations of the presented DM-based ADC and measured SFDR values of a popular PMD delta ADC architecture.

sitivity of these modulators was found to be adjustable through the adjustment of certain circuit element values. Two delta type modulators were evaluated. For both these modulators RSFQ-based circuits were presented and simulated circuit responses were supplied. These circuits were then modelled in MATLAB and the model simulation results were compared with the circuit simulation results. The models were also used to evaluate and compare the output spectrum of these modulators. A simple decimation filter structure was proposed, modelled and used to decimate the modulator outputs. From this chapter the following contributions may be identified:

- An overview of superconductor ADCs along with a study of their advantages and different superconductor ADC types.
- The superconductor quantizer is modelled along with the superconductor LPF generally used for integration purposes in the feedback loop of an oversampling ADC modulator.
- A detailed specification of the ADC input waveform frequency and amplitude. The specification is for delta-type modulators which are limited by the slew rate of a received waveform.
- The designs of two different superconductor delta-type ADC modulators. Firstly a classic delta modulator design and then an advanced delta modulator design with

asynchronous quantization and multi-channel synchronizer.

- A simplified MATLAB model is presented for each modulator. These models simplify the quantum effects of the superconductor circuits to allow faster simulation times and evaluate circuits over long time periods, mainly for ADC spectrum analysis.

- A simplified superconductor based decimation filter design to allow for a relatively small circuit that produces decimated ADC output samples that can be obtained by room-temperature electronics.

The following conclusions are made from the work contributed in this chapter:

- Superconductor ADC research is an exciting and relatively new field. These converters have the potential of superior performance based on quantum accuracy and rapid sampling speeds.

- Oversampling superconductor ADC modulators offer high performance ADCs with simple high-speed circuits where sufficient resolution is obtained through decimation. Oversampling ADCs can be programmed to give a certain output resolution and bandwidth by changing the decimation filter clock signals.

- Oversampling ADC performance increases based only on the oversampling frequency are limited. Large oversampling rate increases offer relatively small DR increases. More complex modulators produce more significant DR increases. The popular PMD modulator offer such DR increases with increased complexity in multi-channel synchronizers.

- The simple DM design shows how basic superconductor quantizing and feedback techniques are implemented. The modulator is found to show the potential of oversampling converters in terms of implementation size, power consumption and programmability, but shows DR performance that would not justify the implementation of such a modulator on a cryocooled superconductor circuit. Modulators of higher complexity are therefore required.

- The ADM is based on the same modulation concept as the simple delta modulator, but the design is an attempt to improve the modulator DR by adding complexity to the synchronizer of the modulator. A two-channel synchronizer is proposed to increase the number of modulator output bits per clock period. The performance is

greatly dependent on the correct and fast operation ($2f_s$) of a few TFF elements. It was found that the asynchronous quantizer frequently produces more output flux than expected, even for very small input signal powers. The excess flux cannot be accounted for and causes saturation in the 2-channel synchronizer. The saturation effect causes non-linearity in the practical ADM-based ADC. An ideal model of the ADM, where no saturation occurs, shows that the ADM offers potential DR and sensitivity increases. A more ideal ADM-based ADC requires an increased number of synchronizers and therefore increased circuit complexity.

- The proposed decimation filter design provides a very simple technique for obtaining samples at room-temperature from a superconductor modulator. The modulator provides samples containing averaged derivatives of the input signal. Integration after the averaging is proven to be best implemented in more complex room-temperature electronics. The decimator is dependent on a sharp HTS pre-filter for the rejection of possible aliasing components. It is concluded that the proposed simple decimation filter structure offers the possibility for simplified ADCs with an increase in distortion because of frequency components produced by the oversampling modulator that are aliased into the band of interest. Such simplified ADCs may be useful for initial small-scale testing of ADC modulators.

- With the specification of modulator input signals it is concluded that ADC modulator sensitivity is dependent on the quantizer-loop inductance value. For a specific loop inductance value the presented DM modulator is sensitive to input signal powers in the range of about $-53.18\,dBm \rightarrow\approx -120\,dBm$ when matched to a 50 Ω load (as seen in Fig. 4.33). When compared to the receiver sensitivity of $-121\,dBm$ for a 3G Node-B transceiver [50], it is clear that the sensitivity of the presented superconductor ADCs are enough to operate with minimal or no LNA between the ADC and receiver antenna. The quantizer loop inductance can be optimized for optimal receiver sensitivity. It is also concluded that higher DR is possible for less sensitive ADC modulators [49] due to the effects of flux noise.

Chapter 5

An RSFQ-based Rapid Multi-Path Delay Estimator

As discussed in Section 2.2, any CDMA system requires correlation to recover received CDMA signals. All asynchronous CDMA systems require some acquisition technique to estimate phase differences between received signals and stored sequences. Rake receivers in particular, evaluate multiple signal paths and utilize estimated phase differences to find the strongest signal paths. In order to detect strong signal paths, the incoming signal can be despread at each possible phase shift of the stored despreading code and then be evaluated. Maximum correlation values then represent strongest signal paths. Generally, exploring all possibilities is a time consuming process and in this chapter superconducting electronics structures are proposed for quick and effective path estimation.

This chapter starts off by evaluating possible RSFQ correlator types and it is shown how they differ from conventional logic correlators. A comparison is done between two RSFQ correlator implementations by analysing peak detection threshold values along with the dependability of peaks above threshold. A solution is then provided to do fast path estimation with RSFQ logic by supplying RSFQ correlators with accelerated and repeated data with extra shifting functions to meet the correlation needs. This supply structure is referred to as a rapid data supply. The chapter is concluded with a short discussion on possible areas of implementation and feasibility of the estimation technique.

5.1 RSFQ Correlation Method Comparison

As discussed in Section 2.2 (and seen in Fig. 2.4), correlation is done via multiplication and accumulation (more specifically, addition and subtraction). In spreading and scrambling

operations binary codes are generally converted to NRZ (signed/bi-polar) values. In a correlation process where similarity is revealed between signals, the multiplication of similar signal signs would result in a positive output to the accumulator. Differing signal signs result in negative output, implying subtraction at the accumulator. When using binary logic, it is possible to detect whether signals are similar or dissimilar by using XOR logic functions and accumulate these similarities (as seen in [51]). Table 5.1 shows how the XOR function is used to obtain multiplication with the NRZ transforms: $0 \rightarrow 1$ and $1 \rightarrow -1$. The table clearly shows how at the XOR output zeros indicate similar values and ones indicate where values differ. Correlation theory implies addition and

Table 5.1: Basic XOR truth table showing the XOR relation to multiplication when using certain NRZ transforms.

A	B	$A \oplus B$
$0(1)$	$0(1)$	$0(1)$
$0(1)$	$1(-1)$	$1(-1)$
$1(-1)$	$0(1)$	$1(-1)$
$1(-1)$	$1(-1)$	$0(1)$

subtraction of the multiplied (XOR) result. The RSFQ correlation method proposed by Przybysz *et al.* [51] clearly has a single ripple adder, allowing only addition. When using RSFQ logic for correlation there are a few reasons to avoid RSFQ subtraction structures. RSFQ subtraction has:

- Added complexity because the correlator input signal register is much smaller than the correlator accumulation register.
- Increased margin for error at high clock speeds. This is because all bits in the accumulation register are constantly changed with subtraction operations (successful subtraction will always cause an overflow in a ripple adder).

Two types of correlators are therefore studied and compared:

1. The simplified correlator - a non-ideal structure using only addition
2. The ideal correlator - allows for addition and subtraction

A Simplified Correlator

The simplified correlator is modelled to be similar to the correlator by Przybysz *et al.* [51]. XOR logic is used to pass or invert the incoming signal depending on the code. This correlator also allows for additions when incoming signal sign and code differs. These additions clearly decrease the correlator performance, since differences should cause subtractions.

An ideal RSFQ Correlator

For an ideal implementation two accumulation registers are suggested. One will accumulate similarities and the other dissimilarities. This enables a single subtraction operation at the end of accumulation. Also, signed signal values are expected at the input. This allows that only the sign bit and code bit needs to be XORed to determine routing of the signal magnitude to the correct accumulation register. The suggestion, as shown in Fig. 5.1, is therefore to use an XOR logic function to determine similarity and use two ripple adders to accumulate similarities and dissimilarities respectively. The much slower subtraction operation can be implemented in conventional electronics or in superconductor electronics. When implemented in conventional electronics, time multiplexing can deliver the large number of parallel bits (two accumulation registers) to a limited number of superconductor integrated circuit output pins.

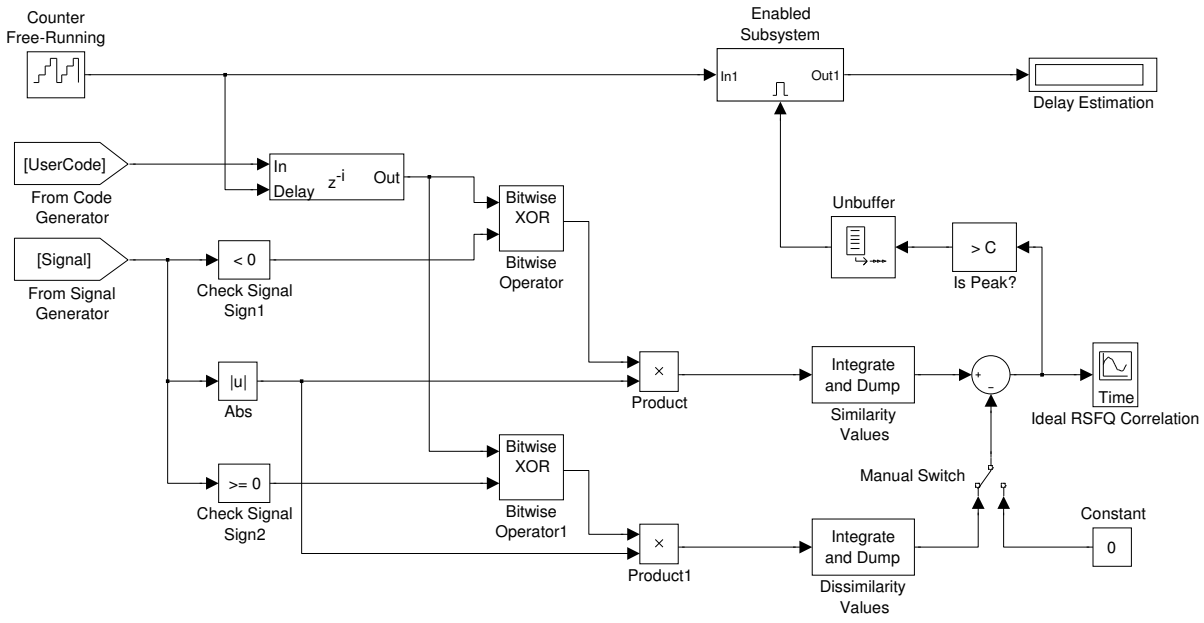
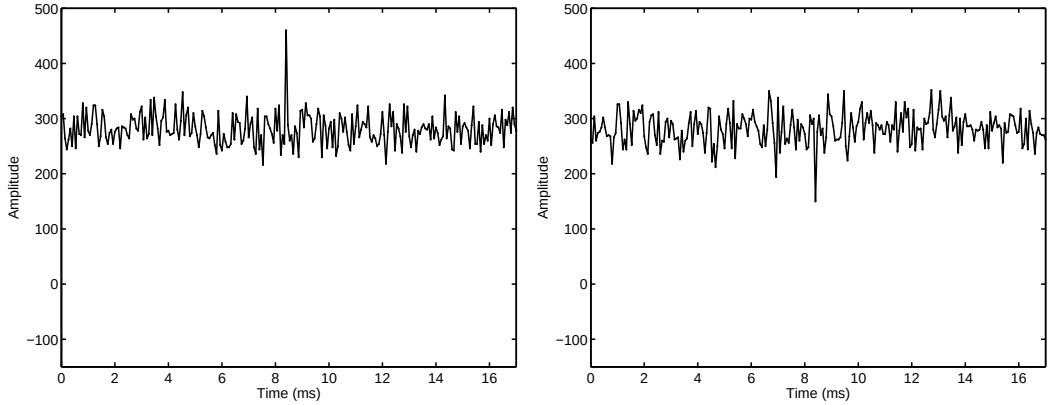


Figure 5.1: A MATLAB model of a correlation method, suitable for RSFQ logic

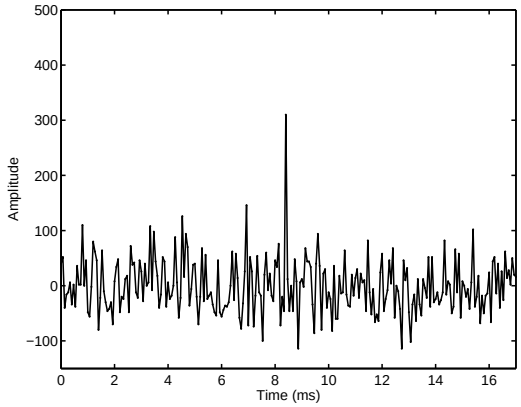
Model Simulation

The RSFQ correlation method is demonstrated using the MATLAB circuit model shown in Fig. 5.1. The input signal and descrambling code is as generated in Section 2.5.1. In order to see where signals correlate, the stored code is delayed with a variable delay element. The delay is increased each time the complete correlation result is obtained for a specific code delay. In Fig. 5.2(a) and (b) the typical output for the similarity (S_{RA}) and dissimilarity (D_{RA}) ripple adders can be seen respectively. In Fig. 5.2(c) the results are shown for $S_{RA} - D_{RA}$.



(a) RSFQ correlation similarities

(b) RSFQ correlation dissimilarities



(c) An ideal RSFQ correlation response

Figure 5.2: Responses for the MATLAB model presented in Fig. 5.1.

Model Comparison Technique

For comparison of different correlator models it will be shown how well signal path correlation peaks can be distinguished from interference correlation peaks. Peak detection thresh-

old values are therefore evaluated. These threshold values are generally programmable and variable within runtime. Correlator performance in relation to threshold range is therefore of importance. To analyse the performance, despreading of a received signal is done with two different despreading codes to obtain two different correlation results from the same set of data. The following two codes are used:

1. Firstly a code is used that was used in the spreading process (using this code should give a sharp peak at a specific phase). When using this code, the correlation is referred to as a '*user signal correlation*'.

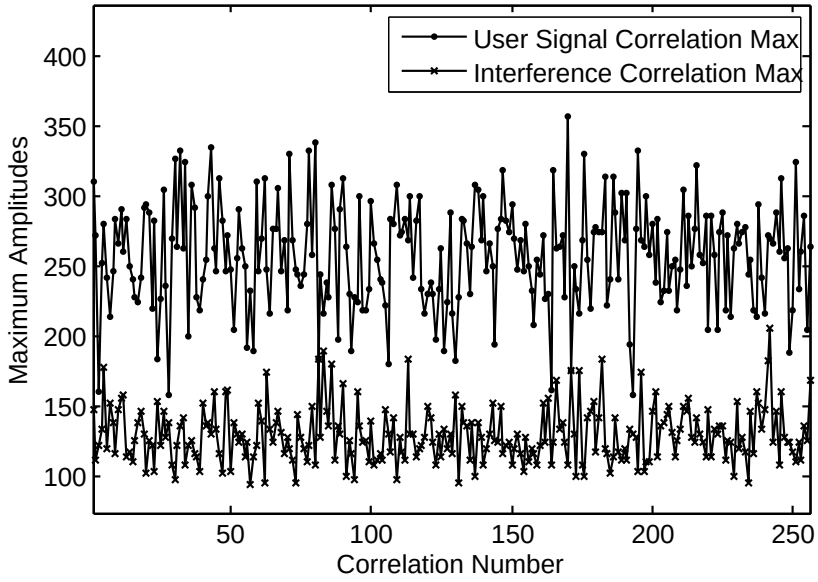
2. The second code used is not present in the received signal (not used in spreading process). This is done to evaluate the correlation peaks that are attributed to interference and noise in the system. When using this code, the correlation is referred to as an '*interference correlation*'.

In order to evaluate correlator performance according to threshold values, the model in Fig. 5.1 is set up to do multiple correlations for randomly generated user data scrambled with different parts of a long Gold code sequence. The data of the user that is selected is set to a constant value to produce positive correlation peaks (otherwise, an absolute value function at the correlator output will produce the positive peaks for a single positive threshold). To obtain an average value, the simulation is run for:

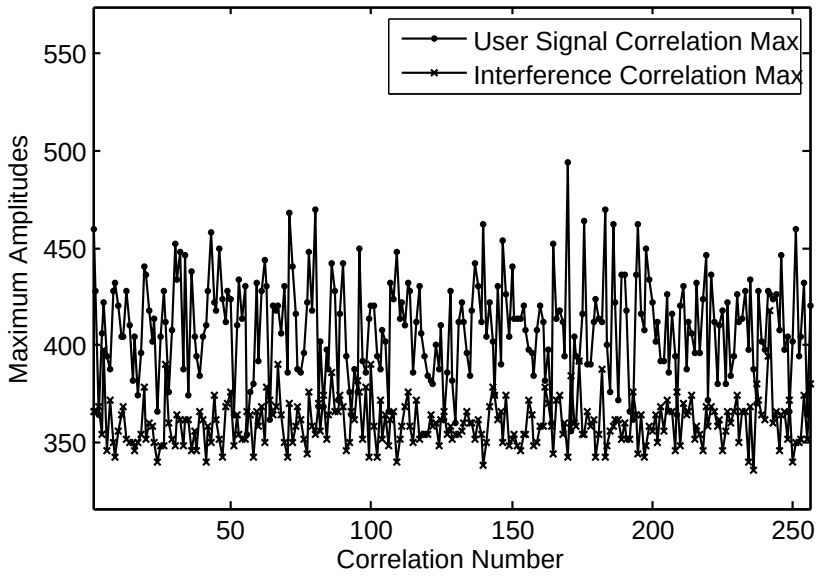
$$t_{simulation} = t_{chip} \times PG_1 \times PG_2 \times PG_3 = \frac{1}{3.84 \times 10^6} \times 256 \times 256 \times 256 \approx 4.37\,s, \quad (5.1)$$

where t_{chip} is the scrambling code period, PG_1 the number of correlation multiplications and additions, PG_2 the number of all possible phase shifts and PG_3 the number of correlation runs taken to obtain an average for performance evaluation. *User signal correlation* maximum values and *interference correlation* maximum values are given in Fig. 5.3 for each correlation run ($t_{chip} \times PG_1 \times PG_2$). The values in Fig. 5.3(a) are obtained by the ideal model where dissimilarity values are included. Fig. 5.3(b) shows the values for a simpler model where dissimilarity values are ignored(manual switch in Fig. 5.1 turned to the constant zero value). Three important comparisons are introduced at this stage that all relate to correlator performance. These comparisons are intended for evaluation of each correlation run and are as follows:

1. Check if the *user signal correlation* maximum values ($Corr_{user}$) are above a specific threshold value (K).



(a) The ideal RSFQ correlator (using similarities and dissimilarities)



(b) A non-ideal RSFQ correlator (using only similarities)

Figure 5.3: Maximum user signal correlation peaks and interference correlation peaks for a number of different correlation runs.

2. Check if *interference correlation* maximum values ($Corr_i$) are above the threshold value (K).

3. If the latter condition in occurs, it is desired to whether these peaks override (are greater than) the *user signal* peaks ($Corr_i > Corr_{user}$).

These conditions are then put into a truth table (Table 5.2) to identify two conditions that are important for correlator performance evaluation. These conditions relate to the dependability of detected correlation peaks. Dependability is a measure of how sure one can be that an actual signal path caused the peak above the threshold. The conditions are as follows:

1. When *user signal correlation* values are above threshold and *interference correlation* values are below threshold, it is with confidence that a detected peak reveals a user signal path. Condition:

$$X = (Corr_{user} > K) \cap (\overline{Corr_i > K}) \cap (\overline{Corr_i > Corr_{user}}) \tag{5.2}$$

2. When at least the *user signal correlation* maximum values are above the threshold, a detected peak might be an actual signal path. The larger value above threshold is probable to be the signal path. Condition:

$$Y = (Corr_{user} > K) \cap (\overline{Corr_i > Corr_{user}}) \tag{5.3}$$

Table 5.2 is shortened, because where the condition $Corr_{user} > K$ is false, the conditions X and Y are always false. All possible combinations of how maximum correlation values may relate to the threshold value and to each other are shown. These conditions are tested

Table 5.2: Conditions used for correlator model comparison.

$Corr_{user} > K$	$Corr_i > K$	$Corr_i > Corr_{user}$	X	Y
1	0	0	1	1
1	0	1	-	-
1	1	0	0	1
1	1	1	0	0

by taking the values from each correlation run (as shown in Fig. 5.3) and comparing them to different threshold values. For each type of correlator, two lines are presented in Fig. 5.4, where each data point on the lines are the accumulation of all correlation runs that satisfy conditions X and Y respectively (shown in Table 5.2) for a range of threshold values. Optimal threshold is defined as the value where a maximum number of signal paths can be detected along with a minimum number of interference peaks. Two measures are identified and used for model comparison. They are:

1. Minimum correlator error - When using relatively high threshold values, some valuable signal paths are not detected and are considered as errors. *Interference correlation* peaks that are higher than *user signal correlation* peaks also contribute to this figure. For this error value, the number of peaks indicating possible user signal paths is divided by the number of correlation runs (SF_3):

$$error_{min} = \frac{\sum Y_{condition}}{SF_3} \tag{5.4}$$

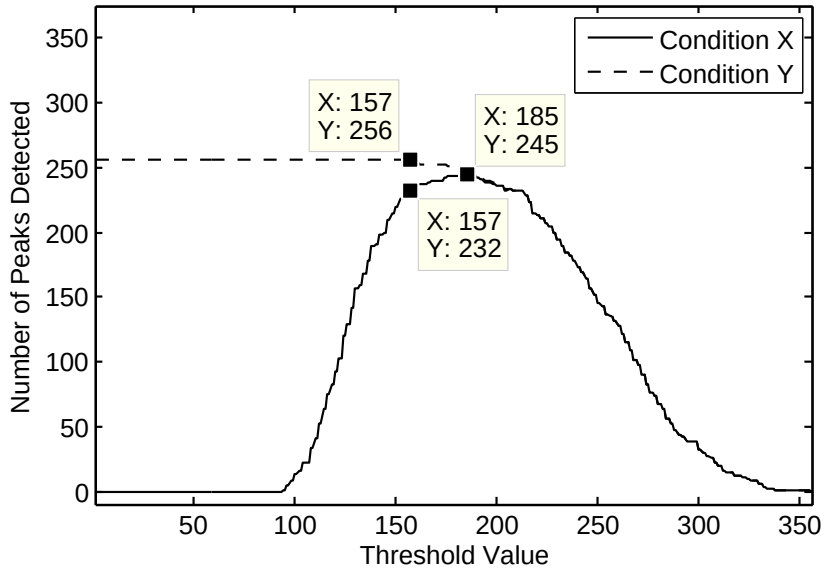
2. Above threshold peak dependability - When using relatively low threshold values, *interference correlation* peaks are also detected above threshold. These generally below *user signal correlation* peaks, but are evaluated as possible *user signal* paths. When the number of actual signal paths are lower than the number of rake receiver channels, these *interference correlation* peaks are evaluated as *user signal* paths and degrade the rake receiver performance. The dependability figure is defined as:

$$D = \frac{\sum X_{condition}}{\sum Y_{condition}} \tag{5.5}$$

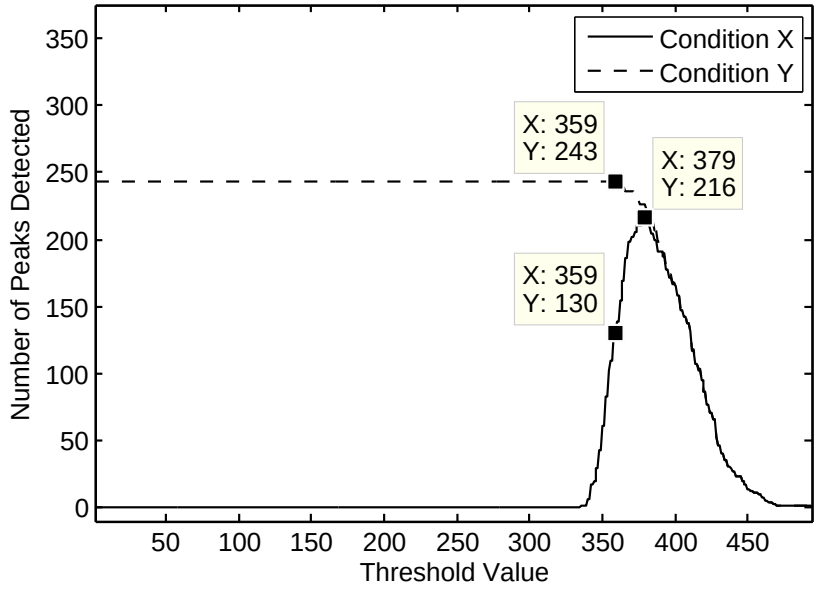
For each correlator these comparative figures are evaluated at two extremes as seen in Fig. 5.4. Evaluation is done for minimum error and then for maximum dependability. Threshold ranges between these two figures are considered optimal ranges for the respective correlator models. Table 5.3 shows these threshold ranges for different correlators along with the correlator figures for comparison. Table 5.3 clearly shows that the simplified correlation method produces much more errors in order to produce more dependable correlation peaks. In order to decrease the errors made, many correlation peaks that result from interference and are also above threshold need to be distinguished from multi-path signal correlation peaks. From Table 5.3 it is clear that much more of these interference

Table 5.3: Minimum probable errors and path dependability for different threshold values and different correlation techniques

Correlator Type	Threshold (K)	$\sum X_{condition}$	$\sum Y_{condition}$	$error_{min}$	Dependability (D)
Ideal	157	232	256	0%	90.6%
Ideal	185	245	247	3.5%	99.2%
Non-ideal	359	130	243	5.1%	53.5%
Non-ideal	379	216	226	11.7%	95.6%



(a) An ideal RSFQ correlator



(b) A simplified RSFQ correlator

Figure 5.4: Comparison of the number of correlation peaks that satisfy condition X and Y in Table 5.2 respectively. The number of peaks is shown for a range of threshold values.

correlation peaks are present above threshold in the simplified correlator model than the ideal model for similar amounts of $error_{min}$. The ideal RSFQ correlator clearly performs much better than the non-ideal correlator, especially for multi-path signal detection purposes in a rake receiver where all peaks above threshold need to be considered. Therefore the ideal RSFQ correlator is suggested for application in telecommunications where per-

formance gain outweighs increased size and complexity. Simplified RSFQ correlators can be used for applications where size requirements outweigh the performance requirements.

5.2 A rapid path estimation technique using RSFQ

Received CDMA signals in an asynchronous wireless system always require some form of synchronization. Rake receivers (as discussed in Section 2.2) perform synchronization procedures when acquiring different path delays in a multi-path environment. Such receiver estimation techniques in the uplink and downlink differ because of the resources available and transmission channel differences [13]. For superconductor electronic applications only uplink receiver implementation is considered because cooling constraints can currently be satisfied only at stationary base station transceivers.

Existing path estimation techniques

In transmission channels that vary with time, estimation time is limited in proportion to the varying characteristics of the channel. In UMTS, estimation time is recommended to be less than 10 symbols [52]. The need to use multiple paths to achieve reliable data detection has led to the development of numerous channel estimation techniques. Some techniques take other user signals into account for interference cancellation (joint multi-user estimation) while others only use the spreading code for the user of interest along with the received signal (blind estimation). Techniques either provide excellent performance coupled with intense computational complexity or decreased performance (estimates within 50-100 symbols) at reduced complexity [52]. Advanced joint multi-user estimation approaches provide estimates within five to eight symbols [52].

Path estimation with RSFQ circuits

Suggested for this thesis is a blind estimation method using iteration and superconductor electronics to determine channel multiple path delays within a single symbol. This technique provides a single structure that can be time-shared among multiple users or provide a dedicated estimator for a rapidly varying channel.

RSFQ correlators are able to obtain correlation results very quickly when operated at multi-GHz rates [51]. This enables us to rapidly detect where signals correlate with user code so that multiple paths can be speedily obtained for uplink rake receivers. Fig. 5.5 places the path estimation technique that is aided by superconductors into the perspective of a simplified receiver system that uses a rake receiver and superconductor digitization.

The relatively slow input signal and code is read into an RSFQ circuit which is used to

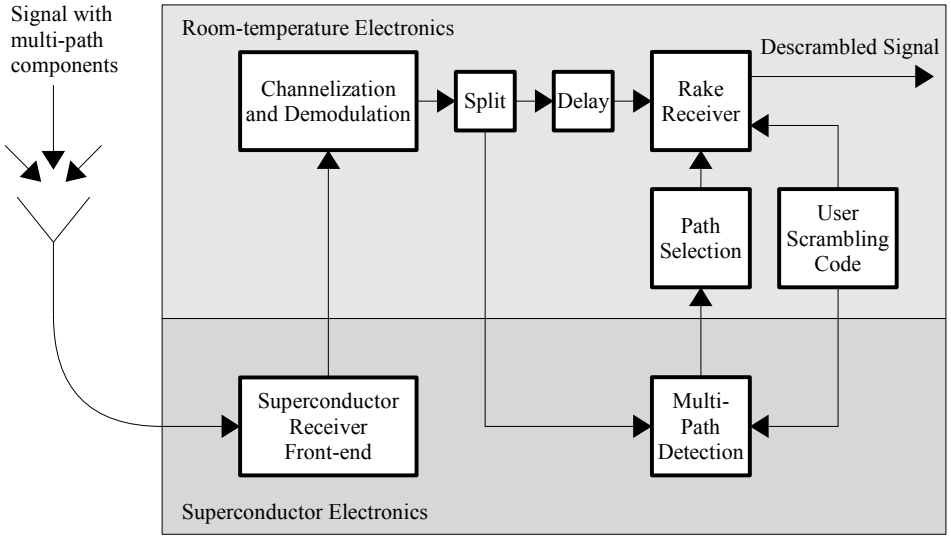


Figure 5.5: Diagram of a simplified receiver doing multi-path estimation aided by superconducting components.

rapidly detect all possible signal path correlation components for a specific user code. Room-temperature electronics then uses the correlation components from the RSFQ path detector to estimate strongest signal paths. A number of delay values (K) is then sent to the K-finger rake receiver for combined signal descrambling.

In order to correlate data at high speeds, an RSFQ correlator must be supplied with the received signal and stored user code at equally high speeds. The ability to do this is made possible by the fact that correlation is obtained by the shifting the same code signal in relation to the same received signal. Therefore a signal and code segment for a single symbol can be stored in a structure where rapid circulation and additional shifts are possible. This structure is termed the RSFQ rapid data supply. For this purpose FIFO queues are suggested consisting of storage units with destructive readouts. The length (N) of the queues are determined by the maximum processing gain (PG), determined by the scrambling code specifications. The head and tail of these queues are linked for data cycling purposes. Multiple clock signals, differing in frequency, are applied to the clock circuitry of these queue storage units in order to facilitate:

- the input of a received signal into the queue (chip clock),
- the cycling of queue elements for rapid correlation (fast clock) and
- the additional phase shifts of stored code elements (shift clock).

To improve the estimation time, two received signal input queues are suggested along with two stored code input queues. Therefore, while one set of queues is busy obtaining data at a slower rate (baseband CDMA signals and codes), the other set is busy cycling through the stored signals and codes for correlation purposes. Switching between these queues occur after each received symbol. Channel estimation data is obtained within a single symbol. A diagram for the RSFQ rapid data supply which feeds an RSFQ correlator with high speed data, is shown in Fig. 5.6.

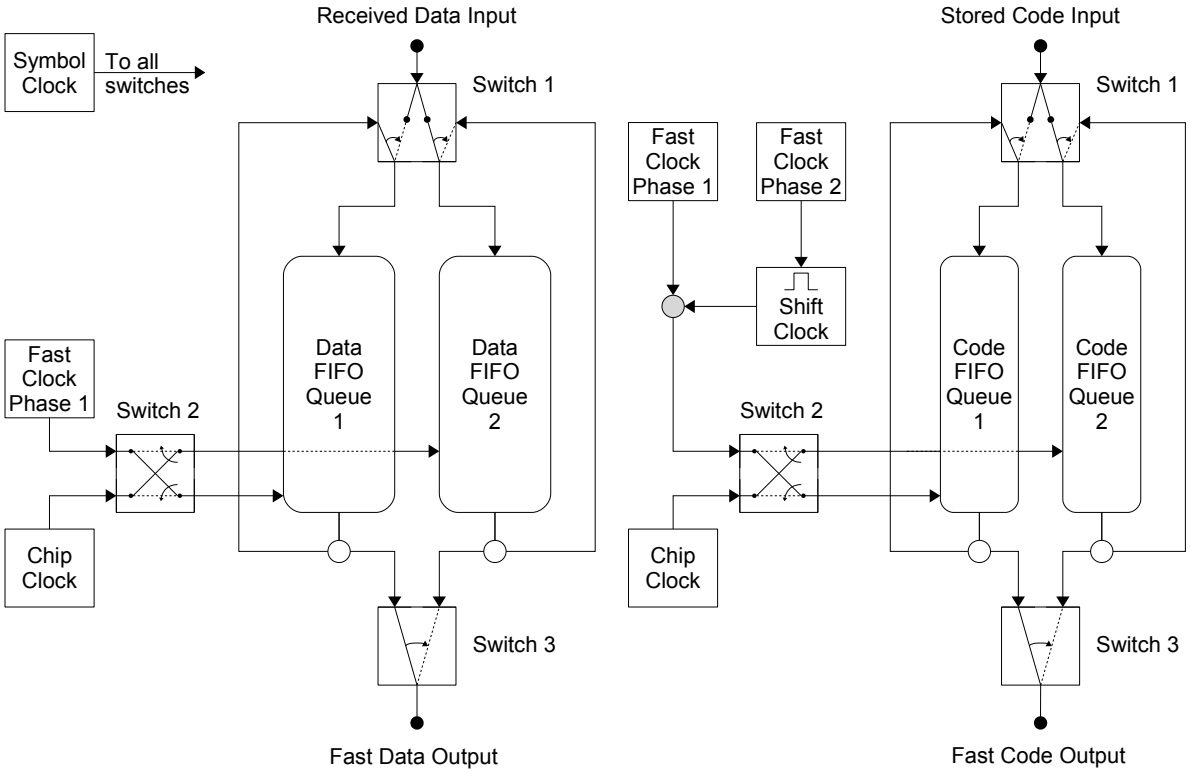


Figure 5.6: Diagram of the RSFQ rapid data supply

5.3 Modelling of an RSFQ rapid data supply

A MATLAB model of the rapid data supply is presented in Fig. 5.7. State-flow is used to model the switching between input and cycling states. Fig. 5.8 shows the state-flow diagram for the *Stored Code* model. The state-flow for the *RX Signal* model differ minimally from the *Stored Code* model, in that the extra FIFO pop function call for the '*shift_clk*' event is excluded. The data supply model is configured for a simple simulation

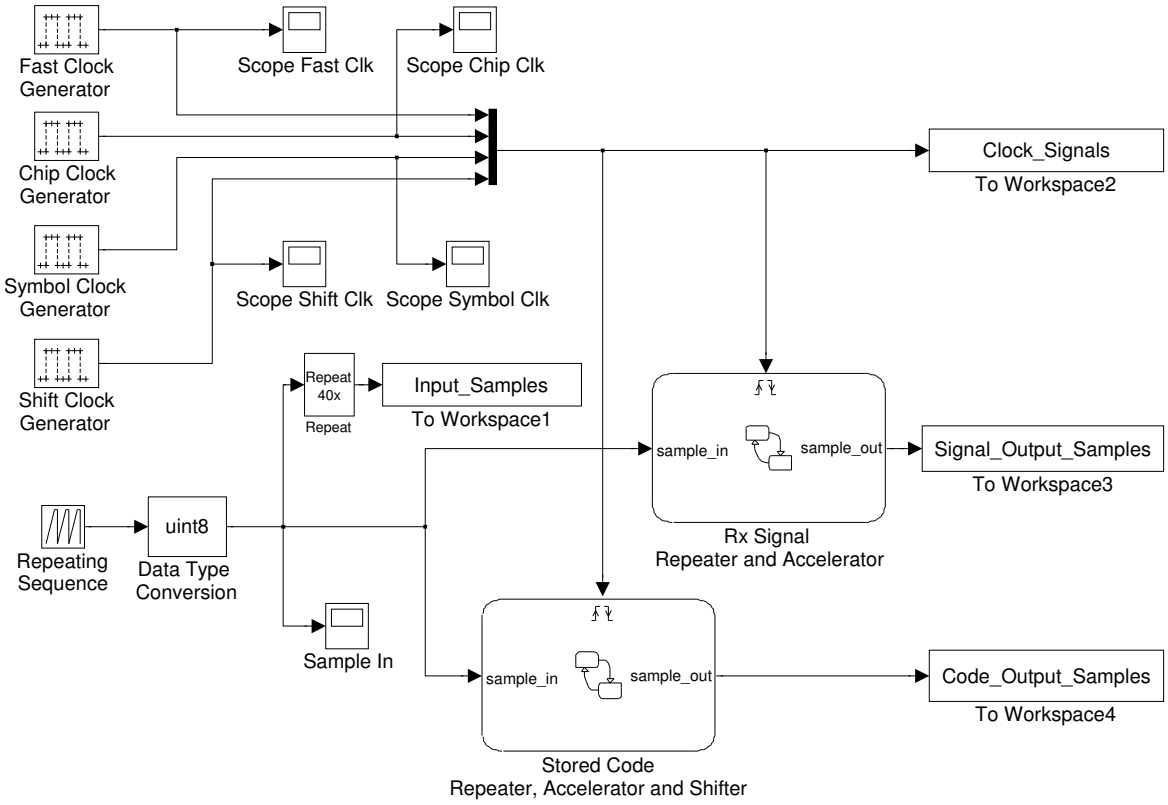


Figure 5.7: High speed data supply modelling for RSFQ correlation

to demonstrate functionality. A repeating sequence with a length of 4 is selected as input to both the data and code queues. The rapid output of the data queues is expected to be a fast repetition of the input sequence. Code queues are expected to deliver rapid repetitions of the input data sequence, while each repetition has a different phase. Code queues are required to at least cycle through all phase possibilities once for effective signal path detection. This simply implies the following requirement: $Chip\ Clock_{period} \geq (Fast\ Clock_{period})^2$.

The first model simulation results show how the slower input signals relate to the fast output signals. From Fig. 5.9 it is clear that a slow input signal is rapidly repeated at the output. Note that here sampling by the *Chip Clock* is rising edge triggered and repeating by the *Symbol Clock* is falling edge triggered. The second model simulation result in Fig. 5.10 shows how a stored code replica is shifted in relation to the received signal replica (both queues have the same input). Here it is seen that for all possible phase shifts, the sequence only matches at a single phase shift. Note that shifting by the *Shift Clock* is falling edge triggered and sampling by the *Fast Clock* is rising edge triggered.

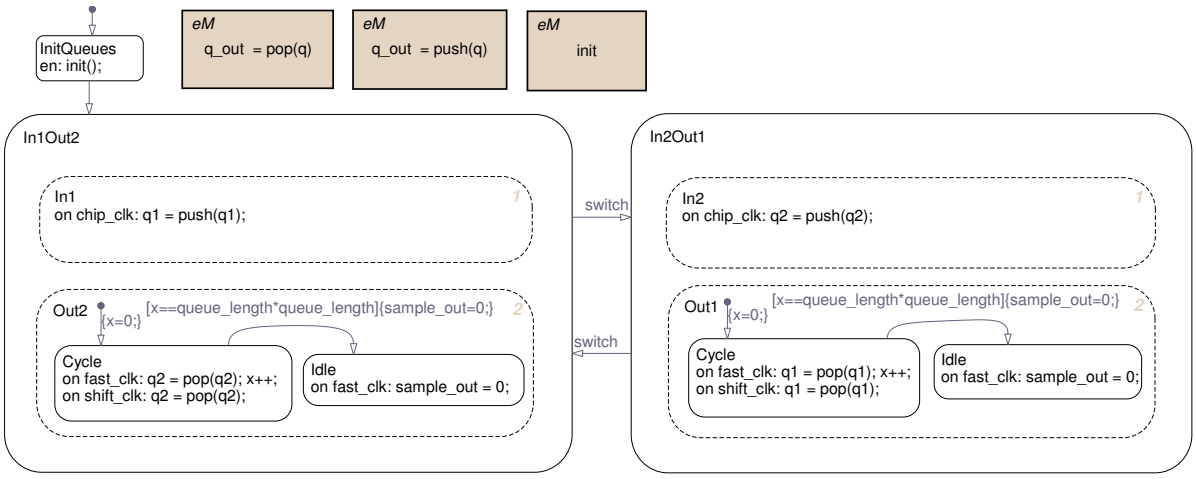


Figure 5.8: State-flow diagram for the Stored Code model seen in Fig. 5.7.

5.4 RSFQ rapid path estimator implementation

In this section the ideas presented by functional models are translated to RSFQ circuit models. The correlator translation and rapid data supply unit translation is presented separately. Functional circuit simulations are presented along with the evaluation of each of these units.

5.4.1 Correlator Circuit

Translation is started by evaluating different components in the model presented in Section 5.1. The components are listed as used in the model along with some details about suitable RSFQ components for implementation.

1. *Check Signal Sign* and *Absolute Value* - Before deciding on how to check the signal sign, a decision is made about the binary number representation. It is assumed that the values coming into the estimator are of the ubiquitous two's complement format. The sign can be extracted by a simple evaluation of the MSB. In order to determine the magnitude of the signal, an inversion is needed for negative two's complement numbers. To keep the RSFQ implementation as simple as possible, the conversion of two's complement values to sign-and-magnitude values is assumed before values are processed by the RSFQ circuit. When pre-conversion of the number format is not possible, inversion can be achieved by using XOR gates which can invert bits depending on the code value (as done by Przybysz *et al.* [51]).

2. *Bitwise XOR* - The correlator only determines similarity between the code and

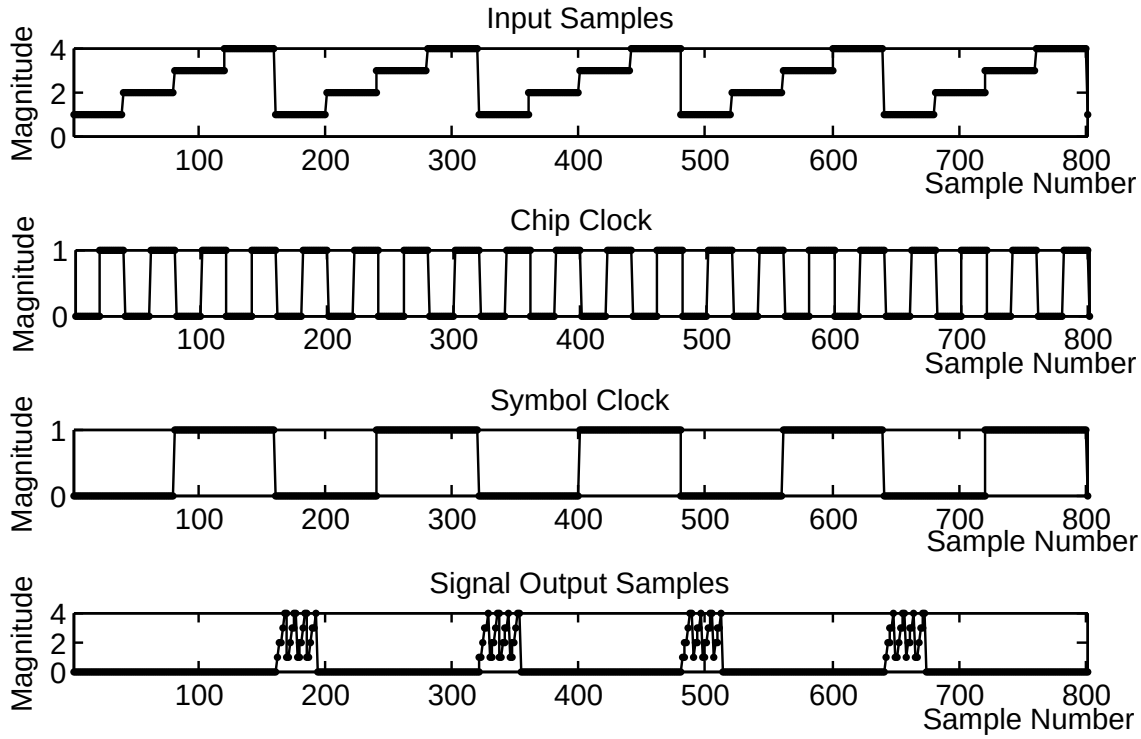


Figure 5.9: Rapid signal repetitions in relation to the slower input signals along with the sampling and enabling clock signals

received signal sign. A single RSFQ XOR operation is used for this purpose.

3. *Product* - This model element is used to allow a received signal magnitude to pass or not according to the result of similarity (0 or 1). For this purpose an RSFQ AND gate is implemented at each bit of the received signal magnitude. Alternatively, DC-enabled JTLs switched by an SFQ pulse interfaced bi-polar DC current driver (HUFFLE [53]) can be used, but relatively large inductances in the current loop limits the switching speed.

4. *Integrate and Dump* - All values at this stage are positive magnitudes and RSFQ T flip-flop (TFF) ripple adders are implemented to accumulate the magnitudes of similarities and dissimilarities respectively. These TFFs have asynchronous inputs and outputs to decrease accumulator latency. Of the two TFF types presented in Section 3.4.4, the T2FF is suited for use in such an accumulator. The T2FF is also provided with a destructive readout input to periodically dump the correlation data and reset the ripple adder.

5. *Subtraction* - The accumulated value of dissimilarities is subtracted from the accu-

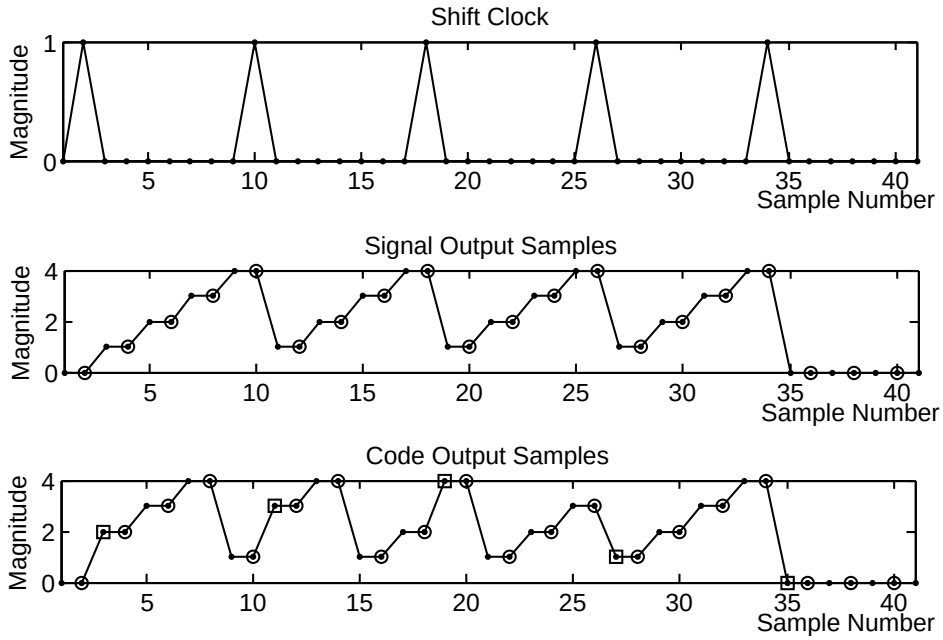


Figure 5.10: Graph of a rapid repetition cycle showing the shift clock and code phase shifts in relation with the received signal. Code values after shifts are marked with a ⊡ and *Fast Clock* sampling points are marked with a ⊙.

mulated value of similarities. This operation is generally required at much lower speed and therefore the subtraction can be implemented in superconducting electronics or in conventional electronics. If implemented in conventional electronics, the number of RSFQ chip outputs might be a limiting factor (depending on the correlation register size) and time domain multiplexing can be used to deliver the results in series over the same output ports. It was decided to limit the superconductor implementation size and perform the subtraction in conventional electronics.

6. *Peak Detection* and *Delay Estimation* - These procedures can now be effectively performed in conventional electronics (as seen in Fig. 5.5) by evaluating correlation peak 'pictures' formed by the RSFQ correlator.

Presented in Fig. 5.11 is a diagram that shows how the RSFQ components of such a correlator are linked. A two-phase clock is used to increase the readout operation margin of the correlation register. Readout clocking direction also differs between T2FFs with data inputs and T2FFs with only carry inputs for the same reason. Circuit simulations are done for this correlator operated at 10 GHz with a 3-bit signed signal input and 1-bit code input. A PG of 16 is chosen to accumulate values for 16 clock cycles before dumping. Fig. 5.12 shows how accumulated values are dumped at the end of each 16 clock cycles.

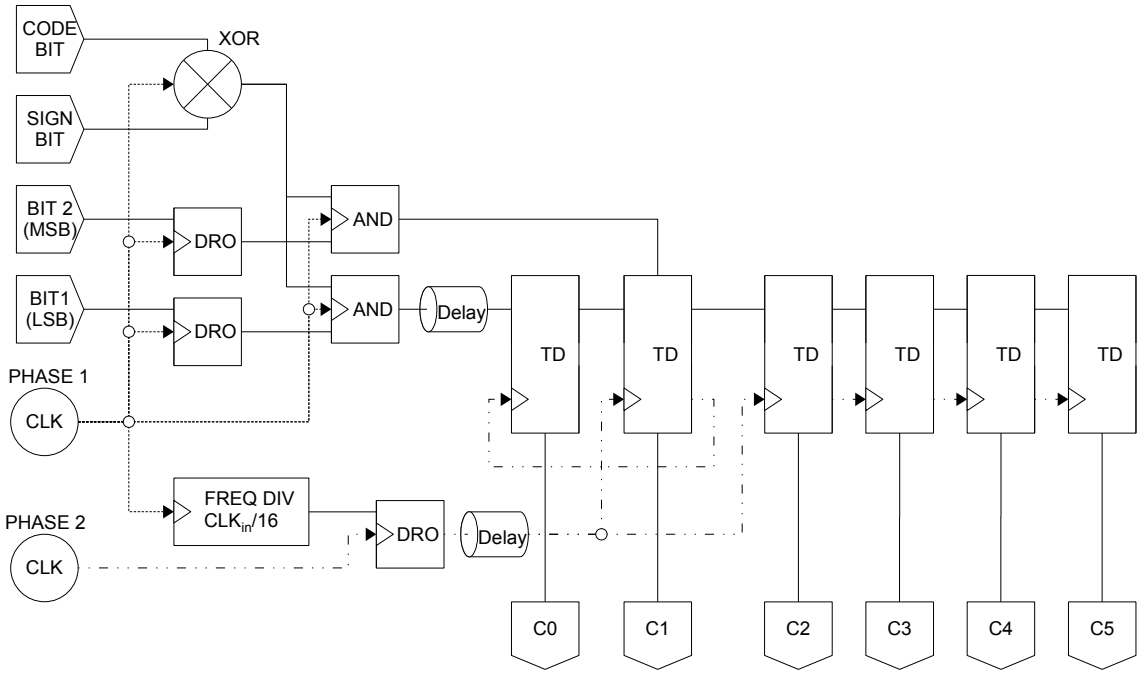


Figure 5.11: Diagram of an RSFQ correlator design

For the results shown in Fig. 5.12, the code is a constant stream of ones and the sign is kept positive (zero). This is done to test the correlator at maximum input values and to show that interference between the shifting operation of the T flip-flop register and input signals do not occur. The maximum clock speed of the correlator is mainly limited by the combined latency of the asynchronous T2FFs that are used for data input and therefore inversely proportional to the input signal resolution. To ensure correct readout operation for large correlator output registers, the T2FF still has to be optimized to produce the same latency for the passed readout signals than for the T2FF carry outputs. This would prevent data (input after readout signal) from out-running the readout clock, producing errors.

5.4.2 Rapid Data Supply Circuit

Translation of the rapid data supply model is started by evaluating the different components in the model and discussing suitable RSFQ components to perform the different functions. Most components are named as in the model and are as follows:

1. Clocking is an important part of the circuit. The circuit switches between a slow input state and a fast cycling state. The slow and fast states operate independent of each other and therefore the slower clocks need not be in synchronization with the

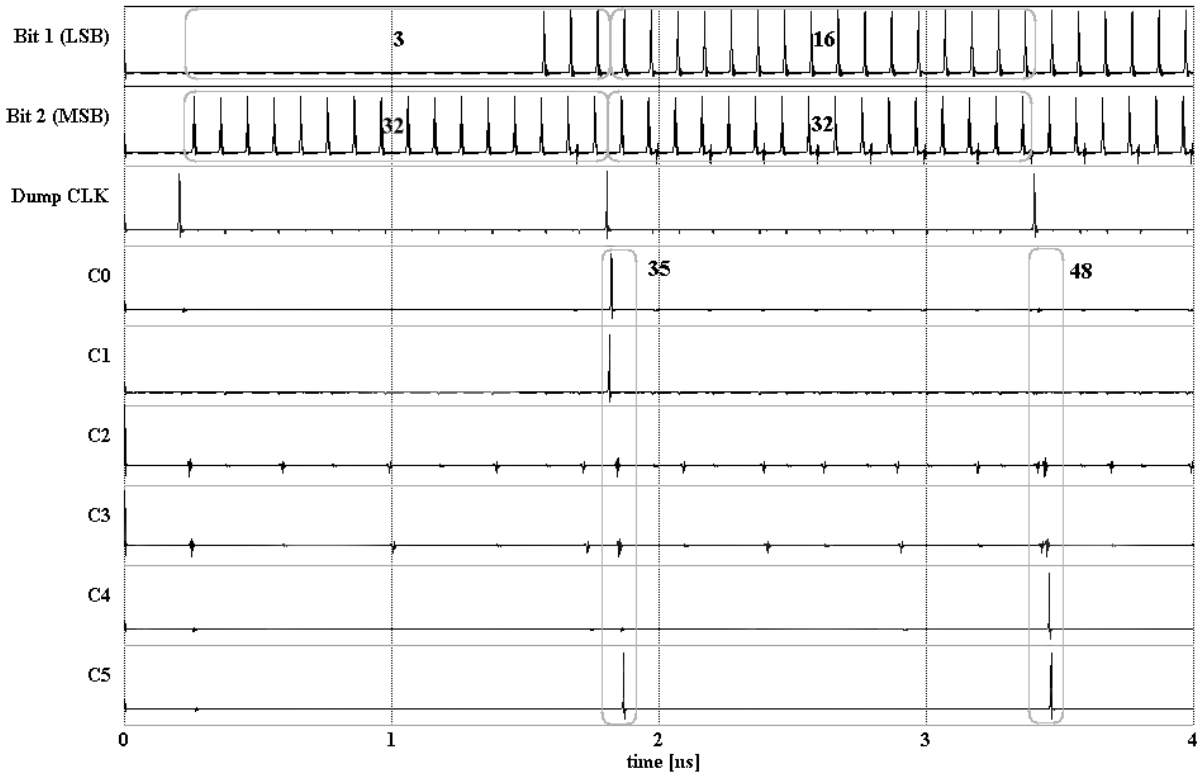


Figure 5.12: Circuit simulation of the RSFQ correlator showing two dump cycles

fast clocking signals. The method for generating each of these clock signals follow:

(a) *Fast Clock* - This clock is used to quickly cycle the stored FIFO data and enable the necessary code shifts. A two-phase clock is used to allow cycling in conjunction with the routine phase shifts, implemented in code queues. Cycling is enabled by the first phase of this clock. The clock pulses are obtained from an externally generated sine wave and DC-SFQ converters (as explained in Section 3.4.1).

(b) *Shift Clock* - This clock has the function of producing the routine shift needed for correlation purposes. The actual shift is enabled by the second phase of the fast clock. A frequency divider (consisting of T1FFs - see Section 3.4.4) is used to derive this clock signal internally. It is related to the PG as follows: $ShiftClock = FastClock/PG$.

(c) *Chip Clock* - The chip clock is obtained from the external input signal clock with DC-SFQ converters.

(d) *Symbol Clock* - The symbol clock is derived from the chip clock in the same way that the *Shift Clock* is derived from the *Fast Clock* so that: $SymbolClock =$

ChipClock/*PG*. This clock enables switching between slow and fast states. DC signals, varying in polarity, are used to switch states and therefore external polar DC signal sources are driven by this clock signal in order to switch between states.

2. *Switch* - An operation directly coupled to the *Symbol Clock*, used to enable slow or fast data input flow to FIFO queues. DC-enabled JTL structures (from Section 3.4.5) are used for this purpose. These structures allow pulses to be passed or blocked depending on the polarity of an input DC signal. The *Switch* implementation is described further on in this section.

3. Queues (*q1* and *q2*) - A FIFO queue consists of a register of connected DROs, clocked from the opposite direction than the data flow to prevent data racing through the register in a single clock cycle. Initially the fast data repetitions (cycling) were implemented by passing the queue output values back to the input. Another DRO was added to the feedback loop to ensure that the first element in the queue is cleared before the feedback data is fed to it. This approach works well for small PG values where the clock latency for the queue length is smaller than the clock period. When larger PGs are used (factors generally used for scrambling), the clock latency for the queue length is much larger than the clock period and a pipelined feedback system is required. Such a cycling queue implementation is described further on in this section.

4. Shifting - All normal queue cycling is driven by one phase of the *Fast Clock*. The other phase is used to produce an extra shift. This produces a shift in the whole queue, but data collides in the output DRO that is clocked by a single phase of *Fast Clock*. This is because the rapid data supply circuit supplies a correlator that operates only on a single phase of *Fast Clock*. Such data collision results in a sign error probability of 50 % when the shift occurs, because only the code queue is affected by the phase shift. The code queue only affects the sign of the signal going to the correlator. The error ratio can be roughly quantified as:

$$err_{ratio} = \frac{2\overline{Signal_{RX}}}{\overline{Signal_{RX}} \times PG} = \frac{2}{PG} \tag{5.6}$$

where $\overline{Signal_{RX}}$ is the average value of the received signals. Serious correlation errors are possible with low spreading factors ($PG = 4$ could give a correlation error of 50%) but larger SFs for which the circuit is intended for, show much lower

percentages for possible errors ($PG = 256$ could give a correlation error of about 0.78 %). At −42 dB below the correlation peaks, such errors are negligible for a single level threshold, when searching for correlation peaks.

The data supply circuit components are presented separately along with simulation results. Switching circuits followed by the FIFO circular queue circuits (with and without the phase shift components) are discussed before the complete data supply circuit is presented.

Switching Circuit

As shown in Fig. 5.6 from Section 5.2, there are three places for each queue where switching is required. Firstly, to input data into the FIFO at a slow rate, then switch to fast input from the head of the FIFO queue. Secondly, to supply the FIFO queue with a slow clock in the one state and then a fast clock in the other. Lastly, no data is to pass to the correlator in the slow state, but data should be passed to it in the fast state. Clearly all these switching needs can be met by a single configuration of DC-enabled JTLs. Fig. 5.13 show the suggested switching circuits for a single circular FIFO queue.

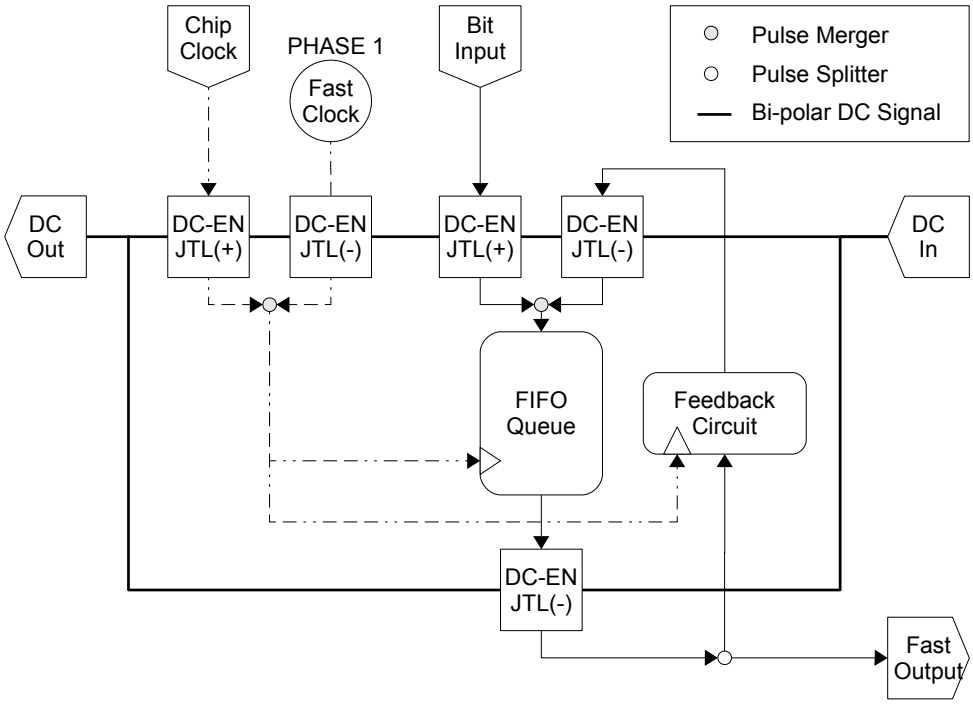


Figure 5.13: RSFQ switching circuitry for the rapid data supply circuit

Circuit simulation output in Fig. 5.14 show how changes in the DC signal polarity causes

different input signals to be directed to the data and clock input of the FIFO queue. It also shows how the FIFO output data is blocked in the slow state and passed in the fast state. It is also clearly shown how the number of values, equal to the size of the queue, is rapidly repeated. After the fast state, the output is blocked, allowing the queue to clear previous data and obtain new input data.

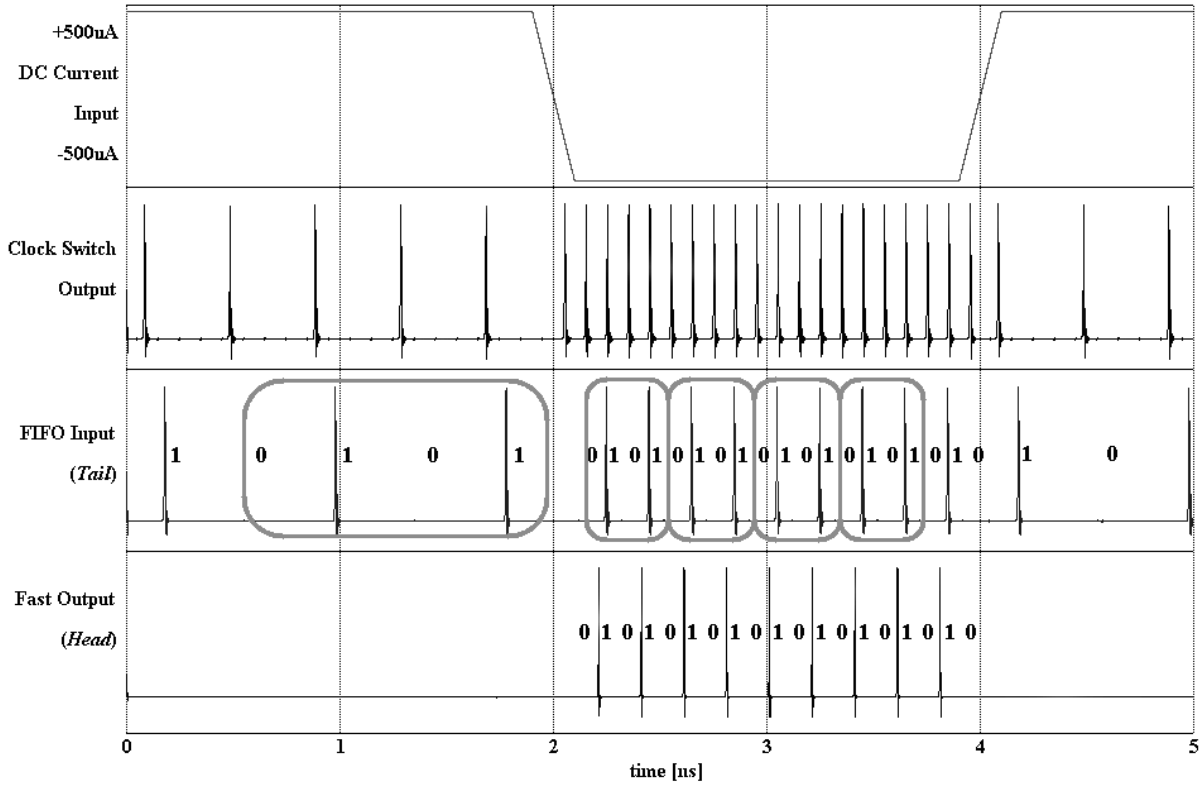


Figure 5.14: Simulation results of the rapid data supply circuit showing how changes in the DC signal polarity causes switching of FIFO queue inputs and outputs.

FIFO Circular Queue Circuit

An RSFQ FIFO queue circuit can be implemented as follows:

- Connect the output of each DRO storage unit through a JTL to the input of the next DRO for all queue elements except the last element.
- The FIFO is clocked from the head element of the FIFO queue to the tail element to prevent data from racing through the queue. The same clock signal is distributed from the head element to the tail (input) element by the use of pulse splitters and JTLs.

However, the pulse splitters and JTLs introduce a delay that becomes quite substantial when implementing the required long FIFO queues (large PG values). This delay specifically affects the design of a circular FIFO queue. Some design considerations and requirements follow:

- The delay between the readout of the *head* element and readout of the *tail* element implies a similar delay for the data feedback in a circular queue implementation. Feedback data must be passed to the *tail* only after the *tail* has been clocked, otherwise feedback data will collide with *tail* data.
- The *head* element supplies feedback data at a fast rate. Therefore, a pipelined feedback structure is necessary to prevent collisions between the *head* data and feedback data.
- To obtain the correct clocking phase (when the feedback data can be written to the *tail*), it is necessary to clock the feedback data in the same direction as the feedback data flow.

With these considerations and requirements in mind, a second queue (feedback queue), similar to the main FIFO queue is suggested for circulation purposes (see Fig. 5.15). This queue is implemented much the same as the main FIFO queue, except for some added delays due to the change in clocking direction. To prevent data from racing through the feedback circuit, JTLs are placed between the output of a DRO feedback queue element and the input of the next element. This introduces a delay so that the clock from one queue element arrives at the next queue element before the data arrives. The addition of a feedback queue more than doubles the circuit size of the circular FIFO, but allows for the necessary long queue lengths.

It is important to note that the feedback queue needs to be initialized with data before rapid circulation is started, otherwise the feedback queue will clear the main FIFO queue. Therefore, in the slow input state, the feedback queue is filled with the same data from *tail* to *head* as the main FIFO queue. Therefore the circuit effectively consists of two FIFO queues connected *head*-to-*tail* and *tail*-to-*head* as shown in Fig. 5.15. The slow input data is therefore duplicated and another switch is added to allow input to the feedback queue in the slow state.

The added switch (DC enabled JTL) is shown in Fig. 5.16. This circuit diagram is an extension of Fig. 5.13. The added clocking logic that facilitates the phase shift of code data needed for the correlation purposes is shown. The added clocking and switching components are darkened to distinguish this figure from Fig. 5.13. The circuit

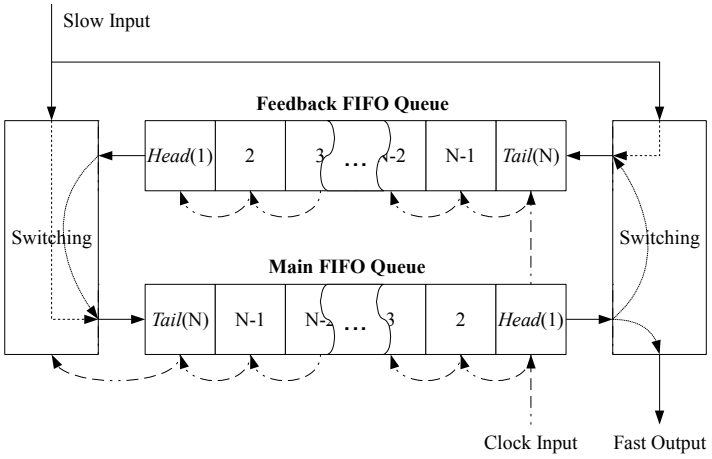


Figure 5.15: Diagram of the circular FIFO Queue for RSFQ implementation

for the circular FIFO queue is presented in Fig. 5.17. The circuit diagram is shown for an arbitrary number of queue elements. Circuit elements that facilitate the data transfer between the main FIFO queue and feedback queue are also clearly shown. Circuit simulation results in Fig. 5.18 show how this circular FIFO structure reads data externally in slow states and circulates data rapidly in fast states. Clock circuitry used is as shown in Fig. 5.16, to allow an extra phase shift each time the FIFO data is cycled. For this simulation a circular FIFO structure with a length of 4 is used. Therefore, the last 4 bits of slow input data is repeated with different phase shifts. Each repetition is grouped in Fig. 5.18 with the phase shift clock causing an extra bit at the output while shifting. For correct shifting, the second bit is chosen when a shift occurs. The fast output bit sequences are therefore: '*0110*', '*1100*', '*1001*', '*0011*' and '*0110*' (as grouped in Fig. 5.18).

5.4.3 Rapid Estimation Circuit Composition

Description of the RSFQ correlator and rapid data supply circuit is now complete. Presented in Fig. 5.19 are the abstractions of these components with the necessary inputs and outputs shown. In Fig. 5.20 a diagram is presented for a 3-bit RSFQ rapid path estimator. Two rapid data repeaters are used for each bit to obtain maximum circuit effectivity by loading the one FIFO while the other is rapidly repeating data. Clock signals are omitted in this diagram in order to unclutter the data and DC signal connections.

Layout size considerations

Before considering the feasibility of the proposed rapid estimation technique, it is important to analyse and estimate the size of a realistic and useful implementation. A

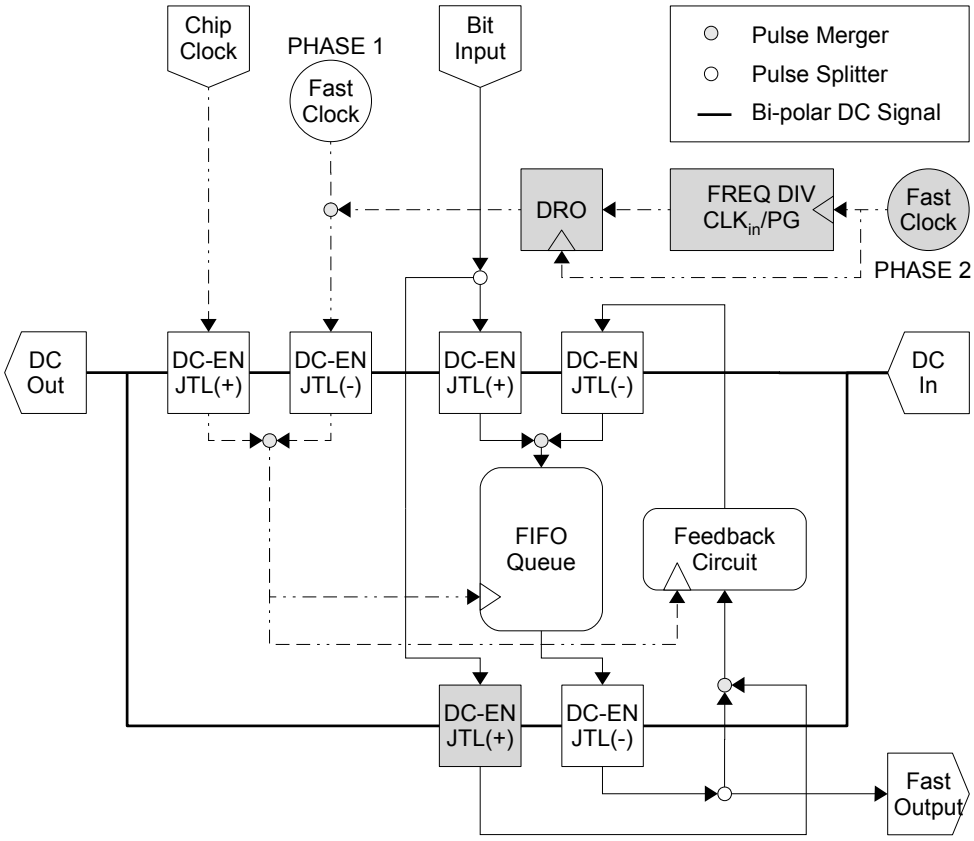


Figure 5.16: Complete RSFQ switching circuitry for the rapid data supply circuit. This diagram is an extension of Fig. 5.13. The added clocking circuitry (used for correlation phase shifts) is only used for code bit queues.

size estimation is therefore made for an RSFQ rapid path estimator with an 8-bit signed CDMA input signal and PG of 256. Therefore, 16 rapid data repeaters are required along with a single correlator. The correlator has an 8-bit input signal, 1-bit code input and an accumulation register that is able to at least accumulate values up to the maximum value of the threshold range. With an undetermined threshold, the maximum possible correlation value is accounted for. An accumulation register with the following length is estimated for:

$$L = log_2(2^{n-1} \times PG) = 15, \tag{5.7}$$

where L is the number of accumulation register bits and n the number of input signal bits.

Table 5.4 shows different components of the RSFQ rapid path estimator along with the types of cells used and number of those cells used. Using the cell layout sizes done by Fourie [25], the area this circuit could occupy on a superconducting die is estimated

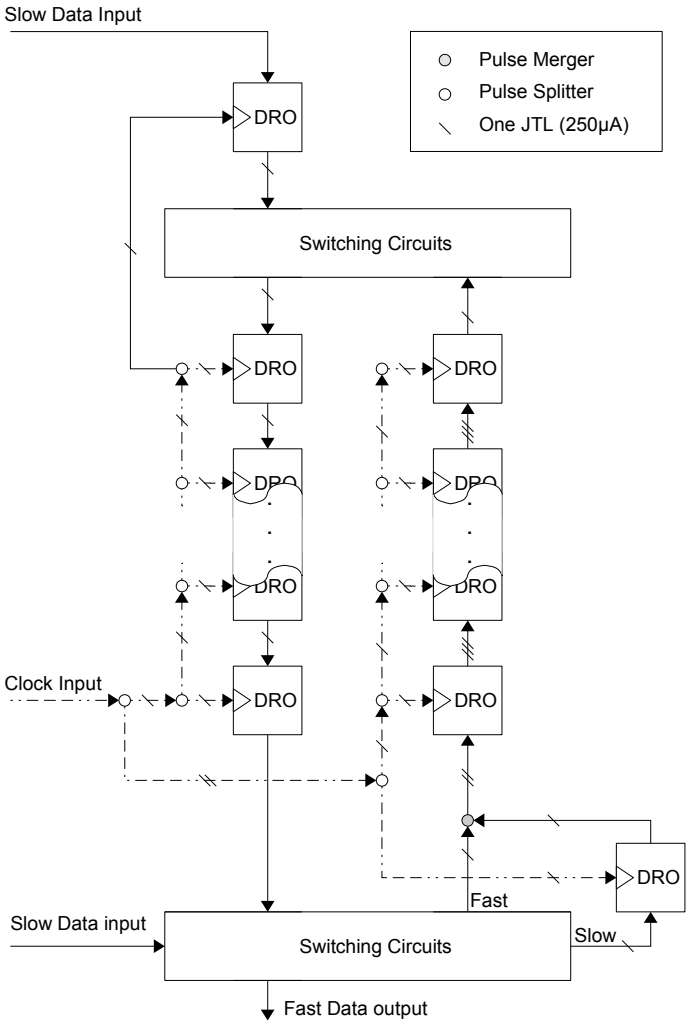


Figure 5.17: The RSFQ circuit for a circular FIFO structure used for rapid data supply.

using the Hypres $1\,\mathrm{kA/cm^2}$ process. According to these rough estimates, the core circuit would occupy an area of at least $93.5 \times 10^6\,\mu m^2$ ($9.67 \times 9.67\,mm^2$). Interface circuits are excluded from this figure. When compared to the size of superconducting dies available in commercial fabrication processes, Fig 5.21 shows that the circuit could fit on some of the larger die sizes, when meticulous care is taken with the layout procedure.

Further size reduction can be obtained by implementing the long FIFO queues with advanced asynchronous FIFO structures such as proposed by Hara *et al. [54]*. Using the circuit area given by Hara *et al. [54]* of $80 \times 240\,\mu m^2$ for a 4-bit FIFO, the minimum layout predictions of the RSFQ rapid path estimator can be adapted. Using the advanced FIFOs, a single circular FIFO buffer area can be reduced from $5.717 \times 10^6\,\mu m^2$ to about $2.46 \times 10^6\,\mu m^2$. The total size estimate of the rapid path estimator with the adanced FIFOs can therefore be as small as $41.36\,\mu m^2$ ($6.34 \times 6.34\,mm^2$). All layout predictions

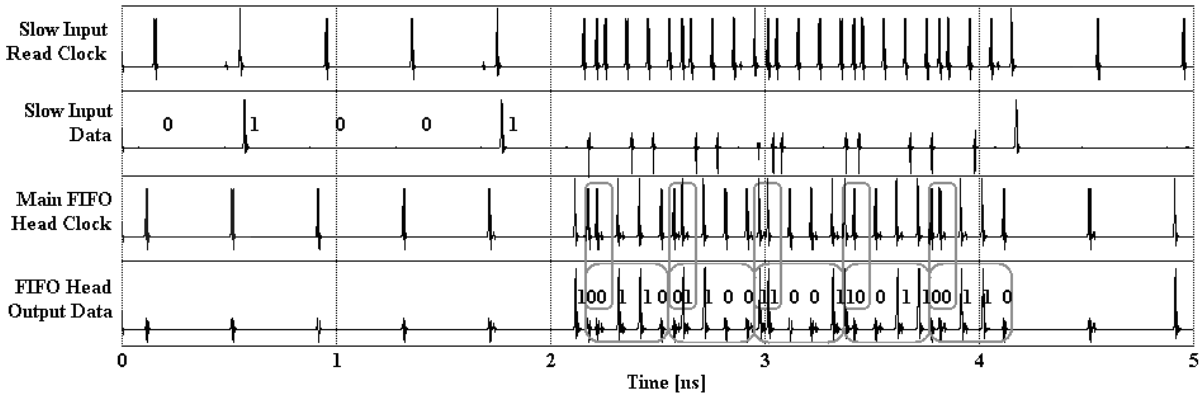


Figure 5.18: Results of an RSFQ rapid data supply circuit using phase shift clock circuitry.

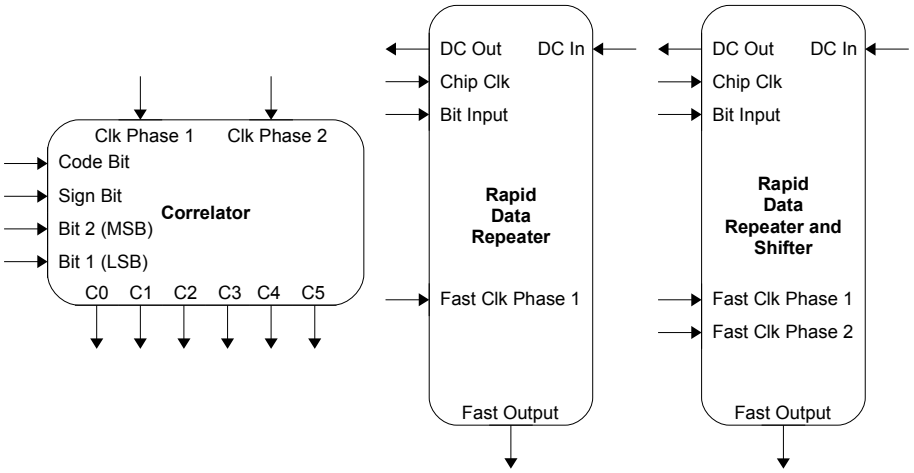


Figure 5.19: High-level blocks used in the rapid estimator, showing necessary inputs and outputs.

are shown in Fig. 5.21 in relation to available die sizes. Implementation of the relatively large rapid path estimator is therefore possible with current fabrication technologies.

5.5 Conclusions

A superconductor circuit is proposed for rapidly providing conventional electronics with information about the magnitude and phase of possible signal paths . A blind estimation technique is implemented, rapidly exploring all phase possibilities. The technique uses RSFQ circuits, clocked at multi-GHz rates, to deliver path estimation information within a single symbol period. These may lead to multiple path estimation times of up to 5-10 times faster than other more complex methods, not using superconductors.

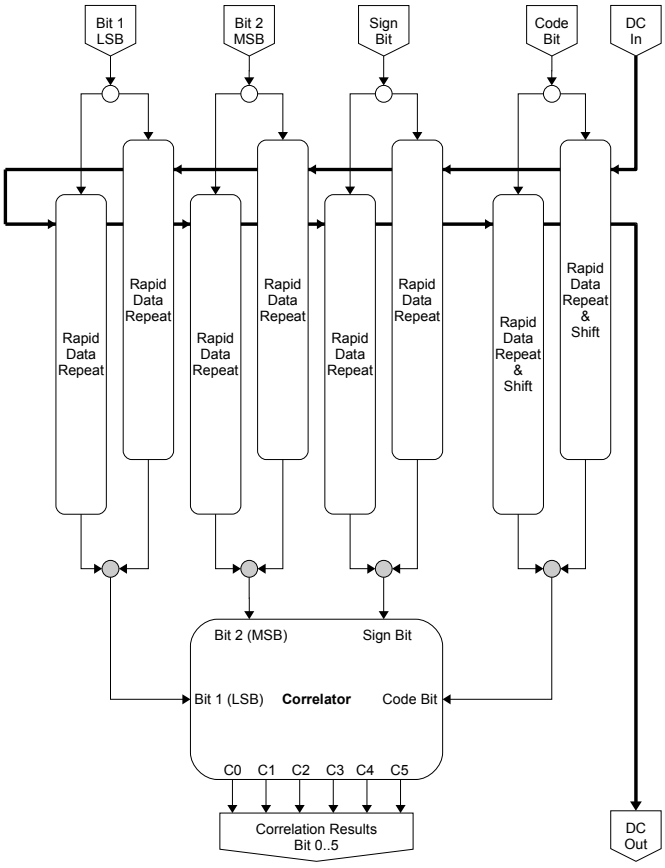


Figure 5.20: A 3-bit RSFQ rapid estimation system

Correlators suitable for superconductor implementation are evaluated. A method is introduced by which different correlator configurations can be compared according to threshold range and performance within the range. Functional correlator models are introduced along with the rapid data supply model for fast correlations. These models are then translated to RSFQ circuit models and simulated. The results prove functionality of the technique, but optimization and detailed timing analysis of the large structures are still required. Layout estimations show that the gross area occupied by the rapid estimation circuit is small enough for implementation on some of the larger available niobium die sizes. Using FIFO structures with improved data storage and clock distribution circuits [54] produces a much smaller layout estimate. The calculated estimates show the high potential for near-future implementation of the RSFQ-based rapid multi-path delay estimator.

In many ways the rapid path estimator is still a solution that is in need of a problem to solve. The fast estimation times required for a rapidly changing wireless cellular environment may be sufficiently solved by more complex methods implemented in conventional

Table 5.4: Rapid Estimator RSFQ Circuit and cell layout areas for a 1 kA/cm^{2}layout process.

Circuit	Subcircuit	Cells	Cell area [μm^2]	Amount used	Combined area [μm^2]
Rapid Data Supply			5.76×10^6	**16**	$\approx 92.2 \times 10^6$
	Switching		45.9×10^3	**1**	45.9×10^3
		DC-enabled JTL	2.5×10^3	6	15×10^3
		Splitter	2.8×10^3	3	8.4×10^3
		Merger	2.5×10^3	3	7.5×10^3
		JTL	1.25×10^3	≈ 12	15×10^3
	Circular FIFO		5.717×10^6	**1**	5.717×10^6
		DRO	3.34×10^3	514	1.717×10^6
		JTL	1.25×10^3	$\approx 8 \times 256$	2.56×10^6
		Splitter	2.8×10^3	514	1.44×10^6
Correlator			571×10^3	**2**	$\approx 1143 \times 10^3$
		XOR	8.26×10^3	1	8.26×10^3
		DRO	3.34×10^3	7	23.4×10^3
		AND	30×10^3	7	210×10^3
		Splitter	2.8×10^3	16	44.8×10^3
		JTL	1.25×10^3	≈ 48	60×10^3
		TD2FF	15×10^3	15	225×10^3
Frequency Divider			91.3×10^3	**2**	$\approx 182.5 \times 10^3$
		JTL	1.25×10^3	9	11.25×10^3
		T1FF	10×10^3	8	80×10^3

electronics. The gain achieved by the superconductor estimation circuit alone might not be enough to justify the introduction of a cryogenic environment. However, many cellular base stations already have cryogenic environments for HTS analogue filters [6]. In the near future, the advantages of superconductor ADCs could also justify the commercial implementation of more advanced cryogenic environments. In addition to this, rapid estimation results can be obtained within a single symbol period for CDMA chip rates much greater than the UMTS standard 3.84 Mbps, implying that the full estimation potential of these circuits are not reached with current wireless cellular bandwidths. When the RSFQ rapid path estimator is operated at 10 GHz, estimation periods of a single symbol are still possible with chip rates of up to 39 Mbps.

The rapid correlator presented here can also be used to perform correlation between

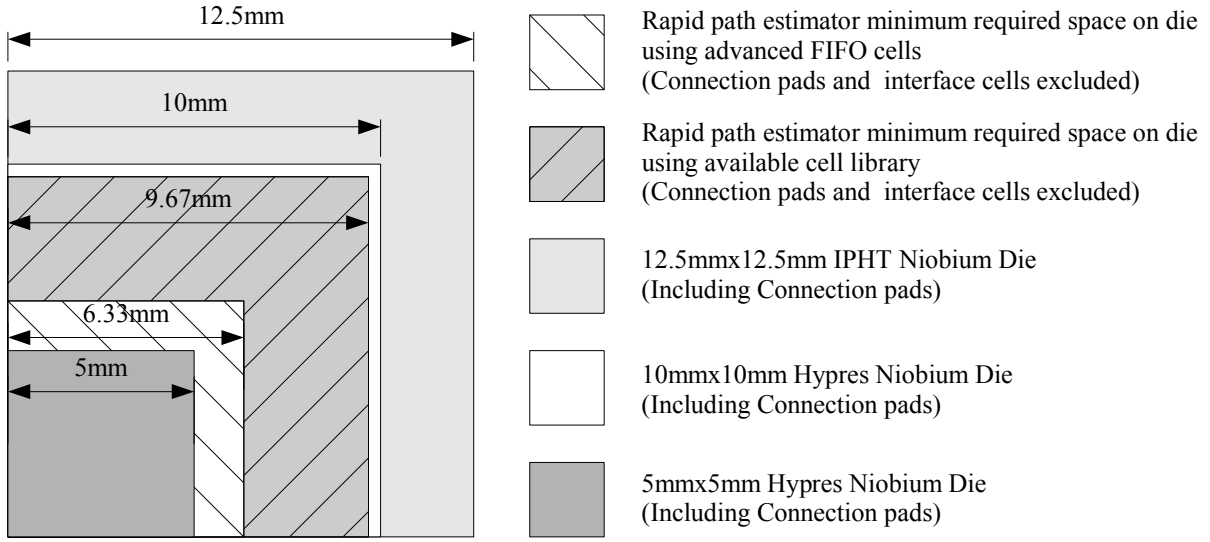


Figure 5.21: A comparison of current commercially available chip sizes and the minimum space required for an RSFQ rapid path estimator

a sampled RF waveform and stored code. In this way a superconductor ADC with channelization can be directly connected to the RSFQ correlator [8, 51].

Chapter 6

Conclusion

6.1 Overview of Thesis

This thesis is aimed at the exploration of potential superconductor applications in cellular network base stations. Research in this field revealed a number of possible applications. Further study revealed which of these applications seems the most promising and which of the applications seem relatively unexplored. The focus of this thesis is directed towards cellular network base station receiver applications and CDMA multiplexing technology. More specifically, the following base station receiver components are identified for research:

- The oversampling analogue to digital converter (ADC)
- The estimation of received CDMA-based signal multiple-path delays

Information on the background, design and evaluation of superconductor oversampling ADCs are presented in the following chapters:

- Chapter 3: Here the fundamentals of RSFQ logic are presented along with some of the RSFQ cells required in the superconductor ADCs.
- Chapter 4: Here basic principles about ADCs in general and superconductor ADCs are presented along with the detailed design of RSFQ-based superconductor ADC components.

Information on the background, design and evaluation of the RSFQ-based multiple path delay estimator is presented in the following chapters:

- Chapter 3: Here the fundamentals of RSFQ logic are presented along with some of the RSFQ cells required in the RSFQ-based path delay estimator.

- Chapter 2: Here the basic principles of wireless communications based on CDMA are presented. The fundamental principles behind multi-path delay estimation are presented in this chapter.
- Chapter 5: The implementation of the RSFQ-based multi-path delay estimator is presented here.

6.2 Main contributions

The main contributions of this thesis are divided into different categories and are as follows:

- Contributions in RSFQ Superconductor Electronics (SCE)
  - Detailed analysis of the WRspice JJ model including the equations necessary to adapt the model for a specific fabrication process.
  - A specific Toggle Flip-Flop cell (T2FF) which is derived from other TFFs. A T2FF with destructive readout and 2 inputs is also contributed.
  - A DC-enabled JTL cell for blocking and allowing SFQ pulses.
- Superconductor ADC contributions
  - Detailed specifications of superconductor ADC input waveform frequency and amplitude depending on certain parameters. The specification is for delta-type modulators which are limited by the slew rate of a received waveform.
  - Two different superconductor delta-type ADC modulator designs. Firstly a classic delta modulator design and then an advanced delta modulator design with asynchronous quantization and multi-channel synchronizer.
  - A MATLAB model for each of the designed modulators. These models simplify the quantum effects of the superconductor circuits to allow faster simulation times and evaluate circuits over long time periods, mainly for ADC spectrum analysis.
  - A simplified superconductor based decimation filter design. This design allows for a relatively small circuit that produces decimated ADC output samples that can be obtained by room-temperature electronics.

  - A MATLAB model of the decimation filter. The model is used along with the models of the ADC modulators for ADC spectrum analysis.
  - Dynamic range evaluations that lead to conclusions about how modulator slew-rate and sensitivity relate to the dynamic range of the modulator.

- Contributions in CDMA-based communications

  - A CDMA channel model incorporating random user data, scrambling codes (Gold codes), multiple path delays and AWGN. This model is used in the evaluation of a path delay estimator.
  - A multi-path delay estimation model. This model forms the foundation from which the RSFQ multi-path delay estimator is built.

- Path delay estimation contributions

  - A comparison method for different correlator configurations. Correlators are compared according to threshold range and performance within the range.
  - RSFQ-based correlator model. The model forms part of the estimator model.
  - An RSFQ correlator circuit design based on an ideal correlator model.
  - A rapid data supply model based on a dual function circular FIFO buffer that is controlled by data and clock switching components.
  - An RSFQ circuit implementation of the rapid data supply model. Together with the correlator, this forms the RSFQ-based part of the multi-path delay estimator.

6.3 Concluding Remarks

It is concluded that RSFQ-based wireless receiver components offer promising new options for data conversion, correlation and multi-path delay estimation implementations.

Discussions on superconductor ADC architectures reveal areas of possible performance increases. From the delta-type ADC evaluations it is concluded that the ADC modulator sensitivity, response and quantization noise are dependent on certain feedback inductance and resistance values. It is also found that increased ADC modulator sensitivity decreases dynamic range. A simplified decimation filter structure is found to be effective for pre-filtered input signals. The ADM oversampling modulator shows non-linear behaviour

because of excessive quantizer switching even for small input signals. It is concluded that the ADM linearity can be improved by an increase of synchronizer channels and therefore an increase in circuit complexity. The simple delta-type modulator demonstrates good linearity, but it is concluded that more complex oversampling superconductor modulators are required to produce superior superconductor ADCs with performance exceeding that of ADC built with room-temperature electronics.

In spread spectrum communication systems the estimation of multi-path delay values can be rapidly determined by the use of superconductor electronics. It is found that very fast and effective correlation circuits can be implemented with superconducting electronics. Such fast correlation circuits can be supplied with data rapidly circulating in a circular FIFO queue structure that is loaded with a slow input signal. The RSFQ-based rapid multi-path delay estimator is found to function correctly at 10 GHz. Circuit size predictions show promising results for fabrication of the estimator on some of the larger available niobium die sizes.

6.4 Future research recommendations

Research following on any of the categories mentioned in Section 6.2, may benefit from the following recommendations:

- Recommendations for RSFQ Superconductor Electronics (SCE) research
  - Underdamped JJs allow faster JJ switching speeds [24]. It is recommended to explore the effect that the use of JJs with $\beta_c > 1$ have on RSFQ cell circuit yield as obtained through Monte Carlo analysis [25].
  - Optimization of all new cells are recommended.
- Recommendations for Superconductor ADC research
  - For research about superconductor oversampling ADC modulators it is recommended to first understand the modulator designs contributed in this thesis (DM and ADM) along with their advantages and disadvantages. It is then recommended to study and implement a PMD modulator. This modulator seems to be most popular because of the DR increases that are obtained by using multiple channel synchronizers based on the digitization of modulated pulse phases [38].

  - For research about superconductor decimation filters it is recommended to first understand the concepts of popular decimation filter structures such as the CIC decimation filter [55]. The implementations of large RSFQ decimation structures generally require many TFFs and therefore the optimization and accurate timing analysis of TFF cells are highly recommended. These timing restrictions should then be implemented in an HDL such as Verilog in order to verify decimation circuit operation by taking timing restrictions into consideration. After these evaluations effective RSFQ decimation circuits can be created.

- Recommendations on CDMA-based communication models

  - Study the book by Andrew Richardson on WCDMA design [15].
  - For more accurate channel models it is recommended to create WCDMA channel models where user signals are mixed with both channelization codes (OVSF) and scrambling codes.

- Recommendations on multiple-path delay estimation using RSFQ electronics

  - In order to produce effective path estimation circuits, optimization and accurate timing analysis of all cells are required for simulations that test functionality.
  - According to rapid multi-path delay estimator size predictions, it is small enough to fit on some of the larger niobium die sizes. For significant size reductions it is recommended that optimal FIFO buffers with minimal interconnection JTLs and clock splitting components are used in the rapid data supply circuits. The asynchronous FIFO buffer proposed by Hara *et al.* [54] is recommended for further research of the RSFQ-based estimator. It has a much smaller circuit area and could lead to the fabrication of the first RSFQ-based multi-path delay estimator.

Beyond the contributions in this thesis the following fields are recommended for further research into the field of superconductor applications in cellular base station receivers:

- An investigation into RSFQ-based multi-user CDMA detectors as described in Section 1.5 is recommended. These detectors basically require iterations at high clock speeds for CDMA channel parameter extraction.

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Appendix A

More on telecommunications

A.1 Dynamic Range

Dynamic range is encountered in industry and research in many different forms. In simple terms it is described as an indication of the range between the biggest signal and smallest signal that can be recognized in a system.

Dynamic range and signal to noise ratio of a device are very closely related and normally quoted in dB or some variant thereof.

Three common measures for the biggest signal are Peak-to-Peak, Zero-to-Peak and RMS Full-scale. As an example, for a $1\,V$ sine wave the three values are $2\,V$, $1\,V$ and $0.707\,V$ respectively.

A common measure for the smallest signal is the RMS noise with no signal applied. RMS noise depends on the bandwidth that it is measured over. Another measure is the least-significant-bit (LSB) which is applicable when working with ADCs. The LSB corresponds to the change of one in the numerical output of the converter.

Dynamic range (DR) can be generally expressed as follows:

$$DR = SNR = \frac{RMS\,full\,scale}{RMS\,noise} \tag{A.1}$$

$$DR\,(dB) = SNR\,(dB) = 20log_{10}\left(\frac{RMS\,full-scale}{RMS\,noise}\right) \tag{A.2}$$

For discrete systems such as the ADC, the ideal dynamic range is expressed as in eq. A.2 with:

$$RMS\,full-scale = \frac{2^{N-1}\times q}{\sqrt{2}} \tag{A.3}$$

Where N is the number of ADC resolution bits and q the LSB amplitude. Now all ADCs have rms noise that is generated by the quantization process. The ideal uncertainty of any ADC bit is $\pm 1/2\, LSB$ as shown in figure. When assumed that the quantization error is triangular as illustrated in figure, the quantization noise error can be given as:

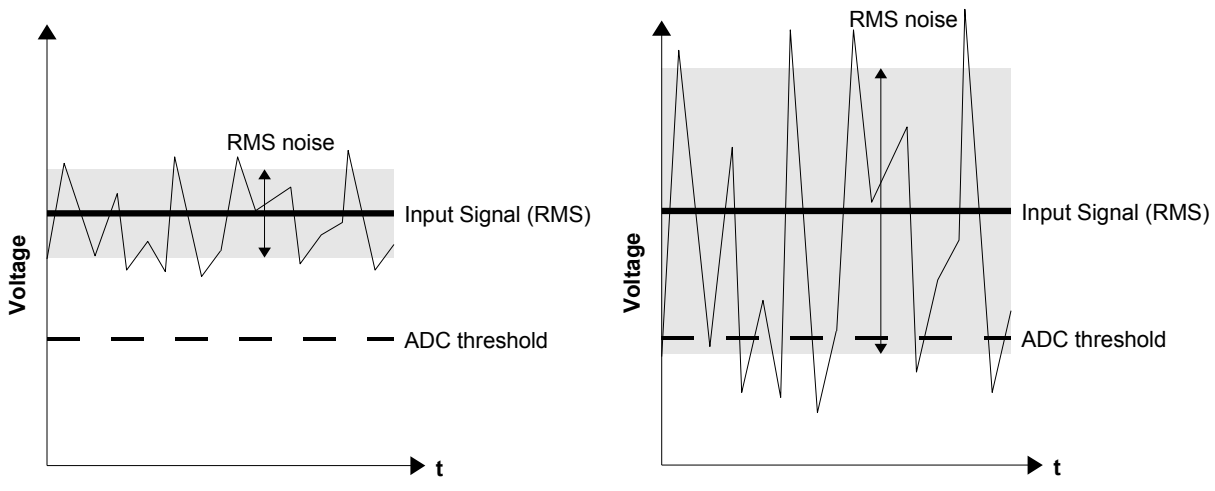
$$RMS\, noise = \frac{q}{2}\frac{1}{\sqrt{3}} = \frac{q}{\sqrt{12}} \tag{A.4}$$

With the rms value of a triangular error signal being its magnitude divided by $\sqrt{3}$. The ideal dynamic range of an ADC is then given as:

$$SNR_{ADC}(dB) = 20log_{10}\left(\frac{2^{N-1} \times q/\sqrt{2}}{q/\sqrt{12}}\right) = 6.02N + 1.76\ dB \tag{A.5}$$

Effective Number of Bits

Another form of dynamic range is the Effective Number of Bits (ENOB). This measurement is often used in ADC specifications and allows direct comparison between ADCs. In practice the resolution of an ADC is limited by the SNR of the signal being converted. Noise will limit the signal to be accurately converted past a certain number of bits of resolution. The full scale input signal should be at least twice as large as the RMS noise in order for the ADC to correctly discern the input signal (see Fig. A.1). Therefore SNR



(a) SNR > 2 (b) SNR < 2

Figure A.1: Effective bit requirements conceptually illustrated with a 1-bit ADC modulator

should be about $6\,dB$ per bit of resolution required. ENOB is expressed as follows with the full-scale range (FSR) being the range of the ADC for bipolar signals:

$$ENOB = log_{10}\left(\frac{FSR_{ADC}}{RMS\,noise}\right)/log_{10}2 = \frac{SNR_{ADC}(dB) - 1.76}{6.02} \tag{A.6}$$

Spurious Free Dynamic Range

Spurious free dynamic range (SFDR) is the ratio of the rms value of the signal to the rms value of the worst spurious signal regardless of where it falls in the frequency spectrum. The worst spur may or may not be a harmonic of the original signal. SFDR is an important specification in communications systems because it represents the smallest value of signal that can be distinguished from a large interfering signal. SFDR can be specified with respect to full-scale (dBFS) or with respect to the actual signal amplitude (dBc).

Signal to Noise and Distortion Ratio

Signal-to-Noise-and-Distortion (SINAD) is the ratio of the rms signal amplitude to the mean value of the root-sum-square (rss) of all other spectral components, including harmonics, but excluding DC. SINAD is a good indication of the overall dynamic performance of an ADC because it includes all components which make up noise and distortion. SINAD is often plotted for various input amplitudes and frequencies.

Appendix B

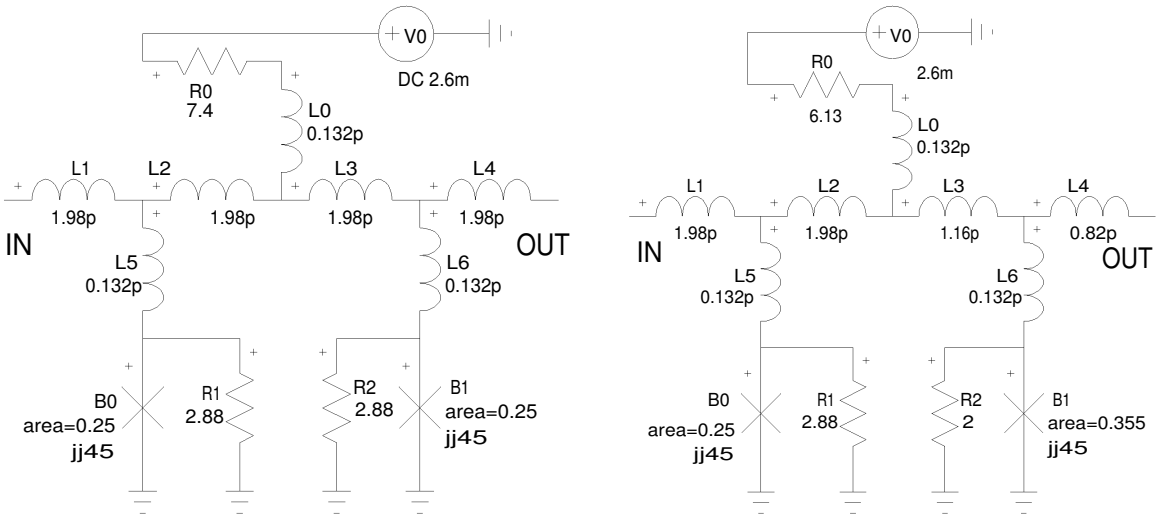
MATLAB Code

B.1 MATLAB Code for Josephson Junction Damping Resistance Calculator

```
Bc = 1; %Beta_c - damping characteristic
Q = 2.067833636e-15; %one magnetic flux quantum
Ic = [148; 171; 194; 200; 212;
      237; 245; 250; 275; 305; 325; 355];  %JJ Critical current
Jc = 45e-6; %fabrication specific current density
ICRN = 1.3e-3; %Normal Resistance Product

Ic = Ic*1e-6;
rn = ICRN./Ic;

Cs = 69e-15; %Capacitance per unit area
a = Ic./Jc;
Cj = Cs.*a;     %Specific JJ capacitance

Rj = sqrt(Bc*Q./(2*pi.*Ic.*Cj)); %Total required JJ shunt resistance
Rs = Rj.*rn./(rn-Rj); %Required Shunt resistor in parallel
 with rn to obtain Bc
```

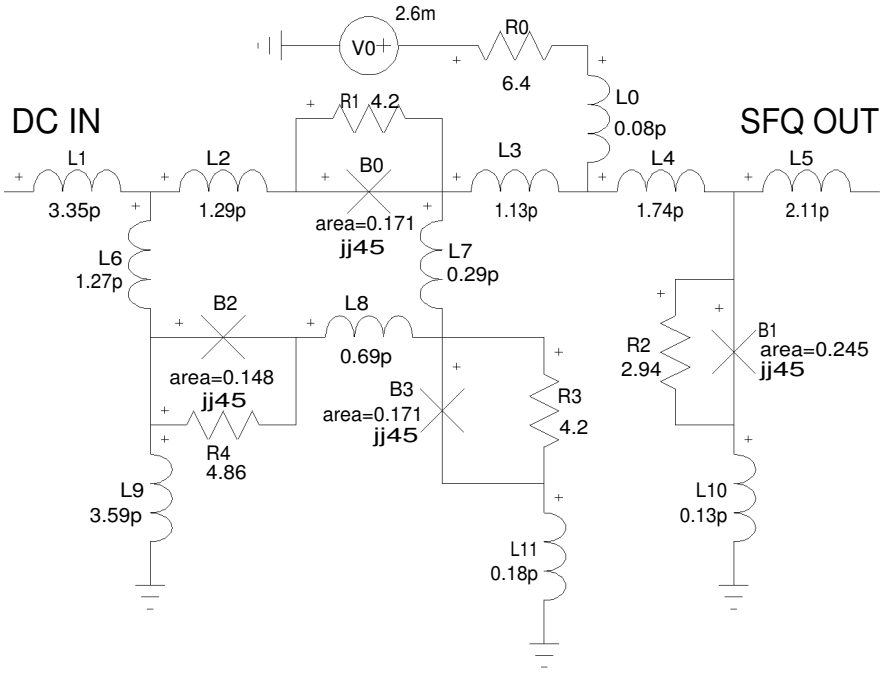
Appendix C

RSFQ cell diagrams

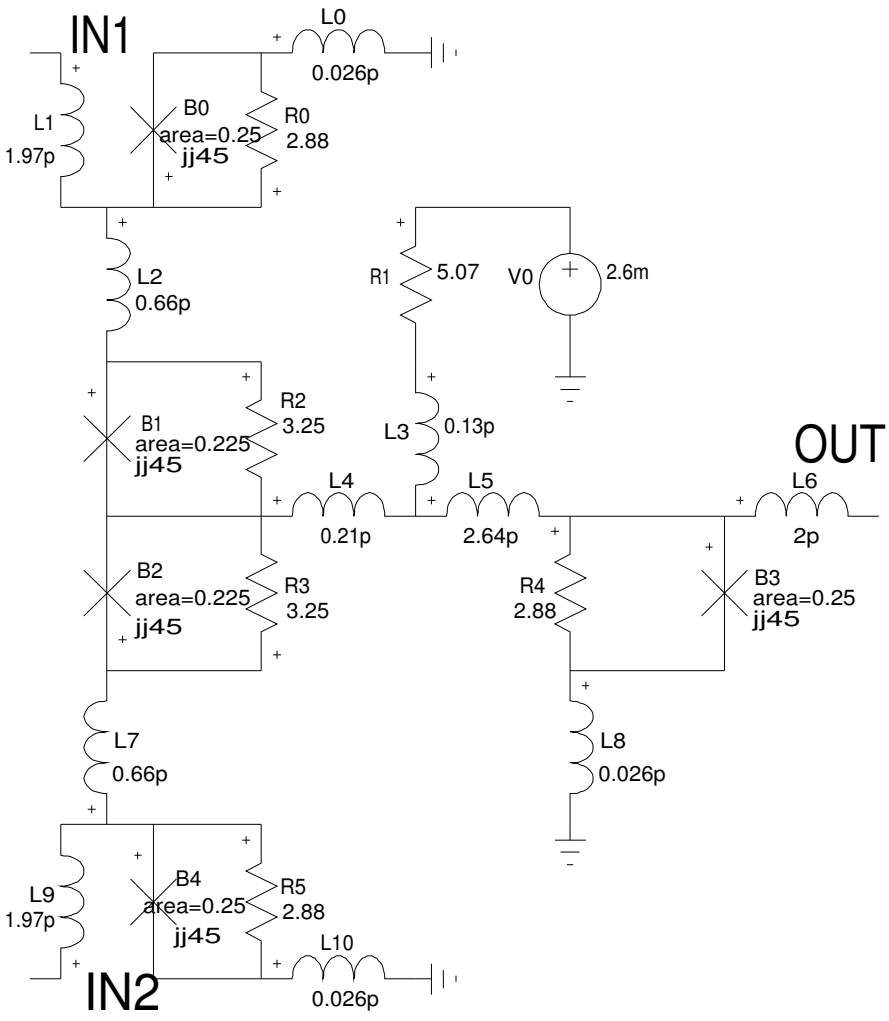


(a) (b)

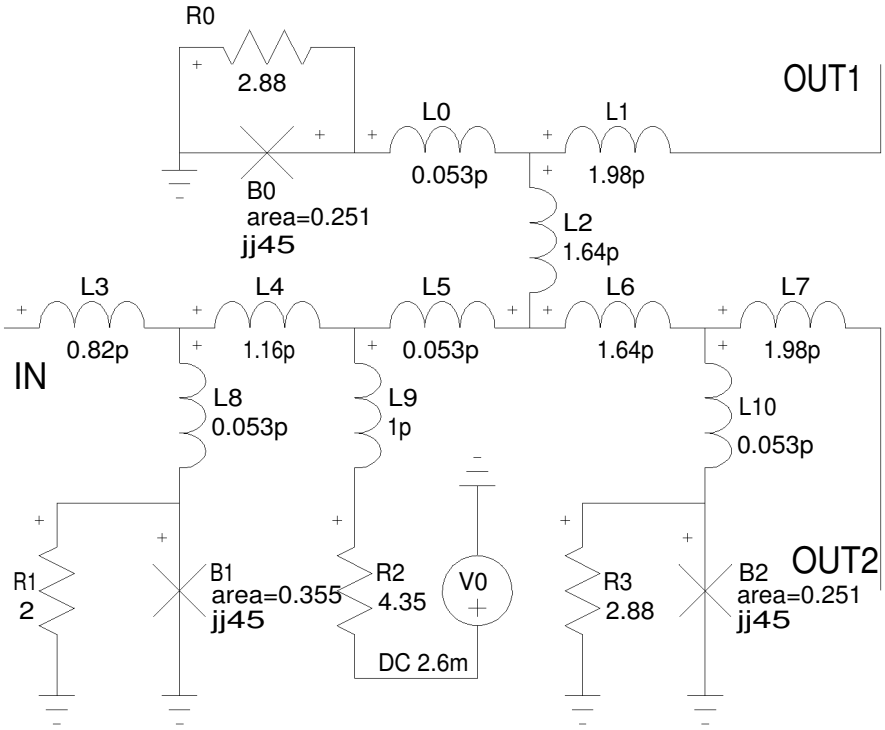
JTL Circuit Diagrams for (a) $250\mu A$-JTL and (b) $250\mu A - 355\mu A$-JTL



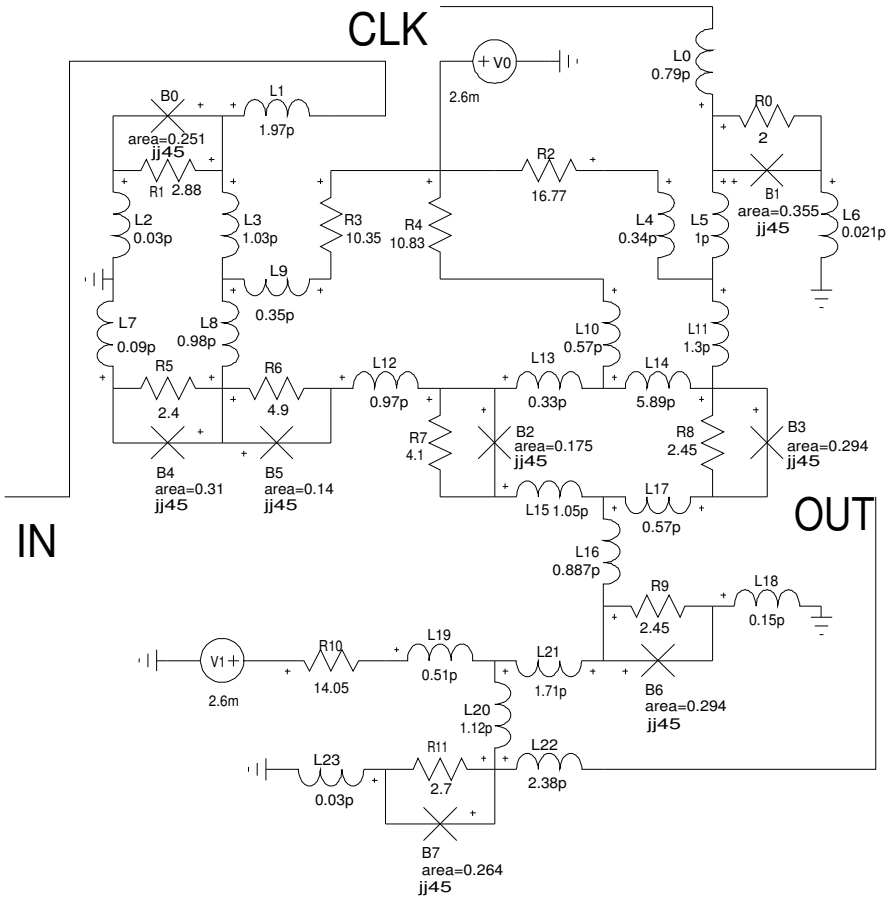
DC-to-SFQ Converter (DC-SFQ)



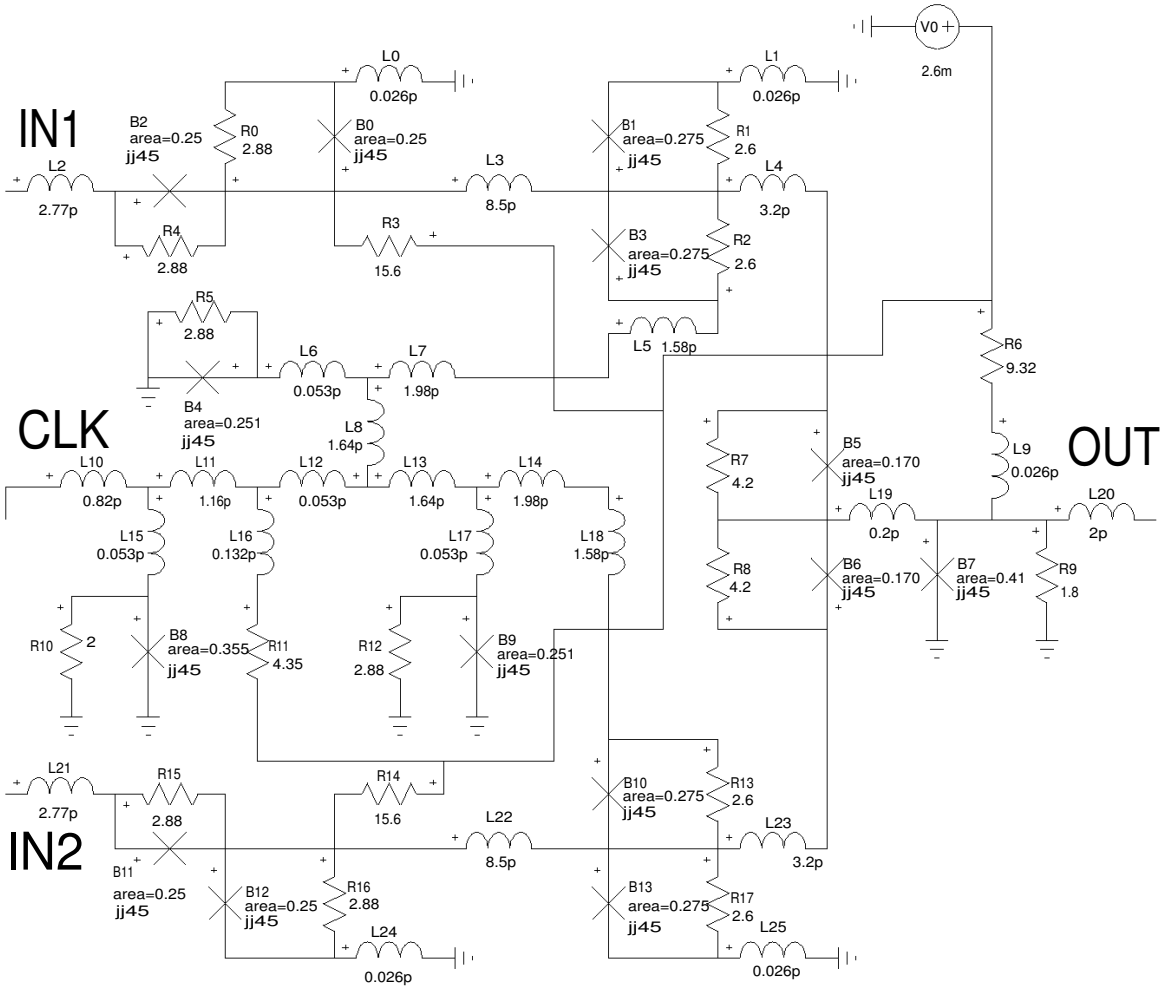
Pulse Merger



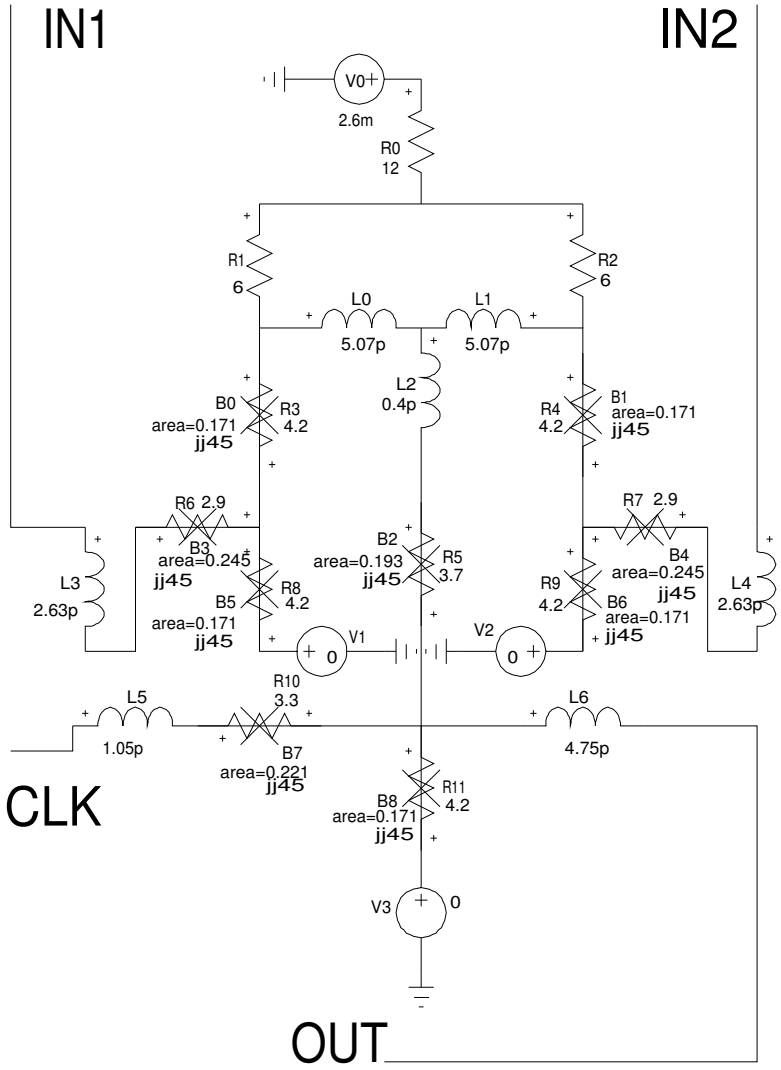
Pulse Splitter



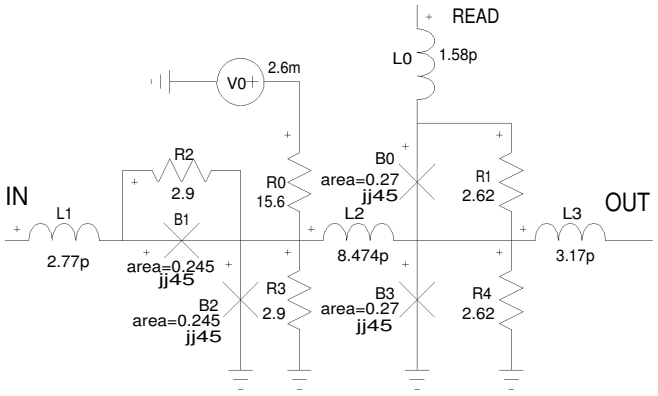
Inverter (NOT)


V0
2.6m
L0
0.026p
L1
0.026p
IN1
B2
area=0.25
jj45
R0
2.88
B0
area=0.25
jj45
B1
area=0.275
jj45
R1
2.6
L2
2.77p
L3
8.5p
L4
3.2p
R4
2.88
R3
15.6
B3
area=0.275
jj45
R2
2.6
R5
2.88
L5
1.58p
R6
9.32
L6
0.053p
L7
1.98p
B4
area=0.251
jj45
L8
1.64p
CLK
OUT
L10
0.82p
L11
1.16p
L12
0.053p
L13
1.64p
L14
1.98p
R7
4.2
B5
area=0.170
jj45
L9
0.026p
L19
0.2p
L20
2p
L15
0.053p
L16
0.132p
L17
0.053p
L18
1.58p
R8
4.2
B6
area=0.170
jj45
B7
area=0.41
jj45
R9
1.8
R10
2
B8
area=0.355
jj45
R11
4.35
R12
2.88
B9
area=0.251
jj45
L21
2.77p
R15
2.88
R14
15.6
B10
area=0.275
jj45
R13
2.6
IN2
L22
8.5p
L23
3.2p
B11
area=0.25
jj45
B12
area=0.25
jj45
R16
2.88
B13
area=0.275
jj45
R17
2.6
L24
0.026p
L25
0.026p

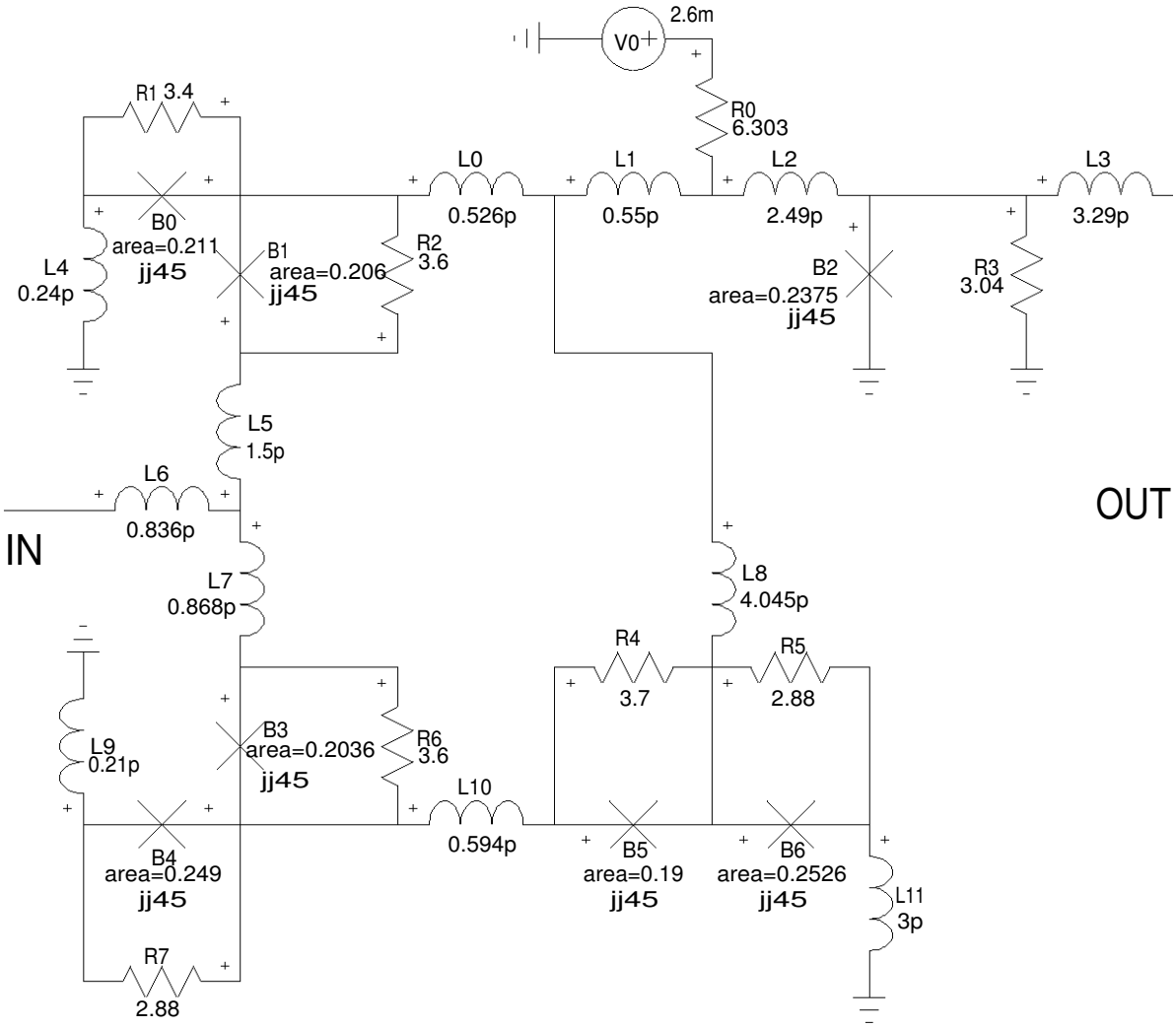
AND Gate



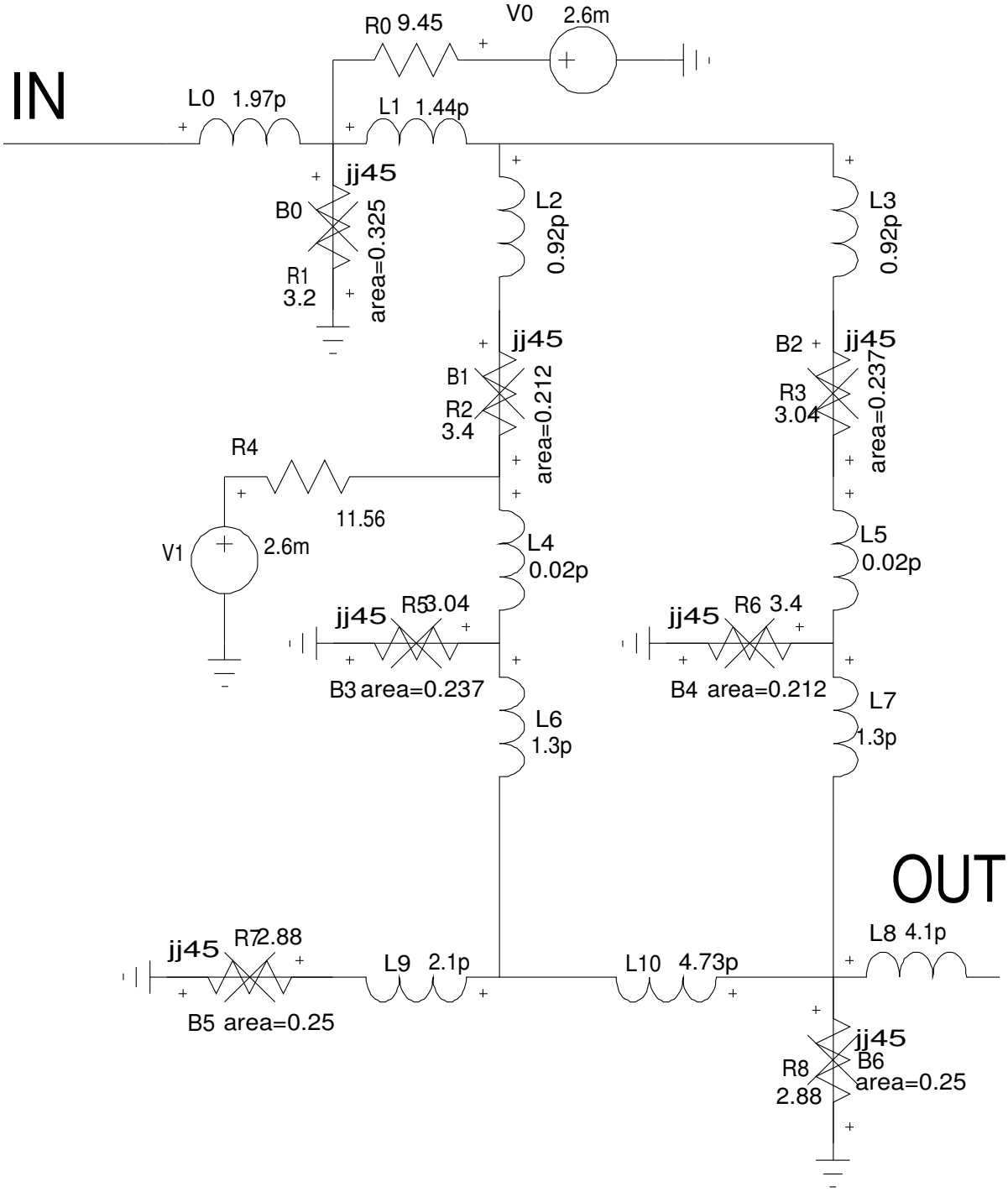
Exclusive-OR (XOR)



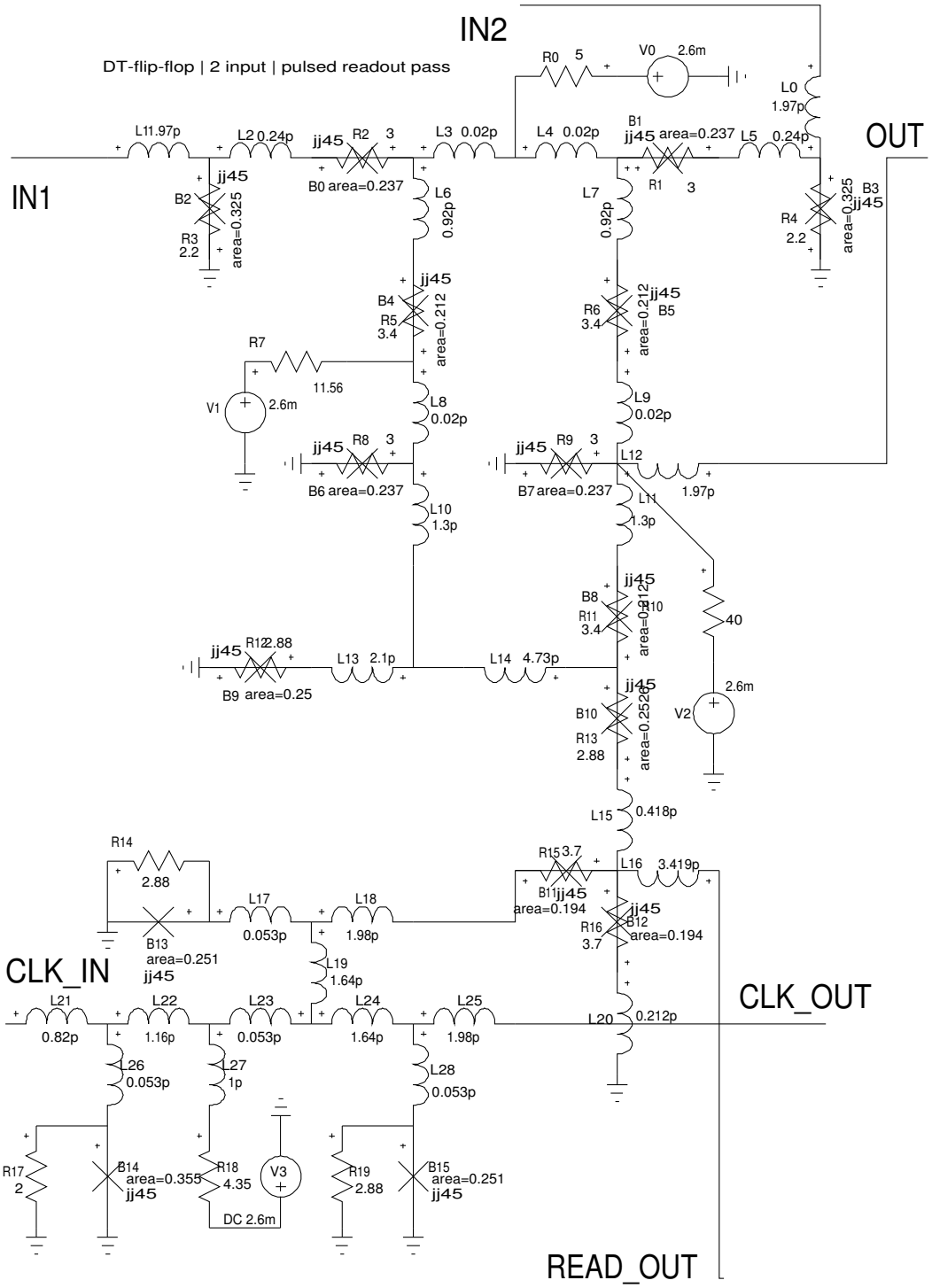
Destructive Readout Register (DRO)



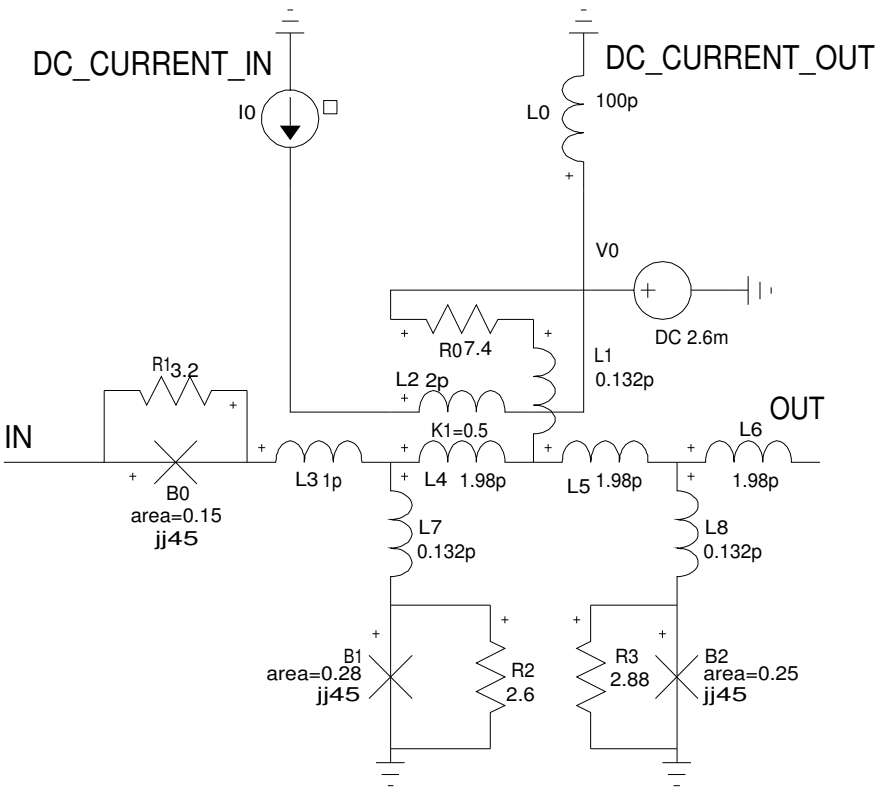
T1FF Circuit



T2FF Circuit



DT2FF Circuit



DC-enabled JTL (DCE-JTL)

Appendix D

Monte Carlo Analysis Files

D.1 DCE-JTL yield calculation

```
* Generated by Xic from cell dc-en-jtl
* WRSpice Monte Carlo circuit file - generated by MConvert
* File edited for insertion into document - subcircuits removed
.monte
.exec
checkSTP1=5
checkSTP2=5
* global variations
let Jtol = gauss(0.1/3,1)
let Ctol = gauss(0.05/3,1)
let Rtol = gauss(0.2/3,1)
let Ltol = gauss(0.1/3,1)
.endc
.control
if (tg1*90e-12) > 0.5f
  let checkFAIL=1
end
if (tp1*40e-12) < 1.5f or (tp1*40e-12) > 2.5f
  let checkFAIL=1
end
if (tg2*151e-12) > 0.5f
  let checkFAIL=1
```

```
end
if (tp2*40e-12) < 1.5f or (tp2*40e-12) > 2.5f
  let checkFAIL=1
end
if (tg3*139e-12) > 0.5f
  let checkFAIL=1
end
if (tg4*101e-12) > 0.5f
  let checkFAIL=1
end
if (tp3*40e-12) < 1.5f or (tp3*40e-12) > 2.5f
  let checkFAIL=1
end
if (tg5*329e-12) > 0.5f
  let checkFAIL=1
end
.endc
* local variations
.param Jvar = Jtol*gauss(0.05/3,1)
.param Avar = gauss(0.05/3,1)
.param Rvar = Rtol*gauss(0.05/3,1)
.param Lvar = Ltol*gauss(0.15/3,1)
.measure tran tg1 from=20p to=110p avg v(4)
.measure tran tp1 from=115p to=155p avg v(4)
.measure tran tg2 from=160p to=311p avg v(4)
.measure tran tp2 from=316p to=356p avg v(4)
.measure tran tg3 from=361p to=500p avg v(4)
.measure tran tg4 from=20p to=121p avg v(19)
.measure tran tp3 from=126p to=166p avg v(19)
.measure tran tg5 from=171p to=500p avg v(19)
.tran 0.25p 500p 0 0.5p UIC
B0 4 3 18 jjmc1 area=$&(0.15*Avar)
B1 2 0 17 jjmc2 area=$&(0.28*Avar)
B2 1 0 16 jjmc3 area=$&(0.25*Avar)
I0 0 7 pwl 0 -500u 100p 500u 200p 500u 300p -500u
K1 L4 L2 0.5
```

```
L0 6 0 $&(100p*Lvar)
L1 14 13 $&(0.132p*Lvar)
L2 7 6 $&(2p*Lvar)
L3 3 10 $&(1p*Lvar)
L4 10 13 $&(1.98p*Lvar)
L5 13 9 $&(1.98p*Lvar)
L6 9 12 $&(1.98p*Lvar)
L7 10 2 $&(0.132p*Lvar)
L8 9 1 $&(0.132p*Lvar)
R0 5 14 $&(7.4*Rvar)
R1 3 4 $&(3.2*Rvar)
R2 11 8 $&(28*Rvar)
R3 2 0 $&(2.6*Rvar)
R4 1 0 $&(2.88*Rvar)
V0 5 0 DC $&(2.6m*Rtol*Jtol)
V1 8 0 sin 0 10m 5g 100p
X0 12 19 jtl-250-term
X1 15 4 jtl_250
X2 11 15 dc-sfq

.model jj45 jj(rtype=1, cct=1, icon=10m, vg=2.5m, delv=0.1m,
+ icrit=1m, r0=13, rn=1.3, cap=1.5333p)
*Nb 4500 A/cm2   area = 22.2 square microns (generated by JJMODEL)
.save @I0[c]
.model jjmc1 jj(rtype=1, cct=1, icon=10m, vg=2.5m, delv=0.1m,
+ icrit=$&(1m*Jvar), r0=13, rn=1.3, cap=$&(1.5333p*Ctol))
*Nb 4500 A/cm2   area = 22.2 square microns (generated by JJMODEL)
.model jjmc2 jj(rtype=1, cct=1, icon=10m, vg=2.5m, delv=0.1m,
+ icrit=$&(1m*Jvar), r0=13, rn=1.3, cap=$&(1.5333p*Ctol))
*Nb 4500 A/cm2   area = 22.2 square microns (generated by JJMODEL)
.model jjmc3 jj(rtype=1, cct=1, icon=10m, vg=2.5m, delv=0.1m,
+ icrit=$&(1m*Jvar), r0=13, rn=1.3, cap=$&(1.5333p*Ctol))
*Nb 4500 A/cm2   area = 22.2 square microns (generated by JJMODEL)
```