

Predictive Control of a Series-Input, Parallel-Output, Back-to-Back, Flying-Capacitor Multilevel Converter

by

Daniël Josias du Toit

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Department of Electrical and Electronic Engineering
University of Stellenbosch
Private Bag X1, 7602, Matieland, South Africa.

Supervisor: Prof. H. du T. Mouton

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Declaration

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Summary

This thesis investigates the viability of constructing a solid-state transformer (SST) with a series-input, parallel-output connection of full-bridge, three-level flying-capacitor converters. It focusses on the active rectifier front-end of the SST which is used to control the input current to be sinusoidal and in-phase with the sinusoidal input voltage. A stack of two converters are built and tested. The input current, as well as the flying capacitor voltages of the two active rectifiers in the stack, are actively controlled by a finite-state model-based predictive (FS-MPC) controller.

The use of multiple flying-capacitor converters poses a problem when using FS-MPC because of the large number of possible switching states to include in the prediction equations. Three FS-MPC control algorithms are proposed to attempt to overcome the problem associated with the large number of switching states. They are implemented on an FPGA digital controller. The algorithms are compared on the bases of voltage and current errors, as well as their responses to disturbances that are introduced into the system. The simulation and experimental results that are presented shows that by interleaving the control actions for the two converters, one can obtain fast and robust responses of the controlled variables. The viability of extending the interleaving control algorithm beyond two converters is also motivated.

Opsomming

Hierdie tesis ondersoek die moontlikheid van volbrug, drievlak vlieënde-kapasitoromsetters wat gebruik word om 'n serie-intree, parallel-uitree drywingselektroniese transformator (DET) te bou. Dit fokus op die aktiewe gelykrichter van die DET wat gebruik word om die intreestroom te beheer om sinusvormig en in fase met die sinusvormige intreespanning te wees. 'n Stapel van twee omsetters word gebou en getoets. Die intreestroom, sowel as die vlieënde kapasitorspannings van die twee aktiewe gelykrichters in die stapel, word aktief beheer met behulp van 'n eindige-toestand, model-gebaseerde voorspellende beheerder (ET-MVB).

Die gebruik van veelvuldige vlieënde-kapasitoromsetters bemoeilik die implementering van 'n ET-MVB-beheerder as gevolg van die groot aantal skakeltoestande wat in die voorspellende vergelykings in ag geneem moet word. Drie ET-MVB-algoritmes word voorgestel om te poog om die probleme, wat met die groot aantal skakeltoestande geassosieer word, te oorkom. Die algoritmes word in 'n FPGA digitale verwerker geïmplementeer. Die algoritmes word vergelyk op grond van hul stroom- en spanningsfoute, asook hul reaksie op steurings wat op die stelsel ingevoer word. Die simulاسie en praktiese resultate toon dat, deur die beheeraksies vir die twee omsetters te laat oorvleuel, die gedrag van die beheerde veranderlikes vinniger en meer robuust is. Die moontlikheid om die oorvleuelende beheeraksies uit te brei tot meer as twee omsetters word ook gemotiveer.

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Nomenclature

AC	Alternating Current
ADC	Analogue-to-Digital Converter
α	Cost Function Weight
APOD	Alternative Phase Opposition Disposition
β	Cost Function Weight
C	Capacitance
CAT5	Unshielded Twisted Pair Type Cable Connector
D	Duty Cycle
DC	Direct Current
DCM	Discontinuous Conduction Mode
DSP	Digital Signal Processor
EEPROM	Electrically Erasable Programmable Read-Only Memory
f_{iso}	Isolation Stage Switching Frequency
FPGA	Field-Programmable Gate Array
f_{pre}	Predictive Controller Prediction Frequency
f_s	Switching Frequency
FS-MPC	Finite-State Model-based Predictive Control
IO	Input-Output
L	Inductance
LCD	Liquid Crystal Display

LVDS	Low-Voltage Differential Signalling
LV	Low Voltage
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPC	Model-based Predictive Control
MV	Medium Voltage
N	Number of Stacked Converters
PCB	Printed Circuit Board
PD	Phase Disposition
PID	Proportional-Integral-Derivative
PI	Proportional-Integral
PLL	Phase-Locked Loop
PWM	Pulse-Width Modulation
R	Resistance
RMS	Root-Mean-Square
SIPO	Series-Input, Parallel-Output
SPWM	Sinusoidal Pulse-Width Modulation
SST	Solid-State Transformer
T_{iso}	Isolation Stage Switching Period
T_{pre}	Predictive Controller Prediction Period
T_s	Switching Period

Chapter 1

Introduction

1.1 Background

In recent years the applications of power electronics in power systems have increased due to the advancements in available hardware, namely faster digital controllers and power switches with higher voltage and current ratings. This led to the study of a solid-state transformer (SST) consisting of high voltage power electronics with the purpose of replacing existing iron core transformers. The first mention of the SST concept is found in 1980 [1], although the technology did not exist at the time the concept's future viability was clear. With better hardware available today the concept made a new attempt to be implemented [2–4]. This replacement of iron core transformers does have its advantages [5, 6]:

- **Input power factor correction:** Depending on the topology used the converter can be able to draw currents on its medium voltage (MV) side which are sinusoidal and have a specific phase relation with the input voltage. The SST can therefore be used as an active power factor correction tool while delivering power to its low voltage (LV) side.
- **Near perfect output voltage regulation:** The three-phase output of the SST is generated with an actively controlled inverter. The fast response of these converters ensures that the output voltages are regulated even under load changes or non-linear load conditions.
- **Harmonic filtering:** Harmonic content generated by non-linear loads are not transferred to the MV side of the SST.
- **Output short circuit protection:** The controller of the SST will be able to sense fault conditions and limit the output current as to not disturb the primary side.

- **Voltage dip and swell compensation:** The added capacitance of the SST can be used to keep the output voltages regulated under input voltage dip or swell conditions.
- **Single phase or three phase operation:** The SST can be configured to operate from either a single or three-phase supply and it can either supply a single- or three-phase load.
- **Supply frequency variation:** The primary and secondary sides of the SST are controlled separately and can therefore operate where the input and output frequencies are not necessarily the same.
- **Capable of supplying a DC voltage:** The DC voltages of the bus capacitors are available for DC supplies.
- **Operation under a fault condition:** Depending on the fault conditions, the SST may be able to only cut out one of its output phase while still delivering power to the remaining two.

The project in this report stems from work done by Stellenbosch University on such an SST [6]. The topology used for the 11 kV-to-400 V three-phase solid state transformer is based on a series stack of full-bridge, back-to-back converters [5]. Each back-to-back converter forms a cell, shown in Figure 1.1. These cells are stacked, shown in Figure 1.2, to obtain the required input voltage rating. Because the total working voltage of the SST is much higher than the blocking voltage capability of each of the power transistors used, the correct voltage balancing of the cell voltages were important. The natural balancing of the cell voltages was proved by [7, 8].

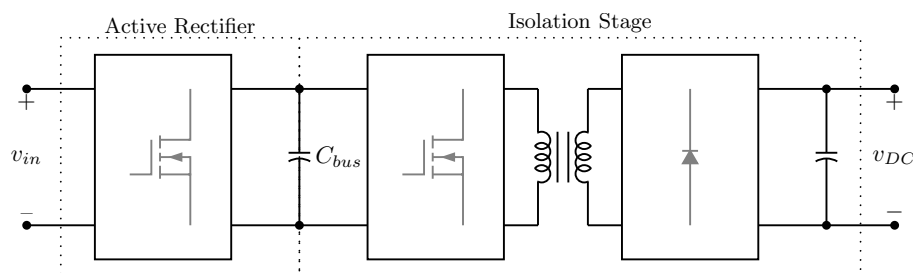
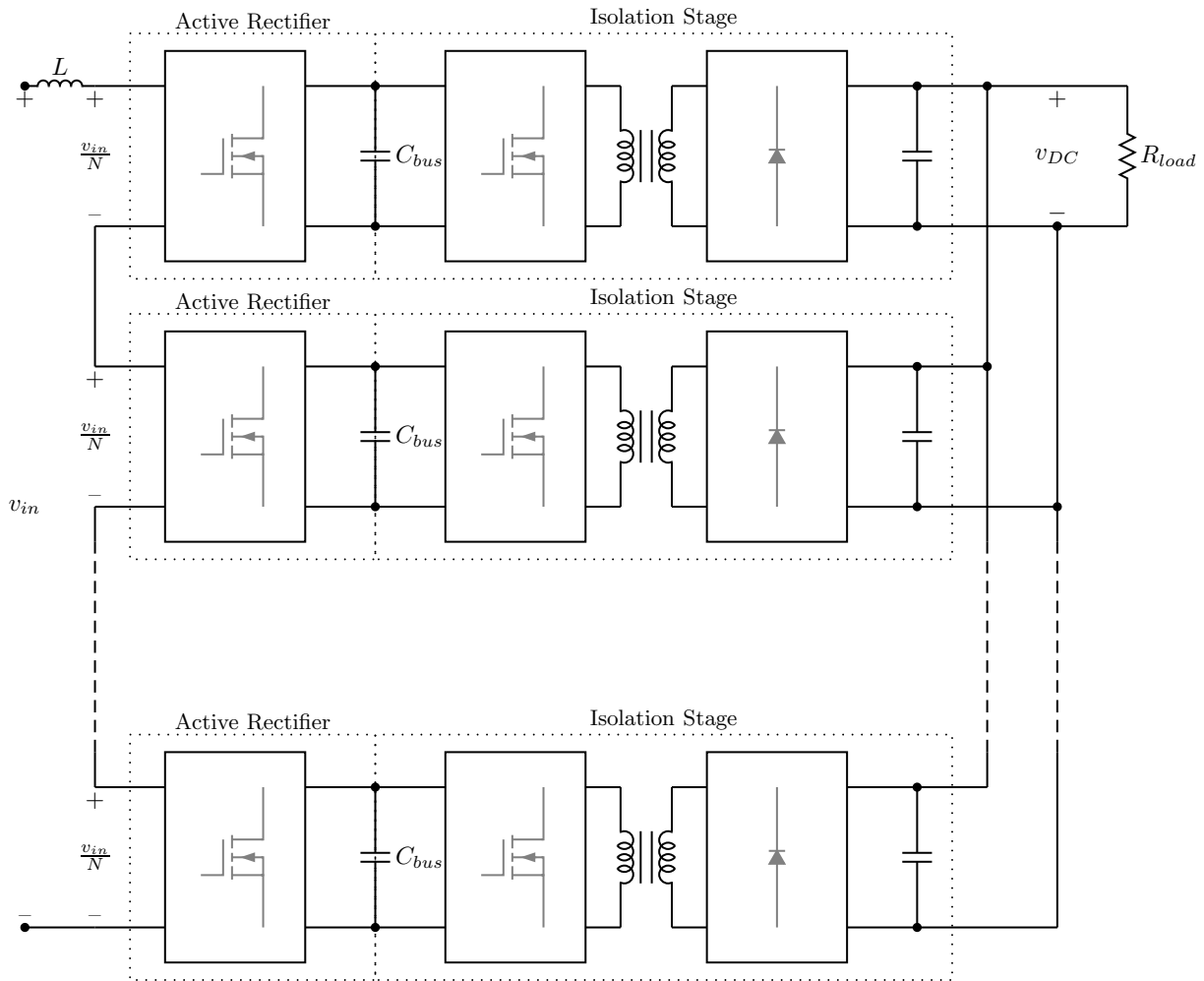


Figure 1.1: A single cell of a stacked converter.

The SST prototype was successfully implemented on a 6.6 kV scale using 36 cells. One stack consisting of 12 cells is shown in Figure 1.3. Also, 36 cell controllers and three main controllers [9, 10] were needed to control the three-phase, stacked converter. The question arises whether it is possible to reduce the amount of hardware. If three-level, instead

Figure 1.2: An N -cell stack topology.

of the full-bridge, converters are used, the amount of cells needed will be halved. The amount of cell controllers will also be halved. This will reduce the cost and complexity of the system. The problem with using multilevel converters is that their internal voltages that to be balanced. Furthermore, the SST call for a cell converter than can be stacked in series to achieve a total voltage rating that is higher that a single cell's rating.

Although [11] suggested against the use of multilevel converters due to their cost, it became necessary to be able to compare the use of different cell topologies. Multilevel inverters have been successfully implemented [12, 13] the difficulty being to balance the internal voltages of the converter [14–19]. These converters have also been coupled with predictive control methods [20–26]. These were able to regulate the internal voltages of the converter, as well as to produce the required output waveforms. Multilevel converters have, however, not been applied as series stacked active rectifiers.

The authors of [11] compared the diode-clamped, flying-capacitor and series stacked full-bridge converters mostly on their cost. They did not, however, consider using a series stack of multilevel converters such as this thesis will investigate. Therefore, repeating their



Figure 1.3: Twelve-cell stack of the 6.6 kV SST.

comparison, the cost of a three-phase 6.6 kV SST for a series stacked full-bridge, diode-clamped and flying-capacitor converter is given in Table 1.1. The breakdown of the cost analysis is shown in Appendix A. The diode-clamped and flying-capacitor converters are both taken to be full-bridge, three-level converters. Each, therefore, has eight transistors in both the rectifier and isolation stage. The total amount of transistors is therefore the same between the three topologies. The assumption is made that the bus- and flying capacitors should equal $300 \mu\text{F}$ with the bus capacitors having a voltage rating of 800 V and the flying capacitors a minimum rating of 400 V. 800 V, $60 \mu\text{F}$ and 450 V, $100 \mu\text{F}$ capacitors are available to make up the $300 \mu\text{F}$ totals. Furthermore, the assumption is made that each cell controller carries a cost of R1 500.00.

From the cost evaluation it is clear the diode-clamped and flying-capacitor topologies have similar costs. The cost therefore does not have any influence on deciding on the topology for this thesis. A detail analysis of the cost should however be done but for the purpose of defending the choice in topology for this thesis the analysis is sufficient. The flying-capacitor converter does have the added advantage of larger internal capacitance. This could prove useful in dip/swell prone power systems where the added capacitance could provide longer periods of ride-through during dip conditions. The flying-capacitor topology is therefore chosen for this thesis.

Table 1.1: Cost comparison of SST topologies.

	Full-Bridge	Flying-Capacitor	Diode-Clamped
Cells	36	18	18
Controllers	36	18	18
	R54 000	R27 000	R27 000
800 V, 20 A Transistors	288	288	288
60 μ F, 800 V Capacitors	180	90	0
	R19 000	R9 500	0
100 μ F, 450 V Capacitors	0	216	216
	0	R26 000	R26 000
400 V, 20 A Diodes	0	0	144
	0	0	R5 750
Comparative Total	R73 000	R62 500	R58 750

1.2 Study Objectives

The aim of this project is to provide a proof-of-concept for replacing the full-bridge converters in the SST prototype with multilevel converters. A laboratory prototype of two stacked full-bridge, three-level flying-capacitor converter cells should be built and tested. To achieve this objective the following needs to be completed:

- Study series-input, parallel-output converters and controllers to be able to re-design the converter cell.
- Study diode-clamped and flying-capacitor converters to be able to choose and design a converter that is suited for a series stacked application.
- Study predictive control techniques to be able to choose and design a predictive controller for the series stacked converter.
- Design a suitable multilevel converter.
- Design a suitable predictive controller to control a series stack of two converters.
- Simulate the proposed converter topology and controller.
- Confirm the correct working of both the stacked converter and the predictive controller on a laboratory prototype.
- Comment on the viability of extending the two converters for a medium voltage application.

1.3 Thesis Overview

The literature review starts in Chapter 2 with an overview of the solid-state transformer concept. Different SST topologies are given and the series-input, parallel-output (SIPO) topology is further discussed. The contents of one cell of such a SIPO converter is given. The active rectifier front-end of the cell is used to let the converter operate at unity power factor on its primary side. This is achieved by controlling the input current of the converter to be sinusoidal and in-phase with the input voltage. The front-end thus converts the AC input to DC. The isolation stage converts the DC voltage to a high frequency square wave, passes it through a high frequency transformer and then rectifies it again by means of a passive rectifier. This stage is needed to be able to connect all the outputs from the cells in parallel when they are stacked in series. The reason for stacking the converters is to be able to achieve higher voltage rating on the input side. The voltage balancing required by the series stack is also discussed. It relies on the fact that a higher DC bus voltage will deliver more power to the load resulting in a drop in the voltage of that bus. The bus voltages will therefore balance naturally. Although the bus voltages will balance with respect to each other they will not balance naturally to a specific reference voltage. The double loop controller for this is shown. It consists of the inner loop that controls the input current to be sinusoidal and the outer loop that regulates the sum of the bus voltages. The outer loop controls the magnitude of the input current in order to regulate the bus voltages.

Chapters 3 and 4 give overviews of the diode-clamped and flying-capacitor multilevel converters, respectively. The basic converter layout and operation of both is given. The diode-clamped multilevel converter has a split DC bus capacitor that provides different voltage levels. The three-level converter has two bus capacitors each having voltage of $\frac{1}{2}v_{bus}$. Apart from the four power switches this three-level converter also requires two clamping diodes. Its clamping mechanism uses the different voltages from the DC bus capacitors to clamp the voltage across an off-state power switch. The flying-capacitor converter has only a single bus capacitor but the three-level converter requires one flying capacitor. This flying capacitor needs to have a balanced voltage of $\frac{1}{2}v_{bus}$ in order for the switching waveform and clamping mechanism to function correctly. Simulation results for both converter types are given.

Different predictive control strategies are discussed in Chapter 5. The concepts of a cost function, receding horizon and computational effort are discussed. Hysteresis-based control aims to keep the controlled variable within a defined boundary while trajectory-based control aims to keep the variable on the shortest trajectory towards the reference. Dead-beat control uses a modulator to produce the switching signals for a power electronic

converter. The reference value for the modulator that will result in a zero error between the converter output and output reference is calculated at each sampling instant. Model-based predictive control, with and without a modulator, where a cost function is used to choose the control action is also discussed. Modelling a system to be used with predictive controllers and approximating differential and integral operations in these models are also reviewed. Euler backward and forward, and the fourth-order Runge-Kutta approximations are mentioned while Euler's forward method is used in an example simulation of model-based predictive control.

The designing of the converter is done in Chapter 6. The active rectifier and isolation stage is handled separately. For the active rectifier we have to adapt the well known PWM design equations to accommodate the predictive controller. The losses in the power switches are calculated on a worst-scenario case: for the conduction losses we assume the switch conducts 100% of the time, and for the switching losses we assume that the switch switches at every possible instance. The bus capacitor and flying capacitors are also designed for a less than 5% voltage ripple. For the isolation stage the balancing of the flying capacitor voltages need to be considered. As the back-end is not actively controlled, while the flying capacitor voltages still need to be balanced, balance resistors are used. Knowing that the isolation stage operates at a fixed duty cycle and frequency the resistors can be designed. To power the driver circuits for all the power switches a bootstrap supply is designed.

Chapter 7 concludes the designs with the controller hardware and control algorithms. The measurement circuits are designed taking into account that some of the voltage measurements will have to be taken at a floating ground reference. An isolated op-amp and power supply unit are used to isolate the measurement resistors from the ADC. The input current is measured with a series resistor instead of a hall-effect sensor. The small amount of current makes an hall-effect sensor inaccurate. The switching signals for the power switches are carried via optic fibre links. The control algorithms is developed next. The algorithms for controlling the input current and the internal voltages for a single and dual converters are given. The voltage controller to regulate the bus voltages is also designed.

Simulation and experimental results are given in Chapters 8 and 9, respectively. Simulations are done to verify the correct design of the converters, as well as the functioning of the control algorithms. The experimental results include measurements taken to compare the three proposed control algorithms. Step disturbances and steady-state measurements are used for the comparisons. Chapter 10 concludes this thesis with some conclusions and recommendations.

Chapter 2

The Solid-State Transformer

The author of [1] was the first to propose the use of power electronics for a medium voltage solid-state transformer (SST) application. The advantages that an SST has over a conventional line frequency transformer is plentiful: active power filtering; perfect output voltage; ability to output any frequency; ability to interconnect systems with different frequencies or phases; and voltage dip/sag compensation to name but a few. The authors of [11] compared the use of different converter topologies by means of cost and proposed the use of a series-input, parallel-output converter topology. It was compared to the flying-capacitor and diode-clamped multilevel converters. The series connection of smaller converters on the medium voltage input side is to overcome the voltage limitations of available power switches as the applied voltage is divided between all the converters in the series stack. A 6.6 kV three-phase prototype was constructed [5, 9, 10]. Each phase consisted of 12 cells, each with its own digital controller receiving commands from three main controllers. The voltage balancing between the converters in the stack is of utmost importance to keep the total system voltage divided equally between the stacked converters. Voltage balancing mechanisms were investigated in [8, 27–29]. Other implementations of SST converters, also known as intelligent universal transformers, can be found in [3, 4, 30].

This chapter will give a brief overview of the series-input, parallel-output converter topology proposed by [11] and constructed by [5, 9, 10]. It will also discuss the balancing mechanisms present at the topology and the basic double-loop control strategy to control the active rectifier front-ends will be shown.

2.1 Converter Overview

The AC/AC buck converter is possibly the most simple approach to a single phase, power electronics-based transformer. Such an AC/AC converter is shown in Figure 2.1. Each

power switch consists of n power devices to make up the desired voltage rating of the converter and S_1 and S_2 operate complimentary to each other. The relationship between the input and output voltage is given by $\frac{v_{out}}{v_{in}} \approx D$ [31] where D is the duty cycle of S_1 .

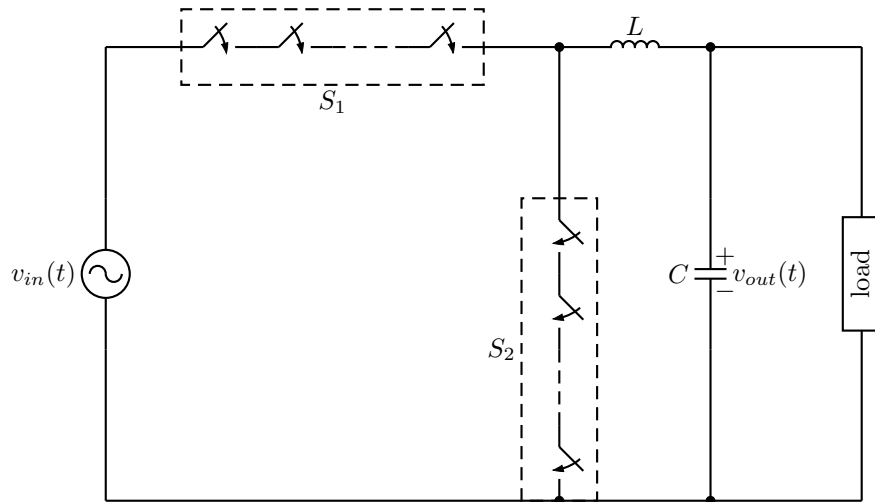


Figure 2.1: AC/AC buck converter.

This approach, although simple and easy to control, is problematic in several areas. Both switch groups S_1 and S_2 need to block total input voltage. For that reason each group consists of several individual power switches. The switches should also be capable of conducting the full load current. The high voltage, high current requirements of the power devices makes the design costly. Other drawbacks are the lack of magnetic isolation; inability to do power factor correction on the input; and its inability to provide dip/sag compensation [4]. These, and other disadvantages, make the use of the AC/AC buck converter unsuitable for the use in medium voltage applications.

An alternative to the AC/AC buck converter has been proposed by [32]. The author's proposed topology is shown in Figure 2.2. The sinusoidal input voltage is modulated by the front-end converter to a high frequency square wave and then passed through the high frequency transformer. The back-end converter synchronously demodulates the output voltage at the secondary winding of the transformer. The topology provides the advantages of reducing the transformer size and voltage stresses on components. It does not, however, provide any added benefits regarding control or power factor improvements.

The topology suggested by [11] has the same advantages as mentioned above, as well as control over the power factor, dip/sag compensation and other power quality benefits. A single cell of such a series-input, parallel-output converter is shown in Figure 2.3. The cell is the building block of the SST concept. The front-end is an active rectifier to convert the 50 Hz input voltage to DC. The isolation stage then converts the DC to a high frequency square wave to pass it through the isolation transformer to the passive rectifier. For the

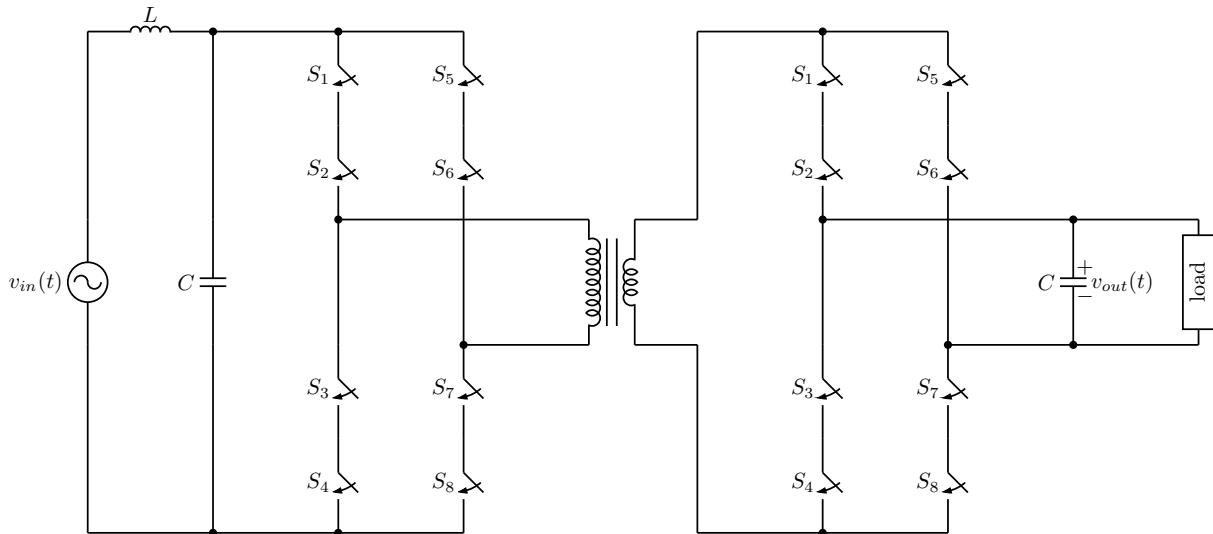


Figure 2.2: Alternative solid-state transformer topology.

implementation by [6] each cell consists of a back-to-back full-bridge converter, isolation transformer, passive rectifier and LC -low-pass filter. Other implementations made use of diode-clamped converters [3,30] and boost converters [4] to construct the cell.

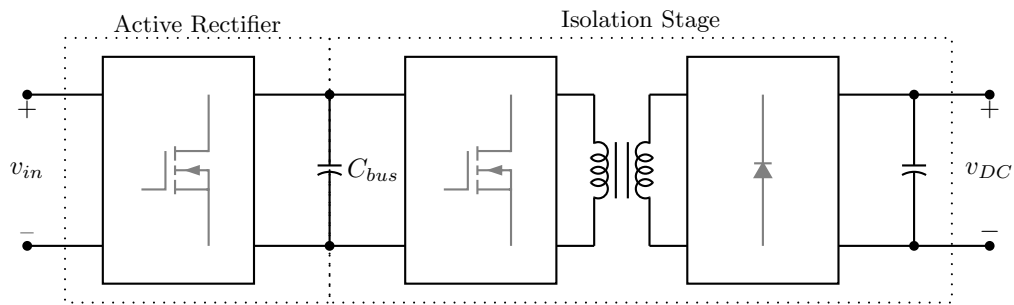
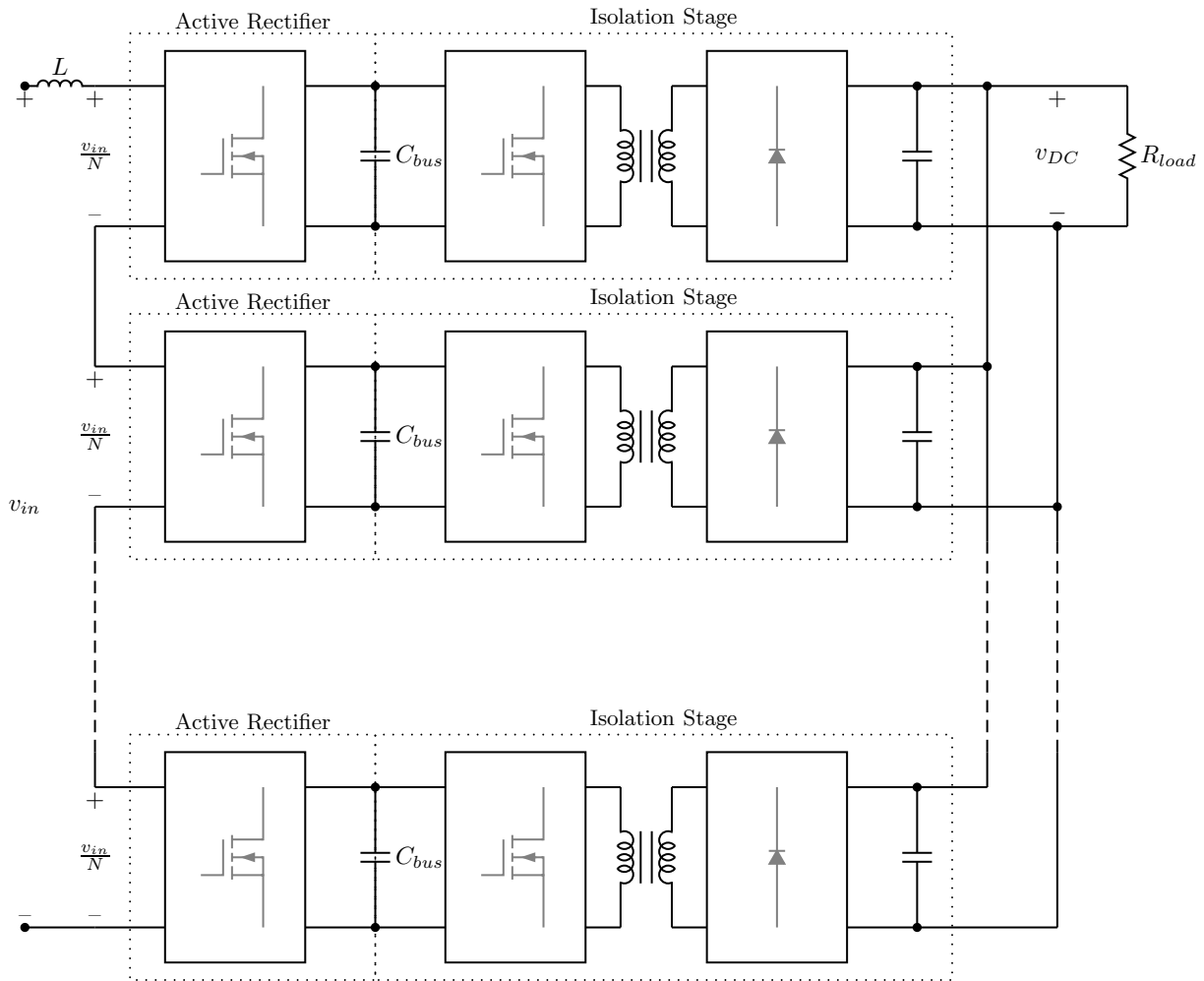


Figure 2.3: A single cell of a stacked converter.

The series-input, parallel-output converter topology is shown in Figure 2.4. The series input will let the input voltage divide between the cells in the stack. An input voltage larger than the blocking voltage of a single power switch can therefore be handled. The DC outputs are connected in parallel to produce a low voltage DC bus. This bus can be connected to an inverter to produce a line frequency, low voltage output for residential use.

The active rectifier front-end of the converter provides the user with control over the input power factor of the SST. The converter can operate at unity power factor or be applied for power factor correction when used in conjunction with conventional transformers. Furthermore, the bus capacitors of each cell provides energy storage capacity that can be utilised during times of input voltage dips in order to provide an uninterrupted output.

Figure 2.4: An N -cell stack topology.

2.2 Bus Voltage Balancing

The use of a series-input, parallel-output converter has the challenge that the bus voltages of all the cells need to be balanced in steady-state. The authors of [7] proved that a two cell, series-input, parallel-output converter with synchronous rectifiers has a natural balancing mechanism. This proof was extended to a 12-cell converter with passive rectifiers in [33]. Series-input, parallel-output converters exhibits two types of natural balancing: a weak and strong mechanism.

The weak mechanism is first mentioned in [34–36] in the study of flying-capacitor converters. It depends on the use of an interleaved switching scheme where the same reference value is used for all the converters in the stack but their PWM carriers are phase shifted with respect to each other. Any unbalance in the bus voltages will result in an increased current ripple on the actively rectified input current. The unbalanced energy will be dissipated in this increased ripple and therefore attempt to rebalance the bus voltages.

The addition of the isolation back-end to the active rectifier brings with it the strong

balancing mechanism. An unbalance in the bus voltages will be opposed by the fact that a higher bus voltage will deliver more power across the isolation barrier. If more power is delivered the bus voltage will tend to decrease. It is therefore important that all isolation stages be switched at equal effective duty cycles. A larger duty cycle also has the effect of delivering more power across the isolation barrier and will thus let its bus voltage decrease below the nominal.

The sensitivity to component mismatches is also described in [33]. Unequal transformer turn ratios between cells will let unequal amounts of power across the various isolation barriers. The leakage inductance of the transformer has the effect of reducing the effective duty cycle of the isolation stage converter. A mismatch in the leakage inductances will again let unequal amounts of power across the various isolation barriers. The leakage inductance mismatch will affect the voltage balancing the most at high power levels where the transformer currents are higher. With variations in the filter inductors of the passive rectifiers the cells will go into discontinuous conduction mode at different (DCM) times. DCM will only appear at small output currents and will therefore occur at low power levels.

2.3 Control

The author of [9] used a double loop control scheme to control the sinusoidal input current and bus voltages of a 12-cell series-input, parallel-output converter. The scheme is shown in Figure 2.5 where v_{bus} is the sum of the bus voltages. The control scheme's output u_I is the duty cycle command that will be compared to phase shifted carriers to obtain the switching signals for the power switches of the active rectifiers.

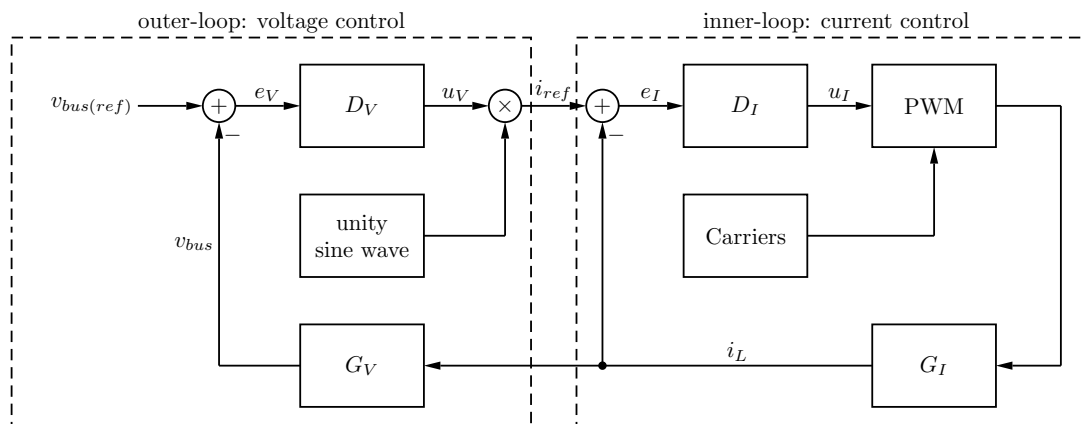


Figure 2.5: Double-loop active rectifier control block diagram.

The converter is divided into two plant transfer functions: G_I and G_V . G_I receives the switching signals and produces the input current for the active rectifier. G_V takes

this current as input and produces the bus voltage. The control scheme has two loop compensators, both of which are PI compensators. D_V is responsible for regulating the total bus voltage. Its output is multiplied with an unity sine wave which is in-phase with the input voltage. This gives the input current reference for which D_I is the compensator. D_I has a large gain integral component to have a fast current tracking response. D_V also has a integral component to ensure a zero steady-state tracking error but this is much slower than the inner current loop. The current loop can thus be designed and then considered as a current source to design the voltage compensator.

2.4 Summary

This chapter introduced the solid-state transformer concept and discussed various converter topologies associated with it. The series-input, parallel-output topology was highlighted and discussed further. The contents, and purpose thereof, of each cell in an n -stack SST as implemented by [6] were given. The natural voltage balancing mechanism present was also discussed. The importance of balanced bus voltages throughout the stack of series-input converters should be respected. In the event of a severe unbalance in the bus voltages the operating voltage of one or more cells could be exceeded. This could happen while the input voltage is still within the voltage limitation of the SST as a whole.

Fortunately, the balancing of the bus voltages occurs naturally and quite strongly. The use of series-input converters is therefore an effective way to increase the operating voltage of a converter beyond that of a single power switch. Furthermore, the parallel-output converters, as in Figure 2.4, has the advantage of providing the user with a low voltage DC bus that could be used for industrial applications.

Chapter 3

Diode-Clamped Converter

The diode-clamped converter was developed in the late 1970s and early 1980s [13,37]. It was developed to reduce the harmonic content in the outputs of motor drives as PWM techniques have their limitations when trying to reduce harmonic content [38,39]. The new converter was able to eliminate the fifth and seventh harmonics of the output voltage. Another advantage of the new converter type is the fact that the voltage stresses on the power switches are only half that of conventional converters. The number of power switches in the converter is, however, double that of a conventional full-bridge converter.

After the publications of [13,37] variations of the diode-clamped concept was proposed to further increase the voltage handling capability of the converter. These include expanding the three-level converter to an arbitrary number of levels as in [12] and some modifications to the layout of the converter such as proposed by [40]. The authors of [40] proposed a solution to the different blocking voltages need for the clamping diodes. A simple solution is to tie the appropriate amount of diodes in series. The large RC snubbers required to ensure even voltage division between the series diodes lead to an expensive and large system. They proposed a new *pyramid* structure for the clamping diodes where all diodes have the same voltage rating and no diodes are connected in series.

This chapter gives the basic layout for a full-bridge, three-level, diode-clamped active rectifier. The switching states for the possible output voltages are given and the clamping mechanism for the power switches is discussed. Next, the importance and methods of voltage balancing of the bus capacitors are discussed and simulation results are presented to show the inability of PWM to control a full-bridge, three-level, diode-clamped converter as an active rectifier front-end.

3.1 Converter Layout

An m -level converter consists of $(m - 1)$ DC bus capacitors which provides the converter with m levels of DC voltages [12]. Figure 3.1 shows two phase-legs of a three-level converter. A five-level converter will consist of four DC bus capacitors and eight switches in each leg instead of four.

Although the use of multilevel converters requires quite a large number of active devices it has the following advantages [18]:

1. lower input current harmonics
2. bidirectional power flow
3. ability to control the DC bus voltage
4. ability to control input power factor

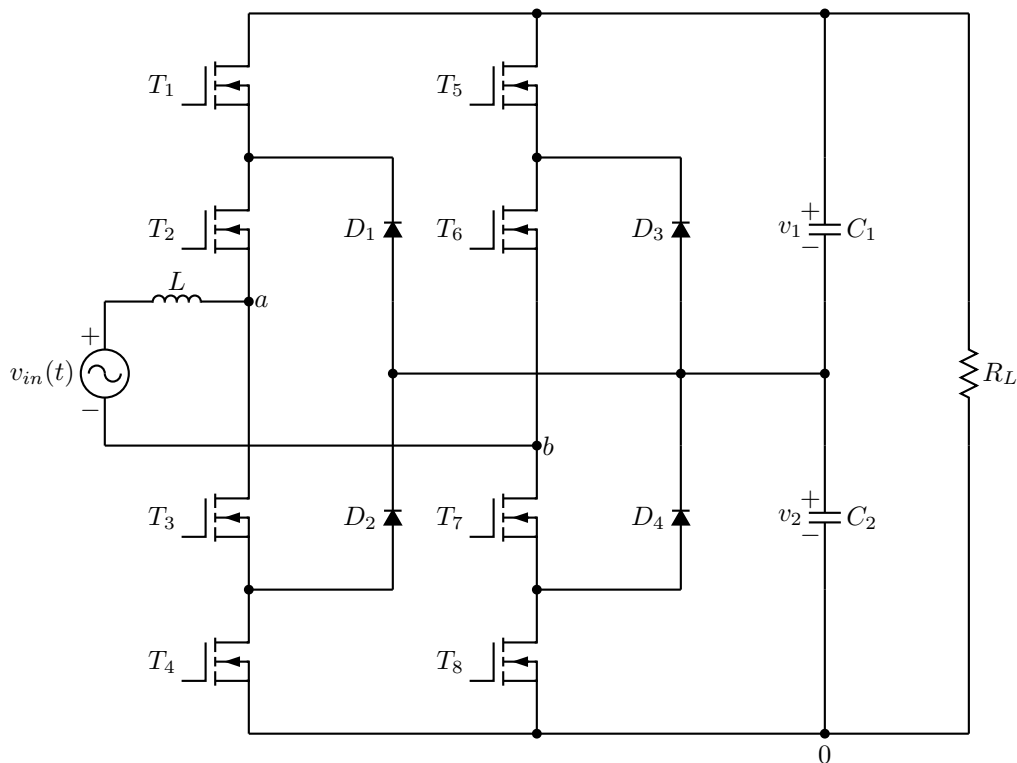


Figure 3.1: A full-bridge, three-level, diode-clamped active rectifier

3.2 Basic Operation

3.2.1 Voltage Synthesizing

From its name it is clear that the three-level converter can produce three different voltage levels. An m -level converter can produce m different voltage levels [12].

Taking the full-bridge, three-level converter in Figure 3.1 the synthesizing of the terminal voltage of the active rectifier can be explained. Firstly, it should be noted that the switches operate in complementary pairs. This means that if switch T_1 is on, T_3 will be off; with T_2 on, T_4 will be off. Taking the voltage between points a and the negative DC rail, 0, three different voltages can be produced:

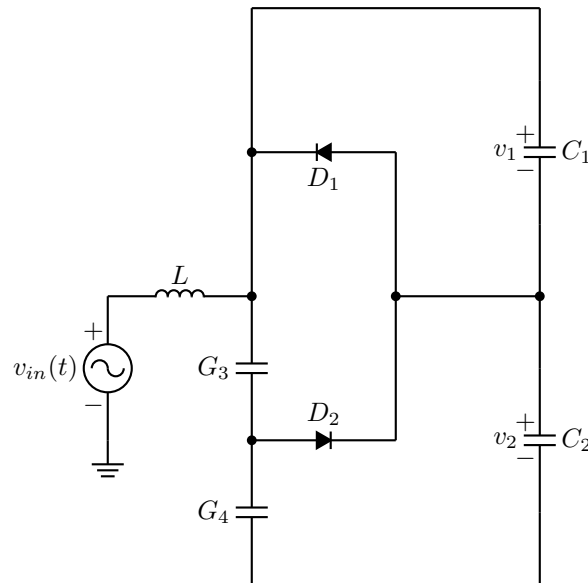
1. $v_{a0} = v_{bus} \rightarrow$ turn on T_1 and T_2
2. $v_{a0} = \frac{1}{2}v_{bus} \rightarrow$ turn on T_2 and T_3
3. $v_{a0} = 0 \rightarrow$ turn on T_3 and T_4

where v_{bus} is equal to the sum of v_1 and v_2 . The same three voltages for v_{b0} are possible. The terminal voltage possibilities v_{ab} of the converter are $v_{a0} - v_{b0}$ for all the combinations of v_{a0} and v_{b0} . When using a full-bridge, three-level converter such as in Figure 3.1, five voltage levels between points a and b can therefore be produced. By using a full-bridge it also means that the complete series string of bus capacitors have to be able to handle the peak input voltage.

3.2.2 Clamping Mechanism

The series connected switches of the converter enables it to be a multilevel converter. It also enhances the voltage handling capability of the converter, because the total supply voltage is divided equally between the switches. Because each switch requires a lower blocking voltage rating, cheaper switches can be used. Lower voltage switches usually also have better characteristics. When a single switch cannot handle the total voltage applied to the whole series string it is important to ensure that the total voltage is divided equally between all the switches. The diode-clamped converter has a built-in clamping mechanism for switches in the off-state.

Suppose that switches T_1 and T_2 are switched on. Switches T_3 and T_4 will therefore be turned off. The equivalent circuit of the phase leg is shown in Figure 3.2. Switches T_1 and T_2 are short circuits and T_3 and T_4 are represented by their output capacitances, G_3 and G_4 respectively.

Figure 3.2: Equivalent circuit of phase leg when T_1 and T_2 are on

Although most of the supply current will flow through the turned-on switches into the DC bus, some current will flow through the turned-off capacitances of the switches. This current will charge up the capacitances until their voltages equals the input voltage. However, when G_4 is charged up to a voltage higher than C_2 , D_1 will become forward biased. Because C_2 is much larger than G_4 , the voltage over G_4 will be clamped by C_2 . Therefore, the voltage across G_4 will be kept at $\frac{1}{2}v_{bus}$ by the constant charging and clamping of G_4 's capacitance.

G_3 is involved in a similar process. Because G_4 is kept at $\frac{1}{2}v_{bus}$, G_3 will only be able to charge up to v_{bus} before C_1 and C_2 will clamp its voltage.

3.3 Voltage Balancing

It has been proved that the three-level converter has the ability to naturally balance the voltages across the two DC bus capacitors [18]. However, it does still have a low frequency ripple at the centre point of the two bus capacitor, but [41–44] have addressed this problem. The natural balancing of the voltage makes the three-level converter very attractive with respect to higher level converters.

For converters with levels greater than three, the bus capacitors tend to either overcharge or discharge completely. These higher level converters then converge to a three-level converter for odd m or towards a two-level converter for even m .

Figure 3.3 shows the sinusoidal input current and synthesized stepped voltage of a half-bridge bridge, five-level converter [16]. Figure 3.3(a) shows that when the input current and voltage are in-phase, each level of the DC bus are not charged and discharge an

equal amount. This results in some levels overcharging and others discharging. However, when the current and voltage are 90° out of phase, such as in Figure 3.3(b), each level is charged and discharged by equal amounts. This will leave the different voltage levels with a constant voltage and thus the DC bus has balanced voltages. The problem with the 90° phase shift is that only reactive power can be absorbed or delivered. The higher level converters are therefore good solutions to static var compensators, but cannot deliver real power to a load without unbalancing the bus capacitor voltages.

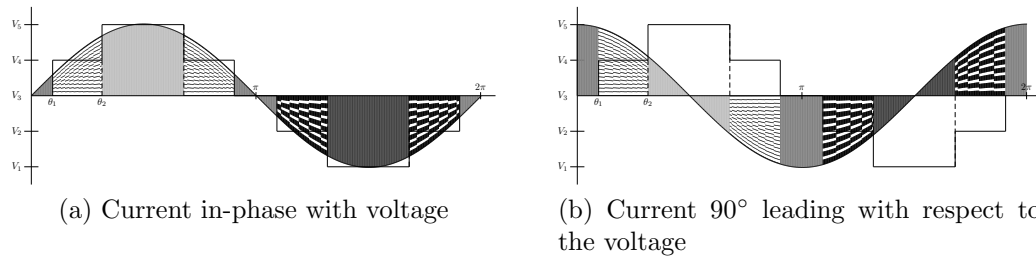


Figure 3.3: Currents flowing into capacitor junctions.

Different methods to balance the bus voltages have been developed, some of which are [18,19,45,46]. A simple, although expensive, solution to the voltage unbalance problem is to use a back-to-back topology and then control the switching angles of the rectifier and inverter independently [16]. This method relies on the fact that the rectifier and inverter in the symmetrical back-to-back converter compensates for each other's effect on the bus voltages. Where the rectifier tend to overcharge a specific voltage level the inverter will tend to discharge that level. By controlling the switching angles at which the input and output voltage levels are changed, the net charging/discharging for each voltage level can be controlled to be zero. The angles θ_1 and θ_2 in Figure 3.3 are the switching angles. Both the rectifier and inverter have these angles and can be controlled.

Another control scheme is a sinusoidal PWM method [18].

3.4 Simulations

The full-bridge, three-level active rectifier in Figure 3.1 was simulated with PWM control. Two different carriers were used [47]. The phase disposition (PD) carrier, Figure 3.4(a), uses two triangular waves per phase-leg, one for each switching pair in the leg. The modified alternative phase opposition disposition (APOD), Figure 3.4(b), uses four triangular waves in total to determine which of the four available switching states should be used.

If a sinusoidal reference is to be compared to the PWM carriers a stepped voltage will be obtained. For the converter shown in Figure 3.1 this voltage will have five steps: v_{bus} ,

$\frac{1}{2}v_{bus}$, 0 , $-\frac{1}{2}v_{bus}$ and $-v_{bus}$. This is due to the fact that a full-bridge, three-level converter is used. Each phase-leg can only produce three voltage levels, but the combination of the two legs can produce five.

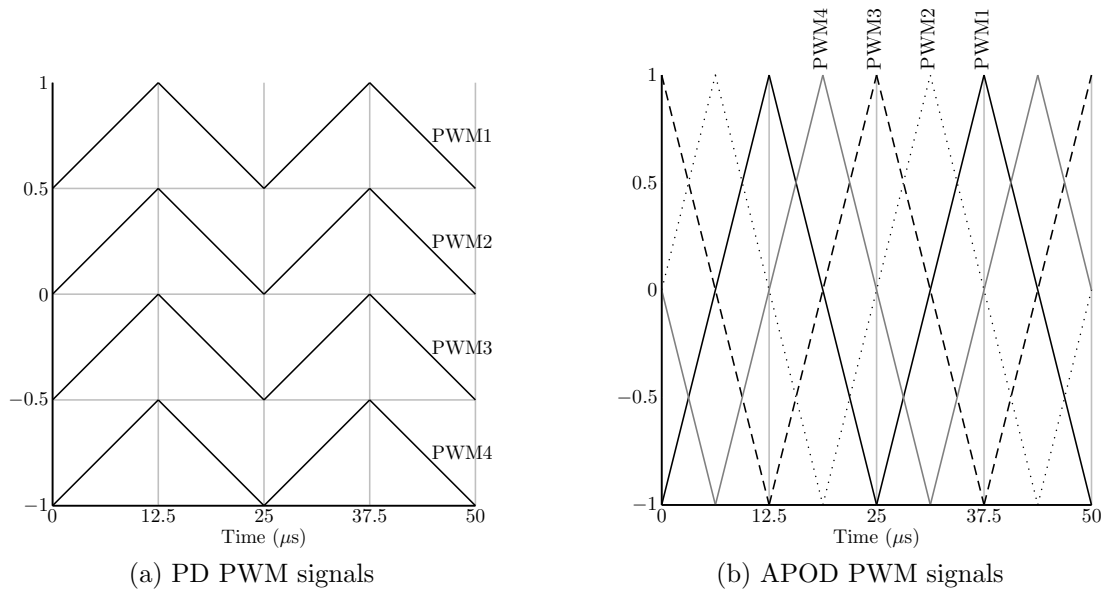


Figure 3.4: Phase disposition and alternative phase opposition disposition PWM carrier waves.

The simulation parameters are listed in Table 3.1. Figure 3.5 shows the double-loop control circuit used to control the rectifier. The inner-loop controls the input current to be sinusoidal and in-phase with the input voltage. The outer-loop adjusts the amplitude of the reference current to regulate the DC bus voltage.

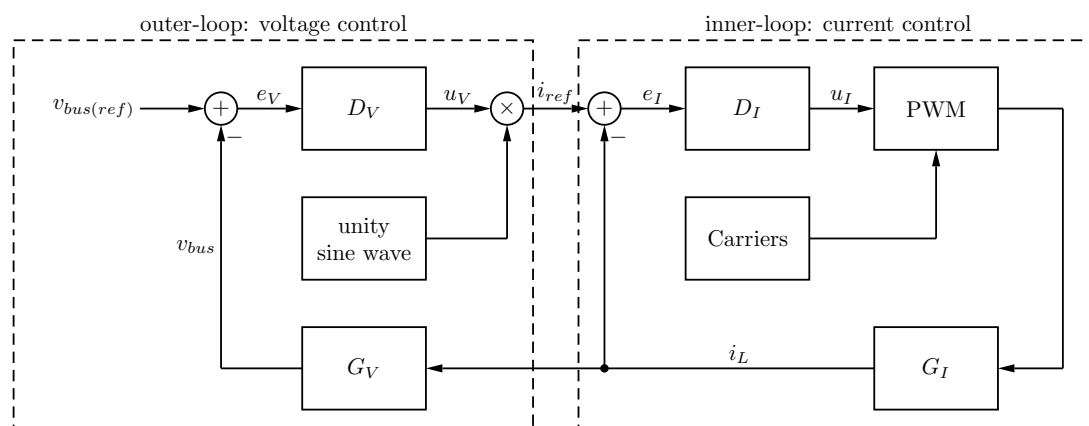


Figure 3.5: Control circuit used in simulation

Table 3.1: Diode-clamped converter simulation parameters

Parameter	Value	Description
R	360Ω	load resistor
L	15 mH	boost inductor
C	$300 \mu\text{F}$	all capacitors
v_{in}	500 V_{peak} at 50 Hz	input voltage
v_{bus}	600 V	nominal bus voltage
v_1 and v_2	300 V	nominal capacitor voltage
f_s	40 kHz	switching frequency

3.4.1 PD PWM Scheme

The duty cycle output of D_I in Figure 3.5 was compared to the carriers in Figure 3.4(a) through the algorithm in Algorithm 3.1 to produce the switching signals for the eight power switches.

Algorithm 3.1 Phase Disposition PWM Control Algorithm

$T_1 = \text{on if PWM1} > \text{duty cycle}$

$T_2 = \text{on if PWM2} > \text{duty cycle}$

$T_5 = \text{on if PWM3} < \text{duty cycle}$

$T_6 = \text{on if PWM4} < \text{duty cycle}$

$T_3 = \text{not } T_1$

$T_4 = \text{not } T_2$

$T_7 = \text{not } T_5$

$T_8 = \text{not } T_6$

The PD PWM switching scheme was able to control the input current to be sinusoidal, as well as keeping the capacitor voltages balanced. The input current is shown in Figure 3.6(a) and the capacitor voltages in Figure 3.6(b). At time 100 ms a 100Ω resistor was switched in across C_1 for 20 ms. The controller was not able to rebalance the voltages after the disturbance was applied. The controller is therefore not suitable to control a full-bridge, three-level diode-clamped converter as an active rectifier.

3.4.2 APOD PWM Scheme

Similar to Section 3.4.1 a simulation of the circuit in Figure 3.1 was done using the APOD carriers in Figure 3.4(b). The algorithm to generate the switching signals from the sinusoidal reference and the four carrier waves is shown in Algorithm 3.2.

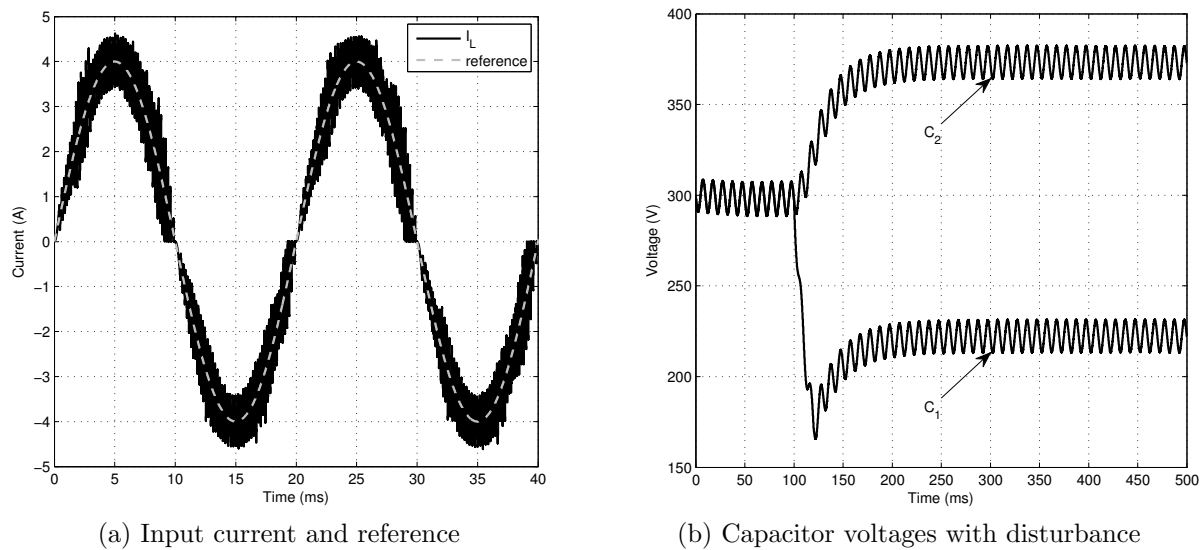


Figure 3.6: PD PWM control for full-bridge, three-level, diode-clamped active rectifier.

Algorithm 3.2 Alternative Phase Opposition Disposition PWM Control Algorithm

 $T_1 = \text{on if PWM1} > \text{duty cycle}$
 $T_2 = \text{on if PWM2} > \text{duty cycle}$
 $T_8 = \text{on if PWM3} > \text{duty cycle}$
 $T_7 = \text{on if PWM4} > \text{duty cycle}$
 $T_3 = \text{not } T_1$
 $T_4 = \text{not } T_2$
 $T_7 = \text{not } T_5$
 $T_8 = \text{not } T_6$

The same disturbance as in Section 3.4.1 was applied to obtain the results shown in Figure 3.7. Although the ripple on the input current is smaller, the controller still cannot rebalance the voltages after the disturbance is removed.

The reason the ripple is smaller than that of the PD PWM scheme is because of the two voltage waveforms in Figure 3.8. The PD PWM scheme does not utilise all five possible voltage levels that the converter can produce. APOD, however, does utilise all five: 600 V, 300 V, 0 V, -300 V and -600 V which corresponds to v_{bus} , $\frac{1}{2}v_{bus}$, 0, $-\frac{1}{2}v_{bus}$ and $-v_{bus}$.

The change in current through an inductor with respect to the applied voltage across the inductor is $v = L \frac{\Delta i}{\Delta t}$. For the PD PWM scheme the applied voltage across the input inductor is double that of the APOD PWM scheme, because it utilises only three of the five voltage levels. Because the switching frequency of both simulations were equal, their Δt terms are equal. The Δi for the PD PWM scheme will therefore be double that of the APOD PWM which is why its input current ripple is larger.

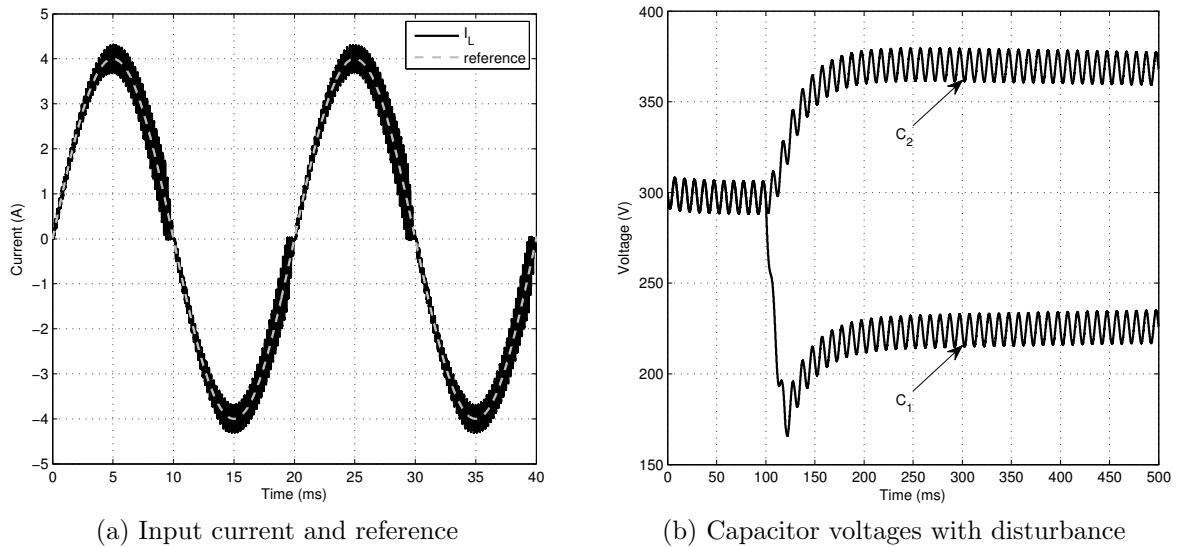


Figure 3.7: APOD PWM control for full-bridge, three-level, diode-clamped active rectifier.

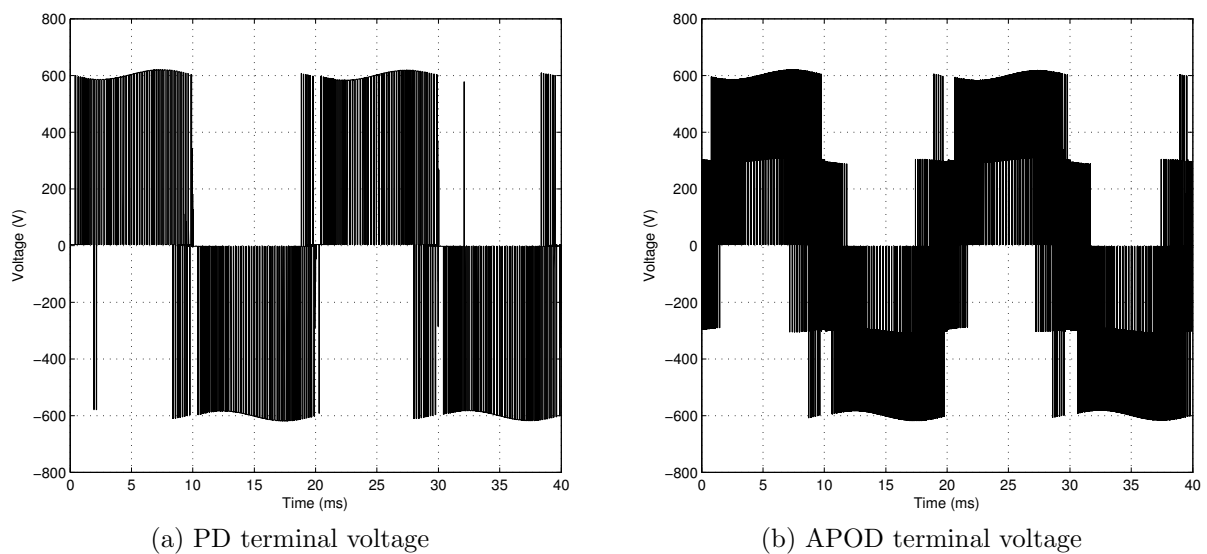


Figure 3.8: The terminal voltages of the PD and APOD PWM schemes for the full-bridge, three-level, diode-clamped active rectifier.

3.5 Summary

This chapter introduced the diode-clamped multilevel converter. Its operating and voltage clamping principles were discussed and the problems with balancing the bus capacitor voltages were highlighted. Simulations were used to show the inability of PWM control to regulate these capacitor voltages for a full-bridge, three-level converter operating as an active rectifier. Although the alternative phase opposition disposition PWM controller produced a sinusoidal input current with a much smaller ripple than the phase disposition PWM controller, neither could re-balance the capacitor voltages after the dis-

turbance. One solution to this is to use the back-to-back topology suggested in [16] or others mentioned in Section 3.3. The back-to-back topology is disadvantageous in terms of the large number of active devices that are needed which will increase costs. To be able to only use the single ended converter, such as in Figure 3.1, a controller that is more sophisticated than PWM with a PID compensator is needed.

Chapter 4

Flying-Capacitor Converter

The flying-capacitor converter was proposed by Meynard and Foch to be an alternative to the diode-clamped converter [48]. The flying-capacitor converter shares the advantages that multilevel converters have, similar to the diode-clamped converter. For the same number of voltage levels a flying-capacitor converter will have the same number of power switches as a diode-clamped converter. The main difference between the flying-capacitor and diode-clamped converters is the clamping mechanisms that are used. Where the diode-clamped converter has clamping diodes the flying-capacitor converter has clamping (flying) capacitors. Both converters have a series string of switches that the clamping mechanism has to protect by dividing the supply voltage equally among the different switches in their off-states. The voltages of the flying capacitors therefore needs to be controlled to certain values. Control schemes which are used to balance these flying capacitor voltages are well researched. The flying capacitors do present some form of natural balancing under certain conditions [49]. To actively balance the voltages the authors of [50] used a phase shifted sinusoidal pulse-width modulation (SPWM) scheme where a small square wave is added to the sinusoidal reference. The square wave is controlled to regulate the flying capacitor voltages in a five-level converter. By adding two- and three-level comparators to the SPWM technique the authors of [17] were able to make a selection between the switching states which will have the preferred effect, either charging or discharging, on the flying capacitors. This is achieved by utilising the redundant switching states of the converter. There will be more than one possible switching state to output a specific voltage where each switching state will charge/discharge different sets of flying capacitors. By choosing the correct switching state the voltages of the flying capacitors can be controlled.

This chapter gives the basic layout for a full-bridge, three-level, flying-capacitor active rectifier. The switching states for the possible output voltages are given and the clamping mechanism for the power switches is discussed. Next, the importance and methods of volt-

age balancing of the flying capacitors are discussed and simulation results are presented to show the inability of PWM to control a full-bridge, three-level, flying-capacitor converter as an active rectifier front-end. A simulation with a look-up table-based controller that utilises all the redundant switching states is also shown.

4.1 Converter Layout

Assuming that the voltage rating of the capacitors in a flying-capacitor converter is $\frac{v_{bus}}{m-1}$, an m -level flying-capacitor converter will consist of $(m-1)$ DC bus capacitors and $\frac{(m-1)(m-2)}{2}$ flying-capacitors for each phase-leg [12]. Figure 4.1 shows a single phase, full-bridge, three-level converter. The full-bridge converter consists of two phase-legs and thus requires $(m-1)(m-2)$ flying-capacitors. The flying capacitors are charged up to half the DC bus voltage. A five-level converter's capacitors will be charged up to $\frac{1}{4}v_{bus}$, $\frac{1}{2}v_{bus}$ and $\frac{3}{4}v_{bus}$, alternatively.

The converter has, in addition to those mentioned in Section 3.1, the following advantages:

1. The large amount of capacitors used provides extra ride through during power dips
2. Redundant switch combinations makes the balancing of the capacitor voltages easier

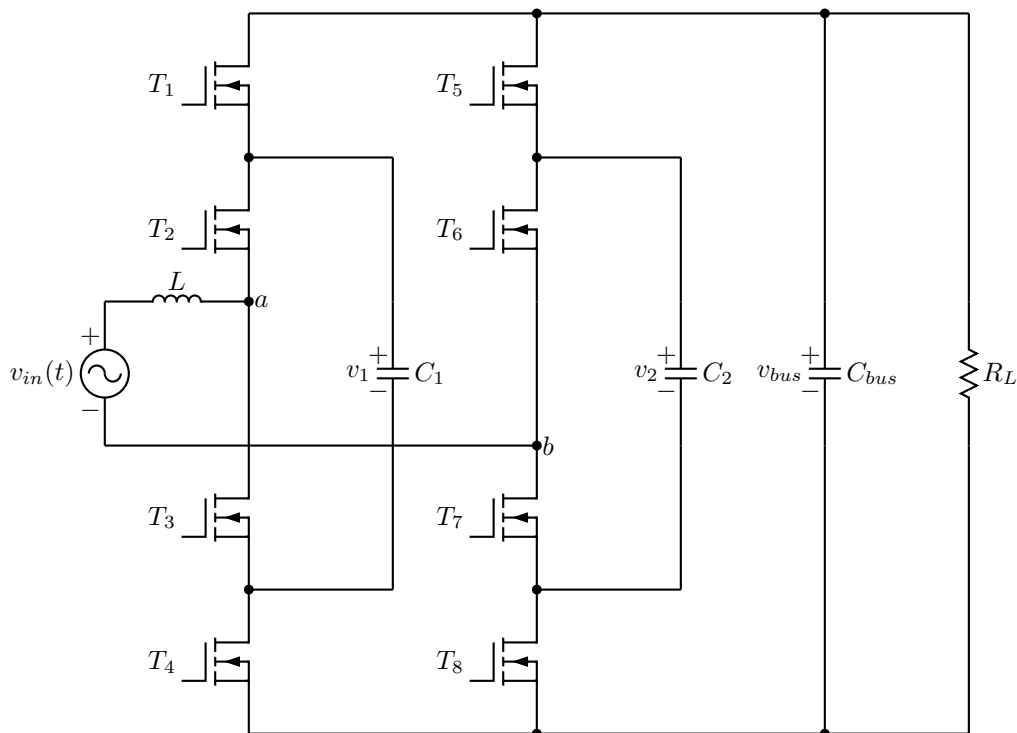


Figure 4.1: A full-bridge, three-level, flying-capacitor converter

4.2 Basic Operation

4.2.1 Voltage Synthesizing

From Figure 4.1 the synthesizing of the converter's terminal voltage can be explained. Similar to the diode-clamped converter, the switches operate in complimentary pairs. Taking leg-A, switches T_1 and T_4 should not be turned on together as this will short circuit the bus capacitors and the flying capacitor. Switches T_2 and T_3 also form a complimentary pair.

The full-bridge, three-level converter, similar to the diode-clamped converter, is also capable of producing five different voltage levels. Taking the voltage between points a and b the following five voltages can be produced, with v_{bus} , v_1 and v_2 as defined in Figure 4.1:

1. $v_{ab} = v_{bus} \rightarrow$ turn on T_1, T_2, T_7, T_8
2. $v_{ab} = \frac{1}{2}v_{bus} \rightarrow$ four possibilities:
 - a) turn on $T_2, T_4, T_7, T_8 (+v_1)$
 - b) turn on $T_1, T_2, T_5, T_7 (+v_2)$
 - c) turn on $T_1, T_3, T_7, T_8 (v_{bus} - v_1)$
 - d) turn on $T_1, T_2, T_6, T_8 (v_{bus} - v_2)$
3. $v_{ab} = 0 \rightarrow$ six possibilities:
 - a) turn on T_1, T_2, T_5, T_6
 - b) turn on T_3, T_4, T_7, T_8
 - c) turn on $T_2, T_4, T_6, T_8 (v_1 - v_2)$
 - d) turn on $T_1, T_3, T_5, T_7 (v_2 - v_1)$
 - e) turn on $T_2, T_4, T_5, T_7 (v_{bus} - v_1 - v_2)$
 - f) turn on $T_1, T_3, T_6, T_8 (v_1 + v_2 - v_{bus})$
4. $v_{ab} = -\frac{1}{2}v_{bus} \rightarrow$ four possibilities:
 - a) turn on $T_1, T_3, T_5, T_6 (-v_1)$
 - b) turn on $T_3, T_4, T_6, T_8 (-v_2)$
 - c) turn on $T_2, T_4, T_5, T_6 (v_1 - v_{bus})$
 - d) turn on $T_3, T_4, T_5, T_7 (v_2 - v_{bus})$
5. $v_{ab} = -v_{bus} \rightarrow$ turn on T_3, T_4, T_5, T_6

Note the number of redundant switching states for each voltage level. For $v_{ab} = \frac{1}{2}v_{bus}$ and $v_{ab} = -\frac{1}{2}v_{bus}$ there are four switching states to produce the same output voltage. Any one of six switching states can be utilised to produce zero volt.

4.2.2 Clamping Mechanism

Suppose the input voltage is at its maximum positive value and switches T_1 and T_2 of leg-A are switched on. Switches T_3 and T_4 need to block the input voltage and the voltage across the two switches has to divide equally. Switches T_1 and T_2 can be represented as short circuits, while switches T_3 and T_4 can be represented by their output capacitances, G_3 and G_4 . The equivalent circuit of leg-A is shown in Figure 4.2.

The input current will primarily flow through the short circuited switches, but some amount of current will flow through the off switches' output capacitances. This current will charge up the capacitors. G_4 will only be able to charge up to $(v_{bus} - v_1)$ which is equal to $\frac{1}{2}v_{bus}$. G_3 will, if G_4 has $\frac{1}{2}v_{bus}$ across it, also only be able to charge up to $\frac{1}{2}v_{bus}$. The off switches will therefore share the total bus voltage equally.

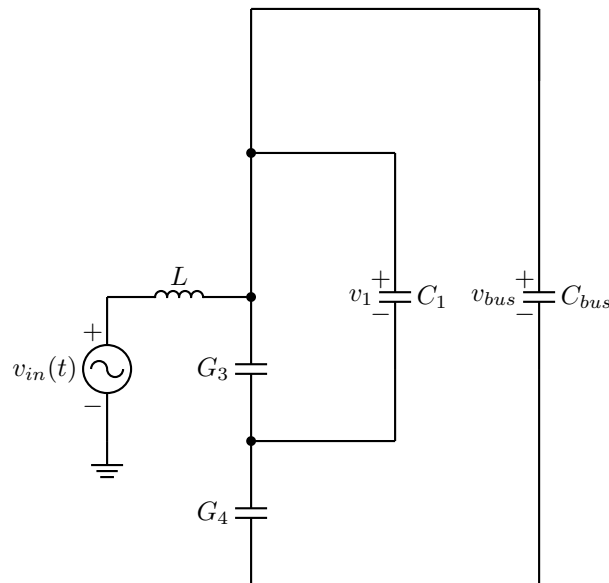


Figure 4.2: Equivalent circuit of phase leg when T_1 and T_2 are on

4.3 Voltage Balancing

The structure of the flying-capacitor converter does not require a split DC bus voltage such as the diode-clamped converter does. Therefore, there are no junction currents between the bus capacitors that will unbalance their voltages. It is, however, very important that, for the three-level converter, the voltages across the flying-capacitors be half the bus

voltage. Different level converters will have different amounts of flying-capacitors, each with a different voltage. If these voltage were to be unbalanced the clamping mechanism will not function correctly and the danger of exposing some switches to over voltages arises. Referring to Section 4.2.1 it can be seen that some of the voltage levels that can be produced can be done by more than one switching state. The full-bridge, three-level converter, for example, can produce 0 V in six different ways. The switching scheme used to operate the converter can therefore utilise the switching state redundancy to balance the flying-capacitors.

One such way to choose between the redundant switching states is implemented by [17]. Their control scheme is shown in Figure 4.3. The desired PWM scheme is input at the *carrier* and the output reference, for example a sinusoidal wave, is input at *reference*. For each flying capacitor a reference exists from which the measured voltage is subtracted. The comparators determine whether the voltage of the flying capacitor should either be increased or decreased. The *control law* receives the switching state input from the *reference* and *carrier* comparison and uses the flying capacitor voltage comparisons to choose out of the appropriate redundant switching states. The corresponding switching signals are then produced by the *gating circuit*.

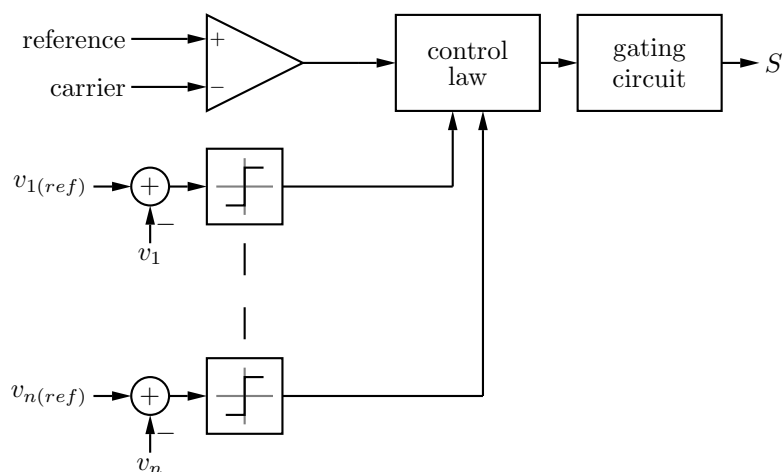


Figure 4.3: Control strategy for voltage balancing of flying capacitor voltages.

An alternative to the PWM scheme is to use a hysteresis-based control scheme [51]. The controller will select out of the n possible voltage levels the inverter can produce in order to attempt to force the output current error to zero. When the current error exceeds the defined hysteresis limit, the next higher (or lower) voltage level should be selected. When selecting the new switching state the redundant switching states are again used to balance the flying capacitor voltages. A look-up table is implemented that pairs each voltage level with its switching states and influences on each flying capacitor. When the

new required voltage level is known, as well as the required effect of the different flying capacitors, the corresponding switching state is selected from the table.

4.4 Simulations

The simulation circuit for the converter is shown in Figure 4.1 with the simulation parameters listed in Table 4.1. The converter is simulated to operate as an active rectifier controlling the input current to be sinusoidal and in-phase with the input voltage. The disturbance used in Sections 4.4.2 and 4.4.3 was achieved by short circuiting capacitor C_2 through a $100\ \Omega$ resistor for 20 ms. The full-bridge, three-level converter as an active rectifier was simulated with two different control techniques.

Table 4.1: Flying-capacitor converter simulation parameters

Parameter	Value	Description
R	$360\ \Omega$	load resistor
L	15 mH	boost inductor
C	$300\ \mu\text{F}$	all capacitors
v_{in}	$500\ \text{V}_{peak}$ at 50 Hz	input voltage
v_{bus}	600 V	nominal bus voltage
v_1 and v_2	300 V	nominal flying-capacitor voltage
f_s	40 kHz	switching frequency

4.4.1 Pre-charging of Capacitors

The clamping mechanism is dependant on balanced capacitor voltages. It is therefore necessary to pre-charge all the capacitor before normal operation of the converter can begin. The authors of [52] proposed a method for pre-charging the capacitors. Taking the full-bridge, three-level converter in Figure 4.1 as an example the method can be explained. Turning on switches T_1 , T_4 , T_5 and T_8 all the capacitors in the converter will be connected in parallel. Note that these switching combinations are illegal for normal operation as this will short circuit the capacitors. Taking capacitor C_1 , if its voltage reaches a value close to its nominal value, switches T_1 and T_4 are switched off and the capacitor starts floating. This is also done for capacitor C_2 . With the flying-capacitors floating the bus capacitors are still allowed to be charged up. When the bus capacitors have reached a voltage close to their nominal voltage, the controller for normal operation of the converter is activated. The controller will let all the capacitors balance at their nominal voltages.

The simulation results of the pre-charging of a full-bridge, three-level converter is shown in Figure 4.4. During the pre-charging cycle the input inductor was disconnected and replaced with a $10\ \Omega$ resistor. The flying-capacitors were charged up to 225 V before letting them float. The nominal voltage for these capacitors was 300 V. The bus was charged up to 450 V before letting the controller for normal operation take over. Although the nominal voltage for the DC bus is 600 V, the pre-charging cannot let it reach a value larger than 500 V. The amplitude of the input voltage is 500 V and to reach the required 600 V the inductor is needed to operate the converter as a boost converter.

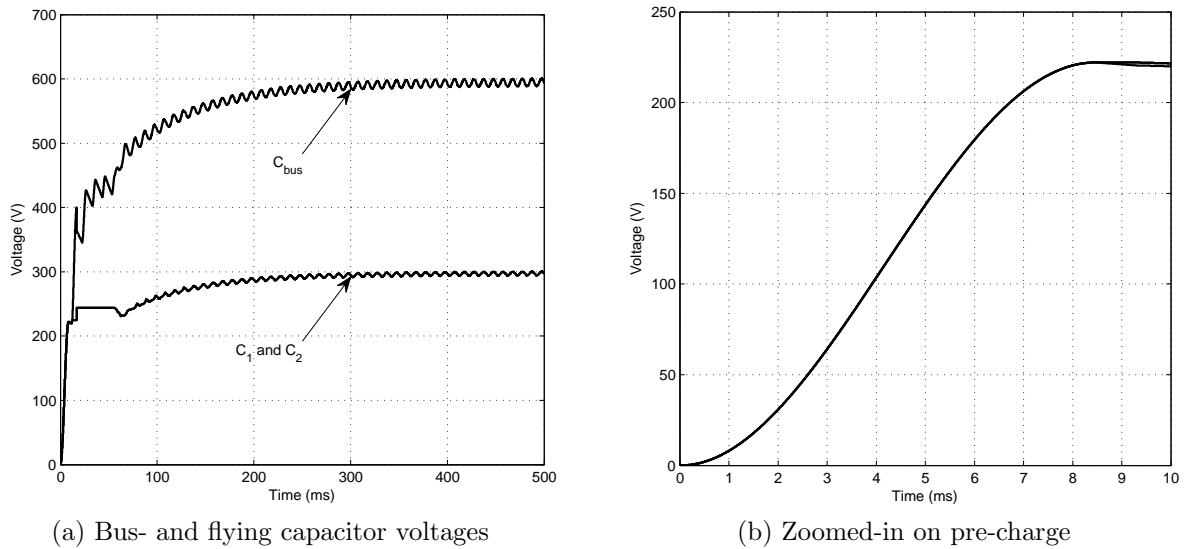


Figure 4.4: Pre-charging of capacitors.

The pre-charging was capable of letting all the capacitors charge up together as can be seen from the zoomed-in plot. The controller used for normal converter operation could then balance the voltages further without the risk of over voltages on any components.

Another method of pre-charging the flying capacitor(s) is to add pre-charge resistors R_{PC} in series with the DC power supply [53] as shown in Figure 4.5. The DC bus capacitors will charge up with a time constant of $T_{PC} = R_{PC}C_{DC}$. A natural balancing PWM strategy is used during the pre-charging. After the pre-charging is complete switches S_{PC} can be closed to resume normal operation. As shown, this solution is only implementable for converters operating as inverters from a given DC supply. The concept was also extended for odd-level converters [54].

The disadvantage of this pre-charging method is the addition of the pre-charging resistors and switches. The resistors do not have to be capable of dissipating large amounts of energy during pre-charging, because the load current is essentially controlled to be zero.

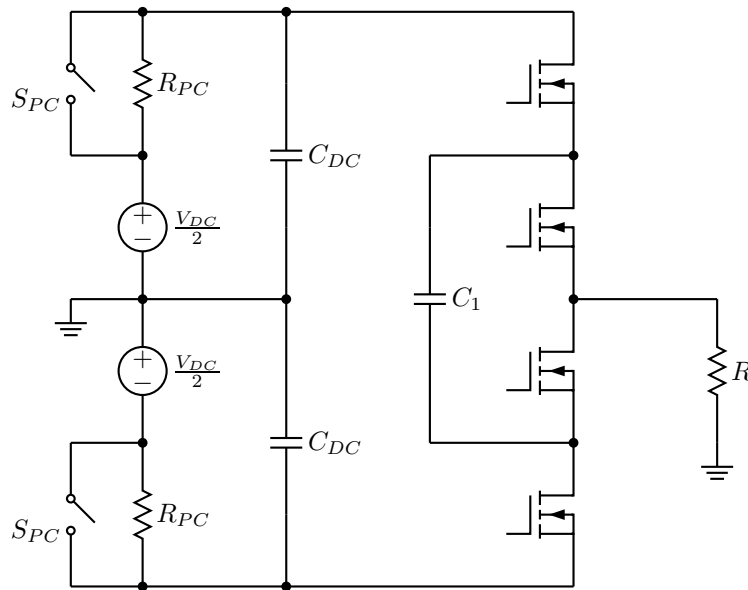


Figure 4.5: Pre-charging circuit for flying-capacitor inverter.

The switches, however, should be able to carry the full load current during normal operating conditions. The scheme can also not be used for active rectifier operation. The pre-charging scheme mentioned earlier does not need any additional components, except maybe for one current limiting resistor and bypass switch at the AC input. This is half the number of extra components required by [53].

4.4.2 PWM Scheme

The authors of [14] compared three different PWM techniques. The carriers, as shown in Figure 4.6, are for a half-bridge, three-level converter. A full-bridge converter will have four carriers. The half-bridge, three-level converter has four possible terminal voltages:

1. P : positive voltage
2. N : negative voltage
3. O_1 : zero voltage, possibility 1
4. O_2 : zero voltage, possibility 2

Of the three different carriers, the saw-tooth carrier produced the best results for its relatively low complexity and thus it was used in the simulation. The PWM scheme used to control the full-bridge active rectifier uses four saw tooth waves with the same control circuit used for the diode-clamped converter. The input current was controlled to be sinusoidal and the capacitor voltages balanced. The input current and capacitor voltages are shown on Figure 4.7.

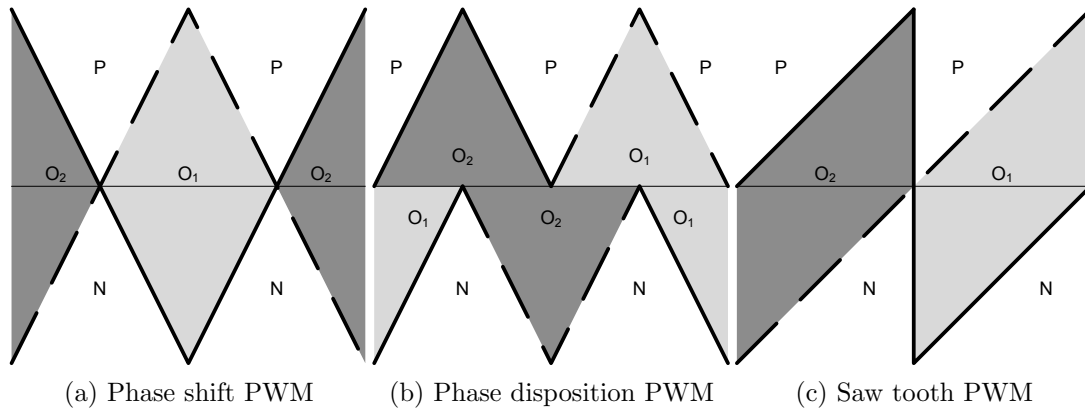


Figure 4.6: Different PWM carriers for a half-bridge, three-level, flying-capacitor converter

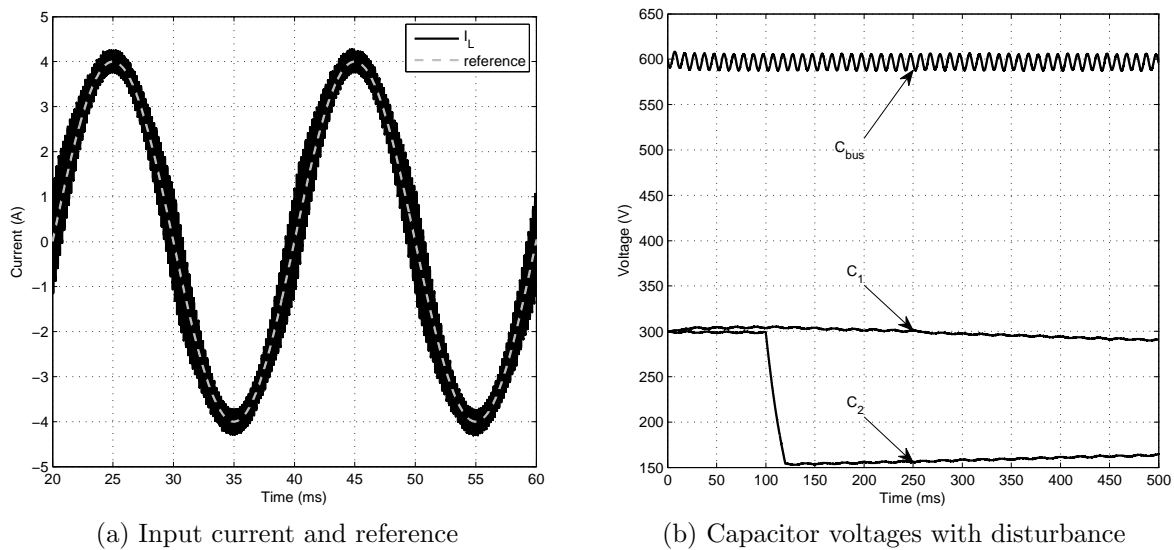


Figure 4.7: PWM control for full-bridge, three-level, flying-capacitor converter.

Capacitor C_2 was disturbed at 100 ms resulting in a voltage drop. The control scheme could compensate for this voltage unbalance through natural balancing. The simulation shows that the natural balancing mechanism of the capacitor voltage with a PWM controller is very weak. The capacitor voltages does show a natural tendency to be equal but the response is very slow.

4.4.3 Look-up Table

The authors of [55] proposed a look-up table control scheme that utilises all the redundant switching states of the converter to actively balance all the capacitor voltages. Six states were employed to determine the correct next switching state of the switches. Table 4.2 shows the complete look-up table that was implemented using `if-else`-statements. The control signals Q_1 , Q_2 , Q_3 and Q_4 controls switches T_1 , T_2 , T_5 and T_6 , alternatively. The

other switches are the other half of the complementary pairs.

The six states are

$$\begin{aligned} x_1 &= 1, \text{ if } v_{in} > 0 \\ &= 0, \text{ if } v_{in} < 0 \end{aligned} \quad (4.4.1)$$

$$\begin{aligned} x_2 &= 1, \text{ if } |v_{in}| < \min(v_1, v_2, v_{bus}/2) \\ &= 0, \text{ if } |v_{in}| > \min(v_1, v_2, v_{bus}/2) \end{aligned} \quad (4.4.2)$$

$$\begin{aligned} x_3 &= 1, \text{ if } i_{ref} - i_L > h \\ &= 0, \text{ if } i_{ref} - i_L < -h \end{aligned} \quad (4.4.3)$$

$$\begin{aligned} x_4 &= 1, \text{ if } v_1 > v_2 \\ &= 0, \text{ if } v_1 < v_2 \end{aligned} \quad (4.4.4)$$

$$\begin{aligned} x_5 &= 1, \text{ if } v_2 > v_{bus}/2 \\ &= 0, \text{ if } v_2 < v_{bus}/2 \end{aligned} \quad (4.4.5)$$

$$\begin{aligned} x_6 &= 1, \text{ if } v_{bus}/2 > v_1 \\ &= 0, \text{ if } v_{bus}/2 < v_1 \end{aligned} \quad (4.4.6)$$

where

v_{in} the supply voltage

v_1 voltage of capacitor C_1

v_2 voltage of capacitor C_2

i_{ref} the reference current

h the allowed hysteresis band around i_{ref}

i_L the input current

v_{bus} the DC bus voltage.

State x_1 determines whether the the input voltage is in its positive or negative half cycle. The switching signals for positive and negative half cycle operation will be mirrors of each other. x_2 shows whether the input voltage is larger than the internal voltages. If it is larger, the input current can be increased while one of the internal voltages are increased. x_3 shows whether the input current should be increased or decreased while x_4 to x_6 shows which internal voltages should be either increased or decreased.

Considering that the look-up table is based on hysteresis control, the problem of a non-constant switching frequency arises. A sampling frequency of 80 kHz means that the switching state will change at a frequency of 80 kHz and the maximum frequency that any switch will operate at, will therefore be 40 kHz. The resulting input current is shown

Table 4.2: Look-up table for full-bridge, three-level, flying-capacitor input current control

x_1	x_2	x_3	x_4	x_5	x_6	Q_1	Q_2	Q_3	Q_4
1	1	1	0	1	1	0	1	0	1
			0	0	1	0	1	1	0
			1	0	1	0	1	1	0
			1	0	0	1	0	1	0
			0	1	0	1	0	0	1
			1	1	0	1	0	0	1
		0	0	1	1	0	1	0	0
			0	0	1	0	1	0	0
			1	0	1	1	1	1	0
			1	0	0	1	1	1	0
			0	1	0	1	1	0	1
			1	1	0	1	0	0	0
	0	1	0	1	1	0	1	0	0
			0	0	1	0	1	0	0
			1	0	1	1	1	1	0
			1	0	0	1	1	1	0
			0	1	0	1	1	0	1
			1	1	0	1	0	0	0
		0	x	x	x	1	1	0	0
0	1	0	0	1	1	1	0	1	0
			0	0	1	1	0	0	1
			1	0	1	1	0	0	1
			1	0	0	0	1	0	1
			0	1	0	0	1	1	0
			1	1	0	0	1	1	0
		1	0	1	1	1	0	1	1
			0	0	1	1	0	1	1
			1	0	1	0	0	0	1
			1	0	0	0	0	0	1
			0	1	0	0	0	1	0
			1	1	0	0	1	1	1
		0	0	1	1	1	0	1	1
			0	0	1	1	0	1	1
			1	0	1	0	0	0	1
			1	0	0	0	0	0	1
			0	1	0	0	0	1	0
			1	1	0	0	1	1	1
		0	0	1	1	1	0	1	1
			0	0	1	1	0	1	1
			1	0	1	0	0	0	1
			1	0	0	0	0	0	1
			0	1	0	0	0	1	0
			1	1	0	0	1	1	1
		1	x	x	x	0	0	1	1

in Figure 4.8(a). To assess the voltage balancing of the control technique the same disturbance as in Section 4.4.2 was introduced. The capacitor voltages are shown in Figure 4.8(b). The RMS value of the input current's ripple is 72% less than that of the PWM controller's input current. The capacitor voltages were rebalanced within 70 ms where the voltages of the PWM simulation have not rebalanced by the end of the simulation.

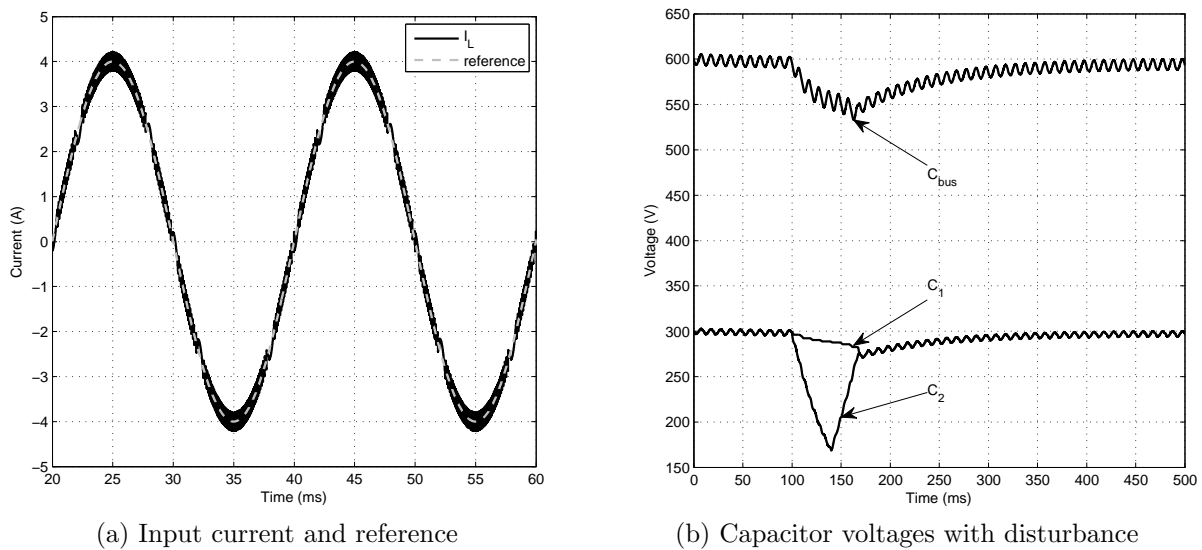


Figure 4.8: Look-up table control for full-bridge, three-level, flying-capacitor converter.

4.5 Summary

The flying-capacitor converter was introduced and its operation was described. Its clamping mechanism uses the balanced voltages of the flying capacitors to limit the voltage across any off-state switch. The importance of balancing the voltages of these capacitors is therefore clear. Pulse-width modulation control techniques were given, as well as a look-up table-based technique. Simulations showed that both the PWM and look-up table controllers could balance the flying-capacitor voltages while actively rectifying the input current. The PWM controller, however, could not recover from a disturbance as well as the look-up table controller. As shown by [17] and [55] it is more effective to use a control scheme that directly utilises the redundant switching states to balance the flying capacitor voltages.

The simulation results proved that balancing the inner voltages of the flying-capacitor converter with a PWM controller is a difficult task. A controller that is built around using the redundancy in the amount switching states delivers far better results than the PWM controller.

Chapter 5

Predictive Control

The author of [56] states that, from a philosophical viewpoint, predictive control should be an obvious choice for controlling any system. This is because it mirrors human behaviour when it comes to making a choice on what to do next. Humans will select the control action that they think will lead to the best predicted outcome over a limited horizon. This is the base of predictive control: selecting a control input that will provide the best output some time in the future.

Hysteresis and linear control schemes with PWM are well established for power electronic converters [57]. Predictive control, on the other hand, has been kept from controlling power electronic converters because of limitations in available digital controllers. Calculation speed is of utmost importance when using predictive control and the high switching frequencies required by some converters rendered available digital controllers too slow. Predictive control could therefore only be applied to relative slow processes such as in chemical and process engineering fields [58, 59]. However, development in digital controllers in recent years made them fast and powerful enough to implement more complex control schemes. Furthermore, power electronic converters are well adapted for predictive control methods because of their discrete nature due to individual switching states.

This chapter firstly presents the terminology used in predictive control in Section 5.1. Next, different predictive control methods are discussed. Hysteresis-based, trajectory, deadbeat and models-based predictive control schemes are all considered. The modelling of a system, as well as approximations for derivatives in differential equations are given. Lastly, a simulation of a full-bridge active rectifier using finite-state model predictive control is shown.

5.1 Control Components

The predictive control law consists of different aspects [56] working together to control certain variables. These interact with each other and the system to provide the inputs that will drive the system.

5.1.1 Predictions

The basis of the predictive control law is the predictions that are made. The state in which the controllable variables will be in the future is predicted. PID control laws do not explicitly predict future values and the control input implications on the controllable variables. Predictive control explicitly predicts the system's response for all the possible control inputs.

5.1.2 System Model

To be able to predict the system's response to a control input, a model is needed. This model should take into account the control inputs, as well as the current state in which the controllable variables are. These models can be linear or non-linear.

The modelling of the system to be controlled is an important step. The author of [56] uses the term *fit for purpose* to qualify a system's model. Such a model will give accurate enough predictions without further modelling effort. For instance, a *fit for purpose* model of a non-linear system may be a linearised version.

5.1.3 Cost Function

After predicting the system's response to all the different control inputs, the predicted states should be evaluated in order to be able to choose the best action. This is done by evaluating a numerical expression that takes the controllable states of the system as its parameters. The control action that minimizes the cost function is chosen.

5.1.4 Receding Horizon

The horizon depicts how far into the future the control law will predict. The horizon is expressed as multiples of the sampling time. Assume a horizon length of two and N states that need to be predicted. At time t_0 the states at $t_0 + T_s$ are predicted, where T_s is the sampling time. Still at time t_0 , but now having the states at $t_0 + T_s$, the states at $t_0 + 2T_s$ can be predicted. Taking the N predicted states as initial values, $N \times N$ states can be predicted. The cost function can now be evaluated to obtain the route that will

minimize the cost. The route is defined as the sequence of control inputs. It is therefore theoretically possible to control a system from start-up up to its steady-state by first predicting all the routes and choosing the best one.

The receding horizon comes into play when only the first control input of the whole route is used. After the input is applied to the system and the time $t_1 = t_0 + T_s$ is reached, the whole process of determining the routes up to time $t_1 + 2T_s$ is repeated. This method of shifting the horizon one time step into future at each sampling instant has the effect of a *receding horizon*.

The horizon should be more than the settling time of the system to take dynamics into account.

5.1.5 Computation

The main disadvantage of predictive control is the large computation effort it takes. At each sampling instant all N states of the system have to be predicted. The quantity of states to be calculated increases exponentially as the horizon increases.

Furthermore, in the finite time it takes to determine the control signals for the next T_s seconds, the states of the system have already changed. The calculation delay should therefore be kept to a minimum to keep the predictions as accurate as possible.

The fast microprocessors and FPGAs available today enabled the control systems via predictive control.

5.2 Control Methods

Converter control can be divided into a number of categories. One type of these is predictive control. Figure 5.1 shows a breakdown of the different control techniques [60].

5.2.1 Hysteresis-based

Hysteresis control aims to keep the controlled variables within some boundary. Hysteresis-based predictive control will predict the outcome of the controlled variables for all the possible control inputs and then select the input that will keep the controlled variables within the boundary for the longest time. This will also automatically reduce the switching frequency to a minimum. It is an improvement on simple “bang-bang” control [61].

Figure 5.2 shows a current controller with the reference vector and boundary shown. Suppose that the power electronics converter being used to control the current has three possible switching states. At the instant that i_L reaches the boundary three trajectories,

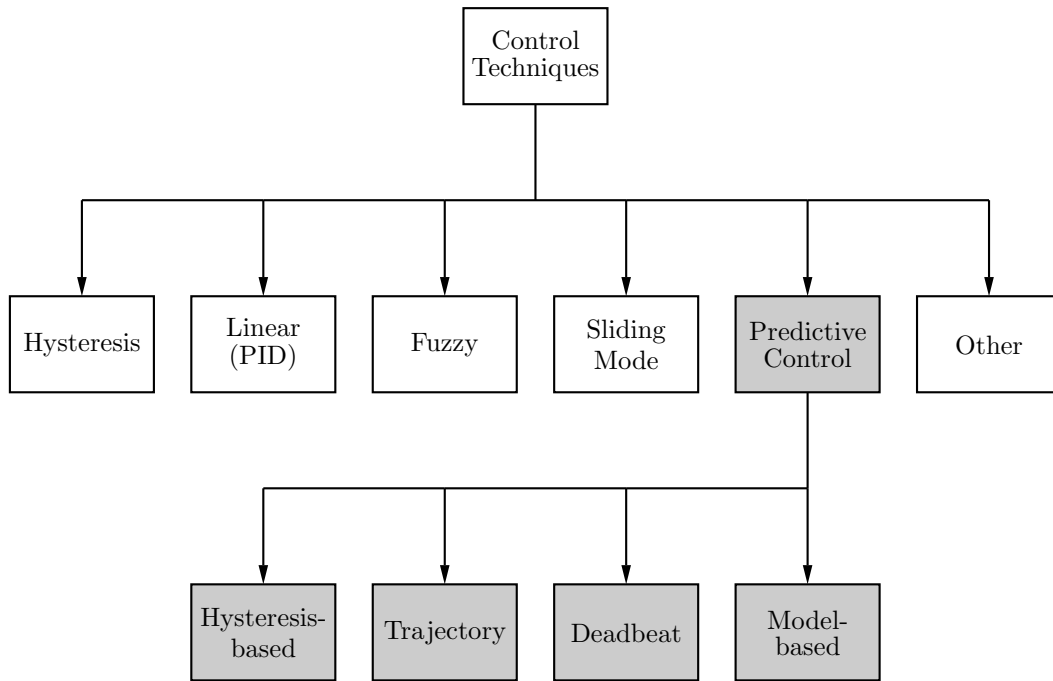


Figure 5.1: Breakdown of different control techniques

one for each of the three switching states, from the touching point are calculated. These trajectories are r_1 , r_2 and r_3 . The switching state that will keep i_L inside the boundary for the longest time will be chosen, in other words r_3 . A zero-sized hysteresis band will result in an infinite switching frequency. This is because the current will always be on or outside the hysteresis band. The switching state will therefore constantly be changed.

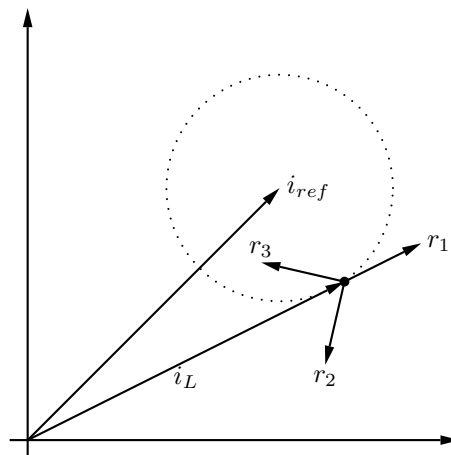


Figure 5.2: Hysteresis-based predictive control

5.2.2 Trajectory

The model of the system is used to calculate, off line, all the possible trajectories that the controlled variables can follow. When the system becomes active, the shortest route from

the initial state via the available trajectories can be determined and thus the sequence of control inputs. The system can then be steered to reach to required state. Varieties of trajectory control are direct self control [62]; direct torque control [63] and direct speed control [64].

Take direct predictive speed control as an example. The trajectories relating the system's acceleration and speed error are parabolas. The route to get to the origin at $e = 0$ can be determined and the system can be steered to reach that point. However, some tolerance band around the final value is required, because only a limited switching frequency is allowed. A zero tolerance will result in an infinite switching frequency, because the controller will want to keep the state within the tolerance band.

Figure 5.2 shows how the trajectory to reach a zero error should be chosen. It does not, however, show a tolerance band around the zero error. The trajectory that the system will move on is the shortest route from its initial state to the required state.

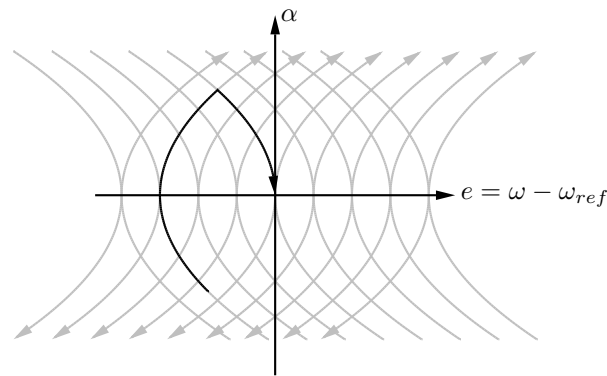


Figure 5.3: Trajectory-based predictive control

5.2.3 Deadbeat

At each sampling instant the model of the system is used to calculate the reference that will result in a zero error at the next sampling instant. For a power electronic converter under pulse width modulation control the PID controller will be replaced by the deadbeat controller, as in Figure 5.4. The references, v_{ref} and i_{ref} , is calculated and compared to the triangular carrier to determine the switching signals for the converter.

Errors in the model of the system severely degrades the performance of the controller and it could render the system unstable. Furthermore, it is difficult to include non-linearities into the controller. However, this controller has been used for inverters [65–67]; rectifiers [68]; active filters [69, 70]; UPS applications [71–73]; DC-DC converters [74]; and torque control of induction motors [75]. The author of [76] investigated the effects of the control delay on the controlled current of PWM inverters.

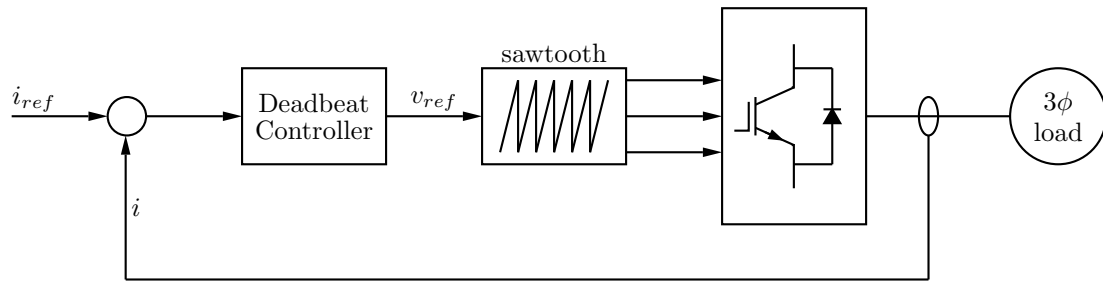


Figure 5.4: Deadbeat predictive control

5.2.4 Model-based

Model-based predictive control (MPC) is the only advanced control technique which has been successful in past decades. The advanced control techniques referred to are techniques which are more advanced than PID control. MPC allows for non-linear models and can handle general system constraints. Constraints need to be put in place to protect components against excess voltages or currents. MPC has been thoroughly researched and published with applications and results [56, 77–79].

MPC can be divided into two subsets: infinite and finite control set MPC.

5.2.4.1 Infinite Control Set

The infinite control set refers to a MPC where the controller outputs are passed through a pulse width modulator. The switching signals for the converter is obtained from the modulator. Thus, the possible reference values passed to the modulator need to be calculated and a cost function is used to choose the optimal set of references.

5.2.4.2 Finite Control Set

The finite control set MPC, FS-MPC, does not make use of a modulator to determine the switching signals for the converter. When modelling a power electronic converter, the switches can be modelled as an ideal switch with only two states: on and off. Thus, a full-bridge converter with four switches will have three unique switching states in which the converter can exist. A three-phase, three-level diode-clamped converter will have twenty-seven switching states.

The FS-MPC predicts what effect the different switching states will have on the controlled variables and then evaluates a cost function to determine the best switching state. The controller will output the switching signals directly to the power switches without using a modulator. FS-MPC has been used as a current controller for two- [80–82], three- [83, 84] and four- [85] level inverters. In addition to controlling the currents, active and reactive power can also be controlled [86]. FS-MPC has also been applied to control more complex

converters such as matrix converters [87]; direct converters [88–90]; and flying-capacitor converters [22].

Figure 5.5 shows an example of a converter under FS-MPC control. \mathbf{X}_{ref} represents the reference values for m controllable variables. $\mathbf{X}(k)$ is the m measurements taken at time k and $\mathbf{X}(k+1)$ are the predicted values of the m states for n possible switching states at time $k+1$. The predicted and reference values are used to evaluate n cost functions and the switching state that produced the lowest cost is chosen. The chosen state's switching signals, \mathbf{S} , are then output to the converter.

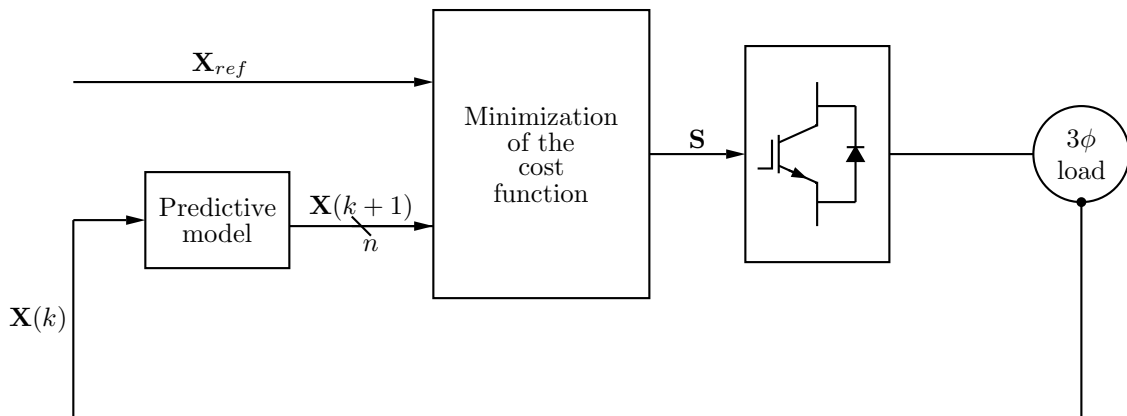


Figure 5.5: Finite control set MPC

5.3 Open-Loop vs Closed-Loop

Similar to PID control, a predictive control law can be implemented closed or open-loop.

Open-loop predictive control has an infinite prediction horizon. The optimal route from the initial conditions to the required steady-state is predicted. The control inputs that will deliver that route is applied to the system without measuring the states of the system at each sampling instant and re-calculating the route to steady-state.

Closed-loop control uses a receding horizon of length N . N sampling steps into the future are predicted and the optimal route is found by evaluating a cost function. However, only the first control input is used after which the same length N predictions are done and the optimal route is found again. The process repeats itself and each time only the first control input is used. The length of the horizon could also be infinite.

5.4 System Modelling

As stated in Section 5.2.4.2, a power electronic converter can be discretised by viewing the power switches as ideal switches with only two states: on and off [60]. This means that, by only changing the switching combinations at fixed sampling intervals, the measuring and predicting actions of the FS-MPC also only need to be done at fixed intervals. Let T_s be the sampling period of the controller and thus discretised time will be $t = kT_s$ with $k \in \{0, 1, 2, \dots\}$ the sampling instants.

The converter can be modelled so that

$$\mathbf{x}(k+1) = f(\mathbf{x}(k), \mathbf{u}(k)) \quad k \in \{0, 1, 2, \dots\} \quad (5.4.1)$$

where $\mathbf{x}(k)$ and $\mathbf{u}(k)$ are the state and control input values at time k and $\mathbf{x}(k+1)$ is the predicted state.

FS-MPC allows for constraints on both the control inputs and the systems states. Therefore, the control inputs can be restricted to

$$\mathbf{u}(k) \in \mathbf{U} \subseteq \mathbf{R}^p \quad k \in \{0, 1, 2, \dots\} \quad (5.4.2)$$

where \mathbf{U} is the set of allowable switching combinations and p is the number of switches. \mathbf{R}^p will therefore contain all the switching combinations, but, taking a flying-capacitor or diode-clamped converter, some of the combinations are not allowed.

In the same way the control system can constrain the states of the converter by

$$\mathbf{x}(k) \in \mathbf{X} \subseteq \mathbf{R}^n \quad k \in \{0, 1, 2, \dots\}. \quad (5.4.3)$$

These constraints, \mathbf{X} , can be to limit voltages or current that components are exposed to.

After predicting the states of the converter with (5.4.1) a cost function is used to evaluate the different switching states and choose the best one. When using a finite horizon of length N the following generic cost function can be used:

$$V(\mathbf{x}(k), \mathbf{u}(k)) \triangleq \sum_{l=k}^{k+N-1} Q(\mathbf{x}(l), \mathbf{u}(l)) \quad (5.4.4)$$

where

$$\mathbf{x}(l+1) = f(\mathbf{x}(l), \mathbf{u}(l)) \quad l \in \{k, k+1, k+2, \dots\} \quad (5.4.5)$$

and

$$\mathbf{u}(l) \in \mathbf{U} \quad l \in \{k+1, k+2, k+3, \dots\} \quad (5.4.6)$$

are the predicted states and control inputs. $Q(\cdot, \cdot)$ is a weighting function to penalise unwanted state or control input behaviour. If, for instance, the predicted state for a given

switching state is $\mathbf{x}(k+1) \notin \mathbf{X}$ the cost function should penalise that switching state so severely that it will not be chosen as the switching state for the next sampling period.

When the cost functions have been evaluated a whole series of control inputs, $u(l)$, are available to drive the system with. However, the receding horizon dictates that only the first control input be used and the horizon over which the values are being predicted be shifted one sample period into the future. Thus, at time $k+1$ a measurement will be taken and the predicted states will be calculated with

$$\mathbf{x}(l+1) = f(\mathbf{x}(l), \mathbf{u}(l)) \quad l \in \{k+1, k+2, k+3, \dots\}. \quad (5.4.7)$$

5.5 Approximations

Equation (5.4.1) is not necessarily a linear equation and because it has to be implemented in a digital controller this poses a problem. Non-linearities such as exponentials or logarithms are not a problem to implement, but differentials and integrals need special attention. Differentials and integrals need to be approximated by discrete-time equations that can be executed on the digital controller. Three major approximation methods for differentials are Euler forward, Euler backward and Runge-Kutta [91]. Approximations for integrals are not given because integrals do not form part the models for the power electronic converters in this thesis.

The state-space representation of a system is

$$\dot{\mathbf{x}}(t) = \mathbf{A} \cdot \mathbf{x}(t) + \mathbf{B} \cdot \mathbf{u}(t) \quad (5.5.1)$$

where $\mathbf{x}(t)$ and $\mathbf{u}(t)$ are the states and the control inputs to the system. Matrices \mathbf{A} and \mathbf{B} are the transition matrices. It is the $\dot{\mathbf{x}}(t)$ that needs to be approximated.

5.5.1 Euler Forward

The Euler forward approximation method will approximate a differential as

$$\frac{dx}{dt} \approx \frac{x(k+1) - x(k)}{T}. \quad (5.5.2)$$

Therefore, the state-space representation of a system in discrete time becomes

$$\mathbf{x}(k+1) \approx T_s \cdot (\mathbf{A} \cdot \mathbf{x}(k) + \mathbf{B} \cdot \mathbf{u}(k)) + \mathbf{x}(k). \quad (5.5.3)$$

5.5.2 Euler Backward

The Euler backward approximation method will approximate a differential as

$$\frac{dx}{dt} \approx \frac{x(k) - x(k-1)}{T}. \quad (5.5.4)$$

Therefore, the state-space representation of a system in discrete time becomes

$$\mathbf{x}(k) \approx T_s \cdot (\mathbf{A} \cdot \mathbf{x}(k) + \mathbf{B} \cdot \mathbf{u}(k)) + \mathbf{x}(k-1). \quad (5.5.5)$$

Shifting time one sample yields

$$\mathbf{x}(k+1) \approx T_s \cdot (\mathbf{A} \cdot \mathbf{x}(k+1) + \mathbf{B} \cdot \mathbf{u}(k+1)) + \mathbf{x}(k). \quad (5.5.6)$$

The difficulty with the backward method is to obtain an explicit solution for $\mathbf{x}(k+1)$. If it is possible to obtain such a solution it will result in a more stable controller for large T_s .

5.5.3 Runge-Kutta

The Runge-Kutta approximation uses a fourth-order function to approximate the gradient at time k . The process approximates the slope, $\dot{\mathbf{x}}(t)$, by averaging four slopes obtained from (5.5.1).

$$\dot{\mathbf{x}}_0 = \mathbf{A} \cdot \mathbf{x}(k) + \mathbf{B} \cdot \mathbf{u}(k) \quad (5.5.7)$$

$$\dot{\mathbf{x}}_A = \mathbf{A} \cdot \left[\mathbf{x}(k) + \frac{1}{2}T_s\dot{\mathbf{x}}_0 \right] + \mathbf{B} \cdot \mathbf{u}(k) \quad (5.5.8)$$

$$\dot{\mathbf{x}}_B = \mathbf{A} \cdot \left[\mathbf{x}(k) + \frac{1}{2}T_s\dot{\mathbf{x}}_A \right] + \mathbf{B} \cdot \mathbf{u}(k) \quad (5.5.9)$$

$$\dot{\mathbf{x}}_C = \mathbf{A} \cdot [\mathbf{x}(k) + T_s\dot{\mathbf{x}}_B] + \mathbf{B} \cdot \mathbf{u}(k) \quad (5.5.10)$$

The four slopes are averaged and the predicted states can then be calculated with

$$\mathbf{x}(k+1) = \mathbf{x}(k) + \frac{1}{6}T_s \cdot (\dot{\mathbf{x}}_0 + 2\dot{\mathbf{x}}_A + 2\dot{\mathbf{x}}_B + \dot{\mathbf{x}}_C). \quad (5.5.11)$$

5.6 Stability

Take the discrete state-space model in (5.5.1) with an initial condition \mathbf{x}_0 and constrained control inputs. The authors of [92] proved the following:

1. If λ_i , the eigenvalues of matrix \mathbf{A} in (5.5.1), lie in or on the unit circle, i.e. $|\lambda_i| \leq 1$, then $\mathbf{x}_0 \in \mathbf{X}$ can be controlled by a sequence of control inputs $\mathbf{u}(l) \in \mathbf{U}$ such that $\mathbf{x}(\infty) = \mathbf{x}_{ref}$.
2. If at least one λ_i , the eigenvalues of matrix \mathbf{A} in (5.5.1), lie outside the unit circle, i.e. $|\lambda_i| > 1$, then $\mathbf{x}_0 \in \mathbf{X}$ cannot be controlled by a sequence of control inputs $\mathbf{u}(l) \in \mathbf{U}$ such that $\mathbf{x}(\infty) = \mathbf{x}_{ref}$.

5.7 Simulation

Before being able to simulate a converter under FS-MPC it should first be modelled. The full-bridge converter in Figure 5.6 with system parameters shown in Table 5.1 is used as an active rectifier.

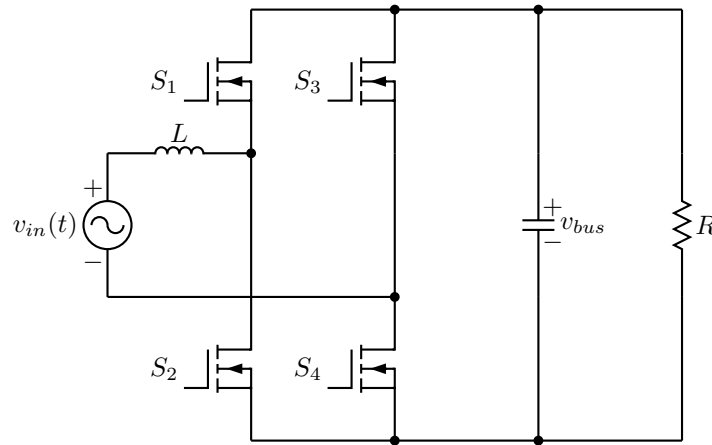


Figure 5.6: Full-bridge active rectifier

Table 5.1: Full-bridge converter simulation parameters

Parameter	Value	Description
R	360Ω	load resistance
L	20 mH	boost inductor
C	$300 \mu\text{F}$	all capacitances
v_{in}	500 V_{peak} at 50 Hz	input voltage
v_{bus}	600 V	nominal bus voltage
T_s	$50 \mu\text{s}$	sampling period

5.7.1 Modelling

The differential equation for the input current is

$$v_L = L \frac{di}{dt} \quad (5.7.1)$$

The converter has three unique switching states. For each of these a prediction equation $f(\mathbf{x}(k), \mathbf{u}(k))$ has to be derived. Equation (5.4.1) therefore has three representations. The $\frac{di}{dt}$ of (5.7.1) is approximated with the Euler forward method with v_L equal to the different voltages across the input inductor for each of the possible switching states.

State 1: S_1 and S_4 are on

$$i_L(k+1) = i_L(k) + T_s \cdot \left(\frac{v_{in}(k) - v_{bus}(k)}{L} \right) \quad (5.7.2)$$

State 2: S_2 and S_3 are on

$$i_L(k+1) = i_L(k) + T_s \cdot \left(\frac{v_{in}(k) + v_{bus}(k)}{L} \right) \quad (5.7.3)$$

State 3: S_1 and S_3 or S_2 and S_4 are on

$$i_L(k+1) = i_L(k) + T_s \cdot \left(\frac{v_{in}(k)}{L} \right) \quad (5.7.4)$$

The cost function is

$$V = |i_{ref} - i_L(k+1)| \quad (5.7.5)$$

with i_{ref} generated from a PI control loop to regulate the output voltage to 120% of the input voltage's amplitude. The weighting function Q equals 1 as there is only one term in the cost function. The control circuit is shown in Figure 5.7.

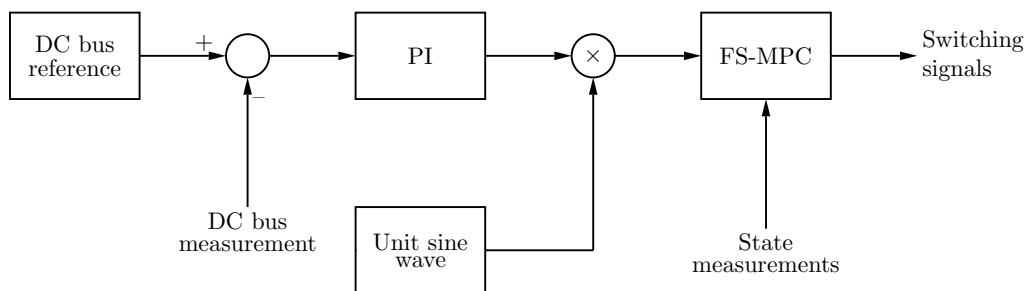
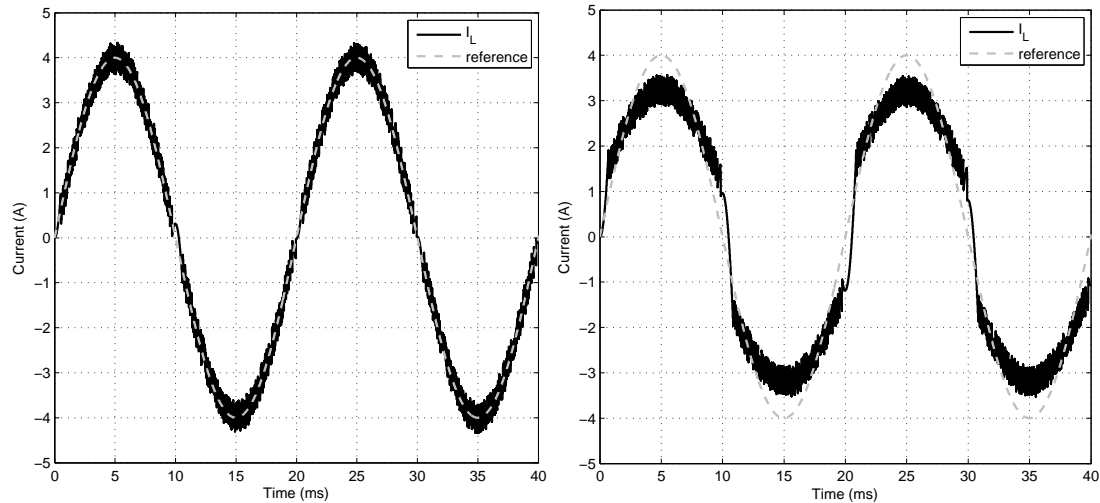


Figure 5.7: Control circuit for active rectifier



(a) Correctly modelled converter input current and reference (b) Incorrectly modelled converter input current and reference

Figure 5.8: Full-bridge active rectifier under FS-MPC control

5.7.2 Simulation Results

Figure 5.8 shows two sets of results: one where the input inductor was correctly modelled as 20 mH and the other with an incorrect value of 5 mH.

The effect of an incorrect model can be seen in the simulation results. The incorrectly modelled converter could not control its input current as well as the correctly modelled converter. Apart from this sensitivity to an incorrectly modelled system, predictive control does have its advantages:

1. It can be implemented for a variety of systems
2. Constraints on the system variables and control inputs are easily taken into account in the cost function
3. Multiple-input-multiple-output systems can be controlled

5.8 Summary

This chapter introduced various predictive control methods. It became clear that predictive control has been widely used for the control of power electronic converters and motor drives. Power electronic converters are also ideally suited for FS-MPC because of their discrete nature. The author of [60] noted that by using all the available information about the system to choose its optimal working, a very fast dynamic response can be obtained. This is primarily achievable, because predictive control does not have a cascaded

structure such as PID control. In a cascaded control system the control input first have to propagate through the whole control structure before it can have an effect on the system that is being controlled.

A finite-state model predictive control law for a full-bridge active rectifier was also implemented. The results showed the controller's sensitivity to an inaccurate model. Considering that the inductor was modelled with a 75% error, it could be argued that the controller actually did control the input current rather well.

Chapter 6

Converter Design

This chapter describes the design of the power electronic converter and other supporting hardware. The design of the converter is based on [93] and is divided into two parts: the active rectifier front-end and the isolation stage with transformer, passive rectifier and low-pass filter.

The rectifier is controlled with predictive control methods with a sampling period T_{pre} of $12.5 \mu\text{s}$. The corresponding sampling frequency f_{pre} is therefore 80 kHz. The predictive control law is thus executed at 80 kHz. If the switching period of any power switch is defined as the time in which it turns on and off once, the maximum instantaneous switching frequency of any power switch is 40 kHz, which is half the sampling frequency. The losses in the power switches, the values of the bus- and flying capacitors, and the value of the boost inductor are all designed in Section 6.1. The difficulty in calculating the losses in the power switches are due to the fact that the exact switching pattern for each power switch cannot be determined. A worst-case approach is therefore used to obtain an upper limit on the losses.

The isolation stage is switched at a constant duty cycle at a frequency f_{iso} of 40 kHz. The same full-bridge, three-level flying-capacitor converter as for the active rectifier is used. However, the multilevel switching is not utilised. The series pairs of power switches are switched together so that the converter essentially operates as a conventional full-bridge converter. The design consists of the losses in the power switches, the LC filter for the passive rectifier and the transformer. Although the multilevel switching of the isolation stage converter is not utilised, the flying capacitors still need balanced voltages. Balancing resistors are designed for this purpose.

The supporting hardware includes the power switch driver circuits and the driver circuit power supplies. A bootstrap scheme is used to power the drivers.

6.1 Active Rectifier

The full-bridge, three-level flying-capacitor active rectifier in Figure 6.1 consists of the following components that need to be designed:

- Power switches
- Bus capacitor
- Flying capacitors
- Boost inductor

Some difficulty in designing these components arise when the rectifier is under predictive control. This is because the voltage and current waveforms applicable to each component cannot be predicted. This, however, is not a problem when using PWM control methods. The techniques used in designing the converter when it is operating under PWM control is still used, though it is adapted to ensure the safe operation of the converter instead of very accurate designed values.

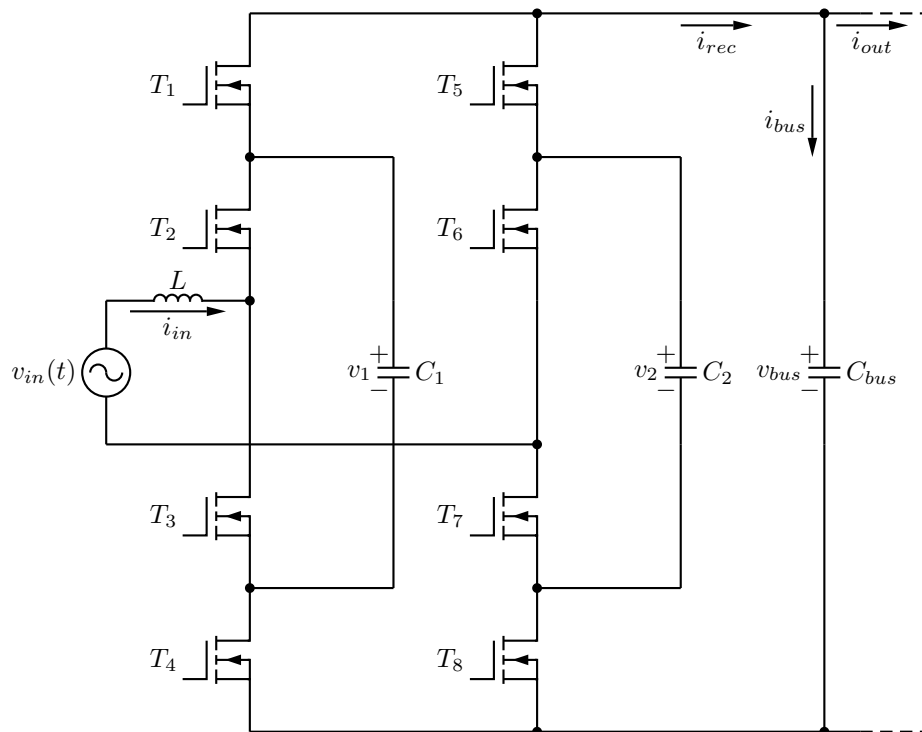


Figure 6.1: Full-bridge, three-level flying-capacitor active rectifier

The active rectifier is operated to draw power at unity power factor. The assumption can therefore be made that the input current will be sinusoidal and in-phase with the input voltage.

For a 1 kW, 600 V bus voltage converter operating with a 20% boost factor, the input voltage should have a 500 V amplitude. The amplitude of the input current for a 1 kW power rating is calculated in (6.1.1).

$$\begin{aligned}
 P &= v_{in(rms)} i_{in(rms)} \\
 &= \frac{v_{in(peak)}}{\sqrt{2}} \cdot \frac{i_{in(peak)}}{\sqrt{2}} \\
 i_{in(peak)} &= \sqrt{2} \cdot 1 \times 10^3 \cdot \frac{\sqrt{2}}{500} \\
 i_{in(peak)} &= 4 \text{ A}
 \end{aligned} \tag{6.1.1}$$

At a bus voltage of 600 V an equivalent load resistor of 360Ω across the bus capacitor is needed for a 1 kW load.

6.1.1 Power Switches

To be able to choose correct power switches several factors need to be taken into account. Firstly, consider the voltage and current stresses that the switches need to withstand. For a three-level converter the theoretical withstand voltage is half the DC bus voltage. The withstand current is the input current calculated in (6.1.1).

Secondly, the power dissipation in the switches need to be calculated to be able to provide enough cooling. Both conduction and switching losses contribute to the heating of the switch. The predictive control scheme used makes it difficult to predict when the individual switches will change their states. To be able to calculate the dissipated power in the switches two assumptions are made:

1. For the conduction losses it is assumed that the switch conducts continuously, i.e. it is not switched and the current through the switch is therefore smooth.
2. For the switching losses it is assumed that the switch is operating at its maximum switching frequency, i.e. it is switching at $\frac{1}{2}f_{pre}$.

These assumptions will provide the worst-case power dissipation. The chosen MOSFET is the *STP20NM60FD* from STMicroelectronics. Its parameters are summarised in Table 6.1.

6.1.1.1 Conduction Losses

Conduction losses in a MOSFET occurs because of its on-state resistance $R_{DS(on)}$. Current flowing through this resistance dissipates power. Assuming that the switches conduct continuously the current paths in Figure 6.2 applies. With a peak current of 4 A and a

Table 6.1: MOSFET Parameters

Parameter	Value	Description
V_{DS}	600 V	maximum drain-source voltage
I_D	20 A	maximum continuous drain current
$R_{DS(on)}$	290 m Ω	static drain-source on resistance
R_{th-jc}	0.65 K/W	junction-case thermal resistance
$V_{GS(th)}$	5 V	maximum gate threshold voltage
V_D	1.5 V	anti-parallel diode turn-on voltage
t_{on}	12 ns	rise time
t_{off}	22 ns	fall time

$R_{DS(on)}$ of 290 m Ω , the maximum on-voltage of each MOSFET will be 1.16 V. This is less than the turn-on voltage of the anti-parallel diode of the MOSFET. The current shown in Figure 6.3 will therefore only flow through each of the eight MOSFETs; not their anti-parallel diodes. The conduction losses of each MOSFET can be calculated by obtaining the root-mean-square (RMS) current through the MOSFET and multiplying it with its on-resistance.

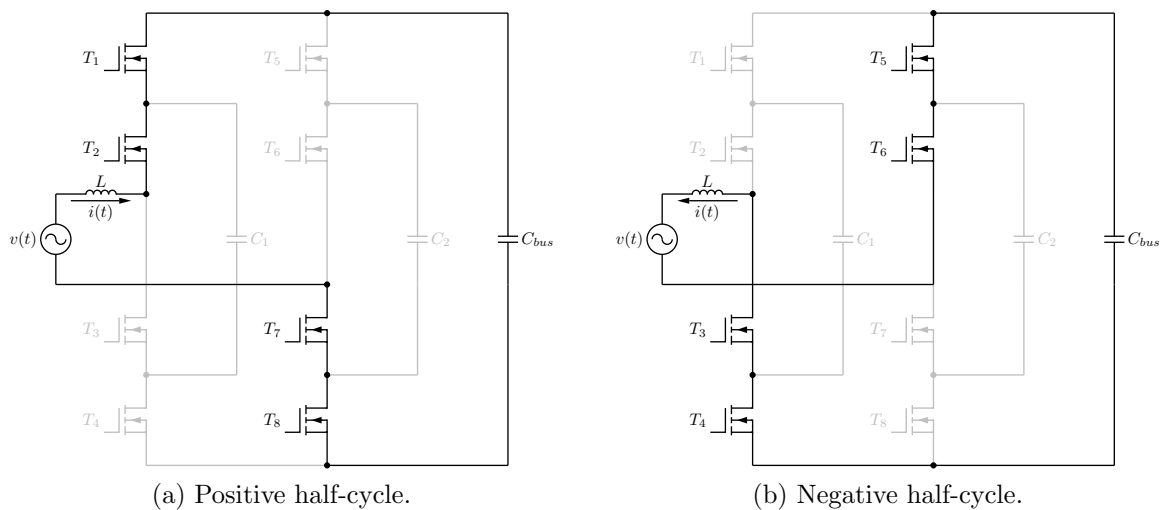
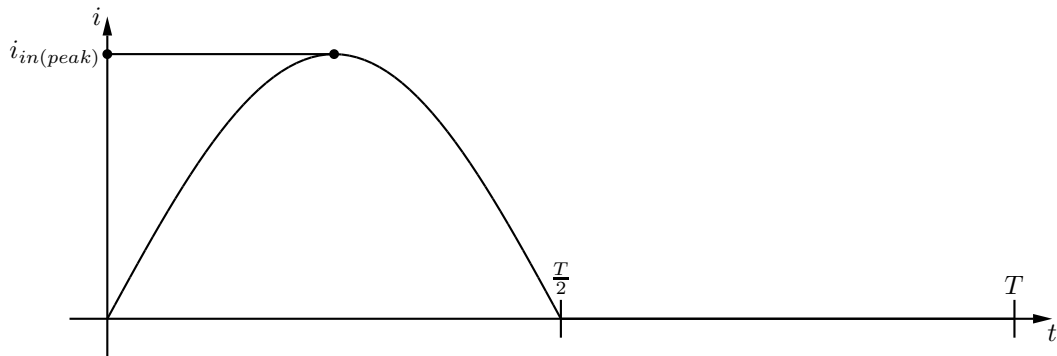


Figure 6.2: Current flow through MOSFETs for worst-case losses.

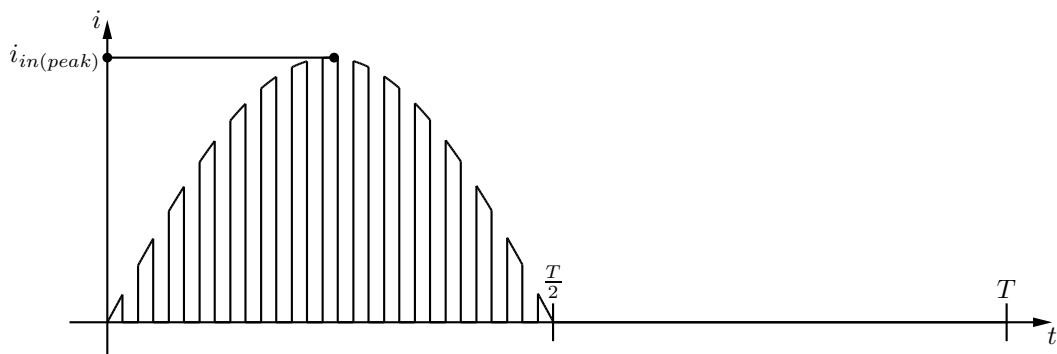
Figure 6.3: Worst-case current through switch T_1 when it is not switched

The conduction losses for a single MOSFET is calculated in (6.1.2).

$$\begin{aligned}
 P_{cond} &= i_{in(rms)}^2 R_{DS(on)} \\
 &= \frac{1}{2\pi} \int_0^\pi i_{in(peak)}^2 \sin^2 \theta \, d\theta \times R_{DS(on)} \\
 &= \frac{1}{4} i_{in(peak)}^2 R_{DS(on)} \\
 &= \frac{1}{4} \cdot 4^2 \cdot 0.29 \\
 &= 1.16 \text{ W}
 \end{aligned} \tag{6.1.2}$$

6.1.1.2 Switching Losses

To calculate the switching losses of the power switches, the voltage in their off-state and the current in their on-state are needed. The clamping mechanism of the flying-capacitor converter will force the voltage across the switches to be half the DC bus voltage. The current through the switches is assumed to be sinusoidal with peak value $i_{in(peak)}$. Furthermore, it is assumed that each switch will only carry one half-cycle of the 50 Hz input current. The current paths as shown in Figure 6.2 again apply. The current through switch T_1 is shown in Figure 6.4.

Figure 6.4: Current through switch T_1 when it is switching

The energy dissipated with each state transition of the switch is

$$E_{switch} = \frac{1}{2} \frac{v_{bus}}{2} i_{in(peak)} \sin(\omega t) (t_{on} + t_{off}) \quad (6.1.3)$$

where ω equals the input current's frequency.

The total power dissipated in each power switch is calculated in (6.1.4).

$$\begin{aligned} P_{switch} &= \frac{1}{T} \sum_{k=0}^N \frac{1}{4} v_{bus} i_{in(peak)} \sin(\omega t_k) (t_{on} + t_{off}) \\ &= \frac{1}{4T T_{pre}} v_{bus} i_{in(peak)} (t_{on} + t_{off}) \sum_{k=0}^N \sin(\omega t_k) T_{pre} \\ &\approx \frac{1}{4T T_{pre}} v_{bus} i_{in(peak)} (t_{on} + t_{off}) \int_0^{\frac{T}{2}} \sin(\omega t) dt \\ &= \frac{f_{pre}}{4\pi} v_{bus} i_{in(peak)} (t_{on} + t_{off}) \\ &= \frac{80 \times 10^3}{4\pi} \cdot 600 \cdot 4 \cdot (12 + 22) \times 10^{-9} \\ &= 520 \text{ mW} \end{aligned} \quad (6.1.4)$$

6.1.1.3 Heat sink

The total losses in each MOSFET is calculated in (6.1.5).

$$\begin{aligned} P_{tot} &= P_{cond} + P_{switch} \\ &= 1.16 + 0.52 \\ &= 1.68 \text{ W} \end{aligned} \quad (6.1.5)$$

All eight MOSFETs of the rectifier are mounted on the same heat sink and their junction temperatures should be kept below 100°C. The power dissipations and thermal resistances can be presented as in Figure 6.5. R_{th-jc} is the junction-to-case thermal resistance of the MOSFET, R_{th-cs} is the case-to-heatsink resistance and R_{th-sa} is the heatsink-to-ambient resistance. The junction temperature can be calculated from

$$T_j = T_a + P_{tot}(R_{th-jc} + R_{th-cs}) + 8P_{tot}R_{th-sa} \quad (6.1.6)$$

where T_a equals 25°C, R_{th-jc} equals 0.65 K/W, R_{th-cs} equals 1.5 K/W and R_{th-sa} is the unknown. To limit the MOSFET junction temperatures to 100°C the maximum R_{th-sa} is calculated to be 5.4 K/W. A heat sink of 1.3 K/W was used.

6.1.2 DC-Link Capacitors

Factors to include in designing the DC-link capacitors include the voltage and current ratings, as well as the capacitance. The bus capacitor of the 600 V converter should have

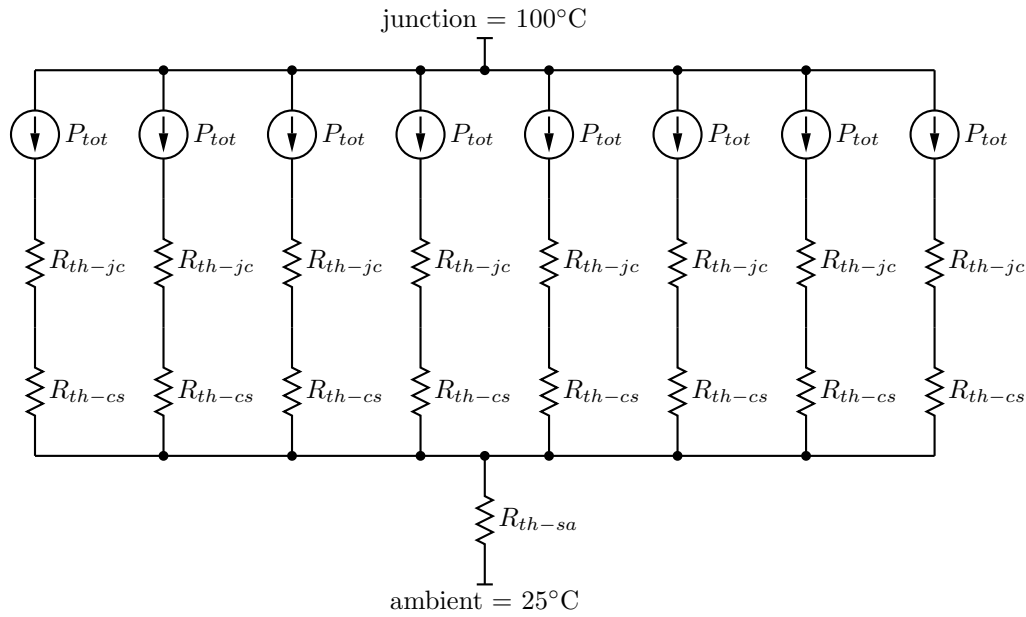


Figure 6.5: Bus capacitor current waveform

a theoretical voltage rating of 600 V. To have some safety factor and taking into account that the measurement circuits can operate at 800 V, the voltage rating of the bus capacitor is set at 800 V. From a similar deduction the voltage ratings of the flying capacitors are set at 400 V.

To calculate the capacitance required to limit the bus voltage ripple, the netto current through the bus capacitor is considered. Assuming that the input current is sinusoidal the netto current flowing through the bus capacitor can be drawn as in Figure 6.6 when i_{out} is assumed to be DC. When the current is positive the bus voltage will increase from the increase in charge in the capacitor. A negative current will decrease the voltage. The capacitance required to limit the change in voltage is defined as

$$C = \frac{\Delta Q}{\Delta V} \quad (6.1.7)$$

where

$$\begin{aligned} \Delta Q &= \text{area under positive current} \\ &= \int_{t_1}^{t_2} (i_{rec(peak)} \sin(\omega t) - i_{out}) dt. \end{aligned} \quad (6.1.8)$$

The current i_{out} can be calculated from $\frac{v_{bus}}{R_{load}} = 1.667$ A. To obtain $i_{rec(peak)}$ a conventional boost converter is first considered. A boost converter has the following relationship for its input and output voltage and current:

$$\frac{V_o}{V_d} = \frac{1}{D} = \frac{I_d}{I_o} \quad (6.1.9)$$

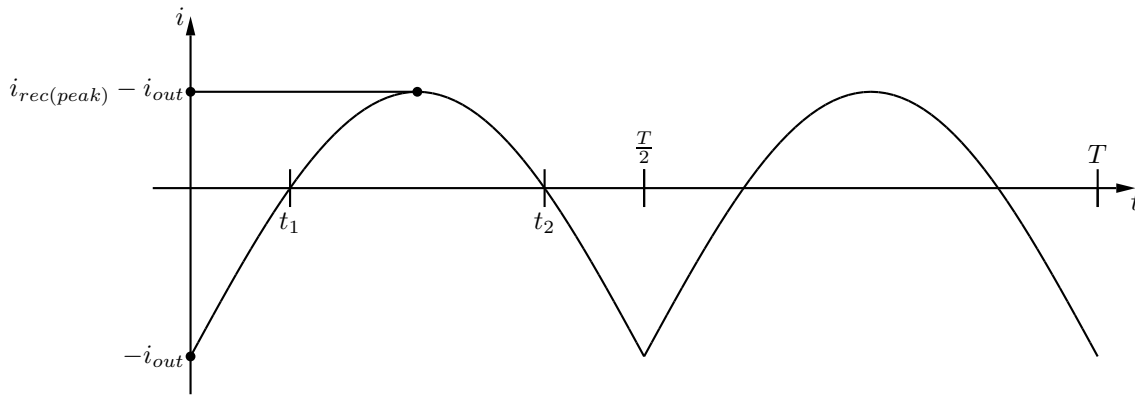


Figure 6.6: Bus capacitor current waveform

where the o -subscript designates the output, the d -subscript the input and D the duty cycle of the PWM controlled power switch. Adapting this for the active rectifier in Figure 6.1 it becomes

$$\frac{v_{bus}}{v_{in(rms)}} = \frac{1}{D_{eff}} = \frac{i_{in(rms)}}{i_{rec(rms)}} \quad (6.1.10)$$

with D_{eff} an effective duty cycle. With $v_{bus} = 600$ V and $v_{in(rms)} = \frac{500}{\sqrt{2}}$ the duty cycle is calculated as 0.589. With $i_{in(rms)} = \frac{4}{\sqrt{2}}$ the RMS value $i_{rec(rms)}$ is 1.667 A.

The relationship between the peak and RMS value of a full wave rectified sinusoidal current is

$$i_{rms} = i_{peak} (1 - e^{-1}) . \quad (6.1.11)$$

From (6.1.11) and knowing that $i_{rec(rms)}$ equals 1.667 A, $i_{rec(peak)}$ can be calculated to be 2.637 A. Through equations (6.1.7) and (6.1.8) the bus capacitance was chosen as 300 μ F for a voltage ripple of less than 5%.

It could happen that the flying capacitors be exposed to the same current waveform as for the bus capacitor. The flying capacitors is therefore chosen to also be 300 μ F with the same current rating as the bus capacitor. The voltage rating of the flying capacitors can, however, be half the bus voltage.

6.1.3 Boost Inductor

An inductor at the input of the active rectifier is needed to let the rectifier operate as a boost converter. The maximum voltage transition across the inductor is taken to be the bus voltage. This will occur when the control algorithm changes the switching state between *state 1*¹ and any of the *state 3* states. In *state 1* the converter's output will equal the bus voltage with *state 3* equalling zero. It should be highly unlikely that the control algorithm would want to change between *state 1* and *state 5* and therefore cause the voltage transition to be double the bus voltage.

¹see section B.2, Flying-Capacitor Converter Modelling

The value of the inductor is calculated in (6.1.12) allowing a 10% input current ripple.

$$\begin{aligned}
 L &= \frac{v \, dt}{di} \\
 &= \frac{v_{bus} T_{pre}}{0.1 i_{in(peak)}} \\
 &= \frac{600 \cdot 12.5 \times 10^{-6}}{0.1 \cdot 4} \\
 &= 18.75 \text{ mH}
 \end{aligned} \tag{6.1.12}$$

6.2 Isolation Stage

The circuit in Figure 6.7 represents the isolation stage of the back-to-back converter. Because the main focus of this project is the active rectifier with predictive control, the isolation stage was kept simple. It is only used to chop the DC bus voltage to a high frequency square wave to pass the power across the isolation barrier. The multilevel switching characteristics of the converter is therefore not utilised. To produce the square wave the isolation stage is switched similar to a bi-polar, full-bridge DC-to-DC converter. A full-bridge DC-to-DC converter cannot, however, be used. The series connected power switches of the flying-capacitor converter are needed to obtain the required voltage rating for the isolation stage. A full-bridge, three-level converter was designed, but it was operated as a full-bridge, two-level converter. The isolation stage is operated at a fixed frequency f_{iso} of 40 kHz and fixed duty cycle of 45%.

The transformer's primary voltage is shown in Figure 6.8 to illustrate the operation of the switches. The switches are operated in two pairs: T_1, T_2, T_7 and T_8 are always switched together; and T_3, T_4, T_5 and T_6 are always switched together. Letting T_{iso} be one switching period and D the duty cycle at which each switch is operated, the following switching states can be defined:

- T_1, T_2, T_7 and T_8 on for $0 < t < D \cdot T_{iso}$
- all off for $D \cdot T_{iso} < t < T_{iso}/2$
- T_3, T_4, T_5 and T_6 on for $T_{iso}/2 < t < (\frac{1}{2} + D) \cdot T_{iso}$
- all off for $(\frac{1}{2} + D) \cdot T_{iso} < t < T_{iso}$

Figure 6.8 shows different waveforms needed to design the inverter [31]. To determine the relation between the duty cycle at which the switches are operated, the input voltage v_{bus} , the transformer's winding ratio $\frac{N_2}{N_1}$, and the output voltage v_o , the voltage across the

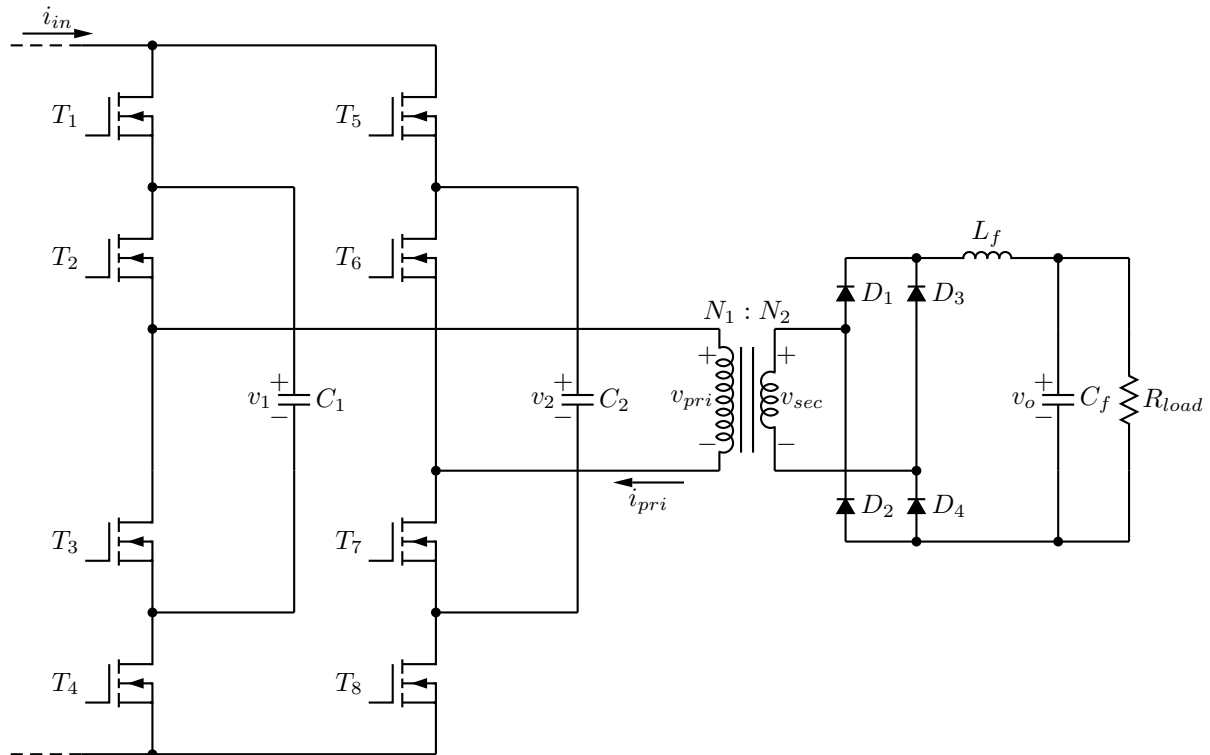


Figure 6.7: Three-level, flying-capacitor converter with transformer and passive rectifier

filter inductor is used. The characteristic of an inductor that the average voltage across it must be zero is used in (6.2.1).

$$\begin{aligned} \left(v_{bus} \cdot \frac{N_2}{N_1} - v_o \right) \cdot D T_{iso} &= v_o \cdot \left(\frac{1}{2} - D \right) \cdot T_{iso} \\ D v_{bus} \frac{N_2}{N_1} &= \frac{v_o}{2} \\ v_o &= 2 D v_{bus} \frac{N_2}{N_1} \end{aligned} \quad (6.2.1)$$

Choosing the transformer's winding ratio as 2:1 and the duty cycle 45%, the output voltage is set to 270 V. To have a 1 kW load, a resistor of 72.9 Ω should be used.

6.2.1 Passive Rectifier

The output current through the load resistor is equal to 3.7 A. This is also assumed to be the average current through the filter inductor i_{L_f} . The DC component of the filter inductor's current is assumed to flow through the load while the ripple is absorbed by the filter capacitor.

The inductance of the filter inductor can be calculated from the inductor's current. A

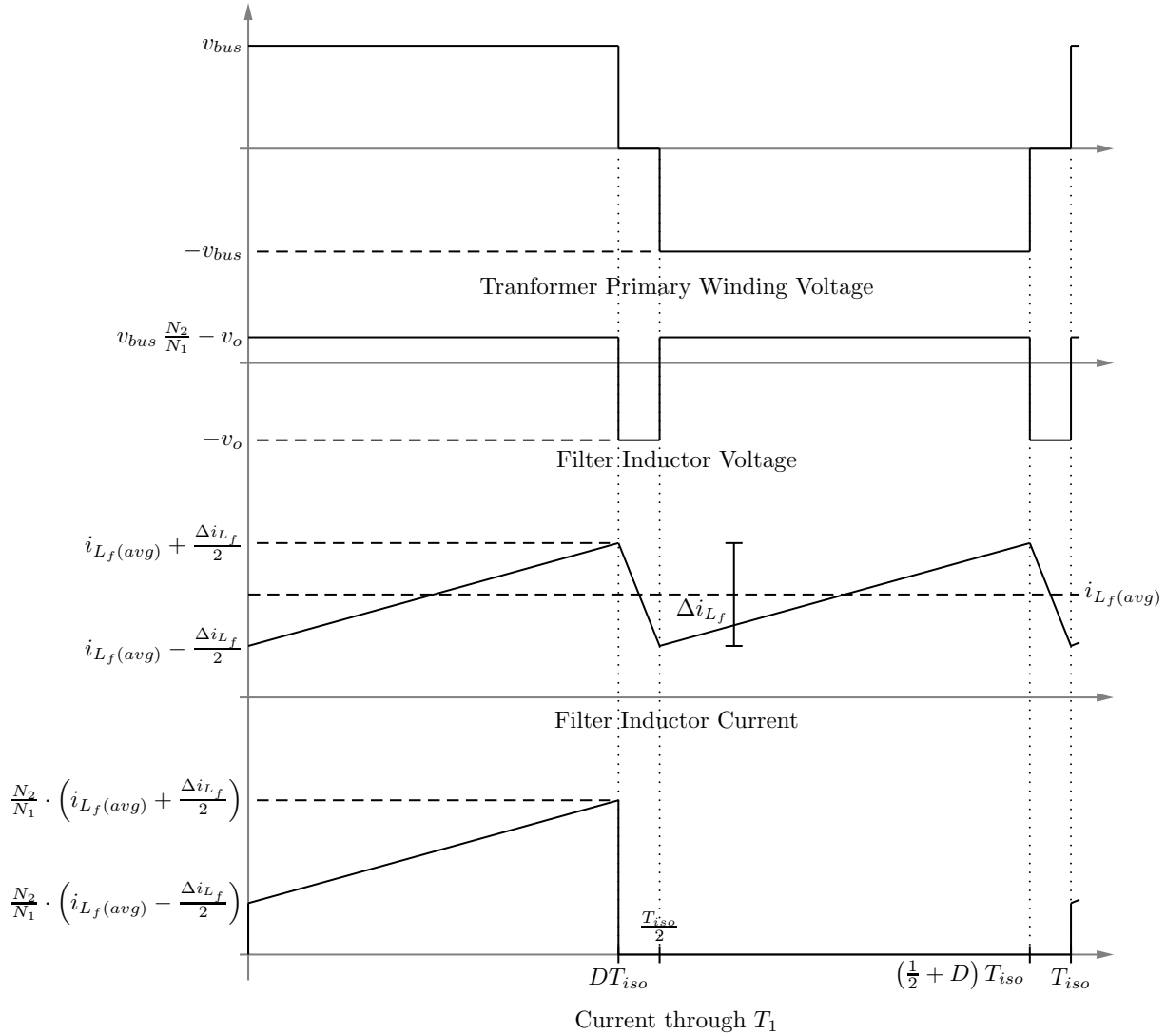


Figure 6.8: Voltage and current waveforms for the inverter

10% current ripple is assumed.

$$\begin{aligned}
 \Delta i_{L_f} &= \frac{D T_{iso}}{L_f} \left(v_{bus} \cdot \frac{N_2}{N_1} - v_o \right) \\
 L_f &= \frac{0.45 \cdot 25 \times 10^{-6} \cdot \left(600 \cdot \frac{1}{2} - 270 \right)}{0.1 \cdot 3.7} \\
 &= 912 \mu\text{H}
 \end{aligned} \tag{6.2.2}$$

The value of the filter capacitor is calculated in (6.2.3) from the inductor's ripple current allowing for a 10 V ripple.

$$\begin{aligned}
 C_f &= \frac{\Delta Q}{\Delta v_o} \\
 &= \frac{\frac{1}{2} \cdot \frac{T_{iso}}{4} \cdot \frac{\Delta i_{L_f}}{2}}{10} \\
 &= 57.8 \text{ nF}
 \end{aligned} \tag{6.2.3}$$

6.2.2 Power Switches

The switches used in the isolation stage also need to be able to withstand half the bus voltage. Their current rating is equal to the peak filter inductor current referenced to the primary of the transformer. The parameters listed in Table 6.1 applies.

6.2.2.1 Conduction Losses

The conduction losses of the MOSFETs can be calculated from the current waveform through switch T_1 in Figure 6.8. The current through the switches will equal i_{pri} for the $D \cdot T_{iso}$ period that the switch is on. The conduction losses of each MOSFET is calculated in (6.2.4).

$$\begin{aligned}
 P_{cond} &= i_{pri(rms)}^2 R_{DS(on)} \\
 &= \frac{1}{T_{iso}} \int_0^{DT_{iso}} \left[\frac{\Delta i_{L_f} \cdot \frac{N_2}{N_1}}{D T_{iso}} t + \left(i_{L_f} - \frac{\Delta i_{L_f}}{2} \right) \frac{N_2}{N_1} \right]^2 dt \times R_{DS(on)} \\
 &= 293 \text{ mW}
 \end{aligned} \tag{6.2.4}$$

6.2.2.2 Switching Losses

The derivation of the switching losses in the isolation stage switches is similar to that of the active rectifier's, the difference being that the converter does not output a sinusoidal current. The switching losses for one MOSFET is calculated in (6.2.5).

$$\begin{aligned}
 P_{switch} &= P_{switch(on)} + P_{switch(off)} \\
 &= \frac{1}{2} \frac{v_{bus}}{2} \frac{N_2}{N_1} (i_{L_f(min)} t_{on} + i_{L_f(max)} t_{off}) f_{iso} \\
 &= \frac{1}{2} \cdot \frac{600}{2} \cdot \frac{1}{2} \cdot ((3.7 - 0.37) \cdot 12 \times 10^{-9} + (3.7 + 0.37) \cdot 22 \times 10^{-9}) \cdot 40 \times 10^3 \\
 &= 389 \text{ mW}
 \end{aligned} \tag{6.2.5}$$

6.2.2.3 Heatsink

The total losses in each MOSFET is calculated in (6.2.6).

$$\begin{aligned}
 P_{tot} &= P_{cond} + P_{switch} \\
 &= 0.293 + 0.389 \\
 &= 682 \text{ mW}
 \end{aligned} \tag{6.2.6}$$

Again, all eight MOSFETs of the rectifier are mounted on the same heat sink and their junction temperatures should be kept below 100°C. The same approach as in Section 6.1.1.3 is followed and a heat sink with a thermal resistance of less than 13.5 K/W is needed.

6.2.3 DC-Link Capacitors

Although the flying-capacitor isolation stage does not utilise its multilevel capabilities, the flying capacitors cannot be omitted. For the converter, the main function of the flying capacitors is snubbing. The switching scheme, however, cannot actively balance the voltages and balancing resistors are therefore needed. The balancing circuit is shown in Figure 6.9.

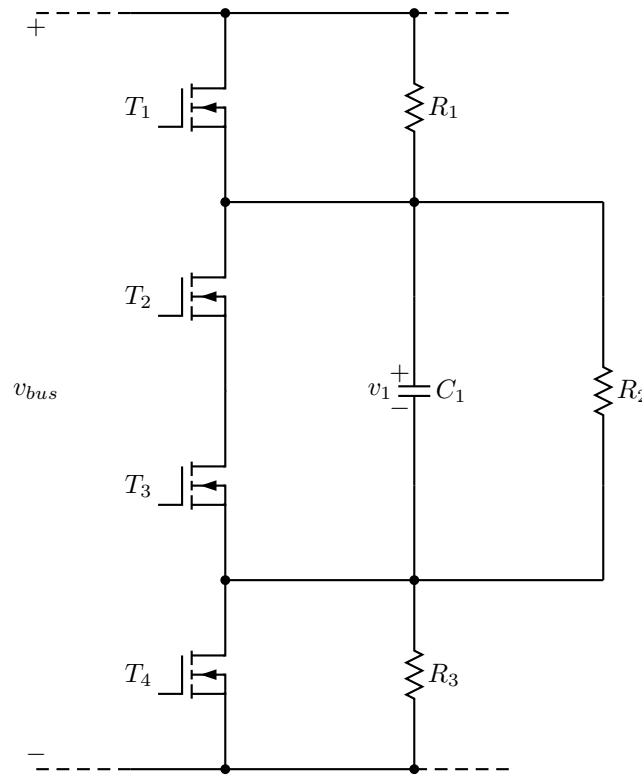


Figure 6.9: Balancing resistors for the inverter's flying-capacitors

The switching scheme used for the isolation stage has the advantage that no current will flow through the flying capacitors. Only when the voltages of the capacitors are not equal to half the bus voltage, will current flow to balance the voltages. The values of the balancing resistors need to be calculated. The switching scheme for the isolation stage will have both T_1 and T_2 on for 45% of the time. Both T_3 and T_4 will also be on for 45% of the time. For the remaining 10% the resistors and flying capacitor is connected to the DC bus. Therefore, by using voltage division and the amount of time the converter spends in each state the following can be obtained:

$$\begin{aligned}
 v_1 &= 0.45 \times \frac{R_2}{R_1 + R_2} \cdot v_{bus} + \\
 & 0.45 \times \frac{R_2}{R_3 + R_2} \cdot v_{bus} + \\
 & 0.1 \times \frac{R_2}{R_1 + R_2 + R_3} \cdot v_{bus}
 \end{aligned} \tag{6.2.7}$$

To limit the power dissipation in the balancing circuits to 10 W per flying capacitor we choose $R_1 = R_3 = 10 \text{ k}\Omega$ and wanting $v_1 = 300 \text{ V}$:

$$\begin{aligned} v_{C_1} &= \frac{0.9 R_2 v_{bus}}{R_1 + R_2} + \frac{0.1 R_2 v_{bus}}{2 R_1 + R_2} \\ 300 &= \frac{0.9 \cdot R_2 \cdot 600}{10 \times 10^3 + R_2} + \frac{0.1 \cdot R_2 \cdot 600}{2 \cdot 10 \times 10^3 + R_2} \\ R_2 &= 10.7 \text{ k}\Omega \end{aligned} \quad (6.2.8)$$

Although the mean voltage of the flying capacitor will be equal to 300 V with $R_1 = R_3 = 10 \text{ k}\Omega$ and $R_2 = 10.7 \text{ k}\Omega$, it will still have a ripple superimposed on it due to the switching that occurs. The value of the capacitor has to be chosen in such a way that it will limit this ripple. The balancing circuit for one leg of the converter has three configurations depending on the switching state of the power switches. These three are shown in Figure 6.10. Figure 6.10(a) shows where switches T_1 and T_2 are on, shorting out resistor R_1 ; Figure 6.10(b) shows switches T_3 and T_4 on, shorting out resistor R_3 ; and Figure 6.10(c) shows all the switches in their off-state. The time-domain expression for the voltage across the flying capacitor is given in (6.2.9).

$$v_1(t) = \frac{R_2 v_{bus}}{R_1 + R_2 + R_3} + \frac{(R_1 + R_2 + R_3)v_1(0) - R_2 v_{bus}}{(R_1 + R_2 + R_3)} e^{\left(\frac{-t(R_1+R_2+R_3)}{R_1 R_2 C_1 + R_2 R_3 C_1}\right)} \quad (6.2.9)$$

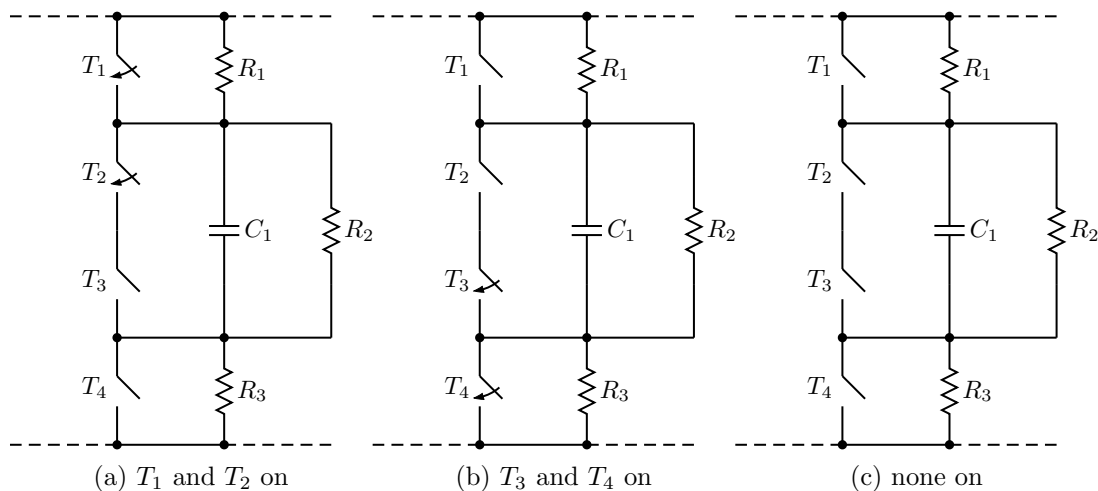


Figure 6.10: Three possible switching state associated with the balancing circuit.

During times when switches T_1 and T_2 are turned on, resistor R_1 is shorted out through T_1 . T_3 and T_4 have a similar effect of R_3 . When the resistor is shorted out it should be set to equal zero in (6.2.9). Using the switching information and (6.2.9) the value of the flying capacitor can now be chosen to limit its voltage ripple. A $10 \mu\text{F}$ capacitor was chosen for a negligibly small ripple.

6.2.4 Transformer

As stated earlier, the transformer should have a winding ratio of 2:1. Using an EPCOS ETD 54/28/19 core from N97 material the transformer was constructed. Table 6.2 lists the core's parameters [94].

Table 6.2: EPCOS ETD 54/28/19 ferrite core parameters

Parameter	Value	Description
R_{th}	15 K/W	thermal resistance of core
A_e	280 mm ²	effective cross-area
V_e	35 600 mm ³	core volume
A_N	315.6 mm ²	winding area
I_N	96 mm	effective winding length
k_{Cu}	0.5	fill factor

By choosing the maximum flux density of the core to be 100 mT the transformer's core losses can be approximated as 1.4 W. This is taken from the N97 material's characteristics showing its losses per volume with respect to the maximum flux density [95]. Taking the fill factor into account, the winding for the primary and secondary winding becomes 157.8 mm². By dividing the available winding area between the primary and secondary winding by the transformer's winding ratio of 2:1, the available area for each winding becomes:

$$A_1 = 105.2 \text{ mm}^2$$

$$A_2 = 52.6 \text{ mm}^2$$

The number of primary windings needed to keep the core from saturating is calculated in (6.2.10).

$$\begin{aligned}
 N_1 &= \frac{v_{bus} D T_{iso}}{4 B_{max} A_e} \\
 &= \frac{600 \cdot 0.45 \cdot 25 \times 10^{-6}}{4 \cdot 100 \times 10^{-3} \cdot 280 \times 10^{-6}} \\
 &= 62
 \end{aligned} \tag{6.2.10}$$

The number of secondary windings is therefore 31.

Litz-wire is used to overcome the skin effect of the copper wire when high frequency currents flow through it. Isolated parallel strands with a diameter smaller than a skin depth is used to make up the Litz-wire. Pre-fabricated Litz-wire consisting of 40 0.2 mm

strands was used. Each strand therefore has a cross sectional area A_{wire} of 0.0314 mm^2 . The total area required for all the windings of the transformer is calculated in (6.2.11).

$$\begin{aligned} A_{tot} &= A_{1(Litz)} + A_{2(Litz)} \\ &= (N_1 + N_2) \cdot 40 \cdot A_{wire} \\ &= 116.8 \text{ mm}^2 \end{aligned} \quad (6.2.11)$$

A_{tot} is less than the available $A_1 + A_2 = 157.8 \text{ mm}^2$ winding area which means that all the windings will fit onto the core.

To calculate the total transformer losses the copper losses due to the current in the primary and secondary windings are needed. The copper losses in the primary winding is calculated in (6.2.12).

$$\begin{aligned} P_1 &= i_{rms}^2 R_1 \\ &= i_{rms}^2 \frac{\rho_{Cu} l}{A} \\ &= i_{rms}^2 \frac{\rho_{Cu} N_1 I_N}{x_1 \cdot A_{wire}} \\ &= 1.87^2 \cdot \frac{1.72 \times 10^{-8} \cdot 62 \cdot 96 \times 10^{-3}}{40 \cdot 0.0314 \times 10^{-6}} \\ &= 285 \text{ mW} \end{aligned} \quad (6.2.12)$$

The secondary winding's copper losses are 558 mW. The total transformer losses is therefore 2.25 W. With a thermal resistance R_{th} of 15 K/W the transformer will have a temperature rise of about 35°C . The transformer will therefore operate within its limits.

6.3 Driver Circuits

Optic fibre carries the switching signals from the controller to the respective power switches where a driver circuit receives them. Each power switch has its own driver, because the switches need to be operated at different voltage levels. Because the switches operate at different voltage levels, a bootstrap supply [93] has to provide power to all the driver circuitry.

The bootstrap supply is shown in Figure 6.11. Capacitors C_x are known as the bootstrap capacitors. C_4 is charged directly from the 35 V power supply. When switch T_4 is turned on, the source of MOSFET T_3 is pulled down to the source of T_4 . This puts the bootstrap capacitors C_3 and C_4 in parallel with bootstrap diode D_3 between them. C_4 will therefore charge C_3 up to a voltage of one diode voltage drop less than the voltage of C_4 . When switch T_3 is turned on, C_3 will charge C_2 through D_2 . Similarly, C_2 will charge C_1 through D_1 when switch T_2 is turned on.

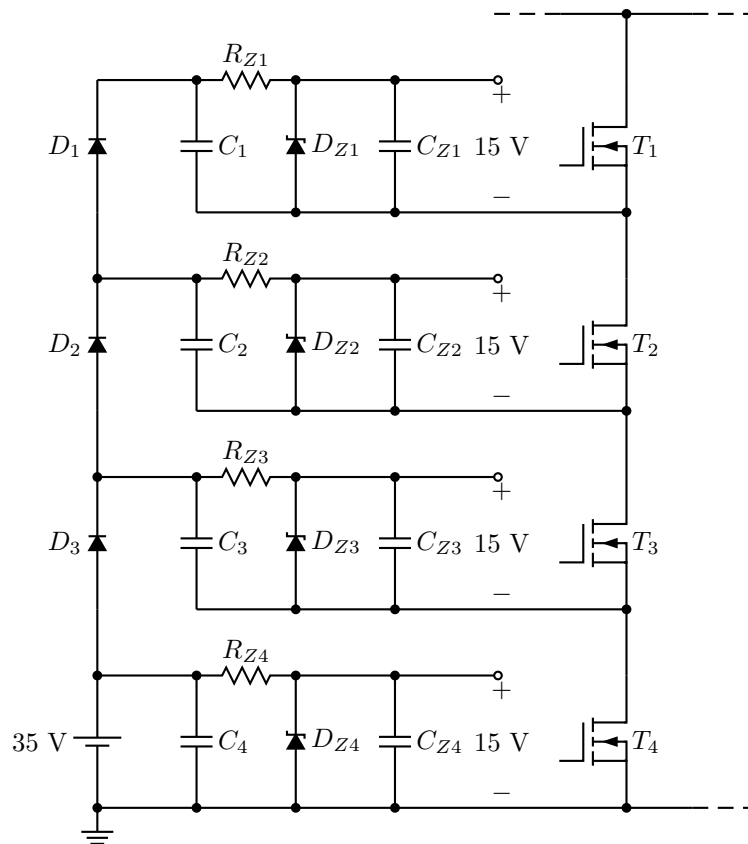


Figure 6.11: Bootstrap driver circuit for one leg.

The voltages of the bootstrap capacitors varies during switching because of their bootstrapped charging and discharging. Their voltages are also too high, from 35 V for C_4 down to approximately 30 V for C_1 . The voltage decrease is due to the subsequent voltage drops across the bootstrap diodes. The bootstrap voltages therefore needs to be regulated for the driver circuits. Resistors R_{Zx} , zener diodes D_{Zx} and capacitors C_{Zx} forms zener regulators that provides the driver circuits with regulated 15 V supplies.

To design the bootstrap supply and zener regulators, the energy consumption of all the circuitry connected to the supply is needed. The driver circuit that needs to be powered from the bootstrap supply is shown in Figure 6.12. The 5 V supply is reference to the same ground as the 35 V of the bootstrap supply. Because the eight MOSFETs cannot be switched relative to the ground of this 5 V supply, the outputs of the optic receivers are isolated through an optocoupler-based MOSFET driver, i.e. the VO3150A from Vishay. The isolated ground of the optocoupler is then connected to the source pin of the MOSFET. The isolated side of the optocoupler driver needs to be powered from the 15 V bootstrap supply and zener regulators. The current to switch the MOSFET also needs to come from the bootstrap supply.

To design the gate resistor R_G we use the MOSFETs gate charge vs gate-source voltage characteristics which is obtained from the MOSFETs data sheet. The gate resistor can

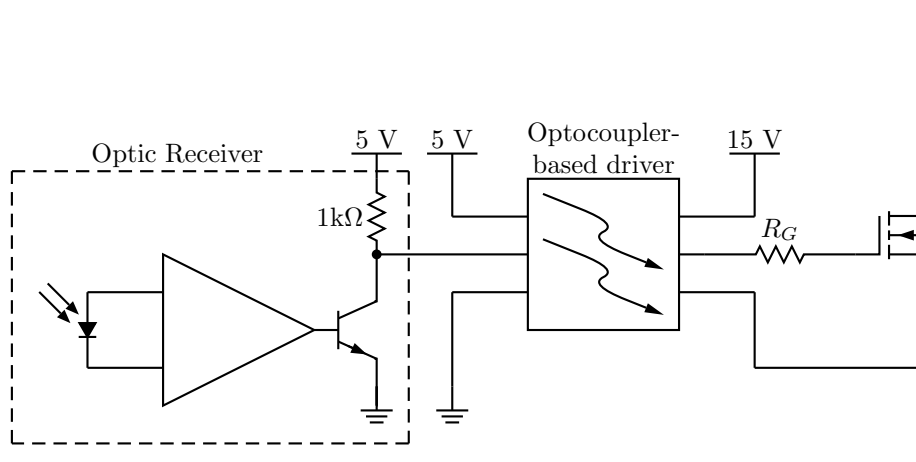


Figure 6.12: Optic receiver and driver circuitry

then be calculated from

$$\begin{aligned}
 R_{gate} &= \frac{V_{gate} - 6.5}{I_{gate}} \\
 &= \frac{15 - 6.5}{0.5} \\
 &\approx 18 \Omega
 \end{aligned} \tag{6.3.1}$$

where V_{gate} and I_{gate} is the output voltage and current of the MOSFET driver. The 6.5 V is obtained from Figure 6.13 as the voltage needed to charge the gate-source capacitance. During the flat part the gate-drain capacitance is charged after which both the gate-source and gate-drain capacitances are charged.

$V_{GS}(V)$

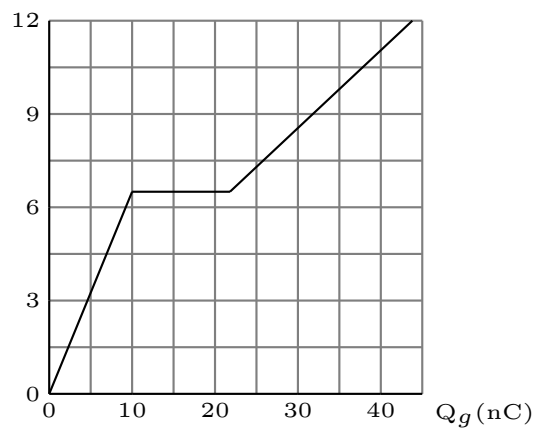


Figure 6.13: Gate charge vs gate-source voltage of *STP20NM60FD*

The energy dissipated in the gate resistor, when the MOSFET is switched, is calculated

in (6.3.2).

$$\begin{aligned}
 E_{RG} &= I_{gate}^2 R_G (t_{on} + t_{off}) \\
 &= 0.5^2 \cdot 18 \cdot (12 + 22) \times 10^{-9} \\
 &= 153 \text{ nJ}
 \end{aligned} \tag{6.3.2}$$

Other energies that are drained from the bootstrap capacitor are those that are absorbed by the driver itself. It consumes a constant 2.5 mA at 15 V and 0.5 A for, respectively, 12 ns and 22 ns when the MOSFET is switched on and off. This gives a total energy consumption of:

$$\begin{aligned}
 E_{driver} &= V_{DD} I_S T_{pre} + V_{DD} I_{PK} (t_{on} + t_{off}) \\
 &= 15 \cdot 2.5 \times 10^{-3} \cdot 12.5 \times 10^{-6} + 15 \cdot 0.5 \cdot (12 + 22) \times 10^{-9} \\
 &= 724 \text{ nJ}
 \end{aligned} \tag{6.3.3}$$

The zener capacitor, C_{Zx} , can be calculated from

$$\begin{aligned}
 E_{R_{gate}} + E_{driver} &= \frac{1}{2} C_Z V_1^2 - \frac{1}{2} C_Z V_2^2 \\
 C_Z &= \frac{E_{R_{gate}} + E_{driver}}{\frac{1}{2} V_1^2 - \frac{1}{2} V_2^2} \\
 &= 60.5 \text{ nF}
 \end{aligned} \tag{6.3.4}$$

allowing for a 1 V drop in its voltage. This capacitance will, however, only be sufficient for the drivers used on the isolation stage. The drivers for the active rectifier will require a bootstrap supply that is capable of powering the driver for half of a 50 Hz cycle. The capacitance should therefore be $\frac{20 \text{ ms}}{25 \mu\text{s}} = 800$ times greater. 100 μF was used.

The 15 V supplies for the MOSFET drivers are regulated with a zener diode regulator. The 35 V input voltage is allowed to drop to 30 V for the top regulator of the bootstrap supply because of the voltage drops across the bootstrap diodes. Assuming a total load current of 10 mA (the sum of the optocoupler's supply and average MOSFET gate current) and a 1 mA quiescent current for the zener diode, the zener resistor can be calculated from

$$\begin{aligned}
 R_Z &= \frac{V_{in(min)} - V_{out}}{I_{RZ}} \\
 &= \frac{30 - 15}{11 \times 10^{-3}} \\
 &\approx 1360 \Omega.
 \end{aligned} \tag{6.3.5}$$

A 0.5 W, 15 V zener diode and 500 mW zener resistor was needed. The bootstrap capacitor

can be calculated from

$$i = C \cdot \frac{dv}{dt}$$

$$11 \times 10^{-3} = C \cdot \frac{1}{25 \times 10^{-6}}$$

$$C = 275 \text{ nF} \quad (6.3.6)$$

assuming the zener regulator consumes a constant 11 mA. Once again the capacitor size will only be sufficient for the driver circuitry of the isolation stage. For the active rectifier the capacitor should again be 800 times greater. 470 μF was used.

6.4 Converter Hardware

Photographs of the built converters are shown in Figures 6.14 and 6.15. Figure 6.14 shows the complete experimental setup. The dual converters are stacked in series with the outputs of their isolation stages connected in parallel at the load. The AC input variac is used to soft-start the system. The digital controller sends the switching signals via optic fibre links to the MOSFET driver boards. Eight measurement boards are visible to take measurements of the seven voltages and the input current. Figure 6.15 shows the active rectifier and isolation stage housed on the same power plane. Each part has its own heat sink and driver board. The transformer and passive rectifier of one of the converters are also indicated.

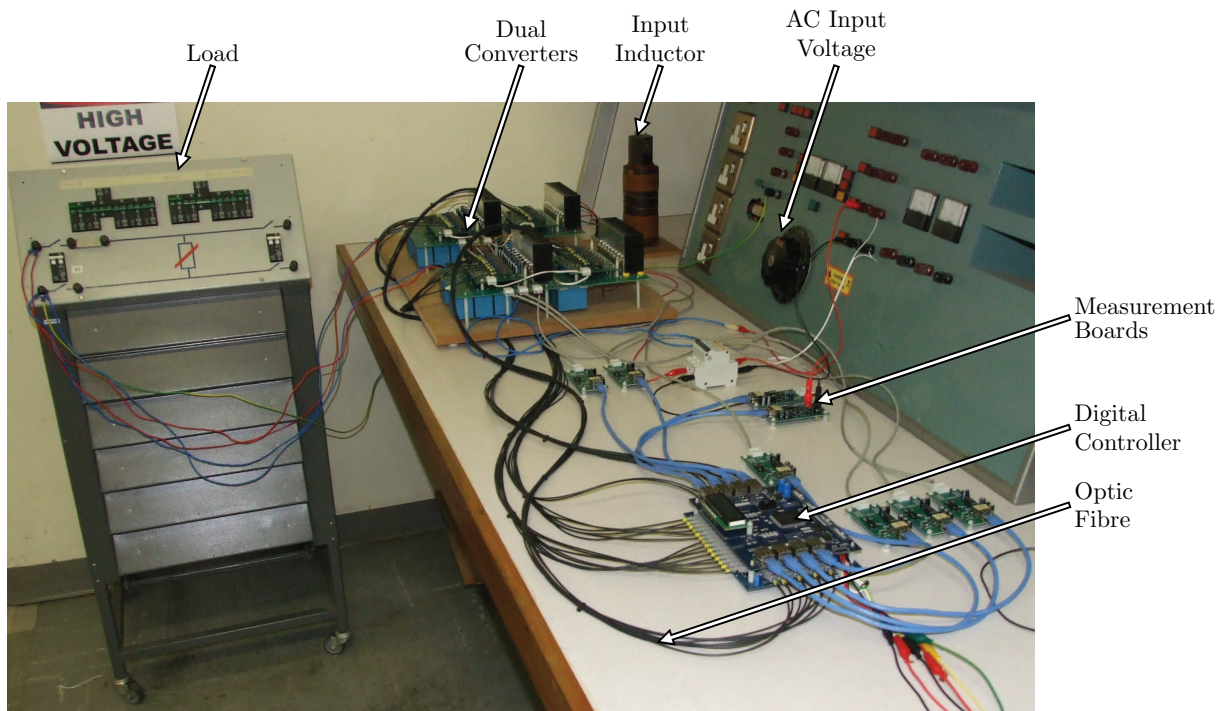


Figure 6.14: Photograph of complete test setup with dual converters.

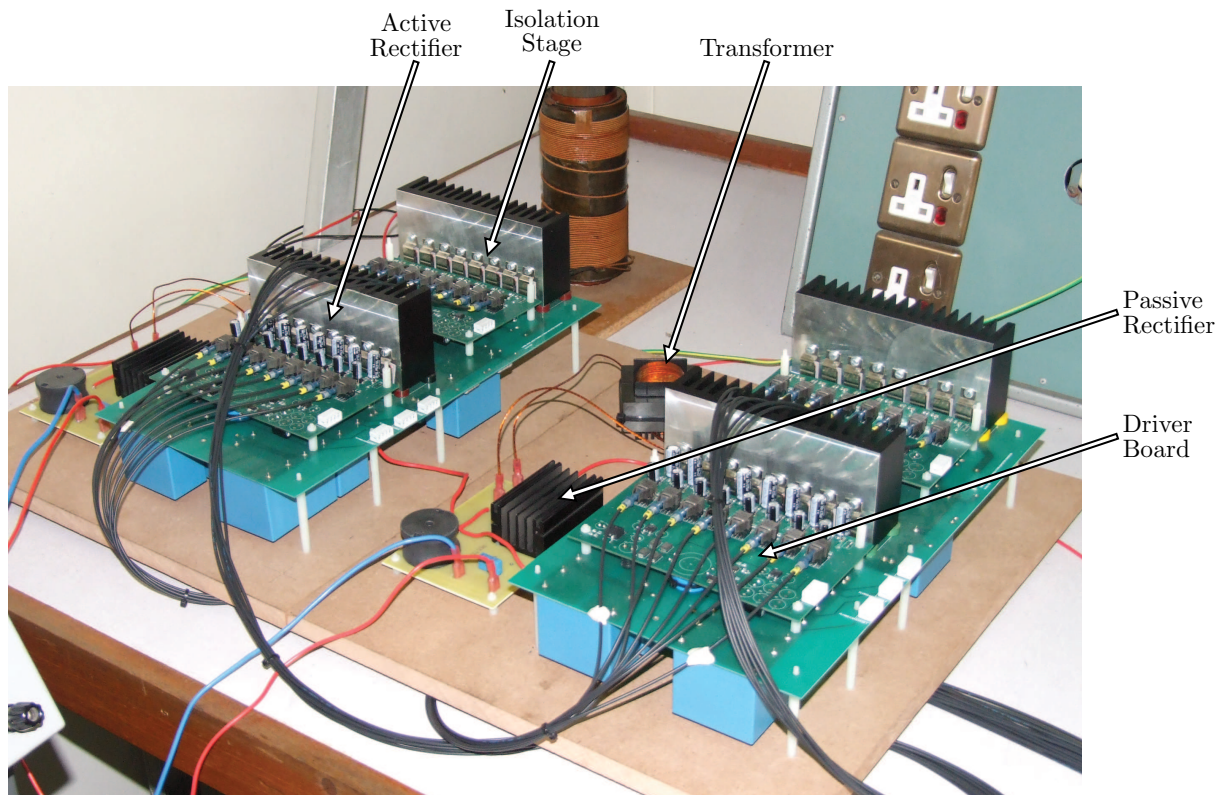


Figure 6.15: Photograph of dual converters.

6.5 Summary

This chapter contained the design of the power electronic converter and support hardware. The converter firstly consisted of the full-bridge, three-level flying-capacitor active rectifier front-end. Some considerations went into choosing the power switches and heat sink. The capacitors and boost inductor were also designed. Secondly, the isolation stage back-end of the converter was designed. It was also a full-bridge, three-level flying-capacitor converter with a high frequency transformer, diode rectifier and passive LC low-pass filter. The supporting hardware included the MOSFET driver circuitry as well as the power supply for these drivers. The drivers consisted of an optic fibre receiver and optocoupler-based MOSFET driver integrated circuit. The power supply for the drivers was based on a bootstrap scheme where each higher level MOSFET driver is powered from the lower driver that is connected to it.

Chapter 7

Controller Design

This chapter describes the design and other considerations of the controller hardware. First, a motivation is given for choosing an FPGA over a DSP as the digital controller that will be used. Next, the measurement circuits together with the analogue-to-digital converter are designed. The measurement circuits use isolated operational amplifiers to isolate the controller hardware from the high voltage measurement side. Lastly, the design of the controller host board is discussed.

The control algorithms that are needed to control the active rectifier and isolation stage is also given. The isolation stage requires a simple PWM switching signal that is generated with a clock counter. The single and dual rectifiers are controlled with model-based predictive control. This consists of predicting the future values for voltages and currents for every possible switching state of the converter. The possibilities are then evaluated with a cost function to choose the best control action. To control the single active rectifier, 16 switching states need to be evaluated. For the dual converter this becomes 256 – an impossible number of calculations to do in real-time. Three control algorithms are proposed to reduce the number of calculations to a realistic amount.

Next, the predictive control algorithms are incorporated into a double-loop control scheme to add voltage regulation for the DC bus of each converter. The outer loop of the scheme produces the input current reference which is in-phase with the input voltage. This will let the active rectifier operate at unity power factor. The current reference is then used by the predictive controller to control the input current and regulate the flying capacitor voltages.

Lastly, an extract of the control software is given to illustrate the organisation of the double-loop controller with its voltage controller and predictive algorithm.

7.1 FPGA vs DSP

Predictive control, as mentioned before, is computationally intensive. This is the main factor to take into account when deciding on the type of controller to be used.

A DSP-based controller has the benefit of built-in analogue-to-digital converters (ADC) and pulse-width-modulators (PWM) which are necessary in controlling the converters. The drawback of the micro controller, however, is that all its instructions are executed sequentially. This poses a problem when the time taken to compute a new switching state should ideally be zero.

An FPGA can execute multiple instructions in parallel due to its logic make-up. A comparison between a 20 MHz dsPIC30F4012 and a Cyclone III FPGA, also with a 20 MHz clock, was done. A section of instructions containing calculations similar to that of predictive control were implemented on both the DSP and FPGA. The DSP took in the order of milliseconds to complete the calculations, while the FPGA could compute the same answer in nanoseconds. This motivates the use of the FPGA solely on its computational superiority over a DSP.

The disadvantage of using an FPGA, however, is the fact that it does not contain built-in ADCs or PWM modules. An external ADC should be added that can convert an analogue input signal and output the result as a digital stream that can be read by the FPGA. The FPGA and chosen ADC hardware is shown in Figure 7.1. The interfaces between the ADC and the measurement boards, the FPGA and the ADC, and the FPGA and the optic fibre transmitters are also shown.

7.2 Measurement Circuits

The series stack of two converters requires eight measurements to be taken. These include the input current, input voltage, two bus voltages and four flying capacitor voltages. The author of [96] proposed using a Discrete Kalman Filter to estimate some of the states of a flying-capacitor converter to reduce the number of measurements. As the focus of this project is the predictive control of the converters, it was decided to measure the states instead of estimating them.

When taking measurements, it is important to take into account the fact that the ground potential at which the measurement is taken can differ from the ground potential of the ADC. To be able to use only one ADC to take all the different measurements, it was decided to isolate the measurements from the ADC. By using the ISO124 isolation operational amplifier from Texas Instruments the ground connections between the measurement

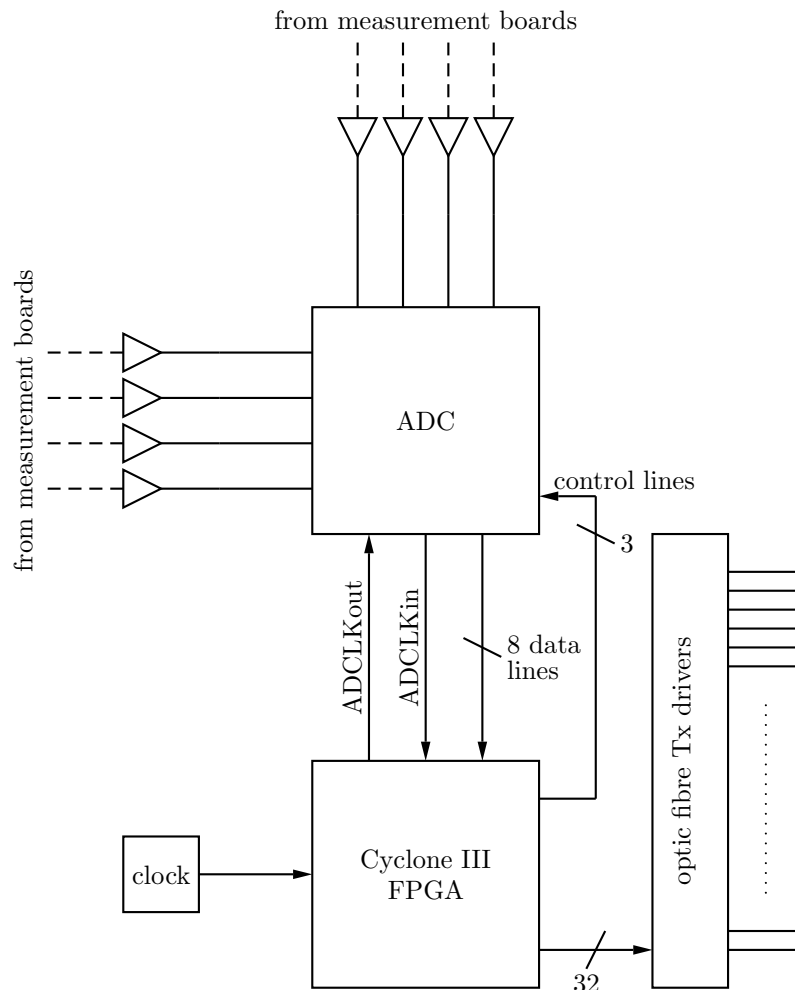


Figure 7.1: Controller hardware.

devices and the ADC can be kept apart. This is done for the voltage as well as current measurements.

7.2.1 Voltage Measurement

The predictive control algorithm requires that seven voltages be measured for the dual active rectifier:

1. Two 600 VDC bus voltages
2. Four 300 VDC flying capacitor voltages
3. One 1000 VAC_{peak} input voltage

The circuit to measure the different voltages is shown in Figure 7.2. Resistors R_a and R_b are used to differentially scale the input voltage [97]. An instrumentation amplifier, an INA129 from Texas Instruments, is used to buffer the differential voltage and output a

single-ended voltage to the isolation op-amp. The gain of the instrumentation amplifier can be programmed with a R_G resistor, but by leaving the terminals unconnected, the gain is set to unity. The isolation op-amp also has a unity gain. The output of the isolation op-amp is converted to a differential signal to lessen the effect of noise picked up by the transmission cable taking the signal to the ADC on the board hosting the FPGA.

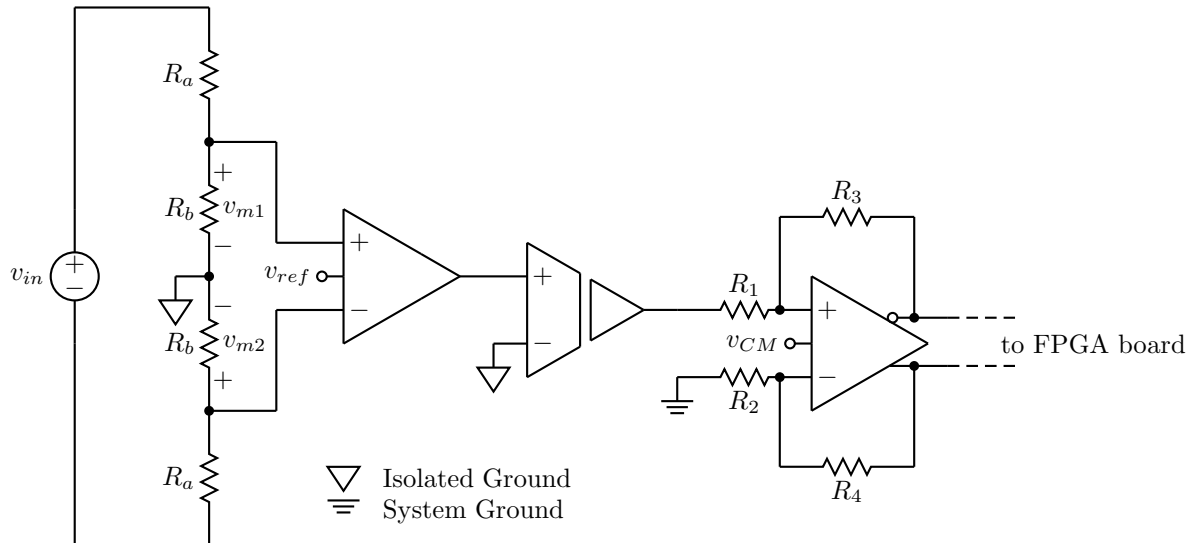


Figure 7.2: Voltage measurement circuit

To measure the 600 VDC bus voltages, resistors R_a and R_b are used to scale the voltage in order for the output of the isolation op-amp to be a maximum of 1 V. The 1 V maximum is because of the input limitations of the ADC. Choosing the measurable range to be 800 VDC leaves an adequate safety margin.

The differential voltage is defined as

$$v_d = v_{m1} - v_{m2} \quad (7.2.1)$$

and the common mode voltage as

$$v_{cm} = \frac{v_{m1} + v_{m2}}{2}. \quad (7.2.2)$$

When

$$v_{m1} = \frac{v_{in}}{2} \quad (7.2.3)$$

and

$$v_{m2} = -\frac{v_{in}}{2} \quad (7.2.4)$$

the differential voltage

$$v_d = v_{in}. \quad (7.2.5)$$

By scaling v_{m1} and v_{m2} with R_a and R_b we find

$$v_d = v_{in} \cdot \left(\frac{R_b}{R_a + R_b} \right). \quad (7.2.6)$$

The output of the isolation op-amp is therefore a scaled version of the input voltage. To convert the voltage to a differential signal a fully differential op-amp, the THS4521 from Texas Instruments, is used. It is also implemented with a unity gain.

To keep within the voltage ratings of the divider resistors each R_a is chosen to be eight resistors in series. Therefore, for v_{in} equal to 800 VDC,

$$v_{in} \cdot \left(\frac{R_b}{8 \times R_a + R_b} \right) = 1. \quad (7.2.7)$$

For the sinusoidal input voltage measurement the peak of the voltage should be scaled down to 1 V. The trough of the sinus wave will therefore be scaled to -1 V which gives a $2V_{pp}$ range.

The divider resistor values for taking the different voltage measurements are shown in Table 7.1. Similar safety factors for both the 300 VDC and 1000 VAC measurements were used.

Table 7.1: Component values for voltage measurements

	Flying capacitor	Bus voltage	Input voltage
nominal voltage	300 VDC	600 VDC	1000 VAC _{peak}
max voltage	400 VDC	800 VDC	1300 VAC _{peak}
R_a	$4 \times 120 \text{ k}\Omega$	$8 \times 120 \text{ k}\Omega$	$13 \times 120 \text{ k}\Omega$
R_b	1.2 k Ω	1.2 k Ω	1.2 k Ω
R_1	10 k Ω	10 k Ω	10 k Ω
R_2	10 k Ω	10 k Ω	10 k Ω
R_3	10 k Ω	10 k Ω	10 k Ω
R_4	10 k Ω	10 k Ω	10 k Ω
v_{ref}	isolated ground	isolated ground	isolated ground
v_{CM}	2.5 V	2.5 V	2.5 V

Figure 7.3 shows a photograph of a voltage measurement board. The divider resistors can be changed to measure the different voltages needed for this project. The isolated power supply is to power the isolated input side of the isolated op-amp, as well as the instrumentation amplifier.

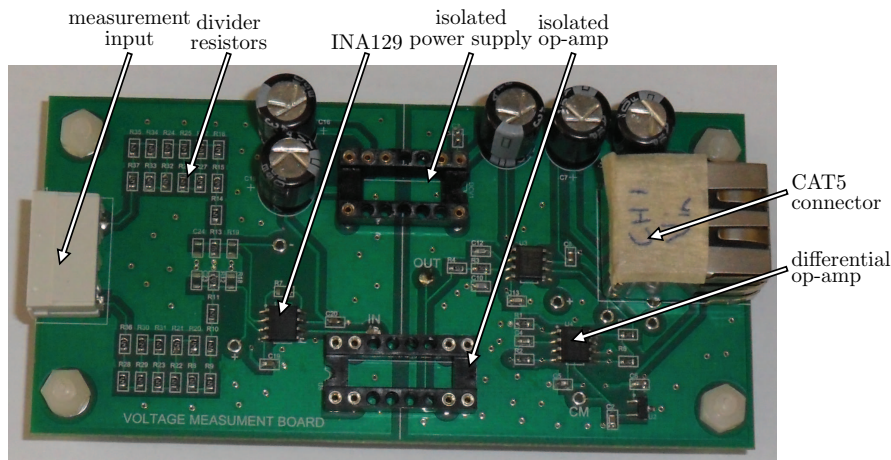


Figure 7.3: Voltage measurement PCB

7.2.2 Current Measurement

Two main methods for measuring currents are hall-effect sensors and using a series resistor. The small amount of current, which the converters require, makes the use of a hall-effect sensor inaccurate. The large input voltage at which the converters operate will make the voltage drop across a series resistor negligibly small. It was therefore decided to use a series resistor and measure the voltage across it.

By using the same circuit as in Figure 7.2 with resistors R_a a short circuit, the differential voltage across the two R_b resistors will be a scaled version of the input current. By using $50\text{ m}\Omega$ resistors for R_b the range of the input current is $10 A_{peak}$.

Figure 7.4 shows a photograph of the current measurement board. The isolated power supply is to power the isolated input side of the isolated op-amp, as well as the instrumentation amplifier.

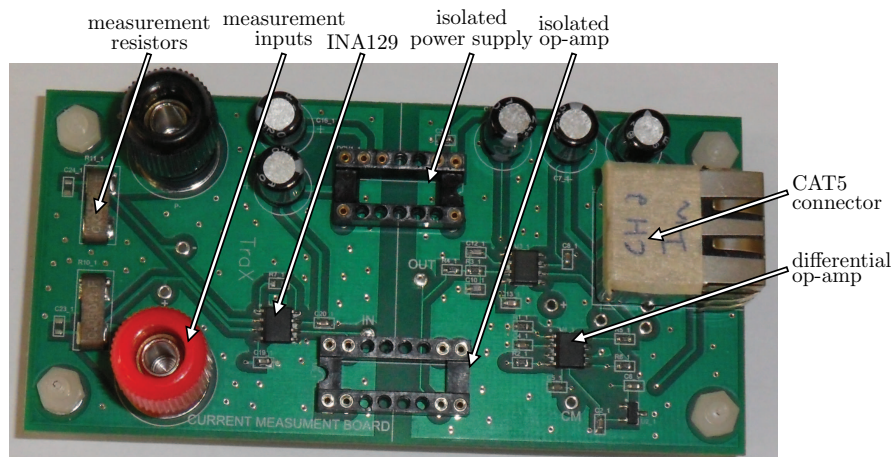


Figure 7.4: Current measurement PCB

7.3 Analogue-to-Digital Converter

The differential measurement signal received by the FPGA host board needs to be buffered and then converted to a digital signal. The buffer and ADC is shown in Figure 7.5. The ADS5272, 12-bit, eight channel ADC from Texas Instruments is used. The ADC requires five control signals from the FPGA, as well as the sampling clock signal $ADCLKout$. The ADC buffers this clock and returns a clock signal $ADCLKin$ that frames the data that is serially output via eight pairs of differential data lines.

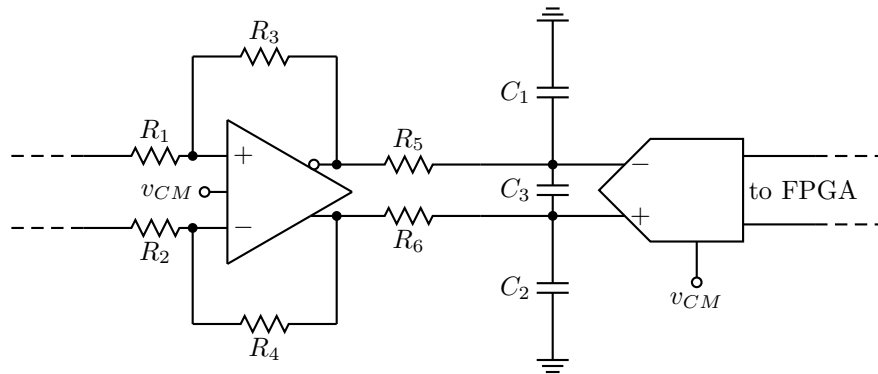


Figure 7.5: Differential input buffer and analogue-to-digital converter

The ADC can operate with a maximum of $2.03 V_{pp}$ differential analogue input signal with a common mode voltage of 1.45 V. The differential buffer should have unity gain and therefore $R_1 = R_2 = R_3 = R_4 = 10 \text{ k}\Omega$.

The combination of R_5 , R_6 , C_1 , C_2 and C_3 forms a low-pass filter. The data sheet of the ADC's prescribed 24Ω for the resistors, 1 nF for C_1 and C_2 , and 10 nF for C_3 . The common mode voltage requirements of the buffer's output is met by supplying the differential op-amp with the 1.45 V reference output from the ADC.

7.4 Switching Signals

The problem of taking the measurements at different voltage levels is extended to the switching signals. The series stacked power switches cannot all be switched relative to the ground plane of the FPGA host board and therefore the switching signals also needs to be isolated. Optic fibre was chosen to carry the signals to the respective switches as this will make the signals immune to interference and also provide the required isolation.

The FPGA cannot provide the current necessary to power the optical transmitters. Therefore, the driver circuit in Figure 7.6 is used. The HFBR-15X1 optic transmitters from Agilent are driven by SN75451B AND-gates.

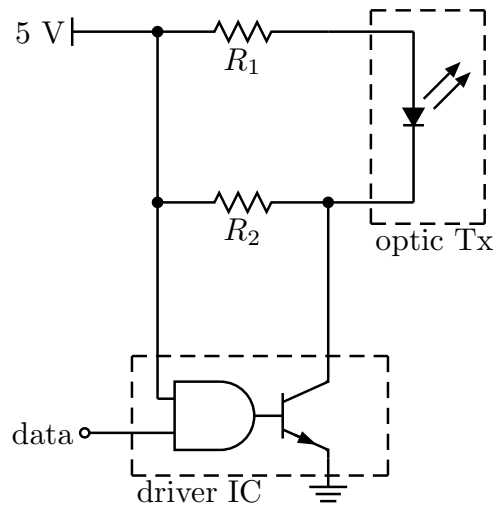


Figure 7.6: Optic fibre transmitter and driver for sending switching signals

The optic transmitter LED has a forward voltage of around 2 V at 60 mA. R_1 is therefore chosen to be $56\ \Omega$ and the pull-up resistor R_2 to be $1\ \text{k}\Omega$.

The optic fibre transmitters host board is shown in Figure 7.7.

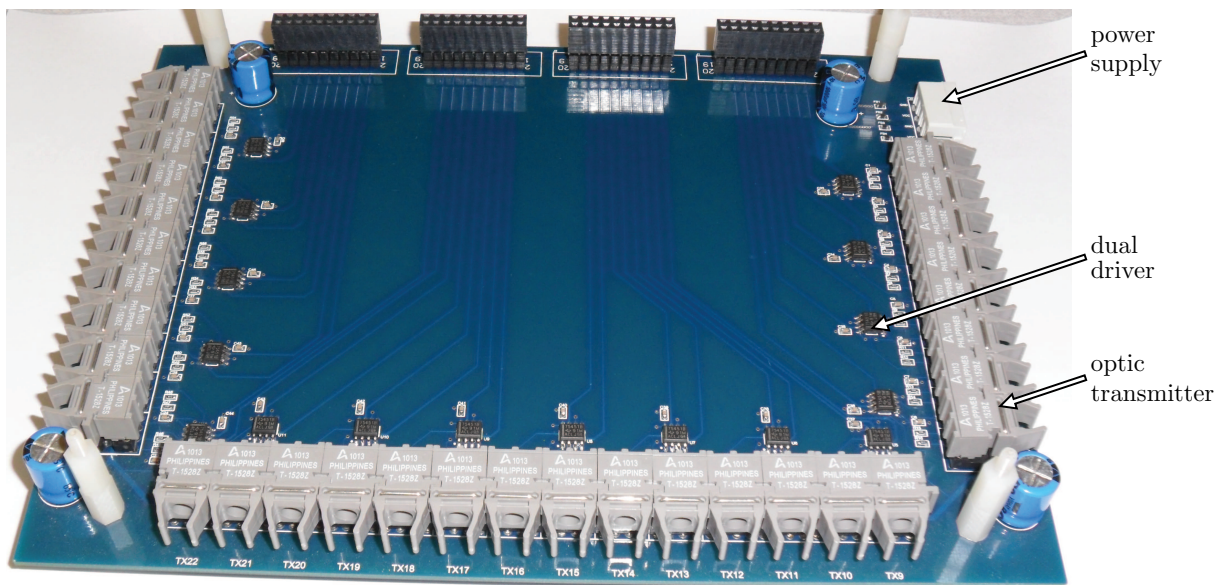


Figure 7.7: Optic fibre transmitters PCB

7.5 Controller Hardware

The FPGA board is shown in Figure 7.8. The photograph shows the FPGA with the location of the ADC indicated. The ADC is located on the underside of the board. The FPGA board sits atop the printed circuit board that houses the optic fibre transmitters.

The label *Switching Signals* indicates one of the four connection points between the two boards. The eight CAT5 connectors are used to connect to the measurement boards.

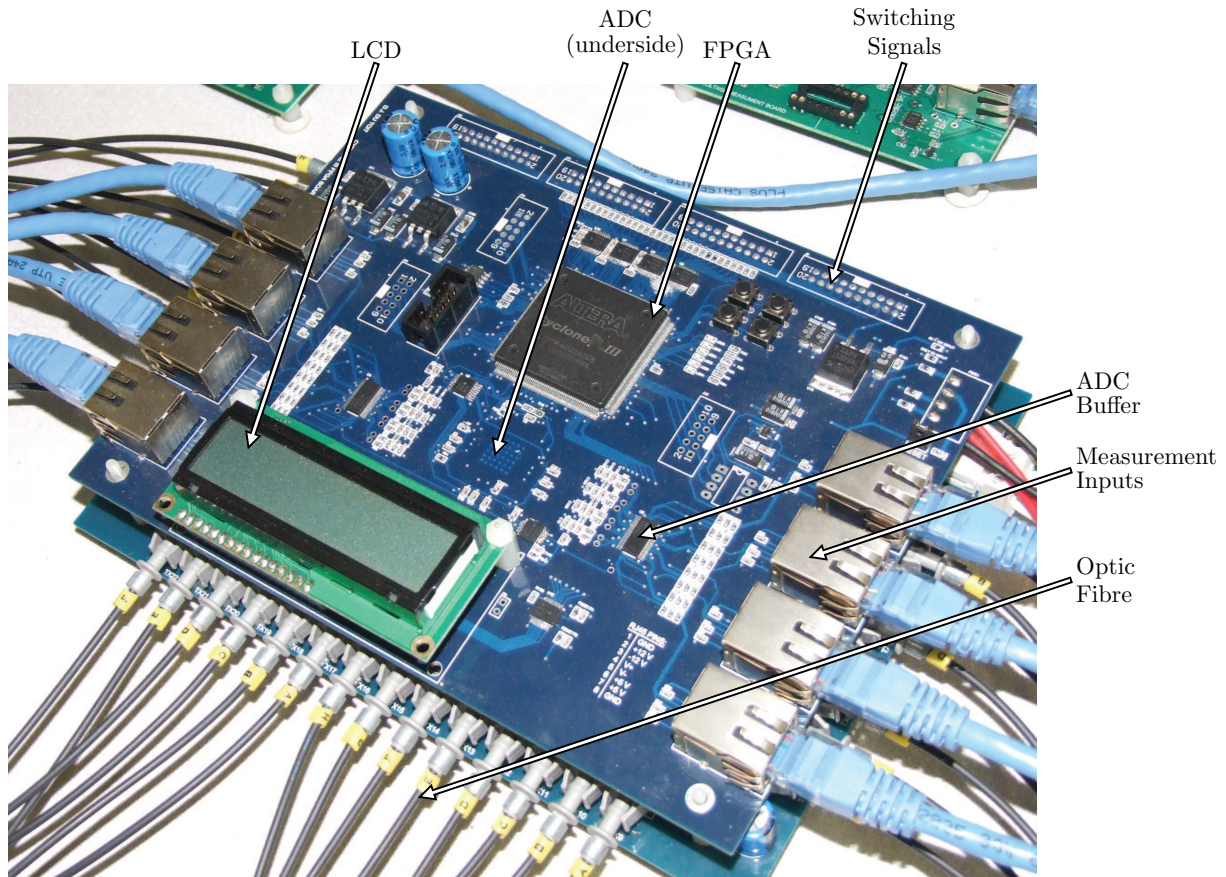


Figure 7.8: Photograph of FPGA board.

7.5.1 FPGA Attributes

The Cyclone III EP3C40Q240 FPGA from Altera was used. It consists of [98]:

- 39 600 logic elements
- 1 134 kilo-bits of memory
- 126 multipliers
- 4 phase-locked loops (PLLs)
- 128 single-ended IOs
- 13 differential IOs

The single-ended and differential IOs are divided into eight IO banks. Model-based predictive control requires large amounts of calculations to do all of its predictions and evaluate the cost functions. For this reason an FPGA with many logic elements, memory and multipliers was chosen. Also, differential input-outputs (IOs) were needed for the ADC.

7.5.2 Low-Voltage Differential Signals

Low-voltage differential signalling (LVDS) is an IO standard for high-speed, low voltage swing, general purpose differential communication [99]. The ADC sends its data and clock signals to the FPGA with this LVDS. The connection, as shown in Figure 7.9, consists of two traces with opposite polarities. The differential signals have a common mode voltage of 1.2 V and the nominal output voltages are either 1.0 V or 1.4 V. If a logic '1' needs to be transmitted, the positive output will equal 1.4 V with the negative 1.0 V. The receiver will subtract the negative trace from the positive. Because the resulting voltage is positive it will be translated to a logic '1'. LVDS receivers require a $100\ \Omega$ termination resistor between the positive and negative terminals.

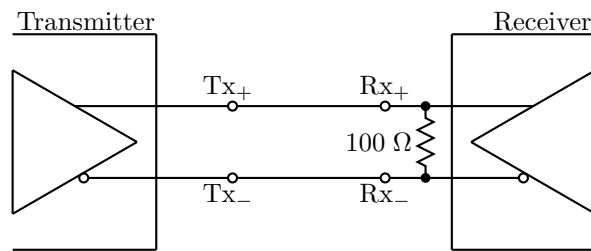


Figure 7.9: Low-voltage differential signalling.

7.5.3 Power Management

Different supply voltages are required by the various components on the FPGA host board. The FPGA itself requires 1.2 V for its internal logic (VCCINT) and digital circuits of the phase-locked loops (VCCPLL). Furthermore, 2.5 V is required by the analogue circuits of the phase-locked loops (VCCA) and the IO banks on which the LVDS IOs are used (VCCIO). The remaining IO banks are powered by 3.3 V (VCCIO).

The ADC only requires 3.3 V. Its control signals interface with an FPGA IO bank which operates at 2.5 V. The control signals are therefore level shifted between 3.3 V and 2.5 V. The differential op-amp buffers between the measurement board and the ADC are directly powered from the 5 V host board supply.

The FPGA host board is supplied by ± 12 V and 5 V. The ± 12 V is fed to the measurement boards through the CAT5 connectors to power the isolated op-amps. The 5 V supply is

regulated down to provide the 1.2 V, 2.5 V and 3.3 V. Figure 7.10 shows the regulation scheme used.

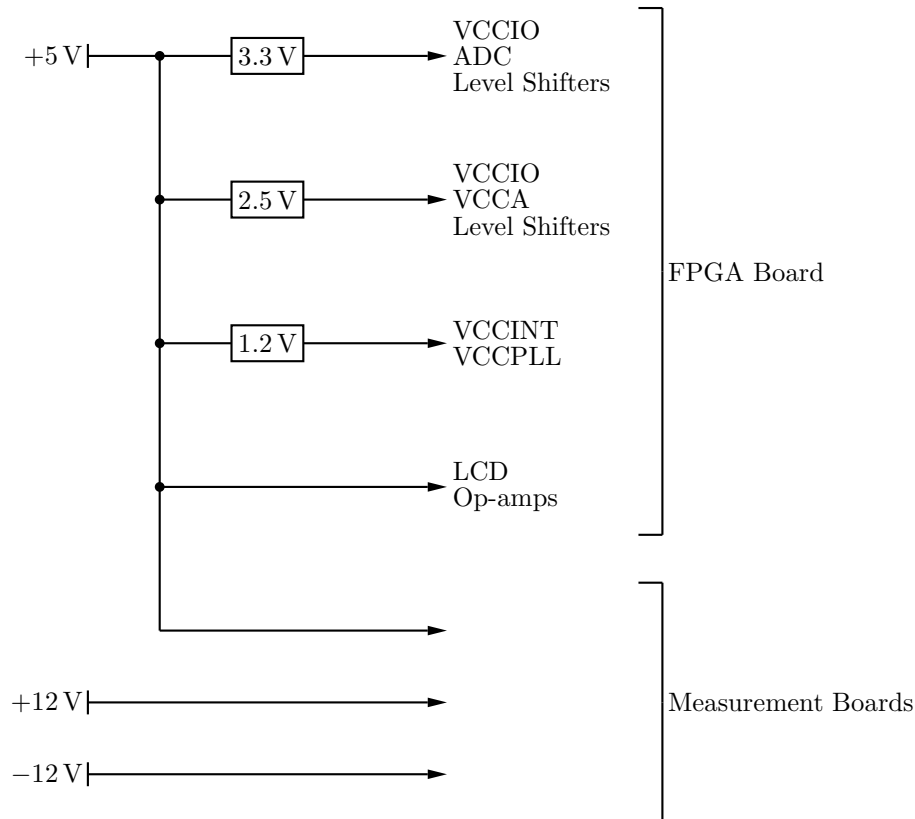


Figure 7.10: Power distribution for FPGA host board.

7.5.4 Voltage Level Shifters

The use of the LVDS communication forces some of the IO banks of the FPGA to use 2.5 V. Push buttons and LEDs can operated from 2.5 V, but the control signals for the LCD and ADC need to be 5 V and 3.3 V, respectively. The IO banks that need not be powered by 2.5 V are supplied with 3.3 V, but they are used for signalling the optic fibre transmitters. These transmitters, on the other hand, requires 5 V signals. Voltage level shifters are therefore added between the FPGA and the other devices to translate the 2.5 V and 3.3 V signals to the correct voltage levels. The TXS010x series of bi-directional level shifters from Texas Instruments are used. Figure 7.11 shows the level shifting setup for the ADC.

7.5.5 LCD Interface

The Powertip PC1602D is used for user feedback. Voltage and current measurements are displayed and error codes during converter fault conditions tell the user what went wrong.

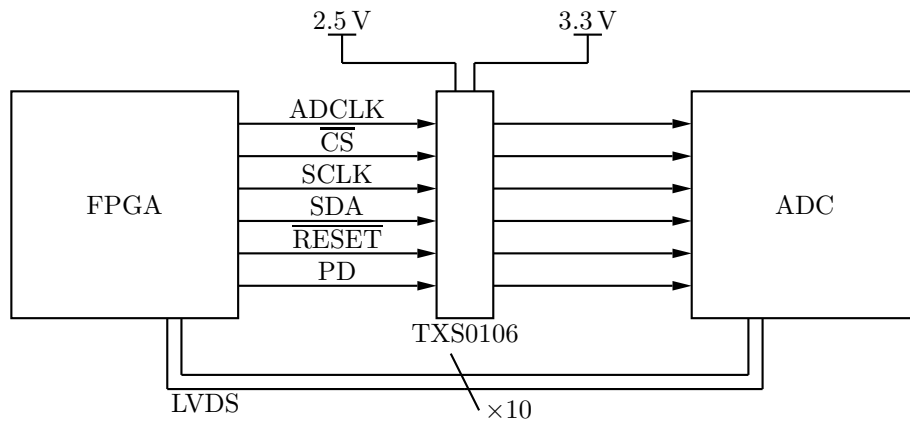


Figure 7.11: Digital connections of FPGA and ADC through voltage level shifter.

The LCD control module requires either eight or four data lines and three control lines. The module can operate in an eight bit mode where all eight bits of every character are transmitted simultaneously. In its four bit mode only four data lines are required, but the character data has to be transmitted one half at a time.

The voltage level of all the FPGA signals to the LCD module is 3.3V. Because of this a voltage level shifter is added between the 5V LCD module and the 3.3V bank of the FPGA. The connections are shown in Figure 7.12.

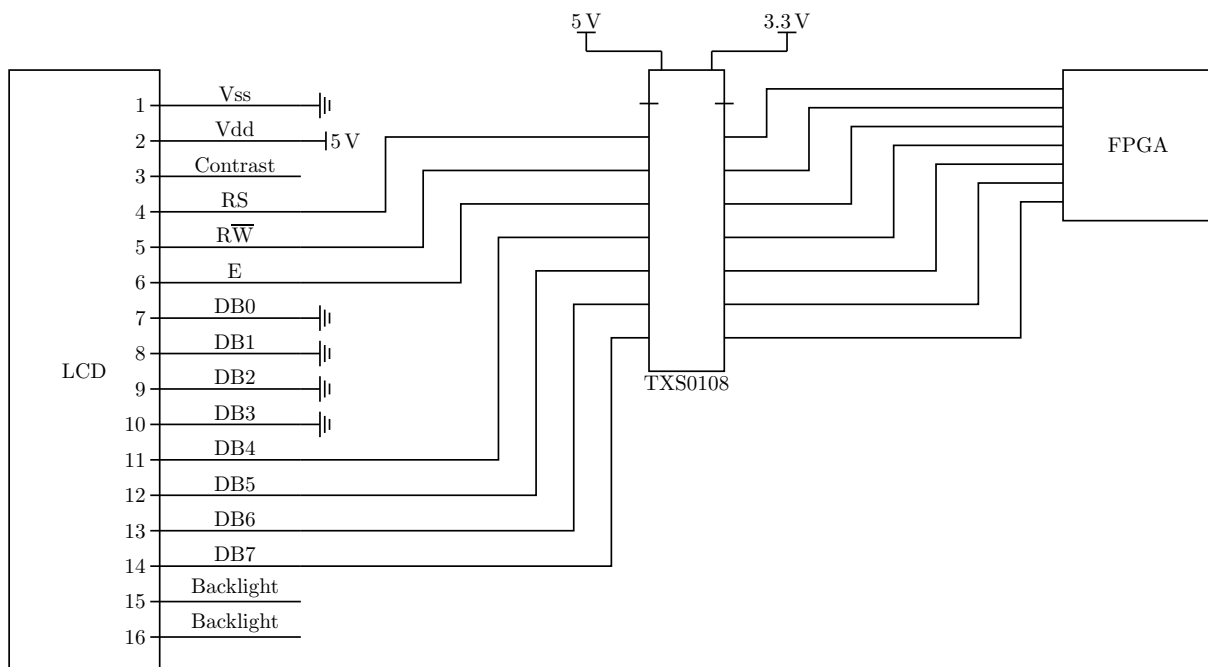


Figure 7.12: Digital connections of FPGA and LCD module through voltage level shifter.

7.6 Control Algorithms

Three sets of control algorithms are needed. One is to control the isolation stage by providing the switching signals for the eight MOSFETs. The other two algorithms are to control a single active rectifier, as well as to control a series stack of two rectifiers.

7.6.1 Isolation Stage

The isolation stage is operated at a fixed duty cycle of 45% at 40 kHz. The input clock of 20 MHz is used as a counter to provide the MOSFETs with their respective switching signals. The 20 MHz clock has a 50 ns period while the 40 kHz switching signal has a 25 μ s period. The 25 μ s is divided into two parts as shown in Figure 7.13. This means that the counter will have to count up to 255 for the states *A* and *C* and up to 25 for the off-states.

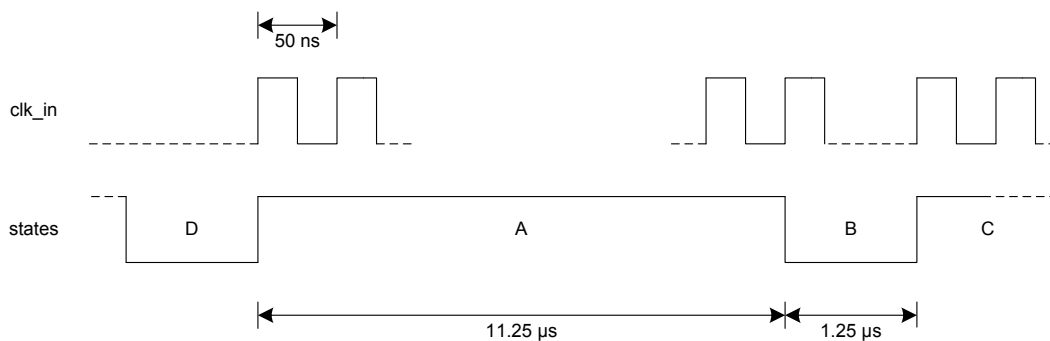


Figure 7.13: Relationship between the input clock and converter states

7.6.2 Cost Function Weights

The weights of the cost functions need to be chosen in such a manner that the controller can control all the states. If one weight is too large, too much control effort will go into controlling that one state that the others will not follow their references.

As a guideline for determining the weights, one could start by setting all the weights equal to 1. But, for the control algorithms in this chapter, setting the weight of the current term in the cost function to 1 the current could not be controlled. This is due to the fact that, for equal weights, an entity with magnitude 4 (such as the current) should now be controlled as hard as another entity with magnitude 600 (such as the bus voltage). For the current error to have a significant effect on the cost of the predicted switching state, it would have to be a much bigger error percentage wise than with the bus voltage. To overcome this problem the weight of the current term was initially set to 10 and then adapted to find the best compromise between the current following its reference and the voltages being balanced.

7.6.3 Single Rectifier

To control the single active rectifier in Figure 7.14, the 16 possible switching states are used in the predictions. Sixteen cost functions are evaluated to get the optimal switching state. Algorithm 7.1 calculates the different predictions and evaluates the cost functions. When the optimal state is known, the switching signals can be produced. The state space models in this algorithm is of fourth-order¹ and the cost function that is used is shown in (7.6.1). The cost function V of (5.4.4) is redefined and now called $cost$. The weighting factors Q has components α , initially with an unknown value, and ones for the other two terms. The value of α was experimentally determined by following the process described in Section 7.6.2 and equals 4.

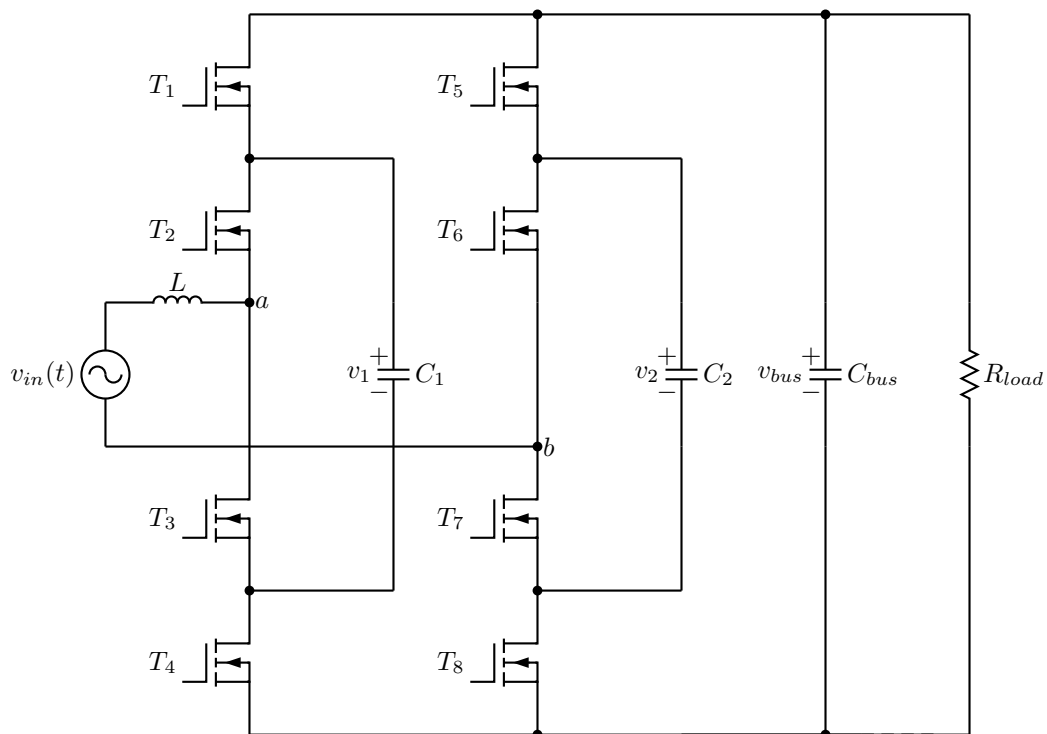


Figure 7.14: Single active rectifier with resistive load.

$$\begin{aligned}
 cost = & \alpha \cdot |i_{L(ref)} - i_L(k+1)| \\
 & + \left| \frac{1}{2} v_{bus}(k+1) - v_1(k+1) \right| + \left| \frac{1}{2} v_{bus}(k+1) - v_2(k+1) \right|
 \end{aligned} \tag{7.6.1}$$

7.6.4 Dual Rectifier

By stacking N converters in series, the total number of switching states becomes 16^N . Using only two converters, as shown in Figure 7.15, gives 256 possible switching states.

¹see section B.3, Converter State-Space Models

Algorithm 7.1 Predictive control algorithm to control a single converter.

$t = t_0$

$state_save \leftarrow 0$

$cost_save \leftarrow \infty$

for $state = 1$ **to** 16 **do**

do predictions: $\mathbf{x}(k+1) = T_{pre}(\mathbf{A}\mathbf{x}(k) + \mathbf{B}v_{in}(k)) + \mathbf{x}(k)$

evaluate cost function

if $cost < cost_save$ **then**

$cost_save \leftarrow cost$

$state_save \leftarrow state$

end if

end for

wait for $t_1 = t_0 + T_{pre}$ and repeat

The prediction algorithm will therefore have to predict 256 sets of states before evaluating 256 cost functions to obtain the optimal switching state. Performing this amount of predictions is computationally expensive and therefore alternative methods to control the two converters need to be found. The algorithm to control the two converters using the full 256 possible switching states is shown in Algorithm 7.2. Three alternatives that require less computational effort are shown in Algorithms 7.3, 7.4 and 7.5.

7.6.4.1 Control Using 256 Switching States

Algorithm 7.2 uses a seventh-order² model obtained by combining the models of the two converters. The model contains the input current, four flying capacitor voltages and the two bus voltages as states. Without taking the cost function evaluations into account the 256 possible switching states requires a total of 2560 multiplications. Added to this number of calculations are those needed to evaluate the cost functions. It is clear that *Control 256* is not a feasible solution for an on-line control algorithm.

The cost function used in Algorithm 7.2 is shown in (7.6.2). The values for α and β were again experimentally determined by following the process described in Section 7.6.2 and equals 10 and 1, respectively. Also, α , β and all the magnitude one coefficients are the elements of the the weighting factor Q .

²see section B.3, Converter State-Space Models

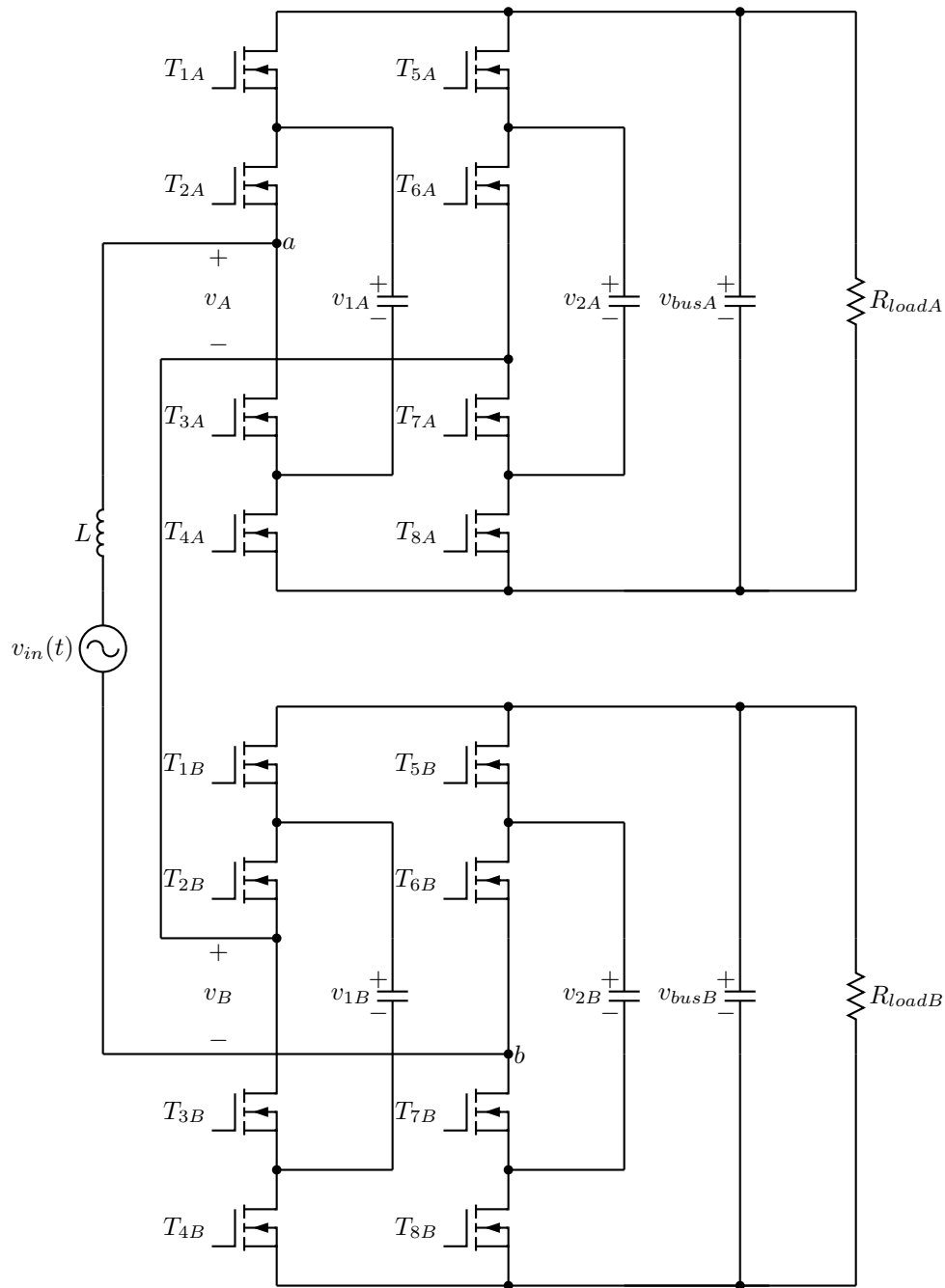


Figure 7.15: Dual active rectifier with resistive loads.

$$\begin{aligned}
 cost = & \alpha \cdot |i_{L(ref)} - i_L(k+1)| + \beta \cdot |v_{busA}(k+1) - v_{busB}(k+1)| \\
 & + \left| \frac{1}{2} v_{busA}(k+1) - v_{1A}(k+1) \right| + \left| \frac{1}{2} v_{busA}(k+1) - v_{2A}(k+1) \right| \\
 & + \left| \frac{1}{2} v_{busB}(k+1) - v_{1B}(k+1) \right| + \left| \frac{1}{2} v_{busB}(k+1) - v_{2B}(k+1) \right|
 \end{aligned} \tag{7.6.2}$$

Algorithm 7.2 *Control 256*

 $t = t_0$ $state_save \leftarrow 0$ $cost_save \leftarrow \infty$ **for** $state = 1$ **to** 256 **do**do predictions: $\mathbf{x}(k+1) = T_{pre}(\mathbf{A}\mathbf{x}(k) + \mathbf{B}v_{in}(k)) + \mathbf{x}(k)$

evaluate cost function

if $cost < cost_save$ **then** $cost_save \leftarrow cost$ $state_save \leftarrow state$ **end if****end for**wait for $t_1 = t_0 + T_{pre}$ and repeat

7.6.4.2 Control Using 16 Switching States

An alternative to Algorithm 7.2 needed to be found to reduce the number of calculations required. Algorithm 7.3 shows one where the two converters are only allowed to exist in the same switching state. This reduces the amount of possible switching states to 16 while still using the same seventh-order³ models as Algorithm 7.2 did. The number of multiplications is therefore reduced to 160. *Control 16* uses the same cost function as *Control 256* does. It is shown in (7.6.2) where the α and β weights also equals 10 and 1, respectively.

7.6.4.3 Control Using 32 Switching States

Algorithm 7.4 lets both converters exist in different switching states. Fourth-order⁴ models for the two converters are used and the input voltage is assumed to divide equally between the two converters. When evaluating the cost function for converter A, the predicted states of converter B is assumed to be measured values at time k instead of the predicted values of time $k+1$. The cost function of converter B can, however, use the predicted values of converter B. The cost functions used are shown in (7.6.3) and (7.6.4). The α and β weights in the cost function equals 10 and 2, respectively. The algorithm requires 96 multiplications for the predictions.

³see section B.3, Converter State-Space Models⁴see section B.3, Converter State-Space Models

Algorithm 7.3 *Control 16*

 $t = t_0$ $state_save \leftarrow 0$ $cost_save \leftarrow \infty$ **for** $state = 1$ **to** 16 **do**do predictions: $\mathbf{x}(k+1) = T_{pre}(\mathbf{A}\mathbf{x}(k) + \mathbf{B}v_{in}(k)) + \mathbf{x}(k)$

evaluate cost function

if $cost < cost_save$ **then** $cost_save \leftarrow cost$ $state_save \leftarrow state$ **end if****end for**wait for $t_1 = t_0 + T_{pre}$ and repeat

$$\begin{aligned}
costA = & \alpha \cdot |i_{L(ref)} - i_L(k+1)| + \beta \cdot |v_{busA}(k+1) - v_{busB}(k)| \\
& + \left| \frac{1}{2} v_{busA}(k+1) - v_{1A}(k+1) \right| + \left| \frac{1}{2} v_{busA}(k+1) - v_{2A}(k+1) \right| \quad (7.6.3)
\end{aligned}$$

$$\begin{aligned}
costB = & \alpha \cdot |i_{L(ref)} - i_L(k+1)| + \beta \cdot |v_{busB}(k+1) - v_{busA}(k+1)| \\
& + \left| \frac{1}{2} v_{busB}(k+1) - v_{1B}(k+1) \right| + \left| \frac{1}{2} v_{busB}(k+1) - v_{2B}(k+1) \right| \quad (7.6.4)
\end{aligned}$$

7.6.4.4 Control Using 16 Interleaved Switching States

Algorithm 7.5 approximates *Control 256*, but with a reduction in the instantaneous number of calculations needed. Its cost functions are shown in (7.6.5) and (7.6.6) with α and β equalling 4 and 1, respectively. It does this by interleaving the predictions of the two converters. At time t_0 we know the switching state of converter B and therefore we know its terminal voltage. The whole system can now be simplified to one converter (converter A) with the supply voltage equal to the real supply voltage minus the terminal voltage of converter B. The future state values for the sixteen switching states of converter A are predicted and the cost functions are evaluated to obtain the new switching state for converter A. When $\frac{T_{pre}}{2}$ seconds have passed the predictions of converter B can be done. The terminal voltage of converter A is now known. The algorithm uses fourth-order models⁵ and requires 48 multiplications for one set of predictions.

⁵see section B.3, Converter State-Space Models

Algorithm 7.4 *Control 32*

 $t = t_0$
 $stateA_save \leftarrow 0$ $costA_save \leftarrow \infty$ $stateB_save \leftarrow 0$ $costB_save \leftarrow \infty$ **for** $state = 1$ **to** 16 **do**do predictions for converter A: $\mathbf{x}(k+1) = T_{pre}(\mathbf{A}\mathbf{x}(k) + \frac{1}{2}\mathbf{B}v_{in}(k)) + \mathbf{x}(k)$

evaluate cost function A

if $cost < costA_save$ **then** $costA_save \leftarrow cost$ $stateA_save \leftarrow state$ **end if**do predictions for converter B: $\mathbf{x}(k+1) = T_{pre}(\mathbf{A}\mathbf{x}(k) + \frac{1}{2}\mathbf{B}v_{in}(k)) + \mathbf{x}(k)$

evaluate cost function B

if $cost < costB_save$ **then** $costB_save \leftarrow cost$ $stateB_save \leftarrow state$ **end if****end for**wait for $t_1 = t_0 + T_{pre}$ and repeat

$$\begin{aligned}
costA = & \alpha \cdot |i_{L(ref)} - i_L(k+1)| + \beta \cdot |v_{busA}(k+1) - v_{busB}(k)| \\
& + \left| \frac{1}{2} v_{busA}(k+1) - v_{1A}(k+1) \right| + \left| \frac{1}{2} v_{busA}(k+1) - v_{2A}(k+1) \right| \quad (7.6.5)
\end{aligned}$$

$$\begin{aligned}
costB = & \alpha \cdot |i_{L(ref)} - i_L(k+1)| + \beta \cdot |v_{busB}(k+1) - v_{busA}(k)| \\
& + \left| \frac{1}{2} v_{busB}(k+1) - v_{1B}(k+1) \right| + \left| \frac{1}{2} v_{busB}(k+1) - v_{2B}(k+1) \right| \quad (7.6.6)
\end{aligned}$$

7.6.5 Voltage Regulation

Apart from the voltages of the flying capacitors that needs to be balanced, the bus voltages also needs to be regulated. The controllers of Section 7.6.4 only balance the two bus voltages with respect to each other, but does not regulate them to any specific steady

Algorithm 7.5 *Control 16×2*

 $t = t_0$ $state_save \leftarrow 0$ $cost_save \leftarrow \infty$ **for** $state = 1$ **to** 16 **do** $v_B =$ terminal voltage of converter Bdo predictions for converter A: $\mathbf{x}(k+1) = T_{pre}(\mathbf{A}\mathbf{x}(k) + \mathbf{B}(v_{in}(k) - v_B)) + \mathbf{x}(k)$

evaluate cost function A

if $cost < cost_save$ **then** $cost_save \leftarrow cost$ $state_save \leftarrow state$ **end if****end for**wait for $t_1 = t_0 + \frac{T_{pre}}{2}$ $state_save \leftarrow 0$ $cost_save \leftarrow \infty$ **for** $state = 1$ **to** 16 **do** $v_A =$ terminal voltage of converter Ado predictions for converter B: $\mathbf{x}(k+1) = T_{pre}(\mathbf{A}\mathbf{x}(k) + \mathbf{B}(v_{in}(k) - v_A)) + \mathbf{x}(k)$

evaluate cost function B

if $cost < cost_save$ **then** $cost_save \leftarrow cost$ $state_save \leftarrow state$ **end if****end for**wait for $t_2 = t_1 + \frac{T_{pe}}{2}$ and repeat

state value. This has the problem that the bus voltages will vary over different loads. The predictive controller is therefore extended to include a bus voltage regulation controller. The combination of the two controllers are set up as the double-loop controller shown in Figure 7.16. The FS-MPC block houses the predictive control algorithms of Sections 7.6.3 and 7.6.4. It requires certain measurements to be able to do the predictions and calculate the next switching state. The input current reference of the rectifier comes from the “sine wave” block. The generated unity sine wave is in-phase with the input voltage so that the input power factor of the converter is unity. The current reference is scaled by factor d to regulate the sum of the bus voltages to a value which is 20% greater than the magnitude of the input voltage. e is the error between the bus reference and the bus measurement.

This error is fed into a linear compensator $D(s)$ to produce d .

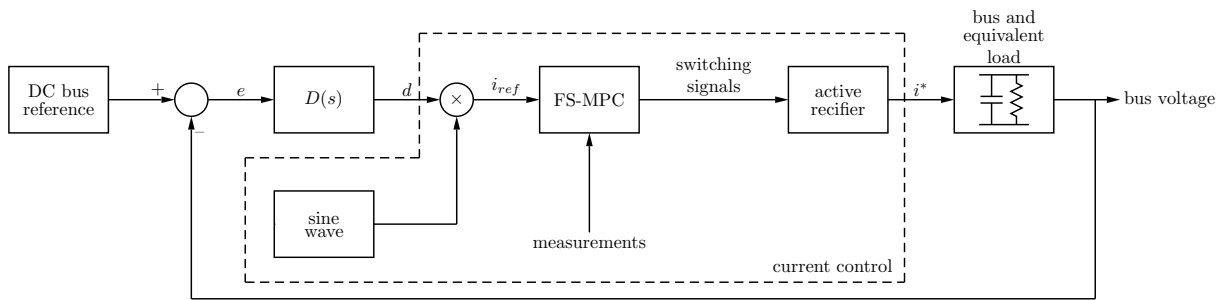


Figure 7.16: Double-loop controller to control input current and regulate bus voltage(s).

$D(s)$ is chosen as $\frac{K_I}{s}$ for its simplicity. The voltage regulator outer loop should be designed to have a 10% overshoot on a step response. The difficulty in designing the outer loop is the fact that a clear model for the current controller is not available. The model of the converter can be approximated by the bus capacitor and an equivalent load. The current controller and the RC -model of the converter can be grouped together to give the resulting control diagram in Figure 7.17 where $D(s)$ is the compensator of the voltage controller and $G(s)$ is the grouped current controller and RC converter model. Because the current controller will be much faster than the voltage controller, the former can be assumed to be a constant gain when designing the voltage controller. To derive this gain we re-visit the effective duty cycle mentioned in Section 6.1.2. It stated that

$$\frac{v_{bus}}{v_{in(rms)}} = \frac{1}{D_{eff}} = \frac{i_{in(rms)}}{i_{rec(rms)}} \quad (7.6.7)$$

where $i_{rec(rms)}$ is i^* in Figure 7.16, the current feeding into the bus capacitor and effective load combination, and D_{eff} equals 0.5893.

To find the gain $\frac{d}{i^*}$ of the current controller we start with (7.6.7). Note that d will be the amplitude of the input current. The RMS value of the input current will therefore be $\frac{d}{\sqrt{2}}$. The gain is calculated in (7.6.8).

$$\begin{aligned} \frac{1}{D_{eff}} &= \frac{i_{in(rms)}}{i_{rec(rms)}} \\ &= \frac{\frac{d}{\sqrt{2}}}{i^*} \\ \frac{d}{i^*} &= \frac{\sqrt{2}}{D_{eff}} \end{aligned} \quad (7.6.8)$$

The RC -model of the converter and the current controller gain from (7.6.8) together is given by

$$G(s) = \left(\frac{\sqrt{2}}{D_{eff}} \right) \cdot \left(\frac{\frac{1}{RC}}{s + \frac{1}{RC}} \right) \quad (7.6.9)$$

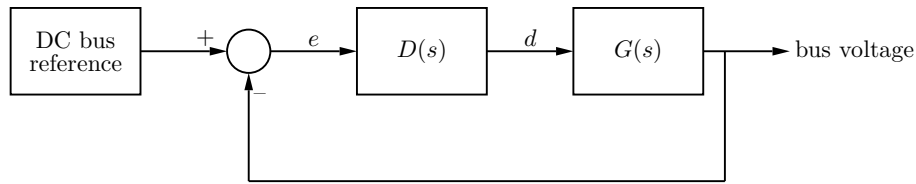


Figure 7.17: Voltage controller.

where R is an equivalent load resistance of 360Ω and C is the bus capacitance of $300 \mu\text{F}$. Defining the compensator $D(s)$ of the voltage controller as

$$D(s) = \frac{K_I}{s} \quad (7.6.10)$$

the closed loop system becomes

$$\begin{aligned} \text{closedloop}(s) &= \frac{D(s) \cdot G(s)}{1 + D(s) \cdot G(s)} \\ &= \frac{\frac{\sqrt{2}K_I}{D_{eff}C}}{s^2 + \frac{s}{RC} + \frac{\sqrt{2}K_I}{D_{eff}C}} \end{aligned} \quad (7.6.11)$$

The required value for K_I can be obtained from (7.6.11) knowing that $2\zeta\omega_n = \frac{1}{RC}$ and $\omega_n^2 = \frac{\sqrt{2}K_I}{D_{eff}C}$. Wanting an overshoot of 10% gives $\zeta = 0.5912$ which gives $K_I = 0.0077$.

The bode diagram of the closed loop system is shown in Figure 7.18(a). It shows that the system has unity DC gain and a closed loop bandwidth of about 0.3 Hz. The low bandwidth does unfortunately mean that the controller will be slow to respond to errors in the bus voltages. The fact that it is much lower than the 100 Hz bus voltage ripple means that it will not try to compensate for that. The step response of the system in Figure 7.18(b) shows that the system will have a zero steady state tracking error and a 10% overshoot.

7.6.6 Software

As stated in Section 7.1 an FPGA should be used to implement the control algorithms. The most important implemented software components are shown in Figures 7.19 and 7.20. These are only a small extract of the complete control software.

The *adc* component in Figure 7.19 receives the *ADCLKin* clock from the ADC and relays the received data bits to the *lvds_io* component. Here, the bits are framed and buffered for further use by the *convert* components. The *convert* components output the scaled, fixed-point values of the measurement to be used by the control algorithms. Eight *convert* components are instantiated so that the conversions are done in parallel. This saves time and the converted results are available with minimal delay between the actual sample and the converted data.

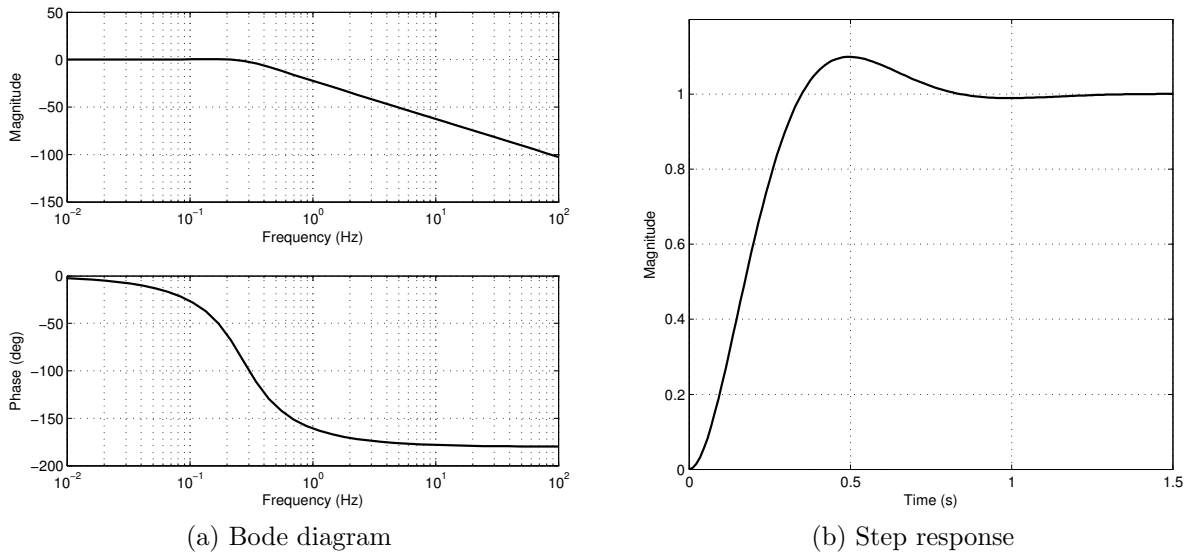


Figure 7.18: Voltage controller bode diagram and step response.

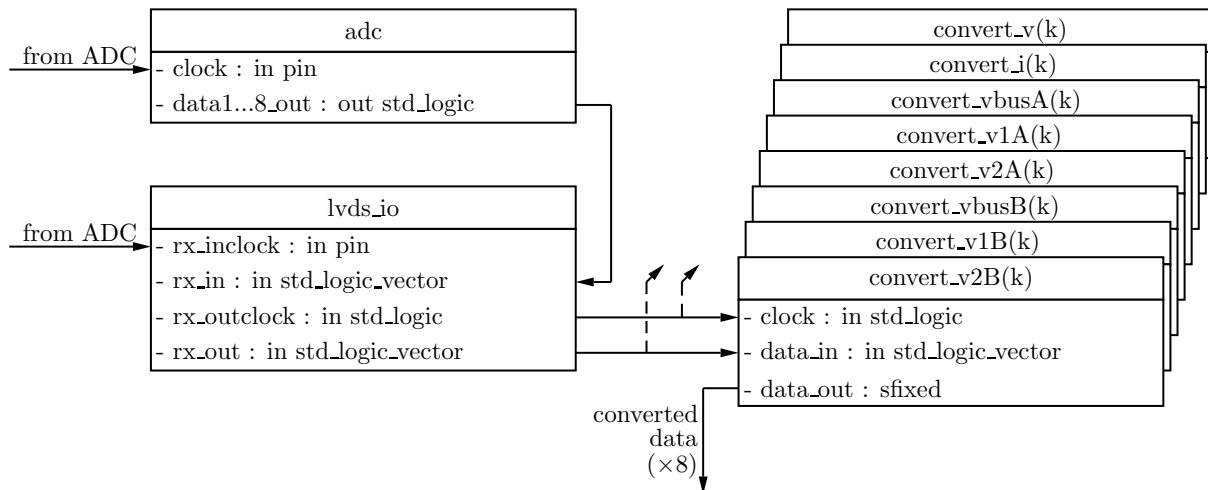


Figure 7.19: VHDL entities implementing the control code for ADC operation.

Figure 7.20 shows the implementation of the predictive controller. The control path starts with the input voltage measurement being used to generate the unity sinusoidal wave. This is passed to the voltage controller that generates the reference current. All the measurements, as well as the reference current are used by *current_control* to calculate the next switching state. The *current_control* component does the predictions for the possible switching states, calculates the cost for each switching state, and compares the costs to determine the minimum. The prediction and cost equations of the different switching states are implemented in parallel. This means that all the costs for all the possible switching states are calculated simultaneously. If a DSP controller was used, all the calculations would have been done in a serial fashion, increasing the computation time.

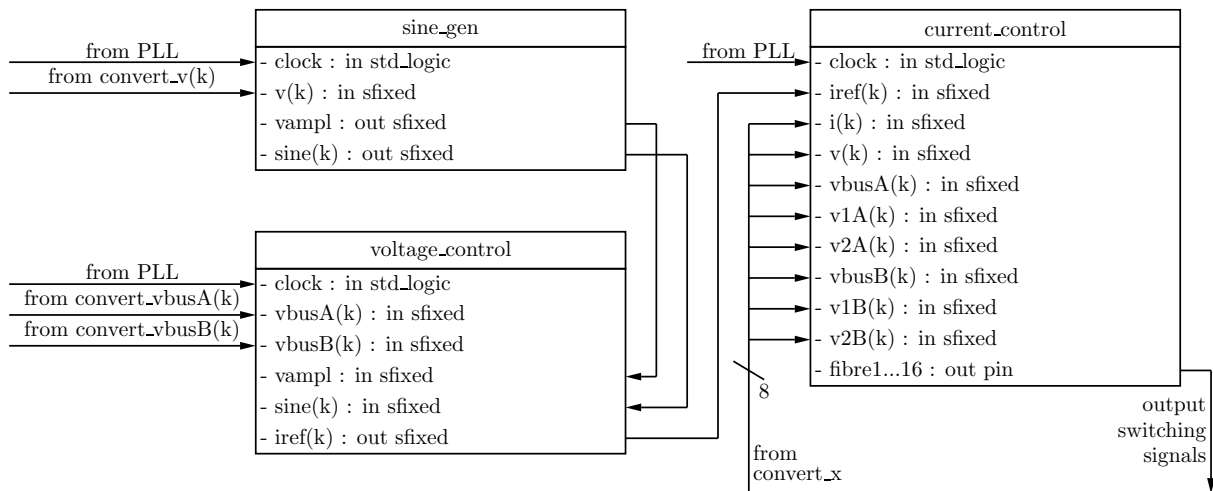


Figure 7.20: VHDL entities implementing the voltage and current control algorithms.

7.7 Summary

This chapter gave a justification for choosing an FPGA as the digital controller of choice. The measurement hardware was designed with isolated operational amplifiers to isolate the FPGA host board from the high voltage measurements. The differential signals from the measurement circuits needed to be buffered and low-pass filter before passing it to the analogue-to-digital converter.

The control algorithms for controlling the isolation stage, a single active rectifier, and dual active rectifiers were also given. For the active rectifiers the predictive controller algorithms were shown. For each algorithm the corresponding cost function and number of multiplications needed were given. *Control 256* proved not suitable for on-line implementation because of the large number of calculations it needed.

Lastly, the double-loop controller was designed. The predictive algorithms formed the inner-loop with an I compensator in the outer-loop. The voltage controller was designed for a 10% overshoot on a step input. The software implementation of the double-loop controller was then given.

Chapter 8

Simulation Results

This chapter includes various simulation results to validate the hardware designs and control algorithms. First, the isolation stage is shown. The correct working of the balancing resistor, transformer, diode rectifier, and LC low-pass filter is validated.

Next, a single active rectifier is simulated with its predictive controller. The input voltage was steadily increased to see whether the controller can balance the flying capacitor voltages from start-up to steady state.

Dual active rectifiers were also simulated. The three proposed predictive control algorithms given in Section 7.6.4 are compared by means of voltage errors, current errors, number of calculations required, etc. Also, the effect of using an inaccurate model for the predictions are investigated.

Lastly, the voltage controller of the double-loop control scheme is simulated.

8.1 Isolation Stage

The isolation stage consists of the flying-capacitor converter back-end with balancing resistors, transformer, diode rectifier and output filter. The circuit used for the simulation is shown in Figure 8.1 with its parameters listed in Table 8.1. The bus voltage v_{bus} was ramped from zero to 600 V over a time of 1 s. This was done to simulate the start-up of the whole converter where the input voltage is steadily increased by hand to the required value. The bus voltage will also increase as the input voltage is increased. The simulation results are shown in Figure 8.2.

The simulation shows two important things. Firstly, Figure 8.2(a) shows that the flying capacitor voltages are indeed balanced to half the bus voltage. The steady-state voltages of these are 303 V with a 80 kHz ripple of negligible amplitude. With a 600 V bus voltage this is only a 1% deviation from the required 300 V. Secondly, Figure 8.2(b) shows that

Table 8.1: Isolation stage simulation parameters

Parameter	Value	Description
R_1, R_3, R_4, R_6	10 k Ω	balancing resistors
R_2, R_5	10.7 k Ω	balancing resistors
C_1, C_2	10 μ F	flying-capacitors
v_{bus}	600 V	nominal bus voltage
v_1 and v_2	300 V	nominal capacitor voltages
C_f	57.8 nF	filter capacitor
L_f	912 μ H	filter inductor
R_{load}	72.9 Ω	load resistor
$\frac{N_2}{N_1}$	$\frac{1}{2}$	transformer winding ratio
v_{out}	270 V	nominal output voltage
f_s	40 kHz	switching frequency

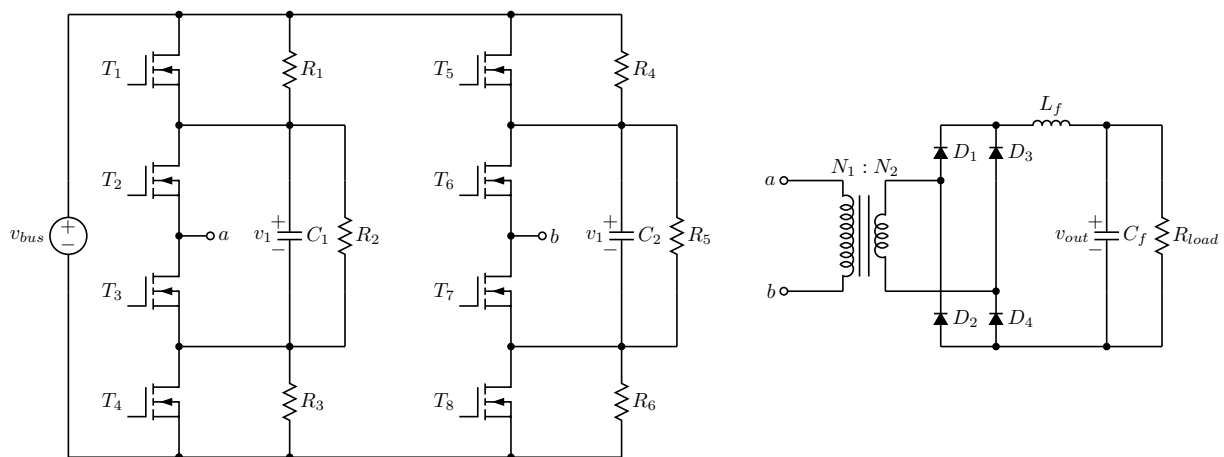


Figure 8.1: Isolation stage circuit with balancing resistors included.

the filter inductor current and filter capacitor voltage is as it was designed. The inductor current has a steady-state value of 3.7 A with a 8% ripple. The capacitor voltage has a 270 V mean value with a 8 V ripple. The ripples were designed to be 10% and 10 V, respectively. These results confirm the correct working of the balancing resistors and that the values of the output filter components were correctly designed.

8.2 Single Converter

A single flying-capacitor active rectifier is shown in Figure 8.3 with its simulation parameters listed in Table 8.2. The back-end has been replaced with an equivalent 360 Ω resistor. The control algorithm used to control the input current and the flying capacitor voltages is shown in Algorithm 7.1. The α weight of the cost function was set to 4.

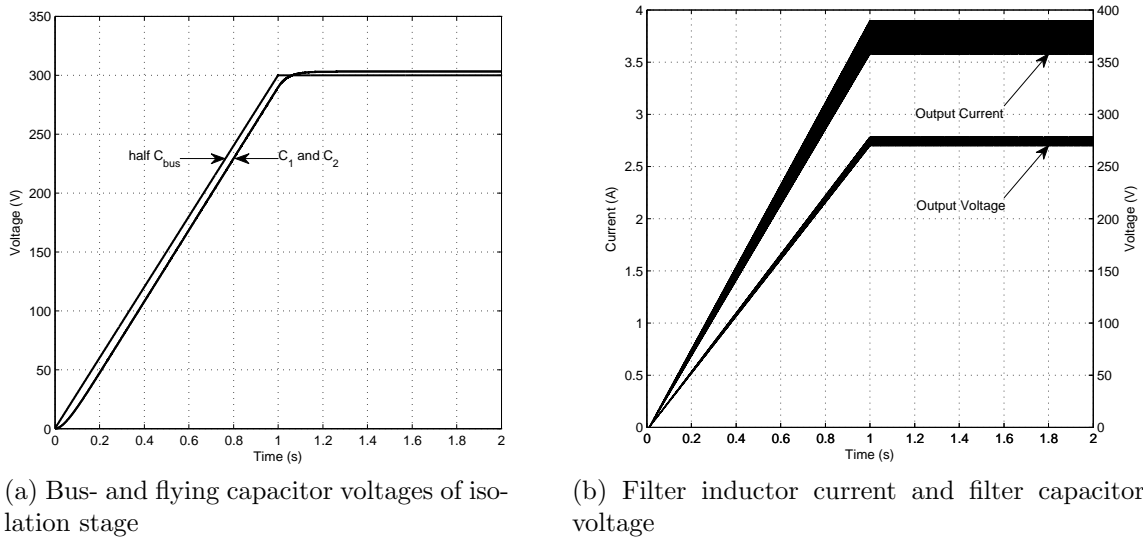


Figure 8.2: Isolation stage simulation results.

Table 8.2: Active rectifier simulation parameters

Parameter	Value	Description
R_{load}	360Ω	load resistor
L	18.75 mH	boost inductor
C	$300 \mu\text{F}$	all capacitors
v_{in}	$500 V_{peak}$ at 50 Hz	input voltage
v_{bus}	600 V	nominal bus voltage
v_1 and v_2	300 V	nominal capacitor voltage
T_{pre}	$12.5 \mu\text{s}$	prediction period

The simulation results are shown in Figure 8.4. The input voltage was increased from zero to $500 V_{peak}$ over a period of 10s. This was done to eliminate the use for an additional pre-charging system. The input voltage cannot be applied at full voltage if the capacitors of the system are not balanced to their correct voltages. The current reference used during start-up and thereafter was calculated as

$$\frac{(1.2 \cdot v_{in(peak)})^2}{360} = \frac{v_{in(peak)} \cdot i_{ref(peak)}}{2} \quad (8.2.1)$$

$$i_{ref(peak)} = \frac{2 \cdot 1.2^2 \cdot v_{in(peak)}}{360}.$$

Figure 8.4(a) shows how the flying capacitor and bus voltage increased when the input voltage was ramped up. Throughout the simulation the control algorithm was capable of balancing the voltages of the two flying capacitor to half the bus voltage. Figure 8.4(b)

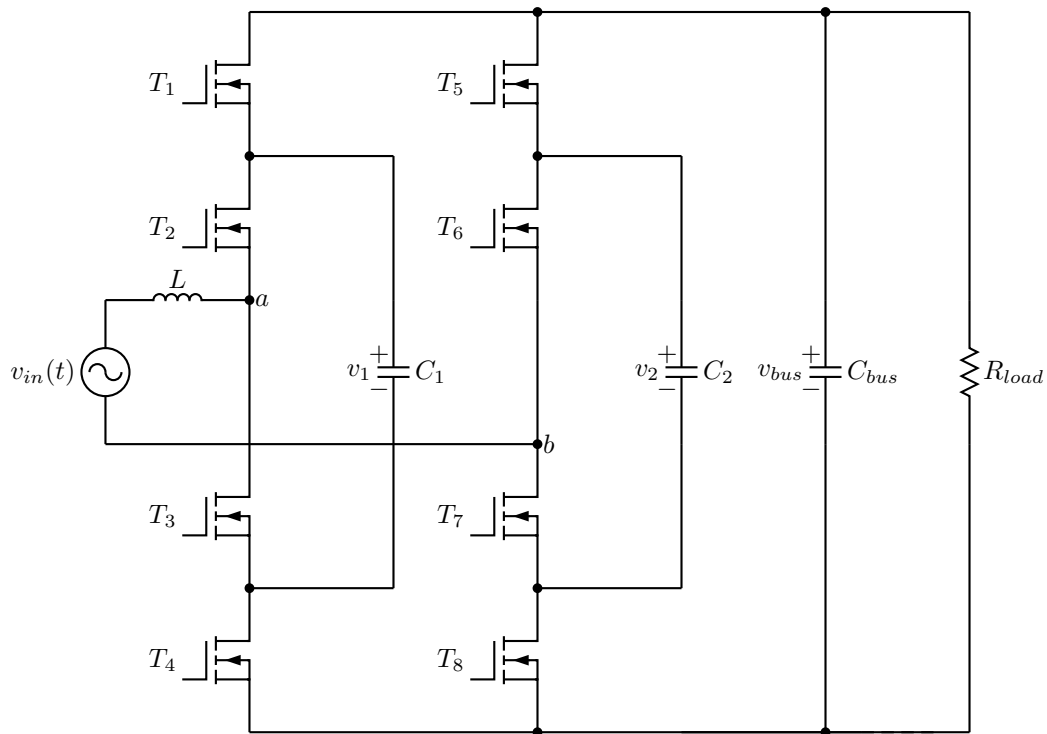
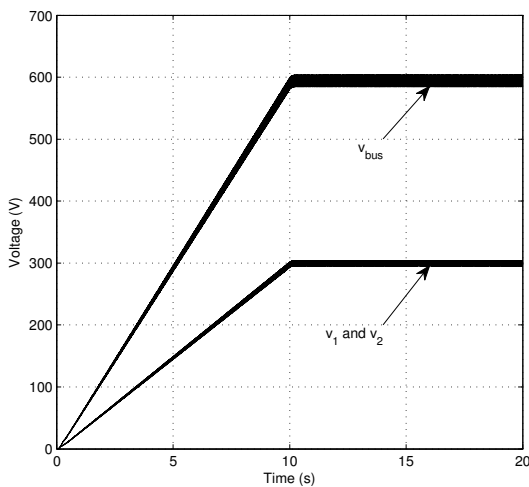
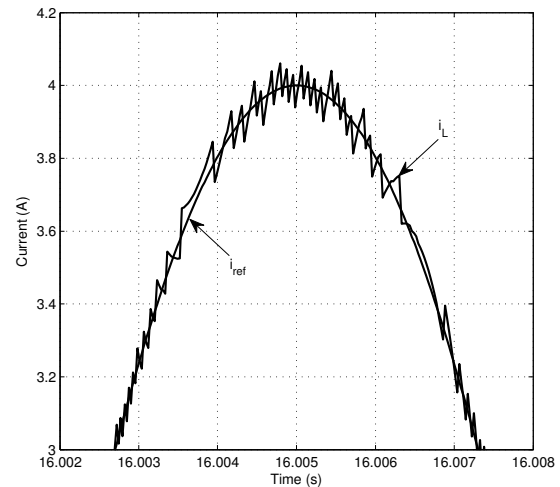


Figure 8.3: Single active rectifier with resistive load.



(a) Internal voltages of active rectifier



(b) Rectifier input current and reference

Figure 8.4: Single rectifier simulation results.

shows the input current where the controller could control it to be sinusoidal. The ripple on the current is non-uniform because of the predictive controller.

For a laboratory prototype the commissioning of the converter, by ramping the input voltage over time, is not a problem. For a final design and implementation a dedicated start-up circuit will have to be included. The control algorithm did, however, prove sufficient for both the start-up and steady-state operation of the converter.

8.3 Dual Converters

The circuit for simulating the dual active rectifier is shown in Figure 8.5. The circuit parameters, as listed in Table 8.3, applies. Note that the inductance of the boost inductor and the input voltage is double the values used for the single active rectifier. The isolation stages have again been replaced by equivalent resistors. The dual rectifiers were simulated with *Control 16*, *32*, and 16×2 .

Table 8.3: Active rectifier simulation parameters

Parameter	Value	Description
R_{loadx}	360Ω	load resistors
L	37.5 mH	boost inductor
C	$300 \mu\text{F}$	all capacitors
v_{in}	1000 V_{peak} at 50 Hz	input voltage
v_{busx}	600 V	nominal bus voltages
v_{1x} and v_{2x}	300 V	nominal capacitor voltages
T_{pre}	$12.5 \mu\text{s}$	prediction period

The simulations were started with the converters in an unbalanced steady-state. This means that the bus voltages were not equal to one another and that the voltages of the flying capacitors did not equal half the respective bus voltages. At time 500 ms, another unbalance was introduced. The two load resistors were made unequal by adjusting their values by 20% in opposite directions. This unbalance was applied for 50 ms before removing it and letting the converters rebalance their voltages. The unbalanced loads will let the bus voltages of two the converters become unequal. The bus voltage of the converter with the smaller resistor will increase while the other's will decrease. The predictive controller is suppose to keep the four flying capacitor voltages balanced with respect to their bus voltage.

8.3.1 *Control 16*

The algorithm for *Control 16* is given in Algorithm 7.3. The α and β weights in the cost function equalled 10 and 1, respectively. Its results are shown in Figure 8.6. The controller was capable of completely balancing the initial unbalance, but could not keep the flying capacitor voltages balanced during the second introduced unbalance.

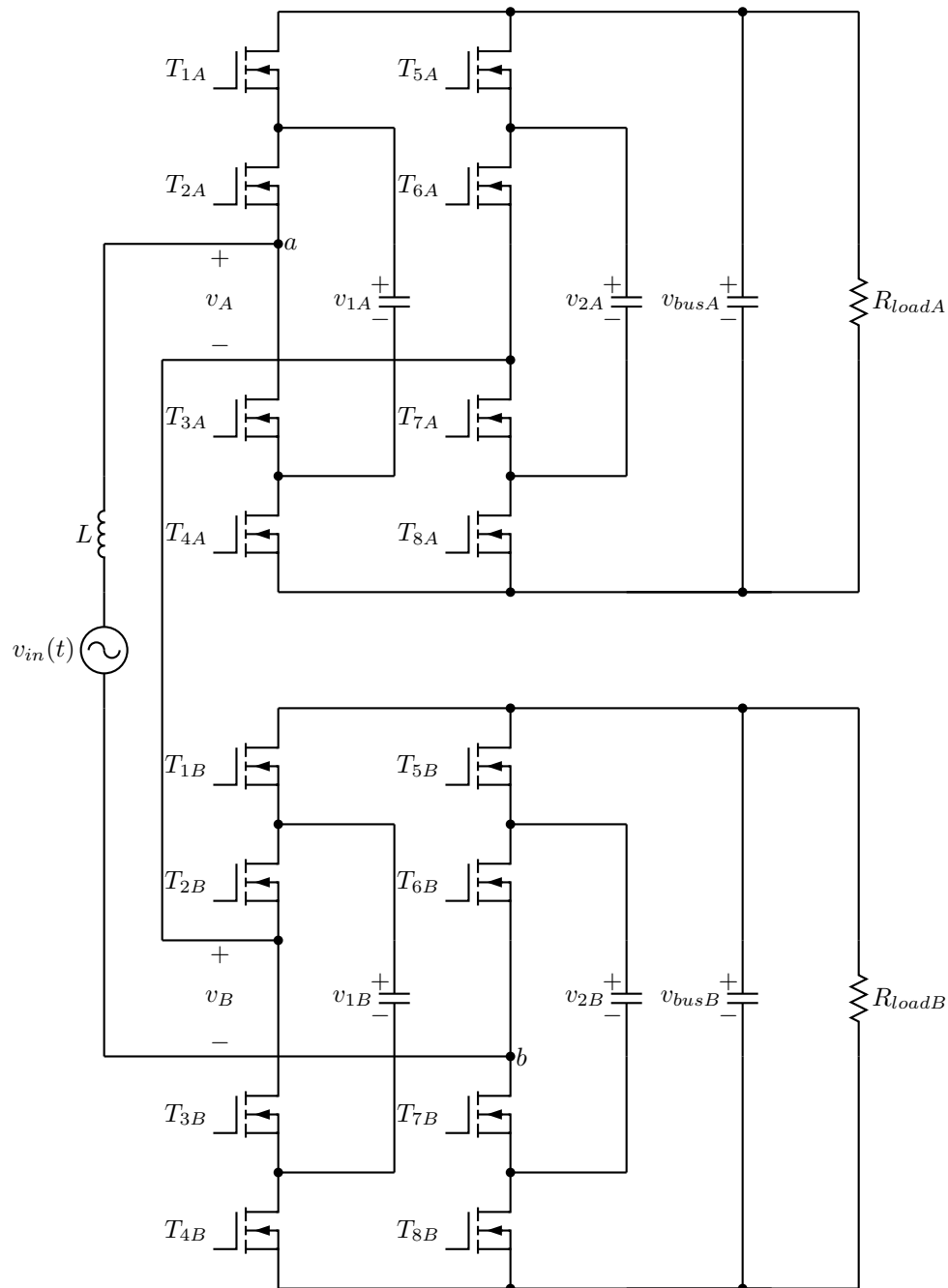
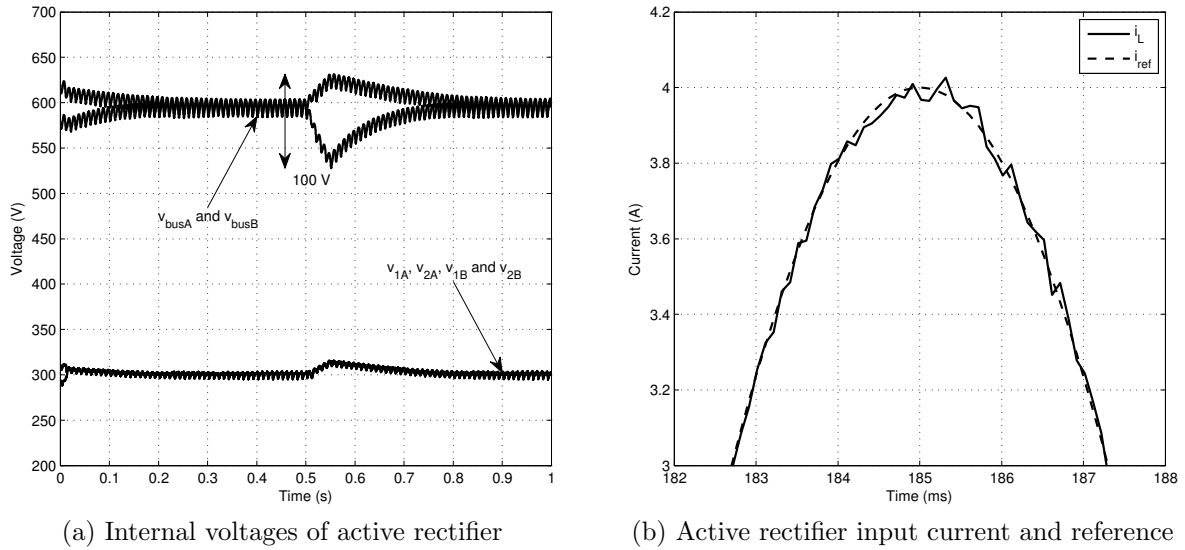
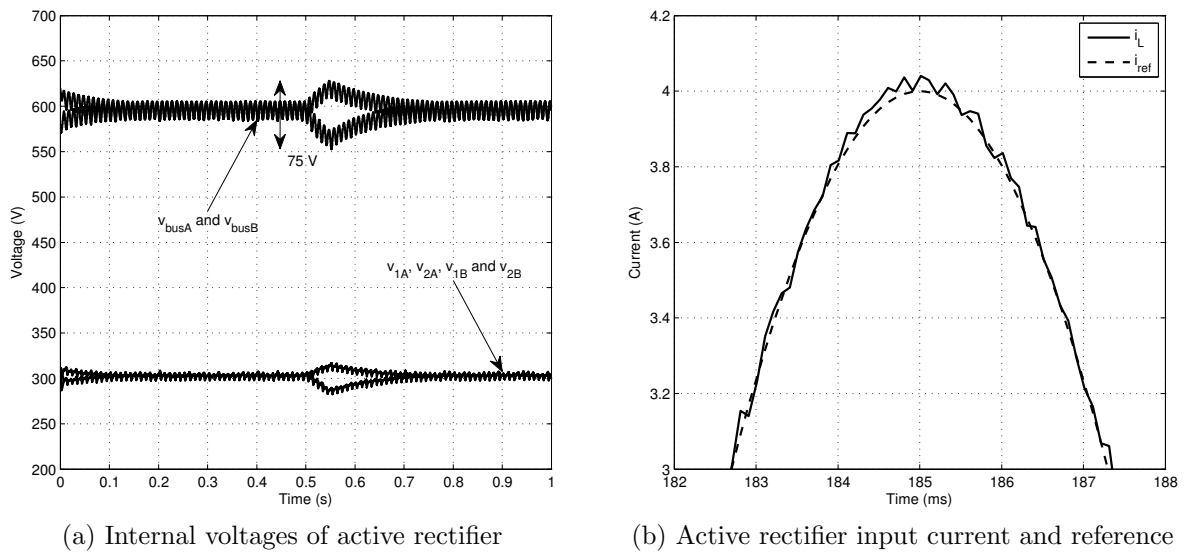


Figure 8.5: Dual active rectifier with resistive loads.

8.3.2 Control 32

The algorithm for *Control 32* is given in Algorithm 7.4 with the results in Figure 8.7. The α and β weights in the cost function equalled 10 and 2, respectively. It was capable of re-balancing all the voltages and kept the flying capacitor voltages balanced with respect to the bus voltages during the times of unbalance.

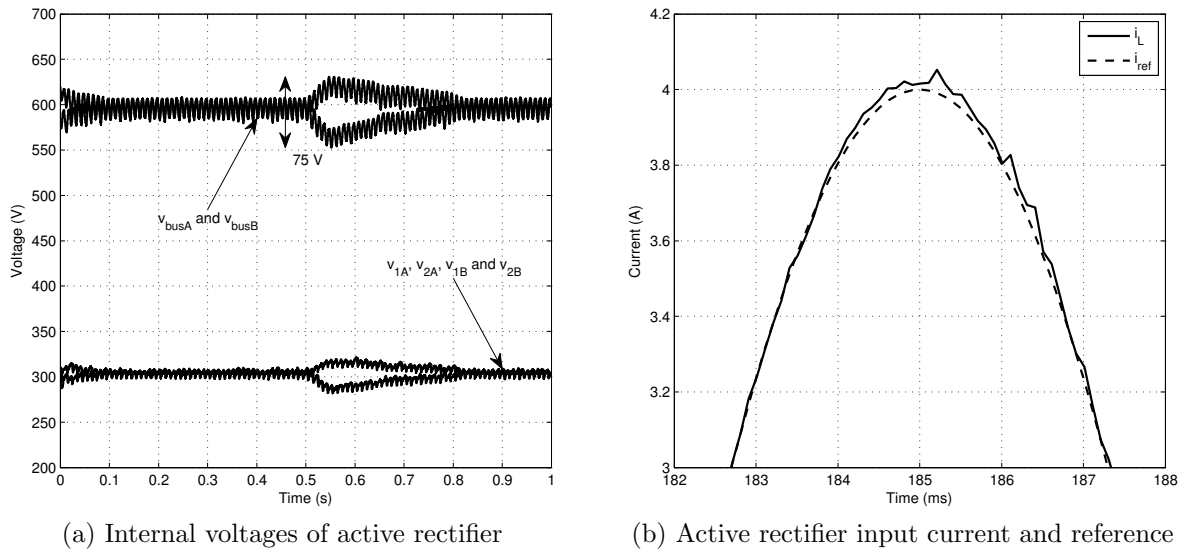

 Figure 8.6: Simulation results of dual rectifier under *Control 16*.

 Figure 8.7: Simulation results of dual rectifier under *Control 32*.

8.3.3 *Control 16* × 2

The algorithm for *Control 16* × 2 is given in Algorithm 7.5 with the results in Figure 8.7. The α and β weights in the cost function equalled 4 and 1, respectively. It was also capable of re-balancing all the voltages and keep the flying capacitor voltages balanced with respect to the bus voltages during the times of unbalance.

8.3.4 Comparison

The three control algorithms are compared by looking at the voltage and input current root-mean-square errors, as well as the settling times after the unbalances were introduced.


 Figure 8.8: Simulation results of dual rectifier under *Control 16* \times *2*.

The errors and settling times are shown in Table 8.4. Percentages are given relative to the error values of *Control 16*.

Table 8.4: Comparison of control algorithms.

	<i>Control 16</i>	<i>Control 32</i>	<i>Control 16</i> \times <i>2</i>
Voltage error	11.9 (+0%)	8.3 (-30.3%)	10.5 (-11.8%)
Current error	0.0298 (+0%)	0.0330 (+10.7%)	0.0213 (-28.5%)
Initial settling time	400 ms	150 ms	100 ms
Unbalance settling time	500 ms	300 ms	300 ms
Bus voltage deviation	100 V	75 V	75 V
Calculations	160	96	48

By comparing the three control algorithms it is clear that *Control 16* is not adequate. It was able to balance the bus voltages, but could not keep the flying capacitor voltages balanced with respect the two bus voltages. It also had the longest settling times.

The simulation of *Control 32* had the smallest voltage error, but the largest current error. Its settling times were much faster than the simulation of *Control 16*, but it uses more calculations for its predictions.

The simulation of *Control 16* \times *2* had a shorter settling time than *Control 16* and although its voltage error was larger, its current error was smaller than that of *Control 32*. It also requires the least number of calculations with better settling times than *Control 32*.

8.4 Inaccurate Model

The effect of using an inaccurate converter model for the predictions was also investigated. The influence of over- and underestimating the value of the load resistors and capacitors used in the predictions by 50% was simulated and the effect on the voltage and current errors is shown in Tables 8.5 and 8.6. The voltage and current error for the $R_{predict} = 1.0 \times R_{real}$ and $C_{predict} = 1.0 \times C_{real}$ cases were used as a baseline to calculate the percentage change in the errors when the modelled value was changed.

Table 8.5: Effect on control algorithms of inaccurate modelling of load resistance.

	<i>Control 16</i>	<i>Control 32</i>	<i>Control 16×2</i>
$R_{predict} = 1.5 \times R_{real}$			
Voltage Error	+0.2%	+2.9%	+0.0%
Current Error	+0.9%	+2.68%	+0.0%
$R_{predict} = 1.0 \times R_{real}$			
Voltage Error	+0.0%	+0.0%	+0.0%
Current Error	+0.0%	+0.0%	+0.0%
$R_{predict} = 0.5 \times R_{real}$			
Voltage Error	-0.6%	+2.6%	+0.0%
Current Error	+0.3%	+3.2%	+0.0%

The results in Table 8.5 show that all three control algorithms are robust in terms of an inaccurate load model. The worst influence of the inaccurate load model was the 3.17% increase in the current error of *Control 32* when the load was underestimated by 50%. *Control 32* was affected the worst by the inaccurate modelling and *Control 16×2* was not influenced at all.

The results in Table 8.6 show that the inaccurate modelling of the capacitor values has a greater effect of the error values than the incorrect model has. Even though *Control 16×2* was affected the worst with a 17.2% increase in its current error, the input was still sinusoidal. The input current for the two cases $C_{predict} = 1.0 \times C_{real}$ and $C_{predict} = 0.5 \times C_{real}$ are shown in Figure 8.9. The 17.2% increase in the current is visible, but the resulting waveform looks still acceptable.

The reason for the negligibly small effects on the errors could be due to the combination of the large capacitance in the converter and the high control frequency. The large capacitance results in a large time constant which, together with the high control frequency, mean that the values of the measured states do not change very much between two consecutive executions of the control algorithm.

Table 8.6: Effect on control algorithms of inaccurate modelling of capacitors.

	<i>Control 16</i>	<i>Control 32</i>	<i>Control 16×2</i>
	$C_{predict} = 1.5 \times C_{real}$		
Voltage Error	-1.2%	+0.8%	-7.7%
Current Error	+2.3%	+3.7%	-4.6%
	$C_{predict} = 1.0 \times C_{real}$		
Voltage Error	+0.0%	+0.0%	+0.0%
Current Error	+0.0%	+0.0%	+0.0%
	$C_{predict} = 0.5 \times C_{real}$		
Voltage Error	-6.1%	+7.0%	+7.7%
Current Error	+5.2%	+8.9%	+17.2%

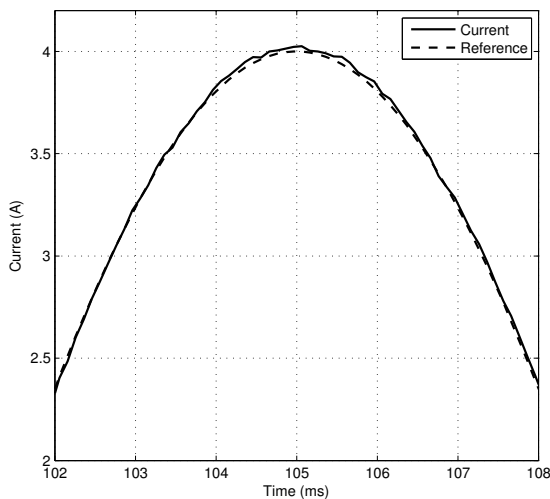
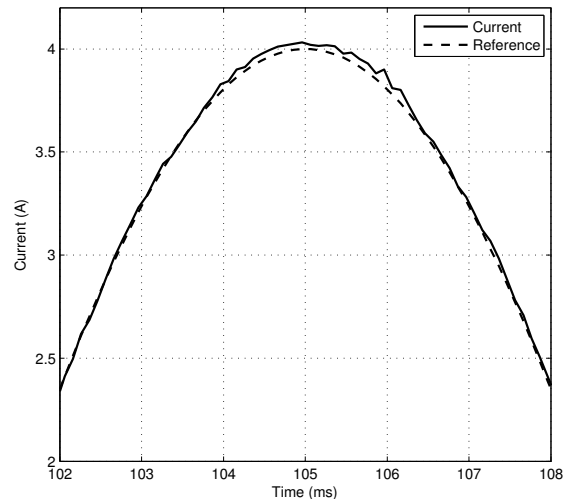

 (a) $C_{predict} = 1.0 \times C_{real}$

 (b) $C_{predict} = 0.5 \times C_{real}$

 Figure 8.9: Input current with *Control 16×2* and inaccurately modelled capacitor values.

8.5 Voltage Regulation

The voltage regulation control loop described in Section 7.6.5 was also simulated. Changes in the input voltage and load was made to investigate the response of the voltage controller.

Figure 8.10 shows the response on a change in the input voltage. At time 500 ms the input voltage was changed from $500 V_{peak}$ to $250 V_{peak}$. The $v_{bus(ref)}$ on the plot is a 20% boost of the input voltage. At time 1.5 s the input voltage was changed back to $500 V_{peak}$. The predictive controller's ability to balance the internal voltages is proved from the fact that the voltages stay balanced during the changes and throughout the simulation.

Figure 8.11(a) shows a single converter where the input voltage stays constant at $500 V_{peak}$, but the load was changed. At time 500 ms the load was changed from 360Ω to 270Ω and

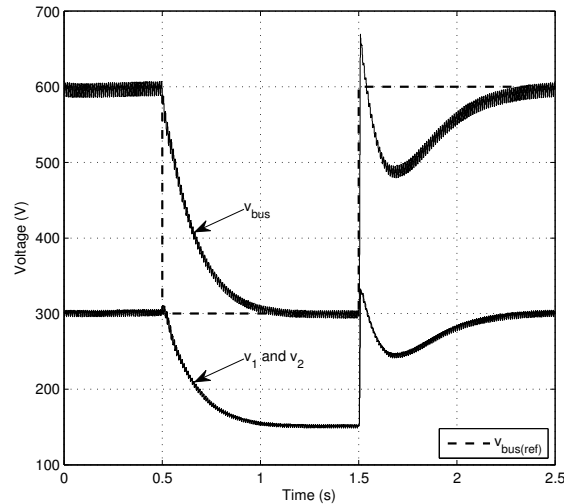
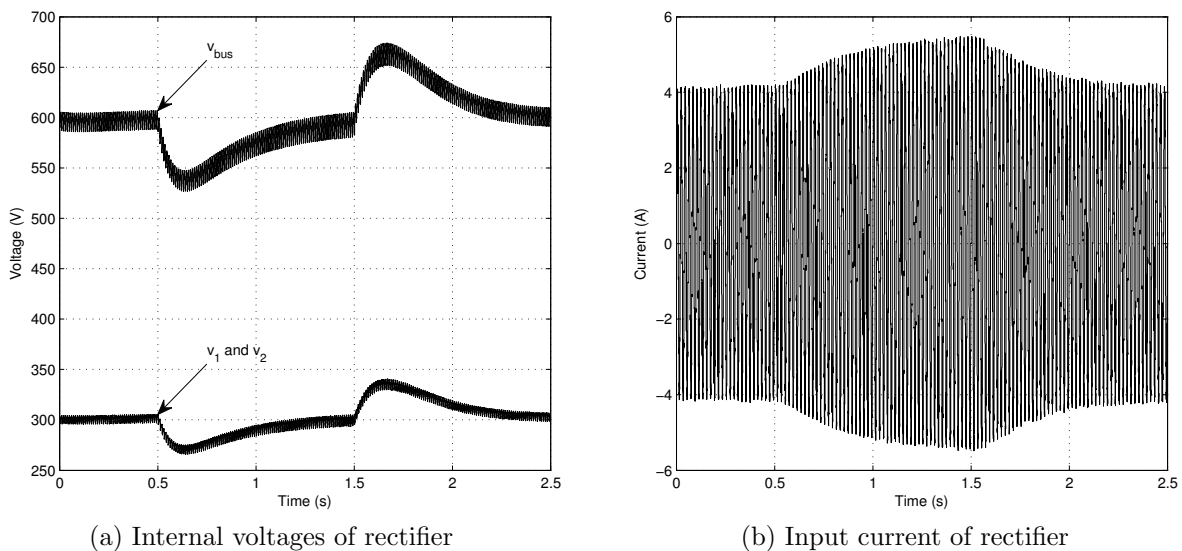


Figure 8.10: Internal voltages of single rectifier with input voltage changes.

at 1.5 s it was reset to 360Ω . The bus voltage reference was therefore 600 V throughout the simulation. From the input current, Figure 8.11(b), the effect of the increase in load can be seen. The voltage controller increased the input current to regulate the bus voltage at 600 V. The ≈ 1 s settling times can also be seen.



(a) Internal voltages of rectifier

(b) Input current of rectifier

Figure 8.11: Single rectifier with load changes.

8.6 Summary

This chapter showed various simulation results to aid in proving the correct design of the component values and control algorithms. The voltage balancing scheme for the isolation stage with its transformer, diode rectifier and LC filter proved adequate. The values of

the balancing resistors proved accurate to balance the flying capacitor voltages within 1% of the required voltage. The fixed duty cycle, fixed frequency PWM controller of the isolation stage proved adequate for this application.

The more important predictive controllers also had satisfactory results. All the predictive controllers were able to control the input current to be sinusoidal, as well as regulate the flying capacitor voltages. The three control algorithms for the dual active rectifiers were compared on the grounds of voltage and current errors, the settling times after unbalances, the voltage deviations during times of unbalance, and the number of calculations each algorithm requires.

The effect of inaccurately modelled load resistors and capacitor value were also simulated. An inaccurate load resistor value did not have a significant effect on any of the three control algorithms. The inaccurate capacitor values had a larger effect on the voltage and current errors. Although the errors were greater, the algorithms still performed acceptably. The input current was still controlled to be sinusoidal and the flying capacitor voltages were still balanced. This shows the robustness of predictive control.

Chapter 9

Experimental Results

This chapter includes experimental results obtained from implementing the different control algorithms on hardware. The results are divided into three sections: the operation of a single active rectifier together with its isolation stage, the operation of dual active rectifiers but with equivalent loads instead of the isolation stage, and finally complete dual active rectifiers with their isolation stages.

The correct operation of a single converter control algorithm and the hardware peripherals were tested first. The predictive controller results are shown for steady-state, as well as unbalanced operation. Measurements of the isolation stage include the balancing of the flying capacitor voltages and the DC output of the transformer and diode rectifier. The multilevel witching at the terminals of the active rectifier is also shown.

Once the single converter operated satisfactory, it was extended to the series stack of two converters to evaluate the three proposed control algorithms. Because the predictive controllers were derived for an active rectifier without an isolation stage, the series stack of two converters were first tested without them. Comparisons between the three predictive controllers are made considering current and voltage errors, and voltage deviations during introduced unbalances.

The effect of the added isolation stages is shown in Section 9.3. The same voltage and current errors as for the dual rectifiers without the isolation stages are again calculated. Unbalanced tests are also conducted. The total harmonic distortion of the input current is also calculated and the voltage controller is validated by means of load steps. Lastly, the switching harmonics and efficiencies of the three control algorithms are shown.

9.1 Single Converter

The complete single converter setup is shown in Figure 9.1. It consists of the active rectifier and isolation stage. The isolation stage consists of the flying capacitor balancing resistors, transformer, diode rectifier and LC low pass filter. The circuit parameters are listed in Table 9.1. The active rectifier is controlled with the predictive controller described by Algorithm 7.1 and the isolation stage is controlled with the PWM controller described in Section 7.6.1.

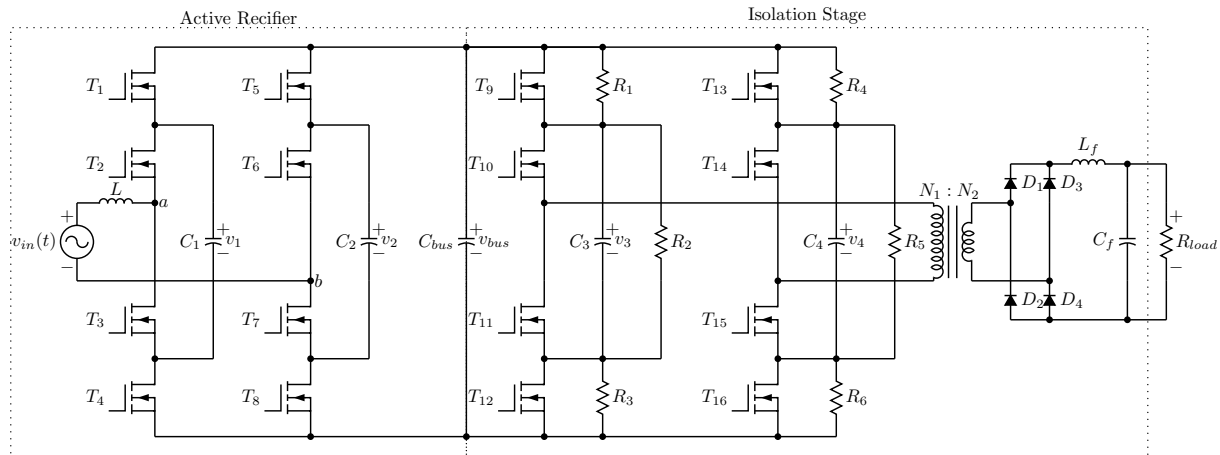


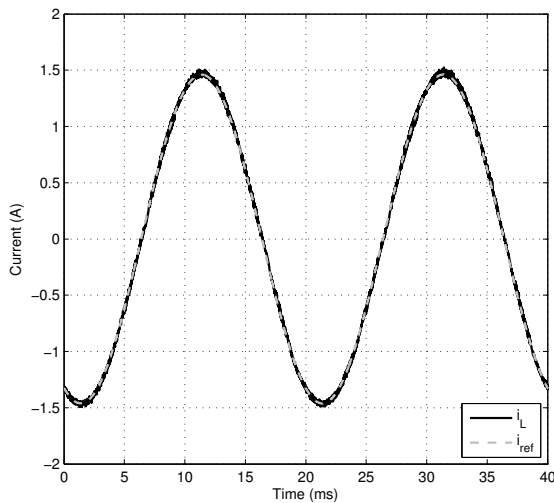
Figure 9.1: Complete single converter with active rectifier and isolation stage.

Table 9.1: Single converter experimental setup.

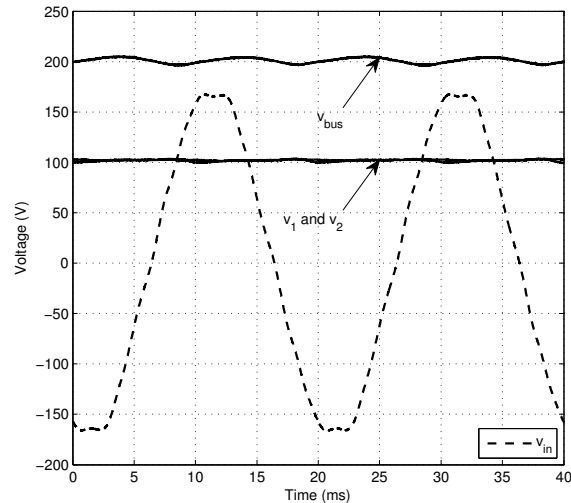
Parameter	Value	Description
Active Rectifier		
L	18.75 mH	boost inductor
C	300 μ F	bus- and flying capacitors
T_{pre}	12.5 μ s	prediction period
Isolation Stage		
R_1, R_3, R_4, R_6	10 k Ω	balancing resistors
R_2, R_5	10.7 k Ω	balancing resistors
C_3, C_4	10 μ F	flying capacitors
$\frac{N_2}{N_1}$	$\frac{1}{2}$	transformer winding ratio
C_f	57.8 nF	filter capacitor
L_f	912 μ H	filter inductor
R_{load}	72.9 Ω	load resistor
f_s	40 kHz	switching frequency

9.1.1 Control Algorithm

The input voltage, input current and bus voltage for the single converter in Figure 9.1 is shown in Figure 9.2. The measurements were taken at a bus voltage of 200 V. The current was controlled to be sinusoidal and in-phase with the input voltage. The bus voltage was the required 20% boosted above the peak value of the input voltage and the flying capacitor voltages were controlled to be half the bus voltage. It also shows the 100 Hz ripple on the bus voltage. The ripple is 9 V which is less than the designed 5% of the bus voltage. This indicates the correct design of the bus capacitor.



(a) Active rectifier input current and reference



(b) Active rectifier input-, flying capacitor- and bus voltages

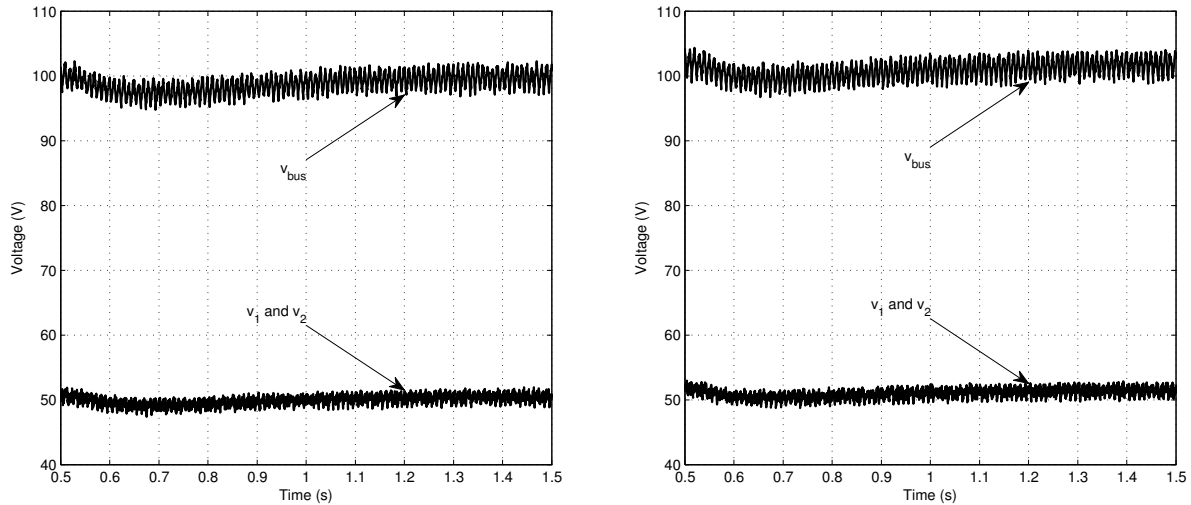
Figure 9.2: The input current, input voltage and internal voltages of the single converter active rectifier.

Note that, even though the input voltage in Figure 9.2(b) is not entirely sinusoidal, the input current in Figure 9.2(a) was controlled to be sinusoidal.

9.1.2 Voltage Unbalance

The capability of the control algorithm to balance the flying capacitor voltages was also measured and is shown in Figure 9.3. A 1.2 k Ω resistor in parallel with flying capacitor C_1 was switched in at 0.5 s. The unbalance was measured at a bus voltage of 100 V with and without the isolation stage connected.

In both cases the control algorithm could keep the voltages balanced, meaning that both the flying capacitor voltages always equalled half the bus voltage. The switched in resistor effectively caused an increase in the load and therefore the bus voltage dropped. The control algorithm kept the flying capacitor voltages balanced throughout the drop. The



(a) Unbalanced voltages without isolation stage

(b) Unbalanced voltages with isolation stage

Figure 9.3: A single converter's internal voltages with an unbalanced disturbance.

voltage controller increased the current reference so that the bus voltage could be the required boosted 20%.

9.1.3 Isolation Stage

The isolation stage was tested with a 100 V bus voltage. The flying capacitors of the isolation stage are also supposed to have voltages equalling half the bus voltage. Figure 9.4 shows the correct balancing of the flying capacitor voltages using the balancing resistors designed in Section 6.2.3. This proves that the balancing scheme, using the resistors, are adequate for this application. The 100 Hz ripple on the bus voltage can also be seen. This ripple comes from the active rectifier and the bus capacitor was designed to limit this ripple to less than 5%.

The DC bus voltage is passed through the isolation transformer as a square wave of 40 kHz. Figure 9.5 shows the square wave voltage and the corresponding primary winding current. Slight ringing occurs at the switching instances due to stray inductances. The ringing is, however, not severe and does not hamper the operation of the isolation stage.

The DC output of the isolation stage is shown in Figure 9.6. Figure 9.6(a) shows the 100 V bus voltage of the converter with its 100 Hz ripple. It also shows the output voltage and current at the $72.9\ \Omega$ load resistor. The ripple diffuses through the transformer as is visible in the DC outputs as well. With a bus voltage of 100 V, a duty cycle of 45% and a transformer winding ratio of 2:1, the theoretical output voltage should be 45 V. The measurement shows an output voltage of 42 V. The drop in voltage is mostly due to the voltage drop across the internal resistance of the transformer and in part to a non-ideal

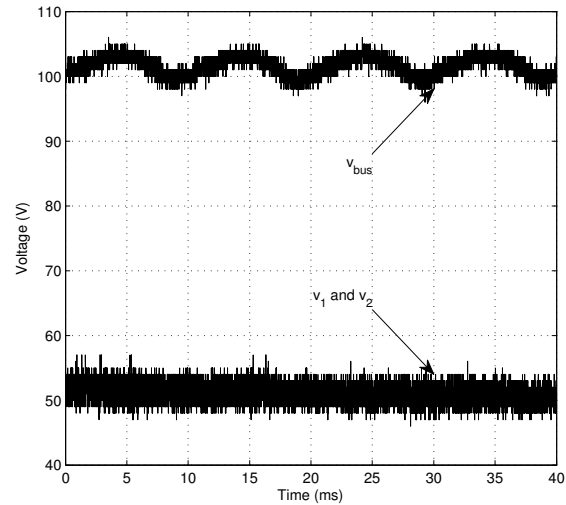
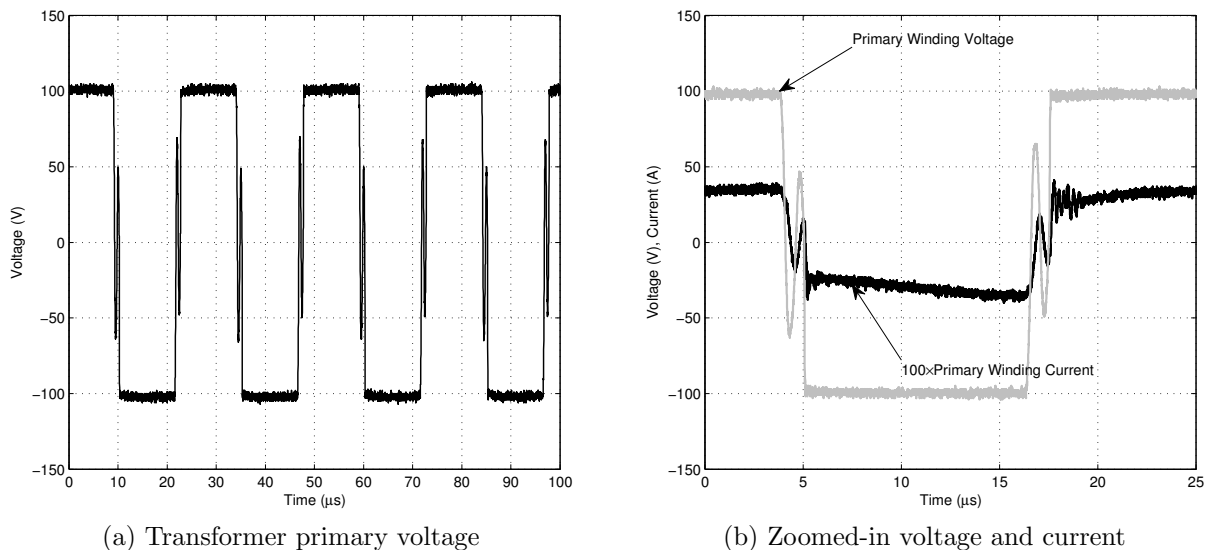


Figure 9.4: Isolation stage flying capacitor- and bus voltages.



(a) Transformer primary voltage

(b) Zoomed-in voltage and current

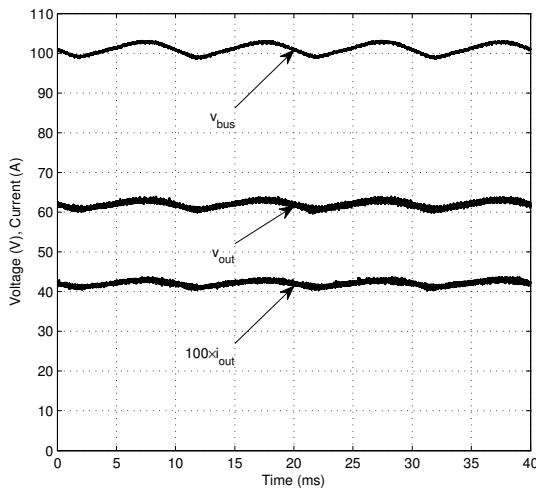
Figure 9.5: Isolation transformer terminal voltage and primary current.

winding ratio.

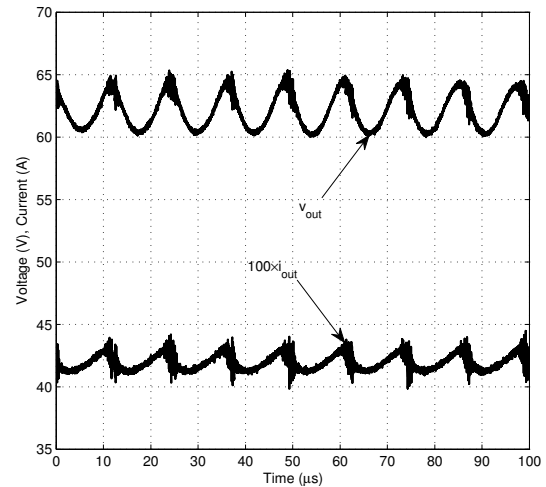
Figure 9.6(b) shows the 80 kHz switching ripple on the output voltage and current. The voltage has a 2 V ripple which, when scaled up to an output voltage of 270 V, corresponds to the designed 10 V ripple. The current has a 45 mA ripple which corresponds to the designed 10% ripple.

9.1.4 Terminal Voltage

The full-bridge, three-level active rectifier can output five different voltage levels: v_{bus} , $\frac{v_{bus}}{2}$, 0, $-\frac{v_{bus}}{2}$ and $-v_{bus}$. This five-level switching can be seen in Figure 9.7. It was taken at a bus voltage of 100 V and the terminal voltage will therefore have values of 100 V,



(a) Isolation stage bus- and output voltage, and output current



(b) Output voltage and current ripples

Figure 9.6: The DC output voltage and current of the isolation stage.

50 V, 0 V, -50 V and -100 V.

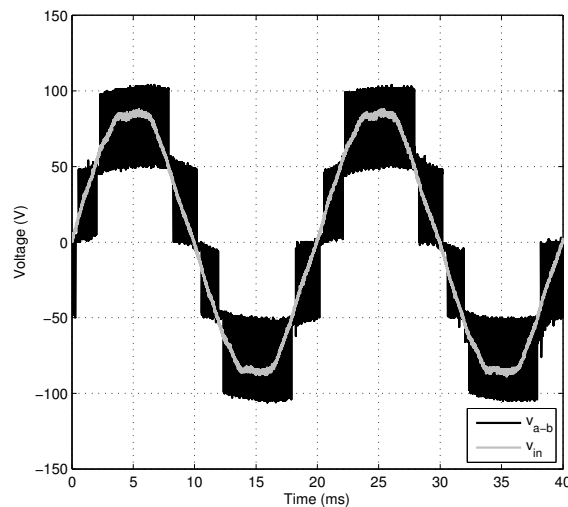


Figure 9.7: The terminal voltage and input voltage of a single active rectifier.

9.1.5 Bootstrap Supply

Table 9.2 lists the supply voltages of the bootstrap supplies of each of the eight MOSFETs. The bootstrap supply has a supply of 35 V and is reduced by each subsequent voltage drop across the bootstrap diodes. The zener regulator has a nominal 15 V output voltage.

The small variation from 15 V for the zener regulator is favourable, because all the MOSFETs are then switched with the same voltage. This helps to ensure that all the MOSFETs operate at the same switching speed.

Table 9.2: Bootstrap supply voltages.

	Bootstrap	Zener-regulator
T_1	31.86 V	14.97 V
T_2	32.82 V	15.17 V
T_3	33.63 V	15.14 V
T_4	34.59 V	15.57 V
T_5	32.12 V	15.37 V
T_6	32.88 V	15.30 V
T_7	33.75 V	15.46 V
T_8	34.63 V	15.37 V

9.2 Dual Converter (without isolation stage)

The control algorithms of Section 7.6.4 for controlling the series stack of two converters were derived for a system of the form shown in Figure 9.8. This is a simplification of the actual system where the isolation stages are used. The purpose of the measurements in this section is to validate the correct operation of the control algorithms. The simplified system is used so that the control algorithms can first be tested on the exact system they were designed for. The isolation stages will be added in the next section.

Experimental results for this configuration includes a comparison of the three control algorithms by measuring their respective current and voltage errors, as well their responses to unbalanced loads. The active rectifiers were controlled by the three predictive controllers *Control 16*, *Control 32* and *Control 16×2* described, respectively, in Algorithms 7.3, 7.4 and 7.5. The circuit parameters are listed in Table 9.3.

Table 9.3: Dual active rectifiers without the isolation stages.

Parameter	Value	Description
L	37.5 mH	boost inductor
C	300 μ F	bus- and flying capacitors
R_{load}	360 Ω	load resistors
T_{pre}	12.5 μ s	prediction period

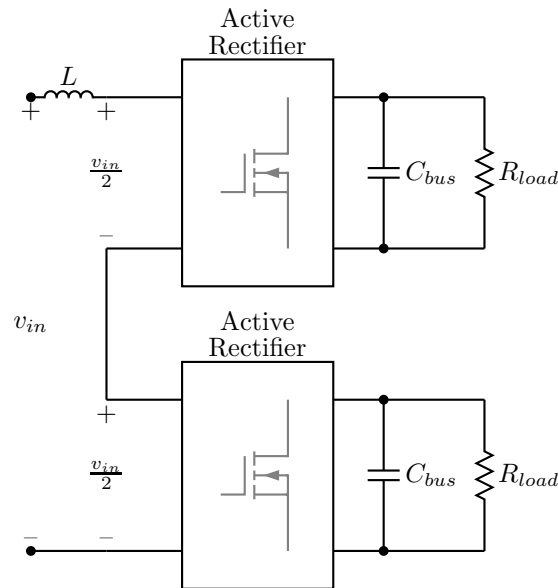


Figure 9.8: Dual, series stacked converters with individual loads.

9.2.1 Voltage and Current Errors

The voltage and current errors for the three control algorithms were measured. The calculation of the error values are defined as

$$i_{error} = \sqrt{\frac{1}{n} \sum_{k=0}^{n-1} (i_{ref}(k) - i(k))^2} \quad (9.2.1)$$

and

$$v_{error} = \sqrt{\frac{1}{n} \sum_{k=0}^{n-1} \left\{ \begin{aligned} & \left[\frac{1}{2} v_{busA}(k) - v_{1A}(k) \right]^2 + \\ & \left[\frac{1}{2} v_{busA}(k) - v_{1B}(k) \right]^2 + \\ & \left[\frac{1}{2} v_{busB}(k) - v_{1B}(k) \right]^2 + \\ & \left[\frac{1}{2} v_{busB}(k) - v_{1A}(k) \right]^2 + \\ & \left[v_{busA}(k) - v_{busB}(k) \right]^2 \end{aligned} \right\}} \quad (9.2.2)$$

where n is the number of samples used. These error values are basically the root-mean-square error between the signal and its reference value.

The voltage and current error values for the three control algorithms are shown in Figure 9.9. *Control 32* clearly produced the worst error values while *Control 16×2* produced the best. All three algorithms, however, were able to control all the necessary voltages and current to their respective reference values.

9.2.2 Voltage Unbalance

Unbalanced load conditions were introduced to verify the voltage balancing capabilities of the control algorithms. The 360Ω load resistors were changed to 288Ω for converter A

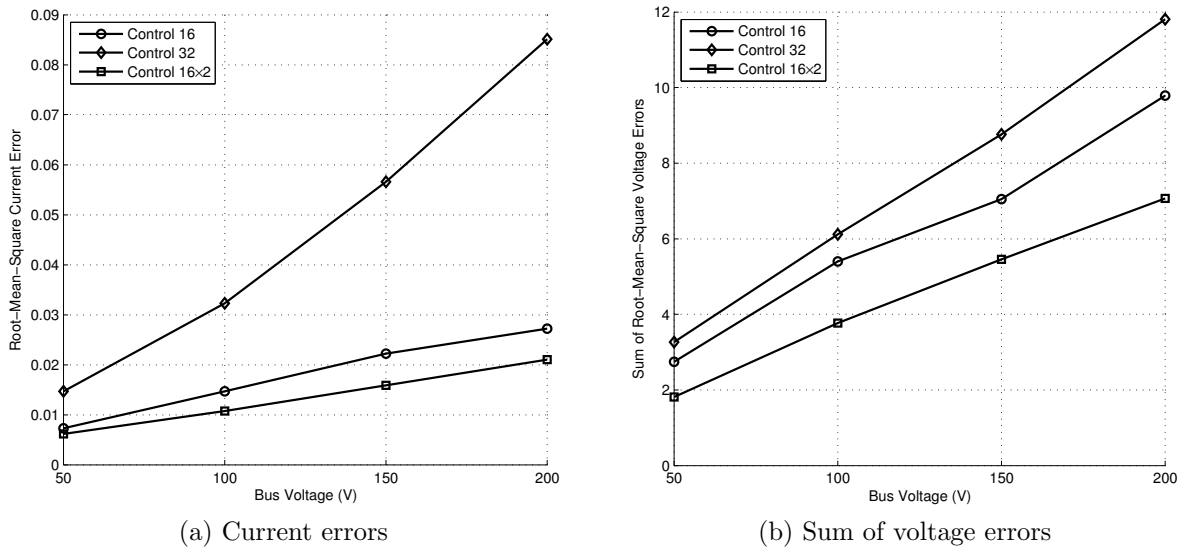


Figure 9.9: The voltage and current errors for the three control algorithms as defined in (9.2.1) and (9.2.2)

and $432\ \Omega$ for converter B (a change of $\pm 20\%$, respectively). The responses for the three control algorithms are shown in Figure 9.10. Table 9.4 gives the voltage deviation, time-to-unbalance and time-to-rebalance for the three control algorithms. The time-to-rebalance was taken as the time the control algorithm took to rebalance the internal voltages from unbalanced conditions after the unbalanced loads were returned to balanced values. The measurements were taken at a steady-state bus voltage of $100\ \text{V}$ per converter.

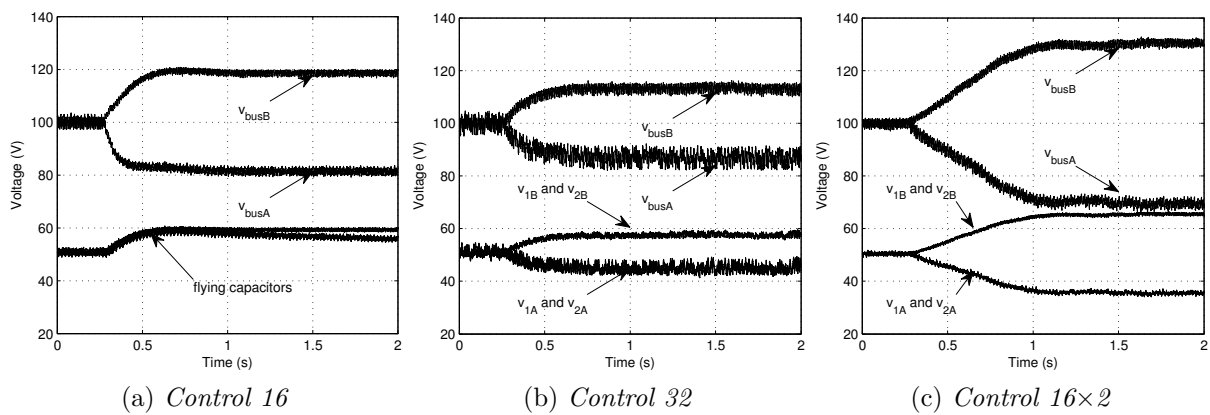


Figure 9.10: Response of internal voltages of dual active rectifiers to an unbalanced load.

Control 16 was unable to balance the four flying capacitor voltages to their respective bus voltages and is therefore not a suitable control algorithm. *Control 32* and 16×2 were able to balance the flying capacitor voltages with *Control 32* obtaining a voltage deviation that was less than half of what *Control 16x2* could achieve.

Table 9.4: Unbalanced measurements of the two converters without their isolation stages.

	<i>Control 16</i>	<i>Control 32</i>	<i>Control 16×2</i>
Voltage deviation	40 V	25 V	60 V
Time-to-unbalance	400 ms	400 ms	900 ms
Time-to-rebalance	330 ms	300 ms	400 ms

Although *Control 16×2* produced a voltage deviation that was much larger than the other algorithms', its time-to-unbalance and time-to-rebalance were favourable. The fact that *Control 16×2* took much longer to reach its final unbalanced point shows that it is reluctant to let its internal voltages become unbalanced. Also, its time-to-rebalance shows that it is capable of rebalancing its internal voltages faster than the other algorithms when taking into account that it rebalanced a voltage deviation almost twice as large as the other algorithms in nearly the same time.

9.3 Dual Converter (with isolation stage)

The complete setup of the two series stacked converters, together with their isolation stages feeding a single load in parallel, is shown in Figure 9.11 with the circuit parameters listed in Table 9.5. This is the complete setup of the two converters. The control algorithms, although they were derived for the system shown in Figure 9.8, should be able to control this complete setup to be considered as adequate. For the active rectifiers the control algorithms in Section 7.6.4 – *Control 16*, *Control 32* and *Control 16×2* – are used. The isolation stages are controlled by the PWM controller in Section 7.6.1.

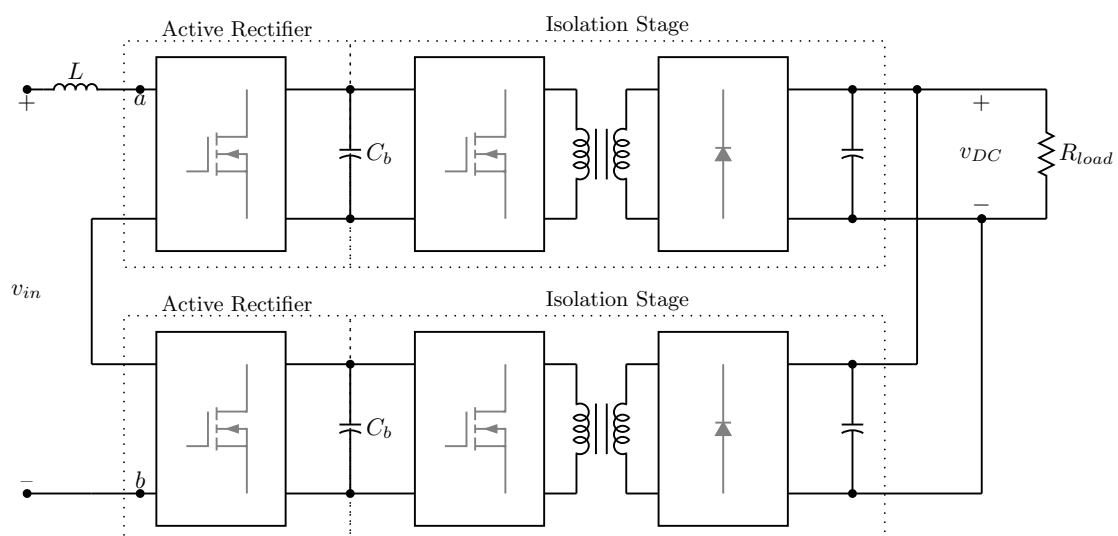


Figure 9.11: Dual, series stacked converters with their isolation stages for a parallel output.

Table 9.5: Dual active rectifiers with the isolation stages.

Parameter	Value	Description
Active Rectifiers		
L	37.5 mH	boost inductor
C	300 μ F	bus- and flying capacitors
T_{pre}	12.5 μ s	prediction period
Isolation Stages		
R_1, R_3, R_4, R_6	10 k Ω	balancing resistors
R_2, R_5	10.7 k Ω	balancing resistors
C	10 μ F	flying capacitors
$\frac{N_2}{N_1}$	$\frac{1}{2}$	transformer winding ratio
C_f	57.8 nF	filter capacitor
L_f	912 μ H	filter inductor
R_{load}	35.5 Ω	load resistor
f_s	40 kHz	switching frequency

9.3.1 Voltage and Current Errors

The voltage and current errors for the three control algorithms were measured. The same definitions for the error values, as in Section 9.2.1, were used here. The results are shown in Figure 9.12.

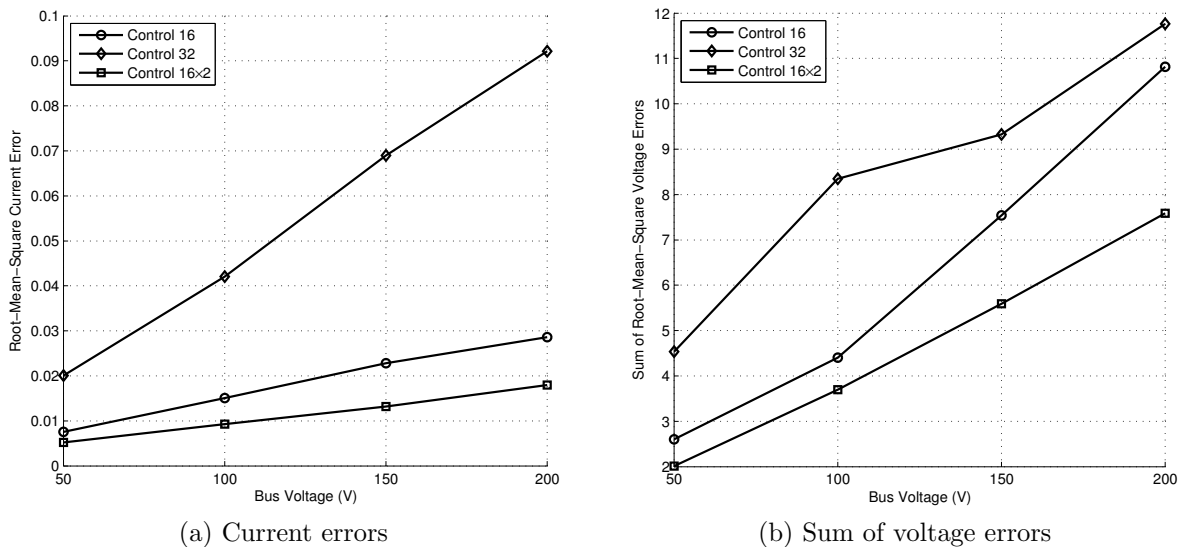


Figure 9.12: The voltage and current errors for the three control algorithms.

The lack in noticeable change in the error values indicate that the isolation stages does not have any effect on the steady-state operation of the converter and any of the three

control algorithms.

9.3.2 Voltage Unbalance

At balanced conditions converter A was loaded with an additional $1.2\text{ k}\Omega$ resistor on its DC bus. This translates to a 30% increase in the power that converter A had to deliver. The resistor was switched in for only an instant to evaluate the transient responses of the internal voltages of the converters. The measurements were taken at a steady-state bus voltage of 100 V per converter.

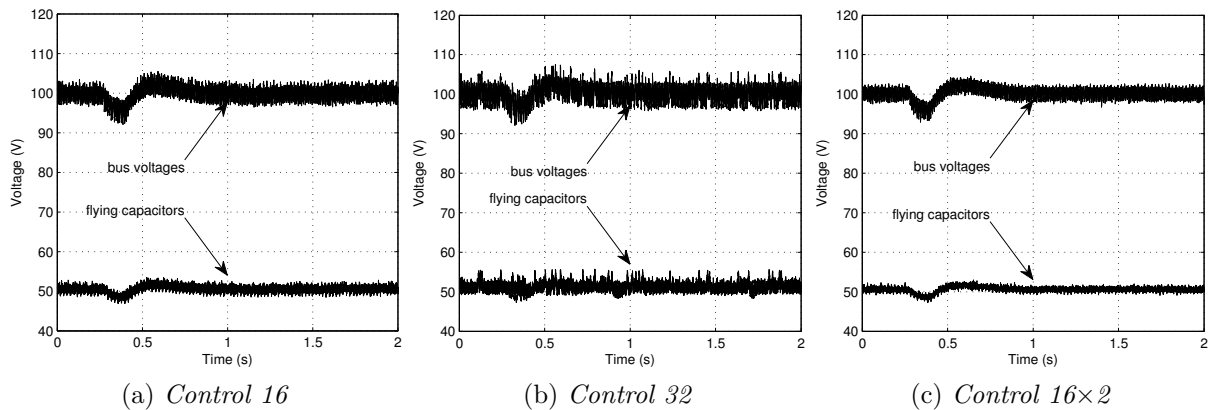


Figure 9.13: Response of internal voltages of dual active rectifiers to an unbalanced load.

All three control algorithms could keep the voltages balanced. When the $1.2\text{ k}\Omega$ resistor was kept switched in, the converters retained their balance in steady-state as well. This indicates that the balancing mechanism [8] obtained from the parallel output aids in the balancing of the bus voltages. The control algorithm need only then balance the flying capacitor voltages.

A moving voltage error value for the momentary disturbance were calculated for each of the control algorithms, again using (9.2.2). The results are shown in Figure 9.14. A window size of 100 samples was used. At sample number 500 the unbalance was introduced at which point the error values of all three control algorithms increased. The results show that *Control 16x2* had the smallest error and that the unbalance affected *Control 32* the worst.

9.3.3 Terminal Voltages

The terminal voltage of the dual converter, as measured between points *a* and *b*, for each of the control algorithms is shown in Figure 9.15. It also shows the sinusoidal input current and voltage. The measurements were taken at a steady-state bus voltage of 100 V

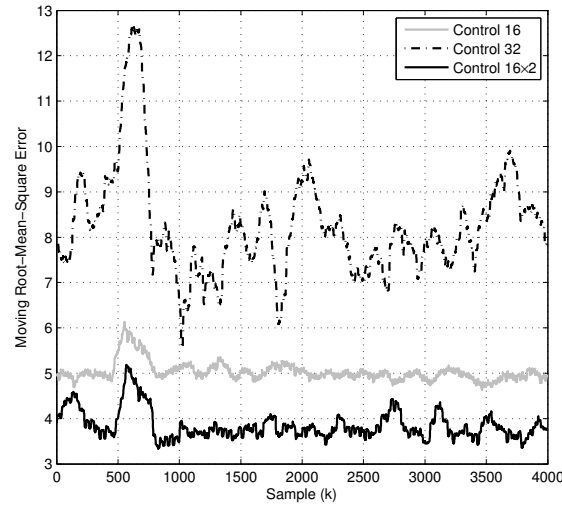


Figure 9.14: Moving RMS error for momentary introduced unbalance of Figures 9.13(a)-(c).

per converter. The current is in-phase with the voltage and the voltage is boosted by 20% so that the converter can output a maximum terminal voltage of 200 V.

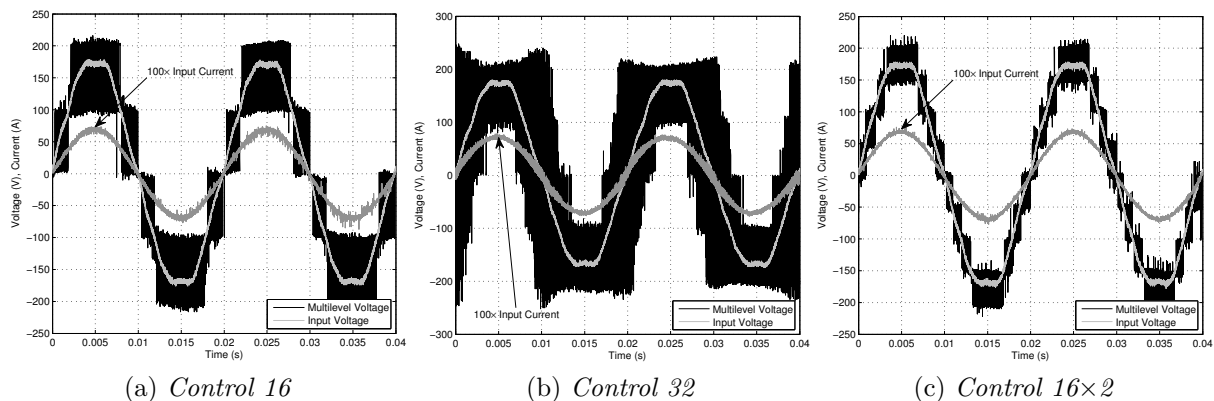


Figure 9.15: The dual active rectifier terminal voltage for the three control algorithms.

The reader is reminded that the full-bridge, three-level converter can output five different voltage levels: v_{bus} , $\frac{v_{bus}}{2}$, 0 , $-\frac{v_{bus}}{2}$ and $-v_{bus}$. *Control 16*, having both converters always switch into the same state, only produce $2v_{bus}$, v_{bus} , 0 , $-v_{bus}$ and $-2v_{bus}$, which is double the values for one converter because of the series stack. *Control 16 \times 2* uses an interleaved switching algorithm and can therefore produce nine voltage levels. The five levels for *Control 16* and the nine levels for *Control 16 \times 2* can clearly be seen in Figures 9.15(a) and 9.15(c), respectively. *Control 32* produces a mixture between five and nine voltage levels.

The nine voltage levels of *Control 16 \times 2* is most likely the reason for its superior current error values. The terminal voltage is already close to sinusoidal and can therefore produce

a current with a smaller ripple because of the smaller voltage transitions on the converter's terminals.

9.3.4 Input Currents

The input currents shown in Figure 9.15 are not perfectly sinusoidal. It does have some harmonic content. Figure 9.16 shows an FFT analysis of the input current of each of the three control algorithms.

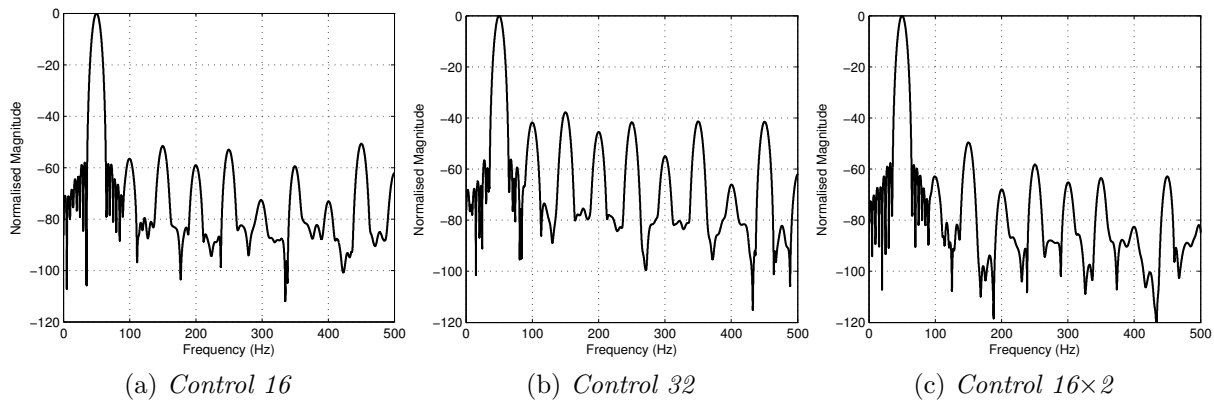


Figure 9.16: FFT analysis of the input currents of the three control algorithms.

From Figure 9.16 it can be seen that *Control 32* has the largest harmonic content. Although *Control 16* and *16x2* has the same harmonics, they are in the order of 20 dB smaller than the corresponding harmonic at *Control 32*. Table 9.6 lists the THD+N values of the input currents for the three algorithms. Harmonics up to 500 Hz were taken into account.

Table 9.6: Input current THD+N.

	<i>Control 16</i>	<i>Control 32</i>	<i>Control 16x2</i>
Current THD+N	0.5%	2.2%	0.4%

9.3.5 Load Step

Using *Control 16x2*, a load step was introduced to test the outer voltage loop. Figure 9.17(a) shows how the bus voltages reacted to the sudden increase in the load. Because a constant amount of input power was available, the bus voltages dropped to reduce the output power. The voltage controller reacted by increasing the current reference to increase the input power and thus increase the bus voltages.

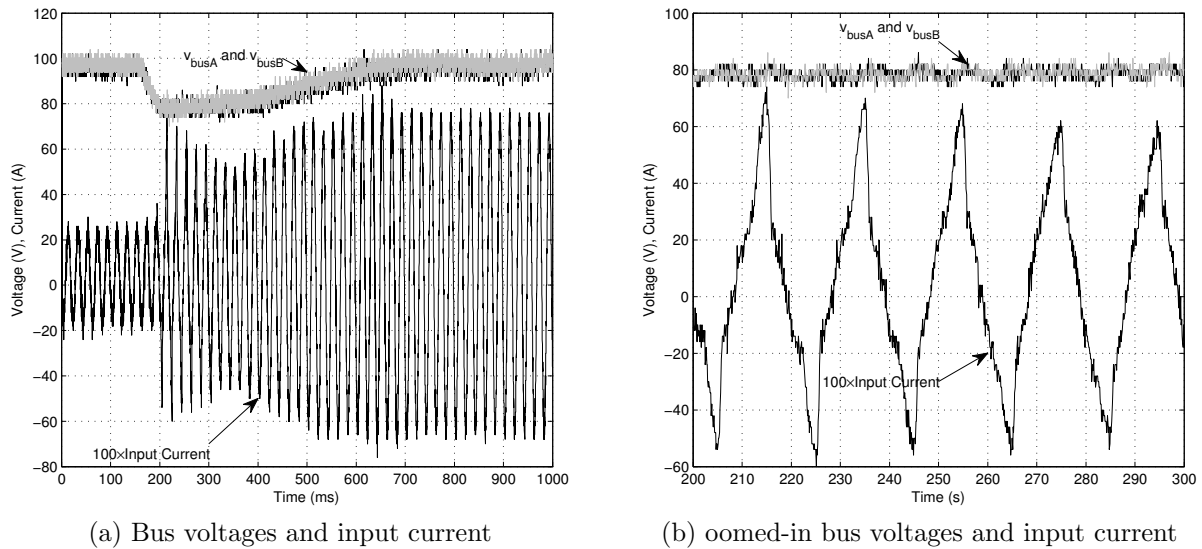


Figure 9.17: Load step for dual converters.

Figure 9.17(b) shows the input current after the bus voltages have dropped. The sum of the voltages dropped below the peak of the input voltage and the MOSFETs anti-parallel diodes therefore became forward biased. The input current could thus not be controlled any more. While the input voltage was less than the sum of bus voltages, the current controller could still control the input current to be sinusoidal. The measurements were taken at a steady-state bus voltage of 100 V per converter.

9.3.6 Current Reference Step

The input currents with reference step for the three control algorithms are shown in Figure 9.18. The measurements were taken at bus voltages of 100 V and the reference step of 20% was done at the peak of the sinusoidal input current. It shows that *Control 16x2* has the most controlled response to reference changes. *Control 32* has large overshoot and excessive ringing with *Control 16* presenting a better response, but still with some ringing. Although the settling times of the three control algorithms does not differ much, the ringing and overshoot of *Control 16* and *Control 32* makes *Control 16x2* the more appropriate controller.

9.3.7 Switching Frequency

An FFT of the switching signal of power switch T_1 of converter A is shown in Figure 9.19. In all three figures the 50 Hz component can be clearly seen. This corresponds to the 50 Hz input current. The harmonics of the 50 Hz is found up to around 2 kHz.

The reader is reminded that all the control algorithms are executed at 80 kHz and that the

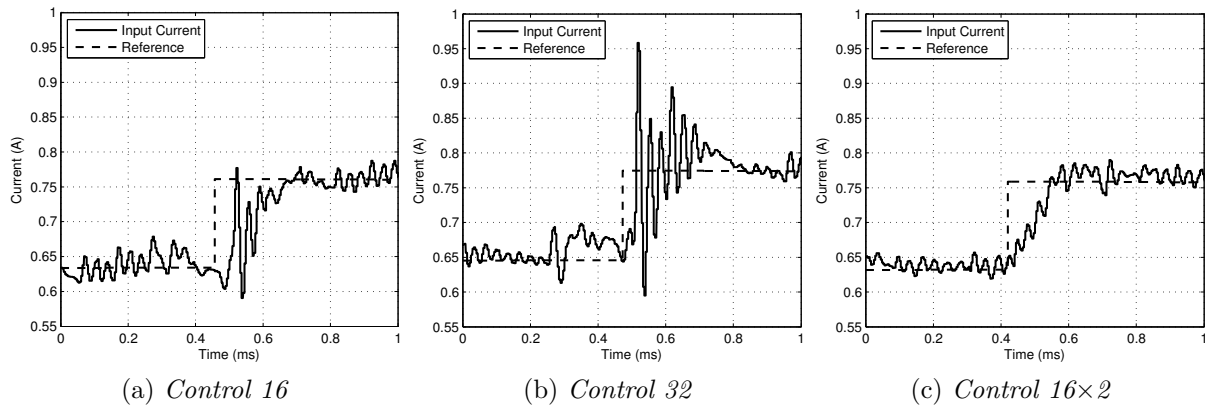
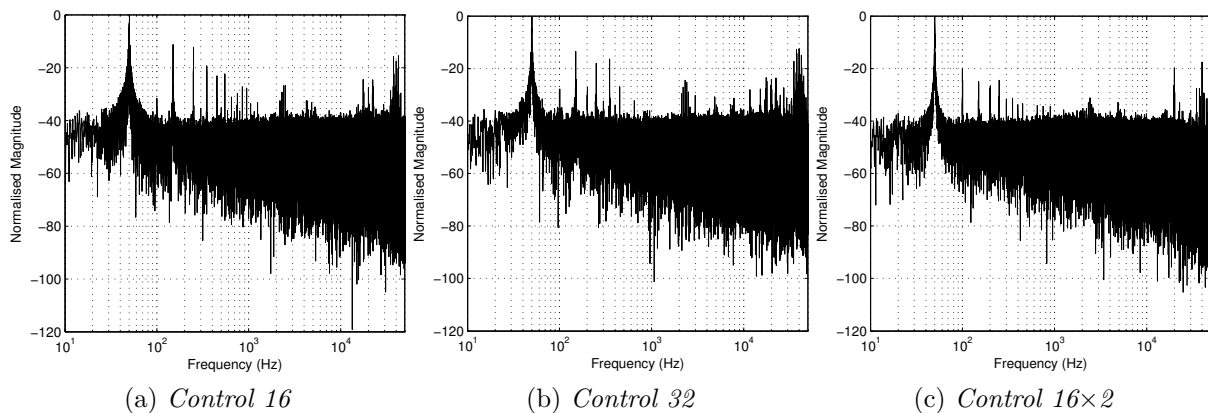


Figure 9.18: Input current responses to a step in their reference.


 Figure 9.19: FFT of the switching signal for switch T_1 for the three control algorithms.

switches therefore have a maximum switching frequency of 40 kHz. *Control 16* and *Control 32* both have a significant 40 kHz harmonic, as well as a 20 kHz harmonic originating from the switching frequency. *Control 16x2* has significant smaller switching harmonics. This is also clear from Table 9.7. It lists the average switching frequencies for switches T_1 , T_2 , T_7 and T_8 for the three control algorithms. The remaining four switches pairs with the listed switches to form the complimentary pairs of switches. The fact that *Control 32* has higher average switching frequencies than the other two control algorithms, show that it must have larger higher order switching harmonics.

Table 9.7: Average switching frequencies of the power switches.

	<i>Control 16</i>	<i>Control 32</i>	<i>Control 16x2</i>
T_1	30.9 kHz	39.4 kHz	24.4 kHz
T_2	26.8 kHz	36.7 kHz	24.4 kHz
T_7	23.9 kHz	30.4 kHz	22.4 kHz
T_8	26.8 kHz	33.5 kHz	22.6 kHz

9.3.8 Efficiency

The efficiencies of the three control algorithms are shown in Figure 9.20. The lower efficiency of *Control 32* could be due to its larger 40 kHz switching harmonic in Figure 9.19(b). The bigger the harmonic and the higher the frequency, the larger the switching losses will be. The lack of large switching harmonics for *Control 16* and *Control 16×2* will reduce their switching losses and therefore increase their efficiencies.

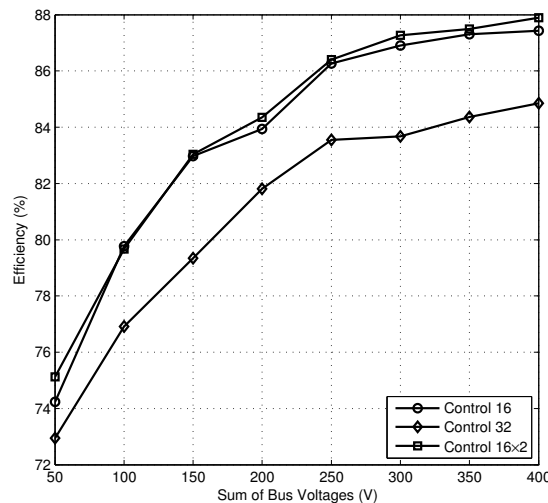


Figure 9.20: Efficiencies of the three control algorithms with a 35.5Ω load.

9.4 Summary

This chapter confirmed the design and implementation of the converter design with various measurement results. A single converter was tested first. It consisted of the active rectifier and isolation stage with its transformer, diode rectifier and LC low pass filter. The sinusoidal input current was of high quality and the predictive controller was able to regulate the flying capacitor voltages of the active rectifier even through unbalanced conditions. The balancing resistors of the isolation stage could balance the flying capacitor voltages satisfactorily.

The dual active rectifiers without the isolation stages were tested next. The isolation stage were replaced by equivalent load resistors. The voltage and current error measurements showed that *Control 32* is the worst control algorithm with *Control 16* and *Control 16×2* more or less the same. *Control 16* could, however, not retain balanced flying capacitor voltages during an introduced unbalanced load. This makes *Control 16×2* the only remaining choice.

Lastly, the dual active rectifiers with isolation stage were measured. The voltage and current error trends were same as for the *without isolation* case. *Control 32* was again affected the worst by an introduced unbalanced load with *Control 16×2* having the best results. *Control 16×2* also had the lowest distortion for its input current. The voltage controller function satisfactorily during load steps and *Control 16×2* again had the best results for current reference steps.

The superiority of *Control 16×2* over the *Control 16* and *Control 32* is argued to be due to its effective double switching frequency. While each converter operates at the same frequency for all three control algorithms, the combined switching state of the two converters changes at double that frequency when controlled by *Control 16×2*.

Chapter 10

Conclusion

This chapter summarises the content of this thesis, draws some conclusions from results obtained and provides areas in which future work can be conducted.

10.1 Summary of Study

The use of series-input converters is an effective way to increase the operating voltage of a converter beyond that of a single power switch. The disadvantage of such converters is the complex controllers needed. Fortunately, the balancing of the bus voltages occurs naturally which reduces the complexity of the control algorithms. Furthermore, the combination of the series-input and parallel-output converters, as in Figure 2.4, has the advantage of providing the user with a low voltage DC bus that could be used for industrial applications.

The diode-clamped and flying-capacitor converters were introduced as alternatives to the full-bridge converters of [8]. Using only pulse-width modulation techniques, the internal voltages of the active rectifiers could not be balanced under all conditions. The look-up table controller implemented on the flying-capacitor converter proved satisfactory to balance the internal voltages of the converter. It has already been proved that a back-to-back topology for the diode-clamped converter has the ability to balance the capacitor voltages, but has the disadvantage of the large amount of active devices that are needed. To be able to only use a single ended converter, diode-clamped or flying-capacitor, a controller that is more sophisticated than PWM is needed. The use of predictive control was therefore proposed to directly utilise the redundant switching states of the converters.

The finite-state, model predictive controller is easily implemented on power electronic converter due to their discrete switching states. The predictive controller is built around using the redundancy in the amount of switching states to deliver far better results than

a PWM controller – in the case of the multilevel converters, FS-MPC was able to balance the internal voltages of the controller where a PWM controller could not.

This study chose the flying-capacitor converter to prove the concept of stacking these converters in series. Model-based predictive control was used to control the stack of two converters. The viability of extending the two converter stack for a medium voltage application should be commented upon.

10.2 Conclusions

10.2.1 Controller Hardware

The measurement circuits consisted of voltage divider resistors, an isolation op-amp, and fully differential op-amp to transmit the measurement to the ADC on the FPGA host board. A problem arose from the fact that the ADC only had a 2 V peak-to-peak input. The output of the isolation op-amp is very noisy due to its internal switching. Even with the prescribed filters, the noise overpowered the measurements. This would not have been a problem if the ADC had a larger range, e.g. 5 V. The isolation op-amp was therefore removed. The differential measurement voltage divider resistors and instrumentation amplifier had a large enough range to measure all the necessary voltages.

The FPGA proved adequate for implementing all the control algorithms. With some coding optimisations it should still be adequate to control a series stack of converter large enough for medium voltage applications.

10.2.2 Control Algorithms

The fixed duty cycle, PWM controlled isolation stage proved suitable for the application in this thesis. This should, however, be extended to closed-loop control of the output voltage for a truly SST application. Because the DC output of all the isolation stages will feed a three-phase inverter, the output voltage should be controlled as this will vary with load changes.

Control 16 was not always able to regulate the flying capacitor voltages. This excludes it as a viable solution for controlling a series stack of converters. *Control 32* always had the largest voltage and current errors. This leaves *Control 16×2* as the controller of choice. It presented the smallest voltage and current errors, smallest total harmonic distortion for the input current, and highest efficiency.

The smaller error values and THD measurement is argued to be due to its effective double switching frequency. While each converter operates at the same frequency for all three

control algorithms, the combined switching state of the two converters changes at double that frequency when controlled by *Control 16×2*. This makes the voltage and current ripples smaller and therefore reducing the error values. *Control 16×2* also utilises all nine voltage levels at its terminals. This will also aid in producing a low THD input current.

The average switching frequency of the switches, when controlled by *Control 16×2*, was lower than with the other control algorithms. This will explain the higher efficiency. *Control 32* had the highest average switching frequencies and therefore the lowest efficiency.

The question whether *Control 16×2* could control a larger stack of converters still remains. *Control 16×2* interleaves its predictions; thus, for an N -converter series stack, the time between predictions will be $\frac{T_{pre}}{N}$. The implementation of *Control 16×2* in this thesis took 350 ns to complete its predictions. Lets assume this can be reduced to 200 ns and the prediction period is increased from 12.5 μ s to 25 μ s. This makes the switching frequency 20 kHz instead of 40 kHz. The 20 kHz should still be sufficient for good results. If we want to keep the time spent on doing the predictions to less than 10% of the time between predictions, the maximum number of series stacked converters is 12. Theoretically this is sufficient to solve the problem of the large amount of cells needed in the SST. Taking into account that each three-level converter will replace two full-bridge converter cells a new SST will have the equivalent of 24 full-bridge cells. This is more than the current implementation of [5, 9, 10].

The controllers proposed in this thesis, specifically *Control 16×2*, should therefore be suitable for controlling an arbitrary number of series stacked multilevel converters.

10.2.3 Converter Hardware

Only one recommendation regarding the converter hardware needs to be made. The converter itself, the active rectifier and isolation stage, presented no problems and the design can be kept similar for future implementations. The MOSFET driver circuitry did, however, present problems. At times the bootstrap supply was unable to power the driver circuits of the upper MOSFETs. This happened when the bootstrap capacitors were discharged below the voltage threshold of the MOSFET driver. The result was total failure of the control algorithm to keep the input current and flying capacitor voltages controlled. In some instances this even lead to the failure of some of the MOSFETs themselves.

The failure of the bootstrap supply is partly due to the predictive controller. The unpredictable switching waveforms of the power switches makes the design of the bootstrap capacitors difficult. The primary cause, however, is the fact that very large capacitors are needed to power the driver circuits for a full 50 Hz cycle. This makes the bootstrap supply

unrealistic and an isolated power supply for each MOSFET driver should preferably be used. The bootstrap supply can still be used for the isolation stage as it does not have the low, i.e. 50 Hz, fundamental switching frequency.

10.3 Further Work

First, a new MOSFET driver board should be designed for the active rectifier. This is to replace the bootstrap supply used in the current design.

Then the stack of two converters can be extended to an arbitrary amount. A measurement system should be designed that can send the measurements of each cell to the digital controller on which the predictive control algorithm is implemented. It is proposed that each cell have its own controller that takes measurements and sends it to the main controller, and receives the switching state information from the main controller to relay to the power switches.

The predictive control algorithms proved to be good choice for controlling the flying-capacitor active rectifiers. This should be kept as it is a relative simple control technique and is relatively straightforward to implement. The control law for the isolation stage should, however, be improved. Although it was adequate for this proof-of-concept project, it could easily be extended to a closed-loop controller. A measurement of the DC output voltage should be taken and used to control the duty cycle at which the isolation stage is operated. The range of the allowable duty cycles should, however, be limited if the balancing resistors are still to be used. The flying capacitor voltages of the isolation stage will be balanced at slight offsets from the ideal values if the duty cycle is changed. By limiting the duty cycle range, this offset can also be limited within reasonable boundaries.

Bibliography

- [1] J. Brooks, “Solid state transformer concept development,” Naval Material Command, Civil Engineering Laboratory, Naval Construction Battalion Center, Port Hueneme, CA, Tech. Rep., 1980.
- [2] L. Heinemann and G. Mauthe, “The universal power electronics based distribution transformer, an unified approach,” in *IEEE Power Electronics Specialists Conference*, vol. 2, 2001, pp. 504–509.
- [3] J.-S. Lai, A. Maitra, and F. Goodman, “Performance of a distribution intelligent universal transformer under source and load disturbances,” in *Conference Record of the Industry Applications Conference*, vol. 2, Oct. 2006, pp. 719–725.
- [4] E. Ronan, S. Sudhoff, S. Glover, and D. Galloway, “A power electronic-based distribution transformer,” in *IEEE Transactions on Power Delivery*, vol. 17, no. 2, Apr. 2002, pp. 537–543.
- [5] M. Wolf, “Design and implementation of a modular converter with application to a solid state transformer,” Master’s thesis, Stellenbosch University, Oct. 2009.
- [6] J. van der Merwe and H. du T. Mouton, “The solid-state transformer concept: A new era in power distribution,” in *AFRICON*, Sep. 2009, pp. 1–6.
- [7] W. van der Merwe and T. Mouton, “Natural balancing of the two-cell back-to-back multilevel converter with specific application to the solid-state transformer concept,” in *IEEE Conference on Industrial Electronics and Applications*, May 2009, pp. 2955–2960.
- [8] W. van der Merwe, “Natural balancing mechanisms in converters,” Ph.D. dissertation, Stellenbosch University, Mar. 2011.
- [9] L. M. Schietekat, “Design and implementation of the main controller of a solid-state transformer,” Master’s thesis, Stellenbosch University, Dec. 2011.

- [10] C. F. Breet, "Cell control and measurement system design for implementation in a solid-state transformer," Master's thesis, Stellenbosch University, To Be Completed 2011.
- [11] W. van der Merwe and T. Mouton, "Solid-state transformer topology selection," in *IEEE International Conference on Industrial Technology*, Feb. 2009, pp. 1–6.
- [12] J.-S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," in *IEEE Transactions on Industry Applications*, vol. 32, no. 3, May 1996, pp. 509–517.
- [13] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," in *IEEE Transactions on Industry Applications*, vol. IA-17, no. 5, Sep. 1981, pp. 518–523.
- [14] W.-K. Lee, S.-Y. Kim, J.-S. Yoon, and D.-H. Baek, "A comparison of the carrier-based PWM techniques for voltage balance of flying capacitor in the flying capacitor multilevel inverter," in *IEEE Applied Power Electronics Conference and Exposition*, Mar. 2006.
- [15] E. Christopher and M. Sumner, "Voltage balance control for a multilevel interface for renewable energy systems," in *International Power Electronics and Motion Control Conference*, Sep. 2006, pp. 189–193.
- [16] Z. Pan, F. Z. Peng, K. Corzine, V. Stefanovic, J. Leuthen, and S. Gataric, "Voltage balancing control of diode-clamped multilevel rectifier/inverter systems," in *IEEE Transactions on Industry Applications*, vol. 41, no. 6, Nov. 2005, pp. 1698–1706.
- [17] A. Shukla, A. Ghosh, and A. Joshi, "Capacitor voltage balancing schemes in flying capacitor multilevel inverters," in *IEEE Power Electronics Specialists Conference*, Jun. 2007, pp. 2367–2372.
- [18] Z. Pan and F. Z. Peng, "A sinusoidal PWM method with voltage balancing capability for diode-clamped five-level converters," in *IEEE Transactions on Industry Applications*, vol. 45, no. 3, May 2009, pp. 1028–1034.
- [19] L. Grzesiak and J. Tomasik, "Novel DC link balancing scheme in five-level back-to-back converter system," in *The International Conference on Computer as a Tool*, Sep. 2007, pp. 1929–1934.
- [20] F. Defay, A.-M. Llor, and M. Fadel, "A predictive control with flying capacitor balancing of a multicell active power filter," in *IEEE Transactions on Industrial Electronics*, vol. 55, no. 9, Sep. 2008, pp. 3212–3220.

- [21] P. Cortes, J. Rodriguez, S. Alepuz, S. Busquets-Monge, and J. Bordonau, "Finite-states model predictive control of a four-level diode-clamped inverter," in *IEEE Power Electronics Specialists Conference*, Jun. 2008, pp. 2203–2208.
- [22] E. Silva, B. McGrath, D. Quevedo, and G. Goodwin, "Predictive control of a flying capacitor converter," in *American Control Conference*, Jul. 2007, pp. 3763–3768.
- [23] J. Hu, L. Zhang, and S. Watkins, "Active power filtering by a flying-capacitor multi-level inverter with capacitor voltage balance," in *IEEE International Symposium on Industrial Electronics*, Jul. 2008, pp. 2348–2352.
- [24] F. Defay, A. Llor, and M. Fadel, "Direct control strategy for a flying capacitor converter," in *European Conference on Power Electronics and Applications*, Sep. 2009, pp. 1–9.
- [25] F. Defay, A.-M. Llor, and M. Fadel, "Direct control strategy for a four-level three-phase flying-capacitor inverter," in *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, Jul. 2010, pp. 2240–2248.
- [26] P. Lezana, R. Aguilera, and D. Quevedo, "Model predictive control of an asymmetric flying capacitor converter," in *IEEE Transactions on Industrial Electronics*, vol. 56, no. 6, Jun. 2009, pp. 1839–1846.
- [27] H. du Toit Mouton, "Natural balancing of three-level neutral-point-clamped PWM inverters," in *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, Oct. 2002, pp. 1017–1025.
- [28] H. Mouton, J. Enslin, and H. Akagi, "Natural balancing of series-stacked power quality conditioners," in *IEEE Transactions on Power Electronics*, vol. 18, no. 1, Jan. 2003, pp. 198–207.
- [29] R. Wilkinson, T. Meynard, and H. du Toit Mouton, "Natural balance of multicell converters: The general case," in *IEEE Transactions on Power Electronics*, vol. 21, no. 6, Nov. 2006, pp. 1658–1666.
- [30] J.-S. Lai, A. Maitra, A. Mansoor, and F. Goodman, "Multilevel intelligent universal transformer for medium voltage applications," in *Conference Record of the Industry Applications Conference*, vol. 3, Oct. 2005, pp. 1893–1899.
- [31] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power electronics*, 3rd ed. United States of America: John Wiley and Sons, 2003.

- [32] M. Kang, P. Enjeti, and I. Pitel, "Analysis and design of electronic transformers for electric power distribution system," in *IEEE Transactions on Power Electronics*, vol. 14, no. 6, Nov. 1999, pp. 1133–1141.
- [33] W. van der Merwe and T. Mouton, "Natural balancing of the modular AC/DC converter," in *Annual Conference of the IEEE Industrial Electronics Society*, Nov. 2011.
- [34] S. Thielemans, A. Ruderman, B. Reznikov, and J. Melkebeek, "Five-level H-bridge flying capacitor converter voltage balance dynamics analysis," in *IEEE International Symposium on Industrial Electronics*, Jul. 2010, pp. 826–831.
- [35] R. Wilkinson, "Natural balancing of multicell converters," Ph.D. dissertation, Stellenbosch University, Dec. 2004.
- [36] B. McGrath and D. Holmes, "Natural capacitor voltage balancing for a flying capacitor converter induction motor drive," in *IEEE Transactions on Power Electronics*, vol. 24, no. 6, Jun. 2009, pp. 1554–1561.
- [37] J. Holtz, "Self-commutated power converter with stair cased output voltage for high power and high switching frequency," in *Siemens Research and Development Report*, 1977, pp. 146–171.
- [38] J. Casteel and R. Hoft, "Optimum PWM waveforms of a microprocessor controller inverter," in *IEEE Power Electronics Specialists Conference*, 1978.
- [39] A. Schönung and D. Stemmelr, "Static frequency changer with subharmonic control in conjunction with reversible variable drives," in *Brown Boveri Rev.*, Aug. 1964.
- [40] X. Yuan and I. Barbi, "A new diode clamping multilevel inverter," in *Applied Power Electronics Conference and Exposition*, vol. 1, Mar. 1999, pp. 495–501.
- [41] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," in *IEEE Transactions on Power Electronics*, vol. 15, no. 2, Mar. 2000, pp. 242–249.
- [42] J. Pou, R. Pindado, D. Boroyevich, and P. Rodriguez, "Limits of the neutral-point balance in back-to-back-connected three-level converters," in *IEEE Transactions on Power Electronics*, vol. 19, no. 3, May 2004, pp. 722–731.
- [43] D. Zhou, "A self-balancing space vector switching modulator for three-level motor drives," in *IEEE Transactions on Power Electronics*, vol. 17, no. 6, Nov. 2002, pp. 1024–1031.

- [44] D. H. Lee, S. Lee, and F. Lee, "An analysis of midpoint balance for the neutral-point-clamped three-level VSI," in *IEEE Power Electronics Specialists Conference*, vol. 1, May 1998, pp. 193–199.
- [45] F. Z. Peng, J.-S. Lai, J. McKeever, and J. VanCoevering, "A multilevel voltage-source converter system with balanced DC voltages," in *IEEE Power Electronics Specialists Conference*, vol. 2, Jun. 1995, pp. 1144–1150.
- [46] L. Grzesiak and J. Tomasik, "Novel DC link balancing scheme in generic n-level back-to-back converter system," in *International Conference on Power Electronics*, Oct. 2007, pp. 1044–1049.
- [47] D. Holmes and T. Lipo, *Pulse Width Modulation for Power Converters*. United States of America: John Wiley and Sons, 2003.
- [48] T. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *IEEE Power Electronics Specialists Conference*, vol. 1, Jun. 1992, pp. 397–403.
- [49] T. Meynard, H. Foch, P. Thomas, J. Courault, R. Jakob, and M. Nahrstaedt, "Multicell converters: basic concepts and industry applications," in *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, Oct. 2002, pp. 955–964.
- [50] L. Xu and V. Agelidis, "Active capacitor voltage control of flying capacitor multilevel converters," in *IEE Proceedings - Electric Power Applications*, vol. 151, no. 3, May 2004, pp. 313–320.
- [51] A. Shukla, A. Ghosh, and A. Joshi, "Improved multilevel hysteresis current regulation and capacitor voltage balancing schemes for flying capacitor multilevel inverter," in *IEEE Transactions on Power Electronics*, vol. 23, no. 2, Mar. 2008, pp. 518–529.
- [52] S.-G. Lee, D.-W. Kang, Y.-H. Lee, and D.-S. Hyun, "The carrier-based PWM method for voltage balance of flying capacitor multilevel inverter," in *IEEE Power Electronics Specialists Conference*, vol. 1, 2001, pp. 126–131.
- [53] S. Thielemans, A. Ruderman, and J. Melkebeek, "Self-precharge in single-leg flying capacitor converters," in *IEEE Annual Conference of Industrial Electronics*, Nov. 2009, pp. 812–817.
- [54] S. Thielemans, A. Ruderman, B. Reznikov, and J. Melkebeek, "Self-precharge for single-leg odd-level multilevel converter," in *IET International Conference on Power Electronics, Machines and Drives*, Apr. 2010, pp. 1–6.

- [55] B.-R. Lin and Y.-L. Hou, "High-power-factor single-phase capacitor clamped rectifier," in *IEE Proceedings - Electric Power Applications*, vol. 148, no. 2, Mar. 2001, pp. 214–224.
- [56] J. Rossiter, *Model-based Predictive Control: A Practical Approach*. United States of America: CRC Press, 2003.
- [57] J. Holtz, "Pulsewidth modulation for electronic power conversion," in *Proceedings of the IEEE*, vol. 82, no. 8, Aug. 1994, pp. 1194–1214.
- [58] J. W. Eaton and J. B. Rawlings, "Model-predictive control of chemical processes," in *Chemical Engineering Science*, vol. 47, no. 4, 1992, pp. 705–720.
- [59] J. G. V. Antwerp and R. D. Braatz, "Model predictive control of large scale processes," in *Process Control*, vol. 10, no. 1, 2000, pp. 1–8.
- [60] P. Cortes, M. Kazmierkowski, R. Kennel, D. Quevedo, and J. Rodriguez, "Predictive control in power electronics and drives," in *IEEE Transactions on Industrial Electronics*, vol. 55, no. 12, Dec. 2008, pp. 4312–4324.
- [61] J. Holtz and S. Stadtfeld, "A predictive controller for the stator current vector of AC machines fed from a switched voltage source," in *International Power Electronics Conference*, 1983, pp. 1665–1675.
- [62] M. Depenbrock, "Direct self-control (DSC) of inverter-fed induction machine," in *IEEE Transactions on Power Electronics*, vol. 3, no. 4, Oct. 1988, pp. 420–429.
- [63] I. Takahashi and T. Noguchi, "A new quick-response and high-efficiency control strategy of an induction motor," in *IEEE Transactions on Industry Applications*, vol. IA-22, no. 5, Sep. 1986, pp. 820–827.
- [64] P. Mutschler, "A new speed-control method for induction motors," in *Power Conversion Intelligent Motion*, May 1998, pp. 131–136.
- [65] H. Le-Huy, K. Slimani, and P. Viarouge, "Analysis and implementation of a real-time predictive current controller for permanent-magnet synchronous servo drives," in *IEEE Transactions on Industrial Electronics*, vol. 41, no. 1, Feb. 1994, pp. 110–117.
- [66] L. Springob and J. Holtz, "High-bandwidth current control for torque-ripple compensation in PM synchronous machines," in *IEEE Transactions on Industrial Electronics*, vol. 45, no. 5, Oct. 1998, pp. 713–721.

- [67] J. Chen, A. Prodic, R. Erickson, and D. Maksimovic, "Predictive digital current programmed control," in *IEEE Transactions on Power Electronics*, vol. 18, no. 1, Jan. 2003, pp. 411–419.
- [68] L. Malesani, P. Mattavelli, and S. Buso, "Robust dead-beat current control for PWM rectifiers and active filters," in *IEEE Transactions on Industry Applications*, vol. 35, no. 3, May 1999, pp. 613–620.
- [69] S.-G. Jeong and M.-H. Woo, "DSP-based active power filter with predictive current control," in *IEEE Transactions on Industrial Electronic*, vol. 44, no. 3, Jun. 1997, pp. 329–336.
- [70] J. Mossoba and P. Lehn, "A controller architecture for high bandwidth active power filters," in *IEEE Transactions on Power Electronics*, vol. 18, no. 1, Jan. 2003, pp. 317–325.
- [71] S. Buso, S. Fasolo, and P. Mattavelli, "Uninterruptible power supply multiloop control employing digital predictive voltage and current regulators," in *IEEE Transactions on Industry Applications*, vol. 37, no. 6, Nov. 2001, pp. 1846–1854.
- [72] P. Mattavelli, "An improved deadbeat control for UPS using disturbance observers," in *IEEE Transactions on Industrial Electronics*, vol. 52, no. 1, Feb. 2005, pp. 206–212.
- [73] A. Nasiri, "Digital control of three-phase series-parallel uninterruptible power supply systems," in *IEEE Transactions on Power Electronics*, vol. 22, no. 4, Jul. 2007, pp. 1116–1127.
- [74] S. Saggini, W. Stefanutti, E. Tedeschi, and P. Mattavelli, "Digital deadbeat control tuning for DC-DC converters using error correlation," in *IEEE Transactions on Power Electronics*, vol. 22, no. 4, Jul. 2007, pp. 1566–1570.
- [75] P. Correa, M. Pacas, and J. Rodriguez, "Predictive torque control for inverter-fed induction machines," in *IEEE Transactions on Industrial Electronics*, vol. 54, no. 2, Apr. 2007, pp. 1073–1079.
- [76] O. Kukrer, "Discrete-time current control of voltage-fed three-phase PWM inverters," in *IEEE Transactions on Power Electronics*, vol. 11, no. 2, Mar. 1996, pp. 260–269.
- [77] C. Garcia, D. Preth, and M. Morari, "Model predictvie control: Theory and practice - a survey," in *Automatica*, May 1989, pp. 335–348.
- [78] D. Mayne, J. Rawlings, C. Rao, and P. Scokaert, "Constrained model predictive control: Optimality and stability," in *Automatica*, Jun. 2000, pp. 789–814.

- [79] A. Linder and R. Kennel, "Model predictive control for electrical drives," in *IEEE Power Electronics Specialists Conference*, 2005, pp. 1793–1799.
- [80] J. Rodriguez, J. Pontt, C. Silva, M. Salgado, S. Rees, U. Ammann, P. Lezana, R. Huerta, and P. Cortes, "Predictive control of three-phase inverter," in *Electronics Letters*, vol. 40, no. 9, Apr. 2004, pp. 561–563.
- [81] A. Linder and R. Kennel, "Direct model predictive control - a new direct predictive control strategy for electrical drives," in *European Conference on Power Electronics and Applications*, 2005.
- [82] J. Rodriguez, J. Pontt, C. A. Silva, P. Correa, P. Lezana, P. Cortes, and U. Ammann, "Predictive current control of a voltage source inverter," in *IEEE Transactions on Industrial Electronics*, vol. 54, no. 1, Feb. 2007, pp. 495–503.
- [83] G. Perantzakis, F. Xepapas, S. Papathanassiou, and S. Manias, "A predictive current control technique for three-level NPC voltage source inverters," in *IEEE Power Electronics Specialists Conference*, Jun. 2005, pp. 1241–1246.
- [84] R. Vargas, P. Cortes, U. Ammann, J. Rodriguez, and J. Pontt, "Predictive control of a three-phase neutral-point-clamped inverter," in *IEEE Transactions on Industrial Electronics*, vol. 54, no. 5, Oct. 2007, pp. 2697–2705.
- [85] G. Perantzakis, F. Xepapas, and S. Manias, "Efficient predictive current control technique for multilevel voltage source inverters," in *European Conference on Power Electronics and Applications*, Sep. 2005.
- [86] J. Rodriguez, J. Pontt, P. Correa, P. Lezana, and P. Cortes, "Predictive power control of an AC/DC/AC converter," in *Conference Record of the Industry Applications Conference*, vol. 2, Oct. 2005, pp. 934–939.
- [87] S. Muller, U. Ammann, and S. Rees, "New time-discrete modulation scheme for matrix converters," in *IEEE Transactions on Industrial Electronics*, vol. 52, no. 6, Dec. 2005, pp. 1607–1615.
- [88] M. Catucci, J. Clare, and P. Wheeler, "Predictive control strategies for zcs direct converter hv power supply," in *European Conference on Power Electronics and Applications*, Sep. 2005.
- [89] M. Catucci, J. Clare, and P. Wheeler, "Predictive control strategy for ZCS single stage resonant converter," in *IEEE Annual Conference on Industrial Electronics*, Nov. 2006, pp. 2905–2910.

- [90] H. Dang, P. Wheeler, and J. Clare, "A control analysis and implementation of high voltage, high frequency direct power converter," in *IEEE Annual Conference on Industrial Electronics*, Nov. 2006, pp. 2096–2102.
- [91] D. Zill and M. Cullen, *Advanced Engineering Mathematics*. Sudbury, Massachusetts: Jones and Bartlett, 2000.
- [92] A. Tsirukis and M. Morari, "Controller design with actuator constraints," in *IEEE Conference on Decision and Control*, vol. 3, 1992, pp. 2623–2628.
- [93] S. A. Molepo, "A multilevel inverter for DC reticulation," Master's thesis, Stellenbosch University, Apr. 2003.
- [94] EPCOS. (2006, Sep.) EPCOS ETD 54/28/19 Core and Accessories. [Online]. Available: <http://www.epcos.com>
- [95] EPCOS. (2006, Sep.) SIFERRIT Material N97. [Online]. Available: <http://www.epcos.com>
- [96] R. Aguilera and D. Quevedo, "Capacitor voltage estimation for predictive control algorithm of flying capacitor converters," in *IEEE International Conference on Industrial Technology*, Feb. 2009, pp. 1–6.
- [97] M. Tomlinson, "Power electronic inverter for synchronising an alternative power source to the grid," Dec. 2009, final Year Project, Stellenbosch University.
- [98] Altera. (2010, Jan.) Cyclone III device handbook. [Online]. Available: <http://www.altera.com>
- [99] N. Semiconducotr. (1998, Jul.) An overview of LVDS technology. [Online]. Available: <http://www.national.com>

Appendices

Appendix A

Cost Analysis

This chapter contains a breakdown of the comparative cost analysis shown in Chapter 1. It is only *comparative*, because not all component costs are taken into account. Only the cost of the cell controllers, power switches, bus capacitors, and blocking capacitors and diodes are considered. This chapter will give an explanation for the quantities of the components in the cost breakdown.

A.1 Cells

The 6.6 kV-to-400 V three-phase solid-state transformer constructed by [5,9,10] consisted of 36 full-bridge cells and cell controllers. The three-level converters will each replace two full-bridge converters. Therefore, the diode-clamped and flying-capacitor SSTs will consist of 18 cells each. The diode-clamped and flying-capacitor SSTs will also have 18 cell controllers. At R1 500.00 each, the cost of the cell controllers are R54 000 for the full-bridge topology and R27 000.00 for the diode-clamped and flying-capacitor topologies.

Table A.1: Cost Analysis: Number of cells for each SST topology.

	Full-Bridge	Flying-Capacitor	Diode-Clamped
Cells	36	18	18
Controllers	36	18	18
	R54 000	R27 000	R27 000

A.2 Power Switches

Each cell of the SST consists of an active rectifier and isolation stage. For the full-bridge converter SST topology, four switches for both the rectifier and isolation stage are needed.

The diode-clamped and flying-capacitor converters requires eight switches for both their active rectifiers and isolation stages.

The total number of power switches required by the full-bridge topology is:

$$\begin{aligned} n &= (\text{number of cells}) \times (\text{switches for rectifier} + \text{switches for isolation stage}) \\ &= 36 \times (4 + 4) \\ &= 288 \end{aligned} \tag{A.2.1}$$

The total number of power switches required by the diode-clamped and flying-capacitor topologies are:

$$\begin{aligned} n &= (\text{number of cells}) \times (\text{switches for rectifier} + \text{switches for isolation stage}) \\ &= 18 \times (8 + 8) \\ &= 288 \end{aligned} \tag{A.2.2}$$

Table A.2: Cost Analysis: Number of power switches for each SST topology.

	Full-Bridge	Flying-Capacitor	Diode-Clamped
800 V, 20 A Transistors	288	288	288

A.3 Capacitors

The bus capacitance for each cell is required to be $300 \mu\text{F}$ rated at 800 V. $60 \mu\text{F}$ capacitors rated at 800 V are available at R105.45 each. The flying capacitors of the flying-capacitor converter topology are also required to be $300 \mu\text{F}$, each rated at 400 V. $100 \mu\text{F}$, 450 V capacitors are available at R122.40 each.

The full-bridge and flying-capacitor topologies does not require a neutral point in the bus capacitor. Therefore, five $60 \mu\text{F}$ capacitors in parallel will provide the required capacitance. The diode-clamped topology, however, does require a neutral point. Its bus capacitance could therefore be made up out of two groups of 450 V capacitors in series. Each group should be six $100 \mu\text{F}$ capacitors in parallel to have a total bus capacitance of $300 \mu\text{F}$.

Each cell of the flying-capacitor topology has two flying capacitors for both the active rectifier and isolation stage. Furthermore, each flying capacitor will have to consist of three $100 \mu\text{F}$ capacitors.

The total number of 60 μF , 800 V capacitors required by the full-bridge SST topology are:

$$\begin{aligned} n &= (\text{number of cells}) \times (\text{capacitors per bus}) \\ &= 36 \times 5 \\ &= 180 \end{aligned} \tag{A.3.1}$$

The total number of 60 μF , 800 V capacitors required by the flying-capacitor SST topology are:

$$\begin{aligned} n &= (\text{number of cells}) \times (\text{capacitors per bus}) \\ &= 18 \times 5 \\ &= 90 \end{aligned} \tag{A.3.2}$$

The diode-clamped topology does not require any 60 μF , 800 V capacitors and the full-bridge topology does not require any 100 μF , 450 V capacitors. The total number of 100 μF , 450 V capacitors required by the flying-capacitor SST topology are:

$$\begin{aligned} n &= (\text{number of cells}) \times (\text{number of flying capacitors}) \times (\text{capacitors per flying capacitor}) \\ &= 18 \times 4 \times 3 \\ &= 216 \end{aligned} \tag{A.3.3}$$

The total number of 100 μF , 450 V capacitors required by the diode-clamped SST topology are:

$$\begin{aligned} n &= (\text{number of cells}) \times (\text{number of bus capacitors}) \times (\text{capacitors per bus capacitor}) \\ &= 18 \times 2 \times 6 \\ &= 216 \end{aligned} \tag{A.3.4}$$

Table A.3: Cost Analysis: Number of capacitors for each SST topology.

	Full-Bridge	Flying-Capacitor	Diode-Clamped
60 μF , 800 V Capacitors	180 R19 000	90 R9 500	0 0
100 μF , 450 V Capacitors	0 0	216 R26 000	216 R26 000

A.4 Diodes

The diode-clamped topology is the only one that requires clamping diodes. Two diodes for each phase-leg are required and the active rectifier and isolation stage have both two legs. The diodes are R 40.00 each.

The total number of clamping diodes required are therefore:

$$\begin{aligned}
 n &= (\text{number of cells}) \times (\text{number of phase-legs}) \times (\text{diodes per leg}) \\
 &= 18 \times 4 \times 3 \\
 &= 144
 \end{aligned} \tag{A.4.1}$$

Table A.4: Cost Analysis: Number of diodes for each SST topology.

	Full-Bridge	Flying-Capacitor	Diode-Clamped
400 V, 20 A Diodes	0	0	144
	0	0	R5 750

Appendix B

Converter Modelling

In Section 4.2.1 the sixteen different switching states in which the converter can exist is listed. These states each have an equivalent circuit associated with it that can be used to derive a discrete model of the converter.

In this chapter the sixteen equivalent circuits of the converter will be given and the prediction equations will be derived.

B.1 Approximation Methods

The predictions of the controlled variables are done at fixed sampling times T_s . The continuous state space or transfer function model of the converter should therefore be discretised. Linear models are trivial to discretise, but the converter has inductors and capacitors whose voltage-current relations are differential equations. These should be approximated, the simplest methods being the Euler forward and backwards method.

Euler forward:

$$\frac{dx}{dt} \approx \frac{x(k+1) - x(k)}{T_s}$$

$$x(k+1) = x(k) + T_s \cdot f(x(k), u(k)) \quad (\text{B.1.1})$$

This is easy to implement but could be unstable for large T_s .

Euler backwards:

$$\frac{dx}{dt} \approx \frac{x(k) - x(k-1)}{T_s}$$

$$x(k) = x(k-1) + T_s \cdot f(x(k), u(k))$$

$$x(k+1) = x(k) + T_s \cdot f(x(k+1), u(k+1)) \quad (\text{B.1.2})$$

This is more stable than the forwards approximation, but is not always possible to implement.

The sampling frequency of the predictive controller is 80 kHz. It is assumed that this is fast enough so that the Euler forward approximation method can be used.

B.2 Flying-Capacitor Converter Modelling

The single converter has four variables that need to be controlled: $i_L(t)$, $v_{bus}(t)$, $v_1(t)$ and $v_2(t)$. The derivation of the prediction equations for the dual converter is just a combination of the equations for the two single converters. Only the single converter derivation will therefore be shown.

B.2.1 State 1

T_1 , T_2 , T_7 and T_8 are turned on. The equivalent circuit is shown in Figure B.1.

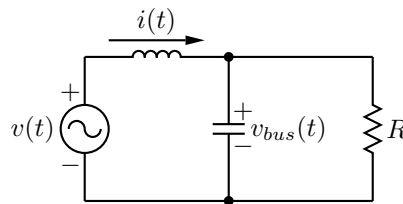


Figure B.1: State 1

The voltage-current relationship for the input inductor is:

$$v(t) = L \cdot \frac{di(t)}{dt} \quad (\text{B.2.1})$$

Expanding the voltage term the following is obtained:

$$\begin{aligned} v(t) - v_{bus}(t) &= L \cdot \frac{di(t)}{dt} \\ v(k) - v_{bus}(k) &\approx L \cdot \frac{i(k+1) - i(k)}{T_s} \\ i(k+1) &= \frac{T_s}{L}(v(k) - v_{bus}(k)) + i(k) \end{aligned} \quad (\text{B.2.2})$$

The voltage-current relationship for the DC bus capacitor is:

$$i(t) = L \cdot \frac{dv(t)}{dt} \quad (\text{B.2.3})$$

Expanding the current term the following is obtained:

$$\begin{aligned}
 i(t) - \frac{v_{bus}(t)}{R} &= C \cdot \frac{dv(t)}{dt} \\
 i(k) - \frac{v_{bus}(k)}{R} &\approx C \cdot \frac{v_{bus}(k+1) - v_{bus}(k)}{T_s} \\
 v_{bus}(k+1) &= \frac{T_s}{C} \cdot i(k) - \frac{T_s}{RC} \cdot v_{bus}(k) + v_{bus}(k)
 \end{aligned} \tag{B.2.4}$$

The flying capacitors does not carry any significant current and thus their voltages will remain constant.

$$v_1(k+1) \approx v_1(k) \tag{B.2.5}$$

$$v_2(k+1) \approx v_2(k) \tag{B.2.6}$$

B.2.2 State 2(a)

T_2 , T_4 , T_7 and T_8 are turned on. The equivalent circuit is shown in Figure B.2.

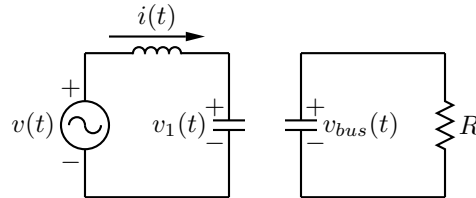


Figure B.2: State 2(a)

$$i(k+1) = \frac{T_s}{L} \cdot (v(k) - v_1(k)) + i(k) \tag{B.2.7}$$

$$v_{bus}(k+1) = -\frac{T_s}{RC} \cdot v_{bus}(k) + v_{bus}(k) \tag{B.2.8}$$

$$v_1(k+1) = \frac{T_s}{C} \cdot i(k) + v_1(k) \tag{B.2.9}$$

$$v_2(k+1) = v_2(k) \tag{B.2.10}$$

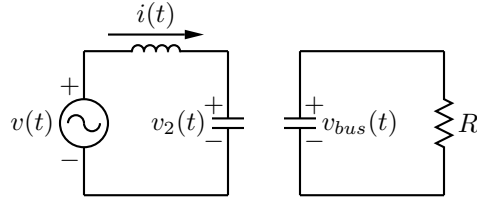


Figure B.3: State 2(b)

B.2.3 State 2(b)

T_1 , T_2 , T_5 and T_7 are turned on. The equivalent circuit is shown in Figure B.3.

$$i(k+1) = \frac{T_s}{L} \cdot (v(k) - v_2(k)) + i(k) \quad (\text{B.2.11})$$

$$v_{bus}(k+1) = -\frac{T_s}{RC} \cdot v_{bus}(k) + v_{bus}(k) \quad (\text{B.2.12})$$

$$v_1(k+1) = v_1(k) \quad (\text{B.2.13})$$

$$v_2(k+1) = \frac{T_s}{C} \cdot i(k)v_2(k) \quad (\text{B.2.14})$$

B.2.4 State 2(c)

T_1 , T_3 , T_7 and T_8 are turned on. The equivalent circuit is shown in Figure B.4.

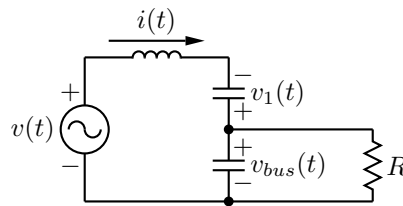


Figure B.4: State 2(c)

$$i(k+1) = \frac{T_s}{L} \cdot (v(k) + v_1(k) - v_{bus}(k)) + i(k) \quad (\text{B.2.15})$$

$$v_{bus}(k+1) = \frac{T_s}{C} \cdot i(k) - \frac{T_s}{RC} \cdot v_{bus}(k) + v_{bus}(k) \quad (\text{B.2.16})$$

$$v_1(k+1) = -\frac{T_s}{C} \cdot i(k) + v_1(k) \quad (\text{B.2.17})$$

$$v_2(k+1) = v_2(k) \quad (\text{B.2.18})$$

B.2.5 State 2(d)

T_1 , T_2 , T_6 and T_8 are turned on. The equivalent circuit is shown in Figure B.5.

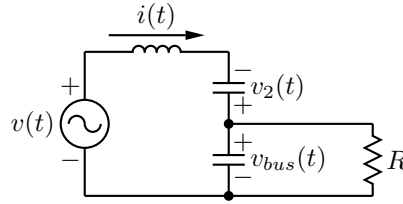


Figure B.5: State 2(d)

$$i(k+1) = \frac{T_s}{L} \cdot (v(k) + v_2(k) - v_{bus}(k)) + i(k) \quad (\text{B.2.19})$$

$$v_{bus}(k+1) = \frac{T_s}{C} \cdot i(k) - \frac{T_s}{RC} \cdot v_{bus}(k) + v_{bus}(k) \quad (\text{B.2.20})$$

$$v_1(k+1) = v_1(k) \quad (\text{B.2.21})$$

$$v_2(k+1) = -\frac{T_s}{C} \cdot i(k) + v_2(k) \quad (\text{B.2.22})$$

B.2.6 State 3(a)+(b)

T_1 , T_2 , T_5 and T_6 or T_3 , T_4 , T_7 and T_8 are turned on. The equivalent circuit is shown in Figure B.6. Both states 3(a) and 3(b) will result in the same equivalent circuit and thus the states can be grouped together.

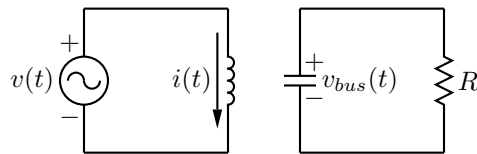


Figure B.6: State 3(a)+(b)

$$i(k+1) = \frac{T_s}{L} \cdot v(k) + i(k) \quad (\text{B.2.23})$$

$$v_{bus}(k+1) = -\frac{T_s}{RC} \cdot v_{bus}(k) + v_{bus}(k) \quad (\text{B.2.24})$$

$$v_1(k+1) = v_1(k) \quad (\text{B.2.25})$$

$$v_2(k+1) = v_2(k) \quad (\text{B.2.26})$$

B.2.7 State 3(c)

T_2 , T_4 , T_6 and T_8 are turned on. The equivalent circuit is shown in Figure B.7.

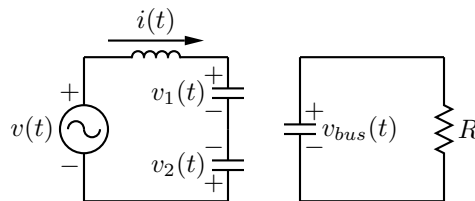


Figure B.7: State 3(c)

$$i(k+1) = \frac{T_s}{L} \cdot (v(k) - v_1(k) + v_2(k)) + i(k) \quad (\text{B.2.27})$$

$$v_{bus}(k+1) = -\frac{T_s}{RC} \cdot v_{bus}(k) + v_{bus}(k) \quad (\text{B.2.28})$$

$$v_1(k+1) = \frac{T_s}{C} \cdot i(k) + v_1(k) \quad (\text{B.2.29})$$

$$v_2(k+1) = -\frac{T_s}{C} \cdot i(k) + v_2(k) \quad (\text{B.2.30})$$

B.2.8 State 3(d)

T_1 , T_3 , T_5 and T_7 are turned on. The equivalent circuit is shown in Figure B.8.

$$i(k+1) = \frac{T_s}{L} \cdot (v(k) + v_1(k) - v_2(k)) + i(k) \quad (\text{B.2.31})$$

$$v_{bus}(k+1) = -\frac{T_s}{RC} \cdot v_{bus}(k) + v_{bus}(k) \quad (\text{B.2.32})$$

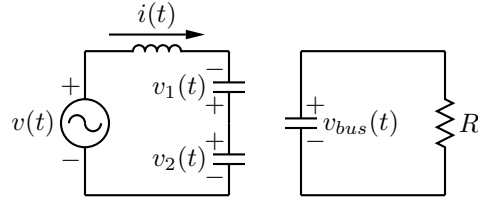


Figure B.8: State 3(d)

$$v_1(k+1) = -\frac{T_s}{C} \cdot i(k) + v_1(k) \quad (\text{B.2.33})$$

$$v_2(k+1) = \frac{T_s}{C} \cdot i(k) + v_2(k) \quad (\text{B.2.34})$$

B.2.9 State 3(e)

T_2 , T_4 , T_5 and T_7 are turned on. The equivalent circuit is shown in Figure B.9.

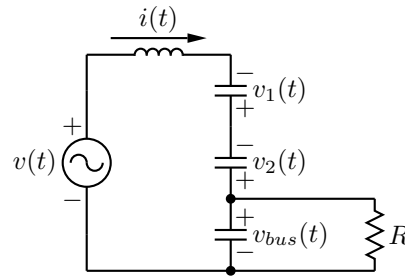


Figure B.9: State 3(e)

$$i(k+1) = \frac{T_s}{L} \cdot (v(k) + v_1(k) + v_2(k) - v_{bus}(k)) + i(k) \quad (\text{B.2.35})$$

$$v_{bus}(k+1) = \frac{T_s}{C} \cdot i(k) - \frac{T_s}{RC} \cdot v_{bus}(k) + v_{bus}(k) \quad (\text{B.2.36})$$

$$v_1(k+1) = -\frac{T_s}{C} \cdot i(k) + v_1(k) \quad (\text{B.2.37})$$

$$v_2(k+1) = -\frac{T_s}{C} \cdot i(k) + v_2(k) \quad (\text{B.2.38})$$

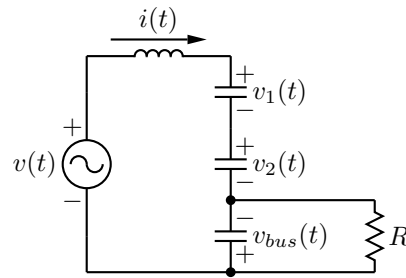


Figure B.10: State 3(f)

B.2.10 State 3(f)

T_1 , T_3 , T_6 and T_8 are turned on. The equivalent circuit is shown in Figure B.10.

$$i(k+1) = \frac{T_s}{L} \cdot (v(k) - v_1(k) - v_2(k) + v_{bus}(k)) + i(k) \quad (\text{B.2.39})$$

$$v_{bus}(k+1) = -\frac{T_s}{C} \cdot i(k) - \frac{T_s}{RC} \cdot v_{bus}(k) + v_{bus}(k) \quad (\text{B.2.40})$$

$$v_1(k+1) = \frac{T_s}{C} \cdot i(k) + v_1(k) \quad (\text{B.2.41})$$

$$v_2(k+1) = \frac{T_s}{C} \cdot i(k) + v_2(k) \quad (\text{B.2.42})$$

B.2.11 State 4(a)

T_1 , T_3 , T_5 and T_6 are turned on. The equivalent circuit is shown in Figure B.11.

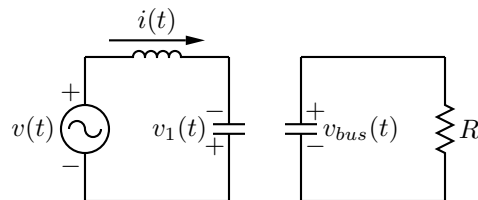


Figure B.11: State 4(a)

$$i(k+1) = \frac{T_s}{L} \cdot (v(k) + v_1(k)) + i(k) \quad (\text{B.2.43})$$

$$v_{bus}(k+1) = -\frac{T_s}{RC} \cdot v_{bus}(k) + v_{bus}(k) \quad (\text{B.2.44})$$

$$v_1(k+1) = -\frac{T_s}{C} \cdot i(k) + v_1(k) \quad (\text{B.2.45})$$

$$v_2(k+1) = v_2(k) \quad (\text{B.2.46})$$

B.2.12 State 4(b)

T_3 , T_4 , T_6 and T_8 are turned on. The equivalent circuit is shown in Figure B.12.

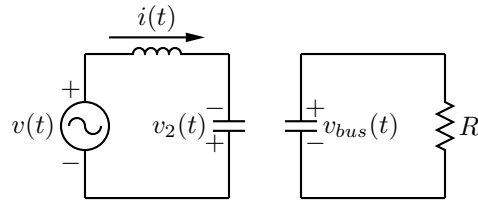


Figure B.12: State 4(b)

$$i(k+1) = \frac{T_s}{L} \cdot (v(k) + v_2(k)) + i(k) \quad (\text{B.2.47})$$

$$v_{bus}(k+1) = -\frac{T_s}{RC} \cdot v_{bus}(k) + v_{bus}(k) \quad (\text{B.2.48})$$

$$v_1(k+1) = v_1(k) \quad (\text{B.2.49})$$

$$v_2(k+1) = -\frac{T_s}{C} \cdot i(k) + v_2(k) \quad (\text{B.2.50})$$

B.2.13 State 4(c)

T_2 , T_4 , T_5 and T_6 are turned on. The equivalent circuit is shown in Figure B.13.

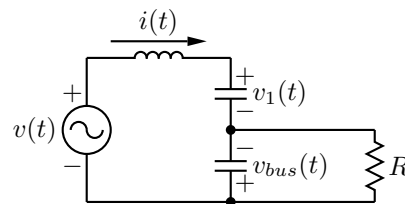


Figure B.13: State 4(c)

$$i(k+1) = \frac{T_s}{L} \cdot (v(k) - v_1(k) + v_{bus}(k)) + i(k) \quad (\text{B.2.51})$$

$$v_{bus}(k+1) = -\frac{T_s}{C} \cdot i(k) - \frac{T_s}{RC} \cdot v_{bus}(k) + v_{bus}(k) \quad (\text{B.2.52})$$

$$v_1(k+1) = \frac{T_s}{C} \cdot i(k) + v_1(k) \quad (\text{B.2.53})$$

$$v_2(k+1) = v_2(k) \quad (\text{B.2.54})$$

B.2.14 State 4(d)

T_3 , T_4 , T_5 and T_7 are turned on. The equivalent circuit is shown in Figure B.14.

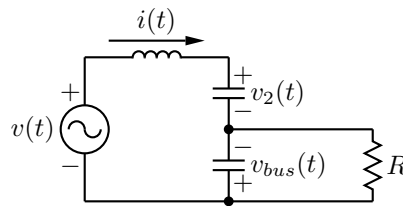


Figure B.14: State 4(d)

$$i(k+1) = \frac{T_s}{L} \cdot (v(k) - v_2(k) + v_{bus}(k)) + i(k) \quad (\text{B.2.55})$$

$$v_{bus}(k+1) = -\frac{T_s}{C} \cdot i(k) - \frac{T_s}{RC} \cdot v_{bus}(k) + v_{bus}(k) \quad (\text{B.2.56})$$

$$v_1(k+1) = v_1(k) \quad (\text{B.2.57})$$

$$v_2(k+1) = \frac{T_s}{C} \cdot i(k) + v_2(k) \quad (\text{B.2.58})$$

B.2.15 State 5

T_3 , T_4 , T_5 and T_6 are turned on. The equivalent circuit is shown in Figure B.15.

$$i(k+1) = \frac{T_s}{L} \cdot (v(k) + v_{bus}(k)) + i(k) \quad (\text{B.2.59})$$

$$v_{bus}(k+1) = -\frac{T_s}{C} \cdot i(k) - \frac{T_s}{RC} \cdot v_{bus}(k) + v_{bus}(k) \quad (\text{B.2.60})$$

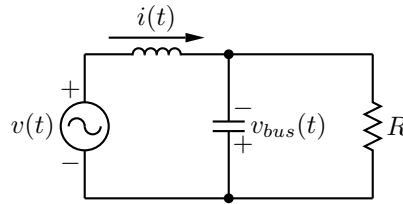


Figure B.15: State 5

$$v_1(k+1) = v_1(k) \quad (\text{B.2.61})$$

$$v_2(k+1) = v_2(k) \quad (\text{B.2.62})$$

B.3 Converter State-Space Models

The predictive control algorithms in Section 7.6 uses different configurations of the prediction equations derived in Section B.2 of this chapter. The single converter is controlled using these equations directly. The $i(k)$, $v_{bus}(k)$, $v_1(k)$ and $v_2(k)$ are the four state of the fourth-order state-space model used for the single converter. Sixteen fourth-order models completely describes the converter, one for each switching state. The state-space model for *State 1* in Section B.2.1 is shown in (B.3.1).

$$\begin{aligned} \mathbf{x}(k+1) &= \mathbf{A}\mathbf{x}(k) + \mathbf{B}u(k) \\ \begin{bmatrix} i(k+1) \\ v_{bus}(k+1) \\ v_1(k+1) \\ v_2(k+1) \end{bmatrix} &= \begin{bmatrix} 1 & -\frac{T_s}{L} & 0 & 0 \\ \frac{T_s}{C} & 1 - \frac{T_s}{RC} & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i(k) \\ v_{bus}(k) \\ v_1(k) \\ v_2(k) \end{bmatrix} + \begin{bmatrix} \frac{T_s}{L} \\ 0 \\ 0 \\ 0 \end{bmatrix} v(k) \end{aligned} \quad (\text{B.3.1})$$

This fourth-order model is the same used by *Control 32* and *Control 16×2*. *Control 256* and *Control 16* uses a seventh-order model which is the combined fourth-order models for the two active rectifiers. The states of the seventh-order model are divided as $i(k)$, $v_{bus(A)}(k)$, $v_{1(A)}(k)$, $v_{2(A)}(k)$, $v_{bus(B)}(k)$, $v_{1(B)}(k)$ and $v_{2(B)}(k)$. Equation B.3.2 shows the seventh-order state-space model for the dual active rectifiers when both converters are switched into *State 1*.

$$\begin{aligned}
 \mathbf{x}(k+1) &= \mathbf{A}\mathbf{x}(k) + \mathbf{B}u(k) \\
 \begin{bmatrix} i(k+1) \\ v_{bus(A)}(k+1) \\ v_{1(A)}(k+1) \\ v_{2(A)}(k+1) \\ v_{bus(B)}(k+1) \\ v_{1(B)}(k+1) \\ v_{2(B)}(k+1) \end{bmatrix} &= \begin{bmatrix} 1 & -\frac{T_s}{L} & 0 & 0 & -\frac{T_s}{L} & 0 & 0 \\ \frac{T_s}{C} & 1 - \frac{T_s}{RC} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ \frac{T_s}{C} & 0 & 0 & 0 & 1 - \frac{T_s}{RC} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i(k) \\ v_{bus(A)}(k) \\ v_{1(A)}(k) \\ v_{2(A)}(k) \\ v_{bus(B)}(k) \\ v_{1(B)}(k) \\ v_{2(B)}(k) \end{bmatrix} + \begin{bmatrix} \frac{T_s}{L} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} v(k)
 \end{aligned} \tag{B.3.2}$$

Constructing the seventh-order model from the two fourth-order models are illustrated in Figure B.16. The fourth-order model of *Converter A* are extended by adding the parts of the fourth-order model of *Converter B*. The figure depicts how the extensions are arranged.

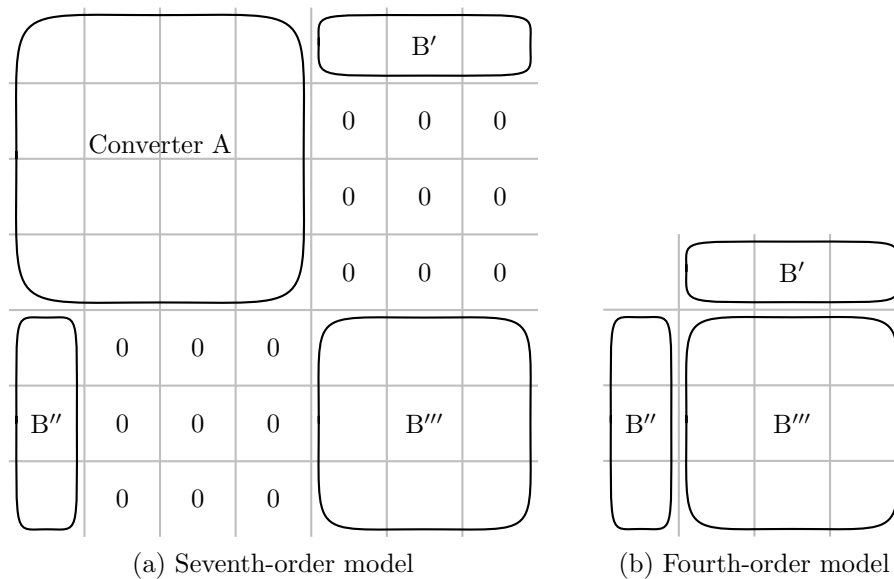


Figure B.16: Constructing the seventh-order model for the dual active rectifiers from the two fourth-order models.

Appendix C

PCB Schematics

This chapter contains the schematics for the printed circuit boards. They are divided into the measurement boards, converter hardware; FPGA board and optic transmitters board.

C.1 Measurement Boards

Pages *CURRENT MEASUREMENT* and *GENERIC VOLTAGE MEASUREMENT* are the schematics for the measurement boards. They contain the measurement resistors, instrumentation op-amp, isolated op-amp and its power supply, low pass filter, and fully differential op-amp.

C.2 Converter Hardware

Pages *POWER CONVERTER* and *PASSIVE RECTIFIER* contain the circuits for the actual converter hardware. The flying capacitors, bus capacitors, MOSFETs, terminals for the transformer, diode rectifier, and filter inductor and capacitor are all included.

Page *ISOLATION POWER SUPPLY* is the schematic for the 35 V source for the bootstrap supply. Pages *DRIVER CIRCUITS (1 OF 2)* and *DRIVER CIRCUITS (2 OF 2)* shows the bootstrap supplies and driver circuits. The active rectifier and isolation stage both have eight power switches arranged in two legs of four switches. Pages *DRIVER CIRCUITS (1 OF 2)* and *DRIVER CIRCUITS (2 OF 2)* will each drive one leg of four power switches.

C.3 FPGA Board

Page *REGULATORS* shows the regulators for the FPGA board. The +12 V and -12 V inputs are relayed to the measurement boards. The 5 V input is regulated down to 1.2 V, 2.5 V and 3.3 V for powering the various parts of the FPGA.

Pages *DIFFERENTIAL OPAMPS PART 1 - ADC INPUTS* and *DIFFERENTIAL OPAMPS PART 2 - ADC INPUTS* shows the differential buffers for the ADC inputs. The differential measurements comes from the measurement boards to the buffers and then goes to the ADC shown on page *ADC + LEVEL SHIFTER*.

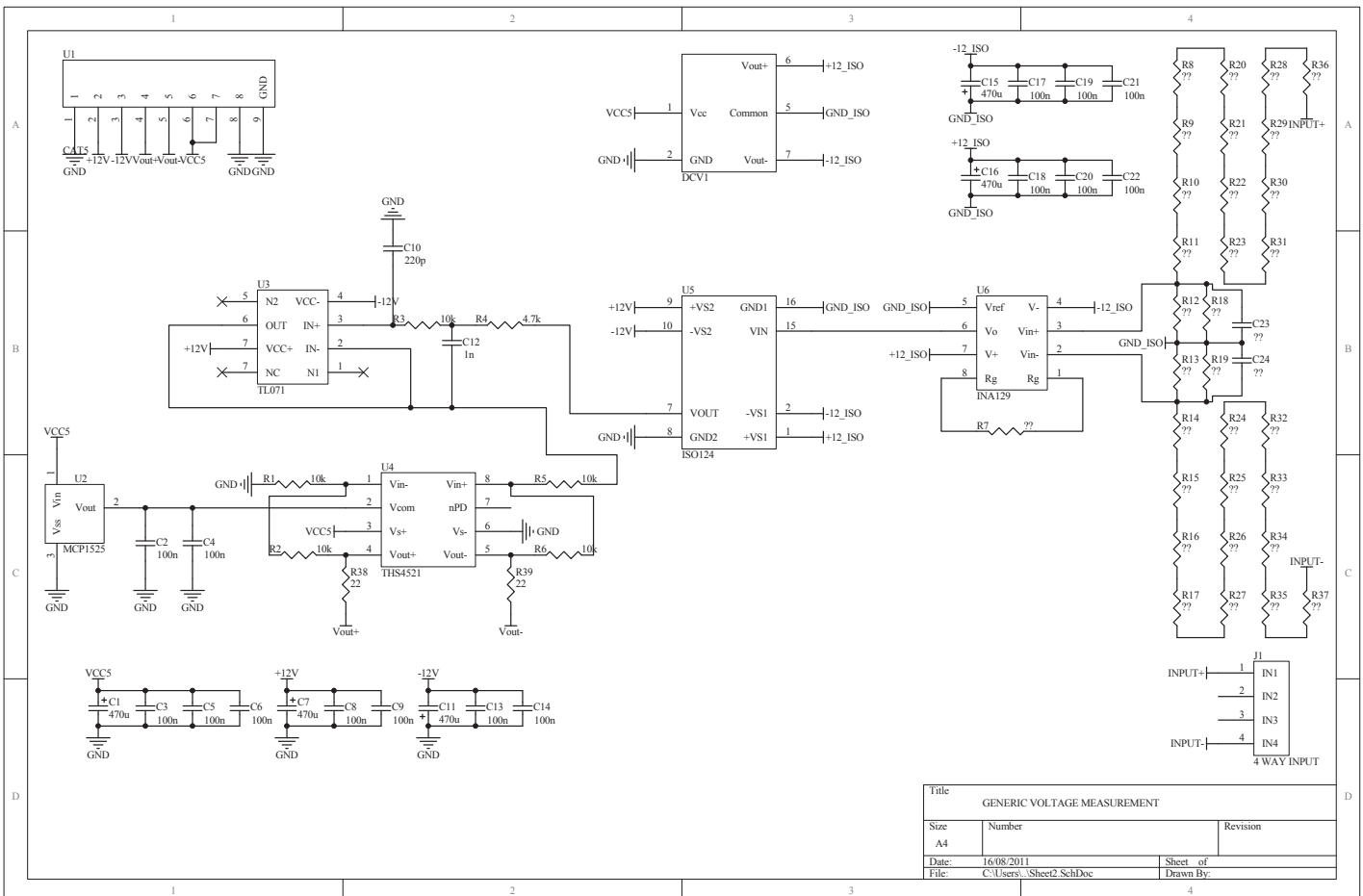
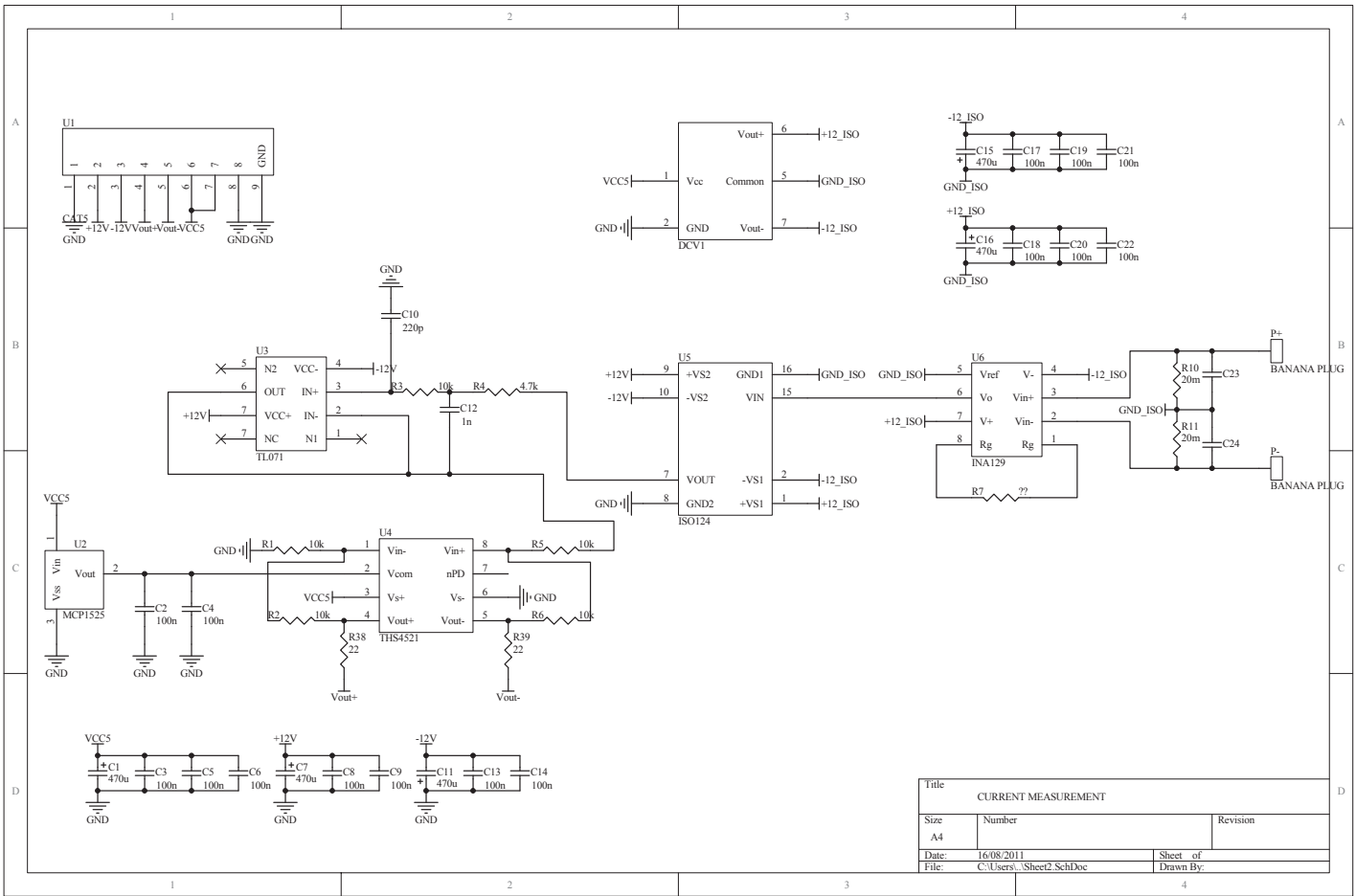
Page *ADC COMMON MODE BEFFERS AND OPTIC FIBRE DRIVERS* shows the level shifters for the optic fibre transmitters. The FPGA can only output 2.5 V, while the transmitters require 5 V. The level shifters translates between the different voltage levels.

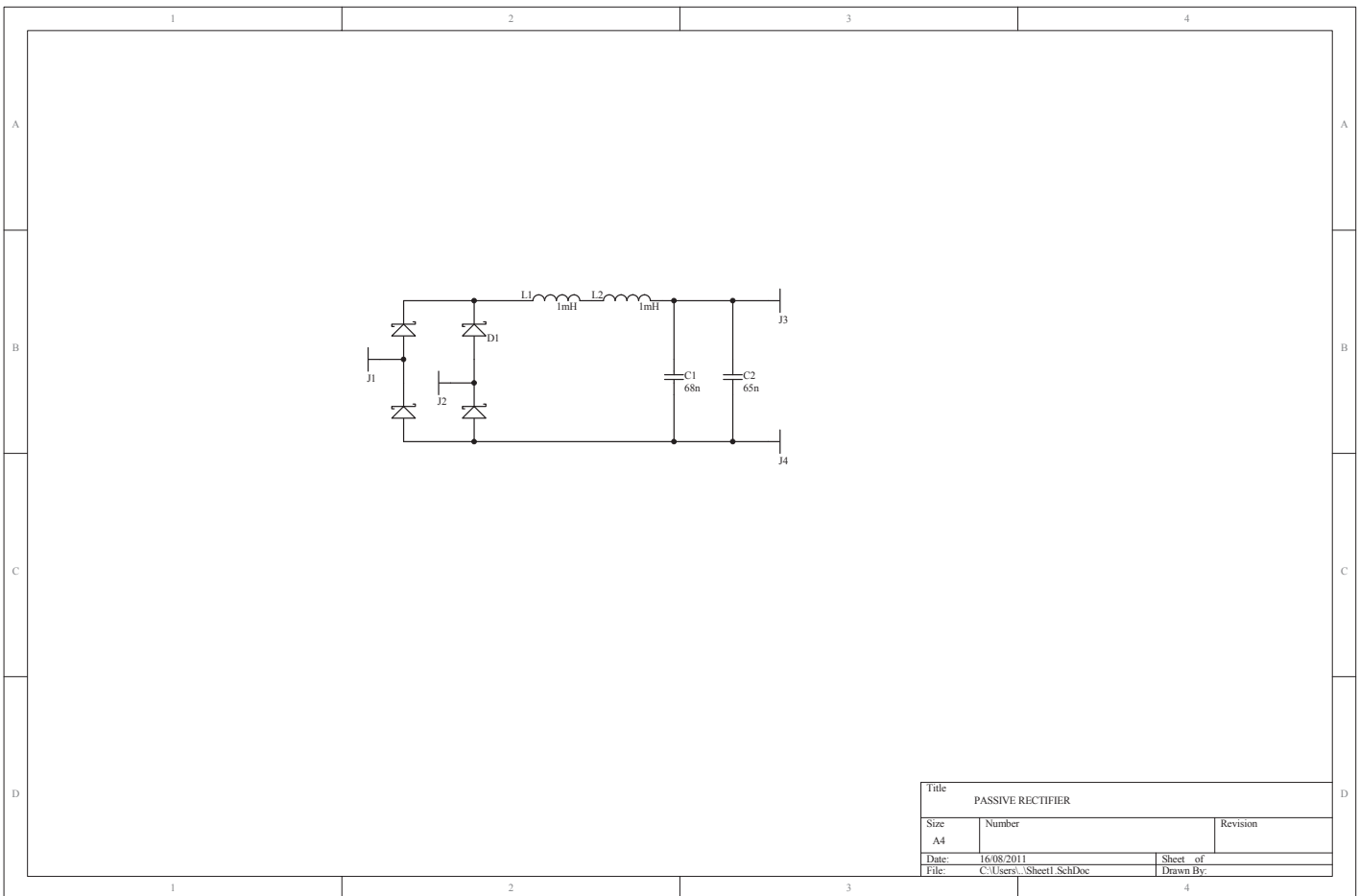
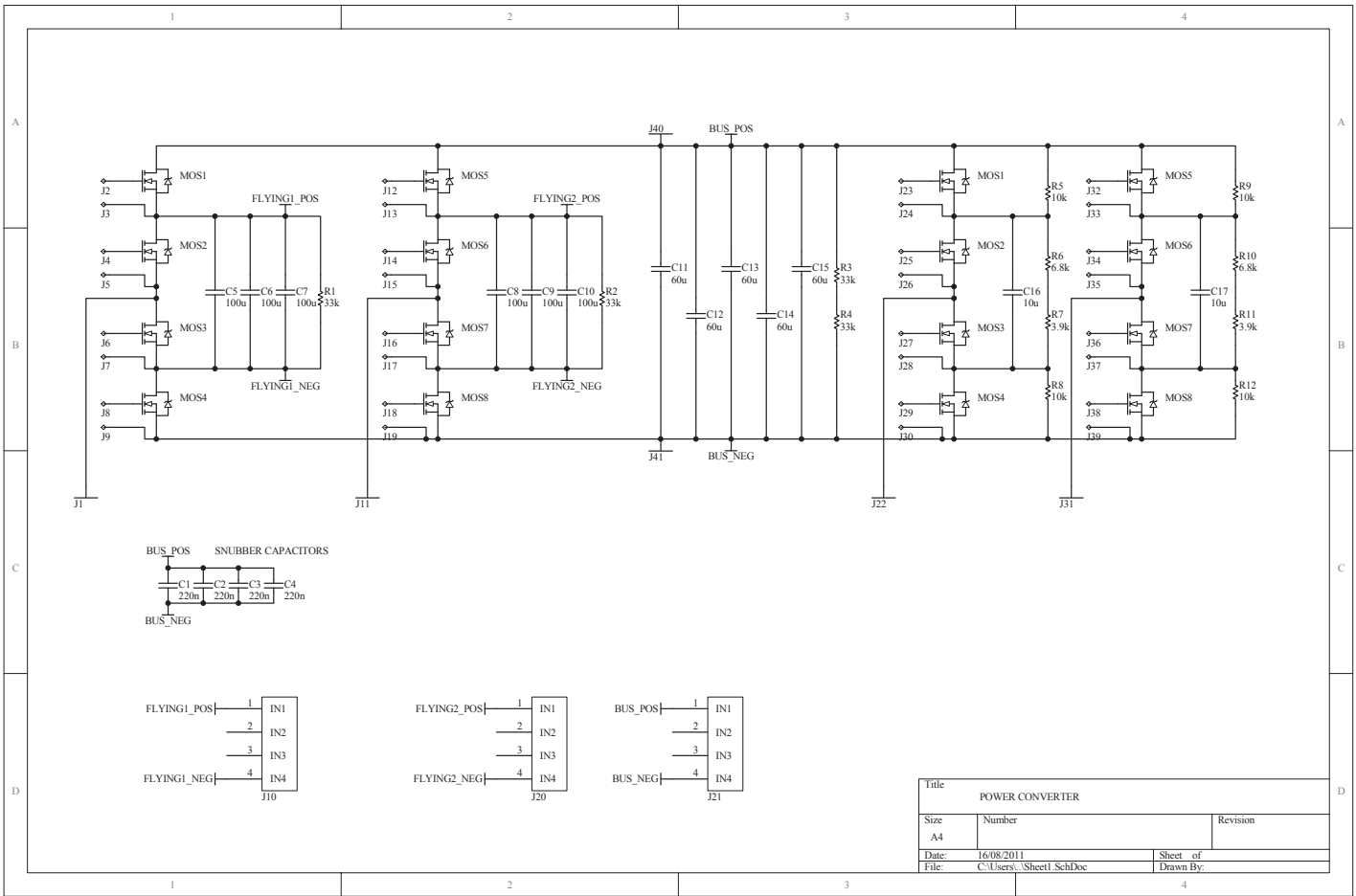
Page *LCD AND EEPROM* shows the connections for the liquid crystal display and memory. Page *ADC INPUTS AND OPTIC FIBRE OUTPUTS* shows the connectors for connecting the measurement boards and outputting the switching signals to the optic fibre transmitters.

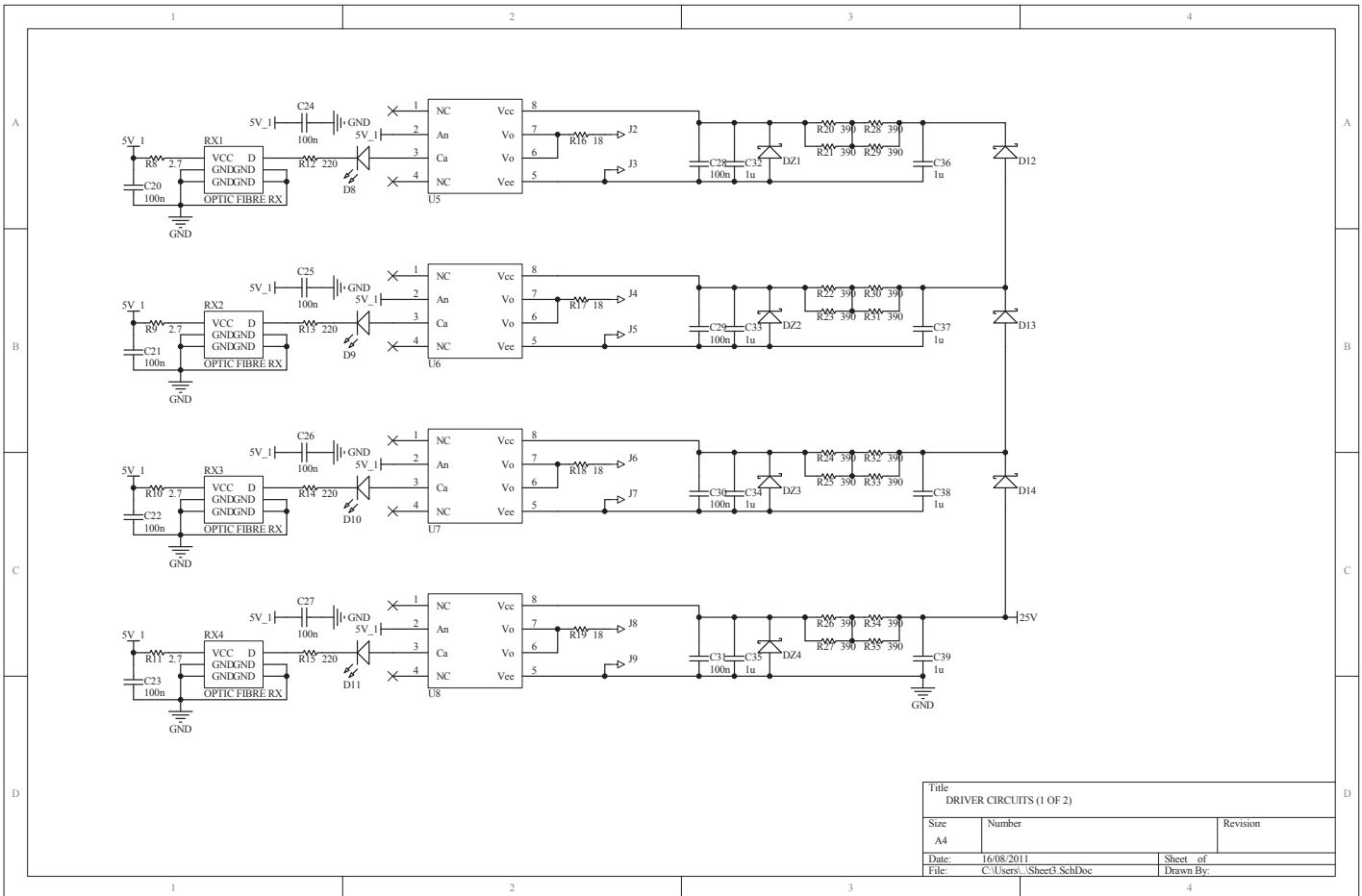
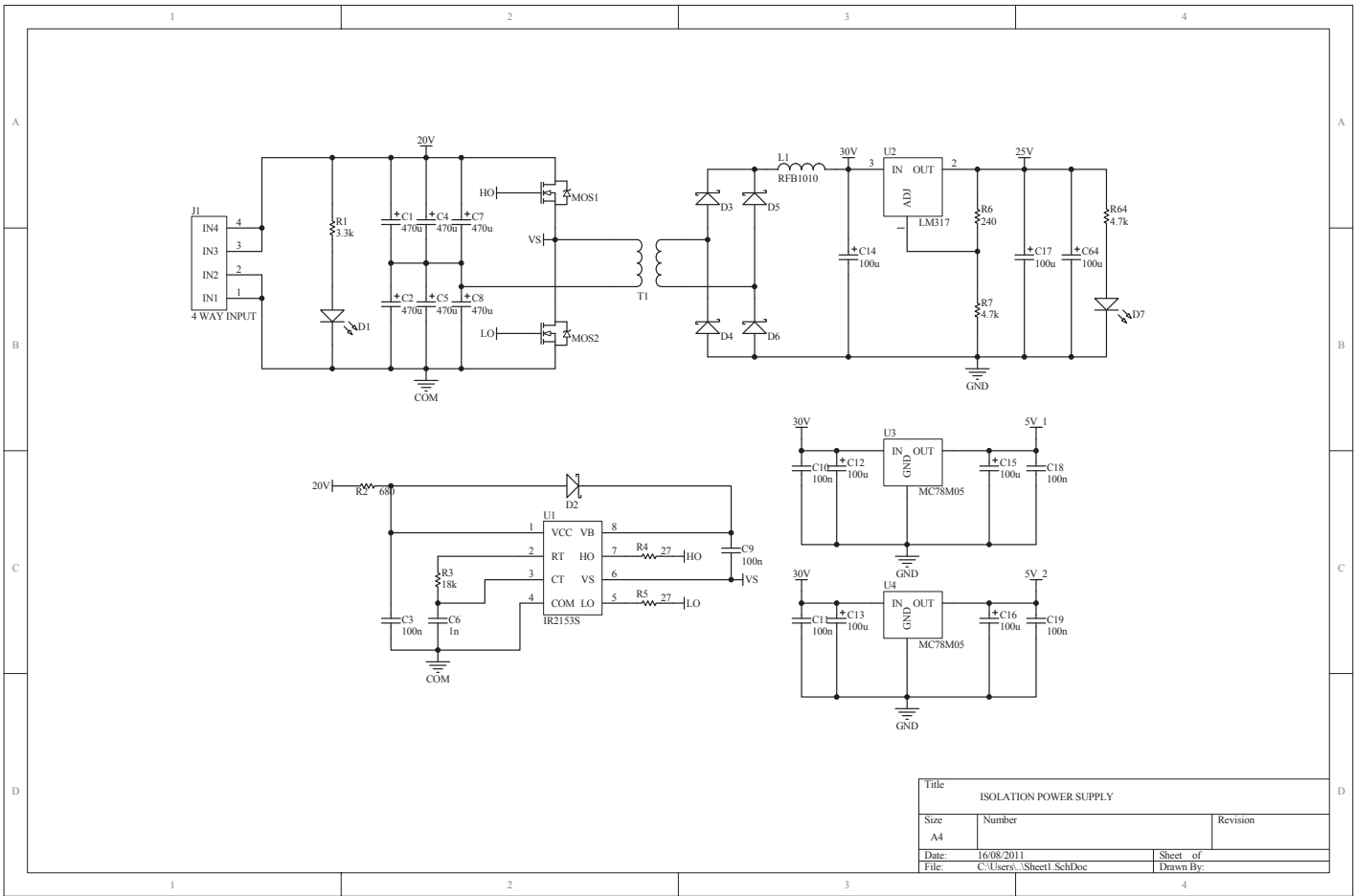
Pages *CONFIGURATION DEVICE, POWER AND GROUND; OSCILLATOR AND DIFFERENTIAL SIGNALLING*; and *FPGA BANKS FOR OPTIC FIBRE OUTPUTS, LEDs AND PUSH-BUTTONS* shows all the connections with the FPGA.

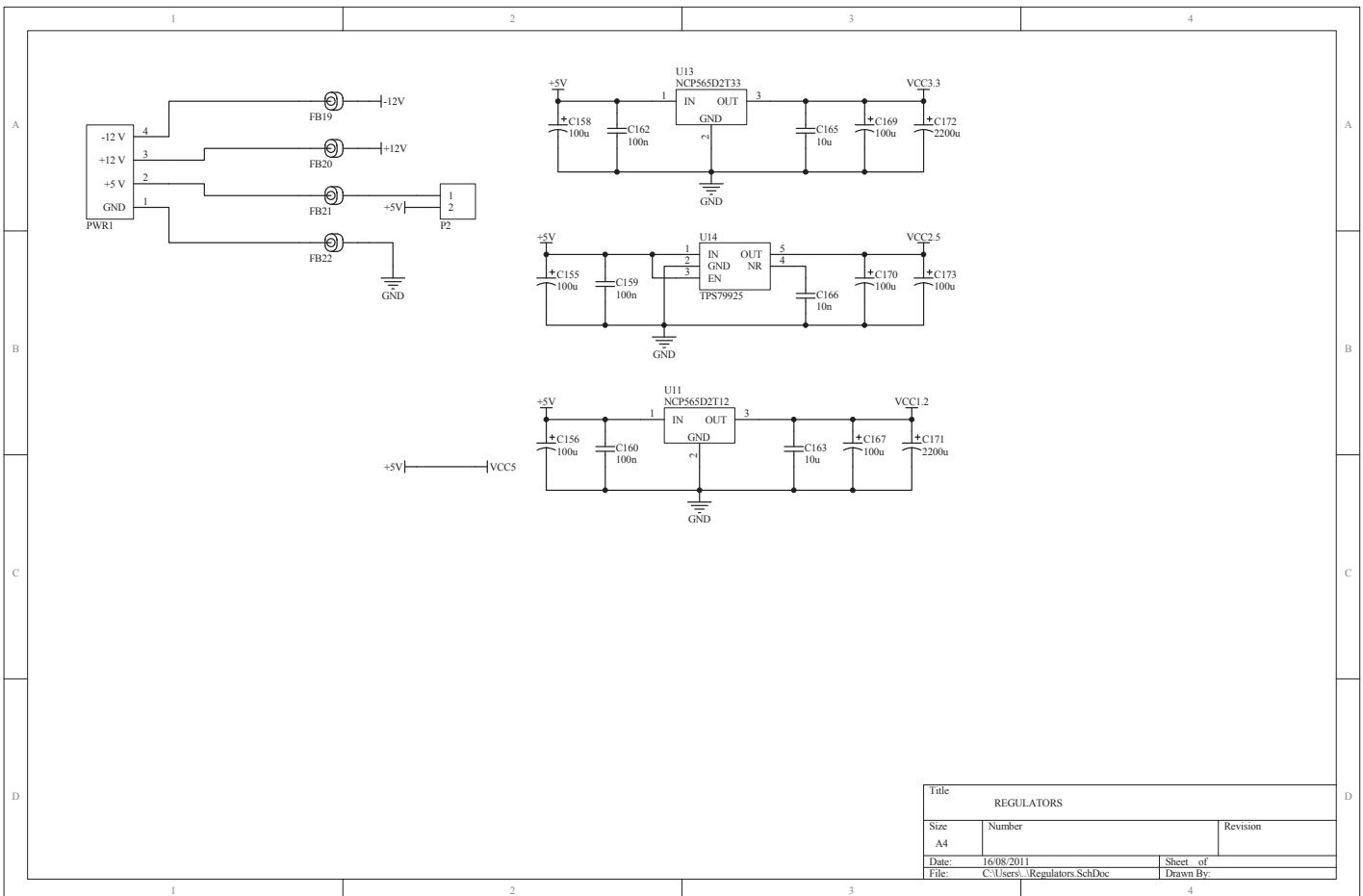
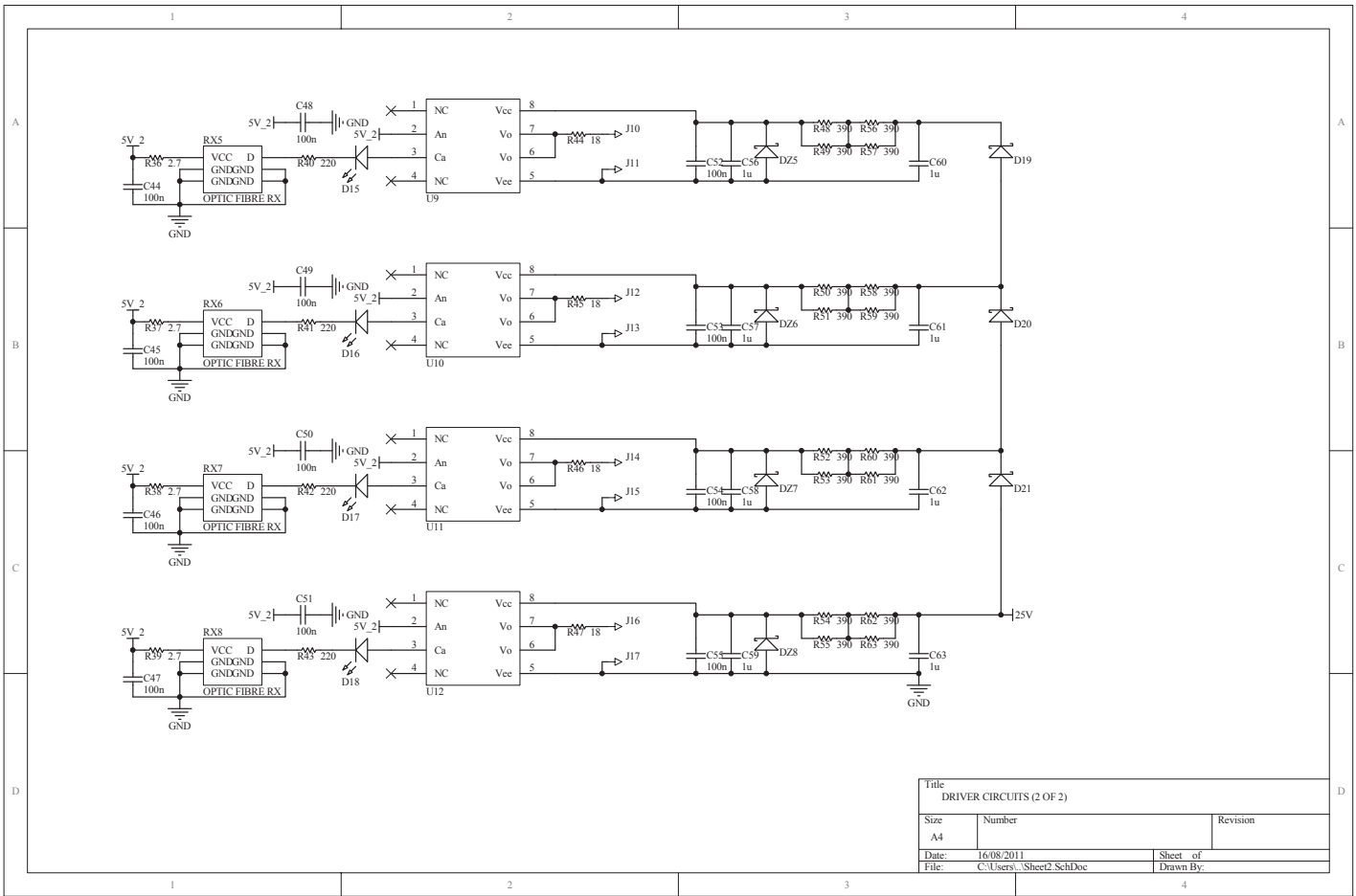
C.4 Optic Fibre Transmitters

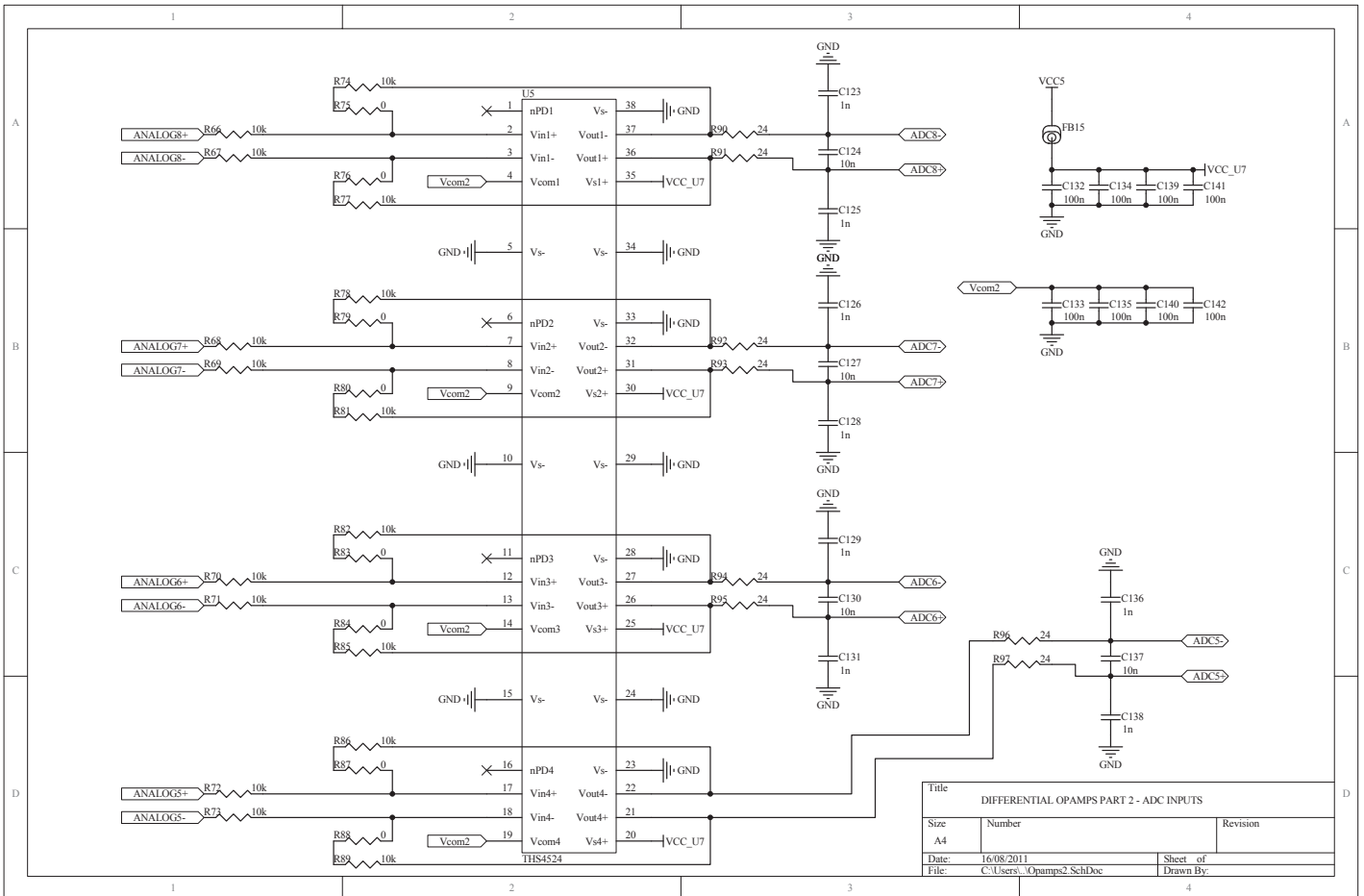
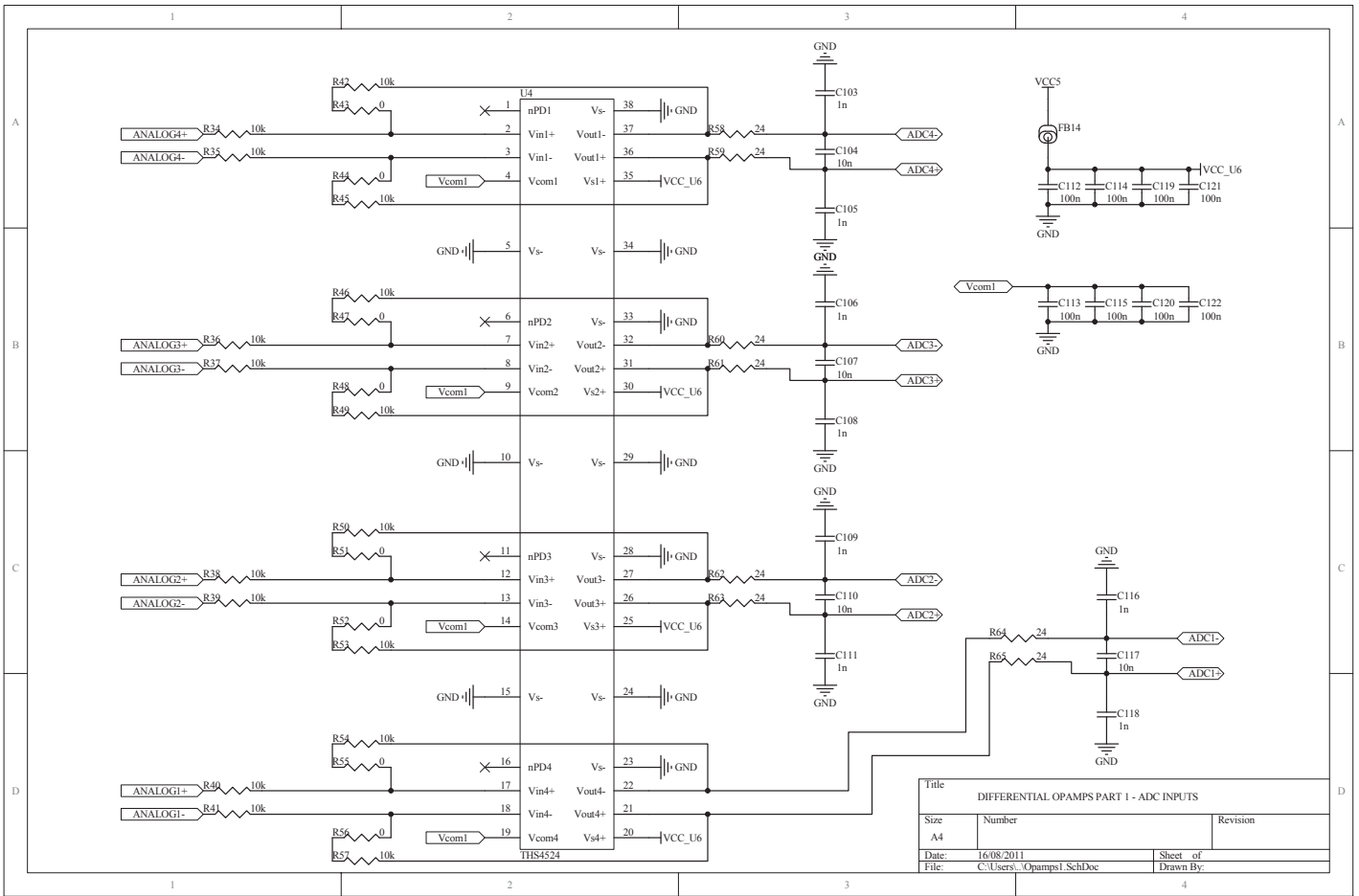
Pages *OPTIC FIBRE TRANSMITTERS - PAGE 1* and *OPTIC FIBRE TRANSMITTERS - PAGE 2* shows the 32 optic transmitters with their drivers. Each driver integrated circuit consists of two drivers and can therefore operate two transmitters. The FPGA and level shifters cannot provide enough current to power the optic transmitters. The drivers are therefore needed.

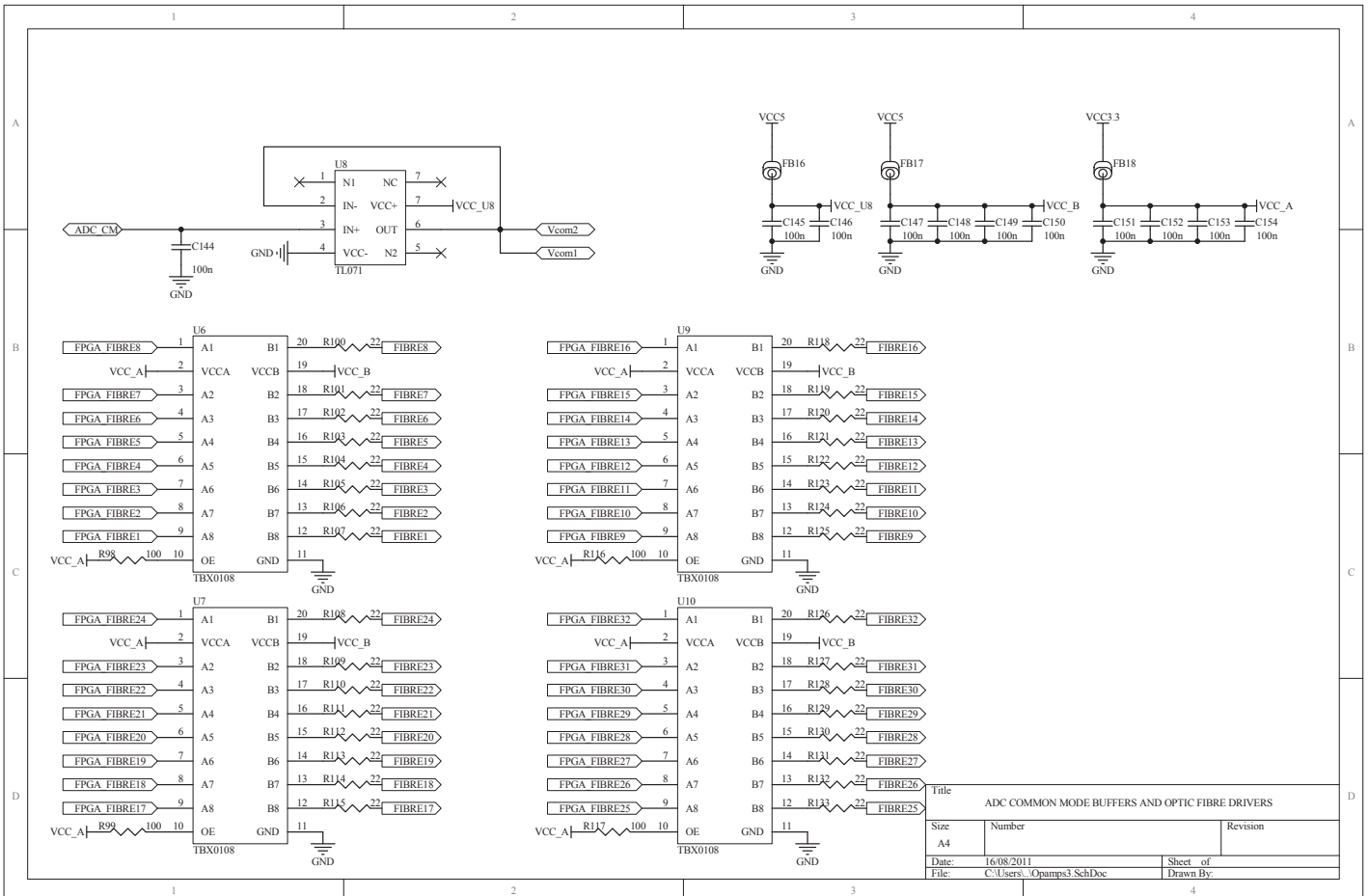
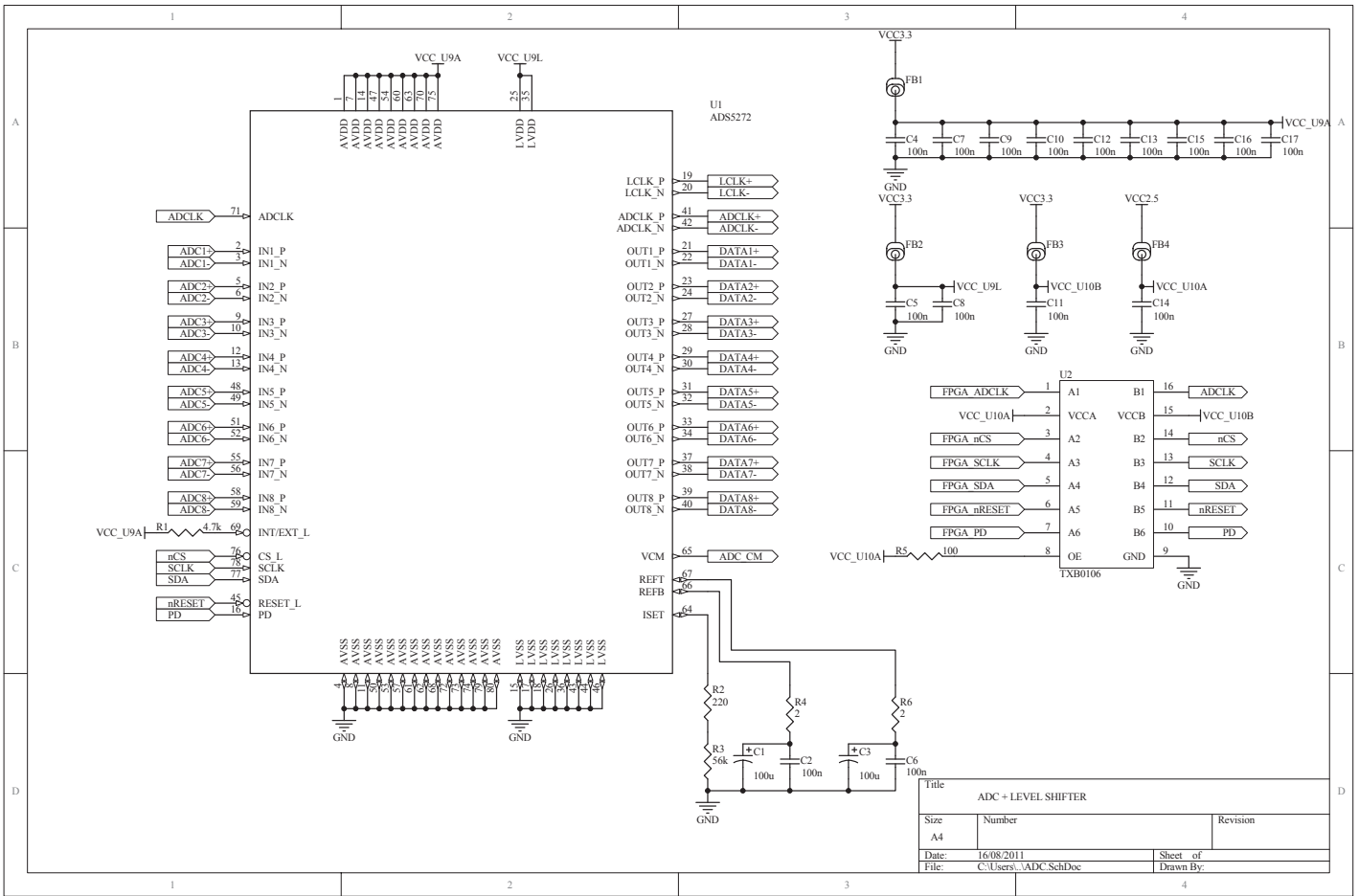


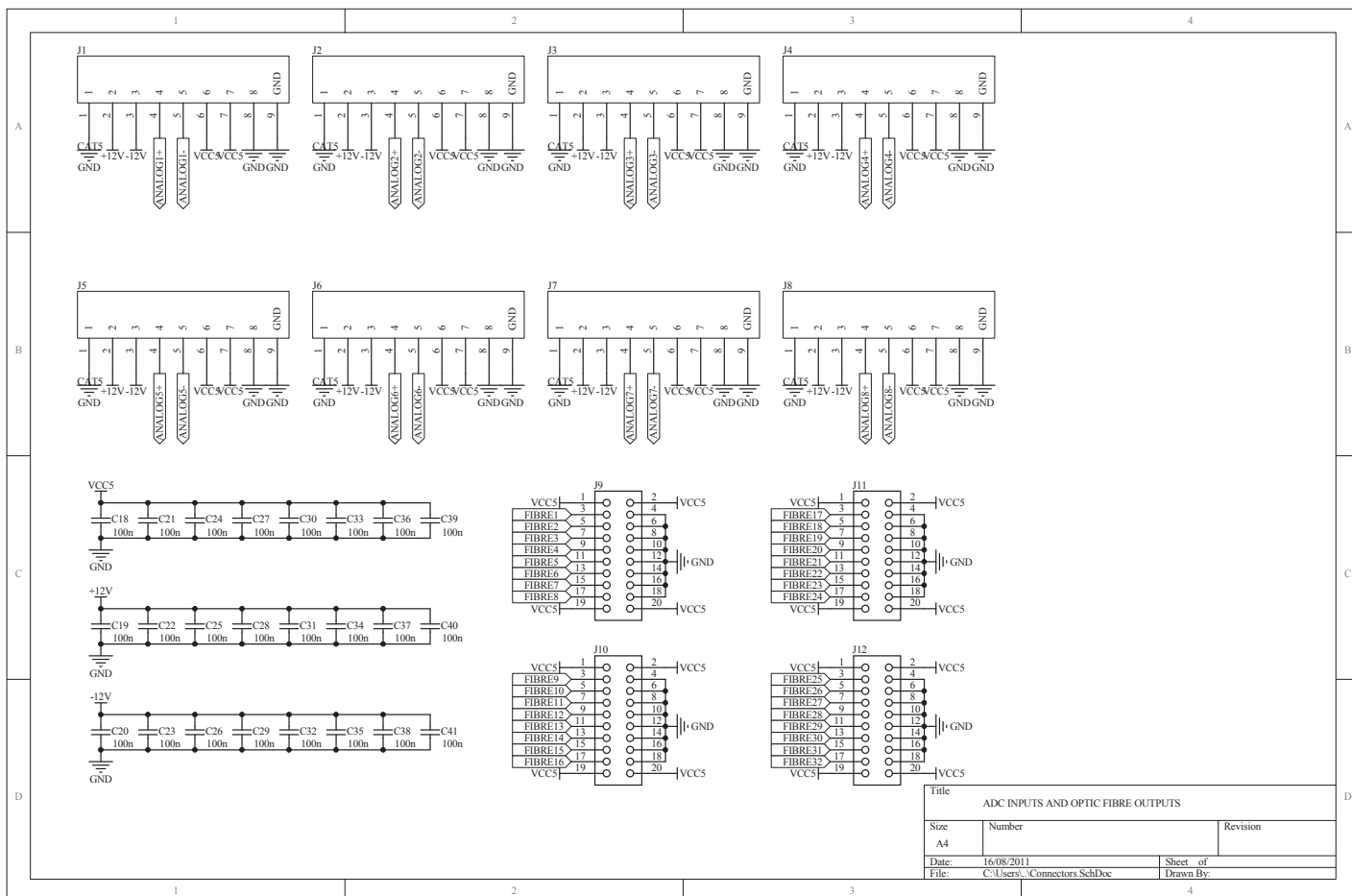
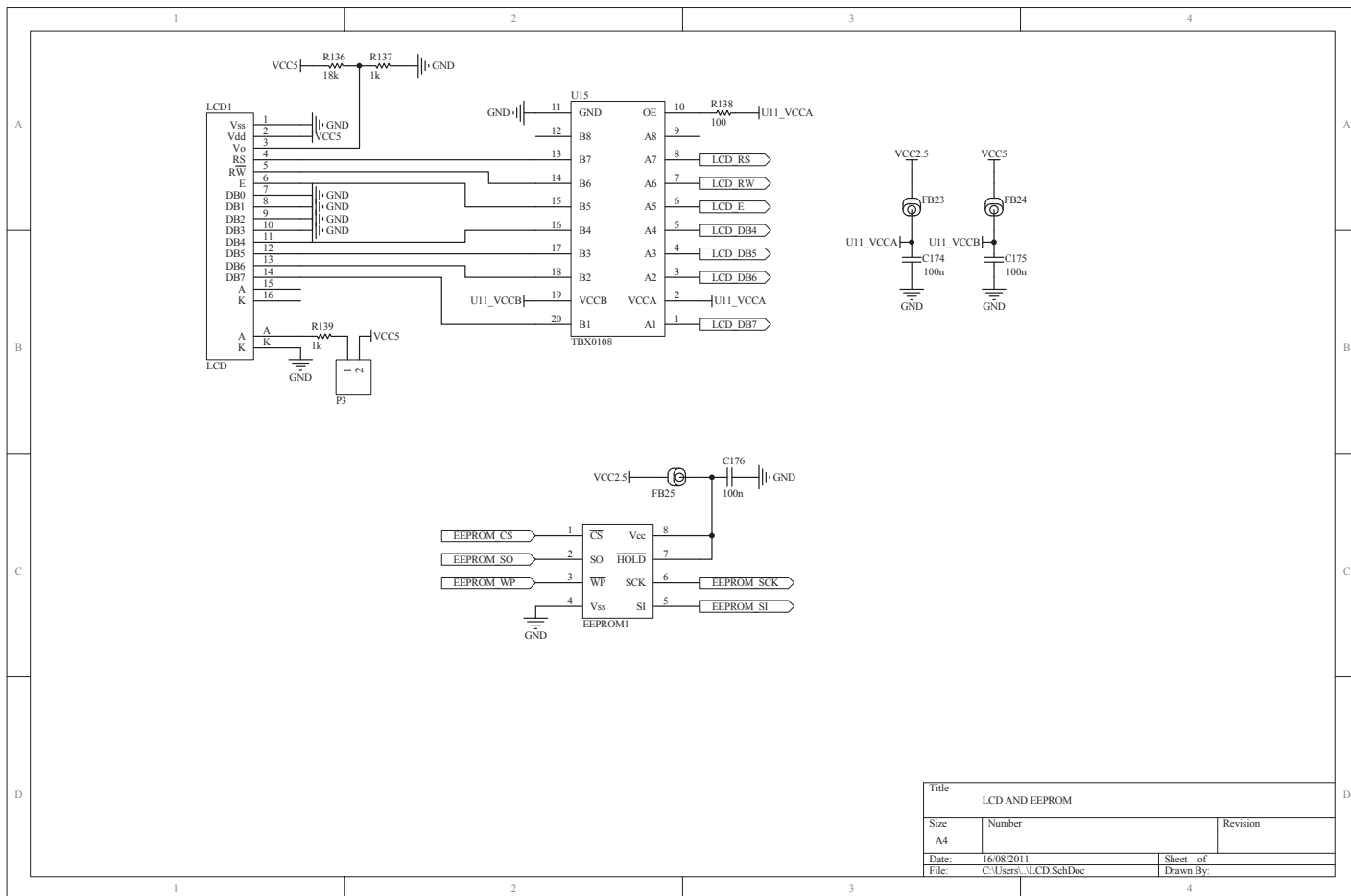


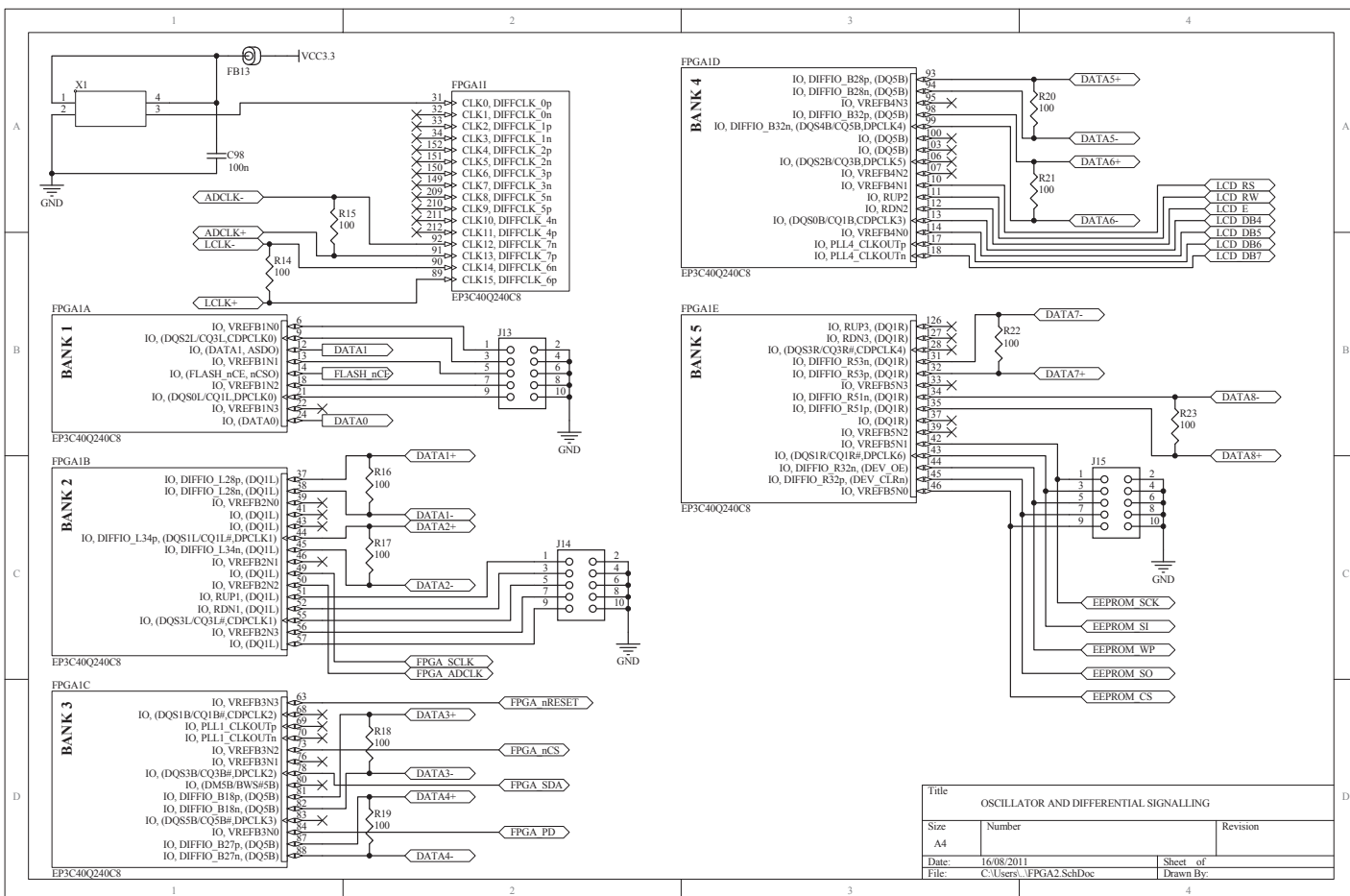
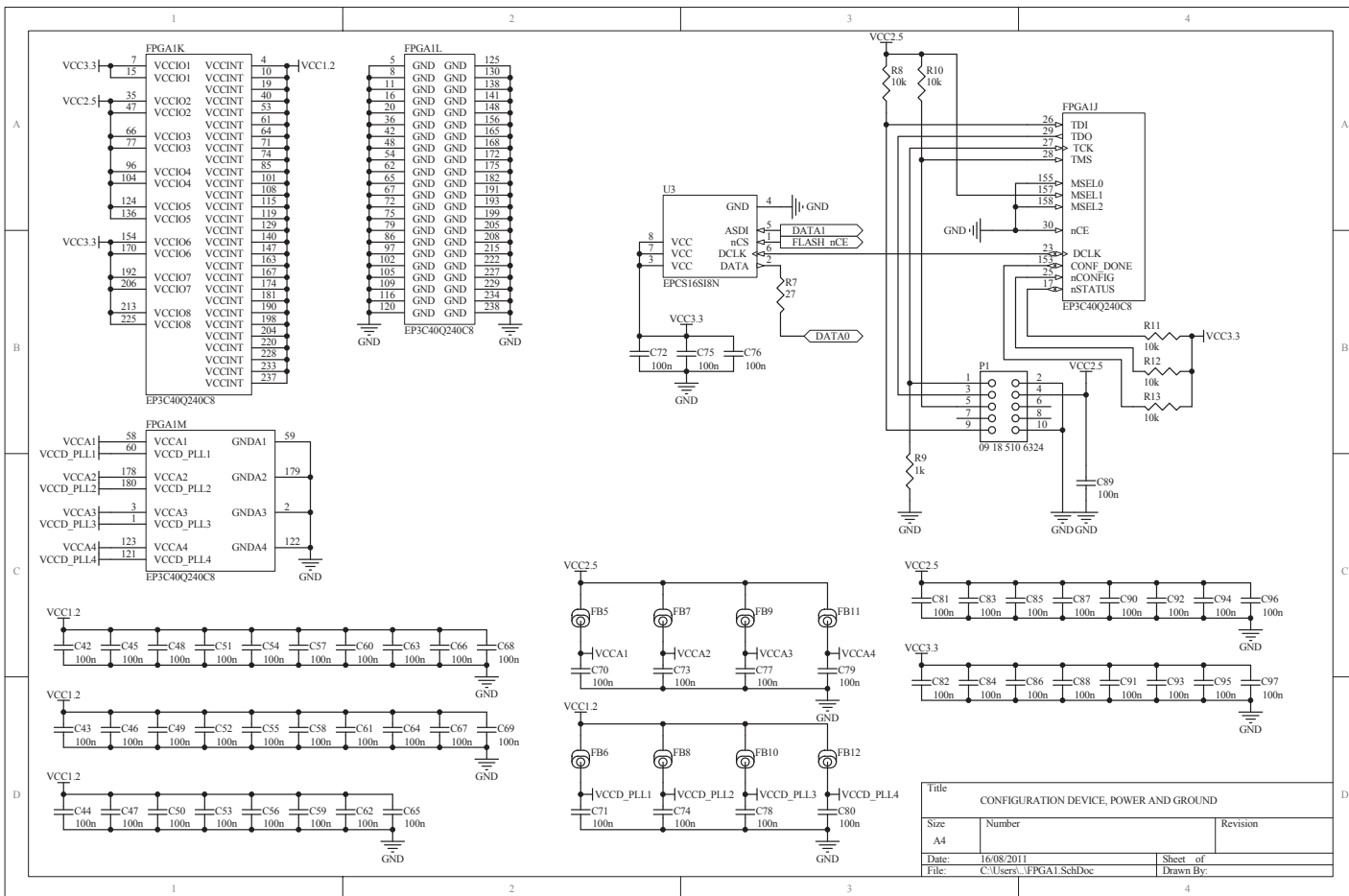


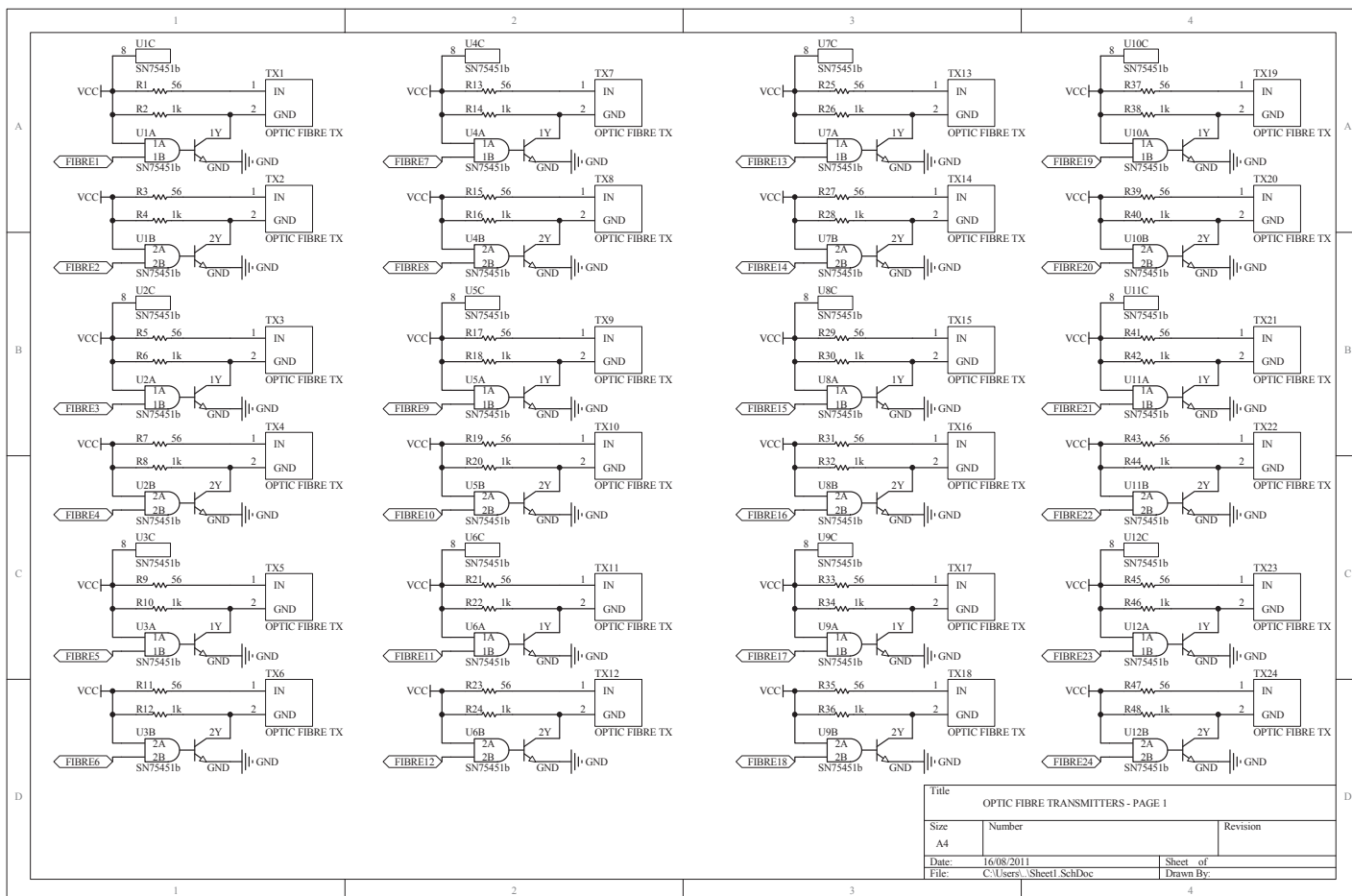
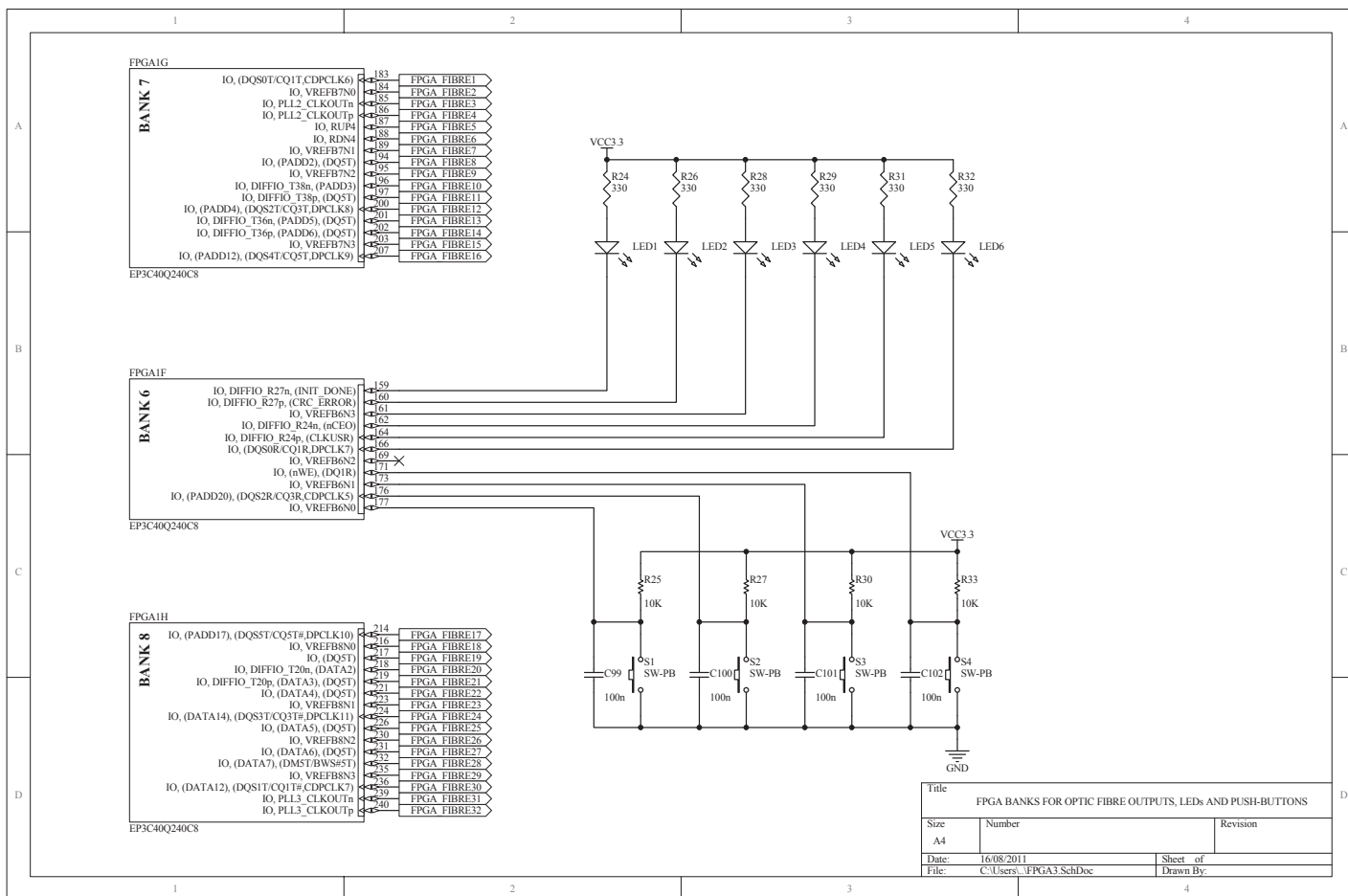


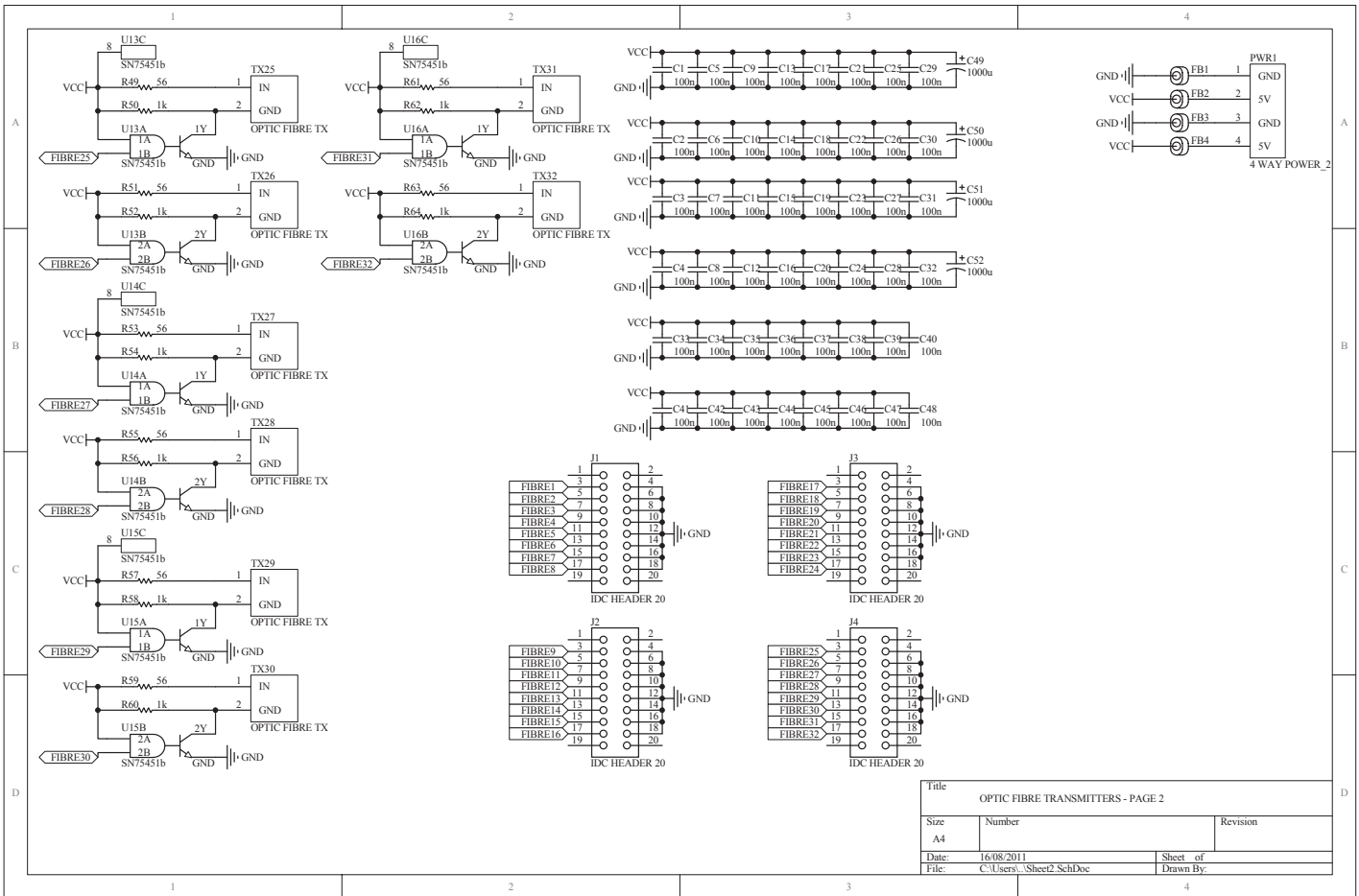












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OPTIC FIBRE TRANSMITTERS - PAGE 2		
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