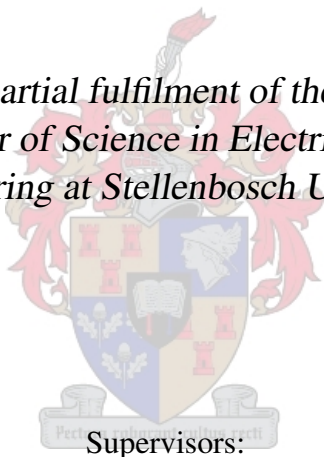


# Design and Implementation of the Main Controller of a Solid-State Transformer

by

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*Thesis presented in partial fulfilment of the requirements for the  
degree of Master of Science in Electrical & Electronic  
Engineering at Stellenbosch University*



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December 2011

# Declaration

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# Abstract

## **Design and Implementation of the Main Controller of a Solid-State Transformer**

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The Solid-State Transformer (SST) is presented as an alternative to the traditional Line-Frequency Transformer (LFT) used for voltage-level transformation in distribution grids. The LFT technology is highly matured which results in low costs and high efficiency. The SST however, introduces several advantages compared to the LFT, some of which are input unity power-factor, near perfect output-voltage regulation, frequency variation as well as harmonic filtering.

The SST consists of three power-electronic converter stages: The input stage, the isolation stage and the output stage. The input and isolation stages are implemented with a multilevel-converter topology incorporating a converter-stack for each phase. Each stack consists of  $N$  converter building blocks, called cells. In this thesis the design and implementation of the main controller is presented. The main controller, together with  $N$  cell controllers, is responsible for the control of the cells within the respective stack. Three main controllers are thus implemented within the SST.

Each cell consists of an Active Rectifier (AR) and a DC-DC Converter (DC-DC). The SST control design thus starts with the AR control which is subsequently expanded to Cascaded Active-Rectifier (CAR) control. Design is completed with the addition of the DC-DC control. Time domain simulations of the AR- and CAR-control are presented and discussed. Test measurements, verifying functionality of each control design-phase, are presented and discussed.

# Uittreksel

## **Ontwerp en Implementasie van die Hoofbeheerder van 'n Drywingselektroniese Transformator**

*(“Design and Implementation of the Main Controller of a Solid-State Transformer”)*

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Die Drywingselektroniese Transformator (DET) word voorgestel as 'n alternatief vir die Lyn Frekwensie Transformator (LFT) wat gebruik word vir spannings-vlak transformasie op distribusie vlak. The LFT tegnologie is ver gevorderd wat ly tot hoë effektiwiteit en lae kostes. The DET bied wel voordele soos intree eenheids arbeid faktor, na aan perfekte uittree-spannings regulasie, frekwensie variasie sovel as harmoniese filrteering.

Die DET bestaan uit drie drywingselektroniese omsetter stadiums: Die intree-stadium, die isolasie-stadium en die uittree-stadium. The intree- en isolasie-stadiums word geïmplimenteer met 'n multivlak-omsetter topologie wat bestaan uit 'n omsetter-stapel vir elke fase. Elke stapel bestaan uit  $N$  omsetter boustene wat selle genoem word. In hierdie tesis word the ontwerp en implementasie van die hoofbeheerder voorgestel. Die hoofbeheerder, tesame met  $N$  selbeheerders, is verantwoordelik vir die beheer van elke sel in die spesifieke stapel. In die DET word daar dus drie hoofbeheerders gebruik.

Elke sel bestaan uit 'n Aktiewe Gelykrichter (AG) en 'n GS-GS omsetter (GS-GS). Die DET beheerontwerp begin dus met die (AG) beheer wat daarna uitgebrei word na Kaskade Aktiewe Gelykrichter (KAG) beheer. Die beheer ontwerp word voltooi deur die byvoeging van die GS-GS beheer. Tyd-gebied simulاسies van die AG- en KAG-beheer word voorgelê en bespreek. Toetsmetings wat die funksionaliteit van elke beheer ontwepfsfase verifeer, word voorgelê.



# Acknowledgements

I would like to express my sincere gratitude to:

- Prof. H.du.T Mouton for his guidance, in depth knowledge and comic relief.
- Dr. Wim van der Merwe for sharing his hands-on experience and for his help and input within the SST team.
- Francois Breet for his exceptional cell-controller design and vast input within the SST team.
- Marko Wolf for his excellent cell design and input within the SST team.
- SANERI for their financial support.
- Jolan van Papendorp and Frans Welgemoed for their outside perspective and insight.
- Niel and Jaco Serdyn for always being ready to lend a helping hand.
- My parents Linus and Genéne for their ongoing support, love and encouragement.
- and last but not least, my girlfriend Sunelle for her continuous love, patience and support.

**God, in him we trust.**

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# Chapter 1

## Introduction

### 1.1 Introduction to the Line-Frequency Transformer

The LFT plays a major role in power transmission systems. Alternating Current (AC) power systems were made more attractive than Direct Current (DC) power systems by the development of the commercially practical transformer by William Stanley in 1885. When load levels and transmission distance increased in the late 1800's, the DC system failed economically. This was due to the high  $I^2R$  losses and  $I \cdot Z$  voltage drops. These problems were overcome by the AC system, together with its transformer. Defined power levels are obtained with low current levels, by means of high voltage levels, as shown in:

$$P = I \times V \tag{1.1.1}$$

LFTs used in power systems, transform AC current and voltage to optimal levels for the generation, transmission and distribution of power. Modern LFTs have ratings of up to 1300 MVA and beyond [1].

Figure 1.1 depicts a practical model of a single-phase two-winding transformer. This model differs from the ideal transformer model in that it addresses winding resistance, core permeability, flux leakage and power losses in the core.  $R_1$  accounts for the series resistance and  $jX_1$  accounts for the flux leakage of winding 1.  $R_2$  and  $jX_2$  similarly account for winding 2. Since the transformer core permeability,  $\mu_c$  is finite,  $I_e$  is defined as the exciting current. This current comprises of a core loss current,  $I_c$ , and a magnetizing current,  $I_m$ . The shunt resistor with a conductance,  $G_c$ , thus accounts for the power loss through hysteresis and eddy currents within the core. The shunt inductor with a susceptance,  $B_m$ , accounts for the power required to magnetise the core.

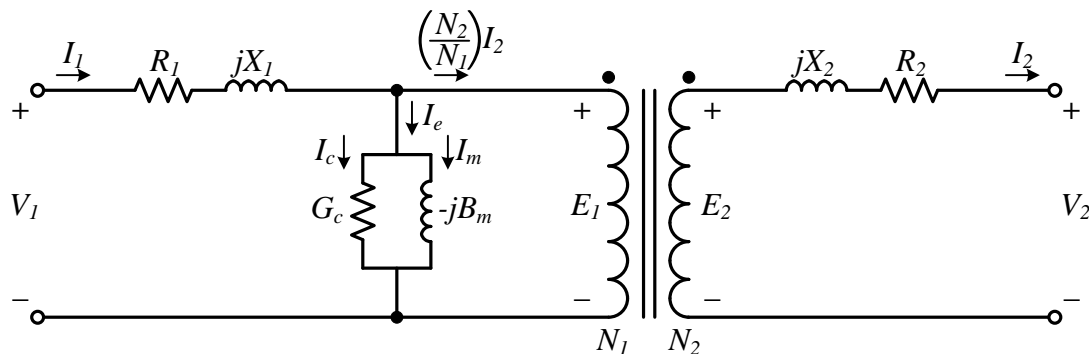
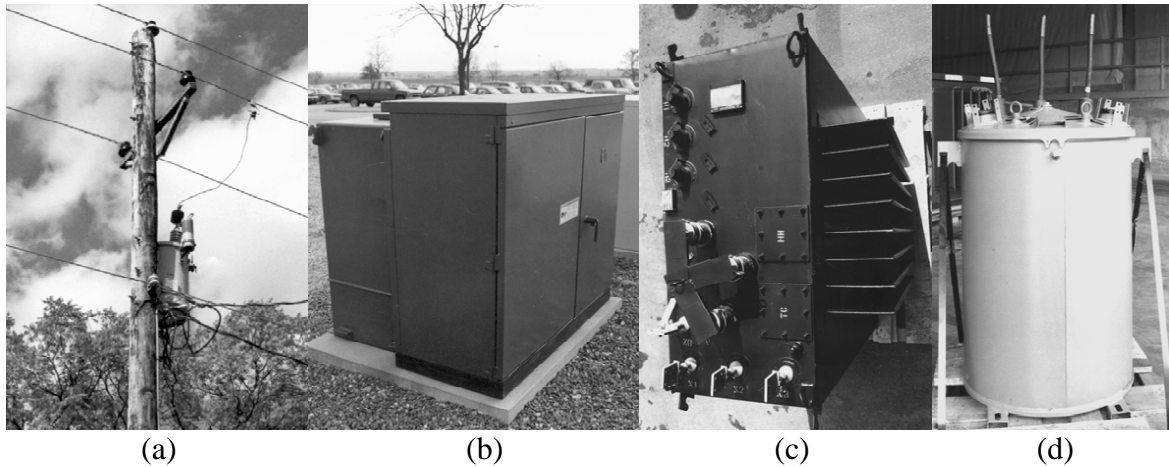


Figure 1.1: Practical Transformer Model [1]



The LFT-type of interest in this study, is the distribution transformer. The purpose of this transformer-type is to transform the primary voltage of the distribution system to the utilisation voltage level. Distribution transformers are manufactured for a range of applications. In figure 1.2 some of these application-specific distribution transformers are depicted[2].



**Figure 1.2:** Distribution Transformers: (a) Pole-Type; (b) Pad-Mounted; (c) Vault-Type; (d) Submersible

LFT technology is a mature field with very high efficiency. This maturity is also accountable for the relatively low price of LFTs. There are however several drawbacks to LFTs as listed below [1][3][4][5][6]:

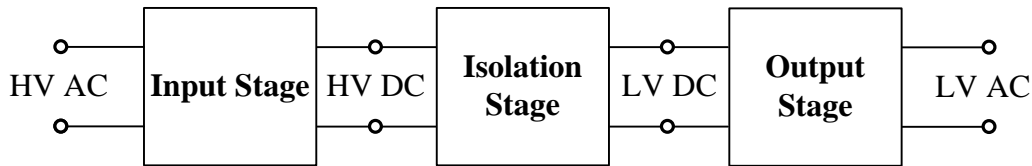
- **Non-Perfect Voltage Regulation:** The LFT output voltage is load dependent. This voltage regulation is furthermore inversely proportional to the LFT power rating. Since distribution LFT's are commonly not very large, their voltage regulation is mediocre.
- **Current Distortion:** The output current is a representation of the input, which leads to harmonic propagation between the primary and secondary. However, output spectral distortion still occurs, even with a perfectly sinusoidal input. This is due to the non-linearity of the B-H curve, representing the permeability of the transformer core.
- **Protection:** There is no output protection against power-system disruptions or overloads. Neither is there system protection against secondary faults. This is caused by the the lack of energy storage and active control within the LFT.

These drawbacks impact severely on power quality. Drawbacks of a different nature include the environmental issue regarding large quantities of mineral oil as dielectric and the sheer size and weight of an LFT. All the mentioned drawbacks, together with the recent advancements in power semiconductors, have rekindled interest in the SST as replacement for the LFT.

## 1.2 Introduction to the Solid-State Transformer

The SST concept as alternative to the LFT was mentioned as early as the 1980's, when researchers proposed a power-electronic step-down transformer for naval purposes [7]. The general SST concept is based on AC-AC transformation with an intermediate High Frequency (HF) AC stage, to reduce the size of the isolation transformer. As depicted in Figure 1.3, the SST can





**Figure 1.3:** Three Stage SST Concept

be broken down into three stages, each consisting of a power-electronic converter configuration [3].

The input stage consists of a unity power-factor rectifier, converting the single- or three-phase HV AC, to HV DC. The operation of the isolation stage can be split into 3 steps. Firstly the HV DC is converted to HF AC. Secondly the HF AC is transformed across a HF isolation-transformer. Finally the HF AC is re-rectified to bipolar LV DC. The output stage converts the bipolar LV DC to single- or three-phase LV AC. All three stages are actively controlled, which leads to key SST advantages as listed below [4]:

- **Input unity power-factor:** The input stage controls the input current, drawn from the HV supply, making it sinusoidal. The SST can be a resistive, capacitive or inductive load by configuring the input current to be in-phase, leading or lagging, compared to the supply voltage. This achieves a certain degree of reactive power compensation.
- **Near perfect output voltage regulation:** The output stage controls the single- or three-phase output voltage instantaneously.
- **Frequency variation:** The input and output stages can be configured independently to operate at different frequencies. The consumer can, for example, be supplied with a line frequency output, transformed from a different frequency supply. A different frequency output can also be obtained, transformed from a line frequency supply.
- **Output short circuit protection:** The output stage limits the output current during a fault condition. The input current is thus not affected.

Energy storage can be added in the form of bus capacitors on the HV and LV DC buses. This SST feature adds more key advantages as listed below [4][8]:

- **Input voltage dip and swell compensation:** The output stage creates the output voltage from the LV DC energy-storage capacitor voltage. The DC voltage is controlled, at a predefined average value, by the isolation stage. This means that the output voltage is immune to input voltage dips and swells, within the designed range.
- **Harmonic filtering:** Harmonic propagation is prevented between the input and output, in either direction. This filtering is jointly performed by the energy-storage capacitors and active control.

The isolation stage splits the SST into an HV side and an LV side. The SST concept can thus also be depicted as shown in Figure 1.4. The problematic aspects of this concept fall in two categories: The high voltage-levels of the LF-AC to HF-AC converter, and the isolation and parasitic issues of the HF transformer [5]. A multilevel converter is thus proposed for the HV side to clamp the voltage across each solid-state switch. This reduces the required switch blocking-voltage.

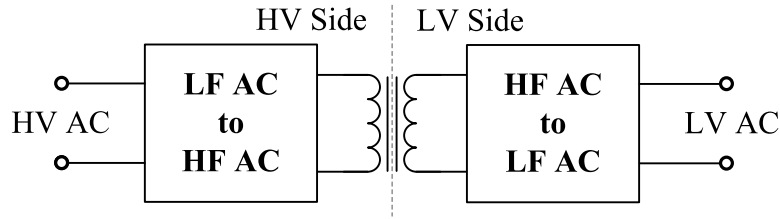


Figure 1.4: Two side SST Concept

The three basic multilevel-converter topologies are the diode-clamped, capacitor-clamped and the cascaded converter. A three-level diode-clamped converter is shown in Figure 1.5(a). The voltage,  $V_{an}$ , can be equal to  $\frac{V_{dc}}{2}$ , 0 or  $-\frac{V_{dc}}{2}$ , hence three-levels. The key components are the diodes  $D_1$  and  $D_1'$ . These diodes clamp the voltage across each switch to only half the DC bus voltage. For example, the voltage across  $a$  and  $o$  is  $V_{dc}$ , when  $S_1$  and  $S_2$  turn on. During this scenario,  $D_1'$  clamps the voltage across  $S_1'$  and  $S_2'$ , so that  $S_1'$  blocks the voltage across  $C_1$  and  $S_2'$  blocks the voltage across  $C_2$ .

Figure 1.5(b) depicts a three-level capacitor-clamped converter, also known as a flying-capacitor converter. This converter works in much the same way as the diode-clamped converter, in that the voltage,  $V_{an}$ , can also be one of the three values,  $\frac{V_{dc}}{2}$ , 0 or  $-\frac{V_{dc}}{2}$ . The voltage across the switches is however clamped by clamping capacitors. There is only one switching-configuration requirement, that the switch pairs,  $S_1$  and  $S_1'$ , etc. should be switched as alternate pairs.

The diode- and capacitor-clamped converters are further discussed in [6]. The cascaded converter topology is discussed in Section 1.3.1. The three converters are compared with each other in terms of cost and complexity in [5].

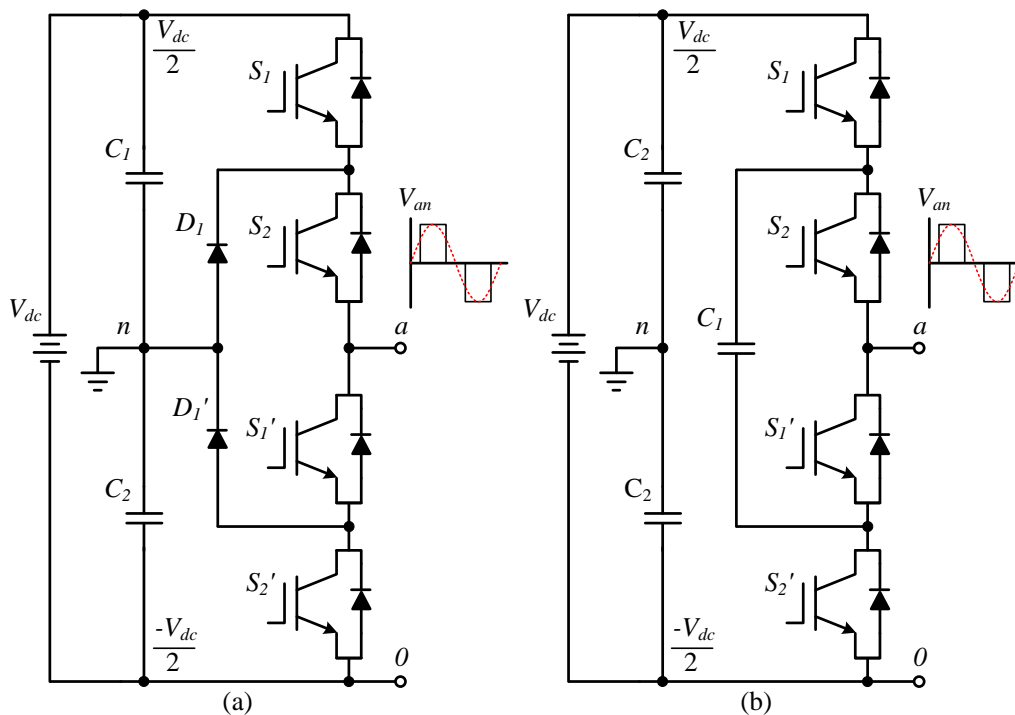
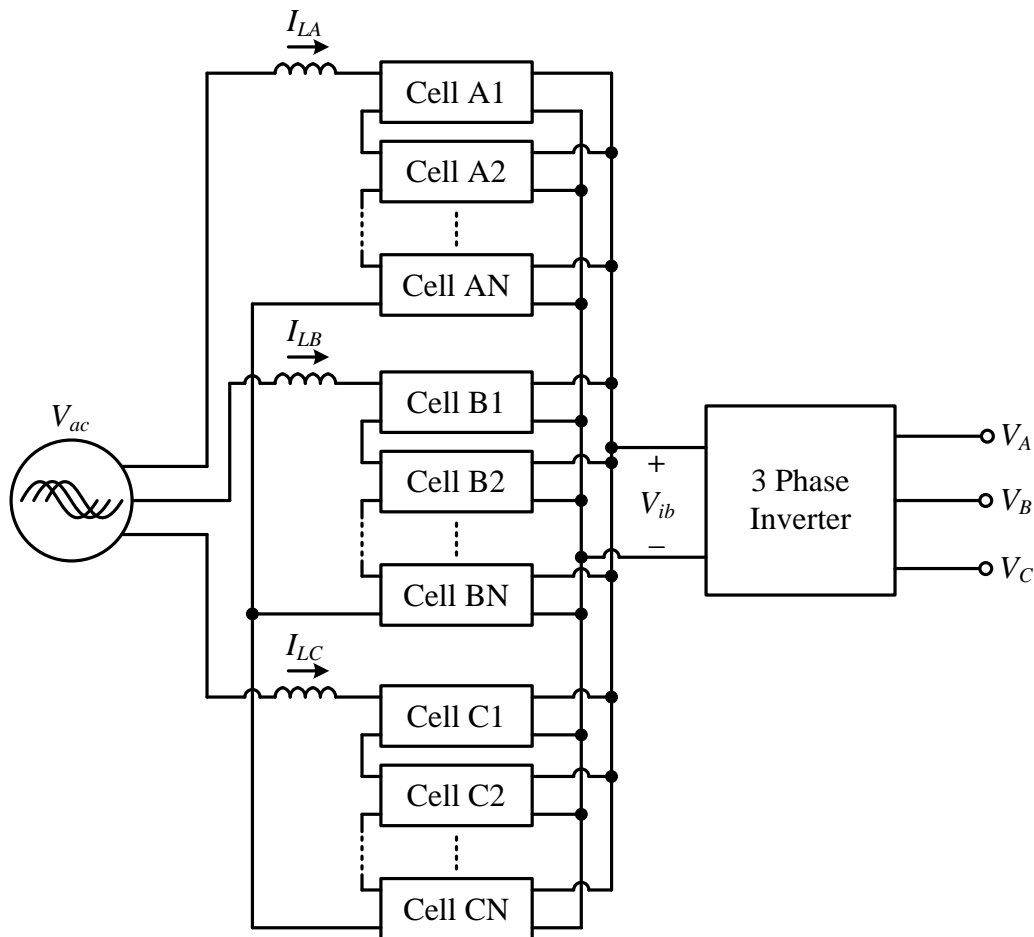


Figure 1.5: (a) 3-level Diode-Clamped Configuration; (b) 3-level Capacitor-Clamped Configuration

## 1.3 Topicality of Study

### 1.3.1 SST Topology of Interest

This thesis is part of a project aimed at designing, developing and testing a three-phase SST at distribution level. Due to the findings in [5], the series-stacked converter topology is used to account for the high input voltage level. This topology is also known as the cascaded converter topology. Figure 1.6 depicts the topology with three converter stacks, one per phase-arm. Each converter stack consists of  $N$  converter building-blocks, called cells. These cells convert the line-frequency HV AC,  $V_{ac}$ , to LV DC. The SST input is connected in star with each stack input connected in series. This splits the line to neutral input-voltage among  $N$  cells. The stack output is connected in parallel to the LV DC inverter bus,  $V_{ib}$ , which facilitates the high current output of the stack. The Three-Phase Inverter (TPI) converts the LV DC to three-phase line-frequency LV AC, for residential use.



**Figure 1.6:** Three-Phase SST Topology

A closer look will reveal that each cell consists of two back-to-back full-bridge converters as shown in Figure 1.7. The front-end converter is an AR, which converts the line-frequency AC to DC, the cell bus-voltage,  $V_{cb}$ . The AR is responsible for input unity power-factor, through input-current control, and cell bus-voltage control. The back-end converter is a DC-DC converter and consists of a full-bridge converter, an isolation transformer, a passive rectifier and an output filter. The DC-DC converter is responsible for driving power across the isolation

transformer, through control of the transformer input current, while implementing inverter bus-voltage control.

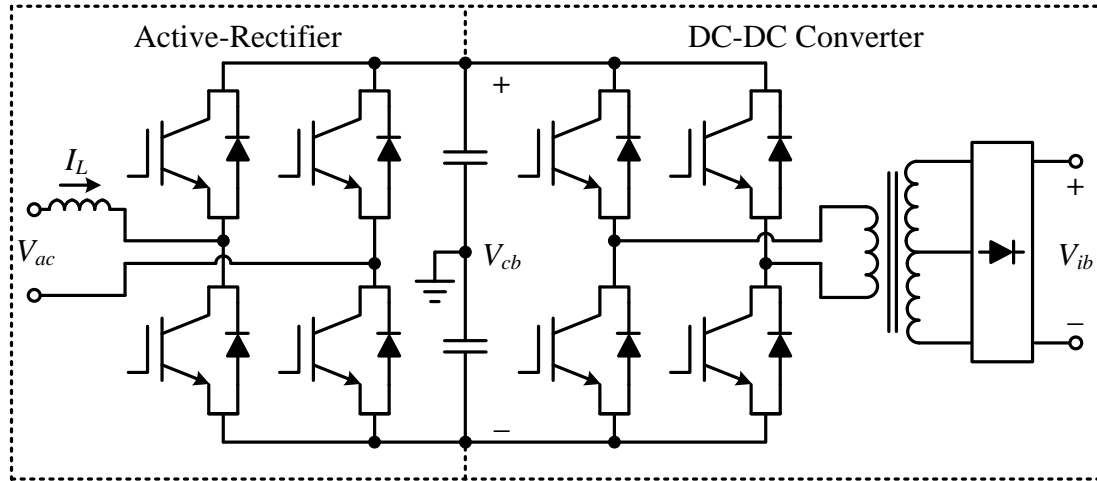


Figure 1.7: Cell Configuration

The TPI consists of three half-bridge converters and an output filter as shown in Figure 1.8. This topology provides a neutral point to the load which is equivalent to the output configuration of a distribution LFT.

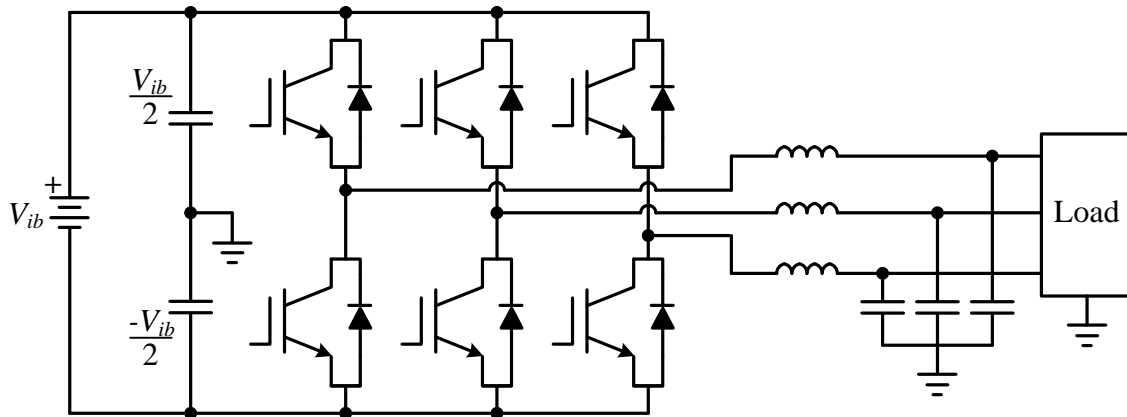


Figure 1.8: Three-Phase Inverter Configuration

### 1.3.2 Topology Advantages

The proposed SST topology has several advantages above and beyond the general SST advantages mentioned in Section 1.2. These advantages are briefly discussed below:

- **Modularity:** The topology of interest is highly modular. The input and isolation stages consist of a number of identical cells. This has numerous advantages for example, a faulty cell can automatically be shut down and isolated from the, still functioning, system. This cell can be swapped with a new or refurbished cell. The SST can be tailored for a specific input voltage-level by simply adding or removing cells.

- **Single-Phase or Three-Phase Operation:** The SST is able to facilitate a single-phase or three-phase input since the total number of cells present in the SST all feed a single DC bus,  $V_{ib}$ . The SST is able to facilitate single-phase and three-phase output since the TPI consists of three half-bridge converters. When a fault condition occurs on a single phase, the three-phase inverter can shut that phase down without disrupting the other two phases.
- **High Input Stage Switching Frequency:** The cascaded ARs in each phase-arm, are switched in an interleaved fashion, as discussed in Section 5.2.1. This increases the switching frequency of each input stage to  $N \times f_{ar}$  with  $f_{ar}$  defined as the switching frequency of each AR respectively. The increased switching frequency leads to a reduction in the required input-stage inductor size.
- **Reduced Input-Stage Inductor Isolation:** The input-stage inductor can be split into  $N$  smaller inductors to configure them as input-inductors of each AR respectively. This increases the modularity of the input stage and reduces the isolation requirements of the inductors, due to the multilevel characteristic of the SST.
- **Smaller High Frequency Transformer:** The DC-DC converter's high switching frequency drastically reduces the size of the isolation transformer. This reduces core loss and magnetising loss. The isolation stage is incorporated in the cascaded cells. Each isolation-transformer input-voltage is thus  $N$ -times smaller than the total bus-voltage of the stack. This reduces the required isolation between the primary windings. The isolation requirement between the primary and secondary windings is however not reduced by the cascaded topology.

### 1.3.3 Control Hardware Scheme

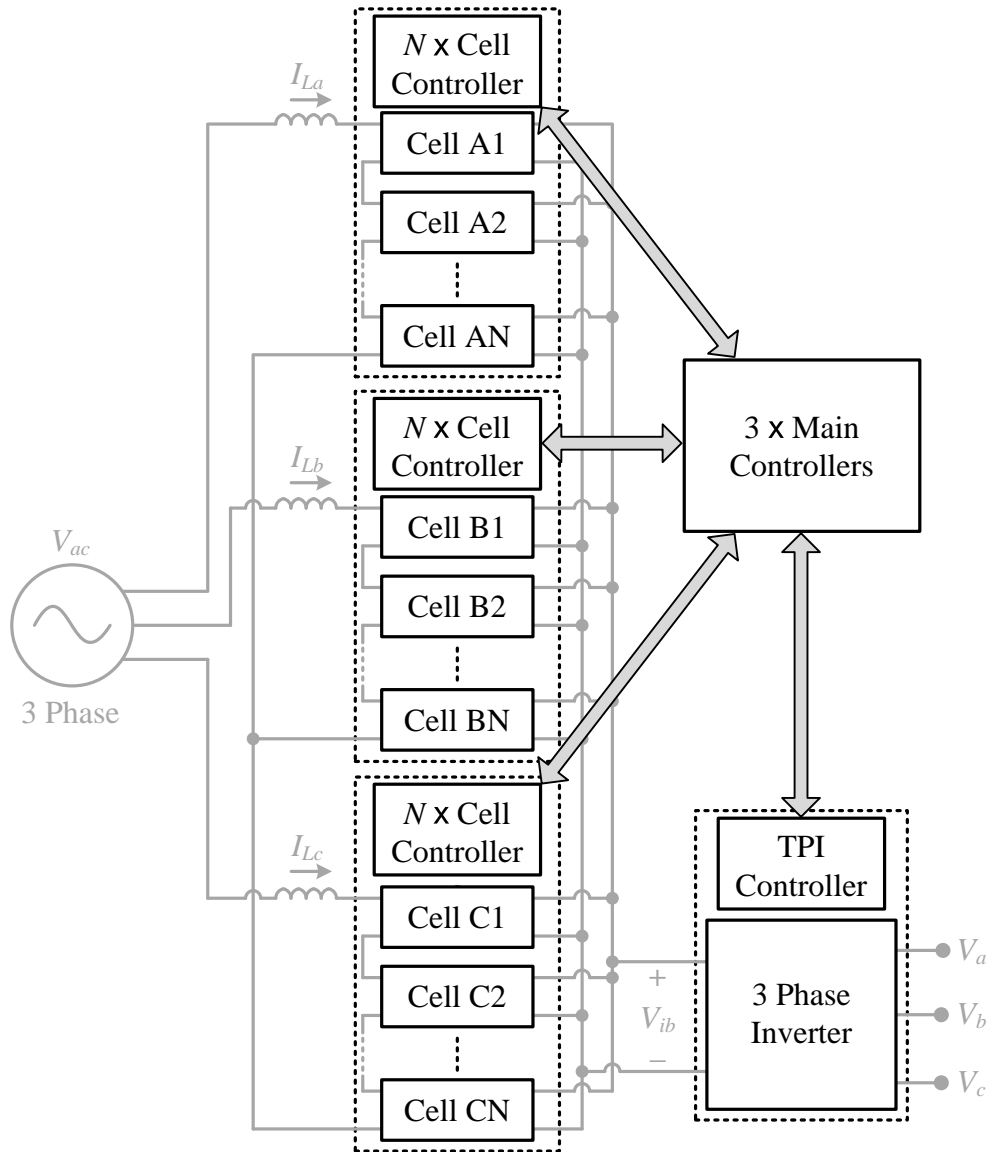
There are several system parameters which require control within the SST topology. These parameters include the three input-inductor currents of the isolation stage,  $I_{La}$ ,  $I_{Lb}$  and  $I_{Lc}$ , the bus voltage of each cell,  $V_{cb}$ , the transformer input-current of each cell,  $I_t$ , the TPI bus voltage,  $V_{ib}$ , and the TPI output voltages,  $V_a$ ,  $V_b$  and  $V_c$ . The proposed control scheme includes a Cell Controller (CC) for each cell, a Main Controller (MC) for each phase and a TPI controller for the output stage. Figure 1.9 depicts this control scheme with the arrows indicating the communication network between controllers.

The CC adds to the prominent SST topology-advantage of modularity. The functionality of the CC can be grouped into three categories as listed below. It is responsible for:

- **Measurements:** Measuring cell parameters and measurement processing.
- **Communication:** Relaying the processed measurements to, and receiving control information from the specific MC.
- **Control:** Facilitating control-loop segments and thus, together with the MC, controlling the input and isolation stages.

The MC, using the CC as cell interface, is responsible for the prominent SST advantage of facilitating input unity power-factor. The MC functionality can be grouped into six categories as listed below. It is responsible for:

- **Measurements:** Measuring phase parameters and measurement processing.



**Figure 1.9:** Control Hardware Scheme

- **Communication:** Relaying control information to, and receiving processed measurements from the respective CCs. There is also communication between MCs and between an MC and the TPI controller.
- **Control:** Facilitating the greater part of the input- and isolation-stage control.
- **Fault Handling:** Handling faults detected through MC, CC and TPI-controller measurements.
- **Data logging:** Logging system parameters in non-volatile memory.
- **External communication:** Relaying fault warnings to the utility and logged data to a download storage-device.

The TPI controller is responsible for the prominent SST advantage of perfect output regulation. The functionality of the TPI controller can also be grouped into three categories as listed below. It is responsible for:

- **Measurements:** Measuring TPI parameters and measurement processing.
- **Control:** Facilitating the output-stage control.
- **Communication:** Relaying fault indications to, and receiving control-start information from an MC.

### 1.3.4 Topology Challenges

There are a few challenges in developing an SST. There are also a few topology-specific challenges in developing the SST topology of interest, as with any new development. Some of these are listed below:

- **Voltage Balancing:** There are several active balancing techniques for cascaded converters however, natural voltage balancing mechanisms have been identified in cascaded ARs [9], and in cascaded back-to-back converters [10]. These mechanisms require certain control and switching schemes.
- **Complex Control:** All three SST stages require control. Each phase of the input stage is jointly controlled by  $N$  CCs and one MC. These controller phase-groups are also responsible for the control of each isolation-stage phase. The output stage is controlled by the TPI controller. The input-stage output serves as the isolation-stage input, and the isolation-stage output serves as the output-stage input. This requires the careful design of three control systems functioning in harmony.
- **Complex Communication:** Communication is required between controllers to facilitate the three control systems, together with fault handling. It consists of  $3N$  communication channels between CC and MC, 2 channels between MC and MC and 1 channel between TPI controller and MC. Each channel consists of one send and one receive fibre.
- **Large Number of Measurements:** The advantages of system modularity are paired with the challenge of administrating a large number of measurements. There are at least two measurements required from each cell as control inputs, namely the cell bus-voltage,  $V_{cb}$ , and the isolation transformer input current,  $I_t$ . Additional measurements are also advised for fault handling, e.g. strategically chosen temperature measurements. Each MC measures the input-inductor current and input voltage of its respective phase. The inverter bus-voltage is also measured.

## 1.4 System Parameters

The parameters needed to characterise the SST broadly are listed below:

Parameter	Symbol	Value	Units
3-Phase Input Line-Voltage	$V_{ac}$	6.6	kV rms
3-Phase Output Line-Neutral Voltage	$V_a, V_b, V_c$	230	V
SST Power Rating	$P_{SST}$	60	kW
Input Frequency	$f_{in}$	50	Hz
Output Frequency	$f_{out}$	50	Hz
Number of Cells per Phase	$N$	15	Units Max
AR Switching Frequency	$f_{ar}$	20	kHz
DC-DC Switching Frequency	$f_{dc}$	15	kHz
TPI Bus-Voltage	$V_{ib}$	800	V

**Table 1.1:** SST System Parameters

## 1.5 Study Objectives

The aim of the author is the design and implementation of the SST main controller. The objectives can be split into three categories, namely hardware, control firmware and peripheral firmware. The MC hardware block-diagram is depicted in Figure 1.10.

The hardware objectives include the design, populating and testing of PCBs, as listed below:

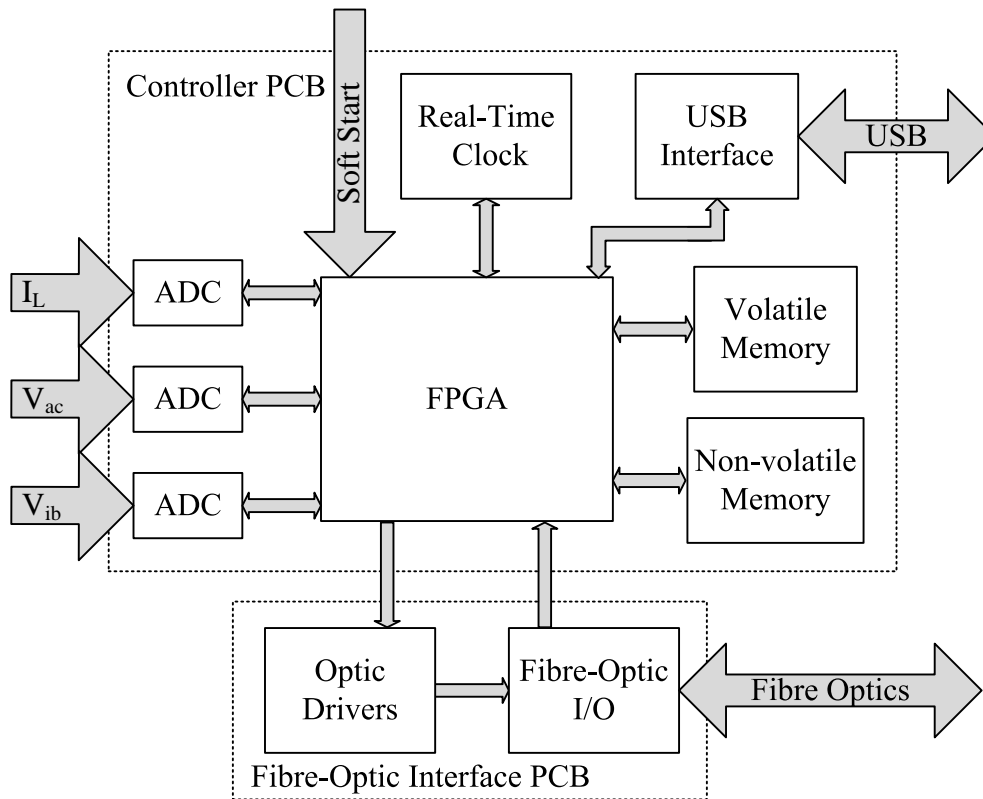
- The measurement PCBs, converting two single-ended measurements to differential signals and scaling a third differential measurement.
- The controller PCB, including a Field Programmable Gate Array (FPGA), a measurement acquisition system, an interface to the fibre-optic interface PCB and peripheral hardware. The peripheral hardware includes a memory system, a real-time clock and a USB interface.
- The fibre-optic interface PCB, facilitating fibre-optic transmitters and receivers as well as an interface to the controller PCB.

The control firmware includes the control systems of the input- and isolation-stage and the objectives are as listed below:

- **Input-Stage Control:** Responsible for input unity power-factor and the cell bus-voltage control.
  - Investigate control strategies to identify the most suited control method.
  - Simulate the proposed strategy with computer simulation software to establish theoretical functioning.
  - Implement the proposed strategy in VHDL, to be uploaded to the MC and CC FPGAs<sup>1</sup>.

<sup>1</sup>This Objective is jointly accomplished, together with [11]





**Figure 1.10:** Simplified MC Hardware Block Diagram

- Test the proposed strategy with physical test-setups<sup>2</sup>.
- **Isolation-Stage Control:** Responsible for transforming the power across the isolation barrier through control of the transformer input current, while controlling the TPI bus-voltage.
  - Investigate control strategies to identify the most suited control method<sup>2</sup>.
  - Simulate the proposed strategy with computer simulation software to establish theoretical functioning<sup>2</sup>.
  - Implement the proposed strategy in VHDL to be uploaded to the MC and CC FPGAs<sup>2</sup>.
  - Test the proposed strategy with physical test-setups<sup>2</sup>.

The SST Peripheral functionality can be classified as functionality above and beyond the three-phase HV to LV transformation. The peripheral firmware together with the peripheral hardware is responsible for this functionality. The related objectives are listed below:

- Implement an interface, in C programming-language, to utilise the memory system.
- Implement an interface, in C programming-language, to utilise the real-time clock.
- Implement an interface, in C programming-language, to utilise the USB interface.
- Implement an operating system, in C programming-language, to manage housekeeping.

## 1.6 Thesis Overview

The literature review in Chapter 2 starts with a discussion regarding average current-mode control. The key differences between voltage- and current-mode control are firstly identified, after which the benefits of current-mode control are discussed. Current-mode control is then split into peak- and average- current-mode control and the basic operation of each mode of control is explained. The disadvantages of peak current-mode control and the advantages of average current-mode control are listed. It is concluded that average current-mode control is the most applicable with regard to the AR control scheme.

The existence of natural voltage-balancing is investigated within two converter topologies: A CAR which is represented by a two-AR stack and two separate loads and a cascaded back-to-back converter which is represented by a two cell-stack and an output-parallel load. A converter model is incorporated consisting of an ideal transformer with a time-varying turn ratio dependent on the converter switching-function. This model is expanded for each converter topology to a circuit model representing total- and difference-parameters. Frequency-domain analysis leads the quantification of a weak- and strong rebalancing mechanism within a CAR and a second order rebalancing equation for a cascaded back-to-back converter. Weak rebalancing is only present with interleaved switching. The existence of natural voltage-balancing is thus confirmed and quantified.

The literature review is concluded with a discussion regarding a discrete-time modelling technique for modelling PWM comparators. The norm is to linearise this comparator together with the power stage as a linear gain. This model accuracy lessens at frequencies higher than the switching frequency and it does not account for frequency anomalies caused by PWM comparators. The discrete-time model however, accounts for PWM signals having image components at even harmonics of the switching frequency as well as aliasing of high frequency components down to the lower frequencies. The discrete model is incorporated in the current-loop to establish a single-frequency stimulus small-signal response. This model is a functional tool in shedding light on the sampling effects of PWM comparators. It can however not be used as a compensator design-tool because the compensator transfer-function is required to quantify the model in the first place.

The focus in Chapter 3 is on the main controller hardware design. The hardware is categorised as measurements, controller PCB and fibre-optic interface PCB. The measurement PCB designs are explained with emphasis on measurement noise and Electromagnetic Interference (EMI) prevention as well as protection circuitry. Each measurement channel starts with a measurement PCB followed by a scaling and sampling process implemented on the controller PCB.

This PCB design is discussed in terms of the FPGA and its supporting circuitry, the secondary measurement-circuitry, the parallel communication, the peripheral circuitry and the Double Data Rate (DDR) memory. The parallel communication facilitates the link between the FPGA and the fibre-optic interface PCB. It accounts for voltage-level differences between PCBs as well as a degree of FPGA protection. The peripheral circuitry is classified as circuitry adding functionality above and beyond the SST three-phase voltage step-down. It consists of flash memory, a real-time clock and a USB interface. The non-volatile flash memory is incorporated to facilitate data storage and a real-time clock is incorporated to facilitate data time-stamping. The USB interface is incorporated to facilitate data download to any USB storage device. The peripheral circuitry is thus centred around data capture and download for analytical and statistical use. DDR memory is incorporated to achieve a higher level of firmware and software design freedom. Emphasis is placed on PCB design aimed at preserving DDR signal-integrity.

The fibre-optic interface PCB design is discussed in terms of its requirements established by

the total SST communication layout. The design is also steered by the bidirectional fibre-optic channel, as design building block, as well as the interface between this PCB and the controller PCB.

In Chapter 4, the AR role within the SST is explained, after which its control scheme is discussed. The choice of unipolar voltage switching, with the implementation of two PWM carriers, is explained. The double-loop control scheme is designed by first separating the inner current-loop. The current-loop plant is linearised using a state-space averaging technique and the current-loop compensator is subsequently designed. This design utilises graphical methods guided by an analog-control criterion. The voltage-loop is then separated from the control scheme and the voltage-loop plant is linearised through circuit analysis and time averaging over a relatively long period. Graphical methods utilising the MATLAB<sup>®</sup> SISO design tool are then used to design the voltage-loop compensator.

Time domain simulations are presented to verify control functionality. A current-loop simulation is presented to emphasise the system startup-transient and the system response to current-loop reference steps. An AR simulation, incorporating the current- and voltage-loop, is presented to emphasise the system startup-transient and the system response to load steps.

The control implementation within the MC and CC is explained in terms of the current-loop, voltage-loop, startup sequence and error handling. The current-loop discussion highlights the input inductor-current measurement scaling process, the current-loop compensator implementation process and the particular PWM communication protocol. The voltage-loop discussion highlights the voltage-loop compensator implementation and the input-voltage scaling process. The startup sequence is explained in terms of the state progression, starting with the ping state, the initialise state, the active state and the shutdown state. Errors are classified as measurement errors and system errors and the system response to such errors is explained.

Test measurements are presented to confirm control-system functionality as a whole as well as successful control and circuit implementation. The tests presented are similar to the simulations presented earlier in the chapter. Normal system behaviour as well as the system response to current-loop reference steps is examined, while only implementing the current-loop. The system startup transient as well as the system response to load steps is examined, while implementing the complete control system.

The CAR role within the SST is explained after which the AR-control expansion is discussed in Chapter 5. The AR-control system is expanded to facilitate the control of  $N$  ARs. Interleaved switching, with the implementation of  $N$  PWM carrier-pairs, is explained. The double-loop control scheme is designed by first separating the inner current-loop. The current-loop plant model is obtained by expanding the AR current-loop plant model with a time averaging technique. The current-loop compensator is redesigned, again utilising graphical methods guided by an analog-control criterion. The voltage-loop is then separated from the control scheme and the voltage-loop plant model is obtained. The AR voltage-loop plant model is expanded in the same manner as done for the current-loop. Graphical methods utilising the MATLAB<sup>®</sup> SISO design tool are used to redesign the voltage-loop compensator.

Time domain simulations are presented to verify control functionality and natural voltage balancing in a two AR stack with two separate loads. A simulation is presented to emphasise the system startup-transient and natural voltage balancing with equal loads. Another simulation is presented to emphasise the system response to load steps in terms of natural voltage rebalancing. The load steps are implemented by stepping one of the two loads which qualifies in an external perturbation causing a voltage imbalance. Natural voltage rebalancing is then observed when the load is stepped back. The result is compared to the findings in Section 2.2.

The control implementation within the MC and  $N$  CCs is explained in terms of the current-loop, voltage-loop, startup sequence and error handling. The current-loop and voltage-loop discussions highlight the changes made in control firmware to facilitate the expanded control scheme. The startup sequence is explained in terms of the state progression, with emphasis on the modifications to accommodate  $N$  ARs. The system response to measurement errors and system errors is explained with emphasis on the modifications to accommodate  $N$  ARs.

Test measurements are presented to confirm control-system functionality as a whole, successful control and circuit implementation as well as natural voltage balancing and rebalancing. The tests presented are similar to the simulations presented earlier in the chapter. The system startup transient including natural voltage balancing is examined, while implementing equal loads. The system response including natural voltage rebalancing is examined, while implementing load steps. The natural voltage rebalancing result is compared to the findings in Section 2.2.

In Chapter 6, the DC-DC role within the SST is explained after which its control scheme is discussed. The double loop control scheme incorporates an outer voltage-loop and an inner current-loop which consists of three parallel current-loops. The current-loop design is explained in [12] and the voltage-loop design is started by separating it from the control scheme. The voltage-loop plant is linearised through circuit analysis and time averaging over a relatively long period. Graphical methods utilising the MATLAB<sup>®</sup> SISO design tool are then used to design the voltage-loop compensator. The fact that the AR voltage-loop and the DC-DC voltage-loop influence each other is considered within this design.

The implementation of the DC-DC control, in parallel with the AR control, within three MCs and  $3N$  CCs is explained in terms of the current-loop, voltage-loop, startup sequence and error handling. In the voltage-loop discussion the TPI bus-voltage scaling process and the voltage-loop compensator implementation are highlighted. The startup sequence is explained in terms of the state progression, with emphasis on the modifications to accommodate  $N$  DC-DC converters. The system response to measurement errors and system errors is explained with emphasis on the modifications to accommodate  $N$  DC-DC converters.

Three tests are presented to confirm control-system functionality as a whole as well as other aspects distinctive to each respective test. The first test presents a two-phase scaled SST to verify active output-current balancing with an output-parallel load. Normal system behaviour as well as the system response to load steps is examined. The second test presents a single-phase full-scale SST to verify successful operation at rated input-voltage as well as successful addition of the TPI and three-phase output load. Normal system behaviour as well as the system response to load steps is examined. The third test presents a three-phase full-scale SST to verify successful operation in terms of total cell bus-voltage balancing between phases as well as active output-current balancing. Normal system behaviour as well as the system response to load steps is examined.

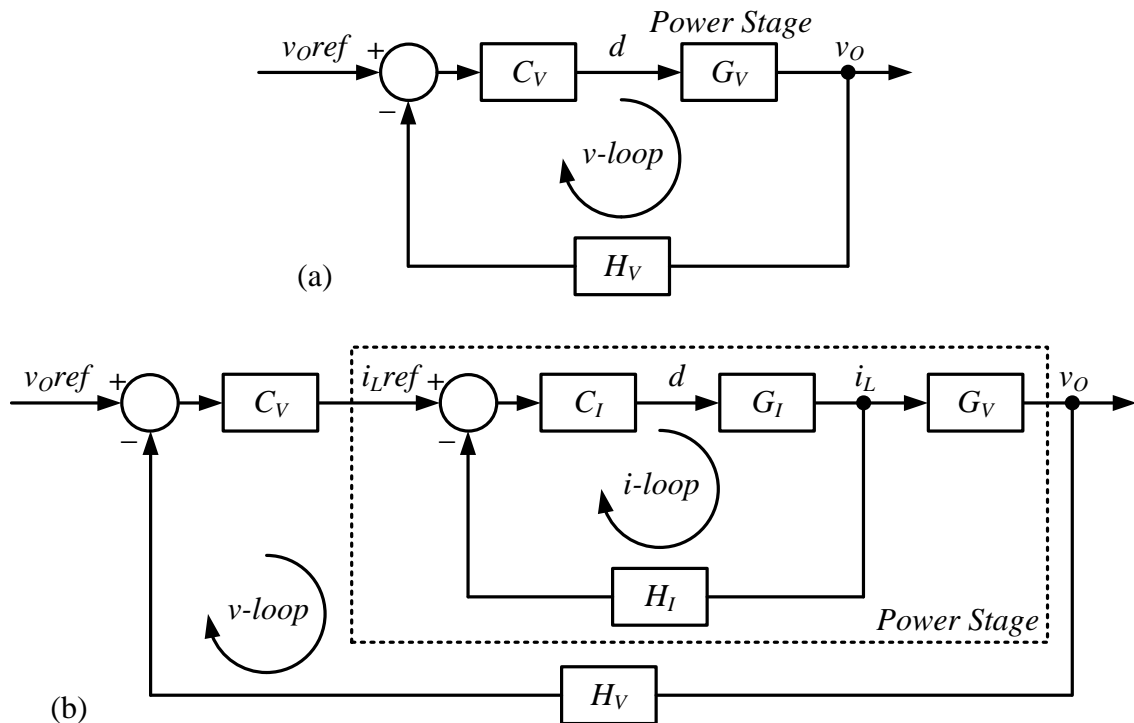
The thesis conclusion obtained from these chapters is presented in Chapter 7. A comprehensive project conclusion is also presented where the project outcome as well as future work is discussed.

## Chapter 2

### Literature Review

#### 2.1 Average Current-Mode Control

Two modes of control are reviewed for switching converters. These modes include voltage-mode control, where the output voltage is regulated by controlling the switching duty cycle, and current-mode control, where the output voltage is regulated by controlling the inductor current via the switching duty cycle. Voltage-mode control is thus a single loop scheme while current-mode control is a double loop scheme with an inner current-loop and an outer voltage-loop, as shown in Figure 2.1.



**Figure 2.1:** (a) Voltage-Mode Control Scheme; (b) Current-Mode Control Scheme

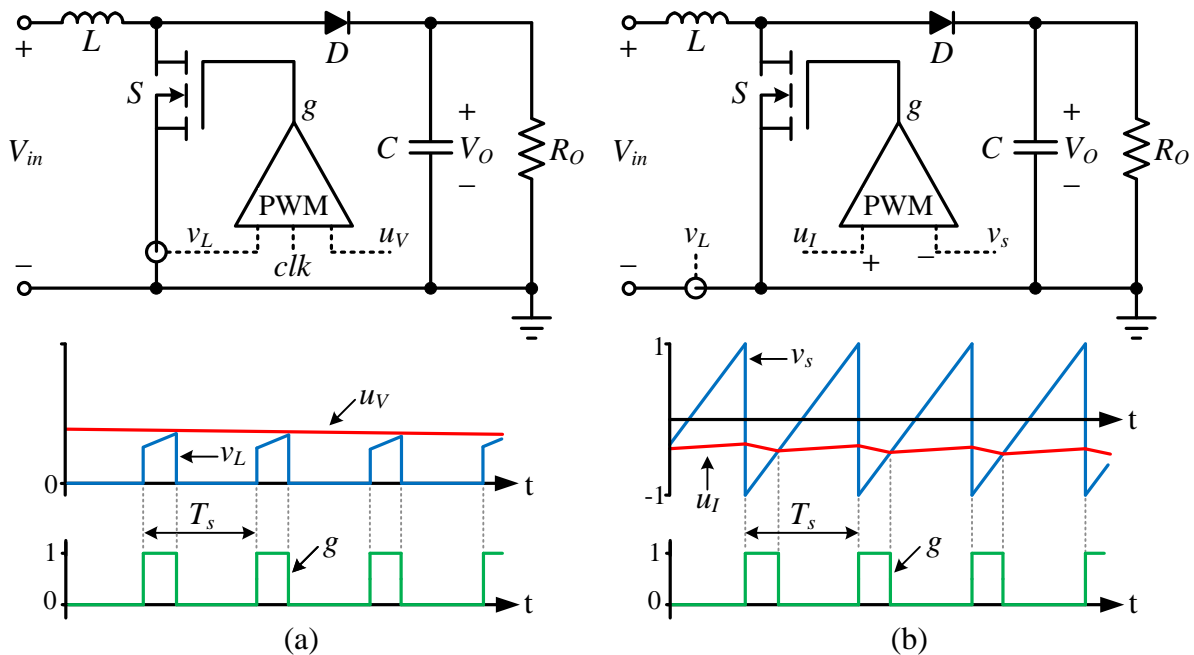
These two modes of control are compared in [13] where it is said that voltage-mode control is more familiar and that current-mode control can be difficult to analyse due to its double-loop scheme. This analysis however, is greatly simplified by recognising that the inner current-loop can be seen as a controlled current source.

Current-mode control also exhibits a few advantages over voltage-mode control:

- Analysing the voltage-loop, the second order system with  $L$  and  $C$  as reactive elements becomes a single pole system dominated by the  $C$  and  $R$  parallel impedance.
- The control-to-output transfer function with current-mode control is independent of  $V_{in}$ , unlike with voltage-mode control. This results in excellent line regulation<sup>1</sup>
- Proficiency with large load variation.
- Small performance deviation between continuous and discontinuous conduction mode.
- Built in current limiting.

Some switching converter applications are suited for voltage- and current-mode control. Some switching converter applications however require current-mode control due to the need for current as well as voltage control. The AR is an application where the input current is controlled to be sinusoidal and in phase with the input voltage while the output voltage is controlled to have a predefined average value. Current-mode control can be divided into three categories namely peak-, average- and hysteretic current-mode control.

The first two current modes of control are compared in [14] with the key differences depicted in Figure 2.2. In peak current-mode control the switch current is often measured<sup>2</sup> and compared to the voltage-compensator output,  $u_V$ . This comparison determines when the switch is turned off. A clock determines when the switch is turned on and thus determines the switching frequency. In average current-mode control the inductor current is directly measured and compared to the voltage-compensator output. The current error is fed to a high gain integrating current compensator. This compensator output,  $u_V$ , is then compared to a carrier signal,  $v_s$ , to determine the switch gating signal,  $g$ .



**Figure 2.2:** (a) Peak Current-Mode Control Scheme; (b) Average Current-Mode Control Scheme

<sup>1</sup>Line regulation is defined as the change in output voltage caused by a change in input voltage.

<sup>2</sup>The switch current is equal to the inductor current while the the switch is turned on.

Peak current-mode control exhibits a few disadvantages:

- It requires a very high-bandwidth current sensor.
- It has poor noise immunity because the instantaneous current measurement is compared to the voltage-compensator output. System noise, such as spikes generated as the switch is turned on, can cause subharmonic oscillation.
- The control is inherently unstable with subharmonic oscillation, when the duty ratio is greater than 0.5. This instability can be removed with slope compensation where a compensating ramp is applied to the PWM comparator. The required slope of this ramp however, is not constant for all converter topologies.
- The peak-to-average current error in AR converters is of concern. The peak current tracks its reference, however the average current does not. This error is more severe at discontinuous conduction mode.

Average current-mode control overcomes these disadvantages with its high gain integrating current compensator. The gain and bandwidth of this compensator can be adapted for optimum performance. The adapted bandwidth can be approximately equal to the peak current-mode control bandwidth, however the low frequency gain will be much greater. Average current mode control exhibits the following advantages:

- It displays excellent noise immunity because the carrier signal drops to its lowest value when the switch is turned on. This value is sufficiently far away from the corresponding current-compensator output value.
- Slope compensation is not required, however to avoid instability, there is a limit to the adapted current-loop gain at the switching frequency.
- The average current tracks its reference with high accuracy, even in discontinuous conduction mode.

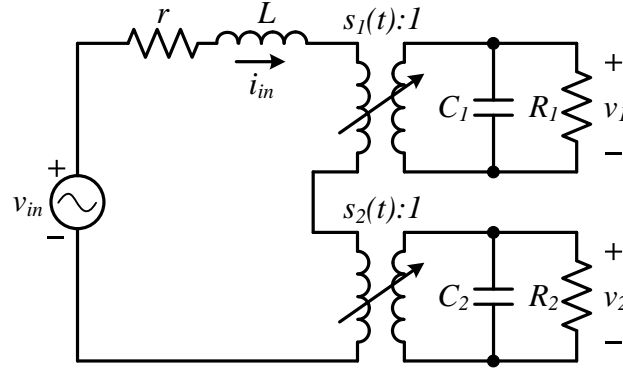
It is concluded from these two comparisons that current-mode control, in general, offers great advantages when controlling switching converters. The advantages in utilising average current-mode control to control the SST AR are also apparent. This is because of the importance of effective SST input-current control. The DC-DC controller, on the other hand, might make use of either peak- or average-current mode control.

## 2.2 Natural Voltage Balancing

All multilevel-converter topologies require some clamping mechanism to distribute the voltage equally among the different levels. The SST includes three stacks of cascaded back-to-back converters, one stack per phase. There are several active balancing techniques for cascaded converters, however natural balancing mechanisms are identified and analysed for cascaded ARs[9] as depicted in Figure 5.1, and cascaded back-to-back converters[10] as depicted in Figure 6.2.

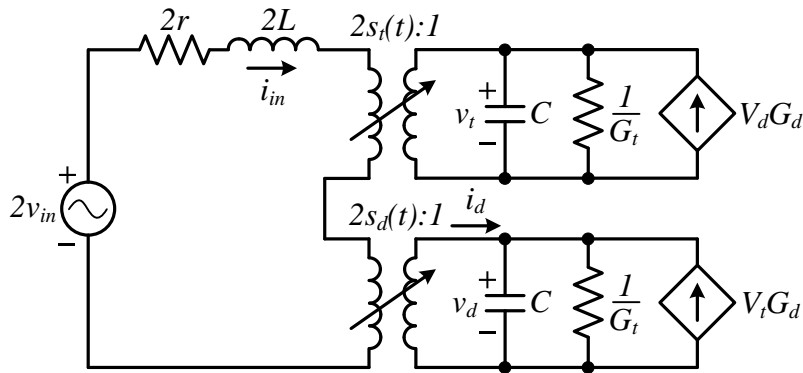
The cascaded AR study models a single full-bridge converter as an ideal transformer. This transformer has a time varying turn-ratio dependent on the switching function  $s(t)$ . The model is expanded to model two cascaded ARs with the circuit shown in Figure 2.3.




**Figure 2.3:** Circuit Model of Two Cascaded Active-Rectifiers

To study the unbalance in the circuit, the model is again expanded to a circuit in terms of  $d$  and  $t$  parameters. Figure 2.4 depicts this circuit with  $v_d$  the difference, or unbalance, voltage and  $v_t$  the total voltage. The switching functions and loads are represented as:

$$\begin{aligned} s_t &= \frac{1}{2}(s_1 + s_2) & s_d &= \frac{1}{2}(s_1 - s_2) \\ G_t &= \frac{R_1 + R_2}{2R_1R_2} & G_d &= \frac{R_1 - R_2}{2R_1R_2} \end{aligned} \quad (2.2.1)$$


**Figure 2.4:** Circuit Model of Two Cascaded Active-Rectifiers in Terms of  $d$  and  $t$  Parameters

The circuit is analysed in the frequency domain with  $v_{in}$  defined as a DC source and the two ARs operating at constant and equal duty cycles,  $d$ . The input inductor-current can be found as:

$$\begin{aligned} I_{in} &= \frac{V_{in} - V_t S_t(\omega) - V_d S_d(\omega)}{Z(\omega)} \\ Z(\omega) &= r + j\omega L \end{aligned} \quad (2.2.2)$$

The current  $i_d$  can thus be written in terms of  $v_{in}$ ,  $v_t$  and  $v_d$ , where  $*$  denotes the convolution operator:

$$I_d(\omega) = \left( 2 \frac{V_{in}}{Z(\omega)} * S_d(\omega) \right) - \left( 2V_t \frac{S_t}{Z(\omega)} * S_d(\omega) \right) - \left( 2V_d \frac{S_d}{Z(\omega)} * S_d(\omega) \right) \quad (2.2.3)$$



The steady-state influences on  $i_d$  are examined and it is found that the source  $V_{in}$  and the value of  $V_t$  have no influence on this current. It is however found that  $i_d$  is influenced by  $v_d$  and is always negative. This current thus always extracts unbalance energy from the  $v_d$  capacitor. The current  $i_d$  is defined as:

$$I_d = V_d \frac{\sin^2(\pi d) r}{4\pi^4 L^2 f_s^2} \quad : \text{ with interleaved switching} \quad (2.2.4)$$

$$I_d = 0 \quad : \text{ with ordinary switching}$$

with  $f_s$  defined as the switching frequency. Interleaved switching is explained in Section 5.2.1. With ordinary switching,  $s_d = 0$  and therefor  $I_d = 0$  under all circumstances.

The  $V_d$  steady state value is established to be zero with equal loads,  $R_1$  and  $R_2$ , and alternatively a function of the unequal loads. Analysis of rebalancing after an external perturbation with ordinary switching yields the, always present, strong rebalancing mechanism:

$$v_d(t) = V_d(0)e^{-\frac{t}{\tau}} \quad (2.2.5)$$

$$\tau = \frac{C}{G_t} \quad (2.2.6)$$

with  $V_d(0)$  representing the initial deviation from steady state. To study any rebalancing separate from the strong rebalancing mechanism, the ARs are unloaded with  $R_1 = R_2 \rightarrow \infty$  and  $G_t \rightarrow 0$ . The analysis after an external perturbation yields the weak rebalancing mechanism:

$$v_d(t) = V_d(0)e^{-\frac{t}{\tau}} \quad (2.2.7)$$

$$\tau \approx \frac{\sin^2(\pi d) r}{4\pi^4 L^2 f_s^2} \quad (2.2.8)$$

It is concluded that unloaded rebalancing is not possible with ordinary switching. During loaded interleaved operation the rebalancing is due to a combination of the weak and strong rebalancing mechanisms. The strong rebalancing mechanism dominates due to the dimensioning of the load and filter components determining the strength of the strong and weak rebalancing mechanisms respectively.

The cascaded back-to-back converter study also models a single full-bridge converter as an ideal transformer. This transformer has a time varying turn-ratio dependent on the switching function  $s(t)$ . The model is expanded to model two cascaded back-to-back converters with the circuit shown in Figure 2.5. The front end of each converter is an AR, operating as a boost converter, back-to-back to a DC-DC converter connected in output parallel.

To study the unbalance in the circuit, the model is again expanded to a circuit in terms of  $d$  and  $t$  parameters. Figure 2.6 depicts this circuit with  $v_d$  the difference, or unbalance, voltage and  $v_t$  the total voltage etc.

The circuit is analysed in the frequency domain with the AR switching function attained from a main controller. The DC-DC converters operate with interleaved switching, at equal and constant duty cycles,  $d$ . A numerical solution for the AR switching functions is approximated and the DC-DC switching functions are expressed in exponential Fourier form. It is shown by combining these switching functions that  $v_d$  is zero at steady state.

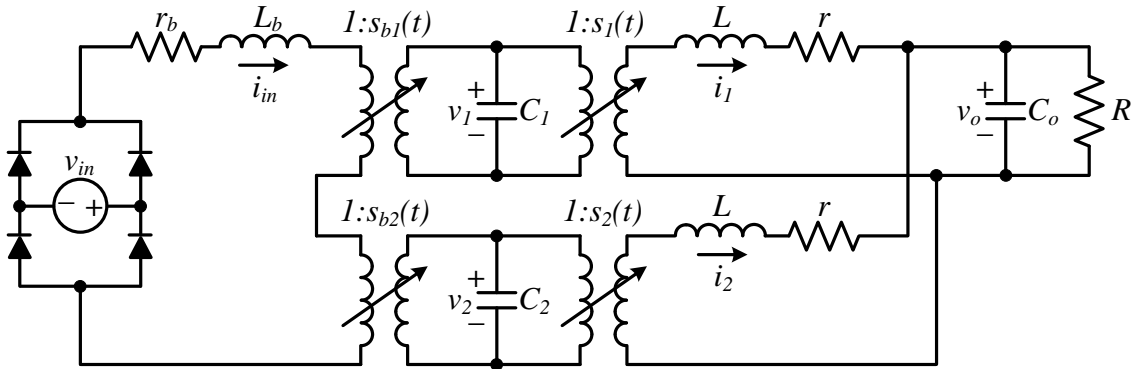


Figure 2.5: Circuit Model of Two Cascaded Back-To-Back Converters

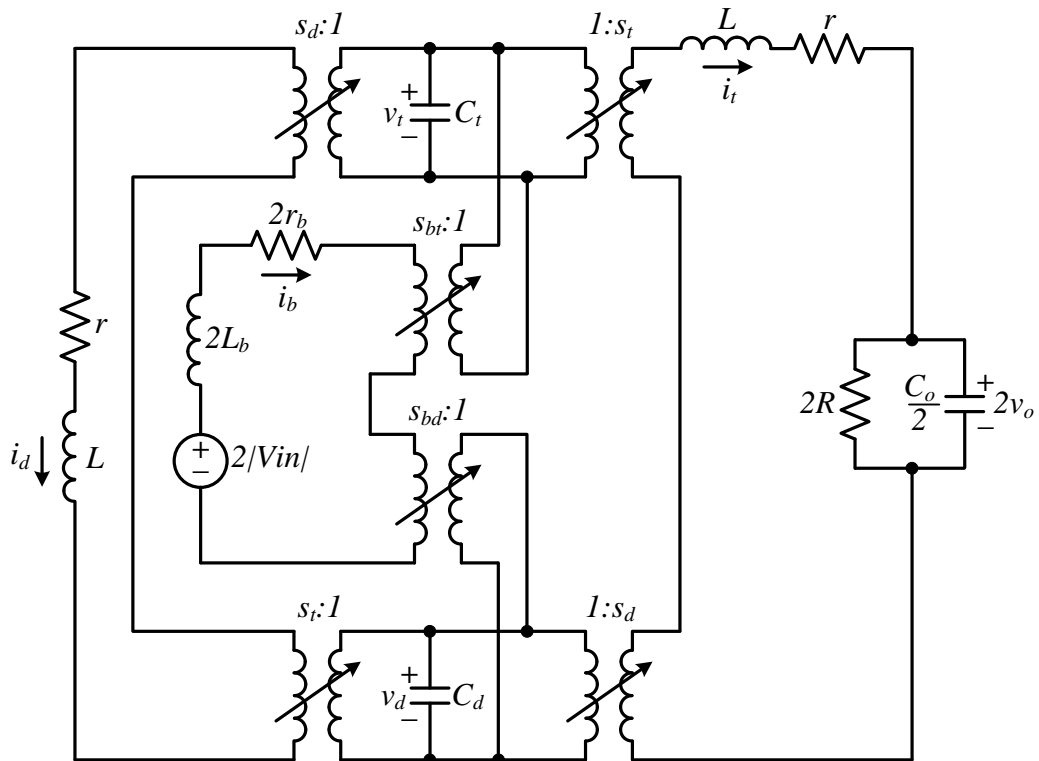
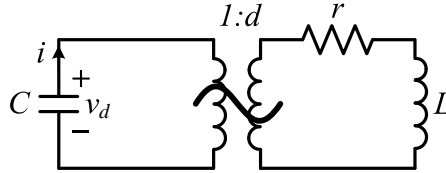


Figure 2.6: Circuit Model of Two Cascaded Back-To-Back Converters in Terms of  $d$  and  $t$  Parameters

It is further established that the current through the capacitor,  $C_d$ , is dominated by the DC term of the difference current,  $i_d$ . From this it is concluded that the balancing process can be analysed using time averaging techniques within the  $i_d$  subcircuit. The RLC components of this subcircuit together with the result of time averaging the switching function,  $S_t$ , yields the rebalancing circuit shown in Figure 2.7. Rebalancing can thus be expressed as the second order differential equation:

$$0 = \frac{L}{d^2} \frac{di}{dt} + \frac{r}{d^2} + \frac{1}{C} \int_0^t id\tau \quad (2.2.9)$$

$$i(0) = dI_d(0), v(0) = v_d(0) \quad (2.2.10)$$



**Figure 2.7:** Equivalent Rebalancing Circuit

These two studies verify the existence of natural voltage balancing within each phase stack of the SST. The prerequisite is interleaved switching. It is also verified that the cascaded ARs can be tested separately from the DC-DC converters while demonstrating natural voltage balancing. The only form of active balancing necessary within the SST, is thus the balancing of the power delivered to the TPI by each phase-stack.

## 2.3 Discrete-Time Modelling of PWM Comparators

Control loops containing PWM comparators, as with many switching-converter controllers, demonstrate a non-linear nature which complicates analytical analysis. These loops are conventionally linearised by combining the comparator with the power stage and replacing this combination with a linear gain. This continuous-time model has some shortcomings. The model accuracy decreases at high frequencies, starting at the switching frequency region. This reduces the accuracy of stability analysis. Another phenomenon which the model does not account for, is frequency translation which causes false components and excess noise.

An ideal comparator model is proposed in [15] which includes the comparator and power stage. This model consists of a high gain followed by saturation to the rails. The small signal behaviour of this model is determined by comparing the outputs of two identical comparator models operating at 50% duty cycle, as shown in Figure 2.8. The un-perturbed reference model input is the carrier signal,  $c(t)$ , with frequency,  $f_s$ , while the other model input is a small-amplitude perturbation,  $y(t)$ , superimposed on the same carrier signal. The small signal PWM response,  $\tilde{p}(t)$ , is thus the difference between the perturbed model output and the un-perturbed model output.

Figure 2.9 shows that the comparator is saturated and uninfluenced by perturbation except for short periods of time,  $\Delta t$ , at carrier zero-crossings. The comparator acts as a linear gain,  $G$ , during these periods and a zero gain otherwise. The period can thus be expressed as:

$$\Delta t \approx \frac{2V_{DD}}{|\dot{c}_0| G} \quad (2.3.1)$$

with  $|\dot{c}_0|$  the slope of the carrier at zero-crossings.

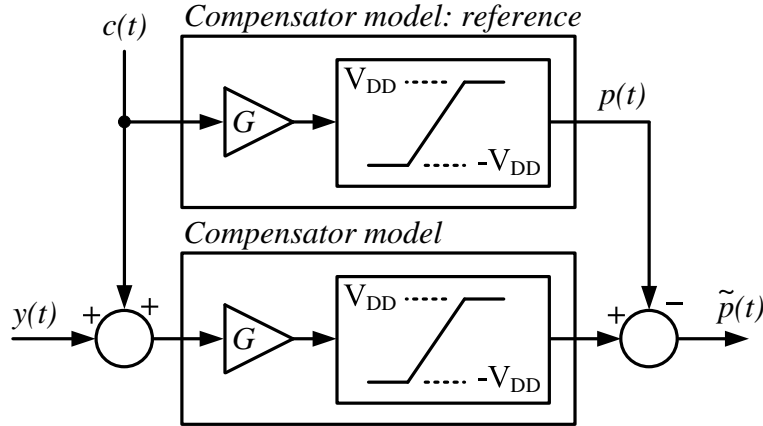


Figure 2.8: Ideal Compensator Small-Signal Model

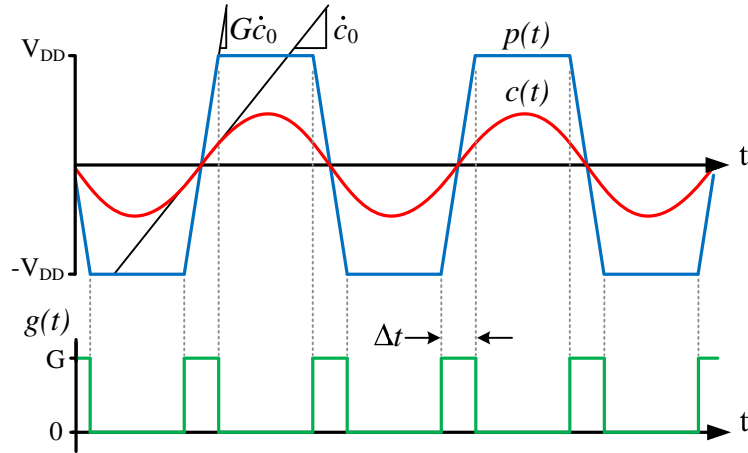


Figure 2.9: Ideal Compensator Signals

The small signal PWM response,  $\tilde{p}(t)$ , is thus the product of the perturbation signal,  $y(t)$  and a pulse train,  $g(t)$ . This pulse train has a frequency of  $2f_s$  and each pulse has a duration  $\Delta t$  and an area of:

$$A = G \cdot \Delta t \approx \frac{2V_{DD}}{|\dot{c}_0|} \quad (2.3.2)$$

It is clear that the area of each pulse is independent of  $G$  and that  $\Delta t \rightarrow 0$  for  $G \rightarrow \infty$ . This results in the approximation of  $g(t)$  as a Dirac comb. Multiplication with  $g(t)$  is thus the equivalent of sampling at a frequency of  $2f_s$  and subsequently multiplying with the effective comparator gain:

$$K = \text{mean}[g(t)] = 2f_s \cdot A = 4V_{DD} \frac{f_s}{|\dot{c}_0|} \quad (2.3.3)$$

This model successfully represents the PWM comparator in that it accounts for PWM signals having image components at even harmonics of the switching frequency. It also accounts for aliasing of high frequency components down to the lower frequency region.

This derived framework is further examined in [16]. A method is discussed to determine the single frequency narrow-band input/output transfer function,  $K_s(f)$ , of the comparator. The switch-mode control-loop model consists of a comparator block, loop filter,  $H_s(s)$  and external carrier signal,  $V_{ext}(t)$ , as shown in Figure 2.10. The comparator block includes the physical comparator together with the switching power stage. The loop filter includes the compensator and plant  $s$ -domain transfer functions.

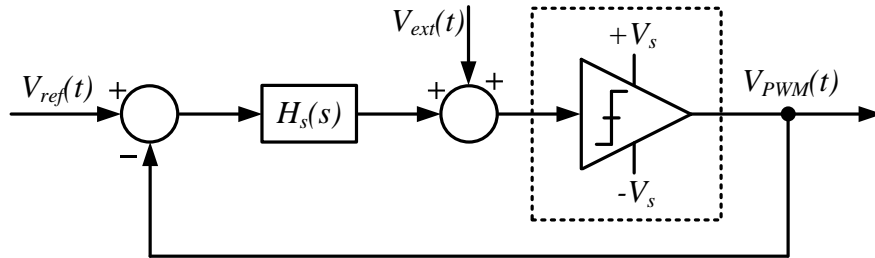


Figure 2.10: Switch-Mode Control-Loop Model

As mentioned, the comparator block is the equivalent of a sampler together with the gain,  $K$ . This produces Dirac delta pulses which propagate through  $H_s(s)$  and are thus superimposed on the carrier and again sampled by the comparator. This feedback loop can be represented in discrete-time, as shown in Figure 2.11. because the comparator input is ignored at all times except during the sampling instances.

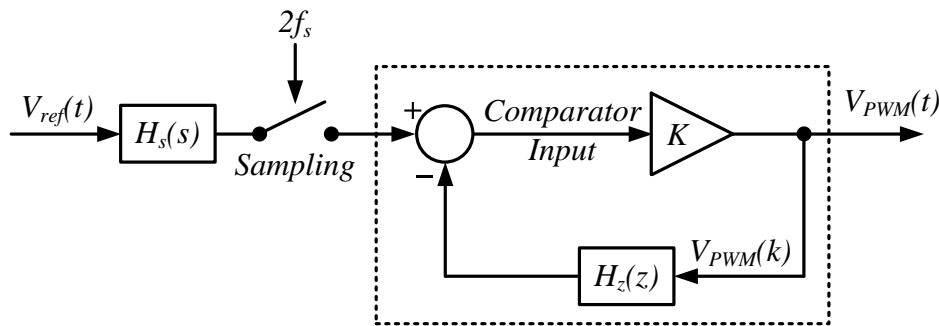


Figure 2.11: Continuous-Discrete Control-Loop Model

The  $z$ -domain equivalent of  $H_s(s)$  is determined by the following steps:

- Expand  $H_s(s)$  into partial fractions.
- Implement transformation  $z = \exp(s \cdot (2f_s))$ , thus using the Impulse Invariance Method.
- Scale the gain down by the sample rate.
- Subtract impulse response at  $k = \text{zero}$ .

This subtraction is necessary because the feedback of the current comparator-transition cannot affect the timing of that same transition. It does however affect the timing of following transitions. The discrete time feedback loop can be expressed as the compensator transfer function:

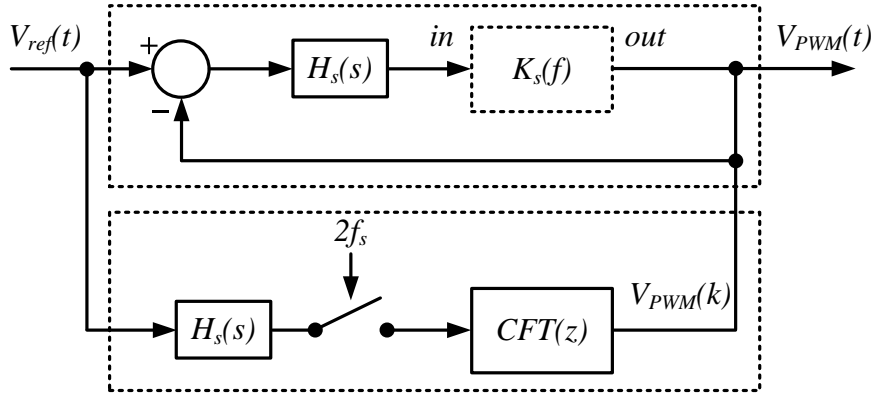
$$CTF(z) = \frac{K}{1 + K \cdot H_z(z)} \quad (2.3.4)$$

The input to output transfer function of the continuous-discrete control-loop model is thus given as:

$$G_{ref-out}(s) = H_s(s) \cdot CTF(z) \quad (2.3.5)$$

The  $s$ - and  $z$ -domain are combined in this transfer function and it should thus be analysed carefully. The analysis starts with a single-frequency sinusoidal stimulus as input. Its amplitude and phase are altered by the loop filter,  $H_s(s)$ , resulting in an altered sinusoidal steady-state response. The result is sampled at  $2f_s$  which leads to a spectrum consisting of a component at the stimulus frequency together with spectral images at multiples of the sampling frequency. The amplitude and phase is then modified by the  $z$ -domain loop which has a period of  $2f_s$ . This modification is described by  $CTF(z)$ . The continuous-time output is a periodic spectrum containing a component at the stimulus frequency and at spectral images. This output can be observed through a narrow-band filter, centred at the stimulus frequency, to determine the amplitude and phase modifications caused by the mixed-domain system.

The single-frequency stimulus method of analysis is used to determine the continuous-time comparator transfer function,  $K_s(f)$ . The approach, as depicted in Figure 2.12, is to determine the single-frequency response at both the input and output of the comparator.



**Figure 2.12:** Continuous Comparator Frequency Response

The comparator output frequency response is described in Eq. 2.3.5 and the comparator input frequency response is given as:

$$G_{ref-in}(s) = H_s(s) [1 - H_s(s) \cdot CTF(z)] \quad (2.3.6)$$

This leads to the comparator transfer function:

$$K_s(f) = \frac{G_{ref-out}(s)}{G_{ref-in}(s)} = \frac{K}{1 + K \cdot H_z(z) - K \cdot H_s(s)} \quad (2.3.7)$$

while defining the stimulus frequency,  $f$ , and the sample time,  $T_s$ , as:

$$s = j2\pi f \quad T_s = \frac{1}{2f_s} \quad z = e^{sT_s} \quad (2.3.8)$$

The entire system, as shown in Figure 2.10, can thus be evaluated in the continuous-time domain to establish its single-frequency stimulus small-signal response. This response is valid for any frequency, even beyond the switching frequency. Frequency images caused by the sampling process are however not accounted for by the  $s$ -domain model.

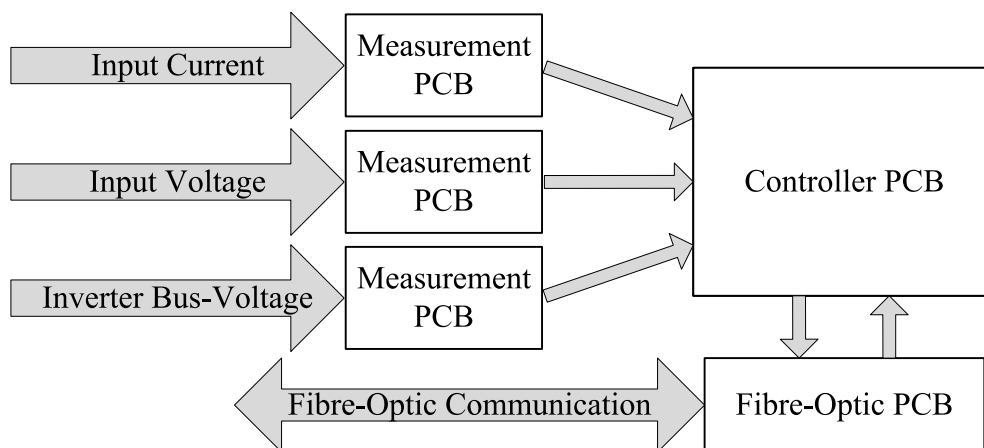
As a whole this model is a functional tool. It sheds light on the underlying sampling characteristics of the PWM comparator widely used in switch-mode control. The drawback however is that the obtained  $s$ -domain frequency-response cannot simply be used in the compensator design process. This is because  $H_s(s)$  contains the compensator transfer function which means that this transfer function is required before eliciting  $K_s(f)$  and the  $s$ -domain frequency response.

## Chapter 3

# Main Controller Hardware Design

### 3.1 Introduction

The Main Controller (MC), together with the Cell Controller (CC)'s is responsible for the control of the input and isolation stages. To accomplish this jointly, three ingredients are necessary: measurements, calculations and communication. The MC thus comprises of three measurement PCBs, a fibre-optic interface PCB and the controller PCB. Figure 3.1 depicts the basic MC structure.



**Figure 3.1:** Main Controller Block Diagram

The measurement PCB's convert the measurements from the single-ended analog domain to the differential analog domain and interface with the controller Printed Circuit Board (PCB). Here the measurements are further converted to the digital domain and are used as inputs to the control strategies. The outputs of the control strategies are, in turn, interfaced with the fibre-optic PCB. This PCB converts the outputs to the optic domain for communication with the respective CC's and between the fibre-optic PCB's of each phase.

In this chapter the design of the MC hardware present in a single phase is described. The MC requirements are analysed and broken down to clarify certain design and component decisions. The hardware discussed is tripled in the full-scale Solid-State Transformer (SST), one set is implemented for each phase. There are a few features that are not directly tripled. They are noted clearly.



## 3.2 Measurements

The measurements needed for the control strategies are taken from different physical locations within the SST. This leads to the unfortunate necessity of lengthy conducting wires from where the measurements are taken, to the MC. Differential interfaces are thus used to minimize the even-order harmonics and maximize common-mode noise immunity of the different measurements. A Measurement PCB is placed as close as possible to where the physical measurement is taken, to convert it to a differential pair signal. Listed below are the five measurements needed as input for the control strategies:

- Input-inductor current  $I_L$
- Input voltage  $V_{ac}$
- Cell bus-voltage  $V_{cb}$
- Isolation-transformer input current  $I_t$
- Three-phase inverter bus-voltage  $V_{ib}$

The MC measures  $I_L$ ,  $V_{ac}$  and  $V_{ib}$ . These measurement PCB's will be discussed in the sections to follow. The  $V_{cb}$  and  $I_t$  measurements for each Cell are taken by the respective CC. This is because these measurements are physically located on each Cell and are in the close vicinity to the respective CC.

### 3.2.1 Input-Inductor Current Measurement

The input-inductor current is measured using an *LTS 6-NP*[17] LEM current transducer. This device converts the current measurement to a voltage output and supplies galvanic isolation<sup>1</sup> between its primary and secondary circuits. This specific current transducer was chosen for its primary current measuring range ( $\pm 19.2$  A) which is close enough to the input current parameter, as listed in Table B.3. It has a Bandwidth (BW) of 100kHz which is sufficiently higher than the current measurement sampling frequency, discussed in Section 4.4.1. The third important characteristic is voltage isolation. The device is rated at 3 kV<sub>RMS</sub>. This is lower than the input voltage parameter, as listed in Section 1.4, which means that extra isolation or an innovative measurement technique is necessary.

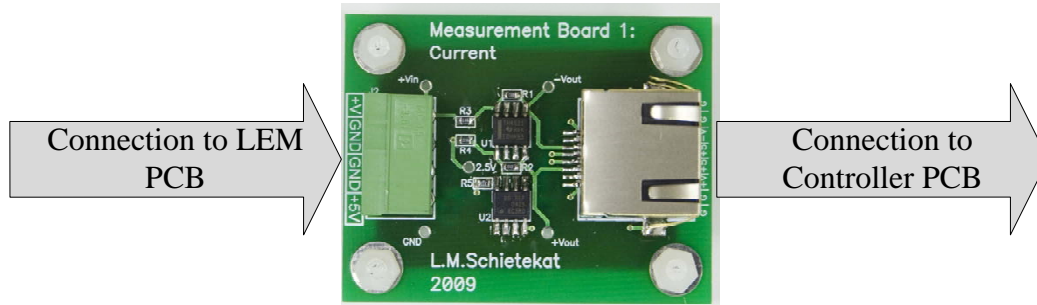
The function of the input-inductor current measurement PCB is to convert the single-ended input, received from the current transducer, to a differential, common-mode<sup>2</sup> output. The *THS4521*[18] fully differential op amp is used for this function. This device has several advantages, however only three are of interest here. It is a very low-power device which only uses a single supply and it offers a rail-to-rail output. It is also used in other applications within the MC where some of the other advantages are utilised. The op amp designed gain is discussed in Appendix A.1.1.

The current transducer output has a common-mode voltage of 2.5 V and the ADC, discussed in Section 3.3.2, has a common-mode input of 2.5 V. The common-mode voltage, throughout the measurement channel, is thus 2.5 V. The op amp on the measurement PCB requires a common-mode reference voltage which is supplied by a *REF1004-2.5*[19] reference diode.

<sup>1</sup>No current flow from one section to the next, only energy and/or information exchange by other means, electromagnetic in this case.

<sup>2</sup>The voltage common to the positive and negative differential signal which is coupled into the signals by the op amp.

This device offers a high accuracy reference voltage ( $\pm 20$  mV) at a low operating current. It also has an excellent temperature characteristic (5 mV maximum drift from  $-55$  °C to  $125$  °C). The input-inductor current measurement PCB is shown in Figure 3.2.



**Figure 3.2:** Input-Inductor Current Measurement PCB

The output of this PCB is fed to the Controller PCB using an 8-core twisted-pair cable, terminated by RJ-45 connectors on both ends. Two cores are used for the differential pair signal and two cores are used for the 5 V PCB supply voltage. The remaining four cores serve as ground connections. The measurement signals transported together with power and ground lines in a twisted-pair fashion, further counteract Electromagnetic Interference (EMI).

An unforeseen high-frequency op amp oscillation was detected during the hardware testing phase. This oscillation is due to the op amp driving a capacitive load, the twisted-pair cable connecting the input-inductor current measurement PCB and the controller PCB. A 1<sup>st</sup> order low-pass filter is implemented between the op amp and this cable as a solution to the oscillation. The filter is discussed in Appendix A.1.2.

### 3.2.2 Input-Voltage Measurement

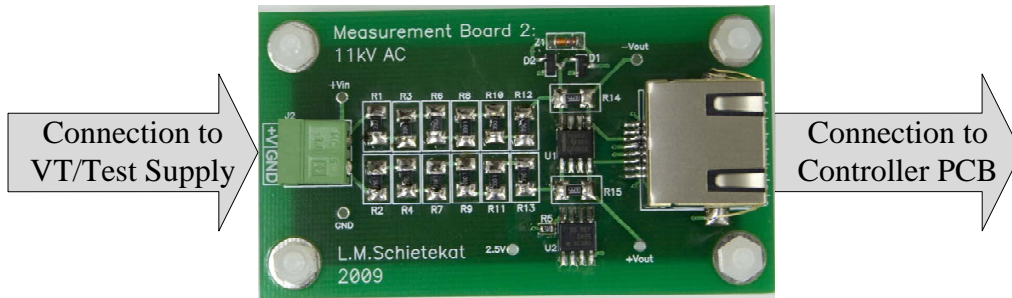
The input voltage is measured with one of two strategies, one being the use of a Voltage Transformer (VT). This strategy will be used where the SST is implemented in the field. The VT steps down the input voltage with a winding ratio of more or less:

$$\frac{N_1}{N_2} = \frac{100}{1} \quad (3.2.1)$$

The second strategy for measuring the input voltage is used in the SST development stage. A standard 230 V line-to-neutral source is stepped up with a transformer to generate the required input voltage, as listed in Section 1.4. This means that the 230 V input can be measured directly with the input-voltage measurement PCB.

As with the input-inductor current measurement PCB, the function of the input-voltage measurement PCB is to convert the single-ended input, received from the VT or test supply, to a differential, common-mode output. Again the *THS4521* fully differential op amp, together with the *REF1004-2.5* reference diode, is used for this function. The op amp designed gain for the test-supply measurement strategy is discussed in Appendix A.2.1. The input-voltage measurement PCB is shown in Figure 3.3.

The output of this PCB is fed to the Controller PCB in the same manner as with the input-inductor current measurement PCB. An issue of concern, which is not present on the input-inductor current measurement PCB, is the high input voltage. This voltage will be in the order of 100 V which is scaled to the range of 0 V to 5 V. The problem arises when connection to the



**Figure 3.3:** Input-Voltage Measurement PCB

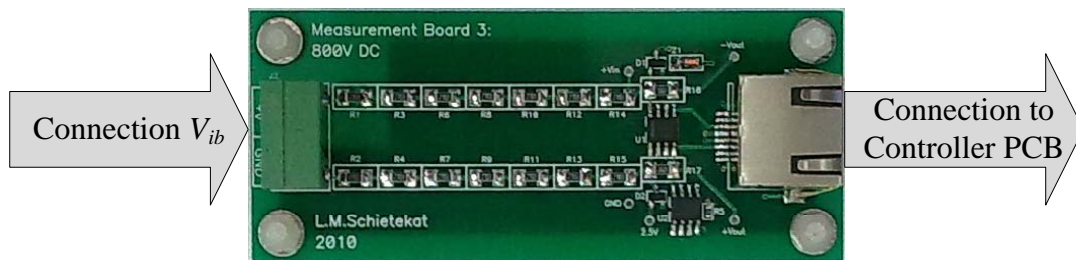
Controller PCB is lost while the high input voltage is connected. This issue, together with the protection-circuit solution is discussed in Appendix A.2.2.

As with the input-inductor current measurement PCB, an unforeseen high-frequency op amp oscillation was detected during the hardware testing phase. This oscillation is due to the op amp driving a capacitive load, the twisted-pair cable connecting the input-voltage measurement PCB and the controller PCB. A 1<sup>st</sup> order low-pass filter is implemented between the op amp and this cable as a solution to the oscillation. The filter is discussed in Appendix A.2.3.

### 3.2.3 Three-Phase Inverter Bus-Voltage Measurement

The TPI bus-voltage measurement is an instance of hardware which is not tripled for the three phases. Unlike the previous two measurement PCB’s, there are no conversion strategies present, such as a VT or current transducer. The input of this PCB is directly connected to the three-phase inverter bus. This bus is at the potential of 800 V, as listed in Section 1.4, which means extra care is taken with the design of the PCB to provide sufficient distance between component terminals with high potential-differences.

The function of the TPI bus-voltage measurement PCB is to convert the high-voltage differential input, received directly from the inverter bus, to a differential, common-mode output. Again the *THS4521* fully differential op amp, together with the *REF1004-2.5* reference diode, is used for this function. The op amp designed gain is discussed in Appendix A.3.1. The bus-voltage measurement PCB is shown in Figure 3.4.

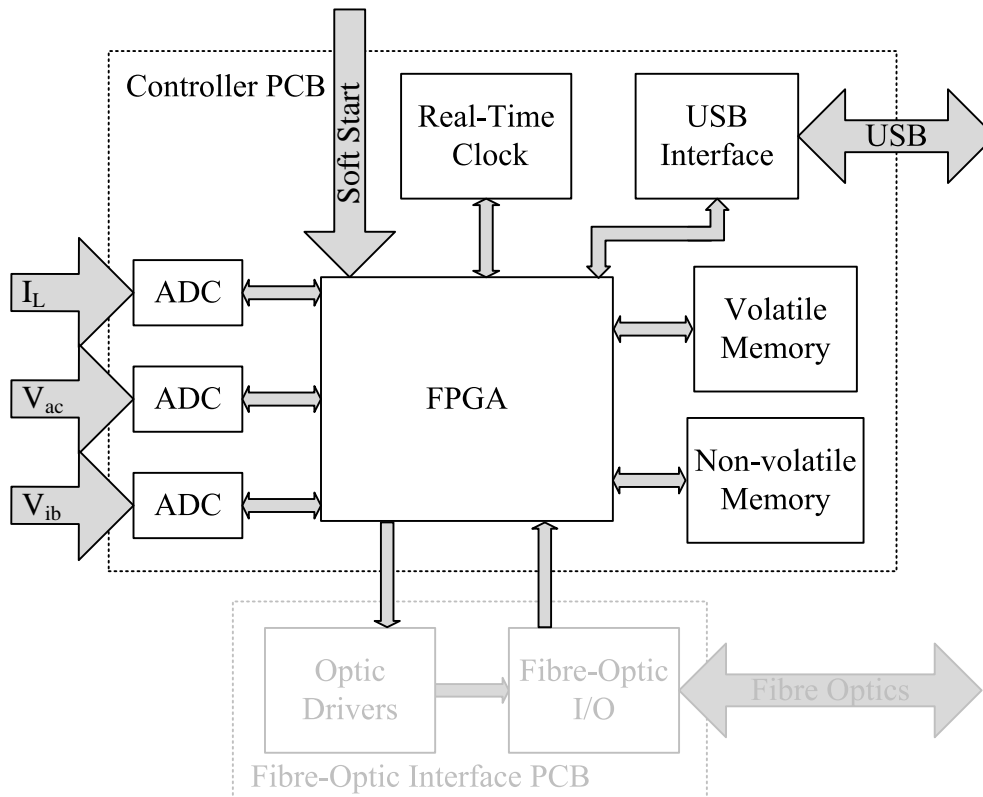


**Figure 3.4:** Three-phase Inverter Bus-Voltage Measurement PCB

The output of this PCB is fed to the Controller PCB in the same manner as with the input-voltage measurement PCB. The high input voltage is also of concern. The problem arises when the connection to the Controller PCB is lost while the high input voltage is connected. This issue, together with the protection-circuit solution is discussed in Appendix A.3.2.

### 3.3 Controller PCB

The controller PCB is where the main control strategies, as well as the peripheral functions, are implemented. Hardware is therefore present to handle measurement inputs, calculations, outputs and peripheral and supporting functionality. In the following sections the functionality and implementation of this hardware are described in detail. The controller PCB hardware block diagram is shown in Figure 3.5 and Figure 3.6 is a photograph of the controller PCB.



**Figure 3.5:** Controller PCB Hardware Block Diagram

#### 3.3.1 Field Programmable Gate Array and Supporting Circuitry

The design process involving the Field Programmable Gate Array (FPGA) together with its supporting circuitry is described in this section. Figure 3.7 depicts the controller PCB hardware in question:

The current trend among the digital-control community is to use either an FPGA or a Digital Signal Processor (DSP) or a combination of the two, for their control needs. The most prominent differences are that a DSP is a specialized form of processor programmed in a sequential programming language and an FPGA is a form of highly configurable hardware configured in a hardware description language [20]. The belief, up until recent years, is that if an application requires complex calculation, a DSP is the answer. If an application requires high-speed and possibly repetitive calculations, an FPGA is the answer. The decision, however, is not so clean cut. Most engineers choose an FPGA over a DSP on Millions of Instructions per Second (MIPS) comparison where FPGA technology is continually advancing in performance and density. This choice has come at a price. Designers who think in terms of software are forced

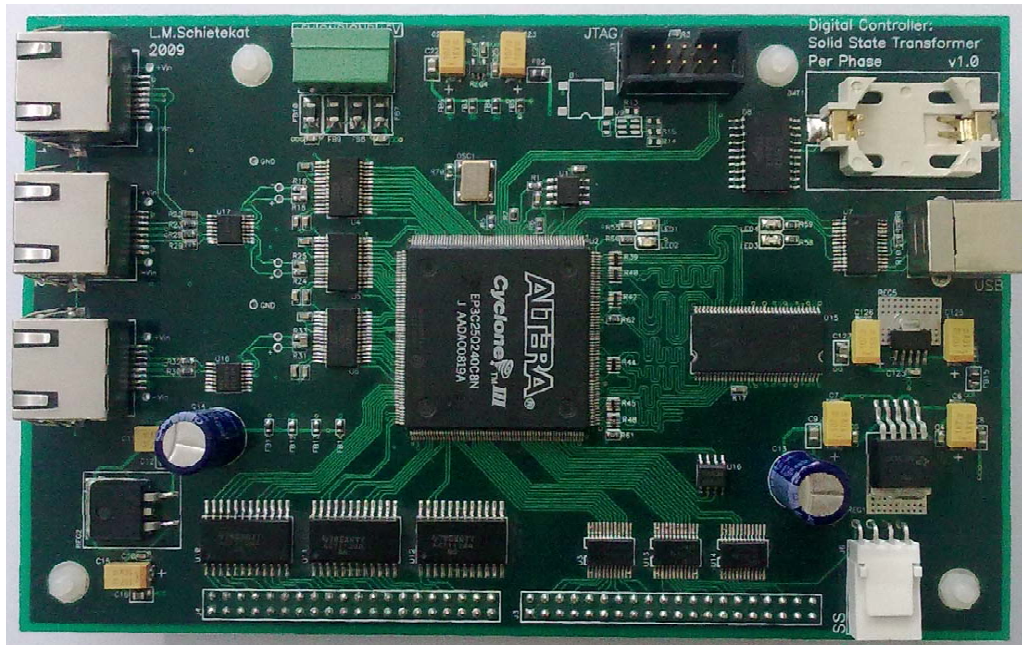


Figure 3.6: Controller PCB Photograph

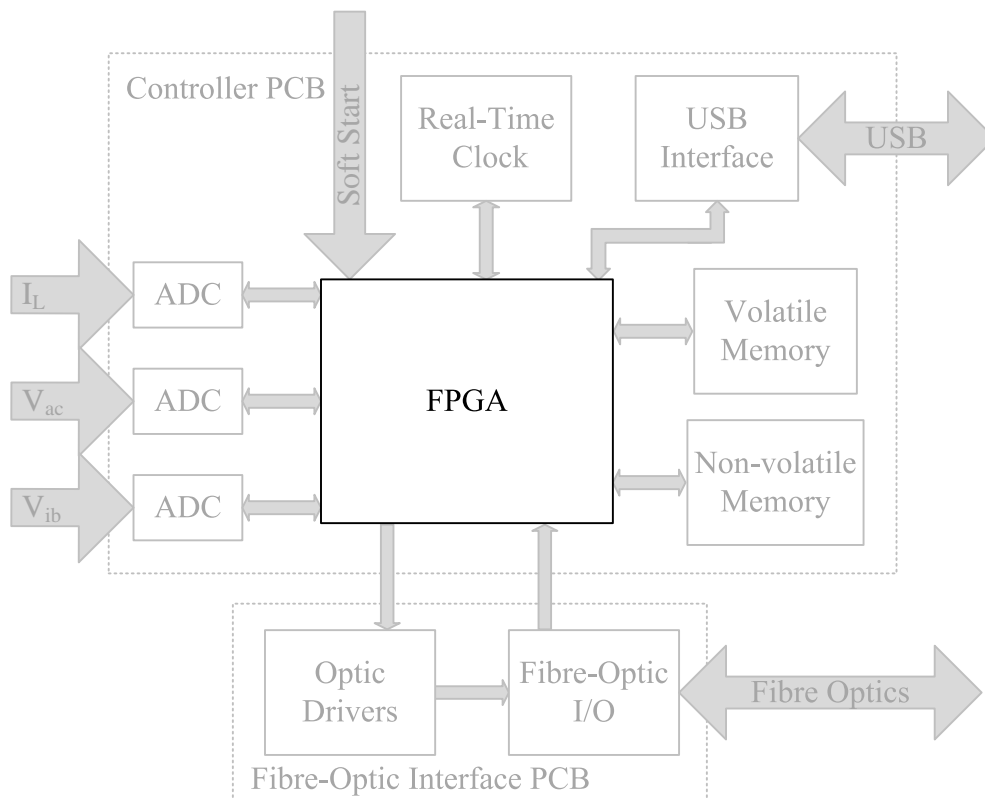


Figure 3.7: Controller PCB Hardware Block Diagram: FPGA



to think in terms of logic gates and Very-High-Speed Integrated Circuit Hardware Description Language (VHDL) code. Fortunately it is now possible to have the best of both worlds with algorithms available as Intellectual Property (IP) together with tools for incorporating IP into FPGA designs [21].

The Cyclone III *EP3C25QP240* FPGA from Altera was chosen. This third-generation Cyclone series is cost-optimized and memory rich. Its prominent attributes are listed below [22], p17:

- 24,624 Logic elements
- 594 Kbits of memory
- 66 Multipliers
- 4 PLLs
- 148 I/O Pin count
- Support for high speed memory interfaces
- Broad spectrum of pre-built and verified IP cores
- NIOS II embedded processors

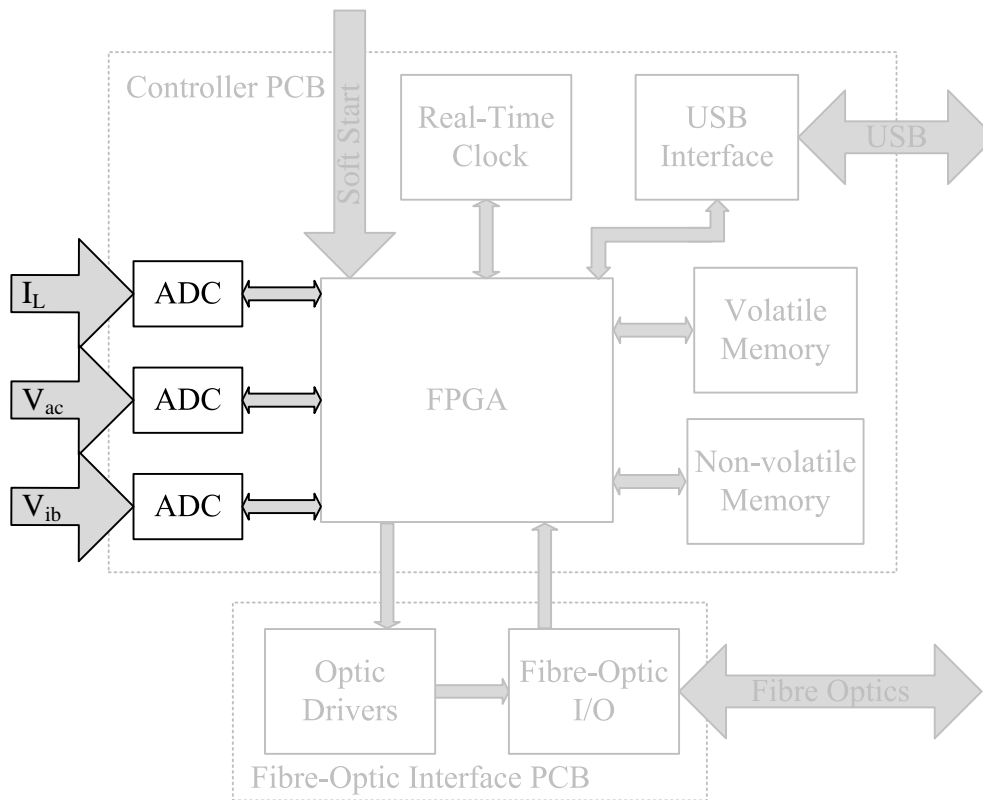
A NIOS II processor system is a microcontroller equivalent implemented on a single Altera chip. It refers to a NIOS II processor core, on-chip memory, a set of on-chip peripherals and interfaces to off-chip memory. The NIOS software is developed in an environment based on the GNU's Not Unix (GNU) C/C++ tool chain and Eclipse Integrated Development Environment (IDE) [23].

The FPGA uses volatile SRAM cells to store configuration data. The configuration data must thus be downloaded to the FPGA at every power up. The active serial configuration scheme together with a Joint Test Action Group (JTAG) scheme is used for this function[22],p281. The active serial scheme uses the *EPCS16*[24] external serial flash memory configuration device to configure the FPGA. The JTAG scheme, on the other hand, uses a 10-pin download cable, together with a USB-Blaster, to access the *.jic* or *.sof* file. The file is downloaded directly to the FPGA's internal serial flash loader which is a bridge between the JTAG interface and the active serial interface. The serial flash loader then programs the *EPCS16* which, in turn, programs the FPGA at the next power up.

The remaining supporting circuitry includes the FPGA input clock oscillator, the supply supervisor and two indication LEDs. The 20 MHz *CTZ FBC 20.0000*[25] clock oscillator, with a accuracy of 100 Parts per Million (ppm), is chosen with the following in mind: The Phase-Locked Loop (PLL) input frequency specification of 5-472.5 MHz, the ADC maximum sampling frequency of 53 MHz and available internal clock frequencies with PLL clock division and multiplication. The *TPS3106K33*[26] supply supervisor monitors the 3.3 V VCCIO and the 1.2 V VCCINT of the FPGA and triggers a reset when VCCIO drops below 2.941 V or VCCINT drops below 0.551 V. This reset signal should preferably be connected to the DEV-CLRn pin of the FPGA which is a chip-wide reset that clears all registers.

### 3.3.2 Measurement Conversion

The MC is responsible for three measurements, as discussed in Section 3.2. The three measurement PCB outputs are received on the controller PCB as differential inputs. Each one of these signals has secondary measurement circuitry located on the controller PCB, as shown in Figure 3.8. This circuitry consists of a differential op amp to scale the signal to the correct input voltage levels for the Analog to Digital Converter (ADC). The digital output of the ADC is directly connected to the FPGA where the measurements are used as inputs to the control strategies. This circuitry is explained in the following paragraphs.



**Figure 3.8:** Controller PCB Hardware Block Diagram: Measurement Conversion

As with the measurement PCBs, the *THS4522* op amps are used to scale the measurement signals. The last digit of the op amp product-code indicates that there are two op amps per package. This package can be used because all three secondary measurement circuits are located next to each other and so only two Integrated Circuit (IC)'s are used. The op amp gains of the input current, input voltage and the bus-voltage secondary measurement circuits are discussed in Appendix A.4.1, A.5.1 and A.6.1 respectively.

The *ASD807*[27] ADC is used in the secondary measurement circuits because of its fast sampling capabilities minimizing the delay from measurement to control output. It has a differential input, a 12-Bit output and a maximum sampling rate of 53 MHz. The designed sample rate of each secondary measurement circuit is dependent on the control strategies. The ADC has a pipelined architecture with a six clock cycle, input to output, delay. This means that each digital sample value is available six clock cycles after the sample is taken. This concept is depicted in Figure 3.9. The remaining ADC conversion parameters are discussed in Appendix A.7.1 and the ADC clock termination is discussed in Appendix A.7.2.

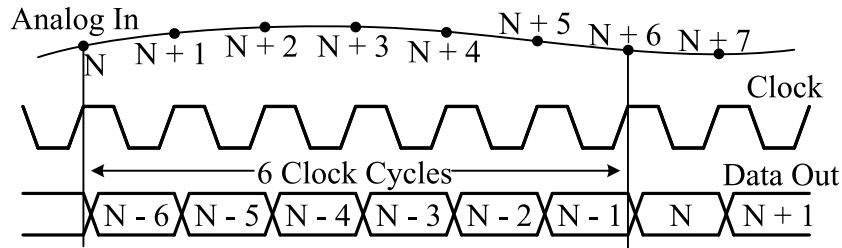


Figure 3.9: Pipeline Timing Diagram

There are two low-pass filters present in each of the secondary measurement circuits. Both are 1<sup>st</sup> order filters. The first is incorporated in the op amp circuit to prevent high frequency noise. The second is incorporated with the ADC analog-input capacitance. It is prescribed in [27] to a series resistor between the op amp and the ADC to decouple the op amp output from the capacitive load of the ADC to avoid gain peaking. This resistor and the capacitive load doubles as the second low-pass filter with an extra shunt capacitor to adjust its cut-off frequency. The filter designs of the input-inductor current, input voltage and the bus-voltage secondary measurement circuits are discussed in Appendix A.4.2, A.5.2 and A.6.2 respectively.

The ADC and the two op amps jointly form a sufficiently differential measurement channel. The only single ended section of the channel is the section between the physical measurement and the respective measurement PCB. This differential nature minimizes even-order harmonics and delivers an excellent common-mode noise immunity, as mentioned in Section 3.2. Figure 3.10 depicts the structure of all three measurement channels<sup>3</sup> where  $A1$  and  $A2$  are op amp gains and  $RATIO$  is the ADC conversion ratio.

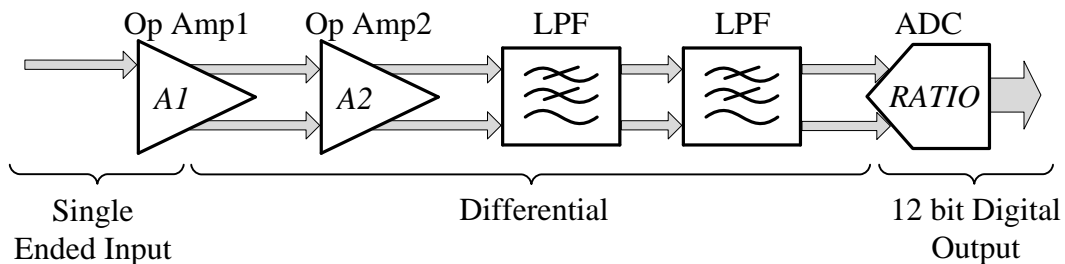


Figure 3.10: Measurement Channel Structure

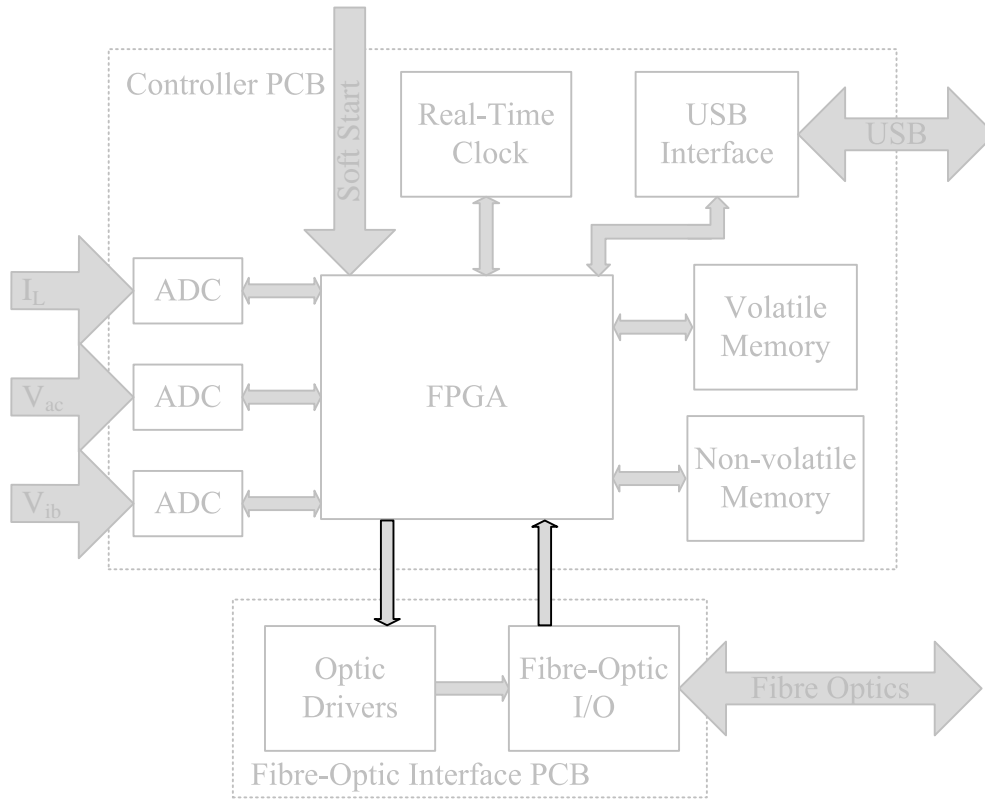
### 3.3.3 Parallel Communication

The parallel communication starts at the MC FPGA and continues through a parallel interface to the fibre-optic interface PCB, as shown in Figure 3.11. The communication continues through fibre-optic cables to the respective CCs. The hardware aspects of this communication are further explained in the following paragraphs.

The FPGA Input/Output (I/O) banks used for the parallel communication are 3.3 V banks. The fibre-optic interface PCB, on the other hand, operates at 5 V. This leads to the implementation of an interface between these FPGA I/O banks and the fibre-optic interface PCB. The interface has a second, very important, purpose. It serves as isolation between the FPGA and the fibre-optic PCB and so protects the FPGA I/O pins from any over voltage or current

<sup>3</sup>The TPI bus-voltage measurement channel however, has a differential input.

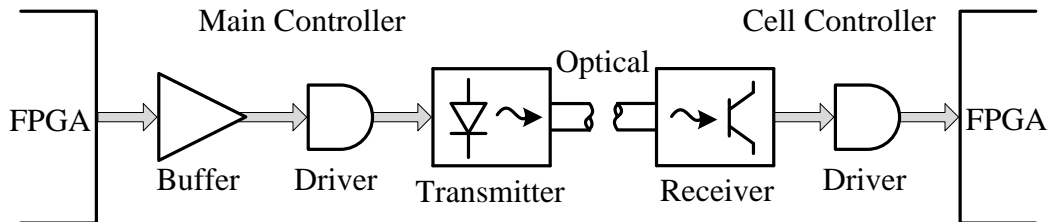




**Figure 3.11:** Controller PCB Hardware Block Diagram: Parallel Communication

spikes which may occur on the fibre-optic PCB. The FPGA outputs are interfaced using three *74ACT11244*[28] octal buffers. These components operate at 5 V with a minimum high-level input voltage of 2 V. This means that a 3.3 V logic high, from the FPGA, will be transformed to a 5 V logic high for the fibre-optic drivers, discussed in Section 3.4.1. The FPGA inputs are interfaced using three *SN74LVC4245A*[29] level shifters. These components have two separate voltage rails, one 5 V and one 3.3 V rail, thus shifting the 5 V logic high, from the fibre-optic receivers, to a 3.3 V logic high for the FPGA inputs. All six ICs are enabled and the level shifter directions are set indefinitely because there is no need to control these parameters.

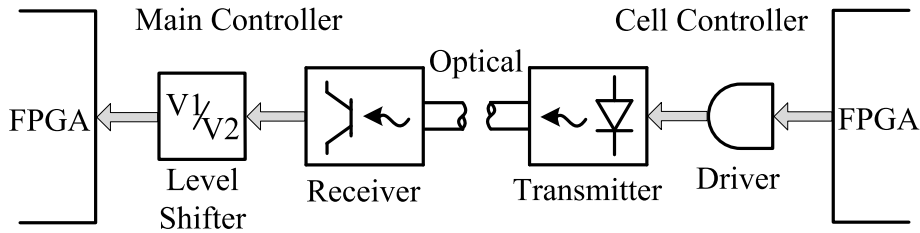
The parallel communication can now be broken down into 17 separate bidirectional channels, 15 for CC's<sup>4</sup>. The signal in the forward direction starts at the MC FPGA and continues to an octal buffer, a fibre-optic driver, a fibre-optic transmitter, through an optic fibre and to the CC. On the CC, the signal continues through a fibre-optic receiver, to a peripheral driver and to the CC FPGA. This half of the bidirectional channel is depicted in Figure 3.12.



**Figure 3.12:** Bidirectional Communication Channel: Forward Signal

<sup>4</sup>For information on the remaining two channels, refer to Section 3.4

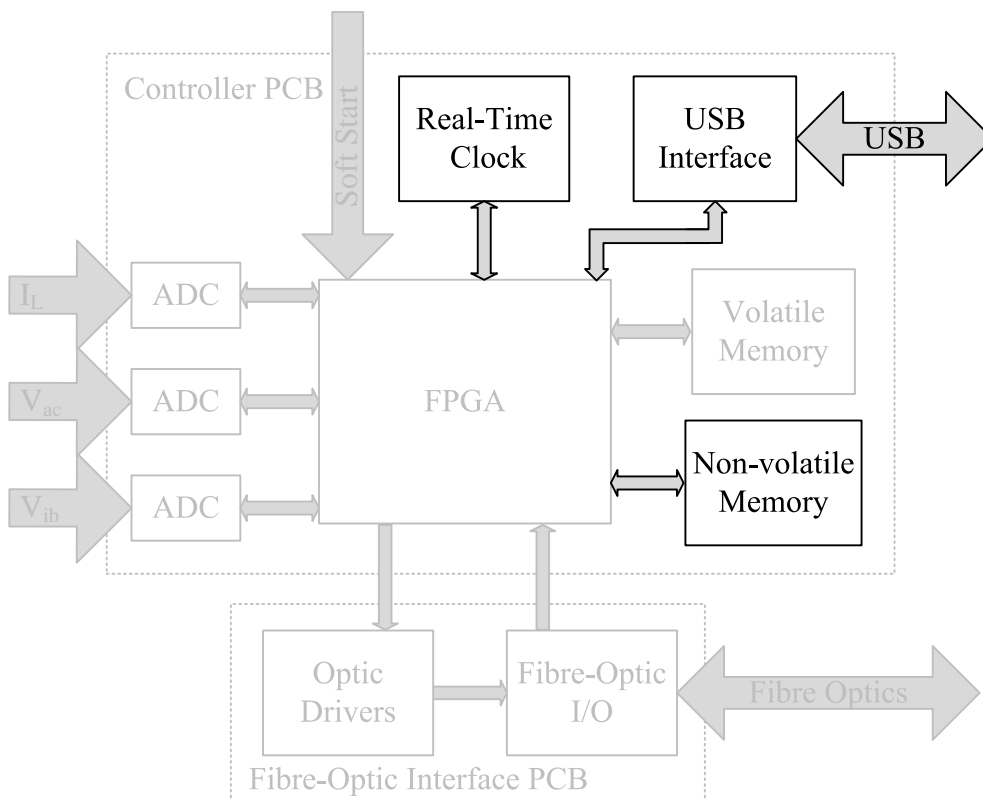
The signal in the reverse direction starts at the CC FPGA and continues to a fibre-optic driver, a fibre-optic transmitter, through an optic fibre and to the MC. On the MC, the signal continues through a fibre-optic receiver, a level shifter and to the MC FPGA. This half of the bidirectional channel is depicted in Figure 3.13.



**Figure 3.13:** Bidirectional Communication Channel: Reverse Signal

### 3.3.4 Peripheral Circuitry

The peripheral circuits are classified as the circuits adding extra functionality to the SST above and beyond the three-phase high-voltage transformation to three-phase line-voltage. This functionality includes the communication to any Universal Serial Bus (USB) interfaced device, data storage as well as data time-stamping, as shown in Figure 3.14. These circuits are further discussed in the following paragraphs.



**Figure 3.14:** Controller PCB Hardware Block Diagram: Peripheral Circuitry

Data is stored using non-volatile memory to preserve saved data even during a main-supply interruption. This is important because the most important data is the data leading up to a primary trip which may trip the main-supply. This data will be carefully examined to help determine the reason for the primary trip. The 16 Mega Bit (Mb) *M25P16*[30] serial flash memory IC is thus used for this function. It communicates with the FPGA through a Serial Peripheral Interface (SPI) interface with a 50 MHz maximum clock rate.

A measurement would be of little interest without its corresponding time. It is thus very beneficial to have the real time available on the MC. It can be used to monitor operational parameters at specific times or for specific periods of time for analytical and statistical use. An example would be to monitor the power usage throughout the day, or the difference in power usage at different stages of the year. The data captured is thus paired with time-stamps using the extremely accurate *DS3232*[31] Real-Time Clock (RTC)<sup>5</sup>. It is clocked with an integrated temperature-compensated crystal oscillator which enhances its long-term accuracy. The device is also equipped with supply-monitoring circuitry, incorporating a backup-battery input to maintain accuracy even with main-supply interruptions. This RTC maintains real time from the decade to the second, compensating for months with less than 31 days as well as leap years. It communicates with the FPGA through an Inter-Integrated Circuit (I<sup>2</sup>C) bidirectional interface.

Saving time-stamped data is only part of the process. The data should be made available for analysis. This is done with a USB interface which adds the functionality to download data via a USB cable to a laptop or even incorporate a bluetooth or Global System for Mobile Communication (GSM) device for this purpose. This interface can be used for live measurement download during development stages and communication between the SST and the utility during field operation. The USB interface is established with an *FT232R*[32] Universal Asynchronous Receiver/Transmitter (UART) to USB interface IC. It supports a transfer rate of 300 baud to 1 Mega Baud (MBd) and has a fully integrated clock. It also has a unique ID burnt into the device during the manufacturing process which can be used for security purposes.

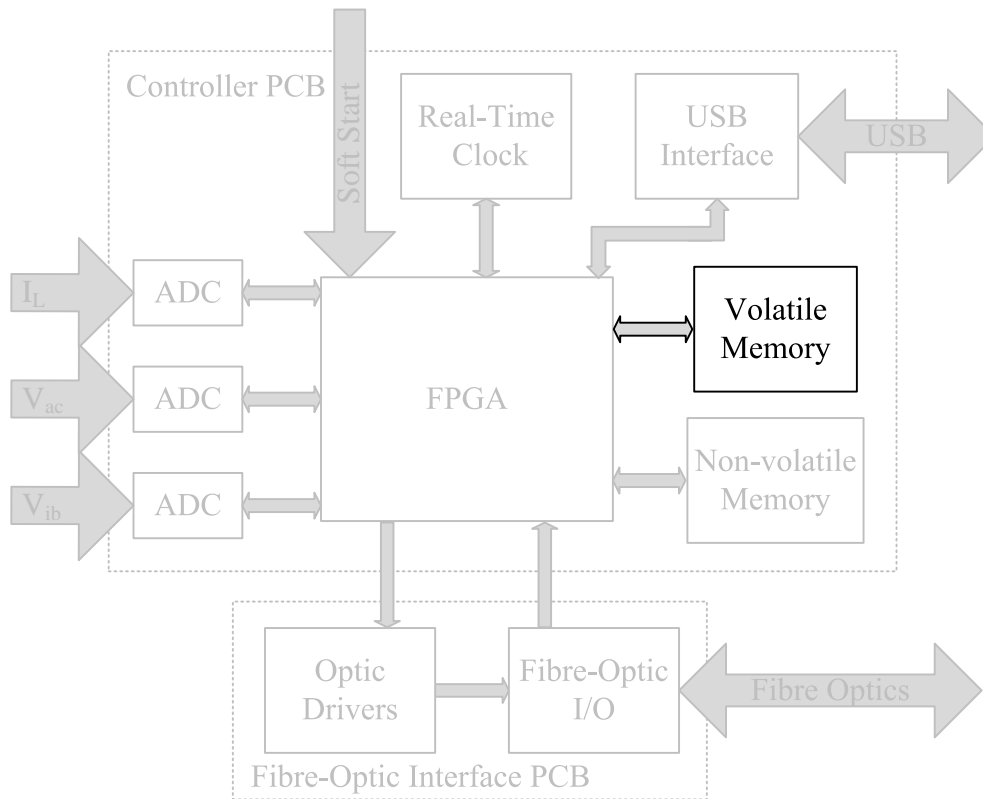
### 3.3.5 DDR Memory

A NIOS II embedded processor, as mentioned in Section 3.3.1, is utilised for various functions. The source code written to execute these functions needs Random Access Memory (RAM) to operate. The FPGA memory blocks can be configured as RAM, however the number of memory blocks required by the control systems as well as the amount of RAM required by the NIOS is not certain at the hardware design phase. External RAM is thus incorporated to achieve a higher level of design freedom during the software design phase, as depicted in Figure 3.15. This phase includes the control implementation as well as the NIOS design. An overlooked FPGA hardware specification causes incompatibility between the FPGA and the RAM unit using the current controller PCB. This means that the RAM is not used. Nonetheless, all control systems and peripheral devices are supported in terms of required memory, but with less design freedom. The original RAM design details are discussed in the following paragraphs.

Two aspects are taken into consideration when choosing a RAM unit. Firstly the availability of the unit and secondly its compatibility with the FPGA. Software compatibility is not as stringent as hardware compatibility. The RAM interface can be written from scratch, however software-development time is greatly reduced when an ALTERA Megafunction<sup>6</sup> can be used for this purpose. The hardware limitations include, but are not limited to, the number of available

<sup>5</sup>[31] claims accuracy to within  $\pm 2$  minutes per year.

<sup>6</sup>Pre-built intellectual property ready to incorporate straight into VHDL code or to use together with a NIOS embedded processor.



**Figure 3.15:** Controller PCB Hardware Block Diagram: DDR

FPGA I/O pins, clock rate support and the number of DQ, DQS and DM pins. These pins are an important consideration because the FPGA has dedicated DQ, DQS and DM pins used by the megafunction for DDR2/DDR interfaces.

The 32 Mega Byte (MB) *MT46V32M8*[33] Double Data Rate (DDR) Synchronous Dynamic Random Access Memory (SDRAM) unit from Micron is thus chosen. It has a 133 MHz clock rate, 8 DQ pins, one DQS pin and one DM pin. These specifications are compatible with the FPGA column I/O banks<sup>7</sup> and the RAM unit is also compatible with the megafunction for the DDR2/DDR interface. One hardware specification was however overlooked in the hardware design phase and surfaced during the software design phase with a Quartus compilation error. This error states that if voltage-referenced input or bidirectional pads exist in a specific I/O bank, five outputs are supported per 12 consecutive pads in column banks [22], p161. The number of I/O pads used as output pads exceeds this restriction to such an extent that the RAM cannot be used on the designed Controller PCB.

In addition to this hardware specification, there are several other design specifications regarding the implementation of DDR memory. Signal integrity is of concern due to the high clock frequency of the DDR memory. At such high frequencies, PCB traces become Radio Frequency (RF) transmission lines and cannot be treated as simple connection-wires. Signal integrity is threatened by transmission line effects and interaction between circuits [34]. Transmission line effects, such as ringing and reflection, are addressed by single-ended and differential line-termination, as discussed in Appendix A.8.1 and A.8.2 respectively. Interaction between circuits, such as cross talk and noise, are addressed by careful PCB layout, as discussed in Appendix A.8.3.

<sup>7</sup>Column I/O banks include FPGA pins 1-60 and 181-240.

### 3.4 Fibre-Optic Interface PCB

The control strategies require bidirectional communication between the MC and the respective CCs. Error handling and peripheral functionality, on the other hand, require bidirectional communication between the three MC's as well as the Three-Phase Inverter (TPI) controller. The communication channels are implemented with optic fibres to provide isolation between the different controllers as well as immunity to EMI. The communication channel layout is depicted in Figure 3.16.

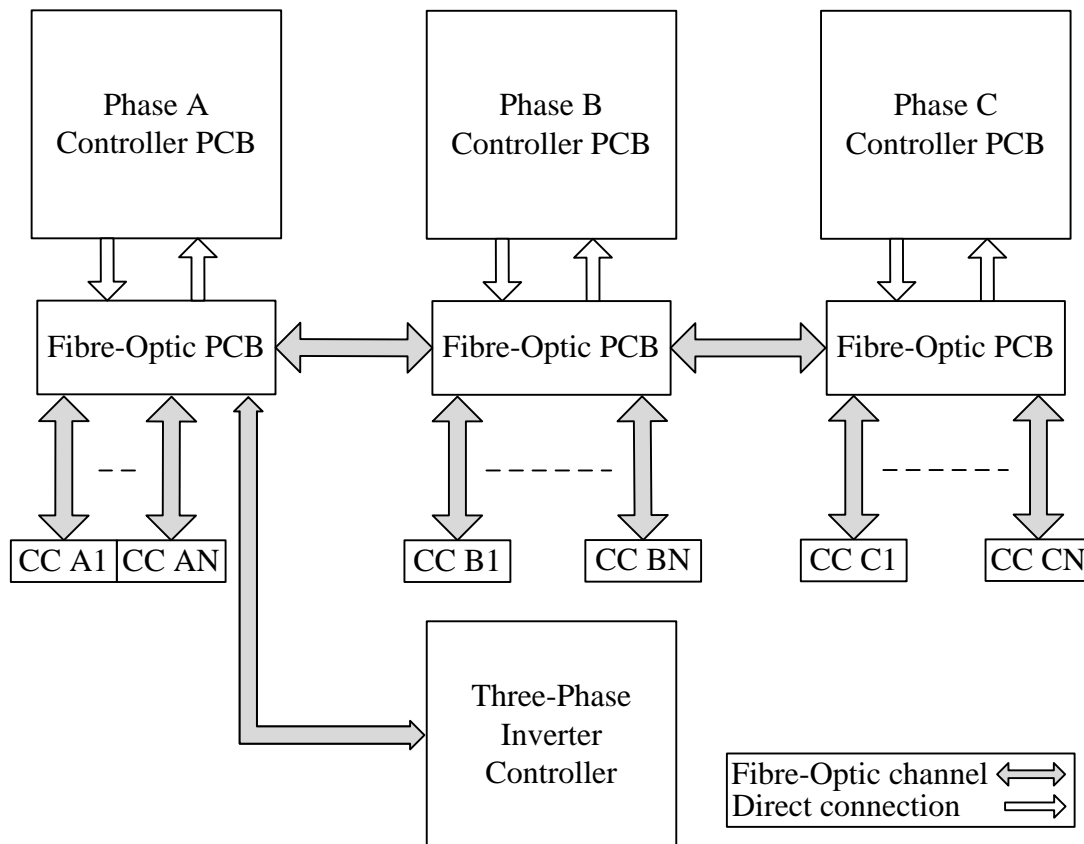


Figure 3.16: Communication Channel Layout

It is clear that the fibre-optic PCB's of phase *A* and *B* require the most channels. As listed in Section 1.4, the maximum number of cells per phase is 15. Therefore the maximum channels required for a fibre-optic PCB is 17. To maintain the modular nature of the SST as well as minimizing the PCB manufacturing cost, the three fibre-optic PCB's are designed identically. This means that the fibre-optic PCB of phase *C* has one extra communication channel.

#### 3.4.1 Bidirectional Fibre-Optic Channel

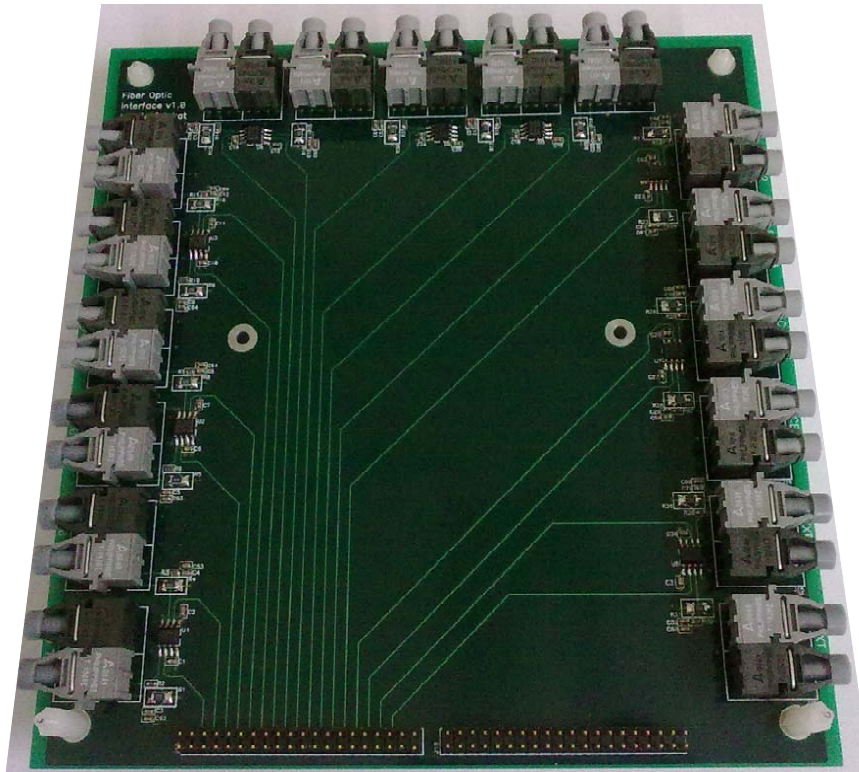
Each channel consists of two optic fibres, one fibre for each communication direction. For each channel, the fibre-optic PCB thus has one fibre-optic transmitter, the *HFBR1528Z*[35], and one fibre-optic receiver, the *HFBR2528Z*[35]. Both the transmitter and receiver have a baud rate of 10 MBd. The necessity for this communication speed will become apparent in Section 4.4.1.

The *SN75451B*[36] driver is used to drive the fibre-optic transmitter. It is chosen due to its sufficiently high-current switching speed. One IC consists of two drivers. Each IC thus drives

two channels except for one, due to the uneven number of channels. The transmitter driving-circuit design details are discussed in Appendix A.9.1. The fibre-optic receiver is extremely easy to implement and the receiver circuit is shown in Appendix A.9.2.

### 3.4.2 Overall PCB Design

The fibre-optic transmitters and receivers combined, need a large PCB circumference. They are placed on a separate PCB from the controller PCB simply to keep the controller PCB relatively small. The fibre-optic interface PCB is shown in Figure 3.17.



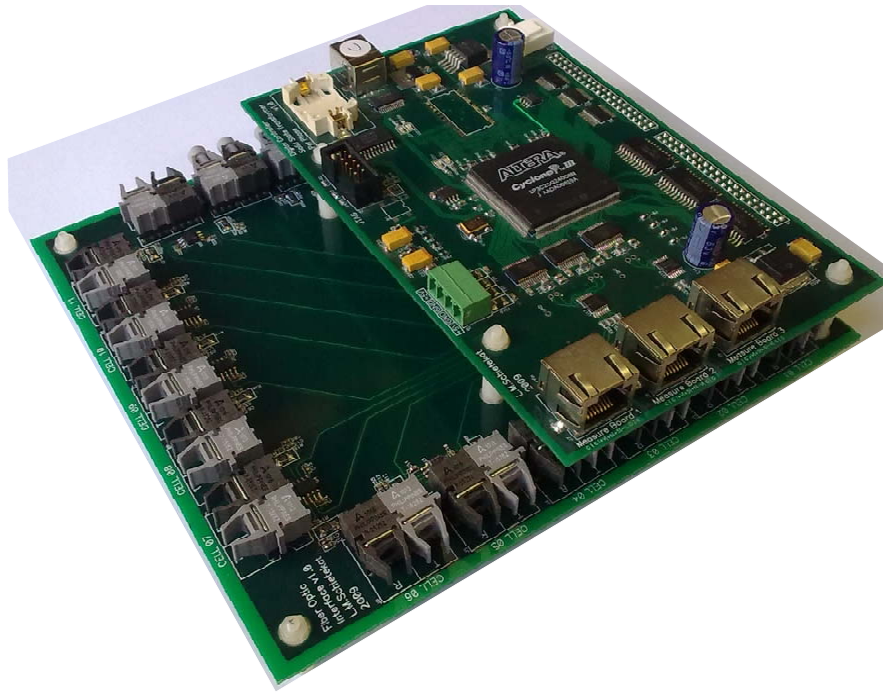
**Figure 3.17:** Fibre-Optic Interface PCB (Top)

The two options for connecting the two PCBs are: Using ribbon cabling or using male and female headers. Two male and female headers are chosen to keep the EMI and cross-talk<sup>8</sup> to a minimum by plugging the two PCB's on top of each other. Each header has 40 pins and carries 17 signals. One male-female group carries the output signals to be transmitted and the other, carries the input signals received. The remaining pins of the two header groups are used as  $V_{CC}$  and ground connections between the PCBs. Figure 3.18 depicts the two PCB plugged in.

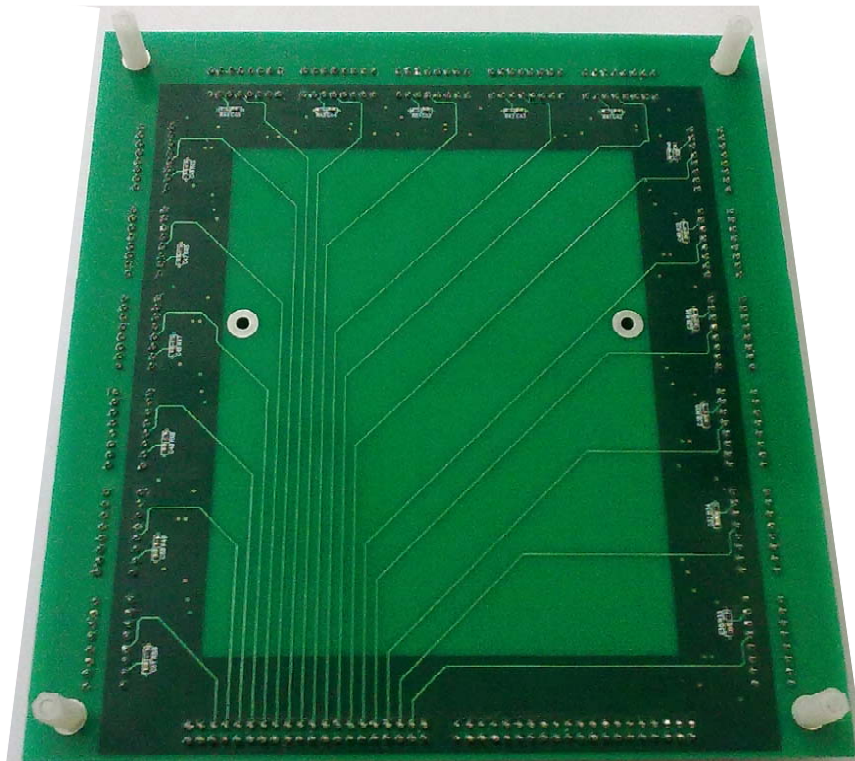
The fibre-optic PCB has four copper layers. The top layer is dedicated to the transmitting circuitry and the bottom layer is dedicated to the receiving circuitry. Between these layers is a ground plane layer and a thick  $V_{CC}$  strip layer, as can be seen in Figure 3.19.

<sup>8</sup>The disturbance caused by the electric or magnetic fields of one signal affecting an adjacent signal.





**Figure 3.18:** Controller PCB and Fibre-Optic Interface PCB



**Figure 3.19:** Fibre-Optic Interface PCB (Bottom)

## 3.5 Conclusion

The input inductor current, input voltage and TPI bus-voltage measurement channel designs were discussed. Each channel in its entirety was covered, with emphasis on preventing noise interference. The FPGA and incorporated NIOS II embedded processor advantages were revealed. The MC peripheral functions together with their facilitating circuitry were discussed. The DDR hardware incompatibility was explained. This drawback is not critical as it merely reduces the software development freedom to a still acceptable level. The complex DDR hardware design was emphasised nonetheless. Finally the fibre-optic PCB design, as the communication interface between MCs and between MCs and CCs, was discussed.

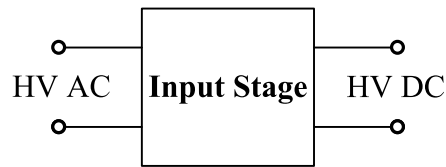


# Chapter 4

## Active-Rectifier Control

### 4.1 Introduction

The input stage is situated in the high-voltage side of the SST, and converts the HV AC-input to HV DC, as shown in Figure 4.1. This conversion is accomplished with an Active Rectifier (AR) to facilitate unity power factor by drawing a sinusoidal input-current, as well as regulating the HV DC output.



**Figure 4.1:** Three Stage SST Concept: Input Stage

A multilevel-converter topology is used to manage the three-phase HV input. The input line to neutral voltage is split between  $N$  cascaded ARs, as depicted in Figure 4.2, which reduces the required blocking-voltage of each switch. The isolation stage, adjacent to the input stage, forms part of the cascaded topology. The HV DC-output of the input stage is thus also split into  $N$  buses for each phase.

Due to the modularity of the cascaded converter topology, the input-stage control can be designed for a single AR and subsequently expanded for  $N$  ARs in each phase. The proposed AR controller incorporates a double loop control scheme. The outer voltage loop controls the cell bus-voltage, at a predefined average-level, by manipulating the current-loop reference. It regulates the sinusoid amplitude, synchronised with the input voltage,  $V_{ac}$ . This amplitude-modified sinusoid serves as the current-loop reference. The current loop thus controls the input-inductor current to be sinusoidal and in phase with  $V_{ac}$ , to facilitate unity power factor. Figure 4.3, from the left, depicts that the cell bus-voltage feedback,  $v_{cb}$ , is compared with the constant voltage reference,  $V_{cbref}$ , to determine the voltage error,  $e_V$ . The error is converted by the voltage compensator,  $C_V$ , to determine the compensator output-signal,  $u_V$ , representing a current-command. This signal is multiplied with the unit-sinusoid to create the current reference,  $i_{Lref}$ , which is compared with the inductor current feedback,  $I_L$ , to determine the current error,  $e_I$ . The error is converted by the current compensator,  $C_I$ , to determine the compensator output-signal,  $u_I$ , representing an AR duty-cycle command. This signal is fed to the Pulse Width Modulator (PWM) to determine the AR duty-cycle,  $d$ . This duty-cycle is fed to the plant,  $G_I$ , which returns  $i_L$  as feedback and as input to the plant,  $G_V$ , which returns  $v_{cb}$  as feedback.

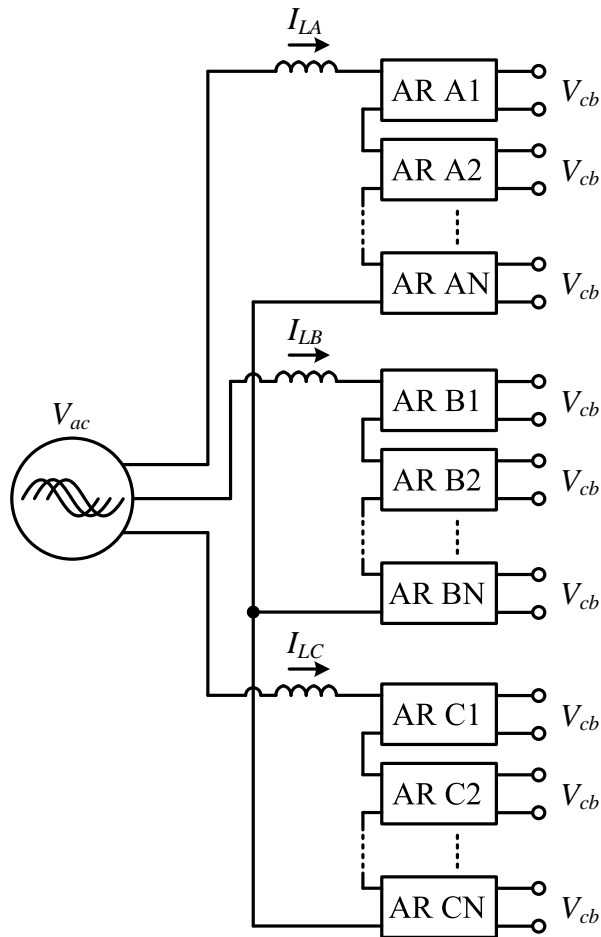


Figure 4.2: Three-Phase Cascaded Active-Rectifier Topology

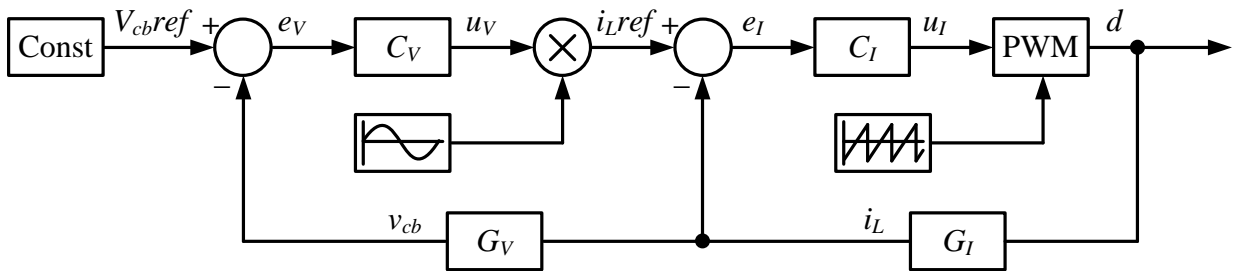


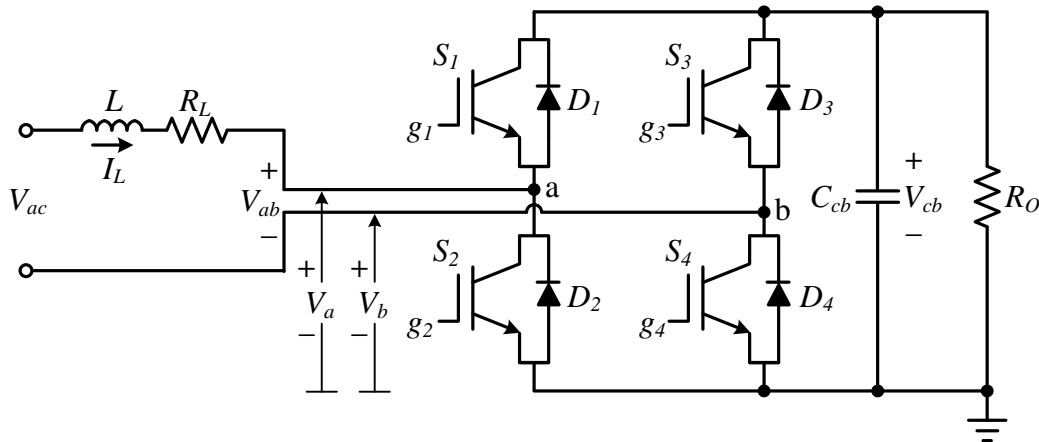
Figure 4.3: Double-Loop Active-Rectifier Control Scheme

In this chapter the methodology followed in designing the AR control system for a single AR is thoroughly described. Time-domain simulation results and tests measurements are presented and explained. The control implementation is discussed with emphasis on distinctive features.

## 4.2 Control Design

The first step in control design is to characterise the system, including the controlled- as well as the control system. The controlled system characterisation involves defining models for physical components playing key roles within the system. The control system characterisation involves defining the capabilities of the hardware available for control implementation.

With regard to characterising the controlled system: A single AR consists of an input inductor<sup>1</sup>,  $L$ , the inductor resistance,  $R_L$ , a full-bridge converter and a bus-capacitor,  $C_{cb}$ , as shown in Figure 4.4. The resistive load,  $R_O$ , is added to the circuit to imitate power transfer from the input-stage to the isolation-stage. The full-bridge converter consists of four switches,  $S_1 - S_4$ , each realised with an Insulated Gate Bipolar Transistor (IGBT) and controlled through its respective gate-signal,  $g_1 - g_4$ .



**Figure 4.4:** Active-Rectifier Circuit Diagram

With regard to characterising the control system: As discussed in Chapter 3, the MC includes ADCs capable of sampling at 53MHz, an FPGA capable of calculations at a matched, or higher, clock rate and 10 Mbd communication between the MC and the CCs. The CCs assist with the AR control and thus include the same ADCs and FPGA as the MC. Most FPGA control-components are clocked at 10 MHz to incorporate design freedom during the control design and testing phase. In terms of FPGA clock speeds, this is relatively slow, however, this control-bandwidth still results in very small time delays compared to the norm of digital controllers in power electronics.

In the remainder of this section the AR control design in terms of the two control loops, as shown in Figure 4.3 is described, starting with the inner current-loop, and followed by the outer voltage-loop. Each loop design entails, among other steps, linearising the respective plant,  $G_I$  and  $G_V$ , and designing the respective compensator,  $C_I$  and  $C_V$ .

### 4.2.1 Pulse Width Modulator Design

PWM is how the switch duty ratio,  $d$ , is generated by comparing the compensator output to a carrier signal. This output is also referred to as the carrier-reference. The AR full-bridge switch topology can utilize one of two switching schemes namely, bipolar-voltage switching or unipolar-voltage switching. As depicted in Figure 4.5, with bipolar-voltage switching the switch pairs,  $(S_1; S_4)$  and  $(S_2; S_3)$ , are treated as alternate switch pairs [37]. Switch pair  $(S_2; S_3)$  is turned on when the reference is greater than the carrier, and turned off otherwise. Switch pair  $(S_1; S_4)$  is turned on when the carrier is greater than the reference, and turned off otherwise. This results in two possible  $V_{ab}$  voltage levels,  $-V_{cb}$  or  $V_{cb}$ .

As depicted in Figure 4.6, with unipolar-voltage switching, also known as double-PWM, the switch pairs,  $(S_1; S_2)$  and  $(S_3; S_4)$ , are controlled independently [37]. However, each switch pair

<sup>1</sup>The cascaded topology can include a single input inductor per phase, or an input-inductor per AR.

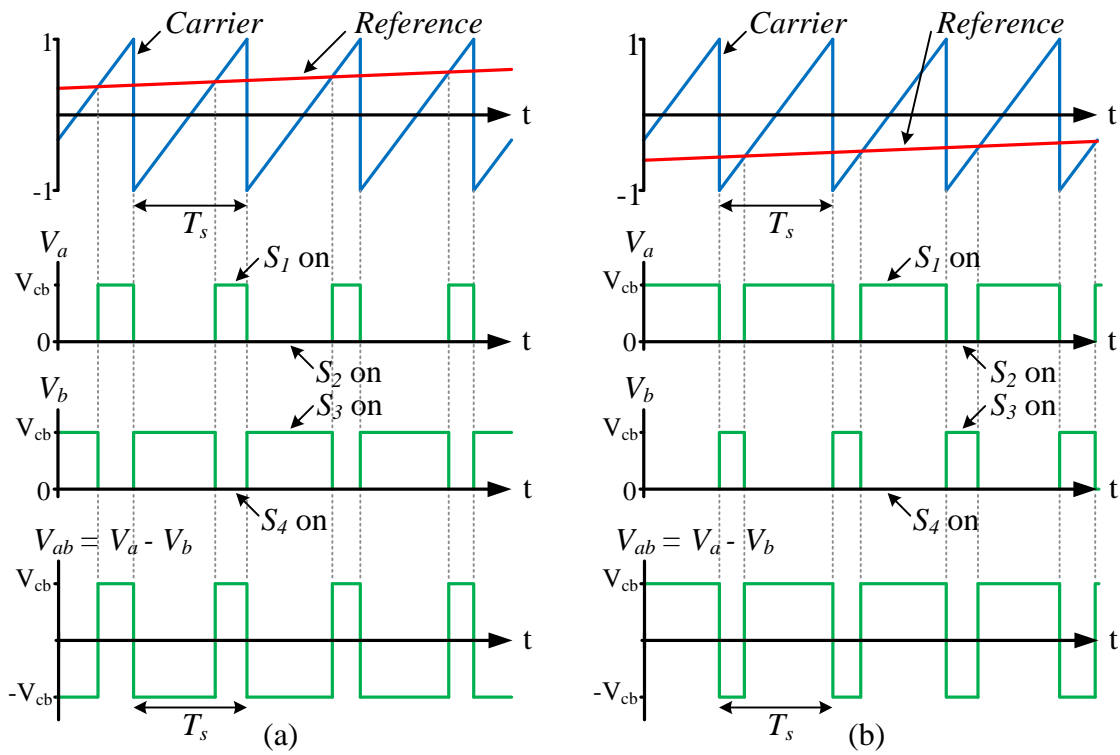


Figure 4.5: Bipolar PWM: (a) Positive Reference; (b) Negative Reference

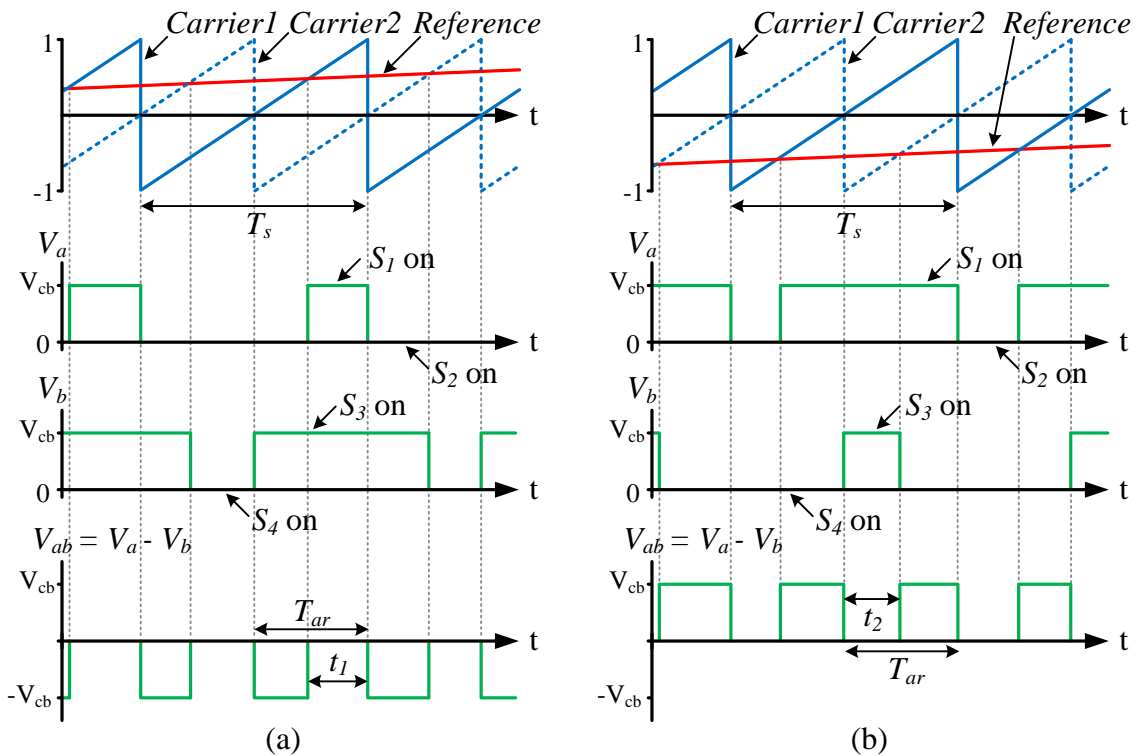


Figure 4.6: Unipolar PWM: (a) Positive Reference; (b) Negative Reference

is switched as an alternate pair. This is achieved by comparing the reference signal with two carriers. Carrier2 is phase shifted by  $180^\circ$ , compared to carrier1. The reference compared with carrier1, determines the switching state of switch pair ( $S_1; S_2$ ). When the reference is greater than carrier1,  $S_2$  is turned on an  $S_1$  is turned off and vice-versa, when carrier1 is greater than the reference. The reference compared with carrier2 determines the switching state of switch pair ( $S_3; S_4$ ). When the reference is greater than carrier2,  $S_3$  is turned on an  $S_4$  is turned off and vice-versa, when carrier2 is greater than the reference. This results in three possible  $V_{ab}$  voltage levels,  $-V_{cb}$ ,  $0 V$  or  $V_{cb}$ .

The PWM design choices are thus confined to which switching scheme to use, which carrier waveform to use, and the implemented switching frequency,  $f_s$ , where:

$$f_s = \frac{1}{T_s} \quad (4.2.1)$$

Unipolar-voltage switching is chosen because it effectively doubles the AR switching frequency. It also reduces the voltage drop across the inductor,  $L$ , with respect to that of bipolar-voltage switching [4]. The switching frequency is chosen as  $10 \text{ kHz}^2$ , which leads to an effective AR switching frequency of:

$$f_{ar} = 2 \times f_s = 20 \text{ kHz} \quad (4.2.2)$$

and effective switching period:

$$T_{ar} = \frac{1}{f_{ar}} = 50 \mu\text{s} \quad (4.2.3)$$

The choices of carrier waveforms are sawtooth or triangle, thus implementing asymmetric or symmetric PWM respectively. Asymmetric PWM yields more current harmonics however, this is acceptable, given the high effective AR switching frequency. Additional benefits in implementing asymmetric PWM include, simplified system analysis, less vulnerability to reference ripple as well as simplified reference ripple compensation[38]. These advantages lead to the choice of sawtooth carriers and thus asymmetric PWM.

The switching duty ratio is defined as:

$$d = \frac{t_1}{T_{ar}} \quad \text{for: Reference} > 0 \quad (4.2.4)$$

$$d = \frac{t_2}{T_{ar}} \quad \text{for: Reference} < 0 \quad (4.2.5)$$

with  $t_1$  and  $t_2$  defined in Figure 4.6.

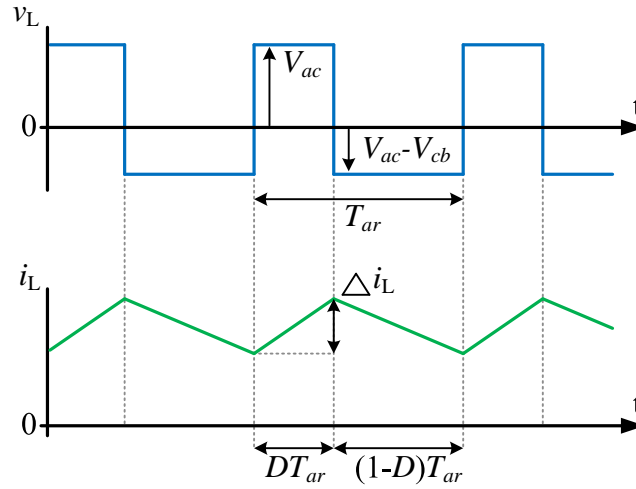
## 4.2.2 Input-Inductor Design

To determine the appropriate input-inductor value, the inductor voltage-drop as well as the inductor-current waveforms are analysed. Figure 4.7 depicts these waveforms for the first two AR states. These AR states, together with the analysis assumptions are discussed in Appendix B.1.1. It is also assumed that the  $50 \text{ Hz } V_{ac}$  is constant compared to the  $i_L$  rate of change.

From this Figure, the inductor-current gradient during  $DT_{ar}$  is given as:

$$i_L \text{gradient} = \frac{V_{ac}}{L} \quad (4.2.6)$$

<sup>2</sup>This frequency value is subject to change due to findings during the SST testing phase.



**Figure 4.7:** Input-Inductor Voltage and Current Waveforms

and so the inductor-current ripple:

$$\Delta i_L = \frac{V_{ac}}{L} \cdot DT_{ar} \quad (4.2.7)$$

Defining the inductor-current ripple as the peak inductor-current value multiplied with the maximum permitted ripple-percentage yields<sup>3</sup>:

$$L = \frac{V_{ac}}{i_{Lp} \times rip\%} \cdot DT_{ar} \quad (4.2.8)$$

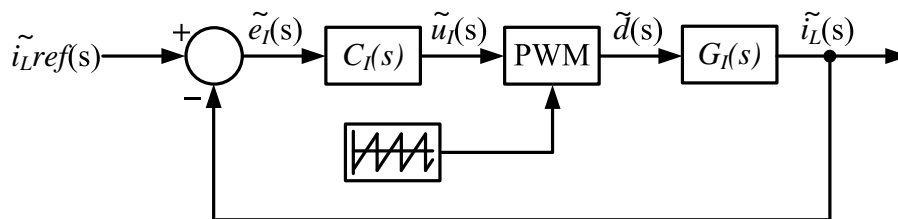
Using the values for  $V_{ac}$ ,  $i_{Lp}$  and  $D$  as defined in Appendix B.1.5 and  $T_{ar}$  as defined in Eq. 4.2.3 results in:

$$L = 4 \text{ mH with maximum: } rip\% = 10\% \quad (4.2.9)$$

This inductor value is subject to change during the design and testing phase as the maximum ripple-percentage is not a fixed requirement.

### 4.2.3 Current-Loop Plant Linearisation

The current loop can be analysed separately from the voltage loop, as shown in Figure 4.8, with the small AC signals denoted by " $\sim$ ". A state-space averaging technique is used to obtain the AC small-signal linear model of the plant:



**Figure 4.8:** Active-Rectifier Inner Current-Loop

<sup>3</sup>Applying the analysis assumptions, the maximum inductor-current ripple occurs at the peak inductor current with unipolar-voltage switching

$$G_I(s) = \frac{\tilde{i}_L(s)}{\tilde{d}(s)} \quad (4.2.10)$$

where  $\tilde{i}_L(s)$  and  $\tilde{d}(s)$  are the small perturbations of the input-inductor current,  $i_L$ , and AR duty ratio,  $d$ . This model includes the power stage and output filter and is linearised around a steady-state DC operating point [37][39].

Step 1 is to determine the state variable model, describing each circuit state. These states as well as the assumptions made for this analysis, are discussed in Appendix B.1.1 where the following results are given:

State equations for state 1 and 2, with  $(\mathbf{A}_1, \mathbf{A}_2)$  state matrices and  $(\mathbf{B}_1, \mathbf{B}_2)$  column vectors:

$$\dot{\mathbf{x}} = \mathbf{A}_1 \mathbf{x} + \mathbf{B}_1 v_{ac} \quad \text{during } d \cdot T_{ar} \quad (4.2.11)$$

and

$$\dot{\mathbf{x}} = \mathbf{A}_2 \mathbf{x} + \mathbf{B}_2 v_{ac} \quad \text{during } (1-d) \cdot T_{ar} \quad (4.2.12)$$

Output equations for state 1 and 2, with  $(\mathbf{C}_1, \mathbf{C}_2)$  row vectors:

$$y = \mathbf{C}_1 \mathbf{x} \quad \text{during } d \cdot T_{ar} \quad (4.2.13)$$

and

$$y = \mathbf{C}_2 \mathbf{x} \quad \text{during } (1-d) \cdot T_{ar} \quad (4.2.14)$$

The system state,  $\mathbf{x}$ , and the output,  $y$ , are defined as follow:

$$\mathbf{x} = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} i_L \\ v_{cb} \end{bmatrix} \quad (4.2.15)$$

$$y = [i_L] \quad (4.2.16)$$

Step 2 is to determine an averaged description of the equations, describing the two states in question. The equations are time weighted and averaged over one switching period,  $T_{ar}$ , resulting in the state equation:

$$\dot{\mathbf{x}} = [\mathbf{A}_1 d + \mathbf{A}_2 (1-d)] \mathbf{x} + [\mathbf{B}_1 d + \mathbf{B}_2 (1-d)] v_{ac} \quad (4.2.17)$$

and the output equation:

$$y = [\mathbf{C}_1 d + \mathbf{C}_2 (1-d)] \mathbf{x} \quad (4.2.18)$$

Step 3 is to separate small-signal perturbation and steady-state components. Steady-state components are denoted with capital letters and perturbations with " $\tilde{\cdot}$ ":

$$\mathbf{x} = \mathbf{X} + \tilde{\mathbf{x}} \quad (4.2.19)$$

$$y = Y + \tilde{y} \quad (4.2.20)$$

$$d = D + \tilde{d} \quad (4.2.21)$$

$$v_{ac} = V_{ac} + \tilde{v}_{ac} \quad (4.2.22)$$

The following perturbation equations are given in Appendix B.1.2:

$$\dot{\tilde{\mathbf{x}}} = \mathbf{A}\tilde{\mathbf{x}} + [(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)V_{ac}]\tilde{d} \quad (4.2.23)$$

$$\tilde{y} = \mathbf{C}\tilde{\mathbf{x}} + [(\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X}]\tilde{d} \quad (4.2.24)$$

where

$$\mathbf{A} = \mathbf{A}_1D + \mathbf{A}_2(1 - D) \quad (4.2.25)$$

and

$$\mathbf{C} = \mathbf{C}_1D + \mathbf{C}_2(1 - D) \quad (4.2.26)$$

Step 4 is to transform the perturbation equations into the  $s$ -Domain, to obtain the transfer function denoted in Eq. 4.2.10. Appendix B.1.3 results in:

$$G_I(s) = \frac{\tilde{y}(s)}{\tilde{d}(s)} = \frac{\tilde{i}_L(s)}{\tilde{d}(s)} = \mathbf{C}[s\mathbf{I} - \mathbf{A}]^{-1}[(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X}] \quad (4.2.27)$$

Step 5 is to simplify this transfer function into symbolic form including the component symbols as depicted in Figure 4.4. This is a comprehensive model-form in terms of understanding the system behaviour, especially during the system testing stage, where system parameters may vary from the defined steady-state DC operating point. Appendix B.1.4 results in:

$$G_I(s) = \frac{V_{cb}}{L} \times \frac{s + \frac{2}{ROCb}}{s^2 + \left(\frac{R_L}{L} + \frac{1}{ROCb}\right)s + \frac{R_L}{ROLCb} + \frac{(1-D)^2}{LCb}} \quad (4.2.28)$$

The current-loop plant thus consists of a zero and a complex pole-pair. The plant gain is proportional to  $V_{cb}$  and inversely proportional to  $L$ . This is a significant characteristic in that a change in plant gain directly alters the current-loop bandwidth.

Step 6 is to define the steady-state DC operating point and use it, together with system parameters, to quantify this transfer function. Appendix B.1.5 results in:

$$G_I(s) = 8.622 \times 10^4 \times \frac{s + 71.747}{s^2 + 135.9s + 3.508 \times 10^5} \quad (4.2.29)$$

which yields the linear model of the current-loop plant. The frequency response, as shown in Figure 4.9, results in a plant resonant-frequency of:

$$f_{Glr} = 93.5 \text{ Hz} \quad (4.2.30)$$

and a plant crossover-frequency of:

$$f_{GI} = 19.4 \text{ kHz} \quad (4.2.31)$$

The plant model is further analysed in Appendix B.1.6, to establish its sensitivity to change in system parameters. It is found that the only parameters to change the transfer-function frequency response significantly are the input-inductor and cell bus-voltage values. It is thus advisable to re-evaluate the plant model, once a significant variation in these parameters are implemented.



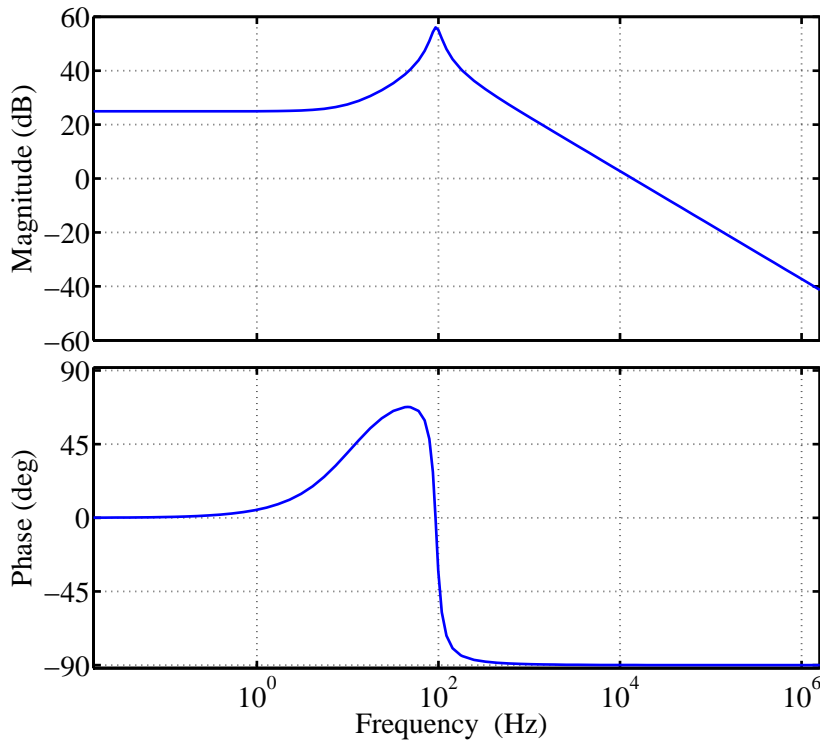


Figure 4.9: Frequency Response of the Current-Loop Plant Model,  $G_I(s)$

#### 4.2.4 Current-Loop Compensator Design

Average current mode control is implemented within the inner current-loop, as discussed in Section 2.1. This loop requires a large bandwidth to achieve optimum reference tracking, as large as possible without causing loop instability. The current-loop compensator design thus starts off with the analog control criterion: The amplified inductor-current downslope should not exceed the carrier slope with which it is compared, as shown in Figure 4.10. This criterion is a result of analog power-electronic controllers causing sub-harmonic oscillation problems when the carrier and carrier-reference slopes are unsuitably matched.

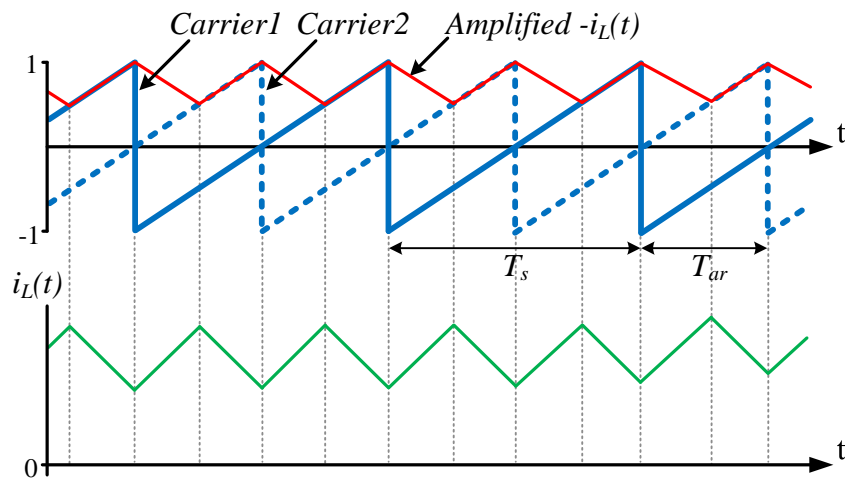
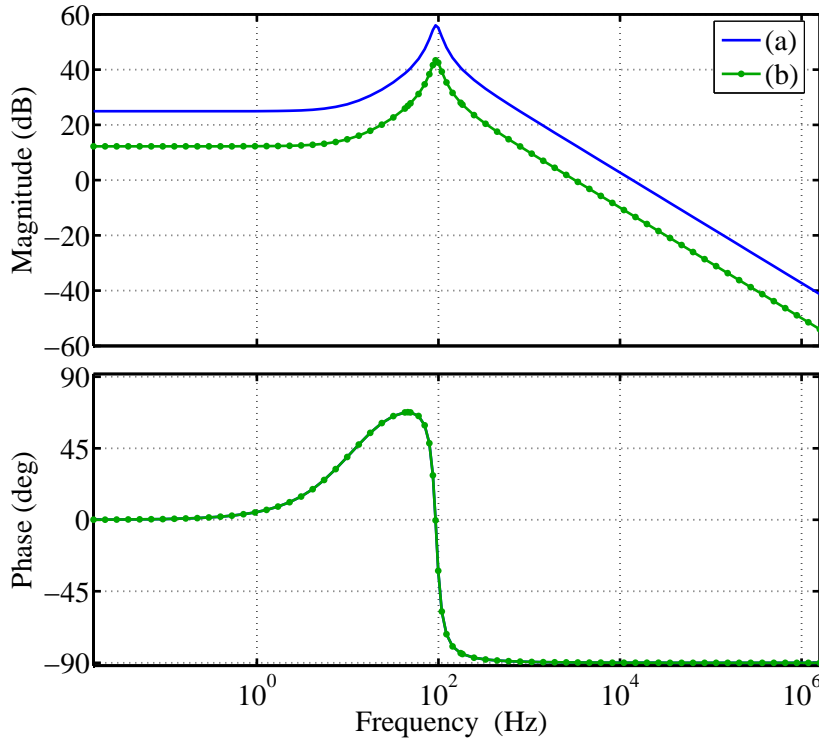


Figure 4.10: Optimal Gain Active-Rectifier Waveforms

This criterion is used as a compensator-design starting point even though digital controllers can prevent these oscillation problems. The current-loop compensator,  $C_I(s)$ , thus has an upper gain limit at the switching frequency, which ultimately determines the maximum current-loop crossover frequency [14]. The maximum inductor-current and carrier slopes are analysed in Appendix B.2.1, which results in the optimum compensator gain:

$$G_{CIopt} = \frac{V_s \cdot f_s \cdot L}{V_{cb}} = 0.232 \quad \text{at } f_s \quad (4.2.32)$$

with  $V_s$  being the carrier peak-to-peak amplitude. To determine the maximum crossover frequency, the current-loop plant transfer function of Eq. 4.2.29, is multiplied with this optimum compensator gain. The result is analysed using its bode plot representation, as shown in Figure 4.11:



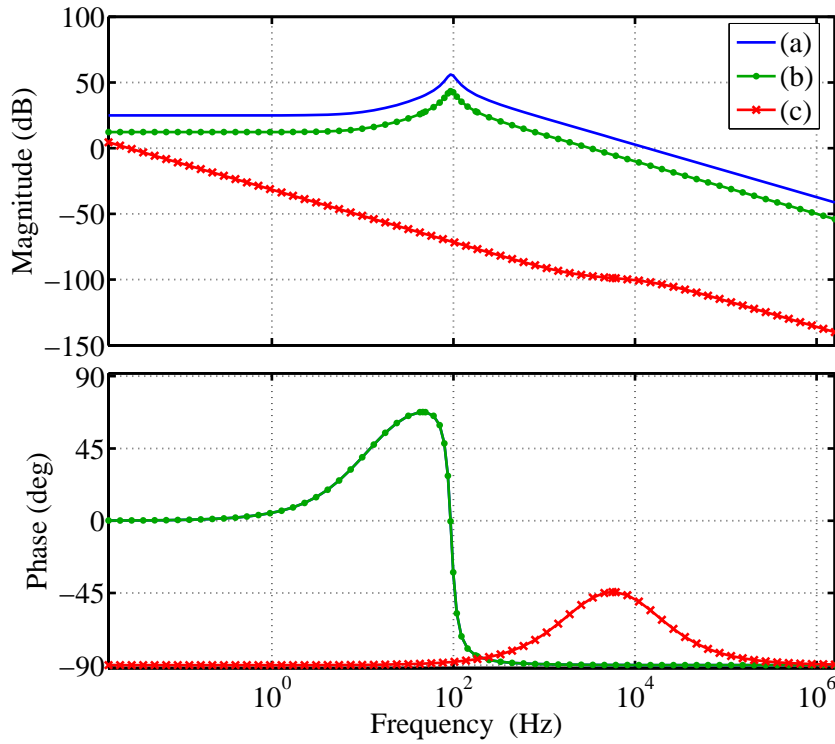
**Figure 4.11:** Frequency Response of: (a)  $G_I(s)$ ; (b)  $G_{CIopt} \cdot G_{CI}$ .

The maximum crossover frequency is thus:

$$f_c = 4497.8 \text{ Hz} \approx 4.5 \text{ kHz} \quad (4.2.33)$$

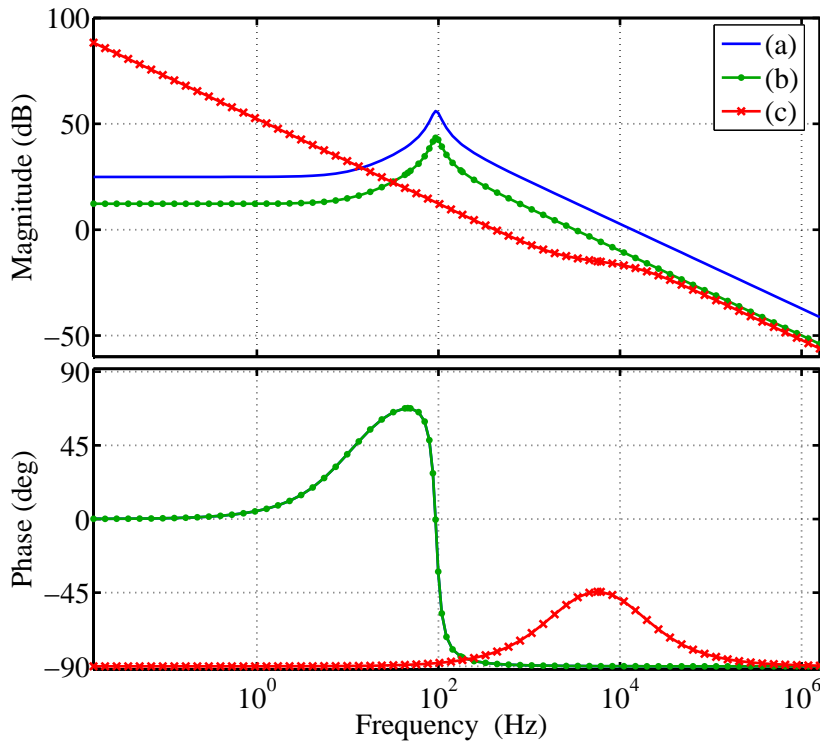
The compensator design continues by placing a pole and a zero together with an integrator. The zero is placed at  $\frac{1}{2} \cdot f_c$  providing a boost at low frequencies and its position is chosen to increase the open-loop phase-margin. The pole is placed at  $3 \cdot f_c$  to suppress noise spikes. As shown in Figure 4.12, this pole, zero and integrator placement result in the preliminary compensator:

$$C_{Ipre}(s) = \frac{s + (\frac{1}{2} \cdot f_c \cdot 2\pi)}{s(s + (3 \cdot f_c \cdot 2\pi))} \approx \frac{s + 14500}{s(s + 87000)} \quad (4.2.34)$$



**Figure 4.12:** Frequency Response of: (a)  $G_I(s)$ ; (b)  $G_{CIopt} \cdot G_I(s)$ ; (c)  $C_{Ipre}(s)$ .

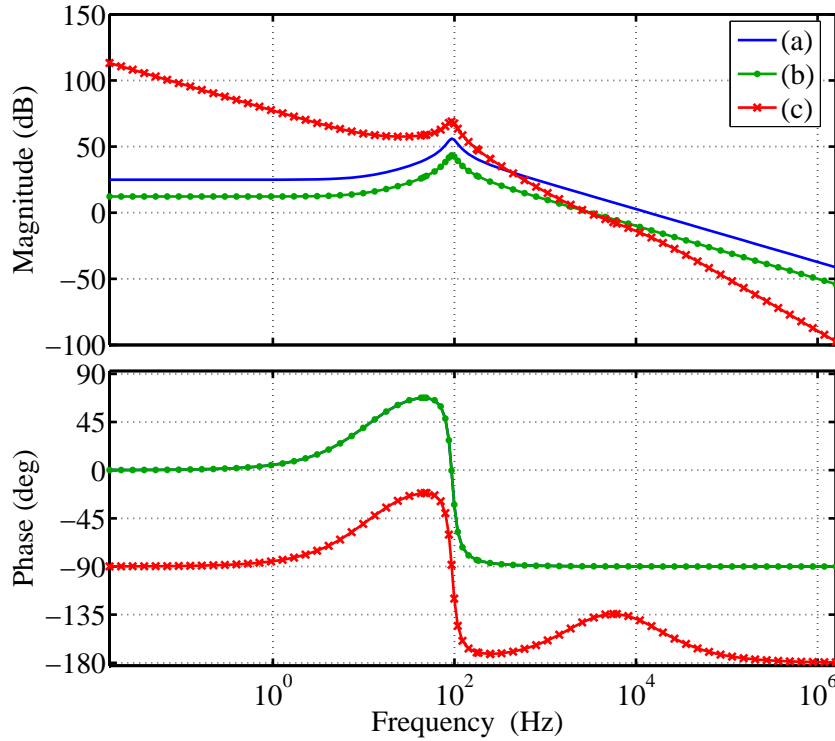
The preliminary-compensator gain is analysed to determine the additional gain required to achieve the desired closed-loop bandwidth. As shown in Figure 4.13, the compensator is thus given as:



**Figure 4.13:** Frequency Response of: (a)  $G_I(s)$ ; (b)  $G_{CIopt} \cdot G_I(s)$ ; (c)  $C_I(s)$ .

$$C_I(s) = 15600 \cdot \frac{s + 14500}{s(s + 87000)} \quad (4.2.35)$$

Figure 4.14 depicts the open-loop frequency response and Figure 4.15 depicts the closed-loop frequency response of the current-loop.



**Figure 4.14:** Frequency Response of: (a)  $G_I(s)$ ; (b)  $G_{Cl_{opt}} \cdot G_I(s)$ ; (c)  $C_I(s) \cdot G_I(s)$ .

The resulting current-loop bandwidth is:

$$BW_I = 4.9 \text{ kHz} \quad (4.2.36)$$

The effect of the ever changing AR duty-cycle variable,  $D$ , on the open current-loop frequency response is discussed in Appendix B.2.2. The closed current-loop response is also analysed in this appendix.

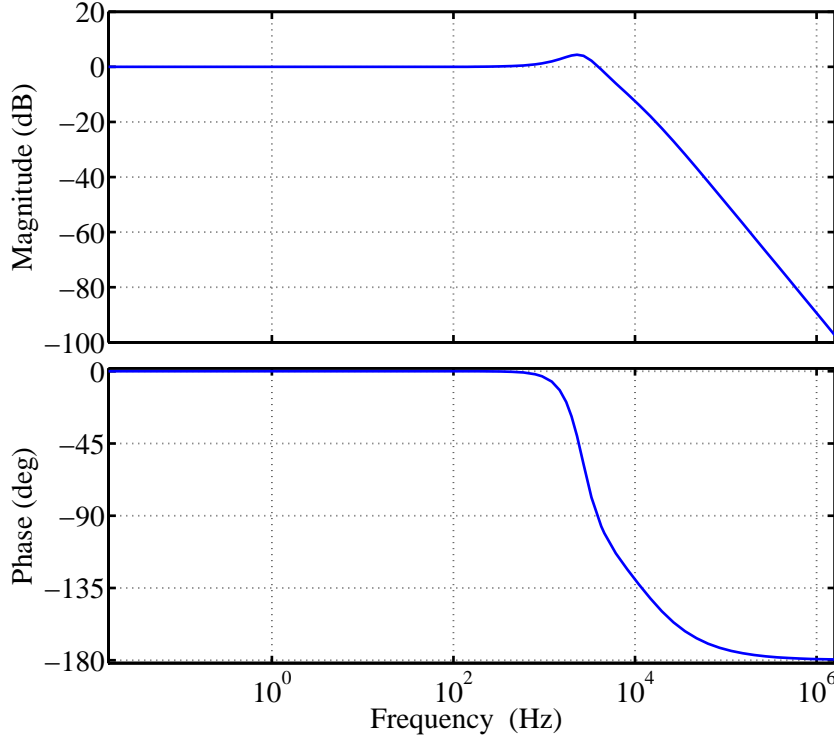


Figure 4.15: Closed Current-Loop Frequency Response

#### 4.2.5 Voltage-Loop Plant Linearisation

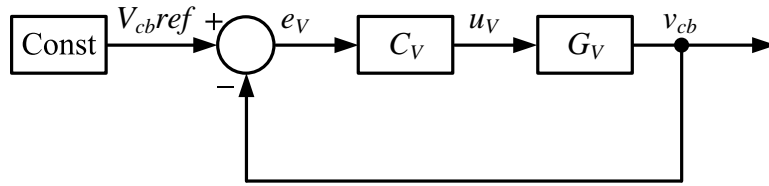
The voltage-loop plant linearisation process involves the use of parameter values averaged over a relatively long period. This method is suitable because of the desired low voltage-loop bandwidth. The voltage loop can be analysed separately from the current loop. Separating the voltage loop from the double-loop control scheme is not as straight forward as doing so with the current loop. The process is split into three steps, the first being to determine a switching-stage transfer function, representing the transition from the peak input-inductor current,  $I_{Lp}$ , to the cell bus input-current,  $I_{cb}$ . The derivation of this transfer function discussed in Appendix B.3.1, yields:

$$G_{SW}(s) = \frac{I_{cb}}{I_{Lp}} = \frac{1-D}{\sqrt{2}} \quad (4.2.37)$$

The second step is to determine the bus-stage transfer function, representing the transition from the cell bus input-current,  $I_{cb}$ , to the cell bus-voltage,  $V_{cb}$ . The derivation of this transfer function discussed in Appendix B.3.2, yields:

$$G_{BUS}(s) = \frac{v_{cb}}{i_{cb}} = \frac{\frac{1}{C_{cb}}}{s + \frac{1}{C_{cb}R_O}} \quad (4.2.38)$$

The final step in separating the voltage loop from the control scheme shown in Figure 4.3, is to treat the control components between the signals,  $u_V$  and  $i_L$ , as a unity gain. These components include the sinusoidal multiplication, the compensator,  $C_I$ , the PWM generation and the plant,  $G_I$ . This substitution is possible when modelling the voltage loop, due to the high current-loop bandwidth, in comparison. The transition from  $u_V$  to  $i_L$  has no impact on the voltage loop. Combining steps one to three yields a voltage loop as depicted in Figure 4.16.



**Figure 4.16:** Active-Rectifier Voltage Loop

The voltage-loop plant transfer function is thus given in symbolic form including the component symbols as depicted in Figure 4.4:

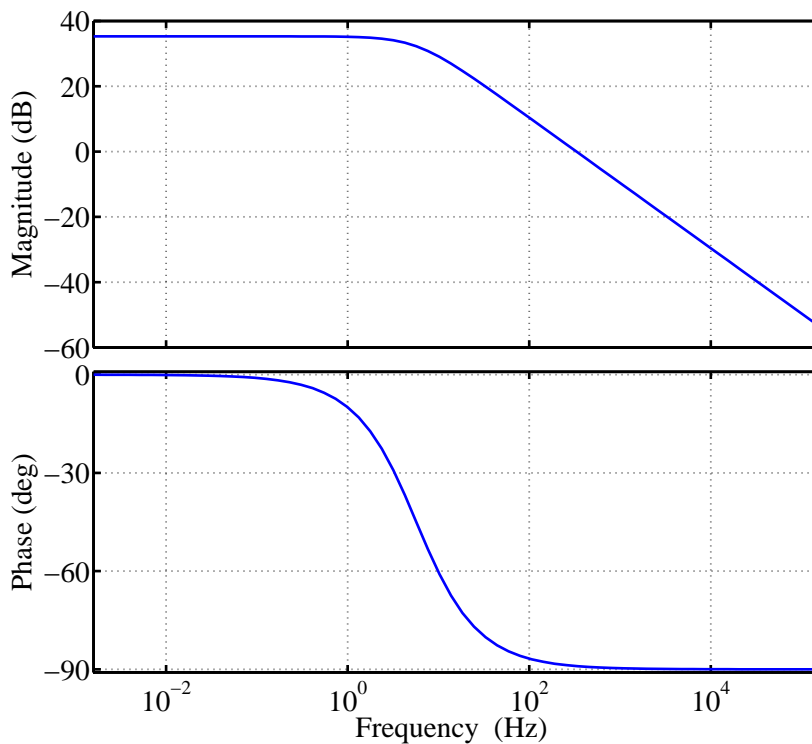
$$G_V(s) = G_{SW}(s) \cdot G_{BUS}(s) = \frac{1-D}{\sqrt{2}} \cdot \frac{\frac{1}{C_{cb}}}{s + \frac{1}{C_{cb}R_O}} \quad (4.2.39)$$

Quantifying this transfer function with Eq. B.1.32 and Table B.4 yields:

$$G_V(s) = \frac{2083}{s + 35.87} \quad (4.2.40)$$

The voltage-loop plant frequency response, as shown in Figure 4.17, results in a plant crossover-frequency of:

$$f_{GV} = 468 \text{ Hz} \quad (4.2.41)$$



**Figure 4.17:** Frequency Response of the Voltage-Loop Plant Model,  $G_V(s)$

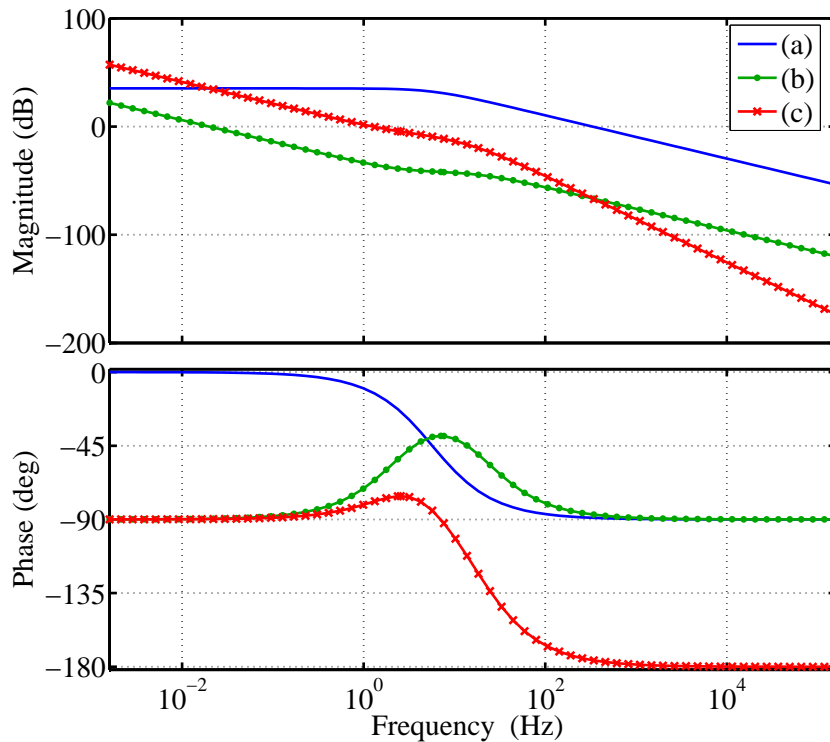
## 4.2.6 Voltage-Loop Compensator Design

The outer voltage-loop controls the average cell bus-voltage value. The value is adjusted by adjusting the peak input inductor-current value, while maintaining its sinusoidal profile. This is a 50 Hz current profile which causes a 100 Hz bus-voltage ripple around the desired average value. This is expected from a full-bridge rectifier. The voltage-loop should thus ignore the 100 Hz ripple to avoid distorting the controlled input inductor-current.

From Figure 4.17 it is clear that the voltage-loop compensator,  $C_V$ , would have to suppress the voltage-loop plant,  $G_V$ , to lower the loop bandwidth. Graphical methods are used, utilising the MATLAB<sup>®</sup> SISO design tool to design the compensator. This includes an integrator together with a pole at 20 Hz, to suppress noise spikes as well as current distortion. A zero is placed at  $20/8$  Hz to provide a boost at low frequencies. The voltage-loop compensator is thus given as:

$$C_V(s) = \frac{s + (\frac{1}{8}20 \cdot 2\pi)}{s(s + (20 \cdot 2\pi))} = \frac{s + 15.71}{s(s + 125.66)} \quad (4.2.42)$$

Figure 4.18 shows the frequency response of the voltage-loop plant, compensator and open-loop system.

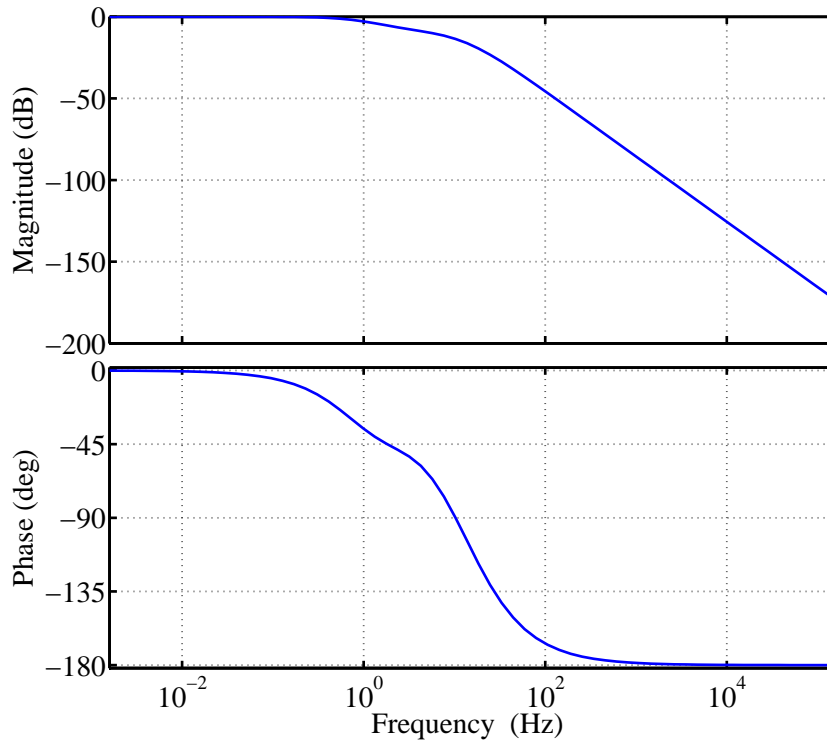


**Figure 4.18:** Frequency Response of: (a)  $G_V(s)$ ; (b)  $C_V(s)$ ; (c)  $C_V(s) \cdot G_V(s)$

Figure 4.19 shows the closed-voltage-loop frequency response, resulting in a voltage-loop bandwidth of:

$$BW_V = 1.04 \text{ Hz} \quad (4.2.43)$$

The open voltage-loop as well as the closed voltage-loop response are further analysed in Appendix B.3.3. Due to the lack of stringent voltage-loop specifications, the designed compen-



**Figure 4.19:** Closed Voltage-Loop Frequency Response

sator,  $C_V$ , is subject to modification. Findings during the testing phase might require changes in terms of bandwidth and transient response. Any such modifications will be noted.



### 4.3 Control Simulation

Time domain simulations are performed to verify the functionality of the designed current- and voltage-loop. The simulation software-package used is Simplorer 8 from Ansoft LLC. The compensators are implemented as time-domain transfer-function blocks, the plant is implemented as an electrical circuit and the control-loop feedback is implemented as circuit measurements. The compensators are designed in the continuous time domain and simulated with very small time steps. This method is suitable because each implemented control loop is clocked much faster than its respective bandwidth. For example, the current-loop is clocked at 10MHz, as mentioned in Section 4.2, while it has a bandwidth in the order of a kHz as mentioned in Section 4.2.4. A 0.1  $\mu$ s clock time thus seems like continuous time in comparison with a 4.9 kHz bandwidth.

#### 4.3.1 Current-Loop Simulation

The current-loop simulation is a test where an AC inductor-current,  $I_L$ , is drawn from a AC input voltage,  $V_{ac}$ . It is aimed at verifying successful circuit and control integration as well as current-loop functionality in terms of its reference tracking ability. The various components of this simulation, as shown in Figure 4.20, are set up as listed in Appendix B.4.1.

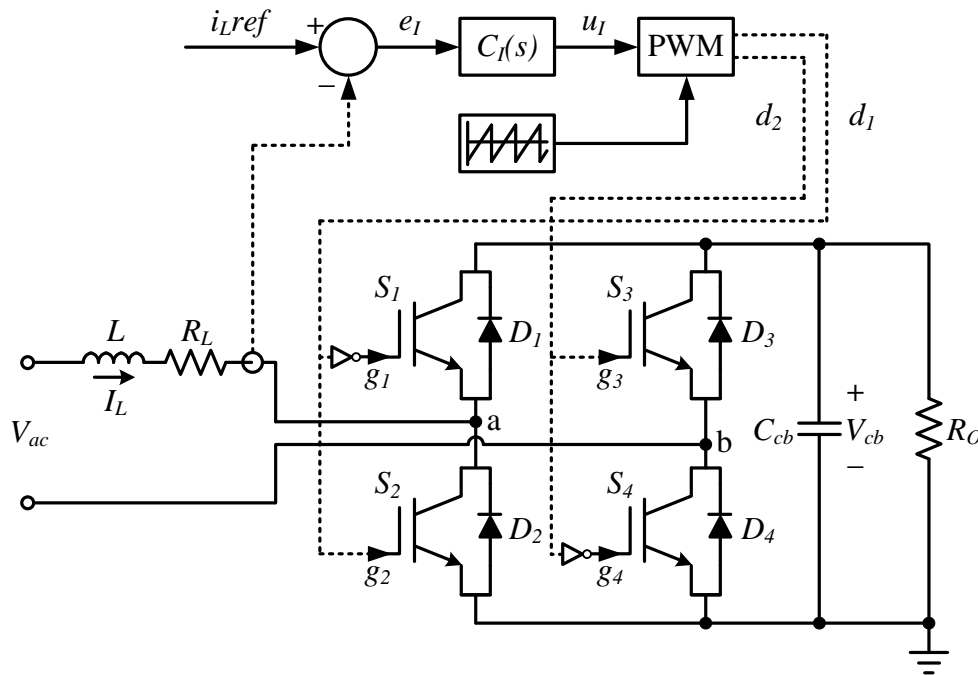
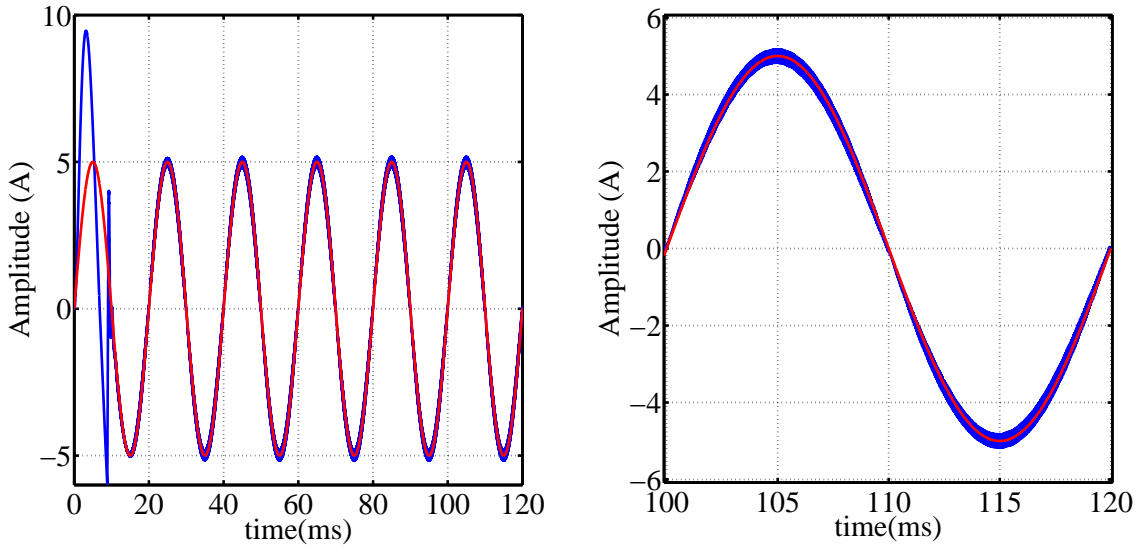


Figure 4.20: Current-Loop Simulation Setup

Figure 4.21 depicts the inductor-current transient response on the left and its steady-state result on the right, together with the current reference signal,  $i_L ref$ . The transient response indicates a high current peak, which means a specific startup sequence will be necessary when this test is physically implemented. The steady-state result indicates excellent reference tracking.

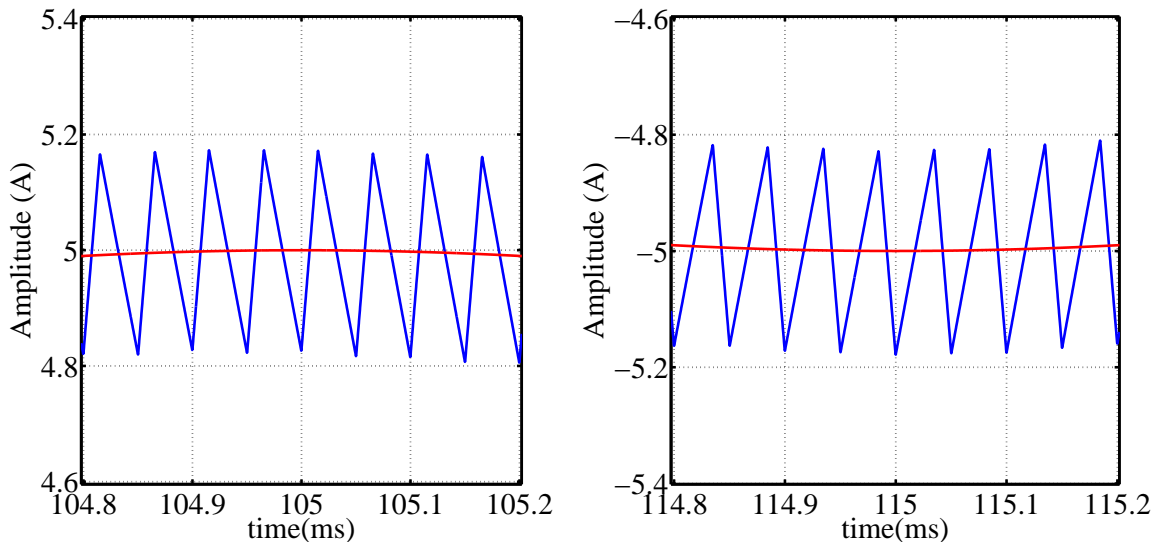
Figure 4.22 depicts the inductor-current maximum and minimum on the left and right respectively. The switching ripple at the sinusoidal extremities, can thus be calculated as:



**Figure 4.21:** Inductor Current and Current-Loop Reference

$$rip\% = \frac{rip_{max} - rip_{min}}{i_{Lrefp}} = \frac{5.172 - 4.817}{5} = 7.1\% \quad (4.3.1)$$

with  $i_{Lrefp}$  defined as the reference peak,  $rip_{max}$  defined as the maximum ripple value around this peak and  $rip_{min}$  defined as the minimum ripple value around this peak. This result is quite acceptable, although it is not the maximum ripple. Examining Figure 4.21 and 4.23, it is found that the maximum ripple occurs at the time of maximum  $v_{cb}$  when  $i_L$  is positive, and at the time of minimum  $v_{cb}$  when  $i_L$  is negative. Section 4.2.2 does not indicate this, due to the analysis assumptions. It is assumed that  $v_{ac}$  is constant, compared to the  $i_L$  rate of change, and the  $v_{cb}$  ripple effects are also ignored.



**Figure 4.22:** Inductor Current and Current-Loop Reference

Figure 4.23 depicts the cell bus-voltage,  $v_{cb}$ , transient response on the left and its steady-state result on the right. The transient response indicates no voltage peaks and the steady state

response indicates an acceptable average value. The expected 100 Hz voltage ripple, of a rectified 50 Hz input voltage, is also clearly visible.

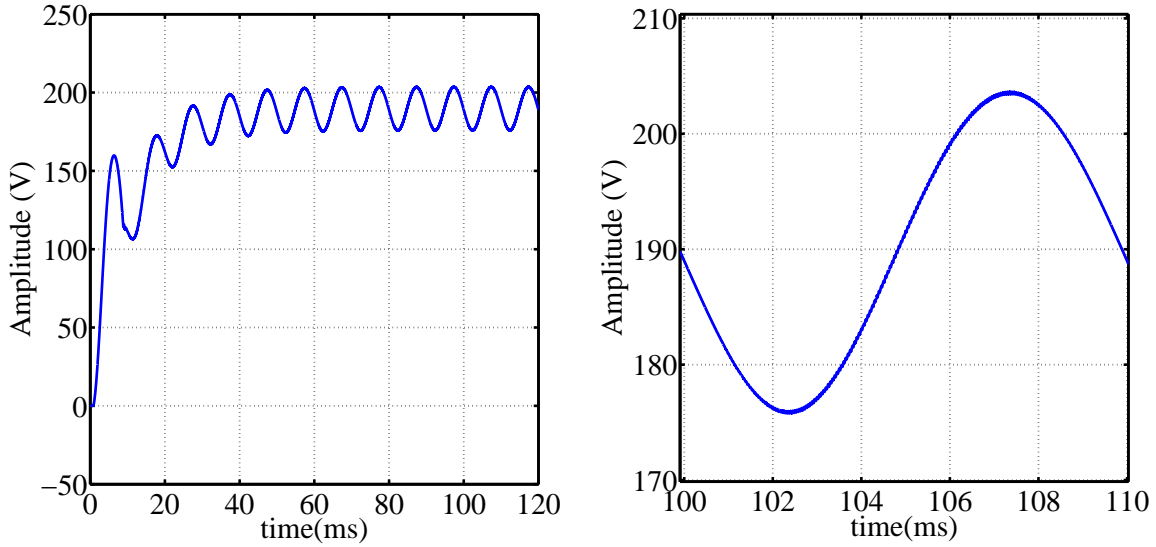


Figure 4.23: Cell Bus-Voltage

Figure 4.24 indicates the small switching ripple present on the cell bus voltage.

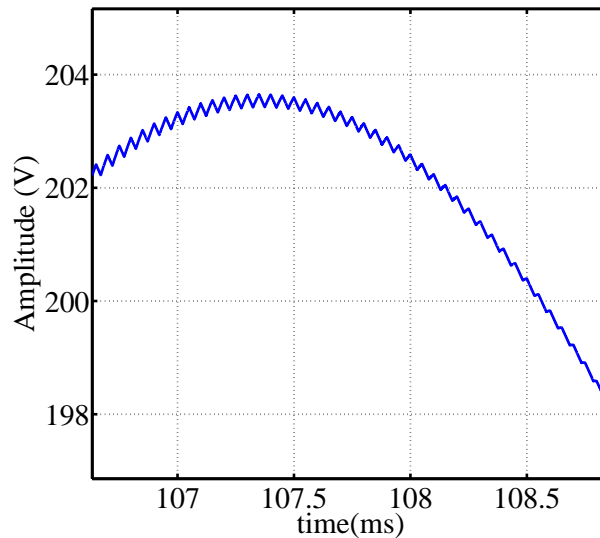


Figure 4.24: Cell Bus-Voltage

Figure 4.25 depicts the compensator output,  $u_I$ , transient response on the left and its steady-state result on the right, together with the two sawtooth carrier-signals. The transient response, as with the inductor-current transient response, indicates where the AR operates as a full-bridge passive rectifier. This operation causes  $u_I$  to exceed the carrier amplitude limits, because the current-loop attempts to control a system over which it has no control. The steady state response has a sinusoidal shape with a  $180^\circ$  phase shift, compared to the current reference signal.

Figure 4.26 depicts the compensator-output minimum and maximum on the left and right respectively. The compensator-output ripple indicates the effect of the compensator, on the feedback inductor-current ripple.

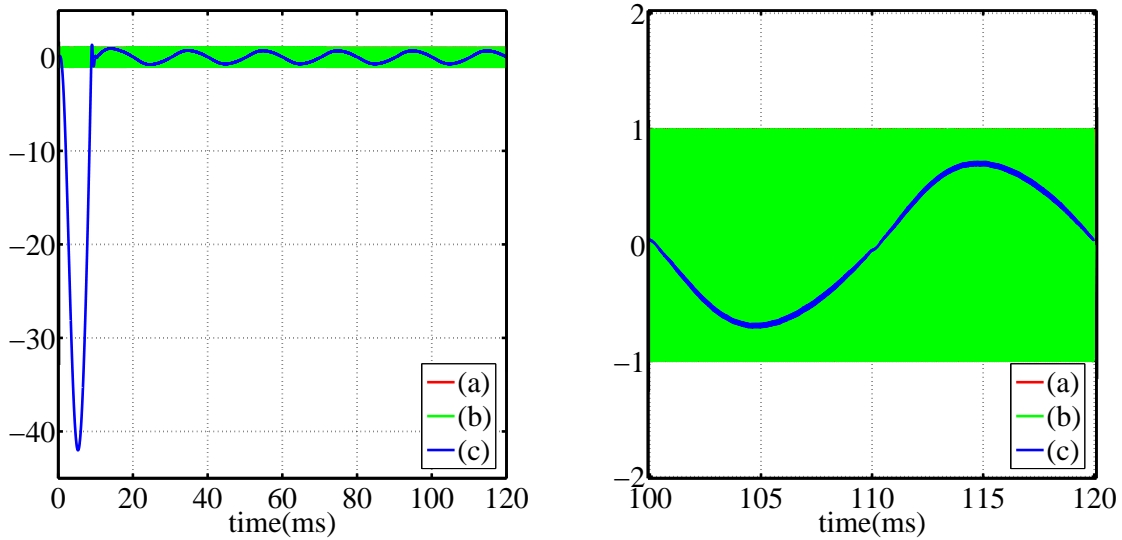


Figure 4.25: PWM Signals: (a) Carrier1; (b) Carrier2; (c)  $u_I$

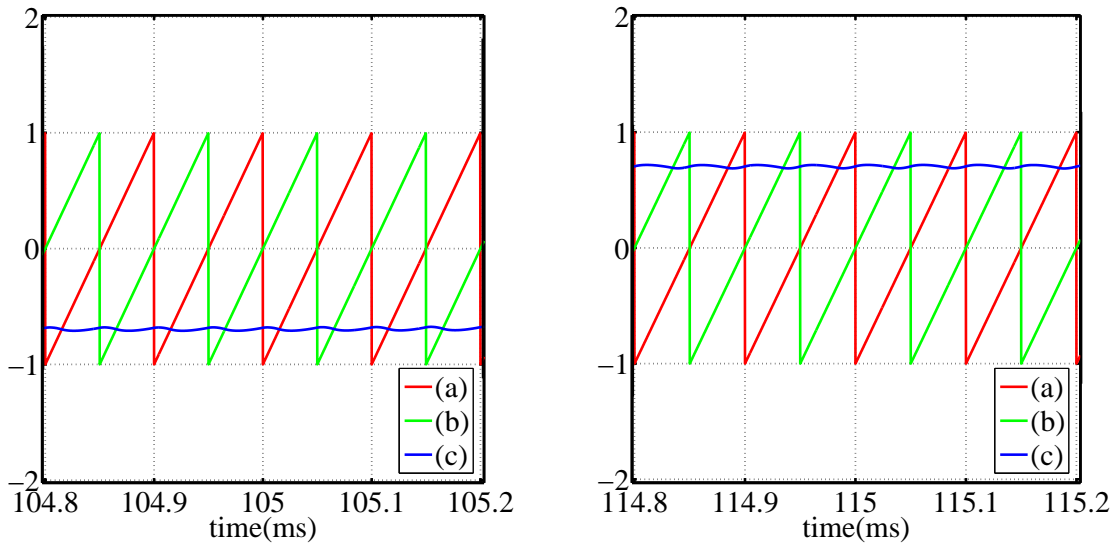


Figure 4.26: PWM Signals: (a) Carrier1; (b) Carrier2; (c)  $u_I$

The results obtained from this simulation are satisfactory in determining current-loop functionality. Simulation results showing the current-loop reaction to reference steps are discussed in Appendix B.4.2.

### 4.3.2 Active-Rectifier Simulation

The AR simulation is a test where an AC inductor-current,  $I_L$ , is drawn from a AC input voltage,  $V_{ac}$ , to maintain a specific average bus-voltage,  $V_{cb}$ . It is aimed at verifying successful current- and voltage-loop integration as well as voltage-loop functionality in terms of its reference tracking ability. The various components of this simulation, as shown in Figure 4.27, are set up as listed in Appendix B.4.3.

Figure 4.28 depicts the  $v_{cb}$  transient response on the left and its steady-state result on the right. The transient response indicates acceptable voltage peaks and shows a slower bus charge-up, compared to the current-loop simulation. This is due to the low bandwidth of the voltage-

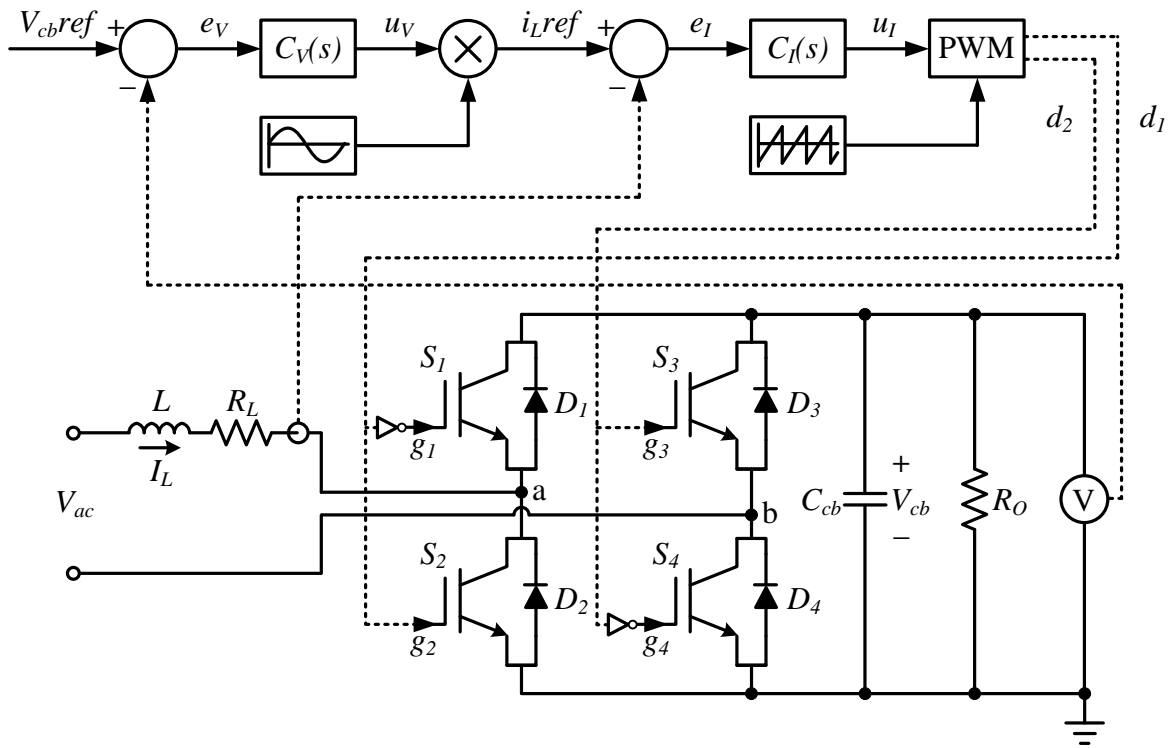


Figure 4.27: Active-Rectifier Simulation setup

loop. It is also clear that the AR only starts normal operation once  $v_{cb}$  is larger than  $v_{ac}$ . The AR operation prior to this point is analysed in the inductor-current discussion to follow. The steady state response indicates an acceptable average value. The expected 100 Hz voltage ripple of a rectified 50 Hz input voltage, is also clearly visible.

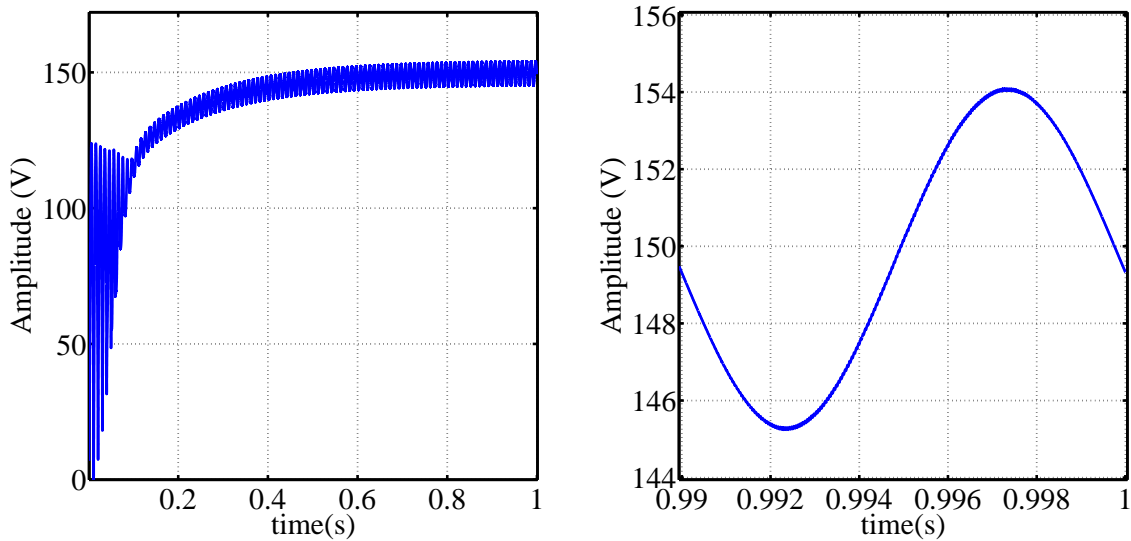
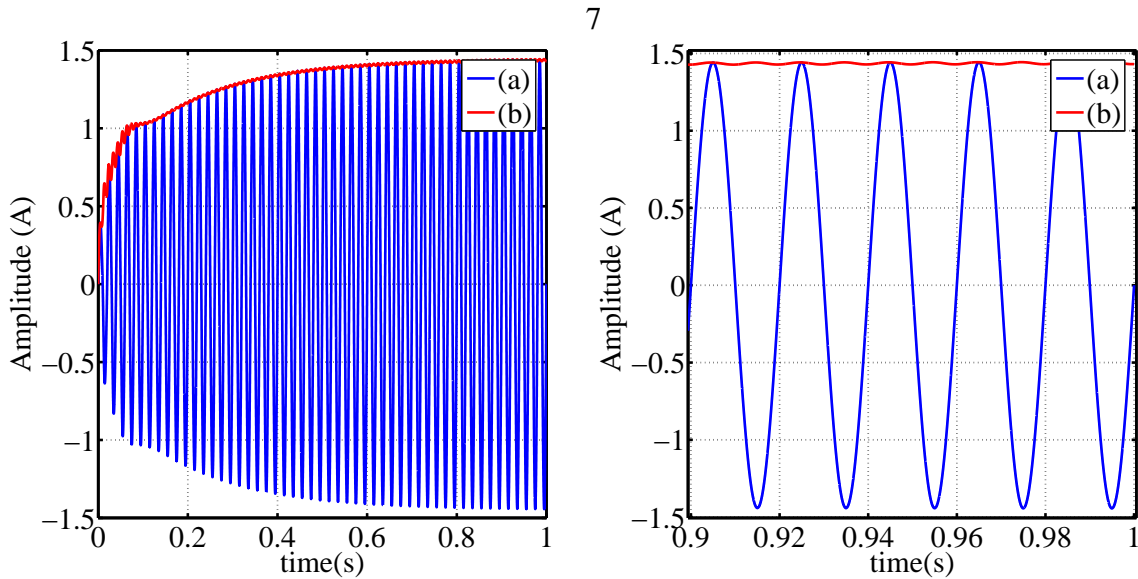


Figure 4.28: Cell Bus-Voltage

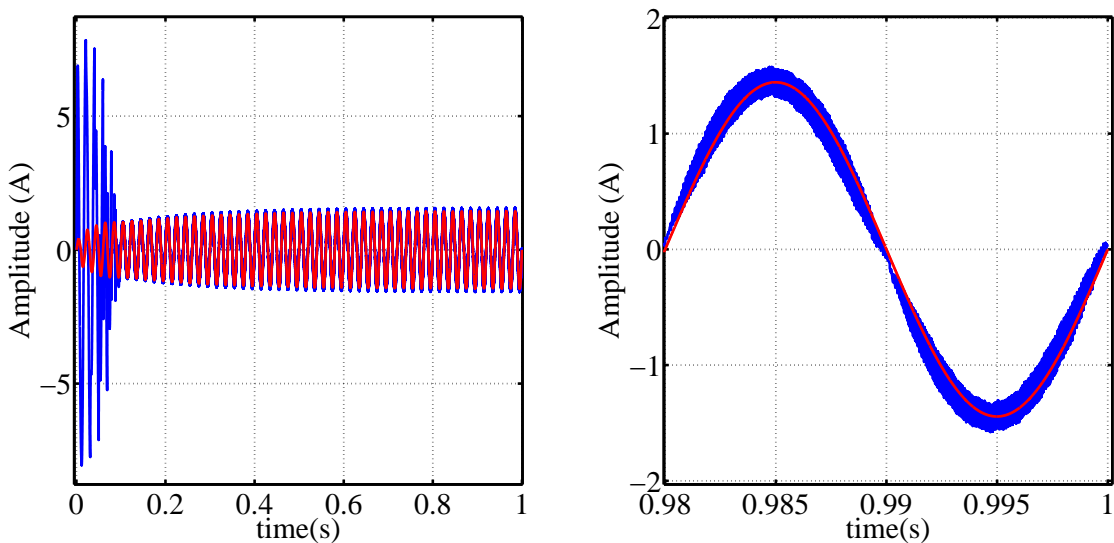
Figure 4.29 depicts the  $i_{Lref}$  and  $u_v$  transient response on the left and their steady-state result on the right. The  $i_{Lref}$  signal is the result of  $u_v$  multiplied with the unit sinusoid which is in phase with  $V_{ac}$ . This means that the transient response of  $i_{Lref}$  is directly related to the low bandwidth of the voltage-loop. The steady-state result highlights the necessity for

this low voltage-loop bandwidth. An increase in bandwidth will cause an increase in the  $u_V$  ripple amplitude. This will, in turn, increase the harmonic distortion of  $i_{Lref}$  and thus also the harmonic distortion of  $i_L$ .



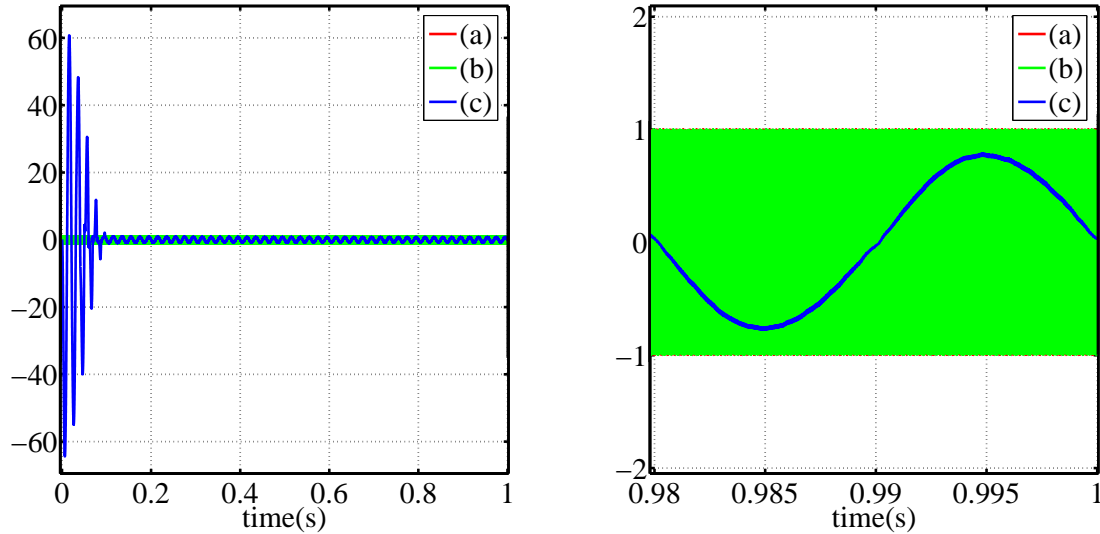
**Figure 4.29:** (a) Current-Loop Reference; (b) Voltage-Loop Compensator Output

Figure 4.30 depicts the  $i_L$  transient response on the left and its steady-state result on the right, together with  $i_{Lref}$ . The transient response indicates high current peaks, as with the current-loop simulation, which means a specific startup sequence will be necessary when this test is physically implemented. The current reference transient response causes a slower current transient response, compared to the current-loop simulation. While  $v_{cb}$  is smaller than  $v_{ac}$ , diodes  $D_{1-4}$  act as a full-bridge passive rectifier, which causes the extensive current peaks. The steady-state result, as with the current-loop simulation, indicates excellent reference tracking. The current ripple seems less smooth compared to the current-loop simulation. This is due to a larger simulation time-step, required to facilitate a larger total simulation-time.



**Figure 4.30:** Inductor Current and Current-Loop Reference

Figure 4.31 depicts the compensator output,  $u_I$ , transient response on the left and its steady-state result on the right, together with the two sawtooth carrier-signals. The transient response, as with the inductor-current transient response, indicates where the AR operates as a full-bridge passive rectifier. This operation causes  $u_I$  to exceed the carrier amplitude limits, because the current-loop attempts to control a system over which it has no control. The steady state response has a sinusoidal shape with a  $180^\circ$  phase shift, compared to the current reference signal.



**Figure 4.31:** PWM Signals: (a) Carrier1; (b) Carrier2; (c)  $u_I$

The results obtained from this simulation are satisfactory in determining voltage-loop as well as system functionality. Simulation results showing the system reaction to load steps are discussed in Appendix B.4.4.

## 4.4 Control Implementation

The AR control strategy is jointly implemented within the MC and CC, as depicted in Figure 4.32. The input-inductor current measurement,  $i_L(t)$ , is sampled by the MC and subtracted from the current-loop reference,  $i_Lref$ . The error,  $e_I$ , is converted by the current compensator,  $C_I(z)$ , to determine the compensator output-signal,  $u_I$  representing an AR duty-cycle command. This signal is fed to the PWM to determine the point at which a state-change occurs. At this point,  $u_I$  is sent to the CC via the forward fibre of the fibre-optic channel. In the CC,  $u_I$  is fed to its PWM to determine the AR duty-cycle,  $D$ , in the form of the four gate-signals,  $g_{1-4}$ . The cell bus-voltage measurement,  $v_{cb}$  is sampled by the CC and sent to the MC via the reverse fibre of the fibre-optic channel. In the MC,  $v_{cb}$ , is subtracted from the voltage-loop reference,  $V_{cbref}$ . The error,  $e_V$ , is converted by the voltage compensator,  $C_V(z)$ , to determine the compensator output-signal,  $u_V$  representing a current-command. This signal is multiplied with the unit-amplitude sinusoid to determine the current-loop reference,  $i_Lref$ . The unit-amplitude sinusoid is synchronised with the input voltage,  $v_{ac}$ , which is also sampled by the MC.

All calculations are implemented using two identical FPGA's, one on the MC and one on the CC. All sampling is implemented using identical ADC's. Using the same components as far as possible has quite a few advantages, including increased modularity and shortened development time. The FPGA's are programmed using Very-High-Speed Integrated Circuit Hardware



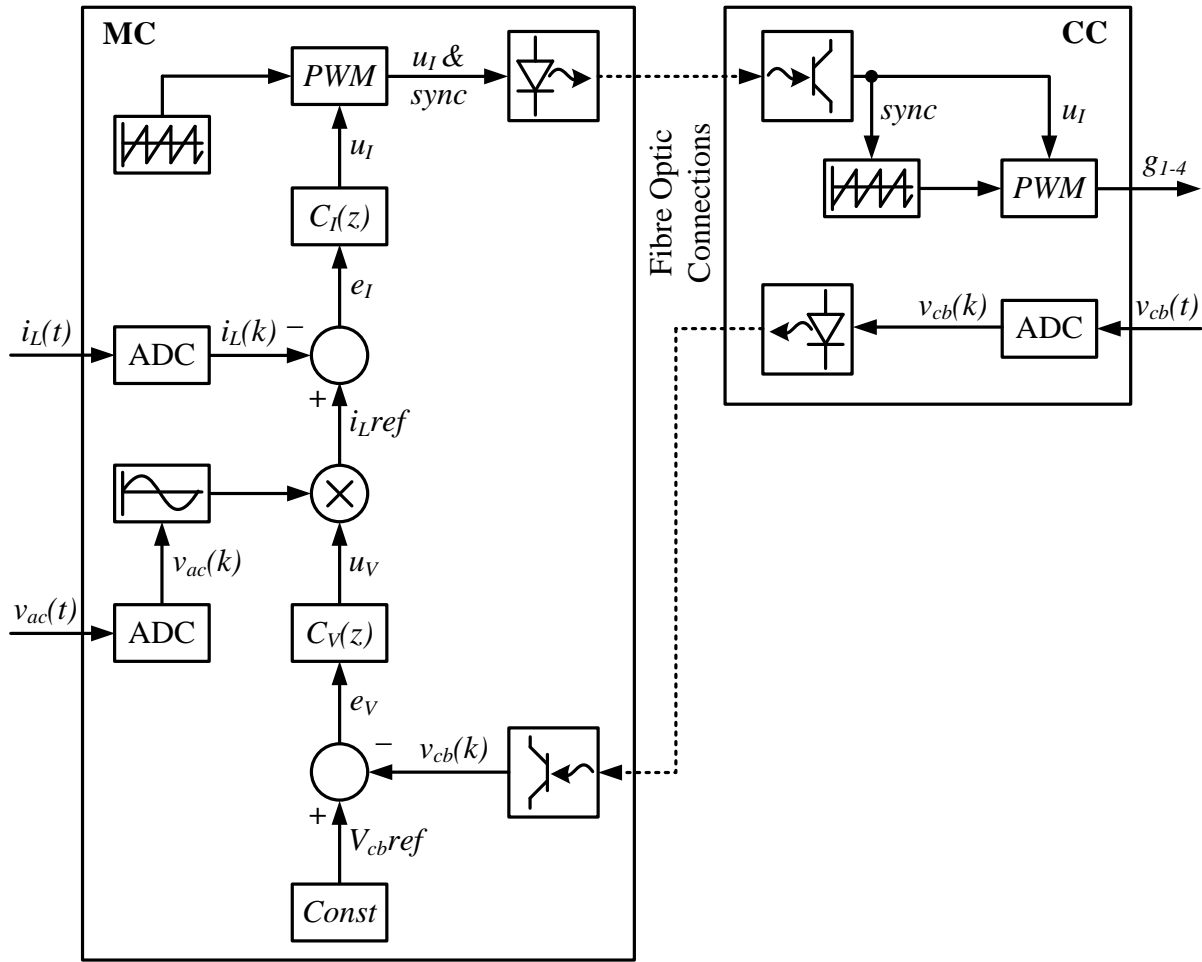


Figure 4.32: AR Control Implementation

Description Language (VHDL). This enables parallel processing as well as a modular programming structure. The functionality required is implemented by programming in building blocks, called components. These components each have an input clock and a combination of I/O ports, used to connect components to each other. Some of these components are implemented in both FPGA's, which also shortens development time.

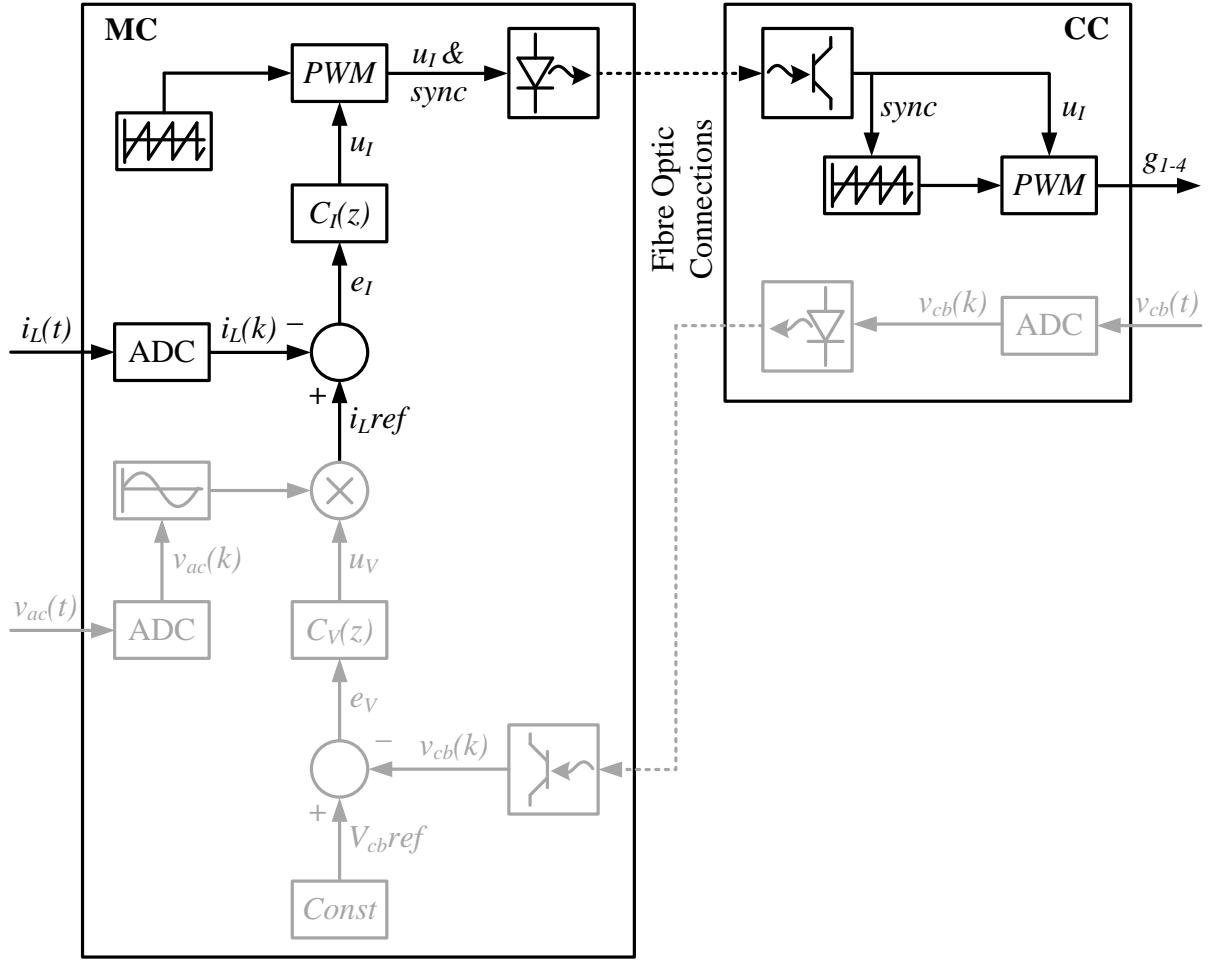
In the remainder of this section the AR control implementation is further described. Key components of each control loop are emphasized in terms of implementation techniques and hardware utilisation. Implementation challenges as well as their solutions are also discussed.

#### 4.4.1 Current-Loop Implementation

The current loop is defined, in terms of implementation, as the control section from  $i_{Lref}$  to  $g_{1-4}$ , as depicted in Figure 4.33. The current loop can thus be tested separately from the voltage loop. For such a test,  $i_{Lref}$  is set to a constant value, for a DC test, or a sinusoid with constant amplitude, for an AC test. This sinusoid should be synchronised with  $V_{ac}$ .

The discrete input-inductor current measurement is received from the ADC, at a 10 MHz sample rate. Each sample is scaled to a current value represented in amperes:

$$i_L(k) = \frac{(ADC_{OUT} - 0x800)}{RATIO \cdot 2 \cdot A2 \cdot A1 \cdot ALEM} \quad (4.4.1)$$


**Figure 4.33:** AR Current-Loop Implementation

The hexadecimal value, 0x800, is the zero-offset of the ADC output,  $ADC_{OUT}$ .  $RATIO$  is the ADC conversion ratio, as discussed in Appendix A.7.1. The factor 2 is due to the differential ADC input.  $A1$  and  $A2$  are the op amp gains of the measurement PCB and secondary measurement-circuit, discussed in Appendix A.1.1 and A.4.1 respectively. The current transducer gain,  $A_{LEM}$ , is defined as [17]:

$$A_{LEM} = \frac{(LEM_{OUT} - V_{cm})}{i_L} = 104.1667 \times 10^{-3} \quad (4.4.2)$$

Eq. 4.4.1 can thus be quantified as:

$$i_L(k) = (ADC_{OUT} - 0x800) \times 9.374973 \times 10^{-3} \quad (4.4.3)$$

The scaled samples are subtracted from  $i_L(ref)$  to determine  $e_I$ , the input of the compensator,  $C_I(z)$ . This discrete compensator form is obtained by using the bilinear approximation together with the  $c2d$  function in MATLAB<sup>®</sup>. The bilinear approximation utilises the s-plane to z-plane mapping:

$$s = \frac{2}{T} \cdot \frac{z-1}{z+1} \quad (4.4.4)$$

where  $T$  is the sample rate. Substitution of Eq. 4.4.4 into Eq. 4.2.35 yields the discrete compensator transfer function:

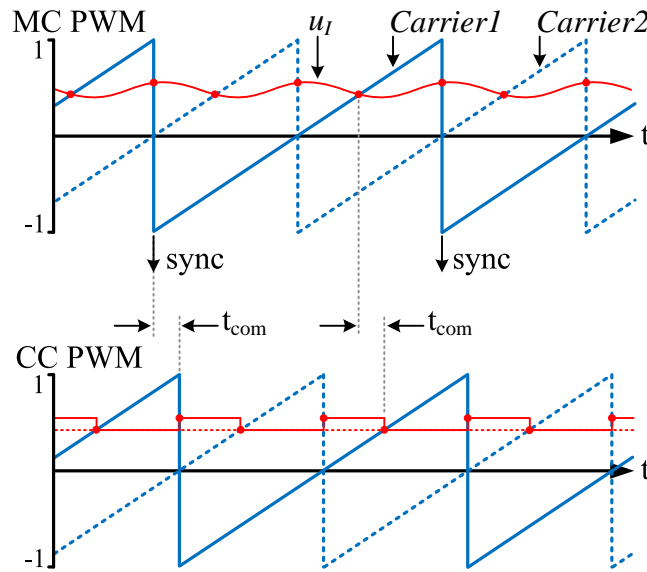
$$C_I(z) = 7.7718 \times 10^{-4} \times \frac{(z - 0.9986)(z + 1)}{(z - 1)(z - 0.9913)} \quad (4.4.5)$$

which leads to the difference-equation compensator form:

$$u_I(k) = -0.9913u_I(k - 2) + 1.9913u_I(k - 1) - 7.7606 \times 10^{-4}e_I(k - 2) + 1.1261 \times 10^{-6}e_I(k - 1) + 7.7718 \times 10^{-4}e_I(k) \quad (4.4.6)$$

which is implemented in the compensator component, clocked at 10 MHz. The subtraction to determine  $e_I$  is also implemented in this component. The compensator output,  $u_I(k)$ , is limited between 1.01 and -1.01. This limit is slightly outside the carrier amplitude-limits, to facilitate all possible state-changes. The main function of this limit however, is to prevent the compensator integrator-output from increasing to extreme values. When this output reaches such extremes and the error signal changes in polarity, it has to decrease from this extreme. The extreme decrease may cause a negative overshoot. This chain of events may cause system instability and/or numerical overflow and it might be repeated to cause system oscillation.

The PWM component implements unipolar-voltage switching, by comparing  $u_I(k)$  with two sawtooth carriers, as explained in Section 4.2.1. The carriers are each implemented with a counter, clocked at 10 MHz, which continuously counts from -1 to 1 after which resetting, again to -1. The counter increment-value is calculated to produce carriers with a frequency of  $f_s$ , and the initial counter-value is calculated to incorporate a carrier phase-shift of  $180^\circ$ . The PWM component is also clocked at 10 MHz. Multisampling PWM is thus implemented, because the entire current-loop is clocked at 10 MHz, up until and including the PWM component. This is much faster than the carrier frequency of 10 kHz. From the PWM component, the rate of change is dependent on the time between  $u_I$ -carrier crossings. The only information required by the CC, is thus the time of each  $u_I$ -carrier crossing and the  $u_I(k)$  value at that point. This leads to the particular PWM communication protocol, as depicted in Figure 4.34.



**Figure 4.34:** PWM Communication Protocol

To relay the PWM information to the CC, two package types are sent. The first is a synchronise package, sent at every down-slope of *carrier1*. This package contains a synchronise-

carriers command, as well as the  $u_I$  value at that moment in time. The second package type is a reference package sent at every  $u_I$ -carrier crossing, excluding the crossing at the *carrier1* down-slope. This package contains a reference command, as well as the  $u_I$  value at that moment in time. When receiving a synchronise package<sup>4</sup>, the CC resets its carriers and updates its  $u_I$  value, whereas on receiving a reference package, the CC only updates its  $u_I$  value. This communication protocol ensures that the  $u_I$ -carrier crossings and thus the system state-changes, are implemented by the CC, exactly as they occur on the MC. The only difference is the time delay,  $t_{com}$ , which is the time required to send a communication package. The  $u_I$  signal is effectively sampled at  $u_I$ -carrier crossings and sent to the CC. The time delay is relatively small, as discussed below, and does not have a significant effect on the AR control.

The data package is sent via two Serial Communication Interface (SCI) components<sup>5</sup>, one on both the MC and the CC. Both these components are clocked at 80 MHz to achieve a baudrate of 5 Mega Baud (MBd) across the fibre-optic channels. This results in a bit transfer rate of 10 MHz. The package consists of 32 bits, with 8 bits allocated to the package command, 12 bits allocated to the AR control and another 12 bits allocated to the DC-DC control. The data is sent least significant bit first. There is one start bit, one parity bit and two stop bits, as depicted in Figure 4.35.

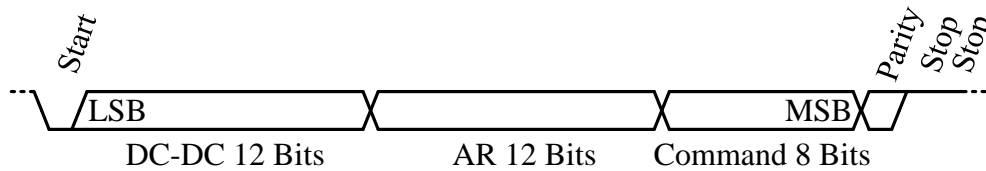


Figure 4.35: Communication Package

This results in a package transfer time of:

$$t_{com} = T_1 + \frac{n}{10 \times 10^6} + T_2 = 0.05 \mu\text{s} + 3.6 \mu\text{s} + 0.16 \mu\text{s} = 3.81 \mu\text{s} \quad (4.4.7)$$

with  $n$  defined as the number of bits in a package,  $T_1$  defined as the time from a transmit-trigger to the start of transmission and  $T_2$  defined as the time from the end of transmission to having data available for use in other components.

The CC PWM component implements the same switching scheme as the MC PWM component and is also clocked at 10 MHz. The difference between these components is that the CC component generates the gating signals,  $g_{1-4}$ , which triggers the IGBT driver-circuits on the cell. Both MC and CC use the same carrier generation components.

## 4.4.2 Voltage-Loop Implementation

The voltage loop is defined, in terms of implementation, as the control section from  $V_{cbref}$  to  $i_Lref$ , as depicted in Figure 4.36.

The discrete cell bus-voltage measurement is received from the CC ADC, at a 10 MHz sample rate. Each sample is scaled, by the CC, to a voltage value represented in volts. This scaled measurement has a resolution of 1 V, which is sent to the MC in the AR-control allocation in the communication package. This  $v_{cb}$  measurement package is sent as reply to any of the

<sup>4</sup>The CC carriers are synchronised, at every MC carrier1 down-slope, to prevent carrier drift between the MC and CC.

<sup>5</sup>Developed by [11]

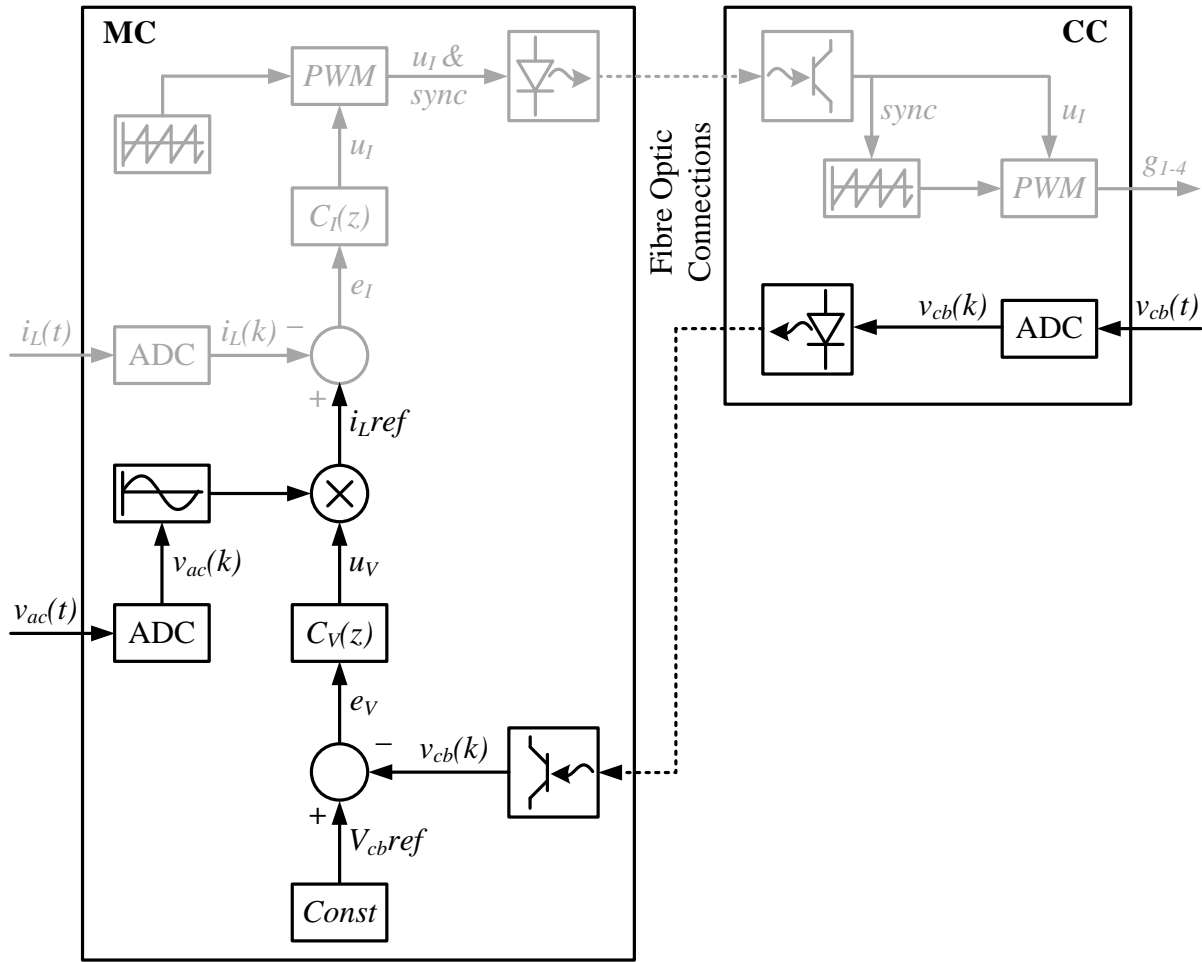


Figure 4.36: AR Voltage-Loop Implementation

two relevant packages discussed in Section 4.4.1. This reply also acts as a communication functionality check. The MC reacts if this reply is not received within a predefined time, after an AR-control package was sent. The MC assumes communication loss and moves to an error state.

The MC updates its  $v_{cb}(k)$  sample value, as the  $v_{cb}$  measurement package is received. This means that  $v_{cb}(k)$  is updated four times in a 10 kHz carrier period, with only two at fixed intervals, as shown in Figure 4.34. The samples are subtracted from the constant reference,  $V_{cb}(ref)$ , to determine  $e_V$ , the input of the compensator,  $C_V(z)$ . This discrete compensator form is also obtained by using the bilinear approximation together with the  $c2d$  function in MATLAB<sup>®</sup>. This compensator, together with the subtraction to determine  $e_V$ , is implemented in a single component, clocked at a much slower 20 kHz, because of its much lower bandwidth, compared to  $C_I(z)$ . Substitution of Eq. 4.4.4 into Eq. 4.2.42 yields the discrete compensator transfer function:

$$C_V(z) = 24.931 \times 10^{-6} \times \frac{(z - 0.9993)(z + 1)}{(z - 1)(z - 0.9937)} \quad (4.4.8)$$

which leads to the difference-equation compensator form:

$$u_V(k) = -0.9937u_V(k-2) - 1.9937u_V(k-1) - 24.9111 \times 10^{-6}e_V(k-2) + 19.945 \times 10^{-9}e_V(k-1) + 24.931 \times 10^{-6}e_V(k) \quad (4.4.9)$$

which is implemented in the compensator component. This component also limits  $u_V(k)$  between  $I_{Lp}$  and  $-1$ , which limits  $i_L(ref)$  and thus  $i_L$ . The maximum limit is to protect the cell from over-current. The maximum negative-limit is to enable the AR to dump a limited amount of energy back into the grid, when necessary, to lower the cell bus-voltage more effectively. This functionality is especially useful when the cell bus-voltage needs to be lowered under no-load conditions. Another function of these limits, however, is to prevent the compensator integrator-output from increasing to extreme values. When this output reaches such extremes and the error signal changes in polarity, it has to decrease from this extreme. The extreme decrease may cause a negative overshoot. This chain of events may cause system instability and/or numerical overflow and it might be repeated to cause system oscillation.

The discrete input-voltage measurement is received from the ADC, at a 200 kHz sample rate. Each sample is scaled to a voltage value represented in volts:

$$v_{ac}(k) = \frac{(ADC_{OUT} - 0x800) \cdot N_2}{RATIO \cdot 2 \cdot A2 \cdot A1 \cdot N_1} \quad (4.4.10)$$

The hexadecimal value, 0x800, is the zero-offset of the ADC output,  $ADC_{OUT}$ .  $RATIO$  is the ADC conversion ratio, as discussed in Appendix A.7.1. The factor 2 is due to the differential ADC input.  $A1$  and  $A2$  are the op amp gains of the measurement PCB and secondary measurement-circuit, discussed in Appendix A.2.1 and A.5.1 respectively. The step-up transformer ratio,  $\frac{N_2}{N_1}$ , is defined as:

$$\frac{N_2}{N_1} = \frac{6600}{400} \quad (4.4.11)$$

Eq. 4.4.10 can thus be quantified as:

$$v_{ac}(k) = (ADC_{OUT} - 0x800) \times 2.905 \quad (4.4.12)$$

The scaled samples are used to detect the  $v_{ac}$  zero-crossings to synchronize the unit-sinusoid with  $v_{ac}$ . The clock cycles between zero-crossings are counted to determine the exact frequency of  $v_{ac}$ . At every  $v_{ac}$  negative to positive zero-crossing, the unit-sinusoid is reset to start from zero. Its frequency is also adjusted at this point, within a range of 47.62 - 52.63 Hz, to closely match  $v_{ac}$ . This matched unit-sinusoid is multiplied with  $u_V$  to determine  $i_L(ref)$ .

The multiplication component, the unit-sinusoid component and the component responsible for its synchronisation are all clocked at 200 kHz. There is also a component which checks the  $v_{cb}(k)$  sample as it is received from the CC. This component is clocked at 10 MHz. It is thus clear that all the MC components which form part of the voltage-loop are not clocked at the same rate. Flags are thus implemented between successive components to indicate when a component has updated its output value. These flags are necessary to prevent FPGA timing errors.

### 4.4.3 Startup Sequence

The startup sequence is defined as the sequence of events to start up the AR, from system power-up to AR-control enable to AR-shutdown, as shown in Figure 4.37. The CC is programmed with a *.jic* file which means its FPGA is automatically programmed at every power-up. This necessitates the firmware revision check. The MC is programmed with a *.sof* file which means its FPGA is programmed manually at every power-up.

As the MC is programmed, the start command is given and it opens the input relay disconnecting the input voltage, and initiates a time delay for the operator to do a quick visual

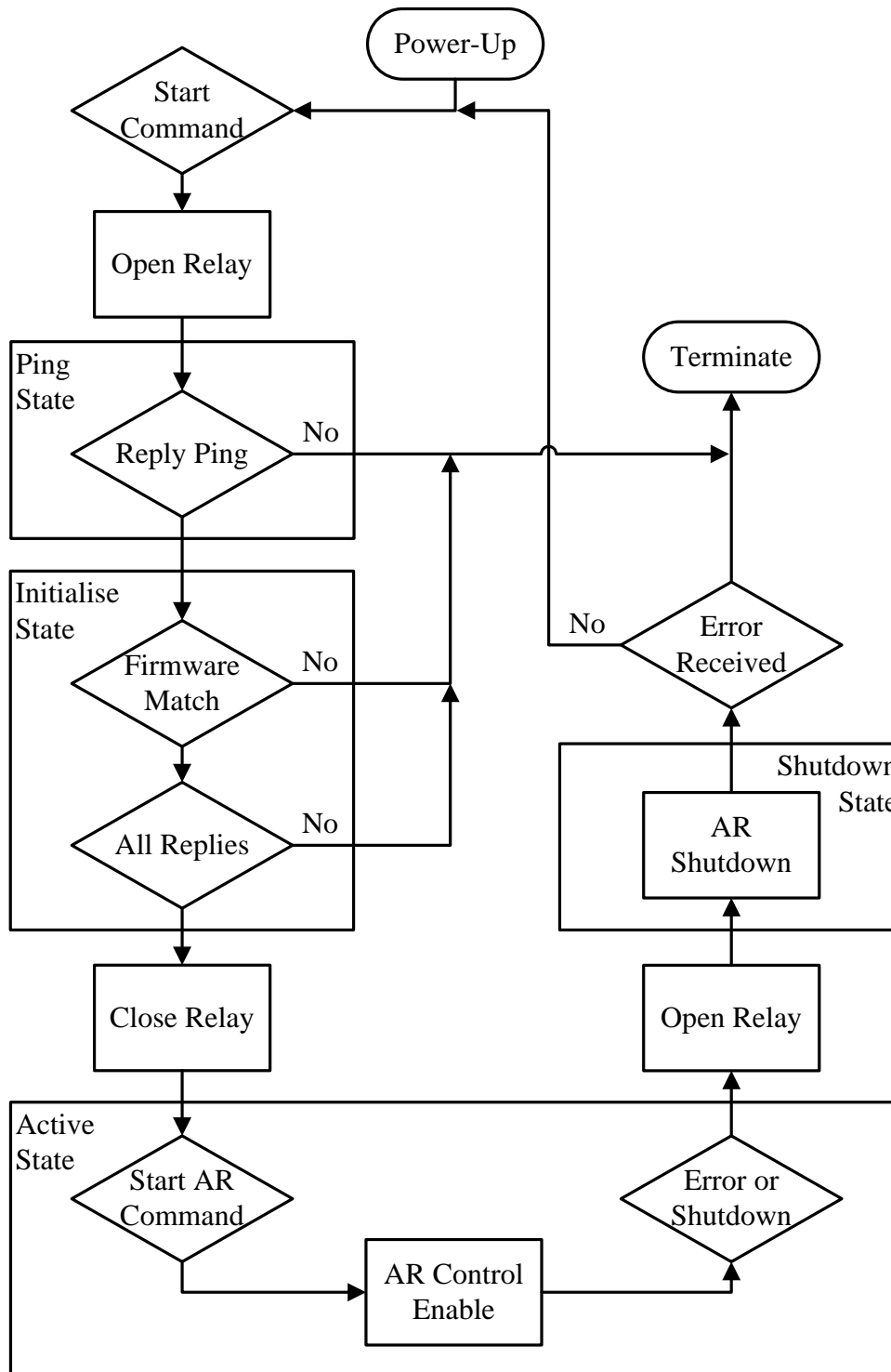


Figure 4.37: AR Startup Sequence



system check. The MC then moves to the ping state, where a ping package is sent to the CC to confirm successful communication with a reply ping-package. If a reply ping-package is not received within a predefined time, a second ping package is sent. A maximum of five ping packages are sent at one second intervals before a Ping-Error is triggered and the startup process is terminated.

Once a reply ping-package is received, the MC moves to the initialisation state where a sequence of packages is sent. The first package is a reset-cell package followed by an initialisation package and a request-firmware-revision-number package. The reply package holds the firmware-revision number of the firmware currently programmed on the CC. This number is compared to the required firmware-revision number. A Firmware-Revision-Number-Mismatch-Error is triggered if these numbers do not match and the startup process is terminated. If the firmware-revision numbers match, the MC sends a sequence of packages containing the measurement-limits for all the CC measurements. After all these package replies have been received, the MC sends a Detect-Cell-Bus-Voltage-Measurement-Offset package. This triggers the CC to measure its  $v_{cb}$  measurement-offset, and compensate its  $v_{cb}$  measurements in the active state. This concludes the initialisation. The MC closes the input relay and moves to the active state if all package replies have been received. Otherwise a Reply-Lag-Error is triggered and the startup-process is terminated

The active state is where the AR physically starts up. A specific startup sequence is necessary to prevent undesirable current peaks, as mentioned in Section 4.3.1 and 4.3.2. The key is to precharge the cell bus-capacitor,  $C_{cb}$ , before the AR control is enabled. This minimises in-rush currents and the initial error signal of the voltage loop,  $e_V$ , thus minimising the overshoot of the voltage-compensator output,  $u_V$ , and in turn the overshoot of  $i_L(ref)$  and  $i_L$ . Precharging  $C_{cb}$  also reduces the time where  $v_{cb}$  is less than  $v_{ac}$ , where the current-loop attempts to control a system over which it has no control.  $C_{cb}$  is precharged by slowly increasing  $v_{ac}$ , from zero, to a predefined value while the AR control is disabled. During this time the AR acts as a full-bridge passive rectifier and the diode currents charge  $C_{cb}$ . There are two ways of determining when  $C_{cb}$  has been precharged. One is checking the  $v_{ac}$  measurement and the second is checking the  $v_{cb}$  measurement. If the latter is implemented, the MC regularly sends Requesting-Bus-Voltage packages to the CC, to check this measurement.

Once  $C_{cb}$  has been precharged, the Start-AR command is given and the component responsible for synchronising the unit-sinusoid, is enabled. After three successfully synchronized cycles, the AR-control components are enabled and reset and an enable-AR package is sent to the CC. From this point the MC continually sends AR-control packages to the CC, as discussed in Section 4.4.1, which facilitates the control of  $v_{cb}$  at a certain average value, while drawing a sinusoidal input-current,  $i_L$ .

The AR remains in operation until a shutdown is triggered or any of the errors mentioned in Section 4.4.4 occur. This triggers the MC to open the input relay, disconnecting the input voltage, and move to the shutdown state. A shutdown-AR package is sent to the CC which triggers it to shut down the AR by disabling its AR control components and opening all AR switches. If the shutdown was triggered by the operator reducing the input voltage to a predefined value, the system resets and waits for the next start command. On the other hand, if the shutdown was triggered by an error, the system terminates. At this stage the operator should determine the cause of the error and rectify the problem.

#### 4.4.4 Error Handling

There are quite a few aspects that may cause the AR to malfunction. These aspects include hardware failure, hardware design mistakes, assembly mistakes, software design and imple-

mentation mistakes. Some mistakes or failures may cause the AR to operate abnormally, but still within acceptable ranges. Other mistakes or failures on the other hand, may cause voltages or currents to exceed acceptable ranges. These may cause AR damage as well as danger to the operator. The trouble is that the transition from safe to dangerous operation may occur too rapidly for the operator to shut down the AR. This necessitates the implementation of error handling firmware.

Errors can be classified as measurement errors and system errors. Measurements errors are defined as measurements exceeding predefined limits and system errors are defined as system malfunction. All measurements are checked for measurement errors. The measurements checked by the CC, for AR implementation, are:

- Cell Bus-Voltage,  $V_{cb}$
- Load Current<sup>6</sup>,  $I_{Ro}$
- IGBT Heat Sink Temperature,  $T_{sink}$
- Isolated Power Supply Voltage,  $V_{ips}$

The measurements checked by the MC, for AR implementation, are:

- Input Voltage,  $V_{ac}$
- Input-Inductor Current,  $I_L$
- Cell Bus-Voltage,  $V_{cb}$

The system errors handled by the MC are:

- **SCI Read Data Error:** When the SCI component indicates that a package could not be read successfully.
- **Firmware Revision Number Mismatch:** When the firmware revision, programmed on the CC, does not match the firmware revision required by the MC.
- **Ping Error:** When the CC does not echo the ping package sent at system startup.
- **Command Mismatch:** When any reply-package command sent by the CC does not match the package command sent by the MC.
- **Reply Lag Error:** When any reply package is not received within the predefined time.

With the occurrence of a CC measurement error during the active state, it sends an error package to the MC, with an error indicating command. When any of the MC measurement- or system-errors occur during the active state, or when an error package is received from the CC, the MC proceeds to the shutdown state as discussed in Section 4.4.3. The AR is thus shut down before any system damage or operator danger can arise.

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<sup>6</sup>This measurement circuitry is designed primarily to measure the Transformer Current,  $I_t$ , during implementation of the complete cell.

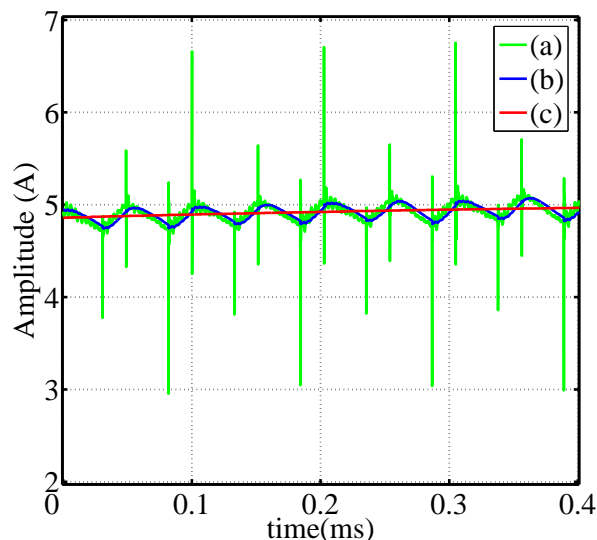
## 4.5 Test Measurements

Physical tests were performed to verify control-system functionality as a whole. All distinct aspects of the control system are also separately checked to establish proper functioning. These aspects include: all measurements, implemented compensators and other control components and the communication between the MC and CC. These checks are performed by utilising the Signal-Tap II Logic Analyzer development-tool within the Quartus 9 FPGA-development software package. This tool enables the developer to view any signal, programmed within the FPGA, while the firmware is in operation. Signals are sampled at a predefined sample rate and stored in a buffer within the FPGA. The buffer content is then downloaded at the command of the developer and displayed on screen. This is an extremely useful tool which plays a vital role in establishing firmware functionality as well as faultfinding and debugging.

The measurements taken vary between Signal-Tap measurements and Oscilloscope measurements. The Tektronix TDS 3014 Oscilloscope is used with a bandwidth of 100 MHz, capable of a 1.25 GS/s sample rate.

### 4.5.1 Current-Loop Test Measurements

The current-loop test, like the current-loop simulation, is a test where an AC inductor-current,  $i_L$ , is drawn from a AC input voltage,  $V_{ac}$ . It is aimed at verifying successful circuit and control implementation as well as current-loop functionality in terms of its reference tracking ability. The physical test setup, as depicted in Figure 4.39, is discussed in Appendix B.5.1. The measurements discussed in this section are AR steady-state measurements, as the startup measurements are discussed in Section 4.5.2. Figure 4.38 depicts the Signal-Tap measurement of  $i_L$  after firmware filtering and  $i_L(ref)$ . The inductor current measurement is filtered in firmware to remove the switching noise before feeding it to the current-loop. This 1<sup>st</sup> order low-pass filter is programmed with a 30 kHz cutoff frequency. Its gradual cutoff allows the 20 kHz switching ripple to pass through while blocking the switching noise. The  $i_L$  measurement will refer to the filtered  $i_L$  measurement throughout the rest of the Test Measurements Section.



**Figure 4.38:** Signal-Tap Measurement: (a)  $i_L$ ; (b) Filtered  $i_L$ ; (c)  $i_L(ref)$

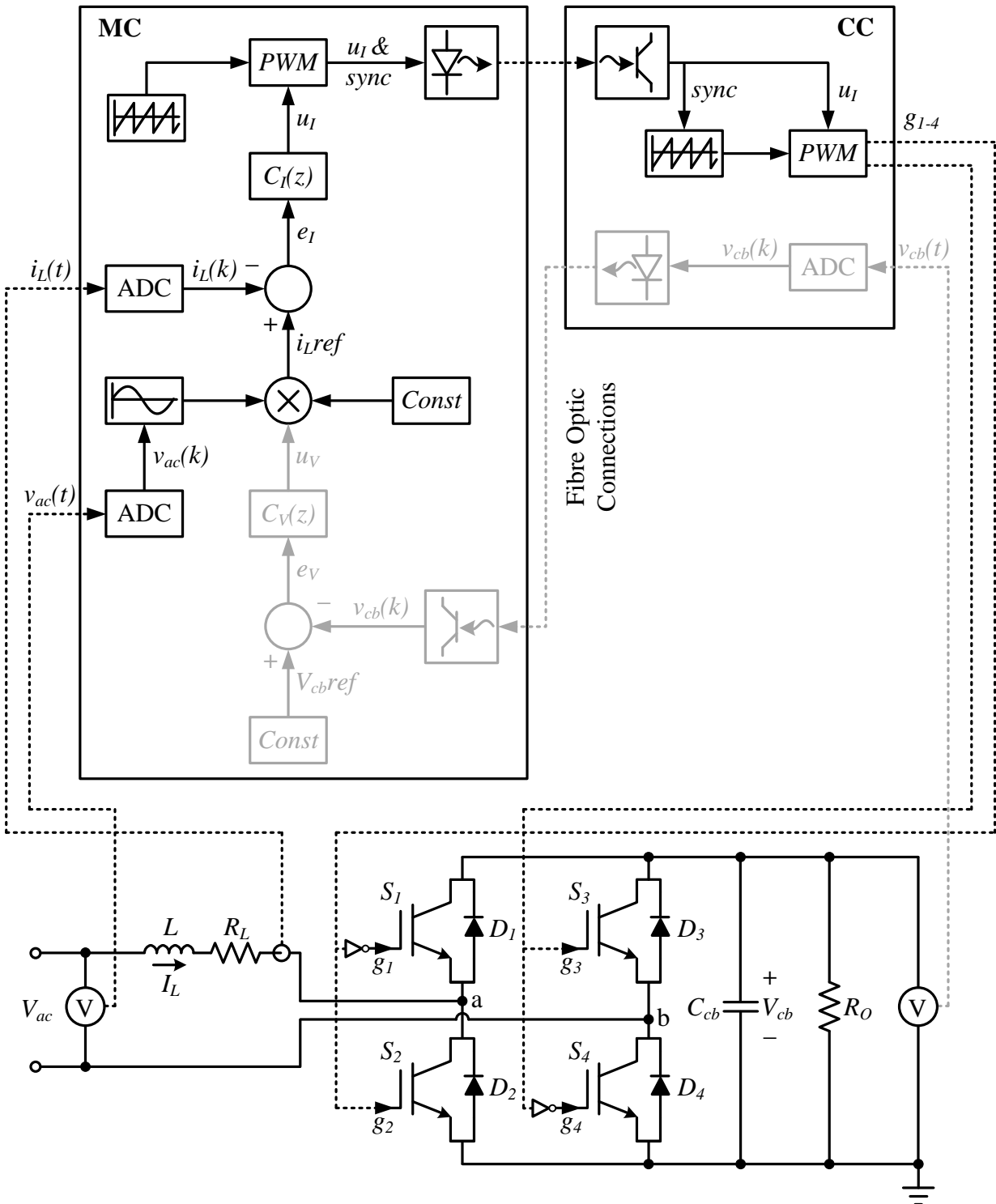
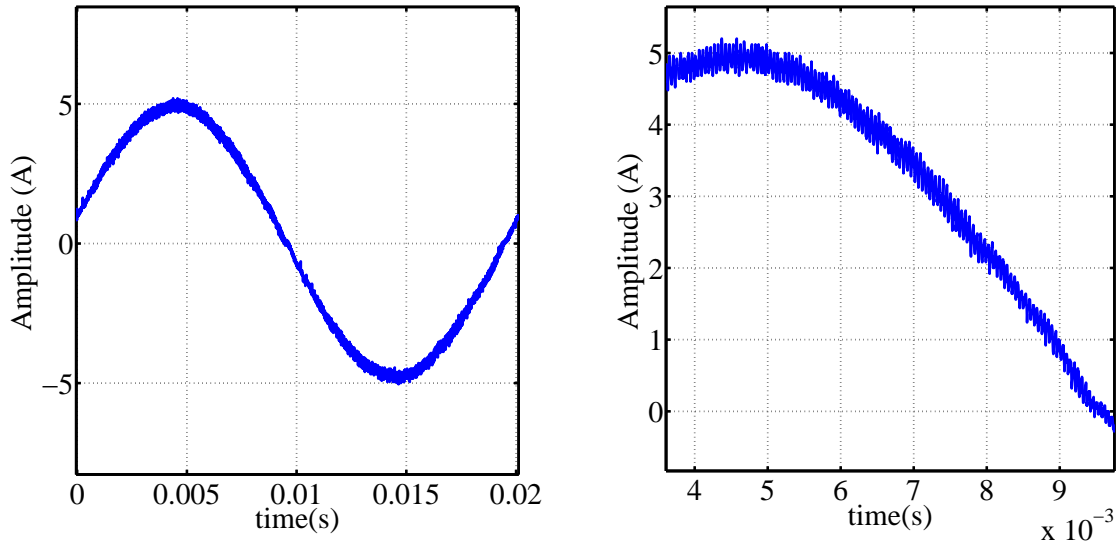
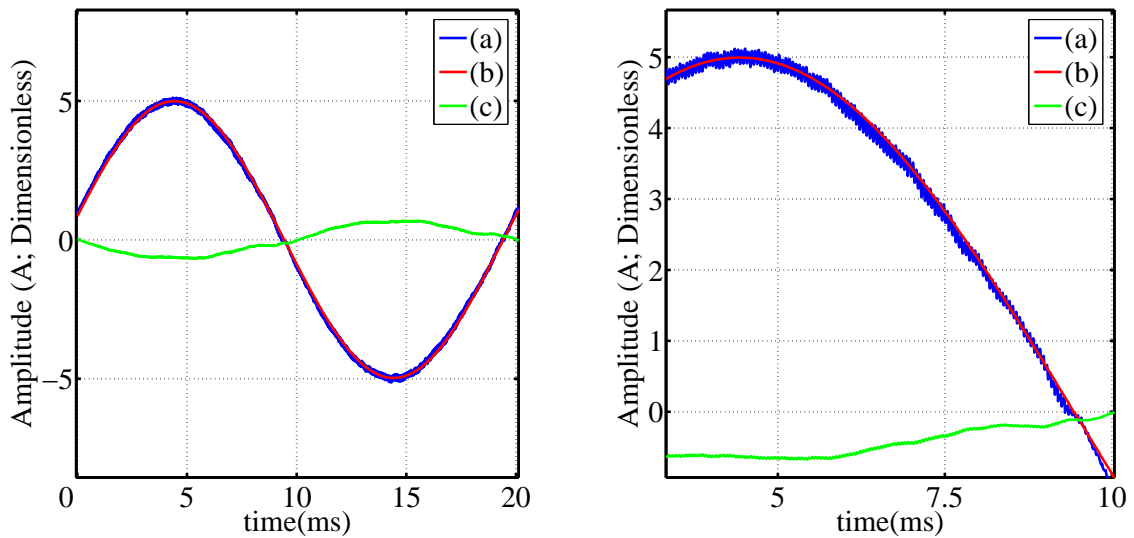


Figure 4.39: Current-Loop Test Setup

Figure 4.40 depicts the inductor-current, measured with the oscilloscope, with one cycle on the left and a detailed representation on the right. Figure 4.41 depicts the  $i_L$ ,  $i_L(ref)$  and  $u_I$  Signal-Tap measurement with one cycle on the left and a detailed representation on the right. Both measurements indicate excellent reference tracking.

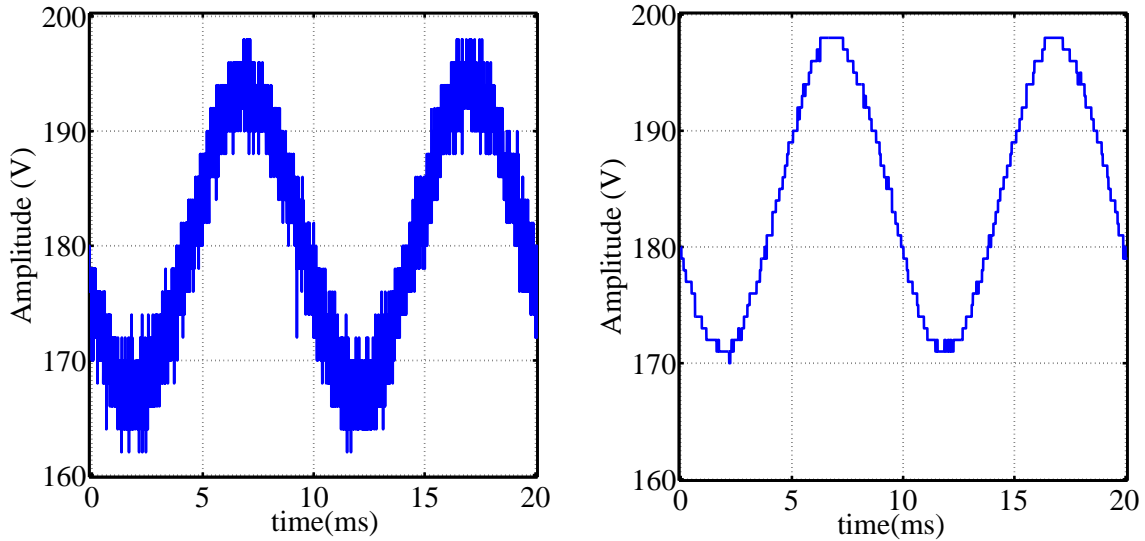


**Figure 4.40:** Oscilloscope Measurement: Inductor-Current



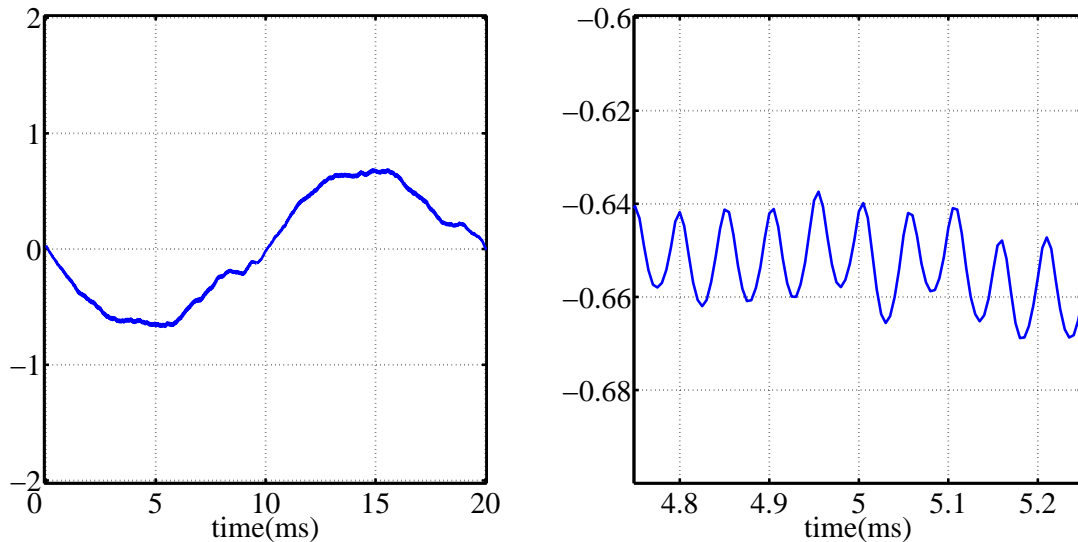
**Figure 4.41:** Signal-Tap Measurement: (a)  $i_L$ ; (b)  $i_L ref$ ; (c)  $u_I$

Figure 4.42 depicts the  $v_{cb}$  oscilloscope measurement on the left and Signal-Tap measurement on the right. The cell bus-voltage measurement is filtered by the CC, in firmware, to eliminate measurement noise. The 1<sup>st</sup> order filter is programmed with a cutoff frequency of 1 kHz. The measurement is then scaled to a resolution of 1 V to utilize the 12 bits of the communication package allocated to the AR control. This measurement handling process causes the Signal-Tap measurement to appear as the top of the oscilloscope measurement quantisation-envelope.



**Figure 4.42:** Cell Bus-Voltage

Figure 4.43 depicts one cycle of the compensator output,  $u_I$ , on the left and a detailed result on the right. The  $u_I$  signal has a sinusoidal shape with a  $180^\circ$  phase shift, compared to the current reference signal. The  $u_I$  ripple indicates the effect of the compensator on the feedback inductor-current ripple.



**Figure 4.43:** Current-Loop Compensator Output

The measurements obtained from this test are satisfactory in determining current-loop functionality. It should be noted that the measurement results are sampled representations of the physical system parameters. The oscilloscope has a limited sample rate and the Signal-Tap has a limited buffer size. This means that measurement resolution is inversely proportional to measurement duration. Test measurements showing the current-loop reaction to reference steps are discussed in Appendix B.5.2.

### 4.5.2 Active-Rectifier Test Measurements

The AR test, like the AR simulation, is a test where an AC inductor-current,  $I_L$ , is drawn from a AC input voltage,  $V_{ac}$ , to maintain a specific average bus-voltage,  $V_{cb}$ . It is aimed at verifying successful current- and voltage-loop integration as well as voltage-loop functionality in terms of its reference tracking ability. The physical test setup, as depicted in Figure 4.44, is discussed in Appendix B.5.3.

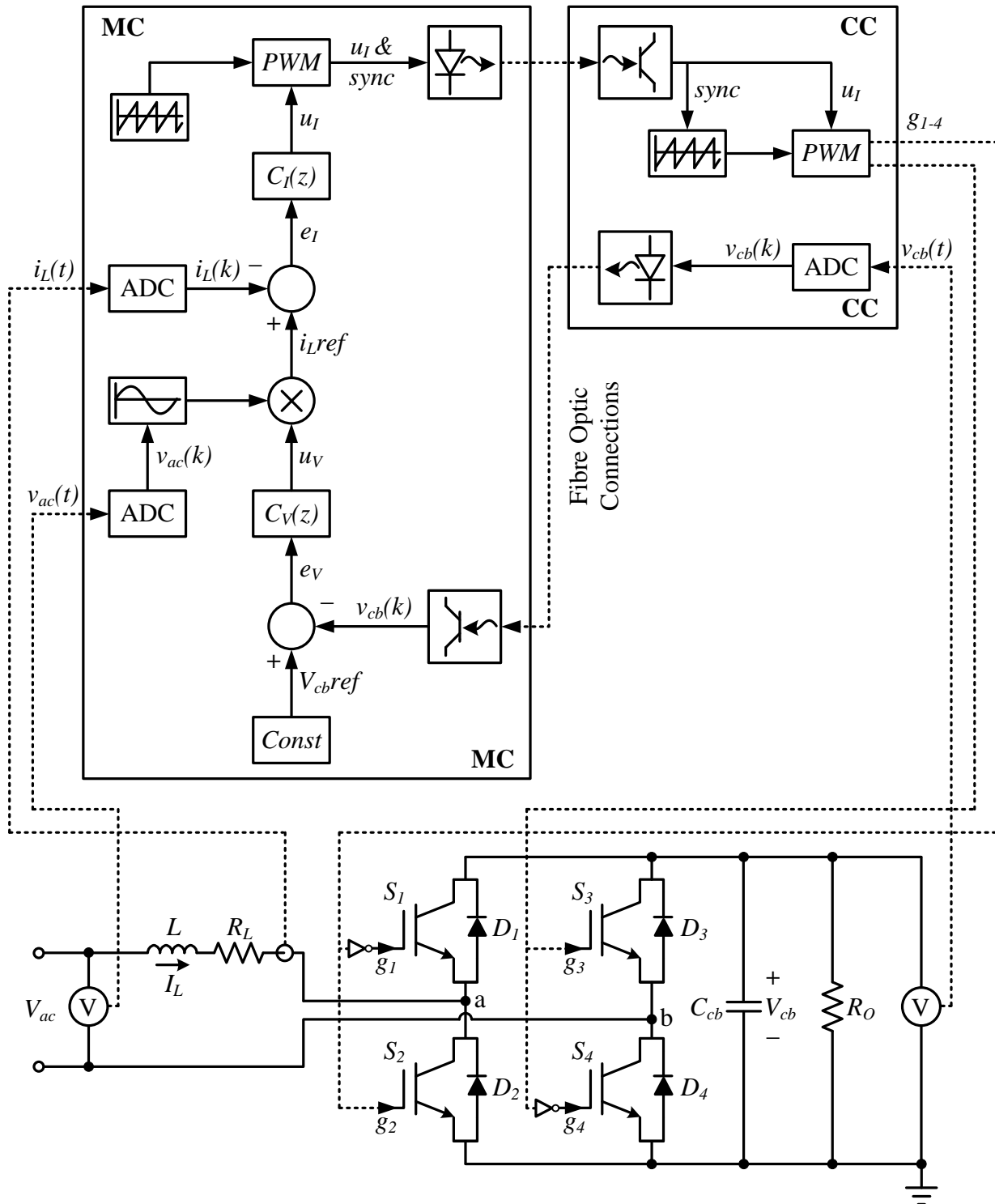
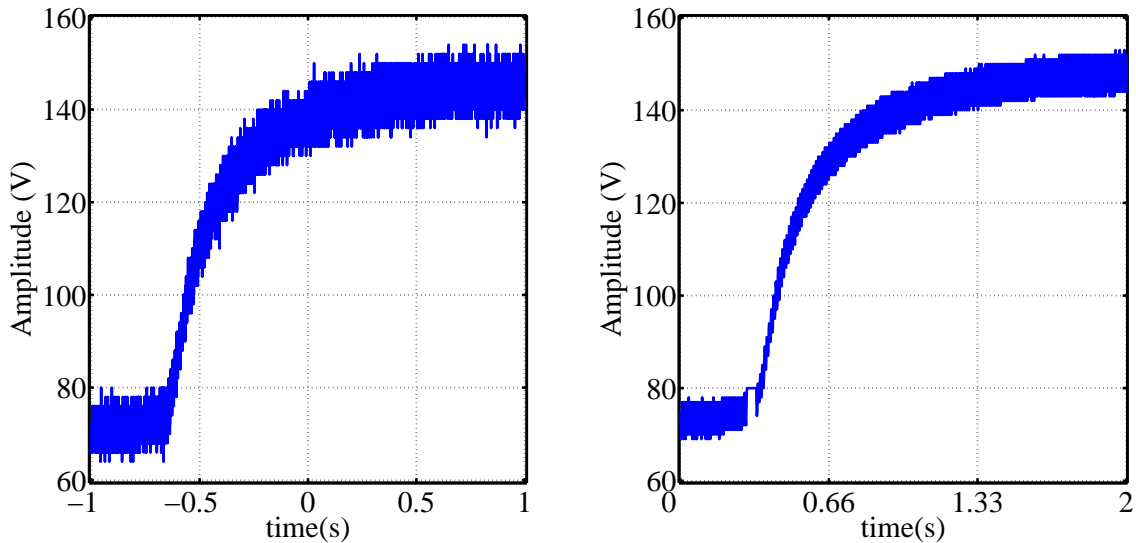


Figure 4.44: Active-Rectifier Test Setup



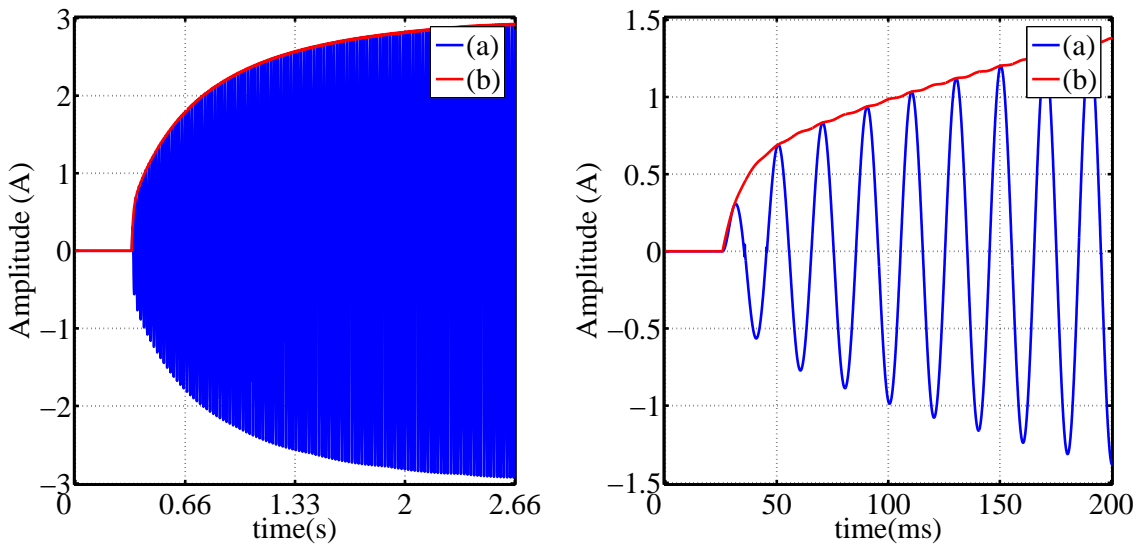
The startup sequence is followed as discussed in Section 4.4.3 with a load of  $277 \Omega$ . The operator waits until the MC enters its active state before turning up the variac by hand. The cell bus-capacitor is charged by diode currents and the AR starts up as soon as  $v_{cb}$  reaches 80 V. After the successful startup, the operator increases  $v_{ac}$  to 125 Vp to achieve a *Boost* of 1.2.

Figure 4.45 depicts the  $v_{cb}$ -transient oscilloscope measurement on the left and the Signal-Tap measurement on the right. This startup method prevents any voltage peaks, as observed in the AR simulation results. The relatively slow transient response bears witness to the low bandwidth of the voltage-loop.



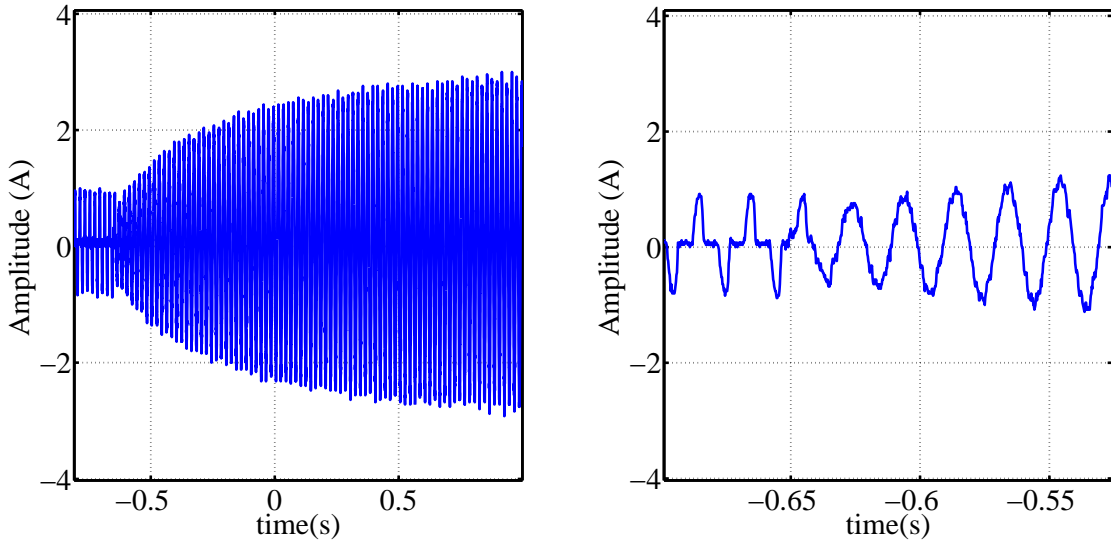
**Figure 4.45:** Cell Bus-Voltage

Figure 4.46 depicts the  $i_{Lref}$ - and  $u_V$ -transient Signal-Tap measurement on the left and a detailed measurement on the right. The  $i_{Lref}$  signal is the result of  $u_I$  multiplied with the unit sinusoid which is in phase with  $V_{ac}$ . This means that the transient response of  $i_{Lref}$  and  $i_L$  are directly related to the low voltage-loop bandwidth.

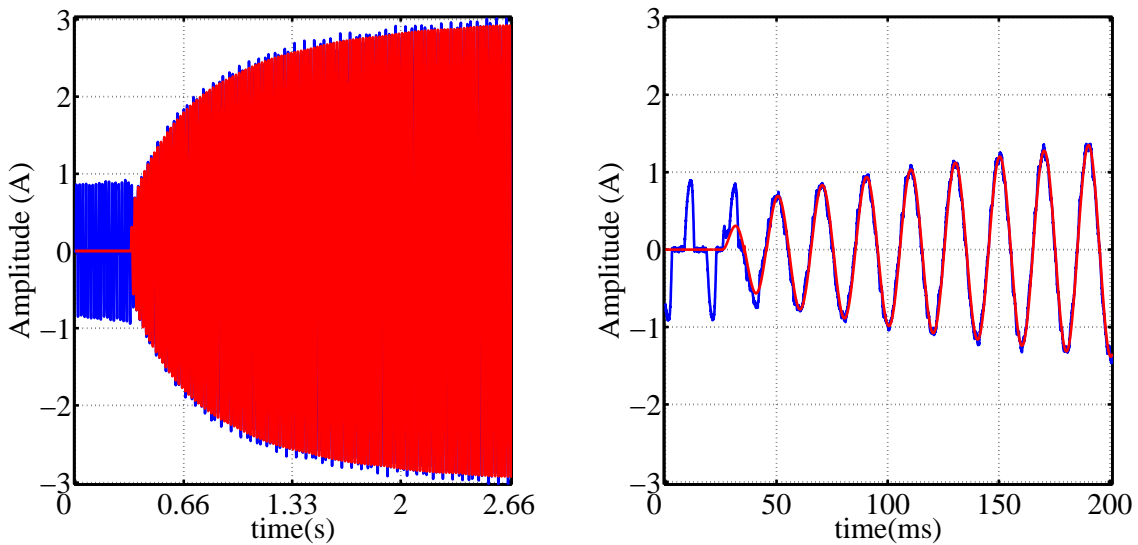


**Figure 4.46:** Signal-Tap Measurement: (a)  $i_{Lref}$ ; (b)  $u_V$

Figure 4.47 depicts the  $i_L$ -transient oscilloscope measurement on the left and a detailed measurement on the right. Figure 4.48 depicts the  $i_L$ - and  $i_{Lref}$ -transient response Signal-Tap measurement on the left and a detailed measurement on the right. Both these figures indicate the diode current-flow prior to AR startup, after which the current waveform flows directly into a sinusoidal profile. This startup method thus prevents any current peaks, as observed in the simulation results.

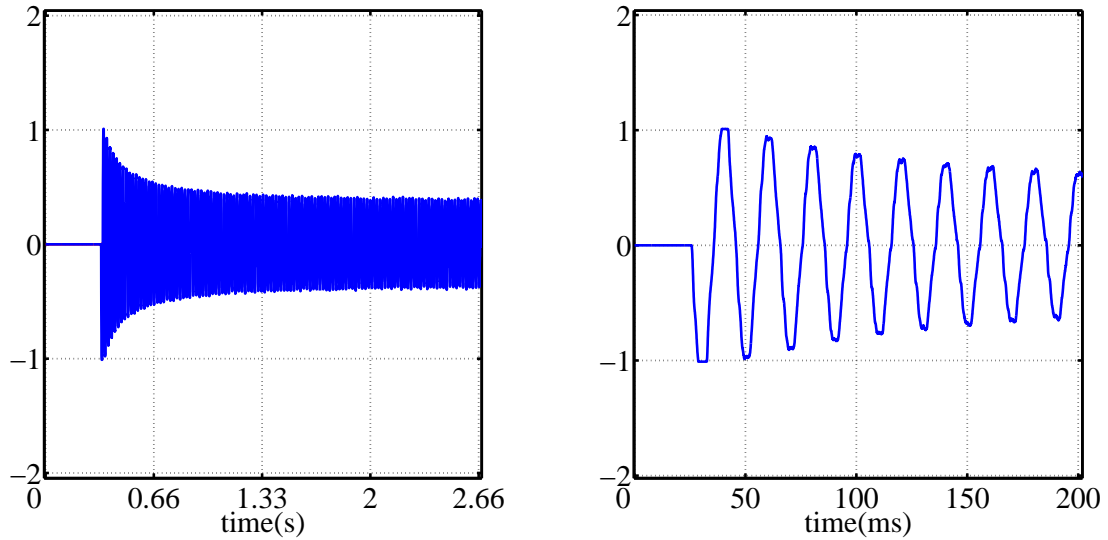


**Figure 4.47:** Oscilloscope Measurement: Inductor-Current



**Figure 4.48:** Signal-Tap Measurement: Inductor-Current and Current-Loop Reference

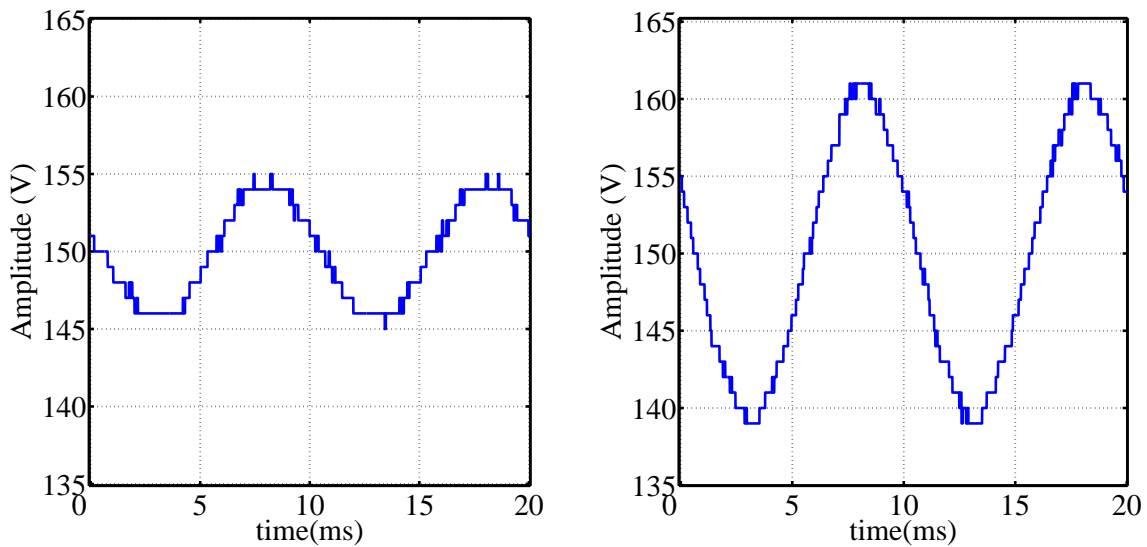
Figure 4.49 depicts the  $u_I$ -transient Signal-Tap measurement on the left and a detailed measurement on the right. The fast initial  $u_I$ -step at startup is due to the high current-loop bandwidth, while the gradual decrease in amplitude is due to the slow voltage-loop bandwidth.



**Figure 4.49:** Signal-Tap Measurement: Current-Loop Compensator Output

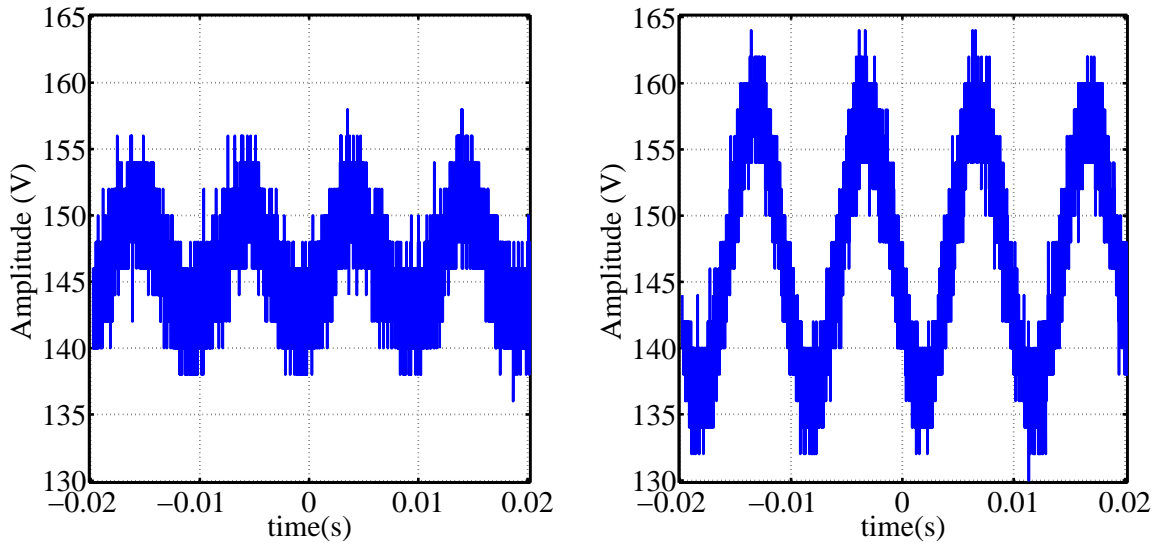
It should be noted that the  $i_L$  peak-value is dependent on the values of  $v_{ac}$  and  $v_{cb}$  respectively. At startup  $v_{cb}$  is 80 V and  $v_{ac}$  is also in this range. As  $i_L$  and  $v_{cb}$  increases, the voltage drop across the variac increases. This in turn causes  $v_{ac}$  to decrease. The  $i_L$  peak-value after startup is thus not the same as the  $i_L$  peak-values in the measurements to follow. This is because  $v_{ac}$  is increased after startup, by hand, to achieve a *Boost* of  $\pm 1.2$ .

Figure 4.50 depicts the  $v_{cb}$  Signal-Tap measurement with a 277  $\Omega$  load on the left and the measurement with a 110  $\Omega$  load on the right. It is clear that the  $v_{cb}$ -average tracks the constant 150 V voltage-loop reference in both cases. The 100 Hz ripple is also visible in both cases, however this ripple amplitude is directly proportional to the power delivered by the AR.



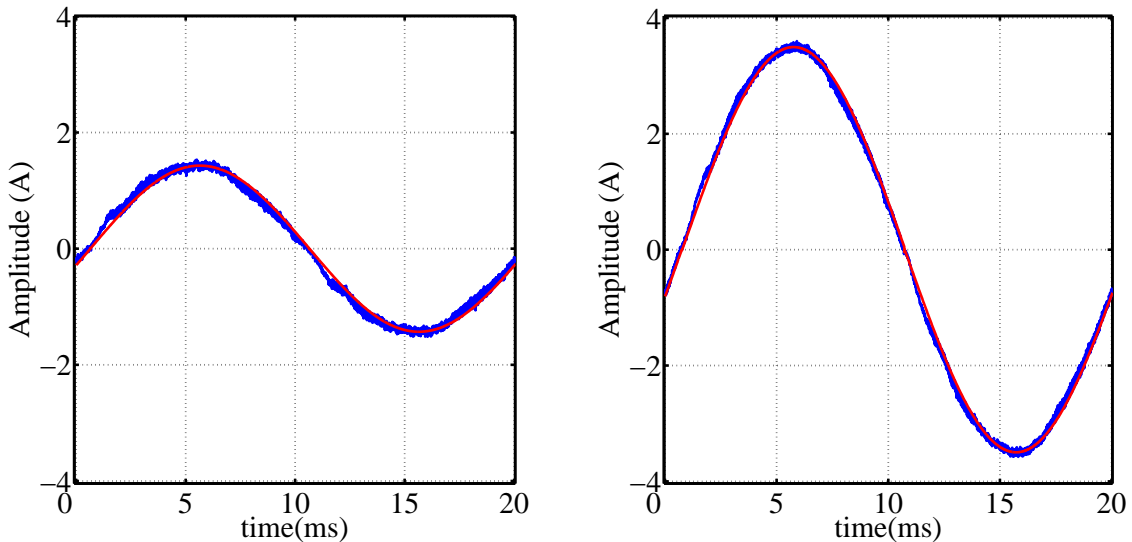
**Figure 4.50:** Signal-Tap Measurement: Cell Bus-Voltage

Figure 4.51 depicts the  $v_{cb}$  oscilloscope measurement with a 277  $\Omega$  load on the left and the measurement with a 110  $\Omega$  load on the right. The same characteristics are visible as in Figure 4.50.



**Figure 4.51:** Oscilloscope Measurement: Cell Bus-Voltage

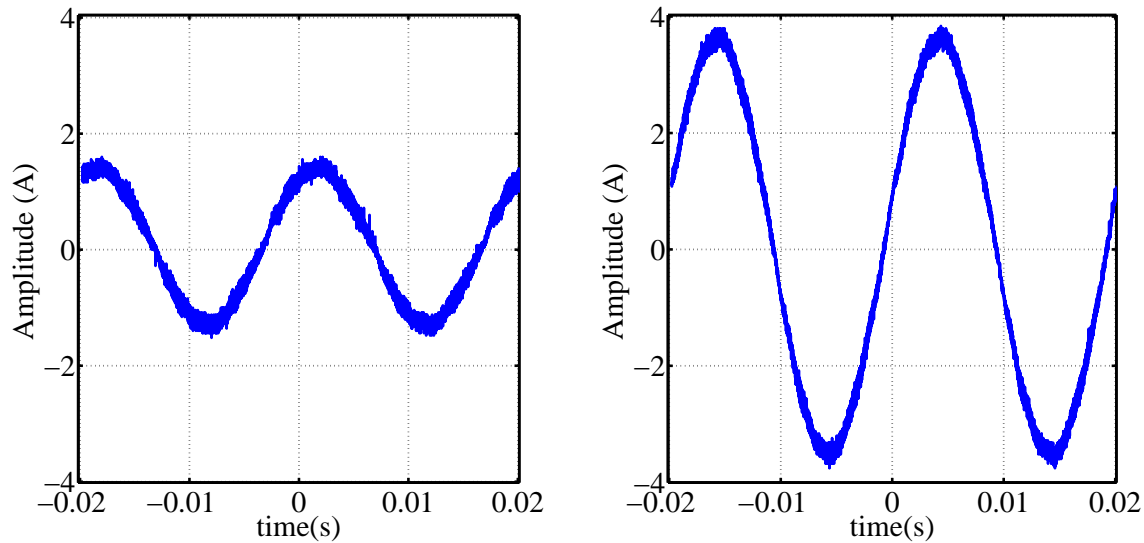
Figure 4.52 depicts the  $i_L$  and  $i_{Lref}$  Signal-Tap measurement with a  $277 \Omega$  load on the left and the measurement with a  $110 \Omega$  load on the right. The current-loop displays excellent reference tracking in both cases. It is shown however, that a large  $i_L$  amplitude results in less prominent switching ripple and thus a more sinusoidal profile.



**Figure 4.52:** Signal-Tap Measurement:  $i_L$  and  $i_{Lref}$

Figure 4.53 depicts the  $i_L$  oscilloscope measurement with a  $277 \Omega$  load on the left and the measurement with a  $110 \Omega$  load on the right. The same characteristics are visible as in Figure 4.52.

The measurements obtained are satisfactory in determining voltage-loop as well as system functionality. Measurement results showing the system reaction to load steps are discussed in Appendix B.5.4.



**Figure 4.53:** Oscilloscope Measurement: Inductor-Current

## 4.6 Conclusion

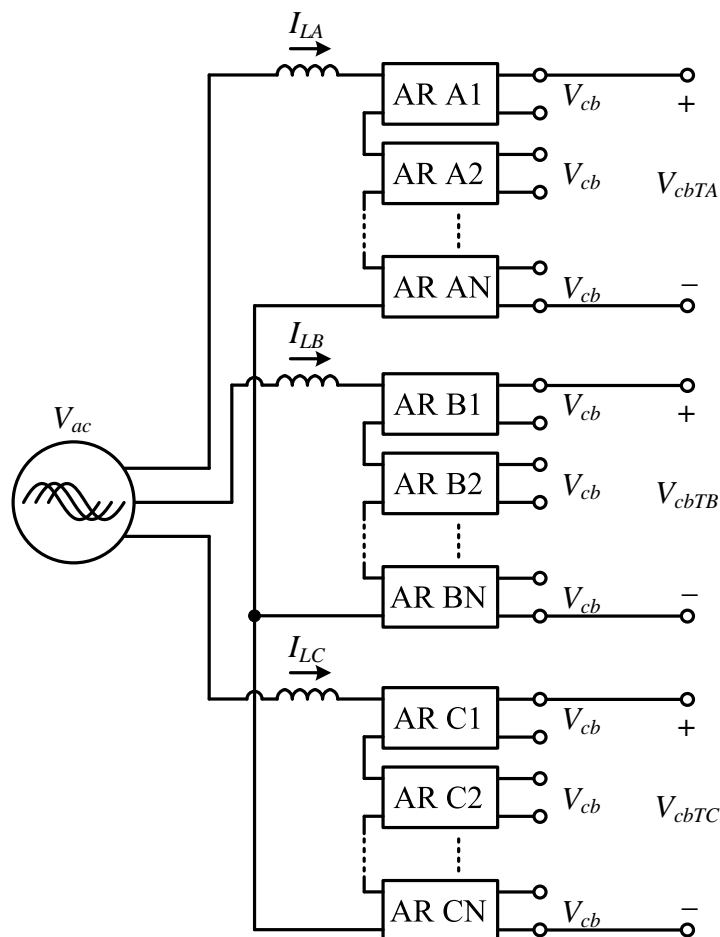
The AR role within the SST as well as its double-loop control strategy, was briefly discussed. Control design was discussed in terms of system analysis, plant modelling and compensator design. Time domain simulations were performed to verify current- and voltage-loop functionality as well as successful control and circuit integration. Detailed simulation analysis included the system response at startup, the system response to current-loop reference steps and the system response to load steps. Control implementation was discussed in terms of firmware structure. The joint control established by the MC and CC as well as the significance of different component clocks, was emphasised. Test measurements were presented to verify current- and voltage-loop functionality as well as successful control and circuit integration within a physical system. Detailed measurement analysis included the system response at startup, the system response to current-loop reference steps and the system response to load steps. The results described in this chapter show that the AR control is ready for expansion to cascaded AR control.

## Chapter 5

# Cascaded Active-Rectifier Control

### 5.1 Introduction

The Active Rectifier (AR) facilitates the input stage of the SST. The problematic aspect of this stage is the high input and output voltage levels. To overcome the HV hurdle, the AR discussed in Chapter 4 is used as a building block to construct the Cascaded Active-Rectifier (CAR). The input line to neutral voltage is split between  $N$  AR-inputs and the output DC bus-voltage is split between  $N$  AR-buses. This cascaded multilevel-converter topology is tripled to facilitate a 3-phase input, as shown in Figure 5.1.



**Figure 5.1:** Three-Phase Cascaded Active-Rectifier Topology

The AR control scheme can be expanded to control a phase with  $N$  cascaded ARs due the modularity of this converter topology. As shown in Figure 5.2, the double loop control scheme is maintained with the control objectives remaining unchanged. The control-scheme alterations include the following: The voltage-loop constant reference is changed to the desired total cell bus-voltage,  $V_{cbTref}$ , and the voltage-loop feedback is changed to the total cell bus-voltage,  $v_{cbT}$ . The voltage- and current-loop compensators,  $C_V$  and  $C_I$ , are redesigned due to the the expanded voltage- and current-loop plants,  $G_V$  and  $G_I$ , respectively. The number of PWM carriers are increased to  $2 \times N$  and the carrier pairs are interleaved. Each carrier-pair results in a AR duty-cycle,  $d$ , which increases the number of duty cycles to  $N$ . The plants,  $G_I$  and  $G_V$ , are re-evaluated to obtain time averaged models of the CAR.

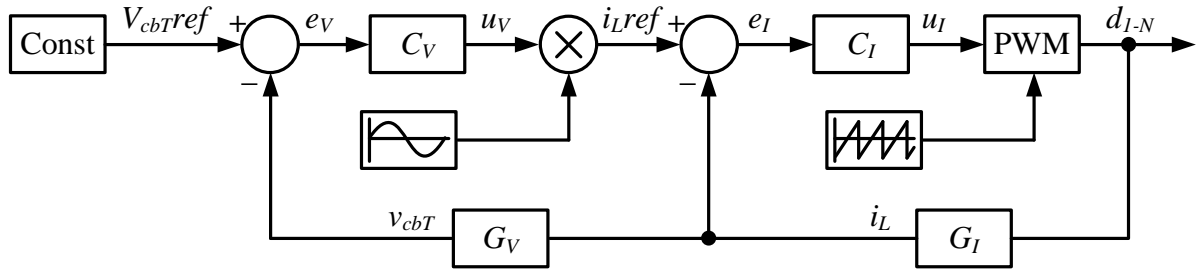


Figure 5.2: Double-Loop Cascaded Active-Rectifier Control Scheme

In this chapter the methodology followed in designing and implementing the expanded AR control system for a single-phase CAR is thoroughly described. Time-domain simulation results and test measurements are presented and explained with emphasis on multilevel characteristics and natural cell bus-voltage balancing.

## 5.2 Control Design

The CAR control-design process involves expanding the AR control system to facilitate  $N$  ARs. The fundamentals regarding the characteristics of the controlled- and control system are thus already established.

With regard to the expanded controlled system characteristics: Each AR is identical to the AR discussed in Chapter 4, consisting of a full-bridge converter and a bus-capacitor,  $C_{cb}$ . The resistive load,  $R_O$ , is added to the circuit to imitate power transfer from the input-stage to the isolation-stage. Each full-bridge converter consists of four switches,  $S_1 - S_4$ , each realised with an Insulated Gate Bipolar Transistor (IGBT) and controlled through its respective gate-signal,  $g_1 - g_4$ . The AR stack includes a single inductor,  $L$ , and the inductor resistance,  $R_L$ , as shown in Figure 5.3.

With regard to the expanded control system characteristics: The hardware available for control implementation includes the same MC utilized in the AR control system. The number of CC is however increased with a factor  $N$ .

In the remainder of this section the CAR control design is described in terms of the two control loops, as shown in Figure 5.2, starting with the inner current-loop, and followed by the outer voltage-loop. Each loop design entails, among other steps, expanding the respective plants,  $G_I$  and  $G_V$ , and redesigning the respective compensators,  $C_I$  and  $C_V$ .

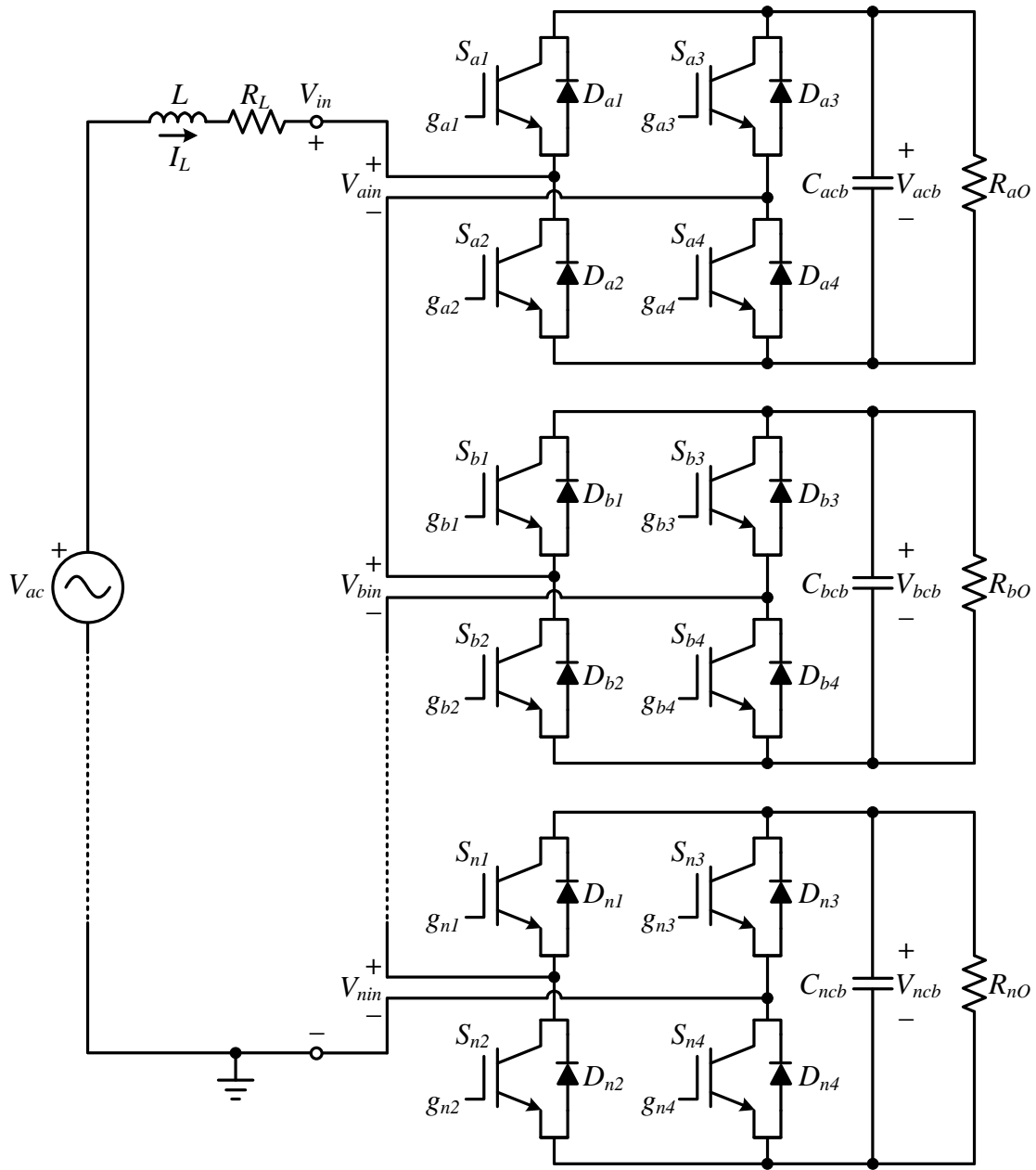


Figure 5.3: Cascaded Active-Rectifier Circuit Diagram

### 5.2.1 Interleaved Pulse Width Modulator Design

The PWM design choices, as discussed in Section 4.2.1, include which switching scheme to use, which carrier waveform to use and the implemented switching frequency. There is an added design choice which results in how the duty cycle of each AR will be related to each other.

Unipolar-voltage switching remains the chosen scheme and sawtooth carriers remain the chosen carrier waveform. The switching frequency,  $f_s$ , is however increased to 15 kHz where:

$$f_s = \frac{1}{T_s} \tag{5.2.1}$$

The reason for this increase is discussed in Section 6.3.1. This leads to an effective AR switching frequency of:



$$f_{ar} = 2 \times f_s = 30 \text{ kHz} \quad (5.2.2)$$

and switching period:

$$T_{ar} = \frac{1}{f_{ar}} = 16.667 \mu\text{s} \quad (5.2.3)$$

The respective AR duty cycles are related in an interleaved fashion. This is to facilitate natural cell bus-voltage balancing, as discussed in Section 2.2. The sawtooth carriers of a single AR are defined as:

$$\begin{aligned} \text{Carrier}_1 &= \text{sawtooth}(2\pi f_s t) \\ \text{Carrier}_2 &= \text{sawtooth}(2\pi f_s t - \pi) \end{aligned} \quad (5.2.4)$$

Interleaved switching leads to the CAR carrier definition:

$$\begin{aligned} \text{Carrier}_{i1} &= \text{sawtooth}\left(2\pi f_s t - \frac{i}{N} \cdot \pi\right) \\ \text{Carrier}_{i2} &= \text{sawtooth}\left(2\pi f_s t - \left(1 + \frac{i}{N}\right) \cdot \pi\right) \end{aligned} \quad (5.2.5)$$

with  $N$  defined as the number of ARs in the stack and  $i$  defined as the number of the specific AR within the stack. This number is determined by counting the ARs starting from zero, from the positive terminal of  $V_{ac}$ . The interleaved carriers of a two AR stack are depicted in Figure 5.4.

It is clear that interleaved switching increases the effective CAR switching frequency by a factor  $N$ :

$$f_{car} = N \times f_{ar} = 2N \times f_s \quad (5.2.6)$$

Another outcome of interleaved switching is the decreased voltage drop across the inductor,  $L$ . This voltage drop is dependent on the number of voltage levels within the total input switched-voltage,  $V_{in}$ . The number of voltage levels is defined as:

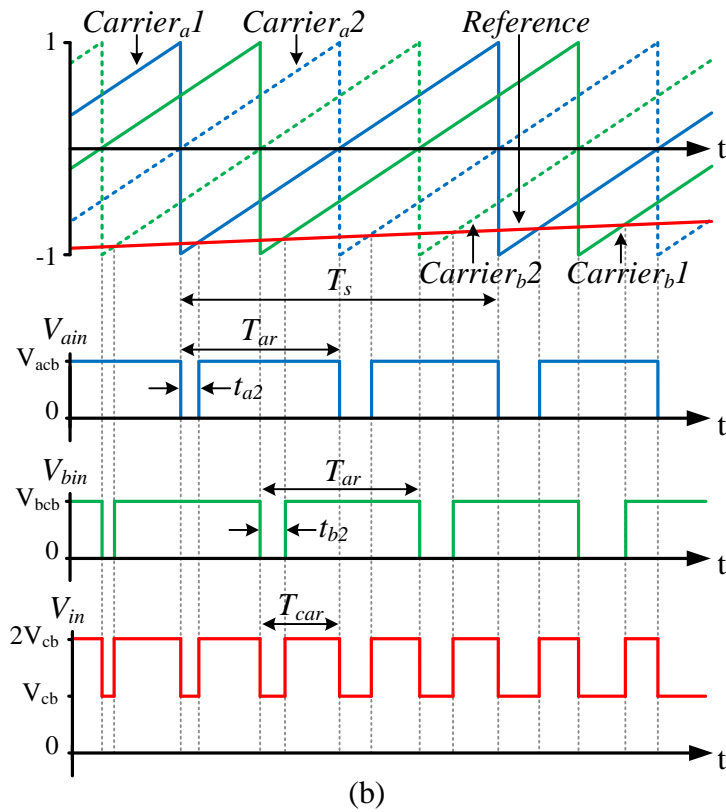
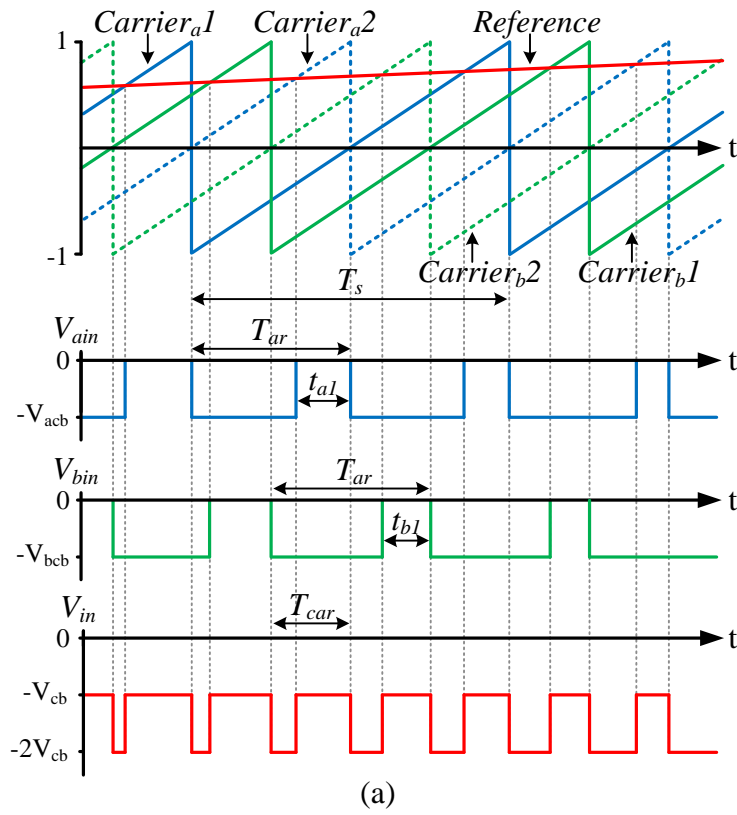
$$N_{Vin} = 2N + 1 \quad (5.2.7)$$

The switching duty ratio of a two AR stack is defines as:

$$\begin{aligned} d_a &= \frac{t_{a1}}{T_{ar}} & \text{for: Reference} > 0 \\ d_b &= \frac{t_{b1}}{T_{ar}} \end{aligned} \quad (5.2.8)$$

$$\begin{aligned} d_a &= \frac{t_{a2}}{T_{ar}} & \text{for: Reference} < 0 \\ d_b &= \frac{t_{b2}}{T_{ar}} \end{aligned} \quad (5.2.9)$$

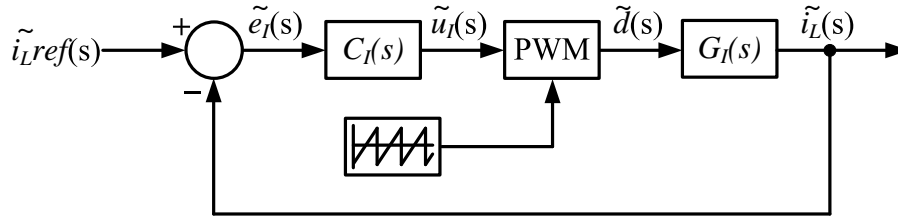
with  $t_{a1}$ ,  $t_{a2}$ ,  $t_{b1}$  and  $t_{b2}$  defined in Figure 5.4.



**Figure 5.4:** Two AR Interleaved Unipolar PWM: (a) Positive Reference; (b) Negative Reference

### 5.2.2 Current-Loop Plant Expansion

The current loop can be analysed separately from the voltage loop, as with a single AR. This current loop is shown in Figure 5.5, with the small AC signals denoted by " $\sim$ ".

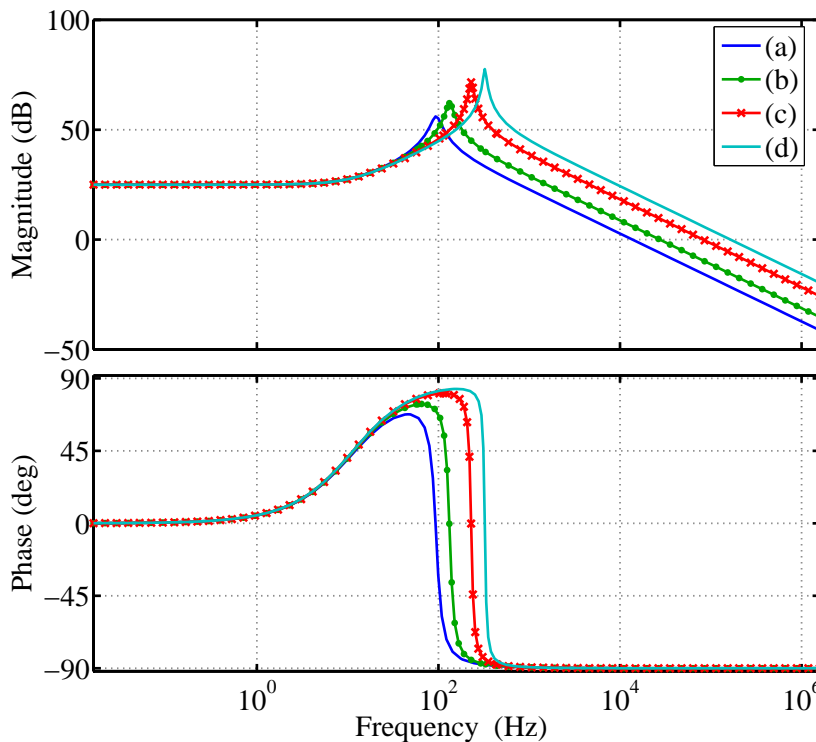


**Figure 5.5:** Cascaded Active-Rectifier Inner Current-Loop

A state-space averaging technique is used in Section 4.2.3 to obtain the AC small-signal linear model of the plant represented by Eq. 4.2.28. This model represents the inductor-current response to small duty cycle variations of a single AR. The model is expanded by time averaging the plant observed by the input inductor of an  $N$  AR stack. Appendix C.1 results in:

$$G_I(s) = \frac{NV_{cb}}{L} \times \frac{s + \frac{2}{R_0C_{cb}}}{s^2 + \left(\frac{R_L}{L} + \frac{1}{R_0C_{cb}}\right)s + \frac{R_L}{R_0LC_{cb}} + \frac{N(1-D)^2}{LC_{cb}}} \quad (5.2.10)$$

From Figure 5.6, it is clear that adding ARs to the stack increases the plant gain with a factor  $N$  and moves the complex pole-pair to a higher frequency. Moving the complex pole pair only affects the frequencies below its position with the low-frequency gain decreased with a factor  $N$ . The low-frequency gain is thus left unchanged and an increased bandwidth is observed.



**Figure 5.6:** Frequency Response of  $G_I(s)$ : (a)  $N = 1$ ; (b)  $N = 2$ ; (c)  $N = 6$ ; (d)  $N = 12$

### 5.2.3 Current-Loop Compensator Design

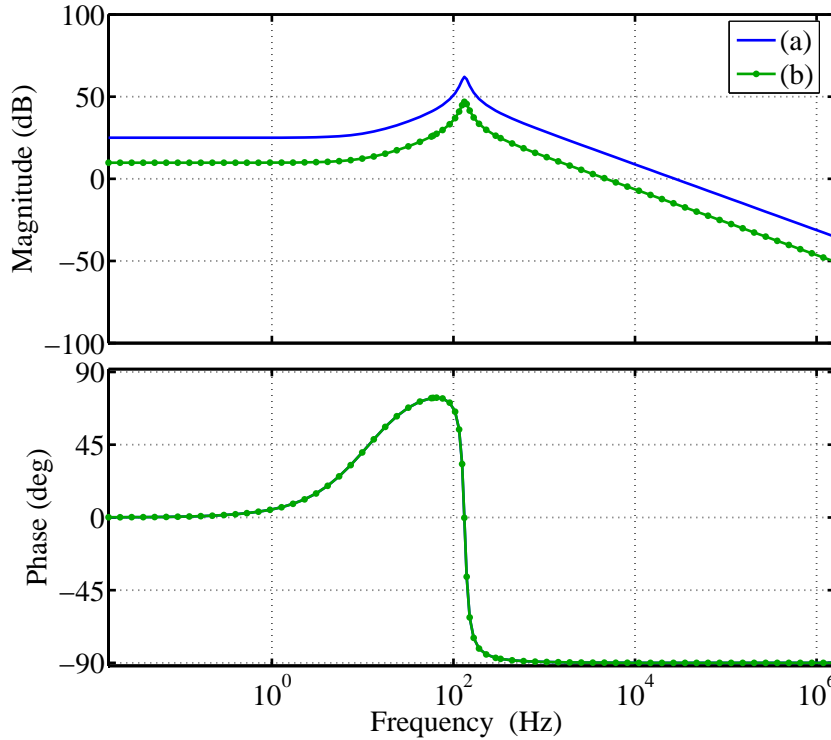
Average current mode control is implemented within the CAR inner current-loop, as with the single AR current-loop. This loop requires a large bandwidth to achieve optimum reference tracking, as large as possible without causing loop instability. The current-loop compensator design also starts by determining the optimum compensator gain with Eq. 4.2.32. A two AR stack with a switching frequency,  $f_s$ , defined in Section 5.2.1, results in the compensator optimum gain of:

$$G_{C_{opt}} = \frac{V_s \cdot f_s \cdot L}{V_{cbT}} = 0.174 \quad \text{at } f_s \quad (5.2.11)$$

with  $V_s$  being the carrier peak-to-peak amplitude. From Eq. 5.2.10, the current-loop plant transfer function of a two AR stack is quantified as:

$$G_I(s) = 1.724 \times 10^4 \times \frac{s + 71.747}{s^2 + 135.9s + 6.98 \times 10^5} \quad (5.2.12)$$

To determine the maximum crossover frequency, the current-loop plant transfer-function is multiplied with this optimum compensator gain. The result is analysed using its frequency response as showed in Figure 5.7.



**Figure 5.7:** Frequency Response of: (a)  $G_I(s)$ ; (b)  $G_{C_{opt}} \cdot G_{CI}$ .

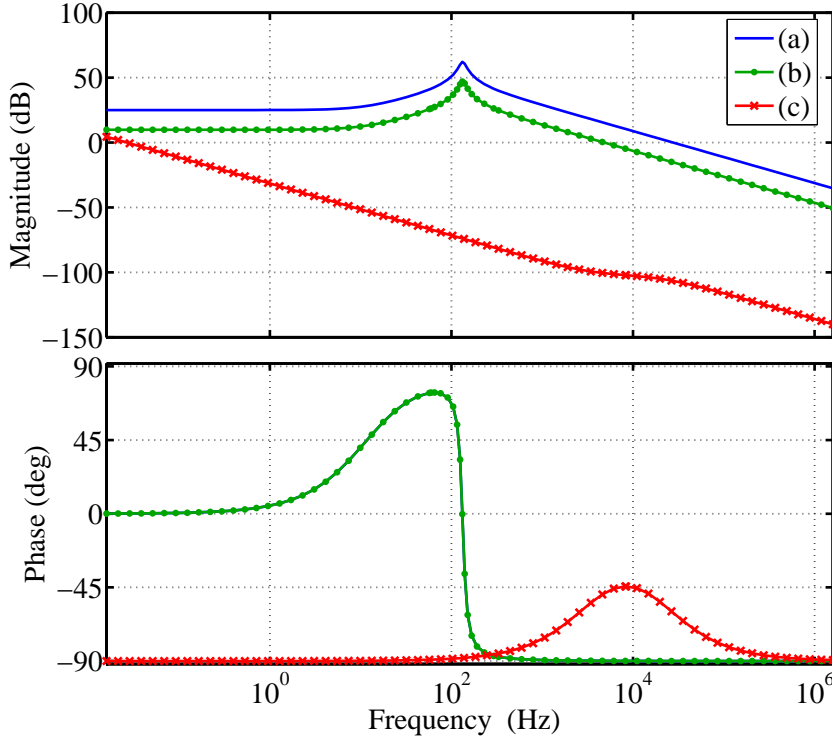
The maximum crossover frequency is thus:

$$f_c = 6747 \text{ Hz} \approx 6.75 \text{ kHz} \quad (5.2.13)$$

The compensator design continues by placing a pole and a zero together with an integrator. The zero is placed at  $\frac{1}{2} \cdot f_c$  providing a boost at low frequencies and to increase the open-loop

phase-margin. The pole is placed at  $3 \cdot f_c$  to suppress noise spikes. This pole, zero and integrator placement results in the preliminary compensator, as shown in Figure 5.8:

$$C_{Ipre}(s) = \frac{s + (\frac{1}{2} \cdot f_c \cdot 2\pi)}{s(s + (3 \cdot f_c \cdot 2\pi))} \approx \frac{s + 2,15 \times 10^4}{s(s + 1,29 \times 10^5)} \quad (5.2.14)$$



**Figure 5.8:** Frequency Response of: (a)  $G_I(s)$ ; (b)  $G_{Ctopt} \cdot G_I(s)$ ; (c)  $C_{Ipre}(s)$ .

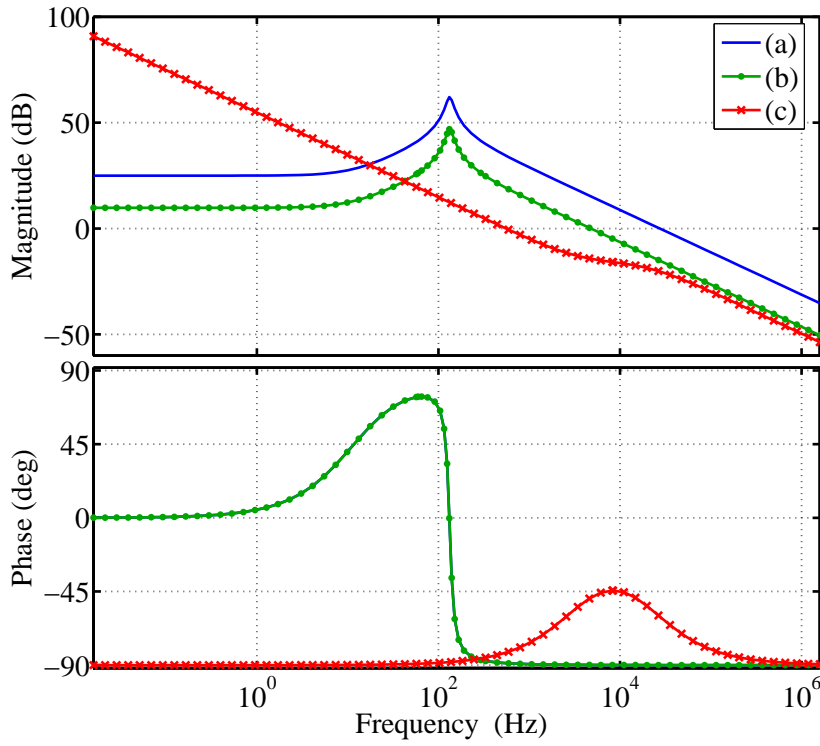
The preliminary-compensator gain is analysed to determine the additional gain required to achieve the desired closed-loop bandwidth. As shown in Figure 5.9, the compensator is thus given as:

$$C_I(s) = 2,075 \times 10^4 \cdot \frac{s + 2,15 \times 10^4}{s(s + 1,29 \times 10^5)} \quad (5.2.15)$$

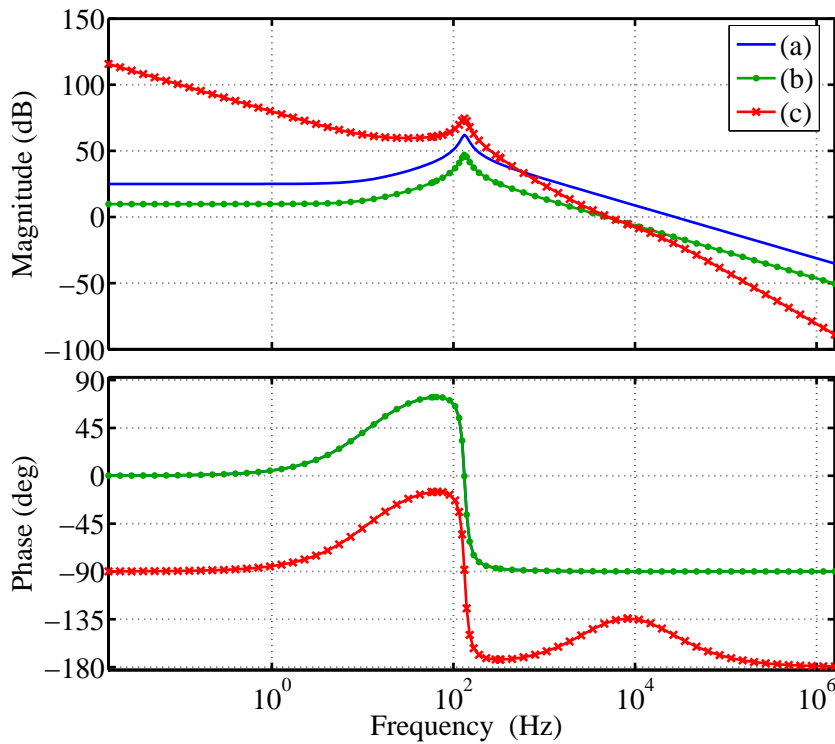
Figure 5.10 depicts the open-loop frequency response and Figure 5.11 depicts the closed-loop frequency response of the current-loop. The resulting current-loop bandwidth is:

$$BW_I = 4.9 \text{ kHz} \quad (5.2.16)$$

The effect of the ever changing AR duty-cycle variable,  $D$ , on the open current-loop frequency response is discussed in Appendix C.2. The closed current-loop is also analysed in this appendix.



**Figure 5.9:** Frequency Response of: (a)  $G_I(s)$ ; (b)  $G_{Clopt} \cdot G_I(s)$ ; (c)  $C_I(s)$ .



**Figure 5.10:** Frequency Response of: (a)  $G_I(s)$ ; (b)  $G_{Clopt} \cdot G_I(s)$ ; (c)  $C_I(s) \cdot G_I(s)$ .

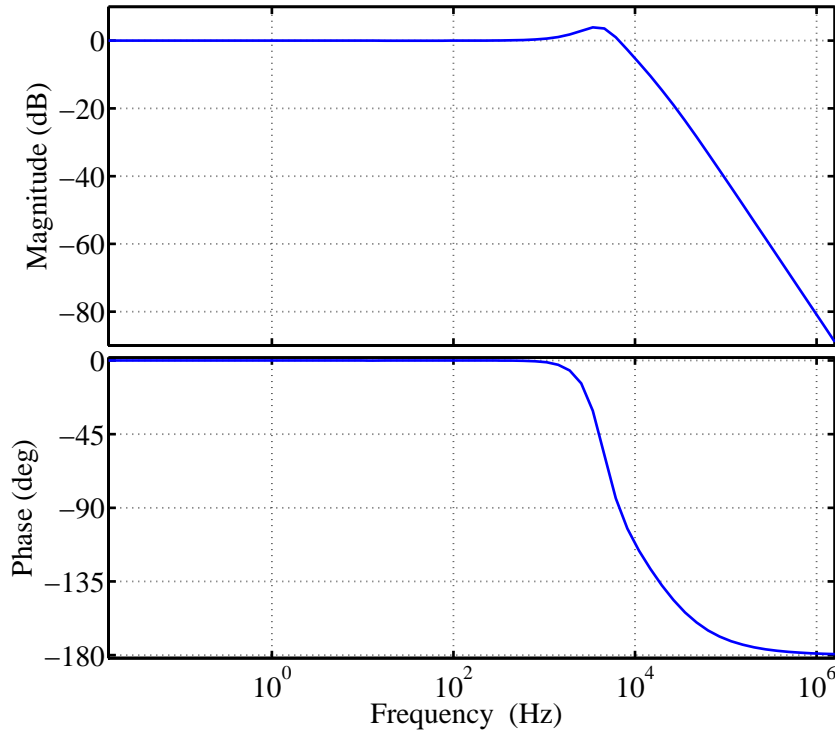


Figure 5.11: Closed Current-Loop Frequency Response

### 5.2.4 Voltage-Loop Plant Expansion

The voltage loop can be analysed separately from the current loop. Separating the voltage loop from the double-loop control scheme is not as straight forward as doing so with the current loop. The process is discussed in Section 4.2.5 for a single AR. The resulting voltage loop is expanded, as depicted in Figure 5.12, to accommodate an  $N$  AR stack.

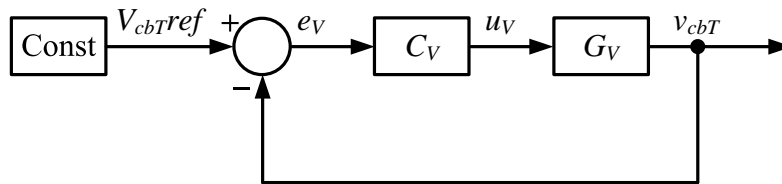


Figure 5.12: Cascaded Active-Rectifier Voltage Loop

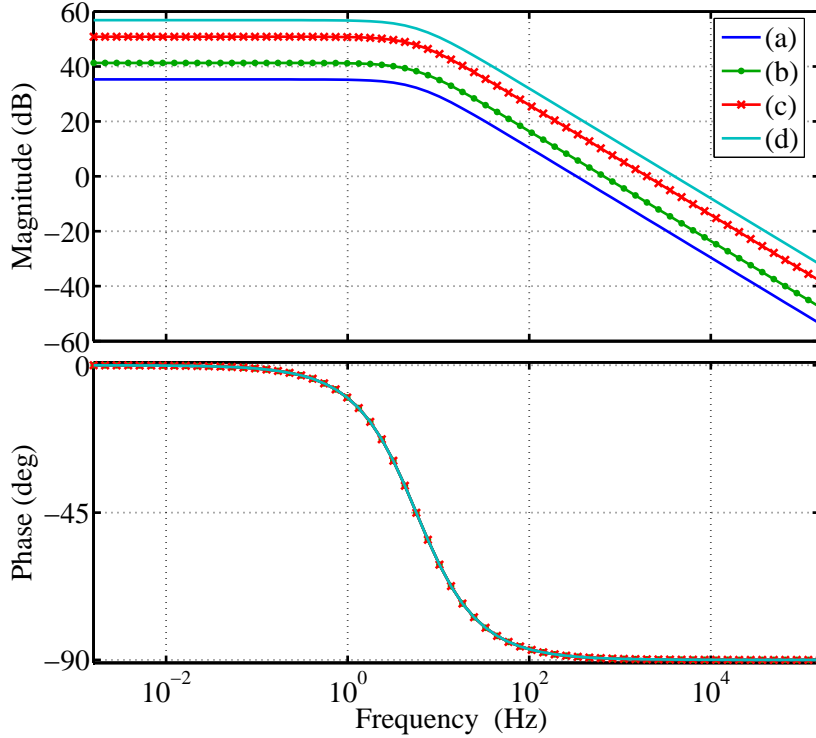
The voltage-loop plant model for a single AR is derived in Section 4.2.5 as:

$$G_{VAR}(s) = \frac{V_{cb}}{I_{Lp}} = \frac{1-D}{\sqrt{2}} \cdot \frac{\frac{1}{C_{cb}}}{s + \frac{1}{C_{cb}R_O}} \quad (5.2.17)$$

This model represents the bus-voltage response to peak input-current variations. The model is expanded by altering the symbolic parameters as shown in Table C.1 for an  $N$  AR stack. The same model expansion technique is thus used as in Appendix C.1 for the current-loop plant model. The  $N$  AR stack voltage-loop plant model is given as:

$$G_V(s) = \frac{1-D}{\sqrt{2}} \cdot \frac{\frac{N}{C_{cb}}}{s + \frac{1}{C_{cb}R_O}} \tag{5.2.18}$$

It is clear that the only alteration to the voltage-loop plant model is a gain increase with a factor  $N$ . The frequency-response alteration is thus depicted in Figure 5.13 with increased gain throughout the spectrum resulting in an increased bandwidth.



**Figure 5.13:** Frequency Response of  $G_V(s)$ : (a)  $N = 1$ ; (b)  $N = 2$ ; (c)  $N = 6$ ; (d)  $N = 12$

### 5.2.5 Voltage-Loop Compensator Design

The outer voltage-loop controls the average total cell bus-voltage value. The value is adjusted by adjusting the peak input inductor-current value, while maintaining its sinusoidal profile. This is a 50 Hz current profile which causes a 100 Hz bus-voltage ripple around the desired average value of each AR in the stack. This is expected from a full-bridge rectifier. The voltage-loop should thus ignore the 100 Hz ripple to avoid distorting the controlled input inductor-current.

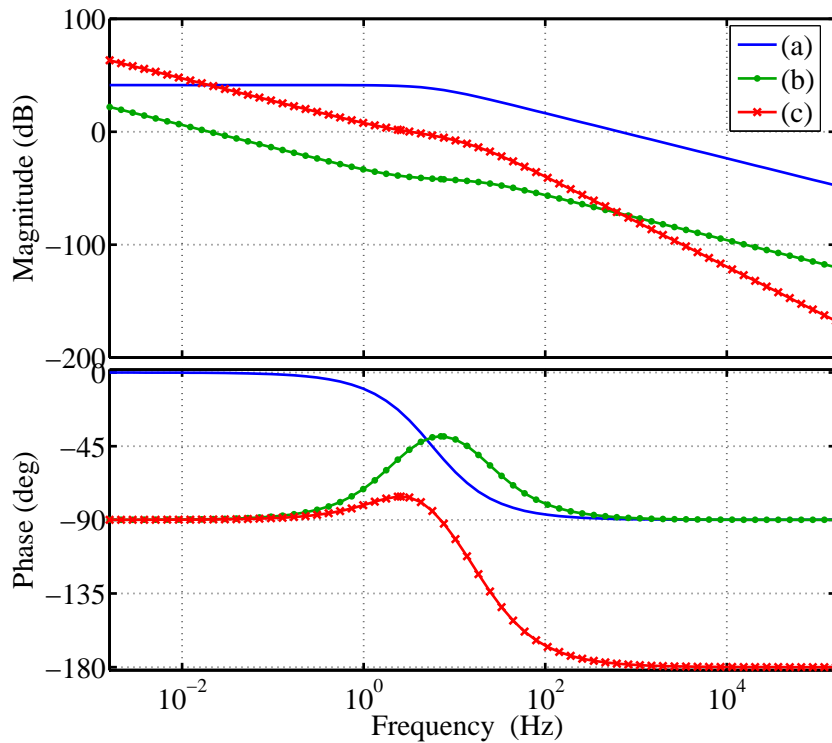
The voltage-loop compensator designed for the single AR can be used in the CAR voltage-loop. This is because the same objectives are set for both voltage-loops. The CAR voltage-loop plant has a larger gain value, of factor  $N$ , compared to the AR voltage-loop plant. The CAR voltage-loop compensator is thus divided with a factor  $N$  to achieve the same voltage-loop frequency response. A slight increase in bandwidth is however required for reasons discussed in Section 6.2.2. The compensator gain is thus increased with a factor 2 resulting in the voltage-loop compensator transfer-function:

$$C_V(s) = \frac{2}{N} \cdot \frac{s + (\frac{1}{8}20 \cdot 2\pi)}{s(s + (20 \cdot 2\pi))} \tag{5.2.19}$$



This compensator results in a frequency response independent of  $N$  and thus independent of the number of ARs added to the stack. Figure 5.14 shows the frequency response of the voltage-loop plant, compensator and open-loop system for a two AR stack. The voltage-loop compensator transfer-function for a two AR stack is quantified as:

$$C_V(s) = \frac{s + 15.71}{s(s + 125.7)} \quad (5.2.20)$$



**Figure 5.14:** Frequency Response of: (a)  $G_V(s)$ ; (b)  $C_V(s)$ ; (c)  $C_V(s) \cdot G_V(s)$

Figure 5.15 shows the closed-voltage-loop frequency response, resulting in a voltage-loop bandwidth of:

$$BW_V = 2.25 \text{ Hz} \quad (5.2.21)$$

The open voltage-loop response as well as the closed voltage-loop response are further analysed in Appendix C.3. Due to the lack of stringent voltage-loop specifications, the designed compensator,  $C_V$ , is subject to modification. Findings during the testing phase might require changes in terms of bandwidth and transient response. Any such modifications will be noted.

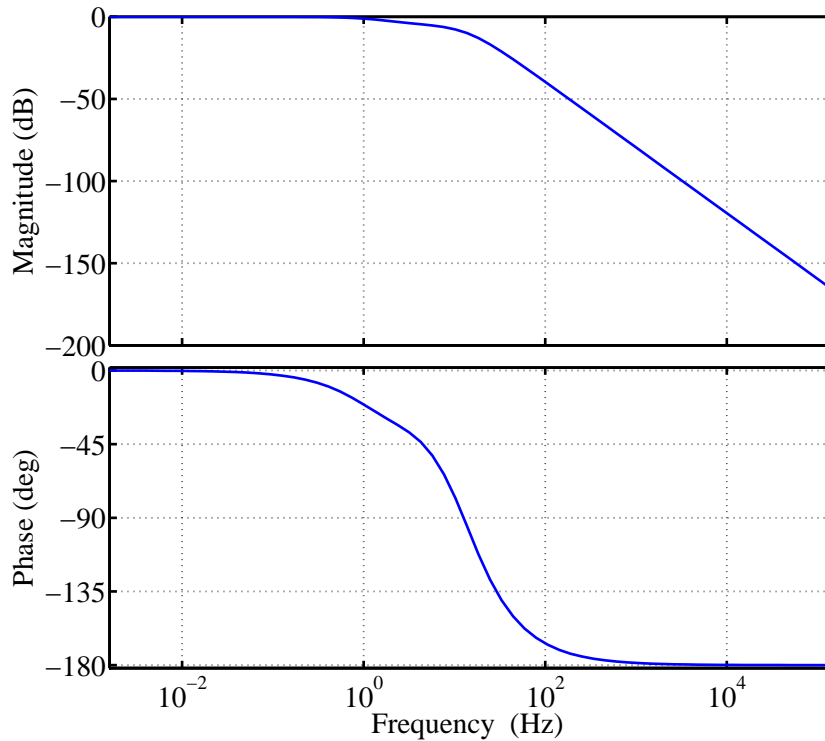


Figure 5.15: Closed-Voltage-Loop Frequency Response

## 5.3 Control Simulation

Time domain simulations are performed to verify the functionality of the designed Current- and Voltage-loop. The compensators are implemented as time-domain transfer-function blocks, the plant is implemented as an electrical circuit and the control-loop feedback is implemented as circuit measurements. The compensators are designed in the continuous time domain and simulated with very small time steps. This method is suitable because each implemented control loop is clocked much faster than its respective bandwidth. For example, the current-loop is clocked at 10MHz, as mentioned in Section 4.2, while it has a bandwidth in the order of a 1 kHz as mentioned in Section 5.2.3. A  $0.1 \mu\text{s}$  clock time thus seems like continuous time in comparison with a bandwidth in the order of a 1 kHz.

### 5.3.1 Cascaded Active-Rectifier Simulation

The CAR simulation is a test where an AC inductor-current,  $I_L$ , is drawn from a AC input voltage,  $V_{ac}$ , to maintain a specific total average bus-voltage,  $V_{cbT}$ . Two ARs are stacked to verify successful current- and voltage-loop integration as well as natural voltage-balancing with equal loads. Only two ARs are stacked to ensure simulation completion. The various components of this simulation, as shown in Figure 5.16, are set up as listed in Appendix C.4.1.

Figure 5.17 depicts the transient response of  $v_{acb}$  and  $v_{bcb}$  on the left and their steady-state result on the right. The transient response indicates improved voltage peaks compared to the AR simulation discussed in Section 4.3.2. This is due to precharging the cell bus-capacitors before control startup, as described in Section 4.4.3. The steady state response indicates acceptable and equal average values. The expected 100 Hz voltage ripple of a rectified 50 Hz input voltage, is also clearly visible. The two bus-voltages are balanced throughout the transient response and the effect of interleaved switching can be seen in the switching ripple, as shown in Figure 5.18.

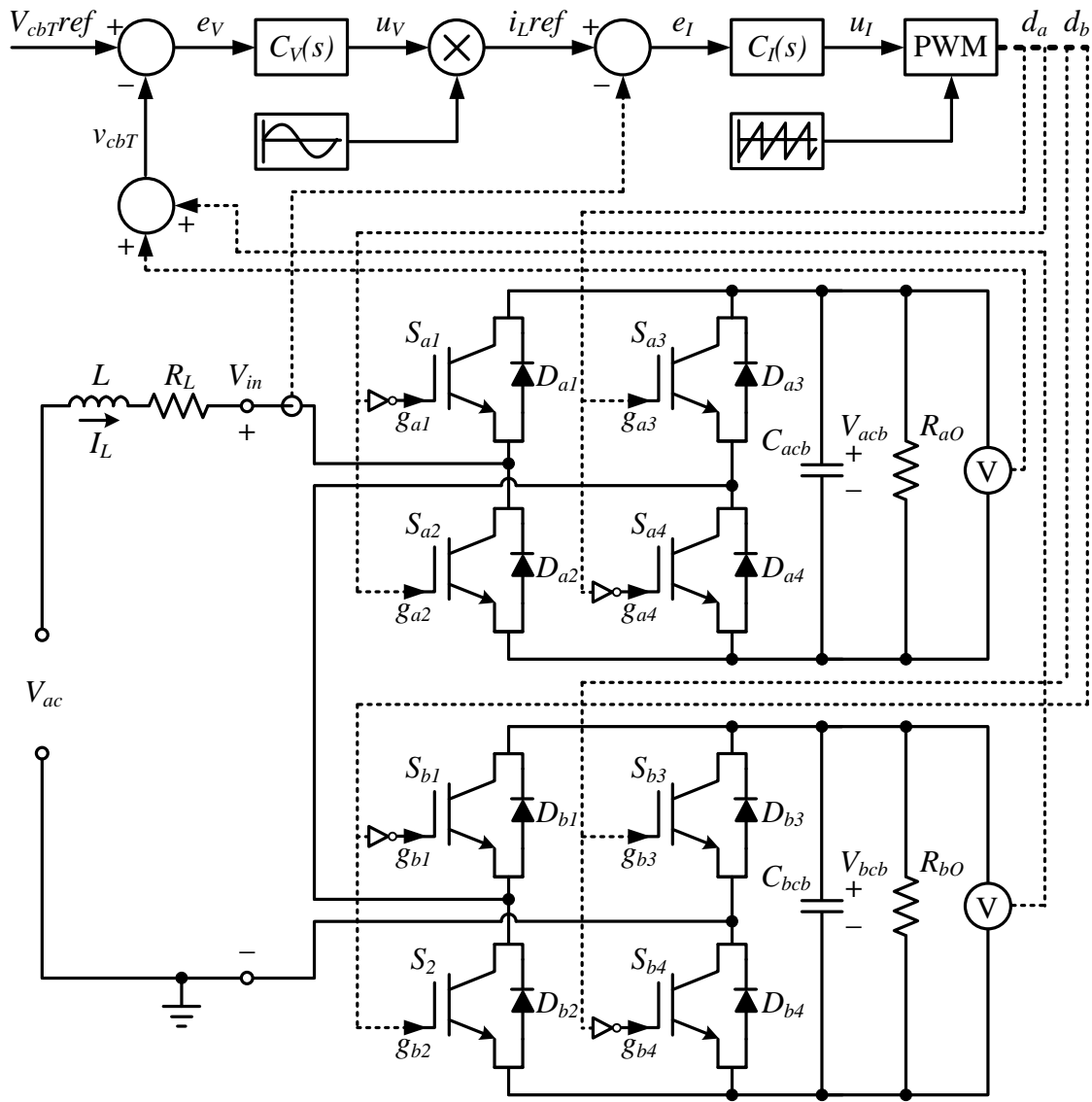


Figure 5.16: Cascaded Active-Rectifier Simulation Setup

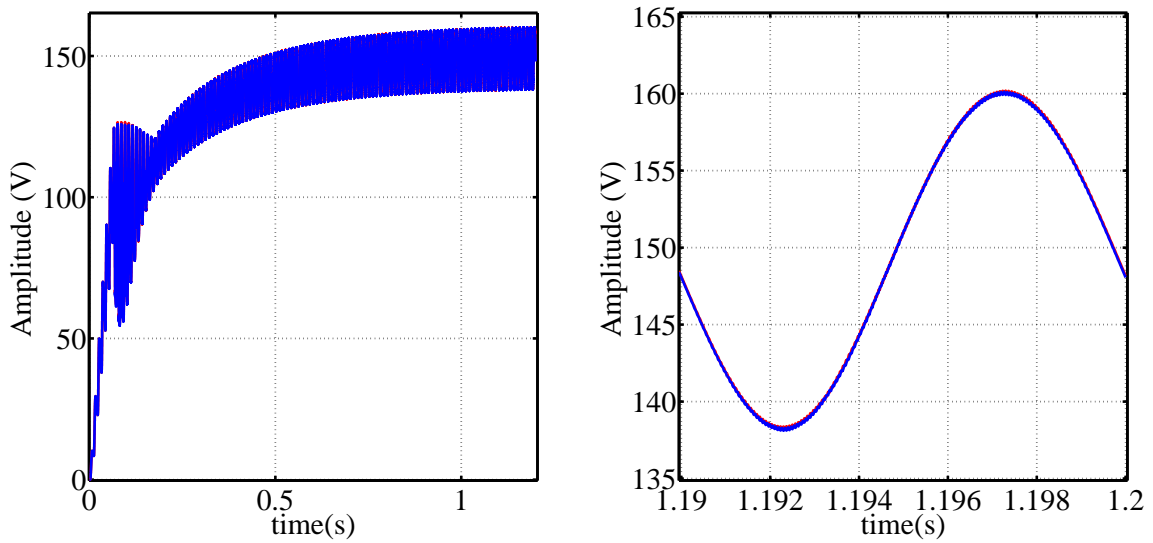


Figure 5.17: Cell Bus-voltages

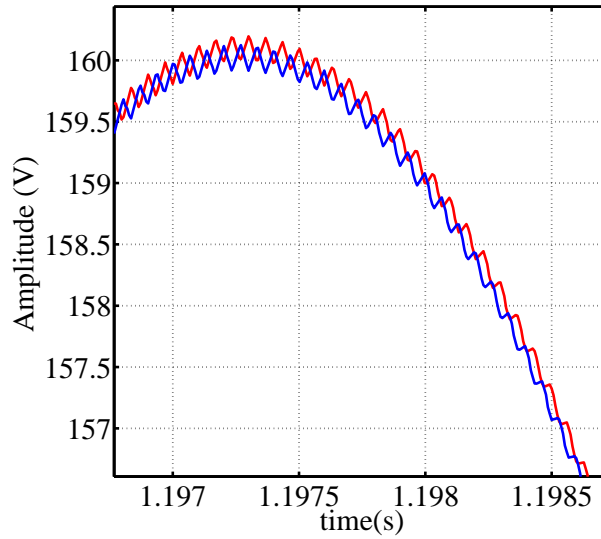


Figure 5.18: Cell Bus-voltages

Figure 5.19 depicts the  $i_{Lref}$  and  $u_V$  transient response on the left and their steady-state result on the right. The transient response shows the same characteristics as discussed in Section 4.3.2. The steady-state result highlights the necessity for a low voltage-loop bandwidth. An increase in bandwidth would cause an increase in the  $u_V$  ripple amplitude. This would, in turn, increase the harmonic distortion of  $i_{Lref}$  and thus also the harmonic distortion of  $I_L$ . The slight CAR voltage-loop bandwidth increase, compared to the AR voltage-loop bandwidth, has a very limited effect on the harmonic distortion of  $I_L$ .

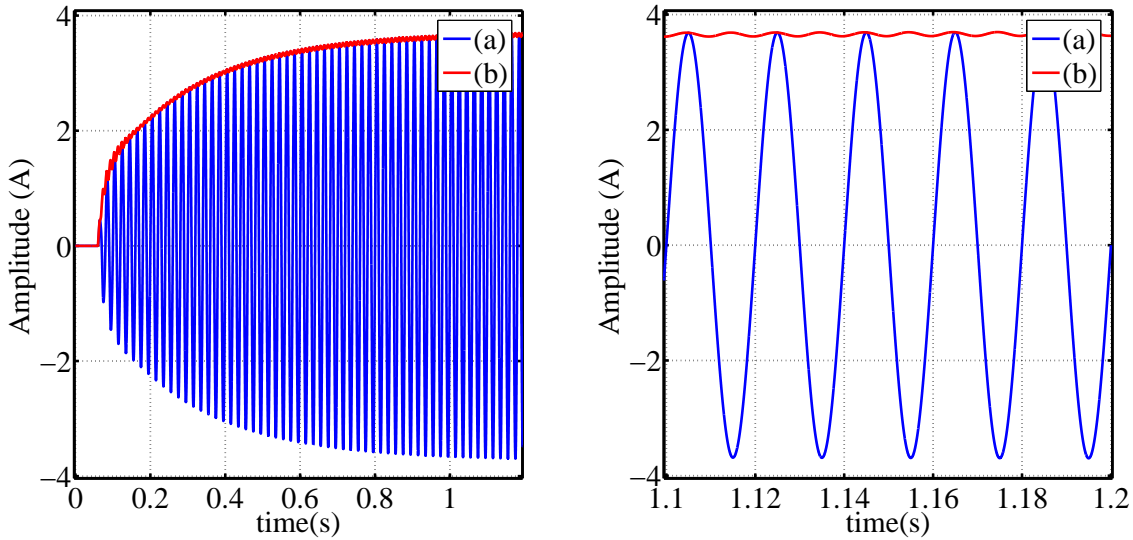
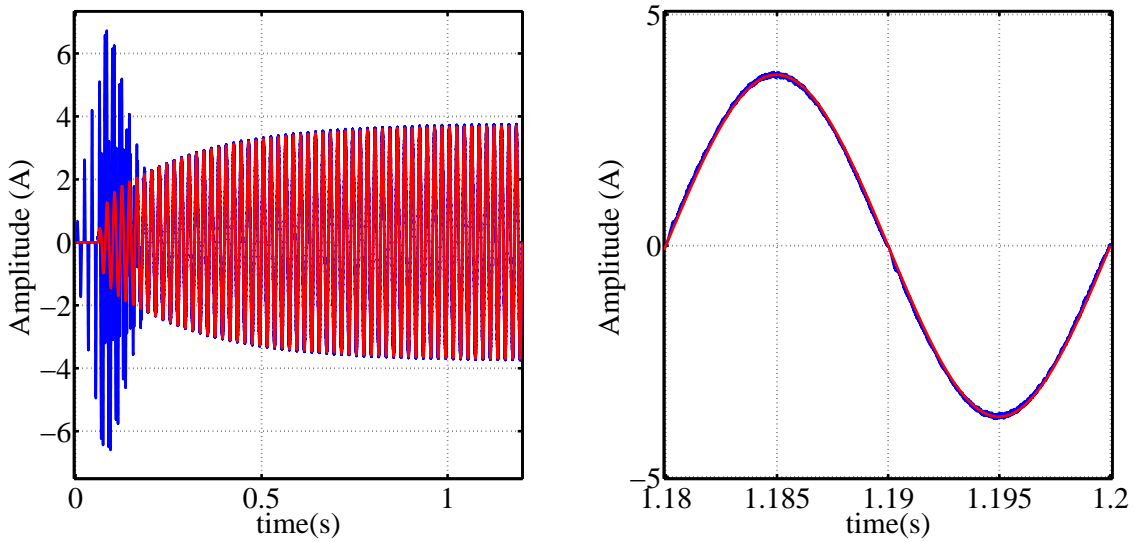


Figure 5.19: (a) Current-Loop Reference; (b) Voltage-Loop Compensator Output

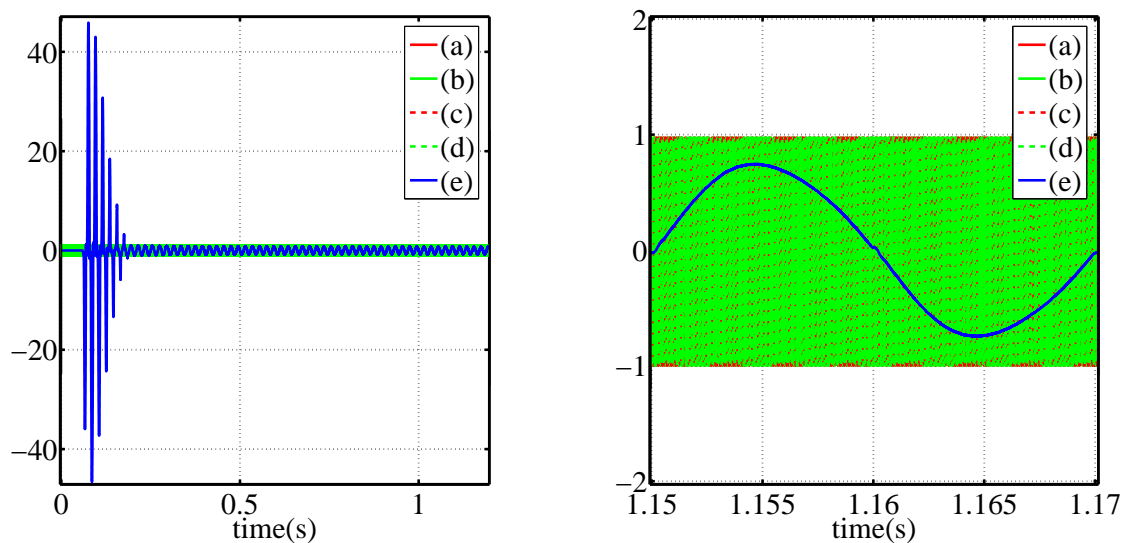
Figure 5.20 depicts the  $i_L$  transient response on the left and its steady-state result on the right, together with  $i_{Lref}$ . The transient response indicates improved current peaks compared to the AR simulation. This is due to the same reason causing the reduced transient bus-voltage peaks, discussed above. The remaining current peaks are due to the ARs acting as full-bridge passive rectifiers while  $v_{cbT}$  is less than  $v_{ac}$ . The steady-state result indicates excellent reference tracking and the current ripple is less compared to the AR simulation. This is due to the

increased effective switching-frequency, as shown in Eq: 5.2.6, while implementing a similar inductor.

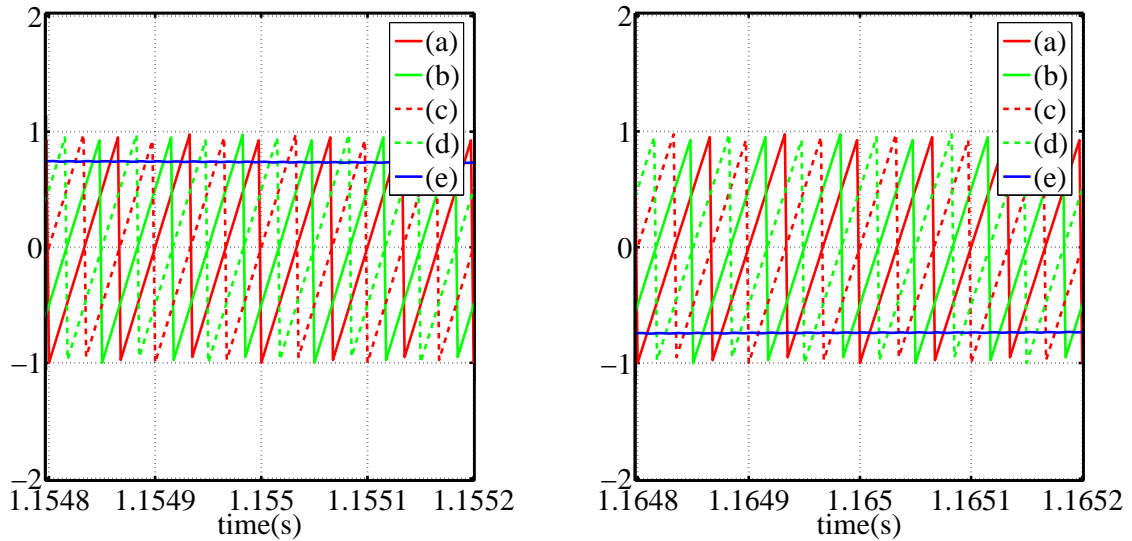


**Figure 5.20:** Inductor Current and Current-Loop Reference

Figure 5.21 depicts the compensator output,  $u_I$ , transient response on the left and its steady-state result on the right, together with the two pairs of interleaved sawtooth carrier-signals. The transient response, as with the inductor-current transient response, indicates where the ARs operates as full-bridge passive rectifiers. This operation causes  $u_I$  to exceed the carrier amplitude limits, because the current-loop attempts to control a system over which it has no control. The steady state response has a sinusoidal shape with a  $180^\circ$  phase shift, compared to the current reference signal. Figure 5.22 depicts the two pairs of interleaved sawtooth carrier-signals. It is also clear the the  $u_I$  ripple is reduced compared to the AR simulation. This ripple indicates the effect of the compensator, on the feedback inductor-current ripple.

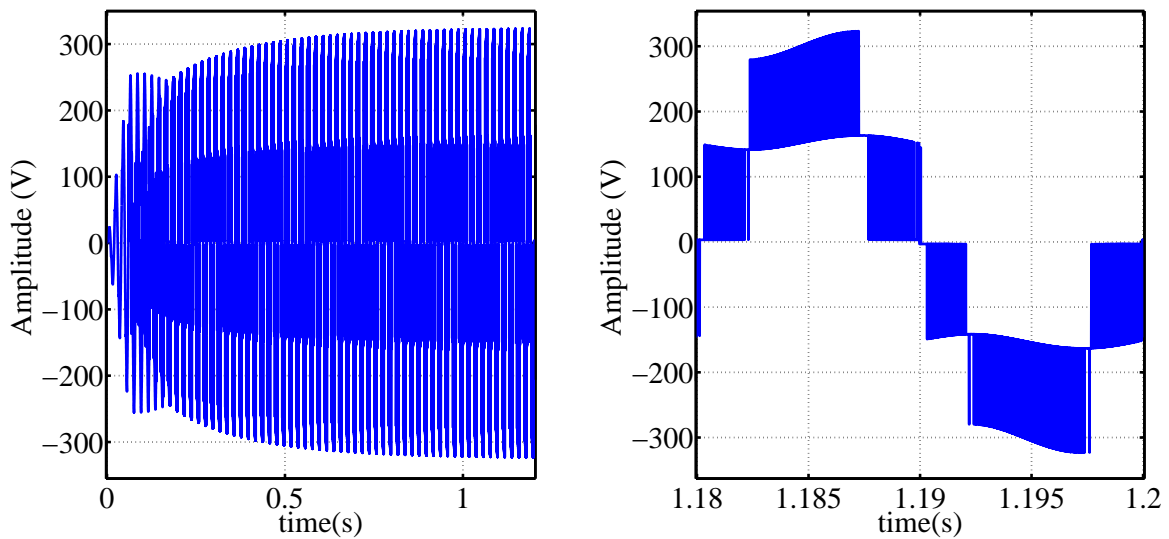


**Figure 5.21:** PWM Signals: (a)  $Carrier_a1$ ; (b)  $Carrier_b1$ ; (c)  $Carrier_a2$ ; (d)  $Carrier_b2$ ; (e)  $u_I$



**Figure 5.22:** PWM Signals: (a)  $Carrier_a1$ ; (b)  $Carrier_b1$ ; (c)  $Carrier_a2$ ; (d)  $Carrier_b2$ ; (e)  $u_l$

Figure 5.23 depicts the input switched-voltage,  $v_{in}$ , transient response on the left and its steady-state result on the right. The transient response peak value mimics the  $v_{cbT}$  transient response. The steady-state result clearly shows five voltage levels with the 100 Hz representation of the cell bus-voltage ripple also visible. This number of voltage levels is expected from a two AR stack, as shown in Eq. 5.2.7. This stack is thus a 5-level converter.



**Figure 5.23:** Input Switched-Voltage

The results obtained from this simulation are satisfactory in determining current- and voltage-loop functionality. Natural cell bus-voltage balancing with equal loads is also verified.

### 5.3.2 Cascaded Active-Rectifier Load-Step Simulation

Two simulations are presented, aimed at verifying acceptable CAR operation during load steps as well as verifying natural voltage rebalancing. The first simulation qualifies as an external perturbation, as discussed in Section 2.2, introducing an  $R_{aO}$  step, at  $t = 0.8$  s, of  $267 \Omega$  to

110 Ω. This increases the power delivered to the total load by ± 40 %. The load,  $R_{bO}$ , remains 267 Ω throughout the simulation.

Figure 5.24 depicts the transient response of  $v_{acb}$ ,  $v_{bcb}$  and  $v_{cbT}$  on the left and their detailed results on the right. The total cell bus-voltage,  $v_{cbT}$  has a very similar, yet faster, transient response compared to the single AR cell bus-voltage load-step result discussed in Appendix B.4.4. The faster response is due to the increased voltage-loop bandwidth. It is also noted that the  $v_{acb}$  decrease from its balanced state is equal to the  $v_{bcb}$  increase from its balanced state. The detailed transient response indicates the 100 Hz cell bus-voltage ripple in all three results throughout.

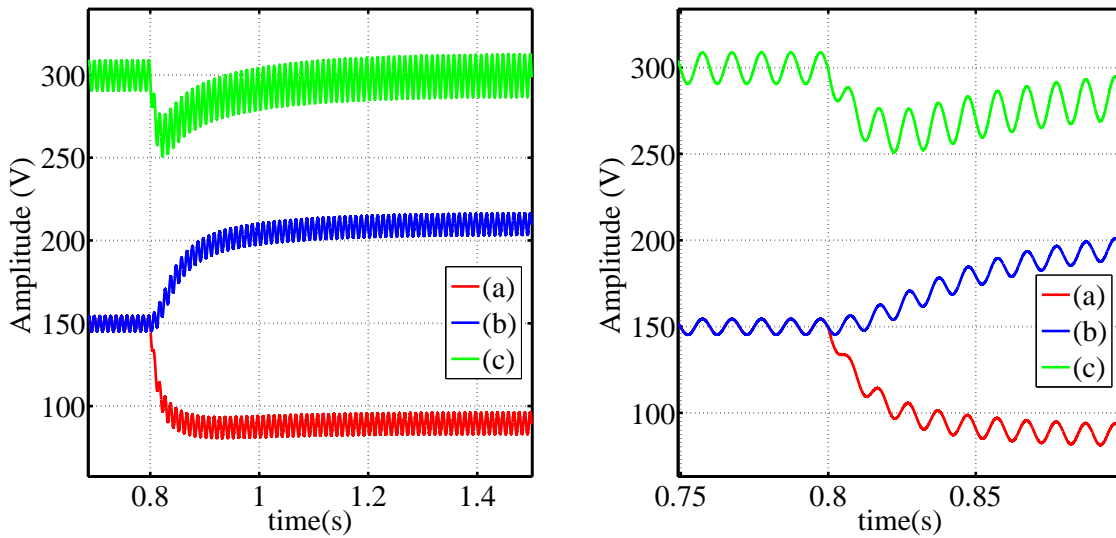


Figure 5.24: (a)  $v_{acb}$ ; (b)  $v_{bcb}$ ; (c)  $v_{cbT}$

Figure 5.25 depicts the  $i_L$  transient response on the left and a detailed result on the right, together with  $i_L ref$ . The current loop is oblivious to the unbalanced cell bus-voltages. It merely increases the inductor current to increase the input power. Excellent current-loop reference tracking is observed and there are no current peaks at the early stages of the transient response. This is because  $v_{cbT}$  never drops below  $v_{ac}$  and normal CAR operation is achieved throughout.

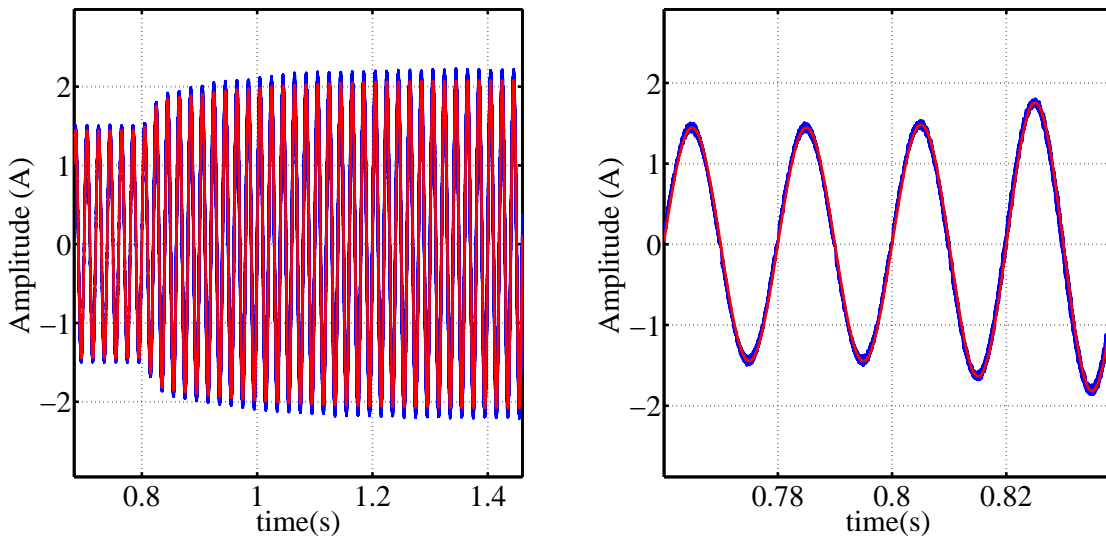


Figure 5.25: Inductor Current and Current-Loop Reference

The second simulation qualifies as AR bus-voltage rebalancing, as discussed in Section 2.2, introducing a  $R_{aO}$  step, at  $t = 1$  s, of  $110 \Omega$  to  $267 \Omega$ . This decreases the power delivered to the total load by  $\pm 30 \%$ . The load,  $R_{bO}$ , remains  $267 \Omega$  throughout the simulation.

Figure 5.26 depicts the transient response of  $v_{acb}$ ,  $v_{bcb}$  and  $v_{cbT}$  on the left and their detailed result on the right. The total cell bus-voltage,  $v_{cbT}$  has a very similar, yet faster, transient response compared to the AR cell bus-voltage load-step result discussed in Appendix B.4.4. The two cell bus-voltages clearly return to a balanced state and maintain their 100 Hz ripple throughout.

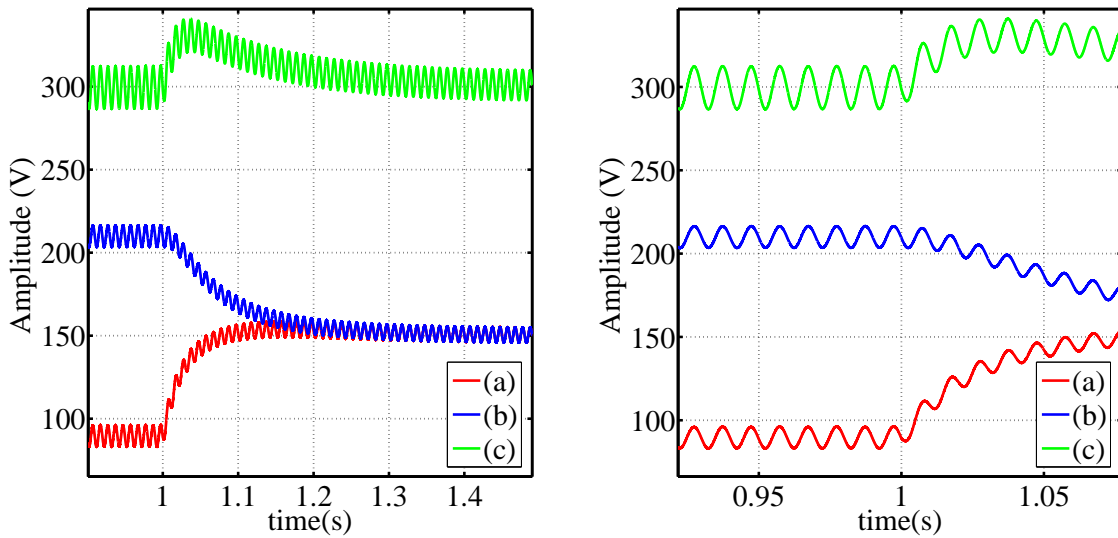


Figure 5.26: (a)  $v_{acb}$ ; (b)  $v_{bcb}$ ; (c)  $v_{cbT}$

Figure 5.27 depicts the  $i_L$  transient response on the left and a detailed result on the right, together with  $i_{Lref}$ . The current loop is oblivious to the rebalancing of the cell bus-voltages. It merely decreases the inductor current to reduce the input power. Excellent current-loop reference tracking is observed throughout.

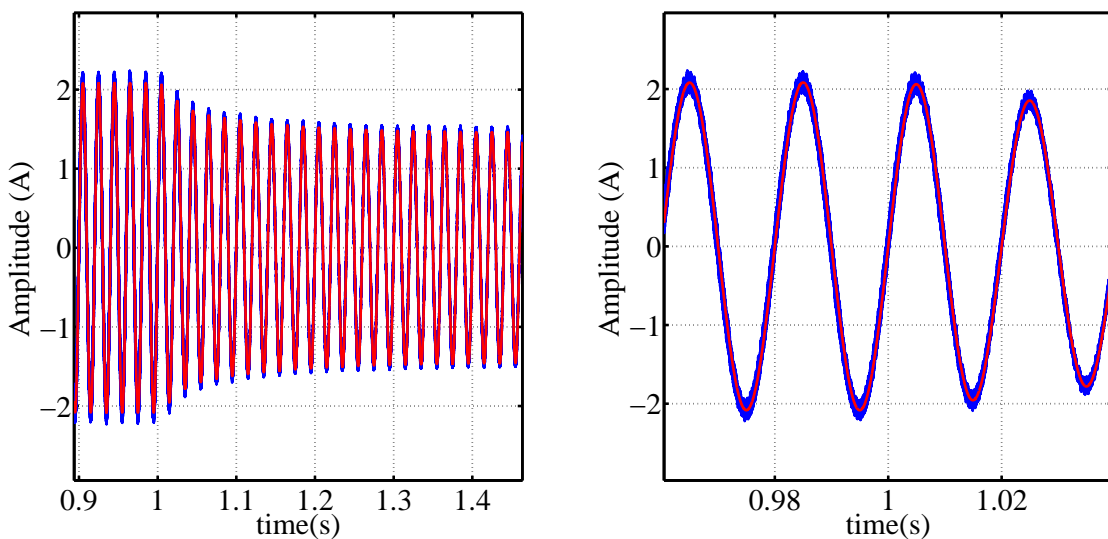
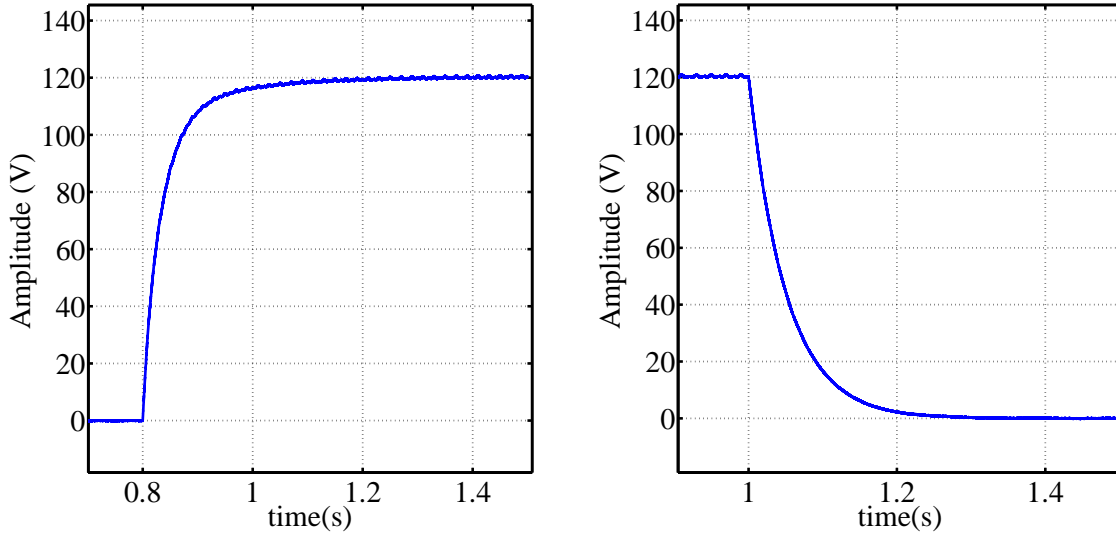


Figure 5.27: Inductor Current and Current-Loop Reference



Figure 5.28 depicts the cell bus difference-voltage,  $v_d$ , for the first and second simulation on the left and right respectively. This voltage is discussed in Section 2.2 and defined as:

$$v_d = v_{bcb} - v_{acb} \tag{5.3.1}$$

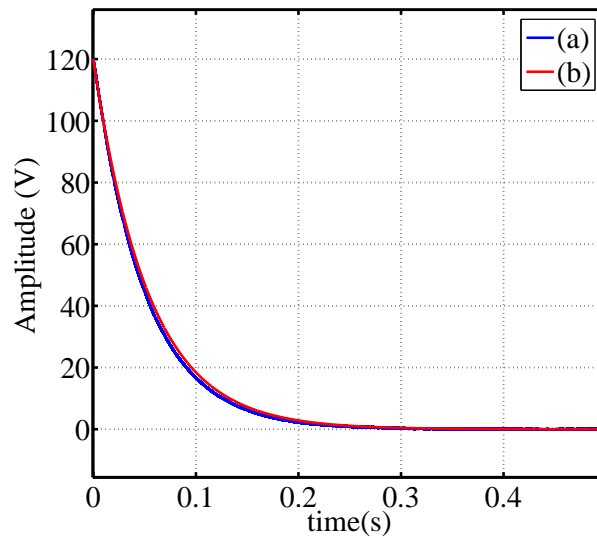


**Figure 5.28:** Cell Bus Difference-Voltage

The result from the rebalancing simulation, on the right, is compared to a calculated rebalancing result as shown in Figure 5.29. This result is obtained, from Eq 2.2.5 and 2.2.6, representing the dominating strong rebalancing mechanism:

$$v_d(t) = V_d(0)e^{-\frac{t}{\tau}}$$

$$\tau = \frac{C}{G_t}$$



**Figure 5.29:** Cell Bus Difference-Voltage: (a) Simulated; (b) Calculated

with  $C$  defined as the bus capacitor value each AR and  $G_t$  defined as:

$$G_t = \frac{R_{aO} + R_{bO}}{2 \cdot R_{aO} \cdot R_{bO}} \quad (5.3.2)$$

The simulation result coincides very closely with the calculated result, however the weak rebalancing mechanism is also present due to interleaved switching. To add the effect of this mechanism to the calculation process is not as straight forward as with the strong rebalancing mechanism. The weak rebalancing mechanism is represented in Eq. 2.2.7 and 2.2.8. These equations are derived for a CAR switching at constant duty cycle,  $d$ . The modulated duty cycle of a controlled CAR can be averaged to determine an effective duty cycle[40]:

$$d_{eff} = \frac{\cos^{-1}(-J_0(\pi m_a))}{2\pi} \quad (5.3.3)$$

with  $J_0$  a Bessel function of the first kind, [41]p632, and  $m_a$  the modulation index.

The results obtained from these simulations are satisfactory in determining acceptable CAR operation during load-steps. Natural cell bus-voltage rebalancing with interleaved switching is also verified and compared to the findings in Section 2.2.

## 5.4 Control Implementation

The CAR control is jointly implemented within the MC and  $N$  CCs, as depicted in Figure 5.30. The control system is implemented in much the same way as the single AR control system. With regard to control hardware, the MC utilises an added fibre-optic transmitter/receiver pair for each added AR. Every added AR is paired with an added CC. With regard to control firmware, the MC firmware needs minor adjustments to accommodate the added ARs. The CC on the other hand, is unaware of other ARs, it is only aware of the MC. The CC firmware thus remains unchanged.

In the remainder of this section the CAR control implementation is further described. The adjustments to accommodate added ARs are emphasized in terms of implementation techniques and hardware utilisation. Implementation challenges as well as their solutions are also discussed.

### 5.4.1 Current-Loop Implementation

The current loop is defined, in terms of implementation, as the control section from the current-loop reference,  $i_L ref$ , to the respective gating signals,  $g_{a1-4}$ - $g_{n1-4}$ . The input-inductor current sampling and scaling procedure remains unchanged. The scaled samples are subtracted from  $i_L(ref)$  to determine  $e_I$ , the input of the compensator,  $C_I(z)$ . This compensator is dependent on the number of ARs in the stack. The appropriately designed compensator,  $C_I(s)$ , is thus transformed to discrete time by using the bilinear approximation together with the  $c2d$  function in MATLAB<sup>®</sup>. The discrete compensator is physically implemented as a difference-equation.

There is a PWM component for each added AR. It implements unipolar-voltage switching by comparing  $u_I(k)$  with the two respective sawtooth carriers, as explained in Section 4.2.1. Interleaving is implemented by configuring the carriers with the correct phase shift, as described in Eq. 5.2.5. Each carrier is implemented with a counter which continuously counts from -1 to 1 after which resetting again to -1. The counter increment-value is calculated to produce carriers with a frequency of  $f_s$ , and the initial counter-value is calculated to incorporate the carrier phase-shift. The single AR PWM communication protocol is altered to a fixed interval protocol, as depicted in Figure 5.31.

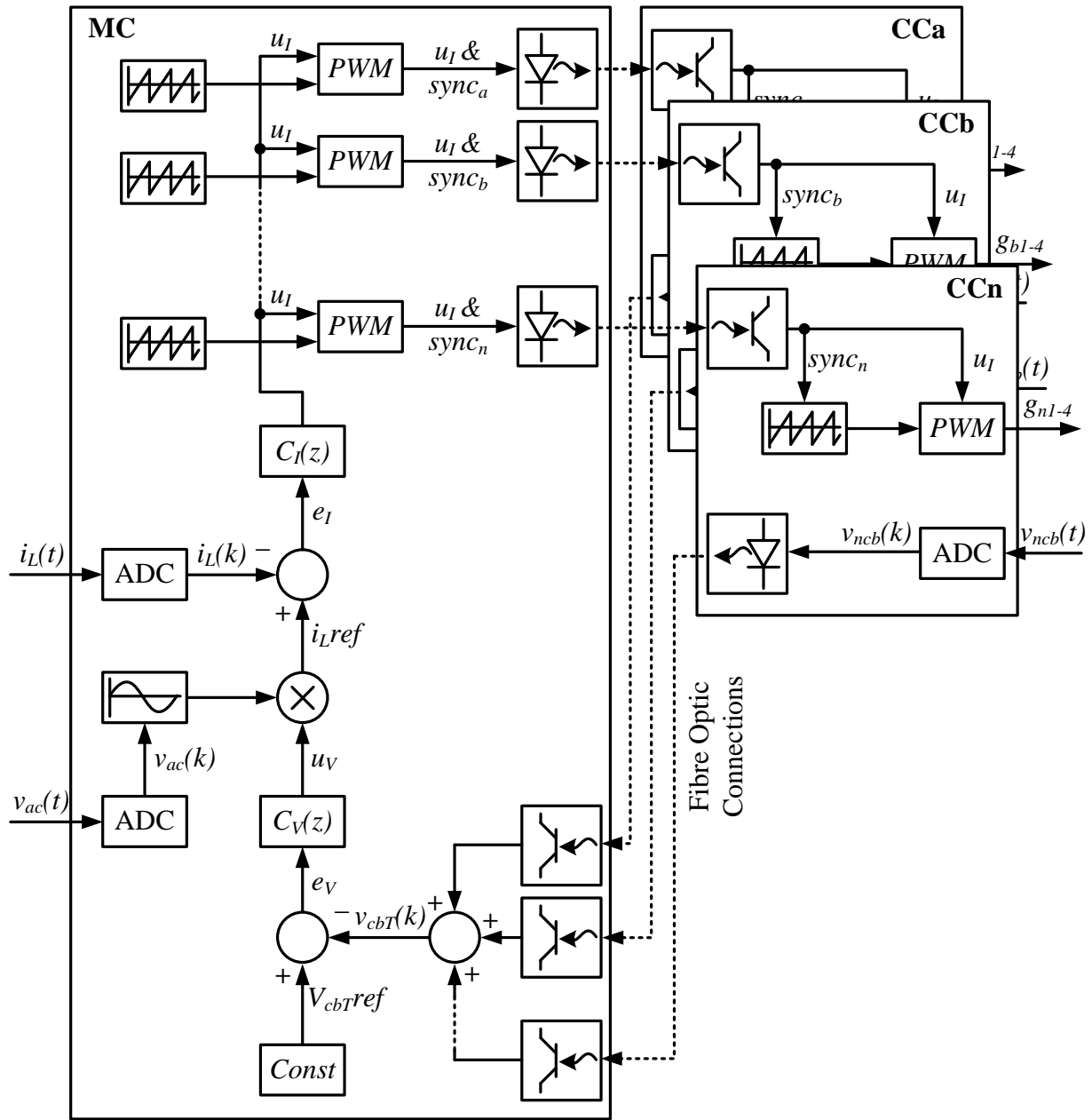
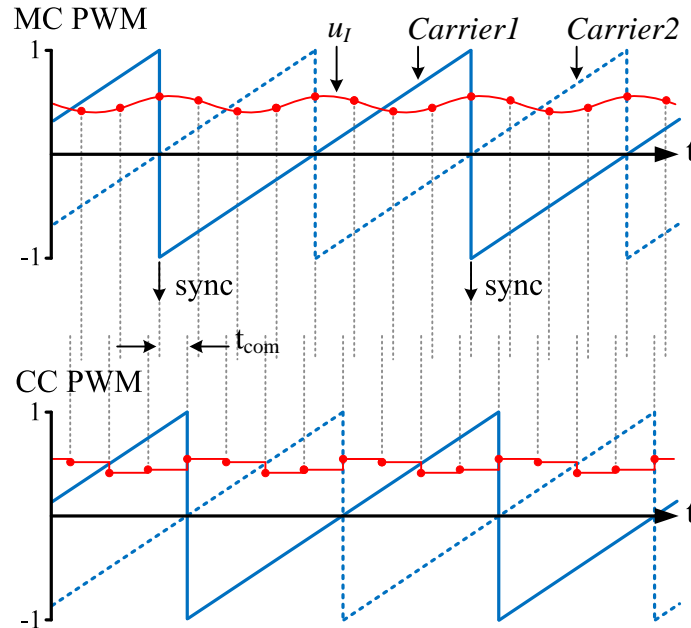


Figure 5.30: Cascaded Active-Rectifier Control Implementation



**Figure 5.31:** PWM Communication Protocol

Eight packages are sent within a switching period,  $T_s$ , to relay the PWM information to the respective CCs. These packages are sent at fixed intervals relative to *carrier1*. One of two package types are used. The first is a synchronise package, sent at every down-slope of *carrier1*. This package contains a synchronise-carriers command, as well as the  $u_I$  value at that moment in time. The second package type is a reference package sent at every interval excluding the interval at the *carrier1* down-slope. This package contains a reference command, as well as the  $u_I$  value at that moment in time. When receiving a synchronise package<sup>1</sup>, the CC resets its carriers and updates its  $u_I$  value, whereas on receiving a reference package, the CC only updates its  $u_I$  value. This PWM communication protocol introduces an error in the CC reference-carrier crossing compared to the MC reference-carrier crossing. The error is reduced with an increased number of packages sent within a switching period. Eight packages per switching period fabricates a small enough error with no noticeable difference in controlled parameters, compared with the PWM communication protocol used for single AR control. The communication protocol change is initiated at the testing phase where fixed-time communication became a desirable feature. This feature is also necessitated by the DC-DC control implementation described in Section 6.3.

There are no changes regarding the Serial Communication Interface (SCI) component<sup>2</sup> used to facilitate the physical package transfer between the MC and respective CC. The CC PWM component implements the same switching scheme as the MC PWM component. The difference between these components is that the CC component generates the gating signals,  $g_{1-4}$ , which trigger the IGBT driver-circuits on the cell. Both MC and CC use the same carrier generation components. The CC carrier signal phase-shift is however implemented by the periodic carrier reset, triggered by a received synchronise package.

<sup>1</sup>The CC carriers are synchronised, at every MC carrier1 down-slope, to prevent carrier drift between the MC and CC.

<sup>2</sup>Developed by [11]

### 5.4.2 Voltage-Loop Implementation

The voltage loop is defined, in terms of implementation, as the control section from  $V_{cbTref}$  to  $i_{Lref}$ . Every discrete cell bus-voltage measurement is received from the respective CC ADC and each sample is scaled to a voltage value represented in volts. This scaled measurement has a resolution of 1 V, which is sent to the MC in the AR-control allocation in the communication package. This  $v_{cb}$  measurement package is sent as reply to any of the two AR-control packages discussed in Section 5.4.1. This reply also acts as a communication functionality check. The MC reacts if this reply is not received within a predefined time, after an AR-control package has been sent. The MC assumes communication loss and moves to an error state.

The MC updates its  $v_{cb}(k)$  sample value from each CC, as the respective  $v_{cb}$  measurement package is received. This means that  $v_{cb}(k)$  from each CC is updated eight times every switching period, as shown in Figure 5.31, while received in an interleaved fashion. The respective  $v_{cb}(k)$  samples from each CC are added to determine the total cell bus-voltage measurement samples,  $v_{cbT}(k)$ . This summation is triggered by flags indicating when a new  $v_{cb}(k)$  sample is received from the respective CC.

The total cell bus-voltage measurement samples is subtracted from the constant reference,  $V_{cbT}(ref)$ , to determine  $e_V$ , the input of the compensator,  $C_V(z)$ . This compensator is dependent on the number of ARs in the stack. The appropriately designed compensator,  $C_V(s)$ , is thus transformed to discrete time by using the bilinear approximation together with the *c2d* function in MATLAB<sup>®</sup>. The discrete compensator is physically implemented as a difference-equation.

The remaining components of the voltage-loop are not altered when adding ARs to the stack. These components include the discretisation of the input-voltage measurement,  $v_{ac}(t)$ , the synchronisation of the unit-sinusoid and the multiplication of this sinusoid with the voltage-loop compensator output,  $u_V$ , to determine  $i_{Lref}$ .

### 5.4.3 Startup Sequence

The startup sequence is defined as the sequence of events to start up the CAR, from system power-up to CAR-control enable to CAR-shutdown, as shown in Figure 5.32. The CCs are programmed with a *.jic* file which means their FPGAs are automatically programmed at every power-up. This necessitates the firmware revision check. The MC is programmed with a *.sof* file which means its FPGA is programmed manually at every power-up.

As the MC is programmed, the start command is given and it opens the input relay disconnecting the input voltage, and initiates a time delay for the operator to do a quick visual system check. The MC then moves to the ping state, where a ping package is sent to each CC to confirm successful communication with a reply ping-package. If a reply ping-package is not received from a specific CC within a predefined time, a second ping package is sent. A maximum of five ping packages are sent at one second intervals. If any of the CCs do not reply by the fifth ping package, a Ping-Error is triggered and the startup process is terminated.

Once all the reply ping-packages have been received, the MC moves to the initialisation state where a sequence of packages are sent to each CC. The first package is a reset-cell package followed by an initialisation package and a request-firmware-revision-number package. The reply package holds the firmware-revision number of the firmware currently programmed on the respective CC. This number is compared to the required firmware-revision number. A Firmware-Revision-Number-Mismatch-Error is triggered if any of the CC firmware-revision numbers do not match and the startup process is terminated. If all firmware-revision numbers match, the MC sends a sequence of packages to each CC containing the CC measurement-limits. After all these package replies have been received, the MC sends a Detect-Cell-Bus-Voltage-Measurement-

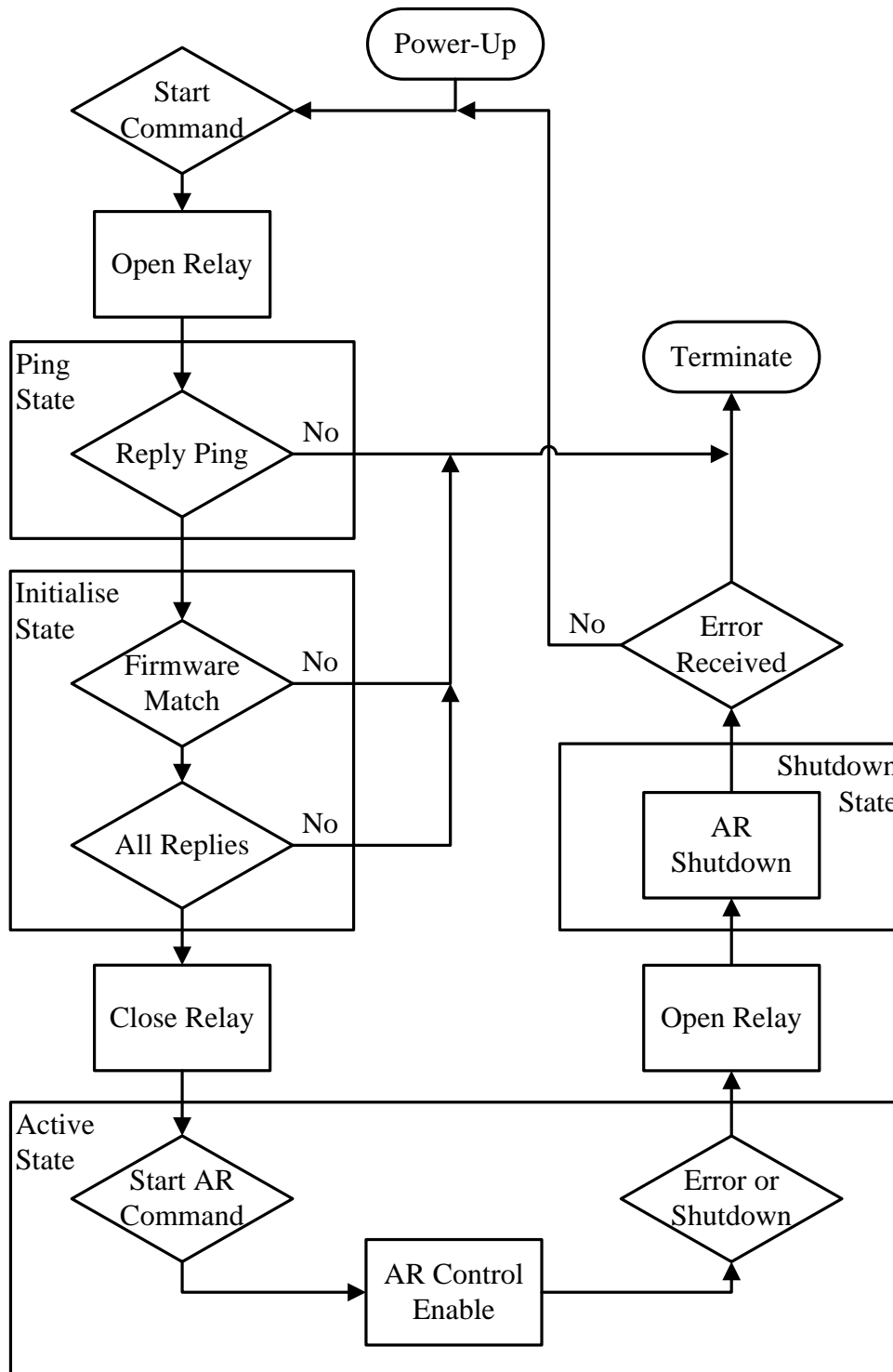


Figure 5.32: CAR Startup Sequence

Offset package. This triggers each CC to measure its  $v_{cb}$  measurement-offset, and compensate its  $v_{cb}$  measurements in the active state. This concludes initialisation. The MC closes the input relay and moves to the active state if all package replies have been received. Otherwise a Reply-Lag-Error is triggered and the startup-process is terminated

When ready, the operator can increase the input voltage to precharge the cell bus-capacitors with diode currents. There are two ways of determining when all the  $C_{cbs}$  have been precharged. One is checking the  $v_{ac}$  measurement and the second is checking the  $v_{cb}$  measurements. If the latter is implemented, the MC regularly sends Requesting-Bus-Voltage packages to each CC, to check these measurements.

Once the average  $v_{cb}$  measurement reaches a predefined value, the cell bus-capacitors are perceived as precharged and the Start-AR command is given. The component responsible for synchronising the unit-sinusoid, is then enabled. After three successfully synchronized cycles, the AR-control components are enabled and reset and an enable-AR package is sent to each CC. From this point the MC continually sends AR-control packages to each CC, as discussed in Section 5.4.1, which facilitates the control of  $v_{cbT}$  at a certain average value, while drawing a sinusoidal input-current,  $i_L$ .

The ARs remain in operation until a shutdown is triggered or any of the errors mentioned in Section 5.4.4 occur. This triggers the MC to open the input relay, disconnecting the input voltage, and move to the shutdown state. A shutdown-AR package is sent to each CC which triggers it to shut down its AR by disabling its AR-control components and opening all AR switches. If the shutdown was triggered by the operator reducing the input voltage to a predefined value, the system resets and waits for the next start command. On the other hand, if the shutdown was triggered by an error, the system terminates. At this stage the operator should determine the cause of the error and rectify the problem.

#### 5.4.4 Error Handling

CAR errors can be classified as measurement errors and system errors. Measurement errors are defined as measurements exceeding predefined limits and system errors are defined as system malfunction. All measurements are checked for measurement errors. The measurements checked by each CC, for CAR implementation, are:

- Cell Bus-Voltage,  $V_{cb}$
- Load Current<sup>3</sup>,  $I_{Ro}$
- IGBT Heat Sink Temperature,  $T_{sink}$
- Isolated Power Supply Voltage,  $V_{ips}$

The measurements checked by the MC, for CAR implementation, are:

- Input Voltage,  $V_{ac}$
- Input-Inductor Current,  $I_L$
- Cell Bus-Voltage,  $V_{cb}$

---

<sup>3</sup>This measurement circuitry is designed primarily to measure the Transformer Current,  $I_t$ , during implementation of the complete cell.

- Cell Bus-Voltage imbalance<sup>4</sup>

The system errors handled by the MC are:

- **SCI Read Data Error:** When the SCI component indicates that a package could not be read successfully.
- **Firmware Revision Number Mismatch:** When the firmware revision, programmed on a CC, does not match the firmware revision required by the MC.
- **Ping Error:** When a CC does not echo the ping package sent at system startup.
- **Command Mismatch:** When any reply-package command sent by a CC does not match the package command sent by the MC.
- **Reply Lag Error:** When any reply package is not received within the predefined time.

With the occurrence of a CC measurement error during the active state, the respective CC sends an error package to the MC, with an error indicating command. When any of the MC measurement- or system-errors occurs during the active state, or when an error package is received from any CC, the MC proceeds to the shutdown state as discussed in Section 5.4.3. The CAR is thus shut down before any system damage or operator danger can arise.

## 5.5 Test Measurements

Physical tests were performed to verify control-system functionality as a whole as well as natural cell bus-voltage balancing. All distinct aspects of the control system are also separately checked to establish proper functioning. These aspects include: all measurements, implemented compensators and other control components and the communication between the MC and respective CCs. The measurements taken vary between Signal-Tap measurements, as described in Section 4.5, and Oscilloscope measurements. The Tektronix TDS 3014 oscilloscope is used with a bandwidth of 100 MHz, capable of a 1.25 GS/s sample rate.

### 5.5.1 Cascaded Active-Rectifier Test Measurements

The CAR test, as with the CAR simulation, is a test where an AC inductor-current,  $I_L$ , is drawn from a AC input voltage,  $V_{ac}$ , to maintain a specific total average bus-voltage,  $V_{cbT}$ . Two ARs are stacked to verify successful current- and voltage-loop implementation as well as natural voltage-balancing with equal loads. The physical test setup, as depicted in Figure 5.33, is discussed in Appendix C.5.1.

The startup sequence is followed as discussed in Section 5.4.3 with  $R_{aO} = R_{bO} = 267 \Omega$ . The operator waits until the MC enters its active state before turning up the variac by hand. The cell bus-capacitors are charged by diode currents and the ARs start up as soon as the average of  $v_{acb}$  and  $v_{bcb}$  reaches 100 V.

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<sup>4</sup>Cell Bus-Voltage imbalance is the only measurement-check added to the single AR measurement checks for CAR implementation.



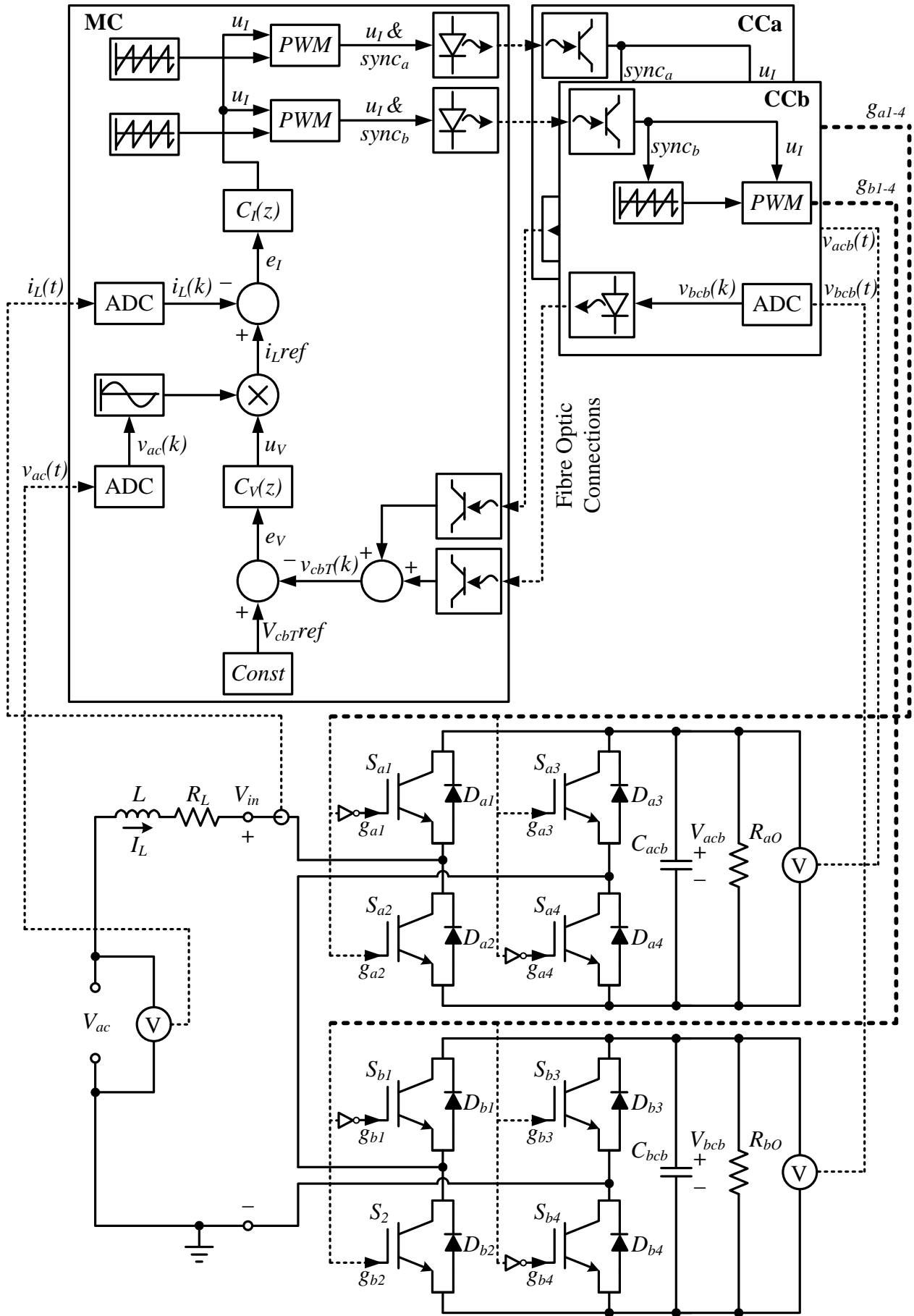
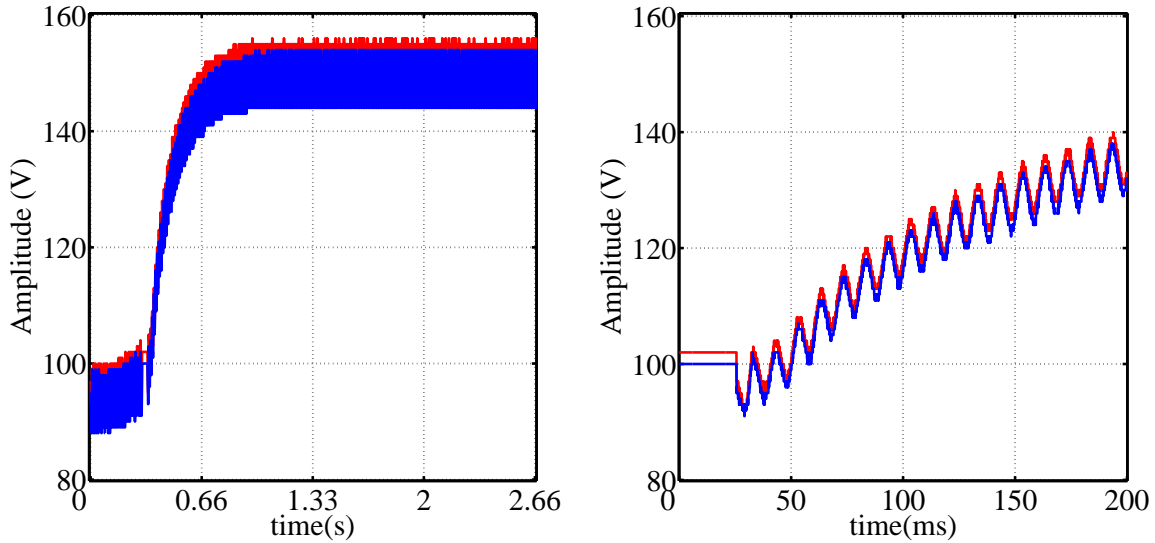


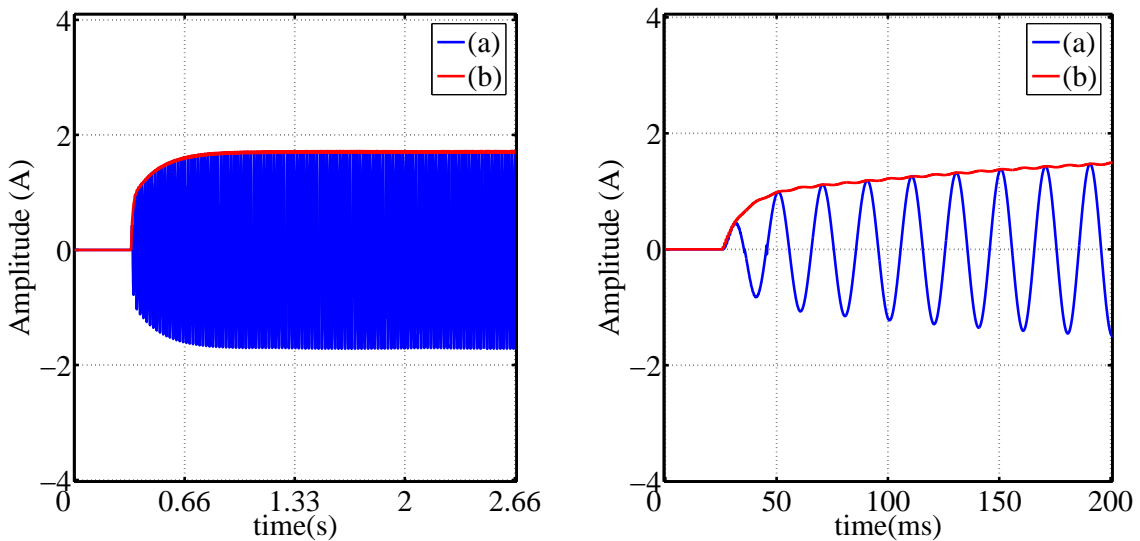
Figure 5.33: Cascaded Active-Rectifier Test Setup

Figure 5.34 depicts the  $v_{acb}$  and  $v_{bcb}$  transient Signal-Tap measurement on the left and a detailed measurement on the right. The two cell bus-voltages are well balanced. The slight 1-2 V imbalance is due to the loads used. These load resistors are high power, wire wound, with their values not exactly equal.



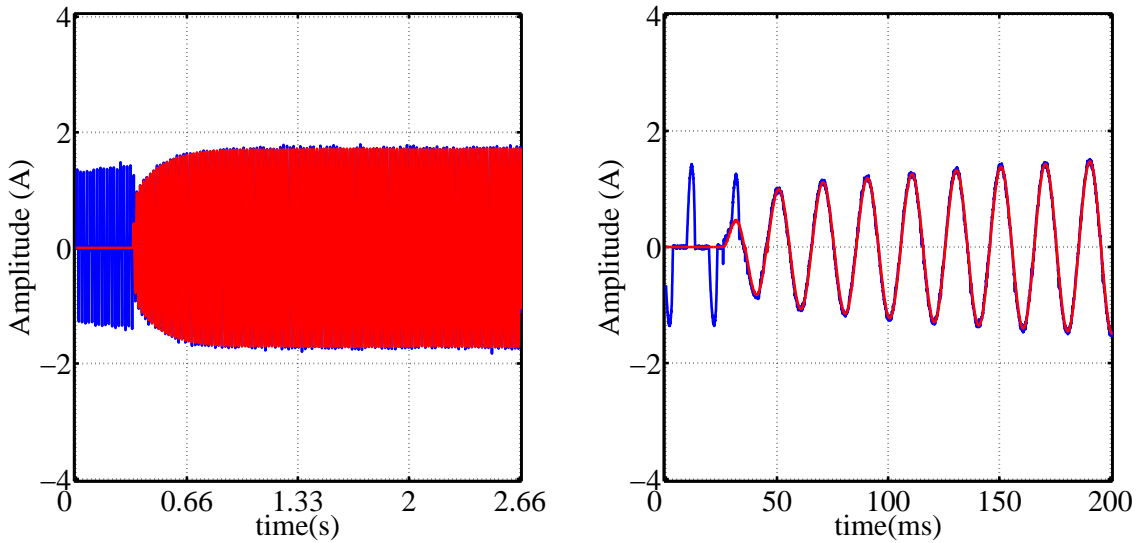
**Figure 5.34:** Signal-Tap Measurement: Cell Bus-Voltages

Figure 5.35 depicts the  $i_{Lref}$ - and  $u_V$ -transient Signal-Tap measurement on the left and a detailed measurement on the right. The result shows the same characteristics as the single AR test, discussed in Section 4.4.2.



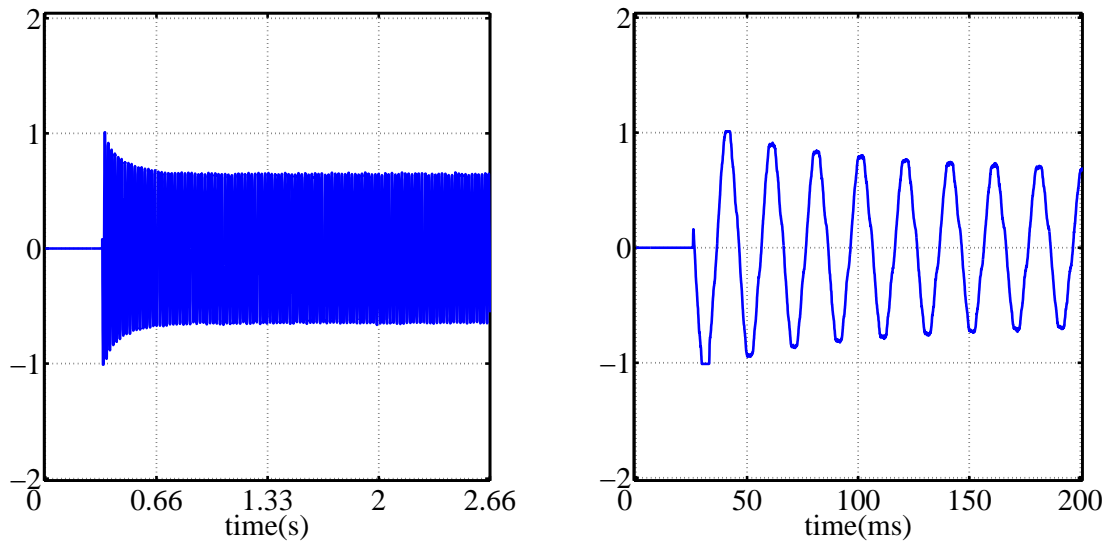
**Figure 5.35:** Signal-Tap Measurement: (a)  $i_{Lref}$ ; (b)  $u_V$

Figure 5.36 depicts the  $i_L$ - and  $i_{Lref}$ -transient response Signal-Tap measurement on the left and a detailed measurement on the right. The diode current-flow prior to AR startup is clearly visible, after which the current waveform flows into a sinusoidal profile. This startup method thus prevents any extensive current peaks, as observed in the simulation results.



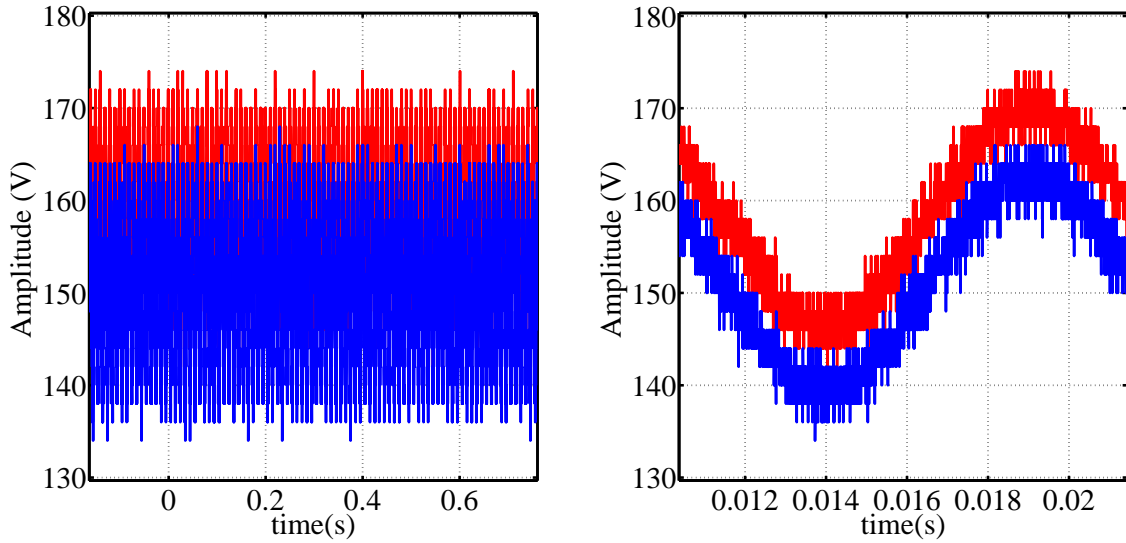
**Figure 5.36:** Signal-Tap Measurement:  $i_L$  and  $i_Lref$

Figure 5.37 depicts the  $u_I$ -transient Signal-Tap measurement on the left and a detailed measurement on the right. The result shows the same characteristics as the single AR test, discussed in Section 4.4.2. The fast initial  $u_I$ -step at startup is due to the high current-loop bandwidth, while the gradual decrease in amplitude is due to the slow voltage-loop bandwidth.

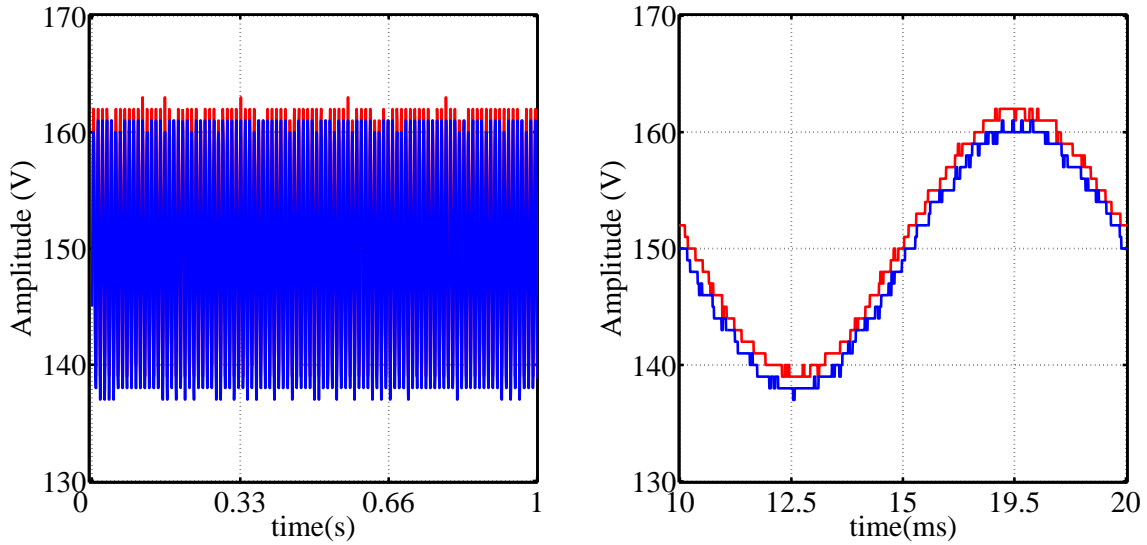


**Figure 5.37:** Signal-Tap Measurement:  $u_I$

For the following measurements the two loads,  $R_{aO}$  and  $R_{bO}$ , are stepped to  $110 \Omega$  each. Figure 5.38 depicts the  $v_{acb}$  and  $v_{bcb}$  steady-state oscilloscope measurement on the left and a detailed result on the right. Figure 5.39 depicts the  $v_{acb}$  and  $v_{bcb}$  steady-state Signal-Tap measurement on the left and a detailed result on the right. The oscilloscope measurement shows a 6-7 V imbalance while the Signal-Tap measurement shows a 1-2 V imbalance. The differential probes used with the oscilloscope measurement are prone to measuring a slight offset. The Signal-Tap measurement is received from the respective CCs. Each CC cell bus-voltage measurement-offset is detected during the initialise state and compensated for during the active state. The Signal-Tap measurement is thus the superior measurement.



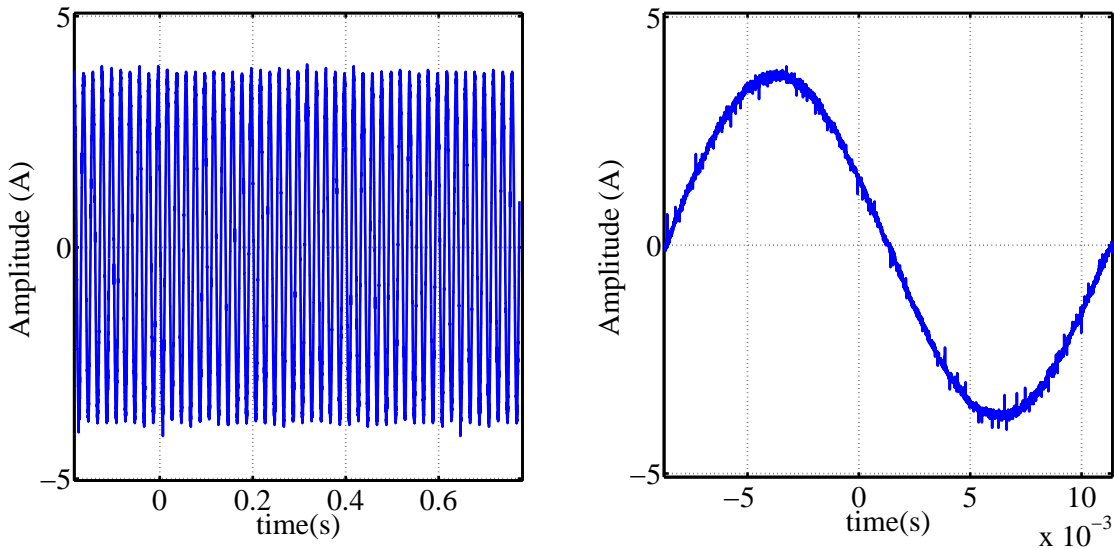
**Figure 5.38:** Oscilloscope Measurement: Cell Bus-Voltages



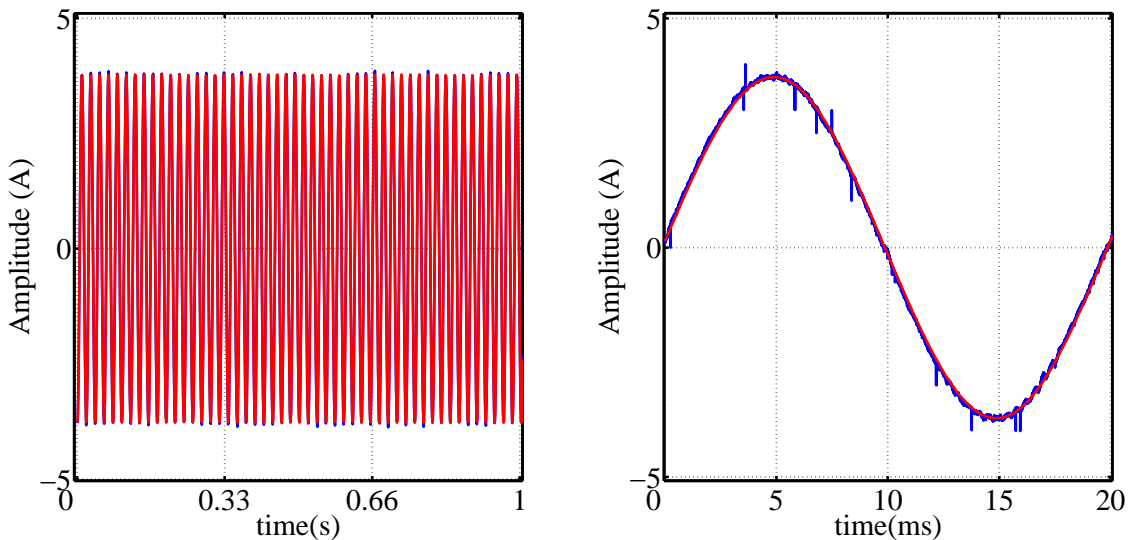
**Figure 5.39:** Signal-Tap Measurement: Cell Bus-Voltages

Figure 5.40 depicts the  $i_L$  steady-state oscilloscope measurement on the left and a detailed result on the right. Figure 5.41 depicts the  $i_L$  and  $i_{Lref}$  steady-state Signal-Tap measurement on the left and a detailed result on the right. Both measurements show a superb sinusoidal current waveform. The Signal-Tap measurement reveals excellent current-loop reference tracking.

Figure 5.42 depicts the  $V_{in}$  steady-state oscilloscope measurement on the left and a detailed measurement on the right. As with the CAR simulation discussed in Section 5.3.1, the result clearly shows five voltage levels with the 100 Hz representation of the cell bus-voltage ripple also visible.



**Figure 5.40:** Oscilloscope Measurement: Inductor Current



**Figure 5.41:** Signal-Tap Measurement:  $i_L$  and  $i_Lref$

The measurements obtained are satisfactory in verifying successful current- and voltage-loop integration. Natural cell bus-voltage balancing with equal loads is also verified.

## 5.5.2 Cascaded Active-Rectifier Load-Step Test Measurements

Two measurement tests are presented, aimed at verifying acceptable CAR operation during load steps as well as verifying natural voltage rebalancing. The first test qualifies as an external perturbation, as discussed in Section 2.2, introducing an  $R_{aO}$  step of  $267 \Omega$  to  $110 \Omega$ . This increases the power delivered to the total load by  $\pm 40 \%$ . The load,  $R_{bO}$ , remains  $267 \Omega$  throughout the test.

Figure 5.43 depicts the oscilloscope measurement of the  $v_{acb}$ ,  $v_{bcb}$  and  $v_{cbT}$  transient response on the left and their detailed result on the right. The total cell bus-voltage,  $v_{cbT}$  coincides very well with the simulation result discussed in Section 5.3.2 as well as with the single AR cell bus-voltage load-step result discussed in Appendix B.4.4. It is also noted that the  $v_{acb}$

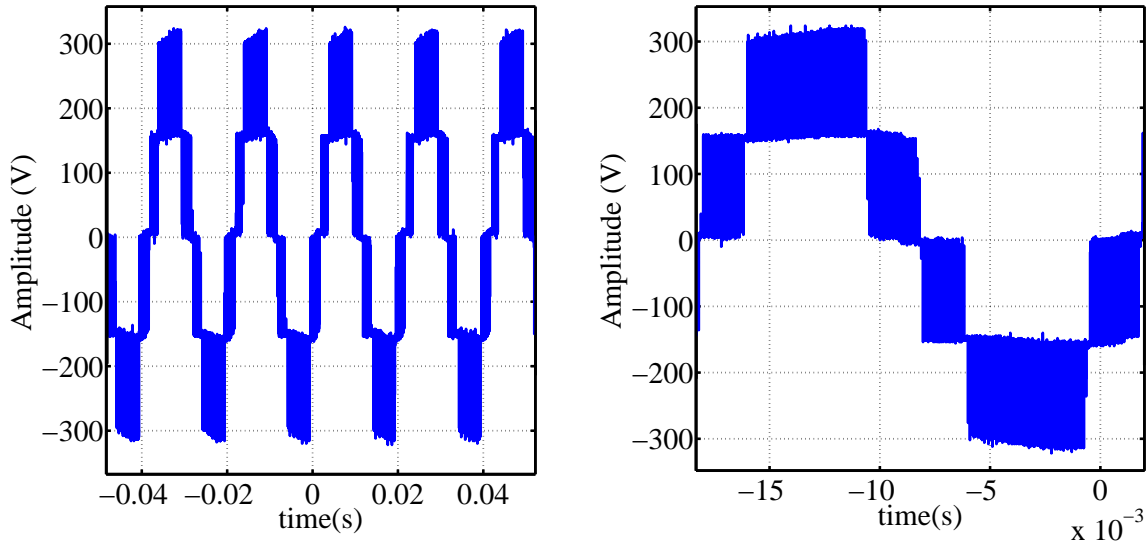


Figure 5.42: Input Switched Voltage

decrease from its balanced state is equal to the  $v_{bc}$  increase from its balanced state. The detailed transient response indicates the 100 Hz cell bus-voltage ripple on all three measurements throughout.

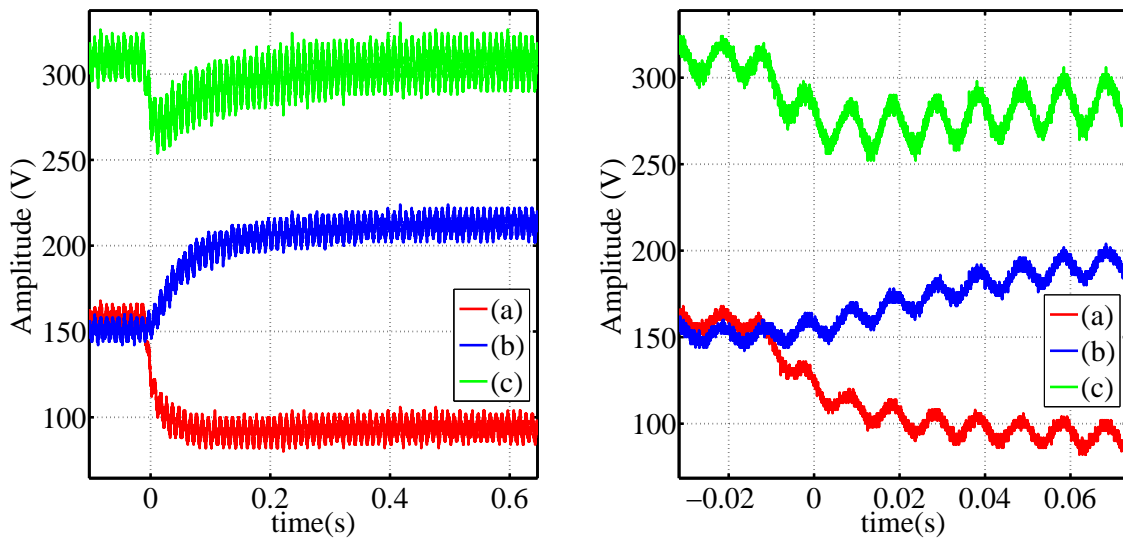
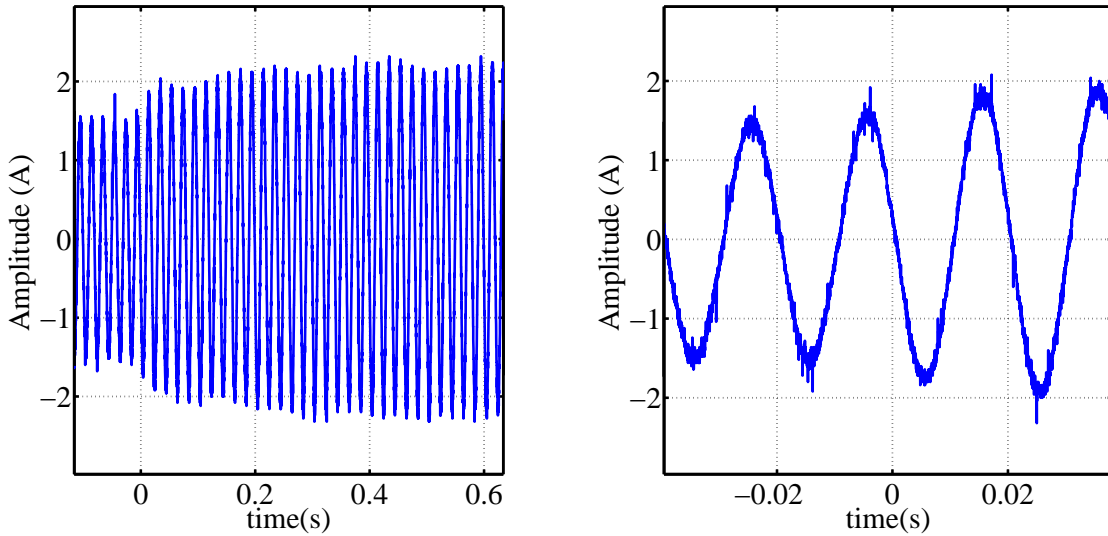


Figure 5.43: Oscilloscope Measurement: (a)  $v_{acb}$ ; (b)  $v_{bc}$ ; (c)  $v_{cbT}$

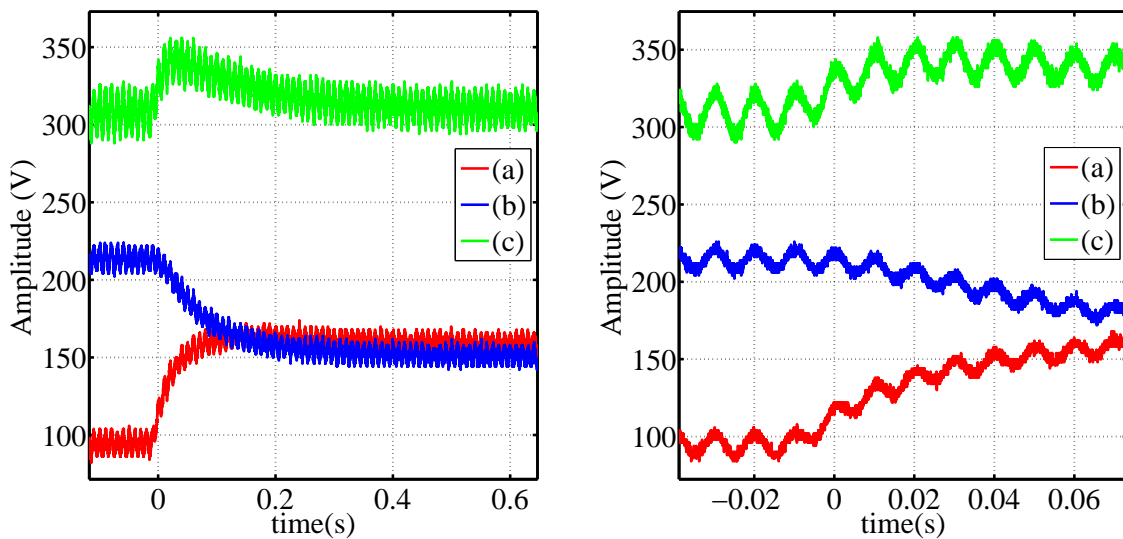
Figure 5.44 depicts the oscilloscope measurement of the  $i_L$  transient response on the left and its detailed result on the right. As with the simulation results discussed in Section 5.3.2, the measurement shows that the current loop is oblivious to the unbalanced cell bus-voltages. It merely increases the inductor current to increase the input power. An excellent sinusoidal waveform is observed with a seemingly drifting average. This measurement error is due to aliasing effects within the oscilloscope. There is also a degree of switching noise present.

The second test qualifies as AR bus-voltage rebalancing, as discussed in Section 2.2, introducing an  $R_{aO}$  step of  $110 \Omega$  to  $267 \Omega$ . This decreases the power delivered to the total load by  $\pm 30 \%$ . The load,  $R_{bO}$ , remains  $267 \Omega$  throughout the test.



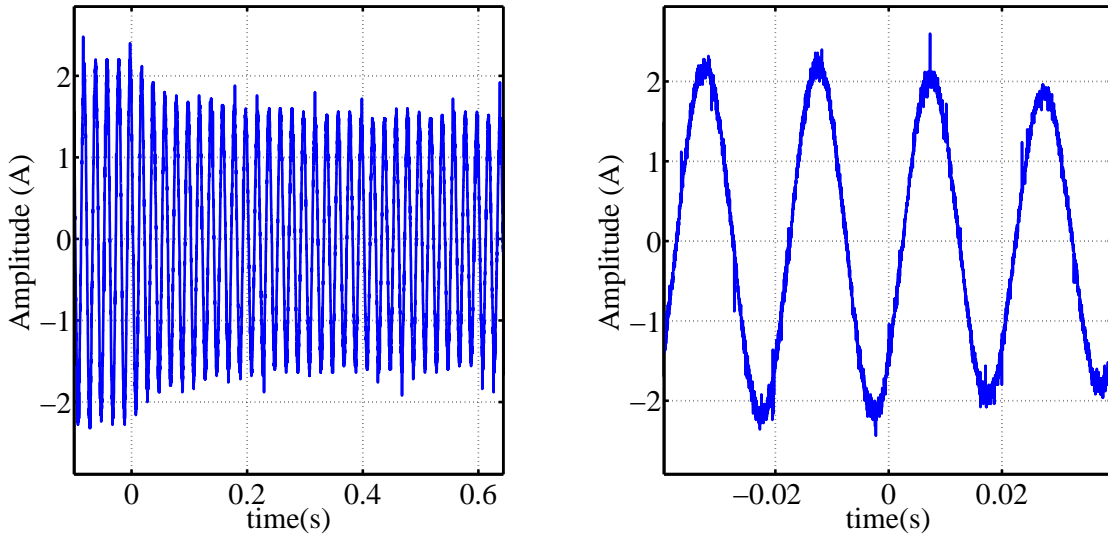
**Figure 5.44:** Oscilloscope Measurement: Inductor Current

Figure 5.45 depicts the oscilloscope measurement of the  $v_{acb}$ ,  $v_{bcb}$  and  $v_{cbT}$  transient response on the left and their detailed result on the right. The total cell bus-voltage,  $v_{cbT}$  coincides very well with the simulation result discussed in Section 5.3.2. It is also noted that the two cell bus-voltages clearly return to a balanced state, overlooking the differential probe offset. The 100 Hz bus-voltage ripple of all three measurements are maintained throughout.



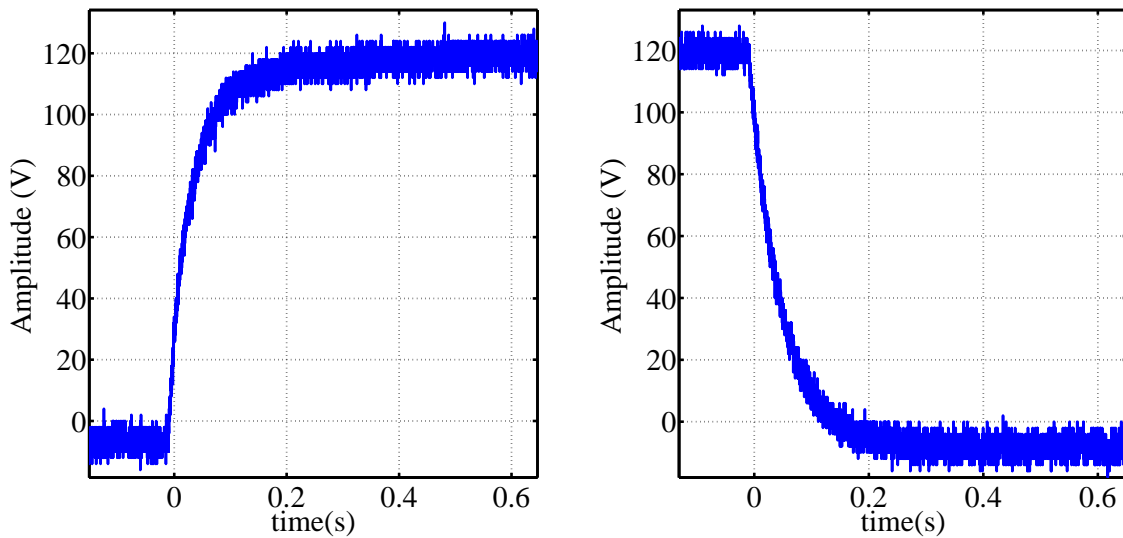
**Figure 5.45:** Oscilloscope Measurement: (a)  $v_{acb}$ ; (b)  $v_{bcb}$ ; (c)  $v_{cbT}$

Figure 5.46 depicts the oscilloscope measurement of the  $i_L$  transient response on the left and its detailed result on the right. As with the simulation results discussed in Section 5.3.2, the measurement shows that the current loop is oblivious to the rebalancing of the cell bus-voltages. It merely decreases the inductor current to decrease the input power. An excellent sinusoidal waveform is observed with a seemingly drifting average. This measurement error is due to aliasing effects within the oscilloscope. There is also a degree of switching noise present.



**Figure 5.46:** Oscilloscope Measurement: Inductor Current

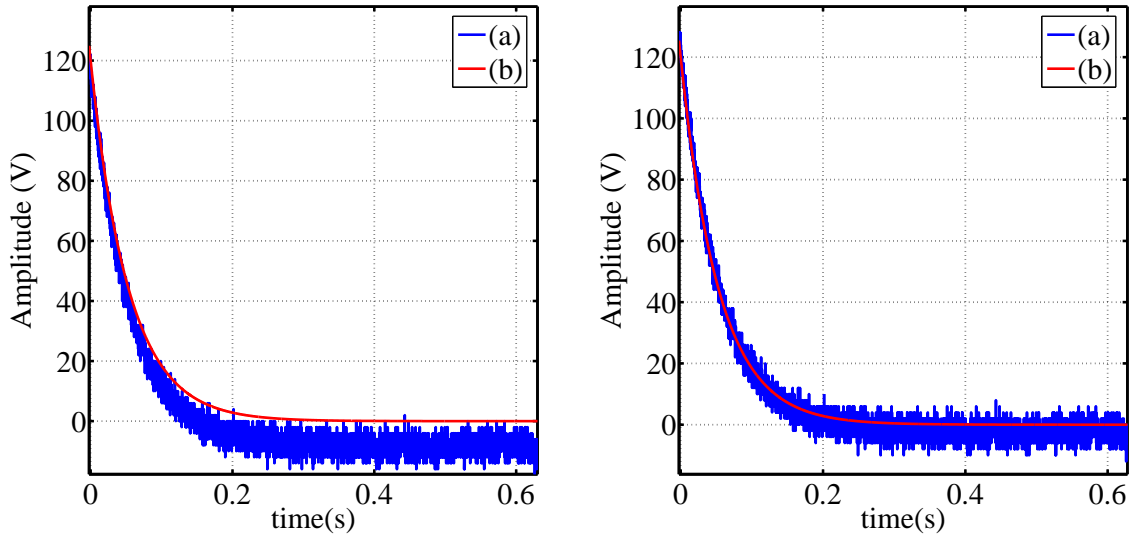
Figure 5.47 depicts the cell bus difference-voltage,  $v_d$ , for the first and second measurement test on the left and right respectively. These measurements coincide very well with the simulation results discussed in Section 5.3.2.



**Figure 5.47:** Cell Bus Difference-Voltage

The result from the rebalancing test, on the right, is compared to a calculated rebalancing result obtained from Eq 2.2.5 and 2.2.6. These equations represent the dominating strong rebalancing mechanism. Figure 5.48 depicts the measurement compared to the calculated result on the left and the differential-probe offset compensated measurement compared to the calculated result on the right. Overlooking the differential probe offset, the measurement coincides well with the calculated result, however the weak rebalancing mechanism is also present due to interleaved switching. To add the effect of this mechanism to the calculation process is not as straight forward as with the strong rebalancing mechanism, as discussed in Section 5.3.2.





**Figure 5.48:** Cell Bus Difference-Voltage: (a) Measured; (b) Calculated

The measurements obtained are satisfactory in determining acceptable CAR operation during load-steps. Natural cell bus-voltage rebalancing with interleaved switching is also verified and compared to the findings in Section 2.2.

## 5.6 Conclusion

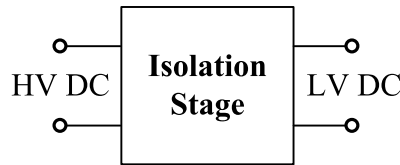
The CAR role within the SST, as a multi-level converter, as well as its modular design was briefly discussed. The single AR control-strategy expansion to facilitate CAR control was discussed. The control design was thus explained in terms of plant-model expansion followed by compensator redesign. Interleaved switching, its implementation and the effect thereof were discussed. Successful current- and voltage-loop integration was verified with time domain simulations. The simulations tested a CAR consisting of two ARs and verified natural voltage-balancing with equal loads as well as natural voltage rebalancing after an external perturbation. The expanded control system implementation within the MC and CCs was explained. The successful current- and voltage-loop implementation was confirmed through test measurements. Natural voltage-balancing with equal loads as well as natural voltage rebalancing after an external perturbation, were verified. The natural voltage rebalancing within the simulation results and test measurements were compared with the findings of Section 2.2 to confirm a very similar result. The outcome as described in this chapter, shows that the CAR control is ready to include the DC-DC converters to subsequently facilitate the three-phase SST.

# Chapter 6

## DC-DC Converter Control

### 6.1 Introduction

The isolation stage is the link between the high-voltage side and the low-voltage side of the SST and converts the HV DC to LV DC, as depicted in Figure 6.1. This conversion is accomplished with a DC-DC Converter (DC-DC) facilitating isolation between the primary and secondary of the SST.



**Figure 6.1:** Three Stage SST Concept: Isolation Stage

The multilevel-converter topology is maintained to manage the three HV total bus-voltages of the input stage. These outputs are connected as the isolation-stage inputs. Each HV total bus-voltage is split between  $N$  cascaded DC-DC converters, as depicted in Figure 6.2, which reduces the required blocking-voltage of each switch. The isolation-stage output consists of  $3 \times N$  DC-DC outputs, which are connected in parallel to facilitate the Three-Phase Inverter (TPI) bus-voltage,  $V_{ib}$ .

The proposed DC-DC control incorporates a double loop control scheme. The outer voltage loop controls the TPI bus voltage, at a predefined average value, by manipulating the current-loop reference. The current loop is implemented with three parallel current loops, one per isolation-stage phase. Each current-loop indirectly controls the average DC-DC output-current, by controlling the peak isolation-transformer input-current, within the DC-DC converters of the respective phase. This is an AC switched-current drawn from the respective cell bus to facilitate power transfer across the isolation transformer. The isolation-transformer AC output-current is rectified and filtered to produce the DC-DC output-current. Each current loop receives the same current-loop reference, which equally distributes the power delivered to the TPI bus, between the three isolation-stage phases.

Figure 6.3, from the left, depicts that the TPI bus-voltage feedback,  $v_{ib}$ , is compared with the constant voltage reference,  $V_{ibref}$ , to determine the voltage error,  $e_V$ . The error is converted by the voltage compensator,  $C_V$ , to determine the compensator-output signal,  $u_V$ , representing a total isolation-stage output-current command. This signal is divided by  $3N$  to determine the average DC-DC output current reference,  $i_{oref}$ , sent to the current loop of each phase.

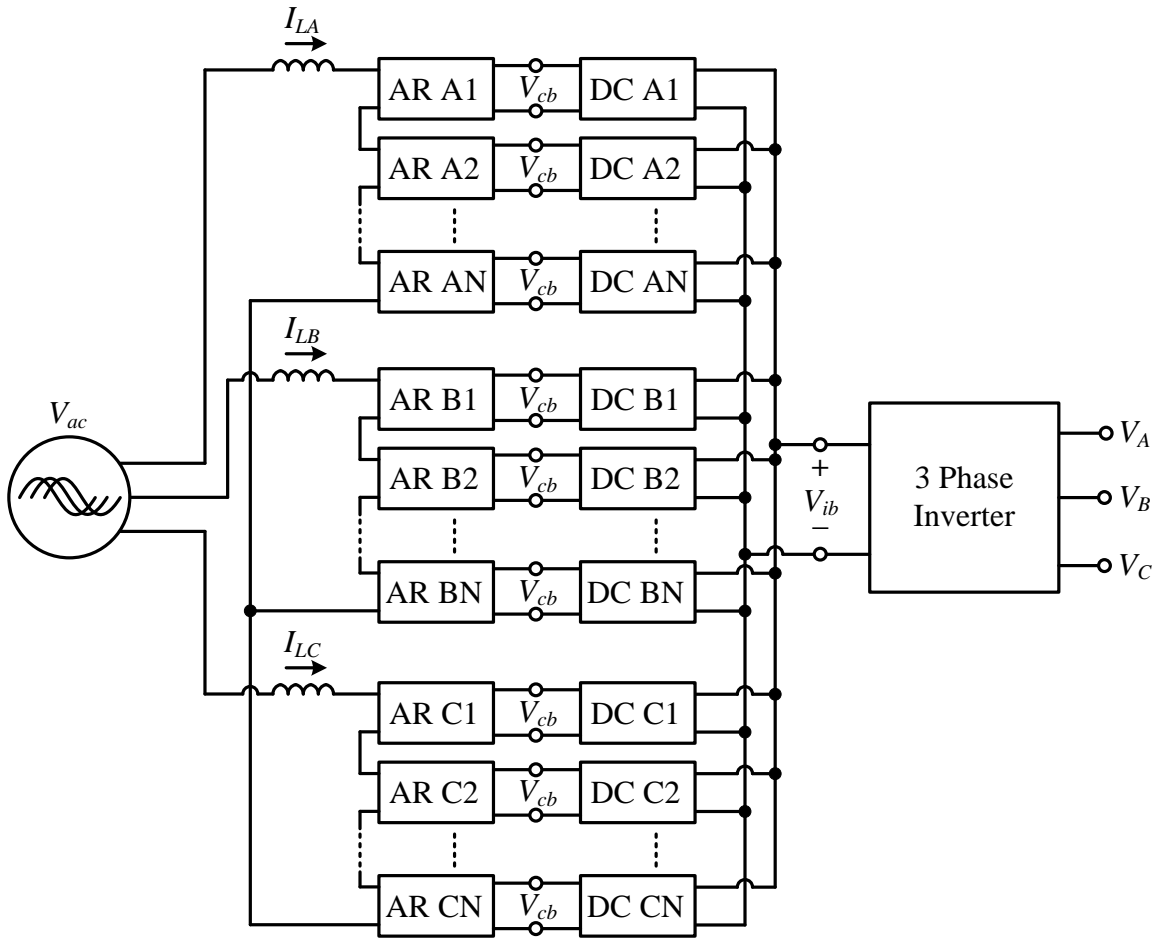


Figure 6.2: Three-Phase Back-To-Back Cascaded Active-Rectifier and DC-DC Converter Topology

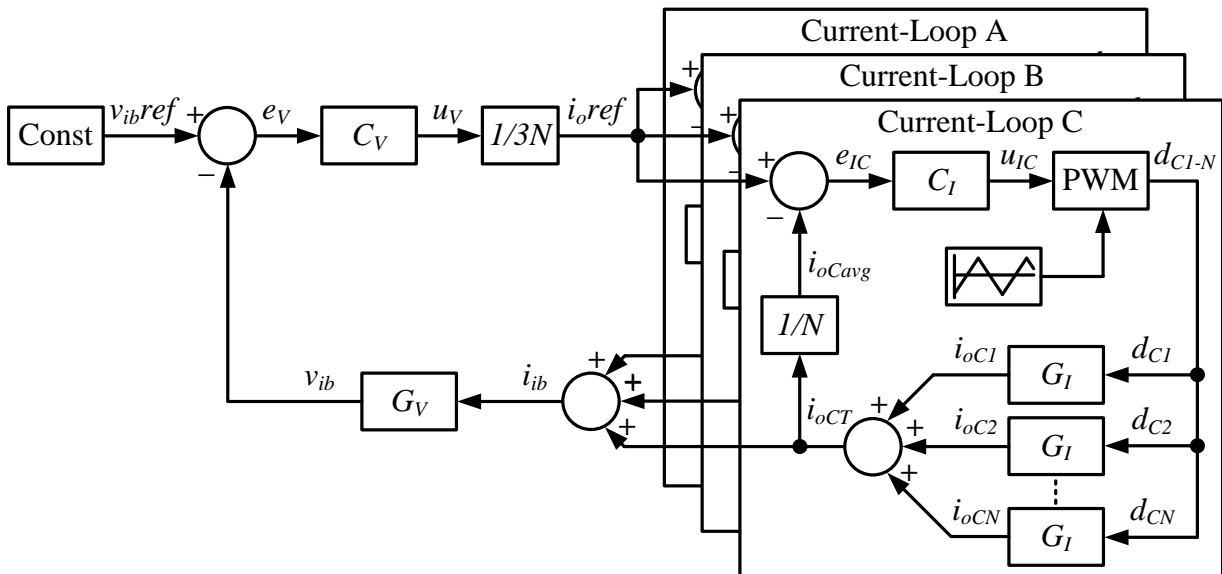


Figure 6.3: Double-Loop DC-DC Converter Control Scheme

Within each current loop,  $i_{oref}$  is compared with the average output-current feedback of the DC-DC converters in the respective phase,  $i_{oavg}$ , to determine the current error,  $e_I$ . The error is converted by the current compensator,  $C_I$ , to determine the compensator-output signal,  $u_I$ , representing a DC-DC duty cycle command. This signal is fed to the PWM where it is compared to  $N$  interleaved carrier-pairs to determine the DC-DC duty-cycles,  $d_{1-N}$ . The duty cycles are each fed to a current-loop plant,  $G_I$ , to determine the DC-DC output-currents,  $i_{o1-N}$ . The output currents are added to determine the total phase output current,  $i_{oT}$ , and divided by  $N$  to determine the average output-current feedback of the DC-DC converters in the respective phase,  $i_{oavg}$ . The added output currents of the three current loops,  $i_{oTA-C}$ , are added to determine the total isolation-stage output-current,  $i_{ib}$ . This current is fed to the voltage-loop plant,  $G_V$ , to determine the TPI bus-voltage feedback,  $v_{ib}$ .

In this chapter the methodology followed in designing the DC-DC control voltage-loop is thoroughly described. The current-loop is designed by [11] and thoroughly discussed in [12]. The control implementation is explained with emphasis on distinctive features. The DC-DC control is the final SST-control section which leads to SST test measurements. Test measurements of a scaled two-phase SST, a full-scale single-phase SST and a full-scale three-phase SST are presented and explained.

## 6.2 Control Design

The first step in control design is to characterise the system, including the controlled- as well as the control system. The controlled system characterisation involves defining models for physical components playing key roles within the system. The control system characterisation involves defining the capabilities of the hardware available for control implementation.

With regard to characterising the controlled system: Each DC-DC converter consists of a full-bridge converter, an isolation transformer, a passive rectifier and an output filter, as depicted in Figure 6.4. The filter outputs are connected, in parallel, to the TPI bus capacitor,  $C_{ib}$ . The resistive load,  $R_O$ , is added to the circuit to imitate power transfer from the isolation stage to the output stage. Each full-bridge converter consists of four switches,  $S_5 - S_8$ , each realised with an IGBT and controlled through its respective gating signal,  $g_5 - g_8$ .

With regard to characterising the control system: The DC-DC control is implemented within the same MCs and CCs used for CAR control implementation. The two control systems are implemented in parallel sharing communication between the MC and respective CCs. The communication between MCs is mainly used for DC-DC control.

In the remainder of this section the DC-DC control design is described in terms of the outer voltage loop shown in Figure 6.3. The process involves linearising the plant,  $G_V$ , and designing the compensator,  $C_V$ .

### 6.2.1 Voltage-Loop Plant Linearisation

The voltage-loop plant linearisation process involves the use of parameter values averaged over a relatively long period. This method is suitable because of the desired low voltage-loop bandwidth. The voltage loop can be analysed separately from the control scheme, shown in Figure 6.3, by treating the control components between the signals,  $u_V$  and  $i_{ib}$  as a unity gain. These components include the division by  $3N$ , the three current-loops and the total phase output-current summation. This substitution is possible when modelling the voltage loop, due to the relatively high current-loop bandwidth. The transition from  $u_V$  to  $i_{ib}$  has no impact on the voltage loop depicted in Figure 6.5.

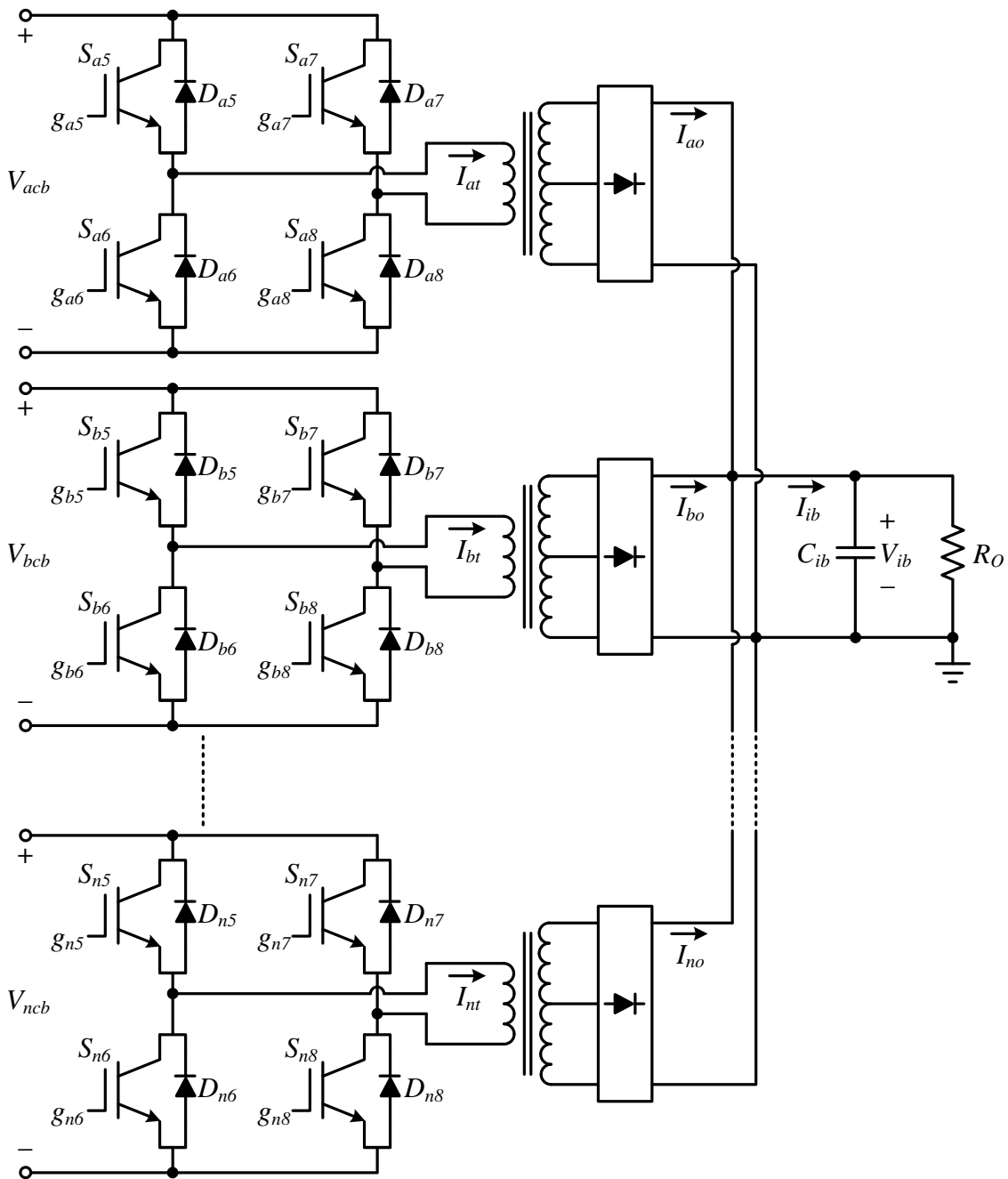


Figure 6.4: Cascaded DC-DC Converter Circuit Diagram

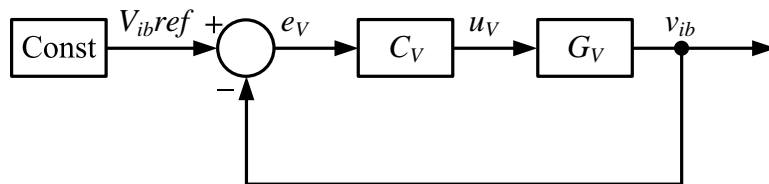
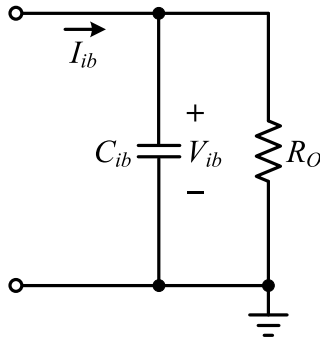


Figure 6.5: DC-DC Converter Voltage Loop

The voltage-loop plant transfer-function thus represents the  $v_{ib}$  response to  $i_{ib}$  variations. Straightforward circuit analysis of the TPI bus stage, as shown in Figure 6.6, yields:

$$G_V(s) = \frac{v_{ib}}{i_{cb}} = \frac{\frac{1}{C_{ib}}}{s + \frac{1}{C_{ib}R_O}} \tag{6.2.1}$$



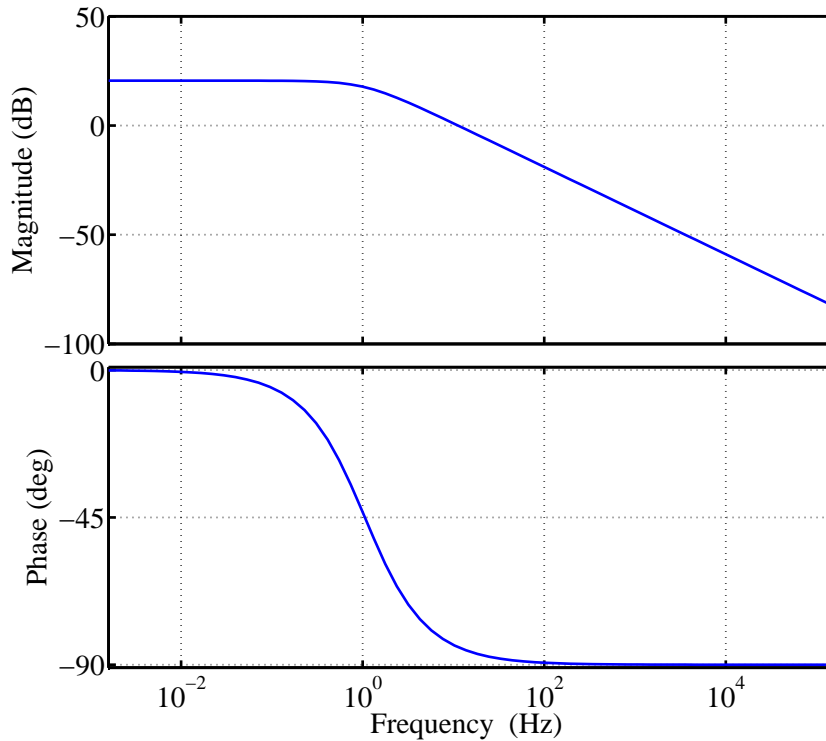
**Figure 6.6:** Three-Phase Inverter Bus-Stage Circuit Diagram

Table D.1 is used to quantify the transfer function as:

$$G_V(s) = \frac{70.92}{s + 6.647} \tag{6.2.2}$$

resulting in the frequency response, as shown in Figure 6.7, and a crossover frequency of:

$$f_{GV} = 15.9 \text{ Hz} \tag{6.2.3}$$



**Figure 6.7:** Frequency Response of the Voltage-Loop Plant Model,  $G_V(s)$

It is clear that the voltage-loop plant model is not dependent on the number of cells stacked within a phase or even on the number of phases incorporated in the SST. It is only dependent on the load value,  $R_O$ , because the TPI bus-capacitor value is fixed. The effect of load variations on the voltage-loop plant model is discussed in Appendix D.1.2.

## 6.2.2 Voltage-Loop Compensator Design

The outer voltage-loop controls the TPI bus-voltage value. The value is adjusted by adjusting the average output-current of the DC-DC converters. This current is indirectly adjusted by adjusting the peak isolation-transformer input-current. The voltage loop thus controls the power transfer from the cell-bus to the TPI-bus while the AR voltage-loop controls the power transfer from the input supply to the cell-bus. The two voltage loops thus influence each other and their respective bandwidths determine this influence.

The AR voltage-loop bandwidth has an upper limit to minimise the input-current second-order harmonic distortion. The DC-DC voltage-loop bandwidth has a lower limit to prevent extensive voltage-peaking when a TPI load-step occurs. This voltage-loop bandwidth also has an upper limit. The voltage-loop cannot be separated from the control scheme for analysis, as discussed in Section 6.2.1, if its bandwidth is too high. The voltage-loop bandwidth limitations and physical tests have led to the designed DC-DC voltage-loop bandwidth of more or less double the AR voltage-loop bandwidth, which is altered to the value discussed in Section 5.2.5.

In terms of power flow, the bandwidth ratio results in the following load step reaction: When a load step requires an increase in power, the DC-DC voltage-loop increases the current-loop reference and the current-loop, in turn, increases the DC-DC duty-cycle. This increases the power flow from the cell-bus to the TPI-bus. This power flow is limited by the power flow from the input supply to the cell-bus, governed by the AR voltage-loop. This results in DC-DC duty-cycle saturation until the input power has reached the desired value, after which the duty cycle resumes its controlled state. When a load step requires a decrease in power, the DC-DC voltage-loop decreases the current-loop reference and the current-loop, in turn, decreases the DC-DC duty-cycle. This decreases the power flow from the cell-bus to the TPI-bus. The power flow can be halted altogether when the current-loop decreases the DC-DC duty-cycle to zero. This causes the cell bus-voltage to increase until the input power has decreased to the desired value, after which the duty cycle resumes its controlled state. The bandwidth ratio thus results in a cell bus-voltage increase rather than a TPI bus-voltage increase. The voltage increase of each cell bus is acceptable because the total cell bus-voltage increase is distributed between the respective cells in the stack.

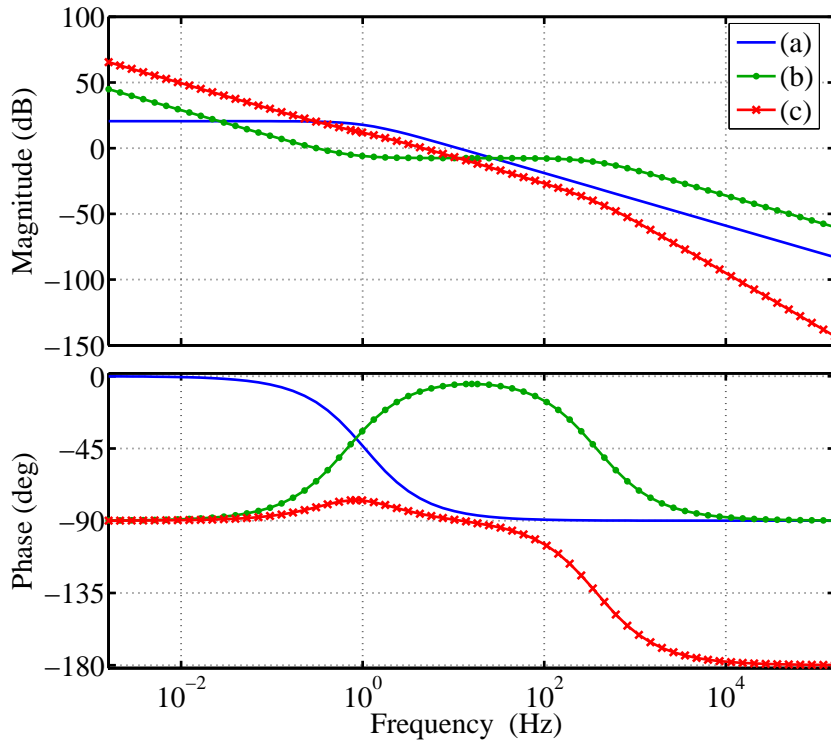
Graphical methods are used, utilising the MATLAB<sup>®</sup> SISO design tool to design the compensator. The compensator includes an integrator together with a pole at 377 Hz, to suppress noise spikes. A zero is placed at 0.672 Hz to provide a boost at low frequencies and the gain is set at 990 to achieve the desired bandwidth. The voltage-loop compensator is thus given as:

$$C_V(s) = 990 \times \frac{s + (0.672 \cdot 2\pi)}{s(s + (377 \cdot 2\pi))} = 990 \times \frac{s + 4.22}{s(s + 2370)} \quad (6.2.4)$$

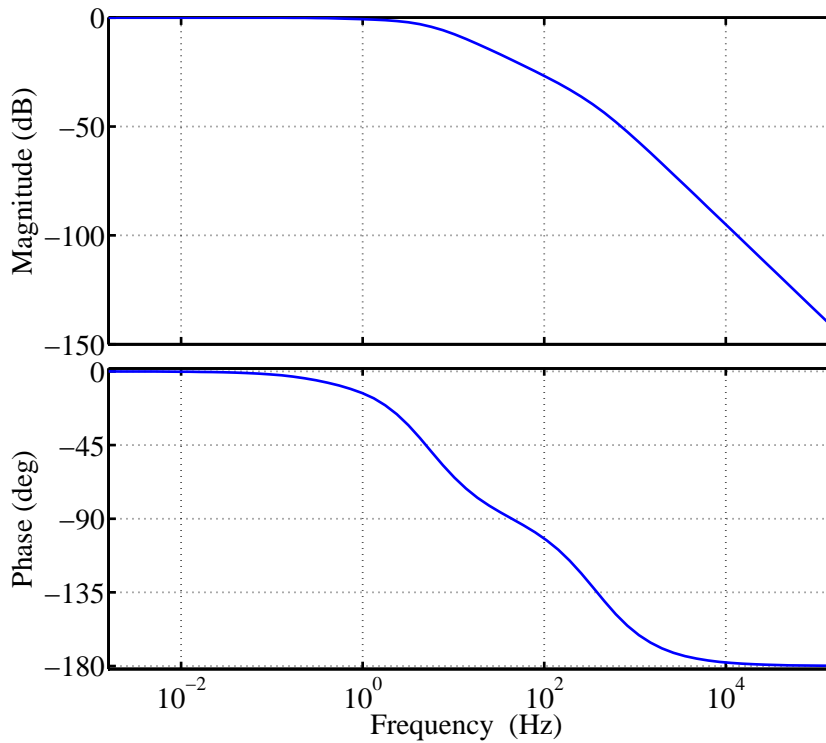
Figure 6.8 depicts the frequency response of the voltage-loop plant, compensator and open-loop system.

Figure 6.9 depicts the closed voltage-loop frequency response, resulting in a voltage-loop bandwidth of:

$$BW_V = 4.26 \text{ Hz} \quad (6.2.5)$$



**Figure 6.8:** Frequency Response of: (a)  $G_V(s)$ ; (b)  $C_V(s)$ ; (c)  $C_V(s) \cdot G_V(s)$



**Figure 6.9:** Closed-Voltage-Loop Frequency Response

The open voltage-loop response as well as the closed voltage-loop response are further analysed in Appendix D.1.3.



## 6.3 Control Implementation

The DC-DC control strategy is implemented, in parallel with the CAR control strategy, within the three MCs and  $3N$  CCs, as depicted in Figure 6.10 and 6.11. Each of the three current loops are jointly implemented within the MC and  $N$  CCs of the respective phase. The voltage loop is implemented within MCB<sup>1</sup> and feeds the current-loop reference directly to the MCB current-loop. MCB also feeds the current-loop reference, via a fibre-optic connection, to the MCA and MCC current-loops.

In the remainder of this section the DC-DC control implementation, the SST startup sequence and SST error handling are further described. Key components of each control loop are emphasized in terms of implementation techniques and hardware utilisation. Implementation challenges as well as their solutions, are also discussed.

### 6.3.1 Current-Loop Implementation

In this section a single current loop implemented in tripple, one within each phase, is described. The current loop is defined, in terms of implementation, as the control section from the current-loop reference,  $i_{oref}$ , to the gating signals,  $g_{a5-8} - g_{n5-8}$ <sup>2</sup>.

Each isolation-transformer input-current is measured by the respective CC using a LEM current-transducer and measurement circuit. These are AC measurements,  $i_t(t)$  with a frequency of  $f_s$ . This is the triangular-carrier frequency of 15 kHz. The measurement is sampled at 10 MHz by the respective ADC and scaled to a current value represented in ampere. This discrete measurement is processed to determine its peak values sent to the MC, in the DC-DC control allocation of the communication package. This package is sent as reply to any of the two control packages discussed in Section 5.4.1. The measurement hardware and processing is discussed in [12].

The MC updates its  $i_t(k)$  sample value from each CC, as the respective control-reply package is received. This means that  $i_t(k)$  from each CC is updated at eight fixed intervals every switching period, as shown in Figure 5.31, while in an interleaved fashion. The respective  $i_t(k)$  samples from each CC are added to determine the total isolation-transformer input-current measurement samples,  $i_{iT}(k)$ . These samples are divided by  $N$  and multiplied by  $Gain_I$  to determine the average DC-DC output-current measurement samples,  $i_{oavg}(k)$ . The summation and division are implemented within a single component and triggered by flags indicating when a new  $i_t(k)$  sample is received. This component is clocked at 10 MHz.  $Gain_I$  represents the relation between the isolation-transformer input-current and the DC-DC output-current.

The  $i_{oavg}(k)$  samples are subtracted from  $i_o(ref)$  to determine  $e_I$ , the input of the compensator,  $C_I(z)$ . The compensator design in the continuous-time domain, transformation to the discrete-time domain and the subsequent difference equation are discussed in [12]. The multiplication with  $Gain_I$ , the subtraction from  $i_o(ref)$  and the  $C_I$  difference equation are implemented in a single component clocked at 30 kHz.

The compensator output,  $u_I$ , is sent to all the CCs, in the DC-DC control allocation of the communication package. The DC-DC control communication, between the MC and respective CCs, is thus piggybacked on the AR-control communication consisting of two package types. The first is a synchronise package, sent at every down-slope of AR *carrier*1. This package contains a synchronise-carriers command, as well as the AR- $u_I$  and DC-DC- $u_I$  values at that moment in time. The second package type is a reference package sent at every interval excluding

<sup>1</sup>The capital letter 'A', 'B' and 'C' indicate the respective phase of the MC in question.

<sup>2</sup>The letters 'a', 'b', ..., 'n' indicate the number of the cell in question within the respective phase stack.

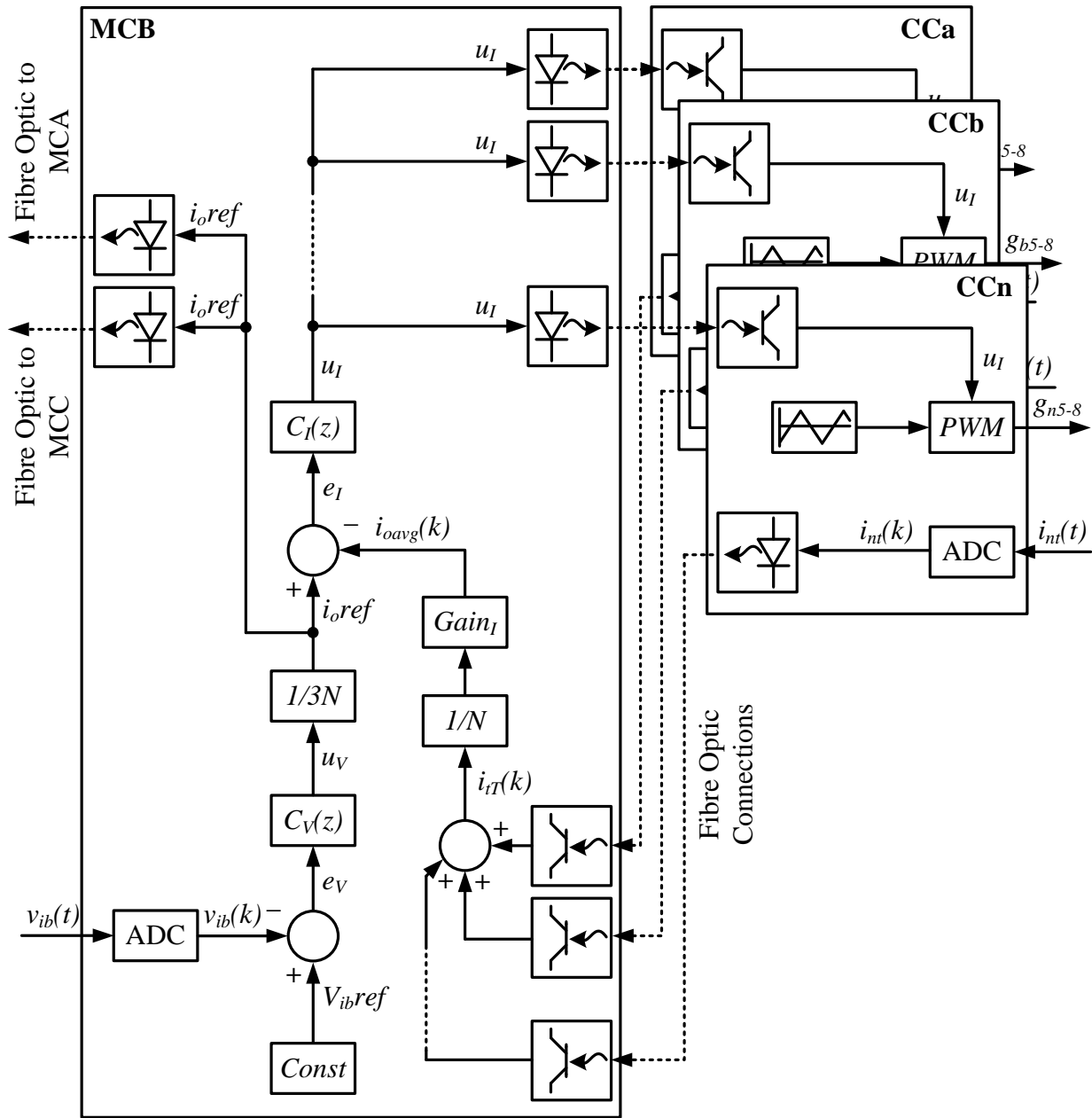


Figure 6.10: DC-DC Converter Control Implementation: MCB

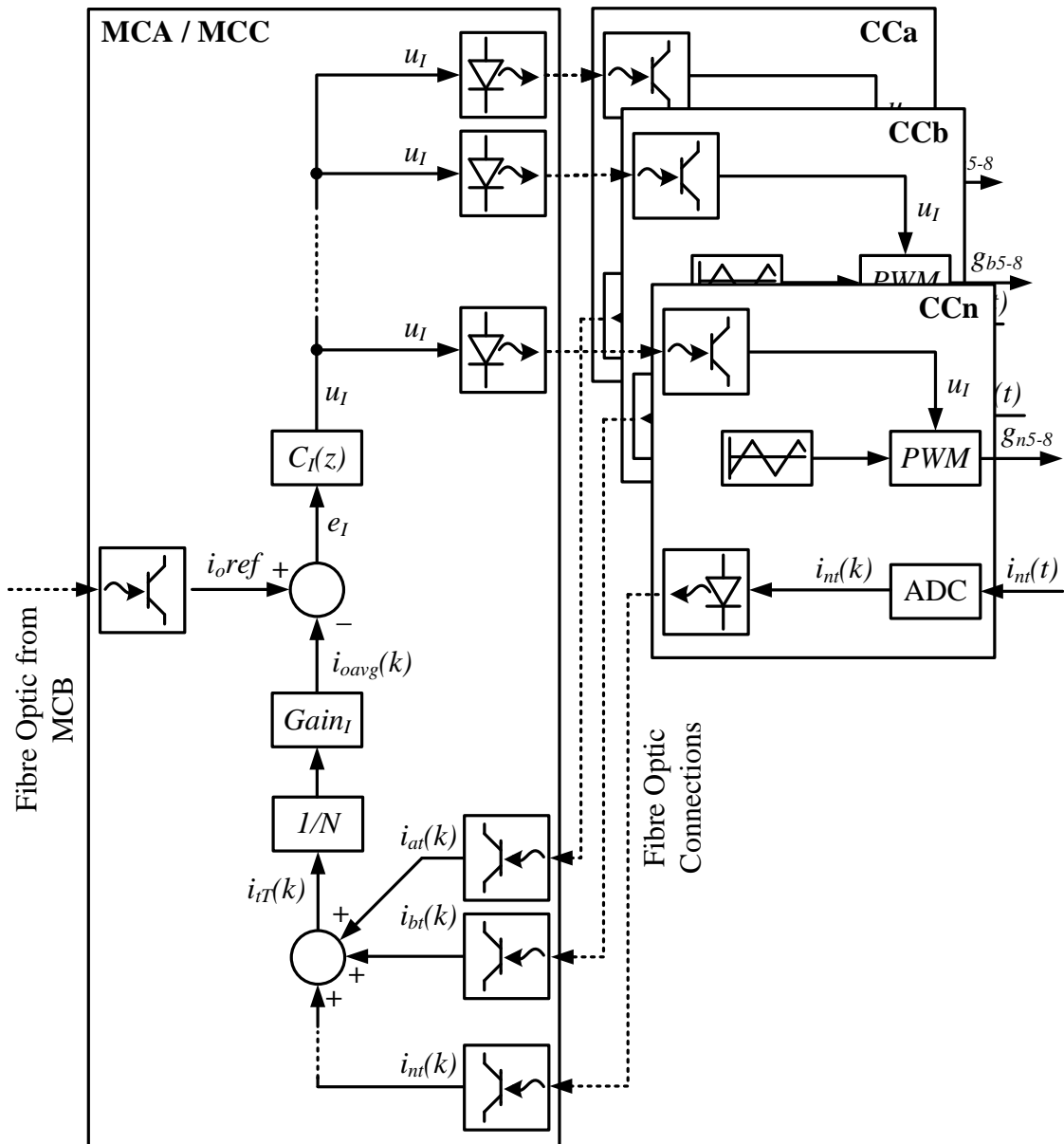


Figure 6.11: DC-DC Converter Control Implementation: MCA and MCC

the interval at the AR-carrier1 down-slope. This package contains a reference command, as well as the AR- $u_I$  and DC-DC- $u_I$  values at that moment in time.

When receiving a synchronise package<sup>3</sup>, the CC resets its AR carriers and DC-DC carriers and updates its AR- $u_I$  and DC-DC- $u_I$  values, whereas on receiving a reference package, the CC only updates its AR- $u_I$  and DC-DC- $u_I$  values. The DC-DC carriers of the respective CCs are thus also interleaved. To facilitate this interleaving, the AR- and DC-DC-carrier frequencies should match.

The final phase of the current loop is the PWM component implemented within each CC. The received DC-DC- $u_I$  value is compared to the DC-DC carriers to determine the gating signals,  $g_{5-6}$  which triggers the respective IGBT driver-circuits on the cell. The PWM component is also discussed in [12].

<sup>3</sup>The CC carriers are synchronised, at every MC AR-carrier1 down-slope, to prevent carrier drift between the MC and CC.

### 6.3.2 Volage-Loop Implementation

In this section the single voltage loop implemented within MCB is described. The voltage loop is defined, in terms of implementation, as the control section from the voltage-loop reference,  $V_{ibref}$ , to the current-loop reference,  $i_{oref}$ .

The discrete TPI bus-voltage measurement is received from the ADC, at a 200 kHz sample rate. Each sample is scaled to a voltage value represented in volts:

$$v_{ib}(k) = \frac{(ADC_{OUT} - 0x800)}{RATIO \cdot A2 \cdot A1} \quad (6.3.1)$$

The hexadecimal value, 0x800, is the zero-offset of the ADC output,  $ADC_{OUT}$ .  $RATIO$  is the ADC conversion ratio, as discussed in Appendix A.7.1.  $A1$  and  $A2$  are the op amp gains of the measurement PCB and secondary measurement-circuit, discussed in Appendix A.3.1 and A.6.1 respectively. Eq. 6.3.1 can thus be quantified as:

$$v_{ib}(k) = (ADC_{OUT} - 0x800) \times 441.856 \times 10^{-3} \quad (6.3.2)$$

The scaled samples are subtracted from  $V_{ib}(ref)$  to determine  $e_V$ , the input of the compensator,  $C_V(z)$ . This discrete compensator form is obtained by using the bilinear approximation together with the *c2d* function in MATLAB<sup>®</sup>. The bilinear approximation utilises the s-plane to z-plane mapping:

$$s = \frac{2}{T} \cdot \frac{z-1}{z+1} \quad (6.3.3)$$

where  $T$  is determined by the clock rate of the compensator component. Substitution of Eq. 6.3.3 into Eq. 6.2.4 yields the discrete compensator transfer function:

$$C_V(z) = 3.2161 \times 10^{-4} \times \frac{(z-0.9986)(z+1)}{(z-1)(z-0.9196)} \quad (6.3.4)$$

This transfer function leads to the difference-equation compensator form:

$$\begin{aligned} u_V(k) = & -0.9196u_V(k-2) + 1.9196u_V(k-1) - 3.1826 \times 10^{-4}e_V(k-2) \\ & + 3.3503 \times 10^{-6}e_V(k-1) + 3.2161 \times 10^{-4}e_V(k) \end{aligned} \quad (6.3.5)$$

which is implemented in the compensator component, clocked at 1.5 kHz. The compensator output  $u_I$  represents a total DC-DC output-current command which is divided by  $3N$  to determine the average DC-DC output-current reference,  $i_{oref}$ . The subtraction to determine  $e_V$  and the division by  $3N$  is also implemented in the compensator component.

The current-loop reference is fed directly to the MCB current-loop and fed via fibre-optic connections to the MCA and MCC current-loops. The reference is sent in the DC-DC control allocation of the communication package. The package contains a DC-DC-reference command and the  $i_{oref}$  value at that point in time. It is sent to both MCA and MCC, eight times every switching period, as shown in Figure 5.31. The communication to both MCs is synchronised relative to the  $AR\_carrier_a1$ . As MCA and MCC receive this package, they reply with a package containing only the DC-DC-reference command. This reply also acts as a communication functionality check. MCB reacts if this reply is not received, within a predefined time, after a DC-DC-reference package was sent. MCB assumes communication loss and moves to an error state.

### 6.3.3 Startup Sequence

The startup sequence is defined as the sequence of events to start up the SST, from system power-up, to AR- and DC-DC-control enable, to AR- and DC-DC-shutdown. The sequence is shown in Figure 6.12. Each CC is programmed with a *.jic* file which means its FPGA is automatically programmed at every power-up. This necessitates the firmware revision check. Each MC is programmed with a *.sof* file which means its FPGA is programmed manually at every power-up.

The startup sequence is led by MCB, which is programmed after MCA and MCC. This triggers the start command and a time delay for the operator to do a quick visual system check. MCB then triggers the ping state, by sending a ping package to MCA and MCC to confirm successful communication with a reply ping-package. If a reply ping-package is not received within a predefined time, a second ping package is sent. A maximum of five ping packages are sent at one second intervals before a Ping-Error is triggered and the startup process is terminated. Once a reply ping-package is received from both MCA and MCC, MCB sends a ping-cell package instructing the MCs to ping the CCs in their respective phase. At this stage MCB also pings the CCs in phase B. The cell ping process is discussed in Section 4.4.3. The input relay is opened by MCA as soon as it enters the ping state.

Once all reply ping-packages have been received, MCB triggers the initialise state, by sending an initialise-cell package to MCA and MCC instructing the MCs to initialise the CCs in their respective phase. At this stage MCB also initialises the CCs in phase B. The cell initialise process is discussed in Section 4.4.3. The Detect-Cell-Bus-Voltage-Measurement-Offset package is sent as part of the initialise process, instructing each CC to detect the zero offset of its  $v_{cb}$  measurement circuit. A DC-DC dump is triggered, prior to the offset measurement, to dump the energy stored in the cell bus-capacitors to the output load. The DC-DC converters are enabled with a ramped duty-cycle and the measurement offset is taken after a predefined dumping period. Once all initialise package-replies have been received, the active state is triggered and MCA closes the input relay. Otherwise a Reply-Lag-Error is triggered and the startup-process is terminated.

The active state is where the ARs and DC-DC converters physically start up. A specific startup sequence is necessary to prevent undesirable current peaks, as mentioned in Section 4.3.1 and 4.3.2. A second physical occurrence responsible for the specific startup sequence, is bus-voltage imbalance. The non-linearities and component differences within the cell are influenced by power flow, as discussed in Section 6.4.1. The key is to precharge the cell bus-capacitors while driving a load. The DC-DC converters are thus operated at constant duty cycle, before AR- and DC-DC-control is enabled. Power flow from input to load is thus insured while charging the cell bus-capacitors with diode currents. Bus-voltage imbalance, in-rush currents and the initial error signal of the AR voltage loop,  $e_V$ , are minimised. The MCs regularly send Requesting-Bus-Voltage packages to the CCs, to check the  $v_{cb}$  measurements.

Once the average  $v_{cb}$  measurement of all three phases reach a predefined value, the cell bus-capacitors are perceived as precharged and the Start-Control command is given. Up until this stage the DC-DC converters have not been interleaved and are disabled. The AR-component responsible for synchronising the unit-sinusoid, is then enabled. After three successfully synchronized cycles, the MC AR-control components are enabled and an enable-AR package is sent to each CC. From this point the MCs continually send AR-control packages to the CCs in their respective phase, as discussed in Section 5.4.1. This facilitates the control of  $V_{cbTA}$ ,  $V_{cbTB}$  and  $V_{cbTC}$  at a certain average value, while drawing three sinusoidal input-currents,  $i_{LA}$ ,  $i_{LB}$  and  $i_{LC}$ . With AR-control startup, the average  $v_{cb}$  measurements increase to the desired value. As these measurements reach a predefined value, the DC-DC control is enabled. Each

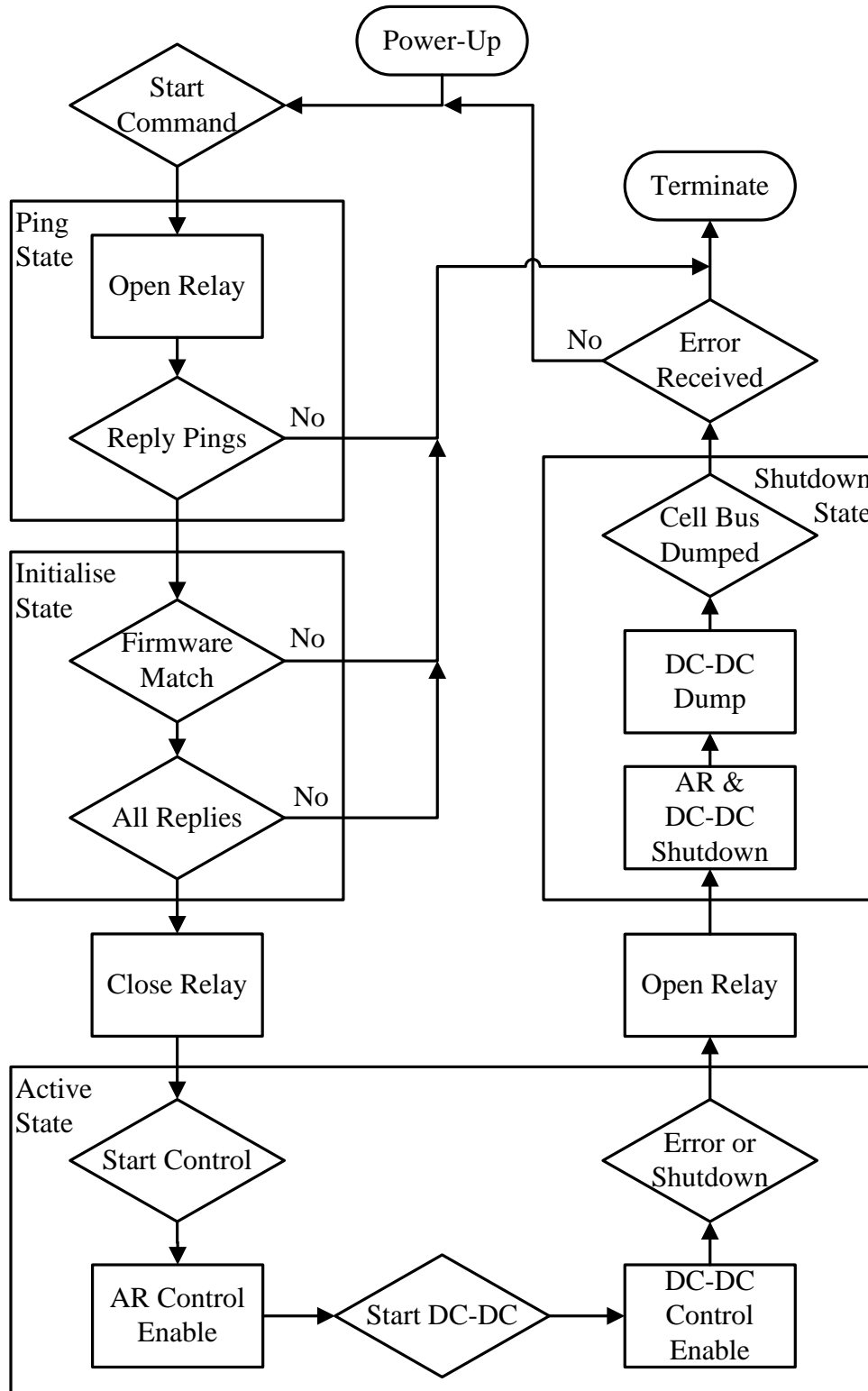


Figure 6.12: SST Startup Sequence

MC enables its DC-DC-control components and sends an enable-DC-DC package to the CCs in its respective phase. From this point the DC-DC control communication is piggybacked onto the AR-control communication and MCB continually sends the  $i_{o,ref}$  value to MCA and MCC. The  $V_{ib,ref}$  value is ramped from the current  $v_{ib}$  value to the desired  $v_{ib}$  value. This reference ramp ensures a relatively smooth startup by gradually increasing the delivered output power.

The SST remains in operation until a shutdown is triggered or any of the errors mentioned in Section 6.3.4 occur. This triggers the shutdown state and MCA opens the input relay, disconnecting the input voltage. The MCs send a shutdown package to the CCs in their respective phase. This command triggers each CC to shut down its AR and DC-DC converter by disabling its control components and opening all switches. The MCs then send a DC-DC-dump package which triggers the CCs to enable the DC-DC converters and ramp their respective duty cycles while the ARs are disabled. This process dumps the energy stored in the cell bus-capacitors to the output load. The MCs check the respective  $v_{cb}$  values and disable the process when they have dropped to a predefined value. If the shutdown was triggered by the operator reducing the input voltage to a predefined value, the system resets and waits for the next start command. On the other hand, if the shutdown was triggered by an error, the system terminates. At this stage the operator should determine the cause of the error and rectify the problem.

### 6.3.4 Error Handling

SST errors can be classified as measurement errors and system errors. Measurements errors are defined as measurements exceeding predefined limits and system errors are defined as system malfunction. All measurements are checked for measurement errors. The measurements checked by each CC, for SST implementation, are:

- Cell Bus-Voltage,  $V_{cb}$
- Isolation-Transformer Input-Current,  $I_t$
- Isolation Transformer Temperature,  $T_t$
- IGBT Heat Sink Temperature,  $T_{sink}$
- Isolated Power Supply Voltage,  $V_{ips}$

The measurements checked by each MC, for SST implementation, are:

- Input Voltage,  $V_{ac}$
- Input-Inductor Current,  $I_L$
- Cell Bus-Voltage,  $V_{cb}$
- Cell Bus-Voltage imbalance
- TPI Bus-Voltage,  $V_{ib}$ <sup>4</sup>

The system errors handled by each MC are:

- **SCI Read Data Error:** When the SCI component indicates that a package could not be read successfully.

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<sup>4</sup> $V_{ib}$  is only measured and checked by MCB.



- **Firmware Revision Number Mismatch:** When the firmware revision, programmed on a CC, does not match the firmware revision required by the MC.
- **Ping Error:** When an MC or CC does not echo the ping package sent at system startup.
- **Command Mismatch:** When any reply-package command received from an MC or CC does not match the package command sent by the MC.
- **Reply Lag Error:** When any reply package from a CC is not received within the predefined time. The communication between MCs is also monitored.

With the occurrence of a CC measurement error during the active state, the respective CC sends an error package to the MC in its phase, with an error indicating command. When any of the MC measurement- or system-errors occur during the active state, or when an error package is received from any respective CC, the error is relayed to the other MCs and a shutdown state is triggered, as discussed in Section 6.3.3. The SST is thus shut down before any system damage or operator danger can arise.

## 6.4 Test Measurements

Physical tests were performed to verify control-system functionality as a whole as well as natural cell bus-voltage balancing within each phase and input- and output-current balancing. All distinct aspects of the control system are also separately checked to establish proper functioning. These aspects include: all measurements, implemented compensators and other control components, communication between the MC and respective CCs and between respective MCs. The measurements taken vary between Signal-Tap measurements, as described in Section 4.5, and oscilloscope measurements. The Tektronix TDS 3014 Oscilloscope is used with a bandwidth of 100 MHz, capable of a 1.25 GS/s sample rate.

### 6.4.1 Two-Phase Scaled SST Test Measurements

The two-phase SST test, is where two-phase AC inductor-currents,  $I_{LA}$  and  $I_{LB}$ , are drawn from two-phase AC input voltages,  $V_{acA}$  and  $V_{acB}$ , to maintain the two bus-voltages,  $V_{cbA}$  and  $V_{cbB}$ , at a specific average value. Two HF currents,  $I_{tA}$  and  $I_{tB}$ , are drawn from these buses, transformed, rectified and filtered to the output-currents,  $I_{oA}$  and  $I_{oB}$ . The average of these currents are controlled to maintain a specific average TPI bus-voltage,  $V_{ib}$ . The test is aimed at verifying successful DC-DC control implementation as well as active output-current balancing with an output-parallel load. The physical test setup, as depicted in Figure 6.13, is discussed in Appendix D.2.1.

Figure 6.14 depicts the  $i_{LA}$  and  $i_{LB}$  steady-state oscilloscope measurement on the left and a detailed result on the right. Both currents have a superb sinusoidal waveform. The amplitude of  $i_{LA}$  is larger than that of  $i_{LB}$  because the bench variac does not supply perfectly balanced 3-phase voltages. In this case,  $v_{acB}$  has a higher value than  $v_{acA}$ . Due to equal AR voltage-loop references on both MCs, a larger  $i_L$  is drawn from the lower  $v_{ac}$  to achieve the same  $v_{cb}$  value.

Figure 6.15 depicts the  $v_{cbA}$  and  $v_{cbB}$  steady-state oscilloscope measurement on the left and a detailed result on the right. The measurement shows a 6-7 V imbalance as well as an offset from the  $V_{cbref}$  values. The differential probes used with oscilloscope measurements are prone to measuring a slight offset, as mentioned in Section 5.5.1. The 100 Hz voltage ripple is clearly visible with an expected 120° phase shift between the two cell bus-voltages.



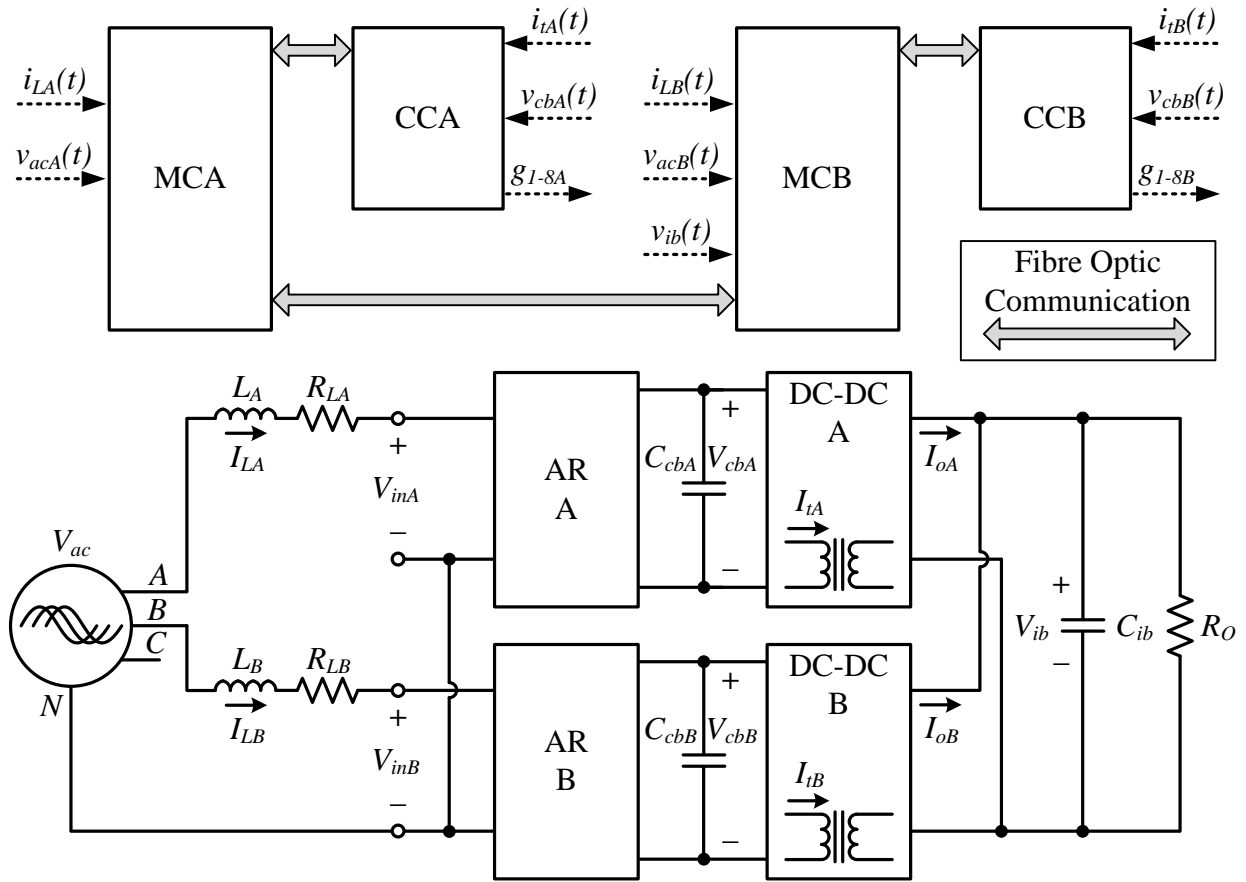


Figure 6.13: Two-Phase SST Test Setup

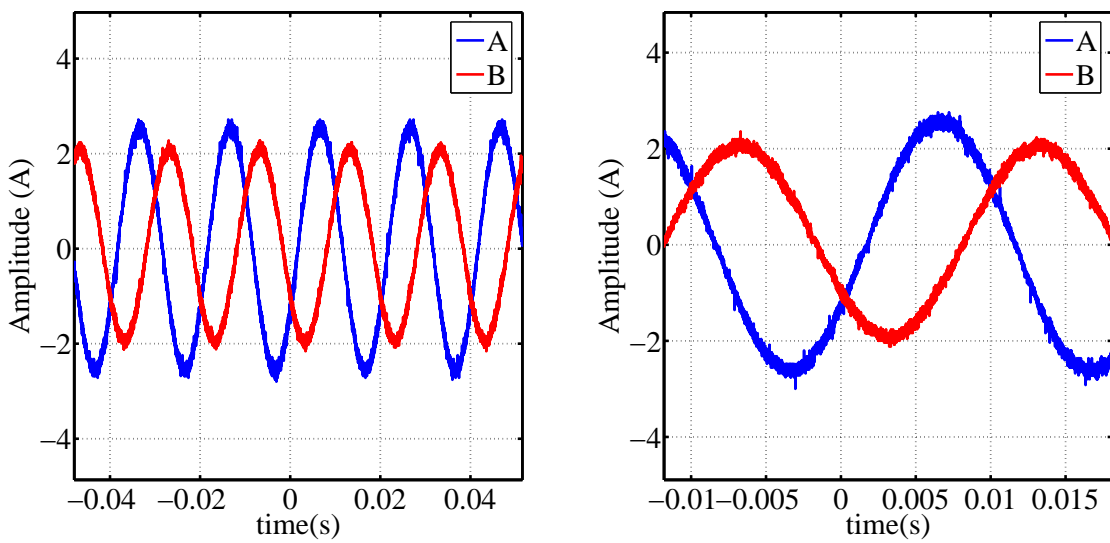
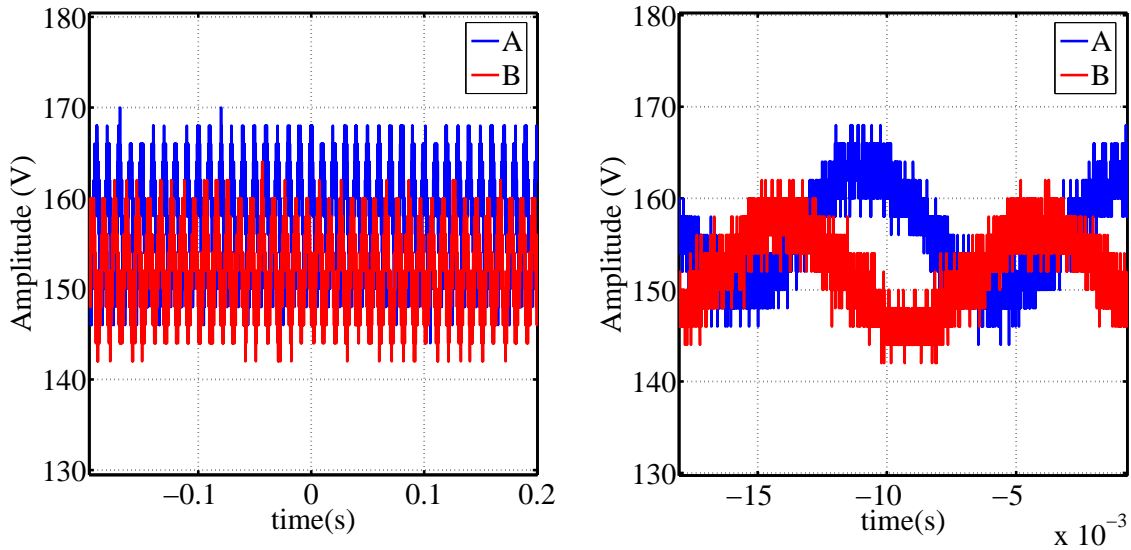
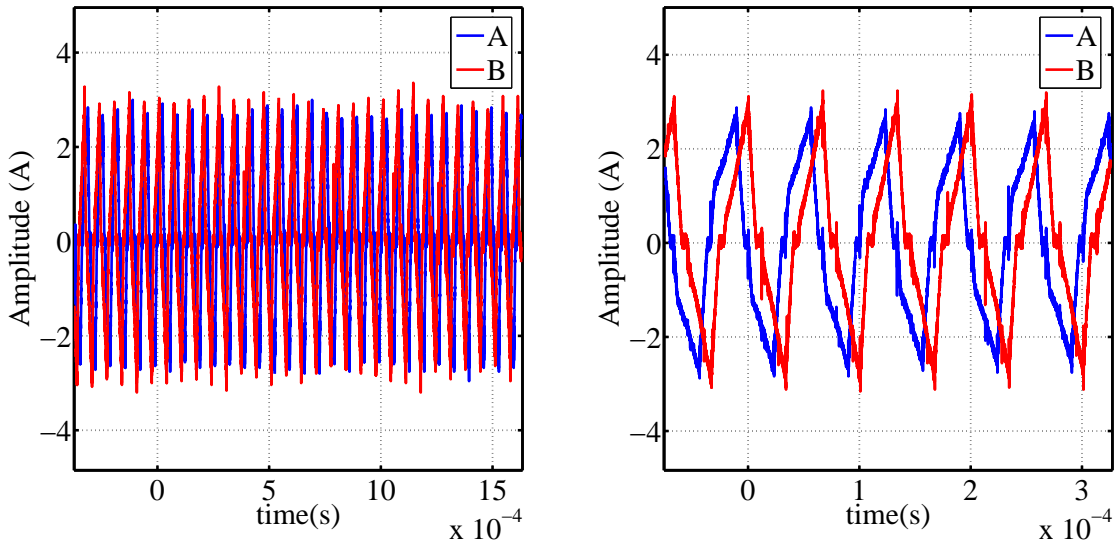


Figure 6.14: Oscilloscope Measurement: Input Inductor-Currents



**Figure 6.15:** Oscilloscope Measurement: Cell Bus-Voltages

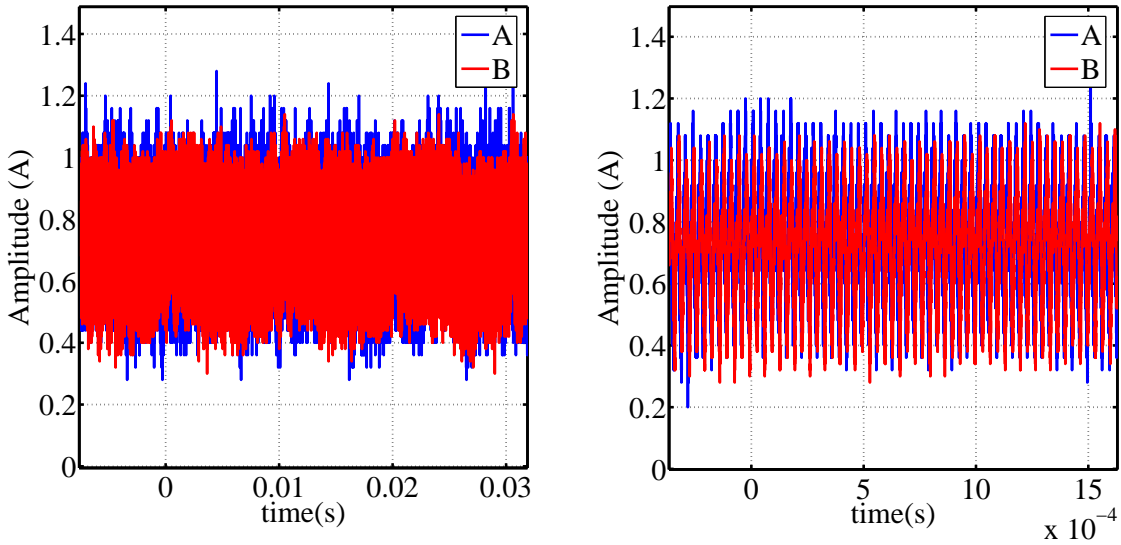
Figure 6.16 depicts the  $i_{tA}$  and  $i_{tB}$  steady-state oscilloscope measurement on the left and a detailed result on the right. These are the HF AC-currents drawn from the cell buses. The amplitudes of the currents are quite well matched, however they drift compared to each other. This is because the carriers of each CC are synchronised with the carriers of the respective MC. The carriers of the MCs are however not synchronised with each other and the MCs exhibit slight clock-oscillator drift.



**Figure 6.16:** Oscilloscope Measurement: Isolation-Transformer Input-Currents

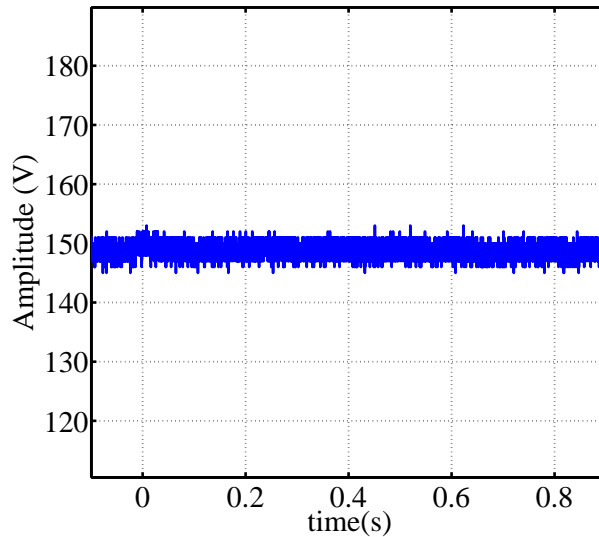
Figure 6.17 depicts the  $i_{oA}$  and  $i_{oB}$  steady-state oscilloscope measurement on the left and a detailed result on the right. The current amplitudes are well matched, however not as well matched as the  $i_t$  currents. This is because the  $i_t$  currents are directly controlled after which they are transformed by the isolation-transformer, rectified and filtered by the output filter of each respective DC-DC converter. There are DC-DC components that have significant value differences from one DC-DC converter to another. Examples of these components are the

isolation-transformer and filter inductors. This leads to a slight differences in current transformation from  $i_t$  to  $i_o$ . There are other effects caused by these component differences which are discussed later in this section and in sections to follow.



**Figure 6.17:** Oscilloscope Measurement: DC-DC Output-Currents

Figure 6.18 depicts the  $v_{ib}$  steady-state oscilloscope measurement. The output bus-voltage has a satisfactory stable DC value compared to  $V_{ibref}$ .



**Figure 6.18:** Oscilloscope Measurement: DC-DC Output Bus-Voltage

Figure 6.19 depicts the  $v_{inA}$  and  $v_{inB}$  steady-state oscilloscope measurement on the left and a detailed result on the right. The result clearly shows three voltage levels with the 100 Hz representation of the respective cell bus-voltage ripples also visible. This number of voltage levels is expected from two single ARs, as shown in Eq. 5.2.7.

A second and third measurement test are presented, aimed at verifying acceptable DC-DC converter operation during load steps in terms of the output-voltage response and the output-current balancing response. The second test introduces an  $R_O$  step, of 110  $\Omega$  to 267  $\Omega$ . This

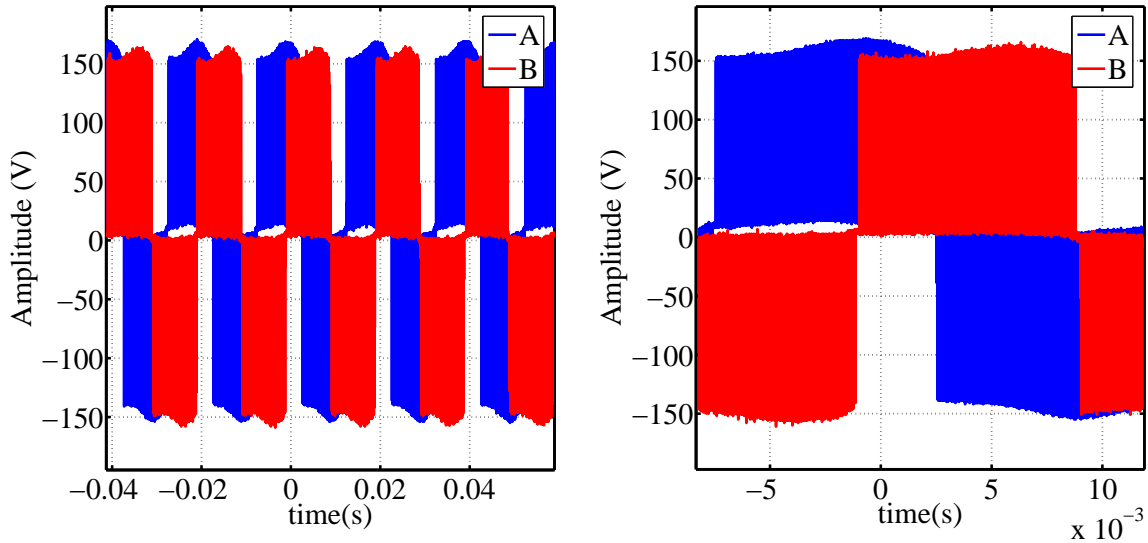


Figure 6.19: Oscilloscope Measurement: Input Switched Voltages

decreases the power delivered to the load by  $\pm 60\%$ . Figure 6.20 depicts the oscilloscope measurement of the  $v_{cbA}$  and  $v_{cbB}$  transient response on the left and the detailed result on the right. The cell bus-voltages have a result relatively similar to the single AR result shown in Appendix B.5.4. The two cell bus-voltages do however, show a difference in transient amplitude. The hypothesis is that this is caused by DC-DC component differences mentioned earlier. The differences include, among others, the isolation-transformer leakage-inductance and the filter inductor values. The isolation-transformer leakage-inductance has a power-related effect on the effective DC-DC duty-cycle. The filter-inductor differences cause discontinuous inductor-currents at different power levels.

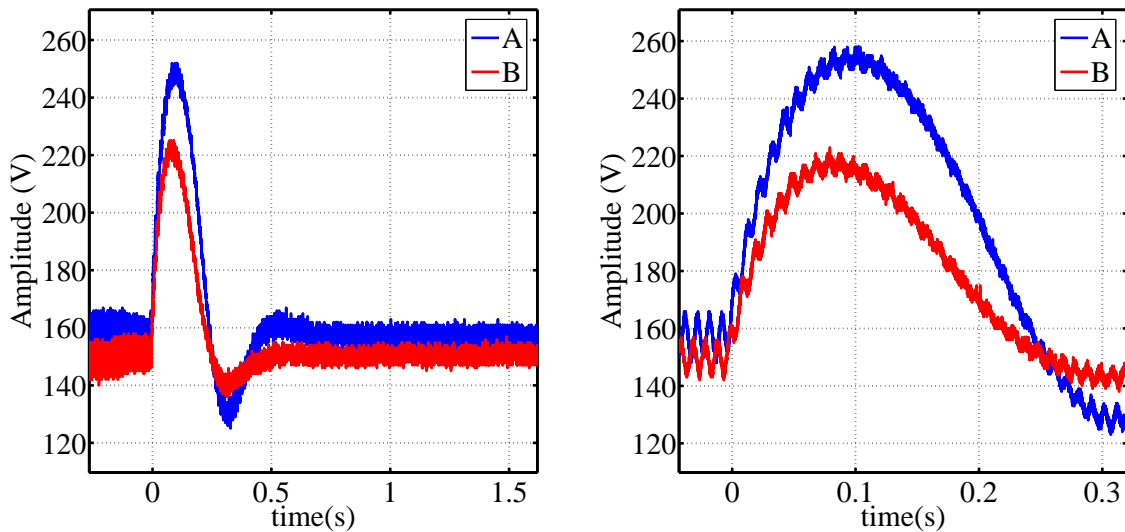
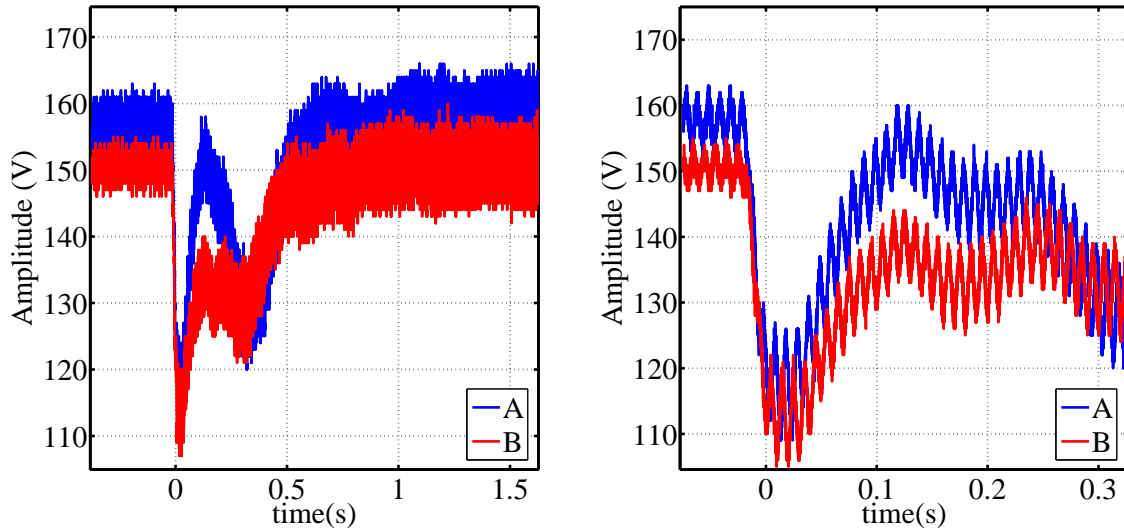


Figure 6.20: Oscilloscope Measurement: Cell Bus-Voltages

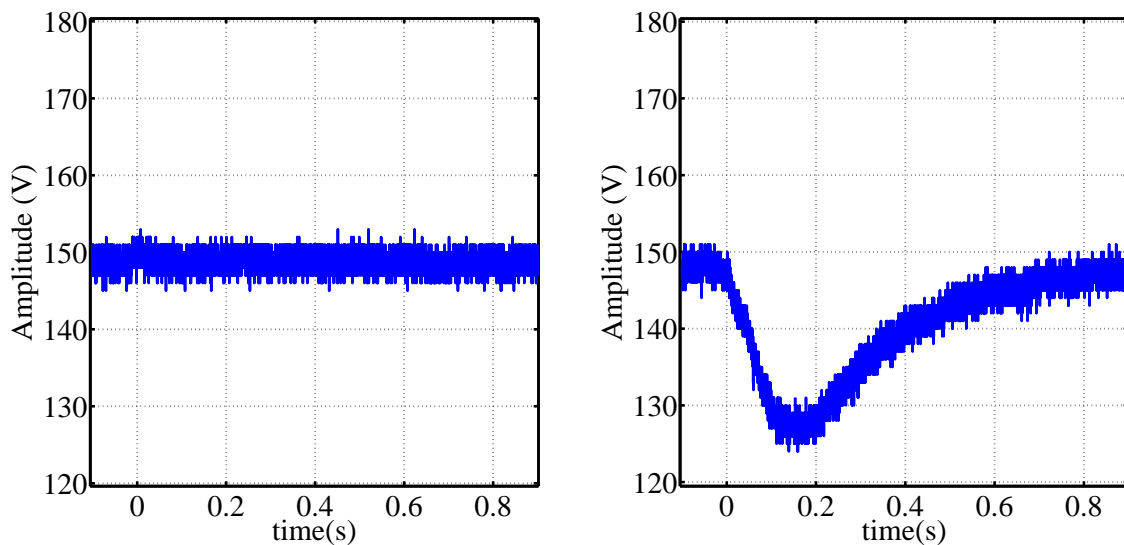
The third test introduces an  $R_O$  step, of  $267\ \Omega$  to  $110\ \Omega$ . This increases the power delivered to the load by  $\pm 140\%$ . Figure 6.21 depicts the oscilloscope measurement of the  $v_{cbA}$  and  $v_{cbB}$  transient response on the left and the detailed result on the right. The cell bus-voltages have an exaggerated result compared to the single AR result shown in Appendix B.5.4. This is

because the DC-DC voltage-loop cannot maintain the required  $v_{ib}$  value, as shown on the right of Figure 6.22. The DC-DC duty-cycles are increased to their limit to keep this voltage from dropping. The AR voltage-loops thus compete with the DC-DC voltage-loop for a brief period. The two cell bus-voltages again show the effect of component differences.



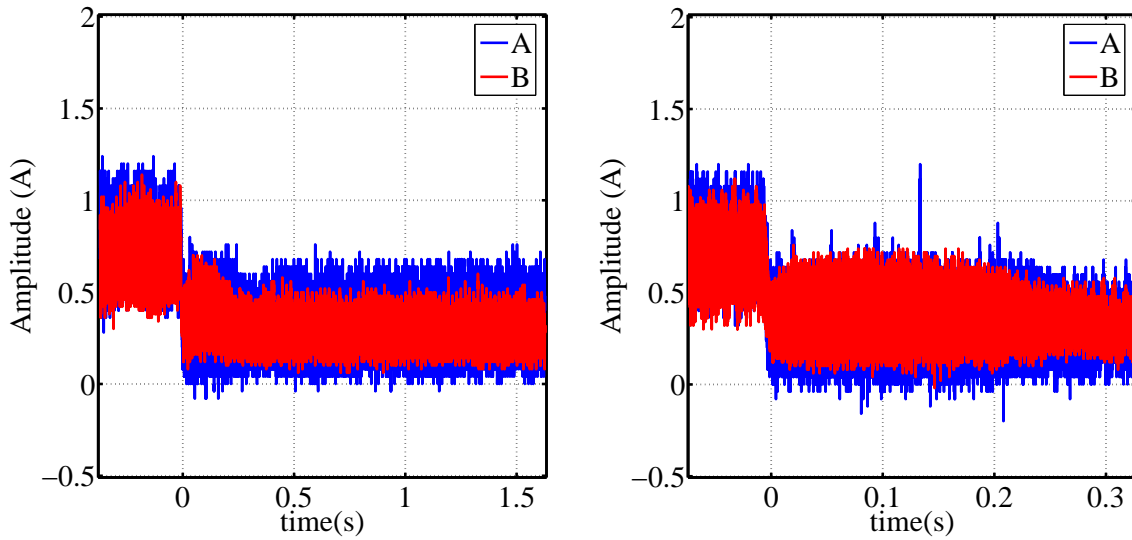
**Figure 6.21:** Oscilloscope Measurement: Cell Bus-Voltages

Figure 6.22 depicts the oscilloscope measurement of the  $v_{ib}$  transient response of the second test on the left and of the third test on the right. The second test result shows an excellent seemingly constant transient response. This is because the DC-DC duty-cycles can be lowered to zero to prevent the cell bus-voltage transient effects from propagating to the output voltage. The third test result, on the other hand, shows the bus-voltage transient effects because the DC-DC duty-cycles can only be increased to a predefined value.



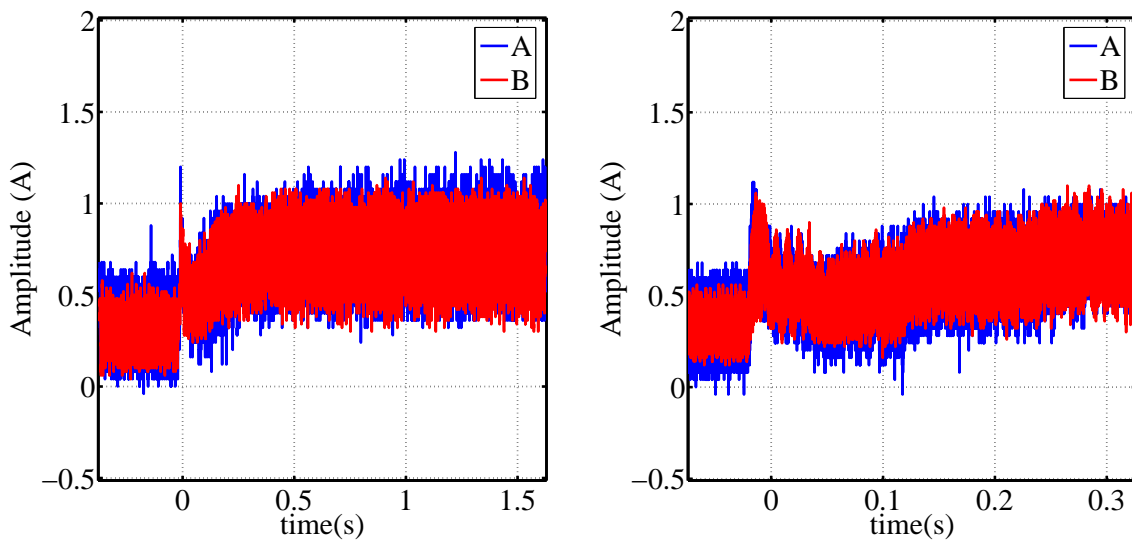
**Figure 6.22:** Oscilloscope Measurement: DC-DC Output Bus-Voltage

Figure 6.23 depicts the second test oscilloscope measurement of the  $i_{oA}$  and  $i_{oB}$  transient response on the left and the detailed result on the right. An excellent step transient is achieved because of the zero DC-DC duty-cycles discussed above.



**Figure 6.23:** Oscilloscope Measurement: DC-DC Output-Currents

Figure 6.24 depicts the third test oscilloscope measurement of the  $i_{oA}$  and  $i_{oB}$  transient response on the left and the detailed result on the right. An acceptable transient is achieved with an increased step-time due to the limited DC-DC duty-cycles discussed above.



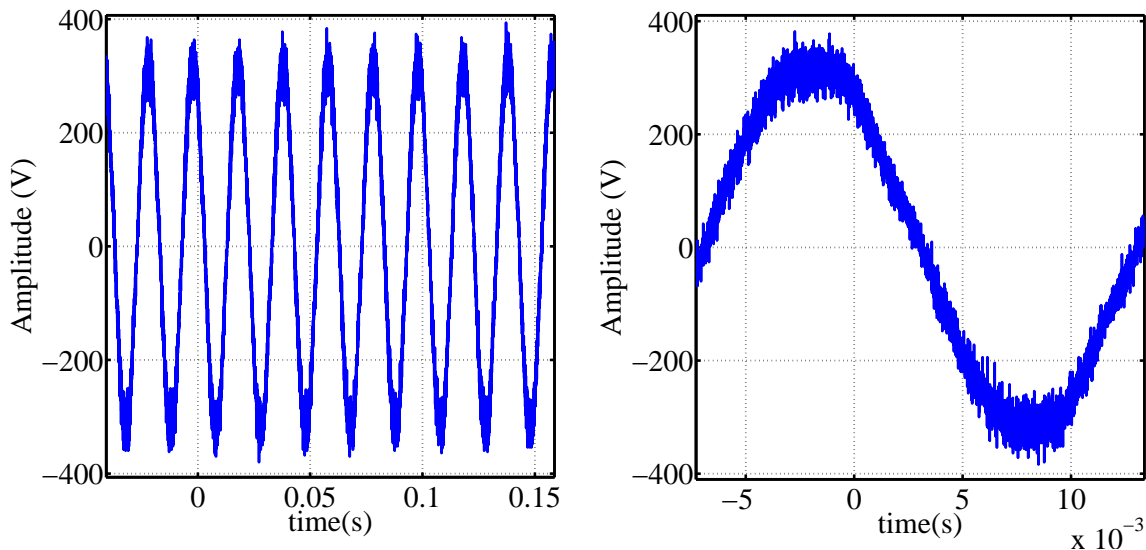
**Figure 6.24:** Oscilloscope Measurement: DC-DC Output-Currents

The measurements obtained are satisfactory in determining successful DC-DC control implementation and active output-current balancing. Satisfactory results are obtained during load-steps, in terms of the output-voltage response and the output-current balancing response.

### 6.4.2 Single-Phase Full-Scale SST Measurements

The single-phase full-scale SST test is where an AC inductor-current,  $I_L$ , is drawn from an AC input voltage,  $V_{ac}$ , to maintain a total bus-voltage,  $V_{cbT}$ , at a specific average value. Twelve HF currents,  $I_{at} - I_{lt}^5$ , are drawn from twelve buses, transformed, rectified and filtered to the output-currents,  $I_{ao} - I_{lo}$ . These currents add up to the total output-current,  $I_{oT}$ , which is indirectly controlled to maintain a specific average TPI bus-voltage,  $V_{ib}$ . The test is aimed at verifying successful single-phase full-scale SST operation at rated input-voltage as well as successful addition of the TPI and three-phase output load. The physical test setup is discussed in Appendix D.2.2.

Figure 6.25 depicts the  $v_{ac}$  steady-state oscilloscope measurement on the left and a detailed result on the right. The supply voltage indicates limited deformation with switching ripple propagated through the step-up transformer. The measurement also shows a line-neutral peak value of  $\pm 325$  V which indicates a line-line voltage of 400 V. This is then stepped up to a rated line-line input-voltage of 6.6 kV.

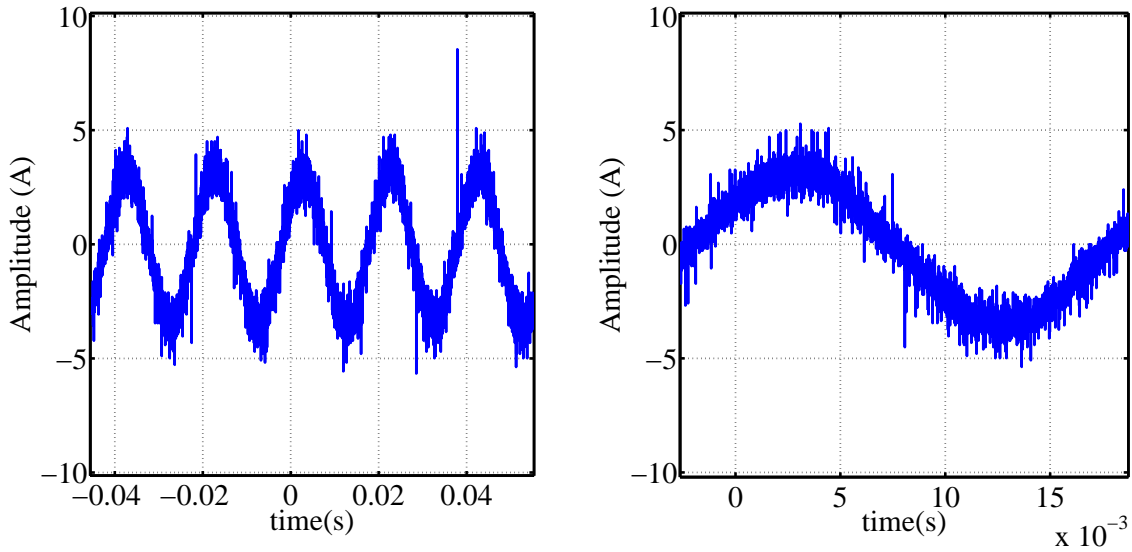


**Figure 6.25:** Oscilloscope Measurement: Input Supply-Voltages

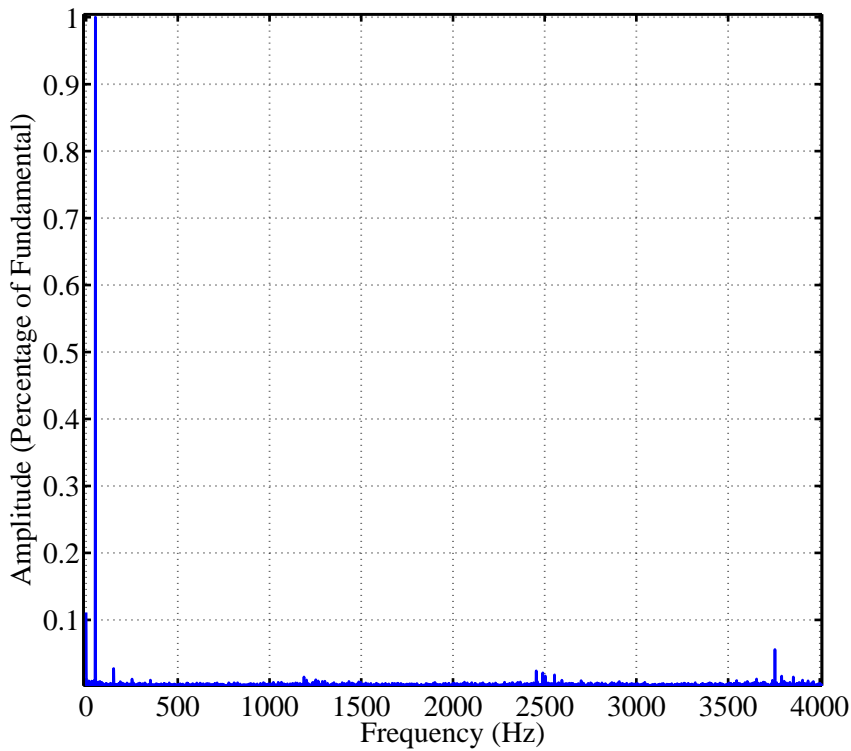
Figure 6.26 depicts the  $i_L$  steady-state oscilloscope measurement on the left and a detailed result on the right. The current has an excellent sinusoidal waveform with its frequency spectrum, determined with an FFT, shown in Figure 6.27 and 6.28.

The harmonic distortion is well below the IEEE Std 519-1992 Harmonic Limits[42]. This standard dictates a most stringent limit for current distortion of general distribution systems of 4% for harmonics lower than the 11<sup>th</sup> and 2% for harmonics from the 11<sup>th</sup> to the 17<sup>th</sup>. The switching harmonics start at  $2N \times f_s$ , as shown in Eq. 5.2.6. The effective switching frequency is thus 360 kHz which is much too high to measure in such a noise-rich environment. The frequency component clusters around 1250 Hz, 2500 Hz and 3750 Hz are presumed to be due to measurement noise folded back through aliasing.

<sup>5</sup>The letters 'a', 'b', ..., 'l' indicate the number of the cell in question within the stack.



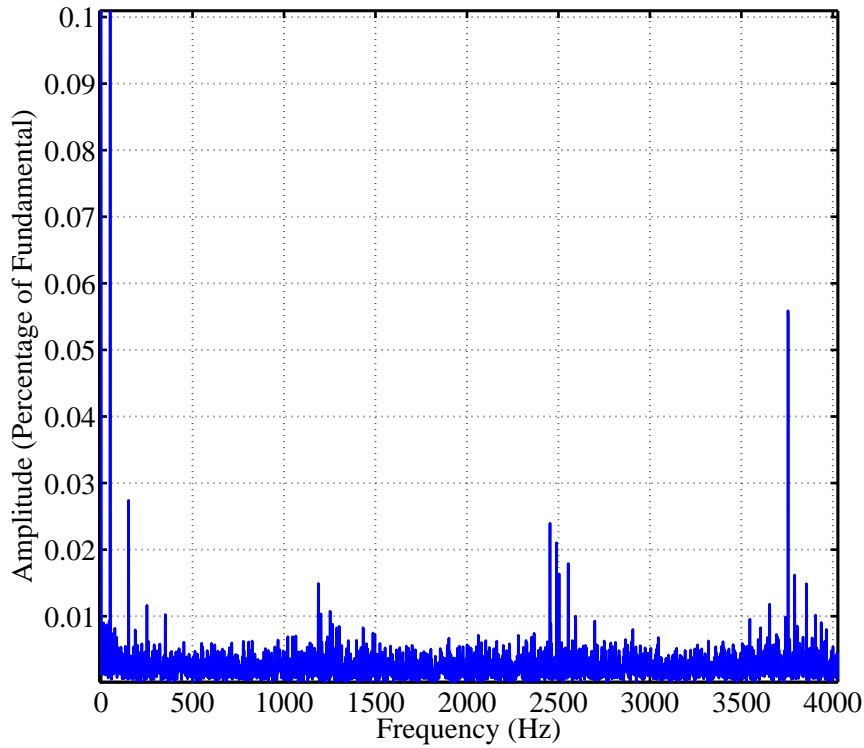
**Figure 6.26:** Oscilloscope Measurement: Input Inductor-Current



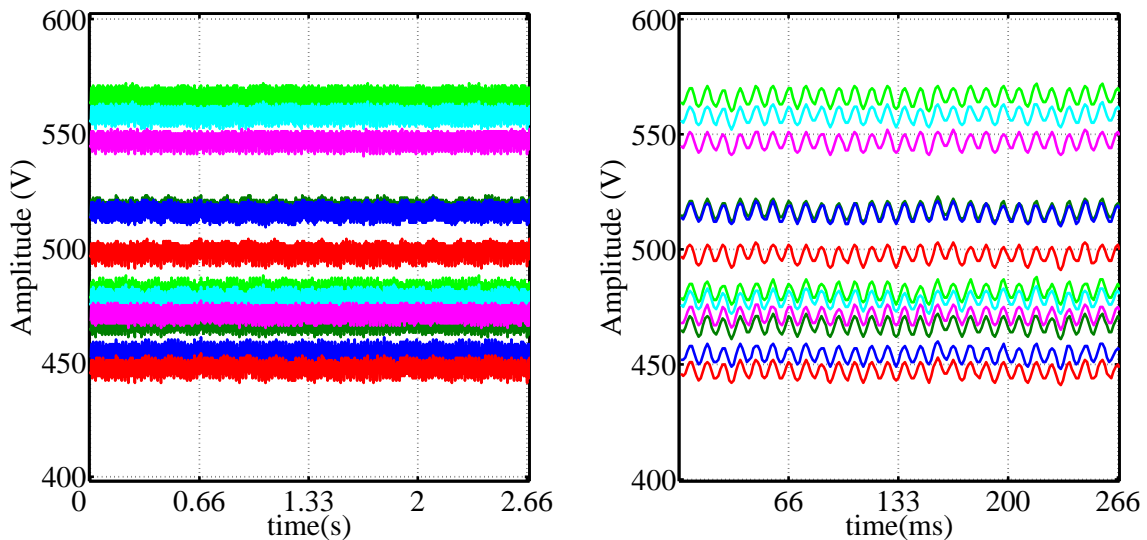
**Figure 6.27:** Frequency Spectrum of the Input Inductor-Current (Amplitude: 0 - 100%)

Figure 6.29 depicts the  $v_{acb} - v_{lcb}$  steady-state oscilloscope measurement on the left and a detailed result on the right. The result shows cell bus-voltage balancing to within 12% of the desired 500 V. This wide spread distribution is due to the component differences mentioned in Section 6.4.1. The component differences cause the effective duty cycle to vary from one DC-DC converter to the next. This leads to the ARs experiencing different loads and it is shown in Section 2.2 that ARs with different loads exhibit bus-voltage imbalance.





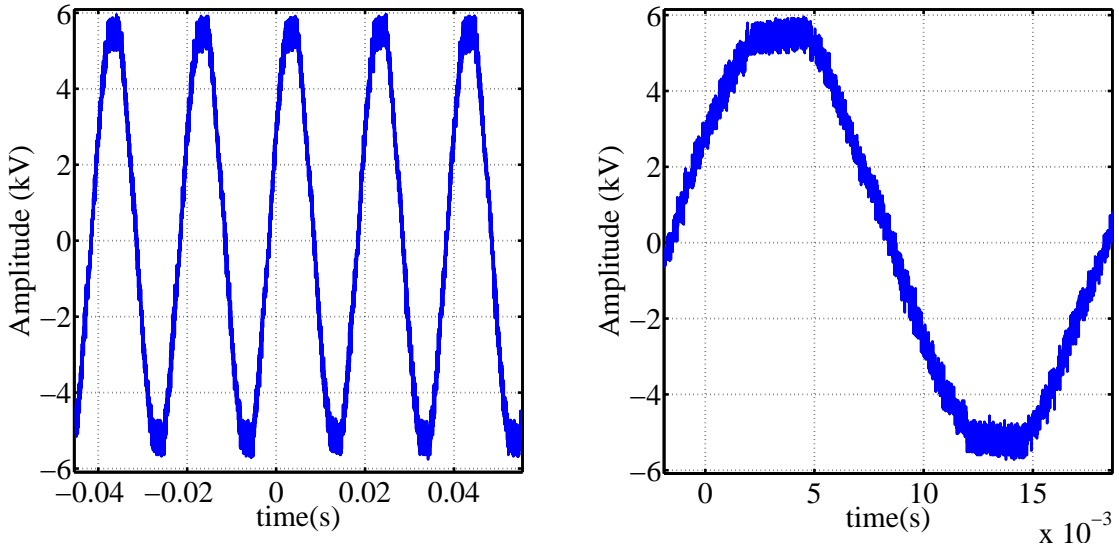
**Figure 6.28:** Frequency Spectrum of the Input Inductor-Current (Amplitude: 0 - 10%)



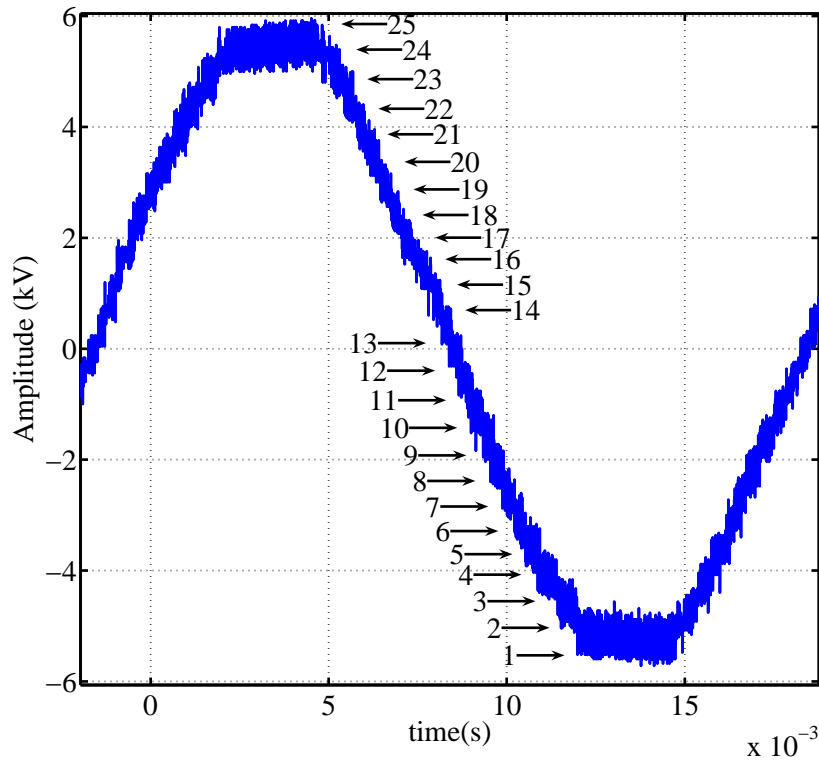
**Figure 6.29:** Signal-Tap Measurement: Cell Bus-Voltages

Figure 6.30 depicts the  $v_{in}$  steady-state oscilloscope measurement on the left and a detailed result on the right. The result shows 25 voltage levels, better indicated in Figure 6.31, with the 100 Hz representation of the respective cell bus-voltage ripples also visible. This number of voltage levels is expected from a 12 AR stack, as shown in Eq. 5.2.7. This stack is thus a 25-level converter.

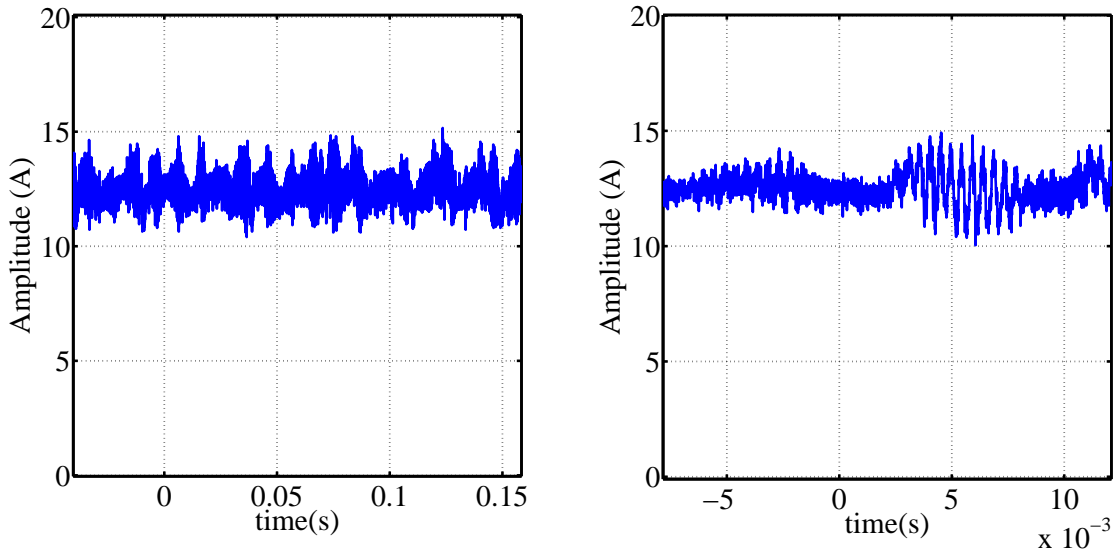
Figure 6.32 depicts the  $i_{oT}$  steady-state oscilloscope measurement on the left and a detailed result on the right. This current has a relatively stable average value. There are however, several unwanted oscillating frequencies.



**Figure 6.30:** Oscilloscope Measurement: Input Switched Voltages

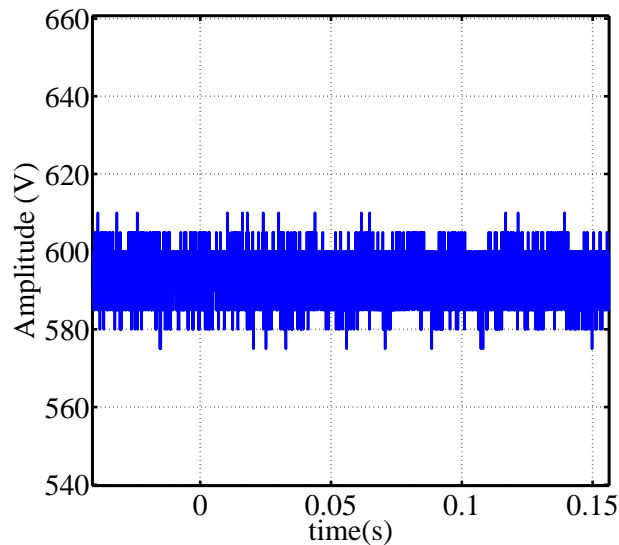


**Figure 6.31:** Oscilloscope Measurement: Input Switched Voltages



**Figure 6.32:** Oscilloscope Measurement: DC-DC Total Output-Current

Figure 6.33 depicts the  $v_{ib}$  steady-state oscilloscope measurement. The TPI bus-voltage has a satisfactory stable DC value compared to  $V_{ibref}$ .

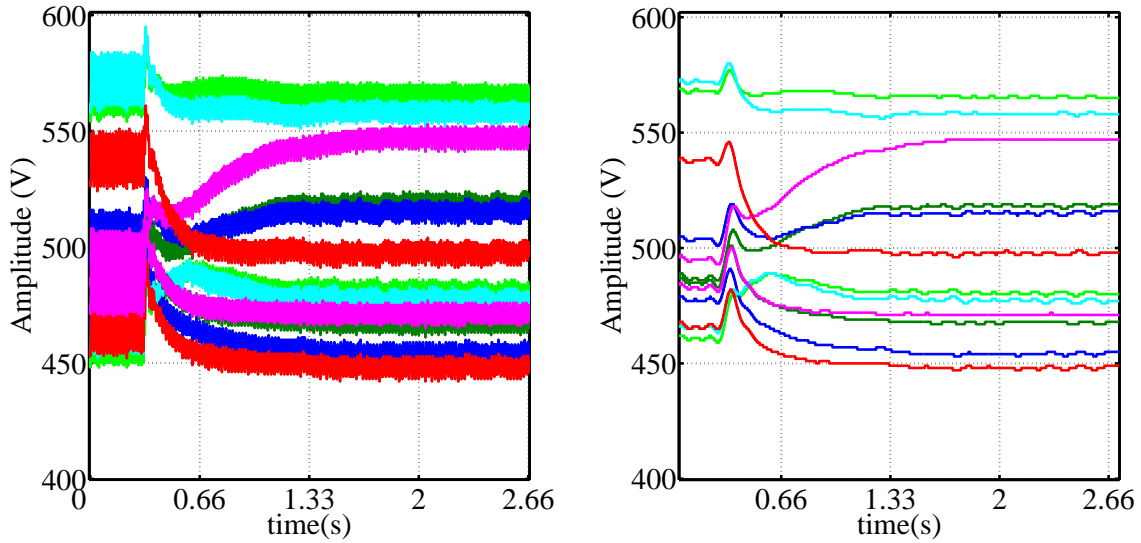


**Figure 6.33:** Oscilloscope Measurement: TPI Bus-Voltage

A second and third measurement test are presented, aimed at verifying acceptable full-scale SST operation during load steps in terms of the cell bus-voltage balancing, the output-voltage response and the output-current response. The second test introduces a high-low load-step as depicted in Figure D.7. This decreases the power delivered to the load by  $\pm 70\%$ . The output power is decreased from 8.4 kW to 2.6 kW with a TPI output line-line voltage-increase of 300 V to 312 V. This voltage is load-dependent because the TPI output-voltage is not controlled during this test.

Figure 6.34 depicts the Signal-Tap measurement of the  $v_{acb} - v_{lcb}$  transient response on the left and the filtered result on the right. An eighth order butterworth filter is implemented with a cutoff frequency of 20 Hz. The non-linear power-related component-difference effects are clearly visible. The cell bus-voltage balancing shows a very slight deterioration. The interesting

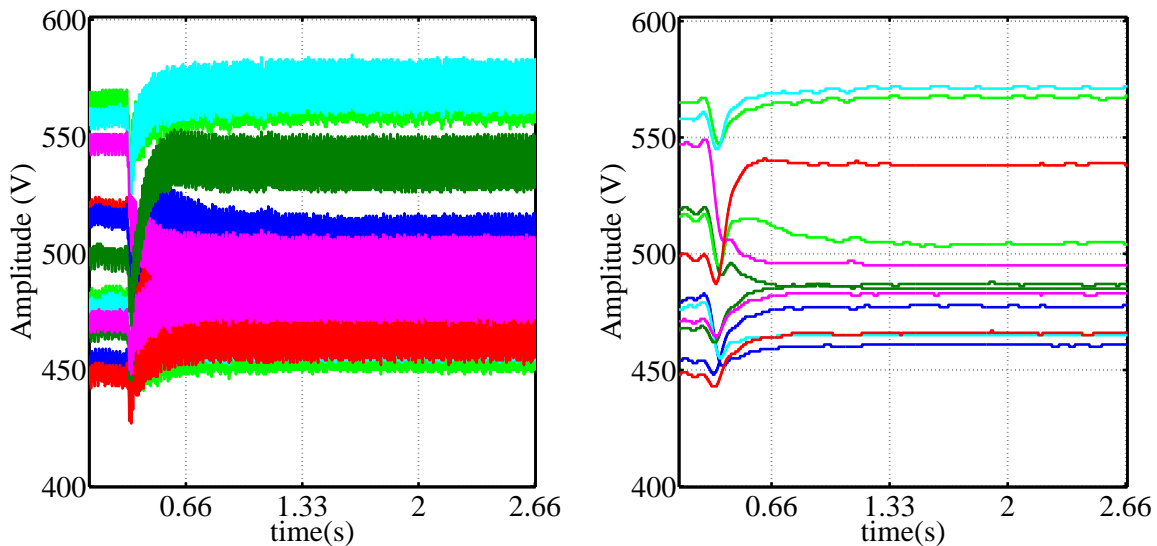
effect however, is the roll swapping between cells where some cells move up in the balancing hierarchy while others move down.



**Figure 6.34:** Signal-Tap Measurement: Cell Bus-Voltages

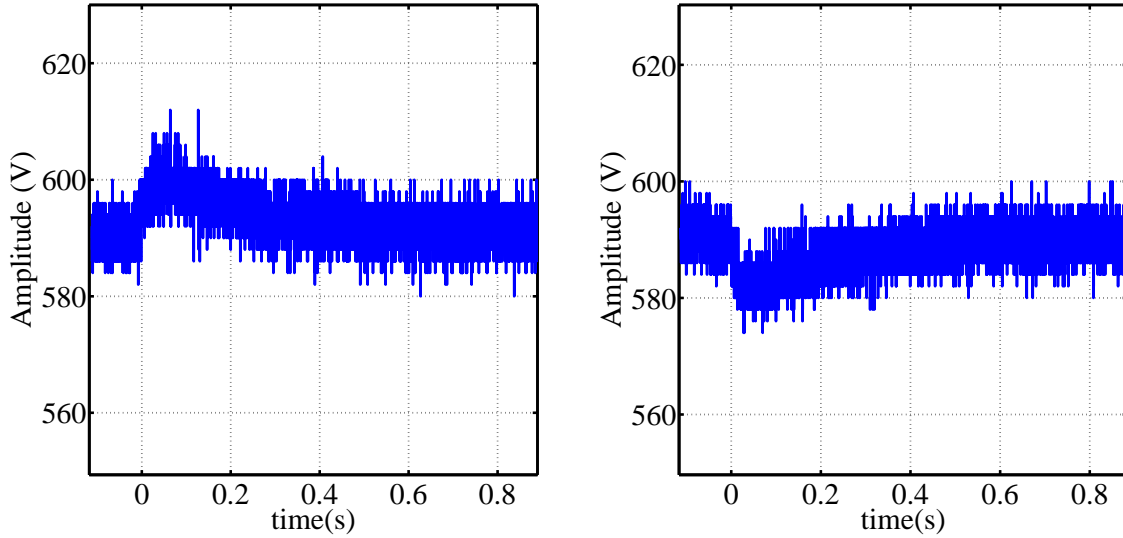
The third test introduces a low-high load-step as depicted in Figure D.7. This increases the power delivered to the load by  $\pm 220\%$ . The output power is increased from 2.6 kW to 8.4 kW with a TPI output line-line voltage-drop of 312 V to 300 V. This voltage is load-dependent because the TPI output-voltage is not controlled during this test.

Figure 6.35 depicts the Signal-Tap measurement of the  $v_{acb} - v_{lcb}$  transient response on the left and the filtered result on the right. An eighth order butterworth filter is implemented with a cutoff frequency of 20 Hz. Again, the non-linear power-related component-difference effects are clearly visible. The cell bus-voltage balancing shows a very slight improvement. Again, the interesting effect is the roll swapping between cells where some cells move up in the balancing hierarchy while others move down.



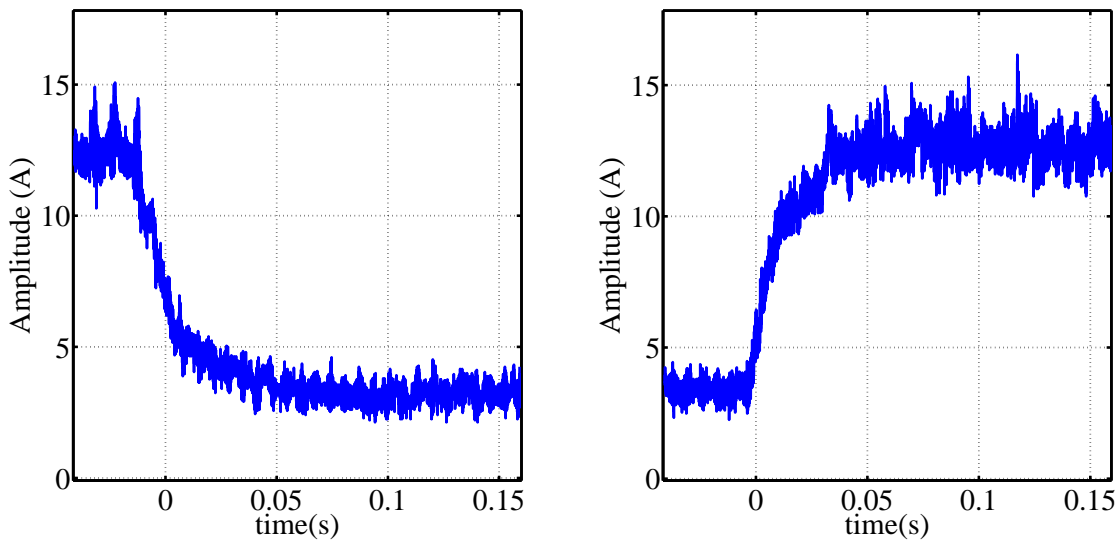
**Figure 6.35:** Signal-Tap Measurement: Cell Bus-Voltages

Figure 6.36 depicts the oscilloscope measurement of the  $v_{ib}$  transient response of the second test on the left and of the third test on the right. Both results are satisfactory with slight voltage deviations. These results show slower transients, compared to the results in Figure 6.22, due to the DC-DC voltage-loop plant difference between the scaled output-bus and the TPI-bus.



**Figure 6.36:** Oscilloscope Measurement: TPI Bus-Voltage

Figure 6.37 depicts the oscilloscope measurement of the  $i_{oT}$  transient response of the second test on the left and of the third test on the right. Both results are acceptable. There are however, several unwanted oscillating frequencies during the high- and low-load conditions.



**Figure 6.37:** Oscilloscope Measurement: Total Output-Current

The measurements obtained are satisfactory in determining successful full-scale SST operation at rated input-voltage as well as the successful addition of the TPI and three-phase output load. Satisfactory results are obtained during load-steps, in terms of the cell bus-voltage balancing, the output-voltage response and the output-current response.

### 6.4.3 Three-Phase Full-Scale SST Test Measurements

The three-phase full-scale SST test, is where AC inductor-currents,  $I_{LA} - I_{LC}$ , are drawn from AC input voltages,  $V_{acA} - V_{acC}$ , to maintain total bus-voltages,  $V_{cbTA} - V_{cbTC}$ , at a specific average value. A total of 36 HF currents,  $(I_{atA} - I_{ltA}) - (I_{atC} - I_{ltC})$ <sup>6</sup>, are drawn from 36 buses, transformed, rectified and filtered to the output-currents,  $(I_{aoA} - I_{loA}) - (I_{aoC} - I_{loC})$ . These currents add up to the three total-stack output-currents,  $I_{oTA} - I_{oTC}$ , which are indirectly controlled to maintain a specific average TPI bus-voltage,  $V_{ib}$ . The test is aimed at verifying successful three-phase full-scale SST operation in terms of total cell bus-voltage balancing between phases as well as active output-current balancing. The physical test setup is discussed in Appendix D.2.3.

Figure 6.38 depicts the  $i_{LA}$ ,  $i_{LB}$  and  $i_{LC}$  steady-state oscilloscope measurement on the left and a detailed result on the right. All three currents have a well-shaped sinusoidal waveform with a 120° phase shift with respect to each other. The measurement contains a high degree of switching noise. A workaround is to take a sample-averaged measurement for analytical purposes. The 64 sample-average oscilloscope function is used where 64 triggered waveforms are averaged to present the measurement.

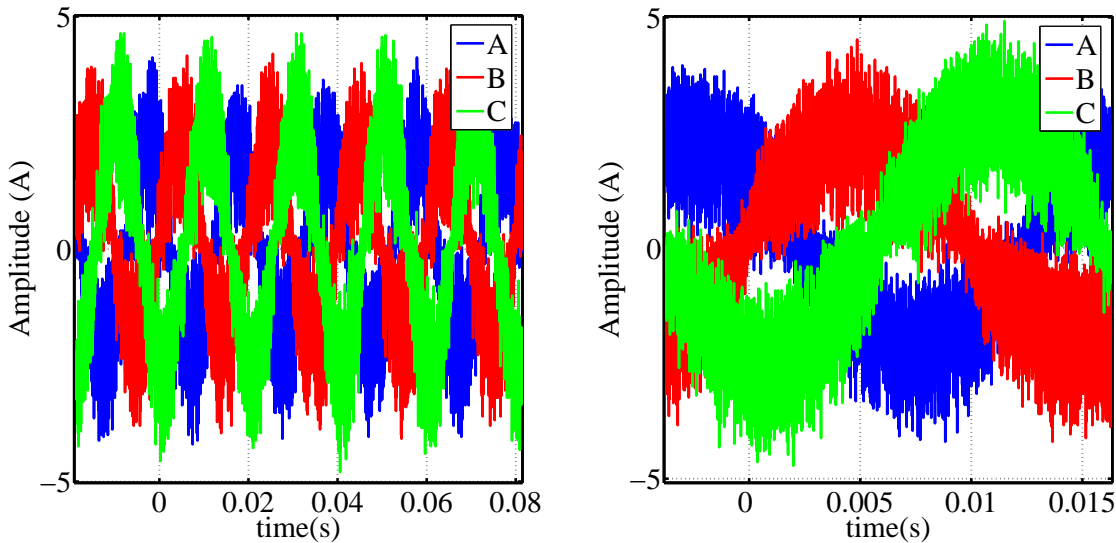


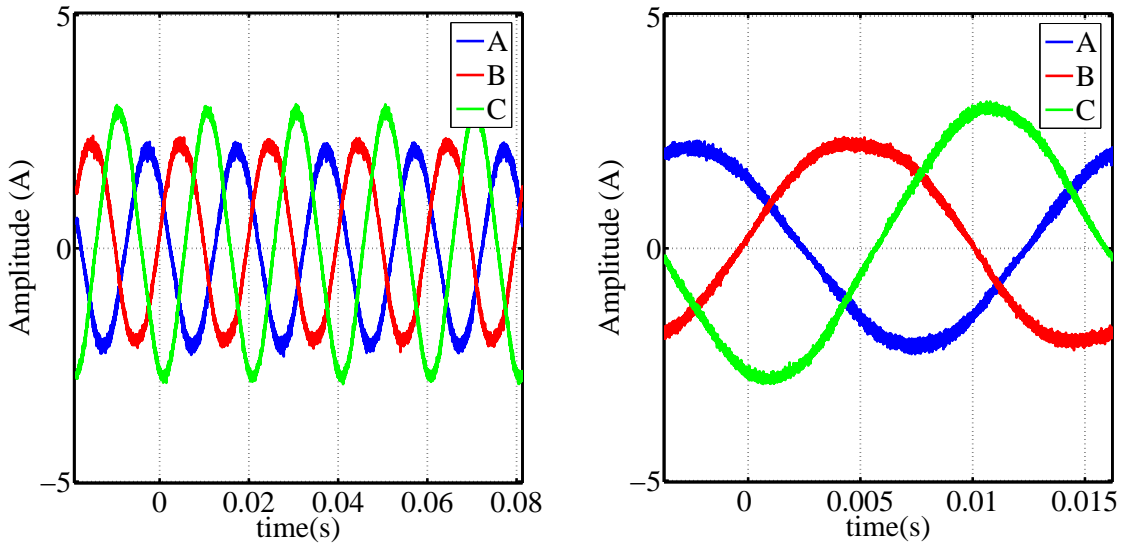
Figure 6.38: Oscilloscope Measurement: Input Inductor-Currents

Figure 6.39 depicts the  $i_{LA}$ ,  $i_{LB}$  and  $i_{LC}$  sample-averaged steady-state oscilloscope measurement on the left and a detailed result on the right. It is clear that  $i_{LC}$  has a significantly greater amplitude compared to  $i_{LA}$  and  $i_{LB}$ . This is, as mentioned in Section 6.4.1, because the 3-phase variac does not supply perfectly balanced 3-phase voltages. In this case,  $v_{acC}$  has a lower value compared to  $v_{acA}$  and  $v_{acB}$ . This voltage difference is exaggerated by the step-up transformer. Due to equal AR voltage-loop references on all MCs, a larger  $i_L$  is drawn from the lower  $v_{ac}$  to achieve the same  $v_{cbT}$  value.

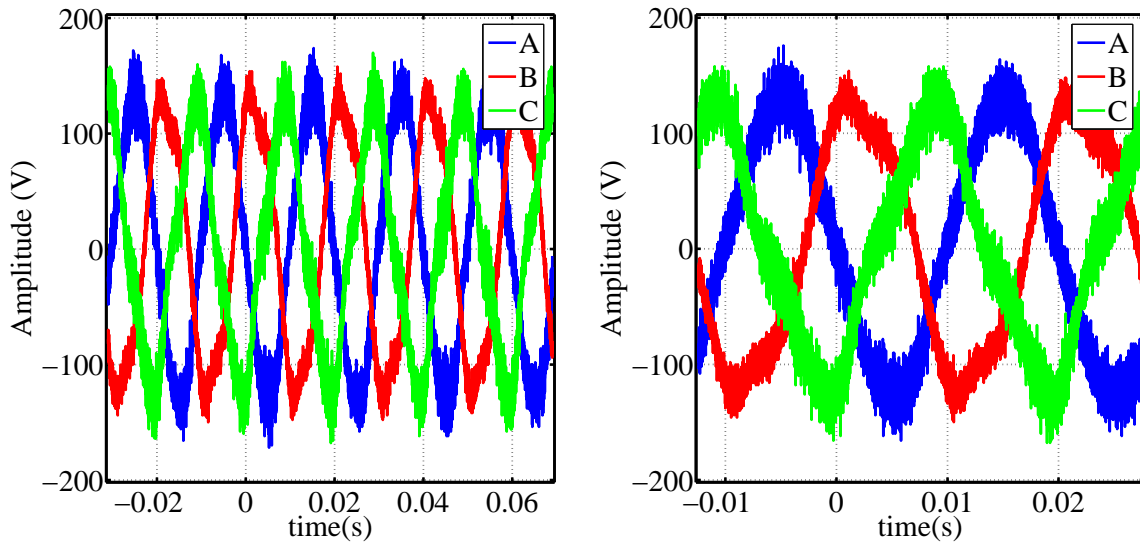
Figure 6.40 depicts the  $v_{acA}$ ,  $v_{acB}$  and  $v_{acC}$  steady-state oscilloscope measurement on the left and a detailed result on the right. The voltage differences are not obvious in this measurement, however the step-up transformer exaggerates the voltage difference by 400:6600.

Figure 6.41 depicts the  $v_{lcbA}$ ,  $v_{lcbB}$  and  $v_{lcbC}$  steady-state oscilloscope measurement on the left and a detailed result on the right. The three cell bus-voltages are relatively balanced with

<sup>6</sup>The letters 'a', 'b', ..., 'l' indicate the number of the cell in question within the stack.



**Figure 6.39:** Oscilloscope Measurement: Sample-Averaged Input Inductor-Currents



**Figure 6.40:** Oscilloscope Measurement: Variac Supply Voltages

the imbalance caused by a combination of differential-probe offsets and difference-effects discussed in Section 6.4.1 and 6.4.2. Only 3 of 36 cell bus-voltages are thus measured. This is due to the limited number of available differential probes, the high common-mode voltage of cells higher in the stack<sup>7</sup> and the depletion of FPGA logic elements. At this stage of the SST development, the FPGA percentage used is above 90%. There are thus not enough logic elements to facilitate a large Signal-Tap measurement like the measurement shown in Figure 6.29.

Figure 6.42 depicts the  $v_{inA}$ ,  $v_{inB}$  and  $v_{inC}$  steady-state oscilloscope measurement on the left and a detailed result on the right. The result shows 25 voltage levels of all three input switched-voltages. The 100 Hz representation of the respective total cell bus-voltage ripples is not as clearly visible. This number of voltage levels is expected from 12 AR-stacks, as shown in Eq. 5.2.7. The SST is thus a three-phase 25-level converter.

Figure 6.43 depicts the  $i_{oTA}$ ,  $i_{oTB}$  and  $i_{oTC}$  steady-state oscilloscope measurement on the

<sup>7</sup>Cells higher in the stack are closer to the positive  $v_{in}$  terminal and are thus at a higher common-mode voltage

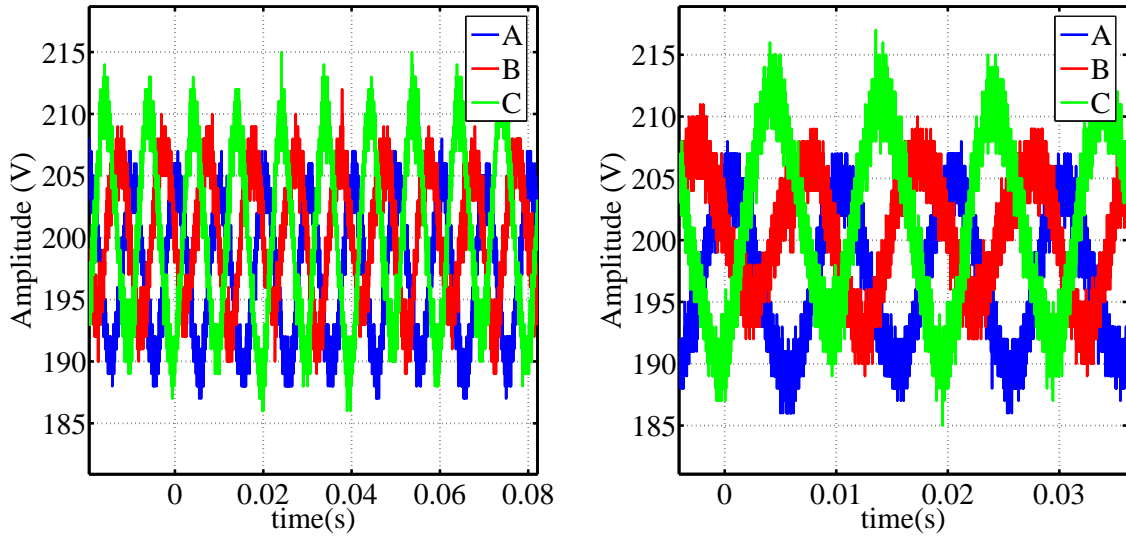


Figure 6.41: Oscilloscope Measurement: Cell Bus-Voltages

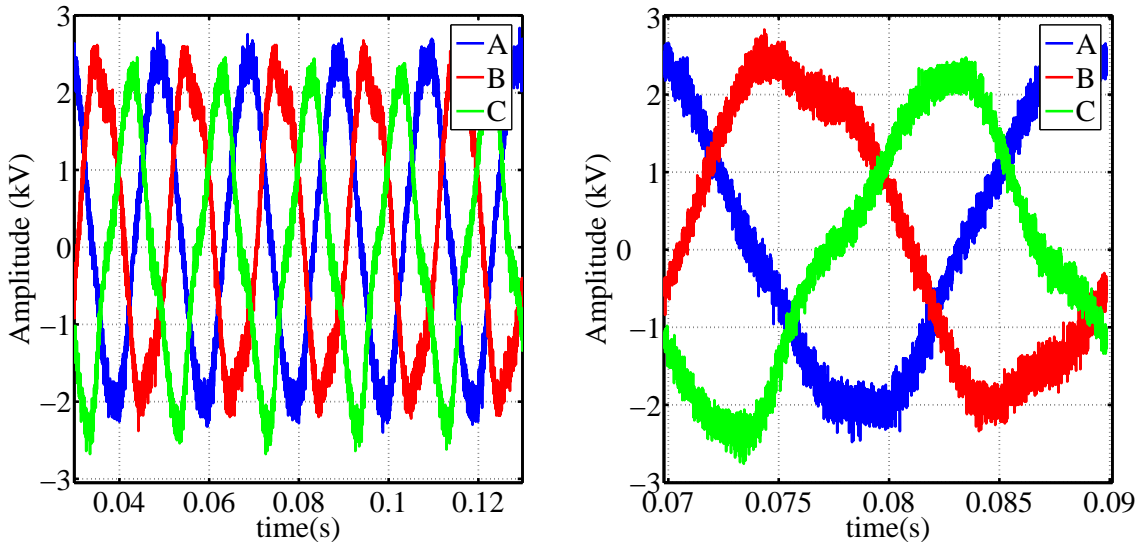


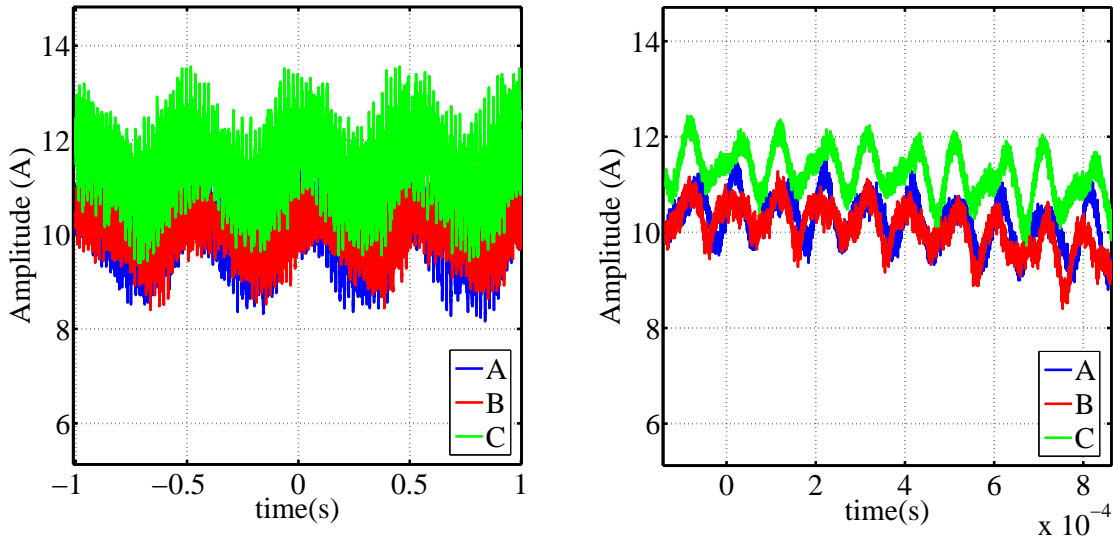
Figure 6.42: Oscilloscope Measurement: Input Switched Voltages

left and a detailed result on the right. The output-currents are relatively balanced. The imbalance is partly caused by the direct control of the  $i_t$  currents after which they are transformed by the isolation-transformer, rectified and filtered by the output filter of each respective DC-DC converter. The component differences from one DC-DC converter to the next thus cause differences in current transformation from  $i_t$  to  $i_o$ . The currents show several unwanted oscillating frequencies of which a 2 Hz component is most prominent.

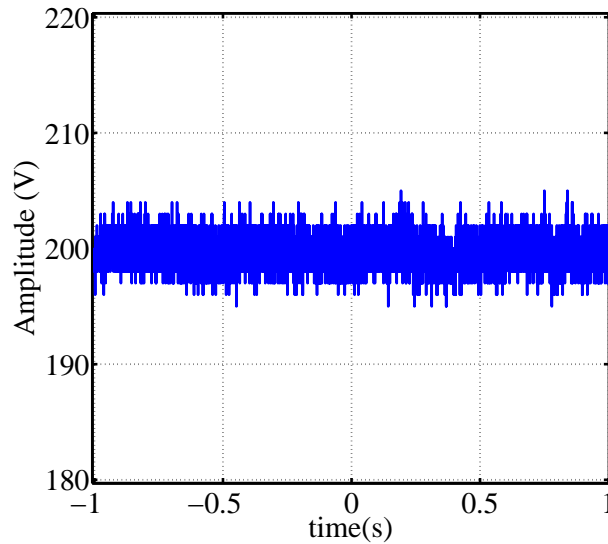
Figure 6.44 depicts the  $v_{ib}$  steady-state oscilloscope measurement. The TPI bus-voltage has a satisfactory stable DC value compared to  $V_{ibref}$ .

A second and third measurement test are presented, aimed at verifying acceptable three-phase full-scale SST operation during load steps in terms of the output-voltage response and the output-current response. The second test introduces a high-low load-step as depicted in Figure D.9. This decreases the power delivered to the load by  $\pm 70\%$ . The third test introduces a low-high load-step as depicted in Figure D.9. This increases the power delivered to the load by  $\pm 230\%$ .





**Figure 6.43:** Oscilloscope Measurement: Isolation Stage Output-Currens

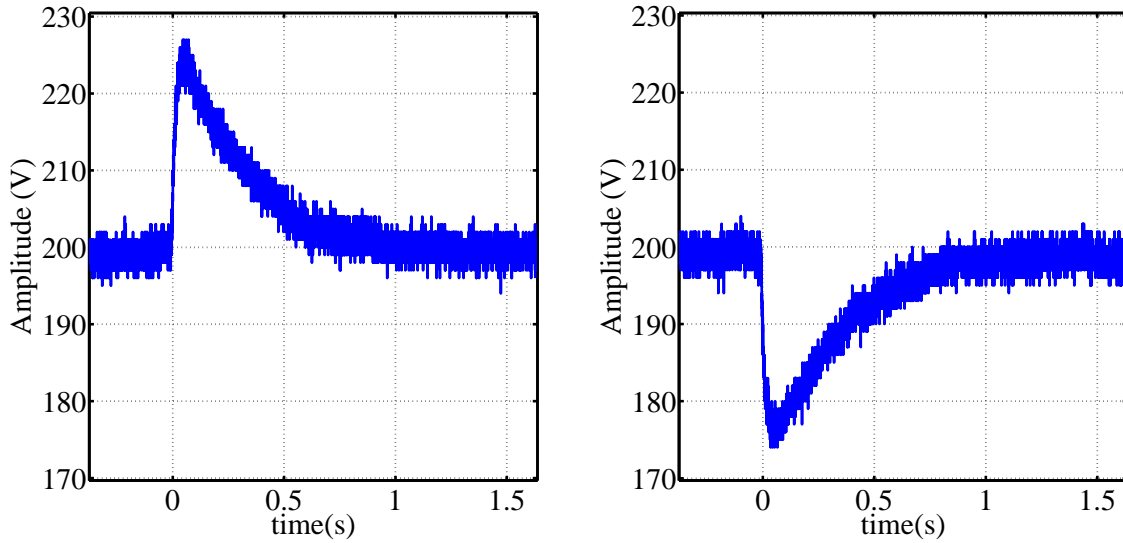


**Figure 6.44:** Oscilloscope Measurement: TPI Bus-Voltage

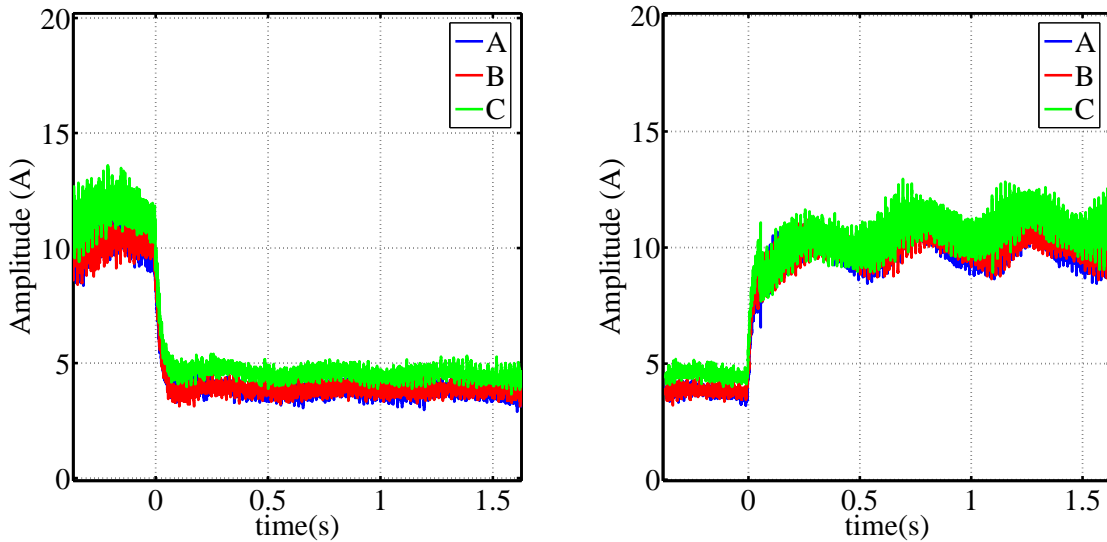
Figure 6.45 depicts the oscilloscope measurement of the  $v_{ib}$  transient response of the second test on the left and of the third test on the right. Both results are satisfactory with slight voltage deviations. These results show slower transients, compared to the results in Figure 6.22, due to the DC-DC voltage-loop plant difference between the scaled output-bus and the TPI-bus.

Figure 6.46 depicts the oscilloscope measurement of the  $i_{oTA}$ ,  $i_{oTB}$  and  $i_{oTC}$  transient response of the second test on the left and of the third test on the right. Both results are acceptable. There are however, several unwanted oscillating frequencies during the high- and low-load conditions. The most prominent 2 Hz oscillation however, has a larger amplitude during the high-load condition.

The measurements obtained are satisfactory in determining successful three-phase full-scale SST operation in terms of total cell bus-voltage balancing between phases as well as active output-current balancing. Satisfactory results are obtained during load-steps, in terms of the output-voltage response and the output-current response.



**Figure 6.45:** Oscilloscope Measurement: TPI Bus-Voltage



**Figure 6.46:** Oscilloscope Measurement: Isolation-Stage Output-Currents

## 6.5 Conclusion

The DC-DC role within the SST, as an extension to the multi-level converter topology, as well as its modular design was briefly discussed. The double-loop DC-DC control-strategy with its single voltage-loop and three fold current-loop was discussed. The control design was explained in terms of the voltage-loop plant-model linearisation followed by the voltage-loop compensator design. The implementation of the DC-DC control-system within three MCs and 3N CCs, in parallel with the AR control-system, was explained. Successful current- and voltage-loop implementation was confirmed through test measurements. Active output-current balancing within a two-phase scaled SST as well as a three-phase full-scale SST was verified. The former incorporated an output-parallel scaled load and the latter incorporated the TPI together with a three-phase load. A single-phase full-scale SST test verified successful operation with a rated line-line input-voltage of 6.6 kV. All three measurement-tests indicated DC-DC control functionality, however unwanted oscillations are present on the isolation-stage output-currents. The

MC FPGA logic elements are near depletion at the three-phase full-scale SST development stage. This reduces the Signal-Tap functionality and complicates debugging. Firmware optimisation is thus recommended if control-strategy improvement or expansion is necessary. The outcome as described in this chapter, shows that the SST control is functional with room for improvements.

# Chapter 7

## Thesis Conclusion

In this chapter, the conclusions obtained from preceding chapters are highlighted. This is followed by a comprehensive project conclusion where the project outcome as well as future work is discussed.

### 7.1 Main Controller Hardware Design

The MC hardware designed and implemented, consists of three measurement PCBs, a controller PCB and a fibre-optic interface PCB. These PCBs are implemented in triplicate to facilitate the three-phase SST control.

The measurement PCBs were designed with the focus on preventing noise interference. The resulting PCBs function perfectly after filter modifications were made to prevent high frequency op amp oscillation. This oscillation was caused by the op amp driving a capacitive load, facilitated by the twisted-pair cable connecting each measurement PCB with the controller PCB.

The controller PCB functions well in terms of the secondary measurement circuitry, the parallel communication, and the peripheral circuitry. The NIOS II embedded processor was successfully implemented within the FPGA. The flash memory interface, the real-time clock interface and the USB interface were subsequently implemented within the C/C++ tool chain and Eclipse Integrated Development Environment (IDE). The NIOS II embedded processor could however not be incorporated within the three-phase full-scale SST system. This is due to the depletion of the FPGA logic elements at this stage of development. An overlooked FPGA hardware specification caused incompatibility between the FPGA and the DDR RAM unit. This means that the DDR is not used, which reduces the software development freedom, to a still acceptable level. It should be noted that the depletion of FPGA logic elements is not linked to a lack of system memory.

The fibre-optic PCB functions extremely well with no sign of interference or communication failures. Its design was steered by the total SST communication layout, the bidirectional fibre-optic channel, as building block, as well as the interface between this PCB and the controller PCB

### 7.2 Active-Rectifier Control

The double-loop AR control-scheme was designed by separating the inner current-loop and outer voltage-loop. Each loop plant was subsequently linearised and each compensator designed.

Time domain simulations were presented to verify current- and voltage-loop functionality as well as control and circuit integration. The results obtained proved very promising with excellent current and voltage reference tracking. Current peaking at startup was revealed, which led to the implementation of a specific startup sequence. The simulation results further showed the system response to current-loop reference steps while implementing only the current-loop. These results correspond very well with the calculated step-response of the current-loop. A satisfactory system-response to load steps was also shown, while implementing the current- and voltage-loop. It was explained how current peaking can be expected at a load step with a substantial power increase.

The control implementation within the MC and CC was discussed in terms of the two control-loops, the startup sequence and error handling. The control loop implementation was focused on facilitating multisampling PWM with a specific PWM communication protocol. The communication was established between the MC and CC with a communication package consisting of bit allocations for a command package, an AR-control package and a DC-DC-control package. The startup sequence is explained in terms of the state progression with emphasis on precharging the cell bus-capacitor.

Test measurements were presented to verify successful circuit and control implementation. Oscilloscope measurement as well as Signal-Tap measurement were presented to examine control functionality thoroughly. The control measurement-system accuracy was thus also established. The results obtained show excellent current and voltage reference tracking and correspond very well with the AR simulation results. The startup sequence incorporating cell bus-capacitor precharging proves successful in eliminating current peaking at startup.

### 7.3 Cascaded Active-Rectifier Control

The double-loop AR control-scheme was expanded to facilitate an  $N$  AR stack. The inner current-loop and outer voltage-loop were separated and each loop plant was subsequently expanded. Each compensator was thus redesigned to achieve similar closed-loop characteristics compared to the AR control.

Time domain simulations of a two-AR stack were presented to verify successful current- and voltage-loop integration as well as natural voltage balancing and rebalancing. Excellent results were obtained in terms of current and voltage reference tracking as well as the multilevel switched input-voltage. Natural voltage balancing with equal loads and natural voltage rebalancing after an external perturbation was confirmed. The external perturbation was facilitated with load steps. The rebalancing result corresponds closely with the results from the natural voltage balancing literature review in Section 2.2.

The control implementation within the MC and  $N$  CCs was discussed in terms of the two control-loops, the startup sequence and error handling. The discussion regarding control loop implementation was focused on the changes made in control firmware to implement the expanded control scheme. The PWM communication protocol was simplified while still facilitating multisampling PWM. The startup sequence is explained in terms of the state progression with emphasis on precharging the  $N$  cell bus-capacitor.

Test measurements of a two-AR stack were presented to verify successful current- and voltage-loop implementation as well as natural voltage balancing and rebalancing. Outstanding results were obtained in terms of current and voltage reference tracking as well as the multilevel switched input-voltage. Natural voltage balancing with equal loads and natural voltage rebalancing after an external perturbation was confirmed. The rebalancing result corresponds closely with the simulation results and the results from Section 2.2.

## 7.4 DC-DC Converter Control

The double-loop control scheme was designed to facilitate the control of  $3N$  DC-DC converters. The inner current-loop consists of three parallel current-loops, each dedicated to a single phase. This loop design is explained in [12] and the voltage loop was designed by separating it, linearising the plant, and subsequently designing the compensator. This design focused on the fact that the AR voltage-loop and the DC-DC voltage-loop influence each other. The bandwidths of these loops determine this influence. Bandwidth limitations together with physical tests led to the design of a DC-DC voltage-loop bandwidth of at least double the AR voltage-loop bandwidth.

The control implementation within the three MCs and  $3N$  CCs was discussed in terms of the two control-loops, the startup sequence and error handling. The control loop implementation was focused on facilitating the voltage-loop within a single MC and a current-loop within each MC. The DC-DC control communication between an MC and a CC is piggybacked on the existing AR control communication. The DC-DC control communication between MCs was also implemented. The startup sequence is explained in terms of the state progression with emphasis on precharging the  $3N$  cell bus-capacitor while facilitating power transfer to improve cell bus-voltage balancing prior to startup.

Test measurements of a two-phase scaled SST, a single-phase full-scale SST and a three-phase full-scale SST were presented. The first test verified successful DC-DC control implementation as well as active output-current balancing with an output-parallel load. The second test verified successful single-phase full-scale SST operation at rated input-voltage with the addition of the TPI and three-phase load. The third test verified successful three-phase full-scale SST operation, together with total cell bus-voltage balancing and active output-current balancing between phase stacks.

## 7.5 Project Outcome

The SST main controller design and implementation proved successful in terms of facilitating the primary functionality of the SST. The NIOS II embedded processor, together with the peripheral-circuit interfaces, was successfully developed. The integration of these developments together with the SST primary functionality could however not be completed due to the depletion of FPGA logic elements.

The design, expansion and implementation of the separate control systems led to the control of a three-phase full-scale SST. A single-phase was operated at rated input-voltage with excellent results. The input inductor-current showed outstanding harmonic distortion results and the input switched-voltage was exceedingly sinusoidal due to its 25 voltage-levels.

The three-phase SST input inductor-currents show an imbalance due to the imbalance in the input-voltage supply. The SST flexibility however provides the option to substitute this current imbalance with an imbalanced power distribution between phase stacks.

The voltage balancing within each phase stack shows a wide spread distribution around the desired value. This is caused by component differences from one cell to the next. These differences include the isolation-transformer leakage-inductance values and the DC-DC filter inductor values. This leads to a power related difference in the effective DC-DC duty cycle of each cell. There is thus a difference in the load experienced by each AR and natural voltage balancing is not possible without equal loads.

The SST, as an innovative proof-of-concept project, is functional with room for improvements.

### 7.5.1 Future work

- The MC peripheral functionality can be integrated with the primary functionality of the SST. This will require firmware optimisation to reduce its logic-element usage or controller PCB redesign incorporating a larger FPGA.
- The AR- and the DC-DC control can be optimised with control modifications or introducing a different control strategy e.g. predictive control.
- The component differences between cells can be minimised by remanufacturing these components with more stringent tolerances.
- The redundancy within the SST can be increased by facilitating the safe continual operation after a cell has malfunctioned.

# Appendices



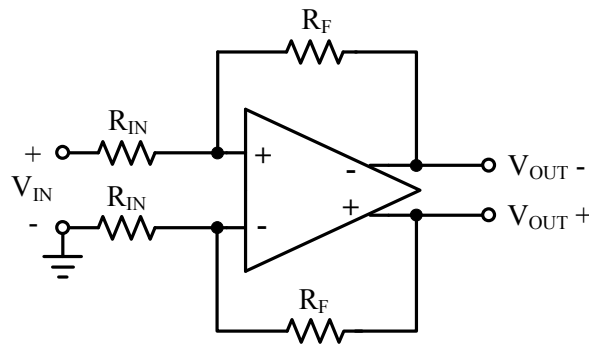
# Appendix A

## Main Controller Design Details

### A.1 Input-Inductor Current Measurement PCB Details

#### A.1.1 Designed Gain

The op amp circuit can be simplified to the circuit shown in Figure A.1.



**Figure A.1:** Simplified Op Amp Circuit with Single Ended Input

The value of  $R_F$  and  $R_{IN}$  is chosen as 1 k $\Omega$  and the op amp gain is determined by the equation:

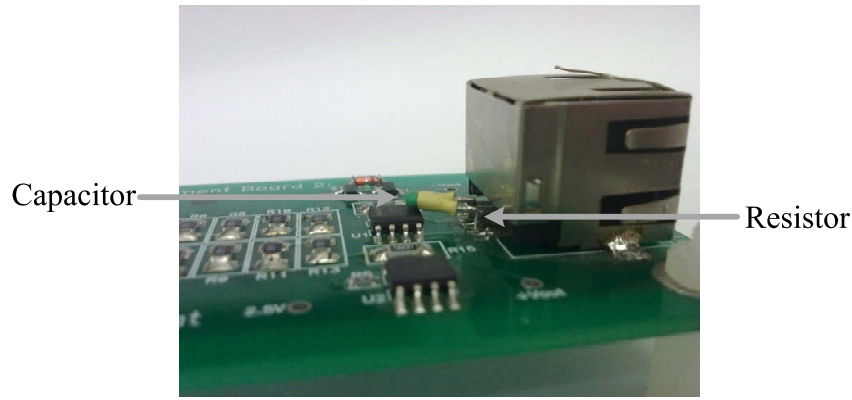
$$A1 = \frac{V_{OUT+}}{V_{IN}} = \frac{R_F}{2 \times R_{IN}} = 0.5 \quad (\text{A.1.1})$$

The reason for this designed gain value will become apparent in Section 3.3.2 where this gain is only a section of the complete measurement channel.

#### A.1.2 Measurement PCB Filter

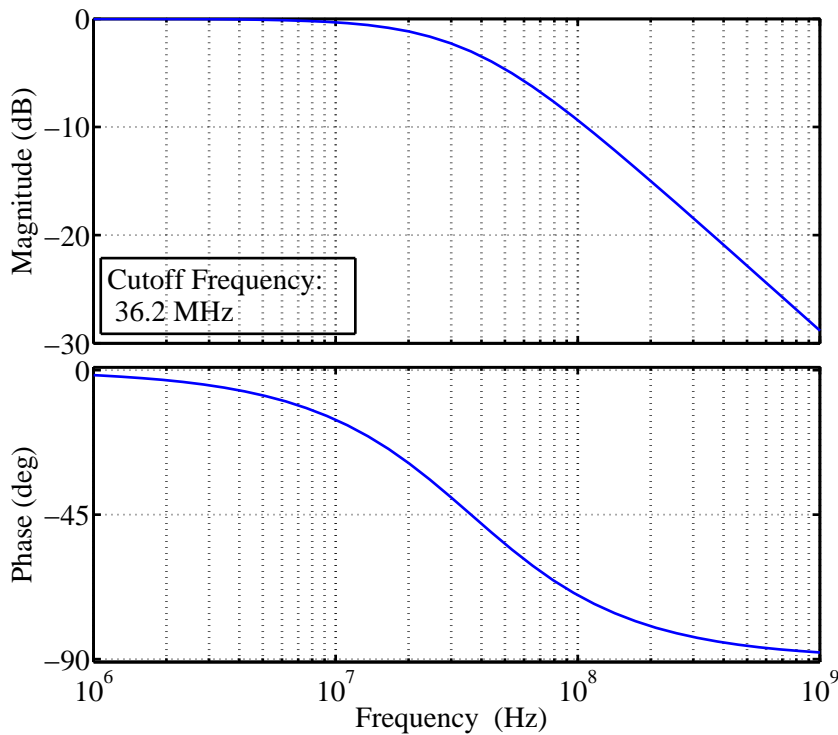
A differential filter is implemented on the input-inductor current measurement PCB after the PCB design phase. Some hardware modifications are thus made as shown in Figure A.2. The filter design is identical to the 2<sup>nd</sup> low-pass filter discussed in Section A.4.2, depicted in Figure A.10. The filter transfer function is thus calculated as:

$$G(s) = \frac{V_{OUT}}{V_{IN}} = \frac{\frac{1}{2CR}}{s + \frac{1}{2CR}} = \frac{2.273 \times 10^8}{s + 2.273 \times 10^8} \quad (\text{A.1.2})$$



**Figure A.2:** Measurement PCB Filter Modification

with a capacitor value of 100 pF and two 22  $\Omega$  resistors. The frequency response of filter  $G(s)$  is shown in Figure A.3.



**Figure A.3:** Frequency Response of the Input-Inductor Current Measurement PCB Filter

## A.2 Input-Voltage Measurement PCB Details

### A.2.1 Designed Gain

As with the input-inductor current measurement PCB, the op amp circuit can be simplified to the circuit shown in Figure A.1 and the op amp gain is determined by Equation A.1.1.

There are two parameters to consider when designing this op amp gain: The values of the resistors,  $R_F$  and  $R_{IN}$ , and their power consumption. Because of the high input voltage,  $R_{IN}$  has

a power consumption problem which is solved by representing  $R_{IN}$  with multiple resistors. The values are chosen as:

$$A1 = \frac{1 \text{ k}\Omega}{2 \times (6 \times 18 \text{ k}\Omega)} = 4.629 \times 10^{-3} \quad (\text{A.2.1})$$

$R_{IN}$  thus consists of 6 resistors each with the value of 18 k $\Omega$ . They are of the 1206 package and have a power rating of 250 mW. According to ideal op amp theory, the potential at the positive and negative op amp inputs are equal [43], p185. Furthermore, because this is a differential op amp, the two inputs are equal to the common-mode input potential,  $V_{CM}$ . The total potential over the 6 resistors can thus be calculated as:

$$V_{RIN} = V_{AC} - V_{CM} = 230 \text{ V} - 2.5 \text{ V} = 227.5 \text{ V} \quad (\text{A.2.2})$$

The current through these resistors is calculated as:

$$I_{IN} = \frac{V_{RIN}}{6 \times 18 \text{ k}\Omega} = 2.106 \text{ mA} \quad (\text{A.2.3})$$

The power dissipated in each resistor is thus:

$$P = \frac{V_{RIN}}{6} \times I_{IN} = 79.87 \text{ mW} \quad (\text{A.2.4})$$

which is sufficiently lower than the 1206 resistor power rating. The two design parameters are thus within range to achieve a suitable gain.

## A.2.2 Protection Circuit

The problem arises when the connection to the Controller PCB is lost while the high input voltage is connected. The 5 V Vcc voltage connection, the ground connection and the differential output pair connections are thus lost. With the op amp not powered and no current flow from the high input-voltage PCB terminal to the feedback path of the op amp, this input pin will be at the same potential as the high input-voltage which will damage the op amp.

The implemented protection circuit thus consists of a ZMM5.6[44] zener diode and two BAT54[45] schottky diodes. For the positive half cycle of the input voltage, the current can flow through  $D1$  and  $Z1$  to ground. The current flow through  $Z1$  causes it to clamp Vcc at 5.6 V to power the op amp. For the negative half cycle of the input voltage, the current can flow through  $D2$  to ground. With current flow, the voltage divider,  $R1$ - $R12$ , can function properly and the op amp is protected [11]. Figure A.4 depicts the protection circuit.

## A.2.3 Measurement PCB Filter

As with the input-inductor current measurement PCB, a differential filter is implemented on the input-voltage measurement PCB after the PCB design phase. Some hardware modifications are thus made as shown in Figure A.2. The filter design is identical to the 2<sup>nd</sup> low-pass filter discussed in Section A.4.2, depicted in Figure A.10. The filter transfer function is thus calculated as:

$$G(s) = \frac{V_{OUT}}{V_{IN}} = \frac{\frac{1}{2CR}}{s + \frac{1}{2CR}} = \frac{2.273 \times 10^8}{s + 2.273 \times 10^8} \quad (\text{A.2.5})$$

with a capacitor value of 100 pF and two 22  $\Omega$  resistors. The frequency response of filter  $G(s)$  is shown in Figure A.3.

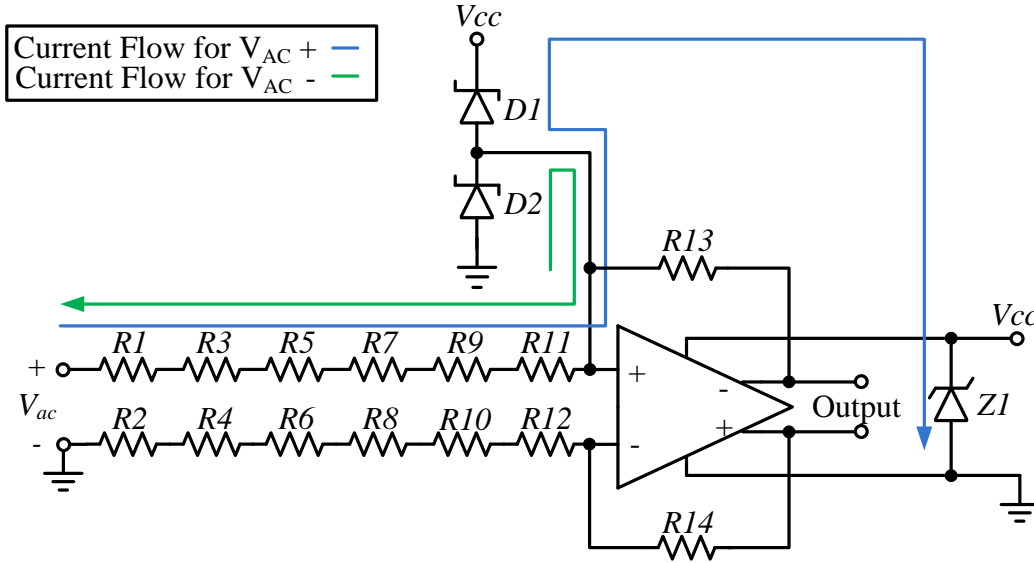


Figure A.4: Input-Voltage Measurement Protection Circuit

### A.3 TPI Bus-Voltage Measurement PCB Details

#### A.3.1 Designed Gain

As with the input-inductor current measurement PCB, the op amp circuit can be simplified to the circuit shown in Figure A.1 and the op amp gain is determined by Equation A.1.1.

As with the input-voltage measurement PCB, the two parameters to consider are the values of the resistors,  $R_F$  and  $R_{IN}$ , and their power consumption. Because of the high input voltage,  $R_{IN}$  has a power consumption problem which is solved by representing  $R_{IN}$  with multiple resistors. The values are chosen as:

$$A1 = \frac{5k2}{7 \times 270 \Omega} = 2.96 \times 10^{-3} \quad (\text{A.3.1})$$

$R_{IN}$  thus consists of 7 resistors each with the value of 270 k $\Omega$ . They are of the 1206 package and have a power rating of 250 mW. According to ideal op amp theory, the potential at the positive and negative op amp inputs are equal [43], p185. Furthermore, because this is a differential op amp, the two inputs are equal to the common-mode input potential,  $V_{CM}$ . The total potential over the 7 resistors can thus be calculated as:

$$V_{RIN} = V_{ib} - V_{CM} = 800 \text{ V} - 2.5 \text{ V} = 797.5 \text{ V} \quad (\text{A.3.2})$$

The current through these resistors is calculated as:

$$I_{IN} = \frac{V_{RIN}}{7 \times 270 \text{ k}\Omega} = 0.422 \text{ mA} \quad (\text{A.3.3})$$

The power dissipated in each resistor is thus:

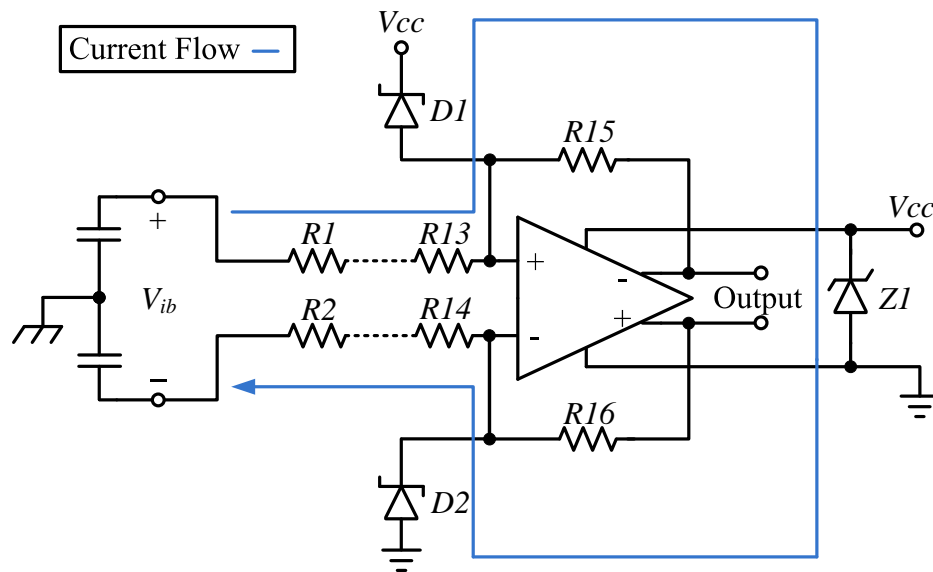
$$P = \frac{V_{RIN}}{7} \times I_{IN} = 48.07 \text{ mW} \quad (\text{A.3.4})$$

which is sufficiently lower than the 1206 resistor power rating. The two design parameters are thus within range to achieve a suitable gain.

### A.3.2 Protection Circuit

The problem arises when the connection to the Controller PCB is lost while the high input voltage is connected. The 5 V  $V_{cc}$  connection, the ground connection and the differential output pair connections are thus lost. With the op amp not powered and no current flow from the high input-voltage PCB terminal to the feedback path of the op amp, the op amp input pin will be at the same potential as the high input voltage, which will damage the op amp.

The implemented protection circuit thus consists of a *ZMM5.6* zener diode and two *BAT54* schottky diodes. As depicted in Figure A.5, the input voltage is strictly Direct Current (DC). The negative measurement PCB input is connected to the negative bus terminal and the positive measurement PCB input is connected to the positive bus terminal. The current can flow from the positive bus terminal, through *D1*, *Z1* and *D2* to the negative bus terminal. The current flow through *Z1* causes it to clamp  $V_{cc}$  at 5.6 V to power the op amp. With current flow, the voltage divider, *R1-R14*, can function properly and the op amp is protected [11].



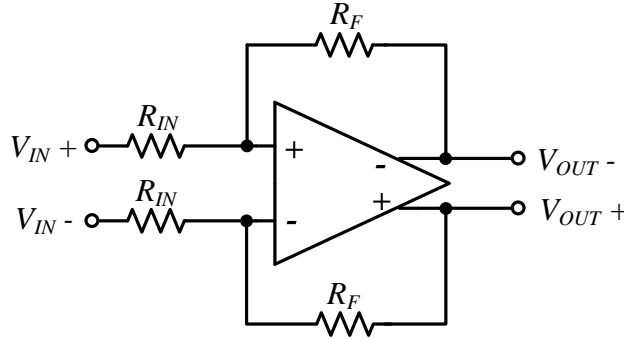
**Figure A.5:** TPI Bus-Voltage Measurement Protection Circuit

This measurement circuit design isolates the measurement PCB ground from the inverter-bus ground. This prevents the formation of a ground loop, as the input-voltage measurement PCB connects the SST-input ground to the MC ground.

## A.4 Input-Inductor Current Secondary Measurement Circuit Details

### A.4.1 Designed Gain

The main function of this op amp circuit is to scale the op amp input to the input voltage level of the ADC, which is 1.5 Volt peak to peak (V<sub>pp</sub>) and 3.25 Volt peak (V<sub>p</sub>) for each input [27]. The circuit can be simplified to the circuit shown in Figure A.6.



**Figure A.6:** Simplified Op Amp Circuit with Differential Input

The op amp gain is determined by:

$$A_2 = \frac{V_{OUT+}}{V_{IN+}} = \frac{R_F}{R_{IN}} \quad (\text{A.4.1})$$

To determine the resistor values, we have to determine the op amp input and output voltage levels.  $V_{OUT+}$  corresponds to the ADC input voltage level.  $V_{IN+}$  can be determined by the following equation, where  $V_{IN}$  is the LEM current transducer maximum output-voltage level and  $A_1$  is the op amp gain of the input-inductor current measurement PCB.

$$V_{IN+} = V_{IN} \times A_1 = 4\text{Vpp} \times 0.5 = 2\text{Vpp} \quad (\text{A.4.2})$$

The op amp gain can thus be calculated as:

$$A_2 = \frac{V_{OUT+}}{V_{IN+}} = \frac{1.5 \text{ Vpp}}{2 \text{ Vpp}} = 0.75 \quad (\text{A.4.3})$$

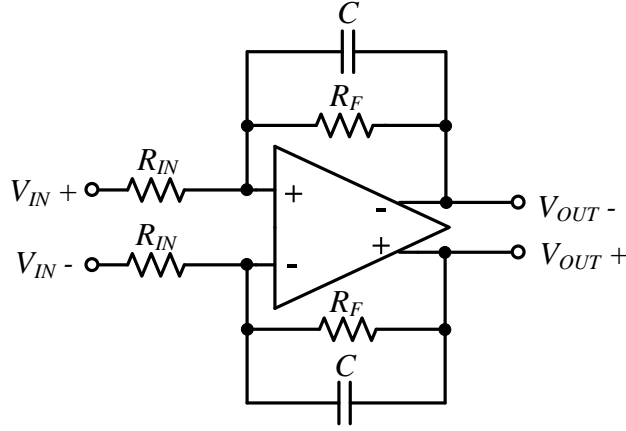
The value of  $R_F$  and  $R_{IN}$  is thus chosen as 750  $\Omega$  and 1 k $\Omega$  respectively with the actual gain as:

$$A_2 = \frac{R_F}{R_{IN}} = \frac{750 \Omega}{1 \text{ k}\Omega} = 0.75 \quad (\text{A.4.4})$$

### A.4.2 Filter Design

The low-pass filter circuit incorporated in the op amp circuit can be simplified as shown in Figure A.7.

This filter transfer function is thus calculated as:



**Figure A.7:** Simplified Low Pass Filter Circuit Incorporated in Op Amp Circuit

$$G_1(s) = \frac{V_{OUT+}}{V_{IN+}} = \frac{\frac{1}{CR_{IN}}}{s + \frac{1}{CR_F}} \quad (\text{A.4.5})$$

The input-inductor current is expected to have a switching-frequency ripple of  $n \times f_{ar}$ , caused by the switching of the cascaded ARs, discussed in Section 5.2.1. The current-loop bandwidth however, is much lower. It is initially designed for a single AR and subsequently expanded for an  $N$  AR stack. This means that  $f_{ar}$  is the primary current ripple of concern. The filter cutoff frequency is thus chosen in the order of 1 MHz, around a decade higher than the ripple frequency. This is to enable the measurement of some switching harmonics and prevent any significant phase shift. The capacitor value is thus chosen as 100 pF which leads to the filter transfer function:

$$G_1(s) = \frac{1 \times 10^7}{s + 1.333 \times 10^7} \quad (\text{A.4.6})$$

The frequency response of filter  $G_1(s)$  is shown in Figure A.8.

The ADC inputs are driven through two  $56 \Omega$  resistors,  $R_S$ , as suggested in [27]. These resistors decouple the op amp outputs from the ADC capacitive load,  $C_{ADC}$ , to avoid gain peaking. These resistors, together with  $C_{ADC}$ , also form a  $1^{st}$  order low-pass filter. The original design of the  $1^{st}$  filter is flawed in that the op amp drives a capacitive load, regardless of  $R_S$ . Due to this flaw, a shunt capacitor,  $C_{SHUNT}$ , is added to the  $2^{nd}$  low-pass filter to adjust its cutoff frequency. This filter is depicted in Figure A.9.

The value of  $C_{SHUNT}$  is determined through trial and error by examining the measurement noise with specific capacitor values. Two 16 pF capacitors in parallel give desirable results. This differential filter can be analysed as a single-ended filter once it has been converted as shown in Figure A.10 [46].

The filter transfer function is thus calculated as:

$$G_2(s) = \frac{V_{OUT}}{V_{IN}} = \frac{\frac{1}{2CR}}{s + \frac{1}{2CR}} = \frac{1.276 \times 10^8}{s + 1.276 \times 10^8} \quad (\text{A.4.7})$$

The frequency response of filter  $G_2(s)$  is shown in Figure A.11.

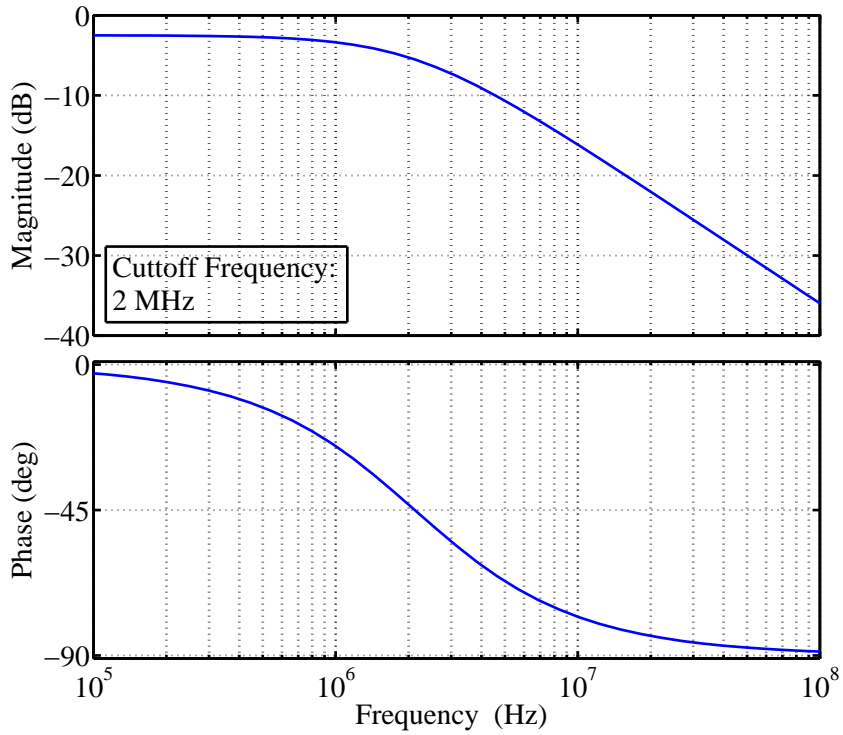


Figure A.8: Frequency Response of the Low Pass Filter Incorporated in the Op Amp Circuit

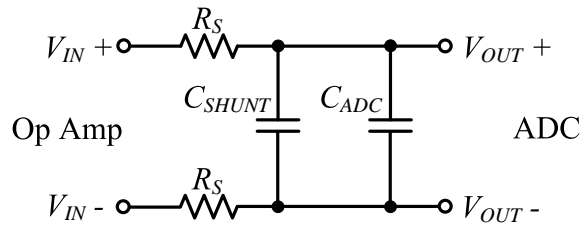


Figure A.9: Low Pass Filter Circuit Incorporated with the ADC Input Capacitance

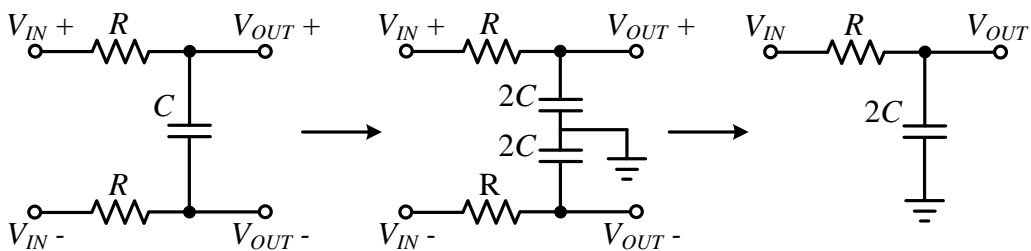
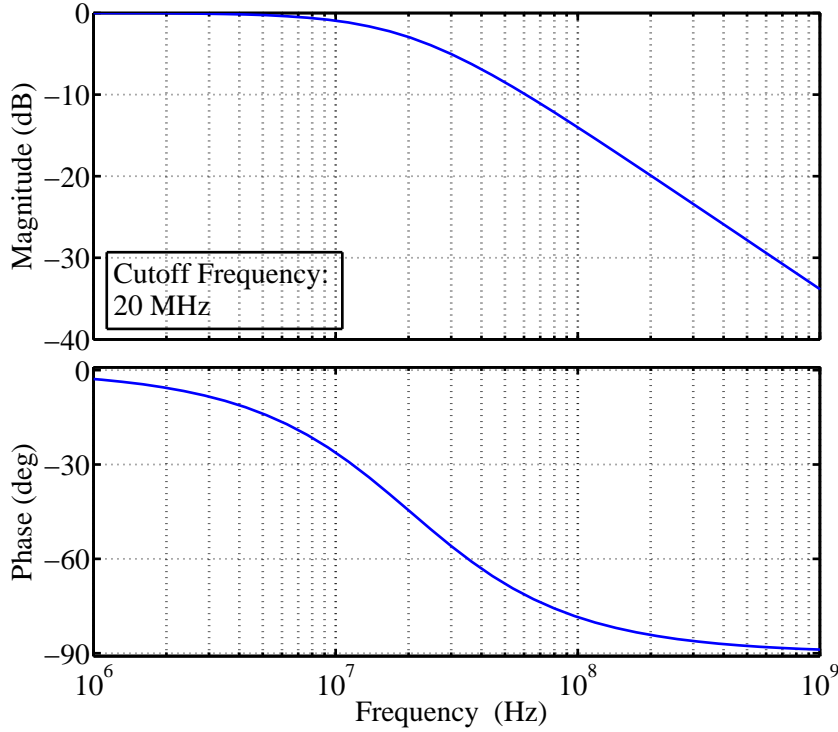


Figure A.10: Differential to Single-Ended Filter Conversion





**Figure A.11:** Frequency Response of the Low Pass Filter Incorporated with the ADC Input Capacitance

## A.5 Input Voltage Secondary Measurement Circuit Details

### A.5.1 Designed Gain

As with the input-inductor current secondary measurement circuit, the main function of this op amp circuit is to scale the op amp input to the input voltage level of the ADC, which is 1.5 Vpp and 3.25 Vp for each input [27]. The circuit can also be simplified to the circuit shown in Figure A.6 with the op amp gain determined by:

$$A_2 = \frac{V_{OUT+}}{V_{IN+}} = \frac{R_F}{R_{IN}} \quad (\text{A.5.1})$$

To determine the resistor values, we have to determine the op amp input and output voltage levels.  $V_{OUT+}$  corresponds to the ADC input voltage level.  $V_{IN+}$  can be determined by the following equation, where  $V_{IN}$  is the test supply maximum expected output-voltage level and  $A_1$  is the op amp gain of the input voltage measurement PCB.

$$V_{IN+} = V_{IN} \times A_1 = 230\text{Vp} \times 4.629 \times 10^{-3} = 2.13\text{Vpp} \quad (\text{A.5.2})$$

The op amp gain can thus be calculated as:

$$A_2 = \frac{V_{OUT+}}{V_{IN+}} = \frac{1.5 \text{ Vpp}}{2.13 \text{ Vpp}} = 0.7 \quad (\text{A.5.3})$$

The value of  $R_F$  and  $R_{IN}$  is thus chosen as 1 k $\Omega$  and 2k2 respectively with the actual gain as:

$$A_2 = \frac{R_F}{R_{IN}} = \frac{1 \text{ k}\Omega}{2\text{k}2} = 0.45 \quad (\text{A.5.4})$$

## A.5.2 Filter Design

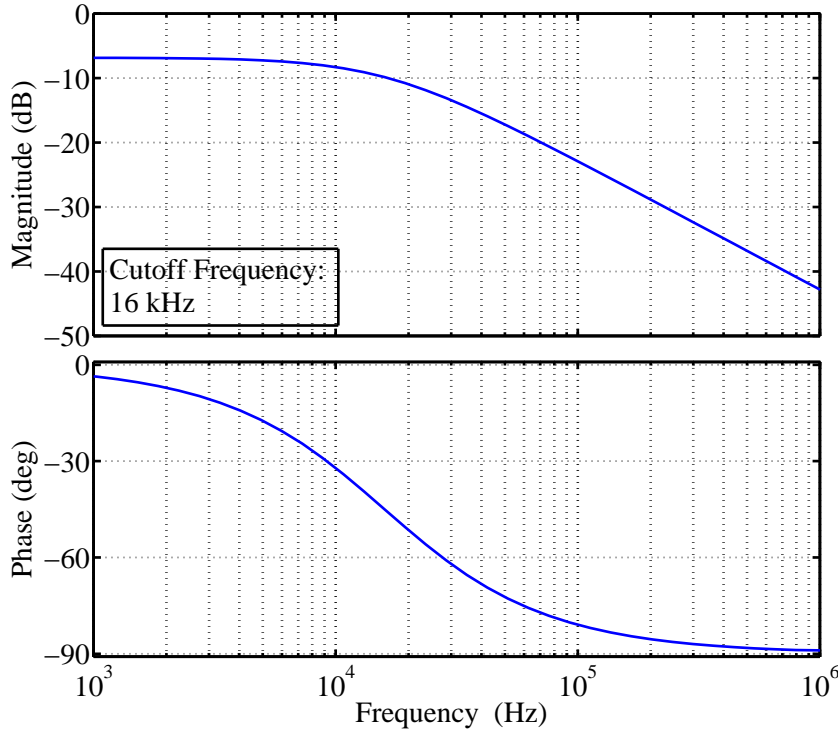
As with the input-inductor current secondary measurement circuit, the low-pass filter circuit incorporated in the op amp circuit can be simplified as shown in Figure A.7. This filter transfer function is thus calculated as:

$$G_1(s) = \frac{V_{OUT+}}{V_{IN+}} = \frac{\frac{1}{CR_{IN}}}{s + \frac{1}{CR_F}} \quad (\text{A.5.5})$$

The input voltage is at line frequency, 50 Hz. This is the highest frequency of useful information which leads to the designed filter cutoff frequency in the order of 10 kHz. The cutoff frequency is chosen around two decades higher than the line frequency to prevent any significant phase shift. The capacitor value is thus chosen as 10 nF which leads to the filter transfer function:

$$G_1(s) = \frac{4.545 \times 10^4}{s + 1 \times 10^5} \quad (\text{A.5.6})$$

The frequency response of filter  $G_1(s)$  is shown in Figure A.12.



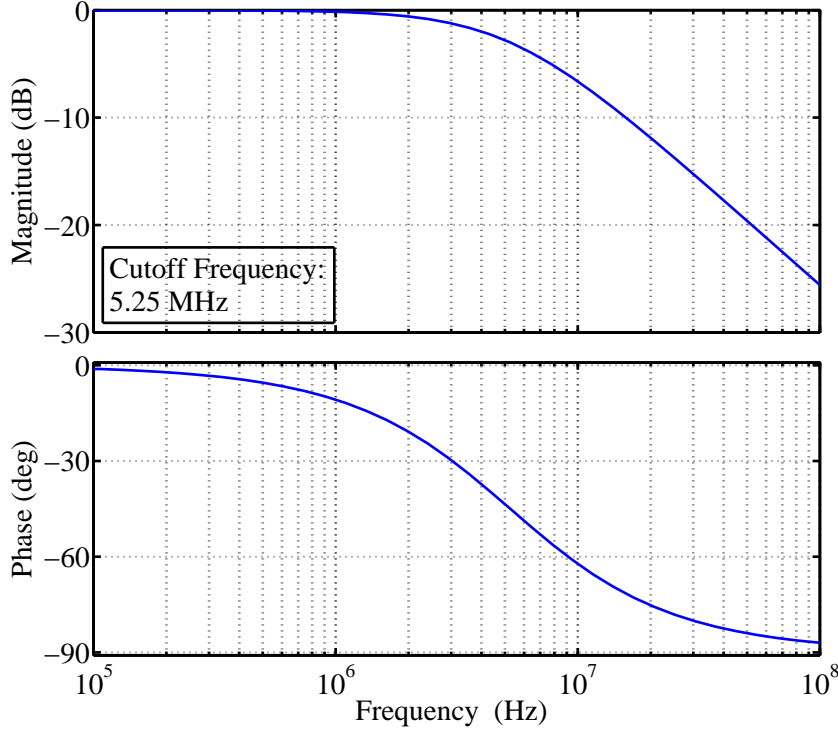
**Figure A.12:** Frequency Response of the Low Pass Filter Incorporated in the Op Amp Circuit

The ADC inputs are driven through two  $56 \Omega$  resistors,  $R_S$ , as suggested in [27]. These resistors decouple the op amp outputs from the ADC capacitive load,  $C_{ADC}$ , to avoid gain peaking. These resistors, together with  $C_{ADC}$ , also form a 1<sup>st</sup> order low-pass filter. The original design of the 1<sup>st</sup> filter is flawed in that the op amp drives a capacitive load, regardless of  $R_S$ . Due to this flaw, a shunt capacitor,  $C_{SHUNT}$ , is added to the 2<sup>nd</sup> low-pass filter to adjust its cutoff frequency. This filter is also depicted in Figure A.9. The value of  $C_{SHUNT}$  is determined through trial and error by examining the measurement noise with specific capacitor values. Two 16 pF capacitors together with a 100 pF capacitor in parallel gives desirable results. This differential filter can be

analysed as a single-ended filter once it has been converted as shown in Figure A.10 [46]. The filter transfer function is thus calculated as:

$$G_2(s) = \frac{V_{OUT}}{V_{IN}} = \frac{\frac{1}{2CR}}{s + \frac{1}{2CR}} = \frac{3.307 \times 10^7}{s + 3.307 \times 10^7} \quad (\text{A.5.7})$$

The frequency response of filter  $G_2(s)$  is shown in Figure A.13.



**Figure A.13:** Frequency Response of the Low Pass Filter Incorporated with the ADC Input Capacitance

## A.6 TPI Bus-Voltage Secondary Measurement Circuit Details

### A.6.1 Designed Gain

As with the input-inductor current secondary measurement circuit, the main function of this op amp circuit is to scale the op amp input to the input voltage level of the ADC, which is 1.5 V<sub>pp</sub> and 3.25 V<sub>p</sub> for each input [27]. The circuit can also be simplified to the circuit shown in Figure A.6 with the op amp gain determined by:

$$A_2 = \frac{V_{OUT+}}{V_{IN+}} = \frac{R_F}{R_{IN}} \quad (\text{A.6.1})$$

To determine the resistor values, we have to determine the op amp input and output voltage levels.  $V_{OUT+}$  corresponds to the ADC input voltage level.  $V_{IN+}$  can be determined by the following equation, where  $V_{IN}$  is the  $V_{ib}$  positive terminal maximum expected voltage level and  $A_1$  is the op amp gain of the bus-voltage measurement PCB.

$$V_{IN+} = V_{IN} \times A1 = 450\text{Vpp} \times 2.96 \times 10^{-3} = 1.33\text{Vpp} \quad (\text{A.6.2})$$

The bus-voltage measurement is different to the input-inductor current and input-voltage measurements in that it is a DC measurement. This means that the measurement peak-to-peak value ranges from zero to a maximum and does not swing around zero. The gain is thus calculated with half of the Vpp rating of the ADC to satisfy its Vp requirement in the following equation:

$$A2 = \frac{V_{OUT+}}{V_{IN+}} = \frac{\frac{1.5 \text{ Vpp}}{2}}{1.33 \text{ Vpp}} = 0.564 \quad (\text{A.6.3})$$

The value of  $R_F$  and  $R_{IN}$  is thus chosen as  $560 \Omega$  and  $1 \text{ k}\Omega$  respectively with the actual gain as:

$$A2 = \frac{R_F}{R_{IN}} = \frac{560 \Omega}{1 \text{ k}\Omega} = 0.56 \quad (\text{A.6.4})$$

## A.6.2 Filter Design

As with the input-inductor current secondary measurement circuit, the low-pass filter circuit incorporated in the op amp circuit can be simplified as shown in Figure A.7. The filter transfer function is thus calculated as:

$$G_1(s) = \frac{V_{OUT+}}{V_{IN+}} = \frac{\frac{1}{CR_{IN}}}{s + \frac{1}{CR_F}} \quad (\text{A.6.5})$$

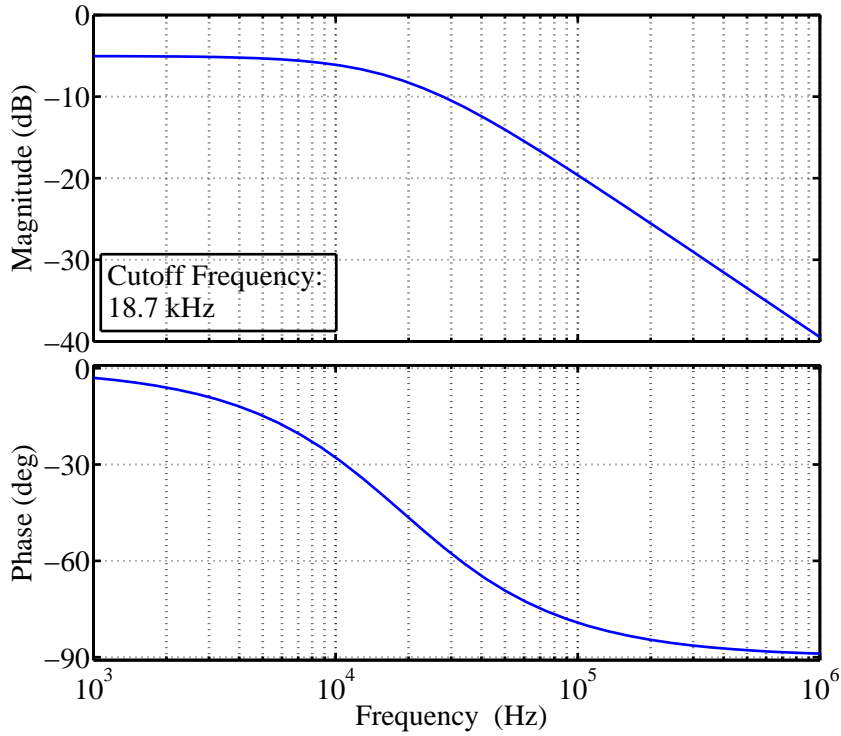
The bus voltage is at DC and the voltage loop responsible for the control of this voltage has a bandwidth in the order of 5 Hz to 50 Hz. This is the highest frequency of useful information which leads to the designed filter cutoff frequency in the order of 10 kHz. The cutoff frequency is chosen around two decades higher than the voltage-loop bandwidth to allow design freedom while prevent any significant phase shift. The capacitor value is thus chosen as 15 nF which leads to the filter transfer function:

$$G_1(s) = \frac{6.667 \times 10^4}{s + 1.19 \times 10^5} \quad (\text{A.6.6})$$

The frequency response of filter  $G_1(s)$  is shown in Figure A.14.

The ADC inputs are driven through two  $56 \Omega$  resistors,  $R_S$ , as suggested in [27]. These resistors decouple the op amp outputs from the ADC capacitive load,  $C_{ADC}$ , to avoid gain peaking. These resistors, together with  $C_{ADC}$ , also form a 1<sup>st</sup> order low-pass filter. The original design of the 1<sup>st</sup> filter is flawed in that the op amp drives a capacitive load, regardless of  $R_S$ . Due to this flaw, a shunt capacitor,  $C_{SHUNT}$ , is added to the 2<sup>nd</sup> low-pass filter to adjust its cutoff frequency. This filter is also depicted in Figure A.9. The value of  $C_{SHUNT}$  is determined through trial and error by examining the measurement noise with specific capacitor values. Two 16 pF capacitors together with a 100 pF capacitor in parallel gives desirable results. As with the input-voltage secondary measurement circuit, this differential filter can be analysed as a single-ended filter once it has been converted as shown in Figure A.10 [46]. The filter transfer function is thus calculated as:

$$G_2(s) = \frac{V_{OUT}}{V_{IN}} = \frac{\frac{1}{2CR}}{s + \frac{1}{2CR}} = \frac{3.307 \times 10^7}{s + 3.307 \times 10^7} \quad (\text{A.6.7})$$



**Figure A.14:** Frequency Response of the Low Pass Filter Incorporated in the Op Amp Circuit

The frequency response of filter  $G_2(s)$  is shown in Figure A.13.

## A.7 ADC Design Details

### A.7.1 ADC Conversion

The ADC input ratings are 1.5 V<sub>pp</sub> with a 2.5 V Common Mode Voltage ( $V_{cm}$ ). These inputs are converted to a 12 bit digital output. Figure A.15 shows how the maximum, minimum and zero input values correspond to the digital output values.

The conversion ratio thus is calculated as:

$$RATIO = \frac{\text{Digital output value}}{IN_{TOT}} = \frac{0xFFF}{3 \text{ V}} = \frac{1}{732.42 \mu\text{V}} \quad (\text{A.7.1})$$

### A.7.2 Clock Termination

The signal integrity of the high frequency ADC input clock is of concern. At such high frequencies, PCB traces become Radio Frequency (RF) transmission lines and cannot be treated as simple connection-wires. Signal integrity is threatened by transmission line effects and interaction between circuits [34]. Series termination is thus implemented in the same way as with the DDR signals, discussed in Appendix A.8.1.

Input (IN+) - (IN-) = (IN <sub>TOT</sub> )	Output HEX	Binary
(3.25 V) - (1.75 V) = (1.5 V)	FFF	1111 1111 1111
(2.5 V) - (2.5 V) = (0 V)	800	1000 0000 0000
(1.75 V) - (3.25 V) = (-1.5 V)	000	0000 0000 0000

Figure A.15: ADC Conversion Diagram

## A.8 DDR design Details

### A.8.1 Single-Ended Line-Termination

[47] Recommends series termination for DDR designs with less than four DDR memory IC's and trace lengths of less than 2 inches. Series termination dampens overshoot and simplifies PCB routing. Figure A.16 depicts series termination with a series resistor,  $R_S$ , physically close to the FPGA for unidirectional signals and in the middle of the trace for bidirectional signals.  $C$  is discarded for a bidirectional signal.

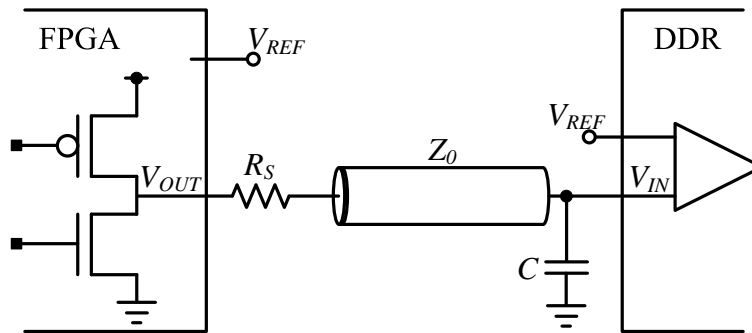


Figure A.16: Series Termination Circuit

The values of  $R_S$  and the trace impedance,  $Z_0$ , are jointly chosen with a few considerations in mind. Firstly the availability of the chosen  $R_S$  value, secondly the recommended trace width which is used in Appendix A.8.4 to calculate  $Z_0$  and thirdly:

$$Z_0 = R_{OUT} + R_S \tag{A.8.1}$$

With the FPGA output-impedance:

$$R_{OUT} = 25 \Omega \tag{A.8.2}$$

$R_S$  is chosen as  $63 \Omega$  and  $Z_0$  is calculated as  $82.15 \Omega$  with:

$$\begin{aligned} W &= 0.1524 \text{ mm} \\ t &= 0.035 \text{ mm} \\ h &= 0.2 \text{ mm} \end{aligned}$$

The DDR memory operates with the Stub Series Terminated Logic for 2.5V (SSTL-2) Class II I/O standard. The following calculations are to check if the chosen  $R_S$  and  $Z_0$  values satisfy the relevant I/O specifications. The minimum DDR input high voltage is given as:

$$V_{IHmin} = V_{ref} + 0.15 \text{ V} = 1.25 + 0.15 = 1.4 \text{ V} \quad (\text{A.8.3})$$

The minimum FPGA output high voltage is given as:

$$V_{OHmin} = V_{ref} + 0.76 \text{ V} = 1.25 + 0.76 = 2.01 \text{ V} \quad (\text{A.8.4})$$

This means the minimum needed FPGA output high current is:

$$I_{OHmin} = \frac{V_{OHmin} - V_{IHmin}}{R_S} = 9.84 \text{ mA} \quad (\text{A.8.5})$$

Which is less than the rated FPGA output high current of 16.4 mA. For communication in the opposite direction, the minimum FPGA input high voltage is given as:

$$V_{IHmin} = V_{ref} + 0.18 \text{ V} = 1.25 + 0.18 = 1.43 \text{ V} \quad (\text{A.8.6})$$

The minimum DDR output high voltage is given as:

$$V_{OHmin} = V_{ref} + 0.76 \text{ V} = 1.25 + 0.42 = 1.67 \text{ V} \quad (\text{A.8.7})$$

This means the minimum needed DDR output high current is:

$$I_{OHmin} = \frac{V_{OHmin} - V_{IHmin}}{R_S} = 3.87 \text{ mA} \quad (\text{A.8.8})$$

Which is much less than the rated DDR output high current of 16.8 mA. These results prove that the chosen  $R_S$  and  $Z_0$  values are compatible with the I/O standard in question.

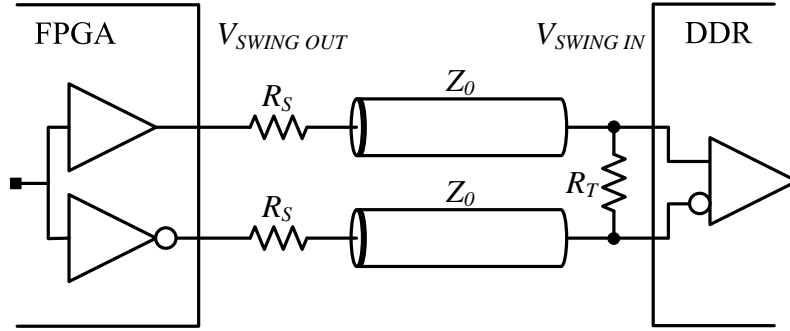
## A.8.2 Differential Line-Termination

[47] Recommends differential termination for the DDR CK and CK# traces with the termination resistor of between 100  $\Omega$  and 200  $\Omega$ . Figure A.17 depicts differential termination with series resistors,  $R_S$ , physically close to the FPGA and a termination resistor,  $R_T$ , physically close to the DDR.

The values of  $R_S$ ,  $R_T$  and the trace impedance,  $Z_0$ , are jointly chosen with a few considerations in mind. Firstly the availability of the chosen  $R_S$  value, secondly the recommended trace width which is used in Appendix A.8.5 to calculate  $Z_0$  and thirdly the differential clock signals example 5.4.1 in [48].  $Z_0$  is calculated as 100.3  $\Omega$  with:

$$\begin{aligned} W &= 6 \text{ mil} \\ S &= 7 \text{ mil} \\ t &= 1.378 \text{ mil} \\ B &= 26.181 \text{ mil} \end{aligned}$$

The series and termination resistors are thus chosen as:



**Figure A.17:** Differential Termination Circuit

$$R_S = 50 \, \Omega \quad (\text{A.8.9})$$

$$R_T = 100 \, \Omega \quad (\text{A.8.10})$$

The DDR memory operates with the SSTL-2 Class II I/O standard. The following calculations are to check if the chosen  $R_S$ ,  $R_T$  and  $Z_0$  values satisfy the relevant I/O specifications. The FPGA minimum output high and maximum output low voltages are given as:

$$V_{0Hmin} = V_{ref} + 0.76 \, \text{V} = 1.25 + 0.76 = 2.01 \, \text{V} \quad (\text{A.8.11})$$

$$V_{0Lmax} = V_{ref} - 0.76 \, \text{V} = 1.25 - 0.76 = 0.49 \, \text{V} \quad (\text{A.8.12})$$

The minimum FPGA swing output voltage is thus calculated as:

$$V_{SWINGOUTmin} = V_{0Hmin} - V_{0Lmax} = 1.52 \, \text{V} \quad (\text{A.8.13})$$

The current through the termination network can be calculated as:

$$I = \frac{V_{SWINGOUTmin}}{R_S + R_T + R_S} = 7.6 \, \text{mA} \quad (\text{A.8.14})$$

The minimum DDR input high voltage can now be calculated as:

$$V_{IHmin} = V_{0Hmin} - (I \times R_S) = 1.63 \, \text{V} \quad (\text{A.8.15})$$

Which is more than the minimum DDR rating of 1.6 V. The maximum DDR input low voltage can now be calculated as:

$$V_{ILmax} = V_{0Hmin} - (I \times (R_S + R_T)) = 0.87 \, \text{V} \quad (\text{A.8.16})$$

Which is less than the maximum DDR rating of 0.9 V. These results prove that the chosen  $R_S$ ,  $R_T$  and  $Z_0$  values are compatible with the I/O standard in question.

### A.8.3 PCB Layout Considerations

There are four aspects to consider when designing the high-speed PCB section connecting DDR memory to its controller, the FPGA. Firstly the orientation and distance of the DDR unit with respect to the FPGA. Secondly, trace length which has certain specifications. The third aspect is on which layer to route each trace type and the fourth is trace spacing. Trace thickness, on the other hand, is determined by the impedance calculations in Appendix A.8.1 and A.8.2 respectively.



The DDR signals are grouped into 3 sets, namely the Clock set, the Data/Data-strobe set and the Address/Command/Control set. Trace lengths and spacings are specified in [47]. It is also recommended to route the Data/Data-strobe set on an outer PCB layer, the Address/Command/Control set on the other outer PCB layer and the Clock set on an inner PCB layer. Figure A.18 shows the orientation of the DDR memory with respect to the FPGA which determines the maximum trace length. To stay within specifications for trace-length differences, the traces starting closer to the FPGA are lengthened by S-bends to optimize the available space between the DDR and the FPGA. The last design technique to minimize cross-talk and noise, is to shield every signal layer with adjacent ground planes.

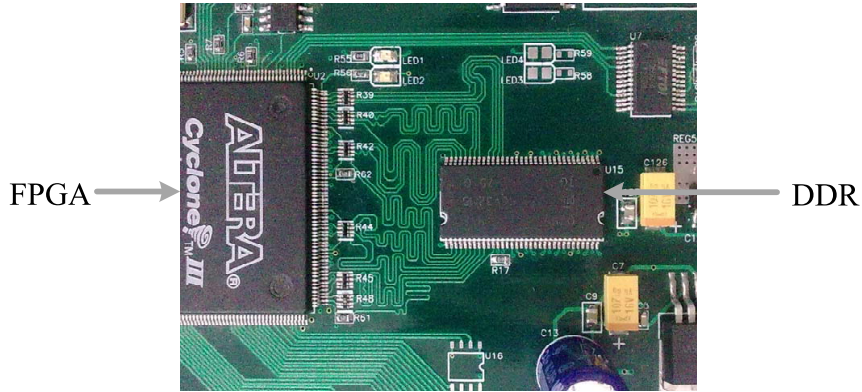


Figure A.18: DDR Orientation with respect to the FPGA

### A.8.4 Single-Ended Trace Impedance Calculation

The trace impedance is calculated with an on-line microstrip transmission line characteristic impedance calculator [49]. This calculator uses the parameters shown in Figure A.19 where:

- $\epsilon_r$  = Relative Dielectric Constant
- W = Width of trace
- t = Thickness of trace
- h = Thickness of dielectric

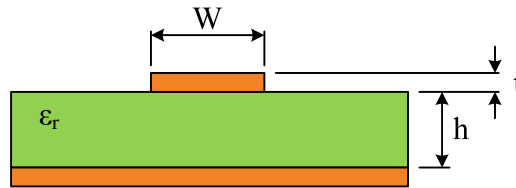


Figure A.19: Impedance Calculation Parameters

The relative dielectric constant,  $\epsilon_r$ , for FR4<sup>1</sup> is 4.2. throughout the scope of this thesis. The calculator uses the following equations derived from [50], p94:

For  $\frac{W}{h} < 1$ :

<sup>1</sup>FR4 is the specific fibre glass commonly used as dielectric in PCBs.

$$Z_o = \frac{60}{\sqrt{\epsilon_{\text{eff}}}} \times \ln \left( \frac{8h}{W} + \frac{W}{4h} \right) \quad (\text{A.8.17})$$

$$\epsilon_{\text{eff}} = \frac{\epsilon_r + 1.0}{2} + \frac{\epsilon_r - 1.0}{2} \left[ \frac{1}{\sqrt{1 + \frac{12h}{W}}} + 0.04 \left( 1 - \frac{W}{h} \right)^2 \right] \quad (\text{A.8.18})$$

Else :

$$Z_o = \frac{120\pi}{\sqrt{\epsilon_{\text{eff}}}} \times \frac{1}{\left( \frac{W}{h} + 1.393 + 0.677 \times \ln \left( \frac{W}{h} + 1.444 \right) \right)} \quad (\text{A.8.19})$$

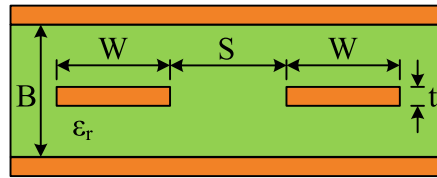
$$\epsilon_{\text{eff}} = \frac{\epsilon_r + 1.0}{2} + \frac{\epsilon_r - 1.0}{2} \left[ \frac{1}{\sqrt{1 + \frac{12h}{W}}} \right] \quad (\text{A.8.20})$$

The trace impedance result calculated using this calculator coincides with the result when using CST Microwave Studio, a well known simulation package used in the field of Electro Magnetics.

### A.8.5 Differential Trace Impedance Calculation

The differential trace impedance is calculated with the on-line Differential Stripline Impedance Calculator from IDEA Consulting [51]. This calculator uses the parameters shown in Figure A.20 where:

- $\epsilon_r$  = Relative Dielectric Constant
- W = Width of traces
- S = Distance between traces
- t = Thickness of trace
- B = Thickness of dielectric



**Figure A.20:** Differential Impedance Calculation Parameters

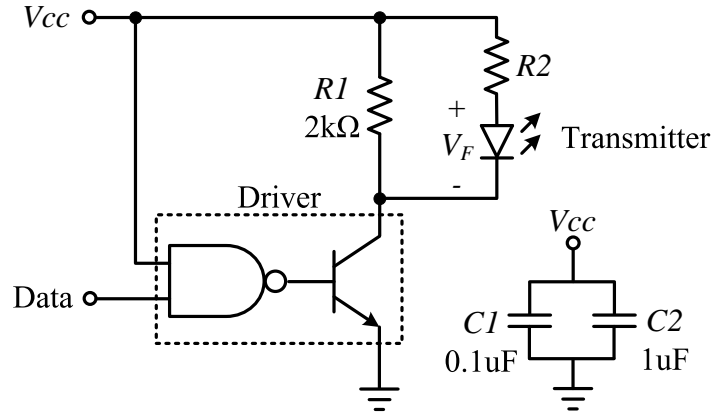
The relative dielectric constant,  $\epsilon_r$ , for FR4<sup>2</sup> is 4.2. throughout the scope of this thesis. The equations used by this calculator can be found in [50], p232-235, and are too extensive to include in this appendix.

<sup>2</sup>FR4 is the specific fibre glass commonly used as dielectric in PCBs.

## A.9 Fibre-Optic Interface PCB Details

### A.9.1 Fibre-Optic Driver Design

The only design parameter present in the driver circuit is  $R2$  as shown in Figure A.21. The fibre-optic transmitter recommended operating conditions state a peak forward current of between 20 mA and 90 mA but with a maximum average forward current of 60 mA [52]. Seeing that there are 17 of these circuits on a fibre-optic interface PCB, an average forward current of <30 mA is chosen to reduce power usage. The transmitter forward voltage is 2.1 V and so  $R2$  is calculated as:



**Figure A.21:** Fibre-Optic Transmitter Driving Circuit

$$R2 = \frac{V_{CC} - V_F}{I_F} = \frac{5 - 2.1}{30 \times 10^{-3}} \approx 100\Omega \quad (\text{A.9.1})$$

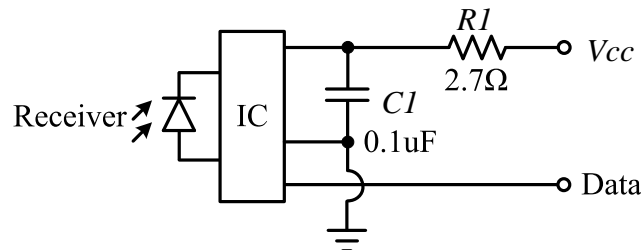
The power dissipated by the resistor is:

$$P = I_F^2 \times R2 = 84.1 \text{ mW} \quad (\text{A.9.2})$$

This results in the choice of the 1206 resistor package with a power rating of 250 mW.

### A.9.2 Fibre-Optic Receiver Circuit

There are no design parameters present in the receiving circuit as shown in Figure A.22.



**Figure A.22:** Fibre-Optic Receiver Circuit

# Appendix B

## Active-Rectifier Control Details

### B.1 Current-Loop Plant Linearisation details

#### B.1.1 Step 1: Determine State-Space Variables

To determine the AR state-space variables, the four circuit states are analysed as listed below:

<i>State</i>	<i>Active Switches</i>	$V_{ac}$	$V_{ab}$
1	$S_1; S_3$ or $S_2; S_4$	$> 0$	$0 \text{ V}$
2	$S_1; S_4$	$> 0$	$V_{cb}$
3	$S_1; S_3$ or $S_2; S_4$	$< 0$	$0 \text{ V}$
4	$S_2; S_3$	$< 0$	$-V_{cb}$

**Table B.1:** Active-Rectifier Circuit States

The switch symbols are used as depicted in Figure 4.4. States 1 and 2 yield identical differential equations to that of states 3 and 4. Therefore only the first two states are analysed. This analysis assumes the switches and diodes to be ideal and that the AR operates in continuous-conduction mode. The input-inductor resistance,  $R_L$ , is included in the analysis however, the equivalent series resistance of the bus capacitor is ignored. The effects of dead-time are also ignored. The state-variable vector,  $\mathbf{x}$ , and the state output,  $y$ , are defined as:

$$\mathbf{x} = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} i_L \\ v_{cb} \end{bmatrix} \quad (\text{B.1.1})$$

$$y = i_L \quad (\text{B.1.2})$$

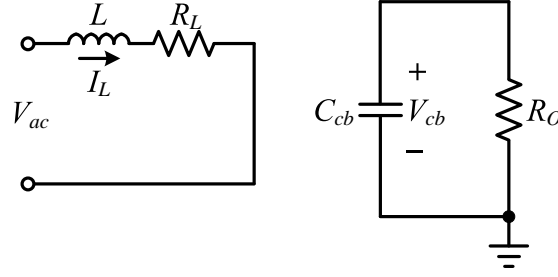
State 1 is represented by the circuit diagram shown in Figure B.1, which yields the following state equation and output equation during  $d \cdot T_{ar}$ :

$$\dot{\mathbf{x}} = \mathbf{A}_1 \mathbf{x} + \mathbf{B}_1 v_{ac} \quad (\text{B.1.3})$$

$$y = \mathbf{C}_1 \mathbf{x} \quad (\text{B.1.4})$$

where

$$\mathbf{A}_1 = \begin{bmatrix} -\frac{R_L}{L} & 0 \\ 0 & -\frac{1}{C_{cb}R_O} \end{bmatrix}; \mathbf{B}_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}; \mathbf{C}_1 = [1 \ 0] \quad (\text{B.1.5})$$


**Figure B.1:** Active Rectifier Circuit: State 1

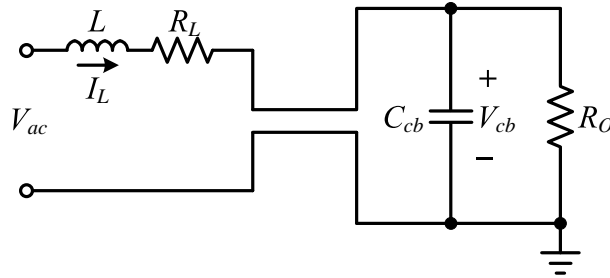
State 2 is represented by the circuit diagram shown in Figure B.2, which yields the following state equation and output equation during  $(1 - d) \cdot T_{ar}$ :

$$\dot{\mathbf{x}} = \mathbf{A}_2 \mathbf{x} + \mathbf{B}_2 v_{ac} \quad (\text{B.1.6})$$

$$y = \mathbf{C}_2 \mathbf{x} \quad (\text{B.1.7})$$

where

$$\mathbf{A}_2 = \begin{bmatrix} -\frac{R_L}{L} & -\frac{1}{L} \\ \frac{1}{C_{cb}} & -\frac{1}{C_{cb}R_O} \end{bmatrix}; \mathbf{B}_2 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}; \mathbf{C}_2 = [1 \ 0] \quad (\text{B.1.8})$$


**Figure B.2:** Active Rectifier Circuit: State 2

### B.1.2 Step 3: Determine Perturbation Equations

The perturbation,  $\tilde{v}_{ac}$ , is assumed to be zero due to the slow-changing<sup>1</sup>  $v_{ac}$ , compared to  $i_L$ . The perturbation equations are calculated from Eq 4.2.17 to 4.2.22. Substitution yields:

$$\begin{aligned} \dot{\mathbf{X}} + \dot{\tilde{\mathbf{x}}} &= [\mathbf{A}_1 D + \mathbf{A}_2 (1 - D)] \mathbf{X} + [\mathbf{A}_1 D + \mathbf{A}_2 (1 - D)] \tilde{\mathbf{x}} + [\mathbf{B}_1 D + \mathbf{B}_2 (1 - D)] V_{ac} \\ &+ [(\mathbf{A}_1 - \mathbf{A}_2) \mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2) V_{ac}] \tilde{d} + [(\mathbf{A}_1 - \mathbf{A}_2) \tilde{\mathbf{x}}] \tilde{d} \end{aligned} \quad (\text{B.1.9})$$

However:

$$\dot{\mathbf{X}} = 0 \quad (\text{B.1.10})$$

<sup>1</sup>The input voltage,  $v_{ac}$ , has a frequency of 50 Hz.

and terms containing products of  $\tilde{\mathbf{x}}$  and  $\tilde{d}$  are neglected. The steady-state state equation is obtained by setting the perturbations and their time derivatives to zero:

$$\mathbf{A}\mathbf{X} + \mathbf{B}V_{ac} = 0 \quad (\text{B.1.11})$$

with

$$\mathbf{A} = \mathbf{A}_1D + \mathbf{A}_2(1 - D) \quad (\text{B.1.12})$$

and

$$\mathbf{B} = \mathbf{B}_1D + \mathbf{B}_2(1 - D) \quad (\text{B.1.13})$$

The perturbation state-equation is thus given as:

$$\dot{\tilde{\mathbf{x}}} = \mathbf{A}\tilde{\mathbf{x}} + [(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)V_{ac}]\tilde{d} \quad (\text{B.1.14})$$

Similarly, substitution yields the steady-state output equation:

$$\mathbf{Y} = \mathbf{C}\mathbf{X} \quad (\text{B.1.15})$$

with

$$\mathbf{C} = \mathbf{C}_1D + \mathbf{C}_2(1 - D) \quad (\text{B.1.16})$$

and the perturbation output-equation is given as:

$$\tilde{y} = \mathbf{C}\tilde{\mathbf{x}} + [(\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X}]\tilde{d} \quad (\text{B.1.17})$$

### B.1.3 Step 4: Determine Plant Transfer Function

The perturbation equations established in Appendix B.1.2 can be simplified by examining the two specific states in question. The state matrices and vectors of Eq. B.1.5 and B.1.8 yield:

$$\mathbf{B}_1 = \mathbf{B}_2 \quad (\text{B.1.18})$$

and

$$\mathbf{C}_1 = \mathbf{C}_2 \quad (\text{B.1.19})$$

The perturbation state- and output-equation are therefor:

$$\dot{\tilde{\mathbf{x}}} = \mathbf{A}\tilde{\mathbf{x}} + [(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X}]\tilde{d} \quad (\text{B.1.20})$$

and

$$\tilde{y} = \mathbf{C}\tilde{\mathbf{x}} \quad (\text{B.1.21})$$

Taking the Laplace transform of each perturbation term results in:

$$s\tilde{\mathbf{x}}(s) = \mathbf{A}\tilde{\mathbf{x}}(s) + [(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X}]\tilde{d}(s) \quad (\text{B.1.22})$$

or

$$\tilde{\mathbf{x}}(s) = [s\mathbf{I} - \mathbf{A}]^{-1} [(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X}]\tilde{d}(s) \quad (\text{B.1.23})$$

and

$$\tilde{y}(s) = \mathbf{C}\tilde{\mathbf{x}}(s) \quad (\text{B.1.24})$$

Substitution of Eq. B.1.23 into Eq. B.1.24 yields the desired linear transfer function:

$$G_I(s) = \frac{\tilde{y}(s)}{\tilde{d}(s)} = \frac{\tilde{i}_L(s)}{\tilde{d}(s)} = \mathbf{C}[\mathbf{sI} - \mathbf{A}]^{-1} [(\mathbf{A}_1 - \mathbf{A}_2) \mathbf{X}] \quad (\text{B.1.25})$$

of the plant with the switch duty ratio perturbation as input and the input-inductor current perturbation as output.  $\mathbf{I}$  is defined as a  $2 \times 2$  identity-matrix.

### B.1.4 Step 5: Plant Transfer Function in Symbolic Form

Substitution of the symbolic state matrices ( $\mathbf{A}_1$ ,  $\mathbf{A}_2$ ) and the row vectors ( $\mathbf{C}_1$ ,  $\mathbf{C}_2$ ) into Eq. B.1.25 results in the symbolic plant transfer function:

$$G_I(s) = \frac{\frac{V_{cb}s}{L} + \frac{V_{cb}}{R_O LC_{cb}} + \frac{I_L(1-D)}{LC_{cb}}}{s^2 + \left(\frac{R_L}{L} + \frac{1}{R_O C_{cb}}\right)s + \frac{R_L}{R_O LC_{cb}} + \frac{(1-D)^2}{LC_{cb}}} \quad (\text{B.1.26})$$

The boost ratio of a step-up converter, as discussed in [37], p173, is given as:

$$\frac{V_{cb}}{V_{ac}} = \frac{1}{1-D} \quad (\text{B.1.27})$$

with an RMS value of  $V_{ac}$  in this case. Assuming a lossless circuit yields:

$$\frac{I_L}{I_{cb}} = \frac{1}{1-D} \quad (\text{B.1.28})$$

Using Ohm's law and rearranging terms, yields:

$$I_L = \frac{V_{cb}}{R_O(1-D)} \quad (\text{B.1.29})$$

Substituting Eq. B.1.29 into Eq. B.1.26 results in the simplified plant transfer function:

$$G_I(s) = \frac{V_{cb}}{L} \times \frac{s + \frac{2}{R_O C_{cb}}}{s^2 + \left(\frac{R_L}{L} + \frac{1}{R_O C_{cb}}\right)s + \frac{R_L}{R_O LC_{cb}} + \frac{(1-D)^2}{LC_{cb}}} \quad (\text{B.1.30})$$

### B.1.5 Step 6: Quantify Plant Transfer Function

The DC operating point is used to quantify the model. This operating point is determined by the system parameters as listed below. Starting with the predefined SST parameter:

Parameter	Symbol	Equation	Value	Units
SST Power Rating	$P_{SST}$		60	kW

**Table B.2:** SST Parameter

The predefined phase parameters:

Parameter	Symbol	Equation	Value	Units
Phase Power Rating	$P_{ph}$	$P_{SST} \div 3 =$	20	kW
3-Phase Input Line-Voltage	$V_{ll}$		6.6	kV rms
3-Phase Input Phase-Voltage	$V_{ph}$	$V_{ll} \div \sqrt{3} =$	3.81	kV rms
Input-Inductor Current	$I_L$	$P_{ph} \div V_{ph} =$	5.25	A rms
Peak Inductor Current	$I_{Lp}$	$I_L \times \sqrt{2} =$	7.42	Ap
Peak Input Phase-Voltage	$V_{php}$	$V_{ph} \times \sqrt{2} =$	5.39	kVp
Number of Cells per Phase	$N$		15	Units

**Table B.3:** Phase Parameters

The predefined cell parameters:

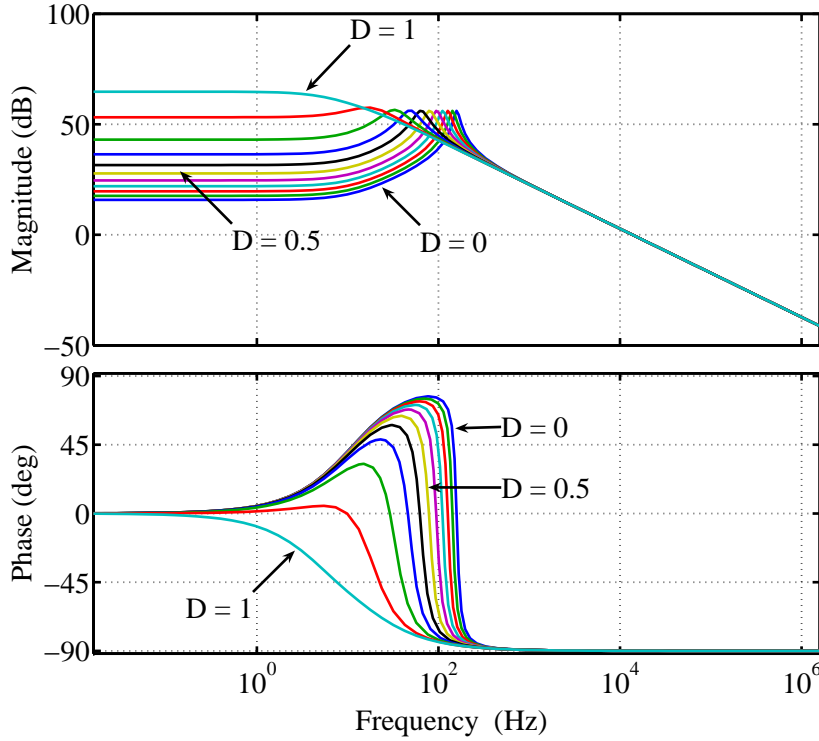
Parameter	Symbol	Equation	Value	Units
Cell Power Rating	$P_{cell}$	$P_{ph} \div N =$	1.33	kW
Peak Cell Input-Voltage	$V_{ac}$	$V_{php} \div N =$	359.26	Vp
Input-Inductance	$L$		5	mH
Inductor Resistance	$R_L$		0.5	$\Omega$
AR Boost Ratio	$Boost$		1.2	Units
Cell Bus-Voltage	$V_{cb}$	$V_{ac} \times Boost =$	431.11	V
Load Resistance	$R_O$	$V_{cb}^2 \div P_{cell} =$	139.39	$\Omega$
Cell Bus-Capacitance	$C_{cb}$		200	$\mu\text{F}$

**Table B.4:** Cell Parameters

The only variable left to quantify is the AR duty cycle,  $D$ . This value changes during normal AR operation, ranging between 0 and 1. This means that the current-loop plant model varies during normal AR operation. Figure B.3 depicts the frequency response of this plant for varied values of  $D$  from 0 to 1, in incremental steps of 0.1.

It is clear that the low-frequency gain as well as the phase transition of the model varies with different values of  $D$ . The effect of an ever changing  $D$  within the current-loop plant model is kept in mind throughout the control design. However, a fixed value for  $D$  is calculated to quantify the plant model. Combining Eq. B.1.27 and the definition of  $Boost$ , in Table B.4, results in:





**Figure B.3:** Frequency Response of the Current-Loop Plant Model,  $G_I(s)$ , with  $D =$  zero to one

$$\frac{V_{cb}}{V_{ac}} = \sqrt{2} \times Boost = \frac{1}{1-D} \quad (\text{B.1.31})$$

with a  $V_{ac}$  RMS value. Rearranging terms yields:

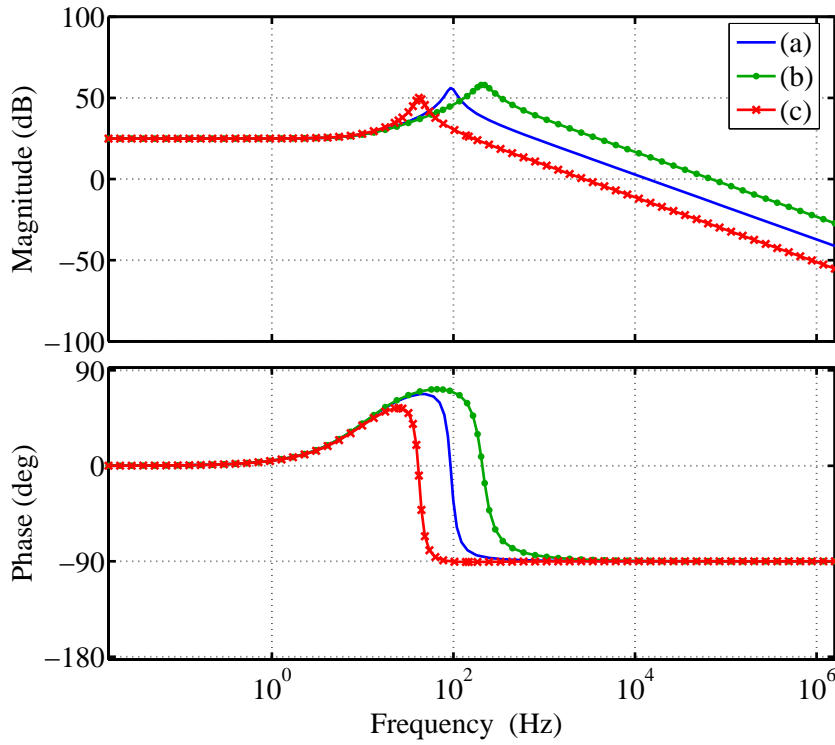
$$D = 1 - \frac{1}{\sqrt{2} \times Boost} = 0.4107 \quad (\text{B.1.32})$$

Substitution of  $D$  and the parameters listed in Table B.4 into Eq. B.1.30 yields the quantified plant transfer function:

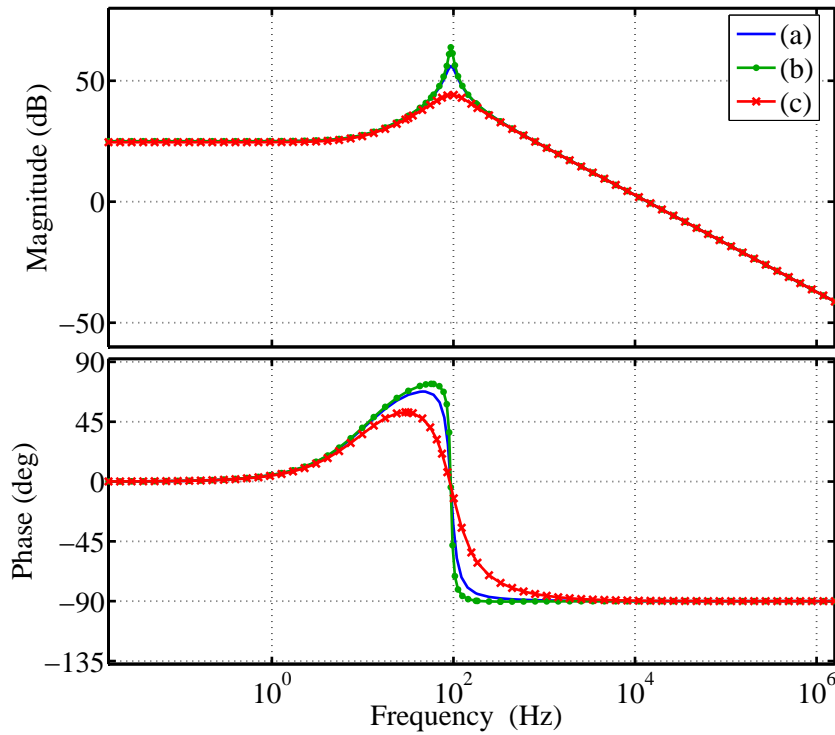
$$G_I(s) = 8.622 \times 10^4 \times \frac{s + 71.747}{s^2 + 135.9s + 3.508 \times 10^5} \quad (\text{B.1.33})$$

### B.1.6 Plant Model Analysis

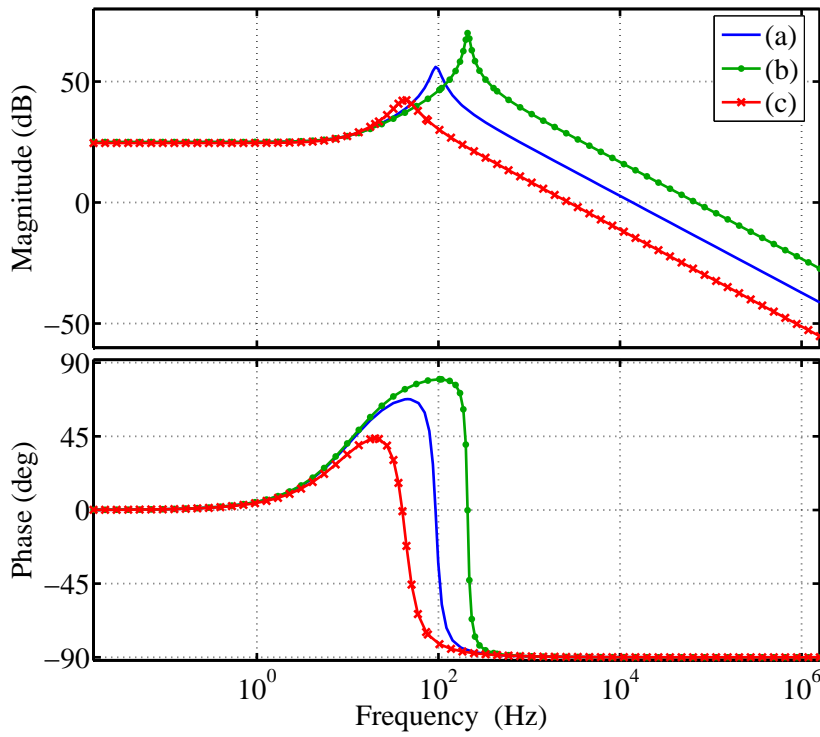
The linear model transfer function is analysed by varying specific system parameters to determine the model sensitivity to such physical changes. The parameters present in the model, that might be changed in practical tests and implementations, are varied in such a manner that an increase and decrease is evaluated. The input-inductor value,  $L$ , is varied in Figure B.4, which alters the resonant frequency and significantly alters the model gain beyond this frequency. The inductor resistance,  $R_L$ , is varied in Figure B.5, which only alters the sharpness of the resonant gain spike and the phase drop. Both the inductor value,  $L$ , and the inductor resistance,  $R_L$ , are varied in Figure B.6, which combines the results of the previous two changes. The cell bus-voltage,  $V_{cb}$ , is varied in Figure B.7, which alters the model gain across the entire frequency spectrum.



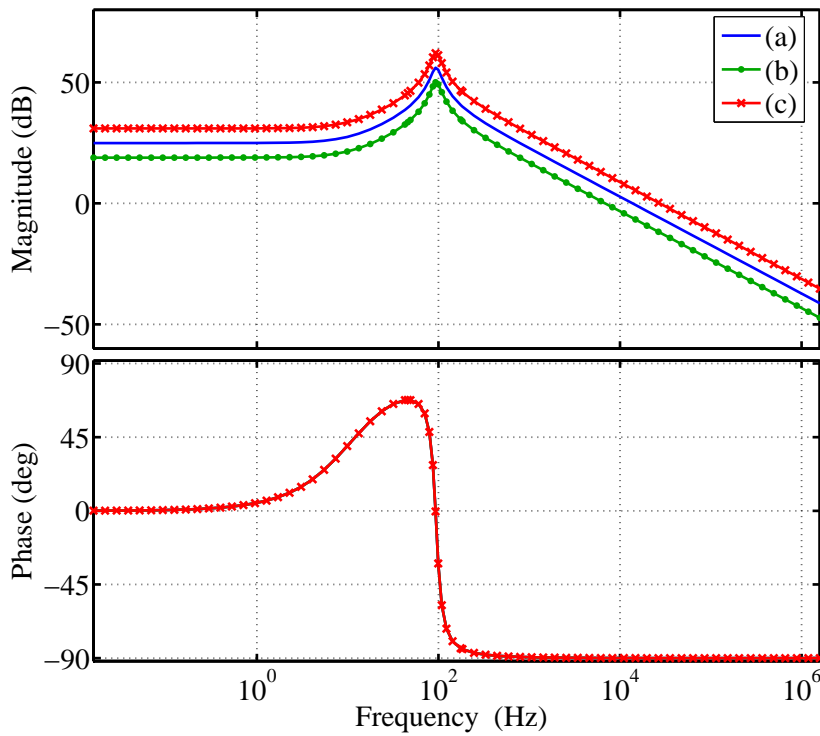
**Figure B.4:** Frequency Response of  $G_I(s)$ : (a)  $L = 5$  mH; (b)  $L = 1$  mH; (c)  $L = 25$  mH



**Figure B.5:** Frequency Response of  $G_I(s)$ : (a)  $R_L = 0.5 \Omega$ ; (b)  $R_L = 0.1 \Omega$ ; (c)  $R_L = 2.5 \Omega$



**Figure B.6:** Frequency Response of  $G_I(s)$ : (a)  $L = 5 \text{ mH}$   $R_L = 0.5 \Omega$ ; (b)  $L = 1 \text{ mH}$   $R_L = 0.1 \Omega$ ; (c)  $L = 25 \text{ mH}$   $R_L = 2.5 \Omega$



**Figure B.7:** Frequency Response of  $G_I(s)$ : (a)  $V_{cb} = 431$ ; (b)  $V_{cb} = 431 \times 0.5 = 215$ ; (c)  $V_{cb} = 431 \times 2 = 862$

## B.2 Current-Loop Compensator Design details

### B.2.1 Optimal Gain design

The inductor-current downslope is analysed because this is the slope parallel to the carrier slope due to the negative feedback of the current loop. The downslope occurs during state 2, as depicted in Figure B.2, which results in:

$$\frac{di_L}{dt} = \frac{V_{cb} - V_{ac}}{L} \quad (\text{B.2.1})$$

with the worst case of  $V_{ac} = 0$ :

$$\frac{di_L}{dt} = \frac{V_{cb}}{L} \quad (\text{B.2.2})$$

The carrier slope is defined as:

$$\frac{dCarrier}{dt} = \frac{V_s}{T_s} = V_s \cdot f_s \quad (\text{B.2.3})$$

Implementing the compensator gain:

$$\frac{di_L}{dt} \cdot G_{CI} = \frac{dCarrier}{dt} \quad (\text{B.2.4})$$

and therefor applying the steady state values from Appendix B.1.5 yields:

$$G_{CI} = \frac{V_s \cdot f_s \cdot L}{V_{cb}} = \frac{2 \cdot 10^4 \cdot 5 \times 10^{-3}}{431.11} = 0.232 \quad (\text{B.2.5})$$

which results in a compensator gain of -12.69 dB at the switching frequency,  $f_{ar}$ .

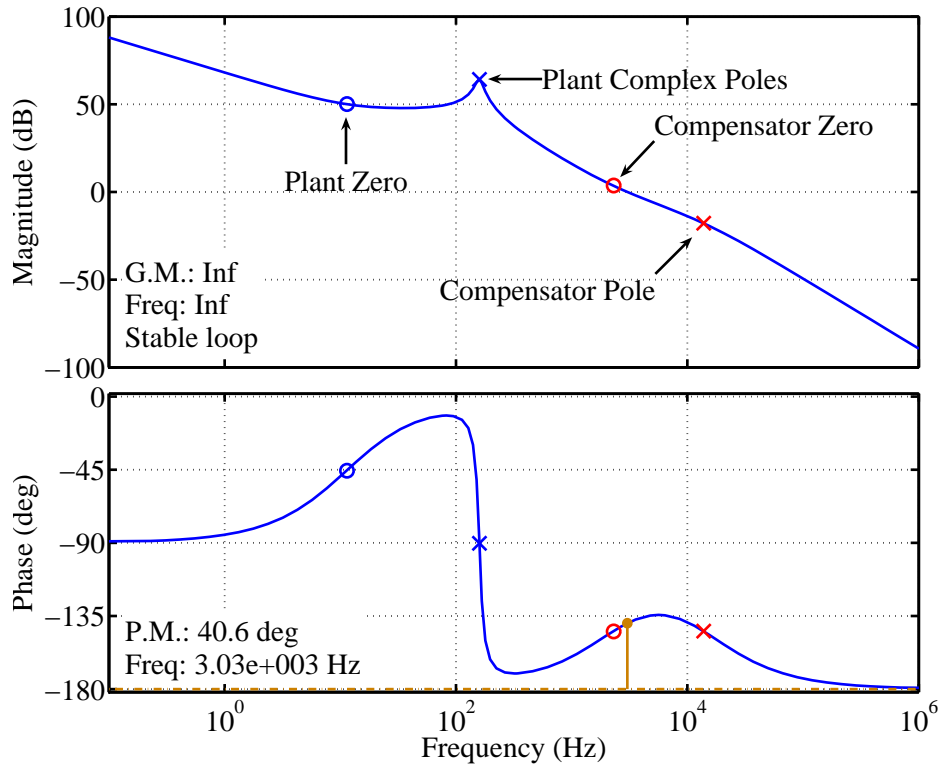
### B.2.2 Current-Loop Analysis

The open current-loop detailed frequency responses with  $D = 0$ ,  $D = 0.4107$  and  $D = 1$  are shown in Figure B.8, B.9 and B.10 respectively. These figures indicate the positions of the poles and zeros of both the plant and compensator. All three open-loops have an infinite gain margin and stable phase margins of 40.6°/40.5°.

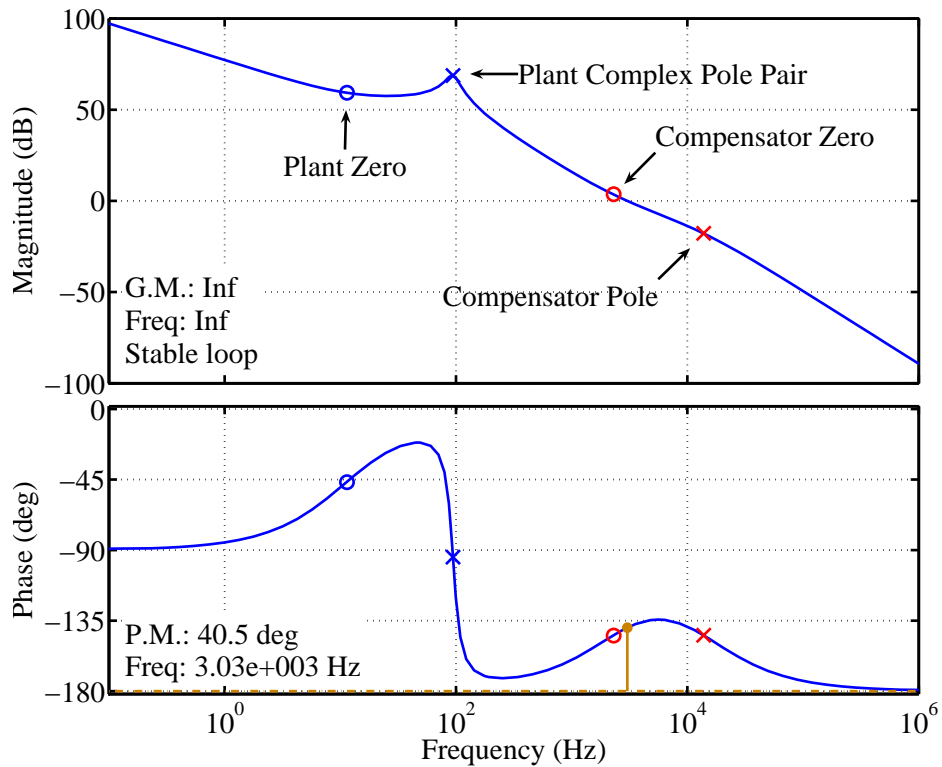
Figure B.11 depicts the unit-step transient response of the current-loop. The transient response characteristics of the underdamped system are listed below:

$$\begin{aligned} \text{Rise time, } t_r &= 78.05 \mu\text{s } 0\text{-}100\% \\ \text{Peak time, } t_p &= 153 \mu\text{s} \\ \text{Peak overshoot, } M_p &= 1.386 \\ \text{Settling time, } t_s \text{ } 2\% &= 472.5 \mu\text{s} \end{aligned}$$

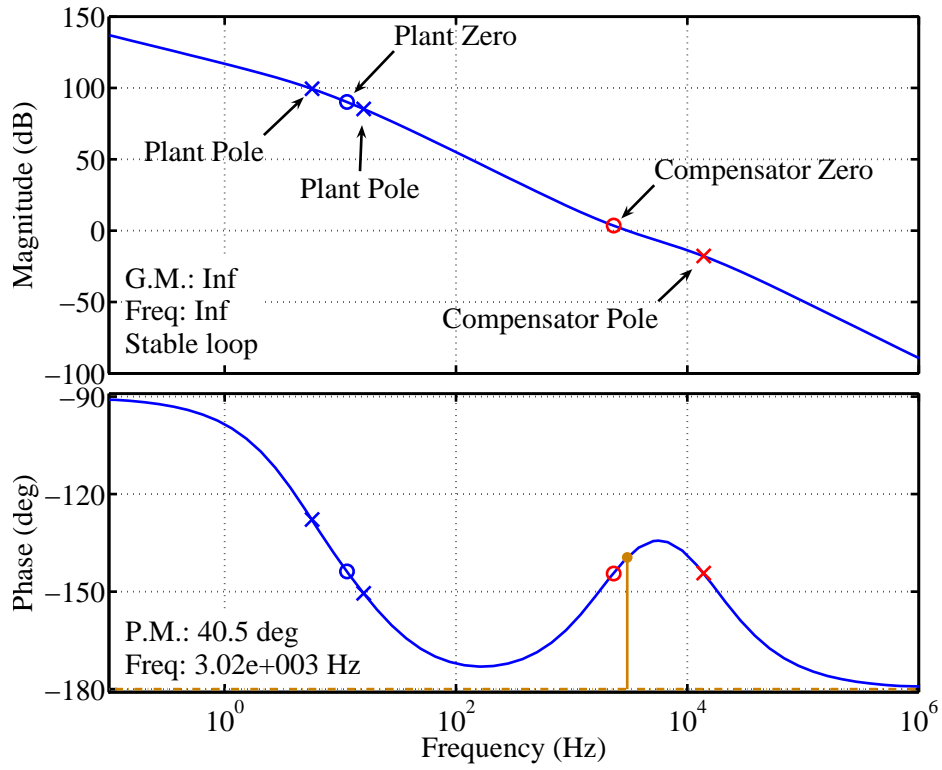
Figure B.12 depicts the impulse response of the current-loop.



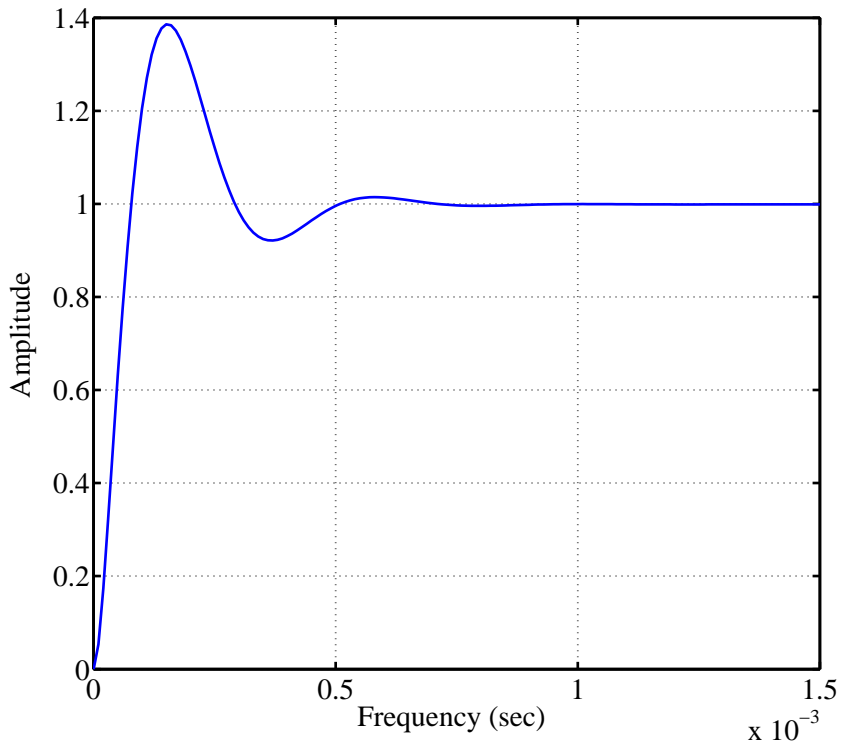
**Figure B.8:** Detailed Frequency Response of  $C_I(s) \cdot G_I(s)$  with  $D = 0$



**Figure B.9:** Detailed Frequency Response of  $C_I(s) \cdot G_I(s)$  with  $D = 0.4107$



**Figure B.10:** Detailed Frequency Response of  $C_I(s) \cdot G_I(s)$  with  $D = 1$



**Figure B.11:** Current-Loop Step Response

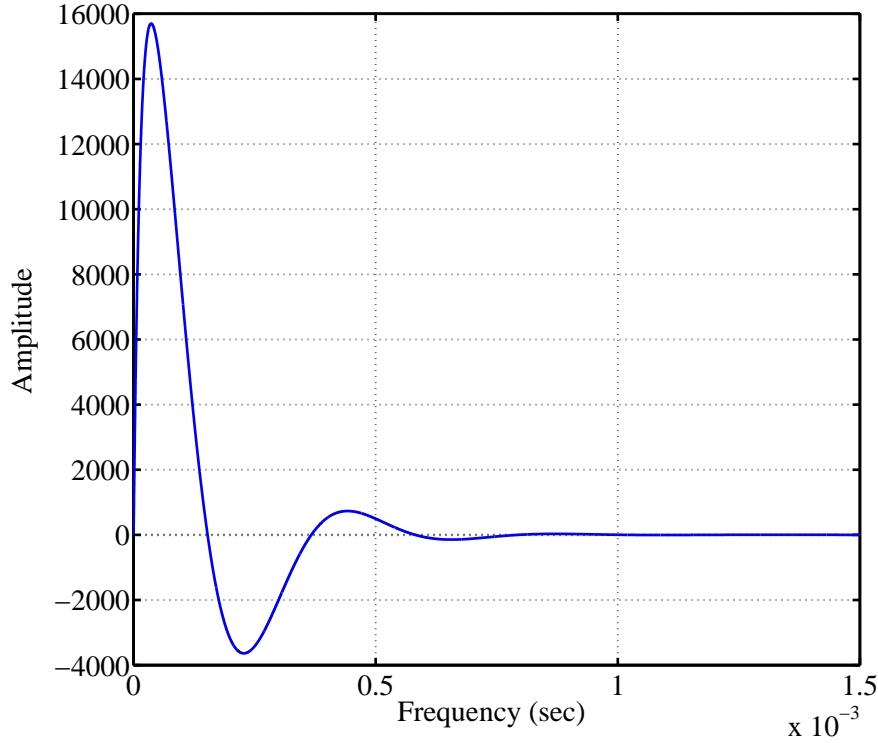


Figure B.12: Current-Loop Impulse Response

### B.3 Voltage-Loop Plant Linearisation details

The voltage-loop plant linearisation process involves the use of parameter values averaged over a relatively long period. This method can be used due to the desired low voltage-loop bandwidth.

#### B.3.1 Step 1: Determine the Switching-Stage Transfer Function

To determine the transfer function of the switching stage, as depicted in Figure B.13, we assume a lossless circuit yielding:

$$P_{in} = P_{out} \quad (\text{B.3.1})$$

and therefor

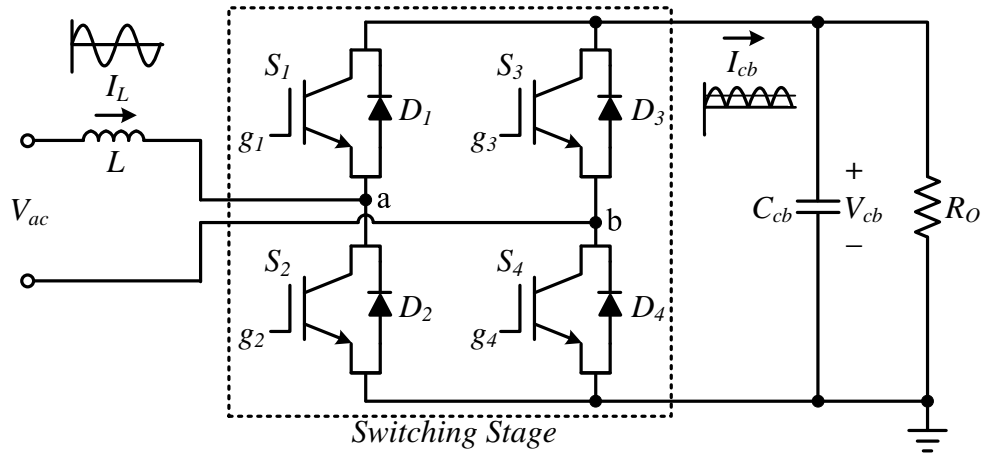
$$V_{ac} I_L = V_{cb} I_{cb} \quad (\text{B.3.2})$$

with  $V_{ac}$  and  $I_L$  as RMS values and  $V_{cb}$  and  $I_{cb}$  as average values. Rearranging terms and incorporating the peak inductor-current,  $I_{Lp}$ , results in:

$$\frac{I_{cb}}{I_{Lp}} = \frac{V_{ac}}{\sqrt{2} V_{cb}} \quad (\text{B.3.3})$$

From Eq. B.1.27:

$$V_{ac} = V_{cb} (1 - D) \quad (\text{B.3.4})$$



**Figure B.13:** Active-Rectifier Circuit Diagram Indicating Currents

and finally combining Eq. B.3.3 and B.3.4 yields:

$$\frac{I_{cb}}{I_{Lp}} = \frac{1-D}{\sqrt{2}} \tag{B.3.5}$$

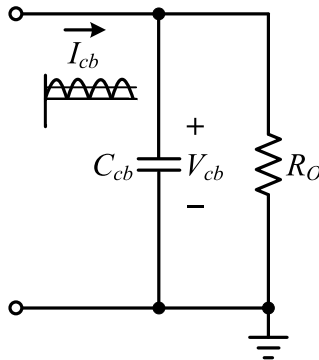
From Table B.4 and Eq. B.1.32, this gain value can be calculated as:

$$\frac{I_{cb}}{I_{Lp}} = \frac{1-0.4107}{\sqrt{2}} = 0.417 \tag{B.3.6}$$

### B.3.2 Step 2: Determine the Bus-Stage Transfer Function

Straightforward circuit analysis of the bus-stage, as shown in Figure B.14, yields the transfer function:

$$G_{BUS}(s) = \frac{v_{cb}}{i_{cb}} = \frac{\frac{1}{C_{cb}}}{s + \frac{1}{C_{cb}R_O}} \tag{B.3.7}$$



**Figure B.14:** Active-Rectifier Bus-Stage Circuit Diagram

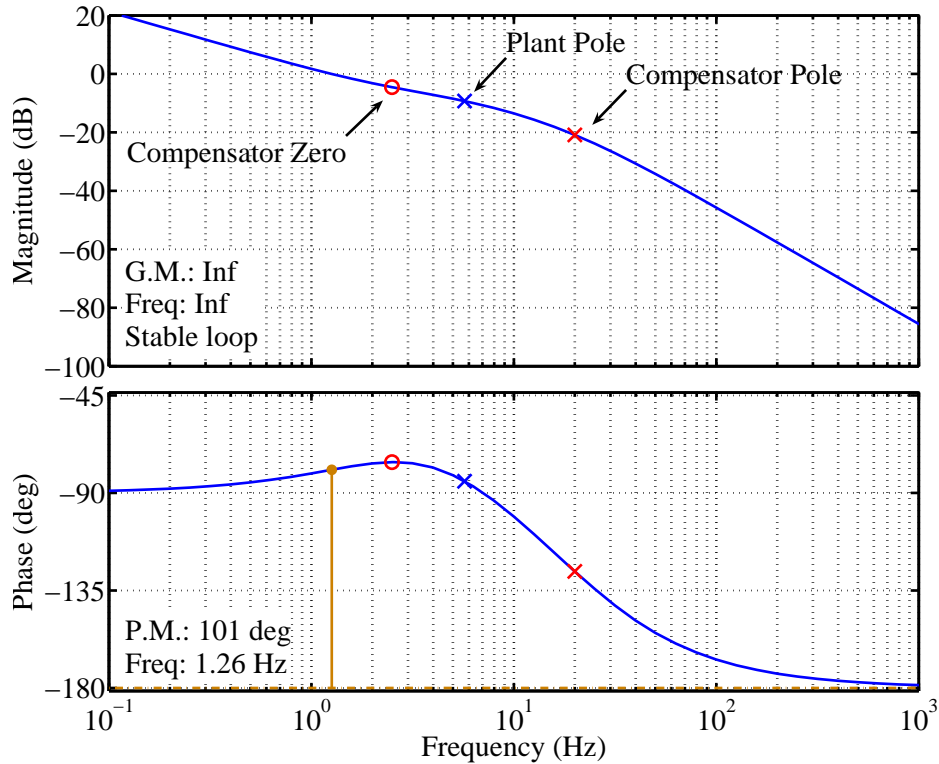
From Table B.4, this transfer function can be quantified as:

$$G_{BUS}(s) = \frac{5000}{s + 35.87} \tag{B.3.8}$$



### B.3.3 Voltage-Loop Analysis

The open voltage-loop is analysed with the detailed frequency response, depicted in Figure B.15. This figure indicates the poles and zeros of the plant,  $G_V(s)$ , and compensator,  $C_V(s)$ , respectively. This open-loop has an infinite gain margin and a very stable phase margin of  $101^\circ$ .

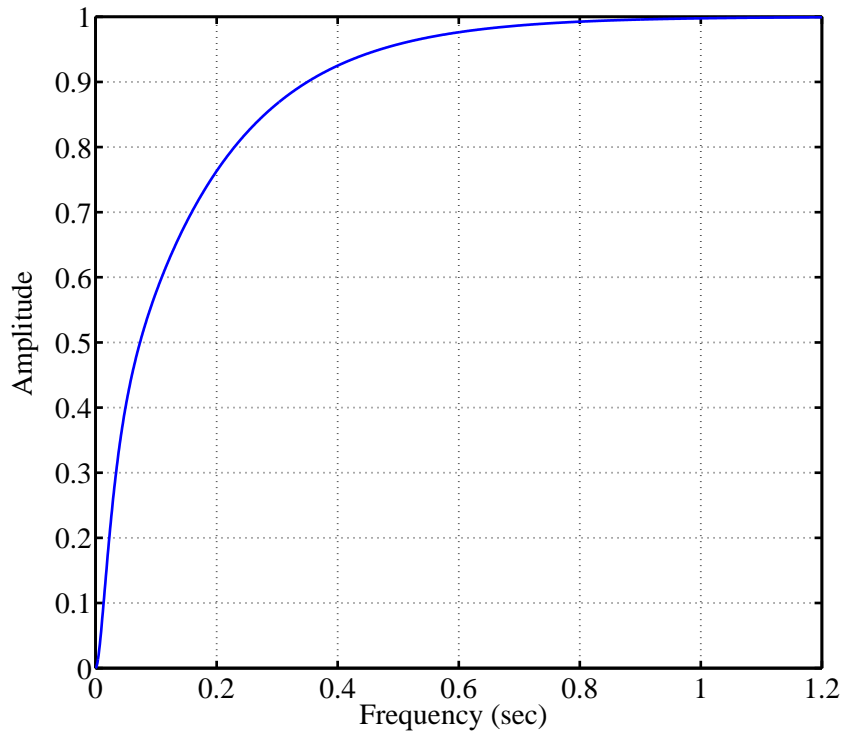
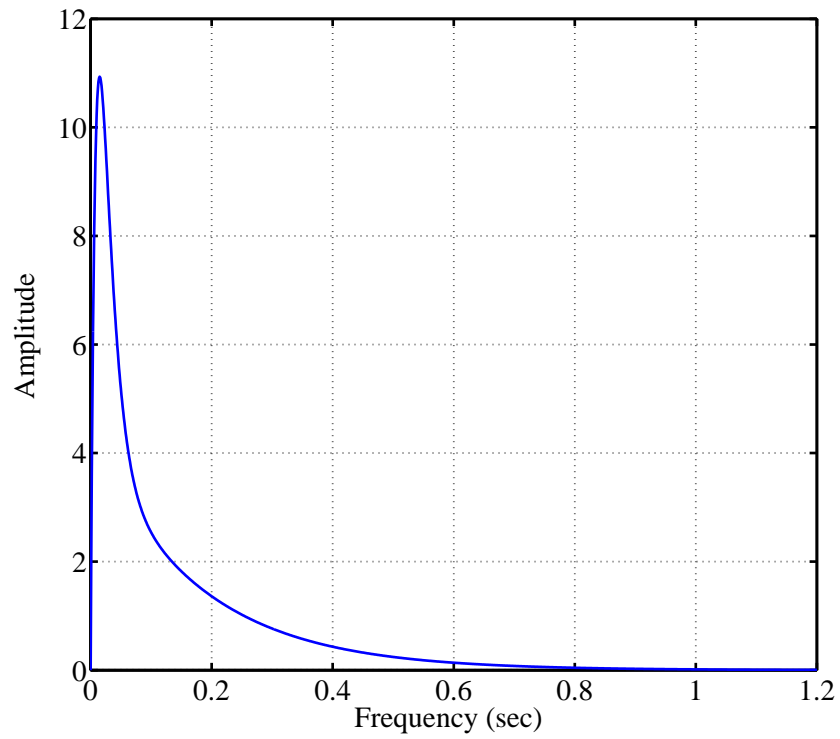


**Figure B.15:** Detailed Frequency Response of  $C_V(s) \cdot G_V(s)$

Figure B.16 depicts the transient response of the voltage-loop with a unity step input. The transient response characteristics of this overdamped system are listed below:

$$\begin{aligned} \text{Rise time, } t_r &= 350 \text{ ms } 0\text{-}90\% \\ \text{Settling time, } t_s \text{ } 2\% &= 630 \text{ ms} \end{aligned}$$

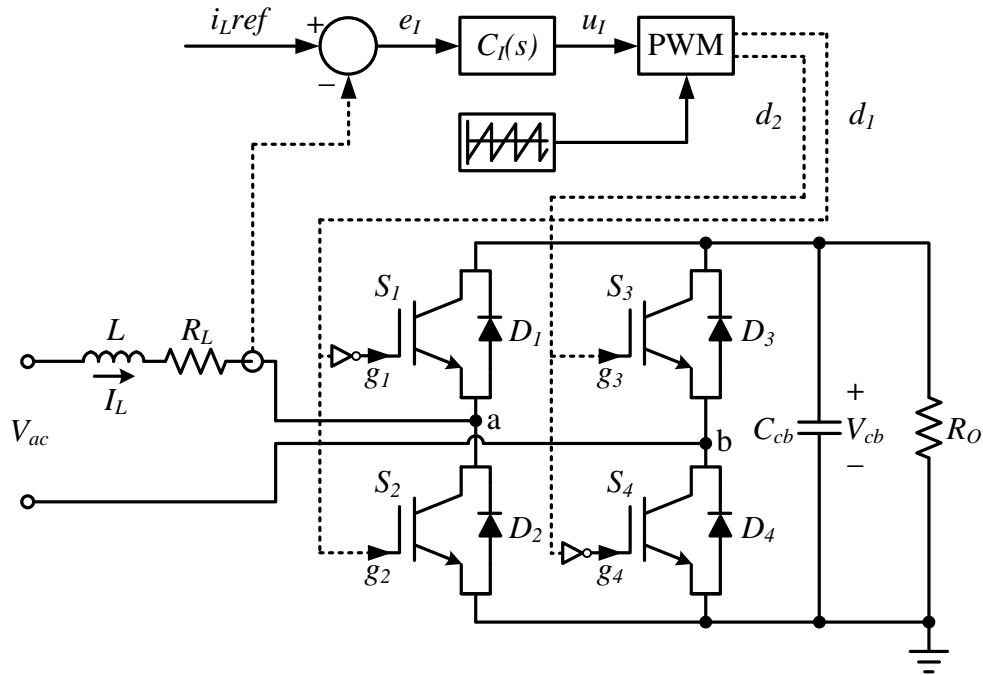
Figure B.17 depicts the impulse response of the voltage-loop.

**Figure B.16:** Voltage-Loop Step Response**Figure B.17:** Voltage-Loop Impulse Response

## B.4 Simulation Details

### B.4.1 Current-Loop Simulation Setup

The simulation setup, as depicted in Figure B.18, is aimed at verifying circuit and control integration as well as current-loop functionality in terms of its reference tracking ability.



**Figure B.18:** Current-Loop Simulation setup

The simulation-setup details are listed below:

- The electrical component values are:

$$V_{ac} = 166.7 \sin(2\pi f_{in} t) \text{ V}$$

$$L = 5.8 \text{ mH}$$

$$R_L = 0.5 + 6 \ \Omega$$

$$C_{cb} = 200 \ \mu\text{F}$$

$$R_O = 110 \ \Omega$$

The inductor resistance,  $R_L$ , represents two lumped resistor values. One is the actual inductor resistance and the second is an input resistor of  $6 \ \Omega$ . The input resistor is added for protection in the measurement test setup, to absorb power if an error occurs causing high current flow.

- The IGBT and Diode are system level models found in the Simplorer8 library, LIBRARY: Simplorer Elements\Basic Elements\Circuit\Semiconductor System Level. The component settings are as follows:

Type = Equivalent Line

Forward Voltage = 0.8 V

Bulk Resistance = 1 m $\Omega$

Reverse Resistance = 10 k $\Omega$

- The current-loop reference is a sinusoid, in phase with  $V_{ac}$ :

$$i_{Lref}(t) = 5 \sin(2\pi f_{in} t) \quad (\text{B.4.1})$$

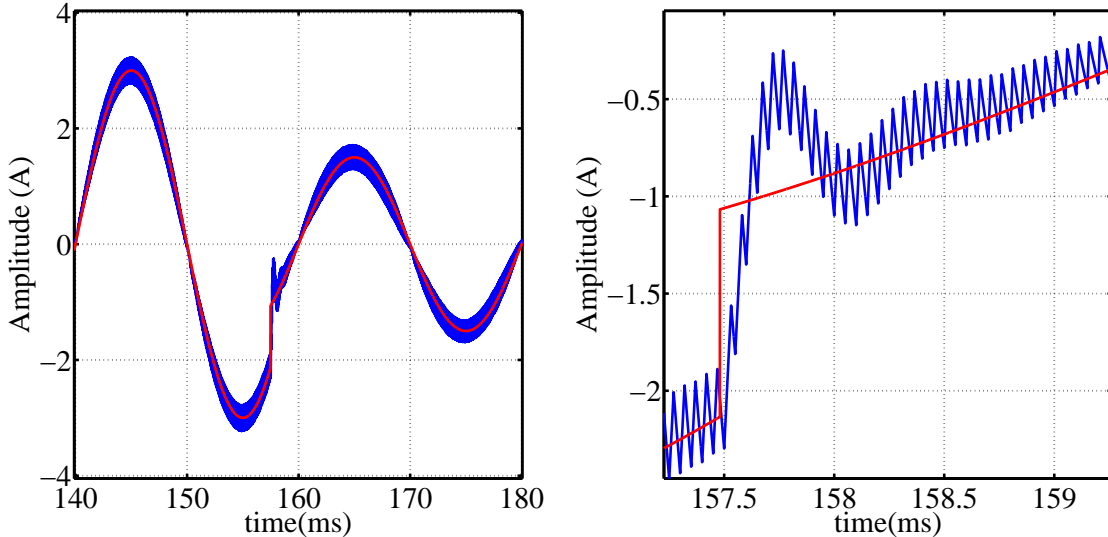
- The compensator,  $C_I(s)$ , is modeled as the transfer function of Eq. 4.2.35.
- The PWM component of the current-loop implements unipolar-voltage switching with two sawtooth carriers, as explained in Section 4.2.1. Gating signal,  $d_1$ , is dependent on the compensator output,  $u_I$ , and Carrier1. Gating signal,  $d_2$ , is dependent on  $u_I$  and Carrier2. Switches  $S_2$  and  $S_3$  are gated on the signals  $d_1$  and  $d_2$  respectively. Switches  $S_1$  and  $S_4$  are gated on the inverse of signals  $d_1$  and  $d_2$  respectively.

### B.4.2 Current-Loop Reference-Step Simulation Analysis

Three simulations are presented aimed at verifying acceptable current-loop operation during reference steps. The input voltage, for all three simulation, is set as:

$$V_{ac} = 130 \sin(2\pi f_{in} t) \text{ V} \quad (\text{B.4.2})$$

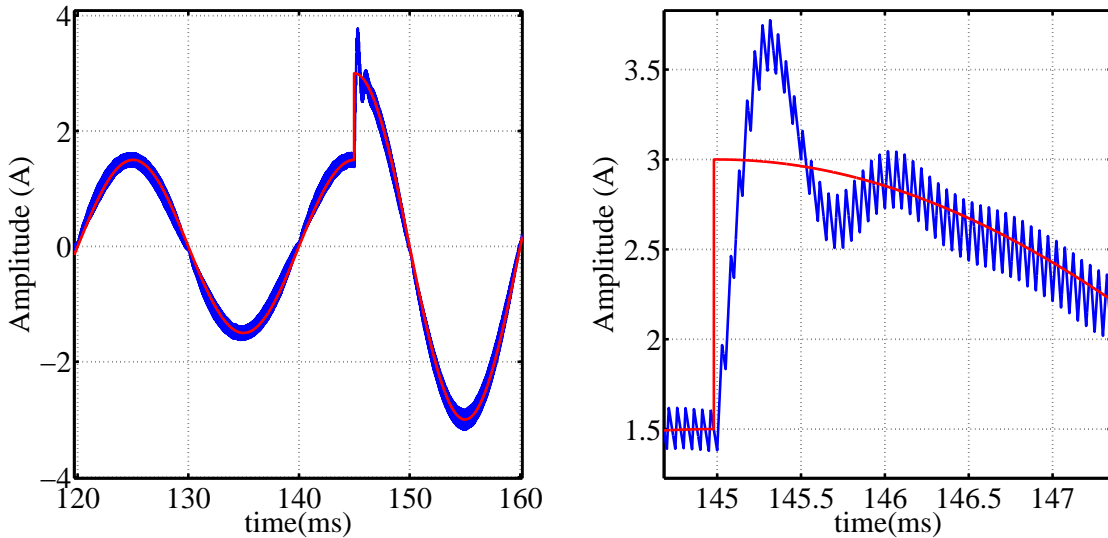
The first simulation introduces a reference step, at  $t = 157.5$  ms, of  $i_{Lref} = 3$  Ap to  $i_{Lref} = 1.5$  Ap. This reduces the input power by 50% at an arbitrary position of the sinusoidal current. Figure B.19 depicts  $i_L$  and the  $i_{Lref}$  step-down on the left and a detailed result on the right. It is shown that  $i_L$  successfully tracks  $i_{Lref}$  within  $\pm 15$  switching cycles, with a  $\pm 40\%$  overshoot. This result corresponds with the underdamped system described in Appendix B.2.2.



**Figure B.19:** Inductor Current and Current-Loop Reference

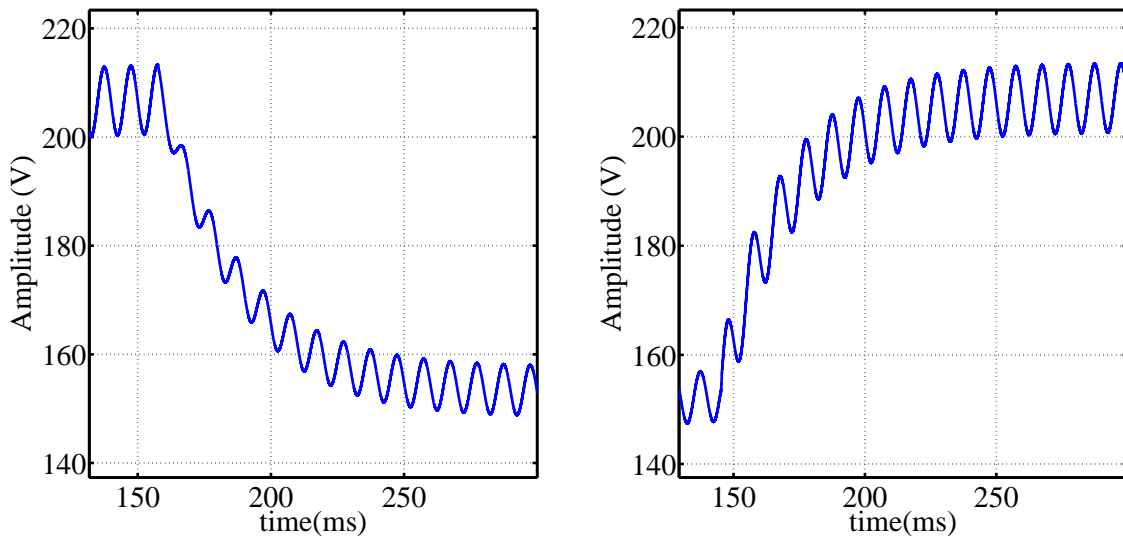
The second simulation introduces a reference step, at  $t = 145$  ms, of  $i_{Lref} = 1.5$  Ap to  $i_{Lref} = 3$  Ap. This increases the input power by 100% at the peak of the sinusoidal current. Figure B.20 depicts  $i_L$  and the  $i_{Lref}$  step-up on the left and a detailed result on the right. It is shown that  $i_L$  successfully tracks  $i_{Lref}$  within  $\pm 19$  switching cycles, with a  $\pm 40\%$  overshoot. This result also corresponds with the underdamped system described in Appendix B.2.2.

Figure B.21 depicts the  $v_{cb}$  transient response of the first simulation on the left and the transient response of the second simulation on the right. The  $v_{cb}$  value merely increases when



**Figure B.20:** Inductor Current and Current-Loop Reference

the input power is increased and decreases when the input power is decreased, maintaining its 100 Hz ripple throughout. Each transient endures for  $\pm 12$  ripple cycles.



**Figure B.21:** Cell Bus-Voltage

The final simulation introduces a reference step-up, at  $t = 160$  ms, of  $i_{Lref} = 1.5$  A to  $i_{Lref} = 3$  A, and a reference step-down, at  $t = 240$  ms, of  $i_{Lref} = 3$  A to  $i_{Lref} = 1.5$  A. The power is thus increased or decreased at zero crossings of the sinusoidal current. Figure B.22 depicts  $i_L$  and the  $i_{Lref}$  step-up on the left, and step-down on the right. It is shown that  $i_L$  seamlessly tracks  $i_{Lref}$  in both cases.

The simulation results presented in this appendix verify acceptable current-loop operation during reference steps. The fast tracking ability of the current-loop, due to its high bandwidth, is also verified. The observed overshoots are expected given the step response of the closed current-loop, discussed in Appendix B.2.2.

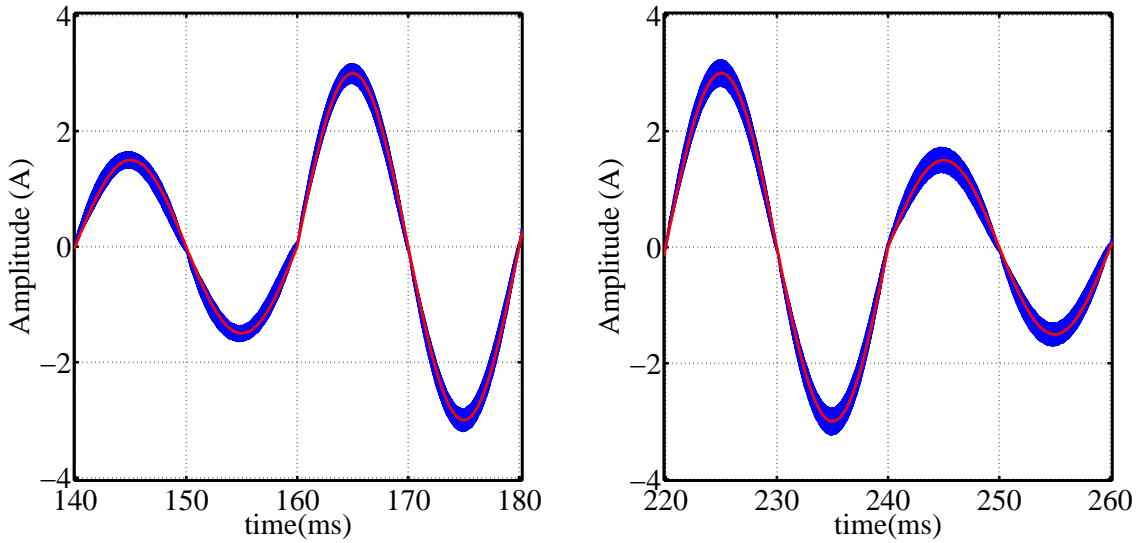


Figure B.22: Inductor Current and Current-Loop Reference

### B.4.3 Active-Rectifier Simulation Setup

The simulation setup, as depicted in Figure B.23, is aimed at verifying current- and voltage-loop integration as well as voltage-loop functionality in terms of its reference tracking ability.

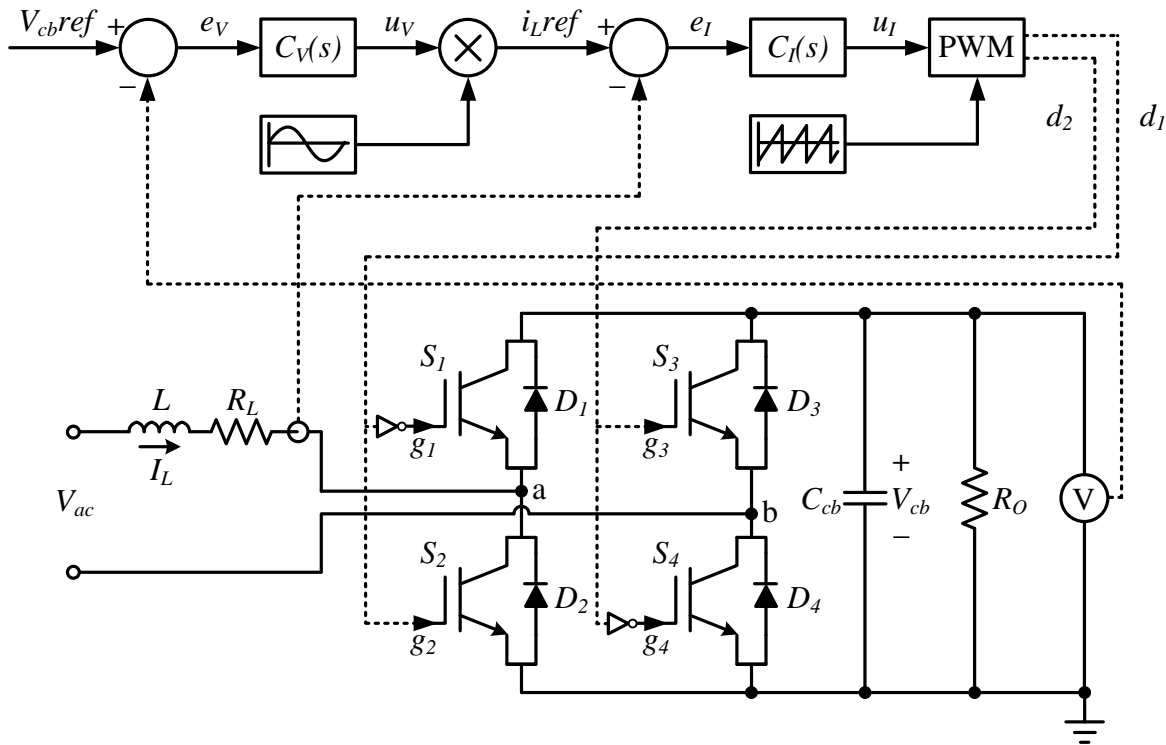


Figure B.23: Active-Rectifier Simulation Setup

The simulation-setup details are listed below:

- The electrical component values are:

$$\begin{aligned} V_{ac} &= 125 \sin(2\pi f_{in} t) \text{ V} \\ L &= 5.8 \text{ mH} \\ R_L &= 0.5 + 6 \Omega \\ C_{cb} &= 200 \mu\text{F} \\ R_O &= 267 \Omega \end{aligned}$$

The inductor resistance,  $R_L$ , represents two lumped resistor values. One is the actual inductor resistance and the second is an input resistor of  $6 \Omega$ . The input resistor is added for protection in the measurement test setup, to absorb power if an error occurs causing high current flow.

- The IGBT and Diode are system level models found in the Simplorer8 library, LIBRARY: Simplorer Elements\Basic Elements\Circuit\Semiconductor System Level. The component settings are as follows:

$$\begin{aligned} \text{Type} &= \text{Equivalent Line} \\ \text{Forward Voltage} &= 0.8 \text{ V} \\ \text{Bulk Resistance} &= 1 \text{ m}\Omega \\ \text{Reverse Resistance} &= 10 \text{ k}\Omega \end{aligned}$$

- The voltage-loop reference is a constant value set to the desired average bus-voltage:

$$V_{cbref} = 150 \text{ V} \quad (\text{B.4.3})$$

- The compensator,  $C_V(s)$ , is modeled as the transfer function of Eq. 4.2.42.
- The output of the voltage compensator,  $u_v$ , is multiplied with a unit sinusoid, in phase with  $V_{ac}$ , to generate the current-loop reference:

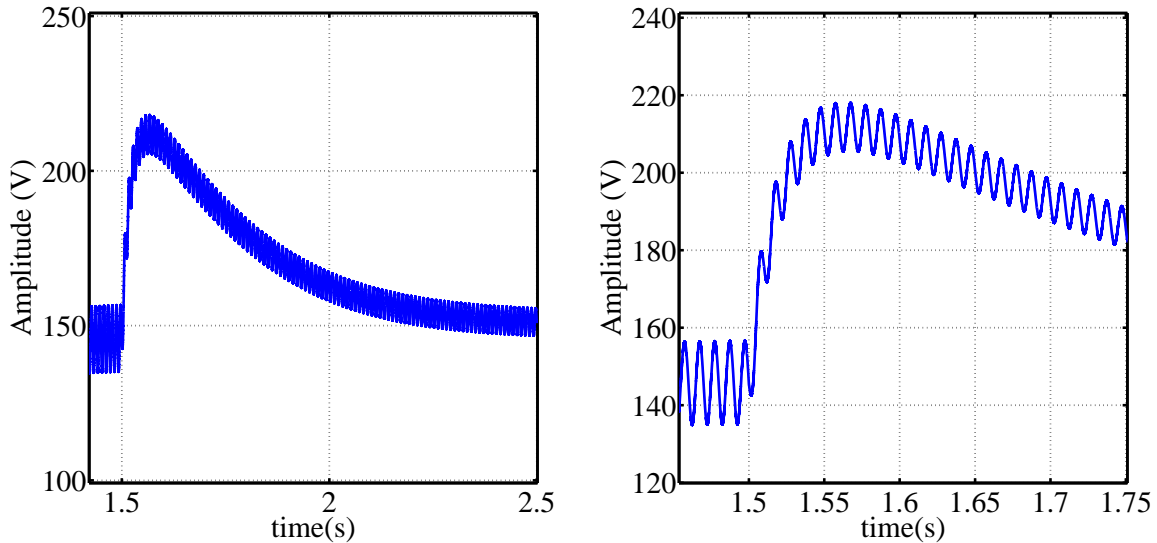
$$i_{Lref}(t) = u_v(t) \cdot \sin(2\pi f_{in} t) \quad (\text{B.4.4})$$

- The compensator,  $C_I(s)$ , is modeled as the transfer function of Equation 4.2.35.
- The PWM component of the current-loop implements unipolar-voltage switching with two sawtooth carriers, as explained in Section 4.2.1. Gating signal,  $d_1$ , is dependent on the compensator output,  $u_I$ , and Carrier1. Gating signal,  $d_2$ , is dependent on  $u_I$  and Carrier2. Switches  $S_2$  and  $S_3$  are gated on the signals  $d_1$  and  $d_2$  respectively. Switches  $S_1$  and  $S_4$  are gated on the inverse of signals  $d_1$  and  $d_2$  respectively.

#### B.4.4 Load-Step Simulation Analysis

Two simulations are presented, aimed at verifying acceptable AR operation during load steps. The first simulation introduces a load step, at  $t = 1.5$  s, of  $R_O = 110 \Omega$  to  $R_O = 267 \Omega$ . This reduces the power delivered to the load by 59 %.

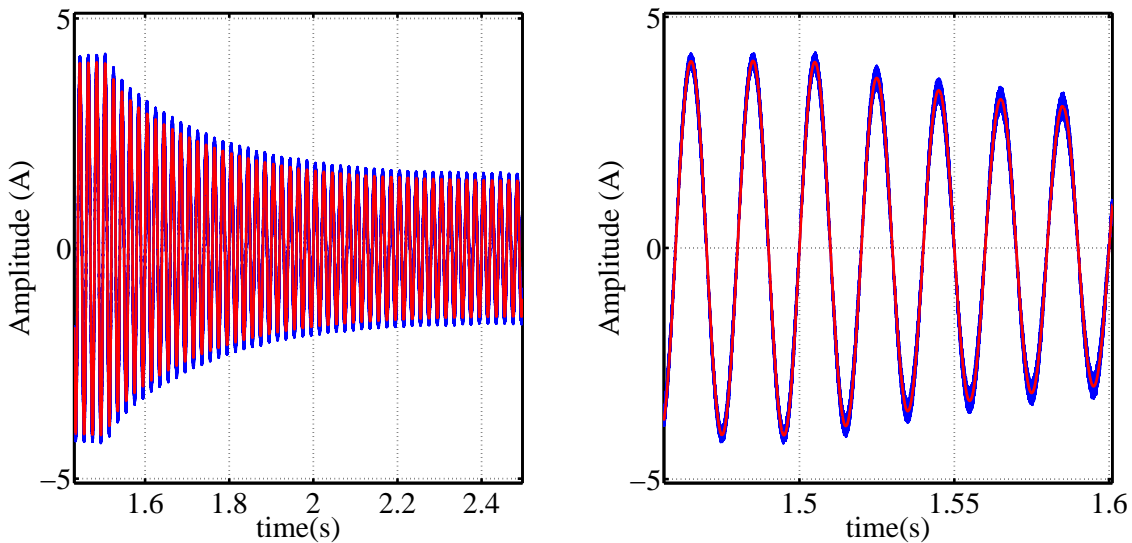
Figure B.24 depicts the  $v_{cb}$  transient response on the left and its detailed result on the right. While the energy transferred from  $C_{cb}$  to  $R_O$  is reduced almost instantly, the energy transferred from  $L$  to  $C_{cb}$  has a relatively slow transient, caused by the low voltage-loop bandwidth. Examining  $C_{cb}$ , the energy input is larger than the energy output which causes  $v_{cb}$  to rise, and then



**Figure B.24:** Cell Bus-Voltage

fall again as the energy input is decreased. The detailed transient shows that the 100 Hz ripple is maintained throughout.

Figure B.25 depicts the transient response of  $i_L$  and  $i_{Lref}$  on the left and their detailed result on the right. Both  $i_{Lref}$  and  $i_L$ , tracking it, have a relatively slow transient caused by the low voltage-loop bandwidth. This current transient is a representation of the energy transient, transferred from  $L$  to  $C_{cb}$ . Also referred to as the  $C_{cb}$  energy input. The detailed result shows that  $i_L$  adequately tracks  $i_{Lref}$  throughout.



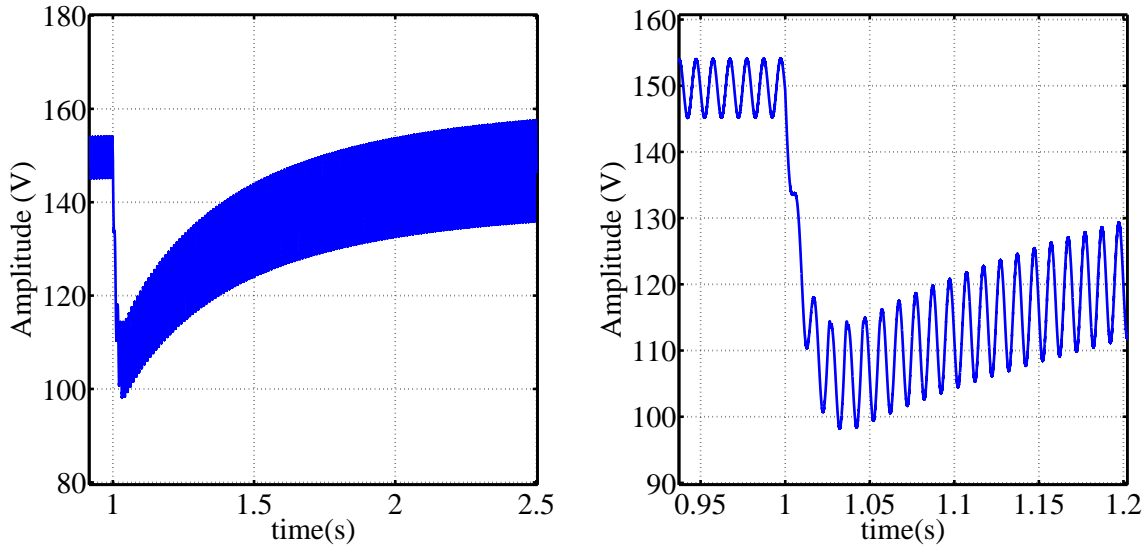
**Figure B.25:** Inductor Current and Current-Loop Reference

The second simulation introduces a load step, at  $t = 1$  s, of  $R_O = 267 \Omega$  to  $R_O = 110 \Omega$ . This increases the power delivered to the load by 140 %.

Figure B.26 depicts the  $v_{cb}$  transient response on the left and its detailed result on the right. While the energy transferred from  $C_{cb}$  to  $R_O$  increases almost instantly, the energy transferred from  $L$  to  $C_{cb}$  has a relatively slow transient, caused by the low voltage-loop bandwidth. Examining  $C_{cb}$ , the energy output is larger than the energy input which causes  $v_{cb}$  to drop, and

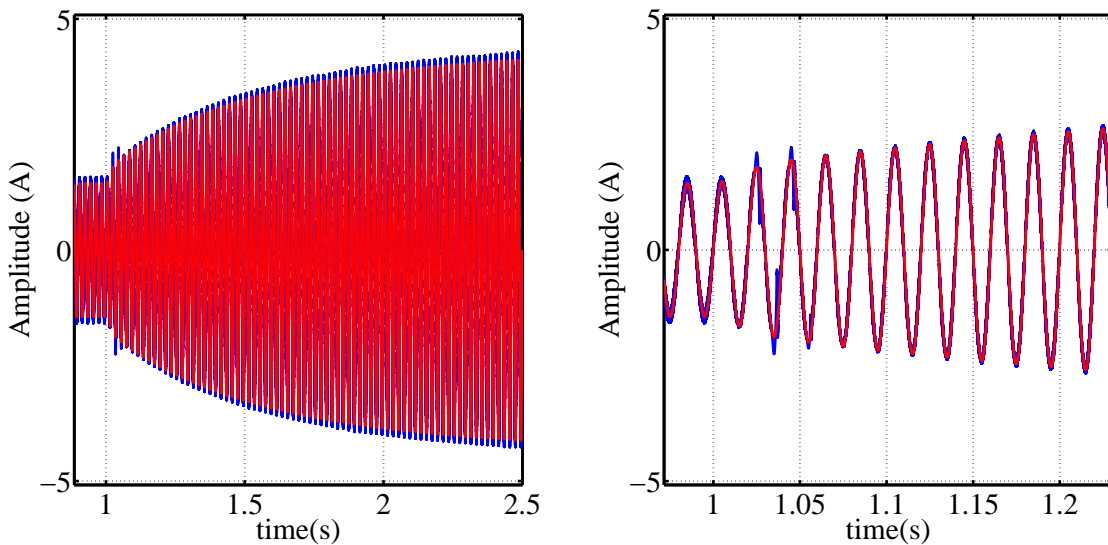


then rise again as the energy input is increased. The detailed result shows that the 100 Hz ripple is maintained with 4 slightly deformed peaks, analysed in the inductor-current discussion to follow and better illustrated in Figure B.28.

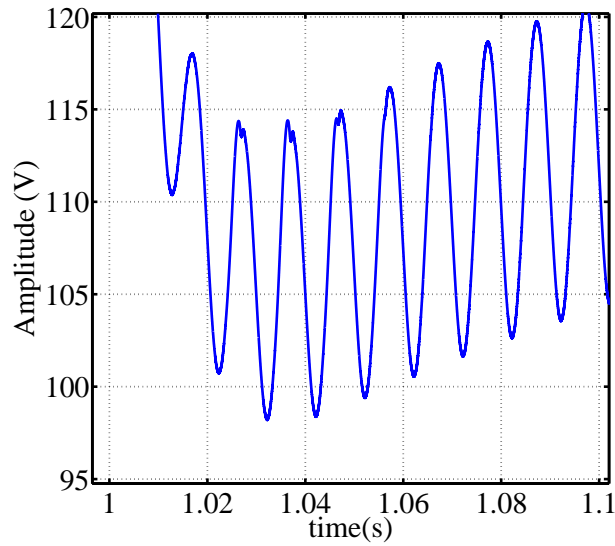


**Figure B.26:** Cell Bus-Voltage

Figure B.27 depicts the transient response of  $i_L$  and  $i_{Lref}$  on the left and their detailed result on the right. Both  $i_{Lref}$  and  $i_L$ , tracking it, have a relatively slow transient caused by the low voltage-loop bandwidth. This current transient is a representation of the energy transient, transferred from  $L$  to  $C_{cb}$ . Also referred to as the  $C_{cb}$  energy input. The detailed result shows that  $i_L$  adequately tracks  $i_{Lref}$ , however  $i_L$  has some peaks where the current-loop fails to track  $i_{Lref}$ . This is due to  $v_{cb}$  dropping below  $v_{ac}$  which causes the AR to act as a full-bridge passive rectifier. These current peaks cause the slightly deformed voltage peaks depicted in Figure B.28.

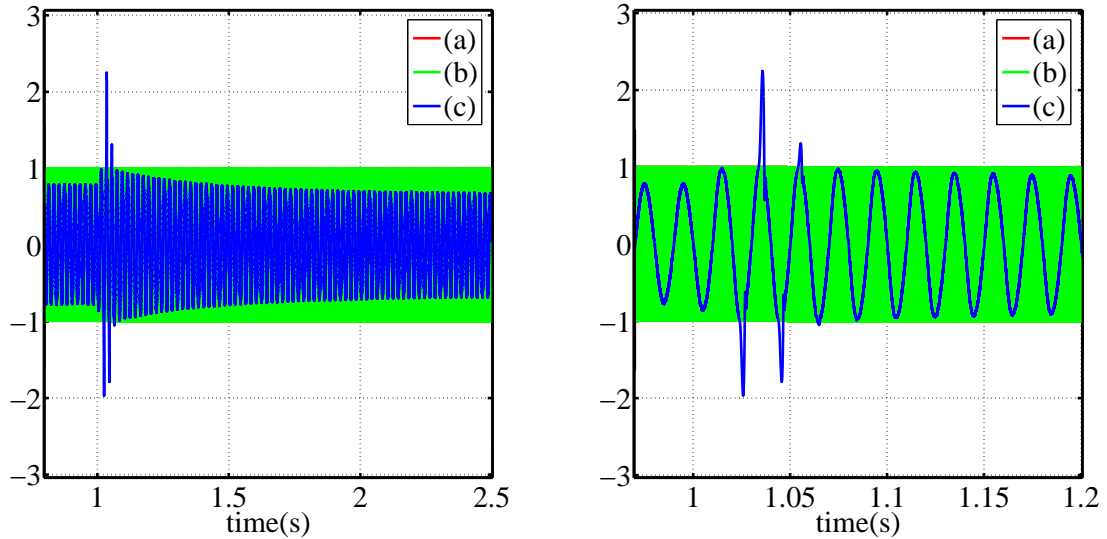


**Figure B.27:** Inductor Current and Current-Loop Reference



**Figure B.28:** Cell Bus-Voltage

Figure B.29 depicts the transient response of  $u_I$  and the two carriers on the left and their detailed result on the right. The transient response, as with the inductor-current transient response, indicates where the AR operates as a full-bridge passive rectifier. This operation causes  $u_I$  to exceed the carrier amplitude limits, because the current-loop attempts to control a system over which it has no control. As soon as  $v_{cb}$  exceeds  $v_{ac}$ , the control-loop regains control and the AR operates normally.



**Figure B.29:** PWM Signals: (a) Carrier1; (b) Carrier2; (c)  $u_I$

The simulation results presented in this appendix verify acceptable AR operation during load steps. It is also shown that  $i_L$  peaks can be expected when the load step causes  $v_{cb}$  to drop below  $v_{ac}$  during the  $v_{cb}$  transient.

## B.5 Test Measurement Details

### B.5.1 Current-Loop Test Setup

The test setup, as depicted in Figure B.30, is aimed at verifying circuit and control implementation as well as current-loop functionality in terms of its reference tracking ability.

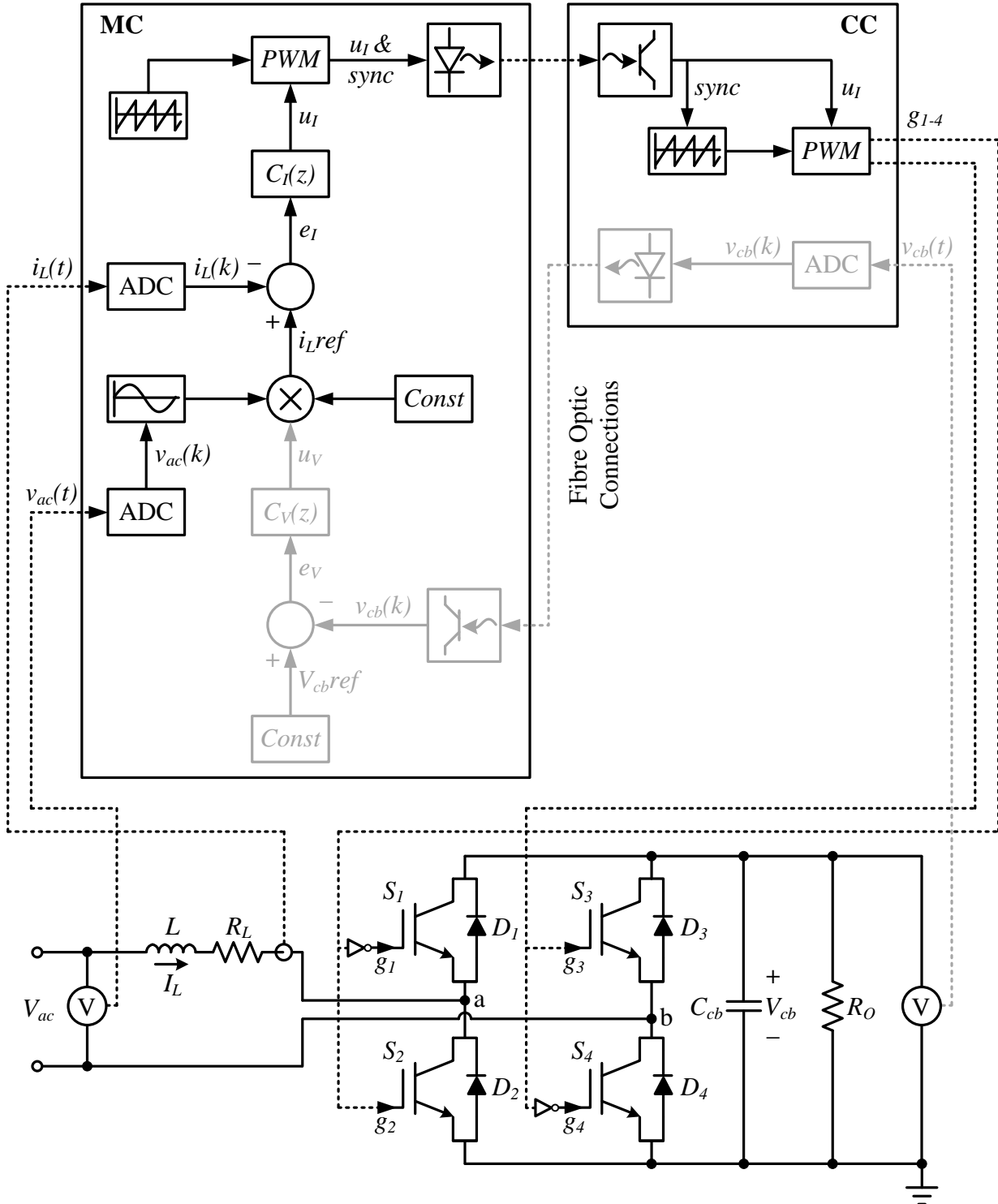


Figure B.30: Current-Loop Test Setup

The test-setup details are listed below:

- The control is jointly implemented on the MC and CC, as discussed in Section 4.4. The voltage-loop is disabled by replacing  $u_V$  with a constant 5 Ap, to be multiplied with the synchronised unit-sinusoid.
- The input voltage,  $V_{ac}$ , is received from a bench variac capable of supplying a 0-230 V line-neutral voltage.
- The inductor,  $L$  has a value of 5.8 mH.
- The inductor resistance,  $R_L$ , represents two lumped resistor values. One is the actual inductor resistance and the second is an input resistor of 6  $\Omega$ . The input resistor is added for protection, to absorb power if an error occurs causing high current flow.
- The cell bus-capacitor,  $C_{cb}$ , has a value of 200  $\mu\text{F}$ .
- The load resistor,  $R_O$ , has a value of 110  $\Omega$ .
- The AR and DC-DC converter is a unit within the cell. The AR is thus tested separate from the DC-DC converter by removing the isolation transformer and connecting the load to the DC-DC output terminals. Switches  $S_5$  and  $S_8$  are closed while switches  $S_6$  and  $S_7$  remain open. Figure B.31 depicts the cell configuration.

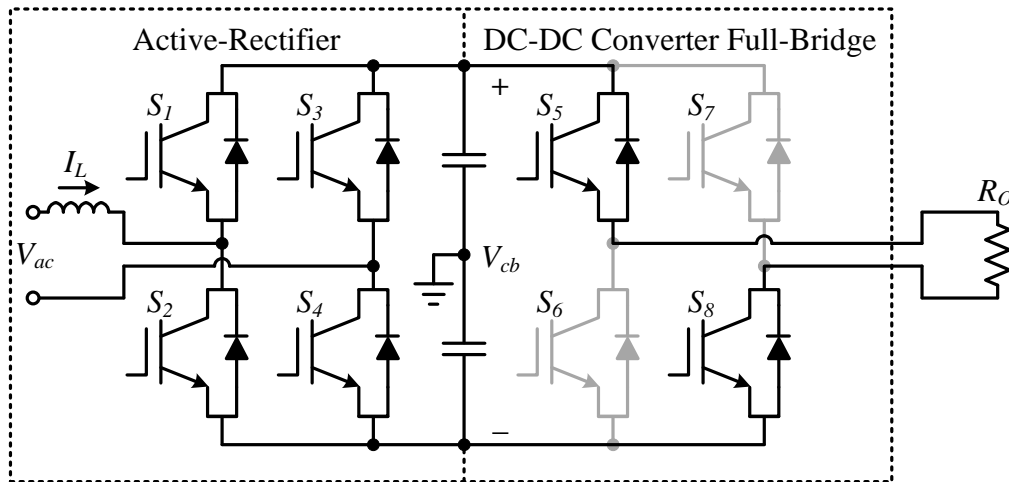


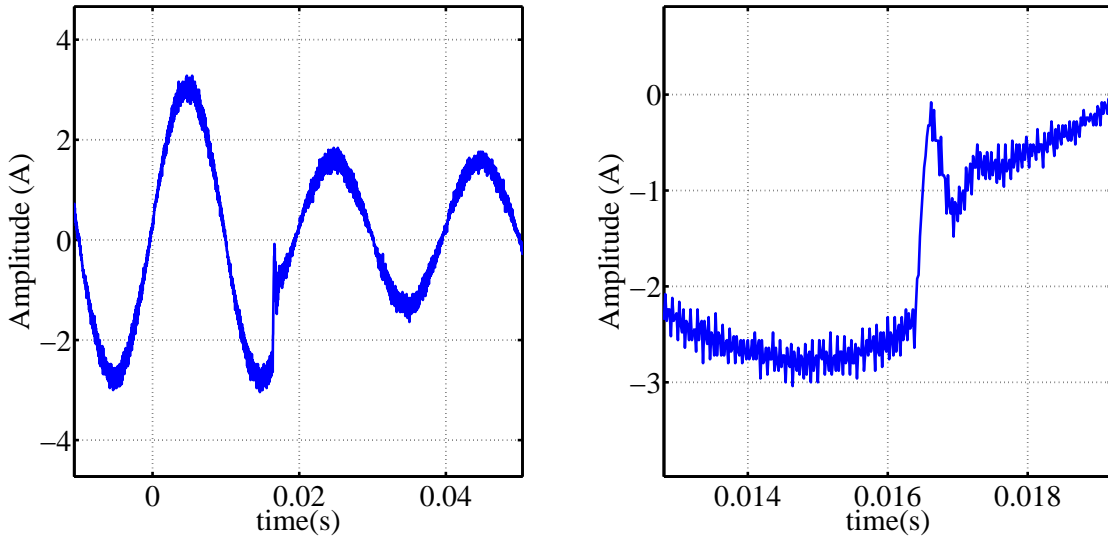
Figure B.31: DC-DC Bypass Cell-Setup

## B.5.2 Current-Loop Reference-Step Measurement Analysis

In this section two measurement tests are presented aimed at verifying acceptable current-loop operation during reference steps.

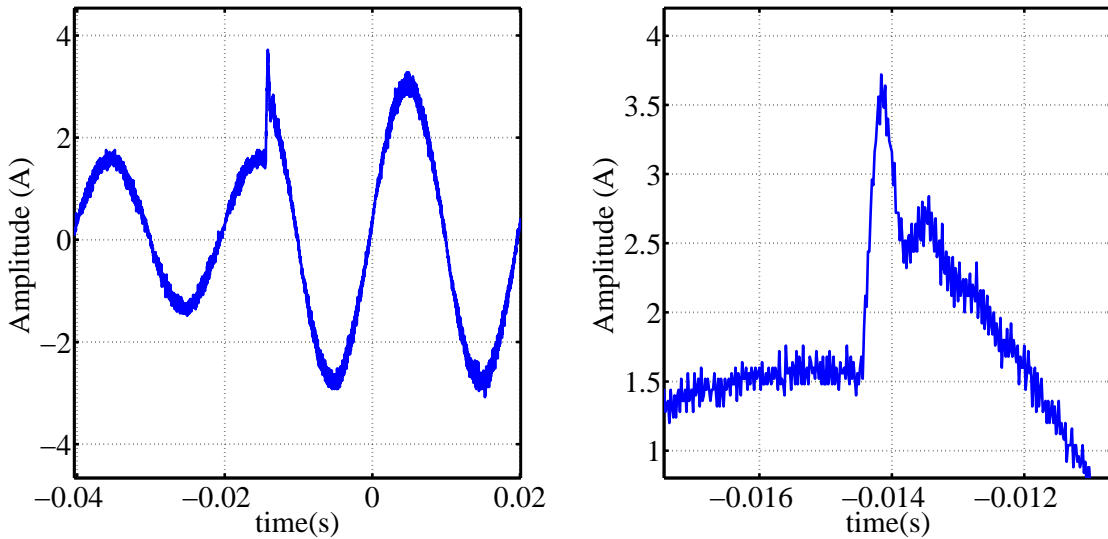
The first test introduces a reference step of:  $i_{Lref} = 3$  to 1.5 Ap. This reduces the input power by 50 % at an arbitrary position of the sinusoidal current. Figure B.32 depicts the  $i_L$  step-down on the left and a detailed result on the right. It is shown that  $i_L$  successfully tracks  $i_{Lref}$  with a  $\pm 30$  % overshoot compared to the  $i_{Lref}$  step size.

The second test introduces a reference step of:  $i_{Lref} = 1.5$  to 3 Ap. This increases the input power by 100 % at an arbitrary position of the sinusoidal current. Figure B.33 depicts the  $i_L$



**Figure B.32:** Oscilloscope Measurement: Inductor Current

step-up on the left and a detailed result on the right. It is shown that  $i_L$  successfully tracks  $i_{Lref}$  with a  $\pm 70\%$  overshoot compared to the  $i_{Lref}$  step size.



**Figure B.33:** Oscilloscope Measurement: Inductor Current

Figure B.34 depicts the  $v_{cb}$  transient response of the first measurement test on the left and its transient response of the second measurement test on the right. The  $v_{cb}$  value merely increases when the input power is increased and decreases when the input power is decreased, maintaining its 100 Hz ripple throughout. Each transient endures for  $\pm$  ten ripple cycles.

The test measurements presented in this appendix verify acceptable current-loop operation during reference steps. The fast tracking ability of the current-loop, due to its high bandwidth, is also verified. The observed overshoots are expected given the step response of the closed current-loop, discussed in Appendix B.2.2.

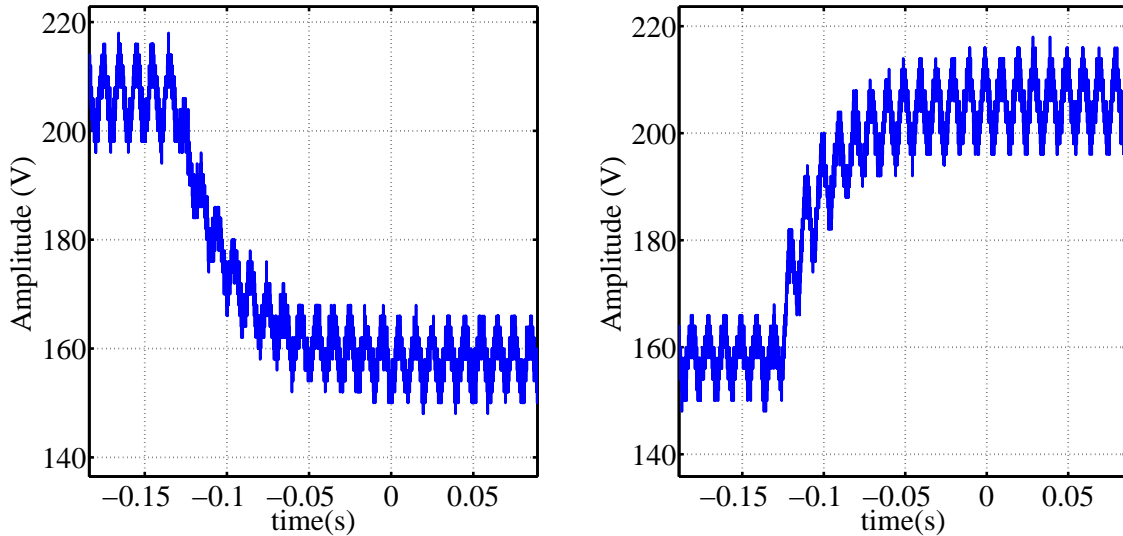


Figure B.34: Oscilloscope Measurement: Cell Bus-Voltage

### B.5.3 Active-Rectifier Test Setup

The test setup, as depicted in Figure B.35, is aimed at verifying successful current- and voltage-loop integration as well as voltage-loop functionality in terms of its reference tracking ability.

The test-setup details are listed below:

- The control is jointly implemented on the MC and CC, as discussed in Section 4.4. The voltage-loop constant reference is set to 150V.
- The input voltage,  $V_{ac}$ , is received from a bench variac capable of supplying a 0-230 V line-neutral voltage.
- The inductor,  $L$  has a value of 5.8 mH.
- The inductor resistance,  $R_L$ , represents two lumped resistor values. One is the actual inductor resistance and the second is an input resistor of 6  $\Omega$ . The input resistor is added for protection, to absorb power if an error occurs causing high current flow.
- The cell bus-capacitor,  $C_{cb}$ , has a value of 200  $\mu\text{F}$ .
- The load resistor,  $R_O$ , has a value of 277  $\Omega$  or 110  $\Omega$ .
- The AR and DC-DC converter is a unit within the cell. The AR is thus tested separate from the DC-DC converter by removing the isolation transformer and connecting the load to the DC-DC output terminals. Switches  $S_5$  and  $S_8$  are closed while switches  $S_6$  and  $S_7$  remain open. Figure B.31 depicts the cell configuration.

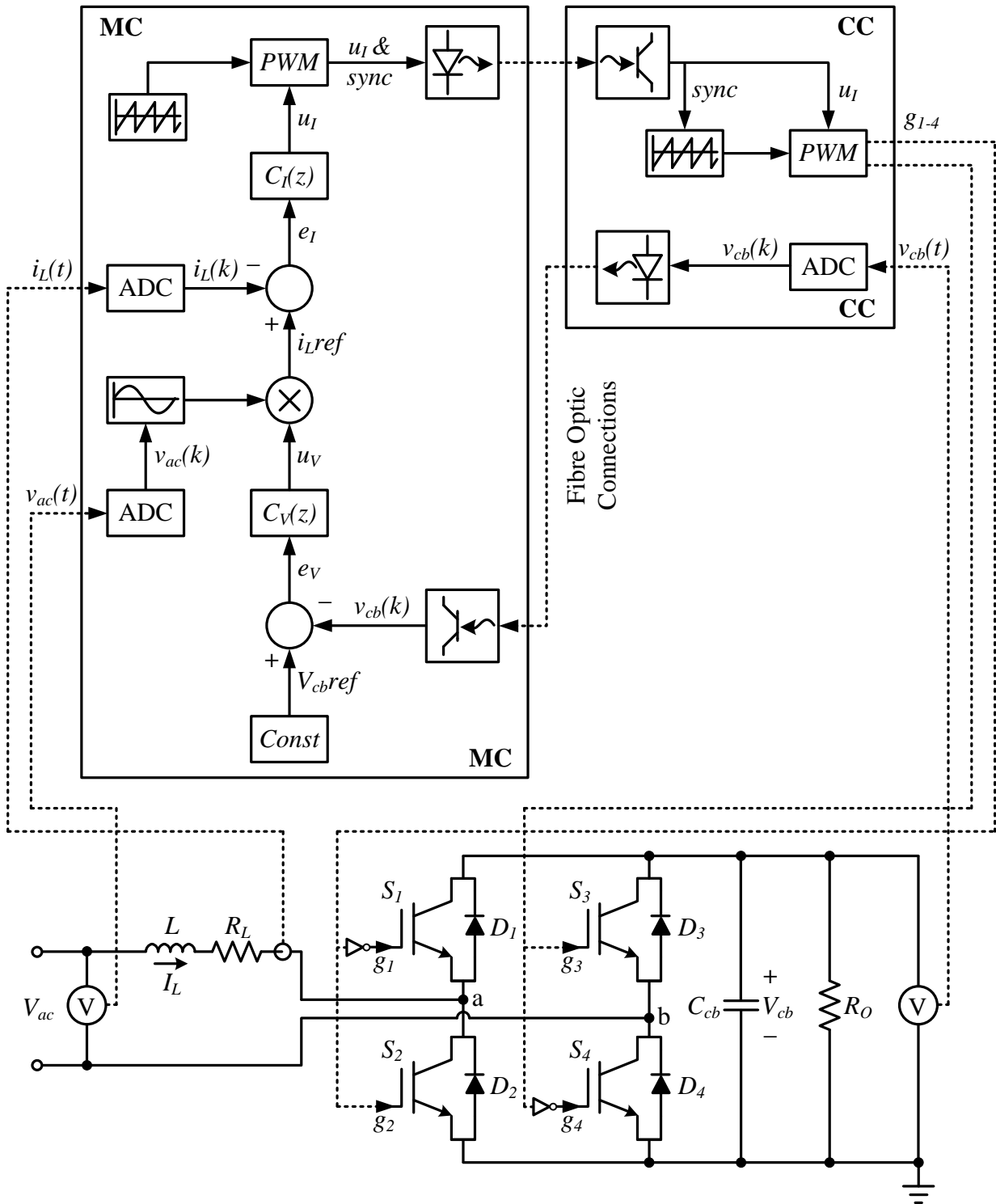
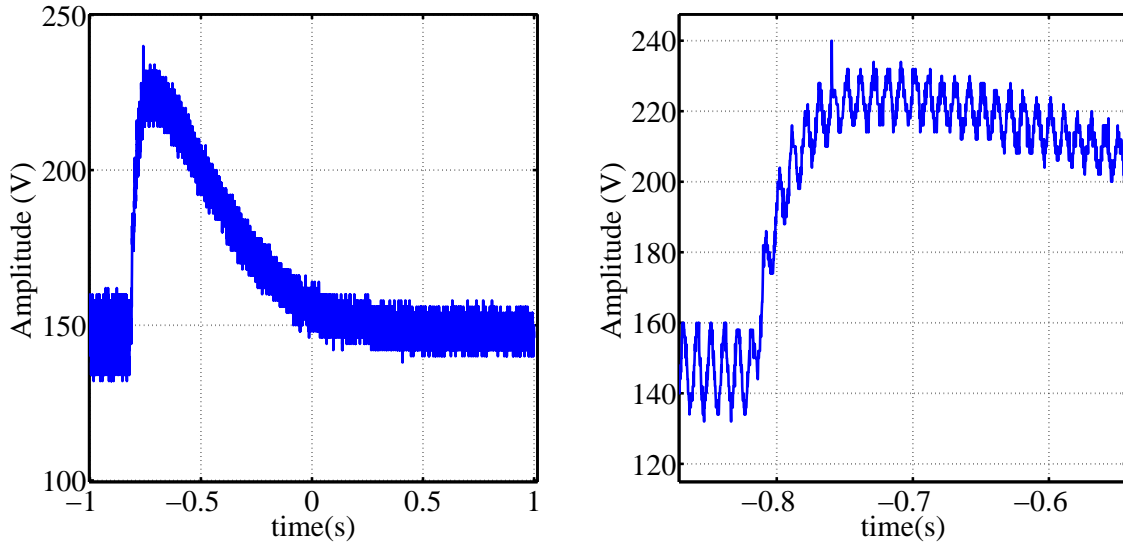


Figure B.35: Active-Rectifier Test Setup

### B.5.4 Load-Step Measurement Analysis

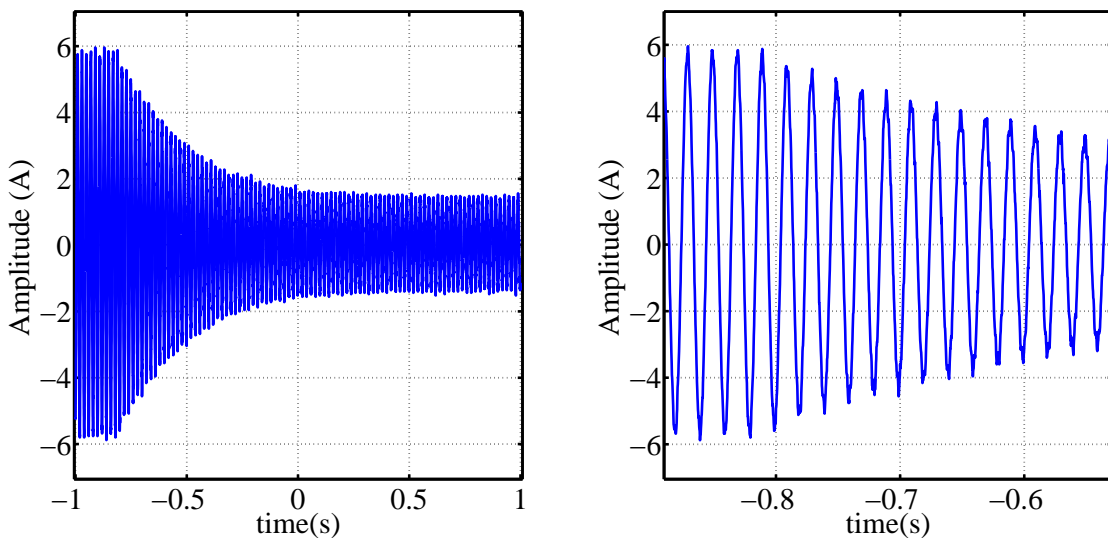
Two measurement tests are presented, aimed at verifying acceptable AR operation during load steps. The first test introduces a load step of 110  $\Omega$  to 277  $\Omega$ . This results in an output power step-down of  $\pm 40\%$ .

Figure B.36 depicts the  $v_{cb}$  transient oscilloscope measurement on the left and the detailed measurement on the right. While the energy transferred from  $C_{cb}$  to  $R_O$  steps down almost instantly, the energy transferred from  $L$  to  $C_{cb}$  has a relatively slow transient, caused by the low voltage-loop bandwidth. Examining  $C_{cb}$ , the energy input is larger than the energy output which causes  $v_{cb}$  to rise, and then fall again as the energy input is decreased. The detailed measurement shows that the 100 Hz ripple is maintained throughout, although its amplitude is decreased.



**Figure B.36:** Oscilloscope Measurement: Cell Bus-Voltage

Figure B.37 depicts the  $i_L$  transient oscilloscope measurement on the left and the detailed measurement on the right. The  $i_L$  transient is a representation of the energy transient, transferred from  $L$  to  $C_{cb}$ . Also referred to as the  $C_{cb}$  energy input. The detailed measurement shows that  $i_L$  maintains its sinusoidal profile throughout.

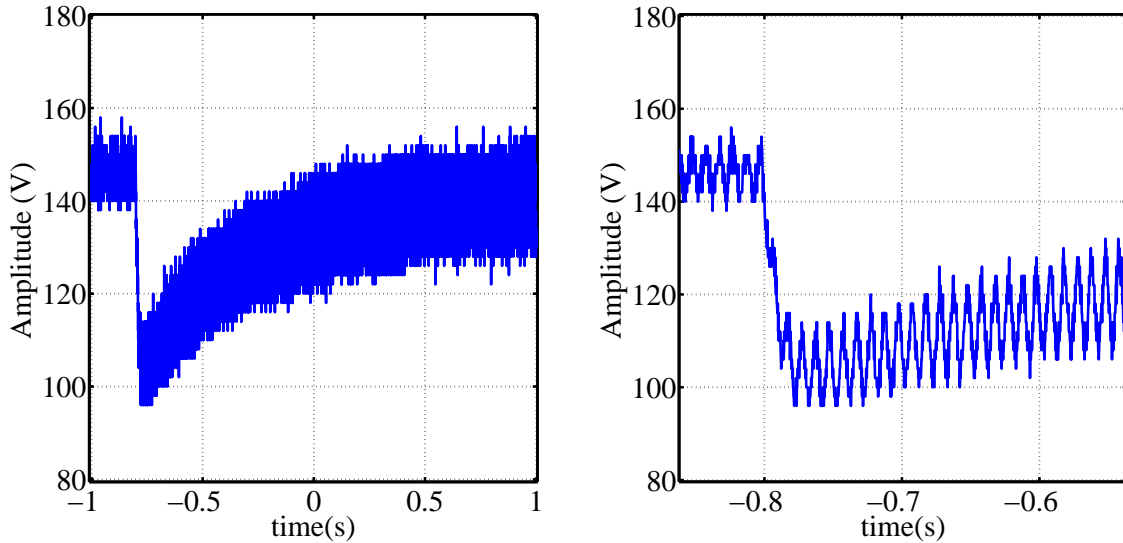


**Figure B.37:** Oscilloscope Measurement: Inductor-Current

The second test introduces a load step of  $277 \Omega$  to  $110 \Omega$ . This results in an output power step-up of  $\pm 150 \%$ .

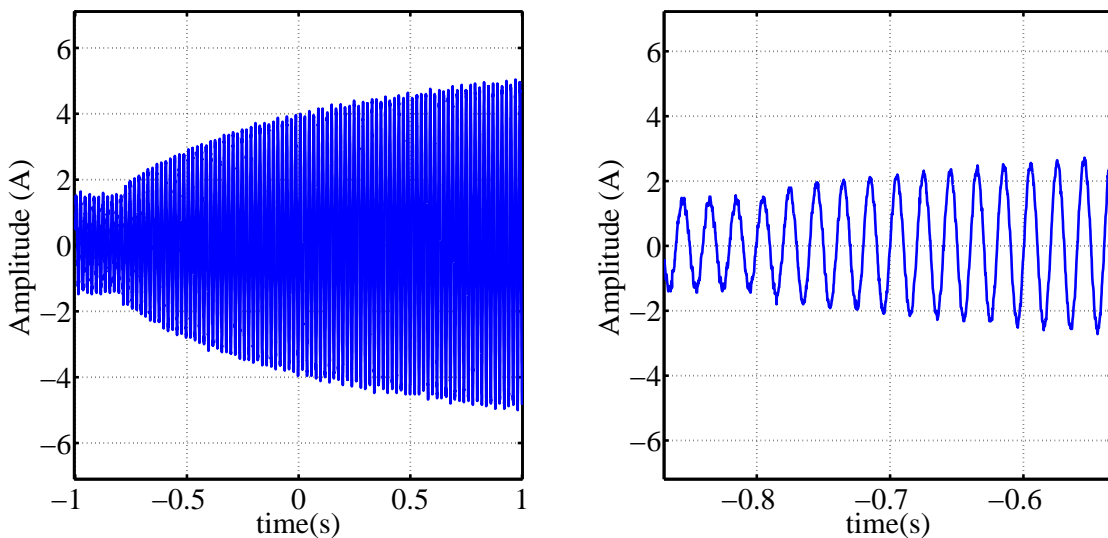


Figure B.38 depicts the  $v_{cb}$  transient oscilloscope measurement on the left and the detailed measurement on the right. While the energy transferred from  $C_{cb}$  to  $R_O$  steps up almost instantly, the energy transferred from  $L$  to  $C_{cb}$  has a relatively slow transient, caused by the low voltage-loop bandwidth. Examining  $C_{cb}$ , the energy output is larger than the energy input which causes  $v_{cb}$  to drop, and then rise again as the energy input is increased. The detailed measurement shows that the 100 Hz ripple is maintained throughout, although its amplitude is increased.



**Figure B.38:** Oscilloscope Measurement: Cell Bus-Voltage

Figure B.39 depicts the  $i_L$  transient oscilloscope measurement on the left and the detailed measurement on the right. The  $i_L$  measurement is a representation of the energy transient, transferred from  $L$  to  $C_{cb}$ . Also referred to as the  $C_{cb}$  energy input. The detailed measurement shows that  $i_L$  maintains its sinusoidal profile throughout.



**Figure B.39:** Oscilloscope Measurement: Inductor-Current

The  $i_L$  peaks at power step-up, as shown in Appendix B.4.4 Figure B.27, are not as prominent in this test. This is partly because  $V_{ac}$  is also decreased at power step-up due to the voltage-drop increase across the variac, for example.

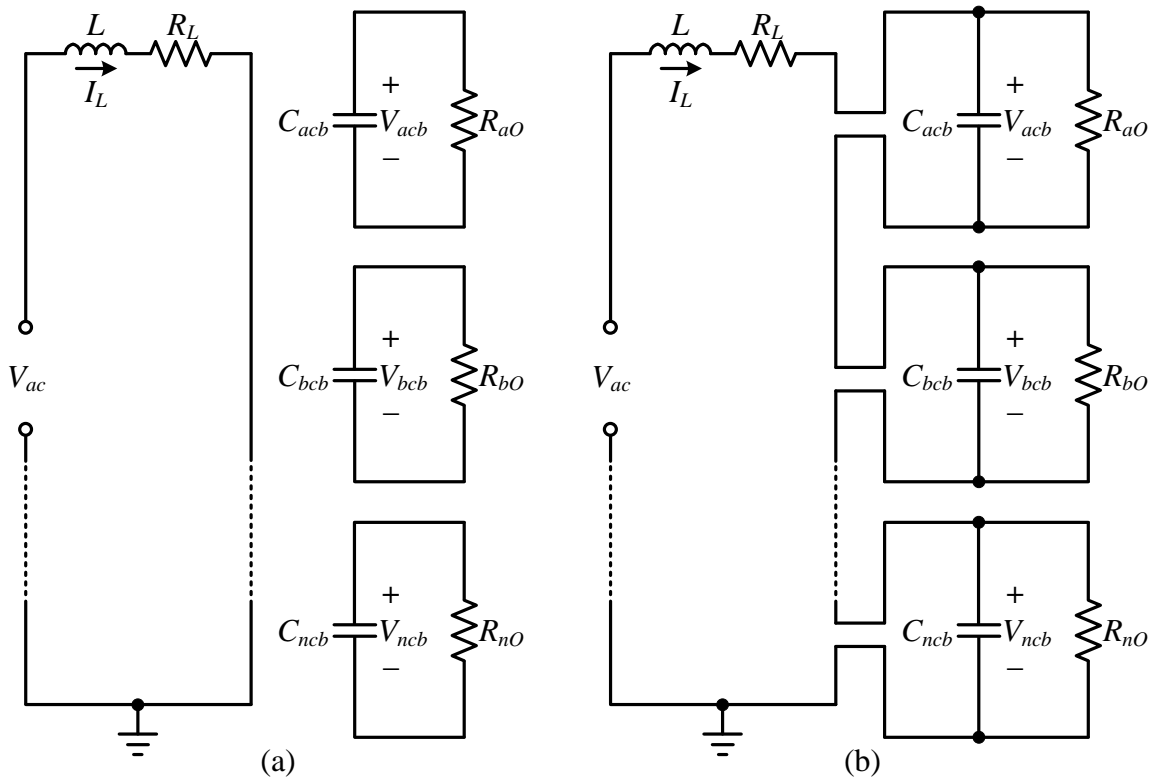
The simulation results presented in this appendix verify acceptable AR operation during load steps.

# Appendix C

## Cascaded Active-Rectifier Control Details

### C.1 Current-Loop Plant Expansion details

The plant analysis starts by using the two AR states discussed in Appendix B.1.1. Each AR in the stack can represent State 1 or State 2. The physical CAR thus has an enormous amount of states consisting of combinations of AR State 1 and State 2. Averaging is used to construct two CAR states with all the ARs simultaneously representing AR State 1 or State 2. Figure C.1 depicts the two CAR states.



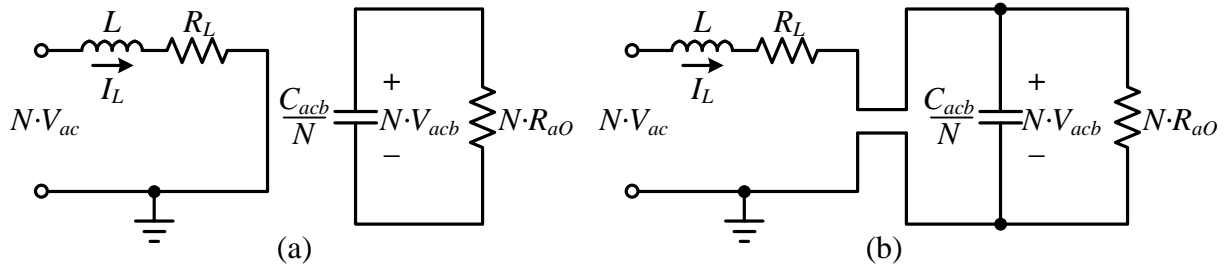
**Figure C.1:** Cascaded Active-Rectifier Circuit Diagram: (a) State 1; (b) State 2

These two state circuits can be reduced to the two AR state circuits. This reduction however involves certain circuit parameter changes. The parameter changes from one AR to an  $N$  AR stack is listed below:

Parameter	One AR	$N$ AR Stack	Units
Power Rating	$P$	$N \cdot P$	kW
Input-Voltage	$V_{ac}$	$N \cdot V_{ac}$	Vp
Input-Inductor Current	$I_L$	$I_L$	A
Input-Inductance	$L$	$L$	mH
Inductor Resistance	$R_L$	$R_L$	$\Omega$
Bus-Voltage	$V_{cb}$	$N \cdot V_{cb}$	V
Bus Capacitance	$C_{cb}$	$C_{cb}/N$	$\mu\text{F}$
Load Resistance	$R_O$	$N \cdot R_O$	$\Omega$

**Table C.1:** Active-Rectifier and  $N$  Active-Rectifier Stack State Parameters

The averaged state circuits are thus depicted in Figure C.2.


**Figure C.2:** Simplified Cascaded Active-Rectifier Circuit Diagram: (a) State 1; (b) State 2

These states are thus identical to the states used to determine the AC small-signal linear model of a single AR. The symbolic parameters in the AR model are thus altered to model the  $N$  AR stack:

$$G_I(s) = \frac{NV_{cb}}{L} \times \frac{s + \frac{2}{R_O C_{cb}}}{s^2 + \left(\frac{R_L}{L} + \frac{1}{R_O C_{cb}}\right)s + \frac{R_L}{R_O L C_{cb}} + \frac{N(1-D)^2}{L C_{cb}}} \quad (\text{C.1.1})$$

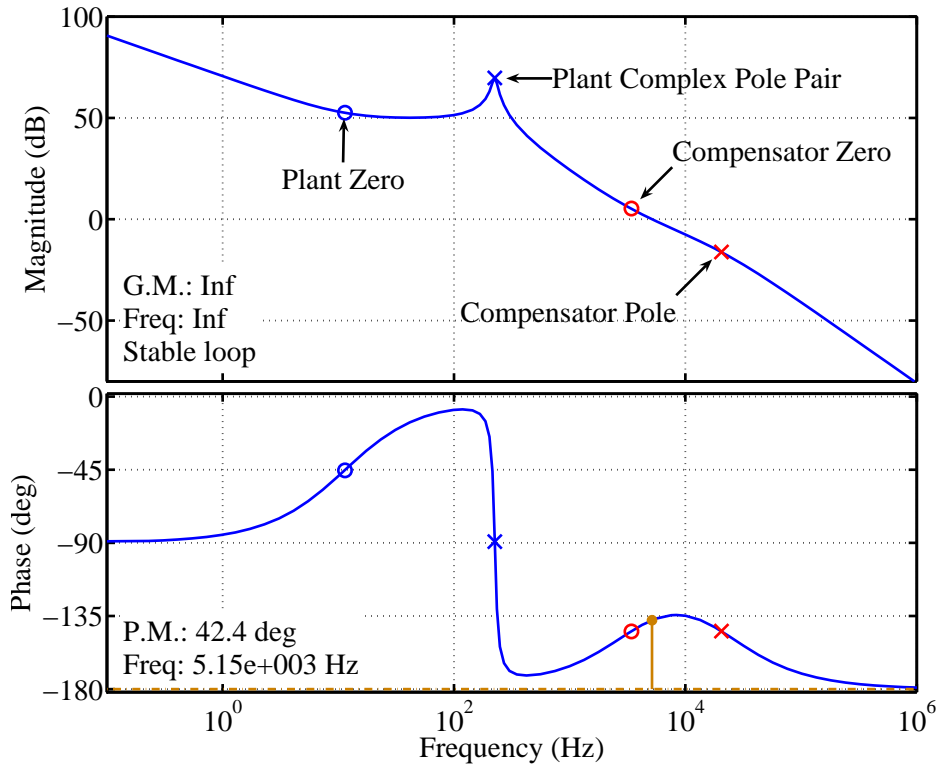
## C.2 Current-Loop Analysis

The open current-loop detailed frequency responses with  $D = 0$ ,  $D = 0.4107$  and  $D = 1$  are shown in Figure C.3, C.4 and C.5 respectively. These figures indicate the positions of the poles and zeros of both the plant and compensator. All three open-loops have an infinite gain margin and stable phase margins of  $42.4^\circ$ .

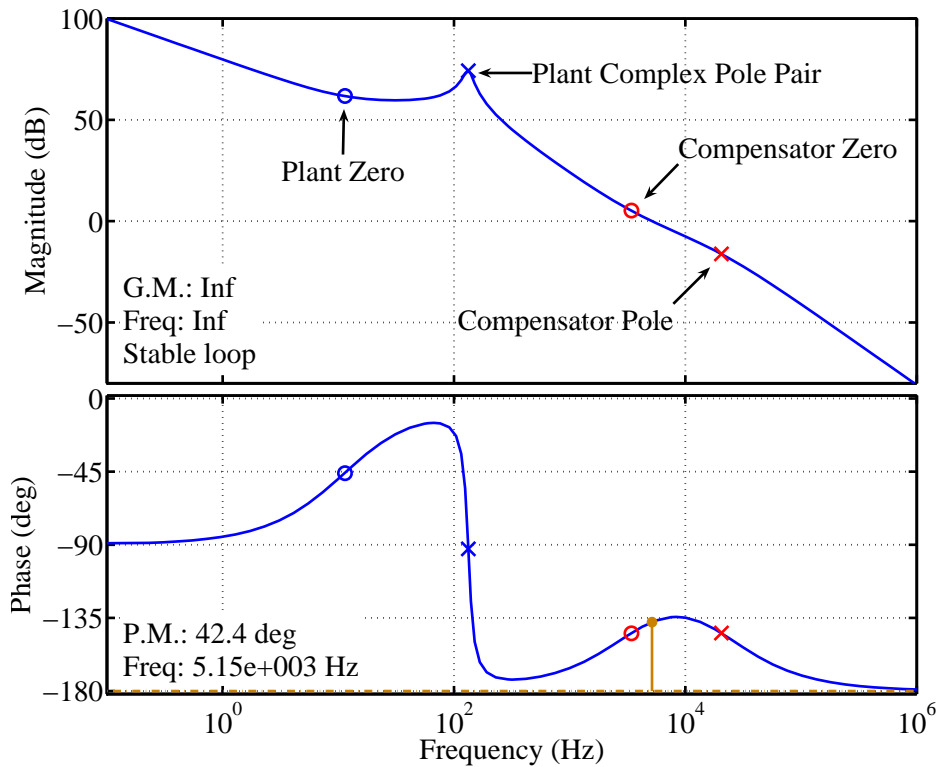
Figure C.6 depicts the unit-step transient response of the current-loop. The transient response characteristics of the underdamped system are listed below:

$$\begin{aligned} \text{Rise time, } t_r &= 55.9 \mu\text{s } 0\text{-}100\% \\ \text{Peak time, } t_p &= 111 \mu\text{s} \\ \text{Peak overshoot, } M_p &= 1.398 \\ \text{Settling time, } t_s \text{ } 2\% &= 338 \mu\text{s} \end{aligned}$$

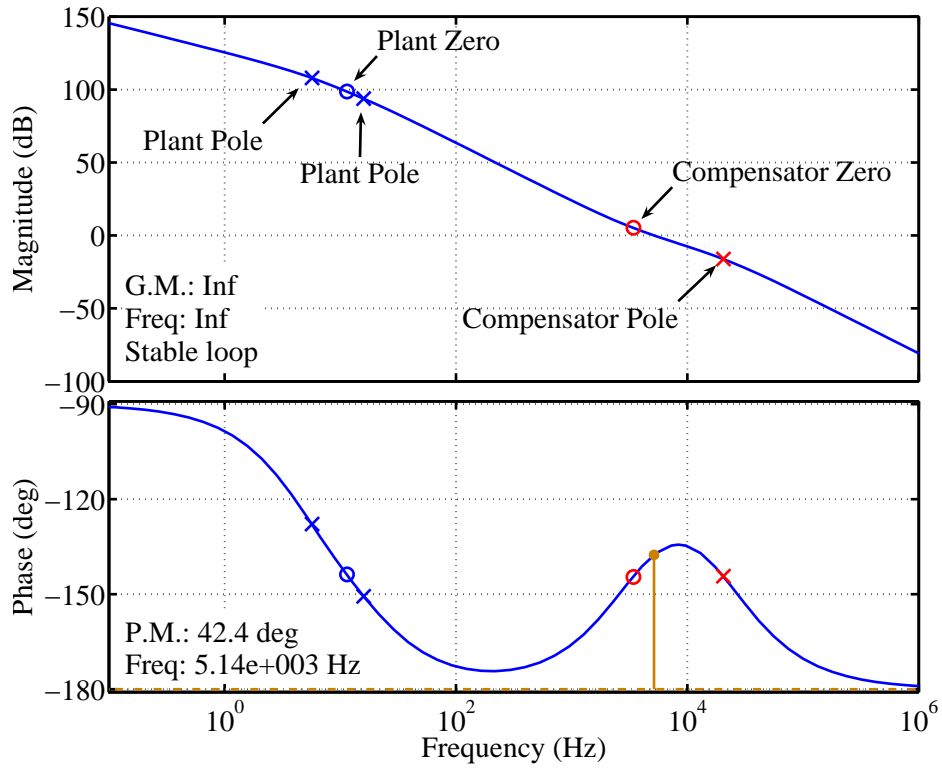
Figure C.7 depicts the impulse response of the current-loop.



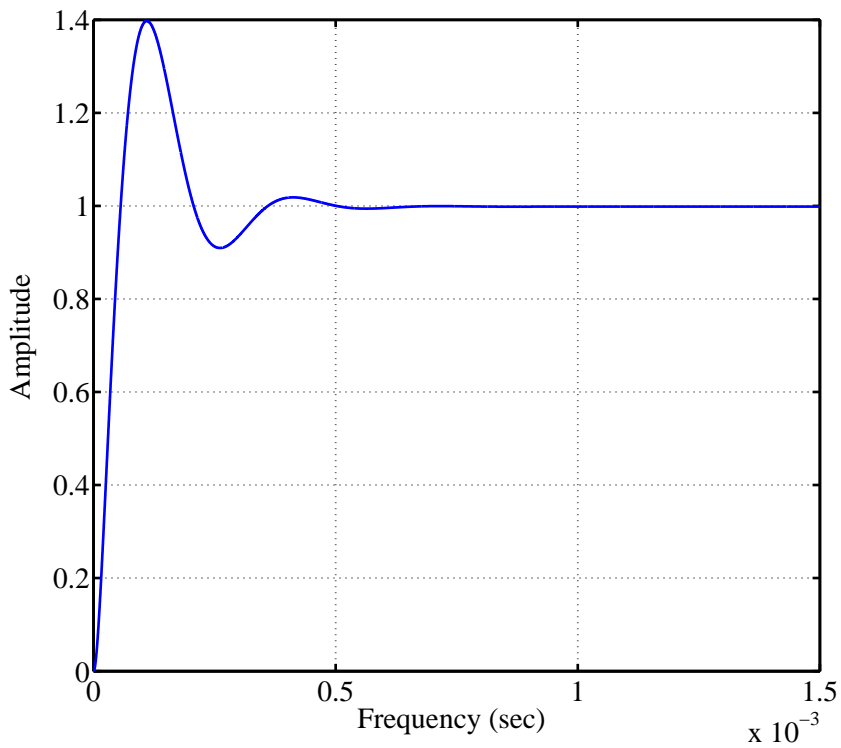
**Figure C.3:** Detailed Frequency Response of  $C_I(s) \cdot G_I(s)$  with  $D = 0$



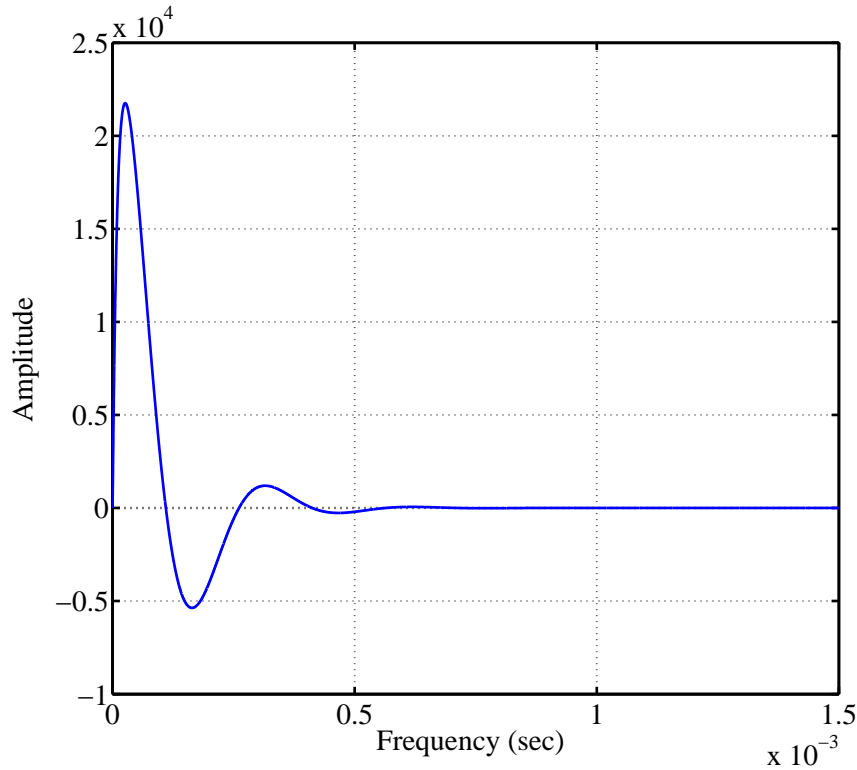
**Figure C.4:** Detailed Frequency Response of  $C_I(s) \cdot G_I(s)$  with  $D = 0.4107$



**Figure C.5:** Detailed Frequency Response of  $C_I(s) \cdot G_I(s)$  with  $D = 1$



**Figure C.6:** Current-Loop Step Response



**Figure C.7:** Current-Loop Impulse Response

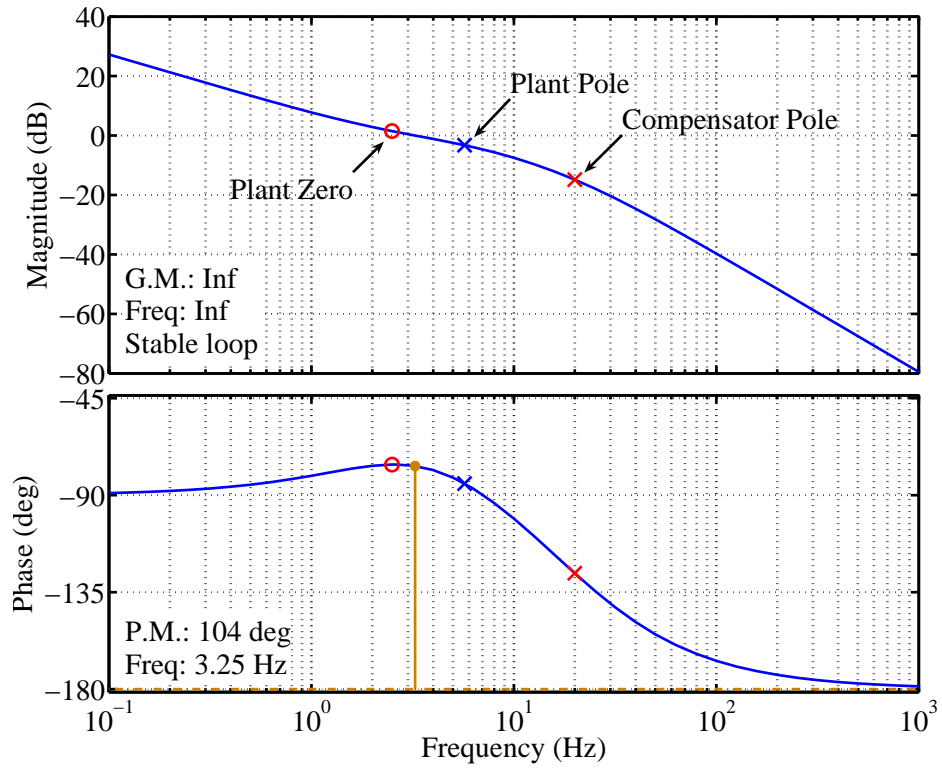
### C.3 Voltage-Loop Analysis

The open-voltage-loop is analysed with the detailed frequency response, depicted in Figure C.8. This figure indicates the poles and zeros of the plant,  $G_V(s)$ , and compensator,  $C_V(s)$ , respectively. This open-loop has an infinite gain margin and a very stable phase margin of  $104^\circ$ .

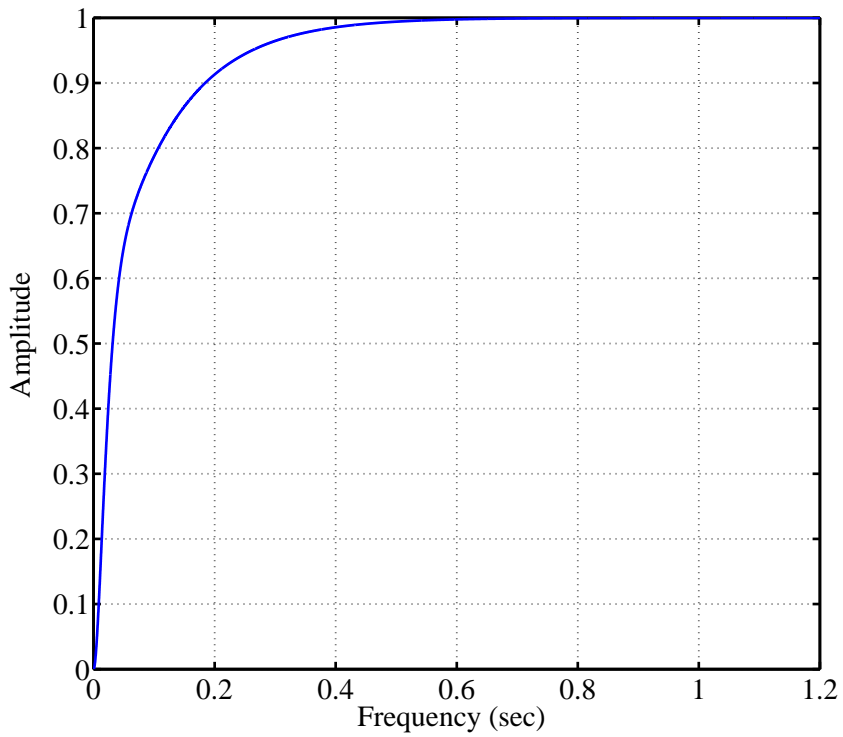
Figure C.9 depicts the transient response of the voltage-loop with a unity step input. The transient response characteristics of this overdamped system are listed below:

$$\begin{aligned} \text{Rise time, } t_r &= 184 \text{ ms } 0\text{-}90\% \\ \text{Settling time, } t_s \text{ } 2\% &= 364 \text{ ms} \end{aligned}$$

Figure C.10 depicts the impulse response of the voltage-loop.



**Figure C.8:** Detailed Frequency Response of  $C_V(s) \cdot G_V(s)$



**Figure C.9:** Voltage-Loop Step Response



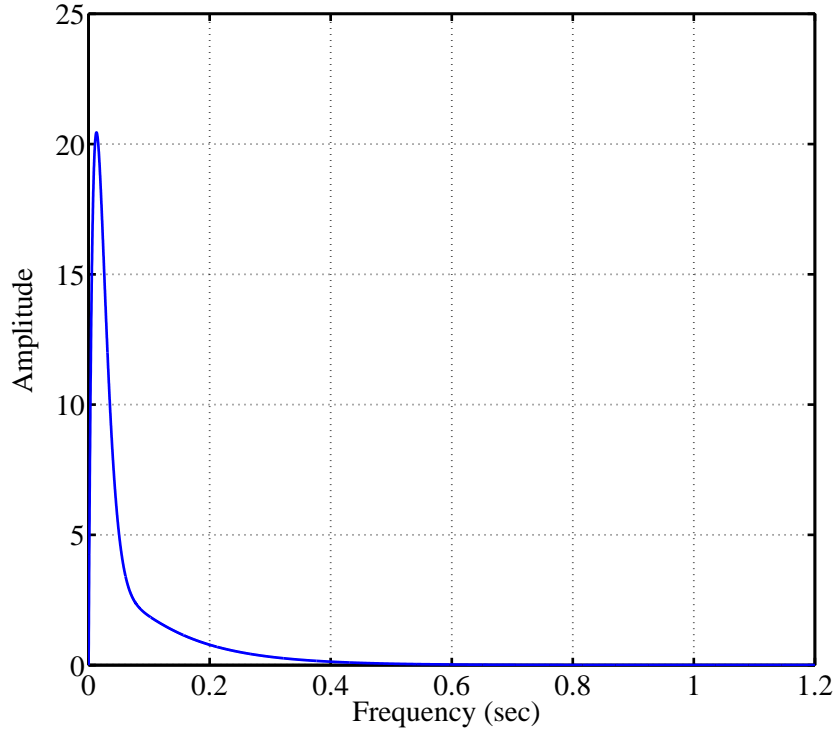


Figure C.10: Voltage-Loop Impulse Response

## C.4 Simulation Details

### C.4.1 Cascaded Active-Rectifier Simulation Setup

The simulation setup, as depicted in Figure C.11, is aimed at verifying current- and voltage-loop integration as well as natural bus-voltage balancing and rebalancing of two ARs.

The simulation-setup details are listed below:

- The electrical component values are:

$$\begin{aligned}
 V_{ac} &= 250 \sin(2\pi f_{in} t) \text{ V} \\
 L &= 5.8 \text{ mH} \\
 R_L &= 6 + 0.5 \Omega \\
 C_{acb}, C_{bcb} &= 200 \mu\text{F} \\
 R_{aO}, R_{bO} &= 110 \Omega \text{ or } 267 \Omega
 \end{aligned}$$

The inductor resistance,  $R_L$ , represents two lumped resistor values. One is the actual inductor resistance and the second is an input resistor of  $6 \Omega$ . The input resistor is added for protection in the measurement test setup, to absorb power if an error occurs causing high current flow.

- The IGBT and Diode are system level models found in the Simplorer8 library, LIBRARY: Simplorer Elements\Basic Elements\Circuit\Semiconductor System Level. The component settings are as follows:

$$\begin{aligned}
 \text{Type} &= \text{Equivalent Line} \\
 \text{Forward Voltage} &= 0.8 \text{ V} \\
 \text{Bulk Resistance} &= 1 \text{ m}\Omega \\
 \text{Reverse Resistance} &= 10 \text{ k}\Omega
 \end{aligned}$$

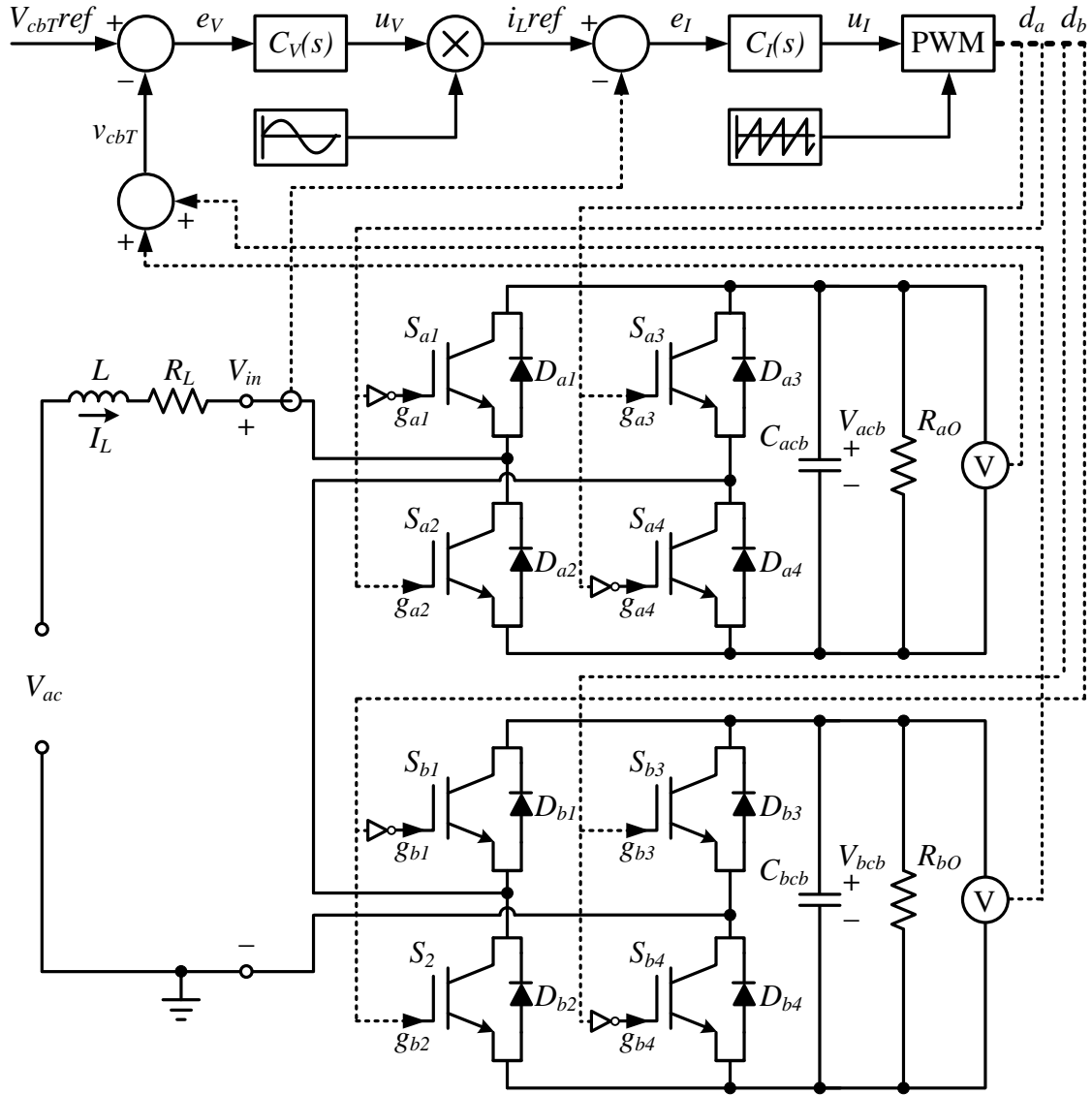


Figure C.11: Cascaded Active-Rectifier Simulation setup

- The voltage-loop reference is a constant value set to the desired average total bus-voltage:

$$V_{cbTref} = 300 \text{ V} \quad (\text{C.4.1})$$

- The total cell bus-voltage feedback is the summation of the respective cell bus-voltages.
- The compensator,  $C_V(s)$ , is modeled as the transfer function of Eq. 5.2.20.
- The output of the voltage compensator,  $u_V$ , is multiplied with a unit sinusoid, in phase with  $V_{ac}$ , to generate the current-loop reference:

$$i_{Lref}(t) = u_V(t) \cdot \sin(2\pi f_{in} t) \quad (\text{C.4.2})$$

- The compensator,  $C_I(s)$ , is modeled as the transfer function of Equation 5.2.15.
- The PWM component of the current-loop implements unipolar-voltage switching with two pairs of interleaved sawtooth carriers, as explained in Section 5.2.1. Gating signal,  $d_{a1}$ , is dependent on the compensator output,  $u_I$ , and  $Carrier_{a1}$ . Gating signal,  $d_{a2}$ , is

dependent on  $u_I$  and  $Carrier_{a2}$ . Gating signal,  $d_{b1}$ , is dependent on  $u_I$  and  $Carrier_{b1}$ . Gating signal,  $d_{b2}$ , is dependent on  $u_I$  and  $Carrier_{b2}$ . Switches  $S_{a2}$  and  $S_{a3}$  are gated on  $d_{a1}$  and  $d_{a2}$  respectively. Switches  $S_{a1}$  and  $S_{a4}$  are gated on the inverse of  $d_{a1}$  and  $d_{a2}$  respectively. Switches  $S_{b2}$  and  $S_{b3}$  are gated on  $d_{b1}$  and  $d_{b2}$  respectively. Switches  $S_{b1}$  and  $S_{b4}$  are gated on the inverse of  $d_{b1}$  and  $d_{b2}$  respectively.

## C.5 Test Measurement Details

### C.5.1 Cascaded Active-Rectifier Test Setup

The two AR stack test setup, as depicted in Figure C.12, is aimed at verifying successful current- and voltage-loop integration as well as natural cell bus-voltage balancing with equal loads and natural cell bus-voltage rebalancing after an external perturbation.

The test-setup details are listed below:

- The control is jointly implemented on the MC and respective CCs, as discussed in Section 5.4. The voltage-loop constant reference,  $V_{cbTref}$ , is set to 300V.
- The input voltage,  $V_{ac}$ , is received from a bench variac capable of supplying a 0-230 V line-neutral voltage.
- The inductor,  $L$  has a value of 5.8 mH.
- The inductor resistance,  $R_L$ , represents two lumped resistor values. One is the actual inductor resistance and the second is an input resistor of 6  $\Omega$ . The input resistor is added for protection, to absorb power if an error occurs causing high current flow.
- The cell bus-capacitors,  $C_{acb}$  and  $C_{bcb}$ , each has a value of 200  $\mu\text{F}$ .
- The load resistors,  $R_{aO}$  and  $R_{bO}$ , has values of 267  $\Omega$  or 110  $\Omega$ .
- The AR and DC-DC converter is a unit within the cell. Each AR is thus tested separate from the respective DC-DC converter by removing the isolation transformer and connecting the respective load to the respective DC-DC output terminals. Switches  $S_{a5}$ ,  $S_{a8}$ ,  $S_{b5}$  and  $S_{b8}$  are closed while switches  $S_{a6}$ ,  $S_{a7}$ ,  $S_{b6}$  and  $S_{b7}$  remain open. Figure B.31 depicts the cell configuration.

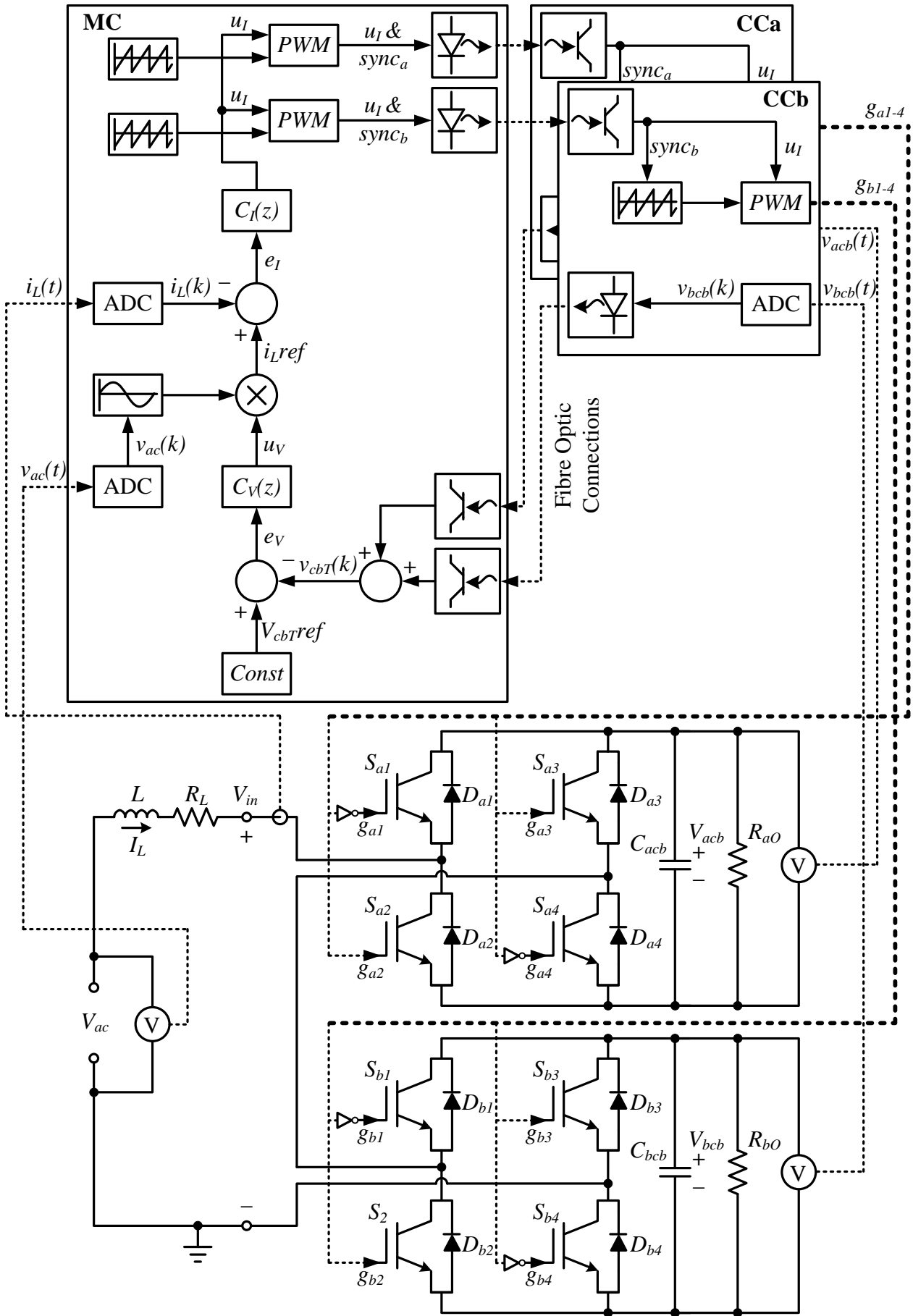


Figure C.12: Cascaded Active-Rectifier Test Setup

# Appendix D

## DC-DC Converter Control Details

### D.1 DC-DC Converter Voltage-Loop Details

#### D.1.1 Voltage-Loop Plant Linearisation Details

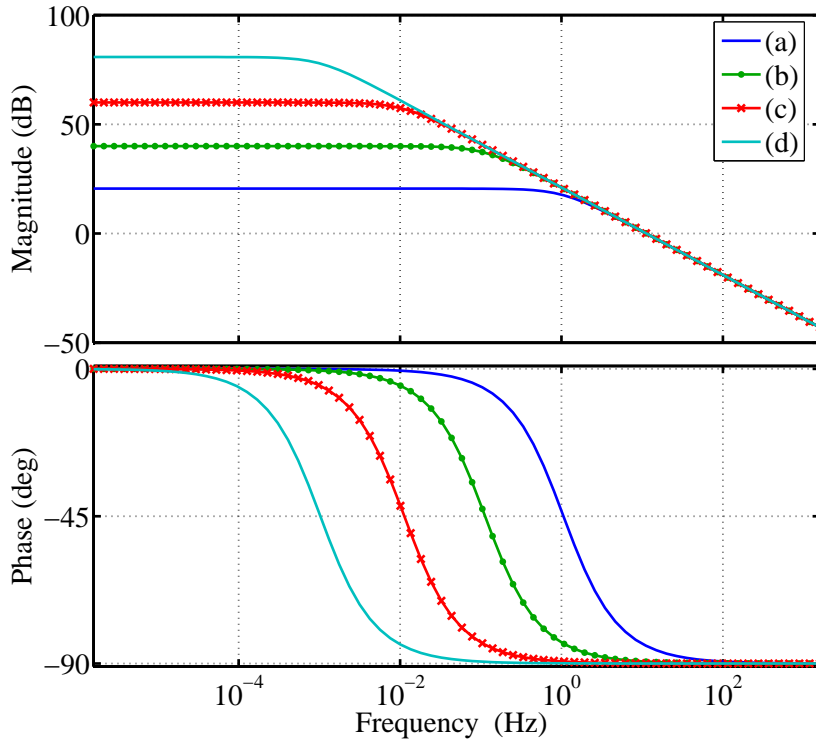
The TPI parameters used to quantify the DC-DC voltage-loop plant model, are listed below:

Parameter	Symbol	Equation	Value	Units
TPI Power Rating	$P_{TPI}$		60	kW
TPI Bus-Voltage	$V_{ib}$		800	V
Load Resistance	$R_O$	$V_{ib}^2 \div P_{TPI} =$	10.67	$\Omega$
TPI Bus-Capacitance	$C_{ib}$		14.1	mF
TPI Bus Bleeding-Resistance	$R_{bleed}$		11	k $\Omega$

**Table D.1:** Three-Phase Inverter Parameters

### D.1.2 Voltage-Loop Plant Model Analysis

Figure D.1 shows the frequency response of the voltage-loop plant model with variations in the load resistance,  $R_O$ . An increase in this resistance and thus a decrease in the power-transfer, results in an increased low-frequency gain and a shift in the phase transition. This shift is to a lower frequency. There is however no variation in the plant bandwidth.



**Figure D.1:** Frequency Response of  $G_V(s)$  with  $R_O$ : (a) 10.67  $\Omega$ ; (b) 100  $\Omega$ ; (c) 1 k $\Omega$ ; (d)  $R_{bleed}$

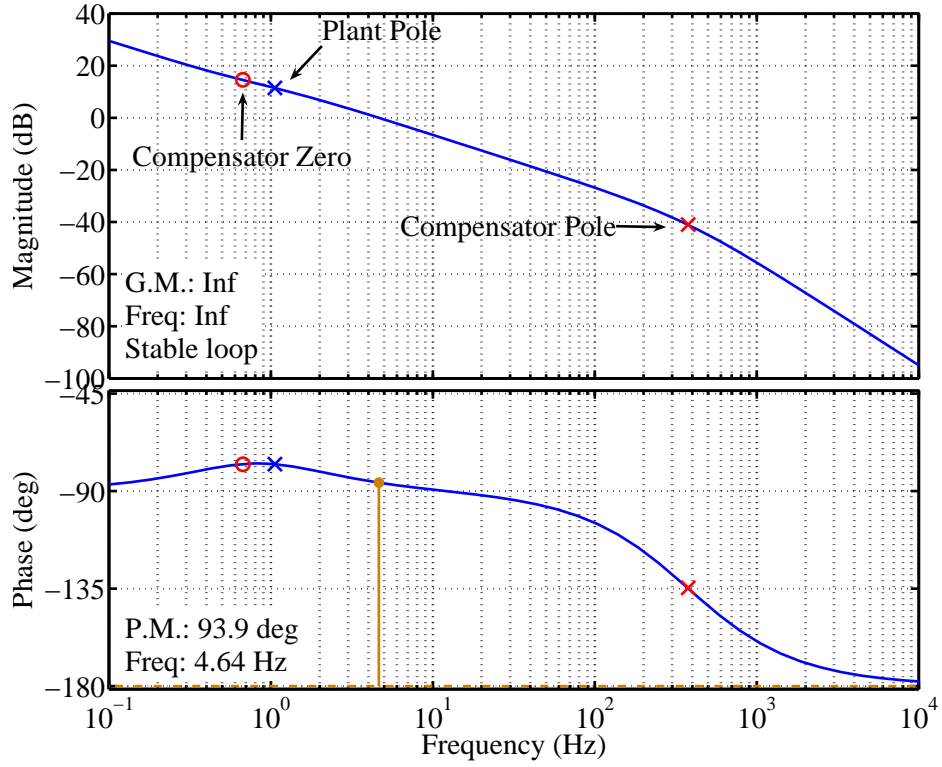
### D.1.3 DC-DC Voltage-Loop Analysis

The open-voltage-loop is analysed with the detailed frequency response, depicted in Figure D.2. This figure indicates the poles and zeros of the plant,  $G_V(s)$ , and compensator,  $C_V(s)$ , respectively. This open-loop has an infinite gain margin and a very stable phase margin of 93.9°.

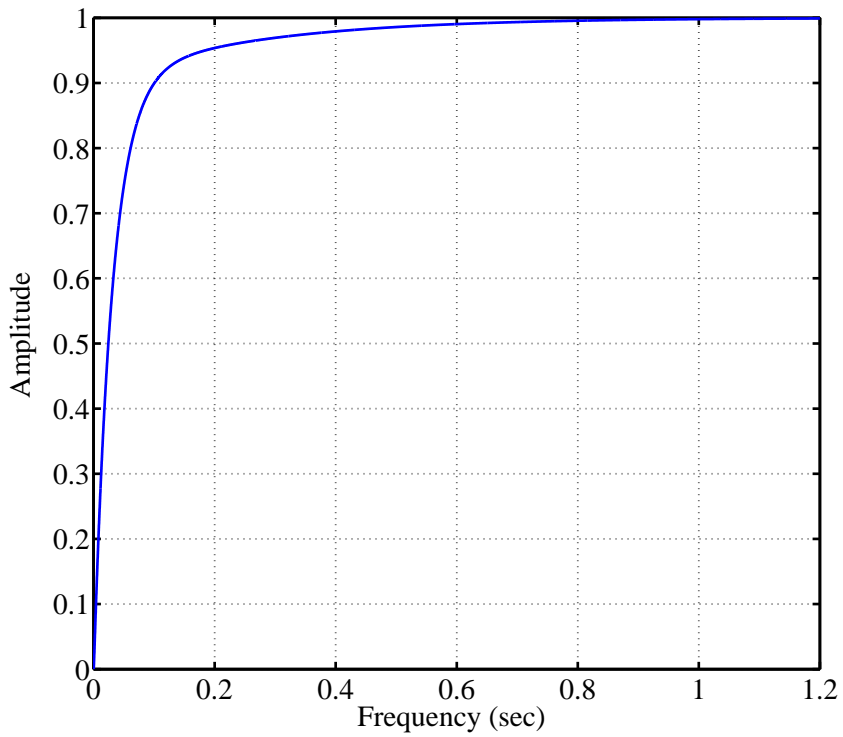
Figure D.3 depicts the transient response of the voltage-loop with a unity step input. The transient response characteristics of this overdamped system are listed below:

$$\begin{aligned} \text{Rise time, } t_r &= 100.5 \text{ ms } 0\text{-}90\% \\ \text{Settling time, } t_s \text{ } 2\% &= 441.3 \text{ ms} \end{aligned}$$

Figure D.4 depicts the impulse response of the voltage-loop.



**Figure D.2:** Detailed Frequency Response of  $C_V(s) \cdot G_V(s)$



**Figure D.3:** Voltage-Loop Step Response

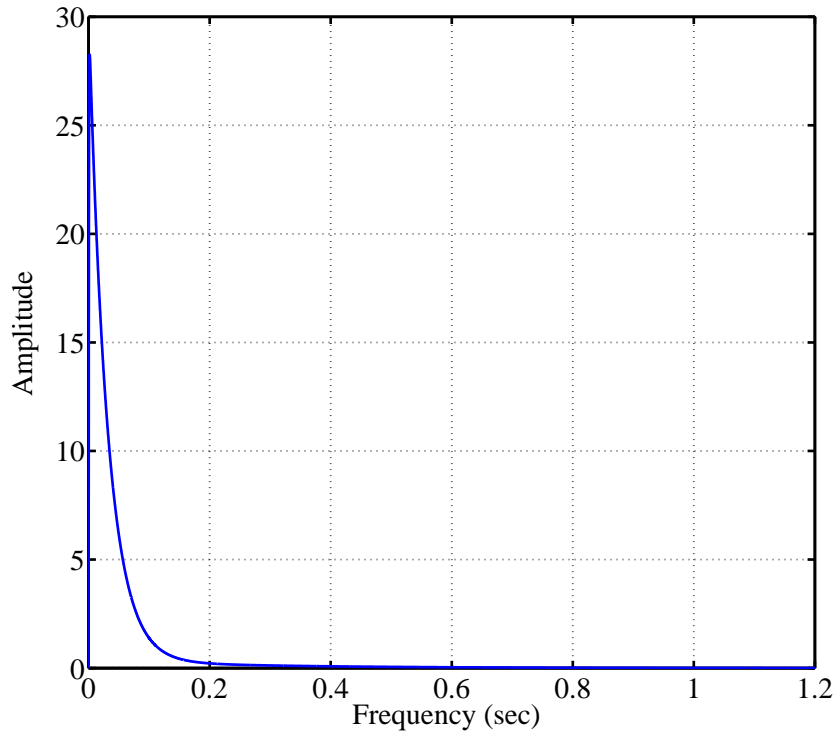


Figure D.4: Voltage-Loop Impulse Response

## D.2 Test Measurement Details

### D.2.1 Two-Phase Scaled SST Test Setup

The test setup, as depicted in Figure D.5, is aimed at verifying successful DC-DC control implementation as well as active output-current balancing with an output-parallel load.

The test-setup details are listed below:

- The control is jointly implemented on MCA, MCB, CCA and CCB, as discussed in Section 5.4 and 6.3. The AR voltage-loop constant references are set to 150 V each and the DC-DC voltage-loop constant reference is also set to 150 V.
- The input voltages,  $V_{acA}$  and  $V_{acB}$ , are received from a bench variac capable of supplying a 0-230 V line-neutral voltage.
- The inductors,  $L_A$  and  $L_B$ , both have a value of 5.8 mH.
- The inductor resistances,  $R_{LA}$  and  $R_{LB}$ , both represents two lumped resistor values. One is the actual inductor resistance and the second is an input resistor of 6  $\Omega$ . The input resistor is added for protection, to absorb power if an error occurs causing high current flow.
- The cell bus-capacitors,  $C_{cbA}$  and  $C_{cbB}$ , both have a value of 200  $\mu\text{F}$ .
- The output bus-capacitor,  $C_{ib}$ , has a value of 1650  $\mu\text{F}$ .
- The load resistor,  $R_O$ , has a value of 267  $\Omega$  or 110  $\Omega$ .



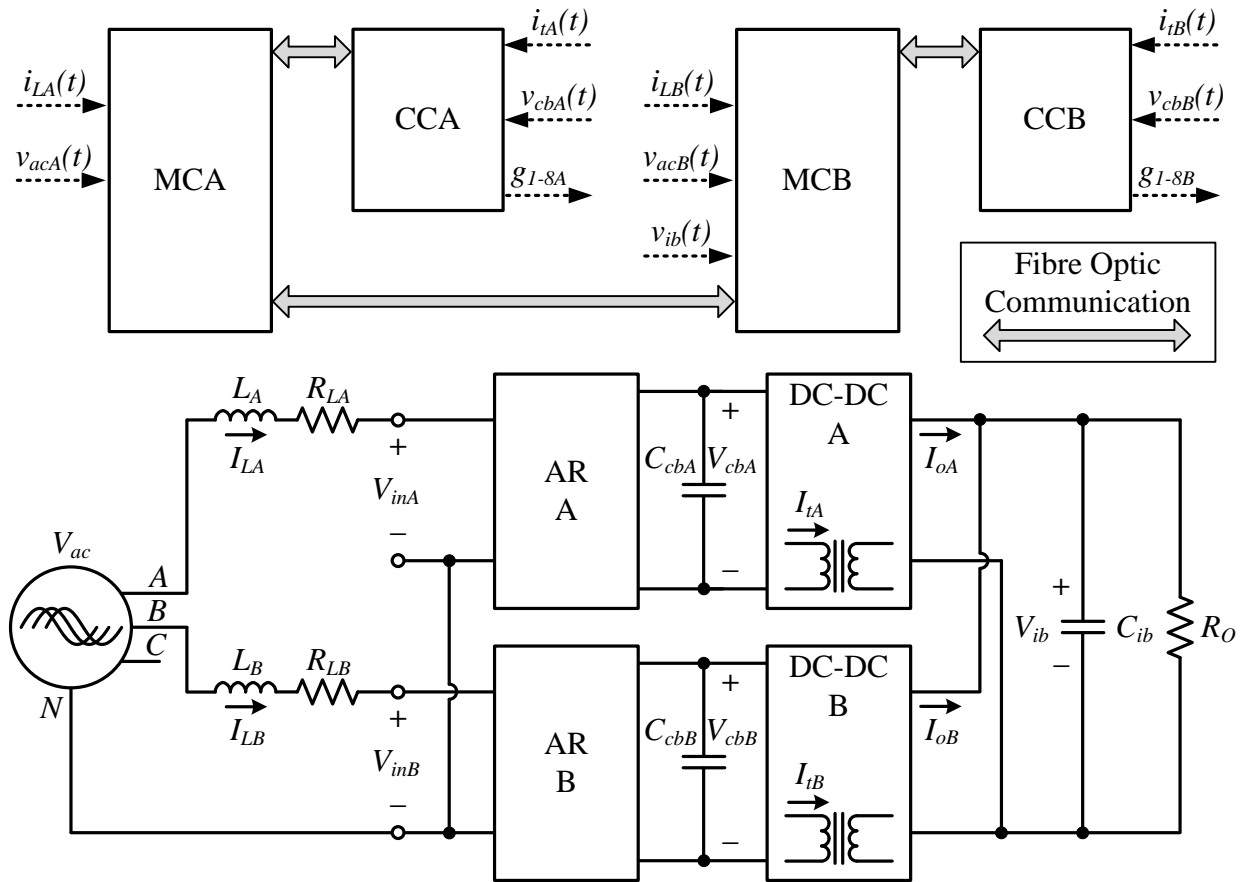


Figure D.5: Two-Phase SST Test Setup

### D.2.2 Single-Phase Full-Scale SST Test Setup

The test setup is similar to the setup depicted in Figure 6.2 with only one phase-stack in operation. The test is aimed at verifying successful full-scale SST operation at rated input-voltage as well as successful addition of the TPI and three-phase output load.

The test-setup details are listed below:

- The control is jointly implemented on the MC and twelve CCs as discussed in Section 5.4 and 6.3 . The AR voltage-loop constant reference is set to 6 kV and the DC-DC voltage-loop constant reference is set to 600 V.
- The input voltage,  $V_{ac}$  is received from a three-phase variac capable of supplying a 0-400 V line-line voltage. This voltage is stepped to a 0-6.6 kV line-line voltage, with a step-up transformer as depicted in Figure D.6
- The transformer leakage inductance is used as the input inductor,  $L$ , with a value in the range of 120 mH.
- The cell bus-capacitors,  $C_{acb} - C_{lcb}$ , each have a value of 200  $\mu$ F.
- The TPI bus-capacitor,  $C_{ib}$ , has a value of 14.1 mF.

- The load, including a load step, is set up as depicted in Figure D.7 with the following resistor values:

$$R_{ib} = 800\Omega$$

$$R_{o1} = 45\Omega$$

$$R_{o2} = 30\Omega$$

$$R_{o3} = 100\Omega$$

(D.2.1)

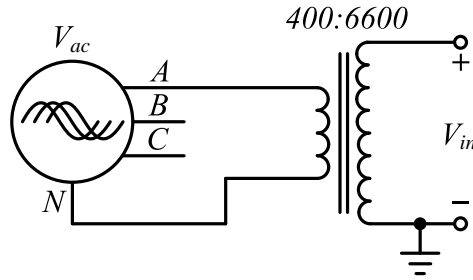


Figure D.6: Single-Phase Full-Scale SST Input-Voltage Setup

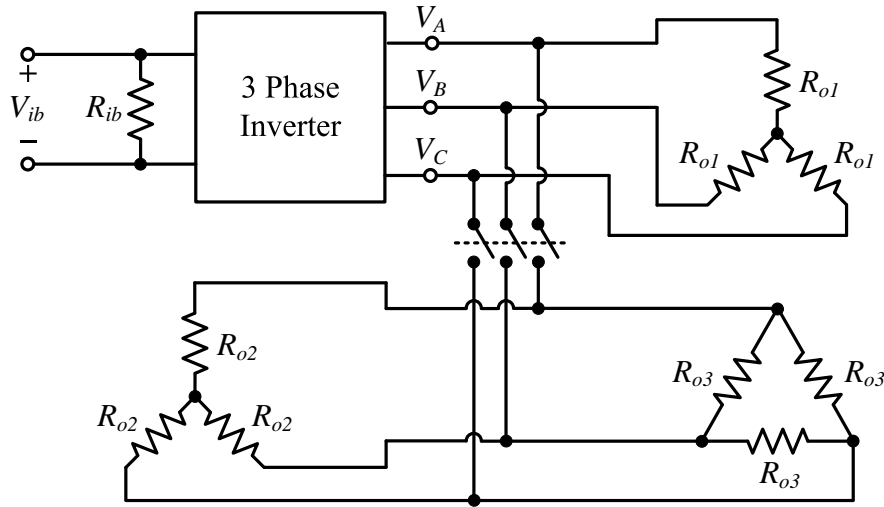


Figure D.7: Single-Phase Full-Scale SST Load Setup

### D.2.3 Three-Phase Full-Scale SST Test Setup

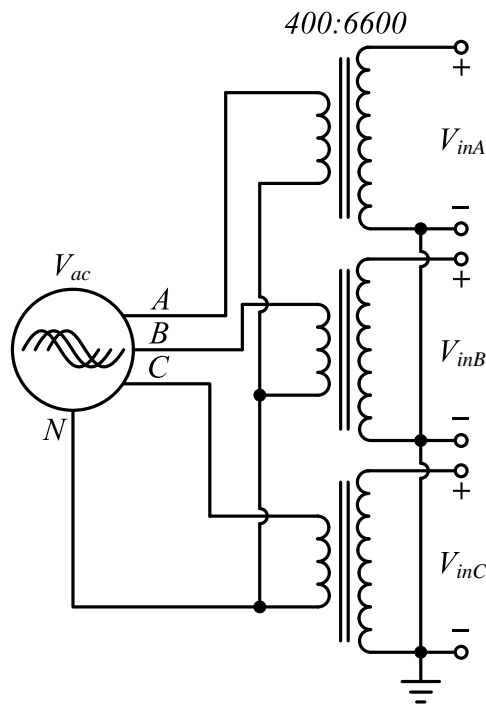
The test setup, as depicted in Figure 6.2, is aimed at verifying successful three-phase full-scale SST operation in terms of total cell bus-voltage balancing between phases as well as active output-current balancing.

The test-setup details are listed below:

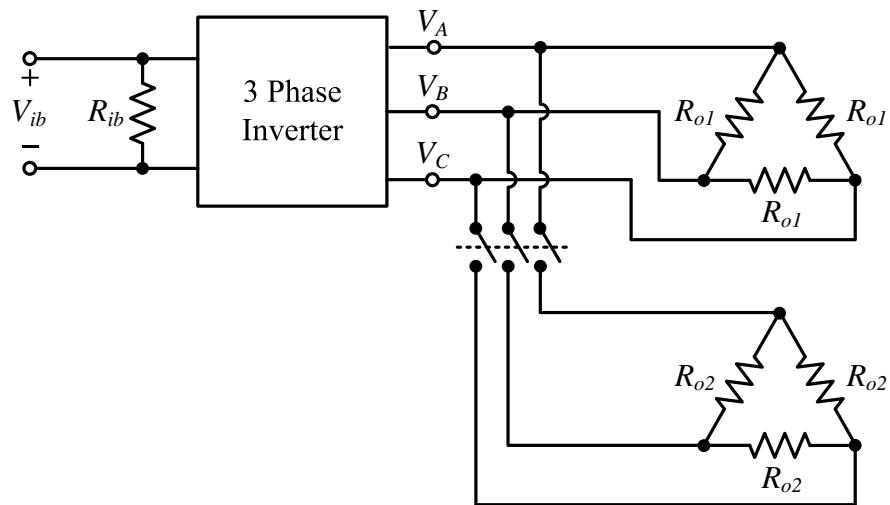
- The control is jointly implemented on MCA, MCB, MCC and 36 CCs as discussed in Section 5.4 and 6.3 . The AR voltage-loop constant references are set to 2.4 kV and the DC-DC voltage-loop constant reference is set to 200 V.

- The input voltages,  $V_{acA} - V_{acC}$  are received from a three-phase variac capable of supplying a 0-400 V line-line voltage. This voltage is stepped to a 0-6.6 kV line-line voltage, with three step-up transformer as depicted in Figure D.8
- The transformer leakage inductances are used as the input inductors,  $L_A - L_C$ , with values in the range of 120 mH.
- The cell bus-capacitors,  $(C_{acbA} - C_{lcbA}) - (C_{acbC} - C_{lcbC})$ , each have a value of  $200 \mu\text{F}$ .
- The TPI bus-capacitor,  $C_{ib}$ , has a value of 14.1 mF.
- The load, including a load step, is set up as depicted in Figure D.9 with the following resistor values:

$$\begin{aligned} R_{ib} &= 29\Omega \\ R_{o1} &= 20.8\Omega \\ R_{o2} &= 3.6\Omega \end{aligned} \tag{D.2.2}$$



**Figure D.8:** Three-Phase Full-Scale SST Input-Voltage Setup



**Figure D.9:** Three-Phase Full-Scale SST Load Setup

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