A BROADBAND MICROWAVE LIMITING AMPLIFIER

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Advisors

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DECLARATION

"I, the undersigned, hereby declare that the work contained in this thesis is my own original work and that I have not previously, in its entirety or in part, submitted it at any university for a degree."

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M. Neethling Date

SYNOPSIS

Limiting amplifiers are employed in electronic warfare (EW) systems requiring a high measure of amplitude control. These EW systems employ sensitive signal processing components that are unable to accept the full dynamic range of input signals the system must face. The limiting amplifier, however, offers the unique capability of reducing the received signal spectrum to a suitable dynamic range. A typical application of the limiting amplifier is in the instantaneous frequency measurement (IFM) receiver where the limiting amplifier allows the receiver to accurately measure pulsed signals over a wide input dynamic range

The aim of this study is the design and analysis of a broadband limiting amplifier. Focus is placed on the design of a so-called *backbone* limiting amplifier (BLA) which forms an integral part of a proposed modular design approach for realizing a design with improved input dynamic range. A designed BLA is discussed in this thesis while insight is given as to the intricacies associated with its mechanism of operation. Over its 45 dB (- 40 to + 5 dBm) input dynamic range, the designed 2-18 GHz limiting amplifier offers a typical saturated output power of 7.5 dBm while harmonic suppression of better than 8.6 dBc is achieved.

The BLA design was based on an existing limiting amplifier design, the so-called *baseline* limiting amplifier, employing alternating amplifiers and attenuators. Evaluation of the *baseline* limiting amplifier design allowed for formulation of a design hypothesis for realizing the BLA design. Physical measurements on the BLA were then used to scrutinize and validate the formulated design hypothesis.

The requirements for realizing the BLA design were the establishment of a thorough radio frequency (RF) amplifier design capability, an understanding of the nonlinear phenomena associated with the RF amplifier and the utilization and control thereof within the limiting amplifier. Different RF amplifier designs that were carried out are discussed in this thesis, while it is shown how they were used to further investigate important design considerations for application in the BLA design. The computer-aided design packages namely *MultiMatch* and *Microwave Office* (MWO) were successfully used in realizing the desired broadband RF amplifier designs and the eventual BLA design.

OPSOMMING

Beperker versterkers word gebruik in elektroniese oorlogvoering (EO) stelsels waar ’n redelike mate van amplitude beheer noodsaaklik is. Sensitiewe seinverwerking komponente, wat nie die volle dinamiese bereik van intreeseine kan hanteer nie, maak deel uit van hierdie EO stelsels. Die beperker versterker bied egter die unieke eienskap om die ontvangde seinspektra te reduseer tot ’n gepaste dinamiese bereik. ’n Tipiese toepassing vir die beperker versterker is as deel van die oombliks-frekwensie-meting ontvanger waar die beperker versterker die ontvanger toelaat om akkurate meting van gepulsde seine te doen oor ’n wye intree dinamiese bereik.

Die doel van hierdie studie is die ontwerp en analise van ’n wye-band beperker versterker. Fokus word geplaas op die ontwerp van ’n sogenaamde *kruks* beperker versterker wat ’n integrale deel uitmaak van ’n voorgestelde modulêre ontwerpsbenadering, wat ten doel het om ’n verbeterde intree dinamiese bereik daar te stel. Oor die 45 dB (- 40 tot + 5 dBm) intree dinamiese bereik, bied die ontwerpte 2-18 GHz beperker versterker ’n tipiese versadigde uittreedrywing van 7.5 dBm terwyl harmonieke onderdrukking van beter as 8.6 dBc verkry is. Die ontwerp van hierdie komponent word in hierdie tesis bespreek terwyl belangrike aspekte oor die werking daarvan uitgelig word.

Die ontwerp van die *kruks* beperker versterker is gebaseer op ’n bestaande beperker versterker ontwerp, of sogenaamde *basis* ontwerp, wat gebruik maak van afwisselende versterkers en attenuators. Evaluering van die *basis* ontwerp het toegelaat vir die formulering van 'n ontwerpshipotese om die *kruks* beperker versterker te realiseer. Fisiese metings op die *kruks* beperker versterker is gebruik om die ontwerpshipotese krities te evalueer.

Om die *kruks* beperker versterker te realiseer moes die nodige RF versterker ontwerpsvaardigheid daargestel word, ’n begrip vir die nie-liniêere verskynsels in die RF versterker en die gebruik en beheer daarvan in die beperker versterker moes daargestel word. Verskeie RF versterkers wat ontwerp is word in hierdie tesis bespreek, terwyl getoon word hoe hierdie ontwerpe gebruik is om belangrike ontwerpsaspekte te ondersoek wat uiteindelik toegepas is in die *kruks* beperker versterker ontwerp. Die ontwerpspakkette naamlik *MultiMatch* en *Microwave Office* is suksesvol gebruik vir die realisering van die nodige wye-band RF versterkers en die uiteindelike *kruks* beperker versterker ontwerp.

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To my wife, Christelle

GLOSSARY

AC	Alternating Current
AM	Amplitude Modulation
BLA	*Backbone* Limiting Amplifier
BPL	Bandpass Limiter
CAD	Computer-Aided Design
CW	Continuous Wave
DC	Direct Current
DF	Direction Finding
DRE	Dynamic Range Extension
DUT	Device Under Test
ELINT	Electronic Intelligence
EM	Electromagnetic
ESM	Electronic Support Measures
EW	Electronic Warfare
FET	Field Effect Transistor
HB	Harmonic Balance
HPOI	High Probability of Intercept
IFM	Instantaneous Frequency Measurement
IL	Insertion Loss
IM	Intermodulation
JFET	Junction Field Effect Transistor
LNA	Low-Noise Amplifier
MAG	Maximum Available Gain

MDS	Minimum Detectable Signal
MIC	Monolithic Integrated Circuit
MWO	Microwave Office
NF	Noise Figure
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PM	Phase Modulation
RF	Radio Frequency
RL	Return Loss
RWR	Radar Warning Receiver
SCM	Simultaneous Conjugate Match
SHS	Second Harmonic Suppression
SNA	Scalar Network Analyzer
TCA	Temperature Coefficient of Attenuation
TEM	Transverse Electromagnetic
THS	Third Harmonic Suppression
TVA	Temperature Variable Attenuator
VNA	Vector Network Analyzer
VPF	Voltage Parallel Feedback
VSWR	Voltage Standing Wave Ratio
VVA	Voltage Variable Attenuator

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INTRODUCTION

In modern day electronic warfare (EW), rapid identification of radar pulses and response to the associated weapon systems will be aided if the associated weapon systems can be encoded from critical parameters. Data such as direction of arrival, frequency of the radio frequency (RF) carrier, amplitude, pulse width and time of arrival of each detected pulse are vital requirements for advanced counter measure systems.

The limiting amplifier is a device used primarily in conjunction with instantaneous frequency measurement (IFM) receivers which form part of the EW suite of most new generation fighter aircraft. The IFM does *instantaneous* frequency measurement on threat radar signals to enable electronic support measures (ESM) such as jamming. At the heart of the IFM receiver's frequency measurement mechanism is a digital frequency discriminator that is unable to accept the broad input power range presented by a typical dense signal environment. The limiting amplifier used on the IFM front-end, limits this broad input power range to a specific output power window, required for optimal operation of the receiver.

Furthermore, the IFM gives accurate frequency information typically when only one signal is present on its input and may generate erroneous frequency information in response to simultaneous signals. With adequate suppression of an undesired signal, the IFM will, however, retain measurement accuracy, when simultaneous signals are present. The limiting amplifier's *capturing effect* aids in this requirement by suppressing the weaker of two signals.

Chapter 1 of this thesis provides the reader with the key features of a limiting amplifier and deals with the limiting amplifier's *capturing effect* which proves essential for the intended use on the front-end of an IFM receiver. A limiting amplifier implementing an alternating attenuator-amplifier configuration is proposed, opposed to the more commonly known alternating limiter-amplifier approach. The attenuator-amplifier approach, although very complex, offers one the opportunity to deal with, and understand, the nonlinear effects of the RF amplifiers used within the limiting amplifier RF chain.

Compared to the design of other microwave components, limiting amplifier designs, especially over the 2-18 GHz frequency band, is a topic rather limited in discussion. Fortunately, an existing limiting amplifier design complying with certain set specifications could be used as reference for an intended design. This *baseline* limiting amplifier, implementing an alternating attenuator-amplifier configuration is discussed in Chapter 2 to establish an intuitive feel for the requirements of a final design.

Chapter 3 deals with the RF amplifier and considerations that had to be taken into account for doing the final limiting amplifier design. It was seen that before attempting a limiting amplifier design, a proper RF amplifier design capability was crucial. Initial designs were rather limited in terms of bandwidth, but offered the necessary experience in working with the design packages namely *MultiMatch* and *Microwave Office* (MWO). It was shown that these two packages, used in conjunction with each other, offered a powerful amplifier design and analysis tool. This tool was exploited as best possible to eventually produce two amplifiers that could be implemented successfully in the final limiting amplifier design. With successful amplifier designs in place, the stage was set for the evaluation of the nonlinear behaviour of the RF amplifier.

Chapter 4 discusses the nonlinear RF amplifier with specific reference to its associated nonlinear phenomena and the techniques used for analyzing them. The nonlinear device models of the field effect transistors (FETs) used in RF amplifier

designs are evaluated and it is shown to what extent nonlinear analysis can be done, in MWO. Nonlinear analysis was taken a step further by reconstruction of an existing design, confirming that it gave a true representation of actual device performance and eventually optimizing it for some desired response for use in the final limiting amplifier design.

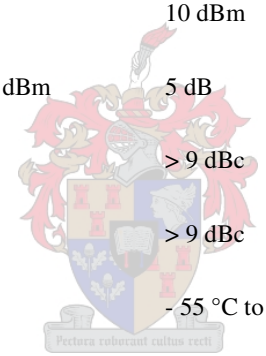
With the acquired design experience and theoretical background in place, a design hypothesis as based on the existing *baseline* limiting amplifier was formulated in Chapter 5. The formulated design hypothesis was tested by evaluating a design implemented in MWO. The nonlinear analysis of this design showed to which extent a limiting amplifier design was possible after some optimization. Pleasing, as the simulated results may be, the true test, however, would be in building and testing the design.

Chapter 6 deals with the tests performed on the designed limiting amplifier while giving an estimation of how accurately the simulated design could be implemented. The mastering of a broadband limiting amplifier design is validated in this chapter while it is shown how it succeeded in dealing with the difficulties associated with the design. In conclusion, Chapter 7 summarizes the achievements leading up to the final limiting amplifier design, while a critical review of the designed limiting amplifier is given. The design of a linear amplifier opposed to the design of a limiting amplifier is discussed while suggestions as to fields of further study are offered.

LIMITING AMPLIFIER SPECIFICATIONS

With the aim of designing a fully functional limiting amplifier, some design specifications have to be laid down. The shown specifications were taken from an existing limiting amplifier or the so-called *baseline* limiting amplifier and are therefore requirement specific. The following specifications will be used as reference for performance evaluation of the final limiting amplifier design that was done for purposes of this study:

Frequency Range	2-18 GHz
Input Return Loss @ P_{in} = - 20 dBm	7.36 dB
Input Dynamic Range	- 50 to + 5 dBm
Minimum Output Power @ P_{in} = - 50 dBm	10 dBm
Minimum Output Power @ P_{in} = + 5 dBm	10 dBm
Maximum Output Power Window @ P_{in} = + 5 dBm	5 dB
Harmonic Suppression @ P_{in} = - 50 dBm	> 9 dBc
Harmonic Suppression @ P_{in} = + 5 dBm	> 9 dBc
Operating Temperature Range	- 55 °C to + 85 °C



The shown specifications are typical of a limiting amplifier covering the 2-18 GHz frequency bandwidth and with the input dynamic range in question. Meeting the shown specifications is no mean feat and is complicated by the broad frequency bandwidth, the broad input dynamic range, the limiting amplifier's associated nonlinear phenomena and associated temperature effects. Few manufacturers succeed in producing limiting amplifiers with similar specifications; a fact that tends to show the complexity and intricacy associated with the design of this device. In this thesis, however, it will be shown how the design of a broadband limiting amplifier was mastered after thorough theoretical and practical research methodology.

CHAPTER 1

THE LIMITING AMPLIFIER

1.1 INTRODUCTION

Figure 1.1 offers a very basic, but insightful description of limiting amplifier operation. It is seen that, unlike a linear amplifier, the limiting amplifier provides a constant output signal level, independent of the input signal level presented to it over its input dynamic range. In general, this would mean that amplitude information on a pulsed input signal will be lost. The input dynamic range referred to, is the range of input powers for which the saturated output power is maintained within a specified power window, whilst ensuring desired harmonic and spurious suppression.

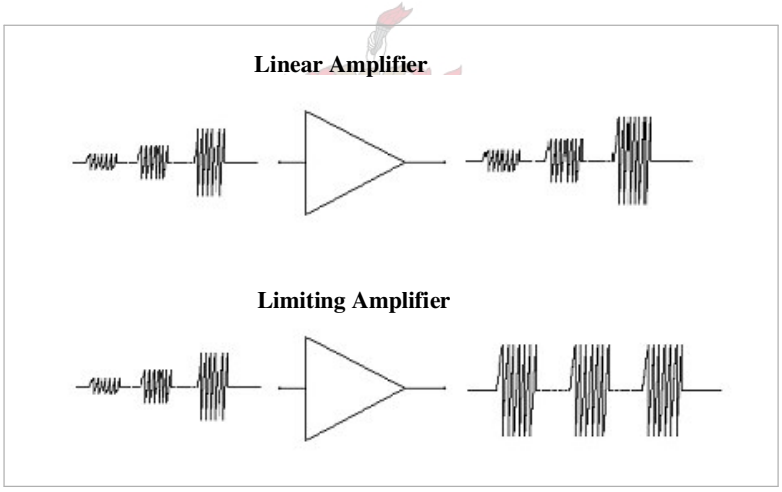


Figure 1.1: Graphical description of limiting amplifier operation

The ideal transfer characteristic of a limiting amplifier is shown in Figure 1.2. With the input signal below the shown threshold level, the limiting amplifier will function as a linear amplifier. However, when the input threshold is exceeded, the limiting amplifier enters a nonlinear operating region where its output power (saturated) is limited ideally to a constant level [1]. Correct operation of the limiting amplifier will require it to be operated exclusively in this nonlinear region. Not only is the objective to characterize the device's associated nonlinear behaviour, but also to exploit it for realizing a functional limiting amplifier.

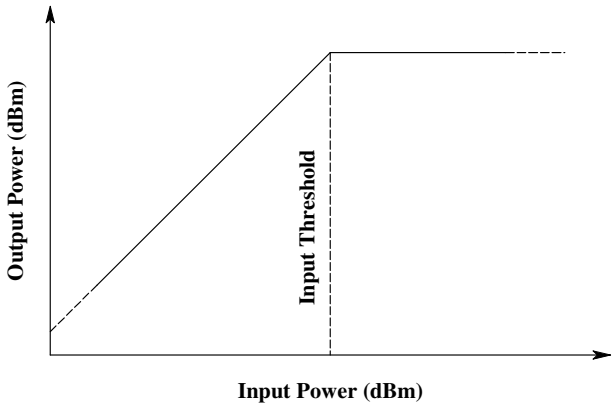


Figure 1.2: Transfer characteristic of an ideal limiting amplifier

A practical limiting amplifier does not have the shown abrupt transition between the linear and nonlinear regions of operation as seen in Figure 1.2, but rather, has a smooth transition. The transfer characteristic of such a practical limiting amplifier is shown in Figure 1.3.

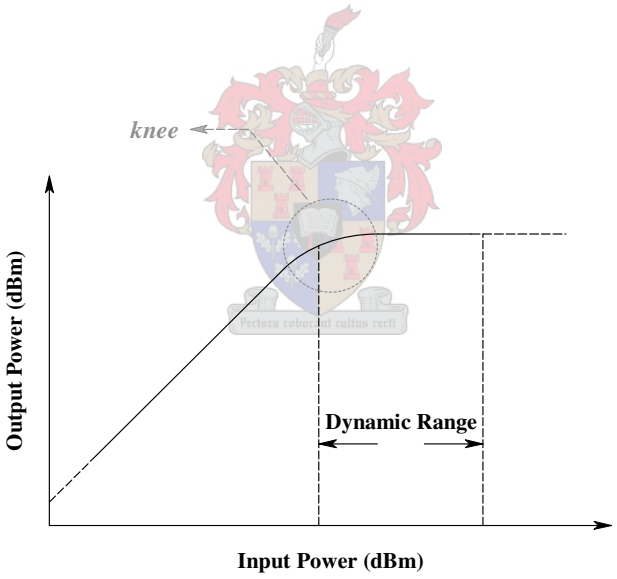


Figure 1.3: Transfer characteristic of a practical limiting amplifier

An input signal of minimum strength should at least reach the *knee* of the limiting amplifier transfer characteristic as shown in Figure 1.3, while stronger signals will be limited to a constant output level. The characteristics of the *knee* will be shown to be very much dependent on the compression characteristics of the last stage amplifier in a proposed limiting amplifier RF chain.

A linear amplifier, as opposed to the limiting amplifier, is so defined because its output power is directly proportional to its input power whilst operated within its dynamic range. The low end of the amplifier's dynamic range is determined by the noise floor and the amplifier noise figure, which places the limit on the lowest level signal to be amplified. The high end of

the dynamic range is defined as the point where saturation of the output starts. A quantitative measure of the onset of saturation is given by the 1 dB compression point, which is defined as the input power for which the output power is saturated 1 dB below that expected from an ideal amplifier [2]. The typical response of a linear amplifier, with its associated nonlinear characteristics, is shown in Figure 1.4.

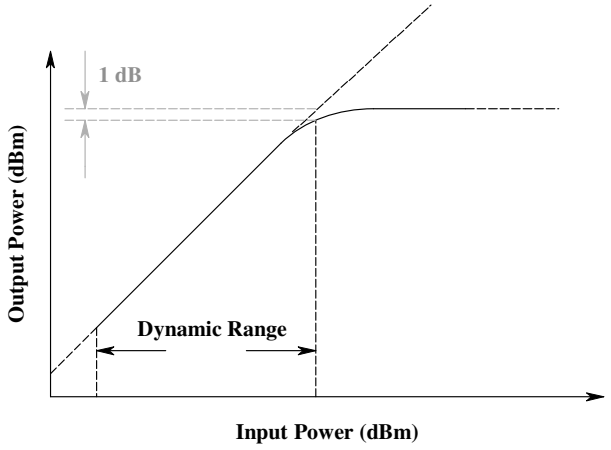


Figure 1.4: Typical linear amplifier response

A linear amplifier is very seldom used outside of its dynamic range. Proper low-noise amplifier design can extend the amplifier's dynamic range by decreasing its noise figure, but little can be done about the limit set by the noise floor. The important question that needs to be asked is, "What about operation, after the onset of saturation?" This may prove to be a very important question to answer since the key to designing a limiting amplifier may lie in the operation of a *linear* amplifier at input powers larger than its 1 dB compression point.

1.2 THE IFM RECEIVER

1.2.1 BASIC PRINCIPLE OF OPERATION

The ability to instantaneously measure the frequency of intercepted threat signals is a necessity in modern day electronic warfare (EW) systems. Accurate instantaneous frequency measurement is done by the high probability of intercept (HPOI), instantaneous frequency measurement (IFM) receiver. Although this receiver does not measure frequency instantaneously, its time response is a small fraction of practical radar pulse widths, so effectively it is instantaneous. An IFM's basic frequency measurement technique consists of comparing the phase delay of a signal propagating down delay lines of known length. The receiver's complex mechanism of ambiguity resolving is not discussed, while focus is rather placed on its basic principle of operation. The relation between phase delay and frequency is derived hereafter to show how frequency information can be extracted.

The expression for the phase delay over a delay line of known length is given by:

$$\theta = \beta L \tag{1.1}$$

where β is the propagation constant and L is the length of the delay line in question. Using the expression for β in terms of the signal wavelength λ gives:

$$\beta = \frac{2\pi}{\lambda} \tag{1.2}$$

where λ can be expressed as follows:

$$\lambda = \frac{v}{f} \tag{1.3}$$

v is the velocity of propagation and f is the signal frequency. Substituting equation (1.3) into equation (1.2), yields the following expression for the propagation constant:

$$\beta = \frac{2\pi f}{v} \tag{1.4}$$

Using the new expression for β in equation (1.1) yields:

$$\theta = \frac{2\pi f L}{v} = kf \tag{1.5}$$

where $k = \frac{2\pi L}{v}$

Equation (1.5) shows a direct dependence of phase delay on frequency. With the constant k known, the frequency of the input signal can be determined by the IFM, by calculating the phase delay θ and substituting its value into equation (1.5). With the IFM's basic mechanism of frequency measurement discussed, one may proceed to evaluating the role of the limiting amplifier as part of this receiver.

1.2.2 THE LIMITING AMPLIFIER AS PART OF AN IFM RECEIVER

In conventional IFM receiver design, a limiting amplifier is used in front of the IFM subsystem, to compress the wide input dynamic range to a more manageable output range. Not only will the limiting amplifier improve sensitivity by providing high-gain radio frequency (RF) amplification but it will also eliminate the effect of input signal amplitude on phase correlator outputs [3]. The IFM receiver uses these phase correlators to obtain the correlation of different lags of the input signal to measure its frequency.

The IFM guarantees accurate frequency measurement when only one signal is present on its input. With simultaneous input signals present, some major deficiencies of the IFM manifest themselves. The IFM receiver is not able to measure simultaneous input signals and may generate erroneous frequency reports, especially when they have comparable power levels. With simultaneous input signals present, adequate suppression of the undesired signal is usually required to ensure

that the IFM retains measurement accuracy. The limiting amplifier's *capturing effect* aids in this requirement. The *capturing effect*, which refers to the suppression of a weaker signal with respect to a stronger signal, is displayed when simultaneous signals are present at the limiting amplifier's input [1]. Figure 1.5 shows a more graphical explanation of the *capturing effect* offered by the limiting amplifier (LA).

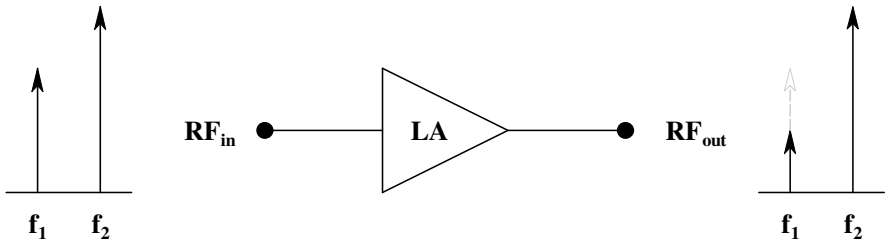


Figure 1.5: The limiting amplifier capturing effect

The *capturing effect* ensures that the relative suppression of the weaker signal (i.e. the undesired signal) is more pronounced at the limiting amplifier's output. With this unwanted signal suppressed, the IFM will process the high level signal for accurate instantaneous frequency measurement.

1.3 THE CLASSIC HARD LIMITER SUPPRESSION EFFECT

A general nonlinear amplifier, such as the limiting amplifier, can be represented by a nonlinearity followed by a bandpass filter whose passband, by definition, stops short of any harmonics of the input frequencies. The nonlinearity, often referred to as a hard-limiter, is assumed to be memoryless and contains only odd harmonic products [1].

The combination of such a hard-limiter and a bandpass filter is called a bandpass limiter (BPL) which displays the typical *capturing effect* mentioned earlier [4]. A mathematical expression for the output of a BPL can be derived by assuming that the input to the BPL is given by:

$$x(t) = A_{desired}\cos(2\pi f_1 t) + A_{undesired}\cos(2\pi f_2 t) \tag{1.6}$$

$x(t)$ is a typical input combination of a desired high-level signal and an undesired low-level signal. For the sake of illustration, $A_{desired}$ is set to 1 V and the weak signal amplitude, $A_{undesired}$ is set to 0.3 V. This establishes a high signal level to low signal level ratio of:

$$Ratio(dB) = 20\log\left(\frac{1}{0.3}\right) \approx 10.5\ dB \tag{1.7}$$

Figure 1.6 shows the input to the BPL in both the frequency and the time domain.

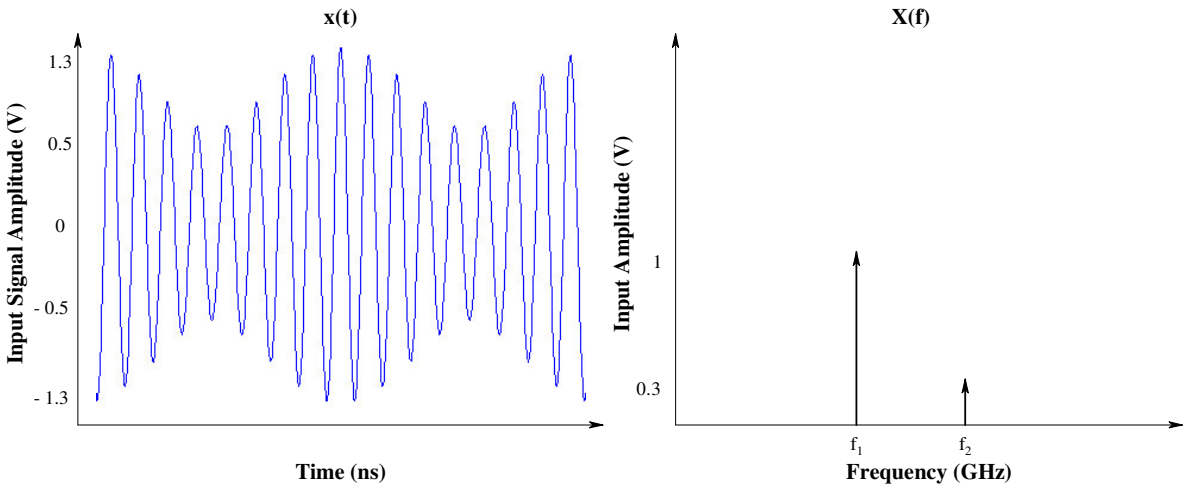


Figure 1.6: Input of the BPL in both time and frequency domain

A close approximation for the BPL output, derived in Appendix A, is given by:

$$r(t) = \cos(2\pi f_1 t) + \frac{A_{undesired}}{2}\cos[2\pi f_2 t] - \frac{A_{undesired}}{2}\cos[2\pi(2f_1 - f_2)t] \tag{1.8}$$

From expression (1.8) it can be seen that the amplitude of the original low-level signal has been halved to 0.15 V and a new component with amplitude also 0.15 V, at frequency $2f_1 - f_2$ has been generated.

A new high signal level to low signal level ratio of:

$$Ratio(dB) = 20\log\left(\frac{1}{0.15}\right) \approx 16.5\ dB \tag{1.9}$$

is now observed.

The classical hard-limiter suppression effect or rather *capturing effect* is evident from the 6 dB difference between expressions (1.7) and (1.9).

The BPL output, in both frequency and time domain, is shown in Figure 1.7.

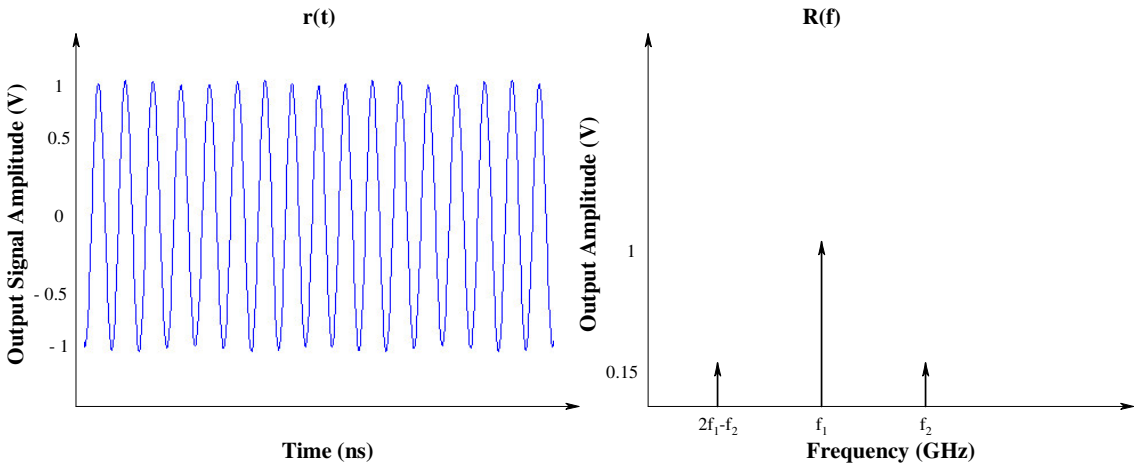


Figure 1.7: Output of the BPL in both time and frequency domain

From Figure 1.7 it can be seen that the *capturing effect* has removed the influence of the low-level signal from the BPL's output. The relative suppression of the low-level signal (not yet suppressed at the input) with respect to the high-level signal on the BPL's input is thus increased at the BPL's output. Should this suppression effect be practically realizable in a linear amplifier driven into saturation, one may very well have a very important building block for a limiting amplifier. The question that needs to be answered is how well defined the so-called *capturing effect* is in a practical amplifier. To find the answer to this question, a more thorough evaluation of this capturing - or small-signal suppression effect, will be done in chapters to follow.

1.4 DIFFERENT LIMITING AMPLIFIER CONFIGURATIONS

1.4.1 LIMITER-AMPLIFIER CONFIGURATION

Most limiting amplifier architectures employ alternating limiters and gain stages as shown in Figure 1.8. Alternative configurations may have interchanged limiters and amplifiers [7]. The function of the limiters is to restrict signal levels such that the gain stages are operated in their linear region [8]. The limiter stages are interspersed through-out the amplifier chain to ensure that harmonic power build-up is prevented [39]. The limiter and amplifier circuitry is designed to suppress the creation of second (and other even-order) harmonics while third (and higher odd-order) harmonics can be controlled by the passband characteristics of the circuitry when applicable.

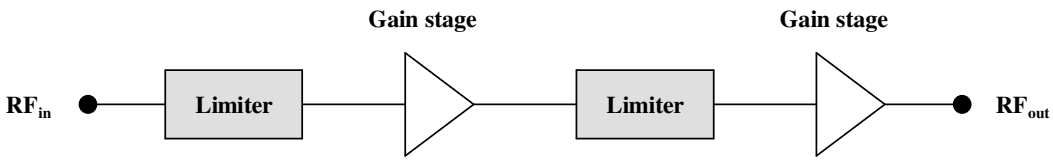


Figure 1.8: Limiting amplifier architecture employing limiters

1.4.1.1 LIMITER OPERATION

The purpose of a limiter is to limit the power in a signal to a level that can be tolerated by the component following it. An ideal limiter has no attenuation when low power is incident upon it, but at some threshold has an attenuation that increases with increasing power to maintain a constant output power. In terms of application in a limiting amplifier, this property is very significant. When operated at the low end of the limiting amplifier's input dynamic range there will be high enough gain to drive the last amplifier stage into compression. The effect of the limiters in this case will be insignificant. At the high end of the input dynamic range, however, the attenuation that the limiters introduce, reduces the effective available gain in the limiting amplifier RF chain. The limiters will thus prevent unwanted overdrive of amplifiers and the occurrence of undesired nonlinear effects associated with the RF amplifier.

The very basic form of a limiter, which incorporates an anti-parallel diode pair, is shown in Figure 1.9. Figure 1.10 shows the expected symmetrical clipped output of this limiter. When non-linear two-terminal circuit elements such as diodes are connected as shown, a certain degree of harmonic suppression may be achieved [9]. The discussion to follow explains this significant property more clearly.

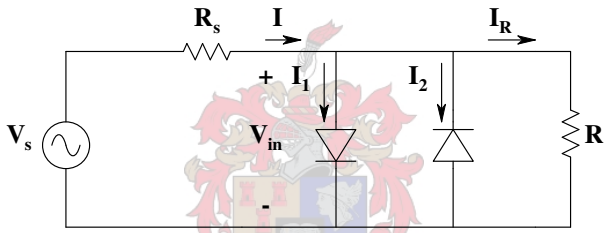


Figure 1.9: Anti-parallel connection of two non-linear devices

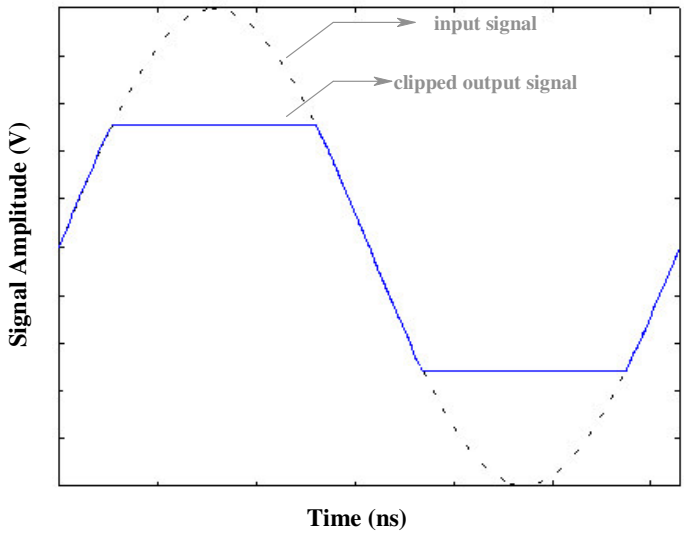


Figure 1.10: Symmetrical clipping in an anti-parallel diode pair

The nonlinear behaviour of the diodes can be illustrated when the diode current is expressed as a third order polynomial.

The current in the first diode is therefore expressed as:

$$I_1 = a_1 V_{in} + a_2 V_{in}^{\ 2} + a_3 V_{in}^{\ 3} \tag{1.10}$$

with the higher order terms of the nonlinear device ignored. With the second diode reversed and the voltage and current conventions remaining the same, the current in the second diode can be written as:

$$I_2 = a_1 V_{in} - a_2 V_{in}^{\ 2} + a_3 V_{in}^{\ 3} \tag{1.11}$$

The total current can be written as:

$$I = I_1 + I_2 + I_R \tag{1.12}$$

Substituting equations (1.10) and (1.11) into equation (1.12) gives:

$$I = 2a_1 V_{in} + 2a_3 V_{in}^{\ 3} + I_R \tag{1.13}$$

or

$$I = 2a_1 V_{in} + 2a_3 V_{in}^{\ 3} + \frac{V_{in}}{R} = kV_{in} + 2a_3 V_{in}^{\ 3} \tag{1.14}$$

where k is a constant.

Equation (1.14) shows that the external current does not include any even-order components. The even-order current components shown in equations (1.10) and (1.11) circulate in the inner loop between the two diodes. Only the odd-order current components therefore circulate in the external loop with even-order harmonics suppressed.

1.4.1.2 SYMMETRICAL VERSUS ASYMMETRICAL CLIPPING

In the previous section it was shown that the anti-parallel diode limiter clips the RF waveform symmetrically, resulting in even-order harmonic suppression. A single diode clipper, shown in Figure 1.11, will cause asymmetrical clipping as seen in Figure 1.12.

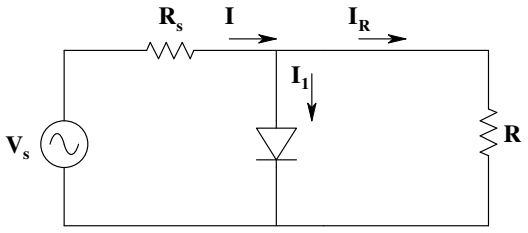


Figure 1.11: Single diode clipper

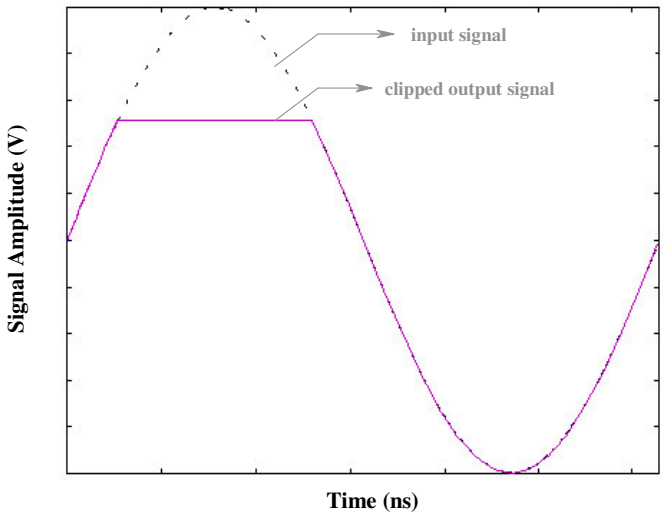


Figure 1.12: Asymmetrical clipping

The current in the diode is given by:

$$I_1 = a_1 V_{in} + a_2 V_{in}^{\ 2} + a_3 V_{in}^{\ 3} \tag{1.15}$$

with higher order terms of the non-linear device ignored.

The total current can be written as:

$$I = I_1 + I_R \tag{1.16}$$

Substituting equation (1.15) into equation (1.16) gives:

$$I = a_1 V_{in} + a_2 V_{in}^{\ 2} + a_3 V_{in}^{\ 3} + I_R \tag{1.17}$$

or

$$I = a_1 V_{in} + a_2 V_{in}^{\ 2} + a_3 V_{in}^{\ 3} + \frac{V_{in}}{R} = k V_{in} + a_2 V_{in}^{\ 2} + a_3 V_{in}^{\ 3} \tag{1.18}$$

where k is a constant.

From expression (1.18) it is clear that both even- and odd-order current components are included in the output spectrum, unlike the anti-parallel diode pair that included only even-order components. Should clipping thus occur in an RF waveform, it is desirable to have symmetrical clipping in order to reduce harmonic generation. The same reasoning will also apply to an amplifier driven into saturation. The extent to which clipping occurs and how symmetrical signal clipping can be guaranteed will, therefore, be an important design consideration.

1.4.1.3 DESIGN APPROACH OF LIMITER-AMPLIFIER CONFIGURATION

The discussion to follow, serves to establish a better intuitive feel of the significance of the limiters in a limiter-amplifier design configuration.

The relative second harmonic suppression of an amplifier driven heavily into saturation, as derived from Figure 1.13, can be expressed as:

$$R_{2\_amplifier} = P_{sat} - P_2 \tag{1.19}$$

with P_{sat} the saturated output power of the amplifier and P_2 the second harmonic output power level.

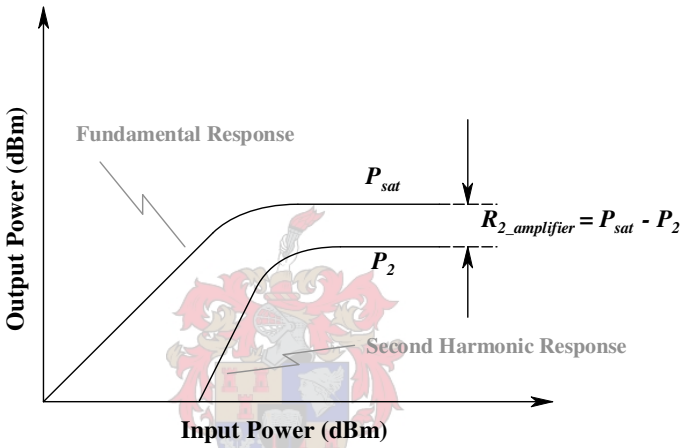


Figure 1.13: Second harmonic response of amplifier

Ideally, the second harmonic suppression should be as high as possible. This is, however, not the case for the heavily saturated amplifier, as seen in Figure 1.13.

To improve on this harmonic suppression, a limiter-amplifier chain configuration can be used. Figure 1.14 depicts the situation where a limiter is followed by an amplifier stage [8]. The limiter is saturated to an output power level of P_L while the amplifier stage is operated in its linear region. Assuming that symmetrical clipping occurs in the limiter, it can be accepted that the second harmonic contribution of the limiter will be much less than that of the amplifier stage.

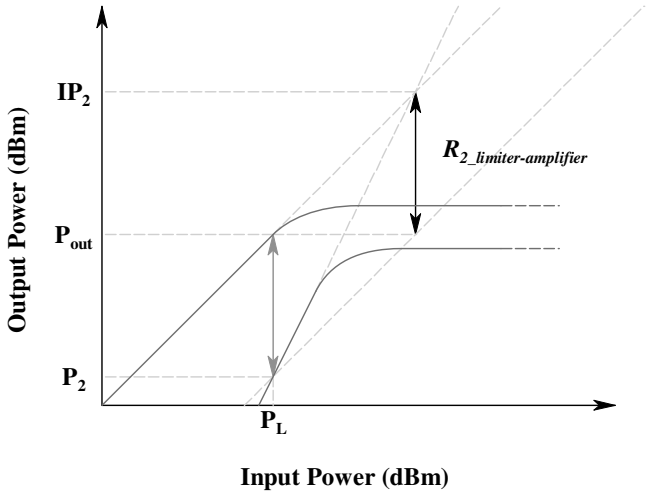


Figure 1.14: Second harmonic response of limiter-amplifier configuration

A new expression for the relative second harmonic suppression can be derived from Figure 1.14 as:

$$R_{2\_limiter\text{-}amplifier} = P_{out} - P_2 \tag{1.20}$$

P_{out} in expression (1.20) is the fundamental output power level of the amplifier when driven with input power P_L, while P_2 is the resulting second harmonic output power level.

From Figure 1.14, expression (1.20) can be written as:

$$R_{2\_limiter\text{-}amplifier} = IP_2 - P_{out} \tag{1.21}$$

or alternatively as:

$$R_{2\_limiter\text{-}amplifier} = IP_2 - (G+P_L) \tag{1.22}$$

where G is the gain of the amplifier and IP_2 is the second order intercept point.

From expression (1.22) it is apparent that the relative second harmonic suppression is a function of the limiter output power level P_L, the amplifier gain G, and the amplifier intercept point IP_2.

Comparing Figures 1.13 and 1.14, one can see a definite improvement in second harmonic suppression when the limiter-amplifier approach is followed. Another potential advantage of the limiter-amplifier approach is that the second harmonic suppression may be more readily predicted and more consistently controlled during manufacturing. With the limiter implemented, one may also expect improved small-signal suppression. Furthermore, the bias points of the GaAs field effect transistor (FET) amplifiers will remain unaffected by the RF drive level when using the limiters as shown ([7], [8]).

The negative aspect of the limiter is its gradual transition to a limiting state and its fairly high limiting levels [10]. Typical saturated output levels are in excess of 10 dBm. This would complicate the design of the amplifier accompanying the

limiter since the amplifier would have to be designed for increased compressed output power and would have increased direct current (DC) power consumption. Another aspect is that the voltage standing wave ratio (VSWR) may deteriorate when diode limiters start limiting [11], which may, in turn, cause unwanted interstage reflections. As with the proposed attenuator-amplifier configuration discussed hereafter, the limiter-amplifier approach will require careful design for use in a limiting amplifier configuration. Such a design will prove very dependent on the available limiter and amplifier characteristics.

1.4.2 LIMITING AMPLIFIER EMPLOYING AUTOMATIC GAIN CONTROL

Unwanted non-linear phenomena in the limiting amplifier become more serious as the input drive level increases. At the maximum drive level all the amplifiers in the limiting amplifier are heavily saturated. Clearly, problems with regards to the associated nonlinear phenomena are expected. The biggest problem is that the gain of the limiting amplifier RF chain is too high; especially at the higher drive levels. On the other hand, the gain of the complete RF chain cannot be decreased, since one needs a limited output at the low drive levels as well. Achieving a saturated output power response over a broad input dynamic range thus presents one with a significant problem.

A proposed solution is to monitor the input drive level and to adjust the total gain in the amplifier chain accordingly. This could typically be done by increasing or decreasing the attenuation levels of attenuators used between different amplifier stages. In doing this, one may prevent unwanted overdrive of amplifiers in the limiting amplifier, resulting in overall improved limiting amplifier operation. Shown in Figure 1.15 are two different proposed options to implement automatic gain control (AGC).

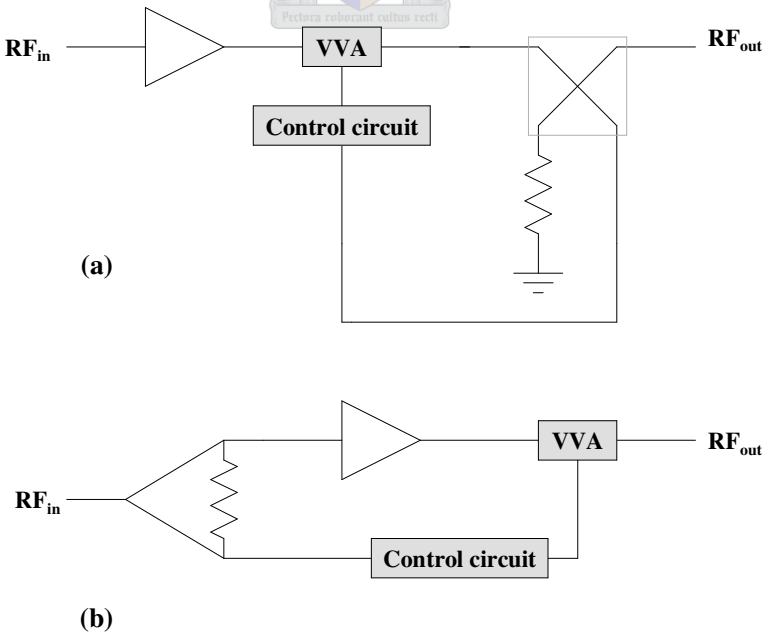


Figure 1.15: Proposed automatic gain control configurations

Configuration (a) shows a closed-loop control circuit that could typically be used just after the low-noise amplifier (or other amplifier) on the input of the limiting amplifier RF chain [10]. The control circuit would typically adjust the nominal attenuation value of the voltage variable attenuator (VVA) according to the detected RF signal power. The problem with this configuration would be the reaction time of the VVA control loop. This option is viable for continuous wave (CW) applications rather than for pulsed RF applications.

An alternative option is configuration (b). In this configuration, the input power is split and again the control circuit adjusts the VVA's nominal attenuation value to prevent overdrive of the next amplifier in the chain. As with configuration (a), this configuration is also suited for CW rather than pulsed applications [10].

A better alternative to the previous two configurations is shown in Figure 1.16. The reaction time issue is addressed in this configuration by making use of a delay line.

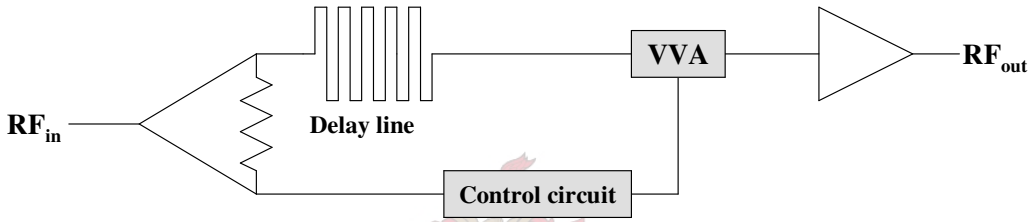


Figure 1.16: Alternative gain control configuration

The shown configuration implements a delay line on the one output of the power splitter. The idea with this configuration is to allow the control circuit enough time to react on incident pulsed RF signals. The feasibility of this type of gain control is, however, another issue, especially when considering the required delay line dimensions. To establish the requirement for the delay line necessary to implement an arbitrary delay of say 45 ns, the following calculation may be done:

The velocity of propagation of a transverse electromagnetic (TEM) wave is given by:

$$v = \frac{c}{\sqrt{\varepsilon_r}} \tag{1.23}$$

where c is the speed of light in free-space (3×10^8 m/sec) and ε_r is the relative dielectric constant of the material in which the wave propagates. If a delay of t_{delay} = 45 ns is required, the length of the delay line with ε_r = 2.2, can be determined from:

$$l = v \times t_{delay} = \frac{(3\times10^{8})(45\times10^{-9})}{\sqrt{2.2}} = 9.1\ m \tag{1.24}$$

This example shows that physical implementation of delay line needed is not feasible when size is an issue. Automatic gain control as discussed is, however, an option to take into account where the application allows for it.

1.4.3 ATTENUATOR-AMPLIFIER CONFIGURATION

An alternative limiting amplifier architecture using alternating attenuators and RF amplifiers (gain stages) is shown in Figure 1.17. This limiting amplifier configuration has been functionally proven and is discussed in more detail hereafter.

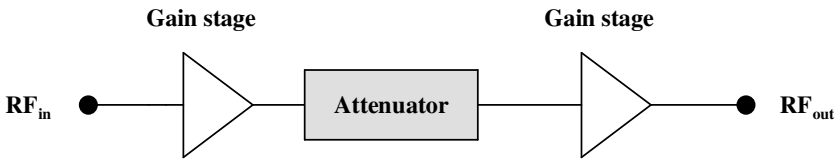


Figure 1.17: Alternative limiting amplifier architecture

The operation of such a configuration is based on the amplitude limiting properties of GaAs FETs used in RF amplifiers. When the output drain current or voltage of a class A GaAs FET amplifier varies along the load line and reaches the saturation or the cut-off region of the FET, amplitude limitation is caused. This limiting effect of the RF amplifier was shown previously in Figure 1.13. The amplifier undergoes gain saturation, with resulting nonlinear effects such as harmonic generation. The question that comes to mind is whether one may allow the nonlinear effects of the RF amplifier while exploiting its power limiting ability.

Figure 1.18 shows the typical harmonic response of an RF amplifier, as obtained from a single-tone experiment. This figure clearly shows how gain saturation occurs above a certain input power level and how the resulting harmonic levels increase as well. The region indicated by **A** in Figure 1.18 will typically have deteriorated harmonic suppression.

Region **B**, hereafter called the *safe limiting region*, on the other hand, provides for an amplitude limited fundamental signal, with harmonic suppression well below that expected in region **A**. If one can operate the amplifier within this region, with harmonics suppressed below a desired level one may very well be able to use this amplifier in a limiting amplifier configuration. A definite consideration will be to what extent one will be able to control and possibly increase this desired *safe limiting region*. This consideration will be particularly important when operating the limiting amplifier at the high end of its dynamic range. When the device is operated at the low end of its input dynamic range, it is only required that the gain of the complete limiting amplifier chain be at least high enough to drive the last amplifier stage into compression.

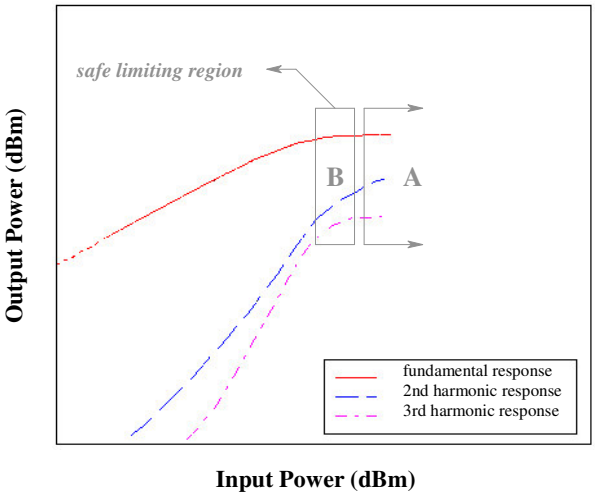


Figure 1.18: Typical harmonic response of an RF amplifier

Looking at the actual results of a single-tone test performed on an RF amplifier, one can get a better idea of the desired operating region of the amplifier and the typical levels of harmonic suppression. From Figure 1.19 it can be seen that the amplifier will offer harmonic suppression in excess of 10 dB when driven with a 5 dBm input tone.

Should this amplifier be used on the front-end of the limiting amplifier, the amplifier's resulting saturated output power will be in the order of 10 dBm when the limiting amplifier is operated at the high end (5 dBm input power) of its dynamic range. To prevent this amplifier from overdriving the next amplifier in the RF chain, an attenuator is placed between the amplifiers. This will ensure that the amplifier following the first will also operate within its *safe limiting region*. The use of attenuators will also improve isolation between different gain stages while minimizing possible interstage reflections.

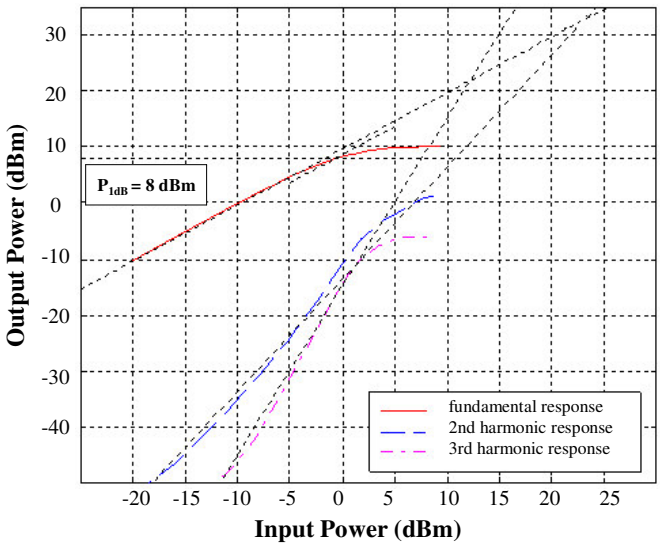


Figure 1.19: Actual results from a single-tone test

The undesired aspect of the attenuator-amplifier configuration is that a sacrifice in gain will have to be made. This may necessitate the need for more amplifier stages which will increase DC power consumption. More gain stages may also contribute to a deteriorated output ripple. Furthermore, one must remember that the *safe limiting region* of an amplifier may vary with frequency, especially in terms of saturated output power and harmonic suppression.

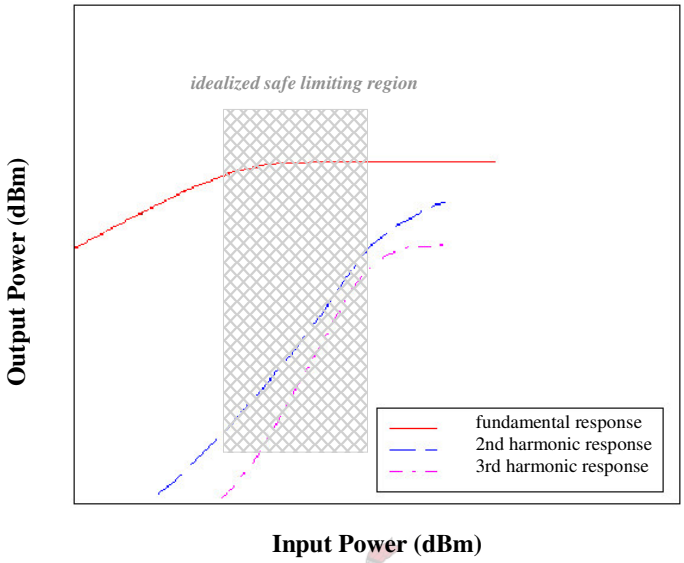


Figure 1.20: Idealized representation of a more desirable safe limiting region

Optimizing the *safe limiting regions* of all the RF amplifiers comprising a limiting amplifier, over its full input dynamic range and operating frequency bandwidth, will be an important design consideration. Figure 1.20 shows an idealized representation of a more desirable *safe limiting region* that will be the aim of an optimization process. The extent to which this optimization is possible will be discussed in chapters to follow.

1.5 CONCLUSION

Automatic gain control within a limiting amplifier configuration has been ruled out for purposes of this study. The question, therefore, remains whether to use attenuators or limiters between the gain stages of a limiting amplifier, since it was shown that both approaches offer significant advantages and disadvantages. It was decided, however, to attempt a limiting amplifier design employing the attenuator-amplifier configuration. No references to this configuration could be found, but sources suggest that with proper small-signal amplifier design, one may be able to realize a limiting amplifier [1]. A few considerations must, however, be taken into account with the small-signal amplifier design to ensure optimum limiting amplifier performance. Typical concerns will be the harmonic output level of the heavily saturated small-signal amplifier, the small-signal gain flatness and some general nonlinear phenomena associated with the RF amplifier [12]. These concerns will typically have to be addressed according to design specifications.

An existing limiting amplifier, employing the attenuator-amplifier configuration, would serve as a suitable baseline for an intended improved design. This existing baseline design is discussed in the following chapter.

CHAPTER 2

THE BASELINE LIMITING AMPLIFIER

2.1 INTRODUCTION

In this chapter an existing 2-18 GHz limiting amplifier, employing the mentioned attenuator-amplifier configuration, is discussed. The discussion is done in terms of actual design, layout and operation, with the specific purpose of providing further insight as to this limiting amplifier's operation. This component hereafter referred to as the *baseline* limiting amplifier, will be used as reference for the formulation of a design hypothesis for the final limiting amplifier design.

2.2 DESIGN BACKGROUND

A strongly nonlinear device, such as the limiting amplifier, operates under large-signal excitation and is plagued by a range of undesired nonlinear phenomena that deteriorates the device's performance. Typically, nonlinear circuits cannot be designed accurately using small-signal S-parameters [9]. S-parameter design techniques, however, offer a good starting point to become familiar with aspects surrounding the RF amplifier and will form the basis for designing a limiting amplifier. S-parameter design techniques also prove useful in designing passive components such as attenuators to be used in a limiting amplifier RF chain. In chapters to follow it will also be shown how an RF amplifier, initially designed for small-signal operation could be optimized to have the desired *save limiting region* as proposed earlier.

2.3 DEVICE OPERATION

The limiting amplifier under discussion operates on the principle previously described as the *capturing effect*. If an amplifier is simultaneously excited by a high-level signal and a low-level signal, where the high-level signal drives the amplifier into saturation, gain is decreased for the low-level signal [9]. Each successive amplifier in the RF chain thus drives the next one closer to saturation thereby providing an overall constant output power level. This ability of the limiting amplifier implies that undesired low-level signals are ideally suppressed well below the wanted saturated power level.

2.4 DESIGN LAYOUT

Shown in Figure 2.1 is the schematic layout of the *baseline* limiting amplifier. Also shown, are the actual *building blocks* of this design. Each amplifier stage, except the first two stages, is separated by a broadband Wilkinson splitter. This splitter is implemented on the plate labelled as (c). The role of the Wilkinson splitters in this configuration is discussed in section 2.9.

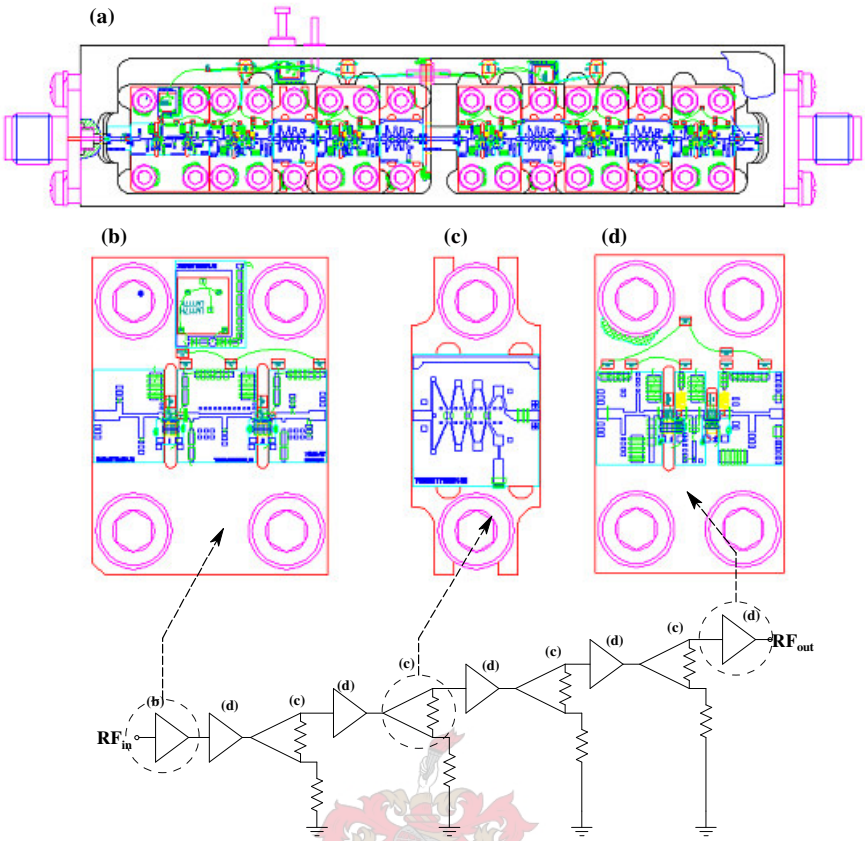


Figure 2.1: Baseline limiting amplifier design layout

The amplifier plate labelled as (b) in Figure 2.1 is a two-stage low-noise amplifier (LNA) comprising the front-end of the limiting amplifier. All the other amplifiers are similar two-stage amplifiers, designed for specific gain and flat compressed output power. For practical operation in the limiting amplifier itself, these amplifiers are tuned to achieve the desired limiting amplifier response, while amplifier small-signal characteristics serve as reference only for physical implementation. Table 2.1 gives a summary of the LNA specifications, while the other gain stages will be discussed in sections to follow.

Description	Specification
Frequency range	2-18 GHz
Gain	12.5 dB
Gain ripple	± 1 dB
P_{1dB} (min)	7.5 dBm
NF	3.5 dB (max)
VSWR	2:1

Table 2.1: Specifications of the LNA used in the baseline limiting amplifier

2.5 THE SIGNIFICANCE OF THE LOW-NOISE AMPLIFIER

The noise figure (NF) of an amplifier is a measure of the degradation in the signal-to-noise ratio between its input and output [1].

The mathematical expression for noise figure, measured in dB, is given by:

$$NF = 10 \log_{10} F \tag{2.1}$$

where F, the noise factor, is defined as:

$$F = \frac{S_{in}/N_{in}}{S_{out}/N_{out}} \tag{2.2}$$

S_{in} and N_{in} are the input signal and noise powers respectively, while S_{out} and N_{out} are the output signal and noise powers respectively. An ideal amplifier would amplify the noise at its input along with the desired signal, while maintaining the same signal-to-noise ratio at its input and output. Figure 2.2 illustrates this situation.

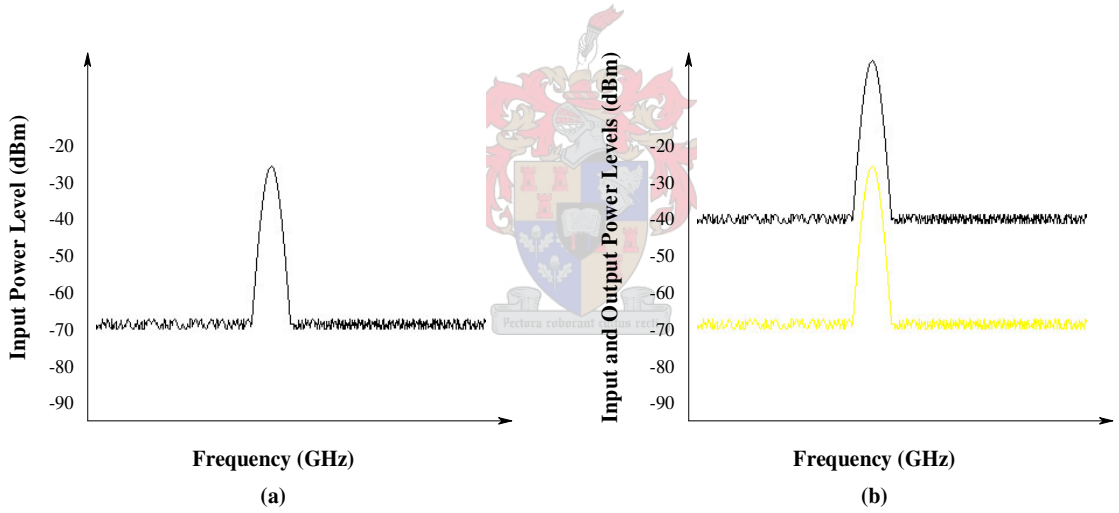


Figure 2.2: Signal and noise levels at an ideal amplifier's input and at its output

Figure 2.2 (a) shows a signal above the noise floor. When the ideal amplifier amplifies this signal together with the noise at its input, the output power levels of both signal and noise will be as shown in Figure 2.2 (b). It is seen that both wanted signal and noise are amplified by the same factor. Using equation (2.2), one can then determine that the noise factor is unity and the noise figure, determined from equation (2.1), is 0 dB. No noise is thus introduced by this ideal amplifier. In practice an amplifier will introduce (additional) noise that will deteriorate the signal-to-noise ratio. This situation is depicted in the Figure 2.3. It is seen that in relation to the wanted signal; the noise level has raised more due to the added noise from the amplifier.

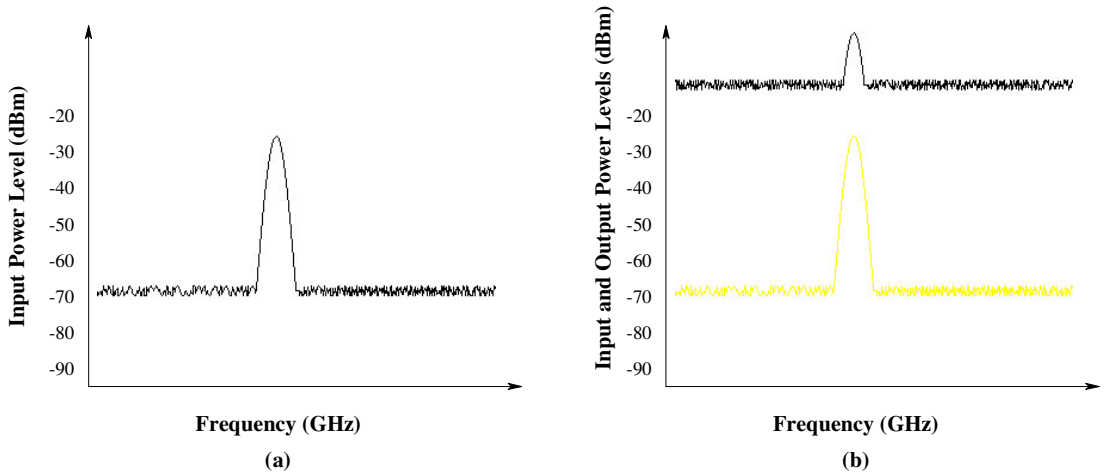


Figure 2.3: Signal and noise levels at a practical amplifier's input and at its output

The significance of a low noise figure is quite apparent. In keeping the noise figure of an amplifier low, one may prevent high noise outputs from the amplifier and losing low-level signals in the noise floor. A low noise figure will therefore also be an important consideration in a proposed limiting amplifier design. The section to follow discusses noise figure in a general system of cascaded amplifiers and provides valuable insight as to the noise figure requirement of the amplifier to be used on the front-end of the proposed limiting amplifier design.

2.6 CASCADED NOISE FIGURE

The general formula for the noise factor of a system of cascaded amplifiers as shown in Figure 2.4, is given by

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots + \frac{F_n - 1}{G_1 G_2 G_3 G_{n-1}} \tag{2.3}$$

where F_n is the noise factor of the nth stage and G_n is the gain factor of the nth stage [4].

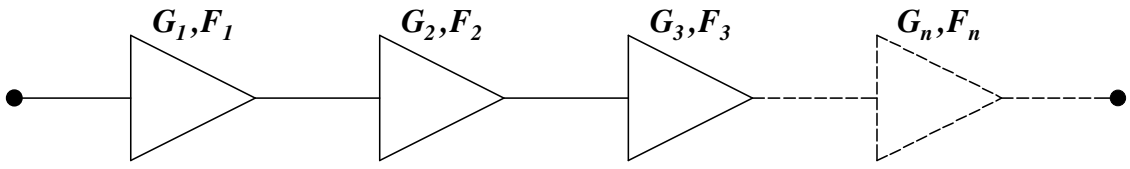


Figure 2.4: General cascaded system

From expression (2.3) it is seen that each amplifier in the cascaded system introduces noise and thus influences the overall noise performance of the system. The noise contribution of the stages following the first stage is much less than that of the first, which dominates noise performance. Apparent from expression (2.3) is that for the best overall noise performance, the first stage should have a low noise figure and high gain.

The unfortunate trade-off in a single-stage LNA design is, however, between low noise and high gain, since both cannot be achieved simultaneously. This fact is apparent from Figure 2.5, which shows the relation between noise figure and associated gain of a typical low-noise GaAs FET. At the point where the noise figure is a minimum, the associated gain is only moderate. Similarly, the noise figure is only moderate for maximum associated gain. The best compromise would be to design the first stage of a cascaded system for optimum noise and moderate gain and the following stages for higher gain and moderate noise [2].

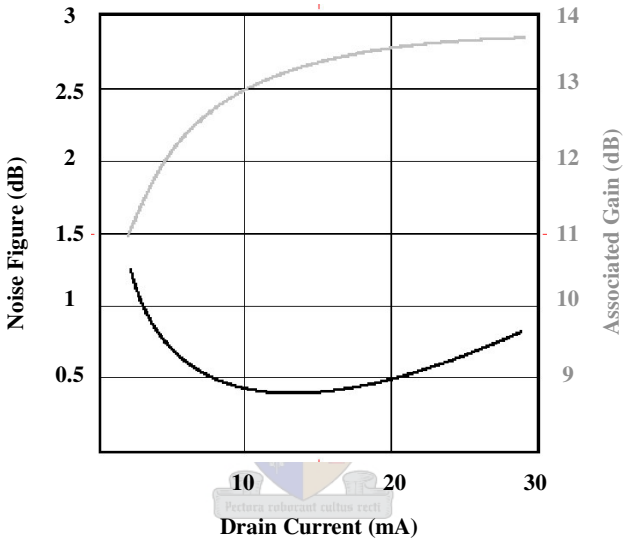


Figure 2.5: Noise figure and associated gain of a typical low-noise GaAs FET

2.7 NOISE FIGURE REQUIREMENTS FOR LIMITING AMPLIFIER DESIGN

The significance of noise figure in an amplifier is that it determines the lowest signal level that can be detected in the presence of noise. The noise figure of the limiting amplifier will thus directly influence the low end of its input dynamic range. As reference for the proposed limiting amplifier design, a calculation is done hereafter that estimates the desired noise figure of the *baseline* limiting amplifier.

The formula used as a *rule of thumb* to determine the minimum detectable signal (MDS) of an amplifier is given by [13] as:

$$MDS = 10\log[\,kTBF\,]\ dBm$$

$$= [10\log(kT) + NF + 10\log(B)]\ \ dBm \qquad (2.4)$$

where k is Boltzman's constant (k = 1.38 × 10^{-23} J/°K), T is the absolute temperature measured in Kelvin and B is the measurement bandwidth measured in hertz (Hz). NF is the limiting amplifier noise figure, which will be influenced mainly by the noise figure of the amplifier used on the limiting amplifier front-end.

It is apparent that the MDS is influenced by the absolute temperature, the relevant measurement bandwidth and the noise figure of the limiting amplifier. Knowing the desired variables of equation (2.4) and the desired operating specifications of the limiting amplifier, one may determine an expression for the MDS in terms of the noise figure of the limiting amplifier. The limiting amplifier's noise figure may then be determined from this relation. For illustration purposes, an approximate *worst-case-scenario* with bandwidth of 20 GHz and T = 358 K (85 °C) is used.

Thus,

$$10\log(kT) = 10\log(4.9404\times10^{-18}) = -173 \text{ dBm} \tag{2.5}$$

In the same way with $B = 20\times10^{9}$ Hz,

$$10\log(B) = 10\log(20\times10^{9}) \approx 103 \text{ dB} \tag{2.6}$$

The expression for MDS then looks as follows:

$$MDS \approx [-173 + NF + 103] \text{ dBm}$$

$$\approx (-70 + NF) \text{ dBm} \tag{2.7}$$

From expression (2.7), for a specified MDS, one can estimate a minimum requirement for the limiting amplifier's noise figure to prevent the limiting amplifier from limiting on noise in the presence of the minimum signal. To achieve an MDS of at least 3 dB better than the threshold level of - 50 dBm, the noise figure of the limiting amplifier must be better than:

$$NF = MDS + 70 = -53+70 = 17 \text{ dB} \tag{2.8}$$

If a - 50 dBm signal is thus applied to the limiting amplifier, the noise floor will ideally only be amplified to within a maximum of 3 dB from the desired signal. One of the requirements for the limiting amplifier is, however, that all spurious signals must be at least 9 dB below the desired signal. The 3 dB separation between the desired signal and the noise is thus insufficient. Taking the desired 9 dB separation into account, a more realistic noise figure is calculated as follows:

This minimum requirement on the limiting amplifier noise figure is determined from:

$$MDS + G = (-53 + G) - 9 \tag{2.9}$$

thus

$$-70 + NF + G = (-53 + G) - 9 \tag{2.10}$$

where G is the small-signal gain of the limiting amplifier. This mathematical relation is illustrated in Figure 2.6.

The minimum requirement on the noise figure, is then determined from equation (2.10) as 8 dB. This noise figure will serve as a *rugged* guideline of what to achieve, with an improvement on this figure the ideal.

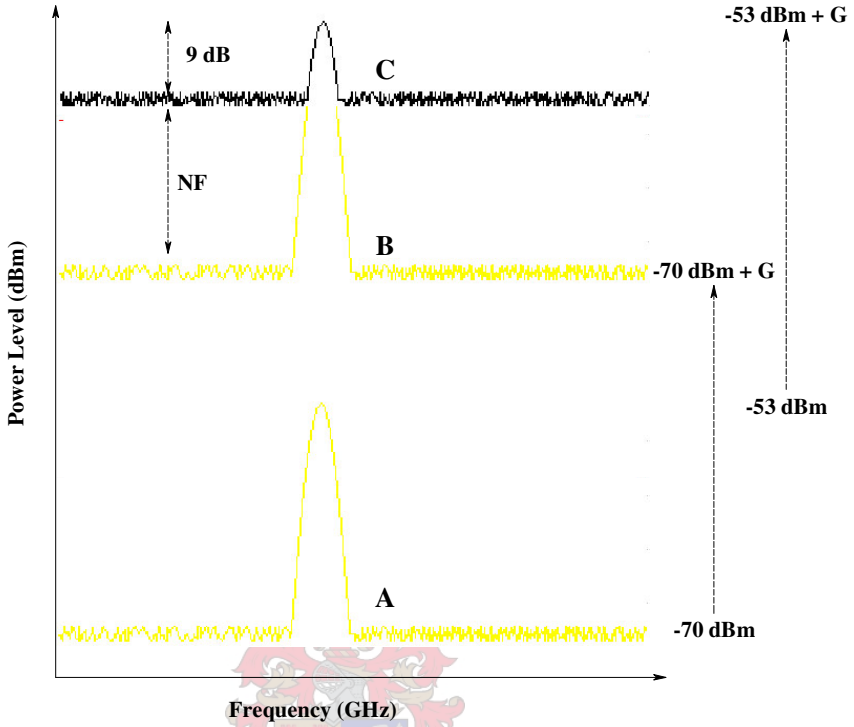


Figure 2.6: Graphical illustration of noise figure calculation

2.8 LNA CONSIDERATIONS

As mentioned, the design criteria for an LNA to be used as the first stage of the limiting amplifier are for optimum noise figure and moderate gain. Other aspects to be taken into account as well are the biasing of the LNA, the variation of the LNA's noise figure as a function of biasing and then also noise figure variation with temperature. Also important, is to know how the gain and output power of the LNA will be influenced if the LNA is biased for optimum noise figure for example. These different LNA considerations are discussed hereafter.

2.8.1 NOISE FIGURE VARIATION AS A FUNCTION OF BIASING

For a GaAs FET, the variation of noise figure with bias current is characterized by a minimum at approximately 0.1-0.15I_{DSS} and a linear rise as the current increases to I_{DSS} [14]. At I_{DSS} the noise figure will typically be only a few dB higher than the minimum. This approximation will only serve as a *rule of thumb* and should practically be verified from manufacturer data sheets or measurements. In terms of bias voltage, the variation of the noise figure with drain-source voltage at a constant current is less spectacular than the variation with current [14]. Keeping this in mind, one may vary the

bias voltage of the LNA, without too much deterioration in noise figure, in order to improve the gain or output power if necessary.

Figure 2.7 shows the noise figure of a typical low-noise GaAs FET. The measurement shows the approximate linear rise in noise figure, from its minimum value as the drain current increases. This type of measurement is typically done at the midband of the FET's operating frequency band, with biasing at the optimum point. The shown response, however, only gives an estimate of the noise figure expected from the device.

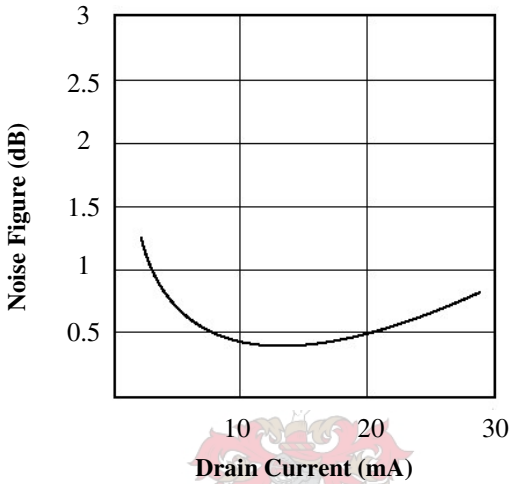


Figure 2.7: Noise figure versus drain current for a typical low-noise GaAs FET

2.8.2 NOISE FIGURE VARIATION WITH TEMPERATURE

An intuitive assumption regarding noise figure variation with temperature can be made, if one examines the noise figure response of a typical GaAs FET, as a function of drain current. It is known that the drain current of a GaAs FET will be influenced by temperature variation and a decrease in drain current is expected as temperature increases and vice versa [15].

From Figure 2.7 it can be seen that the worst deterioration in noise figure will occur when the drain current decreases below its optimum value. This deterioration will typically occur when the device is heated up. To show this deterioration experimentally, noise figure measurements were made on a single-stage 2-18 GHz amplifier. This amplifier was not designed for optimum noise figure, but rather for moderate noise figure. Nevertheless, the amplifier was suitable for establishing how noise figure varies over temperature. Noise figure measurements were made from 2-18 GHz at temperatures of - 54 °C, 25 °C and 85 °C. The results are shown in Figure 2.8. The measured results confirmed that deterioration in noise figure occurs as the temperature increases. At low temperatures the measured noise figure improved on that measured at room temperature, indicating a shift in bias point that allowed for a better noise figure.

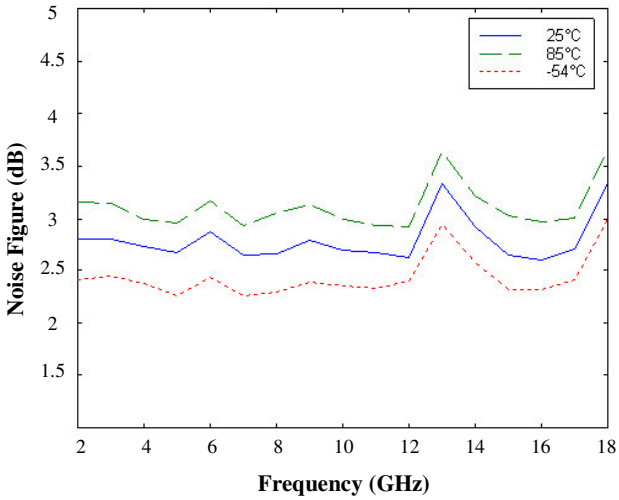


Figure 2.8: Variation of noise figure with temperature

The discussion on noise figure allowed for better insight as to the significance thereof in the RF amplifier and in the limiting amplifier for that matter. The significance of the LNA on the *baseline* limiting amplifier's front-end was established and it was shown to be an important design consideration. The remaining topics for discussion regarding the *baseline* design are the Wilkinson splitters and the other gain stages that form part of this design.

2.9 THE WILKINSON SPLITTERS

The Wilkinson splitters, in the *baseline* configuration do not function as power splitters, but rather as attenuators. These *attenuators* provide at least 5 dB (insertion loss of the broadband power splitter) isolation between the saturated amplifiers. The *attenuators* also allow for improved matching between the different amplifiers. The improved matching is of particular importance since the amplifiers will suffer from a deteriorated return loss as they are driven with increasing input levels. The splitters also decrease amplifier input drive levels and so prevent unwanted overdrive of the amplifiers. Without going into the detail of broadband Wilkinson splitter design, a short summary of the normalized parameters needed to implement these splitters will be given. These design parameters were used for the design of a broadband splitter, used as attenuator, to be compared with an actual designed 3 dB attenuator.

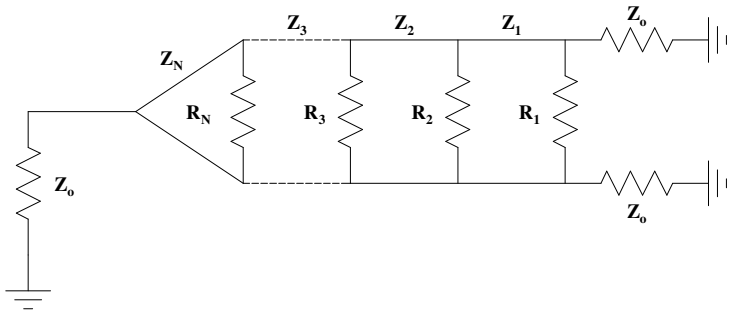


Figure 2.9: Multi-section Wilkinson power splitter configuration

Figure 2.9 shows an *N-section* circuit, containing *N* pairs of equal length transmission lines and *N bridging* resistors. Using the normalized design parameters as given in [16], broadband Wilkinson splitters can be designed, with bandwidth being dependent on the amount of sections used. A summary of the normalized design parameters is given in Table 2.2.

Number of sections (*N*)	**2**	**3**	**4**
Z_1	1.2197	1.1497	1.1157
Z_2	1.6398	1.4142	1.2957
Z_3	*	1.7396	1.5435
Z_4	*	*	1.7926
R_1	4.8204	8.0000	9.6432
R_2	1.9602	4.2292	5.8326
R_3	*	2.1436	3.4524
R_4	*	*	2.0633

Table 2.2: Broadband Wilkinson splitter design parameters

The shown design parameters were used to design a three-section 2-18 GHz splitter. At first, the splitter is simulated without any T-junctions or practical interconnects as shown in Figure 2.10. In doing this, one gets an intuitive feel for the splitter response and how accurate the given design parameters can be used in the design of such a splitter.

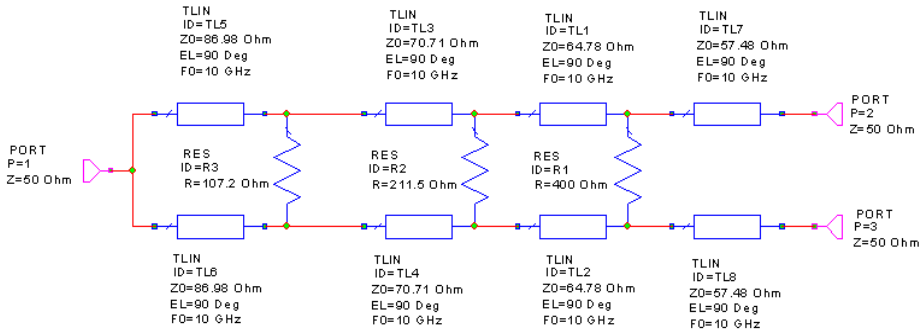


Figure 2.10: Basic implementation of the multi-section Wilkinson power splitter

The simulated response of the shown configuration is given in Figure 2.11. From the simulation it is apparent that the multi-section splitter is more lossy, with the insertion loss (IL) being more than the ideal 3 dB. The return loss (RL) on all ports and the isolation between the output ports are acceptable.

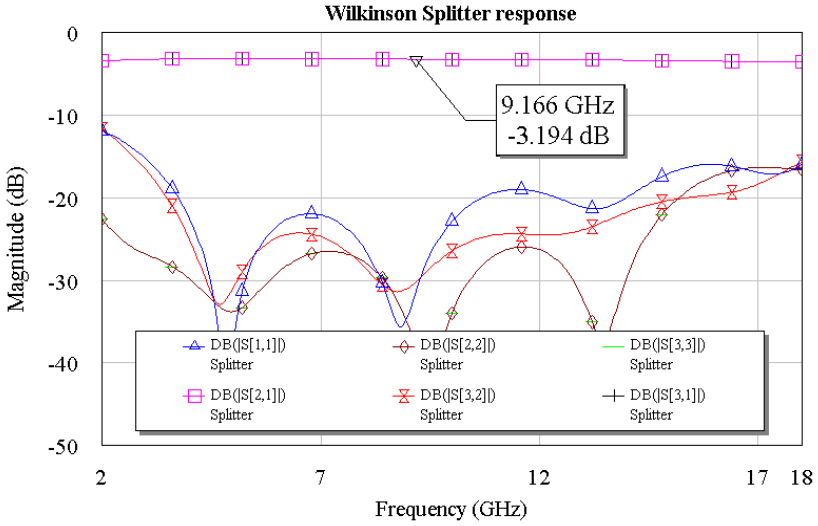


Figure 2.11: Simulated response of the multi-section Wilkinson power splitter

With a baseline splitter design established one may implement the practical aspects of the splitter, such as interconnects, T-junctions, bends, etc. The schematic layout of the splitter as implemented in MWO is shown in Figure 2.12. This layout shows the implementation of the desired interconnections, T-junctions and bends as required for physical implementation of the design.

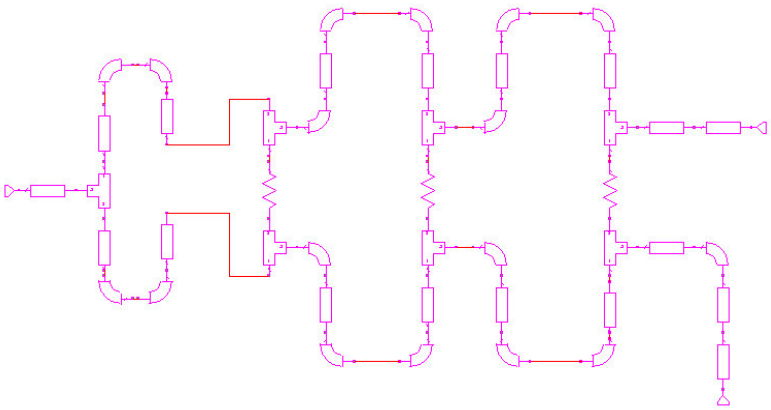


Figure 2.12: Schematic layout of the multi-section Wilkinson power splitter

The design is optimized for improved response and operation is confirmed by use of MWO's electromagnetic (EM) simulator. Confirmation with the EM simulation is suggested since this offers a better representation of the actual expected response of the design. The simulated response of the completed design, after optimization, is shown in Figure 2.13. The simulated response again shows that the insertion loss is more than the ideal 3 dB. Further deterioration may then also be expected after physical implementation of the design. The return loss over the 2-18 GHz band is typically better than 10

dB. The isolation between the two output ports is typically better than 10 dB. Improved isolation could be achieved with an extra section, but at the expense of insertion loss.

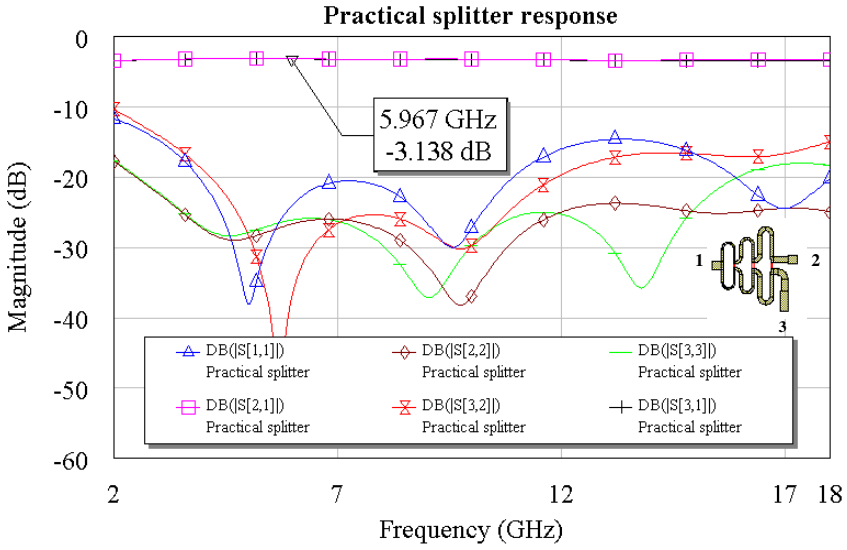


Figure 2.13: Simulated response of the practical multi-section Wilkinson power splitter

Figure 2.14 shows the artwork of the designed three-section Wilkinson splitter complete with bends, junctions and interconnects implemented. The resistors on the actual splitter are implemented as thin-film etched resistors.

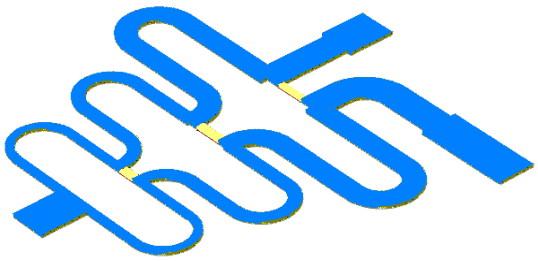


Figure 2.14: Artwork layout for the three-section Wilkinson power splitter

The illustrated design was implemented on Alumina and measurements were made to confirm the simulated results. The actual measured results are shown in Figure 2.15. Comparing the measured results to the simulated results, it is seen that the actual implemented splitter is more lossy than the simulated splitter. The typical measured IL is in the order of 3.65 dB, reaching a maximum of about 5 dB. The main reason for the poorer IL is due to long transmission lines (with the associated transitions) that were used to test the splitter in a test jig. The effects of these extra line lengths as well as transitions were not taken into account during simulations. The typical measured return loss is better than 9.5 dB. Although not as good as simulated, the measured results are acceptable and show the extent to which a design can be practically implemented.

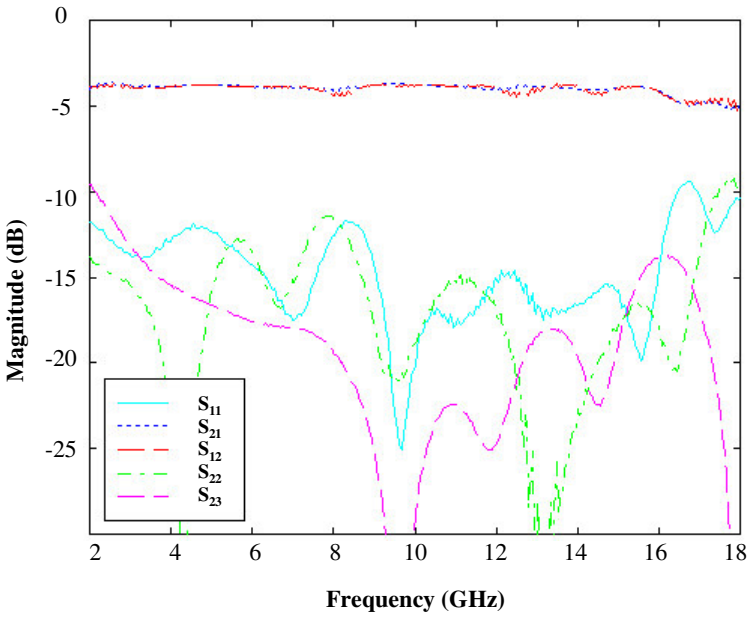


Figure 2.15: Measured response of the designed three-section Wilkinson power splitter

2.10 DESIGN AND IMPLEMENTATION OF A 3 dB ATTENUATOR

A short discussion follows on the design of an etched 3 dB attenuator for use in the limiting amplifier. Shown in Figure 2.16 is the well-known configuration of a 3 dB T-attenuator with a characteristic impedance of 50 Ω, [2]. The attenuator is matched on its input and output with the associated input and output return loss expected to be ideally infinitely small. The mechanism of operation of this passive device is well-documented ([2], [17]) and is not discussed further in this thesis. A significant consideration, however, is the physical implementation of this device for operation up to 18 GHz. The design requires the inclusion of lengths of transmission lines between the different thin-film resistors and careful consideration of their effect on the desired attenuator response.

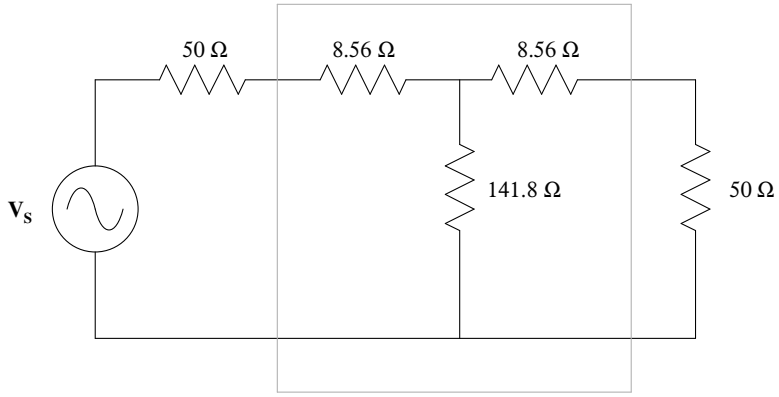


Figure 2.16: The 3 dB attenuator in a 50 Ω system

Shown in Figure 2.17 is the design layout of the 3 dB attenuator after optimization of different interconnects. This design will be recognized as part of the final limiting amplifier design with deviations on this design allowed merely to ensure the desired physical implementation.

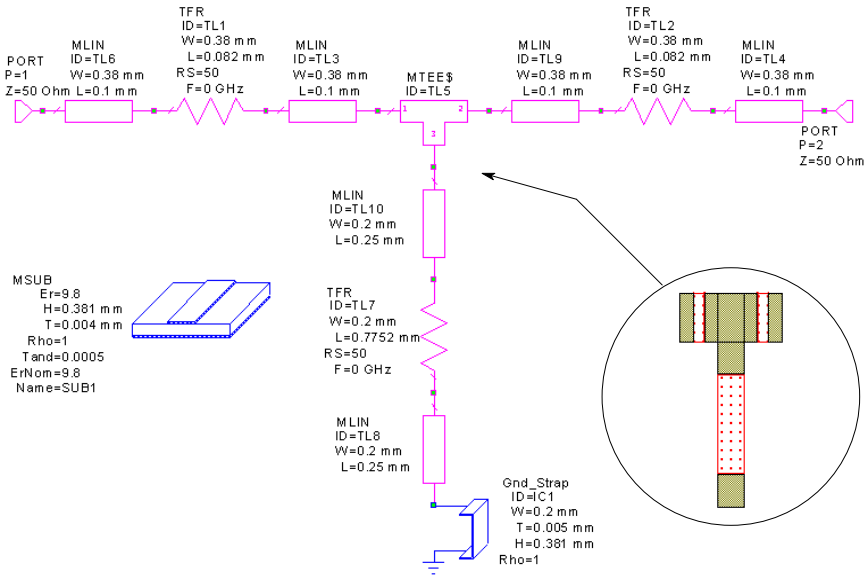


Figure 2.17: Layout for the 3 dB attenuator

The simulated results for the designed attenuator are shown in Figure 2.18.

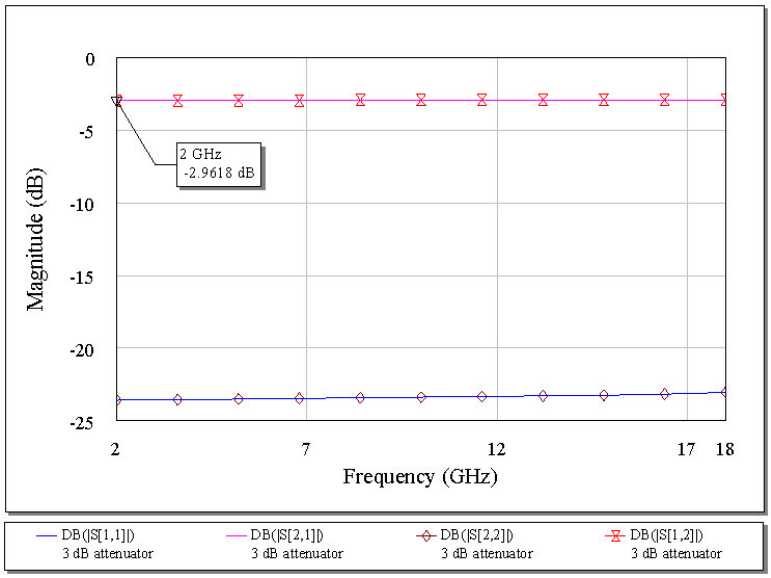


Figure 2.18: Simulated response of the 3 dB attenuator

The simulated response shows that the attenuator will be well-matched over the 2-18 GHz bandwidth. The typical insertion loss (IL) is simulated as 2.96 dB, close to the expected 3 dB. No effort was put in to optimize the simulated IL to exactly 3 dB, since practical implementation would also include contributory losses.

Actual measurements on the designed attenuator are shown in Figure 2.19. It is seen that the IL is quite a bit higher than expected. This is due to rather long transmission lines that were connected to the input and output of the attenuator. Nevertheless, the input and output return loss is very good over the 2-18 GHz bandwidth. A more accurate measurement may have been performed by making use of the vector network analyzer's *gating* function. This would allow for characterizing the design without the effect of extra losses as part of the test assembly.

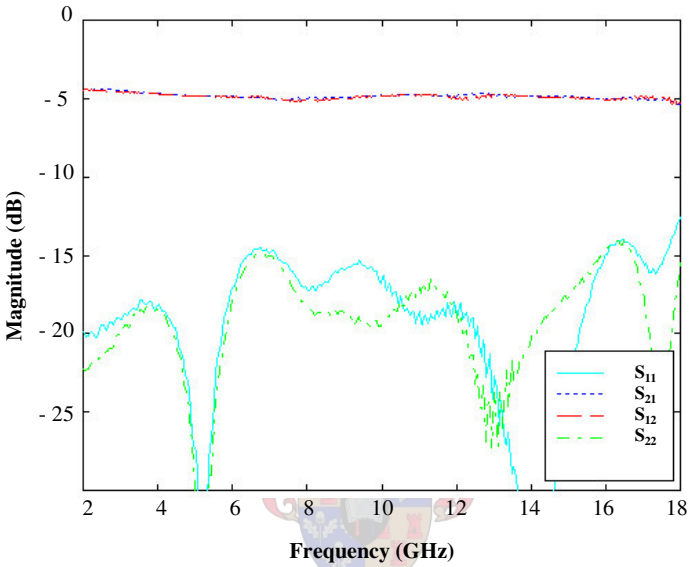


Figure 2.19: Measured response of the 3 dB attenuator

With a physical attenuator and splitter design available, it allowed for actual testing to compare the response of the attenuator with that of the splitter used as attenuator. The section to follow, discusses this comparative evaluation.

2.11 COMPARISON OF AN ATTENUATOR, WITH A POWER SPLITTER USED AS ATTENUATOR

Experiments were carried out to establish whether a normal etched attenuator could be used as a form, fit and function replacement for the Wilkinson splitters used in the *baseline* limiting amplifier design.

As a first step, an experiment was done in MWO to determine how responses of the ideal splitter and attenuator models would differ for varied load conditions. In a practical situation, these varied load conditions would be caused by an amplifier exposed to varied drive levels, bias point variations etc. Figure 2.20 shows the implementation of an ideal attenuator and splitter in MWO. The port element PORTG allows the terminating impedance of the port to be specified as a

magnitude and angle of reflection coefficient. The parameters of this port, GM and GA, are enabled for tuning. The responses (S_{11}, S_{21}, S_{12} and S_{22}) for both configurations are monitored for different values of GM and GA.

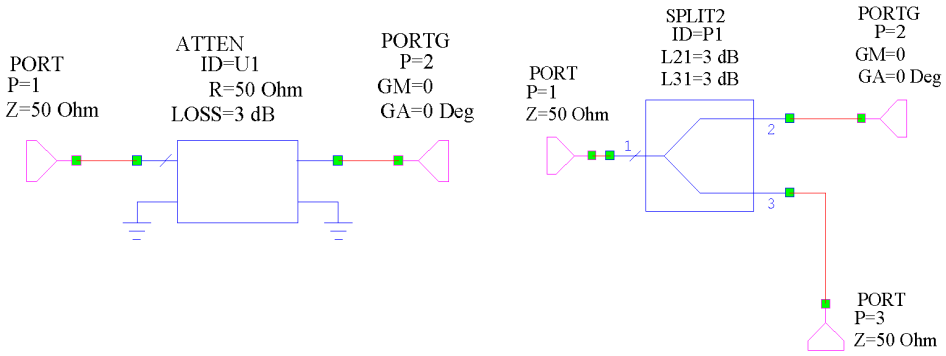


Figure 2.20: Ideal attenuator and splitter as implemented in MWO

Varying the phase angle (GA) of the terminating impedance between - 180° and 180° resulted in no difference whatsoever in simulated responses of the splitter and attenuator. Varying the magnitude (GM) of the terminating impedance between 0 and 1 resulted in deteriorated insertion loss and return loss for both passive components. The problem with the simulation is that the ideal models do not take into account the finite isolation between the splitter output ports, the actual phase shifts associated with the practical attenuator and splitter and the parasitics associated with actual implementation. To obtain a more accurate comparison, actual designs were used for simulations.

Figure 2.21 shows the simulated response of the designed attenuator and splitter for a specific load (GA = 30° and GM = 0.2). Similar measurements were also made at different load conditions in order to establish how the two devices compared to each other. In terms of input and output return loss, it is difficult to say which device's response is best. This being due to the attenuators overall flat return loss response while the splitter's return loss response is more varied. In general however, the attenuator's input and output return loss is better than that of the splitter, when comparing maximum values. Point **A** in Figure 2.21, which indicates the maximum point of the splitter's input return loss, is higher than point **B**, which indicates the maximum point of the attenuator's input return loss. Over the rest of the frequency band, one can see that the input return loss of the splitter is actually lower than that of the attenuator over the largest part of the frequency band. Similarly one can make conclusions regarding the output return loss.

Simulations also highlighted some other significant considerations. As with the ideal case, the insertion loss and the return loss is influenced by varying GM. Varying GA became very significant in changing the simulated response. The insertion loss of the splitter is more than that of the attenuator; this being due to the multiple sections used in the splitter. Simulations also showed that the ripple on the attenuator's typical insertion loss response was ± 0.03 dB, compared with the splitter's ± 0.24 dB.

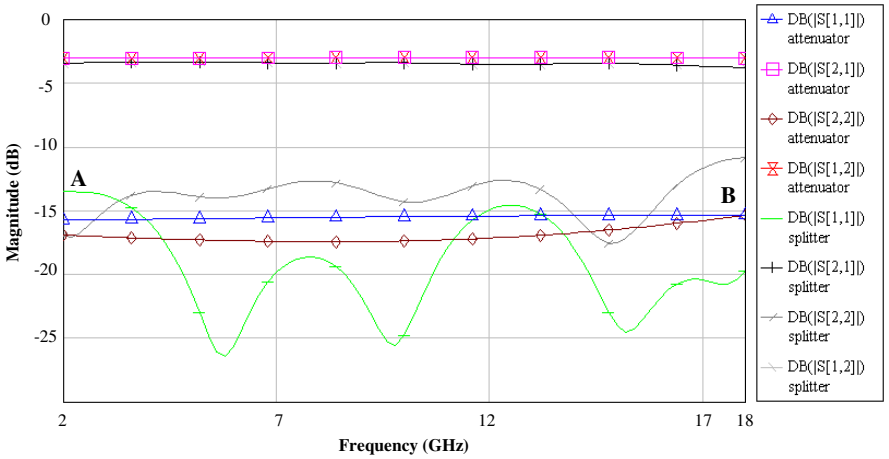


Figure 2.21: Simulated response for designed splitter and attenuator

In general it would appear as though an attenuator would be a good replacement for a splitter used as an attenuator. It is less lossy, its ripple is less, and it is physically smaller than a multi-section splitter and offers good input and output return loss.

Some other aspects have to be taken into account as well. A splitter may offer better matching at certain frequency points as was shown. The phase shift introduced by either splitter or attenuator when used between amplifiers may be important and should be taken into account when used in a design. Another aspect that was investigated was the response of the splitter and attenuator with temperature. In doing this experiment one may then also establish whether there is any temperature variation associated the etched resistors used in these passive components. Figures 2.22, 2.23 and 2.24 show the response of the designed attenuator with temperature. The results show that the deterioration in response of the attenuator is practically negligible over temperature.

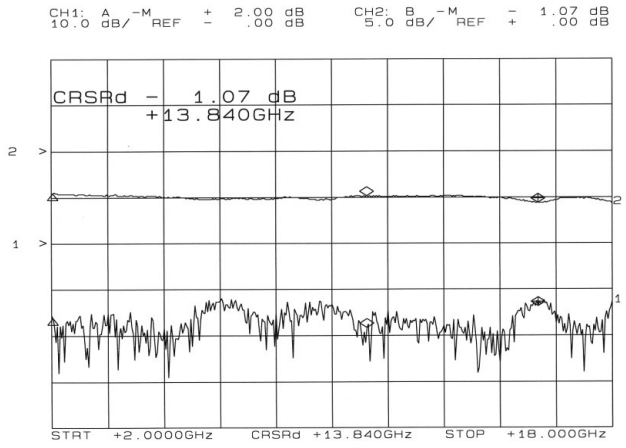


Figure 2.22: Attenuator response at - 54 °C

At - 54 °C (Figure 2.22) the attenuator offers a ripple of 1.1 dB, which is a slightly worse than the 1 dB ripple measured at room temperature (Figure 2.23).

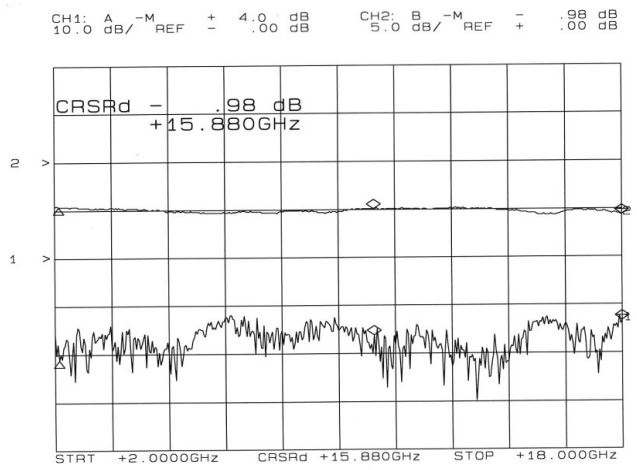


Figure 2.23: Attenuator response at 25 °C

Figure 2.24 shows the attenuator response as measured at 85 °C. With a ripple of 0.95 dB, it shows little deterioration from the response measured at room temperature.

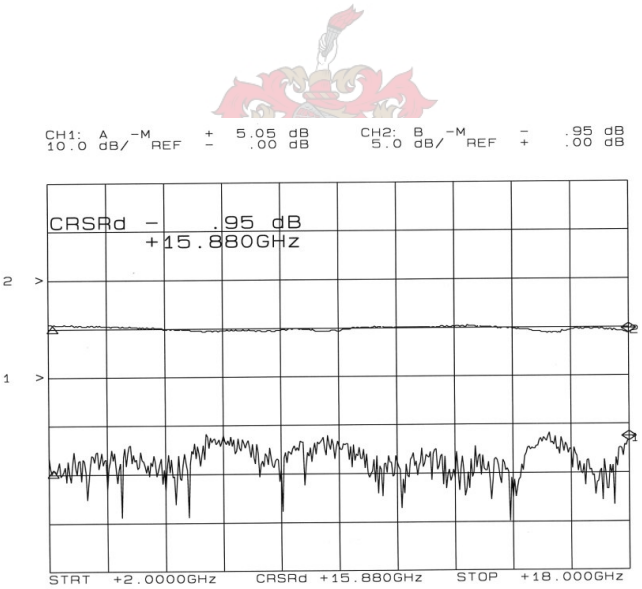


Figure 2.24: Attenuator response at 85 °C

Figures 2.25, 2.26 and 2.27 show the response of the designed splitter over temperature. Again there is little deterioration in the measured response over temperature. At 85 °C, a ripple of 1.4 dB was measured for the designed splitter, as seen in Figure 2.25.

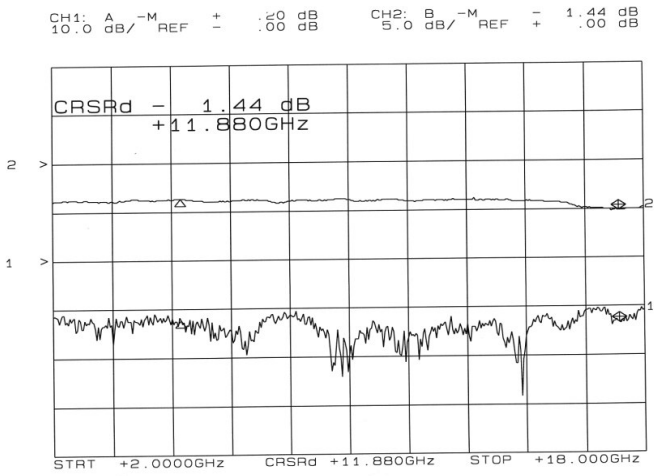


Figure 2.25: Splitter response at - 54 °C

The splitter response at room temperature, as seen in Figure 2.26, shows a slight improvement on the measured ripple, when compared to that measured at - 54 °C. The measured ripple of 1.3 dB does not deteriorate further as the temperature increases to 85 °C, as is evident from Figure 2.27.

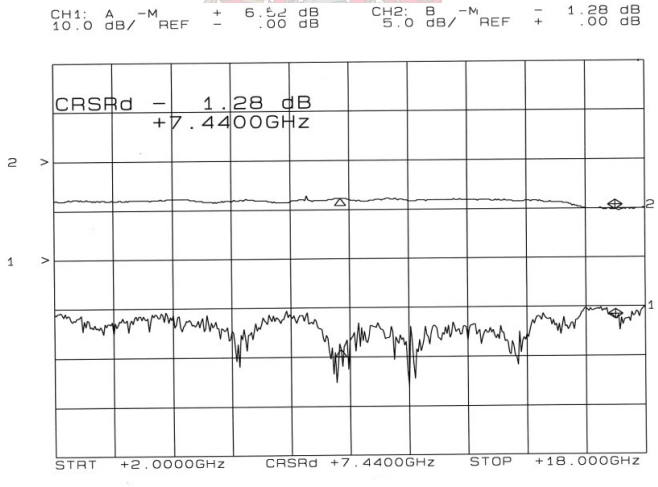


Figure 2.26: Splitter response at 25 °C

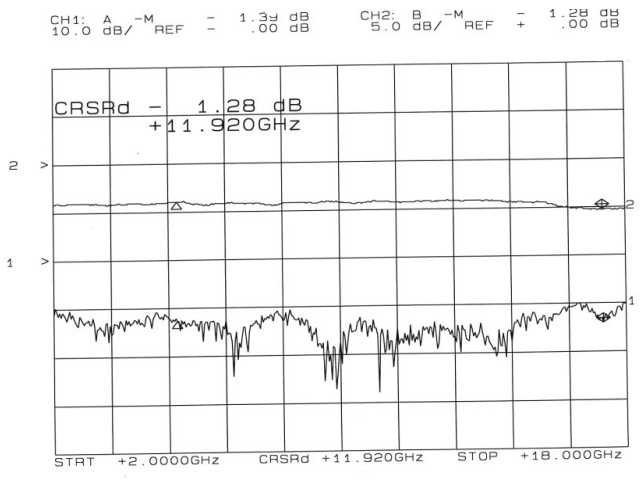


Figure 2.27: Splitter response at 85 °C

Experimental results thus showed that an attenuator could replace a splitter used as attenuator, without significant deterioration in response expected. Neither of the two components offers significant variation over temperature, which may serve as an indication that the resistance of the etched thin-film resistor does not vary much over temperature. Small changes that are observed may be due to test cables subjected to undesired temperature transfer. The only other effect that may necessitate the use of a splitter is when the phase shift introduced by it, is required within a limiting amplifier configuration. This, however, can only be confirmed during an actual design.

2.12 GAIN STAGES

The amplifiers other than the first, used in the *baseline* limiting amplifier are two-stage amplifiers, designed for maximally flat compressed output power. Ideally, this would mean that gain compression would only be a function of input power and not frequency. Practically, however, one would see that gain compression occurs at certain frequencies, before other frequencies. A summary of the design specifications for these amplifiers are given in Table 2.3.

Description	Specification
Frequency range	2-18 GHz
Gain	15 dB
Gain ripple	± 1 dB
P_{1dB} (min)	10 dBm
NF	≈ 4.5 dB
VSWR	2.5 : 1

Table 2.3: Amplifier specifications

The compression characteristics of the different gain stages are measured before they get inserted in the limiting amplifier RF chain. With the typical compression characteristics of the amplifier known one can establish an intuitive feel of typical output power from the amplifier when driven into saturation. One can also intuitively establish how hard the amplifiers in the limiting amplifier RF chain are driven into saturation depending on the excitation signal levels. What is not clear, however, is the actual signal distortion caused in these amplifiers. The biggest problem with this small-signal S-parameter design was that no nonlinear characterization was available to accurately predict the nonlinear behaviour of the respective RF amplifiers. The desirable alternative is accurate nonlinear modelling of the different small-signal RF amplifiers in order to evaluate their nonlinear response. This will then also be the design approach to be discussed in chapters to follow. In the section to follow, some of the measurements that were done on the *baseline* limiting amplifier are given.

2.13 MEASUREMENTS ON THE BASELINE LIMITING AMPLIFIER

Shown hereafter are measurements that were performed on the *baseline* limiting amplifier so as to give a better indication of the desired response of the intended design. Figure 2.28 shows the measured saturated output power of the limiting amplifier measured at input drive levels of - 50 dBm, - 30 dBm and + 5 dBm respectively. The results show that the saturated output power stays within a window of approximately 4 dB, independent of the input drive level.

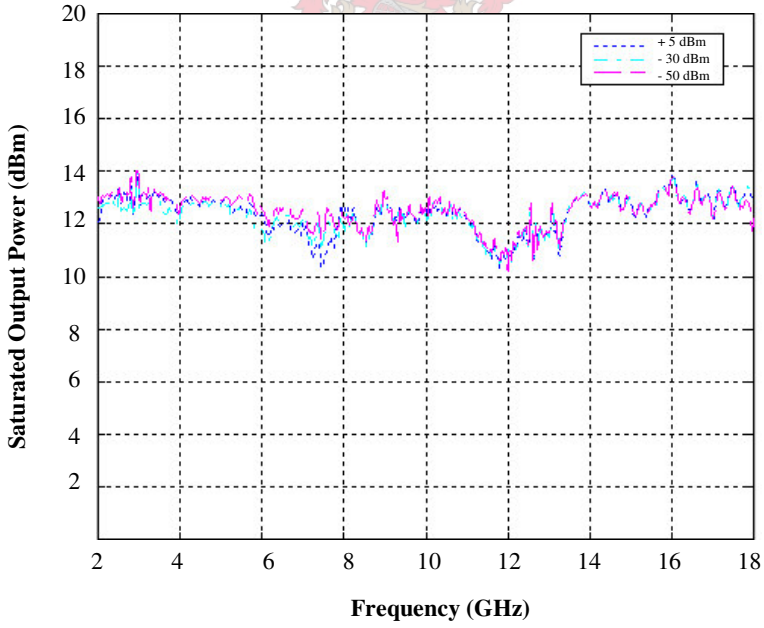


Figure 2.28: Saturated output power of the baseline limiting amplifier

The limiting amplifier is driven with a synthesized sweeper at a certain drive level. The input signal frequency to the limiting amplifier is swept over 2-18 GHz with the *max hold* function of the spectrum analyzer enabled. The *max hold* function allows the spectrum analyzer to sample only the peak values of the resulting output spectra. The result is a

saturated output power trace of the fundamental tone. Important in this regard is that the sweep time of the input signal be much longer than that of the actual spectrum analyzer, to ensure an accurate output power trace.

Harmonic suppression can be observed by manually sweeping the input signal over the 2-18 GHz band and monitoring at which drive level and input frequency, deterioration of harmonic suppression occurs. A typical result of such a measurement is shown in Figure 2.29.

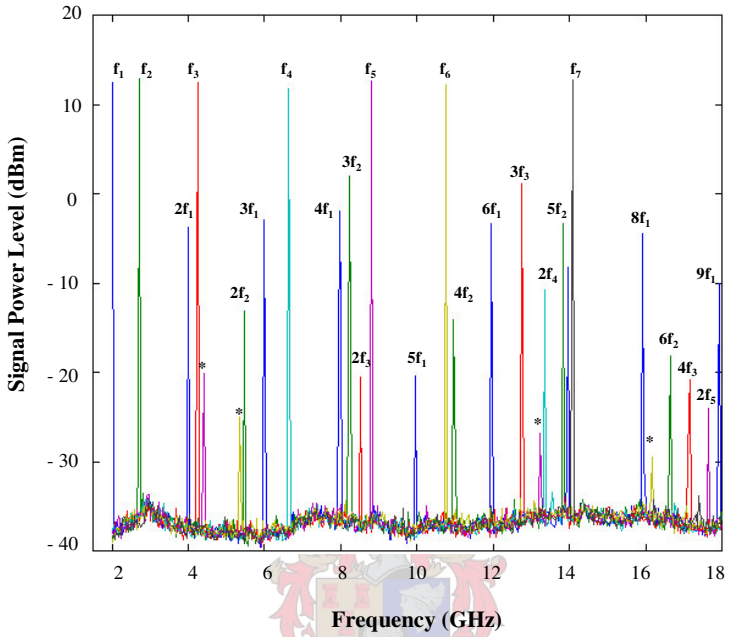


Figure 2.29: Harmonic suppression measurement done on the baseline limiting amplifier

Figure 2.29 shows a portion of a measurement done on the *baseline* limiting amplifier. The result seen is that obtained when driving the limiting amplifier at a certain drive level (0 dBm in this case) at a few spot frequencies. The swept measurements show the extent to which harmonic generation occurs and what the typical expected suppression below the wanted fundamental signal, is. Most frequency components seen are merely harmonics of the input signal and their presence within the operating bandwidth is easily predicted. The frequency components labelled with asterisks, however, are spurious products generated within the limiting amplifier RF chain. The presence and actual power levels of these products are not easily predicted. Ideally, a proper simulated design will accurately predict all relevant frequency components and their levels within the RF chain. Only then will one know about undesired frequency components and could one attempt to suppress them as required.

At the time of doing the previously discussed measurements, no automated test setup was available to do swept measurements over the whole input dynamic range of the *baseline* limiting amplifier and over its full 2-18 GHz bandwidth. Manual measurements were done that failed in characterizing the complete limiting amplifier response. As part of this study it was attempted to acquire an improved measurement configuration that would allow for better characterization of a designed limiting amplifier. The following chapters will elaborate on this aspect and it will be shown how automated measurements offered the desired limiting amplifier characterization.

2.14 CONCLUSION

An existing limiting amplifier design was discussed in this chapter. This *baseline* limiting amplifier was investigated in order to establish some reference for an intended improved design. No other references to a 2-18 GHz limiting amplifier employing the shown configuration were found.

Before attempting any improved limiting amplifier design, a sound RF amplifier design capability had to be established. This was deemed necessary in order to better understand the behaviour of the RF amplifier and to better understand its operation within the limiting amplifier RF chain. The following chapter reports on some of the amplifier designs that were attempted and it is shown to what extent an amplifier design capability was established.

CHAPTER 3

RF AMPLIFIER DESIGN CONSIDERATIONS

3.1 INTRODUCTION

With RF amplifiers forming such an integral part of a limiting amplifier design, it is justified to have a chapter devoted exclusively to this topic. Different RF components, essential to the design of an RF amplifier, are discussed to become familiar with their physical implementation, limitations and response. Without going into the detail of already well-documented amplifier design theory, a discussion on the RF amplifiers that were designed for purposes of this study is given. These designs were done not only to establish the necessary theoretical foundation for RF amplifier design, but also offered valuable practical design experience. These designs were used effectively for evaluating different concepts discussed in this study, while providing substance to existing theory. Attention is given to the two design packages, *Microwave Office* (MWO) and *MultiMatch*, which were used in conjunction with each other. It is shown how they complement each other to form a powerful RF amplifier design tool.

3.2 COMPUTER-AIDED DESIGN

Three computer-aided design packages namely *MultiMatch*, MWO and *AutoCad* were used for the design and implementation of RF amplifier designs. At the heart of all designs is *MultiMatch*, a complete amplifier design program with a generalized approach to estimate the output power (1 dB compression point) of a linear amplifier without resorting to nonlinear analysis techniques [33]. This program was used since MWO did not offer this complete amplifier synthesis ability (as yet). The most significant property of *MultiMatch* is its artwork output of a design which allows for direct manufacturing. It does, however, not offer the tuning and optimization features that are available in MWO. For this reason, designs done in *MultiMatch* were exported to MWO for refined tuning and optimization. The artwork generated by MWO was then exported to *AutoCad* to do circuit layout and mechanical design for eventual manufacturing.

3.3 SMALL-SIGNAL VERSUS LARGE-SIGNAL OPERATION

A general single-stage RF amplifier is shown in Figure 3.1. This configuration shows a two-port device, characterized as an S-parameter model, together with its associated impedance matching networks. Typically the S-parameters of an active device, measured at a specific bias point, makes up this S-parameter model. In the shown configuration the bias network is not shown, since it should ideally not influence the amplifier's response.

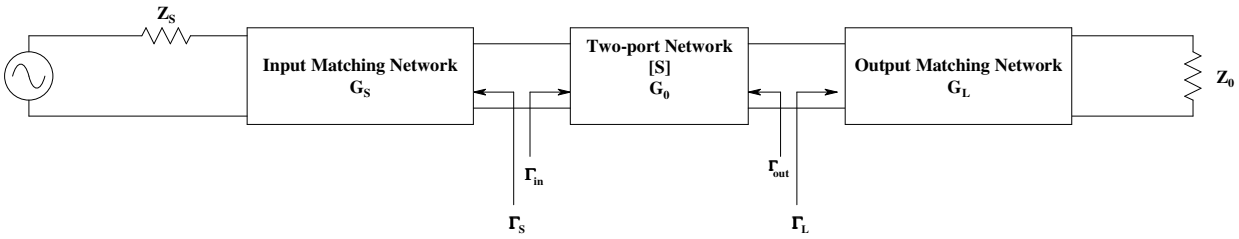
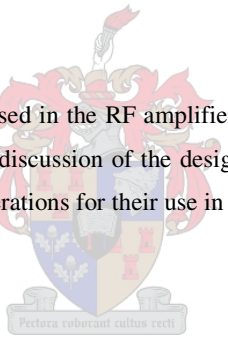


Figure 3.1: The general RF amplifier configuration

The RF amplifiers to be discussed are common-source small-signal amplifiers under class A operation. The term *small-signal* indicates that the amplifier is operated in its linear region, but more importantly is the fact that one can make use of small-signal S-parameter design techniques. Small-signal S-parameters can be used for the design of large-signal amplifiers operating in class A, but large-signal operation will introduce nonlinearities in the output signal [17]. The term *large-signal* is thus associated with nonlinear operation.

3.4 RF COMPONENTS

A discussion on the most essential components used in the RF amplifier follows hereafter to better understand their place and purpose in a design and to better follow the discussion of the design examples to follow. Although these devices are familiar to most, there are some important considerations for their use in a broadband RF amplifier that needs mentioning.



3.4.1 FETS

There are quite a few considerations in deciding on the active device to be used for an intended RF amplifier design. A general purpose FET covering a broad frequency range is usually chosen to allow for standardization of designs. The device should offer reasonable associated gain, as well as a low noise figure. FETs operated up to 18 GHz are typically not packaged and come in a die form such as that shown in Figure 3.2. The physical dimension of this die is typically in the order of 0.3 × 0.3 mm. The die does not have all the parasitics and losses associated with a packaged device and allows for low-inductance interconnections between the device itself and the rest of the RF circuit. The die should be mounted on a metal *rib* to keep interconnecting bond wire lengths between the device and the rest of the RF circuit to a minimum [18].

Another consideration for using a specific FET is whether an accurate nonlinear model exists for the device. The nonlinear model is necessary for evaluating the nonlinear behaviour of an RF amplifier designed with small-signal S-parameter techniques and to compare its response with implemented S-parameter models, measured at different bias points.

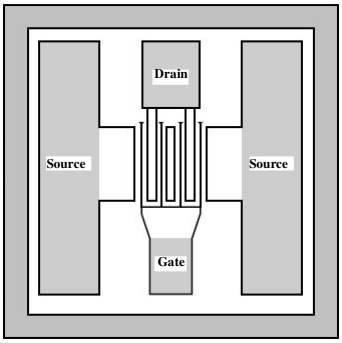


Figure 3.2: Layout of a typical GaAs FET die

3.4.2 CAPACITORS

Figure 3.3 shows the implementation of a chip capacitor on a transmission line. The capacitor functions as a coupling capacitor but also decouples DC where applicable in a physical circuit.

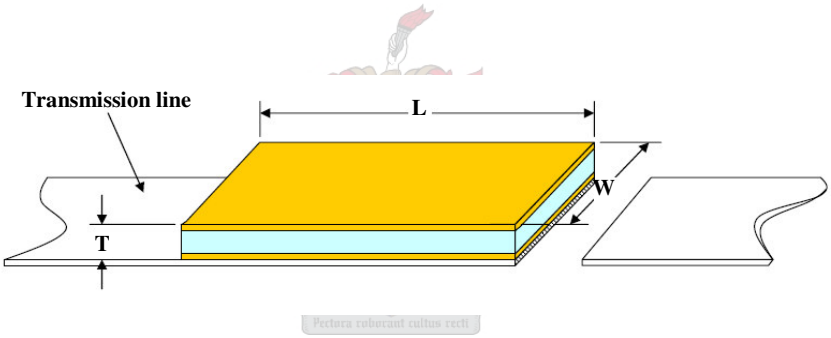


Figure 3.3: Chip capacitor on a transmission line

Not shown in Figure 3.3 is the actual interconnection between the capacitor and the adjacent transmission line. This connection is either made with bonding ribbon or with bonding wires. To reduce the inductance associated with these interconnects, their length is kept to a minimum and typically, more than one wire bond or ribbon is used. The inclusion of the capacitor in a physical circuit thus adds additional parasitics determined by the design and mounting of the component. It is usually attempted to have a *snug* fit of the capacitor on the transmission line without it protruding over the transmission line edges. When doing a design one should try and *force* the use of a specific capacitor such as the D10 (0.254 × 0.254 × 0.1012 mm) sized 51 pF capacitor from *DiLabs*. Figure 3.4 shows a *snug* fit of the coupling capacitor on the transmission line.

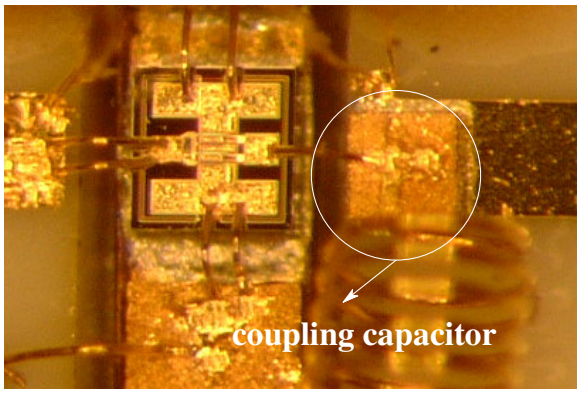


Figure 3.4: Physical implementation of coupling capacitor

Another important aspect is whether this capacitor introduces any resonance within the proposed 2-18 GHz operating band. Figure 3.5 shows the expected response of a 51 pF capacitor for use as a coupling capacitor. The seen IL and RL over the 2-18 GHz frequency band is very low with the *resonant* trough at 9.5 GHz not having a significant influence on transmission. Practical experience showed that one should try and prevent the use of exactly similar capacitors, especially to prevent undesired complementing effects. The seen *resonant* trough, although not serious when considering a single capacitor, will be more prominent when considering multiple capacitors.

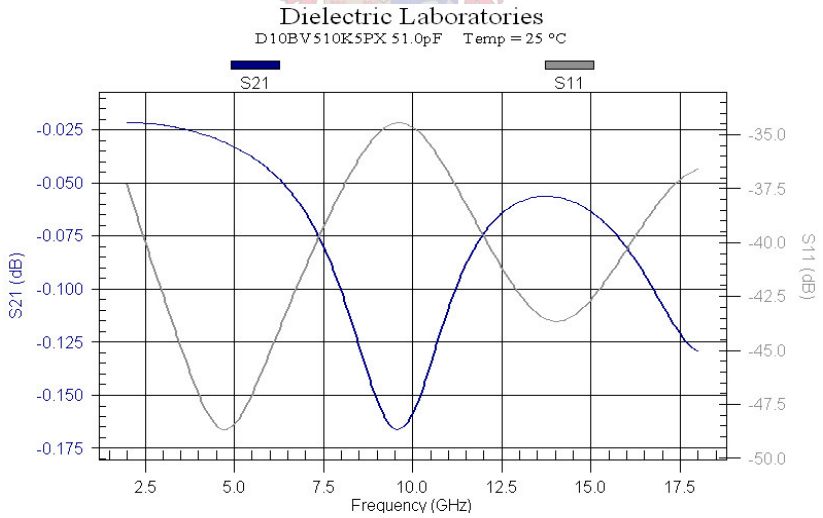


Figure 3.5: Simulated chip capacitor response

The other important consideration for the capacitors to be used in a design is their response over temperature. Figure 3.6 shows typical capacitance variation with temperature for two arbitrary dielectric materials. This figure also shows the physical size constraints of capacitors having these dielectric materials, for some arbitrary capacitance of 51 pF.

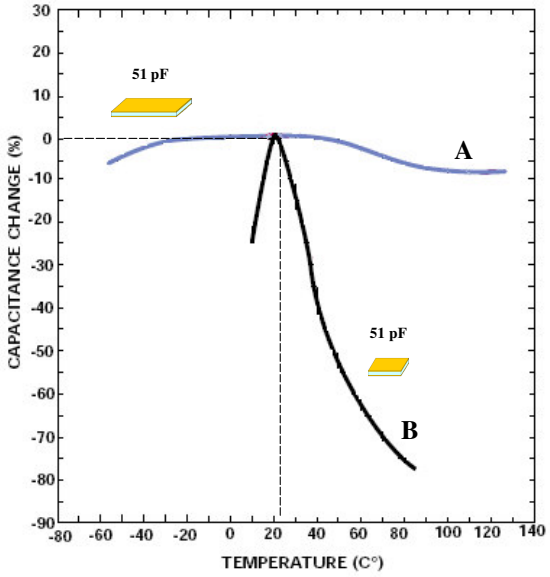


Figure 3.6: Capacitance variation as function of temperature

A capacitor with dielectric material **A** will offer the best response over temperature. It offers very little capacitance variation around its nominal capacitance at room temperature. On the downside, however, compared to a capacitor with the same capacitance, but with dielectric material **B**, this capacitor will be physically larger in size. A capacitor with dielectric **B** will be physically smaller but will have a large capacitance variation over temperature.

In a practical design there is thus a trade-off between physical size, capacitance and capacitance variation over temperature. Physical size however is the biggest deciding factor in choosing a capacitor and one therefore has to settle for the large capacitance variation over temperature. The only time that a capacitor offering less capacitance variation over temperature can be used is when the physical transmission line dimensions in the circuit design allows for it.

3.4.3 INDUCTORS

Figure 3.7 shows a typical air-core inductor for use in a broadband RF amplifier. Of interest, is that the shown air-core inductor measures only a few tenths of a millimetre in length.

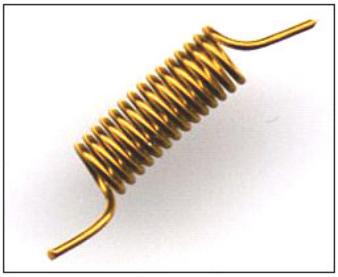


Figure 3.7: Air-core inductor

For use as a bias inductor, the *rule of thumb* is that the impedance presented by this inductor must be at least ten times that of the characteristic 50 Ω impedance. The calculation shown hereafter is used to determine the required inductance at 2 GHz. Thus,

$$\omega L = 10Z_0 \tag{3.1}$$

The value of the bias inductor can thus be determined as follows:

$$L = \frac{10Z_0}{\omega} = \frac{10Z_0}{2\pi f} = \frac{10(50)}{2\pi(2\times10^9)} \approx 40\ nH \tag{3.2}$$

The formula for inductance calculations, in terms of the physical dimensions shown in Figure 3.8, is given by:

$$L = \frac{17n^{1.3}[0.0394(cd+wd)]^{1.7}}{[0.0394(wd+s)]^{0.7}} \tag{3.3}$$

where L is the nominal inductance in nH, n is the number of turns, cd is the coil diameter in mm, wd is the wire diameter in mm and s is the space between turns in mm [19].

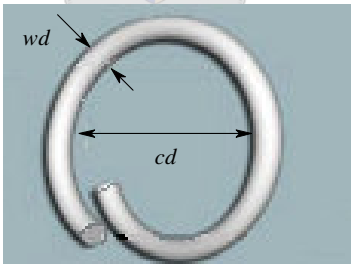


Figure 3.8: Inductor physical dimensions

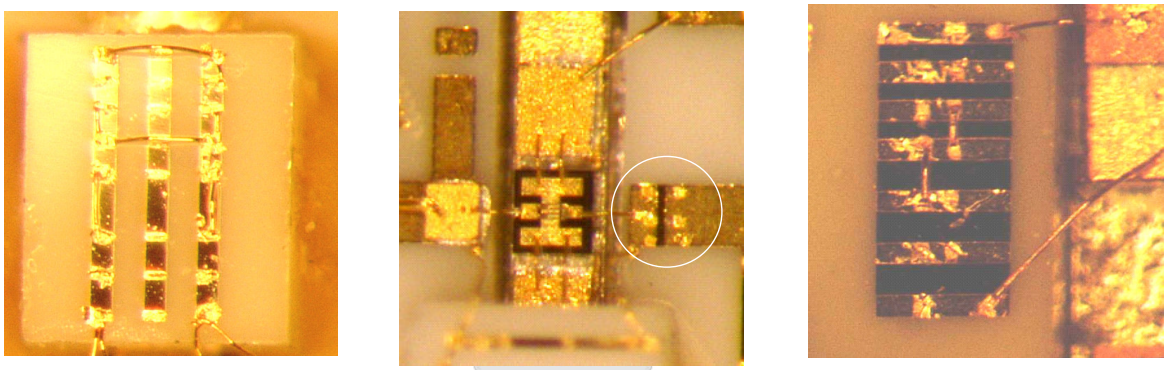
The inductor typically used for 2-18 GHz amplifier designs consists of 10 turns, has a wire diameter of 0.036 mm, an inside diameter of 0.381 mm and a spacing between turns approximately equal to the wire diameter. Using these known parameters in equation (3.3), the nominal inductance is determined to be approximately 20 nH. It is seen that this inductance is half of that calculated in equation (3.2) with the resulting impedance at 2 GHz being only 5 times that of the characteristic impedance. The inductance can be increased by increasing the amount of turns, but one may then risk the introduction of resonance within the operating band. The inductor, with dimensions as mentioned, however proved to be

resonance free over the 2-18 GHz bandwidth; this being said after practical implementation and confirming resonance free operation.

Although the impedance of the bias inductor is lower than that calculated, the inclusion of the drain resistor as part of the bias network ensures a high impedance combination that should not influence the propagation of the RF signal. Above 2 GHz, the impedance of the inductor-resistor combination will, however, increase to well above the specified impedance.

3.4.4 RESISTORS

Resistors used in the RF amplifier are implemented as etched thin-film resistive layers. The resistance of this etched resistive layer is very stable over temperature, as was pointed out in the previous chapter, and eliminates the parasitics and losses associated with a surface mount resistor. The etched resistors fulfil three purposes namely feedback resistors, stabilizing resistors and bias resistors. The physical implementation of these resistors is shown in Figure 3.9.



(a) feedback resistor **(b) stabilizing resistor** **(c) bias resistor**

Figure 3.9: Physical implementation of thin-film resistors

The feedback resistor is implemented on a small Alumina substrate with its rear metallization etched away. This implementation offers a feedback path with insignificant parasitics. The stabilizing resistor is etched in-line with the transmission line as seen in (b). The bias resistor is implemented as a resistive ladder. Resistors not needed are shorted out with wire bonds as seen in (c).

With the most prominent components used in RF amplifiers designs discussed, one may proceed to discussing the actual amplifier designs that were done for purposes of this study. The following section discusses the single-stage 2-18 GHz amplifier design that was used in the final limiting amplifier.

3.5 DESIGN OF A SINGLE-STAGE 2-18 GHz AMPLIFIER

Before attempting the desired broadband design, two narrow-band amplifier designs were attempted. These narrow-band designs, which included a 50 MHz amplifier designed for maximum gain and a 3.6-4.3 GHz low-noise amplifier, are discussed in Appendix B. These designs offered the opportunity to apply acquired theoretical knowledge, to gain the necessary RF amplifier design experience and to gain confidence in the available computer-aided design software. After successful completion of these designs a more challenging design, in the form of a single-stage 2-18 GHz amplifier, could be attempted.

Appendix C offers a detailed discussion of the design procedure of a single-stage 2-18 GHz amplifier. Focus is placed on the *MultiMatch* design procedure and the implementation of the design in MWO. Measurements compared well with simulated results and showed to what extent the two design packages could be used for accurate RF amplifier designs. This design was the first attempted broadband design, but was not considered for use in the final limiting amplifier. Its modification network included an inductive element that proved extremely sensitive to physical tolerances during implementation. For this reason, an alternative amplifier had to be designed. This improved design, discussed hereafter, was used in the final limiting amplifier design.

Design criteria were for optimum gain, gain flatness, output compression and input/output VSWR. The active device chosen for this design was the NE321000 from *NEC*. The main consideration in choosing this device was the availability of a nonlinear model for it. The design approach for doing this design was similar to that discussed in Appendix C. The resulting design is discussed hereafter.

3.5.1 THE DESIGNED 2-18 GHz AMPLIFIER

Figure 3.10 shows the schematic layout of the design as done in MWO while Figure 3.11 shows part of the physical assembly of the designed 2-18 GHz amplifier. From the schematic layout one may visually establish how good a representation this design was of the physically implemented design. Only through practical evaluation, however, would one be able to distinguish the true accuracy of the simulated design.

The physical assembly shows the implementation of the feedback network and the impedance matching networks of this single-stage design. Also visible is the implementation of the thin-film resistors as part of these networks. The foregoing discussion on the most common RF components allows one to identify the other components comprising the design.

Included in the shown design are extra stubs to allow for tuning after actual manufacturing. These stubs are generally placed at transitions and steps in the transmission line to compensate for possible mismatches. The stubs also allow for varying the length of open circuited stubs for intended improved impedance matching. The implementation of these tuning stubs is decided upon in the MWO design environment. The amplifier response is typically monitored in response to varying the stub dimensions. In doing this, one may decide on some nominal length which offers the ideal simulated response and from there include extra stubs as required. Typically only the length of stubs is adjusted in this way. Lengths of interconnecting wire bonds and ribbons are typically not used for tuning purposes and are kept to a minimum.

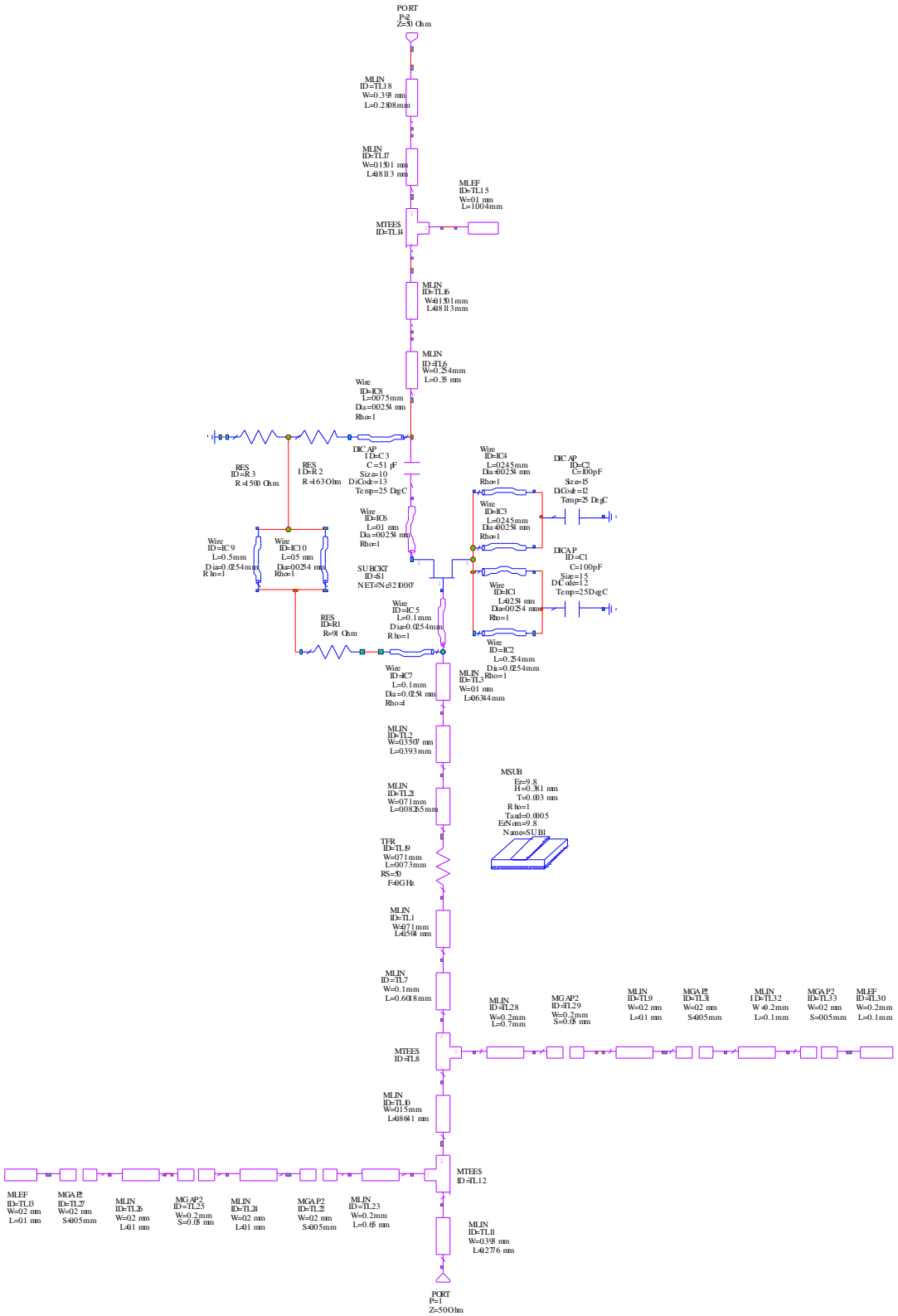


Figure 3.10: Schematic layout of the designed 2-18 GHz amplifier

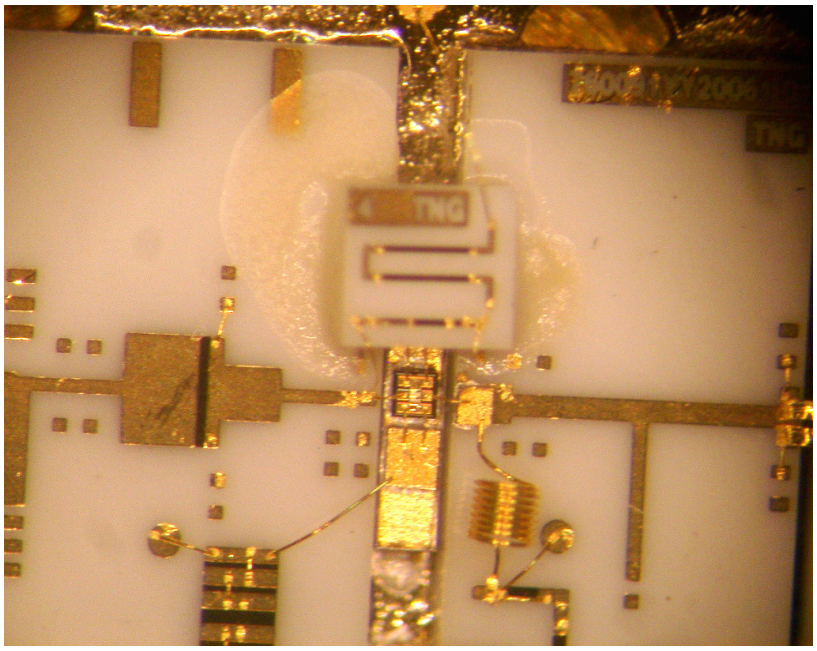


Figure 3.11: Part of the single-stage 2-18 GHz amplifier assembly

Shown in Figure 3.11 is the passive bias network of the device as mentioned before. It can be seen that some of the thin-film resistors have been shorted out; indicating that the amplifier's bias point was already set. The circular pads seen were etched for the specific purpose of probing for bias voltage measurements.

While the previous discussion provides useful insight as to the design and implementation of the RF amplifier, the true test of the design lies in its physical evaluation. In the sections to follow, a result summary is given that compares the response of the simulated design with that of the physical measured response.

3.5.2 RESULT SUMMARY

In this section the single-stage 2-18 GHz design that was done, is evaluated in terms of simulated and measured results. The simulated results as obtained with MWO are shown in Figure 3.12. The results show a moderate gain of about 7.3 dB with input return loss being better than 10 dB over the whole 2-18 GHz frequency band. The output return loss is seen to be typically better than 15 dB. The gain flatness is particularly good at ± 0.3 dB.

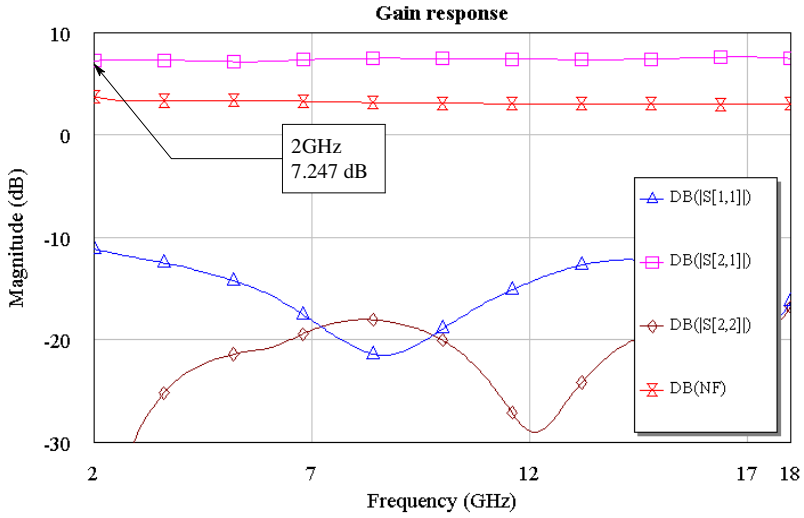


Figure 3.12: Simulated response of single stage 2-18 GHz amplifier

The actual measured response of the 2-18 GHz amplifier is shown in Figure 3.13 Only the gain response and the input return loss is shown in this result. The output return loss was simulated to be at least 15 dB while the measured result was not expected to deteriorate much from this value.

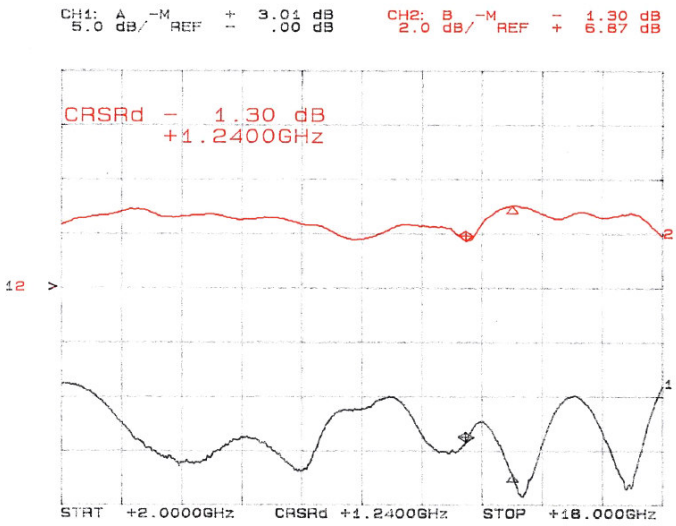


Figure 3.13: Measured response of the single stage 2-18 GHz amplifier

From the measured and simulated results one can see a close correlation but there is, however, a slight difference. The measured gain was higher than what was obtained with simulation and the measured return loss was poorer than simulated. The main reason for this deviation was due to a bias point that was higher than it was supposed to be. The design was done

using a set of S-parameters obtained at a specific bias point and for practical implementation it is important to keep the actual bias point close to this bias point of measurement. Not simulated were transitions that were included in the actual amplifier test jig. These transitions could further deteriorate the measured gain ripple and the return loss; however only to a lesser extent if implemented properly. Table 3.1 gives a summary of the worst-case measured results for comparison with simulations. Simulations did not take into account temperature variations.

Temperature	**- 54 °C**	**25 °C**	**85 °C**
Ripple (dB)	± 0.74	± 0.7	± 0.65
Input Return Loss (dB)	8.3	8.4	8.5
P_{1dB} (dBm)	*	7.5	*
Gain (dB)	9.3	9	8.9

Table 3.1: Summary of measured results

The designed amplifier was easily implemented and showed the extent to which actual measurements compared with simulated results. Unlike the design discussed in Appendix C, this design did not have a critical element as part of the design. Such a critical element can typically not be manufactured within strict enough tolerances and should best be avoided. The designed single-stage 2-18 GHz amplifier offered reasonably good results and will be shown to form part of the final limiting amplifier design. It will also be shown how this design was altered and optimized for optimal use within the limiting amplifier's RF chain. The section to follow further discusses broadband amplifier design and focuses on some important considerations that need mentioning.

3.6 BROADBAND AMPLIFIER DESIGN

3.6.1 COMPENSATED IMPEDANCE MATCHING AND NEGATIVE FEEDBACK

The bandwidth specification of an amplifier directly influences design complexity. In doing a 2-18 GHz amplifier design there are quite a few considerations. The matching networks become much more involved and require the use of computer-aided design methods. The technique of compensated matching networks is used and involves mismatching the input and output matching networks to compensate for changes in $|S_{21}|$ with frequency [2].

As the bandwidth requirements of the amplifier approach a decade of frequency, a combination of both negative feedback and compensated impedance matching offer the optimal solution for such a design [9]. The foregoing discussion on the single-stage 2-18 GHz amplifier showed how both negative feedback and compensated impedance matching were used to realize the design. Negative feedback was used to flatten the gain response, improve the input and output match and improve device stability. Negative feedback increases the bandwidth of an amplifier but with a corresponding reduction in gain [20]. On the downside, degradation in noise figure and reduction in gain is thus caused when negative feedback, is implemented.

3.6.2 BALANCED AMPLIFIERS

A possible solution to the mismatched input or output of an amplifier, resulting from a requirement such as bandwidth improvement or low noise is the use of a balanced amplifier. Balanced amplifiers offer a practical method for implementing a broadband amplifier that has a flat gain response and good input and output VSWR [17]. Although a balanced amplifier was not used in the final limiting amplifier design, it was deemed necessary to highlight some of the interesting properties of this amplifier. Figure 3.14 shows the basic balanced amplifier configuration using two identical amplifiers cascaded between two hybrid couplers.

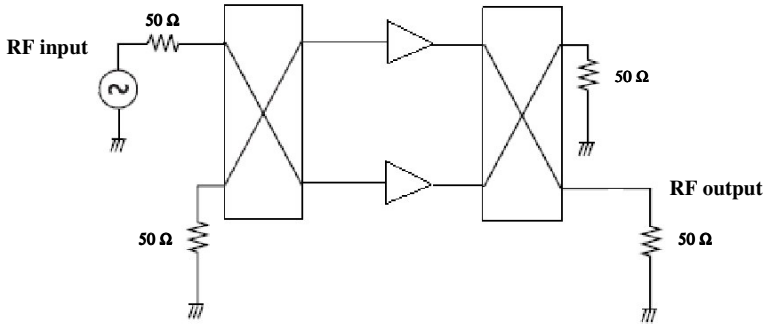


Figure 3.14: Balanced amplifier configuration.

The balanced amplifier shown in Figure 3.15 is analyzed by exciting the input port with a phasor which was chosen as $1\angle 0°$ for simplicity. Two identical amplifiers with gains of $A\angle\theta°$ are used between two ideal hybrid couplers. The input wave emerges from the direct port of the input coupler with a value of $0.707\angle -90°$ (a 90° phase delay is introduced on the direct port) and enters the bottom amplifier where it is amplified to give a value of $(0.707A\angle\theta° - 90°)$. The input wave emerges from the coupled port of the input coupler with a value of $0.707\angle 0°$ and enters the top amplifier where it is amplified to give a value of $0.707A\angle\theta°$.

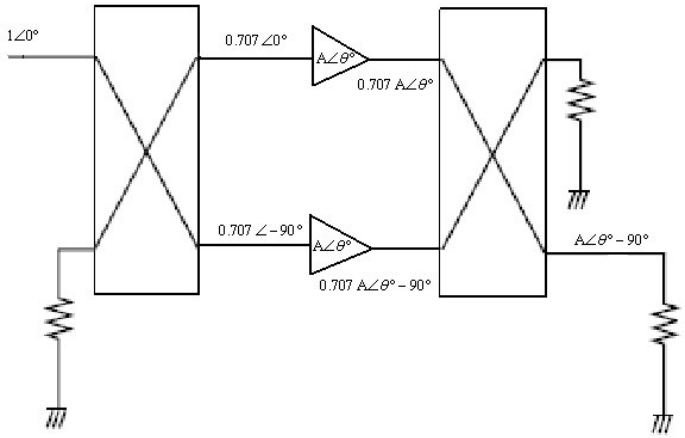


Figure 3.15: Balanced amplifier phasor analysis

Figure 3.16 shows the recombination of the amplifier outputs to give the output of $(A\angle\theta° - 90°)$. At the terminated port the contributions from the two amplifiers cancel out. No power is thus lost in the coupler terminations. The terminations do, however, absorb power which is reflected from the input and output ports of the individual amplifiers.

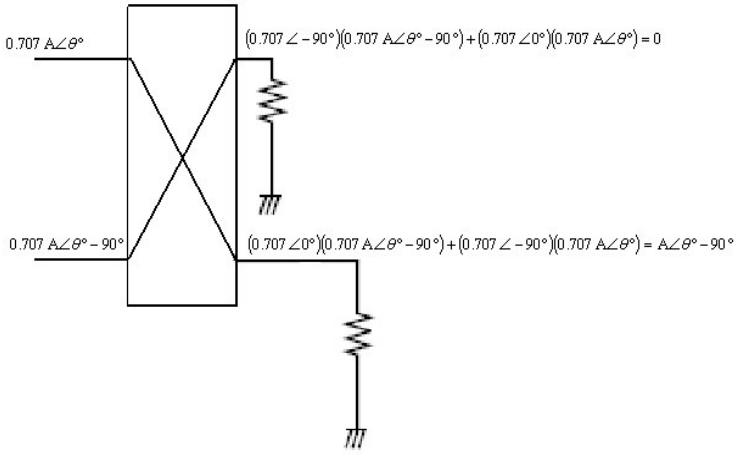


Figure 3.16: Balanced amplifier gain analysis

In the configuration shown in Figure 3.17 a portion of the input signals get reflected with an arbitrary phase shift, β. The reflected signals are $(0.707\alpha\angle 0° + \beta°)$ and $(0.707\alpha\angle -90° + \beta°)$ respectively.

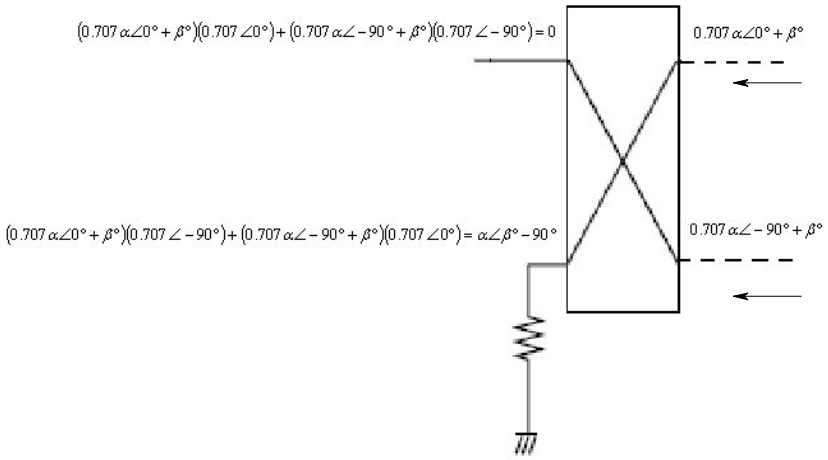


Figure 3.17: Analysis of the reflections from amplifiers

The reflected power cancels at the input port of the balanced amplifier, but adds at the terminated port. This is true at the output port of the balanced amplifier as well. The assumption is made that the configuration is ideal and that the amplifiers

are identical. If the amplifiers are not identical, all the reflected power will not cancel at the input and output ports of the amplifier and some of the reflected power will be seen at these ports.

Another non-ideal effect that should be taken into account is electrical line lengths different to 90°. This effect will be seen when the balanced amplifier is operated over broader bandwidths. The power split of the couplers will deteriorate at frequencies different to the design frequency. The unequal power split of the couplers will then also influence the gain response of the balanced amplifier.

The bandwidth restriction of the hybrids used in the balanced amplifier is one of the main reasons why balanced amplifiers were not considered for implementation from 2-18 GHz. If the hybrid were to operate from 2-18 GHz, its size would pose a definite problem. To evaluate the bandwidth restrictions opposed to physical size, the branch-line coupler was investigated for possible use in a balanced amplifier. This investigation is summarized in Appendix D.

The question remaining is why the balanced amplifier will be especially useful in a limiting amplifier configuration. The answer to this question will become apparent during the discussion in the section to follow, but also during the evaluation of the final designed limiting amplifier and the RF amplifiers that form part thereof.

3.6.2.1 THE ADVANTAGES OFFERED BY THE BALANCED AMPLIFIER

The balanced amplifier offers quite a few advantages. The output power is twice that obtained with a single amplifier. Assuming no loss in the couplers, the noise figure is typically the same as that of the individual amplifiers while the balanced amplifier also offers improved third-order intermodulation [22]. Significant spurious- and harmonic-rejection may be achievable through the use of 180° hybrids [9]. It will be shown that if the phase and amplitude balance of the hybrid is uniform over a wide frequency range; it is possible for the balanced structure to have significant spurious rejection. A derivation is done hereafter to show the spurious rejection properties of the balanced structure implementing 180° hybrids. Figure 3.18 shows a balanced amplifier configuration implementing 180° hybrids.

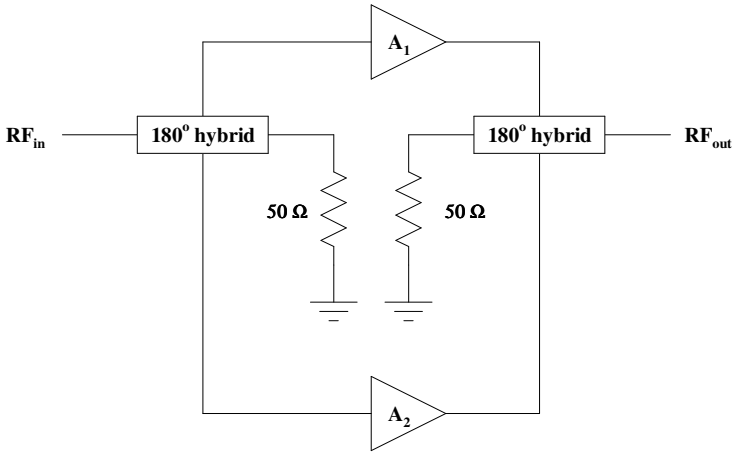


Figure 3.18: Balanced amplifier configuration implementing 180° hybrids

It is assumed that the amplifiers are identical, have unity gain and can be described by the expression: $V_{out} = a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3$. The excitation signal is a two-tone signal V_{in}.

$$V_{in} = V_1 \angle \theta_1 + V_2 \angle \theta_2 \tag{3.4}$$

The expression at the output of amplifier A_1 due to the second order non-linearity is as follows:

$$V_{out1} = a_2 \left[V_1 \angle \theta_1 + V_2 \angle \theta_2 \right]^2 = a_2 \left[V_1^2 \angle 2\theta_1 + V_2^2 \angle 2\theta_2 + 2V_1 V_2 \angle (\theta_1 + \theta_2) \right] \tag{3.5}$$

The expression at the output of amplifier A_2 due to the second order non-linearity is as follows:

$$\begin{aligned} V_{out2} &= a_2 \left[V_1 \angle (\theta_1 + \pi) + V_2 \angle (\theta_2 + \pi) \right]^2 \\ &= a_2 \left[V_1^2 \angle (2\theta_1 + 2\pi) + V_2^2 \angle (2\theta_2 + 2\pi) + 2V_1 V_2 \angle (\theta_1 + \theta_2 + 2\pi) \right] \end{aligned} \tag{3.6}$$

It can be seen from the two derived expressions that both V_{out1} and V_{out2} are the same. If V_{out2} now undergoes an additional 180° phase shift through the hybrid on the output of the balanced configuration, all the second order voltages will cancel at the output. In the same way it can be shown that all the even-order harmonics and intermodulation products will be suppressed ([9], [22]).

The ideal setup would obviously be where one has a balanced amplifier configuration with two hybrids offering a 180° phase shift over the complete 2-18 GHz bandwidth. These types of couplers (not necessarily hybrids) are asymmetrical couplers that have the unfortunate characteristic that the phase shift between the two output ports is frequency dependent.

As an example, measurements were done on an asymmetrical 6-18 GHz 10 dB coupler to show the frequency dependent phase shift between the coupler output ports. Figure 3.19 shows the measurement on the *through path* of the coupler, where it is seen that the transmission loss is practically negligible.

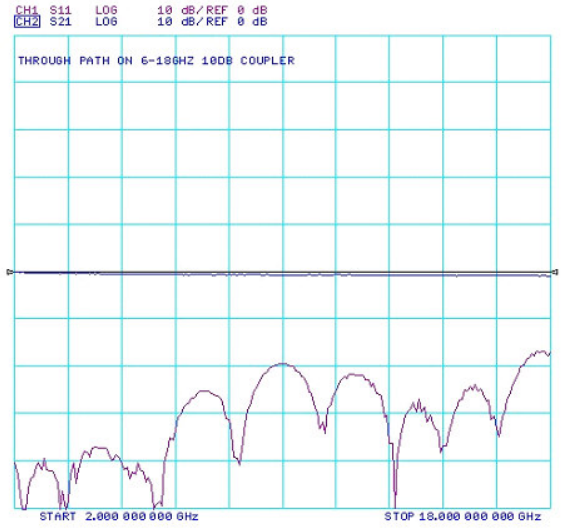


Figure 3.19: Through path measurement on coupler

Shown hereafter are plots of the coupled path response for the 6-18 GHz 10 dB coupler, the phase response of the two output ports and the phase difference between the output ports. Figure 3.20 shows the measured coupled path response, which clearly shows the out-of-band roll-off.

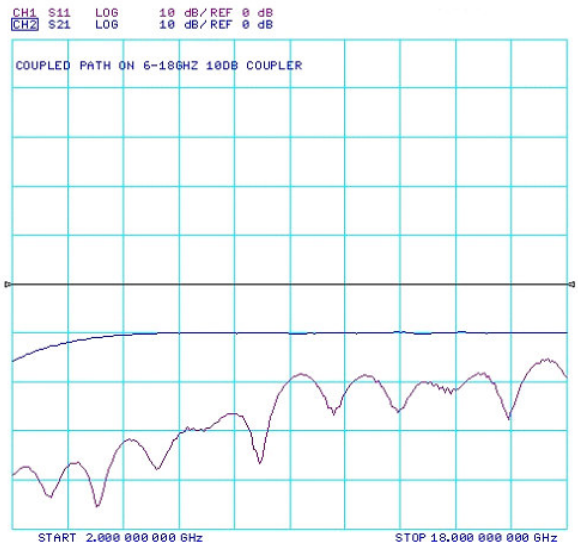


Figure 3.20: Coupled path response

Figure 3.21 shows the phase response of the two output ports. Important to observe from this plot is the fact that the phase difference between the two traces vary with frequency. To better quantify this phase difference, a single phase difference measurement such as that shown in Figure 3.21, can be made.

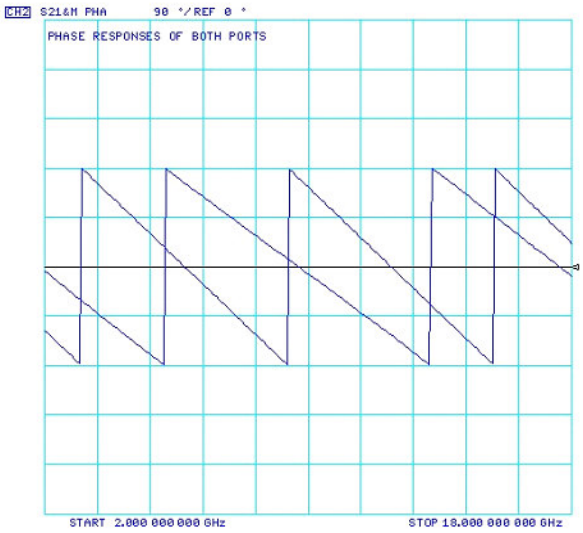


Figure 3.20: Phase response of the output ports

Figure 3.21: Phase difference between output ports

From Figure 3.21 it can be seen that the phase difference between the two output ports is not constant and varies over frequency. This measurement is done by using the VNA's data-divide-by-memory function (phase is selected as measurement). The one output port's response is saved in memory and the other port is the actual current measured port.

For interest sake, the same measurements were done on a 90° hybrid coupler. This coupler is symmetrical and it is expected that the phase difference between the two output ports will be constant over frequency. Figure 3.22 shows the response of a 3 dB quadrature coupler as measured on the coupled port. The measured response shows the expected 3 dB insertion loss response with its associated ripple.

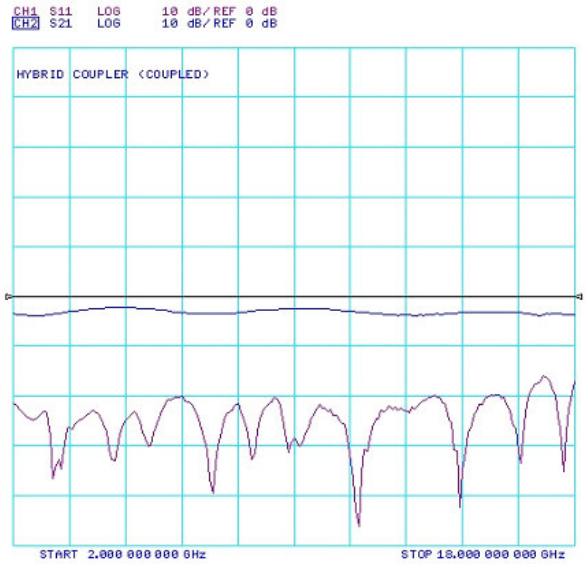


Figure 3.22: Typical response of a 3 dB quadrature coupler

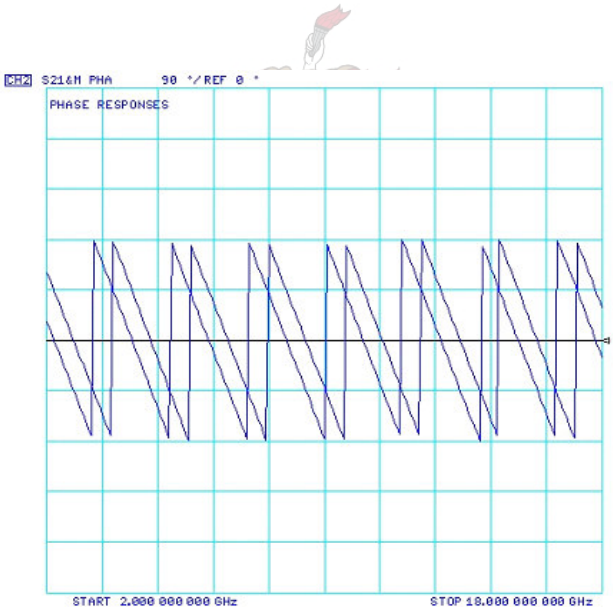


Figure 3.23: Phase response of the two output ports

Figure 3.23 shows a uniform phase relation between the coupler output ports. Figure 3.24 shows the phase difference measurement (data-divide-by-memory) resulting in a constant 90° phase shift between the two output ports, independent of frequency.

Figure 3.24: Phase difference between two output ports

It was shown that significant spurious rejection can be achieved in a balanced amplifier configuration when using 180° hybrids. It was, however, shown that the phase shift between the output ports are frequency dependent, opposed to the quadrature hybrid that has a constant 90° phase shift, independent of frequency. Other advantages of balanced amplifiers include optimization of individual amplifiers for gain flatness or noise figure, without much concern for input and output matching. The balanced amplifier is easy to cascade and offers improved stability. Should one of the amplifiers fail, the gain of the balanced amplifier will drop by only 6 dB [23]. Balanced amplifier design principles are also useful in simplifying the cascading and control of harmonic content of the limiting amplifier [39].

The balanced amplifier does however offer some disadvantages as well. Broadband operation is limited to the bandwidth of the hybrid used in the balanced amplifier configuration. Two amplifiers are used with increased DC power consumption. The balanced amplifier is physically larger than a single amplifier and hybrids introduce insertion losses that influence the balanced amplifier gain.

3.7 DEVICES USED FOR IMPROVED IMPEDANCE MATCHING

An alternative to the balanced amplifier is the use of isolators and circulators to realize a matched input and output [22]. These devices were further evaluated for their most significant property namely, its unidirectional transmission characteristics. The S-matrix for an ideal isolator has the form:

$$[S]=\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}=\begin{bmatrix} 0 & 0 \\ 1 & 0 \end{bmatrix} \tag{3.7}$$

The S-matrix shows that both ports are matched and that transmission occurs only in the forward direction. Power reflected from the load gets absorbed by the isolator. An isolator would thus be ideal to provide isolation between heavily saturated gain stages and prevent interstage reflections.

A circulator on the other hand is a device that can be used as an isolator when one of its ports is terminated with a matched load. A circulator has an S-matrix as shown by expression (3.8). Termination of one of the circulator ports would thus give an equivalent S-matrix as that shown for the isolator.

$$[S]=\begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix}=\begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \tag{3.8}$$

Figure 3.25 shows the representation of a circulator.

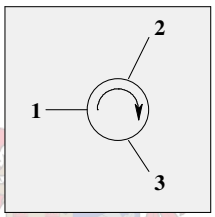


Figure 3.25: Circulator representation

Shown in Figure 3.26 are two typical isolators (circulators with terminated ports). The limitations in using these isolators between amplifiers are their physical size and bandwidth.

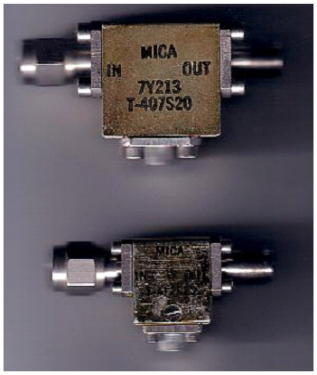


Figure 3.26: Typical isolators

Measurements were made to establish a better intuitive feel for the bandwidth of these components. These measurements are shown in Figure 3.27. It is seen that transmission occurs only in the forward direction ($S_{21} = 1$) and that both ports are well matched only over a limited operating frequency band. The reverse transmission is very small as expected.

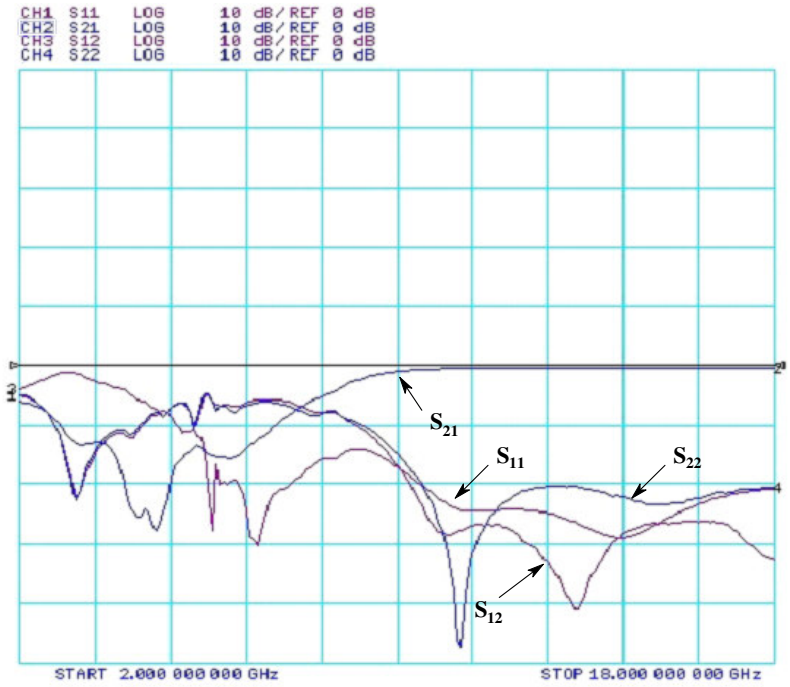


Figure 3.27: Measured isolator response

The isolator's unidirectional transmission is a very significant property that can unfortunately not be utilized over the complete 2-18 GHz bandwidth. Should size and bandwidth specifications allow for it; this component may prove very useful in a proposed limiting amplifier design.

In the sections to follow, some other RF amplifier considerations are investigated to establish valuable practical experience in dealing with the RF amplifier. The acquired knowledge allows one a far better intuitive feel of what to expect from the RF amplifier under certain operating conditions. Of particular importance is the RF amplifier's response over temperature and the significance of biasing for proper operation.

3.8 GAIN VARIATION OVER TEMPERATURE

The problem with RF amplifiers employing GaAs technology is their gain variation over temperature. The gain of the RF amplifier will vary by approximately - 0.001 dB/°C, for every dB of gain [24]. Depending on the application, this gain variation over temperature might not be desirable.

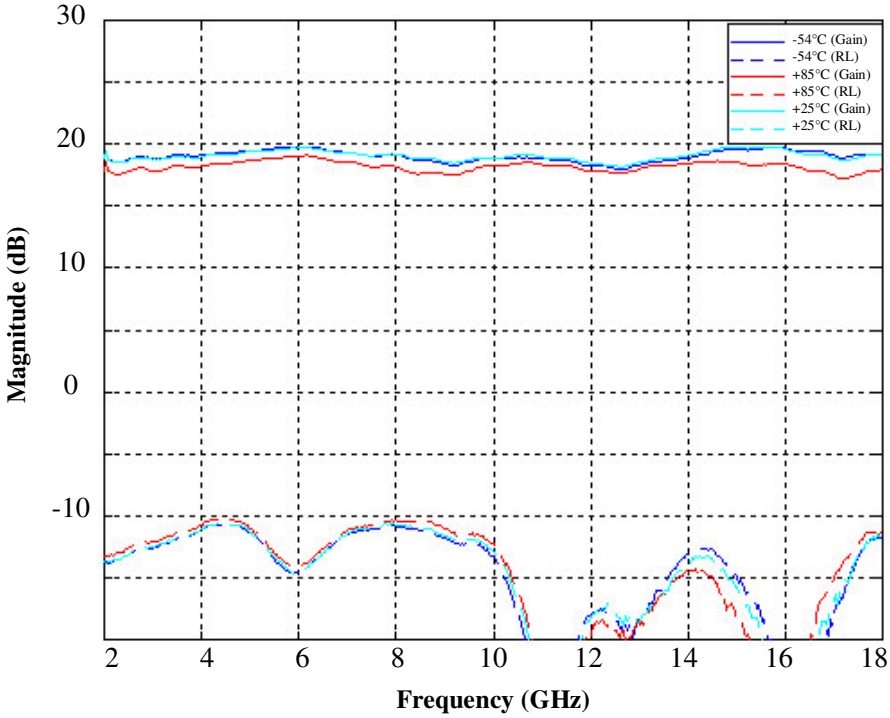


Figure 3.28: Gain response of amplifier over temperature (passive biasing)

Figure 3.28 shows the typical gain response of a two-stage 2-18 GHz amplifier as measured at - 54 °C, 25 °C and 85 °C, with a passive biasing configuration used. From this measured response, it is seen that the gain at 85 °C is a few dB lower than at 25 °C and - 54 °C. In a practical limiting amplifier, which consists of multiple gain stages, the drop in gain at high temperature will be more pronounced. This may deteriorate the device's input dynamic range since the small-signal gain may be too small to drive the last amplifier into compression.

Also seen from Figure 3.28 is that the gain at - 54 °C is close to that at 25 °C, while one may have expected a higher gain at this temperature. The reason for this is that the tested RF amplifier also included components such as coupling capacitors of which the capacitance varies quite a bit over temperature. As mentioned earlier, the type of capacitors used becomes very *lossy* when not operated at room temperature (25 °C) and will therefore counter the expected increase in gain at low temperatures. At high temperatures the effect of these capacitors adds to the effect of the GaAs FET devices so that an overall deteriorated gain is observed. Temperature compensation as achieved with active biasing or with passive temperature variable attenuators is discussed in the sections to follow.

3.9 TEMPERATURE VARIABLE ATTENUATORS

An attractive form of temperature compensation comes in the form of a temperature variable attenuator (TVA). The attenuation characteristic of the device varies in response to the device temperature while keeping the characteristic impedance constant. Because the device is passive, distortion products are not generated. Complex temperature control circuitry can be avoided when using TVA's or so-called *thermopads*.

Typically, a TVA is identified by its attenuation value at room temperature (25 °C) and its temperature coefficient of attenuation (TCA). The TCA is the change in attenuation with respect to temperature from its nominal attenuation at room temperature. A 15 dB amplifier's gain would change with - 0.015 dB/°C. The amplifier's gain can be compensated over temperature by cascading it for example with a 3 dB TVA with a TCA of - 0.005 dB/dB/°C (- 0.015 dB/°C). As the temperature increases, the gain of the amplifier will tend to decrease. At the same time, however, the TVA will offer less attenuation as the temperature increases and thereby introduce the desired temperature compensation.

Figure 3.29 shows the expected gain response of an amplifier over temperature after the inclusion of temperature compensation. The nominal gain is dropped due to the attenuation introduced by the TVA. This attenuation may be beneficial in providing isolation and improved interstage matching between the gain stages in a multi-stage amplifier configuration. These TVA's may also comfortably form part of a limiting amplifier employing the proposed attenuator-amplifier configuration. Temperature variable attenuators thus offer a good option for providing temperature compensation in RF amplifiers and a limiting amplifier for that matter.

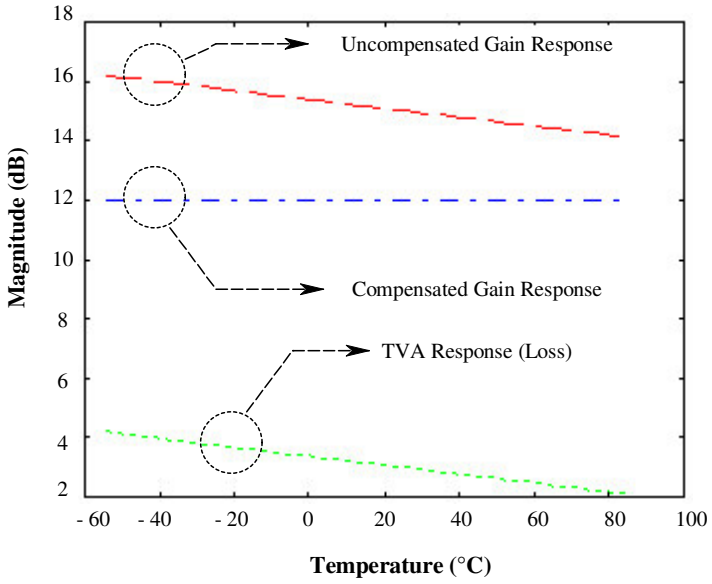


Figure 3.29: Temperature compensation using a TVA

3.10 THE SIGNIFICANCE OF BIASING

Considerable effort is normally put into the design of an amplifier for given performance like gain, bandwidth, noise etc. Another important aspect of the design, however, is the proper selection of a DC biasing network. The DC bias network sets the operating point for the active device in question and holds it constant over variations in device characteristics and temperature. A properly designed bias network will not influence the RF response of an amplifier.

Figure 3.30 shows a general passive biasing configuration together with its physical implementation. This passive bias configuration will be seen in the amplifier designs discussed in this thesis and will be seen as part of the final designed limiting amplifier as well.

The coupling capacitors C_1 and C_2 should offer low insertion loss and return loss so as not to influence signal transmission. These capacitors also function as DC blocking capacitors especially to protect sensitive measurement equipment for testing the amplifier. Capacitor C_s functions as a bypass capacitor that provides the active device with a proper RF ground. The bias inductor L_d in combination with the drain bias resistor R_d should present a high impedance so as not to load the RF circuit with 50 Ω characteristic impedance. Ideally, the bias inductor will appear as an open circuit to an RF signal while capacitors will act as short circuits to an RF signal.

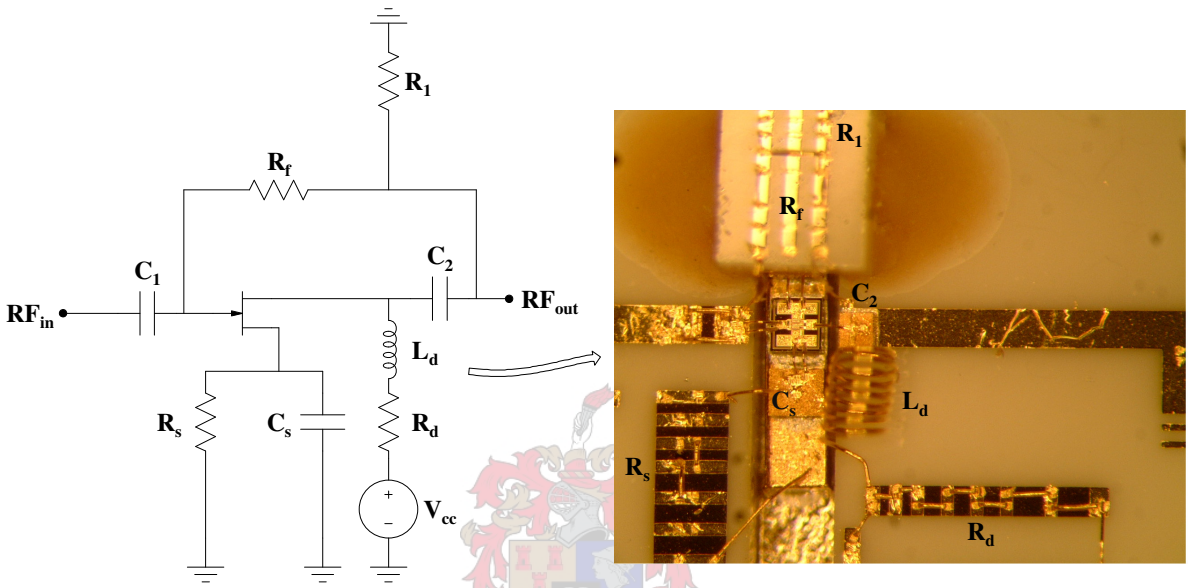


Figure 3.30: General passive biasing configuration with physical implementation

The resistor R_f, as shown in Figure 3.30, is a feedback resistor that will typically form part of a broadband amplifier design. R_f , together with resistor R_1 provides a large gate grounding resistor to ensure a zero gate voltage. An alternative to the discussed passive bias configuration is active biasing. The section to follow, offers a comparative evaluation between active and passive biasing.

3.11 ACTIVE VERSUS PASSIVE BIASING

Active biasing is evaluated hereafter as an alternative to passive biasing. An experiment was done in SPICE, to get a better intuitive feel for bias point variation over temperature in GaAs FETs. Three bias configurations were evaluated to determine which would offer the least bias point variation over temperature. Although there are many bias configurations, the ones discussed are probably the more prominent. SPICE implements models with temperature being one of the variable transistor parameters and allows for swept temperature measurements. A SPICE parametric analysis was set up and the temperature was varied from - 40 °C to 80 °C in 20 °C steps. The drain current variation over temperature was then monitored. Figure 3.31 shows the three bias configurations that were evaluated. The 2N3819 JFET and 2N2907A BJT were used for simulations with the bias set to approximately 5 V, 5 mA for each of the configurations.

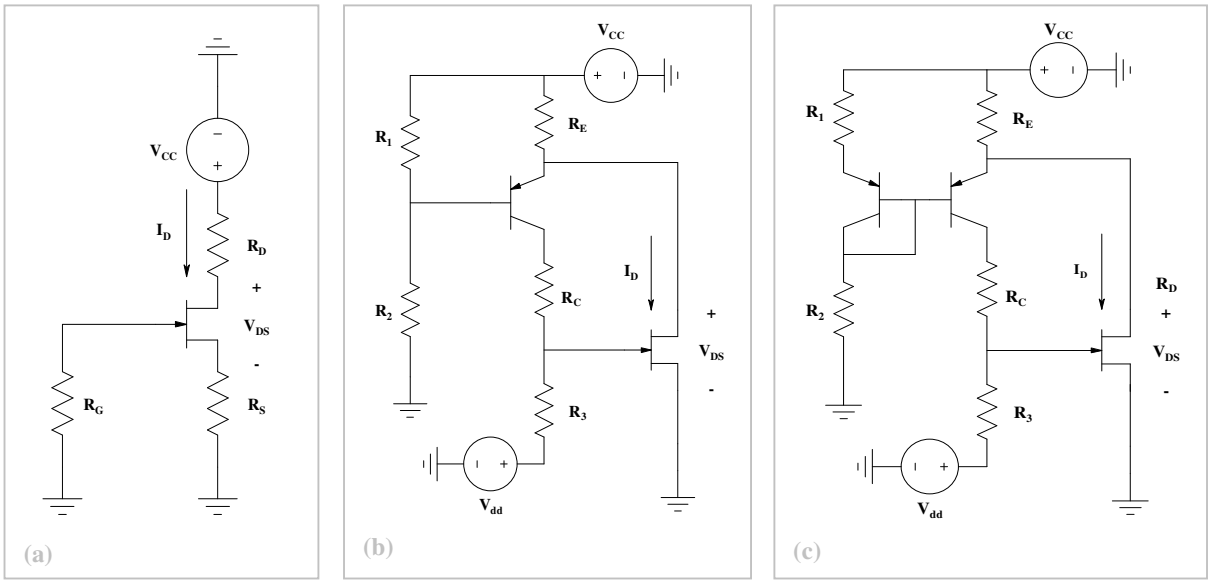
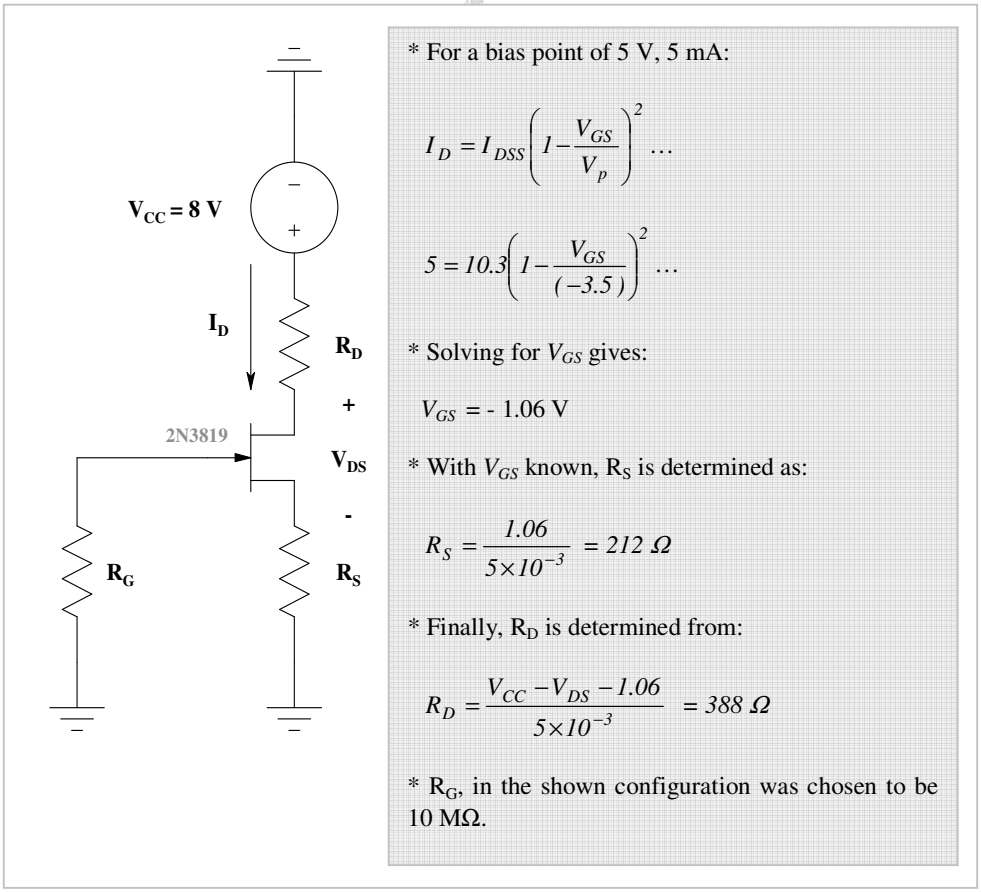


Figure 3.31: Bias configurations for evaluation



* For a bias point of 5 V, 5 mA:

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)^2 \ldots$$

$$5 = 10.3\left(1-\frac{V_{GS}}{(-3.5)}\right)^2 \ldots$$

* Solving for V_{GS} gives:

V_{GS} = - 1.06 V

* With V_{GS} known, R_S is determined as:

$$R_S = \frac{1.06}{5\times10^{-3}} = 212\ \Omega$$

* Finally, R_D is determined from:

$$R_D = \frac{V_{CC} - V_{DS} - 1.06}{5\times10^{-3}} = 388\ \Omega$$

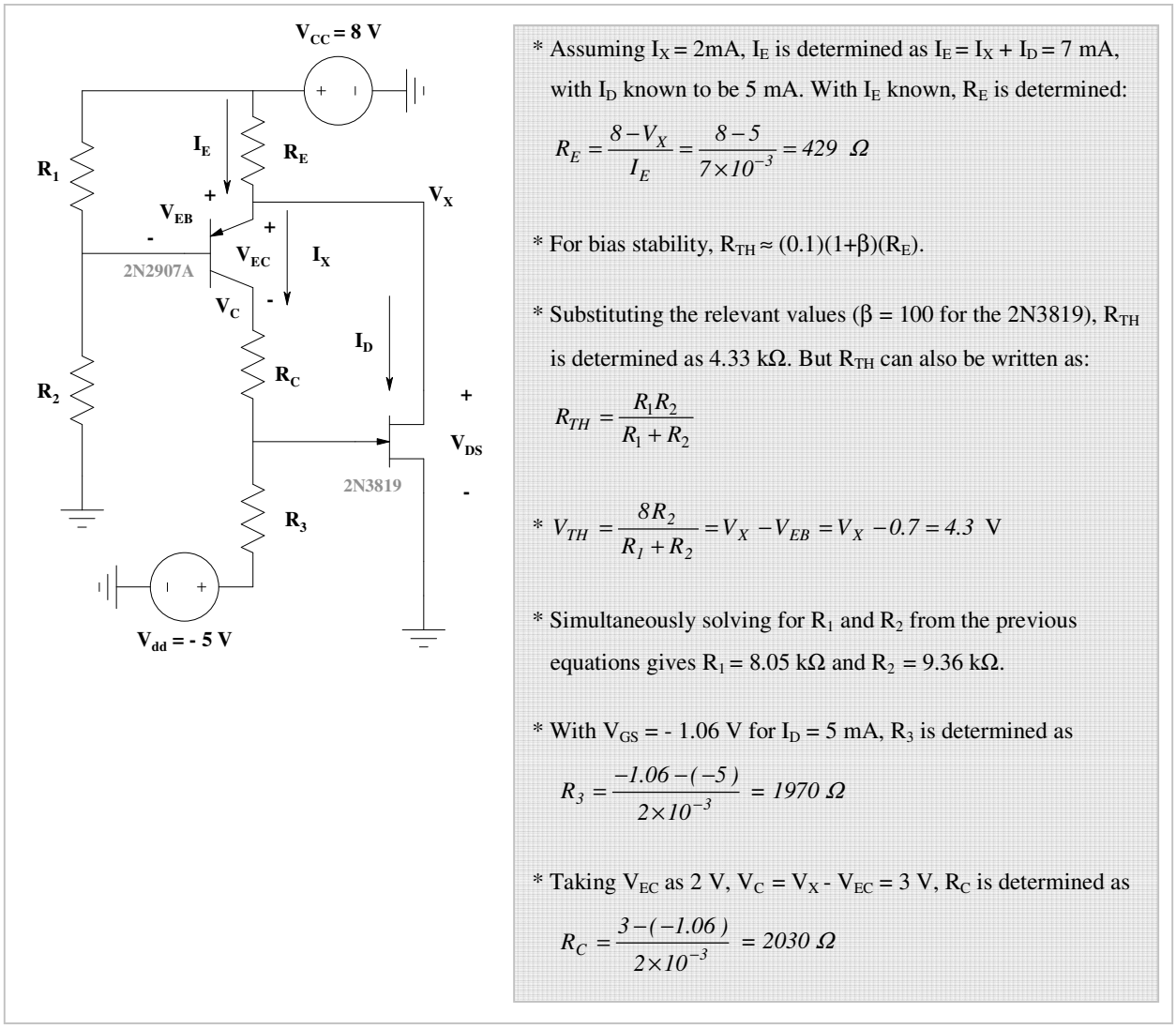
* R_G, in the shown configuration was chosen to be 10 MΩ.

Figure 3.32: Bias calculation for the passive bias configuration

Figure 3.32 shows the bias calculations for the proposed passive bias configuration [25]. The functional description for this configuration as well as that of the two active bias configurations is given hereafter. The calculated resistor values served as reference for simulations; with tuning done in SPICE to get the bias points exactly the same for each of the configurations.

In the passive bias configuration shown in Figure 3.32, R_S is necessary for automatic transient protection and to establish the relevant gate-source voltage. R_D on the other hand serves a role in temperature compensation. As the temperature decreases, the drain current will increase, causing a larger voltage drop over R_D. The drain voltage will decrease and tend to decrease the increase in drain current.

Figure 3.33 shows an alternative on the passive bias configuration [17]. The circuit constantly adjusts the gate voltage of the JFET in order to maintain the voltage at the base of the 2N2907A at a certain reference. This has the effect of holding the current through R_E constant. The actual current flowing through the PNP transistor should be low; typically in the order of a few mA's.



* Assuming $I_X = 2$mA, I_E is determined as $I_E = I_X + I_D = 7$ mA, with I_D known to be 5 mA. With I_E known, R_E is determined:

$$R_E = \frac{8 - V_X}{I_E} = \frac{8-5}{7\times10^{-3}} = 429\ \Omega$$

* For bias stability, $R_{TH} \approx (0.1)(1+\beta)(R_E)$.

* Substituting the relevant values ($\beta = 100$ for the 2N3819), R_{TH} is determined as 4.33 kΩ. But R_{TH} can also be written as:

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

* $$V_{TH} = \frac{8R_2}{R_1 + R_2} = V_X - V_{EB} = V_X - 0.7 = 4.3\ \text{V}$$

* Simultaneously solving for R_1 and R_2 from the previous equations gives $R_1 = 8.05$ kΩ and $R_2 = 9.36$ kΩ.

* With $V_{GS} = -1.06$ V for $I_D = 5$ mA, R_3 is determined as

$$R_3 = \frac{-1.06 - (-5)}{2\times10^{-3}} = 1970\ \Omega$$

* Taking V_{EC} as 2 V, $V_C = V_X - V_{EC} = 3$ V, R_C is determined as

$$R_C = \frac{3 - (-1.06)}{2\times10^{-3}} = 2030\ \Omega$$

Figure 3.33: Bias calculation for the active bias configuration (b)

If the drain current tends to increase, I_E increases and the voltage over R_E increases, resulting in a decrease in V_{DS} since:

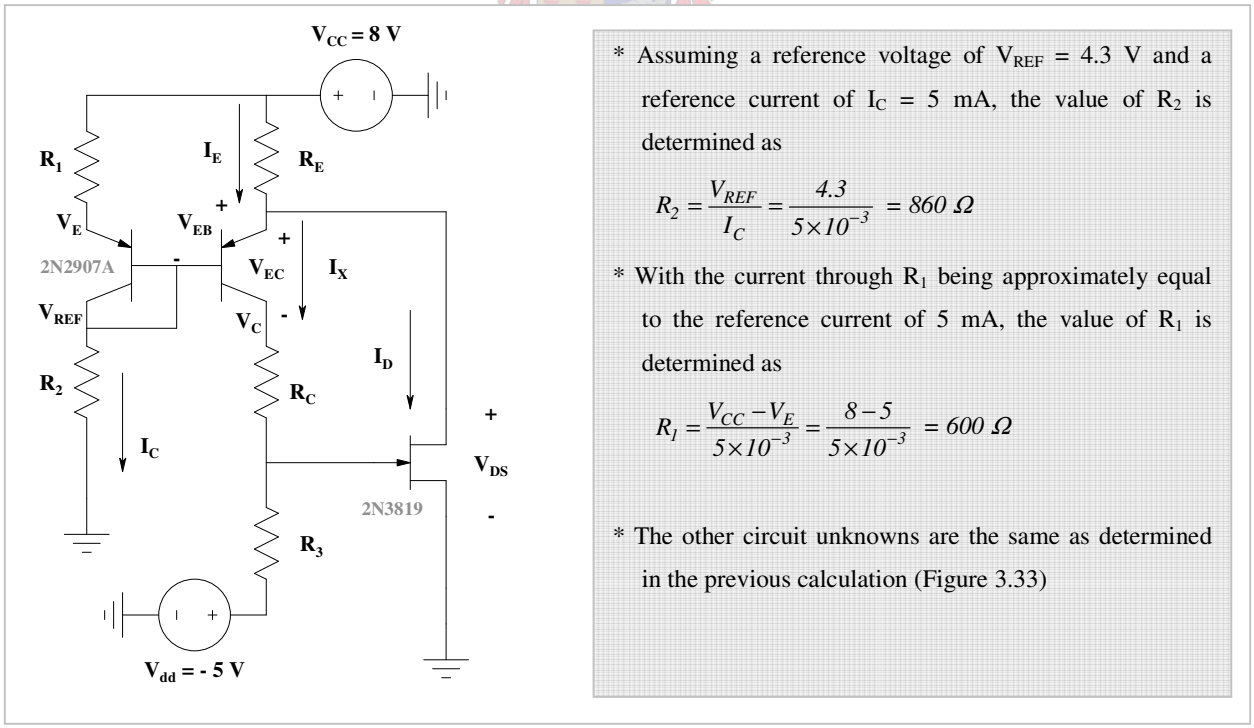
$$V_{CC} = V_{R_E} + V_{DS} \tag{3.9}$$

But since V_{DS} is equal to the emitter voltage, a decrease in V_{DS} results in a lower base current and thus a lower collector current. A lower collector current implies that the voltage over R_C must decrease. That would imply that V_{GS} must become more negative. With V_{GS} having a larger negative value, the JFET's drain current will decrease, and thus counter the initial increase.

As I_E (and thus I_D) decreases, the voltage over R_E decreases, resulting in an increase in $V_{DS.}$ An increase in V_{DS} results in a higher base current and thus a higher collector current. That would imply that V_{GS} must be less negative. With V_{GS} having a less negative value, the JFET's drain current will increase, and thus counter the initial decrease.

The effect of the BJT over temperature should however also be taken into account. The BJT will counter the temperature compensating effect of the bias configuration shown in Figure 3.33, since the emitter-base voltage will also vary over temperature.

The effect of the BJT over temperature can be overcome to a large extent by the inclusion of another PNP transistor to form a matched pair, as shown in Figure 3.34. Operation is similar to that discussed in the previous calculation (Figure 3.33), with the difference being that the BJT's emitter-base voltage variation over temperature is countered.



* Assuming a reference voltage of V_{REF} = 4.3 V and a reference current of I_C = 5 mA, the value of R_2 is determined as

$$R_2 = \frac{V_{REF}}{I_C} = \frac{4.3}{5\times10^{-3}} = 860\ \Omega$$

* With the current through R_1 being approximately equal to the reference current of 5 mA, the value of R_1 is determined as

$$R_1 = \frac{V_{CC} - V_E}{5\times10^{-3}} = \frac{8-5}{5\times10^{-3}} = 600\ \Omega$$

* The other circuit unknowns are the same as determined in the previous calculation (Figure 3.33)

Figure 3.34: Bias calculation for the active bias configuration (c)

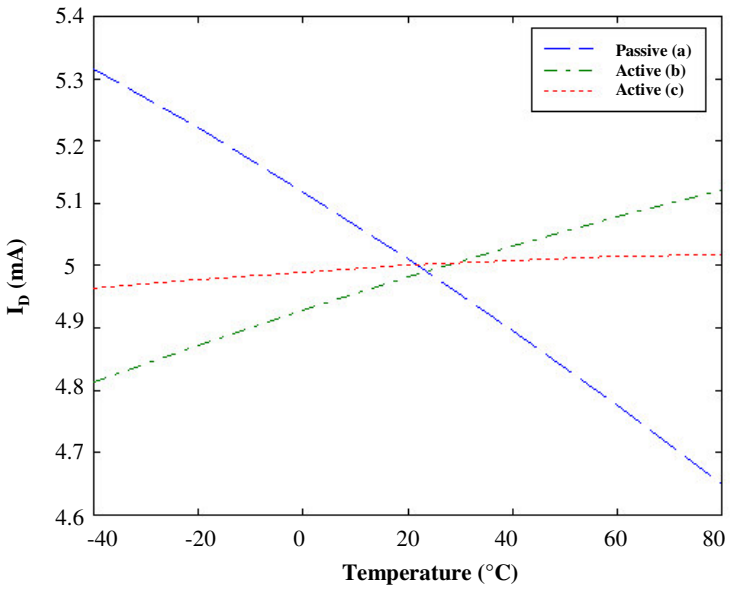


Figure 3.35: Drain current variation over temperature

The simulated results for the SPICE parametric analysis are shown in Figure 3.35. The results show that the drain current variation over temperature is worst when using passive biasing. As expected, the drain current decreases with increasing temperature and vice versa. The active biasing configuration with the single BJT, labelled as (b), offers reasonable temperature compensation, but the best response is achieved with the active biasing configuration, labelled as (c), that employs two matched BJT's.

A passive bias network such as that discussed previously can be used with good results over moderate temperature changes. Measurements, however, confirmed that an active bias network will ensure less gain variation over large temperature changes. To further assess this statement, the gain response of an RF amplifier employing active biasing was evaluated over temperature. Using the same two-stage 2-18 GHz amplifier with response shown in Figure 3.28, but with active biasing in place, the measurements shown in Figure 3.36 were made. Bias points for both the passive biased amplifier and the active biased amplifier were adjusted to be as close as possible to each other while the drive levels for both amplifiers were the same.

Figure 3.36 shows the gain of the amplifier as measured at temperatures of - 54 °C, 25 °C and 85 °C. The associated input return loss is also shown.

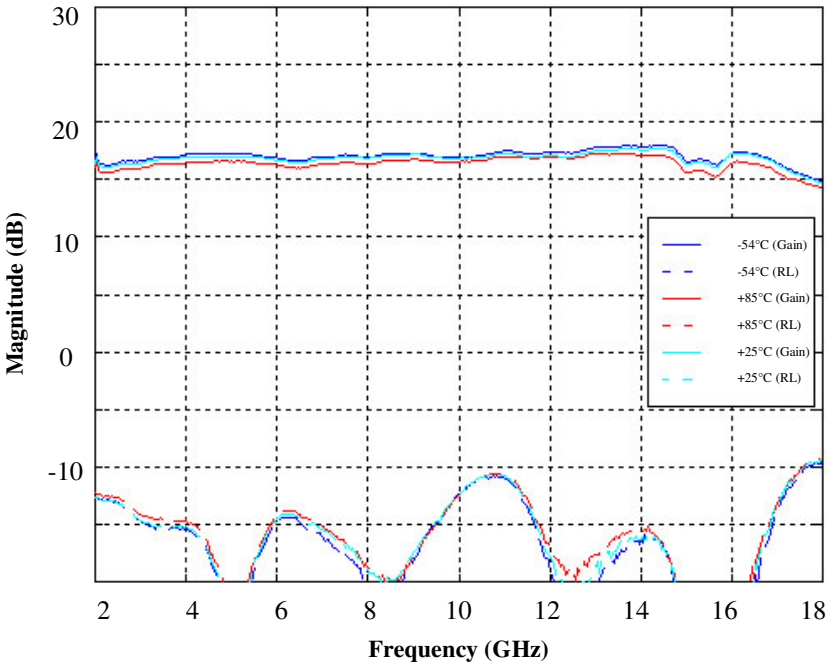


Figure 3.36: Gain response of amplifier over temperature (active biasing)

Compared to Figure 3.28, a definite improvement on the gain variation over temperature is seen in Figure 3.36, with the active biasing configuration shown in Figure 3.37 used. Some subtle differences in measured results can be seen, which are primarily due to the implementation of the active bias network.

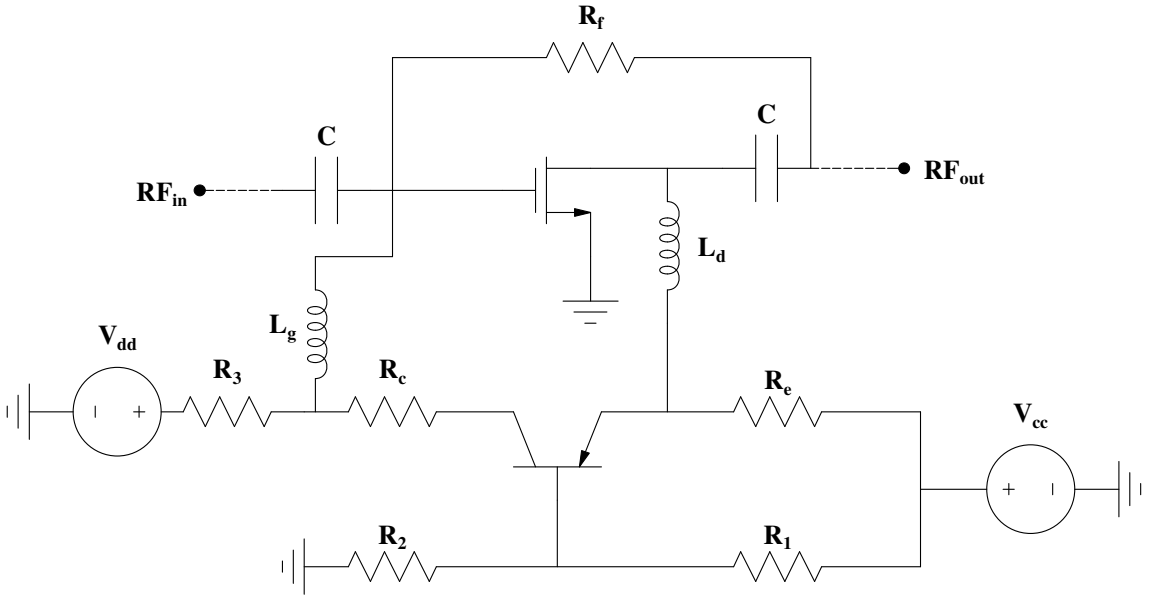


Figure 3.37: Active biasing configuration

The actual implementation of the active bias network as part of the two-stage amplifier is shown in Figure 3.38. Compared to the amplifier with passive biasing, as shown in Figure 3.39, the layout with active biasing is very *busy*. The layout includes extra bias inductors and DC blocking capacitors that may introduce undesired parasitics and losses. The effect of the DC blocking capacitors, introducing more insertion loss, was quite prominent in the measured results. This, together with slight bias variations in the two amplifiers, may then explain the difference in observed responses.

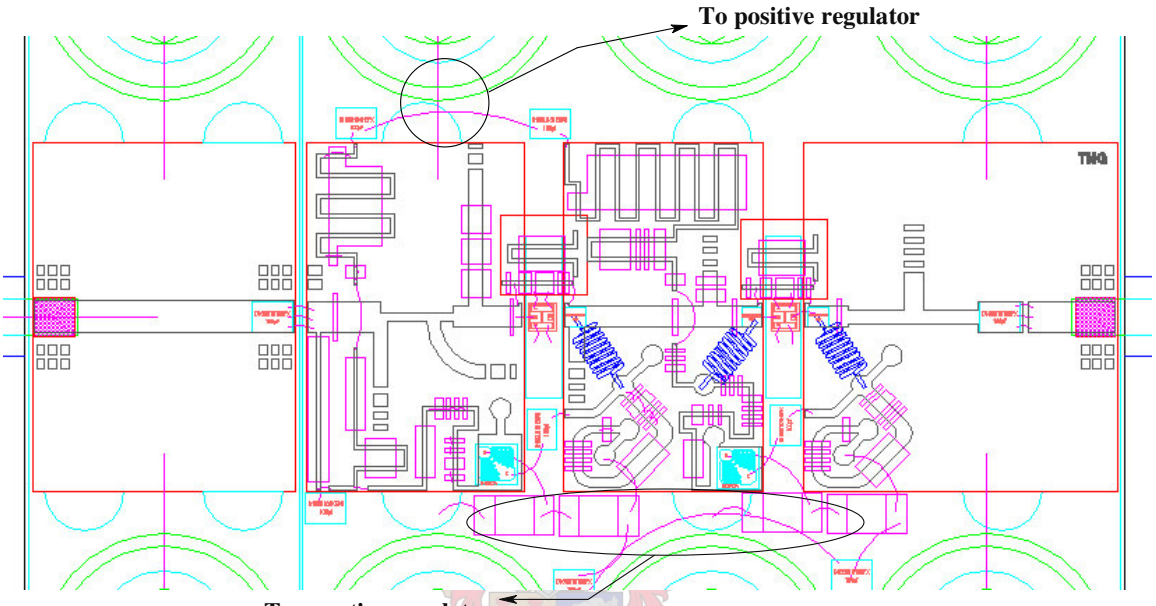


Figure 3.38: Physical implementation of amplifier with active biasing

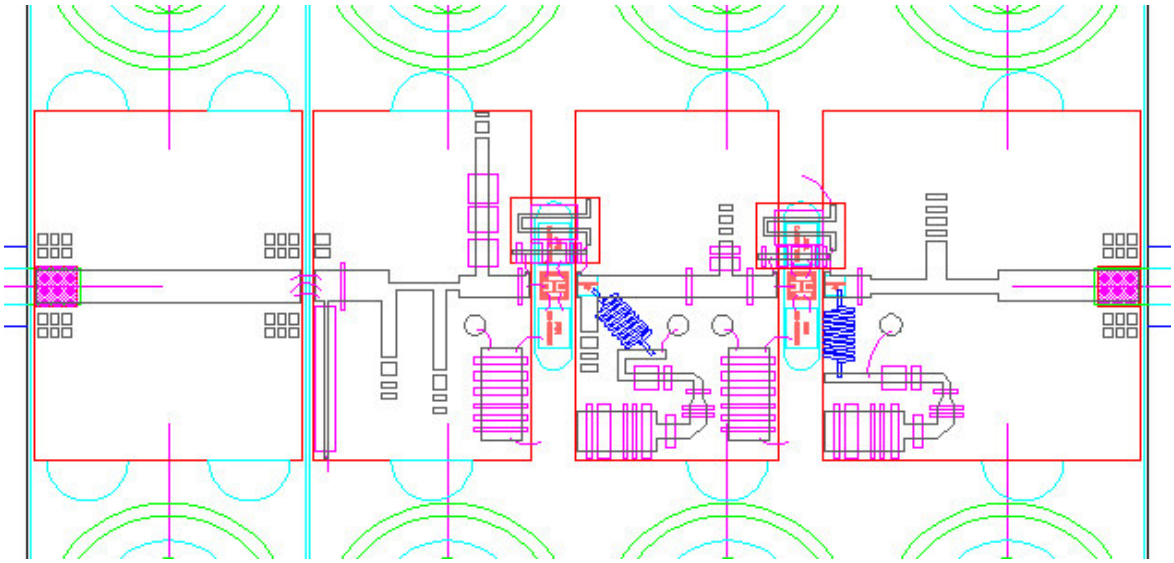


Figure 3.39: Physical implementation of amplifier with passive biasing

Implementing active biasing does require more care than would be the case with passive biasing. Gain variation over temperature is less when using active biasing and should be used especially in a multi-stage amplifier design where the effect of temperature will be exceedingly prominent. The problem, however, is that when implementing active biasing, it necessitates the use of both a positive and a negative DC supply; something which may not be desirable. Components such as BJT's, negative voltage regulators etc., will increase size and cost. At the end, the decision on the bias configuration to be used will be based on size and cost, versus device operation. These considerations were taken into account while doing the final limiting amplifier design and unfortunately, active biasing could not be implemented in this design.

The alternative, however, would be to use passive temperature compensation, in the form of the discussed temperature variable attenuators, in conjunction with passive biasing. This may offer a cheaper alternative for temperature compensation with reasonable results expected.

3.12 BIASING VERSUS LINEARITY

The best gain and IM (intermodulation) response of a GaAs FET is obtained when its bias current is set to approximately $0.5I_{DSS}$. The gain and IM intercept points at this bias point is a few dB's higher than that obtained at the bias that optimizes for example noise figure [9]. An explanation for the improved IM response at $0.5I_{DSS}$ is evident from Figure 3.40. It shows a plot of drain current versus gate-source voltage for some arbitrary FET. From this plot, it is seen that the shown I-V curve is more linear near $0.5I_{DSS}$, where I_{DSS} is approximately 40 mA.

Operation within the linear region of this I-V characteristic will minimize harmonic generation. If a small-signal sinusoidal gate-source voltage is applied to the device and operation is within the linear operating region, the output current response will also be sinusoidal, with ideally no distortion expected. If operation, however, is within the non-linear operating region, harmonic distortion is caused and the output current response will not be purely sinusoidal. In the section to follow, it will be shown that the proposed operation at $0.5I_{DSS}$ may also help in ensuring the desired maximum symmetrical swing in the output waveform.

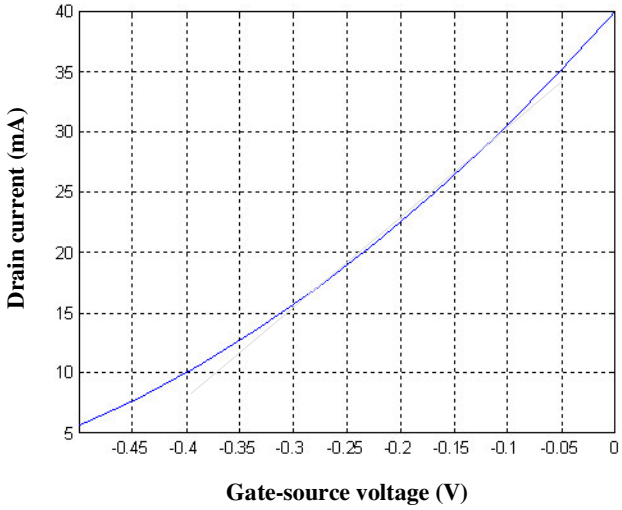


Figure 3.40: Drain current versus gate-source voltage for a GaAs FET

3.13 FUNCTIONAL BIASING

Selecting the right bias point for a certain RF amplifier application is of great importance. Also important is to choose the bias point within the safe operating region of the GaAs FET in question. The safe operating region for a GaAs FET is determined by the maximum drain current it can handle; the maximum drain-source voltage, the maximum input power to the gate and the maximum power dissipation [15].

Figure 3.41 shows a typical GaAs FET's I-V characteristics as a function of gate-source voltage. The selection of the bias point depends on a particular requirement such as low noise, maximum P_{1dB}, minimum distortion etc. For a low-noise and low-power amplifier, the FET can be biased at approximately $0.1\text{-}0.2I_{DSS}$. This bias point would be situated around point **A** as seen in Figure 3.41. The bias voltage V_{DS}, at this point, is thus also quite low.

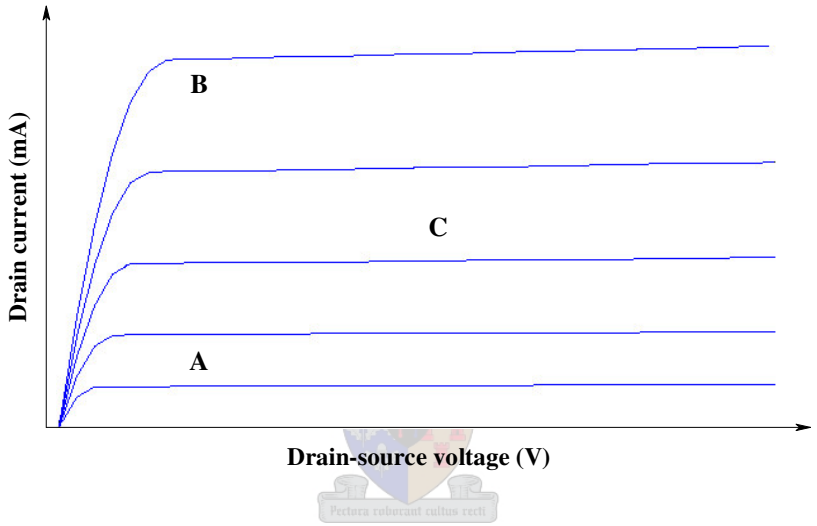


Figure 3.41: Typical GaAs FET I-V characteristic and recommended operating points

Keeping V_{DS} the same as for bias point **A**, but increasing the bias current to about $0.8\text{-}0.9I_{DSS}$ will result in an increase in both gain and power. The noise figure will still be low, but not as low as for point **A**. The new bias point is shown as point **B**. Point **C** is the bias point chosen for maximum symmetrical current and voltage swing. Biasing the FET at point **C**, which is typically at $0.5I_{DSS}$, allows for maximum P_{1dB} and minimum distortion to be achieved [15].

3.14 GAIN VARIATION AS A FUNCTION OF BIASING

Figure 3.42 shows the results of an experiment, documented in Appendix E, to determine the variation of gain in a single-stage 2-10 GHz amplifier as a function of biasing. This amplifier is the same as that discussed in Appendix C, but due to its drop-off in gain and deteriorated return loss at higher frequencies, it was only used over the 2-10 GHz frequency band. The traces seen in Figure 3.42 show how the amplifier's gain varies with bias current, at some *spot* frequency, at different bias voltages.

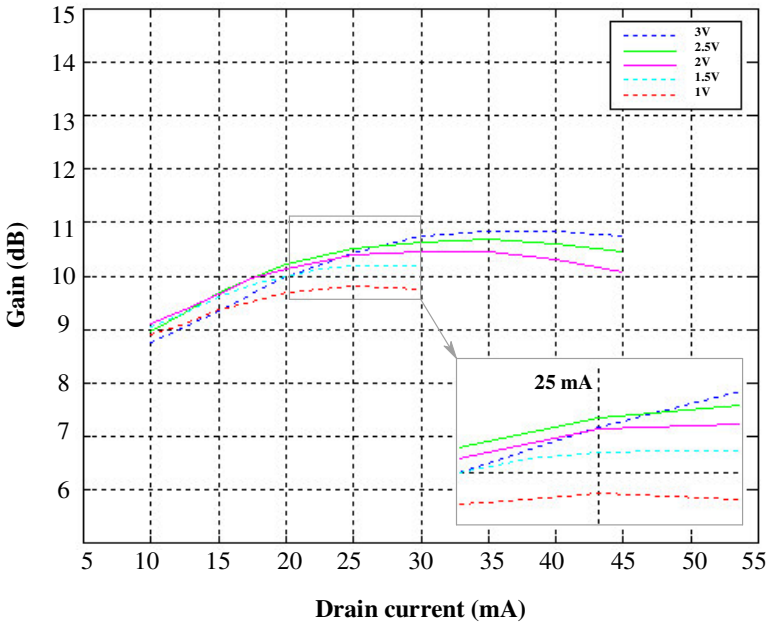


Figure 3.42: Gain variation with bias current

From Figure 3.42 it is clear that the gain is very dependent on the drain current. In general it is seen that an increase in drain current results in an increase in gain. The same can, however, be said for the drain-source voltage, since one can also see an increase in gain as V_{DS} is increased. This was then also confirmed in the section on functional biasing.

Another important deduction is that the variation of gain with bias voltage at a constant current is less spectacular than the variation with bias current at a constant voltage [14]. This statement is true, however, only if the drain current varies outside the range where the resulting gain, is essentially flat. Looking at the enlarged plot area in Figure 3.42, one can see that for a fixed bias current of 25 mA, the gain does not vary much with bias voltage. Variation of the bias current around 25 mA for example at a fixed bias voltage will, however, have a greater effect on gain variation. Over the range of drain currents for which the resulting gain is flat, the gain will be influenced primarily by the bias voltage. Maximum gain, for a certain bias voltage, exists over a rather broad range of I_{DS}, indicating that critical biasing is not necessary for optimum gain. Another result seen from Figure 3.42 is that gain variation is more serious at lower bias points; another aspect that necessitates careful choosing of a bias point.

3.15 CASCADING OF IDENTICAL AMPLIFIERS

One of the problems encountered when cascading amplifiers that *track* each other, is their complementing effect. This could cause a cascaded amplifier to have a larger ripple than that of the single amplifier. When amplifiers having poor return loss at a certain frequency are cascaded, the cascaded response yields an even worse return loss at that frequency or in the close vicinity of that frequency. The total complimentary effect of these unwanted reflections may very well deteriorate system performance at the specific problem frequency. This issue was also addressed during the discussion on RF capacitors and the avoidance of undesired complementing effects.

The S-parameters of an arbitrary amplifier at a frequency where the return loss is poor (8.9 dB) was used to see what the effect would be if two similar amplifiers were cascaded.

The S-matrix for the amplifier at the *spot* frequency is:

$$S = \begin{bmatrix} 0.36\angle -86.56° & 0.14\angle -87° \\ 2.67\angle 81.61° & 0.09\angle -61.1° \end{bmatrix} \tag{3.10}$$

From the shown S-matrix the following information can be extracted:

Input return loss: 8.9 dB

Output return loss: 20.9 dB

Gain: 8.5 dB

Isolation: 17 dB

When cascading two-port networks the ABCD matrices are used for analysis.

The ABCD matrix for the amplifier under discussion is:

$$\begin{bmatrix} \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{2S_{21}} & \frac{50(1+S_{11})(1+S_{22})-S_{12}S_{21}}{2S_{21}} \\ \frac{(1-S_{11})(1-S_{22})-S_{12}S_{21}}{50(2S_{21})} & \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{2S_{21}} \end{bmatrix} = \begin{bmatrix} 0.264\angle -93.97° & 7.37\angle -114.16° \\ 0.0026\angle -40.9° & 0.27\angle -70.97° \end{bmatrix} \tag{3.11}$$

To determine the cascaded effect of the two identical amplifiers, the two ABCD matrices are multiplied with each other to get a resultant ABCD matrix. The resultant S-matrix for the two cascaded amplifiers can then be determined from this ABCD matrix.

The resultant ABCD matrix was determined as:

$$\begin{bmatrix} 0.086\angle 179° & 3.867\angle 163.22° \\ 0.0014\angle -122.73° & 0.093\angle -144.86° \end{bmatrix} \tag{3.12}$$

From the determined ABCD matrix, the resultant S-matrix is determined as follows:

$$S = \begin{bmatrix} \frac{A+B/50-50C-D}{A+B/50+50C+D} & \frac{2(AD-BC)}{A+B/50+50C+D} \\ \frac{2}{A+B/50+50C+D} & \frac{-A+B/50-50C+D}{A+B/50+50C+D} \end{bmatrix} = \begin{bmatrix} 0.497\angle -88.3° & 0.019\angle -175.13° \\ 6.951\angle 162.21° & 0.127\angle -62.84° \end{bmatrix} \tag{3.13}$$

From the shown S-matrix the following information can be extracted:

Input return loss: 6.1 dB

Output return loss: 17.9 dB

Gain: 16.8 dB

Isolation: 34.4 dB

From the obtained results it can be seen that the input return loss of the cascaded amplifier has deteriorated by about 2.8 dB, when compared to that of the single amplifier. Similar calculations can be performed for the case where both amplifiers have good return loss at a certain frequency or where only one of the two amplifiers has good return loss at a certain frequency. One can then also determine the amplifier position in the cascade for optimum response. From these calculations one can get a good estimate of the cascaded effect of two amplifiers. It is therefore suggested that the use of similar amplifiers for a cascaded configuration is avoided. Rather break the uniformity and unwanted complementing effects to prevent undesired deterioration in amplifier response. This principle of *breaking the uniformity* was successfully applied in the final limiting amplifier design.

3.16 CONCLUSION

This chapter served as an introduction to RF amplifier design while offering the reader unique exposure to actual designs, their physical implementation and performance. Different designs were discussed without going into too much detail of the design theory. The challenges associated with different designs, especially for broadband operation was pointed out. The balanced amplifier shown offered some significant properties that may be quite useful, however, over a limited frequency band only. Designs covering the full 2-18 GHz bandwidth made use of compensated matching networks and negative feedback. Even though certain trade-offs had to be taken in the design of these amplifiers, the results were reasonably good. The two design packages, *Microwave Office* and *MultiMatch*, were successfully used in conjunction with each other for broadband designs. The designs proved useful in investigating some of the important properties of the RF amplifier. The importance of biasing was highlighted and it was shown to what extent active biasing could be used to counter gain variations in the amplifier; especially over temperature. Other aspects surrounding the biasing of the RF amplifier were investigated to arm oneself with knowledge that would only show its worth when working with an actual amplifier design.

Chapter 4 takes the investigation done in this chapter a step further, but by considering the nonlinear behaviour of the RF amplifier.

CHAPTER 4

THE NONLINEAR RF AMPLIFIER

4.1 INTRODUCTION

A discussion on the limiting amplifier would not be complete without a discussion on the most prominent nonlinearities associated with the RF amplifiers used in this component. Not only is it important to understand these nonlinearities and their effect in an RF amplifier and a limiting amplifier for that matter, but it is also important to have nonlinear analysis techniques to predict the occurrence thereof. Harmonic balance (HB) is discussed as the main analysis technique opposed to Volterra-series analysis, while power-series analysis is used in a theoretical context. The use of *Microwave Office* for nonlinear analysis is discussed with specific reference to nonlinear device modelling and model validation. With accurate device models in place, an existing amplifier design is implemented in MWO and compared to actual measurements. Without resorting to load pull design techniques, the design is optimized for use in the final limiting amplifier design, by making use of MWO's optimization tools.

4.2 NONLINEAR ANALYSIS METHODS

MWO utilizes two nonlinear analysis techniques namely HB analysis and Volterra-series analysis. Of these two techniques, HB is most useful for analyzing strongly nonlinear circuits while Volterra-series analysis is reserved for analysis of weakly nonlinear circuits. Power-series analysis, which is a special case of Volterra analysis, is discussed to provide the intuitive insight gained from representing a nonlinear device as some general transfer characteristic.

4.2.1 HARMONIC BALANCE ANALYSIS

A general circuit will contain one or more nonlinear elements embedded in linear circuitry. These different circuit elements can be regrouped to form a linear subcircuit as well as a nonlinear subcircuit as shown in Figure 4.1. This partitioning of linear and nonlinear subcircuits forms the basis for doing HB analysis ([9], [26]).

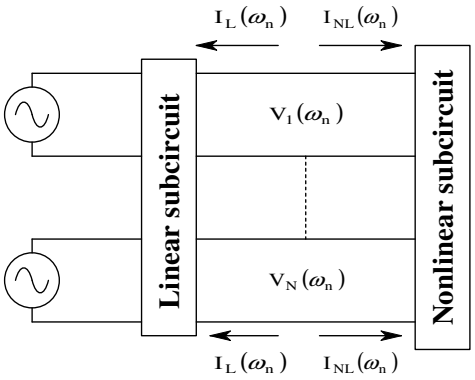


Figure 4.1: Linear and nonlinear partitioning for harmonic balance analysis

The HB technique uses an iterative calculation method to determine a steady-state solution of a nonlinear circuit, excited by some given sinusoid. The voltages at the interconnecting ports shown in Figure 4.1 are considered as the unknowns. The goal of the HB technique is to find the set of voltage phasors that satisfy Kirchoff's laws to a desired level of accuracy or else,

find

$V_1(\omega_n), V_2(\omega_n), \ldots, V_N(\omega_n)$

for all ω_n such that

$$\left| I_L(\omega_n) - I_{NL}(\omega_n) \right| < \varepsilon$$

holds at each interconnecting port. Here, ω_n is the set of significant frequencies in the port voltage spectra and ε is an error constant specifying the desired accuracy. $I_L(\omega_n)$ and $I_{NL}(\omega_n)$ are the linear and nonlinear circuit currents respectively.

In Figure 4.1, the linear subcircuit is most conveniently represented in the frequency domain by a set of two-port parameters. The nonlinear subcircuit, however, is modelled in the time domain by its global I/V characteristics and must be analyzed in the time domain ([9], [27]). These different subcircuit representations require that frequency-to-time and time-to-frequency domain conversions form an integral part of the HB method. Figure 4.2 shows a flow diagram that better explains the HB algorithm as executed at some arbitrary frequency point.

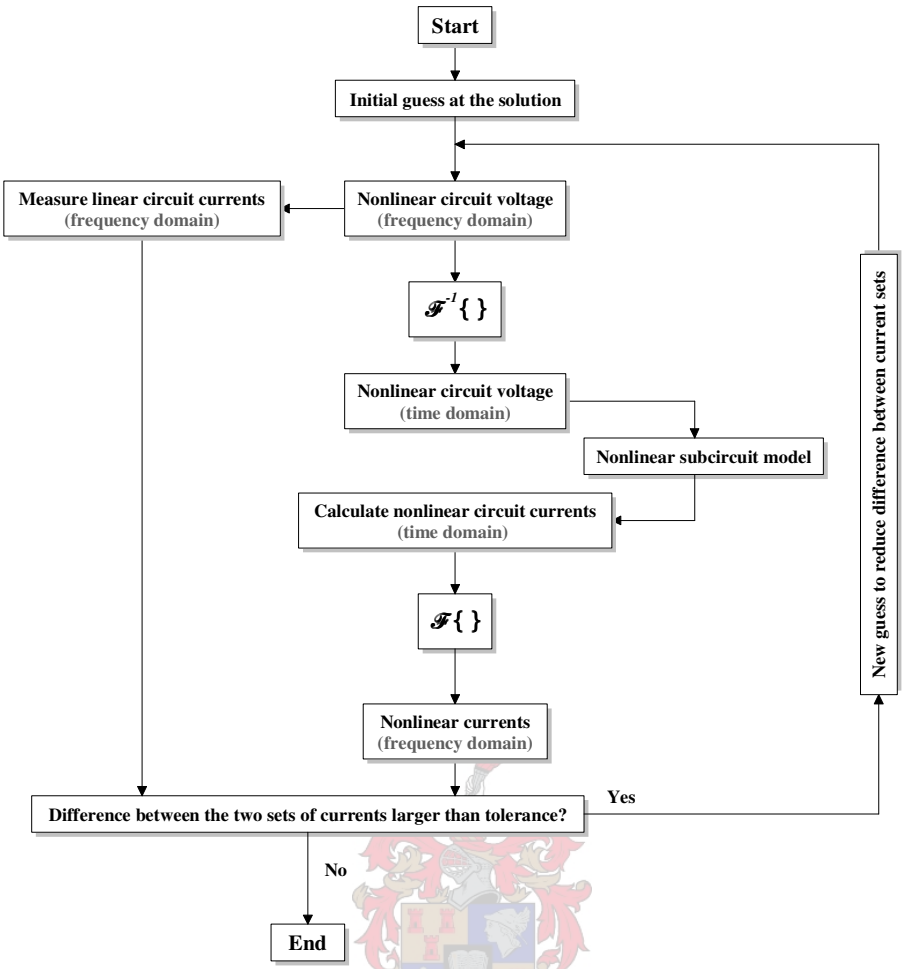


Figure 4.2: Flow diagram showing the harmonic balance algorithm

4.2.2 POWER-SERIES AND VOLTERRA ANALYSIS

Alternative methods of nonlinear analysis do exist. These include power-series and Volterra-series analysis. Power-series analysis is based on the representation of a circuit as a nonlinear transfer function where the output voltage for example, can be expressed as a power series in terms of the input voltage. The general transfer characteristic of a nonlinear amplifier can be expressed in a polynomial form as follows:

$$V_{out} = a_0 + a_1 V_{in} + a_2 V_{in}^{\ 2} + a_3 V_{in}^{\ 3} + \ldots + a_n V_{in}^{\ n} + \ldots \tag{4.1}$$

This expression is particularly useful in predicting the occurrence of nonlinear distortion phenomena both under single- or two-tone sinusoidal excitation and will be used for that purpose in discussions to follow. Power-series analysis, however, cannot predict frequency components having an order greater than the degree of the power series. Volterra-series analysis, which is related to power-series analysis, may be used instead, to solve this problem ([9], [28]). Volterra-series analysis additionally offers the calculation of harmonic and intermodulation distortion in weakly nonlinear circuits, such as amplifiers operating below 1 dB compression. Due to the fact that the amplifiers in the limiting amplifier are operated primarily above their 1 dB compression point, Volterra-series analysis was not used for evaluation of these amplifiers.

4.3 NONLINEARITIES IN RF AMPLIFIERS

Linear circuits are defined as those for which the superposition principle holds [7], and implies that the response of a linear device will only include those excitation frequencies that are present on the device's input. Looking at expression (4.1), one can see that under small-signal excitation, there will be a linear relation ($V_{out} = a_1 V_{in}$) between the input signal and the output signal. The higher order terms in expression (4.1) can be ignored and the output signal will be a true amplified version of the input signal. Should V_{in} be a multi-tone excitation such as $V_{in} = (A\sin\omega_1 t + B\sin\omega_2 t)$, the resulting output response will be $V_{out} = a_1 A\sin\omega_1 t + a_1 B\sin\omega_2 t$, which shows no extra generated frequency components. In a nonlinear device the superposition principle does not hold and the associated output response will include newly generated frequency components.

4.3.1 HARMONIC DISTORTION

Harmonic distortion is probably one of the most prominent phenomena associated with a nonlinear device and is of greatest concern in this study. As the input signal amplitude increases, the effect of the higher order terms in expression (4.1) become more prominent, resulting in newly generated frequency components, or harmonics.

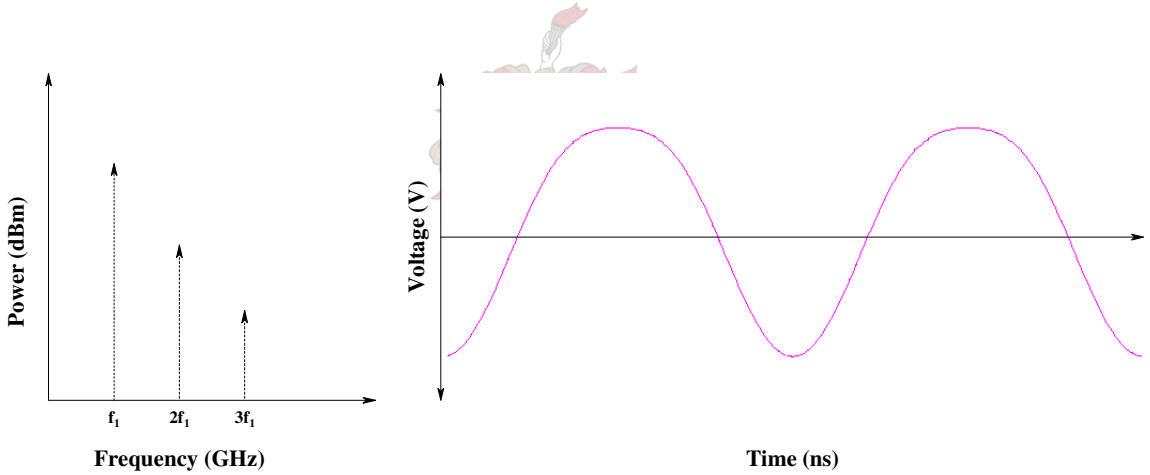


Figure 4.3: Harmonic distortion as seen in the frequency and time domain

Figure 4.3 shows an example of the effect of harmonic distortion on an amplifier's output as seen in the time and frequency domain respectively. It is seen that the output signal will be a distorted version of the ideal sinusoidal input signal. Harmonic distortion will become increasingly serious as the amplitude of the input signal is increased, causing another nonlinear phenomenon called gain compression.

4.3.2 GAIN COMPRESSION

The nonlinear phenomenon called gain compression can be mathematically explained by considering the transfer characteristic of the nonlinear amplifier. If only the terms up to the third-order are included, the transfer characteristic can be expressed as:

$$V_{out} = a_0 + a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3 \quad (4.2)$$

V_{in} is assumed to be a sinusoid, $A\sin\omega t$. This expression for V_{in} is substituted into expression (4.2) to give:

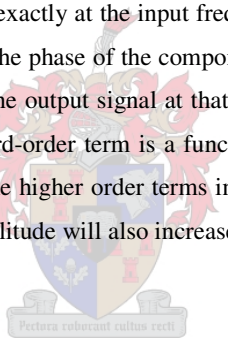
$$V_{out} = a_0 + a_1(A\sin\omega t) + a_2 (A\sin\omega t)^2 + a_3(A\sin\omega t)^3 \quad (4.3)$$

After mathematical manipulation the following expression for V_{out} is obtained:

$$V_{out} = (a_0 + 0.5a_2A^2) + (a_1A + 0.75a_3A^3)\sin\omega t - (0.5a_2A^2)\cos 2\omega t - 0.25a_3A^3\sin 3\omega t \quad (4.4)$$

The first-order term of equation (4.2) reproduces the input signal amplified by the small signal gain, a_1. With only a single tone present, the second-order term will produce output components at the second harmonic and a DC component.

The third-order term creates an output frequency exactly at the input frequency, ω. This output component adds vectorially to the output produced by the first-order term. If the phase of the component created by the third-order term is out of phase with that produced by the first order term, then the output signal at that frequency will be reduced. It is also seen that the output amplitude of the signal created by the third-order term is a function of the input signal level. The larger the input signal level thus becomes, the more significant the higher order terms in the overall transfer characteristic become. As the signal level increases, the reduction in output amplitude will also increase. This is known as gain compression [29].



4.3.3 INTERMODULATION DISTORTION

Intermodulation distortion occurs due to the mixing of multiple input tones exciting a nonlinear device. Considering the case of a two-tone excitation, with $V_{in} = (A\sin\omega_1 t + B\sin\omega_2 t)$, one can mathematically derive the output expression of a nonlinear amplifier described by $V_{out} = a_0 + a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3$.

Substituting the expression of V_{in} into the general nonlinear transfer characteristic gives:

$$V_{out} = a_0 + a_1(A\sin\omega_1 t + B\sin\omega_2 t) + a_2 (A\sin\omega_1 t + B\sin\omega_2 t)^2 + a_3(A\sin\omega_1 t + B\sin\omega_2 t)^3 \quad (4.5)$$

After some mathematical manipulation the desired result is obtained:

$$V_{out} = a_0 + a_1 A\sin\omega_1 t + a_1 B\sin\omega_2 t + 0.5a_2A^2 - 0.5a_2A^2\cos 2\omega_1 t + 0.5a_2B^2 - \ldots$$

$$0.5a_2B^2\cos 2\omega_2 t + a_2AB\cos(\omega_2 - \omega_1)t - a_2AB\cos(\omega_1 + \omega_2)t + a_3A^3(0.75\sin\omega_1 t - \ldots$$

$$0.25\sin 3\omega_1 t) + a_3B^3(0.75\sin\omega_2 t - 0.25\sin 3\omega_2 t) + a_3 1.5A^2B\sin\omega_2 t - \ldots$$

$a_3 0.75A^2B(\sin(2\omega_1+\omega_2)t - \sin(2\omega_1-\omega_2)t) + a_3 1.5AB^2 \sin\omega_1 t - a_3 0.75AB^2(\sin(\omega_1+2\omega_2)t - ..$

$\sin(\omega_1 - 2\omega_2)t$ (4.6)

It is seen that the output spectrum consists of harmonics of the form $n\omega_1 + m\omega_2$ where m and n may be positive or negative integers. The V_{in}^2 term of the nonlinear transfer characteristic generates second-order products at frequencies $2\omega_1$, $2\omega_2$, $\omega_1 - \omega_2$ and $\omega_1 + \omega_2$. The V_{in}^3 term in turn generates third-order products at frequencies $3\omega_1$, $3\omega_2$, $2\omega_1 - \omega_2$, $2\omega_1 + \omega_2$, $2\omega_2 - \omega_1$ and $2\omega_2 + \omega_1$. A typical spectrum that might be expected from the amplifier output as described by equation (4.6) is shown in Figure 4.4. In this case the input tones are spaced out quite far from each other.

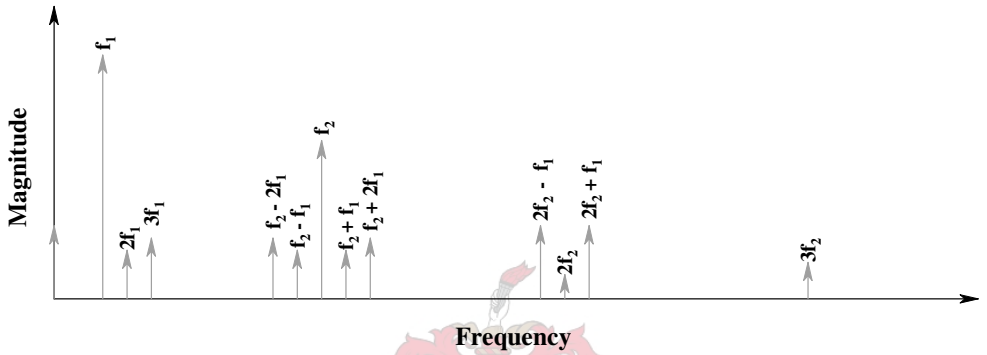


Figure 4.4: Typical output spectrum of an amplifier under two-tone excitation with a large separation between tones

Comparing Figure 4.4 with Figure 4.5, one can see the presence of intermodulation products as a function of tone separation. Of particular importance is the level of the third-order products, $2\omega_2 - \omega_1$ and $2\omega_1 - \omega_2$, in the vicinity of the input tones, especially when the separation between the tones is small. In a broadband amplifier, these third-order products, together with other generated frequency products cannot be filtered out. It is thus apparent that intermodulation products generated in an amplifier can present a very serious problem as they can interfere with desired signals and can even be mistaken for desired signals.

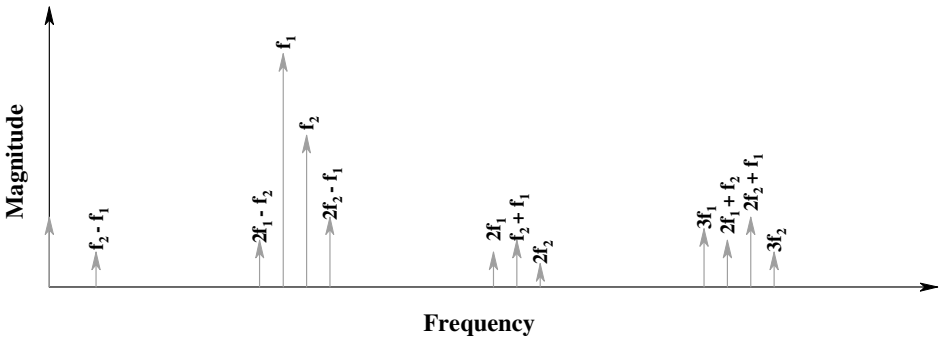


Figure 4.5: Output spectrum of an amplifier under two-tone excitation with a small separation between tones

The relevance of the discussion on intermodulation distortion will become clear in chapters to follow where the suppression of the weaker of two input tones, on the output of an RF amplifier (and the limiting amplifier) is discussed.

4.3.4 SATURATION

An amplifier has a finite output power and is unable to amplify input signals indefinitely. The result is that the amplifier's gain decreases as a function of input power level until a saturated output power level is reached. In a limiting amplifier configuration, this aspect is useful in constraining the output power window. Driving an amplifier further into saturation is associated with increased harmonic distortion while driving the amplifier too hard will destroy the device. Another significant property of gain saturation occurring in a particular amplifier is that it will have a smaller gain ripple compared to the same amplifier under small-signal operation. This statement was then also confirmed during compression point measurements on the previously discussed amplifier designs. This feature will be useful in establishing the desired output power window of the limiting amplifier.

4.3.5 AM-PM CONVERSION

AM-PM conversion is a phenomenon where changes in the amplitude of a signal applied to a nonlinear device cause a phase shift in the resulting output signal [9]. This phenomenon can be better explained in terms of the output expression (4.4) at ω, thus:

$$V_{out} = (a_1 A + 0.75 a_3 A^3) \sin \omega t \tag{4.7}$$

Expression (4.7) assumes that the first- and third-order components at ω are in phase and therefore do not give any info about phase changes associated with varying signal amplitudes. It is, however, possible that a phase difference exists between these two components so that expression (4.7) can be written as:

$$V_{out} = a_1 A \sin \omega t + 0.75 a_3 A^3 \sin(\omega t + \theta) \tag{4.8}$$

where θ is the associated phase difference between the two components. The effect of this phase difference is best explained by looking at a phasor diagram. Figure 4.6 shows that even if θ remains constant, the phase of V_{out} changes with variation in the input amplitude, A. It is seen that the phase change in V_{out} increases as the input signal amplitude increases. Intuitively one can reason that this AM-PM conversion will be particularly problematic when the nonlinear device is driven into saturation.

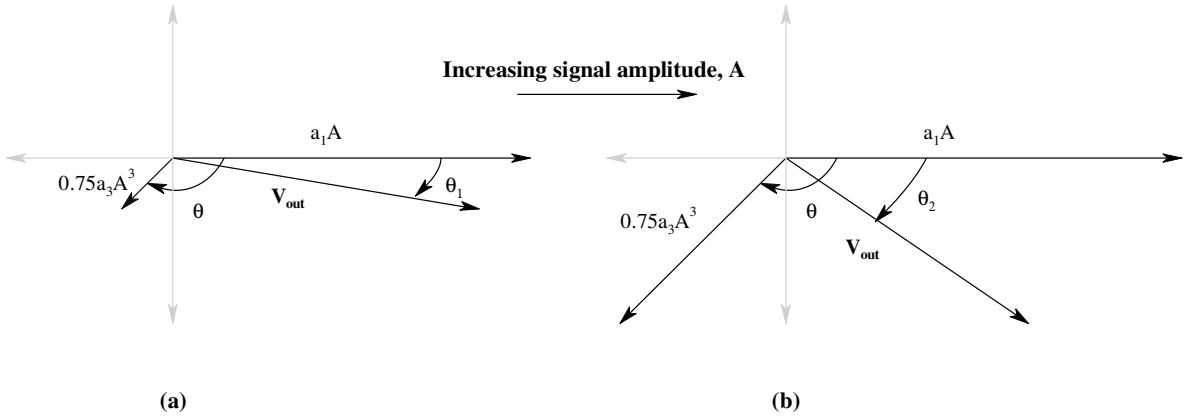


Figure 4.6: Phasor diagram showing AM-PM conversion

AM-PM conversion is an important consideration in systems requiring accurate phase information. This form of distortion may have serious consequences in a direction finding (DF) receiver for example. Should a limiting amplifier be used on the front-end of such a receiver, AM-PM conversion will definitely be one of the design considerations. This, however, is not a requirement for the limiting amplifier used in an IFM receiver since it does frequency measurement independent of phase shifts introduced by the limiting amplifier.

4.3.6 BIAS POINT VARIATION

It was shown that the third-order term in equation (4.2) produces non-linear phenomena such as gain compression and intermodulation distortion. These nonlinear phenomena, however, can be indirectly influenced by the second-order term in equation (4.2). This is due to the fact that the second-order term generates a DC component, which may influence the amplifier's bias point. In expression (4.4), $0.5a_2A^2$ was produced as part of the DC component. If this DC component causes a shift in the bias point of the nonlinear device, the coefficient of the third-order term is affected [29]. The gain compression as well as intermodulation distortion will thus also be influenced. The effect of the second-order term will again be dependent on the input signal amplitude. As the input signal level increases, the DC contribution changes and a shift in bias point is caused. Intuitively, one may also reason that bias point variation will influence the performance of an amplifier designed with S-parameter techniques. The extent, to which the amplifier's performance is influenced and possibly deteriorated, will be investigated in following chapters.

4.4 THE EFFECT OF BIASING ON INTERCEPT POINTS

The second- and third-order intercept of an amplifier are often used as figures of merit for the amplifier. The higher the intercept point, the better the amplifier is at amplifying large input signals without distortion. The third-order intercept point, IP_3, is the point where the linear extrapolation of the fundamental amplifier response and the third harmonic response intercept. The higher the third-order intercept point, the higher the input power has to be before third harmonics become

problematic. The second-order intercept point, IP_2, is the point where the linear extrapolation of the fundamental amplifier response and the second harmonic response intercept. The higher the second intercept point, the higher the input power has to be before second harmonics become problematic.

A single-tone experiment was performed on an RF amplifier, to evaluate the effect of biasing on its intercept points. The experiment would also serve the purpose of evaluating the amplifier's saturation characteristics and the generation of harmonics. Figure 4.7 shows the experimental setup for doing a single-tone test.

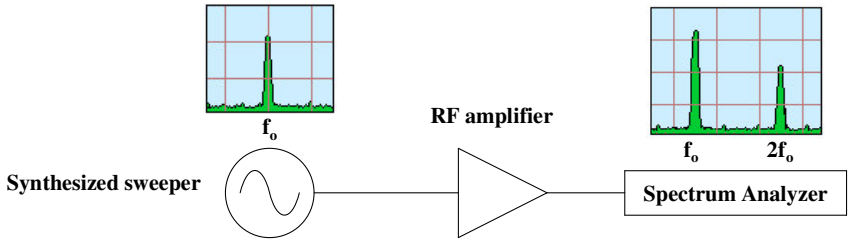


Figure 4.7: Experimental setup for single-tone tests

The synthesized sweeper is used to vary the input signal power (drive level) as well as the input signal frequency. A fixed frequency (single tone) is applied at the input of the amplifier at varying input power, while the amplifier's output spectra are measured on the spectrum analyzer. A synthesized sweeper, capable of providing enough power to drive the amplifier into saturation, is required. Initially, very low power is applied to the amplifier to make certain that the amplifier is operated in its linear region. The power is increased gradually while the output power at the fundamental frequency, the power at the second harmonic and the power at the third harmonic are measured with the spectrum analyzer. The results of single-tone tests that were done at some arbitrary fixed bias points are shown hereafter.

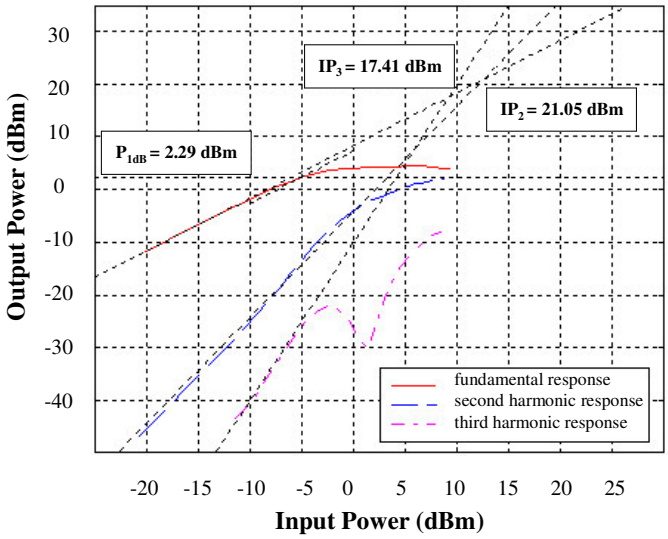


Figure 4.8: Single-tone test with bias fixed at 2 V, 10 mA

Figure 4.8 shows the result of the single-tone test for the amplifier biased at 2 V, 10 mA. When compared to results shown in Figure 4.9 and Figure 4.10, which were measured at different bias points, it is seen that the amplifier saturates at a lower input power (- 5.8 dBm). The measured output 1 dB compression point (P_{1dB}) is 2.3 dBm for this case. Another important aspect observed from this plot is to what extent the shown harmonic responses start to deviate from what is theoretically expected; especially after the onset of gain compression. An estimate of the intercept points was obtained by doing a linear extrapolation of the fundamental and harmonic responses. For the bias point of 2 V, 10 mA the measured IP_3 was 17.4 dBm while the measured IP_2 was 21.1 dBm.

Figure 4.9 shows the single-tone test result for a bias point of 2 V, 20 mA. Here an IP_3 of 22 dBm was measured, while the IP_2 was measured as 33 dBm. Again, the deviation from the theoretical expected responses is observed while the saturation of the harmonic levels also becomes more prominent. Also observed is the fact that the amplifier saturates at a higher input power level (- 0.6 dBm) with P_{1dB} = 8.1 dBm in this case.

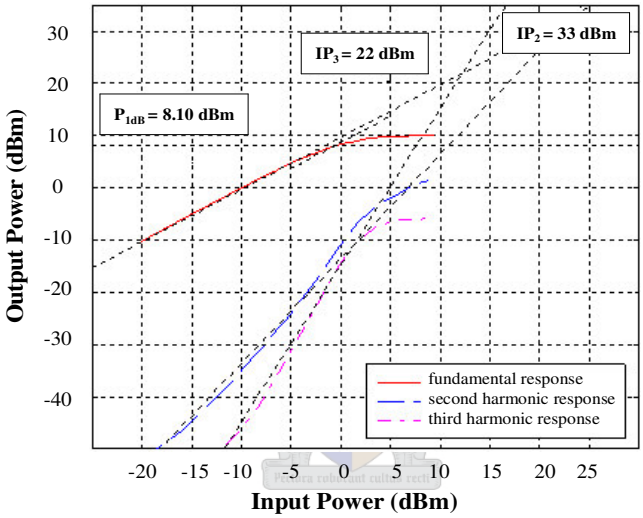


Figure 4.9: Single-tone test with bias fixed at 2 V, 20 mA

For a bias point of 2 V, 30 mA, IP_2 could not be measured accurately from Figure 4.10 while the IP_3 was measured as 23.3 dBm. For this bias point, the amplifier saturates at a higher input power level (0.7 dBm) than was the case for the other two bias points. The output 1 dB compression point was measured at 9.8 dBm for this case.

Again, a deviation in harmonic responses is observed in Figure 4.10 that is ideally not expected. Intuitively one may reason that if the shown responses could be accurately predicted and possibly optimized, one may achieve the desired limited output from the amplifier while harmonics are well-suppressed.

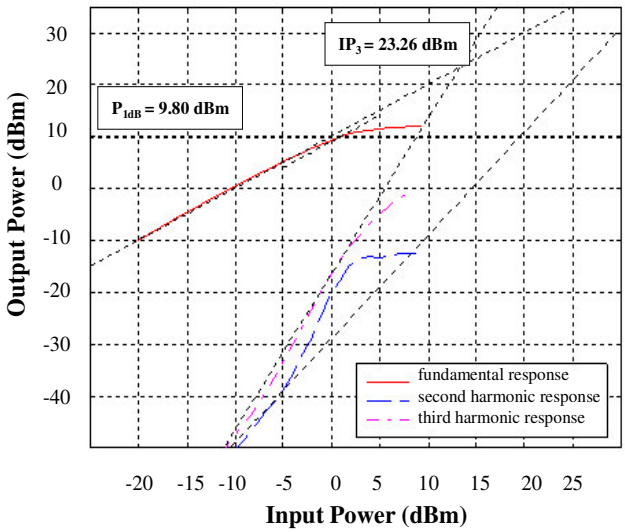


Figure 4.10: Single-tone test with bias fixed at 2 V, 30 mA

The most significant result seen from the foregoing measurements is that the 2nd and 3rd harmonic responses do not increase indefinitely in a linear relation to input power. The harmonic responses also undergo saturation. These harmonic saturation levels compared to the fundamental levels may become crucial in amplifiers to be used in a limiting amplifier configuration and were the reason for proposing operation within the *safe limiting region*. A consideration may then also be as to how the proposed *safe limiting region* is influenced by the relevant bias point.

Bias condition	P_{1dB} (dBm)	IP_2 (dBm)	IP_3 (dBm)
2 V, 10 mA	2.3	21.1	17.4
2 V, 20 mA	8.1	33	22
2 V, 30 mA	9.8	*	23.3

Table 4.1: Summary of single-tone measurements

A summary of the foregoing measured results is given in Table 4.1. This summary shows in general that an increase in bias current increases the 1 dB compression point. An increase in bias current also increases the intercept points. To confirm the obtained results, the single-tone tests were also performed at different bias points. A summary of the results where V_{DS} was held fixed at 3 V is shown in Table 4.2. Again, it is seen that the output compression and intercept points increase as the bias current increases.

Bias	P_{1dB} (dBm)	IP_2 (dBm)	IP_3 (dBm)
3 V, 10 mA	1.8	19.7	17
3 V, 20 mA	7.6	27.9	22.2
3 V, 30 mA	10.1	35.9	23.6

Table 4.2: Summary of single-tone measurements (V_{DS} = 3 V)

From the single-tone tests performed on the RF amplifier, one can make important deductions regarding the characteristics of the amplifier's intercept points, saturation levels and harmonic generation. It can be deducted that an improvement in intercept points, which is accompanied with an increase in the amplifier's ability to handle large input signals, is achieved by increasing the bias current. These measured intercept points would be particularly useful for characterizing an amplifier to be used primarily in its linear region. What should, however, be taken into account, is the fact that the harmonic response may deviate from the predicted theory, especially above the 1 dB compression point. Of greater relevance would be both single- and two-tone measurements on the amplifier to better characterize the nonlinear behaviour of the amplifier. While these measurements may be tedious and time consuming, the ideal would be to predict the nonlinear behaviour of the amplifier with a design package such as MWO, where the desired nonlinear device models are available.

4.5 NONLINEAR MODELLING

Small-signal RF amplifiers are classified as weakly nonlinear, because they are usually not operated in their nonlinear region. The small-signal RF amplifier is designed by making use of S-parameter design techniques which prove to be very accurate for small-signal operation. The S-parameter design technique, however, is a linear concept that cannot accurately predict the behaviour of an RF amplifier under large-signal excitation. If, however, an accurate nonlinear model of the active device can be obtained, one can use nonlinear analysis techniques to predict the behaviour of an RF amplifier under large signal excitation.

Another approach to the analysis of large-signal nonlinear devices is to make use of the large-signal S-parameter design technique. The nonlinear device is characterized by an S-parameter model obtained under large signal excitation. The normal small-signal S-parameter design techniques are then used to design the amplifier. This technique is problematic in the sense that a linear design approach is used to design an amplifier that will be operated solely in its nonlinear region [8].

One of the main considerations for amplifier designs requiring nonlinear analysis is whether nonlinear models exist for the active devices used. If one is confident with the particular nonlinear device models, designs can be done to specifically implement these devices. The NE27200 and NE321000, the two FETs that were evaluated and used in all 2-18 GHz designs are discussed hereafter.

4.5.1 THE NE27200 HJFET NONLINEAR MODEL

The NE27200 HJFET, which is available as part of the MWO nonlinear device library, was evaluated for use in a 2-18 GHz amplifier. Considerable effort goes into the development of nonlinear device models such as that for the NE27200 and NE321000, and it was therefore accepted that the nonlinear device models would offer an accurate portrayal of actual device characteristics. Very basic model verification was carried out, irrespective of the assumption that the device models were accurate.

Actual implementation in the MWO design environment requires that the particular device be biased at some point to ensure operation and to determine the model's accuracy. The only effective way to verify such a nonlinear model is to show that it accurately portrays the phenomena that it was designed to model. Verification of the nonlinear models under discussion was performed only to the extent of showing functionality and was not used to validate the nonlinear model again.

Firstly, the response of an amplifier designed with S-parameters of the NE27200 can be compared to the response of the same amplifier with the nonlinear device model in place. This comparison is typically done at different bias levels. Secondly, the I/V characteristics of the nonlinear device model can be compared to that measured on the actual device. Thirdly, the output compression of a design as suggested by *MultiMatch*, can be compared to that obtained with MWO simulations.

These comparison procedures give an indication of the accuracy of the nonlinear model's linear response, but they do not indicate the accuracy with which this model will predict nonlinear phenomena. Verification measurements must show that the model reproduces the phenomena of interest when all relevant parameters are varied. Parameters such as input level, frequency and biasing should be varied within operating constraints for model verification purposes.

Figure 4.11 shows part of the evaluation of the NE27200's nonlinear model. An S-parameter matrix,[$S_{measured}$] , obtained from measurements on the actual device at a certain bias point, is compared with a model-derived S-parameter matrix, [$S_{model\text{-}derived}$], at the same bias point. The result of such an S-parameter comparison, for a bias point of 2 V, 20 mA is shown in Figure 4.11. The result shows a very close comparison between the two sets of measurements, which would suggest that the nonlinear device model is accurate. Ideal *bias-tee* networks are used to apply the biasing so as not to influence the measured response.

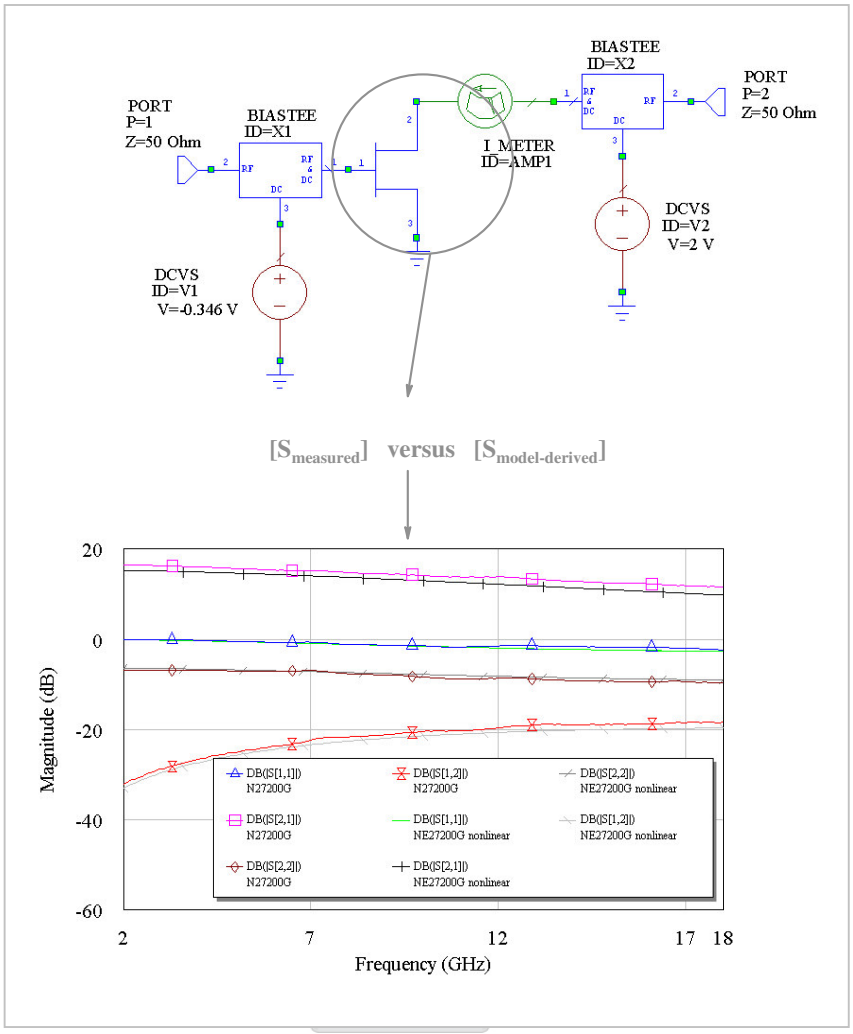


Figure 4.11: Basic evaluation of the NE27200 nonlinear model

4.5.2 THE NE321000 HJFET NONLINEAR MODEL

A similar model evaluation as done with the NE27200 was done with the NE321000. Figure 4.12 shows these results. Again it is seen that the model-derived S-parameter response is very close to the measured S-parameter response. There is, however, a noticeable deviation in the S_{22} responses above 15 GHz. In spite of this deviation, the nonlinear device can be used for designs. The effect of this deviation should, however, be assessed by replacing the nonlinear model with the relevant S-parameter model in a specific design. If there is no serious deterioration in the simulated response when the S-parameter model is used and the response is still comparable with the model-derived response, the design can be considered accurate enough for implementation.

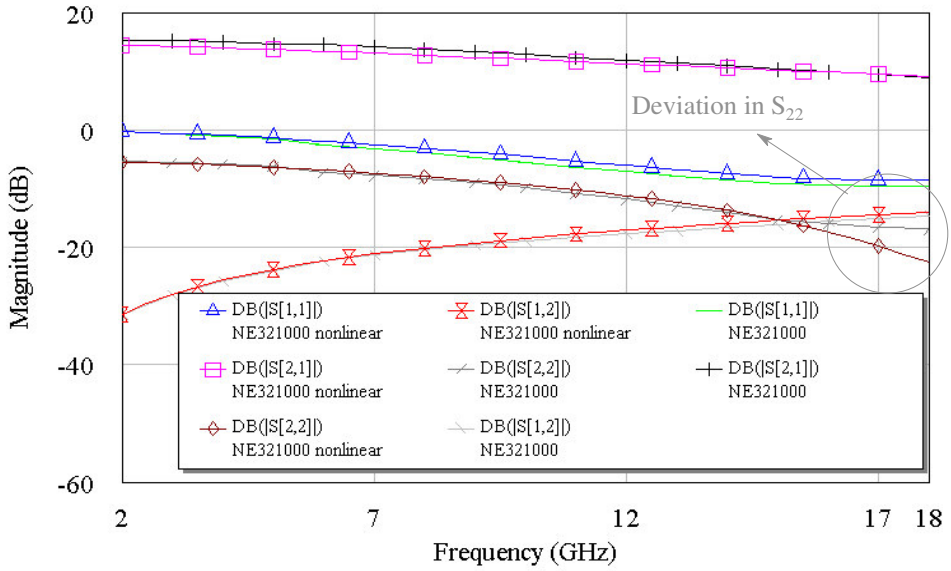


Figure 4.12: NE321000 nonlinear model evaluation

4.6 NONLINEAR ANALYSIS IN MICROWAVE OFFICE

The analysis of RF amplifiers done in MWO consisted mainly of single-tone analysis techniques. Large-signal S-parameter measurements together with power spectra measurements were used for nonlinear analysis. The large-signal S-parameter measurements are used to compute the equivalent of an S-parameter under large-signal excitation conditions [28].

Figure 4.13 shows the result of such a large-signal S-parameter measurement as well as the accompanying spectral output for an amplifier driven with a 4 GHz signal at 5 dBm input power. Significant about the large-signal S-parameter measurement (S_{21} in this case) is that it gives the gain associated with each spectral component over the frequency band of interest, at some relevant input power. From this measurement, one can therefore determine the actual levels of the frequency spectra in question, thus:

$$P_n = P_{in} + (S_{21})_n \tag{4.9}$$

P_n is the power of the specific spectral component measured in dBm, P_{in} is the power of the single-tone excitation measured in dBm and $(S_{21})_n$ is the gain associated with the relevant spectral component, measured in dB. At 4 GHz for example, the gain associated with the second harmonic is - 7.775 dB as seen from Figure 4.13. The actual power level of the second harmonic, with P_{in} equal to 5 dBm, can therefore be determined as:

$$P_2 = 5 + (-7.775) = -2.775\ dBm \approx -2.8\ dBm \tag{4.10}$$

The determined power level for the second harmonic is exactly that measured for the second harmonic as part of the amplifier's spectral output. The same argument goes for the other spectral components as well. Another important aspect is that harmonic suppression, indicated as Y_1 and Y_2, may be determined from the large-signal S-parameter response as well.

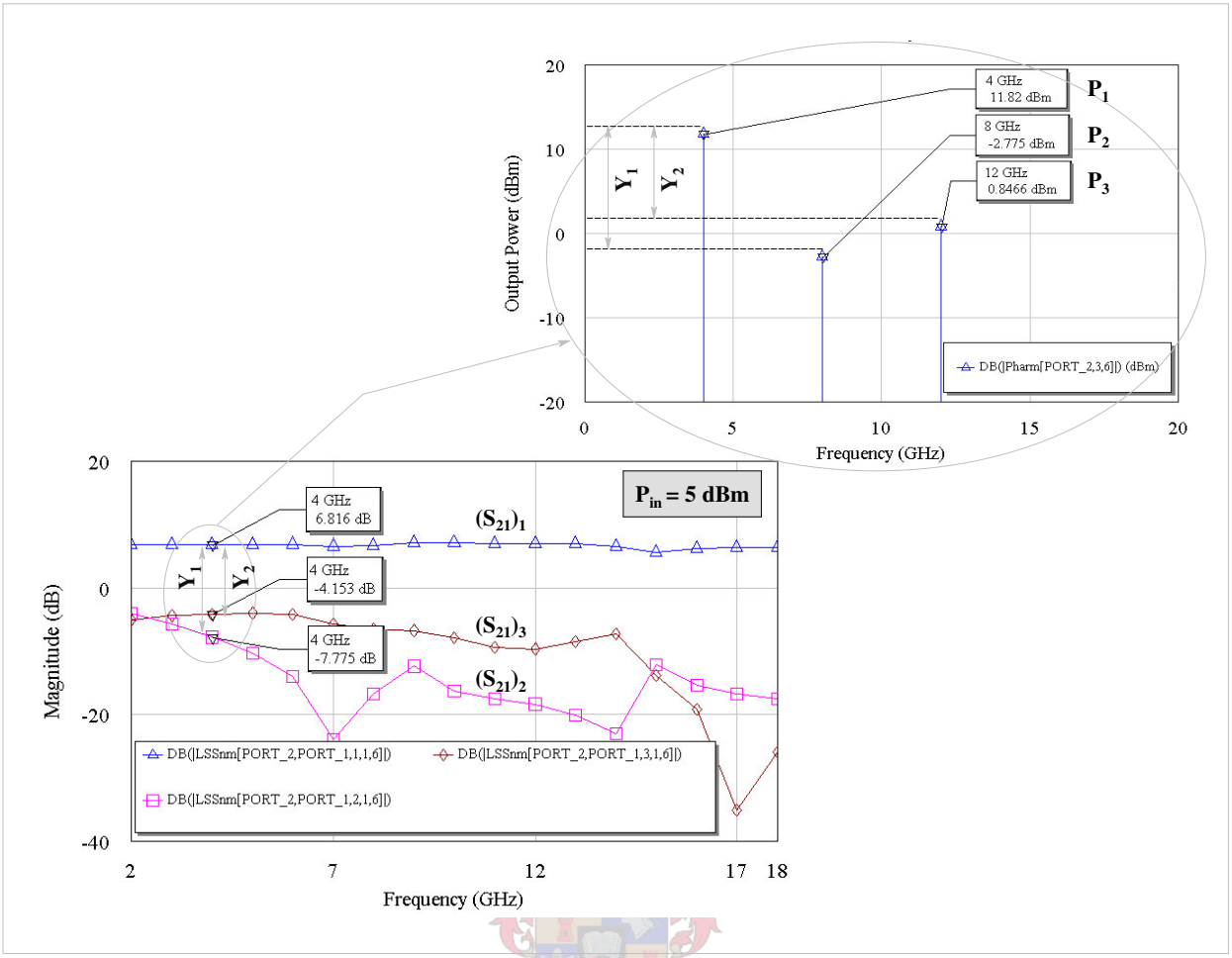


Figure 4.13: Nonlinear analysis using large-signal S-parameters

The previous argument is significant in establishing a measurement set that can be tuned and optimized in MWO. A range of large-signal S-parameter measurements, at different input powers can be set up so that the amplifier in question can be optimized for improved behaviour over the relevant input dynamic range.

4.7 NONLINEAR IMPLEMENTATION OF A 2-18 GHz AMPLIFIER

4.7.1 RECONSTRUCTION OF AN EXISTING DESIGN

In this section the reconstruction and optimization of a two-stage amplifier used in the baseline limiting amplifier is discussed. The amplifier is reconstructed from an existing design layout and then implemented in MWO for simulation. Such a reconstruction proved useful since no design files existed for the specific amplifier. In doing the reconstruction and nonlinear implementation one eliminates the need for a complete initial design phase and one establishes a reference for evaluating an existing design. Figure 4.14 shows a measurement of the gain response of the actual amplifier.

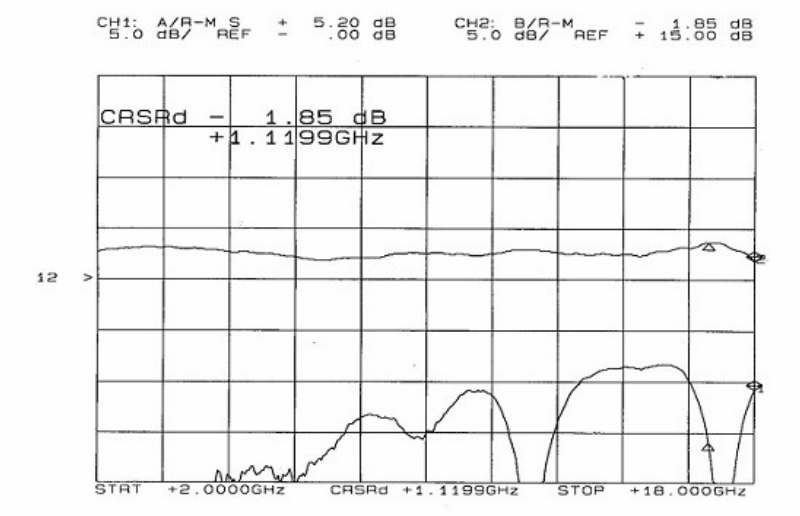


Figure 4.14: Gain response of the amplifier used in the baseline limiting amplifier

Compared to the response of the reconstructed amplifier and its nonlinear implementation, as shown in Figure 4.15, it is clear to what extent an accurate reconstruction of an existing design can be made.

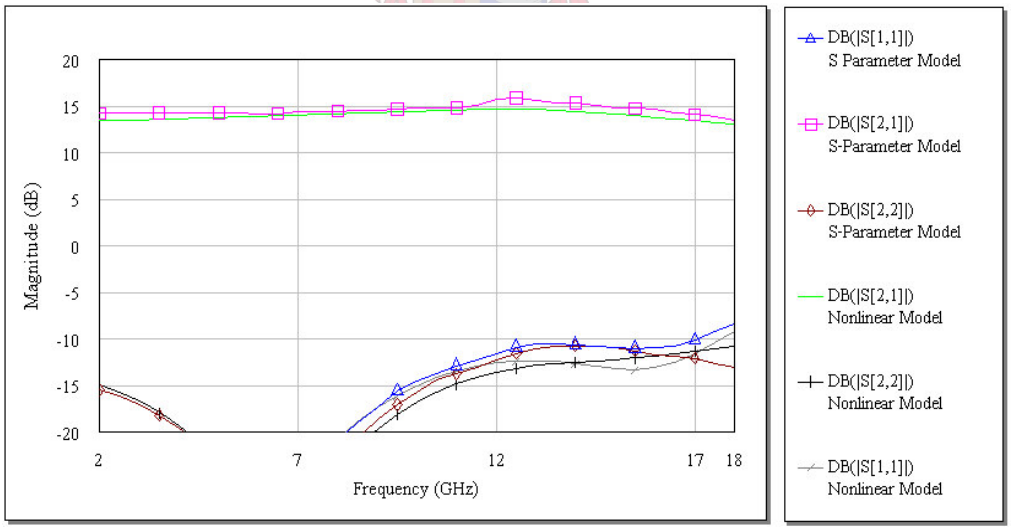


Figure 4.15: Response of the reconstructed amplifier

Comparing Figure 4.14 and Figure 4.15 one can see both similarities and differences between the actual measured results and the MWO implementation. The input return loss response for both measured and simulated amplifiers shows the same general trend. The output return loss for the specific amplifier was not measured. The measured gain is higher than that simulated and is probably due to a higher bias point used on the actual design.

One may reason that the measured response is not exactly that simulated, and that the simulation will therefore not accurately portray the amplifier's behaviour. Simulated results, however, how perfect they may be, cannot take into account all the different tolerances associated with the actual manufacturing of the amplifier. For this reason, a design must allow for ample tuning stubs to help compensate for these tolerances.

Figure 4.15 shows another useful aspect namely that the amplifier response implementing an S-parameter model is similar to the response of the accompanying nonlinear model. The amplifier under discussion made use of the NE27200 HJFET discussed earlier. Figure 4.16 shows the schematic layout of the reconstructed amplifier, with the different matching sections that were measured up in *AutoCad* implemented as functional blocks. Actual *DiLabs* capacitor models were used for simulations.

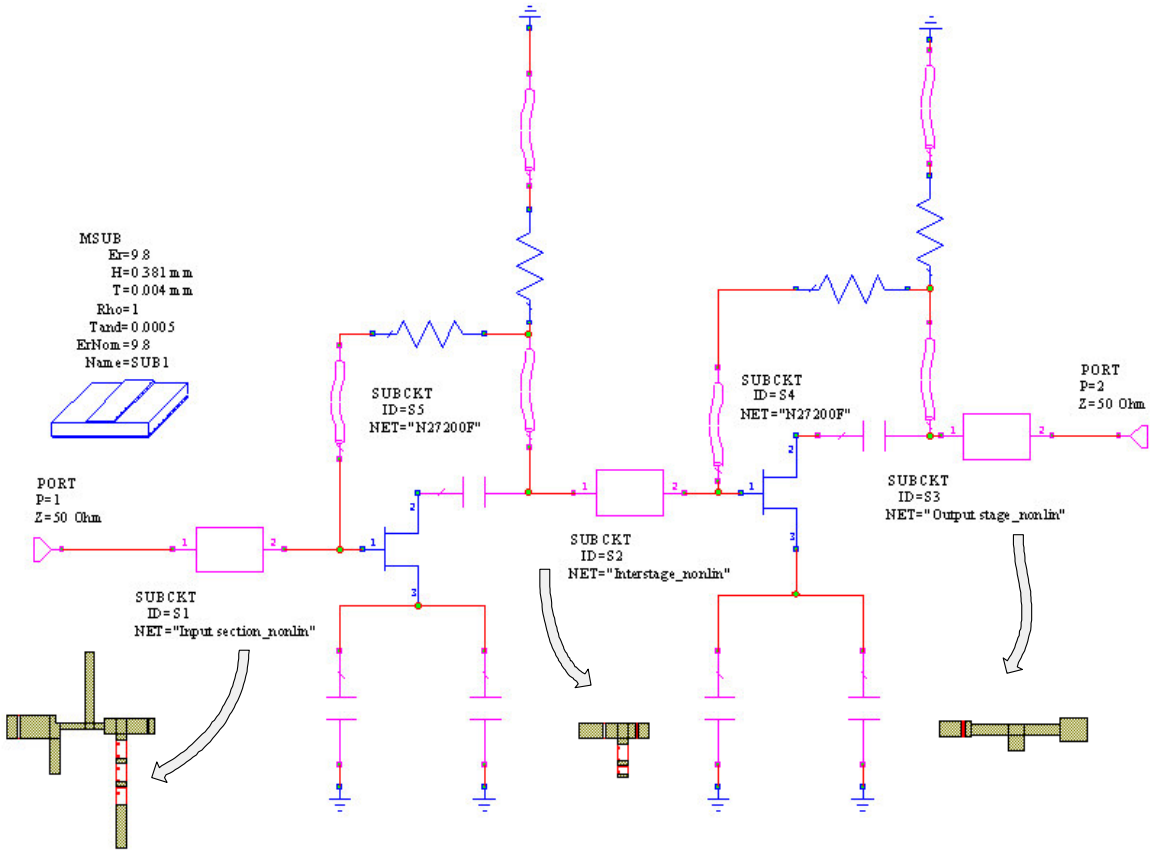


Figure 4.16: Schematic layout of the reconstructed amplifier

The reconstructed amplifier, but with the nonlinear model in place is shown in Figure 4.17. The shown layout includes the necessary bias circuitry as well as a swept power source for nonlinear analysis. The matching sections are exactly the same as that shown in Figure 4.16.

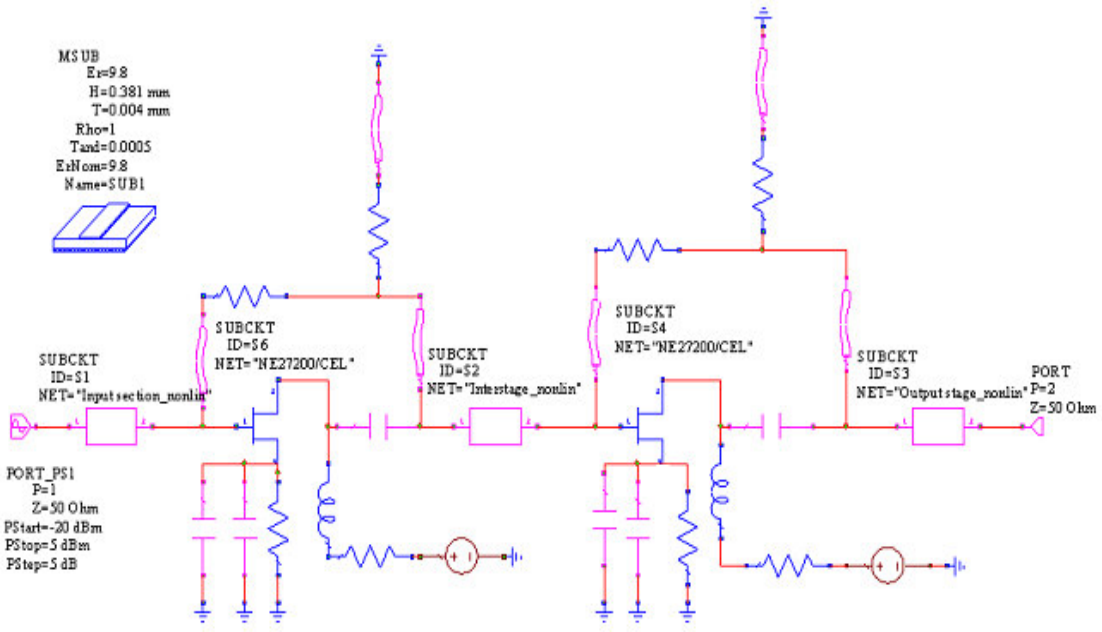


Figure 4.17: Implementation of the reconstructed amplifier for nonlinear analysis

Compression measurements on both the reconstructed amplifier and the actual amplifier were done to further confirm that the reconstructed amplifier gave an accurate representation of the actual amplifier. Figure 4.18 shows the result of the 1 dB compression measurement. It is seen that 1 dB compression occurs first at a frequency of 3.24 GHz, with resulting 10 dBm output power.

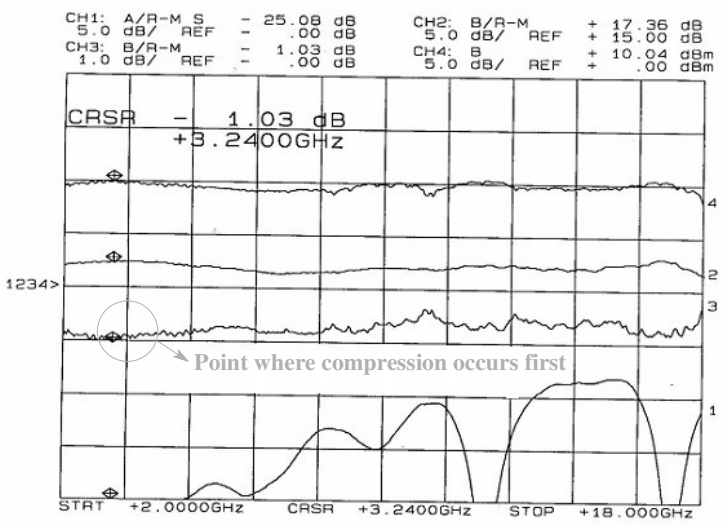


Figure 4.18: Compression measurement done on the actual amplifier

A simulation was done on the nonlinear implementation of the reconstructed amplifier to determine the predicted 1 dB compression point. This simulation was done at 3.24 GHz, the point where gain compression occurred first in the actual amplifier.

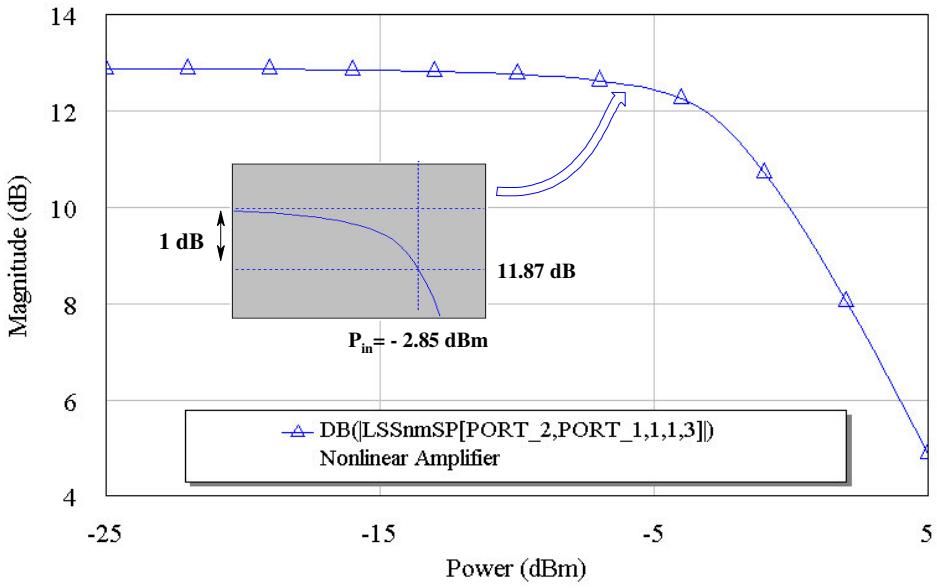


Figure 4.19: Simulated gain compression at 3.24 GHz

Figure 4.19 shows the result of a large-signal S-parameter measurement that was set up so that the gain associated with the fundamental tone could be plotted as a function of input power. The shown gain response drops by 1 dB, to 11.87 dB, at an input power of - 2.85 dBm. This corresponds to an output power of approximately 9 dBm. Compared to the measured 10 dBm on the amplifier with a slightly higher bias point, the simulated result gave a good indication of what to expect from the actual amplifier.

4.7.2 OPTIMIZATION OF THE RECONSTRUCTED AMPLIFIER

The discussion thus far was concerned mainly with the reconstruction of an existing design, its implementation in MWO and comparing how well a representation it was of the actual existing design. The comparison between the actual design and its implementation in MWO, although very basic, is sufficient in establishing the feasibility of physical implementation of a design from simulations.

With reasonable confidence in the nonlinear implementation of a design established, one may commence to evaluating the actual nonlinear behaviour of the design, as well as to what extent the design may be optimized for some desired response. The discussed reconstructed amplifier was used as reference for an optimized design to be used on the output of the final limiting amplifier design. Large-signal S-parameter measurement sets, as discussed earlier, were used for tuning and optimization purposes. Figure 4.20 shows the gain response of the optimized amplifier. Not only does the optimized amplifier offer slightly higher gain and good gain flatness, but it also offers an improved input and output return loss. The

improved gain response, although important, says nothing about the amplifier's nonlinear behaviour. Optimization constraints should, therefore, be set up to take into account the small-signal behaviour of the amplifier as well as the associated nonlinear phenomena. The aim of optimization was therefore to have an amplifier with good harmonic suppression over some relevant input dynamic range while still offering a good small-signal response.

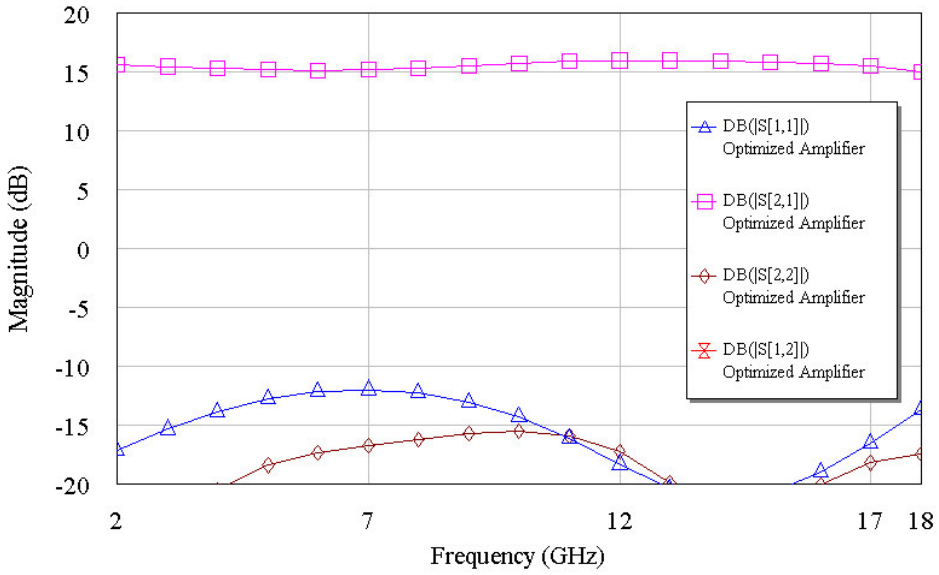


Figure 4.20: Gain response of the optimized amplifier

Figure 4.21 shows a comparative result of the third-order intercept measurements for the reconstructed and optimized amplifier under single-tone excitation. The single-tone intercept point measurement predicts the intercept point of the fundamental and third harmonic but is conceptually similar to the two-tone 3rd order intercept point. This measurement in MWO offers a useful starting point for optimization, since an improved third-order intercept response will ensure improved third harmonic suppression, for some input dynamic range. It is seen to what extent the reconstructed amplifier could be optimized for an improved third-order intercept point from 2-18 GHz. The result shows an improvement in response over the largest part of the frequency band, but more important, is the improved response at frequencies below 6 GHz. Harmonics of these frequencies are present in-band and should ideally be suppressed as low as possible. Also evident is that a complete improved response is not easily achieved over the entire bandwidth.

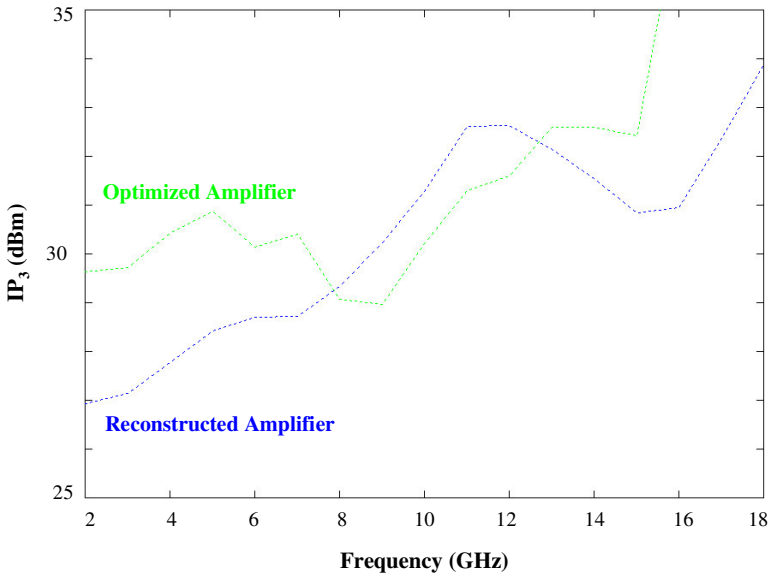


Figure 4.21: Comparative third-order intercept measurements

The second-order intercept point can be optimized in a similar fashion, but focus was rather placed on the more troublesome third-order effects. Second harmonic suppression was addressed, but as part of the large-signal S-parameter analysis of the design.

Large-signal S-parameter measurements that were done on the reconstructed and optimized amplifier were concerned mainly with the nonlinear behaviour of the amplifier above its 1 dB compression point. For the amplifier with a gain of approximately 15 dB and 1 dB compression point of about 10 dBm, operation at input powers above - 5 dBm were considered very carefully. The large-signal S-parameters sets as measured at these higher input powers are therefore the main considerations for tuning and optimization purposes. It was seen that it is difficult to quantify exactly which parameter to set up for optimization. At a certain input power for example, the second harmonic suppression may be worse than the third harmonic suppression, while this may not be the case at a different input power. For this reason, optimization constraints were rather set up to get the best trade-off between results.

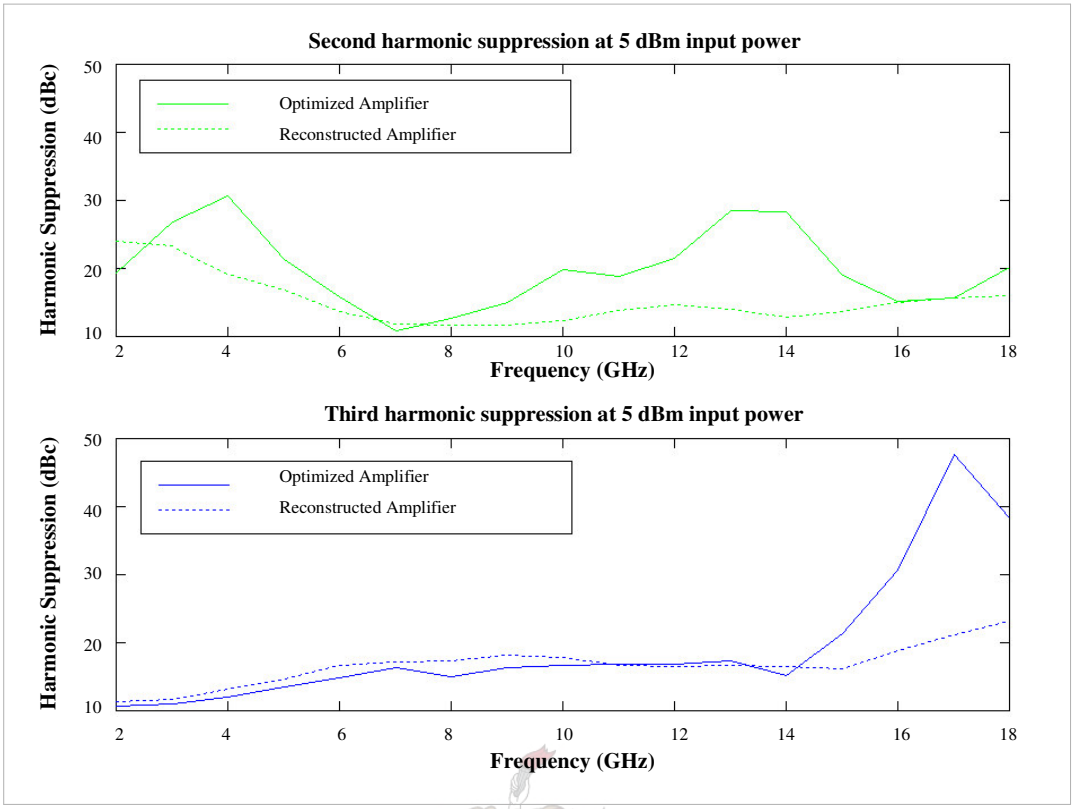


Figure 4.22: Harmonic suppression as measured at 5 dBm input power

Figure 4.22 shows a set of harmonic suppression measurements that compares the response of the reconstructed amplifier with that of the optimized amplifier at an input power of 5 dBm. From the plots it can be seen that the optimized amplifier offers improved second harmonic suppression over the largest part of the frequency band while a slight deterioration in the third harmonic response was introduced over a portion of the frequency band. Evident from this response is again the difficulty in optimizing a specific parameter for overall improved response over the entire frequency band. Pleasing, however, is the fact that harmonic suppression can at least be optimized to larger than 10 dB's. Intuitively one may reason that the particular amplifier, even though optimized, should not be operated above an input power of 5 dBm. Operation above 5 dBm will typically lead to deteriorated harmonic suppression and is suggested as upper limit on the input drive level. With optimization constraints set up to improve the harmonic suppression at an input power of 5 dBm, one would expect improved harmonic suppression for the optimized amplifier at lower drive levels as well. This, however, is not necessarily the case. The results for lower drive levels showed that the original reconstructed amplifier actually offered better harmonic suppression at certain drive levels, than was the case for the optimized amplifier.

Figure 4.23 shows a similar measurement such as that shown in Figure 4.22, but with an input power of 0 dBm. The harmonic suppression in this case is as expected, quite a bit higher than the 10 dB suppression achieved at a 5 dBm drive level. Typical harmonic suppression in this case exceeds 15 dB. Here one can see an overall improved third harmonic suppression but a slightly deteriorated second harmonic suppression.

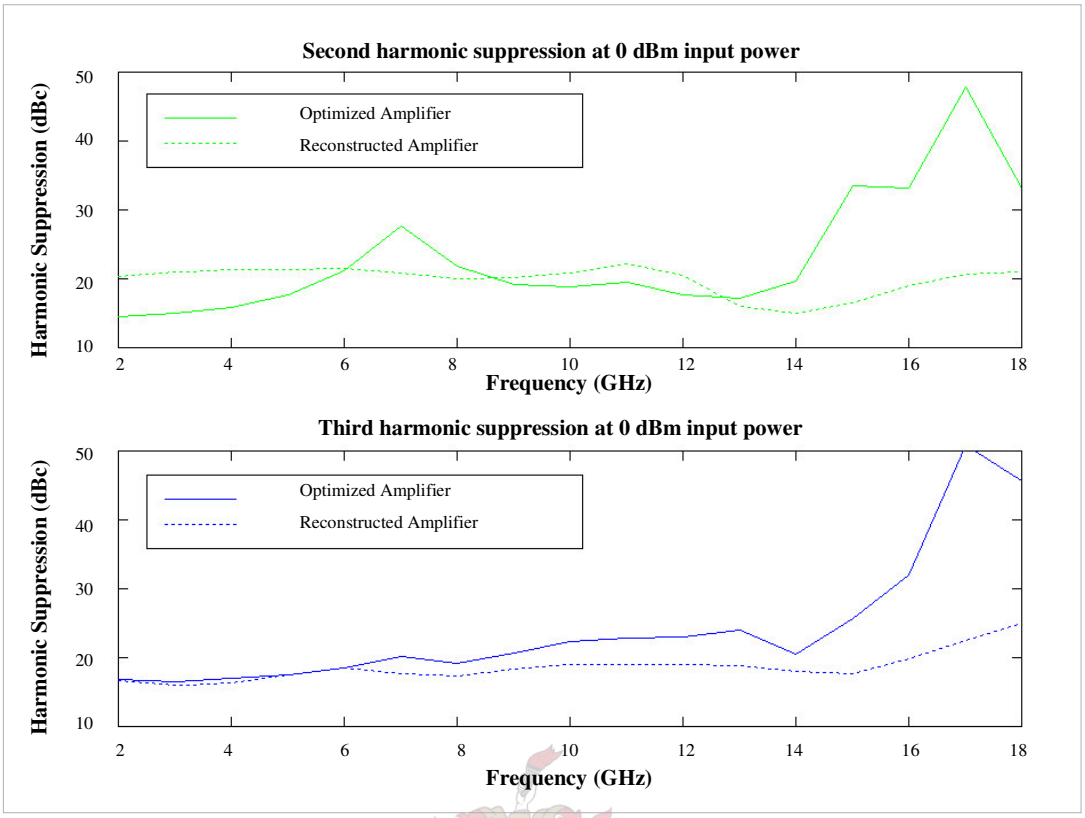


Figure 4.23: Harmonic suppression as measured at 0 dBm input power

Figure 4.24, which shows harmonic suppression for an input power of - 5 dBm, actually shows an overall deterioration in harmonic suppression when comparing the *optimized* response with the reconstructed response. The conclusions drawn from the simulated results are that harmonic suppression may be optimized for a specific input drive level even though an improvement in harmonic suppression may not be achievable over the complete operating frequency band or input dynamic range in question. Optimization constraints for harmonic suppression must therefore be requirement-specific to achieve the optimal response during normal operating conditions.

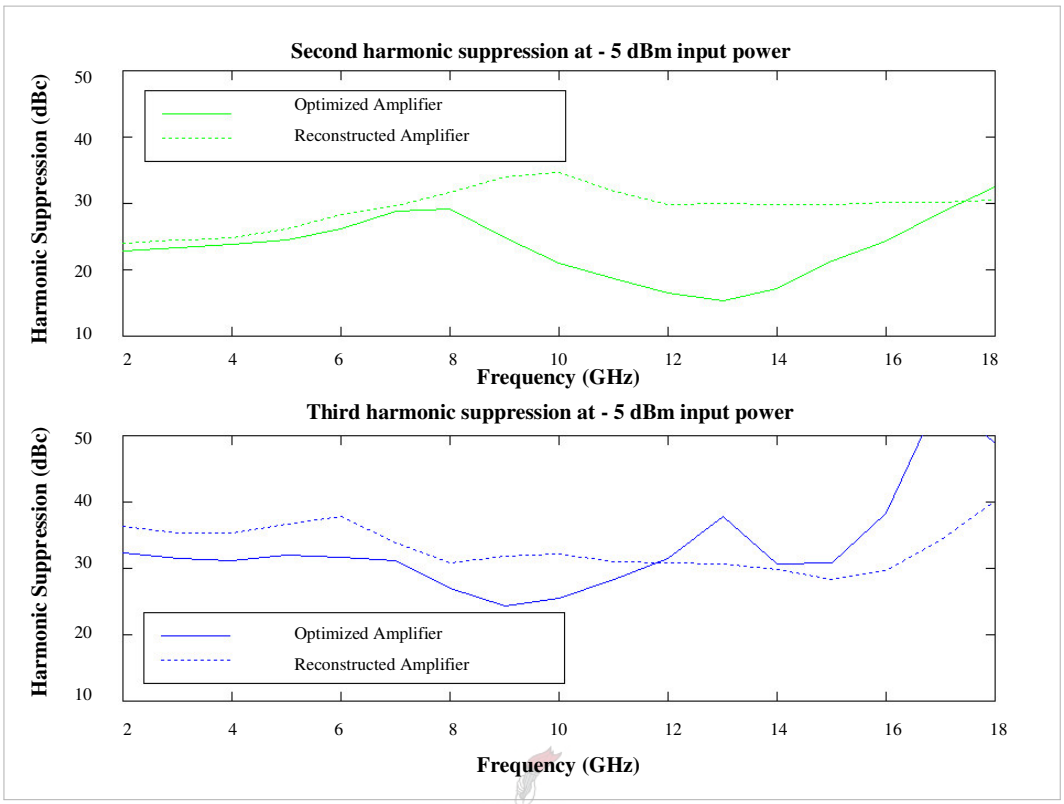


Figure 4.24: Harmonic suppression as measured at - 5 dBm input power

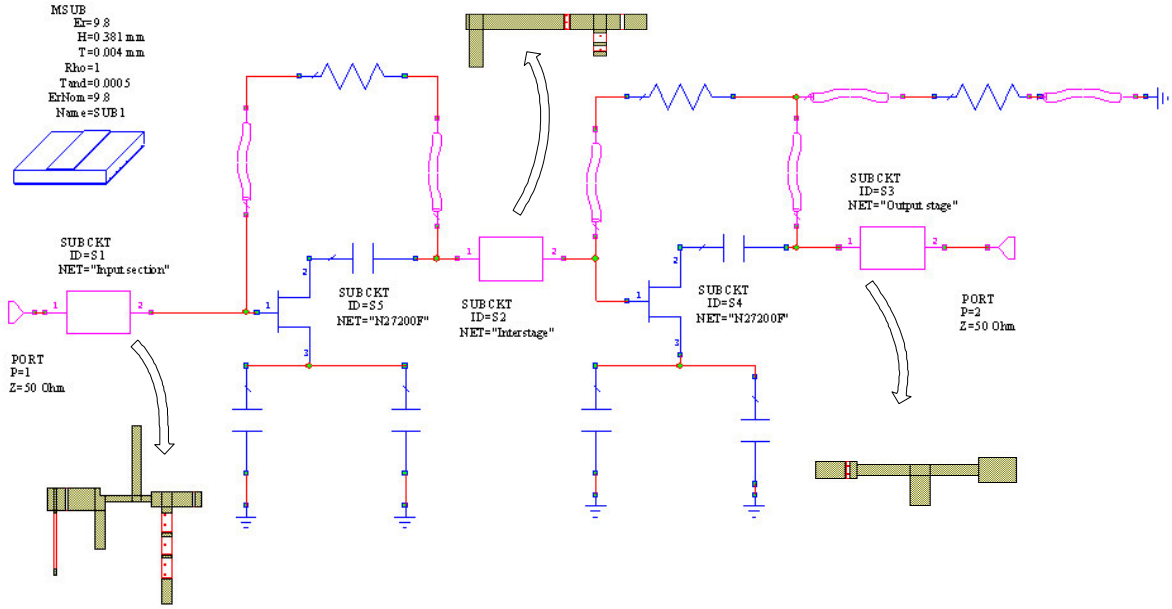


Figure 4.25: Schematic layout of the optimized amplifier

Figure 4.25 shows the layout of the optimized amplifier together with the artwork of the associated matching networks. Figure 4.26 shows part of the assembly of the actual built optimized amplifier.

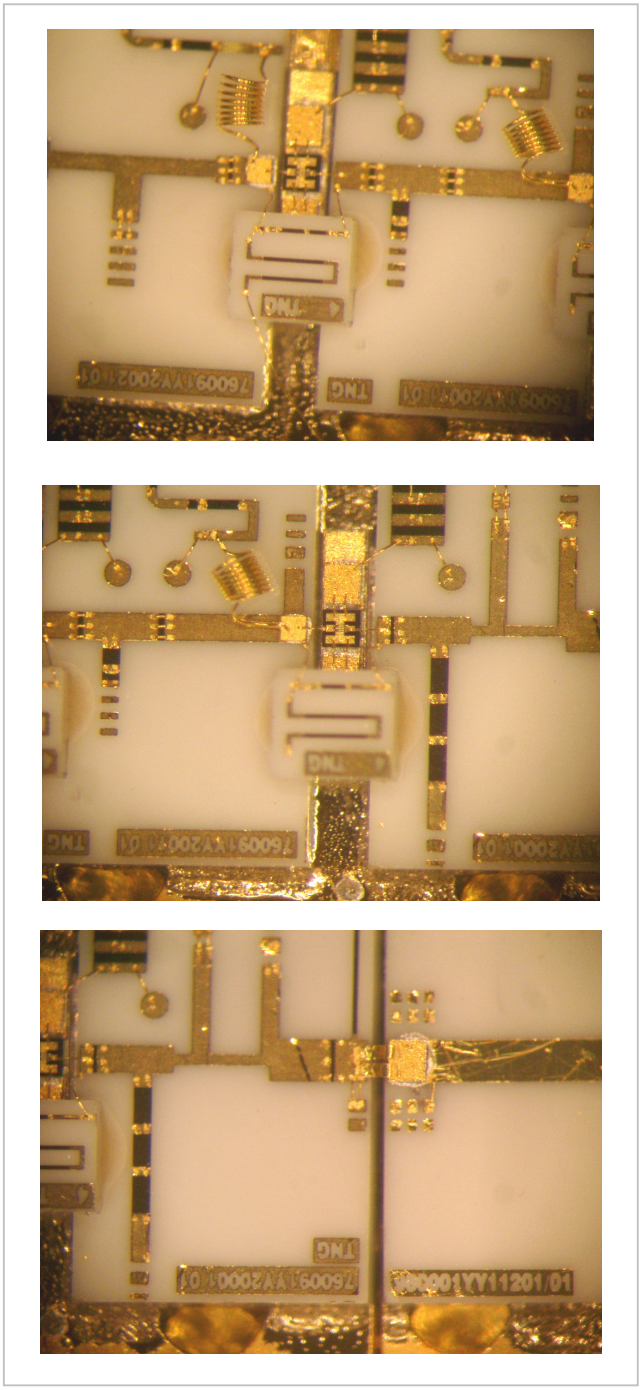


Figure 4.26: Assembly of the actual optimized amplifier

4.8 LOAD PULLING

Load pull measurements consist of varying or *pulling* the load impedance seen by a device-under-test while measuring its performance [31]. This is particularly useful in characterizing a device's behaviour in actual operating conditions. An amplifier may for example be characterized by the contours of its load impedances that result in specific values of output power and gain.

Early research on load pulling was concerned only with the load impedance at the fundamental frequency, not taking into account that the load impedance at harmonics of the excitation signal could significantly affect circuit performance [9]. More recent research suggests harmonic load pull measurements, which allows for the design of matching networks optimized for both fundamental and harmonic impedances ([31], [32]). In the case of broadband designs, however, one may not have the flexibility in selecting proper harmonic terminations since several harmonics may fall within the amplifier's operating bandwidth. Despite this, load pulling may still offer a better initial design approach, from where optimization can be done, as compared to a design done in *MultiMatch*. In terms of load impedances, *MultiMatch* is concerned mainly with the load required for flat compressed output power over the frequency band of interest. Load pulling, however, is a field of study on its own and is mentioned only as a consideration for designs. Rather than doing in-depth designs using load pulling, the design approach followed in this study was to do RF amplifier designs in *MultiMatch* and to optimize them in MWO for use in a limiting amplifier configuration.

4.9 CONCLUSION

Some of the prominent nonlinearities associated with the RF amplifiers to be used in a limiting amplifier were discussed in this chapter while the nonlinear analysis methods to predict the occurrence thereof, were investigated. It was shown that *Microwave Office* offers a powerful tool for improving the large-signal response of an originally small-signal amplifier design, without having to resort to complex design techniques implementing load pull data.

Using the acquired knowledge on the RF amplifier and its associated nonlinear behaviour, one may proceed to formulating a design hypothesis for implementing a broadband limiting amplifier. Chapter 5 formulates the design hypothesis for the proposed limiting amplifier design, as based on the discussed *baseline* limiting amplifier. The hypothesis is evaluated in terms of simulations done on a proposed design configuration.

CHAPTER 5

THE LIMITING AMPLIFIER DESIGN AS SIMULATED

5.1 INTRODUCTION

This chapter discusses the design of a *backbone* limiting amplifier (BLA) to be used as part of a configuration, similar to the discussed *baseline*. A proposed modular design approach, requiring a fully functional limiting amplifier, or *backbone* limiting amplifier (BLA), so-called because it is the most essential part of the modular designed limiting amplifier, is investigated. Suggestions as to the use of a modular limiting amplifier design approach to comply with initial set specifications will be given, but not physically implemented. Rather, the design principles that were followed to implement the BLA design in *Microwave Office* are discussed. A design hypothesis as based on the existing *baseline* limiting amplifier is formulated from where the actual design was implemented for functional evaluation. The functional evaluation implements harmonic balance (HB) analysis techniques and is based on the assumption that the nonlinear models for the devices used give true representations of the physical device characteristics. The amplifier stages comprising the proposed BLA design are analyzed and discussed from the output to the input of the RF chain, while giving a better insight as to each stage's functional role. A complete evaluation is then done on the proposed BLA to further assess the design formulation.

5.2 DESIGN HYPOTHESIS

To formulate the design hypothesis it is necessary to revisit the previously discussed *baseline* limiting amplifier configuration as shown in Figure 5.1. This figure shows the gain (G) and output 1 dB compression points ($P_{1dB\ (out)}$) of each respective amplifier within the RF chain. Also shown are the losses associated with the Wilkinson splitters. The values assigned in this figure are based on actual measurements but one should allow for variance on these values that may be introduced during actual tuning on these amplifiers.

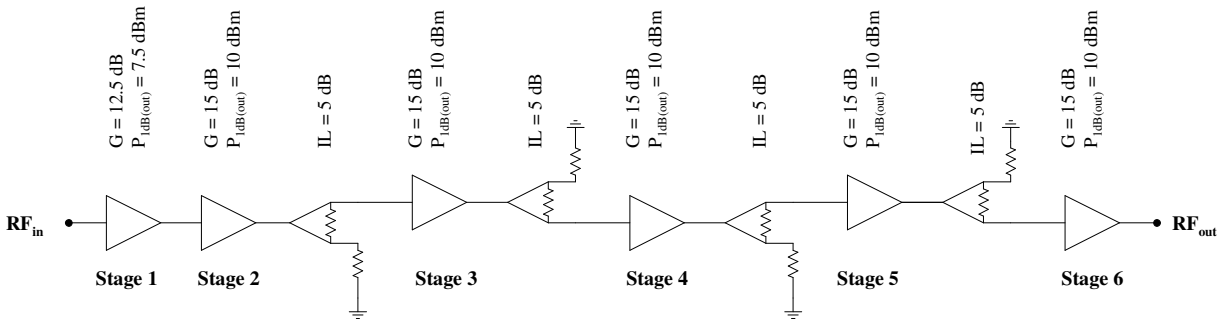


Figure 5.1: Baseline limiting amplifier configuration revisited

The main problem with the shown configuration is amplifiers with relatively high gain and high output 1 dB compression points. This statement is better explained by considering the effect on the amplifiers with a maximum input drive level of 5 dBm present.

When driving the LNA (Stage 1) with a 5 dBm input signal, this amplifier's input 1 dB compression point is significantly exceeded. In fact, this amplifier is driven almost 9 dB into saturation. Not only will the amplifier generate high harmonic levels but the amplifier enters a region of operation where it is increasingly difficult to predict its nonlinear behaviour. A multitude of harmonics is fed through the RF chain which is predicted to deteriorate the limiting amplifier's performance. A deteriorated input and output return loss, due to associated bias point shifts, is predicted while the same deterioration in return loss is also predicted between the different amplifiers within the RF chain. The deteriorated return loss response may be seen as an *attempt* from the respective amplifiers and the complete limiting amplifier to *get rid* of all the extra power that needs to be dissipated. Thus, the input drive levels to the respective amplifiers are reduced due to partial reflection of the relevant incident signals. The degree, to which this deterioration in return loss can be allowed and controlled, requires careful consideration.

With the first stage driven into saturation, one can expect stage two to be driven with a drive level of at least 7.5 dBm. This implies that stage two is driven in excess of 11 dB into saturation. No attenuation was introduced between these two amplifiers, mainly for the sake of achieving the desired input dynamic range. Again, a range of nonlinear phenomena come into play. In an attempt to decrease the interstage drive levels and to reduce interstage reflections, Wilkinson splitters were used between the amplifiers as mentioned earlier. The amplifiers were, however, still being driven heavily into saturation, with all the associated problems with nonlinear operation.

Knowing most of the problems associated with the *baseline* limiting amplifier design, it was decided to base the design hypothesis on a similar, but more subtle approach. In order to achieve the design specifications of a limiting amplifier with an input dynamic range covering - 50 dBm to 5 dBm, a modular design approach is suggested. The modular design approach is based on the principle that a limiting amplifier (similar to the *baseline* design) could be implemented by having a *backbone* limiting amplifier (BLA), to which existing gain modules could be connected. The BLA is typically a limiting amplifier with a limited input dynamic range and with a lower saturated output power than may be desired. This limiting amplifier should be easier to design, implement and evaluate, while the gain blocks connected to it will allow for either a larger saturated output power or for extension of the existing input dynamic range. Figure 5.2 aims to better explain the proposed modular design.

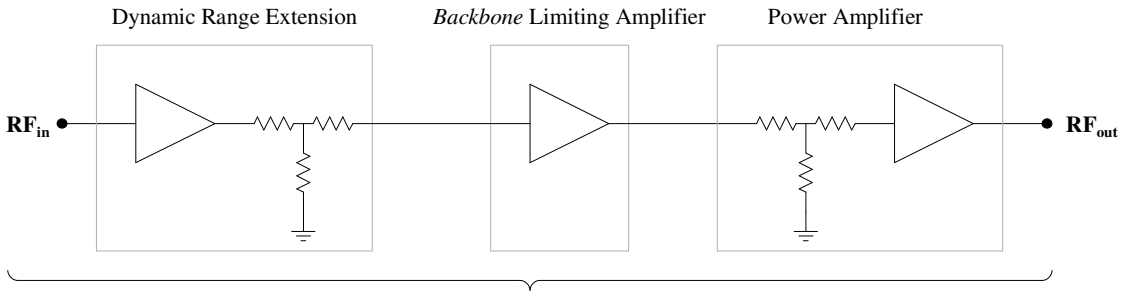


Figure 5.2: The modular limiting amplifier design approach

To achieve the desired output power from the modular designed limiting amplifier, a power amplifier (PA) is used on the output of the BLA. As seen in Figure 5.2, an attenuator forms part of the PA section. The attenuator is desirable in providing isolation between the BLA and the power amplifier, but also to provide the power amplifier with a desirable drive level. To be noted is that the PA need not be operated within its nonlinear region. A small gain ripple from the PA would be of greater concern so as not to deteriorate the ripple presented by the BLA. The attenuator may also be useful in providing slope adjustment to the saturated output power response of the BLA, to provide the modular designed limiting amplifier with a *flat* output power window. The relevance of the proposed slope adjustment will be evident from the simulated response of the BLA, which shows a downward slope toward the higher frequencies.

With the desired output power window established, the next requirement would be to extend the dynamic range of the limiting amplifier. This is done by adding a dynamic range extension (DRE) block. The DRE block will be configured in a very similar fashion to the actual BLA. Its purpose is to provide the gain needed to extend the low end of the limiting amplifier's input dynamic range to - 50 dBm, while providing sufficient harmonic suppression when operated at the intended maximum drive level of 5 dBm. The DRE block would also be optimized for an improved input return loss to compensate for the expected deterioration in return loss as a function of input drive level. Again the attenuator-amplifier configuration is used for reasons discussed earlier.

A design approach, similar to the modular design configuration, is also suggested in [39]. This design approach implements a limiting amplifier consisting of two amplifiers namely a pre-amplifier and a post amplifier. The pre-amplifier is a linear amplifier, while the post amplifier contains the special limiting circuitry [39].

5.3 PROPOSED DESIGN CONFIGURATION

Before going onto the next section, the proposed BLA design configuration is discussed. Important to note at this stage is that this configuration was put together from the knowledge obtained from actual measurements done on the previously discussed amplifier designs. One is thus rather limited to available designs and the use thereof. The proposed design, implementing the designed single-stage 2-18 GHz amplifier and the optimized two-stage 2-18 GHz amplifier in an attenuator-amplifier configuration, is shown in Figure 5.3. The associated small-signal gain, output 1 dB compression point and noise figure is shown for each of the relevant stages.

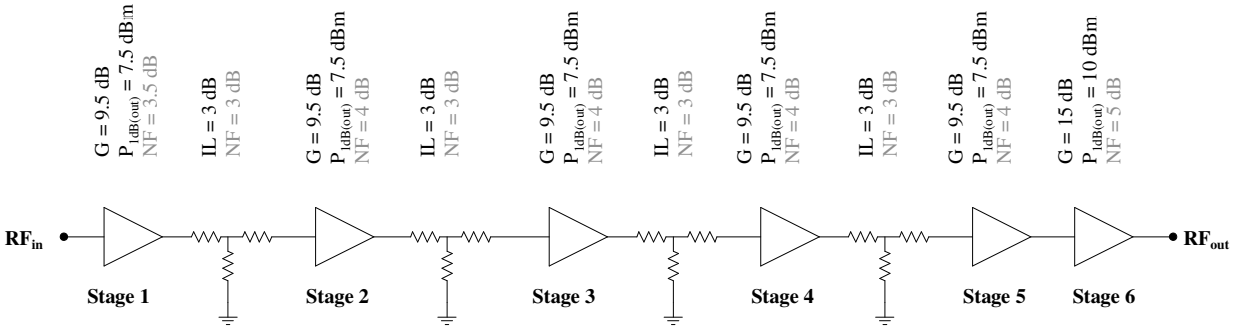


Figure 5.3: Proposed BLA design configuration

The shown configuration implements low-gain amplifiers with low 1 dB output compression points, while only the last amplifier has a larger gain and output 1 dB compression, to achieve some desired saturated output power level. From the configuration shown in Figure 5.3, a small-signal gain of approximately 50 dB is calculated. With an expected saturated output power exceeding 10 dBm, the low end of the proposed BLA's input dynamic range can thus be estimated at about - 40 dBm. At the intended 5 dBm maximum input drive level an intuitive analysis of the limiting amplifier's behaviour is again required.

With a 5 dBm drive level present, the first stage will be driven at least 6 dB into saturation. With the first stage driven into saturation, the drive level to be presented to the next stage is approximately 4.5 dBm, resulting in this amplifier being driven about 5.5 dB into saturation. This was then also the situation for all the following amplifier stages, except the last.

As will be shown in the section to follow, the extent to which each amplifier in the RF chain can handle the drive level that it is subjected to is evaluated and optimized. In doing this, one can actually evaluate each amplifier's *safe limiting region*.

Another attenuator could not be used between the last two stages since this would imply that the low end of the BLA's input dynamic range would be impaired. Thus, with an attenuator used between the last two stages, the last amplifier would not be driven into saturation for a - 40 dBm drive level. Without adding another attenuator between the last two stages, optimization of the last amplifier was necessary, to ensure optimal operation under the increased drive level.

At the low end (- 40 dBm) of the BLA's input dynamic range, one deals with a situation where all the amplifiers within the proposed BLA design configuration, except the last, are operated within their linear regions. Only the last amplifier is driven into compression. The last amplifier therefore remains in saturation over the complete input dynamic range. As the drive level increases, however, all amplifiers will be driven into saturation in sequence from stage five to eventually stage one. When driving the limiting amplifier in the mid-range one may therefore expect that some amplifiers are operated linearly while some are driven well into saturation. It is thus apparent why the small-signal behaviour of the designed amplifiers is as important as their nonlinear behaviour.

As mentioned earlier, the first stage of a proposed limiting amplifier configuration should have a low noise figure. When using the BLA as part of the modular designed limiting amplifier, the focus may rather be placed on the noise figure of the front-end of the dynamic range extension block than that of the BLA. Even though the first stage of the BLA was not designed specifically for low noise, measurements showed that this amplifier offered a noise figure of less than 4 dB as seen in Figure 5.4. A specific low-noise amplifier, for use on the BLA's input, was therefore not designed. The improvement on noise figure in doing such a design would be marginal and not justifiable.

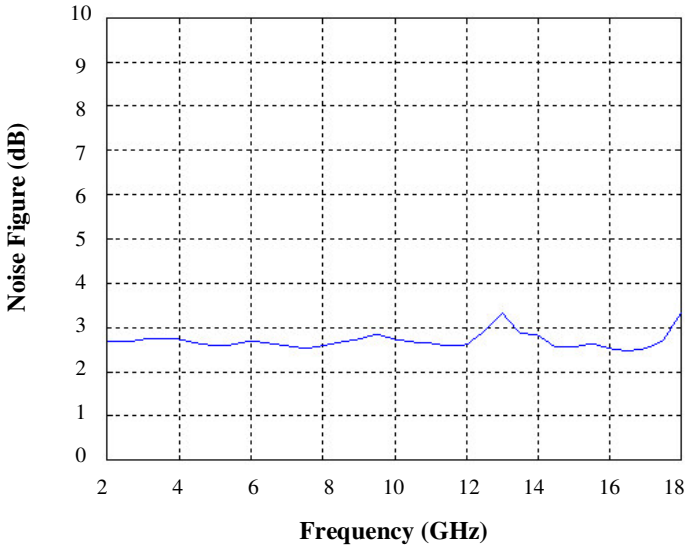


Figure 5.4: Measured noise figure of the designed single-stage 2-18 GHz amplifier

In the proposed BLA design configuration, it was attempted to have the first stage as similar as possible to the original single-stage design, to maintain the achievable noise figure. It will, however, be shown in subsequent sections to what extent this design was altered during implementation as part of the limiting amplifier. The other stages were also altered and optimized within the proposed RF chain, to realize the desired limiting amplifier response. Notwithstanding this, it is not expected that the optimization process too seriously influenced the noise figure of these single-stage amplifiers within the BLA's RF chain. In determining the total noise figure of the BLA design configuration, it was therefore assumed that all the single-stage amplifiers had a noise figure of 4 dB. The total noise figure of the configuration shown in Figure 5.3 is estimated by using the equation for the cascaded noise figure as given by:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots + \frac{F_n - 1}{G_1 G_2 G_3 G_{n-1}} \tag{5.1}$$

Recalling equation (2.3) it is known that F_n is the noise factor of the nth stage and G_n is the gain factor of the nth stage. The different estimated noise factors and gain factors, obtained from Figure 5.3 are summarized in Table 5.1.

$F_1 = 10^{\frac{3.5}{10}} = 2.24$	$G_1 = G_3 = G_5 = G_7 = G_9 = 10^{\frac{9.5}{10}} = 8.91$
$F_2 = F_4 = F_6 = F_8 = 10^{\frac{3}{10}} = 2$	$G_2 = G_4 = G_6 = G_8 = 10^{\frac{-3}{10}} = 0.5$
$F_3 = F_5 = F_7 = F_9 = 10^{\frac{4}{10}} = 2.51$	$G_{10} = 10^{\frac{15}{10}} = 31.62$
$F_{10} = 10^{\frac{5}{10}} = 3.16$	

Table 5.1: Estimated gain and noise factors for the BLA

Using equation (5.1) and the given gain and noise factors in Table 5.1, the cascaded noise factor is calculated to be 2.8, which relates to a cascaded noise figure of about 4.5 dB. In terms of noise figure, the BLA offers a reasonably good noise figure, which allows for operation without an extra low-noise stage on its input.

Seen as a whole, the proposed BLA configuration would offer a much more subtle design approach when compared to the *baseline* limiting amplifier design. The different amplifier stages, although driven well into saturation, are not driven as hard as the amplifiers used in the *baseline* design and should therefore offer a much better harmonic response.

The best evaluation of the proposed design configuration could, however, only be done by implementing the design in *Microwave Office*. In doing this, one may establish a far better feel for the actual nonlinear behaviour of the amplifiers within the proposed RF chain and it could be shown to which extent a limiting amplifier is realizable.

Actual simulations, however, included a rather significant discrepancy that was included in the final BLA design, that needs mentioning. The discrepancy was introduced by the model of the NE321000 HJFET. Although the nonlinear model provided a very good match with the measured S-parameter model, the measured and simulated 1 dB compression points did not match very well. The typical measured output power at 1 dB compression was about 7.5 dBm while that simulated was in the order of 9.5 dBm. This discrepancy should be kept in mind during the discussion on the first five amplifier stages. On the other hand greater confidence exists in the nonlinear model of the NE27200 HJFET and it is accepted that the simulated results will give a true representation of what is practically expected from this device.

5.4 EVALUATION OF THE DIFFERENT AMPLIFIER STAGES

The different amplifier stages comprising the proposed BLA design are discussed hereafter in terms of their functional characteristics required for use within the proposed RF chain. Each amplifier was initially tuned and optimized separately from the complete limiting amplifier RF chain. Only thereafter was tuning and optimization done on the complete assembled limiting amplifier RF chain. Optimization constraints were set up to achieve the desired limiting amplifier response while not allowing for serious deterioration of initial optimized amplifier responses. The results discussed hereafter are that obtained after optimization of the different amplifiers as used within the limiting amplifier. The discussion to follow serves as reference only for doing the limiting amplifier design, while the mentioned nonlinear model discrepancy should be kept in mind. The design configuration showed in Figure 5.3 will offer a much more accurate representation of actual expected compression points and signal power levels.

The schematic layouts of the amplifiers comprising the BLA design are not given in this chapter, but are shown in Appendix F, to allow for reconstruction of the design, if so required. Each stage is evaluated separately in terms of operation under single-tone excitation. In doing this, a better intuitive feel is established as to the expected behaviour of each of the amplifiers. An initial single-tone test was done on the complete BLA to establish the presence of the relevant frequency spectra at each stage of the design configuration. This was done by including ideal 20 dB couplers in MWO at the relevant stages. These couplers included 0 dB residual transmission loss so as not to influence the signal transmission through the BLA's RF chain. Only a small portion of the signal powers present at relevant nodes within the design configuration was therefore *tapped* off for evaluation. Figure 5.5 shows a portion of the BLA design configuration with the ideal couplers in place.

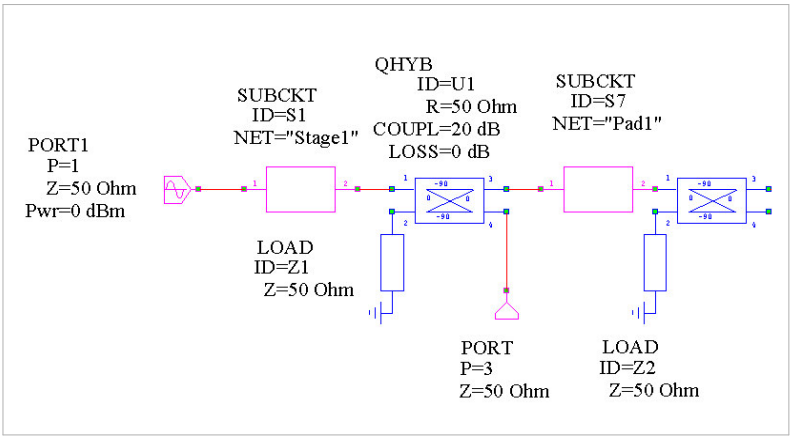


Figure 5.5: Portion of the BLA configuration for spectral analysis

The actual simulation in MWO is therefore concerned with the frequency components at each of the coupled ports within the RF chain. To get the actual level of the frequency components within the transmission path, 20 dB should be added to the level of each frequency component as measured on the coupled path. This calculation is already included in all the spectral analyses to follow.

Figure 5.6 shows a portion of the spectral analysis that was done on the BLA for a 2 GHz input signal at a 0 dBm drive level. The result show harmonics only up to the fourth order with the level of these fourth order harmonics being generally suppressed well below that of the fundamental. Therefore, measurements to follow will be concerned mainly with harmonics up to the third order.

This type of measurement can be done at each point of interest within the RF chain and allows for an in-depth analysis of the frequency components generated within the RF chain. It should, however, be noted that the results obtained from these coupled measurements only give an estimate of what happens within the RF chain. This is due to the fact that the couplers have a loading effect that could influence the actual device performance. This was also confirmed during simulations. Ideally, a *probe* that does not influence the device behaviour in any manner should be used. Physical measurements of this nature can typically not be done and again necessitates the need for a proper simulated design that will accurately predict the physical device performance.

From the spectral analysis, important deductions can be made regarding the frequency components generated within the shown RF chain. It is seen that the first amplifier and the amplifiers following it, generate harmonics that get *fed* through the RF chain. It appears as though there are no intermodulation products but only pure harmonics of the input signal. This, however, is not the case, as one now deals with harmonically related tones. The generated intermodulation products are thus present at exactly the same frequencies as the fundamental and its harmonics. The physical levels of the generated frequency products are therefore influenced by the intermodulation contribution in question. For the purpose of evaluation, the different amplifiers making up the BLA's RF chain were initially evaluated only in terms of single-tone excitation. In sections to follow, the behaviour of the different amplifiers within the BLA's RF chain, under actual multi-tone excitation will be evaluated.

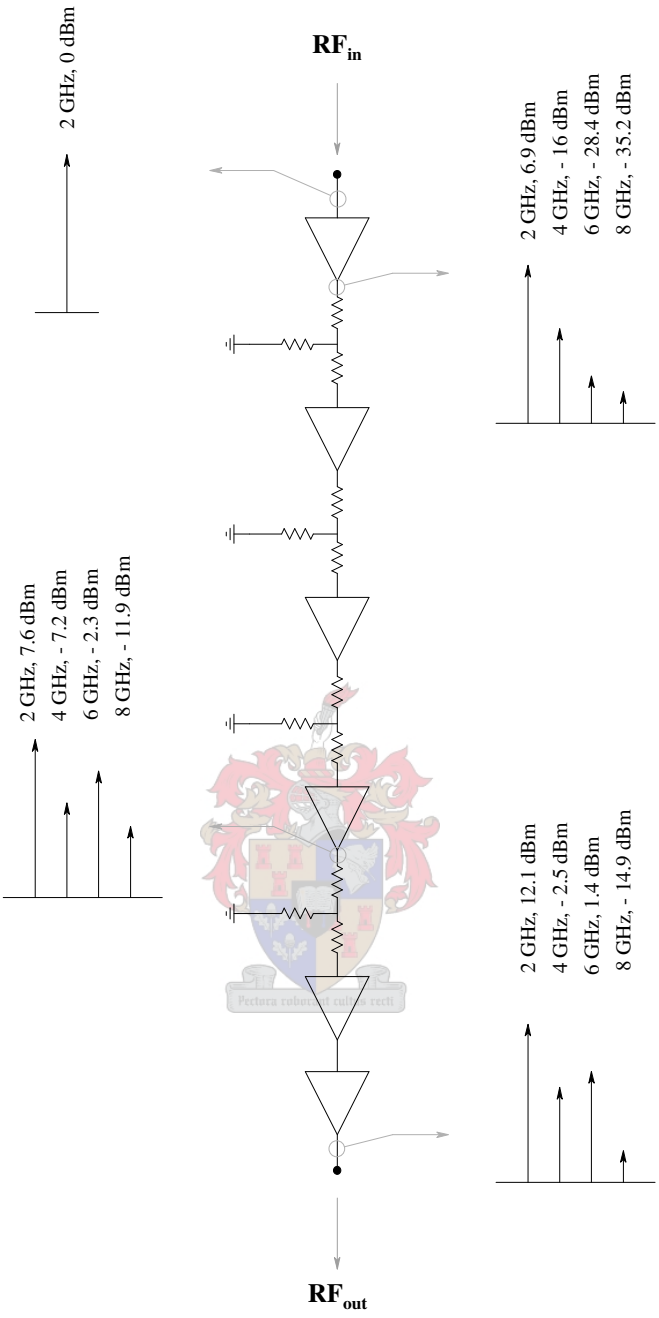


Figure 5.6: Portion of the BLA spectral analysis

5.4.1 EVALUATION OF STAGE SIX

The last stage (Stage 6) of the proposed limiting amplifier or BLA design, consists of the reconstructed two-stage amplifier as discussed previously in Chapter 4. This amplifier is chosen for the last stage, mainly for its higher output power and gain as compared with the single-stage amplifier design that was done. In deciding on the requirements for stage number five, it was deemed necessary to first evaluate the last stage in further detail.

Of particular concern is the maximum drive level that could be presented to the last stage without causing undesired harmonic generation. It was already mentioned that an attenuator could not be used between the last two stages, so it was important to evaluate the last stage's behaviour under an increased drive level. Also important to know is what drive level would be required to drive the relevant stage into saturation. It was decided upon using both input and output 1 dB compression points as reference for evaluation. Figure 5.7 shows the input 1 dB compression response for the last stage. The maximum point on this plot is at about - 3.8 dBm. This requires that the minimum drive level of stage five exceed at least this value to ensure a saturated output power response from the last amplifier stage. This requirement should be adhered to over the entire input dynamic range of the limiting amplifier.

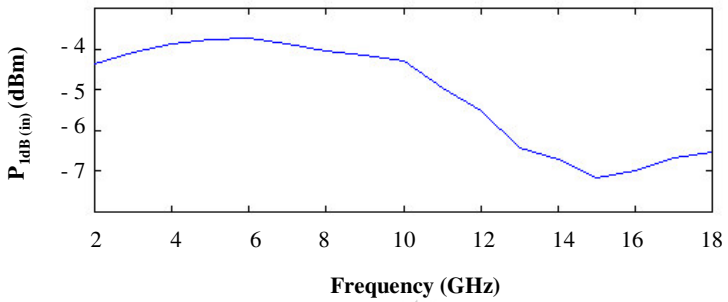


Figure 5.7: Input 1 dB compression response for the last stage

To establish the maximum drive level to be presented to the last stage, its harmonic response above an input drive level of - 3.8 dBm was monitored. The result of the amplifier's harmonic suppression response, as measured for an input drive level of 7 dBm is shown in Figure 5.8. The three traces show the fundamental (blue), second harmonic suppression (pink) and the third harmonic suppression (brown) response respectively. The amplifier's minimum harmonic suppression (second harmonic suppression in this case) exceeds 9 dBc. It was also confirmed that the harmonic suppression at a 9 dBm drive level was approximately 9 dBc. The upper limit on the input drive level of the last stage and the drive level required from stage five is thus automatically set for the case where the limiting amplifier is operated at the high end of its input dynamic range.

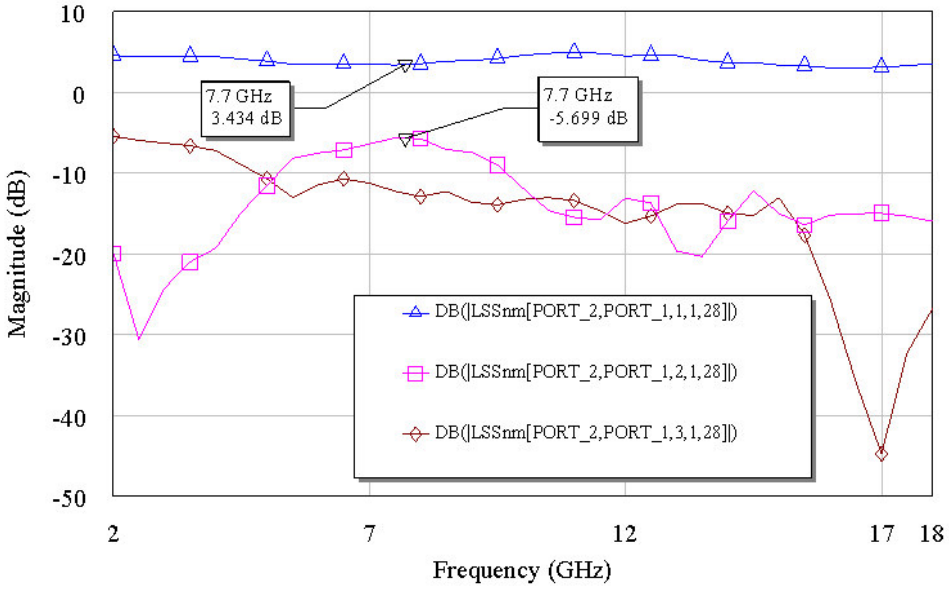


Figure 5.8: Simulated harmonic response of the last amplifier stage for a 7 dBm drive level

The output 1 dB compression response for the last stage is shown in Figure 5.9. Noticeable is the amplifier's flat compressed output power. This can already give an idea as to the expected output power window from the proposed limiting amplifier. The shown response is further sufficient in establishing an intuitive feel for the expected saturated output power since one can expect the saturated output power to be at least higher than the output 1 dB compression point.

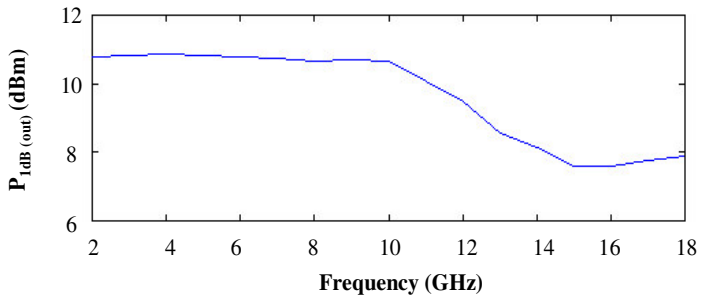


Figure 5.9: Output 1 dB compression response of stage six

With the necessary operating conditions established for the last stage, the next step would be to evaluate the actual gain and return loss response of the amplifier as shown in Figure 5.10. Special effort was expended to get the particular amplifier's gain as flat possible and to achieve a good return loss response. A gain of about 15.8 dB was achieved, with a gain ripple of ± 0.4 dB.

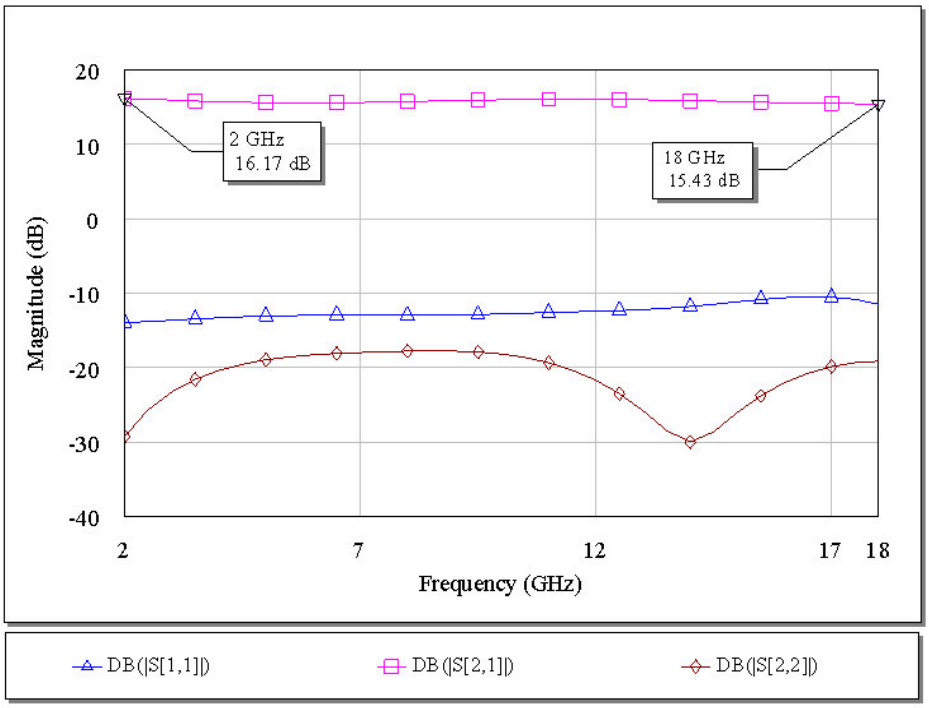


Figure 5.10: Small-signal gain response of the last stage amplifier

The question remains to what extent the shown gain and return loss response would be altered if the amplifier was exposed to increased input drive levels. For this reason, the large-signal S-parameters were monitored while the input drive levels were varied between - 3.8 dBm and 7 dBm. Only the simulated results for a drive level of - 3.8 dBm and 7 dBm, respectively, are discussed hereafter.

The gain response of the last stage amplifier as monitored for an input drive level of - 3.8 dBm is shown in Figure 5.11. When compared to the small-signal response, no deterioration in the input return loss is observed. Not shown in this plot is the output return loss response that could not be accurately measured as a function of input drive level. Interestingly, the transition from the amplifier's linear region to its nonlinear region is clearly shown in the plot. It is seen that the gain is slightly less than that measured from the small-signal response indicating the initiation of gain compression.

Revisiting the input 1 dB compression plot (Figure 5.7), for this particular amplifier, one can see that gain compression occurs at 5 GHz, for a - 3.8 dBm drive level. At frequencies above 10 GHz, however, the amplifier is already well above its 1 dB compression point, when driven at - 3.8 dBm. One would, therefore, expect the gain to decrease at these frequencies due to premature gain compression and the onset of saturation. This would then also explain the drop in gain at the higher frequencies (above 10 GHz) as seen in Figure 5.11. In terms of gain ripple, a deterioration of approximately ± 1 dB is observed.

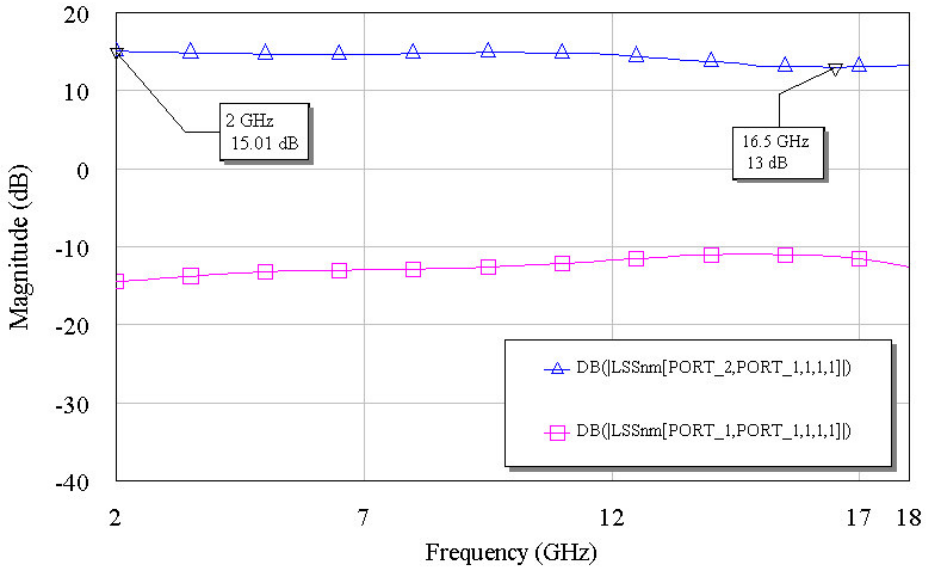


Figure 5.11: Gain response of the last stage amplifier for a - 3.8 dBm drive level

In terms of actual gain, one can expect it to decrease as the input drive level increases, due to the onset of gain compression and eventual saturation as pointed out earlier. Possible deterioration in the gain ripple and the return loss response should, however, be monitored.

Figure 5.12 shows the response of the last stage for a drive level of 7 dBm. The simulated response shows that the gain decreased as expected but also that the gain ripple deteriorated to approximately ± 0.9 dB. Furthermore, it is seen that the input return loss has deteriorated somewhat.

This result suggests that one may rather need to place more focus on the large-signal gain response of the last stage than its small-signal gain response since this stage will be constantly exposed to increased drive levels. The small-signal gain response, on the other hand, will be much more prominent at the low end of the limiting amplifier's input dynamic range.

In terms of the input return loss, one may expect deterioration as the drive level increases. For this reason, the design criteria should always be for optimum input return loss, so as to simplify cascading the last stage with a driver amplifier. It would also serve to compensate to some degree, for the expected return loss deterioration. In terms of the output return loss, no clear prediction as to its change as a function of input drive level was obtained. As a precautionary note, it should be assumed that the output return loss will also deteriorate as the amplifier's input drive level increases. Therefore, the last stage's output return loss should be optimized over the operating frequency band, while the load matching circuit should still provide for a flat output power response.

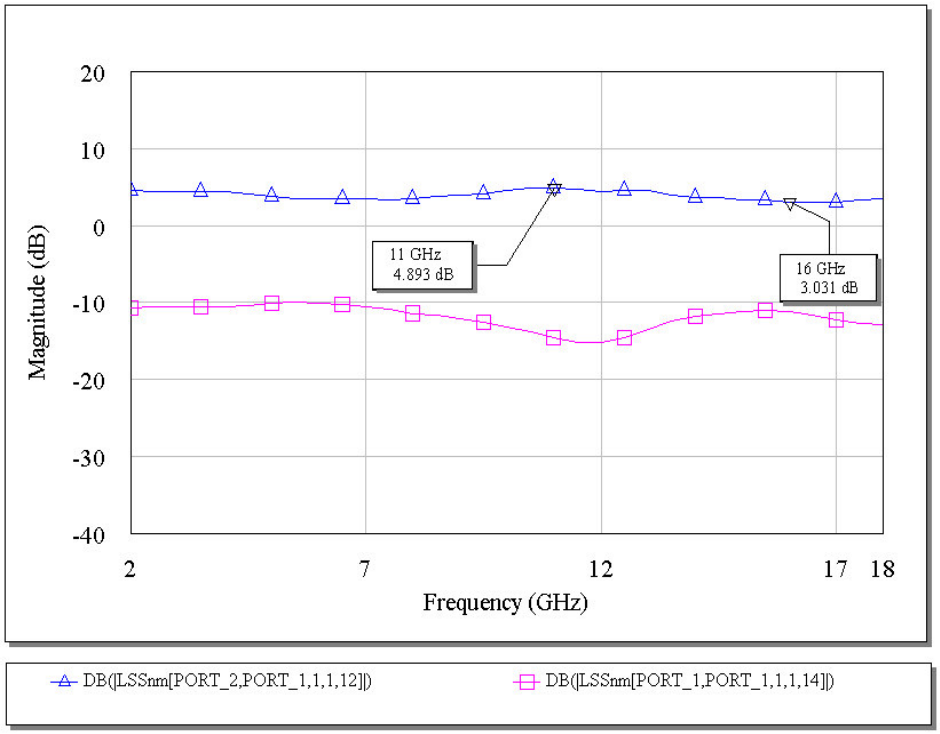


Figure 5.12: Gain response of the last amplifier stage for a 7 dBm drive level

The proposed amplifier to be used as last stage on the limiting amplifier has been discussed to such extent that this amplifier can be used with confidence in the proposed limiting amplifier configuration. The next step would be to evaluate and discuss the amplifier to be used as driver for the last stage. The evaluation of amplifier stage number five is discussed in the following section.

5.4.2 EVALUATION OF STAGE FIVE

As was done for the last stage, stage five will be evaluated in terms of the necessary operating criteria for use in the proposed limiting amplifier's RF chain. Stage five consists of the single-stage 2-18 GHz amplifier discussed earlier in Chapter 3. All the other stages made use of the same single-stage amplifier as baseline, but for each stage, the baseline was optimized for particular design criteria to ensure the eventual operation of the limiting amplifier. Some subtle differences in the responses of the first five amplifiers will therefore be seen mainly as a result of optimization and attempting to break the uniformity of these amplifiers. In doing so, it was ensured that five exactly similar amplifiers were not used in the limiting amplifier RF chain, for reasons discussed earlier. The first five amplifier stages then also made use of the proposed amplifier-attenuator configuration. Figure 5.13 shows the small-signal gain response of stage five. The gain is centred at approximately 9.9 dB with a gain ripple of about ± 0.4 dB.

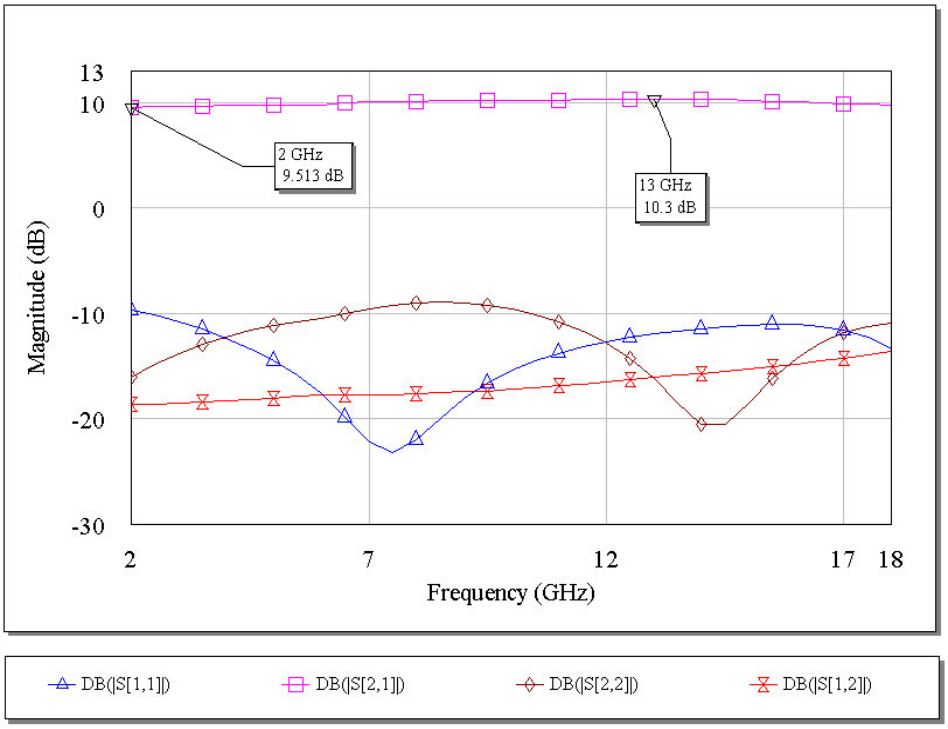


Figure 5.13: Small-signal gain response of the stage five

Figure 5.14 shows the input 1 dB compression response for stage five. The maximum point on this plot is at about 1.9 dBm. This requires that the drive level presented to stage five exceeds this value to ensure a saturated output power from it. Unlike the last stage that was driven close to its maximum allowable drive level to ensure a flat saturated output power, while still staying within the harmonic suppression specification, stage five was not exposed to unwanted overdrive. This was done to ensure that stage five did not introduce any undesired harmonic levels that would be *fed* to the last stage. For this reason, the drive level of stage four would be attenuated down to a level that will ensure the onset of gain compression while still ensuring good harmonic suppression.

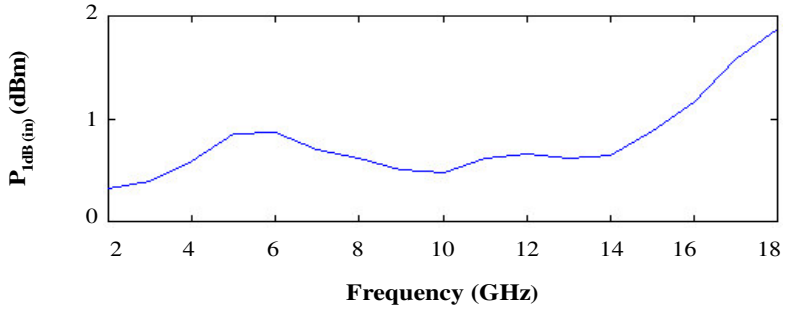


Figure 5.14: Input 1 dB compression response for stage five

Figure 5.15 shows a simulation to determine the harmonic response of the fifth stage for a drive level of 7 dBm. This drive level represents an estimate of the drive level that this amplifier will be exposed to, during operation within the limiting amplifier chain. The shown harmonic suppression is in excess of 10 dBc.

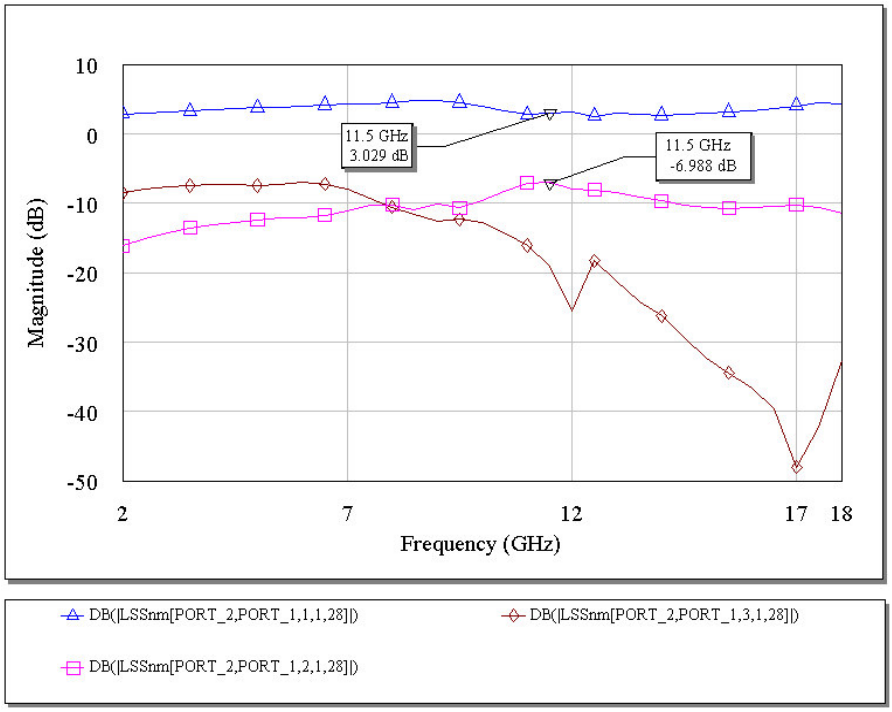


Figure 5.15: Simulated harmonic response of stage five for a 7 dBm drive level

Figure 5.16 shows the output 1 dB compression response for the fifth amplifier stage. From the shown response one may establish an intuitive feel for the expected output power from this stage, when driven above the desired 1.9 dBm input power. Also apparent then is the fact that the drive level to be presented to the last stage will be adequate to ensure a flat saturated output power while achieving the desired harmonic suppression on the output of the limiting amplifier.

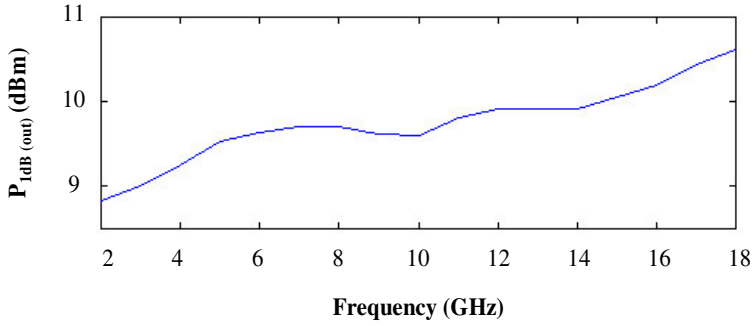


Figure 5.16: Output 1 dB compression response for stage five

5.4.3 EVALUATION OF STAGE FOUR

Shown in Figure 5.17 is the small-signal gain response of fourth stage amplifier. The gain is centred at approximately 9.9 dB with a gain ripple of ± 0.45 dB. A slightly deteriorated input return loss is seen at the low end and at the high end of the frequency band. A discussion to follow in this section, will explain why this deterioration is allowed.

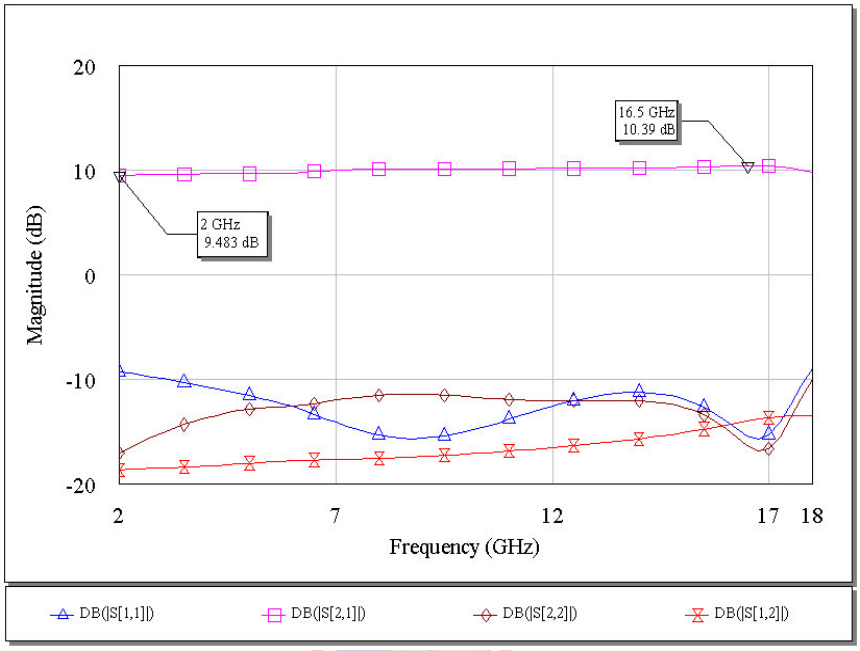


Figure 5.17: Small-signal gain response of the stage four

The evaluation of stage four can be done in a similar fashion as was done for the previous two stages. From Figure 5.18 it can be seen that the maximum point on the input 1 dB compression response is approximately 1.3 dBm. Again, the requirement for the minimum drive level that should be presented to this stage is set.

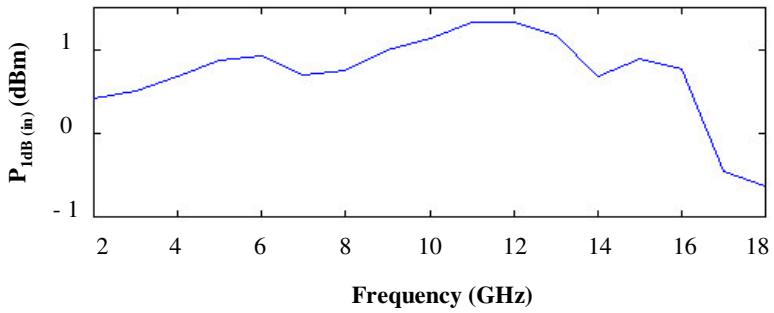


Figure 5.18: Input 1 dB compression response for stage four

From the output 1 dB compression response for stage four, as seen in Figure 5.19, one can again get an idea of the expected drive level to be presented to stage five. The maximum point on this plot is approximately 10.5 dBm. In the previous section it was mentioned that stage five will offer harmonic suppression in excess of 10 dBc when driven at approximately 7 dBm. Increasing the drive level presented to stage five too far beyond 7 dBm would lead to deterioration in harmonic suppression. Knowing this, a 3 dB attenuator can be used between stage four and five to decrease the drive level to be presented to stage five, to a more desirable level. Another useful aspect of the interstage attenuator is that it helps improve on interstage impedance matching while allowing for some *slack* in the input- and output return loss of the individual amplifiers without negatively affecting the limiting amplifier's overall response.

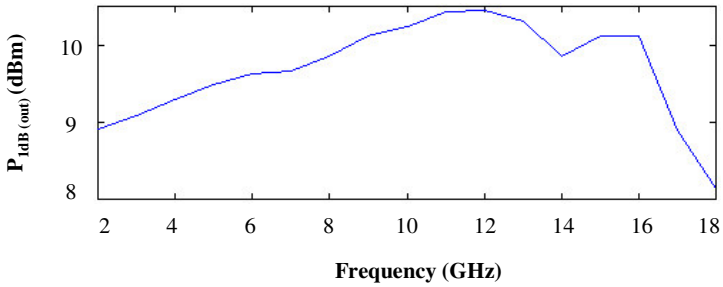


Figure 5.19: Output 1 dB compression response for stage four

With the minimum required drive level for stage four known, the typical maximum drive level to be presented to this stage can again be determined from simulations. Figure 5.20 shows the result of this simulation, where it is again seen that the amplifier will offer harmonic suppression in excess of 10 dBc when driven at 7 dBm.

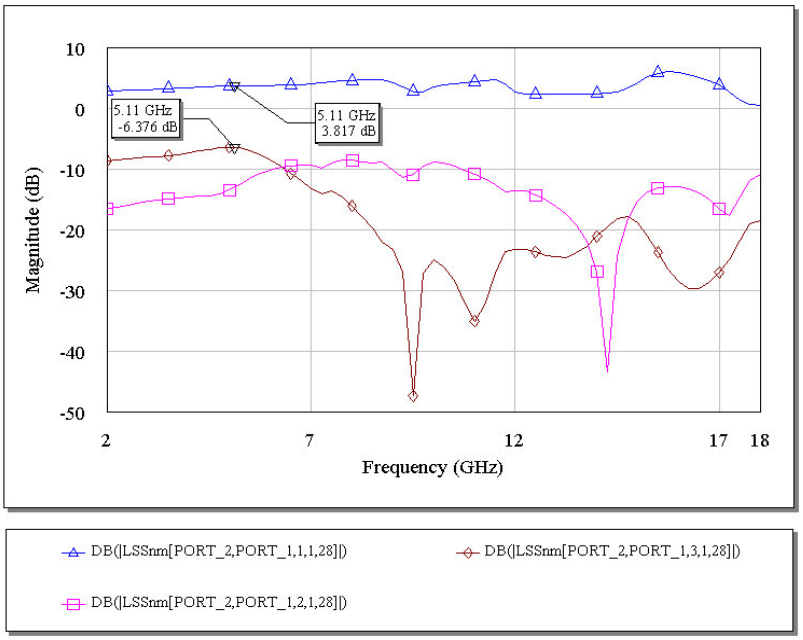


Figure 5.20: Simulated harmonic response of stage four for a 7 dBm drive level

5.4.4 EVALUATION OF STAGES TWO AND THREE

Stage two and three amplifiers were evaluated in a similar fashion as the previously discussed amplifier stages. Only a summary of these stages' simulated results will be given in this section, however. Not only do they have very similar gain and compression responses as that of stage four and five, but they also offer similar harmonic suppression at their intended maximum drive levels.

Figure 5.21 shows the small-signal gain response of stage three. Again the gain (10 dB) of stage three is very similar to that of stages four and five, while it offers ± 0.6 dB gain ripple. Figure 5.22 and Figure 5.23 show the input and output 1 dB compression responses respectively.

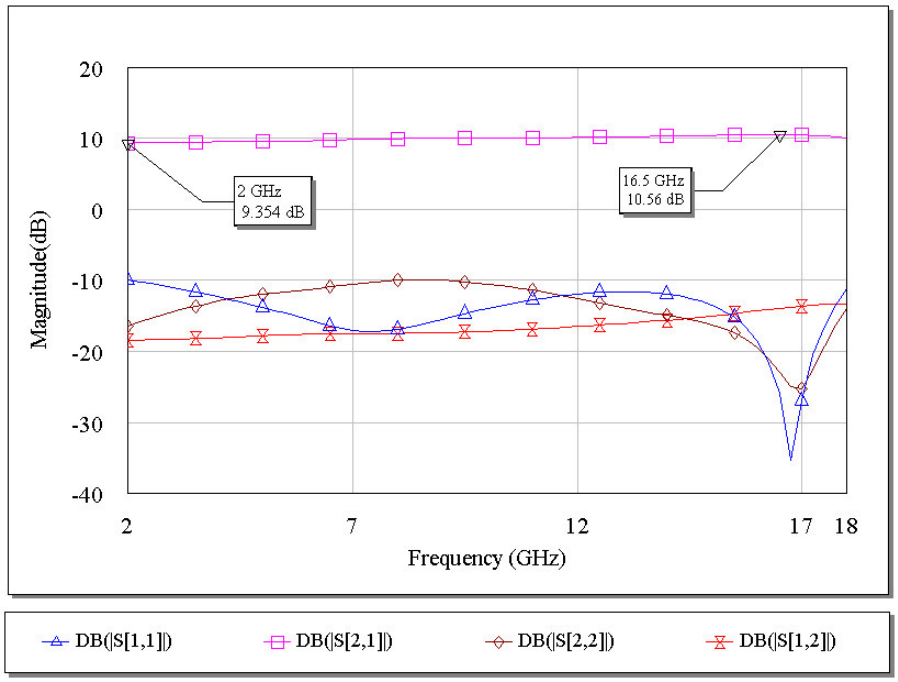


Figure 5.21: Small-signal gain response of stage three

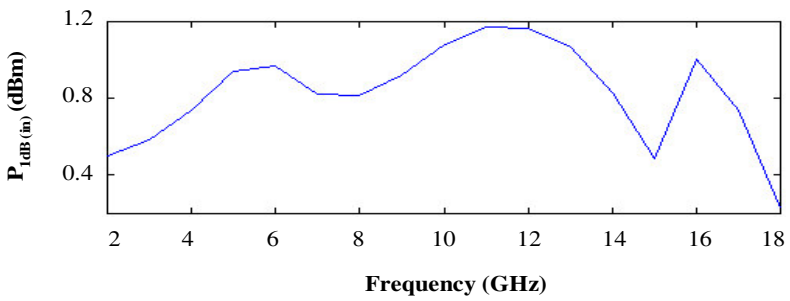


Figure 5.22: Input 1 dB compression response for stage three

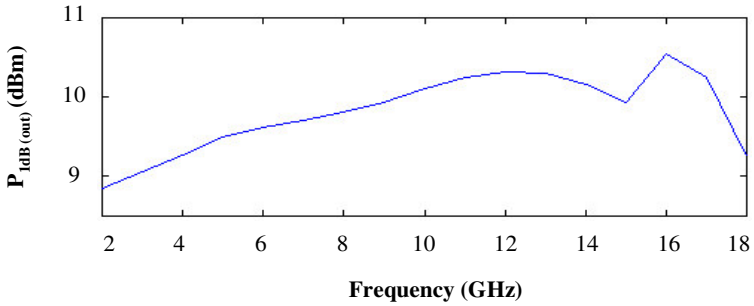


Figure 5.23: Output 1 dB compression response for stage three

From Figure 5.24 it is seen that stage two offers a gain of 9.9 dB with a gain ripple of ± 0.6 dB. Both input and output return loss is better than 10 dB. Comparing this plot to that shown in Figure 5.21, one can see the similarities between the shown results, but also the subtle differences that were introduced during tuning and optimization.

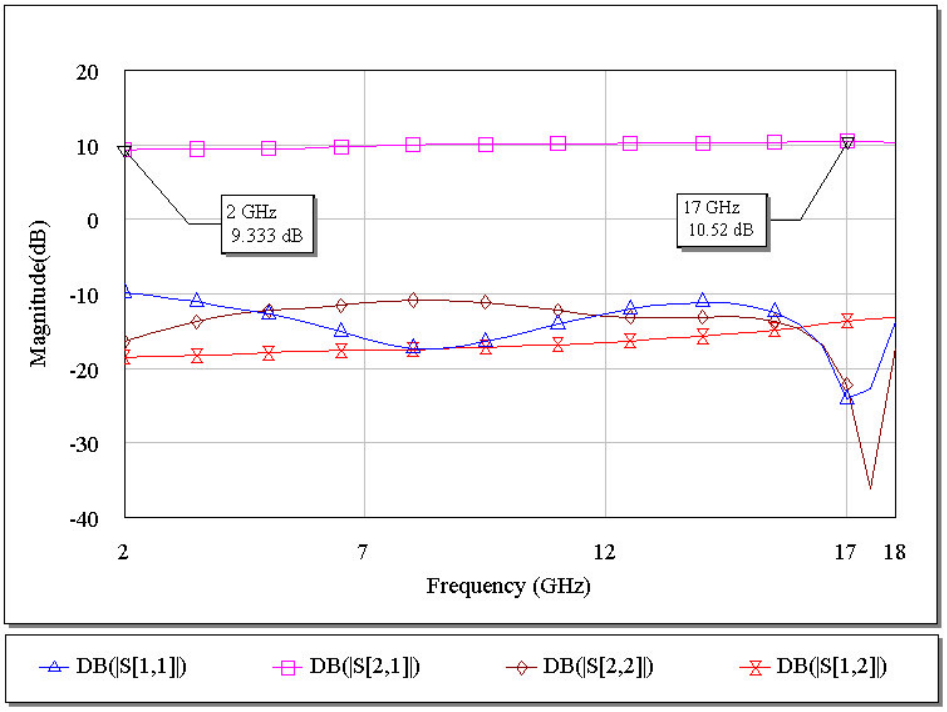


Figure 5.24: Small-signal gain response of stage two

Figure 5.25 and Figure 5.26 shows the input and output 1 dB compression responses of stage two, respectively. It is apparent that stage two offers a very similar response to that of stage three. Not only is there a close comparison between the compression responses for the two amplifiers, but the gain of stage two (9.9 dB) is also comparable with that of stage three.

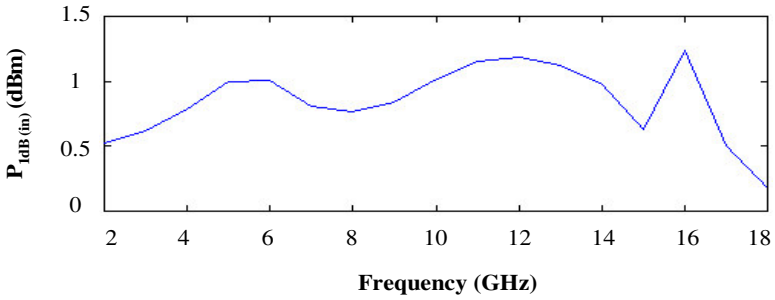


Figure 5.25: Input 1 dB compression response for stage two

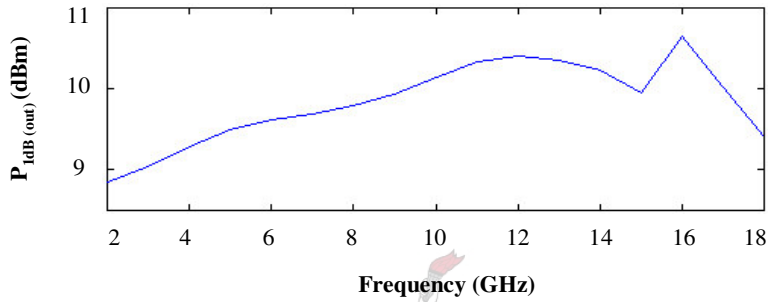


Figure 5.26: Output 1 dB compression response for stage two

5.4.5 EVALUATION OF STAGE ONE

The gain response of the first amplifier stage is shown in Figure 5.27. This amplifier offers a gain of approximately 9.8 dB with a gain ripple of about ± 0.5 dB. The input and output return loss is typically better than 10 dB. It was mentioned that this amplifier was kept as similar possible to the initial 2-18 GHz single-stage amplifier that was done. Compared to the amplifier's response initially shown in Figure 3.30, there are some subtle differences in the observed responses that were introduced during tuning and optimization. Actual implementation also required alteration of the initial design. The only negative aspect of this alteration was a possible deterioration in the noise figure of this amplifier.

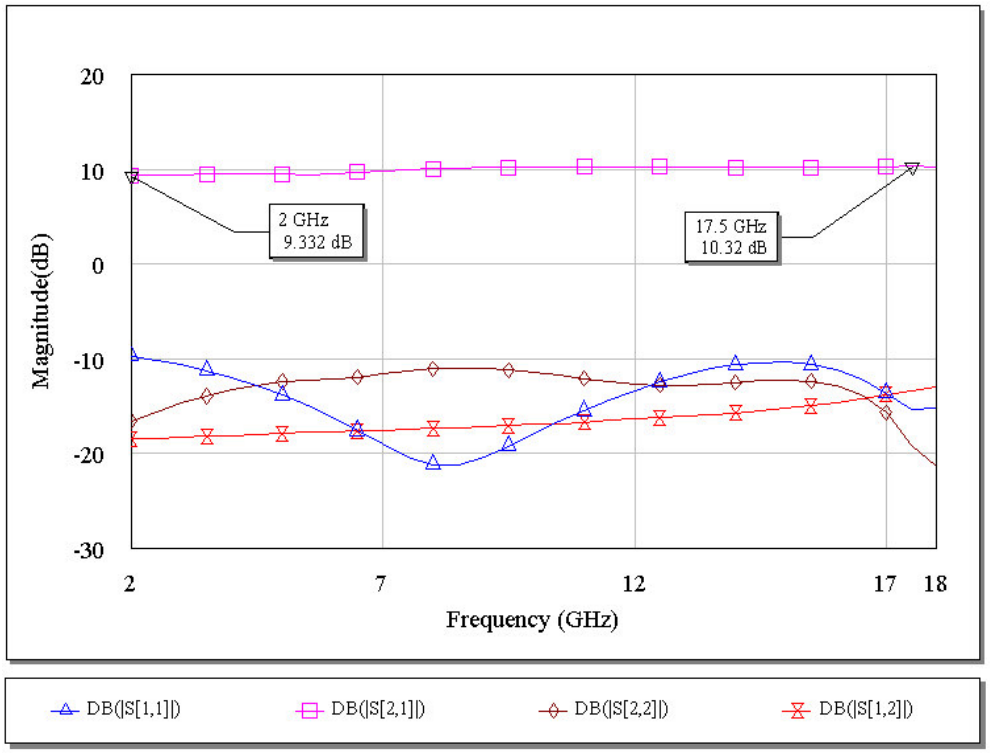


Figure 5.27: Small-signal gain response of stage one

Figure 5.28 shows the input 1 dB compression response of the first stage, with a maximum of 1.3 dBm. The maximum drive level that the first stage will be exposed to is 5 dBm, which is the high end of the BLA's input dynamic range. Intuitively it can already be reasoned that this amplifier will have reasonable harmonic suppression since it is only driven about 4 dB into saturation.

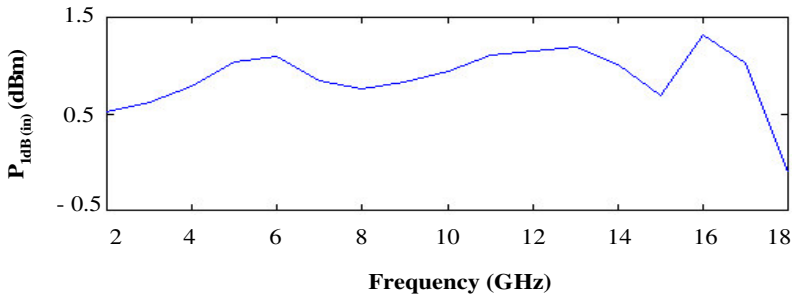


Figure 5.28: Input 1 dB compression response for stage one

Figure 5.29 aims to show the harmonic suppression for the input amplifier for the 5 dBm drive level. The result, which shows a minimum harmonic suppression of 12.4 dBc, confirms that reasonable harmonic suppression will be offered by this amplifier when driven at the intended maximum input level of 5 dBm.

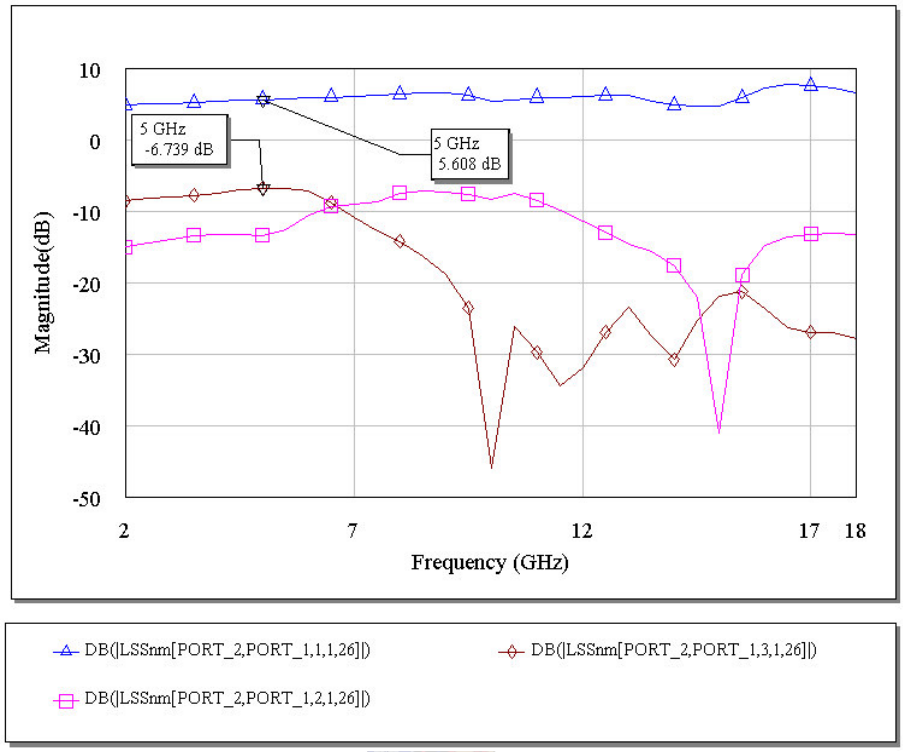


Figure 5.29: Harmonic suppression of stage one for a 5 dBm drive level

In terms of the output 1 dB compression response, an estimate of the drive level to be presented to the second stage after attenuation, can again be formed by evaluating the 1 dB compression response of this amplifier as seen in Figure 5.30. This result shows a maximum output 1 dB compression of approximately 10.5 dBm.

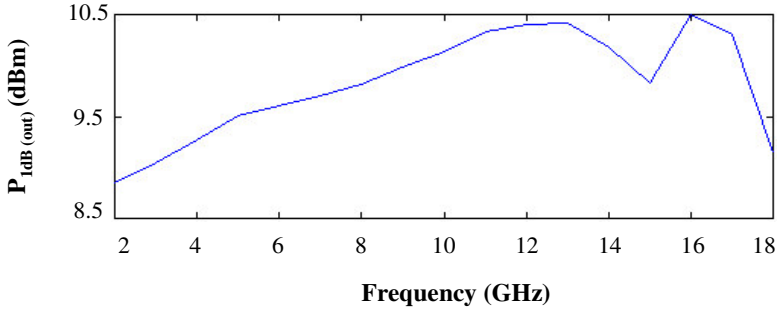


Figure 5.30: Output 1 dB compression response for stage one

With the evaluation of the different RF amplifiers proposed for use in the BLA complete, the next step would be an evaluation of the design configuration as a whole. This evaluation is done in the following section to determine the achieved limiting amplifier operation as well as to establish the degree of interaction between the different amplifiers within the proposed RF chain.

5.5 EVALUATION OF THE DESIGNED LIMITING AMPLIFIER AS A WHOLE

Figure 5.31 shows the block diagram of the designed limiting amplifier together with the specifications for each amplifier stage. The specifications show the gain at the onset of gain compression ($G_{compression}$) as well as the input and output 1 dB compression points ($P_{1dB\ (in)}$ and $P_{1dB\ (out)}$). It should be noted that the shown values are average values as obtained from the previously discussed evaluation of the different amplifier stages. The attenuators in the shown configuration are 3 dB T-attenuators such as those discussed earlier.

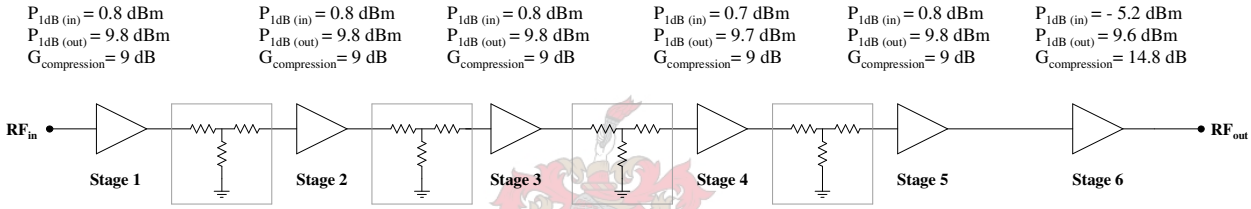


Figure 5.31: Block diagram of the designed limiting amplifier

The block diagram is useful in evaluating the functionality of the initial proposed design configuration. Firstly, one may determine the expected small-signal gain from the shown RF chain. Adding 1 dB to each of the amplifier's gain at 1 dB compression, and taking into account the effect of the four attenuators, results in a small-signal gain of about 53.8 dB. This is close to the small-signal gain of 50 dB that was calculated earlier. Calculations based on both simulated and actual measured results, resulted in the difference between the two gain values. The simulated result, which predicts a small-signal gain of 53.8 dB, however, did not take into account any extra losses in the RF chain. The inclusion of these extra losses will result in a small-signal gain that is closer to the 50 dB that was predicted from Figure 5.3.

The predicted small-signal gain is significant in the sense that it offers a useful starting point for eventual tuning and evaluation of the designed limiting amplifier. Figure 5.32 shows the simulated small-signal gain response of the designed limiting amplifier. It is seen that the gain is just below 54 dB, centred at about 51 dB with a gain ripple of ± 2.9 dB. The shown small-signal response will typically be used only as reference for actual measurements, while the real concern will be the gain ripple variation over the relevant input dynamic range. As one starts to operate the limiting amplifier within its specified input dynamic range, the gain ripple is expected to improve due to the onset of gain saturation in the different amplifiers. Both simulated and measured results will be used to verify this statement. The input return loss shown in Figure 5.32, although not very good, was within the set specification and was therefore of little concern.

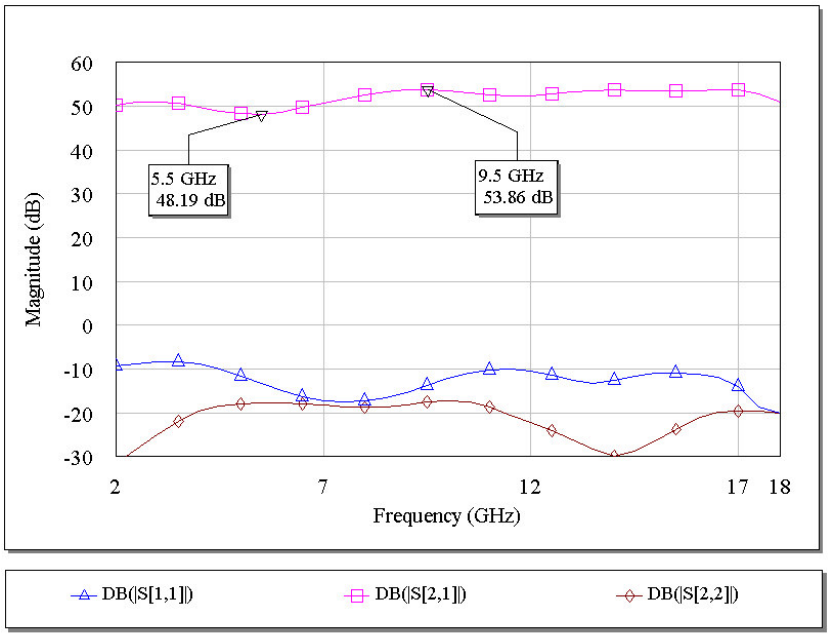


Figure 5.32: Small-signal gain response of the designed limiting amplifier

To estimate the low end of the input dynamic range one may again use the block diagram of the limiting amplifier as shown in Figure 5.31 for calculations. The requirement at the low end of the limiting amplifier's input dynamic range is that the last amplifier in the RF chain must at least be driven into compression. For calculations, the average small-signal gain for the first five amplifiers will be used while the gain at 1 dB gain compression will be used for the last stage. Again an attenuation value of 3 dB is assumed for each attenuator. The result of these calculations is shown in Figure 5.33.

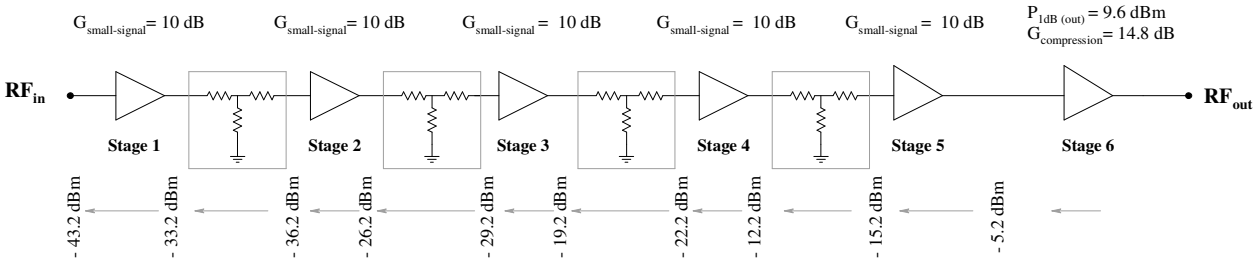


Figure 5.33: Calculating the low end of the limiting amplifier's input dynamic range

Figure 5.33 shows the expected power at each stage within the limiting amplifier RF chain. From these calculations one can determine an approximate limit of - 43.2 dBm at the low end of the limiting amplifier's input dynamic range. With a - 43.2 dBm drive level, the last stage will just be driven into compression. To compensate for design variances and temperature variation, the low end of the input dynamic range should be extended to at least - 40 dBm to ensure that the last

stage will be driven a few dB's into saturation. Figure 5.34 shows the simulated output power response for the designed limiting amplifier for an input drive level ranging from - 40 dBm to 5 dBm. Important to recall, is that this power refers to saturated rather than compressed output power. The observed output power window is approximately 2.6 dB, centred around 11.2 dBm. This implies a minimum and maximum saturated output power of approximately 9.9 dBm and 12.5 dBm respectively.

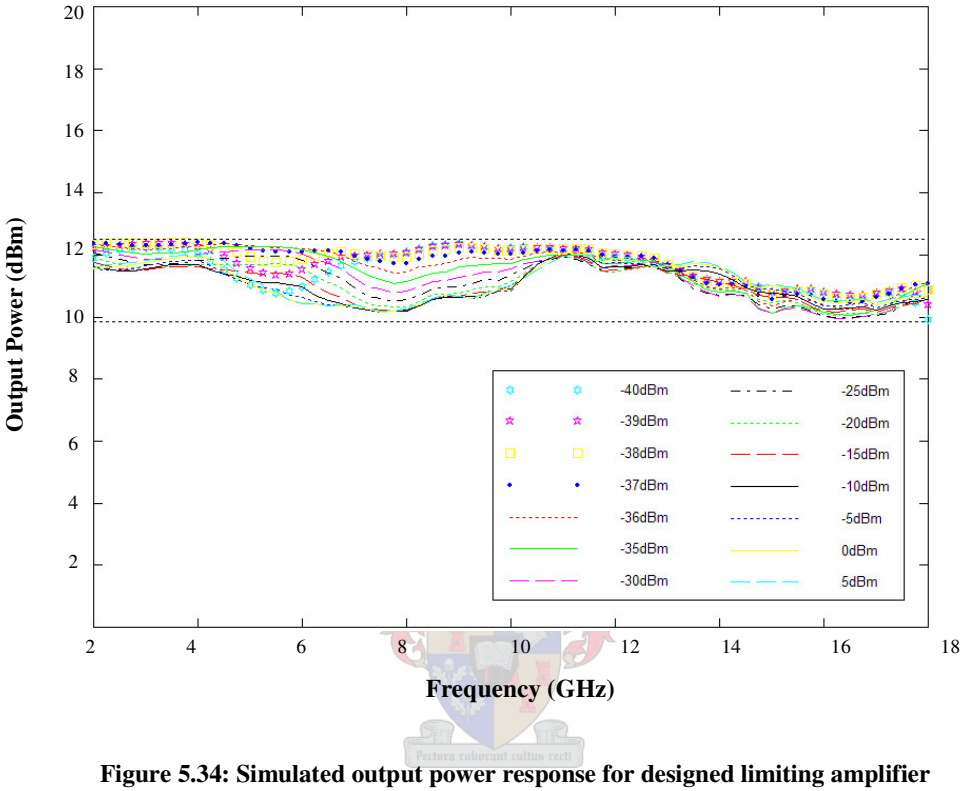


Figure 5.34: Simulated output power response for designed limiting amplifier

Increasing the input dynamic range from - 44 dBm to 5 dBm resulted in an increased output power window of approximately 5 dB, centred around 10 dBm. This result is seen in Figure 5.35. Depending on the desired input dynamic range, one may thus use the shown results for predicting the associated output power window. The problem with the shown line graphs, however, is that they do not accurately point out possible problem areas when considering the limiting amplifier's whole input dynamic range and operating frequency bandwidth. An alternative manner of representation therefore needed consideration.

Such an improved representation of the limiting amplifier's operation required a finer sweep over frequency and input drive level, while the monitored result had to be shown in a simple but insightful manner.

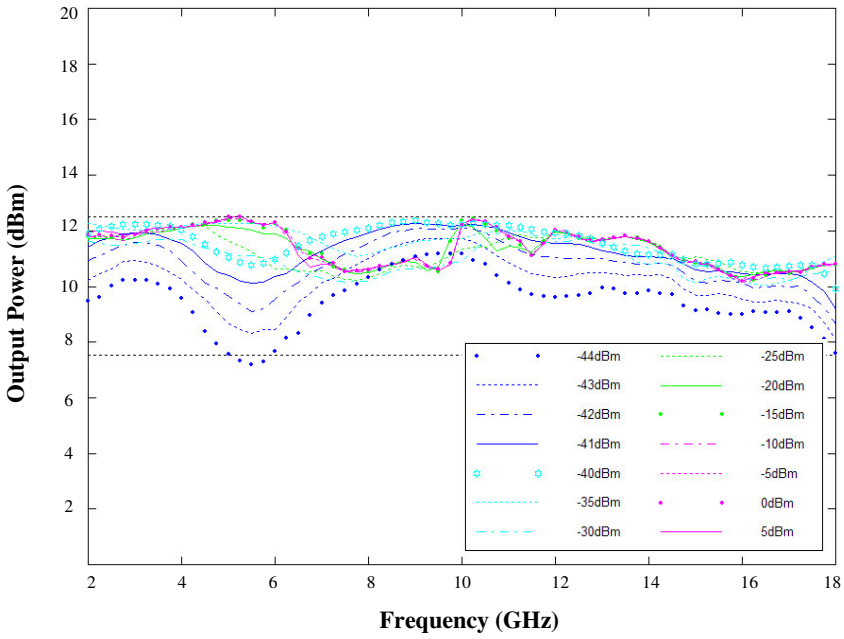


Figure 5.35: Estimating the desired input dynamic range

The shown power window plots are sufficient for establishing an intuitive feel for the expected output power response of the designed limiting amplifier. A better representation of the previously shown results, however, is given in Figure 5.36. The shown colour grid plot shows the associated output power response of the designed limiting amplifier as a function of both input drive level and frequency. The colour scale to the right of the colour grid indicates the *intensity* level of the associated output power.

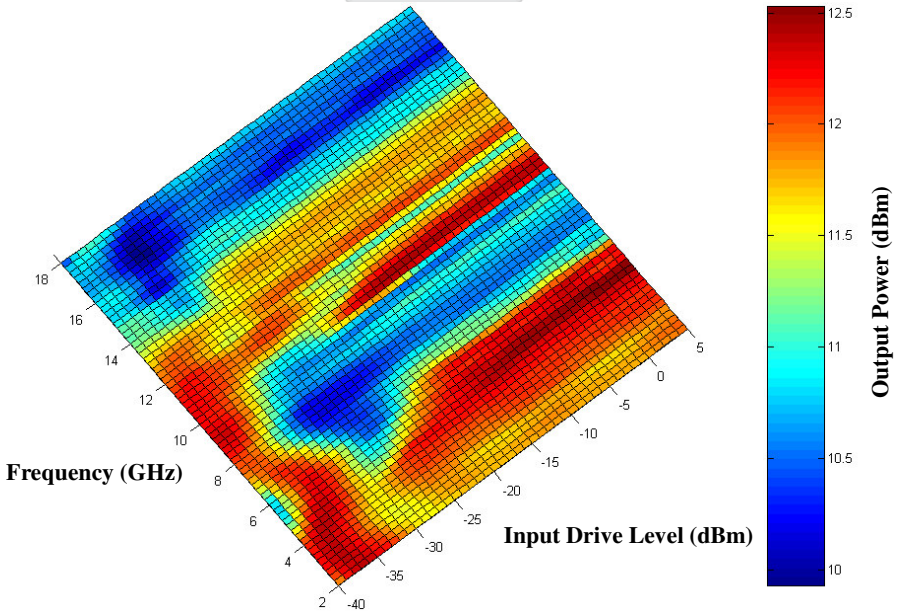


Figure 5.36: Colour grid of the limiting amplifier's associated output power response

The colour grid plot offers a clear first impression of the limiting amplifier's output power response. Not only does it show the result of a finer frequency and input drive level sweep, but it also clearly shows where deviations (blue areas) from the maximum output power occur. This type of graph thus provides a useful method of representing and characterizing a limiting amplifier's response.

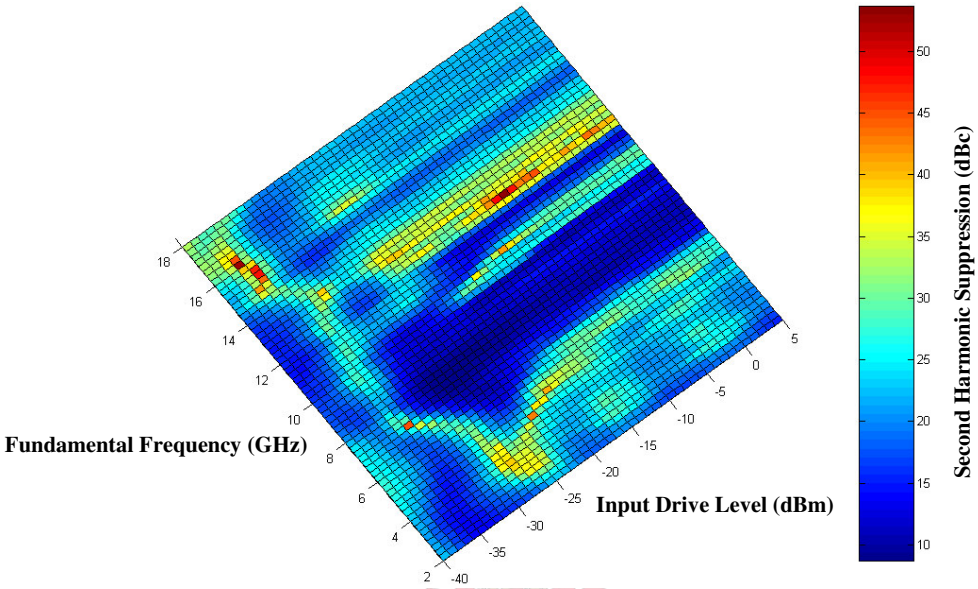


Figure 5.37: Colour grid of the associated second harmonic suppression

In a similar fashion one may plot the harmonic suppression achieved with the limiting amplifier. Figure 5.37 shows a colour grid that indicates to what extent second harmonic suppression is achieved. Again the result of a finer frequency and input drive level sweep is seen, with undesired levels of second harmonic suppression indicated by the dark blue areas. This graph is concerned mainly with the fundamental frequency range from 2-9 GHz, since the associated harmonics will fall within the 2-18 GHz frequency band. For sake of illustration, the complete 2-18 GHz fundamental frequency range is shown.

Typically, the minimum level of second harmonic suppression that was achieved with simulations was 9.2 dBc, which is better than the minimum requirement of 9 dBc. Simulations suggest that the worst-case second harmonic suppression will occur for input drive levels ranging from - 30 to - 25 dBm, at a fundamental frequency of about 8 GHz. A potential problem area has thus been highlighted and will be focused upon during actual measurements.

The similarity of the patterns produced on the previously shown colour grid plots can be indicative of a potential characteristic of a limiting amplifier. Figure 5.38 shows the *mapping* that occurs over the frequency bandwidth and input dynamic range in question. Over the regions where the second harmonic suppression is poor, one can see a resulting decrease in the limiting amplifier's output power. This indicates a power transfer that *bleeds* power from the fundamental only to be added to the second harmonic, or other harmonics for that matter. One may therefore also intuitively reason that the second harmonic suppression will be higher over the regions where the limiting amplifier's output power is a maximum. This knowledge allows one to predict the occurrence of undesired harmonic levels. When a significant drop in

the limiting amplifier's output power response is thus observed, concern as to the actual harmonic levels may be raised. Correcting such a problem after actual manufacturing will offer a big challenge. Rather than trying corrective tuning, one should rather address these problems during the design phase.

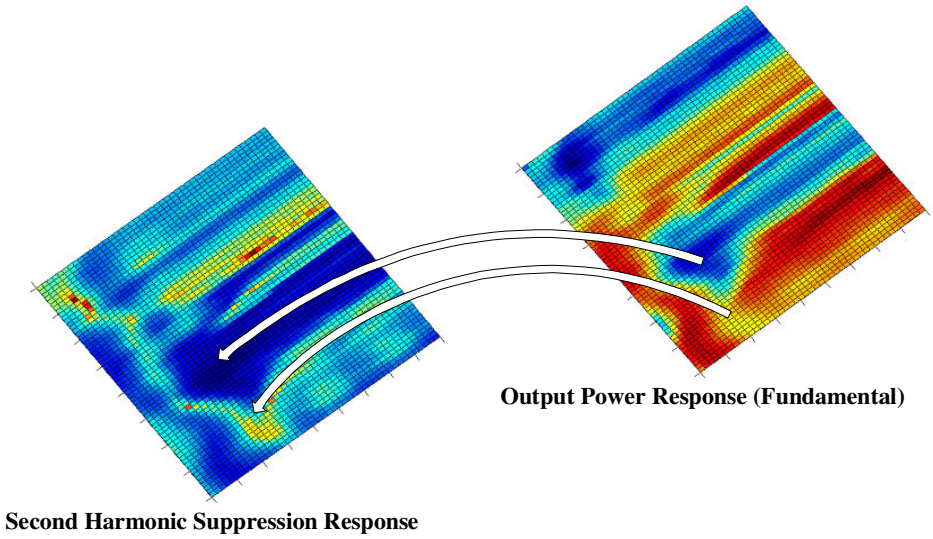


Figure 5.38: Colour grid mapping showing the power transfer from the fundamental to second harmonic

In the same way as was done for the second harmonic suppression, one may also evaluate the third harmonic suppression. The result of this evaluation is shown in Figure 5.39. This plot is concerned mainly with the fundamental frequency range from 2-6 GHz, since the associated harmonics will fall within the 2-18 GHz frequency band. For sake of illustration, the complete 2-18 GHz fundamental frequency range is again shown.

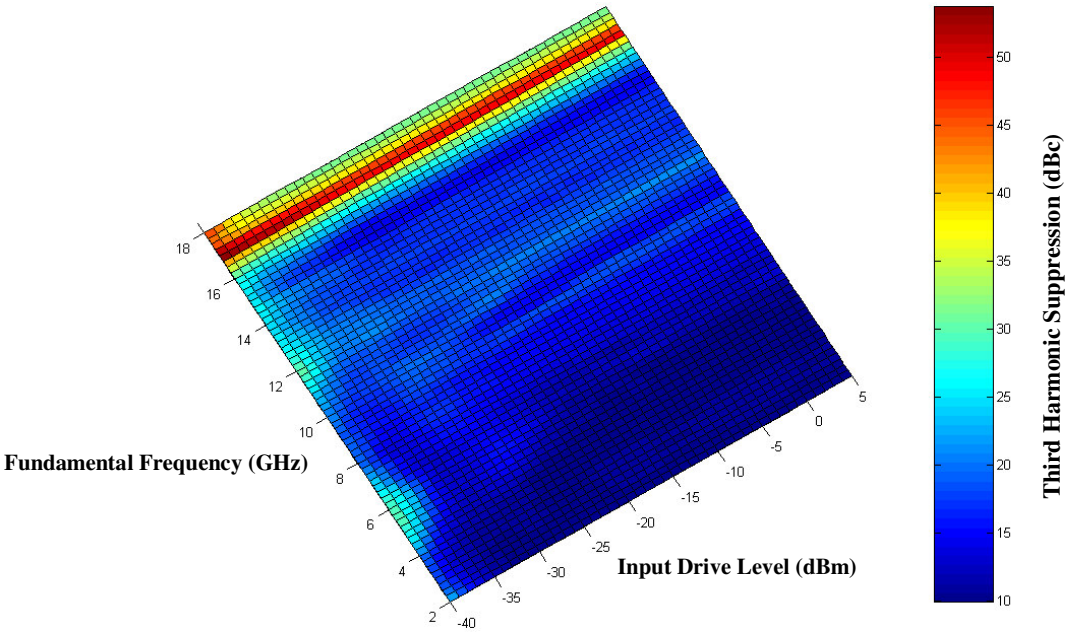


Figure 5.39: Colour grid of the associated third harmonic suppression

Unlike the second harmonic suppression plot that showed some variation over the frequency and input dynamic range in question, the third harmonic suppression response indicates a degree of saturation with the minimum suppression being better than 10 dBc and not varying much from this value.

The foregoing section offered an evaluation of the designed limiting amplifier and showed the extent to which a saturated output power window, and harmonic suppression exceeding at least 9 dBc, was achieved over the - 40 to 5 dBm input dynamic range. The next consideration is the small-signal suppression as expected from this design.

5.6 SMALL-SIGNAL SUPPRESSION

With small-signal suppression being an inherent property of the limiting amplifier, it was not part of the initial design considerations. Rather, focus was placed on the main design considerations of the limiting amplifier, while the small-signal suppression response was only evaluated after completion of the final limiting amplifier design. To be noted is that the *small-signal* suppression referred to is the relative suppression of a signal having smaller amplitude than that of another signal, while these two signals form part of some arbitrary two-tone excitation. The signal with smaller amplitude will be regarded as an undesired interference signal, while the signal with the larger amplitude will be regarded as desired. This distinction is apparent from the discussion on the IFM receiver which is a processor of the signal with largest amplitude.

5.6.1 SMALL-SIGNAL SUPPRESSION INTUITIVELY EXPLAINED

In characterizing the designed limiting amplifier's *capturing* effect and thus its small-signal suppression response, one should ideally evaluate it over its complete frequency range and input dynamic range. Not only should one do the evaluation for a range of frequency separations between the input signals (tone separations) but also for a range of input drive level ratios (signal separations). For obvious reasons, this was not attempted. Rather, it was decided to do an evaluation in such a fashion, as to establish an intuitive feel for small-signal suppression as a function of both frequency and power level separation between two input tones. To start off with, the small-signal suppression response of the first amplifier stage was evaluated using the two-tone setup as shown in Figure 5.40. Some arbitrary two-tone configuration was evaluated with a desired signal (maximum amplitude signal) at 4 GHz and the undesired signal (minimum amplitude signal) at 4.9 GHz.

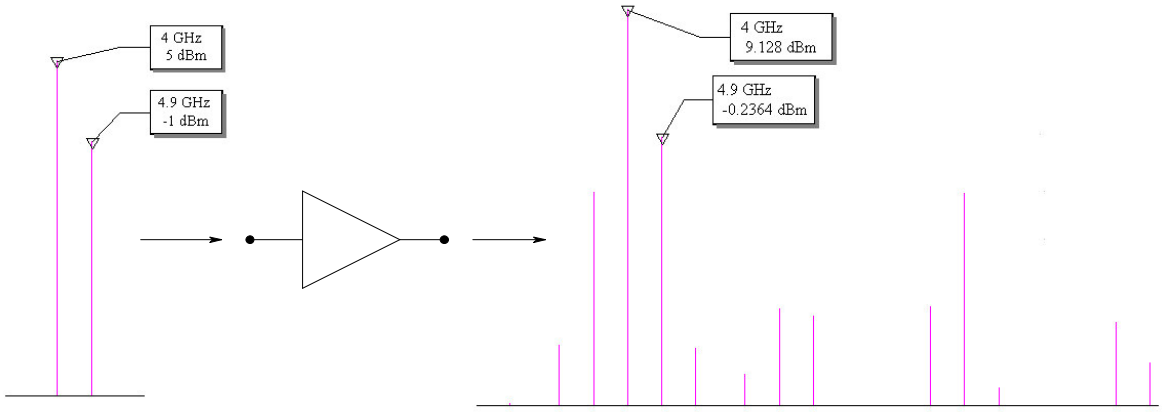


Figure 5.40: Two-tone analysis to evaluate small-signal suppression

In Figure 5.40 one can see an input signal separation of 6 dB, with the desired signal's power level at 5 dBm. At the output of the amplifier one can see the original input tones as well as newly generated intermodulation products. Of concern in the generated output spectrum is the signal separation between the two input tones, rather than the levels of the intermodulation products which are generally suppressed well below the desired signal's level. The shown output signal separation is approximately 9.36 dB (9.128 + 0.2364) which shows an increase of 3.36 dB (9.36 - 6) in the original signal separation. The achieved small-signal suppression is therefore approximated as 3.36 dB.

The obtained result already shows to what extent small-signal suppression may be a reality in an RF amplifier. What should, however, be noted is that small-signal suppression will be dependent on the actual input signal levels and their respective ratios. To evaluate this aspect further, the output signal separation was evaluated as a function of the desired signal's input power level (- 5, 0 and 5 dBm) for different input signal separations (3, 6, 9 12 and 15 dB). The tone separation (f_Δ) was held fixed at 900 MHz. Figure 5.41 shows the varied input spectra presented to the RF amplifier.

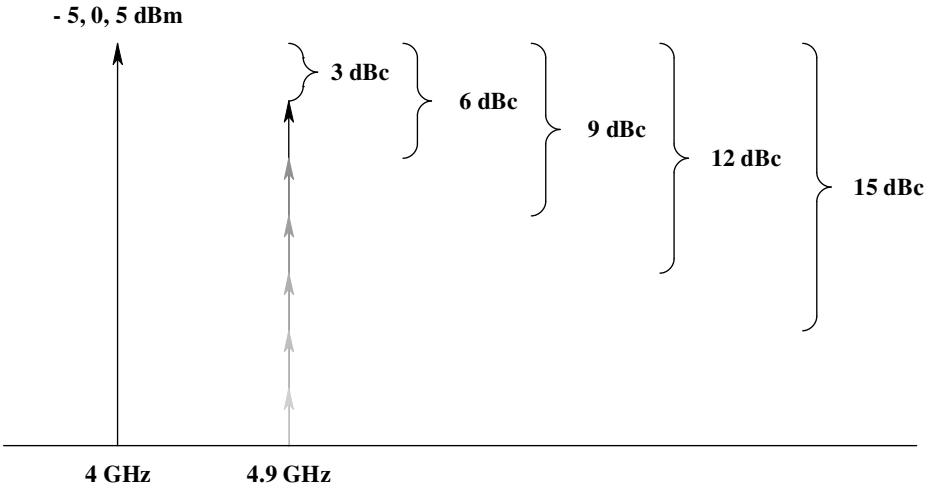


Figure 5.41: Varied input spectra to be presented to the RF amplifier for small-signal suppression evaluation

The result of this experiment is seen in Figure 5.42. The point shown as **A** corresponds to the discussion of Figure 5.40. Thus, with a desired input signal level of 5 dBm and with the undesired signal suppressed 6 dB below this level, the resulting output signal separation is 9.36 dB. The resulting small-signal suppression being the expected 3.36 dB

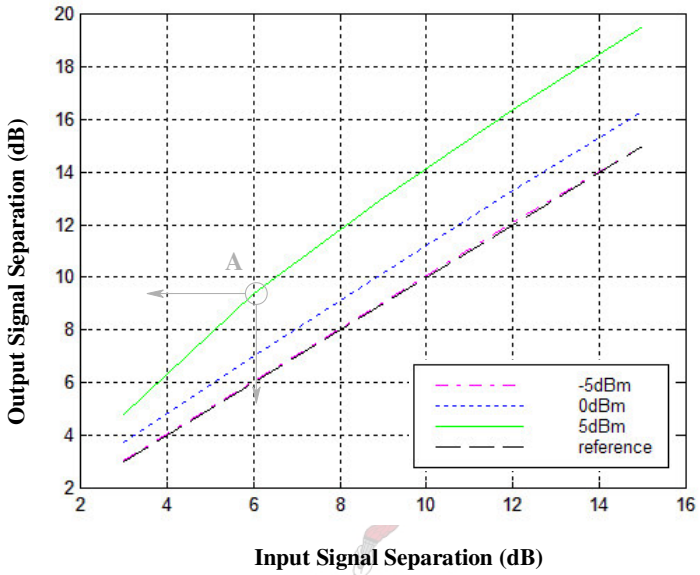


Figure 5.42: Output signal separation (f_Δ = 900 MHz)

From Figure 5.42 one may start to understand the essence of small-signal suppression as observed in an RF amplifier. The desired signal's power levels (- 5, 0 and 5 dBm) were intentionally chosen to cover the amplifier's linear operating region, its nonlinear operating region and the transition between the two regions.

With the power level of the desired signal at - 5 dBm, which implies operation within the amplifier's linear region, one can see that there is no difference between the input and output signal separation. This trace is seen to lie right on the shown reference line. This would mean that both input tones are amplified by the same factor. Intuitively, this can be explained by revisiting the general transfer characteristic of the nonlinear amplifier but with higher order terms (and the DC term) ignored, thus:

$$V_{out} = a_1 V_{in} \tag{5.1}$$

With $V_{in} = (A\sin\omega_1 t + B\sin\omega_2 t)$, the resulting output response will be $V_{out} = a_1 A\sin\omega_1 t + a_1 B\sin\omega_2 t$ which shows that the input amplitude ratio A/B equals the output amplitude ratio, $a_1 A/a_1 B$.

With the power level of the desired signal at 0 dBm, which implies operation near the amplifier's compression point, one can see that the output signal separation (deviation from the reference line) has increased. The shown reference line indicates where linear operation occurs and where there is no difference in input versus output signal separation. From Figure 5.42 it is observed to what extent output signal separation is dependent on input signal separation. In general, while being dependent on the level of the desired signal, it is seen that the larger the input signal separation, the larger the

corresponding output signal separation will be. This statement is then also confirmed (in Figure 5.42) for the case where the power level of the desired signal is 5 dBm. Intuitively, this can be explained by revisiting the general transfer characteristic of the nonlinear amplifier for a two-tone excitation, with $V_{in} = (A\sin\omega_1 t + B\sin\omega_2 t)$. The resulting output equation (from equation 4.6), showing only frequency components at ω_1 and ω_2 is given by equation (5.2).

$$V_{out} = a_1 A\sin\omega_1 t + a_3 A^3(0.75\sin\omega_1 t) + a_3 1.5AB^2\sin\omega_1 t + a_1 B\sin\omega_2 t + a_3 B^3(0.75\sin\omega_2 t) + a_3 1.5A^2 B\sin\omega_2 t + \ldots \quad (5.2)$$

Again an input amplitude ratio of A/B is present, but the output amplitude ratio is now:

$$\frac{a_1 A + 0.75a_3(A^3 + 2AB^2)}{a_1 B + 0.75a_3(B^3 + 2BA^2)} \quad (5.3)$$

Input Ratio: *A/B*	**Input Ratio (dB)**	**Output Ratio**
1.41	3	$\frac{a_1 A + 0.75a_3(2A^3)}{0.71a_1 A + 0.75a_3(1.78A^3)}$
2	6	$\frac{a_1 A + 0.75a_3(1.5A^3)}{0.5a_1 A + 0.75a_3(1.125A^3)}$
2.82	9	$\frac{a_1 A + 0.75a_3(1.25A^3)}{0.35a_1 A + 0.75a_3(0.75A^3)}$
4	12	$\frac{a_1 A + 0.75a_3(1.125A^3)}{0.25a_1 A + 0.75a_3(0.52A^3)}$
5.62	15	$\frac{a_1 A + 0.75a_3(1.065A^3)}{0.18a_1 A + 0.75a_3(0.37A^3)}$

Table 5.2: Output ratio calculation for two-tone excitation

From the discussion on gain saturation one knows that the fundamental signal's amplitude on the nonlinear device output will decrease as the input amplitude increases. With, a two-tone excitation present, one also expects gain saturation and thus suppression of the fundamental output tones. To better quantify this aspect, calculations were done to show how the output amplitude ratio (equation 5.3) will vary in accordance with the input signal amplitude ratio. The result of these calculations is summarized in Table 5.2. Using the given input ratio, an expression for B is obtained which is then substituted into equation (5.3) to give the expression for the output ratio.

From the calculated output ratios one can make an important deduction, especially when looking at the bracketed terms of the numerator and denominator. These terms influence the eventual output signal ratio in that they determine the amplitude portion that gets subtracted (a_3 having a negative value) from the fundamental tone amplitudes. From the summarized result

it is seen that the ratio between these *subtraction portions* increase as the input signal ratio increases. This would then explain the larger output signal separation for larger input signal separation as was shown in Figure 5.42.

With the small-signal suppression characteristics of the amplifier established at a fixed tone separation as a function of input signal separation, the next step would be to evaluate small-signal suppression at fixed input signal separations as a function of tone separation. The output signal separation was therefore evaluated as a function of the desired signal's input power level (- 5, 0 and 5 dBm) for different input signal separations (3, 6, 9, 12 and 15 dB) and for tone separations of 0.1, 0.9, 3.9, 7.9 and 11.9 GHz respectively. The frequency of the desired signal was held fixed at 4 GHz

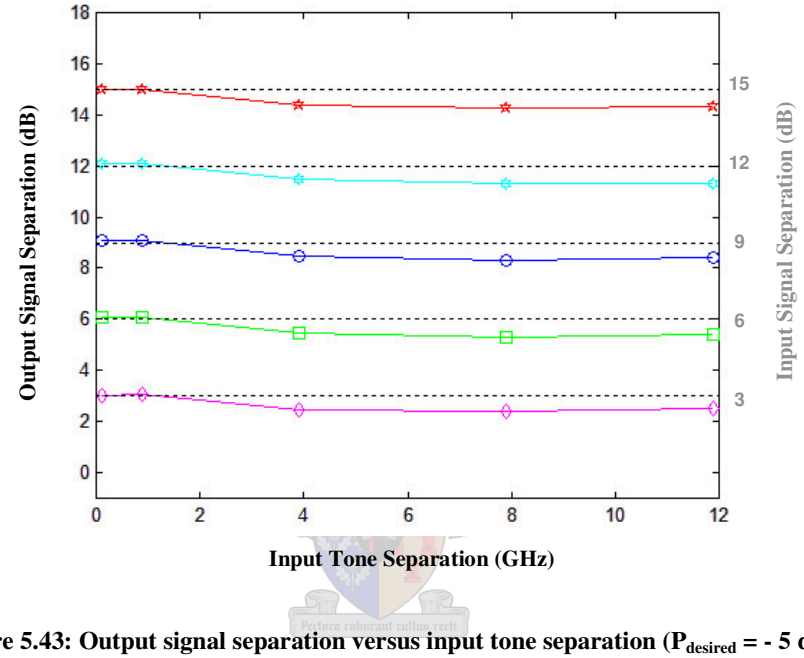


Figure 5.43: Output signal separation versus input tone separation ($P_{desired}$ = - 5 dBm)

Figure 5.43 shows the output signal separation (coloured traces) as a function of input tone separation with the desired signal's input power ($P_{desired}$) equal to - 5 dBm. Again, the signal separation is plotted against the corresponding (dotted) reference lines to show deviation from the initial input signal separation. Evident from the shown response is that there is an overall deterioration in output signal separation as the input tone separation increases. It is also evident that for the drive level of the desired signal not exceeding at least the amplifier's compression point, the output signal separation is smaller than the input signal separation. This is evident from the shown coloured traces lying underneath the dotted reference lines. In fact, small-signal suppression is not achieved at all.

Figure 5.44 shows a different scenario of output signal separation versus input tone separation for a 0 dBm drive level. The same general deterioration in output signal separation is observed as the input tone separation increases. Apparent, however, is that the output signal separation is larger than the input signal separation for the case where $P_{desired}$ = 0 dBm, as compared to the case where $P_{desired}$ = - 5 dBm. This result stresses the importance of the desired signal's power level as compared to the weaker signal's power level, in order to achieve suppression of the weaker signal. The same aspect is also evident from the result seen in Figure 5.45 where $P_{desired}$ was set to 5 dBm. Here, the output signal separation is even more pronounced, indicating increased small-signal suppression.

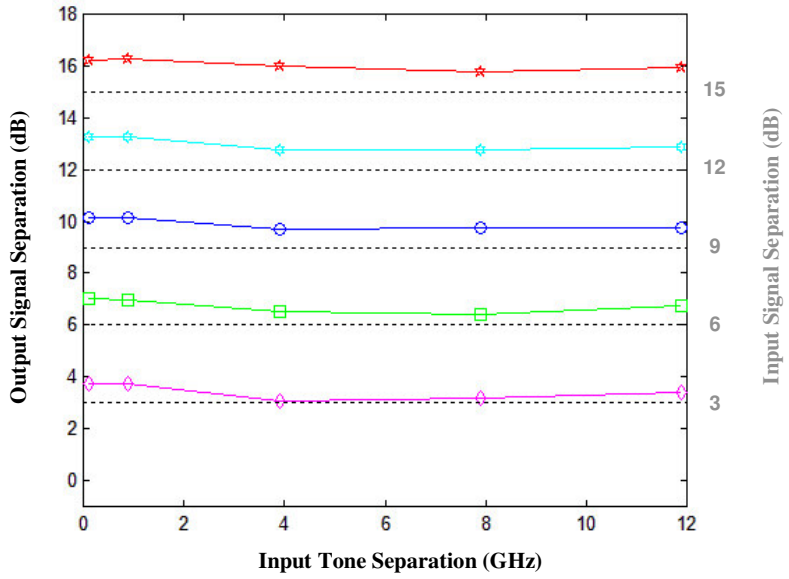


Figure 5.44: Output signal separation versus input tone separation ($P_{desired}$ = 0 dBm)

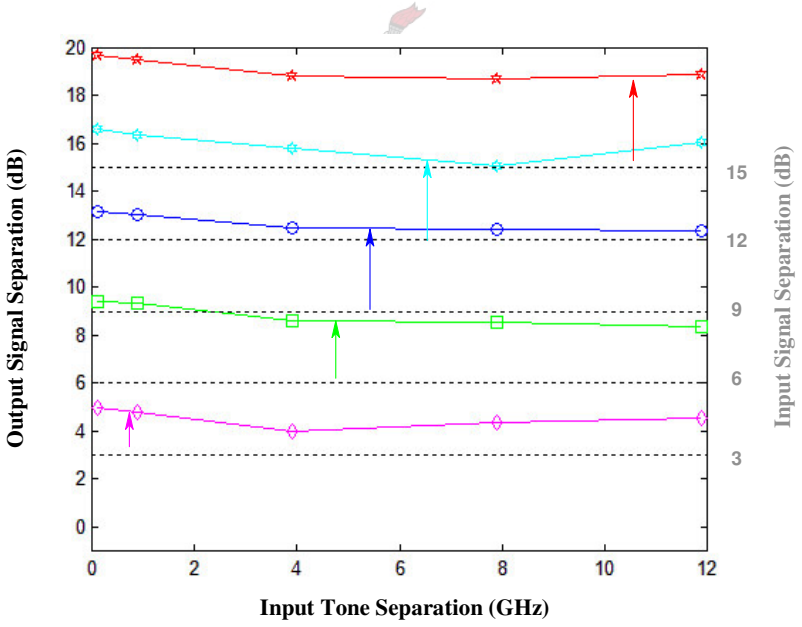


Figure 5.45: Output signal separation versus input tone separation ($P_{desired}$ = 5 dBm)

In conclusion, the results obtained in this section offers valuable insight as to small-signal suppression as observed in the RF amplifier and is well predicted by theory [31]. It was shown that the output signal separation is a function of not only the input signals' separation in frequency, but also the input signal separation and the degree of gain compression (or eventual gain saturation) introduced. Insight is provided as to the difficulty in achieving ideal suppression characteristics for the broadband RF amplifier, especially for signals with comparable amplitudes and large frequency separations.

The investigation was concerned with some arbitrary frequencies within the RF amplifier's operating frequency bandwidth while one should ideally take into account all the deviations from (ideally) constant gain that occur over frequency and the compression characteristics of the amplifier that also varies over frequency. The suppression characteristics of the RF amplifier will vary over frequency and will, together with the other amplifiers within the limiting amplifier RF chain, determine the composite suppression characteristics of the limiting amplifier.

The section to follow investigates the composite small-signal suppression as observed over a portion of the designed limiting amplifier's input dynamic range and gives an indication of the physical expected device performance.

5.6.2 SMALL-SIGNAL SUPPRESSION IN THE DESIGNED LIMITING AMPLIFIER

With the small-signal suppression characteristics as observed in an RF amplifier explained, one may proceed to the composite small-signal suppression as observed in the designed limiting amplifier. This experiment is concerned with the levels of the fundamental tones rather than that of the intermodulation products. The experiment, seemingly simple, offers valuable insight as to the mechanism of small-signal suppression that occurs within the limiting amplifier RF chain and is used solely for that purpose. Again, it should be noted that the measured results were observed at coupled ports within the RF chain and will give only an estimate of the actual expected signal levels.

The evaluation is done by again looking only at a portion of the BLA's spectral response with some arbitrary two-excitation present as seen in Figure 5.46. This figure depicts the observed signal *capturing* or small-signal suppression.

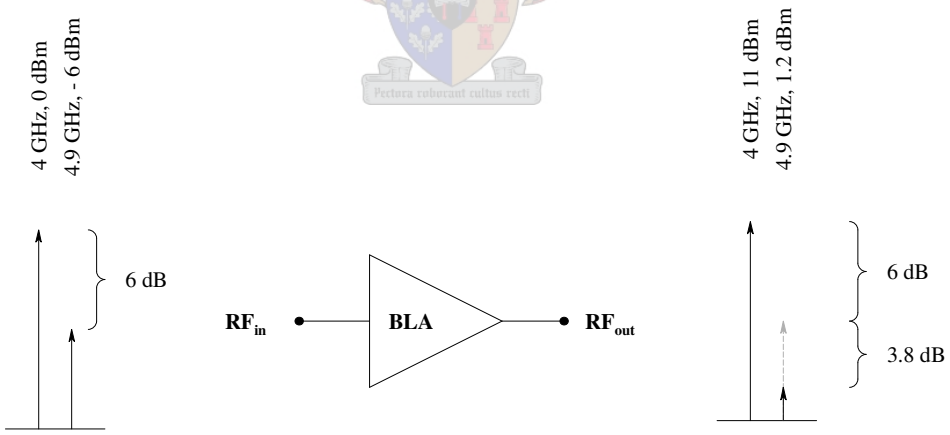


Figure 5.46: Small-signal suppression as seen in the BLA

Figure 5.47 shows how the undesired signal at 4.9 GHz is further suppressed below the desired signal as it progresses through the shown RF chain. It is seen that the 6 dB signal separation on the input, is increased to a 9.8 dB signal separation on the output. This implies small-signal suppression of 3.8 dB.

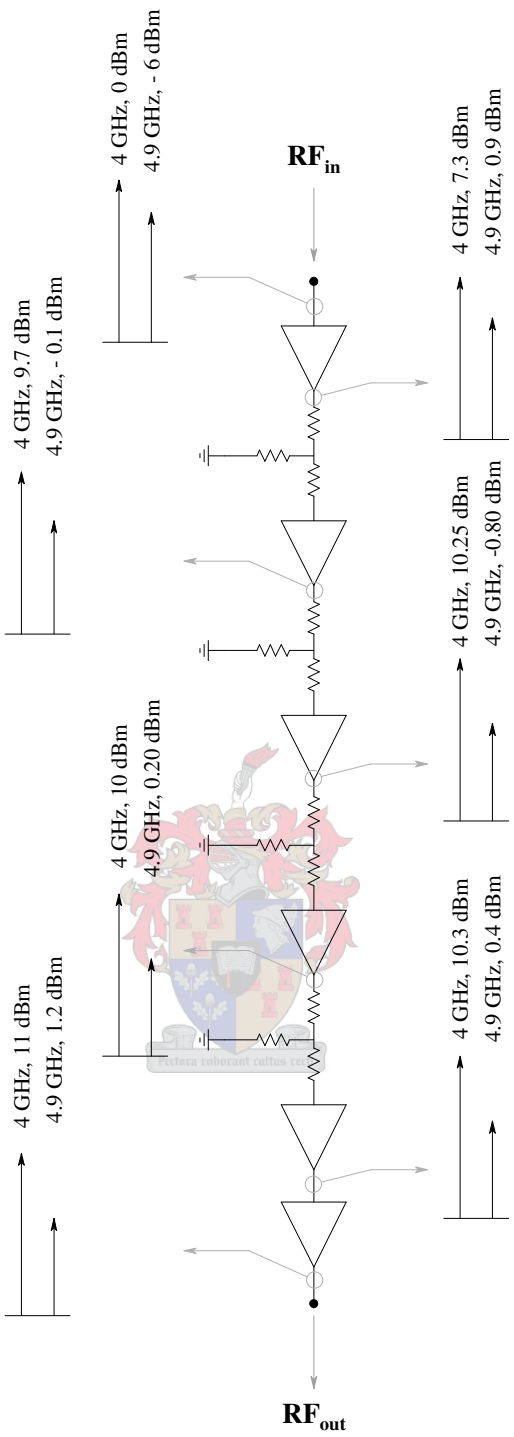


Figure 5.47: Portion of the BLA spectral analysis (two-tone excitation)

From earlier discussions, it is known that small-signal suppression is dependent on the drive level of the two different tones as well as the relevant tone separation. While the previous discussed experiment offers insight as to the mechanism of small-signal suppression that occurs within the limiting amplifier itself, a more refined analysis is required. Similar experiments as that discussed earlier were done at spot frequencies and for different signal level separations, to confirm the mechanism of small-signal suppression as observed in the designed limiting amplifier. It was, however, opted to do the

more refined analysis with physical measurements rather than simulations. These measurements are given in the following chapter which discusses the physical evaluation of the designed limiting amplifier.

5.7 CONCLUSION

The design of a *backbone* limiting amplifier (BLA) as part of a proposed modular design approach was discussed in this chapter. A design hypothesis as based on the existing *baseline* limiting amplifier was formulated from where the actual design was implemented for functional evaluation. The different amplifier stages comprising the proposed BLA design were discussed and analyzed while better insight as to each stage's functional role was given. A complete evaluation of the designed BLA was then done to assess the formulated design hypothesis. The evaluation of the design consisted of thorough single-tone tests and harmonic suppression measurements, while two-tone tests offered a better intuitive feel as to the expected small-signal suppression characteristics of the design. While simulated results gave a reasonable idea of what was practically to be expected, the true evaluation would be from physical measurements. The chapter to follow focuses on the practical evaluation of the designed limiting amplifier (BLA) after physical implementation.

CHAPTER 6

PHYSICAL EVALUATION OF THE DESIGNED LIMITING AMPLIFIER

6.1 INTRODUCTION

The aim of this chapter is to report on the response of the designed *backbone* limiting amplifier, or BLA, as physically measured. Physical measurements are used not only to validate the formulated design hypothesis but also to confirm that simulations give a good prediction of the actual device response. Measurements also highlight some of the flaws associated with the limiting amplifier design, while providing significant insight as to ways of improving on this design.

To start with, the actual design implementation is discussed with specific reference to each of the amplifier stages comprising the design. This is done to highlight some important considerations for physical implementation of the design. After physical implementation, a range of measurements were carried out to evaluate the physical device performance. These measurements included a comprehensive single-tone test, performed over temperature, for determining the achieved output power window and the resulting harmonic suppression response. Focus was also placed on evaluating the actual gain response of the designed limiting amplifier as a function of input drive level. These measurements are useful in providing further insight as to the operating mechanism of the limiting amplifier.

The last concern for evaluation was the small-signal suppression achievable with the designed limiting amplifier. Due to the possible extent of such an evaluation, focus was placed on evaluating the BLA's small-signal suppression response over a limited portion of the device's input dynamic range and operating frequency bandwidth. Irrespective of the limited evaluation, the results offered significant insight as to the expected behaviour from the designed limiting amplifier.

6.2 DESIGN IMPLEMENTATION

A design, no matter how good it may be, means little if it cannot be physically implemented. The implementation of the BLA design is discussed hereafter, since it forms an important part of the technical design as well. A realistic layout may require alterations to an existing design and it should be evaluated to see whether this influences the initial designed response. Therefore, once a layout is complete, it is best to go back to the initial simulation and insert related elements in the fabrication process to the necessary extent for evaluation.

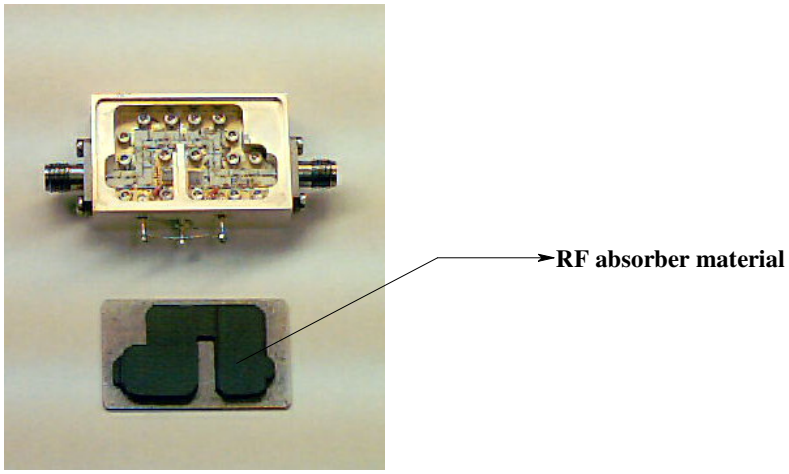


Figure 6.1: Physical BLA design

The physical BLA as shown in Figure 6.1 is discussed hereafter in terms of the implementation of each of the stages comprising this design. The Alumina substrates with etched microstrip elements were mounted on Kovar carrier plates and screwed down on the floor of a silver plated Aluminum housing. This specific combination of substrate and carrier plate is used since the two materials have highly compatible thermal expansion coefficients. Had this not been the case, the substrate would crack when the device is operated over temperature. Another requirement is that the carrier thickness should be at least twice the substrate thickness to prevent warping [29]. SMA connectors with their corresponding feed pins were used on this housing.

The shown *omega* type layout allows for a reasonable length reduction of the actual housing and offers an isolation wall not present in an *open plan* design. To improve the isolation between the first three amplifier stages and the last three amplifier stages, RF absorber material was fixed to the lid of the housing, as can be seen in Figure 6.1. Without the RF absorber material, the design will not function properly and is therefore absolutely essential. The shown housing encloses an amplifier with gain in excess of 60 dB and the absorber material helps absorb radiated power that will otherwise lead to undesired cross coupling between the different amplifiers.

Figure 6.2 shows the physical implementation of the first stage of the designed BLA. Right on the input of this stage, a DC blocking capacitor is used for protection of measurement instruments. Even though the blocking capacitor is present, it should always be confirmed that no DC is measured on the device input. It could happen that the conductive epoxy that is used to mount the relevant capacitor, shorts out the capacitor terminals and so feeds any DC that may be present on the amplifier's input, to the measurement device input. Furthermore, one can see the voltage regulator and the passive bias configuration that was used and to what extent it was routed within the design. The bias configuration includes the relevant drain and source resistors as well as the required bias inductor. The layout also shows the familiar implementation of the feedback network, with the FET and source capacitor network, protruding underneath it. Furthermore, it is seen to what extent provision was made for tuning, by allowing for tuning pads. The output section of the amplifier included a bend in the transmission line that was essential to fit the design into the *omega* type layout. The effect of this bend, and the other bends, were evaluated with MWO's electromagnetic (EM) simulator, to confirm that it did not deteriorate from the initial

straight design response. At the output of the amplifier, an in-line etched attenuator is shown which is grounded at one end with a gold ribbon wrap-around.

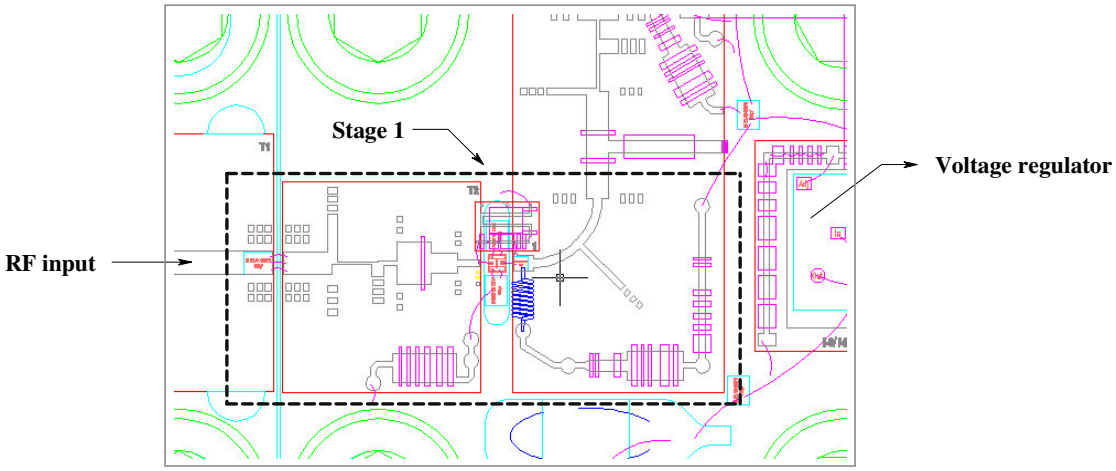


Figure 6.2: Physical implementation of stage one

Figure 6.3 shows the physical design implementation of stage two, which is very similar to that of the first stage. Again the in-line etched attenuator is seen on the output of this amplifier. This portion of the layout also shows the implementation of the bias resistors and the extent to which they were routed within certain size constraints. Ideally, one should attempt to keep these DC lines well-away from the RF transmission lines. Physical size constraints did, however, not allow for placement of these resistors further from the transmission lines.

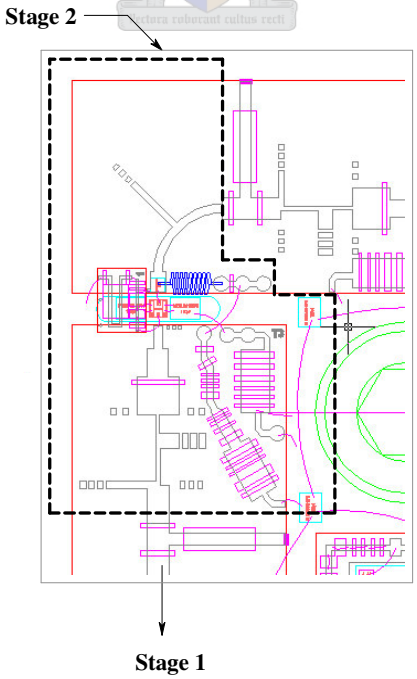


Figure 6.3: Physical implementation of stage two

On the output of the third amplifier stage, shown in Figure 6.4, provision was made for interchanging the etched attenuator with a *thermopad* in case temperature compensation was needed. The same provision would have been desirable on the previous two stages as well, but the design layout did not allow for this. For actual evaluation, two interchangeable carrier plates, one with etched attenuators and one with *thermopads*, were built up. Except for the attenuators, these carrier plates were otherwise identical.

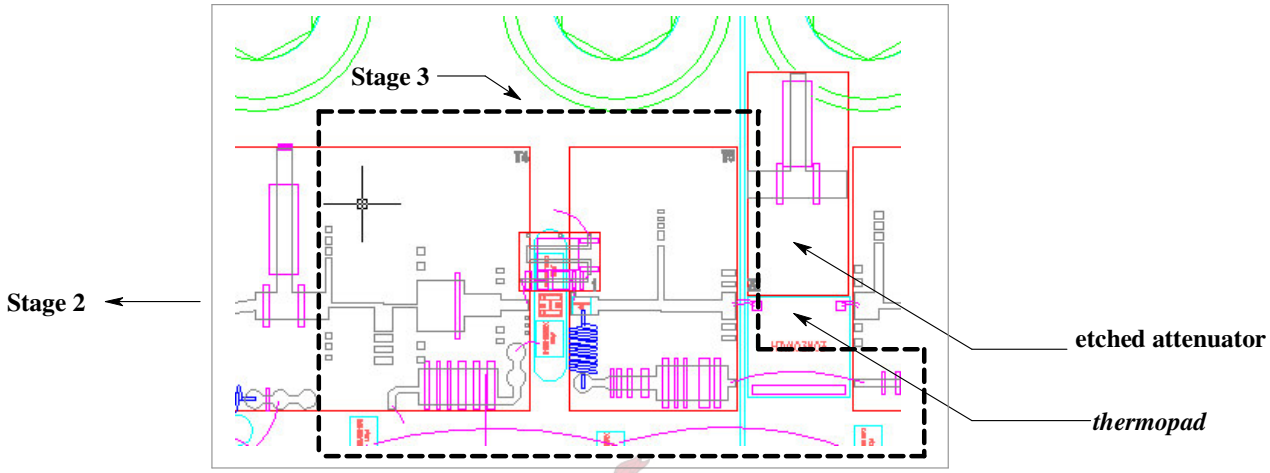


Figure 6.4: Physical implementation of stage three

Stage four implements the same provision for a *thermopad* on its output as did stage three, as seen in Figure 6.5. Furthermore, the layout of stage four is seen to be very similar to that of the first stage.

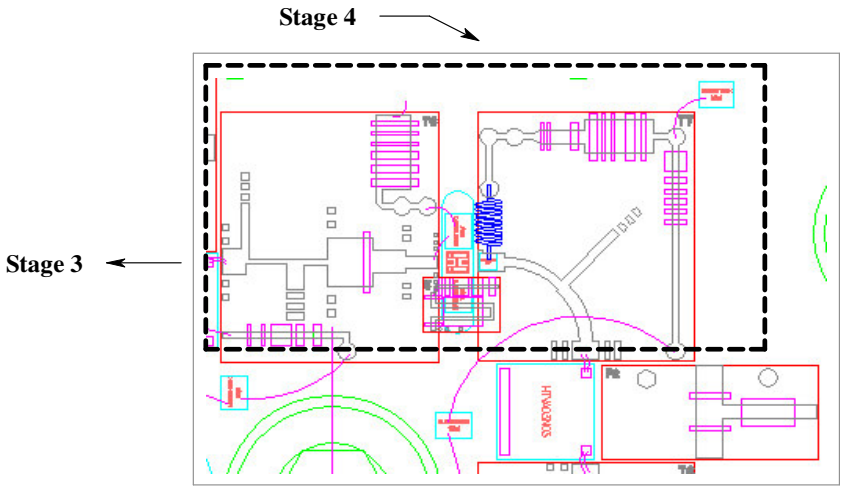


Figure 6.5: Physical implementation of stage four

Figure 6.6 shows the physical implementation of the fifth amplifier stage which is very similar to the previously shown stages. Also shown is the routing of the DC lines that are connected to successive 100 pF bypass capacitors. This routing configuration is also visible on the layouts of the other amplifier stages comprising the design.

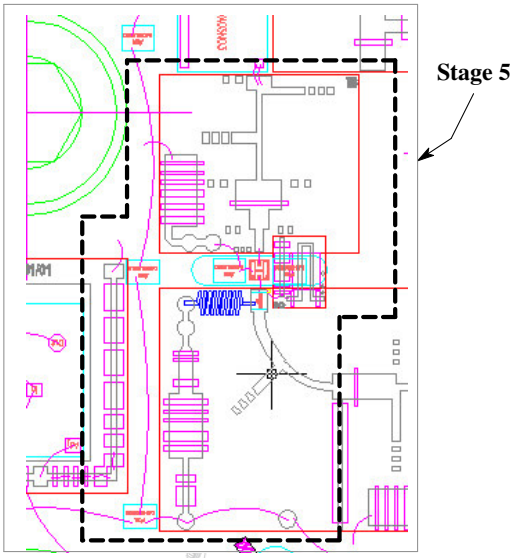


Figure 6.6: Physical implementation of stage five

Figure 6.7 shows the physical implementation of the previously discussed reconstructed amplifier. This is then also the only amplifier that was realized from an existing design, while the other amplifiers were custom designed and optimized for use in the BLA. Physical implementation of this design required custom layout, especially in terms of the bias resistors and for feeding DC to each of the amplifier stages comprising the design.

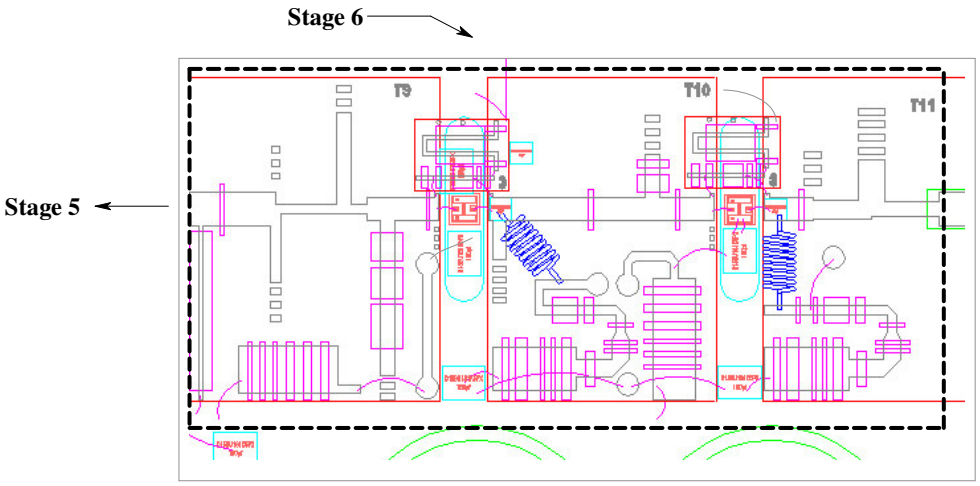


Figure 6.7: Physical implementation of stage six

After the physical implementation of the design, the best evaluation is to physically evaluate the device and compare it with simulated results. The range of measurements that were done on the designed BLA is discussed hereafter and it is shown to what extent the limiting amplifier was successfully realized.

6.3 SPECTRAL ANALYSIS OF THE LIMITING AMPLIFIER: SINGLE-TONE

In this section, a summary of the spectral analysis that was done on the limiting amplifier is given. The measurements show the result of an in-depth single-tone test that was done on the limiting amplifier over temperature. The *thermopads* mentioned earlier, were not implemented in the limiting amplifier RF chain and the device did, therefore, not include any temperature compensation. An automated test setup was used to measure the fundamental and harmonic response of the limiting amplifier over its input dynamic range and the relevant operating frequency bandwidth. The single-tone drive level was adjusted from - 40 dBm to 5 dBm in 1 dBm steps while the frequency was varied in 250 MHz steps. The automated test setup is shown in Figure 6.8.

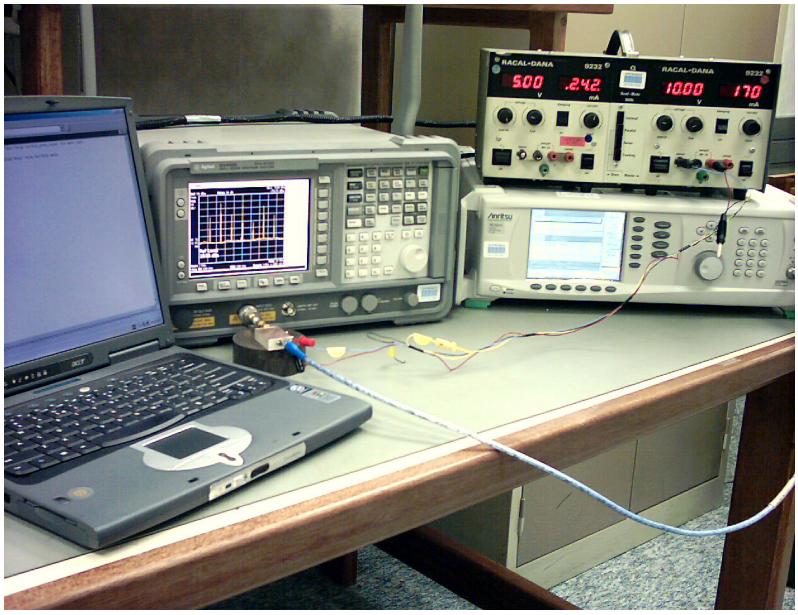


Figure 6.8: Automated test setup for spectral analysis

The setup shows an Anritsu MG3692A 20 GHz signal generator, an Agilent E4408B 9 kHz - 26.5 GHz ESA-L series spectrum analyzer, power supply and PC. As seen in the photo, the device was operated from 10 V while drawing 170 mA. The supply voltage was lowered from 12 V to 10 V since the device operating temperature was very high initially. It is suspected that the actual mounted voltage regulators had a lower rated power handling than what was designed for.

The cable connecting the signal generator to the BLA included some significant loss that was calibrated out during measurements. It should, however, be noted that this calibration was only done at a *spot* drive level of - 20 dBm. Ideally, one should calibrate the cable over the whole frequency band and input power band to take into account the error in drive

level that is introduced by the signal generator. To note as well, is the measurement error that may be introduced by the spectrum analyzer itself. On the output of the BLA a precautionary coaxial type DC blocking capacitor was used that included losses that were not calibrated during measurements. These losses are typically small enough to be ignored.

Figure 6.9 shows the output power response of the designed limiting amplifier as measured at room temperature (25 °C). Again it should be noted, that the output power referred to is the associated saturated output power. The maximum saturated output power was measured at 9.4 dBm, while the minimum saturated output power was measured at 5.8 dBm. This would imply a power window of approximately 3.6 dB centred at 7.6 dBm. Compared to the simulated result which offered a 2.6 dB power window centred at 11.2 dBm, a considerable difference is observed for reasons explained earlier. Compared to simulations, however, one can see a similar drop in the output power response as observed at the higher frequencies (above 12 GHz).

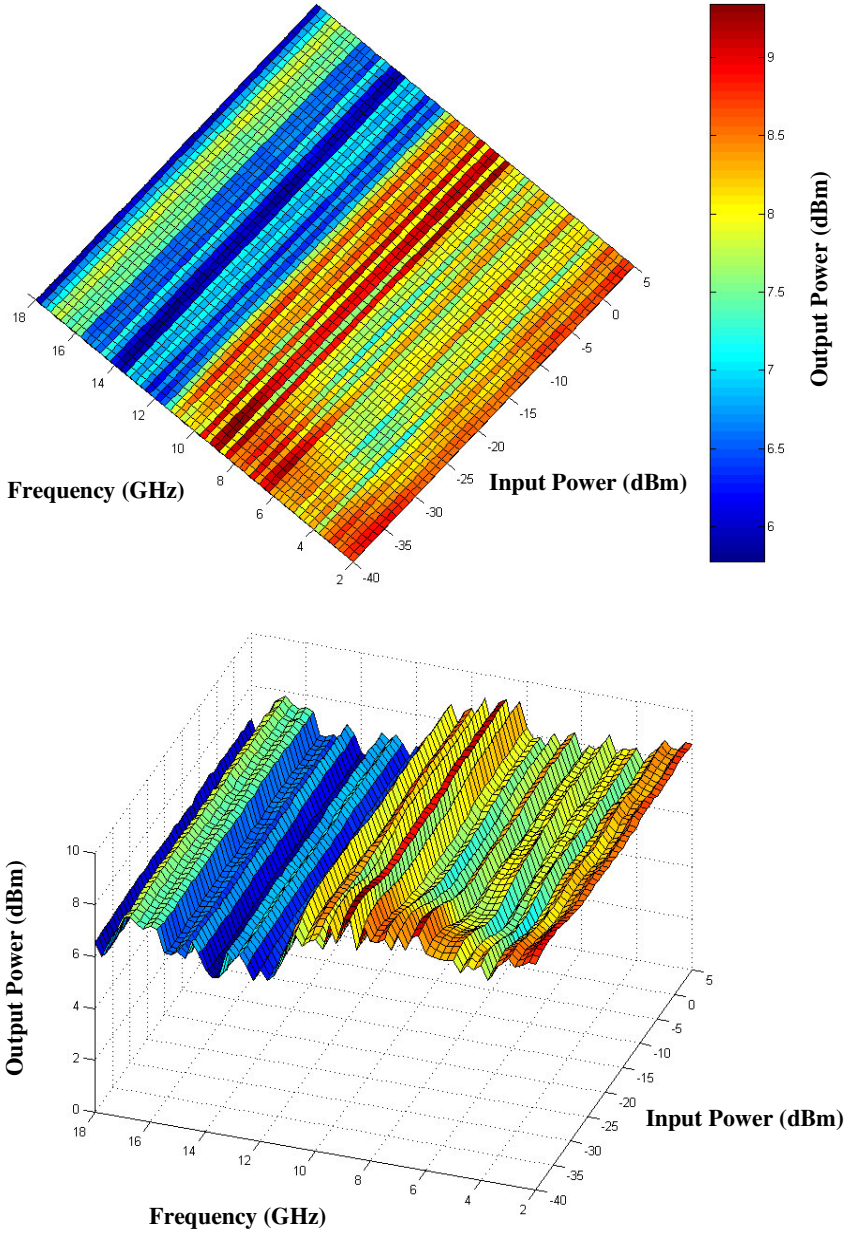


Figure 6.9: Saturated output power response of the designed limiting amplifier (25 °C)

With the saturated output power window of the designed limiting amplifier established, the harmonic suppression was evaluated next. Figure 6.10 shows the second harmonic suppression (SHS) as measured. In the shown graph, the area of concern is for frequencies below 13.25 GHz, since the second harmonics of these frequencies fall within the spectrum analyzer's measurement band. Within the area of concern, the minimum second harmonic suppression is measured to be 15 dBc. This is significantly better than the minimum requirement of 9 dB harmonic suppression.

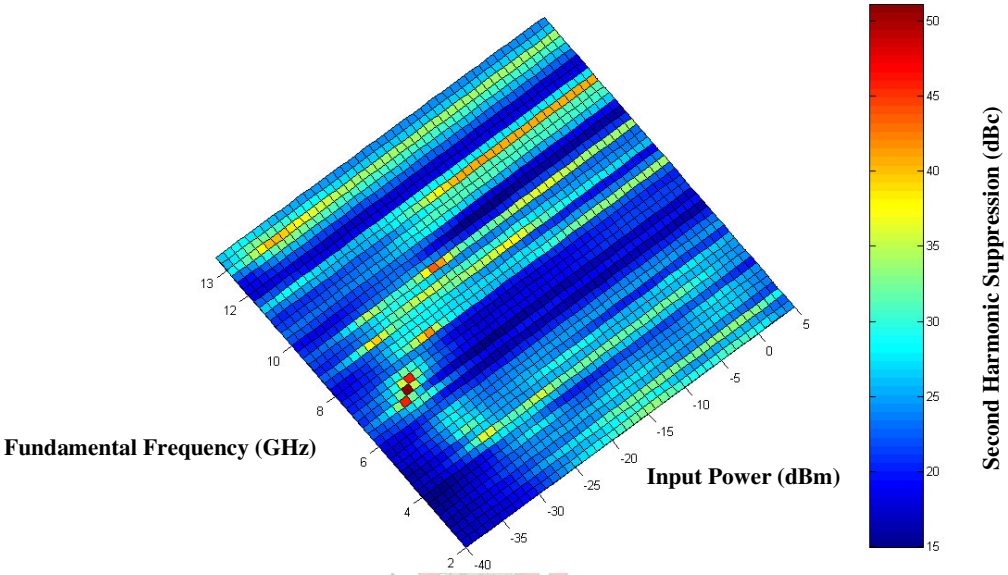


Figure 6.10: Second harmonic suppression of the designed limiting amplifier (25 °C)

The measured third harmonic suppression (THS) is shown in Figure 6.11. The area of concern in this graph is for frequencies below 8.8 GHz, since the third harmonics of these frequencies fall within the spectrum analyzer's measurement band. The shown result was well-predicted by simulations, with typical third harmonic suppression exceeding 8.6 dBc.

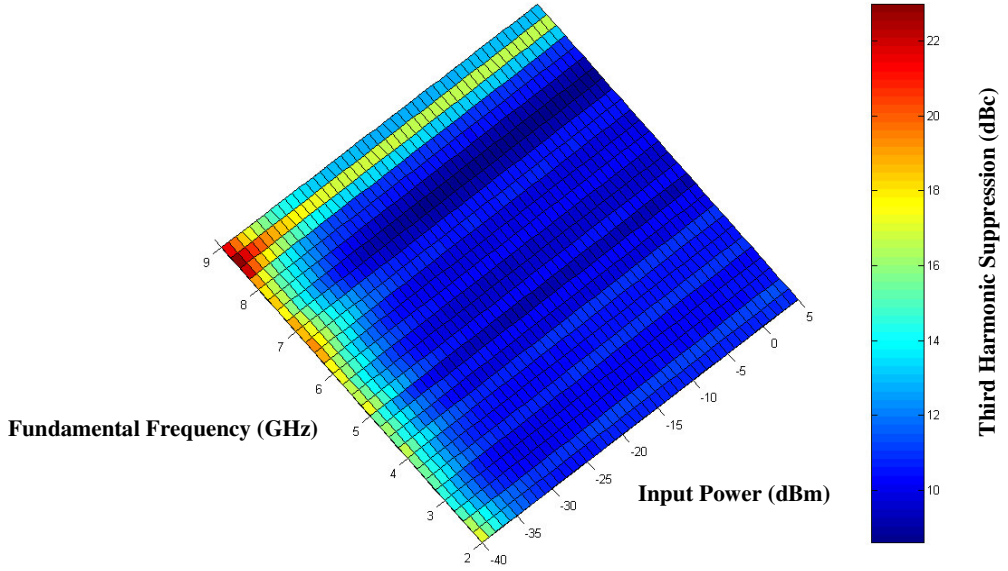


Figure 6.11: Third harmonic suppression of the designed limiting amplifier (25 °C)

The spectral analysis on the designed limiting amplifier was also done at 85 °C and at - 54 °C. These tests made use of the same automated test setup as shown in Figure 6.8, but included a hot/cold plate for testing over temperature. The setup for temperature tests is shown in Figure 6.12.

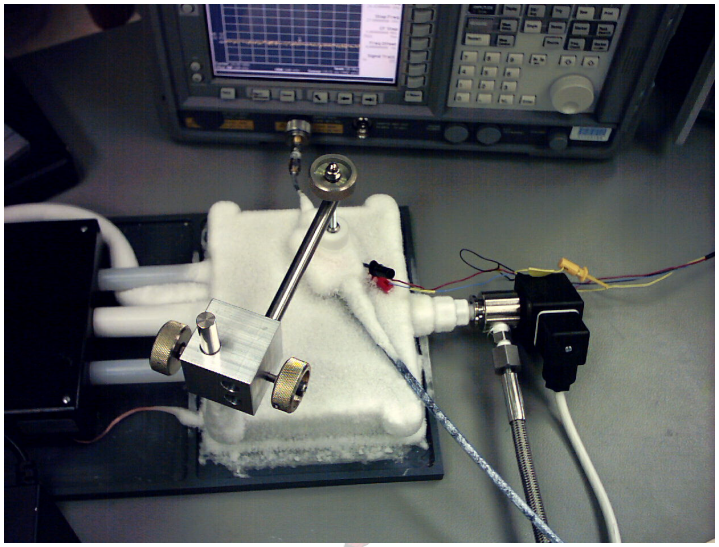


Figure 6.12: Test setup for temperature testing (- 54 °C)

Figure 6.13 shows the saturated output power response of the limiting amplifier as measured at - 54 °C. Evident from this result is the deterioration of the output power window. The maximum saturated output power was measured at 9.3 dBm, while the minimum saturated output power was measured at 5 dBm. This would imply a power window of approximately 4.3 dB centred at 7.15 dBm.

In terms of the measured result at room temperature, the output power window has deteriorated by approximately 0.7 dB. The deterioration, although not very serious, is seen to occur within a certain frequency band rather than for a certain input power range. A range of factors may contribute to the observed deterioration, but the main culprit in this regard is suspected to be the chip capacitors that were used in the design. They have been shown to have at least one significant *dip* in their transmission response (as was shown in Figure 3.5) that typically deteriorates over temperature. The complementing effect of the different capacitors may then cause a significant deterioration at some frequency as was observed. In the original simulated design, it was omitted to take into account the effect of temperature on the capacitors used. Even though, the necessary capacitor models that allowed for temperature variations, existed, the nonlinear FET models did not allow for temperature variations and a full temperature analysis was therefore not done.

In hindsight, it could, however, be suggested that simulations be done taking into account only the temperature effects of the capacitors (if FET models do not allow for temperature variation). The required temperature response may be achieved by establishing a selection of different capacitors that, when used in conjunction with each other, will not deteriorate for example the gain response of the amplifier in question. This again refers to the design approach of *breaking the uniformity* and thereby reducing undesired complementing effects.

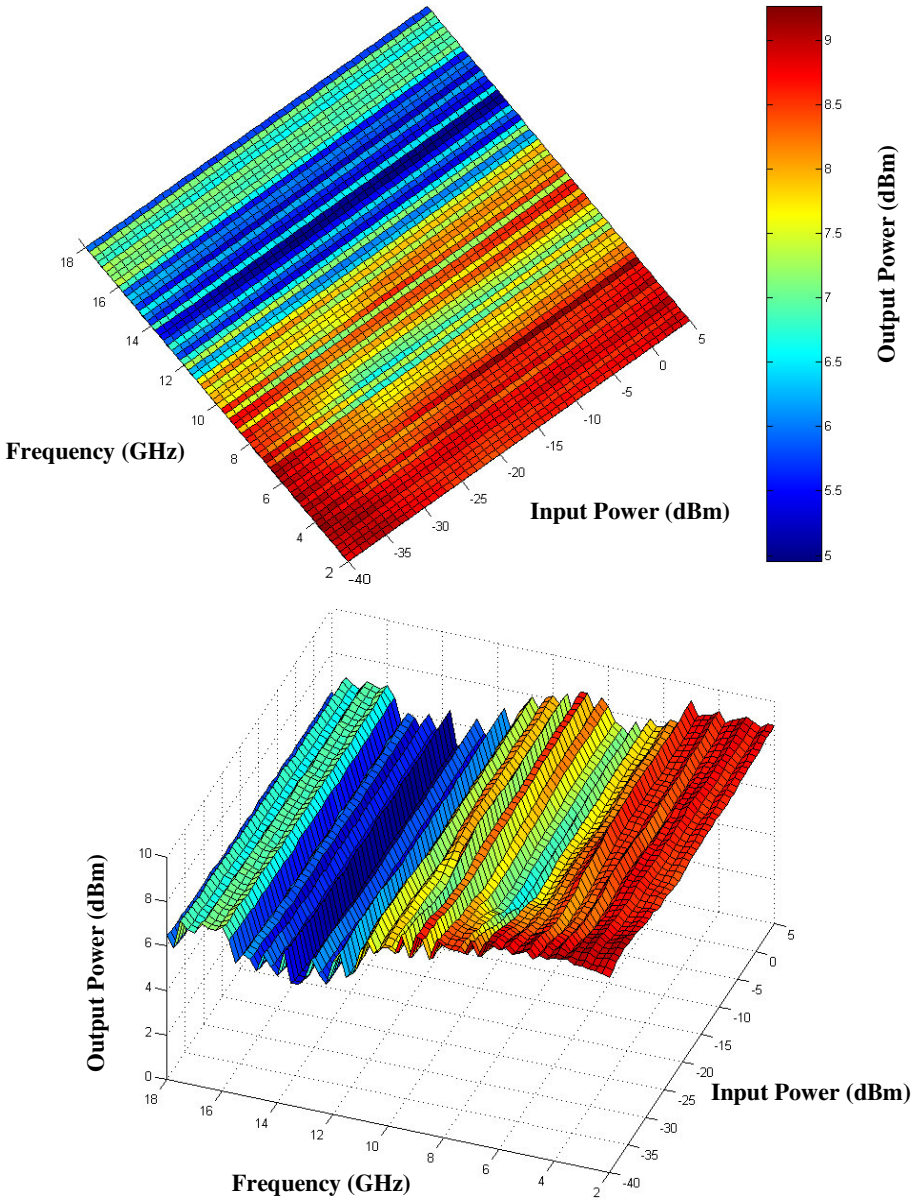


Figure 6.13: Saturated output power response of the designed limiting amplifier (- 54 °C)

The second and third harmonic suppression response of the designed limiting amplifier, as measured at - 54 °C was also evaluated. The graphical results of these measurements are shown hereafter. Figure 6.14 shows the measured second harmonic suppression. The minimum second harmonic suppression was measured to be 12.4 dBc which is worse than the 15 dBc measured at room temperature. Even though this deterioration occurred, the achieved second harmonic remains better than the > 9 dBc specification.

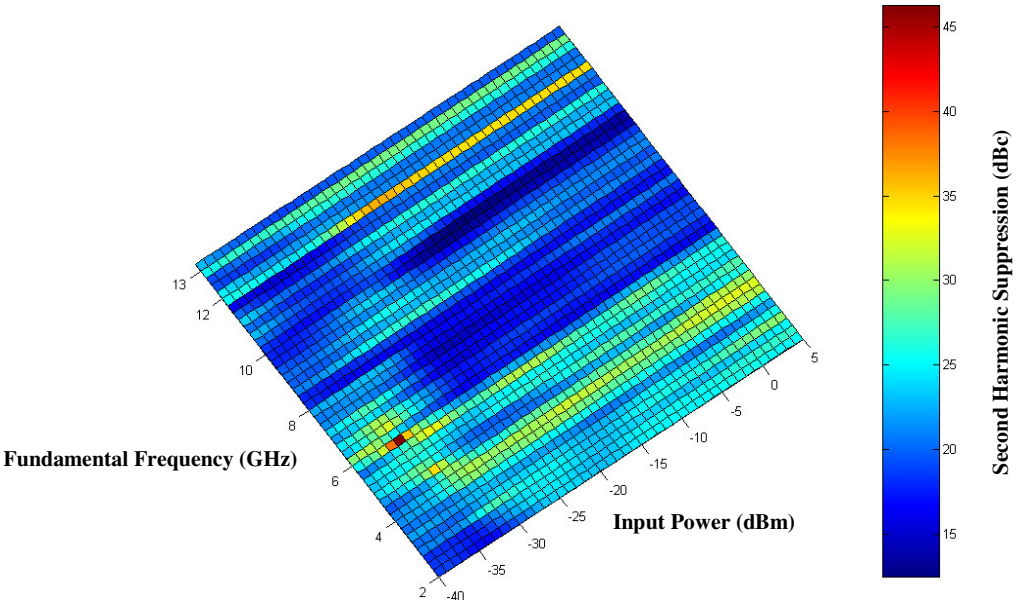


Figure 6.14: Second harmonic suppression of the designed limiting amplifier (- 54 °C)

Figure 6.15 shows the third harmonic suppression of the design limiting amplifier as measured at - 54 °C. The minimum third harmonic suppression was measured to be 8.4 dBc, which indicates a slight deterioration when compared with the 8.6 dBc that was measured at room temperature.

The mechanism, by which this deterioration occurs, was not predicted by the simulated design. One may, however, intuitively reason that the gain of the different amplifiers within the limiting amplifier should be higher at low temperatures and that more power will be fed to the harmonics, with resulting deteriorated harmonic suppression. To evaluate this intuitive reasoning, the design was also evaluated at a temperature of 85 °C.

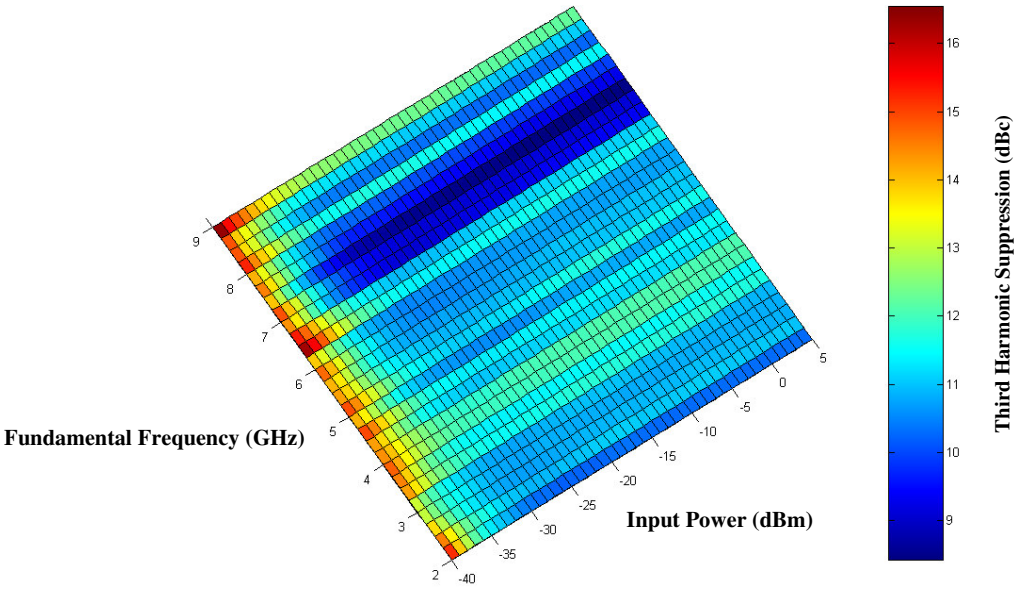


Figure 6.15: Third harmonic suppression of the designed limiting amplifier (- 54 °C)

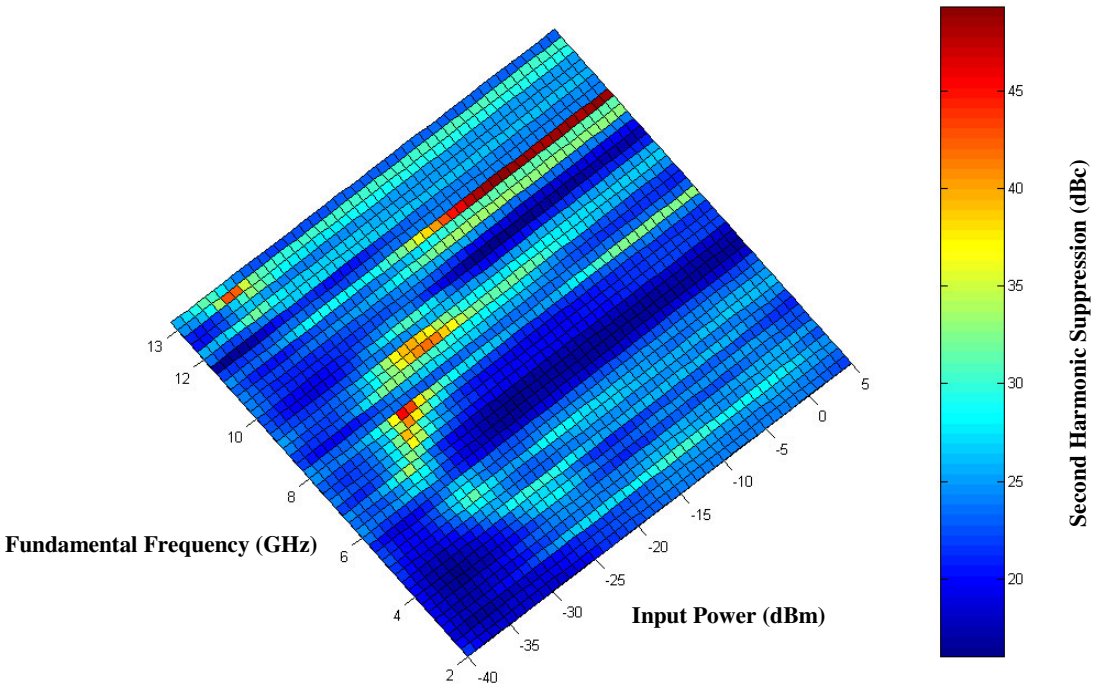


Figure 6.16: Second harmonic response of the designed limiting amplifier (85 °C)

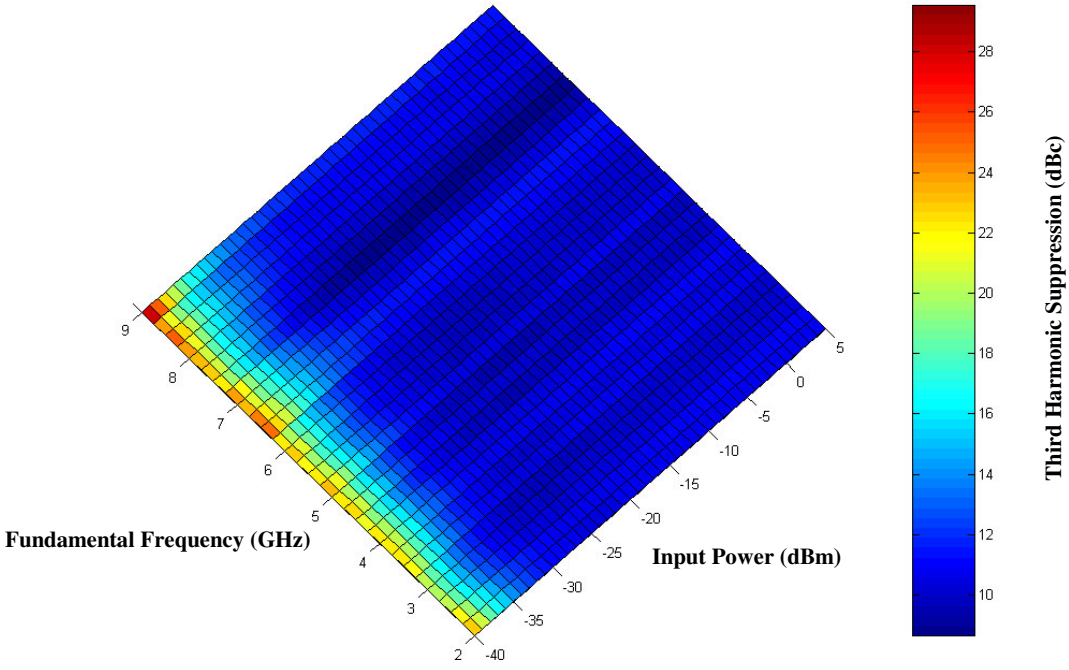


Figure 6.17: Third harmonic suppression of the designed limiting amplifier (85 °C)

At 85 °C, the second harmonic suppression response shown Figure 6.16 was seen to have a minimum of 16 dBc, which shows an improvement on the 15 dBc that was measured at room temperature. The minimum third harmonic suppression, on the other hand, was measured to be 8.7 dBc, which indicates little improvement on the 8.6 dBc that was measured at room temperature. The third harmonic response, as measured at 85 °C, is shown in Figure 6.17.

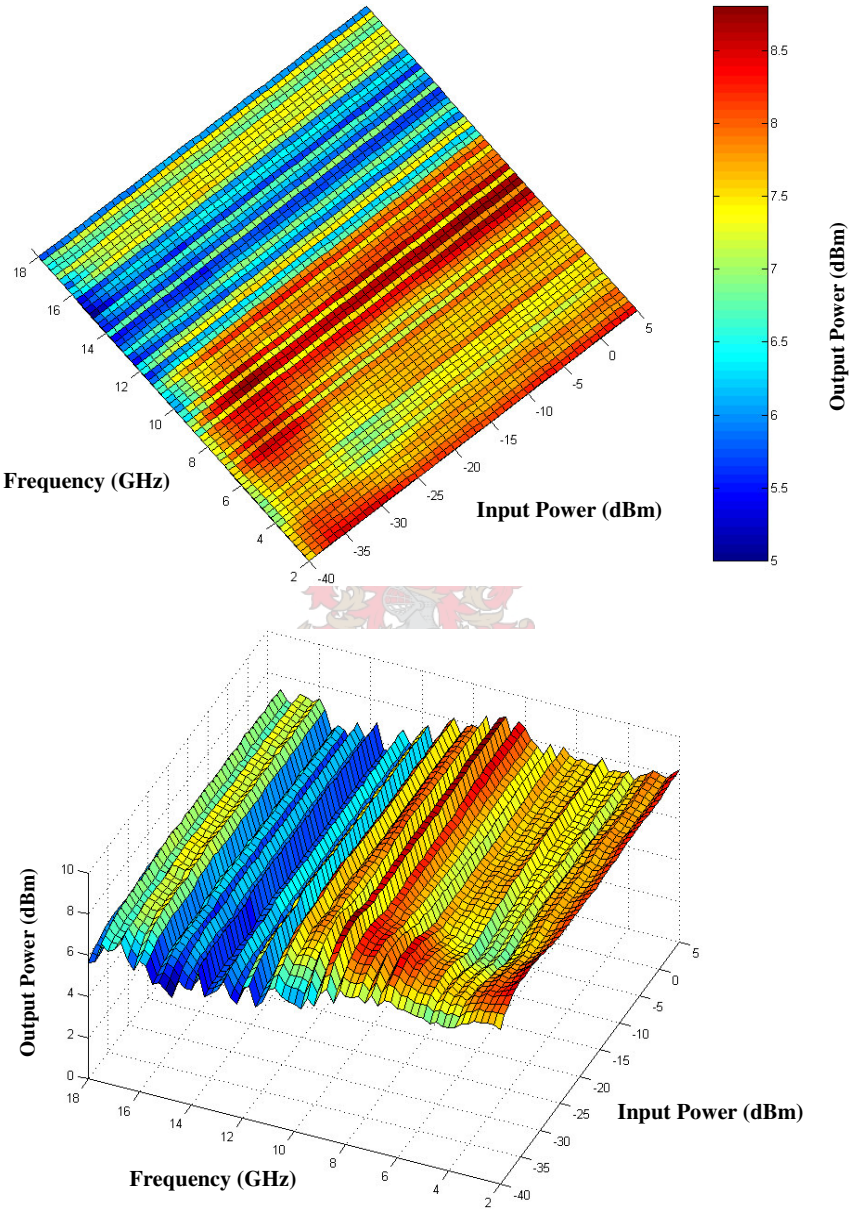


Figure 6.18: Saturated output power response of the designed limiting amplifier (85 °C)

From the measured results, it was seen that temperature variation had almost no influence on the third harmonic levels, while the second harmonic levels were significantly influenced. At the higher temperature one would expect the amplifiers to have less gain and that less power will be fed to the harmonics. In terms of the saturated output power response, there is

little change from the response measured at - 54 °C. The result is shown in Figure 6.18. The output power window as achieved at 85 °C is 3.8 dB with a minimum saturated output power measured at 5 dBm and a maximum at 8.8 dBm.

A summary of the measured results is given in Table 6.1. Seen as a whole, the designed limiting amplifier's response does not deteriorate significantly over temperature. The minimum saturated output power (P_{sat_min}) has a maximum deviation of 0.8 dB from the nominal value at room temperature, while the maximum deviation of the maximum saturated output power (P_{sat_max}) from its nominal is only 0.6 dB. The maximum deviation from the nominal output power window is 0.7 dB.

The minimum second harmonic suppression (SHS_{min}) offers the most significant variation over temperature, with a maximum deviation of 2.6 dB from its nominal value at room temperature. Nonetheless, this variation did not cause a specification failure and still offers good harmonic suppression (12.4 dBc minimum).

The minimum third harmonic suppression (THS_{min}), however, resulted in a specification failure (THS_{min} < 9 dBc) that remained almost unchanged over temperature. It may be assumed that this failure was due to measurement errors in the initial single-tone test setup with only a small error correction required to comply with the required 9 dBc. Rather, this failure is seen as a significant flaw in the designed limiting amplifier that should have been addressed more carefully during the design phase. Simulations showed a minimum THS on the brink of the 9 dBc limit. Rather than allowing for such a *border-case* result, it should rather be attempted to achieve a trade-off between the different harmonic suppression responses. The SHS may for example be *slackened* to achieve the desired THS specification.

Specification	**- 54 °C**	**25 °C**	**85 °C**
P_{sat_min} (dBm)	5	5.8	5
P_{sat_max} (dBm)	9.3	9.4	8.8
Output Power Window (dB)	4.3	3.6	3.8
SHS_{min} (dBc)	12.4	15	16
THS_{min} (dBc)	8.4	8.6	8.7

Table 6.1: Summary of the spectral analysis done over temperature

In terms of temperature compensation, the *thermopads* for which provision was made in the initial design were not used. When physically measured, the temperature compensated attenuators offered significant losses at higher frequencies, independent of different bonding configurations that were attempted. Furthermore, the designed limiting amplifier's response did not deteriorate too much over temperature and did, therefore, not necessitate the need for the *thermopads*. Notwithstanding this, the use of a *thermopad* in a limiting amplifier is suggested since it may still offer an improved response over temperature. It is, however, suggested that a *thermopad* with a higher frequency rating (DC-26 GHz for example) be used, to ensure an optimal response at least over the desired 2-18 GHz bandwidth.

Figure 6.19 shows the response of the proposed temperature variable attenuator over frequency as measured in a test jig with short 50 Ω transmission lines. It is seen that the return loss is typically better than 10 dB, while the point of concern is the sloped response and the eventual 6 dB loss at 18 GHz. Implementation of this attenuator in the existing design would lead to a further drop-off in the measured saturated output power response. For this reason, *thermopads* were not used in the final design.

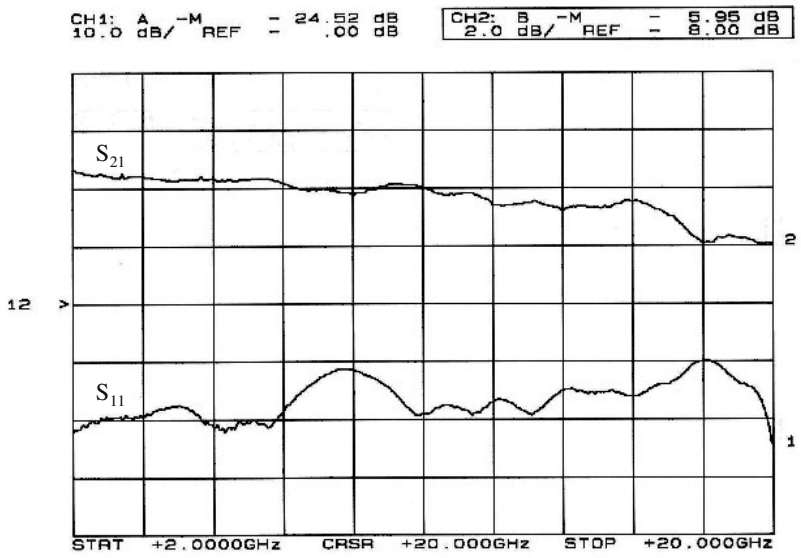


Figure 6.19: Measured response of a *thermopad*

The foregoing discussion was concerned with the single-tone spectral analysis that was done on the designed limiting amplifier and showed to what extent the design was practically realizable. The measured results allowed one some unique insight as to the intricacies of the device's actual operation especially over temperature. The section to follow, discusses another aspect of the limiting amplifier, namely its gain variation, in particular as a function of input drive level. This investigation offers further insight as to the limiting amplifier's capability to provide a *constant* output power.

6.4 GAIN RESPONSE OF THE LIMITING AMPLIFIER

The discussions up to now were concerned mainly with the small-signal power gain of RF amplifiers. When talking about the gain response of the limiting amplifier, the *gain* referred to, is not small-signal power gain in the true sense of the word. Rather, it refers to gain presented to some input tone within the limiting amplifier's operating dynamic range. The normal gain definition is, therefore, not used in conjunction with the limiting amplifier.

Gain response measurements serve to show how the gain of the limiting amplifier varies in accordance with input drive level. Results as measured at input drive levels of - 45 dBm, - 10 dBm and 5 dBm are discussed hereafter. The transfer characteristic of the practical limiting amplifier as shown in Figure 6.20 helps in explaining the expected decrease in gain as the input drive level increases. Within the linear region of the limiting amplifier, the gain ideally stays constant at G_1 as

expected. In this case, G_1 is the actual small-signal power gain. Within the limiting amplifier's dynamic range, however, gains G_2 and G_3 vary in accordance with input power P_{in_2} and P_{in_3}, to ensure a *constant* output power. For sake of illustration, typical values were assigned to the different parameters seen in Figure 6.19.

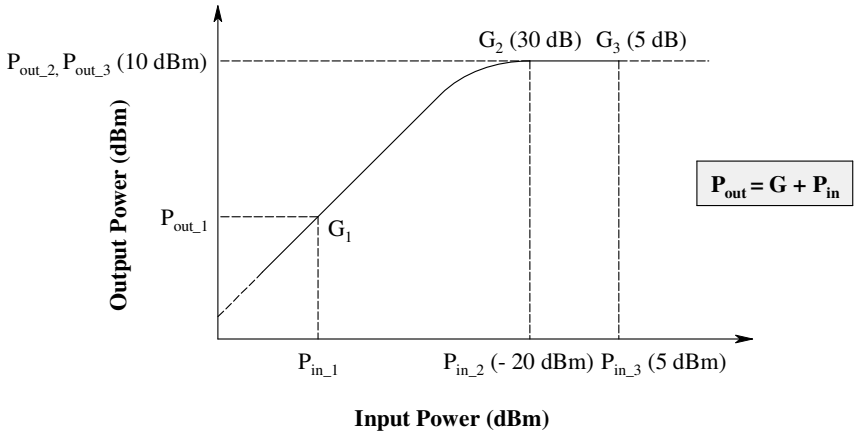


Figure 6.20: Transfer characteristic of a practical limiting amplifier revisited

From previous discussions it is clear that a large small-signal gain is necessary to ensure that a signal at the low end of the limiting amplifier's input dynamic range gets limited to within the desired output power window. Figure 6.21 shows the small-signal (- 45 dBm drive level) gain response of the limiting amplifier as measured on a vector network analyzer (VNA) for comparison with the simulated result. The typical measured small-signal gain is approximately 52 dB with a ± 2 dB ripple. The measured input return loss is approximately 8.2 dB.

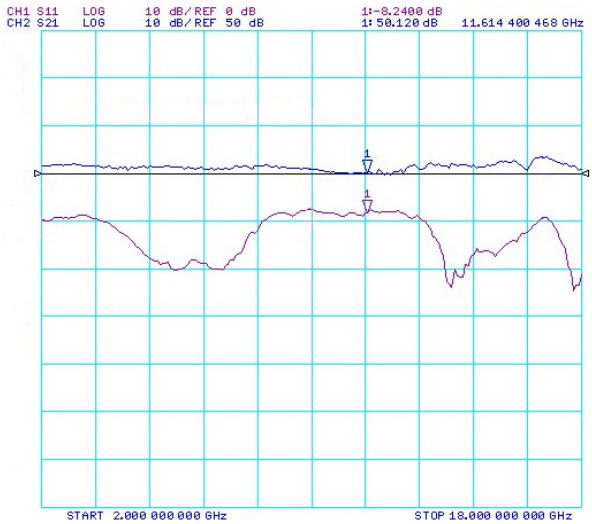


Figure 6.21: Measured small-signal gain response of the limiting amplifier

A close comparison is seen between the measured result and the simulated result as seen in Figure 6.22. A drive level of - 45 dBm was used for the simulation. The simulated response shows a gain of about 53.6 dB and a gain ripple of ± 2.1 dB. Furthermore, it is seen that the return loss response compares well with the measured result, even though the measured response is not as good as simulated. It appears as though one should put more effort into improvement of the input return loss, since actual measurements are seldom as good as simulated and to be taken into account as well, is the expected return loss deterioration as a function of input drive level. Measurements to follow will then also show to what extent the input return loss as measured, deteriorates as the drive level increases.

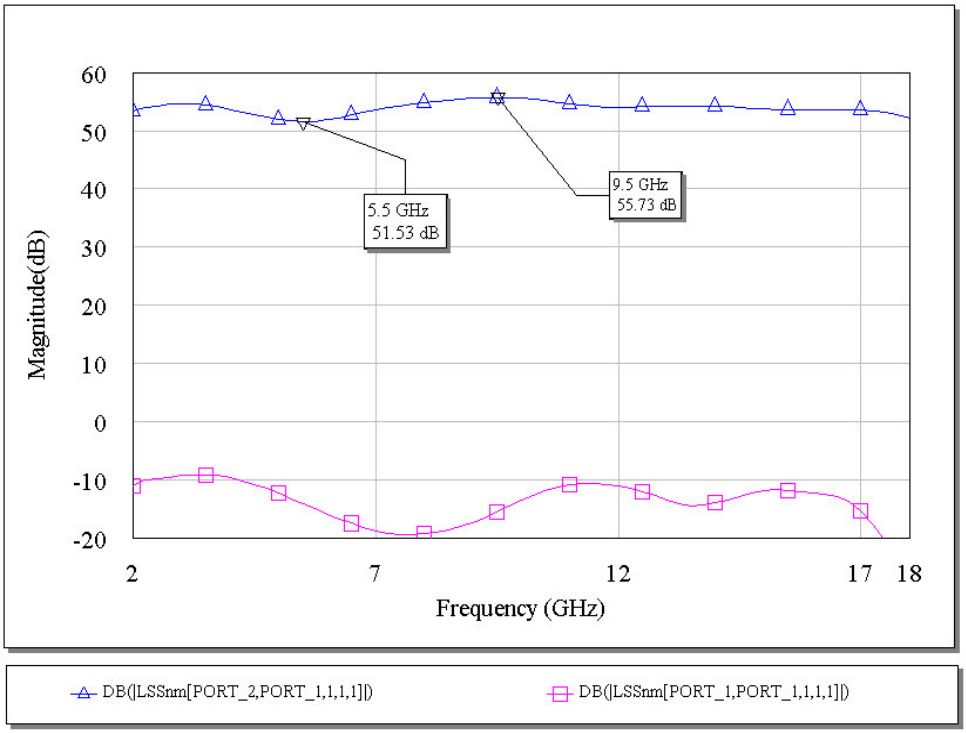


Figure 6.22: Simulated small-signal gain response of the limiting amplifier

Figure 6.23 shows a measurement of the gain response of the designed limiting amplifier as measured for a - 10 dBm drive level. The typical measured gain is in the order of 20 dB which confirms that the gain available to a signal with a - 10 dBm power level will be less than that at a small-signal drive level (less than - 40 dBm). The measurement therefore also confirms the resulting output power as measured on the spectrum analyzer for a - 10 dBm drive level.

The simulated result as seen in Figure 6.24 again shows a close relation with the measured gain response. The measured and simulated return loss response; also track each other fairly well. Another aspect observed is the fact that the gain ripple starts to decrease as the input drive level increases, which allows for a smaller output power window. As explained earlier, this is due to the onset of saturation within the different amplifiers in the limiting amplifier RF chain.

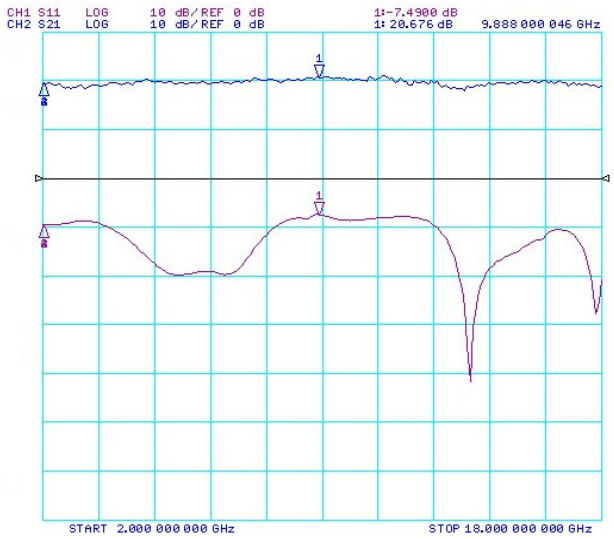


Figure 6.23: Measured gain response of the limiting amplifier for a - 10 dBm drive level

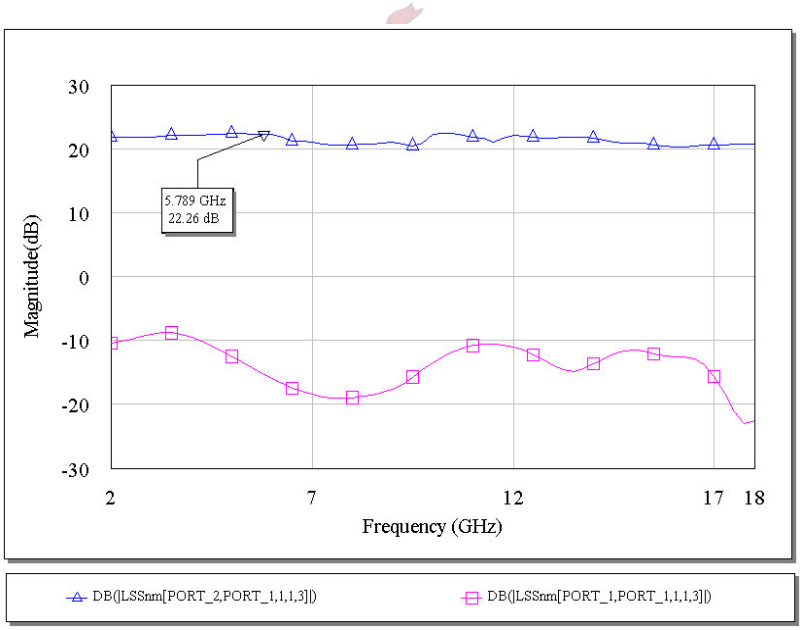


Figure 6.24: Simulated gain response of the limiting amplifier for a - 10 dBm drive level

The gain response measurement as taken at a drive level of 5 dBm is shown in Figure 6.25. Here one sees very significant input return loss deterioration. The simulated result, however, as seen in Figure 6.26, compares well with the shown measured response. The input return loss has deteriorated to a maximum level of approximately 5.7 dB, while the measured result offered a 6.1 dB input return loss. It is seen that the measured gain has decreased to approximately 4 dB while the simulated gain was in the order of 7.5 dB. This would then also explain why simulations offered a higher saturated output power than that measured.

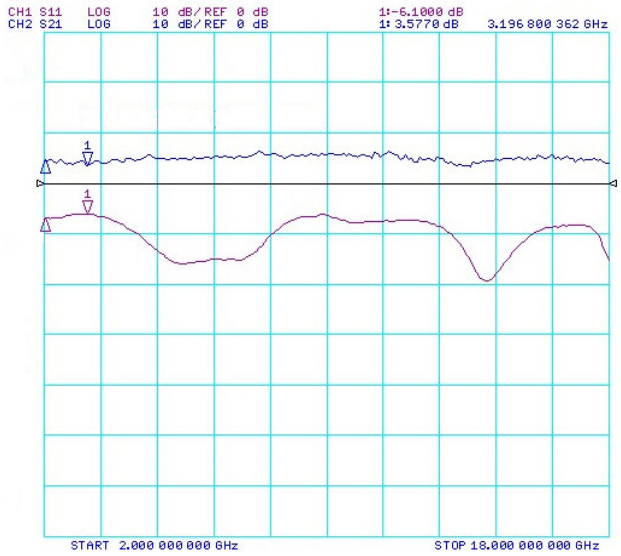


Figure 6.25: Measured gain response of the limiting amplifier for a 5 dBm drive level

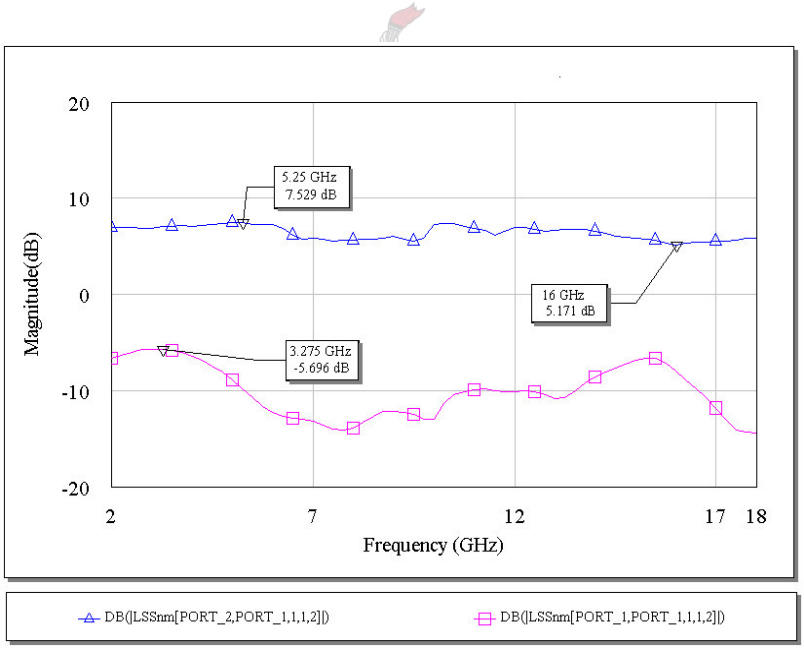


Figure 6.26: Simulated gain response of the limiting amplifier for a 5 dBm drive level

The foregoing discussed results gave an indication of the gain response of the limiting amplifier as a function of input drive level. In general it was seen that the higher the drive level, the lower the measured gain and thereby ensuring a constant saturated output power response. Furthermore, it was seen that there is a general deterioration in the input return loss as the drive level increased. This fact then also establishes a new point of concern in the design of a limiting amplifier that may

necessitate the implementation of the properties associated with the balanced amplifier and other devices used for improved impedance matching (Chapter 3).

The discussion thus far helped in further establishing a better intuitive feel for the designed limiting amplifier's operation and showed to what extent trade-offs, especially in terms of return loss, had to be taken to achieve a desired saturated output power response. The section to follow concludes this chapter with the evaluation of the limiting amplifier's small-signal suppression response as physically measured.

6.5 SMALL-SIGNAL SUPPRESSION MEASUREMENTS

In this section the small-signal suppression characteristics of the designed limiting amplifier are further evaluated with physical measurements. This evaluation is concerned with nominal input tones at 3 GHz and 9 GHz, at drive levels of 0, - 20 and - 35 dBm respectively, while representing only a portion of the BLA's input dynamic range and operating bandwidth.

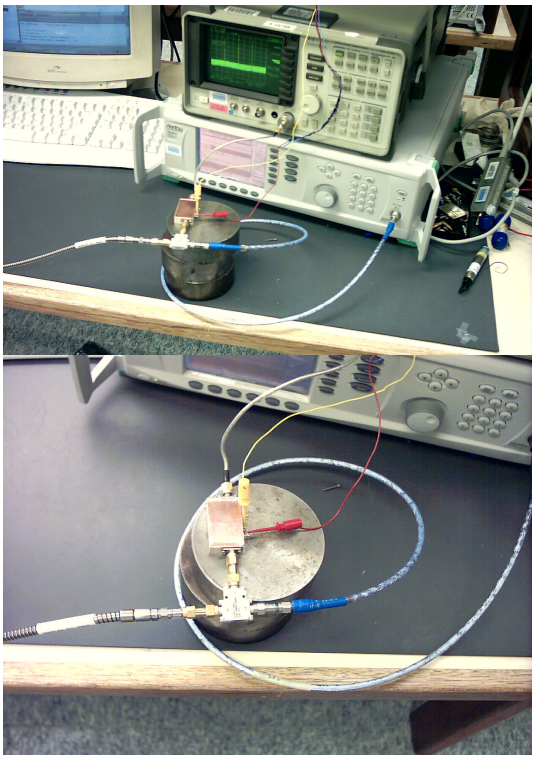


Figure 6.27: Experimental setup for two-tone tests

Figure 6.27 shows the experimental setup for two-tone tests. A Wilkinson splitter is used to combine two separate tones, obtained from two different signal generators. This two-tone signal is then fed to the limiting amplifier for evaluation of the device's small-signal suppression characteristics as seen on a spectrum analyzer. One of the signal generators is used in a static mode for generating a fixed desired (maximum amplitude) signal. The other signal generator is controlled by a PC to

provide the varied frequency and amplitude of the undesired (minimum amplitude) signal. The necessary cable calibrations were done to ensure the desired power levels to be present on the limiting amplifier input.

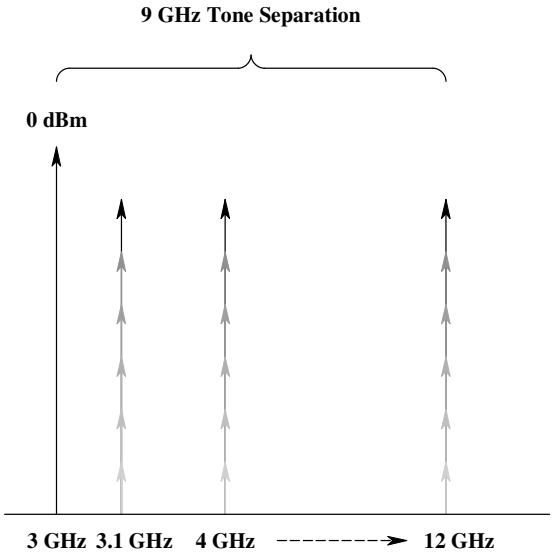


Figure 6.28: Input spectra presented to the BLA (desired signal of 3 GHz @ 0 dBm)

The first set of measurements was taken with the level of the desired signal at 3 GHz with a power level of 0 dBm. Figure 6.28 shows this desired signal together with the varied input spectra that was presented to the BLA. Also shown is the associated 9 GHz tone separation with the frequency of the desired signal being 3 GHz and that of the undesired signal being 12 GHz. Again signal separations of 3, 6, 9, 12 and 15 dB respectively, were used. The result of the measurement is shown in Figure 6.29. This plot shows the resulting output signal separation versus the input signal separation as measured at different tone separations. The level of small-signal suppression is again portrayed by the offset from the shown reference line. In general, small-signal suppression is more pronounced at large input signal separations and for large tone separations, as may have been expected.

The results, however, also show significant deviations from the nominal expected response. These deviations are particularly prominent at tone separations of 3 GHz, 6 GHz and 9 GHz respectively. At a tone separation of 6 GHz, significant deterioration in the output signal separation is seen, with only partially observed small-signal suppression. The reason for this deterioration was found to be the interaction of harmonically related tones. Depending on the phase of the relevant tones, the resulting power level contribution may either be constructive or destructive.

At the 6 GHz tone separation, the resulting undesired signal at 9 GHz adds in phase with the third harmonic of the 3 GHz desired signal, resulting in the deteriorated small-signal suppression as observed on the BLA's output. For tone separations of 3 GHz and 9 GHz, an improved small-signal separation is observed, which suggests that harmonically related tones add out of phase. The observed constructive and destructive power level contributions at harmonically related tones were not predicted by simulations. Rather than showing the contributing effect of harmonically related tones, MWO shows the presence of these tones with their different associated power levels. It is then also for this reason that two-tone simulations did not include evaluations at harmonically related tones.

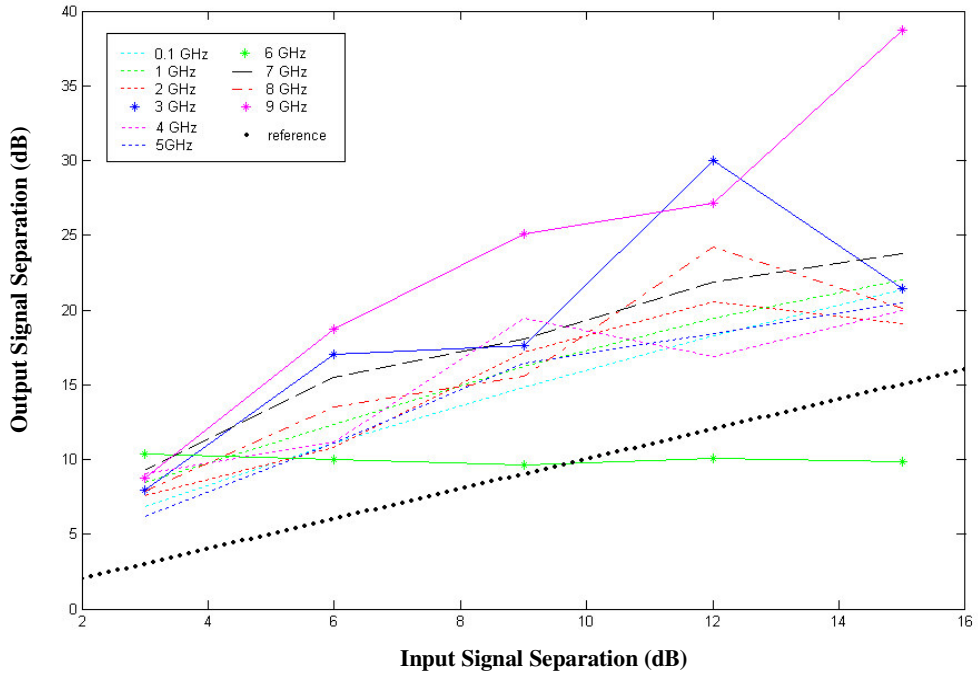


Figure 6.29: Output versus input signal separation at varying tone separations (desired signal of 3 GHz @ 0 dBm)

Figure 6.30 shows the varied input spectra that were presented to the BLA, but with a desired signal at 3 GHz with a power level of - 20 dBm. This situation would then imply operation within the mid-band of the BLA's input dynamic range

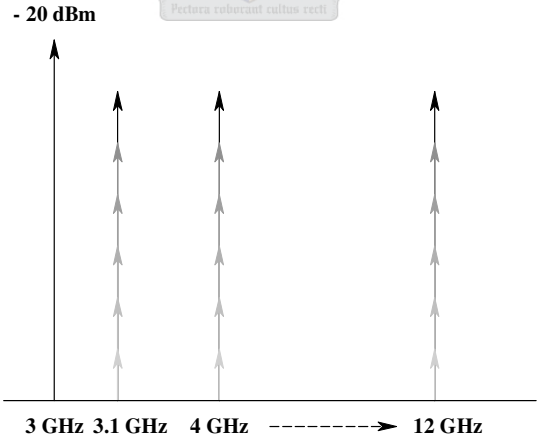


Figure 6.30: Input spectra presented to the BLA (desired signal of 3 GHz @ - 20 dBm)

Figure 6.31 shows the small-signal suppression as measured at the different tone separations. Again one can see the same general trend as was seen in Figure 6.29, with small-signal suppression being more pronounced at large input signal

separations and for large tone separations. Deviations from the nominal expected response due to the interaction of harmonically related tones are again seen.

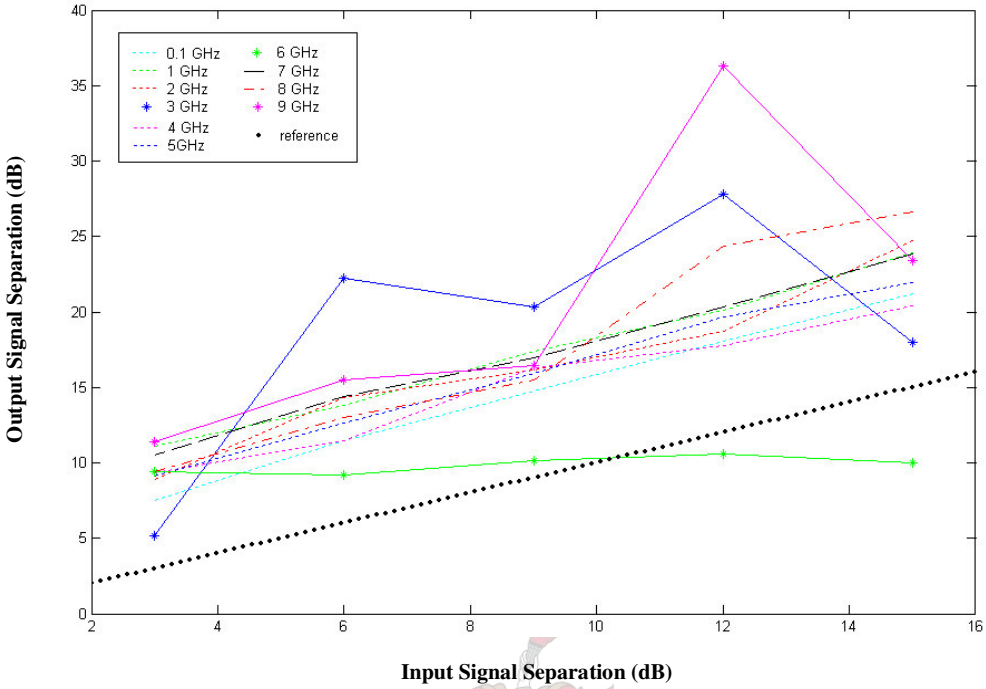


Figure 6.31: Output versus input signal separation at varying tone separations (desired signal of 3 GHz @ - 20 dBm)

Figure 6.32 shows the varied input spectra that were presented to the BLA, but with a desired signal at 3 GHz with a power level of - 35 dBm. This situation implies operation on the brink of the low end of the BLA's input dynamic range.

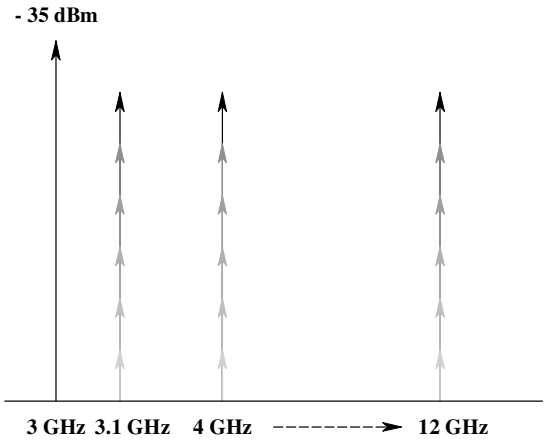


Figure 6.32: Input spectra presented to the BLA (desired signal of 3 GHz @ - 35 dBm)

Figure 6.33 shows the resulting small-signal suppression as measured at the different tone separations. Deviations from the nominal expected response, due to the interaction of harmonically related tones, are again seen. These deviations are more pronounced, particularly at tone separations of 3 GHz and 6 GHz respectively. In this case, the deviation previously observed at a 9 GHz tone separation is less pronounced and coincides with the nominal expected response.

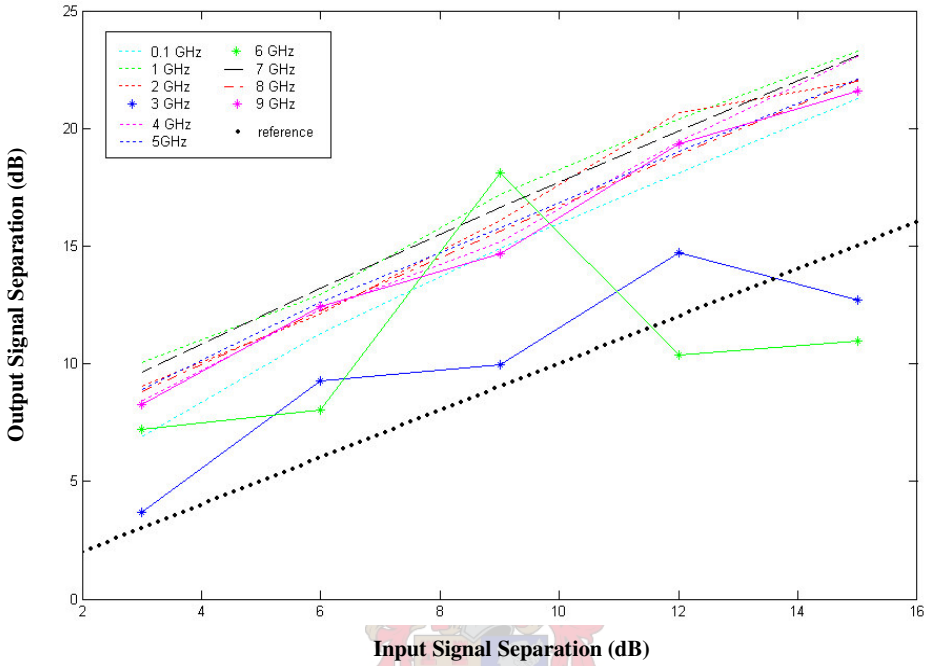


Figure 6.33: Output versus input signal separation at varying tone separations (desired signal of 3 GHz @ - 35 dBm)

Tone Separation (GHz)	**0.1**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
Small Signal Suppression (dB) Desired signal of 3 GHz @ 0 dBm	3.9	5.5	4.1	4.9	4.9	3.2	- 5.2	6.3	4.9	5.7
Small Signal Suppression (dB) Desired signal of 3 GHz @ -20 dBm	4.5	7.8	5.9	2.2	5.4	6.1	- 5	7.5	6.4	7.4
Small Signal Suppression (dB) Desired signal of 3 GHz @ -35 dBm	3.9	6.9	6.1	- 2.3	5.4	5.9	- 4	6.6	5.8	5.3

Table 6.2: Summary of the minimum small-signal suppression as measured (desired signal at 3 GHz)

Table 6.2 shows a summary of the minimum small-signal suppression as obtained from the foregoing results. The negative values shown are due to the interaction of harmonically related tones and indicate where small-signal suppression does not occur.

Typically the small-signal suppression increases as the tone separation increases, but it is seen that variances on this condition do occur. A general deterioration is seen in small-signal suppression as operation shifts to the high end of the BLA's input dynamic range, but variances on this condition is also seen to occur.

To further understand the observed small-signal suppression, the same two-tone measurements were again performed, but with the desired signal at 9 GHz. Figure 6.34 shows the result with the desired signal having power of 0 dBm. The result shows the achieved small-signal suppression, but to an extent that was not predicted. The shown result not only shows the interaction of harmonically related tones but also shows the effect of the varying compression characteristics of the different amplifiers within the limiting amplifier. The compression characteristics of the amplifiers are suspect in this case, because of the deteriorated small-signal suppression at tone separation 8 GHz. At this tone separation there is no apparent harmonic related tones that may influence the relevant small-signal suppression, as was the case for the previous set of measurements.

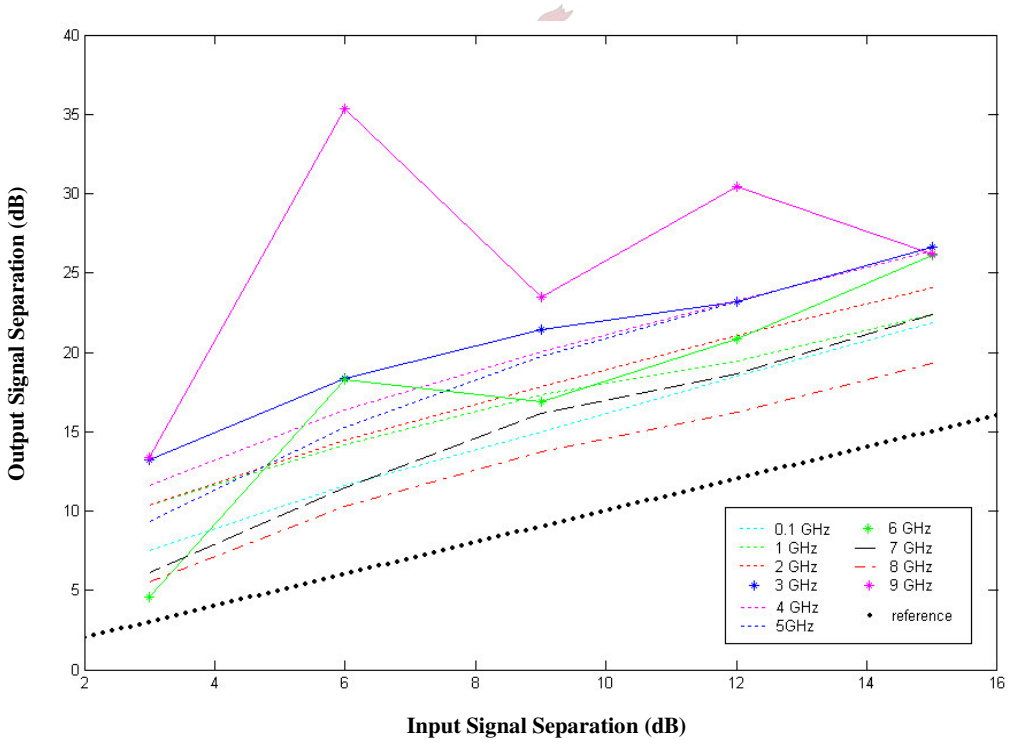


Figure 6.34: Output versus input signal separation at varying tone separations (desired signal of 9 GHz @ 0 dBm)

Figure 6.35 shows the set of measurements for the desired signal having power of - 20 dBm. In general, this result shows overall improved small-signal suppression, with small-signal suppression again deteriorated at a tone separation of 8 GHz.

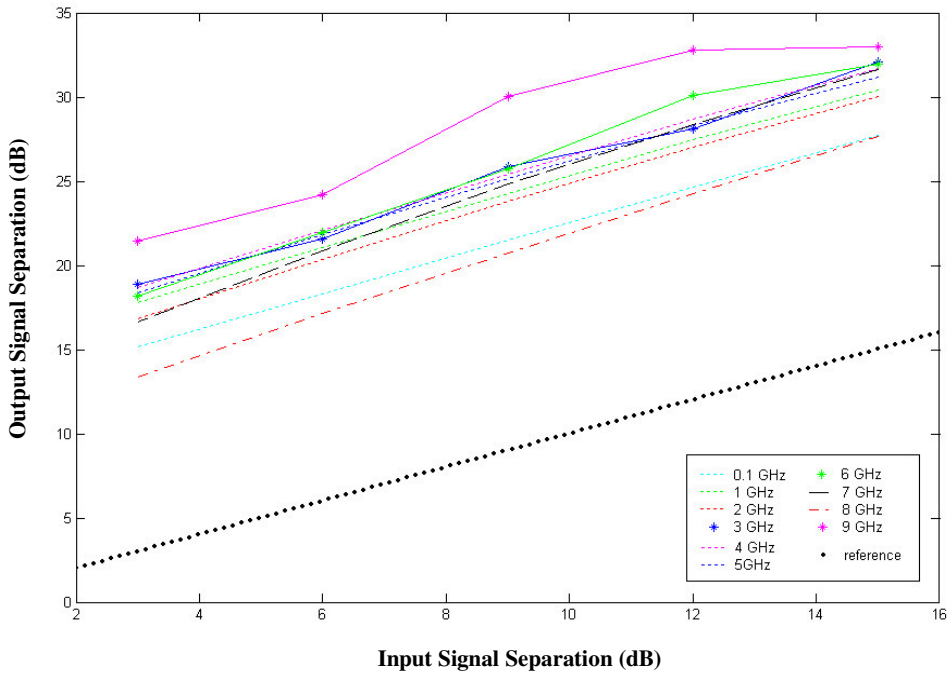


Figure 6.35: Output versus input signal separation at varying tone separations (desired signal of 9 GHz @ - 20 dBm)

Figure 6.36 shows the set of measurements for the desired signal having power of - 35 dBm. This result shows overall deteriorated small-signal suppression, with the deterioration at a tone separation of 8 GHz being very significant.

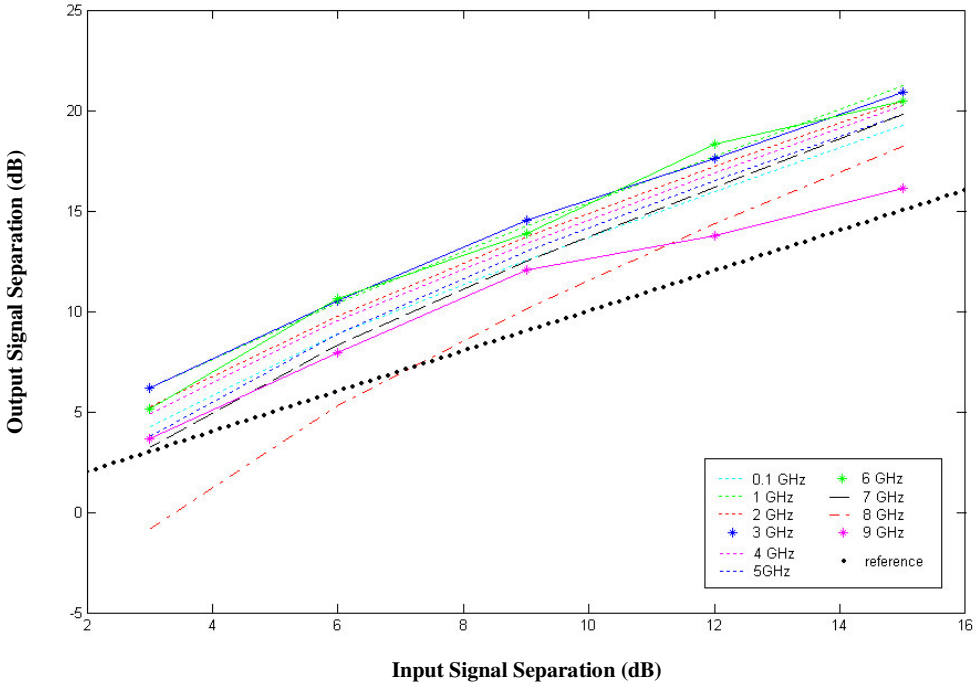


Figure 6.36: Output versus input signal separation at varying tone separations (desired signal of 9 GHz @ - 35 dBm)

Table 6.3 shows a summary of the measured minimum small-signal suppression for the desired signal at 9 GHz.

Tone Separation (GHz)	**0.1**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
Small Signal Suppression (dB) Desired signal of 9 GHz @ 0 dBm	4.5	7.4	7.4	10.2	8.6	6.3	1.6	3.1	2.5	10.4
Small Signal Suppression (dB) Desired signal of 9 GHz @ - 20 dBm	12.2	14.8	13.8	15.6	15.7	15.4	15.2	13.6	10.4	18
Small Signal Suppression (dB) Desired signal of 9 GHz @ - 35 dBm	1.3	3.2	2.2	3.2	1.9	0.7	2.1	0.2	- 3.9	0.7

Table 6.3: Summary of the minimum small-signal suppression as measured (desired signal at 9 GHz)

The results summarized in Table 6.3 give no clear indication as to a general trend in the observed small-signal suppression when seen as a function of tone separation and operation over the BLA's input dynamic range. Apparent however, is that the BLA does offer significant small-signal suppression within the mid-band of its input dynamic range for this particular measurement. At the low end of the BLA's input dynamic range, small-signal suppression is significantly deteriorated while reasonable small-signal suppression is achieved at the high end of the BLA's input dynamic range.

Even though, the shown results do not allow for deriving a sound hypothesis on the achieved small-signal suppression, it offers very significant insight into this topic.

Firstly, it has been pointed out that output signal separation and thus small-signal suppression, generally improves as the input signal separation increases. Deviation on this statement was shown to occur typically at harmonically related tones but may also be influenced by the composite compression characteristics of the different RF amplifiers comprising the BLA design.

Secondly, it has been pointed out that significant variance in small-signal suppression exists as a function of both tone separation and where the BLA is operated in terms of input dynamic range.

It is apparent that achieving reasonable small-signal suppression over the designed limiting amplifier's whole frequency bandwidth and input dynamic range is a significant challenge that requires special attention during the initial design phase. With the saturated output power window and harmonic suppression being the main considerations of the limiting amplifier design, small-signal suppression was done merely for evaluation purposes. This evaluation, however, showed another significant shortcoming in the design. Nevertheless, the evaluation offered valuable insight as to the expected small-signal suppression offered by the designed limiting amplifier.

The question remaining at this stage is whether the BLA would offer sufficient small-signal suppression for use on the front-end of an IFM receiver. The answer to this question is dependent on the sensitivity specification of the IFM and the specification of the minimum signal separation to be presented to the limiting amplifier itself. The IFM will do accurate frequency measurement on a desired signal if all spurious signals are suppressed 9 dBc. This requirement must typically be adhered to for signal separations of ≥ 6 dB on the limiting amplifier input, independent of tone separations. The desired small-signal suppression specification will, therefore, be determined by the actual small-signal suppression required, to ensure the desired 9 dB signal separation at the output of the limiting amplifier. This statement is better explained by revisiting Table 6.2. In this table it was shown that the minimum small-signal *suppression* was measured as - 5 dB ($P_{desired}$ = - 20 dBm) at an input signal separation of 15 dB. This situation is depicted in Figure 6.37. It is seen that the initial 15 dB input signal separation has reduced to only 10 dB signal separation on the output of the BLA.

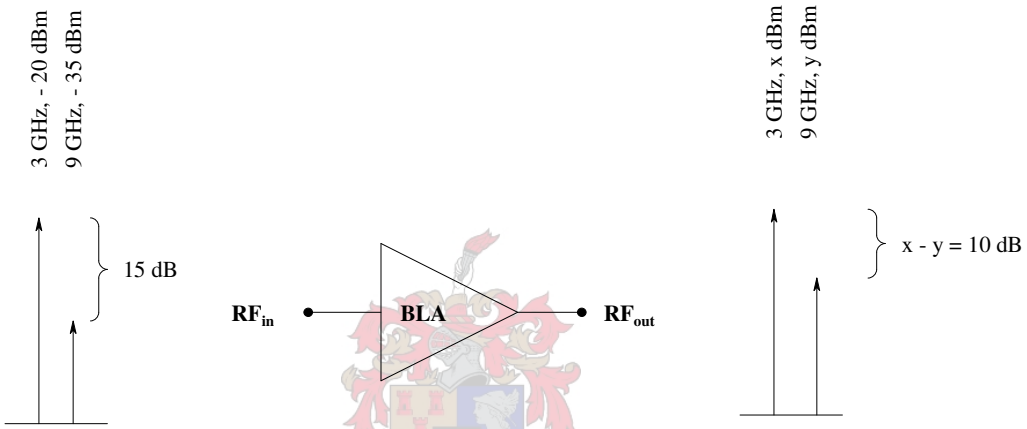


Figure 6.37: Evaluating desirable small-signal suppression

Even though the output signal separation deteriorated to 10 dB, the signal separation is still sufficient to allow for accurate frequency measurement by the IFM. On grounds of this discussion, deteriorated small-signal suppression may be allowed, but only if the IFM's measurement accuracy is not influenced.

6.6 CONCLUSION

In this chapter, a physical evaluation of the designed limiting amplifier was done. Measurements were used to validate the formulated design hypothesis but also showed the flaws in the design formulation. Satisfactory results were obtained, but also stressed the need for a more intensive design exercise. The physical evaluation offered better insight as to the actual operation of the limiting amplifier, while the mechanism of operation could be predicted to great extent from the simulated design. Simulations did therefore offer valuable insight as to what was physically expected from the designed limiting amplifier, but also stressed the need for more accurate nonlinear device models. In conclusion, the chapter to follow offers a critical review of the designed limiting amplifier while offering suggestions as to improvements on the design.

CHAPTER 7

CONCLUSION

7.1 INTRODUCTION

The aim of this concluding chapter is to give an overall summary of the study on the broadband limiting amplifier, to summarize some of the achievements during the course of the study and to critically evaluate the designed limiting amplifier for future reference. The linear amplifier versus the limiting amplifier is discussed and it is shown that the design approach for either component is requirement driven. In conclusion, further study is suggested on the intricacies of the limiting amplifier.

7.2 ACHIEVEMENTS

The aim of this study was the design and analysis of a broadband limiting amplifier. A successful design was completed that showed the extent to which a limiting amplifier, employing the attenuator-amplifier approach, was realizable. The design offered the unique opportunity to investigate the mechanism of operation of a microwave device that is a topic rather limited in discussion.

The fundamental knowledge required to attempt the design of a microwave limiting amplifier covers a wide variety of topics. Some of these topics are summarized shortly hereafter.

- Theoretical and practical background on the mechanism of operation of a broadband limiting amplifier had to be established and only from there could further requirements for its design be established.

- The fundamental aspect proved to be the RF amplifier design capability that had to be established for purposes of this study.

- The intricacies of the components used in RF amplifiers were evaluated to establish their influence on the device performance and was justified as a very important design consideration.

- Amplifier designs started off with the design of a 50 MHz single-stage amplifier and gradually became more complex while requiring the use of design packages namely *MultiMatch* and *Microwave Office*. These packages were used in conjunction with each other to form a powerful amplifier design and analysis tool. They were used successfully in the design of a first iteration single-stage broadband amplifier (2-18 GHz Gain Block) and the iteration on this design that was eventually used in the final limiting amplifier. The designed amplifiers allowed for evaluation of some of their prominent properties and set the stage for the evaluation of their associated nonlinear phenomena.

- In-depth nonlinear analysis, implementing *Microwave Office* followed with the reconstruction and analysis of an existing two-stage 2-18 GHz amplifier. The available nonlinear analysis (HB in particular) techniques offered the capability of simulating and characterizing a device such as the limiting amplifier, which is riddled with associated nonlinear phenomena.

- Another aspect that was focused upon was the design (or operation) of passive components. A range of passive components including couplers, attenuators, broadband splitters etc., were evaluated for the specific purpose of this study.

- The proposed design hypothesis as based on the *baseline* limiting amplifier design was tested and evaluated through simulation. A modular design approach, implementing a *backbone* limiting amplifier (BLA), was proposed, which then formed the focus for a final design.

- Manufacturing limitations and restrictions are of particular importance in industry, and therefore require careful consideration. This requires the use of both *AutoCad* and *Microwave Office* to ascertain a realizable implementation of the simulated design.

- The physical implemented design was tested and evaluated, and allowed for comparison with the simulated design. The critical design evaluation of this limiting amplifier is discussed in subsequent sections.

7.3 CRITICAL DESIGN EVALUATION

The section to follow offers a critical evaluation of the designed limiting amplifier and the design procedure that was followed to arrive at the final design. The shortcomings of the design are discussed and establish a starting point for further study on this topic.

7.3.1 RE-EVALUATION OF NONLINEAR DEVICE MODELLING

Apparent by now is the essence of accurate nonlinear device modelling. Analysis and design of a limiting amplifier can only be done accurately if the nonlinear device models provide an accurate prediction of device behaviour. With accurate nonlinear device models in place, one may much better characterize and predict the limiting amplifier's nonlinear behaviour. This would then also allow for refinements in future design hypotheses.

The existence of an accurate nonlinear device model should therefore be the first consideration when selecting a device to be used in a limiting amplifier design. The aim of this thesis was not to do a full validation of available nonlinear models. It is therefore important that any future studies should place more emphasis on this aspect than was done in this thesis. It was assumed that the nonlinear device models provided, were accurate and therefore the evaluation of these devices was very limited.

7.3.2 CUSTOMIZED AMPLIFIER DESIGN

The design approach that requires optimization of the harmonic response of a *small-signal* amplifier is a rugged approach that was attempted as the method to a means. Although this approach proved successful in the end, a more refined approach is suggested.

The use of load pulling was mentioned as an option for designing an amplifier with improved harmonic suppression but is a topic that requires further investigation. Also to be considered further, is the operating region of each of the amplifiers within the limiting amplifier chain. Knowing this will give better insights as to the required optimization constraints for each amplifier. Each of the amplifiers within the limiting amplifier RF chain should therefore be custom designed for its position within the chain to allow for the desired limiting amplifier response.

7.3.3 TEMPERATURE EVALUATION

Although not very evident from the designed limiting amplifier; temperature effects may seriously deteriorate device performance. For reasons explained previously, simulations performed did not consider temperature variations. Nonlinear device models that allow for accurate prediction of device behaviour over temperature should be used where available.

Temperature variable attenuators offer a viable means of implementing temperature compensation. The problems experienced with the proposed *thermopads* may be corrected by using a device with a higher frequency rating. It is believed that the device with a higher frequency rating will not have the associated drop-off at 18 GHz. Where the desired S-parameters for the device are not available, parameter extraction should be performed for better device characterization. A complete characterization of the device performance over temperature may be needed for eventual implementation in *Microwave Office*, as part of a limiting amplifier design.

7.3.4 RESULT EVALUATION

The measurements performed on the designed limiting amplifier showed the feasibility of the proposed attenuator-amplifier configuration as part of the overall design. The measured results are summarized in Table 7.1 for comparison with the initial laid down design specifications.

The frequency specification was easily achieved while offering the desired saturated output power window for the - 40 to + 5 dBm input dynamic range. The input return loss as measured for a - 10 dBm drive level was shown to be 7.5 dB. The deterioration of the input return loss as a function of input drive level has been pointed out and would suggest this to be an inherent property of a limiting amplifier implementing the attenuator-amplifier configuration. The extent to which this return loss degradation can be allowed will typically be a custom specification.

A reasonable output power window was achieved, that could ideally be improved upon if the drop in output power towards the higher frequencies could be corrected, without deterioration of the achieved harmonic suppression. Alternatively, slope correction could be done as part of the modular design approach to yield an eventual smaller output power window.

Specification	Achieved Result
Frequency Range	2-18 GHz
Input Return Loss @ P_{in} = - 10 dBm	7.5 dB
Input Dynamic Range	- 40 to + 5 dBm
Minimum Output Power @ P_{in} = - 40 dBm	> 5 dBm
Minimum Output Power @ P_{in} = + 5 dBm	> 5 dBm
Maximum Output Power Window @ P_{in} = + 5 dBm	< 4.3 dB
Harmonic Suppression @ P_{in} = - 40 dBm	> 8.4 dBc
Harmonic Suppression @ P_{in} = + 5 dBm	> 8.4 dBc
Operating Temperature Range	- 54 °C to + 85 °C

Table 7.1: Summary of achieved results for comparison with initial laid down specifications

In terms of the achieved harmonic suppression there is room for improvement. As previously suggested, an improvement may only be feasible if a trade-off between second and third harmonic suppression is allowed and if nonlinear analysis accurately predicts the levels of these harmonic products. Consideration must also be given to the fact that there will be a certain limit on the achievable harmonic suppression when considering the 2-18 GHz bandwidth and the input dynamic range in question. Any improvements achieved are predicted to be marginal. The 2-18 GHz bandwidth offers one with the challenge of dealing with a range of in-band harmonics while the large input dynamic range further complicates matters with respect to the different amplifier stages driven into saturation. A definite improvement in harmonic suppression (and other specifications) may be expected if the bandwidth and/or input dynamic range is decreased.

7.3.5 THE INFLUENCE OF LOAD VARIANCE ON ATTENUATORS

An aspect that was not taken into account is the effect of load variance on the attenuation characteristics of the T-attenuators used in the designed limiting amplifier. The T-attenuator that was designed for use in a 50 Ω system, is subjected to deviation from the ideal 50 Ω input/output loads. The result being that the attenuators themselves may deteriorate the desired limiting amplifier performance. An investigation was launched to find an improvement on the initial designed attenuator. The newly designed X-attenuator (star configuration) showed a considerable size reduction as well as a significant reduction in return loss. Intuitively one may reason that this X-attenuator may already be less sensitive to load variance. The design layout of this attenuator is shown in Figure 7.1 while Figure 7.2 shows the comparison between this design and the T-attenuator design that was used in the limiting amplifier.

Figure 7.2 shows that the X-attenuator offers an overall improved response when compared to that of the normal T-attenuator.

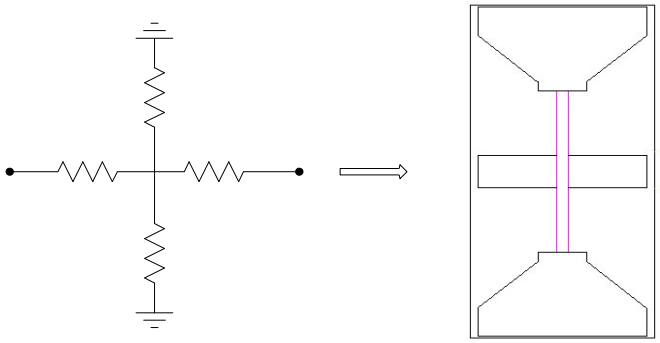


Figure 7.1: Newly designed X-attenuator

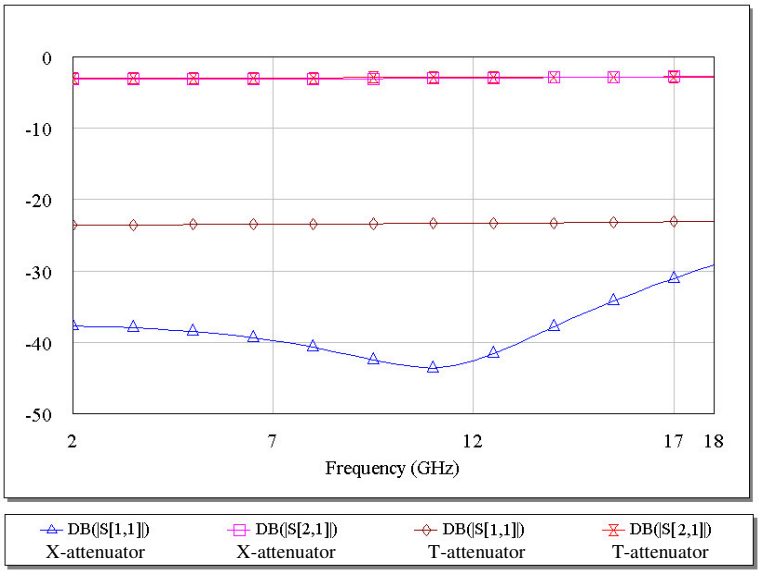


Figure 7.2: Comparison between a T-attenuator and an X-attenuator

7.3.6 OPTIMIZED TRANSITIONS

Another important aspect that needs mentioning is a compensation method allowing for optimum microstrip interconnects. The technique is tolerant of gap variations between substrates and of misalignment of microstrip conductors [33]. In the design that was done, it was assumed that the transitions between carrier plates were ideal, where this is not practically the case. Rather, one has to rely on manufacturing tolerances to determine how *smooth* these transitions will be. The proposed technique was only discovered after completion of the actual limiting amplifier design and was therefore not implemented. It should, however, be a definite consideration for an intended improved design. The configuration as proposed in [33], is given in Figure 7.3. The shown configuration is for 15 mil Alumina and offers a VSWR of better than 1.3 over the frequency range DC-20 GHz. The optimum length of the interconnecting wire bonds is 26 mil (± 1 mil) when using a proposed 1 mil wire diameter.

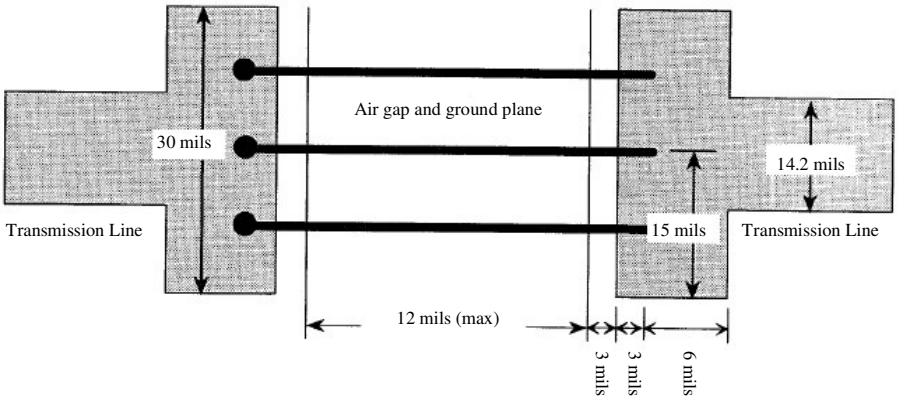


Figure 7.3: Proposed configuration for optimum microstrip interconnects

7.3.7 DUAL-GATE FETS FOR USE IN A LIMITING AMPLIFIER

Reasonable results were obtained with the *NEC* devices discussed in this text. Other devices may, however, provide for improved limiting amplifier response. Of particular interest is the dual-gate GaAs FET, which offers a viable option for use in wide-band output limiter circuits, that should eliminate most of the undesirable characteristics associated with normal FET limiting amplifiers, while providing improved limiting performance.

Dual-gate FETs offer several advantages over diode type limiters discussed earlier and single-gate FETs that are operated in a saturated mode. The dual-gate GaAs FET stage offers a sharp limiting *knee*, which is defined as the change in output power from the 1 dB gain compression point to the saturated output point [34].

One effect of the sharper *knee* region is to increase the available dynamic range of the limiting amplifier by lowering the input power level required to fully saturate the FET limiting module. With a broadened dynamic range, less overall amplifier gain and thus fewer gain stages are required. In essence, the dual-gate FET therefore allows for an improved *safe limiting region*.

The device also offers lower saturated output power for a given device physical size and inherently good pulse response with minimal overshoot. It also has a good degree of controllability of the saturated output power level, through the simple adjustment of DC bias levels [35].

A design, implementing a dual-gate FET (*MWT-5*) was attempted for purposes of this study. The design, however, was not implemented, due to the fact that accurate model fitting in *MultiMatch* could not be achieved. Even though further investigation of this device was not done, it offers a definite opportunity for improved limiting amplifier response, which requires further investigation.

7.3.8 AMPLIFIER OVERLOAD AND RECOVERY TIME

An aspect that was not taken into account for the discussed design was the effect of amplifier overload on recovery time with pulsed signals present at the limiting amplifier input. During amplifier overload, the input level which causes saturation will produce a maximum output level that will remain, until the input signal decays below this level [37]. Once the amplifier saturates, it takes some time to revert or *recover* to a non-saturated mode.

This aspect was omitted merely for the fact that it was not a consideration in the *baseline* limiting amplifier, where the associated recovery time did not deteriorate the IFM's frequency measurement capability. Depending on system requirements, this aspect may be a serious point of concern.

7.3.9 DESIGN CENTERING AND YIELD ANALYSIS

Other aspects that were not considered for the final limiting amplifier design were yield analysis and yield optimization. The yield analysis capabilities within MWO can be used to study the effects of statistical variations on circuit performance. MWO can be used to analyze the yield of a circuit for a given description of the statistical properties of the component values [38]. MWO also allows for design centering which entails yield optimization of a circuit by modifying the nominal values of specified parameters. This ability of MWO allows for a design that takes into consideration all the relevant component variances and manufacturing tolerances, while independent thereof, will still achieve the desired physical performance. This ability could be utilized for improved limiting amplifier designs.

7.4 THE LIMITING AMPLIFIER VERSUS THE LINEAR AMPLIFIER

One of the goals of this study was the formulation of the design differences between limiting amplifiers and linear amplifiers. Looking back at the course of the study it should, however, be apparent that such a formulation would offer a contradictory comparison between two very different components. Not only do they differ in terms of functionality but they also differ in terms of their regions of operation. The design approach for either component will therefore be requirement specific.

The linear amplifier did form the basis of the designed limiting amplifier, however. For a portion of the limiting amplifier's input dynamic range, the linear amplifiers as part of the limiting amplifier were operated within their respective linear regions. For the remaining portion of the limiting amplifier's input dynamic range, these amplifiers were operated within their respective *safe limiting regions*, as proposed in this thesis.

The difference being that the linear amplifier had to be optimized for operation in its nonlinear region while its nonlinear response could be predicted from ideally accurate device models. RF amplifiers used as part of a limiting amplifier are therefore custom designed for their position within the limiting amplifier RF chain, rather than just using uncharacterized gain blocks.

Ideally one would like a flawless recipe for designing a limiting amplifier, and the amplifiers that form its building blocks. This can, however, not be done after a single design iteration that was based on the proposed design configuration. The

study presented in this text serves as reference for future designs rather than setting the standard, while further in-depth study on this topic is proposed. The section to follow gives a short summary on the proposed field of further study.

7.5 FIELD OF FURTHER STUDY

The design study on limiting amplifiers will for the largest part, remain requirement specific while used for customized solutions in the field of electronic warfare. The design that was discussed in this text was also the result of a specific requirement that needed to be addressed.

Unlike RF amplifier design theory, which is well-documented, very little design theory exists for the limiting amplifier. Ideally, further study should establish the desired design theory or at least establish improved references for design, especially over the 2-18 GHz bandwidth.

The alternating limiter-amplifier design configuration does offer a viable option for realizing a limiting amplifier but will also offer considerable design challenges, especially over increased bandwidths. Notwithstanding this, the alternating limiter-amplifier configuration requires further investigation to eventually establish a qualitative comparison with the attenuator-amplifier design approach. An alternative design approach may then also present itself in a limiting amplifier configuration that implements both attenuators and limiters. Depending on the specific limiting amplifier requirements; there exist a number of unique solutions for implementing such a design.

7.6 CONCLUDING REMARKS

The design and analysis of a broadband limiting amplifier was successfully executed for purposes of this study while invaluable insight as to the operation of this device was established. The achieved results are typical of a limiting amplifier covering the 2-18 GHz frequency bandwidth and with the input dynamic range in question. Meeting the desired specifications was no mean feat and was complicated by the broad frequency bandwidth, the broad input dynamic range and the limiting amplifier's associated nonlinear phenomena. Few manufacturers succeed in producing limiting amplifiers with similar specifications; a fact that tends to show the complexity and intricacy associated with the design of this device. The result of this study, however, being a fully operational broadband limiting amplifier, realized after only a single design iteration, showed that the design of this device was mastered after thorough theoretical and practical research methodology.

In conclusion, the hope is expressed that this thesis will initiate further study on this topic to establish further insight into all the intricacies associated with the mechanism of operation of this unique device. The fact remains that for narrow-band designs the popular design approach is modular of nature while requiring the use of alternating limiters and amplifiers as part of the different gain modules. The most popular design approach for broadband limiting amplifiers, however, is still eagerly sought after.

A man with hands in his hair is frustrated today, but enlightened tomorrow…

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APPENDIX A

DERIVATION OF THE BANDPASS LIMITER OUTPUT EXPRESSION

A mathematical expression for the output of a bandpass limiter can be derived by assuming that the input to the BPL is given by ([4], [5]):

$$x(t) = A_{desired}\cos(2\pi f_1 t) + A_{undesired}\cos(2\pi f_2 t) = A_{desired}\cos(\omega_1 t) + A_{undesired}\cos(\omega_2 t) \quad \text{(A.1)}$$

with $A_{desired}$ and $A_{undesired}$ being the amplitudes of a high-level desired signal and an undesired low-level interference signal respectively. Setting $\omega_1 = \omega_c$ and $\omega_2 = \omega_c + \omega_i$ yields a new expression:

$$x(t) = A_{desired}\cos(\omega_c t) + A_{undesired}\cos(\omega_c + \omega_i)t \quad \text{(A.2)}$$

The expression for the envelope of this input signal is determined from the phasor diagram shown in Figure A.1, where $\theta(t) = \omega_i t$ is the relative phase between the desired signal and the undesired signal.

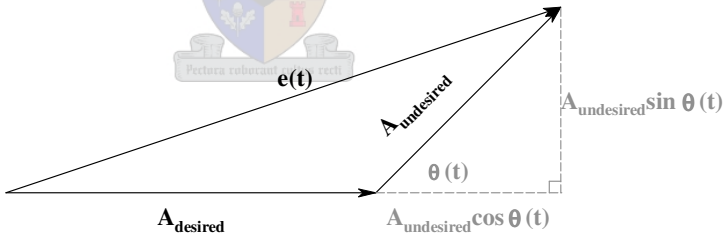


Figure A.1: Phasor diagram for derivation of envelope expression

The input envelope *e(t)* is a non-negative real quantity, being the length of the hypotenuse of a right triangle whose base is $A_{desired} + A_{undesired}\cos\omega_i t$ and whose height is $A_{undesired}\sin\omega_i t$, [6].

Thus,

$$e(t) = \sqrt{(A_{desired} + A_{undesired}\cos\omega_i t)^2 + (A_{undesired}\sin\omega_i t)^2} \quad \text{(A.3)}$$

Expression (A.3) can be further expanded to give:

$$e(t) = \sqrt{(A_{desired})^2 + (2A_{desired}A_{undesired}\cos\omega_i t) + (A_{undesired}\cos\omega_i t)^2 + (A_{undesired})^2(\sin\omega_i t)^2}$$

$$= \sqrt{(A_{desired})^2 + (2A_{desired}A_{undesired}\cos\omega_i t) + (A_{undesired})^2(\cos\omega_i t)^2 + (A_{undesired})^2(\sin\omega_i t)^2}$$

$$= \sqrt{(A_{desired})^2 + (2A_{desired}A_{undesired}\cos\omega_i t) + (A_{undesired})^2} \qquad \text{(A.4)}$$

To simplify the discussion, the value of $A_{desired}$ is assigned a value of unity and expression (A.4) then becomes:

$$e(t) = \sqrt{1 + (2A_{undesired}\cos\omega_i t) + (A_{undesired})^2} \qquad \text{(A.5)}$$

Using the *Maclaurin* series expansion:

$$\frac{1}{\sqrt{1+x}} = 1 - \frac{x}{2} + \frac{3x^2}{8} - \frac{x^3}{16} + \ldots \qquad \text{(A.6)}$$

the inverse of *e(t)* can be written as:

$$\frac{1}{e(t)} = 1 - \frac{(2A_{undesired}\cos\omega_i t) + (A_{undesired})^2}{2} + \frac{3\left[(2A_{undesired}\cos\omega_i t) + (A_{undesired})^2\right]^2}{8} - \ldots \qquad \text{(A.7)}$$

where $x = (2A_{undesired}\cos\omega_i t) + (A_{undesired})^2$

Expression (A.7) can now be further simplified if taken into account that the interference signal is small compared to the unity amplitude of the wanted signal. The result is as follows:

$$\frac{1}{e(t)} = 1 - A_{undesired}\cos\omega_i t + \ldots \qquad \text{(A.8)}$$

The actual limiter output *r(t),* is defined as $\frac{x(t)}{e(t)}$, thus

$$r(t) = \frac{x(t)}{e(t)} = (\cos(\omega_c t) + A_{undesired}\cos(\omega_c + \omega_i)t)(1 - A_{undesired}\cos\omega_i t)$$

$$= \cos(\omega_c t) + A_{undesired}\cos(\omega_c + \omega_i)t - A_{undesired}\cos(\omega_c t)\cos(\omega_i t) - (A_{undesired})^2\cos(\omega_i t)\cos((\omega_c + \omega_i)t) \qquad \text{(A.9)}$$

Dropping the higher order term yields the desired result after some mathematical manipulation.

$$r(t) = \cos(\omega_c t) - \frac{A_{undesired}}{2}\cos(\omega_c - \omega_i)t + \frac{A_{undesired}}{2}\cos(\omega_c + \omega_i)t \qquad \text{(A.10)}$$

Finally, expression (A.10) is written in terms of ω_1 and ω_2 as

$$r(t) = \cos(\omega_1 t) - \frac{A_{undesired}}{2}\cos(2\omega_1 - \omega_2)t + \frac{A_{undesired}}{2}\cos(\omega_2 t) \quad \text{(A.11)}$$

APPENDIX B

RF AMPLIFIER DESIGN EXAMPLES

B.1 INTRODUCTION

Discussed in this appendix are two designs that were done for purposes of this study. The designs include a 50 MHz amplifier designed for maximum gain and a 3.6-4.3 GHz low-noise amplifier. The designs were done in order of difficulty showing progressive design capability as well as increased confidence gained in the available amplifier design tools.

B.2 50 MHz AMPLIFIER DESIGNED FOR MAXIMUM GAIN

The design and implementation of a single-stage 50 MHz amplifier using the 2N3819 N-channel JFET is discussed hereafter. This design, unlike the other design example to follow, is discussed in somewhat detail.

B.2.1 S-PARAMETER MEASUREMENTS

No S-parameters were available for the 2N3819 and were therefore determined by actual measurement on a vector network analyzer. If not measured, S-parameters may be extracted from the amplifier configuration implementing the relevant transistor model, in a design package such as MWO. This is, however, only suggested if one is confident that the model gives a good representation of the actual device performance. The evaluation board that was built up for physical S-parameter measurements is shown in Figure B.1. It was built on 1.2 mm thick FR04 PCB material, with a copper plated ground plane. Actual 50 Ω transmission lines were implemented by using conductive copper tape with approximate width of 2.22 mm. The actual length of these transmission lines was not an important consideration since the physical dimensions of the circuit is very small compared to a $\lambda/4$ of the design frequency.

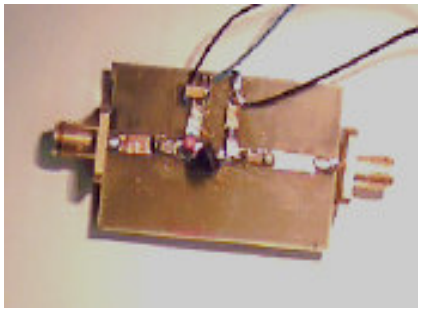


Figure B.1: Evaluation board for S-parameter measurements

The electrical diagram of the evaluation board is shown in Figure B.2.

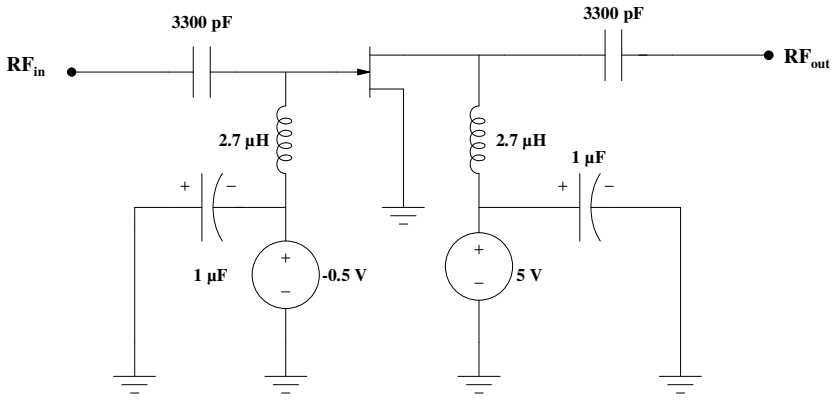


Figure B.2: Electrical diagram of the evaluation board

Measurement equipment such as network analyzers is very sensitive to DC and may be damaged when it is applied to measurement ports. DC blocking capacitors are thus needed at the input and output ports of the shown configuration before measurements are done. These DC blocking capacitors should represent an RF short so as not to affect either the insertion loss or the VSWR of the amplifier configuration. The blocking capacitors must be free of parasitic resonance up to at least the highest operating frequency. As a *rule of thumb*, the capacitive reactance must be at least 1 Ω at the operating frequency.

Thus,

$$X_C = \frac{1}{\omega C} = 1\ \Omega \tag{B.1}$$

The capacitance is then determined as:

$$C = \frac{1}{\omega} = \frac{1}{2\pi f} = \frac{1}{2\pi(50\times10^6)} = 3183.1\ pF \tag{B.2}$$

3300 pF capacitors were used on the actual evaluation board. The inductors, which form part of the bias injection circuit isolate RF signals from the power supply and should ideally not influence the propagation of the RF signal. The impedance of the inductor should thus be much greater than the characteristic impedance of the transmission line. As a *rule of thumb*, the reactance of such a bias coil must equal at least ten times the characteristic impedance.

Thus,

$$\omega L = 10Z_0 \tag{B.3}$$

The value of the bias coils can thus be determined as follows:

$$L = \frac{10Z_0}{\omega} = \frac{10Z_0}{2\pi f} = \frac{10(50)}{2\pi(50\times10^6)} = 1.6\ \mu H \tag{B.4}$$

The 2.7 μH inductor that was used on the actual evaluation board was freely available and would offer increased impedance. Use of bypass capacitors at the connections to the DC supplies is advised to prevent unwanted coupling to circuits external to the amplifier.

B.2.2 DEVICE STABILIZATION

The actual measured S-parameters are as follows:

$$S = \begin{bmatrix} 0.9919\angle -5.4537° & 0.0449\angle 87.4632° \\ 0.3290\angle -11.6001° & 0.9908\angle -1.6785° \end{bmatrix} \tag{B.5}$$

For the amplifier to be unconditionally stable, the stability factor K must be larger than unity, thus

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{B.6}$$

and

$|\Delta| < 1$ must hold true, (B.7)

where

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{B.8}$$

The measured S-parameters as given in (B.5) are substituted into equations (B.7) and (B.8) to get:

$$K = -0.1 \tag{B.9}$$

and

$$|\Delta| = 0.98 \tag{B.10}$$

The amplifier is thus not unconditionally stable and will have to be stabilized before commencing with the design. Shown in Figure B.3 is the stabilized device with input and output shunt stabilizing resistors, with values chosen to achieve a trade-off between actual stability and maximum available gain. No consideration to noise figure was given in this case. The plot of the input and output stability circles confirmed that the regions of instability are not included in the Smith-chart.

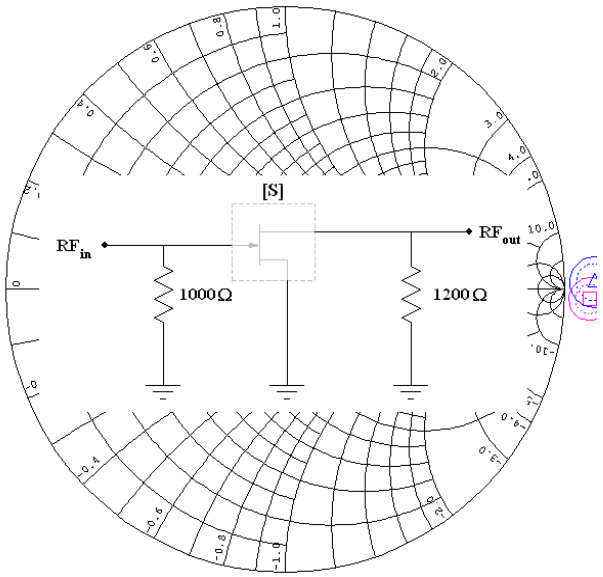


Figure B.3: Stability circles of stabilized device

The new set of S-parameters of the stabilized device is given by:

$$S = \begin{bmatrix} 0.89758\angle -5.4865° & 0.041072\angle 87.625° \\ 0.30095\angle -11.438° & 0.91147\angle -1.707° \end{bmatrix} \tag{B.11}$$

With $K = 1.24$ and $|\Delta| = 0.82$ unconditional stability is further confirmed. Similarly, unconditional stability was confirmed at frequencies close to the design frequency. After the stability of the device has been determined, the input and output matching sections can be designed.

B.2.3 DESIGN OF THE MATCHING NETWORKS

With a design goal of maximum gain in mind, the matching networks must provide a conjugate match between the amplifier source or load and the device itself. Maximum power transfer from the input matching network to the device will occur when:

$$\Gamma_{in} = \Gamma_S^* \tag{B.12}$$

with maximum power transfer from the device to the output matching network occurring when:

$$\Gamma_{out} = \Gamma_L^* \tag{B.13}$$

with Γ_{in}, Γ_{out}, Γ_S and $\Gamma_{L,}$ the input, output, source and load reflection coefficients respectively. The source reflection coefficient is determined from:

$$\Gamma_S = \frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2C_1} \tag{B.14}$$

with variables B_1 and C_1 defined as

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \tag{B.15}$$

and

$$C_1 = S_{11} - \Delta S_{22}^* \tag{B.16}$$

Similarly, the load reflection coefficient is determined from

$$\Gamma_L = \frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2C_2} \tag{B.17}$$

with variables B_2 and C_2 defined as

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 \tag{B.18}$$

and

$$C_2 = S_{22} - \Delta S_{11}^* \tag{B.19}$$

Using equations (B.12), (B.13), (B.14) and (B.17) the input and output reflection coefficients are determined as $\Gamma_{in} = 0.94\angle -1.31°$ and $\Gamma_{out} = 0.95\angle 1.83°$.

The input reflection coefficient is indicated as A on the Smith-chart shown hereafter in Figure B.4. The normalized impedance represented by this point is converted to a normalized admittance, indicated by point B. The normalized admittance at point B is (0.03 + j0.01) S. Moving on a constant conductance line takes us to point C, which intersects the unity circle on the admittance grid. The normalized admittance at point C is (0.03 - j0.17) S. A susceptance of (- j0.18) S thus needs to be added to the admittance at point B to change the admittance to that at point C. This negative susceptance corresponds to a shunt inductor.

Since the normalized inductive impedance is defined as:

$$z_L = \frac{j\omega L}{50} \ \Omega \tag{B.20}$$

the corresponding normalized admittance will be:

$$y_L = \frac{50}{j\omega L} \ S \tag{B.21}$$

The actual value of the shunt inductor can then be determined from:

$$\frac{50}{j\omega L} = -j0.18 \tag{B.22}$$

thus

$$L = \frac{50}{0.18\omega} = \frac{50}{0.18(2\pi f)} = \frac{50}{0.18(2\pi(50\times10^6))} = 884.19 \ nH \tag{B.23}$$

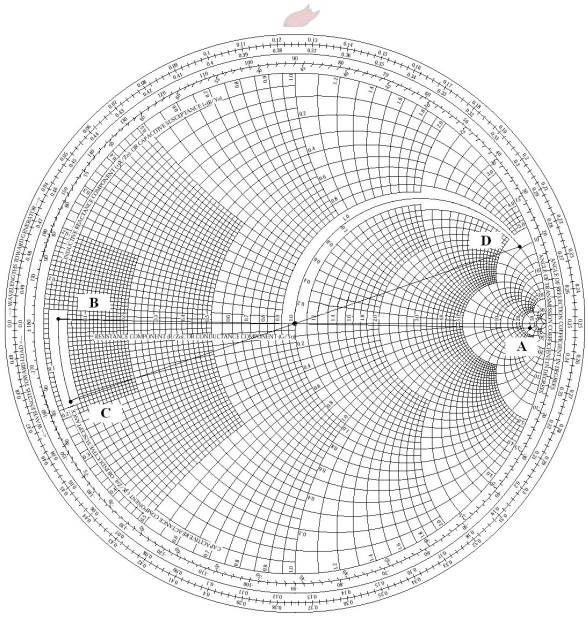


Figure B.4: Design of input matching network using the Smith-chart

Point C is converted back to the impedance (1 + j5.70) Ω, represented by point D. Adding a (- j5.70) Ω impedance to the impedance represented by D, will take us to the centre of the Smith chart, i.e. a proper conjugate match. The negative impedance that needs to be added corresponds to a series capacitor.

Since the normalized capacitive impedance is defined as:

$$z_C = \frac{\frac{1}{j\omega C}}{50} \ \Omega \tag{B.24}$$

The actual value of the series capacitor can then be determined from:

$$-j\frac{1}{50\omega C} = -j5.7 \tag{B.25}$$

thus

$$C = \frac{1}{5.7(50)\omega} = \frac{1}{5.7(50)(2\pi f)} = \frac{1}{5.7(50)(2\pi(50\times10^6))} = 11.17\ pF \tag{B.26}$$

The amplifier configuration with the input matching section included is shown in Figure B.5.

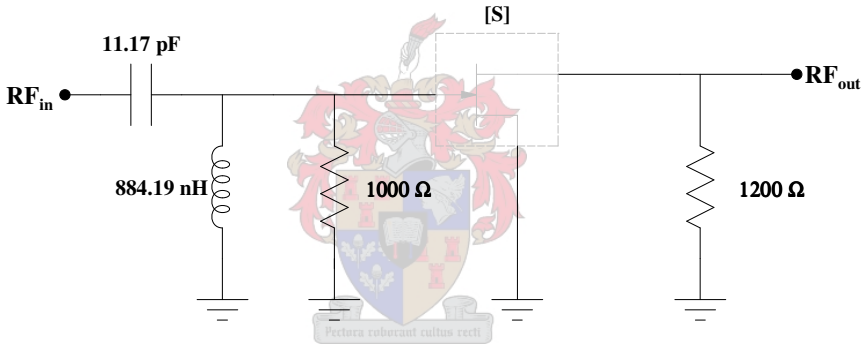


Figure B.5: Amplifier configuration with input matching network included

In a similar fashion as was discussed previously, the output matching network can be designed. The completed amplifier, without bias circuitry is shown in Figure B.6.

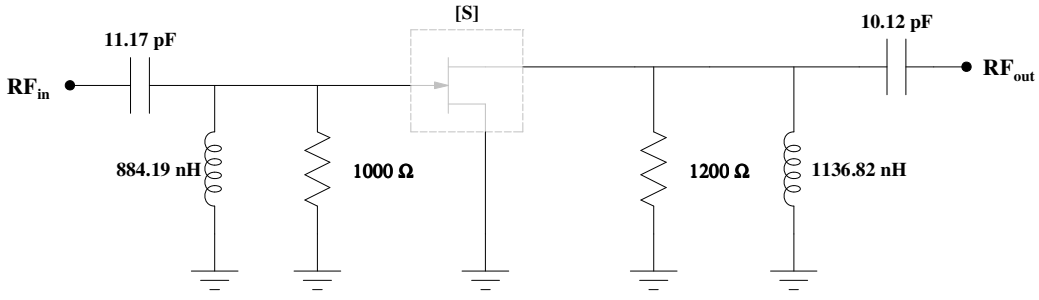


Figure B.6: Stable 50 MHz amplifier with input and output matching networks shown

With Γ_{in} and Γ_{out} known, the expected maximum transducer gain, in dB, can be determined from

$$G_T = 10log[\, G_S G_0 G_L \,] = 10log\left[\left(\frac{1}{1-|\Gamma_S|^2}\right)\left(|S_{21}|^2\right)\left(\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2}\right)\right] \tag{B.27}$$

A value of 5.68 dB for the maximum transducer gain is determined after substitution of relevant parameters into the shown equation. Although not spectacular, the gain will be sufficient for experimentation purposes.

B.2.4 SIMULATED RESPONSE

Shown in Figure B.7 is the simulated response of the designed amplifier. The maximum gain is 5.68 dB, as expected from calculations. A proper conjugate match was achieved, with the input and output return loss being a minimum at the design frequency.

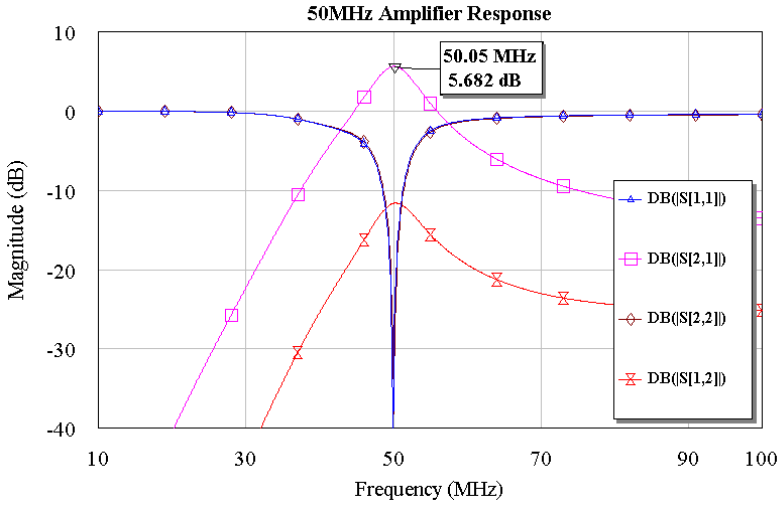


Figure B.7: Simulated response of the 50 MHz amplifier.

Shown in Figure B.8 are the input and output reflection coefficients of the designed amplifier plotted from 40 MHz to 60 MHz. The plotted response crosses the Smith-chart centre at the design frequency of 50 MHz as expected.

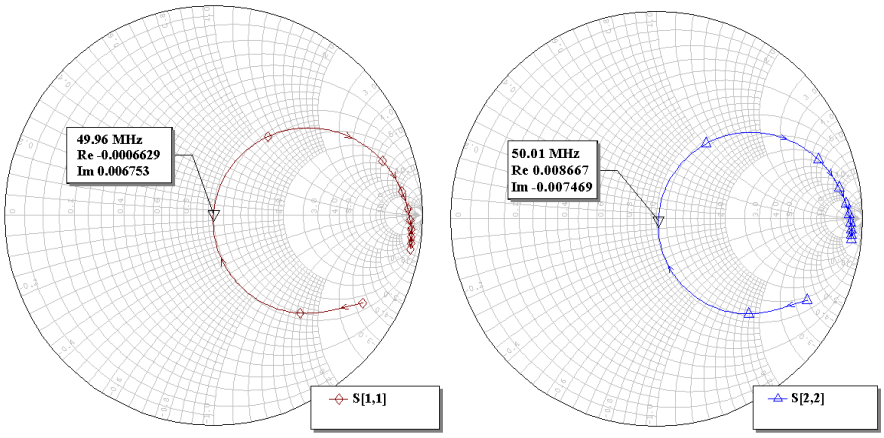


Figure B.8: Input and output reflection coefficient response of designed amplifier

The simulated results of the designed amplifier are as predicted by theory. The question that arises at this stage is how well the simulated results will correspond to actual measurements and simulations implementing a model of the transistor in question. Figure B.9 shows a comparison of the previously shown gain response with that of the designed amplifier, as implemented in *SPICE*. The only difference being that the implementation of the amplifier in *SPICE* did not include losses, parasitics etc. associated with the evaluation board used for S-parameter measurement. This may then also be the reason for the seen deviation in responses.

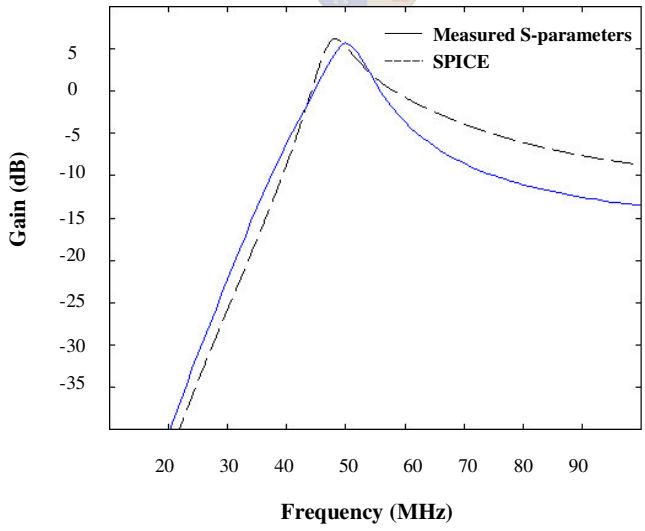


Figure B.9: Gain response comparison of amplifier implemented in SPICE and amplifier designed from measured S-parameters

The *SPICE* circuit used to get the shown simulated result is shown in Figure B.10. The amplifier is excited by an AC source with a 50 Ω internal resistance. An AC sweep was done to get the output voltage response over frequency, as measured over the 50 Ω load resistor.

The actual gain in dB's, as shown in the previous figure, is determined from:

$$Gain = 20\log\left(\frac{V_{out}}{V_{in}}\right) \tag{B.28}$$

where V_{in} and V_{out} are the amplitudes of the input and output signals respectively.

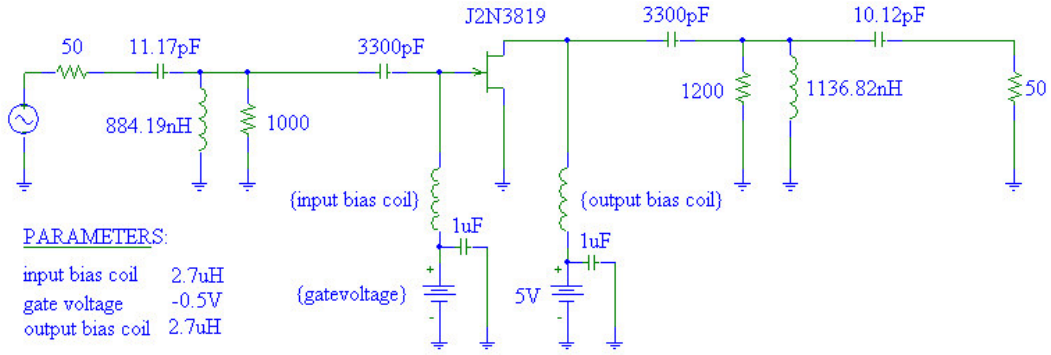


Figure B.10: SPICE circuit implementation of the designed amplifier

To gain more confidence in the model for the 2N3819, the circuit configuration shown before was implemented and simulated in *Microwave Office* in order to show the correlation between *SPICE* and *Microwave Office*. The SJFET (*SPICE* JFET) model of *Microwave Office* was used for simulations. This model uses a few extra parameters, necessary for many RF applications, which are not part of the *SPICE* parameter set. Using this model is thus not just a question of inserting the parameters as obtained from the *SPICE* model. The extra parameters mentioned had to be optimized to at least correlate with the *SPICE* model. Shown in Figure B.11 is the gain response of the designed amplifier as simulated in both *Microwave Office* and *SPICE*. A close correlation in simulated results can be seen.

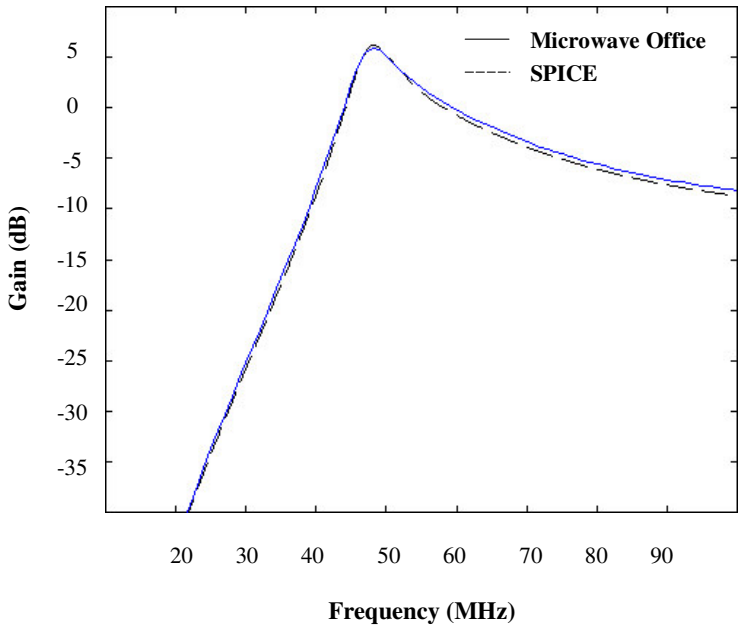


Figure B.11: Simulated amplifier response as done in both SPICE and Microwave Office

B.2.5 MEASURED RESULTS

Shown in Figure B.12 is the actual built 50 MHz amplifier.

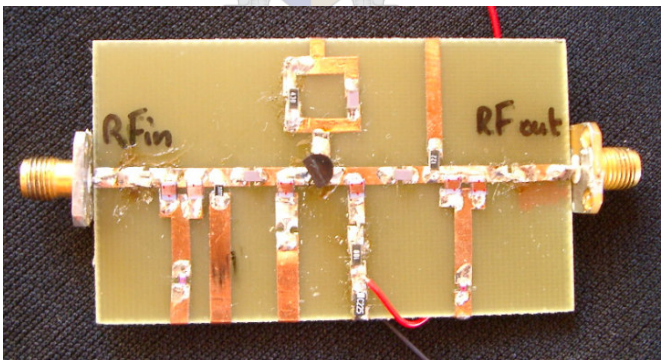


Figure B.12: Actual built 50 MHz amplifier

Figure B.13 shows the actual measured response. Comparing the measured response with the simulated response, one can see a very close relation between the results. From the measured response it is seen that there is a slight offset in the frequency where maximum gain occurs. It was seen that this design was very sensitive to even slight variations in the actual values of the impedance matching components. Despite this, the design was successfully implemented, after going through a complete *manual* design process.

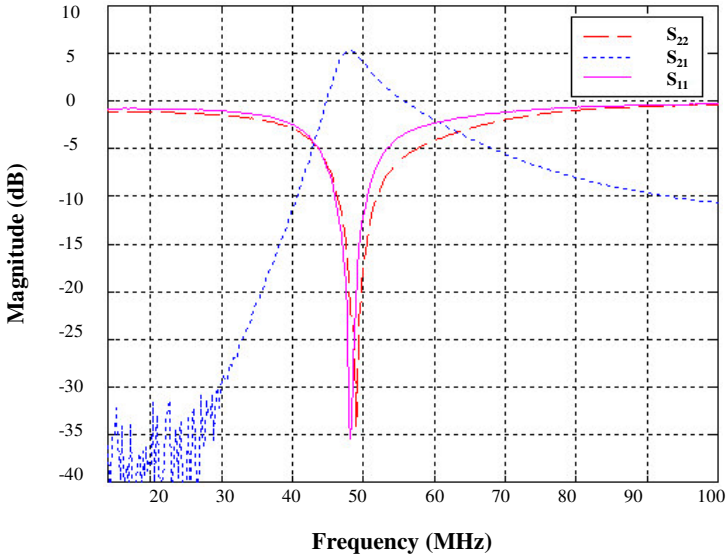


Figure B.13: Actual measured gain response

B.3 LOW-NOISE AMPLIFIER DESIGN: 3.6-4.3 GHz

A narrow-band LNA design is discussed hereafter. The design example serves to show the relevant design procedure making specific use of *MultiMatch*. Measured results are compared with simulated results to ascertain how suitable *MultiMatch* is for RF amplifier design. The specifications for the low-noise amplifier design were as follows:

Frequency range: 3.6 - 4.3 GHz

Gain Flatness: ± 0.5 dB

Gain: 9 dB (min.)

Noise Figure: 1.5 dB (max.)

Input VSWR: 2:1

B.3.1 MULTIMATCH DESIGN PROCEDURE

The *MultiMatch* design procedure that was followed to realize the specified low-noise amplifier design is summarized hereafter. Firstly a device is chosen to ensure that the set specifications can be achieved. The NEC NE32484A HJFET with a typical noise figure specified as 0.6 dB was chosen. G_a (typical) for this device was specified as 11 dB. *MultiMatch* is entered and the necessary setup-routine is completed. Model fitting is done to fit the S-parameter model for the transistor to the FET model as specified in *MultiMatch*. Device modification is then done to get the transistor stable and to improve input and output VSWR's. For low-noise designs the modification is usually done on the output of the amplifier so that the noise figure is not influenced. The matching networks are then designed. The reflection coefficients are selected as follows:

$\Gamma_S = \Gamma_{opt}$ and $\Gamma_L = \Gamma_{out}^*$. Γ_{opt} in this case may vary from what is actually specified for the device because a different noise figure than F_{min} may be required to achieve a certain VSWR or gain. With the matching networks in place, the amplifier is optimized and the artwork layout is finalized.

B.3.2 THE DESIGNED LOW-NOISE AMPLIFIER

The actual designed low-noise amplifier is shown in Figure B.14. Shown in Figure B.15 is the implementation of the passive bias network that was used. The transistor used was a leaded surface mount device. With these types of FET's the leads should be as short as possible to reduce unwanted parasitics. For operation within the specified design bandwidth, this packaging was sufficient.

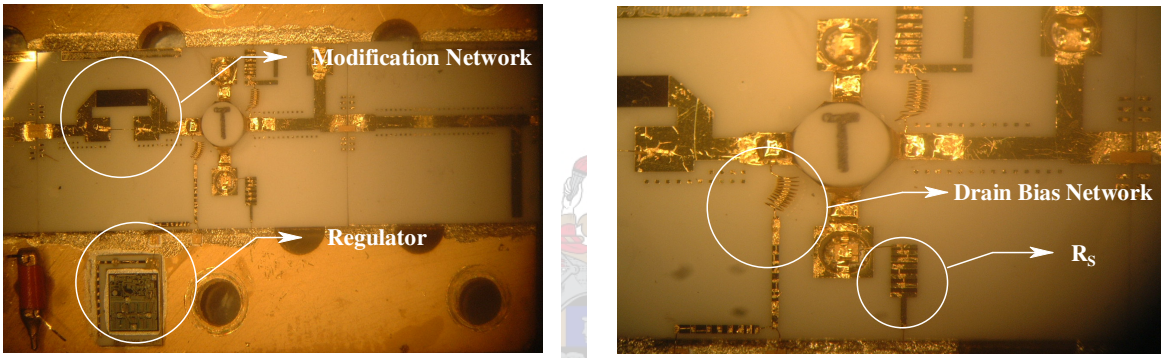


Figure B.14: Actual designed low-noise amplifier

A proper RF ground is obtained with via holes through the substrate. These are not pure through-hole-plated vias. The connection to ground is made via 100 pF chip capacitors. These capacitors also serve as decoupling caps for the DC present on the FET's source leads. Proper grounding of these source leads proved to be very crucial. It was shown that improper grounding leads to deterioration in the gain response. For the same reason, proper bonding of transistor leads to the microstrip transmission lines is also of great importance.

The gate is grounded with a 12-turn inductor (24 nH). The impedance of this inductor was chosen high enough so as not to influence the RF response of the amplifier. A resistive network in series with this inductor was included to increase the impedance if necessary. A 12-turn inductor was also used on the drain for DC bias application.

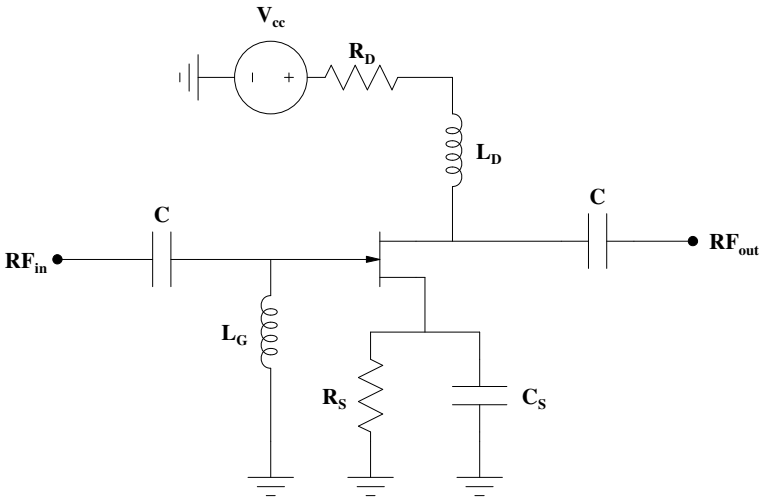


Figure B.15: Passive bias configuration used for the low-noise amplifier

B.3.3 MEASURED RESULTS

Shown in Figure B.16 is a plot of the gain and input return loss of the designed amplifier. The reference level for both S_{11} and S_{21} is 0 dB. The scale is 10 dB per division. The minimum gain was measured at 9.64 dB, the gain ripple measured at ± 0.15 dB and the maximum VSWR was measured at 1.91 (better than the design specification).

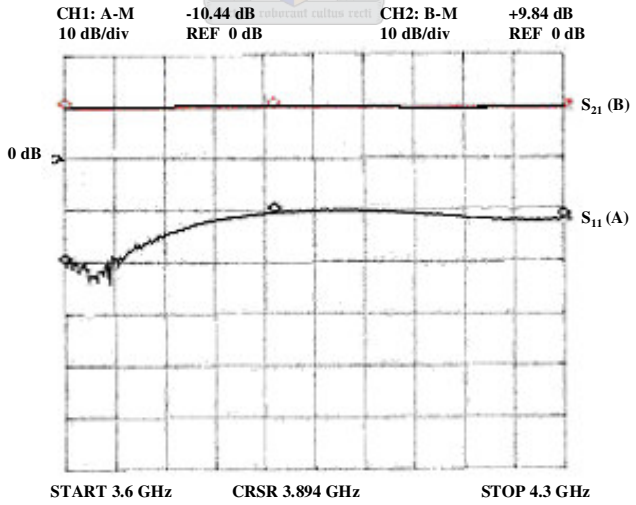


Figure B.16: Measured response of designed LNA

Figure B.17 shows the designed amplifier response as obtained with *MultiMatch*. Comparing the simulated results with the measured results, it can be seen to what extent *MultiMatch* could be used to do a practical amplifier design. There is seen to

be a close comparison between the two sets of results with the largest deviation being the sloped gain response of the simulated design.

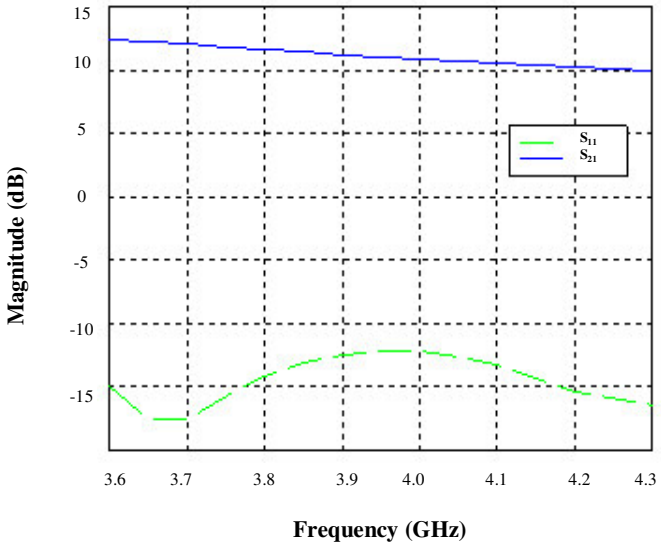


Figure B.17: Simulated response as obtained with MultiMatch

Table B.1 gives a summary of results as measured over temperature. From this summary one can already start to get a feel for an RF amplifier's response over temperature and to distinguish how measurements may vary with temperature.

Temperature	**- 20 °C**	**25 °C**	**65 °C**
Gain (dB)	9.78	9.64	9.49
VSWR	2.00	1.91	1.92
Ripple (dB)	± 0.24	± 0.15	± 0.27

Table B.1: Summary of results for designed low-noise amplifier

Figure B.18 shows the measured and designed noise figure response. The noise figure does not comply with the design specification over the whole band; the reason for this probably being that the actual bias point was higher than what was used in simulations.

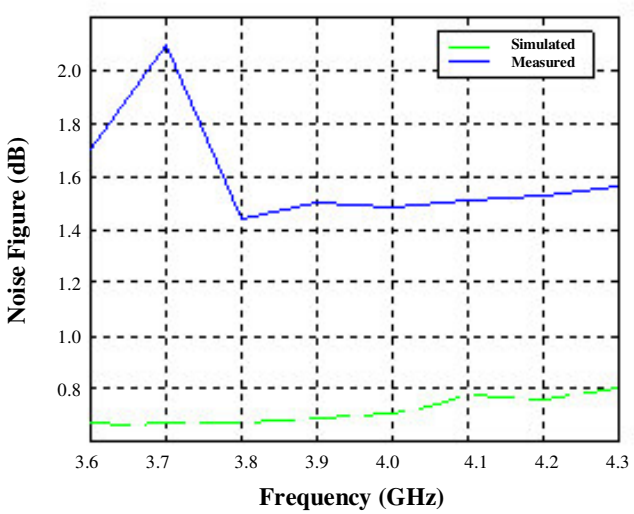


Figure B.18: Measured and simulated noise figure response

B.4 CONCLUSION

The narrow-band designs that were discussed in this appendix offered valuable practical experience in the design of RF amplifiers. These designs required application of theoretical knowledge gained during the course of this study while showing the correlation between theory, simulations and actual measured results. These initial designs offered the opportunity to familiarize oneself with the available design software, while increased confidence in the design software set the stage for attempting a broadband RF amplifier design.

APPENDIX C

DESIGN PROCEDURE: SINGLE-STAGE 2-18 GHz AMPLIFIER

C.1 INTRODUCTION

The *MultiMatch* design procedure that was followed to realize a single-stage 2-18 GHz amplifier is discussed in this appendix. The aim of this discussion is to give insight into the use of this program in the design of amplifiers. Even though the theory behind the program is well-documented in [23], the summary to follow offers useful information on the iterative design process required for realizing the desired RF amplifier. The summary was also intentionally written to allow for reconstruction of the discussed design. A very good theoretical background on RF amplifier design, however, is of the utmost importance if this program is to be used at full potential.

C.2 SETUP

When entering the program, the main menu is shown.

- Main menu: The option to synthesize an amplifier is chosen. This option allows for the design of an amplifier of which the output power can be controlled and for which the noise figure is not as important as the output power. When an amplifier is synthesized, each stage is synthesized sequentially, starting either from the load or source side.

- Project directory: The next window gives the option to change the project directory. The default project directory used is C:\AMPSAMM\MMEXA32. By default, this project directory is not changed.

- Amplifier stages: The number of stages to be used in the amplifier can now be specified. This design is for a single-stage amplifier. The choice under this menu is made accordingly.

- Amplifier name: Insert the new amplifier's name. The design will be saved as type *.ani.

- Amplifier pass band: Only a single pass band (2-18 GHz) is used.

- Amplifier stop band: Zero stop bands are chosen.

- Amplifier pass band: Specify the lower edge (2 GHz) and the higher edge (18 GHz) of the pass band.

- Synthesis direction: For the synthesis of a power amplifier, the design must be done from the load side towards the input side.

- Amplifier terminations: Both the source and load terminations are constant and resistive (50 Ω).

- Amplifier synthesis menu: Specify/modify the transistor for the current stage. Enter the name of the circuit file to be opened or to be created. The DOS file search string will typically look as follows: C:\AMPSAMM\MMDAT32*.SPI. In this directory the specific transistor (N32400AA.SPI) to be used, is chosen.

- Transistor parameters fitting option: Fit with a small-signal GaAs FET model. The GaAs FET model that is used by *MultiMatch* is shown in Figure C.1. *MultiMatch* uses a specific transistor model and modifies the parasitic and lumped elements included in the model, in order to fit S-parameters obtained from this model to the S-parameters as measured (shown on data sheet).

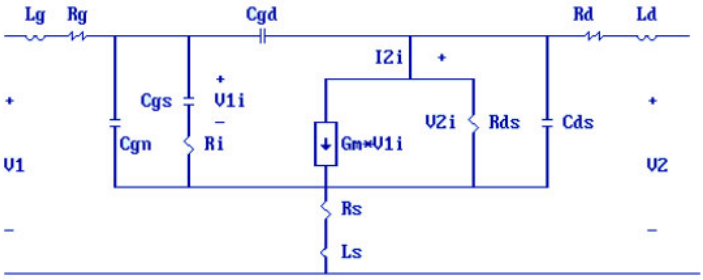


Figure C.1: Basic GaAs FET model

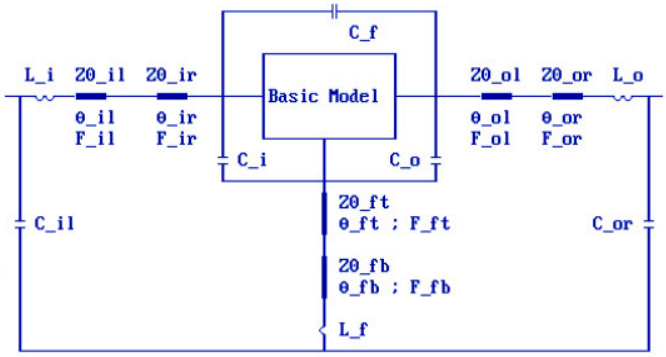


Figure C.2: Transistor package parasitics

- Model extraction option: Use the existing model to initialize model parameters and bypass viewing, editing and optimization. If needed to view/edit or optimize the model components, it can be done at this stage. Optimize only if necessary. Different results may be obtained with the different error functions and parameters to be chosen. The best results were obtained with the *L1* error function used together with S-parameters. An example of the NE32400 *.mdl file is shown hereafter. This file gives the different parasitics included in the transistor. The typical parasitics are shown in the GaAs FET model seen previously. Usually the *MultiMatch* models are good enough to be fitted to the S-

parameter data for a specific transistor. That is why it is suggested to use the existing model as is. Optimization may be done, but sometimes one may alter the existing model to such an extent that obtained results are just not acceptable.

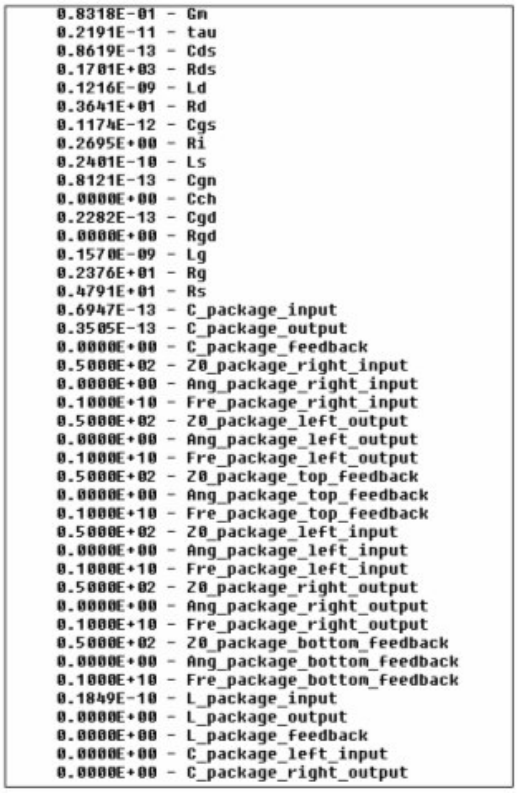


Figure C.3: Model file for the transistor in question

It might happen that for some reason the specific *MultiMatch* model is not good enough and that even optimization does not achieve a good fit. It must be remembered that the model file is also changed when optimization is done. The question remains on what is to be done if a good model cannot be found. The best solution is to make use of MWO's optimization features. Firstly the normal S-parameter model for the transistor in question is imported into MWO and the necessary S-parameter plots are done.

In the same schematic window an estimate transistor model, including parasitics is drawn. Biasing must be included. Variables for optimization on this transistor model are chosen and the optimizer goals are set. The idea is obviously to get the S-parameters of this model as close as possible to the imported S-parameter model. The S-parameters for the two models (S-parameter and transistor) are plotted on the same graph. Optimization is done until satisfactory results are obtained. The variable values can now be used in the model file. These values of the variables should be a very close approximation of the desired transistor model. Any further optimization can be done with *MultiMatch* itself.

- Input section: Before choosing any of the options under this menu, first press F5 to graphically see how accurate the transistor model was fitted to the measured S-parameters. A typical plot of this response is seen on the Smith-chart as seen in Figure C.4. If the fit is not satisfactory, press Alt+F9 to return to the transistor parameters fitting option and

redo the model fitting. Model fitting with the different error functions and parameters are repeated until satisfactory results are obtained.

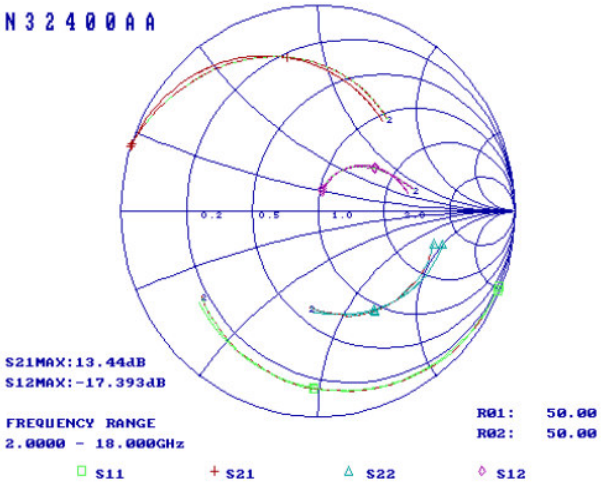


Figure C.4: S-parameters of transistor together with the S-parameters of the fitted model

- Input section: Enter or modify S-parameters. Make certain that there are enough S-parameter points to cover the whole pass band. Use F2 to insert new points and F1 to interpolate.

- Input section: Enter or modify the noise parameters. Usually one does not have to change anything here. Just check that there are enough points to cover the pass band and that the noise parameters are realistic. Correlate the given noise parameters with that given in data sheets. The following parameters are needed:

  F_{min} - Optimum noise figure in dB's.

  Γ_{opt} - Optimum noise reflection coefficient. The magnitude and angle needs to be specified. The value of F_{min}, which occurs when $\Gamma_s = \Gamma_{opt}$, can be read from a noise figure meter while the source reflection coefficient that produces F_{min} can be determined accurately using a network analyzer.

  r_n - The noise resistance.

- Input section: Enter or modify the artwork vectors. Under the transistor common connections, choose to have two common connections. The FET's used usually come in die format with two common source connections.

- Transistor vectors: *MultiMatch* uses transistor vectors to specify the physical dimensions of the transistor to be used. The transistor vectors used for this design are shown in Table C.1.

Input vector (i)		
X(mm) = - 0.385	Y(mm) = 0	θ(°) = 180°

Common_1 vector (c1)		
X(mm) = - 0.192	Y(mm) = - 0.220	θ(°) = - 90°

Common_2 vector (c2)		
X(mm) = - 0.192	Y(mm) = 0.220	θ(°) = 90°

Table C.1: Transistor vector inputs

The vector specifications shown above can be better described by Figure C.5 shown below. Here it can be seen that the output connection stays fixed at the coordinate (0, 0, 0°). All other ports are specified by using this port as reference.

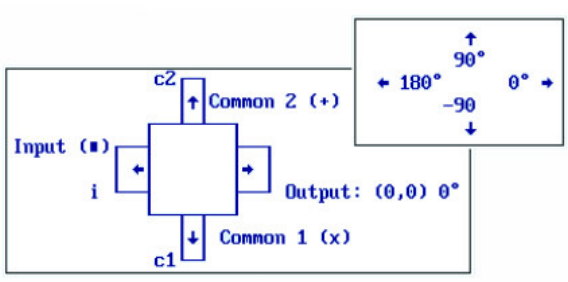


Figure C.5: Transistor vector specifications

Check that the two-port vectors specified correspond to the transistor's physical dimensions and ports.

- Input section: Display *k/MAG/MSG/Ga/Gw/Gt* to see the response of the device before device modification. The following will be displayed:

  F_{opt}: The lowest noise figure obtainable with the transistor at the relevant frequency.

  $G_{a(Znsopt)}$: The available power gain associated with the source impedance associated with the source impedance associated with the minimum noise figure.

  $M_{(Znsopt)}$: The noise measure associated with the minimum noise figure source impedance.

F_m: The noise figure associated with $M_{(Znsopt)}$, that is, the noise figure of an infinite chain of identical amplifiers, all tuned for minimum noise figure.

$TUN_{(Znsopt)}$: The tunability when the source impedance is that required for minimum noise figure.

k: The Rollette stability factor is a measure of the transistor stability. A two-port is inherently stable at any frequency at which k > 1.

MAG: The maximum power gain available from the transistor at the frequency specified.

MSG: The maximum stable gain, that is the gain which would be obtained if the transistor was stabilized (k = 1) without modifying y_{21} and y_{12}.

Gt: The transducer power gain with the default/specified source and load terminations.

- Input section: Define load line boundaries and exit the input section. The intrinsic load-line parameters can now be specified. For Class A amplifiers, limits on the output voltage and the output current of the intrinsic transistor are required to estimate the output power. These limits are defined in *MultiMatch* with four boundary lines. The relevant parameters are: Imax_0, Rimax, Imin_0, Rimin, Vsat, Rsat, Vbrk_0, Rbrk. The load line boundaries and bias point used for the design is shown hereafter.

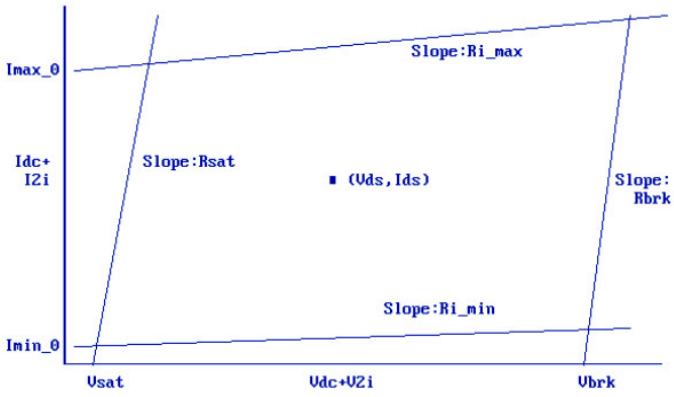


Figure C.6: Graphical description of load line boundaries

Left border	
Vsat (V) = 400E-3	Rsat(Ω) = 1E-3

Right border	
Vbrk_0 (V) = 4	Rbrk (Ω) = 1E-3

Bottom border	
Ids_mi (mA) = 200E-3	Rds_mi (Ω) = 100E3

Top border	
Ids_ma (mA) = 70	Rds_ma Ω) = 100E3

Bias point	
Vds (V) = 2	Ids (mA) = 20

Table C.2: Load line parameters

C.3 DEVICE MODIFICATION

- Device modification menu: Import/connecting lines/pads/component options. This option can be used to specify connecting lines and pads required for lumped components or the transistor used. Connecting lines may be specified for any series or shunt loading components and also for voltage-shunt and current series feedback components. In addition to the connecting lines, pads can be specified for resistors, capacitors or inductors used in each modification section.

- Connecting lines/pads option: Do not use any connecting lines or pads since a transistor in die form is used. The response of *k/MAG/MSG/Ga/Gw/Gt* is now shown after the inclusion of the connecting lines and pads. The schematic of the modified device can now be viewed.

- Add voltage-shunt feedback: Different topologies can be used to improve the amplifier response and to ensure transistor stability. Voltage-shunt feedback can be used to reduce the gain slope of a transistor and to improve its VSWR. It is important to model all parasitic phase-shifts in the loop in order to realize the predicted results in practice. Electrical line lengths must be specified at the highest frequency in the pass band.

  Voltage parallel feedback (VPF) can be added manually. One may experiment with different components, values and configurations in order to get the best results possible. With good results obtained one can combine sections to level

the gain response. If VPF is not chosen initially one can go directly to combining sections and using a global search in order to get the required response. With the VPF already in place, a new double section modification section must be generated with the existing components in place.

- Global search: Specify the pass band as 2-18 GHz. Under the Analysis/Synthesis/Optimization option, select the Gt option.

- Transducer power gain option: One use of this option is to first design an optimum load network to maximize the output power of a single-stage amplifier and then use this option to synthesize an input matching network to level the gain and to minimize the noise figure.

- Power gain option: Do not slope the gain.

- Error function parameters: The error function parameters can now be specified. These parameters are used to specify the necessary limits to be used in the search for the best device modification topology. An example of how this error function parameter table looks is shown in Table C.3

Gain window during synthesis	Default	Target values
Highest acceptable gain (dB)	9.623	9.623
Lowest acceptable gain (dB)	8.836	8
Gain step size (dB)	1.0	1.0

Gain level and ripple	Default	Target values
Average gain weight factor	0	0
Gain flatness weight factor	1.0	1.0

Input VSWR targets	Default	Target values
Input VSWR weight factor	1.0	3
Input VSWR break-point	4.804	5
Zero error input VSWR	1.0	1.0

Output VSWR targets	Default	Target values
Output VSWR weight factor	1.0	1.0
Output VSWR break-point	2.391	2.4
Zero error output VSWR	1.0	1.0

Stability targets	Default	Target values
Stability weight factor	1.0	1.0
Stability break-point	0.747	1.05
Zero error stability factor (k)	1.1	1.8

Noise figure targets	Default	Target values
Noise figure weight factor	1.0	1.0
Noise figure break-point	5.275	6.0
Zero error noise figure	2.638	4

Table C.3: Summary of error function parameters

- Frequency range for the stability error contribution: The stability factor contribution must be calculated at all frequencies. This option is usually chosen to make certain that one does not get amplifier instability at a point just outside your pass band.

Power targets	**Default**	**Target values**
Power weight factor	1.0	4
Power break-point (dBm)	8.142	8
Zero error power (dBm)	13.010	13.010

Table C.4: Table with power targets

- Power option: Control the output power.

- Modification option: Series/shunt loading must be done on the input side. When a power amplifier is designed, modification should usually be done on the input side. When a low-noise amplifier is designed, the modification is usually done on the output side. Modification on the input influences the noise figure to quite a large extent. The same goes for a modification section on the output of the transistor when designing for high power. A trade-off could possible be taken by doing modification on both input and output of the transistor.

- VSWR search parameters: The required VSWR and gain circle angular increments can now be specified. It is good to begin with an angular increment of about 30° for both. The associated simulation and search time will not be too long. A finer search is suggested although the simulation and search time might be longer. The VSWR search parameter table is shown in Table C.5.

VSWR search parameters	**Default**	**Inserted values**
Minimum VSWR to be used	1	1
Maximum VSWR to be used	5	5
VSWR increment to be used	0.5	0.5
VSWR circular increment	30	20
Gain circle increment	30	20

Table C.5: Table showing the VSWR search parameters

- The global search will typically give a result as shown in Figure C.7.

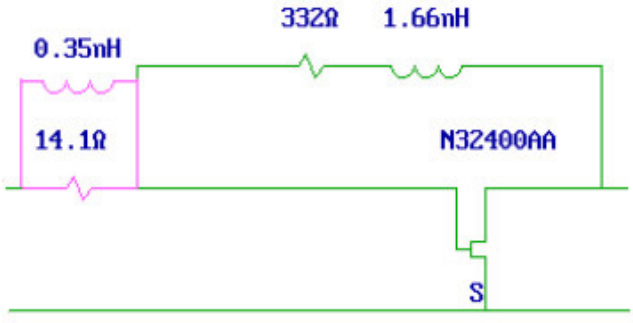


Figure C.7: Typical result obtained with a global search

Figure C.7 shows how a modified transistor will typically look. The modification section was implemented on the transistor's input as was specified. The applied modifications will typically ensure a stable amplifier and better VSWR's than obtained with the unmodified device etc. An option would be to export this circuit layout to MWO and to optimize for even better results from there. From this point on, one can go to the matching network designs for the input and output of the modified transistor.

If one looks at Figure C.7 it will be seen that this modification network does not really allow for easy manufacturing. Firstly there is no transmission line section between the feedback network and the input modification section. If a short transmission line is included at this stage it will be seen that it influences the initially obtained response. What could be done is to include pads on the input and the output side of the transistor and then do the device modification with these pads in place.

Another option, which is preferred, is to leave the modification section as it is and test what the influence of the inclusion of lengths of transmission line would be on the modified transistor's response. Optimization can also be done to accompany the included lengths of transmission line.

Another possible problem might be with the resistor value. If the resistor value is quite small it is important to take into account the physical dimensions of the lines connecting to this thin film resistor. The limit on the length of the thin film resistor is about 0.05 mm. If you choose your main line to be a certain fixed width, for example 0.254 mm (which is the width of a D10 sized chip capacitor) you get limited to a resistor value of about 9.84 Ω. If a smaller resistor value is needed, the width of the main line must be increased. The other issue is the inductance value needed. The typical inductor values usually used are larger than 10 nH. Implementing such a small inductance, especially if the design is sensitive to this inductance, may result in a process of *tweaking* a length of bonding wire to get the desired inductance.

C.4 POWER MODULE

After the device modification section has been completed, one can start on the synthesis of the matching networks for controlling either the output power or the noise figure. For this design the output power is to be controlled and it is thus necessary to complete the power module inputs.

- Exit the device modification section and proceed to the circle/power module.
- Current stage performance to be controlled: Specify the output power required.
- Option for the next matching network: Calculate *Gt* for the current stage.
- Termination option: Generate constant power contours.
- Power option: Control the output power. The effective output power option is only used when an oscillator is designed or when an amplifier is designed for high power added efficiency.
- Power module: Power specifications should be laid down. Insert the power required from the transistor.

  The maximum possible output power is a function of the input signal, the power gain, the load line constraints and also the transistor parameters that are a function of the drive level and the load line. When power contours are generated, the input is scaled automatically for maximum output power.

  Three values can be specified for the power at each frequency when contours of constant output power are to be generated. If a second or third contour is to be generated, it must be done at all frequencies of interest. Power levels of - 30 dBm are used to indicate that a second or third contour is not required.

  F2 can be pressed to edit the absolute power and the second and third contours.

Power inputs	**Target value (dBm)**
Output power required.	9.97
Absolute power for second contour.	9.5
Absolute power for third contour.	8

Table C.6: Power circle/contour targets

A power contour search is done and the potential performance on the circle contours is displayed.

- Power contour menu: Evaluate the performance at the optimum point. This option gives a summary of the results associated with the best position on each constant output power contour.
- Power contour menu: Evaluate the impedance associated with the optimum point.
- Power contour performance: The output power versus frequency response specified corresponds to a set of constant output power contours on the Smith-chart. The performance around these contours is tabulated and listed. The information provided is required to decide on the termination to be used at each frequency of interest. When constant power contours are generated, only the optimum points can be selected. The maximum output power together with the

associated load terminations the transistor needs to see on its output, is shown. The operating power gain associated with this optimum power load is also shown. Figure C.8 shows the optimum load, over a portion of the design bandwidth, needed to obtain the output power that was specified. The matching network to be synthesized must transform the transistor's output impedance to the optimum load as shown. The input impedance of the transistor is also shown.

FREQUENCY	OPTIMUM LOAD	VSWRo	INPUT IMPEDANCE	OUTPUT IMPEDANCE
(GHz)	(Ω)	-	(Ω)	(Ω)
2.0000	96.68 +j7.81	1.95	78.17 -j12.38	65.56 -j2.60
3.0000	93.63 +j14.54	1.93	75.29 -j19.68	66.25 -j3.66
4.0000	93.48 +j14.62	1.93	72.58 -j23.93	66.92 -j5.19
5.0000	86.90 +j21.80	1.90	67.50 -j28.70	67.16 -j6.47
5.2000	87.87 +j20.67	1.90	67.10 -j28.79	67.37 -j6.44
5.4000	84.77 +j23.05	1.88	65.45 -j30.00	67.63 -j6.39
5.6000	83.68 +j24.05	1.88	64.26 -j30.54	67.97 -j6.31
5.8000	82.75 +j24.40	1.87	63.19 -j31.07	68.32 -j6.29
6.0000	83.61 +j23.86	1.87	62.60 -j31.08	68.79 -j6.26
6.5000	81.03 +j24.70	1.85	59.70 -j32.23	70.50 -j6.74

Figure C.8: Power contour performance

- The optimum load impedances obtained from the power contour search will be used in the synthesis of the output matching network. Shown below is the associated output matching problem to be solved. It will be seen that the shown source impedance is the conjugate of the optimum load impedance values as listed in Figure C.9. The conjugate match is necessary to obtain maximum power transfer from the network/transistor to the load.

FREQUENCY	SOURCE IMPEDANCE		LOAD IMPEDANCE		GAIN (GT)
	Rs	jXs	RL	jXL	
(GHz)	(Ω)		(Ω)		-
2.00000	96.677	-7.814	50.000	0.000	1.0000
3.00000	93.629	-14.542	50.000	0.000	1.0000
4.00000	93.512	-14.453	50.000	0.000	1.0000
5.00000	86.888	-21.859	50.000	0.000	1.0000
5.20000	87.874	-20.637	50.000	0.000	1.0000
5.40000	84.773	-23.041	50.000	0.000	1.0000
5.60000	83.686	-24.039	50.000	0.000	1.0000
5.80000	82.752	-24.391	50.000	0.000	1.0000
6.00000	83.643	-23.776	50.000	0.000	1.0000
6.50000	80.969	-24.860	50.000	0.000	1.0000

Figure C.9: Associated output matching problem

C.5 SYNTHESIS OF MATCHING NETWORKS

- With the matching problem defined, one can proceed to the synthesis section and do the setup for the associated matching problem.

- Impedance matching option: Solve the defined matching problem. The impedance matching data file name must be specified at this stage. It is suggested to use the default name supplied. The last character used before the file type indicates the position of the matching network in the amplifier.

- Amplifier synthesis menu: Synthesize the matching network for the current stage.

- Impedance matching option: Synthesize distributed/mixed lumped-distributed solutions.

- Input section: Define terminations and power gain required. Do not adjust the source or load impedances specified. Use F6 to switch to impedance values instead of the default reflection coefficients. The gain (Gt) is left unchanged at 0 dB. This ensures a match for optimum output power.

- Impose topology constraints: Choose the Lumped/Distributed/Microstrip option and synthesize microstrip solutions. Under the distributed option, choose not to use lumped components to reduce line lengths.

- Topology constraints: The number of network elements to be used is usually chosen to be 3. This should be sufficient for most cases. If you've got a more complex matching problem to solve, it is better to use more network elements.

- Modify the parameters for controlling the systematic search: Nothing is changed here except the Q search windows if necessary. It might be necessary to make the Q search window larger than the default values in order to get a more accurate search.

- Specify distributed/microstrip parameters: Under the distributed option the conversion of open-ended stubs to double stubs is not allowed.

- Microstrip specifications: These inputs are used to specify the properties of the microstrip material to be used. Typical inputs are shown in the Table C.7 and Table C.8.

Microstrip substrate specifications (Alumina)	
Relative dielectric constant of the substrate.	9.8
Substrate thickness (mm)	0.381 (15 mil)
Conductor thickness (μm)	2
Cover height (mm)	10

Table C.7: Microstrip substrate specifications

Conductor and substrate losses (Alumina)	
Conductivity (S/m) of the strip inductor.	41E6
Loss tangent of the substrate	0.0005

Table C.8: Conductor and substrate losses

- Microstrip option: Use via holes for any short-circuited stubs, with a minimum via hole diameter of 1 mm and a step size of 0.1 mm for the hole diameter. The minimum value of the pad width relative to the via hole diameter is chosen to be 1.4 while the maximum pad width relative to the via hole parameter is 1.6. The associated gap specifications for lumped elements are given in Table C.9.

Gap specifications	
Capacitor gap (mm)	0.2
Inductor gap (mm)	0.3
Resistor gap (mm)	0.1

Table C.9: Gap specifications

- The specifications for the microstrip solutions to be used can now be specified. Table C.10 shows the specified line widths.

Line widths	
Line width for main line section on the output side (mm).	0.254
Line width for main line section on the input side (mm).	0.254
Line width for shorted stubs (mm).	0.2
Line width for open-ended stubs (mm).	0.2

Table C.10: Line width specifications

Length of main-line section	
Minimum separation between stubs	2
Maximum length of any main line section (mm)	5.043

Table C.11: Length of the main-line section

T-junction parasitics	
δθ_ML (°) - (Shift in reference plane of main-line when a stub is used.	1.056
δθ_SST (°)	14.546
δθ_OST (°)	14.546
BT_SST (mS) - (T-junction parasitics. Must be $\approx \leq 1$.)	1.272
$(1/n^2)$_SST - (Transformer effects must be ≈ 1)	1.114
BT_OST (mS)	1.273
$(1/n^2)$_OST	1.114

Table C.12: T-junction parasitics

Series capacitor pads	
Width of pads to be used for any series capacitors (mm).	0.254
Length of any series capacitor pads (mm).	0.35

Table C.13: Series capacitor pads specifications

Solutions to the matching problem can now be synthesized.

- Optimization option: Optimize the active performance. Specify the main and secondary weight factors for optimization.
- Error function option: Zero the error contribution when Po > Po_specified.

- Display the first solution and accept if the given solution is good enough. Display the output power, impedances, VSWR's, Gt, δ, K etc. to evaluate the solution performance. If the solution is good enough accept the solution displayed and exit this section.

- Circuit file option: Add the current stage to the circuit file and create a data file for the next matching problem to be solved. From here on onwards, the procedure is basically the same as for the synthesis of the last matching network.

After the last matching network is synthesized it will be written into a *MultiMatch* circuit file from where the designed amplifier can be analyzed, modified, optimized etc. Shown hereafter is the artwork configuration of the designed amplifier.

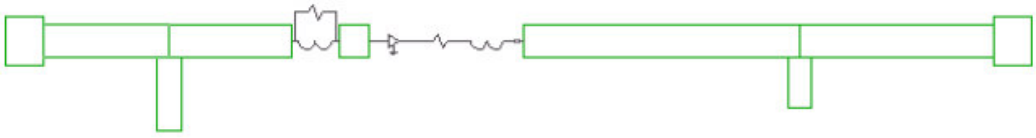


Figure C.10: The MultiMatch artwork configuration for designed amplifier

C.6 SIMULATED RESULTS

The artwork as shown by *MultiMatch* looks very simple and it does not show the correct connection for the voltage shunt feedback configuration. It is from this stage that one has to implement MWO to take into account what the effect, of for example, a thin film resistor would be on the amplifier response. All the components seen in the artwork configuration are lumped components. One could have used *MultiMatch's* thin film resistor option or used pads for specific components like capacitors and inductors. It was however decided to stick to the lumped components as shown and to do physical integration of components with the use of MWO. The results obtained from this amplifier design are shown hereafter. These are the simulated results to which practical results are to be matched to.

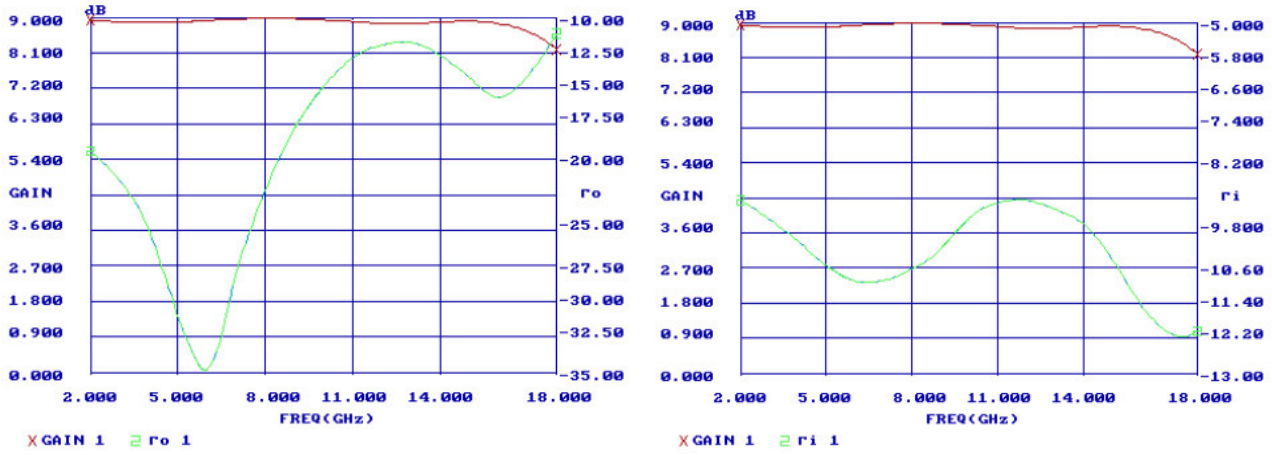


Figure C.11: Gain response together with the input and output return loss

It is seen that the gain is close to the design specification of 10 dB but not quite there yet. It was seen to what extent sacrifices had to be made on the design specifications in order to get acceptable designs. Improvement of one specification will almost surely lead to deterioration of another. The best solution would be to do a design that takes the necessary trade-off to obtain the best possible results with a specific device.

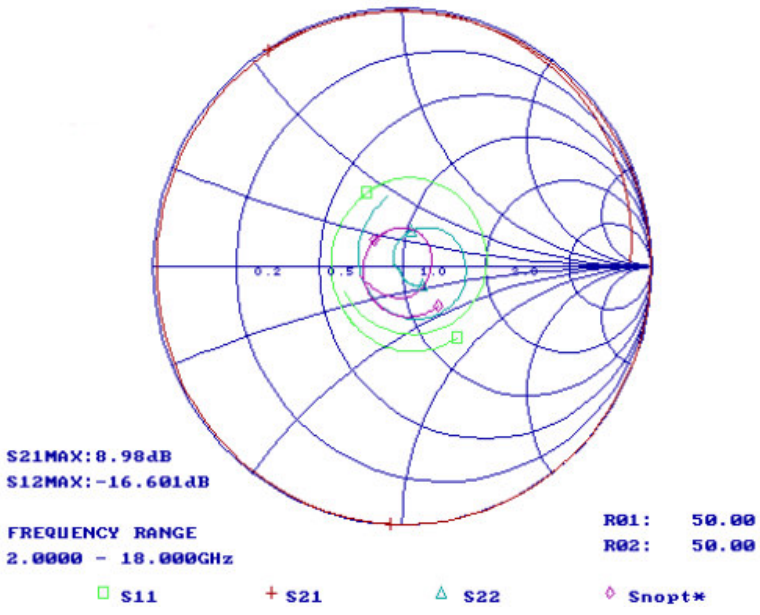


Figure C.12: S-parameter response as seen on the Smith-chart

The Smith-chart provides a very good intuitive feel for the designed amplifier's response. From Figure C.12 it can be seen that the input reflection response is further from the centre of the Smith-chart than that of the output reflection response. The input is thus not as well matched as the output. It can also be seen that the gain will be rather flat all over the band except for frequencies higher than 16 GHz. This can be seen from the transmission response (S_{21}) and the dip it makes at the right hand side of the Smith-chart.

From the noise figure response it can be seen that the designed amplifier complies with the noise figure specification of 4 dB.

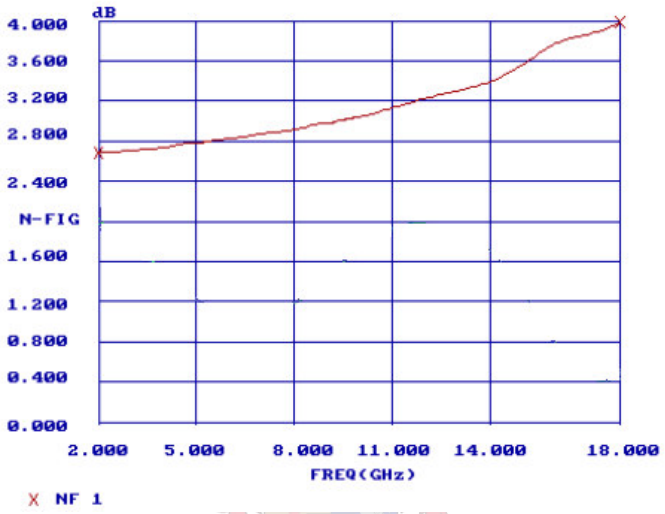


Figure C.13: Noise figure response of the designed amplifier

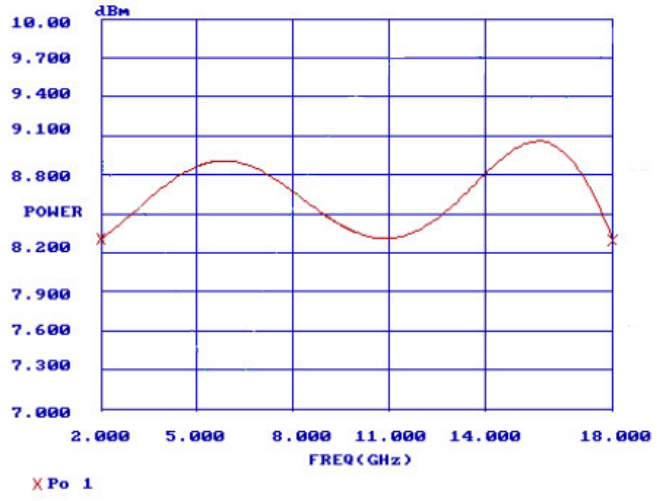


Figure C.14: Maximum unclipped power of the designed amplifier

The figure above shows the maximum unclipped power for the designed amplifier. The output power response is rather flat over the frequency band (± 0.4 dBm) and it is better than the designed 8 dBm.

C.7 MWO IMPLEMENTATION AND RESULTS

Up to this stage, *MultiMatch* was used successfully for amplifier synthesis. It will be shown to what extent MWO can be used for further optimization and fine-tuning. The artwork as shown in *MultiMatch* can be exported as a *.dxf file which can then be accessed with *AutoCad*. This was done and the artwork was measured up. This may seem like quite a tedious process, but the rewards are worth it. The designed amplifier can now be reconstructed in the MWO schematic window. If this process is done accurately it will be seen that the amplifier response obtained with MWO will be a true replica of what is obtained with *MultiMatch*.

C.7.1 MWO SIMULATIONS

With the amplifier reconstructed in the schematic window one can use the optimization and tuning tools to obtain the desired response. For this power amplifier it was seen that any change on the amplifier's output section would influence the maximum unclipped output power. Caution was taken to ensure that the output section was not altered during the optimization or tuning process. If a low-noise amplifier was designed, one would not have tampered too much with the amplifier's input section.

For the power amplifier it was decided to do most of the tuning on the input side. It was also necessary to implement DC blocking capacitors and DC biasing, without influencing the RF response of the amplifier. Figure C.15 shows a typical MWO artwork layout that was obtained from an initial *MultiMatch* artwork.

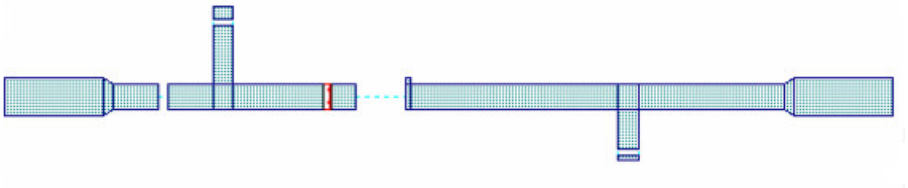


Figure C.15: MWO artwork for amplifier designed in MultiMatch

Figure C.15 shows a functionally and cosmetically improved version of the initial MultiMatch artwork. This artwork also includes space for the necessary DC blocking capacitors. The DC bias network is not shown, but this design allows for easy application of biasing. The thin film resistor used for device modification can also be seen. The inductor (wire) in parallel with this thin film resistor is not shown. Another aspect that makes this design attractive is the fact that it was forced to a certain extent to have 0.254 mm wide main lines. This was done to easily mount a D10 (0.254 mm × 0.254 mm) size

capacitor on the track. The pad specification for the capacitors that was specified during the design process was thus not really used. Pads could have been used but it was avoided because of the introduction of undesired discontinuities. A continuous main line is preferred. If one has to make use of stepped discontinuities, the use of a taper is suggested. It looks much better and it offers a smoother transition between stepped transitions. The use of these types of tapers can be seen in Figure C.15. The physical length of the taper can be adjusted in MWO for optimal performance.

From Figure C.15 it can also be seen that tuning pads were included. One can typically adjust the stub lengths for optimal performance. If a stub needs to be shortened for optimal performance, give the stub this optimal length but include tuning stubs so that the nominal length is what was originally designed for. Care must be taken not to just include tuning stubs at the ends of all open ended stubs. The actual response when a stub is lengthened should be verified. Lengthening a stub might worsen the amplifier response and in this case the tuning stub should be omitted.

The actual results obtained with the *MultiMatch* design implemented in MWO are shown hereafter in Figure C.16.

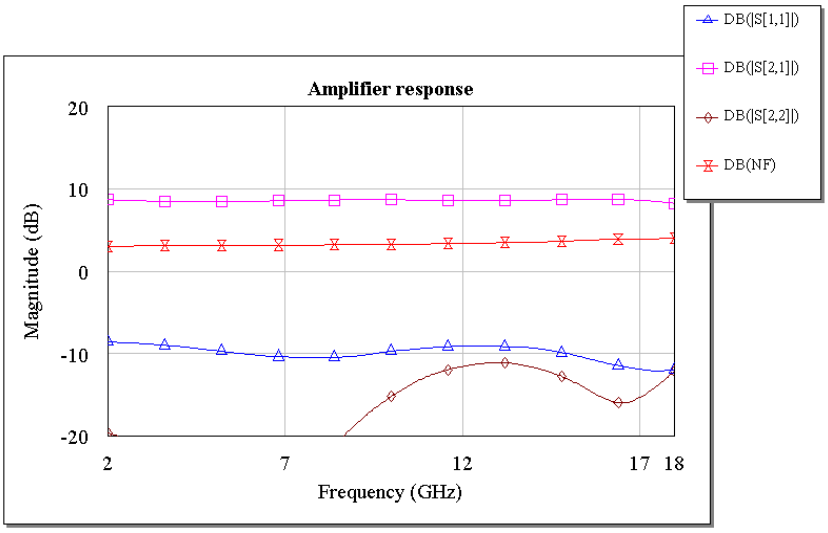


Figure C.16: Simulated results obtained in MWO

The results seen in Figure C.16 show the amplifier response after implementation in MWO. The gain is about 8.5 dB with a ± 0.35 dB ripple. The noise figure is 3.75 dB at its maximum point and below the specified 4 dB. It is seen that the input return loss is not as good as what would have been ideal, but it is true to the design. The output return loss is very good.

The manufacturer's specified S-parameters usually include the effect of bonding wires and it will be seen that in this design no effort was made to include the bonding wires' parasitic effects. It is however important to note how bonding wires that are too long can influence expected results. The use of FET's with more than one gate bonding pad is suggested since the parallel bonding wires will ensure lower parasitic inductance at the FET input. The design did not include the effect of source grounding techniques. Typically the parasitic effects of the 100 pF capacitors used to get proper RF ground is very small.

C.7.2 PHYSICAL IMPLEMENTATION AND MEASUREMENTS

Figure C.17 shows the complete 2-18 GHz amplifier after the artwork has been etched on the Alumina substrate. It is seen how tuning pads were utilized to improve the amplifier response.

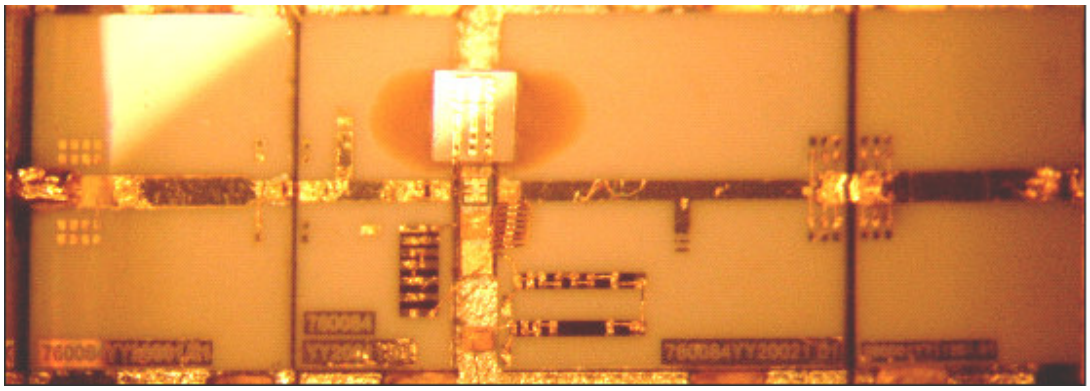


Figure C.17: Complete 2-18 GHz amplifier in its test jig

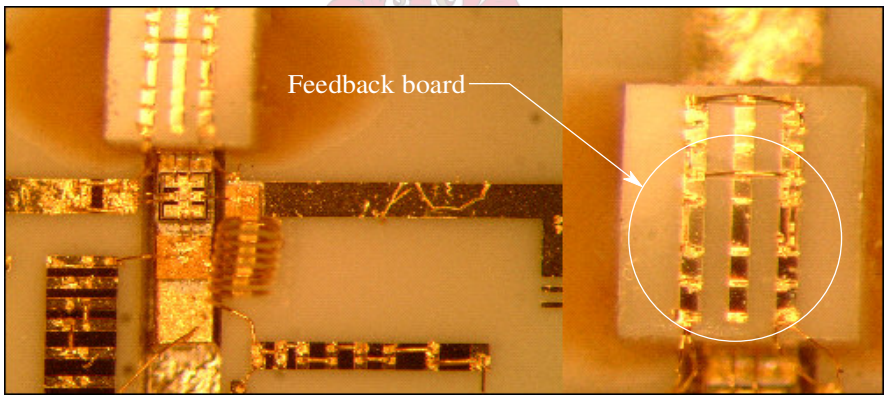


Figure C.19: Physical implementation of the designed amplifier

Figure C.19 shows how the amplifier was physically realized. It shows how feedback was implemented with etched resistors on an Alumina feedback board and how the biasing was realized. The photo also shows the double feedback bonds used to decrease parasitic inductance. On the amplifier input one can also see two wire bonds in parallel with the thin film resistor to obtain the wanted response from the modification network. The DC blocking capacitor as well as the source bypass capacitors is visible.

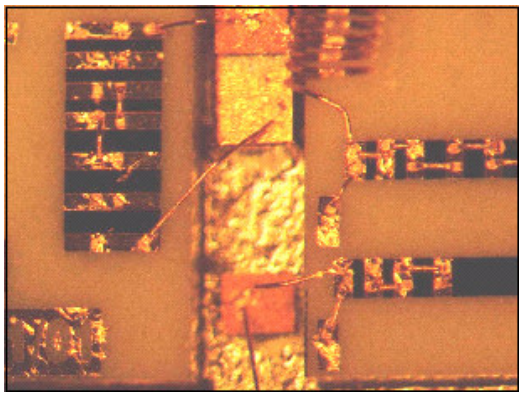


Figure C.20: Bias implementation

Figure C.20 shows the implementation of the passive bias circuit. Special test pads used for tuning are shown in the photo. Multimeter probes can be used on these pads without scratching the gold on pads where bonding is crucial. Both the source and drain resistors are shown with their interconnections. These interconnections must also be kept as short as possible. The standoff used to mount the transistor is also shown. The noise figure measurements and the simulated noise figure are shown in Figure C.21.

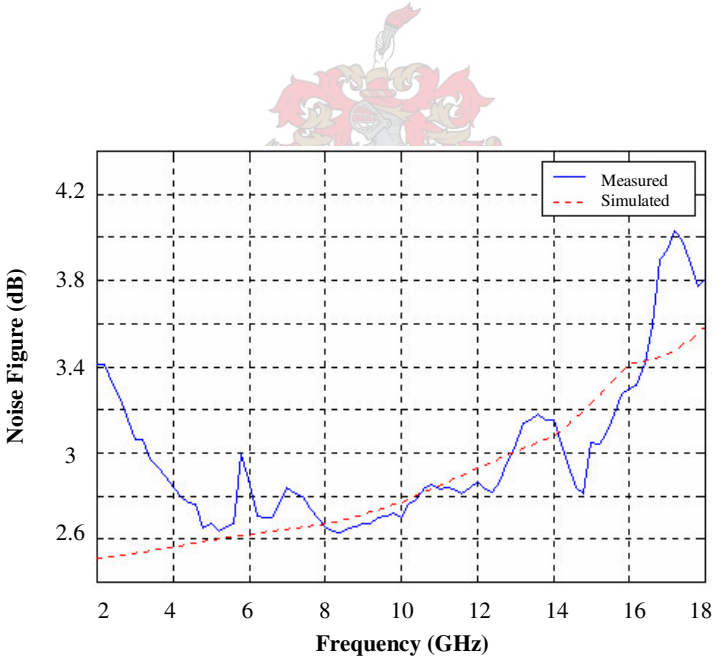


Figure C.21: Measured and simulated noise figure results

The measured noise figure shows a maximum of 4.2 dB at 17.2 GHz. The noise figure response is acceptable and is close to the design specification of 4 dB (max). The gain response obtained with *MultiMatch* and MWO is compared to actual measured results in the figure shown below.

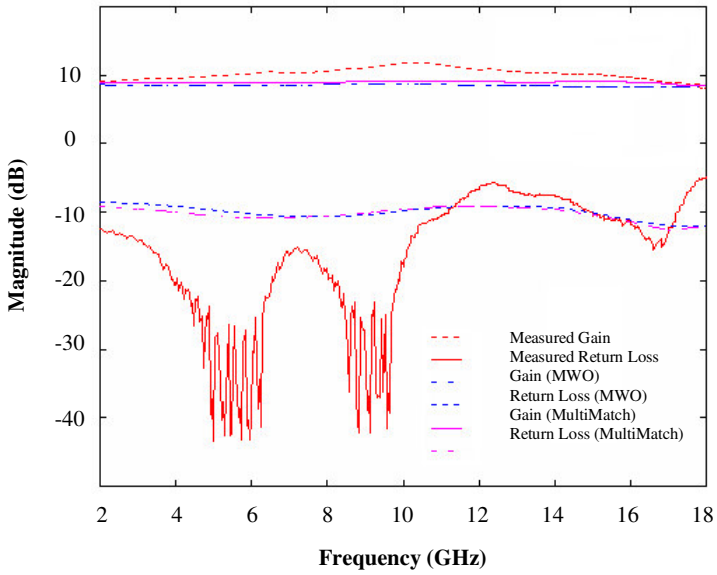


Figure C.22: Simulated and measured gain and input return loss

Figure C.22 shows that the simulated and measured results are quite close. Trends set in the simulated response are seen in the measured results, which show true implementation. The summarized results for the designed amplifier are shown in Table C.14.

Specification	Measured result
Gain(max)	11.3 dB
Gain(min)	7.8 dB
Gain ripple	± 1.75 dB
NF(max)	4.2 dB
P_{1dB}	> 7.5 dBm
$VSWR_{in}$	2.6:1
$VSWR_{out}$	1.9:1

Table C.14: Result summary for the designed amplifier

C.8 CONCLUSION

The design of the single-stage 2-18 GHz amplifier set a firm theoretical and practical foundation for future amplifier designs. It also served the purpose of getting to know both *MultiMatch* and *Microwave Office* to such extent that these tools could be used efficiently for broadband RF amplifier designs.

APPENDIX D

THE BRANCH-LINE COUPLER FOR USE IN A BALANCED AMPLIFIER

D.1 INTRODUCTION

The bandwidth restriction of the hybrids used in a balanced amplifier configuration is one of the biggest limiting factors in implementing this design. To evaluate the bandwidth restrictions opposed to physical size, the branch-line coupler was investigated for possible use in a balanced amplifier. Its typical bandwidth will be evaluated and it will be shown how limited bandwidth improvement is possible by making use of a multi-section design. Suggestions as to alternatives hybrids, which show similar bandwidth restrictions, are made. Even though, the desired hybrids could not be implemented over the full 2-18 GHz bandwidth, it offers a significant consideration for reduced bandwidth designs.

D.2 BRANCH-LINE COUPLER DESIGN

This section serves to show how one would go about in designing a 3 dB branch-line coupler such as that shown in Figure D.1.

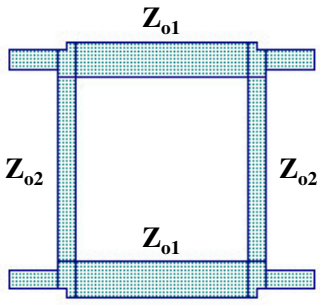


Figure D.1: A 3 dB microstrip branch-line coupler

The design of a 3 dB branch-line coupler in a 50 Ω system is done hereafter without going into the detail of the design theory. For the desired 3 dB coupling, C = 3 in the design equations as discussed in [17]. The first design equation to be solved is given by (D.1).

$$C = 3 = 10\log\left(\frac{1}{1-\left(\frac{Z_{o1}}{50}\right)^2}\right) \tag{D.1}$$

Z_{o1} in this equation is the characteristic impedance of the horizontal branches as seen in Figure D.1. To simplify calculations the bracketed term as part of the denominator is replaced with *k*. The new equation is now:

$$C = 3 = 10\log\left(\frac{1}{1-(k)^2}\right) \tag{D.2}$$

$$\therefore\ \log\left(\frac{1}{1-(k)^2}\right) = 0.3 \tag{D.3}$$

Solving for *k* yields:

$$k = \sqrt{1-\frac{1}{10^{0.3}}} \tag{D.4}$$

The relation between *k* and Z_{o1} is returned, to yield:

$$k = \frac{Z_{o1}}{50} = \frac{1}{\sqrt{2}} \tag{D.5}$$

From (D.5), Z_{o1} is calculated as 35.4Ω. To determine Z_{o2} (characteristic impedance of vertical branches), the determined value of Z_{o1} is substituted into the following equation:

$$\frac{Z_{o2}}{Z_o} = \frac{\frac{Z_{o1}}{Z_o}}{\sqrt{1-\left(\frac{Z_{o1}}{Z_o}\right)^2}} \tag{D.6}$$

Thus,

$$\frac{Z_{o2}}{50} = \frac{\frac{35.4}{50}}{\sqrt{1-\left(\frac{35.4}{50}\right)^2}} \tag{D.7}$$

Thus Z_{o2} = 50 Ω

Depending on the operating frequency, the λ/4 lengths of the branches of the coupler can be determined. With the necessary branch characteristic impedances and the dielectric properties known, the branch widths are determined. The MWO schematic layout for a branch-line coupler with center frequency equal to 7.5 GHz is shown in Figure D.2.

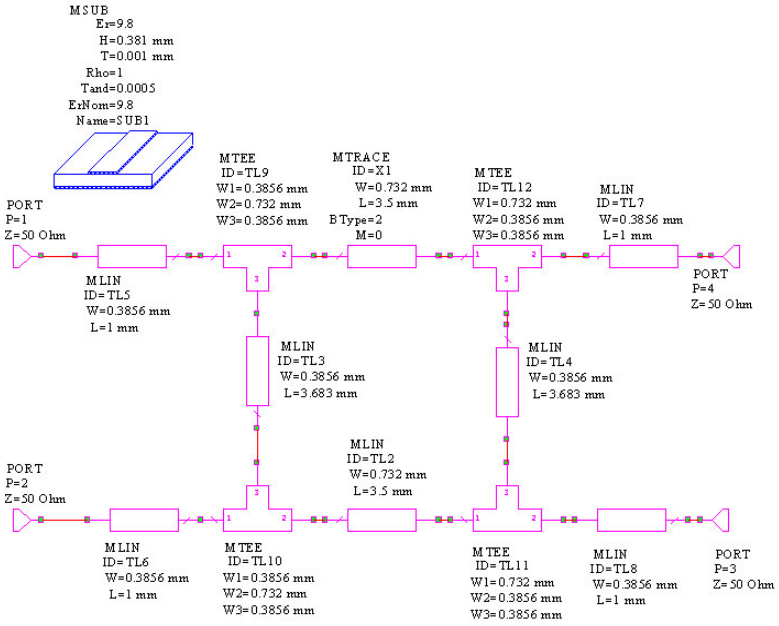


Figure D.2: Schematic layout of a branch-line coupler

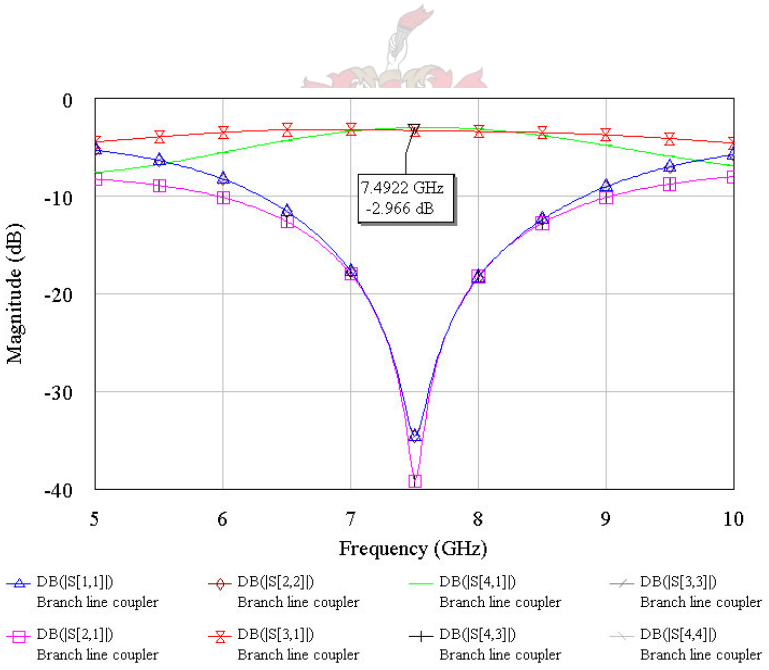


Figure D.3: S-parameter response of the branch-line coupler

The lengths and widths for the different branches were determined with a transmission line calculator. The T-sections as seen in Figure D.2 may have an influence on the branch-line coupler response and actual lengths and widths may, therefore, need to be adjusted to get the proper response. Figure D.3 shows a rather limited bandwidth for the designed coupler. The coupling at the design frequency of 7.5 GHz is approximately 3 dB for both output ports. Figure D.4 shows the plot of the phase difference between the two output ports. At the design frequency the phase difference between the two output ports is

expected to be 90°. The phase difference deviates from the expected 90° as the frequency differs from the design frequency. This would then also explain the fact that the coupling response varies from the ideal response when the operating frequency is other than the design frequency.

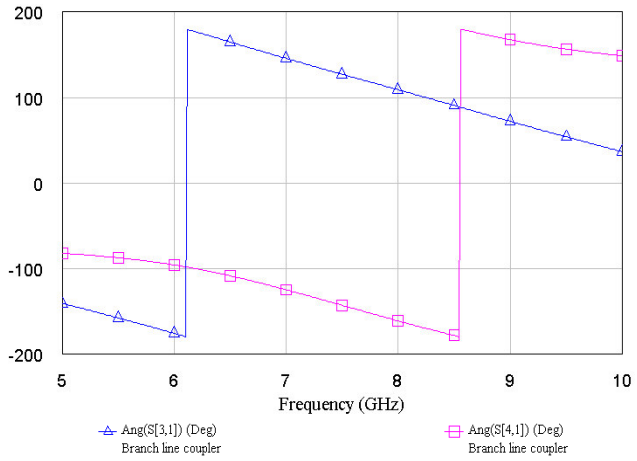


Figure D.4: Phase difference between branch-line coupler outputs

A typical design of a 3 dB branch-line coupler was done and simulations were done in MWO to get a better feel for its operation. Physical implementation of the branch-line coupler will not offer much of a problem, but it has a very narrow bandwidth and will not allow for use over the complete 2-18 GHz band. The following section discusses the effect of cascading different branch-line couplers in order to improve on bandwidth.

D.3 CASCADED BRANCH-LINE COUPLERS FOR BANDWIDTH IMPROVEMENT

This section aims to determine how the bandwidth of a branch-line coupler can be extended for intended use in a balanced amplifier. For purpose of doing an analysis of the cascaded directional coupler, the signal flow diagram shown below is used.

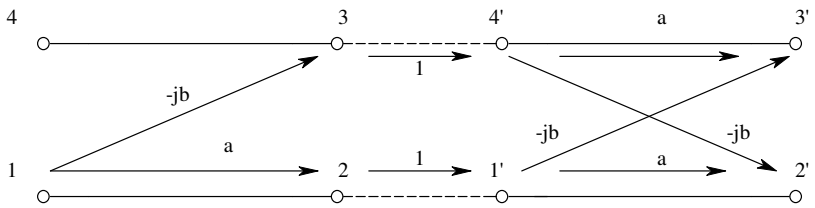


Figure D.5: Signal flow diagram for a cascaded branch-line coupler

In the shown configuration S_{21} = a (coupled path) and S_{31} = - jb (through path).

$$S_{2'1} = (a)(a) + (-jb)(-jb) = a^2 - b^2 \tag{D.8}$$

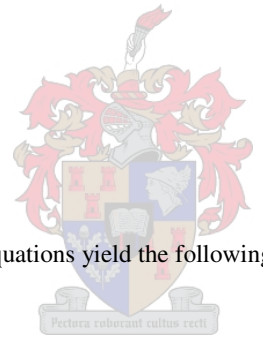
$$S_{3'1} = (a)(-jb) + (-jb)(a) = -j2ab \tag{D.9}$$

For a 3 dB coupler (power divider) the following requirements must be true:

$$S_{2'1} = a^2 - b^2 = \frac{1}{\sqrt{2}} \tag{D.10}$$

and

$$S_{3'1} = -j2ab = -j\frac{1}{\sqrt{2}} \tag{D.11}$$



Solving simultaneously for the previous two equations yield the following values for *a* and *b*.

$a = 0.924$ and $b = 0.38$

The decibel equivalents for *a* and *b* is determined as:

$$20\log(0.924) = -0.68\ dB \tag{D.12}$$

and

$$20\log(0.38) = -8.34\ dB \tag{D.13}$$

A cascade of two 8.34 dB couplers will thus be equivalent to a single 3 dB coupler [21]. To determine the effect of an extra stage on the bandwidth of the coupler a simple design is done to implement two cascaded 8.34 dB couplers. Using the design equations for branch-line couplers as discussed earlier the characteristic impedance of each of the branches can be determined. Z_{o1} is determined to be 46.2 Ω while Z_{o2}, yields a value of 120.6 Ω.

The schematic implementation of the 8.34 dB branch-line coupler in MWO is shown in Figure D.6. Some adjustment on the branch lengths was necessary to account for the inclusion of the T-sections.

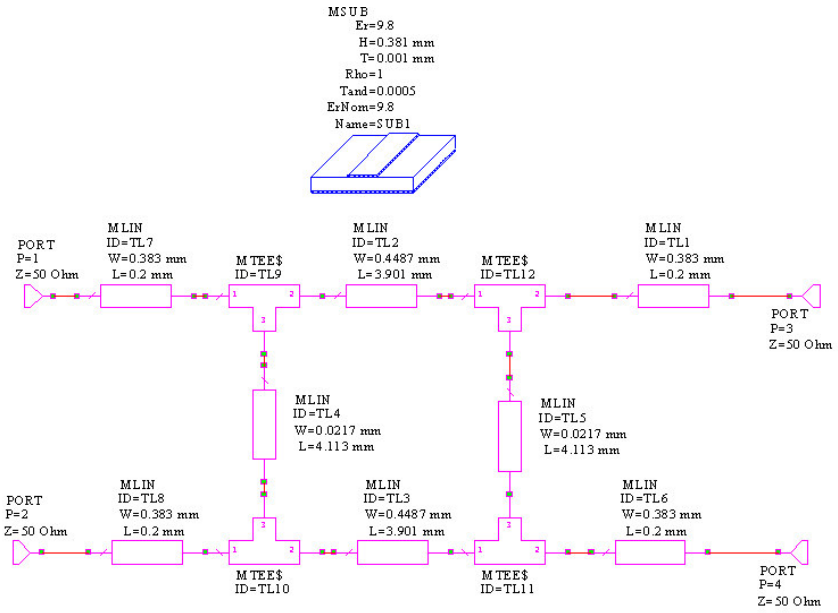


Figure D.6: Schematic layout of an 8.34 dB branch-line coupler

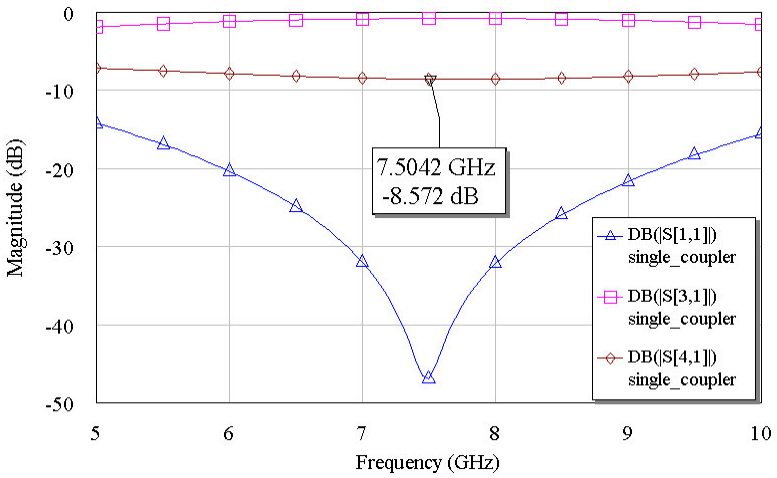


Figure D.7: Response of an 8.34 dB branch-line coupler

The response of the 8.34 dB coupler is shown in Figure D.7. It is seen that the actual coupling is about 8.57 dB at the design frequency and indicates the inclusion of some losses through the coupler as well.

As seen from the cascaded response of the two branch-line couplers in Figure D.8, the resultant coupling is 3 dB on both of the output ports. Compared to the single branch-line coupler response there is a definite bandwidth improvement.

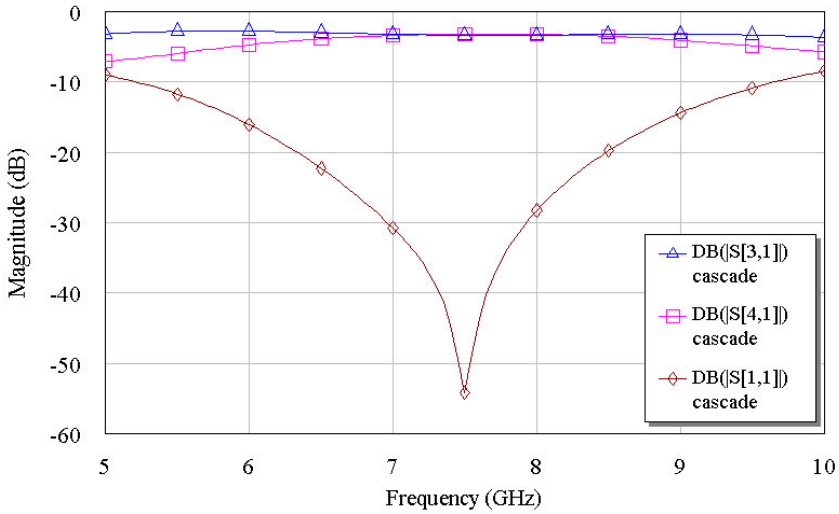


Figure D.8: The cascaded response of two 8.34 dB branch-line couplers

The phase difference between the output ports, as seen in Figure D.9, is fairly constant at 90° near the design frequency of 7.5 GHz. The bandwidth over which the phase difference is approximately 90° will be larger than for the single 3 dB coupler case.

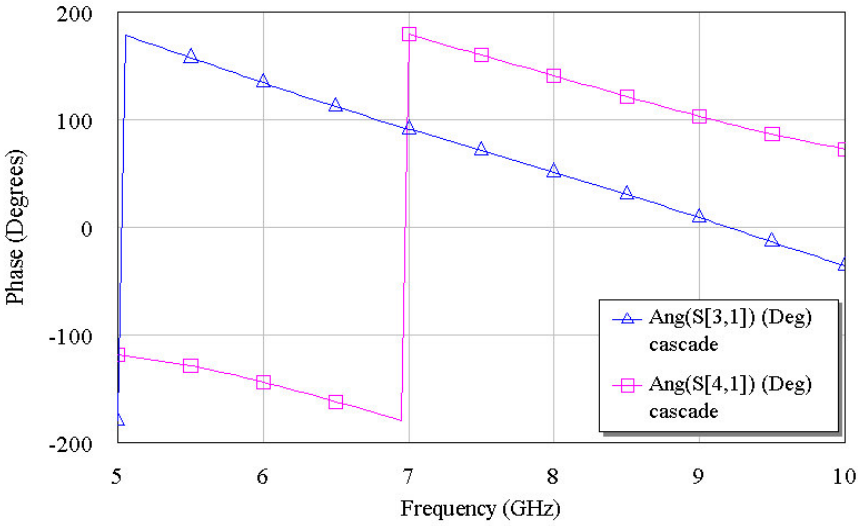


Figure D.9: Phase difference for the cascaded case

What makes the cascade configuration impractical is the fact that the widths of the vertical branches will decrease as the number of couplers in the cascade increase. For the two cascaded 8.34 dB couplers the line widths for the vertical branches are already too thin to be etched. The minimum line width to be etched accurately with available technology is

approximately 0.05 mm. An alternative would be to use a thicker substrate to etch the coupler. In doing this the width of the vertical branches can be increased slightly.

The discussion on cascading of branch-line couplers showed the feasibility thereof for improving bandwidth. The physical limitations, particularly in terms of size, have been pointed out. For narrow band operation, the branch-line coupler would be acceptable for use in a balanced amplifier.

D.4 ALTERNATIVE HYBRIDS

Alternatives to the branch-line coupler are the Lange coupler with improved bandwidth and Wilkinson splitters with λ/4 wavelength lines included [17]. Implementation of the desired Lange coupler however required manufacturing tolerances that were too fine to be physically possible. The balanced amplifier implementing Wilkinson splitters is shown in Figure D.10. The λ/4 wavelength lines included together with the Wilkinson splitters offered significant bandwidth reduction and were not considered for a design. Other alternatives such as coupled line couplers were also experimented with, but offered the same trade-offs between bandwidth and physical size.

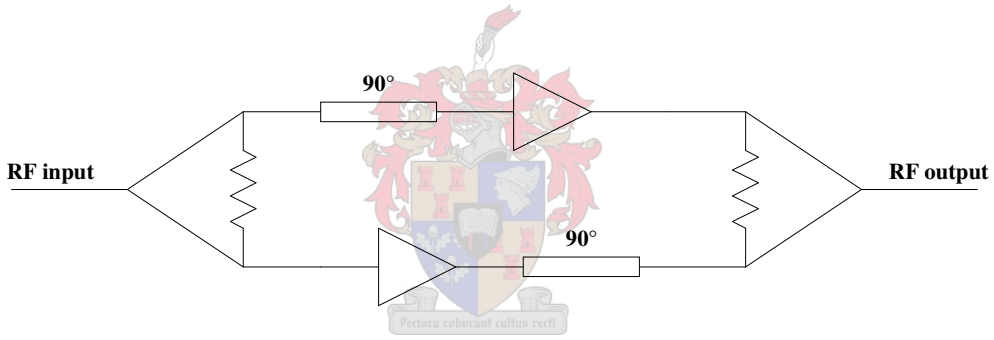


Figure D.10: Balanced amplifier configuration implementing Wilkinson splitters

D.5 CONCLUSION

The bandwidth restriction of the hybrids used in a balanced amplifier configuration was shown to be one of the biggest limiting factors in implementing this amplifier. The discussion, although concerned with the branch-line coupler, also highlighted the bandwidth restriction of other hybrid couplers. Another limitation that was pointed out was the constraints set by existing manufacturing technology.

APPENDIX E

GAIN VARIATION AS A FUNCTION OF BIASING

E.1 INTRODUCTION

Discussed hereafter is an experiment that was performed on a single-stage 2-10 GHz amplifier to determine how gain variation is influenced by biasing. Different sets of gain measurements were done, with the drain-source voltage fixed while the drain current was varied.

E.2 EXPERIMENTAL SETUP

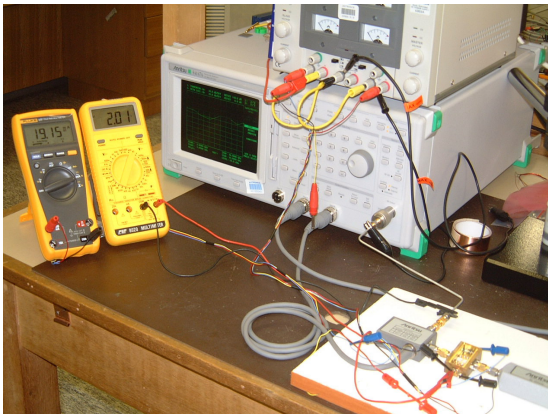


Figure E.1: Experimental setup

Figure E.1 shows the setup for the experiments performed. The scalar network analyzer is calibrated from 2-10 GHz at a low input power, typically about -20 dBm. Keeping the input power to the amplifier low enough, will ensure that the amplifier operates in its linear region and gain compression is thus prevented.

The amplifier was connected to the S.N.A (scalar network analyzer) and the necessary supply voltages were applied. Two multi-meters were used to monitor the drain current as well as the drain-source voltage. The power supply is used to fine-tune the current (I_{ds}) and the voltage (V_{ds}) to obtain a certain operating point. A dual bias configuration such as that shown in Figure E.2 was used for the experiment.

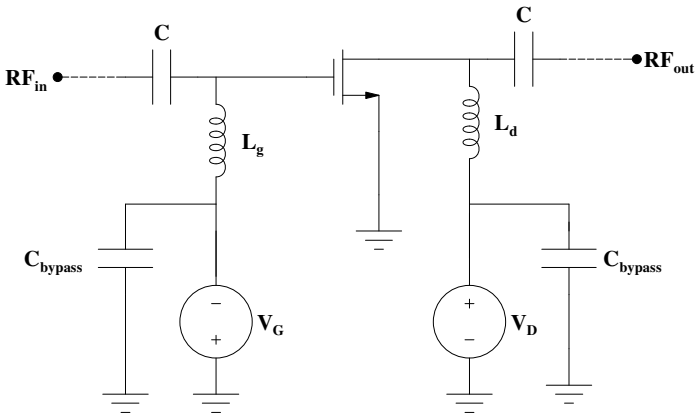


Figure E.2: Dual bias configuration

When two supplies are used as shown, the sequence of applying power is important. The gate (negative) voltage is applied before the drain (positive) voltage, to prevent transient burnout of the FET. Conversely, when removing DC bias, the drain voltage must be removed first, followed by the gate voltage. DC blocking capacitors are needed at the input and output ports. They should present a RF short so as not to affect either the insertion loss or the VSWR of the amplifier. The blocking capacitors must be free of parasitic resonance as high as the highest operating frequency. Use of bypass capacitors at the connections to the DC supplies is advised to prevent unwanted coupling to circuits external to the amplifier. The inductors, which form part of the bias injection circuit, should isolate RF signals from the power supply. Care should be taken that the inductor does not create a significant load on the transmission line. The RF impedance of the inductor should thus be much greater than the characteristic impedance of the transmission line.

E.3 EXPERIMENTAL RESULTS

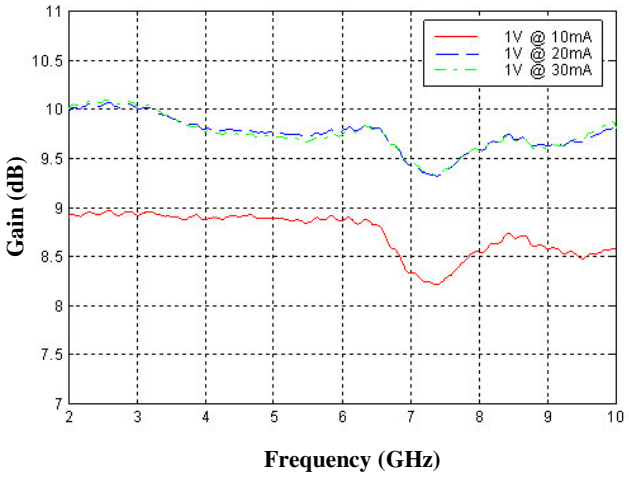


Figure E.3: V_{DS} held constant at 1V

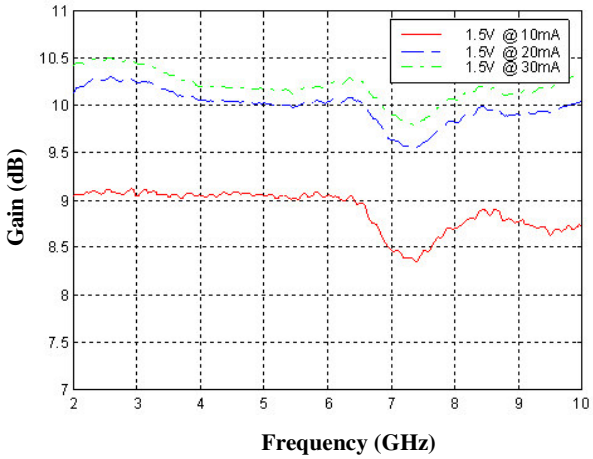


Figure E.4: V_{DS} held constant at 1.5 V

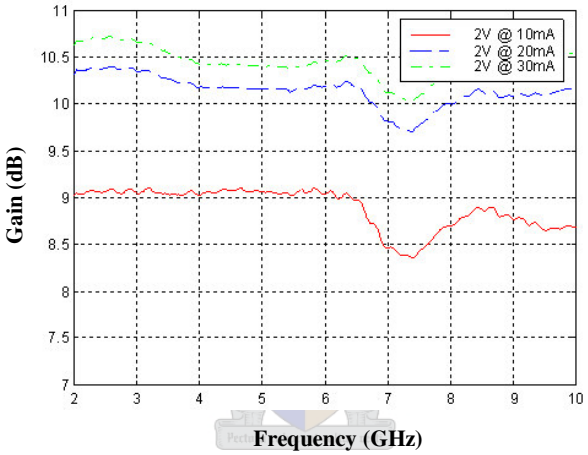


Figure E.5: V_{DS} held constant at 2 V

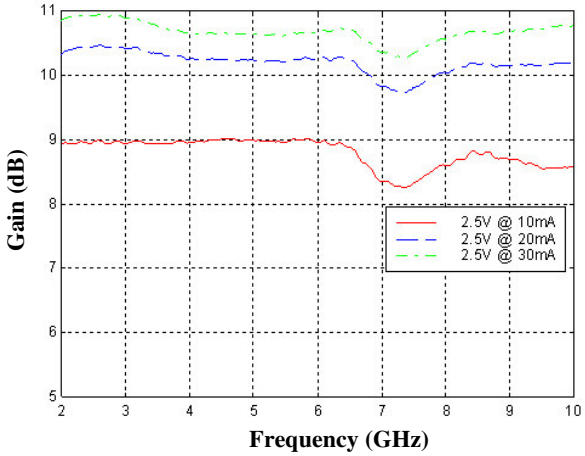


Figure E.6: V_{DS} held constant at 2.5 V

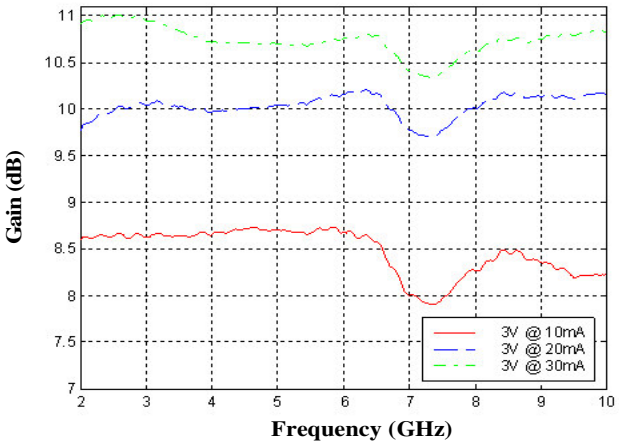


Figure E.7: V_{DS} held constant at 3 V

Figures E.3 to E.7 shows gain measurements for the case where the drain current is varied for different sets of fixed drain-source voltages. To better interpret these plots, the gain at different drain currents was plotted for fixed bias voltages in order to more clearly distinguish between the effects of the bias point variation on the amplifier gain. This result is shown in Figure E.8. The gain as measured at some arbitrary spot frequency was used for the shown plot.

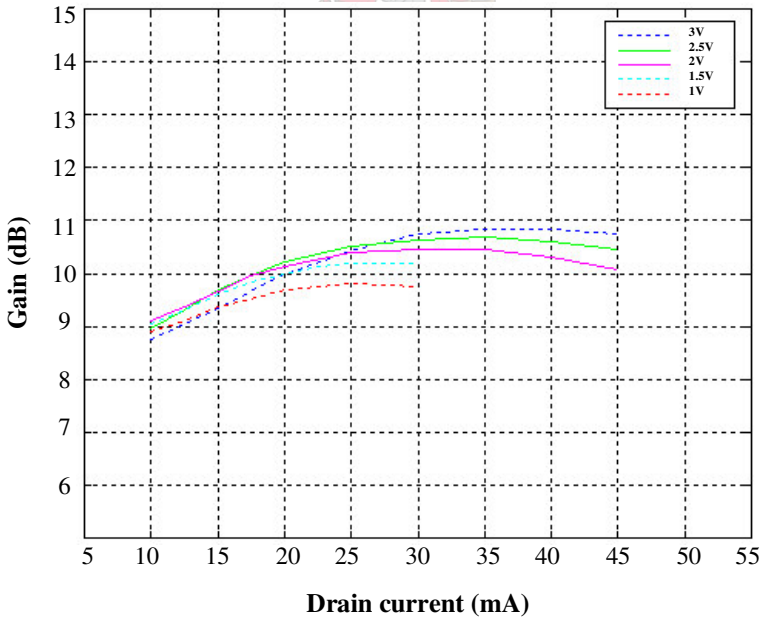


Figure E.8: Gain variation with bias current

Figure E.8 offers a valuable result in establishing a better intuitive feel for gain variation as a function of biasing. It is seen that the gain increases with bias current up to a certain point but then starts to decrease. This effect is explained by looking at the response of the FET's transconductance over bias current as shown in Figure E.9**.**

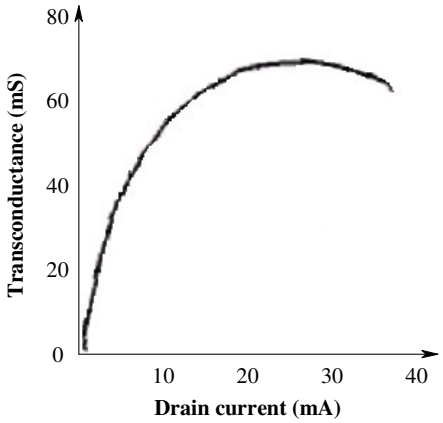


Figure E.9: Transconductance versus drain current

The transconductance response seen in Figure E.9 varies in the same manner as the gain response plotted in Figure E.8. The response shows a definite relation between the gain response of the amplifier and the FET's transconductance as a function of bias current.

E.4 CONCLUSION

The discussed experiment established the relation between transconductance versus drain current and gain versus drain current, while providing a graphical result showing how gain variation is influenced by biasing. Knowledge obtained from such an experiment is particularly useful during the tuning of a designed amplifier or limiting amplifier for that matter. Similar experiments may allow better understanding of how an amplifier's response may deviate when biasing differs from that required by the actual design.

APPENDIX F

SCHEMATIC LAYOUT OF THE FINAL DESIGN

F.1 INTRODUCTION

In this appendix, the schematic layouts of the different building blocks comprising the final limiting amplifier (BLA) are given. This is done to give better insight as to the actual design as done in MWO, while allowing for reconstruction of the complete design or portions thereof, if so required. Even though some of the building blocks are very similar, they are all shown to show subtle differences between the different schematic layouts. The different building blocks are shown in sequence from the input to the output of the designed limiting amplifier.

F.2 SCHEMATIC LAYOUTS AS OBTAINED FROM MWO

Figure F.1 shows the design configuration of the designed limiting amplifier, together with its different functional building blocks.

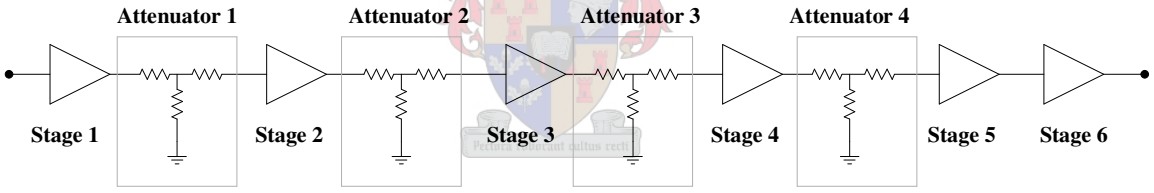


Figure F.1: Design configuration of the designed limiting amplifier

The schematic layout of each of the different functional building blocks is given hereafter. Figure F.2 shows the schematic layout of stage one. From this layout, a range of aspects is observed. On the input of this amplifier, the excitation port used for nonlinear analysis is shown. Also shown on the input of this amplifier is a DC blocking capacitor (Dilabs model). The associated bias configuration and implementation of the NE321000 nonlinear model is also shown. As part of the nonlinear model implementation, there are two parasitic capacitive elements common to the source, which were connected externally to the NE321000 nonlinear model [30]. Furthermore, the schematic layout shows the associated substrate specification that was used for purposes of the design. The feedback network, together with the interconnecting wire bonds is shown. The length of these wire bonds are critical and requires inclusion in the design. Not implemented in the design are the interconnecting wire bonds between the source of the NE321000 and the source bypass capacitors. Generally the inclusion of these bonds in a design is dependent on whether measured S-parameters include their effect or not. Furthermore, these bonds generally offer a low inductance connection if kept as short as possible. If this is the case, they may be omitted in a design. The same fact also applies to the gate and drain bonds.

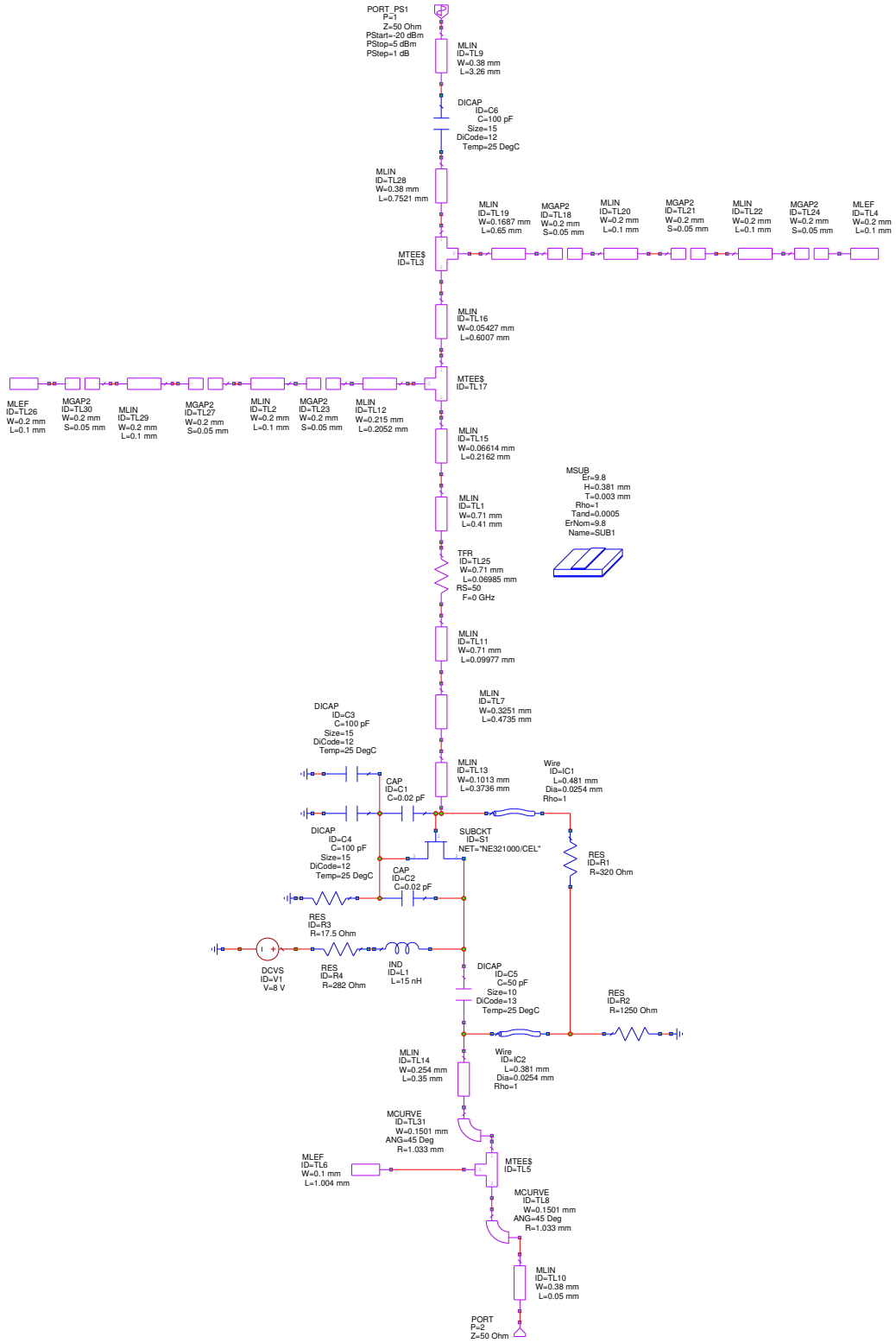


Figure F.2: Schematic layout of stage one

Figure F.2 also shows the associated output matching network with the associated bends required for physical implementation. Another aspect, of less importance, is the implementation of tuning stubs as seen on the input of the amplifier. This allows for having tuning stubs as part of the artwork layout of the relevant design. Where this is not the case, tuning stubs may be included when the design layout is done in *AutoCad*.

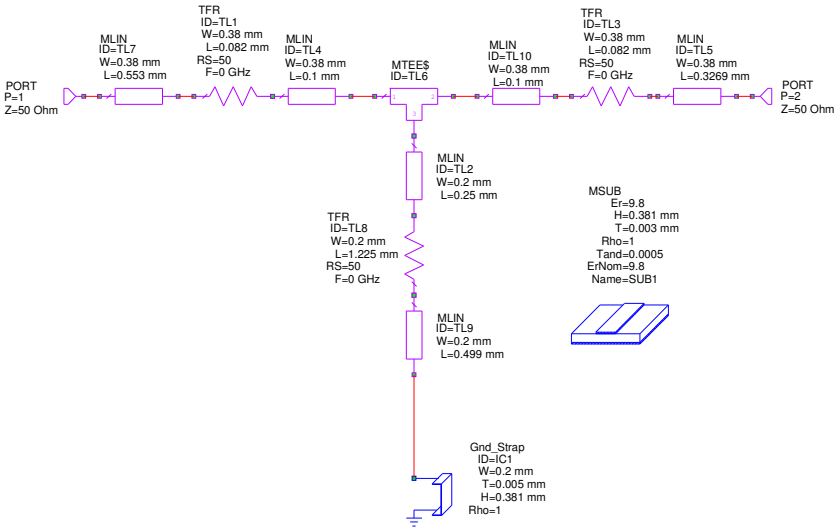


Figure F.3: Schematic layout of the first attenuator

Figure F.3 show the schematic layout of the attenuator used between the first two amplifier stages. This layout was discussed previously in somewhat detail and is, therefore, not further discussed.

Figure F.4 shows the schematic layout of stage two which is very similar to that of the first stage. The same bias configuration and feedback network is shown. Again, provision for tuning stubs was made on the input circuit. The output circuit did not include these tuning stubs, while they were implemented as part of the final design. The physical differences are observed when comparing the artwork layouts of the two designs or when carefully comparing the schematic layouts of the designs.

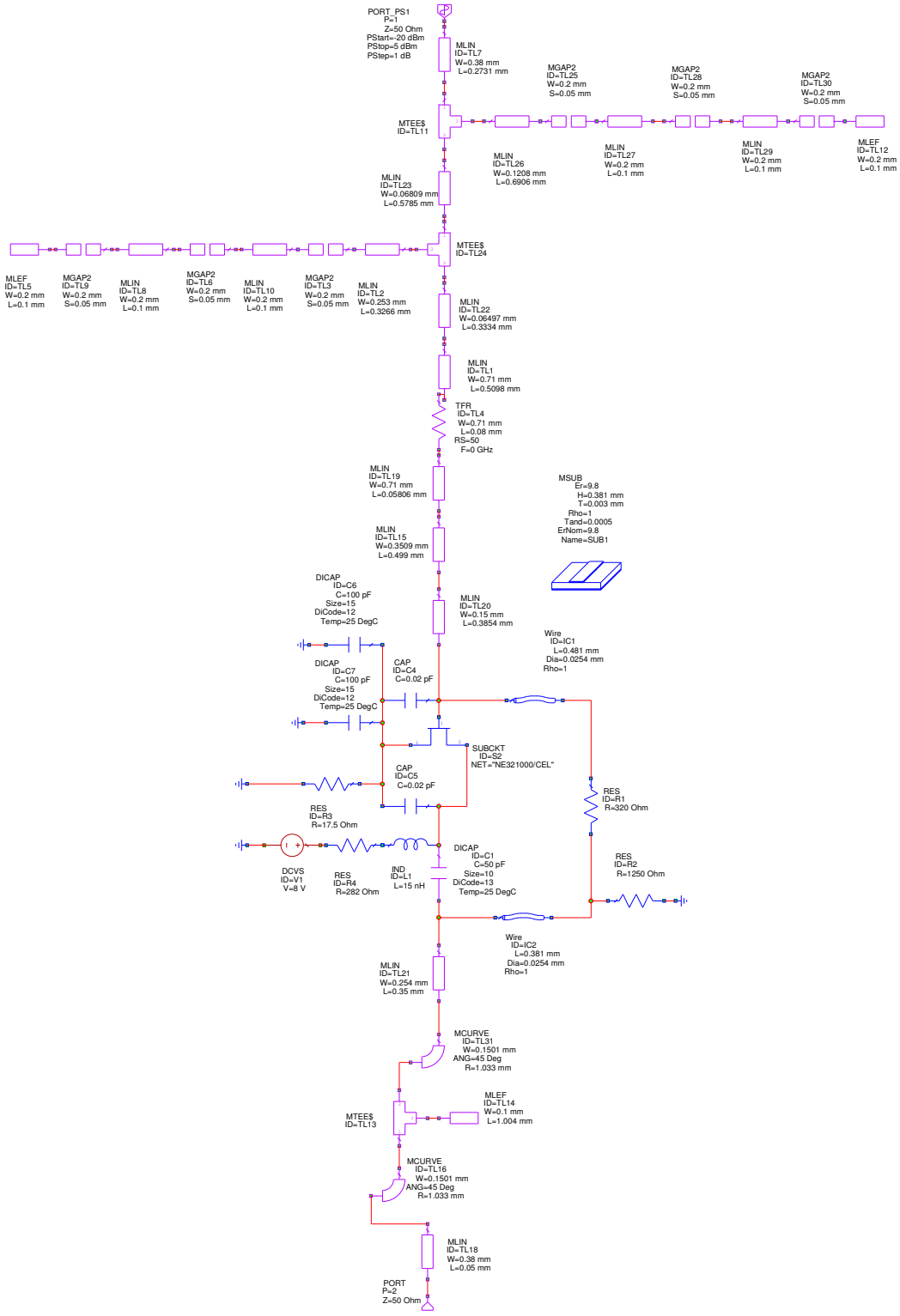


Figure F.4: Schematic layout of stage two

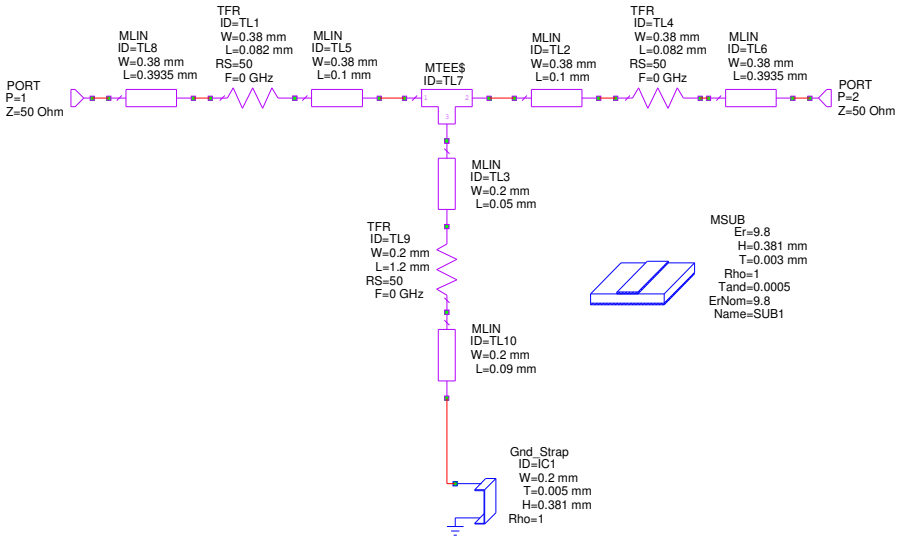


Figure F.5: Schematic layout of the second attenuator

Figure F.5 shows the schematic layout of the attenuator used between the second and third amplifier stages. Again the layout is very similar to the first attenuator. Subtle differences that may be observed are due to tuning and optimization of the attenuator as part the complete limiting amplifier design.

Figure F6 shows the amplifier following the second attenuator. The most apparent difference between this amplifier and the previously discussed amplifiers is the fact that the output circuit does not include any bends. This, being due to the specific position of the amplifier within the proposed *omega* type physical layout.

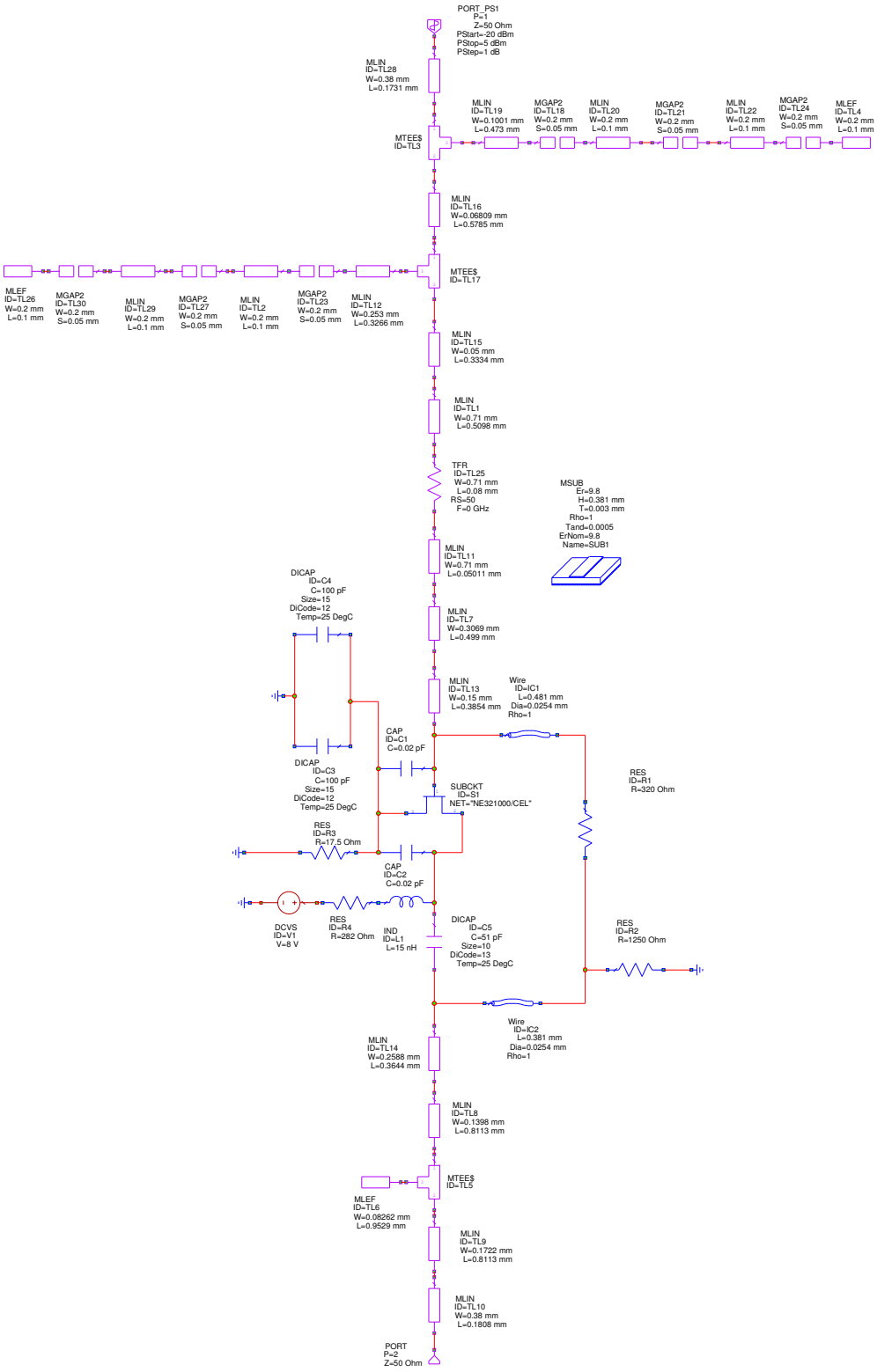


Figure F.6: Schematic layout of stage three

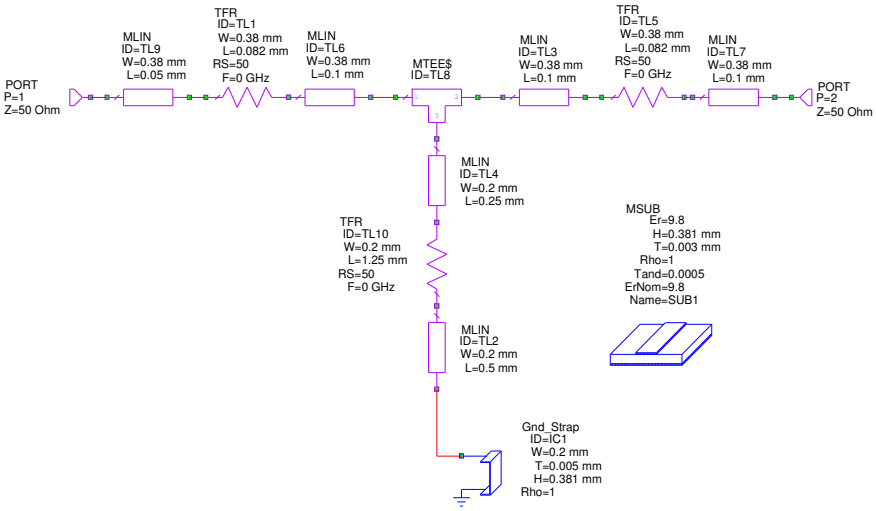


Figure F.7: Schematic layout of the third attenuator

Figure F.7 shows the schematic layout of the attenuator used between the third and fourth amplifier stages. Again the layout is similar to the previously discussed attenuators. Subtle differences that may be observed are again due to tuning and optimization of the attenuator as part the complete limiting amplifier design.

Figure F.8 shows the schematic layout of the amplifier following the third attenuator. This layout is again similar to the previously shown amplifiers.

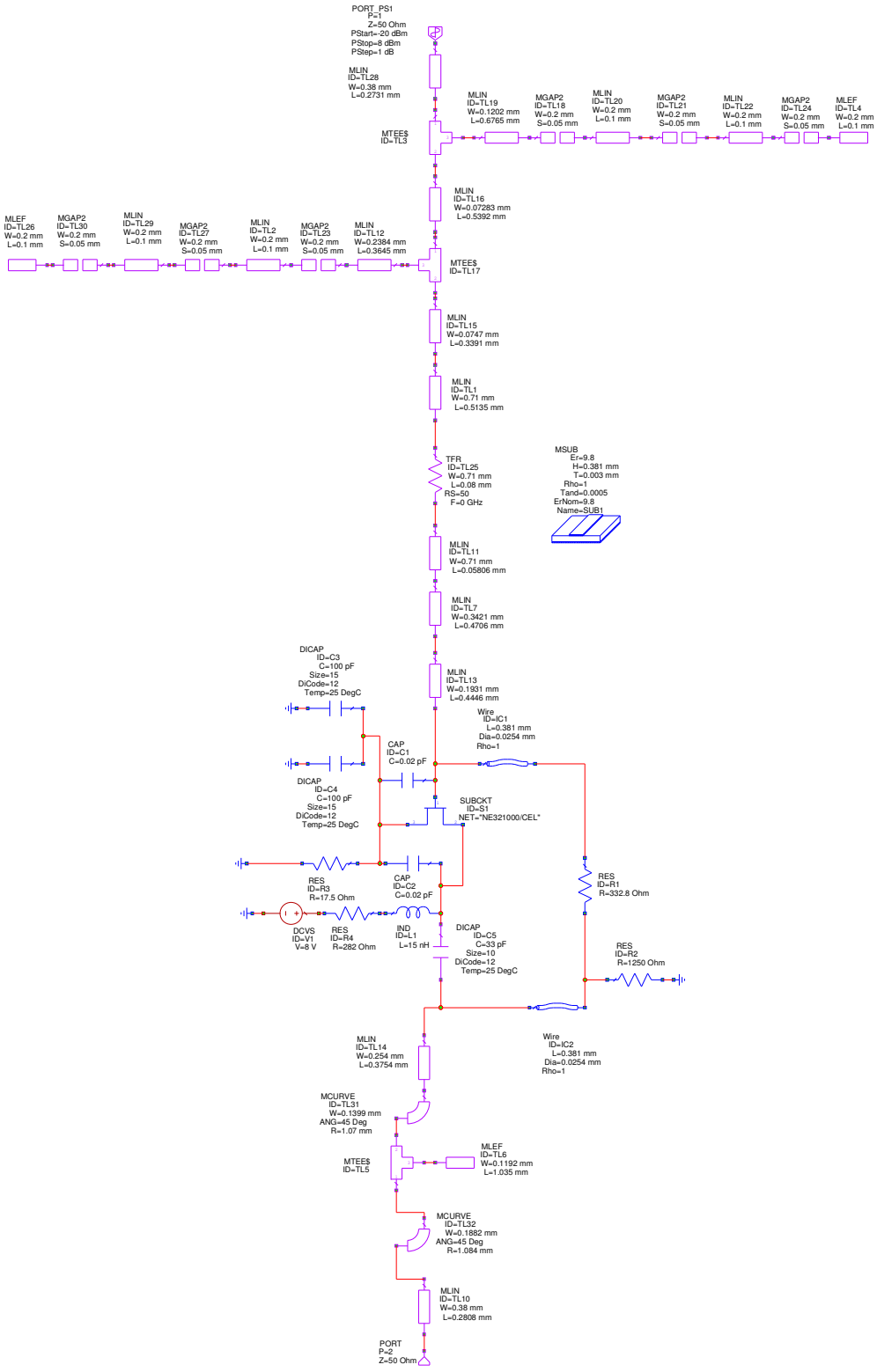


Figure F.8: Schematic layout of stage four

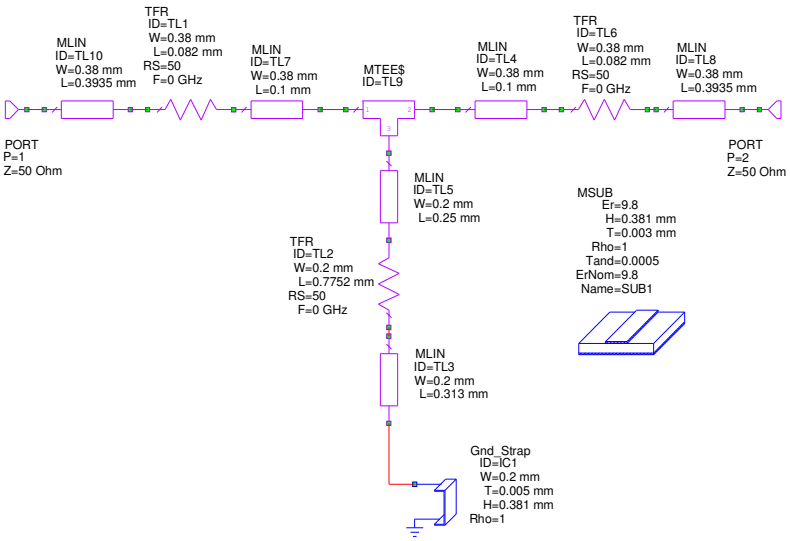


Figure F.9: Schematic layout of the fourth attenuator

Figure F.9 shows the schematic layout of the attenuator used between the fourth and fifth amplifier stages. Figure F.10 shows the schematic layout of the fifth amplifier stage which is also similar to the previously discussed amplifier stages. Figure F.11, on the other hand, shows the reconstructed two-stage amplifier after tuning and optimization. The schematic layout shows the associated input and output matching networks, while the interstage matching network is shown separate from the main design layout.

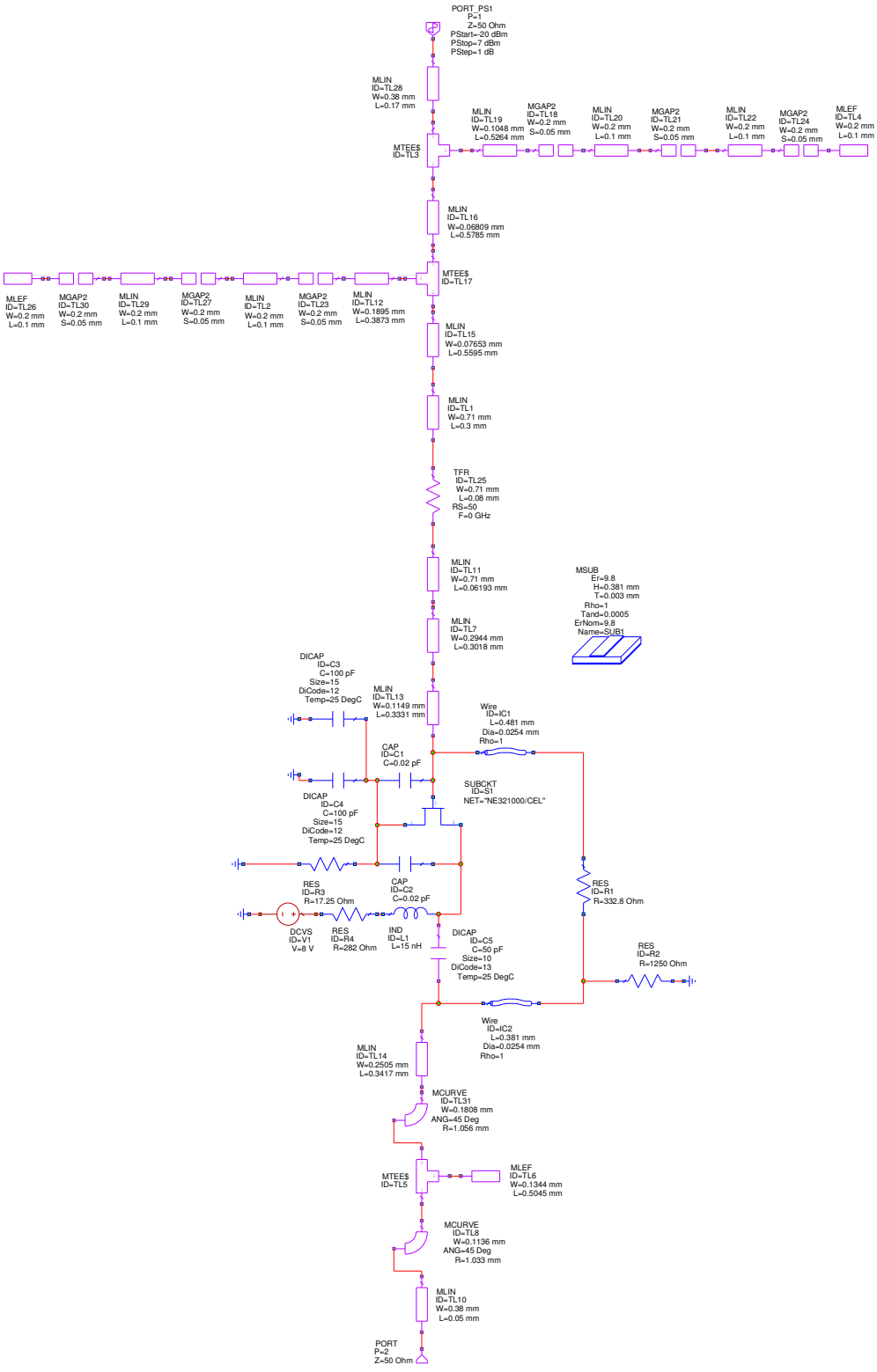


Figure F.10: Schematic layout of stage five

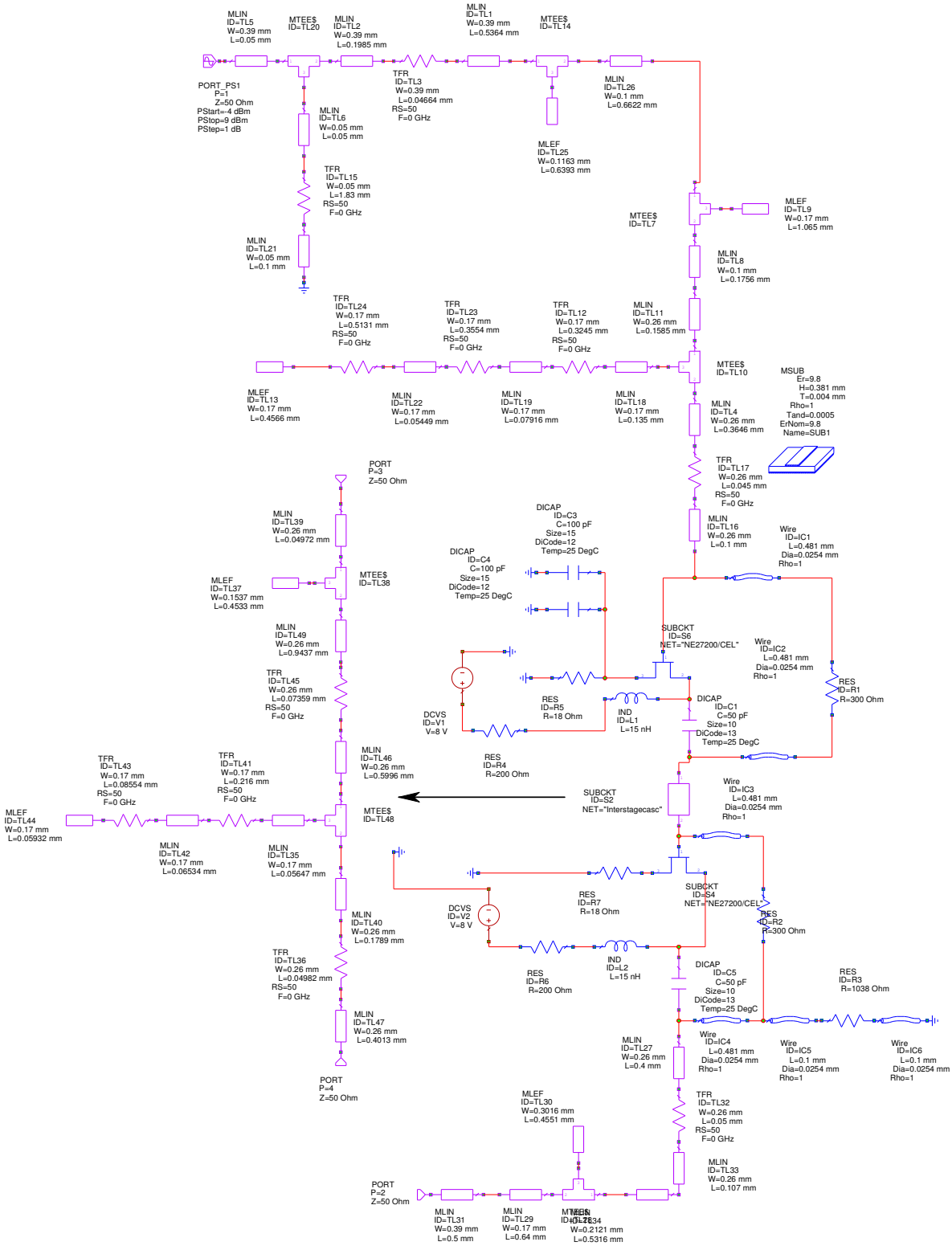


Figure F.11: Schematic layout of stage six

F.3 CONCLUSION

In this appendix, the schematic layouts of the different building blocks comprising the final designed limiting amplifier were given. This was done mainly to give better insight as to the actual design as done in MWO, while allowing for reconstruction of the complete design or portions thereof, if so required. Even though some of the building blocks are very similar, subtle differences between the different schematic layouts are observed. Differences between the four attenuators were mostly due to the tuning and optimization of the final design, but were also the result of achieving the desired physical layout of the design. Tuning and optimization also resulted in some subtle differences in the schematic layouts of the first five amplifiers. This was allowed for the particular purpose of breaking the uniformity of these amplifiers. Other differences in these amplifiers were introduced to ensure that the physical design layout could be achieved.