DMLS 3D-Printed Active Antenna Array

by

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Declaration

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Abstract

This thesis presents the development of an active antenna array for X-band and lower Ku-band frequencies (7.25-12.75 GHz) using modern additive manufacturing technologies. The single-polarized 2D planar antenna array consists of 64 Vivaldi antenna elements. The antenna elements are manufactured using a hybrid aluminium and low-loss dielectric approach. Each antenna element is integrated with an LNA, consisting of commercially available discrete transistors, directly at the feed of the antenna.

When terminated with the active antenna impedance, the LNA achieves a simulated noise figure of less than 1.3 dB for scan angles up to $\theta = 45°$. The active embedded element achieves a measured broadside gain of more than 14.7 dBi over the over frequency band.

Opsomming

Hierdie tesis beskryf the ontwikkeling van 'n aktiewe antenna skikking vir X-band en laer Ku-band frekwensies deur gebruik te maak van moderne 3D-druk tegnieke. Die enkel gepolariseerde planêre skikking bestaan uit 64 Vivaldi antenna elemente. Die antenna elemente bestaan uit 'n kombinasie van aluminium en 'n lae-verlies dielektrikum. Elke antenna word geïntegreer met 'n lae-ruis versterker by die voer van die antenna element. Die versterkers is vervaardig van kommersiëel beskikbare diskrete transistors.

Wanneer die ontwerpte lae-ruis versterker getermineer word met die aktiewe impedansie van die antenna skikking, is die gesimuleerde ruissyfer laer as 1.3 dB oor die hele frekwensie band tot 'n skanderings hoek van $\theta = 45°$. Die gemete aanwins van die antenna element in die omgewing van die antenna skikking is meer as 14.7 dBi oor die ontwerpte frekwensie band.

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Chapter 1

Introduction

Wide-band low-noise systems are used in applications where signals with very low power levels are received such as satellite communication, base stations and Radar.

The first component in the signal chain, often a low noise amplifier, is the most significant noise contributor to the system. A lossy component between the antenna and first stage LNA can further degrade the noise performance of the system. Therefore it is advantageous to add as little as possible lossy components between the antenna and LNA.

Vivaldi antennas are popular in wide-band phased arrays and have shown to achieve bandwidths of more than 10:1 when the elements are electrically connected [1]. This, however, can make it difficult to manufacture [1]. A promising technology for the manufacturing of antennas is the use of 3D printing. This can overcome manufacturing constraints that previously limited the creativity of the antenna designer.

1.1 Objectives

The aim of this project is to design an active antenna array by achieving the following objectives:

- Evaluate the use of metal 3D printing as a manufacturing technique for antennas, especially at small X-band and Ku-band dimensions.
- The integration of an LNA directly at the feed without the use of a matching circuit in an attempt to reduce minimum achievable noise figure. The antenna is designed to match as closely as possible to the optimum noise impedance of the integrated LNA.
- Develop a system that can be measured and compared to simulations to improve the simulation setup for the development of future active arrays. The antenna should further provide a reference performance for future active arrays to improve.

1.2 Overview

Chapter 2 introduces the necessary theoretical background for the successful implementation of an active antenna array. The chapter mainly consists of four parts: Antenna and antenna array theory, general noise and noise sources in systems, amplifier design theory and lastly active antennas. The antenna component of the active array is designed in

Chapter 3. Chapter 4 discusses the design of the low noise amplifier (LNA) integrated at the feed of the antenna. Chapter 5 performs the co-design of the antenna and LNA for increased system performance. Two active antenna prototypes are developed in Chapter 6, the first mainly for evaluation of the transistor in an array environment and secondly to establish a measurement setup whereas the second is the final array prototype. Chapter 7 presents the measured results of the final active antenna array. Finally, the thesis concludes in Chapter 8 with recommendations for possible future work.

Chapter 2

Literature Study

This chapter discusses the general theoretical background needed for the development of the active antenna array. Sections 2.2 to 2.5 discusses general antenna theory, ending with a more detailed discussion of Vivaldi antenna arrays. Section 2.6 introduce powder be infusion additive manufacturing techniques, Selective Laser Melting (SLM) and Direct Metal Laser Sintering (DMLS). Sections 2.7 to 2.8.5 are relevant for the low noise amplifier design. Finally, Section 2.9 discusses active antennas and antenna arrays and provide a method for measuring the absolute gain of these antennas in Section 2.10.

2.1 UV-Space

This section introduces the transformation between Spherical- and UV coordinate systems. U-V Coordinates is often used in Section 2.2 together with spherical coordinates during the discussion of grating lobes in antenna arrays. Figure 2.1 illustrates the relation between Spherical coordinates and the UV space.

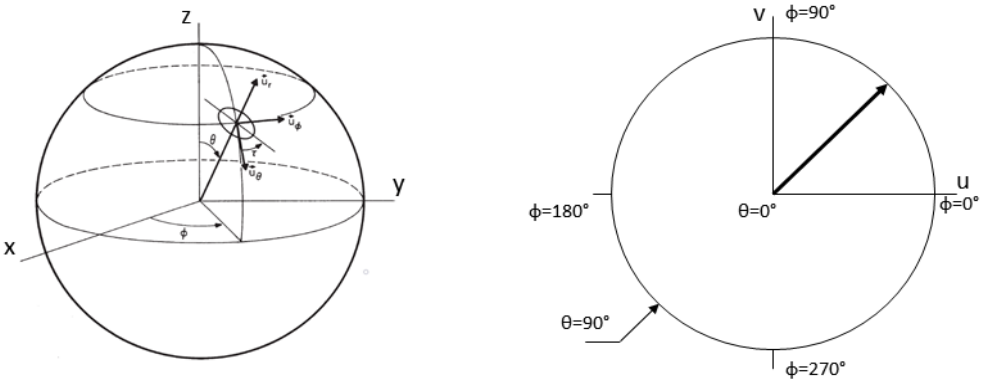


Figure 2.1: Spherical coordinate system represented in the UV-Space.

Mathematically, the transformation between Spherical- and UV coordinates are described by Equations 2.1 and 2.2.

$$u = sin\theta cos\Phi \tag{2.1}$$

$$v = sin\theta sin\Phi \tag{2.2}$$

This section briefly introduced the UV-space and its relation to spherical coordinates. The next section discusses grating lobes in regular antenna arrays.

2.2 Grating lobes in Regular Arrays

This section discusses the occurrence of grating lobes in regular [1] arrays with rectangular and triangular grid layouts. In phased arrays multiple main lobes can exist in the visible region depending on the element spacing and grid layout of the array. Grating lobes refer to the principle maximums that exist at angles other than the intended mainlobe direction. This causes power to be radiated in directions other than intended or power received from directions other than the scan angle of the phased array. This can lead to interference from the grating lobe direction which may for example cause a system that determines direction of arrival to fail. Note that grating lobes are not always negative and in some cases arrays are designed to have main lobes in multiple directions. This section also introduces the steering vector and calculation of phase contributions at each element as a function of the position in the array. These calculations are used in later chapters during the design process. Consider an array with a grid layout as shown in Figure 2.2.

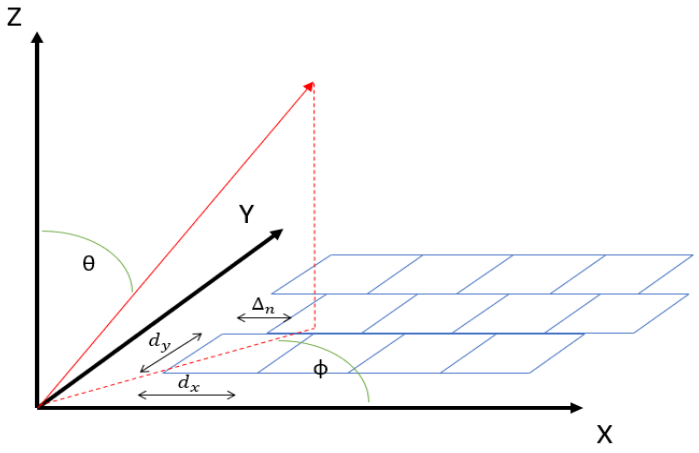


Figure 2.2: Grid Layout of a two-dimensional array with a Δ_n row offset [2].

The normalised far-field for this regular antenna array is [2]

$$\bar{E}(\bar{r}) = \frac{\bar{f}(\theta,\phi)}{N} \sum_m \sum_n a_{mn} e^{jk(umd_x + \Delta_n u + vnd_y)} \tag{2.3}$$

where $\bar{f}(\theta,\phi)$ is the vector element pattern,d_x the spacing in the x-axis, d_y the spacing in the y-axis, N the number of element, Δ_n the offset between rows of array elements as indicated in Figure 2.2 and a_{mn} the steering excitation of the form

$$a_{mn} = |a_{mn}| e^{jk_0(u_0 md_x + u_0\Delta_n + v_0 nd_y)} \tag{2.4}$$

where $k_0 = \frac{2\pi}{\lambda_0}$ and u_0, v_0 the steering angle or position of the main beam. Here λ_0 is the specific frequency at which the steering excitation is calculated. This however

[1] Array elements are periodically spaced in the x- and y-axis

will only result in correct steering at the specific frequency. Assuming that the element pattern $\bar{f}(\theta, \phi)$ and steering excitation a_{mn} are separable the far-field pattern becomes [2]

$$\bar{E}(\bar{r}) = \frac{\bar{f}_x(u)}{N_x}\left\{\sum_m |a_m^x| e^{j(ku-k_0u_0)md_x}\right\}\frac{\bar{f}_y(u)}{N_y}\left\{\sum_n |a_n^y| e^{j[(kv-k_0v_0)nd_y+\Delta_n(ku-k_0u_0)]}\right\}. \tag{2.5}$$

It is evident from Equation 2.5 that the terms $e^{j(ku-k_0u_0)md_x}$ and $e^{j[(kv-k_0v_0)nd_y+\Delta_n(ku-k_0u_0)]}$ represent the phase contributions to the array E-field as a function of element position and steering excitation referenced to the origin of the array.

When Equation 2.5 reaches a maximum, it either represents the main lobe or a grating lobe. As mentioned, usually, grating lobes are a negative consequence of wider element spacing. The remainder of Section 2.2 discusses two individual cases, namely the rectangular and triangular grid layout in more detail to show where grating lobes occur and how to prevent it from entering the visible region.

2.2.1 Rectangular grid layout

Section 2.2 introduced the general theoretical background of electric fields radiated by an array of antennas and the occurrence of grating lobes as a function of position in the array. This section discusses rectangular grid layouts where the offset spacing $\Delta_n = 0$. The normalized pattern for a uniformly exited array can be written as [2]

$$\bar{E}(\bar{r}) = \bar{f}_x(u)\left\{\frac{sin\left[N_x\pi d_x\left(\frac{u}{\lambda}-\frac{u_0}{\lambda_0}\right)\right]}{N_x sin\left[\pi d_x\left(\frac{u}{\lambda}-\frac{u_0}{\lambda_0}\right)\right]}\right\}\bar{f}_y(u)\left\{\frac{sin\left[N_y\pi d_y\left(\frac{v}{\lambda}-\frac{v_0}{\lambda_0}\right)\right]}{N_y sin\left[\pi d_y\left(\frac{v}{\lambda}-\frac{v_0}{\lambda_0}\right)\right]}\right\} \tag{2.6}$$

For a large array Equation 2.6 is maximum at $u = u_p$, and $v = v_q$. u_p and v_q are calculated as [2]

$$u_p = \frac{\lambda}{\lambda_0}u_0 + p\frac{\lambda}{d_x} \tag{2.7}$$

$$v_q = \frac{\lambda}{\lambda_0}v_0 + q\frac{\lambda}{d_y} \tag{2.8}$$

Equation 2.7 and Equation 2.8 reflect the positions of all the E-field maximums. It is important to note at this point that not all these maximums exist in real space and will therefore not all be radiated by the array. The real space criterion is as follows [2]

$$\begin{aligned} u^2 + v^2 &= sin^2\theta cos^2\phi + sin^2\theta sin^2\phi \\ &= sin^2\theta \\ &= 1 - cos^2\theta \end{aligned} \tag{2.9}$$

$$cos\theta = \sqrt{1-u^2-v^2} \tag{2.10}$$

Applying the equation above at maximums u_p and v_q leads to the criterion [2]

$$u_p^2 + v_q^2 < 1 \tag{2.11}$$

Substitute Equation 2.7 and Equation 2.8 into Equation 2.11

$$1 > \left(\frac{\lambda}{\lambda_0}u_0 + p\frac{\lambda}{d_x}\right)^2 + \left(\frac{\lambda}{\lambda_0}v_0 + q\frac{\lambda}{d_y}\right)^2 \tag{2.12}$$

The conditions for avoiding grating lobes can be derived from Equation 2.12 as [2]

$$\frac{d_x}{\lambda} < \frac{1}{u_0 + 1} \tag{2.13}$$

$$\frac{d_y}{\lambda} < \frac{1}{v_0 + 1} \tag{2.14}$$

2.2.2 Triangular grid layout

This section focus on the triangular grid layout and where grating lobes may occur. The most significant difference that distinguish the triangular grid layout from the rectangular grid layout is that every second row of elements are shifted by $\Delta_n = \frac{d_x}{2}$. Grating lobe positions in u do not change and are given by Equation 2.7. The closed-form E-field expression for $u = u_p$ with p $= \pm 1 \pm 3 \pm 5$ and Ny even [2]

$$\bar{E}_y(u_p, v) = \bar{f}_y(v)\left\{\frac{sin\left[\frac{N_y\pi d_y}{\lambda}(v - v_0)\right]}{N_y cos\left[\frac{\pi d_y}{\lambda}(v - v_0)\right]}\right\} \tag{2.15}$$

for even p the closed-form E-field expression is [2]

$$\bar{E}_y(u_p, v) = \bar{f}_y(v)\left\{\frac{sin\left[\frac{N_y\pi d_y}{\lambda}(v - v_0)\right]}{N_y sin\left[\frac{\pi d_y}{\lambda}(v - v_0)\right]}\right\} \tag{2.16}$$

The grating lobes for uneven p are different from the rectangular grid positions and are calculated as [2]

$$v = v_0 + \frac{\lambda}{d_y}\left(q + \frac{1}{2}\right) \tag{2.17}$$

2.2.3 Visual comparison of grating lobes in rectangular and triangular grid layouts

Section 2.2.1 and 2.2.2 focused on the mathematical background of grating lobes. This section aims to provide more insight into the mathematics by visually comparing grating lobe positions in a rectangular and triangular grid layout. The yellow dots indicate the principle maximums of the array far-field. The blue circle represent the visible region of the antenna and the red circle the position of the main lobe.

Figure 2.3a shows the grating lobe positions in the U-V space for $d_x = d_y = \lambda$. Here the grating lobes are on the edge of the visible region. Figure 2.3b shows the grating lobe positions for a triangular grid with $d_x = 1.15\lambda$ and $d_y = \lambda$ indicating that even with the element spacing of $d_x = 1.15\lambda$ the triangular grid still avoided grating lobes in the visible region. Wider element spacing allows the array antenna to use fewer elements for the same aperture size. The next section discusses the active reflection coefficient at the ports of array elements aided by the theory established in Section 2.2.

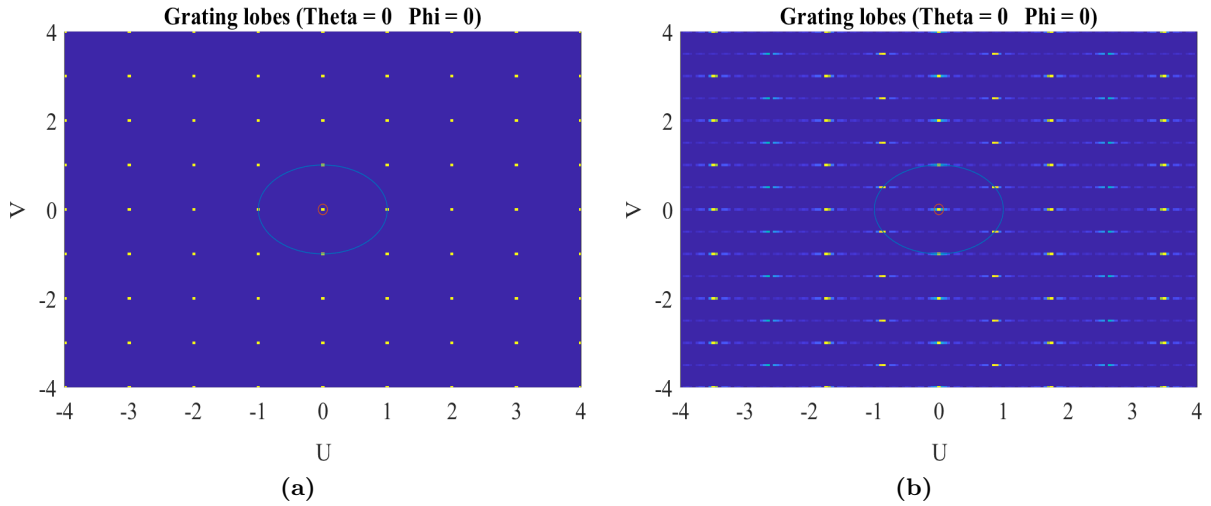


Figure 2.3: Grating lobe positions in a regular array scanned to broadside. (a) Rectangular grid with spacing $d_x = d_y = \lambda$. (b) Triangular grid with spacing $d_x = 1.15\lambda, d_y = \lambda$.

2.3 Active Reflection Coefficient

This section describes the calculation of the active reflection coefficient at the ports of the array elements from the S-Matrix of the antenna array. The derivation follows the work in [3]. Consider an array characterized by the S-matrix

$$S_{ij} = \frac{b_i}{a_j}\Big|_{a_k=0 for k=n} \tag{2.18}$$

where a_j is the incident voltage at j_{th} element and b_i the reflected voltage at the i_{th} element. The reflected voltage b_i is given by Equation 2.19

$$b_i = \sum_{j=1}^{N} S_{ij} a_j \tag{2.19}$$

.

From Equation 2.19 the active reflection coefficient at the i_{th} element is [3]

$$\Gamma_i = \frac{b_i}{a_i} = \frac{1}{a_i} \sum_{j=1}^{N} S_{ij} a_j \tag{2.20}$$

.

For a uniformly excited array at broadside, Equation 2.20 reduces to [3]

$$\Gamma_i = \frac{b_i}{a_i} = \frac{1}{a_i} \sum_{j=1}^{N} S_{ij} a_j = \sum_{j=1}^{N} S_{ij}. \tag{2.21}$$

For a specific scan angle the excitation a can be calculated with Equation 2.4 in Section 2.2 specifically Equation 2.4.

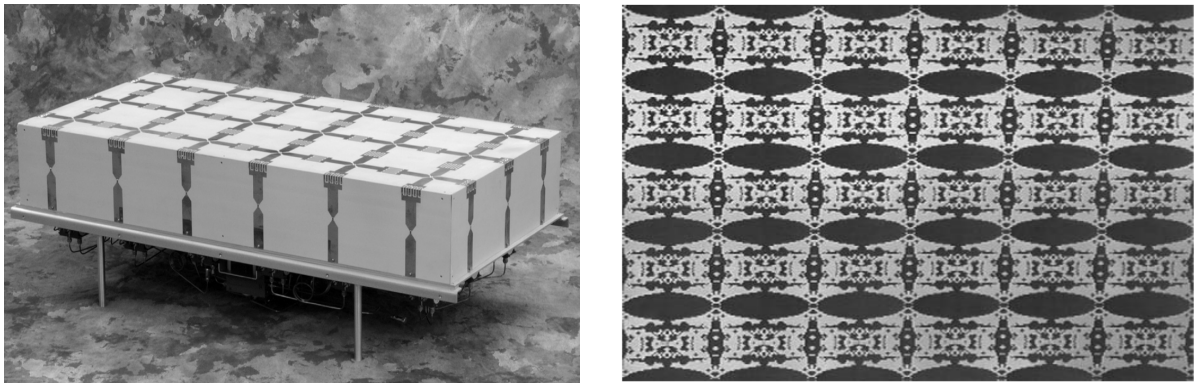
2.4 Wideband antenna arrays

Section 2.2 and 2.3 discussed general antenna array theory that included grid layout, phasing, grating lobes and the active reflection coefficient of an element when placed in an array environment. Section 2.2 and 2.3 however is mostly theoretical and therefore,

this section review practical examples of antenna arrays developed in previous work. Section 2.4.1 discusses Munk's Current Sheet Array, Section 2.4.2 Fragmented Aperture Arrays and Section 2.4.3 Tapered Slot Arrays. These wideband array technologies are all dependent on the mutual coupling between elements to operate over wide bandwidths.

2.4.1 Current Sheet Array

Historically antenna array elements were designed in isolation. In an array environment, mutual coupling effects are present between antenna elements and these effects were often seen as detrimental to element performance. The current sheet array was realised by Munk and Harris corporation [4], [5] and followed a fundamentally different approach by using mutual coupling between elements to extend the bandwidth of the array. The array consisted of small closely spaced dipoles capacitively connected to neighbouring elements through Interdigital capacitors. A prototype of this array is shown in Figure 2.4a



(a) **(b)**

Figure 2.4: Examples of wideband antenna arrays. (a) Munk's Current Sheet Array. (b) Fragmented Aperture Array [6]

Wheeler [7] examined the change in radiation resistance with scanning angles in the E- and H-plane of planar infinite current sheet. Munk's array of connected dipoles was a realisation of Wheeler's current sheet [7] and was named the CSA. The theoretical basis of this array was developed by analyzing the impedance contribution from every component(e.g. ground plane, antenna element) of the array and design them in such a way that it counteract each other to achieve wideband performance. This wideband matching technique is discussed in detail by Munk [8]. Several antenna arrays utilizing this technique were developed over the years, including the Dense Dipole Array [9] developed at Stellenbosch University.

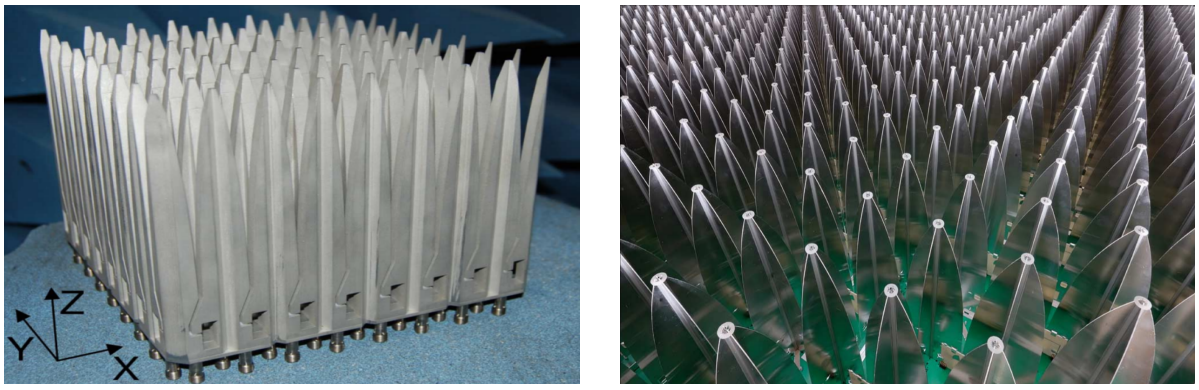
2.4.2 Fragmented Aperture Arrays

The development of Fragmented Aperture Arrays took place at Georgia Tech Research Institute during the same time as the CSA [6]. Fragmented Aperture Arrays follows a different design approach than conventional antenna design. A blank aperture is divided into a many small regions. A Genetic Algorithm determines which of these regions are metalized. The aperture layout is optimized until it reaches specific design goals. The remainder of the regions is left blank. This design methodology delivered successful

designs with bandwidths of up to 33:1 [10]. Figure 2.4b shows an example of a Fragmented Aperture Array.

2.4.3 Tapered Slot Arrays

Tapered slot arrays rely on the strong mutual coupling between antenna elements to achieve wideband performance. Early research demonstrated an 8x8 tapered slot array with a 5:1 bandwidth [11]. Gibson [12] presented a single element TSA with an exponential taper called the Vivaldi Aerial, and tapered slot antennas with exponential tapers adopted the name. Since these antennas were introduced advancements in computing led to extensive studies of the TSA. Multiple arrays have been developed, achieving bandwidths exceeding 10:1 [13]. Vivaldi antenna arrays are further discussed in detail in Section 2.5. Figure 2.5 shows two examples of tapered slot antenna arrays.



(a) **(b)**

Figure 2.5: Different tapered slot antenna configurations.(a) All-metal vivaldi antenna array [13] . (b) EMBRACE antenna array system [14].

2.5 Vivaldi antenna array

The previous section reviewed several wide-band antennas developed in the literature. As the development of a Vivaldi antenna array is the subject of this project, the current section discusses these arrays in more detail. Section 2.5.1 and 2.5.2 review the two main components of the Vivaldi antenna. These components that form the Vivaldi antenna are practically realised in several ways, and these techniques form the subject of Section 2.5.3. Lastly, Section 2.5.4 briefly reviews a few impedance anomalies associated with Vivaldi antenna arrays and how to prevent it during the design process.

2.5.1 Taper region

The taper region transforms the free space wave to the slot line impedance. Although the exponential taper is very common, there are several different taper profiles. Figure 2.6a shows a few taper profiles associated with TSA (Tapered Slot Array).

The exponential taper is associated with the Vivaldi antenna and is described by Equation 2.22. The parameters of Equation 2.22 are defined in Figure 2.6b.

$$y = C1e^{R_a z} + C2 \tag{2.22}$$

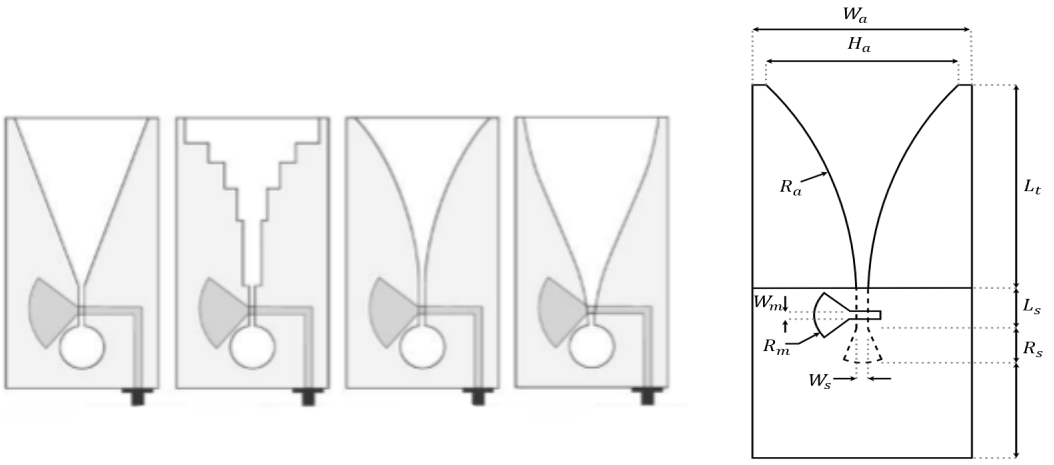


Figure 2.6: (a) Example taper profiles for tapered slot antennas [15] .(b) Vivaldi antenna dimensions.

where

$$C1 = \frac{H_a/2 - W_s/2}{e^{(R_a L_t)} - 1}$$

and

$$C2 = \frac{W_s e^{(R_a L_t)}/2 - H_a/2}{e^{(R_a L_t)} - 1}.$$

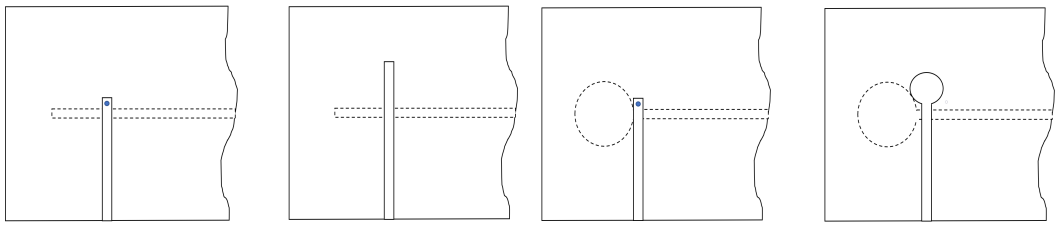
These parameters are defined as:

L_t	Length of the tapered region.
L_s	Length of the feed slot between the radial slot cavity and taper region.
R_a	Exponential opening rate of the tapered region.
H_a	Width of open region at the top of the taper region.
W_s	Width of the feed slot.
W_m	Width of the Microstrip feed line.
R_m	Microstip radial stub radius.
R_s	Radius of the slot cavity.

2.5.2 Vivaldi Feed

The feed of the Vivaldi antenna is implemented in a microstrip/stripline to slotline transition and in some cases as coaxial- to slotline [13]. Cohn [16] introduced the slotline as a transmission line and showed that simple integration with microstrip can be implemented by a right angled transition with the slotline etched in the groundplane of the micostrip. A few variations of microstrip to slotline transitions investigated by Schuppert [17] are shown in Figure 2.7.

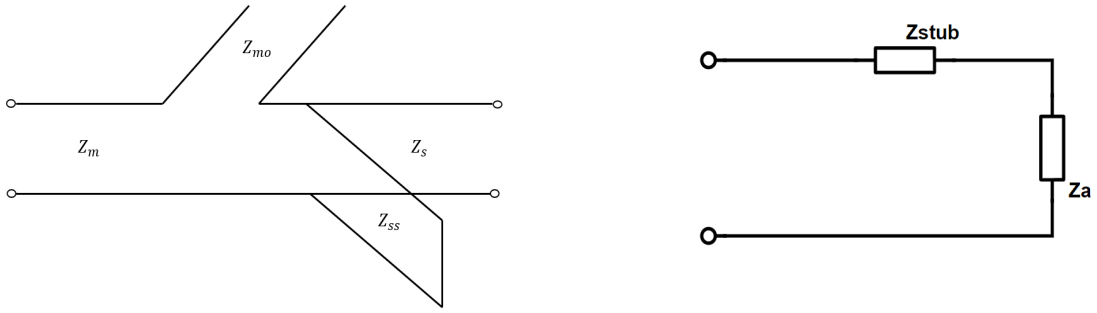
In Figure 2.7a a via physically connect the Microstrip to the edge of the slot. In Figure 2.7b a virtual short is created with a quarter wave stub. In the simplest case, the circuit diagram in Figure 2.8a provides useful insight into how this transition works. When the microstrip and slotline extend a quarter wavelength past the crossing, the slot transforms from short to open circuit and the radial stub from an open to short circuit. Various more accurate circuit models for this transition have been proposed [17], [18]. Shin and Schaubert [19] found that these circuit models are not accurate for tapered slot antenna



(a) (b) (c) (d)

Figure 2.7: Microstrip to slot line transitions investigted by Schuppert [17].

arrays due to strong mutual coupling between the taper regions and slot cavities between neighbouring elements. They suggested the use of the simple circuit model in Figure 2.8b.



(a) (b)

Figure 2.8: (a) Simplified transmission line circuit for microstrip to slot transition. (b) Equivalent circuit for Vivaldi antenna array [19].

In this model, the taper and slot cavity is modelled as a single component with impedance Z_a. The impedance of the stub is added in series with the antenna. This means the taper and slot cavity can be designed separately from the microstrip/stripline.

2.5.3 Manufacturing

So far, Section 2.5 discussed the taper region and microstrip/stripline transition of the Vivaldi antenna. These two components can, however, be implemented and manufactured in several different ways and still perform the same basic principles. This section reviews a few of these manufacturing techniques, together with some of their advantages and disadvantages. These techniques are a fully dielectric Vivaldi array as discussed in Section 2.5.3.1, a Vivaldi array completely manufacture of metal in Section 2.5.3.2 and a metal-dielectric hybrid antenna discussed in Section 2.5.3.3.

2.5.3.1 Dielectric

The antenna is entirely manufactured on printed circuit board. Exploded views of this antenna is shown in Figure 2.9a and 2.9b for the microstrip and stripline fed Vivaldi respectively.

Copper forms the taper and slot cavity region on one surface of the dielectric for the microstrip fed Vivaldi antenna and on both sides for the stripline fed Vivaldi. In the latter case, stripline feeds the antenna in the centre of the dielectric [20]. An advantage

(a) (b)

Figure 2.9: (a) Exploded view of microstrip fed full dielectric antenna. (b) Exploded view of stripline fed full dielectric antenna.

of this configuration is easy integration with electronics as part of the antenna on the same printed circuit board. A disadvantage of this configuration is the dielectric losses in the taper region of the antenna, and if expensive substrate material is used, it can significantly increase the cost of this antenna array.

2.5.3.2 Metal

The entire antenna is manufactured of metal. The advantage of this antenna is that there are no dielectric losses in the taper region of the antenna. The disadvantage of this antenna is that integration with the feed and electronics can be complicated. This array can also typically be more difficult to manufacture as a solid part. The antenna in Figure 2.5a is an example of this configuration.

2.5.3.3 Metal and dielectric Hybrid

This configuration combine metal and dielectric, such as in the EMBRACE [14] system shown in Figure 2.5b. The tapered region and slot cavity consist of metal. The dielectric with the microstrip circuit is added on the side of the metal where power couple from the microstrip to the metal antenna in the microstrip to slot transition. Advantages of this configuration include the benefits of not having dielectric losses in the taper region and still keeping the dielectric with microstrip for integration with electronics.

2.5.4 Impedance anomalies in Vivaldi antenna arrays

This section gives an overview of common impedance anomalies occurring in Vivaldi arrays. These are typically caused by faulty electrical contact, discussed in Section 2.5.4.1, scan blindness, discussed in Section 2.5.4.2 and anomalies associated with stripline fed Vivaldi arrays in Section 2.5.4.3. These anomalies can generally be avoided in the array if carefully designed and manufactured. Therefore this section serves as a reference guide for the designer to design with these restrictions in mind.

2.5.4.1 Mid-band impedance anomalies due to insufficient electrical contact between elements

Tapered slot antenna arrays have shown to have bandwidths exceeding 10:1 given that they are electrically connected to the neighbouring elements. When there is not sufficient electrical contact, a mid-band impedance anomaly exists as described in [21]. Gaps can occur unintentionally due to manufacturing errors or intentionally when elements are added independently in an array to allow replacement of faulty elements.

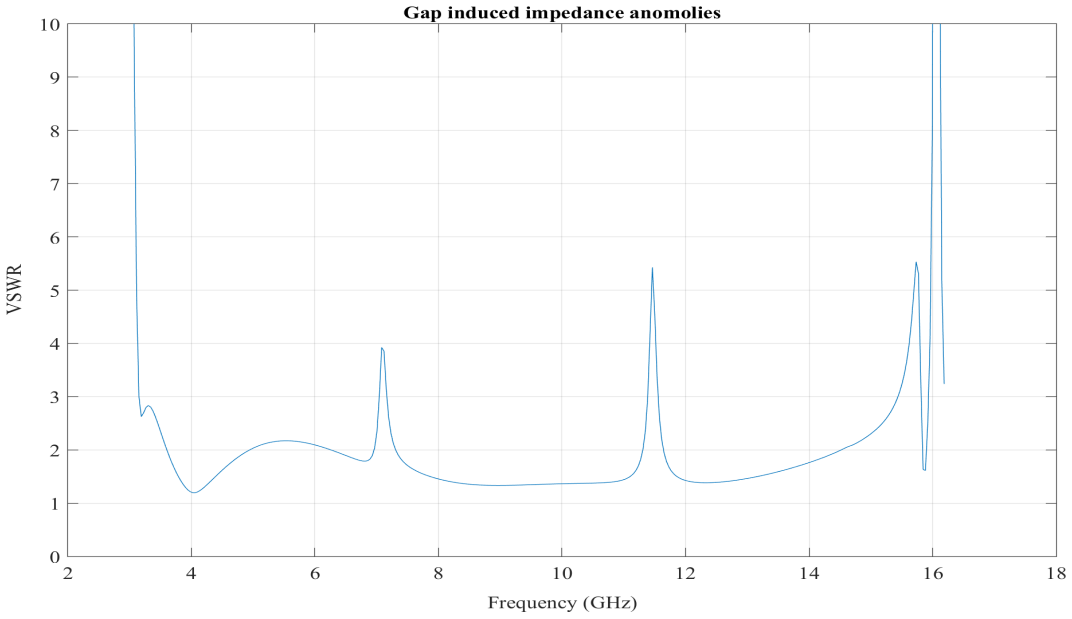


Figure 2.10: Mid-band impedance anomalies due to faulty electrical contact between adjacent elements.

2.5.4.2 Bandwidth limiting scan blindness

In linearly polarized tapered slot arrays impedance anomalies occur that limit the frequency band. These anomalies are described as scan blindness and happens when elements' H-plane spacing exceeds $\frac{\lambda_0}{2}$ [22]. Schaubert [23] suggested it is caused by a guided wave on the parallel plate structure formed by the 2D planar single polarised Vivaldi array and provided a model to predict these anomalies easily. To further provide insight into these upper band anomalies, a few parameter studies are performed. The parameters include E-plane spacing, H-plane spacing, height and scan angle. H-plane spacing has the most significant influence on this anomaly. The results of an infinite array simulation of a single-polarised Vivaldi array are shown in Figure 2.11 for different H-plane spacing.

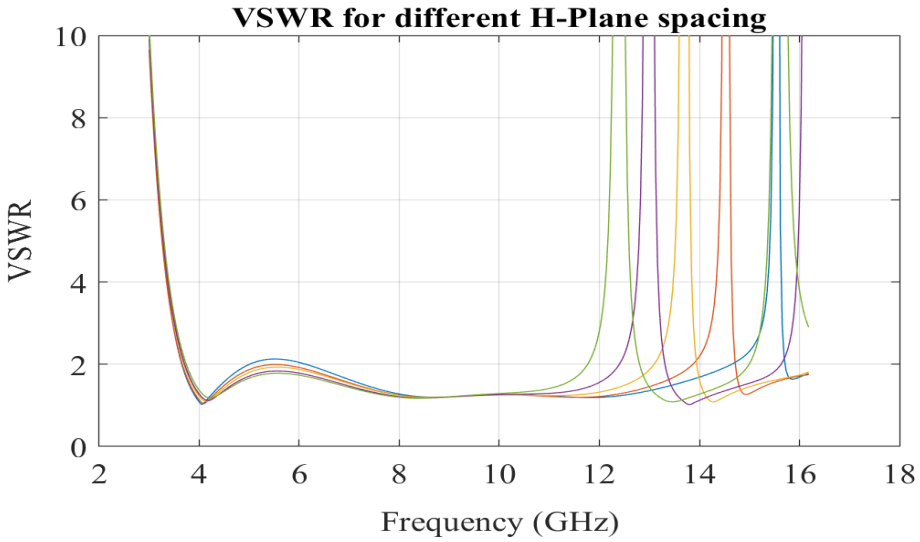


Figure 2.11: Different H-plane spacing.

Evaluating the results in Figure 2.11 shows that as the H-plane spacing decrease the anomaly shifts up in frequency.

2.5.4.3 Impedance anomalies in stripline fed TSA

Holter et al. [24] investigated a different set of mid-band impedance anomalies that occurs in stripline fed tapered slot arrays with copper on both sides of the dielectric. Results showed that the frequency of the anomaly is dependent on the size of the cavity formed by the dielectric region as the frequency where resonances occured moved to higher frequencies with the introduction of metal walls between elements to reduce the cavity size formed by the copper on the sides of the dielectric region [24]. The solution for the cavity resonance is to add vias around the taper region and slot cavity as shown in Figure 2.12. These vias decrease the size of the cavity and are more practical to fabricate than metal walls between elements [24].

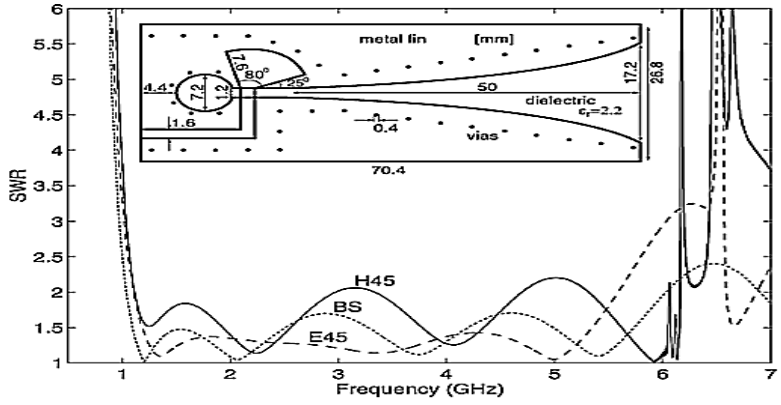


Figure 2.12: Introduced vias to remove mid-band impedance anomalies [24]

2.6 Selective Laser Melting (SLM) and Direct Metal Laser Sinthering (DMLS)

SLM and DMLS forms part of powder bed infusion additvive manufacturing technology. Figure 2.13 illustrates the basic manufacturing process of these technologies.

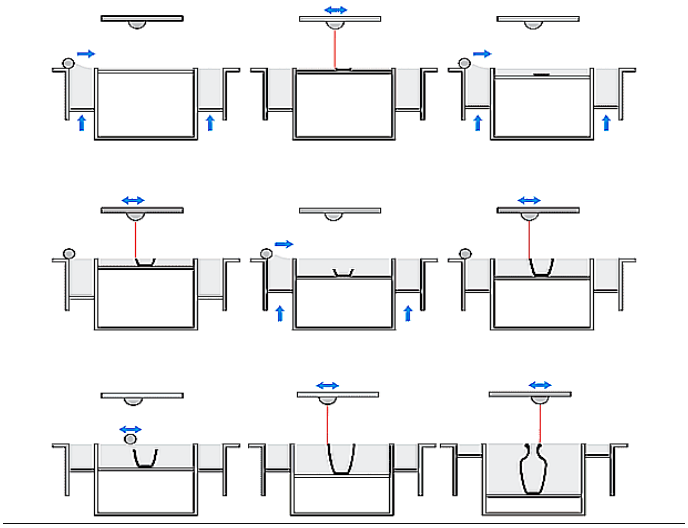


Figure 2.13: SLM/DMLS manufacturing process [25].

A CAD program divides the 3D model into several layers. During manufacturing of the part a thin layer of metal powder, as set in the CAD software, is deposited where high power laser beams sinter the powder into a solid part. When the specific layer has completed the bed that holds the metal powder lowers by a single layer thickness. Then, a new layer of powder is deposited, and the process repeats until the entire part is manufactured.

SLM/DMLS is used in many industries such as aerospace, automotive, medical and tooling [26]. It is also possible to manufacture different materials with the process of which a few include copper, aluminium, stainless steel, tool steel, cobalt, chrome, titanium and tungsten [26].

This metal additive manufacturing process has several advantages. Metal is built up from scratch, which means very little material is wasted in the manufacturing process. As mentioned, many materials can be manufactured with the same machine. It allows the manufacturing of more complex parts that means the designer has more freedom to deliver a more sophisticated design. Manufacturing can continue without human interaction after printing has started. Fast turnaround times which especially help with efficient prototyping.

There are, however, a few disadvantages. It is still costly to manufacture with these technologies. The maximum build size of the parts is still relatively small which limit the size of parts that can be printed [27].

This section concludes the theoretical background of antenna and array theory. The next section discusses general noise analysis in electronic devices.

2.7 Noise Analysis

Noise analysis is critical in the design of electronic devices such as low noise amplifiers. Noise is caused by random processes in devices and determines the smallest signal that can be received. Modelling of noise is essential to predict if the system meets the design goals and to determine the most significant noise contributors in the system. This chapter discusses noise analysis in electronic systems. The chapter begins by defining noise and the different types of noise that are present in electronic devices. Sections 2.7.4 and 2.7.5 introduce the noise correlation matrix - a useful tool to calculate noise in network analysis. The last section of the chapter discusses noise figure measurement with the Y-factor method.

2.7.1 Noise Figure Definition

A common definition for noise power added by a device is the noise factor F [28] defined as the ratio of the input to output SNR so that

$$F = \frac{S_i/N_i}{S_o/N_o}. \tag{2.23}$$

In ultra low noise systems the noise factor becomes small and is represented in decibel scale known as noise figure (NF) of the system.

$$NF = 10log(F) \tag{2.24}$$

The noise factor of an amplifier is [28]

$$F = \frac{S_i/N_i}{GS_i/G(N_i + N_a)} = 1 + \frac{N_a}{N_i} \tag{2.25}$$

where N_a is the noise power added by the amplifier referred to the input.

2.7.2 Types of Noise Sources

Several noise sources contribute to the overall noise of electronic devices. Some of the most significant noise contributions in amplifiers include thermal noise, shot noise and flicker noise. Flicker noise is dominant at low frequencies, but are insignificant at high frequencies. This section discusses thermal and shot noise in more detail.

2.7.2.1 Thermal Noise

Consider the resistor R at temperature T Kelvin in Figure 2.14a. When the temperature is not at absolute zero, a voltage is measured across the terminals of the resistor.

Planck's Blackbody radiation law give RMS voltage measured across the terminals of the resistor [28]

$$V_{RMS} = \sqrt{\frac{(4hfBR)}{e^{\frac{hf}{kT}} - 1}} \tag{2.26}$$

where

- h $= 6.626 \times 10^{-34} J.sec$ (Planck's constant)

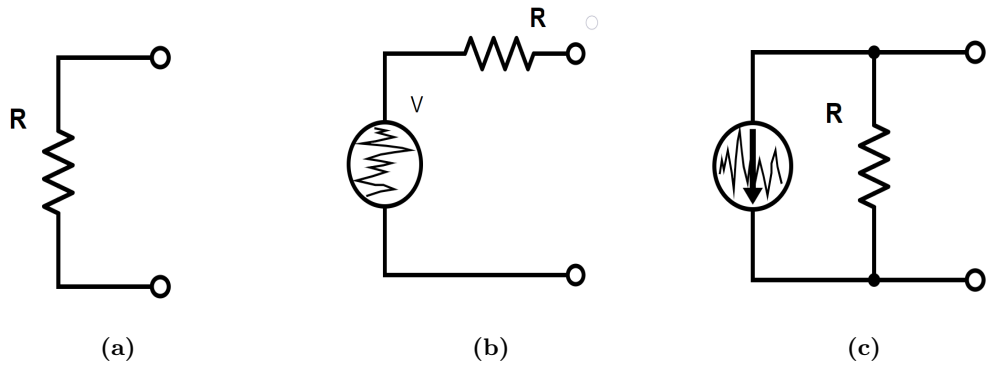


Figure 2.14: (a) Noisy Resistor at temperature $T°$. (b) Thevenin Equivalent of a noisy resistor. (c) Norton equivalent of a noisy resistor.

- k = 1.380×10^{-23}
- T = Temperature in Kelvin
- B = System Bandwidth (Hz)
- f = Center Frequency (Hz)
- R = Resistor Value

.

Equation 2.26 is simplified by using Taylor series to approximate the denominator as $e^{\frac{hf}{kT}} - 1 \approx \frac{hf}{kT}$. The result is shown in Equation 2.27 and is known as the Rayleigh-Jeans approximation [28]

$$V_{RMS} = \sqrt{4kTBR} \tag{2.27}$$

Figure 2.14b shows the Thevenin equivalent circuit of the resistor in Figure 2.14a. Alternatively, a noisy resistor can also be represented by a Norton equivalent circuit as shown in Fig 2.14c. The RMS noise current is given by Equation 2.28.

$$I_{RMS} = \sqrt{4kTBG} \tag{2.28}$$

where $G = \frac{1}{R}$. The corresponding PSD's (Power Spectral Densities) of thermal noise is given by Equation 2.29

$$S_v(f) \approx 2kTR \quad \frac{V^2}{Hz} \qquad S_I(f) \approx \frac{2kT}{R} \quad \frac{A^2}{Hz} \tag{2.29}$$

This approximation does not hold at very high frequencies or very low temperatures. When the resistor output is limited to a bandwidth $B(Hz)$ the available power P_n is equal to

$$Pn = \left(\frac{V_{RMS}}{2R}\right)^2 R = \frac{V_{RMS}^2}{4R} = kTB \tag{2.30}$$

Several conclusions can be made from Equation 2.30. The noise power is independent of frequency over the bandwidth where the Rayleigh-Jeans approximation is valid. The power spectral density does not change with frequency i.e. it is considered white noise. Visible in Equation 2.30 is that the power available from the resistor increases with

bandwidth and temperature. These characteristics of a noisy resistor make it useful as a representation of sources of white noise in electronic systems, especially given their dependence on temperature. The noise contribution of electronic devices is often characterized by their equivalent noise temperature T_e (K) [28]. The equivalent temperature T_e(K) can be used as an alternative to the noise factor defined in Section 2.7.1 for characterization of noise added by a device. The equivalent temperature T_e and noise factor F are related by

$$T_e = (F-1)T_0 \tag{2.31}$$

where noise figure is defined for a temperature of $T_0 = 290K$. The measured voltage across a noisy resistor follows a Gaussian distribution. According to the central limit theorem when a large number (tends towards infinity) of random variables are added together under certain assumptions, it results in a Gaussian distribution. Thermal noise is potential fluctuations caused by random movement of electrons due to heat and therefore a physical explanation of why thermal noise is a Gaussian distribution. Figure 2.15 shows a normal distribution. Thermal noise has a zero mean thus $\mu = 0$.

The Gaussian probability density function is as follows:

$$p(y) = \frac{1}{\sqrt{2\pi\sigma^2}} e^{\frac{-(y-\mu)^2}{2\sigma^2}} \tag{2.32}$$

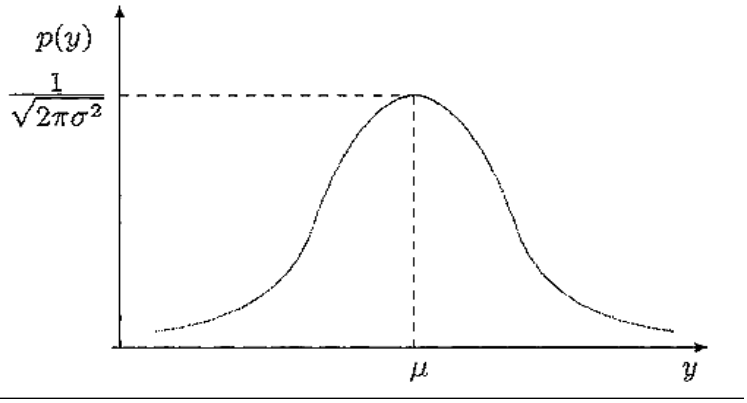


Figure 2.15: Normal distribution around μ.

2.7.2.2 Shot Noise

Shot noise occurs when a barrier, for example in a PN Junction, is crossed by charge carriers. Although the charge carriers cross the barrier at an average rate set by the mean current flow, the charge carriers still cross the barrier randomly at certain instants in time. Figure 2.16 shows this phenomenon. The PSD for shot noise is given by Equation 2.33 [30].

$$S(f) \approx q\bar{I} + \bar{I}\delta(f) \qquad \frac{A^2}{Hz} \tag{2.33}$$

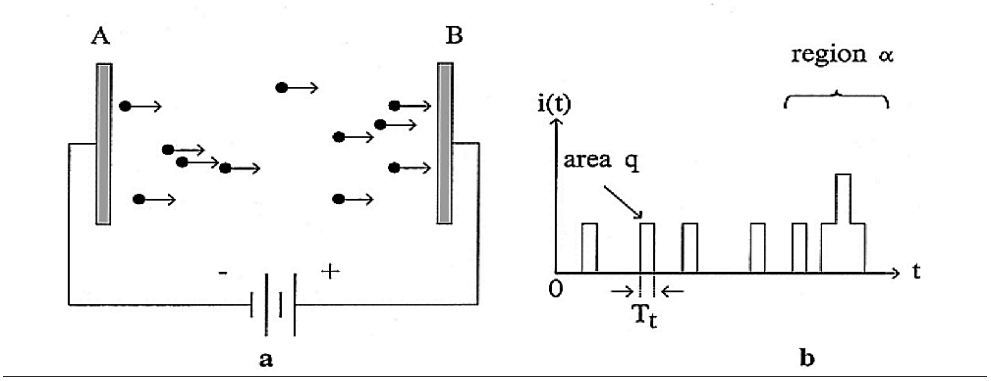


Figure 2.16: Simplified illustraion of Shot Noise [29].

$\bar{I}$ is the mean current and $q = 16 \times 10^{-19}C$. Notice that the second term in Equation 2.33 represents the DC bias. That is usually not of interest and shot noise is often approximated as [30]

$$S(f) \approx q\bar{I} \qquad \frac{A^2}{Hz} \tag{2.34}$$

The mean square value of the noise current is given by [29]

$$\overline{i_{sh}^2} = 2q\bar{I}B \tag{2.35}$$

.

2.7.3 Noise Model for a Bipolar Transistor

Sections 2.7.2.1 and 2.7.2.2 introduced two types of noise present in electronic components and how to model these noise sources. This section serves as an example of how to use these noise sources to model the total contribution of noise by a device. Figure 2.17 shows the simple noise small-signal model of a bipolar transistor and the relevant thermal and shot noise sources.

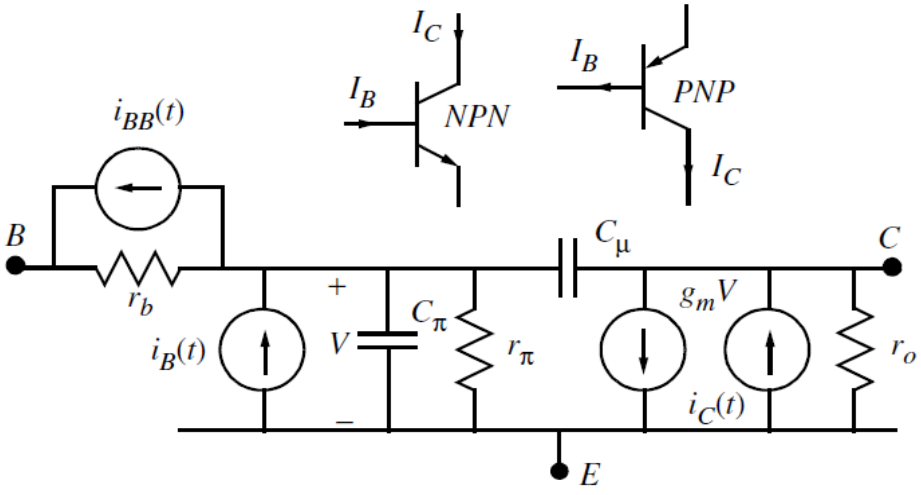


Figure 2.17: Noise model for a bipolar transistor [30].

A description of the noise sources are as follows [30]:

- i_{BB} model base spreading resistance noise.
- i_B shot noise due to base current.
- i_C shot noise due to collector current.

The PSD for each of these sources are given as [30]:

- $S_{BB}(f) = \frac{2kT}{r_b} \quad A^2/Hz$
- $S_B(f) = qI_B \quad A^2/Hz$
- $S_C(f) = qI_C \quad A^2/Hz$

The noise contribution of the resistance r_0 is usually small enough to be ignored in most cases [30]. An equivalent noise source for the transistor can be calculated by referring these sources to the in or output.

2.7.4 Noise Correlation

2.7.4.1 Auto-correlation

The auto-correlation of a function is defined as

$$R_{xx}(\tau) = \lim_{T\to\infty} \frac{1}{2T} \int_{-T}^{T} x(t)^* x(t+\tau) dt. \tag{2.36}$$

When the time lag $\tau = 0$ Equation 2.36 reduces to

$$R_{xx}(0) = \lim_{T\to\infty} \frac{1}{2T} \int_{-T}^{T} x(t)^* x(t) dt =< xx* > . \tag{2.37}$$

The PSD and auto-correlation function are related through the Fourier transform.

$$S_{xx}(f) = \mathcal{F}(R_{xx}(\tau)) \tag{2.38}$$

The total power in the signal is calculated by integrating the PSD over bandwidth.

$$\bar{P} = \int_{-\infty}^{\infty} S_{xx}(f) df \tag{2.39}$$

2.7.4.2 Noise Correlation Matrix

The Noise Correlation Matrix is useful for noise calculations in network analysis. Noise is random, and the instantaneous amplitude cannot be predicted. For this reason, statistical properties are used to characterize these random processes.

A noisy two-port network can be represented by a noiseless two-port network with two noise sources to model noise contribution from the two-port. These representations are shown in Table 2.1 for commonly known Y, Z and Chain networks. As described in Equation 2.38, the auto- and cross power spectral densities can be calculated from the

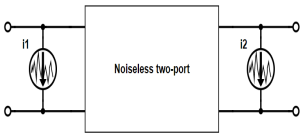
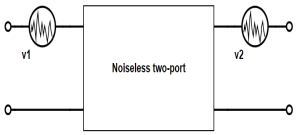
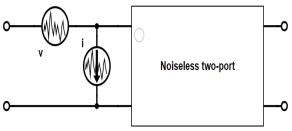
Descriprion	Admittance	Impedance	Chain
Noise Equivalent			
Correlation Matrix	$C_Y = \begin{bmatrix} C_{i1i1^*} & C_{i1i2^*} \\ C_{i2i1^*} & C_{i2i2^*} \end{bmatrix}$	$C_Z = \begin{bmatrix} C_{v1v1^*} & C_{v1v2^*} \\ C_{v2v1^*} & C_{v2v2^*} \end{bmatrix}$	$C_A = \begin{bmatrix} C_{vv^*} & C_{vi^*} \\ C_{iv^*} & C_{ii^*} \end{bmatrix}$
Electrical Matrix	$Y = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}$	$Z = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}$	$A = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix}$

Table 2.1: Correlation matrix representations for noisy Z,Y and Chain networks [31].

auto- and cross-correlations by taking the Fourier transform of these functions. Equation 2.40 describes the relation between the noise sources and the Correlation Matrix [31]

$$< s_i s_j* >= 2\Delta f C_{s_i s_j*} \qquad i,j = 1,2 \tag{2.40}$$

using the relation in Equation 2.40 the Correlation matrix as defined Hillbrand and Russer [31]

$$C = \frac{1}{2\Delta f} \begin{bmatrix} \langle s_1\ s_1^* \rangle & \langle s_1\ s_2^* \rangle \\ \langle s_1\ s_2^* \rangle & \langle s_2\ s_2^* \rangle \end{bmatrix} \tag{2.41}$$

where s_1 and s_2 represent the two noise sources and can either represent the current or voltage source. The correlation matrix for different two port networks is summarized in Table 2.1.

Two current sources are added to the admittance network, two voltage sources for the impedance network and a voltage and current source to the Chain network. Different two-port representations can be transformed between each other with Equation 2.42 [31]

$$C_{new} = TC_{old}T^{\dagger} \tag{2.42}$$

where (†) indicate the Hermitian. The matrix T is defined in Table 2.2. [31]

When multiple two ports are connected in series, parallel or cascade the combined correlation matrix can be calculated with Equations 2.43-2.44 [31]

$$C_Y = C_{Y1} + C_{Y2} \tag{2.43}$$

$$C_Z = C_{Z1} + C_{Z2} \tag{2.44}$$

$$C_A = A_1 C_{A2} A_1^{\dagger} + C_{A1} \tag{2.45}$$

where A is the first lossless two port network in the cascaded network.

Descriprion	Admittance	Impedance	Chain
Admittance	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}$	$\begin{bmatrix} -Y_{11} & 1 \\ -Y_{21} & 0 \end{bmatrix}$
Impedance	$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & -Z_{11} \\ 0 & -Z_{21} \end{bmatrix}$
Chain	$\begin{bmatrix} 0 & A_{12} \\ 1 & A_{22} \end{bmatrix}$	$\begin{bmatrix} 1 & -A_{11} \\ 0 & A_{21} \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$

Table 2.2: Transformation matrices between different network representations [31].

2.7.5 Noise parameter relation to noise correlation matrix

The previous section served as an introduction to the noise correlation matrix and noisy two-port networks. The section discusses the relation of the correlation matrix to well-known noise parameters generally provided in datasheets of low noise amplifiers. Figure 2.18 shows the noise currents referred to the input with the addition of the noise from the input current source.

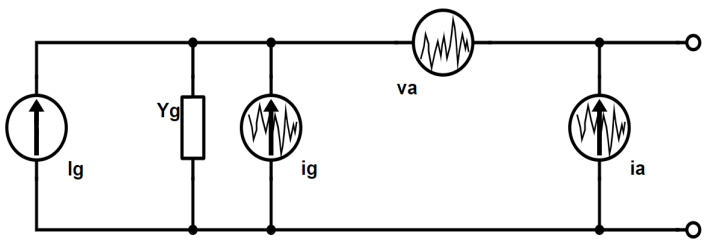


Figure 2.18: Noise sources referred to the input [32].

v_A and i_A are not necessarily uncorrelated and can be written as [32]

$$i_A = Y_{cor} v_A + i_u \tag{2.46}$$

$$Y_{cor} = \frac{\overline{v_A i_A^*}}{v_A^2} \tag{2.47}$$

where Y_{cor} represent the correlation factor between i_A and v_A. i_u and v_A are uncorrelated. The noise figure can be expressed in noise currents and voltages as [32]

$$F = \left|\frac{i_G}{i_G}\right|^2 + \left|\frac{i_A + Y_G v_A}{i_G}\right|^2. \tag{2.48}$$

Using Equation 2.46 we can write Equation 2.48 as [32]

$$F = 1 + \left|\frac{Y_{cor} v_A + i_u + Y_G v_A}{i_G}\right|^2. \tag{2.49}$$

The noise currents and voltages can be written in equivalent noise resistances where [32]

$$i_G^2 = 4kTBG_G \tag{2.50}$$

$$i_u^2 = 4kTBG_u \tag{2.51}$$

$$v_A^2 = 4kTBR_n. \tag{2.52}$$

Equation 2.49 can be written as [32]

$$F = 1 + \frac{G_u}{G_G} + \frac{R_n}{G_G}[(G_G + G_{cor})^2 + (B_G + B_{cor})^2]. \tag{2.53}$$

From Equation 2.53 it is visible that the noise factor is dependant on the source impedance. To calculate the optimum noise impedance of the two port that would result in minimum noise figure can be achieved by differentiating Equation 2.53 by R_G and X_G

$$\frac{dF}{dR_G}\Big|_{R_G,opt} = 0 \tag{2.54}$$

$$\frac{dF}{dX_G}\Big|_{X_G,opt} = 0 \tag{2.55}$$

which gives the noise parameters [32]

$$R_{opt} = \sqrt{\frac{R_u}{G_n} + R_{cor}^2} \tag{2.56}$$

$$X_{opt} = -X_{cor} \tag{2.57}$$

$$F_{min} = 1 + 2G_n R_{cor} + 2\sqrt{R_u G_n + (G_n R_{cor})^2} \tag{2.58}$$

The noise factor in terms noise parameters and source impedance

$$F = F_{min} + \frac{G_n}{R_G}|Z_G - Z_{opt}|^2 \tag{2.59}$$

and in terms of source admittance

$$F = F_{min} + \frac{R_n}{G_G}|Y_G - Y_{opt}|^2 \tag{2.60}$$

The first part of this section derived a relation between commonly used noise parameters and the noise sources in a noisy ABCD network. For noise calculations of a system

consisting of multiple two-port networks correlation matrix calculations is more convenient than noise parameters. The ABCD noise correlation matrix can be calculated from the noise parameters as [31]

$$\mathbf{C_A} = 2kT \begin{bmatrix} R_n & \frac{NF_{min}-1}{2} - R_n Y^*_{opt} \\ \frac{NF_{min}-1}{2} - R_n Y_{opt} & R_n|Y + opt^2| \end{bmatrix}. \tag{2.61}$$

2.7.6 Y-Factor measurement of effective noise temperature

Measurement of noise power in practical applications is not possible because the input noise power is not zero due to the fact it would not be possible to keep the input matched load at 0K. This section describes a method to measure the equivalent temperature of the device by adding two noise sources with distinct equivalent temperatures at the input of the device.

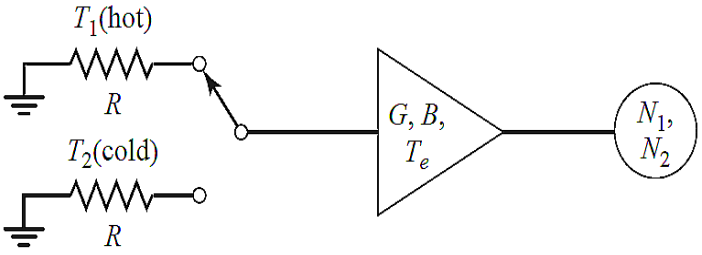


Figure 2.19: Illustration of Y-Factor Method for measuring effective noise temperature [28].

Here T_1 and T_2 is the equivalent temperatures of the hot and cold loads. T_e the equivalent noise temperature of the device, G the gain of the device and B the system bandwidth and T_e the noise equivalent temperature. The output noise power for T_1 presented at the input is [28]

$$N_1 = GkT_1B + GkT_eB \tag{2.62}$$

The output noise power for T_2 presented at the input is [28]

$$N_2 = GkT_2B + GkT_eB \tag{2.63}$$

The ratio of the output power for T_1 and T_2 defines the Y-factor as solved from Equations 2.62 and 2.63 [28]

$$Y = \frac{N_1}{N_2} = \frac{T_1 + T_e}{T_2 + T_e} > 1. \tag{2.64}$$

Finally T_e can be calculated as

$$T_e = \frac{T_1 - YT_2}{Y - 1} \tag{2.65}$$

Accuracy of these measurements are improved by choosing distinct values for T_1 and T_2 [28].

2.8 Amplifier Design Theoretical Background

A number of characteristics are important when designing low noise amplifiers. The purpose of this chapter is to introduce a few of these characteristics such as the amplifier gain definitions, stability and linearity.

Figure 2.20 shows the reference planes of $\Gamma_s, \Gamma_{in}, \Gamma_{out}$ and Γ_L used in the discussions of the above mentioned amplifier characteristics [28].

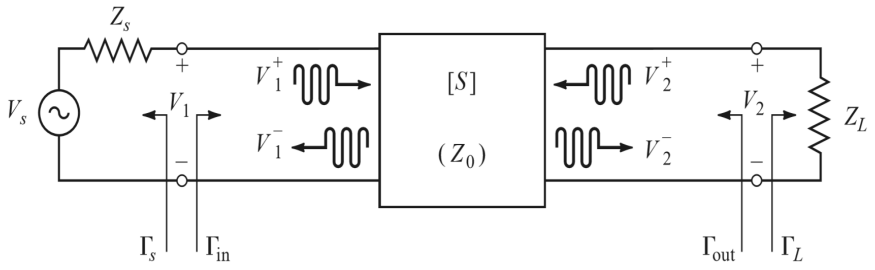


Figure 2.20: Measurement planes for general two-port circuit [28].

2.8.1 Two-Port Power Gain

This section defines three gain definitions. Power gain G, available power gain G_A and Transducer power gain G_T [28].

Power Gain is defined as the power delivered to the load divided by the power accepted by the two-port.

$$G = \frac{|S_{21}|^2(1-|\Gamma_L|^2)}{(1-|\Gamma_{in}|^2)|1-S_{22}\Gamma_L|^2} \tag{2.66}$$

Available power gain refers to the gain between the power from the source and the power at the output of the device. This definitions include mismatches at the input of the two-port.

$$G_A = \frac{|S_{21}|^2(1-|\Gamma_S|^2)}{|1-S_{11}\Gamma_S|^2(1-\Gamma_{out}|^2)} \tag{2.67}$$

Transducer power gain is the measure of the gain between the source and the power dissipated in the load. This definition is very useful as it includes all mismatches at the input and the output of the amplifier.

$$G_T = \frac{|S_{21}|^2(1-|\Gamma_S|^2)(1-|\Gamma_L|^2)}{|1-\Gamma_S\Gamma_{in}|^2|1-S_{22}\Gamma_L|^2} \tag{2.68}$$

2.8.2 Stability Analysis

This section describes stability considerations in the design of a low noise amplifier. Two classes of stability exist. The device can either be unconditionally stable or potentially unstable. It is defined as follows [28]:

- Unconditionally stable: $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ for all combinations of source and load impedances.

- potentially unstable: $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ for certain combinations of source and load impedances.

Based on the definitions of Γ_{in} and Γ_{out} a device is unconditionally stable when

$$|\Gamma_{in}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \tag{2.69}$$

and

$$|\Gamma_{out}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{11}\Gamma_S} \right| < 1. \tag{2.70}$$

This result can be represented with a Smith chart by plotting the regions for the source and load impedance where the inequality in Equation 2.69 and Equation 2.70 holds. The output stability circle centre C_L and radius R_L is calculated as [28]

$$C_L = \frac{(S_{22} - \Delta S_{11}^*)}{|S_{22}|^2 - |\Delta|^2} \tag{2.71}$$

and

$$R_L = \left| \frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2} \right|. \tag{2.72}$$

The input stability circle centre C_S and radius R_S are calculated as[28]

$$C_S = \frac{(S_{11} - \Delta S_{22}^*)}{|S_{11}|^2 - |\Delta|^2} \tag{2.73}$$

and

$$R_S = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right|. \tag{2.74}$$

Δ in Equations 2.71-2.74 are defined as

$$\Delta = S_{11}S_{22} - S_{12}S_{21}.$$

Two well-known tests for unconditional stability exist. The μ-factor and $K - \Delta$ test. The $K - \Delta$ test requires [28]

$$K = \frac{1 - |S_{11}|^2 - |S_{22}| + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{2.75}$$

and

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{2.76}$$

to be satisfied for the frequency range the designer requires to be unconditionally stable. The second test for unconditional stability requires [28]

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1. \tag{2.77}$$

The μ-test does not only calculate if the device is unconditionally stable but also determines the degree of stability. A larger value of μ means the device is more stable.

When the device is potentially unstable stability circles should be used to determine the impedance that may result in an unstable device. More insight into the theoretical basis developed in this section is gained in Section 4.3 through the practical design of the low noise amplifier.

2.8.3 Linearity

This section discusses the common linearity measurements that limit amplifier performance. It includes one-dB compression point (P_{1dB}), third-Order intercept point and Spurious Free Dynamic Range (SFDR). In general, a Taylor series is used to model the output of a nonlinear network so that the output voltage [33]

$$v_o = c_0 + c_1 v_i + c_2 v_i^2 + c_3 v_i^3 \tag{2.78}$$

where v_i is the input voltage and c_0,c_1 ... c_n coefficients of the Taylor series.

2.8.3.1 One-dB Compression Point

One-dB compression point measures the linearity of the fundamental harmonic. When a single tone is applied at the input and the power of this signal is gradually increased the output power of the amplifier increases linearly as a function of input power. When a certain output power is reached, the network loses this linear relationship (Eg. Amplifier limited by rail voltages). The point where the output power is one dB below the theoretical output power if no compression occurred is defined as the one-dB compression point. This is shown in Figure 2.21a.

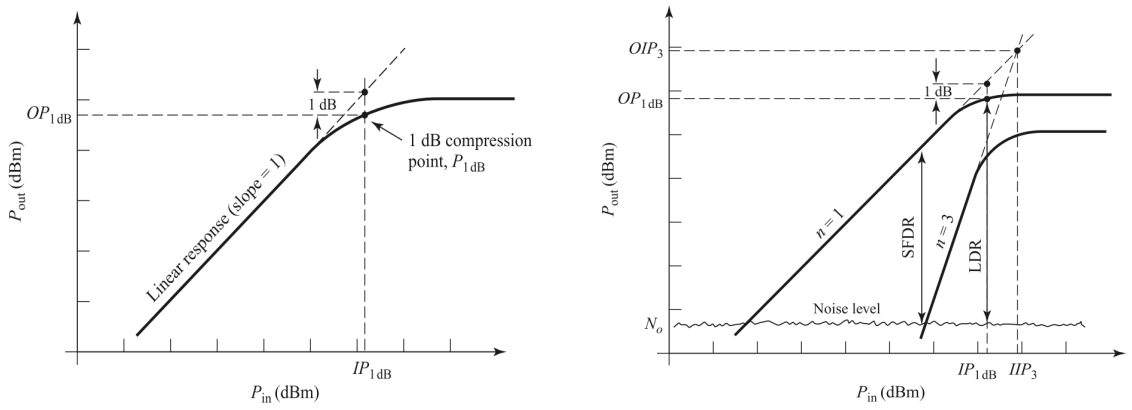


Figure 2.21: Nonlinear amplifier characteristics. (a) 1dB Compression point [28]. (b) Third order intercept point [28].

2.8.3.2 Third-Order Intercept Point

When two tones, ω_1 and ω_2 close in frequency are applied at the input of the nonlinear network so that

$$v_i = V_0(cos(\omega_1 t) + cos(\omega_2 t)) \tag{2.79}$$

substituting v_i into Equation 2.78 results in an output voltage [33]

$$\begin{aligned} v_0 = c_0 &+ c_1 V_0(cos(\omega_1 t) + cos(\omega_2 t)) \\ &+ c_2 V_0^2(cos(\omega_1 t) + cos(\omega_2 t))^2 \\ &+ c_3 V_0^3(cos(\omega_1 t) + cos(\omega_2 t))^3 + ... \end{aligned} \tag{2.80}$$

With some mathematical manipulation Equation 2.80 can be written as [33]

$$\begin{aligned} v_0 = c_0 &+ c_1 V_0 cos(\omega_1 t) + c_1 V_0 cos(\omega_2 t) + \frac{1}{2} c_2 V_0^2(1 + cos(2\omega_1 t)) + + \frac{1}{2} c_2 V_0^2(1 + cos(2\omega_2 t)) + \\ &+ c_2 V_0^2 cos(\omega_1 - \omega_2)t + c_2 V_0^2 cos(\omega_1 + \omega_2)t \\ &+ c_3 V_0^3 \left(\frac{3}{4} cos(\omega_1 t) + \frac{1}{4} cos(3\omega_1 t) \right) + c_3 V_0^3 \left(\frac{3}{4} cos(\omega_2 t) + \frac{1}{4} cos(3\omega_2 t) \right) \\ &+ c_3 V_0^3 \left(\frac{3}{2} cos(\omega_2 t) + \frac{3}{4} cos(2\omega_1 - \omega_2)t + \frac{3}{4} cos(2\omega_1 + \omega_2)t \right) \\ &+ c_3 V_0^3 \left(\frac{3}{2} cos(\omega_1 t) + \frac{3}{4} cos(2\omega_2 - \omega_1)t + \frac{3}{4} cos(2\omega_2 + \omega_1)t \right) + ... \end{aligned} \tag{2.81}$$

Figure 2.22 shows a visual representation of the frequencies present in output voltage from Equation 2.81

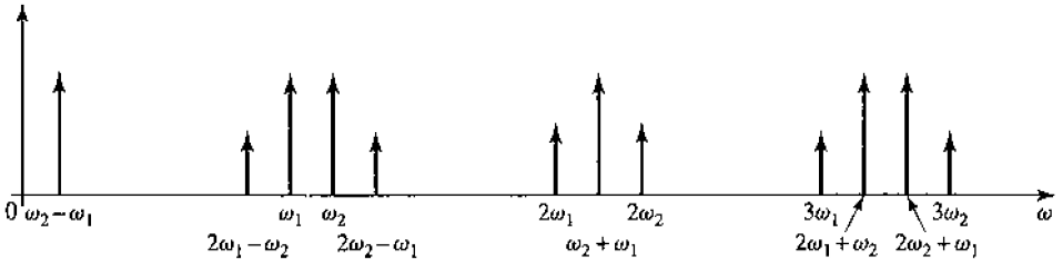


Figure 2.22: Frequencies present in the output voltage represented in the frequency domain [28].

Except for the input frequencies ω_1 and ω_2, most of the frequencies are far outside the frequency band of interest and are normally filtered by a bandpass filter. There are however two frequencies of concern. Consider the frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$. This resulting frequencies are again in the band of interest but an undesired outcome of the nonlinear distortion. Figure 2.21b shows the output power for a given input power. The slope of the first order is 1 and the third order 3. The third order intercept point are defined as the output power where the first order and 3rd order slopes intersect.

2.8.3.3 Spurious Free Dynamic Range

SFDR is an indication of the range of input powers that can be applied without introducing nonlinear effects on the output. The SFDR is indicated in Figure 2.21b. The noise floor is caused by external noise as well as internal noise in the amplifier. When the input power is increased the linear part of the output first increase above the noise floor. As the input power increase the output power stays linear. As the input power increase the third order signal power increases as well. When the power is enough to lift the third order signal above the noise floor the undesired signal shows in the spectrum which make it no longer spurious free. Figure 2.21b shows the SFDR characteristic of a nonlinear amplifier.

2.8.4 Biasing

The optimal design of biasing networks for low noise amplifiers are important to ensure the transistor operates at the desired Q-point without degrading RF performance in the frequency band of interest. This includes setting the correct V_{CE} and I_C for the correct RF performance of the transistor. Therefore it is important to design the bias circuit so that V_{CE} and I_C which set the RF performance of the transistor does not change with variation of the transistor parameters such as β in Bipolar Junction transistors.

2.8.4.1 Passive Bipolar junction transistor biasing circuits

Figure 2.23 shows a number of transistor biasing circuits. Each of the circuits differ in DC stability with changes in β and temperature. This section is based on the work of Agilent technologies [34] where they analysed DC stability of biasing circuits using the HBFP-0405 transistor against changes in H_{fe} and temperature.

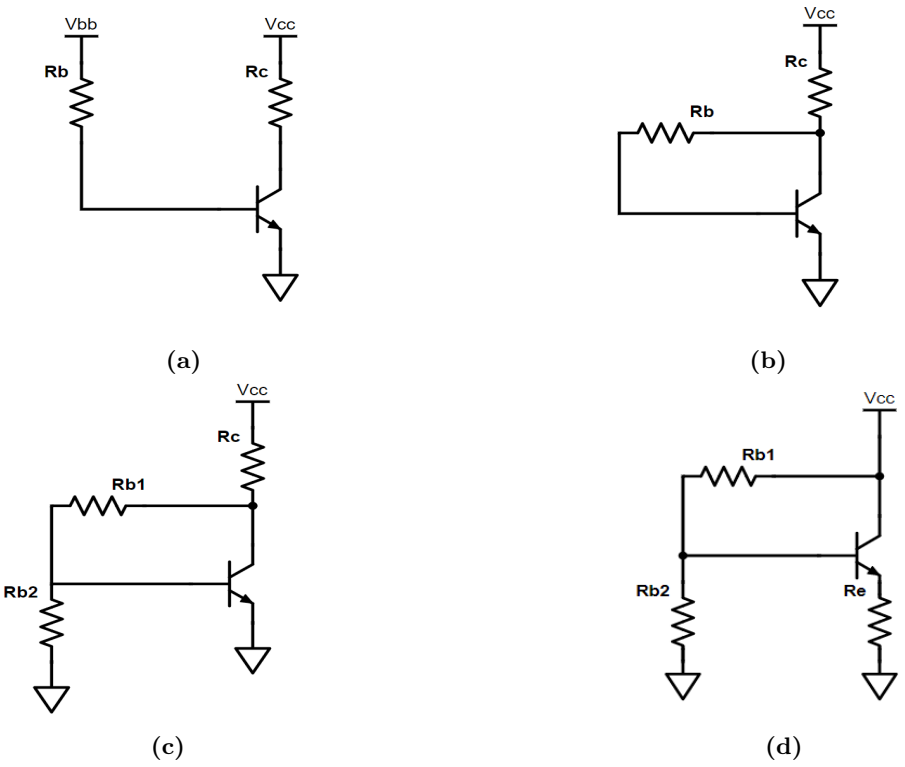


Figure 2.23: Different passive biasing circuits for Bipolar Junction Transistors. [34] (a) Non-Stabilised. (b) Voltage Feedback. (c) Voltage Feedback - Voltage Source. (d) Emitter Feedback.

Figure 2.23a shows the simplest biasing circuit for a BJT. The resistor R_b control the base current while R_C set the voltage V_{CE}. This circuit is not stable against variations in H_{fe} [34]. Bias circuit 2 in Figure 2.23b employ a feedback resistor between the collector and base of the BJT. This simple form of feedback aims to stabilize DC for variations in H_{fe} [34]. The resistor R_B can become rather large if the base current is low. Bias Circuit 3 in Figure 2.23c bias the base of the transistor using a voltage divider circuit which reduces the values of the resistors significantly. Bias circuit 4 in Figure 2.23d provides

high stability for variations in device parameters and temperature [34]. The quiscent collector current is given by

$$I_C = \frac{\beta\left(\frac{V_{CC}R1}{R1+R2} - V_{BE}\right)}{\frac{R2R1}{R1+R2} + R_E(1+\beta)}. \tag{2.82}$$

Given that

$$\frac{R2R1}{R1+R2} << R_E(1+\beta) \tag{2.83}$$

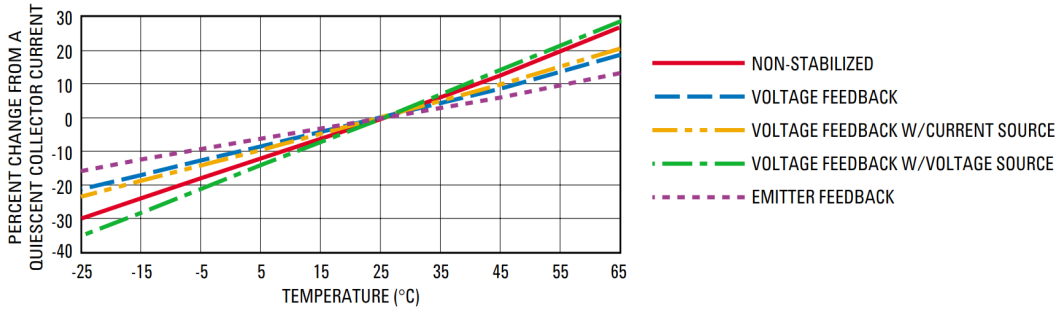
then

$$I_C \approx \frac{\beta\left(\frac{V_{CC}R1}{R1+R2} - V_{BE}\right)}{R_E(1+\beta)} \tag{2.84}$$

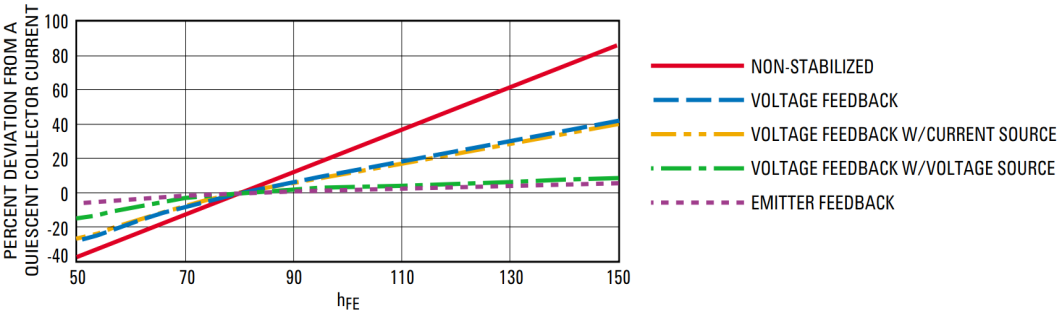
And with β usually much larger than unity the the I_C reduces to

$$I_C \approx \frac{\left(\frac{V_{CC}R1}{R1+R2} - V_{BE}\right)}{R_E} \tag{2.85}$$

making it independent of variation in β. Theoretically the bias circuit in Figure 2.23d is very attractive especially at lower frequencies. To provide a RF ground for the amplifier the resistor is bypassed with a capacitor. With component parasitics at high frequencies it may become difficult to implement this circuit. Figure 2.24 shows comparisons between these circuit analysed by Agilent technologies [34].



(a)



(b)

Figure 2.24: Changes in collector current I_C as a function (a) temperature [34] and (b) H_{fe} [34].

The Voltage Feedback with a current source is the same as the voltage feedback circuit in Figure 2.23c except for an added resistor between the voltage divider circuit and the base of the transistor.

2.8.4.2 Passive Field-effect transistor biasing circuits

Field effect transistors either operate as enhancement mode (positive V_{GS}), or depletion mode (negative V_{GS}) devices. This section discusses biasing circuits for the more complicated depletion mode FET that needs a negative gate-source voltage. Figure 2.24 shows two biasing circuits for depletion mode FET's. Note that resistors can be used to set the correct voltages, the aim of this section is to show the basic principles of the biasing circuit.

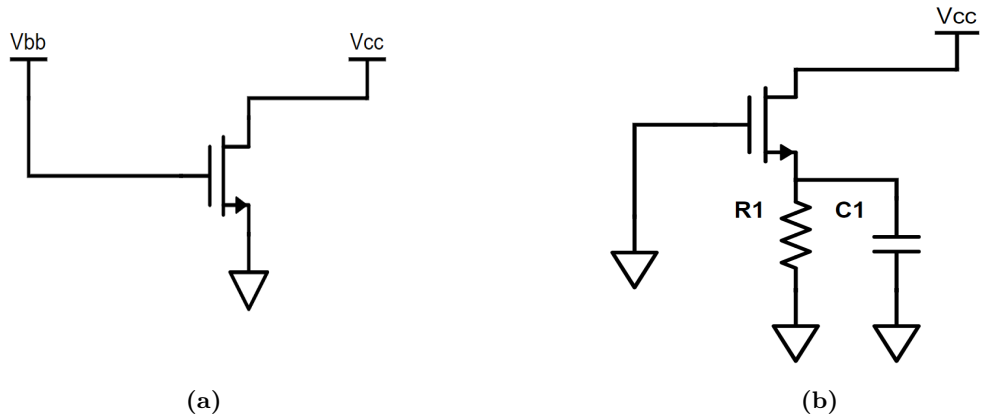


Figure 2.25: Depletion mode FET passive bias circuits. (a) Dual source topology. (b) Single source topology.

In Figure 2.25a V_{bb} is negative and V_{cc} positive so that the gate source voltage is negative and turn the FET on. The disadvantage of this topology is that two sources are needed that increase complexity of the design. The FET in Figure 2.25b only need a single source by taking advantage of the resistor $R1$ connected between the source of the FET and ground. The purpose of the resistor is to increase the source voltage of the FET when there is current flow through the resistor while the gate is grounded. Interestingly, this results in a negative V_{GS} that turn on the depletion mode FET.

2.8.4.3 RF Choke

RF power loss through the biasing network can be avoided by applying the base/gate and source/emitter voltage through RF chokes. The purpose of the RF choke is two act as a short circuit for DC and open circuit at RF. RF chokes are implemented with inductors or transmission line by means of an open-circuited radial stub

Transmission line

A transmission line RF choke is implemented using a quarter-wave radial stub to transform the impedance from an open to short circuit. Another quarter wave transmission line is added to transform the impedance from the radial stub from short to open circuit at the RF path. This circuit is shown in Figure 2.26. DC is connected at the RF short formed by the radial stub which means it does not affect the RF circuit at that frequency. At the RF path this biasing circuit present an open circuit at the specific frequency and prevent power flow into the biasing circuit. It is important to note that this biasing circuit is inherently narrow-band as the sections are only a quarter-wavelength for a single frequency.

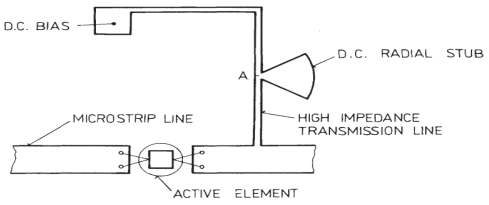
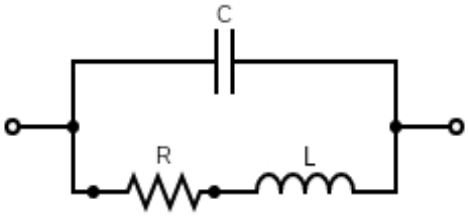


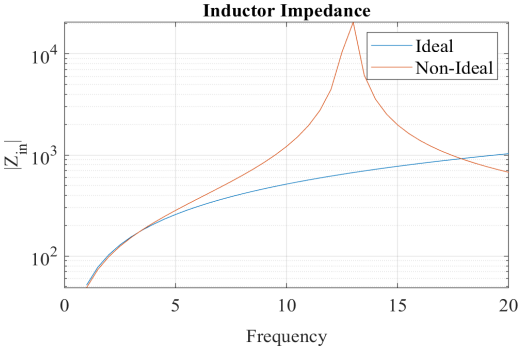
Figure 2.26: Microstrip radial stub implemented as RF choke [35].

Inductors as RF chokes

Inductors do precisely what is required from an RF choke. Ideal inductors are reactive components of which the impedance increases linearly with frequency. In practice, inductors are not ideal and have losses as well as capacitance between wires for example. Figure 2.27a shows the basic circuit model for non-ideal inductors.



(a)



(b)

Figure 2.27: (a) Equivalent circuit model for non-ideal inductor. (b) Impedance of a non-ideal inductor compared to an ideal inductor.

When choosing an inductor as RF choke, it needs to have an impedance high enough in the frequency band to isolate the bias network sufficiently. When the inductor is used as an RF choke the designer can employ the non-ideal effects of the inductor. At resonance where the inductor response changes from dominantly inductive to capacitive, the inductor has a high impedance depending on the Q of the inductor. When the resonant point is chosen in the middle of the frequency band, the inductor act as an excellent open circuit for RF signals.

2.8.5 Lossless two port network theory

This section discusses the theory behind a lossless two port network. This theory is practically implemented in Section 5.2 as a way to calculate the noise contribution of the low noise amplifier (LNA) when terminated with the antenna impedance at the input. In Lossless networks no real power is delivered to the network, which means power into the network is equal to the power out of the network. Equation 2.86 describe the average power delivered to the lossless network [28].

$$\begin{aligned} P_{avg} &= \frac{1}{2}Re\{[V]^t[I]^*\} = \frac{1}{2}Re\{([V^+]^t + [V^-]^t)([V^+]^* - [V^-]^*)\} \\ &= \frac{1}{2}[V^+]^t[V^+]^* - [V^-]^t[V^-]^* = 0 \end{aligned} \tag{2.86}$$

The last terms of Equation 2.86 represents the incident and reflected power respectively. For a two-port lossless network

$$[V^+]^t[V^+]^* = [V^-]^t[V^-]. \tag{2.87}$$

Using the definition of S-parameters Equation 2.87 can be written as

$$[V^+]^t[V^+]^* = [V^+]^t[S]^t[S]^*[V^+]^*. \tag{2.88}$$

For incident voltages $[V^+] \neq 0$

$$[S]^t[S]^* = [S]^\dagger[S] = [U]. \tag{2.89}$$

Equation 2.89 can be expressed in summation form as [28]

$$\sum_{k=1}^{N} S_{ki}S_{ki}^* = 1, \text{for } i = j \tag{2.90}$$

and

$$\sum_{k=1}^{N} S_{ki}S_{ki}^* = 0, \text{for } i \neq j. \tag{2.91}$$

From the conditions in Equation 2.90 and Equation 2.91 derive

$$|S_{11}|^2 + |S_{21}|^2 = 1 \tag{2.92}$$

$$|S_{22}|^2 + |S_{12}|^2 = 1 \tag{2.93}$$

$$S_{12}S_{11}^* + S_{22}S_{21}^* = 0 \tag{2.94}$$

From Equations 2.92-2.94 it can be shown that the following conditions apply to lossless two-port networks

$$|S_{11}| = |S_{22}| \tag{2.95}$$

$$|S_{21}| = |S_{12}| \tag{2.96}$$

$$\angle S_{12} - \angle S_{11} = \angle S_{22} - \angle S_{21} + \pi. \tag{2.97}$$

2.9 Active Receiving antennas

This section discusses noise in active receiving antennas and antenna arrays. The section begins by reviewing noise and power in single active antennas. Section 2.9.2 discusses noise in active antenna arrays as well as new figures of merit developed for these active arrays. Section 2.9.1 and 2.9.2 follow the work of Warnick et al [36] and will therefore use the same defined symbols as in the literature.

2.9.1 Single active antenna

2.9.1.1 Received power from incident plane wave

When characterizing receiving antennas the received power at the antenna terminals from an incident wave is important. Equation 2.98 describes the power flux density of a plane wave $\bar{E}^{inc}$.

$$S_{sig} = \frac{\left|\bar{E}^{inc}\right|^2}{2\eta} \qquad (W/m^2) \tag{2.98}$$

where η is the intrinsic impedance of space. The relation between the available power at the antenna terminals P_o and power flux density of the incident wave S_{sig} is defined as effective area of the antenna [36] and is shown in Equation 2.99, assuming the polarization of the incoming wave is matched to the antenna.

$$P_o = A_e S_{sig} \qquad (W) \tag{2.99}$$

This is illustrated in Figure 7.4h. Equation 2.102 gives the output power when an LNA is connected to the output of the antenna

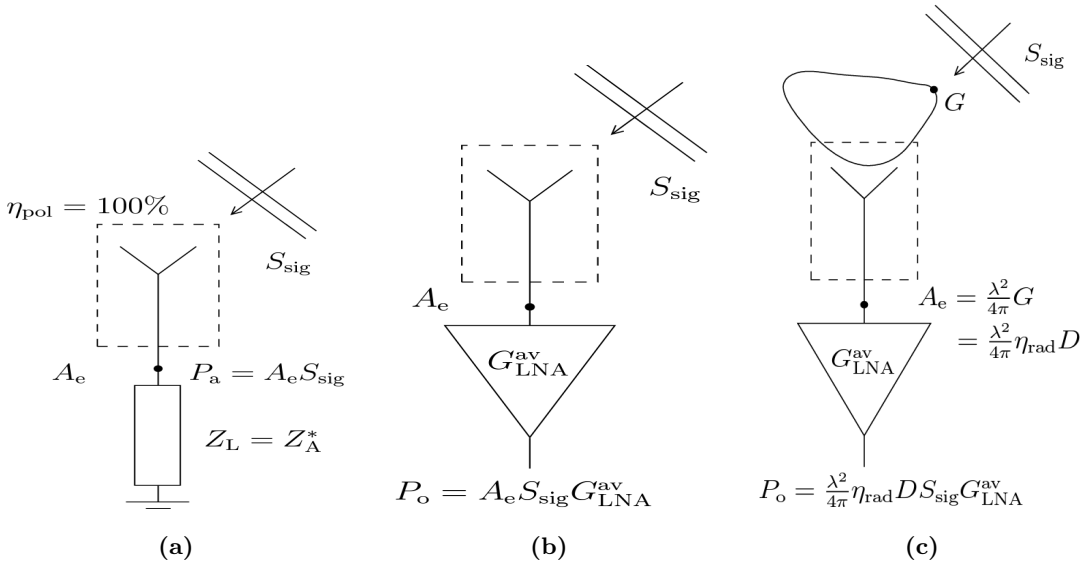


Figure 2.28: (a) Passive antenna terminated in matched load [36]. (b) LNA connected to output of passive antenna [36]. (c) Illustration of output power in terms of passive antenna gain and LNA gain [36].

$$P_a = A_e G_{LNA}^{AV} S_{sig} \qquad (W) \tag{2.100}$$

where G_{LNA}^{AV} is the available gain of the LNA. For reciprocal antennas Equation 2.101 relates the gain to effective area

$$A_e = \frac{\lambda^2}{4\pi} G \tag{2.101}$$

substitute Equation 2.101 into 2.102

$$P_o = \frac{\lambda^2}{4\pi} \eta_{rad} D S_{sig} G_{LNA}^{AV} \qquad (W) \tag{2.102}$$

here D is directivity in certain direction and η_{rad} the radiation efficiency.

2.9.1.2 Noise in active receiving antenna

The main noise contributions in active antenna systems are[36]

- **External** - Noise received by the antenna from the environment it is located. The brightness temperature $T(\Omega)$ varies with angle.
- **Antenna losses** - Ohmic and dielectric losses in the antenna that contributes noise due to the physical temperature T_{ph} of the antenna
- **Receiver Noise** - Noise contributed by the receiver chain. These include noise sources as discussed in Section 2.7.2.

Equation 2.103 gives the effective brightness temperature [36]

$$T_{ext} = \frac{\eta_{rad}}{4\pi} \int D(\Omega) T_{sky}(\Omega) d\Omega \tag{2.103}$$

where $D(\Omega)$ is the directivity at angle Ω and T_{sky} the angle dependent brightness temperature. Secondly the Equivalent temperature T_{Loss} contributed by losses in the antenna[36]

$$T_{loss} = \frac{(L-1)T_{ph}}{L} = (1 - \eta_{rad}) T_{ph} \tag{2.104}$$

where L is the loss factor and T_{ph} the physical temperature of the antenna. The total antenna noise temperature is found by adding the Loss noise and external noise so that [36]

$$T_A' = (1 - \eta_{rad}) T_{ph} + \frac{\eta_{rad}}{4\pi} \int D(\Omega) T_{sky}(\Omega) d\Omega \tag{2.105}$$

From Equation 2.30 and 2.101 the SNR can be related to sensitivity [36]

$$SNR = \frac{\lambda^2 S^{inc} G}{4\pi k_B B T_{sys}} \tag{2.106}$$

The sensitivity figure of merit G/T [36]

$$\frac{G}{T_{sys}} = \frac{4\pi k_B B}{\lambda^2 S^{inc}} SNR \tag{2.107}$$

The sensitivity figure of merit Ae/T_{sys} [36]

$$\frac{A}{T_{sys}} = \frac{k_B B}{S^{inc}} SNR \tag{2.108}$$

Finally Ae/T_{sys} can be written as [36]

$$\frac{A}{T_{sys}} = \frac{\lambda^2 \eta_{rad} D}{4\pi(\eta_{rad} T_{ext} + (1 - \eta_{rad}) T_{ph} + T_{rec})}. \tag{2.109}$$

2.9.2 Active receiving antenna arrays

Section 2.9.1 reviewed power and noise in single active antenna receivers. In an array environment, mutual coupling between antennas needs to be included in the design to improve system performance. Warnick et al. [37] proposed new figures of merit from previous work that include mutual coupling between antennas as well as receiver noise. As of 2013 the following IEEE antenna terms [38] were added or updated to include active antenna arrays :

- Isotropic noise response.
- Active antenna available gain
- Active antenna available power
- Receiving efficiency.
- Effective area for active arrays.
- Noise matching efficiency.
- Noise temperature for active arrays

These antenna terms are thoroughly discussed in [36], [37] and will not be repeated here with exception to the isotropic noise response.

The isotropic noise response of the antenna array is used in the definitions of a number of active antenna array terms [36], [37] and will therefore be discussed here. The standard definition reads [38]:

> *"For a receiving active-array antenna, the noise power at the output of a formed beam with a noiseless receiver when in an environment with a brightness temperature distribution that is independent of direction and in thermal equilibrium with the antenna"*

Consider the simplified block diagram of an antenna array connected to a receiver and beamforming network in Figure 2.29.

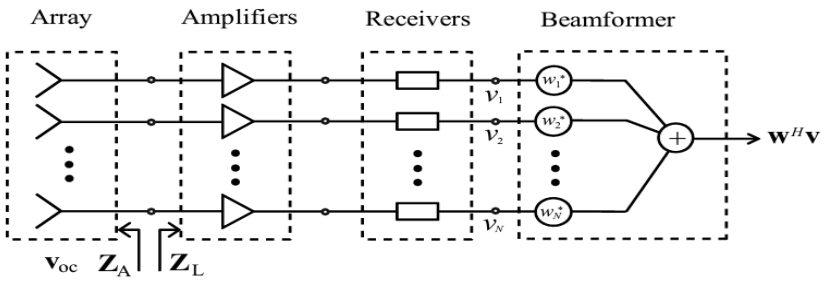


Figure 2.29: Simplified block diagram of an active antenna array [36].

The output voltage at each channel are the combined voltage contributions according to

$$\mathbf{v} = \mathbf{v_{sig}} + \mathbf{v_{ext}} + \mathbf{v_{loss}} + \mathbf{v_{rec}} \tag{2.110}$$

Assuming the voltages are uncorrelated so that $E[\mathbf{v_{sig}}\mathbf{v_n^H}] = E[\mathbf{v_{sig}}\mathbf{v_{int}^H}] = E[\mathbf{v_{int}}\mathbf{v_n^H}] = 0$ the correlation matrix of the array is [36]

$$\mathbf{R_v} = \mathbf{R_{sig}} + \mathbf{R_{ext}} + \mathbf{R_{loss}} + \mathbf{R_{rec}} \tag{2.111}$$

An estimate of the correlation matrix can be determined from a number of samples [36]

$$\hat{\mathbf{R}}_\mathbf{v} = \frac{1}{N}\sum_{n=1}^{N}\mathbf{v}[n]\mathbf{v}[n]^H \tag{2.112}$$

In the special case where the antenna is located in an environment where the brightness temperature is constant with direction $T(\Omega) = T_{iso}$ and correlation matrix for external noise is labeled as $\mathbf{R_{ext}}$ [36]. The isotropic noise response is defined for a lossless receiver so that $\mathbf{R_{rec}} = 0$.

The correlation matrix of the array under these can be written as [36]

$$\mathbf{R_{t,iso}} = \mathbf{R_{ext,iso}} + \mathbf{R_{loss}}. \tag{2.113}$$

Mathematically the isotropic noise response can then be written for a given formed beam as [36]

$$P_{t,iso} = \mathbf{w}^H\mathbf{R_{t,iso}}\mathbf{w} \tag{2.114}$$

The Y-factor hot-cold load measurement technique can be used as a practical method to determine the array correlation matrix. When used with antenna arrays, the array is placed in an environment with a high brightness temperature, T_{hot}, and low brightness temperature T_{cold}.

With each brightness, the outputs are correlated, and the correlation matrix is calculated according to

$$\mathbf{R_{ext,iso}} = \frac{T_{iso}}{T_{hot} - T_{cold}}(\mathbf{R_{hot}} - \mathbf{R_{cold}}) \tag{2.115}$$

$$\mathbf{R_{loss}} + \mathbf{R_{rec}} = \frac{1}{T_{hot} - T_{cold}}(T_{hot}\mathbf{R_{cold}} - T_{cold}\mathbf{R_{hot}}) \tag{2.116}$$

The hot and cold sources must cover enough of the field of view of the antenna so that it approximates an isotropic brightness temperature. A typical hot source is a microwave absorber that covers the antenna, and the sky is used as a cold source. This section briefly introduced the new figures of merit for active antenna arrays. A more in-depth discussion followed for the isotropic noise response and how to practically determine it as it forms the basis of a number of the new figures of merit. The next section describes the three antenna method for measuring the absolute gain of an antenna.

2.10 Gain measurement using the three-antenna method

This section introduces the measurement of antenna gain by using three antennas. This is a useful technique when the antennas under test are not identical [39]. When introducing a third antenna to the measurement, it is possible to get the gain of all three antennas. Three combinations of antennas are measured and from the three measurements Equations 2.117 to 2.119 are used to determine the gain of each antenna [39].

$$G_a + G_b = 20log_{10}\left(\frac{4\pi R_{ab}}{\lambda}\right) + 10log_{10}\left(\frac{P_{rb}}{P_{ta}}\right) \tag{2.117}$$

$$G_a + G_c = 20log_{10}\left(\frac{4\pi R_{ac}}{\lambda}\right) + 10log_{10}\left(\frac{P_{rc}}{P_{ta}}\right) \tag{2.118}$$

$$G_b + G_c = 20log_{10}\left(\frac{4\pi R_{bc}}{\lambda}\right) + 10log_{10}\left(\frac{P_{rc}}{P_{tb}}\right) \tag{2.119}$$

In each of the equations, the first term on the right of the equation account for free space losses while the second term is the ratios between input and output power at the terminals of the transmit and receive antenna, respectively. Using Equations 2.117 to 2.119 the individual antenna gains are calculated as

$$G_a = ((G_a + G_b) - (G_b + G_c) + (G_a + G_c))/2 \tag{2.120}$$

$$G_b = ((G_b + G_c) - (G_a + G_c) + (G_a + G_b))/2 \tag{2.121}$$

$$G_c = ((G_a + G_c) - (G_a + G_b) + (G_b + G_c))/2. \tag{2.122}$$

Chapter 3

Antenna Design

Chapter 4 discusses the design of the LNA to be integrated at the feed of the antenna. In this section, knowledge gathered from Chapter 4 is used to design the antenna for the active antenna array system.

3.1 Integration between Antenna and LNA

There are multiple ways to integrate the LNA and the antenna. Conventionally it is common to design the antenna and match it to 50Ω and design a separate LNA and match it to 50Ω. Depending on the antenna impedance and bandwidth, this matching can become complicated and require a large area to implement it. Another approach of integrating the antenna and LNA is to design the antenna for a non 50Ω reference impedance. A custom LNA is then matched to the reference impedance of the antenna such as implemented by Garcia-Perez et al. [40] for a differential Vivaldi array. The approach followed in this project closely resembles the work by Kruger et al. [41]. With this approach, no matching circuit is added between the antenna and LNA. Therefore, the antenna is designed so that the antenna impedance provides a good match to the optimum noise impedance of the LNA. This approach removes losses from a complex matching circuit and adds the LNA directly at the feed of the antenna. In other words, even if the antenna does not provide a perfect match to the optimum noise impedance, it may still be sufficient due to the reduction of overall minimum noise figure. A disadvantage, however already noticeable from this approach is that the antenna is predominantly designed based on impedance and not its radiation characteristics.

3.2 General Considerations

The initial antenna array prototype implements a single polarized design to keep the array as inexpensive as possible. Two grid layouts are investigated in Section 2.2. For simplicity, the common rectangular grid layout is used. Impedance anomalies discussed in Section 2.5.4 that occurs in single polarized Vivaldi arrays, and grating lobes should be considered in the design of the grid layout of the antenna array. An H-plane spacing of approximately a half-wavelength avoids these impedance anomalies. E-plane element spacing is designed to avoid grating lobes in the visible region of the antenna. Equations 2.13 and 2.14 provide the necessary condition to avoid grating lobes in the visible region. Approximately half-wavelength spacing is selected to avoid grating lobes for all scan angles.

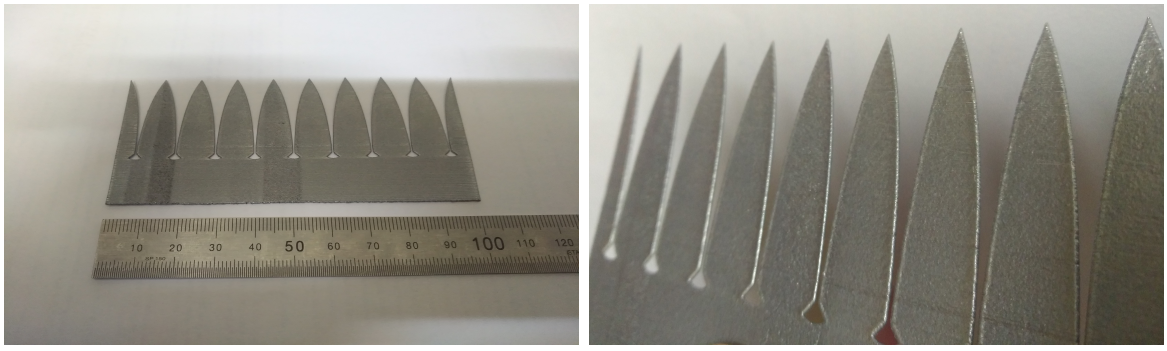
3.3 SLM 3D-printed linear Vivaldi array

This section aims to evaluate the capabilities of aluminium additive manufacturing at the dimensions associated with X-Band frequencies. This array was manufactured with SLM additive manufacturing discussed in Section 2.6 at the smallest anticipated dimensions for the slot width W_s and radial slot radius R_s. The width of this Vivaldi is set to slightly smaller than a half-wavelength at the highest frequency. The length of the Vivaldi is chosen to be longer than expected to evaluate the mechanical stability of the taper regions. Additive manufacturing printing is done with a layer thickness of $30\mu m$. The manufactured metal thickness is 0.5 mm.

Table 3.1: Design parameter values of the 9 Element Vivaldi Array

Parameter	Value (mm)
L_t	30
L_S	2.8
R_a	0.08
H_a	11
W_S	0.4
R_S	2.6

Figures 3.1a and 3.1b shows the printed antenna.



(a) **(b)**

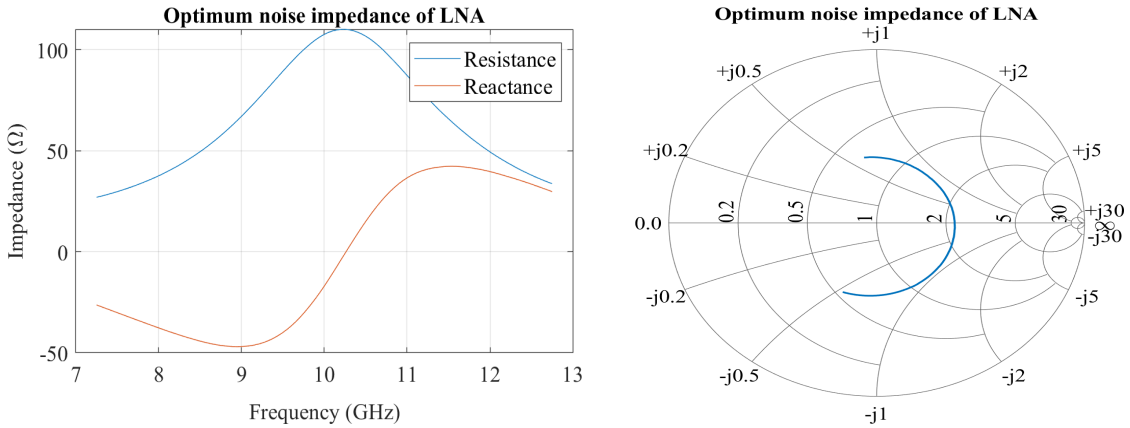
Figure 3.1: SLM 3D printed linear vivaldi array

Dimensionally the antenna was printed very well. One cause for concern, but not possible to predict the outcome before testing, is the surface roughness of the additive manufacturing. The printed model, however, provide the necessary confidence in the manufacturing capability of aluminium additive manufacturing.

3.4 Antenna Unit Cell design

This section discusses the design of the infinite Vivaldi array. A short piece of transmission line is added to the LNA designed in Chapter 4 to reduce the difference between the optimum impedance of the LNA and the higher input impedance of Vivaldi arrays. The

optimum noise impedance of the LNA with the additional transmission line at the source is shown in Figure 3.2.



(a) (b)

Figure 3.2: (a) Optimum noise impedance of the LNA. (b) Optimum noise impedance of the LNA represented on the Smith Chart.

The optimum noise impedance 'moves' counter-clockwise around the smith chart while the passive antenna rotates clockwise which means that perfect noise matching is not possible over the entire frequency band and the noise will be minimum at certain impedance values in the operating bandwidth. Antenna array design is started with an infinite array simulation in FEKO. For convenience Figure 3.3b repeats the antenna dimensions as defined in Section 2.5.1.

(a) (b)

Figure 3.3: (a) Vivaldi taper in infinite array setup. (b) Vivaldi Unit Cell design parameters.

At first, only the taper region antenna is considered. The element spacing of the array was established in the previous section. With the upper-frequency limit set to 12.75 GHz the element width is approximately 12 mm and is used as a starting point in the design. The length of the element set the lower frequency cutoff of the antenna where the structure approaches open circuit. Figure 3.3a shows the infinite array simulation setup of the antenna taper region.

Analysing the impedance of the antenna taper only the impedance between 3 GHz and 8 GHz follows the same pattern as the optimum noise impedance of the LNA, especially the resistance. Resistance was favoured in the design of the initial taper dimensions as the

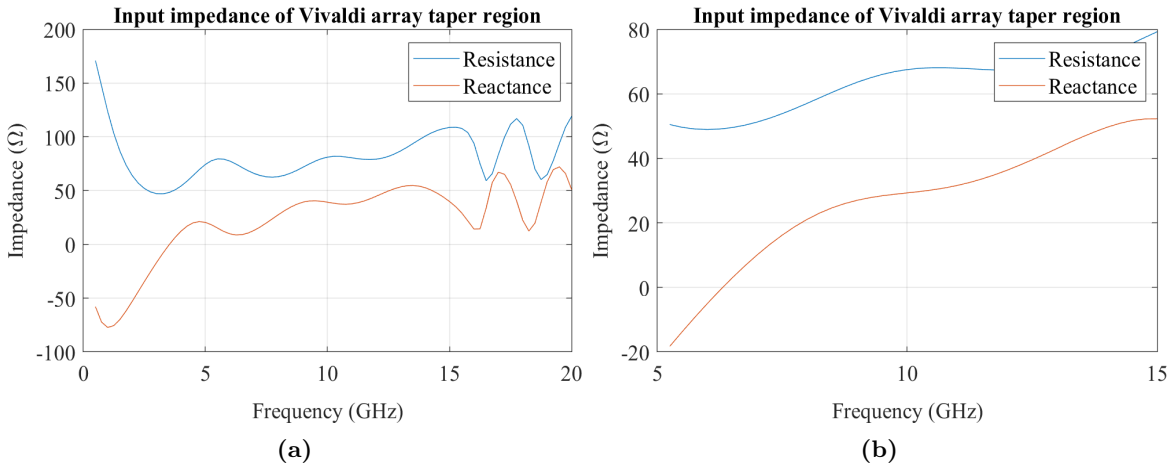


Figure 3.4: (a) Input impedance of the Vivaldi taper region with length $L_t = 30mm$. (b) Input impedance of the Vivaldi taper region with length $L_t = 15mm$.

reactive parts in the microstrip to slot transition can still aid in adjusting the reactance. The antenna length is halved to $L_t = 15mm$ in an attempt to move this impedance characteristics into the operating bandwidth. The new input impedance of the antenna is shown in Figure 3.4b.

The next part of the antenna design is the integrated microstrip to slot transition, as discussed in Section 2.5.2. The microstrip to slot transition used in this project is indicated in Figure 3.3b. A constraint of the aluminium 3D printing is that it allows a maximum unsupported overhang angle of 45°. Therefore the slot cavity, commonly implemented as a square or circular cavity, is implemented as a radial slot cavity to allow 3D printing of the antenna. On the top layer of the substrate, the microstrip that feeds the antenna is terminated in a microstrip radial stub. For the design of the transition, an analytical approach aided by the Smith chart is used. Figure 3.5a shows the impedance of the antenna taper on the smith chart.

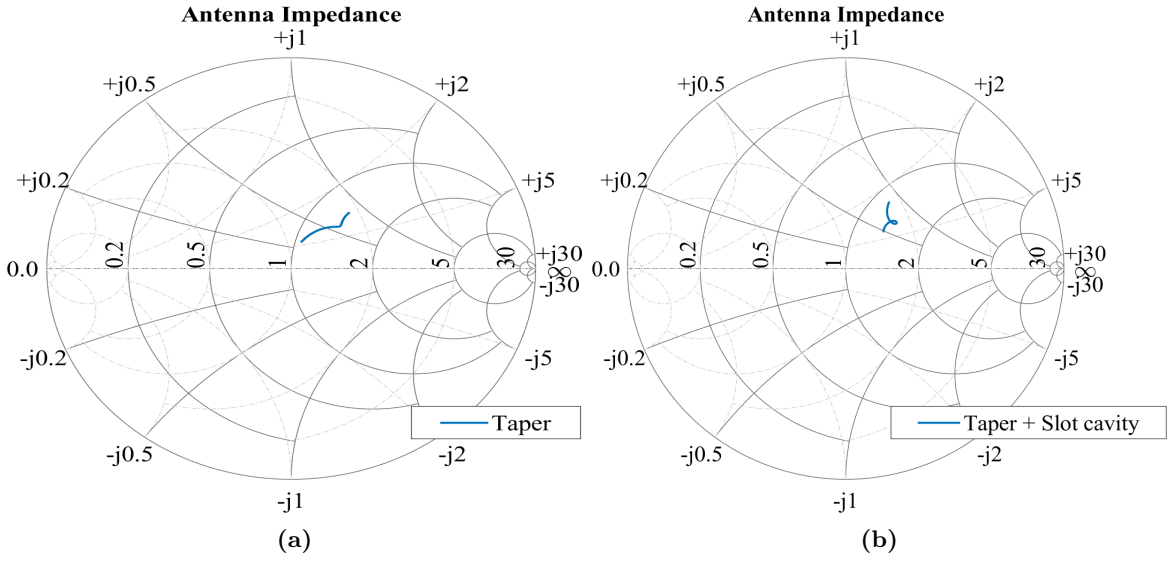


Figure 3.5: (a) Antenna impedance with only taper region. (b) Antenna impedance with taper region and slot cavity.

A slot cavity smaller than a quarter wavelength behaves inductively. Therefore if considered in parallel with the antenna, it is simpler to consider it as a negative susceptance

on the Smith chart. The resulting impedance is shown in Figure 3.5b.

The microstrip radial stub is added in series with the impedance in Figure 3.5b. Therefore it is preferable to examine the impedance Smith Chart. In Figure 3.5b it can be seen that in order to move the impedance of the antenna consisting only of the taper and slot towards the real axis of the Smith chart capacitance is needed. A microstrip radial stub shorter than a quarter wavelength behaves capacitively. The impedance of the radial stub is desirable as it has the potential to transform the impedance closer to the real axis of the Smith Chart. Figure 3.6a shows the impedance of the antenna after the addition of a microstrip radial stub with $R_m = 2mm$.

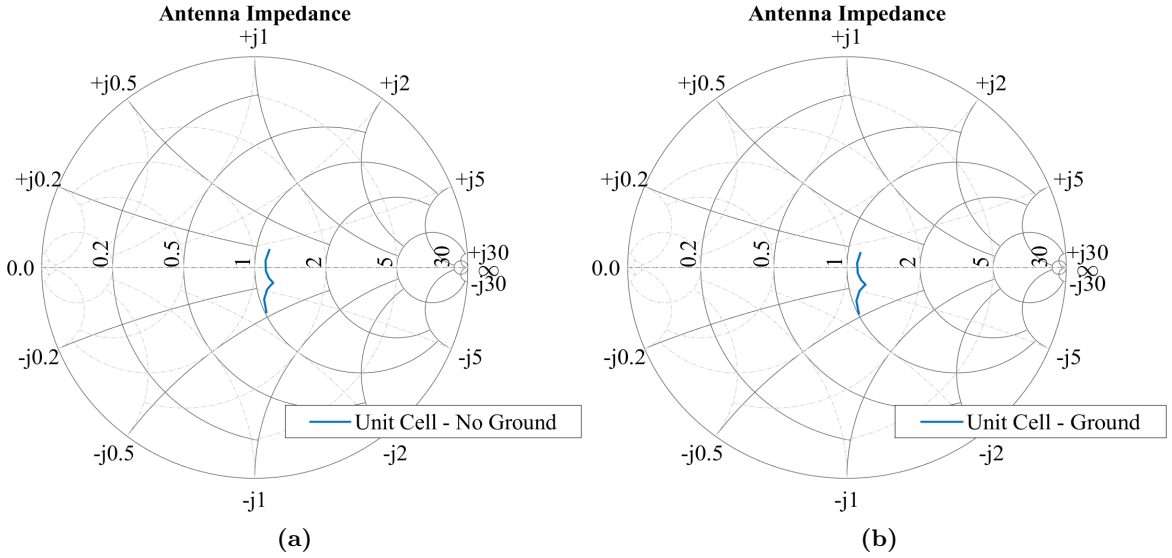


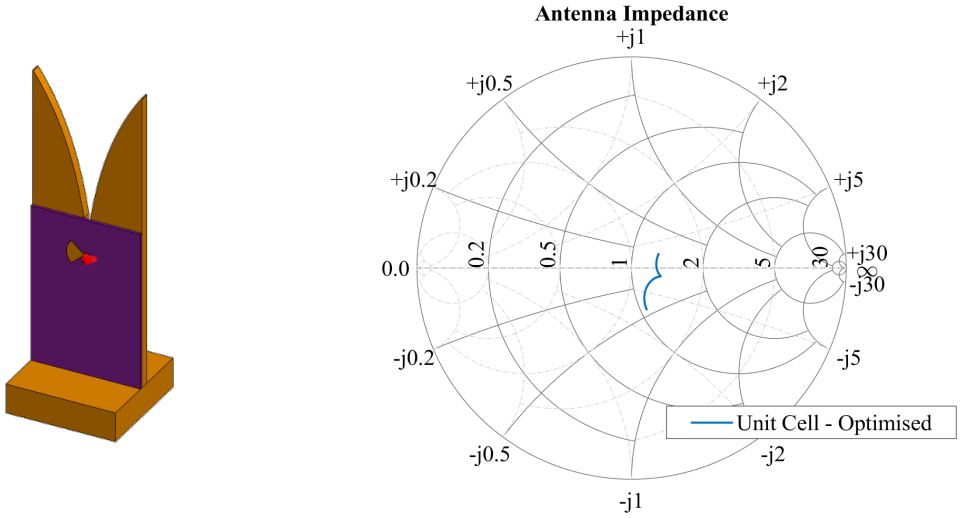
Figure 3.6: (a) Antenna impedance of the unit cell without a groundplane. (b) Impedance of the unit cell.

Finally, a ground plane is added to the antenna array to provide a base to fit each row of antennas and shield the array from ground noise. The ground plane has minimal effect on the antenna impedance. At this point in the design, it is possible to apply a few parameter sweeps around the current parameter values to determine the final impedance. The design parameter values as defined in Figure 3.3b for the designed infinite array is summarized in Table 3.2.

Table 3.2: Design parameter values of the optimised antenna array element.

Parameter	Value (mm)
L_t	14.8
L_S	4.1
R_a	0.1
H_a	11.8
W_S	0.7
R_S	3.2
W_a	12
R_m	1.75
W_m	0.4

Figures 3.7a and 3.7b shows the final unit cell and its associated input impedance at the feed of the antenna.



(a) **(b)**

Figure 3.7: (a) Simulation model of the antenna array element. (b) Antenna impedance of optimised Unit Cell.

This chapter discussed the design of the antenna array element in an infinite array setup. The design approach followed was to evaluate the impedance contribution of the individual components present in the Vivaldi antenna array element. The next chapter design the low noise amplifier to be integrated at the feed of the antenna designed in this chapter.

Chapter 4

LNA Design

This chapter discusses the design process followed in the design of the low noise amplifier to be integrated at the feed of the antenna. In Section 4.1 and 4.2 an appropriate transistor and substrate material are selected. Then a general stabilization circuit for the transistor is derived in Section 4.3. Based on the stability investigation, Section 4.4.2 identify possible circuit components that operate sufficiently in the frequency band. The last part of this chapter evaluates a prototype LNA and finally the LNA to be used in the active antenna array system.

4.1 Transistor Selection

In the sensitivity figures of merit in Equations 2.107 and 2.108 the noise contribution of the LNA is part of the receiver noise temperature T_{rec}. In cascaded systems, the first stage LNA after the antenna is the most significant contributor to the overall noise of the system and therefore requires a low noise figure. In modern times it is more common to see LNA's implemented as an MMIC and is indeed preferable where there are strict size requirements. It is however expensive and therefore the LNA in this proof of concept active antenna array is implemented using commercially available discrete transistors.

Three transistors are considered that met the frequency requirements with an attractive noise figure. The first two transistors are the CE3512K2 [42] and CE3514M4 [43] from California Eastern Laboratories (CEL) both pHemt technology. The third transistor is the BFU910 [44] a bipolar transistor from NXP. The selection of these transistors was mainly based on their noise figure specifications. Table 4.1 summarize key characteristics of these transistors.

Mfr.	Mfr. Part No.	NFmin	Associated gain (dB)	Vce (V)	Id (mA)	Frequency (GHz)
CEL	CE3512K2	0.3	13.7	2	10	12
CEL	CE3514M4	0.42	12.2	2	10	12
NXP	BFU910F	0.65	13	2	6	12

Table 4.1: Key characteristics of selected transistors.

Comparing the transistors, it is visible that the pHemt transistors are superior in terms of noise figure with the noise figure of the BFU910 still acceptable and well below the specification set out for this project. The associated gain of the BFU910 is second

to the CE3512K2 and the power consumption of the BFU910 the lowest. In this project, the BFU910 is selected as the transistor of choice due to the less complicated biasing circuit of bipolar transistors and is available at a significantly lower cost which can be significant in an array with a large number of antennas. The pHemt models both require a negative voltage at the gate which means that either a dual voltage supply is needed for the negative v_{gs} voltage or a resistor between the source and ground as described in Section 2.8.4.2 both not particularly attractive for this project.

4.2 Substrate Selection

Three substrates were considered in this project:

- Rogers RT Duroid 5880 [45]
- Arlon CLTE-AT [46]
- Rogers RO4003C [47]

The RT Duroid 5880 has the lowest loss but comes at a very high price point. The Arlon CLTE-AT is a good compromise between cost and losses and should be highly considered for future projects. As this project mainly acts as a proof of concept, the less expensive RO4003C is used. The thickness of the substrate greatly influences the RF circuit design. As the LNA will consist of transistor packages the microstrip widths should be comparable to the width of the package leads to allow for a good transition to the transistor package. A thinner substrate reduces the overall footprint of the LNA as a consequence of the smaller RF circuits. The microstrip width for a 50 Ω line on 8 mil thickness is 0.422mm, 0.65mm on 12mil thickness and 1.1 mm on a 20mil substrate. Although the 8mil Rogers has a small desired difference in width to the package leads it was decided to use the 12 mil thickness to ease in-house manufacturing of prototype circuits. The 12 mil substrate also provides better stability during testing of the prototype LNAs.

4.3 Stability and Biasing Conditions

According to the datasheet [44] of the BFU910 transistor the DC Quiscent point for optimum noise figure is at $V_{ce} = 2V$ and $I_c = 6mA$. The stability analysis that follows uses the S-parameters supplied by NXP. At high frequencies, the impedance of the vias grounding the transistor can have a significant influence depending on the thickness of the substrate used. Therefore the first step was grounding the transistor with ground vias. The new set of S-Parameters is used for stability analysis. Figure 4.1 shows the Stability factor of the grounded transistor.

Figure 4.1 shows that the device close to stable over the entire operating frequency band. This, however, is not sufficient as the device can still be unstable out of the operating frequency band. Conventional stabilisation methods include the addition of a shunt or series resistor at the source or load terminals of the device. Evaluation of the source and load stability circles in Figure 4.2a and Figure 4.2b shows that it is challenging to select a resistor that will provide the necessary stability given that the potentially stable regions almost cover the entire Smith Chart.

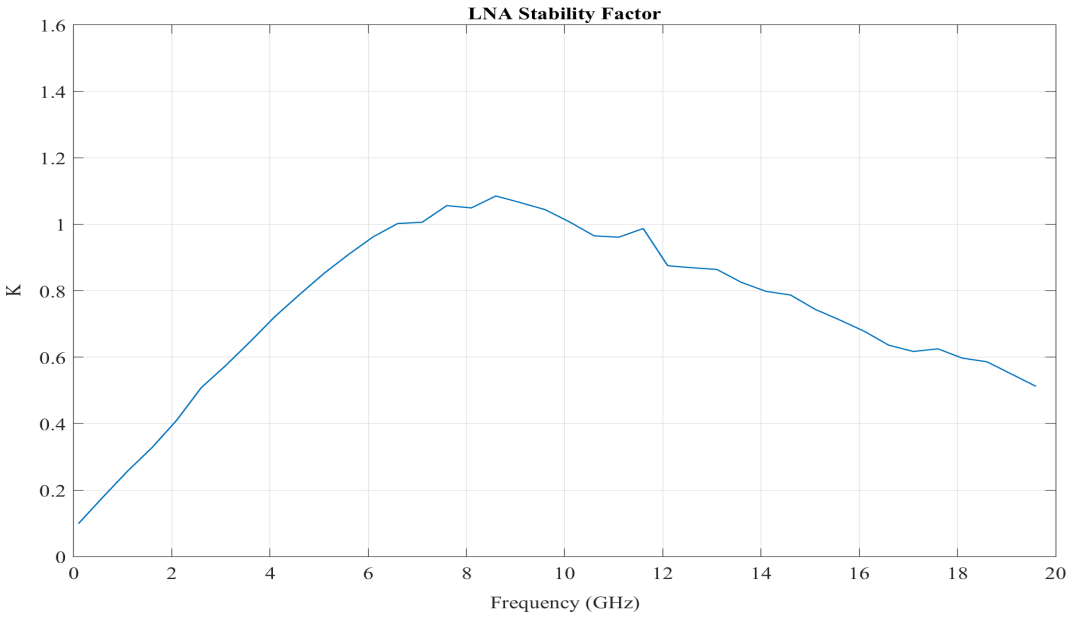
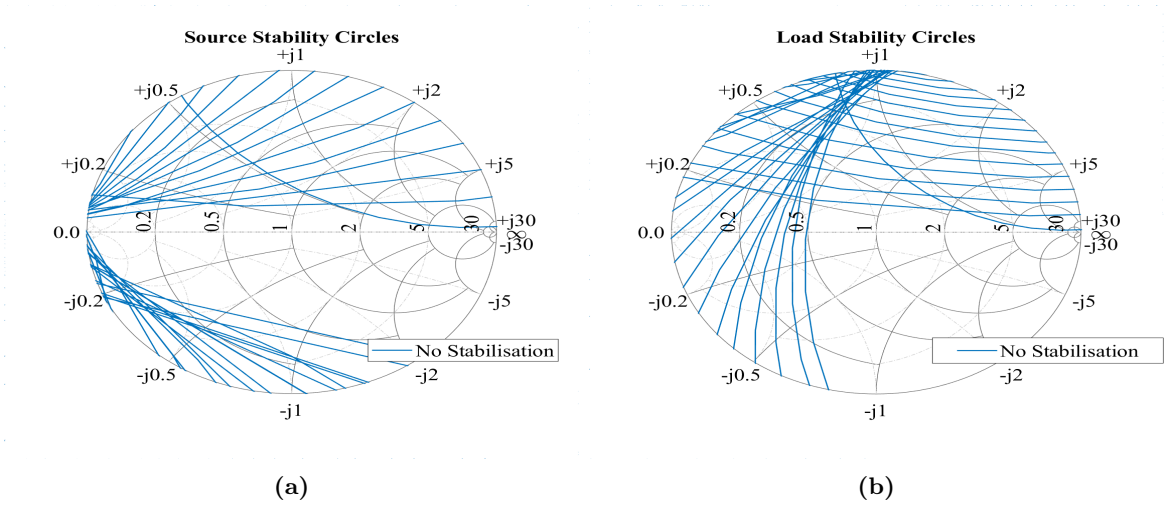


Figure 4.1: Stability factor of the BFU910 transistor grounded with vias.



(a) **(b)**

Figure 4.2: Stability circles of grounded BFU910 transistor. (a) Source stability. (c) Load stability.

A better approach is to evaluate the low-frequency and high-frequency stability region identifiable in Figure 4.1, separately. Consider the stability circles for the device from 10 GHz upwards in Figure 4.3

The stability circles for the device from 10 GHz is more appealing as a definite region of stability can be identified in the load stability circles plot. By adding a 25 Ω series resistor on the output, unconditional stability can be achieved for the frequencies above 10 GHz. Figure 4.4 shows the stability factor and stability circles for the device after the addition of a 25 Ω resistor in series on the output. After the addition of the 25 Ω it stabilised the device at high frequencies.

The next frequency stability analysis is done at frequencies below 8 GHz. Figure 4.5 shows the stability circles for the device below 8 GHz. Evaluating the stability circles in Figure 4.5, a shunt resistor can be identified that will provide unconditional stability for frequencies below 8 GHz. A series resistor at the input of the device is another possibility but adding resistive stabilisation on the input was avoided to achieve optimal noise figure.

In summary, the device was grounded to include grounded via effects on the device

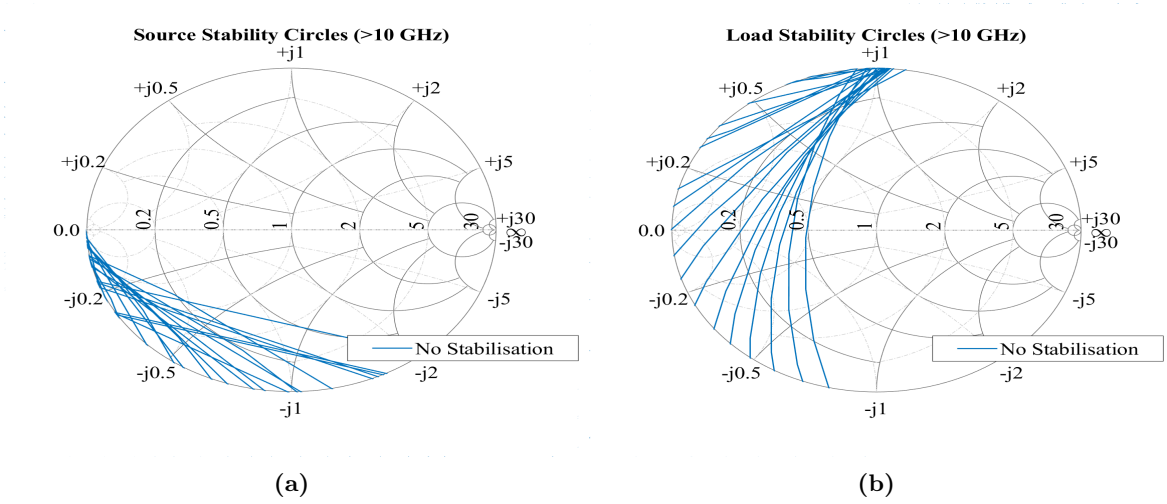


Figure 4.3: Stability circles of grounded BFU910 transistor for frequencies higher than 10 GHz. (a) Source stability. (c) Load stability.

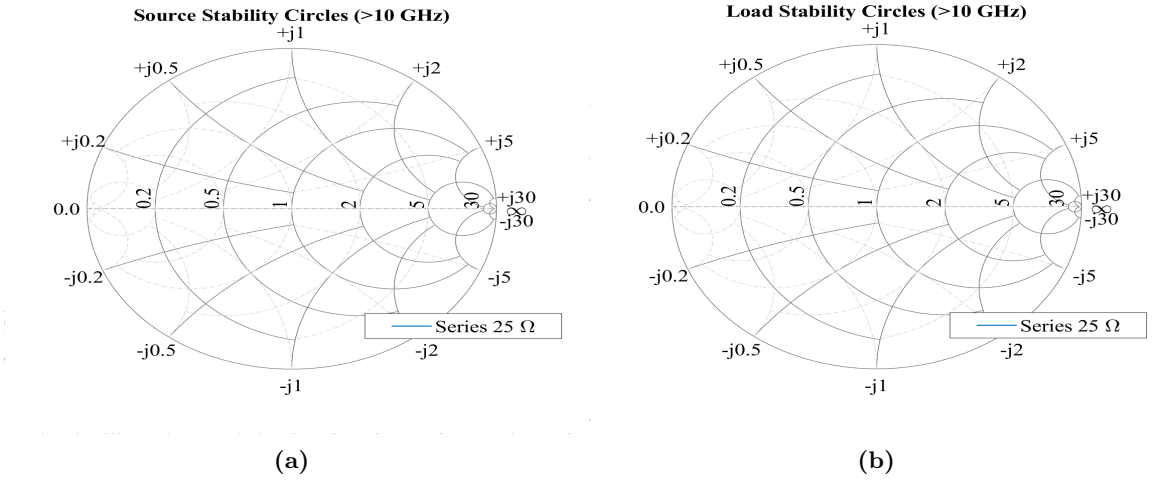


Figure 4.4: BFU910 transistor with series 25Ω output resistor. (a) Source stability. (c) Load stability.

stability. Thereafter a series resistor was added for unconditional stability at high frequencies. An added shunt resistor on the output provides the necessary low-frequency stability. Figure 4.6a shows the resulting stability circuit.

However, the designed resistive stability circuit severely degrades gain and noise performance, especially given that the device was already stable inside the operating frequency range. Recall that the shunt resistor is unnecessary for stability at high frequencies. Therefore to isolate this resistor from the circuit at high frequencies a series inductor is added in series with the shunt resistor to preserve gain at high frequencies while still achieving the required stability at low frequencies.

The series resistor stabilises the transistor at high frequencies and therefore can be added in parallel with an inductor. The inductor act as a short circuit at low frequencies to bypass the resistor and at high frequencies act as an open circuit allowing the resistor to stabilise the device. The resulting circuit is shown in Figure 4.6b.

The purpose of this section is to develop a general stability circuit for the BFU910 transistor. Different realisations of this general stabilisation circuit are implemented during the design of the low noise amplifiers. This section presented a general stability circuit for the BFU910 transistor.

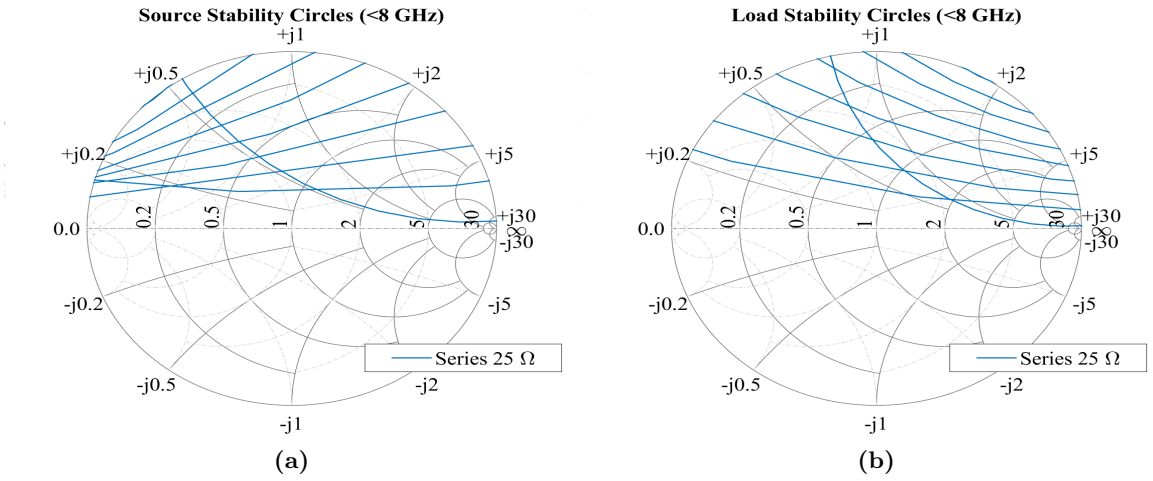


Figure 4.5: BFU910 transistor with series 25Ω output resistor for frequencies below 8 GHz. (a) Source stability. (c) Load stability.

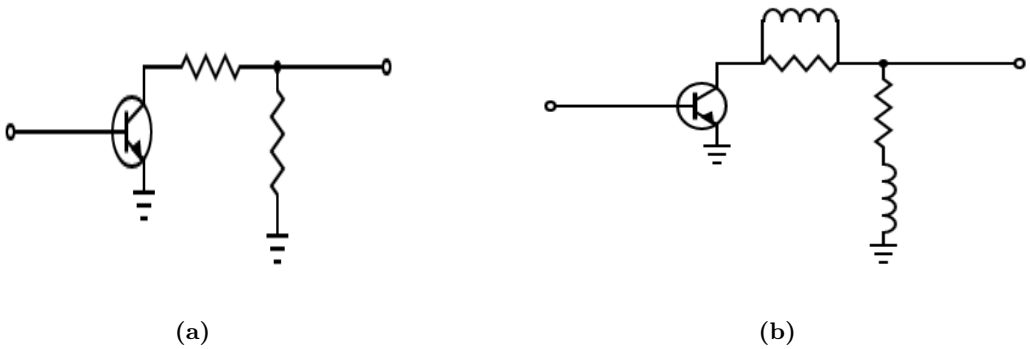


Figure 4.6: (a) General stability circuit. (b) General stability circuit with added inductors.

4.4 Component Selection

The previous section discussed the general stabilization of the BFU910 transistor. In the previous section ideal lumped elements is used to realize the stability circuit of the device. In practical high-frequency circuits the surfacemount components include parasitic effects and the components do not perform ideally. This section aims to identify components that can be used in the design of the low noise amplifier. This include evaluating component models supplied by manufacturers and confirm these models in a suitable measurement setup.

4.4.1 Measurement Setup

During the characterisation and prototyping process, many measurements are taken. Therefore screw-on connectors are used in this project to ease the setup process between measurements. Measurements are also done at frequencies in excess of 25 GHz and therefore Cinch 2.92 mm connectors are selected for this purpose. For an improved coaxial- to microstrip transition, the microstrip is slightly tapered where the connector pin connects to the microstrip. Figure 4.7a shows the model as simulated in HFSS and Figure 4.7b define the taper dimensions. A parameter sweep of W_{taper} is performed to improve the VSWR at the port. The VSWR results for W_{taper} of 0.25 mm, 0.4 mm and 0.65 mm are

shown in Figure 4.7c. A taper Width W_{taper} of 0.4 mm is selected.

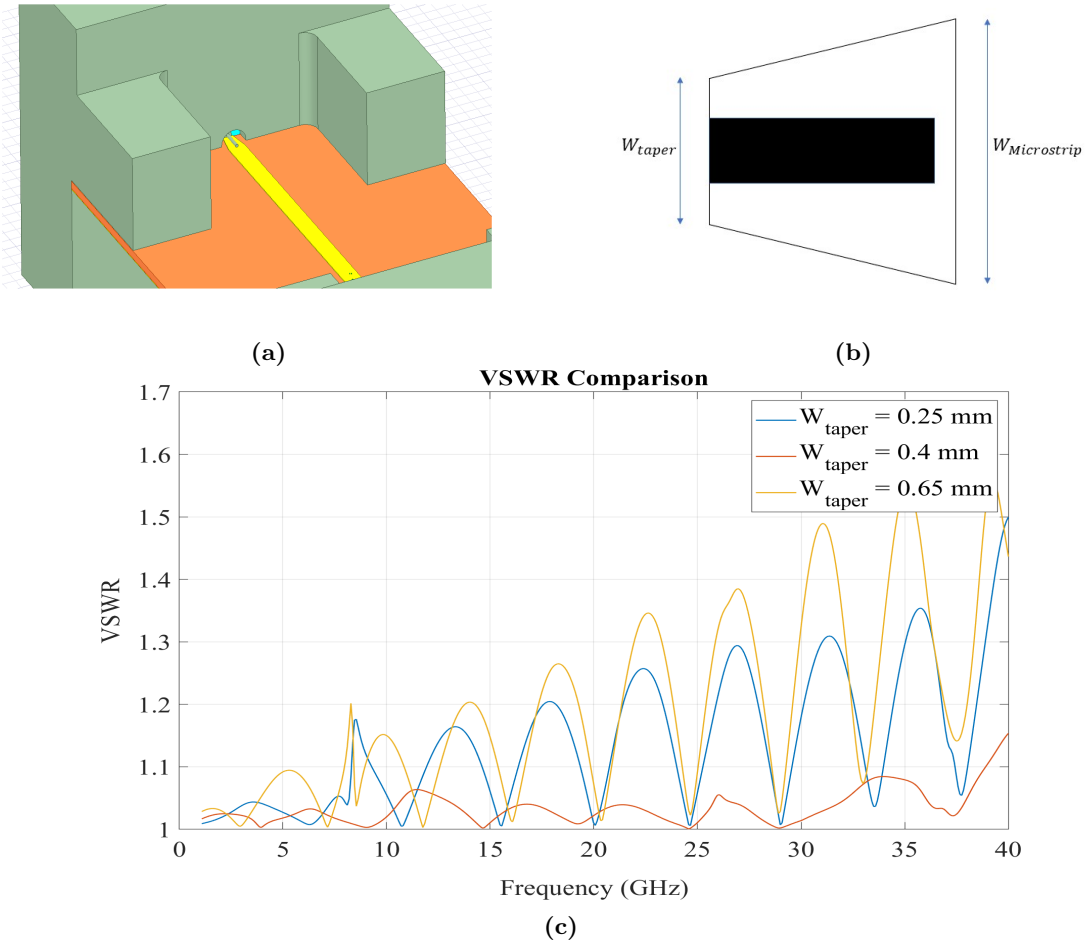
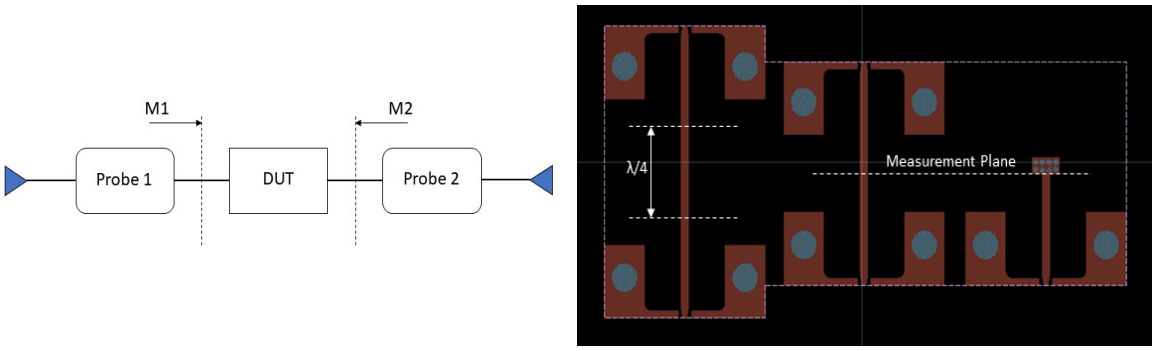


Figure 4.7: (a) Simulated Cinch screw-on connector in HFSS. (b) Transmission line end taper parameter definitions. (c) Simulated VSWR at the connector port for different values of W_{taper}.

As frequencies increase loss in a short piece of microstrip become significant. It is necessary to remove these influences from the measurement circuit to characterise the component alone. The de-embedding scheme selected for this purpose is the Thru-Reflect-line (TRL) [48] technique. Three calibration standards, as shown in Figure 4.8b, are needed for implementation [49].

- **Thru:** M1 and M2 as shown in Figure 4.8a and are connected with zero phase between them
- **Line:** Transmission line with a phase difference of 20° and 160° compared to the Thru standard.
- **Reflect:** Two identical high reflection standards. The reflection coefficient can be unknown, a big advantage as it is not possible to implement a perfect short or open with microstrip.

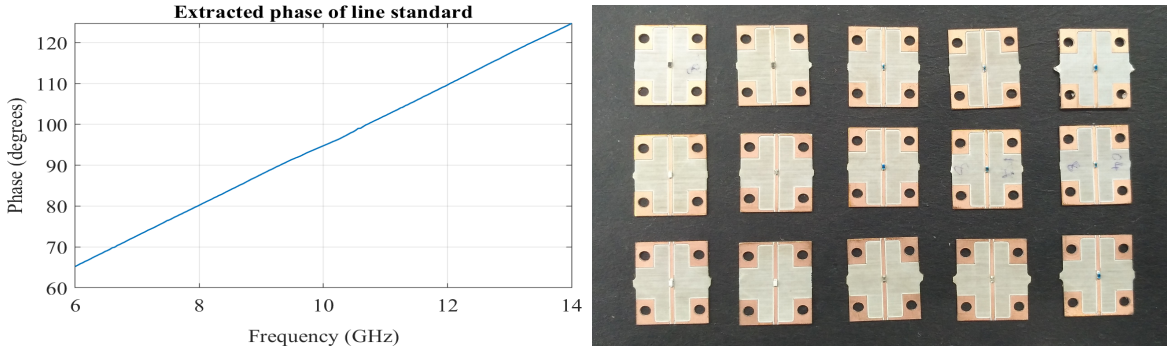
De-embedding is performed from 6-14 GHz. A short is used for the reflect. The line standard has a transmission line with a phase shift of $\lambda/4$ at the geometric mean frequency. Figure 4.9a shows the extracted phase shift between the thru and line standard.



(a) (b)

Figure 4.8: (a) Block diagram of a general measurement setup. (b) Board layout of the TRL PCB with indicated measurement planes.

It is visible that the TRL extracted phase is still between the 20-180 degree requirement. Figure 4.9b shows a few of the components characterised.



(a) (b)

Figure 4.9: (a) Extracted phase of the line standard . (b) Measured components.

4.4.2 Component selection

This section investigates the available components that perform sufficiently at X-band frequencies. The measurement setup described in the previous section is used to confirm the operation of these components. High precision in-house manufacturing is not always possible and may result in small errors in the measurement.

4.4.2.1 Resistors

This section describes the evaluation of high-frequency resistors considered for this project. Note that bias resistors are not included as it does not affect high-frequency performance assuming that the bias circuit is well isolated from the RF circuit in the operating frequency band. From Section 4.3 it can be assumed that resistor values are most likely under 50Ω. Resistors identified include a 10Ω, 25Ω and 50Ω resistor from Vishay as well as a 25Ω manufactured by ATC. Figure 4.10 shows the $|S_{21}|$ plot of the measured resistors compared to their manufacturer supplied models.

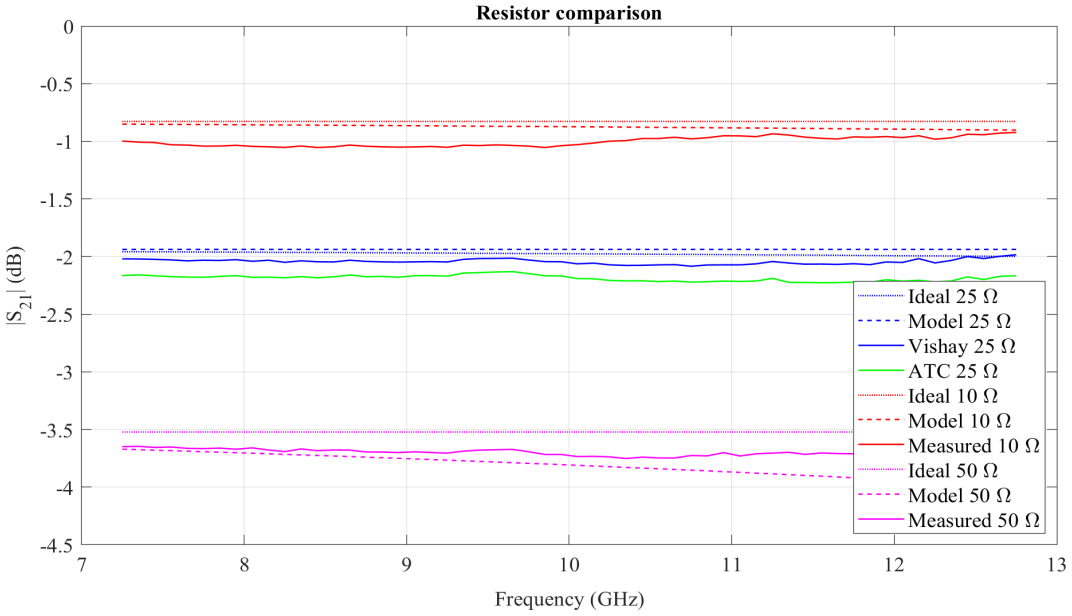


Figure 4.10: Selection of high-frequency resistors.

It is necessary to identify a high-quality resistor, especially for the series stability resistor on the output as it is directly in the signal path. A lower quality resistor can be used for the shunt stability resistor as it has minimal influence at the higher frequencies due to the shunt inductor in the general stability circuit derived in Section 4.3.

4.4.2.2 Inductors

One of the purposes of inductors in an LNA is to block high frequencies over specific bandwidths, i.e. act as an RF choke. The inductors identified to use in this project are 0402 wire-wound inductors manufactured by Murata. Two inductors are present in the LNA designed in this project. This includes a high impedance RF choke inductor on the input and a lower impedance inductor output of the LNA. The RF choke at the input should provide as much isolation to the bias circuit as possible. The inductor on the output forms part of the stability circuit, as discussed in Section 4.3. For low-value inductors, the self-resonant frequency of the inductors are not close to the frequency band and can often be assumed ideal or at least in good agreement with vendor-provided models. However, when implemented as an RF choke the self-resonant frequency is in the operating frequency band and therefore crucial that it is characterised. Inductor values of 7.5nH, 8.2nH and 8.7nH are tested as all of them provide a high degree of isolation in the desired frequency according to their simulation models. Figure 4.11 shows the measured $|S_{21}|$ of the inductors compared to manufacturer provided models. The inductors are measured in series.

4.4.2.3 Capacitors

Capacitors are used as a DC block on the output and also as a high-frequency short circuit to ground where DC and RF are mixed. The ideal capacitor for the RF short is one that only blocks DC and passes all RF frequencies. This, however, is only possible for ideal capacitors. For a capacitor to provide an RF short at low frequencies, it requires a high capacitance. Large capacitors self resonate at low frequencies and are not able to be used as an RF short at higher frequencies. Small capacitor values, on the other

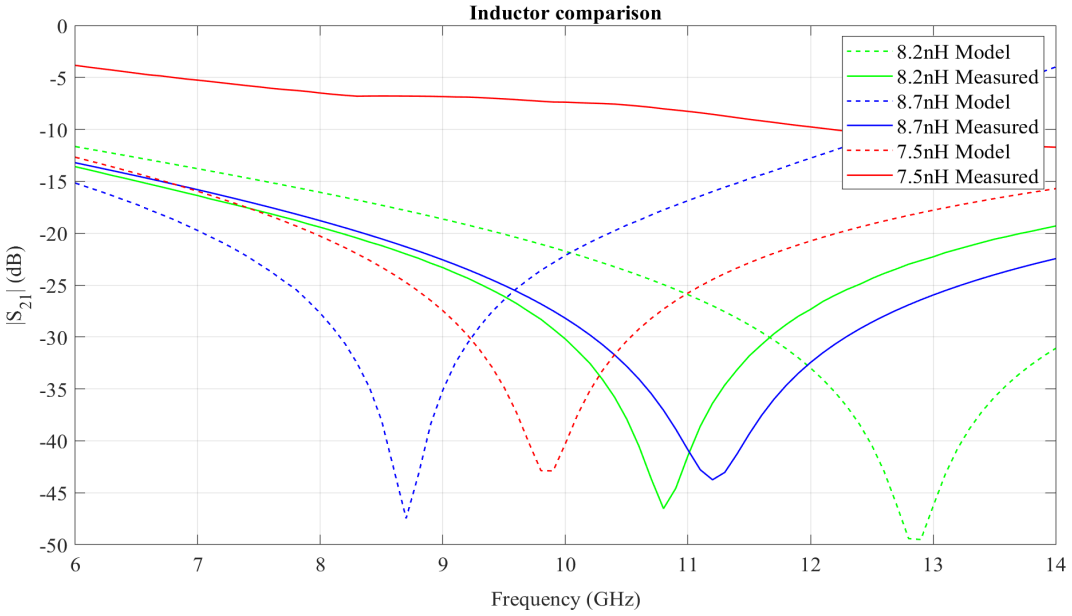


Figure 4.11: Selection of RF choke high frequency inductors.

hand, resonate at higher frequencies but does not provide small enough impedance at low frequencies to act as an RF short. The capacitors identified for this purpose are two $0.1\mu F$ capacitors manufactured by American Technical Ceramics (ATC) only differing in package size. Figure 4.12a shows the insertion loss of the capacitor up to 19.5 GHz.

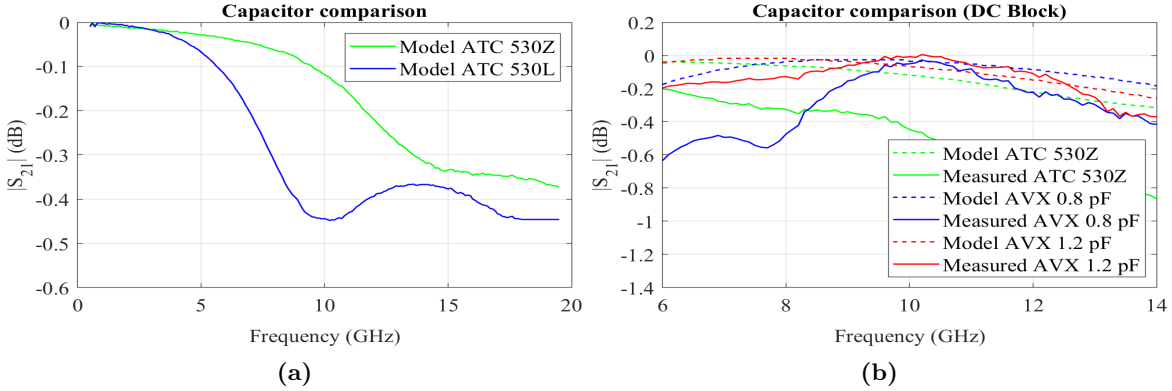


Figure 4.12: (a) Wide-band RF short capacitors. (b) Selection of DC block capacitors.

From the results shown in Figure 4.12a, the ATC530Z capacitor is selected as a wide-band RF short. The output DC block prevents DC coupling to the devices connected after the LNA in the RF chain. The DC block is directly in the signal path and therefore should have as little as a possible influence one the LNA in the operating frequency band. Three capacitors considered for the DC block is the ATC 530Z capacitor as well as 0.8 pF and 1.2 pF capacitors from AVX. Figure 4.12b shows the de-embedded insertion loss from 6-14 GHz.

This section discussed a number of lumped components that operate sufficiently in the operating frequency band. The next section discusses the design of an initial LNA prototype.

4.5 LNA Prototype 1

The previous section discussed the available components that perform sufficiently in the frequency band of interest. This section describes the design of the first prototype LNA. Main objectives for this prototype is to implement the bias and stability circuit and compare the measured results with simulations. Simulations are performed in Keysight's Advanced Design System (ADS). An especially useful feature is the Electromagnetic Co-Simulation. Electromagnetic Co-Simulation allows standard circuit simulation of the circuit components such as transistors and lumped components while taking into account interactions between layout elements. It also provides a more accurate simulation of components such as vias.

4.5.1 Stability Circuit

This prototype is measured in a 50Ω system at the input and output terminals of the device. Therefore it is not expected to have an instability problem with this prototype. However, the stability circuit implemented in this LNA is the groundwork for the LNA to be implemented in the antenna array.

To make the device unconditionally stable over a wide frequency band severely reduces performance if not implemented carefully. Therefore it was decided to allow potential instability in order to improve performance.

In phased arrays, there is coupling between the antennas that influence the impedance of the single elements and cause impedance changes over different scan angles. From initial studies of the Vivaldi antenna array in Section 2.5 the antenna impedance of the Vivaldi array capacitive at low frequencies as it approaches open circuit with decreasing frequencies. At this time of development, it is not very easy to set specific stability specifications for the output. This antenna, for instance, only incorporates a single-stage LNA at the output. Future iterations of this array will most probably consist of a two or three-stage LNA which will require a different stability analysis where the interstage impedance is included in the analysis. This makes use of techniques such as [50] where a so-called S-probe is inserted into the circuit, a feature available in ADS. Therefore the stability region on the input should be as large as possible to accommodate variation in antenna impedance while the output stability circle are designed to be at least stable for loads with approximate VSWR of 2:1.

Following the design process in Section 4.3 with reference to the practical components from Section 4.4.2 the following circuit was derived

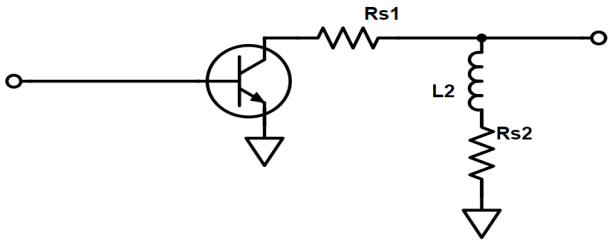
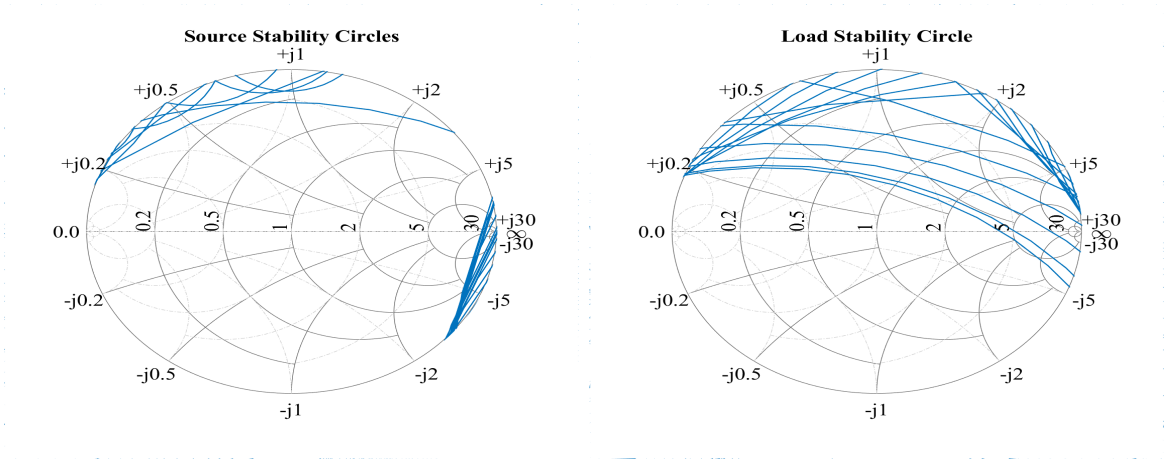


Figure 4.13: Stability circuit for the first prototype LNA.

where R_{S1} and R_{S2} are the 10Ω and 25Ω Vishay resistors respectively. A $3.3nH$ inductor is added at the output as part of the stability circuit to allow the 25Ω resistor to stabilise the device at low frequencies without affecting the performance of the device too much at high frequencies. The final stability circles from 2-18 GHz are shown in Figures 4.14a and 4.14b.

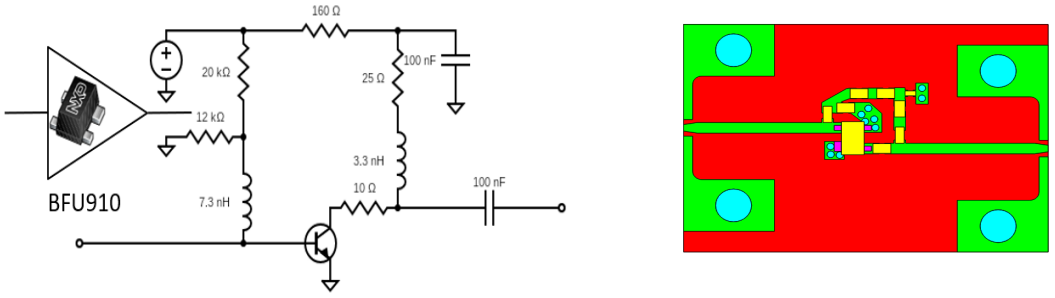


(a) **(b)**

Figure 4.14: (a) Source stability circles of LNA prototype 1. (b) Load stability circles of LNA prototype 1.

4.5.2 Biasing Circuit

The transistor is biased for optimum noise with $V_{CE} = 2V$ and $I_C = 6mA$. For a smaller LNA footprint, it is decided to incorporate the stability circuit into the biasing circuit. The final circuit is shown in Figure 4.15a



(a) **(b)**

Figure 4.15: (a) Circuit schematic of the first prototype LNA. (b) Layout of the first prototype LNA.

The inductor L_1 act as RF bias choke between the RF path and DC biasing circuit at the input. To be able to integrate the stability circuit into the bias circuit, a wideband capacitor is added for an RF ground. The remainder of the resistors form part of the bias circuit. The circuit is supplied with $V_{CC} = 3.3V$.

4.5.3 Measured Results

Figure 4.16 shows the measured results compared to simulations of the initial LNA.

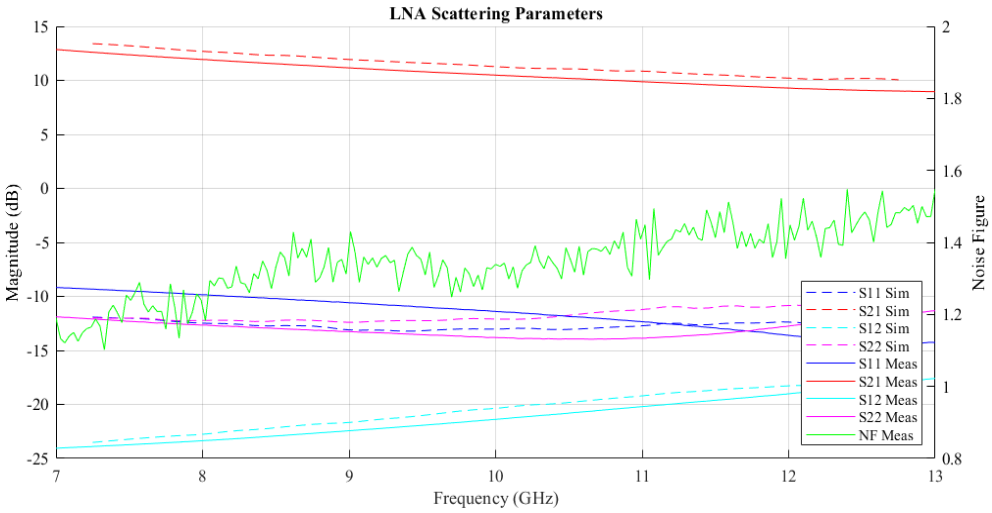


Figure 4.16: S-Paramters and noise figure of the first prototype LNA.

Fairly good comparison is achieved between the measured and simulated results. S_{21}, however, is slightly lower than expected. Overall LNA prototype 1 provides the necessary confidence in the simulation setup.

4.6 Antenna LNA Design

The previous section discussed an initial LNA design that set the groundwork for the final LNA. This section discusses the design of the LNA for the active antenna array.

4.6.1 Stability analysis

As with first LNA prototype, the output 10Ω series resistor is for stability at high frequencies and the 25Ω shunt resistor on the output is used for low-frequency stabilisation. For this design, the value of the shunt inductor on the output is reduced to 2.2 nH increase the stabilising effect of the shunt resistor at lower frequencies. Figures 4.17a and 4.17b shows the source and load stability circles.

4.6.2 Bias Circuit

Two of the problems identified in the first LNA prototype in Section 4.5 is power consumption and β-stability. According to research [34], the bias circuit of the first LNA prototype is not stable against changes in β. Therefore it was decided to change the circuit to a variant of the circuit in Figure 2.23c. Note that this topology is not optimal for stability against changes in temperature [34]. Although this is of concern for the later iterations of this array that may be introduced to harsh environments, this array will mainly be used for laboratory testing where the temperature stays relatively constant. Note that from the bias circuits analysed in Section 2.8.4.1 the bias circuit in Figure 2.23d provides the best stability against changes in temperature and β, but it was decided not to use this

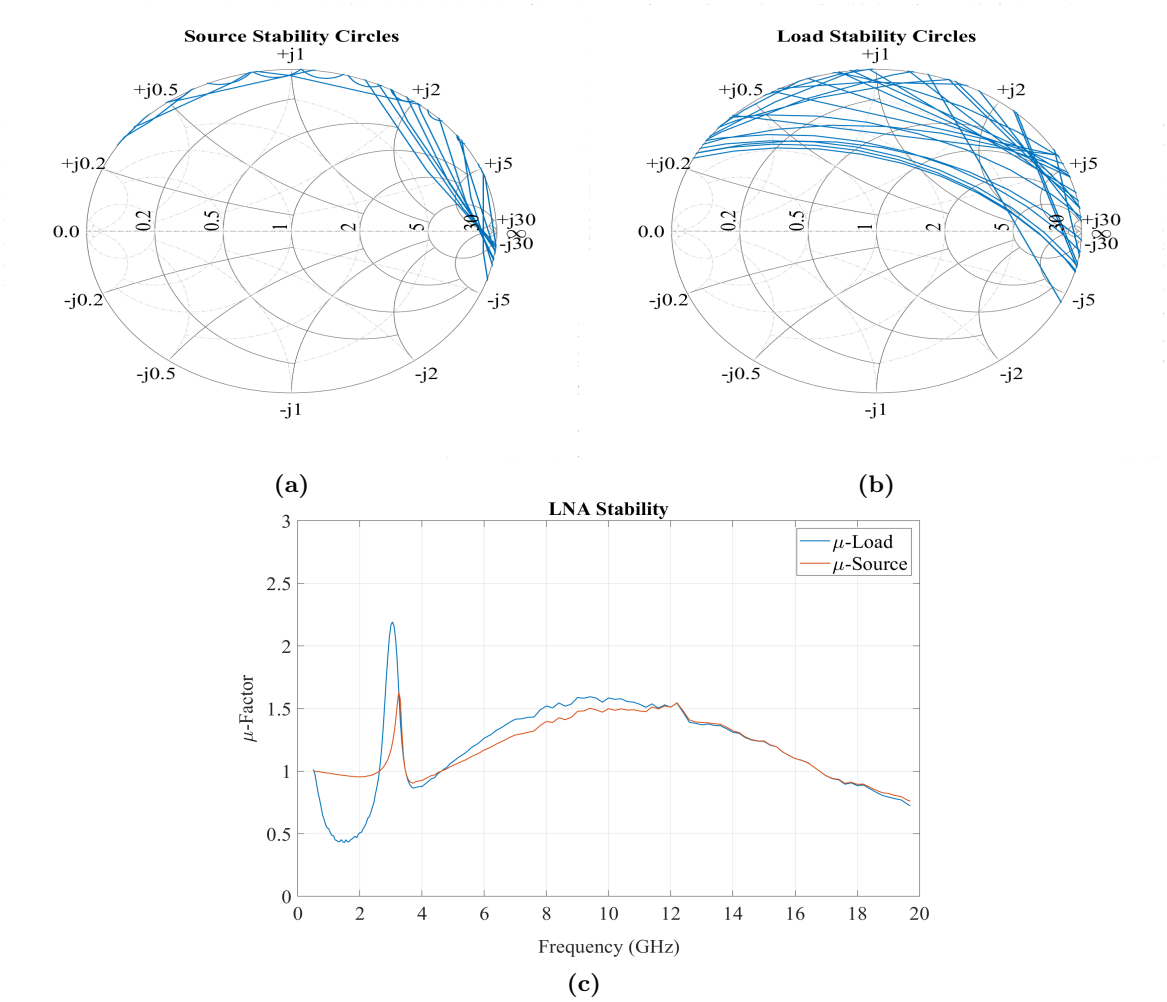


Figure 4.17: Stability analysis of the antenna LNA (a) Source stability circles. (b) Load stability circles. (c) Source and Load μ-factor of the LNA.

circuit and instead supply a good ground for the transistor. The bias circuit implemented is slightly different from the one in Figure 2.23c to include the stability resistors. Figure 4.18 shows the final bias circuit.

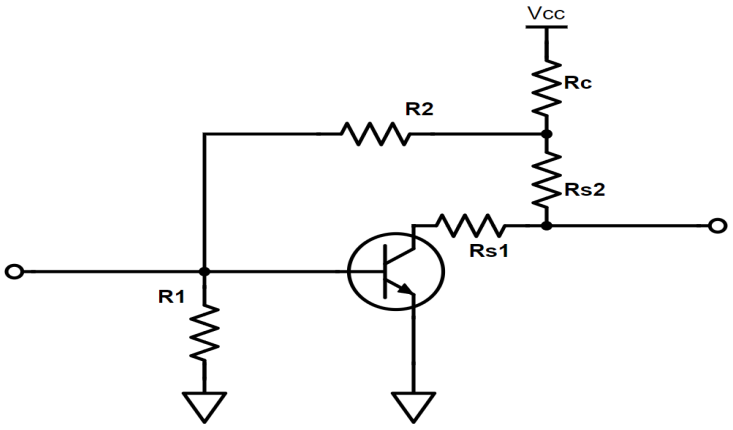


Figure 4.18: Bias circuit for the antenna LNA.

The second problem with the biasing of the initial prototype is power consumption.

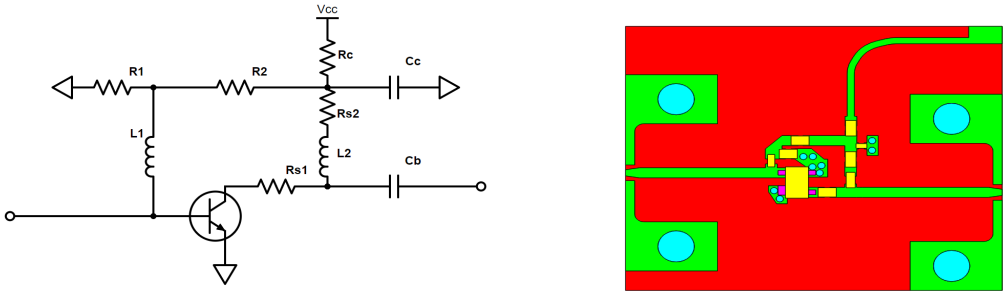
The power consumption due to the DC bias of the transistor is approximately $12mW$. With $5.76mW$ dissipated in the 160Ω it is almost half the power dissipated in the transistor. Power consumption is reduced by using a lower supply voltage, V_{CC}. With the stability resistors included to reduce LNA footprint, the minimum voltage of V_{CC} is approximately $2.21V$. Therefore a common supply voltage of 2.5V is selected with a large number of commercially available fixed voltage regulators to power the LNA. Reducing the power consumption of the single LNA by a few mW become significant in a large antenna array where power consumption may be a problem for the overall design.

Equation 4.1 can be derived using Kirchoff's current law to describe the new DC biasing circuit.

$$V_{BE}\left(\frac{R_2}{R_1 Rc}+\frac{1}{R_c}+\frac{1}{R_1}\right)+I_C\left(\frac{R_2}{\beta R_C}+1+\frac{1}{\beta}\right)-\frac{V_{CC}}{R_C}=0 \tag{4.1}$$

Assuming the base current is much smaller than the collector current of $6mA$, the resistor R_C is calculated as 48.33Ω. The base resistors R_1 and R_2 is selected to minimise power consumption while the current is still large compared to the base current. Resistor R_2 was chosen as $12k\Omega$. From the datasheet, the DC current gain is available as 1900. Using Equation 4.1 resistor $R_1 \approx 7k\Omega$. Confirming these values in the manufacturer supplied non-linear model yields $V_{CE} = 1.95V$ and $I_C = 6.58mA$. E24 standard 0402 resistors are used, and therefore these calculated resistors should be adjusted accordingly. At the base of the transistor, the ratio of the resistors is important and not one of them specifically. R_C, on the other hand, is set and should, therefore, be selected first. The closest value is 47Ω. Resistors in the base voltage divider circuit are chosen as $R1 = 6.2k\Omega$ and $R_2 = 11k\Omega$. Practically implementing the circuit yielded a lower collector current compared to the simulated model. This resulted in the resistors being updated to $R_1 = 12k\Omega$ and $R_2 = 20k\Omega$. The average collector current of six biased transistors measured $I_C = 6.06mA$. Re-evaluating the power consumption of the revised biasing circuit compared to the first LNA prototype, the power dissipation in the 47Ω resistor is approximately $1.7mW$. A reduction of more than than $4mW$.

Another advantage of this bias circuit is that the DC supply is connected to the LNA directly at the wide-band ATC capacitor C_C. Therefore any impedance presented at the LNA by the external DC supply circuit is in parallel with the low impedance of the capacitor and therefore reduces the possibility of affecting the RF performance of the LNA.



(a) **(b)**

Figure 4.19: (a) Antenna LNA circuit schematic. (b) LNA board layout.

Figure 4.20 shows the manufactured LNA and the associated measured results.

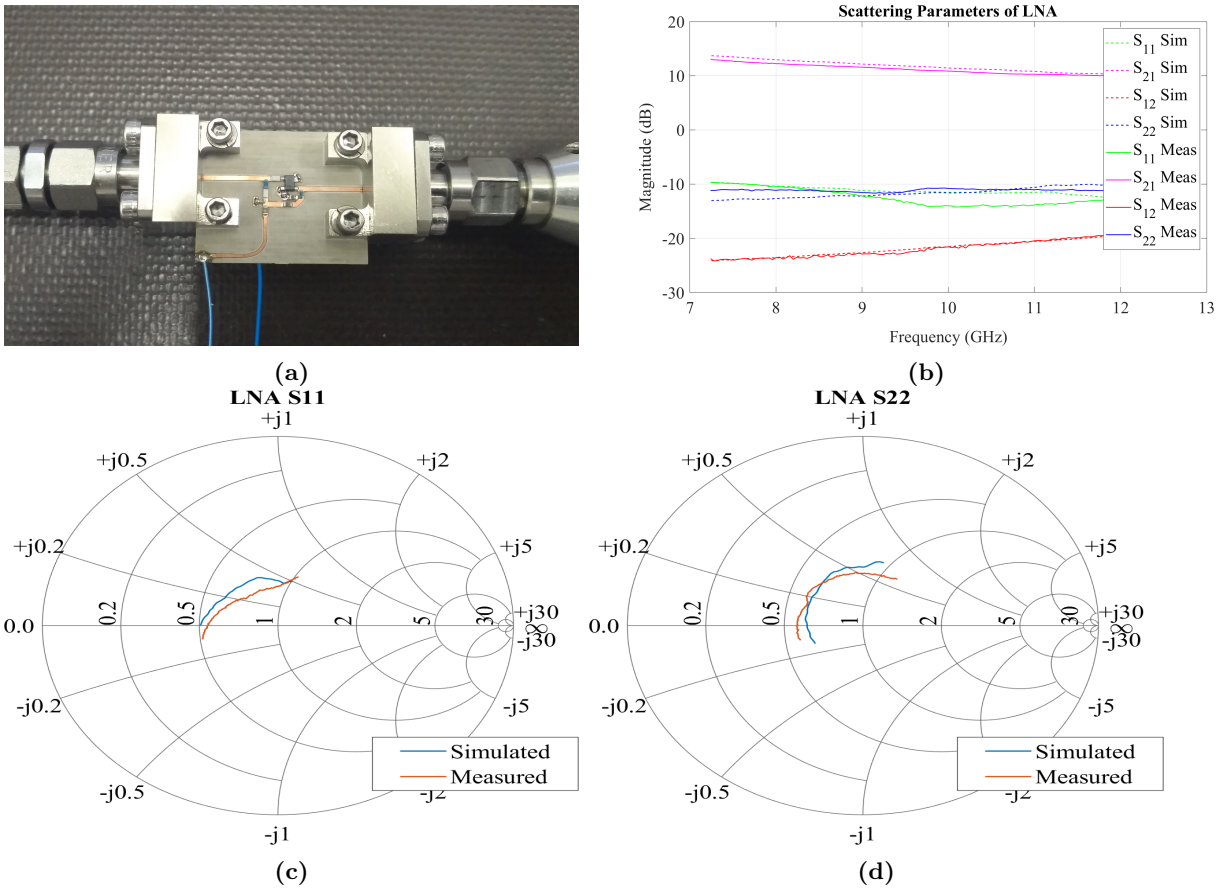


Figure 4.20: (a) Image of the manufactured LNA (b) Simulated and measured S-Parameters (c) De-embedded S_{11} compared with simulations (d) De-embedded S_{22} compared with simulations.

The measured results of the LNA showed good comparison to the simulated results. This section concludes Chapter 4. The chapter designed the LNA integrated at the feed of the antenna to form the active array. The next chapter discusses the system integration of the antenna and LNA.

Chapter 5

System Integration

Chapters 3 and 4 discussed the design of the antenna array element and LNA that are used in the design of the active antenna array. This section discusses the integration between the antenna and LNA to form an active antenna array. Section 5.1 provides a short overview of the system and introduce target specifications. Section 5.2 discusses the co-design of the infinite array element and the LNA followed by the finite array analysis of the active antenna array in Section 5.3. Finally, Section 5.4 describe the DC supply for the active array.

5.1 System Design

This section aims to provide a short overview of the active antenna array system design. The most important components are the antenna and LNA designed in Chapters 3 and 4, respectively. In the design, only a single stage LNA is integrated at the feed of the antenna. This is mainly to reduce the cost of the array. Adding an additional stage to the front-end LNA will significantly increase the cost of the array. It does not only include more components but also more dielectric material and a larger antenna which means more aluminium used during additive manufacturing. Adding another LNA is also not necessary to achieve the objectives of the project. For this initial iteration of the active array, a complete set of target specifications is not established yet. Therefore a few not too stringent specifications were introduced. This includes an LNA noise figure of below 1.5 dB when loaded with the antenna impedance at the input. This should be achieved for scan angles up to 45°. For the DC supply, the antenna is divided into subarrays of two rows each. Each subarray is powered from a single regulator.

5.2 Co-design of the antenna and the LNA

Chapter 4 discussed the design of the LNA. Chapter 3 then proceeded with the design of the antenna to match the optimum noise impedance of the LNA with 4mm 50Ω microstrip between the antenna and LNA. With the direct matching approach followed in this project, where no matching network is added between the antenna and the LNA, the connection between the antenna and LNA only consist of a short piece of 50Ω transmission line.

The main objective of this section includes the evaluation of the noise contribution by the LNA when terminated with the active antenna impedance at the input. Again

circuit simulations are performed in Keysight's ADS. The simulated antenna impedance is represented in ADS with a two-port noiseless network as introduced in Section 2.8.5.

The output of the noiseless network is set to the active impedance of the antenna array element. This section only uses the infinite array impedance. The finite array analysis and corresponding noise analysis is the subject of Section 5.3. The simulation setup is shown in Figure 5.1a. Figure 5.1b, 5.1c and 5.1d shows the noise contribution of the LNA when terminated with the infinite array impedance for different scan angles in the E-, D- and H-plane.

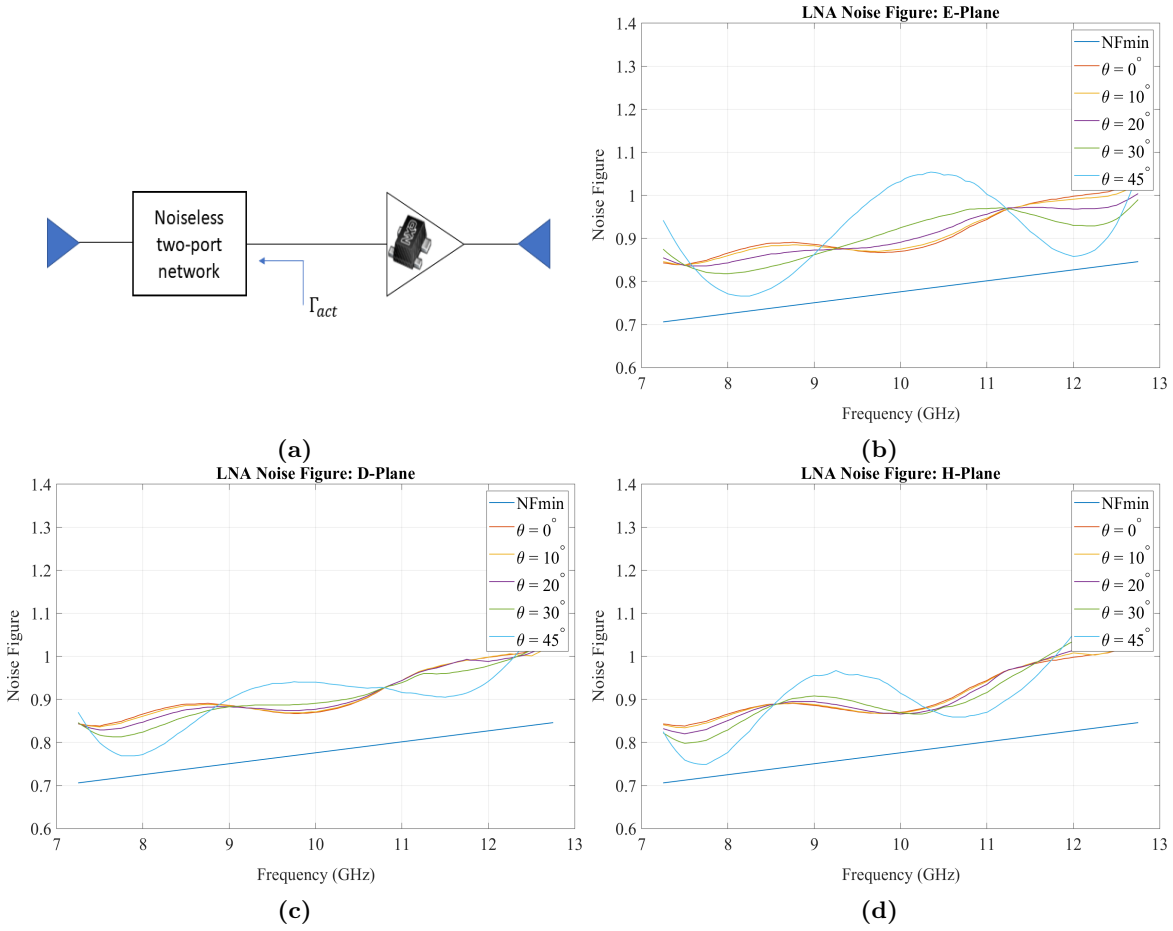


Figure 5.1: (a) Noiseless two-port setup. (b) LNA noise figure for scan angles in the E-plane. (c) LNA noise figure for scan angles in the D-plane. (d) LNA noise figure for scan angles in the H-plane.

5.3 Finite array analysis

Section 5.2 discussed the co-design of the infinite array antenna element designed in Chapter 3 and the LNA as designed in Chapter 4. Section 5.2 also evaluated the noise contribution of the LNA when loaded with the infinite array impedance at the input. The purpose of this section is to move the array analysis from the infinite array environment to a finite analysis.

It is common knowledge that when reducing the size of the array, the impedance of the elements is affected. Especially the edge element can be severely compromised. "Dummy" elements are often added at the edge of the array to mitigate edge effects so that the measured elements perform closer to the designed infinite array environment.

Holter and Steyskal [51] studied these truncation effects and suggested an array size of $5\lambda \times 5\lambda$. In narrow-band arrays spaced at approximately a half-wavelength, it results in a 10×10 array which is quite large but reasonable. However, in wide-band arrays where the elements are spaced at half-wavelength apart at the highest frequency the elements the lowest frequency, dependent on the bandwidth of the antenna, can become very small in terms of wavelength. At 7.25 GHz, the lowest design frequency in this project, the element spacing is approximately 0.29λ. At 0.29λ, 5λ results in 17.24 elements therefore an array size of 18×18 or 324 elements. Financially that is not feasible, especially for such an early prototype array in the design process.

Therefore in this section, different finite array sizes are simulated and compared to find an appropriate size for the finite array. The goal is to manufacture an array as small as possible to still achieve good agreement between the infinite array and finite array analysis. The finite array analysis starts by analysing the infinite-by-finite array for an increasing number of elements. Finite array analysis is performed in Ansys HFSS. The infinite-by-finite array analysis is performed for 5, 7 and 9 elements. Figure 5.3a shows the 7 element infinite-by-finite array.

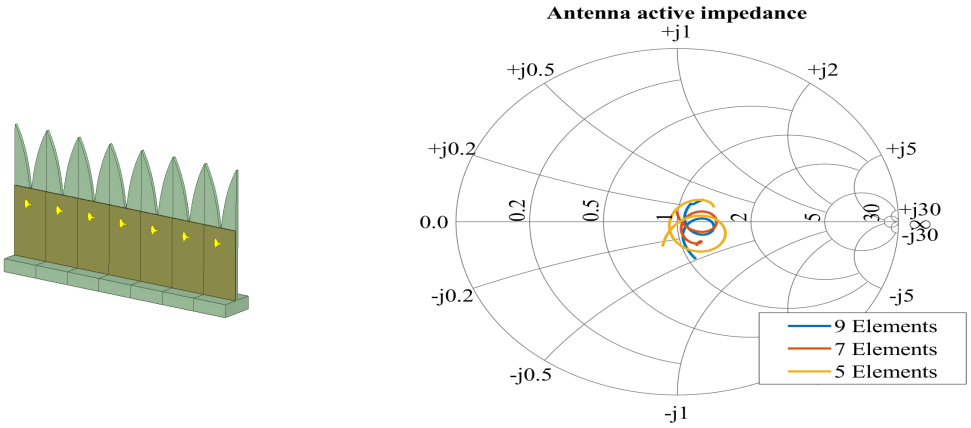


Figure 5.2: (a) Simulation setup of the $7 \times$ infinite array. (b) Simulated results for the infinite-by-finite arrays.

The simulated 9 Element infinite-by-finite array shows acceptable agreement to the infinite array. A 9×9 array is still large number of elements for a prototype array, and a number of other layouts were analysed in an attempt to reduce the number of elements.

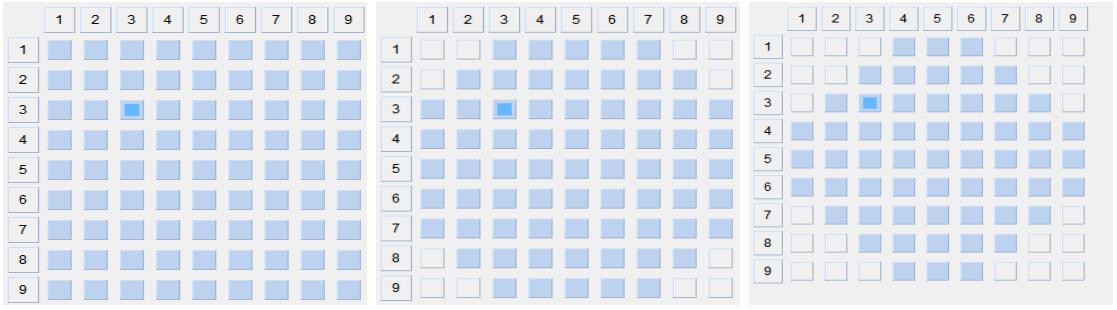


Figure 5.3: Smaller layouts analysed to reduce number of elements.

The smaller versions did not yield acceptable results. It was decided to accept a slightly skewed radiation pattern and therefore an array of 8 × 8 or 64 elements was included in the finite array analysis. Figure 5.5a shows the Infinite-, infinite-by-finite- and the finite array simulation of the 64 element array. The 64 element array showed good agreement between the infinite- and finite array impedance.

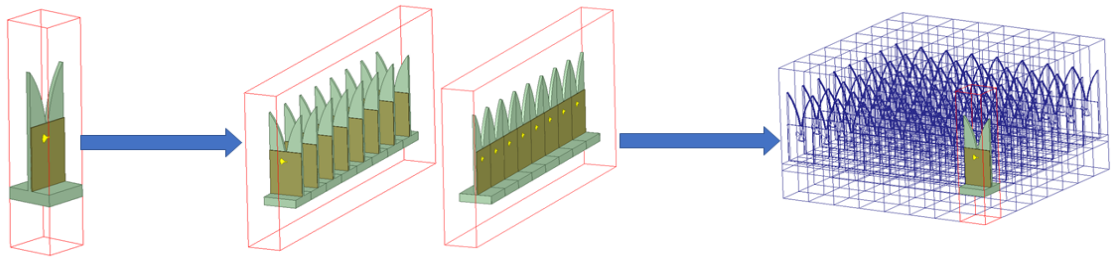


Figure 5.4: Design process of 64 element finite Vivaldi array.

As with the infinite array noise analysis in Section 5.2 the setup in Figure 5.1a is used to evaluate the noise performance of the LNA when terminated with the active impedance of the array at the input of the LNA.

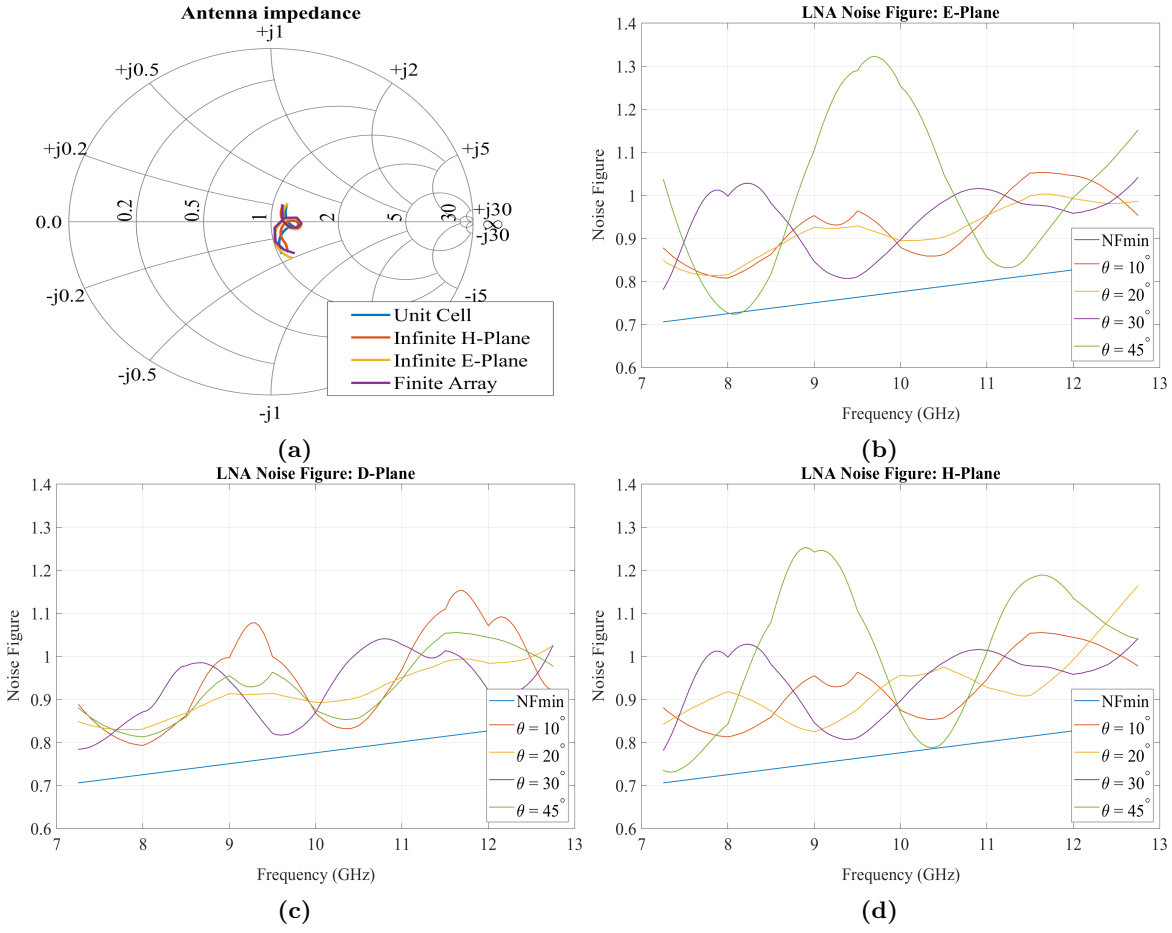


Figure 5.5: (a) Active impedance of passive Vivaldi array. (b) LNA noise figure for scan angles in the E-plane. (c) LNA noise figure for scan angles in the D-plane. (d) LNA noise figure for scan angles in the H-plane.

5.4 DC distribution circuit

The previous sections discussed the design and development of the active antenna array. Throughout the design, V_{CC} was used as the supply voltage and more importantly assumed to be constant. A stable V_{CC} is essential as this influence the quiescent point of the transistor that in turn, change the high-frequency performance. This section discusses the DC supply of the active antenna array.

A single voltage regulator circuit is integrated to supply a bias voltage to two rows of antennas. In other words, four regulator circuits for the entire array. A choice between switching- and linear regulators exist. Switching power supplies are very power efficient but can introduce unwanted interference as a consequence of its switching frequency into the signal chain. This has the possibility of being detrimental in high-sensitive applications if not considered during the design process. On the other hand, linear regulators supply a stable low noise voltage, but at the cost of power efficiency. Another advantage is a high power supply rejection ratio (PSRR) that reduce the unwanted ripple frequencies generated by components such as switching power supplies. The approximate power dissipation P_D in a regulator is [52]

$$P_D \approx V_{IN}(I_{GND}@I_{OUT}) + I_{OUT}(V_{IN} - V_{OUT}). \tag{5.1}$$

Equation 5.1 shows that as the voltage difference between the input voltage V_{IN} and output voltage V_{OUT} of the regulator increase the power dissipation increase. This is mostly dissipated as heat. For reduced power dissipation in a regulator, the input voltage should be as close as possible to the output voltage. Other important specifications applicable to any regulator is a good line- and load regulation. The NCV8114 [52], an inexpensive low dropout voltage regulator (LDO) from ON Semiconductor, is selected. A single regulator circuit is shown in Figure 5.6.

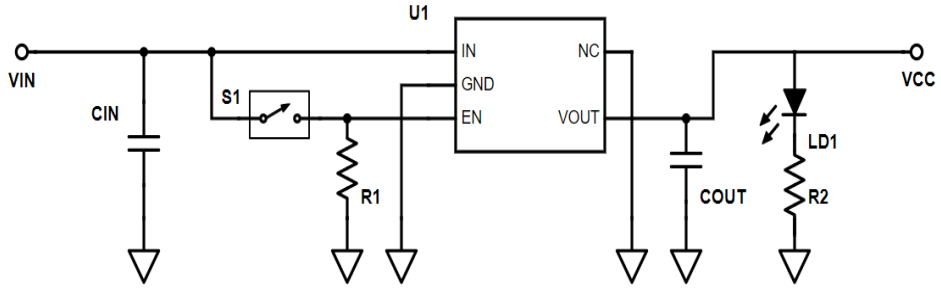


Figure 5.6: Antenna array regulator circuit

Here capacitors C_{IN} and C_{OUT} is the manufacturer recommended $1\mu F$ X5R input and output capacitors. Resistor $R1$ act as pull-down resistor and resistor $R2$ set the current through the LED $LD1$ that indicates that a specific row is powered.

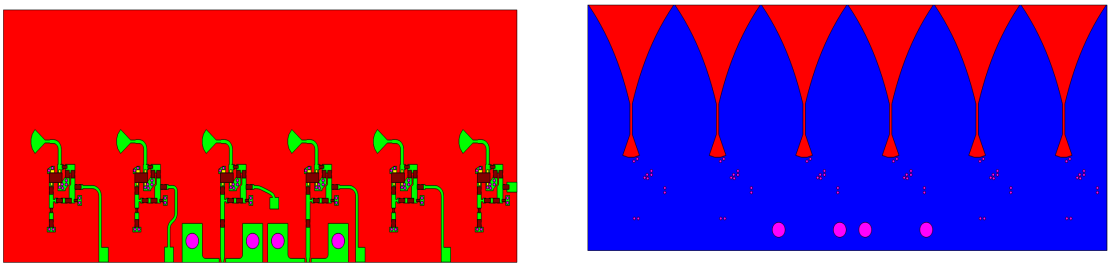
Chapter 6

Prototype Development

6.1 Linear Vivaldi array prototype

Chapter 3 discussed the design of the antenna array element. Chapter 4 described the design of the LNA for the active antenna array. Chapter 5 combined the work presented in Chapters 3 and 4 and discussed the integration between the antenna and the LNA. At this point, the LNA was well characterised independent of the antenna but not tested when introduced in the antenna environment.

Therefore a six-element linear full-dielectric Vivaldi array is built as a final prototype before manufacturing the full 64 element antenna. A simple design is implemented. The antenna was designed to match the input impedance of the LNA at broadside. Objectives for this array is to evaluate if the LNA is stable at all frequencies, a reasonably constant gain is achieved at broadside and to establish a sufficient measurement setup that can be used for the measurement of the final array. The layout of the array is shown in Figure 6.2.



(a) **(b)**

Figure 6.1: (a) Top-layer of 6 element linear array. (b) Bottom-layer of 6 element linear array.

When the LNA is integrated at the feed of the antenna, the antenna is no longer reciprocal. Therefore the antenna is simulated using plane-wave excitation from different angles to determine the embedded element patterns. The simulation setup performed in FEKO is shown in Figure 6.2a.

Firstly the three antenna method discussed in Section 2.10 are used to measure the absolute gain of the antenna at broadside. One of the three antennas low frequency cuttof is 8.4 GHz and therefore the measured frequencies are from 8.4 GHz to 12.8 GHz. Figure 6.2b shows the gain of the third element. The following measurement is an E-plane scan of

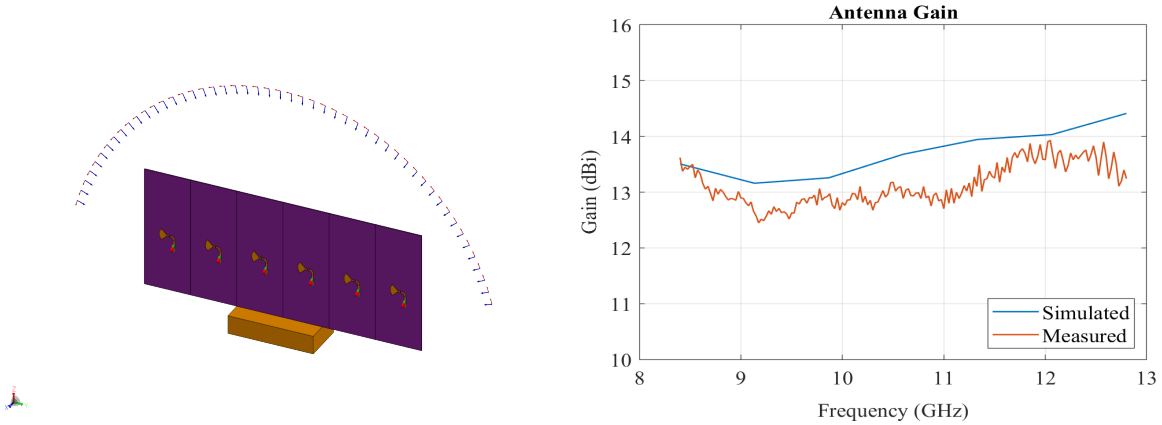


Figure 6.2: (a) Simulation setup. (b) Antenna element gain of 6 element linear array.

the antenna array. Figures 6.3 shows a comparison between the simulated and measured normalised receive power.

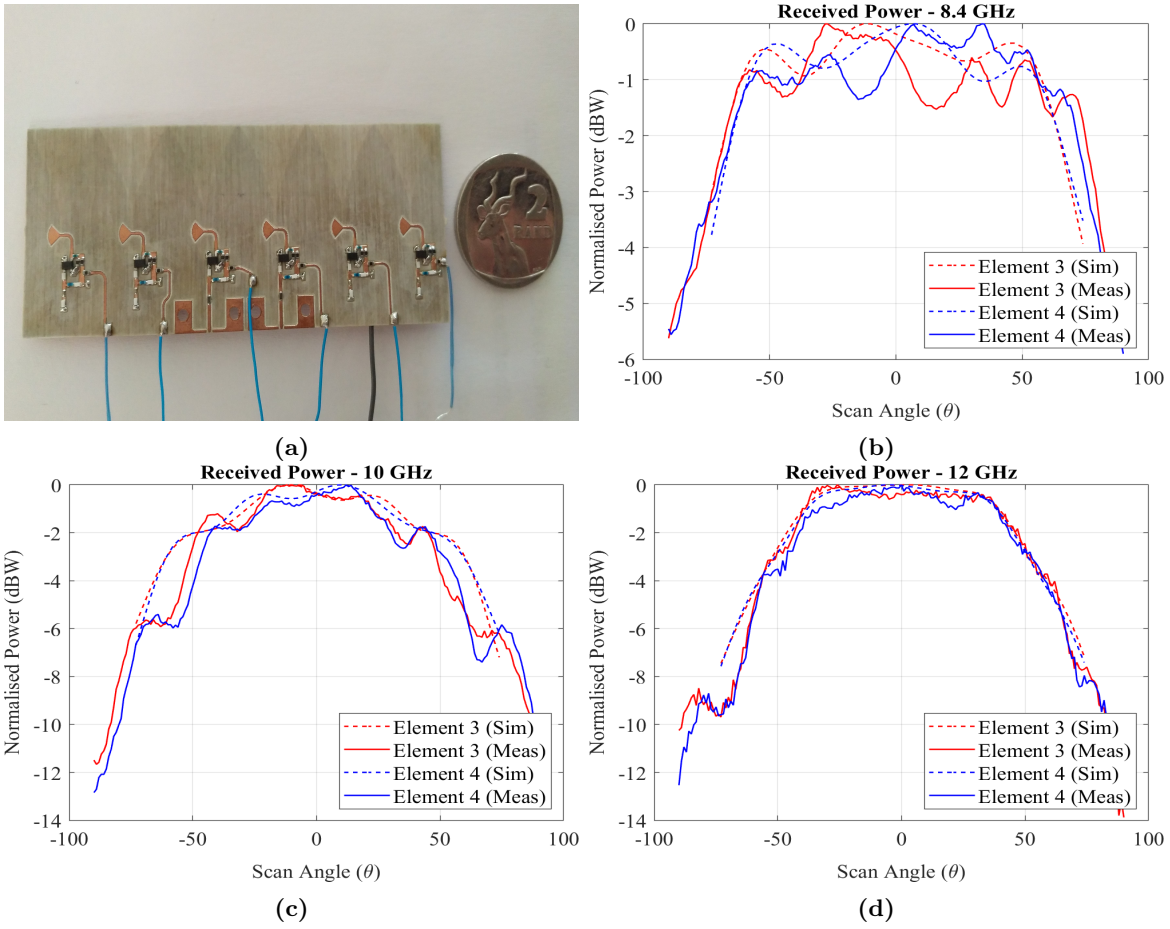


Figure 6.3: (a) Manufactured linear Vivaldi array. (b) E-plane scan at 7.8 GHz. (c) E-plane scan at 10 GHz. (d) E-plane scan at 12 GHz.

Evaluating the gain Figure 6.2b shows a relatively constant gain over the frequency band of interest but lower than expected. However, the gain measurement at broadside is not very intuitive and provide very little to learn from this antenna. The E-plane scan results provide better information than the broadside gain measurement. In Figure 6.3,

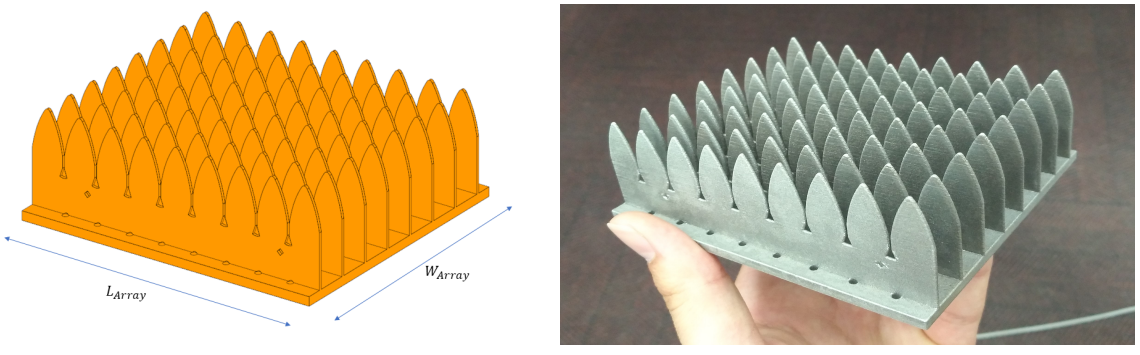
it can be seen that at lower frequencies, the variation in gain increases. This is caused by increased variation in impedance changes that cause a mismatch between the antenna and the LNA.

Another interesting observation is the asymmetry that is present on the same side in the beam patterns of element 3 and 4 of the array. In Figure 6.3d for instance there is a small lobe at $\theta = -80°$ that is not present at $\theta = 80°$. This may point to influence from the feed present on the right side of the antenna elements. In conclusion, the beam patterns did not follow the simulations perfectly, but several things were learned from this antenna. The LNA was stable at all frequencies, and lastly, a measurement setup was established that is sufficient for measurements of the 64 element array. The next sections proceed with the assembly of the 64 element Vivaldi array prototype.

6.2 Assembly and manufacturing of the final array

6.2.1 DMLS aluminium additive manufactured antenna

Currently, in South Africa, not many companies provide metal additive manufacturing. At the time of manufacturing, SLM was not available, and DMLS manufacturing was used for the manufacturing of the final array. Key specifications include a layer thickness of $40\mu m$ and x-,y- tolerances of 0.1 mm. DMLS manufacturing came at a big cost advantage of about less than 40% of the SLM manufacturing cost. The rest of this section discusses the physical evaluation of the DMLS 3D Printed antenna array. Figure 6.4 shows the model and printed antenna.



(a) **(b)**

Figure 6.4: (a) Antenna model with defined dimensions. (b) 3D Printed antenna array.

On first inspection, the surface roughness of the DMLS printed antenna is visibly worse than that of the SLM model discussed in Section 3.3. This is most likely a result of the larger layer thickness employed by the printing process. The smaller dimensions such as the slot line and radial cavity are evaluated by fitting a prototype PCB feed on the side of the antenna. This revealed a defect in the antenna manufacturing: there is a progressive alignment error between the slot-line of the DMLS printed antenna array and the PCB printed slot-line of the feed. This indicated that the entire antenna is possibly a factor smaller than the designed values. Table 6.1 summarises the measured dimensions of the 3D printed antenna.

The element width was determined by taking the average width of several elements. The small change in element width should have minimal influence on the antenna design. The difference in length of an array consisting of eight 12 mm elements and an array

Table 6.1: Measured dimensions of 3D-printed antenna.

Dimension	Nominal Value (mm)	Measured Value (mm)
Array width W_{Array}	96	95.58
Array length L_{Array}	107.3	106.82
Element Width W_a	12	11.942

consisting of eight 11.942 mm elements is 0.464 mm. Therefore with a slot width of only 0.7 mm, this difference can severely degrade antenna performance. To compensate for this defect, the PCB was adjusted to match the 3D printed dimensions.

6.2.2 Feed board

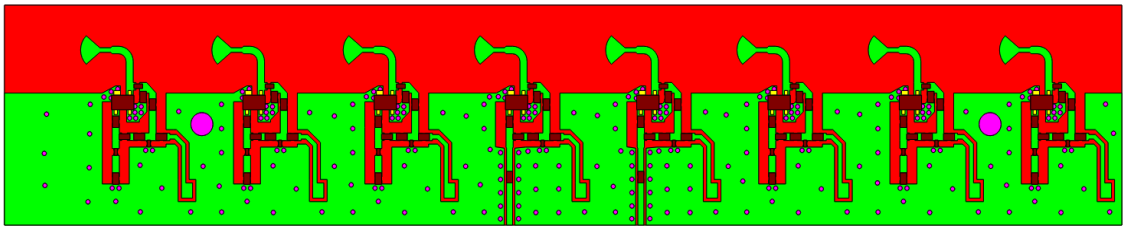
The previous section discussed the 3D printed part of the antenna array. This section discusses the assembly of the feed board. Each feed board consist of eight LNAs as designed in Chapter 4. Only the four centre elements of the 64 element array are fitted with a connector, as a result, two different PCB's are designed for the feed board. The one feed board referred to as the active feed board, contain two active elements, whereas the second feed board only consist of 50Ω terminated elements. Passive feed board will be used to describe the second feed board. Figures 6.5a and 6.5b shows the two different layouts.

All the terminated LNAs have a 50 Ω surface mount resistor on the output. This option is less expensive and simpler to manufacture than fitting a connector to the element and add an SMA load. The AVX 1.2pF capacitor characterised in Section 4.4.2 is implemented as a DC block on the output of the two elements added with a connector in the centre of the active feed board. For the 50Ω terminated elements the same ATC capacitor used for the RF short is implemented as a DC block before the 50Ω resistor. Finally, a coplanar waveguide transmission line is added at the output of the active elements' LNA in Figure 6.5a that extends to the edge of the PCB where the connectors are soldered. The bottom-layers of the feed boards consist of a ground plane for the top-layer and are in electrical contact with the aluminium array. For further cost reduction, all assembly of the feed board components was performed in-house. Figure 6.5c shows a manufactured feed board consisting of only 50Ω terminated elements.

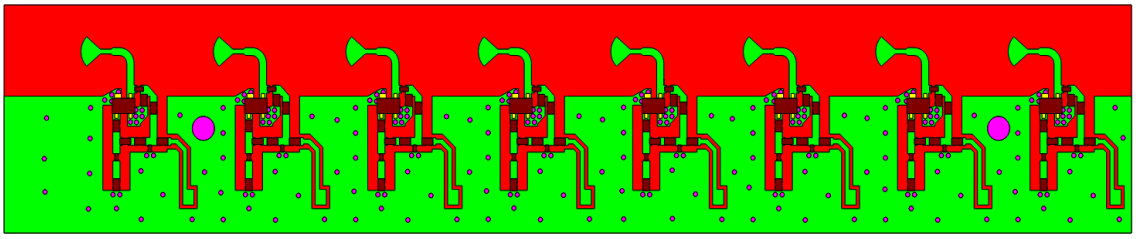
6.2.3 General assembly and the final array

Sections 6.2.1 and 6.2.2 discussed the 3D printed antenna and the feed board with the LNAs, respectively. This section discusses the general assembly of the complete array. Figure 6.6b shows the extended dielectric Cinch connectors that mount to the bottom of the antenna ground plane and feed the coplanar waveguide through a hole in the ground plane. The feed boards discussed in Section 6.2.2 screw to the side of the aluminium antenna. Figure 6.6a shows the assembled array. Note that the screw- and connector holes are printed as part of the 3D printed model, again showing the advantage of additive manufacturing.

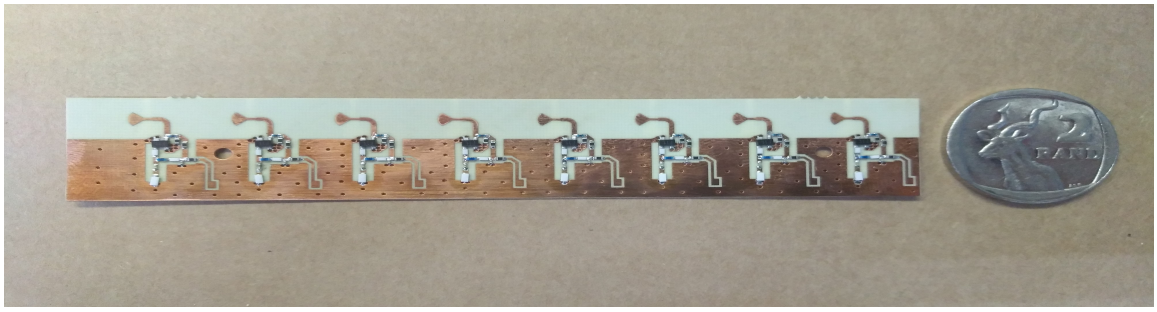
Finally Figure 6.7 shows the manufactured antenna array. This section discussed the assembly of the final array antenna. The next Chapter presents the measurement results of the manufactured antenna.



(a)

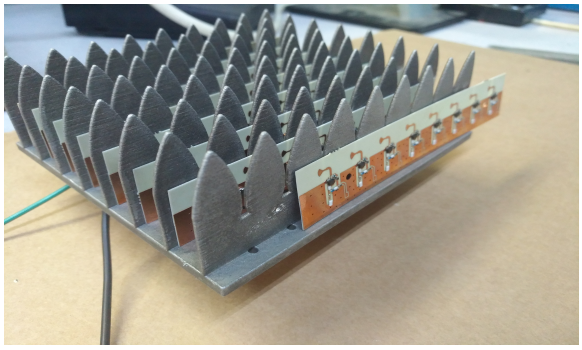


(b)

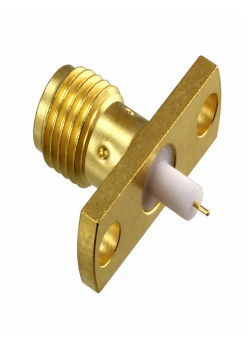


(c)

Figure 6.5: (a) Active feed board. (b) Passive feed board. (c) Manufactured passive feed board.



(a)



(b)

Figure 6.6: (a) Antenna array during assembly. (b) Cinch connector used in array.

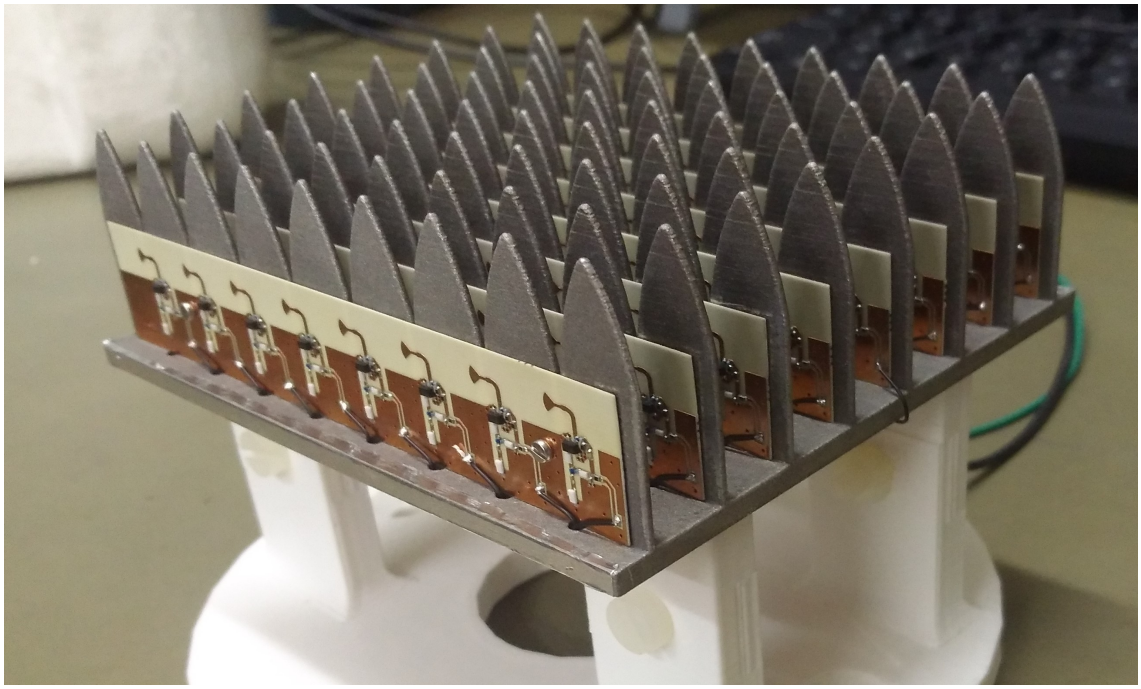


Figure 6.7: Manufactured antenna array.

Chapter 7

Results

Chapters 3-6 discussed the design and development of the active antenna array. This section presents the measured results of the active antenna array. Figure 7.1 shows the manufactured antenna set up in the anechoic chamber.

(a) **(b)**

Figure 7.1: Manufactured antenna in the anechoic chamber (a) top view and (b) bottom view.

The first measurement performed is a stability test. The array was designed for a 50Ω system and is therefore only tested with the spectrum analyser connected at the output of the active elements. The array was analysed for all frequencies up to 25 GHz with no indication of instability.

7.1 Principle plane scans

The next set of measurements follows the same measurement setup as established with the full dielectric linear array in Section 6.1. It was seen in Section 6.1 that the principle plane scans provide the most information and therefore, the first measurements performed. The array consists of four active elements. The array is set up as the receiver. The normalised measured power of all four elements at frequencies 7.8, 10 and 12.8 GHz are presented here.

7.1.1 7.8 GHz

This section presents the results of the E- and H-plane scans performed on the active antenna array at 7.8 GHz.

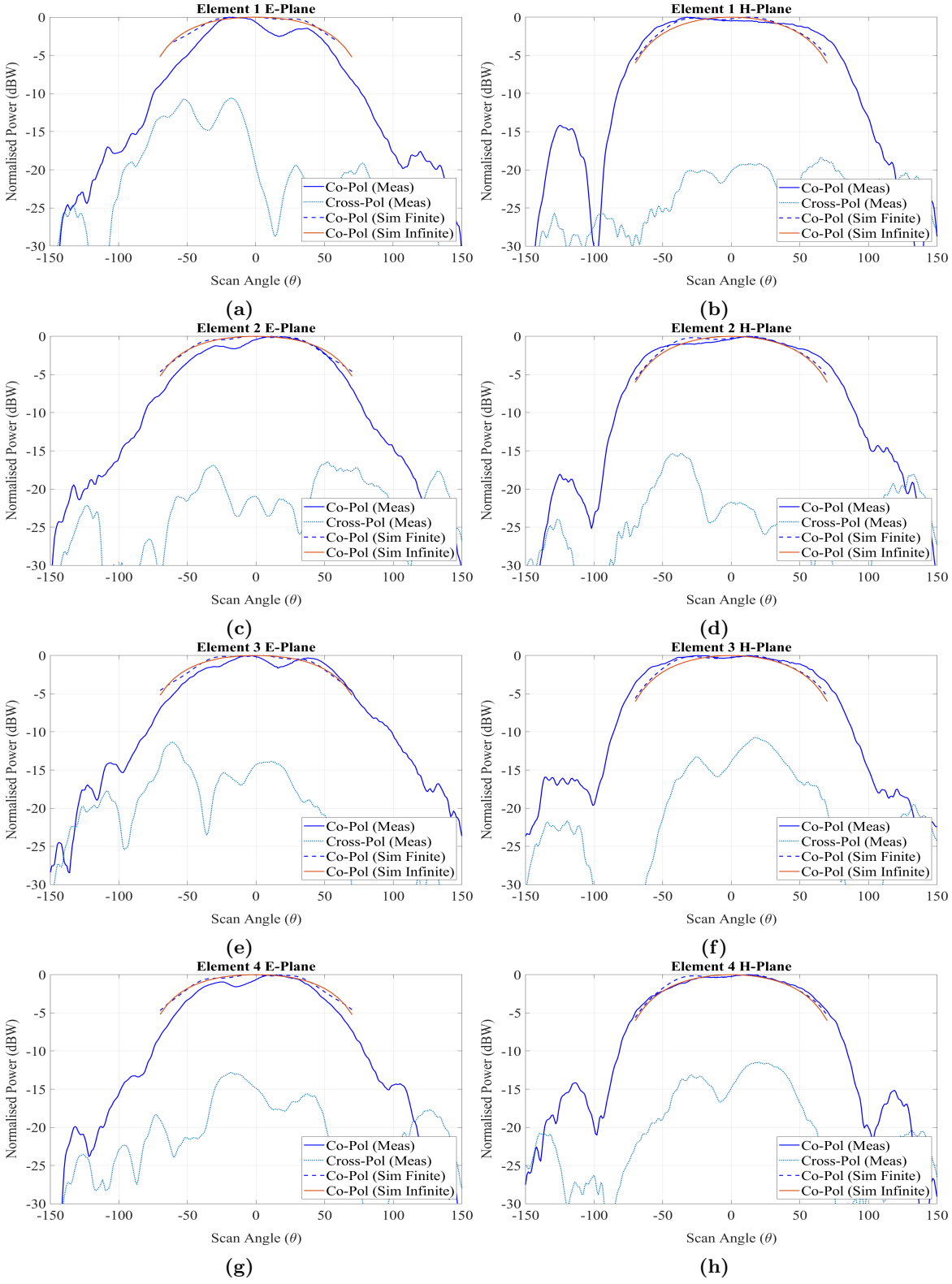


Figure 7.2: E- and H-plane scans at 7.8 GHz.

7.1.2 10 GHz

This section presents the results of the E- and H-plane scans performed on the active antenna array at 10 GHz.

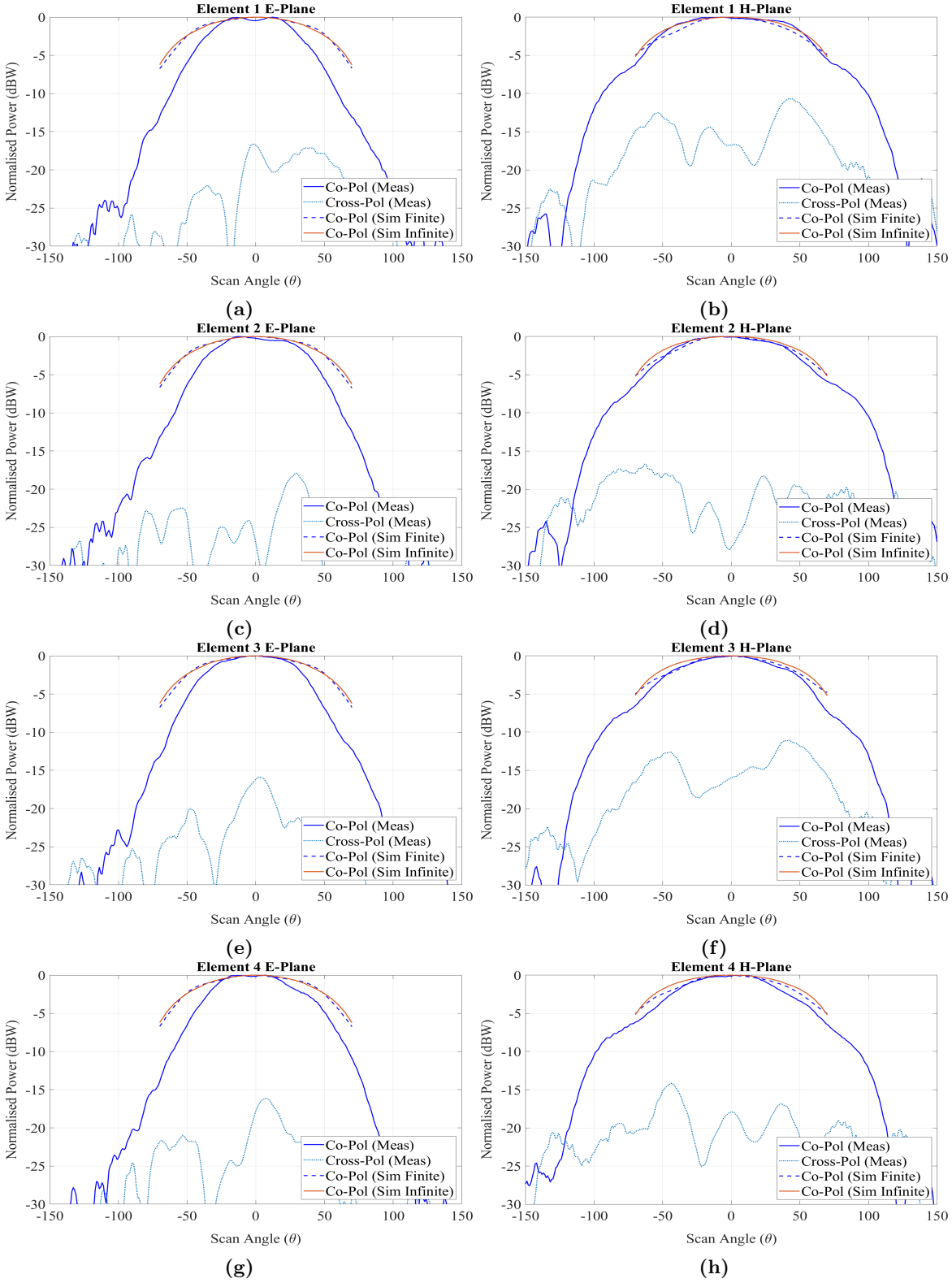


Figure 7.3: E- and H-plane scans at 10 GHz.

7.1.3 12.8 GHz

This section presents the results of the E- and H-plane scans performed on the active antenna array at 12.8 GHz.

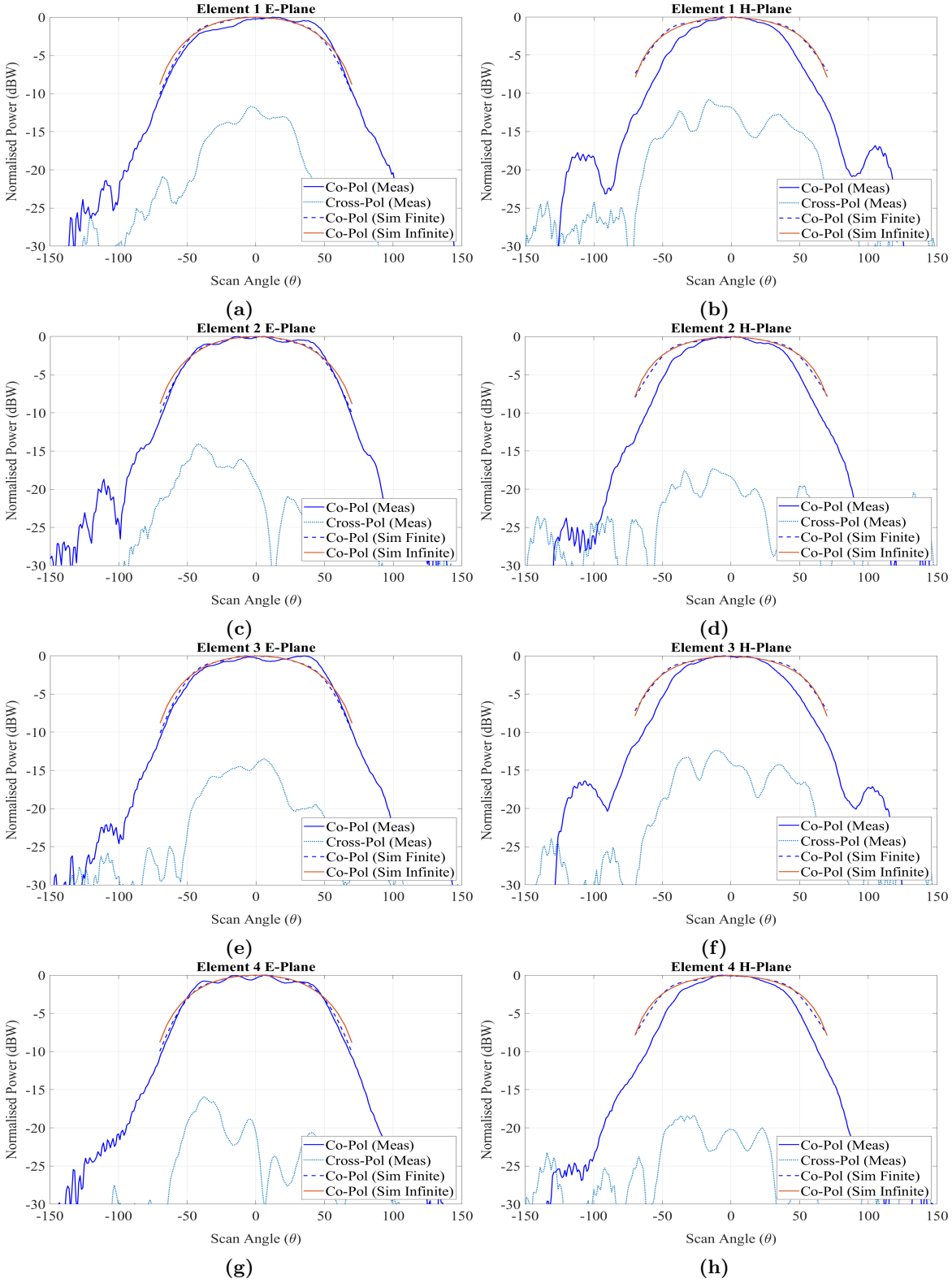


Figure 7.4: E- and H-plane scans at 12.8 GHz.

7.1.4 Conclusion

In general, the measurements show a satisfactory comparison to the simulations for an initial prototype. However, it can be seen that much improvement is still needed to characterise these integrated systems accurately. A starting point can be to simulate and compare it in a different EM simulator. The large amount of focus on the scan area between $\theta = -45°$ and $\theta = 45°$ also caused an analysis of the sidelobes to be neglected. An analysis that can also aid in understanding the asymmetries caused by the feed. A cause for concern, however, is the high levels of cross-polarisation. High levels of cross-polarization are not completely uncommon for Vivaldi arrays. In applications where the system is sensitive to cross-polarisation, this is something that needs to be considered.

7.2 Absolute gain

The second measurement performed is the absolute gain at the broadside of element four using the three-antenna method introduced in Section 2.10. This measurement can be used to determine the gain at all the elements by using the received power measured in principle planes scans. Figure 7.5a shows the broadside gain of element 4 and one of the reference antennas.

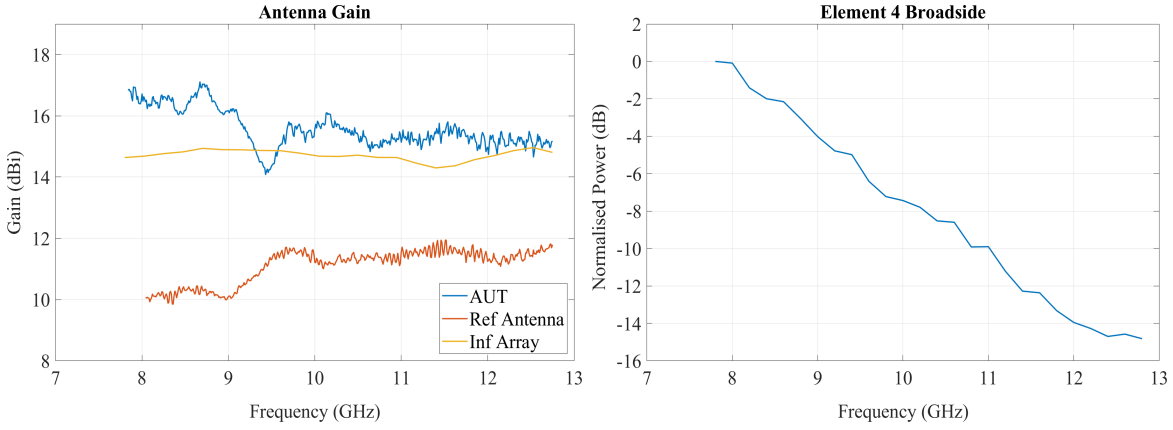


Figure 7.5: (a) Gain of element 4 at broadside (b) Normalised received power at broadside

Fairly accurate results have been measured at frequencies higher than 9.7 GHz with a minimum achieved gain of 14.7 dBi. Gain ripple is also within 0.5 dB. However, at 9.4 GHz, an anomaly occurs where the gain drops about 1.5 dB. For further analysis of this error, the results gathered from the E-plane scans using a different reference antenna was analysed. Figure 7.5b shows the normalised received power for element 4 at broadside. Here cable losses and path losses are included, but the important observation is that there is no anomaly present a 9.4 GHz. Even though this anomaly should be further analysed with more measurements, a possible cause is an error during the specific measurement.

Currently, a system similar to THACO [53] for the noise characterisation of antenna arrays is under development, and therefore a full noise characterisation will be left for future work.

This chapter presented the measured results of the antenna array. The next chapter concludes the thesis.

Chapter 8

Conclusions and Recommendations

This thesis presented the design and manufacturing of an active antenna array for X-band and lower Ku-band frequencies (7.25-12.75 GHz). Main objectives included evaluating 3D printing as a manufacturing technique for antennas, direct integration of the antenna and LNA without the use of a matching circuit and lastly to build an array that can be measured and analysed to improve the simulation and development of future active arrays.

A systematic approach was followed in the design of the active array, starting with the LNA design in Chapter 4. At high frequencies, lumped components are not ideal, and this project showed that confirming the operation of these components is a necessity. The Thru-Reflect-Line de-embedding scheme was used for this purpose. Despite the often inaccurate in-house manufacturing, fairly good success was achieved with de-embedding. However, improvement of the de-embedding to a point where de-embedded components can successfully be used in the simulations is an essential part of future work. The integration of the antenna and LNA combines what was formerly two separate systems that could be characterised independently. Accurate de-embedding of the separate components combined in one system will give the designer the confidence that the component operates as intended. Two LNA designs are presented. The initial LNA focussed on stability. The final version implemented the same stability circuit but focussed on improving power consumption and DC bias stability. The final LNA design compared well with simulations. A good comparison is essential because when the LNA is integrated with the antenna element, it is more difficult to determine whether it is an antenna problem or LNA problem.

Chapter 3 and 5 used the advantage of an infinite array simulation to design the antenna element to closely match the optimum noise impedance of the LNA for minimum noise figure. Chapter 3 presented the first SLM 3D printed model and proved that dimensionally this technology is fully capable of being used for antenna manufacturing. The noise figure analysis of the LNA loaded with the active impedance of the array was aided by the use of a noiseless two-port to represent the EM results of the antenna in Keysight ADS. A noise figure of 1.3 dB was achieved for scan angles up to 45°. Finite array analysis proved to be a trade-off between performance and cost. A larger array be a better approximation to that of the infinite array, providing better performance, but in order to remain within budget, a compromise between performance and price had to be made. Despite accepting the skewed radiation patterns, an array size of 8×8 showed good impedance compared to the infinite array environment at all four central elements.

During the project, two prototypes were developed, a six-element linear full-dielectric Vivaldi array and the final 64 element array. Even though the main focus was the 64

element array, the small array proved to be useful and cost-effective to establish the measurement setup for the final array as well as serve as initial proof that the transistor is stable in the antenna array environment. The 64 element array was manufactured using DMLS additive manufacturing. Apart from the small defect of smaller dimensions discussed in Chapter 6 the antenna manufacturing proved successful. The thesis is still inconclusive regarding surface roughness of the printed antenna. The construction of the array, however, provide an excellent experimental platform for future work. The feed boards can be attached to either an SLM 3D printed antenna or other conventionally manufactured antennas to analyse aspects such as dimensions and surface roughness effects on antenna performance.

The measured results in Chapter 7 showed a satisfactory comparison to the simulations for an initial prototype. An embedded element gain of more than 14.7 dBi was measured over the bandwidth at broadside. High cross-polarization measured is a cause for concern and should be assessed in future projects. Another important piece of future work is a full noise characterisation of the antenna array to compare to simulated results in this project.

In conclusion, the project provides an active antenna array that can be measured for practical confirmation of simulations. Most importantly, the developed array serves as a performance reference that can be improved in the future development of active arrays.

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