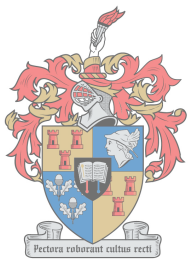
A Digital Low-Level Radio Frequency Control System for the Particle Accelerators at iThemba LABS

by

William Duckitt



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Supervisor: Prof. T. R. Niesler
Co-supervisor: Dr. J. L. Conradie

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Declaration

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Date: March 2018

Abstract

A Digital Low-Level Radio Frequency Control System for the Particle Accelerators at iThemba LABS

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Dissertation: PhD (Electronic Engineering)

March 2018

This dissertation presents the design, implementation and evaluation of a digital low-level radio frequency (RF) control system for the cyclotron particle accelerators at iThemba LABS. This system replaces a 30-year old analog control system. The new system makes extensive use of state-of-the-art field programmable gate arrays (FPGA), high-speed digital to analog converters (DAC) and high-speed analog to digital converters (ADC).

The presented system incorporates a modified direct digital synthesis (DDS) technique to directly convert the digital RF signals to analog RF and local-oscillator (LO) signals with 16-bit amplitude accuracy, programmable in steps of 1 µHz and 0.0001°. Down-conversion of the RF pick-up signals to an optimal intermediate frequency (IF) of 1 MHz and sampling of the IF channels by 16-bit, single sample-latency 10 MHz ADCs were implemented to allow digital high-speed low-latency in-phase/quadrature (I/Q) demodulation of the IF channels within the FPGA. This in turn allows efficient real-time digital closed-loop control of the amplitude and phase of the RF drive-signal to be achieved.

The systems have been successfully integrated at iThemba LABS into the K=8 and K=10 injector cyclotrons (SPC1, and SPC2), the K=200 separated sector cyclotron (SSC), the SSC flat-topping system, the pulse-selector system and the AX, J, and K-line RF bunchers. The system has also been successfully integrated into the K=132 separated sector cyclotron at the Helmholtz-Zentrum Berlin (HZB).

The described system achieves the target peak-peak amplitude and phase stabilities of 0.01% and 0.01° respectively and operates over the wide frequency range of 2-100 MHz. The system has led to a substantial improvement in the beam quality of the SSC at iThemba LABS. Prior to the integration of the presented system, it was difficult to achieve extraction current losses lower than 700-800 nA on the SPM1 and SPM2 magnetic extraction elements of the SSC for high-intensity 66

MeV proton beams with 220 µA on target. Once the presented system had been incorporated, the lowest losses achieved on both extraction elements were 13.1 nA for SPM1 and 18 nA for SPM2 with 227 µA on target. The reduction in losses by more than 90% results in less activation of the extraction components. This significantly reduces the radiation dose that personnel who have to service these components would be exposed to during servicing and emergency repair.

The new system has demonstrated greatly improved performance in terms of amplitude and phase stability as well as efficiency. This places the RF control systems at iThemba LABS at the forefront of the state-of-the-art. It also extends the lifetime of this facility, and paves the way for future experimentation into the production of isotopes at higher current intensities, as well as the continued delivery of high precision particle beams for physics research and medical therapy.

Uittreksel

'n Digitale Laevlak Radiofrekwensie Beheerstelsel vir die Deeltjiesversnellers by iThemba LABS

("A Digital Low-Level Radio Frequency Control System for the Particle Accelerators at iThemba LABS")

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Hierdie proefskrif bied die ontwerp, implementering en evaluering van 'n digitale laevlak radiofrekwensie (RF) beheerstelsel vir die siklotron tipe deeltjiesversnellers by iThemba LABS. Hierdie stelsel vervang 'n 30 jaar oue analoog beheerstelsel. Die nuwe stelsel maak intensief gebruik van die nuutste veldprogrammeerbare hekstruktuur (FPGA), hoëspoed syfer-analoogomsetters (SAO) en hoëspoed analoog-syferomsetters (ASO).

Die voorgestelde stelsel bevat 'n gewysigde direkte digitale sintese (DDS) tegniek om die digitale RF seine direk na analoog RF en lokale ossillator seine om te skakel met 16-bis amplitude akkuraatheid, programmeerbaar in stappe van 1 µHz en 0.0001°. Afmenging van die RF terugvoer seine na 'n optimale tussenfrekwensie van 1 MHz en die meting van die tussenfrekwensie-kanale deur 16-bis, 10 MHz SAO's met enkelmonster-vertraging, is geïmplementeer. Hoë spoed lae vertraging in-fase/kwadratuur (I/Q) demodulasie van die tussenfrekwensie-kanale word deur die FPGA uitgevoer. Die tegnieke maak dit moontlik om effektiewe intydse digitale geslote lus beheer van die amplitude en fase van die RF-dryfsein uit te voer.

Die stelsels is suksesvol by iThemba LABS geïntegreer in die K=8 en K=10 injektor siklotrone (SPC1 en SPC2), die K=200 oopsektor siklotron (OSS), die OSS-platkruin stelsel, die puls-selektor stelsel en die AX-, J- en K-lyn RF verdigters. Die stelsel is ook suksesvol geïntegreer in die K=132 oopsektor siklotron by die Helmholtz-Zentrum Berlyn (HZB).

Die voorgestelde stelsel bereik die teiken piek tot piek amplitude en fase stabiliteit van onderskeidelik 0.01% en 0.01° en kan bedryf word oor 'n wye frekwensie-bereik van 2 tot 100 MHz. Die implementering van die stelsels het bygedra tot 'n aansienlike verbetering in die bundel kwaliteit van die OSS by iThemba LABS. Voor

die integrasie van die voorgestelde stelsel, was dit moeilik om ekstraksie stroomverliese laer as 700-800 nA op die SPM1- en SPM2-magnetiese ekstraksie-elemente van die OSS vir 'n hoëintensiteit 66 MeV protonbundel met 220 µA op die teiken te bereik. Na die integrasie van die voorgestelde stelsel was bundelverliese van so laag as 13.1 nA vir SPM1 en 18 nA vir SPM2 met 227 µA op die teiken gemeet. Die meer as 90% afname in bundelverliese impliseer minder aktivering van die ekstraksie komponente en gevolglik laer vlakke van bestraling waaraan personeel blootgestel word tydens onderhoud en noodherstelwerk daarvan.

Die nuwe stelsel het reeds 'n groot verbetering in terme van amplitude en fase stabiliteit en gevolglike doeltreffendheid gedemonstreer. Dit plaas die RF beheerstelsels by iThemba LABS aan die voorpunt van die nuutse tegnologie. Met die stelsels word die leeftyd en volhoubaarheid van kwaliteit hoë intensiteit bundelvoorsiening deur die fasiliteit verleng. Dit baan ook die weg vir toekomstige navorsing in die verhoging van die maksimum bundelintensiteite vir die produksie van radioisotope asook die voortgesette lewering van bundels met hoë bundelkwaliteit vir kernfisika navorsing en mediese behandeling.

Publications

The work in this thesis has been presented at and appears as a full-length conference paper in the proceedings of the 21st International Conference on Cyclotrons and their Applications, held in Zurich, Switzerland in September 2016. This is a prestigious international event in the field.

- W.D. Duckitt , J.K. Abraham, J.L. Conradie, T.R. Niesler, M.J. Van Niekerk. A New Digital Low-level RF Control System for Cyclotrons. In21st Int. Conf. on Cyclotrons and Their Applications (Cyclotrons' 16), Zurich, Switzerland, September 11-16 2016, 2017 Jan 1 (pp. 258-262). JACOW, Geneva, Switzerland.

Furthermore, the work in this thesis is the subject of a paper that is in the process of being submitted to the Journal of Nuclear Instruments and Methods in Physics Research A, which is a respected peer-reviewed and accredited journal in the field.

- W.D. Duckitt , J.K. Abraham, J.L. Conradie, T.R. Niesler, M.J. Van Niekerk. The Design and Implementation of a Broadband Digital Low-level RF Control System for the Cyclotron Accelerators at iThemba LABS, Submitted to: Nuclear Instruments and Methods in Physics Research A, November 2017

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I would like to thank my friends and colleagues who have assisted me in the completion of this thesis: Mr M.J. Van Niekerk for all the insight into RF systems at iThemba LABS and for the help with mechanical design of the system. Mr L. Heinkelein for all his insight into RF systems and for all the help proof reading this thesis. H. Du Plessis for the photographs of the designs. J. Abraham for all the assistance with the installation and upgrading of the motion control systems. C. Baartman, P. Davids, J.K. Solomons, P. Jones, P. Sheodass, D. April for all the assistance with manufacturing, assembly and installation of the systems.

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Finally, I would like to thank my parents and my wife for their continued support and encouragement over the years.

Dedications

To my wife Jessica

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Nomenclature

Symbols

B	magnetic field strength
q	electric charge of a charged particle
m	relativistic mass of a charged particle
m_0	particle rest mass
β	relative velocity
γ	Lorentz factor
v	velocity
c	speed of light
λ	wave length
w	angular frequency in radians per second
K	proton kinetic energy in MeV

Units

Hz	Hertz
kHz	kilo Hertz
MHz	mega Hertz
V	volt
W	Watt
kW	kilo Watt
MeV	mega electron volt
fs	femtoseconds
dB	decibel
dBc	decibels relative to the carrier

Abreviations

AC	alternating current
ADC	analog to digital converter
ATU	auto-tune
BGA	ball grid array
BM1	bending magnet 1

BM2 bending magnet 2
BOM bill of materials
CA channel access
CORDIC coordinate rotational digital computer
CPU central processing unit
CSS control system studio
DAC digital to analog converter
DC direct current
DDS direct digital synthesis
DLLRF digital low-level radio frequency
DSP digital signal processing
EPICS experimental physics and industrial control system
FIFO first-in first-out
FIR finite impulse response
FPGA field programmable gate array
FTW frequency tuning word
GUI graphical user interface
HZB Helmholtz-Zentrum Berlin
I/O input/output
I/Q in-phase and quadrature
IF intermediate frequency
IOC input output controller
JTAG Joint Test Action Group
LED light emitting diode
LLRF low-level radio frequency
LO local oscillator
LPF low-pass filter
LUT look-up table
PA power amplifier
PCB printed circuit board
PC personal computer
PID proportional integral differential
PIG Penning Ion Gauge
PLL phase-locked loop
RAM random access memory
RF radio frequency
RLC resistance-inductance-capacitance
RMS root mean square

SAR successive approximation register
SFDR spurious free dynamic range
SMA sub-miniature type A
SNR signal to noise ratio
SPC1 solid pole injector cyclotron 1
SPC2 solid pole injector cyclotron 2
SPI serial peripheral interface
SPM1 septum magnet 1
SPM2 septum magnet 2
SSC separated sector cyclotron
TDM time division multiplexing
USB universal serial bus
VCO voltage controlled oscillator
VHDL verilog hardware description language

Chapter 1

Introduction

iThemba Laboratory for Accelerator Based Sciences (iThemba LABS) is a multi-disciplinary accelerator research facility situated in Cape Town, South Africa. At the heart of the facility is the K=200 separate sector cyclotron (SSC), that delivers particle beams for nuclear physics, nuclear chemistry, neutron therapy, proton therapy, radiobiology and isotope production with the following requirements:

- Nuclear physics: Proton beams in the energy range 20 to 200 MeV with beam intensities of up to 10 µA and heavy ions with beam intensities between 1 to 10 µA.
- Nuclear chemistry: Proton beams in the energy range 20 to 200 MeV with beam intensities of up to 10 µA.
- Neutron therapy: 66 MeV protons with beam intensities of up to 40 µA.
- Proton therapy: A 200 MeV proton beam with an intensity of up to 1 µA.
- Radiobiology: Proton beams with a maximum intensity of 1 µA and energies of up to 200 MeV.
- Isotope production: 66 MeV proton beams with a beam intensity of up to 300 µA.

To meet these challenging demands two injector cyclotrons are used as pre-accelerators for the SSC. The first, a K=8 solid pole cyclotron (SPC1) with an internal Penning Ion Gauge (PIG) ion source that produces proton beams with high intensity and the second, a K=10 solid pole cyclotron (SPC2) that accelerates light and heavy ions from external ion sources.

Over the years, significant effort has been made to achieve higher stability and intensity from the systems, with improvements being made to the PIG ion source, SPC1, the buncher systems (Conradie, 1992) and the addition of a flat-topping system to the SSC (De Villiers, 2009).

Fundamental to the operation of the cyclotron systems are the radio frequency (RF) control systems that are responsible for controlling and stabilizing the amplitude and phase of the RF voltages that are used to accelerate the particles. In

total there are 13 RF systems at iThemba LABS that operate at varying frequencies between 2 and 81 MHz and at power levels from 5 W for a buncher system and up to 100 kW for each of the resonators of the SSC.

A critical drive has been to replace these 30 year old legacy analog RF control systems with modern technology. To this effect a new generic digital low-level RF control system has been designed. The design and evaluation of this new system is the topic of this thesis.

1.1 Problem Statement

iThemba LABS requires the development of new RF amplitude and phase control systems to achieve a greater system stability and reliability, which is required for delivering the high intensity beams needed for radioisotope production as well as beams with improved qualities for nuclear physics and medical radiation.

1.2 Research Objectives

The objectives of the research described in this thesis are as follows.

- Develop a modern state-of-the-art digital RF control system utilizing state-of-the-art field programmable gate arrays (FPGA), high-speed digital to analog converters (DAC), high-speed analog to digital converters (ADC) and modern digital signal processing (DSP) technology.
- Improve on the performance of the existing analog control system and achieve a peak-peak amplitude stability of 0.01% and a peak-peak phase stability of 0.01°.
- Design a system that is generically implementable across a range of cyclotron and RF systems that operate between 2 and 81 MHz.
- Improve and optimize the techniques used in current systems in similar facilities so that the desired stability can be achieved.
- Improve on the operational functionality of the cyclotron RF control system and automate the system operation to allow it to recover automatically without intervention from external interlocks and high voltage breakdown within the resonators.

1.3 Research Questions

Based on the stated objectives, the following research questions can be defined.

- Is it possible to improve on the current analog control system using a digital RF control system approach?

- Is it possible to design the system to be generically implementable across the wide frequency range of RF systems at iThemba LABS?
- Will it be possible to improve the operational functionality and the ability to automatically recover from external interlocks and high voltage breakdown within the RF resonators?
- Will it be possible to improve the quality of the beams produced by the cyclotron facility?
- Can the system be implemented on similar accelerators at other facilities around the world?

1.4 Significance of Research

Success of the project will greatly improve the RF system stability, reliability and monitoring capability at iThemba LABS. This in turn will lead to the ability to produce a higher quality beam for medical applications, physics research and will result in a higher radioisotope production yield. Success of this project will put iThemba LABS at the forefront of international developments in the field.

1.5 Outline of Thesis

- Chapter 2 provides a concise introduction to cyclotron particle accelerators, followed by a more detailed description of the facilities at iThemba LABS, giving particular attention to the legacy systems which were replaced. A review of the theoretical description of the effects of dee voltage stability on cyclotron performance is presented, as well as an overview of the current literature regarding digital control of cyclotron RF systems
- Chapter 3 describes in detail the design of the new digital low-level RF (DLLRF) control system and the implementation of the RF control systems at iThemba LABS and at the Helmholtz-Zentrum Berlin (HZB) are discussed.
- In Chapter 4 the operational history and performance of the new RF control system is discussed.
- Finally, conclusions derived from the research presented in this thesis are given in Chapter 5.

Chapter 2

Literature Review

This chapter will provide a concise introduction to cyclotron particle accelerators, followed by a more detailed description of the facilities at iThemba LABS, giving particular attention to the legacy systems which were replaced. A review of the theoretical description of the effects of RF dee voltage stability on cyclotron performance is presented, as well as an overview of the current literature regarding digital control of cyclotron RF systems.

2.1 The Cyclotron Particle Accelerator

A cyclotron is part of the circular family of particle accelerators that recirculate a beam through the accelerating voltage many times (Conte and MacKay, 2008). The cyclotron was first conceptualized in the 1930's by E. O. Lawrence (Lawrence and Edlefsen, 1930) and the first practical cyclotron accelerated protons to an energy of 1.2 MeV in 1932 and reached 590 MeV in 1974. The cyclotron has evolved into many forms such as Isochronous Cyclotrons, Separated Sector Cyclotrons, H^- Cyclotrons and Superconducting Cyclotrons (Chao *et al.*, 2013).

A representation of a classical cyclotron is shown in Fig. 2.1. The principle of operation requires that a constant frequency RF voltage that is stable in amplitude and phase be applied across two electrodes known as "dees" that are situated in a static and uniform magnetic field which causes the particle's path to bend in a circle due to the Lorentz force perpendicular to their direction of motion.

Ions are injected or generated at the centre of the cyclotron and the RF voltage accelerates them to produce a beam. As the beam increases in energy, the orbit radius increases and a spiral beam orbit pattern is produced until finally the beam reaches the extraction radius and can be extracted from the cyclotron. In order for the particles to make one orbit per RF cycle the RF frequency must be set to

$$f = \frac{qB}{2\pi m}. \tag{2.1}$$

where B is the magnetic field strength, q is the electric charge of the particle, and m is the relativistic mass of the charged particle. As particles approach the speed

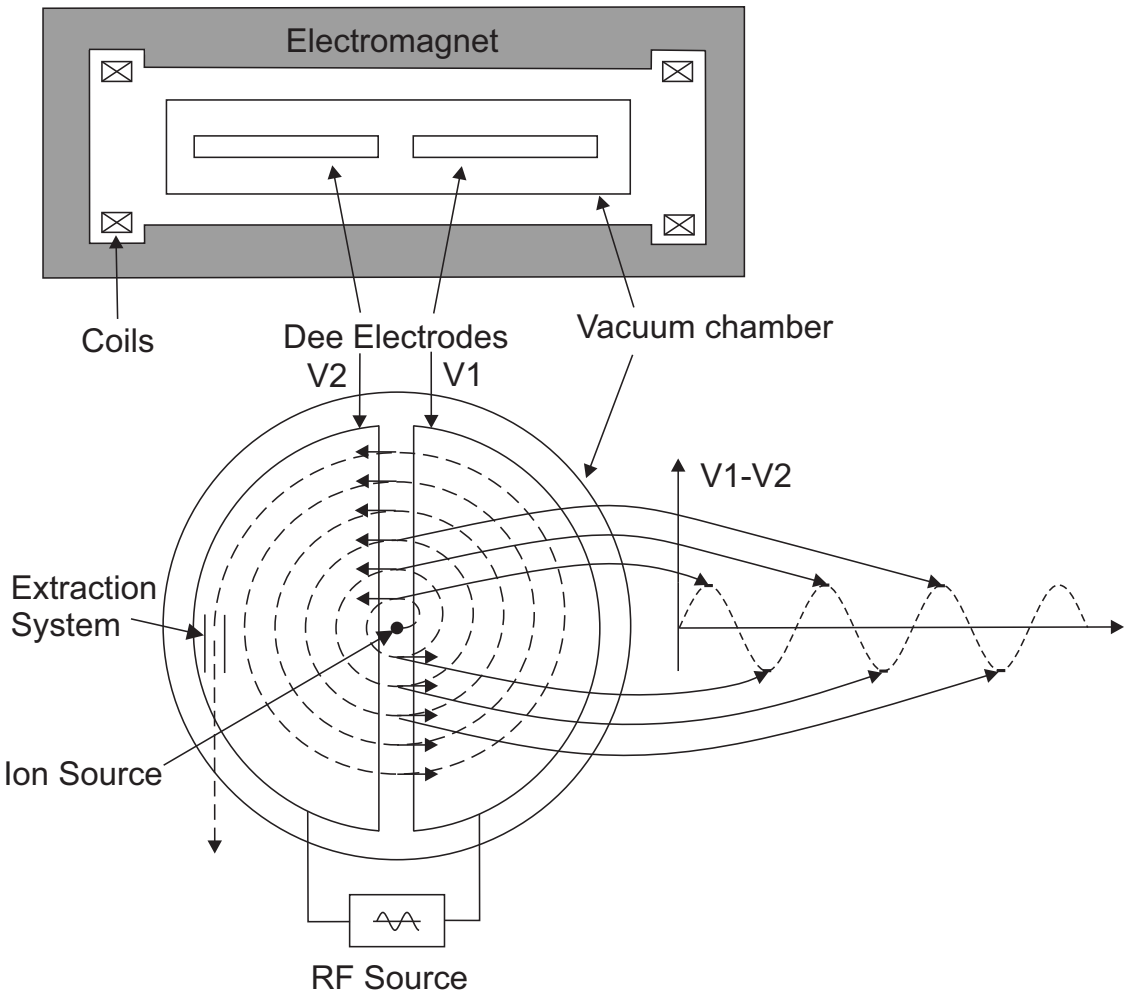

Figure 2.1: Diagrammatic representation of a classical cyclotron.

of light, their relativistic mass increases as defined by

$$m = \frac{m_0}{\sqrt{1 - \left(\frac{v}{c}\right)^2}} = \frac{m_0}{\sqrt{1 - (\beta)^2}} = \gamma m_0 \tag{2.2}$$

where

m_0 is the particle rest mass,
$\beta = \frac{v}{c}$ is the relative velocity, and
$\gamma = \frac{1}{\sqrt{1 - \left(\frac{v}{c}\right)^2}} = \frac{1}{\sqrt{1 - (\beta)^2}}$ is the Lorentz factor.

To compensate for the relativistic mass increase, as in an isochronous cyclotron, the magnetic field can be increased radially. By choosing B proportional to the Lorentz factor $B = \gamma B_0$, it follows that for the relativistic case the cyclotron frequency is defined as

$$f = \frac{qB}{2\pi m_0 \gamma} = \frac{qB_0}{2\pi m_0}. \tag{2.3}$$

There are a number of factors that are critical to the production of a stable beam from a cyclotron. These include ion source stability, vacuum stability, magnetic field stability, RF amplitude and phase stability, mechanical stability and diagnostic ability. Each are equally important. Instability in any one of these factors will be detrimental to the performance and operation of the cyclotron. Individually, poor performance in any of these systems can mask any improvements made in the others.

Fortunately each of these components can to a certain degree be individually optimized in order to improve the performance of the cyclotron.

With this in mind, the focus of this research has been on designing a new digital low-level RF control system to replace the legacy analog control system, thereby improving the RF system's stability, which in turn should improve the beam quality and the operation of the cyclotrons and RF systems at iThemba LABS.

The production version of the designed RF control system has been installed on the K=8 and K=10 injector cyclotrons (SPC1 and SPC2), the K=200 separated sector cyclotron (SSC), as well as the bunching and pulse selector RF systems at iThemba LABS. Furthermore, the system has also been installed on the K=132 separated sector cyclotron at the Helmholtz-Zentrum in Berlin (HZB).

The following sections present a review of the state-of-the-art, an overview of the facilities at iThemba LABS, detailed descriptions of the RF systems, with some emphasis on the legacy components, a description of the facilities at HZB and a discussion on the effects of RF dee voltage on the performance of cyclotrons.

2.2 An Overview of the Cyclotrons and RF Systems at iThemba LABS

iThemba LABS operates 3 cyclotrons and various RF buncher systems. In total there are 13 RF systems that operate at frequencies between 2 and 81 MHz and at power levels between 2 W and 100 kW to deliver particle beams for nuclear physics experiments, radiotherapy and the production of radioisotopes.

Figure 2.2 shows the layout of the facilities at iThemba LABS and the following sections provide an overview of the inter-operation of the ion-sources, injector cyclotrons and buncher RF systems with the SSC at iThemba LABS.

2.2.1 The K=8 MeV Light-Ion Solid-Pole Injector Cyclotron (SPC1)

The first injector cyclotron at iThemba LABS, known as SPC1, is a solid-pole injector cyclotron. A photograph of the system is shown in Fig. 2.3.

The cyclotron magnet has four sectors and the accelerating electrodes consist of two 90° dees. It has an internal hot cathode Penning Ion Gauge (PIG) ion source

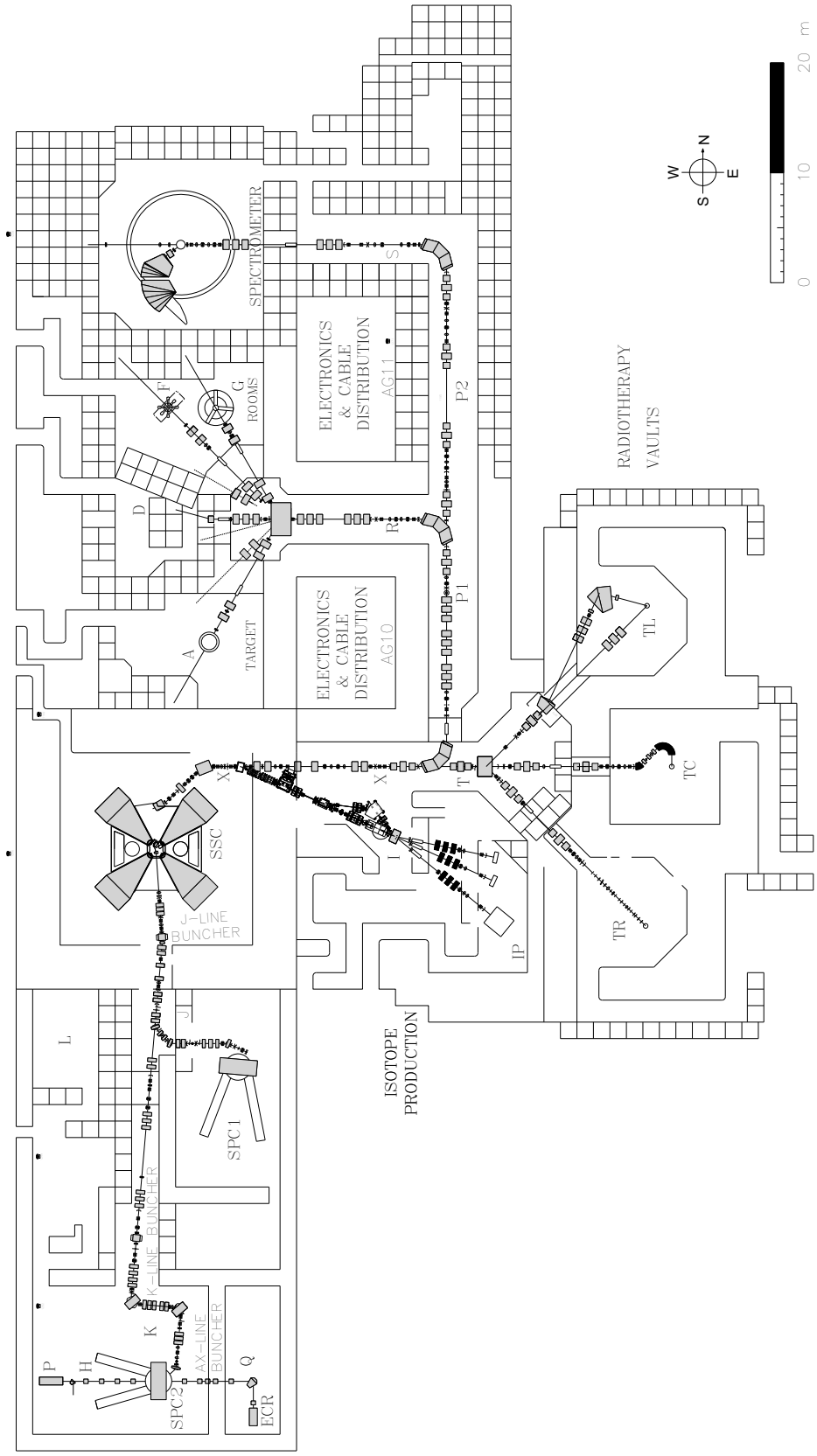

Figure 2.2: The layout of the facilities at iThemba LABS, depicting the injector cyclotrons (SPC1 and SPC2), separated sector cyclotron (SSC), isotope production, radiotherapy and physics experiment facilities.

Figure 2.3: A photograph of SPC1 depicting the east and west resonators, the electromagnet, and the vacuum chamber.

that can be positioned at three constant orbit geometries to produce light ions. A median plane cross section of SPC1 is shown in Fig. 2.4. The diagram indicates the positions of the ion source, the radial differential probes, the magnetic channel and the electrostatic extraction channel. Also shown are the positions of the coupling and trimmer capacitors, the inner and outer conductors as well as the resonator dee that form part of the east resonator RF system.

The west RF resonator system is identical to the east RF resonator system and in the paragraphs below only the east RF system is described using the equivalent circuit diagram shown in Fig. 2.5.

Each system consists of a $\lambda/4$ resonator that can be tuned over 8-26 MHz using movable short-circuit plates. This is represented by the adjustable inductor and capacitor as part of the parallel RLC circuit in the diagram in Fig. 2.5. Fine tuning of the resonant frequency can be performed using the trimmer capacitor. A 25 kW RF amplifier delivers RF power via a 50 Ohm transmission line to the east side dee through a coupling capacitor to produce a maximum dee voltage of 60kV.

The RF control system demodulates the signal of the resonator dee pick-up and compensates for disturbances and errors by correcting the amplitude and phase of the RF drive signal into the 500 W driver. Similarly, compensation for resonant frequency drift due to thermal loading can be performed by demodulating the phase of the auto-tune pick-up and by moving the trimmer capacitor proportionally to the phase change between the auto-tune and the resonator dee pick-up during operation.

SPC1 is primarily used as the injector cyclotron for proton beams to the SSC for isotope production and neutron and proton therapy. The system is typically in operation from Monday to Friday. For isotope production, 3.15 MeV protons with

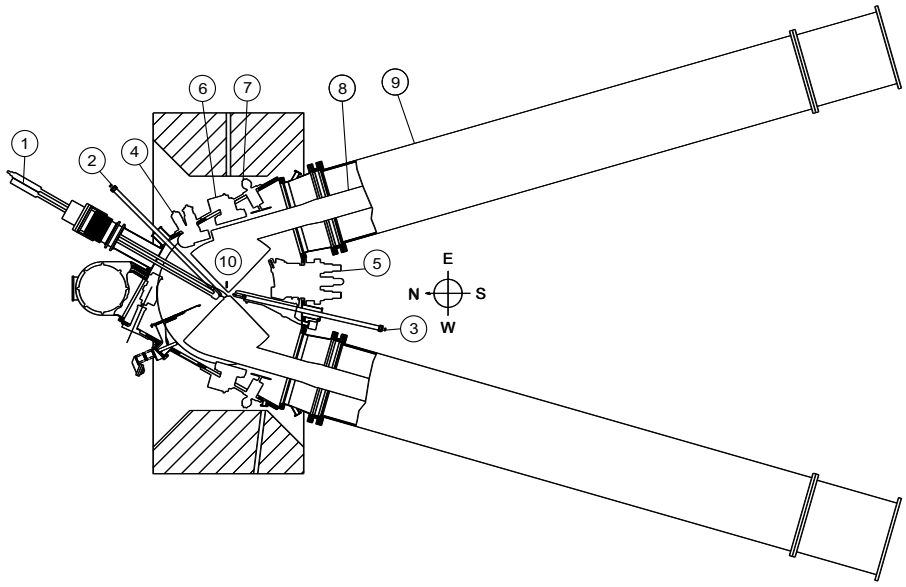

Figure 2.4: A median plane cross section of SPC1 showing (1) the ion source, (2) and (3) the radial differential probes, (4) the magnetic channel, (5) the electrostatic channel, (6) coupling capacitor, (7) trimmer capacitor, (8) inner conductor, (9) outer conductor and (10) the resonator dee.

extraction current intensity of typically 420 µA are produced at an RF frequency of 16.3736 MHz from SPC1. The same beam with a reduced current intensity of up to 40 µA can be used for neutron therapy. In this case, the beam intensity is modulated by adjustable slits in the transfer beam line between SPC1 and the SSC.

For proton therapy, 8 MeV protons with an extraction current intensity of 20-40 µA are produced at an RF frequency of 26 MHz from SPC1 and then cut in the transfer beam line to the required beam intensity of a few nA. Occasionally SPC1 is also used for physics experiments on the weekends.

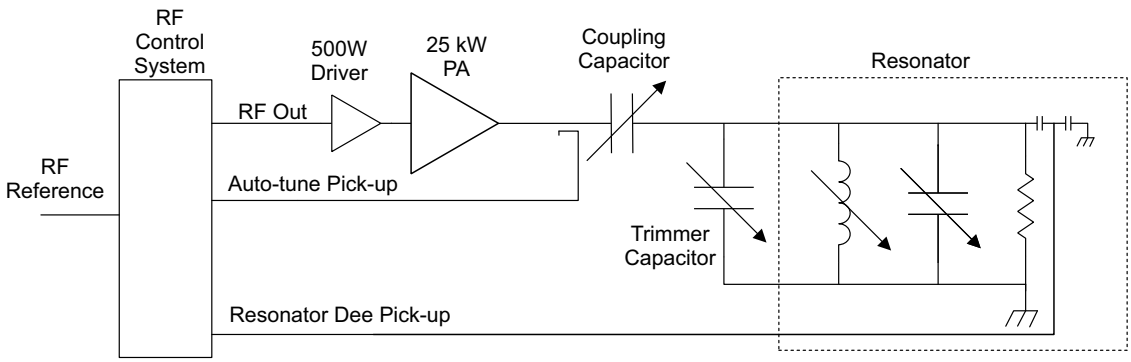

Figure 2.5: An equivalent circuit diagram of the RF system for each of the resonators of SPC1.

2.2.2 The K=10 MeV Solid-Pole Injector Cyclotron (SPC2)

The second injector cyclotron, known as SPC2, is a solid-pole injector cyclotron. A photograph of the system is shown in Fig. 2.6. The system is similar in construction to SPC1 with four-sectors and two 90° dees. However, it does not have an internal ion source. Rather, three interchangeable spiral inflectors allow for the acceleration of polarized hydrogen and heavy ion beams at three constant orbit geometries from 3 external ion sources.

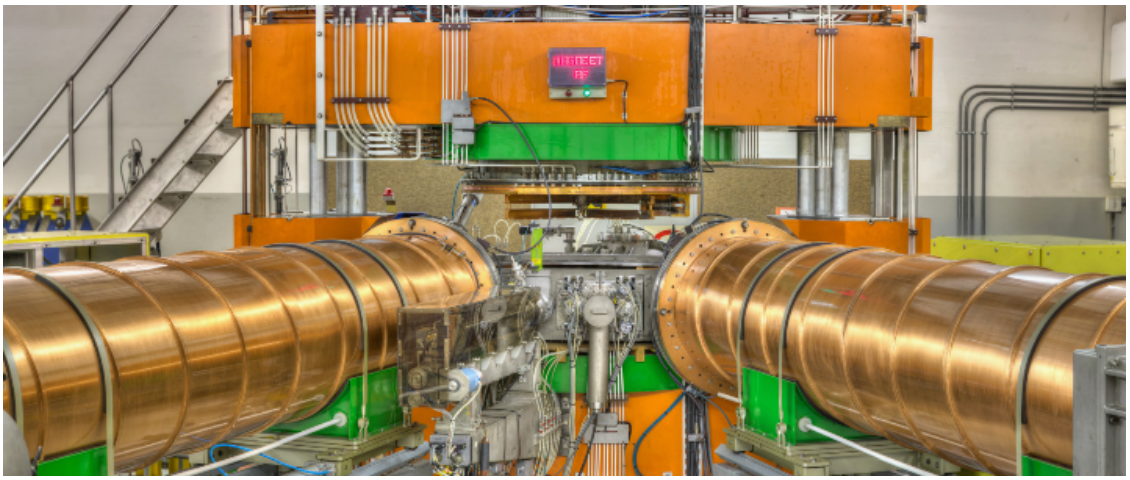

Figure 2.6: A photograph of SPC2 depicting the north and south resonators, the electromagnet, and the vacuum chamber.

A median plane cross section of SPC2 is shown in Fig. 2.7. The diagram indicates the positions of the inflector, the radial differential probes, the magnetic channel and the electrostatic extraction channel. Also shown are the positions of the coupling and trimmer capacitors, the inner and outer conductors as well as the resonator dee that form part of the south resonator RF system.

The south RF resonator system is identical to the north resonator system and in the paragraphs below only the former is described using the equivalent circuit diagram shown in Fig. 2.8

Each system consists of a $\lambda/4$ resonator that can be tuned over 8-27.5 MHz using movable short-circuit plates. This system is identical to the SPC1 resonator as described in Section 2.2.1, apart from the extended frequency range.

As with SPC1, the RF control system demodulates the signal of the resonator dee pick-up and compensates for disturbances and errors by correcting the amplitude and phase of the RF drive signal into the 500 W driver. Frequency drift due to thermal loading can also be compensated by demodulating the phase of the auto-tune pick-up and by moving the trimmer capacitor proportionally to the phase change between the auto-tune and the resonator dee pick-up during operation.

SPC2 is primarily used as the injector cyclotron for heavy ions and polarized protons beams to the SSC for physics experiments. During a typical week at iThemba LABS, development of the beam starts on a Wednesday and must be

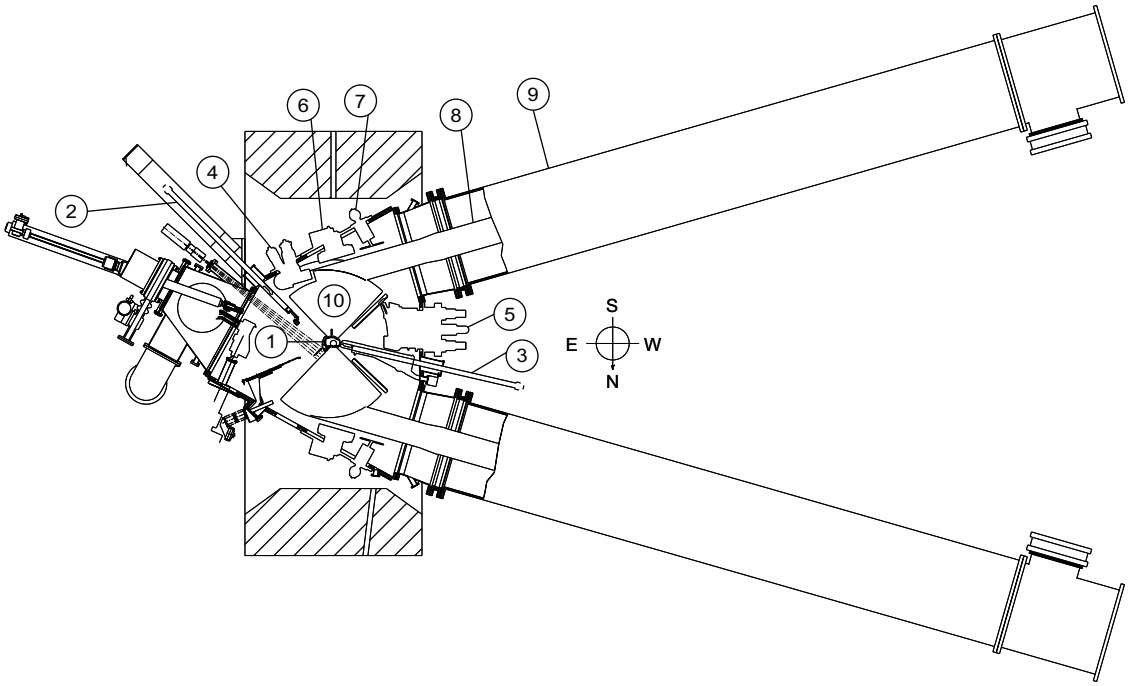

Figure 2.7: A median plane cross section of SPC2 showing (1) the inflector, (2) and (3) the radial differential probes, (4) the magnetic channel, (5) the electrostatic channel, (6) coupling capacitor, (7) trimmer capacitor, (8) inner conductor, (9) outer conductor and (10) the resonator dee.

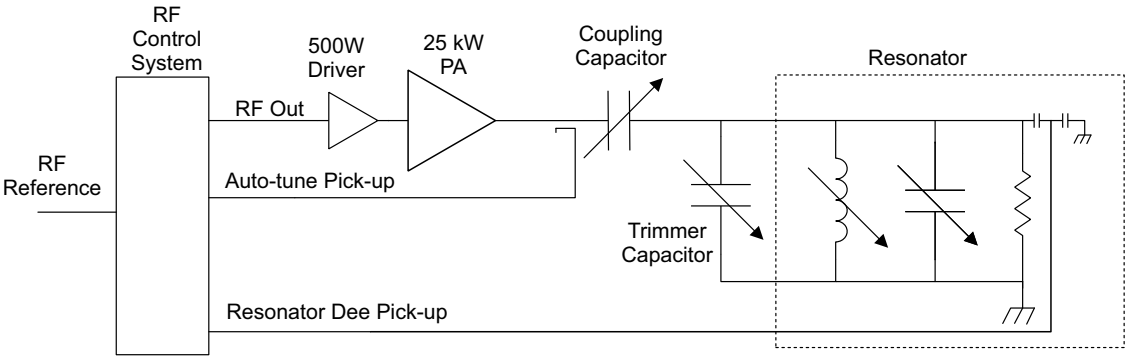

Figure 2.8: An equivalent circuit diagram of the RF system for each of the resonators of SPC2.

operational by Friday. Experiments usually run from Friday until Monday morning when another energy change occurs.

2.2.3 The J,K and AX Line Bunchers

To improve the beam quality and obtain higher extraction efficiency from the SSC there are two 2nd harmonic buncher systems installed between the injector cyclotrons (SPC1 and SPC2) and the SSC. The function of the buncher is to shorten the beam pulse at injection to the SSC to reduce the energy spread during the acceleration process in the SSC. The first buncher (J-line) is installed in the beam line before the SSC that is used for beams from both injectors. The second buncher (K-line) is in the beam line from SPC2.

A fundamental frequency buncher that AC modulates the DC beam is installed in the AX-line between the ion sources and SPC2.

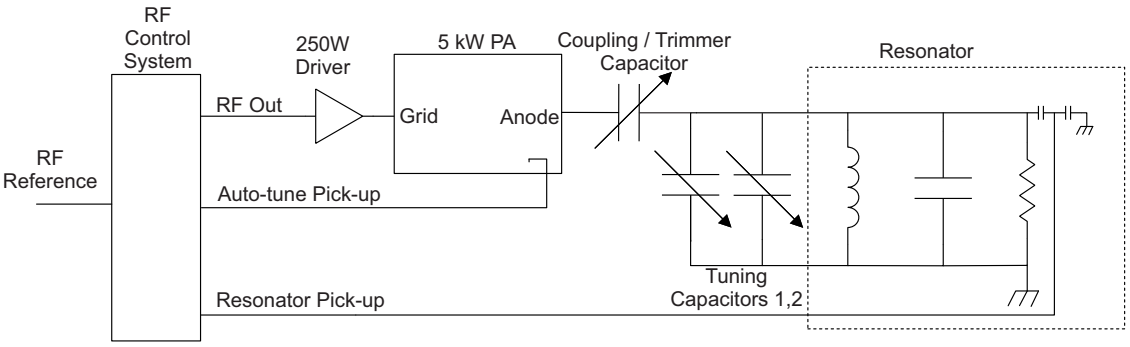

Figure 2.9: An equivalent circuit diagram of the RF system for the J-line and K-line bunchers.

The 2nd harmonic frequency bunchers in the J-Line and K-line are identical and an equivalent circuit diagram of these RF systems is shown in Fig. 2.9. These bunchers operate at frequencies between 16-52 MHz. The resonant frequency of these systems is set by adjusting the tuning capacitors to the required capacitance. Power is delivered at levels up to 5 kW via a tetrode amplifier with the anode coupled directly to the resonator through a coupling capacitor. This coupler also serves as the trimmer and is used to compensate for thermal loading and frequency drift.

The AX-line buncher operates between 8-26 MHz and at power levels between 2 and 10 W. An equivalent circuit diagram of the RF system is shown in Fig. 2.10. A 10 W solid-state amplifier delivers power through a coupling capacitor to an RLC circuit. The coupling capacitor also serves as a trimmer to compensate for frequency and thermal drift. The resonant frequency of the RLC circuit is set by adjusting the tuning inductor.

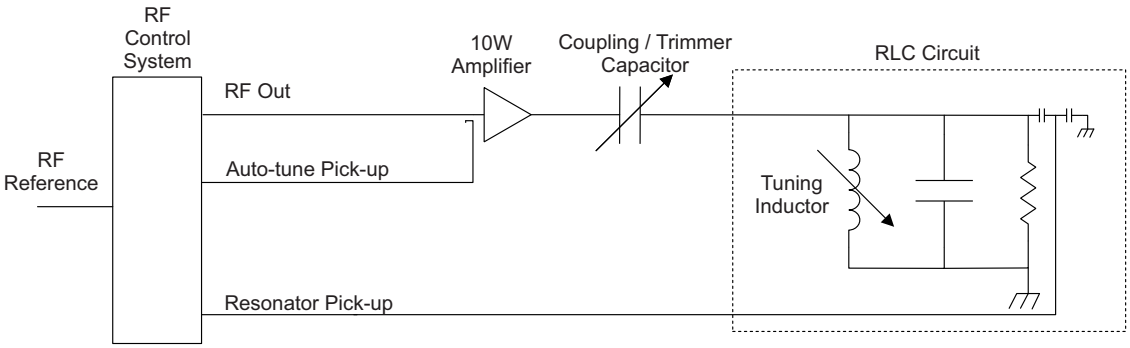

Figure 2.10: An equivalent circuit diagram of the RF system for the AX-line buncher.

2.2.4 The K=200 MeV Separated Sector Cyclotron

A photograph of the west side of the separated-sector cyclotron (SSC) depicting the top half of the west resonator, two of the four sector magnets, the vacuum chamber and the 50 Ohm RF transmission cable that delivers RF power to the west resonator is shown in Fig. 2.11. A detailed diagram depicting a median plane cross section of the SSC from the aspect of the RF system is illustrated in Fig. 2.12.

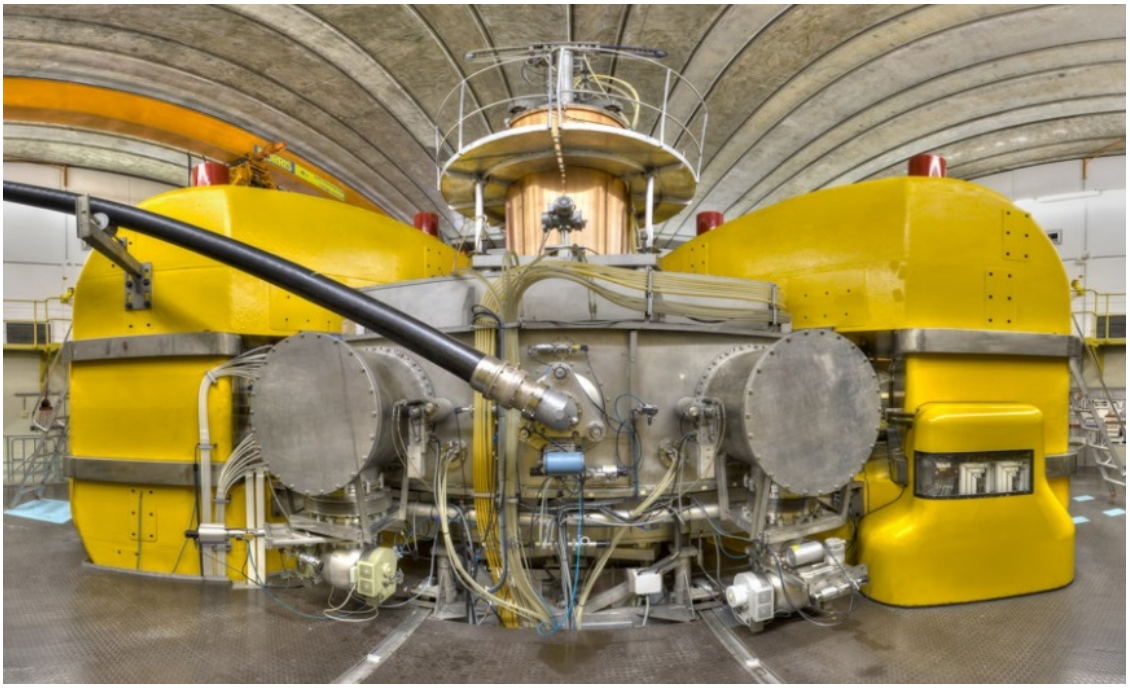

Figure 2.11: A photograph of the west side of the SSC depicting the top half of the west resonator, two sector magnets, the vacuum chamber and the 50 Ohm RF transmission cable that delivers RF power to the resonator.

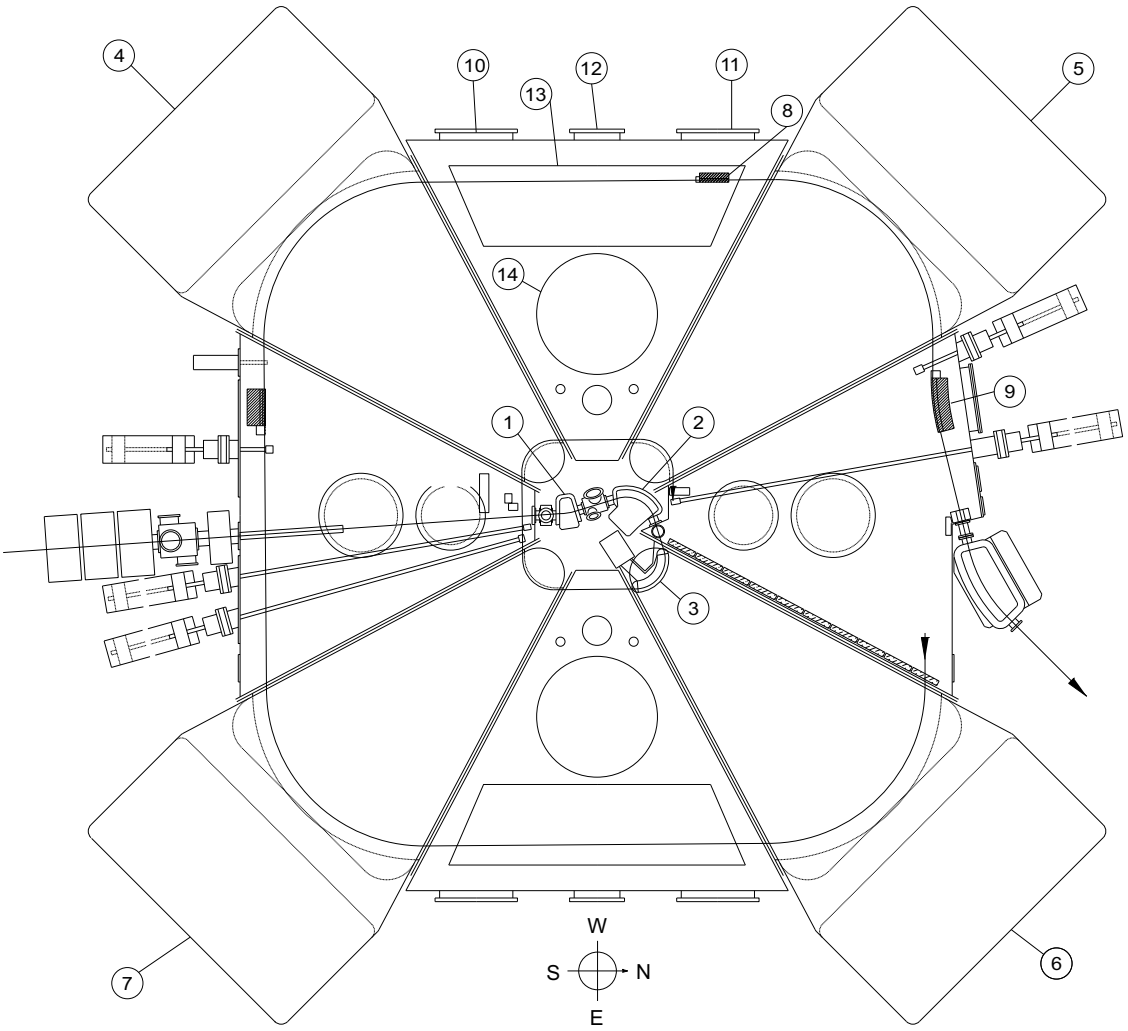

Figure 2.12: A median plane cross section of the SSC showing (1) and (2) the bending magnets (BM1 and BM2), (3) the magnetic inflection channel, (4, 5, 6 and 7) the four sector magnets, (8) and (9) the septum magnets (SPM1 and SPM2), (10) and (11) the west side trimmer capacitors, (12) the west side coupling capacitor, (13) the west side main capacitor and (14) the west side resonator.

The SSC accepts a beam from either SPC1 or SPC2. The beam is injected into the cyclotron at the injection point. The injection system consists of two bending magnets (BM1 and BM2) and a magnetic inflection channel. The bending magnets and the inflection channel are used to place the beam on a centered orbit inside the SSC for the start of the acceleration process.

Two commercial 150KW power amplifiers supply up to 100 kW RF power to two $\lambda/2$ resonators to produce an accelerating dee voltage of 300 kV.The four sector magnets are capable of producing a magnetic field with a flux density of 1.3T. Each magnet rotates the beam through 90° and causes it to orbit inside the accelerator. As the beam is accelerated to higher energies by the RF dee voltage, the orbit radius increases.

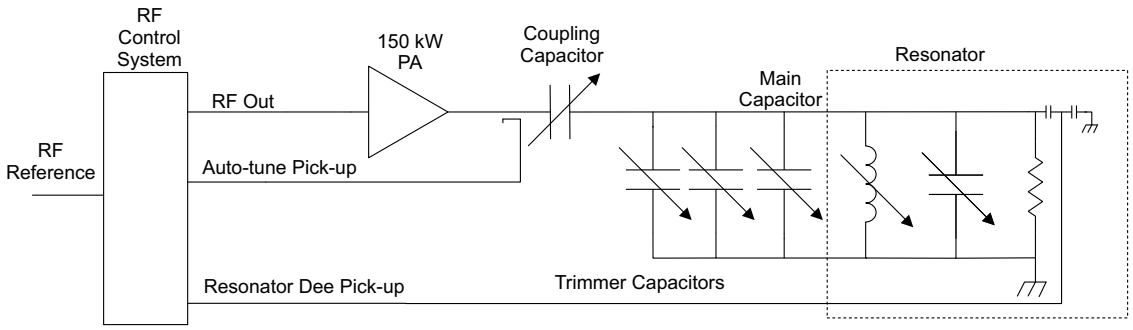

Figure 2.13: An equivalent circuit diagram of the RF system for west and east resonators of the SSC.

Beams of different energies make a different number of orbits in the SSC. The number of orbits varies from 30 for heavy ions to 260 for 200 MeV protons. When the beam reaches its extraction orbit radius, two septum magnets (SPM1 and SPM2) are used to extract the beam into the extraction beam line. Thereafter, the beam is transported to either isotope production, neutron therapy, proton therapy or nuclear physics research.

The east and west RF resonators are identical and only the equivalent circuit diagram of the west resonator is shown in Fig. 2.13. The $\lambda/2$ resonator is represented by a parallel RLC circuit. These resonators can tune over a range of 11 to 26 MHz by means of two short-circuit plates. Below 11 MHz, the variable main capacitors are operated to extend the frequency range of the resonator down to 8 MHz. RF power is delivered via a 50 Ohm transmission line through the coupling capacitor to the resonator. Fine tuning of the resonant frequency is performed using two trimmer capacitors, though at run time only one capacitor is operated by the RF control system to compensate for frequency drift due to thermal loading.

2.2.5 The SSC Flat-Topping System

To improve the beam quality and intensity and to obtain a higher extraction efficiency from the SSC a 3^{rd} harmonic flat-topping system was installed on the SSC.

The system operates at 49.1208 MHz which is the 3^{rd} harmonic of the frequency required to produce a high current 66 MeV proton beam for isotope production. An equivalent circuit diagram of the RF system is shown in Fig. 2.14. A 25 kW amplifier delivers RF power through a coupling inductor to the resonator. A trimmer inductor is used to fine tune the resonant frequency and to compensate for thermal loading and frequency drift during operation.

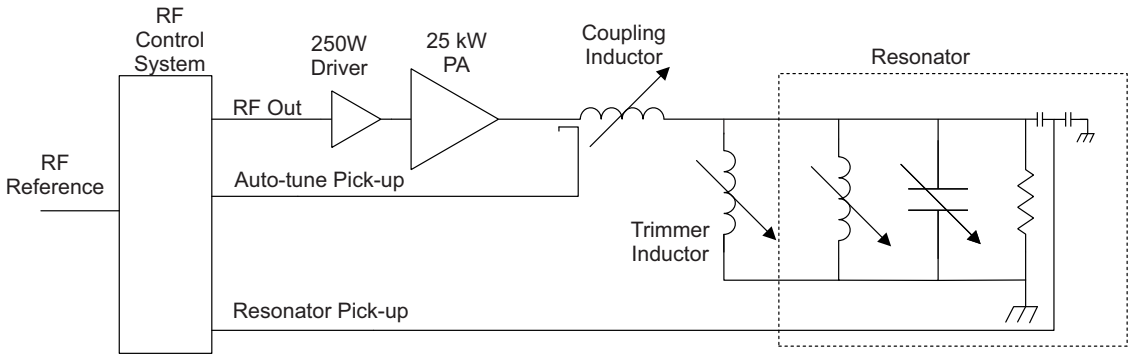

Figure 2.14: An equivalent circuit diagram of the RF system for the SSC flat-topping RF system.

2.2.6 The Pulse-Selector System

A beam pulse-selector system is installed at injection to the SSC. The system selects the number of beam bunches that are allowed into the SSC and can run at 1/7, 1/6, 1/5, 1/4, 1/3 or 1/2 of the fundamental frequency within in a band of 2 to 3.8 MHz.

An equivalent circuit diagram of the RF system is shown in Fig. 2.15. A 1 kW amplifier delivers RF power through a coupling/trimmer capacitor to an RLC circuit. A variable inductor sets the resonant frequency of the RLC circuit. The trimmer/coupler capacitor is used to fine tune the resonant frequency and to compensate for thermal loading and frequency drift during operation.

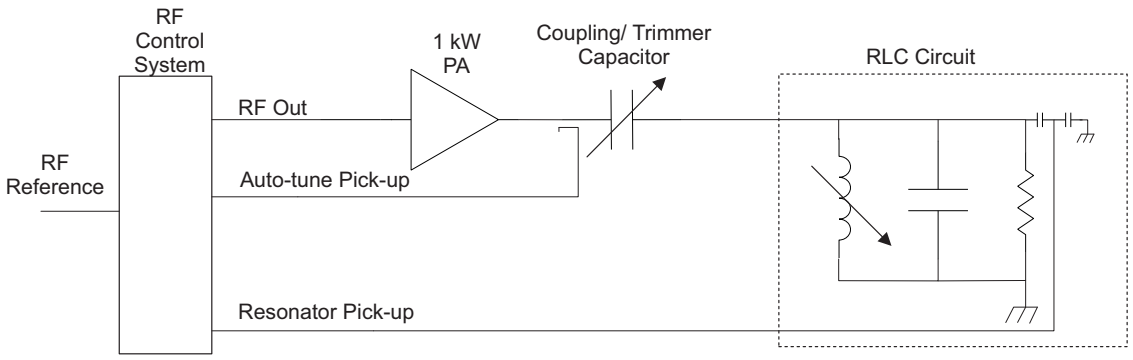

Figure 2.15: An equivalent circuit diagram of the RF system for the pulse-selector RF system.

2.3 The Legacy Analog RF Control System at iThemba LABS

The following section provides a description of the analog RF control system in use before replacement as described in this thesis. The system will henceforth be referred to as the legacy control system. The descriptions will refer to the block diagram shown in Fig. 2.16 and the photographs of the various elements of the RF control system shown in Fig. 2.17.

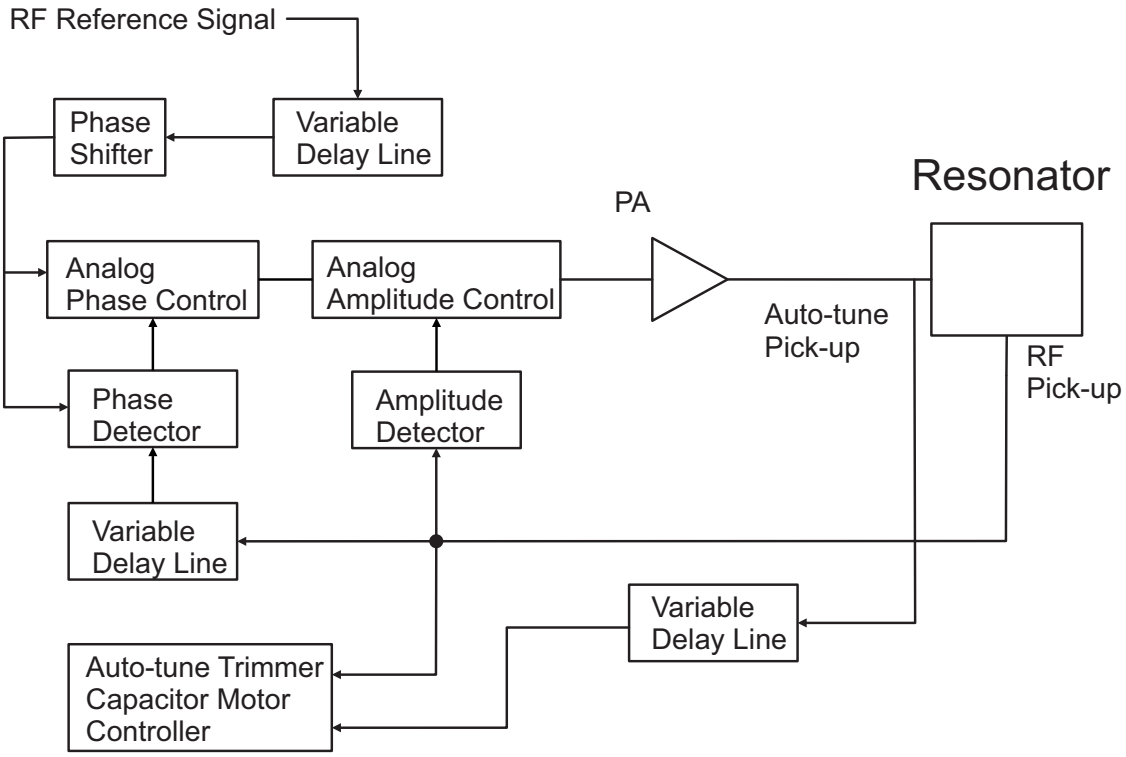

Figure 2.16: A high level block diagram of the previous analog control system.

2.3.1 Description of the Legacy RF Control System

The legacy control system was designed in the 1980's. It was a modular design that was realized as a rack of modules depicted in Fig. 2.17. To a certain extent the core of the system was generically applicable across the various RF systems at iThemba LABS.

The RF reference signal from the main synthesizer was fed through a variable delay line, consisting of switchable line segments, to set the coarse system phase. This signal was then fed through a voltage controlled phase shifter that was used to adjust the fine system phase. The output of the phase shifter was fed to the analog phase controller and phase detector system. The latter compared the system phase with the phase of the resonator pick-up. A variable delay line was used in line with

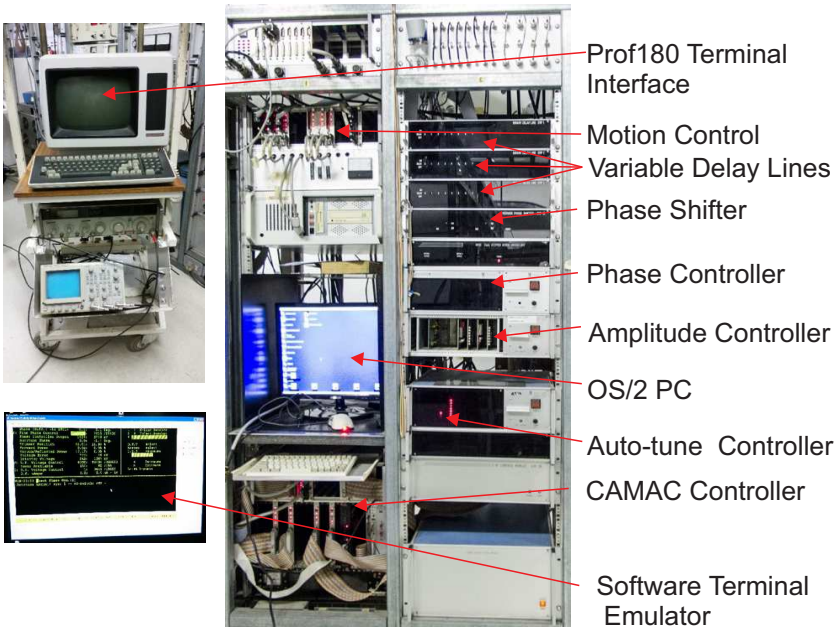

Figure 2.17: Elements of the previous control system.

the resonator pick-up to adjust the phase of the signal to within the working range of the phase detector. The analog output of the phase detector was fed to an analog phase control system where the bandwidth and amplitude of the error signal were determined by a variable pole filter and variable gain amplifier. This conditioned error signal was subsequently passed to a voltage controlled phase modulator.

The analog phase control system output was the input of the analog amplitude control system. The amplitude controller also accepted the output of the amplitude detector module that converted the resonator pick-up signal to a DC voltage proportional to the RF level using rectifier diodes. The bandwidth and amplitude of the rectified signal was conditioned by a variable pole filter and variable gain amplifier. This signal was then compared with a DC voltage reference representing the RF level set point and the error signal was used to drive the input of a diode modulator that modulated the RF signal that came from the output from the phase control system.

The control system parameters were controlled via an embedded PROF180 controller running the Control Program/Monitor (CP/M) operating system, that was interfaced to the control modules through a CAMAC system. The initial user interface for all the RF control systems was a Hazeltine terminal that connected to the processor via RS232. In time, the hardware terminal was replaced with a software terminal emulator. The embedded controller for SPC2's RF systems was also replaced by PC control. This user interface was based on the in-house designed CONS distributed control system that was implemented on the IBM OS/2 operating system. Although the legacy control system performed reliably, the maintainability of the system was significantly hampered by the unavailability of legacy parts.

2.3.2 Performance of the Legacy RF Control System

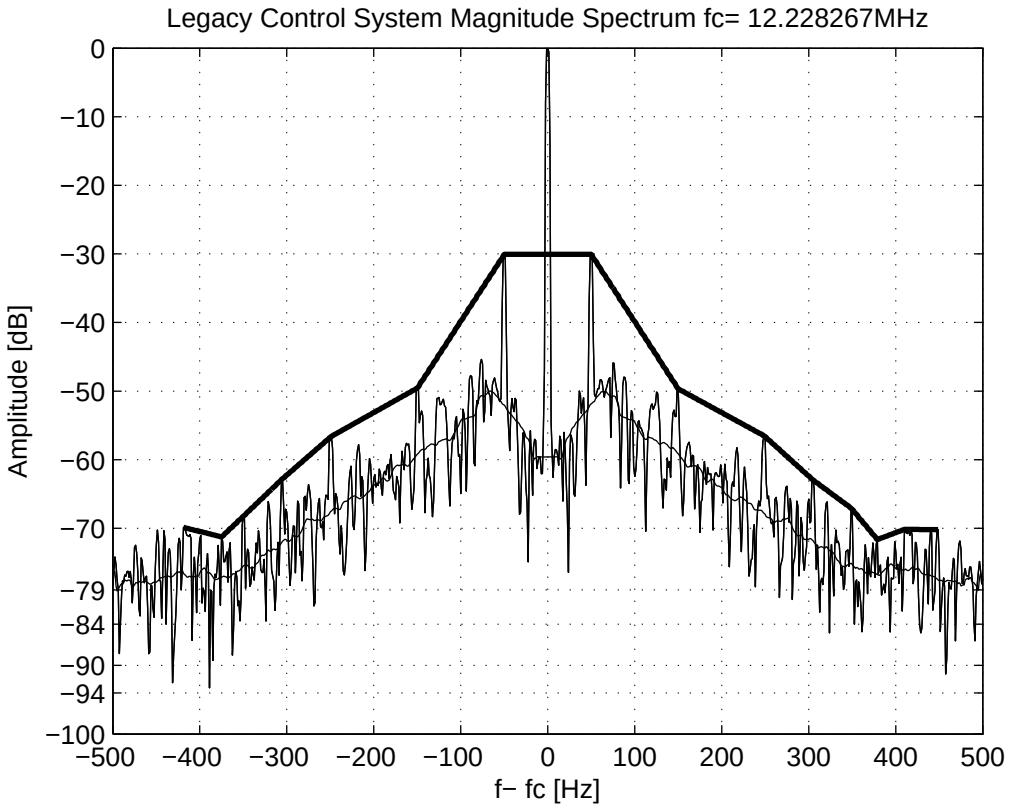

Figure 2.18: The normalized magnitude spectrum of SPC2 south resonator under closed-loop control at 12.228267 MHz using the previous control system.

The reported performance of the legacy RF control systems on SPC2 in terms of amplitude stability was 1/1000 or 60 dB and the phase stability was 0.1° (Conradie, 2004). The normalized magnitude spectrum of SPC2 south resonator under closed-loop control at 12.228267 MHz using the legacy control system is illustrated in Fig. 2.18. The plot also includes the envelope of the normalized magnitude spectrum, which indicates the spurious free dynamic range (SFDR) and a filtered noise floor which gives an indication of the system's noise floor. An analysis reveals that for SPC2, only the amplitude stability close to the carrier is 60 dB. Further away from the carrier the SFDR becomes substantially worse, exhibiting a minimum SFDR of 30 dB which is a result of the 50 Hz side lobes injected by the synthesizer. This noise falls well within the passband of the resonators and it is suspected that this in-band noise contributes to the energy spread of the beam.

2.3.3 Diagnostic Limitations and Operational Problems

Other than connecting a spectrum analyzer and oscilloscope to pick-up signals and diagnostic ports, no real-time diagnostic information was available to the operator for the legacy control system. Only highly filtered error voltage measurements were available at the terminal operator interface and these refreshed slowly (approximately once every second). Diagnosis of higher frequency instabilities was impossible using the operator interface and large or fluctuating error voltages were the only indication of control system or other component failures. Further control system measurements, for example phase and amplitude, were available on 7 segment LED displays forming part of the system modules. However, the displays updated slowly and reported a highly filtered and averaged measurement.

For an analog system, it could be problematic when a critical component such as the diode rectifiers in the amplitude detector module failed. In such a case, the system would need to be recalibrated because all previous amplitude set points would become invalid.

Aside from system failure, a typical operational problem occurred when a high voltage breakdown within the resonator caused the RF control system to trip or when an external interlock from the cooling water supply, safety control or similar system interrupted the system operation. The system would attempt to switch itself back on once the interlock cleared but this was not always successful because the resonance position could change with time as the resonator cooled. Another scenario occurred when the operator moved mechanical assemblies such as the ion source within the cyclotron. The operation of the trimmer and auto-tune circuit should have tracked this change but as in the case where the resonator had cooled, the cold start resonance position could have changed. In both cases, the engineer on standby would need to be called out to find the correct resonance position and switch the system back on.

2.3.4 Setting-up and Operation

Setting up the legacy RF control system for a specific particle energy was achieved using the terminal interface by loading previously-used settings. When a new setup needed to be computed, this was done manually by the RF operator with the help of a network analyzer as well as forward and reflected power meters in the amplifier chain. Typically, the operator would first place the amplifier on a 50 Ohm dummy load. Using a synthesizer, the driver output could be matched to the tube-based power amplifier by adjusting the tunable elements of the grid matching circuit to minimize reflected power. The output stage of the power amplifier could be matched to the 50 Ohm dummy load by adjusting the tunable elements of anode matching circuit to maximize RF output power and minimize anode current.

A network analyzer was used to determine the resonance positions of the tunable elements of the resonator. Typically, the short-circuit plates were moved until the resonator response matched the resonance frequency. The coupling capacitor position was then adjusted to match the resonator's characteristic impedance to 50 Ohms. Finally, the trimmer capacitor was adjusted to achieve a real impedance of

50 Ohms. A good setup was achieved when the real 50 Ohm impedance position was at the middle of the trimmer capacitor's movement range. Once this was completed, the amplifier chain would be reconnected to the resonator.

Although the systems were individually initialized for a characteristic impedance of 50 Ohms, the resonance position of the trimmer may have changed again when the systems were coupled. In this case, fine tuning of the trimmer capacitor position was required. To achieve this, a synthesizer was usually manually connected to the driver amplifier input. The frequency response of the resonator was monitored by connecting the resonator pick-up signal to an oscilloscope. By sweeping the synthesizer frequency manually with a low drive below the multipacting level and at the same time observing the oscilloscope for the occurrence of a peak, the resonance position could be found. This typically required that the oscilloscope was configured at its highest sensitivity because the received signal was small and difficult to distinguish from the noise. The trimmer capacitor position was adjusted until the peak level occurred at the desired system frequency.

Once the system was fine tuned, the cables were reconnected to the RF control system. The operator would first need to ensure that the power level settings were correct before attempting to switch on the RF control system. The key for the operator was to attempt to switch on the RF system at a low amplitude to ensure that no damage would occur to the amplifier chain because the power amplifiers could withstand unmatched loads only at low power levels. The operator also had to ensure that the RF amplitude kick pulse was higher than the multipacting level. Once the system was operational, fine-tuning of the grid matching was carried out to minimize the reflected power between the driver amplifier and the grid circuit of the power amplifier. Next the phase reference of the auto-tune system that controls the trimmer capacitor position was adjusted until the reflected power measured at the output of the power amplifier was minimized. If all the reflected power levels were acceptable, the system would be placed under closed-loop amplitude and phase control. The final check was to gradually increase the power level towards the desired operating level. If the system behaved as expected it was handed over to the cyclotron operators to produce a beam.

2.4 An Overview of the Cyclotron and RF Systems at the Helmholtz-Zentrum Berlin

The Helmholtz-Zentrum Berlin (HZB) is a multi-disciplinary research facility situated in Berlin, Germany. It operates a Tandetron and a Van De Graaff (CN Injector) accelerator as the injectors for its K=132 MeV separated sector cyclotron to deliver particle beams for experiments and radiotherapy used in eye tumour treatment. Figure 2.19 shows the layout of the facilities at Helmholtz-Zentrum Berlin.

Two buncher systems are located in the injection lines and another buncher is located after the cyclotron. In total there are 5 RF systems that operate at frequencies between 10 and 20 MHz and at power levels of between 1 and 30 kW

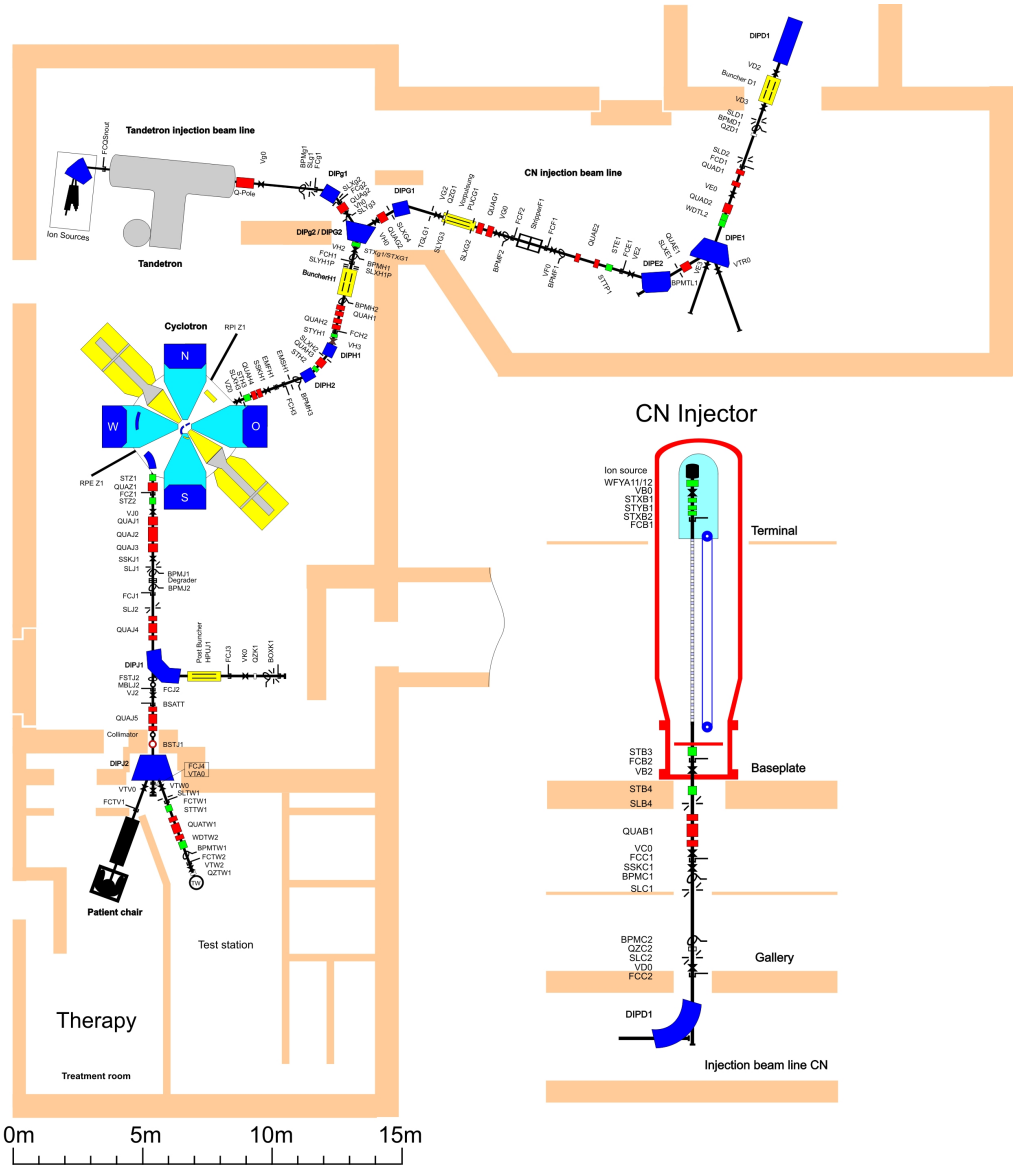

Figure 2.19: The layout of the facilities at the Helmholtz-Zentrum Berlin.

to deliver particle beams for experiments and radiotherapy. The RF systems of the north and south resonator of the HZB separated sector cyclotron were successfully upgraded with the RF control system described in this thesis in April 2017. The following sections provide an overview of the HZB cyclotron's legacy RF control systems.

2.4.1 The K=132 MeV Cyclotron

The cyclotron at the Helmholtz-Zentrum Berlin is a separated sector cyclotron, a photograph of which is shown in Fig. 2.20.

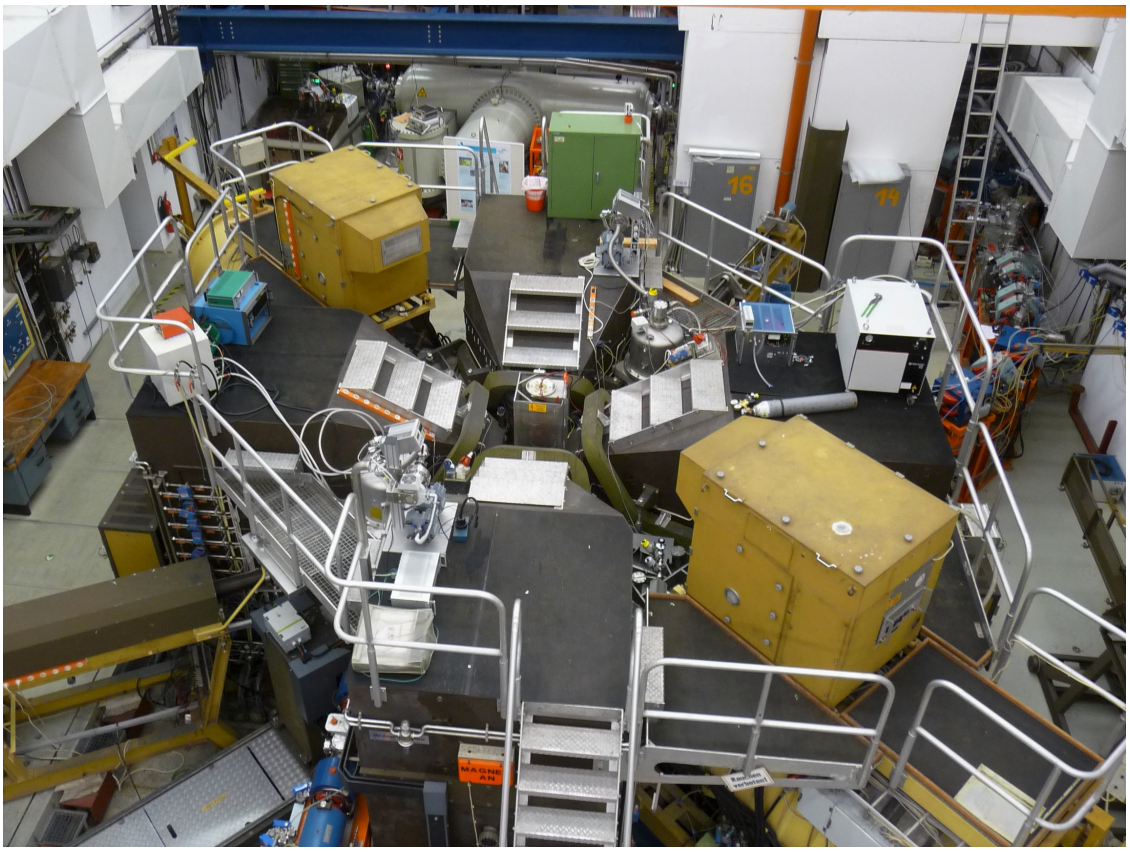

Figure 2.20: A photograph of the separated sector cyclotron at the Helmholtz-Zentrum Berlin.

The cyclotron is a four-sector machine with two 26° dees. The RF systems consist of two $\lambda/4$ resonators which can be tuned between 10-20 MHz using movable short-circuit plates. A simplified equivalent circuit diagram of the RF system for one of the resonators of the HZB cyclotron is shown in Fig. 2.21. The anode circuits of each of the 30 kW tetrode RF amplifiers are directly coupled to the dees through inductive couplers to produce a maximum dee voltage of 140kV. This design is different from that employed by the RF systems at iThemba LABS which have 50 Ohm transmission lines between the RF amplifiers and the resonators.

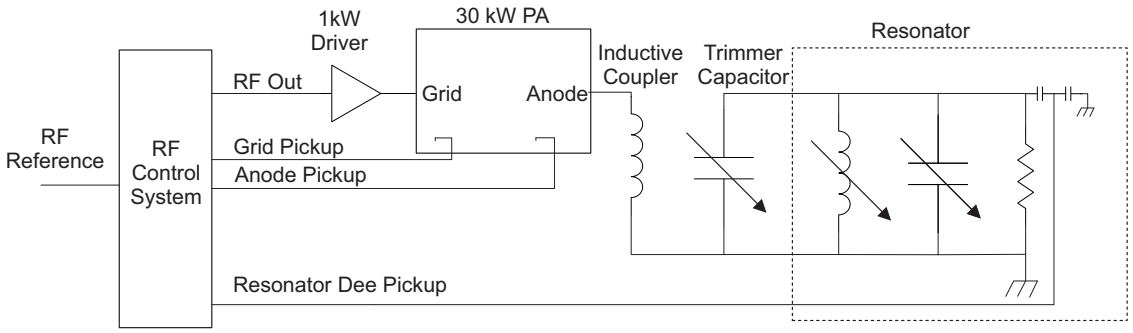

Figure 2.21: A simplified equivalent circuit diagram of the RF system for one of the resonators of the HZB cyclotron.

Fine tuning of the resonant frequency can be performed by using the trimmer flap capacitor. Frequency drift due to thermal loading can be performed by moving the flap during operation. In contrast to iThemba LABS, the anode and grid pick-ups' phase difference are used to control the position of the flap trimmer capacitor. In this case the phase between the two must be kept at 180°.

2.5 Effect of RF Dee Voltage Stability on the Performance of Cyclotrons

In this section the effect of the RF voltage's amplitude and phase noise on the energy spread and the radial width change per turn of a beam of an isochronous cyclotron with and without flat-topping engaged are analyzed. In each case the ideal case without noise and then with noise are analyzed for the SSC for 66 MeV proton beams.

2.5.1 Isochronous Cyclotron without Flat-topping

The ideal energy spread for an isochronous cyclotron without flat-topping engaged can be defined as (see Appendix A.1)

$$\frac{\Delta E}{E} = \cos\left(\frac{\Delta\theta}{2}\right) - 1 \tag{2.4}$$

where $\frac{\Delta\theta}{2}$ is the maximum phase deviation with respect to the central particle.

However, Eqn. 2.4 does not take into account the RF voltage's amplitude and phase noise and can be reformatted as follows to take these into account (see Appendix A.1):

$$\frac{\Delta E}{E} = \left[1 - \frac{V_n}{2V_D}\right]\cos\left(\frac{\phi_n}{2} + \frac{\Delta\theta}{2}\right) - \left[1 + \frac{V_n}{2V_D}\right] \tag{2.5}$$

with

V_D = the dee RF voltage,
$\frac{\Delta\theta}{2}$ = the maximum phase deviation with respect to the central particle,
V_n = the maximum peak-peak amplitude noise of the RF voltage and
ϕ_n = the maximum peak-peak phase noise of the RF voltage.

A measure for the effect of the amplitude and phase noise on the energy spread is graphically illustrated in Fig. 2.22. The ideal energy spread is represented by the dashed line and the envelope of the energy spread resulting from the RF noise components is represented by the solid-lines for the case in which the peak-peak phase stability $\phi_n = 10°$ and peak to peak amplitude stability $\frac{V_n}{V_D} = 1/10$.

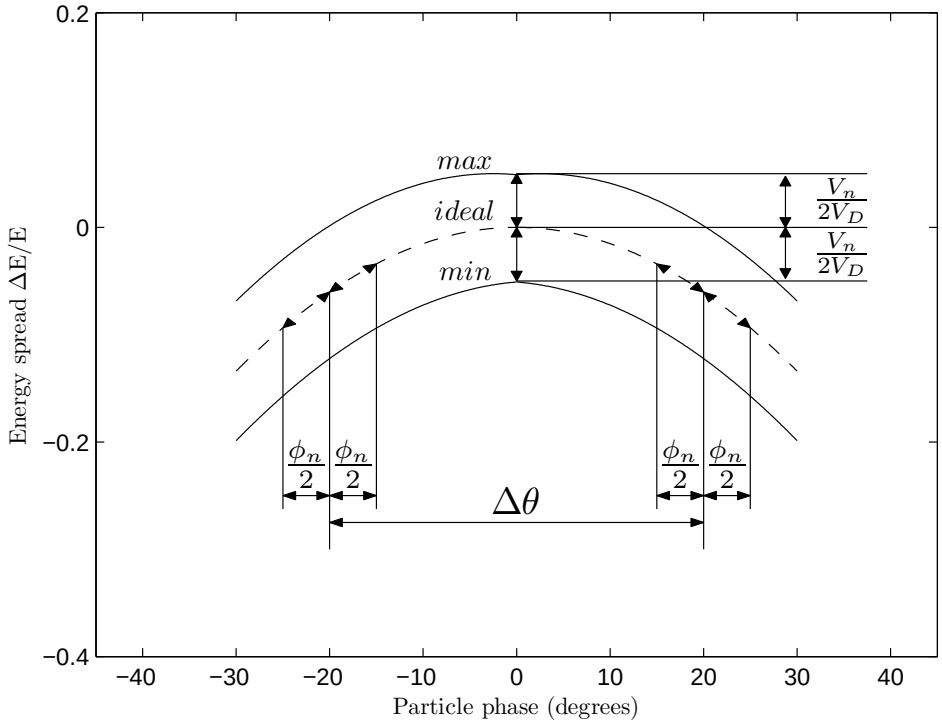

Figure 2.22: The energy spread of a beam pulse from an isochronous cyclotron without a flat-topping system.

The change in radial width due to the energy spread ΔR on a specific orbit in the cyclotron is directly proportional to the energy spread and is given by (Conradie, 1992):

$$\Delta R = \frac{R}{\gamma(\gamma+1)}\frac{\Delta E}{E} \tag{2.6}$$

with

R = the radius,
γ = the Lorentz factor,
$\frac{\Delta E}{E}$ = the energy spread.

The energy spread $\frac{\Delta E}{E}$ and radial width change ΔR at extraction with R=4156 mm of a beam pulse with $\Delta\theta$=18° from the SSC without the flat-topping acceleration RF system engaged are calculated using Eqns. 2.5 and 2.6 with simulated amplitude and phase noise, with a peak-peak amplitude stability $\frac{V_n}{V_D}$ and peak-peak phase stability ϕ_n, for 66 MeV protons. The results are displayed in Table 2.1.

The ideal case with no noise is displayed in the first row. For each following row the amplitudes of the noise components are decreased and the calculated energy spread $\frac{\Delta E}{E}$, radial width increase ΔR, as well as the radial width change from the ideal $\Delta R - \Delta R_{ideal}$ are calculated.

Table 2.1: The energy spread and radial width change at extraction with R=4156 mm of a beam pulse of $\Delta\theta$ = 18 degrees from the SSC without the flat-topping acceleration RF system engaged and with simulated amplitude and phase noise for 66 MeV protons with γ=1.07034.

No	$\frac{V_n}{V_D}$	ϕ_n	$\frac{\Delta E}{E}$	ΔR [mm]	$\Delta R - \Delta R_{ideal}$ [mm]
1	0	0	-0.0123	-23.09	0.00
2	1/100	1	-0.0236	-44.35	-21.26
3	1/100	0.1	-0.0224	-41.99	-18.89
4	1/200	0.1	-0.0174	-32.67	-9.58
5	1/500	1	-0.0157	-29.45	-6.36
5	1/500	0.1	-0.0144	-27.07	-3.98
7	1/2000	1	-0.0142	-26.65	-3.56
8	1/5000	1	-0.0139	-26.09	-3.00
6	1/1000	0.1	-0.0134	-25.21	-2.12
7	1/2000	0.1	-0.0129	-24.28	-1.19
9	1/5000	0.1	-0.0126	-23.72	-0.63
10	1/10000	0.01	-0.0124	-23.30	-0.21
11	1/10000	0.005	-0.0124	-23.29	-0.20
12	1/20000	0.01	-0.0124	-23.21	-0.12
13	1/20000	0.005	-0.0124	-23.20	-0.11

The values in Table 2.1 indicate that the noise components have a significant impact on the energy spread and radial width change for 66 MeV protons. Furthermore, with peak-peak amplitude and phase noise stabilities of below 1/5000 and 0.01°, the effect starts to become smaller and approaches the ideal case.

2.5.2 Isochronous Cyclotron with Flat-topping

The energy spread of an isochronous cyclotron can be improved by the addition of an n^{th} harmonic RF voltage. At iThemba LABS a fixed-frequency 3rd harmonic flat-topping system is used on the SSC to improve the 66 MeV proton beam intensity for isotope production. The principle is illustrated in Fig. 2.23 and the blue line indicates the resultant flat-topped accelerating voltage for three RF cycles.

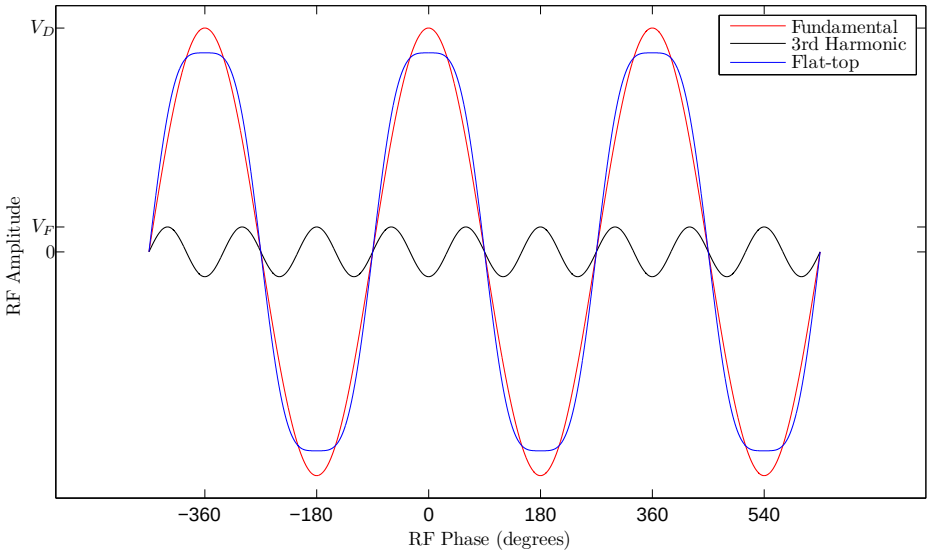

Figure 2.23: The resultant accelerating voltage with a 3rd harmonic flat-topping acceleration RF system for 3 RF cycles.

The ideal energy spread for an isochronous cyclotron with flat-topping can be defined as (see Appendix A.2)

$$\frac{\Delta E}{E} = \frac{\cos(\frac{\Delta\theta}{2}) - \frac{1}{n^2}\cos(n\frac{\Delta\theta}{2})}{1 - \frac{1}{n^2}} - 1 \tag{2.7}$$

with

V_D = the dee RF voltage,

$\frac{\Delta\theta}{2}$ = the maximum phase deviation with respect to the central particle.

However, Eqn. 2.7 does not take into account the RF voltage's amplitude and phase noise and can be reformatted as follows to take these into account (see Appendix A.2):

$$\frac{\Delta E}{E} = \frac{\left[1 - \frac{V_n}{2V_D}\right]\cos(\frac{\phi_n}{2} + \frac{\Delta\theta}{2}) - \frac{1}{n^2}\left[1 + \frac{V_{Fn}}{2V_F}\right]\cos(\frac{\phi_{Fn}}{2} + n\frac{\Delta\theta}{2})}{\left[1 - \frac{1}{n^2}\right]} - \frac{\frac{V_n}{2V_D} + \frac{1}{n^2}\frac{V_{Fn}}{2V_F}}{\left[1 - \frac{1}{n^2}\right]} - 1 \tag{2.8}$$

with

V_D = the dee RF voltage,
V_F = the flat-top RF voltage,
$\frac{\Delta\theta}{2}$ = the maximum phase deviation with respect to the central particle,
V_n = the maximum peak-peak amplitude noise of the dee RF voltage,
ϕ_n = the maximum peak-peak phase noise of the dee RF voltage,
V_{Fn} = the maximum peak-peak amplitude noise of the flat-top RF voltage and
ϕ_{Fn} = the maximum peak-peak phase noise of the flat-top RF voltage.

Equation 2.8 can only be numerically solved using simulated noise values. The SSC has a fixed frequency 3rd harmonic flat-topping resonator. A measure for the effect of the noise is graphically illustrated in Fig. 2.24 for the ideal energy spread (dashed line) and the envelope of the energy spread with the RF noise components (solid lines) for $\phi_n = 10°$, $\frac{V_n}{V_D} = 1/10$, $\phi_{Fn} = 10°$ and $\frac{V_{Fn}}{V_F} = 1/10$. The $\delta\phi$ variable is used to represent the total peak-peak phase noise contribution of both the fundamental and flat-topping systems.

The energy spread $\frac{\Delta E}{E}$ and radial width change ΔR at extraction with R=4156 mm of a beam pulse of $\Delta\theta = 18°$ and $\Delta\theta = 49.5°$ from the SSC with a 3rd harmonic flat-topping acceleration RF system can be calculated from Eqns. 2.8 and 2.6 with simulated dee RF voltage peak-peak amplitude and phase stability, $\frac{V_n}{V_D}$ and ϕ_n, and simulated flat-top RF voltage peak-peak amplitude and phase stability, $\frac{V_{Fn}}{V_F}$ and ϕ_{Fn}, for 66 MeV protons. The results are presented in Tabs. 2.2 and 2.3.

As in the previous section, for both tables, the ideal case with no noise components is shown in the first row. For each of the following rows, the peak-peak amplitudes of the noise components decrease and the calculated energy spread $\frac{\Delta E}{E}$, radial width change ΔR, as well as the radial width change from the ideal $\Delta R - \Delta R_{ideal}$ are calculated.

For $\Delta\theta$=18°, Table 2.2 indicates that there is a dramatic improvement in the energy spread and radial width change with the addition of the flat-topping system. However, we also see that the noise components have a significant impact on the

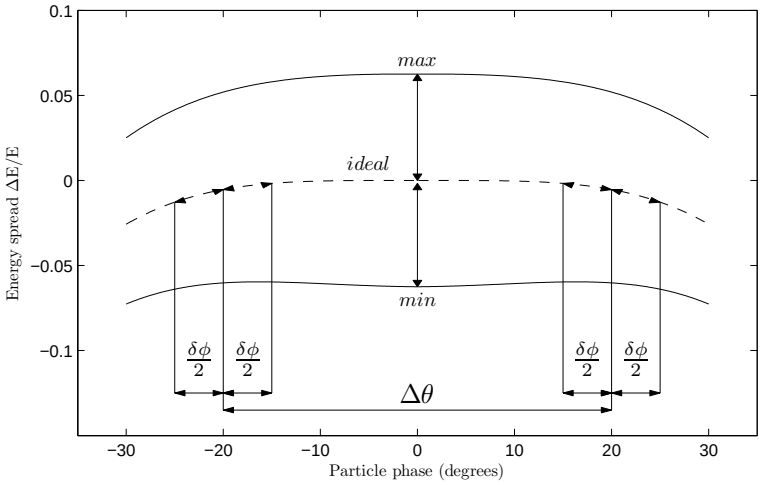

Figure 2.24: The energy spread of a beam pulse from a cyclotron with a 3rd harmonic flat-topping acceleration RF system.

energy spread and radial width change and with peak-peak amplitude and phase noise stabilities below 1/5000 and 0.1°, the effect becomes smaller and approaches the ideal case.

Table 2.2: The energy spread and radial width change at extraction with R=4156 mm of a beam pulse of $\Delta\theta$ = 18 degrees from the SSC with the flat-topping acceleration RF system engaged with simulated amplitude and phase noise for 66 MeV protons with γ=1.07034.

No	$\frac{V_n}{V_D}$	$\frac{V_{Fn}}{V_F}$	ϕ_n	ϕ_{Fn}	$\frac{\Delta E}{E}$	ΔR [mm]	$\Delta R - \Delta R_{ideal}$ [mm]
1	0	0	0	0	-0.0002	-0.42	0.00
2	1/100	1/100	1	1	-0.0137	-25.61	-25.19
3	1/100	1/100	0.1	0.1	-0.0127	-23.80	-23.38
4	1/200	1/200	0.1	0.1	-0.0065	-12.21	-11.79
5	1/500	1/500	0.1	0.1	-0.0028	-5.26	-4.83
6	1/1000	1/200	0.1	0.1	-0.0020	-3.83	-3.40
7	1/1000	1/500	0.1	0.1	-0.0017	-3.16	-2.74
8	1/1000	1/1000	0.1	0.1	-0.0016	-2.94	-2.51
9	1/2000	1/2000	0.1	0.1	-0.0009	-1.78	-1.36
10	1/5000	1/5000	0.1	0.1	-0.0006	-1.08	-0.66
11	1/10000	1/10000	0.01	0.01	-0.0004	-0.68	-0.25
12	1/10000	1/10000	0.005	0.005	-0.0004	-0.67	-0.24
13	1/20000	1/20000	0.01	0.01	-0.0003	-0.56	-0.14
14	1/20000	1/20000	0.005	0.005	-0.0003	-0.55	-0.13

It is clear that the flat-top system allows a wider beam pulse to be injected into the SSC. Table 2.3 shows that a beam pulse width of $\Delta\theta$=49.5° will have the same energy spread and radial width change as a beam pulse width of $\Delta\theta$=18° in Table

2.1. For a beam pulse width of $\Delta\theta$=49.5° and when the peak-peak amplitude and phase noise stabilities are below 1/5000 and 0.1°, the effect becomes smaller and approaches the same energy spread and radial width change of a beam pulse of $\Delta\theta$=18° with no flat-topping system.

Table 2.3: The energy spread and radial width change at extraction with R=4156 mm of a beam pulse of $\Delta\theta$ = 49.5 degrees from the SSC with the flat-topping acceleration RF system with simulated amplitude and phase noise for 66 MeV protons with γ=1.07034.

No	$\frac{V_n}{V_D}$	$\frac{V_{Fn}}{V_F}$	ϕ_n	ϕ_{Fn}	$\frac{\Delta E}{E}$	ΔR [mm]	$\Delta R - \Delta R_{ideal}$ [mm]
1	0	0	0	0	-0.0123	-23.01	0.00
2	1/100	1/100	1	1	-0.0269	-50.39	-27.38
3	1/100	1/100	0.1	0.1	-0.0241	-45.20	-22.19
4	1/200	1/200	0.1	0.1	-0.0183	-34.39	-11.38
5	1/500	1/500	0.1	0.1	-0.0149	-27.91	-4.90
6	1/1000	1/200	0.1	0.1	-0.0140	-26.34	-3.33
7	1/1000	1/500	0.1	0.1	-0.0138	-25.90	-2.89
8	1/1000	1/1000	0.1	0.1	-0.0137	-25.75	-2.74
9	1/2000	1/2000	0.1	0.1	-0.0132	-24.67	-1.66
10	1/5000	1/5000	0.1	0.1	-0.0128	-24.02	-1.01
11	1/10000	1/10000	0.01	0.01	-0.0124	-23.28	-0.27
12	1/10000	1/10000	0.005	0.005	-0.0124	-23.26	-0.24
13	1/20000	1/20000	0.01	0.01	-0.0124	-23.18	-0.17
14	1/20000	1/20000	0.005	0.005	-0.0123	-23.15	-0.14

2.6 Current State Of Technology

The continuing rapid advances in field programmable gate arrays (FPGA), digital signal processing (DSP), high speed digital to analog converters (DAC) and high speed analog to digital converters (ADC) have made it feasible to develop state of the art digital RF control systems (Angoletta, 2006; Yu *et al.*, 2004). With this in mind the following sections are used to evaluate the demodulation, modulation, and DSP techniques of LLRF systems as described in the literature.

2.6.1 Demodulation Techniques

In this section the demodulation techniques that are suited to extract amplitude and phase information from RF signals in LLRF systems are discussed. Schematic representations of possible techniques are illustrated in Fig. 2.25 and the descriptions and utilization are described below. For the implementations that use in-phase and quadrature (I/Q) demodulation, the I/Q components of the RF signal are discussed in Section 2.6.1.2.

The first technique illustrated in Fig. 2.25 utilizes analog amplitude and phase demodulation to generate proportional voltages which are sampled by ADCs. This is a similar method to that used in the legacy control system, except that digital as opposed to analog control is performed once the amplitude and phase information

is extracted. Typically, the RF signal is split. A diode detector followed by a filter demodulates the amplitude information and an LO multiplied with the RF signal and then filtered demodulates the phase (Ziemer and Tranter, 2006; Fong, 2007; Schilcher, 2008).

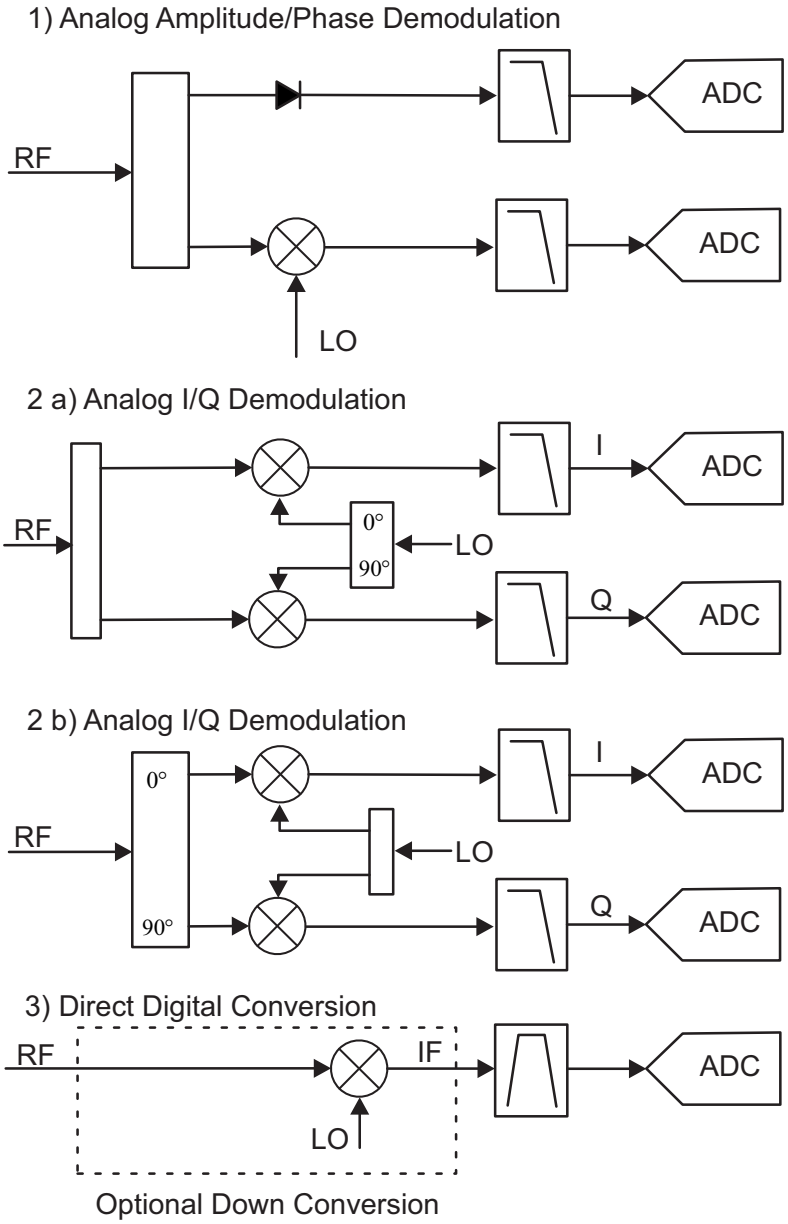

Figure 2.25: The demodulation techniques that can be implemented to extract amplitude and phase information from the RF signal in a LLRF system.

The second technique illustrated in Fig. 2.25 utilizes analog I/Q demodulation, with the I/Q signals sampled by ADCs (Fong, 2007; Schilcher, 2008). Two variants are shown. In the first variant, phase shifted versions of the LO signal are multiplied with the RF signal. In the second variant, phase shifted versions of the RF signal

are multiplied with the LO signal. In both implementations, low-pass filters after the multipliers remove the unwanted high-frequency components that result from the mixing process and extract the I/Q signals. The I/Q demodulation can be implemented discretely as in the two variants described. Integrated devices have also been developed that implement the analog I/Q demodulation. However, these devices do not operate in the required frequency band.

The third technique illustrated in Fig. 2.25 is direct digital conversion, where the RF signal is band-pass filtered and then sampled by an ADC (Fong, 2007; Schilcher, 2008). Critical to the implementation of this method is the frequency band of operation and the amplitude and phase resolution achievable by the ADCs as the effect of the sample clock jitter on the ADCs' performance is substantial, as described in Section 2.6.1.1. The tight specification imposed by the effects of jitter can be averted by utilizing the optional mixer and an LO to perform down conversion of the RF signal to an IF frequency which can be sampled by an ADC at a lower speed (Fong, 2007; Schilcher, 2008).

2.6.1.1 Effect of Clock Jitter on High-speed Analog to Digital Converters

High-speed ADCs can be used to digitally quantize RF or IF signals and the important performance constraints that need to be considered when choosing an ADC are described below.

The ideal SNR of a digitally quantized sinusoidal signal is determined by (Kester, 2005)

$$SNR_{bits} = 6.02 \times N + 1.761 \tag{2.9}$$

with

N the number of bits of the ADC.

To achieve 1/10000 or 80 dB amplitude resolution, the ADC will have 14 or more bits. For 14 and 16 bit ADCs the SNR would be 86.04 and 98.8 dB respectively. For high-speed ADCs, the jitter of the sampling clock effects the SNR of the ADC. The limitation on the achievable SNR as a result of this jitter is given by (Reeder *et al.*, 2008) as

$$SNR_{jitter} = 20 \log_{10} \left[\frac{1}{2\pi f_{in} t_{jitter}} \right] \tag{2.10}$$

with

f_{in} = the input frequency in Hertz,
t_{jitter} = the jitter of the sampling clock in seconds.

Table 2.4 displays the maximum allowable jitter for various frequencies of the signal to be sampled in order to achieve a 80 dB SNR, a 86.04dB SNR for a 14-bit

ADC and a 98.08dB SNR for a 16-bit ADC. The frequency of the signal being sampled is shown in the first column, and the maximum allowable jitter in femtoseconds in the remaining columns. As the table illustrates, the jitter constraints become more severe as the input frequency rises, raising issues of implementability.

Table 2.4: The maximum allowable jitter, in femtoseconds, when sampling an input signal at various frequencies to achieve various SNRs.

f_{in} [MHz]	80 dB SNR Maximum Jitter [fs]	14-bits or 86.08 dB SNR Maximum Jitter [fs]	16-bits or 98.08 dB SNR Maximum Jitter [fs]
1	15915	7940	1985
10	1592	794	199
20	796	397	99
40	398	198	50
60	265	132	33
80	199	99	25
100	159	79	20

2.6.1.2 I/Q Components of an RF Signal

A sinusoidal RF signal can be defined as

$$y(t) = A\sin(\omega t + \phi) \tag{2.11}$$

with

ω = the frequency in radians per second,
t = the time in seconds,
A = the amplitude of the signal and
ϕ = the phase of the signal in radians.

Eqn. 2.12 can be described in terms of its in-phase (I) and its quadrature (Q) components by using a trigonometric identity as

$$\begin{aligned} y(t) &= A\cos(\phi) \times \sin(\omega t) + A\sin(\phi) \times \cos(\omega t) \\ &= I \times \sin(\omega t) + Q \times \cos(\omega t) \end{aligned} \tag{2.12}$$

with

I = $A\cos(\phi)$ and
Q = $A\sin(\phi)$.

The amplitude can be defined in terms of the I and Q components as

$$A = \sqrt{I^2 + Q^2} \tag{2.13}$$

and the phase can be defined in terms of the I and Q components as

$$\phi = \arctan\left(\frac{Q}{I}\right) \tag{2.14}$$

A representation of a demodulator that implements I/Q demodulation to extract the amplitude and phase information of an RF signal is shown in Fig. 2.26. The RF signal is first multiplied by sine and cosine signals of the same frequency as the RF signal. The multiplication process results in baseband and higher frequency components. Low pass filters remove the high frequency components and the remaining baseband I/Q components can be used to extract the amplitude and phase through vector magnitude and arctan calculations. If the sine and cosine signals are chosen with a peak amplitude of 2 then the demodulated amplitude will be exactly the amplitude of the RF signal. If not, the demodulated amplitude will be proportional to the RF signal's amplitude.

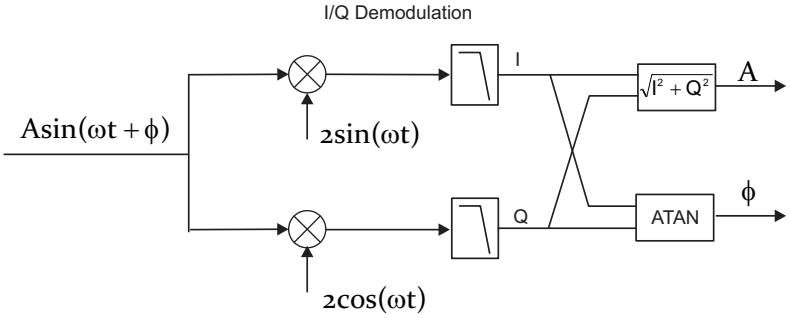

Figure 2.26: A schematic representation of an implementation of an I/Q demodulator and the vector magnitude and arctan function blocks to extract amplitude and phase information from the RF signal.

2.6.1.3 Modulation Techniques

In this section, amplitude and phase modulation techniques of RF signals as applied to LLRF systems are discussed. Schematic representations of possible techniques are illustrated in Fig. 2.27 and the descriptions and utilization are given below.

The first technique illustrated in Fig. 2.27 utilizes analog amplitude and phase modulators. The amplitude and phase reference inputs of the modulators are generated by DACs. This is a similar method to that used in the legacy control system, except that digital as opposed to analog control can be performed on the amplitude and phase of the RF signal (Ziemer and Tranter, 2006; Fong, 2007; Schilcher, 2008).

The second technique illustrated in Fig. 2.27 utilizes analog I/Q modulation. DACs drive the I/Q inputs of the mixers. The phase shifted RF reference is multiplied with the I/Q signals, summed and then band pass filtered. Optionally, the RF signal can be up-converted using an LO and mixer followed by a band pass filter to achieve a higher operating frequency. (Fong, 2007; Schilcher, 2008). As with the I/Q demodulation, the I/Q modulation can be implemented discretely. Integrated

circuits have been developed that implement the analog I/Q modulation, however, these devices do not operate in the required frequency band.

The third technique illustrated in Fig. 2.27 utilizes direct digital synthesis (DDS) integrated circuits to digitally synthesize the RF signal. These devices operate over a wide frequency range and allow the amplitude and phase to be modulated digitally. The highest amplitude resolution available is typically 14 bits. A detailed description of the DDS technique will be presented in Section 2.6.1.4.

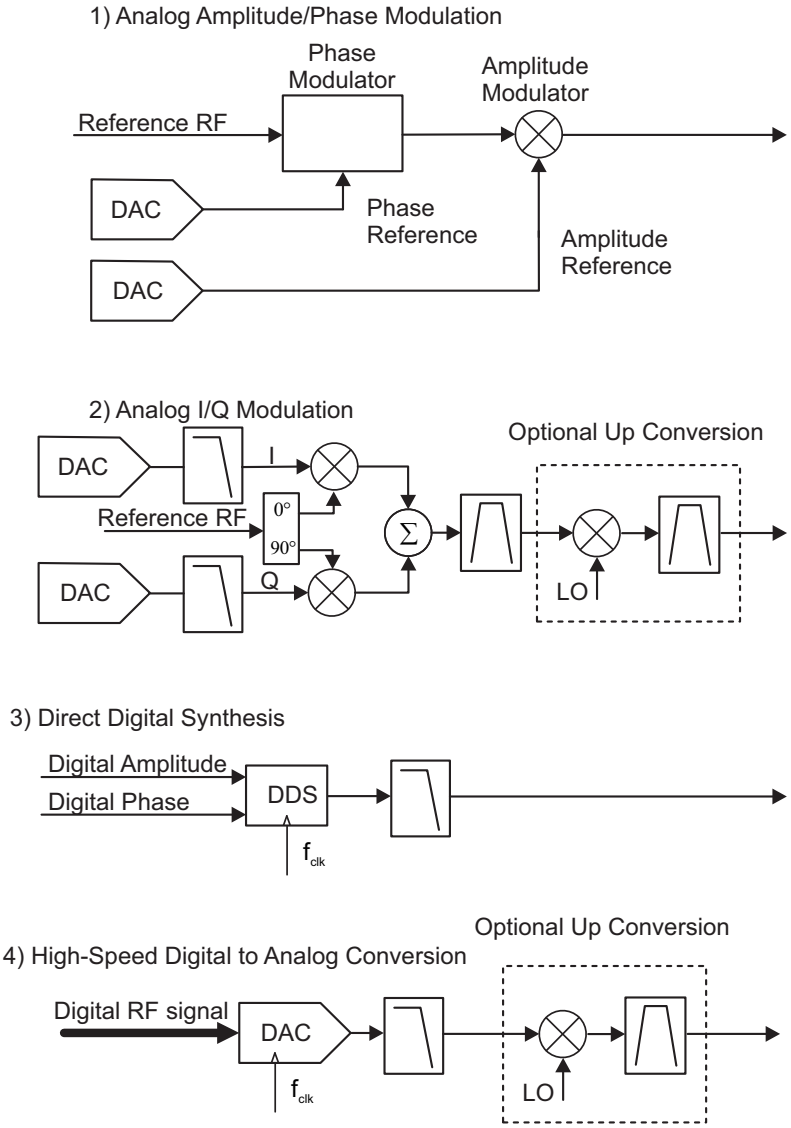

Figure 2.27: The modulation techniques that can be implemented to modulate the amplitude and phase information of an RF signal in a LLRF system.

The fourth technique illustrated in Fig. 2.27 utilizes high-speed DACs to convert a digital representation of the RF signal to an analog RF signal (Fong, 2007;

Schilcher, 2008). A low-pass filter performs anti-aliasing on the reconstructed signal. Optionally, the RF signal can be up-converted using an LO and mixer followed by a band pass filter to achieve a higher operating frequency. The 2-81 MHz operating frequency band of the RF systems at iThemba LABS falls well within the capabilities of modern high-speed 16-bit DACs. Therefore the up-conversion is not necessary and it is possible to implement a customized version of the DDS and perform direct conversion of the RF signal, thereby achieving a higher amplitude resolution than commercially available DDS integrated devices.

2.6.1.4 Direct Digital Synthesis

An RF signal can either be digitally synthesized with commercially available direct digital synthesis (DDS) integrated circuit devices or within the FPGA using parameterizable DDS techniques. A block diagram of a conventional DDS implementation is shown in Fig. 2.28, depicting the major components such as the phase accumulator, phase offset adder, cosine function and the multiplier on the output to set the amplitude. The bus-widths at the various stages are denoted by the letters A, B, C and D. The output frequency is defined by $f_o = f_s \times FTW/2^A$, with $FTW \leq 2^A - 1$ and A a positive integer.

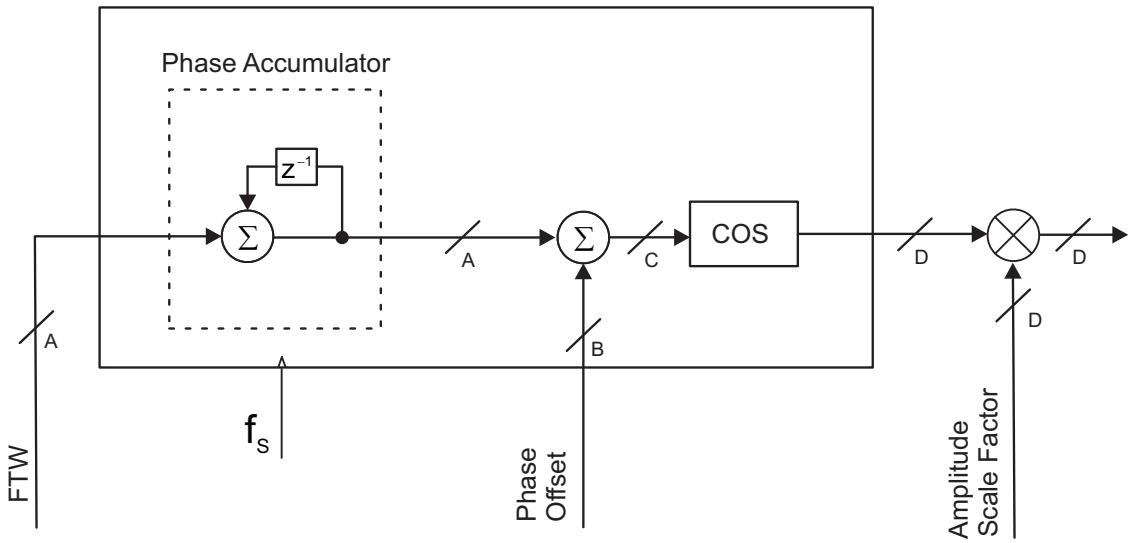

Figure 2.28: A block diagram of the conventional implementation of a DDS.

In essence, the phase accumulator consists of an unsigned counter with a bit width of A, clocked at a frequency of f_s and incremented at each rising clock edge by the value of the frequency tuning word (FTW). The phase accumulator's count value is a digital representation of a value between 0 and 2π radians where 0 is equivalent to $0\times\pi$ and 2^A is equivalent to $2\times\pi$. The output value of the accumulator is summed with the phase offset using a bus width B. The result is truncated to a bus width C and input to the cosine function. The truncation is applied to make the implementation of the cosine function block (Section 2.6.1.5) realizable using

practical hardware. A multiplier on the output of the cosine function performs amplitude modulation of the synthesized signal. The bus width D has a direct impact on the achievable amplitude resolution.

Conventionally, such DDS systems implement a frequency tuning word (FTW) of between 24 and 48 bits, the most common being 32 bits. With A=32, the output frequency is then defined as: $f_o = f_s \times FTW/2^{32}$, with $FTW \leq 2^{32} - 1$.

Since the synthesized frequency will be an integer multiple of $f_s/2^{32}$, it is in general not possible to produce precisely the desired frequency. For example, for a sampling frequency $f_s = 120$ MHz, the output frequency f_o will be an integer multiple of $120 \times 10^6/2^{32} = 0.00279396772384643554 6875$ Hz.

For a closed-loop system, such as the LLRF control system designed in this thesis, this rounding error poses a problem in the down conversion process, because the RF, LO, and IF signals, as well as the sine and cosine look-up tables (LUTs) that are implemented in the I/Q demodulators within the FPGA, must maintain a rational relationship between one another to prevent the phase between the signals drifting in time. We have overcome this problem by modifying the phase accumulator portion of the DDS technique to allow the system to synthesize RF signals in integer multiples of 1 µHz. This is described in Section 3.4.1.

2.6.1.5 Efficient Sine, Cosine and Arctan Calculation

When implementing DDS and I/Q techniques with FPGA systems it is necessary to perform angle to amplitude calculations in the form of Eqn. 2.15 and vector to angle calculations in the form of Eqn 2.16.

$$\text{amplitude} = \cos(\text{angle}) \tag{2.15}$$

$$\text{angle} = \arctan(\frac{Q}{I}) \tag{2.16}$$

with

I = the in-phase component and
Q = the quadrature component.

One possible way to implement Eqn. 2.15 is to use a look-up table (LUT). In a DDS implementation with an angle resolution of 32 bits and an amplitude resolution of 16 bits, then a LUT of 8GB is needed, which is impractical and currently not feasible. An efficient method that implements a coordinate rotational digital computer (CORDIC) algorithm (Xilinx, 2011; Volder, 1959) can be implemented in a FPGA to perform both Eqns. 2.15 and 2.16. The intellectual property (IP) core is highly parametrizable and can be configured to achieve single cycle data throughput in a fully parallel configuration at the expense of FPGA resource utilization and multiple-cycle throughput in a word serial implementation with minimal resource utilization.

The use of a LUT is feasible in a scenario where the input frequency is a rational ratio of the sampling frequency. For example, if a 1 MHz IF is sampled by a 10 MHz ADC then only two LUTs of 10 samples each are needed to implement the digital sine/cosine signals needed to perform I/Q demodulation of the 1 MHz IF. This is illustrated graphically in Fig. 2.29, with the samples of a 16-bit sine LUT shown in the top graph and the samples of a 16-bit cosine LUT shown in the bottom graph. In each case only samples 0-9 are used to implement the LUT. Sample 10 is included to emphasize the periodicity of the LUTs.

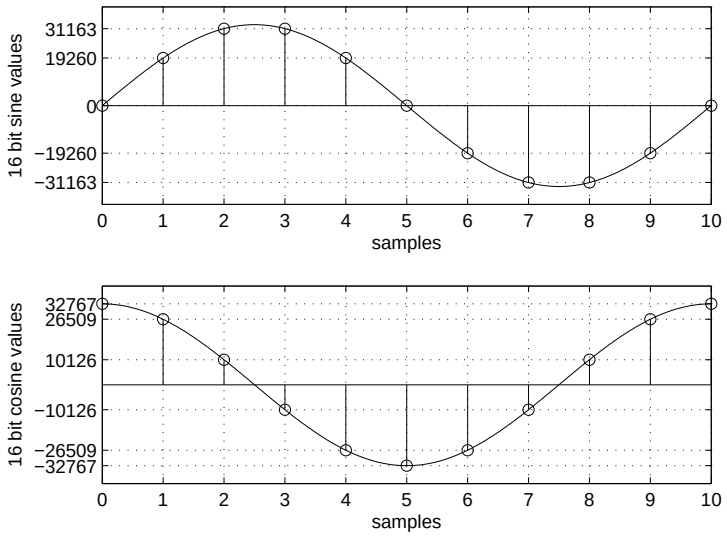

Figure 2.29: A graphical representation of the 10 values needed for a 16-bit sine and cosine LUT when $f_S = 10f$.

2.6.2 Review of Cyclotron LLRF Systems

In this section a review is given of modern LLRF control systems for cyclotron particle accelerators as described in the literature to highlight the stability achieved and the progress made in implementing the techniques and components described in the previous section.

Caruso *et al.* (2007) developed a DLLRF system for their cyclotrons utilizing DDS. Their approach used ADCs to sample the analog amplitude and phase signals and then to perform digital control of the amplitude and phase of the RF output signal by manipulating the DDS' internal amplitude and phase registers. This approach achieved a phase stability of 0.1°.

Huang *et al.* (2011) present a design that uses a 10-bit 400 MHz DDS, microcontroller, RF to DC amplitude detector, variable gain amplifier, and analog phase detector integrated circuits for a cyclotron that operates with 12 KW power at 101 MHz.

Gold and Sabaiduc (2013) describe a digital low level RF control system for medical cyclotrons that uses a FPGA interfaced with 14-bit DACs that drive an external I/Q modulator to synthesize an RF signal between 49 and 80 MHz. The RF pick-up signals are demodulated with an external I/Q demodulator and the I/Q signals are sampled using 14-bit ADCs. The system was successfully commissioned on a single resonator cyclotron and achieved an amplitude stability of 0.05%.

Yin *et al.* (2016, 2015) developed a LLRF control system for a 100 MeV 44.8125 MHz fixed frequency cyclotron. Their approach used multiple DDS integrated circuits, analog amplitude and phase detection and analog amplitude and phase modulation controlled by a DSP processor. They achieved an amplitude and phase stability of 0.1% and 0.03°.

Although there has been some progress in implementing modern digital cyclotron LLRF control systems, no designs exist that can cover the wide frequency band of operation as needed at iThemba LABS. Furthermore, none of the systems described have been able to reach the target peak-peak amplitude and phase stability of 1/10000 and 0.01°. The information available points to designs that implement analog techniques to extract amplitude and phase information or that utilize analog I/Q demodulation and modulation techniques as well as the implementation of commercially available DDS integrated devices.

Aside from cyclotron LLRF control systems, significant progress has been made in the design of modern LLRF control systems for linac accelerators and a review thereof as described in the literature is discussed in the next section.

2.6.3 Review of Linac LLRF systems

In this section, a review is given of modern LLRF control systems for linac particle accelerators as described in the literature. Although the RF systems of a linac accelerator typically operate in pulsed mode and at high frequencies, in contrast to the continuous-wave and lower frequencies used for cyclotrons, modern linac systems implement the same techniques described in the previous sections. Only those designs most applicable to the design of modern cyclotron LLRF control systems are discussed.

Matsumoto *et al.* (2009) developed a DLLRF system for the Superconducting RF Test Facility (STF) at the High Energy Accelerator Research Organization (KEK) in Japan. They used a FPGA with 14-bit DACs that drive I/Q modulators for modulation of the main RF signal at 1300 MHz. They also used multiple feedback channels. The sampling of these multiple feedback channels is simplified by use of a down conversion approach with 4 intermediate frequencies that are combined and sampled by a 16-bit ADC at 40.65 MHz. The system is able to achieve an amplitude and phase stability of 0.03% (RMS) and 0.02° (RMS) respectively.

Qiu *et al.* (2014) developed a DLLRF system for the compact Energy Recovery Linac (cERL) also at KEK. The system uses a FPGA interfaced with 16-bit DACs that perform I/Q modulation using an external modulator at 1300MHz. The system performs down conversion of pick-up signals to a 10 MHz IF which is sampled with 16-bit ADCs. The system is able to achieve an amplitude and phase stability of 0.012% (RMS) and 0.015 ° (RMS) respectively.

Kim *et al.* (2007) developed a DLLRF system for the proton linear accelerator as part of the Proton Engineering Frontier Project (PEFP). The system used 14-bit DACs to drive an I/Q modulator that modulates a 350 MHz reference signal. The system performs down conversion of the pick-up signal to a 10 MHz IF which is sampled by 14-bit ADCs.

Liepe *et al.* (2003, 2005) describe a DLLRF system for an electron recovery linac. The system uses 16-bit DACs to drive an I/Q modulator that modulates a 499.766 MHz reference signal. The system performs down conversion of the pick-up signal to a 11.9 MHz IF which is sampled by 14-bit ADCs. The system can achieve an amplitude and phase stability of 10^{-4} (RMS) and 0.02° (RMS) respectively.

The LLRF systems reviewed above demonstrate that significant progress has been made in linac DLLRF control system design, more so than with respect to cyclotron systems. However, the high linac operating frequencies require the use of analog I/Q modulators and those designs using 16-bit high-speed DACs to drive the I/Q modulators almost achieve the 1/10000 amplitude stability. Down conversion to an acceptable IF is usual as this overcomes the jitter constraints on the ADCs.

In summary, the limited information available on modern cyclotron LLRF systems coupled with the information available for linac accelerator LLRF systems demonstrates that there is substantial room for improvement in the design of a modern wide band digital LLRF control system for the cyclotron particle accelerators at iThemba LABS. In particular, with the advances made with high-speed 16-bit DACs, direct digital synthesis (DDS) of the RF signal could be performed within an FPGA, thereby allowing the optimization of the DDS techniques and overcoming the frequency, amplitude and phase resolution limitations of current commercially available DDS integrated circuit devices. Furthermore, with the correct choice of IF and low-latency 16-bit ADCs, a high resolution I/Q demodulator could be implemented within the FPGA, thereby allowing high-speed digital real-time control of the amplitude and phase of the RF signals and the achievement of an amplitude and phase stability greater than that which has been possible before.

2.7 Conclusion

This chapter has reviewed the theory of operation of a cyclotron particle accelerator and has provided an overview of the facilities at iThemba LABS. Specifically, the RF systems of the K=8 and K=10 injector cyclotrons (SPC1, and SPC2) and their inter-operation with the RF systems of the K=200 separated sector cyclotron (SSC), AX, J, and K-line RF bunchers and the pulse-selector RF system were discussed in detail.

A detailed description was also given of the legacy RF control system and its operation and limitations described. A description was also given of the facilities at the Helmholtz-Zentrum Berlin, because the system designed in this thesis has also been incorporated into this K=132 separated sector cyclotron.

A theoretical review of the effects of RF dee voltage stability on isochronous cyclotron performance highlighted the influence of amplitude and phase instability

on the energy spread of an isochronous cyclotron with and without a flat-topping system.

Finally, a literature review of the current state-of-the-art regarding digital control of cyclotron RF systems was presented. The advances in demodulation, modulation, and DSP techniques applicable to modern digital low-level RF control systems were discussed. It was demonstrated that there is significant room for improvement in current designs, and that higher performance of the cyclotron particle accelerators at iThemba LABS can be achieved by a more modern wide-band digital LLRF control system. In particular, the advances made with high-speed 16-bit DACs allow direct digital synthesis (DDS) of the RF signal to be performed within an FPGA, thus allowing the optimization of the DDS techniques in order to improve on the frequency, amplitude and phase resolution limitations of commercially available DDS integrated circuit devices.

Furthermore, with the correct choice of IF and low-latency 16-bit ADCs, a high resolution I/Q demodulator can be implemented digitally within the FPGA allowing high-speed digital real-time control of the amplitude and phase of the RF signals and the achievement of an amplitude and phase stability greater than that which has been obtained before.

As no modern LLRF system compatible with the facilities at iThemba LABS is currently available, this sets the rationale for the design of the system that is discussed in the following chapter.

Chapter 3

System Design

This chapter describes in detail the design of the new digital low-level RF (DLLRF) control system for the cyclotron particle accelerators at iThemba LABS. The philosophy and methodology of design is considered first and is based on the techniques presented in Section 2.6. This is followed by an overview of the production system and by detailed descriptions of all the developed hardware system modules, the software architecture, real-time control and DSP techniques implemented within the FPGA.

Finally, the implementation of the RF control systems on the K=8 and K=10 injector cyclotrons (SPC1, and SPC2), the K=200 separated sector cyclotron (SSC), the AX, J, and K-line RF bunchers and the pulse-selector system at iThemba LABS, as well as on the K=132 separated sector cyclotron at the Helmholtz-Zentrum Berlin (HZB) is discussed.

3.1 Overview of Design Process

In Section 2.6 the techniques and ideas that can be used to design a modern digital LLRF control system were presented. This forms a platform and starting point for the design of a system to achieve a closed-loop peak-peak amplitude and phase stability of 0.01% and 0.01° respectively over an operating frequency range of 2 to 81 MHz to replace and upgrade the legacy analog control systems at iThemba LABS.

This operating frequency range falls well within the capabilities of modern high-speed 16-bit DACs. By using direct conversion of the RF signals, the proposed design eliminates the need for external up conversion and the need for external analog I/Q modulators. Optimization of the direct digital synthesis (DDS) method used to synthesize RF and LO signals for down conversion of the RF pick-up to a suitable IF allowed the jitter constraints of the ADCs as discussed in Section 2.6.1 to be overcome. The IF signals were sampled by ADCs after which I/Q demodulation was digitally performed within the FPGA.

Initially, a 24 bit 48 kHz ADC was chosen, operating with a sampling clock of 46.75 kHz that sampled an IF of 15.625 kHz. Unforeseen 32 sample latency introduced by a finite impulse response (FIR) filter within the ADCs was detrimental

to the closed-loop performance of this initial prototype as the 300 Hz residual noise components from the high voltage supplies in the RF amplifiers on SPC2 needed to be suppressed by a further 10 dB under closed-loop control to achieve the design specification. Nevertheless, this prototype proved an excellent platform to develop the DSP techniques within the FPGA to implement I/Q demodulation and real-time control of the amplitude and phase of the RF signals.

For the final prototype, an IF of 1 MHz was chosen and sampled by 16-bit successive approximation register (SAR) ADCs with a single sample latency at 10 MHz. The design was also modularized to allow system maintainability and to allow possible future upgrades to portions of the design.

Three of the final prototype systems were manufactured. One system served as a synthesizer and the other 2 systems were implemented and qualified on SPC2 north and south RF resonator systems. The change in IF and ADCs proved successful and the systems worked extremely well and met the design specifications. These final prototypes also provided a platform to develop sequencing code to fully automate the system.

After a satisfactory qualification period, the decision was made to manufacture 35 production systems. This would provide a sufficient number of units to replace the legacy control systems at iThemba LABS, to ensure enough spare parts for the foreseeable future and to meet commitments in international collaborations.

The manufacturing process of the production versions was successful and the next section provides an overview of the production system followed by detailed descriptions of all the hardware system modules, the software architecture, real-time control and DSP techniques implemented within the FPGA.

3.2 Production System Overview

A photograph of the production version of the RF control system designed in this thesis is shown in Fig. 3.1. The system has a modular design with each module performing a specific function, for example RF control, RF synthesis, IF sampling, RF amplification and mixing, and input/output interlocking.

All RF signals in the design are accessible through sub-miniature version A (SMA) links on the front panels, giving the user quick access for diagnostic purposes. The 10 MHz reference signal is available on the far left panel, the main RF and LO signals are available from the RF synthesizer module, the 5 IF signals and the RF output are available from the RF amplification and mixing module and finally, the resonator or RF pick-up, the RF phase reference, auto-tune (ATU) pick-up and two auxiliary RF signals are available on the far right panel. The RF signals on the far right and left connect through to N-type connectors on the rear of the system.

The status LEDs on all the modules provide first line diagnostic ability. The functionality thereof is detailed in later chapters.

The rear of the system, shown in Fig. 3.2, provides N-Type connections for the RF power amplifier input, resonator or RF pick-up, RF reference, auto-tune (ATU) pick-up and two auxiliary RF signals on the far left panel and the 10 MHz

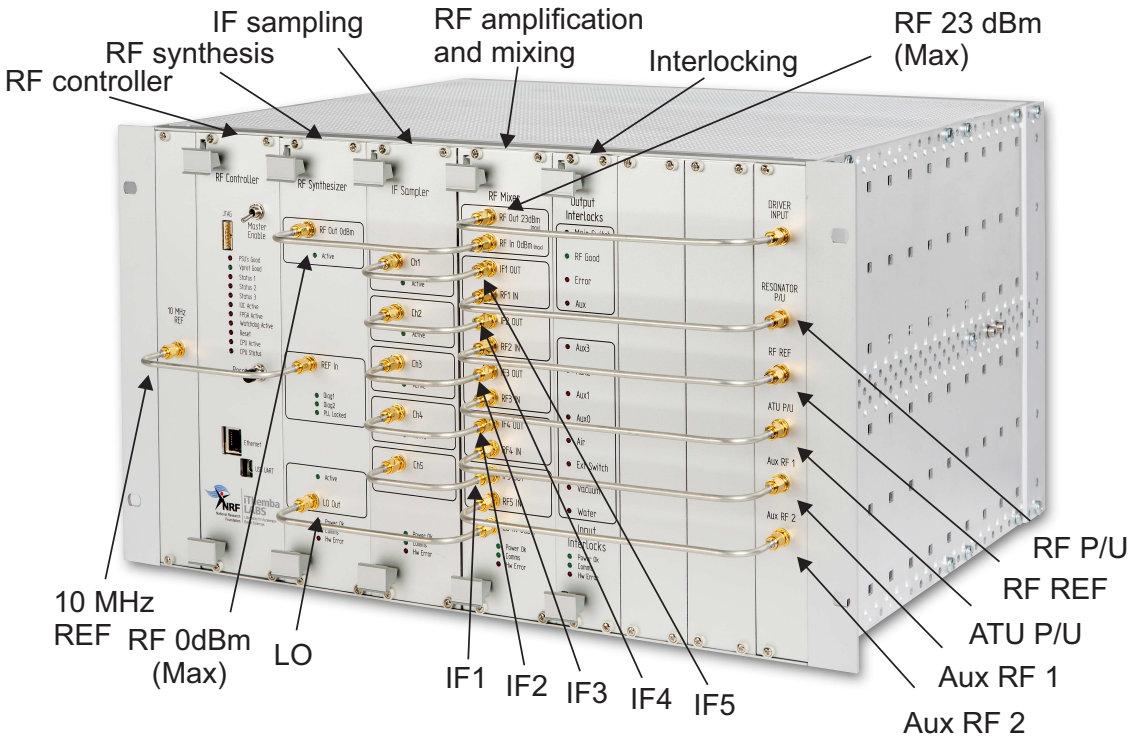

Figure 3.1: A photograph of the new digital low-level RF control system showing the RF controller, RF synthesizer , IF sampling, RF amplification and mixing, and the interlocking system modules, as well as the 10 MHz reference, local oscillator (LO), RF signals, the 5 IF channels, the resonator or RF pick-up, RF reference, auto-tune (ATU) pick-up and two auxiliary RF signals.

Figure 3.2: A photograph of the rear of the new digital low-level RF control system showing connections for the 10 MHz reference, RF output, the resonator or RF pick-up, RF reference, auto-tune (ATU) pick-up, two auxiliary RF signals, auxiliary I/O expansion, input and output interlocks as well as the power inlet and fuse holder.

Figure 3.3: The complete system showing removed modules as well as access to internal power supplies.

reference input signal on the far right. Further connections are provided for the input and output interlock signals, the auxiliary I/O expansion interface on the far left panel and a power inlet and fuse holder is provided on the right panel.

The system is designed for maintainability. All of the modules can be quickly removed and replaced without making any hardware adjustments as is illustrated in Fig. 3.3. The rear centre panel can also be quickly removed to service the internal power supplies.

A high-level block diagram of the system is shown in Fig. 3.4. The system

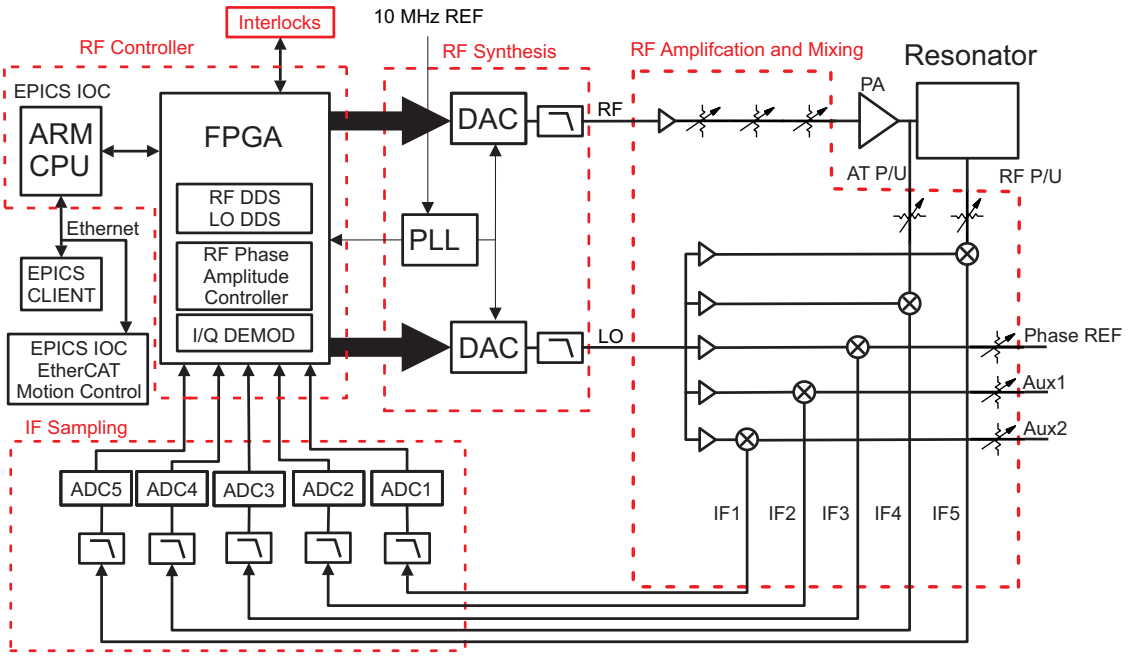

Figure 3.4: A block diagram of the new digital low-level RF control system.

modules as illustrated in Fig. 3.1 are indicated by the red dotted lines on this block diagram. The signals between these modules correspond to the SMA-links or digital signals on the backplane. The parts of the system not enclosed in dotted lines, such as the RF power amplifier (PA), the resonator, the EPICS client and the EPICS EtherCAT motion control IOC, are external to the RF control system.

The following sections describe the design and operation of the RF control system.

3.3 RF Controller Module

The RF controller module is the main control module of the system. It houses a 32-bit ARM CPU that runs Linux and EPICS as well as the FPGA that performs real-time and digital signal processing functions such as closed-loop amplitude and phase control, direct digital synthesis (DDS) of the main RF and LO signals, in-phase and quadrature (I/Q) demodulation of the IF channels and safety interlocking.

The module corresponds to the RF controller section highlighted in Fig. 3.4. A photograph of the module is shown in Fig. 3.5 depicting the major components of the design, such as the PCB, FPGA, ARM processor board, power supplies, high density back plane interface and the connectivity and status LEDs on the front panel.

The RF controller module is the most complex of the modules in the RF control system. The detailed schematics, the bill of materials (BOM) and a multilayer print of the PCB design are shown in Appendix B.1. The PCB has 12 layers, which include 8 routing layers, 3 power planes and 1 ground plane. The PCB trace

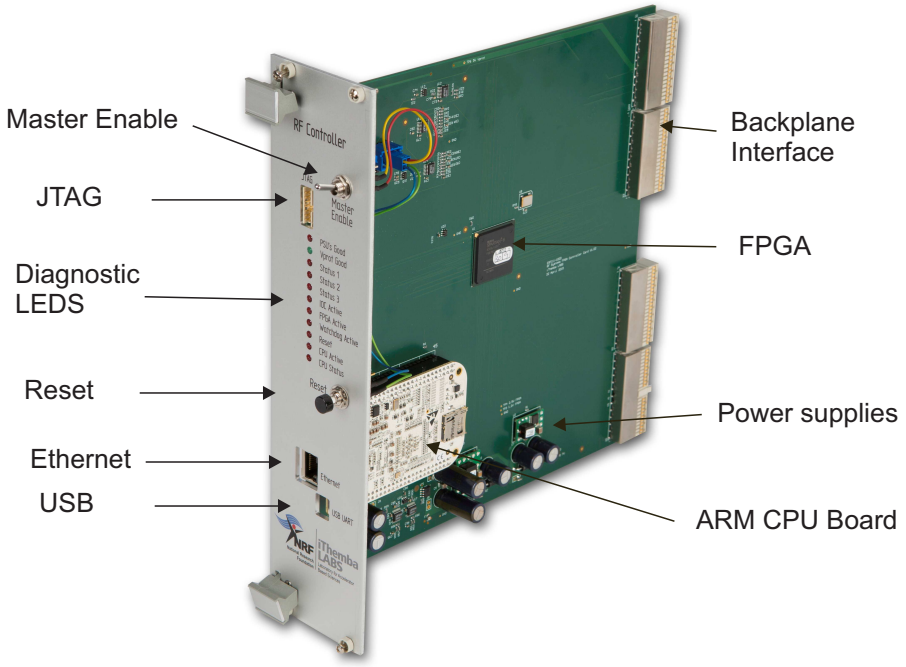

Figure 3.5: A photograph of the RF controller module indicating major components.

separation tolerance is 127 µm. The high layer count and 127 µm trace separation were necessary to route all the signal pins to and from the 676 pin ball-grid array (BGA) FPGA.

Most of the signals in the design are treated as high-speed digital signals with a single-ended or a differential impedance of 50 or 100 Ohms with a maximum data and clock rate of 300 MHz.

The philosophy of design was to route the FPGA signals via the backplane to each of the system modules. No high-speed digital signals are multiplexed and all high-speed digital buses are impedance and length matched to ensure signal integrity and synchronous point-point data transfer. The point to point routing philosophy prevents bus contention problems between the system modules and the FPGA and ensures synchronous unbuffered real-time data transfer.

The RF controller module uses a commercially available CPU board with an 800 MHz 32 bit ARM processor with 1GB of RAM. The Ethernet and USB port are accessible on the front panel as is illustrated in Fig. 3.5 and provide connectivity to the LAN as well as the diagnostic features of the processor.

The processor board is configured to run Linux and an EPICS IOC. An EPICS ASYN driver and corresponding EPICS record database was written to communicate with the FPGA's memory mapped registers via the CPU's 16-bit bi-directional data and 10-bit address bus. There are a total of 205 16-bit memory mapped registers in the FPGA, a complete map of which is illustrated in Table C.1 in Appendix C. When multiple 16-bit registers are needed to create a larger register, the data must first be written to the lower-order register. Once the higher-order register is written to, the larger buffered register is updated.

All real-time control occurs within the FPGA. There is minimal record structure logic within the EPICS IOC's RF controller database. The records are processed sequentially and essentially only provide a means to read and write from the FPGA via EPICS channel access from the EPICS client by the user or by the higher level automation and sequencing code. The EPICS record processing is considered as a slow process with a maximum scan rate of 10 Hz. EPICS waveform records read data from memory mapped FIFO buffers in the FPGA. Typically, the FIFO data is transfered in 256 element data blocks at a scan rate of 10 Hz, allowing amplitude and phase information waveforms to be displayed on the user's client GUI at a 2.5 kHz sample rate.

3.3.1 Cold Boot Configuration

The following describes the system configuration that occurs when a cold boot is performed.

First, the FPGA firmware image is programmed from the CPU via the serial peripheral interface (SPI). Once the firmware is in place, LEDs on the front panel indicate that the FPGA is configured and active. The FPGA has multiple clock input signals. A 100 MHz oscillator on the RF controller module drives the memory mapped interface and other supervisory circuits in the FPGA. This allows communication and configuration of the memory mapped registers to occur independently of the off-board clock inputs from the RF synthesizer module that are synchronized in time with the 10 MHz reference signal.

Next, a purposely designed SPI chip select multiplexing register in the FPGA is then programmed to multiplex the SPI interface of the CPU to the phase-locked loop (PLL), the high-speed DACs and the various system modules. The PLL on the RF synthesizer module is initially configured to output the clock signals to the high-speed DACs and the FPGA. Once this is done, then the DACs are programmed for the correct mode of operation. At each stage, the status LEDS on the front panel are updated, allowing the user to determine whether the programming of the PLL or one of the DACs has failed. For example, if the 10 MHz reference is lost, then the DACs may fail to program and calibrate properly due to a clock signal failure. The configuration routine will halt and the corresponding status LEDs will indicate where the initialization process has failed.

3.3.2 Warm Boot Configuration

For a warm boot, the configuration routine will detect that the FPGA, the PLLs and the DACs are already programmed and will then skip the steps described in the previous section. The skipping of these steps, is relevant when modifying and debugging the EPICS IOC code, as reinitializing the PLL and DACs' clock interface will lead to a random phase initialization of the RF and LO DDS with respect to the RF reference signal, requiring a power on reset configuration of the EPICS sequencer program in order to resynchronize the RF control system.

In general, the system is booted once from a cold start and is then kept in operation until a maintenance shut-down is performed. After the system has detected

that the FPGA, PLLs and DACs are configured, the EPICS IOC is started. The EPICS IOC initialization routine first loads the EPICS Asyn driver and then the previously saved Autosave values of the EPICS database records. The database initialization routine is then triggered, causing the retrieved values to be written to the memory mapped registers of the FPGA. If, for example, a warm start was performed, then from the FPGA's perspective the system would appear to have that same configuration data in memory. This allows simple testing and modification of the IOC code without requiring the reconfiguration of the complete system.

As a safety feature, the EPICS IOC has a watchdog routine that must service a register in the FPGA within a certain time interval. If this does not occur, the interlocking logic within the FPGA prevents the RF signal from being synthesized. The only way that this latched interlock signal can subsequently be cleared is by the sequencer program. This is a safety measure which requires that the IOC must be active and all EPICS process variables must be live and connected through EPICS channel access (CA) before the sequencer program can run. In this way, unstable software that causes a system crash or Linux kernel panic cannot cause unpredictable behavior of the RF control system, since in these situations the RF output signal will be safely interlocked.

After the databases have been initialized, the EPICS sequencer is started. As previously mentioned, the prerequisite for the sequencer to run is that all the EPICS process variables are connected through the EPICS channel access (CA). Furthermore since EPICS is a distributed control system, multiple IOCs can communicate with each other via CA. This principle is used to extend the IO and motion control capability of the RF control system. In particular, the auto-tune control, resonance search and prepositioning of the trimmer capacitor occur via CA to the EPICS EtherCAT motion control IOC. If communication with the EtherCAT IOC is lost, a soft watchdog in the IOC will time-out and interlock the RF output signal. The system can only resume operation and clear the interlock of the watchdog once CA to the EtherCAT IOC and sequencer is re-established.

3.3.3 Real-time Control, Direct Digital Synthesis and I/Q Demodulation within the FPGA

The FPGA performs real-time closed loop control, direct digital synthesis (DDS) of the RF and LO signals and I/Q demodulation of the digitized IF channels. A more detailed block diagram of the FPGA portion of Fig. 3.4 is illustrated in Fig. 3.6. The block diagram is a high level representation of the internal VHDL based modules of the FPGA and a description of the modules is given below.

The 5 IF channels are sampled with 16-bit 10 MHz ADCs on the IF sampling module. The data is transmitted serially with a clock rate of 300 MHz using low-voltage differential signaling to the FPGA via the backplane. The 5 1-bit serial data streams are received in the FPGA and converted to 5 separate 16-bit parallel data streams. FIFO buffers are used to store 1024 samples of the raw ADC data and are accessible via the memory mapped interface.

The design utilizes two DSP processing paths. The first is for high data rate de-

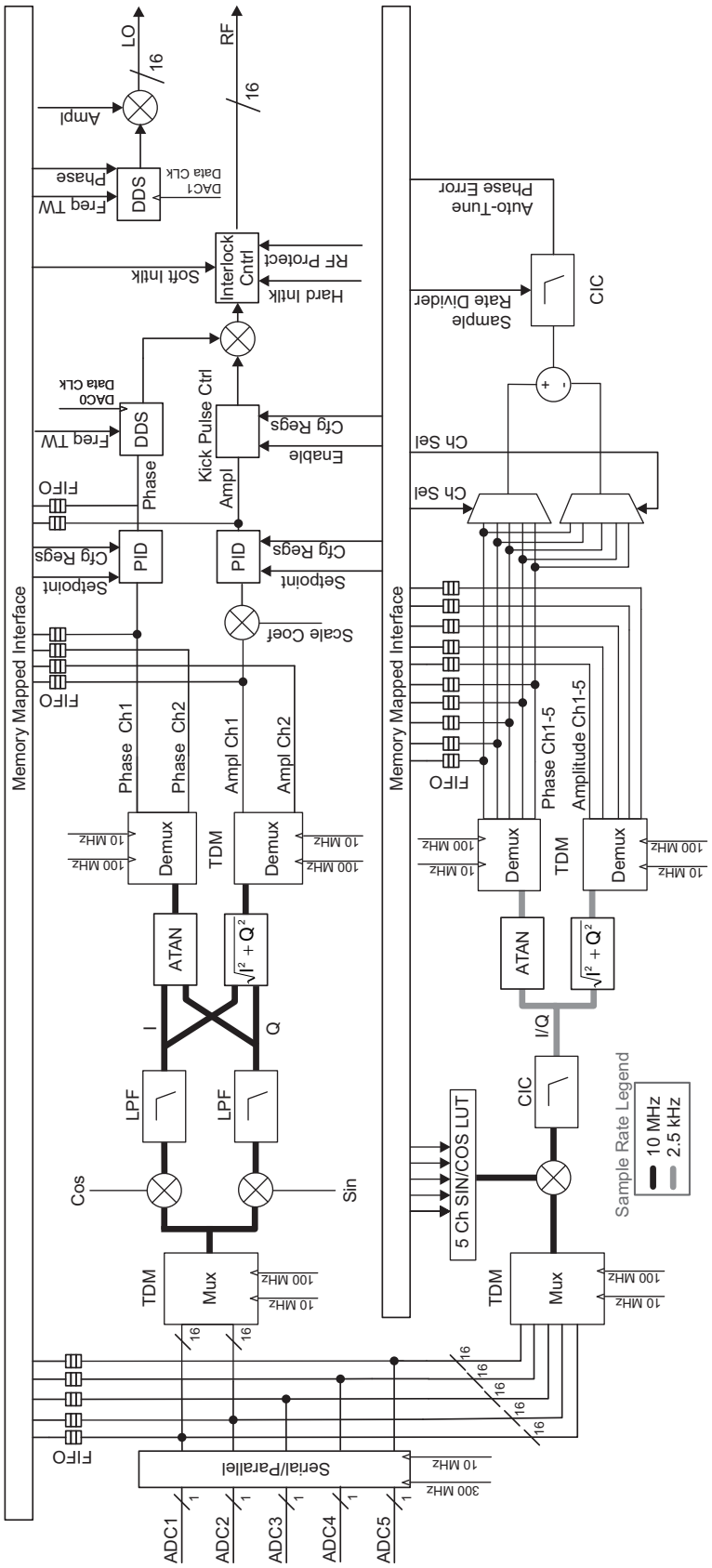

Figure 3.6: A high level block diagram of the real-time control, DDS, and I/Q demodulation implemented in the FPGA.

modulation and low-latency real-time control and modulation of the RF signal, and the second is for low data rate demodulation and higher latency for transmission of amplitude and phase information to the network and for slow process control of the auto-tune trimmer. This configuration allows for the optimal resource utilization within the FPGA.

The following sections describe the high speed DSP data path and the low speed data path respectively.

3.3.3.1 High-speed, Low-latency DSP Data Path

To achieve high data throughput, efficient resource utilization and low latency, a time division multiplexing (TDM) scheme is used. The first two ADC channels, which carry the resonator pick-up and the RF reference signals respectively, are interleaved. This allows efficient resource utilization to occur as the DSP block within each function can be utilized to process both channels. Furthermore, the DSP blocks operate in pipelined mode with a clock rate of 100 MHz allowing each DSP block to complete processing within the sample period of each 10 MHz channel.

The TDM stream is first multiplied with quantized 1 MHz cosine and sine values that are derived from look-up tables. The multiplication process translates the 1 MHz IF data stream to baseband. Finite-impulse response (FIR) low-pass filters remove the high frequency components resulting from the multiplication process. These filtered data streams are the in-phase (I) and quadrature (Q) data. The phase information is extracted by calculating the arc-tangent of the I/Q data streams and the amplitude information is extracted by calculating the vector magnitude of the I/Q data streams. The TDM amplitude and phase data are then demultiplexed. For the raw ADC data, FIFO buffers are used to store 1024 samples of the amplitude and phase values and are accessible via the memory mapped interface.

The demodulated phase angle derived from the RF pick-up signal is then passed to the phase proportional, integral and differential (PID) controller. The set point of the PID controller and configuration registers that modify the PID coefficients are accessible through the memory mapped interface.

Similarly, the demodulated amplitude derived from the RF pick-up signal is passed to the amplitude PID controller. A multiplier first scales the amplitude. This allows for compensation of a mismatch between set point and the demodulated amplitude of the RF pick-up signal. As with the phase PID controller, the amplitude PID set point and configuration registers are accessible via the memory mapped interface.

The phase and amplitude PID outputs are available via FIFO buffers to the memory mapped interface. The phase PID output modulates the phase by updating the phase-offset register within the DDS. The DDS implementation is discussed in Section 3.4.1.

The amplitude PID output is connected to the kick pulse control module. The kick pulse control module allows open-loop amplitude modulation for a short period of the RF signal during the switch-on phase in order to break through the RF multipacting as described in Section 3.10. The amplitude and duration of the kick pulse are modifiable through the memory mapped interface.

The output of the kick pulse module modulates the amplitude of the synthesized RF signal from the DDS. The modulated signal is then passed through the interlocking control module that disables the RF signal output when required by the interlock logic.

The same implementation of the DDS is used to synthesize the LO signal, except that the phase and amplitude of the LO signal are set via the memory mapped interface.

Finally the high-speed 16-bit data representing the RF and LO signals are streamed synchronously via the backplane to the synthesizer module for analog reconstruction.

3.3.3.2 Lower-speed, higher-latency DSP Data Path

A high data throughput, low-latency DSP path is only necessary for the real-time control of the amplitude and phase of the main RF signal as described in the previous section.

To demodulate the remaining channels and to make available the amplitude and phase at a lower data rate to the EPICS clients, a lower-speed, higher-latency DSP data path that optimizes the FPGA resources is used and is described below.

A time division multiplexing (TDM) scheme is used to interleave all 5 ADC channels, allowing efficient resource utilization to occur as the DSP blocks within each function can be utilized to process all 5 channels simultaneously.

A single multiplier DSP is used to multiply the 5 sine/cosine LUTs outputs with incoming ADC channels to translate the IF to baseband. The sine/cosine LUTs are modifiable via the memory mapped interface. By modifying the phase of the sine/cosine LUT, the phase offset of the demodulated phase angle can be altered. Thereafter, a 5 channel cascaded integrator-comb (CIC) filter is used to low-pass filter and down-sample the data to achieve a data rate of 2.5 kHz for the derived I/Q data stream. The arc-tangent and vector magnitude function modules extract the amplitude and phase from the I/Q samples. These functions are highly optimized to use minimal resources by performing the calculations sequentially in a serial architecture as the data rate is much lower than the module clock speed as opposed to the highly pipelined low-latency implementation in the previous section.

The amplitude and phase samples of all 5 channels are de-multiplexed and are accessible from the memory mapped interface via 256 sample depth FIFO buffers.

Any of the five channels' phase information can be selected to calculate the auto-tune phase error. The selection is modifiable via the memory mapped interface. The default is to subtract the RF pick-up phase from the trimmer capacitor's auto-tune pick-up. This error signal can be down-sampled up to 256 times using a CIC filter. It is necessary to down-sample the error signal as the auto-tune pick-up is a phase shifted version of the phase PID controller's output. Depending on the system, the fluctuation can be large, and a highly smoothed error stream is required to control the trimmer capacitor and prevent it from oscillating about its set point. Finally, this auto-tune phase error is available to EPICS via the memory mapped interface.

3.3.3.3 Real-time Control Performance

The performance of the real-time control of the systems was measured in two separate experiments by connecting an amplitude or a phase modulator in-line with the RF output of the control system. This modulated signal is then split, with one leg of the splitter connected to the RF pick-up signal and the other leg to the spectrum analyzer. This allows the loop to be closed and the disturbance rejection capability of the RF control system at a specific offset from the carrier can be viewed with the PID coefficients of the amplitude and phase controllers set to the maximum stable values.

A sinusoidal waveform generator is then connected to the specific modulator. The amplitude of the waveform generator is set to produce a side lobe of -30 dBc in open loop mode at a specific frequency offset from the carrier. The frequency of the waveform generator was then stepped from 2.5 Hz to 20 kHz. At each stage the amplitude of the side lobes below the carrier was recorded in open and closed-loop modes. The disturbance rejection can then be calculated from the difference in the side lobe amplitudes in open loop and closed loop modes. The graphs shown in Fig. 3.7 and Fig. 3.8 illustrate the amplitude and phase disturbance rejection with a synthesized RF frequency of 22 MHz.

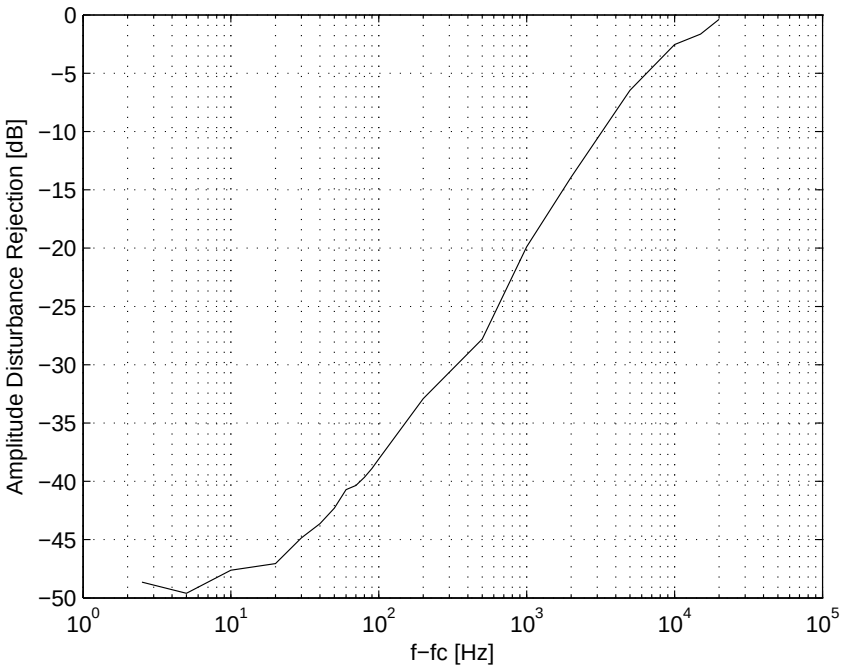

Figure 3.7: The amplitude disturbance rejection under closed-loop control at 22 MHz.

As can be seen in Fig. 3.7, under closed loop control, the amplitude disturbance rejection is better than -47 dB up until 20 Hz and then rolls off linearly and reaches -3 dB at 8kHz. Finally, no effect can be seen above 20 kHz.

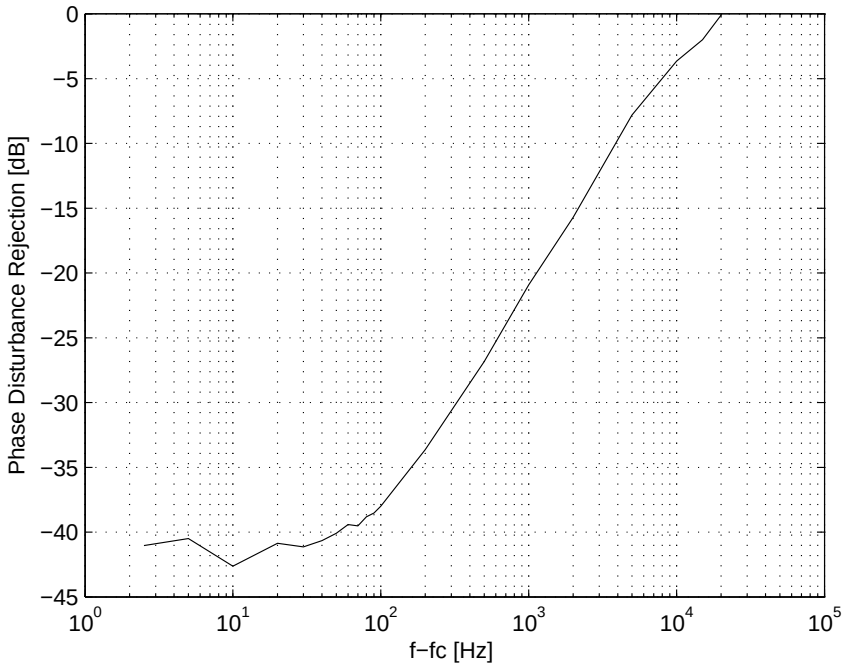

Figure 3.8: The phase disturbance rejection under closed-loop control at 22 MHz.

In Fig. 3.8, under closed loop control the phase rejection disturbance is better than -40 dB up until 40 Hz and then rolls off linearly and reaches -3 dB at 10 kHz. No effect can be seen above 20 kHz.

We can conclude that the closed-loop controllers perform well. The measurement could only be performed at 22MHz since only a phase modulator that operates with a center frequency of 22 MHz was available. The processing latency over the full frequency band of operation is constant, therefore the rejection performance as illustrated in Fig. 3.7 and Fig. 3.8 is valid over the full band.

However, in a cyclotron setup such as iThemba LABS where the electronics is housed separately from the cyclotron, there is more than 50 meters of cabling as well as multi-stage amplifiers between the control system and the resonator. The performance of the system will be impacted by phase delay and by the mechanical and electrical stability of these in-line systems and components. The true performance of the real-time control can only be measured when the cyclotrons are in operation. This is discussed in Section 4.2.

3.4 RF Synthesizer Module

The RF synthesizer module converts the digital 16-bit RF and LO samples generated by the FPGA to analog RF signals. It also contains the 2.4 GHz voltage controlled oscillator (VCO) and PLL that generates the high-speed clock signals required by the high-speed DACs and the FPGA. The module corresponds to the

RF synthesis section highlighted in red in the high level block diagram in Fig. 3.4.

A photograph of the module shown in Fig. 3.9 indicates the major components of the design, such as the PCB, high-speed DACs, 100 MHz low-pass filters, 2.4 GHz VCO and PLL, RF shielding, high density back plane interface and the connectivity and status LEDs on the front panel.

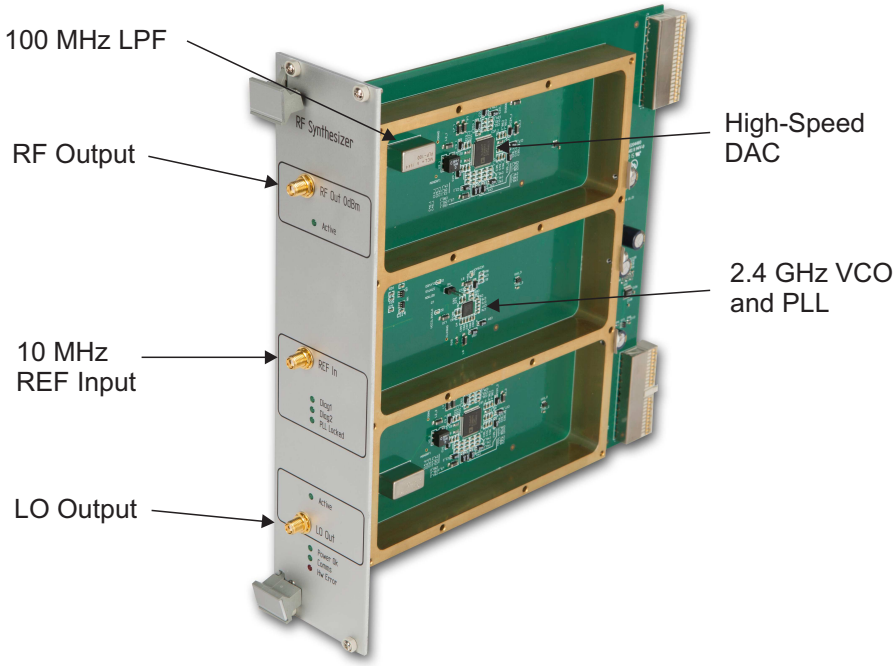

Figure 3.9: A photograph of the RF synthesizer module.

The RF synthesizer module has a complex PCB design because it uses a mixture of high-speed digital bus signals, RF analog signals and high-speed clock signals. The detailed schematics, the bill of materials (BOM) and a multilayer print of the PCB design are shown in Appendix B.4. The PCB has 8 layers, including 4 routing layers, 3 power planes and 1 ground plane. The PCB trace separation tolerance is 127 µm. The high layer count and 127 µm trace separation was necessary to route all the signal pins and to provide multiple power supply voltages.

Most of the signals in the design are treated as high-speed digital signals with a single-ended or a differential impedance of 50 or 100 Ohms and a maximum data and clock rate of 240 MHz.

The RF synthesizer module accepts the 10 MHz RF reference input via the SMA input connector. The PLL locks the on-chip 2.4 GHz VCO to the 10 MHz reference. Internally, the PLL divides the 2.4 GHz clock to the lower clock frequencies and then distributes them to the high-speed DACs and the FPGA. Every clock in each RF control system is therefore synchronized in time with this 10 MHz reference. This allows precise timing to be maintained between systems and greatly simplifies the RF synthesis and demodulation process.

As mentioned previously, this system performs down-conversion which requires a main RF signal that can be modulated in amplitude and phase and an LO signal that is used to mix the RF pick-up signal down to an intermediate frequency (IF). Since the system uses an IF of 1 MHz, the LO frequency in MHz is always given by $f_{LO} = f_{RF} + f_{IF} = f_{RF} + 1$ as this system uses high-side injection. The digital 16-bit data of the RF and LO signals are synchronously streamed from the FPGA via the back plane to the high speed 16-bit DACs on the RF synthesizer module. The reconstructed analog signals are passed through a 100 MHz anti-aliasing low pass filter. The LO and RF signals are then connected via SMA links to the RF amplification and mixing module.

During development it was found that the system noise level could be reduced by operating the high-speed DACs at lower clock frequencies (f_{DAC}) with a data rate interpolation factor of 2 and with the interpolation filter configured for low-pass mode. Consequently, with f_{DAC}=200MHz, the DAC will then supply a data clock of f_{DATA}=100 MHz to the DDS modules in the FPGA.

The maximum frequency that can be synthesized in this mode is then limited by the frequency response of the interpolation filter to $0,41 \times f_{DATA}$. Above this frequency and below the Nyquist frequency of $f_{DATA}/2$, the image frequency from the interpolation process folds down into the operating band, which is undesirable.

This mode works excellently for the fundamental frequency systems and is the default mode of operation for the 3 cyclotrons at iThemba LABS and the Helmholtz-Zentrum in Berlin, which all operate between 8 and 26 MHz.

The DAC can also be operated with a data-rate interpolation factor of 2 and with the interpolation filter configured for high pass mode, which can cover the frequency band of $0,59 \times f_{DATA}$ to f_{DATA} or 59-100MHz.

As mentioned in Chapter 2, iThemba LABS also operates second harmonic bunchers between 16 and 52 MHz and a 3rd harmonic flat-topping system at 49 MHz. For these frequencies, the systems operate with a data rate interpolation factor of 2, with the interpolation filter configured for low-pass mode and with (f_{DAC}) = 240 MHz and f_{DATA} = 120 MHz. The frequency response of interpolation filter limits the operation to 53.3 MHz.

To operate the RF control system in the different modes, the initialization script must be configured to load the correct FPGA firmware and PLL configuration for 200 MHz or 240 MHz operation, as well as the DAC interpolation mode. From an EPICS point of view, no difference appears in the configuration across the different implementations.

3.4.1 Direct Digital Synthesis

The RF and local oscillator (LO) signals are digitally synthesized within the FPGA using direct digital synthesis (DDS) techniques. The conventional implementation (Section 2.6.1.4) uses a frequency tuning word (FTW) of 32-bits with the output frequency given by $f_o = f_s \times FTW/2^{32}$, with $FTW \leq 2^{32} - 1$. Since the synthesized frequency will be an integer multiple of $f_s \times FTW/2^{32}$, it is in general not possible to produce precisely the desired frequency. For example, for a sampling frequency

$f_s = 120$ MHz, the output frequency f_o will be an integer multiple of $120 \times 10^6/2^{32}$ = 0.00279396772384643554687 5 Hz.

Furthermore, the RF control systems employ an IF of 1 MHz across all systems. The I/Q demodulation of the IF (Section 3.3.3.1) utilizes a sampling frequency of 10MHz and hence requires 1 MHz cosine/sine look-up tables (LUTs) containing 10 indexed samples that are multiplied with the IF signals to compute the I/Q components.

When performing down conversion with RF and LO signals synthesized by the conventional DDS, it is not possible to achieve an IF signal of precisely 1 MHz when $f_s = 10$ MHz and the small rounding error will result in the IF frequencies' phase drifting in relation to the phase of the signals represented in the sine/cosine LUT.

This problem can be overcome by modifying the phase accumulator part of the DDS technique so that the DDS can synthesize an output frequency without a rounding error and the solution is discussed below.

In this design a 48-bit accumulator is used, where the maximum value of the accumulator is limited by a comparator to $f_s \times 10^6 - 1$. Extra circuitry is needed to process the overflow but this is straightforward to implement in the FPGA. A block diagram of the modified implementation of the DDS used is shown in Fig. 3.10 and a description is given below.

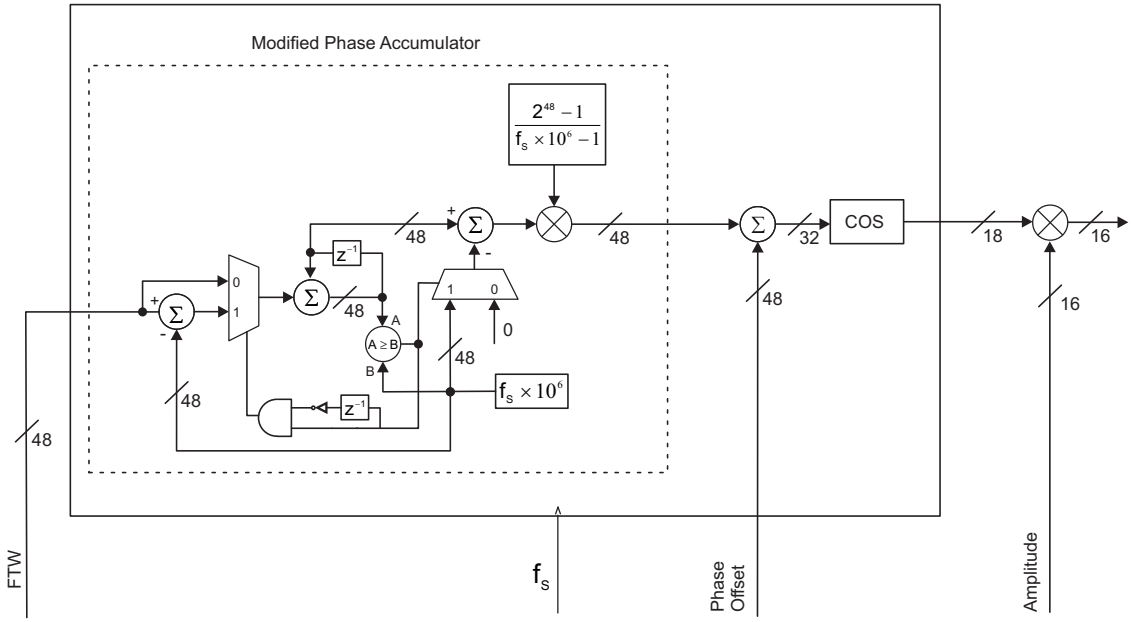

Figure 3.10: A block diagram of the modified implementation of a DDS used in this thesis.

A 48-bit signed adder forms part of the accumulator. The counter value is compared with the overflow threshold value of $f_s \times 10^6$. If the count is below the threshold, the counter is incremented by the FTW, if not, then the overflow

condition loads the counter with a count value less $f_s \times 10^6$. A multiplexer and adder corrects the delayed output value of the adder based on the presence or absence of the overflow condition. The corrected output is multiplied with a scale factor defined by $\frac{2^{48}-1}{f_s \times 10^6 - 1}$ to scale the accumulator output value back to a maximum value of $2^{48} - 1$ and this new output is a digital representation of a value between 0 and 2π radians where 0 is equivalent to $0 \times \pi$ and 2^{48} is equivalent to $2 \times \pi$.

The output frequency is defined by $f_o = \frac{FTW}{f_s \times 10^6} \times f_s = \frac{FTW}{10^6}$ Hz, with $FTW \leq f_s \times 10^6$. This modified phase accumulator allows integer multiples of 1 µHz to be generated for the RF and LO signals, which results in zero phase drift in time between the IF signal and the phase of the sine/cosine LUTs that form part of the I/Q demodulators described previously. This approach then allows the conventional DDS technique to take place whereby a 48-bit phase offset register is used to manipulate the phase of the RF signal. This phase is then passed to a CORDIC based IP core module that implements the cosine function and generates the digital RF signal. It was found by experimentation that by limiting the input of the CORDIC IP core to the 32 most significant bits and by increasing the output accuracy to 18 bits, the synthesized RF signal will have 16-bit accuracy with no bit errors. The output of the cosine function is then multiplied with a 16-bit value to scale the amplitude of the synthesized RF signal. The design has been verified within a Spartan 6 FPGA to operate at 200 MHz clock rate and the VHDL design is shown in Appendix D.

In conclusion, the DDS implementation incorporating the modified phase accumulator allows the RF frequency tuning word to be programmed in steps of 1 µHz and the phase in steps of 0.0001° via the memory mapped interface.

3.5 RF Amplification and Mixing Module

The RF amplification and mixing module amplifies the RF signal and maximizes its dynamic range. The module is also responsible for mixing the 5 input RF channels down to their corresponding 1 MHz IF channel. The module corresponds to the RF amplification and mixing section highlighted in red in the high level block diagram in Fig. 3.4.

Photographs of the module are shown in Figs. 3.11 and 3.12 depicting the major components of the design, such as the PCB, RF amplifiers, passive mixers, digital step attenuators, RF shielding, high density back plane interface and the connectivity and status LEDs on the front panel.

The module has a simpler PCB design than those described in the previous sections. However, as before, the module has a mixture of RF analog signals and digital control signals. The detailed schematics, the bill of materials (BOM), and a multilayer print of the PCB design are shown in Appendix B.4. The PCB has 4 layers with 2 routing layers, 1 power plane and 1 ground plane. The PCB trace separation tolerance is 127 µm. The multi-layer design is required in order to route the RF signals on the outer layers with impedances of 50 Ohms, and to provide power and a unified RF ground plane to enhance shielding of the RF channels. As

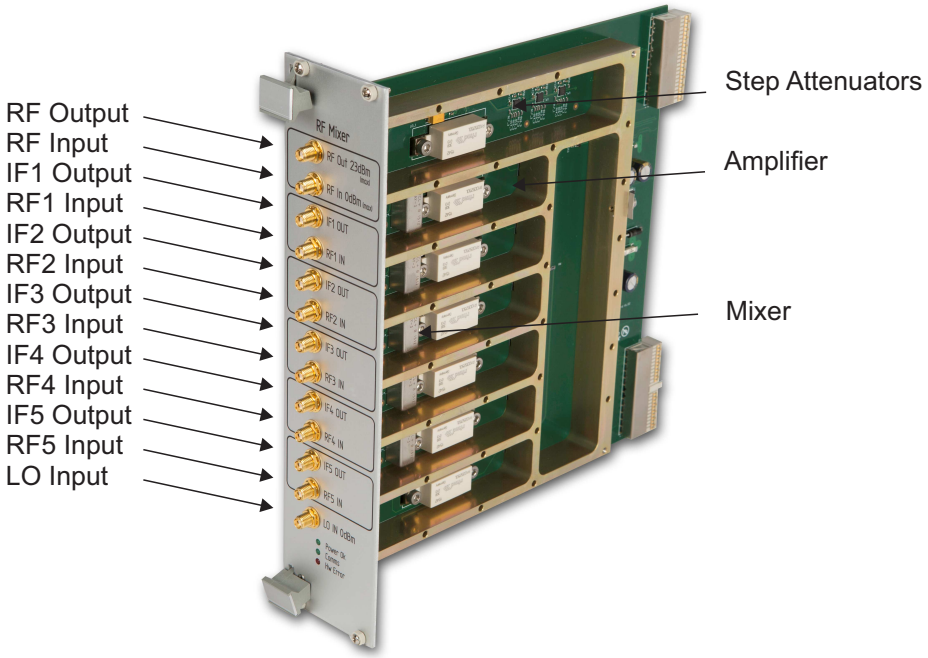

Figure 3.11: A photograph of the RF amplifier and mixing module.

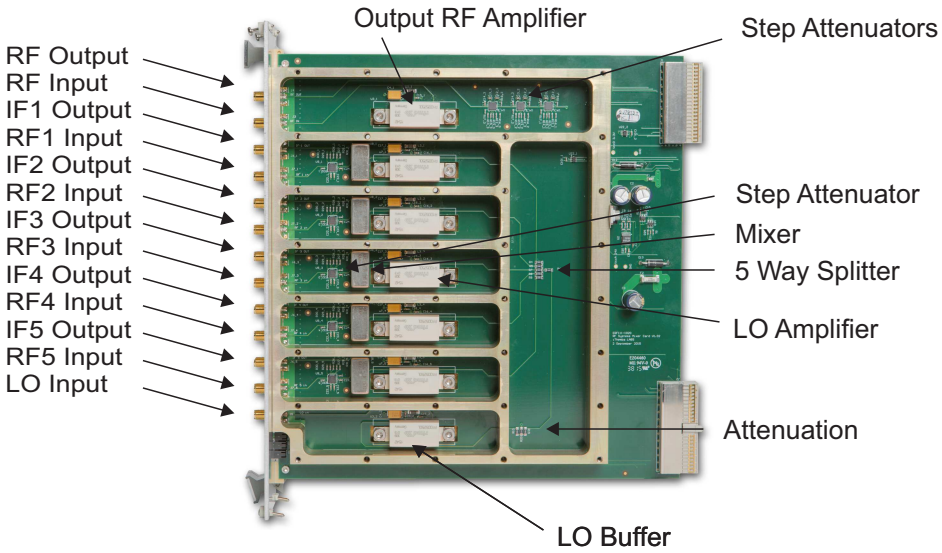

Figure 3.12: A photograph of the top view of the RF amplifier and mixing module.

shown in Fig. 3.12, the RF output channel and the 5 input channels are housed in separate shielded compartments.

The main RF signal is connected to the RF amplifier and mixing module via an SMA link from the RF synthesizer module. High dynamic range is maintained using a 25 dB amplifier cascaded with three 32 dB attenuators that are digitally programmable in 0.5 dB steps as indicated in Figs. 3.4 and 3.12.

The RF output signal is connected via an SMA link to the far right panel on the front of the enclosure and then to the N-type connector at the rear of the system via shielded cabling as illustrated in Figs. 3.1 and 3.2.

Similarly, the resonator pick-up, RF phase reference, auto-tune pick-up and two auxiliary input channels are connected via N-type connectors from the rear of the system to a front panel on the far right and then via SMA links to SMA connectors of the five RF input channels.

High dynamic range is maintained in the input channels by 32 dB attenuators that are programmable in steps of 0.5 dB on each input.

The LO signal is connected to the RF amplifier and mixing module via an SMA link from the RF synthesizer module and then buffered, attenuated, split 5 ways and finally distributed to the buffer amplifiers of each of the passive mixers. The passive mixers utilize the buffered LO signals to mix each RF signal down to a 1 MHz IF signal. Each channel's IF signal is connected to the corresponding input on the IF sampler module via SMA links.

The isolation achieved between the channels is approximately 78 dB with the attenuators set to 0 dB. High isolation is only critical for the first channel which processes the resonator pick-up signal. The isolation can be increased by adjusting the attenuators of the remaining channels. To achieve greater than 80 dB isolation, typically 10 dB attenuation is inserted.

3.6 IF Sampling Module

The IF sampling module samples each of the five 1 MHz IF channels at a sampling rate of 10 MHz, and then streams the digital data serially at a bit clock rate of 300 MHz to the FPGA for demodulation.

The module corresponds to the IF sampling section highlighted in red in the high level block diagram in Fig. 3.4. Photographs depicting the major components of the design, such as the PCB, ADCs, LPF, RF shielding, high density back plane interface and the connectivity and status LEDs on the front panel are shown in Figs. 3.13 and 3.14.

The IF sampling module is complex as it includes a mixture of high-speed digital signals, RF analog signals and high-speed sampling clock signals. The detailed schematics, the bill of materials (BOM), and a multilayer print of the PCB design are shown in Appendix B.7. The PCB is an 8 layer design and has the same design specifications as the RF synthesizer module described in Section 3.4.

The system uses a 1 MHz IF. The five IF channels are first low-pass filtered by passive filters with 3dB frequency responses of 1.2 MHz to remove the high frequency components that result from the mixing process. The frequency response

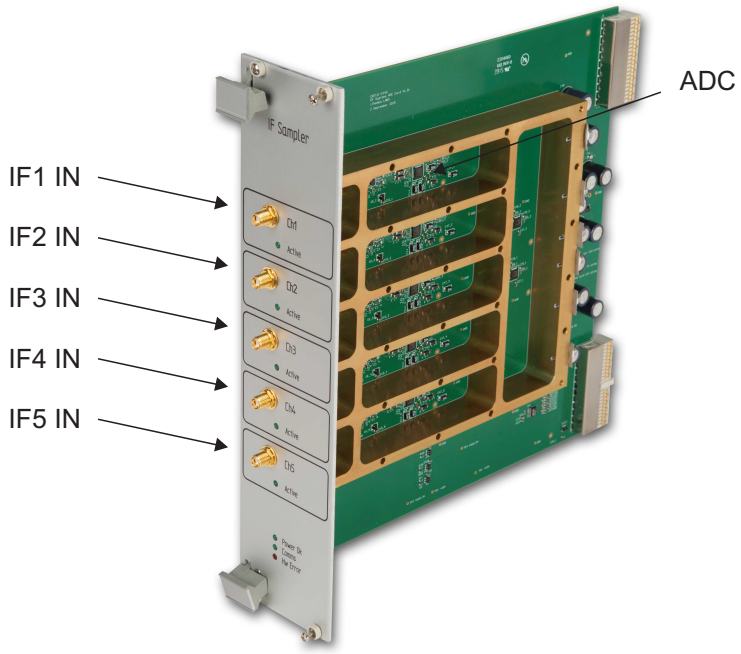

Figure 3.13: A photograph of the IF Sampling module.

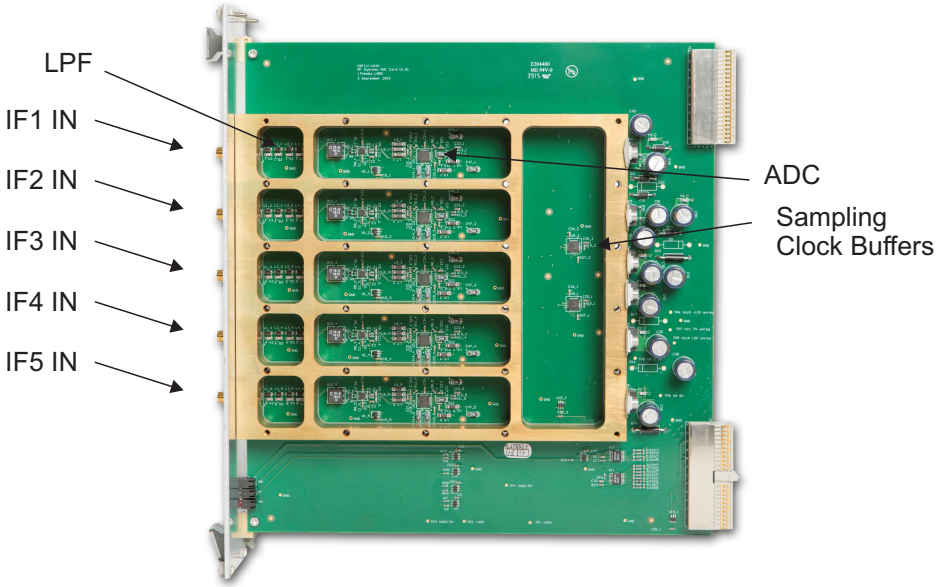

Figure 3.14: A photograph of the top view of the IF Sampling module.

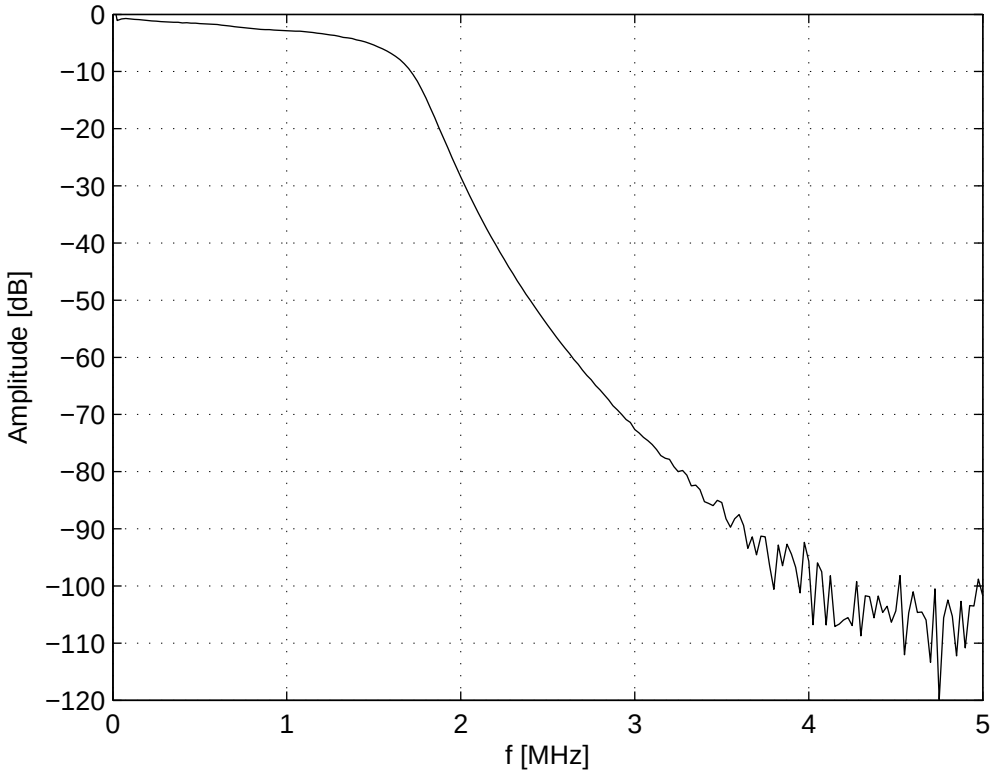

Figure 3.15: The frequency response of the passive IF low-pass filter.

of the filters is shown in Fig. 3.15. For the lowest operating RF frequency of 2MHz the mixing process will result in a high frequency component at 5 MHz which will be attenuated by more than 90 dB.

The filtered IF signals are then sampled by 16-bit 10 MHz successive approximation register (SAR) ADCs. The resulting digital data is streamed serially at a bit rate of 300 MHz via the back plane to the FPGA for demodulation.

3.7 Interlocking Interface Module

The interlocking interface module conditions the input interlock signals from external sources and connects them to the FPGA via the backplane. It also handles the output interlock signals from the FPGA which are connected via relay contacts to external systems.

The module corresponds to the interlocks section highlighted in red in the high level block diagram in Fig. 3.4.

A photograph of the module is shown in Fig. 3.16 depicting the major components of the design, such as the PCB, output relays, input conditioning, high density back plane interface and the connectivity and status LEDs on the front panel.

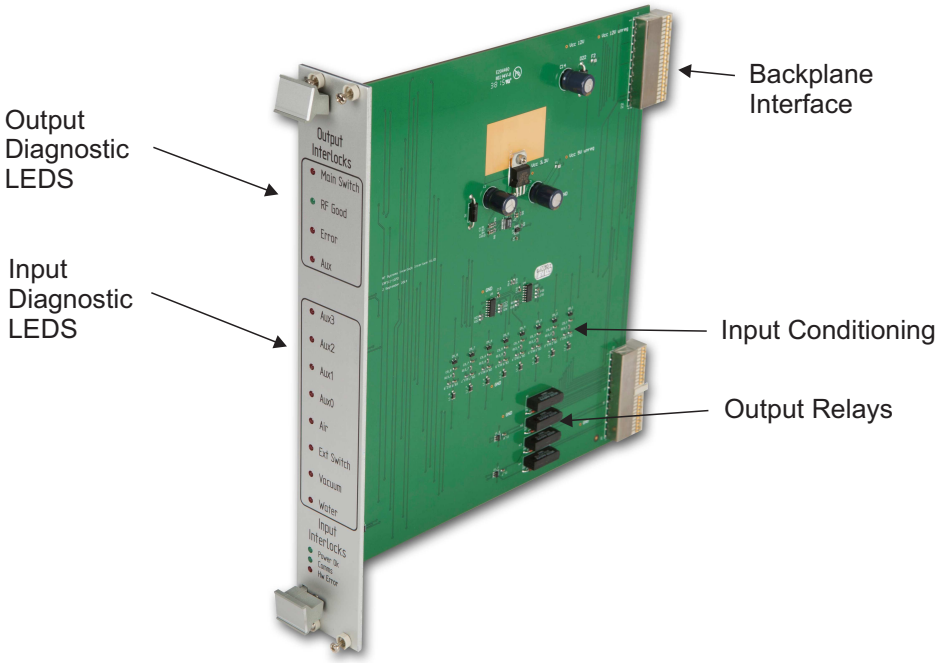

Figure 3.16: A photograph of the Interlocking Interface module.

The FPGA samples the 8 input interlock signals at 100 MHz. A further 8 interlock signals in the FPGA are grouped together with the external input interlocks. The internal interlocks are generated from watchdogs, the RF monitoring circuit and a combination of soft interlocks from registers in the memory mapped interface. The instantaneous and latched status is available via the memory mapped interface. A disable mask for each interlock can also be set via the memory mapped interface. The latched and enabled interlock signals are logically ANDed in the FPGA and if an interlock occurs then the RF output signal is disabled immediately. The status of the interlocks is also output to the status LEDS on the interlocking module. The output interlocks can be configured to trigger from the latched interlock status or from registers in the memory mapped interfaces. This enables slow monitoring loops in the EPICS IOC to trigger an interlock too. The output interlocks can be connected to an external system such as a safety control system.

3.8 EtherCAT Motion Control

In 2015, iThemba LABS adopted EtherCAT as its new industrial communication standard. The EPICS EtherCAT interface (Mercado *et al.*, 2011), as developed by the Diamond Light Source, has been fully integrated to work with stepper motor, DC motor, analog input and output and digital input and output terminals as provided by Beckhoff. This means that all tunable RF elements in the power amplifiers, such as the grid and anode circuits, and the tunable elements within the resonators, such as the coupling capacitors, short-circuit plates, and auto-tune

trimmer capacitors, are under EPICS EtherCAT based motion control.

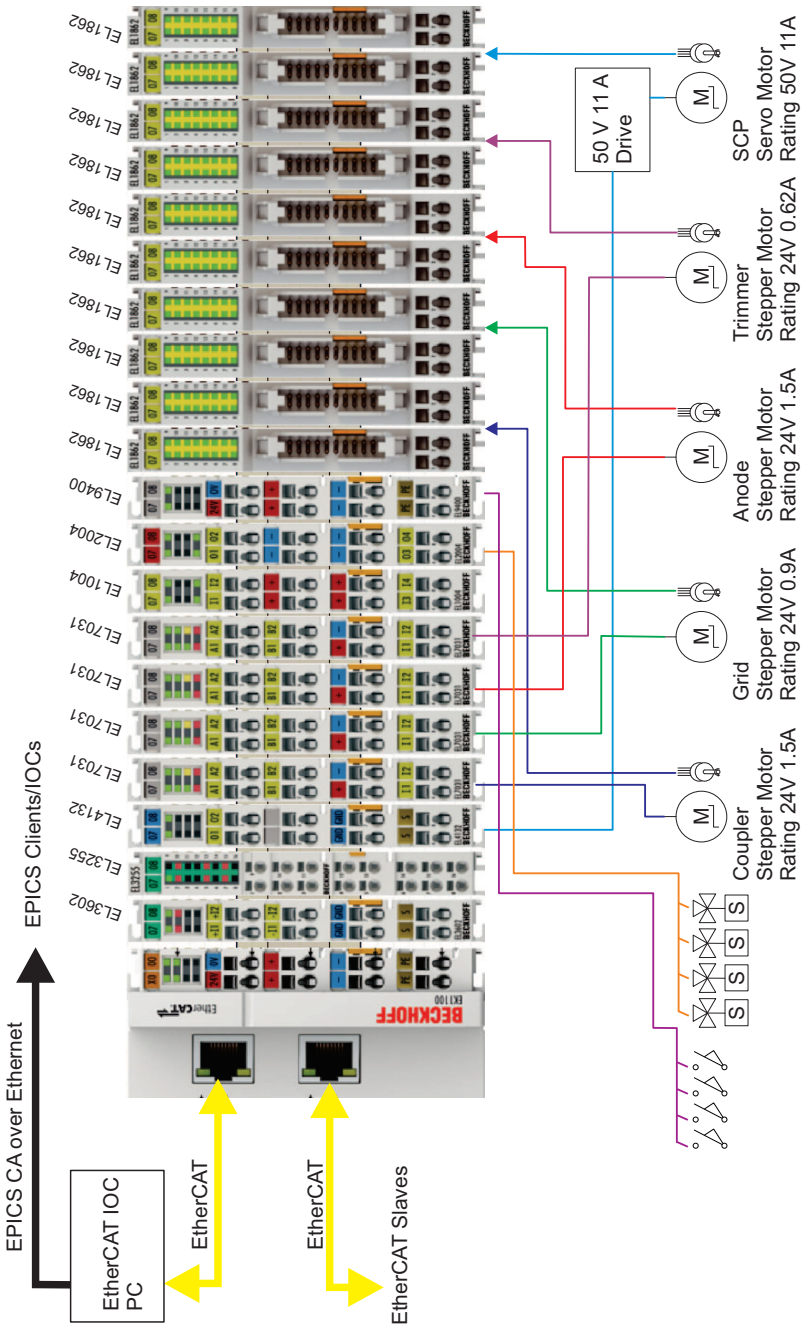

Figure 3.17: A block diagram of the EtherCAT Motion Control as implemented on SPC2 north RF system.

The EPICS EtherCAT IOCs operate on x86 PC hardware. Communication between the RF controller IOC and the EtherCAT IOC occurs via EPICS CA. Heartbeats on the EtherCAT IOC can be configured to reset watchdog timers in the RF controller IOC. If the watchdogs time out then a soft interlock is triggered in the

FPGA preventing unsafe operation of the RF control system when the EtherCAT IOC is not operational.

A block diagram indicating the EtherCAT modules, motors and actuators under control, EtherCAT IOC and EPICS CSS clients as configured on the SPC2 north system is shown in Fig. 3.17.

Each of the tunable elements can be controlled in closed or open-loop mode. In closed-loop mode, a PID controller controls the motor's position based on a set point and the encoder's feedback. The set points are determined by load curves and are set in the CSS user interface. In open-loop mode the motors can be jogged in clockwise and counter-clockwise directions at a fast and slow speed.

Apart from the auto-tune controller described in the next section all the other tunable elements are only operated when initializing their positions for the desired cyclotron operating frequency.

3.9 Auto-tune Control

Auto-tune control of the resonator's trimmer capacitor is necessary to keep the resonator matched to the RF PA's output impedance of 50 Ohm and to minimize the reflected power to prevent the PA's tube from being damaged. Control of the trimmer capacitor for each of the RF systems is performed through EPICS CA between the RF controller IOC and the EPICS-EtherCAT motion control IOC as described in the previous section.

The auto-tune phase error is derived in the FPGA as described in Section 3.3.3.2 and is made available to the RF controller IOC.

The resonator trimmer capacitor can be positioned manually by the operator or automatically by the sequencer as described in the next section, though under normal operating conditions the sequencer will enable the auto-tune control of trimmer capacitor.

When in auto-tune control mode, the RF controller IOC manipulates the trimmer capacitors' position in open-loop mode by using the jog commands.

The user interface for the auto-tune controller of the SSC west trimmer is shown in Fig. 3.18. The user interface is schematically defined and in the case of the SSC west side, the phase difference between the RF pick-up and auto-tune pick-up are used to control the trimmer. To set up the system, a phase offset is added to the auto-tune pick-up's phase by the operator. The EPICS phase-offset process variable then modifies the phase of the sine and cosine look-up table of the auto-tune pick-up channel in the lower-speed, high-latency DSP path as described in Section 3.3.3.2. The FPGA subtracts the offset phase of the auto-tune pick-up from the RF pick-up and calculates the smoothed error which in this case has to be down sampled 32 times.

Two window comparators exist in the RF controller IOC to determine if the phase error is large or small. If the phase error is large then the motor is jogged at a faster speed until the phase is within range (typically 10 °) and if the phase-error is small then the motor is jogged at a slower speed until it is within range of typically 2.5 °.

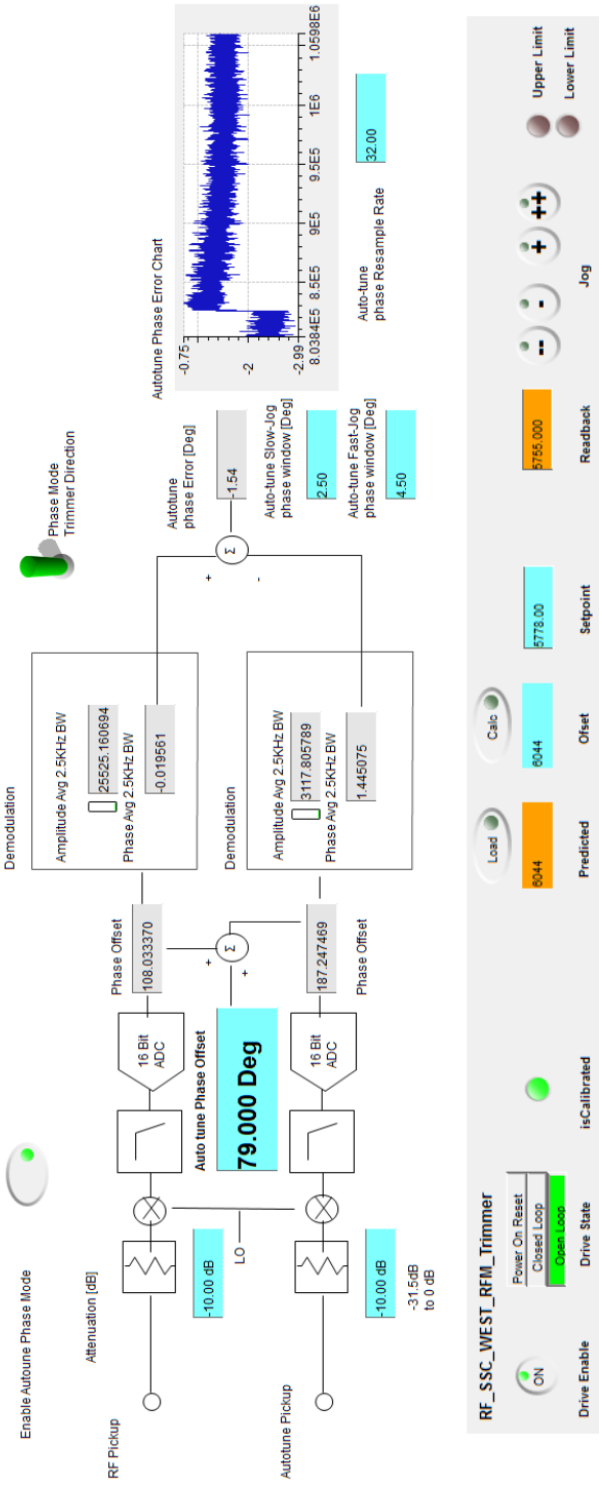

Figure 3.18: The auto-tune control user interface.

The interface provides a graph which displays the auto-tune phase error versus time. As illustrated, there is a step in the phase error as a result of the trimmer being moved when the phase-error drifted outside the small window.

The motion control interface is displayed below the schematic layout allowing the operator to control the trimmer capacitor manually in closed or open-loop mode.

For the implementation at the Helmholtz-Zentrum Berlin the auto-tune controller was configured differently. As described in Section 2.4.1, the PA's anode and grid pick-up phase difference is used to control the position of the flap trimmer capacitor. In this case the phase between them must be kept at 180°. This is accomplished by modifying the auto-tune phase selector to use the 1st auxiliary RF channel in place of the resonator pick-up, connecting the grid pick-up to the auxiliary channel and the anode to the auto-tune channel and then by programming the phase offset to 180°.

3.10 Automation and Sequencing

A State Notation Language based EPICS sequencer has been used to fully automate the operation of the system. The sequencer portion of the engineering user interface is shown in Fig. 3.19. The sequencer state machine flow is illustrated at the top of the figure and the automation routines that the sequencer performs are illustrated in the columns of selection boxes for a power on reset initialization, cold start and warm start.

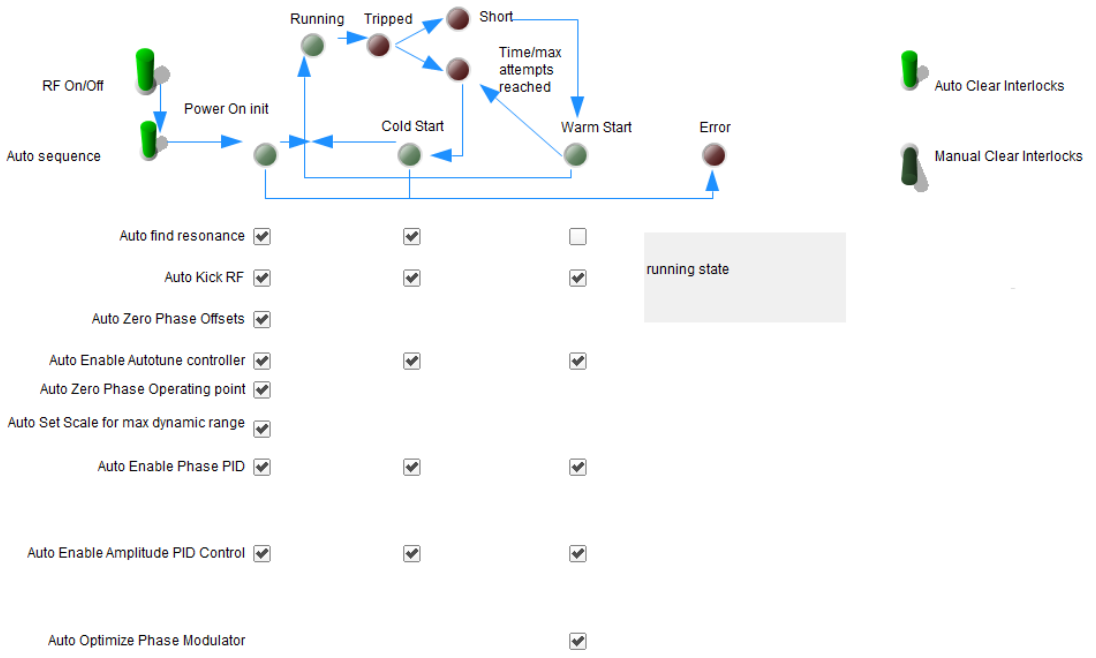

Figure 3.19: A screen shot of the sequencing control user interface.

At any stage, the user can disable any of the automation routines in the sequencer state machine by deselecting the tick box for the corresponding power on reset, cold start or warm start routine. This allows partial automatic configuration of the system and manual diagnosis of a problem with the automation routines. A description of the sequencer program flow is given below.

The sequencer program was designed to allow manual as well as automatic configuration. Manual configuration mode allows the user to manually find resonance and adjust the system parameters. When automatic configuration is selected and the system is powered up for the first time, a power-on reset initialization is performed. The power on reset initialization adjusts system parameters to load the initializing frequency and then the system's LO phase to achieve the desired reference phase offset. It will then move into a cold-start mode and find the resonance peak by applying a small amount of RF power to the resonator and sweeping the trimmer capacitor across its full range. This is illustrated in Fig. 3.20 where two sweeps of the trimmer have been made, one with a low RF power and one with a higher RF power where the effects of multipacting can be seen on the top trace. Multipacting is a vacuum phenomenon of resonant electron multiplication and results when electrons impinge upon a surface and in doing so cause the emission of secondary electrons. If the time of flight of these electrons is a multiple of the RF period it is possible to initiate an electron avalanche that can cause a spark over (Chao *et al.*, 2013). If the multipacting effect is noticed, the user should adjust the resonance search mode power to a level where a sharp peak is seen as is illustrated in the lower trace in Fig. 3.20.

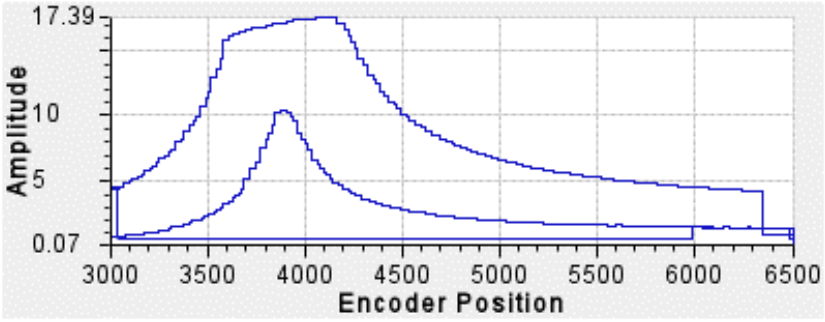

Figure 3.20: Relative demodulated RF signal amplitude on a 16 bit resolution scale vs the trimmer capacitor's 13 bit absolute encoder position during automatic resonance search mode for a low as well as a higher RF power level that results in multipacting.

Once the resonance peak is found, the sequencer will switch on the RF at the predetermined kick level and pulse duration in order to break though the multipacting. Thereafter the RF amplitude is reduced to a hold level. If the detected RF level is not above the minimum threshold level then the system will try to kick the RF a maximum of 5 times. The kick level, pulse duration, hold level and minimum threshold level are determined experimentally and are unique to each RF system

and operating frequency. If none of these attempts are successful, the system will stop and enter into an error state and the operator will need to diagnose the problem. If the RF signal is above the minimum threshold level, the trimmer capacitor auto-tune control followed by the phase and amplitude PID controllers are enabled. The sequencer then increases output power to the desired set point. Once the set point is reached normal operation can occur. The system then enters a warm-start mode. Should any interlock or trip occur and clear within the predetermined time, the sequencer will switch on and restore operation at the current trimmer capacitor position. Should this be unsuccessful or should the maximum time elapse, the system will attempt to switch on from the cold-start state. Should this be unsuccessful, the system will attempt to find resonance by sweeping the trimmer capacitor and subsequently switch on and restore the system. Should this final attempt also fail, the system will stop in an error state and the engineer responsible will need to investigate the problem.

3.11 User Interface

A Control System Studio (CSS) based graphical user interface (GUI) has been developed for the control systems. The CSS GUIs communicate to the EPICS IOCs through EPICS CA. The entry point for the GUI is an overview screen which indicates the operational status of all the RF systems at iThemba LABS. A neutral blue indicates that the systems are not currently in use, green that the systems are in an operational state, red that there is a problem such as an external interlock and orange that the system is busy starting up or recovering from an error condition to enter into the the operational state. An example of the overview screen is shown in Fig. 3.21 indicating the operational status of the systems, with SPC2 as injector to the SSC with the AX, K and J-line bunchers in operation.

The overview screen is active and by clicking on the specific RF system, the operator screen will open. The operator screen for the SSC west and east RF systems is shown in Fig. 3.22 and allows the operator to adjust the amplitude and phase set points. Real-time display of 10 ms and up to 100 seconds of the amplitude and phase of the RF pick-up signal is available to the operator allowing intuitive feedback and diagnostic ability. The operator interfaces are generically designed and implemented with minimal changes for the other RF systems.

A separate, multi-tabbed CSS engineering user interface provides all system-level parameters to the user. The engineering user interface is accessible through the advanced tab of the operator interface. The amplitude and phase settings tab of the engineering GUI for the SSC west system is shown in Fig.3.23. This page allows the user to control the parameters for the resonance search level, kick and ramp profile, trip levels, sequencer modes, and amplitude and phase PID control modes. The send and return signal chains of the RF system are displayed schematically and the instantaneous and latched interlocks are displayed on the lower left portion of the page. The GUI allows the user to intuitively interact with any of the parameters, optimize and diagnose any faults with the system.

Further display tabs are available to perform specific functions such as, loading

and saving of settings, monitoring the RF systems, initializing the RF frequency, controlling the sequencer, controlling and positioning the tunable elements and searching for resonance.

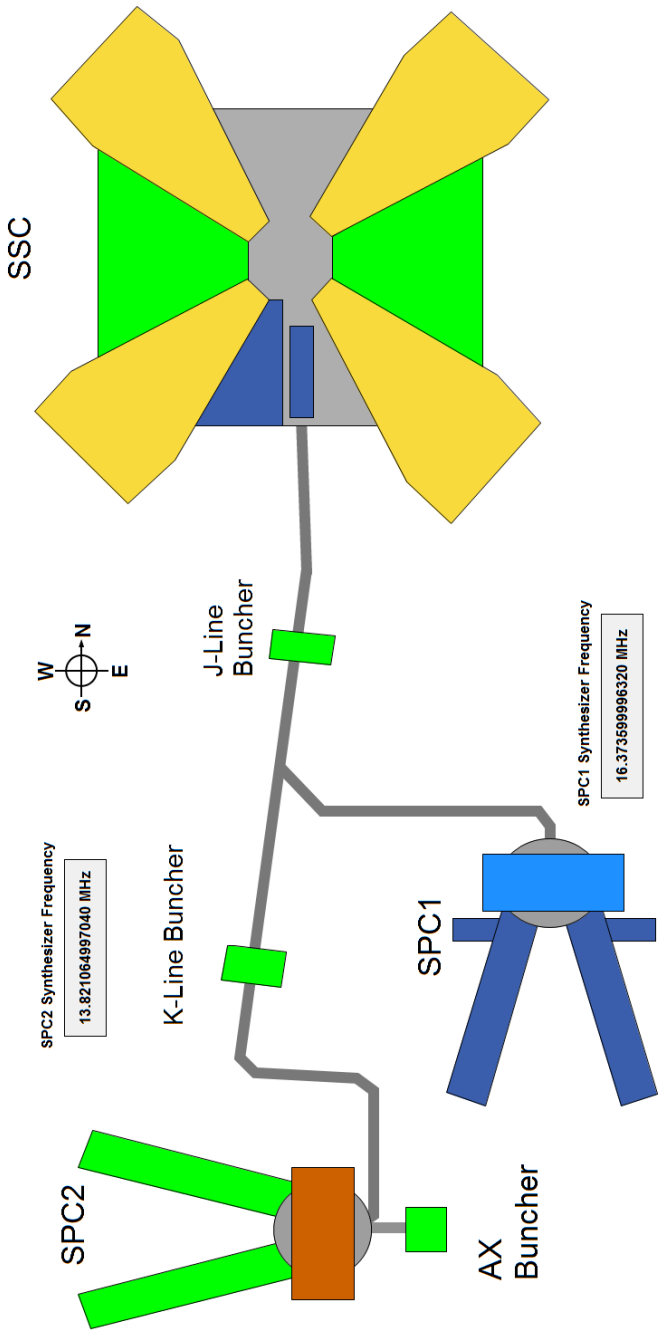

Figure 3.21: The overview user interface, depicting the status of all the RF systems at iThemba LABS.

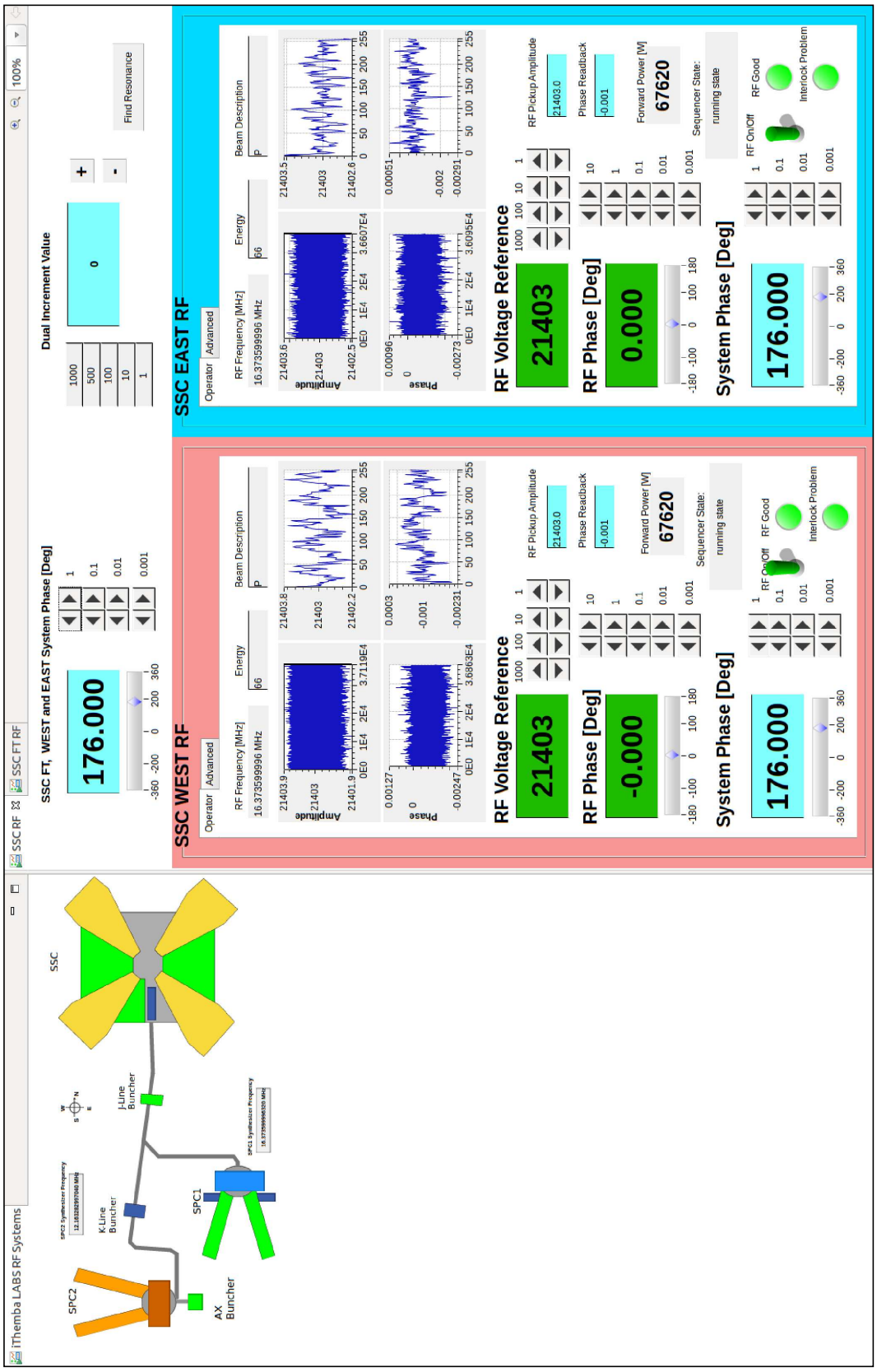

Figure 3.22: The operator user interface for the SSC west and east RF systems.

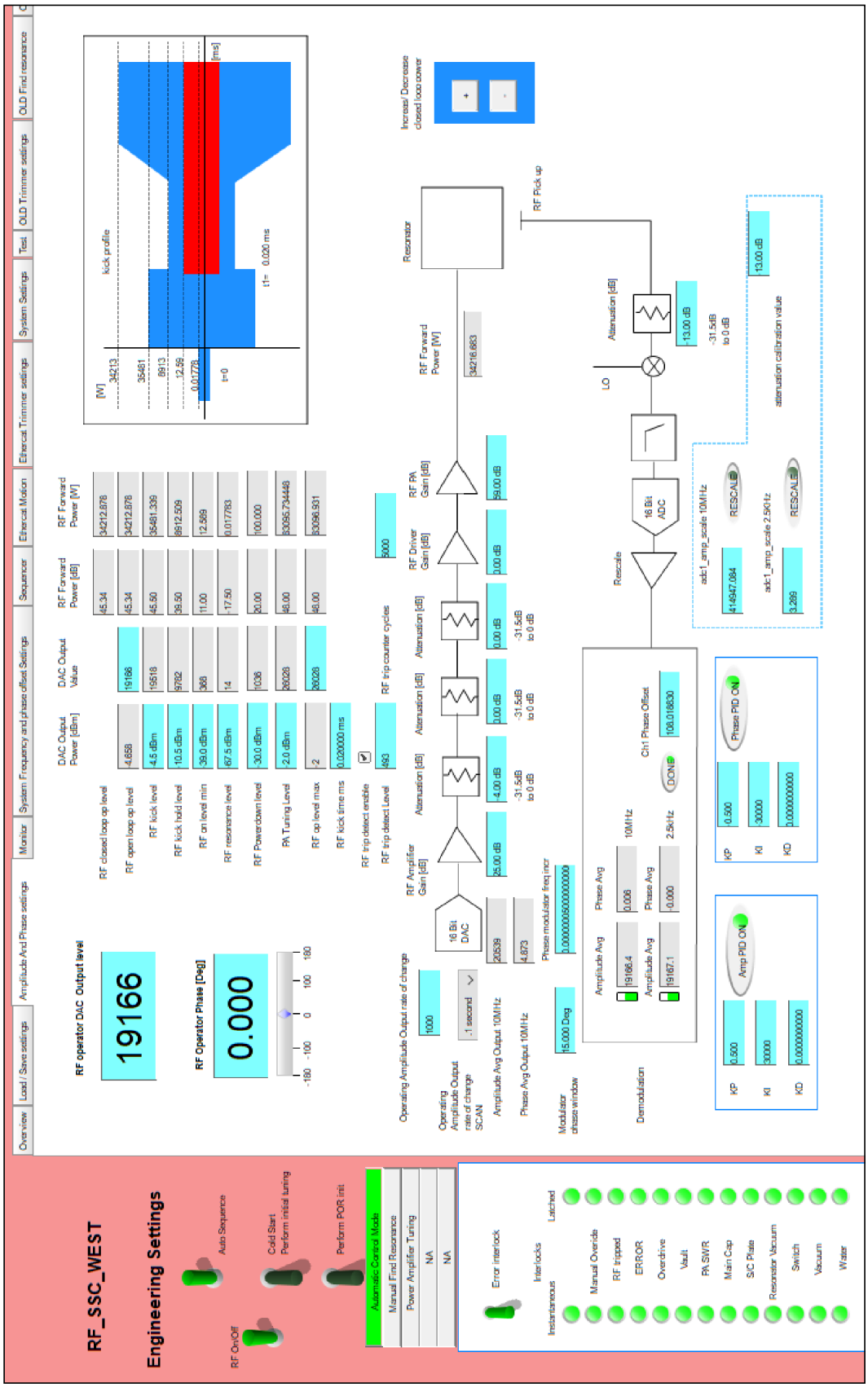

Figure 3.23: The engineering user interface for the SSC west RF system.

3.12 Implementation at iThemba LABS

A total of 13 RF control systems are in operation at iThemba LABS. Eleven are used on the cyclotrons and buncher systems and two of the systems are used as the reference synthesizers for SPC1 and SPC2 respectively.

The cyclotrons and RF system equivalent circuits with connections to the RF control systems have already been described in Section 2.2 and only an overview of the RF, 10 MHz distribution and the EPICS control systems for the complete implementation of the RF control systems at iThemba LABS is discussed below.

The implementation of the RF and 10 MHz distribution is best described with reference to the block diagram in Fig. 3.24.

As previously mentioned, all the RF control systems are time synchronised with a single 10 MHz reference. The reference is housed in the SPC2 electronics area and a distribution network feeds the 10 MHz reference to the SPC2 synthesizer, SPC2 cyclotron north and south resonator control systems, and the AX and K-line bunchers' control systems. The signal is also distributed to another distribution network located in the SPC1 and SSC electronics area which supplies SPC1's synthesizer, SPC1 cyclotron west and east control systems, the SSC's west, east and flat-top control systems as well as the J-line buncher and pulse-selector control systems. Provision was made in both areas for future expansion.

For SPC2, the output of the synthesizer feeds a distribution network for the phase reference of the RF control systems. The 1^{st} leg is split and distributed to both of SPC2's north and south control systems with equal length cables as these systems must be operated in phase. The 2^{nd} leg is distributed to the AX-line buncher, the 3^{rd} leg is doubled in frequency and distributed to the K-line buncher. The remaining legs are used for the monitoring oscilloscope, future expansion and for a connection to the reference distribution of the SSC.

For SPC1, the output of the synthesizer is first split with the 2^{nd} leg split again and distributed to both of SPC1's west and east control systems with equal length cables as these systems must be operated in phase.

The 1^{st} leg of the initial splitter provides a connection to a 16 way RF distribution system that provides the synthesizer reference to the rest of the facility. Depending on which injector cyclotron is required, the specific system's reference is connected to the distribution system. One of the legs is connected to another distribution network which provides the phase reference for the SSC west and east RF systems, the 3^{rd} harmonic reference for the SSC flat-top systems and the 2^{nd} harmonic reference for the J-line buncher.

The synthesizer phase reference for the RF control systems is only used to synchronize the RF control systems to a known phase relative to the synthesizer during a power on reset initialization which is performed during an energy change to a new operating frequency. During operation each system is kept synchronised by the PLL on the RF synthesizer module that is locked to the 10 MHz reference, as described in Section 3.4.

A block diagram of the EPICS implementation of the RF control systems at iThemba LABS is shown in Fig. 3.25. In total 18 IOCs have been deployed along with several client PCs.

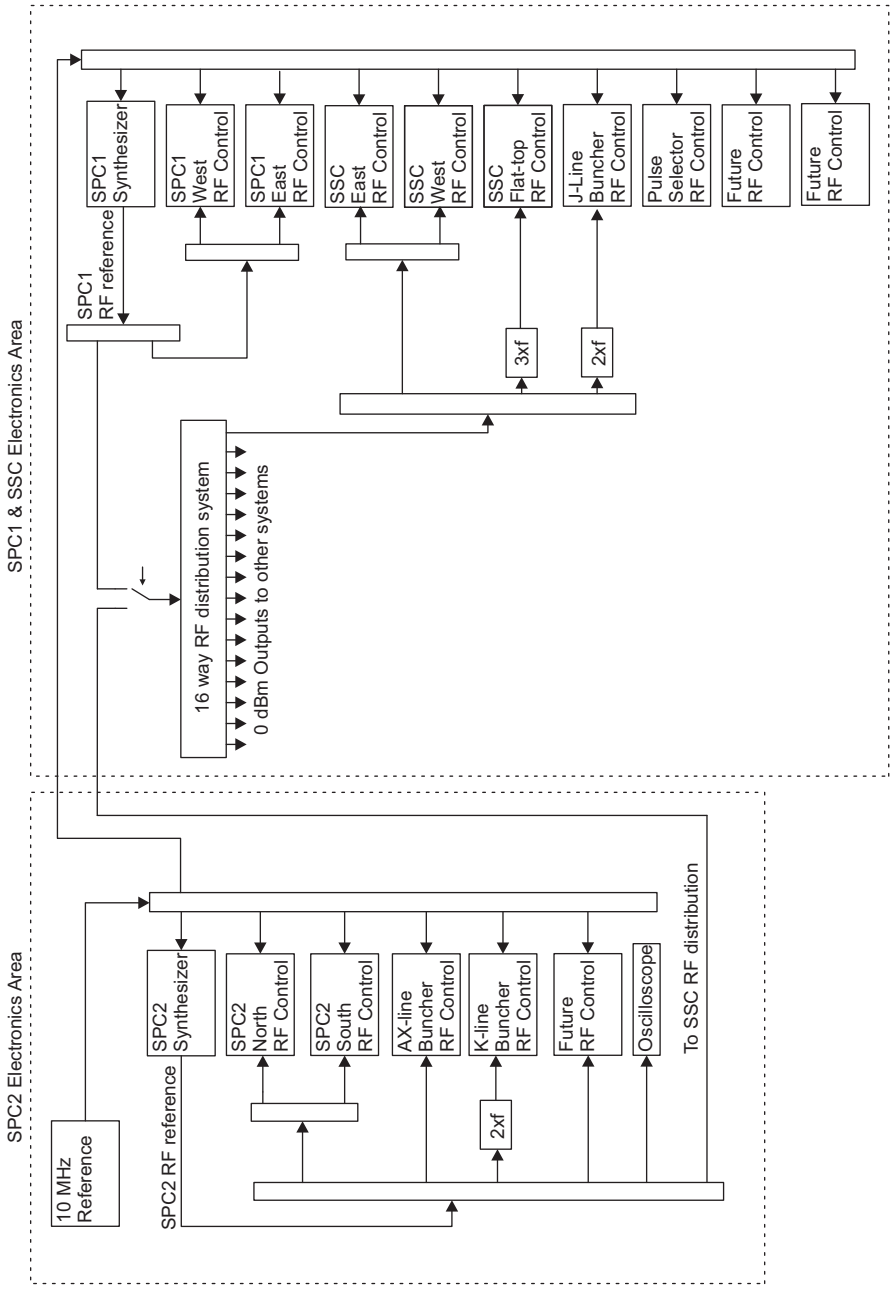

Figure 3.24: A block diagram of the RF and 10 MHz reference distribution for iThemba LABS' RF control systems.

In SPC2 electronics area, engineering and operator client PCs communicate via EPICS CA over the control network to the SPC2 synthesizer IOC, the SPC2 cyclotron north and south resonator RF control system's IOCs, the SPC2 north and south EtherCAT motion control IOC, the AX and K-line bunchers' control system's IOCs and the AX and K-line bunchers' EtherCAT motion control IOC.

In the SPC1 and SSC electronics areas, an engineering client PC communicates with SPC1 synthesizer IOC, the SPC1 west and east RF control system and

EtherCAT motion control IOCs, the SSC west, east and flat-top RF control and EtherCAT motion control IOCs, and the J-line buncher and pulse-selector RF control and EtherCAT motion control IOCs.

In the control room, an overview display is available, and separate operator and engineering client stations provide control to all the RF control system IOCs.

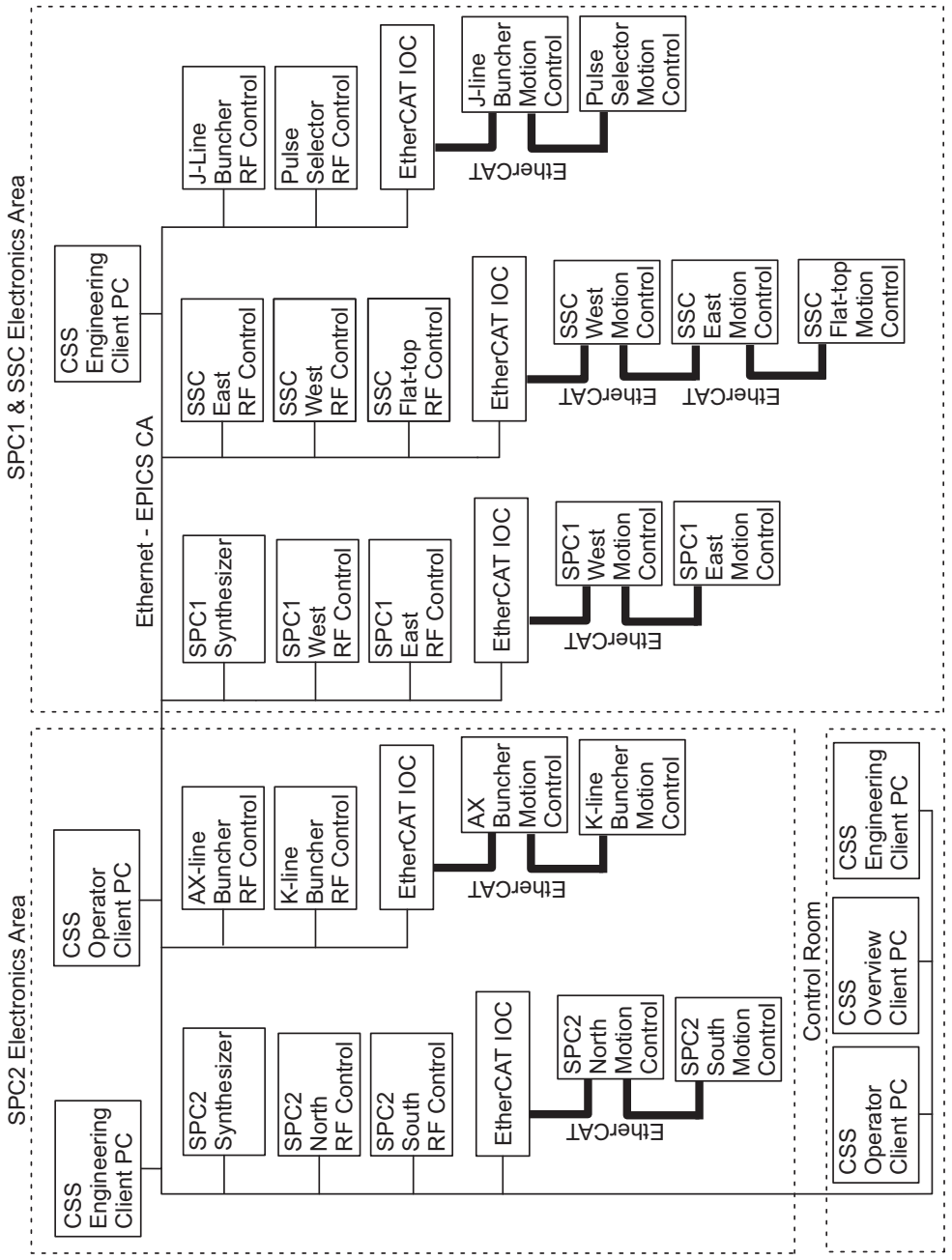

Figure 3.25: A block diagram of the EPICS and EtherCAT IOCs, as well as the EPICS clients implemented for iThemba LABS RF control systems.

3.13 Implementation at Helmholtz-Zentrum Berlin

Two RF control systems are in operation at the Helmholtz-Zentrum Berlin (HZB) on the K=132 cyclotron. The installation of two more systems on the two buncher systems is planned at a later stage.

The equivalent circuits of the cyclotron RF systems and their connections to the RF control systems have already been described in Section 2.4.1. Hence only an overview of the RF, 10 MHz distribution and the EPICS control system implementation of the RF control systems at HZB is discussed below.

The implementation of the RF and 10 MHz distribution is best described in reference to the block diagram in Fig. 3.26. As previously mentioned, all the RF control systems are time synchronized with a single 10 MHz reference. The reference is supplied by the 10 MHz internal reference output of the commercial synthesizer in use at HZB and a distribution network feeds this 10 MHz signal to the HZB cyclotron north and south resonator control systems. Provision was also made in both areas for the future installation of the bunchers' control systems.

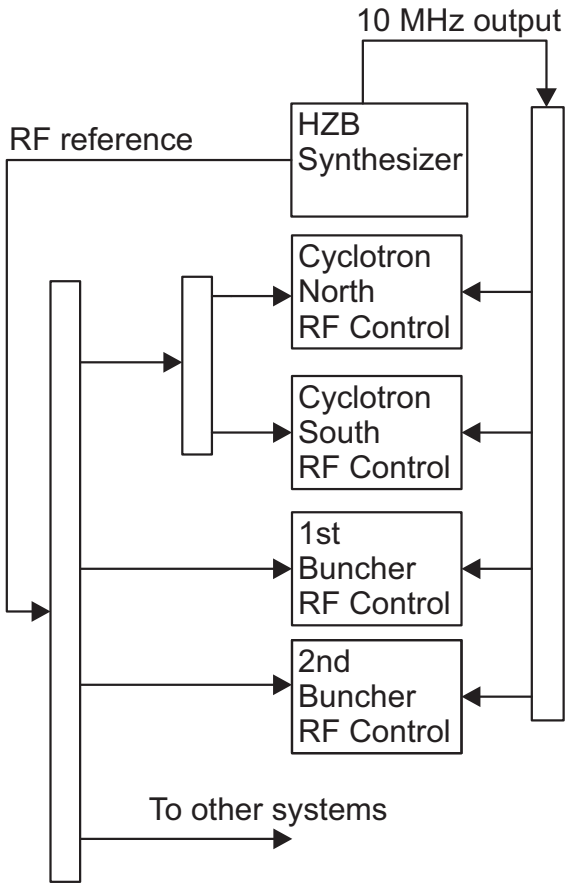

Figure 3.26: A block diagram of the RF and 10 MHz reference distribution for the RF control systems at the HZB.

For HZB, the output of the synthesizer feeds a distribution network for the phase reference of the RF control systems. The first leg is split and distributed to both of HZB's north and south control systems with equal length cables as these systems must be operated in phase. The remaining legs will be used for future expansion and for a connection to other systems within the facility.

As with the iThemba LABS installation, the synthesizer phase reference for the RF control systems is only used to synchronize the RF control systems to a known phase relative to the synthesizer during a power on reset initialization which is performed during an energy change to a new operating frequency. During operation each system is kept synchronised by the PLL on the RF synthesizer module that is locked to the 10 MHz reference, as described in Section 3.4.

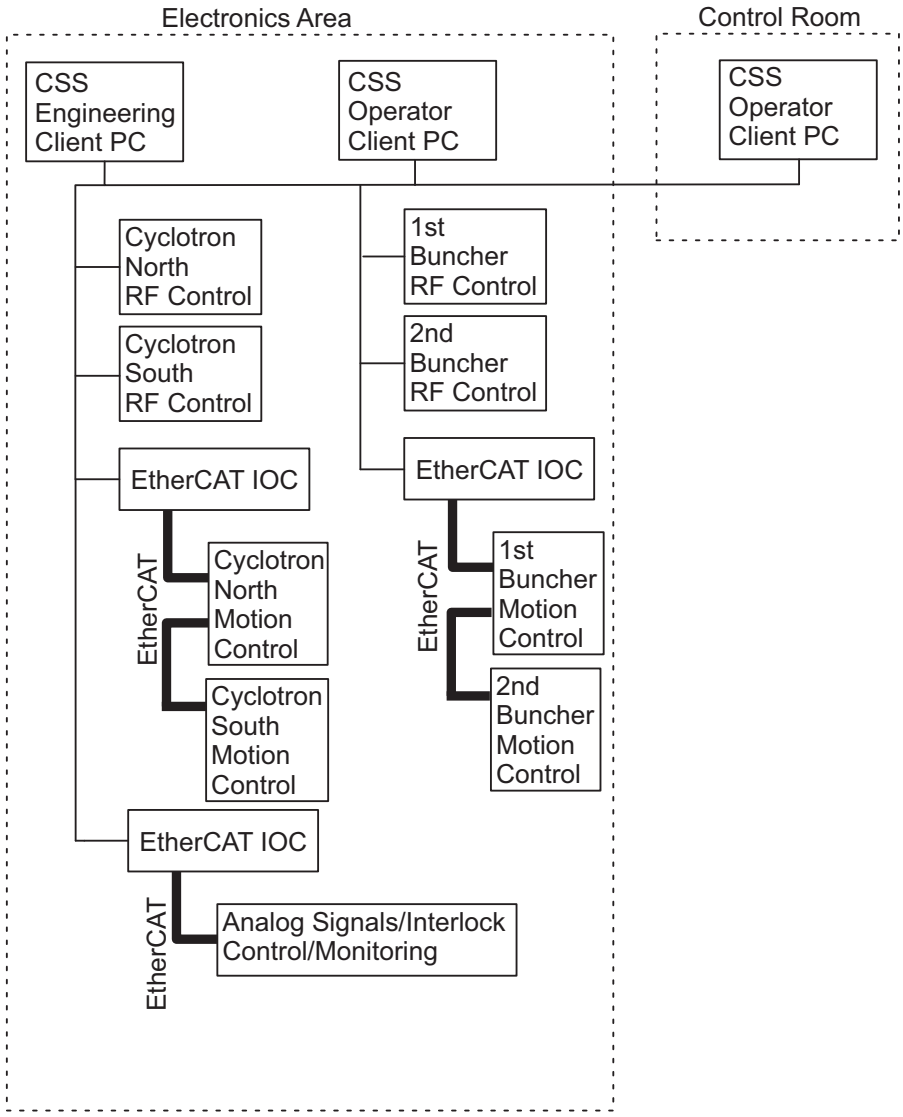

Figure 3.27: A block diagram of the EPICS and EtherCAT IOCs, as well as the EPICS clients implemented for HZB RF control systems.

A block diagram of the EPICS implementation for the RF control systems at HZB is shown in Fig. 3.27. In total, 4 IOCS have been deployed, along with several client PCs. In the electronics areas, engineering and operator client PCs communicate via EPICS CA over the control network to the HZB cyclotron north and south resonator RF control systems IOCs, the north and south EtherCAT motion control IOC, and another EtherCAT IOC used for monitoring and control of the interlock signals and also the monitoring of analog voltage and current signals from the RF PA systems.

3.14 Conclusion

In this chapter the design of the new digital low-level RF (DLLRF) control system was presented. The design culminated in 3 fully functional modular prototypes which were installed and qualified on the second injector cyclotron at iThemba LABS, SPC2 and in the production system, of which 35 units were successfully manufactured.

The design meets the peak-peak amplitude and phase stability targets of 0.01% and 0.01° respectively. This was enabled by a design employing state-of-the-art field programmable gate arrays (FPGA), digital signal processing (DSP), high-speed digital to analog converters (DAC) and high-speed analog to digital converters (ADC).

RF and LO signals with 16 bit amplitude accuracy and programmable in 1 µHz and 0.0001° were achieved by modifying and optimizing the direct digital synthesis (DDS) techniques and by utilizing high-speed 16-bit DACs to directly convert the digital RF signals to analog signals.

Down-conversion of the RF pick-up signals to an optimal IF of 1 MHz and sampling the IF channels by 16-bit, single sample-latency 10 MHz ADCs, eliminates any effect imposed by possible sampling clock jitter. High-speed low-latency I/Q demodulation of the IF channels within the FPGA enables efficient real-time closed-loop control of the amplitude and phase of the RF signal.

The efficient implementation of a Linux based EPICS IOC, which communicates with the FPGA through memory mapped registers, provides a platform with a stable distributed control system allowing full automation using the EPICS based State Notation Sequencer and enabling the system to recover from most situations and with the augmented ability to find resonance.

The ability to monitor the amplitude and phase of the RF pick-up signal in real-time allows intuitive feedback to the operator. Since all the engineering system parameters are available via the cross-platform CSS based user interface, the users of the system are provided with substantial diagnostic ability and remote reconfigurability that was not previously possible.

The modular design allows for easy maintenance, as all of the modules can be quickly removed and replaced without making any hardware adjustments and all of the RF signals are quickly accessible for diagnostic purposes though the sub-miniature version A (SMA) links on the front panels.

The I/O capability of the system was extended via EPICS channel access and was aided by the adoption and implementation of the EtherCAT industrial communication standard to control all the tunable RF elements in the power amplifiers, such as the grid and anode circuits, and the tunable elements within the resonators, such as the coupling capacitors, short-circuit plates, and auto-tune trimmer capacitors.

This combination of the new digital low-level RF control system and the EtherCAT based motion control allowed all the RF control systems at iThemba LABS to be efficiently upgraded and this improved the operating efficiency of the complete cyclotron complex. As a further indicator of the success of the system and ease of implementation and adaptability, it was also installed and commissioned on the Helmholtz-Zentrum in Berlin's K=132 separated sector cyclotron enabling the continued treatment of patients and the execution of physics experiments.

The performance and operational history of the installed systems is discussed in the following chapter.

Chapter 4

Operational History and Performance

The operational history and performance of the new RF control system is discussed in this chapter. The first section briefly discusses the operational history in the chronological order in which the RF systems were upgraded, whilst the complete operational history of all the systems has been tabulated in Appendix E. The second section discusses the performance of the systems.

4.1 Operational History

The primary development of the new control system occurred on SPC2. It has the longest track record as it was the first system that was upgraded (November 2014), followed by SPC1 (October 2016), the Helmholtz-Zentrum Berlin's cyclotron (April 2017), the AX and K-line bunchers (May 2017) and the remaining systems in June 2017.

4.1.1 SPC2

SPC2 is primarily used as the injector cyclotron for particle beams to the SSC used in physics experiments. Development of the beam starts on Wednesday and must be operational by Friday. Experiments would usually run from Friday until Monday morning when another energy change occurs.

The first prototype systems were commissioned on the north and south RF systems of SPC2 in November 2014. During the commissioning, patch panels were installed, thereby making it possible to switch back to the legacy control systems. Testing and optimization of the systems and control algorithms continued for two days of each week until the end of January 2015. During this period, the legacy control system was used for the weekend experiments.

Once the new system was fully qualified, the decision was made to use it for all operations. The first operational beam that was produced and injected into the SSC was 175 MeV $^{40}Ar^{7+}$ on 6 February 2015. Since then, a total of 77 particle beams have been produced up until 19 October 2017. The lowest and highest

frequencies of operation have been 11.379999 MHz in the production of a 120 MeV $^{4}He^{2+}$ beam using 4.2 kW forward power and 26.000645 MHz in the production of a 51.4 MeV $^{3}He^{1+}$ beam using 8.8 kW forward power. The lowest and highest forward power used during operation were 2.1 kW to produce a 134 MeV $^{36}Ar^{7+}$ beam and 21.3 kW to produce a 200 MeV proton beam at 26 MHz. The system performed without error for all 77 particle beams.

4.1.2 SPC1

After the successful commissioning and operation on SPC2, work began on procuring components and manufacturing 35 production versions of the new RF control system. The final assembly of these systems began in August 2016. SPC1 was upgraded in October 2016 and has been fully operational since 1 November 2016.

SPC1 is primarily used as the injector cyclotron for particle beams to the SSC for isotope production and neutron therapy. The systems are typically in operation from Monday to Friday. Occasionally, SPC1 is also used for physics experiments on weekends.

In total 47 particle beams have been produced. The lowest and highest frequencies of operation have been 10.880840 MHz for the production of a 27 MeV H^{+} beam using 7 kW forward power and 26 MHz for the production of 200 MeV H^{+} beam using 14 kW forward power.

4.1.3 The AX, K and J-line Bunchers and the Pulse-selector

The AX and K-line bunchers were successfully upgraded in the middle of May 2017 and were first used on 8 June 2017.

The lowest and highest frequencies of operation for the AX-buncher have been 12.585160 MHz for the production of a 86 MeV $^{22}Ne^{4+}$ beam using 2.5 W forward power and 21.898982 MHz for the production of 48 MeV $^{4}He^{2+}$ beam using 3 W forward power.

The lowest and highest frequencies of operation for the K-buncher have been 25.170320 MHz for the production of a 86 MeV $^{22}Ne^{4+}$ beam using 2.2 kW power and 43.797964 MHz for the production of 48 MeV $^{4}He^{2+}$ beam using 2.5 kW power.

The J-line buncher was successfully upgraded during the June 2017 maintenance period. The lowest and highest frequencies of operation have been 21.761680 MHz to produce a 27 MeV H^{+} beam using 3.9 kW power and 52 MHz to produce a 200 MeV H^{+} beam using 4 kW power. The system has operated a total of 18 occasions during the period 17 July 2017 to 20 October 2017.

The pulse-selector RF system was also successfully upgraded during the June 2017 maintenance period. The lowest and highest frequencies of operation for the pulse-selector have been 2.720210 MHz for the production of a 27.5 MeV H^{+} beam using 200 W forward power and 3.128426 MHz for the production of 48 MeV $^{4}He^{2+}$ beam using 183 W forward power.

4.1.4 SSC

The SSC RF systems were successfully upgraded during the June 2017 maintenance period. In total 18 particle beams have been produced between 17 July 2017 and 20 October 2017. The lowest and highest frequencies of operation have been 10.880840 MHz for the production of a 27 MeV H^+ beam using 33 kW forward power and 26 MHz for the production of a 200 MeV H^+ beam using 72 kW forward power.

4.1.5 SSC Flat-topping

The SSC flat-topping RF system was also successfully upgraded during the June 2017 maintenance period. The flat-topping is a fixed frequency system and is only used when 66 MeV H^+ beams are produced for isotope production. The system has operated a total of 10 occasions during the period 17 July 2017 to 20 October 2017.

4.1.6 The Helmholtz-Zentrum Berlin's Separated Sector Cyclotron

The RF systems of the north and south resonator of the HZB separated sector cyclotron were successfully upgraded in the first week of April 2017. The systems were shipped from South Africa pre-configured in the middle of March 2017. After their arrival, the final software configuration occurred remotely from South Africa. As part of this project, all motion control of the RF systems were upgraded by the HZB team to an EtherCAT solution similar to that used at iThemba LABS. The final commissioning was done on site. The installation was done in a manner similar to the upgrade of SPC2 with patch panels giving the ability to switch between the previous and the new control system. During the commissioning week, the RF control systems were tested at four different frequencies which the HZB operators have used in recent years. Following a testing and qualification period by the HZB team, the systems were successfully used to produce proton beams to treat patients, with a total of 53 patients treated by 25 August 2017.

4.2 Operational Performance

The following section discusses the operational performance of the new control system. The focus is primarily on SPC2 as this is the system on which the new RF control system was developed. SPC2 is also the only system that is available to do measurements during the week without interrupting the 24/7 operating schedule. Further focus is placed on the performance of the SSC as it has the most demanding requirements. The performance of the systems implemented for Helmholtz-Zentrum Berlin's cyclotron is also discussed. Lastly the improved performance and efficiency of the complete cyclotron facility at iThemba LABS is discussed.

4.2.1 A Comparison of the Legacy and New Systems on SPC2

A comparison of the performance of the legacy and the new control systems was performed at 12.228267 MHz. This frequency was chosen because SPC2 was scheduled to operate at this frequency for 3 consecutive weekends. This made it easier to change between control systems. The comparison was performed with 2.6 kW forward power delivered to the south side resonator.

The normalized magnitude spectrum of the signals at the RF pick-up under closed-loop control was used to compare the two systems. The measured spectra are shown in Fig. 4.1.

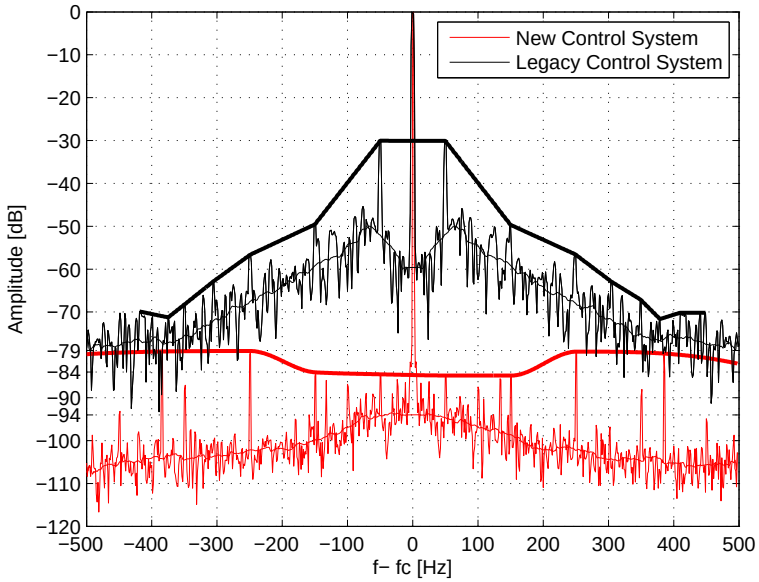

Figure 4.1: A comparison of the normalized magnitude spectra of SPC2 south resonator under closed-loop control at 12.228267 MHz using the legacy and the new control system.

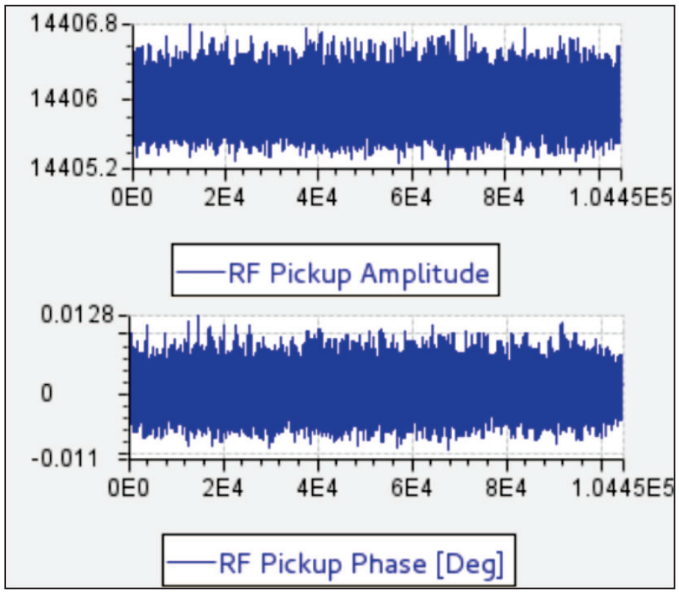

Figure 4.2: The measured amplitude and phase of the RF pick-up signal for the new control system during the test at 12.228267 MHz shown in Fig. 4.1.

The normalized magnitude spectrum of the legacy control system is illustrated in black and the new control system in red. The plot also includes the envelope of the normalized magnitude spectra, which indicates the spurious free dynamic range (SFDR). The filtered noise floor is shown, which gives an indication of each system's noise floor.

The legacy control system has a SFDR of 30 dB which is a result of the 50 Hz side lobes injected into the system by the synthesizer. The signal to noise ratio (SNR) close to the carrier is 60 dB. This corresponds to the previously reported amplitude stability of 0.1% (Conradie, 2004). The SNR away from the carrier decreases to 50 dB and only reaches 60 dB again at approximately 150 Hz.

With the new control system, SPC2 south resonator operates with a SFDR of 79 dB 250 Hz away from the carrier and with a SFDR of 84 dB within 150 Hz of the carrier. The mean noise floor close to the carrier is approximately -94 dBc. The SFDR improvement of the new over the old system close to the carrier is therefore 54 dB and the wideband improvement of the SFDR is 49 dB.

The new control system communicates amplitude and phase measurements to the Control System Studio Client (CSS) at a data rate of 2.5 kHz. Figure 4.2 shows 41 seconds of amplitude and phase information captured during the magnitude spectrum measurement shown in Fig. 4.1. From Fig. 4.2 we see that the peak-peak amplitude stability is 1.6/14406 and at the same time the peak-peak phase stability is 0.0238°.

4.2.2 Best System Performance on SPC2

The performance of the control system is dependent on the mechanical stability of the load resonator. For SPC2 (as described in section 2.2.2), the mechanical stability of the resonator is greatest when the short-circuit plates are closest to the dees which corresponds to the highest operating frequency of 26 MHz. The best closed-loop amplitude and phase stability can be achieved at this frequency.

Figure 4.3 shows a peak-peak amplitude and phase stability of greater than 0.01% and 0.01° respectively for 100 seconds.

The normalized magnitude spectrum for closed-loop and open-loop operation with 12.6 kW on load at 26 MHz is shown in Fig. 4.4. The SNR under closed-loop control close to the carrier is greater than 80 dB and the SFDR has improved from 58 dB in open-loop to greater than 80 dB in closed-loop mode which corresponds to the amplitude stability shown in Fig. 4.3.

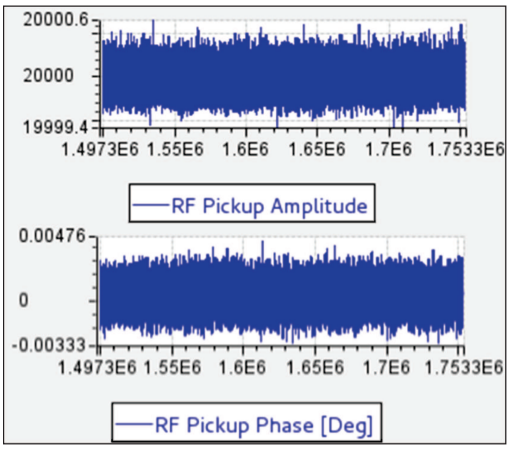

Figure 4.3: The RF amplitude and phase measurements of SPC2 south resonator under closed-loop control at 26 MHz with 12.6 kW power delivered to the resonator.

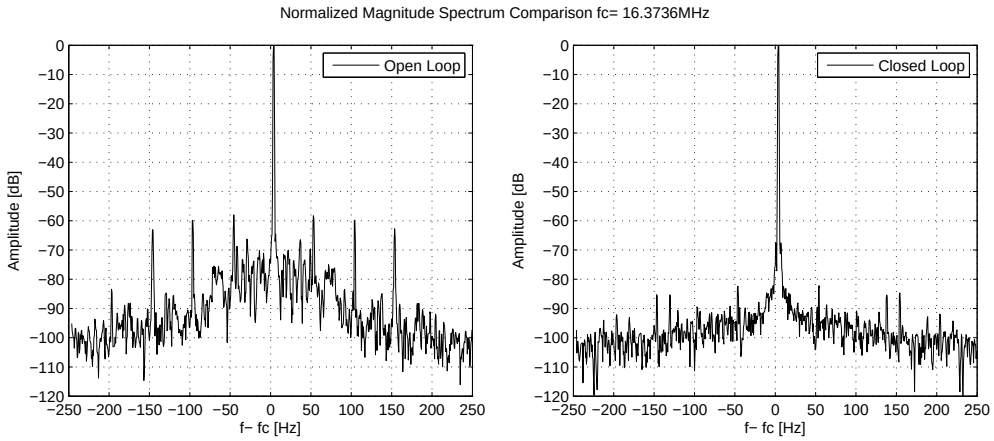

Figure 4.4: The closed-loop and open-loop magnitude spectrum of SPC2 south resonator at 26MHz with 12.6 kW power delivered to the resonator.

4.2.3 A Comparison of the Legacy and New Systems on the SSC

In this section a comparison of the performance of the legacy and new control systems for the SSC is performed at 16.3736 MHz. This frequency is chosen as it is the frequency used to produce 66 MeV proton beams with high current intensity for isotope production. As with the analysis for SPC2, the normalized magnitude spectrum of the RF pick-up signals under closed-loop control is used to compare the two systems. The west and east resonators perform identically, only the performance of the control systems on the west resonator is analyzed here.

The normalized magnitude spectrum for 62 kW RF power delivered to the west Resonator during operation is shown in Fig. 4.5 with a frequency span of 1 kHz. The normalized magnitude spectrum of the legacy control system is illustrated in black and the new system in red.

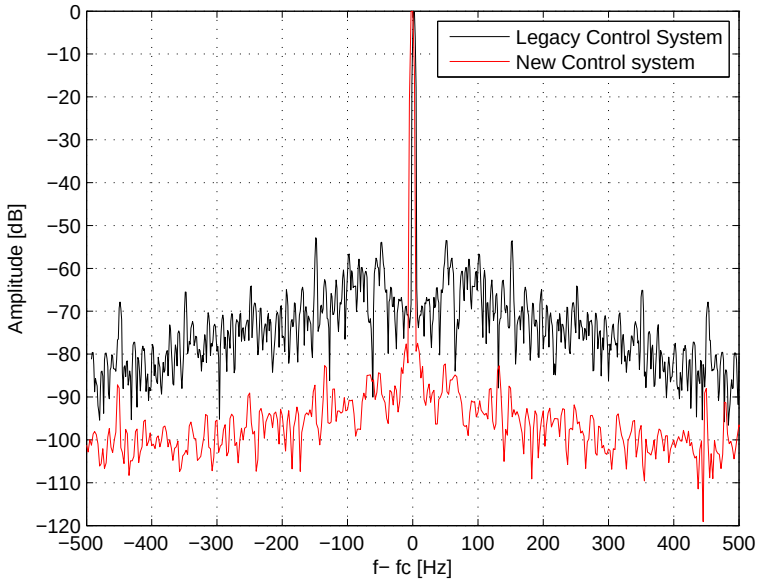

Figure 4.5: A comparison of the closed-loop magnitude spectra for the legacy and new control system over a span of 1 kHz of the SSC west resonator at 16.3736MHz with 62 kW power delivered to the resonator.

The legacy control system has a SNR of 70 dB close to the carrier. The SNR away from the carrier decreases to 53 dB and only reaches 70 dB again at approximately 300 Hz. The SFDR is better than that achieved for SPC2 with a maximum of 52dB at 150 Hz which improves to 68 dB at 450 Hz away from the carrier.

The new control system performs significantly better than the legacy control system with a SNR and SFDR of greater than 80 dB over the full span.

Figure 4.6 shows 14 seconds of amplitude and phase information captured during the magnitude spectrum measurement in Fig. 4.5. From Fig. 4.6 the peak-peak

amplitude stability is 2/21403 (0.0093%) and the peak-peak phase stability is better than 0.004°.

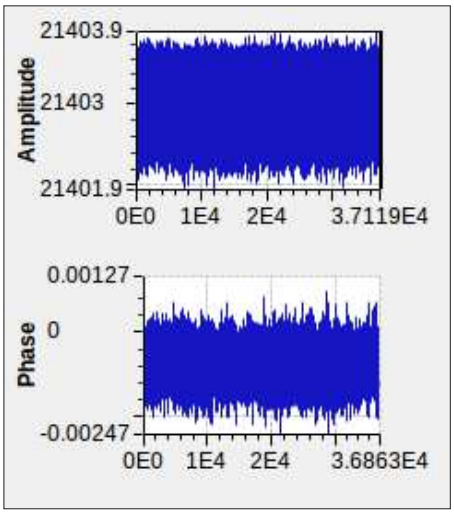

Figure 4.6: The measured amplitude and phase of the RF pick-up signal for the new control system during the test at 16.37636 MHz for 66 MeV protons with a current intensity of 210µA on target at isotope production.

4.2.4 The Open and Closed-loop Performance on the SSC

In this section a comparison of the open and closed loop performance of the new control systems for the SSC west resonator is performed at 16.3736 MHz. As in the previous section, this frequency was chosen because it is the frequency used to produce 66 MeV proton beams with high current intensity for isotope production.

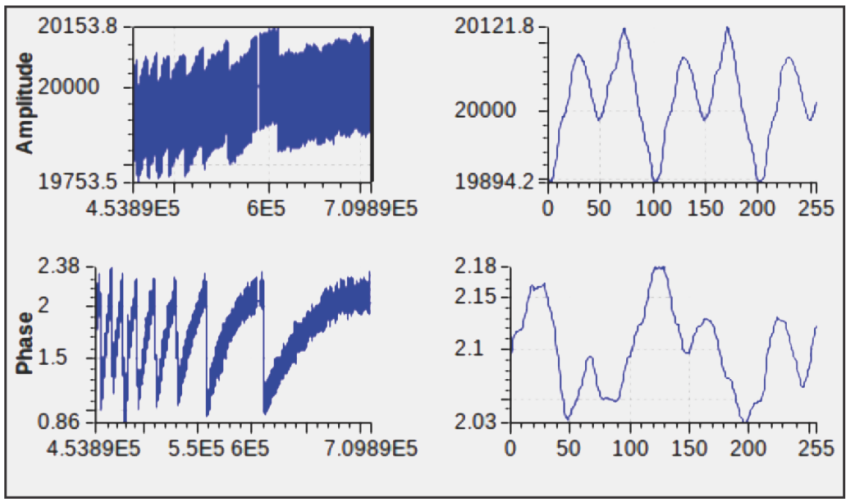

Figure 4.7: The RF amplitude and phase measurements for the SSC west resonator under open-loop control at 16.3736 MHz with 59kW delivered to the resonator.

For both modes, the amplitude reference is set to 20000 which corresponds to 59 kW forward power and the phase reference is set to 0°. Fig. 4.7 illustrates the long term open-loop stability for 100 seconds and the short term stability for 0.1 seconds. The long term peak-peak open-loop amplitude and phase stability for 100 seconds is 400/20000 (2%) and 1.52°. The short-term open-loop amplitude and phase stability is 227.6/20000 (1.138%) and 0.15°.

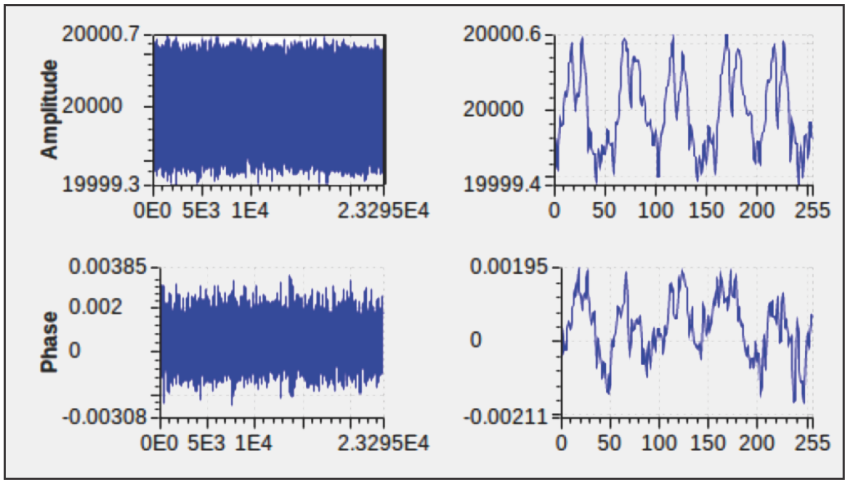

Figure 4.8: The RF amplitude and phase measurements for the SSC west resonator under closed-loop control at 16.3736 MHz with 59 kW delivered to the resonator.

Fig. 4.8 illustrates the long term closed-loop stability for 9 seconds and the short term stability for 0.1 seconds. The long term peak-peak closed-loop amplitude and phase stability is 1.4/20000 (0.007%) and 0.007°. The closed-loop short-term amplitude and phase stability is 1.2/20000 (0.006%) and 0.004°.

The corresponding open and closed-loop normalized magnitude spectrum is shown for a span of 500 Hz and 2 kHz in Figs. 4.9 and 4.10. These magnitude spectra confirm excellent performance of the new RF control system since the SNR under closed-loop control is significantly better than 80 dB over the full 2 kHz span. The SFDR improves from 55 dB in open-loop mode to better than 80 dB over the full 2 kHz span.

It is clear that the system performs better than the best case for SPC2. This can be attributed to the higher quality commercial power amplifiers that are in use in the SSC, the vertical configuration of the $\lambda/2$ resonators as opposed to horizontal configuration of the $\lambda/4$ resonators used in SPC2 and also the greater attention paid to mechanical stability during the design of the SSC.

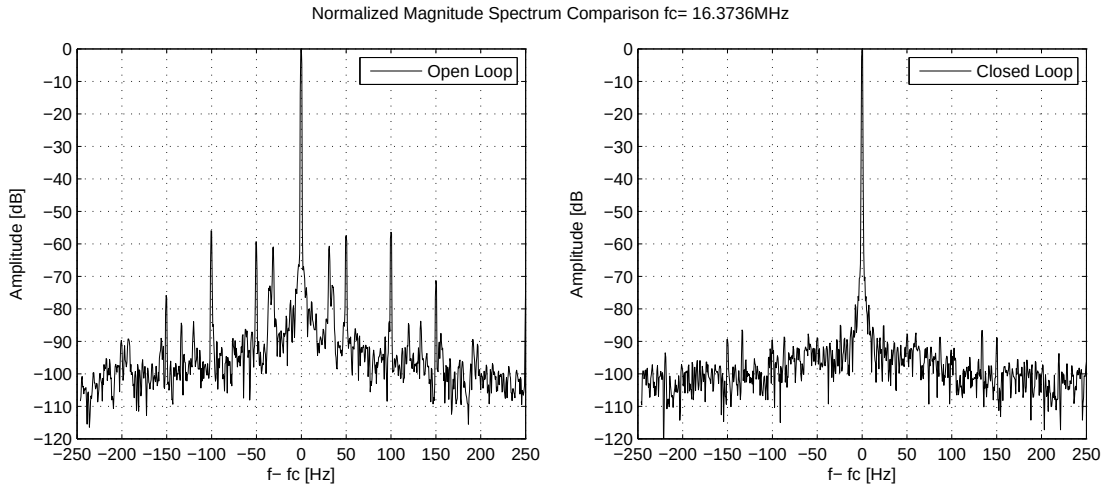

Figure 4.9: The open-loop (left) and closed-loop (right) magnitude spectra with a span of 500 Hz for the SSC west resonator at 16.3736 MHz with 59 kW power delivered to the resonator

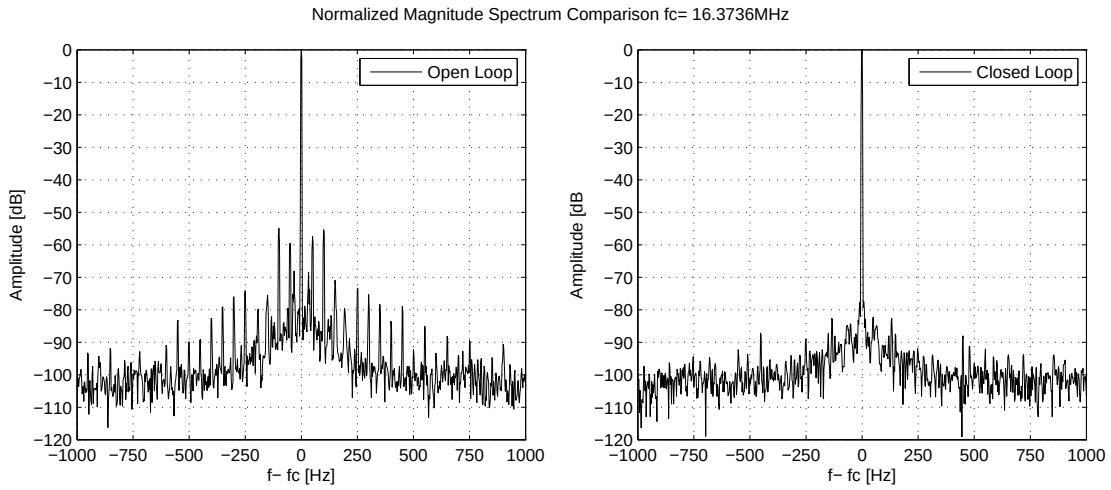

Figure 4.10: The open-loop (left) and closed-loop (right) magnitude spectra with a span of 2 kHz for the SSC west resonator at 16.3736 MHz with 59 kW power delivered to the resonator

4.2.5 Performance at the Helmholtz-Zentrum Berlin

Figures 4.11 and 4.12 show the open loop stability of the new system installed at the HZB north and south resonator at 19.3178 MHz with a 50% voltage of 40 kV respectively. This frequency is used for radiotherapy with 68 MeV protons. The peak-to-peak open-loop amplitude stability for the north and south resonator is 13.2% (-17.6 dB) and 6.7% (-23.5 dB), respectively. The peak-to-peak open-loop phase stability for the north and south resonator is 9.93° and 5.85°, respectively.

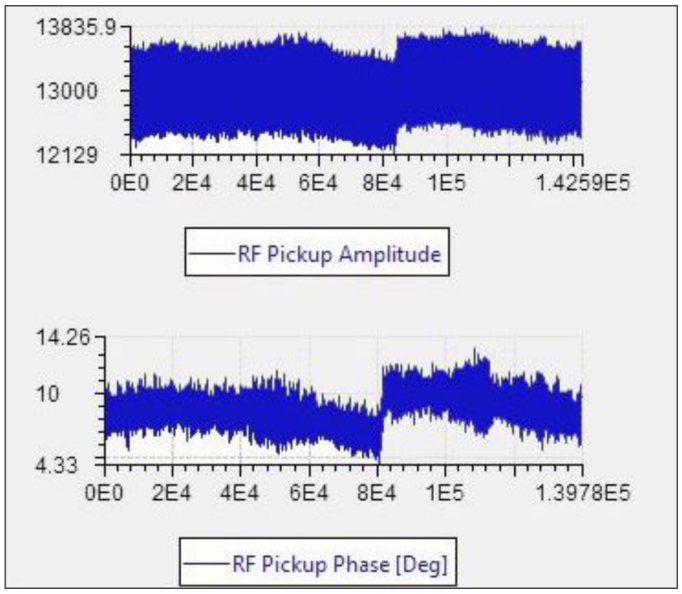

Figure 4.11: The RF amplitude and phase measurements taken at the HZB north resonator under open-loop conditions at 19.3178 MHz with a dee voltage of 40 kV.

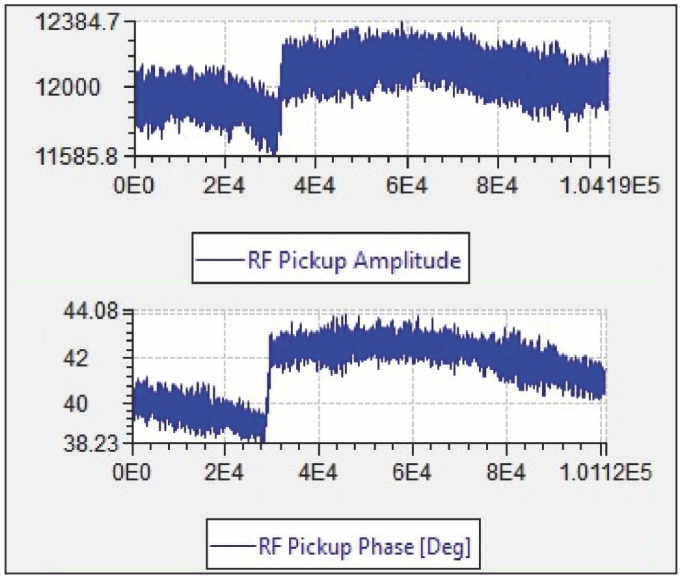

Figure 4.12: The RF amplitude and phase measurements taken at the HZB south resonator under open-loop conditions at 19.3178 MHz with a dee voltage of 40 kV.

In closed-loop mode, the peak-to-peak amplitude and phase stability improves to 0.0752% (-62.4777 dB) and 0.12° for the north resonator and to 0.1172% (-58.6186 dB) and 0.0400° for the south resonator, as illustrated in Figs. 4.13 and 4.14. In closed-loop mode the systems perform well. The systems are stable and as discussed in Section 4.1.6, have been used in three week long therapy sessions to treat patients. In comparison to iThemba LABS' RF systems the open-loop stability is significantly worse leaving much room for improvement in the stability

of the in-line components of their RF systems which would further improve the closed-loop stability.

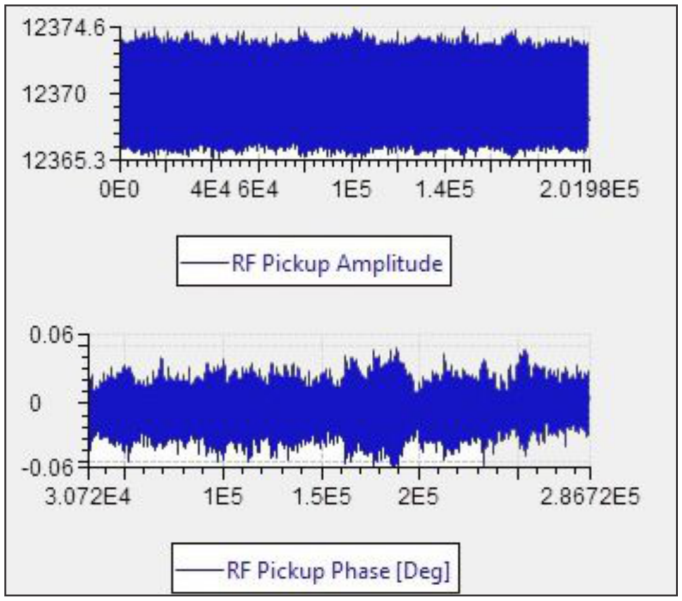

Figure 4.13: The RF amplitude and phase measurements taken at the HZB north resonator under closed-loop control at 19.3178 MHz with a dee voltage of 40 kV.

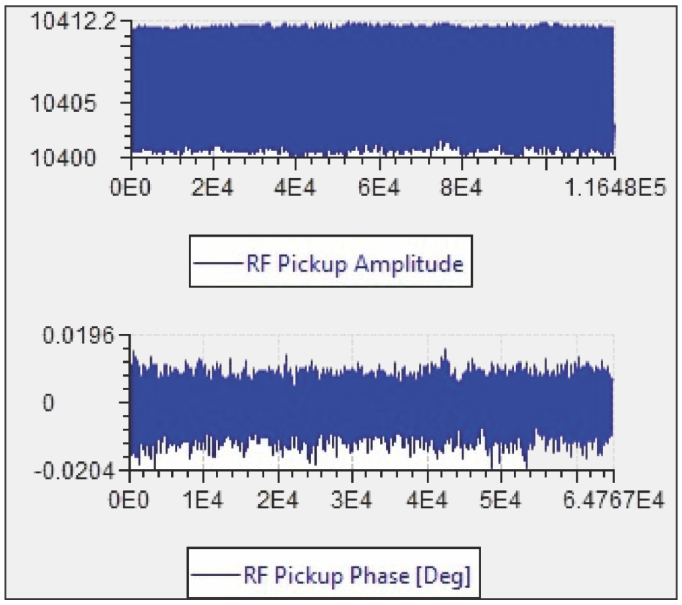

Figure 4.14: The RF amplitude and phase measurements taken at the HZB south resonator under closed-loop control at 19.3178 MHz with a dee voltage of 40 kV.

4.2.6 Improved Efficiency of the Separated Sector Cyclotron System

Following the integration of the new control systems into the J-line buncher, the SSC west and east RF systems, and the SSC Flat-topping system, a significant improvement in the efficiency of the SSC at iThemba LABS was noticed. It is thought that prior to the installation of these systems, the legacy RF control systems of the SSC west, east, flat-topping and J-line buncher were masking the effects of the improvements made on the RF systems of the injector cyclotrons.

The improvement on the efficiency of the complete system is most noticeable at high current intensities when 66 MeV proton beams are produced for isotope production.

Prior to the integration, it was difficult to achieve extraction current losses lower than 700-800 nA on the SPM1 and SPM2 extraction elements of the SSC with 220 µA on target. After the integration, the lowest losses achieved on both extraction elements were 13.1 nA for SPM1 and 18 nA for SPM2 with 227 µA on target.

With the beam losses at extraction reduced by more than 90%, one can expect that the activation of the extraction components will also drop by a similar margin. This significantly reduces the radiation dose that personnel who have to service these components would be exposed to during servicing and emergency repair.

Furthermore, due to the substantial reduction in beam losses at extraction, less time has to be spent on the optimization of the high intensity beam transmission through the SSC for isotope production, resulting in more beam availability for isotope production.

Over the years, significant effort has been made to achieve higher stability and intensity from the systems, with improvements being made to the PIG ion source, SPC1, the buncher systems (Conradie, 1992) and the addition of a flat-topping system to the SSC (De Villiers, 2009). The transmission efficiency of the SSC was last measured in 1989 after the improvements that were made to the ion source and J-line buncher. Following the addition of the SSC flat-topping system, the transmission efficiency was not measured and only the combined transmission efficiency of the flat-topping system and the new RF control systems was measured in 2017.

Fig. 4.15 illustrates the transmission efficiency as a percentage of the injection beam current for 66 MeV proton beams of measurements performed in 1988[1], 1989[1] and 2017. The first two represent the measurements before and after the improvements made to the ion source and J-line buncher in 1989. The 2017 graph represents the measurements taken after the integration with the new RF control systems as well as with the flat-topping system.

With the flat-topping and new RF control system, 100% transmission at 100 µA is achieved. This must be compared with 96.79 and 99.89% achieved in 1988 and 1989 respectively. At 197.3 and 240µA, efficiencies of 99.75 and 99.25% respectively can now be achieved. This is in comparison to 98.88 and 96.67% achieved in 1989. Unfortunately it was not possible to do higher current measurements in 2017 as additions to the safety control systems prohibited this.

[1] *The graphs and data points of 1988 and 1989 have been reproduced from Conradie (1992).*

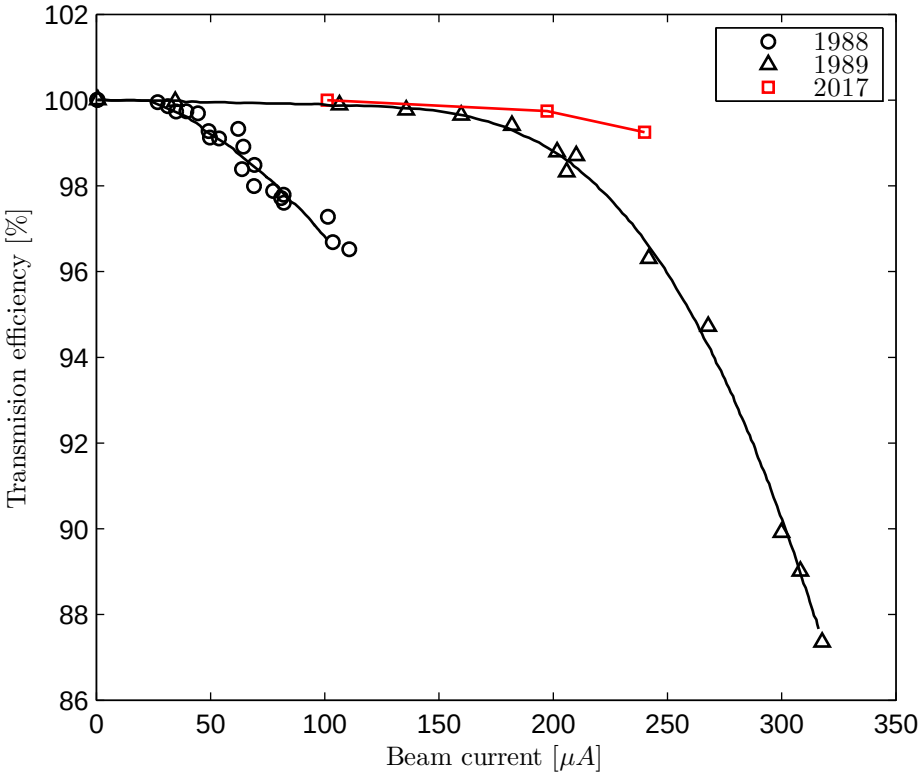

Figure 4.15: The transmission efficiency of the SSC for high current intensity 66 MeV proton beams for the 1988[1], 1989[1] and 2017 systems.

4.3 Conclusion

The success of the new digital low-level RF control system has been confirmed by the operational history and performance presented in this chapter. Since the commissioning of the prototypes on SPC2 in November 2014, a total of 77 particle beams have been successfully produced within specification for the period 6 February 2015 to 19 October 2017 where SPC2 served as the injector to the SSC primarily for physics experiments, ranging from an operational frequency of 11.379999 MHz in the production of a 120 MeV $^{4}He^{2+}$ beam to 26.000645 MHz in the production of a 51.4 MeV $^{3}He^{1+}$ beam.

A comparison of the legacy and new RF control system at 12.228267 MHz for SPC2 revealed a spurious free dynamic range (SFDR) improvement from 30 dB to 84 dB within 150 Hz of the carrier and to 79 dB 250 Hz away from the carrier, corresponding to peak-peak amplitude and phase stability of 0.0111% and 0.0238° respectively. Furthermore, at the highest operating frequency of 26 MHz where the mechanical stability of the resonators is greatest, a closed-loop peak-peak amplitude and phase stability of better than 0.01% and 0.01° respectively could be achieved. This is a factor of 10 improvement over the previously reported amplitude and phase stabilities of 0.1% and 0.1°.

[1] *The graphs and data points of 1988 and 1989 have been reproduced from Conradie (1992).*

Following the integration of the first of the production versions of the new RF control systems into the K=8 injector cyclotron, known as SPC1, in October 2016, 47 operational particle beams have been produced successfully and within specification. In these cases SPC1 functioned primarily as the injector to the SSC for 66 MeV proton beams with high current intensity for isotope production. However, occasionally the system was also used as the injector for proton and neutron therapy.

The AX and K-line bunchers were fitted with the new control system in May 2017 followed by the SSC west and east resonators, the SSC flat-topping, the J-line buncher and pulse-selector system in June 2017. All these systems have performed without fault since these upgrades. As a further measure of the performance improvement of the new RF control system over the legacy system, the SSC was evaluated during the production of 66 MeV proton beams with high current intensity for isotope production. The new system demonstrates a SNR of better than 80 dB over a 1 kHz span compared to the SNR of 70 dB close to the carrier and 53 dB at 150 Hz away from the carrier of the legacy system. The measured peak-peak amplitude and phase stability of the new system was better than 0.01% and 0.01°, respectively.

A substantial improvement in efficiency of the complete cyclotron complex at iThemba LABS was noticed at high current intensities when 66 MeV proton beams are produced for isotope production. Prior to the installation of the new control system it was difficult to achieve extraction current losses lower than 700-800 nA on the SPM1 and SPM2 extraction elements of the SSC with 220 µA on target. After the installation of the new control system, the lowest losses achieved on both extraction elements were 13.1 nA for SPM1 and 18 nA for SPM2 with 227 µA on target.

The reduction in losses by more than 90% results in lower activation of the extraction components. This significantly reduces the radiation dose that personnel who have to service these components would be exposed to during servicing and emergency repair.

The installation of the new RF control system across all the facilities at iThemba LABS will allow the laboratory to extend the lifetime of its facilities for the foreseeable future. Moreover, the improved efficiency paves the way for further experimentation into the production of radioisotopes with higher current intensities.

Finally, the RF systems of the north and south resonator of the Helmholtz-Zentrum Berlin's (HZB) separated sector cyclotron were successfully retrofitted with the system developed in this thesis in the first week of April 2017, demonstrating the system's adaptability and ease of integration with other cyclotron RF systems. HZB has been able to successfully produce proton beams with the new system to treat cancer patients with ocular tumors since 15 June 2017. A total of 53 have been treated using 68 MeV proton beams at an operating frequency of 19.3178 MHz over three week-long therapy sessions up until September 2017. The system was also used to produce a 50 MeV $^{3}He^{2+}$ beam at 19.8521 MHz for physics experiments. These systems should enable HZB to extend the lifetime of their cyclotron and enable them to continue to treat patients and to perform physics experiments for the foreseeable future.

Chapter 5

Summary and Conclusion

This thesis has set out the design and implementation of a new digital low-level RF (DLLRF) control system for the cyclotron particle accelerators at iThemba LABS. The objective was to achieve target peak-peak amplitude and phase stabilities of 0.01% and 0.01° respectively and to operate over the wide frequency range of 2-100 MHz.

The design was enabled by state-of-the-art field programmable gate arrays (FPGA), digital signal processing (DSP), high-speed digital to analog converters (DAC) and high-speed analog to digital converters (ADC).

By modifying and optimizing existing direct digital synthesis (DDS) techniques and by utilizing high-speed 16-bit DACs to directly convert the digital RF signals to analog signals, RF and local-oscillator (LO) signals with 16-bit amplitude accuracy and programmable in steps of 1 µHz and 0.0001° were achieved.

Down-conversion of the RF pick-up signals to an optimal intermediate frequency (IF) of 1 MHz and sampling of the IF channels by 16-bit, single sample-latency 10 MHz ADCs allows digital high-speed low-latency in-phase/quadrature (I/Q) demodulation of the IF channels within the FPGA, and enables efficient real-time digital closed-loop control of the amplitude and phase of the RF drive signal.

The modular design is easily maintainable, as all of the modules can be quickly removed and replaced without requiring any hardware adjustments and all of the RF signals are quickly accessible for diagnostic purposes through the sub-miniature version A (SMA) links on the front panels.

The efficient implementation of a Linux based experimental physics and industrial control system (EPICS) input/output controller (IOC), which communicates with the FPGA through memory mapped registers, provides a platform with a stable distributed control system allowing full automation using the EPICS based State Notation Sequencer and enabling the system to recover from most situations and with the augmented ability to find resonance.

The ability to display the amplitude and phase of the RF pick-up signal to the operator in real-time allows intuitive feedback. All the engineering system parameters are available via the cross-platform Control System Studio (CSS) based user interface, providing the users of the system with extensive diagnostic ability and remote reconfigurability that was not previously possible.

The integration of the RF control systems at iThemba LABS into the K=8 and

K=10 injector cyclotrons (SPC1, and SPC2), the K=200 separated sector cyclotron (SSC) west and east resonator systems, the SSC flat-topping system, the AX, J, and K-line RF bunchers and the pulse-selector system was successfully completed in July 2017.

The systems using the new control system with the longest track record are SPC1 and SPC2. A total of 77 particle beams have been produced successfully and within specification in the period 6 February 2015 to 19 October 2017, where SPC2 functioned as the injector to the SSC primarily for physics experiments, ranging from an operational frequency of 11.379999 MHz in the production of a 120 MeV $^{4}He^{2+}$ beam to 26.000645 MHz in the production of a 51.4 MeV $^{3}He^{1+}$ beam. A total of 47 operational particle beams have been produced successfully and within specification from SPC1 in the period 1 November 2016 to 20 October 2017, where SPC1 primarily functioned as the injector to the SSC for 66 MeV proton beams with high current intensity for isotope production and as the injector for proton and neutron therapy.

A comparison of the legacy and new RF control system on SPC2 at 12.228267 MHz revealed a spurious free dynamic range (SFDR) improvement from 30 dB to 84 dB within 150 Hz from the carrier and a 79 dB SFDR 250 Hz away from the carrier corresponding to a peak-peak amplitude and phase stability of 0.0111% and 0.0238° respectively. Furthermore, at the highest operating frequency of 26 MHz, where the mechanical stability of the resonators is greatest, closed-loop peak-peak amplitude and phase stabilities of greater than 0.01% and 0.01° respectively were achieved. This is a factor of 10 improvement over the previously reported amplitude and phase stabilities of 0.1% and 0.1°.

A further comparison of the legacy and new control system on the SSC during the production of 66 MeV proton beams with high current intensity for isotope production at an operating frequency of 16.3736 MHz revealed that the new system demonstrates an SNR of better than 80 dB over a 1 kHz span compared to the legacy system's SNR of 70 dB close to the carrier and a minimum SNR of 53 dB at 150 Hz offset from the carrier. At the same time, the measured peak-peak amplitude and phase stabilities of the new system was better than 0.01% and 0.01° respectively.

Not only has the RF stability greatly improved, but a significant improvement in efficiency of the complete cyclotron complex at iThemba LABS was observed at high current intensities when 66 MeV proton beams are produced for isotope production.

Prior to the integration of the new control system it was difficult to achieve extraction current losses lower than 700-800 nA on the SPM1 and SPM2 magnetic extraction elements of the SSC with 220 µA on target. Once the new system had been incorporated, the lowest possible losses achieved on both extraction elements were 13.1 nA for SPM1 and 18 nA for SPM2 with 227 µA on target. The reduction in losses by more than 90% results in lower activation of the extraction components. This significantly reduces the radiation dose that personnel who have to service these components would be exposed to during servicing and emergency repair.

The successful installation of the new RF control system across all the facilities at iThemba LABS will allow the laboratory to extend the lifetime of its facilities for the foreseeable future and the improved transmission efficiency paves the

way for further experimentation into the production of isotopes with high current intensities.

This combination of the new digital low-level RF control system and the EtherCAT based motion control has resulted in a highly adaptable and easily implementable solution. Not only have all the RF control systems at iThemba LABS been efficiently upgraded, but as a further indicator of the success of the system and ease of implementation and adaptability, the system was also installed and commissioned on the Helmholtz-Zentrum in Berlin's K=132 separated sector cyclotron, enabling the continued treatment of patients and execution of physics experiments for the foreseeable future.

5.1 Recommendations for Future Work

The modular design allows for numerous possible future upgrades and research applications. Extra routing has already been provided from the FPGA on the RF controller module to each of the system modules and to two spare system slots, allowing for expansion or possible redefinition of the modules for alternate configurations. In addition to the two 16-bit single ended data buses in use with the high-speed DACs, two 16-bit high-speed low-voltage differential signaling (LVDS) buses are routed from the FPGA via the backplane to the RF synthesizer module. This provides the opportunity for the high-speed DACs to be changed to different technologies in future and therefore possibly extend the frequency range of the system. At the same time, the RF amplifiers and mixers could be swapped with modules that operate with a higher frequency range, thereby allowing down-conversion to be applied to the same 1MHz IF.

It may also be possible to extend the frequency range of the system by changing the low-pass filters on the outputs of the current DACs to band-pass filters and using an aliased image of the DAC outputs to extend the operating frequency.

If the frequency range is successfully extended, the system could possibly be applied to higher frequency accelerators. At the same time, the internal software of the controller could be reconfigured to operate in a pulsed mode, thereby allowing the system to operate on alternate particle accelerator technologies such as linacs.

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Appendices

Appendix A

Effect of RF Dee Voltage Stability on the Performance of Cyclotrons

The equations for the energy spread and the radial change per turn of a beam are derived to describe and analyze the effects of the RF voltage's amplitude and phase noise on the performance of an isochronous cyclotron with and without flat-topping. In each case, equations are derived for the ideal case without noise and then with noise.

A.1 Isochronous Cyclotron without Flat-topping

The energy gain per turn for particles with phase $\frac{\Delta\theta}{2}$ with respect to the central particle in an isochronous cyclotron with two resonators, both with two acceleration gaps, is given by the following equation (Conradie, 1992):

$$E_g = 2Q\left[\sum_{i=1}^{2} V_{Di}\cos(2\pi ft + \phi_i + \frac{\Delta\theta}{2})\right] \tag{A.1}$$

with

Q = the charge of the particle,
f = the RF frequency,
V_{Di} = the dee RF voltage,
ϕ_i = the phase of the RF voltage on the dee,
$\frac{\Delta\theta}{2}$ = the maximum phase deviation with respect to the central particle.

In the ideal case, simplifications can be made to Eqn. A.1 for analysis of the beam pulse in the $\Delta E - \Delta\theta$ phase plane by considering each dee's voltage and phase to be equal. Eqn. A.1 then reduces to:

$$E_g = 4QV_D\cos(2\pi ft + \phi + \frac{\Delta\theta}{2}) \tag{A.2}$$

with

V_D=V_{D1}=V_{D2} = the dee RF voltage,
ϕ=ϕ_1=ϕ_2 = the phase of the RF voltage on the dee,
$\frac{\Delta\theta}{2}$ = the maximum phase deviation with respect to the central particle.

The maximum energy gain will occur when $2\pi ft$ is an integer multiple of 2π and when ϕ=0. Eqn. A.2 can then be reduced to:

$$E_g = 4QV_D \cos(\frac{\Delta\theta}{2}) \tag{A.3}$$

The maximum energy gain of the central particle is defined as:

$$E_{g\_max} = 4QV_D \tag{A.4}$$

The ideal energy spread for an isochronous cyclotron without flat-topping can then be defined as:

$$\frac{\Delta E}{E} = \frac{E_g - E_{g\_max}}{E_{g\_max}} = \cos\left(\frac{\Delta\theta}{2}\right) - 1 \tag{A.5}$$

Where $\frac{\Delta\theta}{2}$ is the maximum phase deviation with respect to the central particle.

However, Eqns. A.1, A.2, A.3 and A.5 do not take into account the RF voltage's amplitude and phase noise. Eqn. A.1 can be reformatted as follows to take these into account:

$$E_{g+n} = 2Q\left[\sum_{i=1}^{2}\left[V_{Di} + \frac{V_{ni}(t)}{2}\right]\cos(2\pi ft + \phi_i + \frac{\phi_{ni}(t)}{2} + \frac{\Delta\theta}{2})\right] \tag{A.6}$$

with

$V_{ni}(t)$ = the time varying amplitude noise of the RF voltage on each dee with a peak-peak amplitude of V_{ni}, and
$\phi_{ni}(t)$ = the time varying phase noise of the RF voltage for each dee with a peak-peak amplitude of ϕ_{ni}.

Eqn. A.6 can be simplified by assuming that the dee voltages and phases are equal. In this case, the amplitude noise for each dee can be simplified to a quantity that represents the maximum noise of either dee's amplitude noise and the phase noise of each dee can be simplified to a variable that represents the maximum phase noise of either dee as in Eqn A.7 below:

$$E_{g+n} = 4QV_D\left[1 + \frac{V_n(t)}{2V_D}\right]\cos(2\pi ft + \phi + \frac{\phi_n(t)}{2} + \frac{\Delta\theta}{2}) \tag{A.7}$$

with

V_D=V_{D1}=V_{D2} = the dee RF voltage,

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ϕ=ϕ_1=ϕ_2 = the phase of the RF voltage on the dee,
$V_n(t)$ = $max(V_{n1}(t), V_{n2}(t))$
= the maximum amplitude noise for either dee with a peak-peak amplitude of V_n, and
$\phi_n(t)$ = $max(\phi_{n1}(t), \phi_{n2}(t))$= the phase noise of the RF voltage for either dee with a peak-peak amplitude of ϕ_n.

As with Eqn A.2 it is clear that the maximum energy gain will occur when $2\pi ft$ is an integer multiple of 2π and when ϕ=0. This allows Eqn. A.7 to be reduced to:

$$E_{g+n} = 4QV_D\left[1 + \frac{V_n(t)}{2V_D}\right]\cos(\frac{\phi_n(t)}{2} + \frac{\Delta\theta}{2}) \tag{A.8}$$

An equation for the minimum energy gain with respect to the envelopes of the noise components can be derived when $V_n(t) = -\frac{V_n}{2}$ and $\phi_n(t) = \frac{\phi_n}{2}$:

$$E_{g+n\_min} = 4QV_D\left[1 - \frac{V_n}{2V_D}\right]\cos(\frac{\phi_n}{2} + \frac{\Delta\theta}{2}) \tag{A.9}$$

An equation for the maximum energy gain with respect to the envelopes of the noise components can be derived when $V_n(t) = \frac{V_n}{2}$, $\phi_n(t) = 0$ and $\Delta\theta = 0$.

$$E_{g+n\_max} = 4QV_D\left[1 + \frac{V_n}{2V_D}\right] \tag{A.10}$$

From Eqns. A.4, A.9 and A.10 the energy spread can now then be defined as:

$$\begin{aligned}\frac{\Delta E}{E} &= \frac{E_{g+n\_min} - E_{g+n\_max}}{E_{g\_max}} \\ &= \left[1 - \frac{V_n}{2V_D}\right]\cos(\frac{\phi_n}{2} + \frac{\Delta\theta}{2}) - \left[1 + \frac{V_n}{2V_D}\right]\end{aligned} \tag{A.11}$$

with

V_D = the dee RF voltage,
$\frac{\Delta\theta}{2}$ = the maximum phase deviation with respect to the central particle,
V_n = the maximum peak-peak amplitude noise of the RF voltage and
ϕ_n = the maximum peak-peak phase noise of the RF voltage.

A.2 Isochronous Cyclotron with Flat-topping

The energy spread of an isochronous cyclotron can be improved by the addition of an n^{th} harmonic RF voltage. At iThemba LABS, a fixed- frequency 3$^{\text{rd}}$ harmonic flat-topping system is used on the SSC to improve the 66 MeV proton beam intensity for isotope production.

The following section first derives the ideal energy spread for an n^{th} harmonic flat-top system and then the energy spread when including RF amplitude and phase noise. Thereafter the energy spread for the 3^{rd} harmonic flat-topping system of the SSC is derived.

The energy gain per turn for particles with phase $\frac{\Delta\theta}{2}$ with respect to the central particle in an isochronous cyclotron with two resonators, both with two acceleration gaps and n^{th} harmonic flat-topping can be represented as follows (Conradie, 1992; De Villiers, 2009):

$$E_g = 2Q\left[\sum_{i=1}^{2} V_{Di}\cos(2\pi ft + \phi_i + \frac{\Delta\theta}{2}) - V_F\cos(2\pi nft + n\phi_F + n\frac{\Delta\theta}{2})\right] \quad \text{(A.12)}$$

with

Q	=	the charge of the particle,
f	=	the cyclotron RF frequency,
V_{Di}	=	the main dee RF voltage,
ϕ_i	=	the phase of the RF voltage on the dee,
$\frac{\Delta\theta}{2}$	=	the maximum phase deviation with respect to the central particle,
V_F	=	the flat-topping RF voltage amplitude,
$n\phi_F$	=	the phase of flat-topping RF voltage.

In the ideal case, simplifications can be made to Eqn. A.12 for analysis of the beam pulse in the $\Delta E - \Delta\theta$ phase plane by considering each dee's voltage and phase to be equal. Eqn. A.12 then reduces to:

$$E_g = 2Q\left[2V_D\cos(2\pi ft + \phi + \frac{\Delta\theta}{2}) - V_F\cos(2\pi nft + n\phi + n\frac{\Delta\theta}{2})\right] \quad \text{(A.13)}$$

with

V_D=V_{D1}=V_{D2}	=	the dee RF voltage,
ϕ=ϕ_1=ϕ_2	=	the phase of the RF voltage on the dee.

The ideal energy gain will occur when $2\pi ft$ and $2\pi nft$ are integer multiples of 2π and when ϕ=0 and $n\phi_F$=0. In this case Eqn. A.2 reduces to:

$$\begin{aligned} E_g &= 4QV_D\cos(\frac{\Delta\theta}{2}) - 2QV_F\cos(n\frac{\Delta\theta}{2}) \\ &= 4QV_D\left[\cos(\frac{\Delta\theta}{2}) + k\cos(n\frac{\Delta\theta}{2})\right] \end{aligned} \quad \text{(A.14)}$$

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For a flat-top waveform, the second derivative of E_g, with respect to $\Delta\theta$, must be 0 (Conradie, 1992; Joho, 1968). This condition implies that $k = -\frac{1}{n^2}$. Substituting this value of k into Eqn. A.14 we find:

$$E_g = 4QV_D\left[\cos(\frac{\Delta\theta}{2}) - \frac{1}{n^2}\cos(n\frac{\Delta\theta}{2})\right] \tag{A.15}$$

The ideal energy gain will occur when $\Delta\theta = 0$ and is given by:

$$E_{g\_max} = 4QV_D\left[1 - \frac{1}{n^2}\right] \tag{A.16}$$

The ideal energy spread for an isochronous cyclotron with flat-topping can then be defined as:

$$\begin{aligned}\frac{\Delta E}{E} &= \frac{E_g - E_{g\_max}}{E_{g\_max}} \\ &= \frac{\cos(\frac{\Delta\theta}{2}) - \frac{1}{n^2}\cos(n\frac{\Delta\theta}{2})}{1 - \frac{1}{n^2}} - 1\end{aligned} \tag{A.17}$$

However Eqns. A.12 to A.17 do not take into account the RF voltage's amplitude and phase noise. Eqn.A.12 can be reformatted as follows to take these into account:

$$\begin{aligned}E_{g+n} =& 2Q\left[\sum_{i=1}^{2}\left[V_{Di} + \frac{V_{ni}(t)}{2}\right]\cos(2\pi ft + \phi_i + \frac{\phi_{ni}(t)}{2} + \frac{\Delta\theta}{2})\right. \\ &\left. - \left[V_F + \frac{V_{Fn}(t)}{2}\right]\cos(2\pi fnt + n\phi_F + \frac{\phi_{Fn}(t)}{2} + n\frac{\Delta\theta}{2})\right]\end{aligned} \tag{A.18}$$

with

Q	=	the charge of the particle,
f	=	the cyclotron RF frequency,
V_{Di}	=	each dee's RF voltage,
ϕ_i	=	the phase of the RF voltage on each dee,
$\frac{\Delta\theta}{2}$	=	the maximum phase deviation with respect to the central particle,
$V_{ni}(t)$	=	the time varying amplitude noise of the RF voltage on each dee with a peak-peak amplitude of V_{ni},
$\phi_{ni}(t)$	=	the time varying phase noise of the RF voltage for each dee with a peak-peak amplitude of ϕ_{ni},
V_F	=	the flat-topping RF voltage amplitude,
$n\phi_F$	=	the phase of the flat-topping RF voltage,
$V_{Fn}(t)$	=	the time varying amplitude noise of the flat-top RF voltage

$\phi_{Fn}(t) =$ with a peak-peak amplitude of V_{Fn}, the time varying phase noise of the flat-top RF voltage with a peak-peak amplitude of ϕ_{Fn}.

Equation A.18 can be simplified by assuming that the dee voltages and phases are equal. In this case, the amplitude noise for each dee can be simplified to a quantity that represents the maximum noise of either dee's amplitude noise and that the phase noise of each dee can be simplified to a variable that represents the maximum phase noise of either dee shown as in Eqn. A.19 below:

$$\begin{aligned} E_{g+n} =& 4QV_D\left[1+\frac{V_n(t)}{2V_D}\right]\cos(2\pi ft+\phi+\frac{\phi_n(t)}{2}+\frac{\Delta\theta}{2}) \\ &- 2QV_F\left[1+\frac{V_{Fn}(t)}{2V_F}\right]\cos(2\pi fnt+n\phi_F+\frac{\phi_{Fn}(t)}{2}+n\frac{\Delta\theta}{2}) \end{aligned} \tag{A.19}$$

with

$V_D{=}V_{D1}{=}V_{D2}$	$=$	the dee RF voltage,
$\phi{=}\phi_1{=}\phi_2$	$=$	the phase of the RF voltage on the dee,
$V_n(t)$	$=$	$max(V_{n1}(t), V_{n2}(t))$
	$=$	the maximum amplitude noise for either dee, with a peak-peak amplitude of V_n,
$\phi_n(t)$	$=$	$max(\phi_{n1}(t), \phi_{n2}(t))$
	$=$	the maximum phase noise of the RF voltage for either dee with a peak-peak amplitude of ϕ_{Fn}.

As with Eqn. A.14 it is clear that the maximum energy gain will occur when $2\pi ft$ and $2\pi nft$ are integer multiples of 2π and when $\phi{=}0$ and $n\phi_F{=}0$. In this case, Eqn A.7 can be reduced to:

$$\begin{aligned} E_{g+n} &= 4QV_D\left[1+\frac{V_n(t)}{2V_D}\right]\cos(\frac{\phi_n(t)}{2}+\frac{\Delta\theta}{2}) \\ &\quad - 2QV_F\left[1+\frac{V_{Fn}(t)}{2V_D}\right]\cos(\frac{\phi_{Fn}(t)}{2}+n\frac{\Delta\theta}{2}) \\ &= 4QV_D\left[\left[1+\frac{V_n(t)}{2V_D}\right]\cos(\frac{\phi_n(t)}{2}+\frac{\Delta\theta}{2})\right. \\ &\quad \left. + k\left[1+\frac{V_{Fn}(t)}{2V_F}\right]\cos(\frac{\phi_{Fn}(t)}{2}+n\frac{\Delta\theta}{2})\right] \end{aligned} \tag{A.20}$$

As for the analysis of the ideal case in Eqn. A.14, for the second derivative of E_{g+n} with respect to $\delta\theta$ to be zero, it follows that $k=-\frac{1}{n^2}$ and hence Eqn. A.20 becomes:

APPENDIX A. EFFECT OF RF DEE VOLTAGE STABILITY ON THE PERFORMANCE OF CYCLOTRONS

$$E_{g+n} = 4QV_D\left[\left[1+\frac{V_n(t)}{2V_D}\right]\cos(\frac{\phi_n(t)}{2}+\frac{\Delta\theta}{2}) - \frac{1}{n^2}\left[1+\frac{V_{Fn}(t)}{2V_F}\right]\cos(\frac{\phi_{Fn}(t)}{2}+n\frac{\Delta\theta}{2})\right] \tag{A.21}$$

An equation for the minimum energy gain with respect to the envelopes of the noise components can be derived when $V_n(t) = -\frac{V_n}{2}$, when $\phi_n(t) = \frac{\phi_n}{2}$, when $V_{Fn}(t) = \frac{V_{Fn}}{2}$ and when $\phi_{Fn}(t) = \frac{\phi_{Fn}}{2}$:

$$E_{g+n\_min} = 4QV_D\left[\left[1-\frac{V_n}{2V_D}\right]\cos(\frac{\phi_n}{2}+\frac{\Delta\theta}{2}) - \frac{1}{n^2}\left[1+\frac{V_{Fn}}{2V_F}\right]\cos(\frac{\phi_{Fn}}{2}+n\frac{\Delta\theta}{2})\right] \tag{A.22}$$

An equation for the maximum energy gain with respect to the envelopes of the noise components can be derived when $V_n(t) = \frac{V_n}{2}$, when $\phi_n(t) = 0$, when $V_{Fn}(t) = -\frac{V_{Fn}}{2}$, when $\phi_{Fn}(t) = 0$ and when $\Delta\theta = 0$:

$$E_{g+n\_max} = 4QV_D\left[\left[1+\frac{V_n}{2V_D}\right] - \frac{1}{n^2}\left[1-\frac{V_{Fn}}{2V_F}\right]\right] \tag{A.23}$$

From Eqns. A.16, A.22 and A.23 the energy spread then becomes:

$$\begin{aligned}\frac{\Delta E}{E} &= \frac{E_{g+n\_min} - E_{g+n\_max}}{E_{g\_max}} \\ &= \frac{\left[1-\frac{V_n}{2V_D}\right]\cos(\frac{\phi_n}{2}+\frac{\Delta\theta}{2}) - \frac{1}{n^2}\left[1+\frac{V_{Fn}}{2V_F}\right]\cos(\frac{\phi_{Fn}}{2}+n\frac{\Delta\theta}{2})}{\left[1-\frac{1}{n^2}\right]} \\ &- \frac{\frac{V_n}{2V_D}+\frac{1}{n^2}\frac{V_{Fn}}{2V_F}}{\left[1-\frac{1}{n^2}\right]} - 1\end{aligned} \tag{A.24}$$

with

V_D = the dee RF voltage,
V_F = the flat-top RF voltage,
$\frac{\Delta\theta}{2}$ = the maximum phase deviation with respect to the central

particle,

V_n = the maximum peak-peak amplitude noise of the dee RF voltage,

ϕ_n = the maximum peak-peak phase noise of the dee RF voltage,

V_{Fn} = the maximum peak-peak amplitude noise of the flat-top RF, voltage and

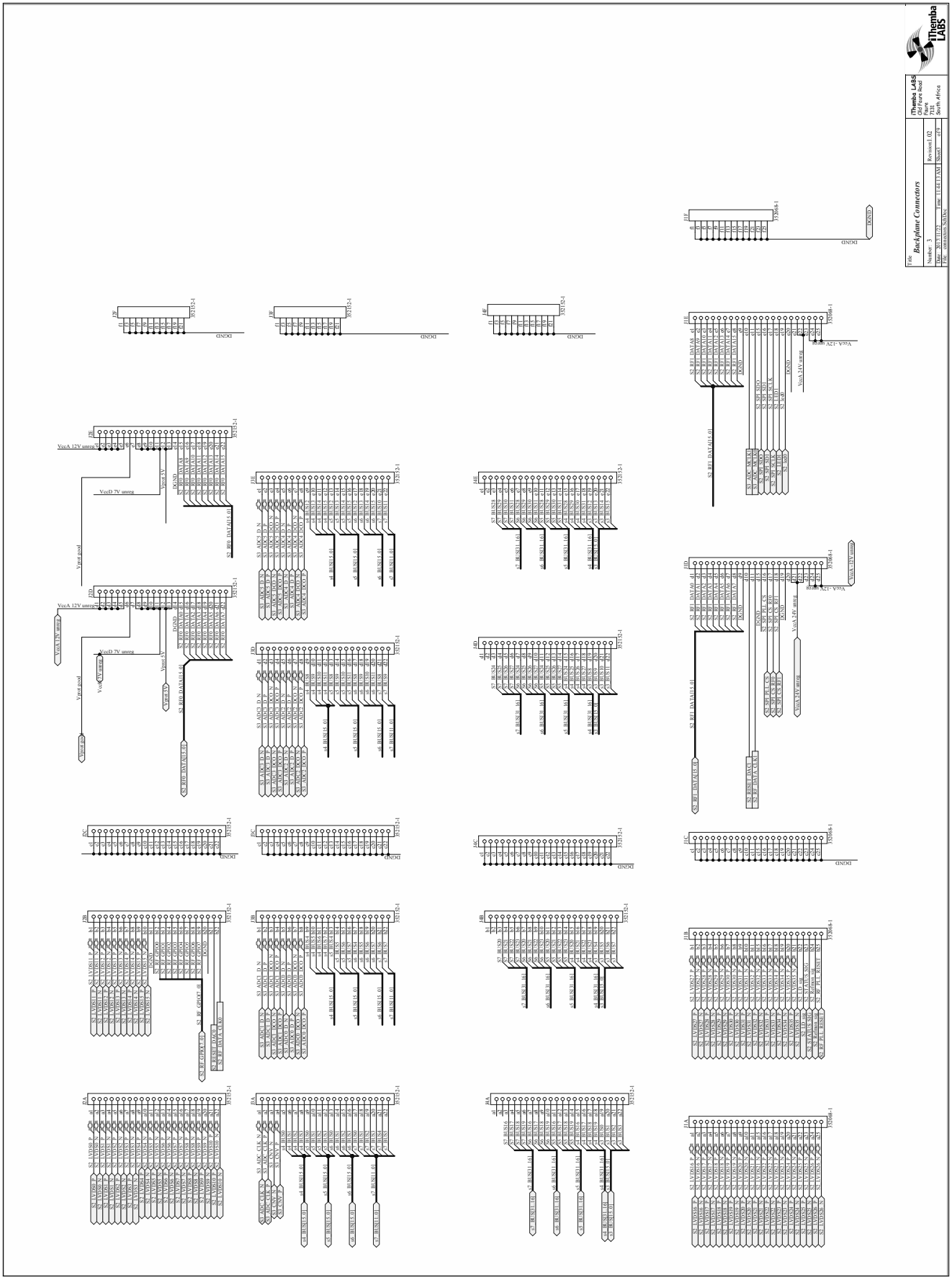
ϕ_{Fn} = maximum peak-peak phase noise of the flat-top RF voltage.

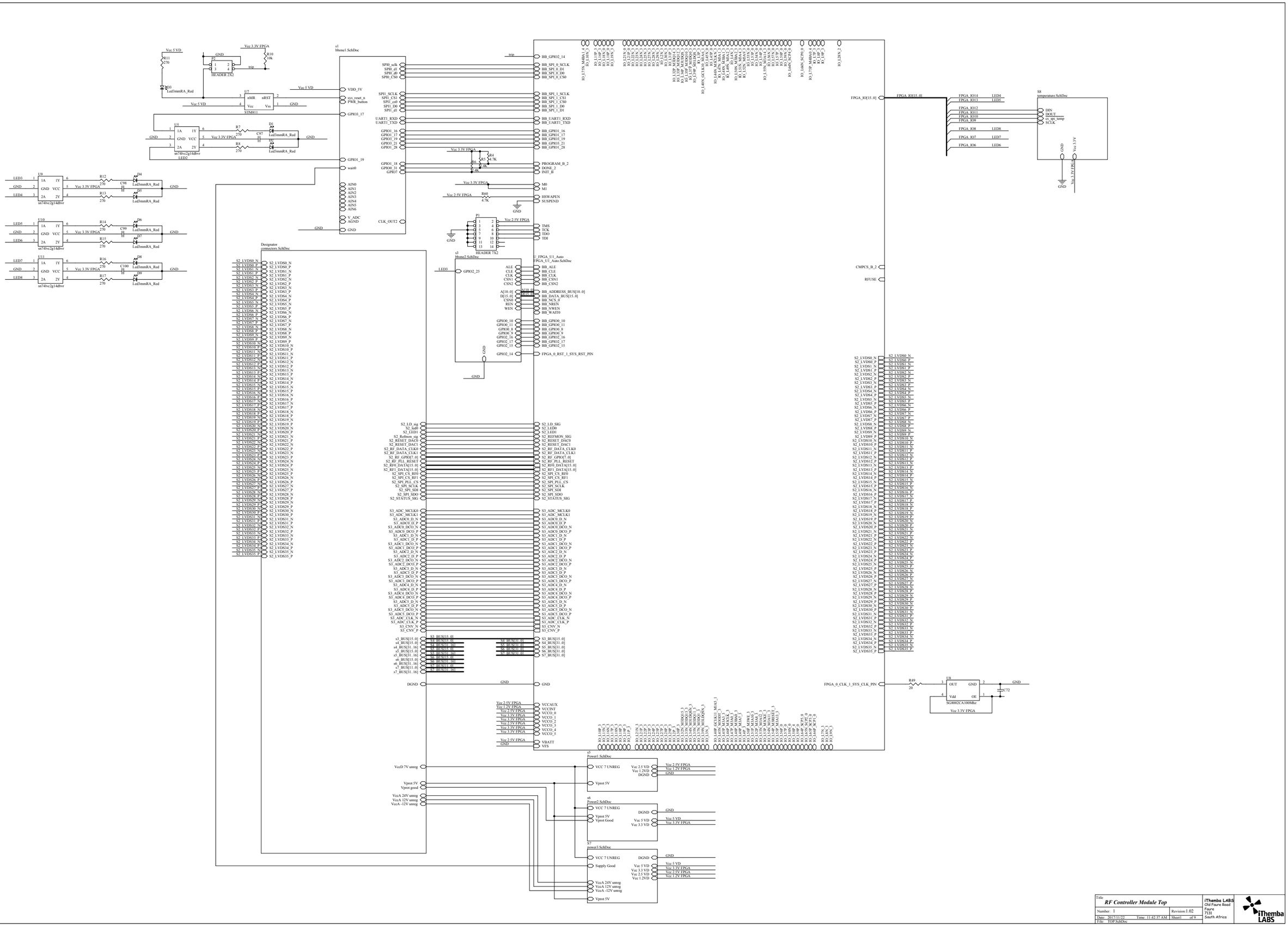
Appendix B

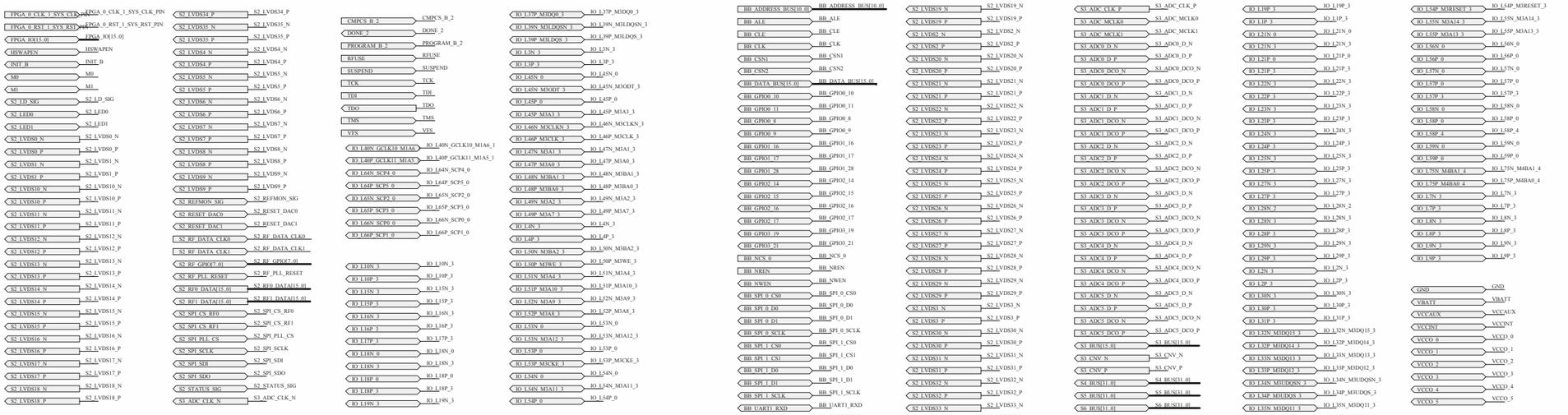
PCB Designs

B.1 RF Controller Module Schematics

Appendix B. RF Controller Module Schematics







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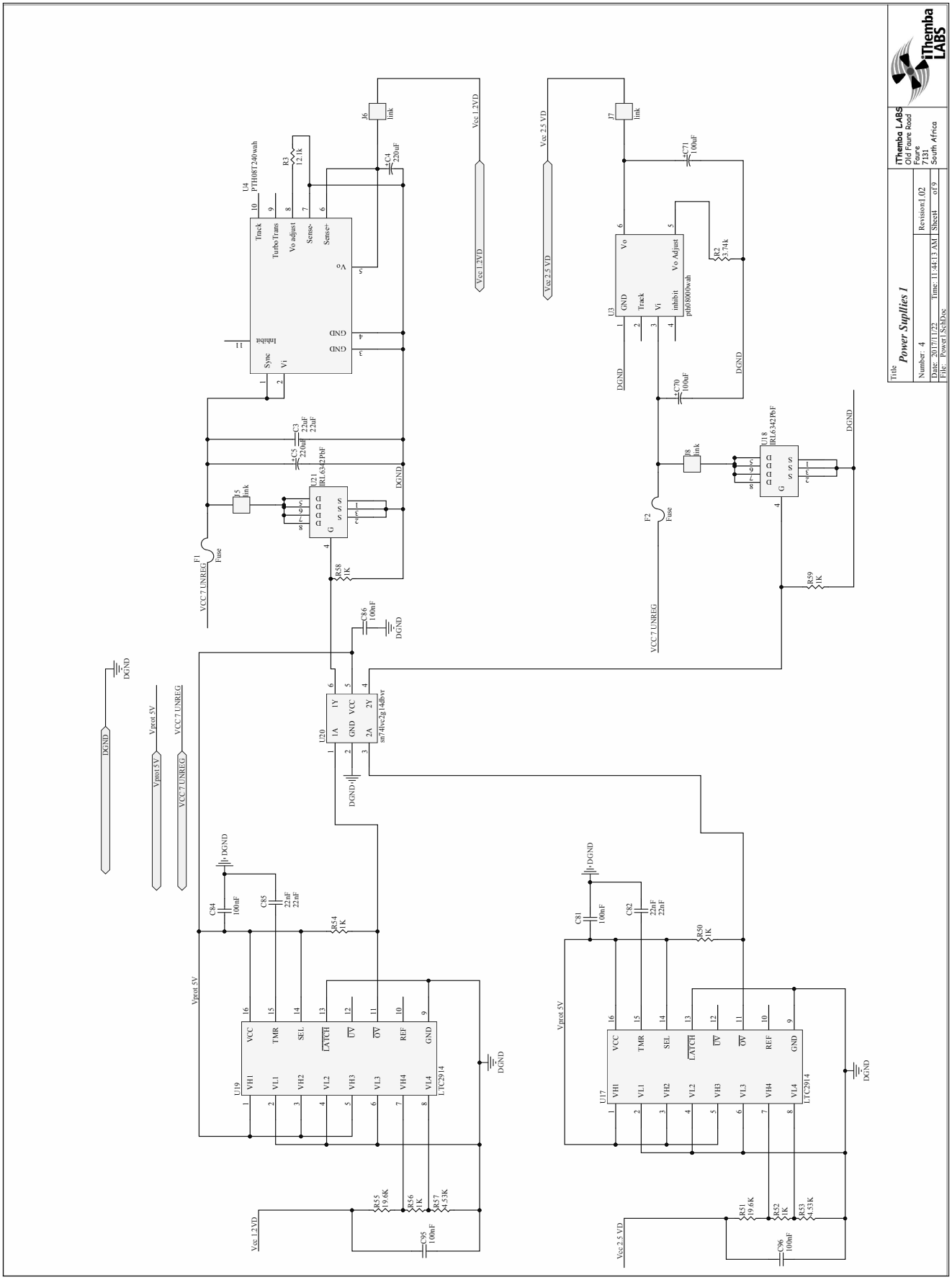
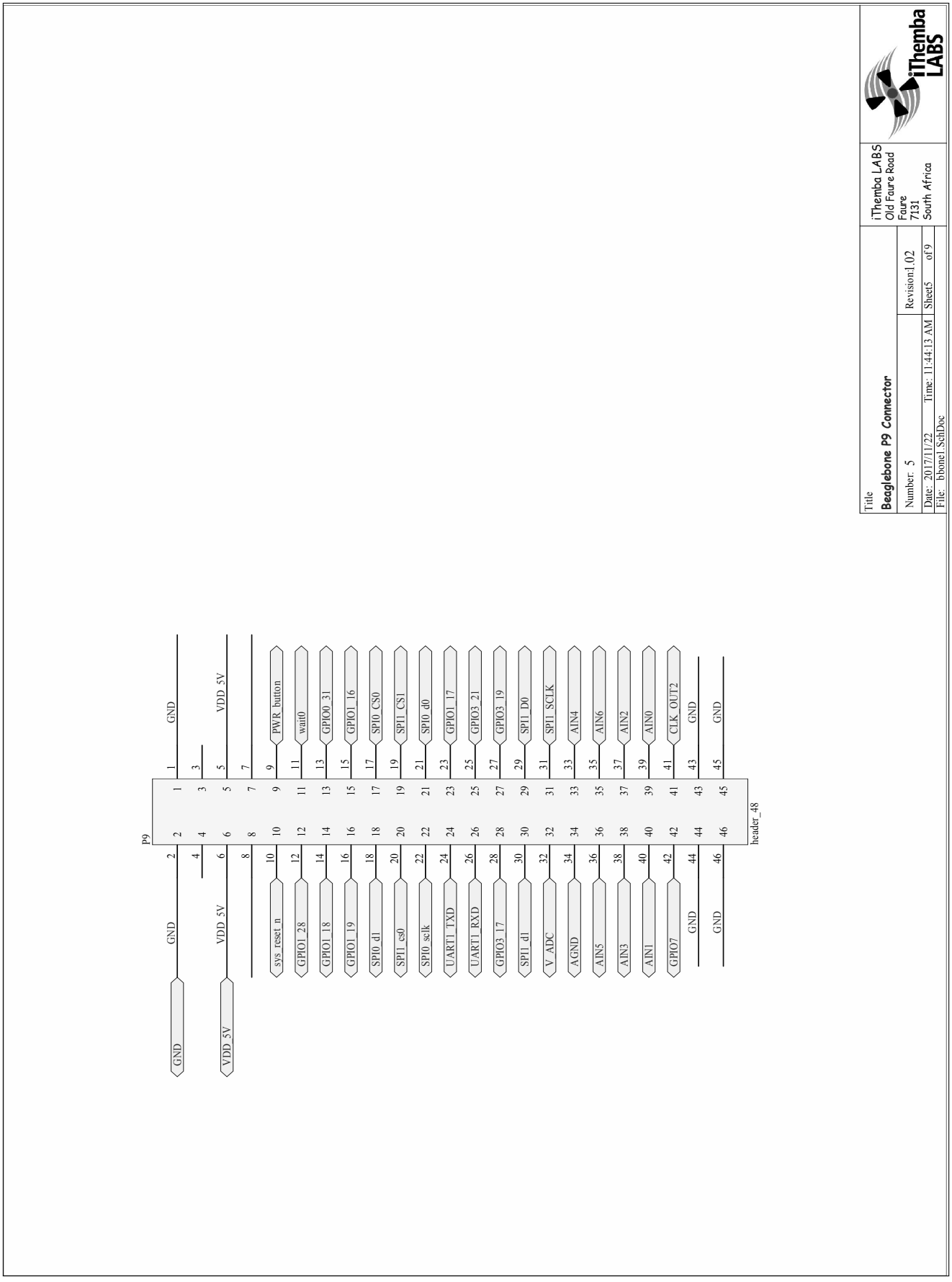
File: FPGA_U1_Auto.SchDoc	Sheet 2 of 9

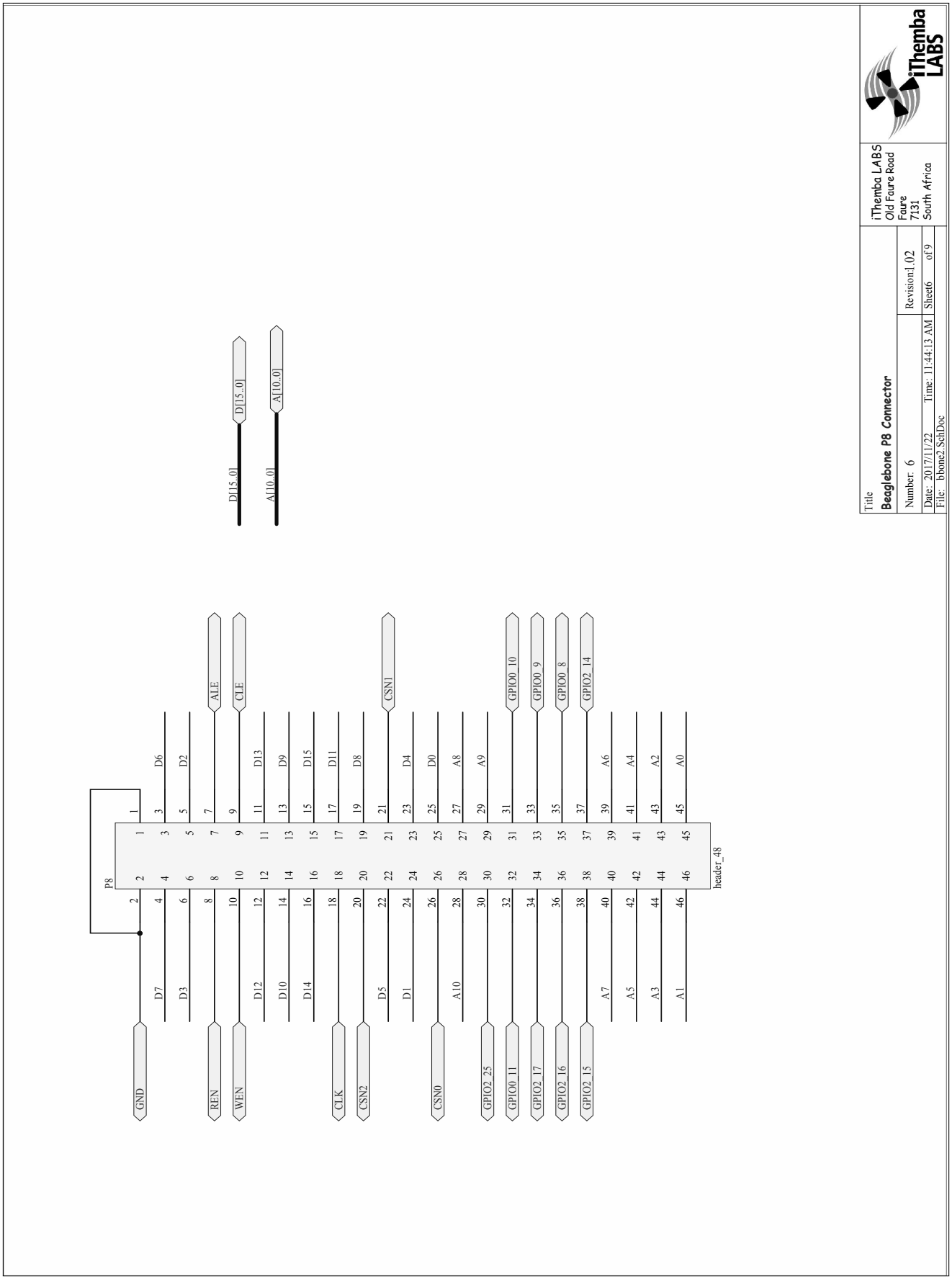
iThemba LABS
Old Faure Road
Faure
7131
South Africa

iThemba LABS

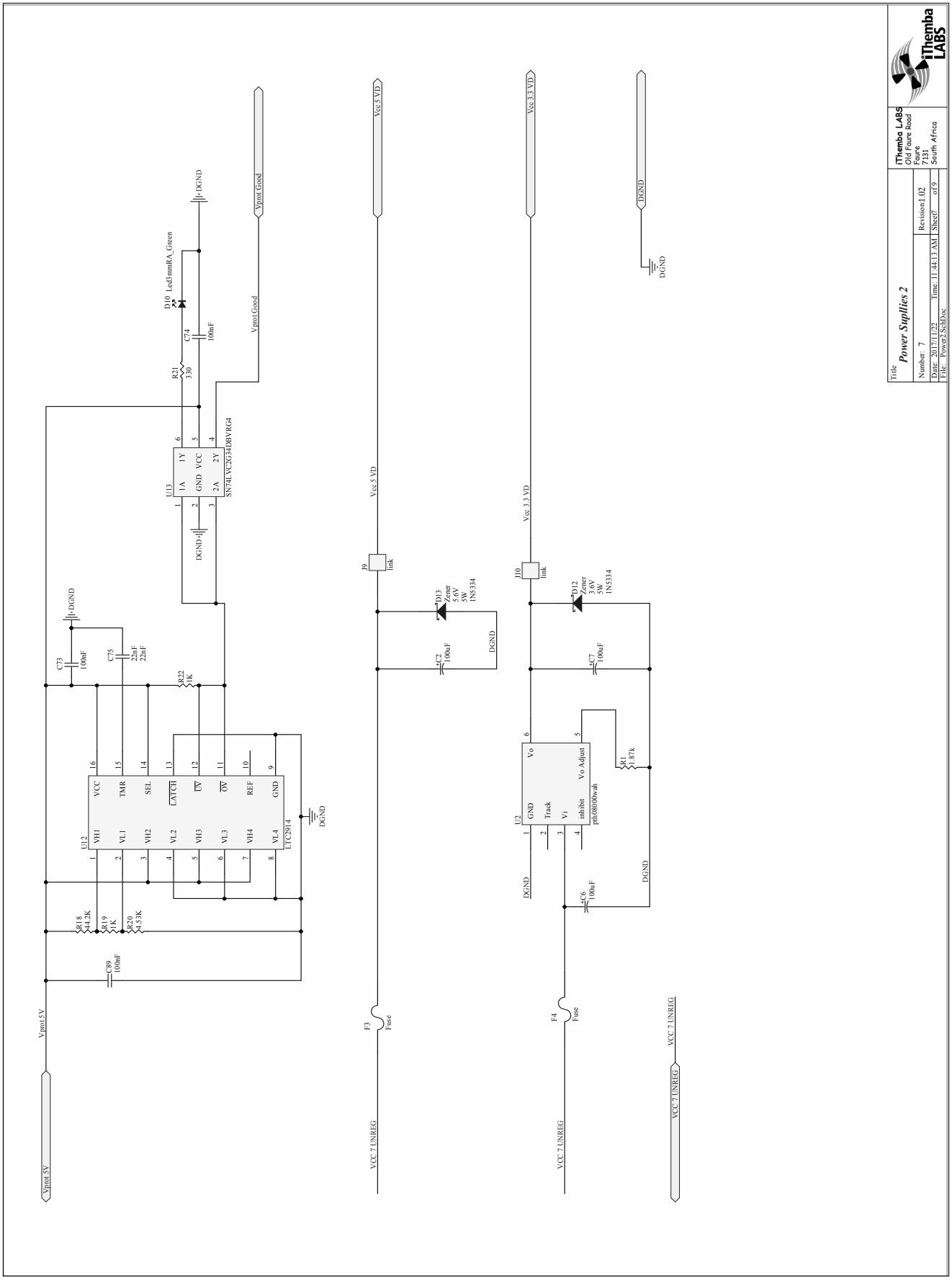
Appendix B. RF Controller Module Schematics



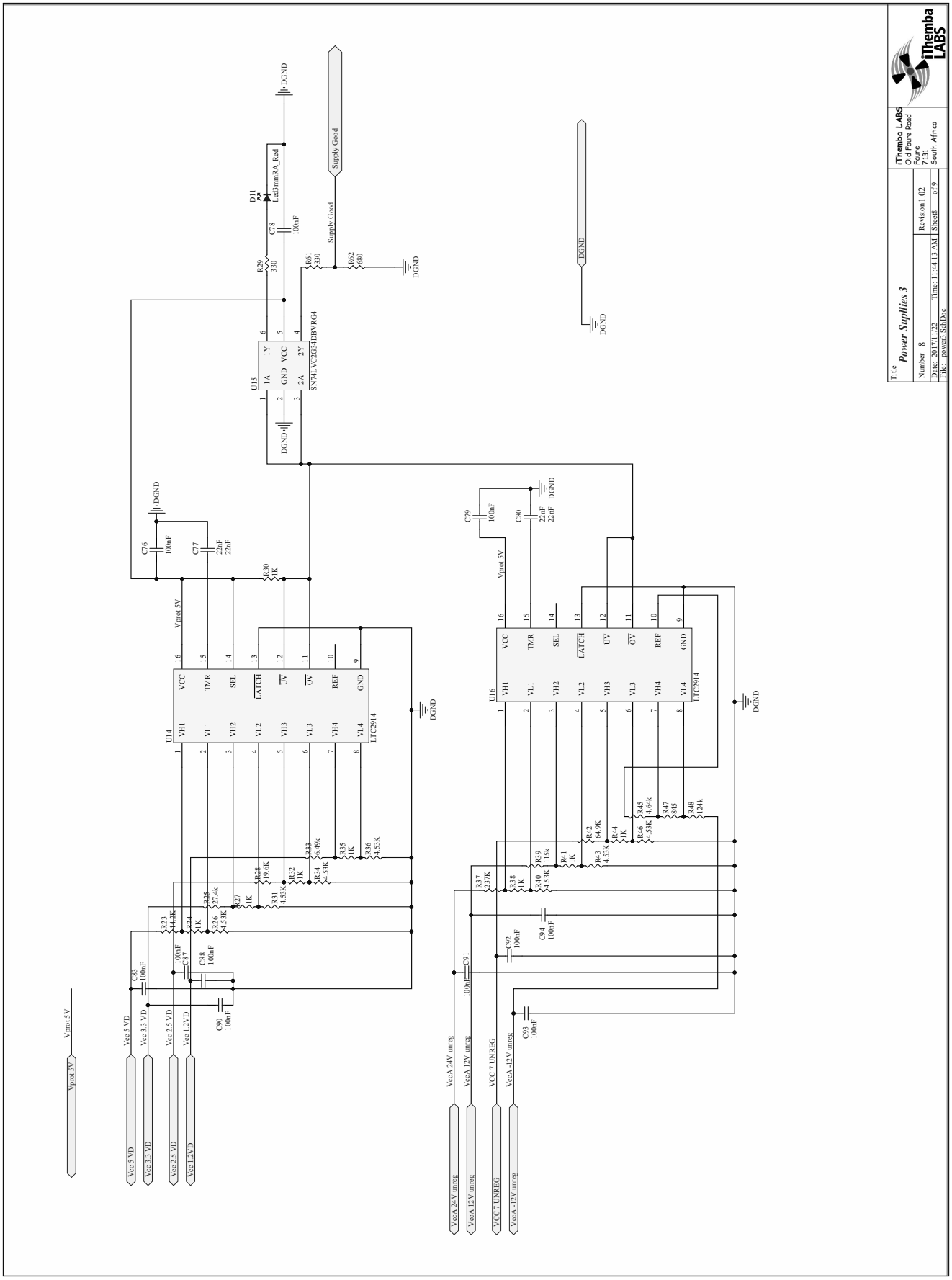


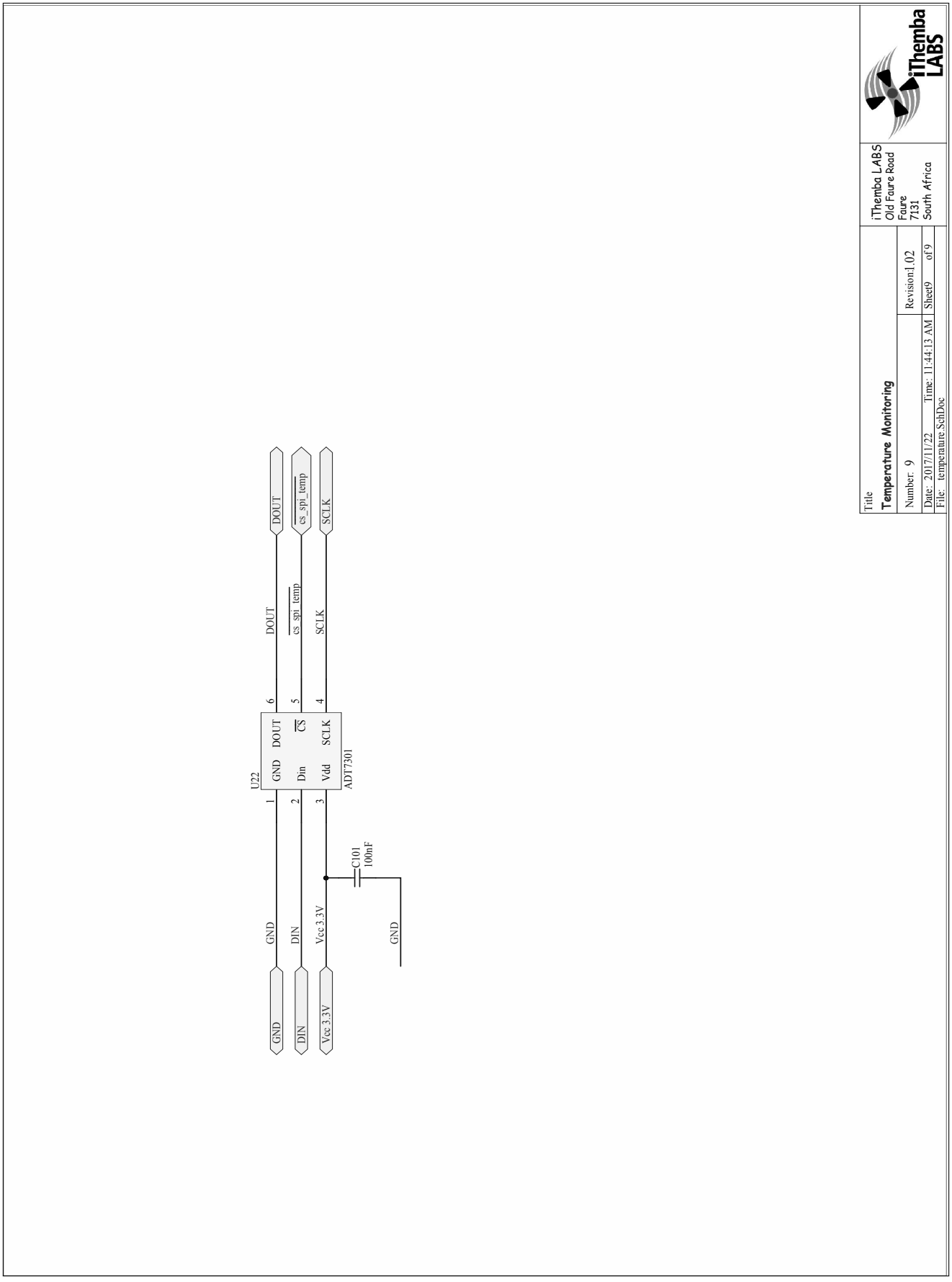


Appendix B. RF Controller Module Schematics



Appendix B. RF Controller Module Schematics





B.2 RF Controller Module BOM

Table B.1: Bill of Materials: RF Controller Module ERF111-1000

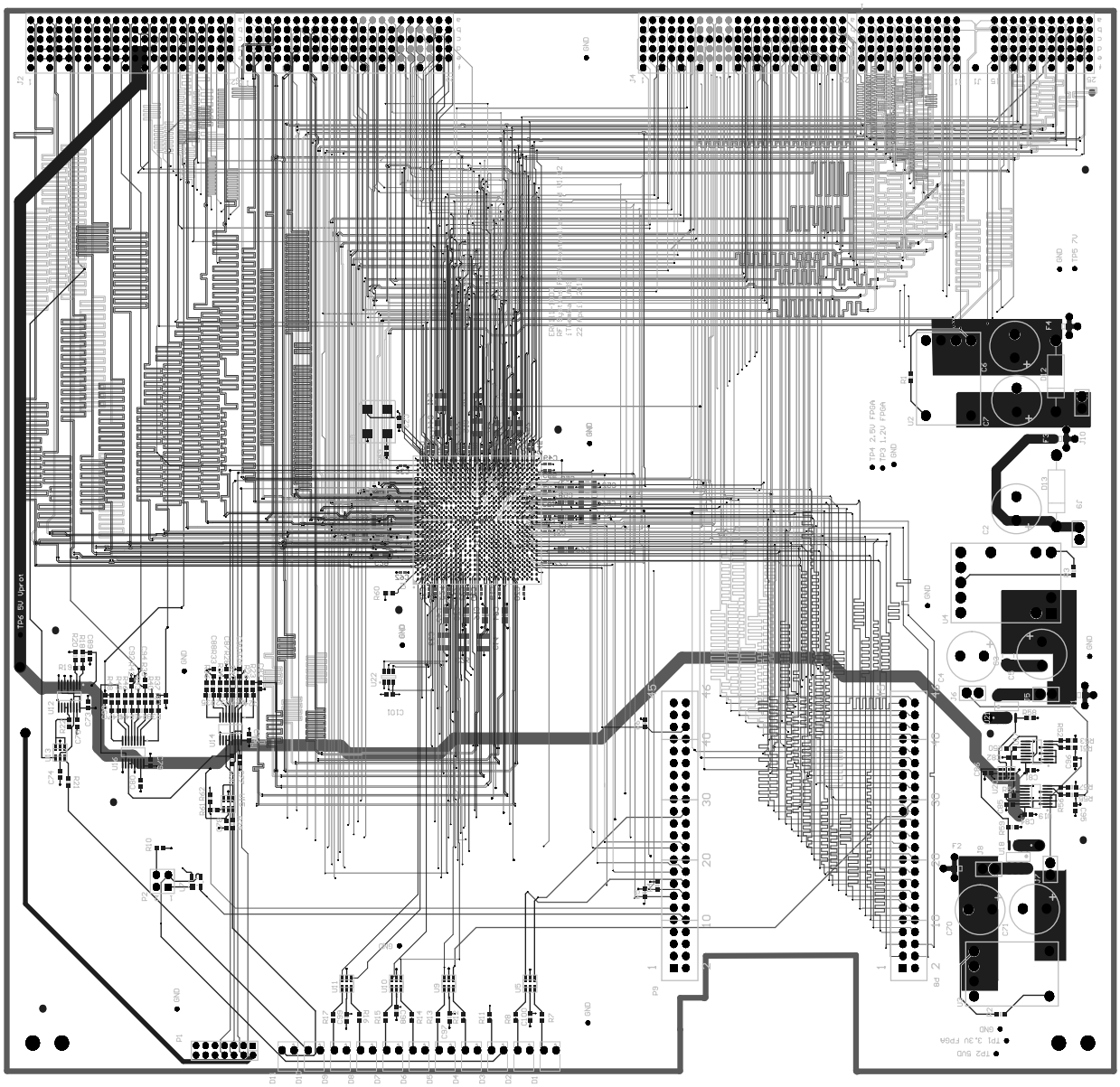
Index	Company Part No	Description	Qty	Manufacturer	Manufacturer Part No	Designator
1	ERF111-0001	4.53K 1% 0603 (1608) Surface Mounted Resistor	10	Yageo	2,3227E+11	R20, R26, R31, R34, R36, R40, R43, R46, R53, R57
2	ERF111-0002	1K Ohm 0603 Surface Mounted Resistor	16	yageo	RC0603FR-071KL	R19, R22, R24, R27, R30, R32, R35, R38, R41, R44, R50, R52, R54, R56, R58, R59
3	ERF111-0003	19.6K Ohm 0603 Surface Mounted Resistor	3	Yageo	RC0603FR-0719K6L	R28, R51, R55
4	ERF111-0004	Voltage Monitor	5	Linear Technologies	LTC2914CGN-1#PBF	U12, U14, U16, U17, U19
5	ERF111-0005	Non inverting buffer	2	Texas Instruments	SN74LVC2G34DBVR	U13, U15
6	ERF111-0006	330 Ohm 0603 Surface Mounted Resistor	3	yageo	RC0603FR-07330RL	R21, R29, R61
7	ERF111-0007	100nF 0603 Ceramic SMT Capacitor	25	Yageo	CC0603KRX7R9BB104	C72, C73, C74, C76, C78, C79, C81, C83, C84, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100, C101
8	ERF111-0008	22nF 0603 Ceramic SMT Capacitor	5	samsung	CL10B223KB8NNNC	C75, C77, C80, C82, C85
9	ERF111-0009	Mosfet	2	International Rectifier	IRL6342PBF	U18, U21
10	ERF111-0010	2.5A 0805 fuse	4	AVX	F0805B2R50FSTR	F1, F2, F3, F4
11	ERF111-0011	220uF Radial Capactior	2	Panasonic	EEUFC1J221	C4, C5
12	ERF111-0012	Voltage Regulator	1	Texas Instruments	PTH08T240WAH	U4
13	ERF111-0013	12.1K Ohm 0603 Surface Mounted Resistor	1	Yageo	2,3227E+11	R3
14	ERF111-0014	Voltage Regulator	3	Texas Instruments	PTH08000WAH	U2, U3, U6
15	ERF111-0015	3.74K Ohm 0603 Surface Mounted Resistor	1	RS	RS-0603-3k74-1%-0.1W	R2
16	ERF111-0016	100uF radial Capacitor 63V	6	Panasonic	EEUFC1J101B	C1, C2, C6, C7, C70, C71
17	ERF111-0017	2x48 2.54mm dual row header	2	Molex	90131-0785	P8, P9
18	ERF111-0018	270 Ohm 0603 Surface Mounted Resistor	9	Yageo	RC0603FR-07270R	R7, R8, R11, R12, R13, R14, R15, R16, R17
19	ERF111-0019	PCB mount right angle LED 3mm RED	10	KingBright	L-710A8EW/1LID	D1, D2, D3, D4, D5, D6, D7, D8, D9, D11
20	ERF111-0020	Header, 4-Pin, Dual row 2.54mm	1	FCI	75869-130LF	P2
21	ERF111-0021	44.2k Ohm 0603 Surface Mounted Resistor	2	Yageo	RC0603FR-0744K2L	R18, R23
22	ERF111-0022	27.4k Ohm 0603 Surface Mounted Resistor	1	Yageo	RC0603FR-0727K4L	R25
23	ERF111-0024	6.49k Ohm 0603 Surface Mounted Resistor	1	RS	RS-0603-6k49-1%-0.1W	R33
24	ERF111-0025	237k Ohm 0603 Surface Mounted Resistor	1	RS	RS-0603-237K-1%-0.1W	R37
25	ERF111-0026	115k Ohm 0603 Surface Mounted Resistor	1	RS	RS-0603-115K-1%-0.1W	R39
26	ERF111-0027	64.9k Ohm 0603 Surface Mounted Resistor	1	Yageo	RC0603FR-0764K9L	R42
27	ERF111-0028	4.64k Ohm 0603 Surface Mounted Resistor	1	yageo	2,3227E+11	R45
28	ERF111-0029	124k Ohm 0603 Surface Mounted Resistor	1	RS	RS-0603-124K-1%-0.1W	R48
29	ERF111-0030	845 Ohm 0603 Surface Mounted Resistor	1	RS	RS-0603-845R-1%-0.1W	R47
30	ERF111-0031	13 bit Digital temperature sensor	1	Analog Devices	ADT7301ARTZ-500RL7	U22
31	ERF111-0032	1.87K Ohm 0603 Surface Mounted Resistor	1	RS	RS-0603-1k87-1%-0.1W	R1
32	ERF111-0033	2.4K Ohm 0603 Surface Mounted Resistor	2	Yageo	RC0603FR-072K4L	R5, R6
33	ERF111-0034	348 Ohm 0603 Surface Mounted Resistor	1	RS	RS-0603-348R-1%-0.1W	R9
34	ERF111-0035	Z-Pack 2mm Hard Metric Type A 110 Position Female PCB Mount Connector	1	TE CONNECTIVITY	5352068-1	J1

Table B.1 continued: Bill of Materials: RF Controller Module ERF111-1000

Index	Company Part No	Description	Qty	Manufacturer	Manufacturer Part No	Designator
35	ERF111-0036	Z-Pack 2mm Hard Metric Type B 110 Position Female Daughter Card Connector	3	TE CONNECTIVITY	5352152-1	J2, J3, J4
36	ERF111-0037	4.7K Ohm 0603 Surface Mounted Resistor	2	yageo	RC0603FR-074K7L	R4, R60
37	ERF111-0038	4.7uF 0805 Ceramic SMT Capacitor.	16	Murata	GRM21BR61A475KA73L	C16, C17, C18, C27, C28, C29, C42, C43, C44, C57, C58, C59, C64, C65, C66, C69
38	ERF111-0039	20 Ohm 0603 Surface Mounted Resistor	1	RS	RS-0603-20R-1%-0.1W	R49
39	ERF111-0040	680 Ohm 0603 Surface Mounted Resistor	1	yageo	RC0603FR-07680RL	R62
40	ERF111-0041	Ceramic SMT Capacitor 1210, 100uF	12	samsung	CL32A107MQVNNNE	C14, C15, C25, C26, C33, C37, C41, C48, C52, C56, C67, C68
41	ERF111-0042	Ceramic SMT Capacitor 1210, 22uF	1	Samsung	CL32B226KOJNNNE	C3
42	ERF111-0043	470nF 0402Ceramic SMT Capacitor.	34	Murata	GRM155F51C474ZA01D	C8, C9, C10, C11, C12, C13, C19, C20, C21, C22, C23, C24, C30, C31, C32, C34, C35, C36, C38, C39, C40, C45, C46, C47, C49, C50, C51, C53, C54, C55, C60, C61, C62, C63
43	ERF111-0044	Header, 14-Pin, Dual row	1	Fanell	192-4619	P1
44	ERF111-0045	PCB mount right angle LED GREEN	1	KingBright	L-710A8EW/1LGD	D10
45	ERF111-0046	100MHz Clock	1	Epson Toyocom	SG8002CAPCB100MHZ	U8
46	ERF111-0048	reset monitor	1	STMicroelectronics	STM811LW16F	U7
47	ERF111-0049	Inverting Schmitt Trigger	5	Texas Instruments	SN74LVC2G14DBVR	U5, U9, U10, U11, U20
48	ERF111-0050	Zener Diode	1	On Semiconductor	1N5334B	D12
49	ERF111-0051	Zener Diode	1	On Semiconductor	1N5339B	D13
50	ERF111-0052	FPGA	1	Xilinx	XC6SLX150-3FG676C	U1
51	ERF111-0111	10k Ohm 0603 Surface Mounted Resistor	1	Yageo	RC0603FR-0710KL	R10

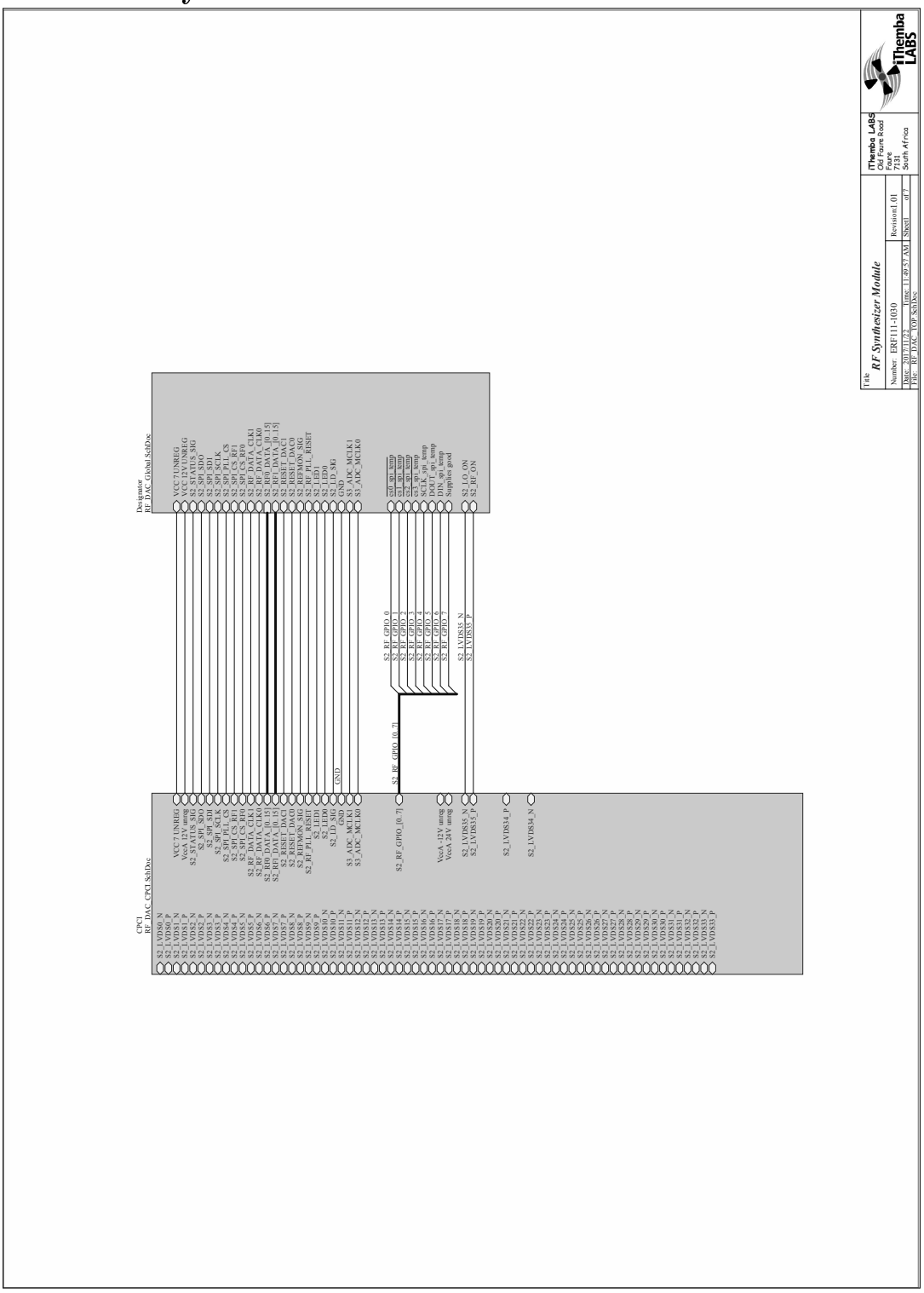
B.3 RF Controller Module PCB Layout

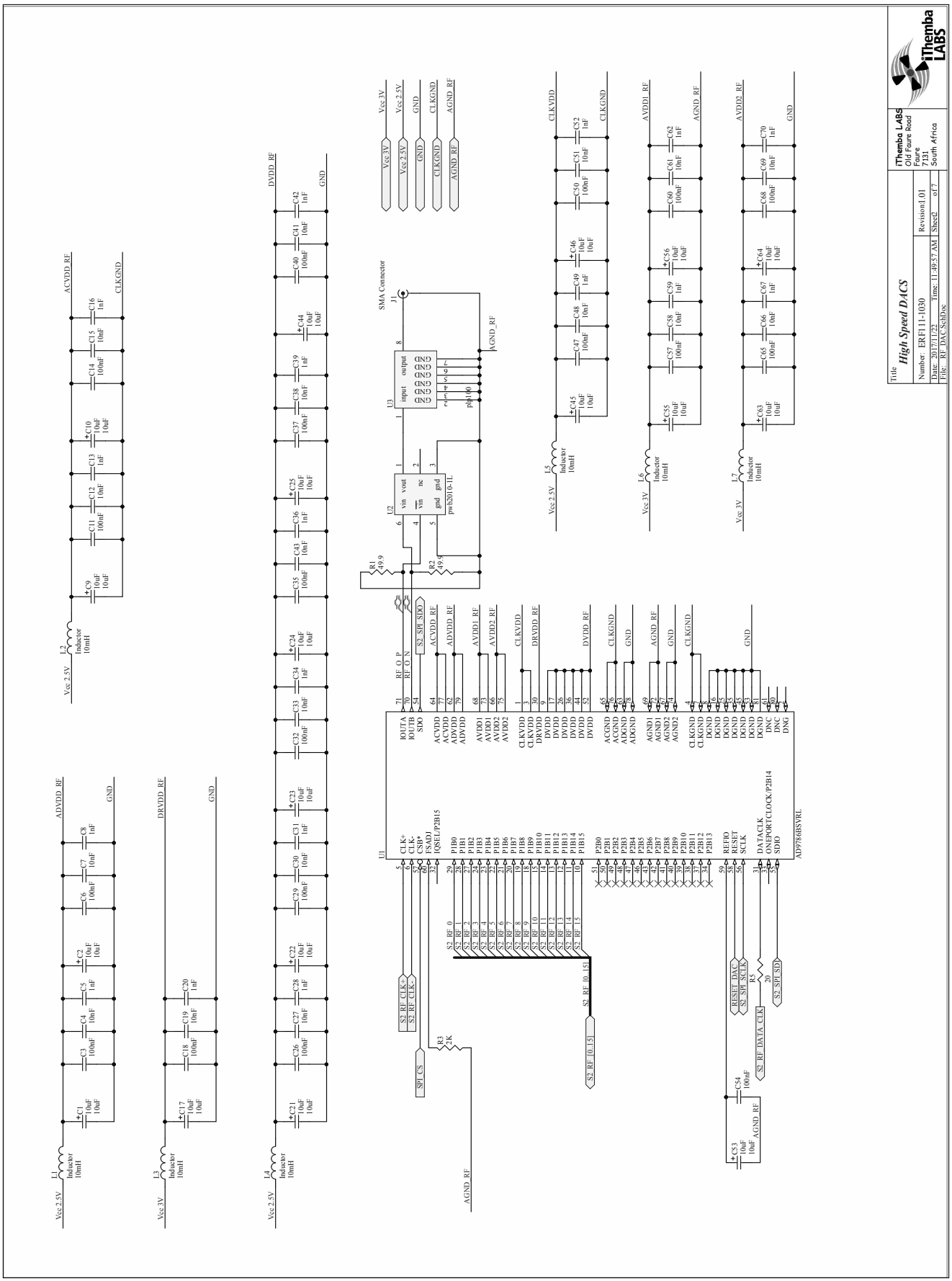
B.3.1 RF Controller PCB 12 layer Composite Print



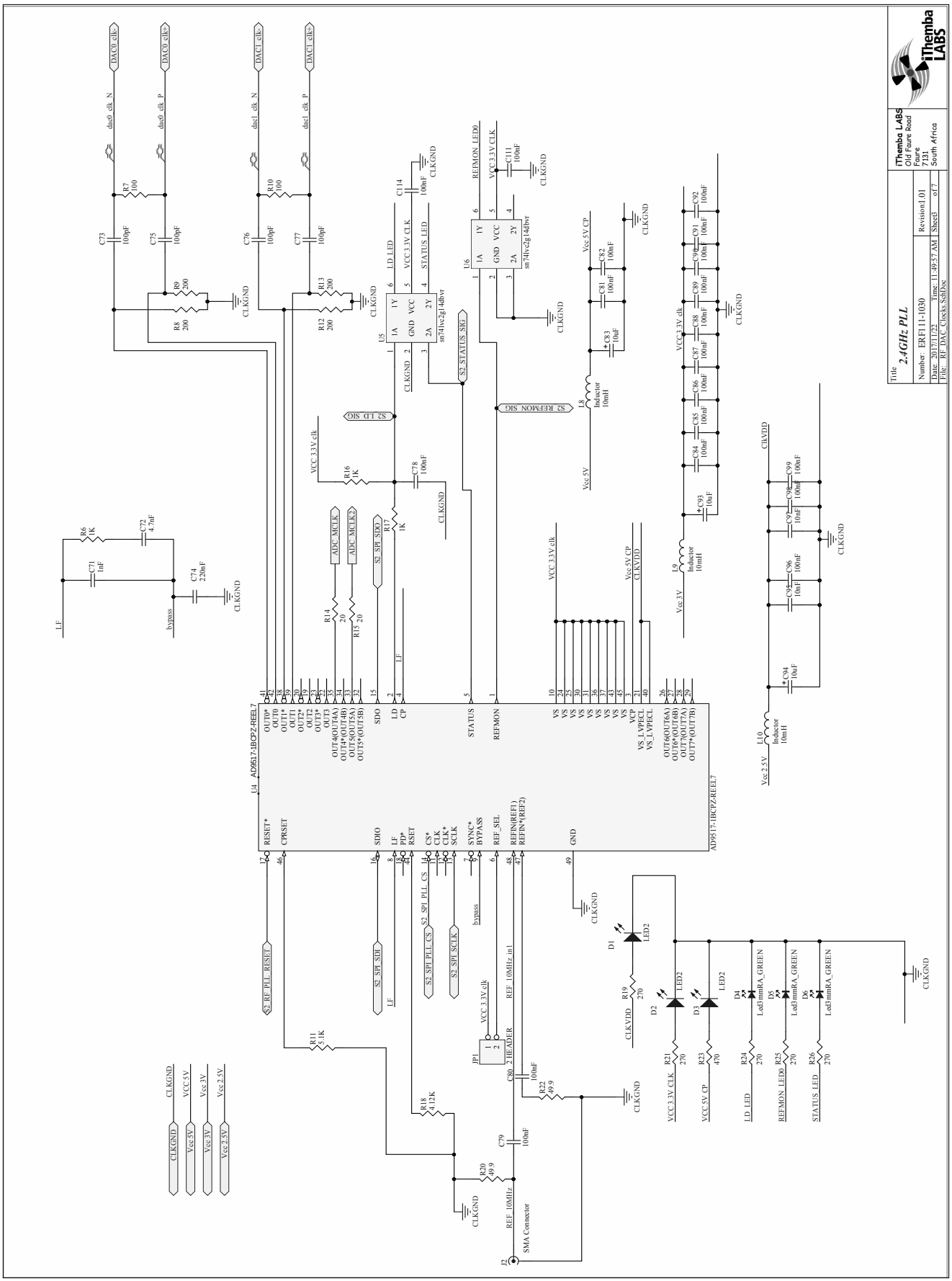
B.4 RF Synthesizer Module

B.4.1 RF Synthesizer Module Schematics

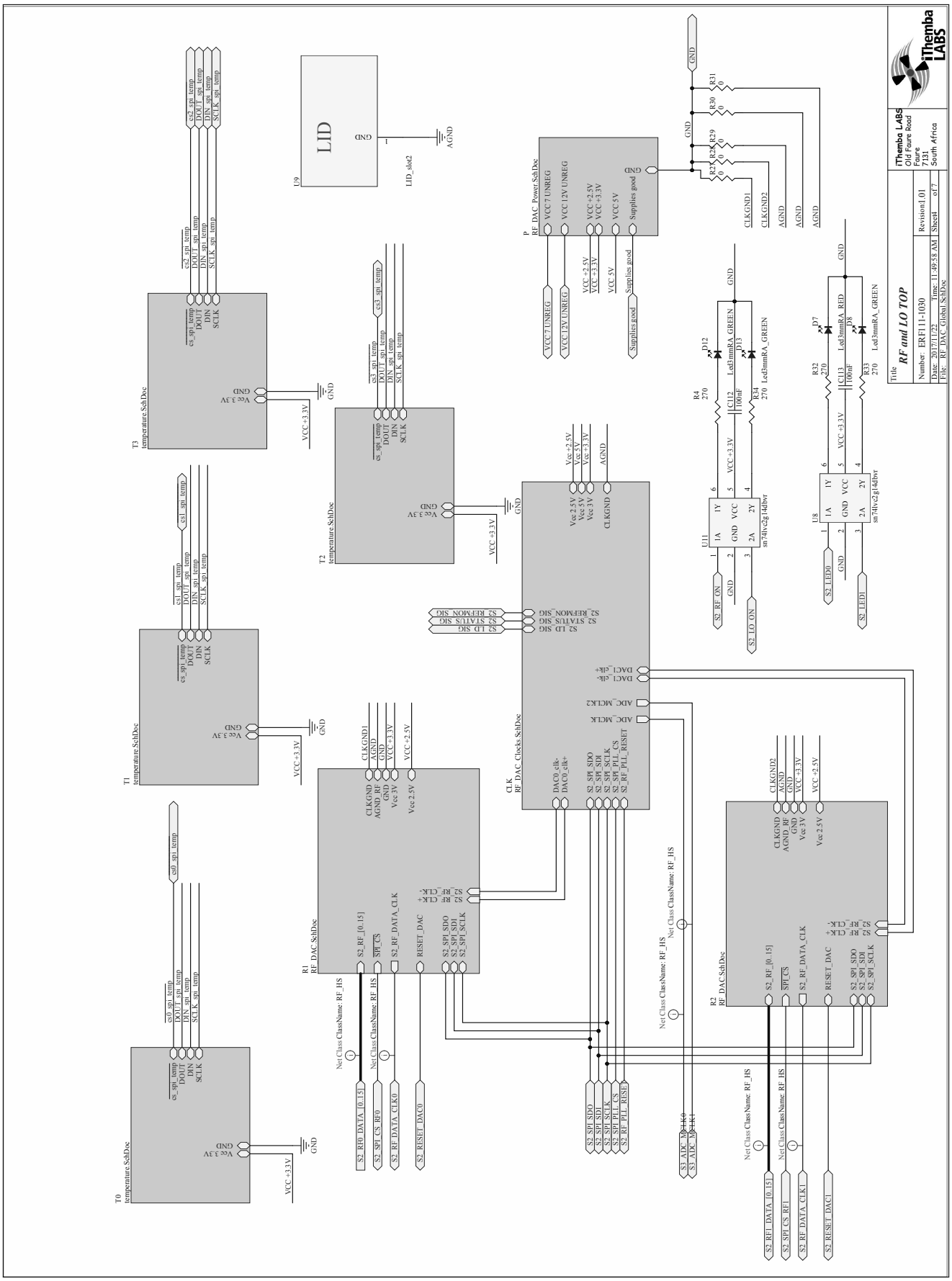




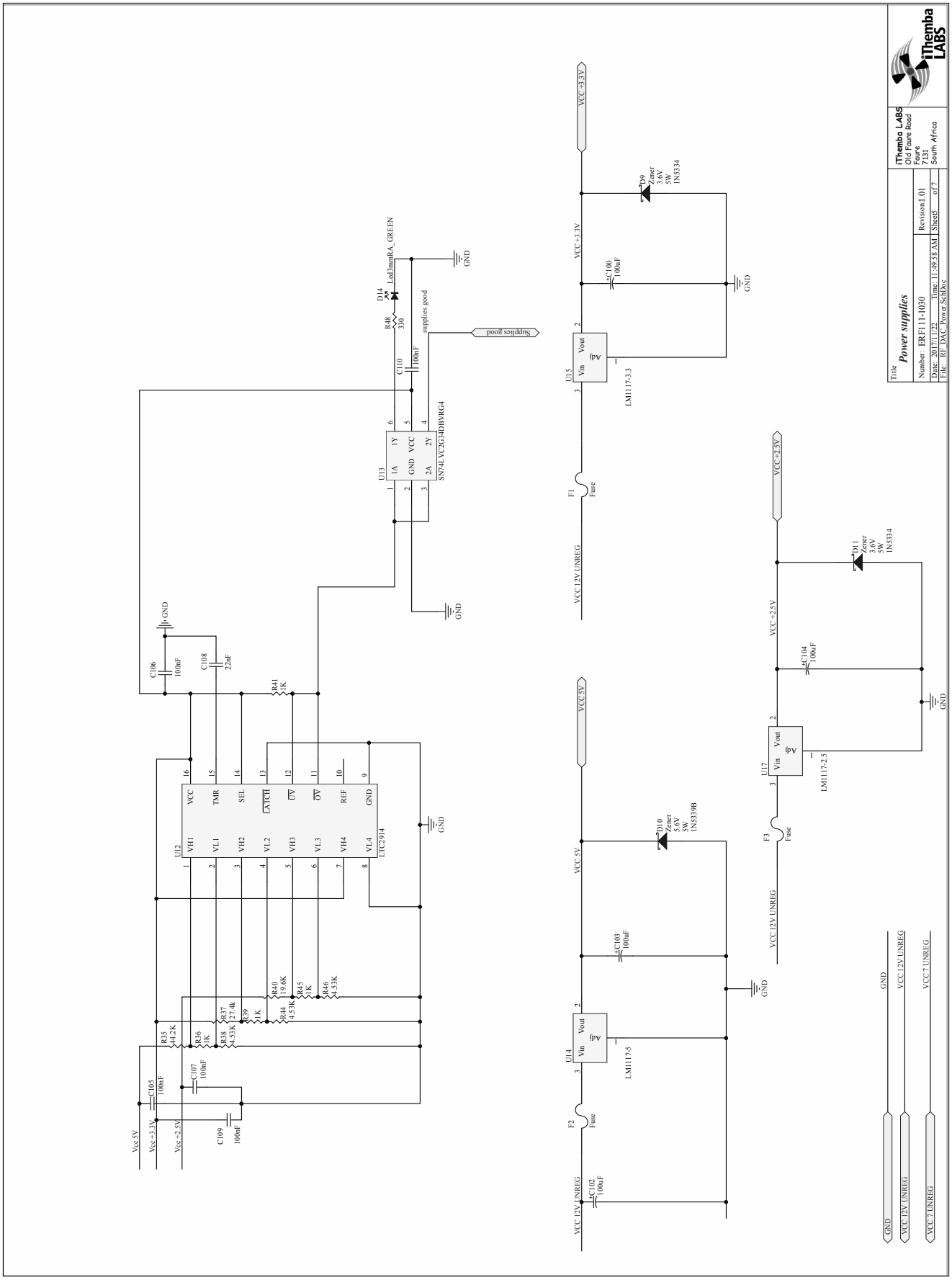
Appendix B. RF Synthesizer Module Schematics



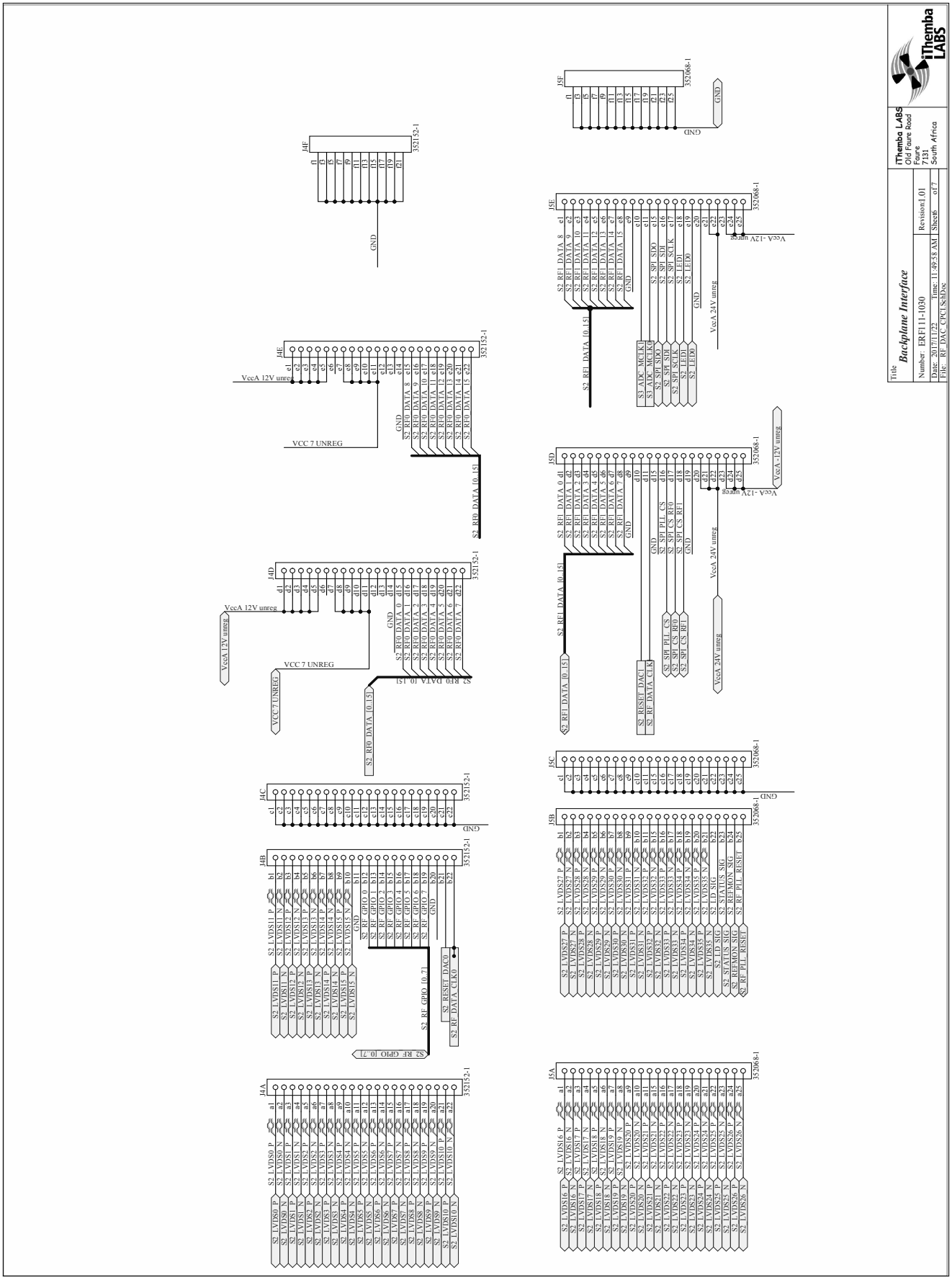
Appendix B. RF Synthesizer Module Schematics

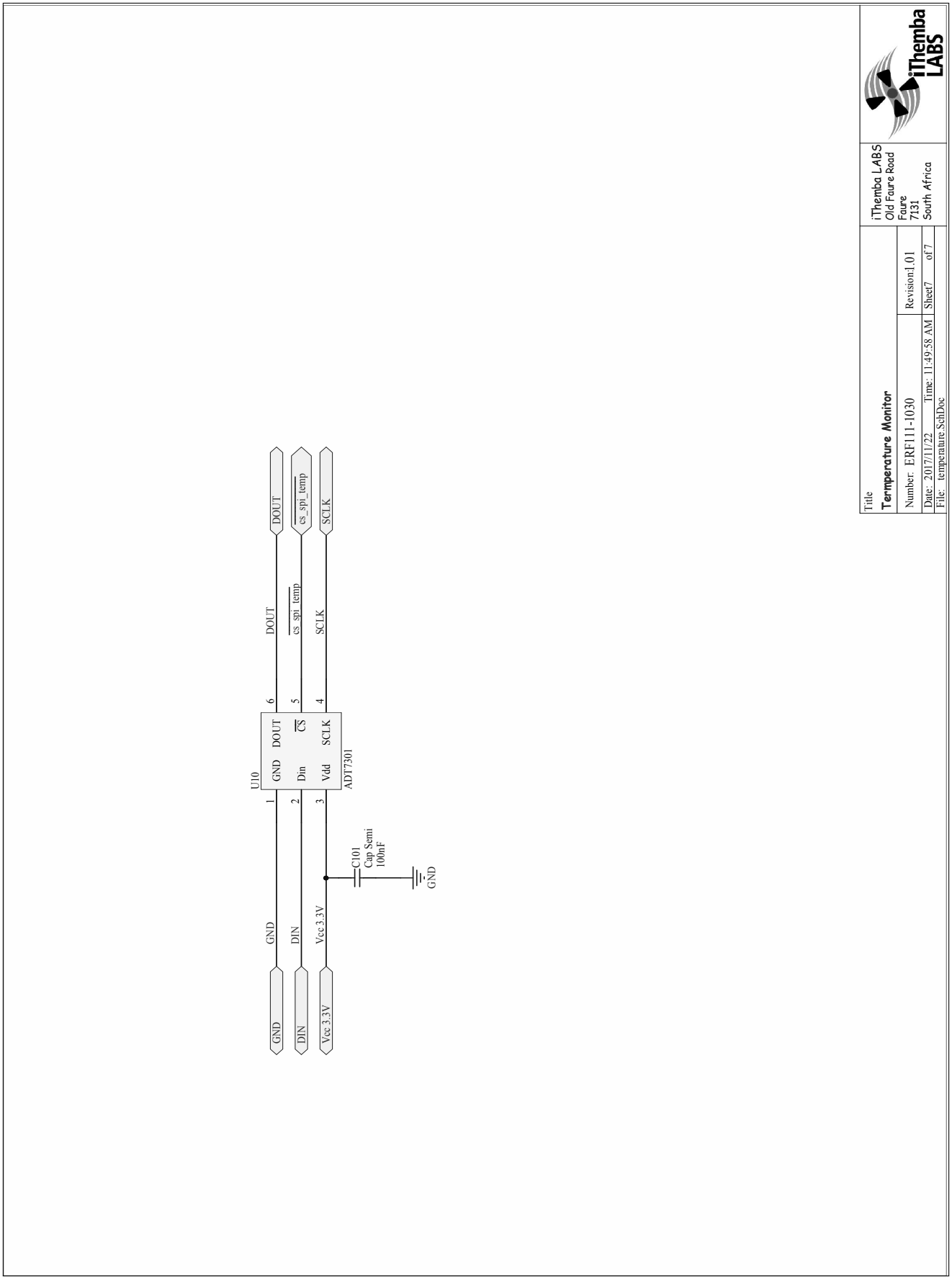


Appendix B. RF Synthesizer Module Schematics



Appendix B. RF Synthesizer Module Schematics





B.5 RF Synthesizer Module BOM

Table B.2: Bill of Materials: RF Synthesizer Module ERF111-1030

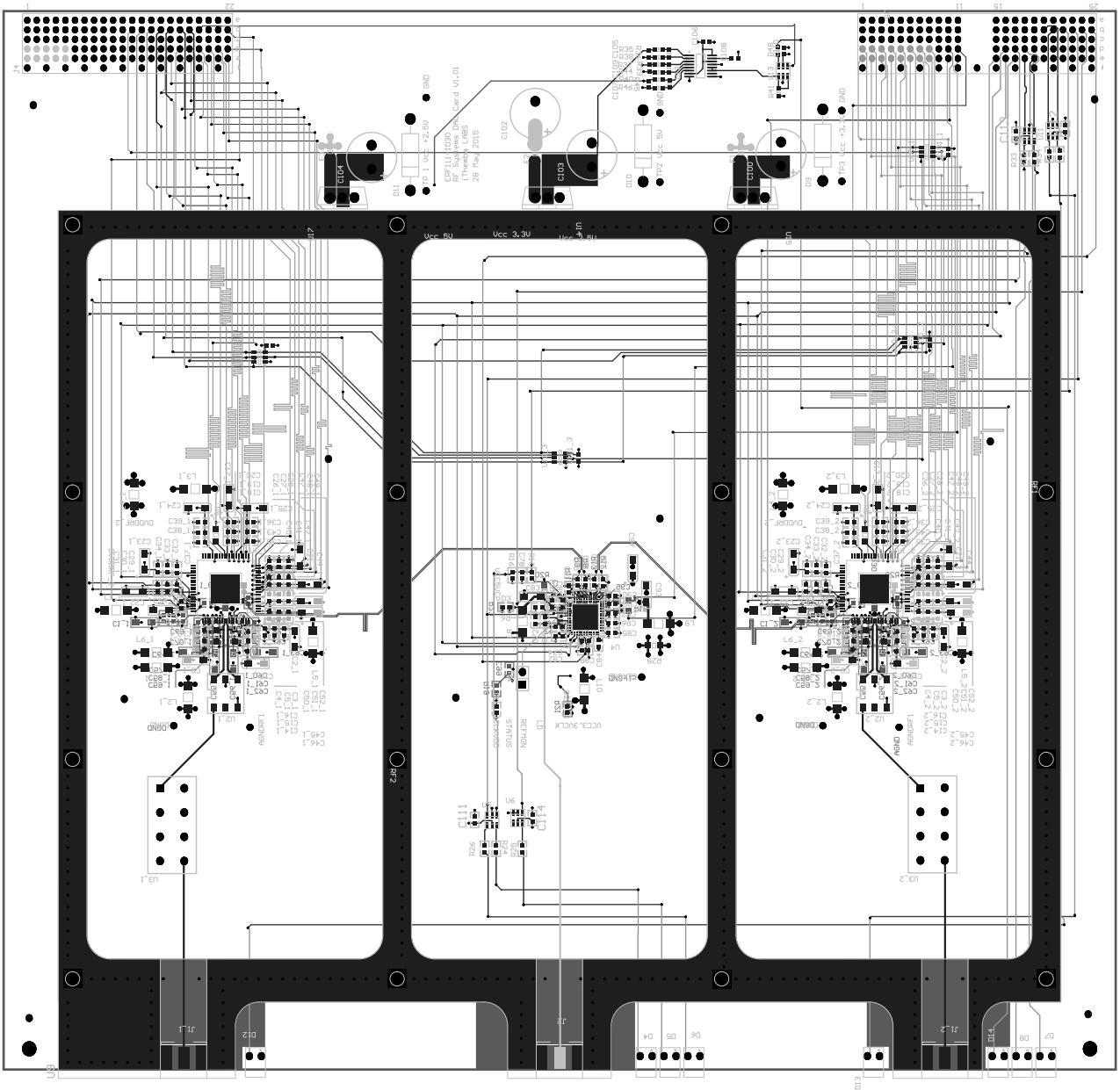
Index	Company Part No	Description	Qty	Manufacturer	Manufacturer Part No	Designator
1	ERF111-0001	4.53K 1% 0603 (1608) Surface Mounted Resistor	3	Yageo	2.3227E+11	R38, R44, R46
2	ERF111-0002	1K Ohm 0603 Surface Mounted Resistor	7	yageo	RC0603FR-071KL	R6, R16, R17, R36, R39, R41, R45
3	ERF111-0003	19.6K Ohm 0603 Surface Mounted Resistor	1	Yageo	RC0603FR-0719K6L	R40
4	ERF111-0004	Voltage Monitor	1	Linear Technologies	LTC2914CGN-1#PBF	U12
5	ERF111-0005	Non inverting buffer	1	Texas Instruments	SN74LVC2G34DBVR	Please Add
6	ERF111-0006	330 Ohm 0603 Surface Mounted Resistor	1	yageo	RC0603FR-07330RL	R48
7	ERF111-0007	100nF 0603 Ceramic SMT Capacitor	66	Yageo	CC0603KRX7R9BB104	C3_1, C3_2, C6_1, C6_2, C11_1, C11_2, C14_1, C14_2, C18_1, C18_2, C26_1, C26_2, C29_1, C29_2, C32_1, C32_2, C35_1, C35_2, C37_1, C37_2, C40_1, C40_2, C47_1, C47_2, C50_1, C50_2, C54_1, C54_2, C57_1, C57_2, C60_1, C60_2, C65_1, C65_2, C68_1, C68_2, C78, C7
8	ERF111-0008	22nF 0603 Ceramic SMT Capacitor	1	samsung	CL10B223KB8NNNC	C108
9	ERF111-0010	2.5A 0805 fuse	3	AVX	F0805B2R50FSTR	F1, F2, F3
10	ERF111-0016	100uF radial Capacitor 63V	4	Panasonic	EEUFC1J101B	C100, C102, C103, C104
11	ERF111-0018	270 Ohm 0603 Surface Mounted Resistor	9	Yageo	RC0603FR-07270R	R4, R19, R21, R24, R25, R26, R32, R33, R34
12	ERF111-0019	PCB mount right angle LED 3mm RED	1	KingBright	L-710A8EW/1LID	D7
13	ERF111-0021	44.2k Ohm 0603 Surface Mounted Resistor	1	Yageo	RC0603FR-0744K2L	R35
14	ERF111-0022	27.4k Ohm 0603 Surface Mounted Resistor	1	Yageo	RC0603FR-0727K4L	R37
15	ERF111-0031	13 bit Digital temperature sensor	4	Analog Devices	ADT7301ARTZ-500RL7	U10_1, U10_2, U10_3, U10_4
16	ERF111-0035	Z-Pack 2mm Hard Metric Type A 110 Position Female PCB Mount Connector	1	TE CONNECTIVITY	5352068-1	J5
17	ERF111-0036	Z-Pack 2mm Hard Metric Type B 110 Position Female Daughter Card Connector	1	TE CONNECTIVITY	5352152-1	J4
18	ERF111-0045	PCB mount right angle LED GREEN	7	KingBright	L-710A8EW/1LGD	D4, D5, D6, D8, D12, D13, D14
19	ERF111-0049	Inverting Schmitt Trigger	5	Texas Instruments	SN74LVC2G14DBVR	U5, U6, U8, U11, U13
20	ERF111-0050	Zener Diode	2	On Semiconductor	1N5334B	D9, D11
21	ERF111-0051	Zener Diode	1	On Semiconductor	1N5339B	D10
22	ERF111-0053	10nF 0603 Ceramic SMT Capacitor	36	Phycomp	CC0603KRX7R9BB103	C4_1, C4_2, C7_1, C7_2, C12_1, C12_2, C15_1, C15_2, C19_1, C19_2, C27_1, C27_2, C30_1, C30_2, C33_1, C33_2, C38_1, C38_2, C41_1, C41_2, C43_1, C43_2, C48_1, C48_2, C51_1, C51_2, C58_1, C58_2, C61_1, C61_2, C66_1, C66_2, C69_1, C69_2, C95, C97
23	ERF111-0054	1nF 0603 Ceramic SMT Capacitor	35	Samsung	CL10B102KB8NNNC	C5_1, C5_2, C8_1, C8_2, C13_1, C13_2, C16_1, C16_2, C20_1, C20_2, C28_1, C28_2, C31_1, C31_2, C34_1, C34_2, C36_1, C36_2, C39_1, C39_2, C42_1, C42_2, C49_1, C49_2, C52_1, C52_2, C59_1, C59_2, C62_1, C62_2, C67_1, C67_2, C70_1, C70_2, C71
24	ERF111-0055	10uF Tantulum capacitor CASE A	39	Vishay	TR3A106K010C1800	C1_1, C1_2, C2_1, C2_2, C9_1, C9_2, C10_1, C10_2, C17_1, C17_2, C21_1, C21_2, C22_1, C22_2, C23_1, C23_2, C24_1, C24_2, C25_1, C25_2, C44_1, C44_2, C45_1, C45_2, C46_1, C46_2, C53_1, C53_2, C55_1, C55_2, C56_1, C56_2, C63_1, C63_2, C64_1, C64_2, C83, C93,
25	ERF111-0056	inductor beed 1000 Ohm 100MHz	17	Murata	BLM41PG102SN1L	L1_1, L1_2, L2_1, L2_2, L3_1, L3_2, L4_1, L4_2, L5_1, L5_2, L6_1, L6_2, L7_1, L7_2, L8, L9, L10
26	ERF111-0057	4.7nF 0603 Ceramic SMT Capacitor.	1	Kemet	C0603C472K5RACTU	C72
27	ERF111-0058	100pF 0603 Ceramic SMT Capacitor.	4	Phycomp	C0603JRNP09BN101	C73, C75, C76, C77
28	ERF111-0059	220nF 0603 Ceramic SMT Capacitor.	1	Murata	GRM188F51H224ZA01D	C74
29	ERF111-0061	Osram Opto CHIPLED 0603 Series Red LED	3	Avago	HSMH-C190	D1, D2, D3
30	ERF111-0064	SMA Connector PCB mounted (DNP)	3	Amphenol	132289	J1_1, J1_2, J2

Table B.2 continued: Bill of Materials: RF Synthesizer Module ERF111-1030

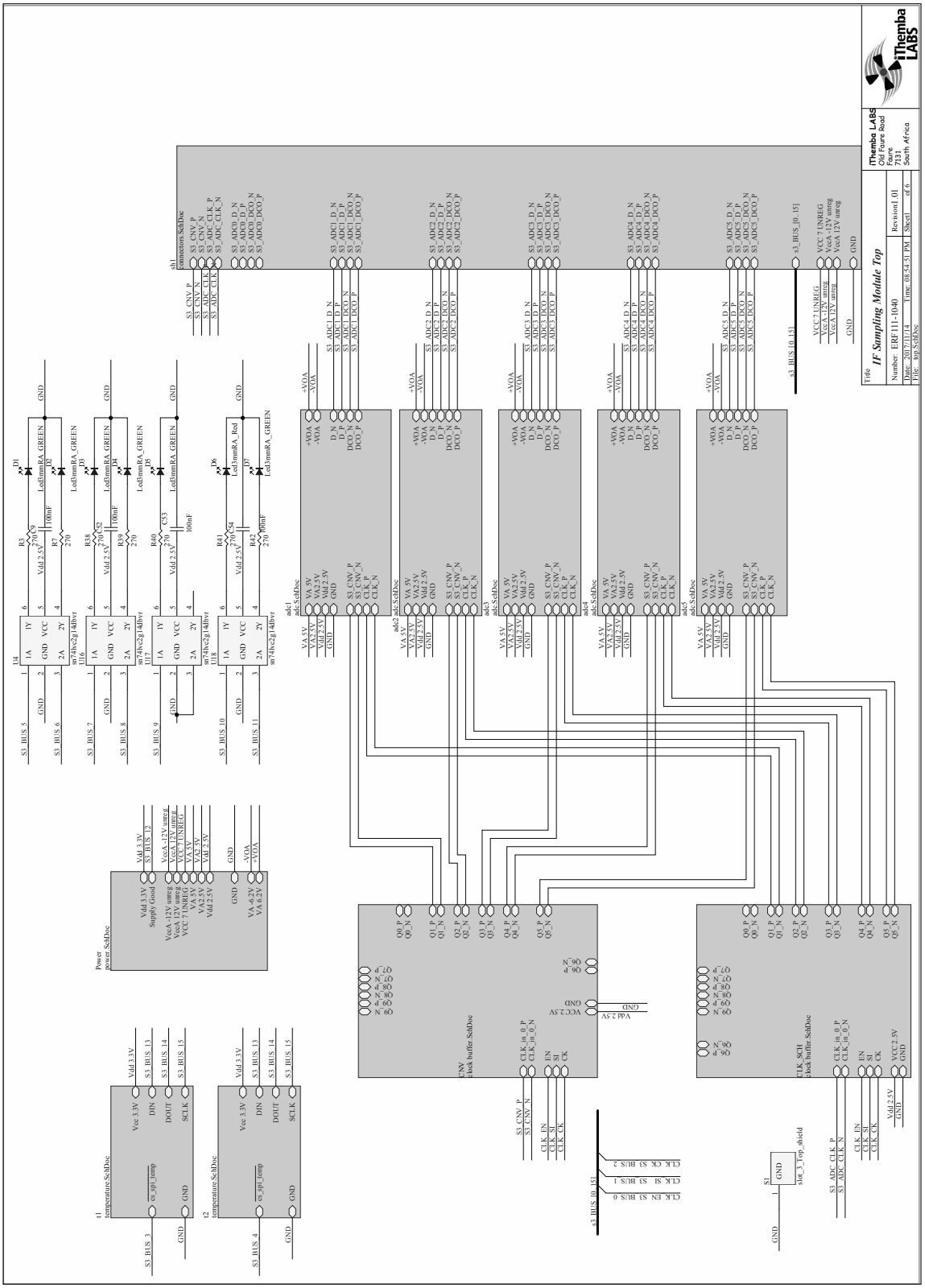
Index	Company Part No	Description	Qty	Manufacturer	Manufacturer Part No	Designator
31	ERF111-0066	2 Pin Header (cut up a 2 x50 way header ERF111-0017)	1	HARWIN	M20-9990246	JP1
32	ERF111-0067	2K Ohm 0603 Surface Mounted Resistor	2	Panasonic	ERA3ARW202V	R3_1, R3_2
33	ERF111-0068	20 Ohm 0805 Surface Mounted Resistor	4	Yageo	RC0805FR-0720RL	R5_1, R5_2, R14, R15
34	ERF111-0070	100 Ohm 0603 Surface Mounted Resistor	2	Yageo	RC0603FR-07100RL	R7, R10
35	ERF111-0071	200 Ohm 0603 Surface Mounted Resistor	4	Yageo	RC0603FR-07200RL	R8, R9, R12, R13
36	ERF111-0072	5.1K Ohm 0603 Surface Mounted Resistor	1	phycomp	RJ0603FRE075K1L	R11
37	ERF111-0073	4.12K Ohm 0603 Surface Mounted Resistor	1	Panasonic	ERA3AEB4121V	R18
38	ERF111-0074	470 Ohm 0603 Surface Mounted Resistor	1	Yageo	RC0603FR-07470RL	R23
39	ERF111-0075	49.9 Ohm 0805 Surface Mounted Resistor	6	TE CONNECTIVITY	RN73C2A49R9BTDF	R1_1, R1_2, R2_1, R2_2, R20, R22
40	ERF111-0076	0 Ohm 0805 Surface Mounted Resistor	5	0	0	R27, R28, R29, R30, R31
41	ERF111-0077	2.4GHz VCO PLL clock distribution	1	Analog Devices	AD9517-1ABCPZ	U4
42	ERF111-0078	500MHz DAC	2	Analog Devices	AD9786	U1_1, U1_2
43	ERF111-0079	100MHZ LPF	2	Mini-Circuits	PLP-100+	U3_1, U3_2
44	ERF111-0080	RF differential to single ended transformer	2	Coil Craft	PWB2010-1LB	U2_1, U2_2
45	ERF111-0081	3.3V Voltage regulator (DNP)	1	STMicroelectronics	LD1117V33C	U15
46	ERF111-0082	5V Voltage regulator (DNP)	1	STMicroelectronics	LD1117V50	U14
47	ERF111-0083	2.5V Voltage regulator (DNP)	1	Texas Instruments	LM1117T-2.5/NOPB	U17

B.6 RF Synthesizer Module PCB Layout

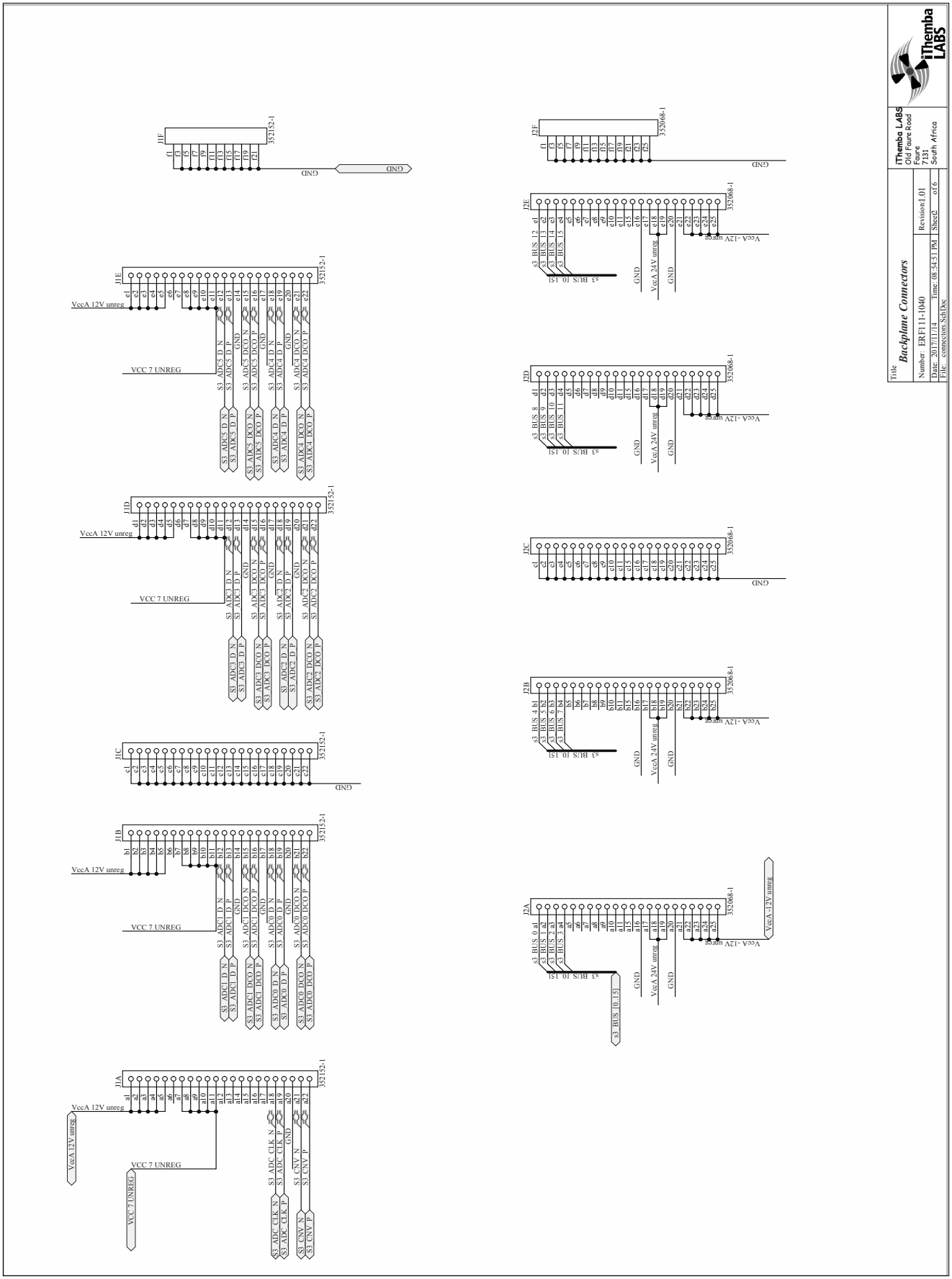
B.6.1 RF Synthesizer PCB 8 layer Composite Print



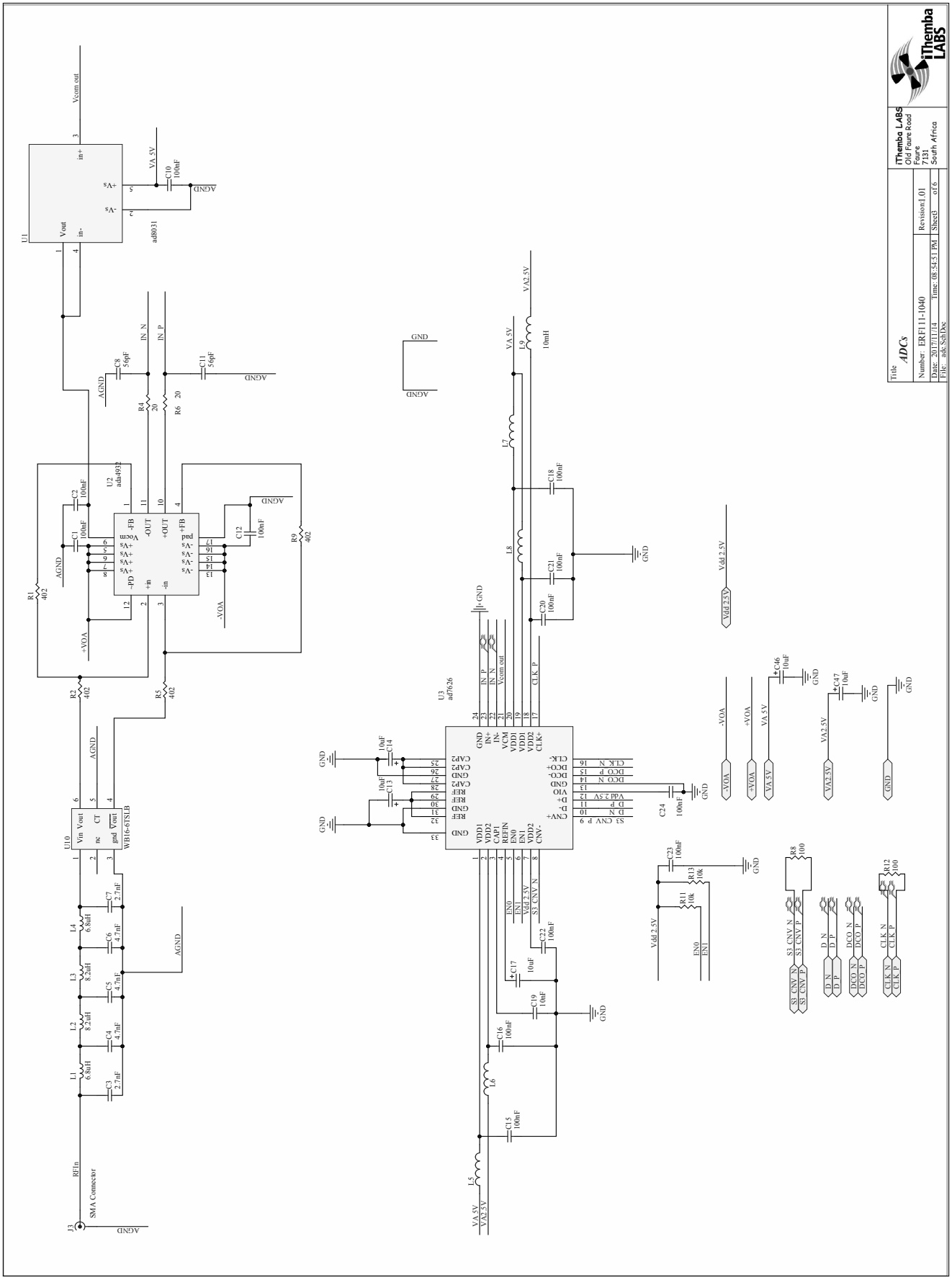
B.7 IF Sampling Module Schematics

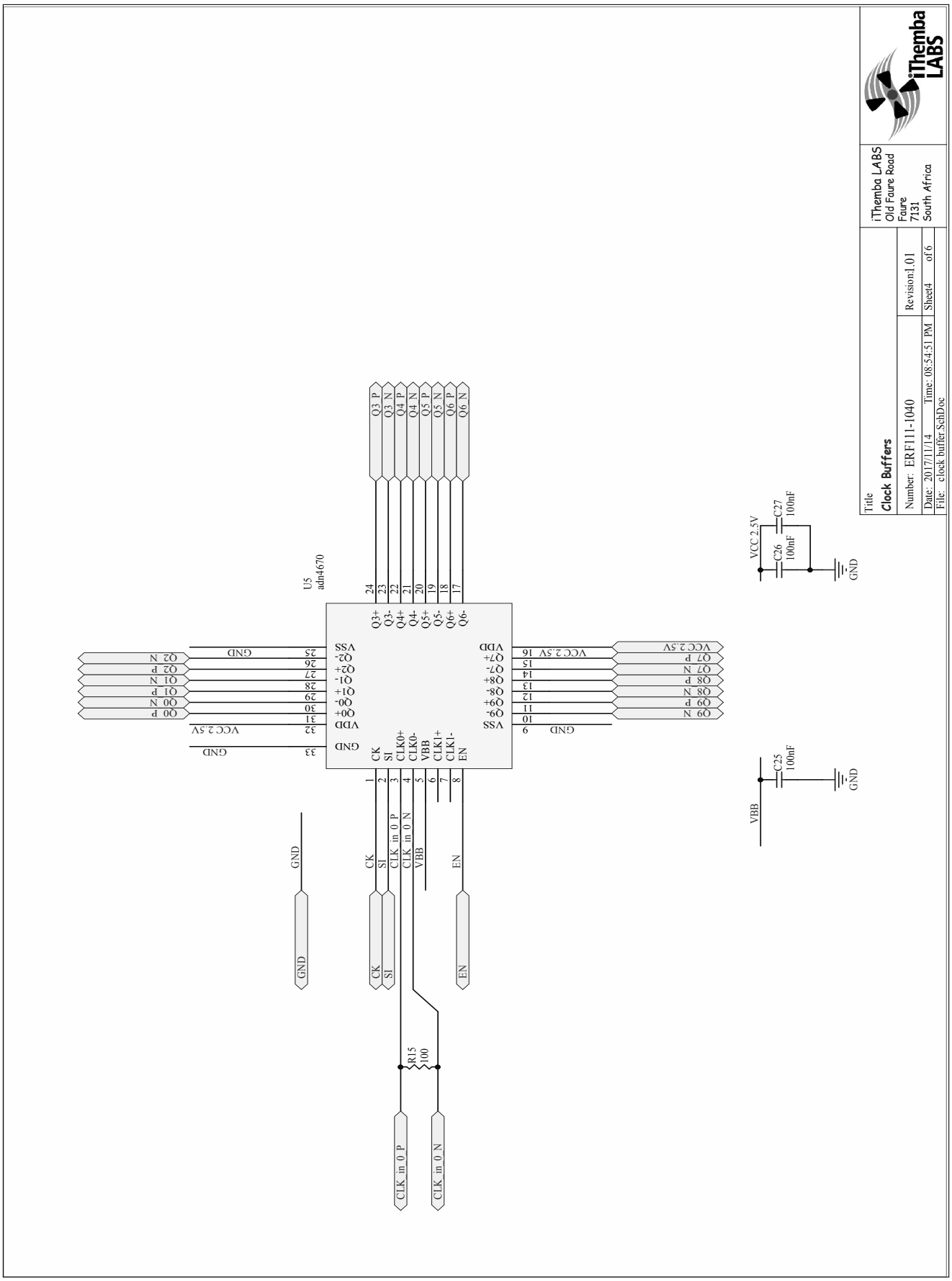


Appendix B. IF Sampling Module Schematics

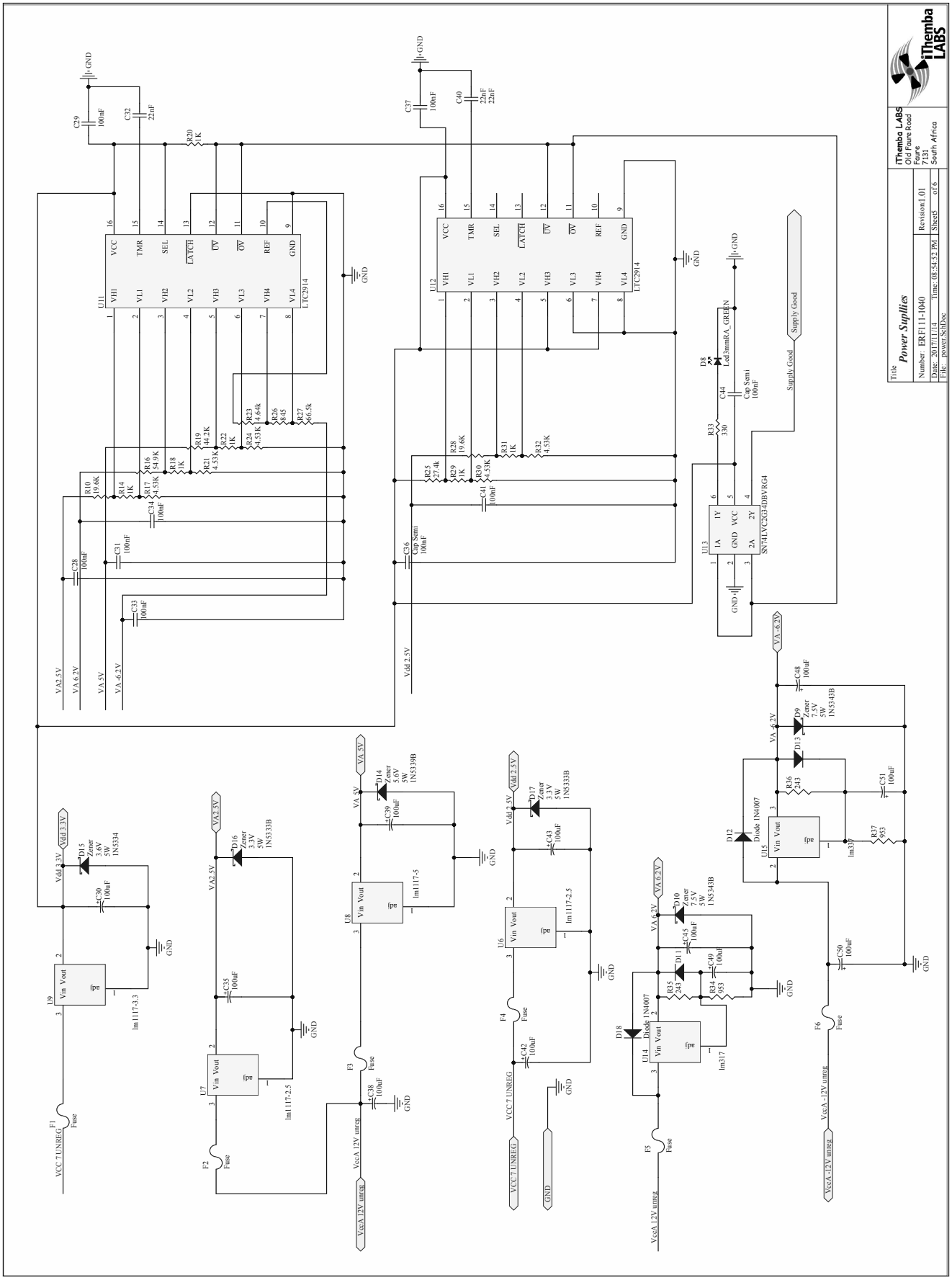


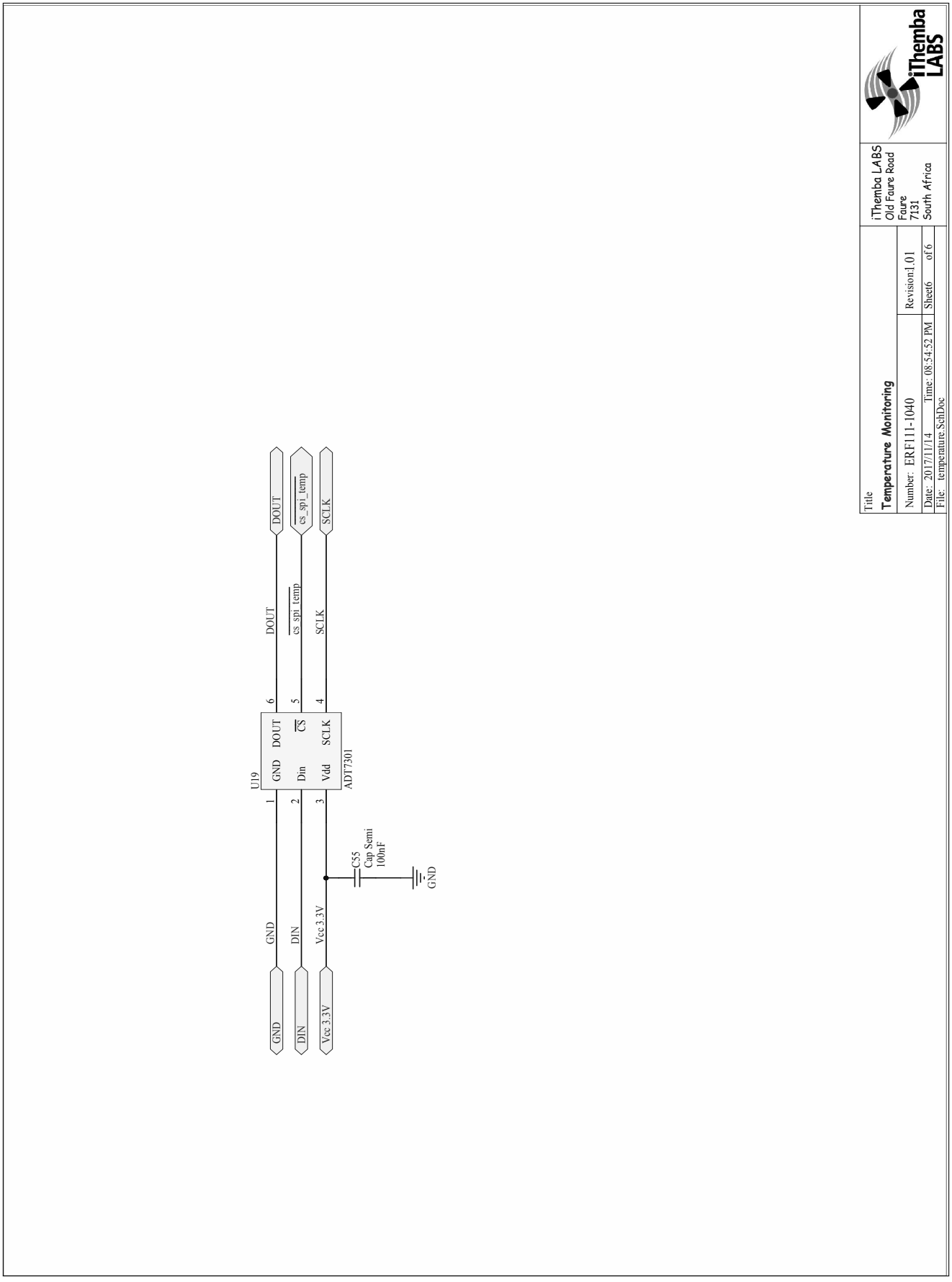
Appendix B. IF Sampling Module Schematics





Appendix B. IF Sampling Module Schematics





B.8 IF Sampling Module BOM

Table B.3: Bill of Materials: IF Sampling Module ERF111-1040

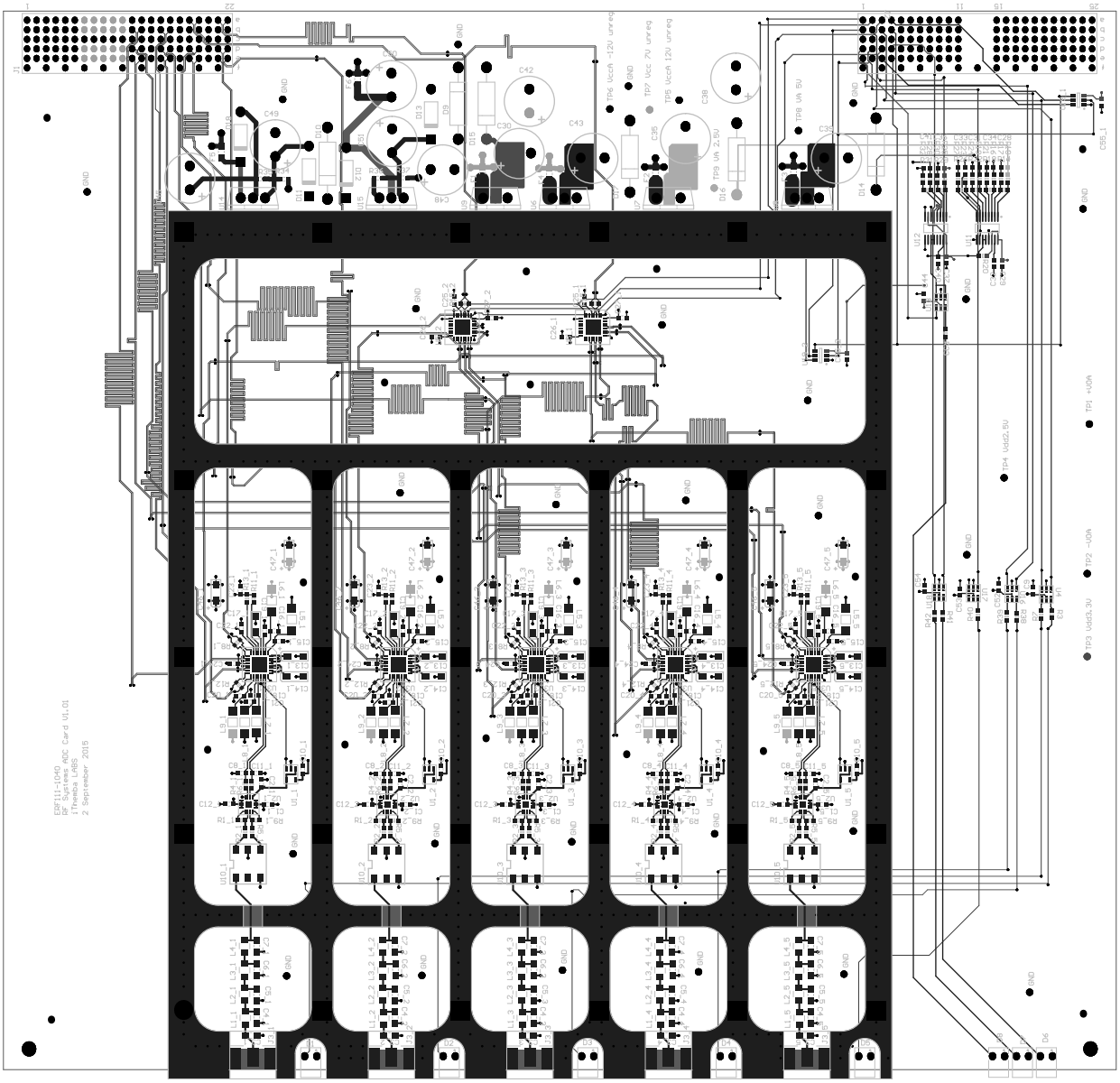
Index	Company Part No	Description	Qty	Manufacturer	Manufacturer Part No	Designator
1	ERF111-0001	4.53K 1% 0603 (1608) Surface Mounted Resistor	5	Yageo	2,3227E+11	R17, R21, R24, R30, R32
2	ERF111-0002	1K Ohm 0603 Surface Mounted Resistor	6	yageo	RC0603FR-071KL	R14, R18, R20, R22, R29, R31
3	ERF111-0003	19.6K Ohm 0603 Surface Mounted Resistor	2	Yageo	RC0603FR-0719K6L	R10, R28
4	ERF111-0004	Voltage Monitor	2	Linear Technologies	LTC2914CGN-1#PBF	U11, U12
5	ERF111-0005	Non inverting buffer	1	Texas Instruments	SN74LVC2G34DBVR	U13
6	ERF111-0006	330 Ohm 0603 Surface Mounted Resistor	1	yageo	RC0603FR-07330RL	R33
7	ERF111-0007	100nF 0603 Ceramic SMT Capacitor	81	Yageo	CC0603KRX7R9BB104	C1_1, C1_2, C1_3, C1_4, C1_5, C2_1, C2_2, C2_3, C2_4, C2_5, C9, C10_1, C10_2, C10_3, C10_4, C10_5, C12_1, C12_2, C12_3, C12_4, C12_5, C15_1, C15_2, C15_3, C15_4, C15_5, C16_1, C16_2, C16_3, C16_4, C16_5, C18_1, C18_2, C18_3, C18_4, C18_5, C20_1, C20_2, C2
8	ERF111-0008	22nF 0603 Ceramic SMT Capacitor	2	samsung	CL10B223KB8NNNC	C32, C40
9	ERF111-0010	2.5A 0805 fuse	6	AVX	F0805B2R50FSTR	F1, F2, F3, F4, F5, F6
10	ERF111-0016	100uF radial Capacitor 63V	11	Panasonic	EEUFC1J101B	C30, C35, C38, C39, C42, C43, C45, C48, C49, C50, C51
11	ERF111-0018	270 Ohm 0603 Surface Mounted Resistor	7	Yageo	RC0603FR-07270R	R3, R7, R38, R39, R40, R41, R42
12	ERF111-0019	PCB mount right angle LED 3mm RED	1	KingBright	L-710A8EW/1LID	D6
13	ERF111-0021	44.2k Ohm 0603 Surface Mounted Resistor	1	Yageo	RC0603FR-0744K2L	R19
14	ERF111-0022	27.4k Ohm 0603 Surface Mounted Resistor	1	Yageo	RC0603FR-0727K4L	R25
15	ERF111-0028	4.64k Ohm 0603 Surface Mounted Resistor	1	yageo	2,3227E+11	R23
16	ERF111-0031	13 bit Digital temperature sensor	2	Analog Devices	ADT7301ARTZ-500RL7	U19_1, U19_2
17	ERF111-0035	Z-Pack 2mm Hard Metric Type A 110 Position Female PCB Mount Connector	1	TE CONNECTIVITY	5352068-1	J2
18	ERF111-0036	Z-Pack 2mm Hard Metric Type B 110 Position Female Daughter Card Connector	1	TE CONNECTIVITY	5352152-1	J1
19	ERF111-0039	20 Ohm 0603 Surface Mounted Resistor	10	RS	RS-0603-20R-1%-0.1W	R4_1, R4_2, R4_3, R4_4, R4_5, R6_1, R6_2, R6_3, R6_4, R6_5
20	ERF111-0045	PCB mount right angle LED GREEN	7	KingBright	L-710A8EW/1LGD	D1, D2, D3, D4, D5, D7, D8
21	ERF111-0049	Inverting Schmitt Trigger	4	Texas Instruments	SN74LVC2G14DBVR	U4, U16, U17, U18
22	ERF111-0050	Zener Diode	1	On Semiconductor	1N5334B	D15
23	ERF111-0051	Zener Diode	1	On Semiconductor	1N5339B	D14
24	ERF111-0053	10nF 0603 Ceramic SMT Capacitor	5	Phycomp	CC0603KRX7R9BB103	C19_1, C19_2, C19_3, C19_4, C19_5
25	ERF111-0055	10uF Tantulum capacitor CASE A	25	Vishay	TR3A106K010C1800	C13_1, C13_2, C13_3, C13_4, C13_5, C14_1, C14_2, C14_3, C14_4, C14_5, C17_1, C17_2, C17_3, C17_4, C17_5, C46_1, C46_2, C46_3, C46_4, C46_5, C47_1, C47_2, C47_3, C47_4, C47_5
26	ERF111-0056	inductor beed 1000 Ohm 100MHz	25	Murata	BLM41PG102SN1L	L5_1, L5_2, L5_3, L5_4, L5_5, L6_1, L6_2, L6_3, L6_4, L6_5, L7_1, L7_2, L7_3, L7_4, L7_5, L8_1, L8_2, L8_3, L8_4, L8_5, L9_1, L9_2, L9_3, L9_4, L9_5
27	ERF111-0064	SMA Connector PCB mounted (DNP)	5	Amphenol	132289	J3_1, J3_2, J3_3, J3_4, J3_5
28	ERF111-0070	100 Ohm 0603 Surface Mounted Resistor	12	Yageo	RC0603FR-07100RL	R8_1, R8_2, R8_3, R8_4, R8_5, R12_1, R12_2, R12_3, R12_4, R12_5, R15_1, R15_2
29	ERF111-0081	3.3V Voltage regulator (DNP)	1	STMicroelectronics	LD1117V33C	U9
30	ERF111-0082	5V Voltage regulator (DNP)	1	STMicroelectronics	LD1117V50	U8
31	ERF111-0083	2.5V Voltage regulator (DNP)	2	Texas Instruments	LM1117T-2.5/NOPB	U6, U7
32	ERF111-0084	953 Ohm 0603 Surface Mounted Resistor	2	Panasonic	ERA3AEB9530V	R34, R37
33	ERF111-0085	845 Ohm 0603 Surface Mounted Resistor	1	RS	RS-0603-845R-1%-0.1W	R26

Table B.3 continued: Bill of Materials: IF Sampling Module ERF111-1020

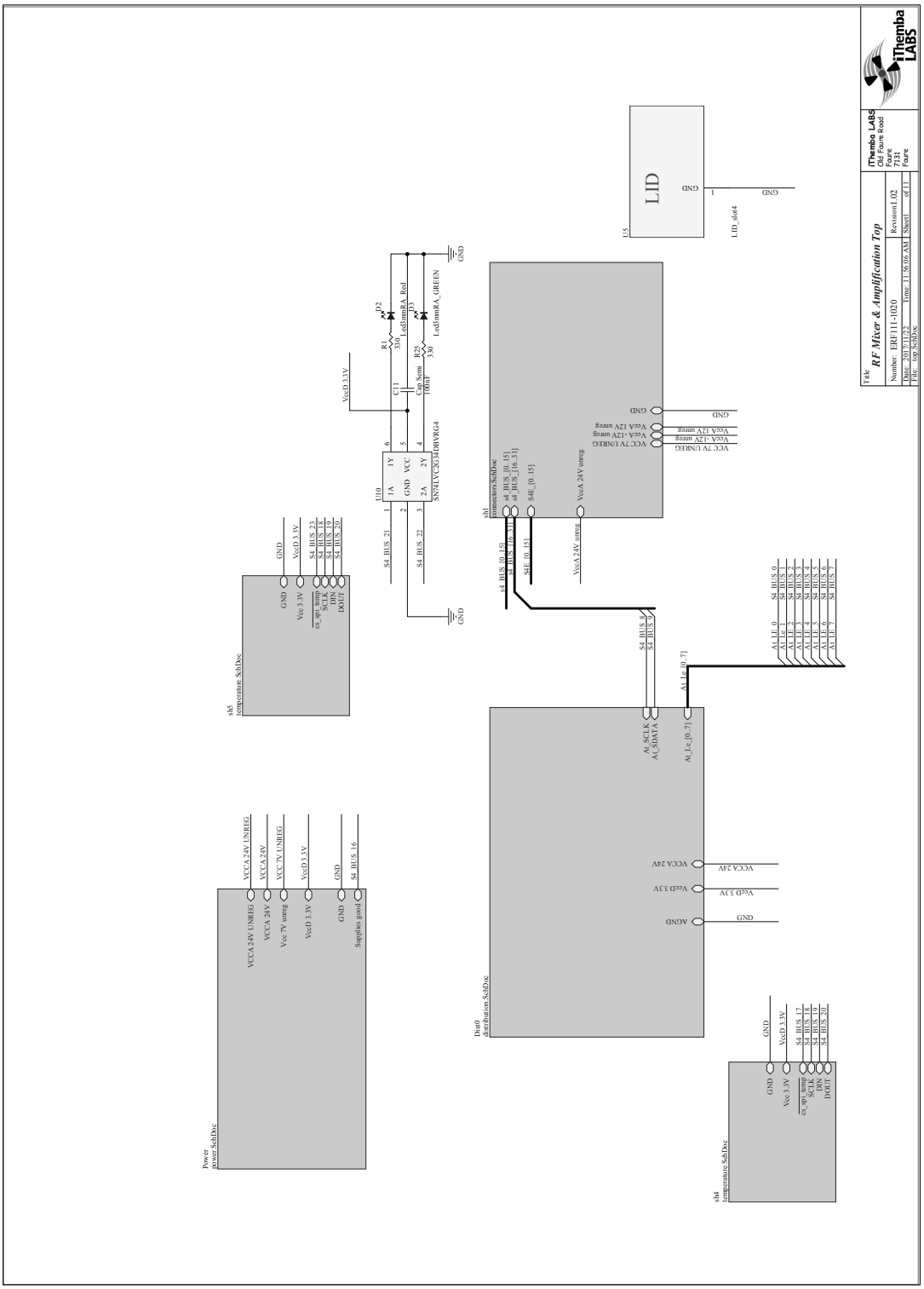
Index	Company Part No	Description	Qty	Manufacturer	Manufacturer Part No	Designator
35	ERF111-0087	243 Ohm 0603 Surface Mounted Resistor	2	Panasonic	ERA3AEB2430V	R35, R36
36	ERF111-0088	66.5k Ohm 0603 Surface Mounted Resistor	1	Yageo	2,3227E+11	R27
37	ERF111-0089	56pF 0603 Ceramic SMT Capacitor	10	Murata	GRM1885C1H560JA01D	C8_1, C8_2, C8_3, C8_4, C8_5, C11_1, C11_2, C11_3, C11_4, C11_5
38	ERF111-0090	54.9k Ohm 0603 Surface Mounted Resistor	1	Vishay	CRCW060354K9FKEA	R16
39	ERF111-0093	8.2uH Small Inductor	10	Toko	FSLM2520-8R2J	L2_1, L2_2, L2_3, L2_4, L2_5, L3_1, L3_2, L3_3, L3_4, L3_5
40	ERF111-0094	6.8uH Small Inductor	10	Toko	FSLM2520-6R8J	L1_1, L1_2, L1_3, L1_4, L1_5, L4_1, L4_2, L4_3, L4_4, L4_5
41	ERF111-0095	4.7nF 0805 Ceramic SMT Capacitor	15	TDK	C2012C0G1H472J060AA	C4_1, C4_2, C4_3, C4_4, C4_5, C5_1, C5_2, C5_3, C5_4, C5_5, C6_1, C6_2, C6_3, C6_4, C6_5
42	ERF111-0097	2.7nF 0805 Ceramic SMT Capacitor	10	TDK	C2012C0G1H272J060AA	C3_1, C3_2, C3_3, C3_4, C3_5, C7_1, C7_2, C7_3, C7_4, C7_5
43	ERF111-0098	AD7626 SAR 10MSPS 16 bit ADC	5	Analog Devices	AD7626BCPZ	U3_1, U3_2, U3_3, U3_4, U3_5
44	ERF111-0099	Amplifier 2.7 V, 800 micro A, 80 MHz	5	Analog Devices	AD8031ARTZ	U1_1, U1_2, U1_3, U1_4, U1_5
45	ERF111-0100	Differential Amplifier 16-Pin ADA4932	5	Analog Devices	ADA4932-1YCPZ-R2	U2_1, U2_2, U2_3, U2_4, U2_5
46	ERF111-0102	1 Amp General Purpose Rectifier Diode	4	Vishay	1N4002-E3/73	D11, D12, D13, D18
47	ERF111-0103	WB16-6TSLB 16:1 tranformer	5	Coilcraft	WB16-6TSLB	U10_1, U10_2, U10_3, U10_4, U10_5
48	ERF111-0105	adn4670 lvds clock buffer	2	Analog Devices	ADN4670BCPZ	U5_1, U5_2
49	ERF111-0107	Adjustable positive Voltage Regulator (DNP)	1	Fairchild	LM317T	U14
50	ERF111-0108	Adjustable negative Voltage Regulator (DNP)	1	ON Semiconductor	LM337TG	U15
51	ERF111-0109	Zener Diode (DNP)	2	ON Semiconductor	1N5343BG	D9, D10
52	ERF111-0110	Zener Diode (DNP)	2	ON Semiconductor	1N5333B	D16, D17
53	ERF111-0111	10k Ohm 0603 Surface Mounted Resistor	10	Yageo	RC0603FR-0710KL	R11_1, R11_2, R11_3, R11_4, R11_5, R13_1, R13_2, R13_3, R13_4, R13_5
54	ERF111-0150	PWB-16-BLB	5	Coilcraft	PWB-16-BLB	-

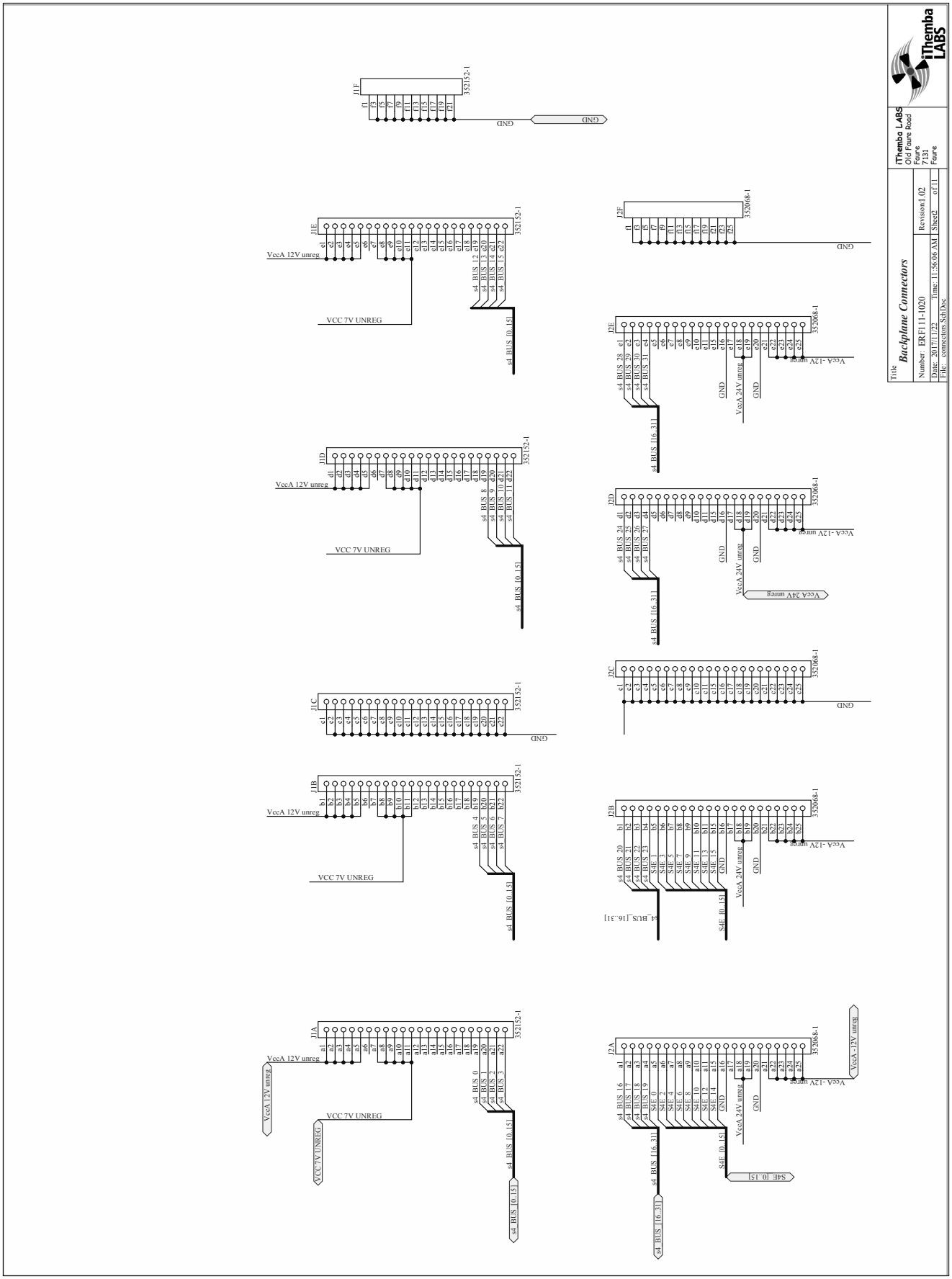
B.9 IF Sampling Module PCB Layout

B.9.1 IF Sampling PCB 8 layer Composite Print

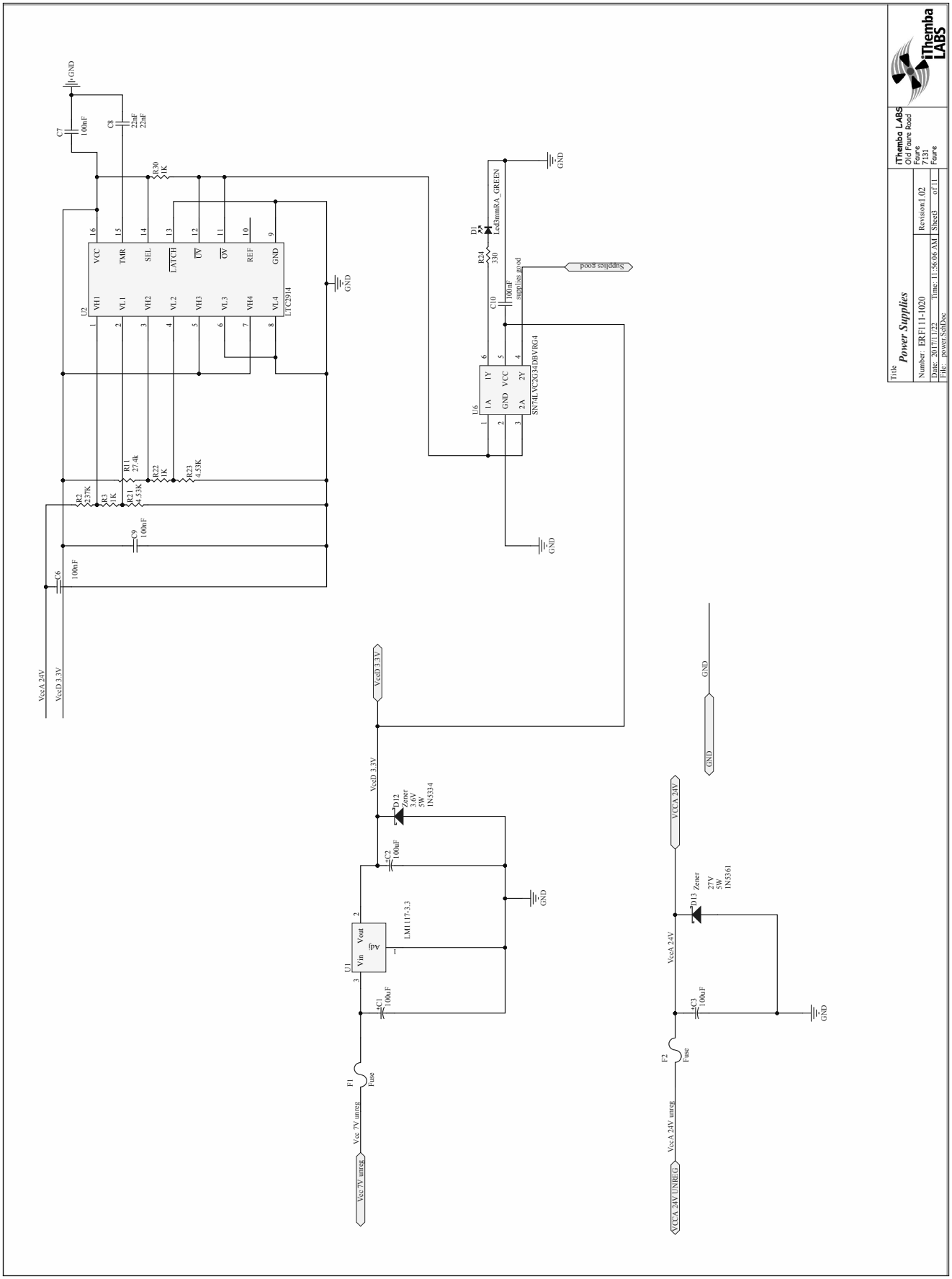


B.10 RF Amplification and Mixing Module Schematics

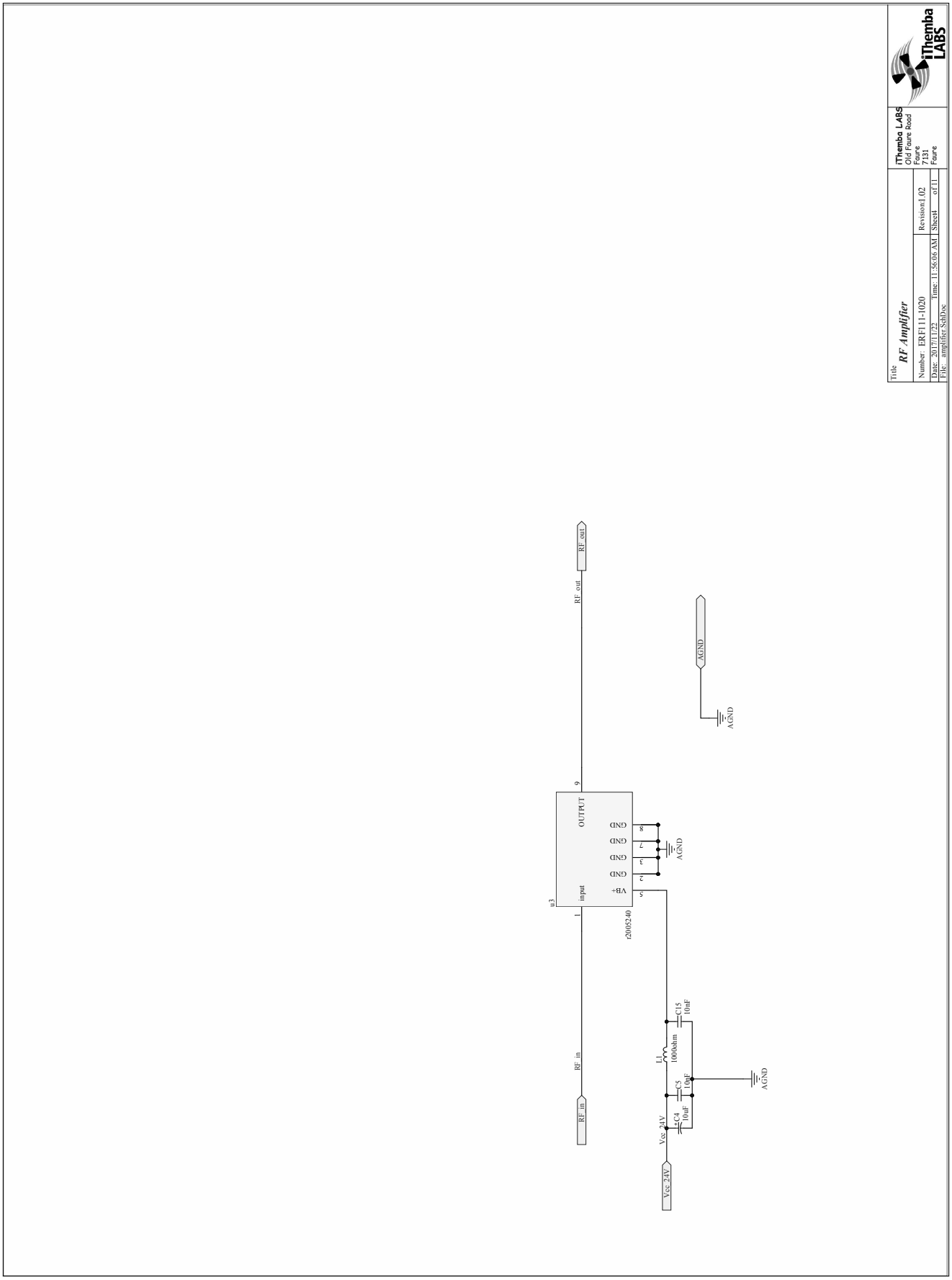


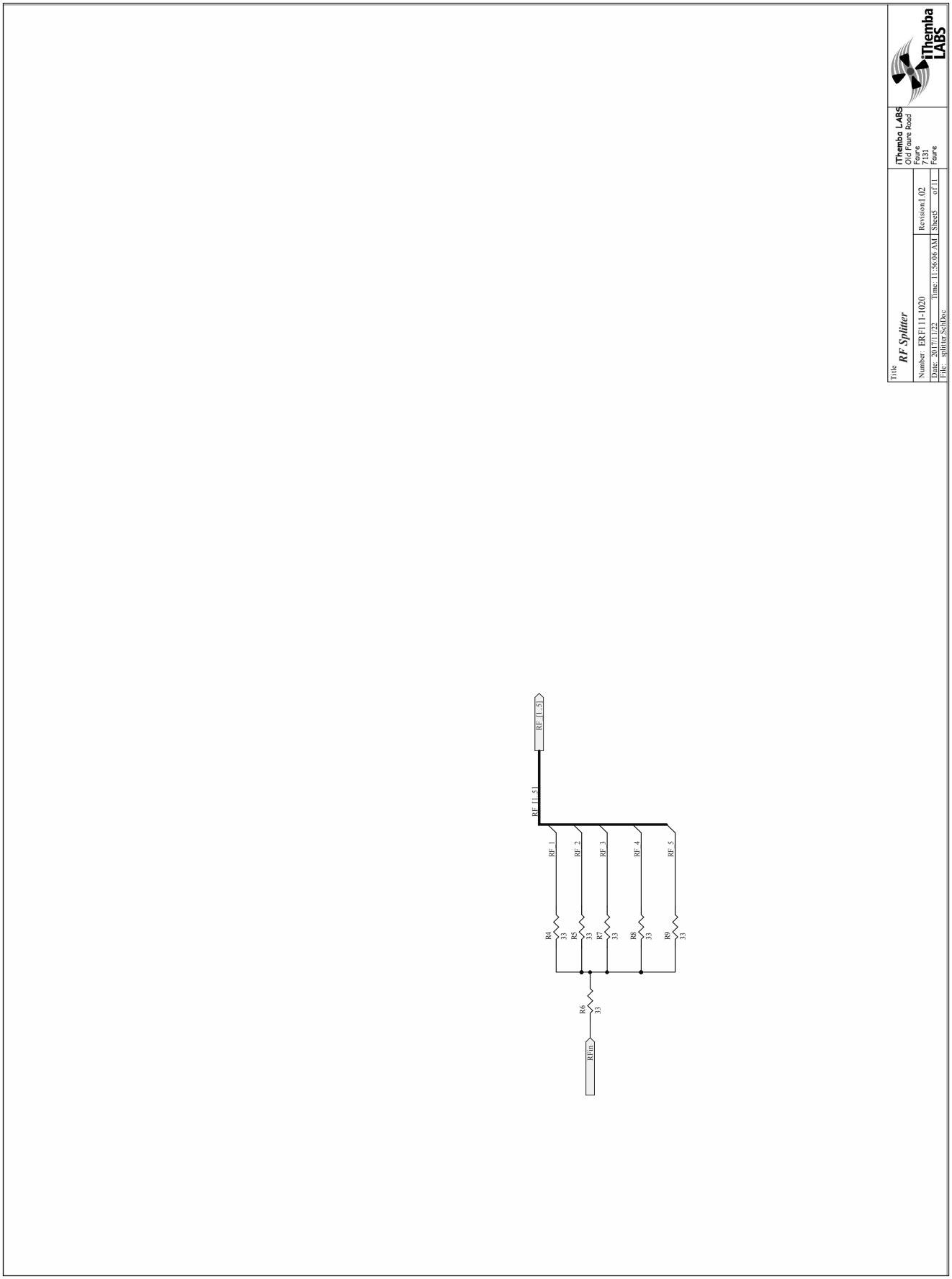


Appendix B. RF Amplification and Mixing Module Schematics

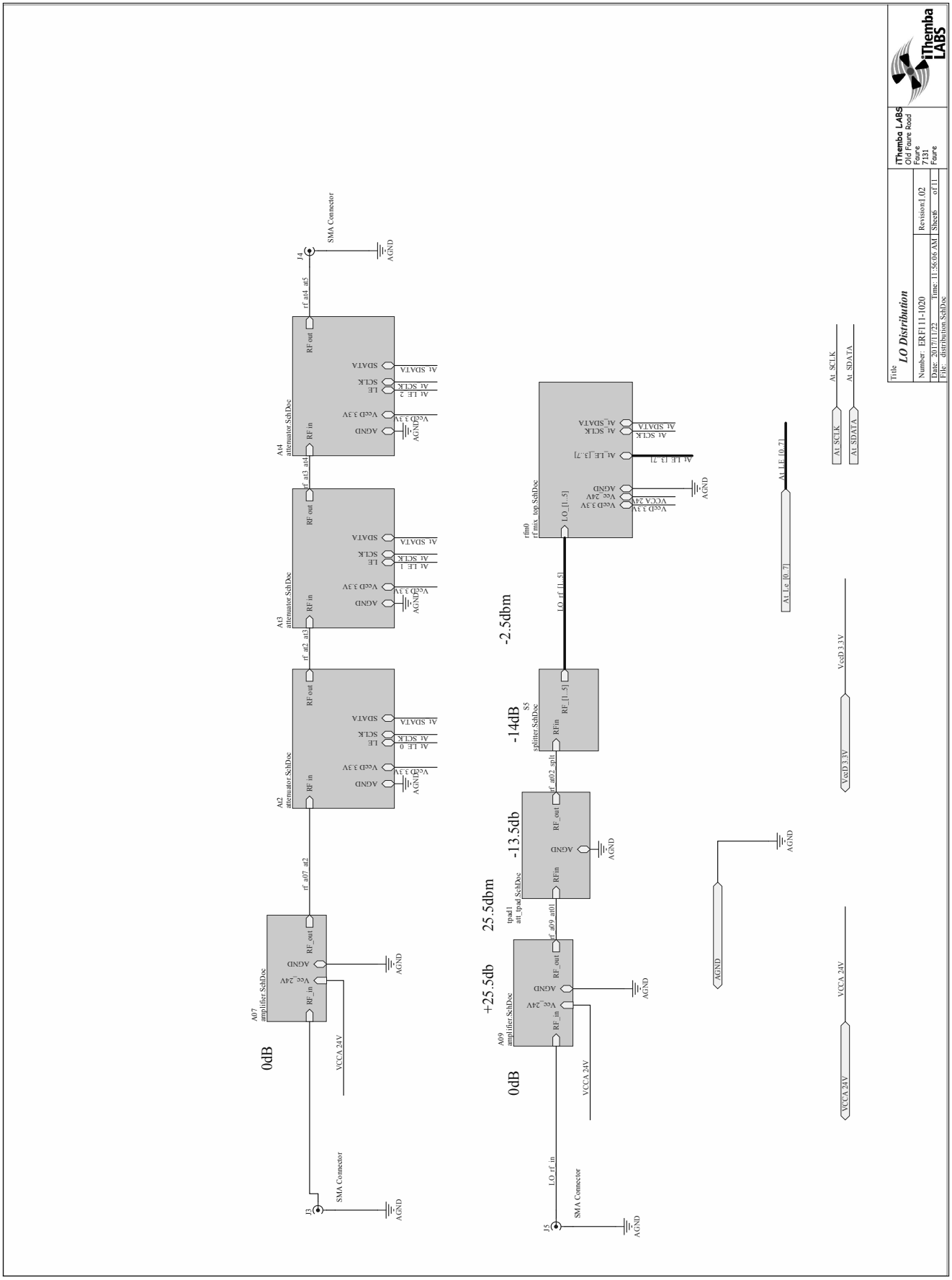


Appendix B. RF Amplification and Mixing Module Schematics

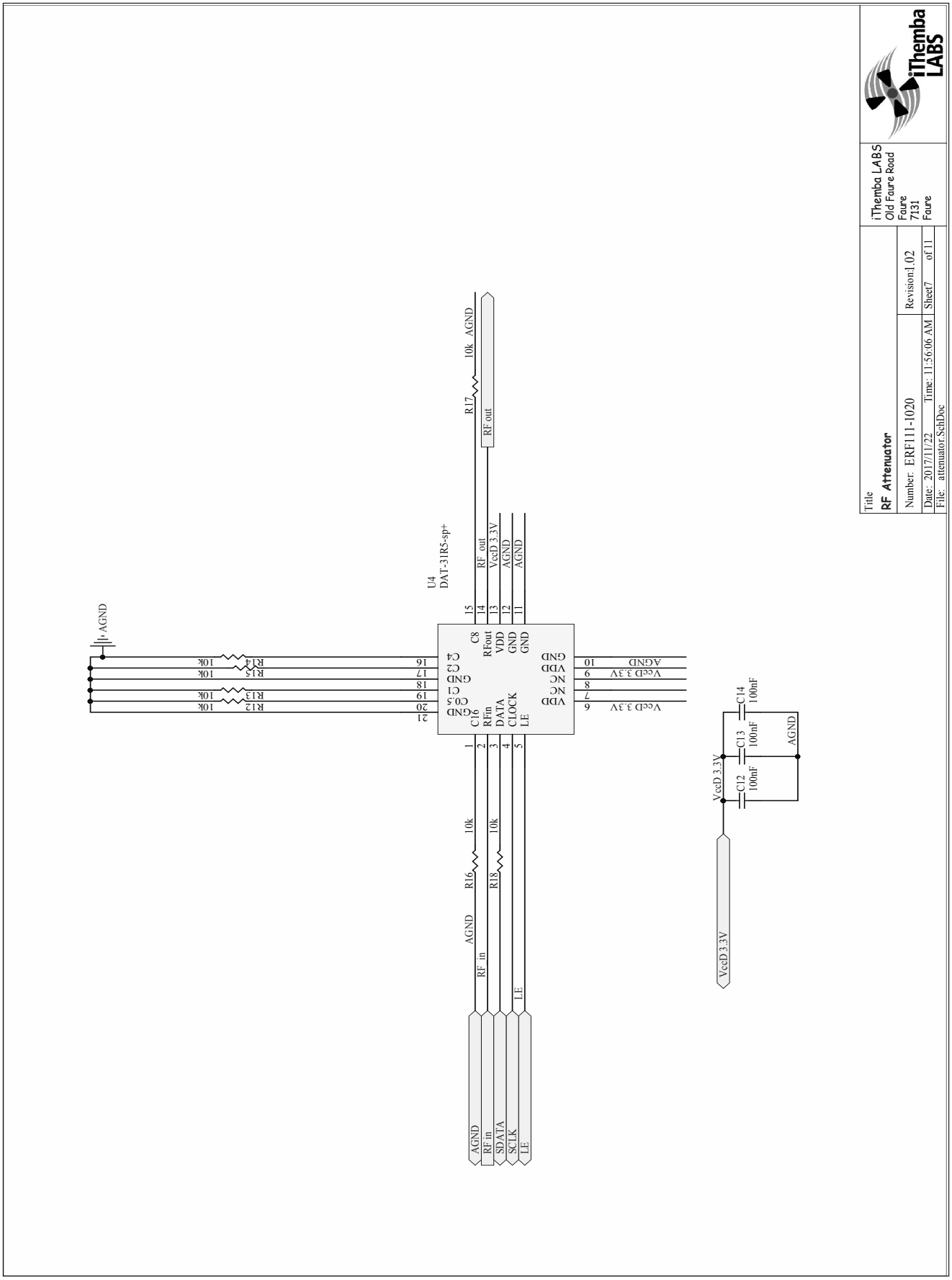


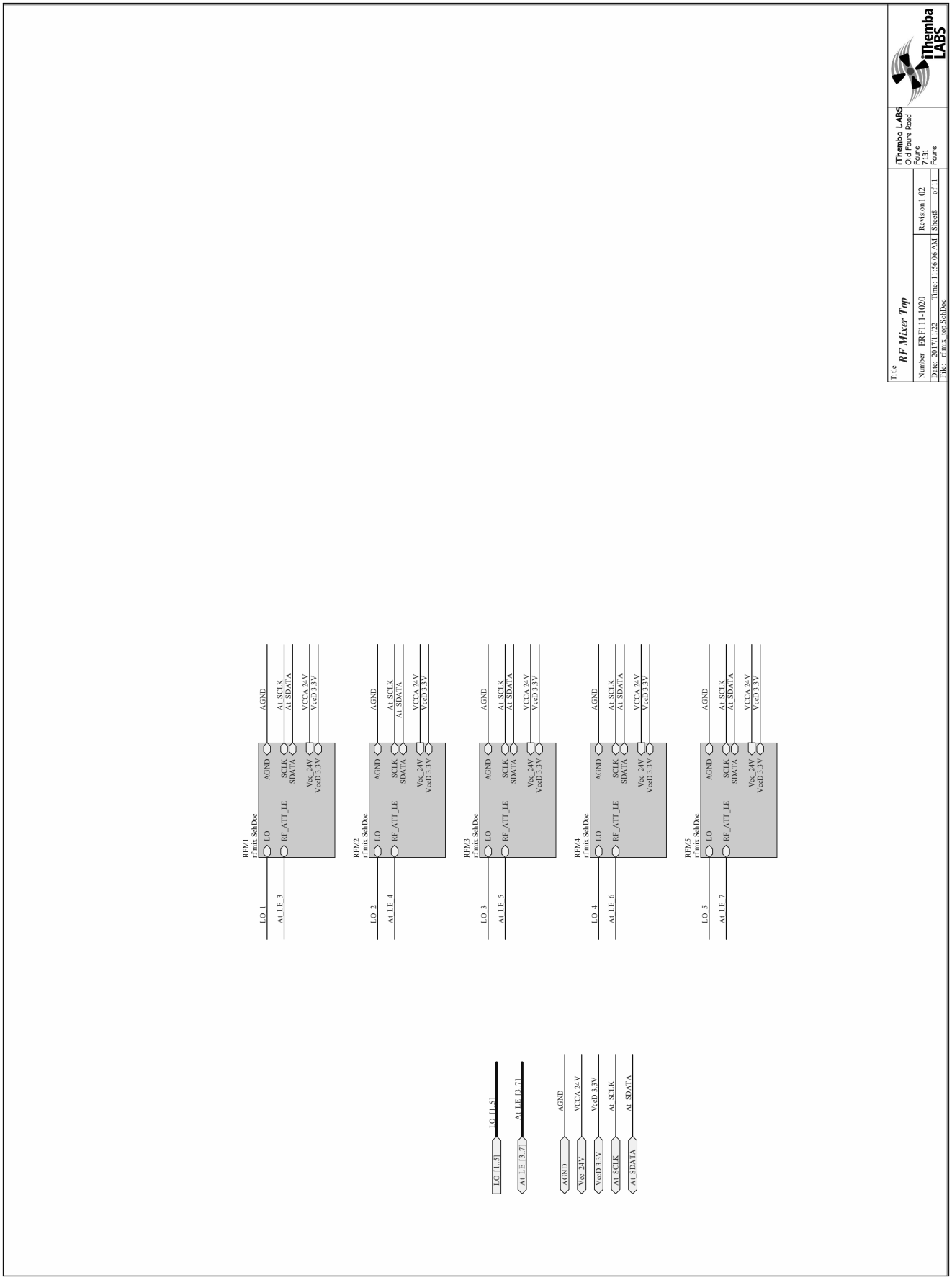


Appendix B. RF Amplification and Mixing Module Schematics

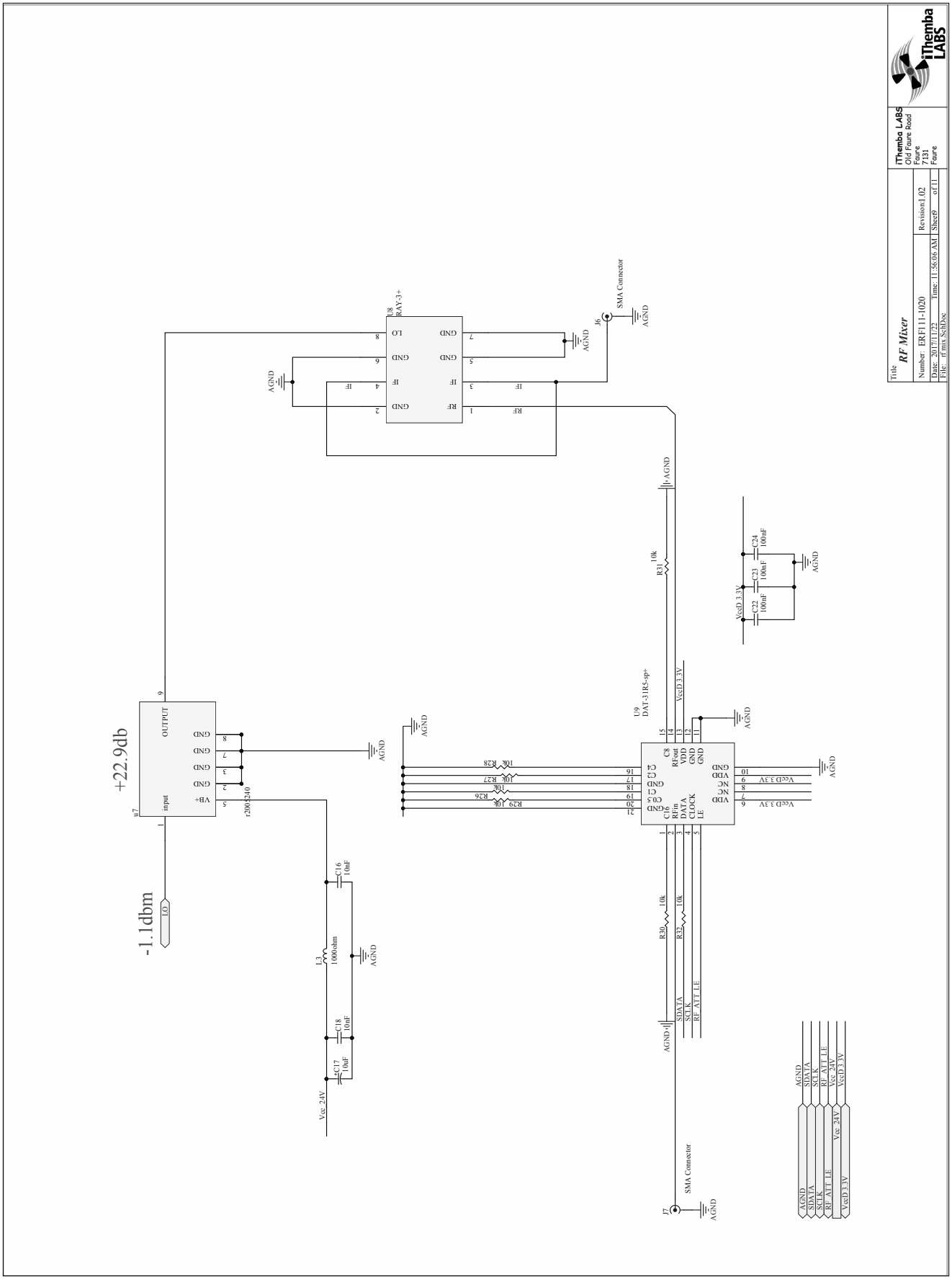


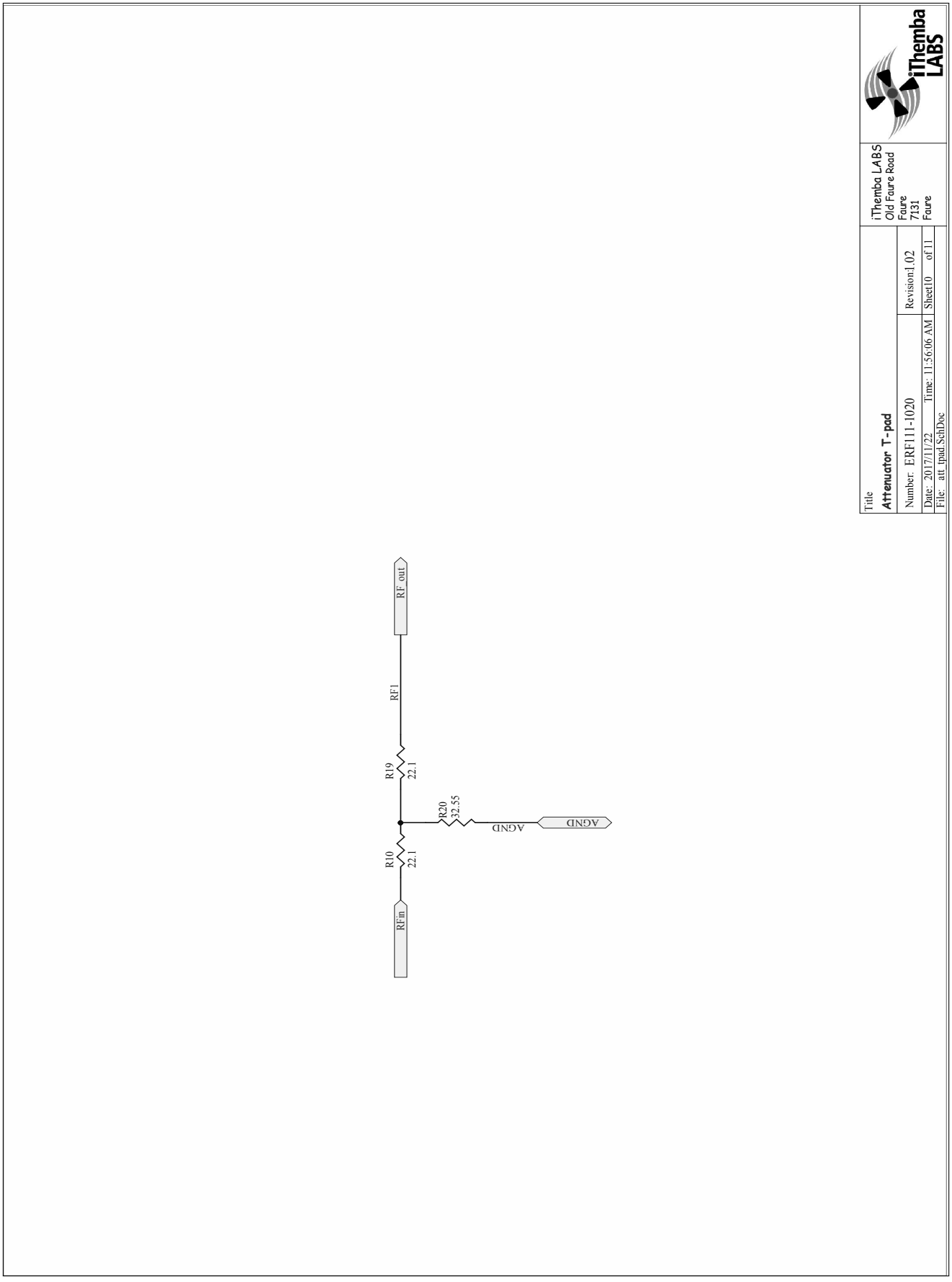
Appendix B. RF Amplification and Mixing Module Schematics

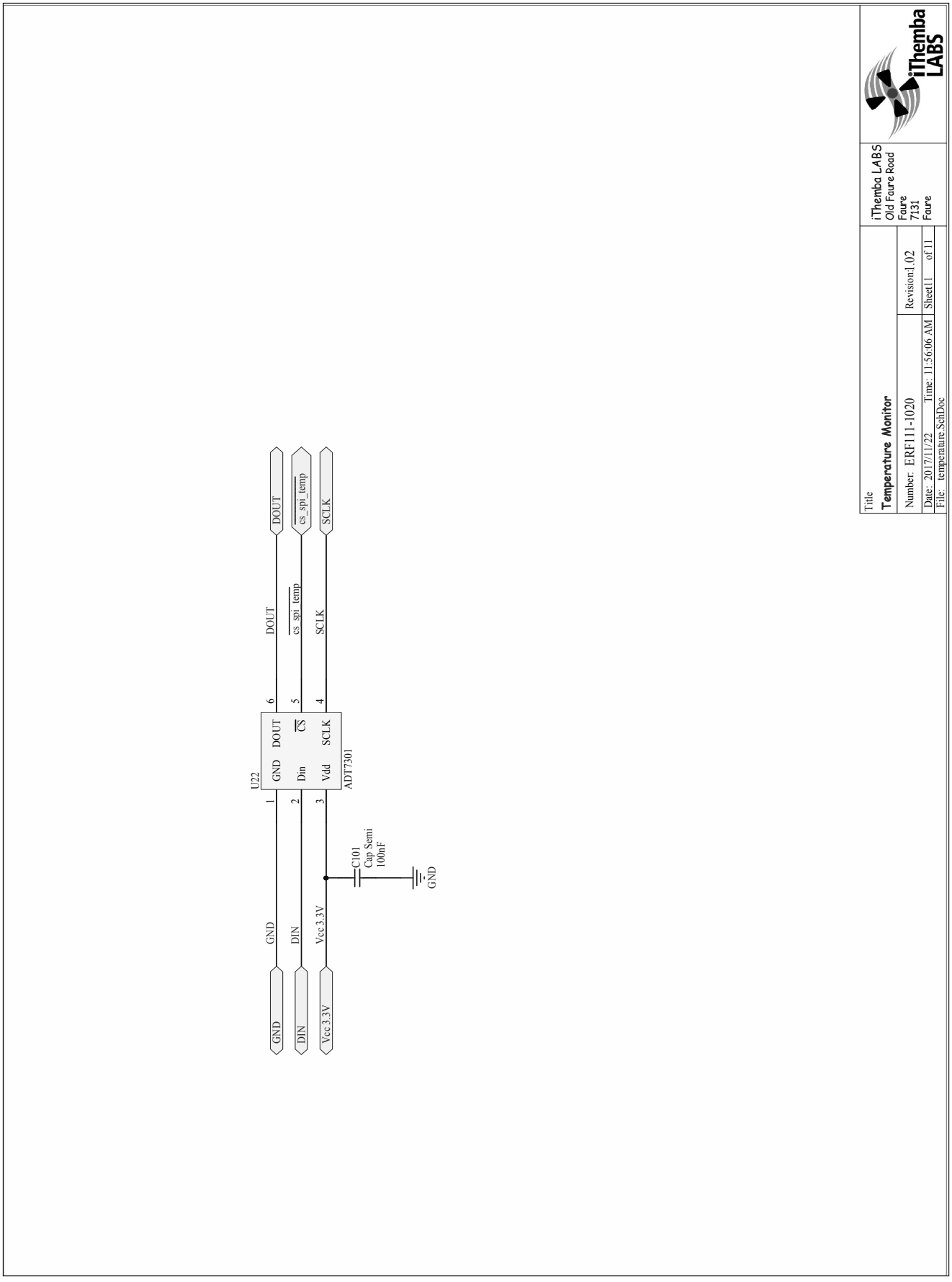




Appendix B. RF Amplification and Mixing Module Schematics







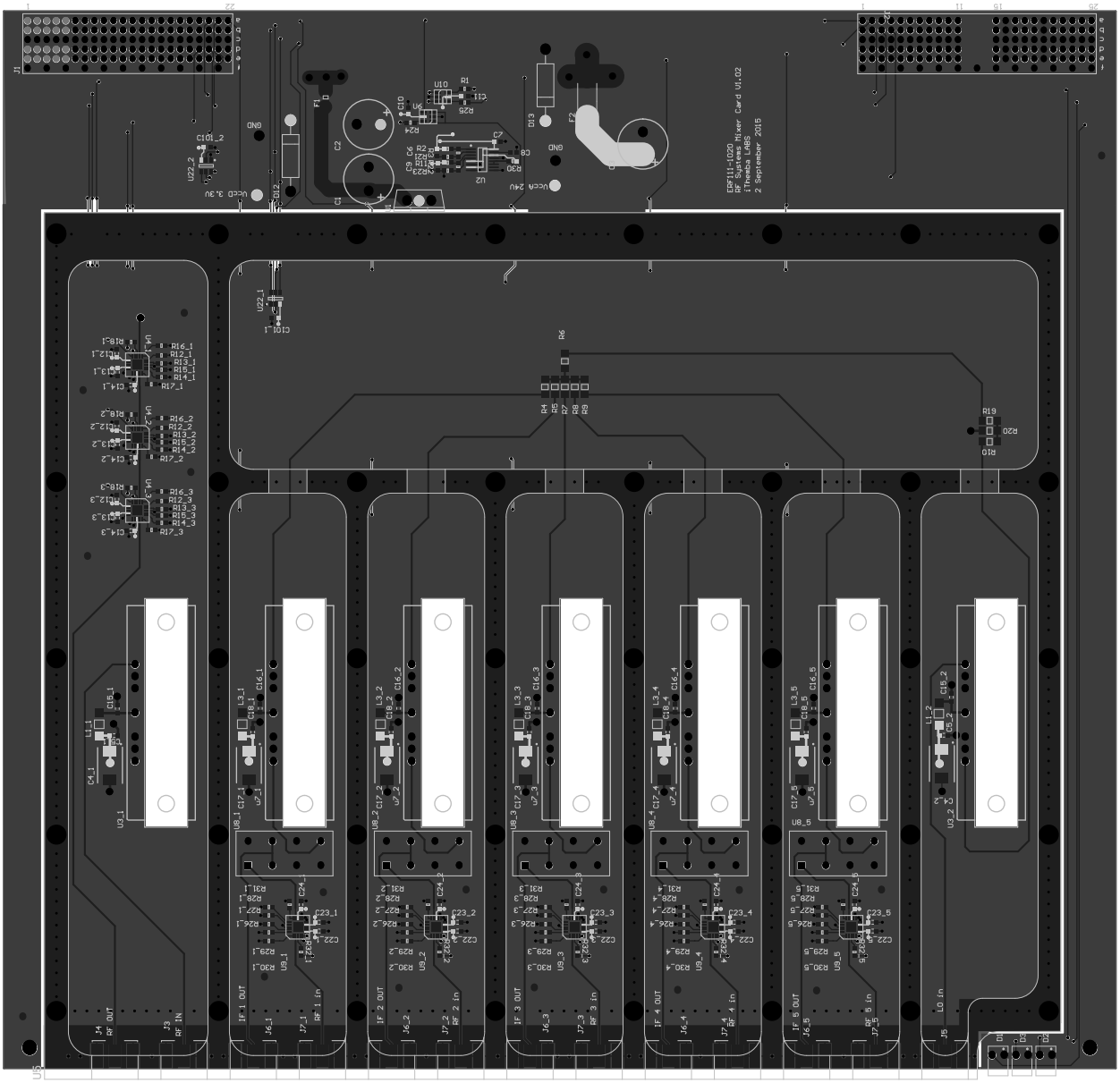
B.11 RF Amplification and Mixing Module BOM

Table B.4: Bill of Materials: RF Amplification and Mixing Module ERF111-1020

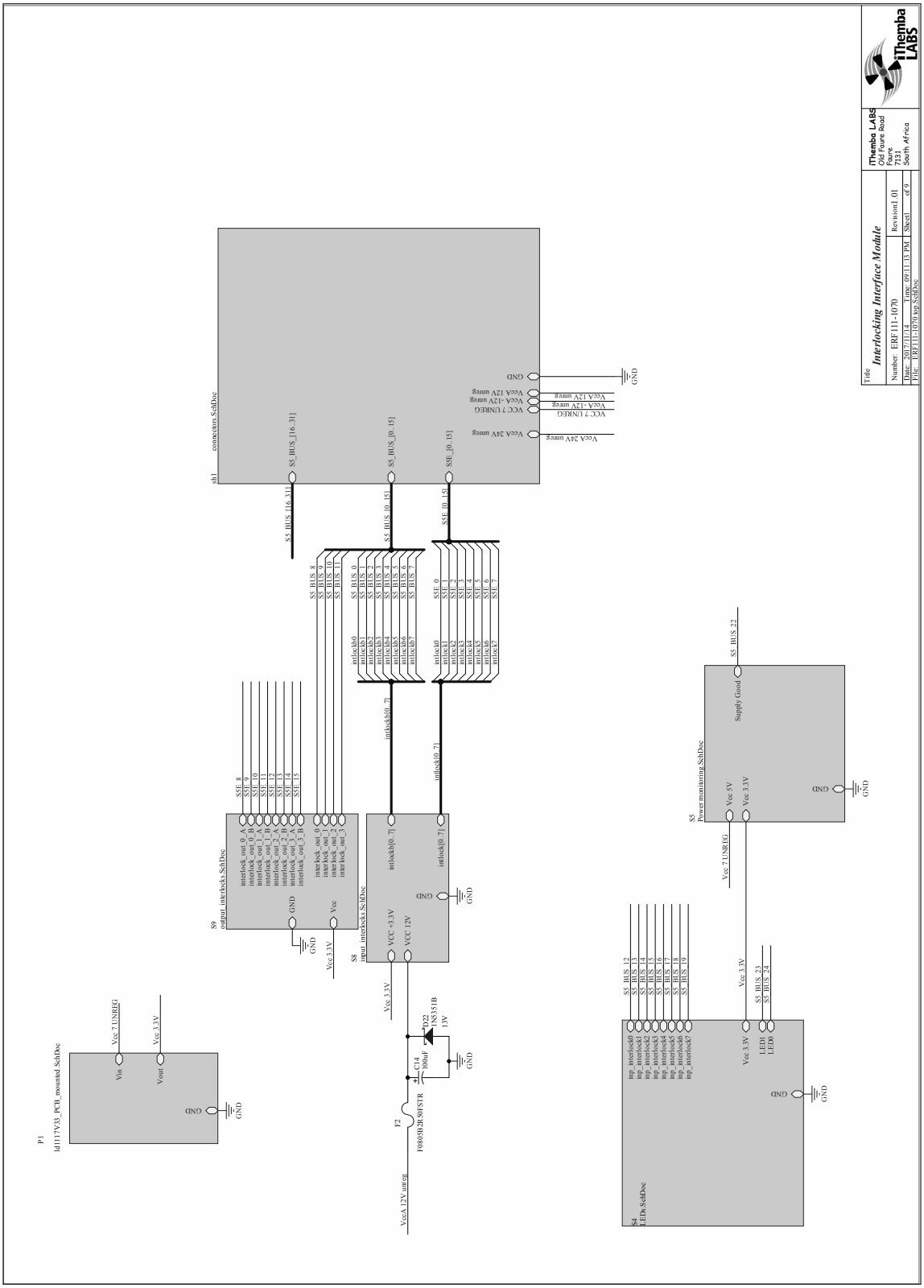
Index	Company Part No	Description	Qty	Manufacturer	Manufacturer Part No	Designator
1	ERF111-0001	4.53K 1% 0603 (1608) Surface Mounted Resistor	2	Yageo	232270464532	R21, R23
2	ERF111-0002	1K Ohm 0603 Surface Mounted Resistor	3	yageo	RC0603FR-071KL	R3, R22, R30
3	ERF111-0004	Voltage Monitor	1	Linear Technologies	LTC2914CGN-1#PBF	U2
4	ERF111-0005	Non inverting buffer	2	Texas Instruments	SN74LVC2G34DBVR	U6, U10
5	ERF111-0006	330 Ohm 0603 Surface Mounted Resistor	3	yageo	RC0603FR-07330RL	R1, R24, R25
6	ERF111-0007	100nF 0603 Ceramic SMT Capacitor	31	Yageo	CC0603KRX7R9BB104	C6, C7, C9, C10, C11, C12_1, C12_2, C12_3, C13_1, C13_2, C13_3, C14_1, C14_2, C14_3, C22_1, C22_2, C22_3, C22_4, C22_5, C23_1, C23_2, C23_3, C23_4, C23_5, C24_1, C24_2, C24_3, C24_4, C24_5, C101_1, C101_2
7	ERF111-0008	22nF 0603 Ceramic SMT Capacitor	1	samsung	CL10B223KB8NNNC	C8
8	ERF111-0010	2.5A 0805 fuse	1	AVX	F0805B2R50FSTR	F1
9	ERF111-0016	100uF radial Capacitor 63V	3	Panasonic	EEUFC1J101B	C1, C2, C3
10	ERF111-0019	PCB mount right angle LED 3mm RED	1	KingBright	L-710A8EW/1LID	D2
11	ERF111-0022	27.4k Ohm 0603 Surface Mounted Resistor	1	Yageo	RC0603FR-0727K4L	R11
12	ERF111-0025	237k Ohm 0603 Surface Mounted Resistor	1	RS	RS-0603-237K-1%-0.1W	R2
13	ERF111-0031	13 bit Digital temperature sensor	2	Analog Devices	ADT7301ARTZ-500RL7	U22_1, U22_2
14	ERF111-0035	Z-Pack 2mm Hard Metric Type A 110 Position Female PCB Mount Connector	1	TE CONNECTIVITY	5352068-1	J2
15	ERF111-0036	Z-Pack 2mm Hard Metric Type B 110 Position Female Daughter Card Connector	1	TE CONNECTIVITY	5352152-1	J1
16	ERF111-0045	PCB mount right angle LED GREEN	2	KingBright	L-710A8EW/1LGD	D1, D3
17	ERF111-0050	Zener Diode	1	On Semiconductor	1N5334B	D12
18	ERF111-0053	10nF 0603 Ceramic SMT Capacitor	14	Phycomp	CC0603KRX7R9BB103	C5_1, C5_2, C15_1, C15_2, C16_1, C16_2, C16_3, C16_4, C16_5, C18_1, C18_2, C18_3, C18_4, C18_5
19	ERF111-0056	inductor beed 1000 Ohm 100MHz	7	Murata	BLM41PG102SN1L	L1_1, L1_2, L3_1, L3_2, L3_3, L3_4, L3_5
20	ERF111-0064	SMA Connector PCB mounted (DNP)	13	Amphenol	132289	J3, J4, J5, J6_1, J6_2, J6_3, J6_4, J6_5, J7_1, J7_2, J7_3, J7_4, J7_5
21	ERF111-0081	3.3V Voltage regulator (DNP)	1	STMicroelectronics	LD1117V33C	U1
22	ERF111-0111	10k Ohm 0603 Surface Mounted Resistor	56	Yageo	RC0603FR-0710KL	R12_1, R12_2, R12_3, R13_1, R13_2, R13_3, R14_1, R14_2, R14_3, R15_1, R15_2, R15_3, R16_1, R16_2, R16_3, R17_1, R17_2, R17_3, R18_1, R18_2, R18_3, R26_1, R26_2, R26_3, R26_4, R26_5, R27_1, R27_2, R27_3, R27_4, R27_5, R28_1, R28_2, R28_3, R28_4, R28_5, R29
23	ERF111-0112	10 uF Tantalum SMT Capacitor, Case E	7	Vishay	TR3E106K035C0250	C4_1, C4_2, C17_1, C17_2, C17_3, C17_4, C17_5
24	ERF111-0114	Resistor 22.1 1206	2	Vishay	CRCW120622R1FKEA	R10, R19
25	ERF111-0115	Resistor 32.4 Ohm 1206	1	Vishay	CRCW120632R4FKEA	R20
26	ERF111-0116	Resistor 33.2 Ohm 1206	6	Vishay	CRCW120633R2FKEA	R4, R5, R6, R7, R8, R9
27	ERF111-0117	32 db digital step antenuator	8	Mini cirucits	DAT-31R5-sp+	U4_1, U4_2, U4_3, U9_1, U9_2, U9_3, U9_4, U9_5
28	ERF111-0118	Fuse UMF250 4A 250VAC 125VDC	1	schurter	3405.0172.24	F2
29	ERF111-0119	25.5 dB RF Amplifier	7	RFMD	-	u3_1, u3_2, u7_1, u7_2, u7_3, u7_4, u7_5
30	ERF111-0120	RF MIXER	5	Mini cirucits	RAY-3+	U8_1, U8_2, U8_3, U8_4, U8_5
31	ERF111-0121	Zener Diode	1	ON Semiconductor	1N5361B	D13

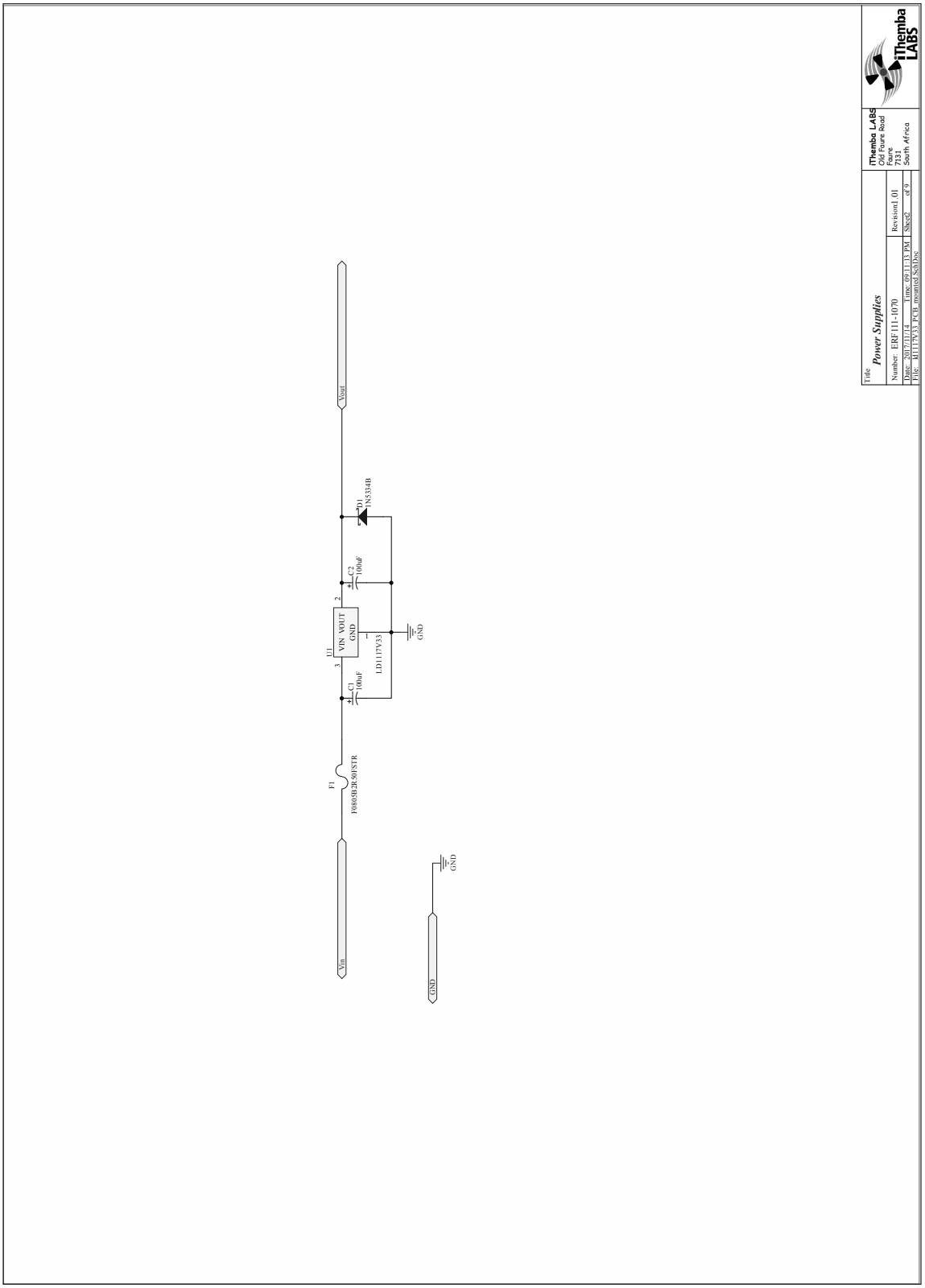
B.12 RF Amplification and Mixing Module PCB Layout

B.12.1 RF Amplification and Mixing PCB 4 Layer Composite Print

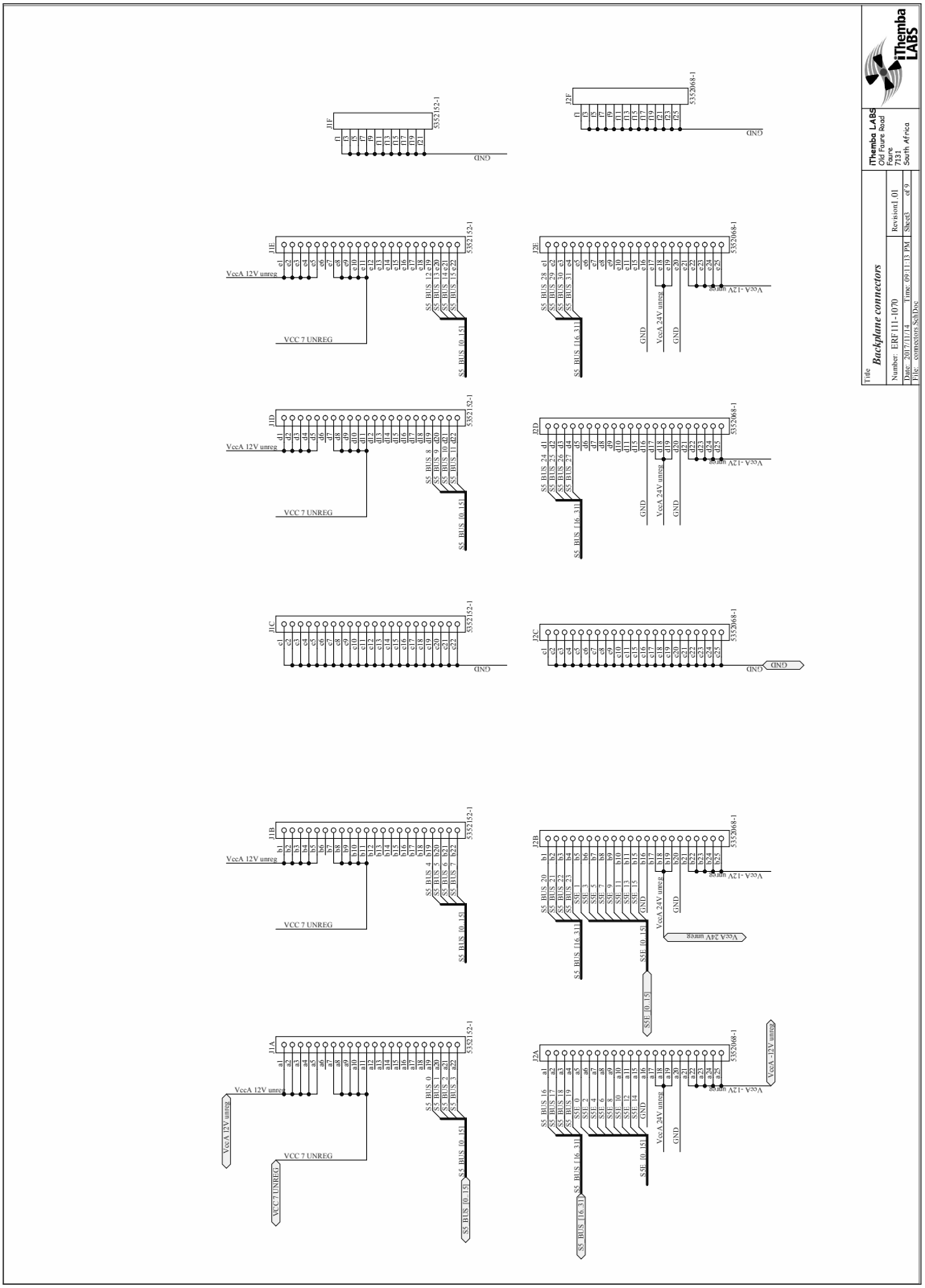


B.13 RF Interlocking Module Schematics

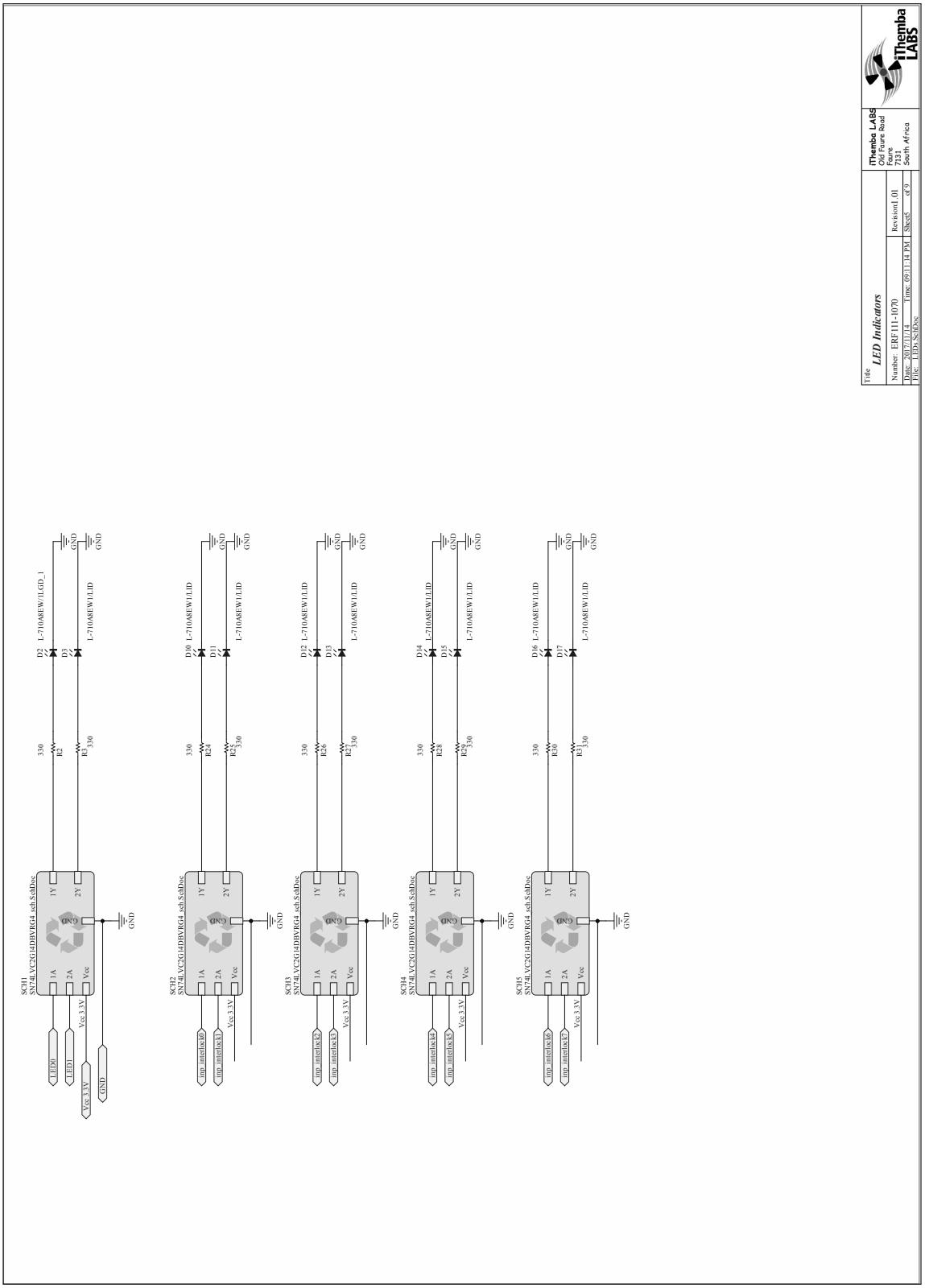




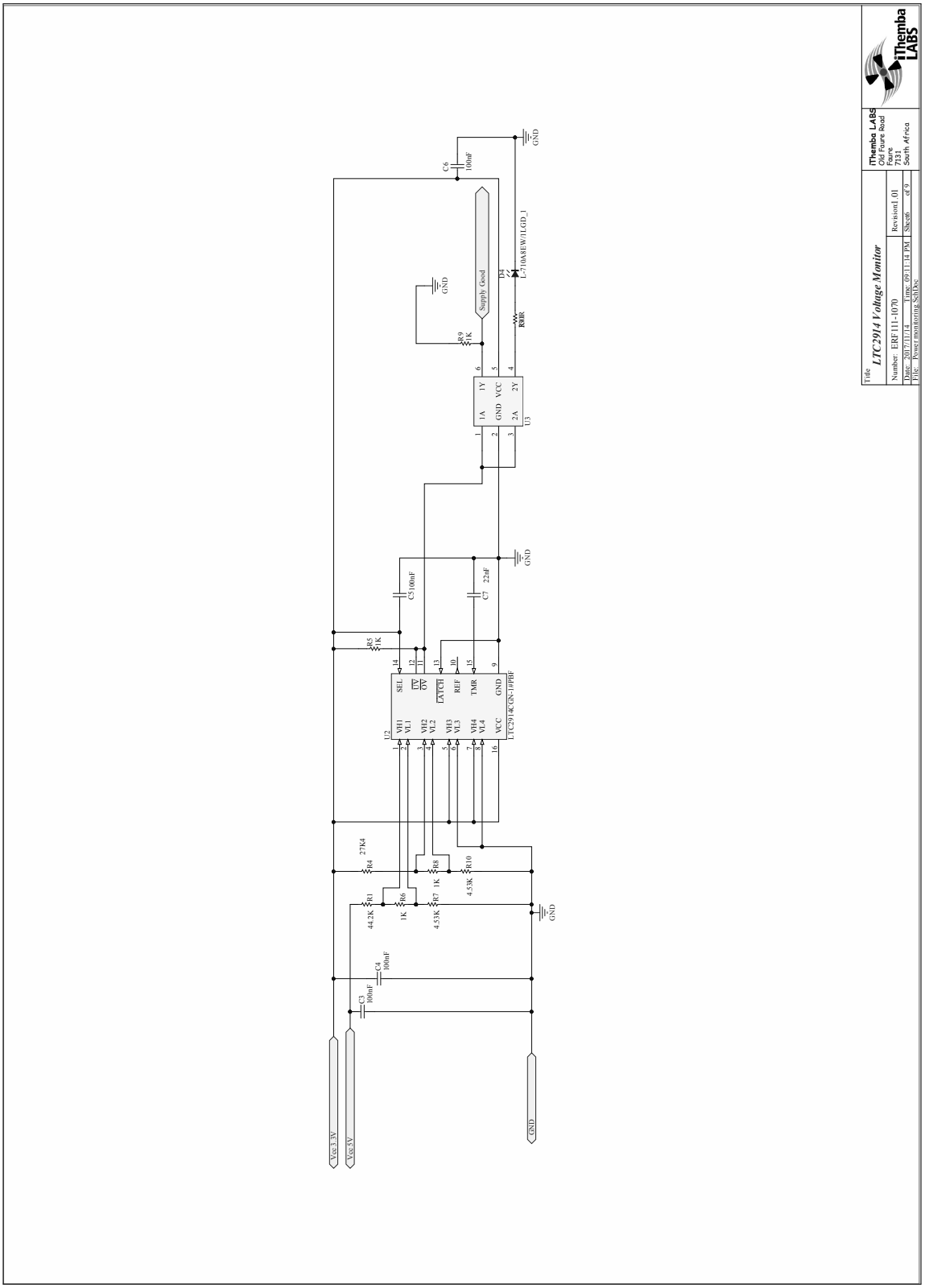
Appendix B. RF Interlocking Module Schematics

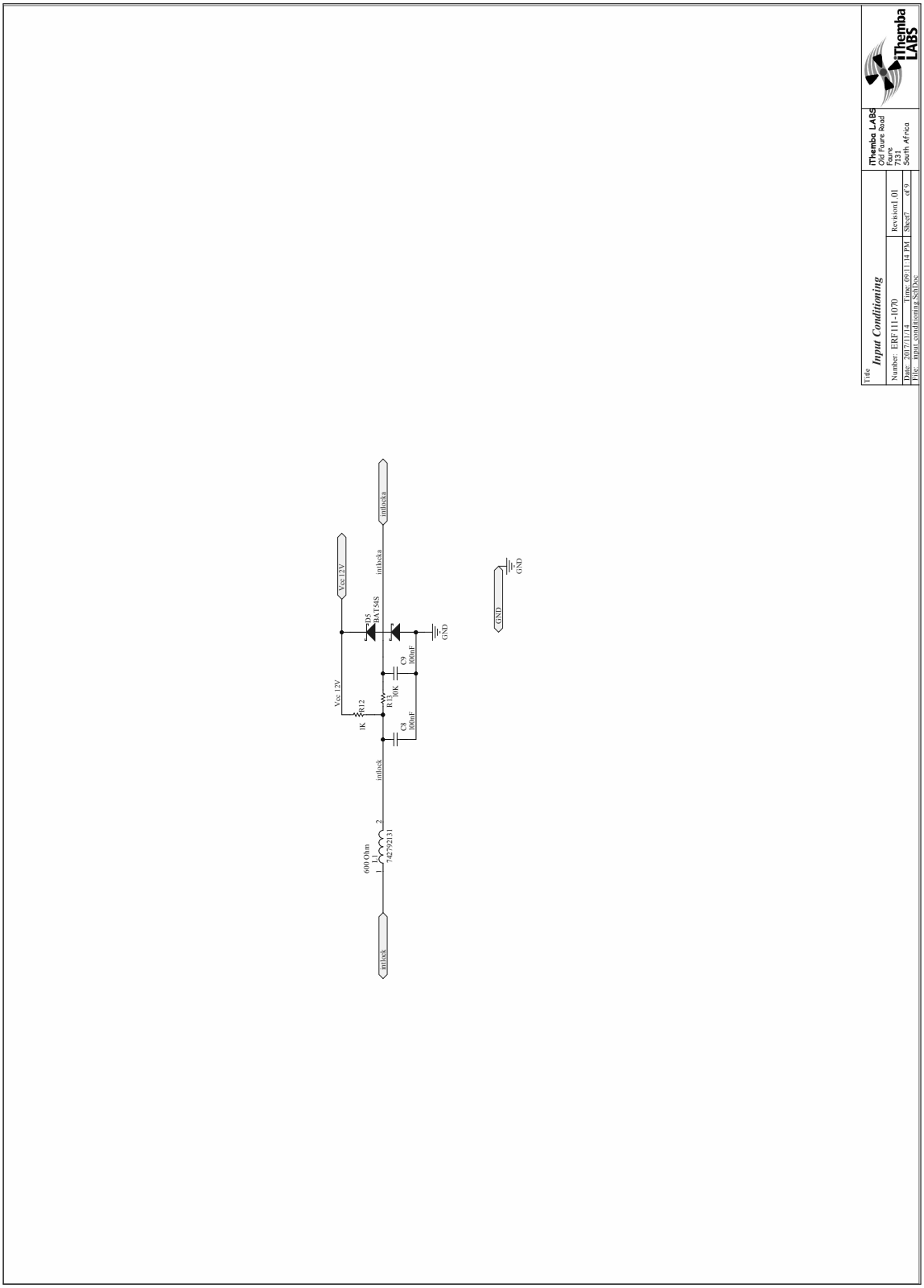


Appendix B. RF Interlocking Module Schematics

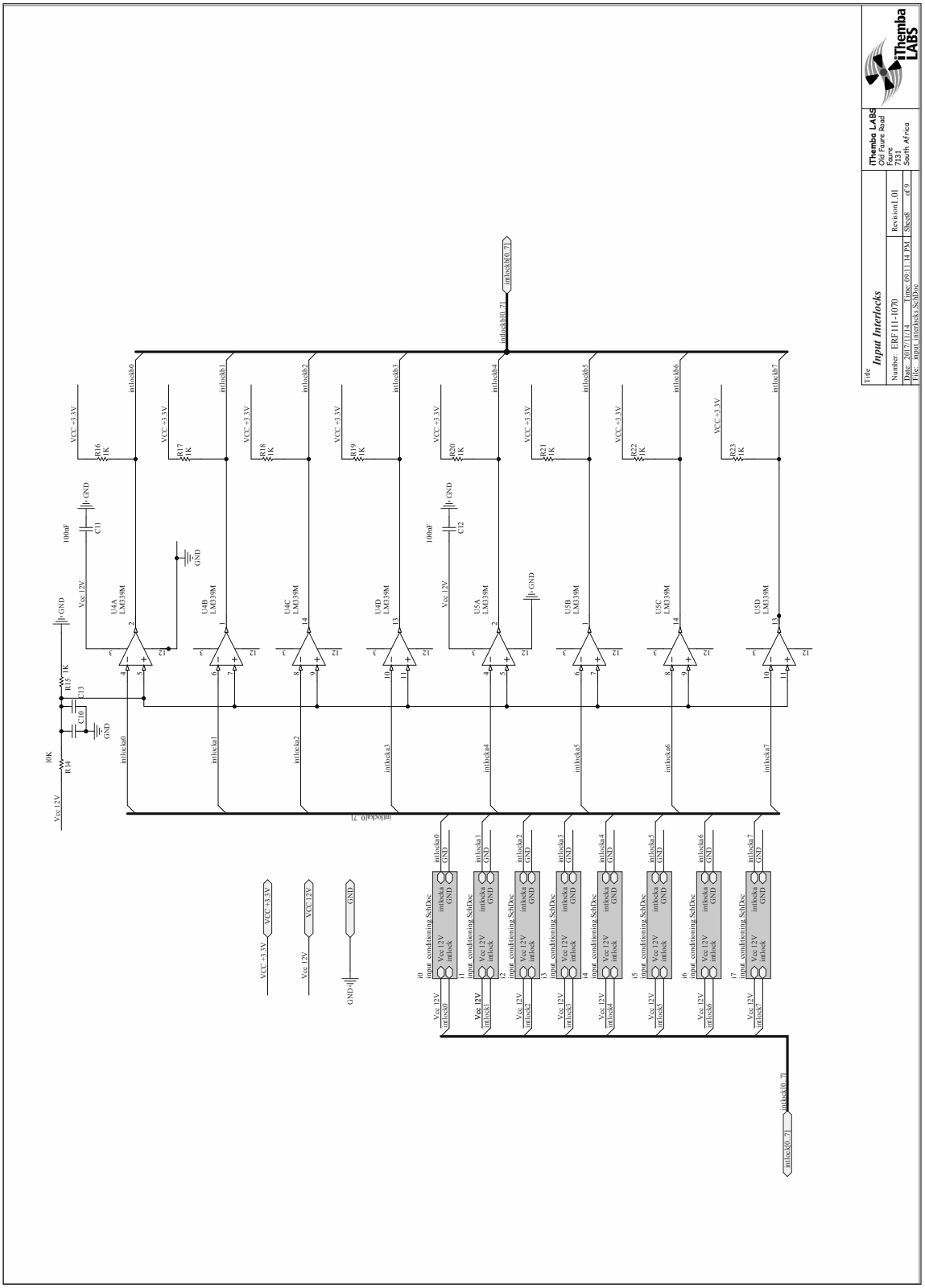


Appendix B. RF Interlocking Module Schematics

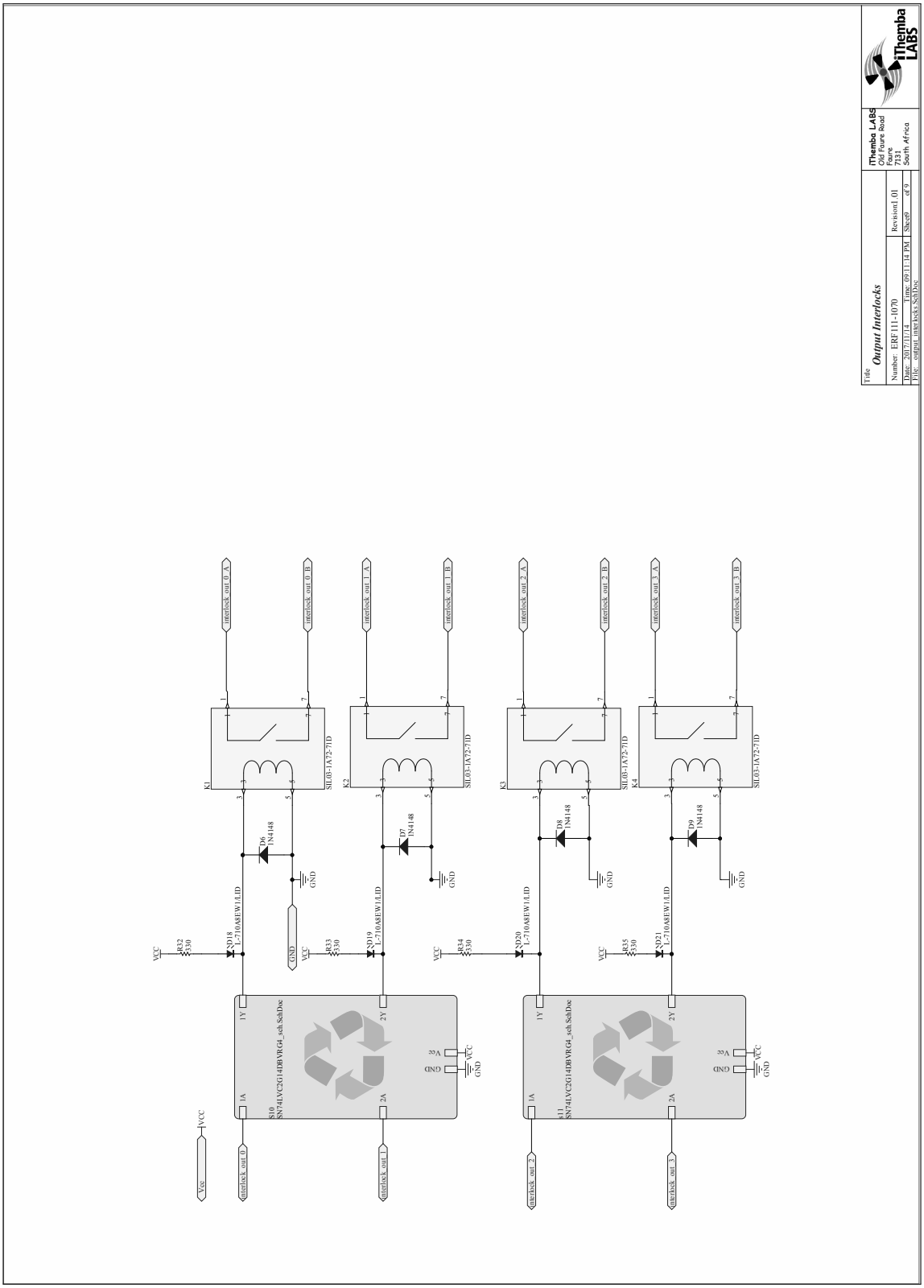




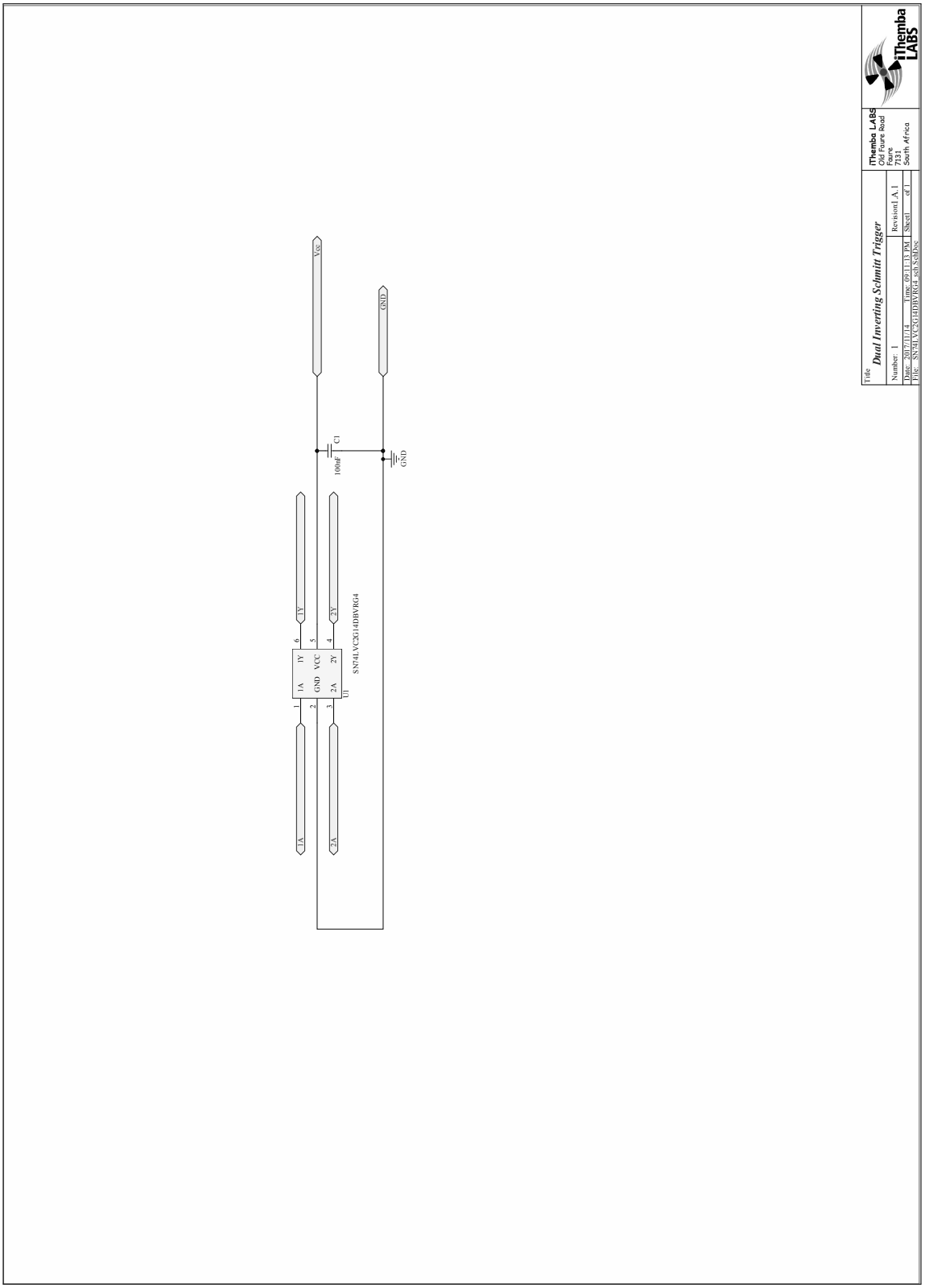
Appendix B. RF Interlocking Module Schematics



Appendix B. RF Interlocking Module Schematics



Appendix B. RF Interlocking Module Schematics



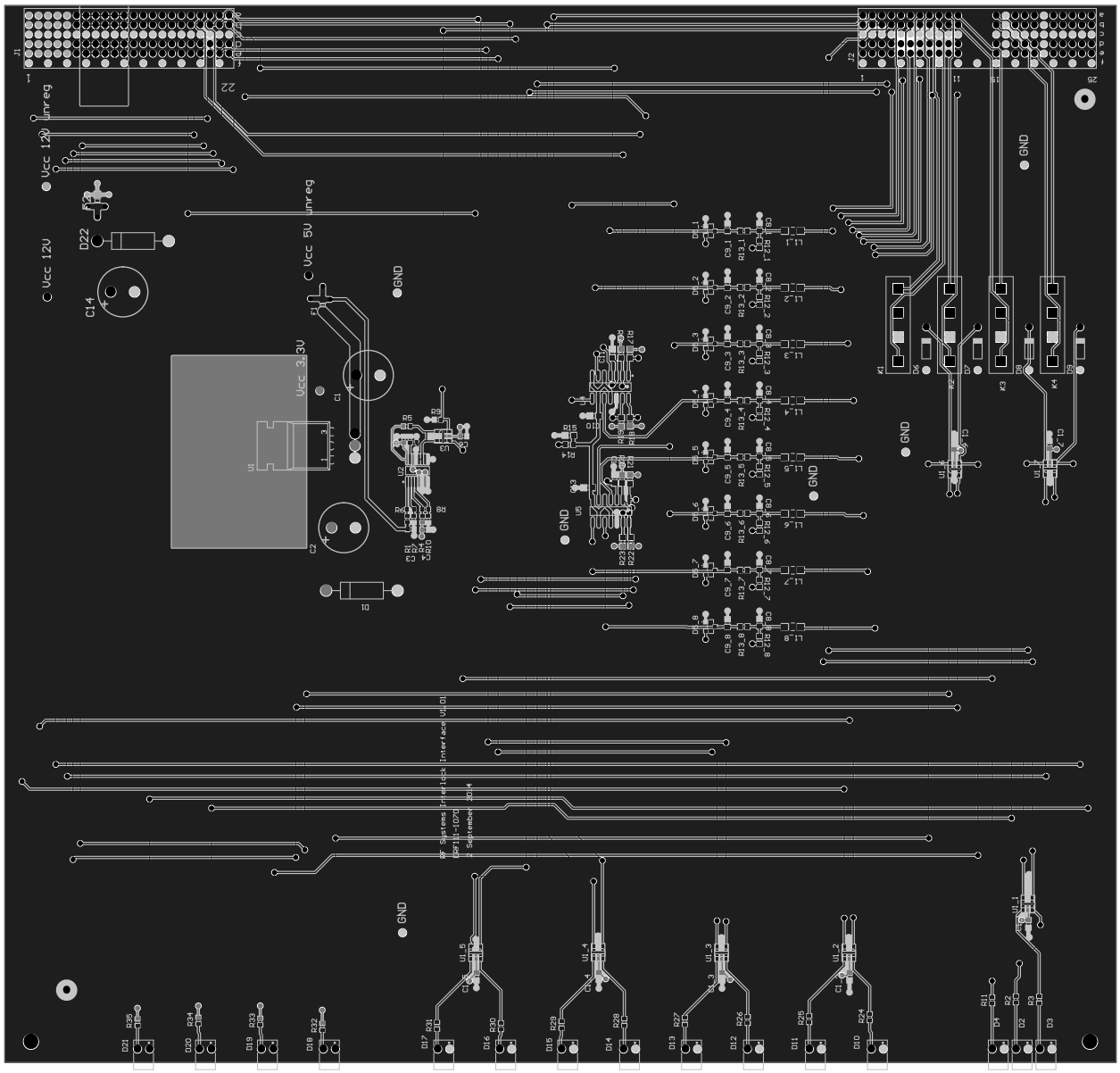
B.14 RF Interlocking BOM

Table B.5: Bill of Materials: RF Interlocking Module ERF111-1070

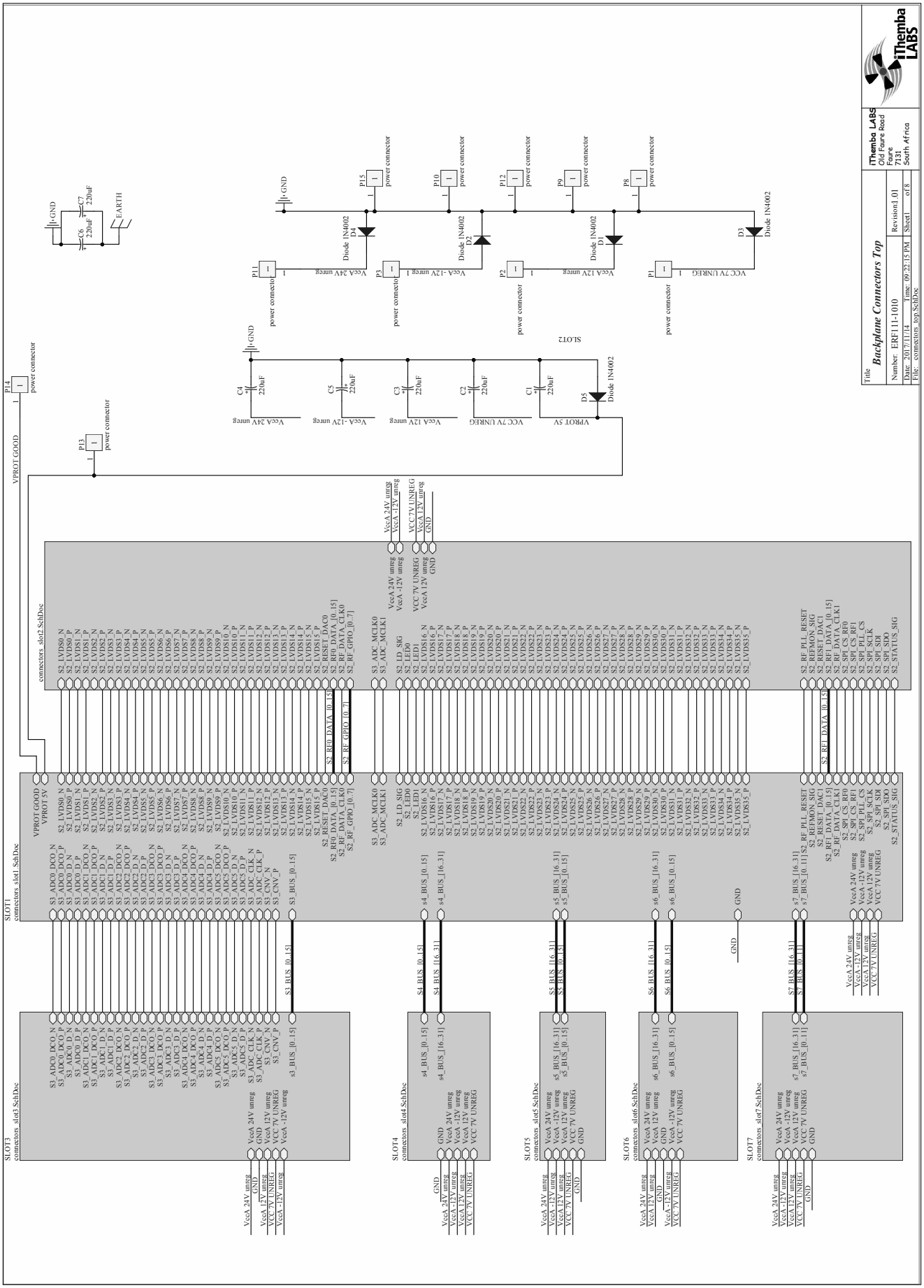
Index	Company Part No	Description	Qty	Manufacturer	Manufacturer Part No	Designator
1	ERF111-0001	4.53K 1% 0603 (1608) Surface Mounted Resistor	2	Yageo	2.3227E+11	R7, R10
2	ERF111-0002	1K Ohm 0603 Surface Mounted Resistor	21	yageo	RC0603FR-071KL	R5, R6, R8, R9, R12_1, R12_2, R12_3, R12_4, R12_5, R12_6, R12_7, R12_8, R15, R16, R17, R18, R19, R20, R21, R22, R23
3	ERF111-0004	Voltage Monitor	1	Linear Technologies	LTC2914CGN-1#PBF	U2
4	ERF111-0005	Non inverting buffer	1	Texas Instruments	SN74LVC2G34DBVR	U3
5	ERF111-0006	330 Ohm 0603 Surface Mounted Resistor	15	yageo	RC0603FR-07330RL	R2, R3, R11, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35
6	ERF111-0007	100nF 0603 Ceramic SMT Capacitor	31	Yageo	CC0603KRX7R9BB104	C1_1, C1_2, C1_3, C1_4, C1_5, C1_6, C1_7, C3, C4, C5, C6, C8_1, C8_2, C8_3, C8_4, C8_5, C8_6, C8_7, C8_8, C9_1, C9_2, C9_3, C9_4, C9_5, C9_6, C9_7, C9_8, C10, C11, C12, C13
7	ERF111-0008	22nF 0603 Ceramic SMT Capacitor	1	samsung	CL10B223KB8NNNC	C7
8	ERF111-0010	2.5A 0805 fuse	2	AVX	F0805B2R50FSTR	F1, F2
9	ERF111-0016	100uF radial Capacitor 63V	3	Panasonic	EEUFC1J101B	C1, C2, C14
10	ERF111-0019	PCB mount right angle LED 3mm RED	2	KingBright	L-710A8EW/1LID	D2, D4
11	ERF111-0021	44.2k Ohm 0603 Surface Mounted Resistor	1	Yageo	RC0603FR-0744K2L	R1
12	ERF111-0022	27.4k Ohm 0603 Surface Mounted Resistor	1	Yageo	RC0603FR-0727K4L	R4
13	ERF111-0035	Z-Pack 2mm Hard Metric Type A 110 Position Female PCB Mount Connector	1	TE CONNECTIVITY	5352068-1	J2
14	ERF111-0036	Z-Pack 2mm Hard Metric Type B 110 Position Female Daughter Card Connector	1	TE CONNECTIVITY	5352152-1	J1
15	ERF111-0045	PCB mount right angle LED GREEN	13	KingBright	L-710A8EW/1LGD	D3, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21
16	ERF111-0049	Inverting Schmitt Trigger	7	Texas Instruments	SN74LVC2G14DBVR	U1_1, U1_2, U1_3, U1_4, U1_5, U1_6, U1_7
17	ERF111-0050	Zener Diode	1	On Semiconductor	1N5334B	D1
18	ERF111-0081	3.3V Voltage regulator (DNP)	1	STMicroelectronics	LD1117V33C	U1
19	ERF111-0111	10k Ohm 0603 Surface Mounted Resistor	9	Yageo	RC0603FR-0710KL	R13_1, R13_2, R13_3, R13_4, R13_5, R13_6, R13_7, R13_8, R14
20	ERF111-0126	13V 5 Watt Surmetic 40 Zener Voltage Regulators	1	ON Semiconductor	1N5351BG	D22
21	ERF111-0127	Schottky Barrier Diode, 30 V, 2 uA, -55 to 150 degC, 3-Pin SOT23, RoHS, Tape and Reel	8	NXP	BAT54S,215	D5_1, D5_2, D5_3, D5_4, D5_5, D5_6, D5_7, D5_8
22	ERF111-0128	High-speed Diode, 100 V, 450 mA, 2-Pin SOD27, RoHS	4	Fairchild Semiconductor	1N4148XTR	D6, D7, D8, D9
23	ERF111-0129	SMD EMI Suppression Ferrite Bead WE-CBF, Z = 600 Ohm	8	Wurth Elektronik	742792131	L1_1, L1_2, L1_3, L1_4, L1_5, L1_6, L1_7, L1_8
24	ERF111-0130	Low Power Low Offset Voltage Quad Comparator, 14-pin Narrow SOIC	2	Texas Instruments	LM339M/NOPB	U4, U5
25	ERF111-0131	Meder electronic Relay SIL03-1A72-71D	4	Standex-Meder Electronics	SIL03-1A72-71D	K1, K2, K3, K4

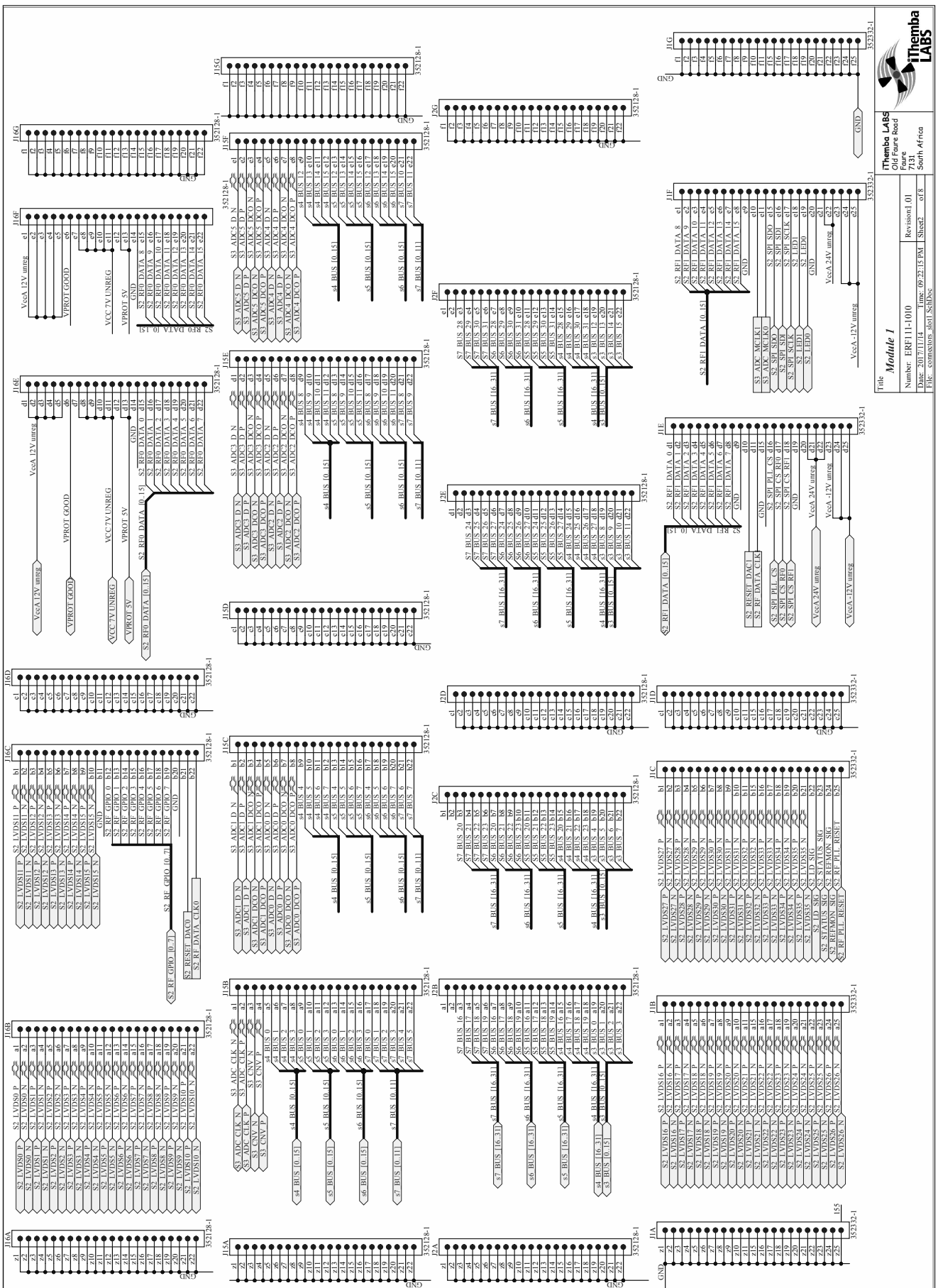
B.15 RF Interlocking Module PCB Layout

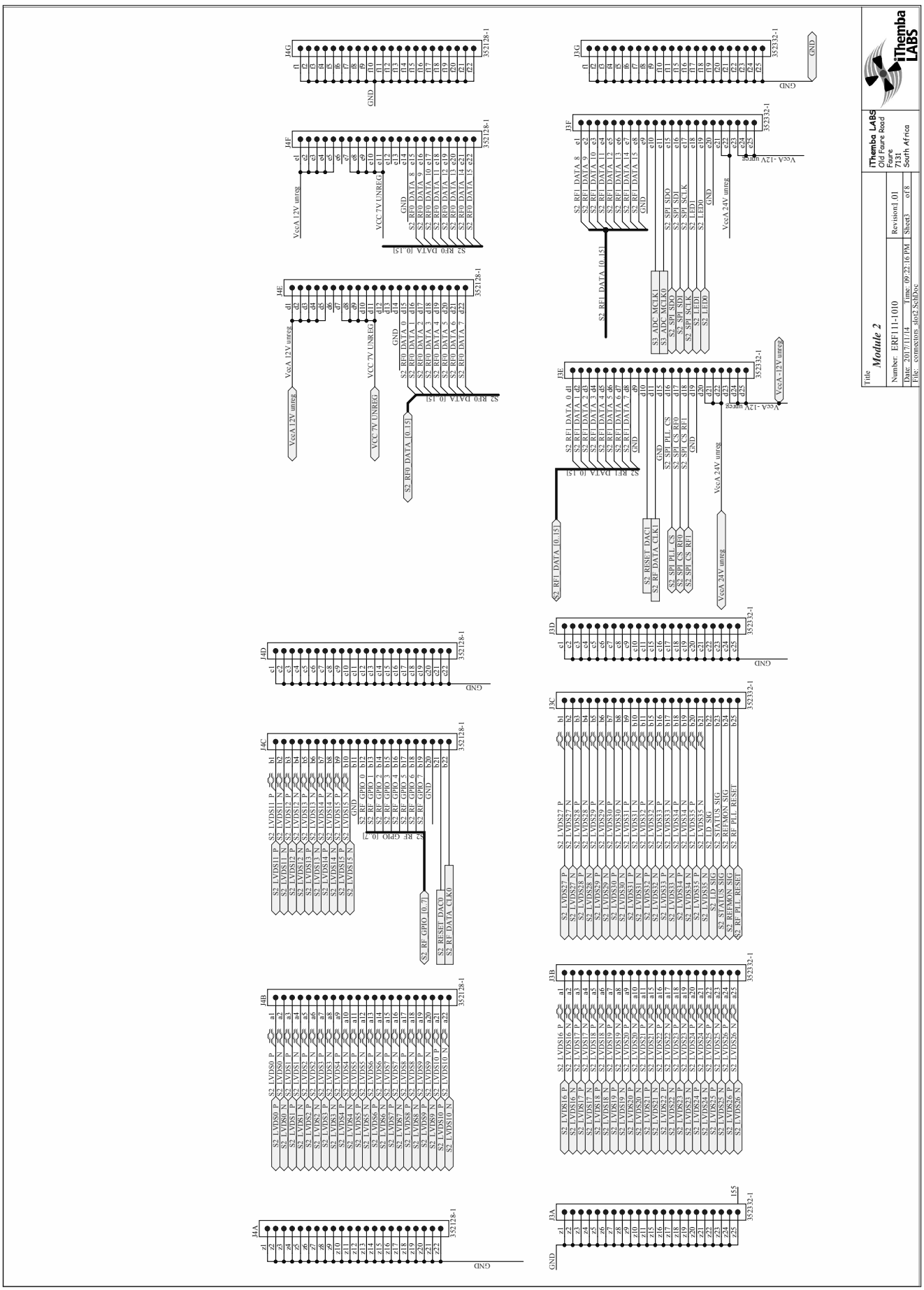
B.15.1 RF Interlocking PCB 4 Layer Composite Print

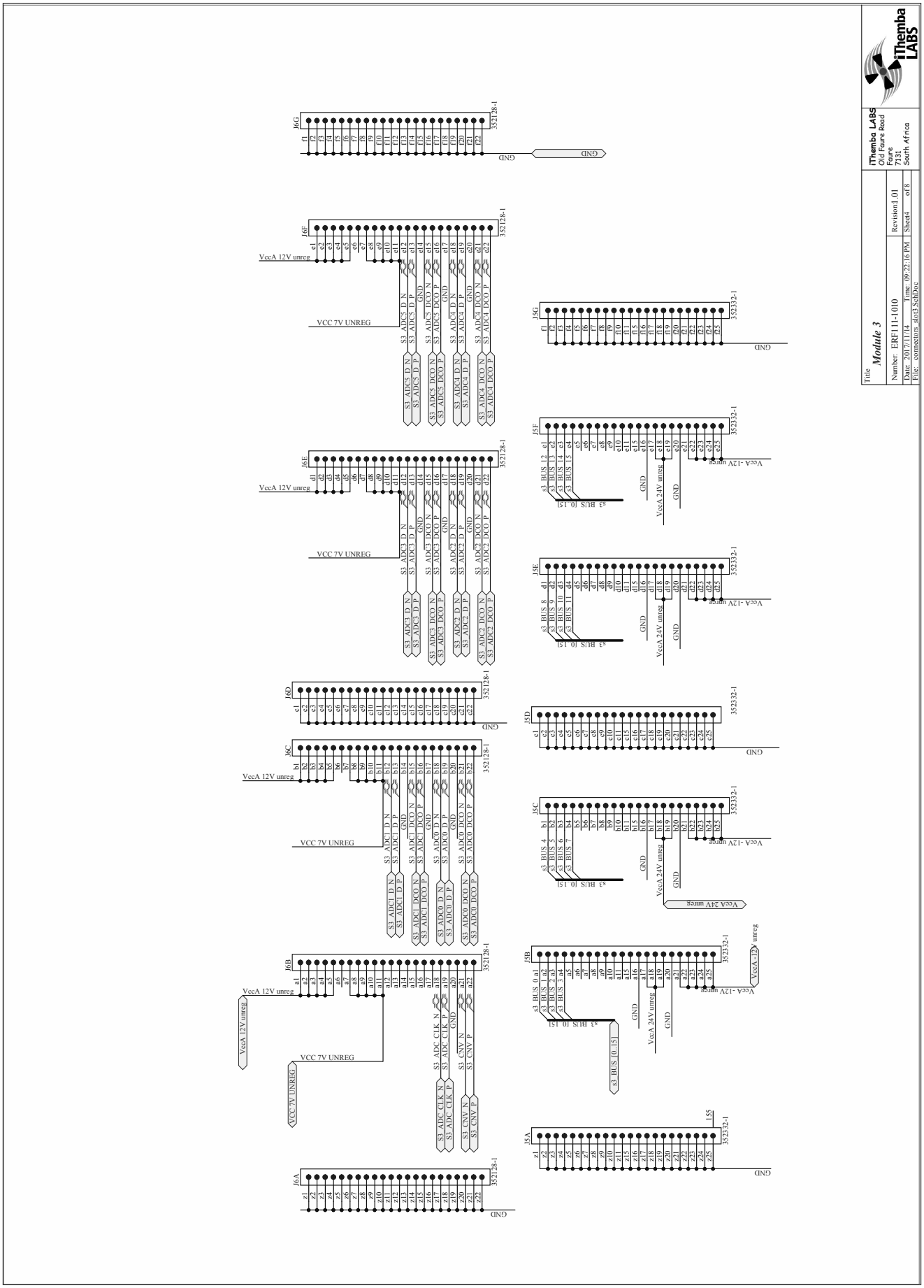


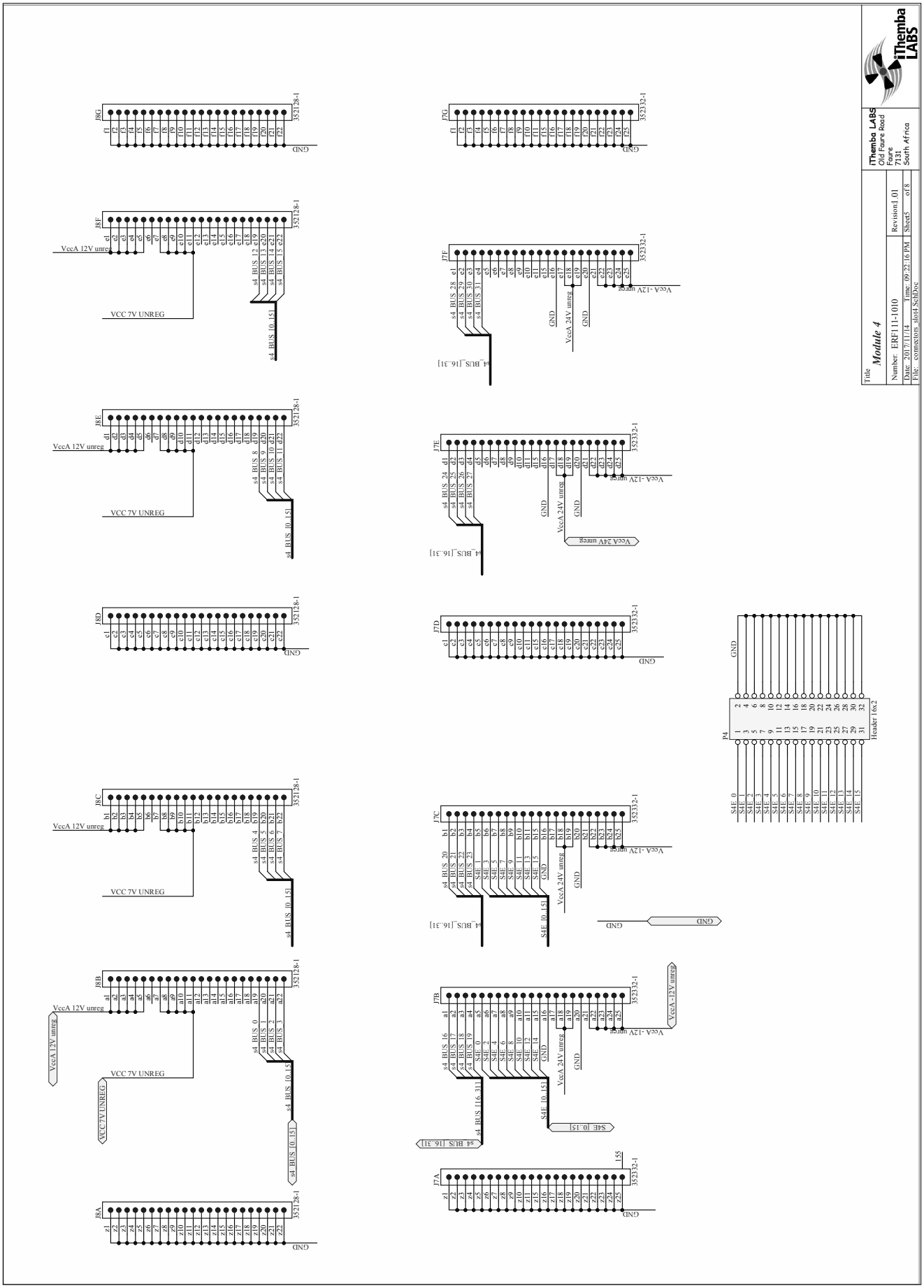
B.16 Backplane Schematics

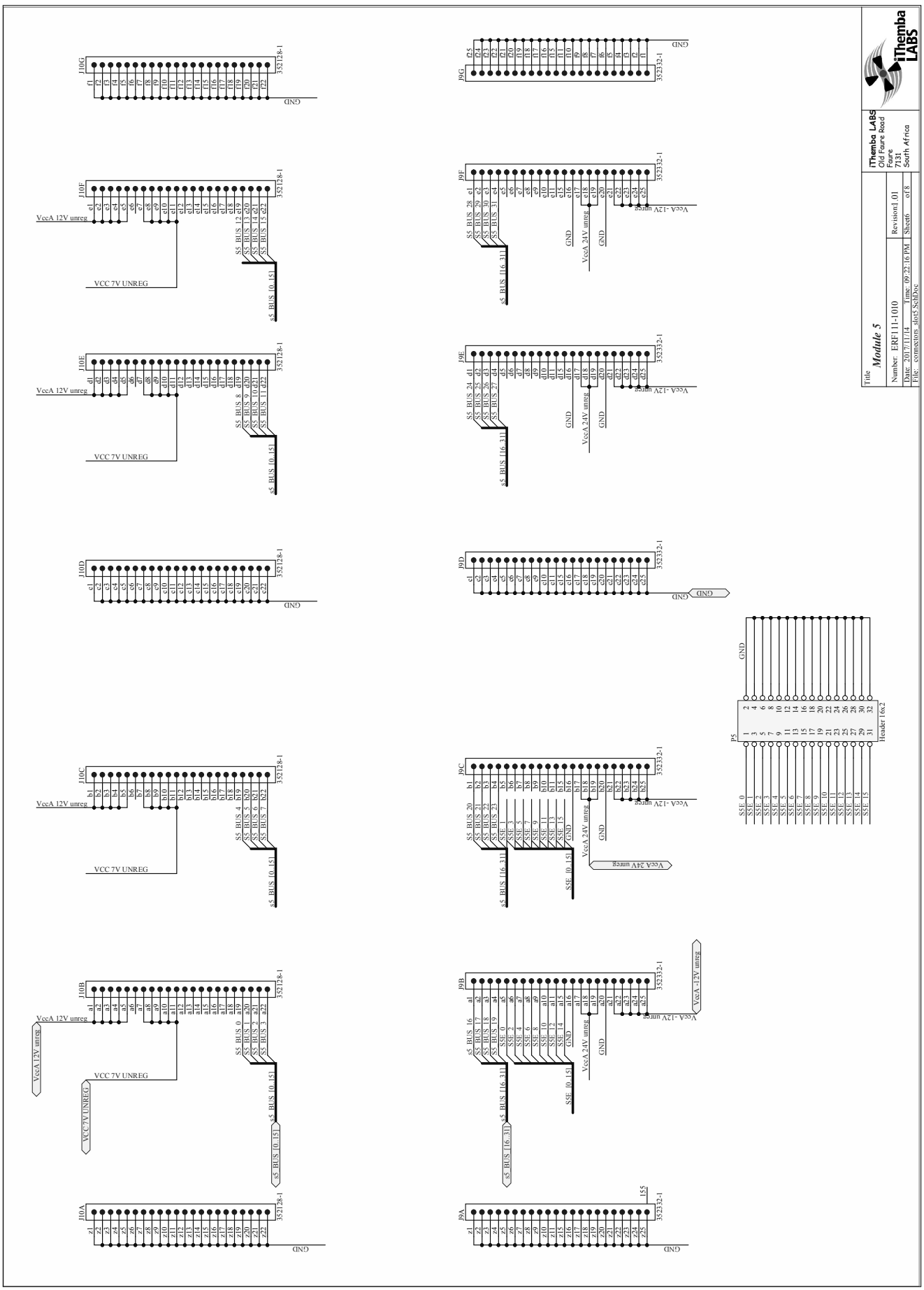


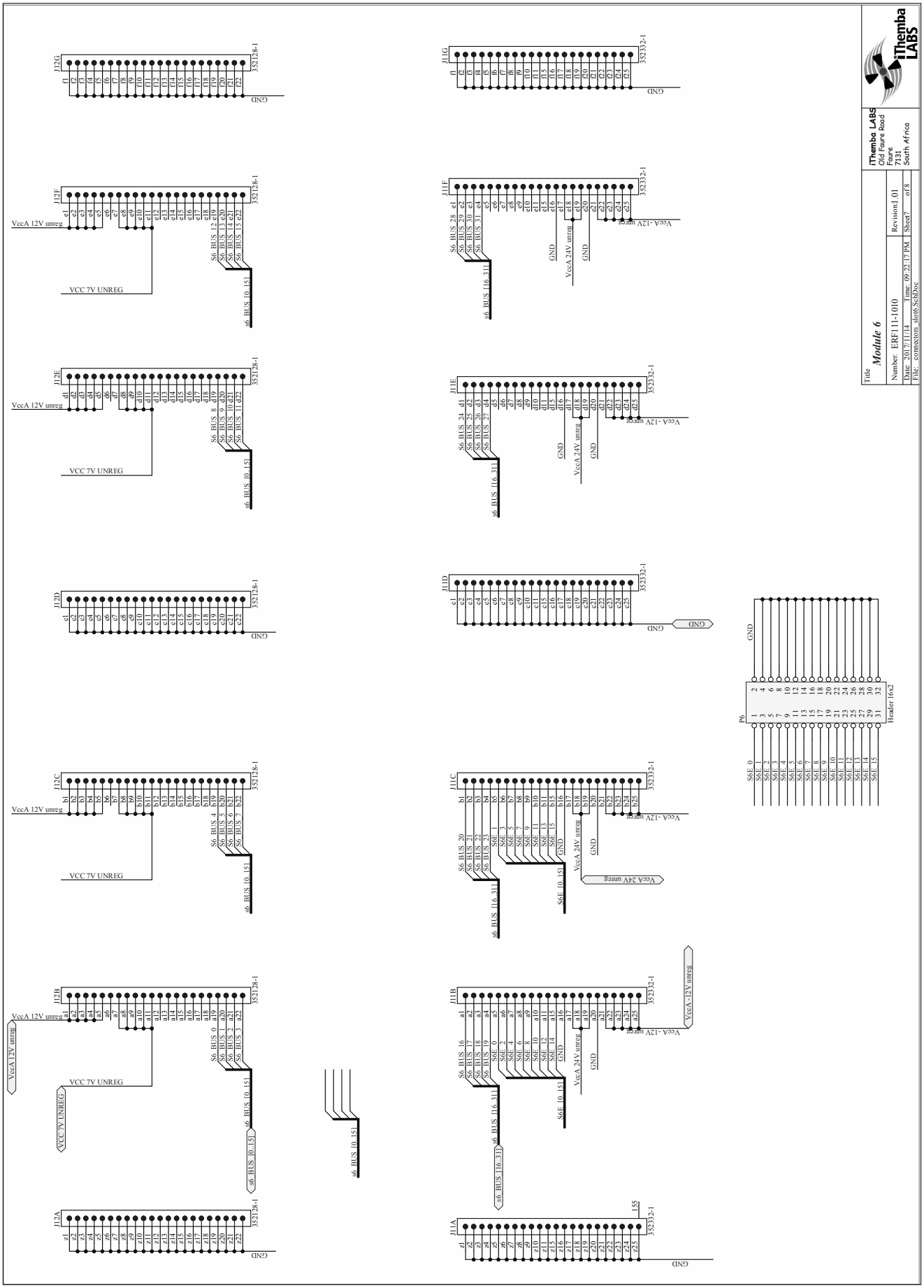


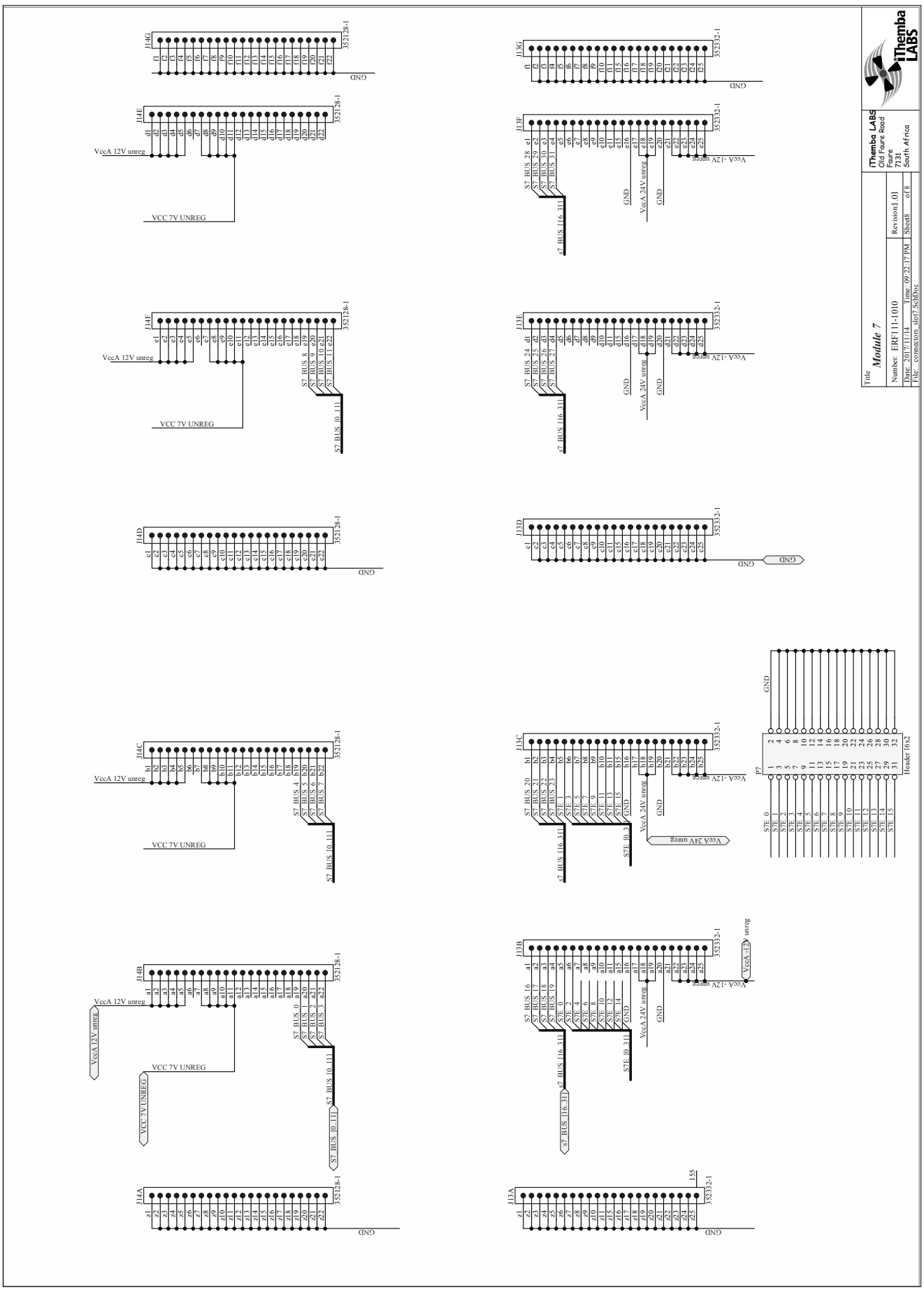












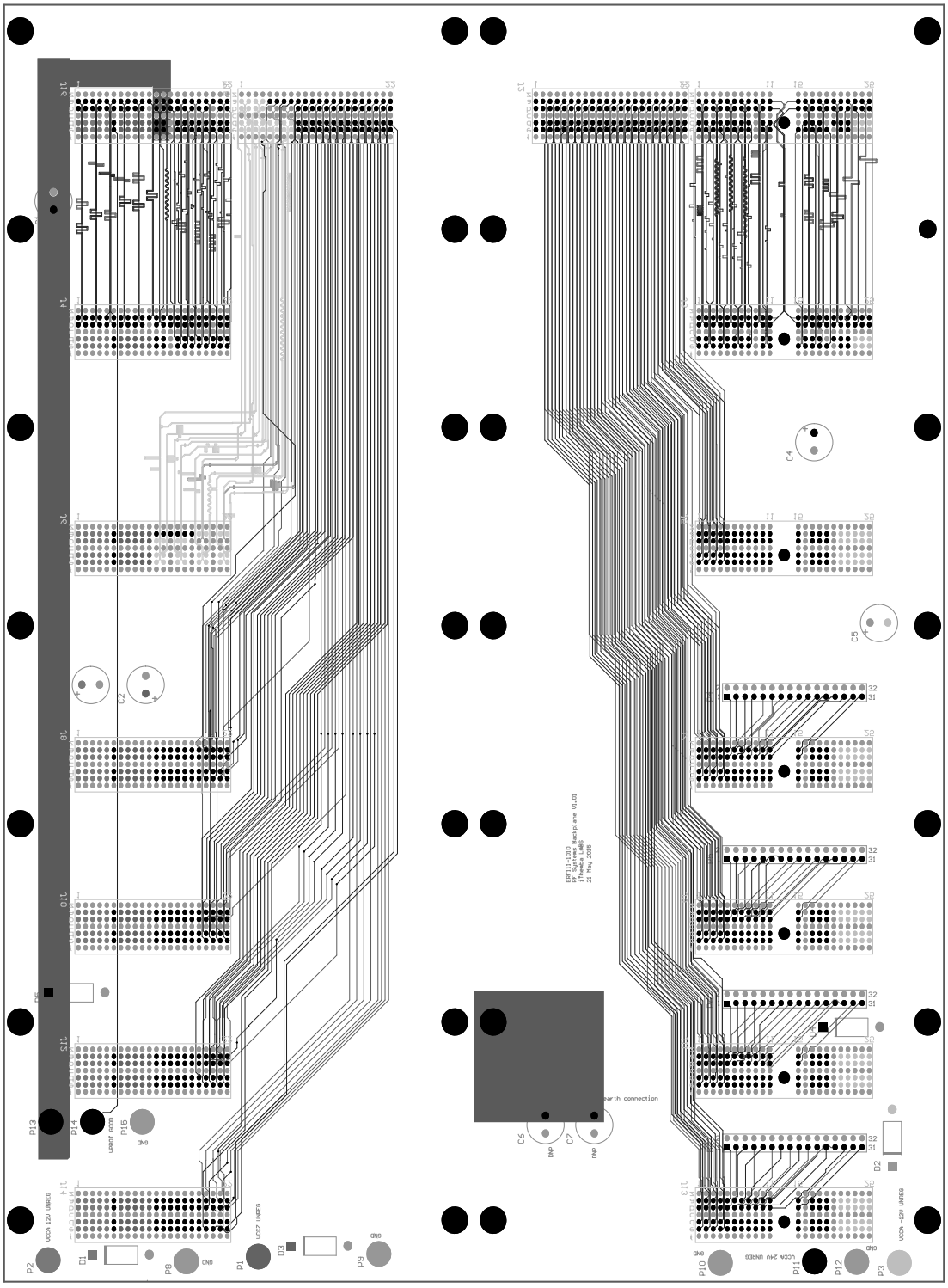
B.17 Backplane BOM

Table B.6: Bill of Materials: Backplane ERF111-1010

Index	Company Part No	Description	Qty	Manufacturer	Manufacturer Part No	Designator
1	ERF111-0011	220uF Radial Capactior	7	Panasonic	EEUFC1J221	C1, C2, C3, C4, C5, C6, C7
2	ERF111-0102	1 Amp General Purpose Rectifier Diode	5	Vishay	1N4002-E3/73	D1, D2, D3, D4, D5
3	ERF111-0122	Z-Pack 2mm Hard Metric Type A (22) 154 Position Male PCB Mount Connector	7	TE CONNECTIVITY	5188834-1	J1, J3, J5, J7, J9, J11, J13
4	ERF111-0123	Z-Pack 2mm Hard Metric Type B 154 Position Male PCB Mount Connector	9	TE CONNECTIVITY	5188835-1	J2, J4, J6, J8, J10, J12, J14, J15, J16
5	ERF111-0133	2.54mm Pitch 34 Way 2 Row Straight PCB Header, Solder Termination, 2.5A	4	Molex	70246-3401	P4, P5, P6, P7

B.18 Backplane PCB Layout

B.18.1 Backplane PCB Top Layer and Overlay L1



Appendix C

FPGA Memory Map

Table C.1: FPGA Memory Map

Byte Address	Name	Description
0	Reg16b_0	RF DDS phase increment register UINT48 [15:0]
2	Reg16b_1	RF DDS phase increment register UINT48 [31:6]
4	Reg16b_2	RF DDS phase increment register UINT48 [47:32]
6	Reg16b_3	N/A
8	Reg16b_4	N/A
10	Reg16b_5	N/A
12	Reg16b_6	N/A
14	Reg16b_7	N/A
16	Reg16b_8	N/A
18	Reg16b_9	RF kick amplitude
20	Reg16b_10	RF kick count UINT32 [15:0] (Time multiples of RF clock periods)
22	Reg16b_11	RF kick count UINT32 [31:16] (Time multiples of RF clock periods)
24	Reg16b_12	RF DDS UINT32 [15:0] configuration register
26	Reg16b_13	RF DDS UINT32 [31:16] configuration register
28	Reg16b_14	RF DDS INT16 [15:0] maximum amplitude
30	Reg16b_15	N/A
32	Reg16b_16	N/A
34	Reg16b_17	N/A
36	Reg16b_18	LO DDS phase increment register UINT48 [15:0]
38	Reg16b_19	LO DDS phase increment register UINT48 [31:6]
40	Reg16b_20	LO DDS phase increment register UINT48 [47:32]
42	Reg16b_21	N/A
44	Reg16b_22	LO DDS phase offset register UINT48[15:0]
46	Reg16b_23	LO DDS phase offset register UINT48[31:6]
48	Reg16b_24	LO DDS phase offset register UINT48[47:32]
50	Reg16b_25	N/A
52	Reg16b_26	LO DDS Amplitude INT16 [15:0]
54	Reg16b_27	N/A
56	Reg16b_28	Amplitude PID K0 IEEE 754-2008 32 bit Float [15:0]
58	Reg16b_29	Amplitude PID K0 IEEE 754-2008 32 bit Float [31:16]
60	Reg16b_30	Amplitude PID K1 IEEE 754-2008 32 bit Float [15:0]
62	Reg16b_31	Amplitude PID K1 IEEE 754-2008 32 bit Float [31:16]
64	Reg16b_32	Amplitude PID K2 IEEE 754-2008 32 bit Float [15:0]
66	Reg16b_33	Amplitude PID K2 IEEE 754-2008 32 bit Float [31:16]
68	Reg16b_34	Amplitude PID feedback scale factor IEEE 754-2008 32 bit Float [15:0]
70	Reg16b_35	Amplitude PID feedback scale factor IEEE 754-2008 32 bit Float [31:16]

Table C.1 continued: FPGA Memory Map

Byte Address	Name	Description
72	Reg16b_36	Amplitude PID set point IEEE 754-2008 32 bit Float [15:0]
74	Reg16b_37	Amplitude PID set point IEEE 754-2008 32 bit Float [31:16]
76	Reg16b_38	Amplitude PID configuration register UINT32[15:0]
78	Reg16b_39	Amplitude PID configuration register UINT32[31:16]
80	Reg16b_40	Phase PID K0 IEEE 754-2008 32 bit Float [15:0]
82	Reg16b_41	Phase PID K0 IEEE 754-2008 32 bit Float [31:16]
84	Reg16b_42	Phase PID K1 IEEE 754-2008 32 bit Float [15:0]
86	Reg16b_43	Phase PID K1 IEEE 754-2008 32 bit Float [31:16]
88	Reg16b_44	Phase PID K2 IEEE 754-2008 32 bit Float [15:0]
90	Reg16b_45	Phase PID K2 IEEE 754-2008 32 bit Float [31:16]
92	Reg16b_46	Phase PID configuration register UINT32[15:0]
94	Reg16b_47	Phase PID configuration register UINT32[31:16]
96	Reg16b_48	Phase PID set point IEEE 754-2008 32 bit Float [15:0]
98	Reg16b_49	Phase PID set point IEEE 754-2008 32 bit Float [31:16]
100	Reg16b_50	Digital step attenuators configuration register
102	Reg16b_51	Digital step attenuators status
104	Reg16b_52	N/A
106	Reg16b_53	N/A
108	Reg16b_54	N/A
110	Reg16b_55	N/A
112	Reg16b_56	N/A
114	Reg16b_57	N/A
116	Reg16b_58	N/A
118	Reg16b_59	N/A
120	Reg16b_60	ADC1 Amplitude FIFO 10MHz data rate IEEE 754-2008 32 bit Float [15:0]
122	Reg16b_61	ADC1 Amplitude FIFO 10MHz data rate IEEE 754-2008 32 bit Float [31:16]
124	Reg16b_62	ADC1 Phase FIFO 10MHz data rate IEEE 754-2008 32 bit Float [15:0]
126	Reg16b_63	ADC1 Phase FIFO 10MHz data rate IEEE 754-2008 32 bit Float [31:16]
128	Reg16b_64	ADC2 Amplitude FIFO 10MHz data rate IEEE 754-2008 32 bit Float [15:0]
130	Reg16b_65	ADC2 Amplitude FIFO 10MHz data rate IEEE 754-2008 32 bit Float [31:16]
132	Reg16b_66	ADC2 Phase FIFO 10MHz data rate IEEE 754-2008 32 bit Float [15:0]
134	Reg16b_67	ADC2 Phase FIFO 10MHz data rate IEEE 754-2008 32 bit Float [31:16]
136	Reg16b_68	N/A
138	Reg16b_69	N/A
140	Reg16b_70	N/A
142	Reg16b_71	N/A
144	Reg16b_72	N/A
146	Reg16b_73	N/A
148	Reg16b_74	N/A
150	Reg16b_75	N/A
152	Reg16b_76	N/A
154	Reg16b_77	N/A
156	Reg16b_78	N/A
158	Reg16b_79	N/A
160	Reg16b_80	Auto-tune phase data rate re-sampling divider register [13:0]
162	Reg16b_81	Auto-tune re-sampled phase data FIFO IEEE 754-2008 32 bit Float [15:0]
164	Reg16b_82	Auto-tune re sampled phase data FIFO IEEE 754-2008 32 bit Float [31:16]
166	Reg16b_83	N/A
168	Reg16b_84	N/A
170	Reg16b_85	N/A
172	Reg16b_86	N/A
174	Reg16b_87	N/A
176	Reg16b_88	N/A
178	Reg16b_89	ADC1 offset INT16 [15:0]
180	Reg16b_90	ADC2 offset INT16 [15:0]
182	Reg16b_91	ADC3 offset INT16 [15:0]

Table C.1 continued: FPGA Memory Map

Byte Address	Name	Description
184	Reg16b_92	ADC4 offset INT16 [15:0]
186	Reg16b_93	ADC5 offset INT16 [15:0]
188	Reg16b_94	FIFO buffers programmed full interrupt UINT32[15:0]
190	Reg16b_95	FIFO buffers programmed full interrupt UINT32[31:16]
192	Reg16b_96	ADC1 Amplitude FIFO 2.5 kHz data rate IEEE 754-2008 32 bit Float [15:0]
194	Reg16b_97	ADC1 Amplitude FIFO 2.5 kHz data rate IEEE 754-2008 32 bit Float [31:16]
196	Reg16b_98	ADC2 Amplitude FIFO 2.5 kHz data rate IEEE 754-2008 32 bit Float [15:0]
198	Reg16b_99	ADC2 Amplitude FIFO 2.5 kHz data rate IEEE 754-2008 32 bit Float [31:16]
200	Reg16b_100	ADC3 Amplitude FIFO 2.5 kHz data rate IEEE 754-2008 32 bit Float [15:0]
202	Reg16b_101	ADC3 Amplitude FIFO 2.5 kHz data rate IEEE 754-2008 32 bit Float [31:16]
204	Reg16b_102	ADC4 Amplitude FIFO 2.5 kHz data rate IEEE 754-2008 32 bit Float [15:0]
206	Reg16b_103	ADC4 Amplitude FIFO 2.5 kHz data rate IEEE 754-2008 32 bit Float [31:16]
208	Reg16b_104	ADC5 Amplitude FIFO 2.5 kHz data rate IEEE 754-2008 32 bit Float [15:0]
210	Reg16b_105	ADC5 Amplitude FIFO 2.5 kHz data rate IEEE 754-2008 32 bit Float [31:16]
212	Reg16b_106	ADC1 Phase FIFO 2.5 kHz data rate IEEE 754-2008 32 bit Float [15:0]
214	Reg16b_107	ADC1 Phase FIFO 2.5 kHz data rate IEEE 754-2008 32 bit Float [31:16]
216	Reg16b_108	ADC2 Phase FIFO 2.5 kHz data rate IEEE 754-2008 32 bit Float [15:0]
218	Reg16b_109	ADC2 Phase FIFO 2.5 kHz data rate IEEE 754-2008 32 bit Float [31:16]
220	Reg16b_110	ADC3 Phase FIFO 2.5 kHz data rate IEEE 754-2008 32 bit Float [15:0]
222	Reg16b_111	ADC3 Phase FIFO 2.5 kHz data rate IEEE 754-2008 32 bit Float [31:16]
224	Reg16b_112	ADC4 Phase FIFO 2.5 kHz data rate IEEE 754-2008 32 bit Float [15:0]
226	Reg16b_113	ADC4 Phase FIFO 2.5 kHz data rate IEEE 754-2008 32 bit Float [31:16]
228	Reg16b_114	ADC5 Phase FIFO 2.5 kHz data rate IEEE 754-2008 32 bit Float [15:0]
230	Reg16b_115	ADC5 Phase FIFO 2.5 kHz data rate IEEE 754-2008 32 bit Float [31:16]
232	Reg16b_116	N/A
234	Reg16b_117	ADC1 Raw Data 10MHz data rate IEEE 754-2008 32 bit Float [15:0]
236	Reg16b_118	ADC2 Raw Data 10MHz data rate IEEE 754-2008 32 bit Float [15:0]
238	Reg16b_119	ADC3 Raw Data 10MHz data rate IEEE 754-2008 32 bit Float [15:0]
240	Reg16b_120	ADC4 Raw Data 10MHz data rate IEEE 754-2008 32 bit Float [15:0]
242	Reg16b_121	ADC5 Raw Data 10MHz data rate IEEE 754-2008 32 bit Float [15:0]
244	Reg16b_122	Raw ADC data FIFO programmed full interrupt [4:0]
246	Reg16b_123	N/A
248	Reg16b_124	FPGA soft reset [0]
250	Reg16b_125	SPI multiplexer address bits[4:0]
252	Reg16b_126	RF ICs reset, bit[0]= PLL, bit [1] =DAC0, bit [2]=DAC1
254	Reg16b_127	N/A
256	Reg16b_128	Ch1 of 5Ch I/Q demodulator Cosine LUT value 0 INT16[15:0]
258	Reg16b_129	Ch1 of 5Ch I/Q demodulator Cosine LUT value 1 INT16[15:0]
260	Reg16b_130	Ch1 of 5Ch I/Q demodulator Cosine LUT value 2 INT16[15:0]
262	Reg16b_131	Ch1 of 5Ch I/Q demodulator Cosine LUT value 3 INT16[15:0]
264	Reg16b_132	Ch1 of 5Ch I/Q demodulator Cosine LUT value 4 INT16[15:0]
266	Reg16b_133	Ch1 of 5Ch I/Q demodulator Sine LUT value 0 INT16[15:0]
268	Reg16b_134	Ch1 of 5Ch I/Q demodulator Sine LUT value 1 INT16[15:0]
270	Reg16b_135	Ch1 of 5Ch I/Q demodulator Sine LUT value 2 INT16[15:0]
272	Reg16b_136	Ch1 of 5Ch I/Q demodulator Sine LUT value 3 INT16[15:0]
274	Reg16b_137	Ch1 of 5Ch I/Q demodulator Sine LUT value 4 INT16[15:0]
276	Reg16b_138	Ch2 of 5Ch I/Q demodulator Cosine LUT value 0 INT16[15:0]
278	Reg16b_139	Ch2 of 5Ch I/Q demodulator Cosine LUT value 1 INT16[15:0]
280	Reg16b_140	Ch2 of 5Ch I/Q demodulator Cosine LUT value 2 INT16[15:0]
282	Reg16b_141	Ch2 of 5Ch I/Q demodulator Cosine LUT value 3 INT16[15:0]
284	Reg16b_142	Ch2 of 5Ch I/Q demodulator Cosine LUT value 4 INT16[15:0]
286	Reg16b_143	Ch2 of 5Ch I/Q demodulator Sine LUT value 0 INT16[15:0]
288	Reg16b_144	Ch2 of 5Ch I/Q demodulator Sine LUT value 1 INT16[15:0]
290	Reg16b_145	Ch2 of 5Ch I/Q demodulator Sine LUT value 2 INT16[15:0]
292	Reg16b_146	Ch2 of 5Ch I/Q demodulator Sine LUT value 3 INT16[15:0]
294	Reg16b_147	Ch2 of 5Ch I/Q demodulator Sine LUT value 4 INT16[15:0]
296	Reg16b_148	Ch3 of 5Ch I/Q demodulator Cosine LUT value 0 INT16[15:0]

Table C.1 continued: FPGA Memory Map

Byte Address	Name	Description
298	Reg16b_149	Ch3 of 5Ch I/Q demodulator Cosine LUT value 1 INT16[15:0]
300	Reg16b_150	Ch3 of 5Ch I/Q demodulator Cosine LUT value 2 INT16[15:0]
302	Reg16b_151	Ch3 of 5Ch I/Q demodulator Cosine LUT value 3 INT16[15:0]
304	Reg16b_152	Ch3 of 5Ch I/Q demodulator Cosine LUT value 4 INT16[15:0]
306	Reg16b_153	Ch3 of 5Ch I/Q demodulator Sine LUT value 0 INT16[15:0]
308	Reg16b_154	Ch3 of 5Ch I/Q demodulator Sine LUT value 1 INT16[15:0]
310	Reg16b_155	Ch3 of 5Ch I/Q demodulator Sine LUT value 2 INT16[15:0]
312	Reg16b_156	Ch3 of 5Ch I/Q demodulator Sine LUT value 3 INT16[15:0]
314	Reg16b_157	Ch3 of 5Ch I/Q demodulator Sine LUT value 4 INT16[15:0]
316	Reg16b_158	Ch4 of 5Ch I/Q demodulator Cosine LUT value 0 INT16[15:0]
318	Reg16b_159	Ch4 of 5Ch I/Q demodulator Cosine LUT value 1 INT16[15:0]
320	Reg16b_160	Ch4 of 5Ch I/Q demodulator Cosine LUT value 2 INT16[15:0]
322	Reg16b_161	Ch4 of 5Ch I/Q demodulator Cosine LUT value 3 INT16[15:0]
324	Reg16b_162	Ch4 of 5Ch I/Q demodulator Cosine LUT value 4 INT16[15:0]
326	Reg16b_163	Ch4 of 5Ch I/Q demodulator Sine LUT value 0 INT16[15:0]
328	Reg16b_164	Ch4 of 5Ch I/Q demodulator Sine LUT value 1 INT16[15:0]
330	Reg16b_165	Ch4 of 5Ch I/Q demodulator Sine LUT value 2 INT16[15:0]
332	Reg16b_166	Ch4 of 5Ch I/Q demodulator Sine LUT value 3 INT16[15:0]
334	Reg16b_167	Ch4 of 5Ch I/Q demodulator Sine LUT value 4 INT16[15:0]
336	Reg16b_168	Ch5 of 5Ch I/Q demodulator Cosine LUT value 0 INT16[15:0]
338	Reg16b_169	Ch5 of 5Ch I/Q demodulator Cosine LUT value 1 INT16[15:0]
340	Reg16b_170	Ch5 of 5Ch I/Q demodulator Cosine LUT value 2 INT16[15:0]
342	Reg16b_171	Ch5 of 5Ch I/Q demodulator Cosine LUT value 3 INT16[15:0]
344	Reg16b_172	Ch5 of 5Ch I/Q demodulator Cosine LUT value 4 INT16[15:0]
346	Reg16b_173	Ch5 of 5Ch I/Q demodulator Sine LUT value 0 INT16[15:0]
348	Reg16b_174	Ch5 of 5Ch I/Q demodulator Sine LUT value 1 INT16[15:0]
350	Reg16b_175	Ch5 of 5Ch I/Q demodulator Sine LUT value 2 INT16[15:0]
352	Reg16b_176	Ch5 of 5Ch I/Q demodulator Sine LUT value 3 INT16[15:0]
354	Reg16b_177	Ch5 of 5Ch I/Q demodulator Sine LUT value 4 INT16[15:0]
356	Reg16b_178	N/A
358	Reg16b_179	N/A
360	Reg16b_180	Amplitude Output FIFO 10MHz data rate IEEE 754-2008 32 bit Float [15:0]
362	Reg16b_181	Amplitude Output FIFO 10MHz data rate IEEE 754-2008 32 bit Float [31:16]
364	Reg16b_182	Phase Output FIFO 10MHz data rate IEEE 754-2008 32 bit Float [15:0]
366	Reg16b_183	Phase Output FIFO 10MHz data rate IEEE 754-2008 32 bit Float [31:16]
368	Reg16b_184	N/A
370	Reg16b_185	N/A
372	Reg16b_186	N/A
374	Reg16b_187	N/A
376	Reg16b_188	N/A
378	Reg16b_189	N/A
380	Reg16b_190	Latched interlock register UINT16 [15:0]
382	Reg16b_191	Instantaneous interlock register UINT16 [15:0]
384	Reg16b_192	Interlock module configuration register UINT16 [15:0]
386	Reg16b_193	Output interlocks configuration register UINT16 [15:0]
388	Reg16b_194	Interlock disable mask UINT16 [15:0]
390	Reg16b_195	RF trip detection minimum level INT16 [15:0]
392	Reg16b_196	RF trip detection configuration register UINT16 [15:0]
394	Reg16b_197	N/A
396	Reg16b_198	N/A
398	Reg16b_199	RF trip detection low cycle time, 100ns multiples UINT32 [15:0]
400	Reg16b_200	RF trip detection low cycle time, 100ns multiples UINT32 [31:16]
402	Reg16b_201	N/A
404	Reg16b_202	N/A
406	Reg16b_203	N/A
408	Reg16b_204	Front panel LEDs UINT16 [15:0]
410	Reg16b_205	Module 5,4,3&2 power ok [3:0]

Appendix D

DDS VHDL Implementation

D.1 DDS

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
library UNISIM;
use UNISIM.Vcomponents.ALL;

entity DDS is
Generic (N : integer :=48);
    Port (
    module_clock : in  STD_LOGIC;
    data_clock : in  STD_LOGIC;
    reset : in std_logic;
    phase_inc : in  STD_LOGIC_VECTOR (N-1 downto 0);
    phase_offset : in std_logic_vector(N-1 downto 0);
    sin : out std_logic_vector(15 downto 0);
    gain : in std_logic_vector(15 downto 0)
        );
end DDS;

architecture Behavioral of DDS is

component mult2
    port (
    clk: IN std_logic;
    a: IN std_logic_VECTOR(17 downto 0);
    b: IN std_logic_VECTOR(15 downto 0);
    ce: IN std_logic;
    p: OUT std_logic_VECTOR(15 downto 0));
end component;

component sin_cos_lut
    port (
    phase_in: IN std_logic_VECTOR(31 downto 0);
    y_out: OUT std_logic_VECTOR(17 downto 0);
    clk: IN std_logic;
    ce: IN std_logic);
end component;

component mult
    port (
    clk: IN std_logic;
    a: IN std_logic_VECTOR(47 downto 0);
    b: IN std_logic_VECTOR(47 downto 0);
    ce: IN std_logic;
    p: OUT std_logic_VECTOR(47 downto 0));
```

```
end component;

component phase_accumulator
    port(
    phase_inc : IN std_logic_vector(47 downto 0);
    reset : IN std_logic;
    clk : IN std_logic;
    accum : OUT std_logic_vector(47 downto 0)
    );
end component;

signal ce:std_logic;
signal accum_output: std_logic_vector(N-1 downto 0);
signal accum_input: std_logic_vector(N-1 downto 0);
signal accum1: std_logic_vector(N-1 downto 0);
signal accum2: std_logic_vector(N-1 downto 0);
signal accum0: std_logic_vector(N-1 downto 0);
signal accum_c_input: std_logic_vector(N-1 downto 0);
signal accum_opmode: std_logic_vector(6 downto 0);
signal sub0: std_logic_vector(N-1 downto 0);
signal adv0: std_logic_vector(N-1 downto 0);
signal sub1: std_logic_vector(N-1 downto 0);
signal sin_sig: std_logic_vector(15 downto 0);
signal sin_sig0: std_logic_vector(17 downto 0);
signal sin_sig1: std_logic_vector(17 downto 0);
attribute KEEP : string;
attribute KEEP of sin_sig0 : signal is "TRUE";
signal cordic_phase_out: std_logic_vector(47 downto 0);
signal cos_sig: std_logic_vector(47 downto 0);
--signal scaler: std_logic_vector(47 downto 0):=x"B424DC35095E";-- 100MHz
signal scaler: std_logic_vector(47 downto 0):=x"961EB78187CD";  --120MHz
signal phase_inc_reg: std_logic_vector(N-1 downto 0);
signal gndbus: std_logic_vector(47 downto 0):=(others=>'0');
signal too_large :std_logic;
signal load :std_logic;
signal phase_offset_reg: std_logic_vector(N-1 downto 0);
signal phase_in: std_logic_vector(47 downto 0);
signal phase_in_corrected: std_logic_vector(47 downto 0);
signal phase_in_2qn: std_logic_vector(47 downto 0);
signal sin_out: std_logic_vector(15 downto 0);
signal sin_out1: std_logic_vector(16 downto 0);
signal sin_out2: std_logic_vector(16 downto 0);
signal phase_plus_offset : std_logic_vector(47 downto 0);
signal data_clock_reg_0 :std_logic;
signal data_clock_reg_1 :std_logic;
signal data_clock_reg_2 :std_logic;
signal data_valid :std_logic;
signal phase_inc_register :  STD_LOGIC_VECTOR (N-1 downto 0);
signal phase_offset_register : std_logic_vector(N-1 downto 0);
signal gain_0 : std_logic_vector(15 downto 0);
signal zeros :  STD_LOGIC_VECTOR (N-1 downto 0):=(others=>'0');
begin
psync: process( module_clock,reset) is
begin
    if reset='1' then
        data_clock_reg_0<='0';
        data_clock_reg_1<='0';
        data_clock_reg_2<='0';
        data_valid<='0';
        phase_inc_register<=(others=>'0');
        phase_offset_reg<=(others=>'0');
        gain_0<=(others=>'0');
    elsif rising_edge(module_clock) then
        data_clock_reg_0<=data_clock;
        data_clock_reg_1<=data_clock_reg_0;
        data_clock_reg_2<=data_clock_reg_1;
        if data_clock_reg_2='0' and data_clock_reg_1='1' then
            data_valid<='1';
        else
```

```
            data_valid<='0';
        end if;
        if data_valid='1' then  --sample_data
            phase_inc_register<=phase_inc;
            phase_offset_reg<=phase_offset;
            gain_0<=gain;
        end if;
    end if;
end process psync;

ce<='1';
sin(15 downto 0)<=sin_out;

m2 : mult2
port map (
    clk => module_clock,
    a =>sin_sig1,
    b => gain_0,
    ce => ce,
    p => sin_out);

sc: sin_cos_lut
    port map(
    phase_in=>phase_in_2qn(47 downto 16),
    y_out=>sin_sig0,
    clk=>module_clock,
    ce=>ce);

m1: mult
    port map(
    clk=>module_clock,
    a=>scaler,
    b=>accum1,
    ce=>ce,
    p=>phase_in);

    phase_in_corrected(47 downto 0)<=phase_in(45 downto 0)&"00";
    phase_in_2qn(47 downto 0)<=phase_plus_offset(47)&phase_plus_offset(47)
        &phase_plus_offset(47)&phase_plus_offset(46 downto 2);

p1:process(module_clock,reset) is
begin
    if reset='1' then
        phase_inc_reg<=(others=>'0');
        sin_sig1<=(others=>'0');
        phase_plus_offset<=(others=>'0');
    elsif rising_edge(module_clock) then
        sin_sig1<=sin_sig0;
        phase_plus_offset<=phase_in_corrected+phase_offset_reg;
        phase_inc_reg<=phase_inc_register;
    end if;
end process p1;

Inst_phase_accum: phase_accumulator PORT MAP(
    phase_inc => phase_inc_reg,
    accum => accum1,
    reset => reset,
    clk =>module_clock
    );

end Behavioral;
```

D.2 Phase Accumulator

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
```

```
library UNISIM;
use UNISIM.VComponents.all;

entity phase_accumulator is
Generic(N : integer := 48);
Port ( phase_inc : in  STD_LOGIC_VECTOR (N-1 downto 0);
    accum : out  STD_LOGIC_VECTOR (N-1 downto 0);
    reset : in  STD_LOGIC;
    clk : in  STD_LOGIC);
end phase_accumulator;

architecture Behavioral of phase_accumulator is

component acc
    port (
    b: in std_logic_vector(47 downto 0);
    clk: in std_logic;
    q: out std_logic_vector(47 downto 0));
end component;

component add_48bit
    port (
    a: in std_logic_vector(47 downto 0);
    b: in std_logic_vector(47 downto 0);
    clk: in std_logic;
    sclr: in std_logic;
    s: out std_logic_vector(47 downto 0));
end component;

--100x10^12
--constant phase_max: std_logic_vector(N-1 downto 0):=x"5AF3107A4000";
-- -100x10^12
--constant neg_phase_max: std_logic_vector(N-1 downto 0):=x"A50CEF85C000";
--120x10^12
constant phase_max: std_logic_vector(N-1 downto 0):=x"6D23AD5F8000";
--120x10^12
constant neg_phase_max: std_logic_vector(N-1 downto 0):=x"92DC52A08000";
constant zeros :  STD_LOGIC_VECTOR (N-1 downto 0):=(others=>'0');
signal inc0: std_logic_vector(N-1 downto 0);
signal inc1: std_logic_vector(N-1 downto 0);
signal adv0: std_logic_vector(N-1 downto 0);
signal accum0: std_logic_vector(N-1 downto 0);
signal accum0_reg: std_logic_vector(N-1 downto 0);
signal phase_inc_reg: std_logic_vector(N-1 downto 0);
signal accum1: std_logic_vector(N-1 downto 0);
signal over_flow : std_logic;
begin
    accum<=accum1;
    add0 : add_48bit
    port map (
        a => accum0,
        b => inc0,
        clk => clk,
        sclr => reset,
        s => accum0);

    add1 : add_48bit
    port map (
        a => accum0_reg,
        b => inc1,
        clk => clk,
        sclr => reset,
        s => accum1);

    p1: process(clk,reset) is
    begin
        if reset='1' then
            inc0<=(others=>'0');
            inc1<=(others=>'0');
```

```
            accum0_reg<=(others=>'0');
            over_flow<='0';
        elsif rising_edge(clk) then
            accum0_reg<=accum0;
            adv0<=neg_phase_max+phase_inc;
            accum0_reg<=accum0;
            if (accum0 >= phase_max )then
                over_flow<='1';
                if over_flow ='0' then
                    inc0<=adv0;
                else
                    over_flow<='0';
                    inc0<=phase_inc;
                end if;
                inc1<=neg_phase_max;
            else
                over_flow<='0';
                inc1<=zeros;
                inc0<=phase_inc;
            end if;
        end if;
    end process p1;
end Behavioral;
```

Appendix E

Operational History

E.1 SPC2

Table E.1: The particle beams produced by SPC2 and injected into the SSC between 6 February 2016 and 19 October 2017.

No	Date	Frequency [MHz]	Power [kW]	Particle	Energy [MeV]
1	2015-02-06	13.312675	4.4	$^{40}Ar^{7+}$	175
2	2015-02-13	26.000000	21.3	H^{+}	200
3	2015-02-20	26.000000	21.3	H^{+}	200
4	2015-02-27	26.000000	21.3	H^{+}	200
5	2015-03-05	12.083549	2.8	$^{40}Ar^{7+}$	144
6	2015-03-06	12.083549	2.8	$^{40}Ar^{7+}$	144
7	2015-03-13	14.468056	3.7	$^{4}He^{2+}$	200
8	2015-03-20	14.468056	3.7	$^{4}He^{2+}$	200
9	2015-03-21	14.468056	3.7	$^{4}He^{2+}$	200
10	2015-03-27	14.468056	3.7	$^{4}He^{2+}$	200
11	2015-04-03	14.468056	3.7	$^{4}He^{2+}$	200
12	2015-04-10	14.468056	3.7	$^{4}He^{2+}$	200
13	2015-04-17	14.468056	3.7	$^{4}He^{2+}$	200
14	2015-04-24	11.896349	3.5	$^{86}Kr^{12+}$	300
15	2015-05-01	11.896349	3.5	$^{86}Kr^{12+}$	300
16	2015-05-08	11.896349	3.5	$^{86}Kr^{12+}$	300
17	2015-05-15	14.468056	3.7	$^{4}He^{2+}$	200
18	2015-05-22	15.376543	5	$^{14}N^{3+}$	82
19	2015-05-29	15.322345	6.3	$^{16}O^{3+}$	93
20	2015-06-05	14.568634	5	$^{16}O^{3+}$	84
21	2015-06-12	14.221051	3.1	$^{22}Ne^{5+}$	110
22	2015-06-26	26.000000	21.3	H^{+}	200
23	2015-07-03	14.468056	3.7	$^{4}He^{2+}$	200
24	2015-07-10	25.962188	16.2	$^{4}He^{2+}$	68
25	2015-07-17	25.398046	14.9	$^{4}He^{2+}$	65

Table E.1 continued: The particle beams produced by SPC2 and injected into the SSC between 6 February 2016 and 19 October 2017.

No	Date	Frequency [MHz]	Power [kW]	Particle	Energy [MeV]
26	2015-09-04	11.379999	4.2	$^{4}He^{2+}$	120
27	2015-09-11	11.379999	4.2	$^{4}He^{2+}$	120
28	2015-09-25	13.740135	3.1	$^{18}O^{4+}$	84
29	2015-11-06	12.080335	2.3	$^{20}Ne^{4+}$	72
30	2015-11-13	25.655769	9	$^{3}He^{2+}$	50
31	2015-11-20	26.000645	8.8	$^{3}He^{1+}$	51.4
32	2015-11-27	26.000000	21.3	H^{+}	200
33	2016-02-05	13.821065	3	$^{18}O^{4+}$	85
34	2016-02-12	13.821065	3	$^{18}O^{4+}$	85
35	2016-02-19	24.024688	9.6	$^{4}He^{2+}$	58
36	2016-02-26	24.819700	10.7	$^{4}He^{2+}$	62
37	2016-03-04	24.819700	10.7	$^{4}He^{2+}$	62
38	2016-03-18	11.701959	2.9	$^{40}Ar^{7+}$	135
39	2016-03-24	12.285665	2.1	$^{36}Ar^{7+}$	134
40	2016-03-31	12.285665	2.1	$^{36}Ar^{7+}$	134
41	2016-04-14	12.285665	2.1	$^{36}Ar^{7+}$	134
42	2016-04-21	12.285665	2.1	$^{36}Ar^{7+}$	134
43	2016-04-28	12.228267	3.0	$^{32}S^{5+}$	118
44	2016-05-05	12.228267	3.0	$^{32}S^{5+}$	118
45	2016-05-13	25.962180	16.6	$^{4}He^{2+}$	68
46	2016-05-20	25.999920	17.9	H^{+}	200
47	2016-05-27	19.664119	4.4	H^{+}	100
48	2016-06-01	19.664119	4.4	H^{+}	100
49	2016-06-08	19.664119	4.5	H^{+}	100
50	2016-06-17	25.655769	8.8	$^{3}He^{2+}$	50
51	2016-06-30	25.655769	9.0	$^{3}He^{2+}$	50
52	2016-07-08	25.655769	9.3	$^{3}He^{2+}$	50
53	2016-07-14	25.655769	9.3	$^{3}He^{2+}$	50
54	2016-07-22	25.655769	9.3	$^{3}He^{2+}$	50
55	2016-07-28	11.049429	2.5	$^{3}He^{2+}$	85
56	2016-10-21	11.380000	4.2	$^{4}He^{2+}$	120
57	2016-10-28	11.380000	4.2	$^{4}He^{2+}$	120
58	2016-11-11	26.000000	18.0	H^{+}	200
59	2016-11-18	26.000000	18.0	H^{+}	200
60	2016-12-12	25.655769	9.3	$^{4}He^{2+}$	200
61	2017-01-19	14.468056	4.6	$^{4}He^{2+}$	200
62	2017-02-09	14.468056	4.6	$^{3}He^{2+}$	50
63	2017-02-17	26.000000	18.0	H^{+}	200
64	2017-02-24	26.000000	18.0	H^{+}	200
65	2017-03-03	26.000000	18.0	H^{+}	200
66	2017-03-10	26.000000	18.0	H^{+}	200
67	2017-04-21	19.664119	5.6	H^{+}	100

Table E.1 continued: The particle beams produced by SPC2 and injected into the SSC between 6 February 2016 and 19 October 2017.

No	Date	Frequency [MHz]	Power [kW]	Particle	Energy [MeV]
68	2017-05-04	11.049429	2.4	$^{3}He^{2+}$	85
69	2017-05-12	17.842609	3.3	H^{+}	80
70	2017-05-18	17.842609	3.3	H^{+}	80
71	2017-05-27	17.842609	3.3	H^{+}	80
72	2017-05-31	14.468056	4.0	$^{4}He^{2+}$	200
73	2017-06-08	14.468056	4.0	$^{4}He^{2+}$	200
74	2017-09-08	21.898982	6.2	$^{4}He^{2+}$	48
75	2017-09-15	21.673964	6.0	$^{4}He^{2+}$	47
76	2017-09-28	13.821064	2.5	$^{18}O^{4+}$	85
77	2017-10-19	12.585160	3.5	$^{22}Ne^{4+}$	86

E.2 SPC1

Table E.2: The particle beams produced by SPC1 and injected into the SSC between November 2016 and 20 October 2017.

No	Date	Frequency [MHz]	Power [kW]	Particle	Energy [MeV]
1	2016-11-01	16.373600	8	H^{+}	66
2	2016-11-07	16.373600	8	H^{+}	66
3	2016-11-14	16.373600	8	H^{+}	66
4	2016-11-21	16.373600	8	H^{+}	66
5	2016-11-28	16.373600	8	H^{+}	66
6	2016-12-05	16.373600	8	H^{+}	66
7	2016-12-12	16.373600	8	H^{+}	66
8	2016-12-19	16.373600	8	H^{+}	66
9	2017-01-16	16.373600	8	H^{+}	66
10	2017-01-23	16.373600	8	H^{+}	66
11	2017-01-30	16.373600	8	H^{+}	66
12	2017-02-06	16.373600	8	H^{+}	66
13	2017-02-13	16.373600	8	H^{+}	66
14	2017-02-20	16.373600	8	H^{+}	66
15	2017-02-27	16.373600	8	H^{+}	66
16	2017-03-06	16.373600	8	H^{+}	66
17	2017-03-13	16.373600	8	H^{+}	66
18	2017-03-17	26.000000	14	H^{+}	200
19	2017-03-20	16.373600	8	H^{+}	66
20	2017-03-24	26.000000	14	H^{+}	200
21	2017-03-27	16.373600	8	H^{+}	66
22	2017-03-31	26.000000	14	H^{+}	200
23	2017-04-10	16.373600	8	H^{+}	66
24	2017-04-13	19.664175	11	H^{+}	100

Table E.2 continued: The particle beams produced by SPC1 and injected into the SSC between November 2016 and 20 October 2017.

No	Date	Frequency [MHz]	Power [kW]	Particle	Energy [MeV]
25	2017-04-17	16.373600	8	H^+	66
26	2017-04-24	16.373600	8	H^+	66
27	2017-05-01	16.373600	8	H^+	66
28	2017-05-08	16.373600	8	H^+	66
29	2017-05-15	16.373600	8	H^+	66
30	2017-05-22	16.373600	8	H^+	66
31	2017-05-29	16.373600	8	H^+	66
32	2017-06-05	16.373600	8	H^+	66
33	2017-07-17	16.373600	8	H^+	66
34	2017-07-24	16.373600	8	H^+	66
35	2017-07-27	10.880840	7	H^+	27.5
36	2017-07-31	16.373600	8	H^+	66
37	2017-08-04	16.373600	8	H^+	66
38	2017-08-18	26.000000	14	H^+	200
39	2017-08-19	16.373600	8	H^+	66
40	2017-08-24	25.504635	12	H^+	190
41	2017-08-26	16.373600	8	H^+	66
42	2017-08-29	26.000000	14	H^+	200
43	2017-09-01	16.373600	8	H^+	66
44	2017-09-11	16.373600	8	H^+	66
45	2017-09-18	16.373600	8	H^+	66
46	2017-10-09	16.373600	8	H^+	66
47	2017-10-20	16.373600	8	H^+	66

E.3 AX-line Buncher

Table E.3: The particle beams for which the AX-line buncher has been in use between 8 June 2017 and 19 October 2017.

No	Date	Frequency [MHz]	Power [W]	Particle	Energy [MeV]
1	2017-06-08	14.468056	2.5	$^4He^{2+}$	200
2	2017-09-08	21.898982	3	$^4He^{2+}$	48
3	2017-09-15	21.673964	3	$^4He^{2+}$	47
4	2017-09-28	13.821064	2.5	$^{18}O^{4+}$	85
5	2017-10-19	12.585160	2.5	$^{22}Ne^{4+}$	86

E.4 K-line Buncher

Table E.4: The particle beams for which the K-line buncher has been in use between 8 June 2017 and 19 October 2017.

No	Date	Frequency [MHz]	Power [kW]	Particle	Energy [MeV]
1	2017-06-08	28.936112	2	$^{4}He^{2+}$	200
2	2017-09-08	43.797964	2.5	$^{4}He^{2+}$	48
3	2017-09-15	43.347928	2.5	$^{4}He^{2+}$	47
4	2017-09-28	27.642128	2.2	$^{18}O^{4+}$	85
5	2017-10-19	25.170320	2.2	$^{22}Ne^{4+}$	86

E.5 J-line Buncher

Table E.5: The particle beams for which the J-line buncher has been in use between 17 July 2017 and 20 October 2017.

No	Date	Frequency [MHz]	Power [kW]	Particle	Energy [MeV]
1	2017-07-17	32.747200	4	H^{+}	66
2	2017-07-27	21.761680	3.9	H^{+}	27.5
3	2017-07-31	32.747200	4	H^{+}	66
4	2017-08-04	32.747200	4	H^{+}	66
5	2017-08-18	52.000000	4	H^{+}	200
6	2017-08-19	32.747200	4	H^{+}	66
7	2017-08-24	51.009270	3.8	H^{+}	190
8	2017-08-26	32.747200	4	H^{+}	66
9	2017-08-29	52.000000	4	H^{+}	200
10	2017-09-01	32.747200	4	H^{+}	66
11	2017-09-08	43.797964	3.7	$^{4}He^{2+}$	48
12	2017-09-11	32.747200	4	H^{+}	66
13	2017-09-15	43.347928	3.6	$^{4}He^{2+}$	47
14	2017-09-18	32.747200	4	H^{+}	66
15	2017-09-28	27.642128	3.8	$^{18}O^{4+}$	85
16	2017-10-09	32.747200	4	H^{+}	66
17	2017-10-19	25.170320	3.7	$^{22}Ne^{4+}$	86
18	2017-10-20	32.747200	4	H^{+}	66

E.6 Pulse-Selector

Table E.6: The particle beams for which the pulse-selector RF system has been in use between 17 July 2017 and 28 September 2017.

No	Date	Frequency [MHz]	Power [W]	Particle	Energy [MeV]
1	2017-07-27	2.720210	200	H^{+}	27.5
2	2017-09-08	3.128426	183	$^{4}He^{2+}$	48
3	2017-09-15	3.096281	180	$^{4}He^{2+}$	47
4	2017-09-28	2.764213	170	$^{18}O^{4+}$	85

E.7 SSC

Table E.7: The particle beams produced by the SSC between 17 July 2017 and 20 October 2017.

No	Date	Frequency [MHz]	Power [kW]	Particle	Energy [MeV]
1	2017-07-17	16.373600	62	H^{+}	66
2	2017-07-27	10.880840	33	H^{+}	27.5
3	2017-07-31	16.373600	62	H^{+}	66
4	2017-08-04	16.373600	62	H^{+}	66
5	2017-08-18	26.000000	72	H^{+}	200
6	2017-08-19	16.373600	62	H^{+}	66
7	2017-08-24	25.504635	65	H^{+}	190
8	2017-08-26	16.373600	62	H^{+}	66
9	2017-08-29	26.000000	72	H^{+}	200
10	2017-09-01	16.373600	62	H^{+}	66
11	2017-09-08	21.898982	35	$^{4}He^{2+}$	48
12	2017-09-11	16.373600	62	H^{+}	66
13	2017-09-15	21.673964	34	$^{4}He^{2+}$	47
14	2017-09-18	16.373600	62	H^{+}	66
15	2017-09-28	13.821064	40	$^{18}O^{4+}$	85
16	2017-10-09	16.373600	62	H^{+}	66
17	2017-10-19	12.585160	37	$^{22}Ne^{4+}$	86
18	2017-10-20	16.373600	62	H^{+}	66

E.8 SSC Flat-topping

Table E.8: The particle beams produced from the SSC while the flat-topping system was enabled between 17 July 2017 and 20 October 2017.

No	Date	Frequency [MHz]	Power [kW]	Particle	Energy [MeV]
1	2017-07-17	49.120800	1.2	H^+	66
2	2017-07-31	49.120800	1.2	H^+	66
3	2017-08-04	49.120800	1.2	H^+	66
4	2017-08-19	49.120800	1.2	H^+	66
5	2017-08-26	49.120800	1.2	H^+	66
6	2017-09-01	49.120800	1.2	H^+	66
7	2017-09-11	49.120800	1.2	H^+	66
8	2017-09-18	49.120800	1.2	H^+	66
9	2017-10-09	49.120800	1.2	H^+	66
10	2017-10-20	49.120800	1.2	H^+	66

E.9 The Helmholtz-Zentrum Berlin's Separated Sector Cyclotron

Table E.9: A table of the particle beams produced at the Helmholtz-Zentrum Berlin using the new control system for the period 15 June 2017 until 15 September 2017.

No	Start Date	End Date	Frequency [MHz]	Power [kW]	Particle	Energy [MeV]	No. of Patients
1	2017-06-15	2017-06-23	19.317800	25	H^+	68	24
2	2017-07-14	2017-07-21	19.317800	25	H^+	68	17
3	2017-08-17	2017-08-25	19.317800	25	H^+	68	12
4	2017-09-14	2017-09-15	19.852100	20	He^{3+}	50	-