

Small-Signal analysis of asymmetrical regular sampled PWM control loops

by

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Declaration

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Summary

In recent years it has become important to be able to design optimal PWM control loops to improve the performance of DC-AC power converters. This would depend on how accurate the stability margins of the control loops can be determined, especially the non-linearity introduced into a PWM control loop by the switching of the pulse-width modulator. By finding the small-signal models of pulse-width modulators it is shown that the stability margins of a control loop can be very accurately determined. However, the derivation of a small-signal model for an asymmetrical regular sampled pulse-width modulator is complicated by the duty cycle value getting updated each half of the switching period. Previously the small-signal model has been approximated by a zero-order hold model, but the accuracy of this approximation is questionable.

In this research an accurate discrete-time small-signal model is derived for an asymmetrical regular sampled pulse-width modulator. It is shown that the proposed small-signal model is able to predict the gain margin of asymmetrical regular sampled PWM control loop more accurately than the original zero-order hold model. Two discrete-time state space small-signal models have been derived for single-phase and three-phase PI current regulator systems.

The accuracy of the small-signal models are verified by incrementing the loop gain and finding the eigenvalues of the closed loop state space system through which the gain margin is predicted. The gain margin predicted by the small-signal model is compared to a bifurcation diagram to determine its accuracy.

The single-phase small-signal model is then compared with the zero-order hold model, to show the influence of the duty cycle value on the gain margin of a closed loop system. This approach differs from the zero-order hold model which assumes that the influence of the duty cycle is negligible.

It is further shown that the accuracy of the zero-order hold model is dependent on the time-constant of the RL-load, in that, for a small time-constant, it becomes inaccurate. However, the single-phase small-signal model derived is still able to accurately determine the gain margin.

The accuracy of applying the zero-order hold model to a balanced three-phase PWM control loop is also investigated. Similar to the single-phase small-signal model, a three-phase small-signal model is derived for the asymmetrical regular sampled pulse-width modulator in its stationary d-q frame. A Clarke's transformation is used to express three-phase system into its equivalent α and β control loops. Again, the shortcomings of the zero-order hold model are pointed out. It is shown that the unstable operation of the α loop causes the β loop to go into unstable operation. Because the zero-order hold model assumes that the α and β loops are independent it is not possible to determine the influence of the α loop on the β loop.

Opsomming

Gedurende die laaste paar jare het dit belangrik begin word om optimale PWM beheerlusse te kan ontwerp om die gedrag van GS-WS omsetters te verbeter. Die ontwerp van optimale PWM beheerlusse sal afhang van hoe akkuraat die stabiliteitgrense van die beheerlusse bepaal kan word om sodoende vir die optimale lus aanswins te kan ontwerp, veral in die geval wanneer daar nie-lineariteit binne 'n PWM beheerlus ontstaan as gevolg van skakeling binne in 'n puls-wydte modulator. Vanaf die kleinsein-model van 'n puls-wydte modulator kan die stabiliteitgrense van 'n beheerlus baie akkuraat bepaal word.

In hierdie navorsing word 'n kleinsein-model vir 'n asimmetries gemonsterde puls-wydte modulator toestandsveranderlike model afgelei. As gevolg van die dienssiklus wat elke halwe skakel periode opgedateer word, raak die probleem meer kompleks. Voorheen is die kleinsein-model slegs deur 'n eenvoudige zero-order hou model voorgestel, maar die akkuraatheid van hierdie benadering word bevraagteken.

In hierdie navorsing is 'n akkurate diskrete-tyd kleinsein-model afgelei vir 'n asimmetriese gemonsterde puls-wydte modulator. Dit word bewys dat die voorgestelde kleinsein-model in staat is om die aanwings grens van 'n asimmetriese gemonsterde PWM beheerlus meer akkuraat te voorspel as die oorspronklike zero-order hou model. Twee diskrete-tyd toestandsveranderlike kleinsein modelle is afgelei vir beide enkelfase en driefase PI beheerde geslotelus stelsels.

Die akkuraatheid van die voorgestelde kleinsein modelle is geverifieer deur die lus aanswins te verhoog en terselfdertyd die eiewaardes te bereken van die toestandsveranderlike model om sodoende die geslotelus pole te analiseer waardeur die aanwings grens voorspel kan word. Die aanwings grens van die kleinsein-model word dan vergelyk met 'n bifurkasie diagram om te bepaal hoe akkuraat die model is.

Die enkelfase kleinsein model word dan vergelyk met die zero-order hou model om die invloed van die dienssiklus waardes op die aanwings grens van die geslotelus van die stelsel te bepaal. In teenstelling met die zero-order hou model wat aanvaar dat die invloed van die dienssiklus geignoreer kan word. Daar word ook bewys dat die akkuraatheid van die zero-order hou model afhanklik is van die tydkonstante van die RL-las en waar 'n klein

tydkonstante gebruik word die zero-order hou model 'n onakkurate model word.

Die akkuraatheid van die zero-order hou model word ook ondersoek op 'n gebalanseerde driefase PWM beheerlus. Soortgelyk aan die enkelfase kleinsein model is 'n driefase kleinsein model afgelei vir die asimmetriese gemonsterde puls-wydte modulator in sy stationere d-q raamwerk. Clarke transformasie is gebruik om die driefase stelsel in sy ekwivalent α en β beheerlusse uit te druk. Weereens is die verkortkoming van die zero-order hou model ook aangedui vir 'n gebalanseerde driefase sisteem. Dit is bewys dat onstabieliteit binne die α lus veroorsaak dat die β lus ook in onstabiele werking gaan. Indien die zero-order hou model gebruik word, word die α en β beheerlusse onafhanklik voorgestel en daarom is dit nie moontlik om met die zero-order hou model die invloed van die α lus op die β lus te bepaal nie.

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Nomenclature

Variables

λ	Ratio for Generalised Triangular Carrier
$\tilde{f}(k)$	Discrete-Time Small-Disturbance Modulating Signal
$\tilde{i}(k)$	Discrete-Time Small-Disturbance Load Current
$c(t)$	Carrier Signal
d	Duty Cycle
d_1	Duty Cycle for First Half of Switching Period
d_2	Duty Cycle for Second Half of Switching Period
$f(k)$	Discrete-Time Large Modulating Signal
$i(k)$	Discrete-time Load Current
$i(t)$	Continuous-Time Load current
$i^*(k)$	Discrete-Time Reference Current
$i_{\alpha,\beta}^*(k)$	Discrete-time α and β Reference Currents
$i_{\alpha,\beta}(k)$	Discrete-time α and β Load Currents
$i_{\alpha,\beta}(t)$	Continuous-time α and β Load Currents
$i_{a,b,c}(t)$	Continuous-Time Load currents for Phases A,B and C
K_i	Integral Gain
K_p	Proportional Gain
L	Load Inductance
$p(t)$	Pulse-Width Modulation Signal

R	Load Resistance
T_c	Switching Period
T_s	Sampling Period
$v(t)$	Phase Voltage
V_{dc}	DC-Bus Voltage

Abbreviations

AC	Alternating Current
ADC	Analogue-to-Digital Converter
DC	Direct Current
$DPWM$	Digital Pulse-Width Modulator
$FPGA$	Field-Programmable Gate Array
KVL	Kirchoffs Voltage Law
$NSPWM$	Naturally Sampled Pulse-Width Modulation
P	Proportional
PI	Proportional-Integral
PWM	Pulse-Width Modulation
ZOH	Zero-Order Hold
DSP	Digital Signal Processor
RSPWM	Regular Sampled Pulse-Width Modulation
SMPS	Switch Mode Power Supplies

Chapter 1

Introduction

1.1 Background

The improvement in performance of digital signal processors (DSP) during the past decades necessitated more complex and accurate digital control algorithms [5]. Figure 1.1 is an example of a digital current control loop, separated into two time domains, the discrete-time and the continuous-time domain. The digital current regulator together with the digital pulse-width modulator (DPWM), also called the regular sampled pulse-width modulator are represented in the discrete-time domain. The plant $G(s)$ is represented in the continuous-time domain.

A DSP is used to implement the digital current regulator and to generate the switching states of the gate signals in the switch mode power supplies (SMPS). The continuous-time load current $i(t)$ is measured by an analog-to-digital converter (ADC) and fed back into digital control loop. According to [6] the ADC can be mathematically modelled as a cascaded ideal sampler and a uniform quantizer.

The difference between the discrete-time current reference $i^*(k)$ and the output current $i(k)$ results in the discrete-time error signal $e(k)$. The discrete-time error signal $e(k)$ is applied to the input of the digital current regulator and results in a discrete modulating signal $f(k)$. Depending on the value of the digital modulating signal $f(k)$, the DPWM will produce the switching states $p(t)$ in the continuous-time domain. In [6] this process is referred to as the interpolation process, or the digital pulse-width modulation (PWM). The DPWM is therefore the interface between the digital-time domain and the continuous-time domain.

It is well known that the switching behaviour of the DPWM contributes to the non-linearity within a PWM control loop [7]. It is therefore important that an accurate DPWM model is obtained to design an optimal performance digital PWM control loops.

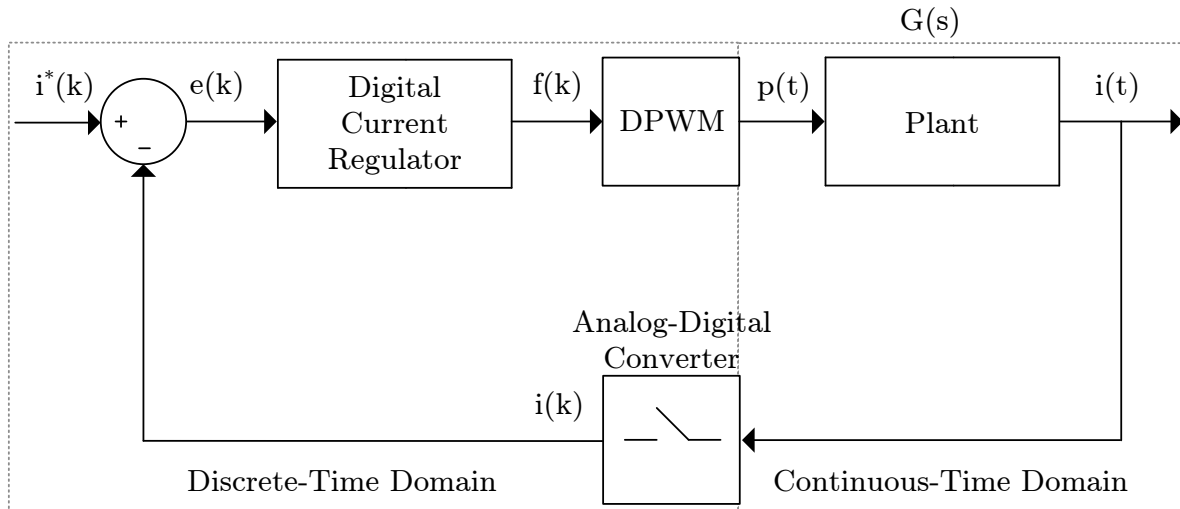


Figure 1.1: Typical example of a digital control loop where a discrete-time reference current $i^*(k)$ is applied to the input and results in a regulated continuous-time output current $i(t)$.

Previously a pulse-width modulator was modelled only using a simple gain, however, recent research [1] has shown that this not the case. The use of the simple gain model implies that the controller bandwidth must be infinite. The maximum controller bandwidth however is limited by the Nyquist frequency. Another constraint not considered by using the average pulse-width modulator model is the ripple component of the feedback signal. This also causes non-linearity in the PWM process due to aliasing of the high-frequency carrier components [8][9]. This suggests that the pulse-width modulator has a much bigger influence on the stability of a control loop than expected.

According to [1] with small-signal models of pulse-width modulators, the stability of PWM control loops can be predicted with a high-degree of accuracy. From the accuracy of the small-signal model it will depend on how accurately the stability limits can be determined. To achieve optimal performance from these digital current regulators it is important to be able to find the stability limits of a system. This will ensure that an optimal loop gain is obtained.

In previous literature [10] [6] [11] different PWM small-signal models have been derived. In [10] the regular sampled pulse-width modulator is modelled as a simple gain, combined with a quarter-carrier-period transport delay. In [11] small-signal approximations have been used to find the Laplace domain transfer functions for different regular sampled pulse-width modulator. In [6] it is shown that a zero-order hold (ZOH) transfer function can be used as a general regular sampled pulse-width modulator small-signal model. This simplifies the design process of regular sampled PWM control loops significantly, but the accuracy of this ZOH model is yet to be discussed. These approximations represent an

averaging method that does not consider the effect of the change in duty cycle in the control loop. In previous research it has been noticed that some of these control loops are unstable in simulation and during testing for a certain set of parameters [1], while the theoretical models predicts them to be perfectly stable.

This thesis takes a look at the accuracy of these approximations and introduces a more precise model that predicts the stability margins with a high-degree of accuracy. Bifurcation diagrams are used to accurately determine the stability limits of the actual system through simulation.

The advantage of using the small-signal model of a pulse-width modulator:

- **Takes into consideration the change in duty cycle:** For asymmetrical regular sampled pulse-width modulator the duty cycle is updated twice over a switching period. This means that the duty cycle will differ for the two halves of the switching frequency. This effect has not been considered in previous research.
- **Accurate method to determine stability limits:** The capability of determining the exact stability limits of the control loop depends on the accuracy of the small-signal model of the pulse-width modulator.
- **Design of optimal PWM control loops:** If a small-signal model is able to accurately determine the stability limits of PWM control loops accurately, it can be used to design optimal controllers.

1.2 Study Objectives

The aim of this study is to derive a small-signal model for an asymmetrical regular sampled pulse-width modulator using a state space representation. This will be implemented for a single and a three phase closed loop system. The small-signal model will then be compared to the conventional (ZOH, etc) method in order to compare the accuracy to which to predict the stability margins. A more accurate asymmetrical regular sampled pulse-width modulator small-signal model is derived and used to predict the stability margins. The mathematical model is then simulated and compared to practical simulation. Various controllers (Proportional (P), Proportional-Integral (PI)) are used to show the difference they will have on the stability. The main objective is to derive accurate small-signal models for the single- and three-phase pulse-width modulators and not the specific design of a current regulator. More focus will be on the stability analysis of the PWM control loop together with the small-signal model. To achieve these objectives the following needs to be completed:

- Study small-signal models used in previous research and how this could contribute to the research about asymmetrical regular sampled pulse-width modulator;
- Study on stability tests that could be used in conjunction with the small-signal models to derive an accurate equivalent asymmetrical regular sampled pulse-width modulator small-signal model;
- A small-signal model for each of the single and three-phase PWM control loops should be derived and tested to determine their accuracy;
- Investigate whether the mathematical models derived for the small-signal models corresponds to the simulation;
- Implementation of P- and PI- current regulators and analyse the influence they have on the small-signal models;
- Determine the effect of variation of parameters on the stability margins of the PWM control loop;
- Verify that the simulation results correlates with the simulation model of the practical system.

1.3 Thesis Overview

In **Chapter 2** the difference between analog- and digital sampled PWM control loops are discussed along with the different regular sampled pulse-width modulators available. Then the effect of non-ideal delays inherent to a digital sampled PWM control loop are discussed. The concept of small-signal models are explained and how it fits in with DPWM. The derivation process involved to obtain a small-signal model is also explained in general. Different regular sampled- and naturally- sampled PWM small-signal models are derived. A short description of non-linear behaviour in power converters follows together with bifurcation models which is used to analyse the stability of the PWM control loop.

Chapter 3 explains the mathematical derivation involved for small-signal models of asymmetrical regular sampled pulse-width modulators. At first only a single-phase DC-AC converter is considered and a single-phase small-signal model is derived for the pulse-width modulator. The single-phase model theory is then extended to derive a small-signal model for a three-phase small-signal model implemented in the stationary reference frame ($\alpha\beta$). The small-signal models of the pulse-width modulators are expressed in their state space form.

Chapter 4 uses state representation of the small-signal models derived in Chapter 4 to design a P- and PI digital current regulator. It also shows how flexible these models are when subject to variation in digital current regulator configurations. The effect of the computational delay is also included. A PI current regulator design strategy introduced in previous research is used to calculate the K_i and K_p gains.

Chapter 5 shows the simulation results using Matlab Simulink[®]. The simulation results are used to verify that the asymmetrical regular sampled pulse-width modulator small-signal models derived are satisfactory. The stability is analysed for a variety of parameters which shows the accuracy of the small-signal models of the pulse-width modulators compared to the ZOH model used in previous research.

Chapter 6 Conclusion and recommendations for further research

Chapter 2

Literature Review

2.1 Analog and Digital Sampled PWM Control Loops

In any power converter control loop design the most important decision is the modulation strategy to be used. There exists several types of modulation strategies, but one of the most widely utilized strategies when controlling the AC output of power electronics is PWM [12]. The advantages of PWM over any other approach is the ease of implementation and the fact that it uses fixed frequency inverter operation [6]. To achieve PWM only a carrier signal and a comparator is required. Different carrier waveforms exist, but the most commonly used is either a sawtooth or a triangular carrier.

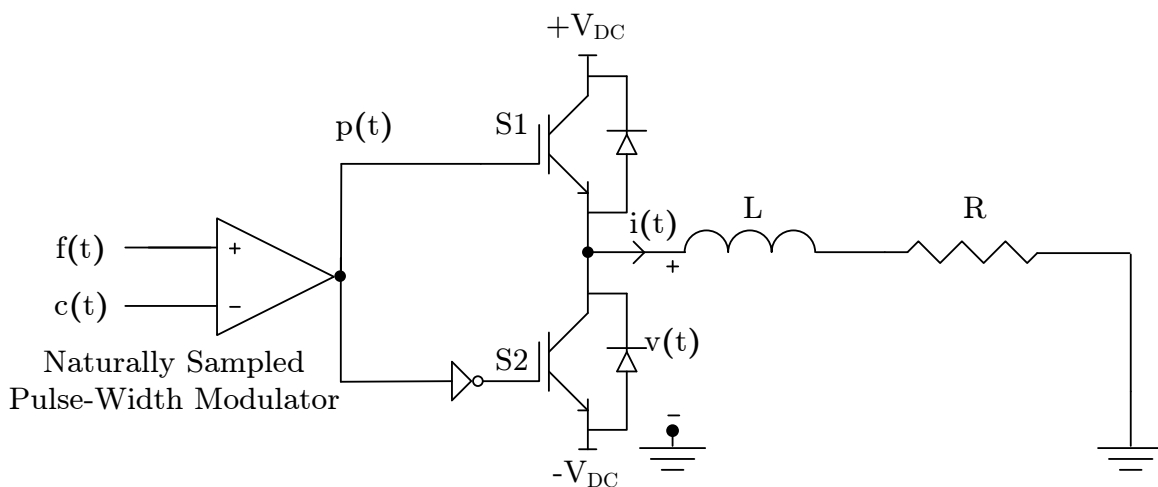


Figure 2.1: Implementation of analog PWM, where the modulating signal $f(t)$ is compared to the carrier signal $c(t)$ to determine state of the switches $S1$ and $S2$.

2.1.1 Naturally Sampled PWM

In Figure 2.1 an example of an analog PWM is shown, also referred to as naturally sampled pulse-width modulation (NSPWM). The pulse-width modulator is used to compare a low-frequency modulating $f(t)$ signal with a carrier signal $c(t)$ which then generates a duty cycle. This duty cycle is used to determine the ON and OFF times of the complimentary switches $S1$ and $S2$ during a switching period. In the waveform shown in Figure 2.2 a switching period equal to the carrier period T_c is used. A switching state change occur at the instant when the modulating signal $f(t)$ intersects with the carrier signal $c(t)$. Figure 2.2 shows that the duty cycle d is updated instantaneously when the intersection occurs; this guarantees a minimum delay between the modulating signal and the duty cycle [6].

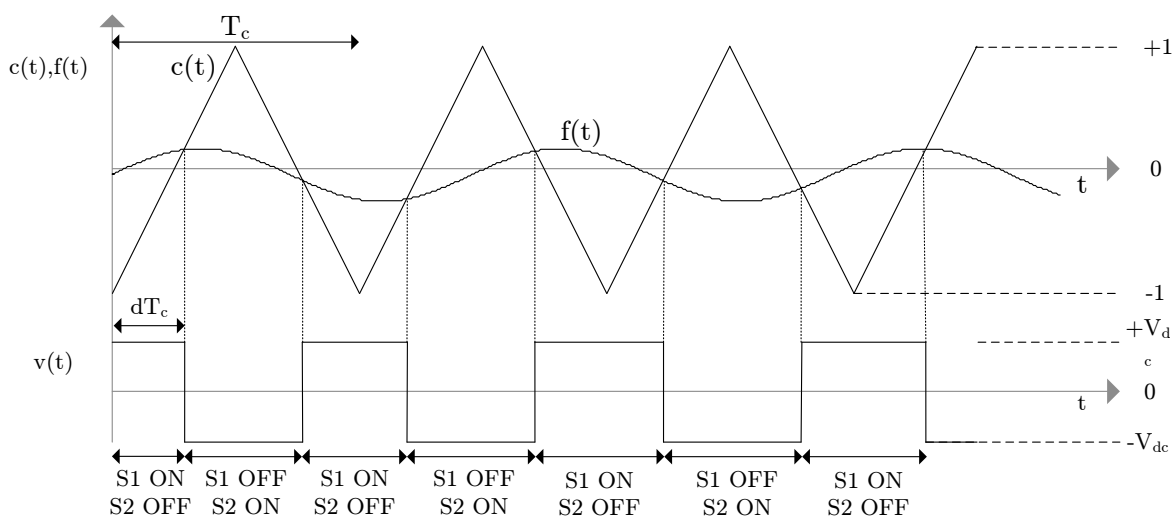


Figure 2.2: The waveforms for the naturally sampled PWM showing the ON and OFF times for $S1$ and $S2$.

In previous research [13] a transfer function has been derived for the pulse-width modulator assuming that for a naturally sampled PWM the delay can be considered negligible. According to this assumption a naturally sampled pulse-width modulator does not contribute to the phase shift of the system and is represented by a simple gain. This assumption is referred to as the average model of the pulse-width modulator. It is also important to note that the average model ignores the sampling process inherent in a pulse-width modulator.

Figure 2.2 also gives the waveforms generated using NSPWM. However, NSPWM is difficult to implement in a digital modulation system, as the intersection between the modulating signal $f(t)$ and the carrier signal $c(t)$ is defined by a transcendental equation [12]. In [11] and [5] small-signal models are used to derive a more accurate models for naturally sampled pulse-width modulators.

2.1.2 Regular Sampled PWM

For digital PWM, also referred to as regular sampled pulse-width modulation (RSPWM), the naturally sampled pulse-width modulator in Figure 2.1 is replaced by a regular sampled pulse-width modulator wherein the modulating signal $f(t)$ is sampled and held constant for each sample period T_s . An equivalent model for a regular sampled pulse-width modulator is shown in Figure 2.3.

The naturally sampled modulating signal $f(t)$ is sampled at each sampling period T_s , resulting in the sampled modulating signal. The sampled modulating signal is then held constant for the entire sampling interval before the sampled modulating signal's value is updated. The sample and hold modulating signal $f(k)$ is then compared to the carrier signal $c(t)$ in order to generate a PWM signal $p(t)$.

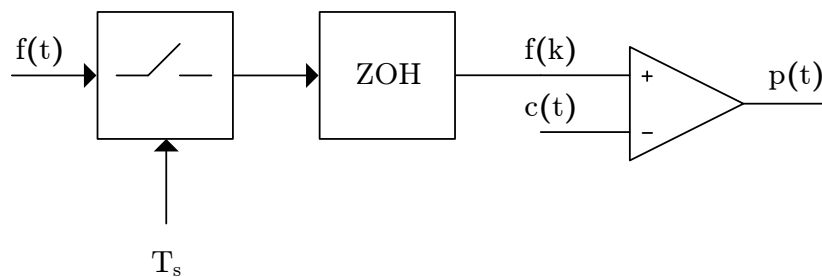


Figure 2.3: Equivalent pulse-width modulator model for regular sampled PWM control loops.

Depending on the type of carrier signal and the sampling used different configurations of regular sampled pulse-width modulators can be obtained. These different configurations of regular sampled pulse-width modulators are shown in Table 2.4.

If the sample period T_s is equal to the carrier period this type of PWM is defined as a symmetrically sampled PWM. This can be achieved by using both sawtooth carriers and triangle carriers. For a sawtooth carrier there are two symmetrically sampled pulse-width modulators, begin-of-on-time- and end-of-on-time symmetrically sampled pulse-width modulators. For a begin-of-on-time symmetrically sampled pulse-width modulator the modulating signal is sampled at the end of the falling edge of the sawtooth carrier, where for the end-of-on-time symmetrically sampled pulse-width modulator the modulating signal is sampled at the end of the rising edge of the sawtooth carrier, with reference to Figure 2.5.

For a triangle carrier there are also two symmetrically sampled pulse-width modulators, symmetric-on-time- and symmetric-off-time symmetrically sampled pulse-width modulators. For a symmetric-on-time symmetrically sampled pulse-width modulator the mod-

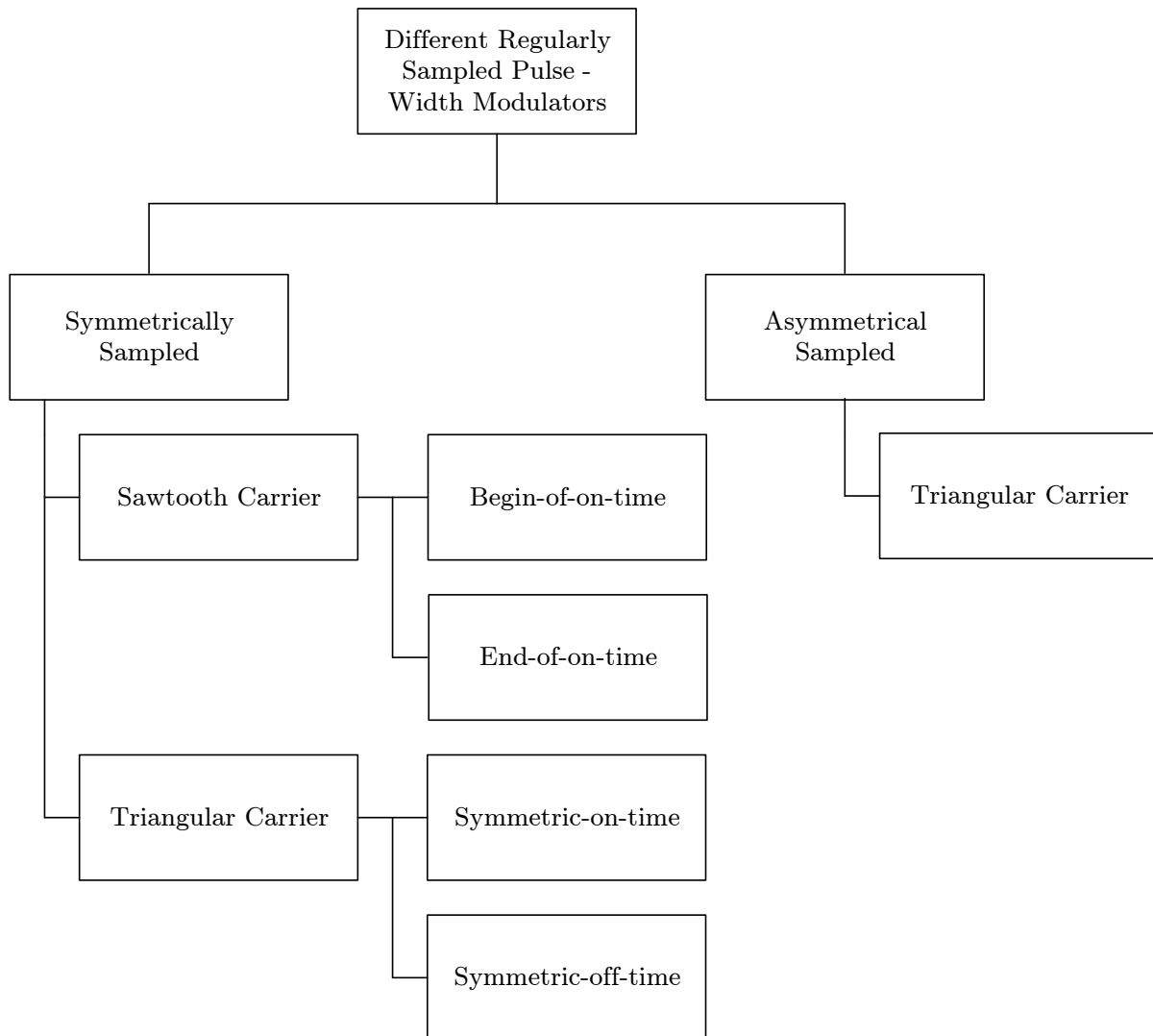
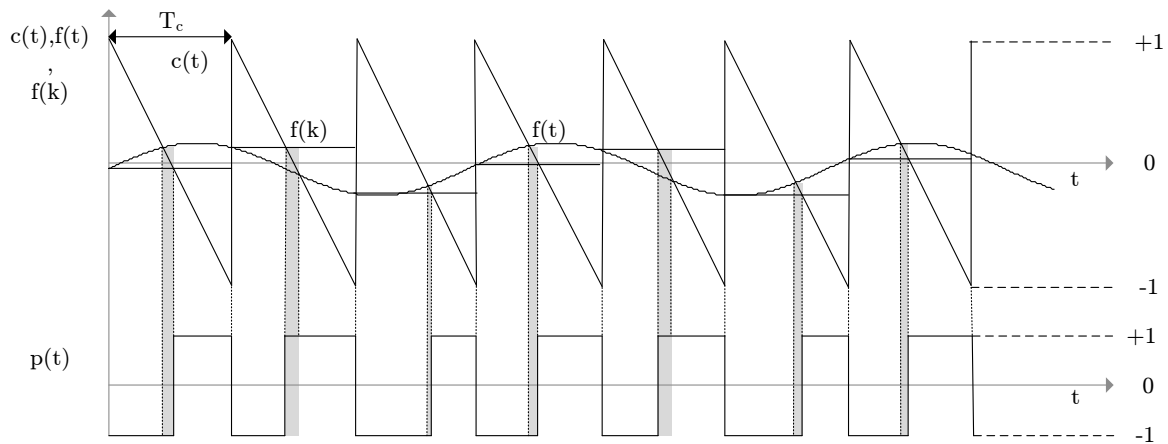


Figure 2.4: Different pulse-width modulators configurations for regularly sampled PWM.

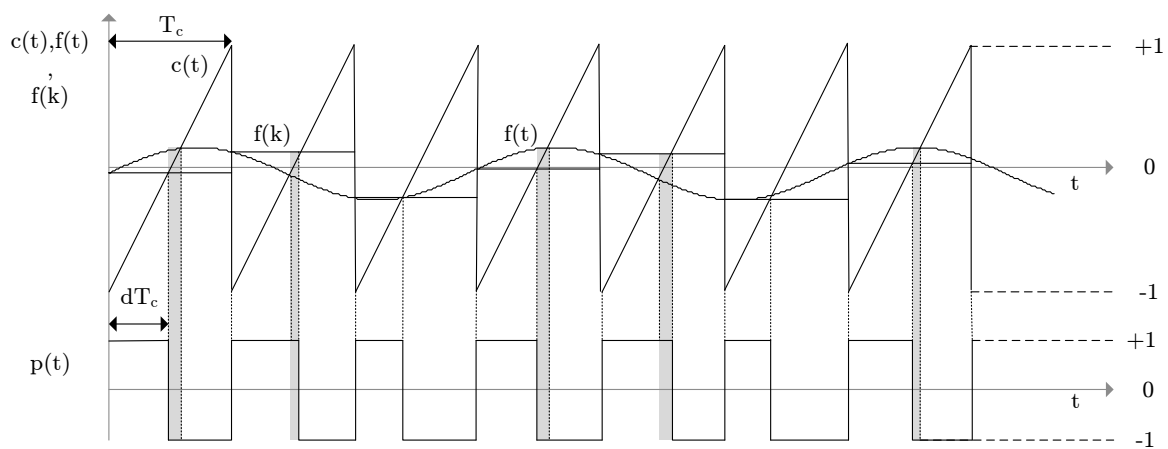
ulating signal is sampled at each positive peak of the triangle carrier, where for the symmetric-off-time symmetrically sampled pulse-width modulator the modulating signal is sampled at each negative peak of the triangle carrier. In Figure 2.6 these different symmetrically sampled pulse-width modulators are shown in more detail.

If the carrier period T_c is equal to twice the sample period T_s this type of PWM is referred to as asymmetrical sampled PWM. Using a triangle carrier the modulating signal is sampled at both the positive and negative peaks of the triangle. The sampled modulating signal is held constant for a half period of the carrier signal before it is updated, resulting in the modulated sample and hold signal.

If the naturally sampled pulse-width modulator in Figure 2.1 is replaced with an asymmetrical regular sampled pulse-width modulator the waveforms in Figure 2.7 are generated. From Figure 2.7 it shows that the intersection between the sample and hold modulating signal and the carrier signal is delayed in comparison with the intersection between the



(a) The begin-of-on-time symmetrically sampled pulse-width modulator.

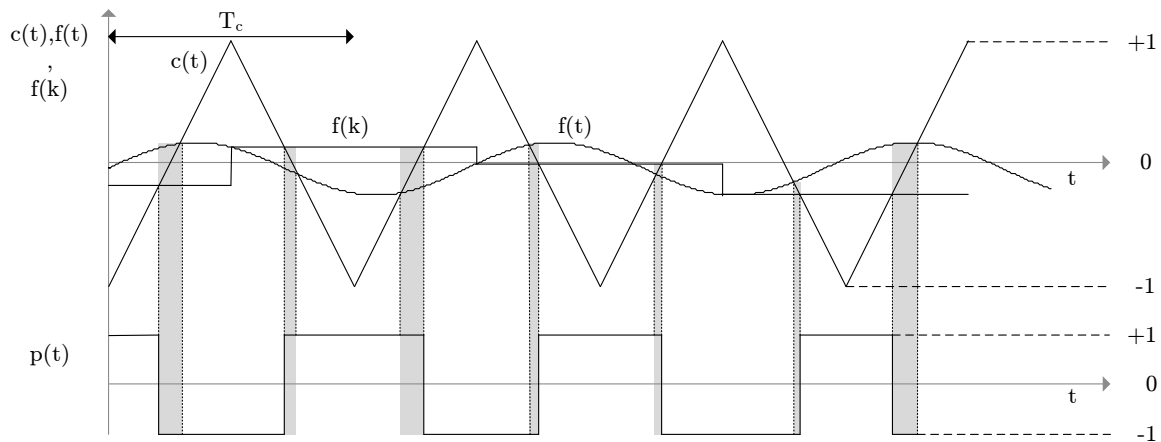


(b) The end-of-on-time symmetrically sampled pulse-width modulator.

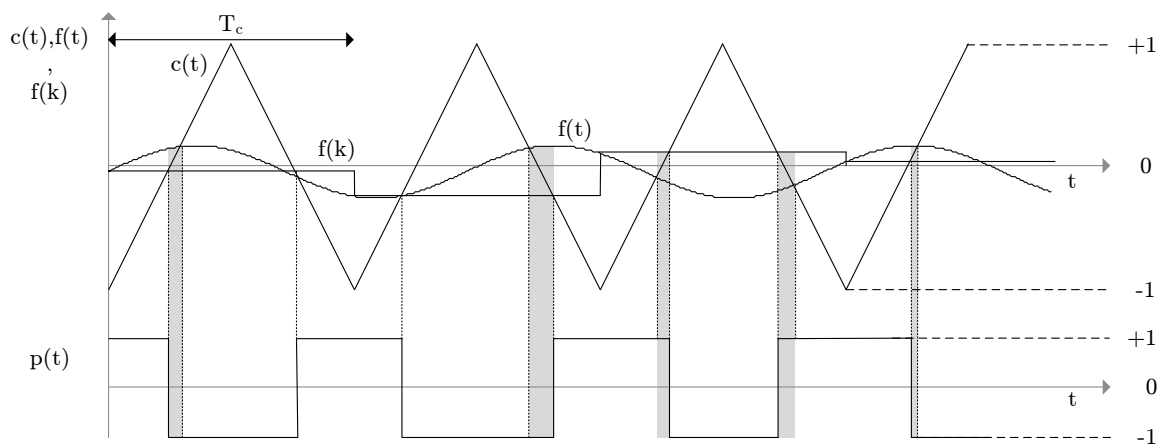
Figure 2.5: Symmetrically sampled pulse-width modulators with sawtooth carrier.

naturally sampled modulating signal and the carrier signal. This delay effect is experienced by each of the regular sampled pulse-width modulators discussed. This forms the significant difference between a NSPWM and RSPWM. The RSPWM therefore introduces additional delays into a digital PWM control loop that contributes to the phase shift of the system, causing the phase margin to reduce. In section 2.2 this will be discussed further.

The main topic in this research is only concerned about asymmetrical RSPWM, more focus will therefore be given to it.



(a) The symmetric-on-time symmetrically sampled pulse-width modulator.



(b) The symmetric-off-time symmetrically sampled pulse-width modulator.

Figure 2.6: Symmetrically sampled pulse-width modulators with triangle carrier.

2.2 Non-Ideal Delays in Digital PWM Control Loops

Over the last few years the use of digital signal processors (DSP's) has become very popular, due to their performance capabilities and reduced cost. A considerable amount of research time has been devoted on increasing the performance to simplify the solution of complex control algorithms. Unlike analog controllers, DSPs are much more adaptable to changes in control strategies. However in the previous section 2.1.2 it is shown that a regular sampled pulse-width modulator introduces additional delays into a digital PWM control loop. These delays affects the stability of the digital PWM control loops which influences the performance of controllers and can therefore not be considered negligible.

The dynamics of digitally controlled power converters are however influenced by two non-ideal delays, firstly the transport delay and secondly the computational delay.

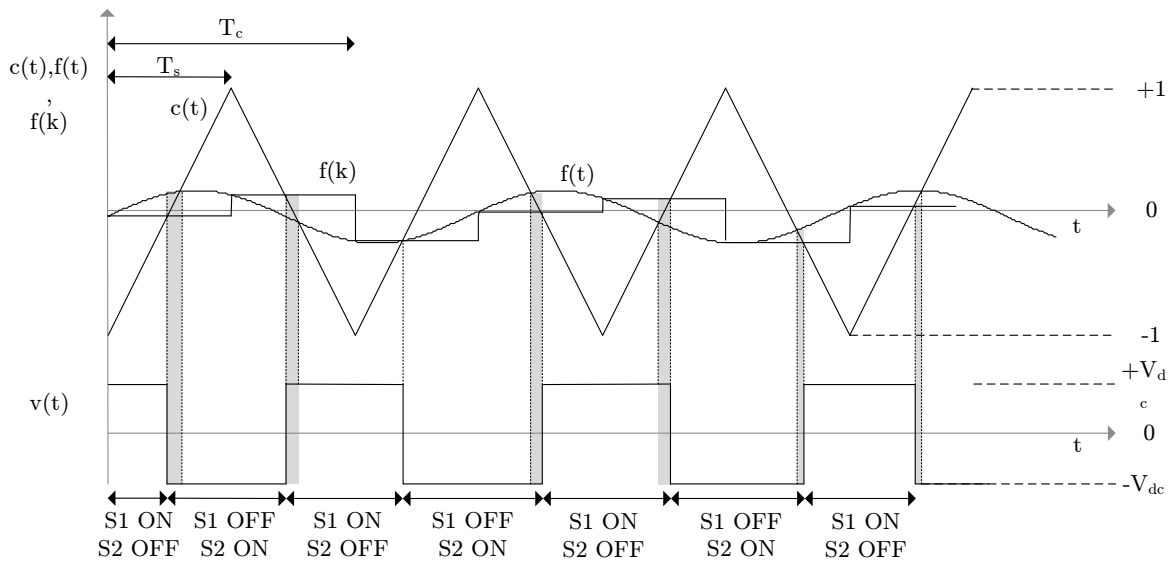


Figure 2.7: The waveforms for the asymmetrical regular sampled PWM showing the ON and OFF times for $S1$ and $S2$ in Figure 2.1.

2.2.1 Transport Delay

From section 2.1.2 it is evident that a regular sampled reference PWM is delayed relative to the naturally sampled PWM. This delay is defined as the transport delay.

In [12] an in-depth investigation is done to determine the delay contribution when using the different regular sampled PWM configurations. In the research it is shown that for any of the symmetrically sampled PWM strategies, the transport delay can be minimized by phase advancing the symmetrically sampled modulating signal by a half carrier period. Similarly for the asymmetrical sampled waveform, where it should be phase advanced by a quarter carrier period. It has been established that a quarter of a carrier period delay is determined to be the maximum error delay that could be experienced between the asymmetrical sampled modulating signal $f(k)$ and the naturally sampled modulating signal $f(t)$. This can be explained by noting that the asymmetrical sampled modulating signal will experience the longest delay when it coincides with the positive (+1) and negative peaks (-1) of the carrier signal. Near the origin (0) the delay would be at its minimum.

Figure 2.8 confirms the above by showing that the delay between the naturally sampled modulating signal $f(t)$ and the asymmetrical sampled modulating signal $f(k)$ is reduced to almost zero if the asymmetrical sampled modulating signal is phased advanced by a quarter carrier period.

A small variation of the instant of the intersection has a marked effect on the stability of a PWM controlled loop system by reducing the phase margin. Using PWM small-signal model theory the influence of these delays can be investigated. In section 2.4 a

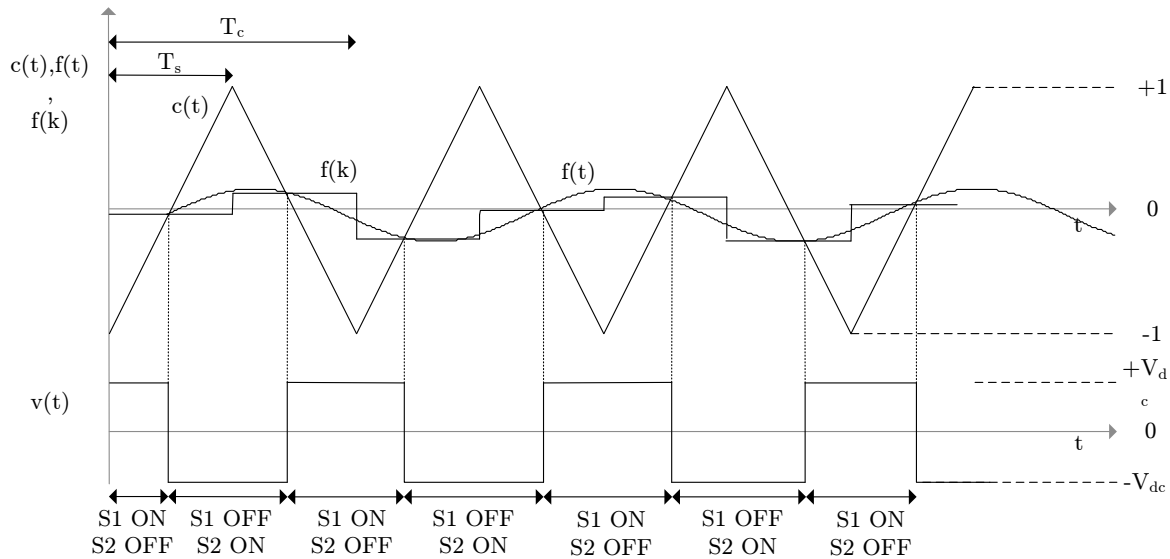


Figure 2.8: The asymmetrical sampled modulating signal $f(k)$ phase advanced by a quarter carrier period.

precise small-signal Laplace-domain analysis is applied to symmetrically sampled- and asymmetrical sampled pulse-width modulators.

2.2.2 Computational Delay

Another type of delay which is common for digital control loops is the computational delay. Since the current cannot be instantaneously sampled and used for calculations a delay of one sample period delay (or half carrier period delay for asymmetrical sampled pulse-width modulators) should also be allowed for in the control loop. When the current is sampled, the output to the pulse-width modulator is calculated and this value is used only at the next sampling instant. As demonstrated in Figure 2.9 which shows that when the modulating signal is sample at ADC 1, the sampled value is used by the DSP to calculate the duty cycle for the next sampling instant. Since high-performance DSPs are now available, this delay becomes very small.

In [10] it is shown how the effect of the computational and transport delay reduces the phase margin of the open loop system. Therefore it is important to be able to predict the stability margins accurately, to be able to design a current regulator having an optimal gain.

2.3 Analysis Using a Small-Signal Model

Due to the pulse-width modulator introducing non-linear effects into the control system, it is difficult to analyse the stability of such a system using the conventional models.

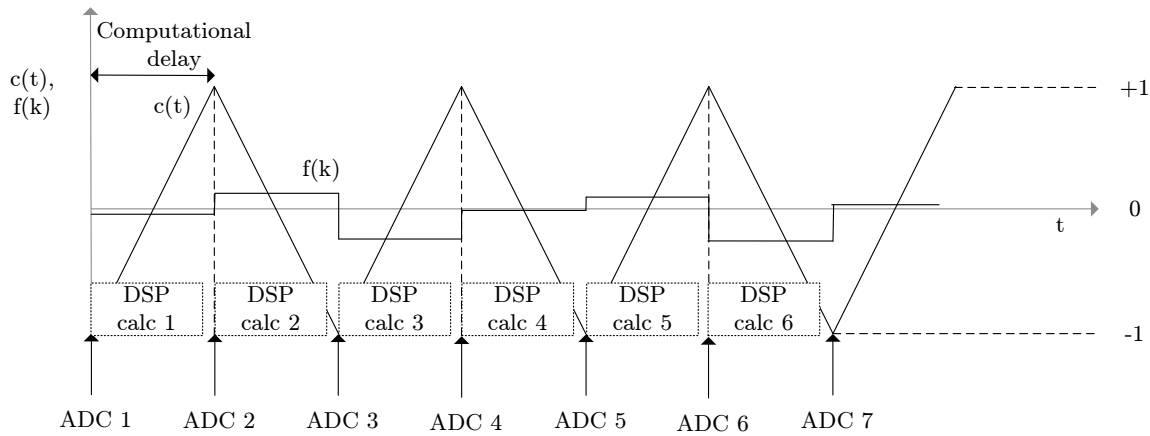


Figure 2.9: The effect of the computational delay on an asymmetrical sampled modulating signal $f(k)$.

The main non-linearity in most switch-mode controllers lies within the comparator of the pulse-width modulator [14]. This non-linear response of the pulse-width modulator affects the stability of a power converter; therefore it is important to be able to predict the non-linear behaviour of the pulse-width modulator.

Especially in PWM control loops it is found [1] that if an accurate small-signal model can be derived for a specific pulse-width modulator, the stability of the large-signal $f(t)$ can be predicted accurately. The large-signal is referred to as the steady-state input signal of the pulse-width modulator. When a small-disturbance signal $\tilde{f}(t)$ is superimposed onto the input of the pulse-width modulator it results in

$$\text{Input to the pulse-width modulator} = f(t) + \tilde{f}(t) \quad (2.3.1)$$

In current literature it is difficult to find a clear definition of exactly what a small-signal model is, but in [15] it is defined as a linearisation around a specific operating point.

2.3.1 Using a Small-Signal Model to Analyse Stability

The method involved in developing a small-signal model is best described using an example. In Figure 2.10a an example of an existing PWM current control loop is shown; also called the large-signal PWM control loop. When a small-perturbation signal $\tilde{i}^*(t)$ is superimposed onto the large-signal $i^*(t)$ the output of the compensator will also experience a small-disturbance signal, $f(t) + \tilde{f}(t)$, because of the continuity of the control loop, where the large-signal input of the pulse-width modulator is $f(t)$ and the small-disturbance signal is $\tilde{f}(t)$. The output current will also initially experience a small-disturbance, $i(t) + \tilde{i}(t)$.

The small-disturbance is therefore used as a way to characterise the behaviour of the pulse-width modulator model with respect to its normal operating point. Figure 2.10b shows the PWM control loop where the small-disturbance signal is added to the large-signal.

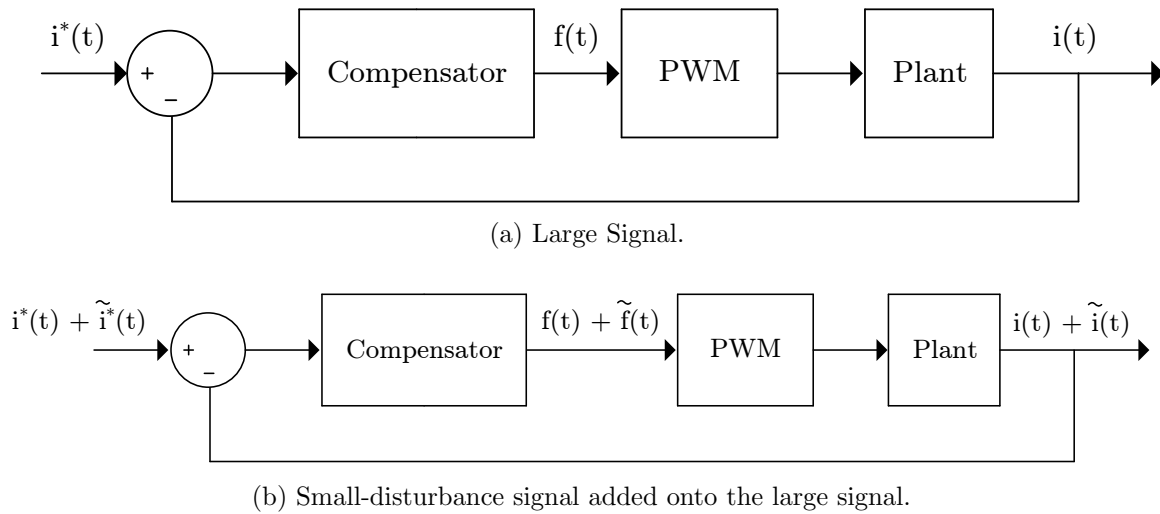


Figure 2.10: Example of an existing PWM control loop.

By means of block diagram manipulation, Figure 2.10b can be separated into two individual control loops, one for the small-disturbance (or also called the small-signal) and another for the large signal - see Figure 2.11. This shows that Figure 2.10b can be separated into the original non-linear PWM control loop (in Figure 2.10a) and a linear small-signal control loop. Since the small-signal model has been proven to be a linear representation of the large-signal model, the stability of the original PWM control loop can now be determined using the linear small-signal model. The small-signal model is therefore a way of analysing the stability of the large-signal.

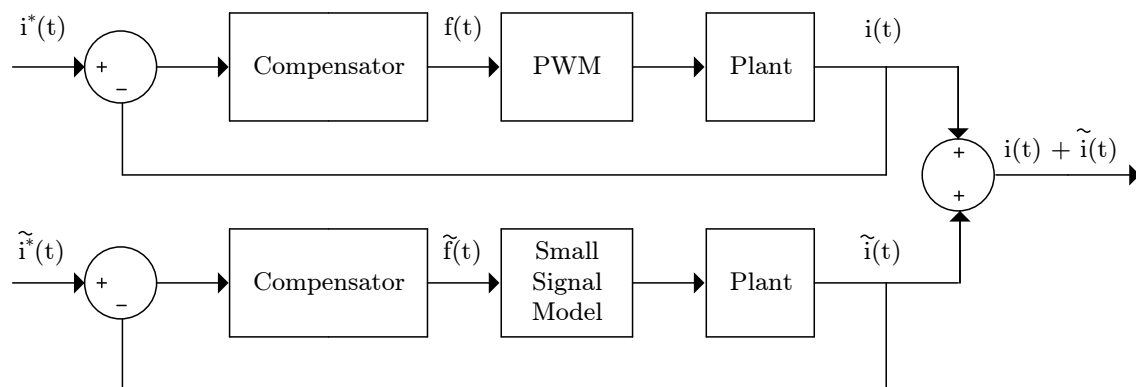


Figure 2.11: Representation of the large-signal PWM control loop and the linearised model.

By adding a small-disturbance signal to the reference input of the large-signal and analysing the behaviour of the control loop it is possible to determine whether a system is in a stable or unstable mode of operation. Since the large-signal model is a non-linear model it is very difficult to analyse its stability, although since the small-signal model is a linear representation of the large-signal model it would be easier to determine the stability margins of the system.

The advantage of being able to predict the stability margins accurately is that the optimal loop gain can be determined for a closed loop system. If the optimal loop gain is known, high performance control loops can be designed. In the following section 2.3.2 the derivation process involved to determine a small-signal model is discussed.

2.3.2 General Derivation of the Small-Signal Model of a Pulse-Width Modulator

Using the same principles discussed in the previous few paragraphs, a pulse-width modulator small-signal model can be derived for all the different types of pulse-width modulators discussed in section 2.1. Since the research in this thesis focuses on deriving a small-signal model for an asymmetrical RSPWM, the following description uses an asymmetrical regular sampled pulse-width modulator. A small-signal model of a single-edged oversampled PWM has already been derived in previous literature [1].

To derive the a small-signal model, a small-disturbance signal $\tilde{f}(t)$ is superimposed on the large-signal $f(t)$ of the pulse-width modulator. When only the large-signal is applied to the input of the pulse-width modulator and compared to the triangular carrier $c(t)$, the output of the comparator produces a pulse train $p(t)$, refer to Figure 2.12.

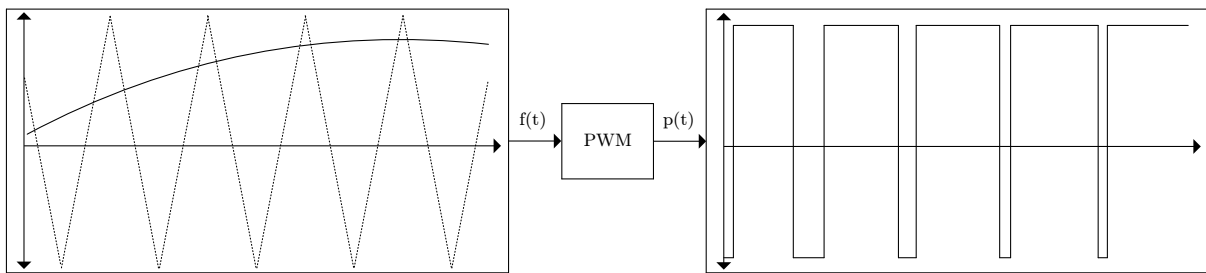


Figure 2.12: PWM generated by only the large-signal, $f(t)$.

When the small-disturbance signal $\tilde{f}(t)$ is added to the large-signal $f(t)$ and compared to the triangular carrier, as shown in Figure 2.13. This also produces a pulse train, $p(t) + \tilde{p}(t)$, in which the rising- as well as falling edges of the pulse train is slightly shifted in time.

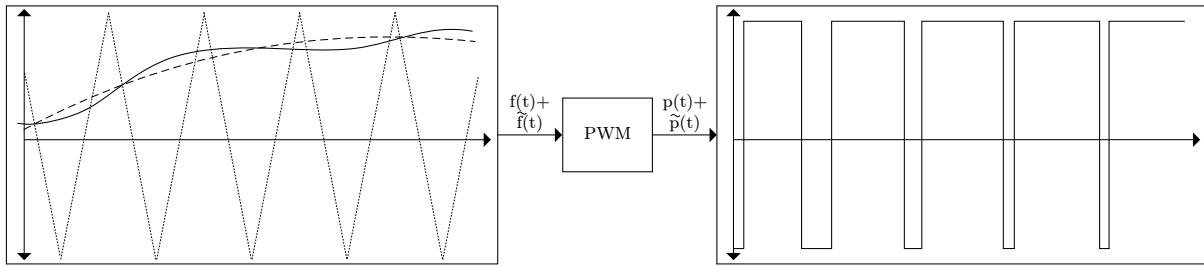
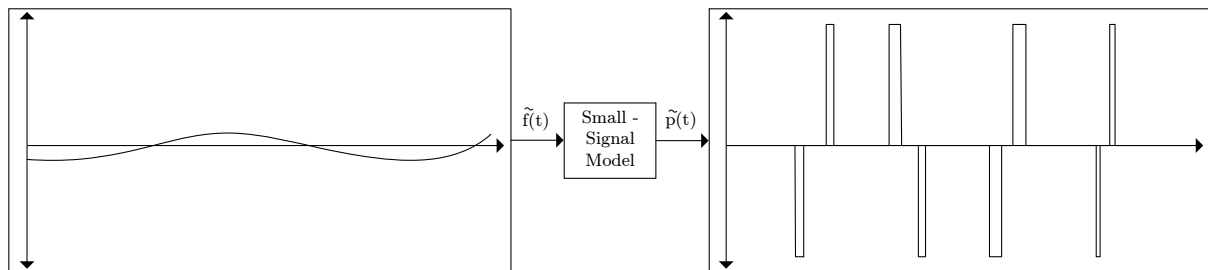


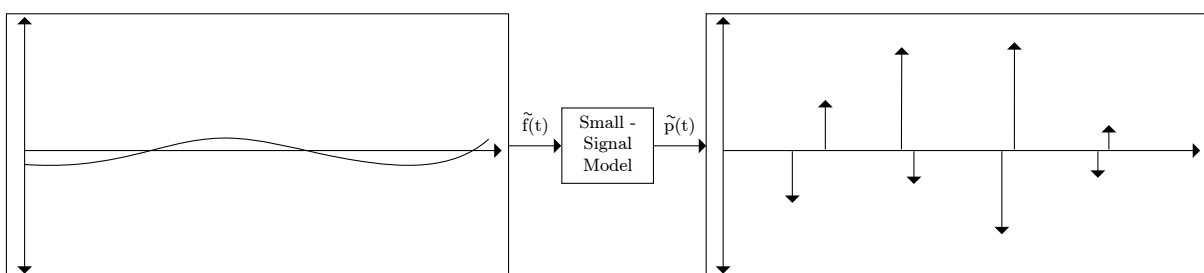
Figure 2.13: PWM generated by the superimposed signal, $f(t) + \tilde{f}(t)$.

When the pulse train, $p(t)$, generated by the large-signal is subtracted from the pulse train generated from the superimposed signal, $p(t) + \tilde{p}(t)$, it results in a series of narrow rectangular pulses $\tilde{p}(t)$. The narrow rectangular pulses can be approximated by a series of impulses (see Figure 2.14). This represents the small-signal model of the pulse-width modulator. To derive a mathematical model of the small-signal model there are two important factors to consider:

- the area of the narrow rectangular pulses to determine the weight of the impulses.
- the time the large-signal intersects the carrier waveform in to determine the position of the impulses.



(a) Small-disturbance signal applied to the input of the small-signal model, resulting in a series of narrow rectangular pulses.



(b) The series of rectangular pulses represented by impulses having a strength equal to the area of the rectangular pulses.

Figure 2.14: Representation of PWM small-signal model.

The small-signal model for an asymmetrical regular sampled pulse-width modulator is derived in Chapter 3.

2.4 Regular Sampled PWM Small-Signal Model

In an article [11] on the small-signal analysis of RSPWM, published in 2004 Laplace domain analysis was used to obtain a small-signal approximation transfer function for each of these pulse-width modulators mentioned in section 2.1.2 are derived. The equivalent model for the regular sampled pulse-width modulator suggested in Figure 2.3 is used together with the basic principles discussed in section 2.3.

2.4.1 Symmetrically Sampled Pulse-Width Modulators

A small-signal model for these pulse-width modulators is obtained when the large-signal $f(t)$ of the pulse-width modulator is superimposed with a small-disturbance signal $\tilde{f}(t)$, as represented in (2.3.1). In Figure 2.15 the modulating signal is shown where the small-disturbance signal $\tilde{f}(t)$ is superimposed on a large-signal $f(t)$, where the large-signal $f(t)$ is considered a constant as a first approximation. The small-disturbance is used to characterise the behaviour of the pulse-width modulators. By determining the effect which this small-disturbance $\tilde{f}(t)$ has on the output of the pulse-width modulator, the small-signal model can be obtained.

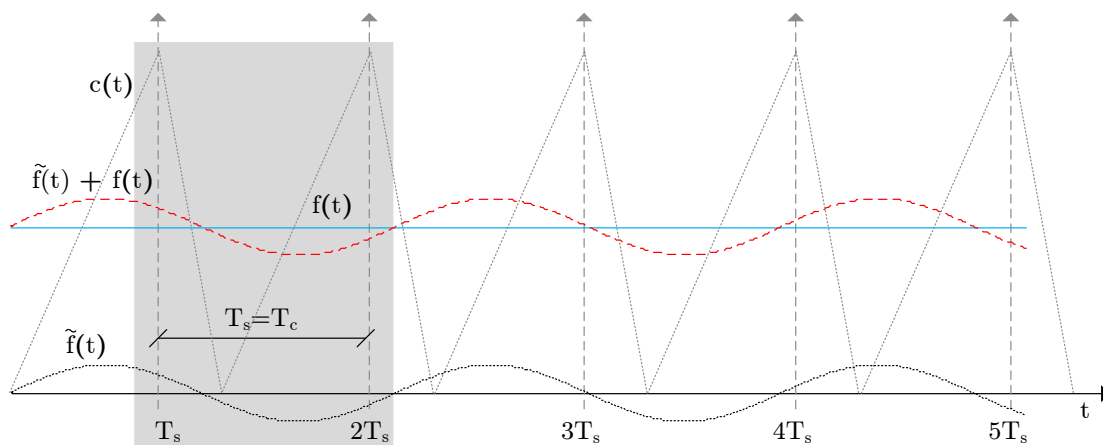


Figure 2.15: The modulating signal (red) consist of the a large-signal $f(t)$ (blue) and a small-disturbance signal $\tilde{f}(t)$ (black). For symmetrically sampled PWM the carrier period T_c is equal to the sampling period T_s .

At first the modulating signal is sampled at each sample period and passed through a zero-order hold, $f(k) + \tilde{f}(k)$, before it is compared to the generalised triangular carrier $c(t)$ in Figure 2.16. By generalised triangle carrier is meant that, depending on the value

of the ratio λ , it is possible to obtain either an end-of-on-time ($\lambda = 0$), the symmetric-on-time ($\lambda = \frac{1}{2}$) or the begin-of-on-time ($\lambda = 1$) pulse-width modulator. By using the triangular carrier representation a single output equation can be derived which represents the different types of symmetrically sampled pulse-width modulator (see Figure 2.4) small-signal models depending on the value of λ .

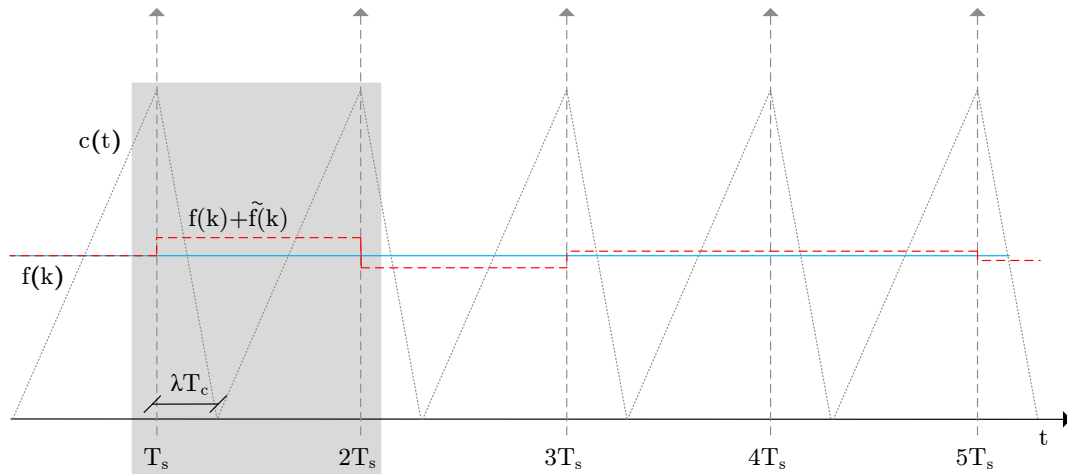


Figure 2.16: The modulating signal is sampled and hold constant for each sampling interval, resulting in $f(k) + \tilde{f}(k)$ (red). The large-signal $f(k)$ (blue) is only considered as a constant at first.

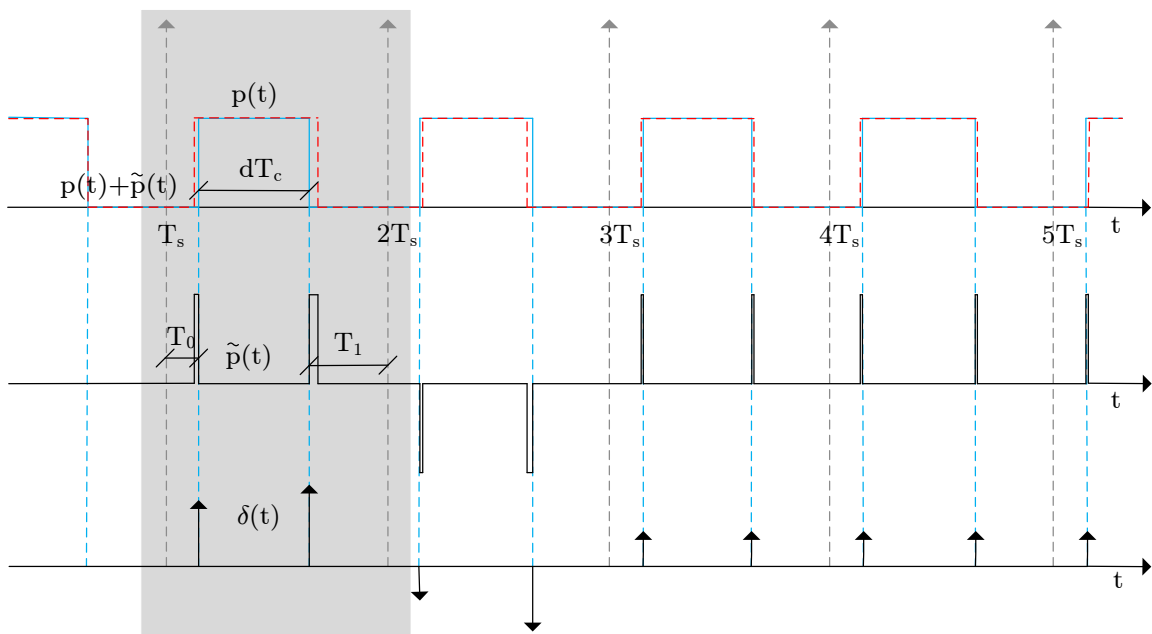


Figure 2.17: The PWM signals generated by the sample and hold modulating, $p(t) + \tilde{p}(t)$, (red) and the large-signal $p(t)$ (blue) is shown respectively. When the two PWM signals are subtracted from one another, it results in a series of narrow-rectangular pulses $\tilde{p}(t)$ which could be approximated by a series of impulses.

Figure 2.17 shows the result when the sample and hold signal is compared with the general triangular carrier $c(t)$, generating the PWM signal $p(t) + \tilde{p}(t)$, having a duty cycle d . Comparing only the large-signal $f(k)$ with the general triangle carrier $c(t)$ another PWM signal $p(t)$ is generated. The effect of the small-disturbance on the pulse-width modulator can then be determined by,

$$\text{Series of narrow rectangular pulses} = \left(p(t) + \tilde{p}(t) \right) - p(t) = \tilde{p}(t) \quad (2.4.1)$$

Equation (2.4.1) gives a series of narrow-rectangular pulses $\tilde{p}(t)$ which could be approximated by a series of impulses $\delta(t)$. The impulses represent the small-signal model of an symmetrically sampled pulse-width modulator. From Figure 2.17 we can see that the impulses occur when the large-signal $f(k)$ intersects the carrier signal $c(t)$. From the highlighted area, we can see that two impulses are generated over the one sample period T_s . The first impulse is generated during the falling edge of the general triangle carrier at $t = T_0$ and the second impulse is generated at $t = T_s - T_1$.

The weight of the impulses is equal to the area of each of the narrow-rectangular pulses. The area of rectangular pulses is dependent on the gradient of the line between the intersection of the large-signal with the carrier signal and the intersection of the sample and hold modulating signal with the carrier signal. In Figure 2.18 the gradients of the falling- and rising edges of the carrier signal is defined by m_1 and m_2 , respectively.

The gradient for the falling edge m_1 of the carrier signal is given by,

$$m_1 = \frac{2}{\lambda T_c} = \frac{\tilde{f}(k)}{\Delta T_1} \quad (2.4.2)$$

where $\tilde{f}(k)$ is value of the small-disturbance signal at the time instant when the large-signal $f(k)$ intersects the carrier signal $c(t)$.

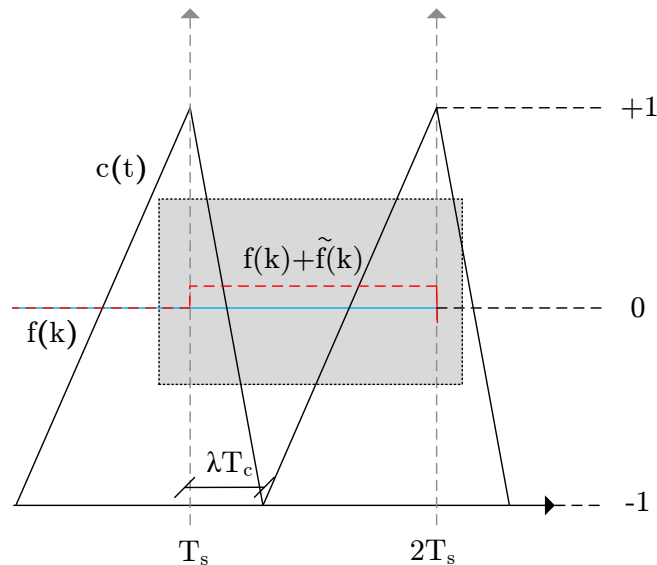
Rearranging (2.4.2) the width of the rectangular pulse ΔT_1 is given by,

$$\Delta T_1 = \frac{\lambda T_c}{2} \tilde{f}(k) \quad (2.4.3)$$

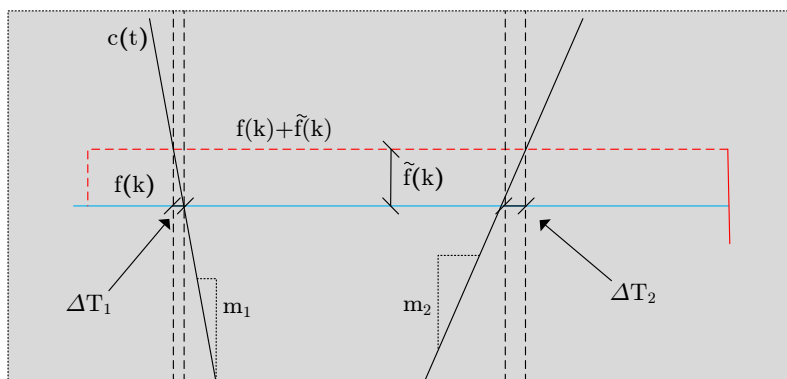
The gradient for the rising edge m_2 of the carrier signal is given by,

$$m_2 = \frac{2}{(1 - \lambda) T_c} = \frac{\tilde{f}(k)}{\Delta T_2} \quad (2.4.4)$$

Rearranging (2.4.2) the width of the rectangular pulse ΔT_2 is given by,



(a) The intersection of the sample and hold modulating signal (red) and the large-signal $f(k)$ (blue) with the carrier signal $c(t)$.



(b) Zoomed views of the intersections. The width of the narrow-rectangular pulse during the falling- and rising edge is ΔT_1 and ΔT_2 respectively. The gradients of the falling- and rising edges of the carrier are given by m_1 and m_2 , respectively.

Figure 2.18: Zoomed view of a symmetrically sampled pulse-width modulated signal.

$$\Delta T_2 = \frac{(1 - \lambda)T_c}{2} \tilde{f}(k) \quad (2.4.5)$$

Multiplying (2.4.3) and (2.4.5) by two for the height of carrier signal, the area of the rectangular pulses can be described by (2.4.6) and (2.4.7). From Figure 2.18 it's clear that the value of the small-disturbance signal $\tilde{f}(k)$ stays constant during the one sampling interval T_s .

For the falling edge of general triangle carrier the area A_1 of the pulse is given by,

$$A_1 = \lambda T_s \tilde{f}(k) \quad (2.4.6)$$

For the rising edge of general triangle carrier the area A_2 of the pulse is given by,

$$A_2 = (1 - \lambda)T_s\tilde{f}(k) \quad (2.4.7)$$

With the position of the impulses and the weight of the impulses determined, the small-signal output for the different symmetrically sampled pulse-width modulators can be described as follows:

- Begin-of-on-time pulse-width modulator:

$$\tilde{p}(t) = T_s\tilde{f}(k)\delta(t - (1 - d)T_s) \quad (2.4.8)$$

where $\lambda = 1$, $T_0 = (1 - d)T_s$ and $T_1 = 0$.

- End-of-on-time pulse-width modulator:

$$\tilde{p}(t) = T_s\tilde{f}(k)\delta(t - dT_s) \quad (2.4.9)$$

where $\lambda = 0$, $T_1 = (1 - d)T_s$ and $T_0 = 0$.

- Symmetric-on-time pulse-width modulator:

$$\tilde{p}(t) = \frac{T_s}{2}\tilde{f}(k)\delta\left(t - \frac{(1 - d)T_s}{2}\right) + \frac{T_s}{2}\tilde{f}(k)\delta\left(t - \frac{(1 + d)T_s}{2}\right) \quad (2.4.10)$$

where $\lambda = \frac{1}{2}$ and $T_0 = T_1 = \frac{(1-d)T_s}{2}$.

Using similar analysis, the small-signal output of the symmetric-off-time pulse-width modulator is given by

$$\tilde{p}(t) = \frac{T_s}{2}\tilde{f}(k)\delta\left(t - \frac{dT_s}{2}\right) + \frac{T_s}{2}\tilde{f}(k)\delta\left(t - \frac{(2 - d)T_s}{2}\right) \quad (2.4.11)$$

These continuous-time signals obtained for the symmetrically regular sampled pulse-width modulators can now be transformed to equivalent discrete-time signals. The main focus of this research is however, to obtain a discrete-time signal for asymmetrical RSPWM.

2.4.2 Asymmetrical Sampled Pulse-Width Modulators

Similarly to the symmetrically sampled pulse-width modulators derivation, a small-signal output equation is derived for the asymmetrical sampled pulse-width modulator. In Figure 2.19 the large-signal $f(t)$ is shown with the small-disturbance $\tilde{f}(t)$ superimposed onto it, together they form the modulating input signal. The difficulty of the asymmetrical sampled pulse-width modulator is that the modulating signal is sampled and hold twice during one carrier period. Figure 2.20 shows the sample and hold modulating signal, $f(k) + \tilde{f}(k)$.

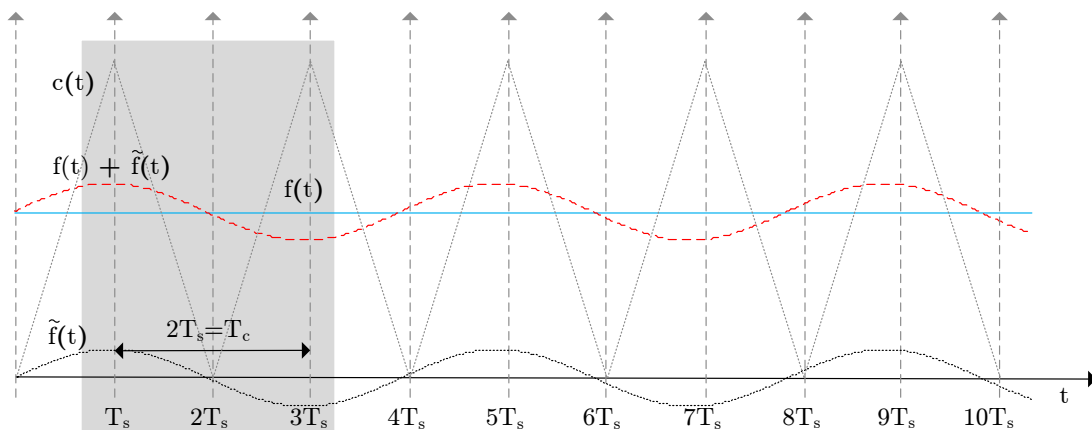


Figure 2.19: The modulating signal (red) consist of a large-signal $f(t)$ (blue) and a superimposed small-disturbance signal $\tilde{f}(t)$ (black). For asymmetrical sampled PWM the carrier frequency f_c is equal two times sampling frequency f_s .

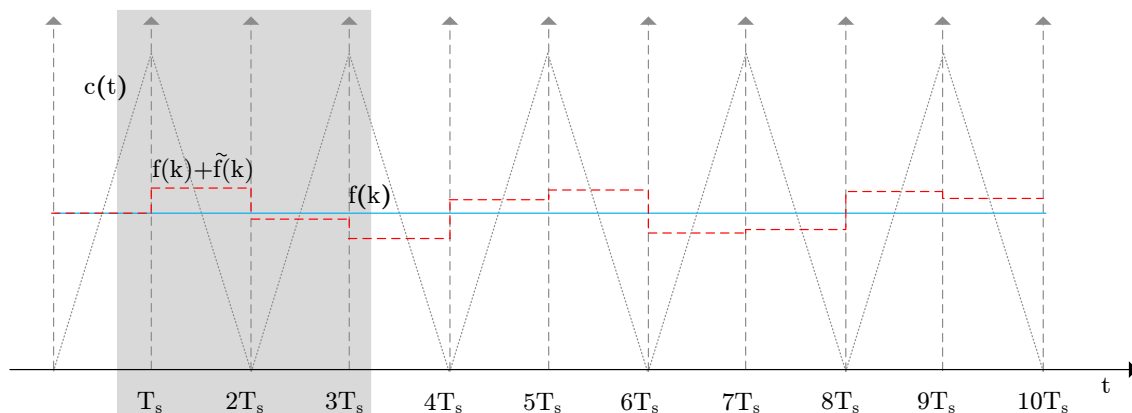


Figure 2.20: The modulating signal is sampled and hold constant for each sampling interval, resulting in, $f(k) + \tilde{f}(k)$ (red). The large-signal $f(k)$ (blue) is only considered as a constant for now.

However, since the modulating signal is now sampled at each half period of the carrier signal, the small-disturbance signals $\tilde{f}(k)$ amplitude changes for each sample period. Al-

though the large-signal $f(k)$ is constant for each sample interval the weight of the impulses occurring at the rising- and falling edges of the carrier period differs. This is caused by the fact that the small-disturbance signal amplitudes are different for each sample period. In Figure 2.20 this effect can be seen. Unlike with symmetric-on-time- and symmetric-off-time pulse-width modulators where the sample and hold modulating signal is constant over the full carrier period. This complicates the derivation of the small-signal output equation of the pulse-width modulator.

Two impulses are generated during the carrier interval T_c . Figure 2.21 shows that the impulses are generated at the falling edge of the carrier signal at $t = T_0$ and during the rising edge of the carrier signal at $t = T_c - T_1$

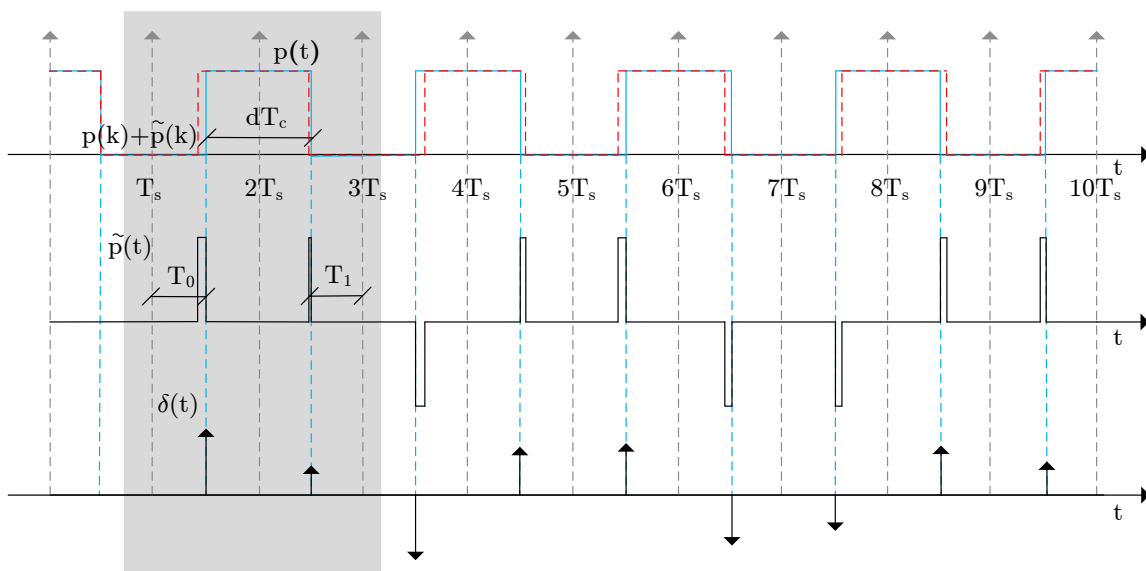


Figure 2.21: The PWM signals generated by the sample and hold modulating signal $p(t) + \tilde{p}(t)$, (red) and the large-signal $p(t)$ (blue) is shown respectively. When the two PWM signals are subtracted from one another, it results in a series of narrow-rectangular pulses $\tilde{p}(t)$ which could be approximated by a series of impulses $\delta(t)$.

Again the weight of the impulses is determined by the area of the narrow-rectangular pulses. If λ in Figure 2.18 is equal to $\frac{1}{2}$ the area of the rectangular pulses is determined by (2.4.16) and (2.4.17).

The gradient for the falling edge m_1 of the carrier signal is given by,

$$m_1 = \frac{2}{T_s} = \frac{\tilde{f}_1(k)}{\Delta T_1} \quad (2.4.12)$$

where $\tilde{f}_1(k)$ is the value of the small-disturbance signal the instant the large-signal $f(k)$ intersects the carrier signal $c(t)$ during the falling edge of the carrier.

Rearranging (2.4.12) the width of the rectangular pulse ΔT_1 is given by,

$$\Delta T_1 = \frac{T_s}{2} \tilde{f}_1(k) \quad (2.4.13)$$

The gradient for the rising edge m_2 of the carrier signal is defined by,

$$m_2 = \frac{2}{T_s} = \frac{\tilde{f}_2(k)}{\Delta T_2} \quad (2.4.14)$$

where $\tilde{f}_2(k)$ is the value of the small-disturbance signal the instant the large-signal $f(k)$ intersects the carrier signal $c(t)$ during the rising edge of the carrier.

Rearranging (2.4.14) the width of the rectangular pulse ΔT_2 is given by,

$$\Delta T_2 = \frac{T_s}{2} \tilde{f}_2(k) \quad (2.4.15)$$

Multiplying (2.4.13) and (2.4.15) by two for the height of carrier signal, the area of the rectangular pulses can be described by (2.4.16) and (2.4.17).

For the falling edge of triangle carrier:

$$A_1 = T_s \tilde{f}_1(k) \quad (2.4.16)$$

For the rising edge of triangle carrier:

$$A_2 = T_s \tilde{f}_2(k) \quad (2.4.17)$$

Now that the position of the impulses and the weight of the impulses have been determined, the small-signal output for the asymmetrical sampled pulse-width modulators can be described as follows:

- For the falling edge of triangle carrier:

$$\tilde{p}_1(t) = T_s \tilde{f}_1(k) \delta(t - (1 - d)T_s) \quad (2.4.18)$$

- For the rising edge of triangle carrier:

$$\tilde{p}_2(t) = T_s \tilde{f}_2(k) \delta(t - (1 + d)T_s) \quad (2.4.19)$$

Equations (2.4.18) and (2.4.19) show that the small-signal output of the asymmetrical sampled pulse-width modulator is described by two equations, one for the falling edge of the carrier signal and another one for the rising edge of the carrier signal. In the following section a Laplace analysis is used to find a solution for the transfer function of an asymmetrical sampled pulse-width modulator.

However, the moment the large-signal is not a constant value the duty cycle value needs to be updated twice over each switching period. The position between the impulses are therefore not necessarily equidistantly spaced. As the duty cycle changes so does the impulse position changes. For example, during the rising edge of the triangular carrier the position of the impulse is defined at $d_1 \frac{T_c}{2}$, where d_1 is the duty cycle dependent on the value of the large-signal sampled at the rising edge of the carrier signal. During the falling edge of the triangular carrier signal the impulse is at $(1 - d_2) \frac{T_c}{2}$, where d_2 is the duty cycle dependent on the value of the large-signal sampled at the falling edge of the carrier signal.

In chapter 3 this phenomenon is included and a state space model is derived for an asymmetrical regular sampled pulse-width modulator.

2.4.3 Zero-Order Hold Approximation for Regular Sampled PWM Small-Signal Model

In [11] the transfer functions are derived for each of the pulse-width modulators, using a small-signal approximation. The transfer functions are summarized in Table 2.1. The asymmetrical sampled pulse-width modulator transfer function is approximated by the symmetrically sampled pulse-width modulator transfer function in [16] and results in

$$PWM(s) = \frac{1}{2} \left(e^{-s(1-d)\frac{T_c}{2}} + e^{-s(1+d)\frac{T_c}{2}} \right) \quad (2.4.20)$$

where T_c is the switching period of the asymmetrical sampled pulse-width modulator.

Applying Euler's formula to (2.4.20), results in

$$PWM(s) = e^{-s\frac{T_c}{2}} \cos\left(w\frac{T_c}{2}d\right) \quad (2.4.21)$$

If the controller bandwidth is limited to well below the modulation frequency, the gain term can actually be approximated by unity, independent of the duty cycle d [6], so that (2.4.21) simplifies to

$$PWM(s) \approx e^{-s\frac{T_c}{2}} \quad (2.4.22)$$

According to (2.4.22), the transfer function $PWM(s)$ can be modelled as a pure, half modulation period delay. This corresponds to the continuous-time model of the zero-order hold function. This simplified model of the pulse-width modulator can be used for different modulator configurations, however this would represent a coarser approximation [6].

In [16] this ZOH model of the $PWM(s)$ is used to design a discrete-time model of a current regulated three-phase inverter. In chapter 5 an investigation is done on the accuracy of this ZOH model when predicting the stability of a system.

Table 2.1: Laplace-domain transfer functions for regular sampled pulse-width modulators

	$PWM(s)$
end-of-on-time	e^{-sdT_c}
begin-of-on-time	$e^{-s(1-d)T_c}$
symmetric-of-on-time	$\frac{1}{2}(e^{-s\frac{(1-d)T_c}{2}} + e^{-s\frac{(1+d)T_c}{2}})$
symmetric-of-off-time	$\frac{1}{2}(e^{-s\frac{dT_c}{2}} + e^{-s\frac{(2-d)T_c}{2}})$
asymmetrical sampled	$\frac{1}{2}(e^{-s(1-d)T_c} + e^{-sdT_c})$

2.5 Naturally Sampled PWM Small-Signal Model

In digital control the performance of RSPWM control is limited as result of additional delays and the non-ideal effects. The additional delays - for example the transport- and computational delay - reduces the control bandwidth leading to poor transient responses. In an article [1] published in 2012 it was shown that a naturally sampled PWM waveform is achieved with oversampling, increasing the controller bandwidth and improving the dynamic response [1]. Oversampling is achieved using a Field Programmable Array (FPGA), where the output signal is sampled at a much higher frequency than the switching frequency. This emulates the behaviour of an analog control in the digital domain [1].

In the design of current regulators it is useful to know the maximum open loop gain over an extended control bandwidth to improve the dynamic performance of these regulators. In oversampled control loops it is possible to minimize the effect of transport delays, since sampling occurs at a much higher rate than the switching frequency. In [1] a small-signal

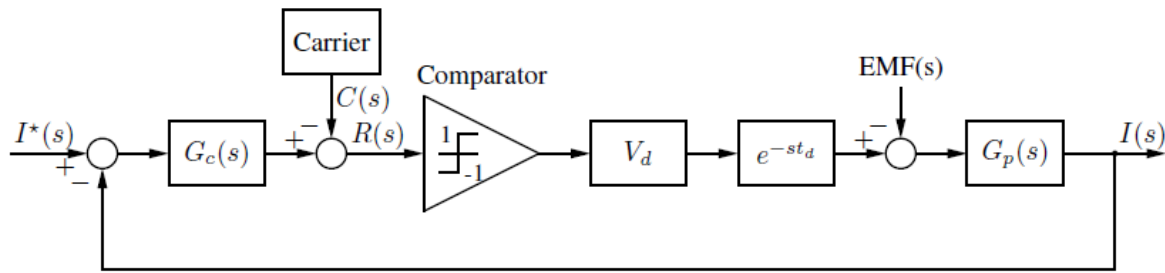


Figure 2.22: PWM current regulator loop (taken from [1]).

model is derived for a naturally-sampled pulse-width modulator, that includes the effect of sampling of the PWM in more detail.

In the small-signal model of a pulse-width modulator the operation of the comparators are characterized by samples at each of the zero-crossings. The zero-crossings occurs when the modulated signal intersects the carrier. For example, using a sawtooth carrier, the sample frequency is approximately equal to the switching frequency. Since the modulated signal consist of a small-signal and a large-signal, the output of the comparator results in a series of narrow rectangular pulses, similar to what was discussed in section 2.4. An additional small-signal gain K_{ss} , equal to the area of each narrow rectangular pulse is included and cascaded to an impulse generator.

The small-signal model of the comparator is modelled as a sampling operation followed by an impulse generator with a small-signal gain K_{ss} . The small-signal gain K_{ss} is derived in [14] and given by

$$K_{ss} = \frac{2f_s}{|\dot{r}_0|} \quad (2.5.1)$$

where r_0 is the slope of the comparator input signal when it intersects with the carrier.

In Figure 2.22 a large-signal PWM current regulator example is shown, where $I^*(s)$ is the reference current, $G_c(s)$ is the analog current regulator transfer function, $C(s)$ is the carrier, $EMF(s)$ is the load back EMF and $G_p(s)$ is the transfer function for the plant. The combined value of the transport delays in the control loop is represented by the delay t_d . In Figure 2.23 the PWM operation is replaced by its small-signal model representation.

The sampling process of the pulse-width modulator creates a discrete-time domain area between the ideal sampler and the impulse generator in Figure 2.23. The PWM behaviour is characterised by the surrounding circuit from the point of view of the discrete-time domain component [1].

When the open loop transfer function is transformed to the z-domain, using the impulse invariance method, it is possible to analyse the stability of the loop very accurately. The

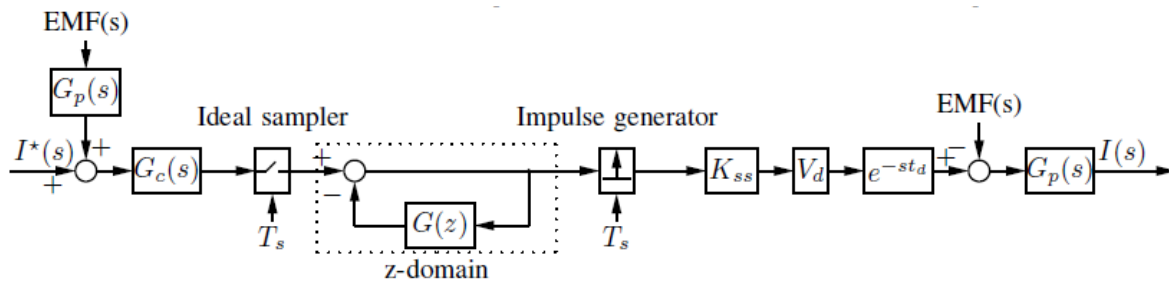


Figure 2.23: Pulse-width modulator modelled in the z-domain (taken from [1]).

regulator then is designed directly in the z-domain, using a root-locus approach, which guarantees stability. The design process is discussed in detail in [1].

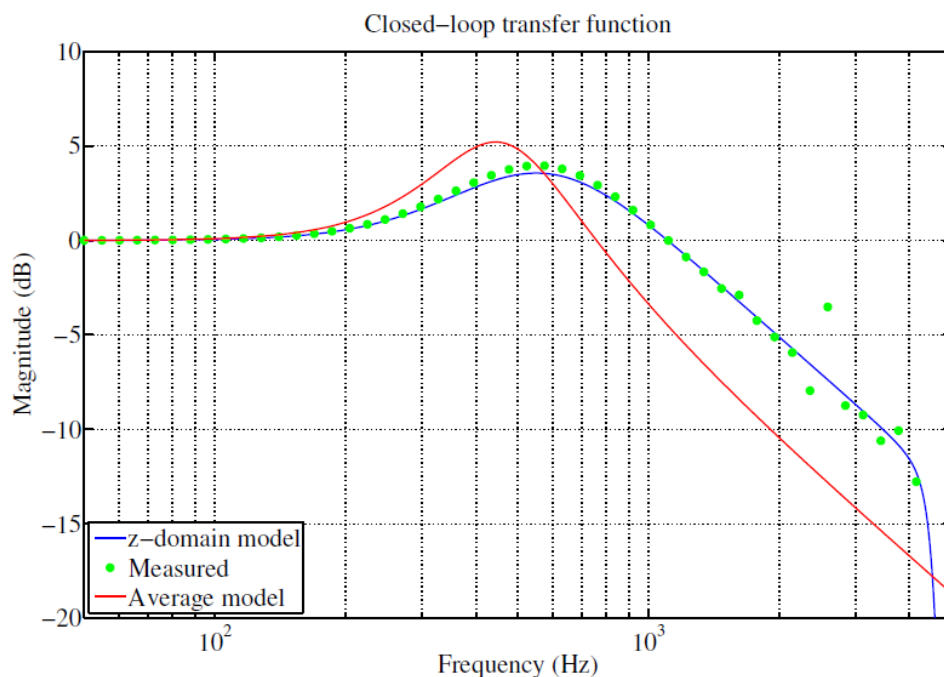


Figure 2.24: Closed loop response (taken from [1]).

Figure 2.24 shows the accuracy of predicting the closed loop response of the design method directly in the z-domain towards the original average model, where the PWM model behaviour is only expressed as a gain block. At high frequencies the average model's accuracy is not sufficient, necessitating the use of small-signal models of PWM for high-performance control loops.

2.6 Non-Linear Behaviour of Power Electronic Systems

It is well known that PWM is a non-linear process. The conventional approach generally ignores non-linear effects, and can sometimes mislead the designer into thinking a circuit will perform acceptably when in practice it will not [4]. This non-linearity may cause instability to occur in a control loop - requiring complicated analysis. Using sophisticated mathematical tools more accurate models could be derived for the different SMPS. Together with the accurate models the stability margins of a system can be predicted more accurately, leading to better performance controllers.

In terms of small-signal models of pulse-width modulators, the stability is predicted using small-disturbance signals together with the input large signal and then to observe the output. If the output signal deviates by only a small amount and returns to the fundamental value, the system is defined a stable system. However, if the output deviates and does not return to the fundamental output signal, the system is considered as an unstable system.

The small-signal model is therefore only a method to analyse the stability of the actual system. However, if the stability could be analysed very accurately it could provide considerable advantages for the design of an optimal controller.

In terms of a state space system, a system is defined to be stable if the initial state is close to the equilibrium and leads to a state which continues to be permanently close to the equilibrium point [2]. This could be better described using limit cycles, where a limit cycle is an isolated periodic solution of an autonomous system, represented in the phase plane by an isolated closed path [2]. If any of the nearby paths spiral into the a limit cycle the system is stable, in contrast if the any of the paths spirals away from the closed path it results in an unstable system. Figure 2.25 shows an example where two separate phase paths represents a stable limit cycle. The first path approaches the limit cycle from the a very small initial phase path value and another approaches it from a big initial phase path. However, if both of these phase paths converge towards the stable limit cycle, it usually is an indication of a stable system.

The theory behind limit cycles can be extended for small-signal models of PWM power converters, where the small-signal model can be seen as an linearisation of a system around it's equilibrium point. When a small deviation is applied near the equilibrium state of the system, the system will return to its equilibrium state if the deviation is small. On the other hand, if the deviation is too large the system will deviate further and become unstable. The deviation could be due to any spurious parameter change experienced by

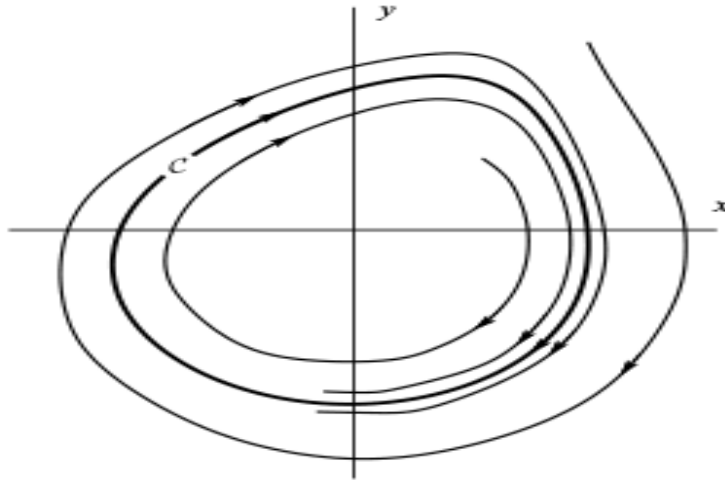


Figure 2.25: An example of a stable limit cycle (taken from [2]).

the system. When this deviation or parameter change passes through a critical value, a sudden change in the system response may occur. This critical value is also known as the bifurcation point and such a sudden change in the systems behaviour is usually an indication of a change in stability. This theory is extended to bifurcation models to better visualize these concepts.

2.6.1 Bifurcation Models

The concept of bifurcation theory was only recently introduced into power electronics to enable the analysis of non-linear phenomena existing in SMPS. In [4], a bifurcation is defined as a qualitative change in the dynamics which occurs as a system parameter is changed. A SMPS can be described as an dynamic system in terms of its discrete-time domain as,

$$\mathbf{x}_{n+1} = \mathbf{f}(\mathbf{x}_n, r) \quad (2.6.1)$$

where \mathbf{x}_n is the state variable vector, \mathbf{f} is the mapping function and r is the external parameter vector. By determining the eigenvalues of the discrete-time system, the type of instability occurrence can be identified depending on the value when they cross the unity circle. This may be classified into three different types of bifurcations shown in Figure 2.26.

Depending on the value of the eigenvalues, or more specifically the value of the closed loop poles, the type of bifurcation can be identified. Where Figure 2.26a refers to a period-doubling bifurcation; Figure 2.26b to a hopf bifurcation and Figure 2.26c to a saddle-node bifurcation.

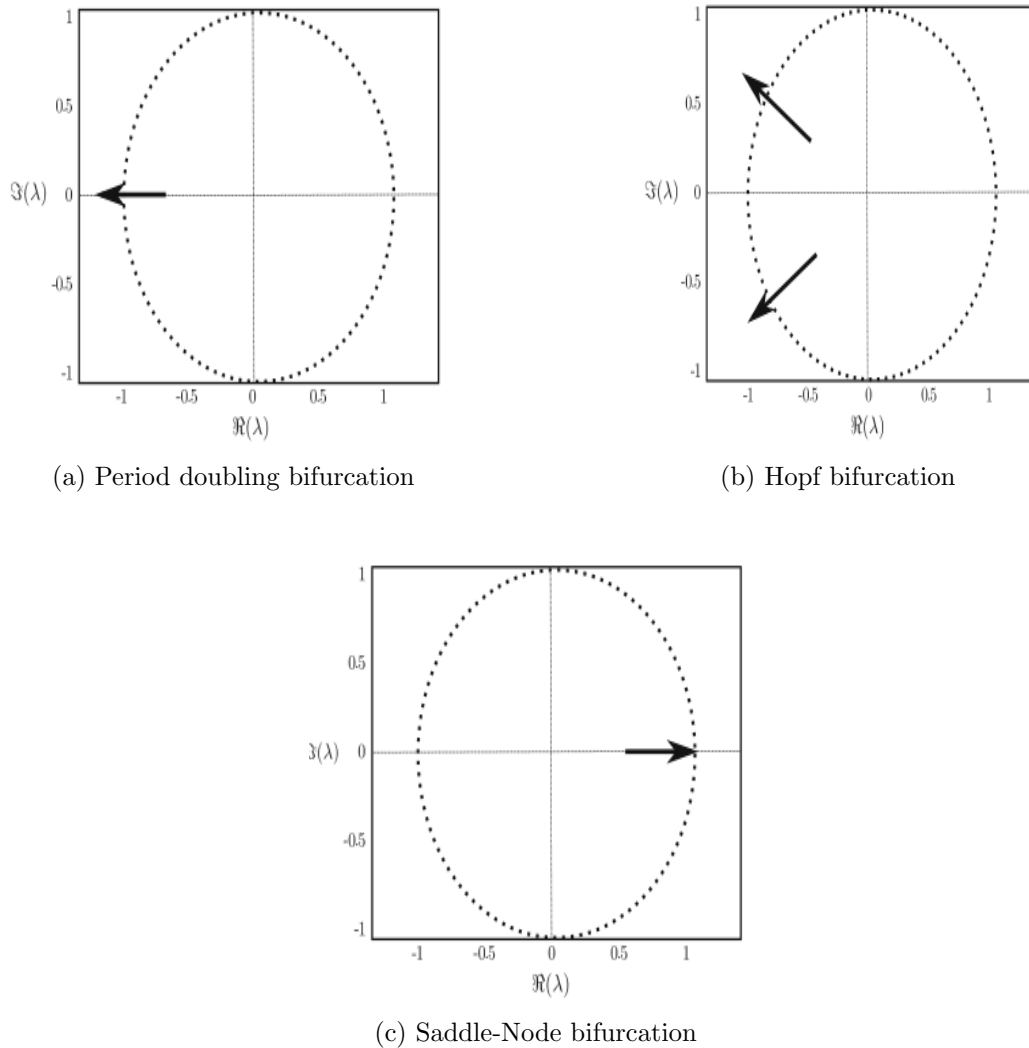


Figure 2.26: The movement of closed loop poles indicates the type of bifurcation (taken from [3]).

When parameter values are changed, the originally intended design operating point experience a change. This change could be visualised, using a bifurcation diagram. Figure 2.27 shows an example of such a bifurcation diagram, where the state vector x is observed at each sample instant against the change in parameter value r . The system initially operates in the period-1 region, where there is only one sample corresponding to the specific parameter value.

However at $r \approx 3$, the system starts to operate in the period-2 region(also known as period-doubling), where there are two samples for the specific parameter value. When the system experiences an infinite of samples for instance at $r \approx 3.5$, the system is said to behave chaotically. The chaotic behaviour is usually an indication of the PWM control loop that is in saturation.

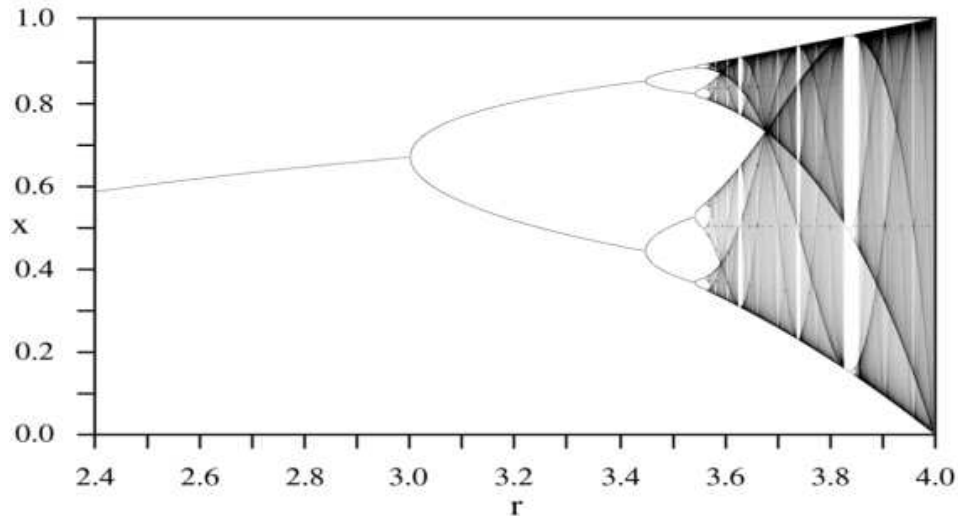


Figure 2.27: Example of bifurcation diagram (taken from [4]).

2.7 Summary

In this chapter an overview is given with a view to explaining the relationship between the NSPWM and RSPWM. A brief discussion of the most common delays in a PWM control loop is presented to describe the effect these delays could have on the stability of a PWM control loop in terms of the phase margin. A closer look is also taken to see how the non-linear behaviour of the pulse-width modulators can be represented by a linear pulse-width modulator small-signal model. The mathematical process involved in deriving pulse-width modulator small-signal models are discussed for different types of regular sampled pulse-width modulators. Also the methods used to derive these small-signal models in previous literature are discussed. Examples of both NSPWM and RSPWM small-signal models are shown.

Because of the non-linearity involved in a PWM control loop, complicated analysis is necessary to determine the stability margins. The concepts of bifurcation diagrams are introduced to be used to predict the stability of the PWM control loops for a practical system.

Chapter 3

Small-Signal Model of Asymmetrical Regular Sampled PWM

3.1 Introduction

Small-signal model analysis is used to investigate the stability of a control loop by superimposing a small-disturbance into the control loop to see if it converges back to a stable state or whether it diverges to an unstable state. Such a control loop is shown in Figure 3.1.

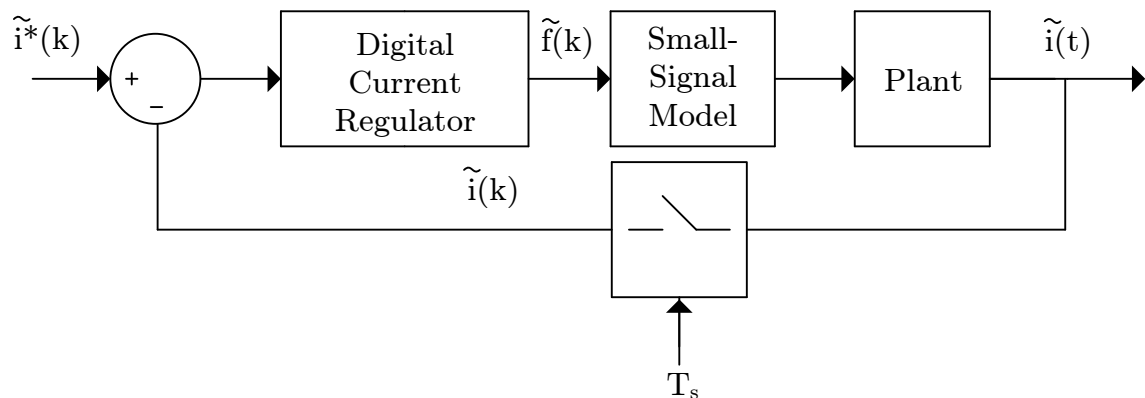


Figure 3.1: Small-signal model representative PWM control loop.

To design a digital current regulator the relationship between the z-domain and the s-domain is important for the design of optimal controllers. If an accurate discrete state space model can be derived for the relationship between the input of the small-signal model $\tilde{f}(k)$ and output of the sampler $\tilde{i}(k)$ in Figure 3.1, it would be possible to predict the stability for the large-signal control loop with high accuracy. Deriving differential equations for the plant of the system, the discrete-time state space model becomes,

$$\tilde{i}(k+1) = \mathbf{F}\tilde{i}(k) + \mathbf{G}\tilde{f}(k) \quad (3.1.1)$$

where, \mathbf{F} is the state matrix and \mathbf{G} is the control input matrix.

The advantage of having a precise small-signal model is that the stability margins of the large-signal control loop can be determined. Once the stability margins of a system is known, the designer can proceed with the design of the optimal current regulator.

This chapter focuses on the mathematical derivation process involved in deriving a small-signal model for an asymmetrical regular sampled PWM control loop. A discrete-time equivalent state space model is obtained for the small-signal model of both a single-phase and three-phase series RL-load.

3.2 Background of the Small-Signal Model of Asymmetrical Regular Sampled PWM

In section 2.4 a small-signal model transfer function has been derived for an asymmetrical regular sampled pulse-width modulator. A similar approach will be used for the derivation of the discrete-time state space model where the duty cycle is updated for each period of the sampling period T_s , at each of the maxima and minima peaks of the triangular carrier. When a small-disturbance is initially added onto the large-signal, impulses are generated at each interval of the sample period; the location of the impulses will, however, depend on the value of the duty cycle.

In research reported in [11] the large-signal was accepted to be a constant signal, resulting in a constant duty cycle. The location of the impulses therefore does not change every sample period. However, in actual fact the duty cycle is varies for the first and second halves of the switching period. This fact initiated our research to derive an equation for the small-signal model where the effect of the change in duty cycle is considered.

3.2.1 Location of Impulses

An impulse is generated at each instant where the large-signal intersects the carrier signal, thus at the rising edge of the triangular carrier as well as- the falling edge of the triangular carrier. However, according to Figure 3.2, if the large-signal is considered to change at each sample period, the duty cycle also changes and therefore the impulse positions as well. To allow for this change of the impulse positions it is necessary to use dummy state variables.

Two state space variables are used to describe the position of the impulses, $\tilde{i}_1(k)$ to describe the position of the impulse during the rising edge of the triangular carrier; $\tilde{i}_2(k)$ to describe position of the impulse during the falling edge of the triangular carrier. However, the initial condition for the state variable $\tilde{i}_2(k)$ only begins after one sample period. A sample instant k is defined for the interval of the switching period T_c .

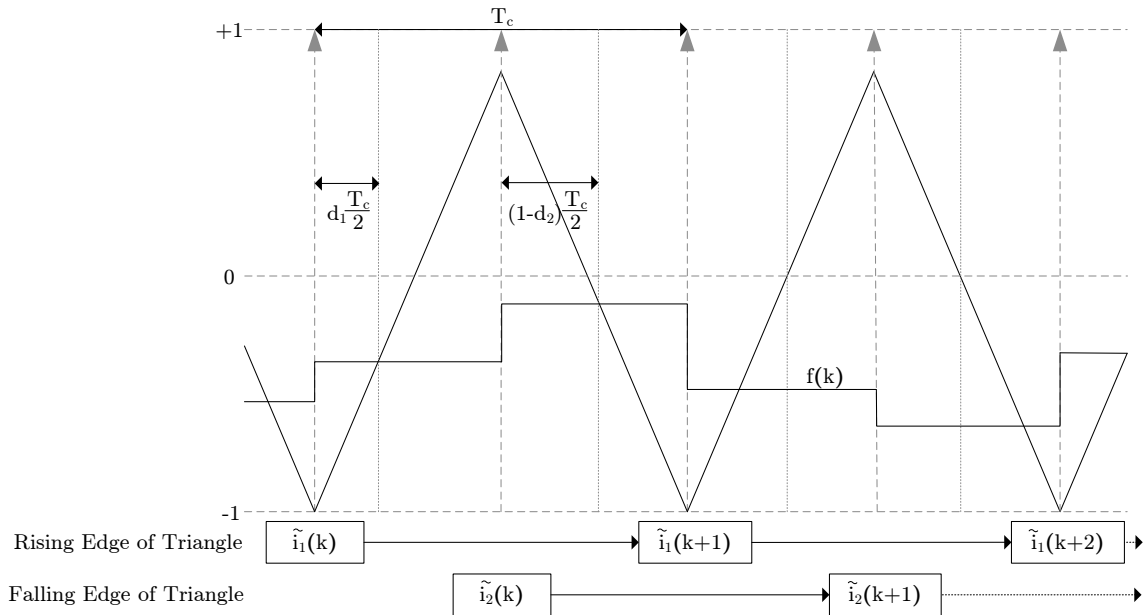


Figure 3.2: Location of impulses when the large-signal intersects the triangular carrier signal.

This strategy of using two state variables prevents the problem from becoming non-linear. The relationship between the input to the small-signal model and the output of the sampler can now be modelled using two separate discrete-time state space equations, which yields:

$$\tilde{i}_1(k+1) = F_1 \tilde{i}_2(k) + G_1 \tilde{f}_2(k) \quad (3.2.1a)$$

$$\tilde{i}_2(k+1) = F_2 \tilde{i}_1(k+1) + G_2 \tilde{f}_1(k+1) \quad (3.2.1b)$$

Equation (3.2.1a), describing the rising edge of the triangular carrier, shows that the next sample instant $\tilde{i}_1(k+1)$ is determined by the current sample $\tilde{i}_2(k)$, the value sampled at the maximum peak of the triangle, and the input $\tilde{f}_2(k)$ representing the impulse generated during the falling edge of the triangle carrier. On the contrary, equation 3.2.1b, describing the falling edge of the triangle carrier, shows that the next sample instant $\tilde{i}_2(k+1)$ is determined by the current sample $\tilde{i}_1(k+1)$, the value being sampled at the minimum of

the triangle, and the input $\tilde{f}_1(k + 1)$ representing the impulse generated during the rising edge of the triangle carrier.

For example at $k = 0$:

$$\tilde{i}_1(1) = F_1\tilde{i}_2(0) + G_1\tilde{f}_2(0) \tag{3.2.2a}$$

$$\tilde{i}_2(1) = F_2\tilde{i}_1(1) + G_2\tilde{f}_1(1) \tag{3.2.2b}$$

For $k = 1$:

$$\tilde{i}_1(2) = F_1\tilde{i}_2(1) + G_1\tilde{f}_2(1) \tag{3.2.3a}$$

$$\tilde{i}_2(2) = F_2\tilde{i}_1(2) + G_2\tilde{f}_1(2) \tag{3.2.3b}$$

Equations (3.2.2a),(3.2.2b),(3.2.3a) and (3.2.3b) are example of the result at the output for the initial condition where $k = 0$ and for the next state where $k = 1$. Again it is clear that the next sample instant for each of the discrete-time state space equations depends on the current sample instant of the other state. The value for $\tilde{i}_1(0)$ is determined by the current sample $\tilde{i}_2(0)$, and vice versa.

Using this technique we are able to update the value for the discrete-time state space equations at each sample instant. Also we are able to compensate for a change in duty cycle. The value of matrices $F_{1,2}$ and $G_{1,2}$ is dependent on the type of plant and the duty cycles.

3.2.2 Small-Signal Gain

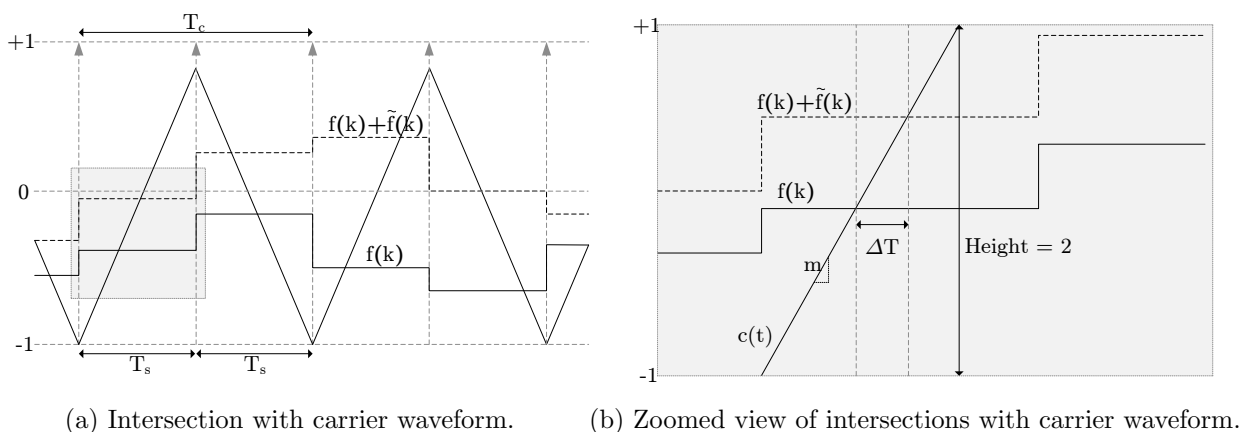


Figure 3.3: Effect of the small-signal gain.

The small-signal gain is dependent on the strength of the impulses, which depends on the gradient m of the line between the intersection of the large-signal and small-signal with the carrier signal. The strength of an impulse refers to the area of the narrow pulse, representing the effect of the small-signal model pulse-width modulator. The gradient m of the line is simply the height of the triangle carrier, divided by one sample period. This results in

$$\begin{aligned} m &= \frac{\text{height of the triangle}}{\text{sample period}} \\ &= \frac{2}{T_c} \\ &= \frac{4}{T_c} \end{aligned} \quad (3.2.4)$$

Using the gradient of the line, the width of the narrow pulse ΔT is determined to be

$$\begin{aligned} m &= \frac{\tilde{f}(k)}{\Delta T} \\ \therefore \Delta T &= \tilde{f}(k) \frac{T_c}{4} \end{aligned} \quad (3.2.5)$$

where $\tilde{f}(k)$ is the height of the small-signal at the current sample instant k .

Combining 3.2.4 and 3.2.5 the weight of the impulse, or the small-signal gain K_{ss} , can be estimated by:

$$\begin{aligned} K_{ss} &= \Delta T \times \text{height of the triangle} \\ &= \tilde{f}(k) \frac{T_c}{2} \end{aligned} \quad (3.2.6)$$

The small-signal gain K_{ss} (3.2.6) is therefore dependent on the value of the small-signal, $\tilde{f}(k)$, at each sampling instant.

3.3 Single-Phase Small-Signal Model

In Figure 3.4 a simple single-phase DC-AC digital current regulator inverter is shown with a series RL-load. Using asymmetrical RSPWM, the inductor current is sampled at twice the switching frequency. In the control loop the reference current $i^*(k)$ and the digital current regulator are defined in the discrete-time domain. The asymmetrical regular

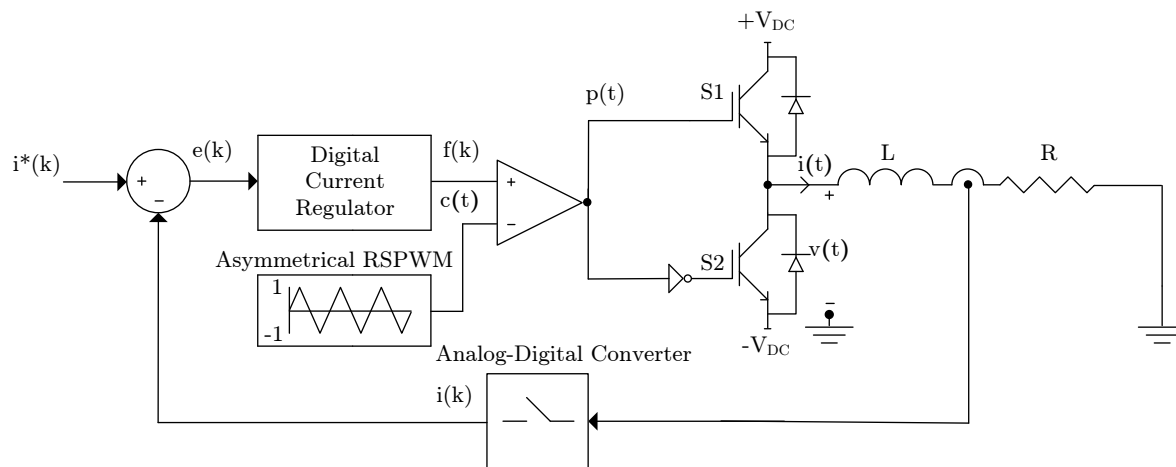


Figure 3.4: Single-phase DC-AC digital current regulator control loop with a series RL load.

sampled pulse-width modulator forms the interface between the discrete-time domain and the continuous-time domain. The inductor current $i(t)$ is defined in the continuous-time domain before it is fed back into the control loop through the analog-to-digital controller, resulting in the discrete-time inductor current $i(k)$.

Using the concept of small-signal models, the asymmetrical regular sampled pulse-width modulator is represented by an impulse generator. As mentioned previously, an impulse is generated for each sample period T_s , depending on where the large-signal intersects the carrier signal. The distance between the impulses will vary as the duty cycle varies.

An example of a small-signal current control loop is shown in Figure 3.5. A small-disturbance $\tilde{i}^*(t)$ is applied to the reference input to analyse the behaviour of the control loop. If the small-disturbance causes the output $\tilde{i}(t)$ to keep increasing the system becomes unstable, however, if the output converges to zero the system is stable.

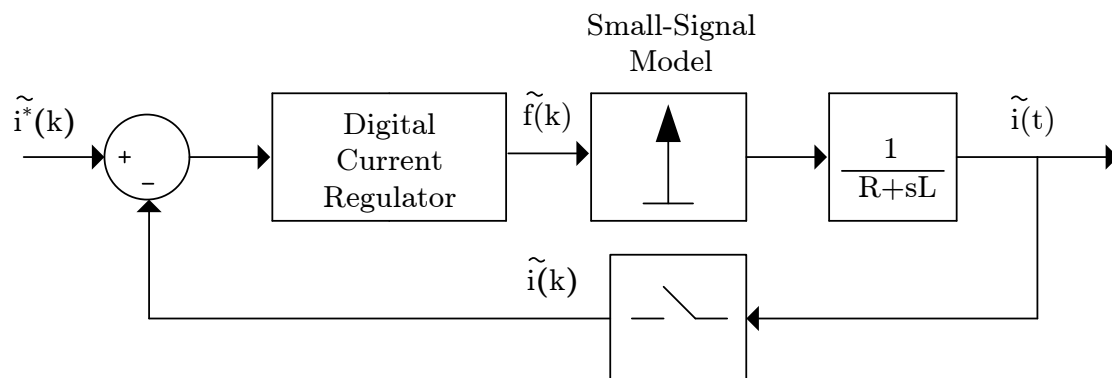


Figure 3.5: Single-phase RL load small-signal model

For the purpose of this research the controller is defined in the digital-time domain while the RL-load is defined in the continuous-time domain. The following section focusses

on deriving a small-signal model to describe the relationship between the input to the small-signal model $\tilde{f}(k)$ and the output $\tilde{i}(k)$, using state space models.

3.3.1 Continuous-Time State Space Model of a RL-load

The RL-load is representative for the plant of the controlled system. For the modelling of the dynamics of the single-phase series RL-load in Figure 3.6 only one first order differential equation is necessary.

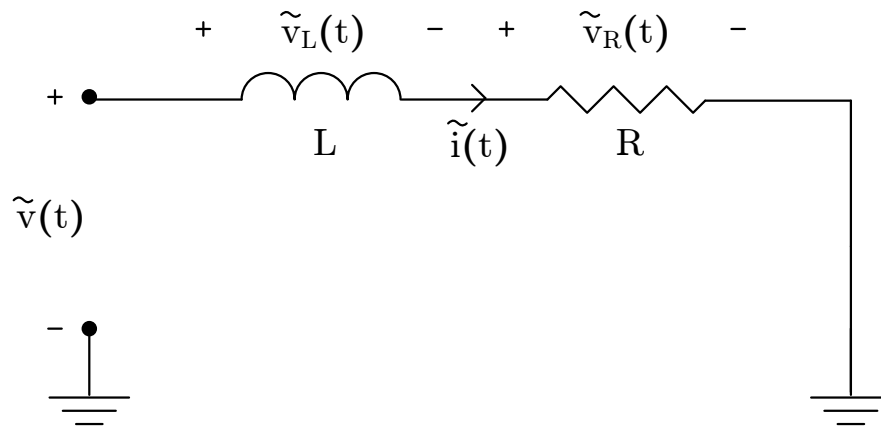


Figure 3.6: Model of a single-phase series RL-load

According to Kirchoff's Voltage Law (KVL) a differential equation for inductor current $\tilde{i}(t)$ can be written as:

$$\begin{aligned}
 \tilde{v}(t) &= \tilde{v}_L(t) + \tilde{v}_R(t) \\
 &= L \frac{d\tilde{i}}{dt} + \tilde{i}(t)R \\
 \frac{d\tilde{i}}{dt} &= \frac{1}{L} (\tilde{v}(t) - \tilde{i}(t)R) \\
 \frac{d\tilde{i}}{dt} &= \frac{\tilde{v}(t)}{L} - \frac{R}{L} \tilde{i}(t)
 \end{aligned} \tag{3.3.1}$$

where

$\tilde{v}(t)$ = small-signal phase voltage

L = load inductance

R = load resistance

$\tilde{i}(t)$ = small-signal output current

The phase voltage $\tilde{v}(t)$ is equal to the voltage drop across the inductor $\tilde{v}_L(t)$ and the resistor $\tilde{v}_R(t)$. Equation (3.3.1) can also be expressed as:

$$\frac{d\tilde{i}}{dt} = \mathbf{A}\tilde{i}(t) + \mathbf{B}\tilde{v}(t) \quad (3.3.2)$$

where $\tilde{v}(t) = K_{ss}\delta(t - t_x)$ and $\mathbf{A} = -\frac{R}{L}$, $\mathbf{B} = \frac{1}{L}$ are the system variables. Solving (3.3.2), an relationship between the input to the small-signal model $\tilde{f}(t)$ and the sampled inductor current $\tilde{i}(t)$ can be determined. The time t_x indicates the position of the impulse which occurs the moment the large-signal intersects the carrier signal.

3.3.2 Solving the Non-Homogeneous System

The continuous-time state space equation of (3.3.2) defines a non-homogeneous system, due to the input $\tilde{v}(t)$ present. Using the state transition equation (3.3.3) a solution is obtained for (3.3.2).

$$\tilde{i}(t) = e^{\mathbf{A}(t-t_0)}\tilde{i}(t_0) + \int_{t_0}^t e^{\mathbf{A}(t-\tau)}\mathbf{B}\tilde{v}(\tau)d\tau \quad (3.3.3)$$

The state transition equation (3.3.3) describes the change of state variable relative to the initial conditions $\tilde{i}(t_0)$ and the input $\tilde{v}(t)$ [17]. To describe the interface between the discrete-time and the continuous-time systems the discrete-time equivalent (3.3.4) of the continuous-time state transition equation (3.3.3) is used.

$$\tilde{i}((K+1)T_s) = e^{\mathbf{A}T_s}\tilde{i}(kT_s) + \int_{kT_s}^{(k+1)T_s} e^{\mathbf{A}((k+1)T_s-\tau)}\mathbf{B}\tilde{v}(\tau)d\tau \quad (3.3.4)$$

where the initial state $t_0 = kT_s$. The particular solution in (3.3.3) is equal to the weight of the impulse defined by (3.2.6). Since the input to the small-signal model $\tilde{f}(kT_s)$ is constant over the entire sample period T_s it can be moved out of the integration term in (3.3.4) and results into

$$\tilde{i}((K+1)T_s) = e^{\mathbf{A}T_s}\tilde{i}(kT_s) + \frac{T_c}{2}\tilde{f}(kT_s) \int_{kT_s}^{(k+1)T_s} e^{\mathbf{A}((k+1)T_s-\tau)}\mathbf{B}\delta(\tau - t_x)d\tau \quad (3.3.5)$$

where an impulse occurs at $t_x = d_1\frac{T_c}{2}$ for the first half of the switching period and at $t_x = (1 - d_2)\frac{T_c}{2}$ over the second half of the switching period. The duty cycle d_1 is defined for the rising edge carrier signal while d_2 is defined for the falling edge of the carrier signal

Using the concept dummy state variables as shown in section 3.2.1, the state space model is separated into two individual discrete-time state space models. The one for the rising edge of the triangular carrier and the other for the falling edge of the triangular carrier. In the next section the discrete-time state space model is derived.

3.3.3 Discrete-Time Equivalent State Space Model

In Figure 3.7 the mathematical procedure to derive the small-signal model is shown. A large-signal $f(k)$ is applied to the input of the pulse-width modulator which is constant over the switching period T_c and generates impulses over the rising edge of the carrier at $t = d_1 \frac{T_c}{2}$ and for the falling edge of the carrier at $t = (1 - d_2) \frac{T_c}{2}$. The small-signal input $\tilde{f}(kT_s)$ will also be constant over the switching period T_c . The small-signal input assumed to be constant and the weight of the impulses is therefore $\tilde{f}(kT_s) \frac{T_c}{2}$.

Similar to the idea explained in section 3.2.1 the separate discrete-time state space equation for the rising and falling edge of the triangular carrier can respectively be expressed as follows:

For the rising edge of triangular carrier:

$$\tilde{i}_1(k+1) = e^{-\frac{T_c}{2\tau}} \tilde{i}_2(k) + \frac{T_c}{2} \frac{1}{L} e^{-\frac{d_1 T_c}{2\tau}} \tilde{f}_2(k) \quad (3.3.6)$$

For the falling edge of triangular carrier:

$$\begin{aligned} \tilde{i}_2(k+1) &= e^{-\frac{T_c}{2\tau}} \tilde{i}_1(k+1) + \frac{T_c}{2} \frac{1}{L} e^{-\frac{(1-d_2)T_c}{2\tau}} \tilde{f}_1(k+1) \\ &= e^{-\frac{T_c}{2\tau}} \left\{ e^{-\frac{T_c}{2\tau}} \tilde{i}_2(k) + \frac{T_c}{2} \frac{1}{L} e^{-\frac{d_1 T_c}{2\tau}} \tilde{f}_2(k) \right\} + \frac{T_c}{2} \frac{1}{L} e^{-\frac{t_2}{\tau}} \tilde{f}_1(k+1) \\ &= e^{-\frac{T_c}{\tau}} \tilde{i}_2(k) + \frac{T_c}{2} \frac{1}{L} e^{-\frac{(1+d_1)T_c}{2\tau}} \tilde{f}_2(k) + \frac{T_c}{2} \frac{1}{L} e^{-\frac{(1-d_2)T_c}{2\tau}} \tilde{f}_1(k+1) \end{aligned} \quad (3.3.7)$$

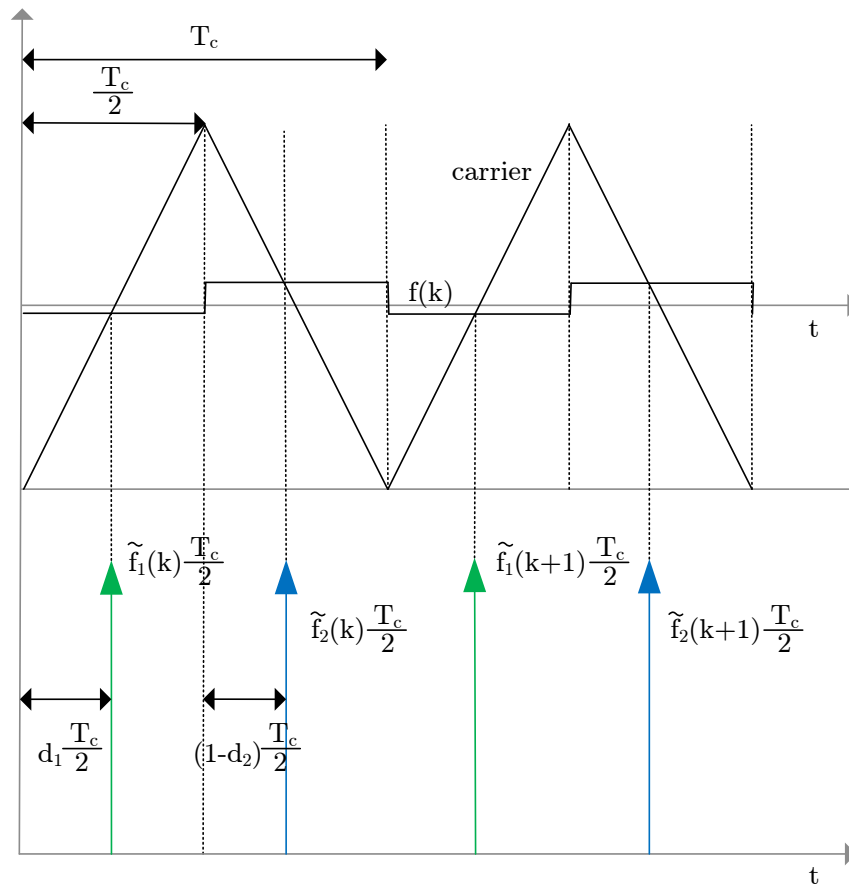
where the time constant is $\tau = -\frac{1}{\mathbf{A}}$.

Combining (3.3.6) and (3.3.7) the following discrete-time state space model is obtained for an asymmetrical regular sampled pulse-width modulator small-signal model with a single-phase RL-load. The state variables $\tilde{i}_1(k)$ and $\tilde{i}_2(k)$ are the impulses generated during the rising edge and falling edge of the triangular carrier respectively.

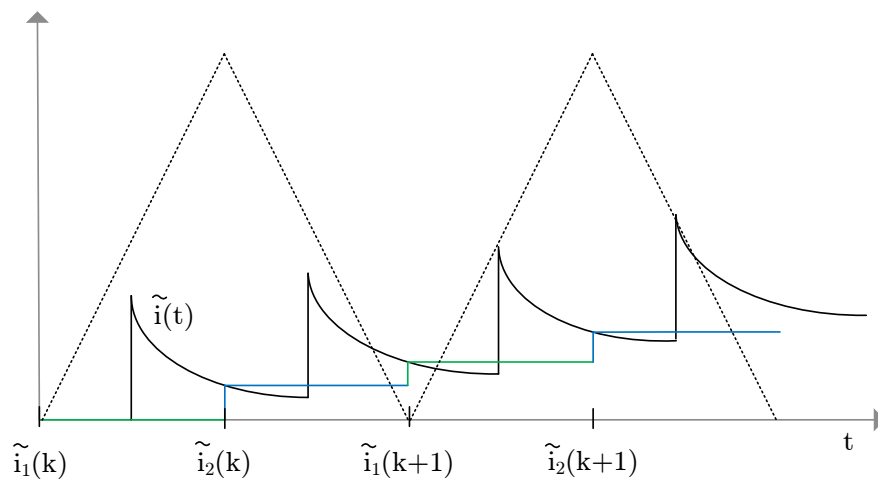
$$\begin{bmatrix} \tilde{i}_1(k+1) \\ \tilde{i}_2(k+1) \end{bmatrix} = \begin{bmatrix} 0 & e^{-\frac{T_c}{2\tau}} \\ 0 & e^{-\frac{T_c}{\tau}} \end{bmatrix} \begin{bmatrix} \tilde{i}_1(k) \\ \tilde{i}_2(k) \end{bmatrix} + \begin{bmatrix} \frac{T_c}{2} \frac{1}{L} e^{-\frac{d_1 T_c}{2\tau}} & 0 \\ \frac{T_c}{2} \frac{1}{L} e^{-\frac{(1+d_1)T_c}{2\tau}} & \frac{T_c}{2} \frac{1}{L} e^{-\frac{(1-d_2)T_c}{2\tau}} \end{bmatrix} \begin{bmatrix} \tilde{f}_2(k) \\ \tilde{f}_1(k+1) \end{bmatrix}$$

with

$$\mathbf{F} = \begin{bmatrix} 0 & e^{-\frac{T_c}{2\tau}} \\ 0 & e^{-\frac{T_c}{\tau}} \end{bmatrix}, \mathbf{G} = \begin{bmatrix} \frac{T_c}{2} \frac{1}{L} e^{-\frac{d_1 T_c}{2\tau}} & 0 \\ \frac{T_c}{2} \frac{1}{L} e^{-\frac{(1+d_1)T_c}{2\tau}} & \frac{T_c}{2} \frac{1}{L} e^{-\frac{(1-d_2)T_c}{2\tau}} \end{bmatrix}$$



(a) The series of impulses representing the small-signal model.



(b) The small-signal continuous and discrete output currents.

Figure 3.7: Derivation of the discrete equivalent small-signal model of the pulse-width modulator.

With \mathbf{F} and \mathbf{G} the new system matrices. By adding a controller the stability of the closed loop system can be determined.

In the next section this theory is extended for a three-phase system.

3.4 Three-Phase Small-Signal Model

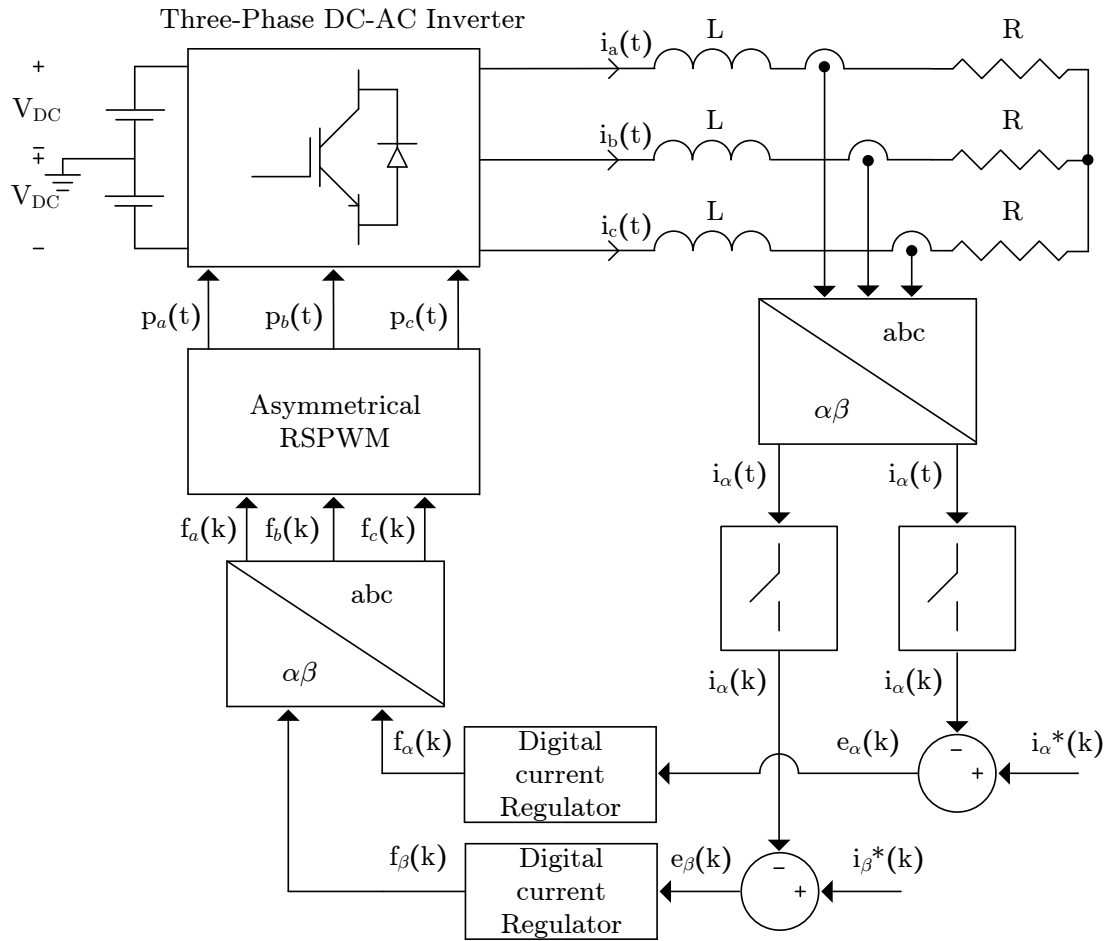


Figure 3.8: Three-phase RL load DC-AC

The single-phase small-signal model derived in section 3.3 is now extended for a three-phase current regulated inverter as shown in Figure 3.8. The balanced three-phase load is connected in a floating star point connection, the sum of three-phase currents being zero.

Two digital current regulators are implemented in the stationary d-q frame, with no zero sequence component as a balanced load is used. The stationary d-q frame can also be denoted by α and β , the so-called Clarke's components [12]. Using the Clarke transformation the abc phase currents are expressed in terms of its α and β components. The α and β currents are then sampled and subtracted from the reference inputs to give the error signal.

Implementing the digital current regulators in a stationary reference frame simplifies the design of the digital current regulators, because only two current regulators are necessary. The control system can then be represented by two independent α and β single-phase current regulator control loops, similar to Figure 3.5. The output of the current regulators

are then transformed back to the abc frame, where the interface between the discrete-time domain and the continuous-time domain is determined by the the asymmetrical regular sampled pulse-width modulator.

Similar to section 3.3, an accurate small-signal model is now derived in the following section to represent the behaviour of the control loop between the input to the modulator and the output of the sampler.

3.4.1 Superposition Theorem

In the context of the small-signal model the asymmetrical regular sampled pulse-width modulator is represented by impulses occurring when the large-signal intersects the carrier. Therefore it is unlikely that the impulses generated for each phase would occur at the same instant. As the impulses are represented by independent voltage sources and the plant of the system is a linear RL-load, the principle of superposition can be applied to analyse the effect of the independent voltage sources on each individual phase. The principle of superposition states that whenever a linear system is excited, or driven, by more than one independent source of energy, the total response is the sum of the individual responses [18]. Since in this case the load is linear the superposition theorem can be applied. According to the law of superposition any independent voltage source behaves as a short-circuit and a independent current source as an open circuit.

In the following sections the differential equation is solved for each of the phase currents, using superposition. The contribution of each of the independent voltage sources to the phase currents are first determined individually and then added together to obtain the phase current, for example $\tilde{i}_a = \tilde{i}'_a + \tilde{i}''_a + \tilde{i}'''_a$.

3.4.1.1 Phase a

At first the contribution of the independent voltage source \tilde{v}_A is considered on its own, while the the voltage sources \tilde{v}_B and \tilde{v}_C are short-circuited. The phase currents in Figure 3.10 results from the independent voltage source \tilde{v}_A only. Using nodal analysis the node voltage \tilde{v}_{1A} across the parallel RL-load is determined as follows:

$$\begin{aligned} \frac{-\tilde{v}_A + \tilde{v}_{1A}}{sL + R} + \frac{\tilde{v}_{1A}}{sL + R} + \frac{\tilde{v}_{1A}}{sL + R} &= 0 \\ -\tilde{v}_A + \tilde{v}_{1A} &= -2\tilde{v}_{1A} \\ \tilde{v}_A &= 3\tilde{v}_{1A} \\ \tilde{v}_{1A} &= \frac{1}{3}\tilde{v}_A \end{aligned} \tag{3.4.1}$$

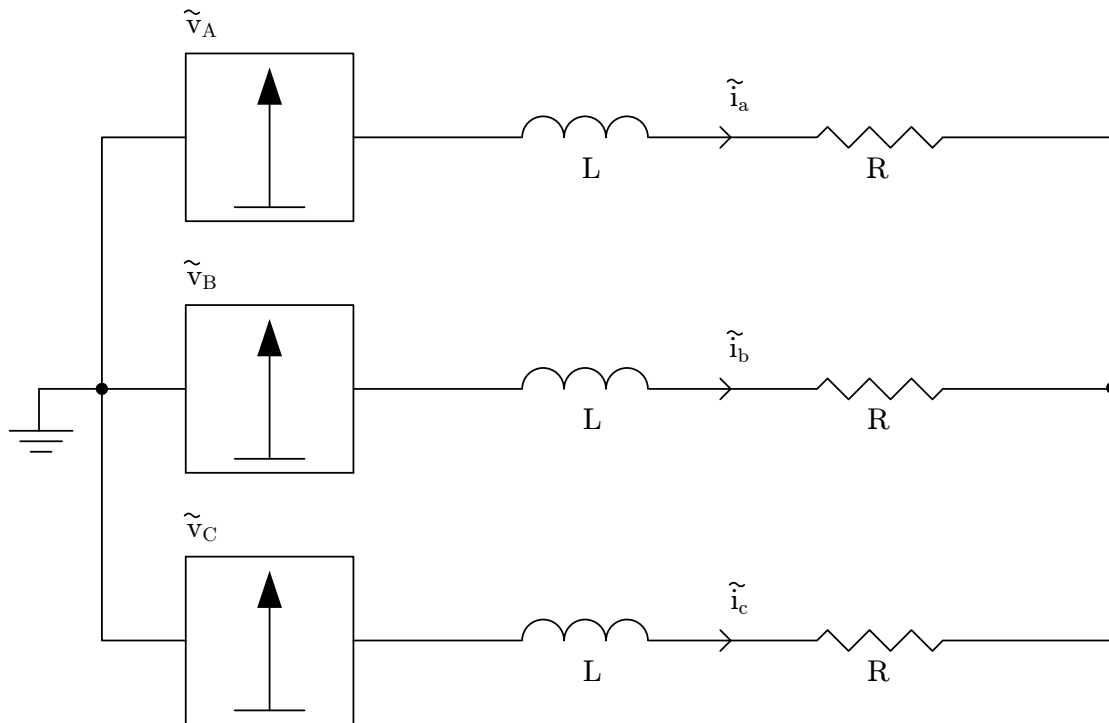


Figure 3.9: The PWM is represented by an impulse generator for each phase of the balanced three-phase load.

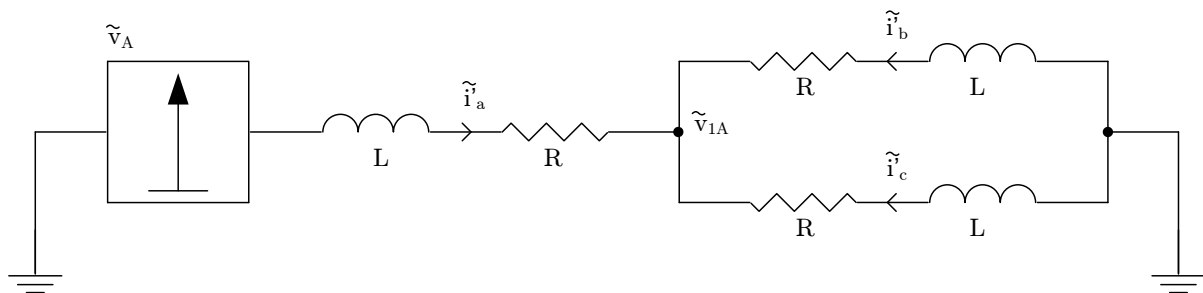


Figure 3.10: Superposition replacing independent voltage sources v_B and v_C by short circuits.

Using the node voltage \tilde{v}_{1A} , an expression for the phase currents $\tilde{i}'_a, \tilde{i}'_b$ and \tilde{i}'_c are obtained

in terms of the independent voltage source \tilde{v}_A .

$$\begin{aligned}\tilde{i}'_a &= -\frac{\tilde{v}_{1A} - \tilde{v}_A}{sL + R} \\ &= \frac{2}{3} \frac{\tilde{v}_A}{sL + R}\end{aligned}\quad (3.4.2a)$$

$$\begin{aligned}\tilde{i}'_b &= -\frac{\tilde{v}_{1A}}{sL + R} \\ &= -\frac{1}{3} \frac{\tilde{v}_A}{sL + R}\end{aligned}\quad (3.4.2b)$$

$$\tilde{i}'_c = \tilde{i}'_b \quad (3.4.2c)$$

Since phases b and c are in parallel, the current through each of them is only half the current through phase a.

3.4.1.2 Phase b

Similarly the phase currents resulting from the independent voltage source \tilde{v}_B can be calculated, replacing voltage sources \tilde{v}_A and \tilde{v}_C by short circuits. The node voltage \tilde{v}_{1B} is determined as follows:

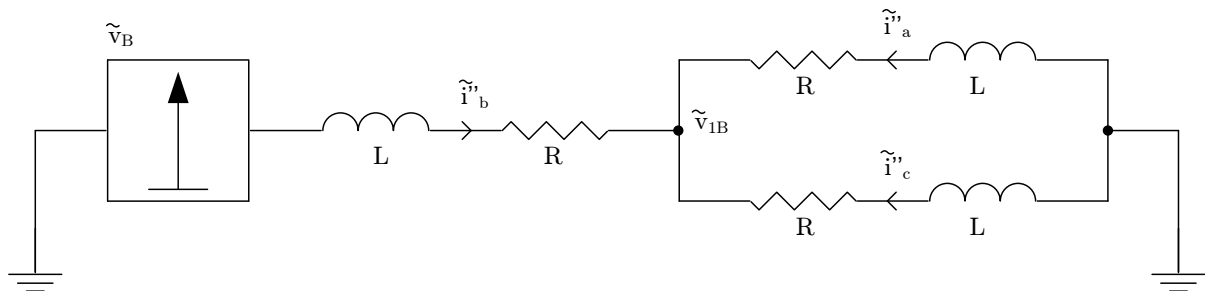


Figure 3.11: Superposition replacing independent voltage sources \tilde{v}_A and \tilde{v}_C by short circuits.

$$\begin{aligned}-\frac{\tilde{v}_B + \tilde{v}_{1B}}{sL + R} + \frac{\tilde{v}_{1B}}{sL + R} + \frac{\tilde{v}_{1B}}{sL + R} &= 0 \\ -\tilde{v}_B + \tilde{v}_{1B} &= -2\tilde{v}_{1B} \\ \tilde{v}_B &= 3\tilde{v}_{1B} \\ \tilde{v}_{1B} &= \frac{1}{3}\tilde{v}_B\end{aligned}\quad (3.4.3)$$

The phase currents \tilde{i}_a'' , \tilde{i}_b'' and \tilde{i}_c'' in Figure 3.11 resulting from the independent voltage source \tilde{v}_B is calculated to be

$$\begin{aligned}\tilde{i}_b'' &= -\frac{\tilde{v}_{1B} - \tilde{v}_B}{sL + R} \\ &= \frac{2}{3} \frac{\tilde{v}_B}{sL + R}\end{aligned}\quad (3.4.4a)$$

$$\begin{aligned}\tilde{i}_a'' &= -\frac{\tilde{v}_{1B}}{sL + R} \\ &= -\frac{1}{3} \frac{\tilde{v}_B}{sL + R}\end{aligned}\quad (3.4.4b)$$

$$\tilde{i}_c'' = \tilde{i}_a'' \quad (3.4.4c)$$

3.4.1.3 Phase c

Again using superposition, the phase currents resulting from the independent voltage source \tilde{v}_C are determined, while the voltage sources \tilde{v}_A and \tilde{v}_B are replaced by short circuits. The node voltage \tilde{v}_{1C} is determined as follows:

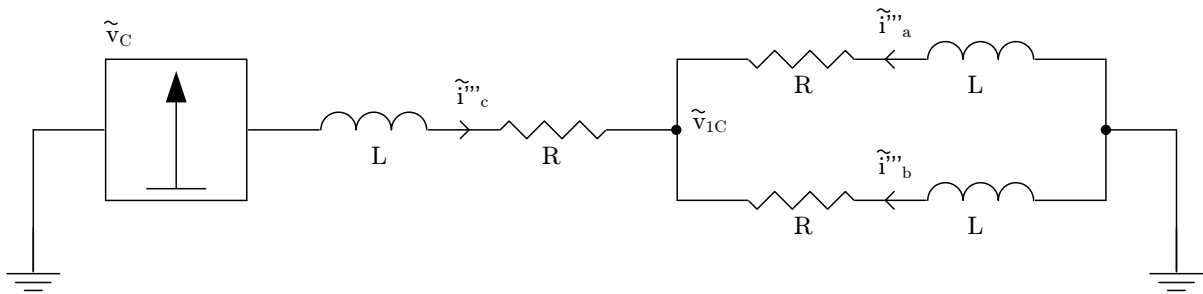


Figure 3.12: Superposition replacing independent voltage sources \tilde{v}_A and \tilde{v}_B by short circuits.

$$\begin{aligned}-\frac{\tilde{v}_C + \tilde{v}_{1C}}{sL + R} + \frac{\tilde{v}_{1C}}{sL + R} + \frac{\tilde{v}_{1C}}{sL + R} &= 0 \\ -\tilde{v}_C + \tilde{v}_{1C} &= -2\tilde{v}_{1C} \\ \tilde{v}_C &= 3\tilde{v}_{1C} \\ \tilde{v}_{1C} &= \frac{1}{3}\tilde{v}_C\end{aligned}\quad (3.4.5)$$

The phase currents \tilde{i}_a''' , \tilde{i}_b''' and \tilde{i}_c''' in Figure 3.12 resulting from the independent voltage source \tilde{v}_C are calculated as follows:

$$\begin{aligned}\tilde{i}_c'' &= -\frac{\tilde{v}_{1C} - \tilde{v}_C}{sL + R} \\ &= \frac{2}{3} \frac{\tilde{v}_C}{sL + R}\end{aligned}\quad (3.4.6a)$$

$$\begin{aligned}\tilde{i}_a'' &= -\frac{\tilde{v}_{1C}}{sL + R} \\ &= -\frac{1}{3} \frac{\tilde{v}_C}{sL + R}\end{aligned}\quad (3.4.6b)$$

$$\tilde{i}_b'' = \tilde{i}_a'' \quad (3.4.6c)$$

The phase currents \tilde{i}_a , \tilde{i}_b and \tilde{i}_c from the original circuit, Figure 3.9, can now be calculated by adding the currents given by equations (3.4.2a-3.4.2c), (3.4.4a-3.4.4c) and (3.4.6a-3.4.6c).

Phase current, \tilde{i}_a :

$$\begin{aligned}\tilde{i}_a &= \tilde{i}_a' + \tilde{i}_a'' + \tilde{i}_a''' \\ &= \frac{2}{3} \frac{\tilde{v}_A}{sL + R} - \frac{1}{3} \frac{\tilde{v}_B}{sL + R} - \frac{1}{3} \frac{\tilde{v}_C}{sL + R} \\ &= \frac{1}{sL + R} \left(\frac{2}{3} \tilde{v}_A - \frac{1}{3} \tilde{v}_B - \frac{1}{3} \tilde{v}_C \right)\end{aligned}$$

$$\begin{aligned}L \frac{d\tilde{i}_a}{dt} + R\tilde{i}_a &= \left(\frac{2}{3} \tilde{v}_A - \frac{1}{3} \tilde{v}_B - \frac{1}{3} \tilde{v}_C \right) \\ \frac{d\tilde{i}_a}{dt} &= -\frac{R}{L} \tilde{i}_a + \frac{1}{L} \left(\frac{2}{3} \tilde{v}_A - \frac{1}{3} \tilde{v}_B - \frac{1}{3} \tilde{v}_C \right) \\ \frac{d\tilde{i}_a}{dt} &= -\frac{R}{L} \tilde{i}_a + \frac{1}{3L} (2\tilde{v}_A - \tilde{v}_B - \tilde{v}_C)\end{aligned}\quad (3.4.7)$$

Phase current, \tilde{i}_b :

$$\begin{aligned}\tilde{i}_b &= \tilde{i}_b' + \tilde{i}_b'' + \tilde{i}_b''' \\ &= -\frac{1}{3} \frac{\tilde{v}_A}{sL + R} + \frac{2}{3} \frac{\tilde{v}_B}{sL + R} - \frac{1}{3} \frac{\tilde{v}_C}{sL + R} \\ &= \frac{1}{sL + R} \left(\frac{2}{3} \tilde{v}_B - \frac{1}{3} \tilde{v}_A - \frac{1}{3} \tilde{v}_C \right)\end{aligned}$$

$$\begin{aligned}L \frac{d\tilde{i}_b}{dt} + R\tilde{i}_b &= \left(\frac{2}{3} \tilde{v}_B - \frac{1}{3} \tilde{v}_A - \frac{1}{3} \tilde{v}_C \right) \\ \frac{d\tilde{i}_b}{dt} &= -\frac{R}{L} \tilde{i}_b + \frac{1}{L} \left(\frac{2}{3} \tilde{v}_B - \frac{1}{3} \tilde{v}_A - \frac{1}{3} \tilde{v}_C \right) \\ \frac{d\tilde{i}_b}{dt} &= -\frac{R}{L} \tilde{i}_b + \frac{1}{3L} (2\tilde{v}_B - \tilde{v}_A - \tilde{v}_C)\end{aligned}\quad (3.4.8)$$

Phase current, \tilde{i}_c :

$$\begin{aligned}
 \tilde{i}_c &= \tilde{i}'_c + \tilde{i}''_c + \tilde{i}'''_c \\
 &= -\frac{1}{3} \frac{\tilde{v}_A}{sL + R} - \frac{1}{3} \frac{\tilde{v}_B}{sL + R} + \frac{2}{3} \frac{\tilde{v}_C}{sL + R} \\
 &= \frac{1}{sL + R} \left(\frac{2}{3} \tilde{v}_C - \frac{1}{3} \tilde{v}_A - \frac{1}{3} \tilde{v}_B \right) \\
 L \frac{d\tilde{i}_c}{dt} + R\tilde{i}_c &= \left(\frac{2}{3} \tilde{v}_C - \frac{1}{3} \tilde{v}_A - \frac{1}{3} \tilde{v}_B \right) \\
 \frac{d\tilde{i}_c}{dt} &= -\frac{R}{L} \tilde{i}_c + \frac{1}{3L} (2\tilde{v}_C - \tilde{v}_A - \tilde{v}_B) \tag{3.4.9}
 \end{aligned}$$

A first-order differential equation is obtained for each of the phase currents. Unlike in the case of the single-phase system, where there was only a single input $\tilde{v}(t)$, each of the phase currents for a three-phase system is dependent not only on its own input, but also on those of the other two phases.

For instance the phase current \tilde{i}_a is dependent on its own input $\tilde{v}_A(t)$, as well as $\tilde{v}_B(t)$ and $\tilde{v}_C(t)$. According to (3.4.7), (3.4.8) and (3.4.9) this could be extended to each of the phase currents. These inputs represent the impulses generated by the small-signal model.

This is a very important concept, because this means that if impulses on the different phases occur during the same instant, the impulses could effect the other phases. In previous research this effect was ignored, due to the assumption that each phase of an three-phase system reacts independently. This assumption will be investigated further, using the small-signal models.

Similar to the single-phase system a discrete-time equivalent state space small-signal model has been derived of a three-phase system. In the single-phase model a 2×2 system matrix is used to express the output of the sampler $i(k)$ relative to the input to the modulator $f(k)$, but for the three-phase model the 2×2 system matrix will now be expanded to a 4×4 system matrix. Something else to consider is that, according to the first-order differential equations, the three-phase model is actually a multiple-input, multiple-output system (MIMO). However, using the Clark transform the three-phase model could be reduced in two separate α and β single-phase models.

3.4.2 Clark Transform (Modified Definition)

Using the Clark transform the abc phase currents could be transformed to its α and β coordinates. This a very useful method that simplifies the design of controllers, because instead of three controllers only two is necessary. This also reduces the calculation effort needed to calculate the matrices, a factor which becomes important for the simulations.

The modified α and β transformation defined in [12] is used. The influence of the zero-component is neglected as it is assumed that a balanced load is used. From the Clark transform (3.4.10) it shows that in the stationary reference frame there is essentially only two phase currents that needs to be controlled.

$$\begin{bmatrix} \tilde{i}_\alpha \\ \tilde{i}_\beta \\ \tilde{i}_0 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & -\frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \tilde{i}_a \\ \tilde{i}_b \\ \tilde{i}_c \end{bmatrix} \quad (3.4.10)$$

$$\tilde{i}_\alpha = \tilde{i}_a \quad (3.4.11a)$$

$$\tilde{i}_\beta = -\frac{1}{\sqrt{3}}\tilde{i}_b + \frac{1}{\sqrt{3}}\tilde{i}_c \quad (3.4.11b)$$

$$\tilde{i}_0 = 0 \quad (3.4.11c)$$

The relationship between the three-phase currents can now be expressed by (3.4.11a)-(3.4.11c). Differentiating the equations above we are able to transform the first order differential equations (3.4.7)-(3.4.9) obtained for the phase currents to their stationary reference coordinates.

$$\begin{aligned} \frac{d\tilde{i}_\alpha}{dt} &= \frac{d\tilde{i}_a}{dt} \\ &= -\frac{R_\gamma}{L}\tilde{i}_a + \frac{1}{L}\left(\frac{2}{3}\tilde{v}_A - \frac{1}{3}\tilde{v}_B - \frac{1}{3}\tilde{v}_C\right) \\ &= -\frac{R_\gamma}{L}\tilde{i}_\alpha + \frac{1}{L}\left(\frac{2}{3}\tilde{v}_A - \frac{1}{3}\tilde{v}_B - \frac{1}{3}\tilde{v}_C\right) \\ &= -\frac{R_\gamma}{L}\tilde{i}_\alpha + \frac{1}{3L}(2\tilde{v}_A - \tilde{v}_B - \tilde{v}_C) \end{aligned} \quad (3.4.12a)$$

$$\begin{aligned} \frac{d\tilde{i}_\beta}{dt} &= -\frac{1}{\sqrt{3}}\frac{d\tilde{i}_b}{dt} + \frac{1}{\sqrt{3}}\frac{d\tilde{i}_c}{dt} \\ &= -\frac{1}{\sqrt{3}}\left(-\frac{R_\gamma}{L}\tilde{i}_b + \frac{1}{L}\left(\frac{2}{3}\tilde{v}_B - \frac{1}{3}\tilde{v}_A - \frac{1}{3}\tilde{v}_C\right)\right) + \frac{1}{\sqrt{3}}\left(-\frac{R_\gamma}{L}\tilde{i}_c + \frac{1}{L}\left(\frac{2}{3}\tilde{v}_C - \frac{1}{3}\tilde{v}_A - \frac{1}{3}\tilde{v}_B\right)\right) \\ &= \frac{1}{\sqrt{3}}\frac{R_\gamma}{L}\tilde{i}_b - \frac{1}{\sqrt{3}}\frac{R_\gamma}{L}\tilde{i}_c - \frac{1}{\sqrt{3}L}\left(\frac{2}{3}\tilde{v}_B - \frac{1}{3}\tilde{v}_A - \frac{1}{3}\tilde{v}_C\right) + \frac{1}{\sqrt{3}L}\left(\frac{2}{3}\tilde{v}_C - \frac{1}{3}\tilde{v}_A - \frac{1}{3}\tilde{v}_B\right) \\ &= \frac{1}{\sqrt{3}}\frac{R_\gamma}{L}\tilde{i}_b - \frac{1}{\sqrt{3}}\frac{R_\gamma}{L}\tilde{i}_c + \frac{1}{\sqrt{3}L}\left(-\frac{2}{3}\tilde{v}_B + \frac{1}{3}\tilde{v}_A + \frac{1}{3}\tilde{v}_C\right) + \frac{1}{\sqrt{3}L}\left(\frac{2}{3}\tilde{v}_C - \frac{1}{3}\tilde{v}_A - \frac{1}{3}\tilde{v}_B\right) \\ &= \frac{1}{\sqrt{3}}\frac{R_\gamma}{L}\tilde{i}_b - \frac{1}{\sqrt{3}}\frac{R_\gamma}{L}\tilde{i}_c + \frac{1}{3\sqrt{3}L}(-2\tilde{v}_B + \tilde{v}_A + \tilde{v}_C) + \frac{1}{3\sqrt{3}L}(2\tilde{v}_C - \tilde{v}_A - \tilde{v}_B) \\ &= \frac{1}{\sqrt{3}}\frac{R_\gamma}{L}\tilde{i}_b - \frac{1}{\sqrt{3}}\frac{R_\gamma}{L}\tilde{i}_c + \frac{1}{3\sqrt{3}L}(3\tilde{v}_C - 3\tilde{v}_B) \end{aligned} \quad (3.4.12b)$$

Equation (3.4.12a) and (3.4.12b) shows that the inputs are still defined in their abc coordinates. Using the inverse Clark transform (3.4.13) their and substituting them their α

and β equivalent is obtained.

$$\begin{bmatrix} \tilde{i}_a \\ \tilde{i}_b \\ \tilde{i}_c \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 0 \end{bmatrix} \begin{bmatrix} \tilde{i}_\alpha \\ \tilde{i}_\beta \\ \tilde{i}_0 \end{bmatrix} \quad (3.4.13)$$

$$\tilde{i}_a = \tilde{i}_\alpha \quad (3.4.14)$$

$$\tilde{i}_b = -\frac{1}{2}\tilde{i}_\alpha - \frac{\sqrt{3}}{2}\tilde{i}_\beta \quad (3.4.15)$$

$$\tilde{i}_c = -\frac{1}{2}\tilde{i}_\alpha + \frac{\sqrt{3}}{2}\tilde{i}_\beta \quad (3.4.16)$$

Substituting (3.4.14) - (3.4.16) into (3.4.12a) and (3.4.12b), two independent alpha- and beta equations is obtained.

$$\begin{aligned} \frac{d\tilde{i}_\alpha}{dt} &= -\frac{R_\gamma}{L}\tilde{i}_\alpha + \frac{1}{3L}(2\tilde{v}_A - \tilde{v}_B - \tilde{v}_C) \\ &= -\frac{R_\gamma}{L}\tilde{i}_\alpha + \frac{1}{3L}(2\tilde{v}_\alpha + \frac{1}{2}\tilde{v}_\alpha + \frac{\sqrt{3}}{2}\tilde{v}_\beta + \frac{1}{2}\tilde{v}_\alpha - \frac{\sqrt{3}}{2}\tilde{v}_\beta) \\ &= -\frac{R_\gamma}{L}\tilde{i}_\alpha + \frac{1}{3L}(3\tilde{v}_\alpha) \\ &= -\frac{R_\gamma}{L}\tilde{i}_\alpha + \frac{1}{L}\tilde{v}_\alpha \\ &= \mathbf{A}_\alpha\tilde{i}_\alpha + \mathbf{B}_\alpha\tilde{v}_\alpha \end{aligned} \quad (3.4.17a)$$

$$\begin{aligned} \frac{d\tilde{i}_\beta}{dt} &= \frac{1}{\sqrt{3}}\frac{R_\gamma}{L}\tilde{i}_b - \frac{1}{\sqrt{3}}\frac{R_\gamma}{L}\tilde{i}_c + \frac{1}{3\sqrt{3}L}(3\tilde{v}_C - 3\tilde{v}_B) \\ &= \frac{1}{\sqrt{3}}\frac{R_\gamma}{L}\left(-\frac{1}{2}\tilde{i}_\alpha - \frac{\sqrt{3}}{2}\tilde{i}_\beta\right) + \frac{1}{\sqrt{3}}\frac{R_\gamma}{L}\left(+\frac{1}{2}\tilde{i}_\alpha - \frac{\sqrt{3}}{2}\tilde{i}_\beta\right) + \frac{1}{3\sqrt{3}L}\left(3\left(-\frac{1}{2}\tilde{v}_\alpha + \frac{\sqrt{3}}{2}\tilde{v}_\beta\right) - 3\left(-\frac{1}{2}\tilde{i}_\alpha - \frac{\sqrt{3}}{2}\tilde{i}_\beta\right)\right) \\ &= \frac{1}{\sqrt{3}}\frac{R_\gamma}{L}\left(-\frac{1}{2}\tilde{i}_\alpha - \frac{\sqrt{3}}{2}\tilde{i}_\beta + \frac{1}{2}\tilde{i}_\alpha - \frac{\sqrt{3}}{2}\tilde{i}_\beta\right) + \frac{1}{3\sqrt{3}L}\left(-\frac{3}{2}\tilde{v}_\alpha + \frac{3\sqrt{3}}{2}\tilde{v}_\beta + \frac{3}{2}\tilde{v}_\alpha + \frac{3\sqrt{3}}{2}\tilde{v}_\beta\right) \\ &= \frac{1}{\sqrt{3}}\frac{R_\gamma}{L}(-\sqrt{3}\tilde{i}_\beta) + \frac{1}{3\sqrt{3}L}(3\sqrt{3}\tilde{v}_\beta) \\ &= -\frac{R_\gamma}{L}\tilde{i}_\beta + \frac{1}{L_s}\tilde{v}_\beta \\ &= \mathbf{A}_\beta\tilde{i}_\beta + \mathbf{B}_\beta\tilde{v}_\beta \end{aligned} \quad (3.4.17b)$$

where

$$\mathbf{A}_\alpha = \mathbf{A}_\beta = -\frac{R_\gamma}{L}, \mathbf{B}_\alpha = \mathbf{B}_\beta = \frac{1}{L}$$

The state equations (3.4.17a) and (3.4.17b) is similar to which was found with the single-phase model in section 3.3.

3.4.3 Continuous-Time State Space Model for Three-Phase RL-load

Combining (3.4.17a) and (3.4.17b) the three-phase α and β transformation can be formulated into an compact vector-matrix notation which can be used for the mathematical model [17]. Equation (3.4.17a) and (3.4.17b) can be expressed in the following vector-matrix notation,

$$\begin{bmatrix} \frac{d\tilde{i}_\alpha}{dt} \\ \frac{d\tilde{i}_\beta}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 \\ 0 & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} \tilde{i}_\alpha \\ \tilde{i}_\beta \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} \tilde{v}_\alpha \\ \tilde{v}_\beta \end{bmatrix}$$

The input $\tilde{v}_{\alpha/\beta}(t)$ of the system, the state variables and the $\tilde{i}_{\alpha/\beta}(k)$ are defined in the stationary d-q frame. The input $\tilde{v}_{\alpha/\beta}(t)$ represents the small-disturbance voltages.

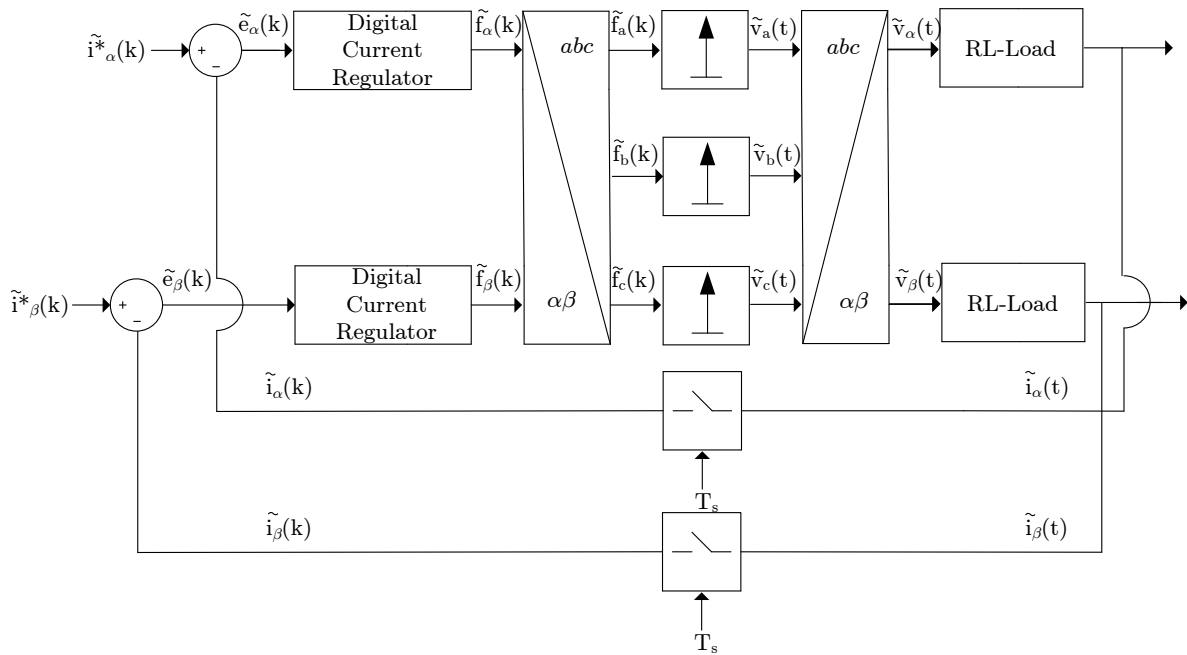


Figure 3.13: Small-signal model representation for a three-phase PI current regulator.

Figure 3.13 shows the equivalent three-phase small-signal model, where only the contribution of the small-disturbance is considered. Resulting in the following continuous small-signal state equations

$$\frac{d\tilde{i}_\alpha}{dt} = \mathbf{A}_\alpha \tilde{i}_\alpha + \mathbf{B}_\alpha \tilde{v}_\alpha \quad (3.4.18a)$$

$$\frac{d\tilde{i}_\beta}{dt} = \mathbf{A}_\beta \tilde{i}_\beta + \mathbf{B}_\beta \tilde{v}_\beta \quad (3.4.18b)$$

The small-signal output of the pulse-width modulator can thus be described by

$$\tilde{v}_a(t) = K_{ss_a} \delta(t - t_a) = \frac{T_c}{2} \tilde{f}_a(k) \delta(t - t_a) \quad (3.4.19a)$$

$$\tilde{v}_b(t) = K_{ss_b} \delta(t - t_b) = \frac{T_c}{2} \tilde{f}_b(k) \delta(t - t_b) \quad (3.4.19b)$$

$$\tilde{v}_c(t) = K_{ss_c} \delta(t - t_c) = \frac{T_c}{2} \tilde{f}_c(k) \delta(t - t_c) \quad (3.4.19c)$$

where the position of the impulses is dependent on the values of the duty cycles and small-signal gains of each of the phases. The relationship between the output of the digital current regulator and the input to the small-signal model can be described by a Clark transform.

$$\tilde{f}_a(k) = \tilde{f}_\alpha(k) \quad (3.4.20a)$$

$$\tilde{f}_b(k) = -\frac{1}{2} \tilde{f}_\alpha(k) - \frac{\sqrt{3}}{2} \tilde{f}_\beta(k) \quad (3.4.20b)$$

$$\tilde{f}_c(k) = -\frac{1}{2} \tilde{f}_\alpha(k) + \frac{\sqrt{3}}{2} \tilde{f}_\beta(k) \quad (3.4.20c)$$

Now the output voltage of the small-signal model can be described in the α and β frame by using the inverse Clarke transformation.

$$\tilde{v}_\alpha(t) = \frac{T_c}{2} \tilde{f}_\alpha(k) \delta(t - t_a) \quad (3.4.21a)$$

$$\tilde{v}_\beta(t) = \frac{1}{\sqrt{3}} \frac{T_c}{2} \left(\frac{1}{2} \tilde{f}_\alpha(k) + \frac{\sqrt{3}}{2} \tilde{f}_\beta(k) \right) \delta(t - t_b) - \frac{1}{\sqrt{3}} \frac{T_c}{2} \left(\frac{1}{2} \tilde{f}_\alpha(k) - \frac{\sqrt{3}}{2} \tilde{f}_\beta(k) \right) \delta(t - t_c) \quad (3.4.21b)$$

Substituting (3.4.21a) and (3.4.21b) into (3.4.18a) and (3.4.18b) respectively, a solution could be obtained for the individual output currents \tilde{i}_α and \tilde{i}_β .

3.4.4 Solving the Non-Homogeneous System

Equations (3.4.18a) and (3.4.18b) defines the two non-homogeneous systems in the α and β frame. A solution is obtained for each system using the state-transition equation defined (3.3.3) in section 3.3.2. Applying the discrete-time state-transition equations (3.3.4) to (3.4.18a) and (3.4.18b) results in

$$\tilde{i}_\alpha((K+1)T_s) = e^{\mathbf{A}T_s} \tilde{i}_\alpha(kT_s) + \int_{kT_s}^{(k+1)T_s} e^{\mathbf{A}((k+1)T_s-\tau)} \mathbf{B} \tilde{v}_\alpha(\tau) d\tau \quad (3.4.22a)$$

$$\tilde{i}_\beta((K+1)T_s) = e^{\mathbf{A}T_s} \tilde{i}_\beta(kT_s) + \int_{kT_s}^{(k+1)T_s} e^{\mathbf{A}((k+1)T_s-\tau)} \mathbf{B} \tilde{v}_\beta(\tau) d\tau \quad (3.4.22b)$$

Since $\tilde{v}_\alpha(t)$ is only dependent on the impulse generated in phase a, the solution of (3.4.22a) is similar to the single-phase small-signal model (3.3.5). However, since $\tilde{v}_\beta(t)$ depends on

both the impulses generated in phase b and phase c, the solution of (3.4.22b) becomes more complex. The particular solution of (3.4.22b) therefore results in

$$\int_{kT_s}^{(k+1)T_s} e^{\mathbf{A}((k+1)T_s-\tau)} \mathbf{B} \tilde{v}_\beta(\tau) d\tau = \frac{1}{\sqrt{3}} e^{-\mathbf{A}d_b \frac{T_c}{2}} \mathbf{b} \frac{T_c}{2} \left(\frac{1}{2} f_{ss_\alpha}(t_b) + \frac{\sqrt{3}}{2} f_{ss_\beta}(t_b) \right) - \frac{1}{\sqrt{3}} e^{-\mathbf{A}d_c \frac{T_c}{2}} \mathbf{b} \frac{T_c}{2} \left(\frac{1}{2} f_{ss_\alpha}(t_c) - \frac{\sqrt{3}}{2} f_{ss_\beta}(t_c \frac{T_s}{2}) \right)$$

As an asymmetrical regularly sampled pulse-width modulator is used, the positions of the impulses generated during the rising- and falling edges of the triangular carrier are different. For the rising edge an impulse occurs each time at $t = d_{x1} \frac{T_c}{2}$ and for the falling edge each time at $t = (1-d_{x2}) \frac{T_c}{2}$. It is therefore necessary to separated each state equation into two individual discrete-time state space models.

In the next section the discrete-time equivalent state space models are derived for the state variables $\tilde{i}_\alpha(k)$ and $\tilde{i}_\beta(k)$.

3.4.5 Discrete-Time Equivalent State Space Model

The discrete-time state space models are derived for the state variables $i_\alpha(k)$ and $i_\beta(k)$ individually. For each of the continuous-time state equations two discrete-time state equations are derived, one to describe the impulses generated during the rising edge and another for the impulses generated during the falling edge of the triangular carrier.

At first only the α control loop is considered, in which case the output of the sampler for the rising edge is given by

$$\tilde{i}_{1\alpha}(k+1) = e^{-\frac{T_c}{2\tau}} \tilde{i}_{2\alpha}(k) + \frac{T_c}{2} \frac{1}{L} e^{-\frac{d_{a1}T_c}{2\tau}} \tilde{f}_{2\alpha}(k) \quad (3.4.23)$$

and for the falling edge by

$$\begin{aligned} \tilde{i}_{2\alpha}(k+1) &= e^{-\frac{T_c}{2\tau}} \tilde{i}_{1\alpha}(k+1) + \frac{T_c}{2} \frac{1}{L} e^{-\frac{(1-d_{a2})T_c}{2\tau}} \tilde{f}_{1\alpha}(k+1) \\ &= e^{-\frac{T_c}{2\tau}} \left\{ e^{-\frac{T_c}{2\tau}} \tilde{i}_{2\alpha}(k) + \frac{T_c}{2} \frac{1}{L} e^{-\frac{d_{a1}T_c}{2\tau}} \tilde{f}_{2\alpha}(k) \right\} + \frac{T_c}{2} \frac{1}{L} e^{-\frac{(1-d_{a2})T_c}{2\tau}} \tilde{f}_{1\alpha}(k+1) \\ &= e^{-\frac{T_c}{\tau}} \tilde{i}_{2\alpha}(k) + \frac{T_c}{2} \frac{1}{L} e^{-\frac{(1+d_{a1})T_c}{2\tau}} \tilde{f}_{2\alpha}(k) + \frac{T_c}{2} \frac{1}{L} e^{-\frac{(1-d_{a2})T_c}{2\tau}} \tilde{f}_{1\alpha}(k+1) \end{aligned} \quad (3.4.24)$$

This result is equivalent to the one obtained for the single-phase small-signal model, where output of the sampler $\tilde{i}_\alpha(k+1)$ only depends on the position of the impulse generated by phase A.

Similarly, the discrete-time state equations are derived for the β control loop, in which case the output of the sampler for the rising edge is given by

$$\begin{aligned}
\tilde{i}_{1\beta}(k+1) &= e^{-\frac{T_c}{2\tau}} \tilde{i}_{2\beta}(k) + \frac{T_c}{2\sqrt{3}L} \left(\frac{1}{2} \tilde{f}_{2\alpha}(k) + \frac{\sqrt{3}}{2} \tilde{f}_{2\beta}(k) \right) e^{-\frac{d_{b1}T_c}{2\tau}} \\
&+ \frac{T_c}{2\sqrt{3}L} \left(-\frac{1}{2} \tilde{f}_{2\alpha}(k) + \frac{\sqrt{3}}{2} \tilde{f}_{2\beta}(k) \right) e^{-\frac{d_{c1}T_c}{2\tau}} \\
&= e^{-\frac{T_c}{2\tau}} \tilde{i}_{2\beta}(k) + \frac{T_c}{2\sqrt{3}L} \frac{1}{2} \left(e^{-\frac{d_{b1}T_c}{2\tau}} - e^{-\frac{d_{c1}T_c}{2\tau}} \right) \tilde{f}_{2\alpha}(k) \\
&+ \frac{T_c}{2\sqrt{3}L} \frac{\sqrt{3}}{2} \left(e^{-\frac{d_{b1}T_c}{2\tau}} + e^{-\frac{d_{c1}T_c}{2\tau}} \right) \tilde{f}_{2\beta}(k) \\
&= e^{-\frac{T_c}{2\tau}} \tilde{i}_{2\beta}(k) + \frac{T_c}{4\sqrt{3}L} \left(e^{-\frac{d_{b1}T_c}{2\tau}} - e^{-\frac{d_{c1}T_c}{2\tau}} \right) \tilde{f}_{2\alpha}(k) + \frac{T_c}{4L} \left(e^{-\frac{d_{b1}T_c}{2\tau}} + e^{-\frac{d_{c1}T_c}{2\tau}} \right) \tilde{f}_{2\beta}(k)
\end{aligned} \tag{3.4.25}$$

and for the falling edge by

$$\begin{aligned}
\tilde{i}_{2\beta}(k+1) &= e^{-\frac{T_c}{2\tau}} \tilde{i}_{1\beta}(k+1) + \frac{T_c}{2\sqrt{3}L} \left(\frac{1}{2} \tilde{f}_{1\alpha}(k+1) + \frac{\sqrt{3}}{2} \tilde{f}_{1\beta}(k+1) \right) e^{-\frac{(1-d_{b2})T_c}{2\tau}} \\
&+ \frac{T_c}{2\sqrt{3}L} \left(-\frac{1}{2} \tilde{f}_{1\alpha}(k+1) + \frac{\sqrt{3}}{2} \tilde{f}_{1\beta}(k+1) \right) e^{-\frac{(1-d_{c2})T_c}{2\tau}} \\
&= e^{-\frac{T_c}{2\tau}} \left(e^{-\frac{T_c}{2\tau}} \tilde{i}_{2\beta}(k) + \frac{T_c}{4\sqrt{3}L} \left(e^{-\frac{d_{b1}T_c}{2\tau}} - e^{-\frac{d_{c1}T_c}{2\tau}} \right) \tilde{f}_{2\alpha}(k) + \frac{T_c}{4L} \left(e^{-\frac{d_{b1}T_c}{2\tau}} + e^{-\frac{d_{c1}T_c}{2\tau}} \right) \tilde{f}_{2\beta}(k) \right) \\
&+ \frac{T_c}{2\sqrt{3}L} \left(\frac{1}{2} \tilde{f}_{1\alpha}(k+1) + \frac{\sqrt{3}}{2} \tilde{f}_{1\beta}(k+1) \right) e^{-\frac{(1-d_{b2})T_c}{2\tau}} \\
&+ \frac{T_c}{2\sqrt{3}L} \left(-\frac{1}{2} \tilde{f}_{1\alpha}(k+1) + \frac{\sqrt{3}}{2} \tilde{f}_{1\beta}(k+1) \right) e^{-\frac{(1-d_{c2})T_c}{2\tau}} \\
&= e^{-\frac{T_c}{\tau}} \tilde{i}_{2\beta}(k) + \frac{T_s}{4\sqrt{3}L} \left(e^{-\frac{(1+d_{b1})T_s}{2\tau}} - e^{-\frac{(1+d_{c1})T_s}{2\tau}} \right) \tilde{f}_{2\alpha}(k) + \frac{T_c}{4L} \left(e^{-\frac{(1+d_{b1})T_c}{2\tau}} + e^{-\frac{(1+d_{c1})T_c}{2\tau}} \right) \tilde{f}_{2\beta}(k) \\
&+ \frac{T_c}{4\sqrt{3}L} \left(e^{-\frac{(1-d_{b2})T_c}{2\tau}} - e^{-\frac{(1-d_{c2})T_c}{2\tau}} \right) \tilde{f}_{1\alpha}(k+1) \\
&+ \frac{T_c}{2\sqrt{3}L} \frac{\sqrt{3}}{2} \left(e^{-\frac{(1-d_{b2})T_c}{2\tau}} + e^{-\frac{(1-d_{c2})T_c}{2\tau}} \right) \tilde{f}_{1\beta}(k+1) \\
&= e^{-\frac{T_c}{\tau}} \tilde{i}_{2\beta}(k) + \frac{T_c}{4\sqrt{3}L} \left(e^{-\frac{(1+d_{b1})T_c}{2\tau}} - e^{-\frac{(1+d_{c1})T_c}{2\tau}} \right) \tilde{f}_{2\alpha}(k) + \frac{T_c}{4L} \left(e^{-\frac{(1+d_{b1})T_c}{2\tau}} + e^{-\frac{(1+d_{c1})T_c}{2\tau}} \right) \tilde{f}_{2\beta}(k) \\
&+ \frac{T_c}{4\sqrt{3}L} \left(e^{-\frac{(1-d_{b2})T_c}{2\tau}} - e^{-\frac{(1-d_{c2})T_c}{2\tau}} \right) \tilde{f}_{1\alpha}(k+1) + \frac{T_c}{4L} \left(e^{-\frac{(1-d_{b2})T_c}{2\tau}} + e^{-\frac{(1-d_{c2})T_c}{2\tau}} \right) \tilde{f}_{1\beta}(k+1)
\end{aligned} \tag{3.4.26}$$

From (3.4.25) and (3.4.26) note that the output of the sampler now depends on the impulse generated in both phase B and C. This introduces coupling between the two phases where the β control loop depends on both the phases.

The discrete-time state space equations for the rising and falling edge of the triangular carrier are combined, resulting in discrete-time equivalent state space models defined in

the stationary d-q frame. Equations (3.4.23) and (3.4.24) are expressed in the following vector-matrix notation:

$$\begin{bmatrix} \tilde{i}_{1\alpha}(k+1) \\ \tilde{i}_{2\alpha}(k+1) \end{bmatrix} = \begin{bmatrix} 0 & e^{-\frac{T_c}{2\tau}} \\ 0 & e^{-\frac{T_c}{\tau}} \end{bmatrix} \begin{bmatrix} \tilde{i}_{1\alpha}(k) \\ \tilde{i}_{2\alpha}(k) \end{bmatrix} + \begin{bmatrix} \frac{T_c}{2} \frac{1}{L} e^{-\frac{d_{a1}T_c}{2\tau}} & 0 \\ \frac{T_c}{2} \frac{1}{L} e^{-\frac{(1+d_{a1})T_c}{2\tau}} & \frac{T_c}{2} \frac{1}{L} e^{-\frac{(1-d_{a2})T_c}{2\tau}} \end{bmatrix} \begin{bmatrix} \tilde{f}_{2\alpha}(k) \\ \tilde{f}_{1\alpha}(k+1) \end{bmatrix}$$

with

$$\mathbf{F}_\alpha = \begin{bmatrix} 0 & e^{-\frac{T_c}{2\tau}} \\ 0 & e^{-\frac{T_c}{\tau}} \end{bmatrix}, \mathbf{G}_\alpha = \begin{bmatrix} \frac{T_c}{2} \frac{1}{L} e^{-\frac{d_{a1}T_c}{2\tau}} & 0 \\ \frac{T_c}{2} \frac{1}{L} e^{-\frac{(1+d_{a1})T_c}{2\tau}} & \frac{T_c}{2} \frac{1}{L} e^{-\frac{(1-d_{a2})T_c}{2\tau}} \end{bmatrix}$$

Similarly the vector-matrix notation is used to express the β -coordinate,

$$\begin{bmatrix} \tilde{i}_{1\beta}(k+1) \\ \tilde{i}_{2\beta}(k+1) \end{bmatrix} = \begin{bmatrix} 0 & e^{-\frac{T_c}{2\tau}} \\ 0 & e^{-\frac{T_c}{\tau}} \end{bmatrix} \begin{bmatrix} \tilde{i}_{1\beta}(k) \\ \tilde{i}_{2\beta}(k) \end{bmatrix} + \begin{bmatrix} \frac{T_c}{4} \frac{1}{L} \left(e^{-\frac{d_{b1}T_c}{2\tau}} + e^{-\frac{d_{c1}T_c}{2\tau}} \right) & 0 \\ \frac{T_c}{4} \frac{1}{L} \left(e^{-\frac{(1+d_{b1})T_c}{2\tau}} + e^{-\frac{(1+d_{c1})T_c}{2\tau}} \right) & \frac{T_c}{4} \frac{1}{L} \left(e^{-\frac{(1-d_{b2})T_c}{2\tau}} + e^{-\frac{(1-d_{c2})T_c}{2\tau}} \right) \end{bmatrix} \begin{bmatrix} \tilde{f}_{2\beta}(k) \\ \tilde{f}_{1\beta}(k+1) \end{bmatrix} + \begin{bmatrix} \frac{T_c}{4\sqrt{3}} \frac{1}{L} \left(e^{-\frac{d_{b1}T_c}{2\tau}} - e^{-\frac{d_{c1}T_c}{2\tau}} \right) & 0 \\ \frac{T_c}{4\sqrt{3}} \frac{1}{L} \left(e^{-\frac{(1+d_{b1})T_c}{2\tau}} - e^{-\frac{(1+d_{c1})T_c}{2\tau}} \right) & \frac{T_c}{4\sqrt{3}} \frac{1}{L} \left(e^{-\frac{(1-d_{b2})T_c}{2\tau}} - e^{-\frac{(1-d_{c2})T_c}{2\tau}} \right) \end{bmatrix} \begin{bmatrix} \tilde{f}_{2\alpha}(k) \\ \tilde{f}_{1\alpha}(k+1) \end{bmatrix}$$

with

$$\mathbf{F}_\beta = \begin{bmatrix} 0 & e^{-\frac{T_c}{2\tau}} \\ 0 & e^{-\frac{T_c}{\tau}} \end{bmatrix}, \mathbf{G}_\beta = \begin{bmatrix} \frac{T_c}{4} \frac{1}{L} \left(e^{-\frac{d_{b1}T_c}{2\tau}} + e^{-\frac{d_{c1}T_c}{2\tau}} \right) & 0 \\ \frac{T_c}{4} \frac{1}{L} \left(e^{-\frac{(1+d_{b1})T_c}{2\tau}} + e^{-\frac{(1+d_{c1})T_c}{2\tau}} \right) & \frac{T_c}{4} \frac{1}{L} \left(e^{-\frac{(1-d_{b2})T_c}{2\tau}} + e^{-\frac{(1-d_{c2})T_c}{2\tau}} \right) \end{bmatrix},$$

$$\mathbf{H}_\beta = \begin{bmatrix} \frac{T_c}{4\sqrt{3}} \frac{1}{L} \left(e^{-\frac{d_{b1}T_c}{2\tau}} - e^{-\frac{d_{c1}T_c}{2\tau}} \right) & 0 \\ \frac{T_c}{4\sqrt{3}} \frac{1}{L} \left(e^{-\frac{(1+d_{b1})T_c}{2\tau}} - e^{-\frac{(1+d_{c1})T_c}{2\tau}} \right) & \frac{T_c}{4\sqrt{3}} \frac{1}{L} \left(e^{-\frac{(1-d_{b2})T_c}{2\tau}} - e^{-\frac{(1-d_{c2})T_c}{2\tau}} \right) \end{bmatrix}$$

Combining the the α and β loops discrete-time equivalent state space equations results in

$$\begin{bmatrix} \tilde{i}_{1\alpha}(k+1) \\ \tilde{i}_{2\alpha}(k+1) \\ \tilde{i}_{1\beta}(k+1) \\ \tilde{i}_{2\beta}(k+1) \end{bmatrix} = \begin{bmatrix} \mathbf{F}_\alpha & 0 \\ 0 & \mathbf{F}_\beta \end{bmatrix} \begin{bmatrix} \tilde{i}_{1\alpha}(k) \\ \tilde{i}_{2\alpha}(k) \\ \tilde{i}_{1\beta}(k) \\ \tilde{i}_{2\beta}(k) \end{bmatrix} + \begin{bmatrix} \mathbf{G}_\alpha & 0 \\ \mathbf{H}_\beta & \mathbf{G}_\beta \end{bmatrix} \begin{bmatrix} \tilde{f}_{2\alpha}(k) \\ \tilde{f}_{1\alpha}(k+1) \\ \tilde{f}_{2\beta}(k) \\ \tilde{f}_{1\beta}(k+1) \end{bmatrix}$$

This discrete-time equivalent state space model is used in the next section to design different current regulators for single- and three phase current regulators.

3.5 Simulation of PWM Small-Signal Model State Space Equations

The equations derived for the single- and three phase PWM small-signal models are simulated with Matlab© and compared to a Simulink© simulation to determine the

accuracy of the equations. A Matlab© m-file is written to iterate through the state space equations for five cycles of the switching period. The state space equations calculate the output which is plotted for each sample period. The m-file is then compared to a Simulink© simulation wherein the small-signal model is represented by an impulse generator. The parameters used are summarized in Table 3.1.

Table 3.1: System parameters

Inverter parameters	
Load Inductance (L)	20 mH
Load Resistance (R)	1 Ω
DC-bus voltage (V_d)	10 V
Switching frequency (f_c)	1 kHz
Sample frequency (f_s)	2 kHz

Figure 3.14 shows the simulation of the single-phase small-signal model. We can see that the state space equations is able to follow the simulated waveform precisely.

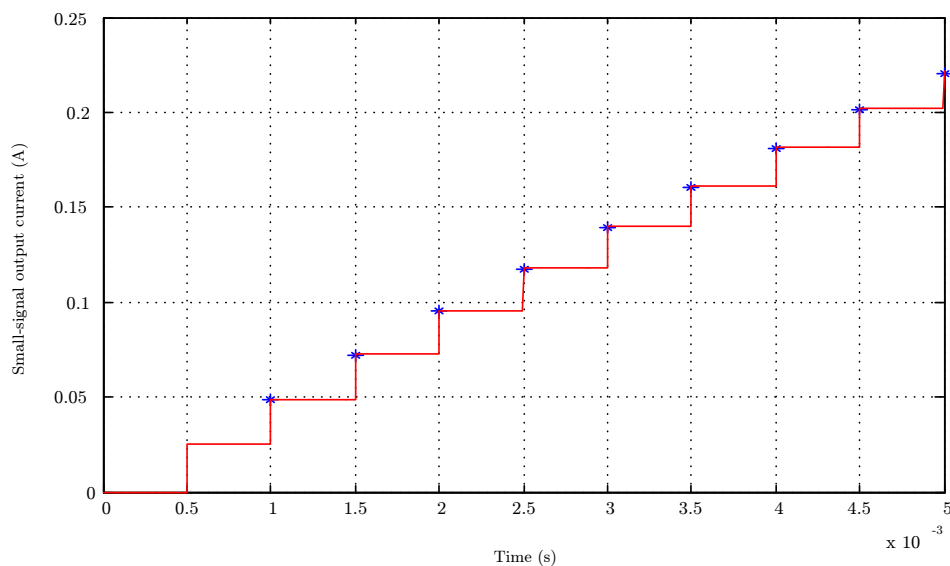


Figure 3.14: Matlab© simulations to test accuracy for single-phase small-signal model, $d_1 = 0.8$ and $d_2 = 0.4$.

3.6 Summary

This chapter discussed the mathematical derivation for the single and three-phase small-signal models for asymmetrical regular sampled pulse-width modulator control loops, where the duty cycle differs for the first and second half of the switching period. Dummy

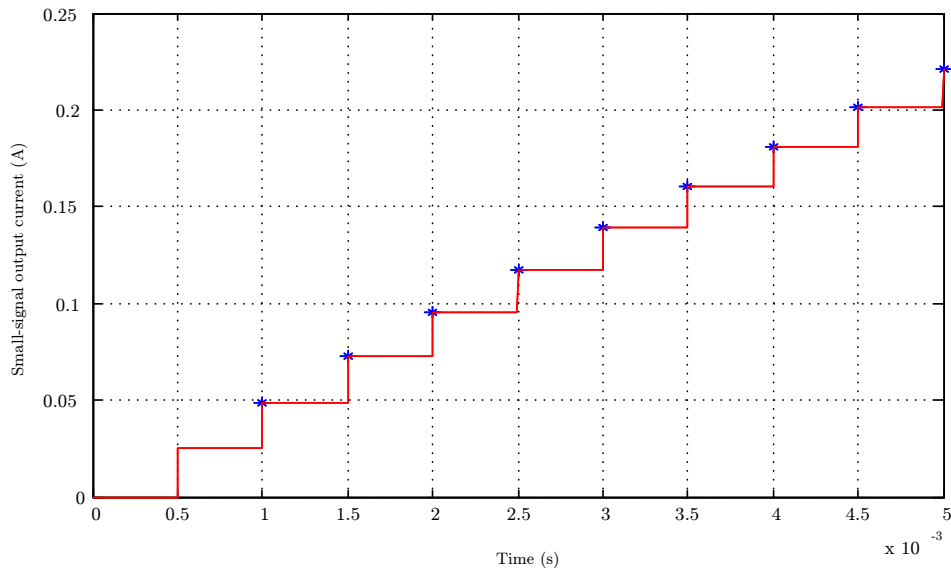
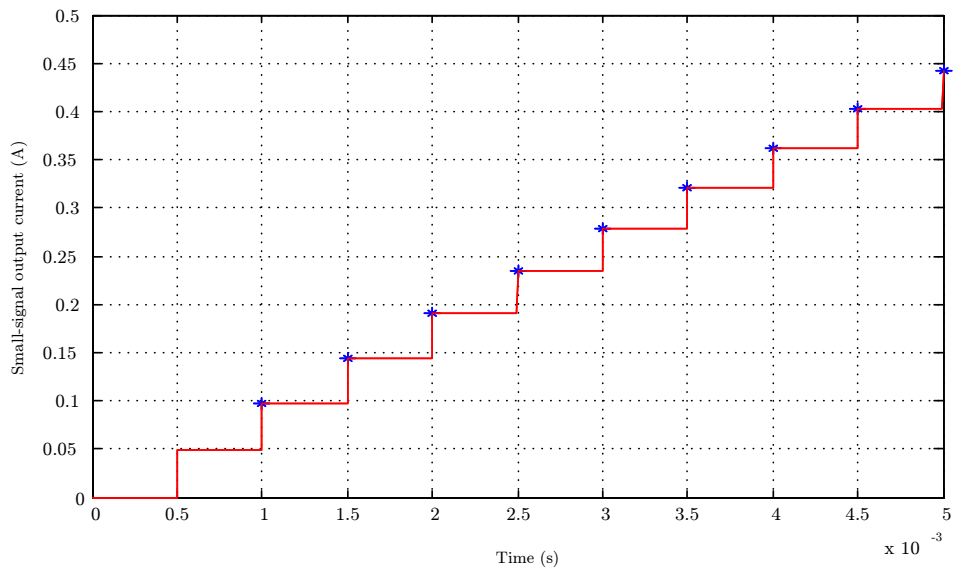
(a) α control loop(b) β control loop

Figure 3.15: Matlab© simulations to test accuracy for three-phase small-signal model, $d_a = 0.8$, $d_b = 0.6$ and $d_c = 0.4$.

state variables was introduced to find a discrete-time state space small-signal model solutions. The three-phase small-signal model was implemented in the stationary d-q frame. A Matlab© simulation is used to iterate through the solutions and to verify their accuracy.

Chapter 4

Derivation of Discrete-Time Equivalent State Space Models for Various Current Regulators

4.1 Introduction

The aim of this chapter is to show how the small-signal models derived in chapter 3 can be used in conjunction with different current regulators to analyse the closed loop stability. In the following section the small-signal models derived in chapter 3 are extended for both linear proportional (P) current regulator, as well as a proportional integral (PI) current regulator. However, its not limited to only these two current regulators, there exist many different current regulator techniques that is already well established that could also be used [19].

The closed loop stability of the single and three-phase systems are analysed by adding either a P or PI current regulator and an one sample period computation delay [16] into the closed loop system. The open loop state space equations derived in chapter 3 are extended to find the closed loop state space model system matrices. From the system matrices the eigenvalues of the closed loop system are calculated to find the closed loop poles.

The same notation introduced in chapter 3 is used in this chapter, where the subscript 1 and 2 indicates the discrete-time state space equations for the first and second halves of the switching period respectively.

In the following sections the closed loop system matrices are calculated for both P and PI current regulators using the small-signal models derived in the previous chapter. In section 4.4 design strategy used to calculate the optimal gains for the PI current regulator

used in the thesis is also described in more detail.

4.2 Proportional Current Regulator

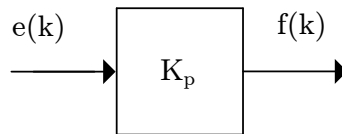


Figure 4.1: Discrete-time proportional current regulator.

Proportional current regulator is the most basic form of a controller. It is not customary to implement a proportional current regulator on its own, but rather together with an integral controller or a resonant controller. To demonstrate how different controllers can be implemented using the discrete-time state space models defined in chapter 3 a proportional current regulator will be used initially.

The proportional current regulator consist of only a proportional gain term K_p . Figure 4.1 shows a discrete-time proportional current regulator, where the output of the current regulator $f(k)$ is simply proportional to the error signal $e(k)$. The output of the proportional current regulator for both halves of the switching period is given by:

$$\begin{aligned} f_1(k+1) &= K_p e_1(k+1) \\ &= K_p \left(i_1^*(k+1) - i_1(k+1) \right) \end{aligned} \quad (4.2.1)$$

$$\begin{aligned} f_2(k) &= K_p e_2(k) \\ &= K_p \left(i_2^*(k) - i_2(k) \right) \end{aligned} \quad (4.2.2)$$

4.2.1 Single-Phase Small-Signal Model

Substituting (4.2.1) and (4.2.2) into the discrete-time equivalent small-signal model derived in the section 3.3, the system matrices of the closed loop system are obtained for

a single-phase proportional current regulator. The closed loop discrete-time state space model is simulated in a Matlab© m-file and compared to a Simulink© model to determine the accuracy of the system matrices obtained - see Figure A.1. In section A.1 the derivation procedure is shown in more detail. The closed loop system matrices are determined to be

$$\mathbf{F} = \begin{bmatrix} F_{12} & -G_{11}K_p \\ 0 & F_{22} - G_{21}K_p \end{bmatrix}; \mathbf{G} = \begin{bmatrix} 1 & 0 \\ G_{22}K_p & 1 \end{bmatrix}$$

where the values of F_{12} , F_{22} , G_{11} , G_{21} and G_{22} are given by Table 4.1

Table 4.1: Open loop matrix variables for single-phase RL-load

$F_{12} = e^{-\frac{T_c}{2\tau}}$	$G_{21} = \frac{T_c}{2L} e^{-\frac{(1+d_1)T_c}{2\tau}}$
$F_{22} = e^{-\frac{T_c}{\tau}}$	$G_{22} = \frac{T_c}{2L} e^{\frac{(1-d_2)T_c}{2\tau}}$
$G_{11} = \frac{T_c}{2L} e^{-\frac{d_1 T_c}{2\tau}}$	

4.2.2 Three-Phase Small-Signal Model

Substituting (4.2.1) and (4.2.2) into both the discrete-time small-signal models of the α and β control loop state space equations derived in section 3.4, the system matrices of the closed loop system are obtained for the three-phase proportional current regulator implemented in the stationary d-q frame. In section A.1 the derivation procedure is shown in more detail. The closed loop system matrices are determined to be

$$\mathbf{F} = \begin{bmatrix} 0 & F_{21} - G_{11}K_p & 0 & 0 \\ 0 & F_{22} - G_{21}K_p & 0 & 0 \\ 0 & -G_{31}K_p & 0 & F_{34} - G_{33}K_p \\ 0 & -G_{41}K_p & 0 & F_{44} - G_{43}K_p \end{bmatrix}; \mathbf{G} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ G_{22}K_p & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ G_{42}K_p & 0 & G_{44}K_p & 1 \end{bmatrix}$$

where the values of F_{12} , F_{34} , F_{22} , F_{44} , G_{11} , G_{21} , G_{22} , G_{31} , G_{41} , G_{42} , G_{33} , G_{43} and G_{44} are given by Table 4.2

4.3 Proportional Integral Current Regulator

The proportional controller from the previous section is now used together with an integral controller to construct a PI current regulator. The effect of the one sample period computational delay is also included. The addition of the integral term improves the

Table 4.2: Open loop matrix variables for three-phase RL-load

$F_{12} = F_{34} = e^{-\frac{T_c}{2\tau}}$	$G_{41} = \frac{T_c}{4} \frac{1}{L} (e^{-\frac{(1+d_{b1})T_c}{2\tau}} + e^{-\frac{(1+d_{c1})T_c}{2\tau}})$
$F_{22} = F_{44} = e^{-\frac{T_c}{\tau}}$	$G_{42} = \frac{T_c}{4} \frac{1}{L} (e^{-\frac{(1-d_{b2})T_c}{2\tau}} + e^{-\frac{(1-d_{c2})T_c}{2\tau}})$
$G_{11} = \frac{T_c}{2} \frac{1}{L} e^{-\frac{d_{a1}T_c}{2\tau}}$	$G_{33} = \frac{T_c}{4\sqrt{3}} \frac{1}{L} (e^{-\frac{d_{b1}T_c}{2\tau}} - e^{-\frac{d_{c1}T_c}{2\tau}})$
$G_{21} = \frac{T_c}{2} \frac{1}{L} e^{-\frac{(1+d_{a1})T_c}{2\tau}}$	$G_{43} = \frac{T_c}{4\sqrt{3}} \frac{1}{L} (e^{-\frac{(1+d_{b1})T_c}{2\tau}} - e^{-\frac{(1+d_{c1})T_c}{2\tau}})$
$G_{22} = \frac{T_c}{2} \frac{1}{L} e^{-\frac{(1-d_{a2})T_c}{2\tau}}$	$G_{44} = \frac{T_c}{4\sqrt{3}} \frac{1}{L} (e^{-\frac{(1-d_{b2})T_c}{2\tau}} - e^{-\frac{(1-d_{c2})T_c}{2\tau}})$
$G_{31} = \frac{T_c}{4} \frac{1}{L} (e^{-\frac{d_{b1}T_c}{2\tau}} + e^{-\frac{d_{c1}T_c}{2\tau}})$	

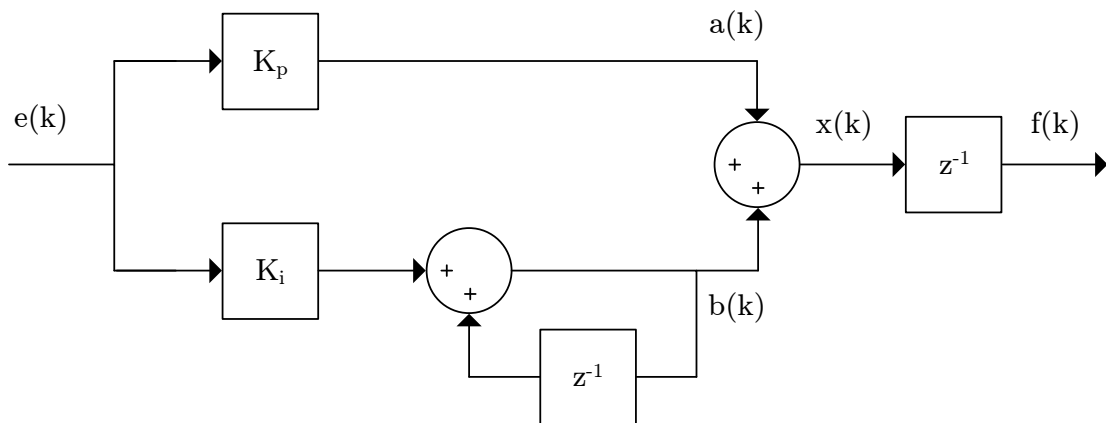


Figure 4.2: Discrete-time proportional integral current regulator.

tracking performance of the current regulator and minimizes the steady-state error [20]. Figure 4.2 shows the block diagram of a discrete-time PI current regulator.

A PI current regulator is first implemented for a single-phase DC-AC system before being extended to a three-phase DC-AC system, implemented in the stationary d-q frame.

The PI current regulator is separated into its proportional and integral terms. The output of the integral term depends on the current value of the error signal $e(k)$ multiplied by the integral gain K_i plus the previous error signal value. Therefore, the output of the integral term $b(k)$ for both halves of the switching period is given by

$$\begin{aligned} b_1(k+1) &= b_2(k) + K_i e_1(k+1) \\ &= b_2(k) + K_i (i_1^*(k+1) - i_1(k+1)) \end{aligned} \quad (4.3.1)$$

$$\begin{aligned} b_2(k+1) &= b_1(k+1) + K_i e_2(k+1) \\ &= b_1(k+1) + K_i (i_2^*(k+1) - i_2(k+1)) \end{aligned} \quad (4.3.2)$$

The output proportional term $a(k)$ simply multiplies the current error signal $e(k)$ with a proportional gain K_p and results in

$$\begin{aligned} a_1(k+1) &= K_p e_1(k+1) \\ &= K_p \left(i_1^*(k+1) - i_1(k+1) \right) \end{aligned} \quad (4.3.3)$$

$$\begin{aligned} a_2(k+1) &= K_p e_2(k+1) \\ &= K_p \left(i_2^*(k+1) - i_2(k+1) \right) \end{aligned} \quad (4.3.4)$$

The summation of the outputs for the integral terms (4.3.1),(4.3.2) and the outputs of the proportional terms (4.3.3),(4.3.4) results in the output of the PI current regulator $x(k)$, which is given by

$$\begin{aligned} x_1(k+1) &= a_1(k+1) + b_1(k+1) \\ &= b_2(k) + (K_p + K_i) i_1^*(k+1) - (K_p + K_i) i_1(k+1) \end{aligned} \quad (4.3.5)$$

$$\begin{aligned} x_2(k+1) &= a_2(k+1) + b_2(k+1) \\ &= b_1(k+1) + (K_p + K_i) i_2^*(k+1) - (K_p + K_i) i_2(k+1) \end{aligned} \quad (4.3.6)$$

The output of the one sample period computational delay $f(k)$ is given by

$$f_1(k+1) = x_2(k) \quad (4.3.7)$$

$$f_2(k+1) = x_1(k+1) \quad (4.3.8)$$

Substituting (4.3.5),(4.3.6) and (4.3.7),(4.3.8) into the discrete-time state space equations of the small-signal models derived in chapter 3 the closed loop system matrices are obtained. Two additional state variables ($x(k)$ and $b(k)$) are included in the closed loop state space model, because of the integral term and the computational delay.

4.3.1 Single-Phase Small-Signal model

Substituting (4.3.7) and (4.3.7) into the discrete-time small-signal model derived in section 3.3, a closed loop state space model is obtained. In section A.1.3.1 the calculations is given

in more detail, together with a Matlab© m-file and Simulink© simulation showing that the single-phase small-signal model implemented with the PI current regulator is able to track the simulation accurately - see Figure A.3. The closed loop system matrices are determined to be

$$\mathbf{F} = \begin{bmatrix} 0 & F_{12} & 0 & 0 & 0 & 0 & 0 & G_{11} \\ 0 & F_{22} & 0 & 0 & 0 & 0 & 0 & G_{21} \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}; \mathbf{G} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & -G_{22} & 0 \\ K_{tot} & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & K_{tot} & 0 & 1 & -1 & 0 & 0 & 0 \\ K_i & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & K_i & 0 & 0 & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

where F_{12} , F_{22} , G_{11} , G_{21} , G_{22} are given by Table 4.1 and $K_{tot} = K_i + K_p$.

4.3.2 Three-Phase Small-Signal Model

For a three-phase DC-AC system, the equations derived in section 4.3.1 can be extended for the α and β open loop state space models derived in section 3.4. For a three-phase system the size of the system matrices becomes very large as more state variables are added. This is caused by the three-phase system represented by both α and β control loops.

Substituting (4.3.7) and (4.3.8) into the discrete-time small-signal model derived in section 3.4, a closed loop state space model is obtained. In section A.2.3.1 the calculations are given in more detail, together with a Matlab Simulink© simulation showing that the three-phase small-signal model implemented with the PI current regulator is able to track the simulation accurately - see Figure A.6. The closed loop system matrices are determined to be

$$\mathbf{F} = \begin{bmatrix}
 0 & F_{12} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & G_{11} & 0 & 0 \\
 0 & F_{22} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & G_{21} & 0 & 0 \\
 0 & 0 & 0 & F_{34} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & G_{33} & 0 & G_{31} \\
 0 & 0 & 0 & F_{44} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & G_{43} & 0 & G_{41} \\
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
 \end{bmatrix}$$

$$\mathbf{G} = \begin{bmatrix}
 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -G_{22} & 0 & 0 & 0 \\
 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -G_{44} & 0 & -G_{42} & 0 \\
 K_{tot} & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & K_{tot} & 0 & 0 & 0 & 1 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & K_{tot} & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & K_{tot} & 0 & 0 & 0 & 1 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 \\
 K_i & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & K_i & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & K_i & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & K_i & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 1 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\
 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1
 \end{bmatrix}$$

where F_{12} , F_{34} , F_{22} , F_{44} , G_{11} , G_{21} , G_{22} , G_{31} , G_{41} , G_{42} , G_{33} , G_{43} , G_{44} are given by Table 4.2 and $K_{tot} = K_i + K_p$.

4.4 Design Strategy for Proportional Integral Current Regulator

In [10] an analytical method is introduced to determine the optimal gain values for a stationary frame three phase PI current regulator. In terms of basic linear analysis a PI current regulated system is defined as a second order system with no theoretical stability limits as the gains are increased [10]. However, in [21] it is shown that the second order effects do contribute to the stability of the system. This analytical method incorporates the transport and computational delays of the system in the open loop design of the controller gains to compensate for the effects of the delay.

The transport and computational delays mentioned in section 2.2 will be used in this design. It is defined as three-quarters of the carrier period, i.e. $T_d = 0.75T_c$ [10].

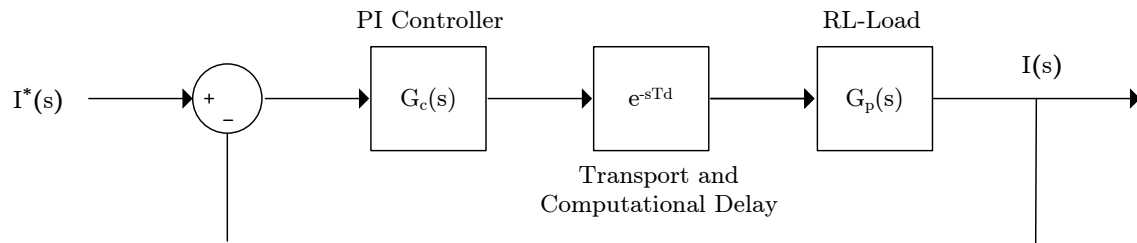


Figure 4.3: The closed loop system is a representation of each independent controlled phase current. The transport and computational delays effects are included.

An open loop design is used to find the optimal gain values for the stationary PI current regulator in the continuous-time domain. The closed loop representation is shown in Figure 4.3. The continuous-time domain transfer function for a simple PI current regulator is given by

$$G_c(s) = K_p + \frac{K_i}{s} \quad (4.4.1)$$

To use this controller as an AC current regulator, the proportional gain K_p and the integral gain K_i should be made as large as possible [10]. This would maximize the magnitude of $G_c(s)$ and thus minimize the reference and tracking errors.

For the RL-load the plant transfer function is defined by

$$G_p(s) = V_{dc} \left(\frac{1}{R + sL} \right) \quad (4.4.2)$$

Adding the transport- and computational delays the open loop transfer function becomes

$$G_c(s)G_p(s) = \frac{K_i V_{dc} (1 + s \frac{K_p}{K_i}) e^{-sT_d}}{R s(1 + s \frac{L}{R})} \quad (4.4.3)$$

If the effect of the delay is neglected in (4.4.3), the open loop system have one zero at $s = -\frac{1}{\tau_i}$ and two poles, at the origin ($s = 0$) and at $s = -\frac{R}{L}$.

However, if the delay term e^{-sT_d} is included its poles and zeros locations can be predicted by the first order Padé approximation shown in (4.4.4). According to (4.4.4) the effect of the delay can be described by a zero-pole pair. Another zero at $s = \frac{2}{T_d}$ and a pole at $s = -\frac{2}{T_d}$ is added to the open loop system.

$$e^{-sT_d} = \frac{(1 - s \frac{T_d}{2})}{(1 + s \frac{T_d}{2})} \quad (4.4.4)$$

The open loop system therefore has two open-loop zeros and three open-loop poles.

The additional delays therefore contributes to the phase margin of the system which would also contribute to the stability of the system. The goal therefore is to increase the proportional gain K_p and integral gain K_i , while retaining the phase margin ϕ_m . According to [10] a phase margin of 40° is an appropriate target to achieve an acceptable damped system response. The controller gains are therefore designed to achieve a phase margin of more or less 40° .

The phase angle at the cross-over frequency w_c is given by

$$\begin{aligned} \angle\{G_c(jw_c)G_p(jw_c)\} &= \angle\left\{K_i \frac{V_{dc}}{R} \frac{(1 + jw_c \frac{K_p}{K_i}) e^{-jw_c T_d}}{s(1 + jw_c \frac{L}{R})}\right\} \\ &= -\pi + \phi_m \\ &= \tan^{-1}(w_c \frac{K_p}{K_i}) - \frac{\pi}{2} - w_c T_d - \tan^{-1}(w_c \frac{L}{R}) \end{aligned} \quad (4.4.5)$$

Assuming that the plant pole frequency is well below the value of the cross-over frequency w_c , the angular contribution of $\tan^{-1}(w_c \frac{L}{R})$ can be approximated by $\frac{\pi}{2}$. The phase margin ϕ_m can then be approximated by

$$\phi_m \approx \tan^{-1}(w_c \frac{K_p}{K_i}) - w_c T_d \quad (4.4.6)$$

Intuitively we know that the maximum proportional gain K_p will occur at the maximum cross-over frequency. To find the maximum cross-over frequency, (4.4.6) can be manipulated to be equal to

$$w_{c(max)} = \frac{\frac{\pi}{2} - \phi_m}{T_d} \quad (4.4.7)$$

where the maximum cross-over frequency will occur when $\tan^{-1}(w_c \frac{K_p}{K_i}) = \frac{\pi}{2}$.

If the open loop gain is set to unity at the maximum cross-over frequency $w_{c(max)}$, the maximum possible value of K_p can be expressed as,

$$\begin{aligned} |G_c(s)G_p(s)|_{s=jw_{c(max)}} &= 1 \\ \therefore K_p &= \frac{RK_p}{V_{dc}K_i} w_{c(max)} \sqrt{\frac{(1 + w_{c(max)}^2 (\frac{L}{R})^2)}{(1 + w_{c(max)}^2 (\frac{K_p}{K_i})^2)}} \end{aligned} \quad (4.4.8)$$

It is assumed that $w_{c(max)}\tau_i \gg 1$ and $w_{c(max)}T_p \gg 1$, which is usually the case for current regulated systems [10]. The maximum value of K_p can then be approximated by (4.4.9), which is dependent on the series load inductance, L , the dc bus voltage, V_{dc} and the maximum cross-over frequency, $w_{c(max)}$.

$$K_p \approx \frac{w_{c(max)}L}{V_{dc}} \quad (4.4.9)$$

The same assumption used in (4.4.7) can be applied, with $\tan^{-1}(w_c\tau_i) \approx \frac{\pi}{2}$, leading to, after substitution into (4.4.9):

$$K_i \approx \frac{w_{c(max)}K_p}{10} \quad (4.4.10)$$

In the rest of the thesis the controller gains will be calculated using (4.4.9) and (4.4.10) for a PI current regulator.

4.5 Summary

In this chapter the discrete-time closed loop system matrices have been calculated for a P and PI current regulator implemented in a single-phase system as well as a three-phase

system. From the eigenvalues of system matrices the stability for the closed loop systems can be determined.

The system matrices are determined for both P and PI current regulators used in single and three-phase systems. Matlab© and Simulink© simulations are used to verify the accuracy of the discrete-time state space models obtained for each of these current regulators.

Also a design strategy is introduced in section 4.4 that will be used in the following section to calculate the optimal proportional K_p and integral gains K_i for a PI current regulated system.

Chapter 5

Model Verification

5.1 Introduction

This chapter presents a comparison between the accuracy of the asymmetrical regular sampled pulse-width modulator small-signal models derived in Chapter 3 and the zero-order hold model [16] commonly used when designing DC-AC current regulator systems. The controller design strategy in section 4.4 is used to design the single and three-phase current regulator systems for a series RL-load.

The zero-order hold model was first used in [6], where the derivation of an asymmetrical regular sampled pulse-width modulator small-signal model [11] is simplified. The approach to use the zero-order hold as representation of the small-signal model for the pulse-width modulator simplifies the process to design current regulators for both single and three-phase systems. An example of the zero-order hold method used can be seen in [16].

However, by using the zero-order hold model, information regarding the position of the impulses represented by the small-signal model is ignored. The effect this would have on the stability of a single-phase closed loop system is analysed in section 5.2. In [16] the zero-order model is used in the design of a balanced three-phase system, where the three-phase load is connected through a floating star point. The three-phase system is implemented in the stationary d-q frame, where it is assumed that the stability of the three-phase system is only dependent on the stability of the α loop and not the β loop. This assumption is based on an average model, where the small-signal model is essentially an instantaneous model dependent on generating impulses based on the duty cycle values. The accuracy of this assumption is analysed further in section 5.3, based on its effect on the stability of the closed loop system.

The aim of this chapter is to investigate if the zero-order hold model is an accurate model

and to determine when it will become an unreliable small-signal model for both single and three-phase systems. Simulations based in Matlab[®] are used to verify the accuracy of the individual small-signal models, the zero-order hold model and the discrete-time state space models derived in chapter 3. By comparing the gain margins predicted by the individual small-signal models to a gain margin, obtained by simulation of the practical system, it can be established which one is more accurate. The gain margin is defined by the total additional loop gain to be added into a loop before the system becomes unstable. In [22] a stable system is defined as follows: a condition if and only if every bounded input sequence produces a bounded output sequence.

Two different approaches are used to investigate the inaccuracy of the zero-order hold model, a bifurcation diagram and a root locus plot. For the root locus plot the closed loop poles describe the stability of a system and therefore only they would be plotted.

A bifurcation diagram is used to analyse the stability of the system, where the loop gain of the practical closed loop system is increased by small increments until the system diverges and instability is reached. As the loop gain is increased, the input to the PWM is measured, a measuring point where the bifurcation is best determined. By increasing the loop gain by small increments and observing the duty cycle of the system, we are able to construct a bifurcation diagram with the bifurcation point indicating the gain margin value of the system.

A root locus plot is used to observe the closed loop system poles of the individual small-signal models. Again the loop gain is incremented while the closed loop poles are plotted on a root locus diagram. The value of the loop gain at which the closed loop poles exit the unit circle of the root locus, represents the value of the gain margin of the system.

Comparing the gain margin of the individual small-signal models to the gain margin determined by the bifurcation diagrams, it can be decided which small-signal model is most accurate. The system parameters used in this chapter are given in Table 5.1. The design method introduced in section 4.4 is used to calculate the stationary PI current regulator gains.

A z-domain closed loop transfer function is derived for a single-phase system, using the zero-order hold model. The discrete-time PI controller transfer function is given by,

$$G_c(z) = (K_p + K_i) \frac{z - \frac{K_p}{K_p + K_i}}{z - 1} \quad (5.1.1)$$

The RL-load, s-domain transfer function is discretized, using the zero-order hold method, resulting in

Table 5.1: System parameters and controller gains

Inverter parameters	
Load Inductance (L)	1 mH
Load Resistance (R)	1 Ω
DC-bus voltage (V_d)	200 V
Switching frequency (f_c)	625 Hz
Sample frequency (f_s)	1250 Hz
Controller gains	
K_i	$0.5288T_s$
K_p	0.0073

$$G_p(z) = \frac{1}{R} \frac{1 - e^{-\frac{T_s}{\tau}}}{z - e^{-\frac{T_s}{\tau}}} \quad (5.1.2)$$

A z-domain open loop transfer function is obtained by multiplying (5.1.1) and (5.1.2) with the computational delay and half the DC-bus voltage V_{dc} . The gain K represents the additional gain used to increase the loop gain.

$$G_{ol}(z) = G_c(z) \times G_p(z) \times V_d \times \frac{1}{z} \times K \quad (5.1.3)$$

From the z-domain open loop transfer function the closed loop transfer function can be described by,

$$G_{cl}(z) = \frac{G_c(z) \times G_p(z) \times V_d \times K}{G_c(z) \times G_p(z) \times V_d \times \frac{1}{z} \times K + 1} \quad (5.1.4)$$

Now the closed loop poles are obtained from the roots of the closed loop transfer functions denominator. A simulation in Matlab[©] is used to calculate the roots and to construct the root locus plot of the closed loop poles. In the simulation the loop gain is gradually increased from 1 to 10, linearly over 30000 data points, and as the loop gain is increased the closed loop poles move towards the unit circle as shown in Figure 5.1. The instant when the closed loop exit the unit circle determines the gain margin. The gain margin for the root locus of the zero-order hold model in Figure 5.1 is calculated to be 2.3960.

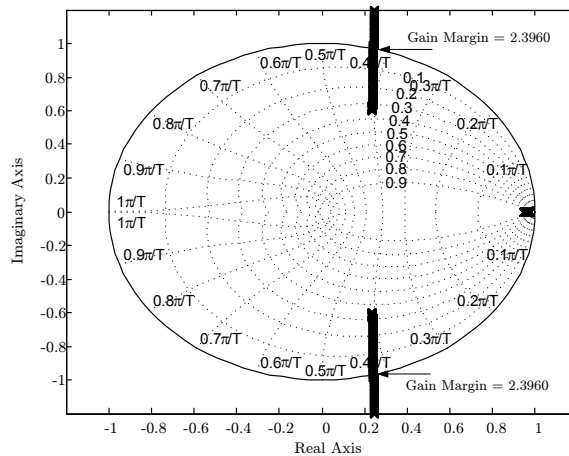


Figure 5.1: Root locus of zero-order hold model.

Also important to remember the zero-order hold model does not take into consideration a change in the duty cycle.

A similar analysis is done with the small-signal models derived in chapter 3 to determine which one is more accurate.

5.2 Single-Phase Small-Signal Model

The single-phase asymmetrical sampled pulse-width modulator small-signal model derived in section 3.3 is now applied to a PI current regulator to obtain a closed loop expression for the system. In section A.1.3 the derivation process to determine the closed loop system is discussed in more detail. The closed loop system is expressed in a discrete-time state space model form, similar to (5.2.1).

$$\mathbf{x}(k+1) = \mathbf{F}\mathbf{x}(k) + \mathbf{h}u(k) \quad (5.2.1)$$

where \mathbf{F} is the system matrix.

The closed loop poles of the state space system can be determined by,

$$|z\mathbf{I} - \mathbf{F}| = 0 \quad (5.2.2)$$

Equation (5.2.2) is the same equation used to calculate the eigenvalues of the system matrix \mathbf{F} [17]. Similar to the zero-order hold model, a root locus plot of the closed loop poles can be constructed for the single-phase small-signal model by calculating the

eigenvalues of the system matrix. Unlike the zero-order hold model, this small-signal model is able to take into consideration the changes in the duty cycle values.

A simulation in Matlab© of the discrete-time control loop is used where the loop gain is increased gradually over 6000 switching periods from 1 to 2.5. The duty cycle is then measured and stored in an array twice over the one switching period. Another simulation is then used which import these duty cycle values into the discrete-time equivalent small-signal state space models. From the closed loop form the eigenvalues of the system matrix are calculated, solving the closed loop pole positions. A root locus is then constructed from the position of the closed loop poles.

Again the gain margin is determined from the value of the loop gain at the instant when the closed loop poles exit the unit circle. To analyse the influence the duty cycle will have on the stability of the single-phase system a few simulations were done using different current reference values. It is also important to note that, according to the zero-order hold model, the duty cycle has a no effect on the stability of the closed loop system.

In Figure 5.2 it can be seen that a change in duty cycle does influence the gain margin of a single-phase current regulated system. Figure 5.2d shows that for large current reference value (also a large duty cycle) the gain margin of the system becomes more dependent on the duty cycle values.

In the following section these predicted gain margins are compared to the bifurcation simulations of a practical system.

5.2.1 Gain Margin

The accuracy of the small-signal model can be verified by comparing the gain margin predicted by the small-signal model to the gain margin of a practical simulation of the system. A bifurcation diagram is used to predict the gain margin of the practical system. By slowly ramping up the loop gain and analysing the duty cycle, a bifurcation diagram can be constructed to analyse the stability of the system.

A Matlab© simulation is used to analyse the behaviour of the practical simulation. In the simulation an additional gain K is added before the input to the pulse-width modulator to increase the loop gain. The value of K at which the instability occurs, identifies the value of the gain margin of the system. For the system to avoid going straight into unstable operation, the loop gain should be incremented slowly. In simulation the loop gain is increased from 1 to 2.5 over period of 500×10^6 switching periods, therefore taking a while for the simulation to be completed.

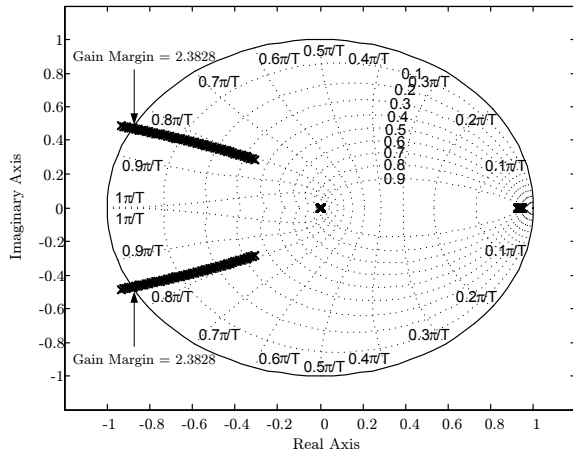
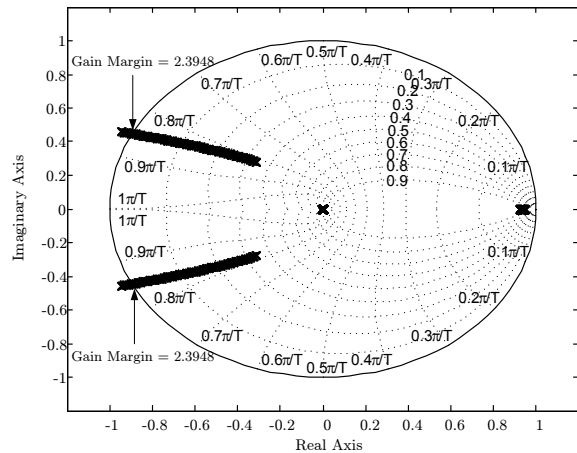
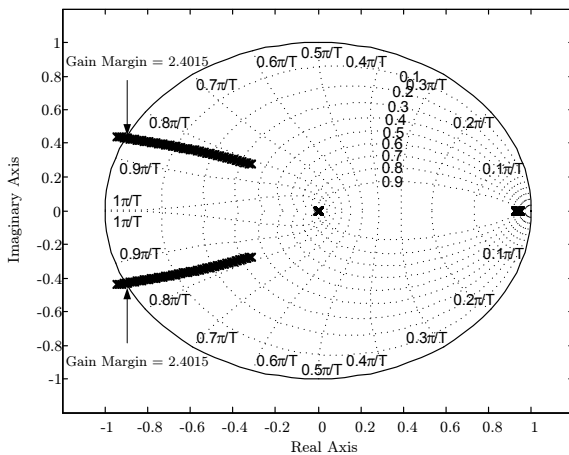
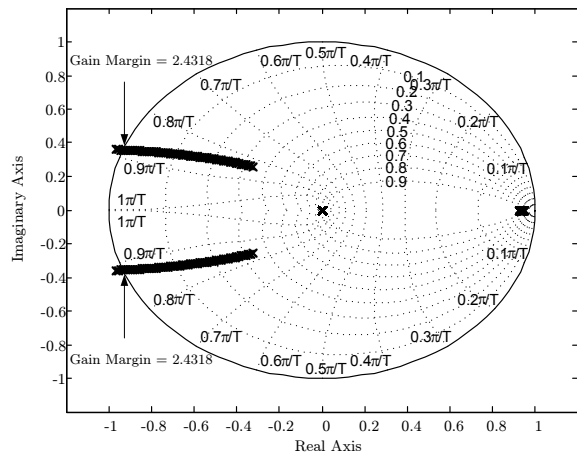
(a) Root locus with $I_{ref} = 0A$ (b) Root locus with $I_{ref} = -40A$ (c) Root locus with $I_{ref} = 50A$ (d) Root locus with $I_{ref} = 80A$

Figure 5.2: Root loci of closed loop poles calculated from single-phase small-signal state space model.

To construct the bifurcation diagram the duty cycle need only be sampled at either the rising edges or the falling edges of triangular carrier. The sampled duty cycle tends to vary from the rising edge to the falling edge of the carrier by small amounts. If the duty cycle is sampled at both edges of the carrier it is possible that small oscillations may occur. This could be problematic when determining where the bifurcation point actually is. Therefore, only the value sampled at the rising edge of the triangular carrier is stored. A bifurcation diagram is constructed with the value of the duty cycle on the y-axis and the loop gain on the x-axis.

The bifurcation point is when a small-disturbance caused by incrementing the loop gain causes the closed loop system to diverge indicating unstable operation. In Figure 5.3 the bifurcation diagram is shown for various current reference values.

The simulations are done for different current reference values to observe the influence

of a change in duty cycle on the gain margin. The same current reference values used to construct the root loci in the previous section are used to prove the accuracy of the small-signal models.

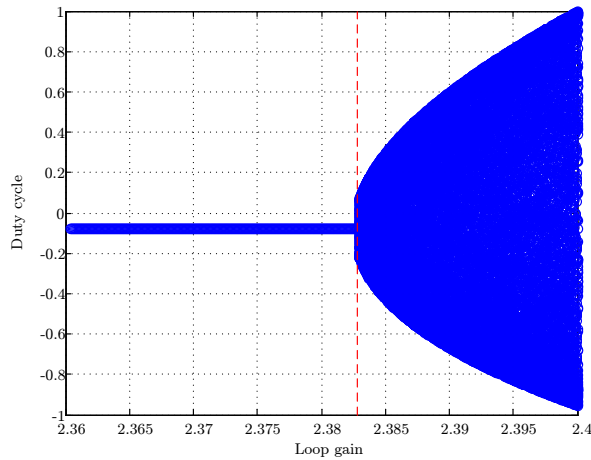
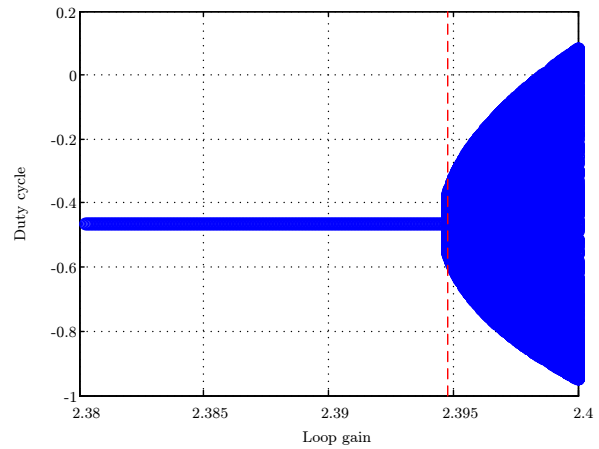
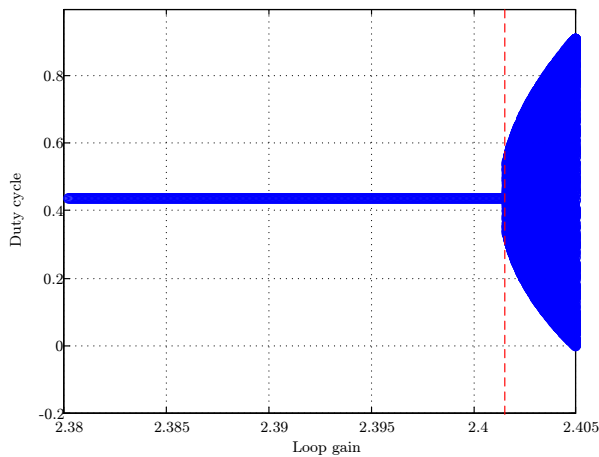
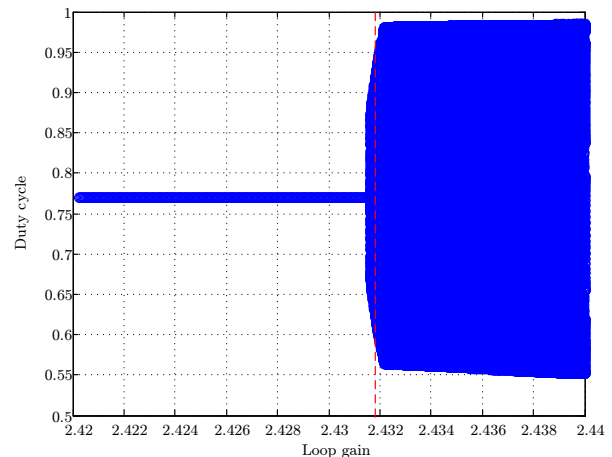
(a) Bifurcation diagram with $I_{ref} = 0A$ (b) Bifurcation diagram with $I_{ref} = -40A$ (c) Bifurcation diagram with $I_{ref} = 50A$ (d) Bifurcation diagram with $I_{ref} = 80A$

Figure 5.3: Bifurcation diagram with gain margin predicted by single-phase small-signal state space model.

The red dotted line shows the theoretical gain margin value predicted by the eigenvalues of the small-signal state space system.

From Figure 5.3 it should be noted that a change in duty cycle does influence the gain margin of the system, unlike what the zero-order hold model predicts. Also comparing the gain margin values predicted by the small-signal state space system in the previous section with the values obtained from the bifurcation diagrams, it can be concluded that the small-signal model derived in section 3.3 predicts the gain margin of a single-phase closed loop system with improved accuracy compared to the zero-order hold model.

Another simulation was done to evaluate the effect the time-constant of the RL-load will have on the systems gain margin. The time-constant of the RL-load is defined as $\tau = \frac{L}{R}$. Instead of 1 mH inductor value used in the previous simulations a 18mH inductance was used to increase the time-constant. The zero-order hold model predicted the gain margin to be 1.6596 while the state space small-signal model predicted it to be 1.6598 for a current reference of 80 A. The root loci of these small-signal models are shown in Figure 5.4.

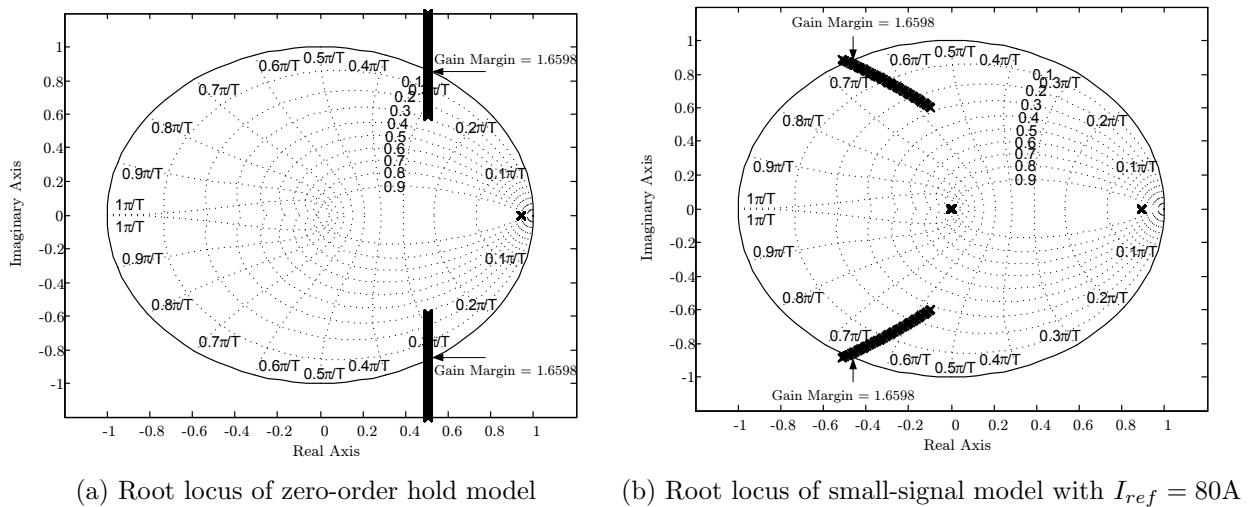


Figure 5.4: Root loci of closed loop poles for inductance of $L = 18mH$.

In Figure 5.5 the red dotted line shows the theoretically value of the gain margin predicted by the state space small-signal model. It compares accurately with the bifurcation point. For a larger time-constant of the load it seems that both the small-signal models are able to predict the gain margin accurately.

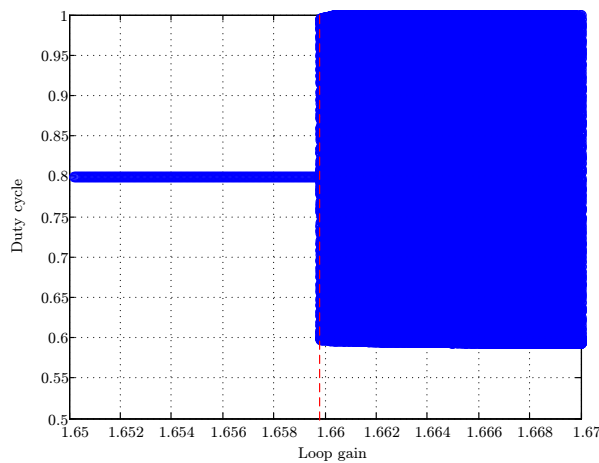


Figure 5.5: Bifurcation diagram with $I_{ref} = 80A$.

It can therefore be accepted that the zero-order hold model becomes less accurate for smaller time-constants τ of the RL-load. In Figure 5.6 the impulse-response of a series RL-load is shown for relatively small and for large time-constants.

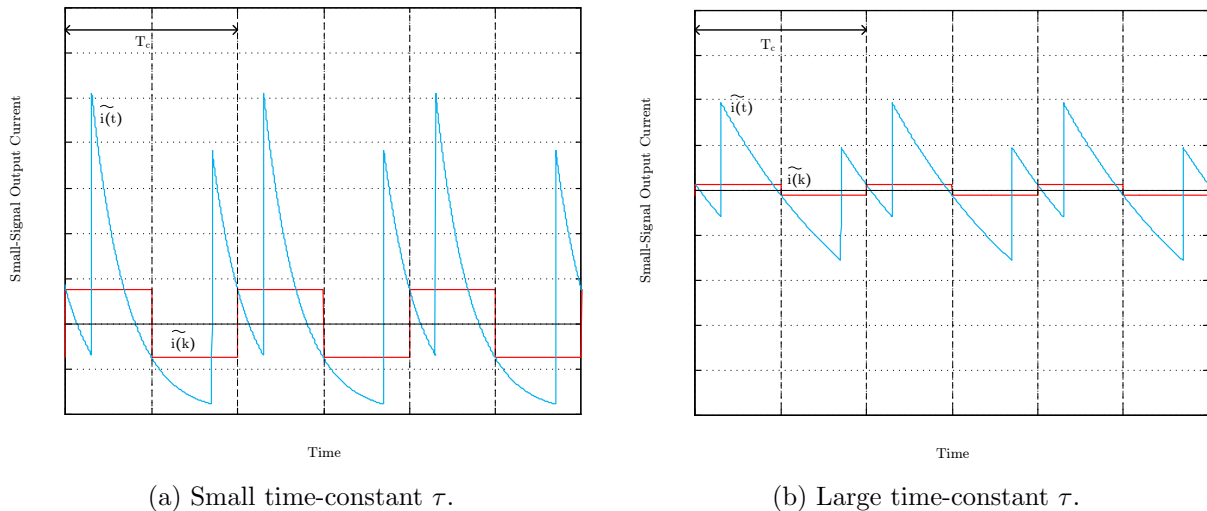


Figure 5.6: Continuous-time and Discrete-time small-signal output current waveforms.

It shows that impulses are generated at both halves of the switching period. In Figure 5.6a and 5.6b the impulse-responses for small and large time-constants of the load are shown. The resulting continuous-time (blue) and discrete-time signals (red) of the output current are also shown. In the case of the small load time-constant, it shows that the output current varies more over half the switching period and it becomes more sensitive to the position of the impulses. However for a larger load time-constant it can be seen that the output current does not vary that much over half a switching period and it can be concluded that the position of the impulses do not have a significant effect. This correlates directly with the results of the the root loci and bifurcation simulations. The zero-order hold model assumes that the impulses occur at fixed positions and if the time-constant is small this assumption is not valid.

5.2.2 Sinusoidal Reference

In this section the constant current reference of the previous section is replaced by a sinusoidal current reference to analyse the stability of a single-phase system. The duty cycle will now differ for each half of the switching period, it is therefore assumed that the closed loop system stays in a quasi-static state. If the reference current varies slowly in comparison to the time-constant of the system this would be an accurate assumption.

For the sinusoidal reference current the duty cycle changes each sample period which makes it difficult to construct the bifurcation diagram. Since the duty cycle follows the

current reference the duty cycle will also vary sinusoidally. This would mean that it could be possible for a system to go from an unstable operation back into a stable operation. If a system gain margin is largely dependent on the duty cycle it may happen that the system is in a unstable operation at its maximum duty cycle, but when the duty cycle becomes smaller the system returns to a stable operation. Therefore the duty cycle is sampled only at its maximum duty cycle value.

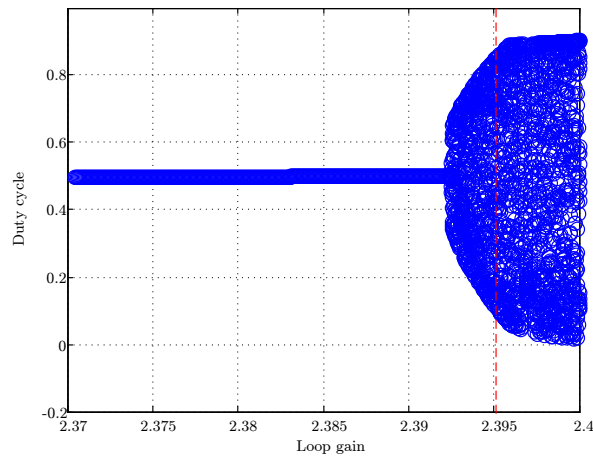


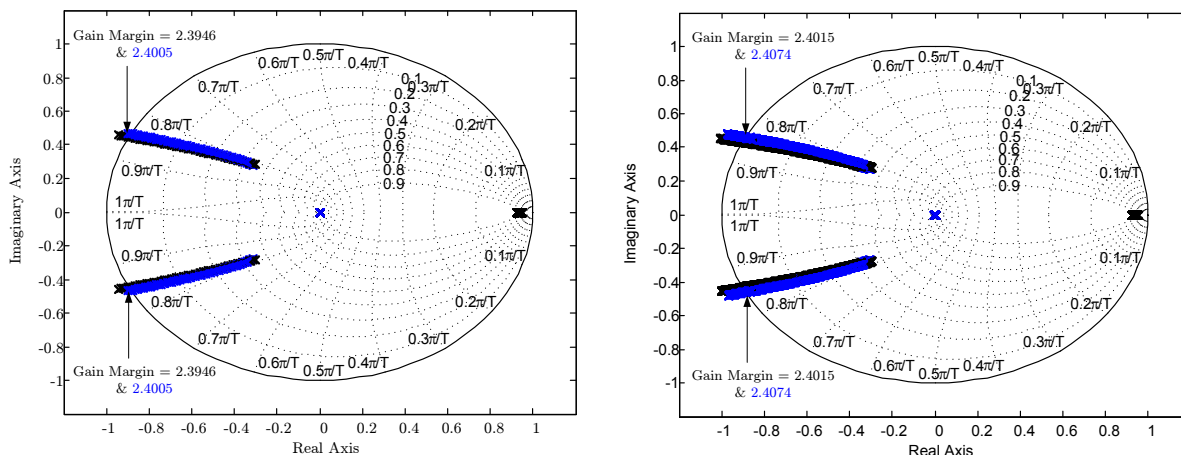
Figure 5.7: Bifurcation with sinusoidal reference.

A simulation is done for a sinusoidal reference with an amplitude of 65A and a frequency of 62.5 Hz. In Figure 5.7 the bifurcation diagram for the sinusoidal reference current is shown. The gain margin of 2.3952 predicted by the single-phase small-signal model compares well to the gain margin of 2.393 found at the bifurcation point. This proves that the single-phase small-signal model is also able to determine the gain margin of a single-phase current regulator with sinusoidal current reference accurately.

5.3 Three-Phase Small-Signal Model

In this section the three-phase asymmetrical regular sampled pulse-width modulator small-signal model derived in section 3.4 is applied to a stationary d-q frame PI current regulator to obtain the closed loop state space equations of the system. In section A.2.3.1 the discrete-time state space closed loop equations are derived in matrix form. From the system matrix the eigenvalues are used to calculate the closed loop poles of the three-phase system as shown in section 5.1.

Similar to the single-phase model, a Matlab© simulation is used to construct the root locus of the closed loop poles. In Figure 5.8 the root loci plots for different constant $I_{ref\alpha}$ and $I_{ref\beta}$ current references are shown. The closed loop poles for the α loop are indicated in black while the closed loop poles of the β loop are indicated in blue.



(a) Root locus with $I_{ref\alpha} = 40\text{A}$ and $I_{ref\beta} = -40\text{A}$ (b) Root locus with $I_{ref\alpha} = 50\text{A}$ and $I_{ref\beta} = -50\text{A}$

Figure 5.8: Root loci of closed loop poles calculated from three-phase small-signal state space model.

From the small-signal state space model of the pulse-width modulator derived in section 3.4 it is shown that the α loop is equivalent to a single-phase small-signal model (see (3.4.23) and (3.4.24)), where the small-signal model is dependent on the duty cycle of phase A only. For the β loop the small-signal model of the pulse-width modulator is dependent on both phase B and C duty cycle values (see (3.4.25) and (3.4.26)). However, since a balanced three-phase load is used with a floating star point, the duty cycle of phase C will depend on both the duty cycle values of phase A and B as follows

$$d_c = \frac{1}{2}[3 - 2d_a - 2d_b] \quad (5.3.1)$$

From Figure 5.8a, comparing the gain margin of 2.3946 for the α loop to the single-phase small-signal model in Figure 5.2b, it can be seen that they are more or less identical. This proves that the α loop is identical to a single-phase small-signal model. The same could be seen when comparing Figures 5.8b and Figure 5.2c. It is also interesting to see that, although the small-signal models derived for the α and β loops differ, the gain margins predicted by the root loci in Figure 5.8 shows they both predict almost identical gain margins. In the following section this phenomenon is further investigated by comparing the gain margins of the root loci to the corresponding bifurcations diagrams.

5.3.1 Gain Margin

The bifurcation diagram simulation of the single-phase system is extended for a three-phase system, where the α and β loops are simultaneously ramped up while analysing the

duty cycles. Similar to the single-phase system the gain margin is determined when the system goes into an unstable operation, which occurs at the bifurcation point.

The α and β loops bifurcation diagrams are shown in Figures 5.9 and 5.10 for current references of $I_{ref\alpha} = 40\text{A}$ and $I_{ref\beta} = -40\text{A}$, as well as $I_{ref\alpha} = 50\text{A}$ and $I_{ref\beta} = -50\text{A}$. The red dotted line shows the theoretical gain margin predicted by the eigenvalues of the discrete-time three-phase small-signal state space model.

Figures 5.9a and 5.10a show that the three-phase small-signal model is able to predict the gain margins of 2.3946 and 2.402 for the α loops very accurately. However, in Figures 5.9b and 5.10b it appears that the β loop goes into unstable operation at a loop gain of 2.3946, earlier as the prediction of the small-signal model. A small-error of $\pm 5.5^{-3}$ is noted which is most likely due to simulation constraints.

Also interesting to see is that β loop bifurcation point occurs at the same instant as that of the α loop for both cases in Figures 5.9 and 5.10. This would mean that the instability of the α loop influences the stability of the β loop and causes to β loop to also go into unstable operation. From the discrete-time small-signal state space equations (see (3.4.25) and (3.4.26) of the β loop in section 3.4.5 it is evident that the stability of the β loop is dependent on the duty cycle value of phase C, while phase C depends on the values of phase A and B for a balanced three-phase system as shown in (5.3.1). Therefore the moment α loop goes into unstable operation, it influences the β loop which then also experience instability.

This also explains why the position of the β loop closed loop poles is very similar to that of the α loops closed loop poles, shown in Figure 5.8. The stability of the β control loop is therefore dominated by the stability of the α control loop.

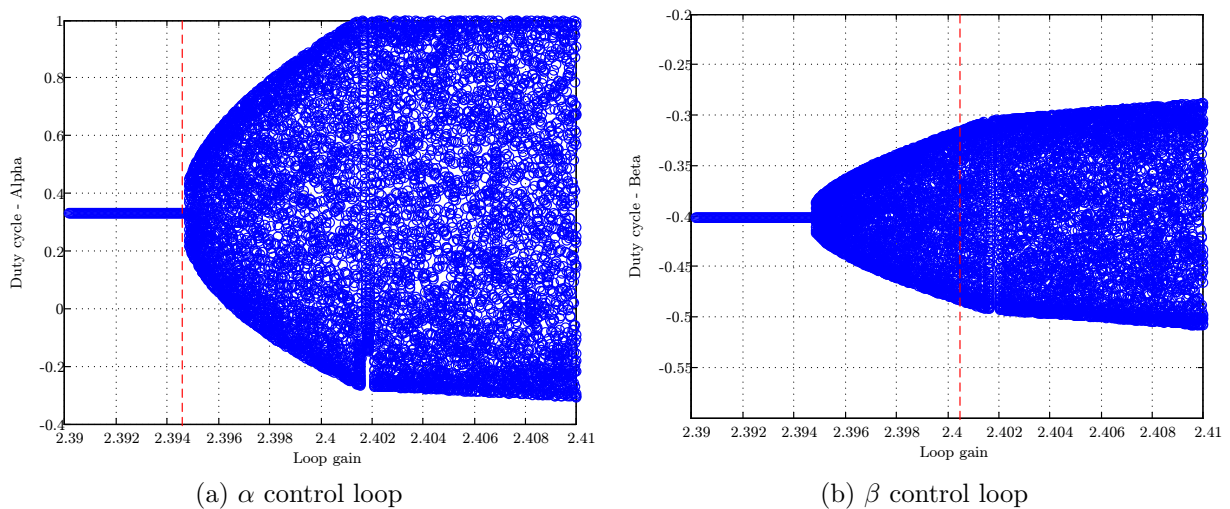


Figure 5.9: Bifurcation diagrams with $I_{ref\alpha} = 40\text{A}$ and $I_{ref\beta} = -40\text{A}$.

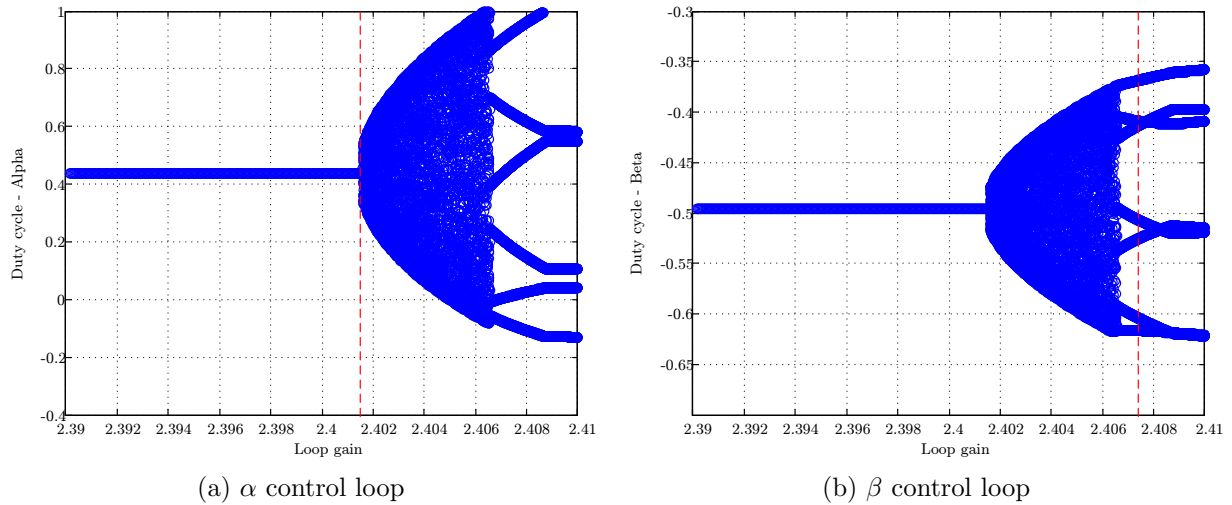


Figure 5.10: Bifurcation diagrams with $I_{ref_\alpha} = 50\text{A}$ and $I_{ref_\beta} = -50\text{A}$.

However, in [16] the α and β loops of the three-phase small-signal model is assumed to be equivalent to a zero-order hold model and as mentioned before the zero-order hold model does not consider the effect of the duty cycle have on a systems gain margin. The zero-order hold model is therefore unable to predict the effect the α loop would have on the β loop.

5.3.2 Sinusoidal Reference

In this section the three-phase small-signal model is used to analyse the stability of the three-phase closed loop system with sinusoidal current references I_{ref_α} and I_{ref_β} . Similar to the single-phase sinusoidal current reference it is accepted that the closed loop stays in a quasi-static state. The current reference of I_{ref_α} is simulated with a sinusoidal reference of 65 A and a frequency of 62.5 Hz. The current reference of I_{ref_β} is simply phase shifted by 120° .

Since a sinusoidal reference is used, the duty cycle value will also vary sinusoidally. The moment the duty cycle reaches its maximum value and the loop gain is beyond the bifurcation point, the system goes into unstable operation. As the duty cycle value become smaller it may be that the system returns to a stable operation, but as shown in the previous sections, the closed loop systems used in this research are not that sensitive to a change in the duty cycle value.

The same strategy used in section 5.2 is applied, where the the duty cycle was sampled once each fundamental cycle at the maximum value of the duty cycle. Figure 5.11 shows the resulting bifurcation diagram.

The red dotted line shows the theoretical gain margin of 2.3935 predicted by the state

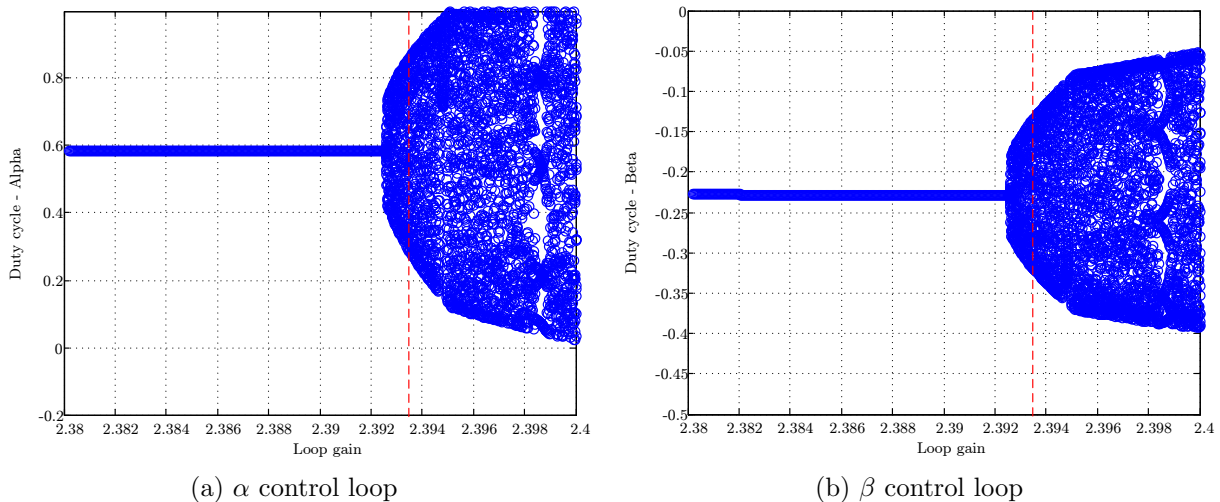


Figure 5.11: Bifurcation diagrams with $I_{ref_\alpha} = 65\sin(\omega t)A$ and $I_{ref_\beta} = 65\sin(\omega t + 120^\circ)A$.

space small-signal model. Comparing this gain margin to the bifurcation point at 2.393 it shows that the three-phase small-signal model is also able to accurately predict the gain margin for a three-phase system.

The zero-order hold model predicts the gain margin to be 2.3960, very similar but not as accurate as the small-signal model.

5.4 Summary

In section 5.2 the zero-order hold model was compared to the single-phase small-signal state space model. The results showed that gain margin is influenced by the change in duty cycle values and that the zero-order hold model is not able to allow for these changes. Another simulation was used to determine if the time-constant of the RL-load affects the ability of the small-signal models to determine the gain margin of a system accurately. A simulation with a larger time-constant was used and it showed that, for a larger time-constant, the effect of the duty cycle becomes less significant and the zero-order hold model becomes more accurate. In contrast, the smaller the time-constant becomes the less accurate the zero-order hold model.

In section 5.3 the three-phase small-signal model is evaluated to analyse its accuracy. It is shown that, for a balanced three-phase RL-load, the stability of the β control loop is influenced by the α control loop. Using the zero-order hold model this influence would not be predicted since the zero-order hold assumes that the α and β loops can be represented by two independent single-phase systems.

From the results it appears that the zero-order hold model does not have a significantly large influence on the gain margins of the single and three-phase systems, although the

root locus plot of the zero-order hold model differs considerably more from that of the proposed small-signal models. It is suspected that this is because the zero-order hold model adds an extra low-pass filter to the control loop, but this should be investigated further using Bode plots.

Chapter 6

Conclusion

In this thesis an accurate small-signal model analysis is proposed for an asymmetrical regular sampled pulse-width modulator control loop. It is known that switching within PWM control loops introduces non-linear behaviour into the control loop which is complicating to analyse, especially the influence of this non-linear behaviour on the stability of the PWM control loop. This research specifically focussed on the influence of this non-linear behaviour on the gain margin of the closed loop system. Using the concepts of small-signal model theory, this non-linear behaviour is analysed for an asymmetrical regular sampled PWM control loop.

In small-signal model analysis a small-disturbance signal is superimposed onto the large-signal to evaluate the stability of the large-signal control loop. The small-signal model is a linear representation of the large-signal control loop and is represented by impulses that occurs at each instant where the large-signal intersects the carrier signal. For asymmetrical regular sampled PWM the large-signal intersects the triangular carrier twice over one switching period, resulting in the duty cycle for the first half of the switching period to differ from that of the second half of the switching period. Dummy state variables were introduced to derive a discrete-time state space model for both single and three-phase small-signal models. These small-signal models are able to take into account the change in duty cycle, unlike the conventional methods i.e. ZOH model.

Using P and PI current regulators, the discrete-time closed loop state space models are obtained. From the discrete-time closed loop state space model the eigenvalues of the system matrices are used to determine the position of the closed loop poles (from which the relevant gain margins can be calculated). In this research a PI current regulator is implemented together with a computational delay of one sample period. This proportional current regulator is applied to both single and three-phase systems, where the three-phase system is implemented in the stationary d-q frame.

The accuracy of the single and three-phase small-signal models are verified by comparing their predicted gain margins to the gain margins of the practical system, determined from bifurcation diagrams. Initially constant current references are used to simplify the simulations, but it is also extended to allow for sinusoidal current references. It was shown that the proposed small-signal model, derived for the asymmetrical regular sampled pulse-width modulator, is able to determine the gain margins of the individual systems with a high degree of accuracy.

The proposed small-signal model was then compared to approximated ZOH hold model. It has been proven that the duty cycle in a single-phase system does influence the gain margin of the system and that the proposed small-signal model can accurately determine the gain margin. Since the ZOH hold model does not consider the influence of the duty cycle, it becomes inaccurate, especially where the RL-load time-constant is small. The inaccuracy is relatively small, but it is suspected that it may become larger for other types of loads i.e LCL-load.

The assumption used to represent a three-phase system in its stationary d-q frame by independent single-phase systems was also investigated. From the discrete-time state space model derived for the three-phase asymmetrical regular sampled pulse-width modulator it was shown that the stability of the α loop contributes to the stability of the β loop, if a balanced three-phase load is used having a floating star point. It is shown that the instability in the α loop causes the β loop to also experience instabilities.

Although under the conditions used, the difference between the small-signal models did not play a big role on the gain margins, with further research more shortcomings of the ZOH model could be investigated.

6.1 Recommendation and Future Work

The research in this thesis focussed on the application of small-signal models on asymmetrical regular sampled pulse-width modulators. However, using the techniques introduced in this thesis, further research can be done on the following aspects:

- Other types of current regulators (i.e. Proportional Resonant current regulator) can be implemented to determine if the time-constant of the controller would also influence the small-signal model.
- Equations can be derived to calculate the duty cycle values for each halve of the switching period. Currently a simulation is used to measure these values, which are imported into the discrete-time state space models of the small-signal models.

- Currently the matrices of the closed loop system are very large and most of the values are equal to zero. A method could be introduced to simplify these matrices.
- Practical implementation of the system to compare the practical results to the theory and simulations.
- It has already been shown that the time-constant of a RL-load contributes to the gain margin of the system. Analysing the effect of more load types (i.e. LCL or LCR load) on the stability of the systems could be advantageous.
- Instead of using the design strategy in [10], the discrete-time state space small-signal models could be used to design optimal PWM control loops by increasing the loop gain to its maximum. Increasing the loop gain will have a positive result on the transient response of the control loop.
- Analyse the effect that additional non-integer delays will have on the stability of a closed loop system. Also see if the ZOH model is still an acceptable model if these delays is included. To analyse the effect of the additional delays I suggest using Bode plots. The non-integer delays refers to delays introduced by gate drivers and ADCs which is usually neglecte within regular sampled PWM control loops. These non-integer can easily be included in the small-signal models derived.
- The three-phase small-signal model should also be modified to analyse the effect of an unbalanced three-phase system to determine if the zero-order hold model would still be an accurate small-signal model. It is expected that the zero-order hold model would then become inaccurate, because it is used as an average model, while small-signal models actually apply to instantaneous models.

It should be noted that the work in this thesis is not limited to single and three phase systems, the concept can be extended to more complicated configurations. I thoroughly enjoyed all the challenges I was exposed to, and especially the theory of the small-signal models.

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Appendices

Appendix A

Closed Loop State Space Models

A.1 Single-Phase Small-Signal Model

A.1.1 Open Loop State Space Representation

$$\begin{bmatrix} i_1(k+1) \\ i_2(k+1) \end{bmatrix} = \begin{bmatrix} 0 & F_{12} \\ 0 & F_{22} \end{bmatrix} \begin{bmatrix} i_1(k) \\ i_2(k) \end{bmatrix} + \begin{bmatrix} G_{11} & 0 \\ G_{21} & G_{22} \end{bmatrix} \begin{bmatrix} f_2(k) \\ f_1(k+1) \end{bmatrix}$$

where $F_{12} = e^{-\frac{T_c}{2\tau}}$, $F_{22} = e^{-\frac{T_c}{\tau}}$, $G_{11} = \frac{T_c}{2L}e^{-\frac{d_1 T_c}{2\tau}}$, $G_{21} = \frac{T_c}{2L}e^{-\frac{(1+d_1)T_c}{2\tau}}$ and $G_{22} = \frac{T_c}{2L}e^{-\frac{(1-d_2)T_c}{2\tau}}$.

A.1.2 Proportional Current Regulator

Output of proportional controller:

$$\begin{aligned} f_1(k+1) &= K_p(i_1^*(k+1) - i_1(k+1)) \\ f_2(k) &= K_p(i_2^*(k) - i_2(k)) \end{aligned}$$

Closed loop state space representation:

$$\begin{bmatrix} i_1(k+1) \\ i_2(k+1) \end{bmatrix} = \begin{bmatrix} 0 & F_{12} \\ 0 & F_{22} \end{bmatrix} \begin{bmatrix} i_1(k) \\ i_2(k) \end{bmatrix} + \begin{bmatrix} G_{11} & 0 \\ G_{21} & G_{22} \end{bmatrix} \begin{bmatrix} K_p(i_2^*(k) - i_2(k)) \\ K_p(i_1^*(k+1) - i_1(k+1)) \end{bmatrix}$$

A.1.3 Proportional Integral Current Regulator

Output of the proportional term:

$$\begin{aligned} a_1(k+1) &= K_p(i_1^*(k+1) - i_1(k+1)) \\ a_2(k+1) &= K_p(i_2^*(k+1) - i_2(k+1)) \end{aligned}$$

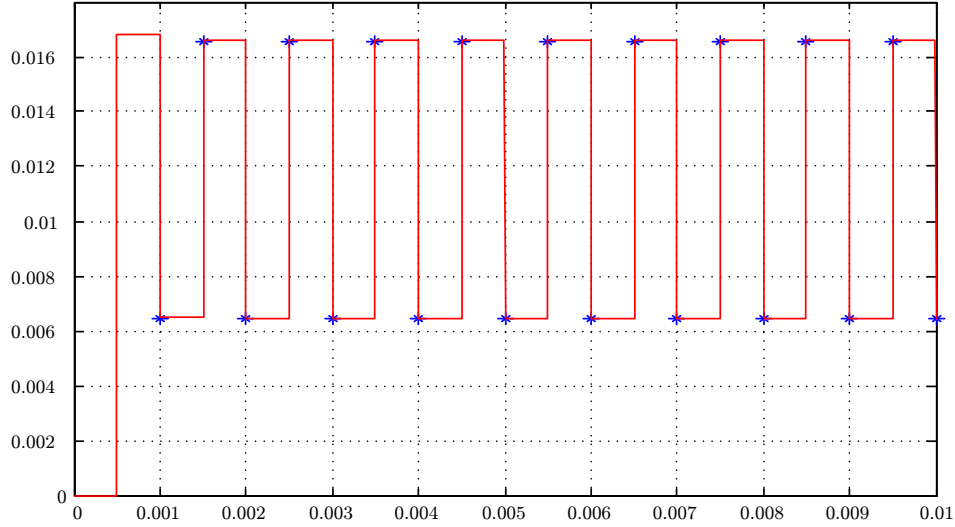


Figure A.1: Iteration of closed loop state space representation for single-phase proportional current regulator compared to Matlab© Simulink.

Output of the integrator term:

$$b_1(k+1) = b_2(k) + K_i(i_1^*(k+1) - i_1(k+1))$$

$$b_2(k+1) = b_1(k+1) + K_i(i_2^*(k+1) - i_2(k+1))$$

Output of the proportional integrator current regulator:

$$f_1(k+1) = x_1(k+1)$$

$$= a_1(k+1) + b_1(k+1)$$

$$= K_p(i_1^*(k+1) - i_1(k+1)) + b_2(k) + K_i(i_1^*(k+1) - i_1(k+1))$$

$$f_2(k+1) = x_2(k+1)$$

$$= a_2(k+1) + b_2(k+1)$$

$$= K_p(i_2^*(k+1) - i_2(k+1)) + b_1(k+1) + K_i(i_2^*(k+1) - i_2(k+1))$$

Closed loop state space representation:

Include $f_1(k), f_2(k), b_1(k)$ and $b_2(k)$ in the state space representation.

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & -G_{22} & 0 & 0 & 0 \\ K_p + K_i & 0 & 1 & 0 & 0 & 0 \\ 0 & K_p + K_i & 0 & 1 & -1 & 0 \\ K_i & 0 & 0 & 0 & 1 & 0 \\ 0 & K_i & 0 & 0 & -1 & 1 \end{bmatrix} \begin{bmatrix} i_1(k+1) \\ i_2(k+1) \\ f_1(k+1) \\ f_2(k+1) \\ b_1(k+1) \\ b_2(k+1) \end{bmatrix} = \begin{bmatrix} 0 & F_{12} & 0 & G_{11} & 0 & 0 \\ 0 & F_{22} & 0 & G_{21} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_1(k) \\ i_2(k) \\ f_1(k) \\ f_2(k) \\ b_1(k) \\ b_2(k) \end{bmatrix} \\
+ (K_p + K_i) \begin{bmatrix} 0 \\ 0 \\ i_1^*(k+1) \\ i_2^*(k+1) \\ 0 \\ 0 \end{bmatrix} + K_i \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ i_1^*(k+1) \\ i_2^*(k+1) \end{bmatrix}$$

Then

$$\begin{bmatrix} i_1(k+1) \\ i_2(k+1) \\ f_1(k+1) \\ f_2(k+1) \\ b_1(k+1) \\ b_2(k+1) \end{bmatrix} = \mathbf{G}^{-1} \mathbf{F} \begin{bmatrix} i_1(k) \\ i_2(k) \\ f_1(k) \\ f_2(k) \\ b_1(k) \\ b_2(k) \end{bmatrix} + (K_p + K_i) \mathbf{G}^{-1} \begin{bmatrix} 0 \\ 0 \\ i_1^*(k+1) \\ i_2^*(k+1) \\ 0 \\ 0 \end{bmatrix} + K_i \mathbf{G}^{-1} \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ i_1^*(k+1) \\ i_2^*(k+1) \end{bmatrix}$$

where

$$\mathbf{G} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & -G_{22} & 0 & 0 & 0 \\ K_p + K_i & 0 & 1 & 0 & 0 & 0 \\ 0 & K_p + K_i & 0 & 1 & -1 & 0 \\ K_i & 0 & 0 & 0 & 1 & 0 \\ 0 & K_i & 0 & 0 & -1 & 1 \end{bmatrix}; \mathbf{F} = \begin{bmatrix} 0 & F_{12} & 0 & G_{11} & 0 & 0 \\ 0 & F_{22} & 0 & G_{21} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

A.1.3.1 Proportional Integral Current Regulator with Computational Delay

Output of the computational delay:

$$f_1(k+1) = x_2(k)$$

$$f_2(k+1) = x_1(k+1)$$

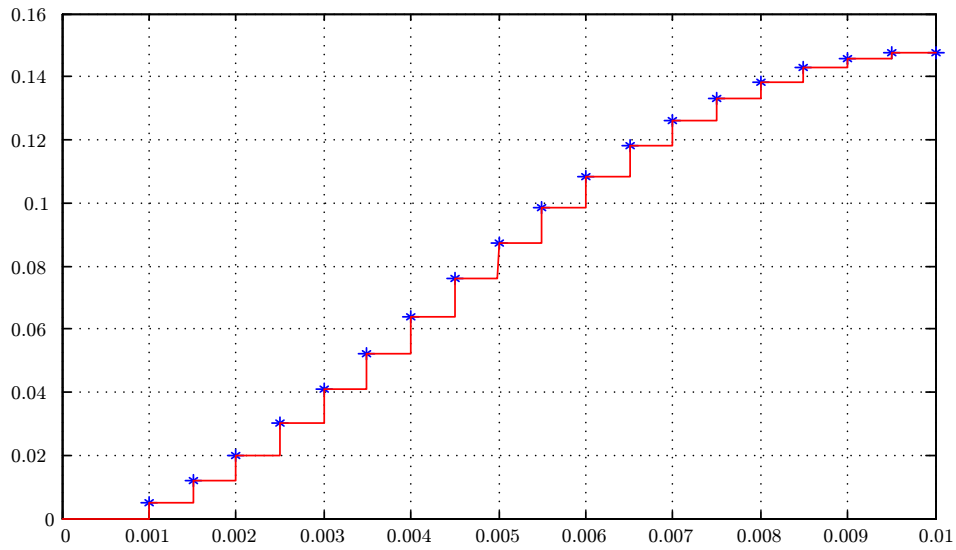


Figure A.2: Iteration of closed loop state space representation for single-phase proportional integral current regulator compared to Matlab© Simulink.

Closed loop state space representation:

Include $x_1(k), x_2(k), b_1(k), b_2(k), f_1(k)$ and $f_2(k)$ in the state space representation. Results in

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & -G_{22} & 0 \\ K_p + K_i & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & K_p + K_i & 0 & 1 & -1 & 0 & 0 & 0 \\ K_i & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & K_i & 0 & 0 & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_1(k+1) \\ i_2(k+1) \\ x_1(k+1) \\ x_2(k+1) \\ b_1(k+1) \\ b_2(k+1) \\ f_1(k+1) \\ f_2(k+1) \end{bmatrix}$$

$$= \begin{bmatrix} 0 & F_{12} & 0 & 0 & 0 & 0 & 0 & G_{11} \\ 0 & F_{22} & 0 & 0 & 0 & 0 & 0 & G_{21} \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_1(k) \\ i_2(k) \\ x_1(k) \\ x_2(k) \\ b_1(k) \\ b_2(k) \\ f_1(k) \\ f_2(k) \end{bmatrix} + (K_p + K_i) \begin{bmatrix} 0 \\ 0 \\ i_1^*(k+1) \\ i_2^*(k+1) \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} + K_i \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ i_1^*(k+1) \\ i_2^*(k+1) \\ 0 \\ 0 \end{bmatrix}$$

Then

$$\begin{bmatrix} i_1(k+1) \\ i_2(k+1) \\ x_1(k+1) \\ x_2(k+1) \\ b_1(k+1) \\ b_2(k+1) \\ f_1(k+1) \\ f_2(k+1) \end{bmatrix} = \mathbf{G}^{-1}\mathbf{F} \begin{bmatrix} i_1(k) \\ i_2(k) \\ x_1(k) \\ x_2(k) \\ b_1(k) \\ b_2(k) \\ f_1(k) \\ f_2(k) \end{bmatrix} + (K_p + K_i)\mathbf{G}^{-1} \begin{bmatrix} 0 \\ 0 \\ i_1^*(k+1) \\ i_2^*(k+1) \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} + K_i\mathbf{G}^{-1} \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ i_1^*(k+1) \\ i_2^*(k+1) \\ 0 \\ 0 \end{bmatrix}$$

where

$$\mathbf{G} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & -G_{22} & 0 \\ K_p + K_i & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & K_p + K_i & 0 & 1 & -1 & 0 & 0 & 0 \\ K_i & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & K_i & 0 & 0 & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}; \mathbf{F} = \begin{bmatrix} 0 & F_{12} & 0 & 0 & 0 & 0 & 0 & G_{11} \\ 0 & F_{22} & 0 & 0 & 0 & 0 & 0 & G_{21} \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

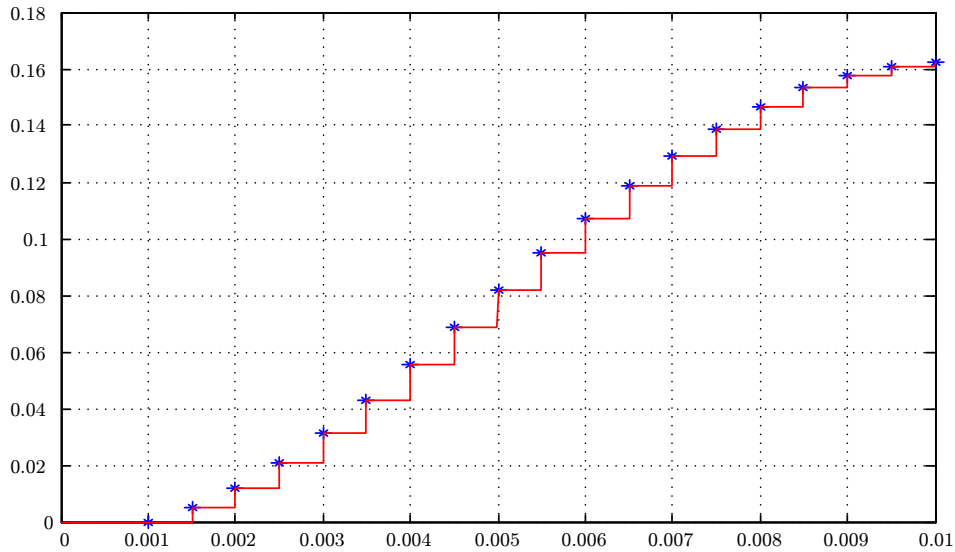


Figure A.3: Test formula derived for Single-Phase Proportional Integral Regulator with one sample period delay.

A.2 Three-Phase Small-Signal Model

A.2.1 Open Loop State Space Representation

$$\begin{bmatrix} i_{1\alpha}(k+1) \\ i_{2\alpha}(k+1) \\ i_{1\beta}(k+1) \\ i_{2\beta}(k+1) \end{bmatrix} = \begin{bmatrix} 0 & F_{12} & 0 & 0 \\ 0 & F_{22} & 0 & 0 \\ 0 & 0 & 0 & F_{34} \\ 0 & 0 & 0 & F_{44} \end{bmatrix} \begin{bmatrix} i_{1\alpha}(k) \\ i_{2\alpha}(k) \\ i_{1\beta}(k) \\ i_{2\beta}(k) \end{bmatrix} + \begin{bmatrix} G_{11} & 0 & 0 & 0 \\ G_{21} & G_{22} & 0 & 0 \\ G_{31} & 0 & G_{33} & 0 \\ G_{41} & G_{42} & G_{43} & G_{44} \end{bmatrix} \begin{bmatrix} f_{2\alpha}(k) \\ f_{1\alpha}(k+1) \\ f_{2\beta}(k) \\ f_{1\beta}(k+1) \end{bmatrix}$$

where $F_{12} = F_{34} = e^{-\frac{T_c}{2\tau}}$, $F_{22} = F_{44} = e^{-\frac{T_c}{\tau}}$, $G_{11} = \frac{T_c}{2} \frac{1}{L} e^{-\frac{d_a T_c}{2\tau}}$, $G_{21} = \frac{T_c}{2L} e^{-\frac{(1+d_a)T_c}{2\tau}}$, $G_{22} = \frac{T_c}{2} \frac{1}{L} e^{-\frac{(1-d_a)T_c}{2\tau}}$, $G_{31} = \frac{T_c}{4L} \left(e^{-\frac{d_b T_c}{2\tau}} + e^{-\frac{d_c T_c}{2\tau}} \right)$, $G_{41} = \frac{T_c}{4L} \left(e^{-\frac{(1+d_b)T_c}{2\tau}} + e^{-\frac{(1+d_c)T_c}{2\tau}} \right)$, $G_{42} = \frac{T_c}{4L} \left(e^{-\frac{(1-d_b)T_c}{2\tau}} + e^{-\frac{(1-d_c)T_c}{2\tau}} \right)$, $G_{33} = \frac{T_c}{4L} \frac{1}{\sqrt{3}} \left(e^{-\frac{d_b T_c}{2\tau}} - e^{-\frac{d_c T_c}{2\tau}} \right)$, $G_{43} = \frac{T_c}{4L} \frac{1}{\sqrt{3}} \left(e^{-\frac{(1+d_b)T_c}{2\tau}} - e^{-\frac{(1+d_c)T_c}{2\tau}} \right)$ and $G_{44} = \frac{T_c}{4L} \frac{1}{\sqrt{3}} \left(e^{-\frac{(1-d_b)T_c}{2\tau}} - e^{-\frac{(1-d_c)T_c}{2\tau}} \right)$.

A.2.2 Proportional Current Regulator

Output of proportional controller:

$$\begin{aligned} f_1(k+1) &= K_p (i_{1\alpha}^*(k+1) - i_{1\alpha}(k+1)) \\ f_2(k) &= K_p (i_{2\alpha}^*(k) - i_{2\alpha}(k)) \end{aligned}$$

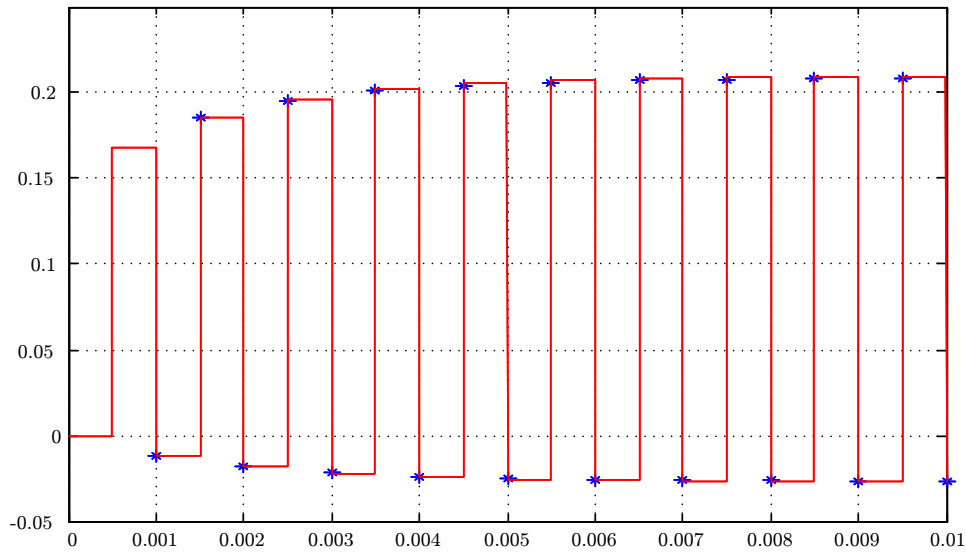
Closed loop state space representation:

$$\begin{bmatrix} i_{1\alpha}(k+1) \\ i_{2\alpha}(k+1) \\ i_{1\beta}(k+1) \\ i_{2\beta}(k+1) \end{bmatrix} = \begin{bmatrix} 0 & F_{12} & 0 & 0 \\ 0 & F_{22} & 0 & 0 \\ 0 & 0 & 0 & F_{34} \\ 0 & 0 & 0 & F_{44} \end{bmatrix} \begin{bmatrix} i_{1\alpha}(k) \\ i_{2\alpha}(k) \\ i_{1\beta}(k) \\ i_{2\beta}(k) \end{bmatrix} + \begin{bmatrix} G_{11} & 0 & 0 & 0 \\ G_{21} & G_{22} & 0 & 0 \\ G_{31} & 0 & G_{33} & 0 \\ G_{41} & G_{42} & G_{43} & G_{44} \end{bmatrix} \begin{bmatrix} K_p (i_{2\alpha}^*(k) - i_{2\alpha}(k)) \\ K_p (i_{1\alpha}^*(k+1) - i_{1\alpha}(k+1)) \\ K_p (i_{2\beta}^*(k) - i_{2\beta}(k)) \\ K_p (i_{1\beta}^*(k+1) - i_{1\beta}(k+1)) \end{bmatrix}$$

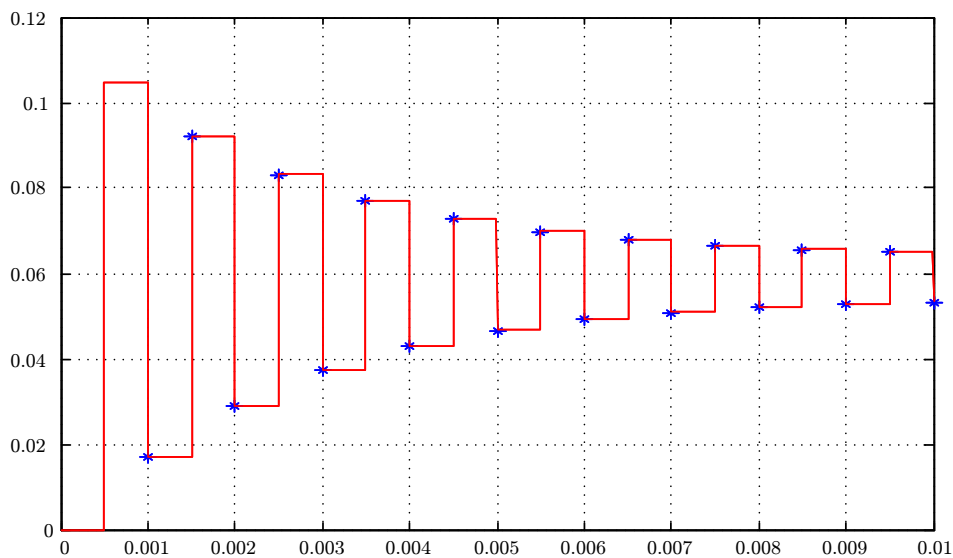
A.2.3 Proportional Integral Regulator

Output of the proportional term:

$$\begin{aligned} a_{1\alpha/\beta}(k+1) &= K_p \left(i_{1\alpha/\beta}^*(k+1) - i_{1\alpha/\beta}(k+1) \right) \\ a_{2\alpha/\beta}(k+1) &= K_p \left(i_{2\alpha/\beta}^*(k+1) - i_{2\alpha/\beta}(k+1) \right) \end{aligned}$$



(a) Alpha Proportional Regulator.



(b) Beta Proportional Regulator.

Figure A.4: Test for three-phase PWM small-signal model simulated in Matlab©.

Output of the integral term:

$$b_{1\alpha/\beta}(k+1) = b_{2\alpha/\beta}(k) + K_i \left(i_{1\alpha/\beta}^*(k+1) - i_{1\alpha/\beta}(k+1) \right)$$

$$b_{2\alpha/\beta}(k+1) = b_{1\alpha/\beta}(k+1) + K_i \left(i_{2\alpha/\beta}^*(k+1) - i_{\alpha/\beta}(k+1) \right)$$

The sum of the proportional- and integral term is the output of the proportional integral controller for individual circuits:

$$\begin{aligned} f_{1\alpha/\beta}(k+1) &= x_{1\alpha/\beta}(k+1) \\ &= a_{1\alpha/\beta}(k+1) + b_{1\alpha/\beta}(k+1) \\ &= K_p \left(i_{1\alpha/\beta}^*(k+1) - i_{1\alpha/\beta}(k+1) \right) + b_{2\alpha/\beta}(k) + K_i \left(i_{1\alpha/\beta}^*(k+1) - i_{1\alpha/\beta}(k+1) \right) \end{aligned}$$

$$\begin{aligned}
f_{2\alpha/\beta}(k+1) &= x_{2\alpha/\beta}(k+1) \\
&= a_{2\alpha/\beta}(k+1) + b_{2\alpha/\beta}(k+1) \\
&= K_p \left(i_{2\alpha/\beta}^*(k+1) - i_{2\alpha/\beta}(k+1) \right) + b_{1\alpha/\beta}(k+1) + K_i \left(i_{2\alpha/\beta}^*(k+1) - i_{\alpha/\beta}(k+1) \right)
\end{aligned}$$

Closed loop state space representation:

Include $f_1(k), f_2(k), b_1(k), b_2(k)$ and $K_{tot} = K_i + K_p$ in the state space representation.

$$\begin{aligned}
& \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & -G_{22} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & -G_{44} & 0 & -G_{42} & 0 & 0 & 0 & 0 & 0 \\ K_{tot} & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & K_{tot} & 0 & 0 & 0 & 1 & 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & K_{tot} & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & K_{tot} & 0 & 0 & 0 & 1 & 0 & 0 & -1 & 0 \\ K_i & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & K_i & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 1 & 0 & 0 \\ 0 & 0 & K_i & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & K_i & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 1 \end{bmatrix} \begin{bmatrix} i_{1\alpha}(k+1) \\ i_{2\alpha}(k+1) \\ i_{1\beta}(k+1) \\ i_{2\beta}(k+1) \\ f_{1\alpha}(k+1) \\ f_{2\alpha}(k+1) \\ f_{1\beta}(k+1) \\ f_{2\beta}(k+1) \\ b_{1\alpha}(k+1) \\ b_{2\alpha}(k+1) \\ b_{1\beta}(k+1) \\ b_{2\beta}(k+1) \end{bmatrix} \\
= & \begin{bmatrix} 0 & F_{12} & 0 & 0 & 0 & G_{11} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & F_{22} & 0 & 0 & 0 & G_{21} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & F_{34} & 0 & G_{33} & 0 & G_{31} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & F_{44} & 0 & G_{43} & 0 & G_{41} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{1\alpha}(k) \\ i_{2\alpha}(k) \\ i_{1\beta}(k) \\ i_{2\beta}(k) \\ f_{1\alpha}(k) \\ f_{2\alpha}(k) \\ f_{1\beta}(k) \\ f_{2\beta}(k) \\ b_{1\alpha}(k) \\ b_{2\alpha}(k) \\ b_{1\beta}(k) \\ b_{2\beta}(k) \end{bmatrix} \\
+ & \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ K_{tot} & 0 & 0 & 0 \\ 0 & K_{tot} & 0 & 0 \\ 0 & 0 & K_{tot} & 0 \\ 0 & 0 & 0 & K_{tot} \\ K_i & 0 & 0 & 0 \\ 0 & K_i & 0 & 0 \\ 0 & 0 & K_i & 0 \\ 0 & 0 & 0 & K_i \end{bmatrix} \begin{bmatrix} i_{1\alpha}^*(k+1) \\ i_{2\alpha}^*(k+1) \\ i_{1\beta}^*(k+1) \\ i_{2\beta}^*(k+1) \end{bmatrix}
\end{aligned}$$

Then

$$\begin{bmatrix} i_{1\alpha}(k+1) \\ i_{2\alpha}(k+1) \\ i_{1\beta}(k+1) \\ i_{2\beta}(k+1) \\ f_{1\alpha}(k+1) \\ f_{2\alpha}(k+1) \\ f_{1\beta}(k+1) \\ f_{2\beta}(k+1) \\ b_{1\alpha}(k+1) \\ b_{2\alpha}(k+1) \\ b_{1\beta}(k+1) \\ b_{2\beta}(k+1) \end{bmatrix} = \mathbf{G}^{-1}\mathbf{F} \begin{bmatrix} i_{1\alpha}(k) \\ i_{2\alpha}(k) \\ i_{1\beta}(k) \\ i_{2\beta}(k) \\ f_{1\alpha}(k) \\ f_{2\alpha}(k) \\ f_{1\beta}(k) \\ f_{2\beta}(k) \\ b_{1\alpha}(k) \\ b_{2\alpha}(k) \\ b_{1\beta}(k) \\ b_{2\beta}(k) \end{bmatrix} + \mathbf{G}^{-1}\mathbf{H} \begin{bmatrix} i_{1\alpha}^*(k+1) \\ i_{2\alpha}^*(k+1) \\ i_{1\beta}^*(k+1) \\ i_{2\beta}^*(k+1) \end{bmatrix}$$

where

$$\mathbf{G} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & -G_{22} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & -G_{44} & 0 & -G_{42} & 0 & 0 & 0 & 0 & 0 \\ K_{tot} & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & K_{tot} & 0 & 0 & 0 & 1 & 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & K_{tot} & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & K_{tot} & 0 & 0 & 0 & 1 & 0 & 0 & -1 & 0 \\ K_i & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & K_i & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 1 & 0 & 0 \\ 0 & 0 & K_i & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & K_i & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 1 \end{bmatrix}$$

$$\mathbf{F} = \begin{bmatrix} 0 & F_{12} & 0 & 0 & 0 & G_{11} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & F_{22} & 0 & 0 & 0 & G_{21} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & F_{34} & 0 & G_{33} & 0 & G_{31} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & F_{44} & 0 & G_{43} & 0 & G_{41} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}; \mathbf{H} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ K_{tot} & 0 & 0 & 0 \\ 0 & K_{tot} & 0 & 0 \\ 0 & 0 & K_{tot} & 0 \\ 0 & 0 & 0 & K_{tot} \\ K_i & 0 & 0 & 0 \\ 0 & K_i & 0 & 0 \\ 0 & 0 & K_i & 0 \\ 0 & 0 & 0 & K_i \end{bmatrix}$$

A.2.3.1 Proportional Integral Current Regulator with Computational Delay

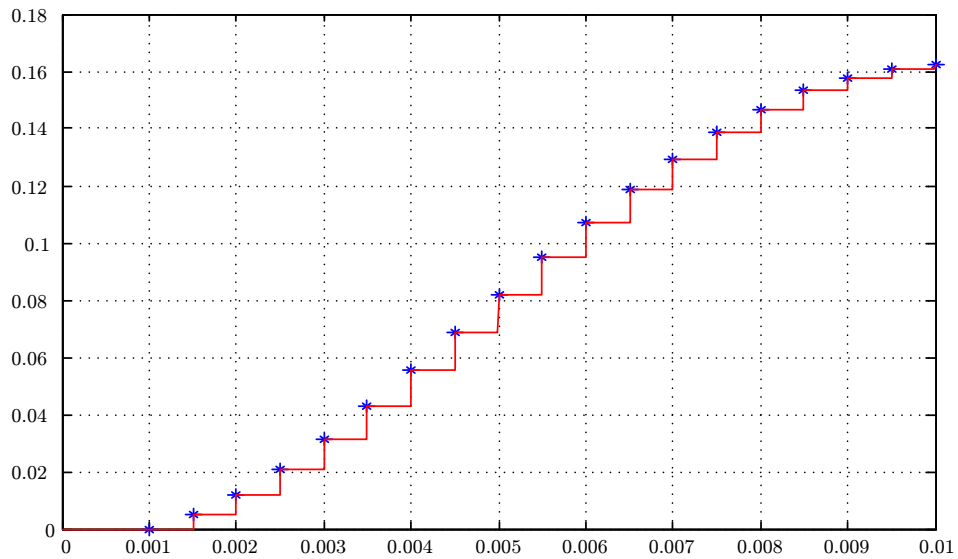
Output of computational delay:

$$f_{1\alpha/\beta}(k+1) = x_{2\alpha/\beta}(k)$$

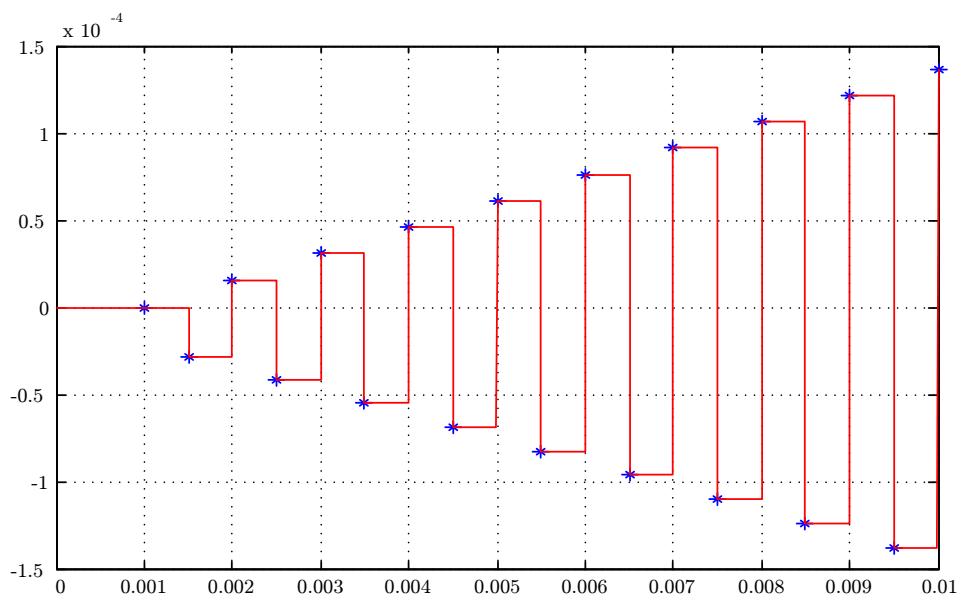
$$f_{2\alpha/\beta}(k+1) = x_{1\alpha/\beta}(k+1)$$

Include $f_1(k), f_2(k)$ in the state space representation.

$$\begin{bmatrix} i_{1\alpha}(k+1) \\ i_{2\alpha}(k+1) \\ i_{1\beta}(k+1) \\ i_{2\beta}(k+1) \\ x_{1\alpha}(k+1) \\ x_{2\alpha}(k+1) \\ x_{1\beta}(k+1) \\ x_{2\beta}(k+1) \\ b_{1\alpha}(k+1) \\ b_{2\alpha}(k+1) \\ b_{1\beta}(k+1) \\ b_{2\beta}(k+1) \\ f_{1\alpha}(k+1) \\ f_{2\alpha}(k+1) \\ f_{1\beta}(k+1) \\ w_{2\beta}(k+1) \end{bmatrix} = \mathbf{G}^{-1}\mathbf{F} \begin{bmatrix} i_{1\alpha}(k) \\ i_{2\alpha}(k) \\ i_{1\beta}(k) \\ i_{2\beta}(k) \\ f_{1\alpha}(k) \\ f_{2\alpha}(k) \\ f_{1\beta}(k) \\ f_{2\beta}(k) \\ b_{1\alpha}(k) \\ b_{2\alpha}(k) \\ b_{1\beta}(k) \\ b_{2\beta}(k) \end{bmatrix} + \mathbf{G}^{-1}\mathbf{H} \begin{bmatrix} i_{1\alpha}^*(k+1) \\ i_{2\alpha}^*(k+1) \\ i_{1\beta}^*(k+1) \\ i_{2\beta}^*(k+1) \end{bmatrix}$$



(a) Alpha Proportional + Integral Regulator + transport.



(b) Beta Proportional + Integral Regulator + transport.

Figure A.6: Test for three-phase PWM small-signal model simulated in Matlab©.