Development of a QPSK demodulator for the Sunsat 1 groundstation.

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Thesis presented in partial fulfilment of the requirements for the degree of Master of Science in Engineering at the University of Stellenbosch.

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Declaration

I, the undersigned, hereby declare that the work in this thesis is my own original work and has not previously in its entirety or in part been submitted at any university for a degree.

Signature

Date 2000/02/14

Abstract

The purpose of this thesis is the description of the development of a QPSK demodulator for the Sunsat 1 groundstation. A general overview of the functioning and requirements of a typical QPSK demodulator system is given. Several methods or algorithms for clock and carrier recovery are discussed. Specific attention is given to the QPSK demodulator chipset from Philips used for the implementation of the demodulator. The digital decoding logic used to serialize the parallel I and Q datastream is explained. Finally measurement techniques for performance evaluation of QPSK systems are investigated. As part of this the implementation loss of the developed QPSK demodulator is measured.

Opsomming

Die doelwit van hierdie tesis is om die ontwikkeling van 'n QPSK demodulator vir die Sunsat 1 grondstasie te beskryf. 'n Algemene oorsig oor die funksionering en vereistes van 'n tipiese QPSK demodulator stelsel word gegee. Verskeie algoritmes en tegnieke vir klok en draersein herwinning word ondersoek en bespreek. Spesifieke verwysing word telkens gemaak na die QPSK demodulasie vlokkie paar van Philips gebruik vir die implementering van die demodulator. Die digitale dekodering logika benodig vir die datastroom verpakking word ondersoek en beskryf. Laastens word daar gekyk na meettegnieke en evaluasie van QPSK demodulasie stelsels se prestasie. As deel hiervan word die implementasie verlies van die ontwikkelde QPSK demodulator stelsel gemeet.

Acknowledgements

To each and everyone who made this thesis possible, thank you.

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Symbols and abbreviations used

AD or ADC	Analog to Digital Converters
AGC	Automatic Gain Control
AM	Amplitude modulation
AWGN	Additive white gaussian noise
BER	Bit Error Rate
BPSK	Binary Phase Shift Keying
dB	decibel
DBS	Digital Broadcast Satellites
DSP	Digital signal processing
DMR	Digital microwave radio
Eb/No	Energy-per-bit to Noise spectral density ratio
EIRP	Equivalent isotropic radiated power
EPLD	Electronic progammable logic device
FD	Frequency detector
FDD	Frequency difference detector
FEC	Forward error correction
FM	Frequency modulation
FPGA	Field programmable logic array
HPA	High power amplifier
IC	Integrated Circuit
IF	Intermediate Frequency
ISI	Inter Symbol Interference
LNB	Low Noise Block
LNC	Low Noise Converter
LO	Local Oscillator
LSB	Least significant bit
MSB	Most significant bit
NF	Noise figure
NR	Noise ratio
NRZ	Non-return to zero
NRZI	Non-return to zero inverted
PCB	Printed circuit board
PD	Phase detector
PLL	Phase-locked loop
PN	Psuedo noise
PPM	Parts per million
PRBS	pseudo-random binary sequence
PSK	Phase shift keying
Q	Quality factor
QAM	Quadrature amplitude modulation
QPSK	Quadrature phase shift keying
RF	Radio frequency
SAW	Surface acoustic wave
S/N	Signal-to-noise Ratio
SNR	Signal-to-noise Ratio
VCO	Voltage controlled oscillator
VCXO	Voltage controlled crystal oscillator

Chapter 1

Introduction

The high-resolution pushbroom imager onboard the Sunsat 1 micro-satellite generates an enormous amount of image data that needs to be downloaded. This image data must be downloaded in the short time span, typically 10 to 15 minutes, that Sunsat is in range of the groundstation at Stellenbosch. Realtime downloading of image data requires even higher bitrates.

The lower microwave bands, 1 to 10 GHz, are popular for high-bitrate satellite downlinks. More bandwidth is available compared to VHF/UHF and the pathloss is not excessive.

When digital microwave signals are transmitted from satellite the most important constraint is the satellite power budget. The size of the satellite limits the power budget and thus the output power of the transmitter. The further large path loss from satellite to groundstation results in a received signal with a low signal-to-noise (SNR) ratio. For this reason robust modulation formats such as QPSK and OQPSK which are power efficient and tolerant to noise degradation are employed.

In this thesis the development a QPSK demodulator for the Sunsat micro-satellite project is discussed. The prototype demodulator hardware developed is shown in Figure 1.1.

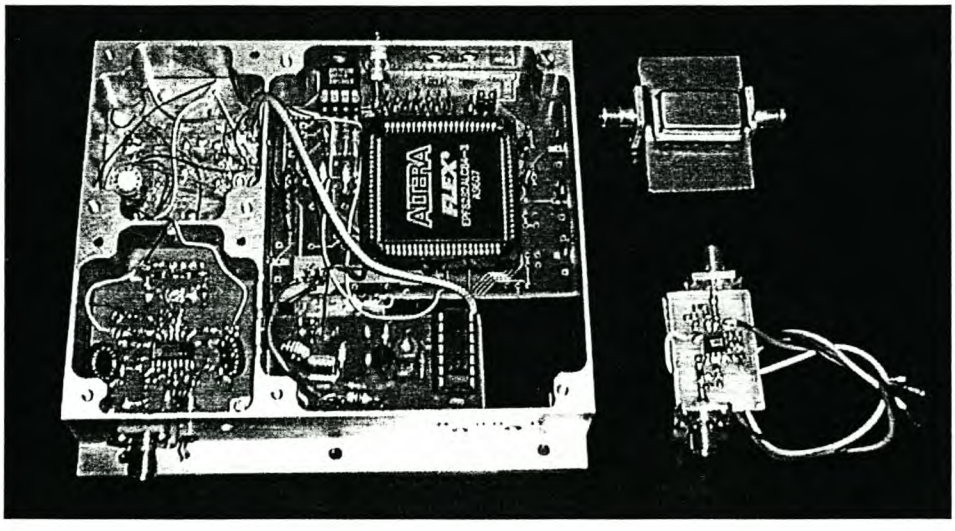


Figure 1.1: The fixed datarate demodulator (left) with SAW filter (top right) and AGC amplifier (bottom right).

This chapter provides high level block diagrams of a QPSK modulator and demodulator with a discussion of the theory involved. The various factors influencing the choice of receiver architecture are also introduced.

1.1 QPSK modulation and demodulation

1.1.1 QPSK Modulation

QPSK modulates the phase of the carrier signal rather than using the amplitude or frequency to convey information. The carrier is forced into one of four different phase states. The main advantage of QPSK over BPSK or other binary techniques is that each symbol contains two data bits, thus doubling the potential quantity of data that is transmitted in a given bandwidth.

The digital input stream is split into two parallel data streams at half the rate of the original bit rate and mapped to symbols. Each symbol is represented by a value of I and Q. This I/Q plane with the possible symbol states is also called a constellation diagram.

The rate or frequency at which the symbols change value is called the symbol rate, f_s or f_{symbol} and is the inverse of the symbol time ($T_s = 1/f_{symbol}$). QPSK has a symbol rate half that of the bit rate whereas for BPSK the bit rate and symbol rate are the same.

Low pass filters are used to shape the digital symbols into analogue voltages suitable to drive a quadrature modulator. If the analogue sequences are represented by i_n and q_n, the i_n signal is multiplied with $\cos\omega_o(t)$ and q_n with $-\sin\omega_o(t)$. These translated signals are added and then bandpass filtered to produce the RF signal.

A blockdiagram of the modulation process is shown in Figure 1.2.

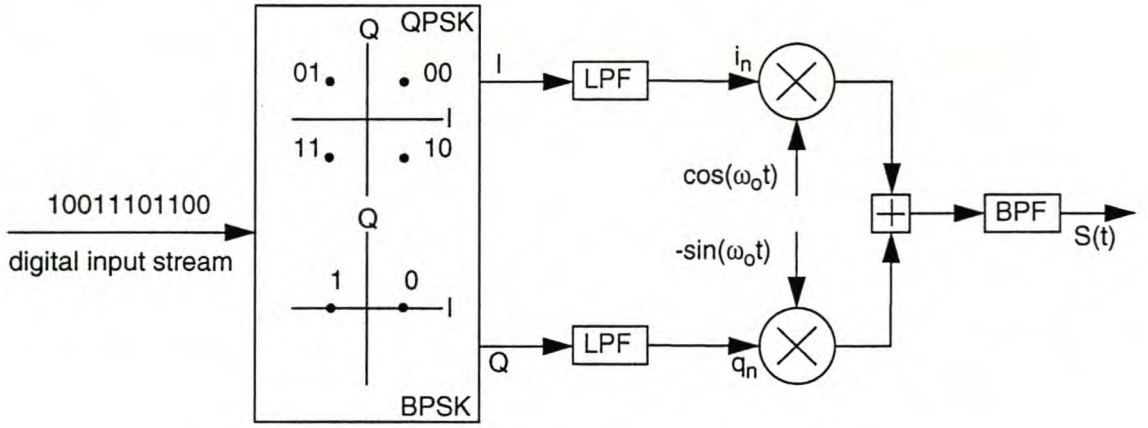


Figure 1.2: BPSK/QPSK modulator blockdiagram [1].

The modulator output signal $S(t)$ can be expressed as:

$$S(t) = \sum i_n h(t - nT_s)\cos(\omega_o t) - \sum q_n h(t - nT_s)\sin(\omega_o t) \tag{1.1}$$

where $h(t)$ is the pulse shape of the low pass filter and band pass filter combined.

The discrete frequency components of the carrier, w_o, and the symbol clock, T_{symbol}, are completely suppressed during the modulation process and have to be recovered at the demodulator. This is the function of the clock and carrier recovery loops (see Chapter 2).

1.1.2 Offset keyed QPSK (OQPSK) Modulation

An objective of QPSK modulation is a constant waveform envelope where the signal phase conveys the information. In practice the signal envelope fluctuates due to filter effects on the phase transitions. The nonlinear amplifiers used in satellite applications reduce the envelope fluctuations but cause spectrum regrowth or regeneration. This regeneration can cause unacceptable interference to adjacent frequency bands.

To decrease envelope variations due to filtering, offset QPSK (OQSPK) is often employed.[1] A one-bit delay (T_b) is introduced in the quadrature baseband datastream which cause the phase transitions of the modulator to be separated by $T_b = T_s/2$ seconds.

The maximum phase transition in an OQPSK waveform is 90° compared to the 180° of a QPSK waveform although these transitions occur at double the frequency of the QPSK transitions. The reduced magnitude of the phase transitions results in a reduced variation of the OQPSK envelope and thus less spectral regeneration.

1.1.3 QPSK Demodulation

The quadrature demodulator mixes the input signal with an in-phase and quadrature-phase carrier signal to produce the analogue I and Q signals. The received signal $S(t)$ is thus multiplied by a $\sin(\omega_o t + \phi)$ and with $\cos(\omega_o t + \phi)$ component, where ϕ is the phase difference between the received and locally generated carrier frequency. After mixing, both I and Q signals are low pass filtered to remove the high order mixing products. A blockdiagram of the demodulation process is shown in Figure 1.3.

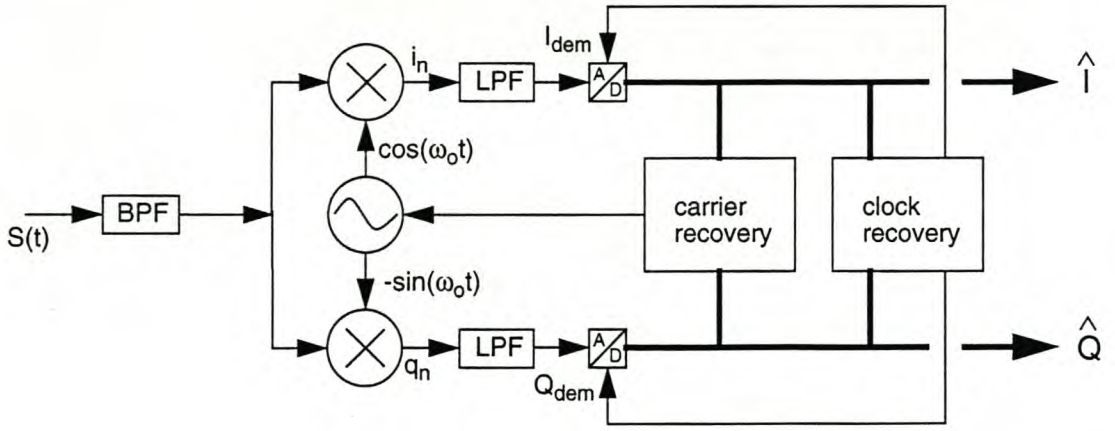


Figure 1.3: BPSK/QPSK demodulator blockdiagram [1].

[1]OQPSK is also referred to as staggered QPSK (SQPSK). This should not be confused with unbalanced QPSK where unrelated datastreams are sent in the I and Q channel.

If the phase error ϕ is zero, the I and Q channel output after filtering will be:

$$S_i(t) = \sum_n i_n p(t - nT_s) \tag{1.2}$$

$$S_q(t) = \sum_n q_n p(t - nT_s) \tag{1.3}$$

where $p(t)$ is the channel transfer characteristic.

For non-zero phase difference ϕ the output is given by:

$$I_{dem} = S_i(t)\cos(\phi) + S_q(t)\sin(\phi) \tag{1.4}$$

$$Q_{dem} = S_q(t)\cos(\phi) + S_i(t)\sin(\phi) \tag{1.5}$$

It can be seen that there will be no crosstalk between the I and Q channels when the following expression is true:

$$\phi = 0 \pm n\frac{\pi}{2} \tag{1.6}$$

The above equation shows that four combinations are possible where $I_{dem} = \pm S_i(t)$ or $\pm S_q(t)$ and where $Q_{dem} = \pm S_q(t)$ or $\pm S_i(t)$ respectively. This results in a phase ambiguity of $n\times 90°$ or a rotation of the constellation diagram by $n\times 90°$. Phase ambiguity is inherent in PSK systems and must be removed by coding or other means.

For values different from $\phi = 0 \pm n\frac{\pi}{2}$, the second term in each equation for I_{dem} and Q_{dem} represents crosstalk. The carrier recovery loop should ensure that $\phi = 0 \pm n\frac{\pi}{2}$ in order to minimize crosstalk for static values as well as fluctuations (phase jitter).

From Figure 1.3 it can be seen that the intention is to extract the clock and carrier recovery control information from the baseband digital I and Q channels.

1.2 Demodulator system requirements

The following criteria serve as guidelines to the requirements of a demodulation system.[2]

Modulation formats supported

QPSK modulation is popular for low-power satellite reception, while BPSK is often used as a backup for poor communication conditions. The use of OQPSK is also desirable as this results in less spectral regeneration in the transmitter power amplifier.

Minimum Eb/No

The received signal from a satellite is low compared to the thermal noise of the receiver, resulting in a low SNR. A typical minimum signal level value for which the demodulator should acquire and remain in lock is Eb/No = 5 dB [1].

[2]The application note of the Philips chipset [1] as well as existing groundstation hardware were used as guidelines to help determine the necessary demodulator requirements.

Filter roll-off

A square-root raised-cosine filter with a suitable roll-off factor is standard in digital microwave radio [1]. The roll-off factor used is determined by the application. Excess bandwidth in the order of 40 to 100% is common for satellite applications.

Symbol rate

The expected range is between 20 and 30 Msymbols/s for the Sunsat micro-satellite application. The assumption is made that once the symbol frequency is selected it remains fixed for the duration of a transmission.

The required clock frequency for the imaging system to generate square pixels can be calculated using simple orbit mechanics. To enable realtime downloading of images the communications link must be able to operate at this datarate. The resulting datarate varies between 38 Mb/s at apogee and 52 Mb/s at perigee as shown in Figure 1.4. The Matlab calculations are provided in Appendix A.

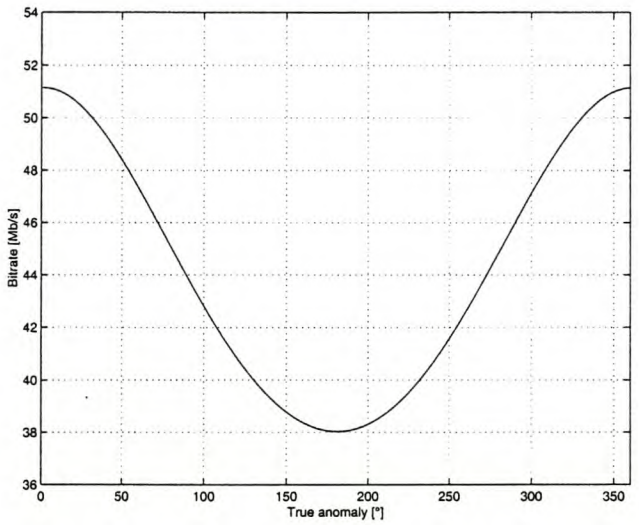


Figure 1.4: Required bitrate for square imager pixels.

Symbol rate uncertainty

If both the transmitter and receiver make use of a crystal clock the combined clock frequency uncertainty will be in the order of $\pm$ 100 *ppm*. This uncertainty is due to the drift and aging of each crystal used.

Intermediate frequency

The preferred standard intermediate frequencies at which demodulation is performed are: 70 MHz, 140 MHz, 480 MHz and 612 MHz.

Intermediate frequency uncertainty

The local oscillator in the low noise converter (LNC) will drift mainly due to temperature variations. The resultant IF uncertainty that the demodulator has to track is in the order of ±2.5 MHz [1]. Other factors on the transmit side as well as Doppler frequency shift due to relative movement between transmitter and receiver also contributes to the frequency uncertainty.

Doppler shift and Doppler shift rate consideration
Doppler shift due to the relative movement between the satellite and groundstation causes frequency shifts in the order of 60 kHz and is therefore only a small contribution to the overall frequency uncertainty. A simulation of the Doppler shift for a direct overhead pass is shown in Figure 1.5. The Matlab source can be found in Appendix B.

The rate of Doppler frequency shift is also important. If the PLL loop bandwidth is not wide enough it will not be able to track the change in carrier frequency. Figure 1.5 also shows the rate at which the Doppler frequency shift changes.

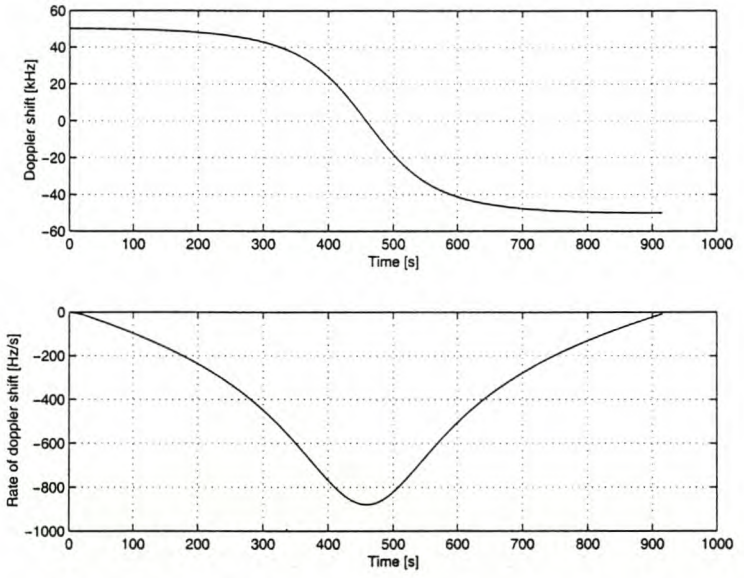


Figure 1.5: Doppler frequency shift and rate of shift (direct overhead pass).

Range of input levels and AGC range

The received modulated signal level will vary due to variations of the losses between the LNC and the receiver. Also changes in weather conditions and satellite antenna orientation will cause signal level variations. To avoid overload of the receiver stages, an automatic gain control (AGC) function must be implemented.

The received signal levels at the receiver input are expected to be between -65 and -35 dBm after antenna, preamplifier and satellite receiver gain is taken into account. A 30 dB AGC range is therefore considered sufficient.

Implementation loss

The difference between the theoretical and measured curves for the Bit Error Rate (BER) as a function of Eb/No is defined as the implementation loss. This loss is normally specified at a certain BER value. An implementation loss of 1 dB at $BER = 10^{-4}$ is generally accepted for the total modulator, satellite and demodulator imperfections [1].

Lock detector

The received Eb/No should be estimated to monitor the quality of the satellite link. This can be used to detect valid BPSK or QPSK signals as well as to control the orientation of the receiving antenna.

Digital decoding

Digital decoding logic is necessary to serialize the datastream as well as NRZ decoding. Custom programmable logic devices, FPGA (Field programmable gate arrays) or digital signal processors are the most common devices used.

1.3 Thesis presentation

The presentation of the thesis document is given below:

Chapter 2 briefly discusses the range of carrier and clock recovery methods available in digital radio. Particular attention is given to the methods used in the Philips chipset used to realise the QPSK demodulator hardware.

The quadrature demodulation is performed by a chipset from Philips. The chipset consists of the TDA8040 quadrature demodulator and the TDA8041 quadrature demodulator controller. The characteristics of the chipset are discussed in detail in Chapter 3.

Chapter 4 gives detail design information on the peripheral circuitry required to complete the demodulator functions. The peripheral circuitry includes the loop filter components of the clock and carrier recovery phase locked loops.

Chapter 5 describes the digital logic necessary in the demodulator. As the demodulator logic is closely related to the modulator logic this is described where necessary.

Chapter 6 deals with the performance analysis of digital microwave radio as applied to the QPSK system. The measurement of the implementation loss of the demodulator system is given.

Chapter 7 concludes the thesis and makes suggestions for improvements. The scope for future research is discussed.

Chapter 2

Clock and carrier recovery methods

2.1 Data synchronizers

In order to transmit a data stream over a communication channel, it must be modulated onto a carrier frequency. When data is transmitted synchronously, optimum detection of data at the receiver requires a local carrier wave and clock generator that are in phase agreement with the received carrier and data stream respectively.

The circuits that generate the receiver clock and carrier signals are known as synchronizers. Phase-locked loops (PLLs) are widely used in these synchronizers to lock onto the desired frequency component.

Efficient modulation techniques suppress the carrier ensuring that all transmitted energy resides in the data sidebands and none is wasted in transmitting a carrier. Efficient data pulse streams also contain no discrete component at the clock frequency. Synchronizers require a discrete signal component at the frequency to be tracked. Suitable nonlinear circuits are therefore required to regenerate a carrier or clock signal component.

2.1.1 Carrier synchronizers

The three main types of carrier synchronizers used for suppressed carrier modulated signals are: the squaring loop, the remodulator and the Costas loop.

Squaring loop

In a squaring loop a nonlinear element is modeled as a square-law device. Passing a suppressed carrier signal through this square law device results in a frequency component at double the carrier frequency. A conventional PLL operating at double the carrier frequency is able to lock to the second harmonic component. The VCO frequency is then simply divided by two to provide the desired reference carrier.

A simple square law rectifier has the following advantages [3]:

- Noise performance is near optimum, especially at low SNR.

- A pure sine input results in pure sinusoidal output at double the frequency.[1]
- A square law is a mathematically manageable non-linearity.

Remodulator

The incoming signal is demodulated and the message waveform $m(t)$ is recovered. This baseband waveform is then used to remodulate the incoming signal. If the waveforms are rectangular and time aligned, then the remodulation removes the modulation completely. A pure carrier component at the input frequency results which can be tracked by a PLL.

Costas loop (2PSK)

The Costas loop is a phase-locked loop configuration used for carrier phase recovery from suppressed-carrier modulation signals. The receiver consists of two coherent detectors fed with the same input signal, but with local oscillators that are in phase quadrature to each other (see Figure 2.1). When the phase of the local oscillator equals the incoming carrier wave the I-channel output contains the desired demodulated signal and the Q-channel output is zero.

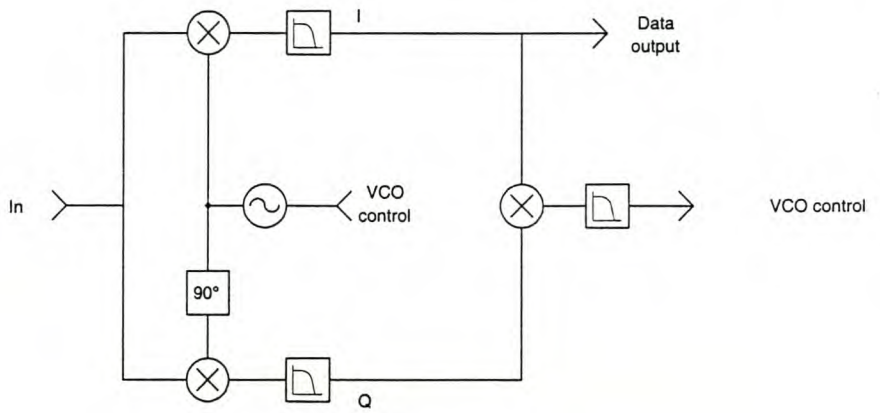


Figure 2.1: The two-phase Costas loop.

If the LO phase differs from the incoming carrier phase by ϕ radians the Q-channel output will increase proportional to $\sin\phi \approx \phi$. This increase will have the same polarity as the I-channel for one direction of LO phase drift and the opposite for the other direction of LO phase drift.

The I- and Q-channel outputs are combined in a phase discriminator (consisting of a multiplier followed by a low-pass filter) providing a DC control signal to the VCO. Phase control ceases when modulation ceases and phase-lock has to be re-established with the reappearance of modulation [6].

The four phase (4PSK) Costas loop is similar to the two phase version but is able to lock to any one of four distinct phases (for a more detail of the Polarity-type Costas loop see Section 2.2.1).

[1]Passing a BPSK signal, $v_s(t) = m(t)sin(w_it + \theta_i)$, through a square law non-linearity results in $v_x(t) = m^2(t)sin^2(\omega_it + \theta_i) = 1/2m^2(t)[1 - \cos(2\omega_it + 2\theta_i)]$.

Decision directed methods

The remodulator removes modulation by multiplying by the demodulated message waveform in analog form. Better noise rejection characteristics are possible if the message is detected first and the digital message is used for modulation removal. This method of obtaining an unmodulated carrier by multiplying with an estimate of the modulation is termed *decision-directed* feedback.

A decision directed circuit cannot acquire the carrier until clock has been acquired and may not be able to acquire the clock until the carrier has been acquired. Thus decision-directed synchronizers may not be acceptable if fast acquisition is required.

Phase ambiguity

A fundamental ambiguity of all phase-shift modulation techniques exists. If the information is transmitted using N different phases there is an N-fold ambiguity in the data recovery. The ambiguity is not a defect of the recovery loop but an inherent characteristic of suppressed-carrier, phase-shift keying modulation. Special encoding or other information in the data is needed to resolve the ambiguity.

2.1.2 Clock synchronizers

In a digital communication link the timing information related to the received data bits must be extracted at the receiver end. The clock recovery purpose is the correct strobing of received data bits to ensure the optimum data decision.

The transmitted spectrum of baseband, square-waveform, random, non-return-to-zero (NRZ) signalling has a spectral null at the clock frequency (f_c). Since non-return-to-zero inverted (NRZI) coding is essentially NRZ data that changes state according to the input data polarity, the output spectrum is the same as that of NRZ data. The power spectral density is shown graphically in Figure 2.2 and can be expressed as:

$$S_y(\omega) = A^2 T_b Sa^2(\omega T_b/2) \tag{2.1}$$

A non-linear process is again needed for recovery as there is no clock frequency component to filter out. Clock synchronizers can be categorized according to the bandwidth of the communications system.

Wideband systems

In wideband systems the bandwidth greatly exceeds the signaling rate and signaling pulses are essentially confined to single symbol intervals. A few wideband synchronization methods are discussed below:

Maximum Likelihood trackers
For confined waveform pulses (wideband systems) there is an optimum clock timing known as the maximum likelihood (ML) estimate or maximum *a posteriori* (MAP) estimate. The optimum estimate uses an open-loop search and measure implementation,

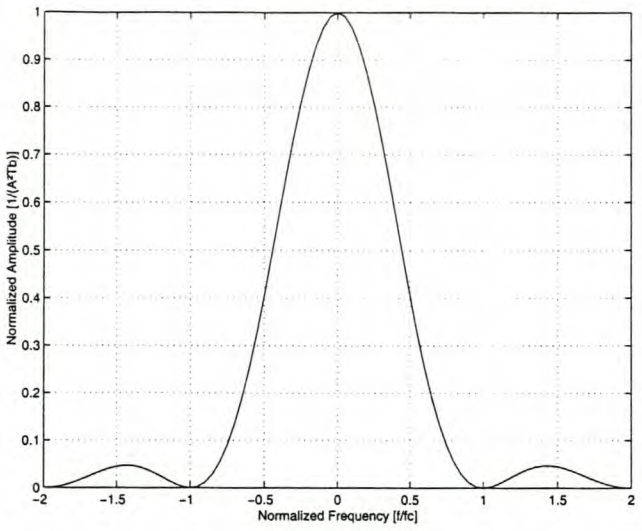


Figure 2.2: Power spectral density of random NRZ data.

which assumes the clock phase is stable once the optimum estimate is found. The derivation does not allow for evaluation of errors in the estimate.

Early-late gates
In an early-late gate synchronizer each received data symbol is sampled once on either side of the data strobe instant. If the strobe timing is at the optimum position the difference between the two sample values will be zero. The value of one sample increases and the other decreases as the timing error increase. The difference between these two values is an indication of timing error.

Random data is required as this method only derives clock error information during data transitions. A low-pass filter is used to smooth the detector timing error voltage applied to the clock generation circuit.

Transition-tracking loop
In the transition-tracking loop an error signal is produced by integration over a transition. If the transition is exactly centered within this integration period, the integration result is zero. As soon as the transition is not centered, a positive or negative integration error output is produced.

The error output can be low-pass filtered to provide an error control voltage. If no data transition is present no information is presented at the detector output.

Narrowband systems

Narrowband systems approach the Nyquist limit, where pulse shapes spread over many symbols and ISI (intersymbol interference) is possible. Due to the pulse overlap, correlators or gated integrators are ineffective for clock regenerators.

In narrowband systems data detection is accomplished by sampling the filter output. To avoid ISI pulses are given Nyquist shaping where the response of one pulse goes through zero at the sampling times of all other pulses. This approach works well on data detection but the clock synchronizer is affected by ISI.

The recovered clock wave has a jitter component caused by the data pattern due to ISI. This is also called pattern noise or pattern jitter and in many applications predominates additive noise effects. Pattern jitter worsens as the bandwidth becomes constricted. A suitable prefilter prior to the regenerator can suppress pattern jitter.

Narrowband methods include full-wave rectifiers, zero crossing detectors and sampled derivative detectors.

Full wave rectify
A popular non-linear method is to full-wave rectify the baseband data signal. The rectified signal is bandpass filtered to obtain a signal component at the clock frequency. The phase of the clock signal is corrected to align with the midpoints of the databits.

Differentiate data method
Another method to recover the clock is to differentiate the baseband data and then stretch the differentiated pulses. A latch is used as a delay element and a XOR gate is used to differentiate the data. The output of this circuit has to be filtered with a bandpass filter to recover the clock component.

Zero crossing detector
For NRZ coding the bit boundaries are identified by the data transitions. At these transitions a pulse is generated which can be filtered and applied to a phaselock loop.

A popular all digital method used in packet radio TNCs is implemented as follows. A locally generated 16× clock is used to generate the required local 1× clock. The local 1× clock is compared to the hard-limited baseband analog data and is advanced or retarded by one state (1/16 of a data bit time) depending on whether the clock is early or late.

One disadvantage of this method is that there is no proportionality in the feedback, the recovered clock is always either early or late. The smallest error possible is one-half the adjustment time (1/32 for 16× clock). A higher (64×) clock rate is needed for improved accuracy.

2.2 Carrier recovery

The carrier loop detector largely determines the performance of the demodulator [4]. The following carrier recovery methods are available in the Philips chipset and are discussed in more detail in the following sections:

- A polarity-type Costas phase detector.
- A track-and-hold device at the Costas phase detector output.
- A balanced quadricorrelator for larger frequency offsets.

2.2.1 Polarity-type Costas loop

The polarity-type Costas loop is implemented in the Philips chipset, the functioning of this tracking loop is discussed in this subsection.[2] A blockdiagram of the polarity-type loop is given in Figure 2.3.

[2]The description of the phase detector characteristics and equations in this subsection are based on the paper by Van der Wal and Montreuil [4].

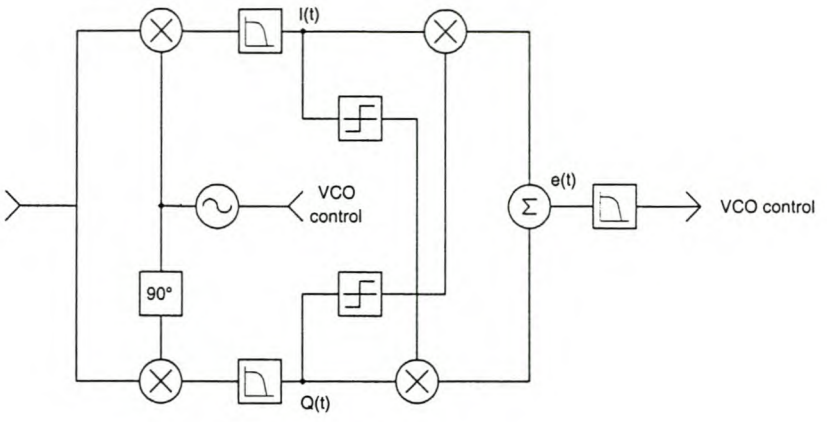


Figure 2.3: Blockdiagram of Polarity-type Costas loop.

Using the symbols defined in Figure 2.3 the Polarity-type baseband algorithm suitable for use in BPSK demodulation is reproduced in equation (2.2) below [4] :

$$e(t) = sgn(I(t))Q(t) \tag{2.2}$$

The Polarity-type baseband algorithm for QPSK demodulation is given below [4]:

$$e(t) = sgn(I(t))Q(t) - sgn(Q(t))I(t) \tag{2.3}$$

A three-dimensional plot of the polarity type detector outputs for BPSK as well as QPSK is shown in Figure 2.4.

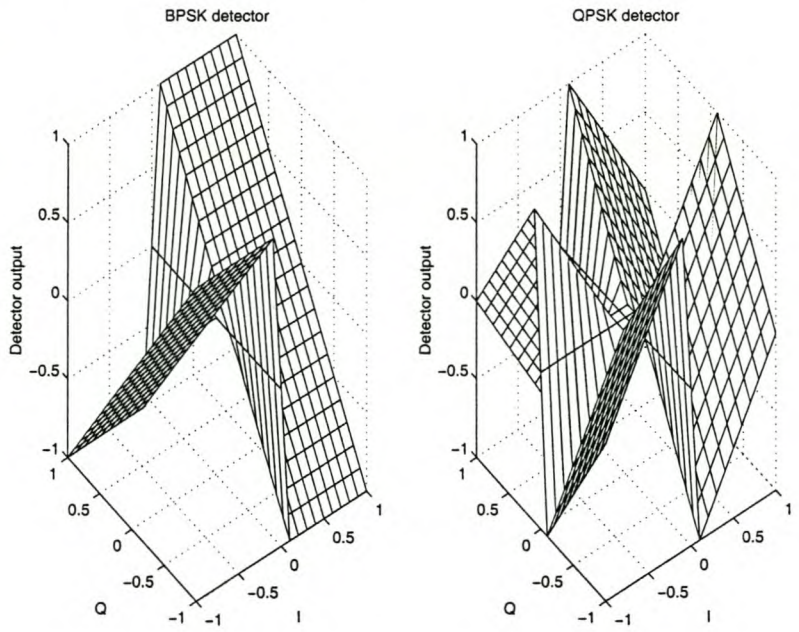


Figure 2.4: Polarity type detector outputs for BPSK and QPSK.

The Mth-power Costas loop however is the optimum tracking loop for low signal-to noise ratio (SNR) signals. The Mth-power loop for BPSK where $M = 2$ is given in equation

(2.4) below [4]:

$$e(t) = 2I(t)Q(t) \tag{2.4}$$

The Mth-power loop for QPSK where $M = 4$ is expressed as follows [4]:

$$e(t) = 4(I(t)^3Q(t) - Q(t)^3I(t)) \tag{2.5}$$

A three-dimensional plot of the detector outputs for the Mth-power loop BPSK as well as QPSK is given in Figure 2.5.

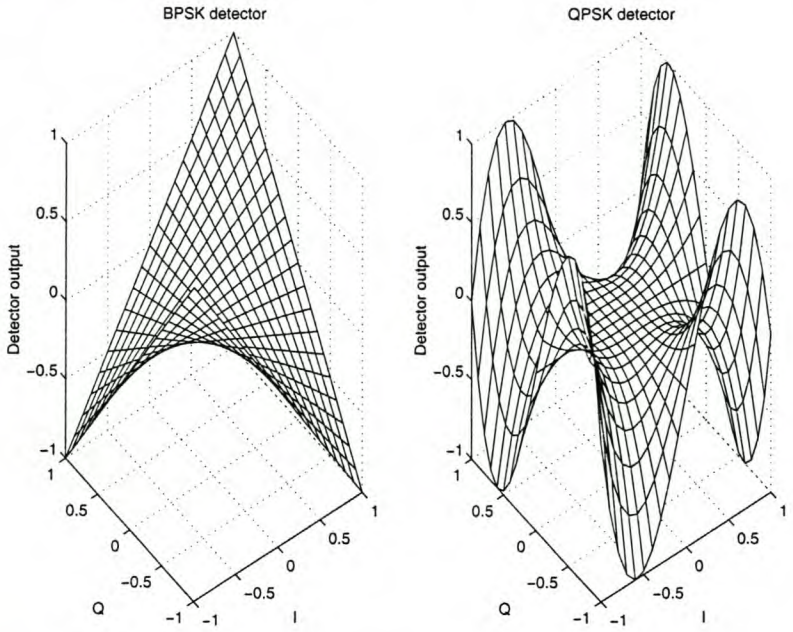


Figure 2.5: Mth-power loop detector outputs for BPSK and QPSK.

From equations (2.2) to (2.5) it is clear that the polarity-type Costas loop is simpler to implement than the Mth-power loop. At high SNR the polarity-type has a higher loop SNR and is also known as the high-SNR carrier loop. The performance of the two loops cross over at a SNR of -5 dB for BPSK and at 1.5 dB for QPSK [7]. Since these crossover points is below the minimum required Eb/No for the Sunsat application, the polarity-type loop as implemented in the Philips chipset is therefore adequate.

In the polarity-type loop the data estimates are used in forming the error signal to the VCO (decision directed method). The polarity-type loop is capable of OQPSK carrier tracking but modifications are necessary for unbalanced QPSK [7]. The S-curve of the limiter loop is dependant on SNR while that of the Mth-power loop is not.

These carrier recovery algorithms can be implemented using analogue as well as digital methods. Analog methods suffer the following impairments:

- Offsets in the analog multipliers and limiters of the I and Q branches.
- Amplitude and phase mismatch in the I and Q baseband signals.
- Temperature effects.

A digitally implemented detector is not affected by any of the above error sources. The information is processed only at valid symbol instants, reducing the variance in the detector output compared to analog implementations. However, analog to digital conversion errors such as non-linearity and overload should be kept in mind.

False lock behaviour

For large initial frequency errors the Costas loop acquisition can fail due to false lock to a data sideband, with the VCO frequency offset by half the data rate. The frequency error causes the phase error to change by 180° over a bit duration. The Costas loop interprets this as a possible phase change due to data.

This false lock characteristic presents a problem especially at high loop signal-to-noise ratios. The method of sweeping the VCO over the frequency uncertainty interval is dangerous as the offset frequency can be reached before the centre frequency.

Lock detector

A technique similar to the Mth-power Costas loop could be used to estimate the received Eb/No of a signal. The BPSK lock indicator equation is given in equation (2.6) below [4]:

$$e(t) = I(t)^2 + Q(t)^2 \tag{2.6}$$

The equation for the QPSK lock indicator is reproduced in equation (2.7) below [4]:

$$e(t) = I(t)^4 + Q(t)^4 - 6I(t)2Q(t)^2 \tag{2.7}$$

A plot of the BPSK and QPSK lock detector output is provided in Figure 2.6.

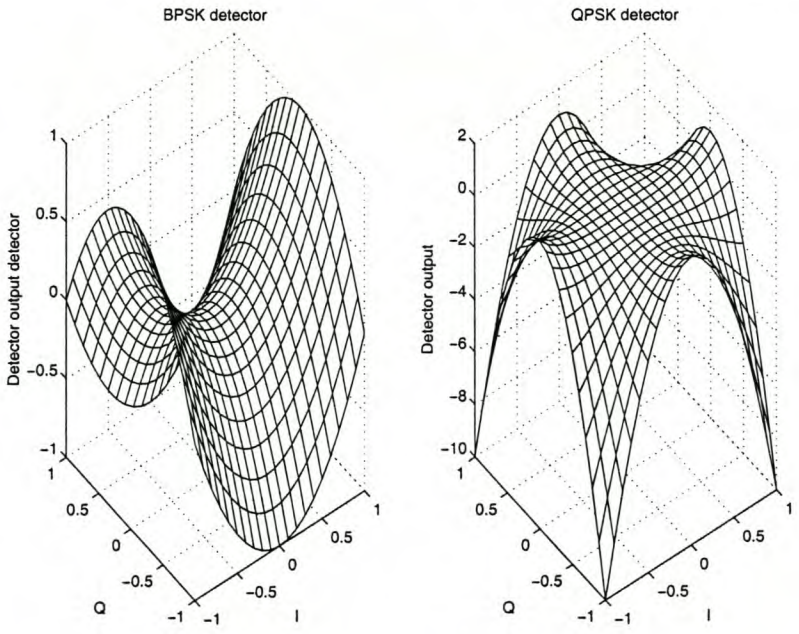


Figure 2.6: Mth-power lock detector outputs for BPSK and QPSK.

2.2.2 Phase and frequency detector

Two requirements that are not compatible in conventional PLL design, sufficiently small phase jitter and large acquisition or pull-in range, must be met in carrier recovery systems. A common approach is to design a narrowband loop that satisfies the phase jitter requirement. The acquisition range is then extended using acquisition aiding techniques such as the following:

- Loop filter switching.
  A large filter bandwidth is used during the acquisition phase. After lock is achieved the loop is switched to a narrower filter. This requires a lock detector to control switching between filters.

- Nonlinear element in loop filter.
  A nonlinear element in the loop is used between phase detector and the loop filter or the loop filter itself could contain a nonlinear element. A loop filter parameter therefore depends on the magnitude of the phase detector (PD) output and thus loop behaviour changes as phase lock is achieved.

- Frequency sweeping.
  The IF oscillator or VCO frequency is swept over the carrier uncertainty interval by adding a periodic signal (sinusoidal or triangular) to the PD output. Sweeping is stopped when lock is acquired to avoid the increase of phase jitter.

  A serious limitation of this method is that the loop acquires lock only if the sweep rate is less than approximately half the natural frequency of the loop [8].

- Frequency detectors.
  Frequency detectors (FD) are used only for frequency acquisition and are not suitable for phase acquisition and tracking. A FD is used in parallel with a PD and the respective outputs are summed after separate filtering. After lock is acquired the FD gives essentially zero output and no contribution is made to the steady state phase jitter.

Principle of track-and-hold device

The polarity-type Costas loop phase detector is changed to a phase and frequency detector with the addition of a track-and-hold device on the detector output (see Figure 2.7).[3] The method explained in this subsection uses a FD during acquisition and PDs during the steady state. It needs only a slight modification to a conventional PD and small additional circuitry.

Although the application requires a discrete-time phase detector (PD) a continuous time PD is used to explain the principle of transforming a PD into a frequency detector (FD). A sinusoidal PD characteristic is used as the operation of other PDs is similar.

In the steady state the PD phase error, defined as $\phi(t) = \phi_{local} - \phi_{received}$, fluctuates around a stable lock point of the form:

$$\phi_k = k\pi/2 \tag{2.8}$$

[3]The description of the track-and-hold device in this subsection is based on the paper by Sari and Moridi [8].

with k an integer.

During acquisition however the phase error $\phi(t)$ revolves at a rate proportional to the instantaneous frequency offset. If the loop is open and the radian frequency offset is $\Delta\omega$, then the phase error revolves linearly with time according to:

$$\phi(t) = \Delta\omega t + \phi(0) \tag{2.9}$$

The PD output is then a sinusoidal signal frequency $\Delta\omega$ with zero DC output and no information on the polarity of the frequency offset is available. A FD provides DC output proportional to, or at least of the same polarity as the frequency offset.

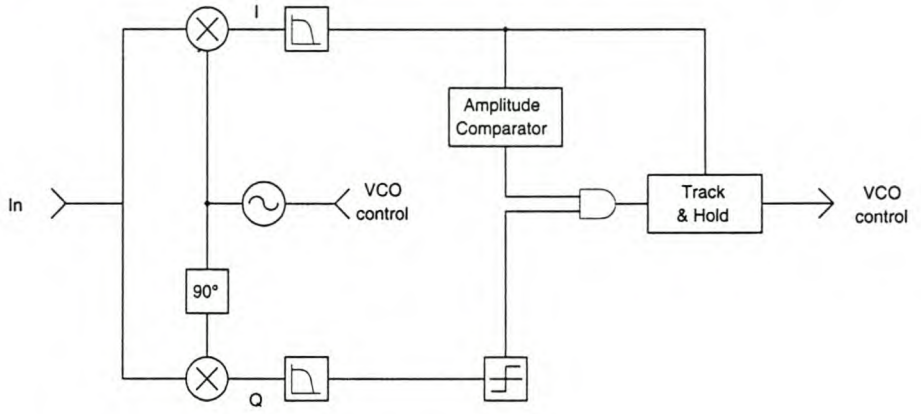


Figure 2.7: Block diagram of the phase and frequency detector.

A track-and-hold device added to the PD is able to provide frequency difference information using the following method:

- Track mode: The main PD output is followed (tracked) when $|\phi(t) - k\pi/2| < \theta$ with θ an arbitrary angle. In other words, the loop tracks when the instantaneous phase error falls within an interval of 2θ centered at a lock point $k\pi/2$.
- Hold mode: If the phase error is outside these stated intervals the output of the PD is held constant at the hold limit.

The track-and-hold device operates in track mode when the amplitude of the main PD output is smaller than $\sin\theta$ and the quadrature PD output is positive. It switches to hold mode when the main PD output is outside this interval. Another way to see this is that the main PD indicates whether the phase error is within a predetermined interval centered on the transition point and the quadrature PD output indicate stable lock points on the S-curve.

For a positive frequency offset the phase error is an increasing function of time. The in-phase and quadrature detector outputs for this case is shown in Subplot 1 and 2 of Figure 2.8. The PFD output shown in Subplot 3 of Figure 2.8 coincide with the original in-phase detector output on each interval from $k\pi/2-\theta$ to $k\pi/2+\theta$, but is held constant between these intervals. The positive DC output of the PFD is clearly visible.

For a negative frequency offset the phase error is a decreasing function of time. The in-phase and quadrature detector outputs for this case is shown together in Subplot 1

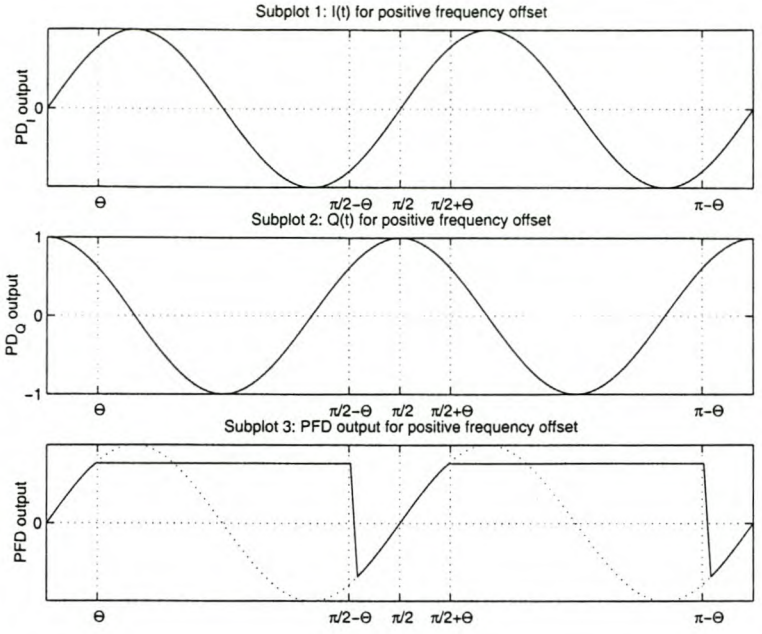


Figure 2.8: Modified detector output for positive frequency offsets.

and 2 of Figure 2.9. The interval where the in-phase detector output is followed spans from $k\pi/2+\theta$ downto $k\pi/2-\theta$. The tracking region is exited at the $k\pi/2-\theta$ point and the in-phase PD output is held constant at this value. The negative DC output of the PFD output is is clearly seen in Subplot 3 of Figure 2.9.

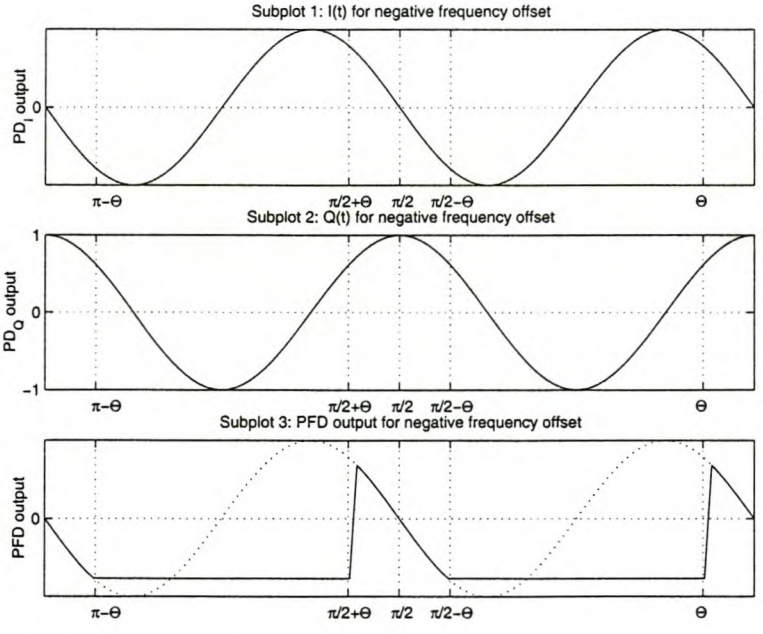


Figure 2.9: Modified detector output for negative frequency offsets.

Although the method is explained using a sinusoidal characteristic, the method is suitable to any PD characteristic.

In the absence of noise the DC at the detector output is [8]:[4]

$$\tilde{v} = \left(1 - \frac{4\theta}{\pi}\right) g(\theta) sgn(\Delta\omega) \tag{2.10}$$

where $g(.)$ is the PD characteristic, assumed to be an odd function of phase error.

In the steady state the phase error $\phi(t)$ remains small, the track-and-hold device is in track mode and the loop operates as a normal PD.

The choice of boundary point θ should maximize the DC at the detector output. The optimum value of θ for continuous-time implementations is approximately 16° for a sinusoidal PD and 22° for a sawtooth PD [8].

The track-and-hold method used is capable of extending the acquisition range of a carrier recovery loop by an order of magnitude. In multilevel-PSK systems no penalty is paid in steady-state phase jitter. However to avoid increased jitter in combined amplitude and phase shift keying systems it is necessary to switch back to the original PD after lock is acquired [8].

Application to carrier recovery

In PSK systems the transformation from PD to PFD using the method above is straightforward. All signal states are equispaced on a circle in the constellation diagram. To derive frequency information, the PD output is activated and passed to the loop filter when the demodulated signal point corresponds to an instantaneous phase error smaller than θ in value. Otherwise the previous output of the discrete-time PD is used as current input to the loop filter.

This method requires the following:

- Windows be placed around nominal points in the signal constellation.
- Control logic that tests at the sampling instant whether the demodulated signal sample is within the window.

The process is easily extended to apply to multilevel PSK systems. For combined amplitude and phase shift keying systems such as rectangular QAM direct application is not possible. A careful choice of suitable constellation points used in the algorithm must be made. Non-diagonal points have to be discarded due to phase ambiguity and also diagonal symbols that lie too close to the decision regions of other symbols.

FD characteristics and acquisition behaviour

The gain of the PFD derived from the above PD depends on the window size chosen around the constellation points. Higher detector gain is achieved with smaller values of θ which is in agreement with equation (2.10).

[4]The $\left(1 - \frac{4\theta}{\pi}\right)$ term is found by subtracting the area where the detector output is in track mode from the area that would result if the output would be in hold mode over the entire S-curve period.

In the noiseless case, the FD output is constant up to a frequency error (Δf) given by:

$$2\pi\Delta fT = \theta \tag{2.11}$$

where T is the symbol period, and θ the phase angle determined by the window chosen around the constellation point.

For larger frequency errors the FD characteristic gain decrease. The FD characteristic eventually undergoes a sign reversal after which acquisition is no longer possible.

A compromise exists between the highest detector gain possible versus the frequency range over which the FD characteristic has the correct sign. As extension of the acquisition range is the primary goal the window size is selected with this in mind.

For continuous time PDs the switching from track to hold mode occurs exactly at the boundary points. However for discrete-time PD the phase error hold process does not start exactly at the boundary points. For discrete time PD the derived FD characteristic is not rectangular and the DC output is optimized for small frequency offsets only, which is not useful for the purpose of frequency difference detection.

2.2.3 Frequency difference detector (Quadricorrelator)

Frequency tracking loops are used extensively in digital receivers as a frequency acquisition aid for coherent reception or as carrier frequency control for non-coherent reception. The quadricorrelator is the best known frequency difference detector (FDD).[5]

Simple quadricorellator

A pair of quadrature driven mixers are used to convert the input passband signal into the corresponding in-phase and quadrature baseband components as shown in Figure 2.10.

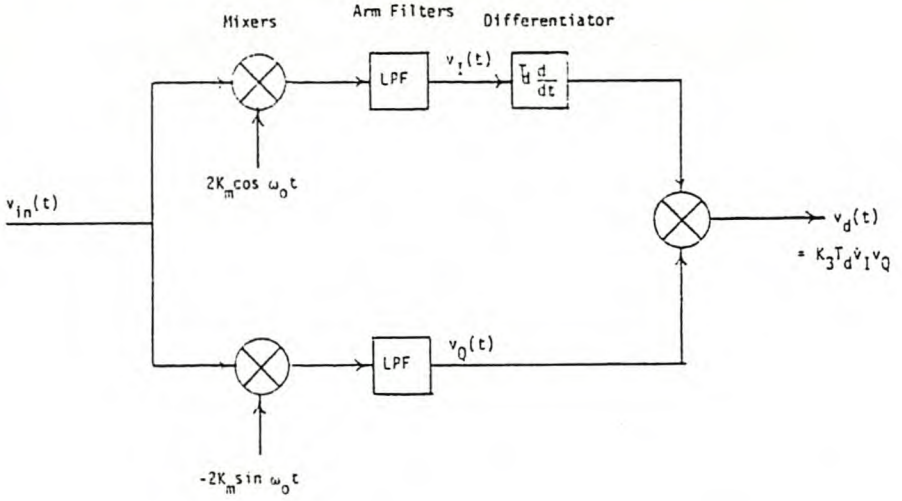


Figure 2.10: The simple quadricorrelator [2].

[5]The description of the quadricorrelator in this subsection is based on the paper by Gardner [2].

The mixers are represented as ideal multipliers but physical circuits could employ switching devices without affecting the results. Low-pass channel filters follow the mixers to suppress the sum frequency components and pass the difference components. Attenuation and phase shift of the difference frequency is not considered. The bandwidth of the arm filters provides a rough estimate of the frequency tracking loop capture range.

The output of one channel filter (I-channel) is differentiated. A perfect differentiator is assumed for the analysis. Although an absolute differentiator is unrealistic, perfect relative differentiation is possible.[6] The time constant (gain) associated with the differentiator is T_d.

Using the notation of Figure 2.10 the channel outputs are multiplied to produce:

$$v_d(t) = K_3 T_d v_Q(t) \dot{v}_I(t) \tag{2.12}$$

To gain further understanding of the operation of the quadricorrelator, let the input signal be a simple sinusoid of the form:

$$v_{in}(t) = V_S \cos(\omega_i t + \theta_i) \tag{2.13}$$

where θ_i is an arbitrary, time-invariant phase angle.

The frequency error is defined as $\Delta\omega = \omega_i - \omega_0$, where ω_0 is the radian frequency of the reference signal, the arm filter outputs are then calculated to be:

$$\begin{aligned} v_I(t) &= K_m V_S \cos(\Delta\omega t + \theta_i) \\ v_Q(t) &= K_m V_S \sin(\Delta\omega t + \theta_i) \end{aligned} \tag{2.14}$$

Differentiating the I-arm output and then multiplying the two arm outputs:

$$v_d(t) = -\frac{1}{2}\Delta\omega T_d K_m^2 K_3 V_S^2 [1 - \cos(2\Delta\omega t + 2\theta_i)] \tag{2.15}$$

This product consists of two components: a DC component proportional to the frequency difference (including its polarity) and a ripple component at double the difference frequency. The phase θ_i term occurs in the ripple only and not the DC component. The ripple component has the same peak amplitude as the DC component and is a source of tracking error.

Numerous variations of the basic quadricorrelator exist, mainly due to relaxing the specifications of the differentiator used. Let the differentiator be replaced by a network with transfer function $H_d(f) = A(f) \exp j\phi(f)$, where A is the amplitude and ϕ is the phase shift of the network frequency response. The output of this network with equation (2.13) as input will be:

$$\tilde{v}_I(t) = K_m V_s A(\Delta f) \cos(\Delta\omega t + \theta_i + \phi(\Delta f)) \tag{2.16}$$

The output of the quadricorrelator is:

$$\begin{aligned} v_d(t) &= K_3 v_Q \tilde{v}_I \\ &= -\frac{1}{2} K_3 K_m^2 V_s^2 A(\Delta f)[\sin\phi(\Delta f) - \sin\{2\Delta\omega t + 2\theta_i - \phi(\Delta f)\}] \end{aligned} \tag{2.17}$$

[6] Let one arm filter have a low-pass filter characteristic $H_a(s)$. If the other arm filter has a characteristic $sH_a(s)$, which is realizable if $H_a(s)$ is low-pass, perfect relative differentiation is achieved [2].

For any physically realizable transfer function $H_d(f)$, the amplitude $A(f)$ is an even function of frequency and the phase $\phi(f)$ is an odd function of frequency. The DC component in equation (2.17) , proportional to $\sin\phi(\Delta f)$, reverses polarity as the difference frequency passes through zero. The null at zero frequency exists for any filter $H_d(f)$ and is a property of the quadricorrelator not of the filter.

Frequency difference information is derived by rotating v_I into phase with v_Q. The amplitude of the DC component is proportional to $\sin\phi$ but the ripple amplitude is independent of ϕ. The largest possible DC component is therefore obtained for a phase shift as close as possible to 90°. The most effective phase shift is thus 90° as provided by a perfect differentiator.

Numerous networks could be used for the differentiating function, for example:

- a differentiator: $H_d(s) = sT_d$
- a high-pass filter: $H_d(s) = s^n H_L(s)$, where $H_L(s)$ is a low pass filter
- a low-pass filter: $H_d(s) = H_L(s)$
- a delay line: $H_d(s) = e^{-sT_d}$
- a delay-differencing network: $H_d(s) = 1 - e^{-sT_d}$

If the phase shift of H_d becomes excessive, $\sin\phi$ reverses polarity and the FDD output increase the frequency error instead of decreasing it. If the phase shift exceeds 270°, there will be one or more points of false lock where the frequency error is not zero.

Balanced quadricorellator

The balanced quadricorrelator shown in Figure 2.11 has ripple cancelling properties. It is a single-sideband cancellation scheme where the unwanted double-frequency component is cancelled and the desired DC components add together.

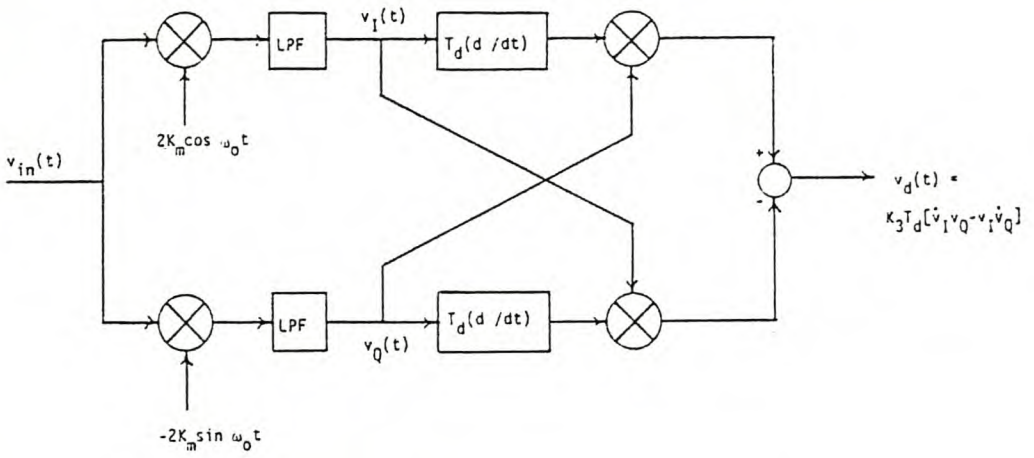


Figure 2.11: The balanced quadricorrelator [2].

From Figure 2.11 the output of the balanced quadricorrelator can be shown to be [2]:

$$v_d(t) = -\Delta\omega K_3 T_d K_m^2 V_S^2 \tag{2.18}$$

The unwanted double- or ripple-frequency component is cancelled. The phase θ_i of the input does not appear in the output expression thus no influence from signals with time-invariant input phases is experienced.

If the signaling pulse is time limited to a single interval then there is no pattern noise whatsoever due to cancellation that arises because of the balanced circuit [2] . Pattern noise arises only if pulses overlap. The unbalanced (simple) quadricorrelator not only offers no pattern noise cancellation but also contain product terms of pattern noise and ripple.

The loop will track the centre-of-gravity of the spectrum of certain classes of its input. If the noise spectrum is not symmetric on the centre of the data signal, the FDD will develop a noise bias. To avoid this bias a long tracking loop and a bandpass filter that is symmetric about the demodulation frequency is required. Notably this FDD is not suitable for single sideband or vestigial sideband modulation methods.

2.3 Clock recovery

2.3.1 Timing-error detector

The timing-error detector algorithm described in this subsection is intended for synchronous, binary, baseband signals and for BPSK or QPSK (balanced, nonstaggered) passband signals, with excess bandwidth of approximately 40 to 100%.[7] This excess bandwidth is typical of satellite communications such as the Sunsat S-band link with 80% excess bandwidth.

The detector requires two signal samples one of which is used for the symbol strobe (i.e. the sample on which the symbol decision is made). The algorithm is not decision directed and independent of the carrier phase (see 2.3.3).

2.3.2 Receiver model

The algorithm assumes a typical I-Q demodulator where the passband signal is demodulated to baseband with quadrature driven mixers as shown in Figure 2.12. Data filters follow the mixers, performing receiver filtering to shape signal pulses, minimize noise and suppress unwanted mixer products.

The sampling point is not specified and the filter outputs are thus available in sampled form as two real sequences $\{y_I()\}$ and $\{y_Q()\}$. The timing information is derived from these sequences.

The symbols are transmitted synchronously, spaced by a time interval T. Each sequence has two samples per symbol and the sample time is coincident between the two sequences. One sample is taken at the data strobe time and the other midway between strobe times.

[7]The description of the timing-error detector in this section is based on the paper by Gardner [3].

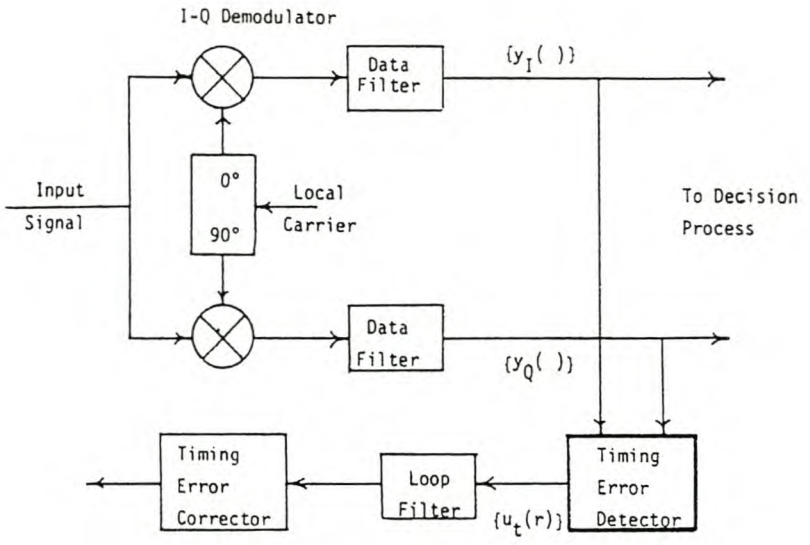


Figure 2.12: Typical I-Q demodulator [3].

If the index r is used to designate the symbol number, the values of the rth sample is denoted as $y_I(r)$ and $y_Q(r)$. The timing error detector operates on these samples and generate one error sample $u_t(r)$ for each symbol.

The resulting error sequence is smoothed by a loop filter before it is applied to the timing correction circuitry.

2.3.3 Derivation of algorithm

Waveform approach

The timing-error detector is described by reasoning from the data waveforms shown in Figure 2.13. The timing-error detector operation is described for a continuous baseband data signal rather than the discrete sequences as this is clearer to understand.

A moderately band-limited baseband signal $x(t)$ is shown in line C of Figure 2.13. The symbol boundaries of $x(t)$ are indicated with line A and the strobe locations with line B.

The data stream after square-law rectification is shown in line D. A DC component (inevitable output from a rectifier) plus a double frequency component at the symbol rate is evident.

This protoclock component is equivalent to a pure sinewave at the symbol frequency with gaps in the absence of data transitions. An analog clock recovery method could employ a narrowband filter or PLL to extract the desired clock and reject disturbances. The same method is possible in a digital system, but is computationally too complex. Sufficient reconstruction of the protoclock for DSP processing is not possible with only two samples per symbol.

Samples $\pm$ 1/4T from the strobe instant is at equal amplitude, opposite slope points of the protoclock. If timing is correct the difference (where data transition exists) between

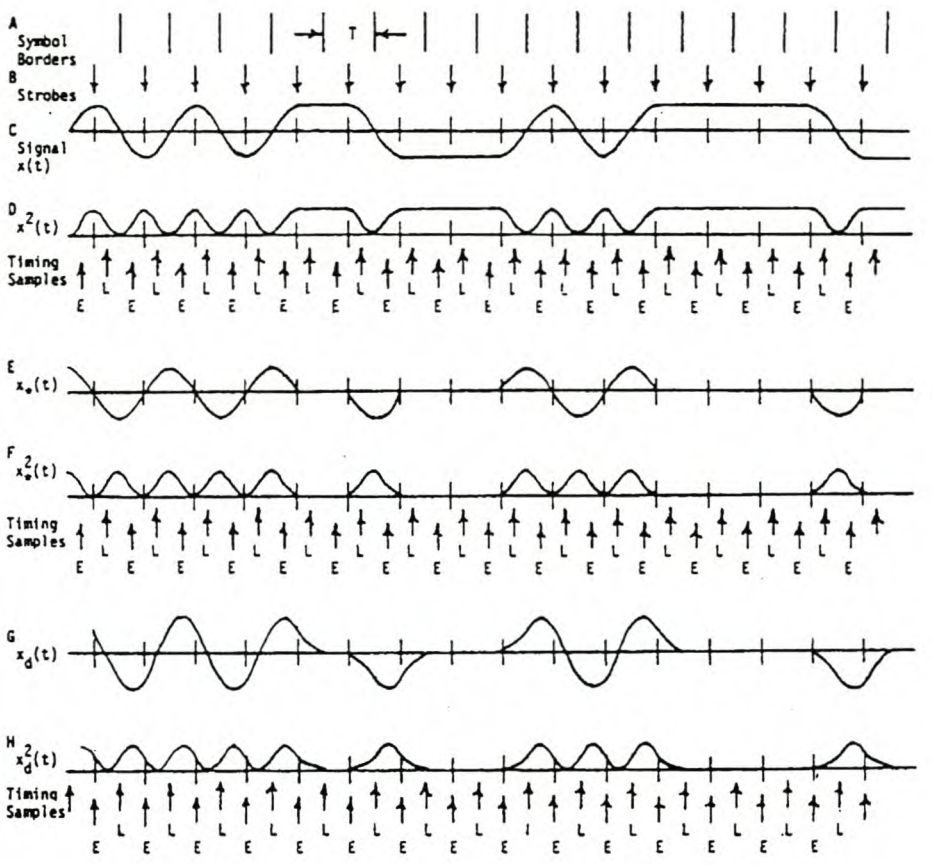


Figure 2.13: Waveforms of timing error detector [3].

the early E and late L sample is zero (E and L are indicated with arrows below line C in Figure 2.13). When the signal is delayed with respect to sampling, the value of one sample increases while the other decreases. This difference between sample values E and L is a measure of timing error.

Using the index r to indicate the timing sample (on line D) an introductory timing algorithm can be expressed as:

$$\begin{aligned} u_t(r) &= E(r) - L(r-1) \\ &= x^2(\tau + (r - 1/4)T) - x^2(\tau + (r - 5/4)T) \end{aligned} \tag{2.19}$$

where the rth strobe is taken at $t = rT + \tau$ and τ is the timing shift from the desired delay.

In the absence of additive noise and for ideal waveforms, $u_t(r)$ will be zero when transitions are absent. This feature avoids significant self noise.

Another possible algorithm for the timing error detector could be: $u_t(r) = E(r) - L(r)$. This algorithm generates large error information when no transitions are present. For random data these errors cancel in the long term, but adds considerable self noise in the short term.

Two deficiencies of the first algorithm need to be considered:

- Two samples per symbol are needed, neither of which is the data strobe. An additional sample is thus required for data sampling.
- No self noise is added with idealized time-limited waveforms but band-limited practical waveforms will cause self noise.

Prefiltering in front of the square-law rectifier as well as postfiltering is often employed to suppress self noise.

Prefilter method

Line E is the output $x_*(t)$ of a prefilter with $x(t)$ as input. For time limited pulses $x_*(t)$ is simply the derivative of $x(t)$. A protoclock is generated by rectifying $x_*(t)$ with the result shown in line F. Closer inspection of line F reveals that it is an inversion and level shift of line D. The same timing algorithm discussed above could be applied to this waveform.

The noise advantages of this prefilter is not obvious and the shift of timing samples from strobe location still remains a problem.

Delay differencing

A prefilter or differentiator can be approximated by the operation:

$$x_d(t) = x(t) - x(t - t_d) \tag{2.20}$$

with t_d a suitable delay time. If $t_d = T/2$ then the average delay of x_d is $T/4$, the time difference between strobe point and timing samples.

Line G is the result if the signal of line C is delay-differenced with a delay of $t_d = T/2$ and is similar but not identical to the signal of line E.

The delay-differenced waveform is square-law rectified and the result is shown in line H. The protoclock is again obtained and timing-error information can be derived from equation (2.19). The early *E(r)* sample coincides with the strobe time for the rth symbol and the need for a third sample is eliminated.

The timing error detector now only requires two samples per symbol and is performed with minimal computational burden. Only one subtraction and one squaring per symbol interval is needed. The detector algorithm also has self-noise rejection properties.

Formal reductions

If formal algebraic methods are used to derive the algorithm described above some elements that contribute no useful output can be eliminated.

Start with:

$$x_d(t) = x(t) - x(t - T/2) \tag{2.21}$$

and thus

$$x_d^2(t) = x^2(t) + x^2(t - T/2) - 2x(t)x(t - T/2) \tag{2.22}$$

Sampling at $t = rT + \tau$ and $t = rT + \tau - T/2$:

$$\begin{aligned} E(r) &= x_d^2(rT+\tau) \\ &= x^2(\tau + rT) + x^2(\tau + (r-1/2)T)\ldots \\ &\quad -2x(\tau + rT)x(\tau + (r-1/2)T) \end{aligned} \tag{2.23}$$

and

$$\begin{aligned} L(r-1) &= x^2(\tau + (r-1/2)T) + x^2(\tau + (r-1)T)\ldots \\ &\quad -2x(\tau + (r-1/2)T)x(\tau + (r-1)T) \end{aligned} \tag{2.24}$$

The algorithm can be rewritten without fundamental effect on operation as:

$$u_t(r) = L(r-1) - E(r) \tag{2.25}$$

The sign reversal in the algorithm cancels the $x^2(\tau + (r-1/2)T)$ terms and assures negative slope at the tracking point of the detector output.

Rewriting equation (2.25) using equation (2.23) to (2.24) results in:

$$\begin{aligned} u_t(r) &= x^2(\tau + (r-1)T) - x^2(\tau + rT)\ldots \\ &\quad +2x(\tau + (r-1/2)T)\{x(\tau + rT) - x(\tau + (r-1)T)\} \end{aligned} \tag{2.26}$$

The useful output of the algorithm is averaged over many samples thus $U_t(r) = Avg_r u_t(r)$ or,

$$\begin{aligned} U_t(\tau) &= Avg\{x^2(\tau + (r-1)T)\} - Avg\{x^2(\tau + rT)\}\ldots \\ &\quad +2Avg\{x(\tau + (r-1/2)T)(x(\tau + rT) - x(\tau + (r-1)T))\} \end{aligned} \tag{2.27}$$

The ensemble average cannot depend on index r because the underlying signal is cyclostationary [3] thus the first two terms in (2.27) must be equal and cancel.

The remaining terms are of the form:

$$\begin{aligned} u_t(r) &= x(\tau + (r-1/2)T)\{x(\tau + rT) - x(\tau + (r-1)T)\} \\ &= x(r-1/2)\{x(r) - x(r-1)\} \end{aligned} \tag{2.28}$$

This is the timing-detector for real, baseband signals. In processing a QPSK signal the timing detector is applied to each channel individually and then added resulting in equation (2.29).

$$\begin{aligned} u_t(r) &= y_I(r-1/2)[y_I(r) - y_I(r-1)]\ldots \\ &\quad +y_Q(r-1/2)[y_Q(r) - y_Q(r-1)] \end{aligned} \tag{2.29}$$

The independence of this algorithm to carrier phase as well as the derivation of the S-curve function is discussed in the following two subsections.

S-curve function

Design of the timing loop requires that the detector characteristic, average output versus timing error τ, is known. The complete derivation can be found in Gardner [3]. Only the result will be given and discussed here.

$$U_t(\tau) = -(4/T)\sin\frac{2\pi\tau}{T}\int_0^{1/T}\{G(f).G(1/T-f)\sin\pi fT\}df \tag{2.30}$$

$G(f)$ is the Fourier transform of $g(t)$ the shape of the filtered signal pulse. The average disappears at $\tau = 0$, corresponding to the center of each pulse, where the eye opening is maximum. The integrand is proportional to the product $G(f)G((1/T)-f)$. The region of overlap between these two functions contributes to protoclock generation. As excess bandwidth decreases, the overlap region shrinks and the gain of the detector decreases.

Carrier phase independance

It is shown below that the timing-error loop provides the same information irrespective of carrier phase.

Start with a time-continuous, complex signal at data filter output of:

$$w(t) = \{a(t) + jb(t)\}e^{j\Delta\theta} \tag{2.31}$$

which has rectangular components:

$$\begin{aligned} x_1(t) &= a(t)\cos\Delta\theta - b(t)\sin\Delta\theta \\ x_2(t) &= a(t)\sin\Delta\theta - b(t)\cos\Delta\theta \end{aligned} \tag{2.32}$$

where $\Delta\theta$ is the carrier-phase tracking error, arbitrary but not fixed.

For a two-dimensional QPSK signal, or during BPSK acquisition, the full timing-detector algorithm is:

$$u_t(t) = x_1(t-T/2)x_1(t) - x_1(t-T) + x_2(t-T/2)x_2(t) - x_2(t-T) \tag{2.33}$$

This is equation (2.29) in the continuous-time domain, applied to both channels of the baseband signal with the two components summed.

Substituting (2.32) in (2.33) and performing the trigonometry results in:

$$u_t(t) = a(t-T/2)a(t) - a(t-T) + b(t-T/2)b(t) - b(t-T) \tag{2.34}$$

which is independent of $\Delta\theta$.

All terms with $\Delta\theta$ cancels or combines according to $\sin^2\Delta\theta + \cos^2\Delta\theta = 1$.

The complete algorithm delivers the same error indication irrespective of carrier phase. The timing loop can lock prior to locking or even closing of the phase loop.

2.3.4 Digital implementation of algorithm.

The carrier recovery detector algorithm assumes that the I- and Q-channel samples are taken at instances when the symbols are valid.[8] The clock recovery must therefore acquire lock before the carrier loop.

The algorithm used uses two samples per symbol to derive the error voltage to control the loop. The A-to-D converters therefore have to operate at the data rate or twice the symbol rate. The algorithm produces one timing-error point from three different samples.

The equations for the digital version of the algorithm is given in equation (2.35) for BPSK and (2.36) for QPSK demodulation.

$$e(t) = sgn(I(t) - I(t-T))I(t-T/2) \tag{2.35}$$

$$\begin{aligned} e(t) &= sgn(I(t) - I(t-T))I(t-T/2)\ldots \\ &\quad + sgn(Q(t) - Q(t-T))Q(t-T/2) \end{aligned} \tag{2.36}$$

Physical explanation

The detector samples the data stream midway between strobe locations (i.e. at symbol borders) in each channel. If there is a transition between two symbols, the average midway value is zero when there is no timing error. A timing error results in a nonzero sample whose magnitude depends on the amount of error. Either slope is equally likely at the midway point so no direction information is in the sample value alone.

No timing information is obtained in the absence of a transition. The algorithm examines the two strobe values on either side of the symbol boundary, if no transition is present the difference of strobe values will be zero and the midway sample is rejected. When a transition is present, the difference between strobe values provides slope information. The product of the slope information and the midway sample provides the timing error.

The signs of strobe values could be used instead of actual values. If all data filtering is performed prior to the strobe point, the sign of the strobe value is the optimum hard decision instant of the symbol. This method improves tracking but acquisition performance may deteriorate. The use of strobe signs instead of actual values eliminates the need for algorithm multiplications, an advantage for digital implementation.

If the excess bandwidth is less than 100% the zero crossings of data transitions do not lie midway between strobe points. The crossing points become scattered around the midway point. The average location is still correct but individual trajectories depart from the average leading to self noise of the algorithm.

Detector characteristics

If a BPSK signal with modulation in one channel is received, the other channel terms provide no information once carrier phase lock is achieved and only adds noise. The full

[8]The digital implementation of the algorithm on the Philips chipset is described in the paper by Van der Wal and Montreuil [4].

algorithm is used during acquisition but is reduced to the terms of one channel after carrier lock is achieved. For QPSK demodulation both I- and Q-channel terms are used during the acquisition as well as tracking stage.

The noise performance of the algorithm deteriorates with decreasing bandwidth, the efficiency of clock regeneration falls off and self noise increases. This feature is inherent to regenerators with quadratic nonlinearities. A harder nonlinearity is needed for narrow bandwidth systems.

Application to OQPSK signals

The clock recovery algorithm used is not intended for OQPSK demodulation. Demodulation of OQPSK modulated signals is possible with increased error rates but clock recovery jitter is present due to the data timing offset. OQPSK systems using the same chipset have been developed by other designers using a time delay in one of the analogue channels to correct the timing offset.

Chapter 3

QPSK demodulator chipset

The TDA8040 is a QPSK demodulator and the TDA8041 is the corresponding demodulator controller. This chipset is capable of quadrature demodulation up to a 150 MHz carrier frequency and up to a symbol rate of 30 Msymbol/s. The necessary control signals needed to close the carrier, clock and gain loops are generated by the TDA8041 demodulator controller. The digital I and Q signals are output together with a derived symbol clock for further processing by a suitable logic device (See Chapter 5).

The chipset has been designed for the demodulation of digital broadcast satellite television signals. This type of signal requires a demodulator which can simultaneously handle low signal-to-noise ratios (SNR $\geq$ 3 dB) and large symbol rates (R $\leq$ 30 Msymbol/s). QPSK is the most common modulation technique used in satellite links with BPSK used in cases of poor reception conditions.

In this chapter the basic functions of the quadrature demodulator and the demodulator controller is decribed.[1]

3.1 Demodulator concept

A blockdiagram of the demodulation process as implemented using the Philips chipset is shown in Figure 3.1.

The demodulator system consists of a quadrature demodulator and two PLLs for carrier recovery and clock recovery. An AGC loop is provided to adjust the input level for variations in the received signal level. The quadrature demodulator is implemented in the TDA8040 and the carrier, clock and AGC detectors are implemented in the TDA8041.

The input to the demodulator is a QPSK modulated signal downconverted to the IF frequency of the demodulator. A SAW filter could be used in the IF path to avoid interference from adjacent channels or to achieve the half Nyquist shaping of the digital symbols.

After IF filtering the QPSK signal is applied to the TDA8040 input. The TDA8040 is simply a quadrature demodulator using two double balanced mixers driven 90° out of phase. The outputs of these two mixers result in the I and Q baseband signals. Provision is made for external lowpass filters to suppress the mixing products of the

[1]The demodulator chipset description is based on the Philips application note [1].

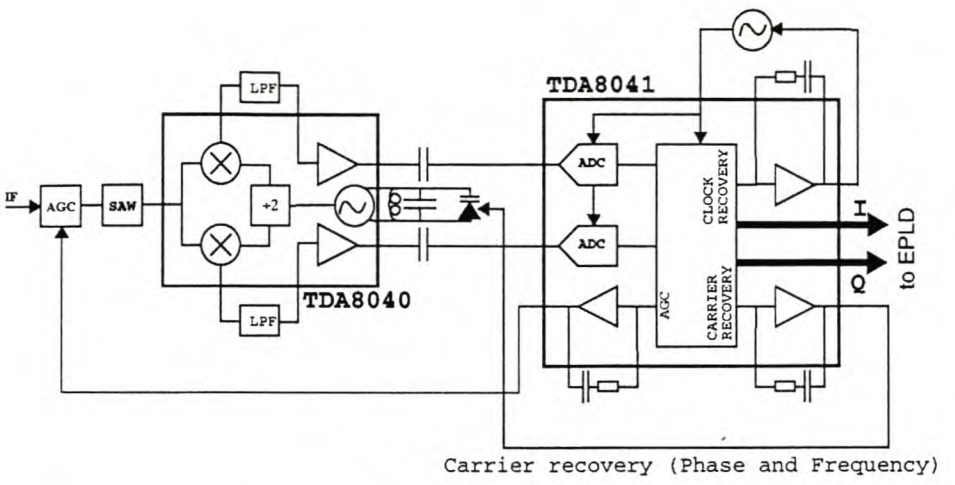


Figure 3.1: Blockdiagram of Philips chipset demodulater implementation [1].

demodulator. After filtering, the I and Q signals are amplified to the necessary levels for A-to-D conversion.

Analog to digital conversion is performed by the TDA8041. The digitized I and Q signals are used to generate the control information for the clock recovery, carrier recovery and AGC loops. For the PLL structure an active loop filter is used to reduce the static phase offset. This is achieved by converting the digital control information to a current, which is then filtered by an active filter consisting of an integrated opamp and an external time constant. The TDA8041 also provides three (3) bit I and Q signals to the outside world for the implementation of a soft decision Viterbi decoder.

An external logic device such as a FPGA or other EPLD is needed to convert the parallel I and Q datastreams to a serial bitstream with clock. The logic decoding and data unscrambling are also performed in the logic device.

3.2 The TDA8040 quadrature demodulator

The TDA8040 is processed using a high frequency bipolar process (Subilo-N30, f_T=6 GHz). The main block diagram of the TDA8040 can be seen in Figure 3.2.

IF amplifier

The IF amplifier is needed to obtain the necessary drive level for the quadrature demodulator. The input of the amplifier is capable of symmetrical and asymmetrical drive in both cases presenting a 50 Ω input impedance. Symmetrical drive by a SAW filter is preferred to reduce coupling of interference.

The input level of the IF amplifier should be 67 dBμV, due to spreads in the manufacturing process and external component variations this level can vary, therefore the amplifier

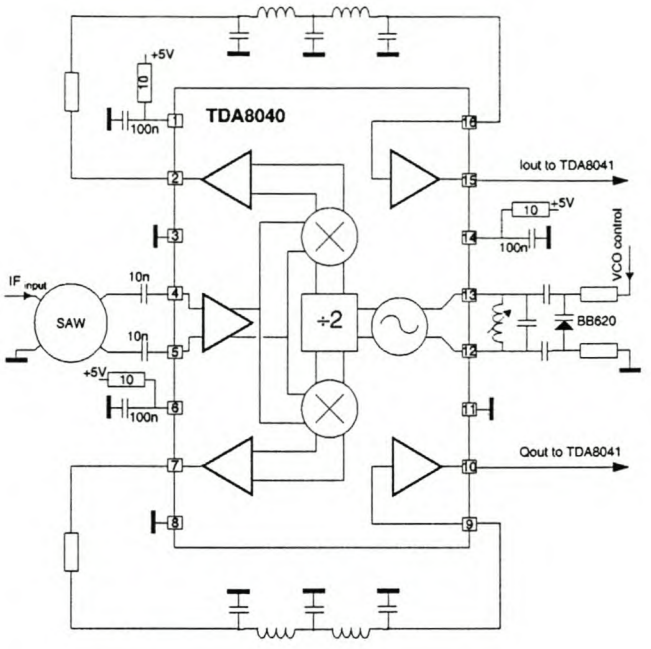


Figure 3.2: TDA8040 and its application [1].

can handle a 64 dBμV to 70 dBμV range. This translates to an input power range of -43 dBm to -37 dBm.[2]

The input IF frequency over which demodulation can be performed ranges from 10.7 MHz to 150 MHz.

Quadrature demodulator and output buffer

The quadrature demodulator is realized using two double balanced mixers. Double balanced mixing has the advantage of suppressing the LO and IF signals present at the mixer outputs. This suppression of the output spurious responses relaxes the design of the lowpass filters.

The mixer amplitude and phase characteristics and that of the filter in each demodulated arm is important, therefore a buffer output stage follows each of the mixers. The output resistance of the buffer stage is 50 Ω and the output voltage level is approximately 100 mV_{pp}.

Frequency divider

The quadrature demodulator requires two accurate sine waves with equal frequency and 90° phase difference. The phase shift is generated by a divide-by-two frequency divider.

[2]For 50 Ω systems dBμV values can be converted to dBm by simply subtracting 107 dB.

To maintain crosstalk at a level of -40 dB the local oscillator reference phases must be accurate to within 0.5°. The phase must remain within this limit with modulation present.

The accuracy of the divider phase shift is guaranteed to be better than 3°. For a 70 MHz IF input signal the accuracy is specified better than 0.5° over the complete I and Q baseband signal range.

Local oscillator

The divider is driven by a local oscillator operating at twice the input IF frequency. The oscillator frequency is selected by an external LC tuned circuit. For reduced supply variation influence the oscillator utilizes an internal reference supply.

External lowpass filters

The remaining spurious present at the quadrature demodulator outputs is suppressed by external lowpass filters. The baseband signals should be passed without additional tilt or group delay. Good matching between the two filters is therefore necessary.

The 10 kΩ input resistance of the baseband amplifiers present a minimal load to the filters and therefore the voltage loss in the filters is small. The arm filters should provide a DC path from input to output to bias the baseband amplifiers.

The filters should satisfy the following criteria:

Passband ripple The overall acceptable tilt in the total receiver is 2 dB. Assuming 1.5 dB tilt in the downconversion and another ±0.25 dB in the TDA8040 allows for ±0.25 dB tilt in the passband.

Passband frequency The end of the passband should be at the maximum signal frequency. The minimum passband frequency for raised cosine filtering can be calculated using:

$$f_{cutoff} = 0.5(1+\beta)f_{symbol} \tag{3.1}$$

where β is the roll-off factor.

Stopband frequency The stopband should start at the lower end of the unwanted spectrum. The unwanted spectrum width is determined by the modulation data rate and centered around half the LO frequency. The baseband filter should ensure that the spectrum around the LO/2 frequency is suppressed completely.

Stopband attenuation The attenuated signals in the stopband should be smaller than $\frac{1}{2}$LSB implying at least 30 dB of attenuation. A margin of 5 dB can be added.

Phase delay The I and Q signals are baseband signals and therefore the phase delay of these filters determines the phase distortion. Phase distortion is defined as: $PD = -\phi(f)/(2\pi f)$. The phase distortion should be as constant as possible.

Filter matching The I and Q filters should match in the passband. For the TDA8040 a maximum mismatch between the two branches of 1 dB is specified. The TDA8040 has matching of 0.4 dB (0.5%) between channels allowing a further mismatch of only 0.6 dB.

Filter order To limit the number of external components the suggested filter order is limited to three.

Baseband amplifiers

After external lowpass filtering, the baseband signals are amplified to a sufficient level for quantization by the A-to-D converters of the TDA8041 demodulator controller. The typical output level of the baseband amplifiers is 500 mV_{pp} and the output resistance is 50 Ω.

Power supply

Three different supply pairs of V_{dd} and ground are used to avoid common mode problems. The following demodulator subparts each have a separate supply:

- Small signal IF part, IF amplifier and quadrature demodulator.
- Small signal baseband part, baseband amplifiers.
- Large signal part, oscillator and divider stage.

The currents flowing into the supply pins at a nominal supply voltage of 5 V is given in Table 3.1. Variations due to process spreads and temperature variations are possible. It is advised to couple the device through a series resistor and with a shunt capacitor (see Figure 3.2 pin 1, 6 and 14). This decoupling should be done as close as possible to the device packaging.

Table 3.1: Supply currents of the TDA8040.

Pin	Description	Current [mA]
1	Baseband amplifiers	30
6	Quadrature demodulator	27
14	VCO	20

3.3 The TDA8041 quadrature demodulator controller

The TDA8041 is a mixed analog and digital design on a CMOS 1 μm process. The chip consumes 30 mA at 5 V and is mounted in a QFP44 package. The main block diagram of the TDA8041 can be seen in Figure 3.3.

The TDA8041 converts the analog I and Q arm signals to internal four-bit digital values suitable for processing by the digital control loops. The clock recovery, carrier recovery, AGC, lock detect and the digital outputs are derived from these four-bit values. The time constants for each of the PLL control loops can be fixed externally. The algorithms used in the control loops are dependent on the modulation method used and therefore a QPSK/BPSK mode select pin is reserved. The digital I and Q arm signals are output in three bit resolution for the implementation of a soft decision Viterbi decoder.

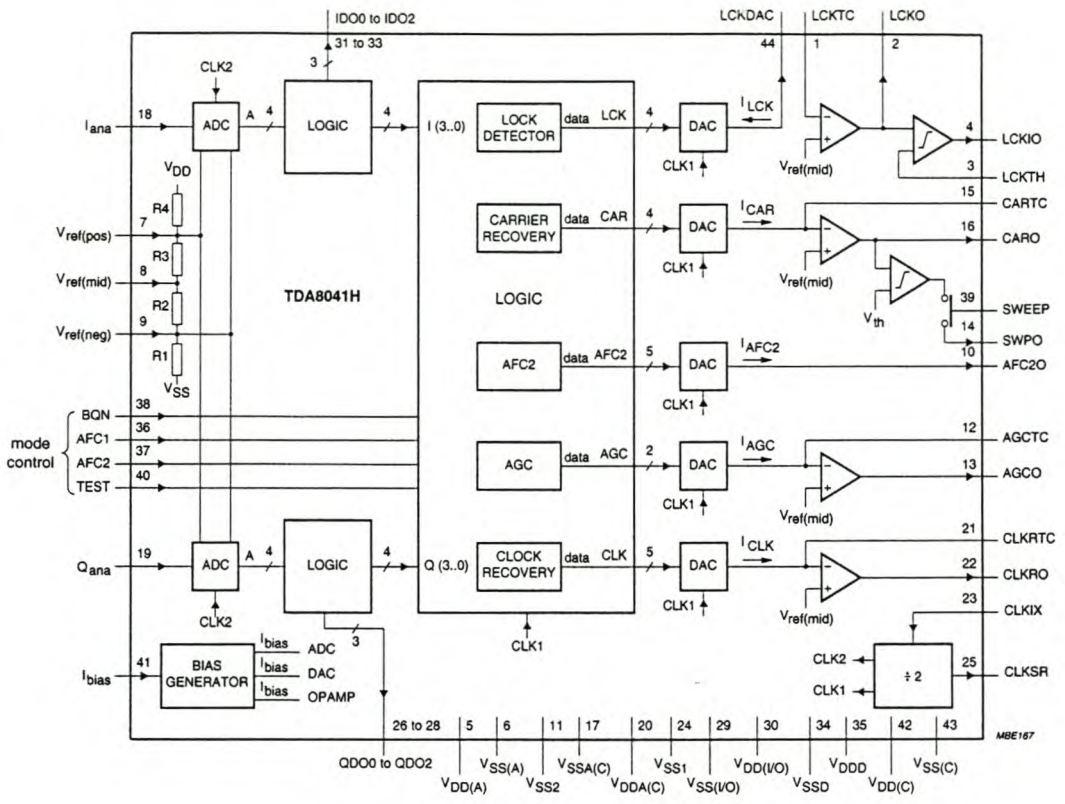


Figure 3.3: TDA8041 and its application [1].

Analog to digital converters

The sampling process of the A-D converters should not distort the amplitude and phase characteristics of the baseband I and Q signals. The TDA8041 demodulator controller guarantees distortionless sampling for symbol rates of up to 30 Msymbol/s. Simultaneous sampling is also needed and therefore the two A-to-D converters should have good matching.

The valid values of the input analog signals are defined to be within the range set between $Vref_n$ and $Vref_p$. Internal resistors determine the nominal reference voltages at:

- $Vref_p = 2.4$ V
- $Vref_m = 1.9$ V
- $Vref_n = 1.4$ V

The DC levels of the TDA8040 outputs and the TDA8041 inputs are different and therefore series capacitors are needed between the two devices. The removal of the DC presents no problem as no information is conveyed in the DC component. The series capacitors should however present low impedance paths between the ICs to avoid suppression of low frequency components in the QPSK signal.

An external capacitor should be connected to the $Vref_p$, $Vref_m$ and $Vref_n$ pins to avoid coupling from the supply to the analog inputs.

Bias generator

A bias generator is needed to supply the integrated DACs and operational amplifiers. A 100 kΩ resistor is typically used resulting in DAC output current range from -100 μA to +100 μA. If required the bias resistor value can be varied between 50 kΩ and 200 kΩ without degradation in operational amplifier performance.

Clock recovery

The clock recovery detector derives a control signal (from the quantized signals) that is used to drive the clock recovery PLL. If the A-to-D converter samples where the eye pattern is maximally open (the main symbol) and between two of these main symbols the VCXO is phase locked to the incoming bit clock. Since the carrier recovery loop uses the sampled I and Q values the clock recovery loop should achieve lock first. A detailed description of the clock recovery algorithm used is given in Section 2.3.

The mid symbols are used to derive the digital control information for the clock recovery detector. This information is converted to an analog current by the DA converters. A current of 42 μA/rad is produced around the zero crossing.

The DAC output is filtered with an active filter realized with an integrated operational amplifier and an external time constant. The detector and filter combination requires a VCXO with a positive slope.

The clock recovery algorithm uses the data strobe values as well as the mid symbol values, therefore the A-to-D converters sample at double the symbol rate. This implies that the VCXO must operate at double the symbol rate.

The TDA8041 amplifies the low level VCXO signal to an internal digital level by means of four inverters. Three of the four inverters are fed back to bias the input. To avoid parasitic oscillation due to this inverter chain the VCXO impedance should be low ohmic ($\approx$ 50 Ω).

Carrier recovery

The carrier recovery utilizes a PLL to lock to the incoming carrier phase. The detector output is converted to a current that is fed to the PLL loop filter. Again a positive slope VCO is required for use with the detector and loop filter combination.

Generally the loop bandwidth of a PLL is a few kilohertz. If the input signal of the carrier recovery PLL has a frequency offset which is outside this loop filter bandwidth, acquisition of the loop could be slow.

To speed up the carrier recovery process three different recovery functions are included:

- AFC1 - AFC1 is a robust detector which forces the offset frequency in the quadrature demodulator to zero. This detector is able to track offsets of up to 1/8 of the symbol rate.
- AFC2 - AFC2 is used to track frequency offsets larger than 1/8 the symbol frequency. This detector is not sensitive enough to detect frequency offsets close to zero. Control signals are generated independent of clock recovery lock.

No internal amplifier is integrated for the AFC2 detector output. The average value of this detector represents the frequency error, therefore an additional lowpass filter is needed. The signal can then be added to the carrier recovery control voltage. When the frequency offset is below 1/8 the symbol frequency this control signal should be switched off.

- VCO sweep function - The sweep function generates a triangle voltage at an integrator output to tune the VCO over its entire frequency range. The sweeping period is selected by one external resistor.

Automatic gain control (AGC)

The TDA8041 has an integrated AGC detector which detects the incoming I and Q signal levels at the symbol instants and compares it to an internal reference. The peak-to-peak reference is defined as $(Vref_p - Vref_n)/2$ ($\approx$ 0.5 V). Active AGC loop filtering can be done by means of an integrated opamp with external loop filter components. The AGC control loop expects a positive gain amplifier.

Lock detection

The lock detector implemented in the TDA8041 gives a unique relation between the lock detect output voltage and the received signal Eb/No. From the lock detector output, LCK_{dac}, the average value should be obtained with a low pass filter to estimate the LCK_0 voltage.

This LCK_0 signal is the low pass filtered output of the carrier lock detect DAC output, LCK_{DAC}. An integrated opamp is provided between the lock time constant pin LCK_T and the LCK_0 pin for the low pass filter. The low pass filter is also required to suppress spurious signals generated by the DAC sampling process.

The TDA8041 provides an integrated comparator with an adjustable threshold. The comparator has a digital level carrier lock indicator output LCK_I to indicate to a microprocessor the received signal status. The lock detect voltage LCK_0 is compared to the lock threshold voltage LCK_{THR} by the internal comparator and a logic high is output at LCK_I when the threshold is exceeded.

The advantages of signal Eb/No estimation and lock detect indication is the following:

- Viterbi decoders are only able to synchronize from a certain BER onwards, the LCK_I could be used to indicate to a microprocessor when the desired BER is reached.
- It is possible to provide the Eb/No or S/N for the adjustment of the satellite antenna or evaluation of the link performance.

Digital outputs

The derived symbol clock is output and used for synchronization in the digital logic. Both the I and Q information is output in a three (3) bits wide format. Only the MSB bits of each channel can be used for a hard decision decoder. All bits are available for soft decision algorithms such as used in soft decision forward error correction schemes.

Chapter 4

The demodulator analog circuitry implementation

This chapter discusses the design and implementation of the analogue demodulator circuitry. This includes all the control loops and filtering required by the Philips demodulator chipset.

The demodulator system consists of two phase-locked loops: the clock recovery and the carrier recovery. Since the carrier recovery requires information at valid symbol instants, the clock recovery loop has to acquire lock before the carrier loop can lock.

In this section the individual loop components of both loops are discussed. The selection of these components determine the loop filter time constants.

4.1 Phase-locked loop overview

Phase locked loops (see Figure 4.1) are used for carrier and clock recovery in many applications. The phase-locked loop is a negative feedback system that consists of three main components: a multiplier, a loop filter and a voltage-controlled oscillator (VCO).

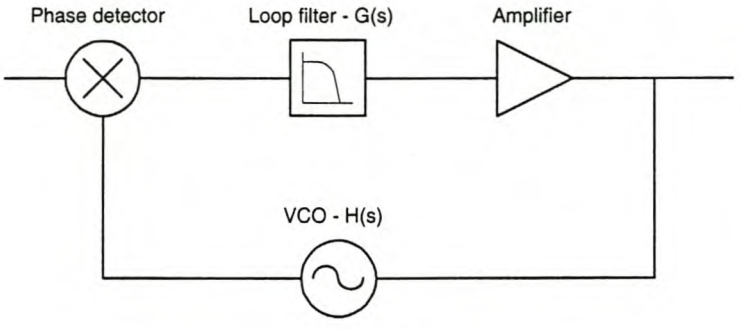


Figure 4.1: Basic PLL blockdiagram.

The multiplier or phase detector compares the phase of the incoming signal to the local VCO frequency and outputs an error signal proportional to the sine of the phase difference. The loop filter averages the multiplier output and limits the slew rate and

bandwidth of the control signal to the VCO. The control voltage corrects the VCO frequency difference to decrease the frequency difference between the two signals. This process continues until the two frequencies are equal and only a constant phase difference exist between the two signals.

PLL characteristics

The basic loop transfer equation for a PLL with loop filter response $G(s)$, VCO response of $H(s) = K_o/s$ and phase detector gain K_d is:

$$F(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{K_o K_d G(s)}{s + K_o K_d G(s)} \tag{4.1}$$

The type and order of the loop filter $G(s)$ determines the amount of control the designer has over the characteristics of the PLL. The most common usage of the terms are identified and used here:

- The *type* of a system refers to the number of poles of the loop transfer functions: $G(s)H(s)$, located at the origin. That is the number of perfect integrators within the loop. Any PLL is at least a type I loop because of the perfect integrator in the VCO.
- The *order* of a system refers to the highest degree of the polynomial expression: $1 + G(s)H(s) = 0$, defined as the characteristic equation. The roots of the characteristic equation become the closed loop poles of the overall transfer function.

A second order loop is usually sufficient in most clock and carrier recovery PLL applications. Loop orders higher than three are seldom required. High order loops are conditionally stable and also tend to be sensitive to changes of gain and circuit components.

Lag-lead type filter or proportional-plus-integral control is popular because it has two independent time constants. The natural frequency and damping can thus be chosen independently. The DC gain can further be made large to ensure good tracking.

A second order active loop filter is used in both the clock and carrier recovery loops of the Philips chipset. An integrated opamp is provided and only a passive feedback network is needed to realize the filter (see Section 4.2.1).

Loop bandwidth

The 3 dB bandwidth of the transfer function $F(s)$ is related to the natural frequency ω_n and damping factor β of the PLL. The loop bandwidth for a type 2 second order system can be found by setting $|F(j\omega)|^2 = 0.5$ and solving for ω_{3dB}:

$$\omega_{3dB} = \omega_n \left(1 + 2\beta^2 + \sqrt{2 + 4\beta^2 + 4\beta^4}\right)^{\frac{1}{2}} \tag{4.2}$$

A low carrier recovery loop bandwidth is undesirable due to the carrier frequency uncertainty. To phaselock in a period of the order of the reciprocal of the loop bandwidth, it is necessary that the initial frequency offset must be the same order as the loop bandwidth [9].

Noise performance

A main advantage of phaselock loops is their ability to operate with large amounts of noise. The noise bandwidth of the loop is defined in [10] and given below:

$$B_L = \int_0^\infty |F(j2\pi f)|^2 \, df \ [Hz] \tag{4.3}$$

The phase variance of the loop under white input noise can then be calculated using the noise bandwidth B_L:

$$\theta_{no}^2 = \frac{2N_o B_L}{V_s^2} = \frac{W_i B_L}{P_s} \tag{4.4}$$

where P_s is the signal power in watts and W_i is the noise power spectral density in W/Hz.

For an active lag-lead type loop filter the noise bandwidth can be calculated using equation (4.3) and is given as [10]:

$$B_L = \frac{1}{2}\omega_n \left(\beta + \frac{1}{4\beta}\right) \ [Hz] \tag{4.5}$$

Minimum noise bandwidth of the second-order loop is achieved with a damping factor of $\beta = 0.5$ but does not change more than 25% for damping between 0.25 and 1.

Loop tracking characterisitics

Steady-state errors
For small phase errors the phaselock loop is assumed linear and the transfer function for a phase error that results from a specified input is:

$$\frac{\theta_e(s)}{\theta_i(s)} = \frac{s}{s + K_o K_d G(s)} \tag{4.6}$$

Using this transfer function together with the final value theorem the steady state error for a specific phase input can be predicted.

A step change of input phase $\Delta\theta$ will eventually be tracked out until there is no steady-state error.

A step change of input frequency $\Delta\omega$ or in other words a ramp change of input phase results in a velocity error (also called loop stress or static phase error):

$$\theta_v = \frac{\Delta\omega}{K_v} \tag{4.7}$$

where $K_v = K_o K_d F(0)$ is known as the velocity constant or DC loop gain.

A linear change of input frequency at a rate of $\Delta\dot{\omega}\ rad/s^2$ might be caused by Doppler shift or sweep-frequency modulation. The acceleration error (also called dynamic tracking error or dynamic lag) that results is given by:

$$\theta_a = \frac{\Delta\dot{\omega}}{\omega_n^2} \tag{4.8}$$

In a second order loop a large natural frequency, and therefore a large noise bandwidth as well, is necessary to handle a rapid varying input frequency. The steady-state acceleration error can be eliminated by using a third-order loop with the additional advantage of a small noise bandwidth.

Non-linear tracking
The assumption of linearity is less useful as the phase error increases and is meaningless if the loop is out of lock. For a sinusoidal phase detector characteristic the static phase error equation (4.7) is rewritten as:

$$\sin(\theta_v) = \frac{\Delta\omega}{K_v} \tag{4.9}$$

If $\Delta\omega > K_v$ the loop is out of lock and the phase detector voltage becomes a beat note. The hold-in range of the loop is can be made large by using a high loop gain, thus:

$$\Delta\omega_H = \pm K_v \tag{4.10}$$

For a sinusoidal phase detector characteristic the dynamic error is also rewritten:

$$\sin(\theta_a) = \frac{\Delta\dot{\omega}}{\omega_n^2} \tag{4.11}$$

This implies that the maximum allowable rate of input frequency change is:

$$\Delta\dot{\omega} = \omega_n^2 \tag{4.12}$$

If the rate of input frequency change exceeds this value the loop will lose lock.

Acquisition

Acquisition is the process by which a loop locks to the PLL input signal frequency. PLLs are tracking devices and are slow and unreliable at self acquisition. Acquisition is inherently a non-linear process as the loop starts out in the unlocked state.

Phase acquisition
Phase acquisition is normally self acquired without the aid of additional circuitry. If the initial phase error is close to an unstable null in the PD characteristic the phase can dwell near the null for an arbitrary period. This is known as the hangup effect and is a problem in applications where rapid acquisition is essential.

The frequency range over which the loop acquires phase without cycle slips is called the lock-in range ($\Delta\omega_L$) of the PLL. The lock-in limit of a first order loop is equal to the loop gain ($\Delta\omega_L \approx \pm K$). The higher order loop has the same lock-in range as the equivalent-gain first order loop.

Frequency acquisition
Frequency acquisition is more difficult and demands more attention than phase acquisition. A number of frequency acquisition techniques exist to aid pull-in such as: frequency sweeping, frequency discriminators and bandwidth widening methods.

Pull-in time T_p is defined as the time required for the average frequency error to change from the initial condition to the lock limit. Pull-in is slow and disturbed by noise,

modulation and phase detector offsets. If the frequency offset $\Delta\omega$ is greater than the loop bandwidth a second order loop will pull-in slowly and skip several cycles. Pull-in is limited to frequency offsets of approximately ten times the loop bandwidth.

If the frequency offset exceeds loop bandwidth it is necessary to sweep the VCO through the band containing the carrier. This method is effective if no modulation is present but dangerous if other frequency components are present, since the loop will false lock to sidebands if the bandwidth is too narrow. A small bandwidth loop has the problem that the maximum frequency sweep rate is normally less than a quarter of the square of the loop bandwidth ($T_{sweep} \pm \frac{1}{4f^2}$) [10].

4.2 Recovery and control loops

4.2.1 Loop filter characteristics

The loop filter used in both the carrier and clock recovery loops makes use of an integrated opamp in the TDA8041 with an external RC feedback network as shown in Figure 4.2.

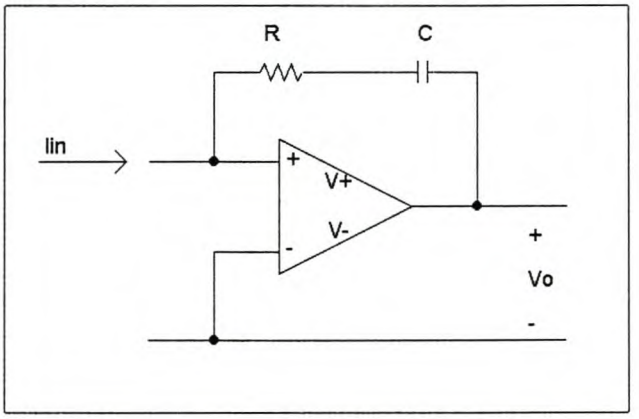


Figure 4.2: PLL loop filter.

The current into the opamp input must equal the current flowing through the feedback loop, thus:

$$I_{in}(s) = \frac{V_o(s)}{R + \frac{1}{sC}} \tag{4.13}$$

The input current to voltage output transfer function can be written as:

$$G(s) = \frac{V_o(s)}{I_{in}(s)} = \frac{sRC + 1}{sC} \tag{4.14}$$

The characteristic equation (C.E.) of the closed loop transfer function can now be written:

$$\begin{aligned} C.E. &= 1 + G(s)H(s) \\ 0 &= 1 + G(s)H(s) \\ &= 1 + \left(\frac{sRC + 1}{sC}\right)\left(\frac{K}{s}\right) \\ &= s^2 + sRK + K/C \end{aligned} \tag{4.15}$$

$G(s)$ is the forward transfer function of the loop filter and $H(s)$ is the transfer function of the VCO. The gain K is the combined gain of the phase detector, loop filter and VCO. The $1/s$ term is contributed by the VCO due to its integrating operation on the loop phase error.

Relating equation (4.15) to the standard second order polynomial expression (4.16), the value of the natural frequency and damping factor can be expressed in terms of filter components.

$$s^2 + 2\beta\omega_n s + \omega_n^2 \tag{4.16}$$

The value for the natural frequency (ω_n) is:

$$\omega_n = \sqrt{\frac{K}{C}} \tag{4.17}$$

The value damping factor (β) is:

$$\begin{aligned} \beta &= \frac{RC}{2}\omega_n \\ &= \frac{RC}{2}\sqrt{\frac{K}{C}} \end{aligned} \tag{4.18}$$

The complete transfer function of the recovery loop will be of the form:

$$F(s) = \frac{2\beta\omega_n s + \omega_n^2}{s^2 + 2\beta\omega_n s + \omega_n^2} \tag{4.19}$$

4.2.2 Clock recovery

VCXO constant

Figure 4.3 shows a blockdiagram of the clock recovery circuitry of the TDA8041.

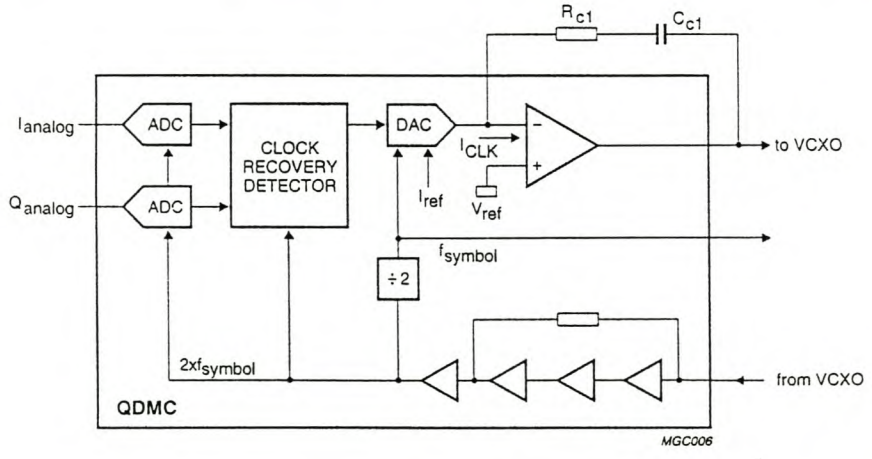


Figure 4.3: Clock recovery functional blockdiagram [4].

Table 4.1: Crystal frequency uncertainty due to physical factors.

Crystal frequency uncertainty	$\frac{\Delta f_{osc}}{f_{osc}}[ppm]$
Manufacturing spreads	± 15 p.p.m.
Temperature	± 30 p.p.m.
Aging	± 5 p.p.m.
Total uncertainty	± 50 p.p.m.

The crystal oscillator should be able to compensate for the symbol frequency uncertainty between the transmitter and receiver. The frequency uncertainty of a crystal oscillator is defined as $\Delta f_{osc}/f_{osc}$ in p.p.m. (parts per million), where f_{osc} is the nominal crystal frequency and Δf_{osc} is the maximum frequency deviation from this nominal frequency. The possible physical factors influencing the frequency stability of a crystal oscillator are set out in Table 4.1.

If both the transmitter and receiver makes use of a crystal controlled symbol clock, the maximum symbol frequency uncertainty can be approximated to be ±100 p.p.m. The VCXO must therefore be able to adjust the receiver symbol clock over the total uncertainty range.

If the VCXO is driven directly from the TDA8041, the VCXO tuning voltage is 3.8 V minimum. The VCXO constant can thus be calculated as:

$$K_o = \Delta f_{osc}/3.8\ [Hz/V] \tag{4.20}$$

The measured response of the implemented VCXO can be seen below in Figure 4.4. A VCXO constant of 2.1 kHz/V is used in the calculation of the loop parameters.

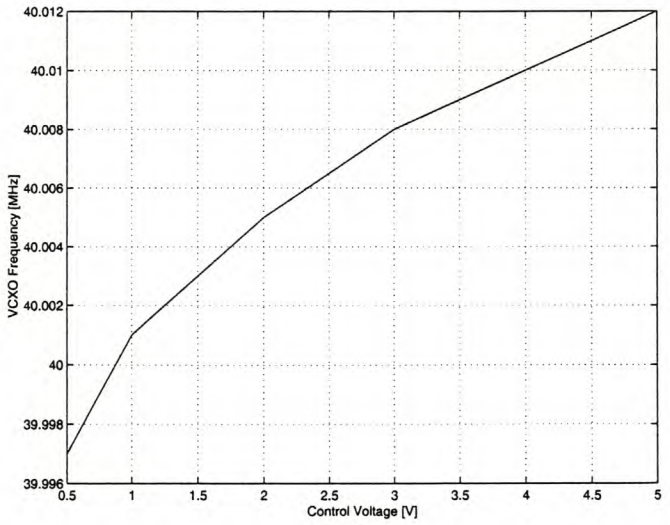


Figure 4.4: Measured clock frequency versus tuning voltage.

Clock recovery loop phase detector constant

The clock recovery loop phase detector constant is given as $K_d = 42\ \mu A/rad$ [1]. The S-curve of the loop is reproduced in Figure 4.5.

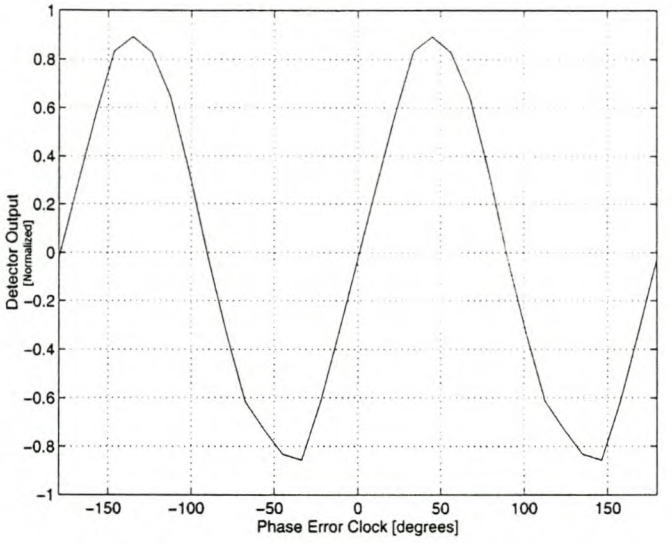


Figure 4.5: S-curve of clock recovery detector [1].

Clock recovery loop filter constants

No algorithm is used to lock to the local clock to the incoming clock frequency if the frequency error is larger than the loop bandwidth. The maximum frequency error Δf_{osc} should not exceed the loop bandwidth of the clock recovery, $2\beta f_n$. This leads to the following expression:

$$\Delta f_{osc} \leq 2\beta f_n \tag{4.21}$$

in which Δf_{osc} is the maximum frequency deviation of the clock oscillator.

Using this equations with equations (4.17) and (4.18) we can find the following:

$$\Delta\omega_{osc} \leq 2\beta\omega_n = KR \tag{4.22}$$

Since $\Delta\omega_{osc}$ and the open loop gain K ($K = K_o K_d$) is known, the minimum value of R can be calculated from this formula.

Choosing the damping factor β, the capacitor needed in the loop filter can be calculated. If $\beta \ll 0.7$ instabilities or peaking will result or if $\beta \gg 1$ the response will be slow. A realistic choice for β lies between 0.7 and 1.3.

An additional capacitor in parallel with the feedback resistor (R_{c1}) allows additional roll-off at high frequencies (see Figure 4.3). The effect of the additional capacitor on the loop behaviour may be ignored if the pole it introduces is more than ten times ω_n.

Table 4.2: Summary of calculated clock PLL parameters.

Datarate	Mbit/s	40
Damping ratio β		1.3
Natural frequency f_n	kHz	4.1
Resistor R_{c1}	kΩ	120
Capacitor C_{c1}	pF	820
Loop bandwidth f_{3dB}	kHz	12.2
Noise bandwidth B_L	kHz	19.2

Filter component values are calculated for a 40 Mbit/s datarate. The results are summarized in Table 4.2. The Matlab source code used to calculate the required filter component values is shown in Appendix C.1.

To verify that the actual circuit is functioning according to design a disturbing current of approximately 12 μA is injected in front of the clock recovery operational amplifier. The impulse response at the opamp output is measured and displayed in Figure 4.6. The measured settling time of 66.8 μs agrees well with the simulated value of 70 μs using the Matlab code in Appendix C.1.

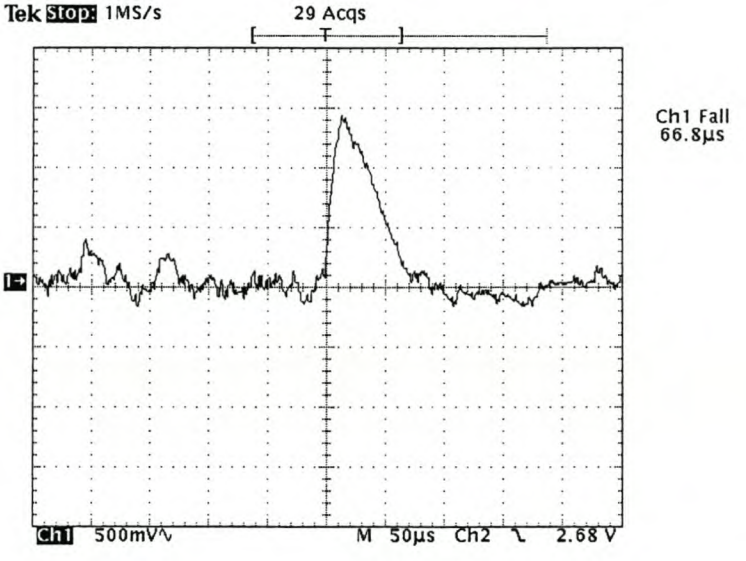


Figure 4.6: Measured impulse response of clock recovery loop.

4.2.3 Carrier recovery

The exciters used in the transmitting process as well as the local oscillators used in the receiving process may drift due to temperature variations. It is estimated that this and other causes results in a frequency uncertainty in the order of ±2.5 MHz maximum. Doppler frequency shift due to relative movement between transmitter and receiver also contributes to the carrier frequency uncertainty. The carrier recovery loop must be able

to track these static as well as dynamic frequency errors. Figure 4.7 shows the high level blockdiagram of the carrier recovery circuitry.

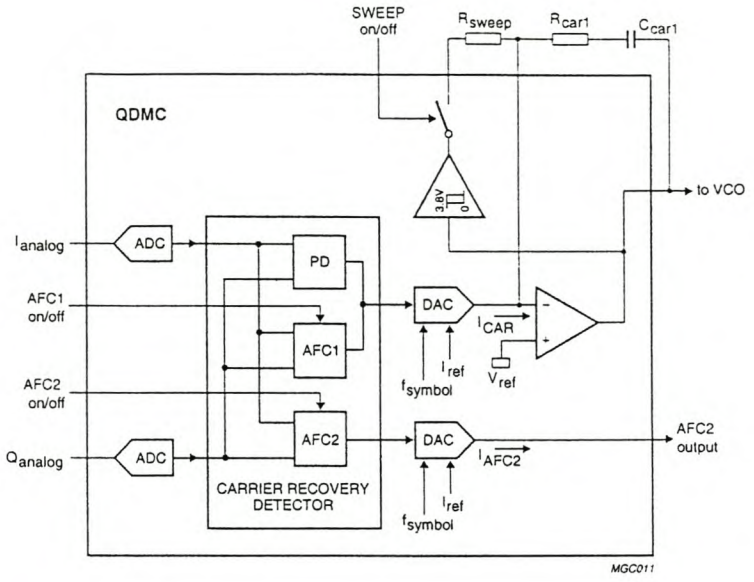


Figure 4.7: Carrier recovery functional blockdiagram [4].

VCO constant

The required VCO constant is determined using a maximum allowable frequency uncertainty of 5 MHz. The TDA8041 can supply a carrier recovery output swing of 3.8 V minimum. The minimum VCO constant can thus be found from:

$$K_o = \Delta f_c / 3.8 \; [Hz/V] \tag{4.23}$$

The measured response for the implemented VCO is shown in Figure 4.8.

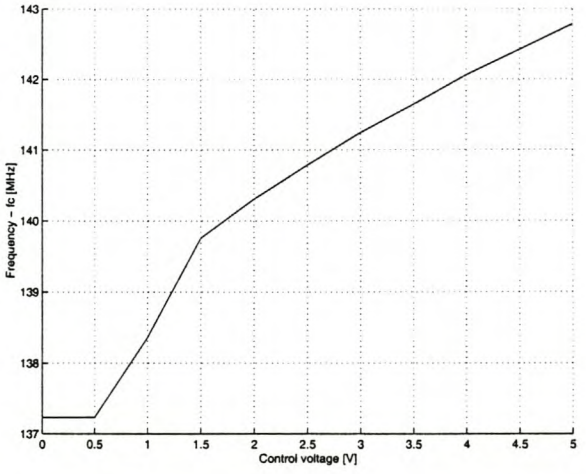


Figure 4.8: Carrier frequency versus tuning voltage.

A VCO constant of 658 kHz/V is used in the calculation of the loop parameters. The VCO constant varies significantly over the full control voltage range due to non-linearity in the VCO characteristic. This needs to be kept in mind when the loop filter components are calculated.

The carrier recovery phase detector constant

The expectation of the phase detector output for the idealized as well as implemented phase detector is given in [1] and reproduced in Figure 4.9.

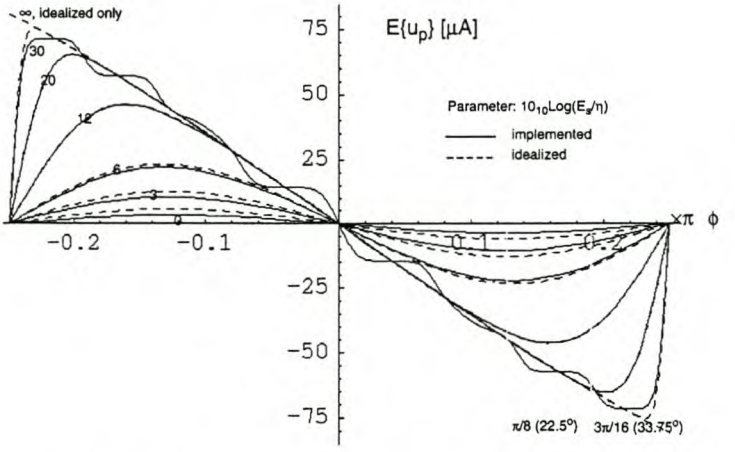


Figure 4.9: S-curve of phase detector in the presence of noise (idealized and implemented) [1].

It can be seen that the implemented curve approaches the idealized curve for Eb/No > 6 dB. Eb/No values over 20 dB results in the quantization of the S-curve reappearing. Eb/No values below 6 dB result in an implemented phase detector curve with a lower slope than the corresponding idealized curve. This is due to the quantizing effect of the AD converters.

If noise at the input of the quantizer is significant relative to the quantization intervals the quantization operation can be described as the addition of white quantization noise. The implemented phase detector will behave as the idealized phase detector with some extra noise added.

The noise is asymmetrically clipped, for positive signal values the clipped noise has an average negative value and for negative signal values the clipped noise has an average positive value. In both cases the signal amplitude decreases towards zero. Thus the slope of the S-curve decreases resulting in a decrease in K_d.

The dependency of K_d on Eb/No is shown for the implemented and idealized phase detector in Figure 4.10. This curve is a reasonable approximation provided Eb/No is in the range from 20 to 6 dB. Below 6 dB the implemented and idealized curves diverge due to limiting effects.

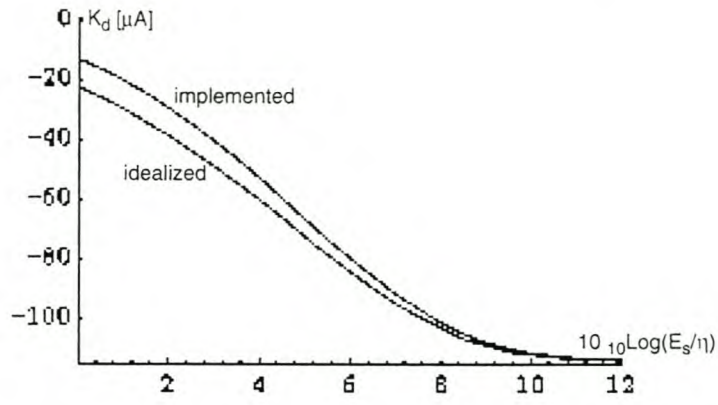


Figure 4.10: Phase detector K_d as a function of E_b/N_o (idealized and implemented) [1].

Calculation of loop filter R and C

The phase detector constant K_d is approximated for an expected Eb/No value. The loop gain is then calculated as the product of this phase detector constant, K_d, and the VCO gain constant, K_o, resulting in $K = K_d K_o$.

A suitable damping coefficient, β, in the order of one (0.7 to 1.3) and a natural frequency, ω_n, is chosen. The required resistor and capacitor value for the loop filter can then be calculated.

The choice of the natural frequency ω_n is influenced by several factors. Noise components due to the VCO are suppressed if its frequency components fall within the loop bandwidth. The acquisition time of the loop is also slow if the loop bandwidth is too small. A simple rule of thumb is to use a natural frequency 1/1000 times the symbol rate ($f_{symbol}/1000$) for a 20 Mbit/s symbol rate we choose a natural frequency of 20 kHz.

The results of the carrier PLL calculations are summarized in Table 4.3. The Matlab source code used to calculate the required filter component values for different carrier loop parameters is presented in Appendix C.2.

Table 4.3: Summary of calculated carrier PLL parameters.

Datarate	Mbit/s	40
Damping ratio β		1.0
Natural frequency f_n	kHz	21.8
Resistor R_{c1}	Ω	680
Capacitor C_{c1}	nF	22
Loop bandwidth f_{3dB}	kHz	55.0
Noise bandwidth B_L	kHz	87.0

The proper functioning of the physical circuit is again checked by injecting a disturbing current of approximately 20 μA in front of the carrier recovery operational amplifier. The impulse response at the opamp output is measured and displayed in Figure 4.11. The measured settling time of 16.6 μs compares well with the expected value of 15 μs calculated using the Matlab code in Appendix C.2.

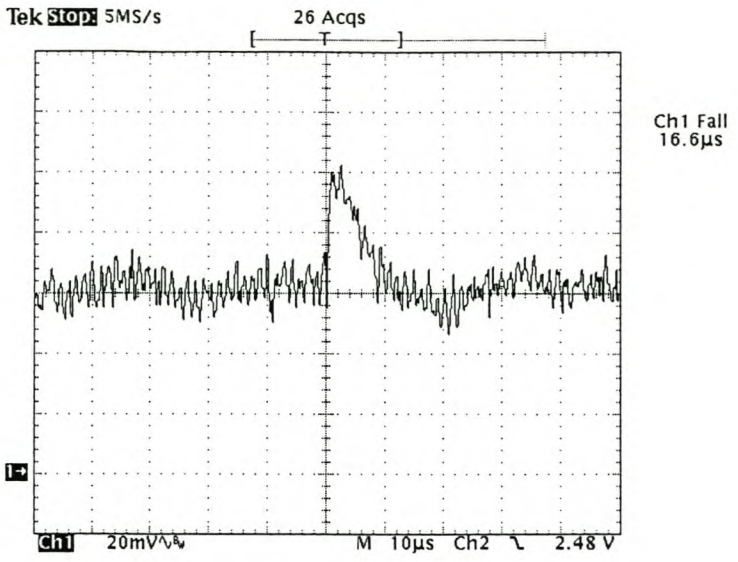


Figure 4.11: Measured impulse response of carrier recovery loop.

4.2.4 Automatic frequency control (AFC)

The TDA8041 has two separate automatic frequency control loops available, namely AFC1 and AFC2.

AFC1 is a combination of a frequency detector and phase detector with the option to switch off the frequency detector. The PD or PFD is selectable via the AFC1 pin. AFC1 is capable of regulating the frequency and phase accurately but has principal falselock points at $\frac{1}{8}$ the symbol rate ($\frac{1}{8} f_{symbol}$).

AFC2 is only a frequency detector but is capable of regulating over a wide frequency range without any principal false lock points. The operation of this frequency detector can be switched off with pin AFC2.

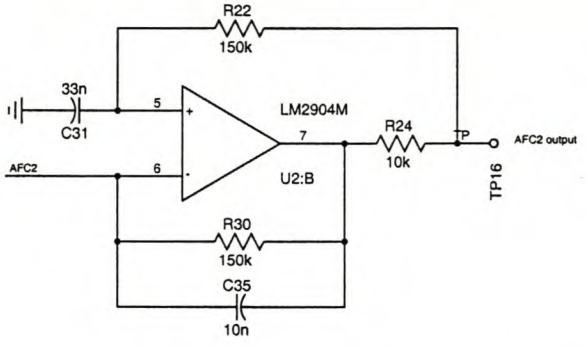


Figure 4.12: Default AFC2 control loop filter.

AFC2 is amplified with an external inverting opamp (see Figure 4.12 for the suggested circuit [1]) and added to AFC1. The reasoning behind this is that AFC2 should bring the VCO frequency within the falselock points of AFC1 and then be switched off. After

this AFC1 is able to lock the local VCO frequency to the incoming carrier frequency. The order in which the functions must be switched is given in Table 4.4.

Table 4.4: Automatic frequency control lock algorithm.

Order	Sweep	AFC2	AFC1	Phase detector
1	1	0	0	1*
2	0	1	0	1*
3	0	0	1	1
4	0	0	1/0	1

* *on but no effect*

Due to the fact that the VCO pulling range is only in the order of 5 MHz the AFC2 loop is not effective in the QPSK demodulator. The suggested AFC2 loop filter is however included in the circuit for testing purposes and future use.

4.2.5 VCO sweep function

A VCO sweep function is implemented to sweep the modulated spectrum within the bandwidth of the demodulator filters in order for the clock oscillator to lock [1]. A sweep current is added to the summing joint of the AFC1 opamp (see Figure 4.7). This function is switched on by asserting the digital SWEEP mode pin.

The sweep period is calculated as follows:

$$T_{swp} = 2R_{sweep}\, C_{car1} \tag{4.24}$$

The capacitor value is shared with the AFC1 control loop filter. The resistance (R_{sweep}) required for a desired sweep time can thus be calculated.

A sweep time of 36 ms is selected by using an 820 kΩ resistor for R_{sweep}. The measured sweep time of 32 ms corresponds well to the design value.

4.2.6 Automatic gain control (AGC)

The AGC response time is not critical and can be relatively low. The response time is set by a single capacitor across the internal AGC opamp. The AGC DAC output has three current levels to indicate the RF input level: $+100\ \mu A$ for high, $-100\ \mu A$ for low and $0\ \mu A$ for correct signal level.

Depending on the voltage span the AGC amplifier requires, the corresponding capacitance is calculated:

$$C = i\frac{\delta t}{\delta v} \tag{4.25}$$

where $i = 100\ \mu$A.

Thus for a 5 V AGC span with 5 ms response time the capacitance required is:

$$C = 100\ \mu A \frac{5\ ms}{5\ V} = 100\ nF$$

The AGC response time is verified by measuring the AGC output voltage when the input signal level of the demodulator is changed. The signal level is given a step change using an adjustable attenuator and the response time is measured to be approximately 5 ms.

IVA-05208 Variable gain amplifier

The Hewlett Packard IVA-05208 is a versatile surface mount variable gain amplifier. The device can be used in any combination of single-ended or differential inputs or outputs. The highest usable frequency is typically 1.2 GHz and the lowest frequency of operation is only limited by the values of blocking and bypass capacitors used. The amplifier features a typical gain control range of 30 dB with a gain response time of less than 10 ns.

The AGC circuit is built in a single-ended input and single-ended output configuration on a separate board with SMA connectors for the RF path. Provision is made for an attenuator pad for isolation and to set the AGC input signal level. The schematic diagram of the AGC amplifier can be seen in Figure 4.13.

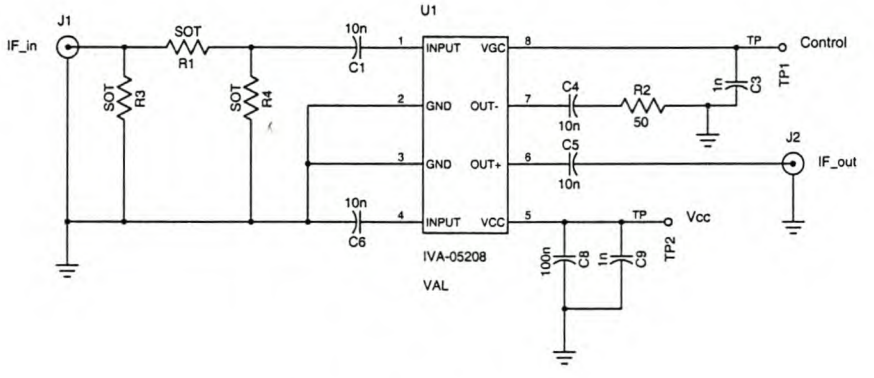


Figure 4.13: AGC schematic.

The measured amplifier gain versus control voltage is shown in Figure 4.14. It can be seen from the response that the amplifier requires a control voltage with a negative slope. An inverting opamp circuit is used to invert the AGC control voltage applied to the amplifier. A surface mount LM2904 opamp is used for this purpose as one is already used for the optional AFC2 control loop. The inverting opamp circuit is shown in Figure 4.15.

4.3 Oscillator circuitry

4.3.1 Clock VCXO design

The purpose of the crystal oscillator is to compensate for the symbol frequency uncertainty in the transmitter-receiver system. Crystal oscillators are the most common means to obtain an accurate single-frequency source.

High clock rates require the use of an overtone crystal. Overtone crystals have the disadvantage that the pulling range is much lower ($\pm$10 to 20 p.p.m.) as pulling range decrease

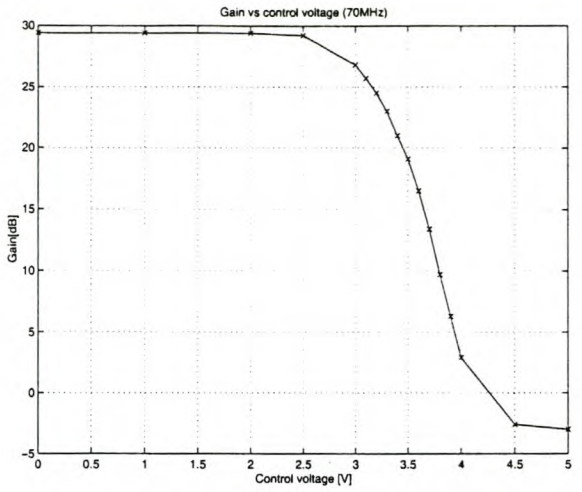


Figure 4.14: AGC amplifier gain versus control voltage.

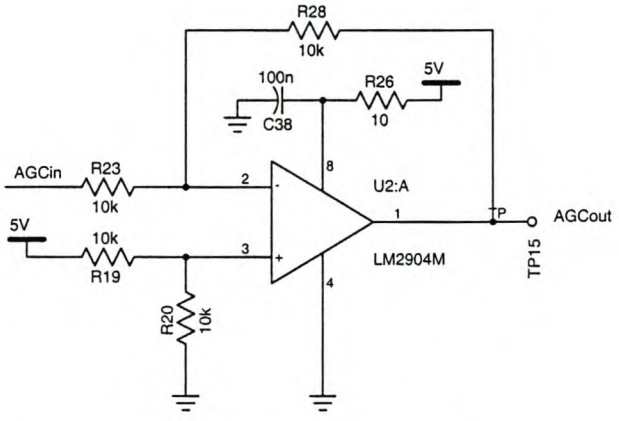


Figure 4.15: AGC amplifier op-amp control circuit.

inversely proportional to the square of the overtone. Oscillation at the fundamental frequency of the overtone crystal is also problematic.

To achieve a pulling range in the order of 100 p.p.m., a second or third harmonic of an oscillator running at the fundamental crystal frequency could be used.

Overtone oscillators

Fundamental mode crystals are rare above 20 MHz as the physical dimensions of the crystal becomes small. Oscillations in a crystal slab take the form of bulk acoustic waves. Bulk acoustic waves result at any frequency that produces an odd half-wavelength of the physical crystal dimension.

Overtone frequencies are not exact harmonics of the fundamental mode but are valid oscillation modes of the crystal slab. The overtone frequencies fall close to but not directly on the harmonics of the fundamental.

A problem with overtone oscillators is obtaining oscillation at the correct overtone and

suppressing oscillations at the fundamental and undesired overtones. A shunt resistor across the crystal is often used to snub oscillations in modes other than the desired overtone.

Colpitts oscillator

A Colpitts type voltage controlled oscillator using a 40 MHz fundamental crystal is used for the fixed datarate symbol clock source.[1] The schematic of the VCXO circuit is shown in Figure 4.16. A feedback network consisting of a tapped capacitive voltage divider (C1 and C2) characterises the Colpitts oscillator. Colpitts oscillators are generally implemented using parallel mode crystals.

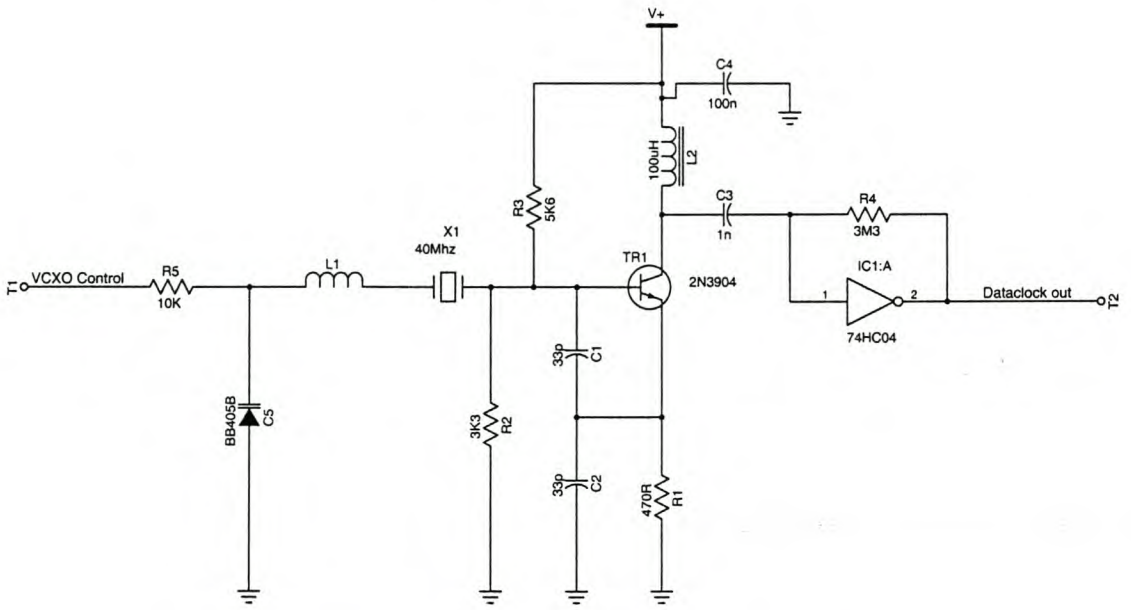


Figure 4.16: VCXO Colpitts oscillator schematic.

Adjustment of the oscillator frequency is possible by shunting a small value trimmer capacitor across the crystal. A BB405B (C5) varactor diode fulfils this function and allows voltage controlled operation of the oscillator. Another method to adjust the frequency of oscillation is to add an inductor (L1) in series with the crystal. Care must be taken not to make the inductor too large, causing oscillation at a frequency not related to the crystal frequency.

Parasitic oscillations are caused when the transistor has sufficient gain at VHF frequencies where stray capacitances or distributed LC elements produce positive feedback. If the oscillator oscillates parasitically in the VHF region a snubber resistor (10 to 50 Ω) could be inserted in series with the transistor base. A small ferrite bead on the base terminal of the transistor can also be used for this purpose. Good layout and careful construction makes an important contribution in eliminating parasitic oscillations.

[1]The specific flavour of the Collpits oscillator was developed by R.H. Honeyborne as part of his practical training at the Electronic Systems Laboratory.

On the output of the oscillator a 74HC04 inverter circuit with a feedback resistor is used as a buffer amplifier. The buffer is required as the oscillator is loaded by the TDA8041 demodulator controller as well as the EPF8282 FPGA clock input.

Fox oscillator

To be able to download data at variable bitrates a programmable variable clock oscillator is desired. The FOX F6053A programmable oscillator is used on the Sunsat Ramtray to generate the clock signal for the imaging system as well as the QPSK modulator. The FOX is a programmable clock generator in a standard oscillator package. A two-wire serial interface is used to program the output frequency. Clock output range from 391 kHz to 90 MHz for CMOS levels and 100 MHz for TTL levels.

The main component of the FOX oscillator is the Cypress ICD2053B programmable phase-lock loop. The only external components required to realise a programmable clock source is a suitable reference crystal.

Due to the high accuracy required between the transmit and receive clocks the demodulator clock was created using the ICD2053B with the standard 14.31818 MHz crystal as used in the FOX circuit. Locking the local clock frequency to the incoming signal clock is achieved by pulling the ICD2053B reference crystal frequency. Figure 4.17 shows the schematic diagram of the programmable FOX oscillator.

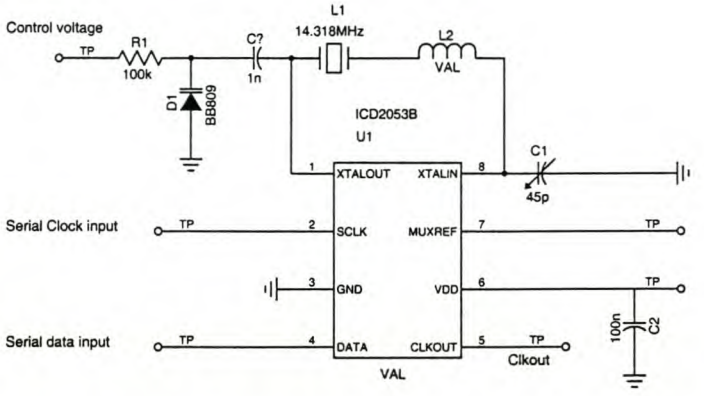


Figure 4.17: FOX oscillator schematic.

The programmable FOX oscillator works satisfactory at lower data rates in the order of 1 to 10 Mbit/s. It is more difficult to lock the transmitted clock to the received clock at higher data rates. This is attributed to the fact that the ICD2053 division ratio is high at faster data rates and this requires extreme accuracy of the original reference oscillator.

4.3.2 IF VCO design

The oscillator tank circuit consists of an inductor in parallel with a variable capacitor configuration as shown in Figure 4.18.

This tank should be tuned to resonate at double the incoming carrier frequency. To close the AFC loop a varactor diode is added to make the oscillator voltage controllable. The

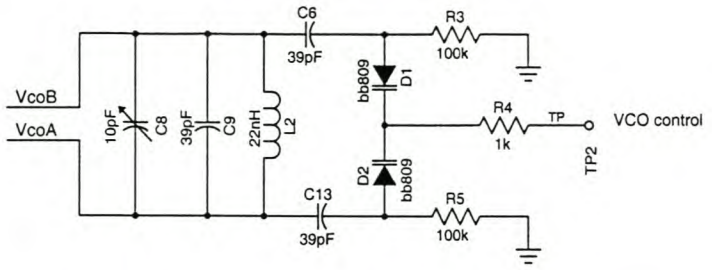


Figure 4.18: IF oscillator tank circuit schematic.

head-to-head varactor configuration (D1 and D2) is used to obtain a more linear frequency versus tuning voltage characteristic with respect to a single varactor configuration.

When calculating the resonant frequency the total capacitance and inductance in the tank circuit loop must be considered. Capacitor C6 and C13 are chosen to select the full range capacitance variation of the varactor diode combination. The main tank capacitance (C9) is adjusted by a trimmer capacitor (C8) to set the centre resonance frequency.

The phase noise of the oscillator is inversely proportional to the quality factor (Q) of the tank circuit . The quality factor can be related to the tank circuit components using the following formula:

$$Q = R\sqrt{\frac{C}{L}} \tag{4.26}$$

in which R is given as 220 Ω and a minimum Q of four is suggested [1].

The simulated frequency versus control voltage is shown in Figure 4.19. The pulling range of the VCO can be seen to be calculated to be approximately 5 MHz which agrees with the measured range of Figure 4.8. The circuit components are selected to ensure that the tank Q exceeds ten at all operating frequencies. The Matlab source for the calculation of the circuit parameters is given in Appendix C.3.

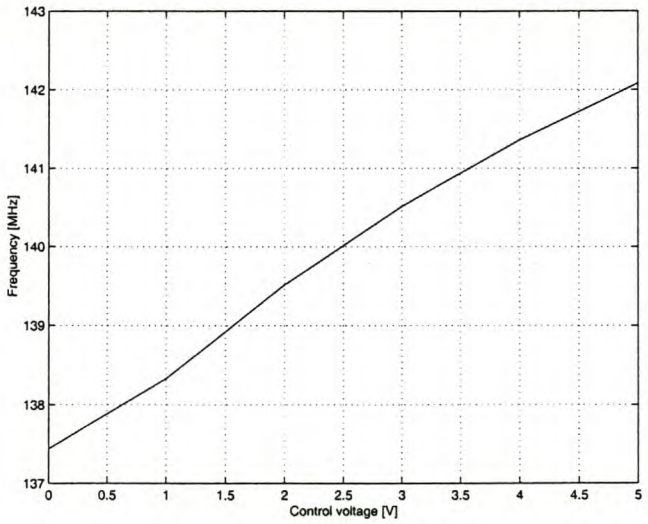


Figure 4.19: VCO tank circuit frequency versus control voltage simulation.

The use of surface mount components for the VCO inductor and trimmer capacitor greatly improves the spectral purity of the VCO. As the VCO operates at double the IF frequency careful layout of the pcb with a good ground plane is essential.

4.4 I and Q channel baseband filters

The I and Q baseband filters can be used to shape the modulated signal (Nyquist filtering) and to suppress unwanted spurious frequency components (assuming all Nyquist filtering is done by a SAW filter in the IF path). Nyquist filtering is needed in the total channel response to minimize inter symbol interference (ISI).

Filtering in the complete transmitter-receiver communication channel takes place in the following sub-systems:

- Low pass filters of the modulator
- Transmitter RF power amplifier
- Low noise converter (LNC) and satellite receiver or tuner
- IF stages and demodulator

It is assumed that little or no filtering takes place in the transmitter, LNC and tuner. Almost all filtering is therefore done in the modulator and demodulator.

Filtering in the modulator prevents transmission of power outside the channel bandwidth. Demodulator filtering is useful to suppress disturbances such as adjacent channels, mixer products and noise. It is therefore logical to split the channel filtering equally between the modulator and demodulator.

4.4.1 Channel response

To obtain the minimum ISI the overall filter response should fulfil the following requirements:

1. The channel amplitude response should cross the half amplitude (-6 dB) point at a frequency equal to half the symbol rate. (Nyquist's first theorem, the minimum bandwidth theorem.)
2. The channel amplitude response must be symmetrical, in linear amplitude terms, about a frequency equal to half the symbol rate. (Nyquist's second theorem, the vestigial symmetry theorem.)
3. The channel phase response should be linear.
4. The filter transition from passband to stopband should be gradual in order to lower the amplitude of ringing.
5. To minimize the zero-crossing jitter, the impulse response should cross half amplitude at plus and minus one-half the symbol duration.

6. Transmitting square bits results in a $\sin(x)/x$ response, this should be compensated for when the overall channel response is designed.

A general class of filter that meets the above requirements and which is often used in digital microwave transmission systems is the raised cosine filter. Raised cosine filtering is simply one class of filter that meets the criteria for Nyquist filtering.

To realise a raised cosine transfer function for the complete channel requires considerable effort. The non-linear characteristic of the satellite power amplifier makes exact design of a raised cosine channel response difficult. General channel filtering with symmetrical amplitude response around the Nyquist frequency minimizes inter symbol interference sufficiently [9, 11].

In addition to the requirements above the I and Q filters must also be closely matched to each other in amplitude and phase response to ensure proper operation of the recovery algorithms.

4.4.2 Modulator filters

The demodulator channel filters have to be designed together with the modulator filters to obtain the desired channel frequency response. The Sunsat 1 modulator data shaping filters are therefore discussed in this section.

The maximum datarate the *modulator* system is designed for is 60 MBit/s implying a symbolrate of 30 Msymbol/s per baseband channel. Bessel or maximally flat delay filters are popular to filter digital signals due to their linear phase response. In the Sunsat 1 modulator fifth order Bessel filters are used to perform the baseband filtering.

An extract of the modulator schematic showing one filter is given in Figure 4.20. The resistor DAC outputs from the FPGA device as well as the voltage divider used to set the desired DC level to the quadrature modulator are shown.

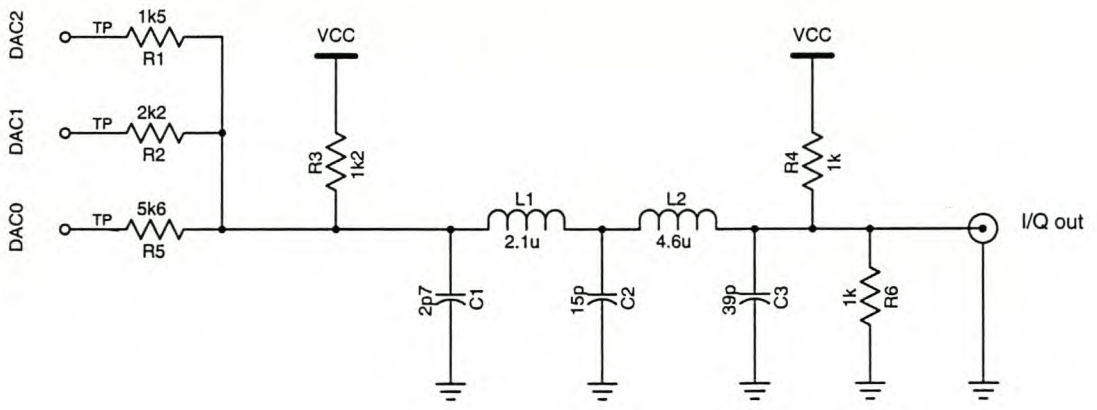


Figure 4.20: Modulator I and Q channel filter schematic.

Filter bandwidth effects

The modulator filter bandwidth not only affects the occupied bandwidth but also the

transmitted power. Filtering smoothes the transitions between signal states and narrows the frequency spectrum required. The filter transition from passband to stopband should be smooth to lower the amplitude of ringing.

If no modulator filtering is done the transitions between signal states are instantaneous and transmitting the signal requires infinite bandwidth. If 100% excess bandwidth is used the transitions between states are gradual and less power is needed for the transitions.

For an unfiltered signal the peak power of the carrier and the nominal power at the symbol states are equal. As the bandwidth is reduced the overshoot and therefore the peak power requirement of the power amplifier increases.[2]

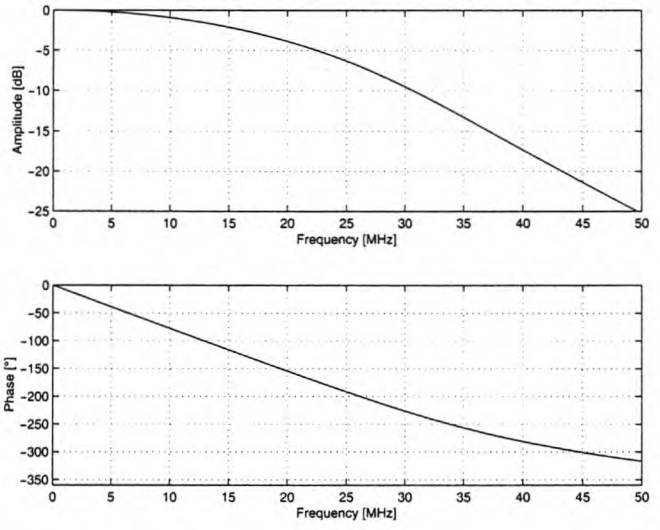


Figure 4.21: Modulator I and Q channel filter amplitude and phase response.

The amplitude and phase response of the modulator channel filters are shown in Figure 4.21. The excess bandwidth of the filter results in a pulse response that is smooth with the minimum of overshoot or ringing as can be seen in Figure 4.22.

The non-linear characteristic of the power amplifier will worsen any amount of overshoot and therefore the pulse is made as smooth as possible to begin with.

At the modulator, bandwidth efficiency is traded for transmit power economy. The satellite transmitter power is limited and therefore all available power is directed towards transmitting the strongest possible signal.

Interference to other users due to the excess bandwidth is unlikely. A high gain groundstation antenna with fast and accurate tracking is required for proper reception of the satellite signal. In addition the short duration of a satellite pass over the groundstation further minimizes the probability of interference to other users of the spectrum.

The natural $\sin(x)/x$ response of the NRZ data will influence the transmitted spectrum of the data. This effect is shown in in Figure 4.23 using 40 Mbit/s data or 20 Msymbol/s per channel. Compression due to the non-linear operation of the RF power amplifier will cause spectral regeneration. Spectral regeneration mainly affects high frequency components

[2]Nyquist filtering with 20% excess bandwidth (the approximate minimum of most digital radios) requires 5 dB signal power above the unfiltered case [12].

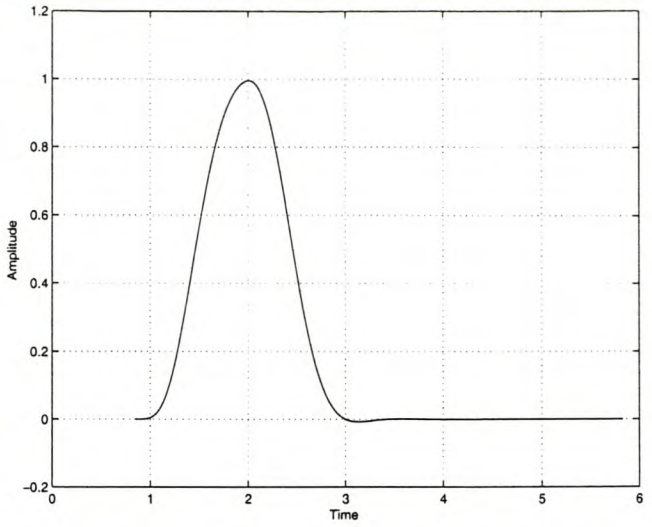


Figure 4.22: Modulator I or Q channel filter unit pulse response.

of the signal as well as the data sidebands which are already greatly attenuated (see [13] for simulation of this effect).

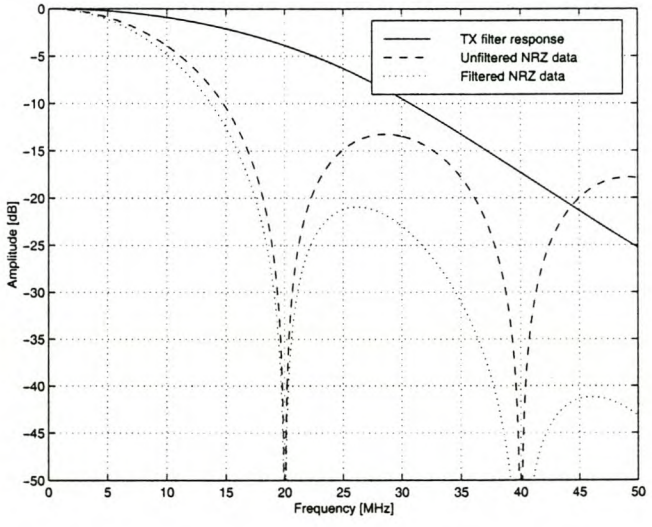


Figure 4.23: Modulator channel spectrum.

4.4.3 Demodulator filters

The lowest error rate is obtained when the received signal is maximized compared to the received noise. The optimum signal to noise ratio solution is a filter matched to the signal component of the received signal. Any matched filter will result in the optimum SNR solution, however only Nyquist filtering provides the minimum bandwidth occupancy while at the same time minimizing ISI.

Due to the fact that variable bitrate is required the *modulator* filters are designed with the maximum bitrate in mind. A demodulator bandwidth designed for the maximum datarate allows more excess bandwidth at lower data rates but also increases the noise power received. For the development and test purposes the demodulator filters are intended for 40 Mbit/s demodulation.

The schematic of the third order LC-ladder Besselfilters used is in the demodulator I and Q channels is shown in Figure 4.24.

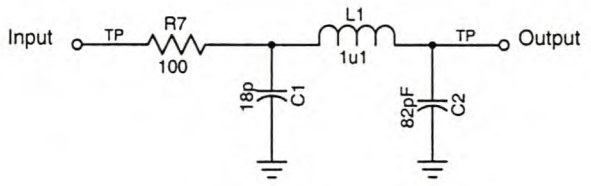


Figure 4.24: Demodulator I and Q channel filter schematic.

The desired filter order and cut-off frequency is found through simulation of the total channel response. The required filter component values are then found from tables [14] and scaled to the proper frequency and impedance using Matlab. The demodulator filter amplitude and phase response is shown in Figure 4.25.

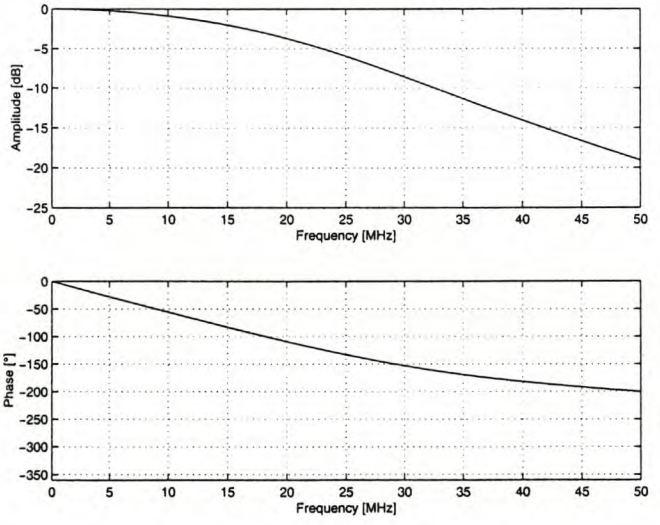


Figure 4.25: Demodulator I and Q channel filter amplitude and phase response.

The demodulator filter combined with the received data spectrum yields the data spectrum shown in Figure 4.26. As can be seen from the total channel frequency response in Figure 4.26 the amplitude decreases gradually.

If the filter output is considered to be negligible below -20 dB (less than 1% of output power) the total filter bandwidth is approximately 17 to 18 MHz. An idea of filter excess bandwidth can be obtained by relating this bandwidth to the minimum Nyquist bandwidth of 10 MHz, resulting in an excess bandwidth of nearly 80%.

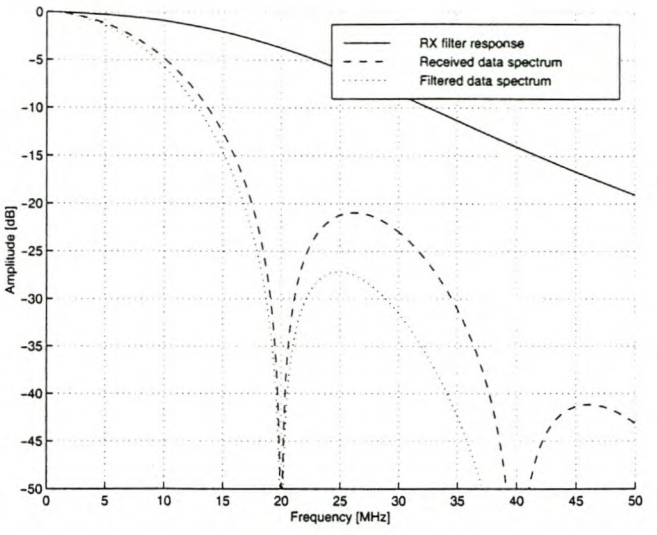


Figure 4.26: Received and filtered data spectrum.

The total channel frequency response is plotted on a linear scale in Figure 4.27. The amplitude response can be seen to go through the half amplitude point at 10 MHz, the Nyquist frequency for a 20 Msymbols/s symbol rate. The response is reasonably symmetric around this point and frequency components above 20 MHz becomes insignificant.

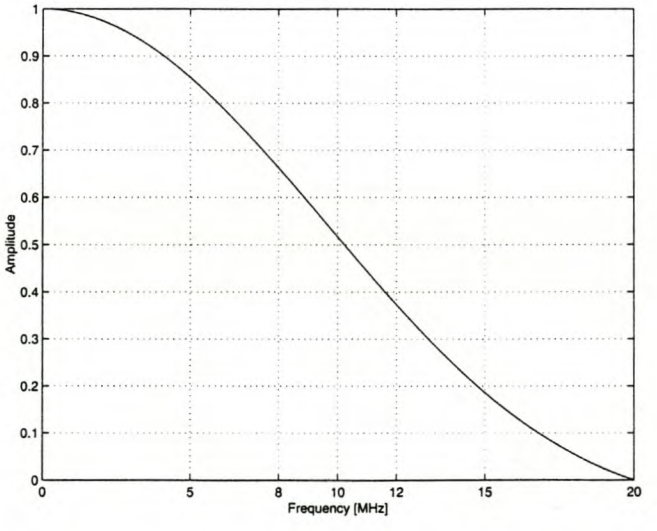


Figure 4.27: Total channel frequency response.

The amount of ISI caused by the filtering can be evaluated by plotting the response to a single input data bit. The response should be symmetrical with the output close to zero at the sampling instants of subsequent data bits.

The total channel response to a unit pulse is shown in Figure 4.28. The large amount of excess bandwidth can be seen in the lack of overshoot or ringing in the response.

The effect of compression is not included in this simulation and will have the effect of emphasizing any amount of overshoot in the pulse.

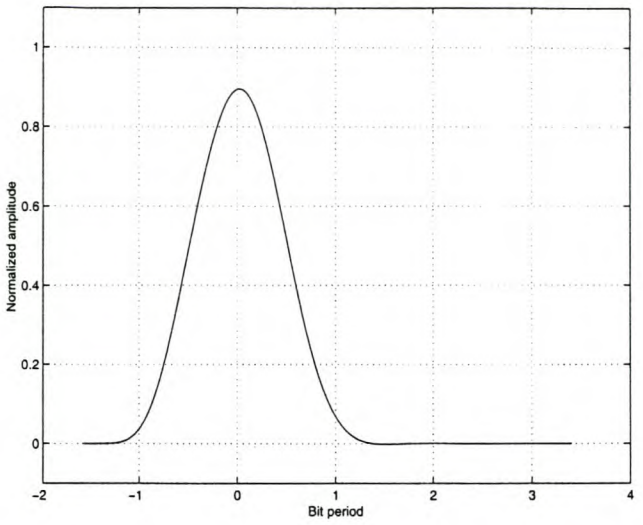


Figure 4.28: Total channel unit pulse response.

Figure 4.29 shows the measured unit pulse response of the complete modulator demodulator chain with the exception of the RF power amplifier.

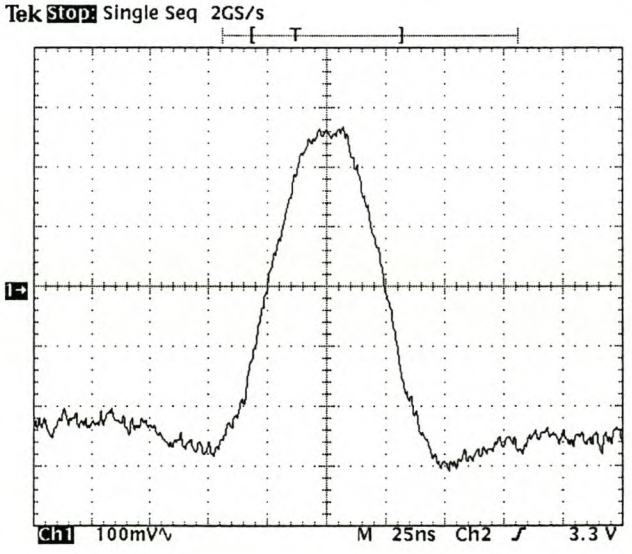


Figure 4.29: Measured channel unit pulse response.

All measurements are made at a bitrate of 40 Mbit/s. There is some noise on the signal caused mainly by the digital demodulator controller and decoding logic. The FPGA device used to do the logic decoding generates significant noise levels. The pulse agrees in shape with that of the simulated pulse shown in Figure 4.28. Additional noise is obvious on the signal as well as overshoot on the base of the pulse.

The measurements are repeated in Figure 4.30 with the RF power amplifier included in the overall transmitter-receiver chain. The power amplifier worsens the overshoot or ringing in the pulse shape.

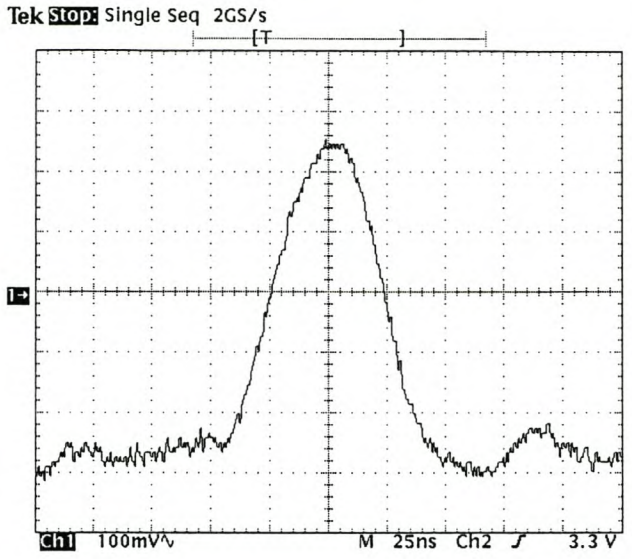


Figure 4.30: Measured channel unit pulse response with PA.

Equivalent noise bandwidth

The noise-equivalent bandwidth for a lowpass filter is given by equation (4.27):

$$B_N = \frac{\int_0^\infty |H(f)|^2 \, df}{H^2(0)} \tag{4.27}$$

The noise bandwidth of the receiver filter is found numerically to be just less than 20 MHz. This is calculated by integrating the area under the receiver filter to where the amplitude response is negligible. This value is then divided by the maximum gain in order to determine the equivalent noise bandwidth.

Chapter 5

The digital decoding logic

5.1 Demodulator logic functions

After bit decision is made on the analogue I and Q channel signals, digital logic is needed to convert the parallel I and Q digital data into a serial bitstream with a synchronized data clock.

The I and Q datastreams, the extracted data clock as well as the synchronized symbol clock are the main inputs to the digital demodulation logic. The desired output is the serial datastream with a synchronized clock signal. Control lines to indicate carrier detect and data detect states are also made available.

The parallel to serial conversion, baseband transitional decoding and PRBS unscrambling are implemented using logic circuits. A data detection circuit is provided to indicate when valid data is available for capture. The correct demodulated phase is multiplexed to the serial data output. Methods to switch between BPSK, QPSK and OQPSK demodulation are also provided.

The versatility and rapid prototyping capabilities of FPGAs are ideal for the development of the logic decoding function. The Altera FLEX8000 FPGA series together with the MaxPlus II environment are used for this development.

The modulator and demodulator logic are closely related. Therefore, where relevant, some of the main components of the modulator logic are discussed together with that of the demodulator.

5.1.1 General overview

A blockdiagram of the digital decoding logic functions is shown in Figure 5.1. The corresponding top level graphic design file is provided in Figure F.1 of Appendix F.

The digital I and Q signals are fed to two decode blocks[1] where the NRZI decoding is done, the data is serialized and then unscrambled. The two decoding blocks are identical except that one is fed with I and Q data that has been shifted by 90° with respect to

[1]The basis of the demodulator decoding block was developed by L.C. Schwardt and R. van der Merwe as part of their development of the Sunsat 1 S-band QPSK modulator logic.

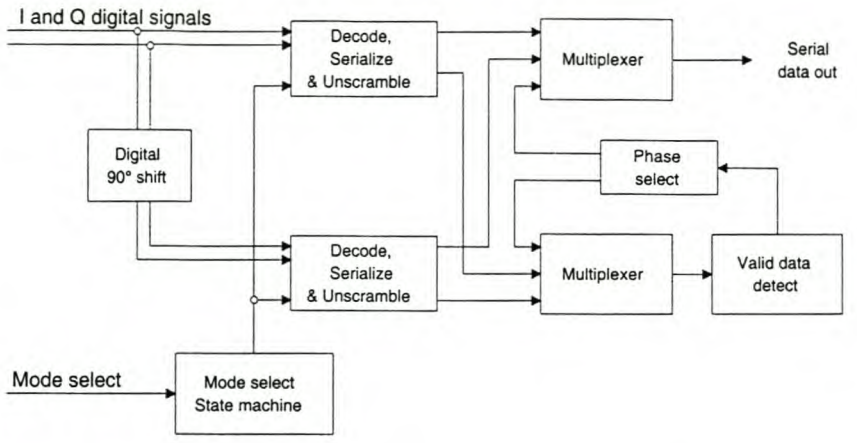


Figure 5.1: Block diagram of digital decoding logic.

the other. This 90° digital phase shift is a simply a digital remapping of the received constellation points.

The output of each decoding block is fed to two different multiplexers. The purpose of the first multiplexer is to select which datastream is output on the serial data output pin. The second multiplexer feeds the *other* datastream to the valid data detector circuitry.

The valid data detector simply consists of three shift registers of which the outputs are compared to a predetermined data pattern. When a valid data pattern is detected a pulse is output to the phase select logic. This pulse causes the phase select circuitry to change state and the datastreams are swapped around. In this manner the most recent valid datastream is output while the other is searched for a recognizable pattern.

Finally a state machine is implemented to select the demodulation method used. The digital decoding logic is capable of decoding BPSK, QPSK and OQPSK even though the preceding hardware is not intended for OQPSK demodulation.

The logic is divided into three main parts: the basic control functions, the decoding logic and the valid data detection.

5.2 Basic control functions

5.2.1 Clock distribution

Reliable clocking is critical to the successful operation of any digital design, irrespective of whether it is implemented with discrete logic, programmable logic or custom silicon. Poorly designed clock configurations lead to erratic behaviour with temperature, voltage or fabrication process variations.

Asynchronous inputs can cause an incorrect value to be clocked into a flip-flop or cause a flip-flop to enter a metastable state in which its output is not recognized as a 1 or a 0. To avoid metastability problems asynchronous signals should not fan out to more than one flip-flop within the device [15].

For the logic circuit to be synchronous, a single master clock from an input pin should clock every flip-flop in the FPGA device. Global (or synchronous) clocks are the simplest

and most predictable to implement. The Altera FLEX 8000 devices support only pin-driven global signals.

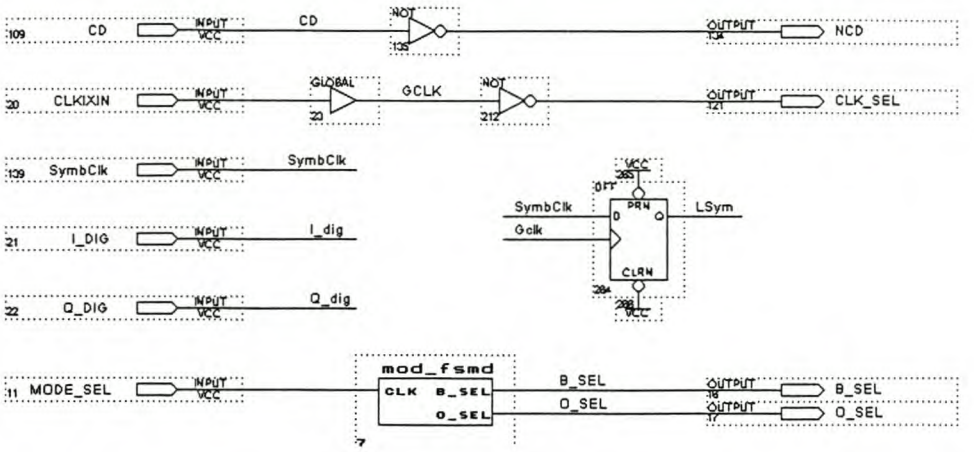


Figure 5.2: Graphic design file of basic control functions.

The clock signal input (see `CLKIXIN` in Figure 5.2) is sent through a global logic cell to ensure that the signal is available throughout the FPGA with minimum delay. A global logic cell passes through the global routing on a device and is able to feed every other cell in an Altera FPGA device. Global signals propagate more quickly than array signals and free up the device resources for other logic.

All signal transitions within and generated by the demodulator logic use the edge of the global clock, `GCLK`, as a reference. The synchronous logic also requires synchronously-clocked inputs to avoid race conditions, setup and hold time violations and other logic problems.

The external symbol clock, `SymbClk`, is also latched using the global clock signal. This is done to ensure that the symbol clock is aligned to the dataclock.

5.2.2 Mode selection: BPSK, QPSK or OQPSK

The mode select input of the mode select block (see `MODE_FSMD`, Figure 5.2) selects between BPSK, QPSK and OQPSK demodulation. The outputs of the mode select block (`B_SEL` and `O_SEL`) control the demodulation method the decoding blocks use.

The mode select pin is connected to the clock input, `MODE_SEL`, of a state machine implemented using Altera Hardware Description Language (AHDL source provided in Appendix F.4). The demodulation method is changed by simply toggling the input of this state machine.

The `B_SEL` signal is connected to a multiplexer in the decode block which selects only the in-phase datastream for BPSK demodulation or both datastreams for QPSK demodulation. The `O_SEL` signal selects between QPSK and OQPSK demodulation by switching one additional latch in or out of the quadrature datastream to compensate for the data timing offset.

The method of using a single input state machine and toggling between states is used on the Sunsat QPSK modulator due to the limited number of telecommand signals available.

5.2.3 Capture hardware signaling

The capture hardware that will be used to capture and save the received digital data consists of a plug-in PCI interface card and a personal computer. The captured data is saved to a conventional harddrive from where it can be processed further. The hardware is currently capable of capturing serial datastreams in excess of 40 Mbit/s.

There are three inputs to the capture hardware: the data, clock and capture signals. The data capture hardware requires a signal to indicate when to start data collection. Data is captured as long as the capture signal is held low.

The carrier detect signal of the demodulator controller indicates that the recovery loops have locked to a valid QPSK signal. As the capture hardware requires an active low signal this carrier detect signal (`CD`, Figure 5.2) is inverted in the digital decoding logic and output as `NCD` to the capture control logic.

The physical interface between demodulator logic and the capture hardware is a direct connection using twisted pair wire. Low-voltage differential signalling (LVDS) drivers has been tested between the two devices resulting in reduced loading and less interference.

5.3 Decoding, serializing and unscrambling

5.3.1 Serializer

To understand the functioning of the deserializing process some aspects of the serial to parallel converter used in the modulator is explained first. The modulator data splitter and demodulator data combiner have several similarities.

Modulator

At the modulator the incoming serial datastream is split into two parallel I and Q channel datastreams at half the bitrate. The method requires a means to synchronize the two individual data streams.

To load a register on a specific rising edge of a global clock the preferred method is to use the clock enable input of a flip-flop to control when the register is loaded. Clock enable is a level-sensitive signal, when the clock enable is low, clock transitions on the clock input to the flip-flop are ignored.

Two timing signals or symbol clocks are generated with a period double that of the original data stream and with a phase difference of 180°. These two signals are then used to control on which edge of the original clock signal the data in each channel is latched. Figure 5.3 shows the logic used in the generation of these two timing signals denoted as `ENA_A` and `ENA_B`. The latching of the incoming datastream can also be seen.

The serial-to-parallel converter is made up of two D-latches with output enable pins that are driven by the `ENA_A` and `ENA_B` signals as shown in Figure 5.4. The latches are still clocked using the original clock signal, but the enable lines are used to separate the datastreams. In this manner the possibility of timing problems due to the use of a secondary clock is avoided.

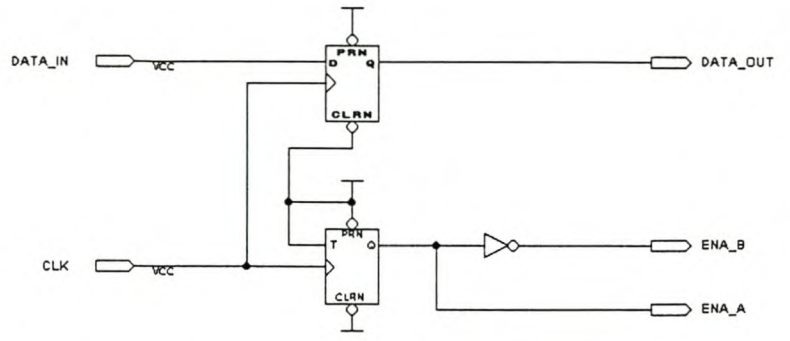


Figure 5.3: Modulator data latches and symbol clock generation.

This method generates two channels that are naturally offset by half a symbol period with respect to the other. An additional latch is required to align the two data channels in order to generate QPSK signals. A multiplexer is added to switch the additional latch in and out of the I-channel. The NRZI encoding can also be seen in Figure 5.4 and is discussed further in Section 5.3.2.

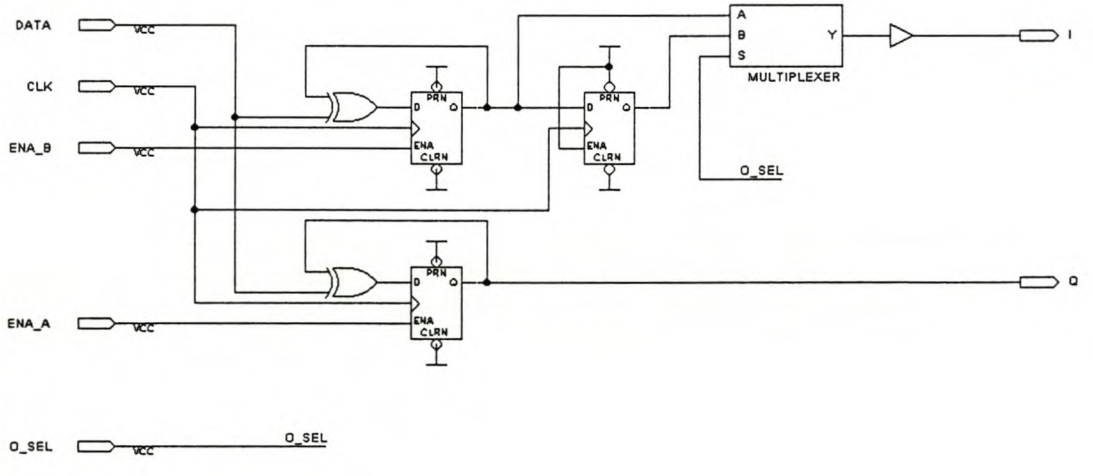


Figure 5.4: Channel data splitter and transitional encoding.

Demodulator

At the demodulator the incoming parallel datastreams are combined in order to reconstruct the serial bitstream. The data combiner and transitional decoder is shown in Figure 5.5 .

As in the modulator the use of a secondary clock is avoided by using the enable inputs of the data latches. The data latches are alternatively enabled by the symbol clock to

control on which edge of the incoming data clock the data is latched.

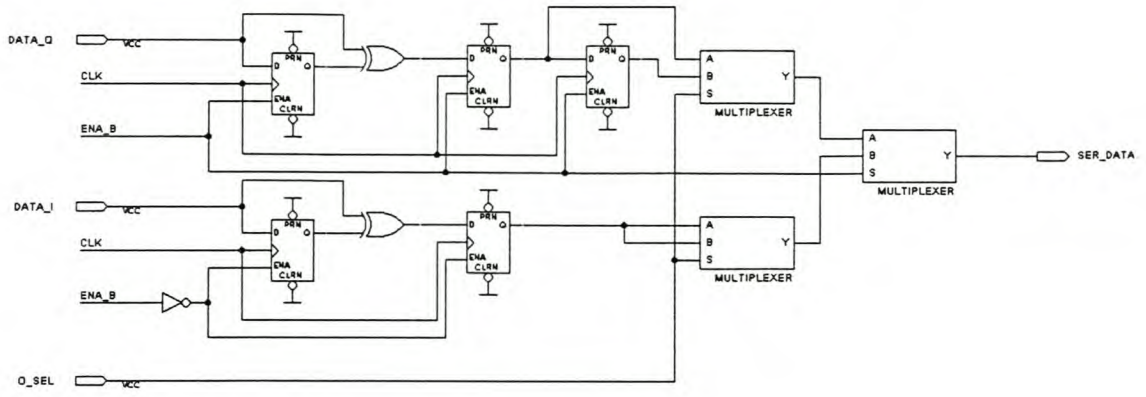


Figure 5.5: Channel data combiner and transitional decoding.

To enable the demodulation of OQPSK datastreams an additional latch can be multiplexed in or out of the Q-phase datastream. The latch delays the Q-phase datastream by one dataclock period to align it with the I-phase channel before being combined. An identical dummy multiplexer is used in the I-phase channel to avoid timing differences between the two datastreams.

5.3.2 Baseband transitional coding

Non-return-to-zero (NRZ) coding is the default representation of uncoded logic signals. The data bit is either high or low for the entire bit period depending on whether a logic 1 or 0 is sent. NRZ data requires a clock signal to synchronize the databits.

A transitional code represents a particular data bit value as a change of the output bitstream state, rather than the data bit value itself. In non-return-to-zero-inverted (NRZI-S or NRZI-Space) encoding the output bitstream changes state whenever the input data is a zero bit. If the input data is a one bit no change is made in the state of the output bitstream.

Alternatively NRZI could be implemented with an output state change on reception of a one bit and no state change on reception of a zero bit (NRZI-M or NRZI-Mark).

Transitional coding implementation

Different methods exist to implement a NRZ to NRZI encoder (or simply coder). The traditional coder and decoder for a zero-bit transitional code (NRZI-Space) is shown in Figure 5.6.

An alternative method to effect one-bit transitional (NRZI-Mark) encoding is shown in Figure 5.7. This is the coding method used for the Sunsat QPSK modulator application due to its simple implementation.

The coder output is inverted depending on the starting state of the flip-flop. The decoder output may also be inverted due to the inherent phase ambiguity of the carrier recovery algorithm employed.

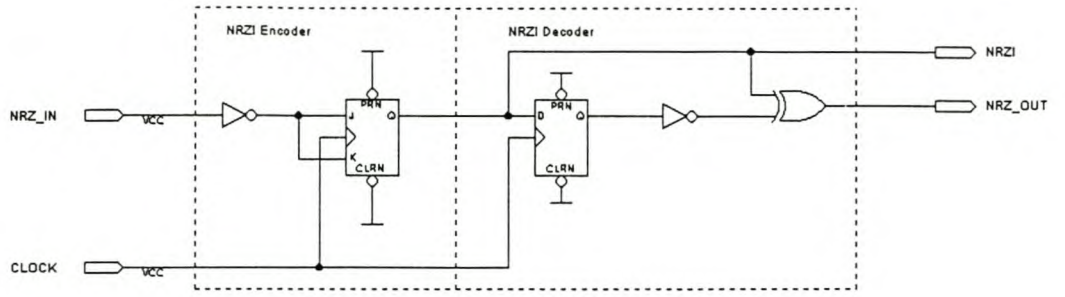


Figure 5.6: Traditional NRZI coder and decoder (NRZI-Space).

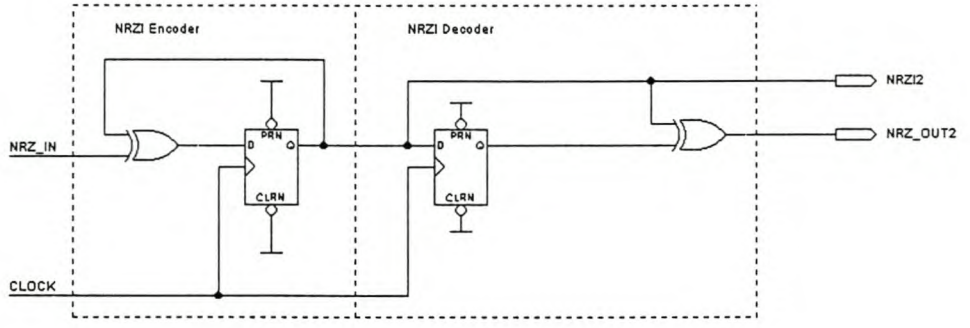


Figure 5.7: Alternative NRZI coder and decoder (NRZI-Mark).

Inversion of the received data is not a concern for the decoder since it acts only on data transitions. The decoder correctly recovers original data stream even if the encoded data stream is accidentally inverted somewhere in the demodulation process.

Transitional coding simulation

Simulated waveforms of both coders and decoders can be seen in Figure 5.8 with the signal names as used in Figure 5.6 and Figure 5.7. The outputs of the two coders are inverted with respect to each other due to the different transitional coding methods employed. It is clear that if a zero-bit transitional decoder is used to decode a one-bit transitional code the data will be inverted.

Glitches in the decoder output can be seen. This is caused by the feedforward structure of the XOR gate and decoder together with the finite switching time of the latch output. An additional latch on the decoder output is used to remove these glitches and also serves to align the data to the clock signal.

5.3.3 Data scrambling and descrambling

Digital data streams may exhibit short cycle periodic patterns that deteriorate receiver performance [11]. The effects of periodicity in the data stream are the following:

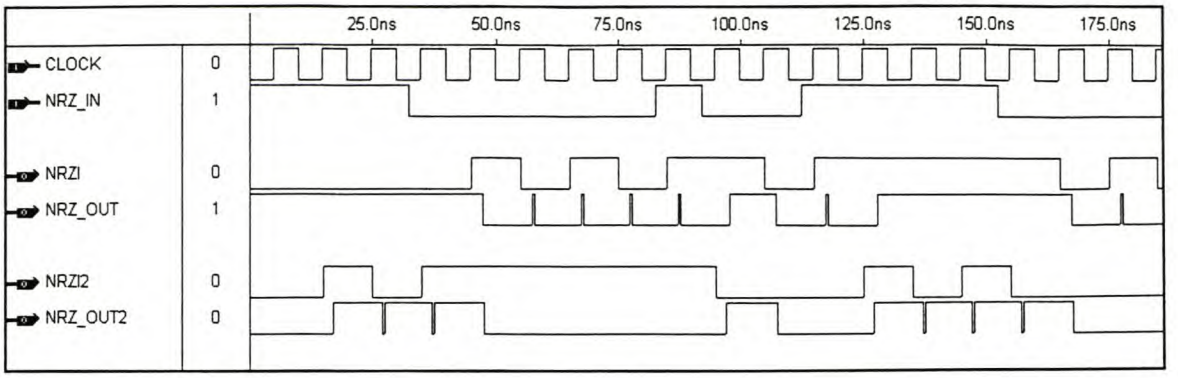


Figure 5.8: Timing waveform simulation of NRZI coding and decoding.

- Unwanted line components appear in the transmitted RF spectrum.
- Possible synchronization loss of the clock recovery circuit.
- False lock to data sidebands created by the clock recovery circuit non-linearity.

Scrambling data is a method of substantially increasing the period of the input data while still permitting recovery of the original data sent. It further ensures that sufficient data transitions exist for the clock recovery circuits at the receiver to function properly. A Pseudo-Random Binary Sequence (PRBS) or Pseudo noise (PN) generator is often used to scramble the transmitted data.

Pseudo-Random Binary Sequences (PRBS)

PRBS sequences are members of a class of codes known as maximal-length codes. By definition, maximal-length codes are the longest codes that can be generated by a shift register of a certain given length.

PRBS sequences are useful in the design and test of data communications equipment, because of the following desirable properties:

- The length of the sequence is $2^n - 1$ where n is the number of bits in the shift register.
- Maximal-length: the sequence is as long as possible without repeating. All possible n-bit words appear only once during the generation of a full cycle except the all-zero word.
- Approximate DC-balance: the sequence has a single more one than zero, which for even small values of n results in a small or negligible DC offset.
- Ideal auto-correlation properties: the sequence does not correlate when shifted and thus resembles white noise. It may even be used as a white noise generator.
- Self-synchronizing: a simple shift register circuit can synchronize the sequence.

PRBS autocorrelation properties

If the periodic autocorrelation value is denoted as $\phi(s)$, where s is the relative shift of the PRBS sequence the following properties are valid:

- $\phi(s) = 2^{n-1}$ for $s = 0$, i.e. when the sequence is perfectly aligned with itself.
- $\phi(s) = -1$ for $s \neq 0$ i.e. for any polar binary (-1,1) sequence offset from itself.
- $\phi(s) = 2^{n-1} - 1$ for $s \neq 0$ i.e. for any on-off binary (0,1) sequence offset from itself.

PRBS generation

A PRBS generator is created using a shift register with some feedback taps. The outputs from the taps are combined using the XOR operation and fed back to the input of the shift register. The generated PRBS output can be taken from any of the register flip-flop outputs.

An eight bit shift register with feedback taps that are combined using XOR gates is used in the Sunsat QPSK modulator. This simple method allows for a low resource burden on the logic device at the transmit as well as receive side.

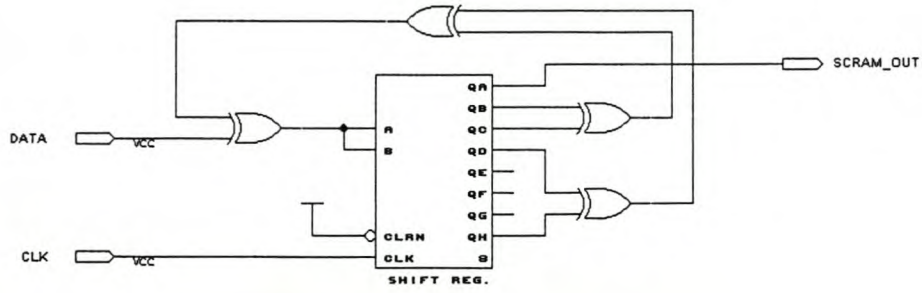


Figure 5.9: Serial data scrambler.

Figure 5.9 shows the data scrambler circuit implementation as used in the modulator logic. The 8 stage shift register with feedback taps at 2, 3, 4 and 8 creates a sequence length of 255. The feedforward structure used in the demodulator to unscramble the data as shown in Figure 5.10.

The data scrambling and descrambling circuitry in both the modulator and demodulator can be switched in or out of the datastream by means of a multiplexer. This function is intended for test purposes only and the operational hardware is hardcoded to scramble data permanently.

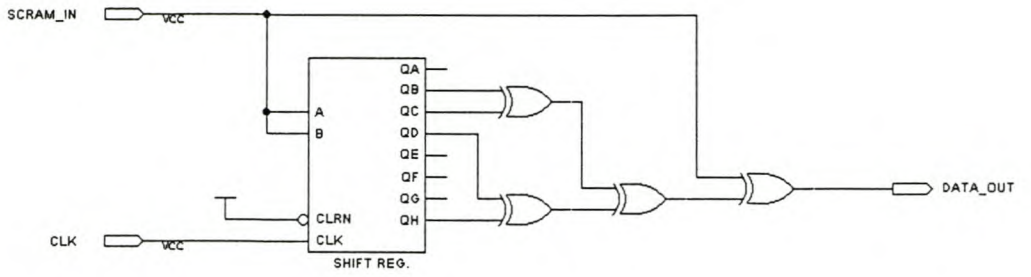


Figure 5.10: Serial data descrambler.

5.4 Data detection output

5.4.1 Phase ambiguity

QPSK demodulation has an inherent four-fold phase ambiguity due to the carrier recovery methods used. The differential coding employed in the modulator/demodulator system reduces the phase uncertainty to only two possible states.

The received datastream as well as a datastream that has been rotated by 90° is demodulated. One datastream is output by default while the other datastream is monitored for the valid data pattern. If the valid data pattern is detected the datastreams are swapped around. Using this method the datastream with the correct phase is thus always multiplexed to the output datastream.

The 90° phase shift is implemented digitally by advancing each symbol received by one position in the constellation. This phase shift is done by the `MAP90` block shown in Figure F.1. The constellation mapping is shown graphically in Figure 5.11. The VHDL source code is provided in Appendix F.5.

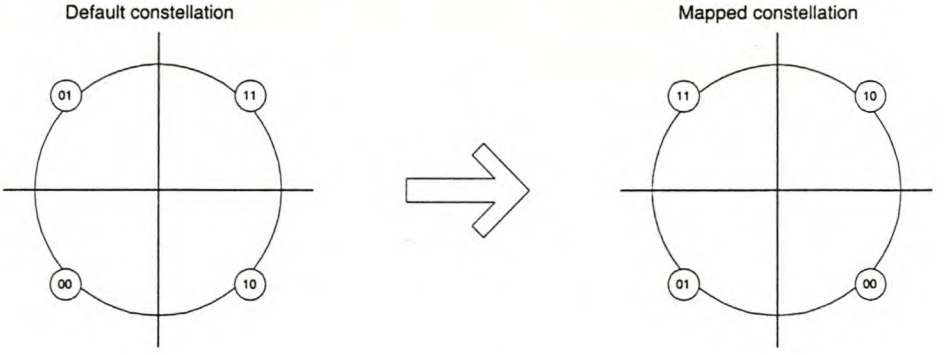


Figure 5.11: Constellation remapping.

5.4.2 Valid data detection logic

Some means to detect whether the correct signal phase is being demodulated is necessary. A simple shift register data detector is implemented to search for the three valid white

reference bytes in the imager data. The reason the white reference bytes are used is as follows:

- The three white reference bytes are information already built into the imager data format that appears at regular intervals.
- The three successive white reference bytes are the maximum length recognizable pattern that will appear in a one colour as well as a three colour image.
- The image data itself should not contain any bytes equaling the value of the white reference bytes.
- Inline telemetry can be used to detect valid data but this will imply that the demodulator data detection sequence will need to change for each received image.
- The use of image line numbers for synchronization will need complex counters that keep log of line numbers as well as the number of received bytes.

The choice of the white reference bytes for synchronization is not optimal for synchronization purposes. An improved modulator system could send a known synchronization code in order for the groundstation to achieve correct phase synchronization before data transmission starts.

Implementation of the valid data detector

The valid data detector consists of three eight bit shift registers in serial as shown in Figure 5.12. The three most recent bytes received are stored in this manner. A pattern detector compares the shift register outputs at each clock interval. If a valid pattern is detected a logical one is output on the valid data output (`DATA_DETECT`).

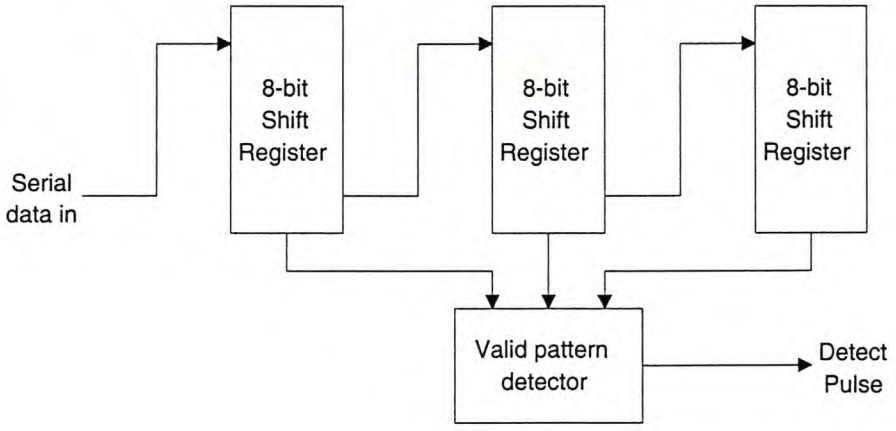


Figure 5.12: Valid data detector blockdiagram.

5.4.3 Phase select state machine

The phase select state machine ensures that the correct demodulated phase is multiplexed to the serial data output. When a valid datastream is detected this datastream is multiplexed to the serial data output and the other datastream is searched for a valid pattern.

The state machine consists of one T flip-flop that simply changes output state with each input pulse (as shown in Figure F.1). The output of the T flip-flop, `Det_state`, controls both multiplexer that feed the serial data output (`SerData`) as well as the multiplexer that feed the valid data detection logic.

Chapter 6

Test and measurement of digital microwave radio

This chapter deals with the measurement and test procedures important to measuring the analogue and digital signals in a digital microwave radio system. Practical measurements relevant to the implemented QPSK demodulator are also presented. Finally the implementation loss of the demodulator is measured.

6.1 Satellite digital microwave radio (DMR)

Regardless of the specific type of PSK or QAM used in a digital microwave radio system, I/Q or vector modulation is the main method used to modulate and demodulate the data.

Digital microwave signals transmitted from satellites suffer from low signal-to-noise (SNR) ratios due to large path loss and limited transmitter output power. In order to transmit the maximum RF power the transmitter operates at a high efficiency causing it to introduce non-linear distortion. This distortion takes the form of AM-to-PM conversion, AM-to-AM conversion and non-flat frequency response characteristics. Microwave satellite links also experience Doppler frequency shift.

Test and measurement procedures are needed to adjust modulator and demodulator quadrature and amplitude imbalances, test bit error rates (BER), measure filter responses and simulate flat and dispersive fades.

6.2 Vector modulation measurements

A spectrum analyser is an integral part in the development and testing of RF components in a communication system. In digital radio systems utilizing vector modulation it is desirable to evaluate the carrier phase as well as carrier magnitude. I- and Q-channel or phase plane measurement is possible with a vector analyser.

I/Q Modulation

An I/Q modulator with accurate quadrature and amplitude balance is needed for demodulator testing and calibration. A high degree of modulator linearity and a spurious free output in the modulation bandwidth is essential. A vector signal generator is capable of a variety of standard vector QAM and PSK modulation types.

For test purposes filtering is required to limit the test signal bandwidth similar to that used in the transmitter. Due to the fact that phase modulation is used, line lengths feeding coherent signals should be of equal length and kept short to avoid phase differences.

I/Q Demodulation

Separate instrumentation quality demodulators are required when trying to separate receiver from transmitter errors in back-to-back tests. Modulators require precise quadrature balance, amplitude balance and linearity. Local oscillator and sum component feedthrough as well as DC I- and Q-channel offsets must be avoided.

Vector modulation analysis

Three fundamental display modes are used to analyse the functioning of a digital radio (see Figure 6.1):

- I and Q inputs versus time - eye diagram
- I and Q inputs in X versus Y format at a specified instant - constellation diagram
- I and Q inputs in X versus Y format continuously - vector diagram

Eye diagram. *Vector diagram.* *Constellation diagram.*

Figure 6.1: Display modes used to analyze QPSK modulation [5].

Eye diagrams are a popular method of evaluating digital radio performance. On an oscilloscope the analogue I and Q channel signals are displayed against time to measure the eye diagram. This method is suitable for observing the eye diagrams of the received data, but the relationship between the phase of the channels is not clear.

The I and Q channel data is best viewed in a X versus Y fashion or vector diagram format. Traditional oscilloscopes have a much lower X bandwidth than Y bandwidth making vector diagram measurement on an oscilloscope impractical for high bitrate systems. However a vector analyser or a constellation analyser is designed for high bandwidth X versus Y displays.

Practical eye diagram measurement

Eye diagrams are measured by synchronizing the oscilloscope to the recovered symbol clock and plotting consecutive data bits over each other. The eye diagram after the demodulator filters at a datarate of 40 Mbit/s can be seen in Figure 6.2.

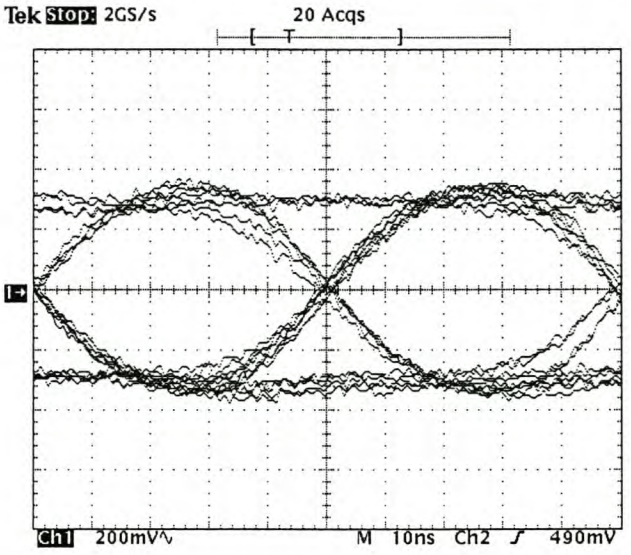


Figure 6.2: Measured eye diagram no power amplifier (40 Mbit/s).

A stable eye diagram is obtained with the eye somewhat closed in the center and with some zero crossing jitter. The zero crossing jitter is typical of a system with a high excess bandwidth (80% in this case) [11]. As the excess bandwidth is increased the eye opens up and the zero crossing jitter decrease. Lower excess bandwidth decrease the occupied spectral width as well as the noise bandwidth but better clock recovery is needed.

The eye diagram with the power amplifier in the modulator/demodulator chain in shown in Figure 6.3. The deformation of the pulse shape leads to increased eye closure. This closure represents a performance penalty of approximately 2 dB over the eye without the power amplifier.

6.2.1 I/Q Modulator/Demodulator alignment

The main component of digital radio link is the I/Q modulator and demodulator. The fundamental measure of performance is the quadrature error and amplitude balance characteristics.

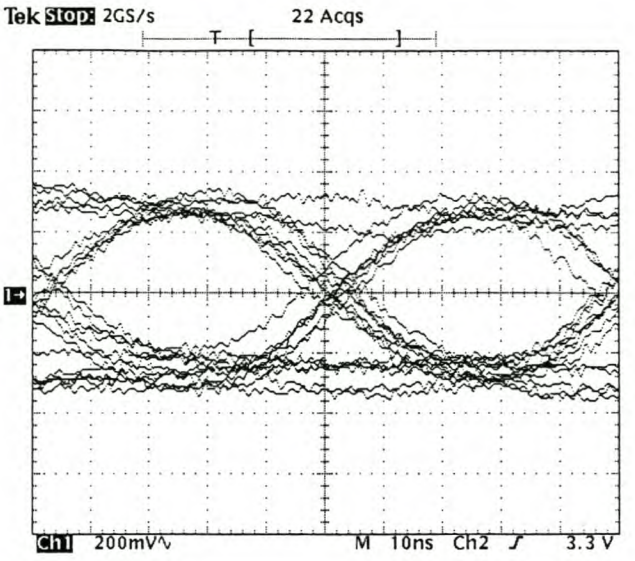


Figure 6.3: Measured eye diagram with power amplifier (40 Mbit/s).

Effects of alignment errors

Alignment errors have similar effects on modulator as well as demodulator performance.

Amplitude imbalance result when one channel has a different gain than the other channel. This results in erroneous phase and magnitude response of the modulated signal output. If the constellation diagram is viewed the constellation appears compressed in one direction and the states are no longer equally spaced. Noise tolerance is reduced as the states are not at the proper location and likely to be misinterpreted in the presence of additive noise.

Quadrature errors have an even more insidious effect. The actual in-phase and quadrature-phase components are skewed with relation to the desired positions. The probability of error increases as the constellation points are closer to the decision thresholds. Both the phase and amplitude of the transmitted signal are incorrect.

Demodulator alignment

The objective of demodulator alignment is to ensure that the I and Q signals at the demodulator output represent the I and Q signals at the demodulator input.

Accurate test signals with filtering similar to that of the actual system are required. Static modulated signals could be used, but these poorly represent the actual operation of the demodulator. The receiver carrier recovery circuits usually require random signals to maintain lock.

Modulator alignment

For modulator alignment an accurate quadrature demodulator is needed. An accurate modulator source could be used to calibrate out errors in the performance of an imperfect demodulator.

Practical phase and gain testing

The phase and gain error between the I and Q channel outputs of the TDA8040 can be measured as follows:

- The LC oscillator is tuned to $f_{i(VCO)} = 140$ MHz. This results in an internal IF frequency of 70 MHz.
- A sine wave signal $f_{i(RF)} = \frac{1}{2} f_{i(VCO)} + 500$ kHz (70.5 MHz) is applied at the IF input.
- The higher frequencies and mixer products (140.5 MHz) are filtered out by the I and Q channel filters.

A 500 kHz sine wave is expected at the I and Q channel output and should have the following properties:

- The sine waves should be 90° out of phase
- The phase error is defined as the phase quadrature imbalance between the I and Q channel
- The gain error is defined as the gain difference between the I and Q channel

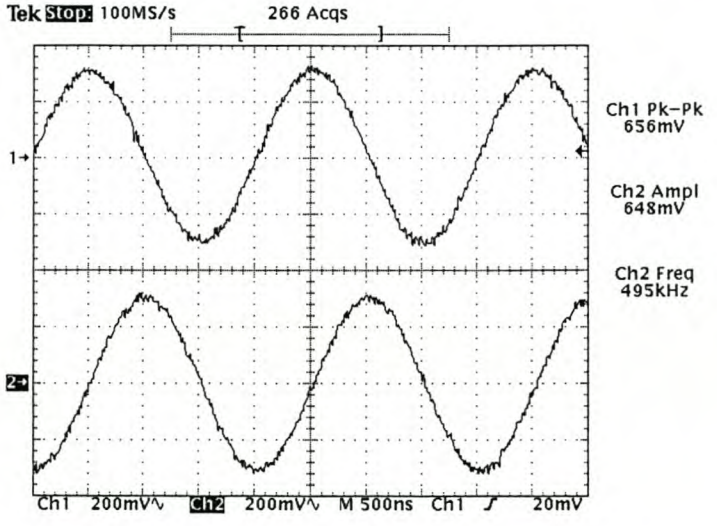


Figure 6.4: Measurement of quadrature demodulator gain and phase.

The measured result of the phase and gain characteristics of the TDA8040 quadrature demodulator are shown in Figure 6.4. The amplitude of both channels are within 0.2 dB of each other. The phase difference between channels is measured to be within one degree of the expected 90°. If the two channels are plotted in a vector diagram format it should represent a circle with no deformation.

This measurement can be made over the entire band of frequencies that the data will occupy. Tilt is defined as the difference between the maximum and the minimum channel gain measured in a frequency band around $f_{i(RF)}$. The specified tilt is the maximum tilt value found in one of the I and Q channels.

6.2.2 Vector and Constellation diagram analysis

The constellation diagram displays how the received I/Q states or symbols looks to the receiver at the sampling instant. A vector diagram shows the transition between these states. These two methods are capable of identifying several types of signal degradation.[1]

Constellation measurements

The statistical analysis of the sampled data of a constellation or vector analyser is possible. The definition of the main parameters measured by these devices is discussed below.

Constellation closure is a measure of the relative RMS cluster size of each channel. The equation is given below with the relevant parameters indicated in Figure 6.5.

$$\text{Closure} = \frac{\text{rms Cluster size}}{0.5 \times \text{Cluster separation}} \times 100 \tag{6.1}$$

The constellation cluster may have unequal spacing or different sizes therefore the mean squared cluster size is used for closure measurement.

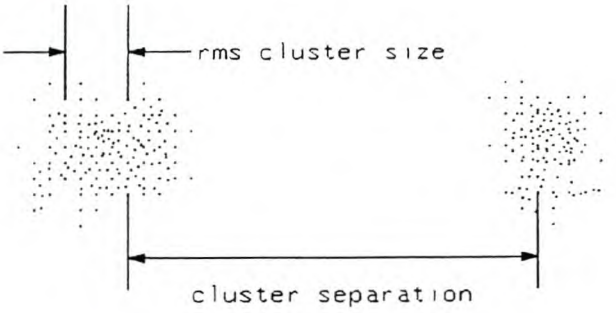


Figure 6.5: Definition of constellation closure [5].

Lock angle error is a measure of the angle of rotation of the constellation. It is defined as the mean of two angles: θ_1, the anti-clockwise angle from the I axis to the cluster lines and θ_2, the anti-clockwise angle from the Q axis to the cluster lines.

The relevant angles used in lock angle error calculation are shown in Figure 6.6. The lock angle error expression is given below:

$$\text{Lock angle error} = \frac{\theta_1 + \theta_2}{2} \tag{6.2}$$

Quad angle error is a measure of the difference from perfect quadrature between the I and Q cluster lines. It is the difference between the two angles θ_l and θ_2 shown in Figure 6.6. Quad angle error is thus defined as:

$$\text{Quad angle error} = \theta_2 - \theta_1 \tag{6.3}$$

[1]The discussion in this subsection is based on Chapter 2 of the HP 3709B constellation analyzer operating manual [5].

A best-fit model is used to line up the clusters of a distorted constellation in order to measure the angles θ_1 and θ_2.

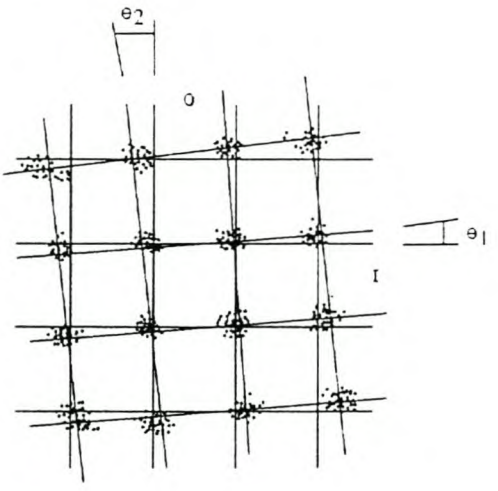


Figure 6.6: Lock and quad angle error determination [5].

RMS non-linear distortion is a measure of the residual distortion after the linear degradations have been calibrated out. It is expressed as the RMS value of the normalized I and Q channel non-linear components.

$$\text{rms Non - lin distortion} = \sqrt{\left(\frac{2 \times I_{non-linear}}{\text{I cluster sep}}\right)^2 + \left(\frac{2 \times Q_{non-linear}}{\text{Q cluster sep}}\right)^2} \tag{6.4}$$

AM - AM distortion is a measure of amplitude related radial compression or expansion of the constellation. Is is defined as:

$$\text{AM - AM} = \frac{\text{Corner cluster radial distortion}}{\text{Corner cluster radius}} \times 100 \tag{6.5}$$

The measured radius is compared against the ideal radius as shown in Figure 6.7. For a linear constellation all the clusters lie on a straight line through the origin. Compression or expansion cause the clusters to curve away from the ideal straight line. The undistorted position of the corner cluster is determined by extrapolating the slope of the curve at the origin.

AM-PM distortion is a measure of the amplitude related rotation of the constellation. It is expressed as:

$$\text{AM - PM} = \text{Corner cluster angle error} - \text{Center angle error} \tag{6.6}$$

The measured angle error of each cluster is plotted against the ideal radius (see Figure 6.8). For a linear constellation all the clusters lie on a horizontal straight line. AM-PM conversion causes the line to slope up or down.

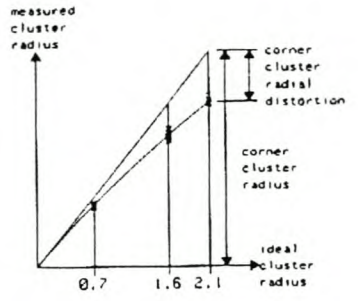


Figure 6.7: AM-AM non-linear distortion [5].

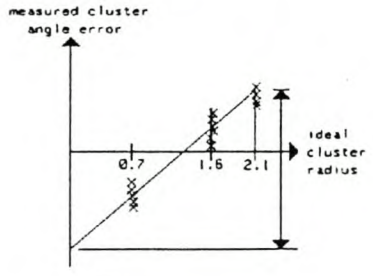


Figure 6.8: AM-PM non-linear distortion [5].

HPA distortion

The distortion due to a high power amplifier (HPA) or other non-linear components operated under conditions where compression takes place is easily identified. The constellation states no longer line-up and the corners of the constellation are rounded off or rotated as shown in Figure 6.9 .

This type of distortion is more visible on a high level QAM constellation than on a PSK constellation since amplitude variations display compression more clearly. The tolerance of PSK to these nonlinearities is one reason why it is used in satellite communications where the HPA is driven particularly hard. Unfortunately this is also where the distortion due to the HPA needs to be identified.

It is possible to artificially produce the amplitude variations necessary to excite amplitude dependent distortions. A constellation diagram will clearly display the amplitude modulation to phase modulation (AM-PM) conversion and compression (AM-AM) due to nonlinearities.

A disadvantage of varying the amplitude artificially is that the receiver require the proper modulation signals to maintain lock. Another problem is that the AGC circuit will track out the effects of amplitude modulation. The AGC needs to be disabled or the amplitude modulation rate applied must exceed the AGC bandwidth.

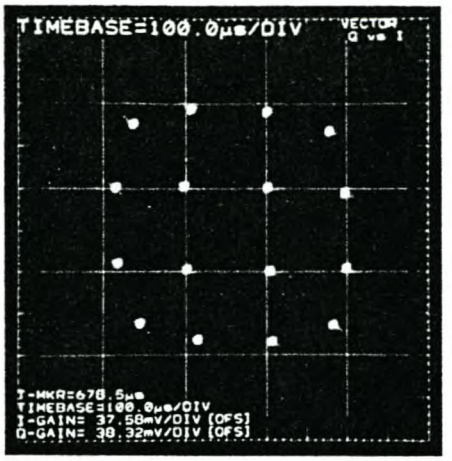


Figure 6.9: 16 QAM constellation with AM-AM and AM-PM non-linearities [5].

I/Q Crosstalk

I and Q modulations are not entirely independent. This is most noticeable in the vector diagram where normal straight line transitions bend and take an oval shape (see Figure 6.10). This is the result when the amplitude of one channel increases but the other channel experiences a small increase as well.

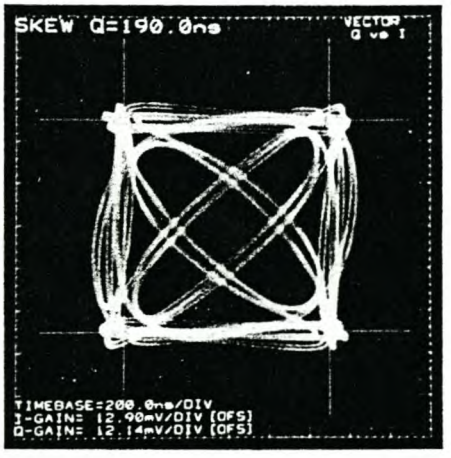


Figure 6.10: QPSK signal with oval transitions indicating I/Q crosstalk [5].

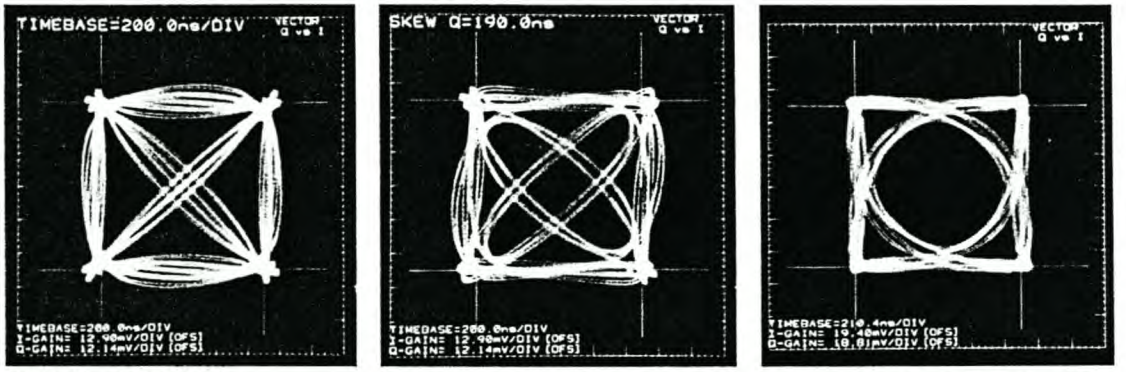
Crosstalk is usually caused by a lack of isolation between the baseband I and Q signals. Amplitude ripple in the IF and RF circuitry of the transmitter, receiver or even the transmission channel could also be a cause.

Crosstalk is a dynamic problem and the effects are more pronounced as the modulation bandwidth is increased. Measurements must therefore be made with representative data rates and bandwidths.

Measuring data skew

Data skew refers to the time difference between the desired switching of the I and Q channels with respect to their actual switching. Skew is introduced by different line lengths in the I and Q channels or a variety of other baseband phenomena. It is generally not caused by IF or RF components.

Skew is an important characteristic as it alters the modulator output during transition times. If skew, as small as a fraction of the symbol period is present, the results look similar to I/Q crosstalk (compare Figure 6.10 with Figure 6.11). Depending on system filtering it may not be possible to determine whether data skew or crosstalk is responsible for the deviation.



QPSK with no I/Q timing offset. *QPSK with ¼ clock period I/Q timing offset.* *QPSK with ½ clock period I/Q timing offset.*

Figure 6.11: QPSK signal with different levels of data skew [5].

Skew effectively shortens the period that the received data is valid. If one channel switches sufficiently later than the other a stable signal state is never achieved, introducing ISI in the received signal.

Systems with nonlinear channels, such as in satellite communications, stagger the I and Q signals intentionally by half a clock period. This is done to avoid large amplitude variations associated with transitions through the center of the vector diagram. No additional data skew or delay is allowed since this will cause larger amplitude variations which excite the nonlinear characteristics of the channel. In terrestrial communication links, degradation due to data skews show up as ISI and eye closure.

Measurement

Data skew is effectively measured on an oscilloscope with a dual trace of the I and Q channel versus time. Provided the rise times are sufficiently high the relative switching time can be measured. Relatively square waveforms are preferred to measure the transition delays accurately.

The optimum eye opening could also be used as a point of reference and compared to the time the other channel takes to reach the maximum opening. This assumes the filter response is the same for both channels.

Another sensitive method to measure skew is to use a vector diagram display. This method is especially useful for filtered signals. With no data skew present straight transitions exist between all signal states. As soon as any skew is present the transitions will deviate from the straight line trajectories.

6.3 DMR performance evaluation

6.3.1 Phase noise in DMR

Every RF or microwave source exhibits some frequency instability. This instability results in unwanted phase modulation of the final signal. The most evident sources are the transmitter LO and the receiver carrier recovery circuits.

Phase noise contributes additional phase modulation and causes rotational jitter in the phase plane. This complicates the detection process and causes additional errors at the receiver. The smearing effect of phase noise on a 16 QAM constellation is shown in Figure 6.12.

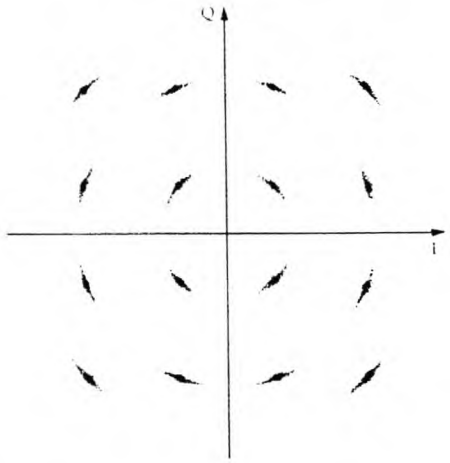


Figure 6.12: 16 QAM signal with phase noise smearing [5].

Phase noise measurements are made in the frequency domain. These measurements contain only energy due to phase noise and residual AM is not measured.

The unit of phase noise $L(f)$ is the ratio of the power in one phase modulation sideband, per Hertz of bandwidth, to the total signal power at an offset frequency, F_M (Hz), away from the carrier. $L(f)$ is presented logarithmically as a spectral density plot of the phase modulation sidebands, expressed in dB relative to the carrier per Hertz (dBc/Hz).

The amount of phase noise of a source is calculated by integrating the $L(f)$ curve over the channel bandwidth (both sidebands if necessary). Only noise outside of the carrier recovery loop bandwidth of the receiver should be integrated since the phase noise within this BW will be tracked out in the detection process.

6.3.2 AGC response testing

Measures of AGC performance are the dynamic range, step response and the AGC transfer function. The functioning of the AGC is tested by varying the amplitude of the received signal and monitoring the AGC control voltage, the I Q baseband signals or the IF signal level after the AGC amplifier.

AGC dynamic range is tested by applying a modulated test signal to receiver input and adjusting the amplitude while observing the baseband I and Q signals. When the limit of the dynamic range is reached the I and Q signal levels will begin to vary in amplitude with the variations in the test signal amplitude.

To test the loop step response a test signal within the AGC bandwidth and dynamic range must be applied to the receiver input. Amplitude variations result due to the AGC step response and show up as amplitude variations of the I- and Q-channel signals or AGC control voltage.

6.3.3 Doppler shifts

Doppler shift results when either transmitter or receiver moves relative to the other. In a satellite application the transmitter and receiver are great distances apart and move rapidly with respect to each other. Frequency shift experienced due to Doppler cause the modulated signal to experience a phase rotation. If the carrier recovery circuits do not track out these phase changes the signal will not be detected correctly and the loop can lose lock.

Measurement of Doppler shift

Doppler shifts at S-band frequency have peak deviations on the order of 60 kHz and vary at a rate in the order of 1 kHz/s or lower (as was shown in Figure 1.5). The effects of Doppler shift can be simulated by gradually varying the frequency at the receiver input.

As a test the modulator carrier frequency is varied with a 60 kHz deviation at a rate of 1 kHz/s. The measured result in Figure 6.13 shows that the carrier recovery loop follows the received carrier deviation with no delay. The top trace shows the control signal to the modulator VCO and the bottom trace shows the output of the carrier recovery loop filter.

6.4 Implementation loss measurement

Implementation loss is the fundamental measurement of digital radio performance. The implementation loss of a demodulator is defined as the difference between the theoretical Eb/No required and the practical measured Eb/No for a given bit error rate.

6.4.1 Bit error rate

BER (bit error rate) is defined as the average number of bits in error divided by the number of bits transmitted. This is an appropriate measure for a system whose primary function is the accurate communication of digital data.

It is possible to observe BER under a variety of degrading operating environments. These include the addition of gaussian noise (carrier-to-noise (C/N)[2]) and sinusoidal interference (carrier-to-interference (C/I)) tests respectively.

[2]The value of Eb/No can be calculated if the carrier to noise power is known using the relation: $Eb/No = C/N \times B/R$, where B is the equivalent noise bandwidth and R is the bitrate.

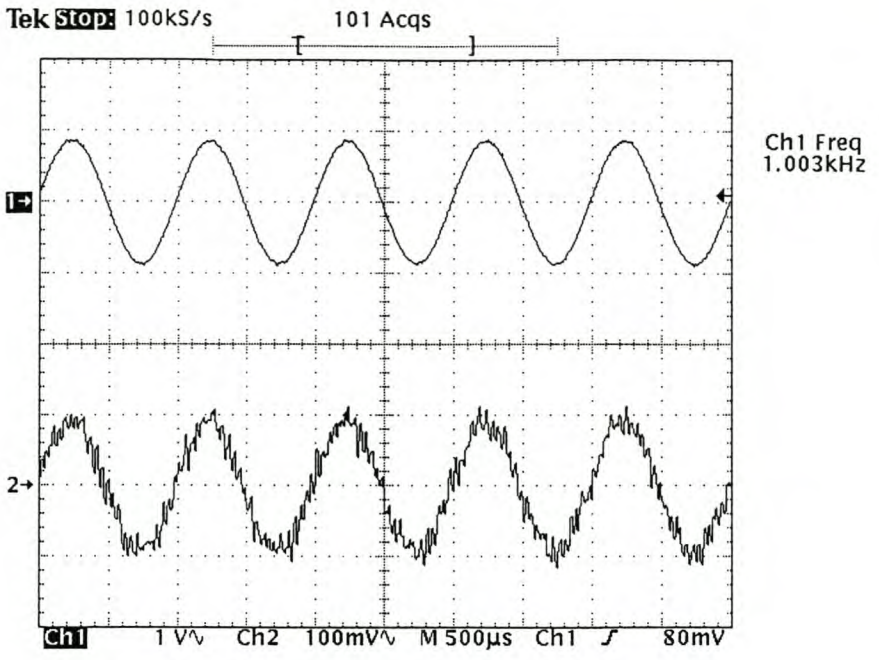


Figure 6.13: Worst case Doppler shift simulation.

Causes of errors are misaligned modulator states and demodulator decision thresholds, power amplifier non-linearity, thermal noise and phase noise on the recovered carrier and clock. BER tests will degrade due to these, but will provide no information as to which causes are responsible for the effects. IF back-to-back and RF back-to-back tests are possible to isolate the amount of degradation due to RF components.

A pseudo-random binary-sequence (PRBS) is used to drive the modulator. A CCITT pattern such as $2^{15} - 1$ for low bitrates and $2^{23} - 1$ for higher bitrates (140 Mb/s and up) is recommended. An error detector synchronizes on the demodulated PRBS and compares this bit-by-bit to the reference PRBS. A pseudo-random data stream should be used even if scrambling or data modifying circuits are used. Modem frequency response errors do not necessarily show when using patterns with short repetition rates.

For statistically meaningful answers, it is desirable to count at least 100 errors in a measurement period. An interfering signal can be added to introduce a controlled amount of eye closure. The increased BER is then measured and the true background BER estimated. A considerable amount of measurement time is saved in this manner [11].

6.4.2 Noise generation techniques

Two methods are available to generate the required noise levels for BER testing:

- A fade simulation using an attenuator to decrease the incoming signal level.
- Additive noise method using a noise generator to add noise to the incoming signal.

The additive noise method is preferred as the digital receiver operates at normal unattenuated levels and the receiver noise figure is negligible. The possibility of synchronization

loss is minimized since the AGC, amplifiers and other components of the receiver all operate at nominal levels. The carrier-to-noise ratio is accurately known and the BER can be checked using a pattern generator and error detector.

Practical implementation loss measurement

Due to lack of wideband noise sources the additive noise method could not be used. To reduce the received Eb/No an attenuator is used to lower the received signal strength. A variable gain amplifier is then used to compensate for the lower signal level. In this manner the signal as well as the noise level is increased. The setup used to reduce the SNR ratio is illustrated in Figure 6.14.

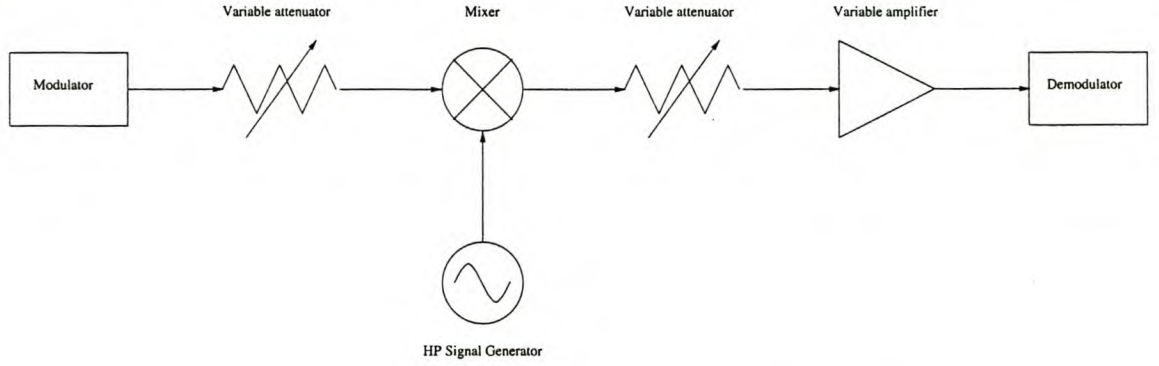


Figure 6.14: Implementation loss measurement setup.

The signal and noise power is measured at the output of one of the channel filters using a HP power meter. A high speed buffer amplifier (Harris/Intersil HA-5002) is used to prevent loading of the filter by the power meter. The signal and noise power measurement setup is shown in Figure 6.15.

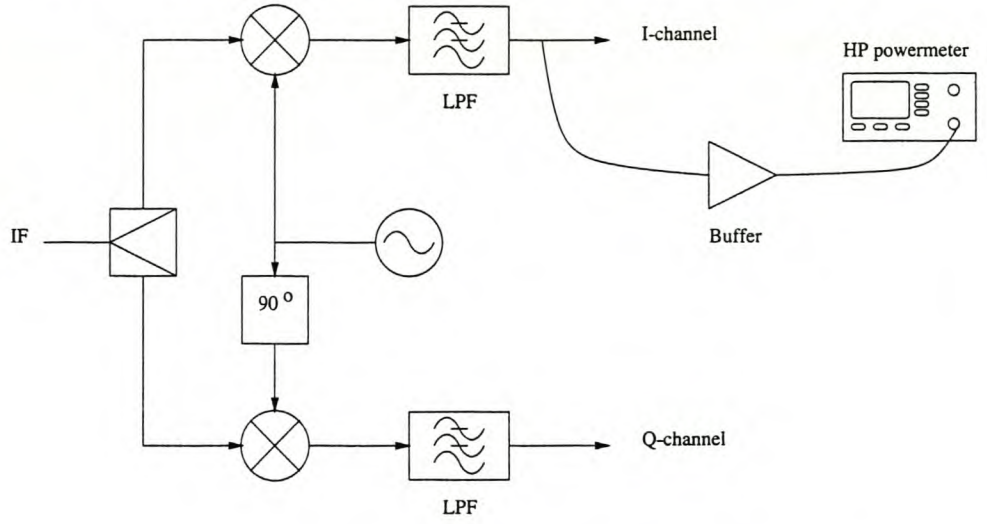


Figure 6.15: Signal and noise power measurement setup.

The Eb/No for each attenuator setting is determined by first measuring the signal and then the noise power. The measured value is in actual fact the signal-plus-noise to noise

ratio which is first converted to a SNR ratio. This ratio is then converted to Eb/No by multiplying with the effective noise bandwidth over datarate.[3]

When the modulation is removed from the signal to measure the noise power, the recovery and control circuits attempt to compensate for the signal loss. The AGC amplifier is therefore removed from the signal path to prevent it rectifying the signal and noise levels. The correct signal level has to be maintained manually to ensure the demodulator is input with the correct signal level.

A block of data is captured using the capture hardware (see Section 5.2.3) and is then checked offline for errors using software. This is a time consuming method and a realtime measurement using a BER-meter or custom logic would be ideal.

Measurement
A demodulator implementation loss in the order of 1 dB at a BER of 10^{-4} is considered admissible. This implies that the demodulator Eb/No must be measured with a precision much better than 1 dB. Accurate measurement of the signal and noise power is found to be difficult due to the noisy test environment.

Three different measurements are compared to the theoretical case in Figure 6.16. The implementation loss can be seen to be in the order of 2 dB . The accurate measurement of the implementation loss is difficult especially at low Eb/No. This measurement is dependent on the signal level input as well as the amplifier gain.

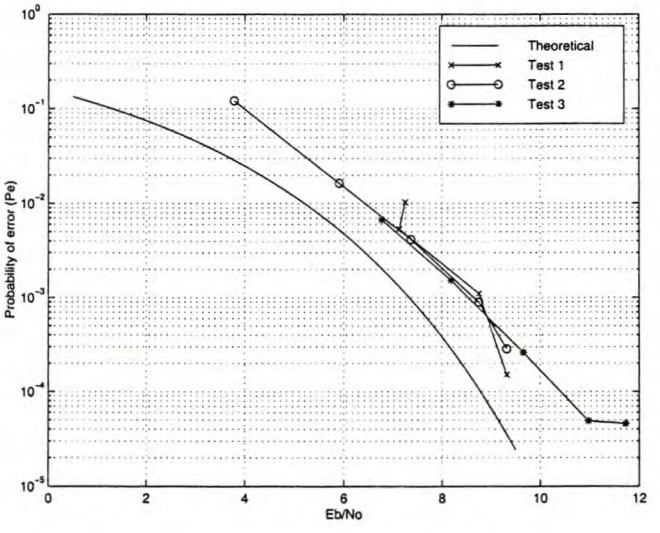


Figure 6.16: Measurement of BER using direct measurement.

Lock detect indicator

The lock indicator of the TDA8041 demodulator controller provides an indication of the received Eb/No. The relation between Eb/No and the lock indicator voltage is given in the TDA8041 application note [1].

[3]Since the datarate in one channel is 20 MHz and the equivalent noise bandwidth of the channel filter is just less than 20 MHz the SNR is approximately equal to the Eb/No ratio.

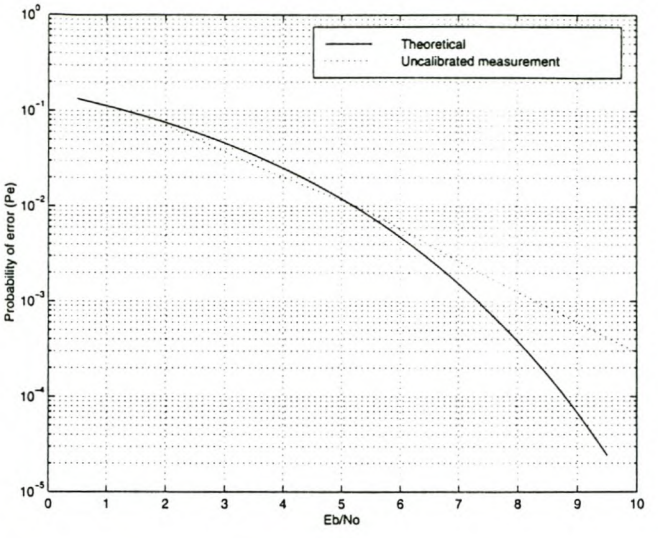


Figure 6.17: Measurement of BER using lock indicator.

Practical results obtained using the lock indicator output is shown in Figure 6.17. This relation is dependent on the demodulator hardware and needs to be calibrated for each hardware configuration. AGC is needed to maintain proper input levels to the AD converters. The lock indicator only functions properly if the input signal is at the correct level and free from distortion.

Calibrating the lock detect output is not possible without an accurate measurement of the Eb/No at a given BER. For antenna tracking the uncalibrated analogue output should be sufficient.

Chapter 7

Conclusions

This thesis has described how a fixed QPSK demodulator for the Sunsat 1 S-band downlink was developed and tested. The implementation loss of the demodulator was measured to be less than 2 dB. This chapter concludes the work by describing some causes of difficulty in the development and suggesting additional work, improvements and future research.

7.1 Development difficulties

The development of the fixed bitrate QPSK demodulator proved to be very challenging for the following reasons:

- Development and characterising of a QPSK demodulator without specialized test and measurement equipment proved to be difficult. The only 40 Mbit/s QPSK source available was the QPSK modulator developed for Sunsat. It took a number of months to discover that data was inducing incidental phase modulation of the microwave carrier, and that this, and not the QPSK demodulator was the cause of poor eye diagrams. Time and effort was thus spent in improving the demodulator while the modulator was at fault.
- Breadboard and prototype construction of 'baseband' circuits which operate in the VHF region are troublesome. PCB layout and manufacture is not always practical during development as it is costly and time consuming. The use of surface mount technology for the high frequency analogue circuitry presented a great improvement in noise performance.
- Shielding of the high-speed decoding logic from the sensitive analogue IF sections presented a significant problem.[1] Shielding is also cumbersome to test and measurement during the development phase.
- The choice of generating QPSK at 2.25 GHz instead of at the carrier frequency of the demodulator significantly complicated testing. The difficulties of screening and isolating signal sources from modulation-dependent impedances, and of down-converting wideband signals added unwanted uncertainties to tests.

[1] During RFI/EMI testing of the Sunsat 1 VHF and UHF trays on an adjacent workbench the FPGA logic signals were competing with switching regulators on the trays itself.

7.2 Additional work

Certain problems encountered identified the following problem areas where additional work is suggested:

- A good stable local oscillator with low phase noise is essential for the downconverter. Neither the ZS6AXT nor the ZCOMM VCO based local oscillators could compare to the HP signal generator.
- Currently the highest bandwidth 70 MHz IF SAW filters available are about 40 MHz. If a higher data rate and thus higher bandwidth is required a higher IF such as 140 MHz should be used.
- The HP IVA-05208 AGC amplifier was selected because of its usage in similar applications. Similar AGC amplifiers in integrated circuit form have become available with positive slope gain control voltage curves. Positive slope gain control will eliminate the need for an additional inverting opamp between the AGC control output and the AGC amplifier.
- The use of the MaxPlus EPF8282ALC84 FPGA allow room for experimentation during development but is excessive for the current decoding logic as only 37% of the logic address blocks are used.
- The FPGA decoding logic and dataclock oscillator PCB can be combined and improved. The use of surface mount technology and proper PCB layout with a solid ground plane and good grounding is suggested.
- The use of low voltage differential signalling (LVDS) for transmission of high speed digital signals between systems is suggested. LVDS was tested between demodulator and the capture hardware and showed a decrease in noise levels as well as reduced loading of the decoding logic FPGA outputs.
- Further screening of the analogue IF stages from the digital stages is necessary. It is suggested that the analogue IF stages be housed in a physically separate enclosure from the digital stages.
- Integration of the demodulator into the Sunsat 1 groundstation still needs to be done.

7.3 Improvements

Problems that were encountered in the demodulator system showed shortcomings in the modulator as well as demodulator systems. The following improvements are suggested:

- The image data format needs careful design to allow the demodulator to synchronize effectively to the line information received in the datastream. This format should be able to incorporate other high volume data sources such as GPS data.

- An initialization sequence is foreseen where a number of flags or headers are transmitted as soon as the QPSK modulator is switched on. The transmission of the flags ceases as soon as data is input to the modulator.
- Both the UHF and S-band QPSK modulators have one fixed frequency local oscillator. Additional oscillator sources should be available for redundancy. The local oscillator of the S-band QPSK modulator on Sunsat 1 failed rendering the S-band QPSK link useless.
- Preferably the local oscillator of the modulator should be synthesized allowing a suitable (i.e. noise and interference free) part of the downlink band to be used. This is learned from the amount of terrestrial interference on the Sunsat 1 UHF QPSK downlink.
- LVDS is suggested for the connection of the clock and data signal between the ramtray and QPSK modulators. Currently the digital signals are output directly from TTL buffers to the FPGA inputs using coaxial cable.

7.4 Future research

The increasing need for higher datarates is driving the move to higher bands for satellite communications where more relative bandwidth is available. X-band is seen as the next logical step for Sunsat micro-satellite high datarate downlinks.

Forward error correction (FEC) codes and Viterbi coding should be investigated for use in future demodulators to add robustness and reliability to the highspeed downlink.

Local knowledge and experience has been gained in high-speed digital microwave radio against which future work can be evaluated. The development of test equipment related to high-speed digital communications is envisioned. Local capacity building in the area of wideband digital microwave radio is foreseen.

Bibliography

[1] F. van Amesfoort and R. van der Wal, "Application note AN95053: QPSK/BPSK demodulator chipset: TDA8040 and TDA8041." Philips Electronics N.V., May 1995.

[2] F. M. Gardner, "Properties of frequency difference detectors," *IEEE Transactions on Communications, Vol. COM-33, No. 2*, February 1985.

[3] F. M. Gardner, "A BPSK/QPSK Timing-error detector for sampled receivers," *IEEE Transactions on Communications, Vol. COM-34, No. 5*, May 1986.

[4] R. van der Wal and L. Montreuil, "QPSK and BPSK demodulator chipset for satellite applications," *IEEE Transactions on Consumer Electronics, Vol. 41, No.1*, February 1995.

[5] "Operating Manual: HP 3709B Constellation analyzer." Hewlett-Packard Limited: Manual Part Number: 03709-90001, August 1987.

[6] J. P. Costas, "Synchronous Communications," *Proc. IRE, Vol. 44*, December 1956.

[7] H. C. Osborne, "A generalized 'Polarity-Type' Costas Loop for Tracking MPSK Signals," *IEEE Transactions on Communications, Vol. COM-30, No.10*, October 1982.

[8] H. Sari and S. Moridi, "New Phase and frequency detectors for Carrier recovery in PSK and QAM Systems," *IEEE Transactions on Communications, Vol. COM-36, No. 9*, September 1988.

[9] G. W. Milne, "Analogue and digital television modulation techniques," Master's thesis, University of Stellenbosch, 1973.

[10] F. M. Gardner, *Phaselock Techniques, Second Edition.* John Wiley & Sons Inc., 1979.

[11] T. McDermott, *Wireless digital communications: Design and Theory.* Tucson Amateur Packet Radio Corporation, 1996.

[12] "Digital Modulation in Communication Systems - An Introduction." Hewlett-Packard Limited: Application Note 1298, 1997.

[13] G. W. Milne, "QPSK modulator/demodulator filter simulation," Tech. Rep. DCI 5.140/6, ESL internal document, University of Stellenbosch, January 1995.

[14] A. I. Zverev, *Handbook of Filter Synthesis.* John Wiley and Sons Inc., 1967.

[15] "Altera Max+Plus II VHDL." Altera Corporation, November 1995.

[16] "Altera Flex 8000 Handbook." Altera Corporation, May 1994.

[17] C. R. Cahn, "Improving Frequency Acquisition of a Costas Loop," *IEEE Transactions on Communications, Vol. COM-25, No. 12*, December 1977.

[18] J. Carr, "Crystals made clear II," *Wireless World*, October 1999.

[19] R. E. Collin, *Antennas and Radiowave Propagation.* McGraw Hill Inc., 1985.

[20] S. S. Haykin, *An introduction to analog and digital communications.* John Wiley & Sons Inc., 1989.

[21] N. D. James, "A digitally implemented QPSK modem operating at up to 10 Mbit/s," *GEC Journal of Research, Vol. 7, NO.1*, 1989.

[22] W. J. Larson and J. R. Wertz, eds., *Space mission analysis and design.* Microcosm Inc. and Kluwer Academic Publishers, Second ed., 1992.

[23] G. Maral and M. Bousquet, *Satellite communications systems: Systems, Techniques and Technology.* Wiley, 1993.

[24] D. G. Messerschmitt, "Frequency Detectors for PLL Acquisition in Timing and Carrier Recovery," *IEEE Transactions on Communications, Vol. COM-27, No. 9*, September 1979.

[25] G. M. Miller, *Modern electronic communication.* Prentice Hall Inc., 1993.

[26] R. J. Murray and P. D. White, "Surface acoustic wave devices," *Wireless World*, March/April 1981.

[27] S. H. Mumford, W. W, *Noise performance factors in communications systems.* Horizen House-Microwave, 1968.

[28] G. Nash, "Phase-locked loop design fundamentals." Application note AN-535, Motorola Communications Device Data, 1995.

[29] F. D. Natali, "AFC Tracking Algorithms," *IEEE Transactions on Communications, Vol. COM-32, No. 8*, August 1984.

[30] T. Noguchi, Y. Daido, and J. Nossek, "Modulation techniques for microwave digital radio," *IEEE Communications Magazine, Vol. COM-24, No.10*, October 1986.

[31] J. J. Roux, "The Design of a VHF and UHF Receiver Front-end for the Sunsat Microsatellite," Master's thesis, University of Stellenbosch, January 1998.

[32] F. G. Stremler, *Introduction to communications systems, Third Edition.* Addison-Wesley, 1990.

[33] P. C. L. Yip, *High-frequency Circuit Design and Measurements.* Chapman & Hall, 1990.

[34] P. H. Young, *Electronic communications Techniques, Third Edition.* Macmillan Publishing Company, 1994.

[35] "Vector modulation measurements: Measurements for digital microwave radio." Hewlett-Packard Limited: Application Note 343-1, November 1986.

Appendix A

Calculation of required bitrate for realtime download of square imager pixels.

```
!

%Description: Calculation of required bitrate for images to have square pixels
%Author:      L.C. Schwardt
%Date:        1999/06/01
%Revisions:   P.P.A. Kotze

%init.
close all;
clear all;

%define constants
Re=6378000;                                 %Mean radius of earth
ra=Re+850000;                               %apogee
rp=Re+650000;                               %perigee

%orbit mechanics
%(simple elliptical orbit)
a=(ra+rp)/2;                                %semi-major axis
e=(ra-rp)/(ra+rp);                          %semi-minor axis
theta=0:359;                                %true anomaly
thetarad=pi*theta/180;                      %converted to radians
r=a*(1-e*e)./(1+e*cos(thetarad));           %radial distance/orbital radius
mu=3.986e14;                                %gravitational parameter
v=sqrt(mu*(2./r-1/a));                      %orbital velocity

%bitrate calculations
pw=(r-Re)*10.7e-6/0.56;                     %pixel width pw/h=p/f
ppl=3490;                                   %pixels per line
bpp=24;                                     %bits per pixels
BR=bpp*ppl*v./pw;                           %BR bit rate

figure(1);
plot(BR/1e6);grid;
axis([0 360 36 54])
xlabel('True anomaly []');
ylabel('Bitrate [Mb/s]');
print -deps c:\tesis\doc\images\bitrate.eps

!

diary off
```

Appendix B

Calculation of Doppler shift and rate of Doppler shift.

```
!

%\begin{verbatim}
%Description:  Calculation of doppler shift and doppler shift rate for S-band
%Author:       P.P.A. Kotze
%Date:         1999
%Revisions:    -

%Init.
close all
clear all
format compact

%Fixed parameters of comms link
c = 299.792e6;                  %speed of light in vacuum
M = 5.98e24;                    %Mass of earth [kg]
G = 6.6725985e-11;              %Universal gravitational constant [N.m^2/kg^2]
%from "Physics for scientists and engineers" - Serway

% Centripal force:              Fc=m.v^2/r
% Gravitational force:          Fg=Gm.M/R^2
% Tangential velocity:          v=sqrt(G.Me/R)
% from "Introduction to physics for scientists and engineers" F. J. Bueche

flink=2.25e9;                   %frequency of comms link
lambda=c/flink;                 %wavelength

%Define elevation of satellite
elev1 = linspace(0,pi,180);     %calculate as function of sat elevation
elev = elev1(1:180);            %sweep elevation from 1 to 90 degrees
rsat=820e3;                     %height of satellite at apogee
rsatmin=650e3;                  %820k apogee - 650k perigee
rearth=6378.4e3;                %radius of earth

%angle between sat-to-station and sat-to-ground beneath
%sine rule approach
teta_sat = asin(rearth*(sin(pi/2+elev)/(rearth+rsat)));

%angle between earthcentre-to-sat and earthcentre-to-station
teta_earth = pi/2 - teta_sat - elev;

%straight distance between station and sat
rslant = (rearth+rsat)*sin(teta_earth)./sin(pi/2+elev);

vmax = sqrt(G*M/(rearth+rsatmin));
                                %maximum tangential velocity at min height
                                %use this for worst case doppler shift
vmin = sqrt(G*M/(rearth+rsat));  %minimum tangential velocity at max height
```

```
vmed = (vmax+vmin)/2;              %average tangential velocity
rsatmed = (rsat+rsatmin)/2;        %average satellite height

vrel=vmax.*cos(pi/2-teta_sat);     %relative velocity between sat and ground
                                   %velocity tangential comp. in sat direction
                                   %[m/s]
dopshift=vrel/c*flink;             %shift = Sat.freq * Rel.velocity / c [Hz]

timerate=2*pi*(rearth+rsatmed)/vmed;
                                   %average time for whole orbit;
                                   %assume satellite mid-range circular orbit

eqtime=timerate/360;               %seconds / degree (angle from earth centre)

elev_time=(-teta_earth+max(teta_earth))/pi*180*eqtime;
                                   %convert to time for elevation angle
                                   %seconds for diff elev.
% *** Graphical output ***


figure;
%subplot(311);
%plot(elev(1:180)/pi*180-90,vrel(1:180))
%title('Relative velocity between satellite and groundstation')
%xlabel('Elevation [deg]')
%ylabel('Relative velocity [m/s]')
%grid
subplot(211);
plot(elev_time,dopshift/1000)
%title('Doppler shift vs time')
xlabel('Time [s]')
ylabel('Doppler shift [kHz]')
grid;
subplot(212);
plot(elev_time,diff([dopshift(1) dopshift]))
%title('Doppler shift rate vs time')
xlabel('Time [s]')
ylabel('Rate of doppler shift [Hz/s]')
grid
print -deps c:\tesis\doc\images\dopboth2.eps

!

diary off
```

Appendix C

Calculation of demodulator loop components

C.1 Calculation of clock recovery filter components

```
!

%Description: Calculation of clock recovery PLL loop component values
%             for 40Mbit datarate, check for 25Mbit standard and 52Mbit max.
%             AN95053 refers to the Philips application note reference number.
%             Add loop frequency, bandwidth and impulse response
%Author:      P.P.A. Kotze

%init.
clc;
close all;
clear all;
format compact;
echo on;

%Computation of loop components for standard datarates
datarate=[25 40 52]*1e6;                %compute for standard datarates [MHz]
                                        %40 Mbit/s default bitrate
dfosc=2*datarate*0.0001                 %2*100 ppm of datarate
dfosc =
        5000        8000       10400
dwosc=2*pi*dfosc                        %2*pi*f of datarate in hertz
dwosc =
  1.0e+004 *
    3.1416    5.0265    6.5345

KO=dfosc/3.8                            %VCXO constant over 3.8V (4V)
KO =
  1.0e+003 *
    1.3158    2.1053    2.7368
Ko=2*pi*KO                              %convert KO to rads/s/V
Ko =
  1.0e+004 *
    0.8267    1.3228    1.7196
Kd=42e-6                                %phase constant Kd, given in AN59053
Kd =
  4.2000e-005
K=Ko*Kd                                 %calculate open loop gain K
K =
    0.3472    0.5556    0.7222

B=1.3                                   %damping factor, chosen ROT
B =
    1.3000
```

```
%loop bandwidth
BWhz=dfosc*1.5                          %use *1.5 ROT for safety
BWhz =
        7500       12000       15600
BWrads=2*pi*BWhz                        %convert to rad/s
BWrads =
  1.0e+004 *
    4.7124    7.5398    9.8018
fn=BWhz/2/B                             %PLL natural frequency Hz
fn =
  1.0e+003 *
    2.8846    4.6154    6.0000
wn=2*pi*fn                              %PLL natural frequenct rad/s
wn =
  1.0e+004 *
    1.8125    2.8999    3.7699

%Calculate PLL component values
R=BWrads./K                             %Loop filter resistor value
R =
  1.0e+005 *
    1.3571    1.3571    1.3571
C=(4*B^2)./(K.*R.^2)                    %Loop filter capacitor value
C =
  1.0e-008 *
    0.1057    0.0661    0.0508

%check calculated values
wn=sqrt(K./C), B=R.*C/2.*wn, fn=wn/2/pi
wn =
  1.0e+004 *
    1.8125    2.8999    3.7699
B =
    1.3000    1.3000    1.3000
fn =
  1.0e+003 *
    2.8846    4.6154    6.0000

%choose resistor value, check wn
R=120e3
R =
      120000
C=(4*B.^2)./(K.*R.^2)
C =
  1.0e-008 *
    0.1352    0.0845    0.0650

wn=sqrt(K./C), B=R.*C./2.*wn, fn=wn/2/pi
```

```
wn =
  1.0e+004 *
    1.6026    2.5642    3.3334
B =
    1.3000    1.3000    1.3000
fn =
  1.0e+003 *
    2.5506    4.0810    5.3053

%choose capacitor value, check wn
C=[1.2e-9 .820e-9 650e-12]
C =
  1.0e-008 *
    0.1200    0.0820    0.0650
wn=sqrt(K./C), B=R.*C./2.*wn, fn=wn/2/pi
wn =
  1.0e+004 *
    1.7011    2.6029    3.3334
B =
    1.2248    1.2806    1.3000
fn =
  1.0e+003 *
    2.7073    4.1427    5.3052

%PLL characteristics
%Loop bandwidth
w3db=wn.*sqrt((1+2*B.^2+sqrt(2+4*B.^2+4*B.^4)))
w3db =
  1.0e+004 *
    4.8482    7.6666    9.9292
f3dB=w3db/2/pi
f3dB =
  1.0e+004 *
    0.7716    1.2202    1.5803

%Noise performance [rad/s]
BL=pi*wn.*(B + 1/4./B)
BL =
  1.0e+005 *
    0.7636    1.2069    1.5628
BLf=BL/2/pi
BLf =
  1.0e+004 *
    1.2153    1.9208    2.4872

%Loop parameters for 40 Mbit/s data rate
B=B(2);
wn=wn(2);
```

```
%Calculation of loop transfer function
num=[2*B*wn wn^2];
den=[1 2*B*wn wn^2];

%Calculation of loop frequency response
stp=1;                                  %Step size
w=2*pi*[0:stp:100]*1e3;                 %Setup frequency range
[m,p,w]=bode(num,den,w);                %Calculate frequency response

%Calculate the effective noise bandwidth numerically
neb=(sum(m.^2))./(m(1).^2)*stp*1e3
neb =
  1.8590e+004

% *** Graphical output ***

%Plot frequency response of loop
figure;
subplot(211);
plot(w/2/pi/1e3,20*log10(m));
grid;
xlabel('Frequency [kHz]');
ylabel('Amplitude [dB]');
axis([0 100 -20 2])
subplot(212);
plot(w/2/pi/1e3,p);
grid;
xlabel('Frequency [kHz]');
ylabel('Phase []');

%Plot impulse response of loop
figure;
impulse(num,den)

!

diary off
```

C.2 Calculation of carrier recovery filter components

```
!

%\begin{verbatim}
%Description:    Sunsat carrier recovery loop calculations
%               40 Mbit data rate design check at 25Mbits/52Mbits
%               Add filter responses, bandwidth, impulse response
%Author:         P.P.A. Kotze
%Date:           4 April 1998
%Revision:       30 September 1998

%init.
clc;
close all;
clear all;
format compact;

%Carrier recovery
fd=[25e6 40e6 52e6]                 %data rates 40 Mbits, 25Mbit and 52Mbit max.
fd =
    25000000    40000000    52000000
fs=fd/2                             %symbol rate half datarate
fs =
    12500000    20000000    26000000
dfcext=5e6                          %Sunsat practical measured VCO freq range
dfcext =
     5000000

dfc=dfcext/2                        %divide by two to get internal freq range
dfc =
     2500000
dwc=2*pi*dfc                        %convert VCO range to rad/s
dwc =
  1.5708e+007
Ko=dwc/3.8                          %VCO constant [rad/s/V]
Ko =
  4.1337e+006

%Kd=64e-6                          %worst case operation [fig 21 an95053]
                                    %for Eb/No=5dB Kd=64  [uA/rad]
Kd=100e-6                           %no/little noise
Kd =
  1.0000e-004
                                    %for Eb/No=10dB Kd=116 [uA/rad]
                                    %Kd constant depend Eb/No [AN95053 p37]

K=Ko*Kd                             %combined loop gain
```

```
K =
  413.3675

B=1                                    %Sunsat value chosen ROT
B =
     1
fn=fs/1000                             %fn chosen approx. 10 kHz
fn =
       12500       20000       26000
                                       %choose factor 1/1000 ROT AN95053 p.39
wn=2*pi*fn                             %convert to rad/s
wn =
  1.0e+005 *
    0.7854    1.2566    1.6336

C=K./wn.^2                             %Calculate capacitor value
C =
  1.0e-007 *
    0.6701    0.2618    0.1549
R=2*B./(C.*wn)                         %Calculate resistor value
R =
  380.0000  608.0000  790.4000

%Calculate with physical values
C=[68e-9 22e-9 15e-9]                  %choose physical capacitor
C =
  1.0e-007 *
    0.6800    0.2200    0.1500

%check PLL parameters with capacitor value
wn=sqrt(K./C),B=R.*C./2.*wn,fn=wn/6.28
wn =
  1.0e+005 *
    0.7797    1.3707    1.6601
B =
    1.0073    0.9168    0.9841
fn =
  1.0e+004 *
    1.2415    2.1827    2.6434

R=2.*B./(C.*wn)                        %calculate corresponding resistor
R =
  380.0000  608.0000  790.4000
R=[390 680 820]                        %choose physical resistor
R =
   390   680   820

%check PLL parameters with physcial component values
```

```
wn=sqrt(K./C),B=R.*C./2.*wn,fn=wn/6.28
wn =
  1.0e+005 *
    0.7797    1.3707    1.6601
B =
    1.0338    1.0253    1.0209
fn =
  1.0e+004 *
    1.2415    2.1827    2.6434

%PLL characteristics
%Loop bandwidth
w3db=wn.*sqrt((1+2*B.^2+sqrt(2+4*B.^2+4*B.^4)))
w3db =
  1.0e+005 *
    1.9772    3.4575    4.1757
f3dB=w3db/2/pi
f3dB =
  1.0e+004 *
    3.1468    5.5028    6.6459

%Noise performance [rad/s]
BL=pi*wn.*(B + 1/4./B)
BL =
  1.0e+005 *
    3.1246    5.4653    6.6015
BLf=BL/2/pi
BLf =
  1.0e+005 *
    0.4973    0.8698    1.0507

%Loop parameters for 40 Mbit/s data rate
R=R(2);
C=C(2);
B=B(2);
wn=wn(2);

%Calculation of loop transfer function
num=[2*B*wn wn^2];
den=[1 2*B*wn wn^2];

%Alternative calculation of loop tranfer function
num2=[0 K*R K/C];
den2=[1 R*K K/C];

%Calculation of loop frequency response
stp=1;                              %Step size
w=2*pi*[0:stp:400].*1e3;            %Setup frequency range
```

```
[m,p,w]=bode(num,den,w);            %Calculate frequency response

%Calculate the effective noise bandwidth numerically
neb=(sum(m.^2))./(max(1).^2)*stp*1e3
neb =
  8.2496e+004

% *** Graphical output ***

figure;
subplot(211);
plot(w/2/pi/1e3,20*log10(m));
grid;
xlabel('Frequency [kHz]');
ylabel('Amplitude [dB]');
axis([0 100 -20 2])
subplot(212);
plot(w/2/pi/1e3,p);
grid;
xlabel('Frequency [kHz]');
ylabel('Phase []');

%Plot impulse response of loop
figure;
impulse(num,den)

!
```

diary off

C.3 Calculation of VCO tank parameters

```
!

%Description:  Calculation of VCO tank circuit parameters
%Author:       P.P.A. Kotze
%Date:         1998

%Init: start with a clean slate
format compact;
clear all;
close all;

%Mimimum Q>4 [An95053 Philips app. note]
%Max Q => less phase noise
%An95053 uses Q=5 vs. Plessey uses Q=10+

%Calculation of all capacitance in loop
Cvari=[22:50]*1e-12; %BB809 varactor Philips 0-5V reverse voltage
Cv1=39e-12;
Cv2=39e-12;
Ctot=1./(2./Cvari + 2./Cv1);
Ctrim=11e-12; %Trimcap: 4.5-20pF midrange 13pF
Cc=39e-12;
Cx=Ctot+Ctrim+Cc;

%Chip inductor in loop, air core coils pick up noise
L=22e-9;

%Resonant frequencies for diff. reverse voltage
f=1/2/pi./sqrt(L.*Cx)
f =
  1.0e+008 *
  Columns 1 through 7
    1.4208    1.4183    1.4159    1.4136    1.4114    1.4092    1.4071
  Columns 8 through 14
    1.4051    1.4032    1.4013    1.3995    1.3977    1.3960    1.3943
  Columns 15 through 21
    1.3927    1.3912    1.3896    1.3882    1.3867    1.3853    1.3840
  Columns 22 through 28
    1.3827    1.3814    1.3801    1.3789    1.3777    1.3766    1.3755
  Column 29
    1.3744

%Pulling range of VCO ( range/2 for internal range)
pulling_range=max(f)-min(f)
pulling_range =
  4.6474e+006
```

```
%Q of VCO at diff. reverse voltage
Q=220*sqrt(Cx/L)
Q =
  Columns 1 through 7
   11.2014   11.2212   11.2402   11.2587   11.2765   11.2938   11.3105
  Columns 8 through 14
   11.3268   11.3425   11.3578   11.3726   11.3869   11.4009   11.4145
  Columns 15 through 21
   11.4277   11.4405   11.4530   11.4652   11.4770   11.4885   11.4998
  Columns 22 through 28
   11.5107   11.5214   11.5318   11.5419   11.5519   11.5615   11.5710
  Column 29
   11.5802

%Plot the frequency vs. control voltage
RevVoltage=[0 1 2 3 4 5];

DiodeCap=[50 42.5 34.5 29 25 22]*1e-12;
Ctot=1./(2./DiodeCap + 2./Cv1);
Cx=Ctot+Ctrim+Cc;

f=1/2/pi./sqrt(L.*Cx)
f =
  1.0e+008 *
    1.3744    1.3833    1.3951    1.4051    1.4136    1.4208
plot(RevVoltage,f/1e6);grid;
ylabel('Frequency [MHz]');
xlabel('Control voltage [V]');
print -deps c:\tesis\doc\images\tanksim.eps

!
```

diary off

Appendix D

Quadrature demodulator schematics

D.1 Quadrature demodulator schematic

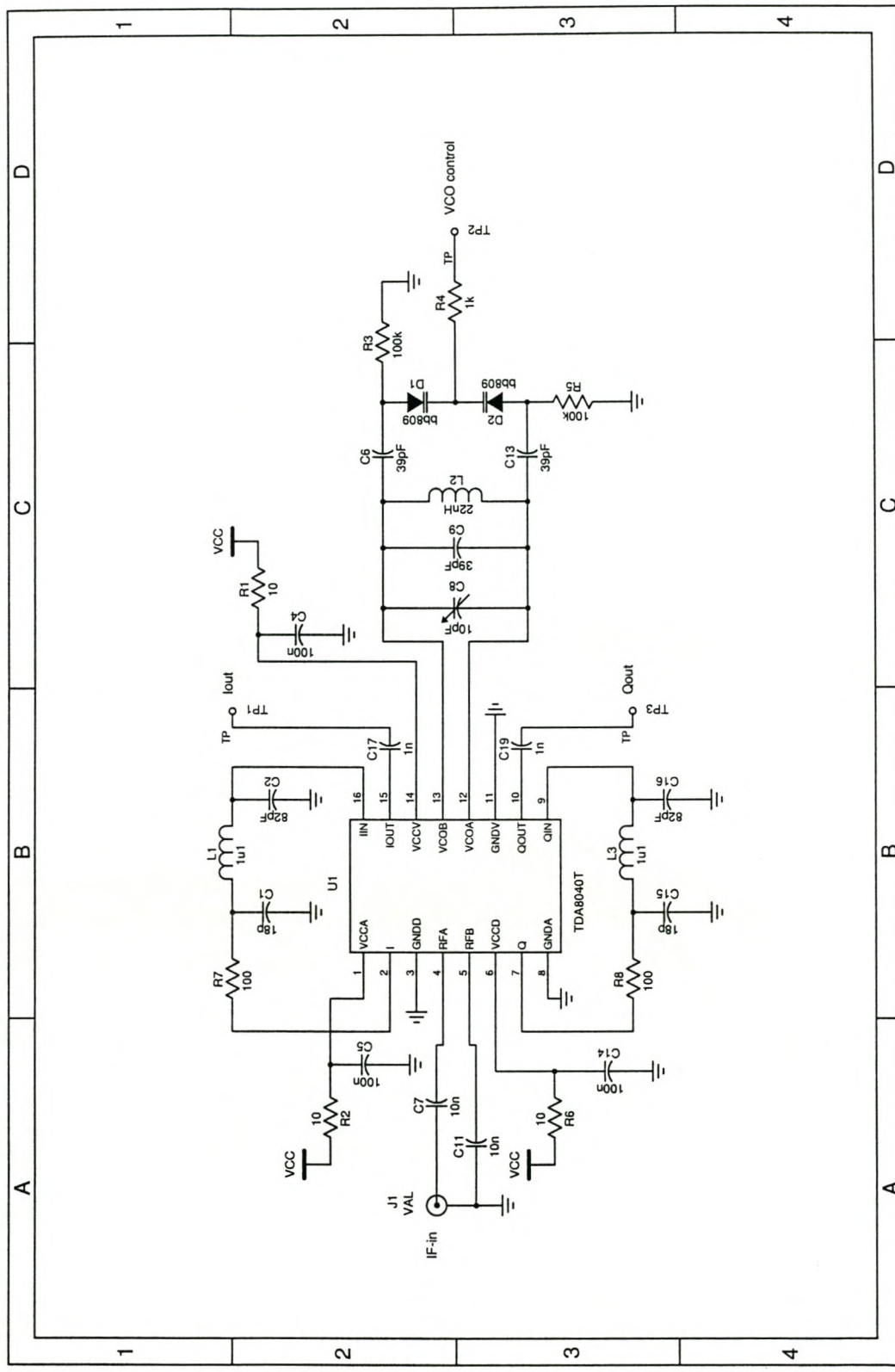


Figure D.1: TDA8040 quadrature demodulator schematic.

D.2 AGC amplifier schematic

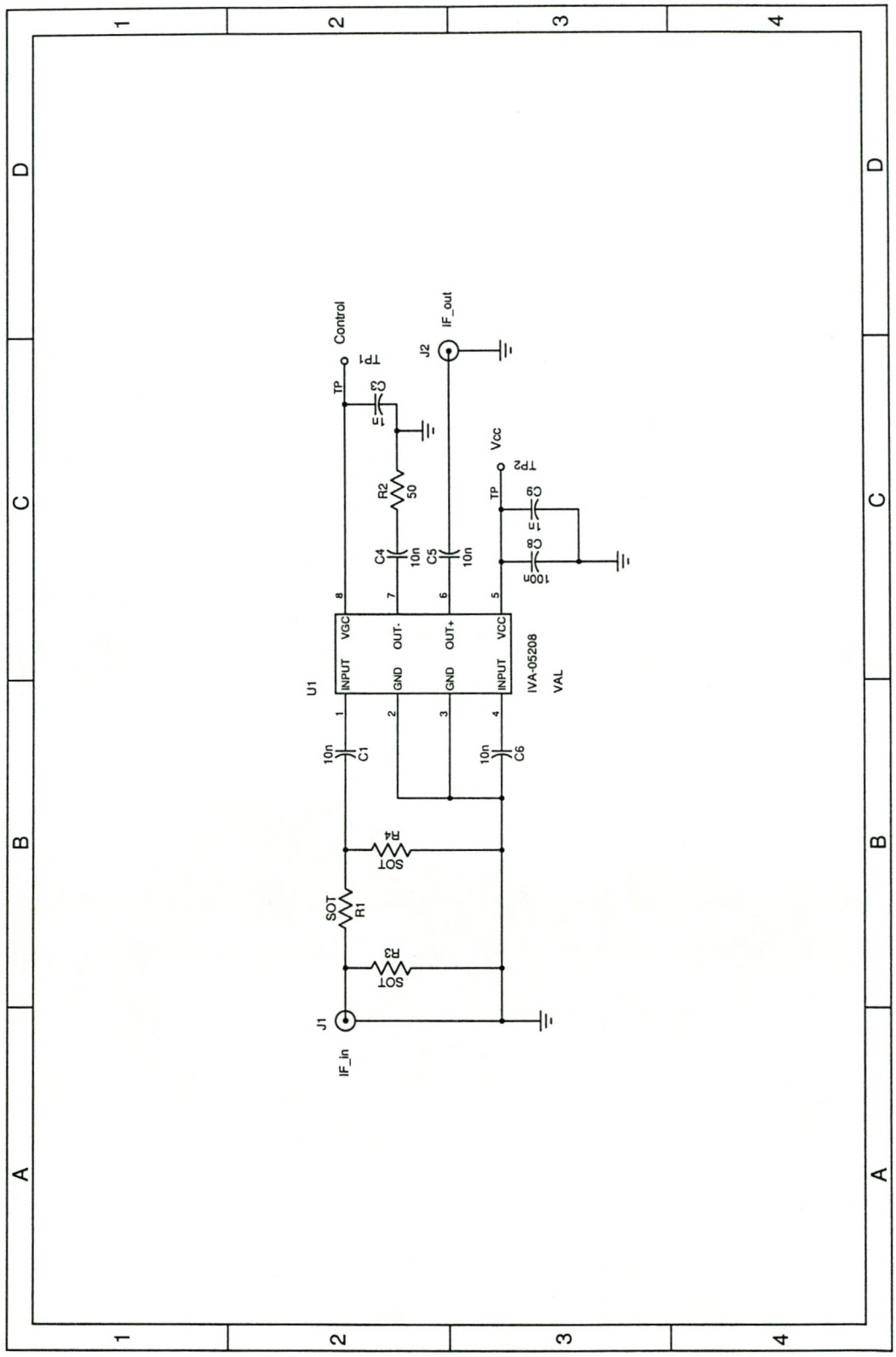


Figure D.2: AGC amplifier circuit diagram.

Appendix E

Demodulator controller schematics

E.1 TDA8041 demodulator controller schematic.

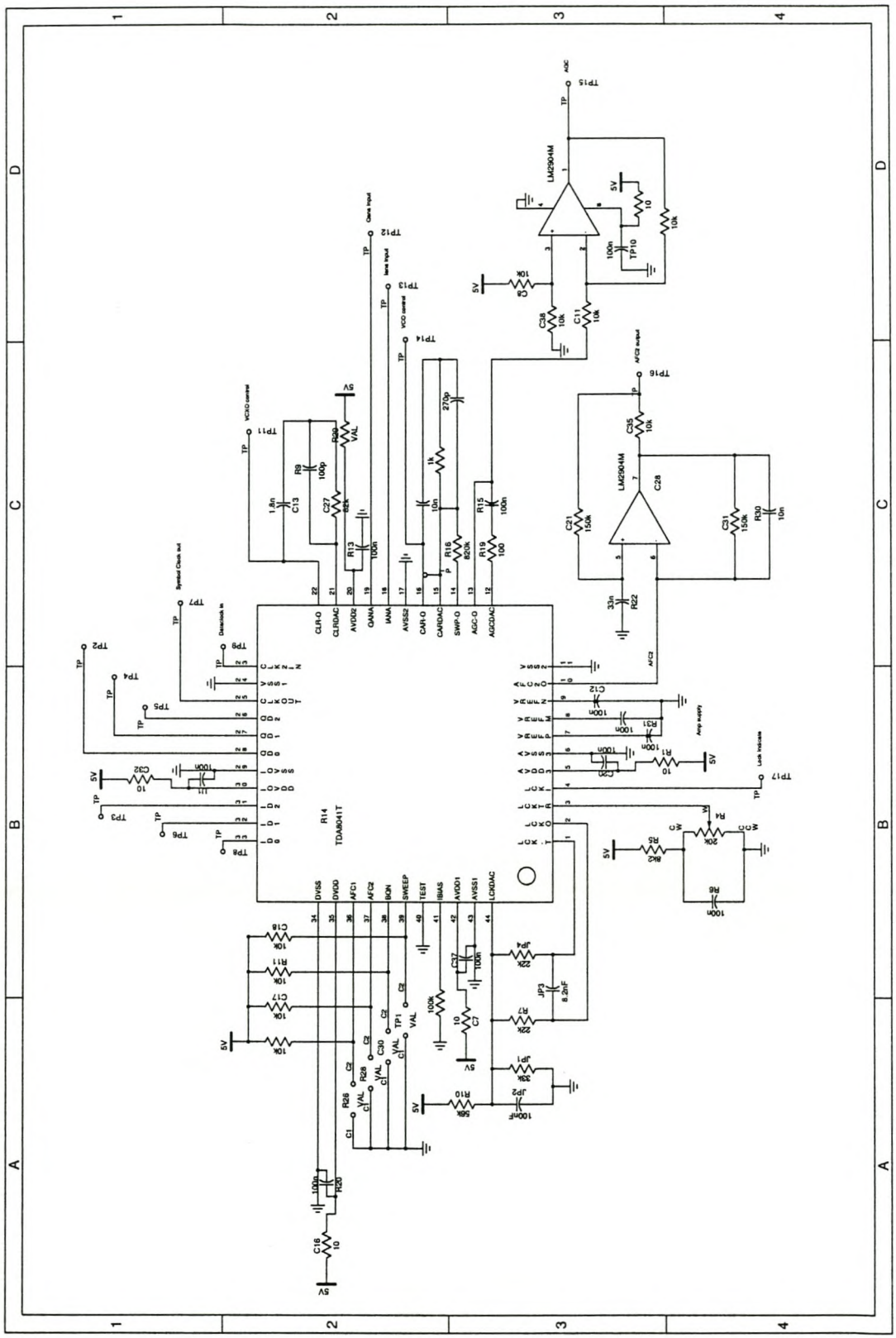


Figure E.1: TDA8041 demodulator controller schematic.

E.2 Voltage controlled crystal oscillator schematic.

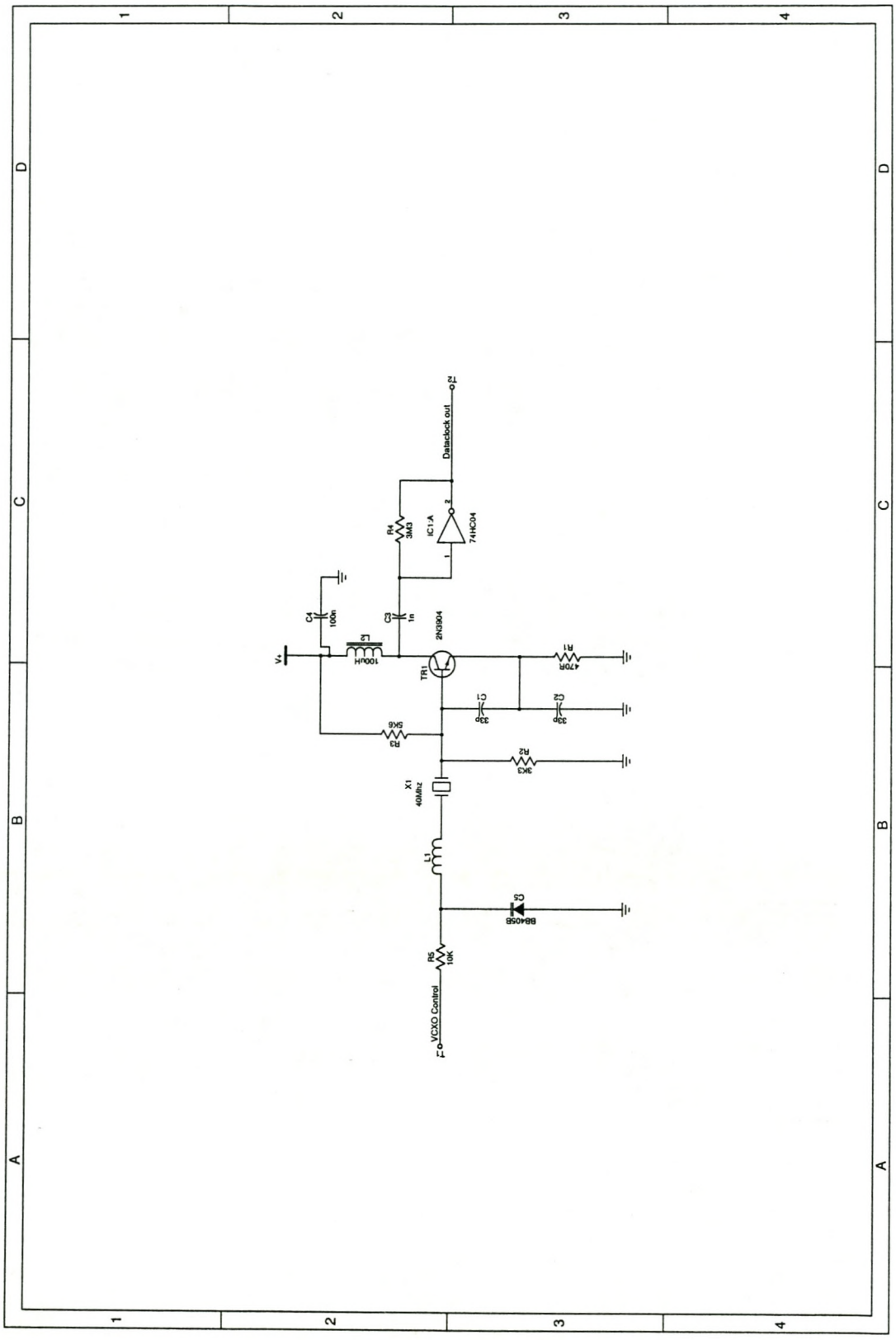


Figure E.2: Voltage controlled crystal oscillator schematic.

E.3 ICD2053B progammable clock oscillator schematic.

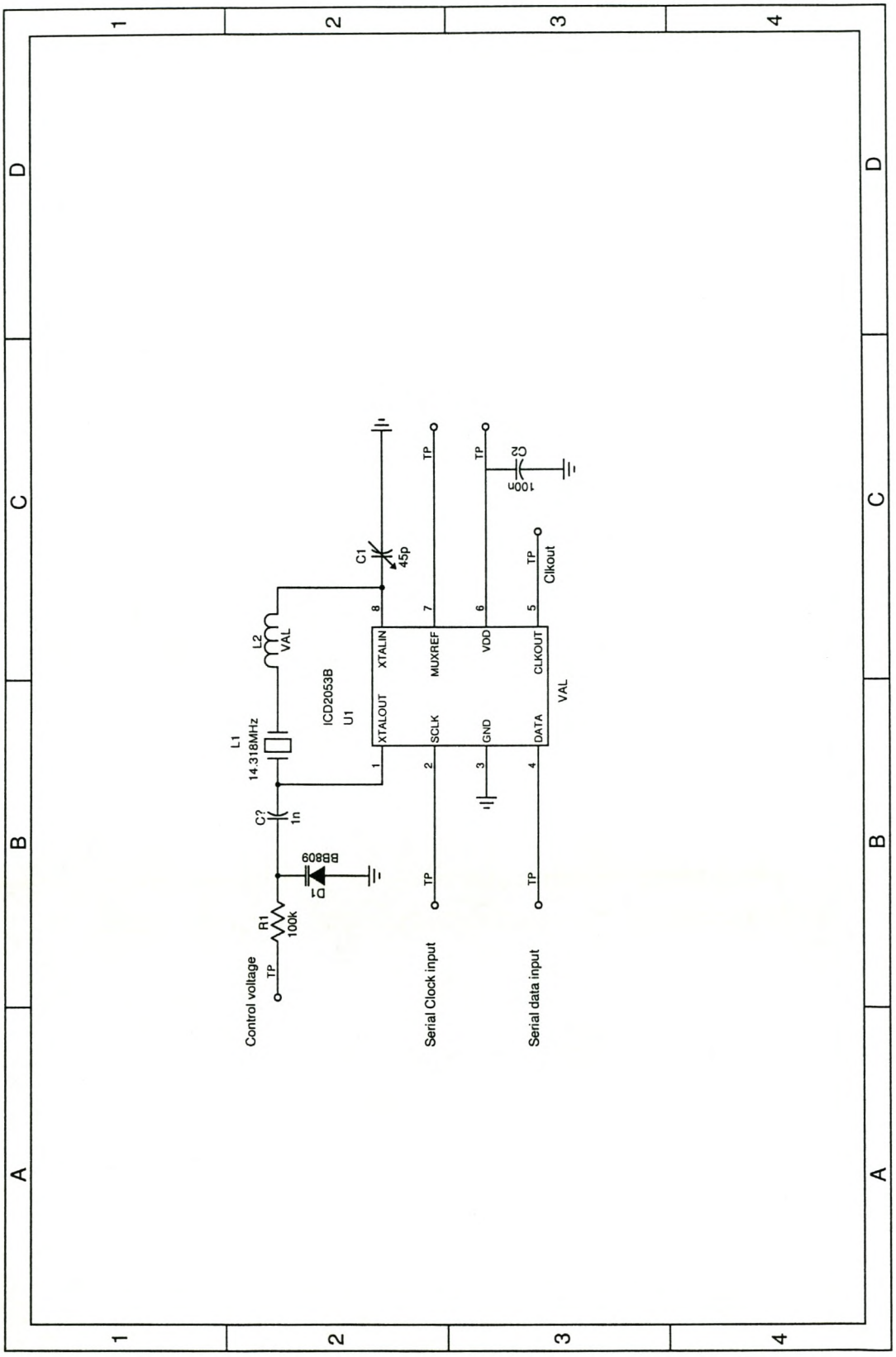


Figure E.3: ICD2053B progammable clock oscillator schematic.

Appendix F

Digital decoding logic design files

F.1 QDEMOD top level graphic design file

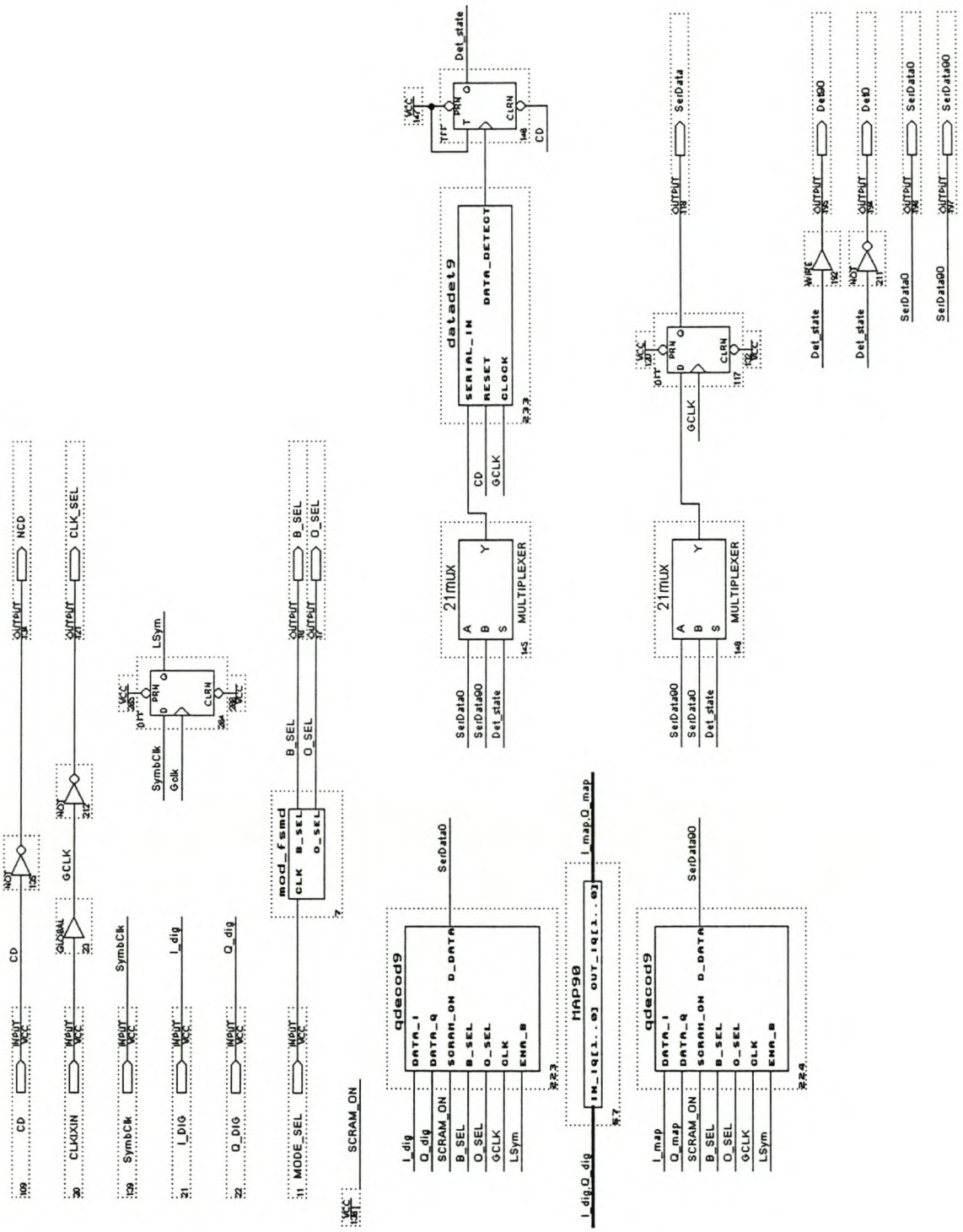


Figure F.1: Graphic design file of digital decoding logic.

F.2 QDECOD top level graphic design file

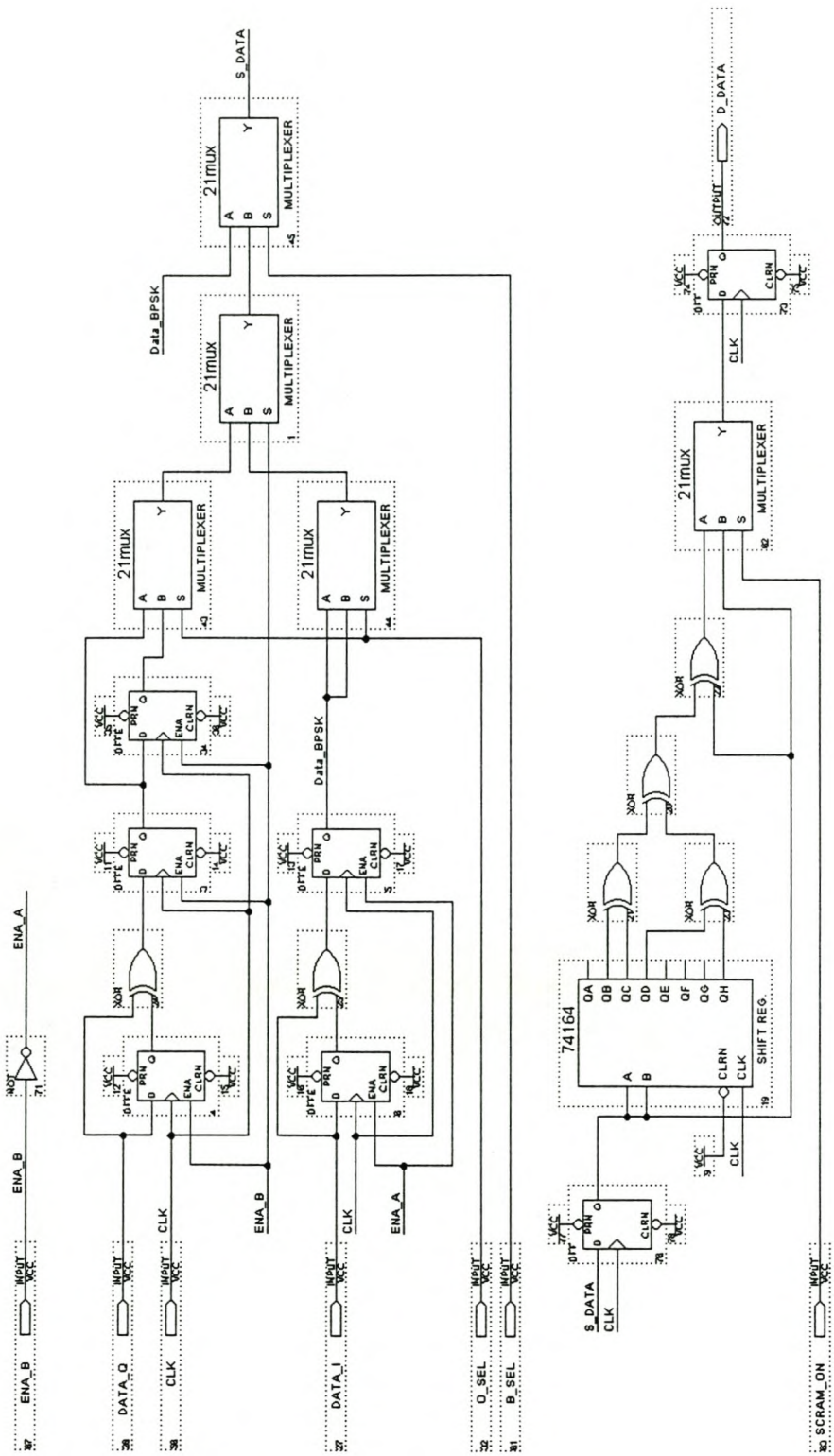


Figure F.2: Graphic design file of decoding and unscrambling logic.

F.3 DATADET top level graphic design file

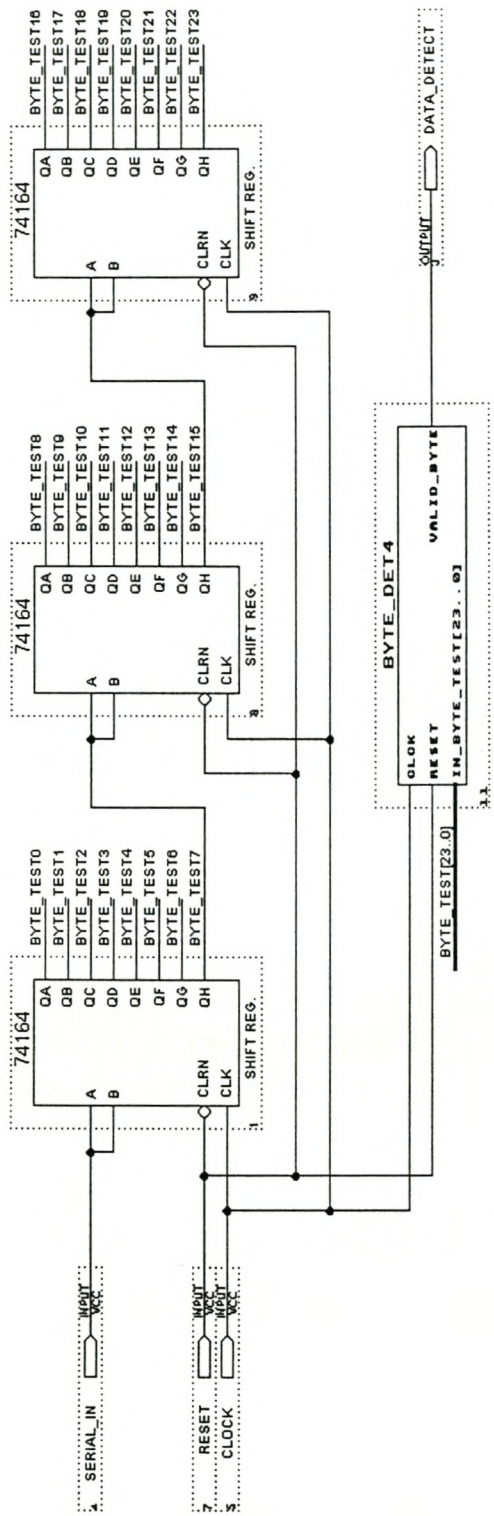


Figure F.3: Graphic design file of data detection logic.

F.4 mod_fsmd AHDL sourcecode

```
SUBDESIGN mod_fsmd
(
clk          : INPUT;          % input   %
b_sel, o_sel : OUTPUT;         % outputs %
)

VARIABLE
mode_fsm     : MACHINE OF BITS (q1,q0)    % create 2-bit state machine %
   WITH STATES (
       QPSK  = B"00",          % normal QPSK (no trellis, no offset)   %
       BPSK  = B"01",          % BPSK (no trellis, no offset)          %
       OQPSK = B"11");         % offset QPSK (no trellis, with offset) %

BEGIN
    mode_fsm.clk = clk;
    b_sel  = !mode_fsm.q1 &  mode_fsm.q0;     % BPSK selected %
    o_sel  =  mode_fsm.q1 &  mode_fsm.q0;     % offset QPSK selected %

    TABLE   % Define state transitions %

    % Present    Next                       %
    % State      State       Outputs        %
    % ---------------------------------- %
        mode_fsm => mode_fsm;
    % ---------------------------------- %
       QPSK     => BPSK;
       BPSK     => OQPSK;
       OQPSK    => QPSK;
    % ---------------------------------- %

END TABLE;

END;
```

F.5 MAP90 VHDL sourcecode

```
-- System      : QPSK S-band demodulator phase re-mapping
-- Description : Maps QPSK symbols (Q Data and I Data) by 90 deg
-- Author      : P.P.A Kotze
-- Date        : 3 August 1998

LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;

ENTITY map90 IS
PORT
(
 in_iq   : IN BIT_VECTOR (1 DOWNTO 0);
 out_iq  : OUT   BIT_VECTOR (1 DOWNTO 0)
);
END map90;


ARCHITECTURE behavioral OF map90 IS
BEGIN
out_iq <= "11" WHEN in_iq = "01" ELSE
  "01" WHEN in_iq = "00" ELSE
  "00" WHEN in_iq = "10" ELSE
  "10" WHEN in_iq = "11";
END behavioral;
```

F.6 BYTE_DET4 VHDL sourcecode

```
-- System          : QPSK S-band demodulator valid code detector
-- Description     : Ouputs a pulse when 3 valid bytes detected
-- Author          : P.P.A Kotze
-- Date            : 3 November 1998

LIBRARY ieee;
   USE ieee.std_logic_1164.all;
   USE ieee.std_logic_arith.all;

ENTITY byte_det4 IS
    PORT
    (
        clck,reset    : IN BIT;
        in_byte_test : IN BIT_VECTOR (23 DOWNTO 0);
        valid_byte    : OUT   BIT
    );
END byte_det4;

ARCHITECTURE behavioral OF byte_det4 IS
    TYPE state_type IS (s0, s1);
    SIGNAL state : state_type;
BEGIN

PROCESS (clck, reset, in_byte_test)  BEGIN
  IF reset = '0' THEN
      state <= s0;
      valid_byte <= '0';
  ELSE
   IF clck'event AND clck='1' THEN
      CASE state IS
      WHEN s0 =>
          --Position      = "765432107654321076543210"
          IF in_byte_test = "111111111111111111111111" THEN
             state <= s1;
          ELSE
             valid_byte <= '0';
             state <= s0;
          END IF;
      WHEN s1 =>
          valid_byte <= '1';
          state <= s0;
      END CASE;
   END IF;   --if CLOCK'event
 END IF;   --if RESET
END PROCESS;
END behavioral;
```

Declaration

I, the undersigned, hereby declare that the work in this thesis is my own original work and has not previously in its entirety or in part been submitted at any university for a degree.

Signature .....PPA Potze..... Date .....2000/02/14.....