Development of Nonlinear CAD Models for the Design of Linear LDMOS Power Amplifiers

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Declaration

I, the undersigned, hereby declare that the work contained in this thesis is my own original work and that I have not previously in its entirety or in part submitted it at any university for a degree.

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Abstract

Nonlinear transistor modeling is becoming increasingly popular due to the demand for high linearity and high efficiency microwave amplifiers. The available models often fail to accurately predict the higher order harmonics and intermodulation distortion, which are essential when designing high-linearity amplifier circuits.

This thesis describes the design of hardware and software used for the development of nonlinear CAD models. A multiline TRL calibration kit is designed and manufactured so that the characterisation of a LDMOSFET, with a RF output power capability of 10W, can be performed using an adaptive-bias S-parameter measurement algorithm. Verification standards are also manufactured and used to determine the measurement accuracy after calibration. A series of GUIs are developed to ease the model extraction process. The extraction of the small-signal model parameters is performed between 0.4 and 3 GHz, and the extraction of the parameter values for the Fager large-signal model is then performed. An improved model is defined that implements two nonlinear charge sources in stead of the three nonlinear capacitors used in the Fager model. The nonlinear charge equations are formulated using the voltage-derivatives of the calculated nonlinear charge at each port of the device. By accurately modeling the voltage-derivatives of the charge, where the voltages are functions of time, the prediction of the current produced by each of the charge sources is improved.

The nonlinear models are verified against the MET model, and all three models are compared to measured data. It is shown that the models are able to accurately predict the single-tone and two-tone output harmonics for class-AB operation, and in many cases the predictions outperform that of the MET model. The single-tone output power is also verified for class-C operation. Although this prediction is not extremely accurate, it is found that the correct trend for the output harmonic power can be predicted.

Uittreksel

Nieliniêre transistormodellering raak al hoe meer gewild weens die vraag na hoëlineariteits- en hoëdoeltreffendheidsmikrogolfversterkers. Die beskikbare modelle faal dikwels om die hoërordeharmonieke en intermodulasievervorming te voorspel, wat noodsaaklik is vir die ontwerp van hoëlineariteitsversterkerstroombane.

Hierdie tesis beskryf die ontwerp van die hardeware en sagteware wat gebruik word vir die ontwikkeling van nieliniêre rekenaargesteunde ontwerpmodelle. 'n Multilyn-TRL-kalibreerstel word ontwerp en vervaardig sodat die opmeet van kenmerke van 'n LDMOSFET, met 'n beskikbare RF-uittreedrywingsvermoë van 10W, met behulp van 'n aanpasbarevoorspanning-meetalgoritme van die S-parameters uitgevoer kan word. Verifikasiestandaarde word ook vervaardig en gebruik om die meetakkuraatheid na kalibrering te bepaal. 'n Reeks grafiese koppelvlakke word ontwikkel om die modelekstraksieproses te vergemaklik. Die ekstraksie van die parameters van die kleinseinmodel word tussen 0.4 en 3 GHz uitgevoer en dan word die ekstraksie van die parameterwaardes van die Fager-grootseinmodel uitgevoer. 'n Verbeterde model word gedefinieer wat twee nieliniêre ladingsbronne implementeer in plaas van die drie nieliniêre kapasitors wat in die Fager-model gebruik word. Die nieliniêre ladingsvergelykings word geformuleer deur die spanningsafgeleides van die berekende nieliniêre lading by elke poort van die toestel te gebruik. Deur die spanningsafgeleides van die lading akkuraat te modelleer, waar die spannings tydfunksies is, word die voorspelling van die stroom deur elke ladingsbron verbeter.

Die nieliniêre modelle word teen die MET-model geverifieer en al drie modelle word met gemete data vergelyk. Daar word getoon dat die modelle die enkeltoon- en tweetoonuittreeharmonieke vir klas-AB-werking akkuraat kan voorspel, en in baie gevalle is die voorspellings beter as dié van die MET-model. Die enkeltoonuittreedrywing word ook vir klas-C-werking geverifieer. Alhoewel hierdie voorspelling nie besonder akkuraat is nie, is daar gevind dat die korrekte neiging vir die uittreeharmoniekdrywing voorspel kan word.

Acknowledgements

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- Dr. Cornell van Niekerk for all the support, effort and opportunities, thank you for always being so patient while explaining such difficult concepts,
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Chapter 1

Introduction

1.1 Introduction

Nonlinear transistor modeling is becoming increasingly popular due to the demand for high linearity and high efficiency microwave amplifiers. The availability of highly sophisticated computer aided design (CAD) software has also made the implementation of these models more viable. A number of suppliers of silicon laterally diffused metal oxide semiconductor field-effect transistors (LDMOSFETs) already provide models for some of their devices such as the Motorola electrothermal (MET) model. Unfortunately some of the models often fail to accurately predict the higher order harmonics and intermodulation distortion, which are essential when designing high-linearity amplifier circuits.

LDMOS transistors provide a better intermodulation distortion (IMD) performance compared to competing technologies. These transistors are manufactured from silicon, and hence also have a relatively low cost-per-Watt performance. A N-type LDMOSFET, the MRF282, is therefore used here to develop models that can be used for high-linearity power amplifier design.

1.2 Device Characterisation and Parameter Extraction

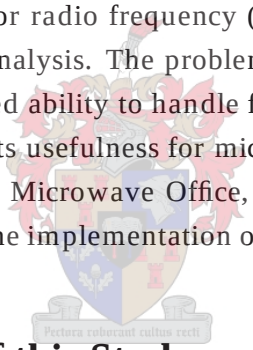
The construction of nonlinear models begin with the characterisation of a device. A spectrum analyzer (SA), vector network analyzer (VNA), suitable microstrip through-reflect-line (TRL) calibration kit, power supply units (PSUs), and a personal computer (PC) are required to perform the characterisation. The spectrum analyzer is used for verifying the stability of the device so that the VNA is not damaged by high-power oscillations, while the TRL calibration kit is used to calibrate the VNA so that the device can be characterised. The PC is used to control the VNA and PSUs, so that time consuming characterisation can be performed with a minimum amount of human intervention.

A PC is also required to perform the extraction for the different models. The extraction of small-signal equivalent circuits and nonlinear model parameters require a reasonable amount of computational power since various optimisation-based algorithms are used to determine each of the elements' values as accurately as possible.

1.3 Nonlinear Modeling

There are three main modeling approaches [1] when describing the non-linear behaviour of a device. The first approach is physically based modeling that describes the active device in terms of the motion of charge carriers and geometrical characteristics. The second approach is black box modeling. This method allows a device to be represented by a behavioural input/output model, where no insight is required to the physical operation of the device. The third approach is empirical equivalent circuit modeling and is the most widely used type of modeling. The empirical equivalent circuit modeling approach is used for this project.

The two dominant methods [2] for radio frequency (RF) and microwave circuit analysis are transient and harmonic balance analysis. The problem with transient analysis methods, such as used by SPICE, is that its limited ability to handle frequency-domain data and lossy or dispersive transmission lines limits its usefulness for microwave simulations. The harmonic balance method of analysis, used by Microwave Office, is more practical for frequency domain simulations and is used here for the implementation of the nonlinear models.



1.4 Scope and Layout of this Study

This thesis presents the following issues regarding nonlinear modeling:

- The impact of different TRL calibration errors is investigated to determine where improvements can be made to develop more accurate TRL calibration standards.
- A multiline TRL calibration kit is designed and manufactured for measuring a LDMOSFET with a RF output power capability of 10W. Verification standards are also produced and used to determine the measurement accuracy after calibration.
- A removable coaxial to microstrip transition is developed that minimises input reflection.
- Measurements are performed on the MRF282 LDMOSFET over a selected set of bias points to determine the stability of the device, and an adaptive-bias S-parameter measurement algorithm is used to perform the characterisation of the MRF282.
- A series of graphical user interfaces (GUIs) are developed to allow the user to perform the extraction of the small-signal model parameters in a fast, efficient and accurate manner.

A GUI is also developed to help the user perform the extraction of the parameter values for the Fager large-signal model.

- An improved model is defined that implements two nonlinear charge sources that are capable of predicting the intrinsic capacitances of the device more accurately over bias. The charge equations are constructed to model the voltage-derivatives of the calculated nonlinear charge at each port of the device.
- The original Fager, improved Fager and MET models are implemented in Microwave Office to verify the quality of the predictions for each of the models against measured data. The verifications include the evaluation of small-signal S-parameter predictions in each of the bias regions, single-tone harmonic output power and fundamental phase prediction as functions of input power for class-C and class-AB operation, and the evaluation of two-tone third-order intermodulation prediction for class-AB operation.

Chapter 2 provides a detailed discussion of the typical calibration errors found, and hardware developed to improve the measurement accuracy. In chapter 3 the hardware is used to perform the characterisation of the device and the extraction of the small-signal model is performed. Chapter 4 describes the operation of the Fager large signal model, the development of an improved Fager model and the extraction of the large-signal model parameters is performed. The models are verified in chapter 5 against measured data. The thesis is concluded in chapter 6 with an overview of the outcome and a discussion of future development of this project.

Chapter 2

Improved TRL Measurement Setup

2.1 Introduction

TRL calibration is probably the most popular calibration technique when performing measurements on microstrip. The components required can easily be manufactured and there is a large amount of literature available to enhance the accuracy of such calibration. In the first part of this chapter the impact of the different calibration errors is investigated. The most prominent errors are listed and improvements are made where it is most important. In stead of performing conventional TRL calibration, a more advanced method called multiline TRL calibration is used. This method uses redundant line standards to minimise the effect of random and systematic errors. An improved calibration kit is designed and manufactured for measuring a LDMOSFET [3, 4] with a RF output power capability of 10W. Verification standards are also designed and manufactured, and used to determine the measurement accuracy after calibration.

The interchanging of the calibration standards plays an important role during calibration. Removable coaxial to microstrip transitions are usually preferred when working with microstrip TRL standards. These transitions allow rapid interchanging and provide convenience when modifying the calibration standards without having to re-design any of the other components. Unfortunately, when dealing with coaxial to microstrip transitions, it is important to note that the inherent discontinuity causes a portion of the input power to be reflected back into the VNA's ports. The magnitude of this reflected power influences the lowest reflection detectable from the device under test (DUT) and thereby affects the accuracy of the calibration. To obtain high measurement accuracy it is therefore essential to minimise the reflection caused by these transitions. The second part of this chapter deals with the development of a coaxial to microstrip transition that minimises this reflection.

2.2 Multiline TRL kit for 10W LDMOS FET

Calibration of the VNA relies on measurements of well-known standards to mathematically de-embed the imperfections up to the measurement planes. A conventional set of three distinct well-characterised impedance standards is usually very difficult to produce for dispersive transmission media such as microstrip. The TRL calibration method [5] provides the advantage that it only relies on transmission line standards that can be accurately manufactured on microstrip. The three or more different standards require that the same characteristic impedance is used throughout, and hence require that the microstrip tracks have the same width. The lengths of the standards only need to be known approximately, except for the length of the through standard that must be manufactured accurately. The reflect standards must have the same lengths, but imperfect reflections with virually unknown characteristics can be used. The first part of this section investigates the sources of TRL calibration error, leading to the better understanding and quantification of typical TRL calibration errors. The rest of this section looks at the development of an improved accuracy multiline TRL calibration kit and the determination of the residual calibration errors.

2.2.1 Sources of Error in Microstrip TRL Calibration

The error model for two-port TRL calibration can be seen in figure 2.1. Error boxes A and B hold the parameters [5] used to remove the non-ideal characteristics of the VNA's reflectometers, cables and other components up to the measurement planes. Additional error boxes σ_A and σ_B that represent the repeatability errors and manufacturing tolerances of the standards are excluded from the traditional error model. These error boxes cannot be determined during calibration since they tend to differ with each measurement and cannot be compensated for in traditional TRL calibration.

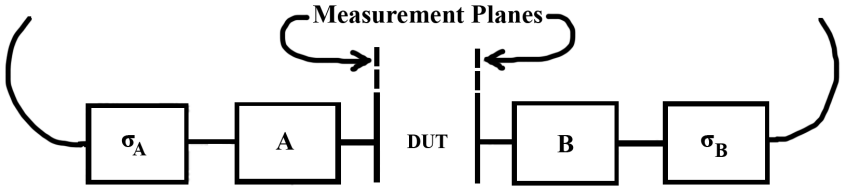


Figure 2.1: Simplified block diagram illustration of VNA calibration. Error boxes A and B represent the de-embedding of the non-ideal effects up to the specified measurement planes.

In order to cover a frequency span greater than 8:1, multiple line standards must be used for calibration. Single transmission lines can only be used in the frequency ranges where the phase of the line varies between 20° and 160° with that of the through [6]. This restriction is because measurement uncertainty increases significantly when the phase difference nears 0° or any integer multiple of 180°. The effects of σ_A and σ_B can be seen when calibrating with more than

one line standard. Figure 2.2 shows this effects on a measurement of $|S_{11}|$ for one of two line standards after performing conventional TRL calibration. A step in $|S_{11}|$ exists between where different line standards were used for calibration. The measured transmission line was used to calibrate for the lower frequency band up to 2.8 GHz. The reflection is low in this band at about -50 dB but increases sharply to -30 dB for the higher frequency band. This phenomenon is due to the existence of error boxes σ_A and σ_B and indicates that different calibration parameters exist for the two line standards even though they were manufactured to be similar apart for their difference in length. A higher reflection is therefore visible in the frequency range where a standard is not used for calibration. This discontinuity becomes problematic when measuring highly-reflective devices with S-parameters on the edge of a Smith chart.

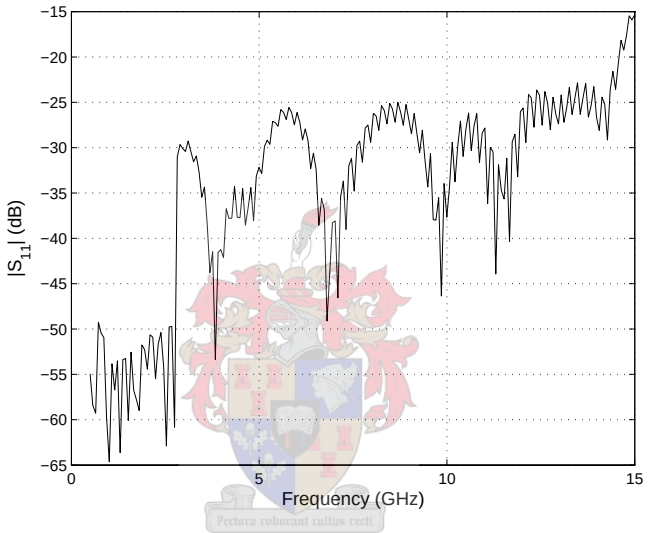


Figure 2.2: Measured $|S_{11}|$ for the longer of the two line standards used for performing conventional TRL calibration over a wide bandwidth.

A number of artificial TRL calibration kits were created for simulation using Microwave Office [7], to determine the impact on calibration accuracy when known non-ideal characteristics are introduced to ideal calibration standards. A circuit diagram in Microwave Office for one of the kits is shown in figure 2.3. Each calibration standard contains a typical set of 30 mm launch lines and in this instance the zero-length through standard contains an inserted length error of 0.3 mm. Five sources of systematic error are described in [8]: asymmetry in a nominally symmetric short, variations in line length and width, error in the capacitance used to determine the calibration reference impedance, and variations in metal thickness and/or resistivity. Along with the above mentioned sources of error the impact of a dispersive transmission line characteristic impedance is also examined. These are the errors most typical to occur in microstrip TRL calibration standards.

A set of previously-measured S-parameters from a CFY-30 gallium arsenide FET is used to emulate a typical device characterisation. Microstrip launch lines are added to the device in

the simulation to create a similar DUT test setup as for physical two-tier measurements. Two-tier TRL calibration is performed and the extracted CFY-30 S-parameters are compared to the inserted S-parameters to examine the impact of each of the non-ideal effects on the extraction accuracy. The most important error results are listed in table 2.1. The percentage error in the magnitude of the S-parameters is less than 0.1% when coaxial standards are used, but increases to approximately 1% when dispersive microstrip is used. The measurement error increases to approximately 7% when an error of 0.3 mm exists in the length of the through standard. Similar error magnitudes exist in $|S_{11}|$ and $|S_{22}|$ when one of the reflect standards varies with 0.3 mm in length from the other one. Good measurement accuracy is therefore strongly dependant on the accuracy of these lengths.

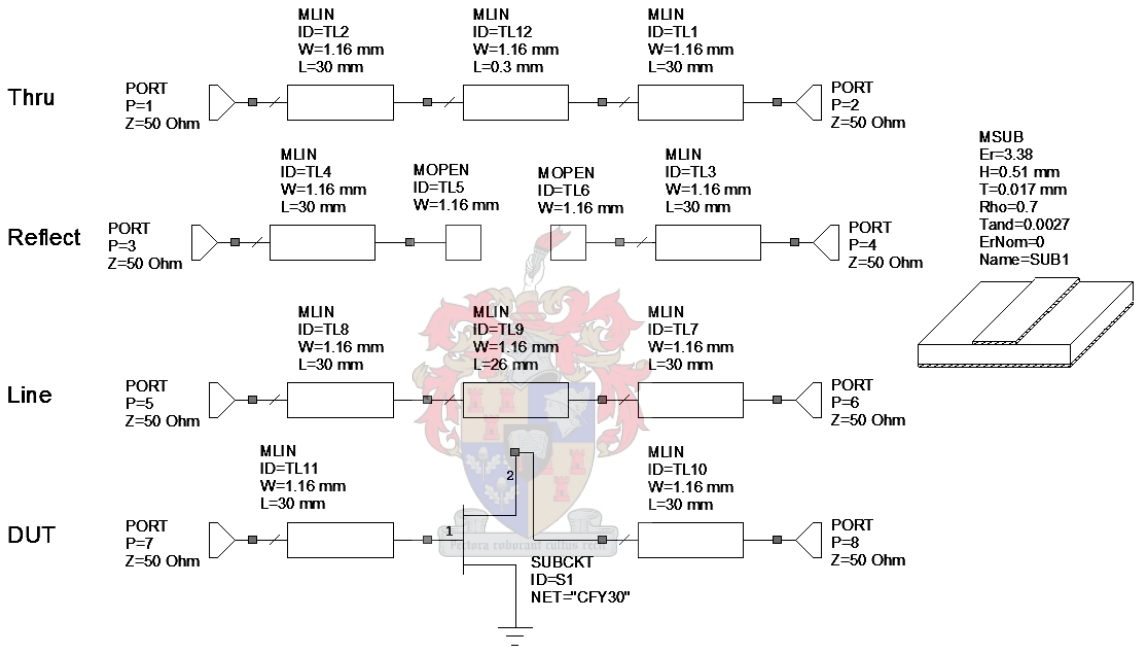


Figure 2.3: Circuit diagram in Microwave Office illustrating an artificial TRL calibration kit. Two-tier TRL calibration is used to de-embed the original S-parameters so that the impact of the non-ideal effects can be examined.

Table 2.1: Impact of calibration errors on the measurement accuracy of a typical DUT between 0.4 GHz and 8 GHz.

Calibration Kit Description	Maximum Error (%)			
	$\|S_{11}\|$	$\|S_{21}\|$	$\|S_{12}\|$	$\|S_{22}\|$
Ideal coaxial TRL calibration	0.04	0.05	0.07	0.09
Dispersive microstrip TRL calibration	0.60	0.75	0.75	1.20
0.3 mm Length error in microstrip through standard	7.50	7.00	7.00	6.75
0.3 mm Length error in one of microstrip reflect standards	6.75	0.75	0.75	6.75

Another source of TRL calibration error is the repeatability of the coaxial to microstrip transitions. A 470Ω 0603 resistor, connected in series between the two calibration planes, was used as

a DUT for this experiment. The repeatability error was examined by taking several measurements between 0.4 and 4 GHz, while mechanically disconnecting and reconnecting the DUT before each measurement. The mean of the variations between the different measurements are plotted in figure 2.4. It can be seen that the phase errors increase slightly at higher frequencies, but the error magnitudes are so low that it is difficult to identify a certain trend in the noisy data. The magnitude repeatability error is typically less than 0.04 dB and the phase repeatability error less than 0.4° and hence no improvements are needed here.

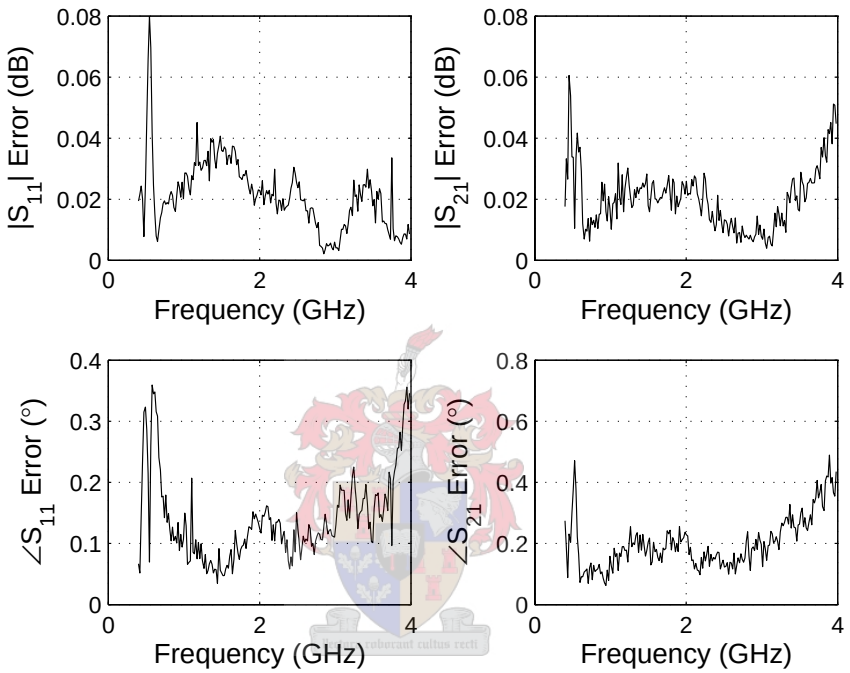


Figure 2.4: Mean S_{11} and S_{21} repeatability errors after several measurements on a 470Ω 0603 resistor. Similar results exist for S_{22} and S_{12}.

The results of the experimentation on calibration errors can be used to design improved TRL standards with improved calibration accuracy. The length of the through standard must be manufactured as accurately as possible and the reflect standards must have the same lengths. The length of the launch lines of the DUT standard must also be manufactured with great accuracy to minimise phase error. Mechanical accuracy can usually be achieved without much difficulty, but is generally neglected due to ignorance. Another substantial rule is that the standards should all be manufactured on the same sheet of laminate. The thickness and permittivity of different sheets of the same type of laminate are known to vary from each other. A laminate should also be chosen so that the relative permittivity stays sufficiently constant over the required bandwidth. During the TRL calibration process it is assumed that all of the launch lines have exactly the same electrical and electromagnetic properties. Care should therefore be taken so that the microstrip tracks have the same width and a very smooth etch-line. The

standards should also not be coated with any kind of conformal coating or silk screen except when the high-frequency properties of the coating is well known.

2.2.2 Multiline TRL Calibration

An improved method to perform TRL calibration is the multiline TRL calibration technique. This method shows improvements [9] in both accuracy and bandwidth over conventional TRL calibration. The most recognisable feature of this method is that it uses redundant transmission line standards to minimise the effect of random errors such as imperfect connector repeatability. This method allows a more efficient utilisation of available information so that optimal calibration accuracy can be obtained over a wide frequency range. The normalised standard deviation (σ) for determining the propagation constant (γ) is calculated by the algorithm over frequency for each line standard, and is used to determine a single (γ) with minimum variance. In other words: γ is determined using all of the line standards over the whole frequency range. The only hardware changes from conventional TRL is that more than one line standard needs to be used in order to obtain more accurate results. This allows the extra implementation cost to be relatively small. When only one line standard is used with multiline calibration, the results are exactly the same as with traditional TRL calibration. Accuracy when performing propagation constant measurements [10] can also be improved using multiline calibration when the characteristic impedance of the lines do not match the reference impedance of the instruments. It is further revealed that when using the multiline method with two or more lines the accuracy when determining the propagation constant is limited only by the random errors encountered in the connections to the lines and by the accuracy of the length difference between the lines. The multiline method delivers optimal results [11] when the measurement frequency points are evenly spaced.

The program MultiCal [12] is used for error-box formulation and for providing the calibration coefficients to the VNA. Figure 2.5 shows the main menu of MultiCal. The user is required to configure [13] the program so that it can be used for the specific calibration kit. The first step is to set up the correct calibration standards' settings. In the case of figure 2.5 three line standards are used together with zero-length through and reflect standards. The length of the transmission lines and the filenames for each standard is specified by the user. The program allows each standard to be characterised separately and the measurements are stored under the specified file names. The user is also required to estimate the effective permittivity (ϵ_{eff}) of the laminate. The estimate can be determined using a program called Txline that is supplied with Microwave Office or by using equation (2.2.1) [14]. The width of the line is represented by W and the height of the laminate by d. The same unit of measure is used for both. After the setup is complete the de-embedding process can be initiated and the 12-term error correction model is determined by the program. The program loads the model coefficients into the VNA and with the completion of multiline TRL calibration the VNA can be used independently to

take calibrated S-parameter measurements.

$$\epsilon_{eff} \approx \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12d/W}} \tag{2.2.1}$$

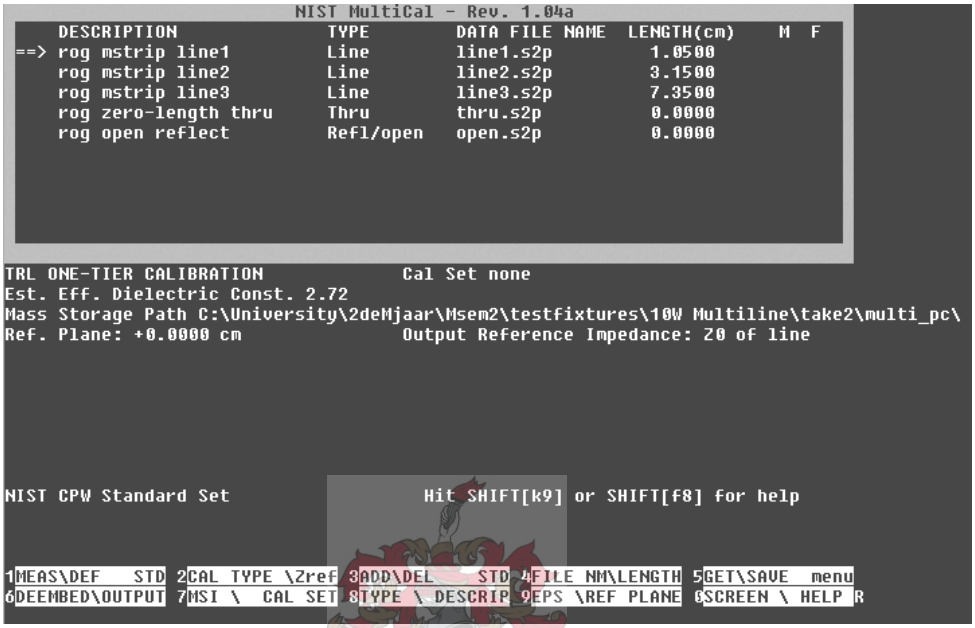


Figure 2.5: The program MultiCal is used to perform multiline TRL calibration on the VNA.

2.2.3 Design of Multiline TRL Standards

A multiline TRL calibration kit is now designed for performing S-parameter measurements on a 10 W LDMOS transistor between 0.4 and 8 GHz. The wide frequency range was chosen in order to allow a detailed equivalent circuit model to be extracted from the S-parameter data. When designing a multiline TRL calibration kit the zero-length through and the reflect standards for each port require only the specification of the length of the microstrip launch lines. 30 mm Launch lines are chosen as a reasonable length that allows for enough attenuation of higher order modes should a lossy cavity be implemented around the line in the future, and allows the design of reasonable-sized calibration standards. The most thought when designing a multiline TRL calibration kit goes into choosing the optimal lengths for the line standards. There is no known literature available describing the optimal number of line standards. Because two or more line standards must be used to honour the term multiline, a decision should be made on how many more redundant standards are required to achieve an acceptable level of calibration accuracy.

It is stated in [11] that the choice of lines should ensure that there is at least one line pair that gives a transmission coefficient phase difference other than 0° or multiples of 180° over the

chosen frequency band. The accuracy is known to increase to an optimal value when the phase difference reaches 90° and the best accuracy over a frequency band is therefore obtained with an even distribution of the phase difference or σ. Such a distribution can be found when the line lengths are chosen as integer multiples of the length of the shortest line. In this case the length is determined to be 10.5 mm, by using FindLen [15] iteratively to calculate σ so that a minimum value at the centre frequency of the desired bandwidth is found. σ for this line length is plotted in figure 2.6 over frequency as determined using FindLen. The length of the longest line is chosen to be 73.5 mm, which is seven times the length of the shortest line. Long transmission line standards can be used at much lower frequencies than shorter lines, but are generally more difficult to manufacture accurately. The multiple seven factor is chosen so that σ is allowed to lower sufficiently at the lowest and highest frequency points, but that the long length of the standard does not greatly influence the manufacturing accuracy. After the determination of the shortest and longest line lengths, any number of additional line lengths can be added to further improve the combined standard deviation. With each added standard comes a number of random and manufacturing errors so that a good trade off is to add just one more line standard. A length of 31.5 mm is chosen, which is three times that of the shortest line. The standard deviation for each of the three determined transmission line lengths is plotted in figure 2.6 and the combined standard deviation for the three lines is plotted in figure 2.7.

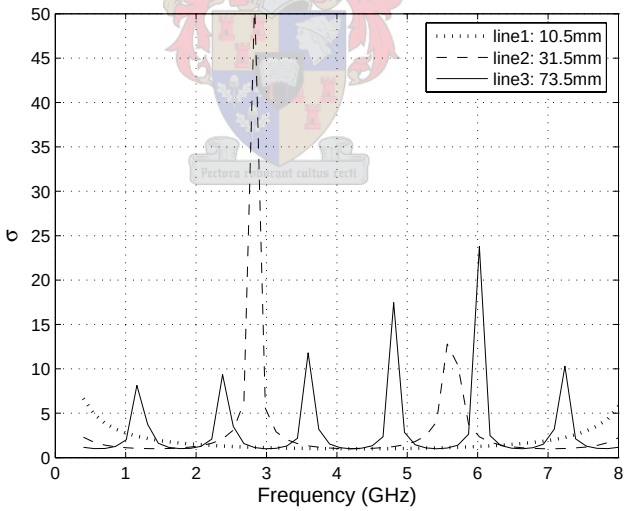


Figure 2.6: Separate standard deviation calculated for each of the three chosen line lengths using FindLen. The standard deviation for each line enables the determination of the propagation constant of the lines, with minimum variance, by the multiline calibration algorithm.

2.2.4 PCB Layout

The designed TRL calibration standards are manufactured using microstrip printed circuit boards (PCBs). The popular Rogers 4003 high frequency low loss laminate is used. The rel-

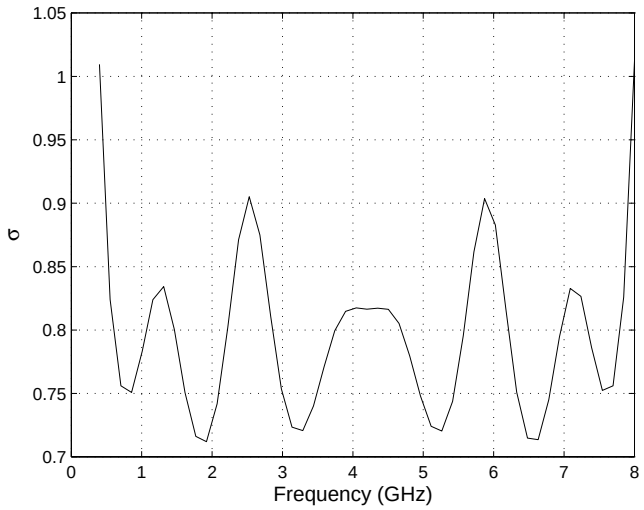


Figure 2.7: Combined standard deviation for the determination of the propagation constant, calculated for the three chosen line lengths using FindLen.

atively low cost of the material is one of the main reasons why this laminate is well-known for commercial use. The material's specifications are listed in table 2.2. The measured properties of the material are also included. These properties were determined using the optimiser in Microwave Office and S-parameter measurements of two of the line standards, after performing a coaxial short-open-line-through (SOLT) calibration. The simulation included the microstrip lines and coaxial transmission lines to simulate the effect of the coaxial to microstrip transitions. The dissipation factor and ϵ_r were optimised so that the simulated S-parameters fitted on the measured S-parameters. The physical dimensions were determined using a micrometer and ϵ_{eff} was determined afterward using Txline. The calculation of ϵ_r was also verified using a Matlab [16] implementation of microstrip transmission line equations [17, 18] and a Gauss Newton optimiser [19], but is not shown here.

Table 2.2: RO4003 laminate specifications.

	ϵ_r	ϵ_{eff} @4GHz	Height (mm)	Copper Thickness (μm)	Dissipation Factor	Line Width (mm)
Specified	3.38	2.71	0.508	55	0.0027	1.524
Measured	3.38	2.70	0.46	100	0.0059	1.51

The width of the lines is chosen to match the recommended pad size of the MRF282 LDMOS transistor. A measured line impedance of 38Ω allows a characteristic impedance closer to the input and output impedances of the device. This allows less chance of device oscillation, and enables measurements closer to the centre of the Smith chart, which improves the measurement accuracy. The pads for the device are incorporated into the launch lines. This is done so that after calibration only the legs of the device and the extra capacitance added due to the soldered connections are included in the measurements. Transmission line elements representing the

effect of the pads can therefore be neglected during the small signal model extraction. The base of the MRF282 is soldered on to a large pad that is connected to the ground plane using 55 micro-vias. The large amount of vias not only reduces the inductance to ground but also enhances the thermal conductivity from the device to the heatsink below.

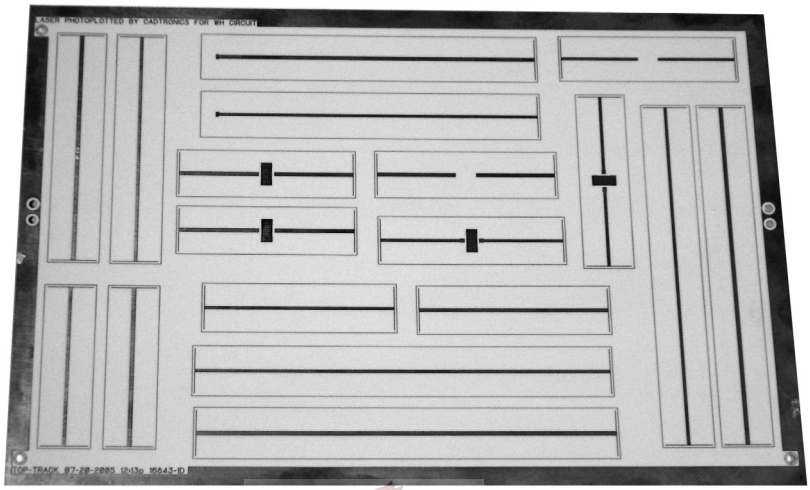


Figure 2.8: Printed circuit board of the TRL calibration standards. Additional standards are included on the board to provide a margin for further experimentation.

2.2.5 Structural Design of the Calibration Kit

The physical structure supporting the calibration kit can be seen in figure 2.9. The structure has already been through many iterations to improve its functionality and ease of use. The calibration standards are inserted from the top into the centre of the structure. The attached fan is powered by an external power supply to allow airflow over the DUT's heatsink. On each side of the calibration standard is a coaxial to microstrip transition block. The coaxial to microstrip transition blocks, along with the other components, can be shifted horizontally to compensate for standards of variable length. A short flexible cable on each side connects to the external bias-Ts. The VNA cables are connected through the cable stabilisers to the bias-Ts. The cable stabilisers (furthest to the left and right sides in the figure) minimises movement in the cables. This improves the phase stability of the cables during calibration.

Each calibration standard block is designed so that optimum measurement accuracy can be obtained. The DUT block can be seen in figure 2.10. The shallow ridges on the sides of the block ensures that the pressure induced when the blocks are clamped together is concentrated near the transition between the coaxial and microstrip ground planes. The channel in which the transmission line lies was added to suppress the propagation of higher order modes along the line. The clamps that form the cavity are used to push down the microstrip board. The cavity width is designed to be narrow so that good contact is ensured between the microstrip

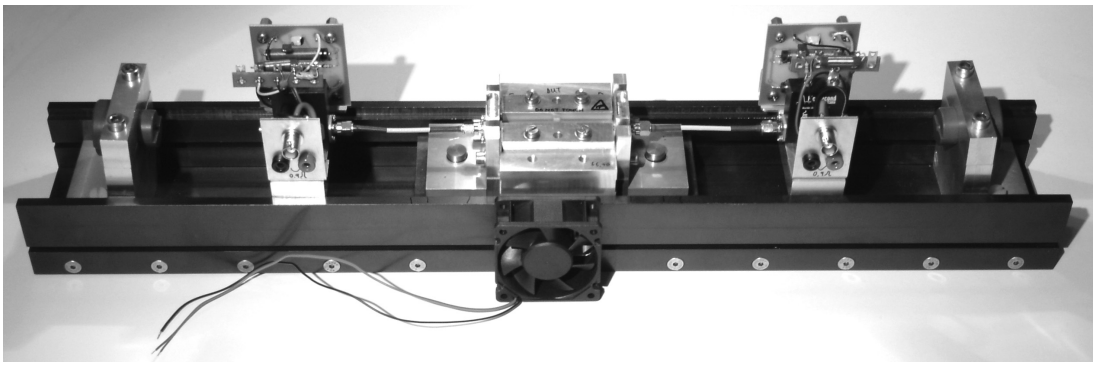


Figure 2.9: The TRL calibration test fixture is used to hold the components required to perform the measurements.

ground plane and the block underneath the transmission line, and to allow a high enough cutoff frequency (f_c) for the higher order modes. The channel is also designed to be wide enough so that coupling between the line and the cavity can be neglected. The rule of thumb for a microstrip transmission line is that objects further away than twice the width of the line or twice the height of the laminate will have insignificant coupling with the line. A gap of two and a half times the width of the line is chosen to allow for reasonable mechanical tolerances. Each channel forms a parallel plate waveguide that depresses the propagation of higher order TE_n and TM_n modes. The cutoff frequency at which the modes start to propagate is found using equation (2.2.2) from [14]

$$f_c = \frac{n}{2d\sqrt{\mu\epsilon}} \tag{2.2.2}$$

where $\epsilon \approx 8.854 \times 10^{-12}$ F/m and $\mu \approx 4\pi \times 10^{-7}$ H/m for air, and d is the distance between the plates in metres. The lowest cutoff frequency is for TE_1 and TM_1 modes, and is calculated using (2.2.2) to be approximately 15 GHz when the width of the channel $d = 10mm$, which is sufficiently higher than 8 GHz. The completed TRL calibration kit can be seen in figure 2.11.

2.2.6 Calibration Verification

Calibration verification standards are manufactured so that the user is able to quantify the measurement uncertainty after calibration. Similar verification standards have been used by the authors of [20] for a low impedance TRL calibration kit. The authors were able to achieve a source and load match uncertainty of better than -45 dB and -52 dB respectively from 0.85 to 3 GHz, which indicates a good measurement uncertainty.

Figure 2.12 shows a graphical interpretation of the measurement uncertainty on a Smith chart. The radius of uncertainty is determined using verification standards and is known to stay constant over all impedance points. Such an uncertainty has a small impact on the measurement accuracy in the centre of the Smith chart, but a much greater impact is found near the high

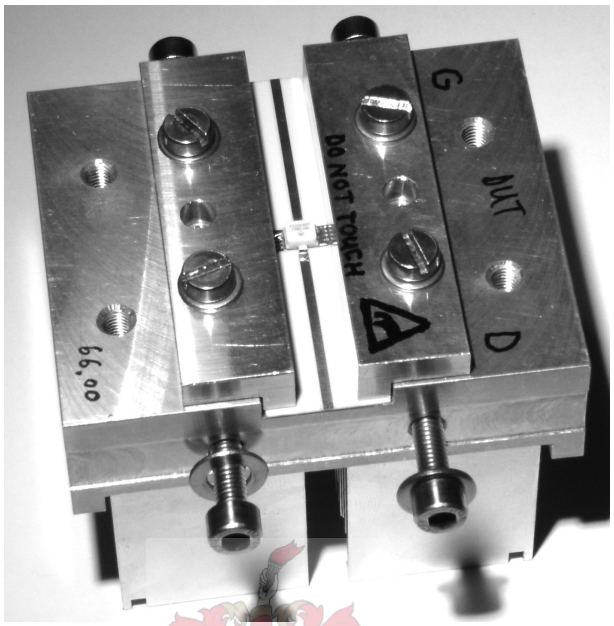


Figure 2.10: The MRF282 LDMOS power transistor on a PCB is mounted onto the DUT block.

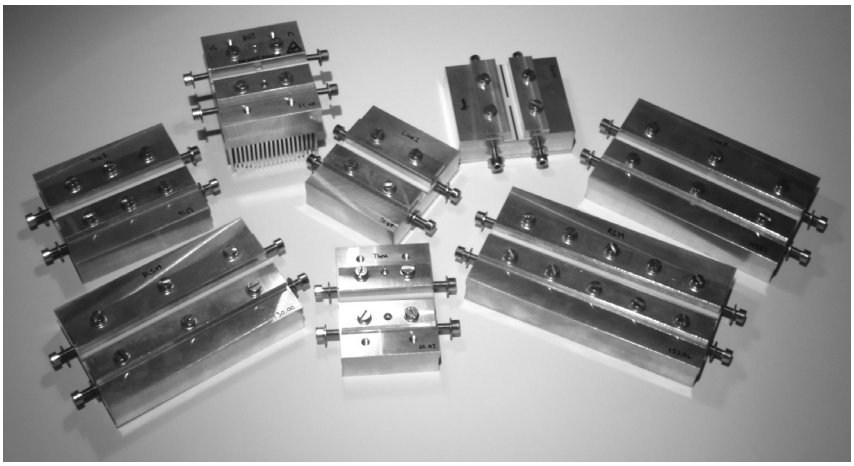


Figure 2.11: The completed TRL calibration kit consists of five calibration standards, two verification standards and a DUT.

reflectivity regions. Because unmatched transistors generally have highly reflective inputs and outputs, it is important that the radius of uncertainty is kept as small as possible.

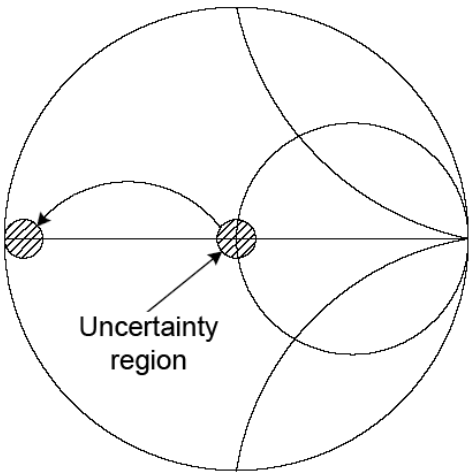


Figure 2.12: Measurement uncertainty is represented by circles with constant radius anywhere on the Smith chart. The magnitude of the measurement uncertainty has a much greater influence near the high reflectivity regions of the Smith chart.

Two verification standards [20], residual load match (RLM) and residual source match (RSM) standards, are designed and manufactured. These standards are not the only type of verification standards available, but provide a sufficient indication of the measurement uncertainty and are easy to manufacture on microstrip. The load match standard consists of a long transmission line with the same characteristic impedance as the previous calibration standards. The minimum line length of the RLM standard is designed to be at least quarter wavelength at the maximum frequency. The source match standard also consists of a long transmission line, but the one end of the line is terminated with a short circuit to ground so that extremely high reflection can be obtained. Equations (2.2.3) and (2.2.4) are used to calculate each of the measurement uncertainties where $|S_{11}|_{max}$ is the maximum measured amplitude of S_{11} for the RLM standard and Δ is the peak-to-peak amplitude in dB of the sinusoidal ripple observed in $|S_{11}|$ of the RSM standard.

$$RLM = |S_{11}|_{max} - 6dB \tag{2.2.3}$$

$$RSM = 20\log\left(\frac{1-10^{\frac{-\Delta}{20}}}{1+10^{\frac{-\Delta}{20}}}\right) dB \tag{2.2.4}$$

The measured reflections plotted in figure 2.13 are used to determine that a source match uncertainty of better than -45 dB and load match uncertainty of better than -40 dB between 0.4 and 8 GHz can be obtained. The worst of the two measurement uncertainties is used to define the

measurement uncertainty of the TRL calibration kit. The developed microstrip TRL calibration kit can therefore perform the characterisation of the MRF282 transistor with a measurement uncertainty of better than -40 dB over a bandwidth between 0.4 GHz to 8 GHz.

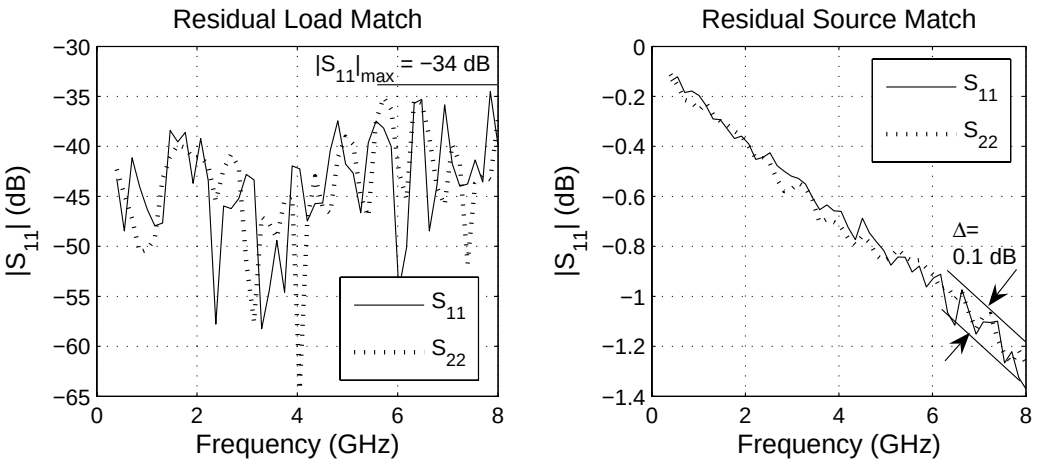


Figure 2.13: Measured $|S_{11}|$ for the residual load and sourch match standards. The indicated $|S_{11}|_{max}$ and Δ are used to calculate the measurement uncertainty.

2.3 Low Reflection Coaxial to Microstrip Transitions

Removable coaxial to microstrip transitions provide a convenient method for interchanging microstrip calibration standards. To successfully implement the transitions some precaution should be taken since the quality of the transitions directly influences the accuracy of the calibration. Many improvement techniques already exist in the literature. The authors of [21] designed and tested a coaxial to microstrip transition that has an input reflection of less than -46 dB. The described techniques are adapted and used to create an improved transition with a low input reflection as well as mechanical advantages.

2.3.1 The Coaxial to Microstrip Transition

Figure 2.14 shows what a standard coaxial to microstrip transition looks like. The coaxial structure consists of a Teflon cylindrical dielectric with a centre pin. The one side of the centre pin is attached to a coaxial connector, while the other side is pressed onto a microstrip track. The structure is implemented into a robust aluminium mounting piece as shown in figure 2.15. The mounting piece can be attached to separate aluminium calibration standard blocks and the structure also allows for variations in height and length in the blocks. Two strong bolts on each side of the standard blocks, shown in figure 2.10, are used to attach the mounting pieces. The blocks are designed so that the attachment pressure is concentrated near the transitions. The aluminium blocks and mounting pieces are coated using alludine to inhibit corrosion and to enhance surface conductivity.

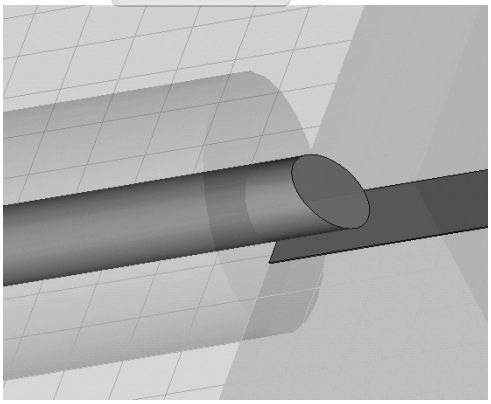


Figure 2.14: Simple coaxial to microstrip transition structure in CST Microwave Studio. The copper, free space and dielectrics are defined as solid structures.

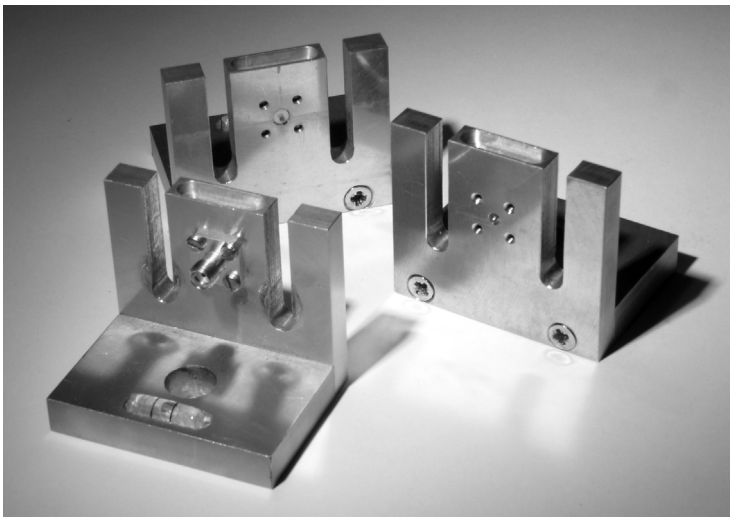


Figure 2.15: Aluminium mounting pieces that incorporate the coaxial to microstrip transitions. The connector tab sticks out so that it can be pressed onto a microstrip calibration standard.

2.3.2 Optimal Connector Tab

The first discontinuity area is where the connector tab makes contact with the microstrip transmission line. The connector tab must be carefully constructed to minimise parasitic elements introduced by the discontinuity. Time domain measurements in [22] reveal that the tab generally has the effect of a shunt capacitor to ground. The capacitance is concentrated near the tip of the tab. This is due to higher field concentration where there are sharp edges. A good mathematical model for the coaxial to microstrip transition is derived in [23].

The optimal connector tab is described in [21] to be only 0.65 mm long. The tab is angled similar to the tab in figure 2.14. Additionally the sharp edges are rounded off to avoid high field concentrations. It was found that the tab length could be slightly increased without causing a large degradation in the results. This allows the contact area to be enlarged slightly. The final tab shown in figure 2.16 is angled for approximately 0.5 mm of the total length of 0.7 mm. The tab is rounded and polished to minimise surface roughness.

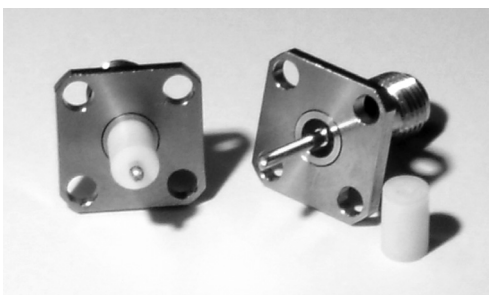


Figure 2.16: Photo of the 3.5 mm precision connectors with optimal tab. The Teflon extension fits securely into a mounting piece so that only the tab sticks out.

2.3.3 Improved Ground Continuity

The second discontinuity area is where the cylindrical ground of the coaxial transmission line meets the planar ground of the microstrip board. One of the problems found with low cost SMA connectors is that the Teflon dielectric can shift inside the connector when pressing against it. This causes an uncontrolled air-gap at the transition. The solution to the problem is to control the air gap. A round hole is machined into the fixture so that the hole diameter is smaller than the cylindrical Teflon dielectric. The hole diameter is designed so that the impedance remains 50 Ω as the dielectric changes to air. The Teflon can be seen in figure 2.17 to push against the walls of the air gap so that it is securely mounted.

The air gap provides the additional advantage of decreasing the discontinuity between the coaxial and microstrip ground planes. This results in a smoother transition between ground planes.

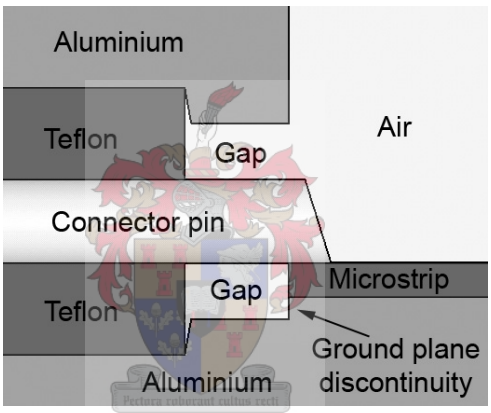


Figure 2.17: Side view of the coaxial to microstrip transition with an air gap in CST Microwave Studio with the different sections indicated.

2.3.4 3-D EM Simulation

The structures shown in figures 2.14 and 2.17 are simulated using the 3-D electromagnetic simulator CST Microwave Studio [24] to determine the transitions' S-parameters. The simulations for each transition are repeated several times with different mesh settings to determine the mesh density with the most reliable results. The structure is implemented in a lossless environment with resulting transmission of near unity ($|S_{21}| = |S_{12}| \approx 1$). The decisive output parameter is consequently the magnitude of reflection, $|S_{11}|$, with $|S_{22}| = |S_{11}|$.

The simulated $|S_{11}|$ for the standard and the new transition is plotted in figure 2.18. The reflection can be seen to be significantly less for the transition with the air gap, especially as the frequency increases. The improvement exeeds 10 dB at 8 GHz. Although simulations of such

sensitive nature cannot be trusted completely, the good results obtained suggested that the design should be implemented and further investigated.

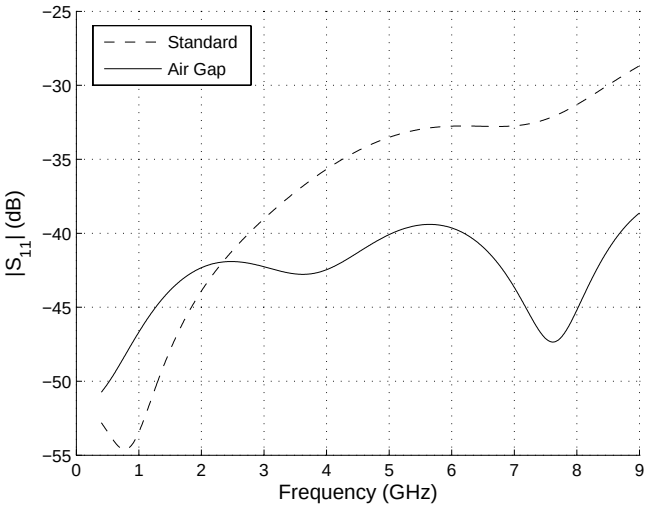


Figure 2.18: Simulated $|S_{11}|$ for two coaxial to microstrip transitions. The simulation compares the reflection of the standard transition with that of the new transition.

2.3.5 Time Domain Measurements

Low pass time domain measurements are performed to better illustrate the nature of the discontinuity at the coaxial to microstrip transition. Three different transitions were constructed and compared against each other. The first is a standard connection made with a SMA connector with extended Teflon. The second transition is made with an additional 3 mm long air gap. In the third construction the SMA connector used in the previous constructions is replaced with a 3.5 mm precision connector. Figure 2.19 illustrates the second measurement setup.

A coaxial SOLT calibration is performed on a HP8510C VNA over a bandwidth of 18 GHz using a 3.5 mm precision calibration kit. Time domain measurements are performed with gating applied so that only the reflection caused by the coaxial to microstrip transition remains visible. The response is plotted in figure 2.20 and indicates that in both transitions the dominant parasitic elements are series inductances and microstrip tracks with lower impedances than Z_0. The measurements have limited spacial resolution and the discontinuities are close to each other. What can be seen though is that the reflection is improved with the new transition and that series inductance is present.

Figure 2.21 shows the low pass step and impulse response for the transition with an air gap. The whole transition is included in the time gate, including the 3.5 mm precision connectors that add a minimal amount of additional reflection. The measurements reveal a small shunt capacitance close to the tip of the tab, but the reflection is still dominated by the microstrip

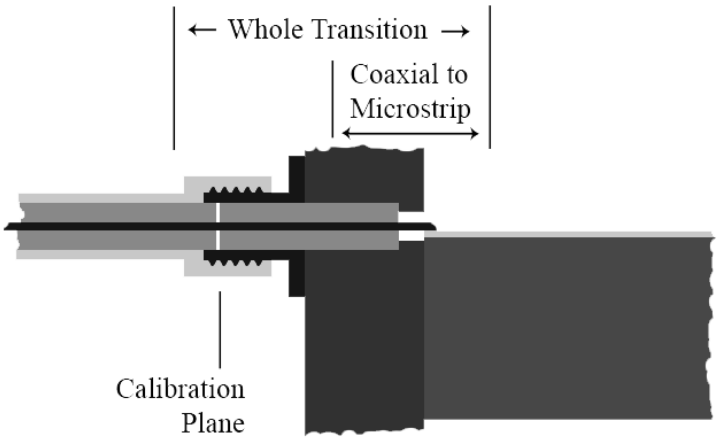


Figure 2.19: Side view of the air gap transition with indicated regions. Gating is applied to exclude the unwanted reflections.

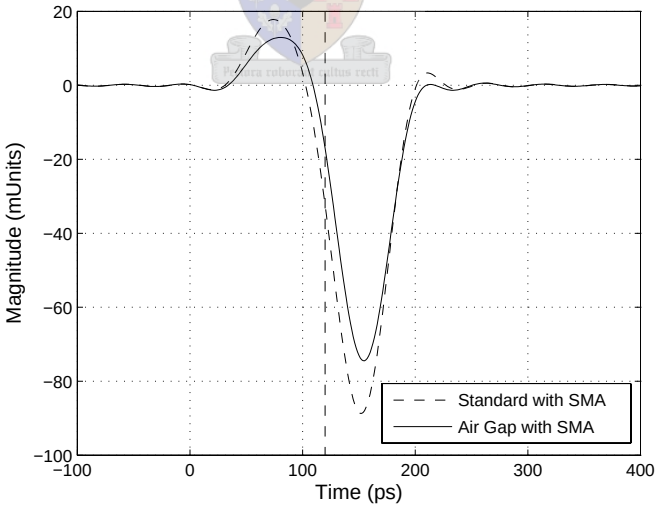


Figure 2.20: Time low pass impulse response for two different coaxial to microstrip transitions with the effects of the SMA connectors removed using gating. Reflections from the tip of the tab are situated at approximately 120 ps.

track having a lower impedance than Z_0. The lower impedance is due to the microtrip track having a width slightly larger than what is needed for $Z_0 = 50\Omega$. The revealed small shunt capacitance proves the existence of the parasitic capacitance described in [22].

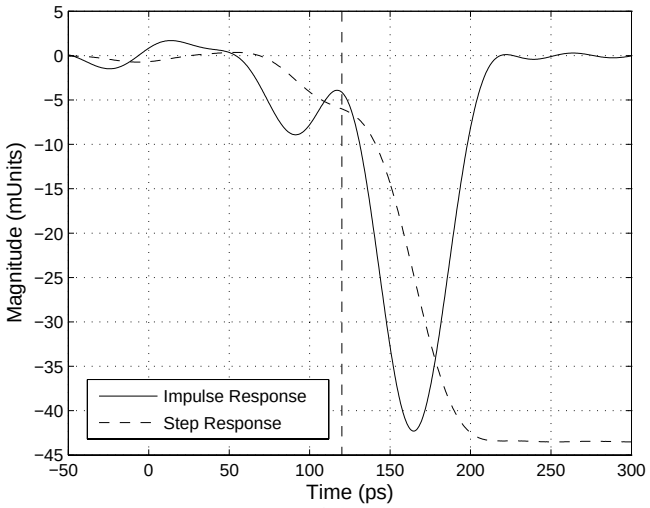


Figure 2.21: Time low pass step and impulse responses for the coaxial to microstrip transition with an air gap including the effects of the 3.5 mm precision connectors. Reflections from the tip of the tab are situated at approximately 120 ps.

2.3.6 Reflection Measurements

$|S_{11}|$ for the three different transitions is measured and plotted in figure 2.22. The standard transition has a reflection coefficient magnitude of -13 dB at 8 GHz. Because two transitions are used the reflection is 6 dB more, which adds up to a $|S_{11}|$ of -7 dB at 8 GHz. Such a large amount of reflection usually results in poor calibration accuracy. When the air gap is implemented, $|S_{11}|$ drops to -18 dB at 8 GHz. The largest improvement is however when the SMA connectors are replaced with 3.5 mm precision connectors. This causes $|S_{11}|$ to drop to -29 dB at 8 GHz, which is significantly lower than previous achievements. It can be seen in figure 2.22 that the resonant point for the SMA connectors is at 12 GHz. This causes the reflection to decrease for a small bandwidth, but then to increase sharply at frequencies above the resonant point limiting the usable bandwidth of the connectors.

Figure 2.23 shows the improvement in $|S_{11}|$ for each structure. The improvement in reflection when adding an air gap is more than 4 dB between 2 and 12 GHz. When a 3.5 mm precision connector is used, the improvement is found mainly between 4 and 10 GHz with a peak of 12 dB at 7 GHz. When both methods are implemented, the reflection is reduced by a total amount of 16 dB at 8 GHz.

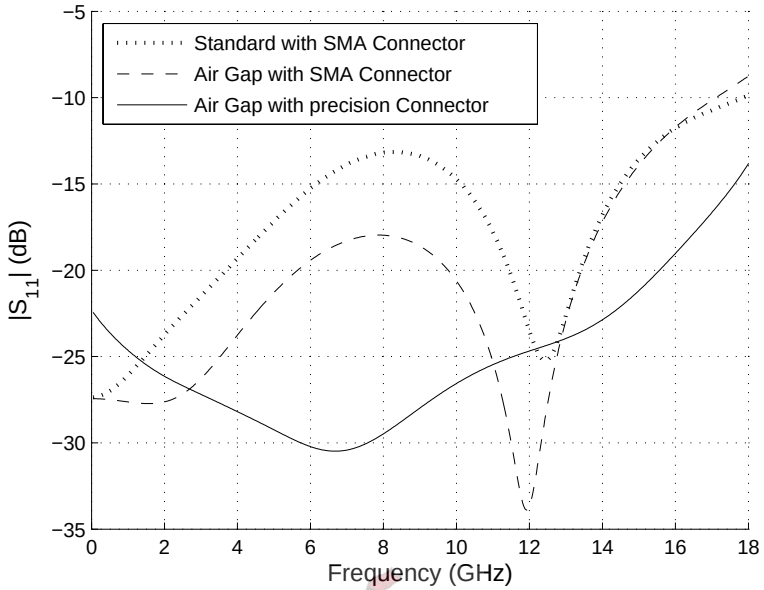


Figure 2.22: Measured $|S_{11}|$ for three different coaxial to microstrip transitions. Gating is applied to display only the reflections from one transition including the connector.

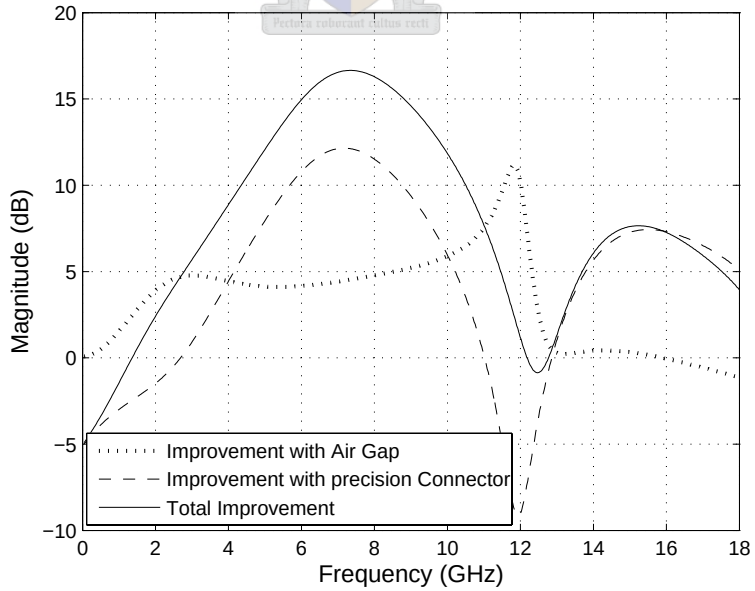


Figure 2.23: Measured Total Improvement in $|S_{11}|$ after modifications.

2.4 Conclusions

The known sources of TRL calibration error were investigated using an artificial TRL calibration kit in order to determine the calibration sensitivity for the different errors. It was found that the largest error could be prevented by manufacturing the lengths of the through and DUT standards as accurately as possible, and to ensure that the reflect standards are identical. Other important findings are listed below:

- The standards should be manufactured on the same sheet of laminate so that a minimum deviation in ϵ_r occurs between standards.
- A laminate should be chosen so that the effective permittivity stays sufficiently constant over the required bandwidth.
- Care should be taken so that the microstrip tracks have the same width and a very smooth etch-line.
- The standards should not be covered with any kind of conformal coating or silk screen, except when the high-frequency properties of the coating are well known.

A highly accurate multiline TRL calibration kit was developed to perform measurements on a 10 W LDMOS power FET. Calibration verification standards were added to the kit and the residual calibration errors were determined after calibration to be less than -40 dB between 0.4 and 8 GHz.

Different removable coaxial to microstrip transitions were investigated and two methods were found to reduce the reflection at the transitions. The first method implemented an air gap at the transition that minimised the discontinuity between the coaxial and planar ground planes. Not only did this provide a secure housing for the Teflon coaxial dielectric, but it also reduced the reflection between 2 and 12 GHz by more than 4 dB. A peak reduction of 11 dB was achieved near 12 GHz. The second method for lowering reflection was to replace the SMA connector with a high quality 3.5 mm precision connector. This improved the reflection with a peak of 12 dB at 7 GHz. The overall bandwidth of the transition was also increased by this modification. When both methods were implemented, the total reflection was reduced with a peak of 16 dB at 7 GHz, which lowers uniformly to 0 dB improvement at approximately 1 GHz.

The improved hardware developed in this chapter is used in the next chapter to characterise the MRF282Z LDMOS FET.

Chapter 3

Small-Signal Model Extraction

3.1 Introduction

After much care has been put into creating an accurate TRL calibration kit, there still exists the extraction of the small-signal model parameters before the large signal models can be constructed. Once again the accuracy of the large signal model depends strongly on the accuracy of the data from which it is constructed; in this case the small-signal model data. The aim is therefore to extract the small-signal parameters as accurately as possible.

Another aspect that comes into consideration is the amount of time that can be spent on extracting the small-signal parameters. When more than one device is to be modelled, the extraction time starts becoming an increasingly important factor. In a world where time equals money it is therefore crucial to work as time-efficiently as possible.

In the first part of this chapter the TRL calibration kit developed in the previous chapter is used to determine the S-parameters of the MRF282 LDMOS transistor. Because of the device's high output power capability, special care is taken to ensure the safety of the equipment. The use of highly specialised algorithms, implemented in Matlab, allows the extraction of small-signal model parameters in a fast, efficient and accurate manner. A series of GUIs are developed to allow the user to visually perform this extraction with a reduced amount of effort. The extracted model data is compared to a selected set of measured data and the accuracy of the extraction is thereby verified.

3.2 S-parameter Centroids

In this chapter S-parameter centroids are used for representing measured S-parameters as single impedance points. A S-parameter centroid is defined as the mean of the complex S-

parameter over frequency and is used conveniently to represent data over many frequencies as a single point. The centroid for an arbitrary S_{11} is shown in figure 3.1 and is indicated by the dot.

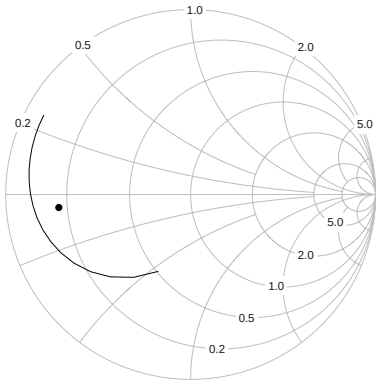


Figure 3.1: An example to show the centroid of an arbitrary S_{11} over frequency. The centroid of the curve is calculated as the mean of the complex S-parameter over frequency and is indicated by the dot.

3.3 Multi-Bias Stability Check

High power active devices have the capability to severely damage the input ports of the VNA. The threat is not as such during normal characterisation, because a very small signal is applied by the VNA, but is where the increased gain of the device at lower frequencies, and high port reflections in the absence of matching, enable the device to oscillate. It is therefore the device's ability to oscillate that poses a threat to the equipment.

In order to avoid such an incident to occur, a device needs to be thoroughly tested while using the exact same setup as what is going to be used during characterisation. It must be considered that the gain of an active device usually varies for different bias conditions. It is therefore necessary to test a device's stability over the required bias range. This is done by terminating the input of the device with a 50Ω load and monitoring the output port with a spectrum analyzer (SA). Enough attenuation is added between the device and the SA to ensure the safety of the SA. The attenuators must be removed again, before the device characterisation can be performed, because the dynamic range of the VNA is critically reduced by the added attenuators. Another way of checking a device's stability is to monitor the current consumption of the device. Any unusual fluctuations in the current also indicates that the device is busy oscillating. Measured IV curves should reveal such peaks.

The algorithm in [25] is modified to take DC and SA measurements in the safe operating area (SOA) of the MRF282 so that the stability of the device can be determined over its bias range.

The SOA is determined by the algorithm using a set of user-defined maximum allowed bias values for the device. The algorithm sweeps over a user-defined set of voltage bias points, while ensuring the safety of the device by checking that each bias condition falls within the SOA. The available HP4141 programmable PSUs restricted the voltage ranges from $0 - 20V$. A voltage bias range between $0 - 16V$ for V_{gs} and $0 - 20V$ for V_{ds} was therefore defined, using the bias restrictions of the PSUs and the voltage, current and power ratings of the device. The PSUs are controlled using the automated algorithm implemented in Matlab to sweep over a user-selected set of voltage bias points. Two grids are defined by the algorithm for each of the gate and drain bias voltages. The first grid is called the user grid and consists of user selected bias points. The second grid is called the fine grid, and consists of an evenly distributed mesh of the finest voltage steps that are allowed to take place. Each selected bias point is forced to fall onto the fine grid. This prevents the redundant selection of bias points closer than a ΔV to each other. The software uses a prediction algorithm to predict the current and thereby calculate the power dissipation before each measurement on the user grid takes place. Each bias point is verified by the software to be within the SOA of the device before the bias is applied accordingly. The algorithm considers the change in the slope of the current from previous measurements to decide whether a prediction can be trusted. If a prediction lies outside the SOA, the algorithm chooses between one of two options. If the prediction is trusted, the algorithm attempts to extrapolate to the boundary of the SAO. If the prediction is not trusted, the algorithm uses the fine grid to step a small step of ΔV closer to the boundary. This is repeated until the stability has been evaluated at all of the user-selected bias points.

The algorithm is executed and the measured DC IV curves can be seen in the left hand side of figure 3.2. No unusual fluctuations in the current can be seen. Due to the voltage limitations of the PSUs the MRF282 never comes close to any of its unsafe operating conditions here. The whole bias range is therefore within the SOA. The overlaid output spectrum for each of the measured bias points is shown in the right hand side of figure 3.2 for a frequency range of 0-500 MHz. It can be seen that no power is generated above the noise floor and that the device is therefore not oscillating at any of the measured bias points.

3.4 Device Characterisation

After no oscillations have been detected, the SA, input termination and attenuators are removed and the device test setup is connected to a VNA. The photograph in figure 3.3 shows what the characterisation test setup looks like. The HP8510C VNA in the middle of the figure is used to perform the characterisation, while HP6612C power supplies in the right hand side are used for sweeping the gate and drain voltages using a PC. The device test fixture can be seen in the bottom left corner of the figure.

An adaptive multi-bias S-parameter measurement algorithm [25], implemented in Matlab, is

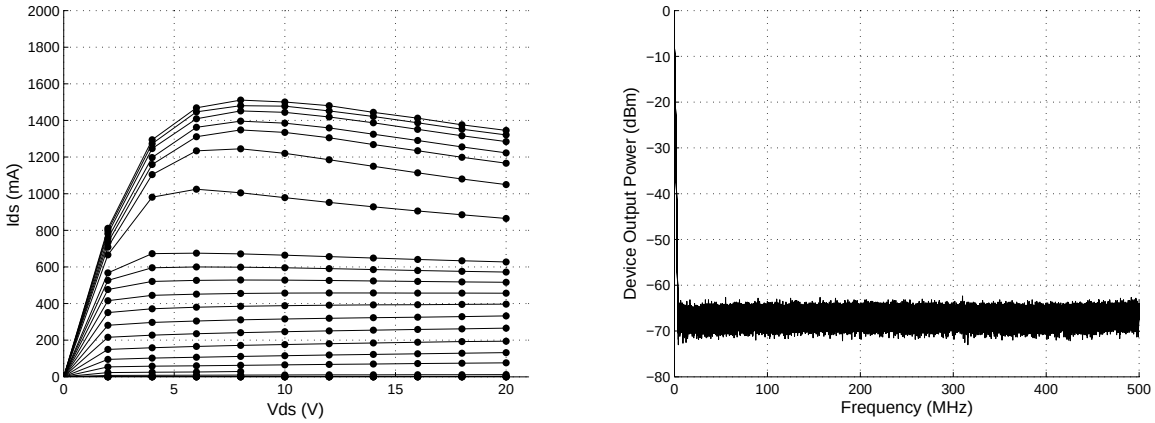


Figure 3.2: Measured DC IV curves and overlaid output spectrum for the MRF282 LDMOS transistor over the whole bias range. The output spectrum is monitored at each DC bias point (indicated by a dot) to verify the device's stability. Smooth current distribution in the IV curves, and no significant output power measured by the SA suggest that device oscillations are not present.

Figure 3.3: A typical automated test setup using a HP8510C VNA to perform the characterisation. The HP6612C power supplies in the right hand side of the figure are used for sweeping the gate and drain voltages using a PC.

used to perform the device characterisation so that a minimum amount of user intervention is required. The algorithm first allows the characterisation of the device at a number of user-selected bias points similar to the bias points used for the stability check. Bias regions are then identified by the algorithm where certain device characteristics are changing rapidly, and an user-specified number of new bias points are added in these regions. The criteria for selecting these bias regions is based on DC and S-parameter measurements. New bias points are added in the regions where the S-parameters of the adjacent bias points have the largest distance between their centroids. A denser distribution of S-parameter measurements is therefore found where the S-parameters of the device change more rapidly. For the DC selection criteria, the currents are calculated at each of the fine grid points, using firstly linear, and secondly cubic spline interpolation algorithms. New bias points are added where the difference between the calculated currents from each interpolation algorithm is the greatest. By using this adaptive measurement algorithm, the characterisation time is kept low, while still collecting enough data so that an accurate model can be constructed.

After a total measurement time of approximately four hours, 1026 measured S-parameters was collected. The distribution of the bias points can be seen in figure 3.4. A higher density of bias points are found in the areas where changes occur more rapidly inside the LDMOS transistor. These areas are identified where the transitions between the linear, saturated and pinch-off regions of the device occur. It can also be seen that more points are added where the DC I_{ds} of the device starts saturating for higher V_{gs} values.

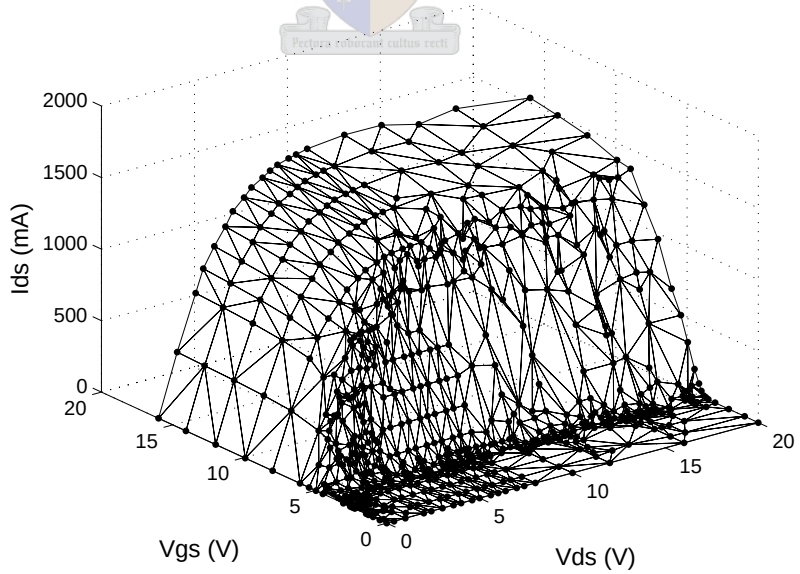


Figure 3.4: Measured 3-D IV curve for the MRF282, using the adaptive multi-bias S-parameter measurement algorithm. S-parameter measurements were performed at each of the indicated dots.

3.5 Intelligent Bias Point Selection

Before the extraction of the extrinsic small-signal model parameter values can be performed, a suitable smaller set of S-parameters must be selected from the 1026 available S-parameters. If a large number of S-parameters are used for the extrinsic model extraction, the extraction time increases significantly without improving the accuracy. Once the extrinsic parameter values have been obtained, all of the measured S-parameters can be used to perform the extraction of the intrinsic small-signal model parameters. The small-signal model topology that is used for the extraction can be seen in figure 3.5. The extrinsic model elements are shown outside the dotted box, while the intrinsic elements are shown on the inside. A GUI is implemented to allow the user to visually perform the selection of a suitable set of S-parameters and the selection of bias points is divided into two groups: cold and hot bias points. The algorithms used for selecting points for each of the groups are discussed in this section.

The first algorithm selects a specified number of cold measurements. This selection contains S-parameters measured under cold bias conditions so that V_{ds} is kept at $0V$ and V_{gs} below the pinch-off voltage. When a FET is biased under these conditions the intrinsic part of the small-signal equivalent circuit in figure 3.5 reduces [26] to only the three intrinsic capacitors C_{gs}, C_{gd} and C_{ds}. This deduction provides valuable information when performing the extraction. The selection algorithm scans through the list of bias points available and selects the S-parameters measured under cold bias conditions. The specified number of points are selected in sequence starting from the lowest V_{gs} value upwards.

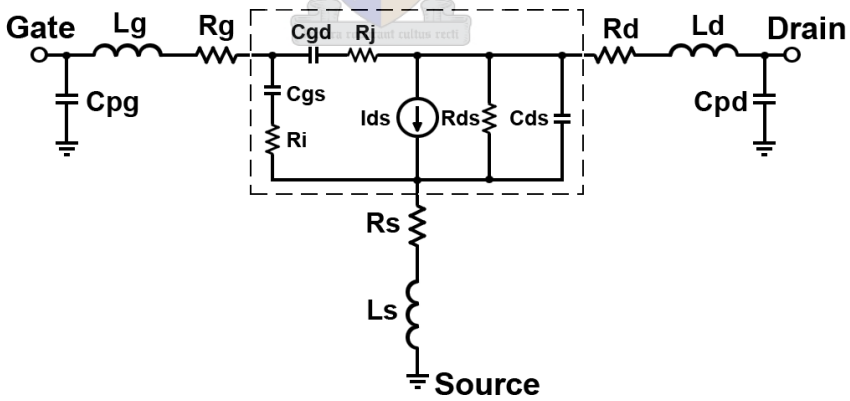


Figure 3.5: The 15 element small-signal FET model. The extrinsic model elements are shown outside the dotted box, while the intrinsic elements are on the inside.

The second algorithm [26] selects a specified number of hot bias points. This means that the device is switched on, and that all 15 elements of the model are therefore relevant. A good selection of S-parameters strongly improves the ability of the extraction algorithm to converge. The performance of this selection algorithm is therefore crucial to accurately extract the model's element values. The GUI used for the selection is shown in figure 3.6. There are four filter

parameters that allow the user to specify a region in which S-parameter selection can take place. A value between 0 and 1 can be selected for the first three filter parameters, where a value of 1 is the strictest and a value of 0 removes the filter. The fourth parameter is the allowed power consumption value, specified in Watts. The user-specified number of bias points allows that only a few bias points can be selected for performing the parameter extraction. The affected areas for each of the filters are shown in figure 3.7.

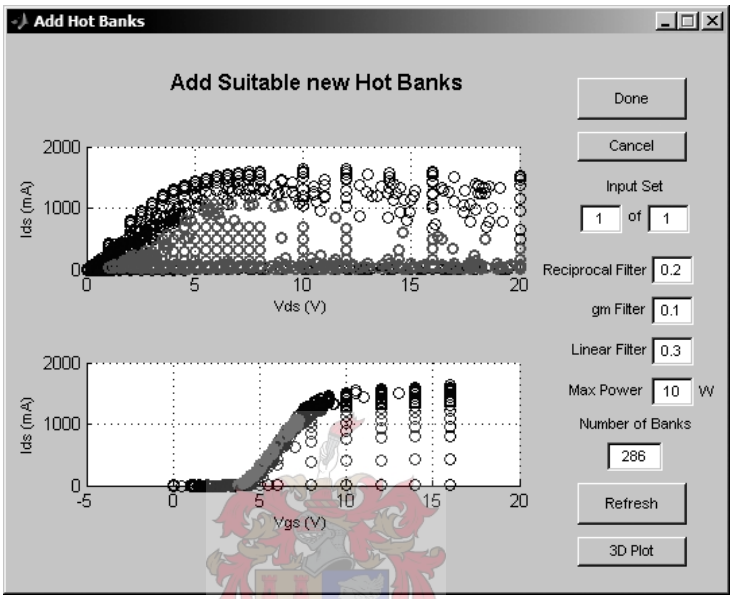


Figure 3.6: GUI for selecting suitable hot bias points. Four variable parameters allow the specification of a suitable region, indicated by the gray circles. The black circles indicate the bias points that fall outside the suitable region.

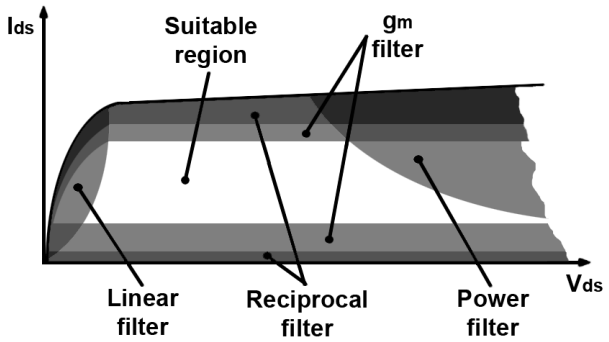


Figure 3.7: Each of the filters allow the exclusion of certain regions of bias. The typical areas affected for a LDMOS device are indicated on the IV curve for each of the filters.

The first filter parameter is called the reciprocal filter. This filter enables the selection of S-parameters that display a certain percentage of nonreciprocal behaviour where the device has low gain. The behaviour is quantified by the difference between S_{21} and S_{12} and the filter is necessary to ensure that every S-parameter provides the maximum amount of information

to the extraction algorithm. The reciprocity factor R is calculated using (3.5.1) and the cutoff value for reciprocity is calculated by multiplying the user-specified fractional value with the maximum calculated reciprocity factor R_{max}

$$R = |C_{21} - C_{12}| \tag{3.5.1}$$

where C represents the centroid of the S-parameter.

The second parameter is labelled the g_m filter, which controls the amount of filtering by limiting the variation of the DC transconductance of the device. This allows the selection of bias points with a specified fraction of nonreciprocal behaviour where the device has high gain. The bias points are discarded where the DC transconductance of the device is below the user-specified fraction times the maximum DC transconductance.

The third user-parameter is the linear filter. This filter allows the exclusion of bias points taken in the linear region of the device for low values of V_{ds}. The reason for excluding such points is because of the low R_{ds} values that make the determination of the intrinsic elements difficult. The S_{22} data in this region also show largely inductive behaviour in this region that leads to overestimation of the parasitic inductors L_d and L_s. The method described in [26] monitors S_{22} and identifies points in the linear region where the corresponding S_{22} enters the inductive region of the Smith chart. This method works for small devices where the inductance of the extrinsic elements are relatively small. Unfortunately this method cannot be used for larger devices. Figure 3.8 shows what S_{22} for the MRF282 typically looks like when the device is switched on.

A new method is introduced to filter out the points in this region. The method is tested on the small CFY-30 GaAs FET and on the MRF282 LDMOSFET and is found to be effective in both cases. The filtering is done by using only the lowest frequency points of the S_{22} data available. These points are indicated in figure 3.8 as black dots. It can be seen that the real values for these points are distributed from close to the short circuit region of the Smith chart up to almost the centre of the chart (50Ω). The algorithm uses the real values of these points to perform a linear selection between 0 and 1. A value of 0 is awarded to the minimum measured real value and a value of 1 to the maximum measured real value. The points in between, with a calculated value below the user-specified fraction of linear filtering, are discarded. If, for instance, a fraction of 0.3 is specified, 30% of the points with the lowest real values will be discarded.

The fourth filter criteria is the amount of power allowed to be dissipated by the device for each bias point. This criteria allows the user to discard the points where self-heating is strongly present. Some of the parameters of the device are known to change over temperature and this is undesired when extracting the extrinsic elements. The typical region of high power can be seen in the right hand side of figure 3.7.

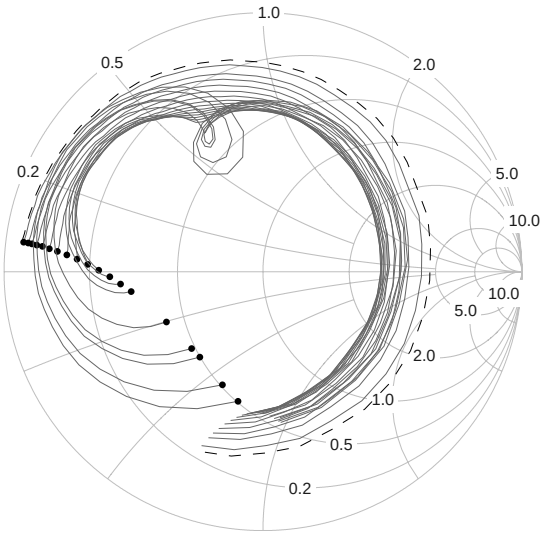


Figure 3.8: The new linear filter uses the measured real values of S_{22} at the lowest frequency point to determine the cutoff criteria. Each arc illustrates a single bias point of S_{22} over frequency where $V_{gs} = 8V$ and V_{ds} is swept from 0 V (dotted arc) up to 20 V. The dots indicate the starting points in frequency (400 MHz) for each arc.

The GUI in figure 3.6 allows the user to generate a 3-D IV plot to better indicate the selected suitable bias points, which can be seen in figure 3.9. There are still too many points selected for performing optimisation-based parameter extraction. A good set of bias points should only include about 10 cold bias points and 10 hot bias points. The number of selected hot points to be selected is specified by the user and the method in [26] is used to select the correct number of points, with their centroids as far from each other as possible. This ensures that the maximum amount of information can be extracted from the small set of selected S-parameters.

3.6 Robust Optimisation-Based Extraction of Extrinsic Elements

When performing parameter extraction, the extrinsic parameter values are determined first. These parameters are defined as the parameters that hold constant values over bias. The determination of the values can be performed using one of two different methods. In the first method, the transistor package is characterised separately after obtaining empty packages from the manufacturer. Modelling procedures described in [27] and [28] show that good results can be obtained this way. This approach is especially attractive for high power devices because it is usually difficult to extract their package parasitics at higher frequencies. However, it is sometimes not possible to obtain empty packages from the manufacturers. The alternative approach is to perform robust multi-bias optimisation-based parameter extraction [29, 26, 30, 31] to compute the values of the extrinsic elements. The intrinsic element values are then com-

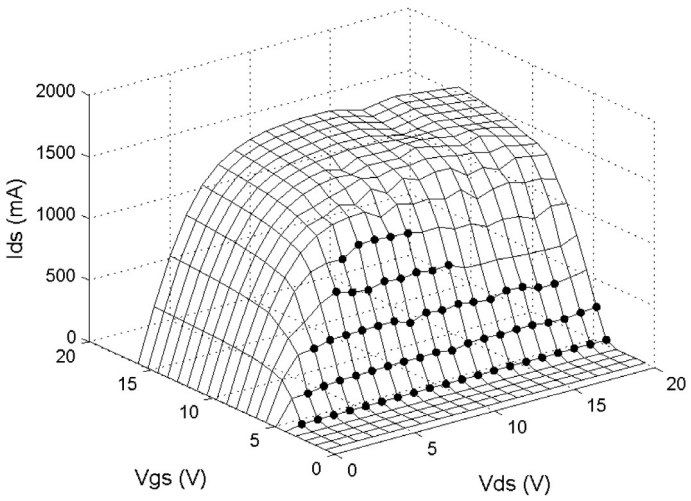


Figure 3.9: A typical selection of bias points on a 3-D IV mesh for the MRF282. The indicated points represent the suitable selection.

puted afterward using a direct extraction method so that the total amount of extraction time is kept low. This method is chosen to perform the extraction of the extrinsic elements of the MRF282.

The robust multi-bias optimisation-based parameter extraction is performed using the program pcFET [32]. The extraction algorithm is robust so that it is independent on parameter starting values. The algorithm calculates an error function from all of the small-signal model parameter values continuously, until one of the user-specified termination criteria for the optimiser is met.

The program uses text configuration files to allow the user to pre-configure the extraction process. The formal configuration procedure for these files can be found in [33]. A GUI is designed to create an user-friendly interface to the configuration files and is shown in figure 3.10. A number of properties can be altered using the GUI for each of the 15 elements and a detailed discussion of the properties can be found in [33]. Each element contains a field in which a parameter value can be specified. The extrinsic element values are updated after each extraction so that the user can monitor the extraction results. The parameter limits are fixed between 0.01% and 400% of the specified parameter values, and are used to limit the parameters within a reasonably wide range. The fix buttons in figure 3.10 allows the user to fix an extrinsic parameter value. This is particularly useful when a parameter is known and the user wants to prevent the extraction algorithm from changing the parameter value. The cold banks buttons are used to specify whether an extrinsic parameter should be determined using only cold measurement data. Certain elements such as R_d and R_s become more dominant [26] under cold bias conditions. These two elements also become more dominant at the upper measurement frequencies. That is why the frequency range can be specified for each element. The combined fix and cold banks buttons for the intrinsic parameters allow the fixing of the specified element values dur-

ing cold bank extraction. This is useful for instance with R_{ds}, which becomes infinitely large when the device is switched off. With very small values of g_m, τ also becomes meaningless and is fixed to zero if the button is enabled. Other parameters include the specification of the total DC resistance of the combined bias-T and power cables at the drain side of the device so that the voltage drop between the power supply and the transistor can be calculated. To estimate parameter values the GUI allows the user to obtain values by performing direct extraction. The same direct extraction algorithms are used as what is described in the next section for the extraction of the intrinsic elements. All the extrinsic elements, except the parasitic capacitances, are calculated from cold measurement data and returned to the GUI. The direct extraction algorithm used is unable to deteremine the values of the two parasitic capacitances C_{pg} and C_{pd}. These capacitance values are usually in the high fF range and values must be guessed before using pcFET to determine more accurate values. The maximum values of the intrinsic elements are returned to the GUI to provide a higher value range for the intrinsic elements. The intrinsic parameter values usually vary a lot for different bias conditions and the user is required to perform minor intuitive adjustments to the values so that the boundaries are set up correctly.

Before performing the optimisation-based extraction the user can specify whether the command-line text of pcFET should be displayed in the Matlab command window. This featured enables the user to monitor progress in the command window. The New Hybrid option allows the user to activate search techniques that will be supported by newer versions of pcFET. The rest of the GUI parameters are used to configure the optimiser. The number of random searches specifies the number of times that the optimiser will repeat with random starting values for the elements. A greater amount of random searches improves the robustness of the extraction algorithm, because the optimiser can be monitored to converge to approximately the same values for each set of starting values. The seed number can be specified for the random number generator so that the same sequence of quasi-random numbers can be repeated each time. The termination change percentage specifies when the optimiser should terminate when the error function changes with less than the specified value for the specified number of iterations. The maximum number of iterations allows the optimiser to terminate after a specified number of iterations regardless of the other termination criteria. The frequency skip integer value specifies how many frequency points to skip between each measured frequency point for the S-parameters. The duration time for the extraction is decreased by skipping more frequency points, while the accuracy of the extraction is not necessarily negatively influenced by this.

The previously determined selection of S-parameters is now used to perform the parameter extraction of the extrinsic elements. The frequency range for the extraction is limited between 0.4 and 3 GHz due to poor results obtained for the intrinsic model when using higher frequency data. The poor results are suspected to occur because the small-signal model topology is not detailed enough to allow the accurate modeling of a large device correctly over such a wide frequency range. A model that works up to 3 GHz is sufficient in this case because the gain of the device is fairly low at this frequency. The extracted extrinsic parameter values are listed in

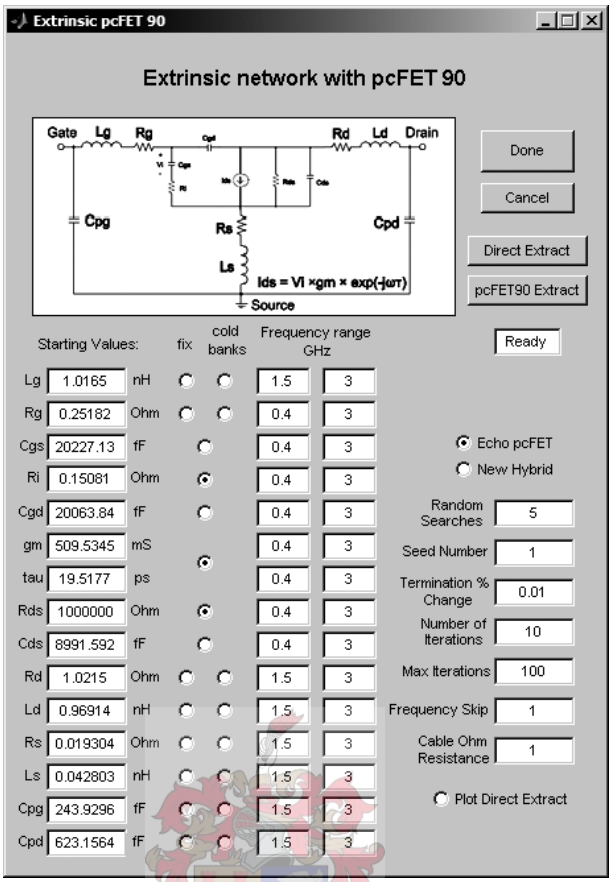


Figure 3.10: A GUI provides an user-friendly interface to the program pcFET. The program is used to perform parameter extraction of the extrinsic elements.

table 3.1.

Table 3.1: Extracted extrinsic parameters of the MRF282 between 0.4 GHz and 3 GHz.

Parameter	Value	Unit
L_g	1.017	nH
R_g	0.2518	Ω
R_d	1.022	Ω
L_d	0.9691	nH
R_s	0.01930	Ω
L_s	0.04280	nH
C_{pg}	243.9	fF
C_{pd}	623.2	fF

3.7 Direct Extraction of Intrinsic Elements

The small-signal equivalent circuit extraction is performed using direct extraction to compute the values of the intrinsic elements. A combination of the methods in [31] is used here to

perform the extraction. The extrinsic element values, calculated in the previous section, are used to de-embed the Y-parameters of the intrinsic model circuit. The intrinsic element values are then calculated using the equations proposed in [34], and a Gauss-Newton optimiser is used to optimise the intrinsic parameter values so that the modelled data are optimally fitted on the measured data. This type of optimisation does not consume a large amount of time because the calculated values are already close to the optimal values. The extraction software used here was programmed by van Niekerk [35] using Matlab.

A GUI is also used here to allow the user to set certain options. The extraction of R_j can be enabled or disabled. The user can thereby decide whether this element should be included in the small-signal model or be set to zero. The clipping of τ can be selected so that τ is set to zero where g_m is lower than 20% of its maximum value. The capacitances can also be clipped so that negative capacitance values are set to zero. This option can be set depending on whether the large-signal model implements nonlinear capacitors or nonlinear charge sources. Different plots can also be selected so that the user can view 3-D representations of each extracted intrinsic element. The extraction is performed with R_j excluded due to the circuit topology of the Fager large-signal model to be used in the next chapter. The extracted g_m and G_{ds} for the MRF282 are plotted in figure 3.11.

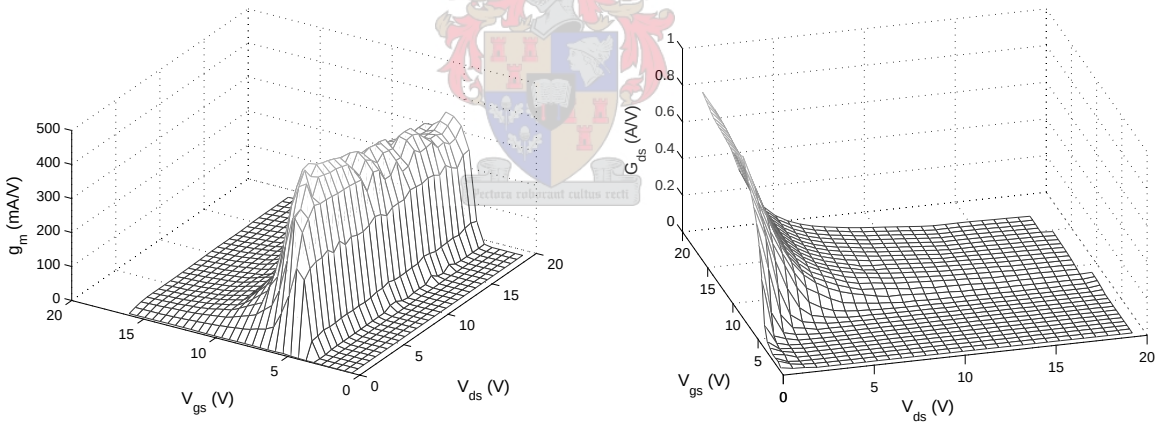


Figure 3.11: Extracted g_m and G_{ds} for the small-signal model of the MRF282 as a function of voltage bias.

3.8 Extraction Verification

The quality of the extraction is verified in the sub-threshold, quadratic and linear regions of I_{ds}. The regions are represented by different values of gate bias and are discussed in detail in the next chapter. The small-signal equivalent circuit's S-parameters are calculated and compared to measured data in each of the regions, and are shown in figures 3.12-3.14. It can be seen that a reasonably good fit exists in all of the regions and the simplicity of the small-signal model is

accountable for the small differences between the modeled and measured data. Expansion of the small-signal model topology in the future should improve the model's ability to accurately predict the measured data over a wider frequency range.

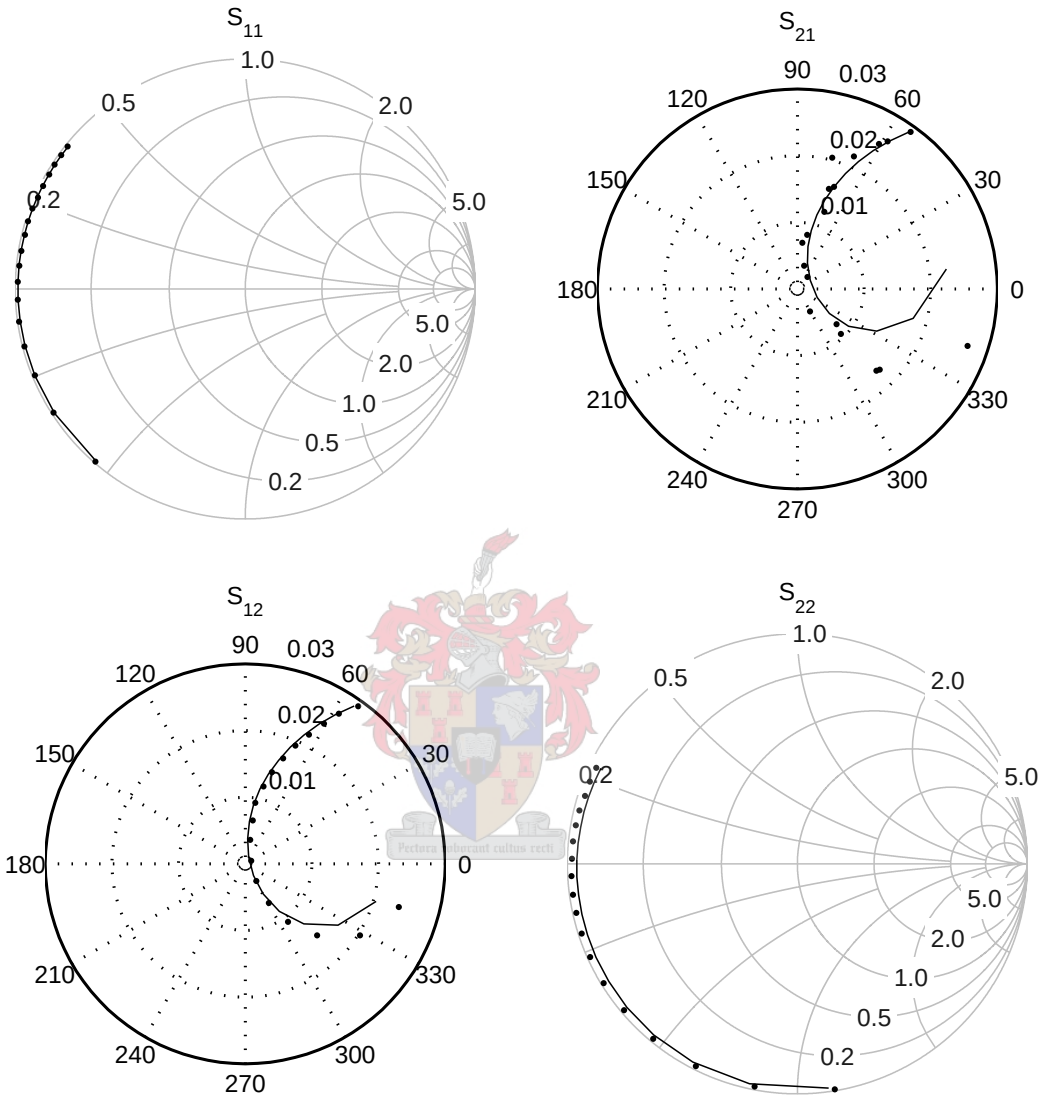


Figure 3.12: Small-signal S-parameters of the MRF282, verified at $V_{gs} = 2V$ and $V_{ds} = 20V$ from 0.4-3 GHz. The dots indicate the measured data.

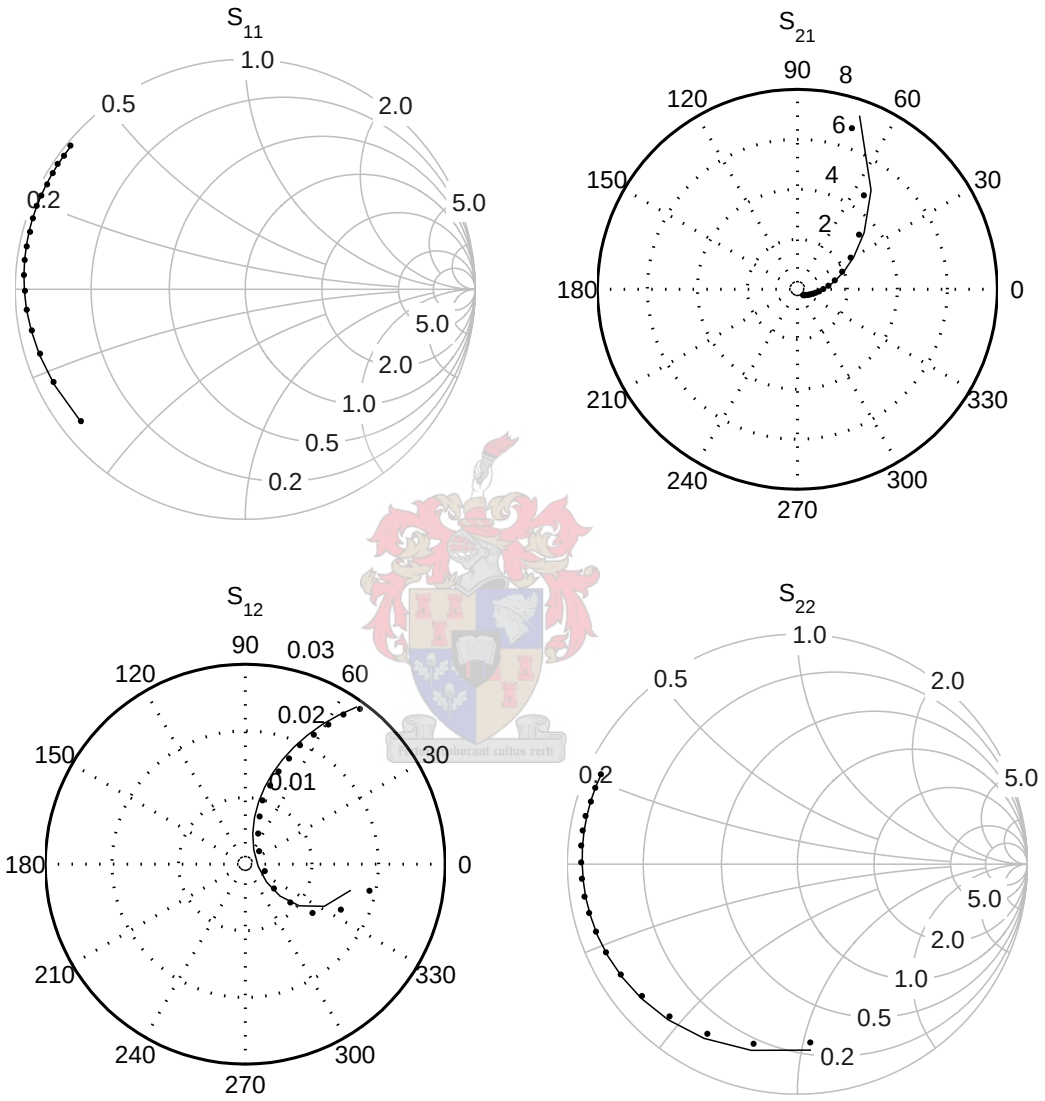


Figure 3.13: Small-signal S-parameters of the MRF282, verified at $V_{gs} = 4.2V$ and $V_{ds} = 19.92V$ from 0.4-3 GHz. The dots indicate the measured data.

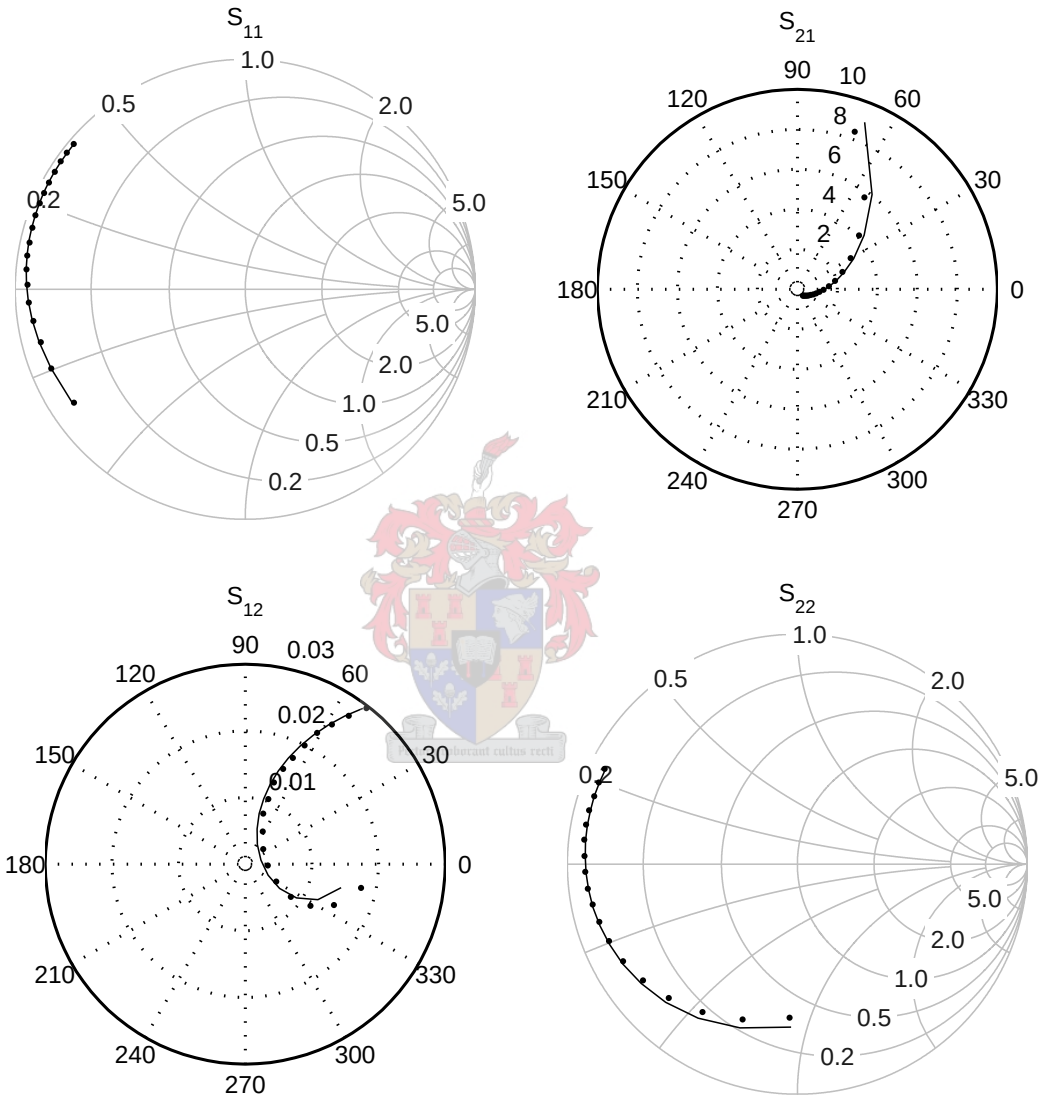


Figure 3.14: Small-signal S-parameters of the MRF282, verified at $V_{gs} = 6V$ and $V_{ds} = 15.33V$ from 0.4-3 GHz. The dots indicate the measured data.

3.9 Conclusions

The stability of the MRF282 LDMOSFET was determined using the test fixture developed in the previous chapter. The input of the device was terminated with a 50Ω load and SA measurements on the output revealed that the device is stable for all the relevant bias conditions.

The device was characterised using a VNA controlled by previously developed adaptive bias measurement software. 1026 measured S-parameters were obtained after approximately 4 hours of automated measurements. A denser distribution of S-parameters was acquired in areas where changes occurred more rapidly inside the device. These areas were identified where the transitions between the linear, saturated and pinch-off regions occurred.

A series of GUIs were developed to aid the user in performing parameter extraction. One of which helps the user determine a suitable selection of S-parameters measured under hot bias conditions. The selection algorithm allows the specification of certain filters so that the S-parameters containing the most valuable information can be selected for extracting the extrinsic element values. The values were determined using a starting-value-independent optimisation-based parameter extraction program. The extrinsic elements were used to perform the extraction of the small-signal equivalent circuit for each of the 1026 measured bias points. The complete extraction of the model could be performed within minutes due to the high time-efficiency when using this method.

The extracted small-signal data were evaluated and graphs were shown to illustrate that the model was sufficiently accurate in the three most relevant regions of bias. The small-signal model data are used in the next chapter to develop a large-signal model that is capable of modelling the linear, as well as the nonlinear behaviour of the device.

Chapter 4

LDMOS Large-Signal Nonlinear Models

4.1 Introduction

In the previous chapter the small-signal model parameters were extracted at each of the measured bias points. In this chapter large-signal models are described that transform the large amount of small-signal parameter values into single sets of model parameter values. A large-signal model is able to predict the behaviour of the device under more than one bias condition and also have the capability of predicting the DC and nonlinear behaviour of a device for different levels of input power. A good nonlinear model allows the design of complex linear amplifiers so that basic operation, and performance aspects such as IMD, can be accurately predicted.

A number of LDMOS model topologies were considered [36, 37, 38, 39] for the modeling of the MRF282 and the model equations published by Fager [36] was chosen to be implemented. The Fager nonlinear drain current equation have an improved capability to predict IMD in LDMOSFETs. The Fager model is implemented and a GUI is developed for the determination of the nonlinear model parameter values. The modeling of thermal effects [40, 41, 37, 42, 43, 44] has not been included in the scope of this study due to the necessary equipment not being available.

The nonlinear charge at each port is computed using a method that allows for charge conservation. An improved Fager model is constructed using equations that are derived from the voltage-derivatives of the nonlinear charge, and the Fager drain current equations. Another GUI is developed for the determination of the nonlinear parameter values for the improved model.

The original Fager and improved Fager models are implemented in Microwave Office using the Nonlinear Model Wizard. The Nonlinear Model Wizard allows the user to generate C++ code for the models, that can be compiled into a dynamic link library (DLL) file for use in Microwave Office. Some of the models' parameters are tuned in Microwave Office so that better small-signal performance is obtained.

4.2 Nonlinear Modeling

There are three main modeling approaches [1] when describing the non-linear behaviour of a device. The first approach is physically based modeling that describes the active device in terms of the motion of charge carriers and geometrical characteristics. The solving of the physically based equations produces the voltages and currents at the ports of the device. Although this method provides valuable insight into the operation of the device, solving the physical equations is extremely time-consuming and impractical for most cases. The second approach is black box modeling. This method allows a device to be represented by a behavioural input/output model, where no insight is required on the physical operation of the device. This method requires a transfer function that is ideally capable of representing any type of nonlinear behaviour and usually contains more complexity than what is necessary. The third approach is empirical equivalent circuit modeling and is the most widely used type of modeling. Equivalent circuit models usually consist of a number of linear and nonlinear elements. The nonlinear elements may be two-terminal devices, or may be current or charge sources controlled by one or more voltage or current. A good equivalent model topology, in addition to being physically meaningful, usually provides an excellent match to measurements over a reasonably wide frequency range. The empirical equivalent circuit modeling approach is therefore used in this chapter.

There are three common problems [45] in this type of modeling. The first problem is that the large-signal simulations do not fit the imaginary parts of the Y-parameters over different bias. The solution is to replace the two-terminal nonlinear capacitors with nonlinear voltage controlled charge sources (VCQSs). A VCQS is the reactive analogue of the familiar voltage controlled current source and can be dependent on more than one control voltage. The imaginary parts of the Y-parameters can therefore be modeled more accurately over bias. Linearising of the VCQS also produces a transcapacitance, which is the reactive analogue of the transconductance g_m. The second problem is that the large signal models do not simulate time delays. The transcapacitance produced by the VCQS element provides a reactive output current that implements the effect of the delay, and solves this problem. The third problem is that the RF output conductance of a LDMOSFET can differ from the output conductance determined from DC measurements. Common past practise has been to put a series RC network in parallel with the output of the model to rectify this problem. The problem with this approach is that the effect of the network remains when the device is biased below pinch-off, which is not the case

in a real FET. A better solution is to use an extra node in the output circuit so that the drain current depends nonlinearly on three control voltages. This approach was not examined in this study.

The conservation of charge when implementing VCQS elements is an important topic of discussion [45, 46, 47, 48, 49, 1]. Charge non-conservation occurs when a charge source is dependent on more than one voltage and when more than one value of charge can exist for each combination of bias. Charge conservation therefore requires that a charge source behaves periodically over a period of simulation, and if it is not satisfied, the model will show a non-physical gain in energy for each period of simulation and this could cause the simulation to crash or to produce incorrect results. Port charges must therefore be constructed via path independent integration so that only one value for charge exists for each combination of V_{gs} and V_{ds}.

4.3 The Fager Nonlinear Model

The circuit diagram in figure 4.1 is used for the implementation of the Fager model, with the same circuit topology that is used in [36]. The circuit contains five extrinsic elements, three voltage-dependent nonlinear capacitors and one nonlinear current source that is dependent on V_{gs} and V_{ds} simultaneously. The bias voltages V_{gs}, V_{gd} and V_{ds} used in this chapter refer to the intrinsic voltages V'_{gs}, V'_{gd} and V'_{ds} respectively as indicated in the figure.

The nonlinear current equation is divided into four regions of bias. The boundaries for the different regions are indicated on the I_{ds} and g_m curves in figure 4.2. The advantage of observing separate regions is that the modeling can be broken into smaller sections which together form the nonlinear current equation. The equations are constructed so that the DC drain current and the transconductance are matched simultaneously in each region. This allows accurate IMD prediction, as well as the accurate prediction of output power and efficiency.

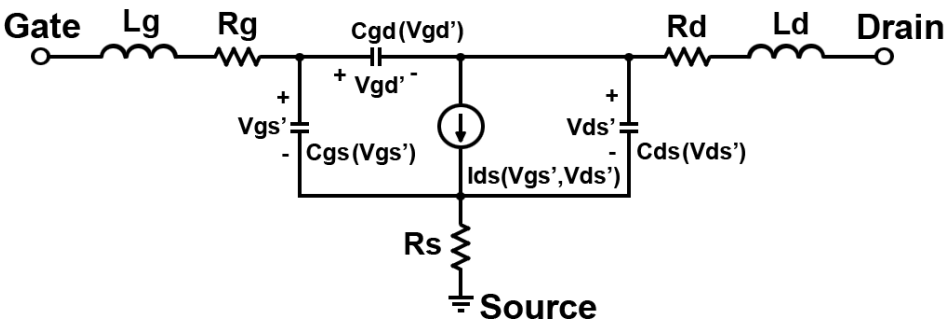


Figure 4.1: The circuit diagram used for the implementation of the Fager model.

A number of nonlinear equations are used to treat each of the four regions. The equations are combined to form the Fager I_{ds} equation. In region A of figure 4.2 the drain current depends

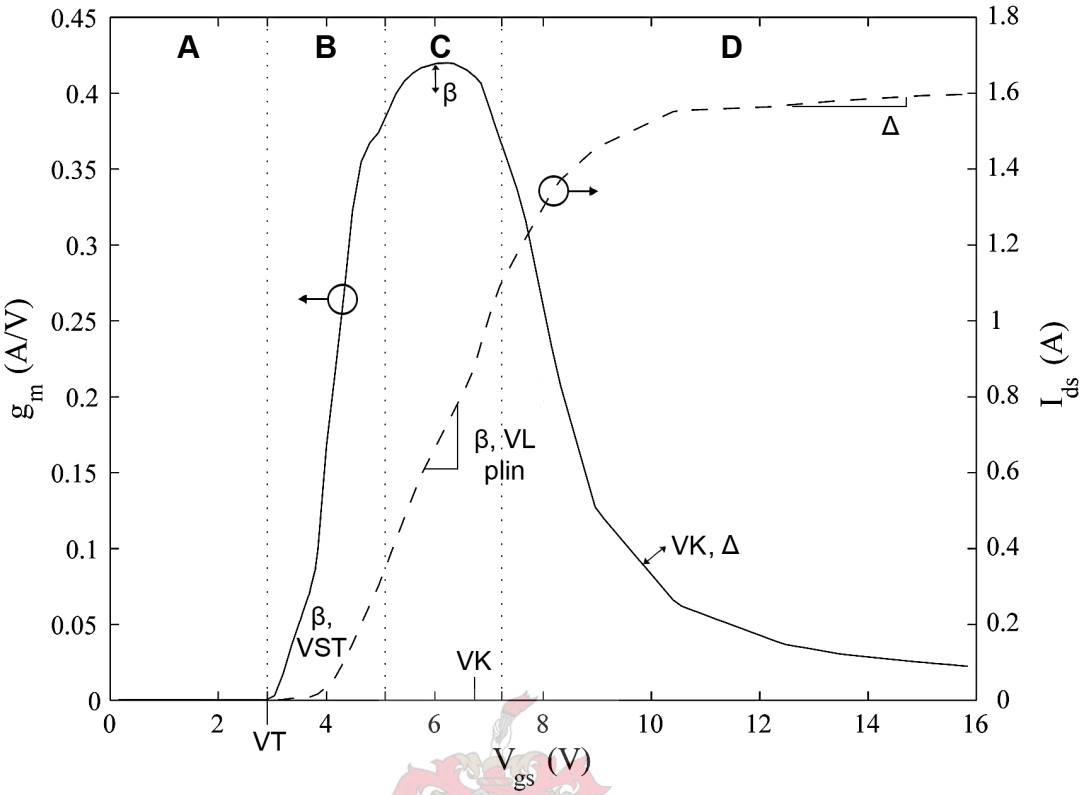


Figure 4.2: Different regions for the MRF282 LDMOS transistor shown on extracted g_m and I_{ds} over V_{gs} at $V_{ds} = 10V$. Region A indicates the sub-threshold, B the quadratic, C the linear and D the compression region. The model parameters are listed in the regions where they influence the nonlinear equation.

exponentially on V_{gs}. When the gate voltage is increased so that region B is entered, I_{ds} starts to rise quadratically and g_m tends to rise linearly. The current in regions A and B are modeled using a combination of equations (4.3.1)-(4.3.3)

$$V_{gs1} = V_{gs} - V_t \tag{4.3.1}$$

$$V_{gst} = VST \ln\left(1 + e^{V_{gs1}/VST}\right) \tag{4.3.2}$$

$$I_{dsq} = \beta V_{gst}^2 \tag{4.3.3}$$

where VST controls the turn-on abruptness, V_t the turn-on voltage and β the slope in the quadratic region. When the device is biased in region C the current increases linearly and the transconductance becomes constant. This region is known to provide good linearity, but at the cost of efficiency. The transition between region B and C is modelled by (4.3.4)

$$I_{ds} = \frac{\beta V_{gst}^2}{1 + \frac{V_{gst}^{plin}}{VL}} \tag{4.3.4}$$

where VL in combination with β determines the slope of the quadratic region and the transition to the linear region. The parameter *plin* is used to tune the transconductance slope in the linear region. As the bias is further increased, the device becomes saturated and the transconductance drops significantly. This behaviour is modelled by (4.3.5).

$$V_{gs2} = V_{gs1} - \frac{1}{2}\left(V_{gs1} + \sqrt{\left(V_{gs1} - VK\right)^2 + \Delta^2} - \sqrt{VK^2 + \Delta^2}\right) \tag{4.3.5}$$

VK represents the constant gate voltage at which the device becomes saturated and Δ the slope of the saturation. The parameters λ and α control the dependence on the drain source voltage V_{ds} and their effect can be seen in figure 4.3. λ is also used to control the output resistivity R_{ds}, which is the inverse of the output conductivity $G_{ds} = 1/R_{ds}$. The impact of λ is also shown in figure 4.4.

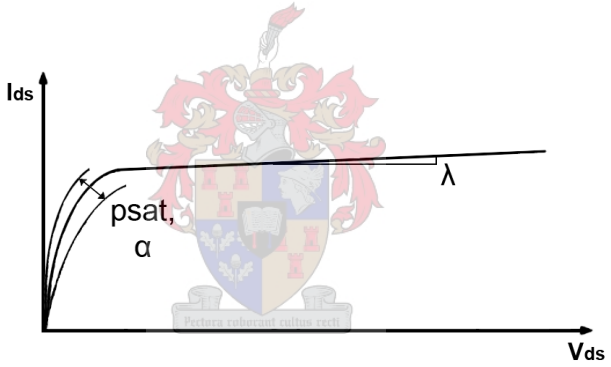


Figure 4.3: The indicated model parameters are used to control the nonlinear V_{ds}-I_{ds} relationship in the compression region.

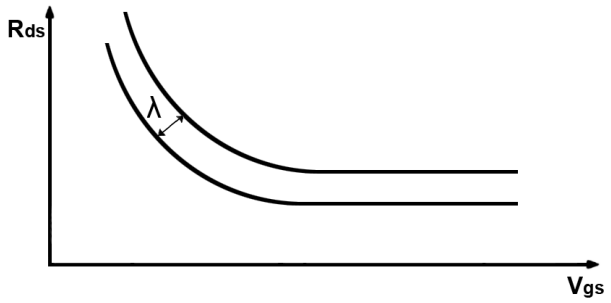


Figure 4.4: The parameter λ is also used to adjust the V_{gs}-R_{ds} relationship.

The nonlinear equations (4.3.1)-(4.3.5) are combined to create (4.3.6)-(4.3.9) that define the control function of the nonlinear current source as a function of V_{gs} and V_{ds}.

$$V_{gs1} = V_{gs} - V_t \tag{4.3.6}$$

$$V_{gs2} = V_{gs1} - \frac{1}{2}\left(V_{gs1} + \sqrt{\left(V_{gs1} - VK\right)^2 + \Delta^2} - \sqrt{VK^2 + \Delta^2}\right) \tag{4.3.7}$$

$$V_{gs3} = VST \ln\left(1 + e^{V_{gs2}/VST}\right) \tag{4.3.8}$$

$$I_{ds} = \frac{\beta V_{gs3}^2}{1 + \frac{V_{gs3}^{plin}}{VL}}\left(1 + \lambda V_{ds}\right)\tanh\left(\frac{\alpha V_{ds}}{V_{gs3}^{psat}}\right) \tag{4.3.9}$$

The intrinsic capacitors of a FET are known to vary as a function of the bias voltages. These elements allow nonlinear displacement currents in the physical device, and allow the modeling of memory effects that result from movement of charge inside the FET. For a large-signal model to correctly predict the small-signal behaviour of a device at multiple bias conditions, bias-dependent elements must be implemented to model the capacitors. Three voltage-dependent capacitors are defined in the Fager model by equations (4.3.10) and (4.3.11)

$$C_{gx}\left(V_{gx}\right) = CGX0 + \frac{ACGX}{2}\left(1 + \tanh\left[KCGX\left(V_{gx} - VCGX\right)\right]\right) \tag{4.3.10}$$

where C_{gx} can be used as either the gate-source or gate-drain capacitance function.

$$C_{ds}\left(V_{ds}\right) = \frac{CDS0}{\sqrt{\left|1 + \frac{V_{ds}}{VDS0}\right| + 10^{-15}}} \tag{4.3.11}$$

Each equation is dependent on only one control voltage and therefore has a limited capability to model the capacitance over bias. The original equation for C_{ds} in [36] is modified so that the absolute value inside the square root is taken and a small insignificant value is added. This is done to prevent the square root of a negative value to occur and to avoid division by zero by the simulator when V_{ds} reaches a certain value below zero.

4.4 Parameter Determination for the Fager Model

The determination of the large-signal parameters requires the fitting of the nonlinear equations on small-signal and measured DC data. The GUI in figure 4.5 was developed to aid the user in the equation fitting. A typical set of starting values is supplied and the user is required to

manipulate the values manually or optimise the parameter values using the built-in optimisers. Five graphs are displayed that are updated when pressing the refresh button. The two graphs in the top left corner display the I_{ds}-V_{ds} and I_{ds}-V_{gs} data, while the three remaining graphs display the nonlinear capacitor data. The graphs provide a convenient way to roughly monitor the quality of the equation fitting. In each case the circles indicate the measured data, while the dots indicate the calculated data from the nonlinear equations.

A weighting feature is added to the GUI that allows the user to select a variable amount of points for the assignment of weights. The user specifies the maximum weight values that can be assigned when calculating each of the two weighting functions. The first weighting function defines a diagonal line, as shown in the top left corner of figure 4.5, that serves as an user-specified load line. Weights are determined according to each point's linear distance to the line. The second weighting function calculates weights by evaluating the rate of change in the S-parameters. The weights are calculated by creating uniform 2-D grids that contain the centroids for all of the measured S-parameters. The gradient in both V_{gs} and V_{ds} directions are calculated for each of the S-parameters and the different results are summed and scaled according to the maximum and minimum values. The specified number of points with the largest weights are used by the optimisers. Two clusters of light-gray circles can be seen in the top left corner of figure 4.5 surrounding the load line and indicating the areas where the S-parameters change a lot. The light-gray circles indicate the points that are assigned weights larger than unity and show what a typical distribution of weights looks like.

The optimisation can be performed separately for each nonlinear equation by pressing each of the fit buttons in the GUI. The displayed values are used as starting values for the optimisation. The error functions for the optimisers calculate the sum of the differences between the optimised function values and wanted data points, multiplied by the weight at the point. An error function of zero is therefore found when the optimised function fits perfectly on the wanted data. Each optimiser terminates when the error function changes with a value equal to or less than the specified termination change value. The optimiser terminates after the specified maximum number of iterations if the termination change value is not reached. The calculated weights for each bias point is used during optimisation so that a better fit is obtained where higher weights are assigned.

Another useful feature of the GUI is that the user can select whether the DC or RF I_{ds} should be used. The RF current is calculated by performing numerical integration on the intrinsic Y-parameters [1] determined during small-signal extraction. The integral equation (4.4.1) is used

$$I_i(V_1, V_2) = I_i(V_{10}, V_{20}) + \int_{V_{10}}^{V_1} Re[Y_{i1}(V, V_{20})]dV + \int_{V_{20}}^{V_2} Re[Y_{i2}(V_1, V)]dV \tag{4.4.1}$$

where the starting points for integration, V_{10} and V_{20}, has been taken as zero. Port 1 represents the gate and port 2 the drain where the source is taken as ground. The RF and DC currents

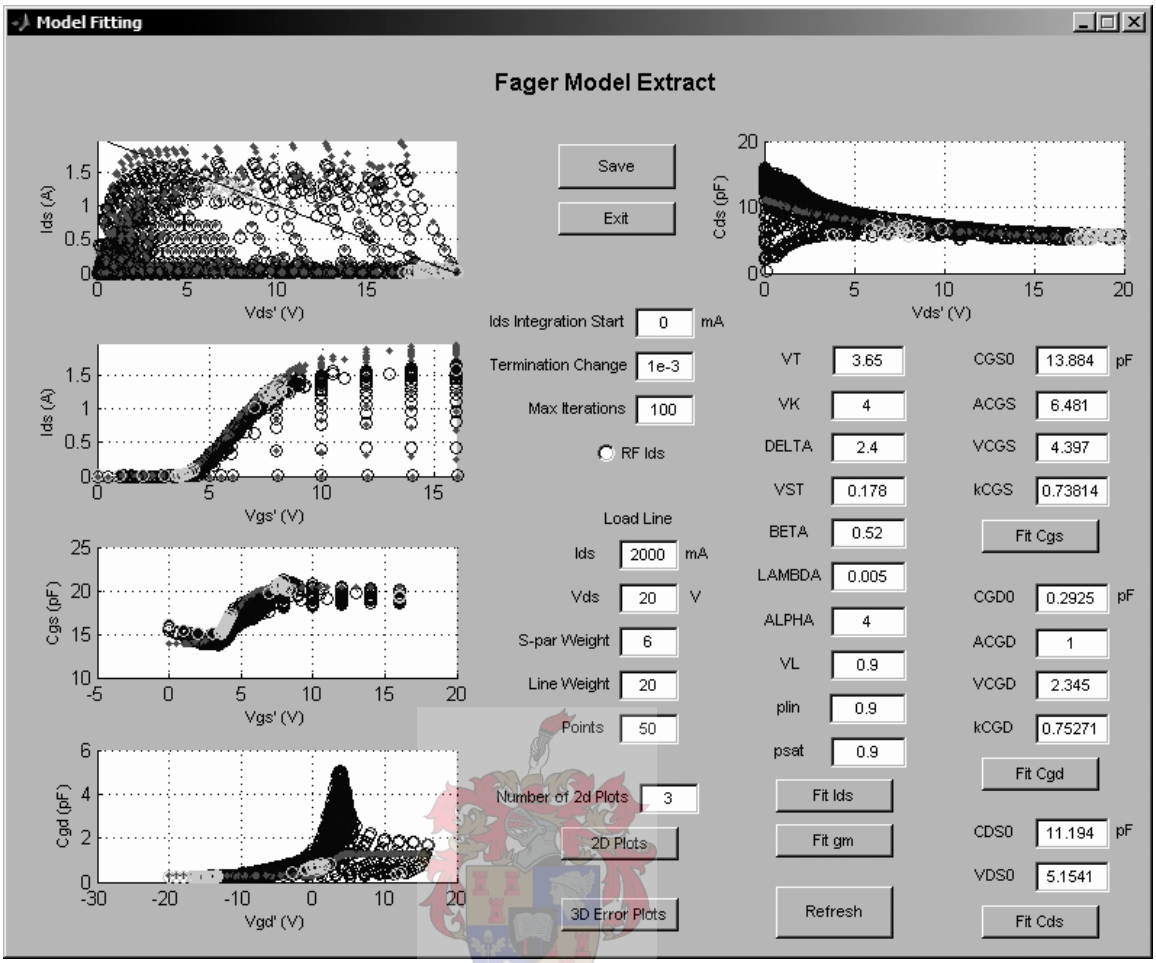


Figure 4.5: A GUI is used to determine the parameters for the Fager nonlinear equations. The parameter values for each equation can be optimised using a built-in Gauss Newton optimiser.

from the MRF282 data are each fitted to the model equations and it is found that the transconductance can be better predicted when using the DC current.

After a suitable set of parameters have been selected, the parameters can be stored in a text file by pressing the save button. The stored data can then be viewed at a later stage when entering the parameters into Microwave Office or other simulation program.

The procedure for fitting the nonlinear current equation can vary for different devices, but a number of guidelines can greatly simplify this task. It is critical that a good fit on I_{ds}, g_m and R_{ds} data is considered when choosing a suitable set of parameters. A number of parameter values for the nonlinear current equation exist so that at least one of the above mentioned data sets is well modeled, but that the other data sets are modeled with poor accuracy. By closely monitoring the fitting on all three data sets together, the user is able to monitor when parameters are assigned values outside their operating ranges.

After reasonable parameter values are obtained using the optimisers, λ is tuned so that a suitable R_{ds} is found. It is important that the value for λ stays small and positive for a suitable R_{ds}.

It is found that an extremely good fit cannot be obtained for both R_{ds} and I_{ds}. Figure 4.6 shows that R_{ds} is much larger when calculated from the derivative (4.4.2) of the DC current than what it should be in comparison to the small-signal model. A compromise should therefore be made between good R_{ds} and I_{ds} prediction. λ is determined by iteration until a satisfactory compromise is found. The final prediction of R_{ds} in comparison with the small-signal model data is shown in figure 4.7.

$$R_{ds} = 1 / \frac{dI_{ds}}{dV_{ds}} \tag{4.4.2}$$

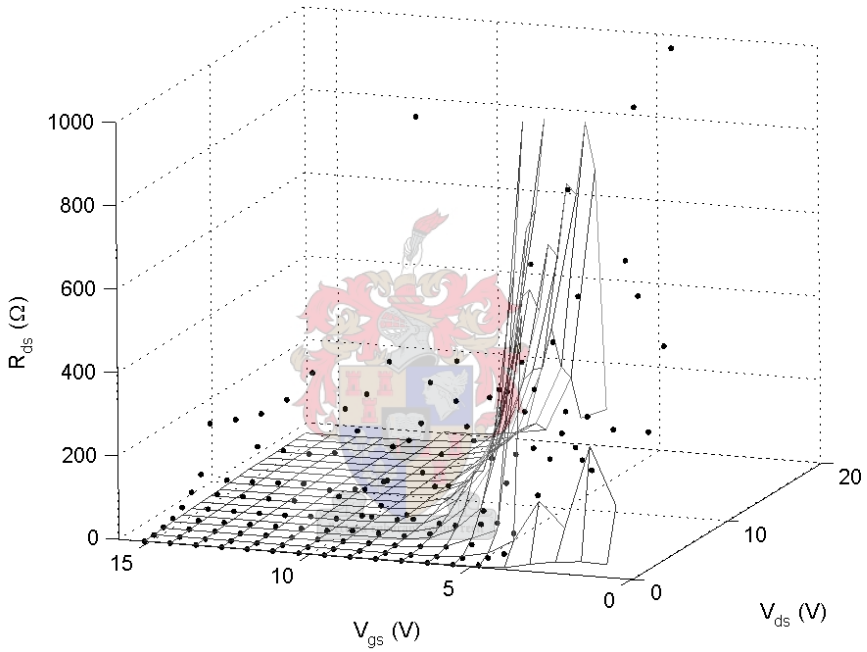


Figure 4.6: Compared R_{ds} for the small-signal model (mesh) and as computed using the measured DC I_{ds} (dots). The small-signal R_{ds} is seen to be much lower than the DC R_{ds}. The dots for $R_{ds} > 1000\Omega$ are not shown in the figure.

A small discrepancy also exists between g_m from the derivative (4.4.3) of the DC current and that of the small-signal model. This can be seen in figure 4.8 and it is suspected that g_m is slightly dispersive with frequency.

$$g_m = \frac{dI_{ds}}{dV_{gs}} \tag{4.4.3}$$

The transconductance is fitted as accurately as possible by tuning β, VL and $plin$ in the linear region and VK and Δ in the compression region. Once again a trade-off is made between the accuracy of I_{ds} and g_m. The final prediction for the transconductance is plotted in figure 4.9.

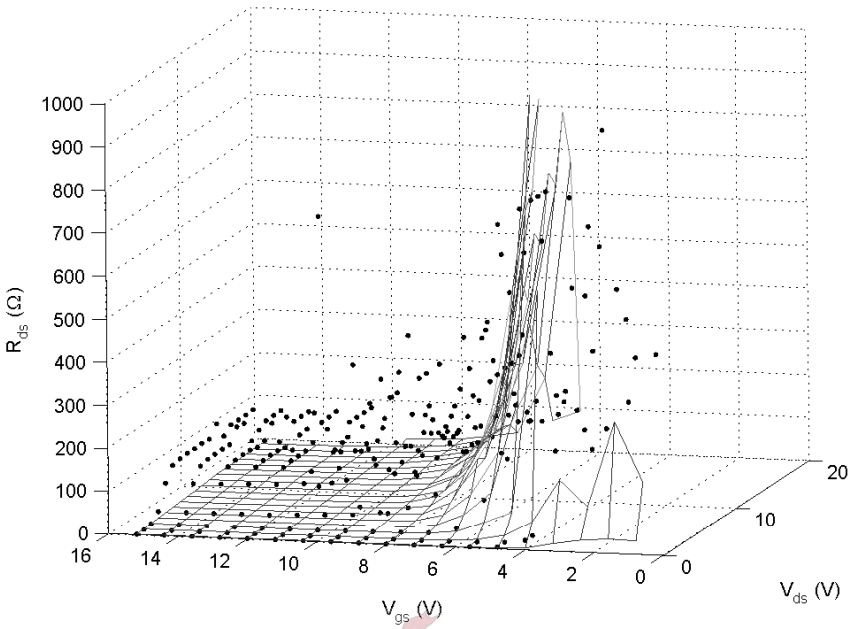


Figure 4.7: Compared R_{ds} for the small-signal model (mesh) and as computed using the Fager I_{ds} equation (dots). The small-signal R_{ds} is seen to be a little bit lower than for the Fager equation.

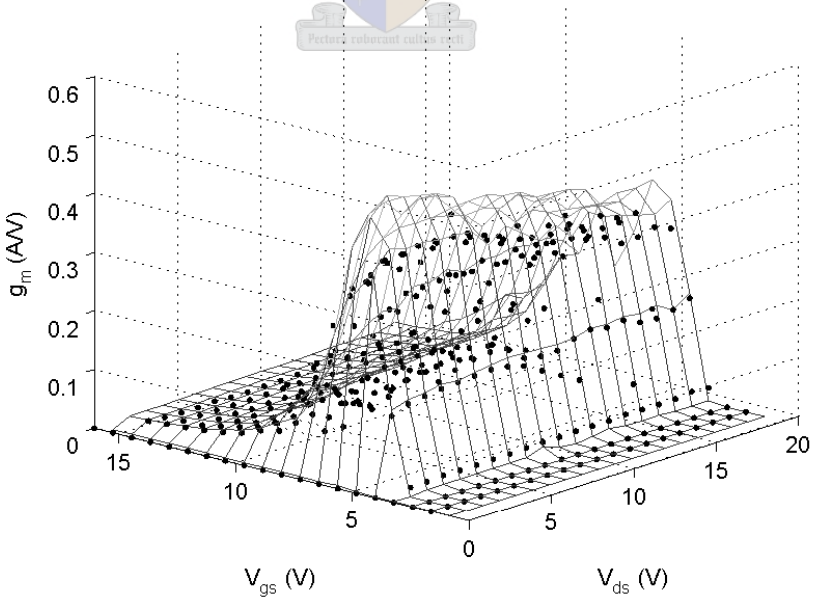


Figure 4.8: Compared g_m for the small-signal model (mesh) and as computed using the measured DC I_{ds} (dots). The transconductance obtained from the DC data is slightly lower and also shows a less negative slope over V_{ds} for large values of g_m.

The most care has been taken to ensure a good fit for g_m in the switch-on region and in the shaded area, where a typical load-line is usually found. The accompanying I_{ds} is plotted in figure 4.10. All the extracted parameter values for the Fager nonlinear current equation are listed in table 4.1.

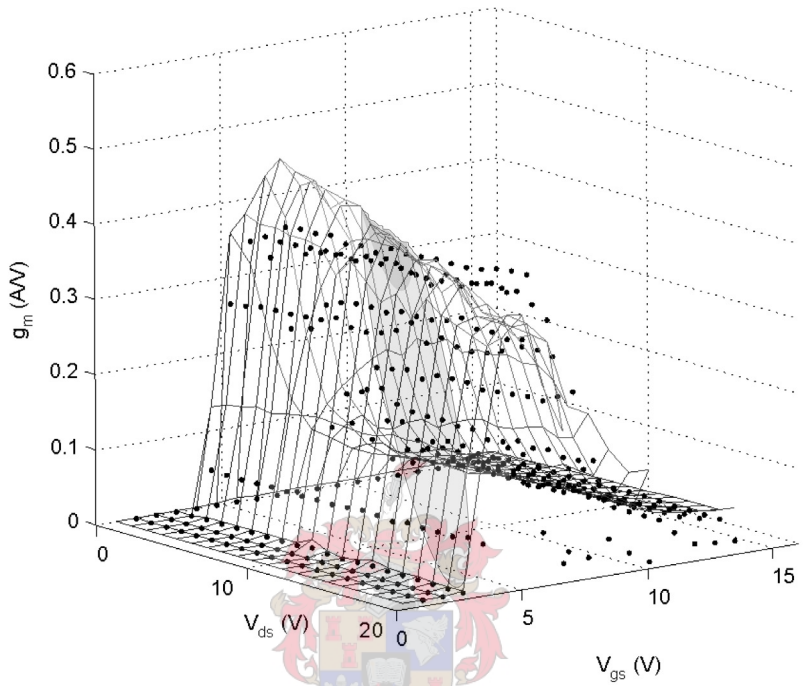


Figure 4.9: Compared g_m for the small-signal model (mesh) and as computed using the Fager I_{ds} equation (dots). The shaded region indicates the typical area of operation (load-line) for a linear amplifier. The g_m prediction is seen to be slightly inaccurate in the linear region because the effect of self-heating is not compensated for.

The parameter values for the nonlinear capacitor equations are determined by using the built-in Gauss-Newton optimisers. The equations are fitted with higher weights assigned to points near the load-line. The fitted capacitances are plotted in figures 4.11-4.13. Because the Fager capacitance equations are dependent on only one controlling voltage, the ability to correctly predict the capacitance for different bias conditions is limited. The extracted values for the capacitance equations are listed in table 4.2.

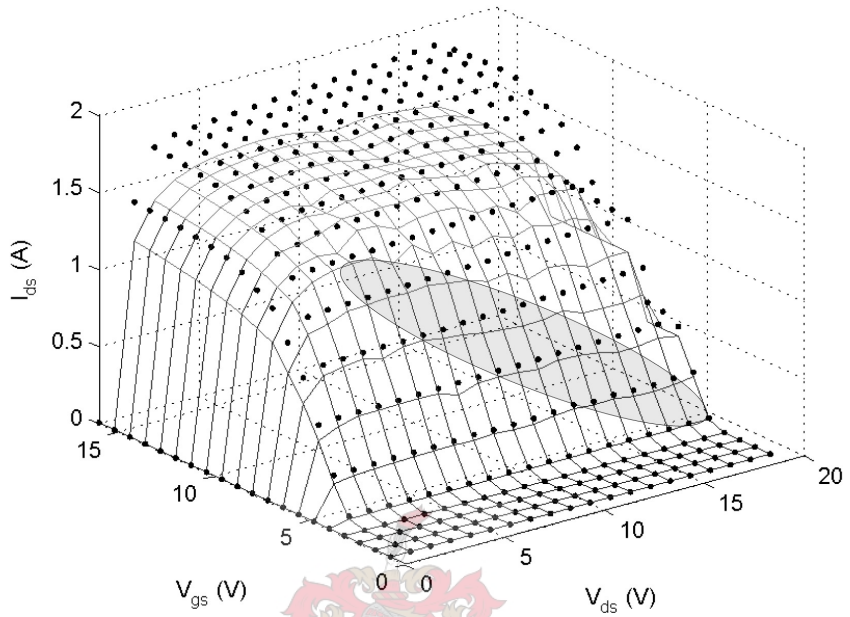


Figure 4.10: Compared I_{ds} for the DC measurements (mesh) and using the Fager equation (dots). The prediction is seen to be slightly inaccurate for higher currents because the effect of self-heating is not compensated for.

Table 4.1: Extracted large signal parameters for the Fager I_{ds} model between 0.4 GHz and 3 GHz.

Parameter	Value
VT	3.74
VK	4
Δ	2.4
VST	0.178
β	0.52
λ	0.005
α	4
VL	0.9
$plin$	0.9
$psat$	0.9

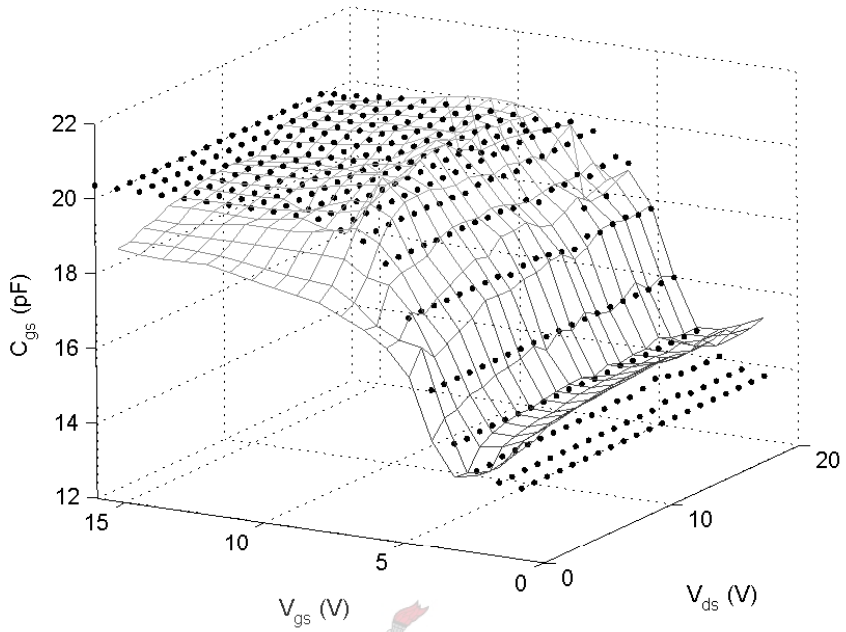


Figure 4.11: Compared C_{gs} for the small-signal model (mesh) and for the Fager capacitance equation (dots). The Fager capacitance equation is unable to produce a good prediction at all of the bias points.

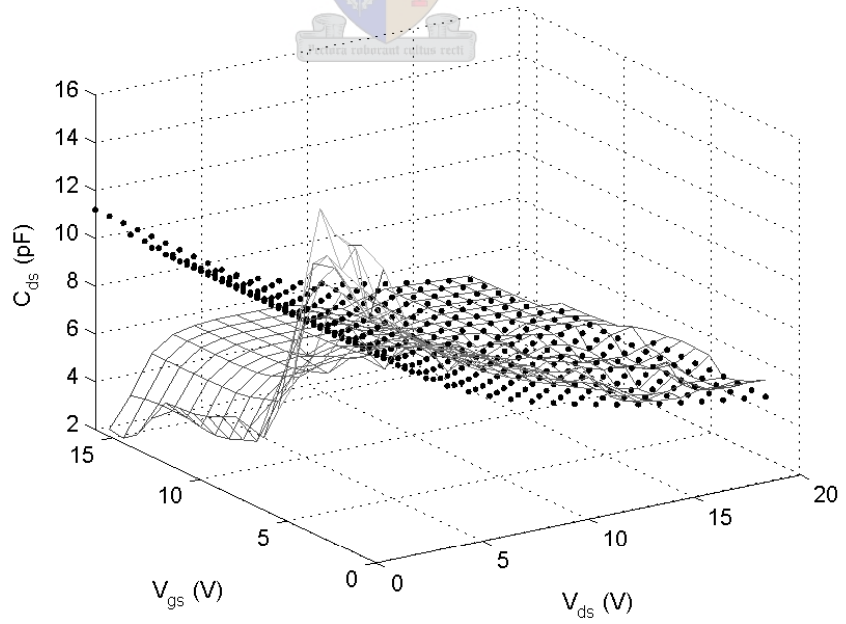


Figure 4.12: Compared C_{ds} for the small-signal model (mesh) and for the Fager capacitance equation (dots). The Fager capacitance equation is unable to produce a good prediction at all of the bias points.

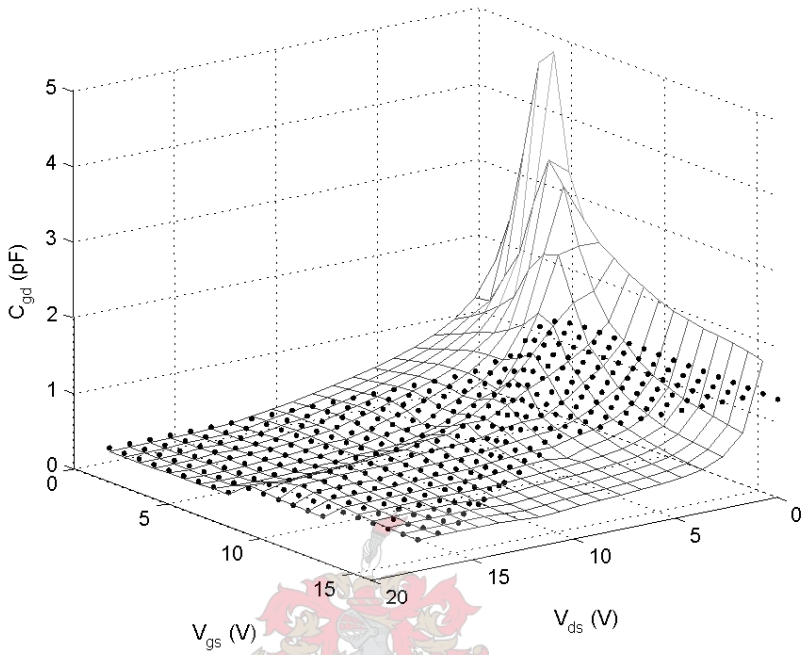


Figure 4.13: Compared C_{gd} for the small-signal model (mesh) and for the Fager capacitance equation (dots). The Fager capacitance equation is unable to produce a good prediction at all of the bias points.

Table 4.2: Extracted large signal parameters for the Fager capacitance models between 0.4 GHz and 3 GHz. The parameters are scaled so that the typical values are close to unity.

Parameter	Value	Scaling Factor
$CGS0$	13.88	10^{-12}
$ACGS$	6.481	10^{-12}
$VCGS$	4.397	1
$KCGS$	0.7381	1
$CGD0$	0.2925	10^{-12}
$ACGD$	1.000	10^{-12}
$VCGD$	2.345	1
$KCGD$	0.7527	1
$CDS0$	11.19	10^{-12}
$VDS0$	5.154	1

4.5 An Improved Fager Model

The three nonlinear capacitors of the Fager model are replaced by two nonlinear charge sources that are each dependent on two control voltages. The circuit diagram used for the Fager model in [36] is modified so that a more detailed equivalent circuit is used. Two series RC networks are added to the input and output of the intrinsic part of the model. This is done to rectify the RF drain-source conductance, determined from DC measurements, and so that the RF input and output conductance can be tuned to absorb some of the inaccuracies caused by imperfect parameter values. The two parasitic capacitors C_{pg} and C_{pd} are also included, together with the source inductance L_s, that were neglected for the implementation in [36]. The schematic diagram used for the improved model is shown in figure 4.14.

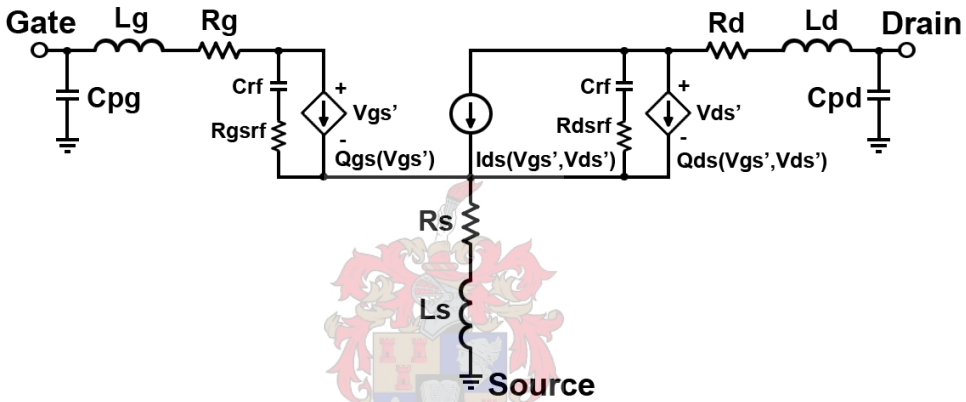


Figure 4.14: The circuit diagram used for the implementation of the improved Fager model.

The charge at each port, where port 1 once again represents the gate and port 2 the drain, is calculated using the extracted Y-parameters with equation (4.5.1), where V_{10} and V_{20} have been taken as zero. The requirement of the path independent integral is equivalent to the integrability conditions in [1] and allows the charge to be treated as a conservative vector field.

$$Q_i(V_1, V_2) = \int_{V_{10}}^{V1} \frac{Im[Y_{i1}(V, V_{20})]}{2\pi f} dV + \int_{V_{20}}^{V_2} \frac{Im[Y_{i2}(V_1, V)]}{2\pi f} dV \tag{4.5.1}$$

The current contribution from each charge source is determined by the time derivative of the charge. Because the voltage at each port is a function of time, the current is best modeled when ensuring that the voltage derivatives are well modelled. The numerical voltage derivatives of the charge are therefore calculated and used to construct the nonlinear charge equations. The derivatives of the charge at each port are plotted in figure 4.15. The calculated Y-parameters were used to determine the charge at each port, so that the derivatives are not affected by assumptions made when extracting the small-signal data.

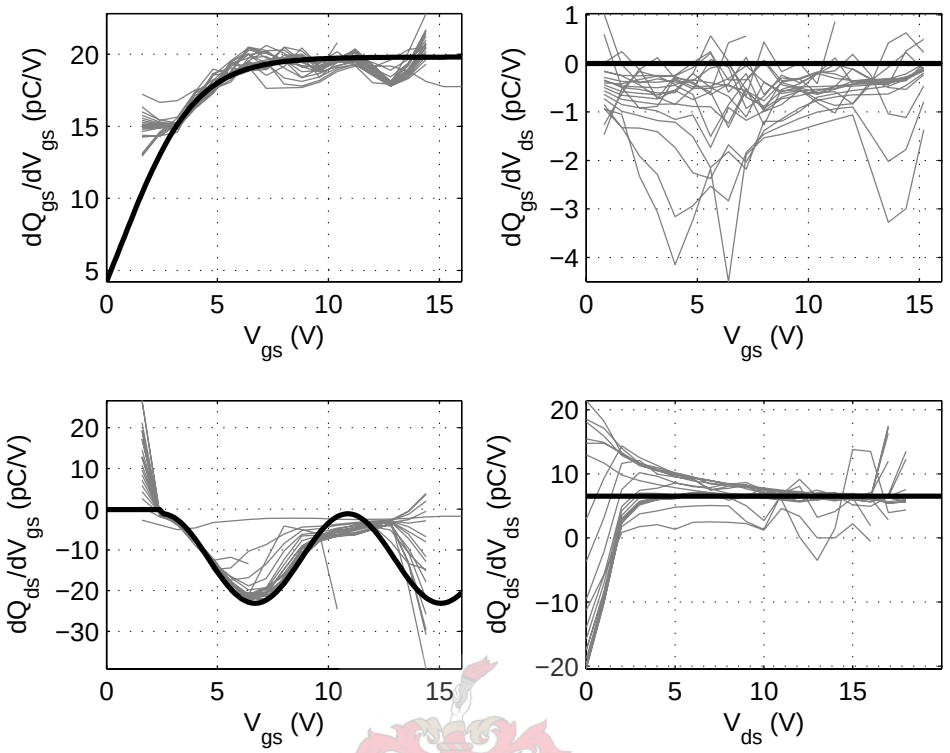


Figure 4.15: The derivatives of the calculated charge over bias are used to select functions that can be used to predict the behaviour of Q_{gs} and Q_{ds}. The gray lines indicate the charge calculated from the measured Y-parameters, while the black lines indicate the prediction using the chosen charge functions.

Simple mathematical functions like cos and tanh are used to construct equations (4.5.2)-(4.5.5) for each derivative. The equations are constructed by simply examining the trend of the slightly noisy data and implementing functions that best describe the behaviour. dQ_{gs}/dV_{ds} can be seen to consist mostly of noise and is relatively small, so it is defined in (4.5.2) to be approximately zero.

$$\frac{dQ_{gs}}{dV_{ds}} \approx 0 \tag{4.5.2}$$

dQ_{gs}/dV_{gs} can be seen to be fairly constant for higher values of V_{gs} and descending for lower values, and is defined in (4.5.3) to be the sum of a constant and a tanh function.

$$\frac{dQ_{gs}}{dV_{gs}} \approx QGS1 + QGS2\tanh\left(QGS3 \cdot V_{gs} + QGS4\right) \tag{4.5.3}$$

The noisy dQ_{ds}/dV_{ds} is fairly constant over bias and is defined in (4.5.4) as a constant.

$$\frac{dQ_{ds}}{dV_{ds}} \approx MVDS \tag{4.5.4}$$

dQ_{ds}/dV_{gs} displays sinusoidal behaviour, which is modeled using a cos function. The parameter DVGS is used to specify the origin of the cos function. V_{gs} is limited inside the cos function so that the smallest value it can obtain is the value of DVGS. This allows the charge to smoothly transcend into the region where the charge remains fairly constant over bias. BVGS allows the fine-tuning of dQ_{ds}/dV_{gs} in the region below DVGS and is used to control the small-signal gain for class C operation.

$$\frac{dQ_{ds}}{dV_{gs}} \approx MVGS + AVGS\cos\left(CVGS\left(V_{gs} - DVGS\right)\right) + BVGS \tag{4.5.5}$$

The combined equations for the derivatives are integrated over voltage to find the two resulting charge equations:

$$Q_{gs}(V_{gs}) = QGS1 \cdot V_{gs} + \frac{QGS2}{QGS3}\ln\cosh\left(QGS3 \cdot V_{gs} + QGS4\right) \tag{4.5.6}$$

and

$$Q_{ds}(V_{gs}, V_{ds}) = MVDS \cdot V_{ds} + MVGS \cdot V_{gs}^{lim} + \frac{AVGS}{CVGS}\sin\left(CVGS\left(V_{gs}^{lim} + DVGS\right)\right) + BVGS \cdot V_{gs} \tag{4.5.7}$$

where V_{gs}^{lim} denotes the limited V_{gs} for values smaller than DVGS.

The integration constants are neglected because a constant charge has no effect on the time-derivatives of the charge, and therefore produces no current.

4.6 Parameter Determination for the Improved Model

The GUI in figure 4.16 is created so that the nonlinear equations of the improved model can be fitted. Some features are added to the GUI to further enhance its usability. Another weighting algorithm is implemented that allows the user to specify a Q-point and calculate weights regarding the linear distance between bias points and the Q-point. The effect of the algorithm can be seen in 4.16 where the light-gray circles are all collected close to the specified Q-point. This algorithm is used together with the load-line and S-parameter change algorithms to provide an extremely flexible weighting scheme. The display of the Fager I_{ds} data in the GUI remains unchanged, while capacitance data plots are replaced by the data for the two nonlinear charge sources. The plot in the right hand side of figure 4.16 is added so that the user can monitor g_m at the Q-point.

Three extra optimisers are added so that the nonlinear current equation can be fitted for separate regions. The optimisers allow greater flexibility and ease for the automatic determination of the current model's parameter values. Because these parameter values have already been determined in the previous section, the new optimisers are only used to verify the previously determined parameter values and no modifications are therefore done. The first optimiser optimises only the parameters that are defined inside the sub-threshold and quadratic regions, the second only the parameters inside the quadratic and linear regions, while the third only those in the linear and compression regions. The whole Fager equation can therefore be evaluated by each of the optimisers, although only the appropriate parameters are optimised in each case.

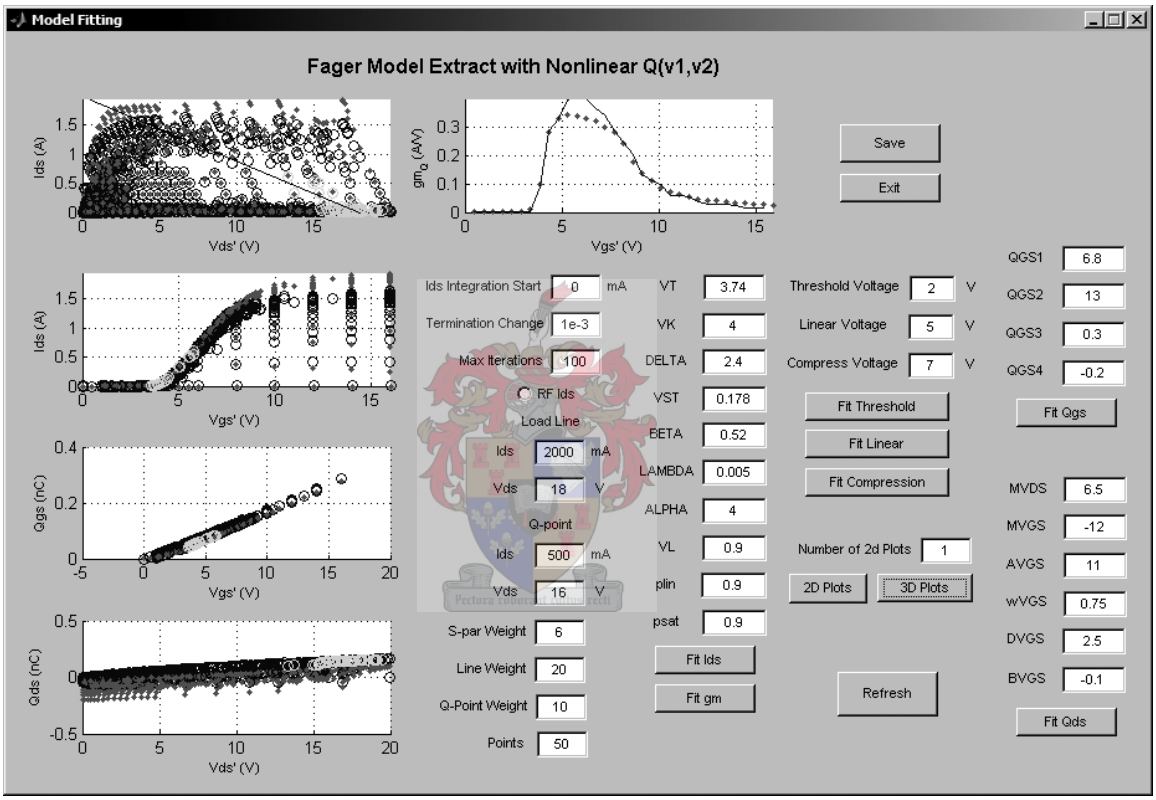


Figure 4.16: The Fager GUI is updated so that the parameters for the new model can be determined.

The optimisers for each nonlinear charge equation are designed to fit the derivatives of the charge equations onto the numerical derivatives of the calculated charge. The parameters are determined for each equation using the optimisers or tuning the values manually to obtain the optimal fit. The resulting parameters are listed in table 4.3. 3-D plots of the fitted derivative data are shown in figures 4.17-4.20. A reasonably good relationship between the measured and modeled charge derivatives can be seen in each case. Most care has been taken in each case to ensure a good fit in the region of a typical load-line. The resulting Q_{gs} and Q_{ds} over voltage bias are shown in figures 4.21 and 4.22. A constant offset in charge is allowed to exist due to its insignificance. It can be seen that it is difficult to evaluate the equation fitting by examining

the charge alone. The evaluation of the charge models should therefore be based on the fitting of the derivatives.

Table 4.3: Extracted large signal parameters for the charge equations between 0.4 GHz and 3 GHz.

Parameter	Value	Scaling Factor
$QGS1$	6.8	10^{-12}
$QGS2$	13	10^{-12}
$QGS3$	0.3	1
$QGS4$	-0.2	1
$MVDS$	6.5	10^{-12}
$MVGS$	-12	10^{-12}
$AVGS$	11	10^{-12}
$CVGS$	0.75	1
$DVGS$	2.5	1
$BVGS$	-0.1	10^{-12}

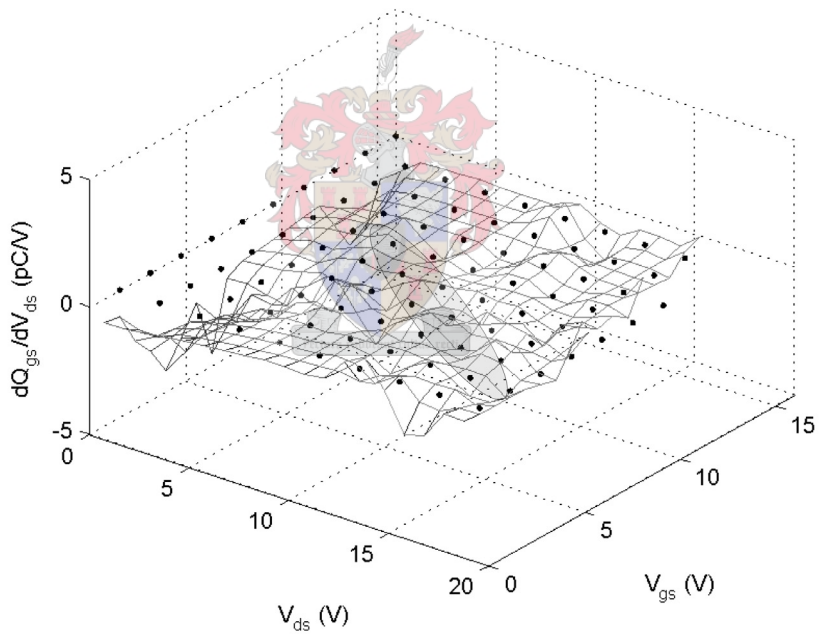


Figure 4.17: The numerical derivative of Q_{gs} over V_{ds} is used to fit the charge model equation.

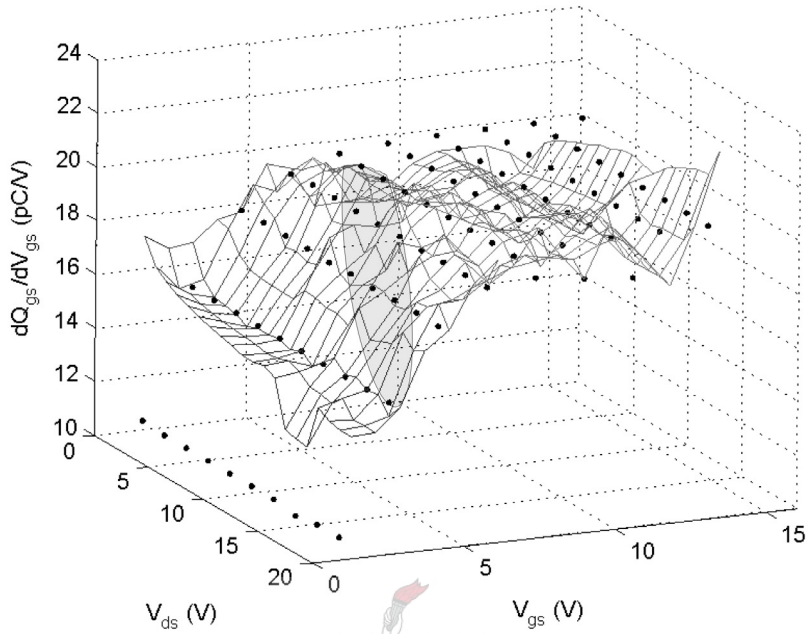


Figure 4.18: The numerical derivative of Q_{gs} over V_{gs} is used to fit the charge model equation.

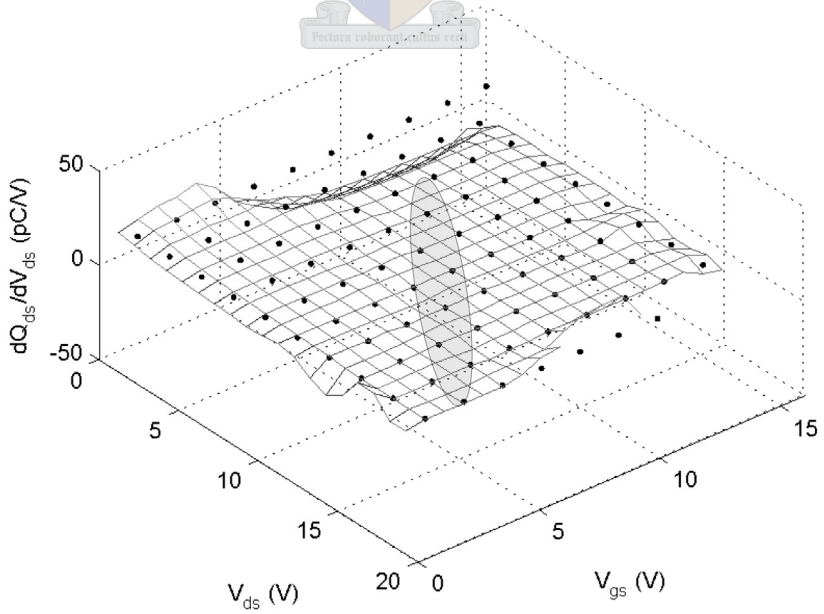


Figure 4.19: The numerical derivative of Q_{ds} over V_{ds} is used to fit the charge model equation.

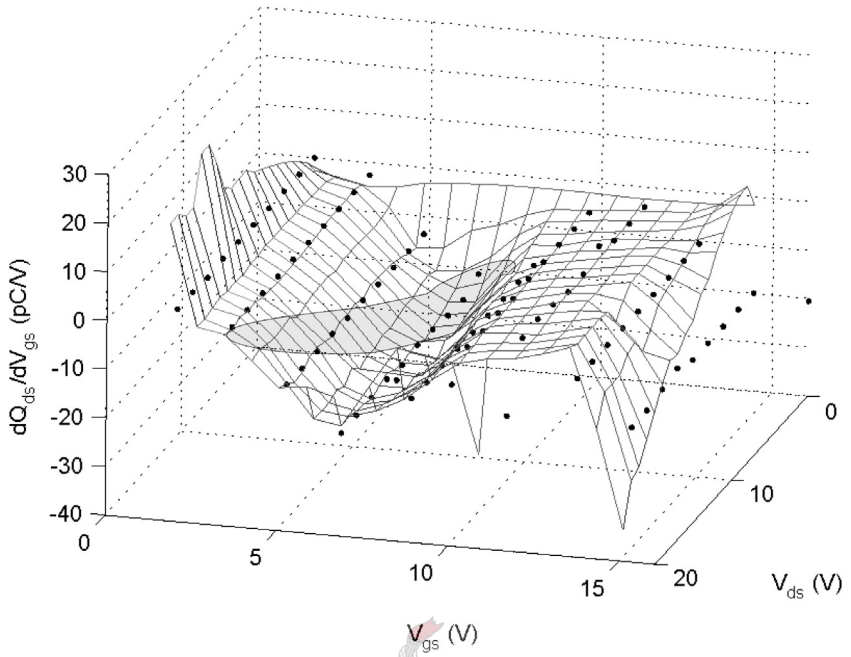


Figure 4.20: The numerical derivative of Q_{ds} over V_{gs} is used to fit the charge model equation.

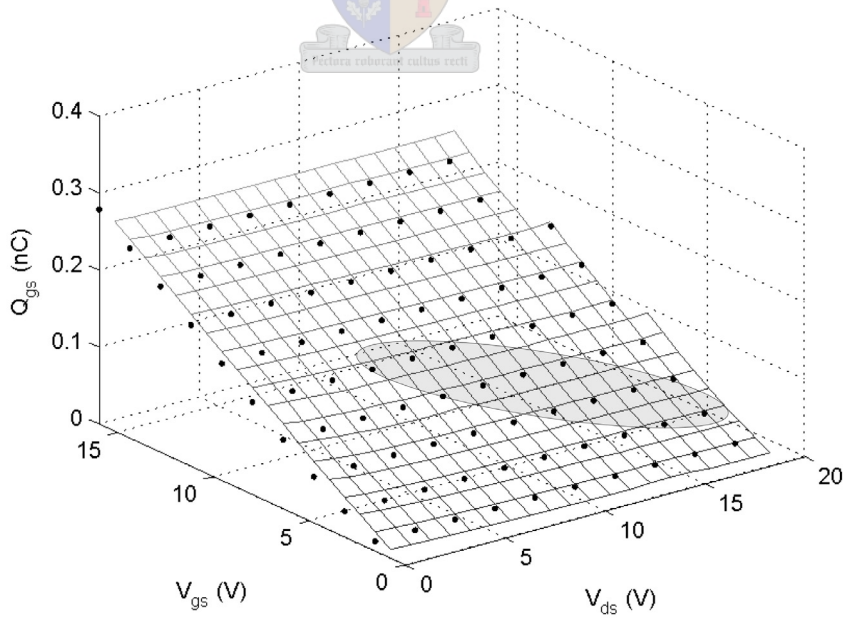


Figure 4.21: The measured Q_{gs} is compared to the calculated charge over bias. Only the slope of the charge is significant.

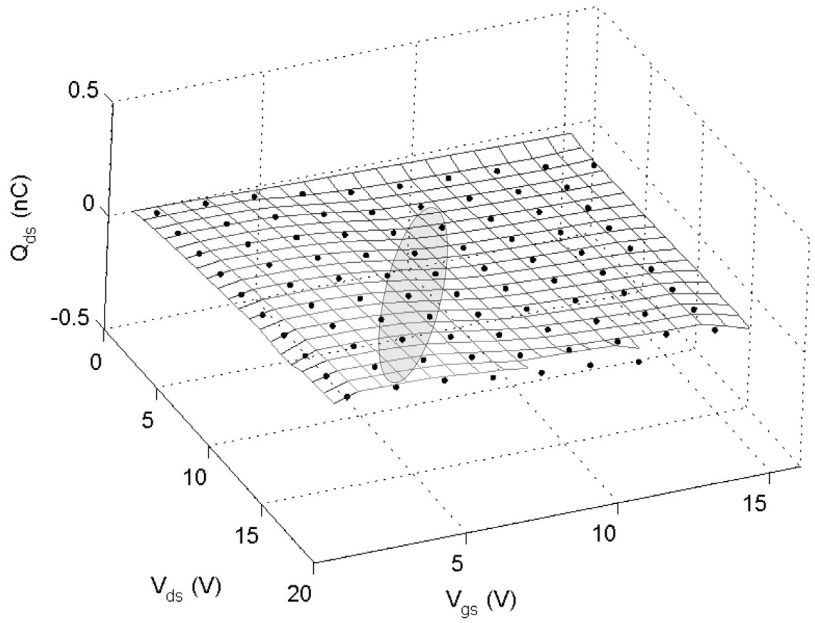


Figure 4.22: The fitting of Q_{ds} over bias with the calculated charge. Only the slope of the charge is significant.

4.7 Implementation of Models

The original Fager and improved Fager models are implemented in Microwave Office using the Nonlinear Model Wizard. A Curtice Cubic nonlinear model template is used as a base to implement the two model topologies. The Fager nonlinear current equation is implemented in both models using a nonlinear current source, while the extrinsic components are implemented as standard passive components. The nonlinear capacitors in the original Fager model and the nonlinear charge sources in the improved Fager model are implemented using nonlinear charge sources. This capacitor equations are converted to charge equations because a suitable nonlinear capacitor component could not be found in Microwave Office. The charge functions are calculated by performing the analytical integrals of each of the capacitance equations over the appropriate voltages. The resultant charge equations can be seen in (4.7.1) and (4.7.2), where the Q_{gx} equation is used for both gate-source and gate-drain charges. The integration constants are neglected because a constant value of charge delivers no current contribution.

$$Q_{gx}\left(V_{gx}\right) = CGX0 \cdot V_{gx} + \frac{ACGX}{2}\left(V_{gx} + \frac{1}{KCGX}\ln\cosh\left[KCGX\left(V_{gx} - VCGX\right)\right]\right) \quad (4.7.1)$$

$$Q_{ds}\left(V_{ds}\right) = 2CDS0 \cdot VDS0\sqrt{\left|1 + \frac{V_{ds}}{VDS0}\right| + 10^{-15}} \quad (4.7.2)$$

Each of the model elements are defined in the Nonlinear Model Wizard using a text script as can be seen in figure 4.23. The models are compiled into a DLL file using a C++ compiler. The DLL file allows the implementation of the models from the element library in Microwave Office.

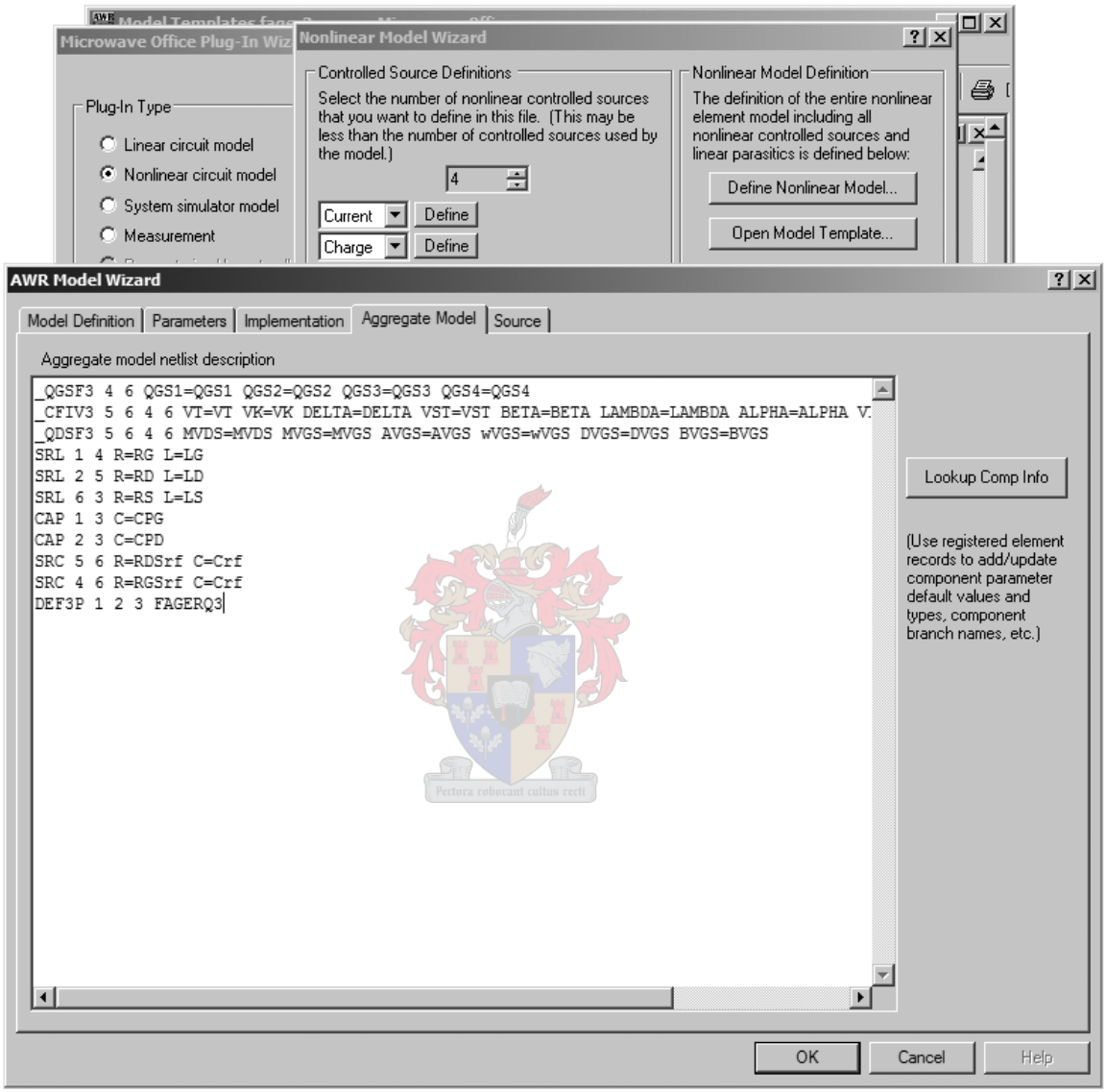


Figure 4.23: The Nonlinear Model Wizard is used in Microwave Office to generate the C++ code for the nonlinear models. The code is compiled into a DLL file so that the models can be implemented from the element library in Microwave Office.

The schematic diagram in figure 4.24 is used to generate simulated S-parameters that can be compared to the measured S-parameters. Some of the models' parameters are tuned so that better small-signal performance is obtained. *RGSRF* is tuned first so that better comparisons for S_{11} in the linear and quadratic regions are obtained. *RDSRF* is similarly tuned for S_{22} in the linear and quadratic regions. *CRF* is assigned a reasonably large value and consequently only

serves as a DC block. *VT*, *AVGS*, *CVGS*, *DVGS* and *BVGS* are tuned so that optimal comparisons for the simulated data in the sub-threshold, quadratic and linear regions are obtained. The small errors that were introduced during the parameter determination is absorbed by this adjustment. Care is taken so that a minimum deviation in the parameter values occur, while still improving the data fit. The new values for the tuned parameters are listed in table 4.4.

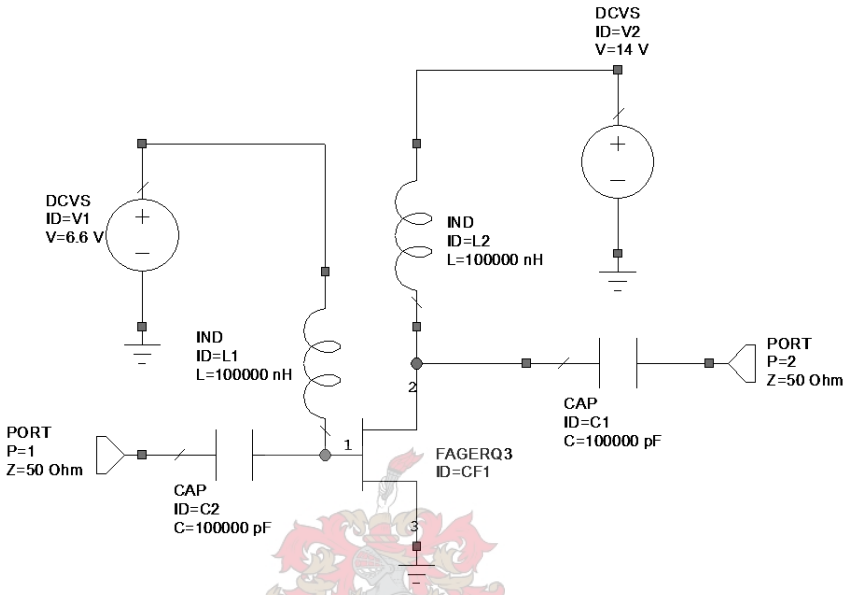


Figure 4.24: Schematic diagram used to compare measured S-parameters to simulated S-parameters in Microwave Office. Large capacitance and inductance values are used so that the effect is minimal on the simulated S-parameters.

Table 4.4: Tuned large signal parameters for the improved Fager model between 0.4 GHz and 3 GHz.

Parameter	Value	Scaling Factor
VT	3.65	1
AVGS	9.8	10^{-12}
CVGS	0.38	1
DVGS	3.33	1
BVGS	-0.46	10^{-12}
CRF	100	10^{-12}
RGSRF	150	1
RDSRF	200	1

4.8 Conclusions

The Fager nonlinear model was implemented and the parameters for the nonlinear equations were determined. A GUI provided an easy to use interface so that the model could be fitted on the measured data with optimal accuracy. It was found that the Fager nonlinear capacitor

equations lacked the capability to accurately model the capacitances inside the device over all the relevant bias points. This is mostly due to the fact that the capacitances are dependent on two controlling voltages in stead of one.

A new large-signal model was proposed that implements two nonlinear charge sources to model the three intrinsic capacitors. The charge over bias was calculated at each port using an integral equation that preserves charge conservation. The two charge sources were modeled with dependency on both the gate and drain voltages so that an improved modeling accuracy was obtained. The nonlinear charge equations were derived by examining each of the numerical voltage derivatives of the charge and implementing simple mathematical functions that represent the trend of the calculated data. The equations were fitted on the data and a good match was obtained for each of the derivatives.

In the next chapter the small-signal and nonlinear behaviour of the Fager and improved Fager large-signal models are compared against another large-signal model and measured data.

Chapter 5

Verification of Large-Signal Models

5.1 Introduction

Three large-signal nonlinear models are evaluated against measured data in this chapter. The original Fager, improved Fager and MET models are implemented in Microwave Office to verify the quality of the predictions for each of the models. The verifications include small-signal S-parameter prediction in each of the bias regions, single-tone harmonic output power and fundamental phase prediction as a function of input power for class-C and class-AB operation, and the two-tone third-order intermodulation (IM3) prediction for class-AB operation.

The MRF282Z MET model is implemented in Microwave Office using the XML library version 6.5. It is important to note that for the same part number each manufactured MRF282 differs slightly from another, due to manufacturing tolerances. The two models from the previous chapter were implemented using measured data from the same device it is evaluated against, while the MET model was created using data from a different device. It is therefore expected that the MET model will produce slightly larger prediction errors than the other two models.

The characterisation hardware was shipped to the Department of Electrical Engineering (ESAT), K.U. Leuven, Belgium, where nonlinear measurements were performed using a large signal network analyzer (LSNA) [50]. The nonlinear measurements consisted of single-tone and two-tone measurements over various bias conditions up to the eighth harmonic.

5.2 Small-signal Verification of Models

The small-signal S-parameters are compared to the measured data in each of the four regions of operation for the original Fager, improved Fager and MET models. The compared S-parameters are plotted in figures 5.1-5.16. The predictions of S_{11} and S_{22} are examined first and it can be

seen that each model predicts the reflection slightly different from the others, but that the predictions are reasonably good for all of the models. The improved Fager model delivers a more accurate prediction in the regions where the device is switched on. This is because series RC networks that are parallel with the charge and current sources of each port are used to lower the RF input and output resistance. The prediction error grows slightly larger, however, when the device is biased in the sub-threshold region. The reason for this is because the series RC networks affect the magnitude of the input and output reflection even when the device is switched off. This is one of the sacrifices when using RC networks to correct the RF input and output resistance of a device. The phase prediction for S_{11} and S_{22} deviates considerably from the measured data for the MET model in the quadratic and linear regions, which suggests that the capacitances are not modelled very accurately. The Fager and improved Fager model predict the phase of the reflections with reasonable accuracy, except for S_{22} in the saturation region where the inability to model the temperature effects is believed to result in poor modeling accuracy.

It is very important that the magnitude as well as the phase of S_{21} is accurately predicted when designing phase-dependent amplifiers such as the Doherty amplifier. The improved Fager model achieves extreme accuracy for S_{21} in the quadratic and linear regions, while the other models predict S_{21} with less accuracy. The prediction for S_{21} in the saturation region is not very accurate for any of the models. The MET model predicts the magnitude of S_{12} with the most accuracy, while the other models do not predict the observed resonant point correctly. Because S_{12} is so small, the modeling accuracy of it's magnitude and especially it's phase is regarded as less important.

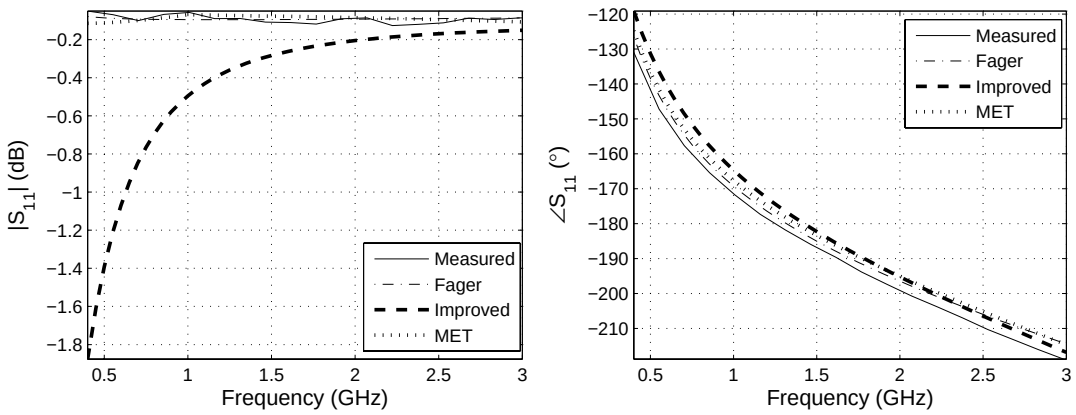


Figure 5.1: Compared S_{11} for the measured MRF282 LDMOSFET and three different large-signal models in the sub-threshold region ($V_{gs} = 2V$ and $V_{ds} = 20V$). The MET model delivers the most accurate predictions here.

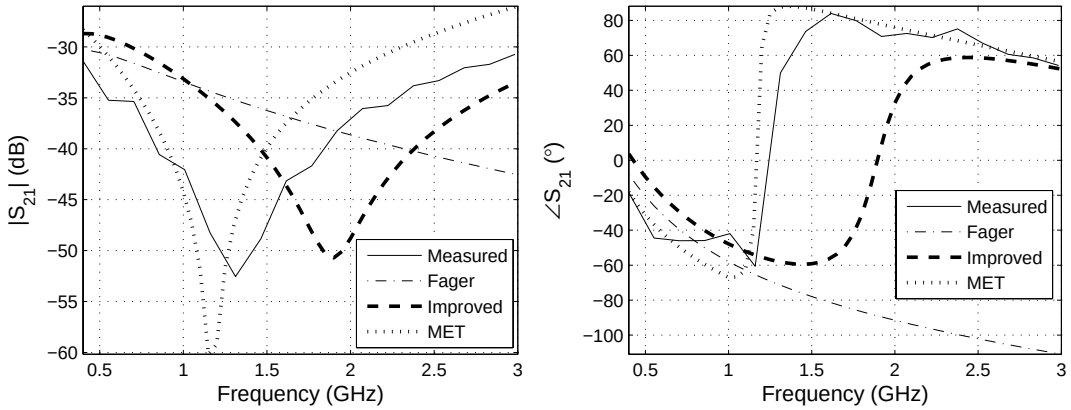


Figure 5.2: Compared S_{21} for the measured MRF282 LDMOSFET and three different large-signal models in the sub-threshold region ($V_{gs} = 2V$ and $V_{ds} = 20V$). The MET model delivers the most accurate predictions here.

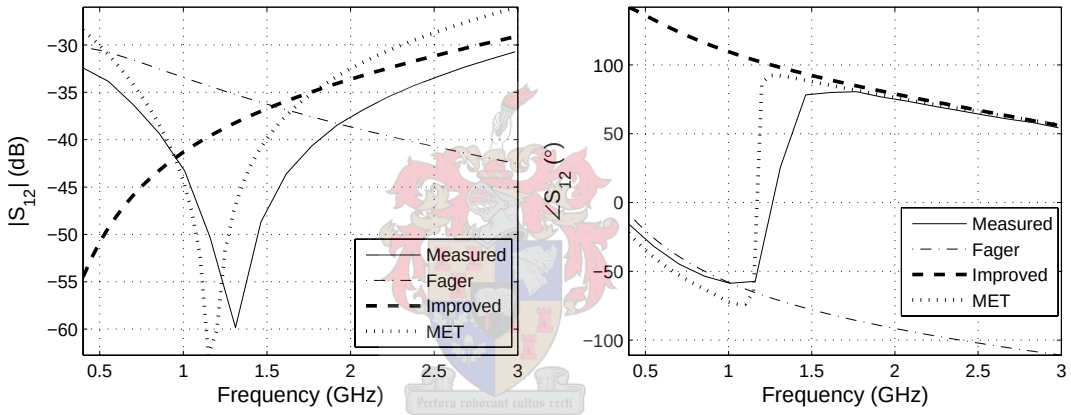


Figure 5.3: Compared S_{12} for the measured MRF282 LDMOSFET and three different large-signal models in the sub-threshold region ($V_{gs} = 2V$ and $V_{ds} = 20V$). The MET model delivers the most accurate predictions here.

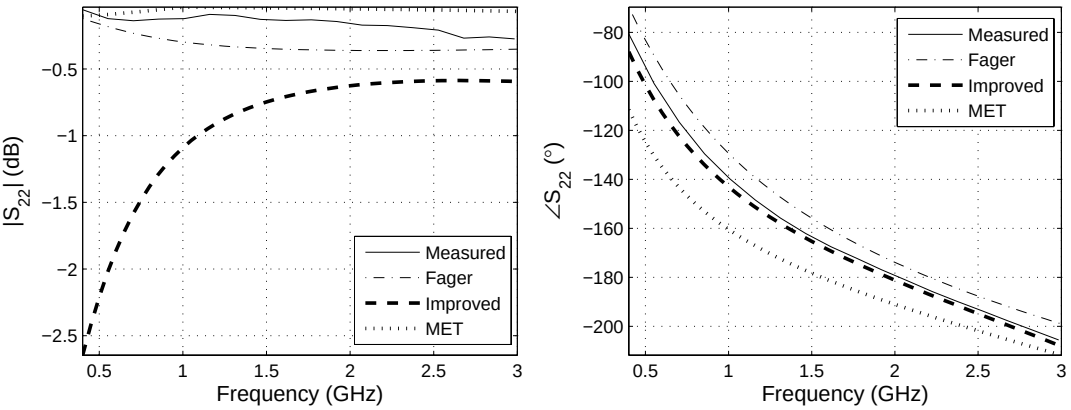


Figure 5.4: Compared S_{22} for the measured MRF282 LDMOSFET and three different large-signal models in the sub-threshold region ($V_{gs} = 2V$ and $V_{ds} = 20V$). The Fager model delivers the most accurate predictions overall here, while the improved Fager model delivers the most accurate phase prediction.

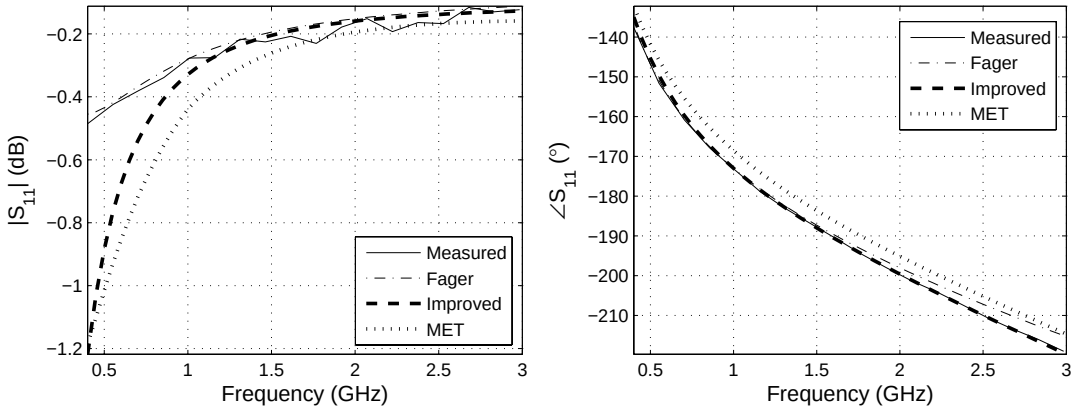


Figure 5.5: Compared S_{11} for the measured MRF282 LDMOSFET and three different large-signal models in the quadratic region ($V_{gs} = 3.9V$ and $V_{ds} = 18.1V$). The Fager and improved Fager models deliver the most accurate predictions here.

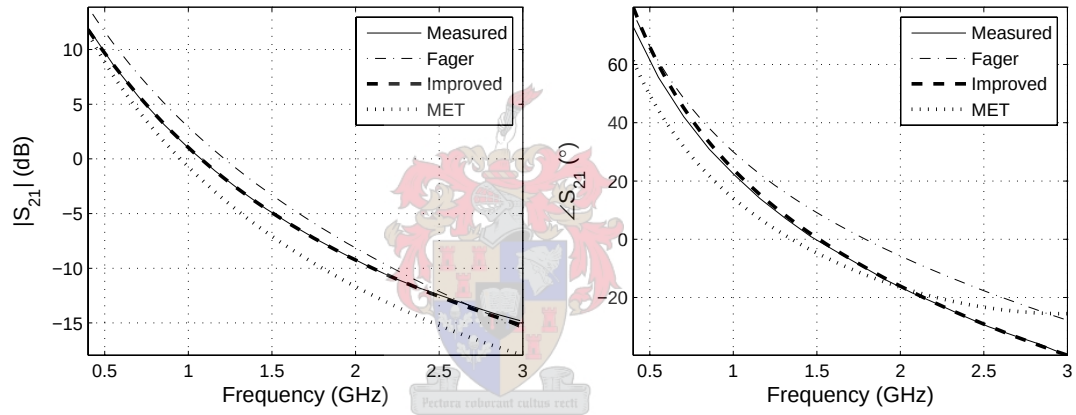


Figure 5.6: Compared S_{21} for the measured MRF282 LDMOSFET and three different large-signal models in the quadratic region ($V_{gs} = 3.9V$ and $V_{ds} = 18.1V$). The improved Fager model delivers the most accurate predictions here.

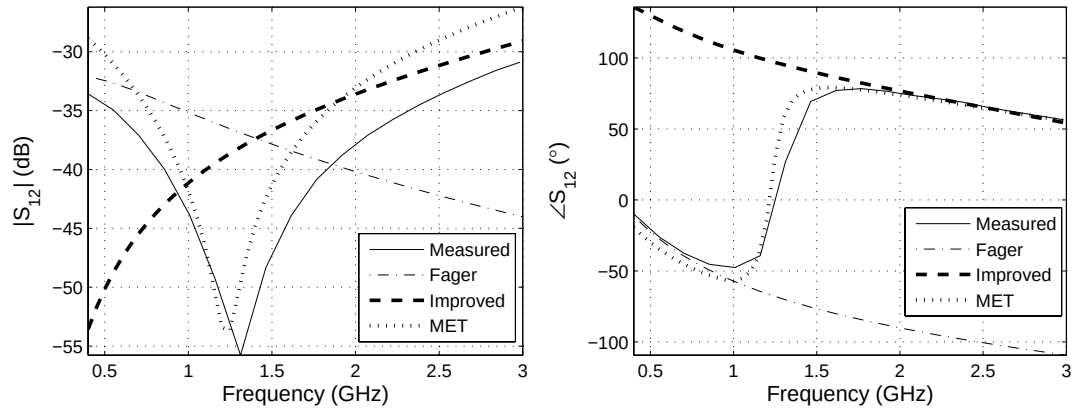


Figure 5.7: Compared S_{12} for the measured MRF282 LDMOSFET and three different large-signal models in the quadratic region ($V_{gs} = 3.9V$ and $V_{ds} = 18.1V$). The MET model delivers the most accurate predictions here.

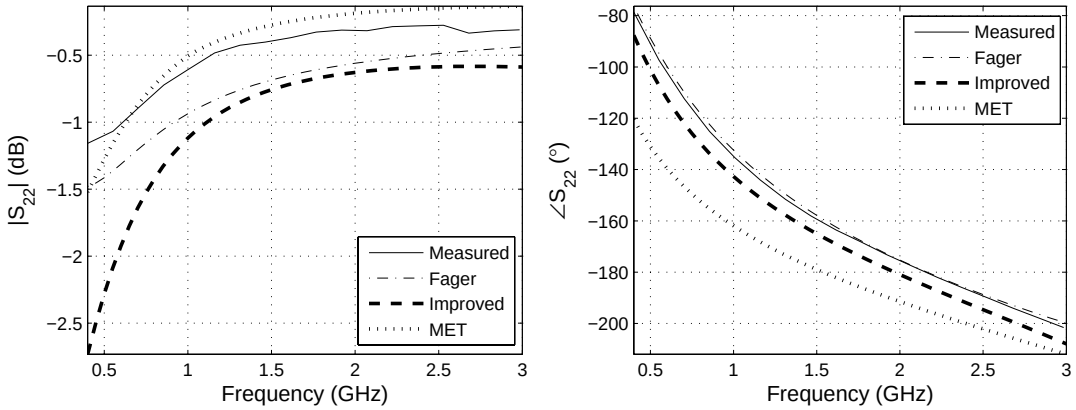


Figure 5.8: Compared S_{22} for the measured MRF282 LDMOSFET and three different large-signal models in the quadratic region ($V_{gs} = 3.9V$ and $V_{ds} = 18.1V$). The Fager model delivers the most accurate predictions here.

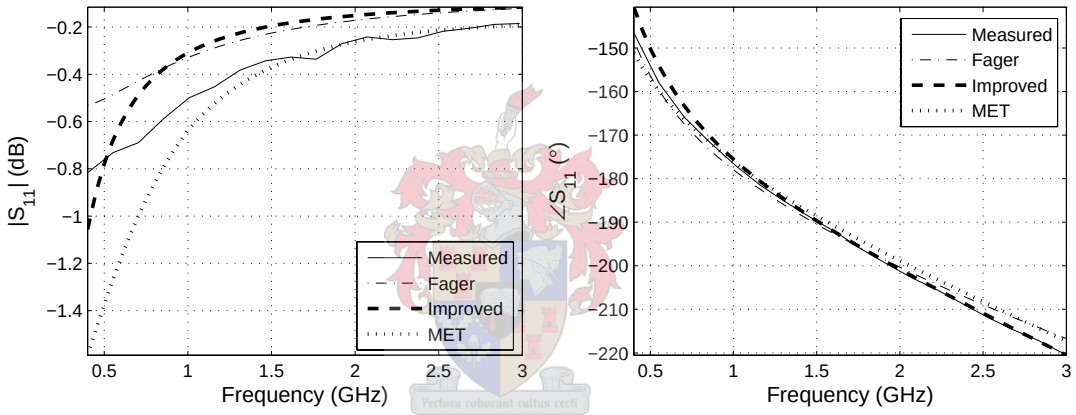


Figure 5.9: Compared S_{11} for the measured MRF282 LDMOSFET and three different large-signal models in the linear region ($V_{gs} = 6.6V$ and $V_{ds} = 14V$). All three models deliver reasonably accurate predictions here.

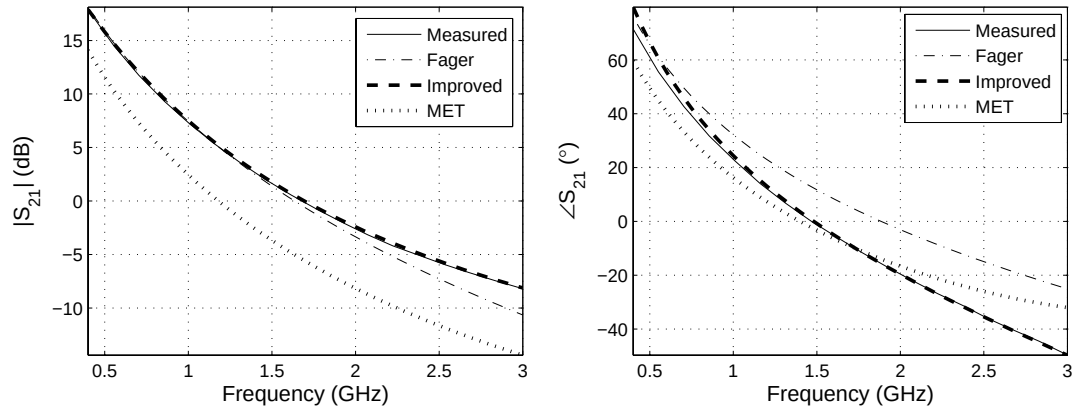


Figure 5.10: Compared S_{21} for the measured MRF282 LDMOSFET and three different large-signal models in the linear region ($V_{gs} = 6.6V$ and $V_{ds} = 14V$). The improved Fager model delivers the most accurate predictions here.

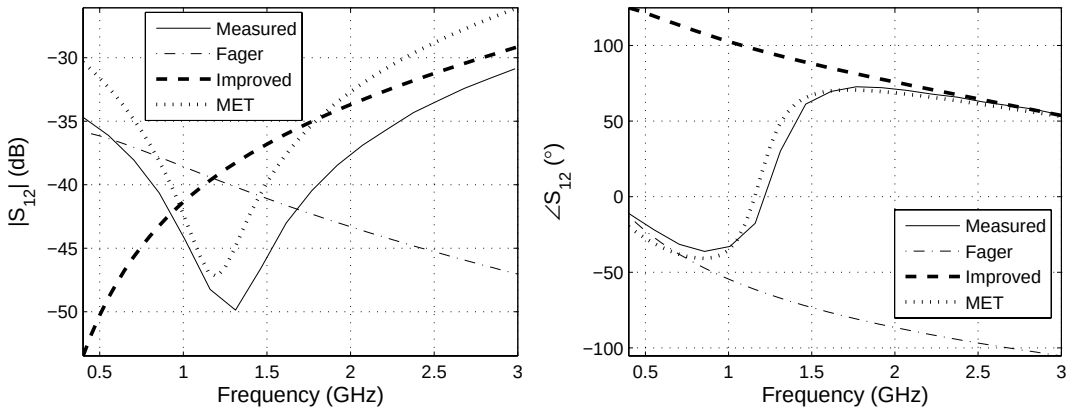


Figure 5.11: Compared S_{12} for the measured MRF282 LDMOSFET and three different large-signal models in the linear region ($V_{gs} = 6.6V$ and $V_{ds} = 14V$). The MET model delivers the most accurate predictions here.

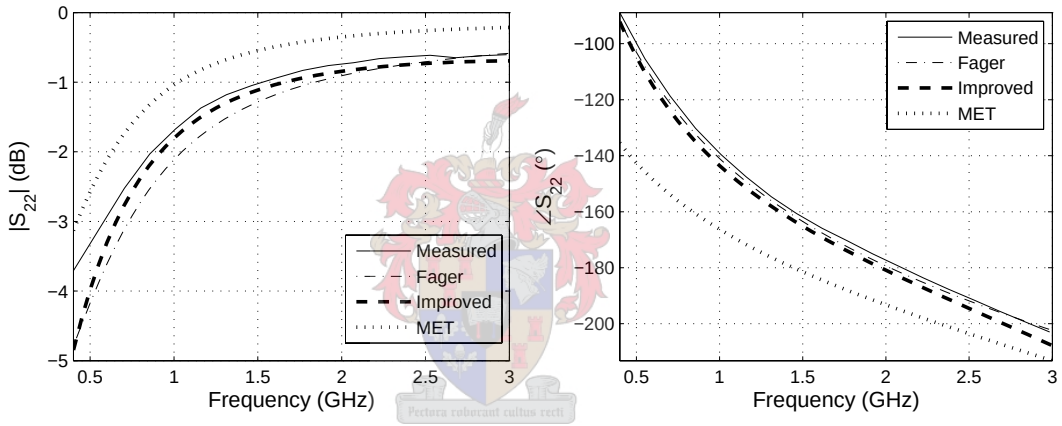


Figure 5.12: Compared S_{22} for the measured MRF282 LDMOSFET and three different large-signal models in the linear region ($V_{gs} = 6.6V$ and $V_{ds} = 14V$). The Fager and improved Fager models deliver the most accurate predictions here.

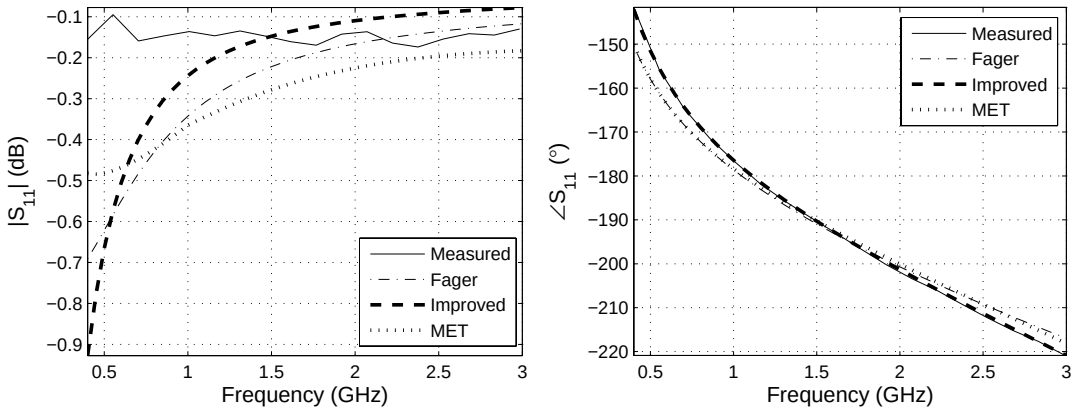


Figure 5.13: Compared S_{11} for the measured MRF282 LDMOSFET and three different large-signal models in the compression region ($V_{gs} = 9.2V$ and $V_{ds} = 5.28V$). All three models deliver reasonably accurate predictions here.

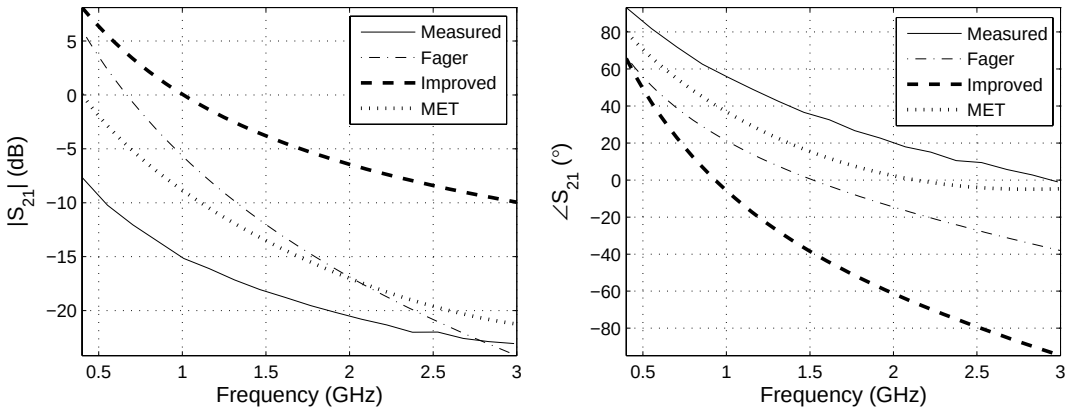


Figure 5.14: Compared S_{21} for the measured MRF282 LDMOSFET and three different large-signal models in the compression region ($V_{gs} = 9.2V$ and $V_{ds} = 5.28V$). None of the models perform well here.

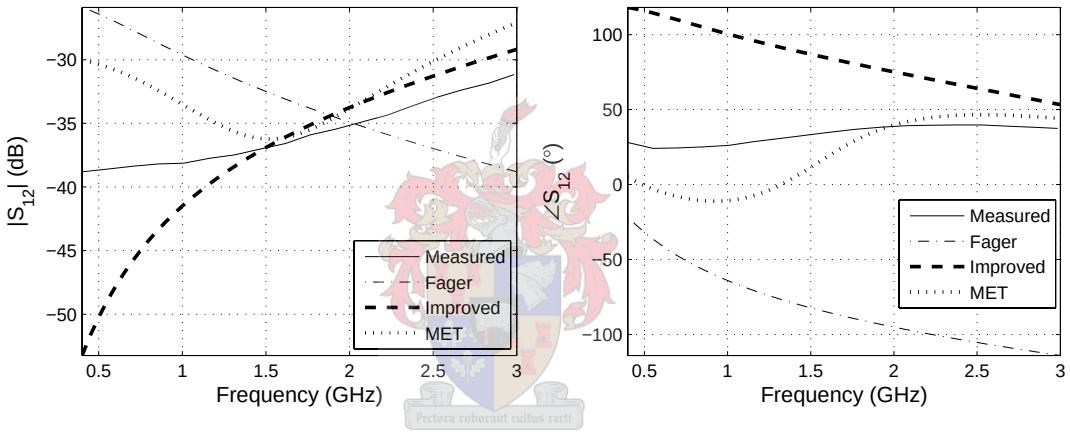


Figure 5.15: Compared S_{12} for the measured MRF282 LDMOSFET and three different large-signal models in the compression region ($V_{gs} = 9.2V$ and $V_{ds} = 5.28V$). The MET model delivers the most accurate predictions here.

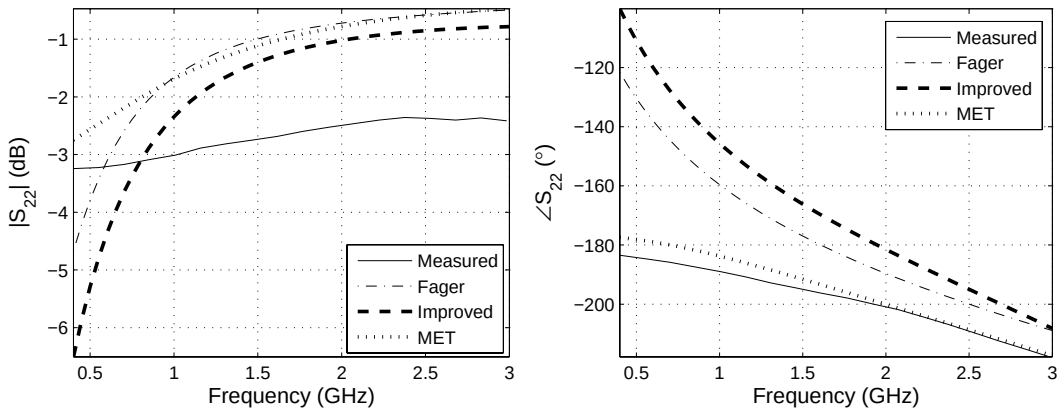


Figure 5.16: Compared S_{22} for the measured MRF282 LDMOSFET and three different large-signal models in the compression region ($V_{gs} = 9.2V$ and $V_{ds} = 5.28V$). None of the models perform well here, while the MET model delivers the most accurate phase prediction.

5.3 Single-Tone Large-Signal Verification of Models

The 1.6 GHz single-tone first, second and third output harmonics for the models are determined as a function of input power and are verified against measured data for class-C and class-AB operation. The measured data are obtained from LSNA measurements in Leuven and from high input-power SA measurements in Stellenbosch. The LSNA was calibrated up to the bias-Ts of the test setup described in chapter 2, excluding 3.5mm to 2.4mm converters connected to each bias-T. The high input-power single-tone measurements, performed in Stellenbosch, included an additional power amplifier, and a 1-2 GHz circulator at the input, and a 30 dB attenuator at the output to ensure low reflections at both ports. The schematic diagram in figure 5.17 is used for the simulations and includes a combination of measured sub-circuits and other elements to incorporate each component of the test setup up to the converters, used in Leuven. A power meter was used to perform signal level calibration, to account for the loss in the cables and bias-Ts, for the high input-power measurements.

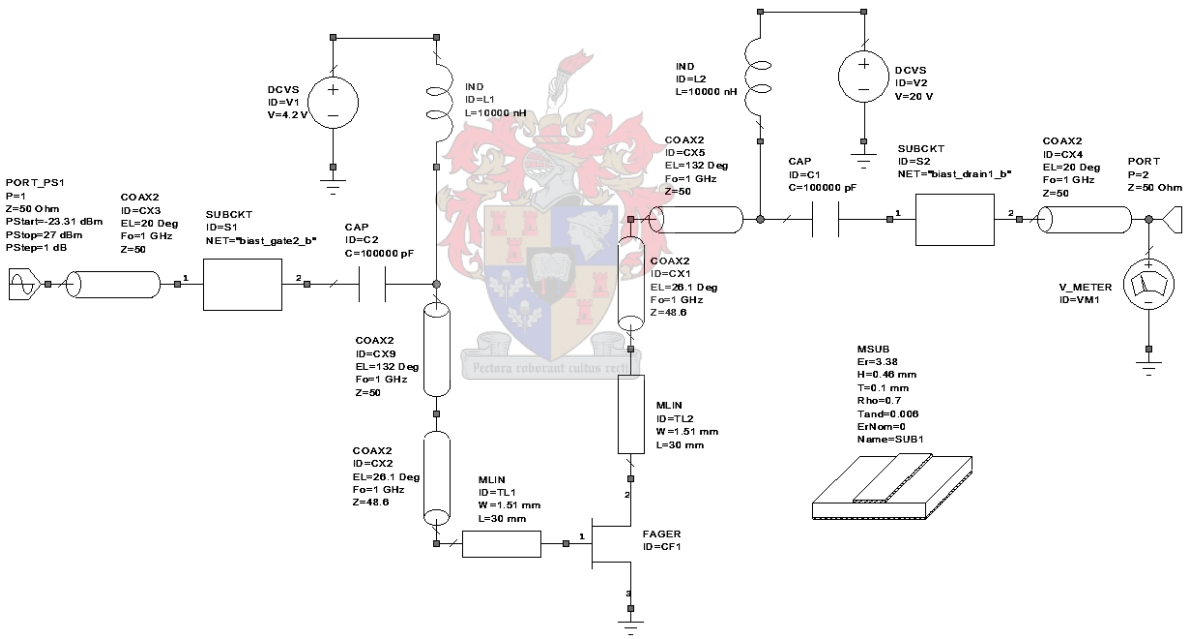


Figure 5.17: The schematic diagram is used in Microwave Office to simulate the test setup so that simulation results can be compared to the measured data.

The magnitudes of the first three harmonics are compared in figure 5.18 for class-AB operation. The improved Fager and MET models predict the first and second harmonics with reasonable accuracy, while the improved Fager model also predicts the third harmonic power with good accuracy. The Fager model only predicts the third harmonic power with reasonable accuracy, while the rest of the predictions vary with 2 dB or more from the measured data.

The measured and simulated output voltage phase is shown in figure 5.19. The improved Fager model predicts the phase for class-AB operation the most accurately with a 4° deviation. The

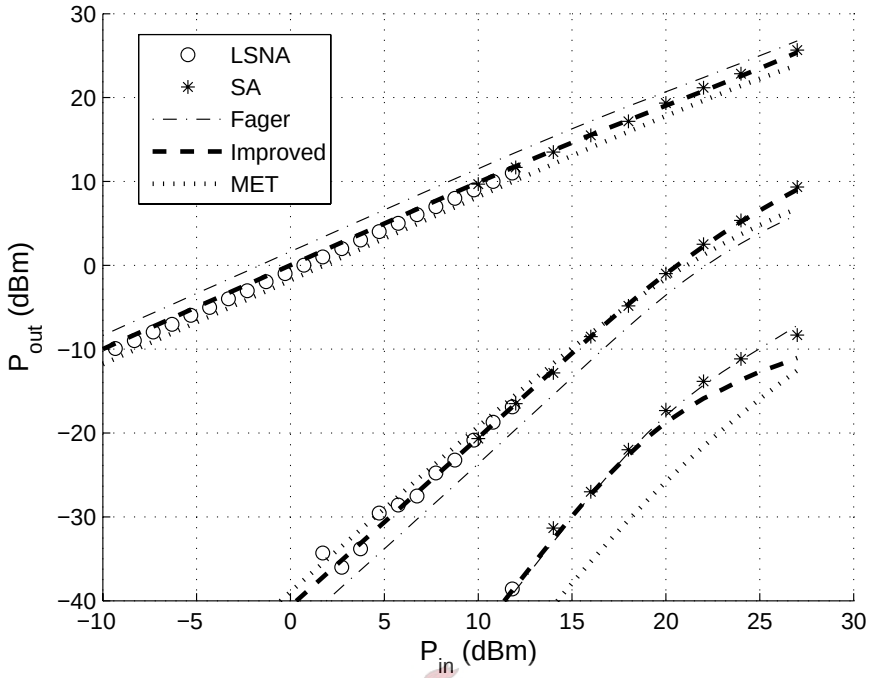


Figure 5.18: Compared 1st, 2nd and 3rd harmonic output power over input power at 1.6 GHz for the measured MRF282 LDMOSFET and three different large-signal models at $V_{gs} = 4.2V$ and $V_{ds} = 20V$. The fundamental frequency is at 1.6GHz.

Fager model predicts the phase with a reasonable 7° deviation and the MET model with a 13° deviation.

The MET model was unable to simulate for an input power sweep at bias voltages below pinch-off. The Microwave Office simulator reported that the step size for source stepping has decreased below a minimum allowed value and the problem persisted even after the simulator settings were adjusted. Similar errors occurred for the Fager and improved Fager models when the input power was increased to values above 30 dBm. The problems were not further investigated due to time constraints for the project.

The single-tone prediction for the Fager and improved Fager models are evaluated for class-C operation and the results are displayed in figure 5.20. The Fager model predicts the second and third order harmonics with the most accuracy, while the improved Fager model predicts the first harmonic at low input power more accurately than the Fager model. The basic trend for class-C operation is observed. The model is found to be very sensitive for parameter value changes in the sub-threshold region, and even though the output power is inaccurately predicted by as much as 10 dB, the careful further tuning of the model parameters should be able to improve the prediction in this region.

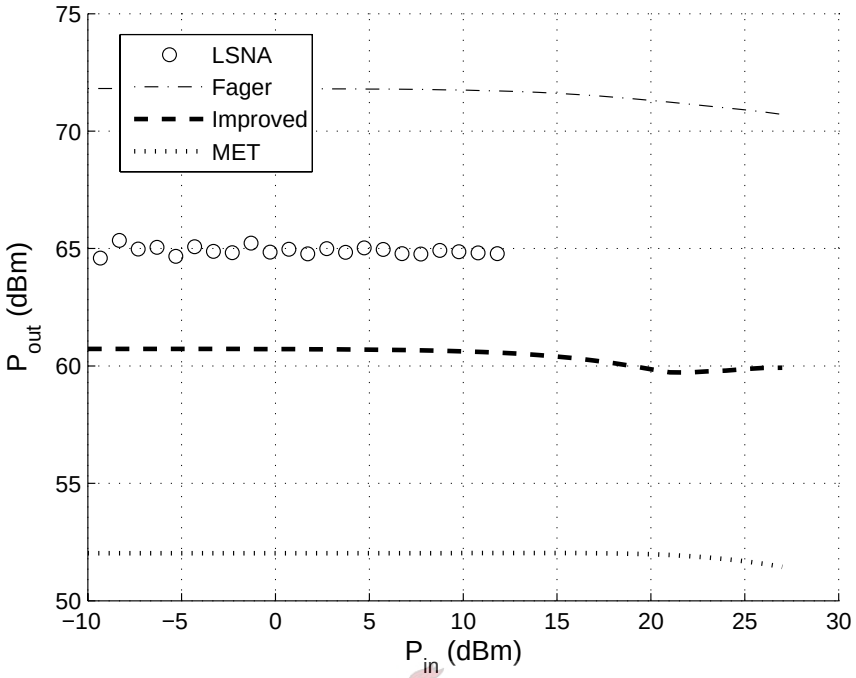


Figure 5.19: Compared voltage phase over input power at 1.6GHz for the measured MRF282 LDMOSFET and three different large-signal models at $V_{gs} = 4.2V$ and $V_{ds} = 20V$.

5.4 Two-Tone IMD Verification of Models

The IM3 predictions are verified for class-AB operation for the original Fager, improved Fager and MET models and are plotted in figure 5.21. The lack of availability of more than one preamplifier limited the measured data to maximum input power levels of 8.5 dBm. Two tones were applied at a centre frequency of 1.6 GHz, with a tone separation of 200 kHz. The third order intermodulation power is accurately predicted by the Fager and improved Fager models, but the MET model's prediction varies with almost 10 dB from the measured data.

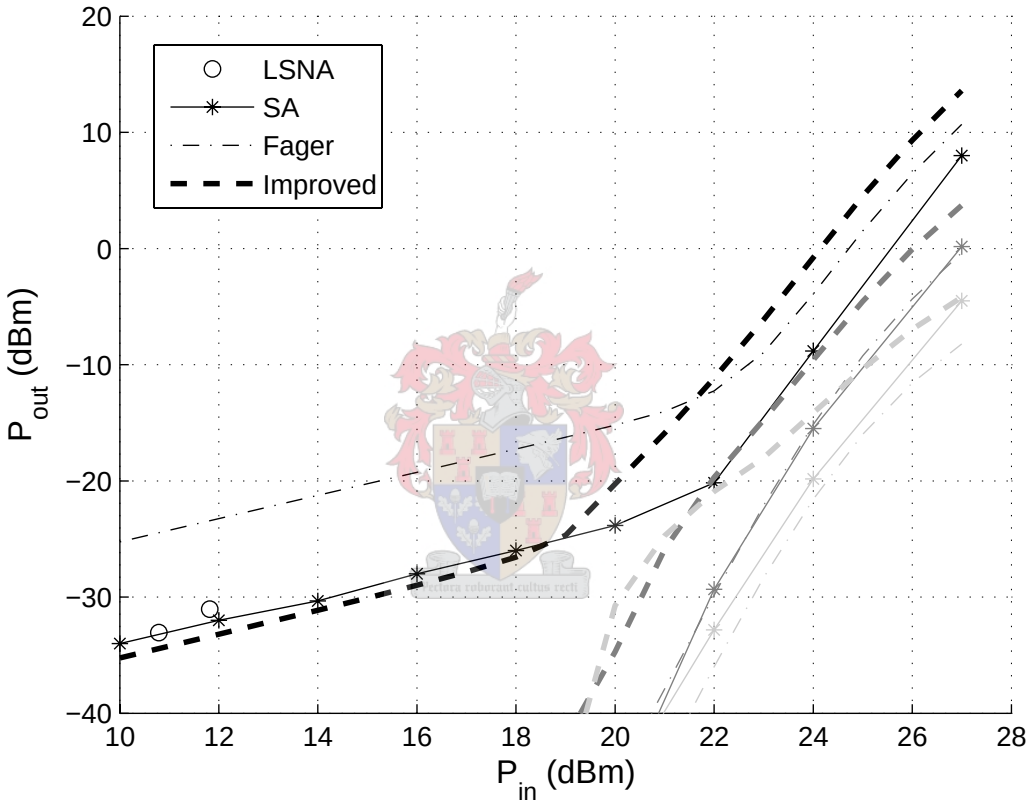


Figure 5.20: Compared 1st (black), 2nd (gray) and 3rd (light gray) harmonic output power over input power at 1.6 GHz for the measured MRF282 LDMOSFET and two different large-signal models at $V_{gs} = 2.5V$ and $V_{ds} = 20V$.

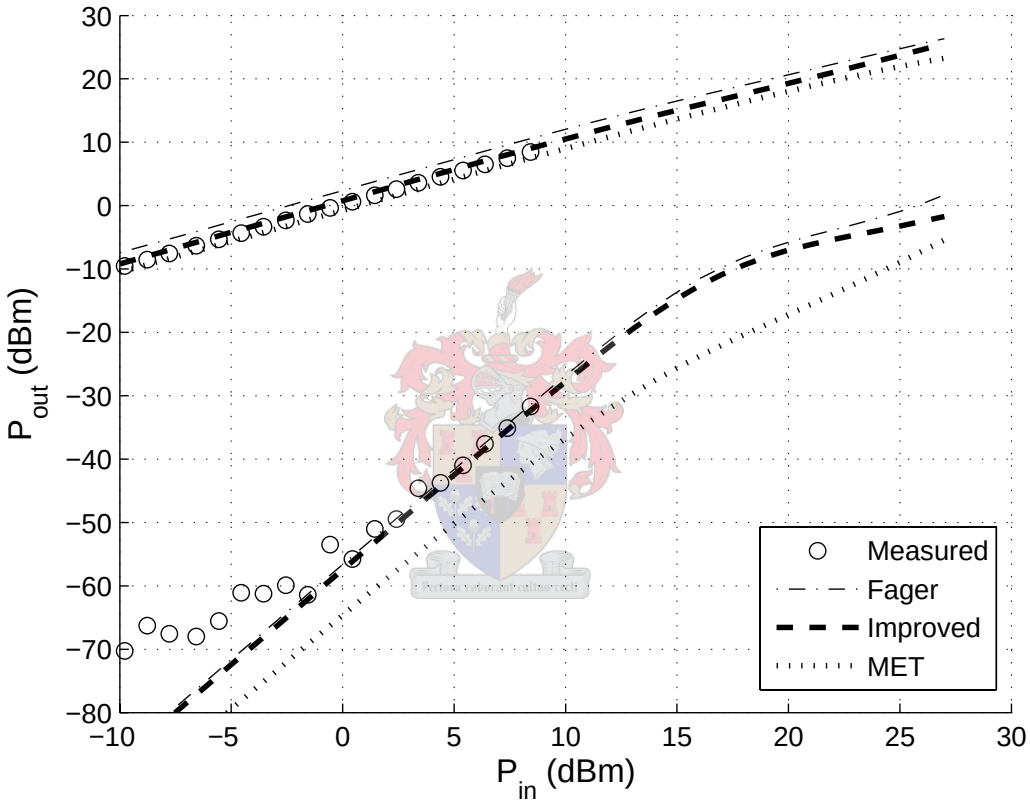


Figure 5.21: Compared IM3 prediction at 1.6 GHz for the measured MRF282 LDMOSFET and three different large-signal models at $V_{gs} = 4.3V$ and $V_{ds} = 20V$. Two tones are applied at a centre frequency of 1.6 GHz, with a tone separation of 200 kHz.

5.5 Conclusions

The Fager, improved Fager and MET models were verified against measured data, and the ability of the models to predict the linear and nonlinear behaviour of the MRF282 LDMOS transistor was evaluated. The models were found to predict the small-signal behaviour in each of the four regions of bias with reasonable accuracy, except for S_{21} in the saturation region, where all of the models failed to produce reasonable prediction accuracies. Because linear amplifiers are usually not biased in this region, the accuracy of the models is not extremely important here. The improved Fager model produced extremely accurate magnitude and phase predictions for S_{21} in the quadratic and linear regions.

The ability of the models to accurately predict single-tone harmonic power and phase as a function of input power was evaluated for class-AB and class-C operation. For class-AB operation, all of the models were able to predict the output power with reasonable accuracy, while the improved Fager model delivered the most accurate results. The phase prediction was found to be most accurate for the improved Fager model, but reasonably accurate for the other models. The Fager and improved Fager models were evaluated for class-C operation, but were unable to predict the power of the harmonics with reasonable accuracy. The basic trend for class-C operation was observed for both of the models and it is believed that more accurate results can be obtained if the model parameters are tuned more carefully.

The IM3 predictions for the three models were evaluated for class-AB operation. The Fager and improved Fager models produced extremely accurate predictions of the intermodulation power, while the MET model differed with almost 10 dB from the measured data.

The Fager and improved Fager models were found to predict the overall linear and nonlinear behaviour of the MRF282 device with reasonable accuracy, and the prediction accuracies of the two models exceeded that of the MET model in many of the cases. The results for each of the models should prove useful when designing linear amplifiers and can be used to identify where further improvements can be made.

Chapter 6

Conclusions

6.1 Introduction

This thesis provided a detailed discussion of the development of nonlinear CAD models for the design of linear LDMOS power amplifiers. An improved characterisation test setup was developed to enhance measurement accuracy and two nonlinear models were constructed using the measured data. The two nonlinear models and the industry standard MET model were evaluated against linear S-parameter measurements and nonlinear single-tone and two-tone measurements. The two models compared reasonably well with the measured data and exceeded the prediction accuracy of the MET model in many cases. An overview of the individual achievements is given in this chapter and future developments for this project are discussed.

6.2 Overview of Achievements

The known sources of TRL calibration error were investigated to determine the calibration sensitivity for the different errors. It was found that the largest error could be prevented by manufacturing the lengths of the through and DUT standards as accurately as possible, and to ensure that the reflect standards are identical. Other important findings are listed below:

- The standards should be manufactured on the same sheet of laminate so that a minimum deviation in ϵ_r occurs between standards.
- A laminate should be chosen so that the effective permittivity stays sufficiently constant over the required bandwidth.
- Care should be taken so that the microstrip tracks have the same width and a very smooth etch-line.

- The standards should not be covered with any kind of conformal coating or silk screen, except when the high-frequency properties of the coating are well known.

A highly accurate multiline TRL calibration kit was developed to perform measurements on a 10 W LDMOS power FET. Calibration verification standards were added to the kit and the residual calibration errors were determined after calibration to be less than -40 dB between 0.4 and 8 GHz. Different removable coaxial to microstrip transitions were investigated and two methods were found to reduce the reflection at the transitions. The reflection was reduced with a peak of 16 dB at 7 GHz, which lowers uniformly to 0 dB improvement at approximately 1 GHz.

The stability of the MRF282 LDMOSFET was verified for all the relevant bias conditions. The device was characterised using a VNA, controlled by previously developed adaptive bias measurement software. A denser distribution of S-parameters was acquired in areas where changes occurred more rapidly inside the device. These areas were identified where the transitions between the linear, saturated and pinch-off regions occurred.

A series of GUIs were developed to aid the user in performing parameter extraction. The values of the extrinsic elements were determined using a starting-value-independent optimisation-based parameter extraction program. The extrinsic elements were used to perform the extraction of the small-signal equivalent circuit for each of the measured bias points. The complete extraction of the model could be performed within minutes due to the high time-efficiency when using this method. The extracted small-signal data were evaluated and graphs were shown to illustrate that the model was sufficiently accurate in the three most relevant regions of bias.

The Fager nonlinear model was implemented and the parameters for the nonlinear equations were determined. It was found that the Fager nonlinear capacitor equations lacked the capability to accurately model the intrinsic capacitances over all the relevant bias points. This is mostly due to the fact that the capacitances inside the device are dependent on two controlling voltages in stead of one.

A new large-signal model was proposed that implements two nonlinear charge sources to model the effect of the three intrinsic capacitors. The two charge sources were modeled with dependency on both the gate and drain voltages, so that an improved modeling accuracy was obtained. The nonlinear charge equations were derived by examining each of the numerical voltage derivatives of the charge and implementing simple mathematical functions that represent the trend of the calculated data. The equations were fitted on the data and a good match was obtained for each of the derivatives.

The Fager, improved Fager and MET models were verified against measured data, and the ability of the models to predict the linear and nonlinear behaviour of the MRF282 LDMOS transistor was evaluated. The models were found to predict the small-signal behaviour in each

of the four regions of bias with reasonable accuracy, except for S_{21} in the saturation region, where all of the models failed to produce reasonable prediction accuracies.

The IM3 predictions for the three models were evaluated for class-AB operation. The Fager and improved Fager models produced an extremely accurate prediction of the intermodulation power, while the MET model differed with almost 10 dB from the measured data. The Fager and improved Fager models were found to predict the overall linear and nonlinear behaviour of the MRF282 device with reasonable accuracy, and the prediction accuracies of the two models exceeded that of the MET model in many of the cases.

6.3 Future Development and Recommendations

The software for the extraction of the small-signal equivalent circuit allows for future improvement so that the model can be used over a wider frequency range. The small-signal model topology can also be improved so that the model can be used over a wider frequency range.

A considerable amount of in-depth research can still be done on the improvement of the large-signal models. The ability of the Fager nonlinear drain current equation to model temperature effects plays an important role in the accurate modeling of I_{ds} and can be implemented using pulsed measurements. The test fixture developed in chapter 2 was designed to allow the use of resisistance temperature detector (RTD) probes, which can be implemented in the future. Further research can also be done on improving the modelling accuracy of R_{ds} for DC and RF operation.

List of References

[1] D. Schreurs, *Measurement Based Modelling of Heterojunction Field-Effect Devices for Non-Linear Microwave Circuit Design*, Ph.D. thesis, Catholic University of Leuven, 1997.

[2] S. Maas, "Measurements and Nonlinear Modeling," Nonlinear Technologies, Inc.

[3] J. Pritiskutch and B. Hanson, "Understanding LDMOS Device Fundamentals," *Microwaves & RF*, pp. 114–116, Aug. 1998.

[4] B. Hanson and J. Pritiskutch, "Relate LDMOS Device Parameters to RF Performance," *Microwaves & RF*, pp. 88–91, Nov. 1998.

[5] C.A. Engen and G.F. Hoer, "'Thru-Reflect-Line': An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer," *IEEE Transactions on Microwave Theory and Techniques*, vol. MTT-27, no. 12, pp. 987–993, Dec. 1979.

[6] Agilent Product Note 8510-8A , "Agilent Network Analysis Applying the 8510 TRL Calibration for Non-Coaxial Measurements," Agilent Technologies, 2001.

[7] Applied Wave Research , "Microwave Office," Version 6.52, 2004.

[8] R.F. Kaiser and D.F. Williams, "Sources of Error in Coplanar-Waveguide TRL Calibrations," National Institute of Standards and Technology.

[9] R.B. Marks, "A Multiline Method of Network Analyzer Calibration," *IEEE Transactions on Microwave Theory and Techniques*, vol. 39, no. 7, pp. 1205–1215, July 1991.

[10] D.E. DeGroot, D.K. Walker, and R.B. Marks, "Impedance Mismatch Effects On Propagation Constant Measurements," National Institute of Standards and Technology.

[11] D.C. DeGroot, J.A. Jargon, and R.B. Marks, "Multiline TRL Revealed," National Institute of Standards and Technology.

[12] National Institute of Standards and Technology , "MultiCal," Version 1.04a, 1998.

[13] National Institute of Standards and Technology , "Program MultiCal User's Guide," Revision 1.00, Aug. 1995.

[14] D.M. Pozar, *Microwave Engineering*, John Wiley & Sons, Inc., second edition, 1998.

[15] National Institute of Standards and Technology , "FindLen," Version 0.93, June 1996.

[16] The Mathworks, Inc. , "Matlab," Version 6.5, 2002.

[17] B. Wadell, *Transmission Line Design Handbook*, Artech House, 1991.

[18] M.D. Janezic and J.A Jargon, "Complex Permittivity Determination from Propagation Constant Measurements," *IEEE Transactions on Microwave Theory and Techniques*, vol. 9, no. 2, pp. 76–78, Feb. 1999.

[19] R.E. Massara, *optimization methods in electronic circuit design*, Longman Scientific & Technical, 1991.

[20] Application Note 5A-036 , "A Sub 1Ω Load-Pull Quarter-Wave Prematching Network based on a Two-Tier TRL Calibration," Maury Microwave Corporation, Dec. 2002.

[21] E.H. England, "A Coaxial to Microstrip Transition," *IEEE Transactions on Microwave Theory and Techniques*, pp. 47–48, Jan. 1976.

[22] M. Hughes, J. Sobol, and J. Caulton, "Measurements on the properties of microstrip transmission lines for MICs," *RCA Rev.*, vol. 27, pp. 377–391, Sept. 1966.

[23] M.L. Majewski, R.W. Rose, and J.R. Scott, "Modeling and Characterization of Microstrip-to-Coaxial Transitions," *IEEE Transactions on Microwave Theory and Techniques*, vol. MTT-29, pp. 799–805, Aug. 1981.

[24] Computer Simulation Technology , "CST Microwave Studio," Version 3.0, Feb. 2001.

[25] C. van Niekerk and D. Schreurs, "A new adaptive multi-bias S-parameter measurement algorithm for transistor characterization," *International Journal of Numerical Modelling: Electronic Networks. Devices and Fields*, 2005.

[26] C. van Niekerk, J.A. du Preez, and D.M.M.-P. Schreurs, "A New Hybrid Multibias Analytical / Decomposition-Based FET Parameter Extraction Algorithm With Intelligent Bias Point Selection," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 3, pp. 893–902, March 2003.

[27] T. Liang, J.A. Pla, P.H. Aaen, and M. Mahalingam, "Equivalent-Circuit Modeling and Verification of Metal-Ceramic Packages for RF and Microwave Power Transistors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 6, pp. 709–714, June 1999.

[28] K. Goverdhanam, J. Lott, S. Moinian, R. Li, J. Zell, S. Perelli, W. Dai, M. Frei, D. Farrell, D.A. Bell, and E. Lau, "Modeling High Power RF LDMOS Amplifiers," .

[29] C. van Niekerk, P. Meyer, D.M.M.-P. Schreurs, and P.B. Winson, "A Robust Integrated Multibias Parameter-Extraction Method for MESFET and HEMT Models," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 5, pp. 777–786, May 2000.

[30] C. van Niekerk and P. Meyer, "Performance and Limitations of Decomposition-Based Parameter-Extraction Procedures for FET Small-Signal Models," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 11, pp. 1620–1627, Nov. 1998.

[31] C. van Niekerk, *Multi-Bias Decomposition-Based Optimisation for the Extraction of Small-Signal GaAs FET Models*, Ph.D. thesis, University of Stellenbosch, July 1999.

[32] C. van Niekerk, "pcFET," Version 9.0, 2005.

[33] C. van Niekerk, "FET Parameter Extraction Software," Version 2, Aug. 2004.

[34] F. Lin and G. Kompa, "FET Model Parameter Extraction Based on Optimization With Multiplane Data-Fitting and Bidirectional Search- A New Concept," *IEEE Transactions on Microwave Theory and Techniques*, vol. 42, no. 7, pp. 1114–1121, July 1994.

[35] Cornell van Niekerk, "cvniekrk@sun.ac.za," Room E315, Electronic Engineering Building, University of Stellenbosch, Stellenbosch, South Africa.

[36] C. Fager, J. C. Pedro, N. B. de Carvalho, and H. Zirath, "Prediction of IMD in LDMOS Transistor Amplifiers Using a New Large-Signal Model," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 12, pp. 2834–2842, Dec. 2002.

[37] W.R. Curtice, J.A. Pla, D. Bridges, T. Liang, and E.E. Shumate, "A New Dynamic Electro-Thermal Nonlinear Model For Silicon RF LDMOS FETs," IEEE MTT-S International Microwave Symposium, Anaheim, 1999.

[38] W. Curtice, L. Dunleavy, W. Clausen, and R. Pengelly, "New LDMOS Model Delivers Powerful Transistor Library - Part 1: The CMC Model," *High Frequency Electronics*, pp. 18–25, Oct. 2004.

[39] S. Wood, R. Pengelly, L. Dunleavy, W. Clausen, T. Weller, and L. Emmadi, "New LDMOS Model Delivers Powerful Transistor Library - Part 2: Library Applications," *High Frequency Electronics*, pp. 26–32, Nov. 2004.

[40] S. Akhtar, P. Roblin, S. Lee, and J. Strahler, "Isothermal DC and Microwave Characterizations of Power RF Silicon LDMOSFETs," *IEEE Transactions on Electron Devices*, vol. 48, no. 12, pp. 2785–2789, Dec. 2001.

[41] S. Akhtar, P. Roblin, S. Lee, X. Ding, S. Yu, J. Kasick, and J. Strahler, "RF Electro-Thermal Modeling of LDMOSFETs for Power-Amplifier Design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 6, pp. 1561–1570, June 2002.

[42] G. Torregrosa-Penalva, A. Asensio-Lopez, and A Blanco-del Campo, "A Method to Obtain the Isothermal Static DC Curves of Microwave FET Power Amplifiers," *Microwave and Optical Technology Letters*, vol. 43, no. 5, pp. 378–380, 2004.

[43] K. Andersson, C. Fager, and J.C. Pedro, "A general procedure for extraction of bias dependent dynamic self heating model parameters," IEEE, 2005.

[44] Y. Yang, Y.Y. Woo, J. Yi, and B. Kim, "A New Empirical Large-Signal Model of Si LDMOSFETs for High-Power Amplifier Design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 9, pp. 1626–1633, Sept. 2001.

[45] D.E. Root and B. Hughes, "Principles of Nonlinear Active Device Modeling for Circuit Simulation," 32nd ARFTG Conference (Automatic RF Techniques Group), Dec. 1988.

[46] D. Snider, "Charge Conservation and the Transcapacitance Element: An Exposition," *IEEE Transactions on Education*, vol. 38, no. 4, pp. 376–379, Nov. 1995.

[47] I.W. Smith, H. Statz, H.A. Haus, and R.A. Pucel, "On Charge Nonconservation in FET's," *IEEE Transactions on Electron Devices*, vol. ED-34, no. 12, pp. 2565–2568, Dec. 1987.

[48] D. Divekar, "Comments on "GaAs Device and Circuit Simulation in SPICE"," *IEEE Transactions on Electron Devices*, vol. ED-34, no. 12, Dec. 1987.

[49] M.V. Calvo, A.D. Snider, and Dunleavy L.P., "Resolving Capacitor Discrepencies Between Large and Small Signal FET Models," IEEE, 1995.

[50] Technical Data 4T-090 revA , "Large-Signal Network Analyzer," Maury Microwave Corporation, 2003.