Tunable Evanescent Mode X-Band Waveguide Switch

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Declaration

I, the undersigned, hereby declare that the work contained in this dissertation is my own original work and that I have not previously in its entirety or in part submitted it at any university for a degree.

Signature: _____ Date: _____

Abstract

Keywords – Waveguide Switch, PIN Diodes, Evanescent Mode, Tunable Diode Mount, X-Band

A tunable X-band PIN diode switch, implemented in evanescent mode waveguide, is presented. To allow in-situ tuning of resonances after construction, a novel PIN diode mounting structure is proposed and verified, offering substantial advantages in assembly costs.

Accurate and time-effective modelling of filter and limiter states of the proposed switch is possible, using an evanescent mode PIN diode and mount model. The model is developed by optimizing an AWR Microwave Office model of a first order switch prototype with embedded PIN diode, to simultaneously fit filter and limiter measurements of four first order prototypes. The model is then used in the design of a third order switch prototype, achieving isolation of 62 dB over a 8.5 to 10.5 GHz bandwidth in the limiting state, as well as reflection of 15.73 dB and insertion loss of 1.23±0.155 dB in the filtering state over the same bandwidth.

A thermal model for the specific PIN diode employed in the switch, is developed using power measurements and physical characteristics of the diode. The third order switch uses a total of six PIN diodes, and successfully reflects a peak power level of 4 kW with a pulse width of 24μs at a 4.8% duty cycle.

The proposed switch is, to the knowledge of the author, the first multi-diode evanescent mode waveguide switch utilizing fully in-situ tunable diode mounts, while achieving specifications better than any published waveguide switch.

Opsomming

Sleutelwoorde – Golfleier Skakelaar, PIN Diodes, Golfleier Onder Afknip, Verstelbare Diodemontering, X-Band

'n Verstelbare X-band PIN diode skakelaar, geïmplementeer in onder afknip golfleier, word in hierdie proefskrif aangebied. Om in-situ resonansieverstellings na konstruksie te bewerkstellig, word 'n nuwe PIN diode monteringstruktuur voorgestel en geverifieer. Hierdie struktuur bied 'n aansienlike besparing in vervaardigingskostes.

Die gebruik van 'n onder afknip PIN diode- en monteringsmodel maak die akkurate en effektiewe modellering van filter- en beperkertoestande moontlik. Hierdie model is ontwikkel deur die optimering van 'n AWR Microwave Office model van 'n eerste-orde skakelaarprototipe met PIN diode, om die gelyktydige passing van filter- en beperkermetings van vier eerste-orde prototipes te bewerkstellig. Hierdie model word vervolgens gebruik in die ontwerp van 'n derde-orde skakelaarprototipe, waarmee isolasie van 62 dB oor die band 8.5 tot 10.5 GHz bereik word in die beperkende toestand. Weerkaatsing van 15.73 dB en insetverliese van 1.23±0.155 dB word oor dieselfde band in die filtertoestand gemeet.

'n Termiese model vir die spesifieke PIN diode wat in die skakelaar gebruik is, word ontwikkel deur van drywingmetings en fisiese diode-eienskappe gebruik te maak. Die derde orde skakelaar gebruik 'n totaal van ses PIN diodes, en is suksesvol getoets met 4 kW, 24μs pulse teen 'n dienssiklus van 4.8%.

Die voorgestelde skakelaar is, volgens die kennis van die skrywer, die eerste multi-diode onder afknip golfleierskakelaar wat van volledige in-situ vertelbare diodemonterings gebruik maak, en terselfdertyd beter resultate lewer as enige gepubliseerde golfleierskakelaar.

Acknowledgements

I would like to thank my Lord and Saviour, Jesus Christ.
Commit to the Lord whatever you do, and your plans will succeed. Proverbs 16:3

Further, I would like to express my sincere gratitude to everyone who has contributed to this dissertation in any way. In particular, I would like to convey my thanks to the persons and institutions below:

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Chapter 1

Introduction

1.1 Background

Microwave switches form and essential part of many microwave systems. Applications include routing of signals, as well as attenuation and limiting of high power input signals to protect the receiver, mixer or other circuitry. Most switches employ PIN diodes as control elements, appearing as very small impedances under forward bias and very large impedances under reverse bias. Conventional switch designs use a difference in input reflection rather than dissipation, leading to relatively little power dissipation in the diode itself. This enables small devices to control large incoming microwave power. Efficient thermal paths are however still necessary to minimize heating effects caused by power absorption within the diode junction.

A limiter is a self-activating switch, employing a detector diode with low forward voltage drop to effectively activate the switch at high incident power levels. Generally, this is accomplished by adding a Schottky detector diode in the transmission path, which senses the incident signal and then supplies sufficient current to drive the PIN diode into conduction.

Various switch and limiter configurations exist, which can be realized in material mediums ranging from coaxial line to waveguide. Design simplicity, suitability, performance and other factors need consideration before deciding on the optimal configuration. Simplicity refers to the manufacturing complexity of the overall limiter structure, including the diode mounting mechanism and number of diodes used in the design. Suitability of the design relates to the ease by which the design can be incorporated into an existing system. In a full waveguide system, integration of a switch implemented in waveguide eliminates the need for transitions to other circuit mediums. Performance considerations include

attaining the highest isolation and lowest receive loss when limiting, and the best VSWR and lowest insertion loss when filtering.

1.2 About The Dissertation

Switches using waveguides as transmission medium form an important class of these devices, as they offer very low loss at high frequencies, as well as very high power switching capability. Unfortunately, most existing switches only achieve this at the cost of small bandwidths and complicated assembly. In addition, the complex electromagnetic environment created by insertion of lumped-element devices in waveguide limits the accuracy of analysis and therefore design, resulting in expensive and time-consuming tuning procedures to achieve optimal performance.

Commercial limiters by Hill Engineering utilize PIN diodes in evanescent mode waveguide to improve bandwidth. The limiters are difficult to tune, as diode mounts are implemented as fixed structures in the waveguide. This dissertation presents a tunable PIN diode switch in evanescent mode waveguide, which achieves isolation of 62 dB over the band of 8.5 to 10.5 GHz in the limiting state, as well as reflection of 15.73 dB and insertion loss of 1.23±0.155 dB in the filtering state over the same bandwidth. The switch was successfully tested at a peak power level of 4 kW, with a pulse width of 24μs at a 4.8% duty cycle. To enable in-situ tuning, a novel PIN diode mounting structure is proposed and verified. This concept offers substantial advantages in assembly costs. The structure allows for very accurate modelling, which further reduces design time and cost.

The dissertation presents two main contributions and a number of secondary ones.

The primary contributions are:

- Design of a tunable evanescent mode waveguide PIN diode switch [1],
- Diode Mounting Topologies for X-Band Waveguide Switches [2].

The secondary contributions are:

- the development of a lumped element PIN diode model in evanescent mode waveguide,
- the development of an electric circuit analogue of the transient heating thermal model for the PIN diode and its mounting structure.

1.3 Layout

The dissertation commences with an overview of microwave switches and limiters in Chapter 2. Various PIN diode switches from literature are presented, followed by the introduction of the proposed switch structure. Since the PIN diode forms the active control element in the design, basic models and practical considerations when choosing a diode are presented in Chapter 3. Evanescent mode waveguide theory is discussed in Chapter 4. An overview of evanescent mode devices from literature provides a historical perspective of various systems and subsystems implemented in the below-cutoff environment. A first principles approach in Chapter 5 is used to validate the design equations for evanescent mode filters proposed in [3], after which a first order filter prototype is designed, simulated and measured.

Chapter 5 marks the end of the discussion of existing structures and techniques. In Chapter 6, a number of of new diode mount topologies are presented and evaluated using a first order filter prototype. The difference between the free-space and evanescent mode model of the PIN diode is established, and the evanescent mode model is used in a linear circuit solver package to accurately predict filter and limiter states of the switch for several new PIN diode mounting topologies. One of the diode mounts, a simple structure with in-situ tuning of resonances, is used in the design of a third order PIN diode switch in Chapter 7, meeting all low power specifications. The transient junction temperature rise of the diodes in the first branch of the third order switch is determined in Chapter 8. A practical PIN diode transient heating thermal model is developed by using the physical diode characteristics and a range of power measurements. The dissertation ends with a conclusion in Chapter 9.

Chapter 2

Microwave Switches And Limiters

2.1 Introduction

Limiting and switching components used in high-power radar systems form an integral part of the receiver front-end, as they provide critically important protection to the sensitive receiver from large signals. White [4] describes a limiter as *a two-port network which passes low power but attenuates high power signals.* Literature differentiates clearly between switches and limiters. The limiting action in a *switch* is achieved through externally switching the device on and off. A *limiter* may be described as a self-activating switch, allowing low level incident power to pass through in its normally "on" state and turning itself "off" at a high level incident power by rectifying its own "off" biasing current [5].

2.2 Ideal Microwave Limiter Configurations

Three working principles for limiters are found in literature, each employing a different type of diode, namely Point Contact and Schottky diodes, Varactor diodes and PIN diodes. Point Contact and Schottky diodes are capable of rectifying a microwave signal, Varactor diodes change capacitance characteristics at microwave frequencies through bias voltage variation and PIN diodes undergo RF conductivity modulation in the I-region when subjected to a large microwave current [4].

Point Contact or Schottky diodes may be used in a back-to-back limiter circuit configuration, as shown in Fig. 2.1, for rectification of microwave signals. The waveform is clipped on the positive and negative half of the waveform, resulting in a maximum output port voltage equal to the junction potential of the diodes. Small signals pass undisturbed.

Due to thin depletion layers for fast turn-on time and the required small microwave capacitance characteristics of the diodes necessary for the design, the resulting small diode volume cannot protect against very high power microwave signals [4].

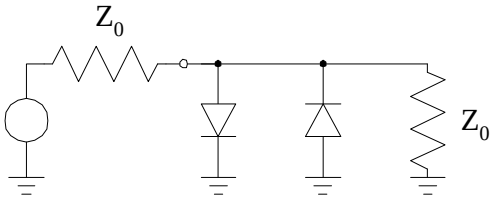


Figure 2.1: Back-to-back Limiter

Limiters using Varactor diodes are based on a resonance concept. A pair of back-to-back Varactor diodes may be parallel resonated by a shunt coil, as shown in Fig. 2.2. The average capacitance of the pair of Varactor diodes decreases at high power levels, resulting in a de-tuned filter at the centre frequency and associated increased reflection. Rectification of the microwave signal provides additional clipping and therefore increases limiting characteristics even further. The Varactor circuit configuration is restricted by the same small volume problem as the Point Contact or Schottky diodes, due to the small capacitance requirement for usable operating bandwidth.

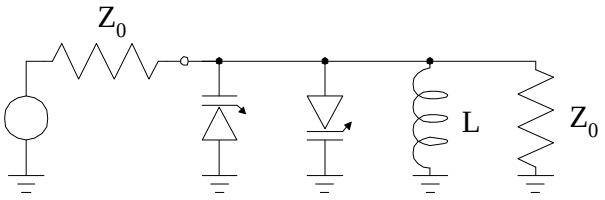


Figure 2.2: Varactor Diode Limiter (DC biasing not shown)

PIN diodes are incapable of rectification of microwave signals. Under zero bias and small signal conditions, a shunt PIN diode will show a high RF impedance to the transmission line. For large RF signals, holes and electrons injected into the I-region during the positive half cycle of the RF waveform are not fully withdrawn during the negative half cycle, leading to a steady-state distribution in the I-layer after a few cycles and an effective DC-bias. This biasing current changes the diode impedance from high to low, shunting the transmission line. The period from switch-on to steady-state, where very little limiting of the RF signal occurs, is known as the spike-leakage period. Following the spike-leakage period, the flat-leakage period provides high attenuation of the signal, presenting the same conductivity to positive and negative halves of the RF cycle. The necessary DC path carries away the DC current produced by the continual recombination process of the PIN diode, as shown in Fig. 2.3.

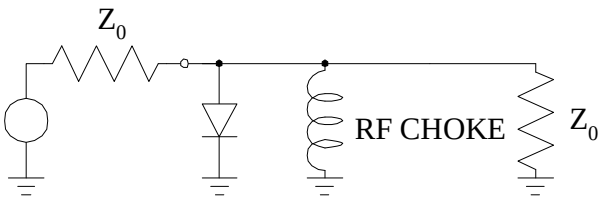


Figure 2.3: PIN Diode Limiter (DC biasing not shown)

Improved power limiting is possible by replacing the DC current path by a Schottky detector diode, with far lower forward voltage drop than the PIN diode, to switch on the PIN diode as fast as possible. In the case of a known high power signal in the vicinity of the Radar receiver, the limiter may be switched on actively, via the external DC bias feed, thereby by-passing the spike leakage period. An unknown high power signal will switch on the limiter passively.

2.3 Ideal Microwave Switch Configurations

In contrast to limiters, switches are turned on and off by external DC-bias currents. Virtually all high power switches use PIN diodes as switching elements, due to the large differences in RF impedance level between the on and off states. Conventional switch designs use a difference in input reflection rather than dissipation, leading to relatively little power dissipation in the diode itself. This enables small devices to control large incoming microwave power.

Three fundamental parameters describe PIN diode switch performance, namely isolation, insertion loss and PIN diode power handling limitation. The **isolation** is a measure of the incident microwave power not transferred to the load in the "on" state, due to attenuation and reflection losses. It is calculated as the difference between the power measured at the output port when the switch is ON and the power at the output port when the switch is OFF.

$$\text{Isolation (dB)} = \text{P}_{\text{out}}\text{on (dBm)} - \text{P}_{\text{out}}\text{off (dBm)} \tag{2.1}$$

The **insertion loss** of the circuit is the transmission loss through the switch structure in the "off" state. The absorption of signal power due to insertion losses cause the Noise Figure of the system to increase by the amount of the insertion loss, making it a troublesome parameter in receivers. The **PIN diode power handling limitation** defines the maximum incident power that a given switch can handle.

A basic consideration in ideal PIN diode switches is whether to use the diode in a series

or shunt configuration. A low characteristic impedance is required for the signal line in series configurations and a high characteristic impedance for shunt configurations of the PIN diode, to obtain the best isolation performance. The series SPST (Single Pole Single Throw) switch, as shown in Fig. 2.4, is used in broadband designs. The maximum isolation is dependent on diode capacitance, while the insertion loss and power dissipation are functions of the diode series resistance.

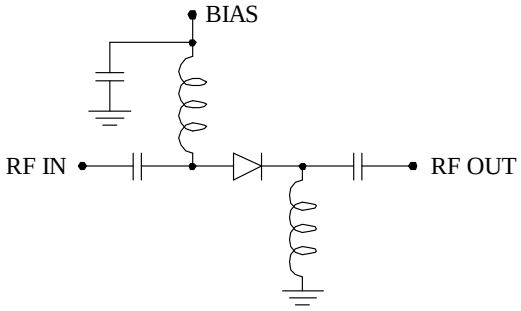


Figure 2.4: Series SPST Switch

The shunt SPST switch, as shown in Fig. 2.5, offers high isolation over a broad frequency range. Since there are no switch elements in series with the transmission line, the insertion loss is low. The circuit has a higher average power handling capability than the series SPST switch, since the diode is electrically and thermally grounded to one side of the transmission line [6]. In both topologies, the capacitance of the practical diodes usually has to be tuned out by parallel inductance, while the series inductance has to be cancelled by series capacitance.

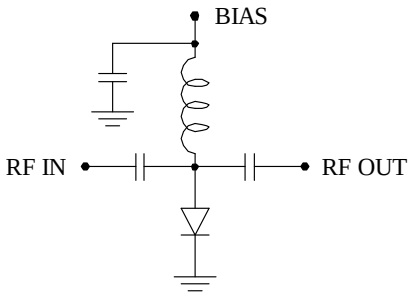


Figure 2.5: Shunt SPST Switch

Combinations of series and shunt mounted diodes may be used in compound switch configurations to improve overall switch performance. Broadband insertion loss of the series switch is combined with the broadband isolation of the shunt switch in various combinations. Two examples are given. The series-shunt SPST switch of Fig. 2.6 and the TEE SP3T switch of Fig. 2.7 offer overall improved performance.

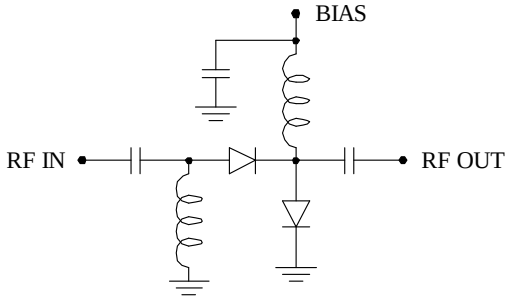


Figure 2.6: Series-Shunt SPST Switch

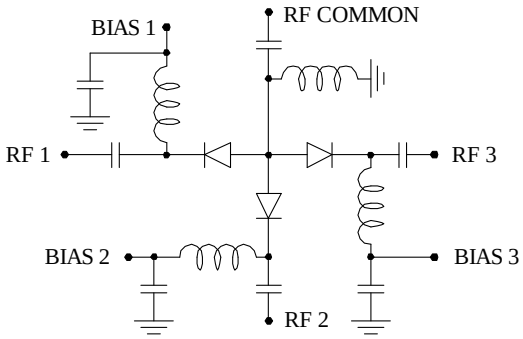


Figure 2.7: TEE SP3T Switch

Negative aspects of the compound configurations include degraded VSWR and insertion loss characteristics due to added circuit complexity, as well as increased bias circuit complexity, since not all diodes are simultaneously biased in the ON or OFF state [6]. Table 2.1 summarizes the isolation and insertion loss characteristics of the four circuits presented, where C_T and R_S are the PIN diode capacitance and forward bias series resistance, respectively.

2.4 Practical PIN Diode Switches

The ideal PIN diode switch configurations of the previous section may be implemented in various circuit topologies. A number of switches are discussed in this section according to their transmission line mediums, namely coaxial line, stripline, microstrip line and waveguide. Relevant examples from literature are described. It should be noted that, in comparison to other research fields, very little material is available on limiters/switches in open literature.

TYPE	ISOLATION (dB)	INSERTION LOSS (dB)
SERIES	$10\log\left[1+\frac{1}{(4\pi f C_T Z_0)^2}\right]$	$20\log\left(1+\frac{R_S}{2Z_0}\right)$
SHUNT	$20\log\left(1+\frac{Z_0}{2R_S}\right)$	$10\log\left[1+(\pi f C_T Z_0)^2\right]$
SERIES-SHUNT	$10\log\left[\left(1+\frac{Z_0}{2R_S}\right)^2 +\frac{1}{4\pi f C_T Z_0}\left(1+\frac{Z_0}{R_S}\right)^2\right]$	$10\log\left[\left(1+\frac{R_S}{2Z_0}\right) +(\pi f C_T)^2(Z_0+R_S)^2\right]$
TEE	$10\log\left[1+\left(\frac{1}{2\pi f C_T Z_0}\right)^2\right] +10\log\left[\left(1+\frac{Z_0}{2R_S}\right)^2+\left(\frac{1}{4\pi f C_T R_S}\right)^2\right]$	$20\log\left(1+\frac{R_S}{2Z_0}\right) +10\log\left[1+(\pi f C_T)^2(Z_0+R_S)^2\right]$

Table 2.1: Summary of Formulas for SPST Switches [6]

2.4.1 TEM Line Switches

Fisher [7] describes how the capacitance of a diode may be tuned out with a short-circuit length of transmission line of less than a quarter wavelength. The resulting circuit could be made to have properties similar to those of a simple quarter wave resonant stub [4], allowing the diode and stub combination to be implemented in a filter design. White [8] presents this concept in a 1-2 GHz SPDT switch, achieving a maximum insertion loss of 1.2 dB and a minimum isolation of 40 dB. The switch employs six PIN diodes, each at bias values of -150 V and 100 mA, and is tested to 6 kW peak power at 1200 MHz, for a 1 μs pulse length and 0.1 % duty cycle. It is fabricated with coaxial lines in a 50 Ω environment. Fig. 2.8 shows the concept of the designed SPDT switch with input directed to output 1.

The reverse breakdown voltage of diodes is the determining factor in the maximum power switching capability of the previous design. By reducing the transmission line impedance at the plane in which the diodes are mounted, the peak RF voltage may be reduced. To reach the point of reverse breakdown, the RF input in a stepped-impedance design, with maximum 50 Ω, must be higher than the RF input in a standard 50 Ω environment,

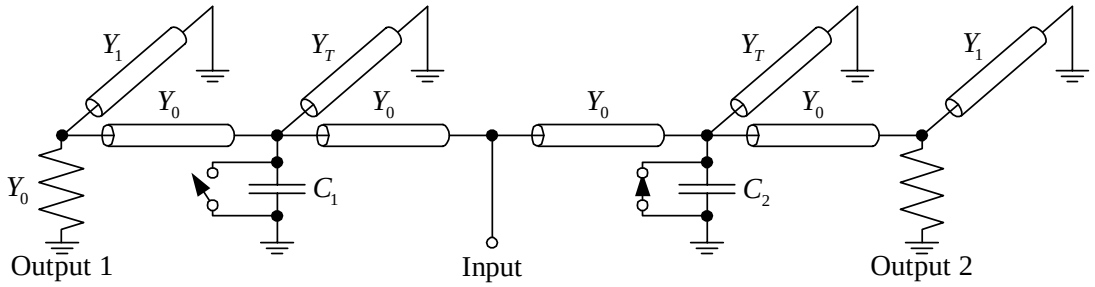


Figure 2.8: SPDT Switch With Input Directed To Output 1 [4]

resulting in an increased power handling capacity. This approach is used in the next design.

White [4] presents a SPDT switch implemented in 3-1/8 in. coaxial line, with the transmission line impedance stepped from 50 Ω to 0.83 Ω at the diodes. The final switch is implemented as an SPST switch and uses two switching rings with a total of 96 diodes, since at a pulse operation of 500 μs the switch requires as many diodes as would be needed for CW operation [4]. A schematic representation of the switch is shown in Fig. 2.9. Isolation of 30 dB is obtained with each diode biased at 100 mA from 1.2 to 1.4 GHz, while the insertion loss, measured at -100 V reverse bias, is below 0.5 dB. Small tuning capacitors are used to series resonate with the series inductances of the diodes. Peak switching is determined as 100 kW and 500 μs pulse width with -100 V reverse bias and 100 mA forward bias.

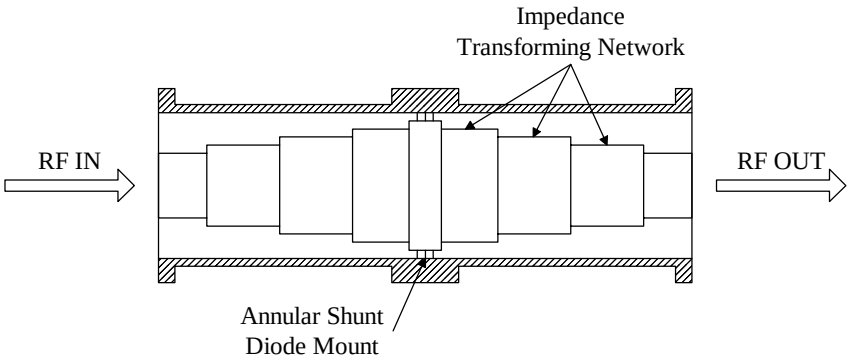


Figure 2.9: Stepped Impedance High Power SPST Switch

The physical nature of the stripline setup makes it ideal for implementing signal and bias feed isolation. White [4] presents an L-band SPDT switch incorporating four diodes. The switch directs transmitter power between two antennas. As shown in Fig. 2.10, two PIN diodes provide the isolation state at one output, while the other two PIN diodes produce the low loss transmission state at the other output. At any given time, all diodes are in

the same bias state. Series capacitance is used to tune the inductance of the diodes.

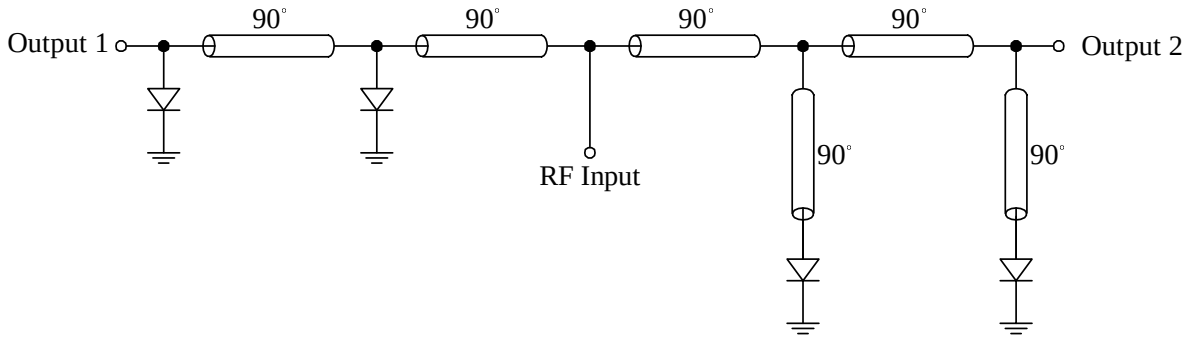


Figure 2.10: RF Schematic Diagram Of Stripline Switch [4]

The switch operates between 1030 MHz and 1090 MHz and achieves an input VSWR of 1.27:1, insertion loss less than 0.4 dB and isolation greater than 44 dB at both output ports. The switch is implemented in stripline with a centre board thickness of 0.254 mm and can handle approximately 3 kW peak power at -100 V reverse bias PIN voltage.

A two stage microstrip limiter, presented by White [4], has two diodes spaced along a transmission line in a shunt configuration, as shown in Fig. 2.11. Through proper lead lengths, series inductances are realized, forming a matched tee filter tuning out the reflection that would otherwise be introduced by the diode capacitance [4]. It has a peak power handling capacity of 1 kW with an input pulse of 1 μs pulse width and 0.1 % duty cycle at X-band, with a VSWR of 1.3:1 and insertion loss of 1.1 dB over a 3 GHz bandwidth. The switch is fabricated on a Teflon fibreglass substrate, using packageless chip diodes.

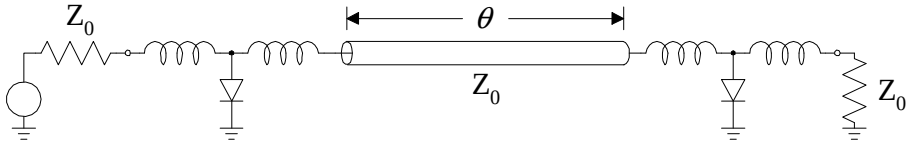


Figure 2.11: Microstrip Limiter Equivalent Circuit [4]

2.4.2 Bulk-effect Switches

A form of avalanche limiter can be obtained by implementing an ionisable dielectric medium, such as silicon [4]. The silicon is placed in a high electric field region of a resonant structure to ensure that limiting occurs at low incident RF power levels. In a waveguide switch, the silicon may be placed in the high electric field region of a resonant

waveguide iris, as shown in Fig. 2.12. The low power reactance of the silicon element at high frequencies is predominantly capacitive. Combined with the inductive nature of the metallic portion of the iris the parallel resonant condition is achieved at the centre frequency.

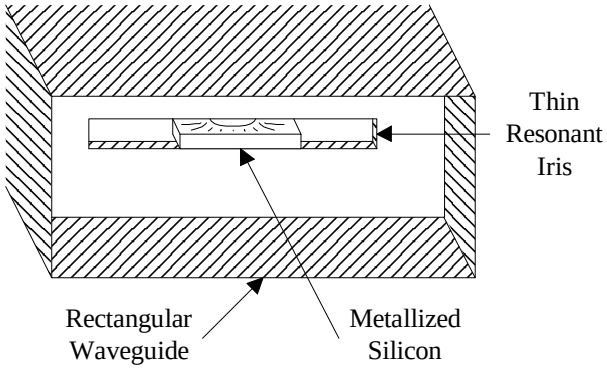


Figure 2.12: Waveguide Bulk Limiter

The equivalent circuit model of the metallic portion of the waveguide iris is derived from a three-port network where a short circuit at any port decouples the other two. The semiconductor element is represented as a lossy capacitive load at one port [4], as shown in Fig. 2.13.

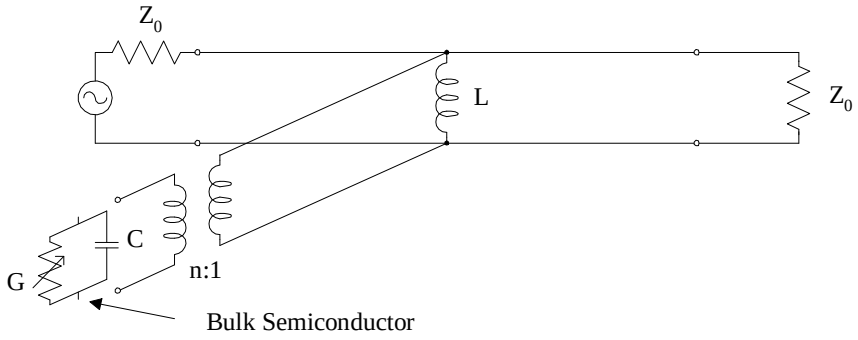


Figure 2.13: Equivalent Circuit of Resonant Iris Bulk Limiter [4]

2.4.3 Waveguide Switches

In applications where modest bandwidth, typically about 10%, and low insertion loss is required, waveguide is well suited due to its high characteristic impedance and low losses. It is, of course, best suited to full waveguide systems, eliminating the need for transitions to the limiter circuit medium. Various PIN waveguide switches exist, each utilizing the PIN diode capacitance and inductance, combined with external series inductances or

embedded coaxial stub structures to achieve the highest isolation, best VSWR and lowest insertion loss over the desired bandwidth. As the proposed evanescent mode PIN diode switch design is constructed in waveguide medium, various waveguide PIN diode switch designs are presented.

Stub Mounted Diode Switches

The principle behind the stub mounted diode design involves shunting the transmission line in which switching is required, utilizing a coaxial stub with embedded diode. Fig. 2.14 is used to explain this principle.

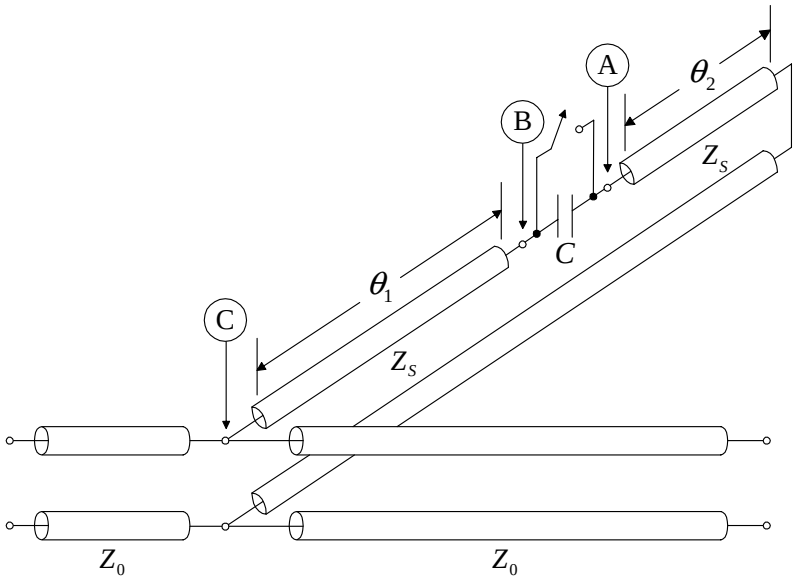


Figure 2.14: Embedded Diode in Shunt Stub [4]

The diode is represented by a simple switched capacitance and the total length of θ_1 and θ_2 is 180°. In the forward bias state, the diode is represented by a short circuit, resulting in a stub length of 180°. The short circuited end of the stub transforms to a short circuit shunting the main transmission line, providing the isolation condition. In the reverse bias condition, the diode is represented as a capacitance. Line lengths θ_1 and θ_2 are equal to 135° and 45°, respectively, while the magnitude of the characteristic impedance Z_S is equal to half the capacitive reactance of the diode capacitance, C [4]. The impedance at point A looking toward the short circuited end of the stub is $+jZ_S$; an inductive reactance of magnitude equal to the characteristic impedance of the stub. Looking toward the short circuited end of the stub at point B, the net impedance has now changed to $-jZ_S$ due to the capacitive nature of the diode. This value of net impedance at point B is then transformed to an open circuit at point C on the main transmission

line [4]. This results in perfect transmission on the line in the reverse bias state of the diode. The conditions described by White are not unique; there are other combinations of stub impedance and electrical lengths θ_1 and θ_2 which give perfect isolation and perfect matching for the two bias states of the diode [4]. Reverse switching mode is also possible by adding or subtracting 90° to θ_1. The result is an open circuit at point C in the forward bias state of the diode and a short circuit when the diode is reverse biased.

Implementation in a waveguide structure typically involves mounting a post with embedded diode between the walls of the waveguide and parallel to the electric field of the dominant TE_{10} mode. Lengths θ_1 and θ_2 may be adjusted by the DC sliding block position and connecting coaxial post protrusion lengths, as shown in Fig. 2.15.

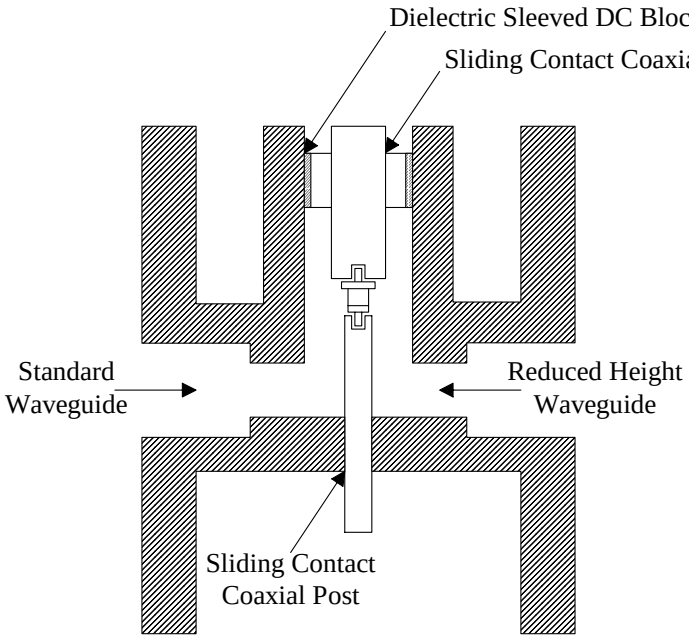


Figure 2.15: Side View of Waveguide Post Coupling Structure [4]

In a practical application for post coupling, a detector diode may be used to detect a portion of the RF signal and apply the rectified current to the bias terminal of the post-coupled PIN diode. This increases the switching speed. A dual diode model described by White [4] achieves 30 dB isolation, 0.8 dB insertion loss and 1.6:1 VSWR over a modest bandwidth of around 10%.

A waveguide stub switch may also be implemented by using series or shunt waveguide T-junctions, as shown in Fig. 2.16. A four-section narrow-band switch employing series waveguide T-junctions is presented in [9]. The design achieves an insertion loss in the passband of less than 0.5 dB, over a frequency of 120 MHz, in the “on” state, and an attenuation in the rejection band in excess of 80 dB, over a 10 MHz bandwidth, in the

"off" state.

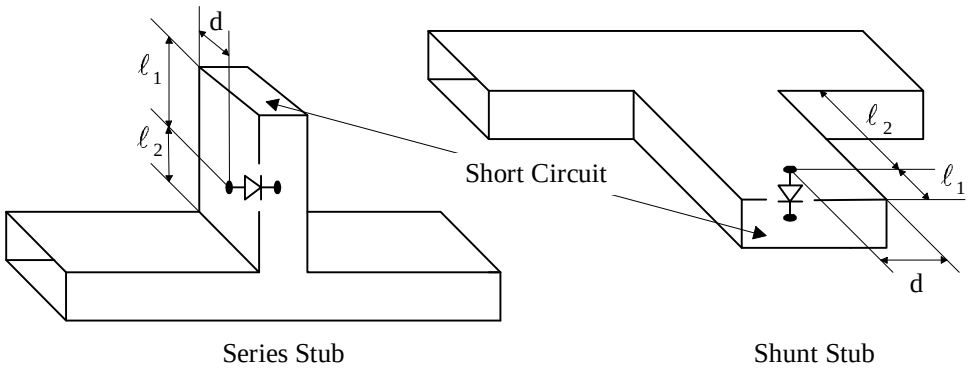


Figure 2.16: Waveguide Stub Switches [5]

Surface Oriented Bulk Window Switches

For high frequency, high power handling capabilities over a broad bandwidth, bulk effect switches possessing orthogonal bias and RF terminals have shown desirable characteristics. The concept involves placing a slab of high resistivity silicon, with P+ diffusions on the one side and N+ diffusions on the other side, across the waveguide window. The slab appears as a very large PIN diode with high capacitance. The RF signal, extending from the top to the bottom of the waveguide, is oriented at right angles to bias terminals and "sees" only the dielectric constant contribution of the silicon, together with some capacitance reactance of the metallized bias patterns across the slab [4]. The normalized shunt susceptance of the window is small compared to the waveguide admittance, resulting in little reflection in the pass state. The thickness of the window determines the rate of diffusion of the holes and electrons from P+ and N+ regions through the silicon, imparting a low resistivity in the forward bias state. With increasing forward bias, the isolation increases, while no bias is required in the transmission state.

Although the bulk window switch provides a great increase in peak power handling capability, its switching speed in the 1 to 10 μs range is often too slow to achieve the desired specifications. To improve this, the P+ and N+ regions are placed on the same side of the window, essentially generating a rectangular array of individual PIN diodes. The diode layout in Fig. 2.17 is that of Bakeman and Armstrong [10].

The design uses 600 PIN diodes fabricated in a single silicon slice across the waveguide. All diodes are connected in parallel by the metallic bias lines, which are perpendicular to the microwave electric field and therefore decoupled from the microwave signal [10]. Switching from a dielectric shunt to a resistive shunt in transmission and isolation states

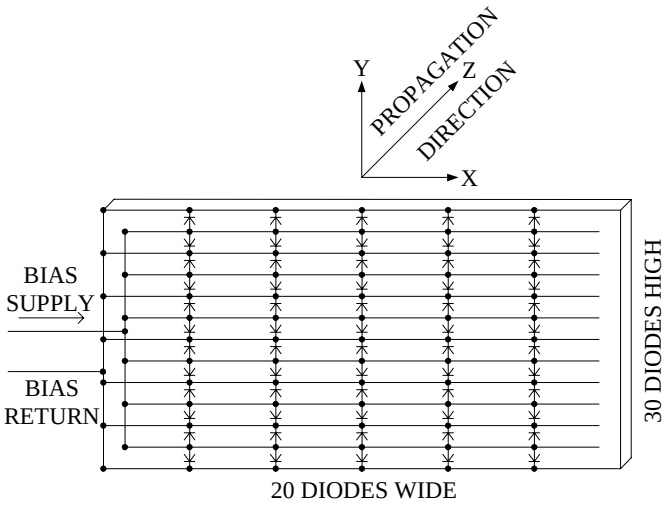


Figure 2.17: Schematic of Diode Layout on Silicon Switching Element [10]

respectively, the circuit may be analysed as a lumped element across the transmission line. Broadband characteristics may be achieved by tuning out the window susceptance over the desired frequency band. This SPST microwave switch presented by Bakeman and Armstrong [10] achieves isolation of 12 dB and insertion loss less than 1 dB over an octave bandwidth.

Reverse Switching Waveguide Switches

The switch design in this section is explained with reference to Dawson and DeLoach's X-Band switch [11]. Under conventional switching configurations, the isolation condition is achieved in the forward bias state of the PIN diode, while the switch allows energy to pass through when the diode is reversed biased. A short piece of coaxial transmission line in series with the PIN diode is incorporated in the wall of the waveguide. This represents an inductance in the microwave equivalent circuit model, denoted by Dawson and DeLoach [11] as L_{STUB}. Fig. 2.18 shows the equivalent circuit models under the forward and reverse bias conditions respectively. L_{PKG} is the package capacitance, R_H the holder resistance and R_T incorporates the combined holder and diode losses. In the isolation state, L_{STUB} and C'_{PKG} are series resonant, resulting in a high transmission loss, while in the receiving state, L_{PKG} and C_{PKG} are parallel resonant, yielding an open circuit condition with small transmission losses only due to the series resistance R_S. Peak Isolation of 22 dB, 12 dB over a 7% band and 0.4 dB insertion loss using a single PIN diode is achieved with the design.

The PIN diode ATR tube described by Sarkar [12] also operates under reverse switching

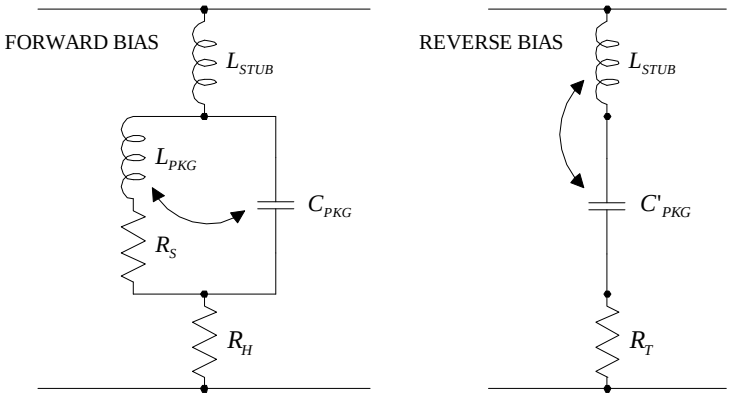


Figure 2.18: Equivalent Circuit of PIN Switch [11]

conditions. It utilizes a stepped post inductance, gap capacitance and PIN diode capacitance to produce series and parallel resonance conditions when reverse biased and forward biased, respectively. Isolation of 27 dB and insertion loss less than 1 dB was achieved over a 5% bandwidth using a single PIN diode. The configuration is shown in Fig. 2.19. The unit is able to handle 45 kW peak power at 1 μs input pulse width at a frequency of 9.375 GHz when the ATR tube is used in a branched duplexer with external DC bias.

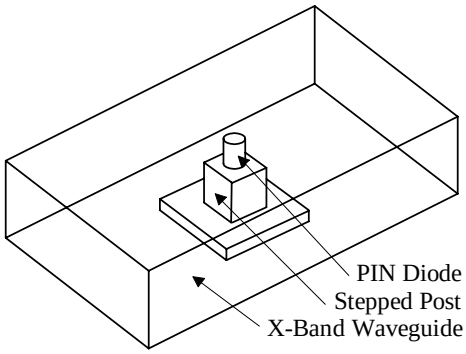


Figure 2.19: PIN Diode ATR Tube [12]

High Frequency Waveguide Switches

PIN diode controlled finline switches may be designed to operate over a very broad band at very high frequencies. A diode shunted finline switch presented in [13] displays broadband behaviour and is suited for frequencies up to 75 GHz. The basic structure is shown in Fig. 2.20, with diodes spaced a quarter wavelength apart at 35 GHz. The switch operates from 18 to 40 GHz, with adjustable attenuation between 1.5 and 25 dB across the band. The finline tapers are implemented on 0.254 μm 5880 RT-Duroid substrate.

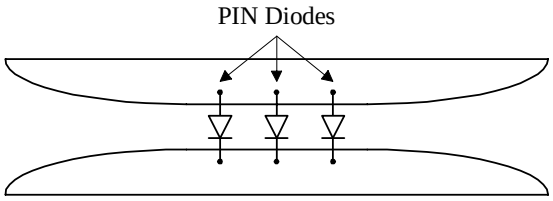


Figure 2.20: Diode Shunted Finline [13]

2.5 Proposed Switch Structure

The discussion in the previous section provides a brief overview of published limiter and switch configurations. While displaying a number of desirable characteristics, the waveguide PIN diode switches all suffer some of the following drawbacks:

- complex diode mount and bias structures
- low fractional bandwidths
- tuning of resonators involving the physical deconstruction of the device, slight modification and re-construction
- slow switching speed, high number of diodes [1]
- low power, in many cases.

In this dissertation, a high power waveguide switch displaying wide bandwidth and very simple diode mounting structure, which additionally offers in-situ tuning, is proposed. The proposed X-band prototype is implemented in evanescent mode waveguide with a novel diode mounting topology, allowing the operating frequency to be shifted after construction. Advantages of using evanescent mode waveguide include broadband operation and a reduction of size and weight. The basic structure is that of a pair of back-to-back PIN diodes in a vertical configuration between the broad walls of the below-cutoff waveguide, as shown in Fig. 2.21.

The capacitive nature of the PIN diodes in the reverse bias state is used to implement the central capacitive obstacle in an evanescent mode waveguide filter, and resonates with two adjacent susceptances, jB. In the forward bias state, the low resistance of the PIN diodes results in a thoroughly detuned filter. The diode mount and DC feed are implemented in such a way as to form a tunable capacitor, and thus a variable series resonance condition

[1] Bulk window switches

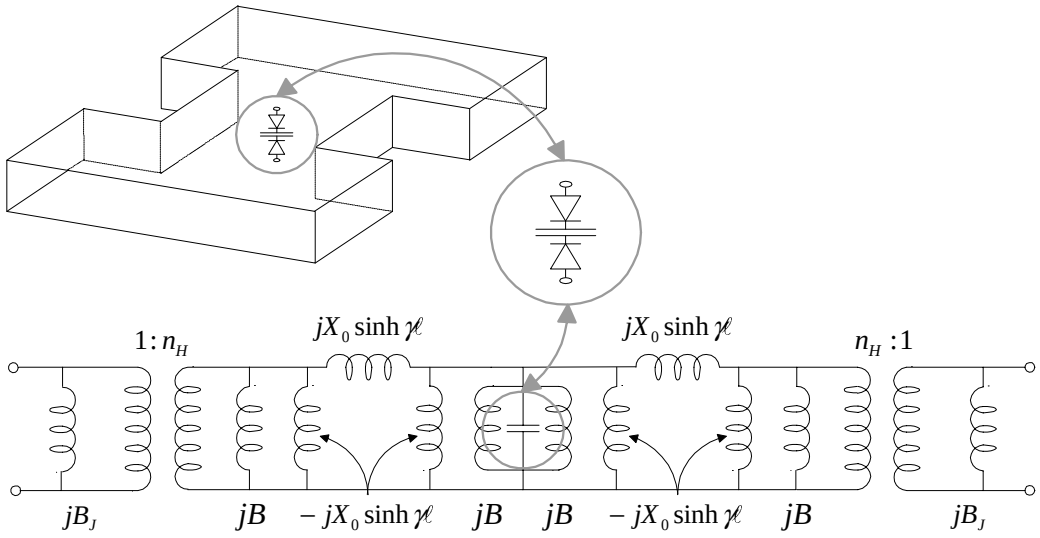


Figure 2.21: Basic Model and Equivalent Circuit Model of Proposed Switch

with the combined PIN diode inductances in both reverse and forward bias states. As well as providing a means to shift the operating frequency, the tunable capacitance also allows fine tuning of the structure for optimal performance, without necessitating structural changes to be made after initial production. This is a huge advantage, since diode mounts implemented in a manufactured switch may be tuned in-situ for the best performance characteristics, while being measured.

The following chapters describe the various components of the proposed switch, followed by several single-branch (2-diode) implementations and a final triple-branch (6-diode) switch. This switch has excellent performance characteristics, achieving a switch fractional bandwidth of 21%, with 15.73 dB reflection coefficient and 1.23±0.155 dB insertion loss when filtering, and 62 dB isolation when limiting. The switch was successfully tested at a peak power level of 4 kW with a pulse width of 24μs at a 4.8% duty cycle, with bias levels of all PIN diodes at -10 V in the reverse bias state and 150 mA in the forward bias state. This switch is, to the knowledge of the author, the first multi-diode evanescent mode waveguide switch utilizing fully in-situ tunable diode mounts, while achieving specifications better than any published waveguide switch.

Chapter 3

PIN Diodes

3.1 Introduction

Following the overview of PIN diode limiters and switches and brief introduction of the proposed switch structure in Chapter 2, the operation of the PIN diode is described in this chapter. The physical construction of the PIN diode, equivalent circuit model and thermal models are discussed.

A PIN diode is a semiconductor device operating as a variable resistor at RF and microwave frequencies, where the resistance value is determined solely by the forward bias current through the diode [6]. The ability to control large RF signals using far smaller DC excitation levels, makes the PIN diode ideal for switch, attenuator and limiter applications. A model of the PIN diode chip is shown in Fig. 3.1, where a P- and N-region have been diffused onto alternate sides of a wafer of almost intrinsically pure silicon.

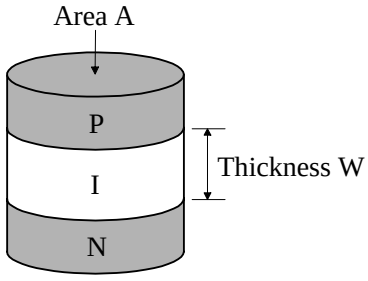


Figure 3.1: PIN Diode Chip

The selection of a PIN diode to perform a particular microwave switching function begins with the choice of the size of the I-region [4]. The thickness W of the I-region is a function of the original silicon wafer, while the area A depends on the size of the resulting chip.

In practice, the choice of diode is usually related to the required junction capacitance C_J, which depends on both A and W, the bulk breakdown voltage V_{BB}, which is proportional to W, and the thermal resistance. According to White [4], there are a number of basic considerations in selecting an appropriate diode, as listed in Table 3.1.

• Increased pulsed and average high power handling capability ↪ Heat sinking capability increased, since I-region volume increases. • Increased P_{AVE} dissipation capability ↪ More efficient path for heat flow from I-region to metallic base to which diode chip is mounted.	↑ P R O S	• High bulk breakdown voltage, V_{BB} ↪Advantage for high power switching. • Low transit time frequency ↪ Less tendency of rectification at μ-wave frequencies, a benefit for high power switching.
← Increased A		Increased W →
• Larger Area - larger C_J ↪ Limitation of RF circuit bandwidth. • Increased diode cost ↪ Fewer diodes per silicon slice. • Lower diode cutoff frequency ↪ Although R decreased, not enough to compensate for increased C_J, ↪ Increased insertion loss.	C O N S ↓	• Low transit time frequency ↪ Less tendency of rectification at μ-wave frequencies, drawback in self-actuation applications, ↪ Longer switching time. • Increased carrier lifetime ↪ Decreases switching speed. • Requires large bias I and V. • Net increase in I-region R with W. • High reverse bias voltage required to keep I-region fully depleted of charge with large RF voltages.

Table 3.1: I-region Cross Sectional Area, A, versus I-region Thickness, W

To summarize the properties listed in Table 3.1, the switching speed-power product of the PIN diode remains approximately constant [14], enabling a speed versus power handling capability trade-off by appropriate diode size variation. A thicker I-region diode would have a higher RF breakdown voltage and better distortion properties, while a thinner device would have faster switching speed [15]. The thicker I-region diode is desirable in high power active PIN switches, however less desirable in passive switches, due to a poor self actuation. The I-region affects RF switching performance through a larger area having a higher junction capacitance C_J, limiting the RF circuit bandwidth [4]. Further restrictions of the microwave characteristics are attributed to parasitic elements introduced by the package in which the PIN diode chip is housed, as shown in Fig. 3.2.

The parasitic resistance of the diode package and contacts limits the minimum resistance value, while the lowest impedance will be affected by the parasitic inductance L_{PIN}, which is generally less than 1 nH [15].

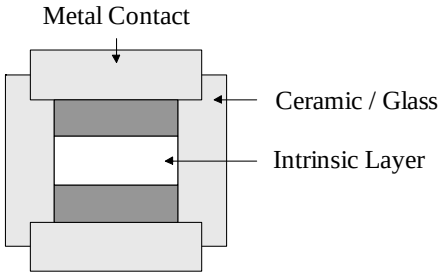


Figure 3.2: Complete PIN Diode Cross Section

The following parameters are used to specify a PIN diode:

C_J	-	junction capacitance at zero or reverse bias
C_P	-	parasitic capacitance introduced by diode package
R_S	-	series resistance under forward bias
R_P	-	parallel resistance at zero or reverse bias
L_{PIN}	-	parasitic inductance introduced by diode package
V_{BB}	-	bulk breakdown voltage, maximum allowable DC reverse bias voltage
V_B	-	DC reverse breakdown voltage at 10 μA, also V_{br}
τ	-	carrier lifetime, also TL
θ_{AVE}	-	average thermal resistance
P_D	-	maximum average power dissipation
θ_{pulse}	-	pulse thermal impedance
P_P	-	maximum peak power dissipation

3.2 PIN Diode Bias States

3.2.1 Reversed Biased PIN Model

When unbiased or reverse biased, the PIN diode is essentially a central insulator wedged between two outer metal sections in a parallel plate capacitor configuration, as shown in Fig. 3.3(a), with a value of

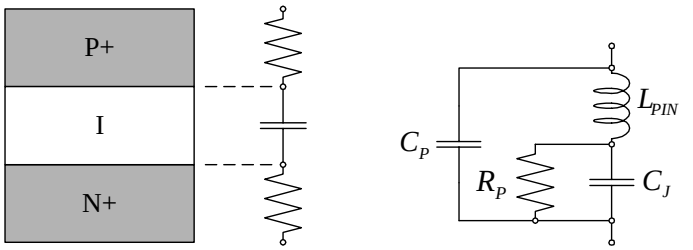
$$C_J = \frac{\epsilon_0 \epsilon_r \mathrm{A}}{\mathrm{W}}, \tag{3.1}$$

where ϵ_r is the dielectric constant of silicon, A is the the area, and W is the width of

the diode junction, as indicated in Fig. 3.1. The capacitance is usually measured at 1 MHz with the I-region fully depleted of charge. Eq. 3.1 is valid for frequencies above the dielectric relaxation frequency of the I-region

$$f > \frac{1}{2\pi\rho\epsilon} \tag{3.2}$$

where ρ is the resistivity of the I-region and $\epsilon = \epsilon_0\epsilon_r$. At lower frequencies the PIN diode acts like a Varactor diode, with voltage variable capacitance.



(a) PIN Diode Chip (b) Complete PIN Diode

Figure 3.3: Reverse Bias PIN Diode Model

The shunt parallel resistance R_P represents the net dissipative resistance in the reverse biased diode. It is proportional to voltage and inversely proportional to frequency. In most RF applications its value is higher than the reactance of capacitance C_J, and is therefore less significant [15]. In a practical PIN diode the package adds an additional shunting capacitance C_P, of typically 0.2 to 0.4 pF [16], depending on the package employed, as well as a series inductance L_{PIN}, as shown in the complete reverse bias model in Fig. 3.3(b).

To create the central resonance condition of the evanescent mode filter structure as discussed in Sec. 2.5, two PIN diodes are mounted in a back-to-back configuration in various diode mounts suited to the waveguide structure, as discussed in Chapter 6. The diode mount creates additional capacitance C_C, as part of the mount, to serially resonate with the PIN diode inductances L_{PIN}, in both forward and reverse bias states. The basic reverse biased PIN and mount model is shown in Fig. 3.4.

3.2.2 Forward Biased PIN Model

In the forward bias state, holes and electrons from the P and N regions respectively are injected into the central I-region. The I-region is thereby converted to a conducting electron hole plasma medium [16]. Due to the finite recombination time known as the carrier lifetime τ, a small quantity of average stored charge Q lowers the effective resistance

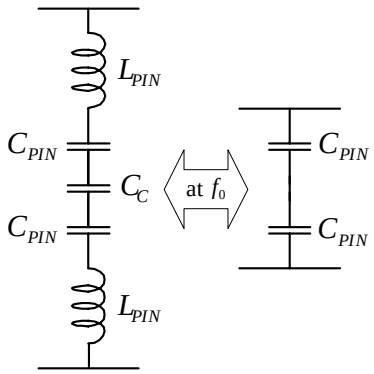


Figure 3.4: Basic Reverse Bias PIN And Mount Model

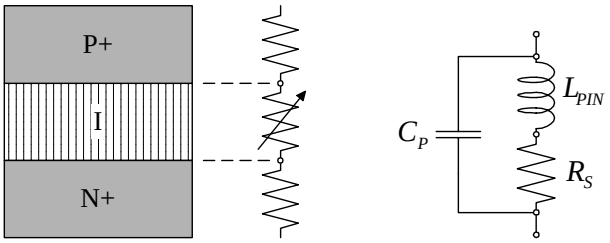
of the I-region to

$$R_S = \frac{\mathrm{W}^2}{(\mu_n + \mu_p)Q} \qquad [\Omega], \tag{3.3}$$

where $Q = I_F \times \tau$ [Coulombs], I_F is the forward bias current, and μ_n and μ_p are the electron and hole mobility respectively. Eq. 3.3 is valid for all frequencies higher than the I-region transit time frequency,

$$f > \frac{1300}{\mathrm{W}^2} \qquad [\mathrm{MHz}], \tag{3.4}$$

where W is in μm, assuming that the RF signal does not affect the stored charge [15]. The circuit model for the forward biased state thus consists of fixed resistances from the P and N regions in series with the variable resistance of the I-region, as shown in Fig. 3.5(a). The large range of the variable resistance allows the diode to be used as a current-controlled resistance. Completing the model to include parasitic package elements gives the complete forward bias model shown in Fig. 3.5(b).



(a) PIN Diode Chip (b) Complete PIN Diode

Figure 3.5: Forward Biased PIN Diode Model

In the forward bias state, the series resonance condition between the mount capacitance C_C, and combined PIN diode inductances L_{PIN}, remains as in the reverse bias state. The central capacitance required for the evanescent mode filter is replaced by forward bias

resistance of the PIN diode, R_S, resulting in a thoroughly detuned resonator section. The basic forward biased PIN and mount model is shown in Fig. 3.6.

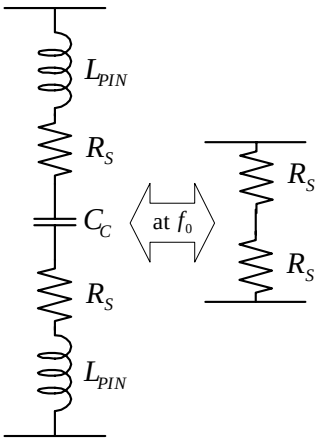


Figure 3.6: Basic Forward Bias PIN And Mount Model

3.3 Switching Speed

The switching speed in any PIN diode application depends on the driver circuit as well as the PIN diode [15]. The two switching speeds in question are the time it takes to switch from forward to reverse bias, T_{FR}, and from reverse to forward bias, T_{RF}. The carrier lifetime τ, of the diode affects the forward to reverse bias time T_{FR}, which may be calculated using the forward current I_F, and the initial reverse current I_R, as

$$T_{FR} = \ln\left(1 + \frac{I_F}{I_R}\right)\tau[s]. \tag{3.5}$$

The reverse to forward bias time, T_{RF}, is primarily dictated by the width of the I-region. The forward bias current reduces the magnitude of the built-in junction potential. This causes holes to diffuse from the P to the N region and electrons to diffuse from the N to the P region. The charge injected into the I-region cannot be removed in the brief duration of a half cycle of RF frequency if that RF frequency is above a few hundred megahertz [4]. A switching speed model of the PIN diode is shown in Fig. 3.7.

Long lifetime does not necessarily imply slow switching speed. Driver design plays a crucial role and may be employed to remove I-region charge in a period shorter than the lifetime [4]. To appreciate a simple switched versus natural recovery of a PIN diode, consider a forward current I_F, permitted to flow in the diode for a long time. The charge stored in the diode is $Q_0 = I_D \cdot \tau$, where $I_D = I_F$. Employing a reverse current I_R to reach

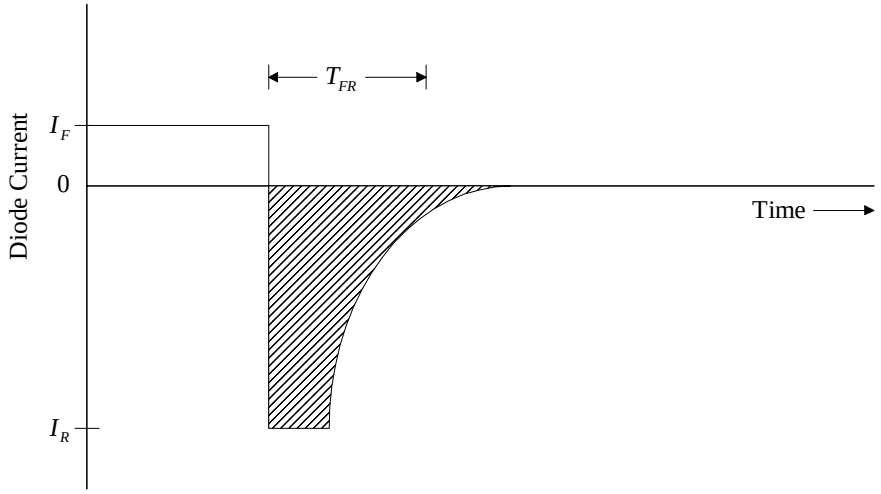


Figure 3.7: Switching Speed Model Of PIN Diode [15]

a diode current of $I_D = I_R - I_F$, and assuming total charge recovery in a discharge period, τ_S, $Q_0 = (I_R - I_F) \cdot \tau_S$. The lifetime τ, and approximate switching time from forward to reverse bias τ_S, are determined through the technique described. Manufacturers provide values for forward and reverse current I_F and I_R, along with minority carrier lifetime TL. In a practical driver circuit, the forward bias current would of course be switched off during reverse bias. The charge versus time profiles are shown in Fig. 3.8.

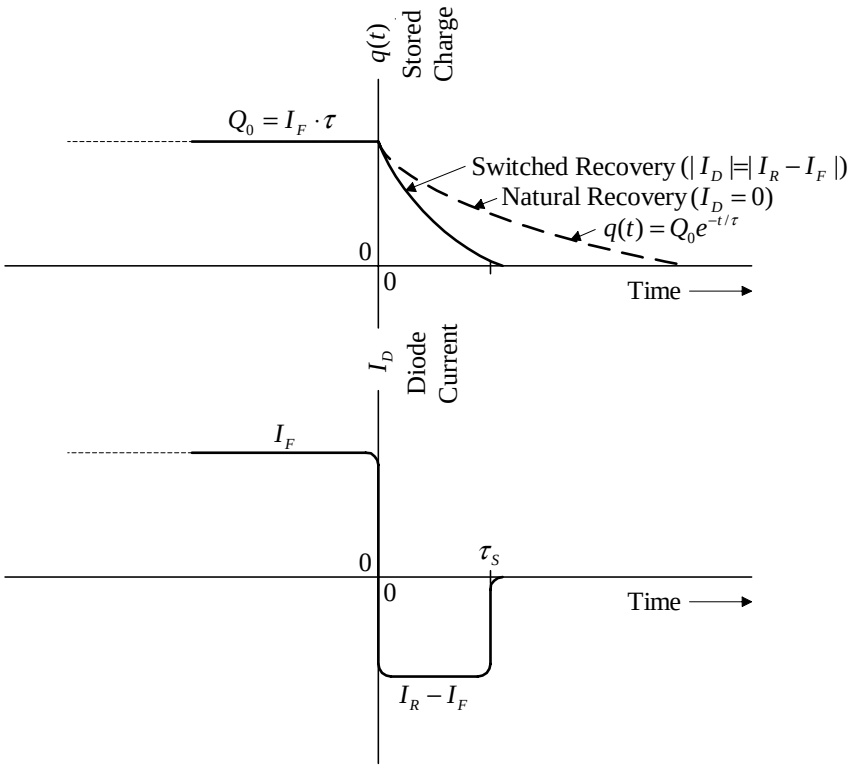


Figure 3.8: I-region Charge and Diode Current Versus Time [4]

3.4 Thermal Model

The operating temperature of any electronic component is an important value specified by the manufacturer. The maximum average power dissipation, P_D, of PIN diodes is determined by the maximum allowable junction temperature T_J, ambient temperature T_A, as well as average thermal resistance θ_{AVE} of the diode, as follows:

$$P_D = \frac{T_J - T_A}{\theta_{AVE}}. \tag{3.6}$$

Thermal resistance θ_{AVE} is defined as the ratio of steady state temperature (°C) rise of the junction per watt of steady state power dissipated within it [4]. It is measured by dissipating a known amount of DC power in the diode and using the diode junction voltage as a thermometer to measure the resulting temperature rise. In typical applications the maximum allowable junction temperature is 175°C and the ambient temperature around 25°C, allowing a maximum temperature change of 150°C per diode. The average thermal resistance θ_{AVE} may be used to represent the diode in CW applications.

The temperature of a thermal conducting device does not rise instantaneously when heated. The tempo at which the temperature rises is determined by the thermal capacitance, C_T. For silicon PIN diodes, the I-region heat capacity, HC, described by Eq. 3.7, is the amount of energy required for a unit increase (1°C) in the I-region temperature in the absence of heat flow from the diode [4], and is also known as the thermal capacitance of the diode. $\mathrm{V_{I\text{-}region}}$ and D are the I-region volume and effective diameter respectively.

$$\mathrm{HC} = (\text{specific heat} \times \text{density})_{\text{silicon}} \cdot \mathrm{V_{I\text{-}region}} \tag{3.7}$$

$$\mathrm{HC} = \frac{1.4\mathrm{D}^2\mathrm{W}}{\text{cubic centimetre}} (\text{joules}/^\circ\text{Celsius}) \tag{3.8}$$

The analysis of absence of heat flow from the diode into the heat sink, is used to calculate the limit of the maximum I-region temperature rise $\Delta\mathrm{T_M}$ above the heat sink as

$$\Delta\mathrm{T_M} < \mathrm{P_D} \cdot \mathrm{t/HC}, \tag{3.9}$$

referring to the temperature rise during each pulse occurring during the short pulse length, t, and assuming that the heat from previous pulses has been dissipated. The product of the steady state heat thermal resistance θ_{AVE} and the I-region heat capacity HC, is known as the minimum thermal time constant τ_T.

$$\tau_\mathrm{T} = \theta_{AVE} \cdot \mathrm{HC} \tag{3.10}$$

An average power dissipated in the I-region, P_D, will increase the junction temperature by an amount ΔT_M above that of the heat sink as described by Eq. 3.9. Since cooling is neglected, the bound given by Eq. 3.9 increases without limit as the pulse length, t, increases. A steady state condition is reached when the change in temperature ΔT, is large enough to permit dissipation of P_D through the thermal resistance θ_{AVE}, to the heat sink [4], as shown in Fig. 3.9. Eq. 3.9 therefore proves useful when estimating the maximum temperature rises for pulses shorter than the minimum thermal time constant, τ_T. The minimum thermal time constant is therefore described as the time taken before the diode reaches steady state operation.

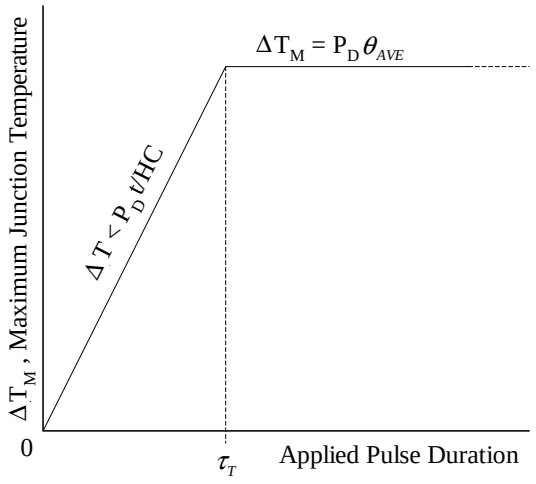
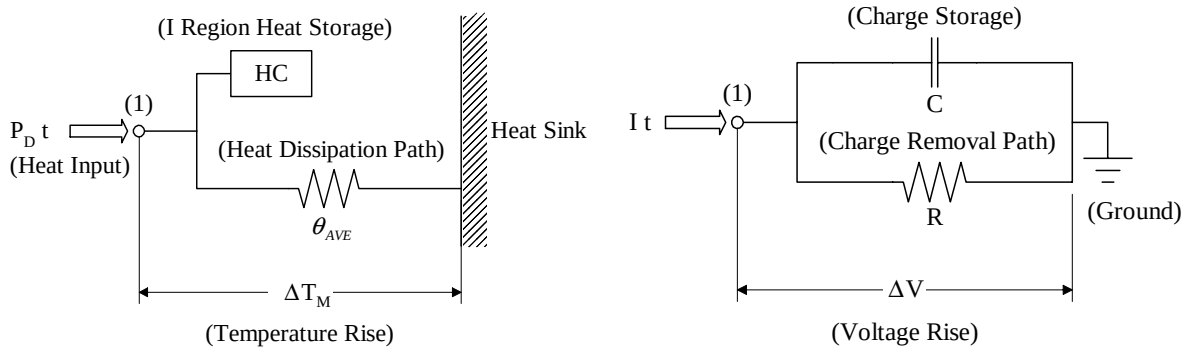


Figure 3.9: Maximum Diode Temperature Rise Estimates Using θ and HC [4]

A more realistic temperature contour is determined since the I-region power dissipation P_D produces heat - only some of which increases I-region temperature by at most ΔT_M. The temperature rise however causes heat to flow out of the I-region through resistance path θ_{AVE}, as shown in Fig. 3.10.



(a) Simplified Diode Thermal Model (b) Electric Circuit Analogue

Figure 3.10: Simplified Thermal Models for Transient Diode Heating [4]

The instantaneous total heat flow input, P_D, must be equal to the change in heat storage, HC·d(ΔT_M)/dt, plus the heat $\Delta T/\theta_{AVE}$ lost by the thermal path to the heat sink [4], described by the differential equation

$$P_D = HC \cdot \frac{d(\Delta T_M)}{dt} + \frac{\Delta T_M}{\theta_{AVE}}. \tag{3.11}$$

White [4] describes the solution for the temperature rise ΔT_M, with thermal time constant $\tau_T = \theta_{AVE}$·HC, as

$$\Delta T_M = P_D \cdot \theta_{AVE} \left[1 - e^{-t/\tau_T}\right]. \tag{3.12}$$

Fig. 3.11 illustrates the difference between the straight line approximation of Eq. 3.9 and more realistic junction temperature profile of Eq. 3.12.

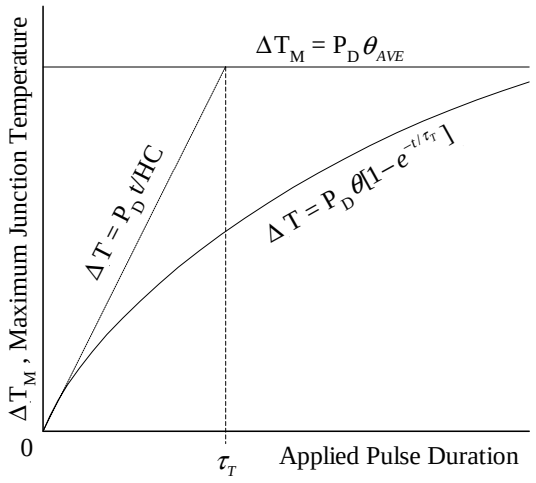


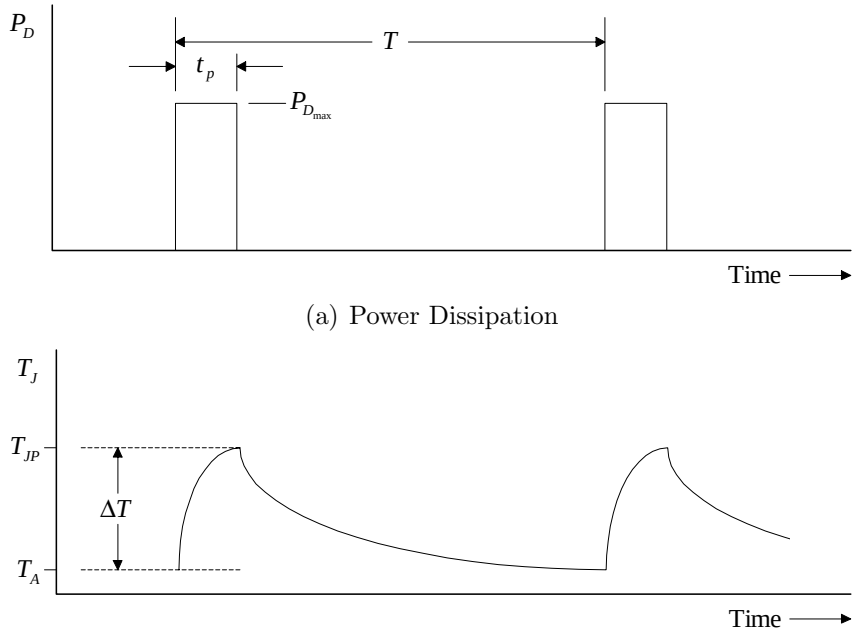
Figure 3.11: Pulsed Temperature Rise Profile of PIN Diode Using Minimum Time Constant Model [4]

The voltage rise in the electric circuit analogue of Fig. 3.10, ΔV, at node (1) represents the I-region temperature rise ΔT_M, at node (1). Dissipation by resistance R, and charge storage by capacitance C, correspond to dissipation by thermal resistance θ_{AVE}, and heat storage by HC respectively. A detailed electric circuit analogue for the chosen PIN diode is presented in Sec. 3.5, offering a practical solution for "measuring" the thermal response of the actual PIN diode.

In pulsed RF and microwave applications it is important to prevent thermal runaway of the PIN diodes. For an interpulse period of more than $5\tau_T$, the junction temperature, T_J, will cool between pulses to the temperature of the heat sink, T_S [4]. The junction temperature response following the heating pulse is described by

$$T_J = T_S + \Delta T_M e^{-t_{interpulse}/\tau_T}, \tag{3.13}$$

where ΔT_M is the temperature reached at the end of the heating pulse. Fig. 3.12 indicates how junction temperature is affected during a pulsed RF application, with an interpulse period, $t_{interpulse} = T - t_p > 5\tau_T$.



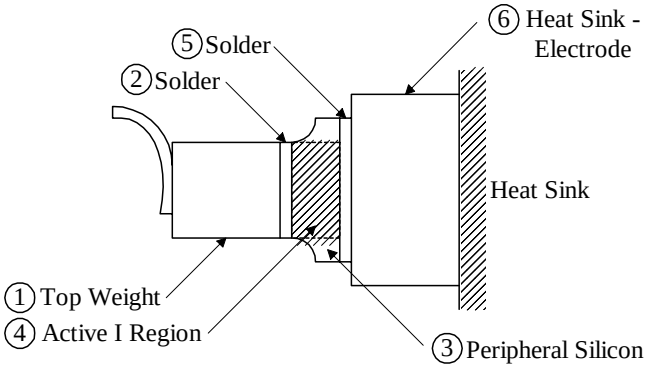
(a) Power Dissipation

(b) Junction Temperature

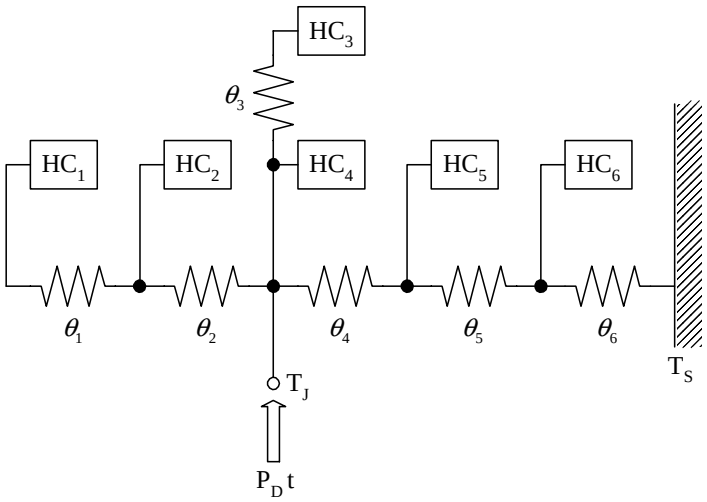
Figure 3.12: Power Dissipation and Junction Temperature In Pulsed RF Application [15]

Designing with the minimum thermal time constant τ_T, and the maximum pulsed temperature rise ΔT_M of Eq. 3.12, ensures diode operation well within its survivable region. The actual junction temperature, T_J, is likely to be lower than the theoretical upper temperature bounds. This is explained by considering the construction of a real PIN diode, as shown in Fig. 3.13(a). The corresponding thermal model proposed by White [4] is shown in Fig. 3.13(b). It has more than one temperature node and a number of time constants in the final solution of the junction temperature, T_J. The more precise model predicts a lower value for ΔT than the conservative result of Eq. 3.12.

A fundamental difference between the practical PIN diode construction presented in [4] and the Micrometrics MMP7067 PIN diode used in the proposed switch design, is the absence of the top weight in the Micrometrics MMP7067 PIN diode. According to Mortenson [17], a semiconductor element is often top loaded at the junction strap contact by adding a block of material, top weight, possessing high heat capacity comparable at least in size to the semiconductor element so as to act as a peak heat storage element to minimize the rapid temperature response of the element to pulse dissipation. This has the effect of lengthening the thermal time constant without adding to the thermal resistance of



(a) Practical PIN Diode Construction



(b) Detailed Transient Heating Thermal Model For Practical PIN Diode

Figure 3.13: Constructional PIN Detail and Detailed Thermal Model [4]

the total diode structure. Characteristics of the MMP7067 PIN diode are presented in Sec. 3.5, complete with practical PIN diode construction and electric circuit analogue.

3.5 Micrometrics MMP7067 PIN Diode

The main factors in diode choice for the proposed switch design are identified as:

- Correct junction capacitance, C_J, required for X-band evanescent mode filter,
- Minimum forward bias series resistance, R_S, for lowest junction temperature rise,
- Minimum thermal impedance, θ_{JC}, for highest power handling capacity,
- Correct package requirements for physics of diode mount structure.

The total diode capacitance, $C_D = C_{PIN}/2$, of a pair of back-to-back diodes, is the maximum overall diode capacitance. The additional tunable capacitance of the diode mount, C_C, in series with the total diode capacitance may be used to decrease the overall capacitance of the diode and mount. The junction capacitance value is therefore chosen as 0.2 pF, which is slightly more than double the required central capacitance of the evanescent mode filter, as calculated in Chapter 4, to be able to tune operating frequencies below the original centre frequency of the basic filter. Desirable characteristics of low values of forward bias series resistance and thermal impedance are found in a high power switching diode. A cylindrical diode package is chosen to allow simple integration of the PIN into its mounting structure. The specifications of the diode used in this work, namely the Micrometrics MMP7067 high power switching and attenuation PIN diode in a CS32 ceramic package, are listed in Table 3.2.

V_{br}[1] MIN	(V)	500
C_J-10 V[2] MAX	(pF)	0.2
TL[3] TYP	(μs)	1.5
R_S[4]@ 1mA MAX	(Ω)	10
R_S[4]@ 10mA MAX	(Ω)	4
R_S[4]@ 100mA MAX	(Ω)	1.0
θ^5_{JC} MAX	(^{o}C/W)	12

Table 3.2: Micrometrics MMP7067 PIN Specifications

Notes:

1. Reverse Breakdown Voltage measured at 10 μA.
2. Junction Capacitance measured at -10 volts at 1 MHz.
3. Minority Carrier lifetime measured with $I_F = 10$ mA, $I_R = 6$ mA. With a good driver, the MMP7067 should be able to switch in 150 ns. Lifetime varies from 1.0 - 2.0 μs [18].
4. Series Resistance measured at 1 GHz using transmission line techniques.
5. It takes about 4 thermal time constants for the device to reach the Thermal Impedance (thermal time constant of silicon is 12.6 μs), therefore about 50.4 μs [18].

Maximum Ratings

Operating Temperature	-55^{o}C to 150^{o}C
Storage Temperature	-65^{o}C to 200^{o}C
Reverse Breakdown Voltage (V_{br})	from 25 volts to 500 volts at 10 μA
Junction Capacitance (C_J-10)	from .03 pF to .5 pF at 10 volts
Switching Speed (T_S)[1]	from 1 ns to 25 ns
Lifetime (TI)	from 5 ns to 2.0 μs
Chip Thickness[2]	.004” - .007” thick

Notes:
1. The switching speed of the diode is dependent on the amount of current with which the diode is pulsed. Generally speaking, a diode may be switched 10 times faster than its lifetime [18].
2. Chip thickness of the MMP7067 is .010"±.004" (.254 ± .100 mm)

After discussion of the PIN diode basics with models of reverse bias and forward bias operating states, a suitable PIN diode is chosen for the proposed switch design. The final choice is the Micrometrics MMP7067 high power switching and attenuation PIN diode in a cylindrical CS32 ceramic package. While the general circuit and thermal models have been shown, specific models have yet to be discussed.

When used in evanescent guide, the value of the diode model capacitance changes quite drastically from its free-space value. The development of an accurate circuit model in evanescent guide is described in Chapter 6.

In order to predict the junction temperature rise in a diode, it is extremely important to have a thermal model for the specific diode. As specific models are non-existent, Chapter 8 is devoted to the description of a full thermal model for the specific diode in its mounting structure, based on manufacturers data and power measurements.

Chapter 4

Evanescent Mode Waveguide Theory and Devices

4.1 Introduction

The proposed switch is implemented in evanescent mode waveguide. Useful properties for resonators built in evanescent mode waveguide were first predicted by I.V. Lebedev and E.M. Guttsait in 1956 [19]. Their use in filters was proposed by W.A. Edson in 1961 and it was declared evident by George F. Craven and C.K. Mok in 1971 that resonant behaviour for any evanescent mode is possible if the appropriate conjugate terminating reactance is realized for that mode.

This chapter introduces various devices, subsystems and complete systems implemented in the below-cutoff environment. Advantages of this topology include simple tuning systems employing capacitive screws, lightweight construction and reduced component size. Evanescent mode filter design principles are presented and used to evaluate transitions between propagating and evanescent mode guide. A technique to measure obstacle admittance in below-cutoff guide, proposed by Mok [20], is used to calculate the evanescent mode equivalent admittance of a stub used in a first order filter. Dimensions for the transitions and filter are equivalent to those used in the first order switch design of Chapter 6.

4.2 Overview Of Evanescent Mode Devices

Evanescent mode waveguide is most commonly used in the implementation of microwave filters. The state-of-the-art is defined by a ten-section filter by Craven and Mok [3], shown in Fig. 4.1, implemented in aluminium X-band waveguide and operating over an

approximate 1 % bandwidth at H-band with a midband loss of 1.9 dB. It is designed to connect to propagating guide and employs simple screw obstacles with contact achieved by lock-nuts. The addition of fine tuning screws enables slight adjustments to be made accurately.

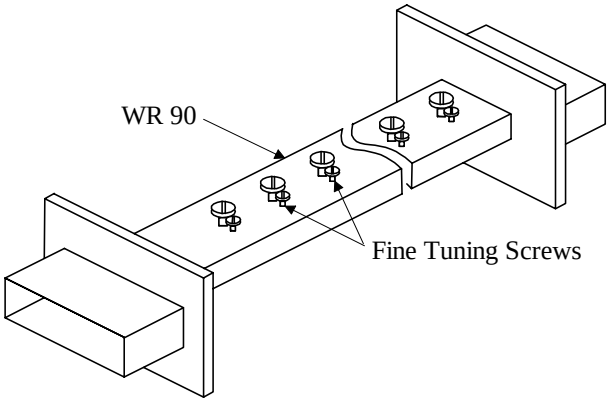


Figure 4.1: Ten-Cavity Maximally Flat Filter [3]

Bharj and Mak [21] present a transition from propagating waveguide to microstrip using evanescent mode guide, as shown in Fig. 4.2. Capacitive screws are used to adjust the electrical length of cutoff guide between two resonators. The transition is best suited for narrow bandwidth applications, since the junction susceptance formed between the propagating and evanescent mode guides limits broadband behaviour. The design achieves a return loss of approximately 20 dB from 11 to 12.5 GHz.

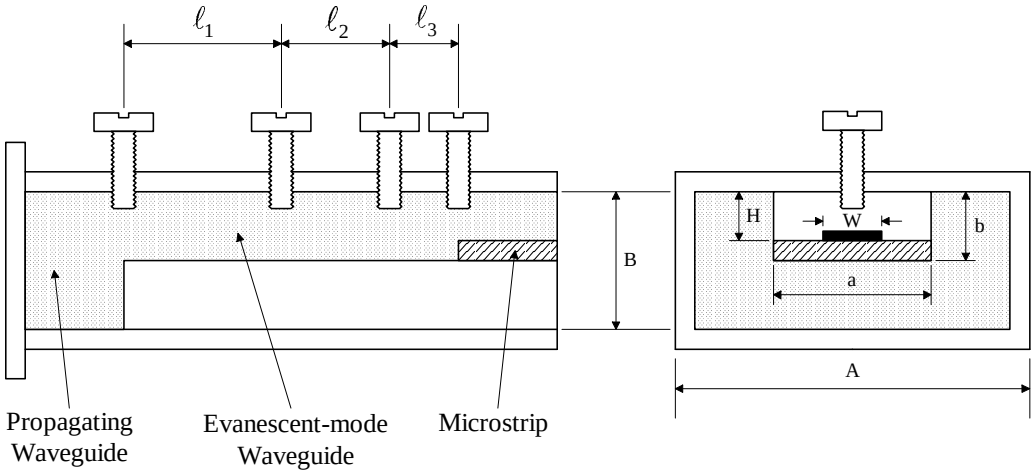


Figure 4.2: Transition from Propagating Waveguide to Microstrip using a Cutoff Waveguide [22]

An important transition in the proposed switch is that of propagating guide to evanescent mode guide, producing a junction susceptance. Tapers in the broad side between the two

guides, whether continuous or stepped, are not acceptable, due to the proximity to cutoff which is encountered at some stage in the taper [22]. Therefore, capacitive stubs have to be introduced to create parallel resonances with junction susceptances at the input and output of the proposed switch. These resonances are incorporated in the filter design.

A hybrid-T proposed by Craven [23] is shown in Fig. 4.3. As in the propagating hybrid-T, the isolation between the series and shunt arms of the below-cutoff equivalent is due to the symmetry of the construction.

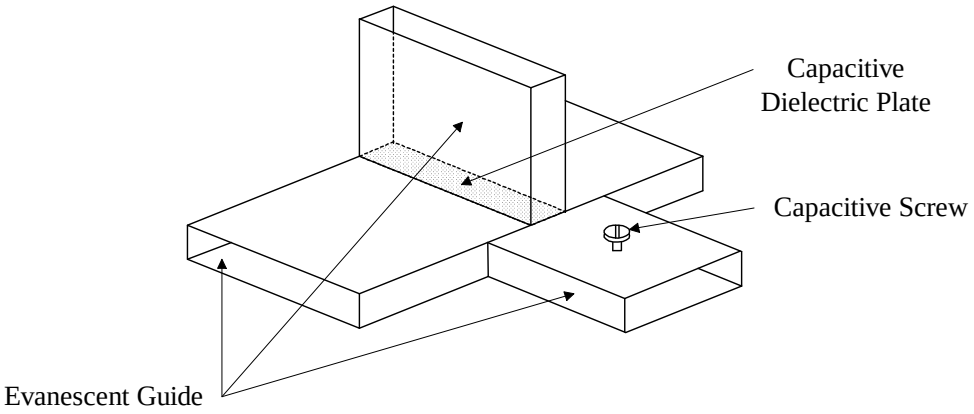


Figure 4.3: Hybrid-T using cutoff waveguide [23]

Microwave ferrite devices use the principle of non-reciprocal behaviour in a range of microwave components. D'Ambrosio [24] presents an important microwave component, a three-port circulator shown in Fig. 4.4, consisting of a cylindrical cavity, including a ferrite magnetised disc, and three evanescent mode coupling filters. A tuning plunger is used to obtain best performance results.

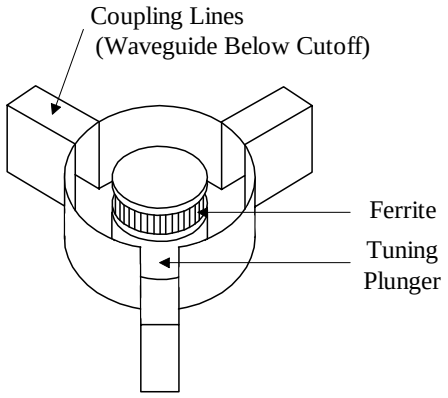


Figure 4.4: Three-Port Evanescent-Mode Circulator [24]

Reich and Schünemann [25] present a low-Q power combiner, which consists of a T-junction implemented in rectangular guide below cutoff, and coupled by an aperture to

propagating guide. Four Gunn diodes are mounted in the evanescent mode resonator, establishing a resonance condition only by the compound effect of the diode and screw capacitances and the guide "inductance". The unit achieves a bandwidth of 500 MHz at an input signal level of -13 dB below the output, and is shown in Fig. 4.5. The follow-

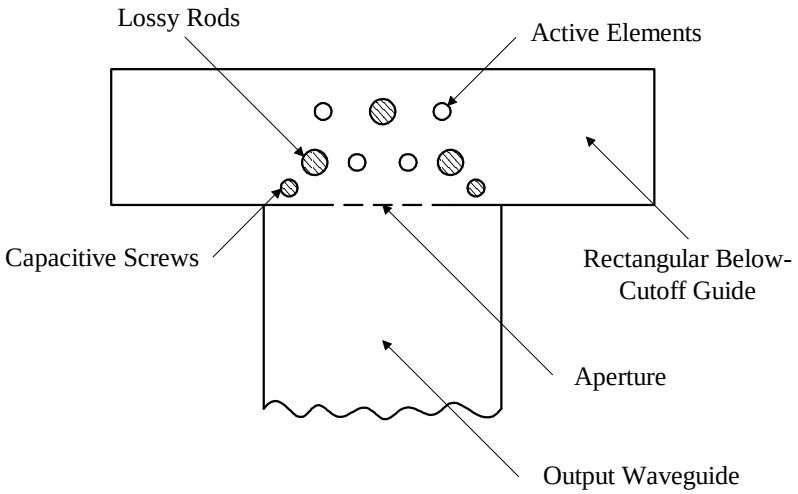


Figure 4.5: Low-Q Multi Device Oscillator [25]

ing characteristics of evanescent mode waveguide make the implementation of complete subsystems favourable: Absence of period resonances of distributed-constant networks, and Q-factors only slightly worse than propagating waveguide equivalents, make it ideal for broadband performance applications. In addition, greater attenuation of unwanted higher-order evanescent modes leads to reduced interaction with adjacent subsystems [22].

The design of a 1.9 - 7.6 GHz frequency multiplier in evanescent mode waveguide is presented by Dahele and Hill [26], and is shown in Fig. 4.6. Parasitic passband problems of the associated filters used in a propagating unit are eliminated. Estimated diode losses in the first and second diode mounts are 1.5 and 2.3 dB respectively.

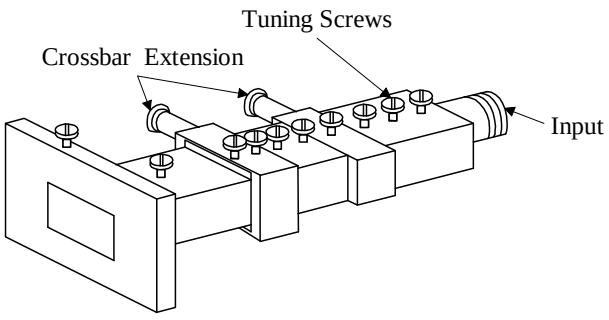


Figure 4.6: 1.9-7.6 GHz Frequency Multiplier consisting of two Doublers in cascade [26]

A telemetry diplexer with a pair of foreshortened 3-section filters with 0.01 dB passband

ripple was designed by Mok [27], and is shown in Fig. 4.7.

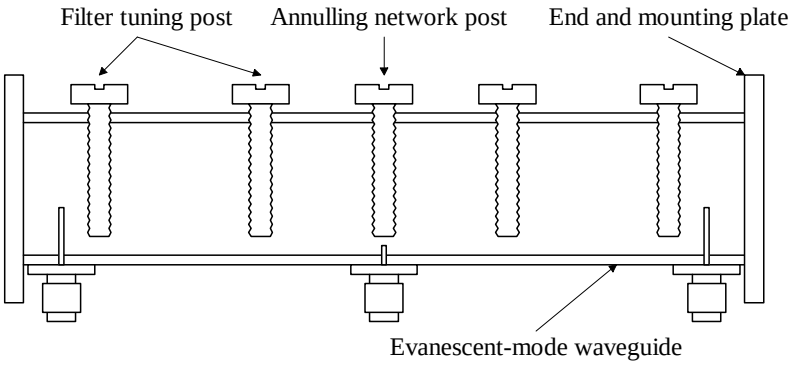


Figure 4.7: S-band telemetry diplexer [27]

The circuit, constructed in X-band waveguide, operates at 2290 and 2300 MHz and has a midband loss of 1.37 dB and a VSWR in the region of 1.25. As conventional diplexers consist of two filters connected to a common port, a fundamental problem in diplexer design is the matching of the two filters into this port [27]. A coaxial termination at the common port permits the construction of the diplexer in a single waveguide body, eliminating the need for conventional T-junctions and connecting flanges, thereby providing weight and bulk reductions. Foreshortened filters (filters with the first element removed) are used in the design and annulling networks at the common port are used to tune out the residual susceptance at each center frequency.

The absence of periodic resonances in evanescent devices can be very useful in up-converters [22]. The design of Kwiatkowski, Arthanayake and Knight [28] introduces a pump frequency of magnitude 2 W, via a propagating guide with included three-resonator filter. A six-resonator output filter combines with the pump frequency filter to produce reactive terminations, thereby eliminating additional resonances. The equivalent circuit of the up-converter is shown in Fig. 4.8, and achieves an output power of 1.1 W and total loss of 2.6 dB between pump and output port.

D'Ambrosio [29] presents an evanescent mode parametric amplifier with circulator and isolator circuits also implemented in below-cutoff guide. Gain of 13 dB over a 300 MHz bandwidth is achieved with a noise figure not exceeding 3.3 dB in the frequency band 14 to 14.3 GHz.

The brief description of published evanescent mode systems and subsystems shows that a range of evanescent mode equivalents exist for their propagating counterparts, offering occasional solutions to problems experienced in the implementation of propagating devices.

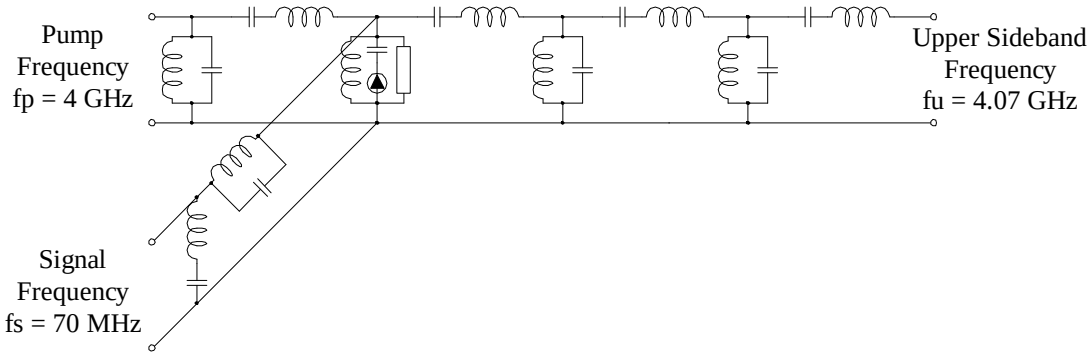


Figure 4.8: Up-converter Equivalent Circuit [28]

4.3 Evanescent Guide Filters

4.3.1 Basic Filter Topology

The switch proposed here, embeds the PIN diodes in an evanescent mode filter structure. The design of these filters is somewhat different than that of normal waveguide filters, and is based on equivalent lumped element models. The principal assumption when working in evanescent guide, as laid out by Craven and Mok [3] is that the only mode existing in the guide is an evanescent TE_{10} mode. This premise allows the use of a simple transmission line equivalent circuit to represent a section of below-cutoff guide, with characteristic impedance $Z_0 = jX_0 + R$.

Considering the lossless case where $R = 0$, Z_0 becomes $Z_0 = jX_0$, where

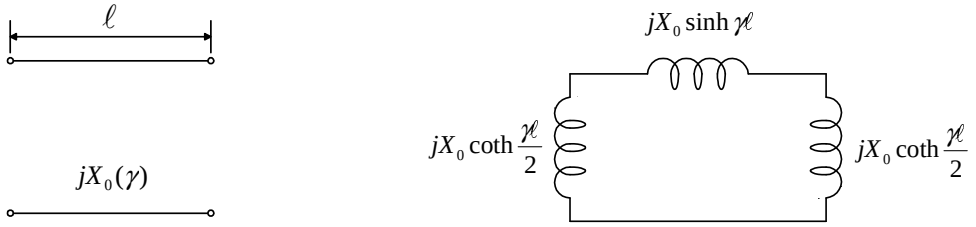
$$X_0 = \frac{\eta b}{a\sqrt{\left(\frac{\lambda}{\lambda_c}\right)^2 - 1}}. \tag{4.1}$$

The propagation constant γ is given by

$$\gamma = \frac{2\pi}{\lambda}\sqrt{\left(\frac{\lambda}{\lambda_c}\right)^2 - 1} \tag{4.2}$$

where λ is the free-space wavelength, λ_c the cutoff wavelength, $\eta = \sqrt{\mu/\epsilon}$ the intrinsic impedance of the material filling the waveguide, a the wide dimension of the waveguide and b the narrow dimension of the waveguide. The basic transmission line and its equivalent π section is shown in Fig. 4.9.

By introducing suitable capacitive obstacles at correct intervals along the evanescent mode waveguide, as shown in Fig. 4.10, a microwave analogue of a lumped inductance bandpass



(a) Basic Transmission Line Circuit (b) Equivalent π Section

Figure 4.9: Model of Evanescent Mode Waveguide [3]

filter with series inductance coupling results, as shown in Fig. 4.11. In this structure, the inductive coupling is controlled by the separation between capacitive obstacles.

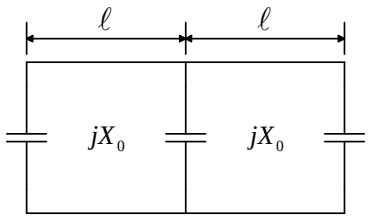


Figure 4.10: Suitable Capacitive Obstacles along the Evanescent Waveguide

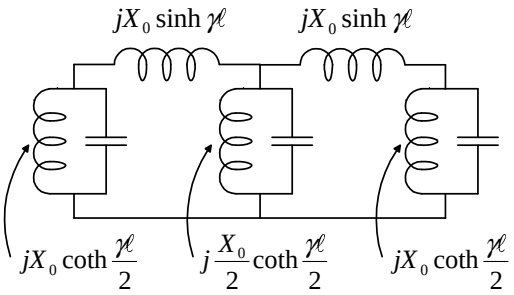


Figure 4.11: Lumped Equivalent Circuit of Evanescent Mode Waveguide Filter

The simple lumped inductance modelling of below-cutoff waveguide is possible since the propagation constant γ is real over the working frequency range, between zero frequency and cutoff frequency [3]. Taking $\coth \gamma\ell/2$ as a constant in the lumped inductance model creates the resonator inductance pole at cutoff frequency instead of at infinite frequency, as is the case with a lumped inductance. Thus, the slope of the reactance-frequency characteristic of the evanescent mode "inductance" will be steeper than that of a corresponding lumped inductance [3]. A bandwidth correction factor, Δ_{CM} in Eq. 4.3, is derived in [3] to account for this deviation, allowing the circuit to be treated as if it was a lumped element circuit.

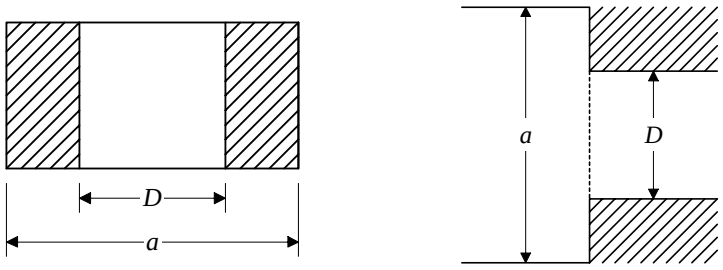
$$\Delta_{CM} = \frac{2}{1 + \frac{1}{1-(\lambda_c/\lambda_0)^2}} \tag{4.3}$$

Practical evanescent mode structures predominantly employ conventional waveguide obstacles to realize suitable capacitive elements. However, the equivalent circuit of an obstacle in cutoff waveguide is not necessarily the same as the one that applies in the propagating region [3], as discussed in Sec. 4.3.3. For most practical filters, Craven and Mok suggest an ordinary machine screw to represent the simplest and most practical obstacle, as screws of moderate radius (r/a = 0.1) in rectangular guide behave like virtually pure capacitances. It is further suggested by Craven and Mok that copper or silver plating is used for low-loss applications, and that the screw threads should be turned off in narrow-band filters, except near the head where the screw is tightened to the guide.

4.3.2 Junction Susceptance

Filter structures may be designed to begin with a shunt or series resonator, depending on the type of load into which the filter terminates. Filters beginning with series resonators are suitable for connection to a wide variety of loads including the impedance presented by propagating guide [3]. Since the cutoff guide is of smaller cross section than the propagating guide, a susceptance at the junction is formed, which may be tuned out to form a relatively broadband resonator [30].

To determine this junction susceptance, an input region in the form of a waveguide supporting only a single propagating mode, and an output region that is below cutoff is considered. More specifically, the case where a symmetrical change in cross section occurs, known as an H-plane step, is considered. The two rectangular guides therefore have equal heights but unequal widths, as shown in Fig. 4.12. The input equivalent circuit of



(a) Cross Sectional View (b) Top View

Figure 4.12: Change in Cross Section, H-Plane Step [31]

such a junction, according to Lewin [32], comprises a junction susceptance, transformer and evanescent guide load admittance, as shown in Fig. 4.13, with the input admittance Y in Eq. 4.4 defined at the plane of cross-sectional change.

$$Y = \frac{1}{Z} = \frac{1}{Z_J} + \frac{n_H^2}{Z_K}. \tag{4.4}$$

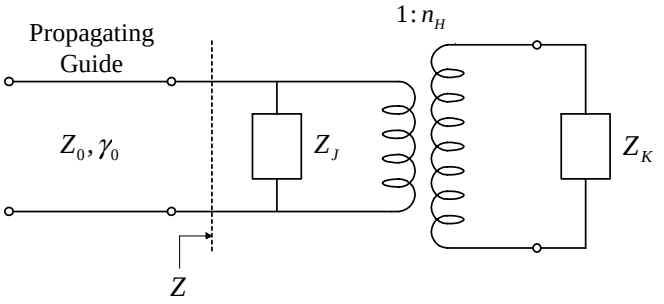


Figure 4.13: Complete Junction Model (Reference plane at change of cross-section)

The junction susceptance and transformer turns ratio can be determined by using two measurements and solving two equations for two unknowns. In Eq. 4.4, Z may be determined from the measured S_{11} value while Z_K is the known input impedance of the waveguide below cutoff, leaving n_H and Z_J as the two unknowns. S_{11} is measured for two situations, firstly, with an infinitely long below-cutoff waveguide shown in Fig. 4.14 with its equivalent circuit model, and secondly, with a short-circuited below-cutoff waveguide

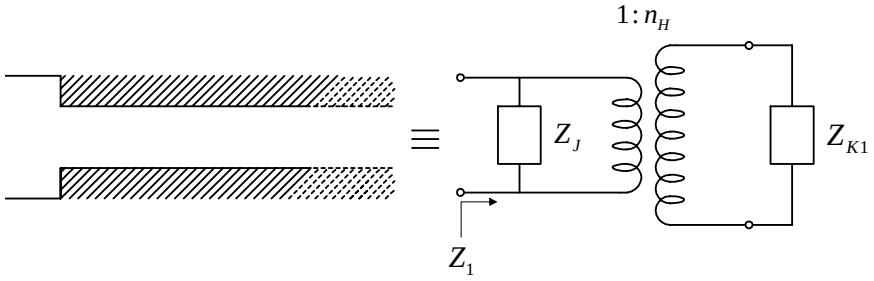


Figure 4.14: Infinite Length Evanescent Guide and Equivalent Circuit Model

of finite length ℓ, as shown in Fig. 4.15.

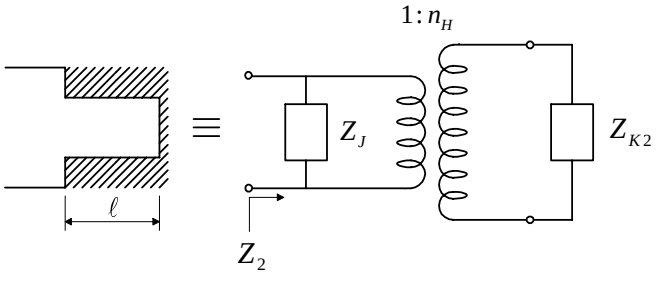


Figure 4.15: Finite Length Evanescent Guide and Equivalent Circuit Model

The infinitely long evanescent mode waveguide in Fig. 4.14 produces $Z_{K1} = jX_0$, since $jX_0 \sinh \gamma\ell \to \infty$, where X_0 is the characteristic impedance of the below-cutoff guide, calculated with Eq. 4.1. In the case where a finite length evanescent mode guide is used in Fig. 4.15, $Z_{K2} = jX_0 \coth \gamma\ell/2 \parallel jX_0 \sinh \gamma\ell$. From these two measurements, n_H and

Z_J can be calculated. The results can be verified for a limited range of geometric values by comparing them with the classical Marcuvitz model, which gives a value for Z_1 as in Eq. 4.5. Marcuvitz [31, p.168] states that at a junction between propagating guide and infinitely long evanescent mode waveguide,

$$\frac{Z_1}{jZ_0} = \frac{X}{Z_0} = \frac{2a}{\lambda_g} \frac{\mathrm{X}_{11}\left\{1 - \left[1 - \left(\frac{2D}{\lambda}\right)^2\right] X_0^2\right\}}{1 - \left[1 - \left(\frac{2D}{\lambda}\right)^2\right] X_0 \mathrm{X}_{22} + \sqrt{1 - \left(\frac{2D}{\lambda}\right)^2}(\mathrm{X}_{22} - \mathrm{X}_0)}, \tag{4.5}$$

with the restriction that the equivalent circuit is applicable in the range $\lambda > 2D$, provided $0.5 < \mathrm{a}/\lambda < 1.5$.

As an example, a reduced-height X-band (a = 22.86 mm, b = 4.3 mm) to K-band (a = 10.7 mm, b = 4.3 mm) transition is analysed using CST Microwave Studio to determine the model by using two equations and two unknowns, and compared to the Marcuvitz model in Fig. 4.16.

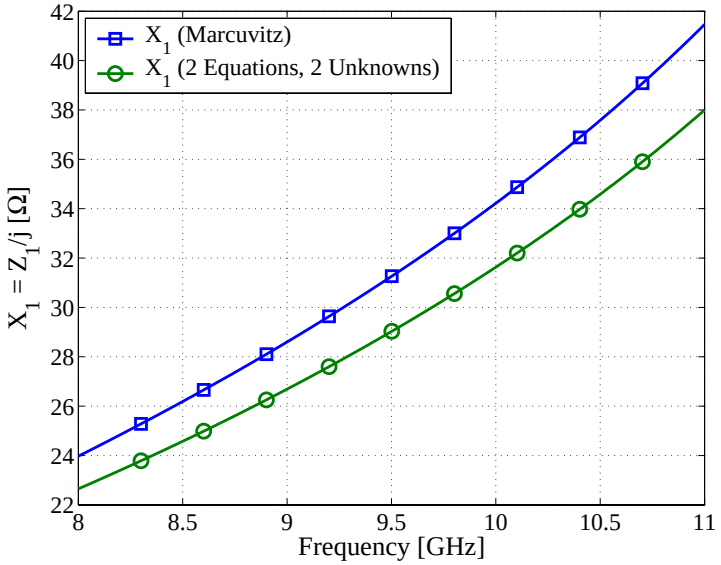


Figure 4.16: Load Impedance Comparison, X-band (a = 22.86 mm, b = 4.3 mm) to K-band (a = 10.7 mm, b = 4.3 mm)

In Fig. 4.17, the transformer turns ratio, n_H, is compared to the predicted value of Lewin [32] obtained by Eq. 4.6.

$$n_H = \sqrt{\frac{a}{D}} \cdot \frac{1 - \left(\frac{D}{a}\right)^2}{\frac{4}{\pi}\cos\frac{\pi D}{2a}}; \tag{4.6}$$

Substitution of n_H into Eq. 4.4, allows the junction impedance and corresponding inductance to be calculated. Values obtained for junction inductance and transformer turns

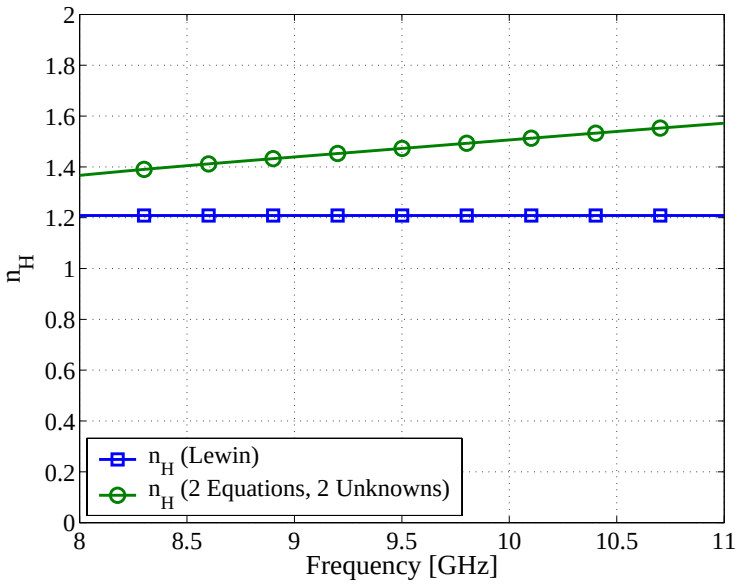
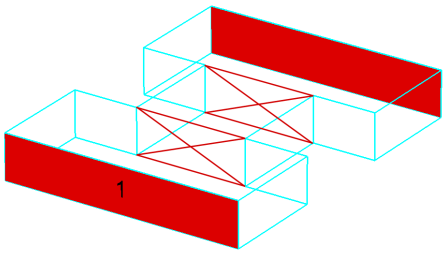
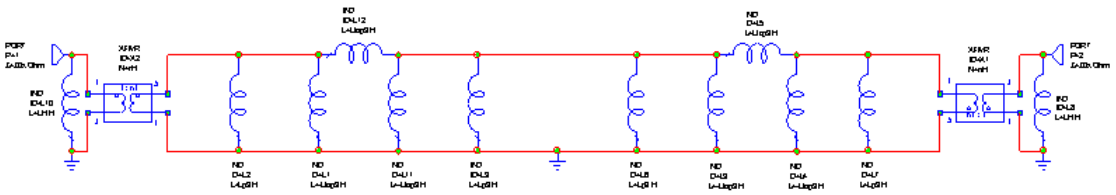


Figure 4.17: Transformer Turns Ratio Comparison, X-band (a = 22.86 mm, b = 4.3 mm) to K-band (a = 10.7 mm, b = 4.3 mm)

ratio using two equations and two unknowns, are simulated in an AWR Microwave Office model and compared to a CST Microwave Studio simulation with corresponding propagating and evanescent mode guide dimensions, as shown in Fig. 4.18. Results are compared in Fig. 4.19, showing excellent amplitude and phase agreement.



(a) CST Model



(b) AWR Model

Figure 4.18: Empty Guide Models (Dimensions in Appendix B)

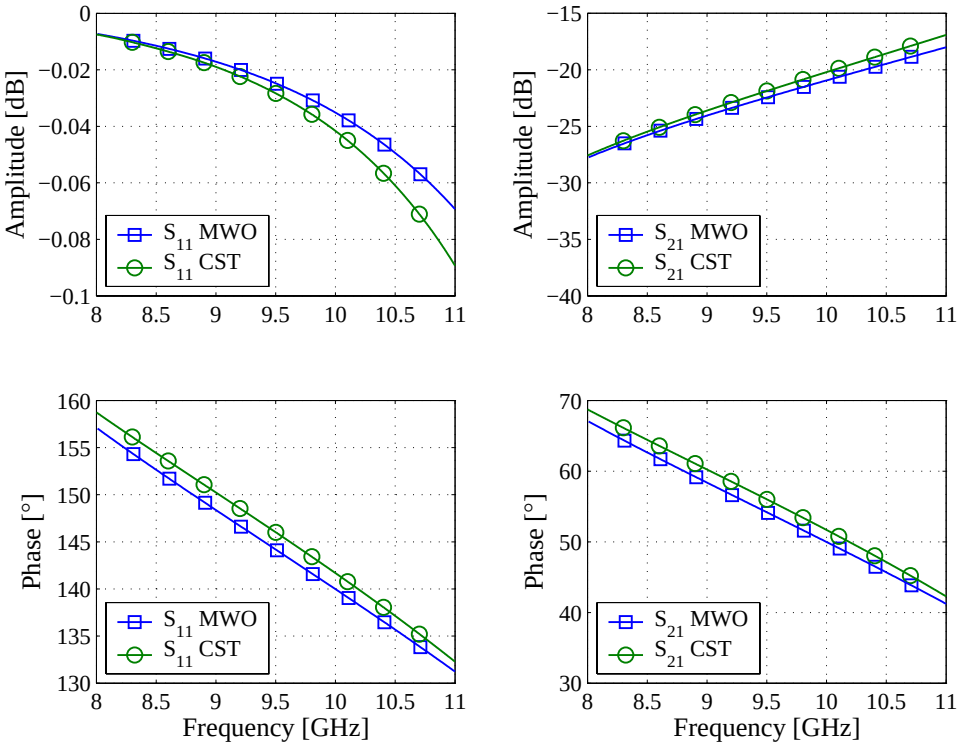


Figure 4.19: Empty Guide Comparison Results

4.3.3 Obstacles In Evanescent Guide

A crucial aspect of an evanescent mode waveguide design is the determination of the equivalent circuit of obstacles used in the cutoff guide. Mok [20] describes a practical measurement technique to obtain obstacle admittance from input reflection measurements alone. The obstacle to be measured is placed between two media, as shown in Fig. 4.20.

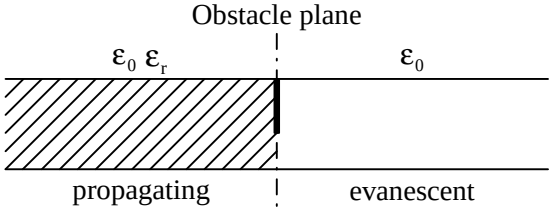


Figure 4.20: Obstacle Placement [20]

Because of the differences in reactive energy associated with any given obstacle in propagating and evanescent guide, such an obstacle can be represented by two different values of shunt susceptance, namely B_f for propagating guide and B_u for evanescent guide. For an object symmetrical about the plane between propagating guide and evanescent guide, the total energy is made up of the energy of half the object in filled guide and half the object in empty guide. The total susceptance, B, is therefore equal to the sum of half the

susceptance when the guide is completely filled, B_f, and half the susceptance when the guide is completely empty, B_u,

$$B = \frac{1}{2}B_f + \frac{1}{2}B_u. \tag{4.7}$$

The relative permittivity, ϵ_r, is chosen in such a way that the filled guide supports the TE_{10} mode, while the unfilled guide does not. The method is only valid for thin obstacles, since thicker obstacles should be represented by a T- or a π-network [20].

Two input admittance measurements are made, as shown in Fig. 4.21. The first measurement is completed with a short-circuited propagating guide of suitable length behind the obstacle, which is replaced by a long evanescent guide in the second measurement [20]. The input admittances are described as

$$\begin{aligned} Y_{i1} &= jB_f + Y_{sc} \qquad \text{and} & (4.8)\\ Y_{i2} &= \frac{j}{2}\left(B_f + B_u\right) + Y_e & (4.9) \end{aligned}$$

yielding

$$\begin{aligned} jB_f &= Y_{i1} - Y_{sc} \qquad \text{and} & (4.10)\\ jB_u &= 2\left(Y_{i2} - Y_e\right) - \left(Y_{i1} - Y_{sc}\right), & (4.11) \end{aligned}$$

where Y_{sc} is the admittance of the short-circuited propagating (filled) guide and Y_e is the characteristic admittance of the evanescent (unfilled) guide. The admittance of the obstacle in the guide below cutoff is therefore obtained from the two measured values Y_{i1} and Y_{i2}, together with the known quantities Y_{sc} and Y_e [20].

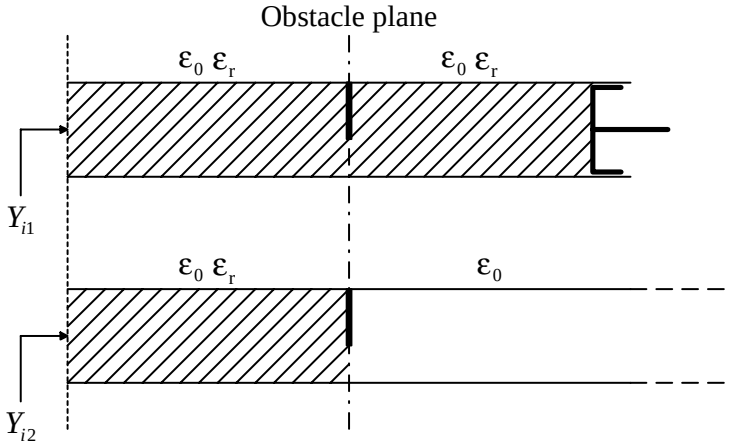
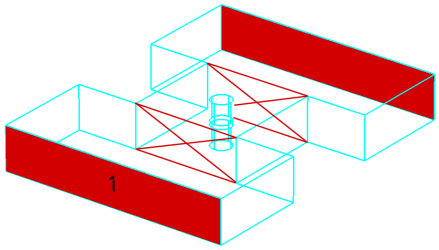


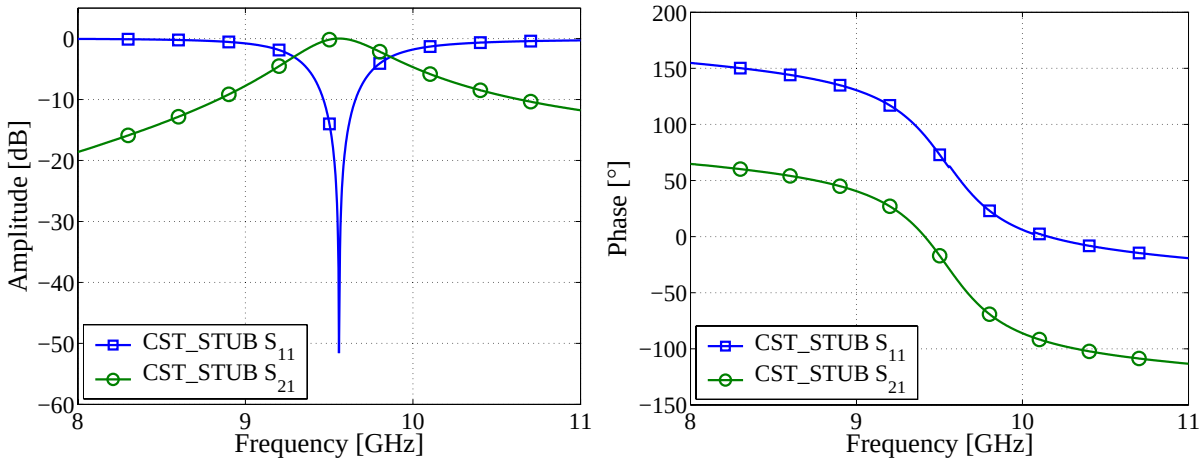
Figure 4.21: Measurement Technique for Mok's Method [20]

To demonstrate the technique, the susceptance of two central stubs a with central gap, as shown in Fig. 4.22(a), is calculated. This is a similar structure to the one used as diode

mount in the proposed switch. S-parameter results are shown in Fig. 4.22(b).



(a) CST_STUB Model

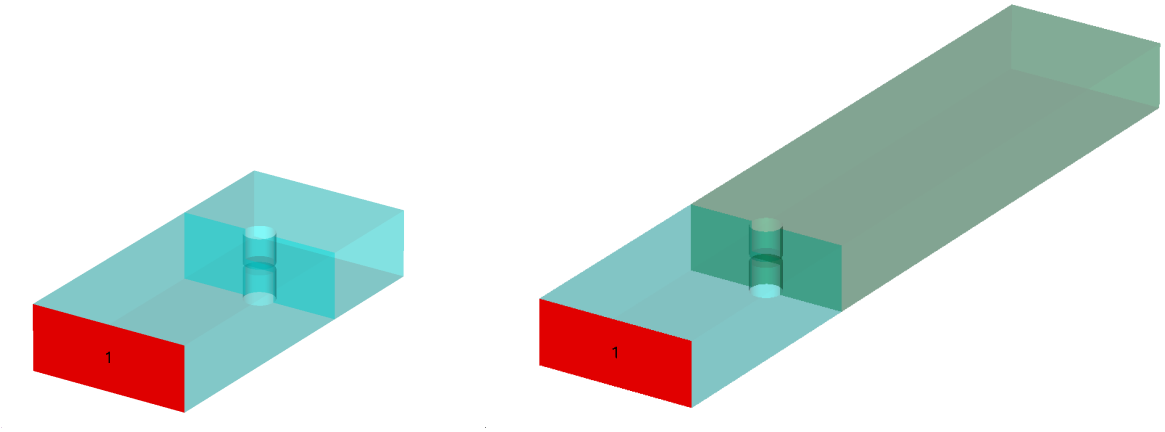


(b) CST Results

Figure 4.22: CST Stub Filter (Dimensions in Appendix B)

The two measurement setups proposed by Mok are shown in Fig. 4.23. Guide dimensions are chosen equal to evanescent mode guide dimensions of Fig. 4.22(a) where a = 10.7 mm and b = 4.3 mm, namely K-band with cutoff frequency $f_C = 14.047$ GHz. The calculated and implemented relative permittivity of the filled sections is $\epsilon_r = 4.56$, to obtain the cutoff frequency of X-band, $f_C = 6.557$ GHz, for the propagating guide. S-parameter measurements are converted and analysed in Matlab, obtaining values for obstacle susceptance in filled guide (B_f), obstacle susceptance in unfilled guide (B_u) and total obstacle susceptance (B). Results are shown in Fig. 4.24.

To prove the accuracy of the results, the admittance of the obstacle in unfilled guide (jB_u) is inserted into the AWR Microwave Office model, determined from Sec. 4.3.2, as shown in Fig. 4.25. The result is compared to the original stub filter in Fig. 4.26 and shows good agreement. Note that due to the sensitive nature of the technique, a slight (<1%) adaption of the relative permittivity used for the calculations in Matlab was introduced, to obtain a better center frequency fit of the CST Microwave Studio and AWR Microwave Office models.



(a) Y_{i1} Measurement (b) Y_{i2} Measurement

Figure 4.23: Input Admittance Measurements (Dimensions in Appendix B)

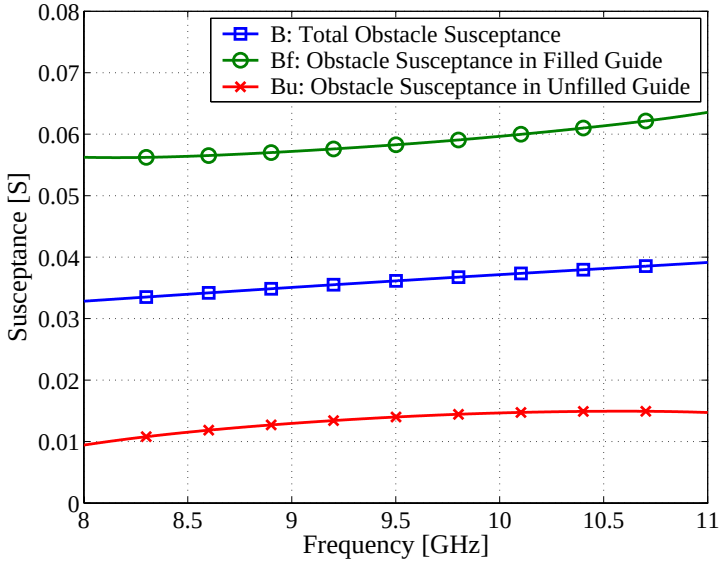


Figure 4.24: Stub Capacitance

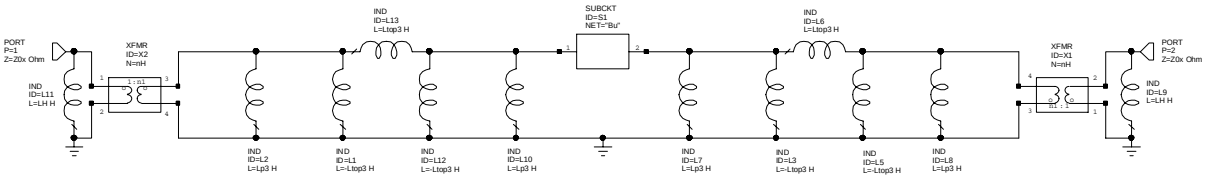


Figure 4.25: B_u Inserted in AWR Model

The main drawback of Mok's technique is the requirement that the obstacle should ideally exist only at the reference plane, and be symmetric with respect to this plane. A more robust technique, based on parameter extraction principles, is used for the determination of the PIN diode model. In this technique, an EM analysis is performed on an obstacle in evanescent guide, terminated on both ends by propagating guide. A linear circuit

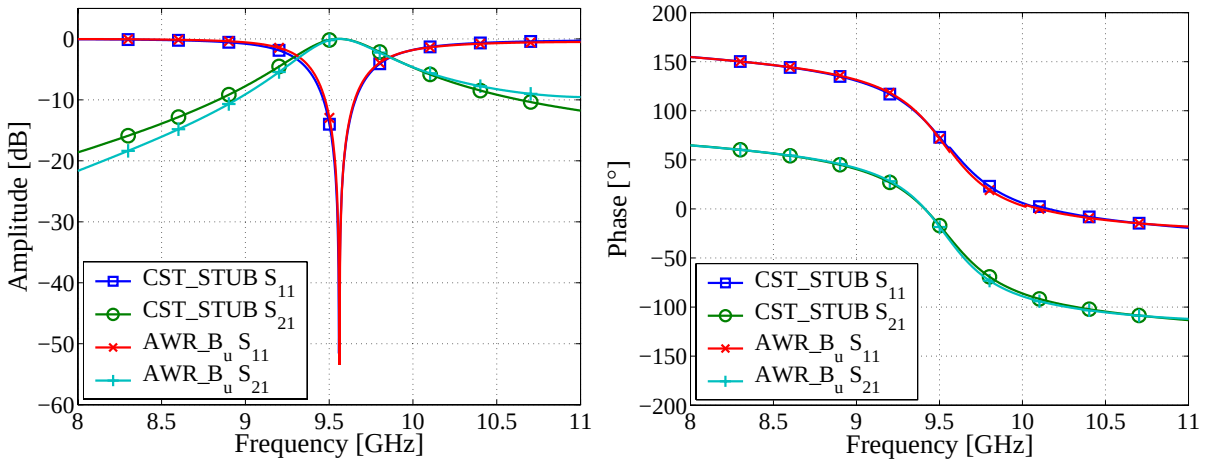


Figure 4.26: CST_STUB Filter vs. AWR_B_u Filter

model, incorporating the evanescent guide model and junction susceptance of the previous sections, together with a single variable shunt reactance at the reference plane, is then fitted to the EM analysis by optimizing the variable shunt susceptance. This procedure is discussed in more detail in Chapter 6.

4.4 Conclusion

Following an overview of evanescent mode devices, the fundamental design principles allow successful implementation of basic evanescent mode filters employing central and junction capacitive stubs. A linear first order filter circuit with junction susceptance, transformer turns ratio and evanescent mode obstacle admittance at the reference plane, is compared to an EM implementation of the filter, showing good agreement. Chapter 5 reviews filter basics to design a first order evanescent mode filter with measurements of the filter tuned to various frequencies.

Chapter 5

Evanescent Mode Filter Design

5.1 Introduction

Following the development of diode and evanescent guide models of the previous chapters, the final theory needed for the design of an evanescent mode switch, is the synthesis procedure of evanescent mode filters. As an illustration, a first order evanescent mode filter prototype is designed from first principles. The filter is implemented in electromagnetic simulation packages CST Microwave Studio Version 3 and ANSYS Version 7.1 respectively, as well as linear-solver packages Matlab Version 6.5 and AWR Microwave Office Version 6.01i. Confirmation of the electromagnetic model in CST Microwave Studio and the lumped-element model in AWR Microwave Office of a section of empty evanescent guide is achieved in Sec. 4.3.2 by comparing the simulated data against measured results of a corresponding physical structure. The filter is measured at various centre frequencies by adjusting the central capacitance, through variation of the gap distance between stubs. Simulations in all solver packages agree well with measurements.

5.2 Chebyshev Bandpass Filter Using J-Inverters

5.2.1 J-Inverter Basics

Starting with a lumped element ladder LC filter, a prototype containing only inductances or only capacitances may be achieved with the aid of idealized inverters. *Impedance* and *Admittance* inverters operate like a quarter-wavelength line of characteristic impedance/admittance K or J respectively at all frequencies, and are simply referred to as K-inverters and J-

inverters. The admittance Y_a seen through a J-inverter with load admittance Y_b is

$$Y_a = \frac{J^2}{Y_b} \tag{5.1}$$

as depicted in Fig. 5.1.

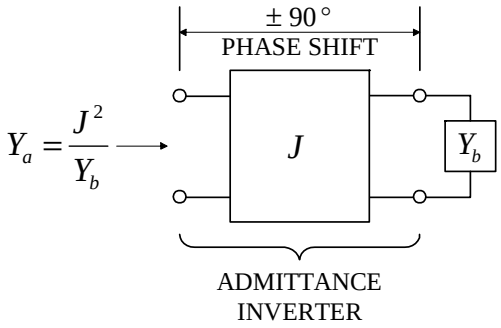


Figure 5.1: Definition of Admittance Inverter [33]

An inverter may have a phase shift of $\pm 90^o$ or an odd multiple thereof [33]. The inverting action causes a series inductance flanked by inverters to look like a shunt capacitance, and a shunt capacitance flanked by inverters to look like a series inductance. The concept of duality is employed to derive equations for the K-inverters, since a given circuit as seen through an inverter looks like the dual of that given circuit [33] with an admittance scale factor.

Fig. 5.2(a) shows a portion of a lowpass prototype circuit, open-circuited just beyond inductance L_{k+1}. The dual circuit is shown in Fig. 5.2(b) where the open circuit has become a short circuit. The corresponding circuit using J-inverters is shown in Fig. 5.2(c). The open and short circuits are introduced to simplify the equations. In Fig. 5.2(a),

$$Y_k = j\omega C_k + \frac{1}{j\omega L_{k+1}}, \tag{5.2}$$

while in Fig. 5.2(c),

$$Y'_k = j\omega C_{ak} + \frac{J^2_{k,k+1}}{j\omega C_{ak+1}}. \tag{5.3}$$

Y_k must be identical to Y'_k except for an admittance scale factor C_{ak}/C_k, which means

$$Y'_k = \frac{C_{ak}}{C_k} Y_k = j\omega C_{ak} + \frac{C_{ak}}{C_k} \frac{1}{j\omega L_{k+1}}, \tag{5.4}$$

from Eq. 5.3. By moving the position of the open circuit, all the J-inverters except those at the ends may be calculated with the simplified expression

$$J_{k,k+1} = \sqrt{\frac{C_{ak} C_{ak+1}}{C_k L_{k+1}}}, \tag{5.5}$$

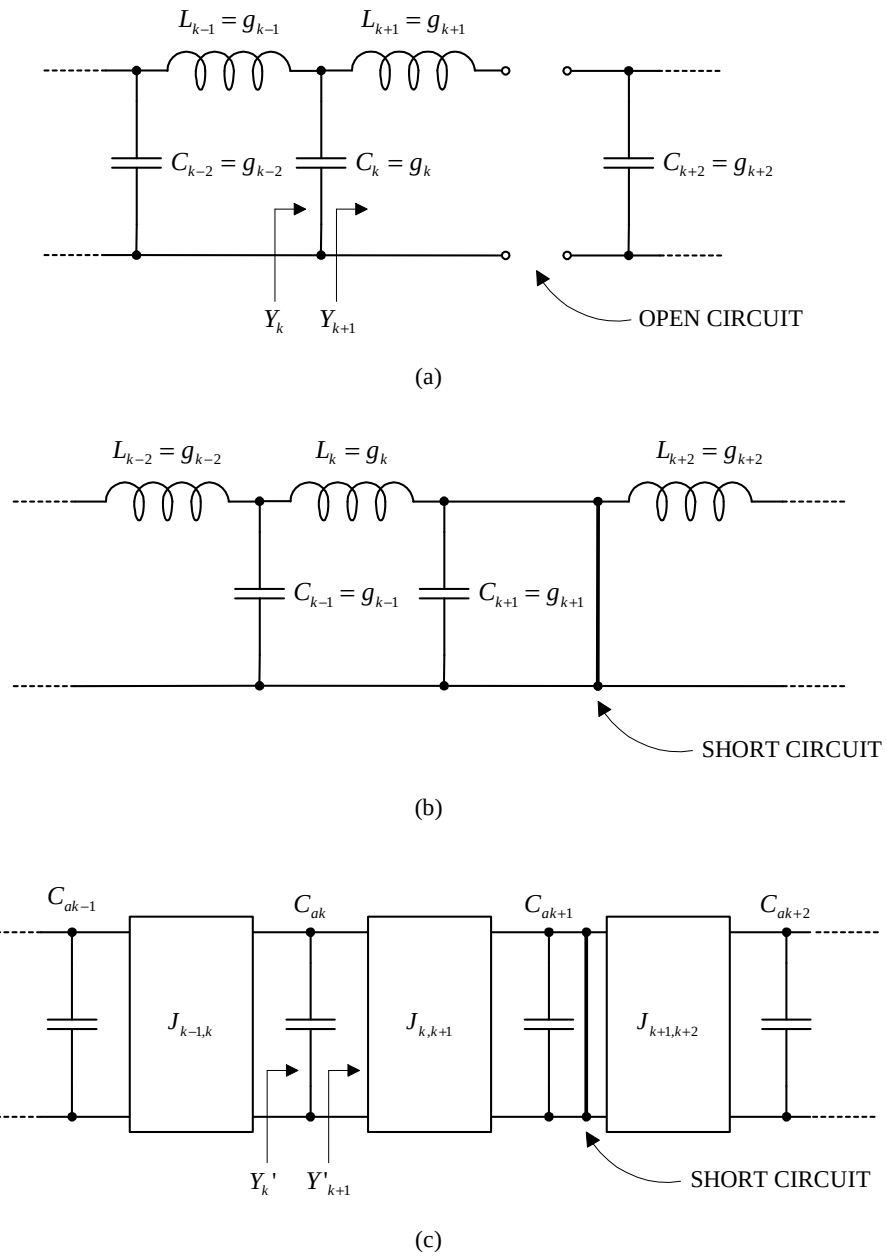


Figure 5.2: A ladder circuit is shown at (a), and its dual is shown at (b). The analogous J-inverter form of these two circuits is shown at (c). Adapted from [33].

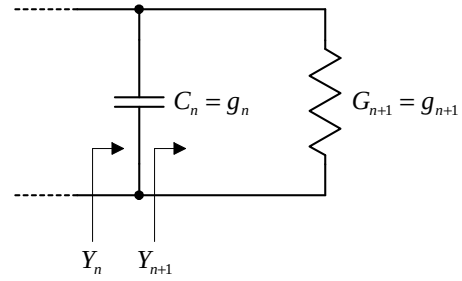
valid for k = 1,2,...,n-1, obtained by equating Eq. 5.3 and Eq. 5.4.
To calculate the J-inverters at the ends consider Fig. 5.3.

The lowpass prototype circuit expression

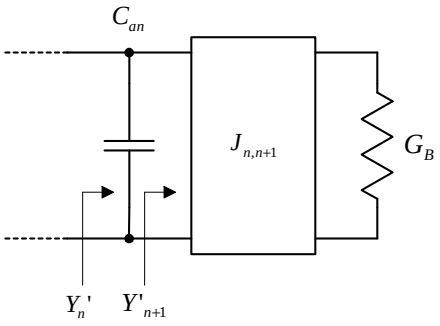
$$Y_n = j\omega C_n + \frac{1}{G_{n+1}} \tag{5.6}$$

is equal to the inverter circuit expression

$$Y_n' = j\omega C_{an} + \frac{J_{n,n+1}^2}{G_B}, \tag{5.7}$$



(a)



(b)

Figure 5.3: The end portion of a prototype circuit is shown at (a) while at (b) is shown the corresponding end portion of a circuit with J-inverters. Adapted from [33].

except for an admittance scale factor C_{an}/C_n. We therefore have

$$Y_n' = \frac{C_{an}}{C_n} Y_n = j\omega C_{an} + \frac{C_{an}}{C_n} \frac{1}{G_{n+1}} \tag{5.8}$$

from Eq. 5.6, leading to the generalized expression

$$J_{n,n+1} = \sqrt{\frac{C_{an} G_B}{C_n G_{n+1}}} \tag{5.9}$$

obtained by equating Eq. 5.7 and Eq. 5.8. A practical inverter using lumped inductances is shown in Fig. 5.4, where $B = \omega L$.

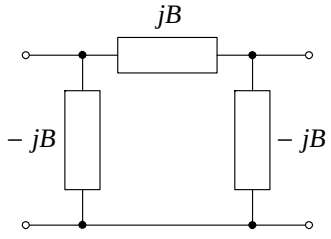


Figure 5.4: Admittance Inverter

As an example of the use of inverters, a basic third order filter lowpass prototype, shown in Fig. 5.5, is transformed to its J-inverter analogue, shown in Fig. 5.6.

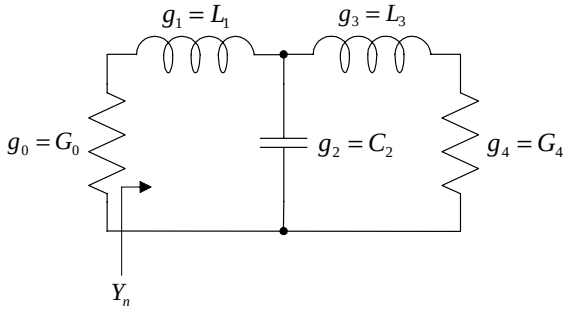


Figure 5.5: Basic Lowpass Prototype

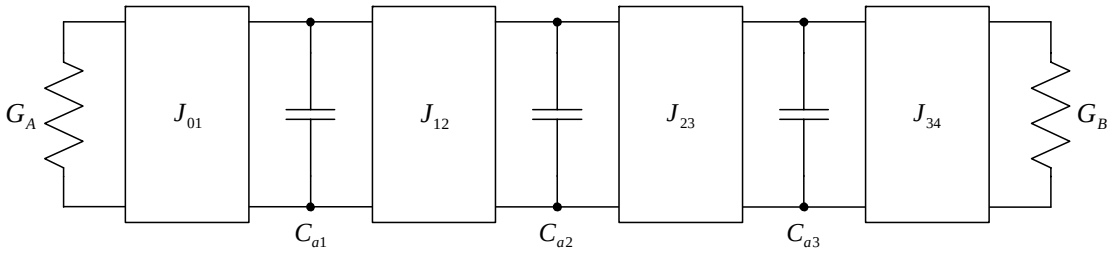


Figure 5.6: J-inverter Analogue of Basic Lowpass Prototype

Values obtained for the admittance inverters are

$$\begin{aligned} J_{01} &= \sqrt{\frac{G_A C_{a1}}{g_0 g_1}}, \\ J_{12} &= \sqrt{\frac{C_{a2}}{L_2'}} = \sqrt{\frac{C_{a1}C_{a2}}{g_1 g_2}}, \\ J_{23} &= \sqrt{\frac{C_{a3}}{L_3'}} = \sqrt{\frac{C_{a2}C_{a3}}{g_2 g_3}} \qquad \text{and} \\ J_{34} &= \sqrt{\frac{G_B}{R_4'''}} = \sqrt{\frac{G_B C_{a3}}{g_3 g_4}}, \end{aligned}$$

as predicted by Eq. 5.9. To equate the coupled structure elements to the evanescent mode waveguide model presented by Craven and Mok [3], the structure in Fig. 5.6 is transformed to its bandpass equivalent and scaled for bandwidth, frequency and impedance, as shown in Fig. 5.7, where Δ is the fractional bandwidth

$$\Delta = \frac{\omega_2 - \omega_1}{\omega_0}. \tag{5.10}$$

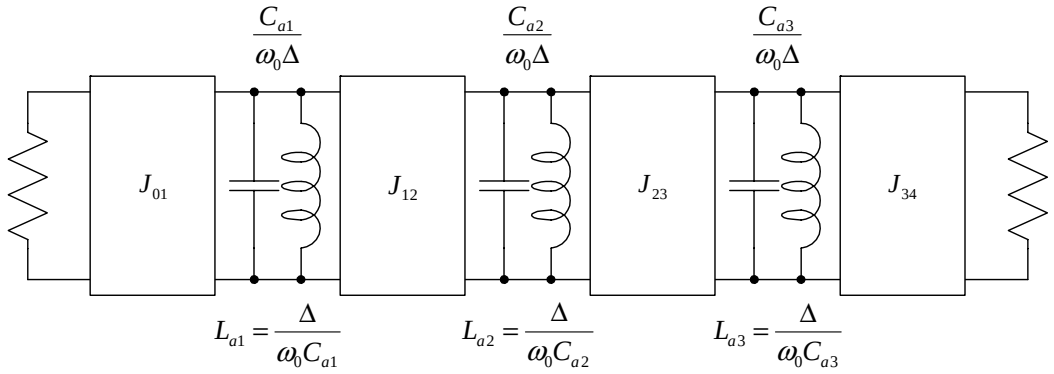


Figure 5.7: Bandpass Equivalent Circuit of Fig. 5.6

This approach is validated by considering Fig. 5.8 of Craven and Mok [3] and obtaining J-inverter expressions as presented in [3]. Correlating the shunt inductances of the circuits in Fig. 5.7 and Fig. 5.8, results in Eq. 5.11 to 5.13.

$$\frac{R}{\Delta_{CM}\omega_0 L_{e1}} = \frac{C_{a1}}{R_0\Delta} \tag{5.11}$$

$$\frac{1}{R\Delta_{CM}\omega_0 L_{e2}} = \frac{R_0 C_{a2}}{\Delta} \tag{5.12}$$

$$\frac{R}{\Delta_{CM}\omega_0 L_{e3}} = \frac{C_{a3}}{R_0\Delta} \tag{5.13}$$

Δ_{CM} takes into account the steeper reactance frequency characteristic of $\omega_0 L_{e1,2,3}$.

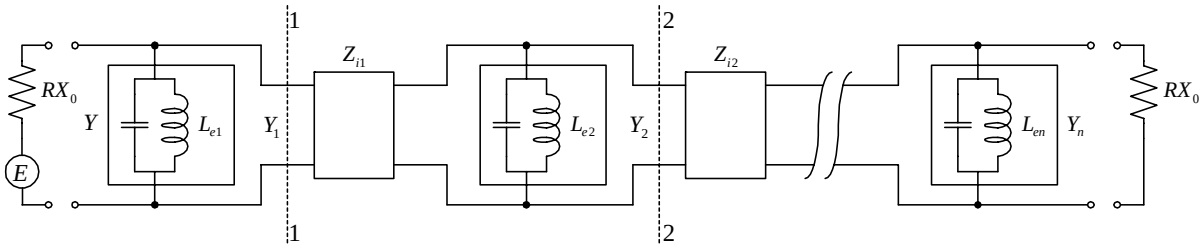


Figure 5.8: Simplified Filter with J-inverters [3]

Expansion of inverter J_{23} yields

$$\begin{aligned} J_{23} &= \sqrt{\frac{C_{a2}C_{a3}}{g_2 g_3}} \\ &= \sqrt{\frac{\Delta}{RR_0\omega_0\Delta_{CM}L_{e2}}\cdot\frac{RR_0\Delta}{\omega_0\Delta_{CM}L_{e3}}\cdot\frac{1}{g_2 g_3}} \\ &= \frac{\omega_2-\omega_1}{\Delta_{CM}\omega_0}\sqrt{\frac{1}{g_2 g_3 \omega_0 L_{e2}\omega_0 L_{e3}}} \end{aligned} \tag{5.14}$$

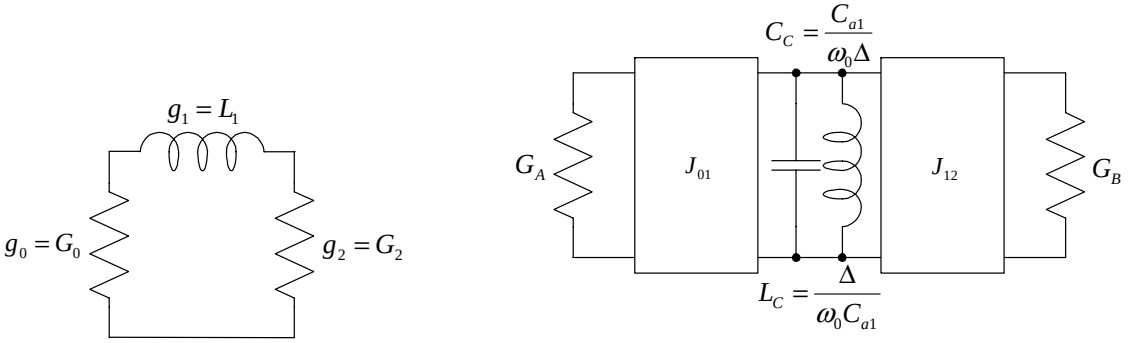
which is related to the general expression of Craven and Mok [3, p.299] by

$$J_{23} = \frac{1}{\sinh \gamma \ell_2}, \tag{5.15}$$

producing $\omega L = \sinh \gamma \ell_2$, as determined by Craven and Mok [3].

5.2.2 First Order Filter Design

A first order filter is designed as an initial step to determine the simulation accuracy of evanescent mode filters in various packages. An equal ripple lowpass filter prototype with 0.5 dB ripple ($g_0 = 1$, $g_1 = 0.6986$, $g_2 = 1$), shown in Fig. 5.9(a), forms the starting point of the design. The lowpass prototype is transformed to its coupled bandpass equivalent, as shown in Fig. 5.9(b). Capacitance C_{a1} is related to evanescent guide length ℓ by Eq. 5.15. At the resonance frequency, the reactance magnitude of C_C must be equal to the reactance magnitude of L_C, which in turn relates to the evanescent guide length by $\omega L_C = \frac{1}{2} X_0 \tanh \gamma \ell$.



(a) Lowpass Prototype (b) Coupled Bandpass Equivalent

Figure 5.9: First Order First Principles Design

As in the approach of Craven and Mok [3], where chosen central capacitance values relate to single lengths ℓ upon which central inductance and J-inverter values are dependent, the first principles approach requires simultaneous solving of equations Eq. 5.16 and Eq. 5.17.

$$J_{k,k+1}(C_{a1}) = \sqrt{\frac{G_A \cdot C_{a1}}{g_0 \cdot g_1}} = \frac{1}{X_0 \sinh \gamma \ell} \quad \text{and} \tag{5.16}$$

$$\omega L_C = \frac{\Delta}{C_{a1}} = \frac{1}{2} X_0 \tanh \gamma \ell. \tag{5.17}$$

A number of fixed specifications form the starting point of the design:

- Arbitrary bandwidth of 20 %, important only in subsequent higher order designs,

- Implementation in K-band guide (a = 10.7 mm, b = 4.3 mm),
- Centre frequency of 9.5 GHz, the centre of the specified filter band.

Simultaneous solving yields an evanescent guide length of $\ell = 5.4$ mm, on either side of the central capacitive obstacle, with a central capacitance C_C of 0.2 pF. Since the design requirements of the first order filter prototype are not that crucial, a first order prototype with length $\ell = 5$mm is manufactured, as shown in Fig. 5.10. Changes in bandwidth are observed as the centre frequency is shifted from the design specification. Measurements of the manufactured first order filter are shown in Sec. 5.3.

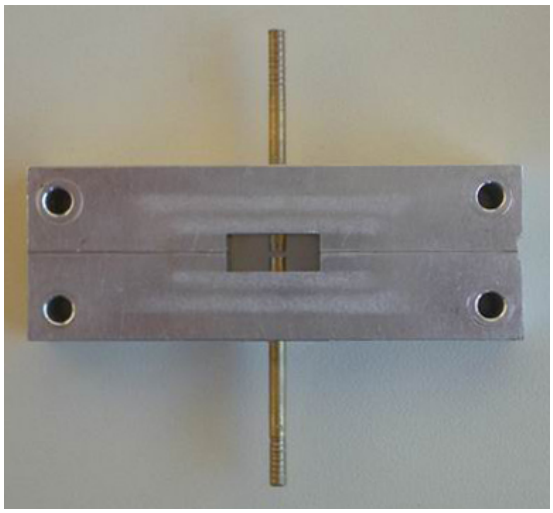


Figure 5.10: Evanescent Mode Section of First Order Filter Prototype (Dimensions in Appendix B)

5.3 Measurements

The manufactured filter is measured in a reduced-height X-band environment. The height standard X-band waveguide is stepped from normal height (10.16 mm) to the evanescent mode guide height (4.3 mm). This is followed by an H-Plane step between the propagating and evanescent mode sections. The manufactured X-band to reduced-height X-band steps and TRL calibration standards, including a zero-length Thru, Short Reflect and Line standard, are shown in Fig. 5.11.

As a first step in the verification process, the empty guide models of CST Microwave Studio and AWR Microwave Office in Sec. 4.3.2 are measured, with the results given in Fig. 5.12. Subsequently, a solid stub (2mm diameter) is entered as the central obstacle in

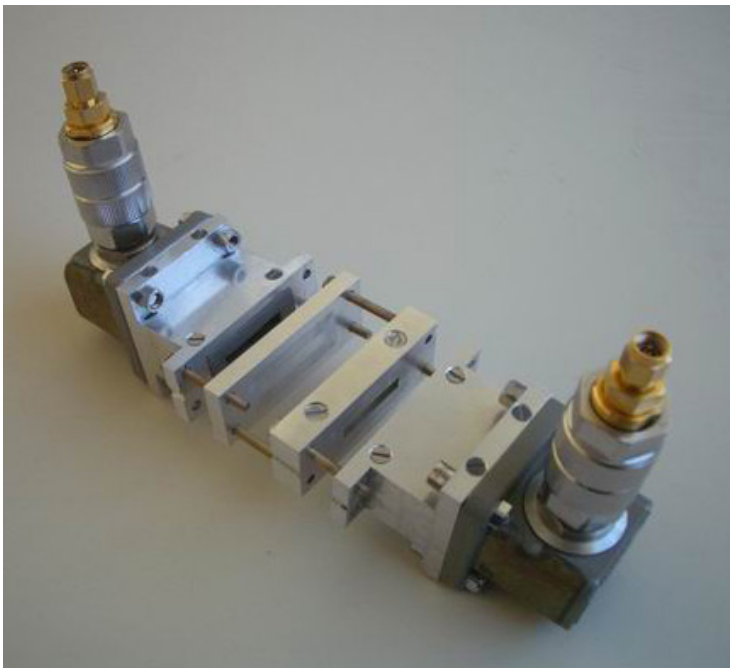


Figure 5.11: Transitions And TRL Standards

the filter of both physical and CST Microwave Studio model. Once again, good agreement is obtained between the measured data and simulation, as shown in Fig. 5.13.

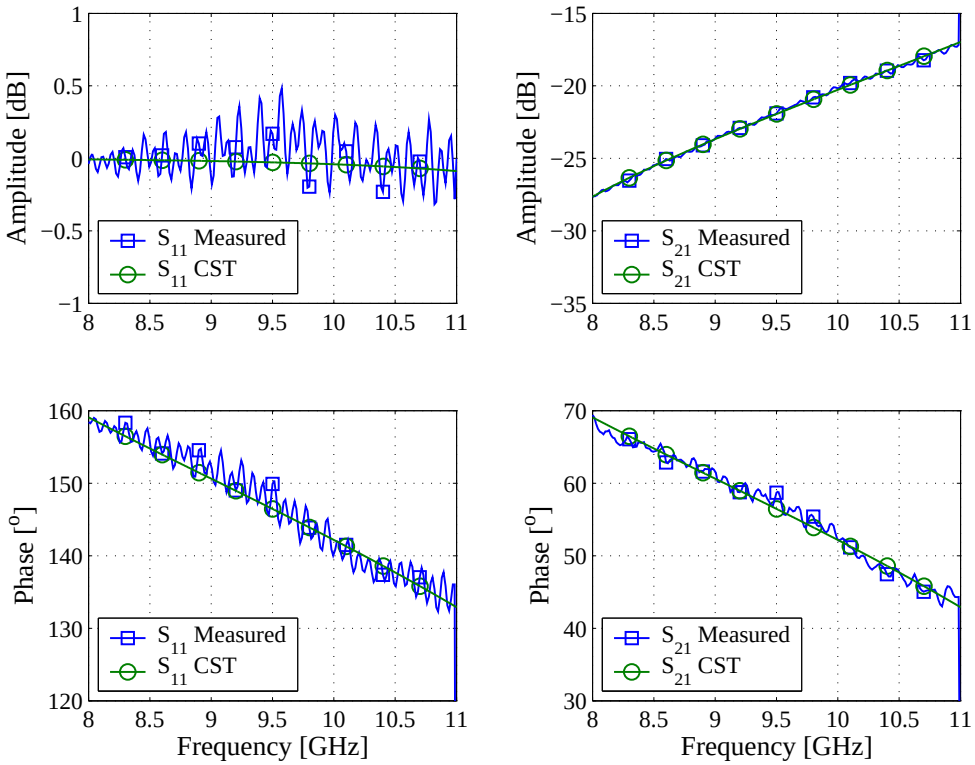


Figure 5.12: Non-Propagation Model: Measured (10 mm guide length) vs CST

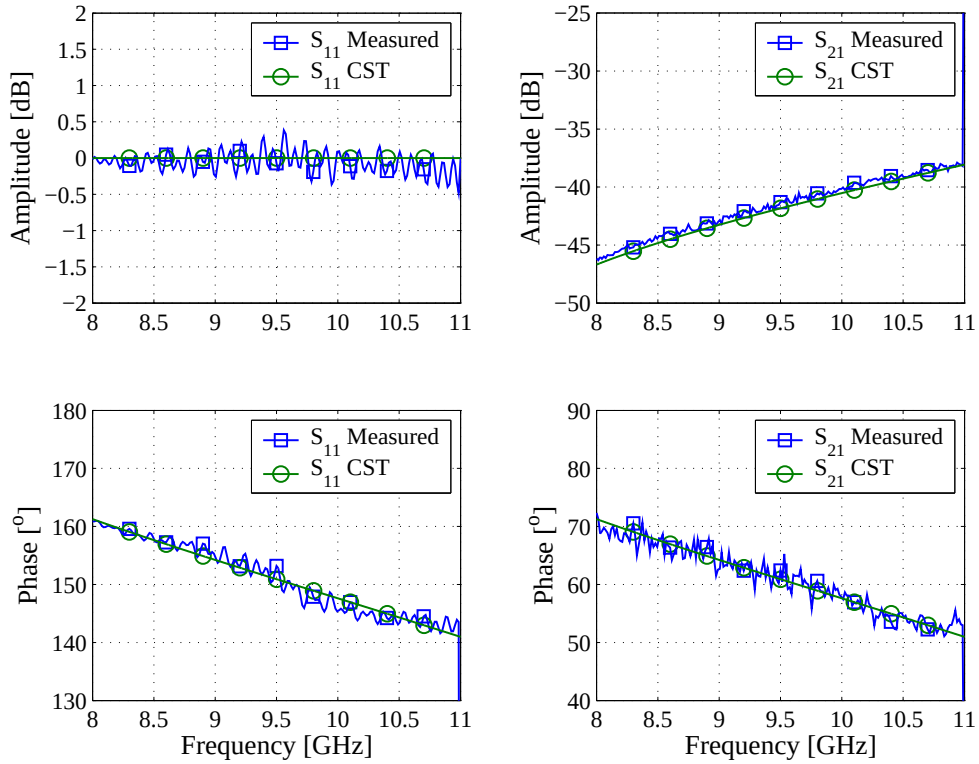
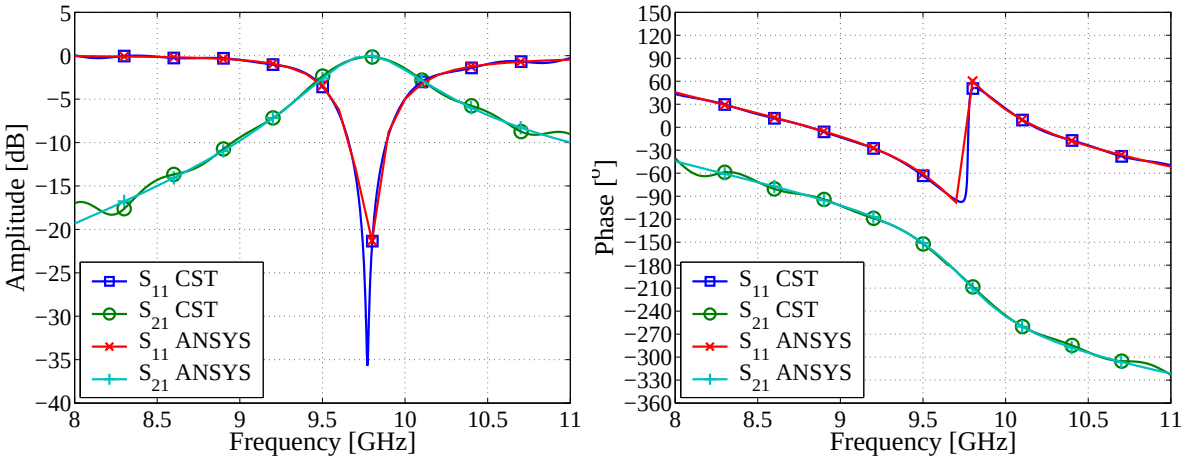


Figure 5.13: Solid-Stub Model: Measured vs CST with central Solid Stub

Next, various measured filters, as shown in Fig. B.4 of Appendix B, with different central gap distances, as indicated, are compared to CST Microwave Studio simulations. One of the filters simulated in CST Microwave Studio is verified in an ANSYS simulation as shown in Fig. 5.14. The centre frequency, roll-off characteristic of the amplitude response and phase data of the two simulations agree very well. For the remainder of the project, CST Microwave Studio is the EM solver of choice, due to its much improved simulation time and infinitely better user interface.



(a) Magnitude (b) Phase

Figure 5.14: CST vs ANSYS

After completing measurements of four filters with different stub gap heights, these gap heights are measured with a travelling microscope, simulated in CST Microwave Studio, and simulations compared with the measured filter responses. Comparisons are shown in Fig. 5.15, 5.16, 5.17 and 5.18, with centre frequency percentage errors between measured and simulated data of 1.60%, 1.98%, 4.25% and 0.82% respectively. These errors are due to imperfect stub manufacturing and alignment characteristics of the filter prototype, as well as the fact that μm-tuning accuracy is required for accurate frequency shifting.

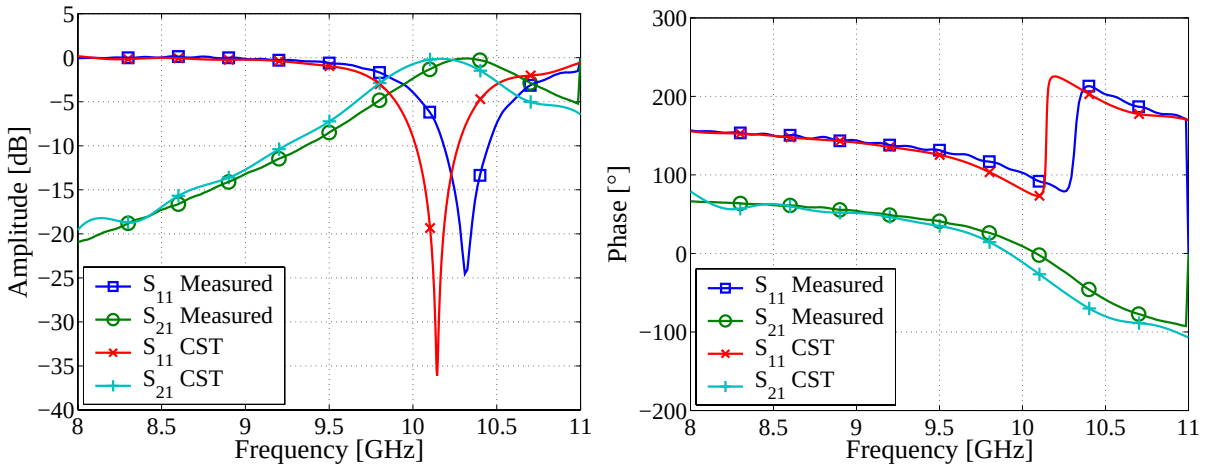


Figure 5.15: Measured Filter vs CST (0.43mm gap)

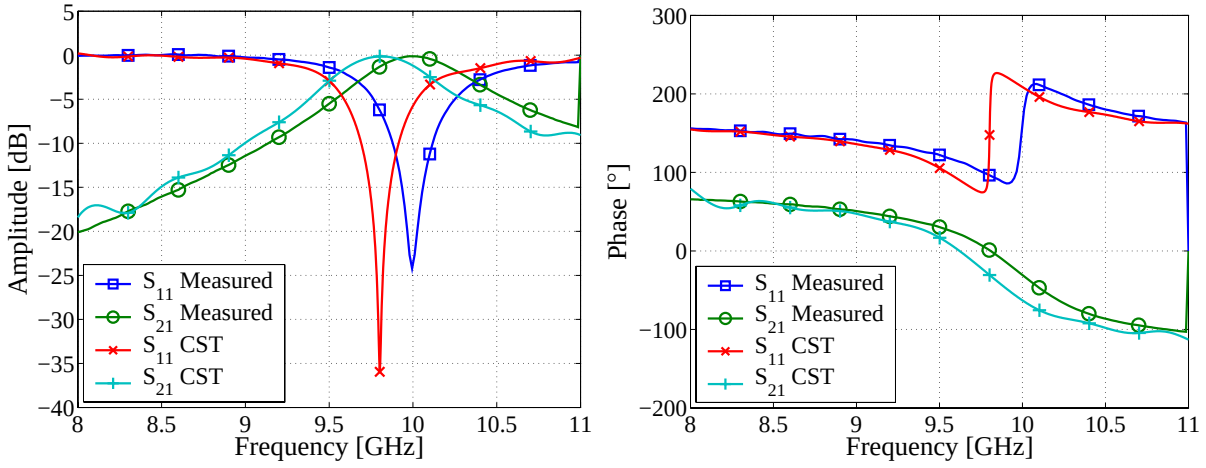


Figure 5.16: Measured Filter vs CST (0.38mm gap)

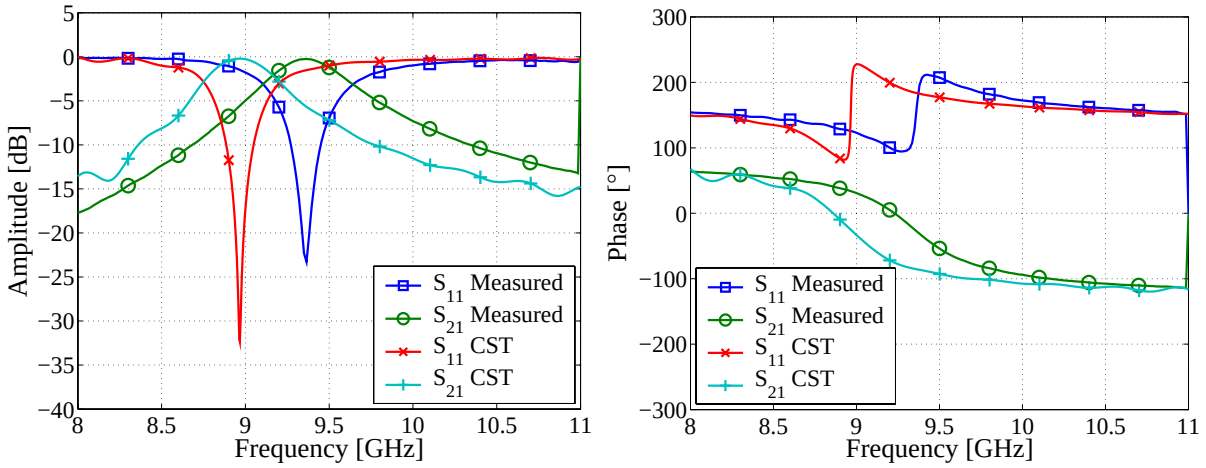


Figure 5.17: Measured Filter vs CST (0.29mm gap)

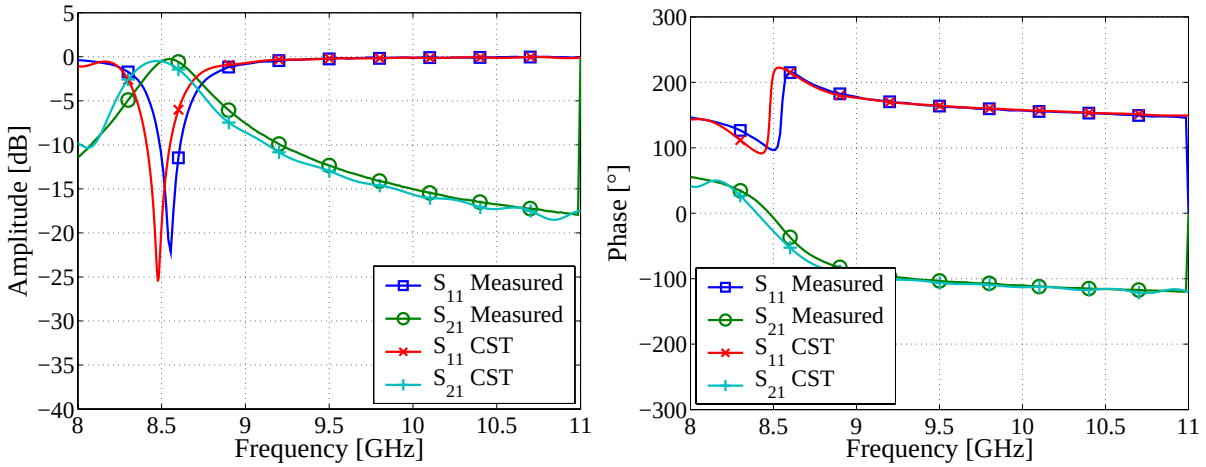
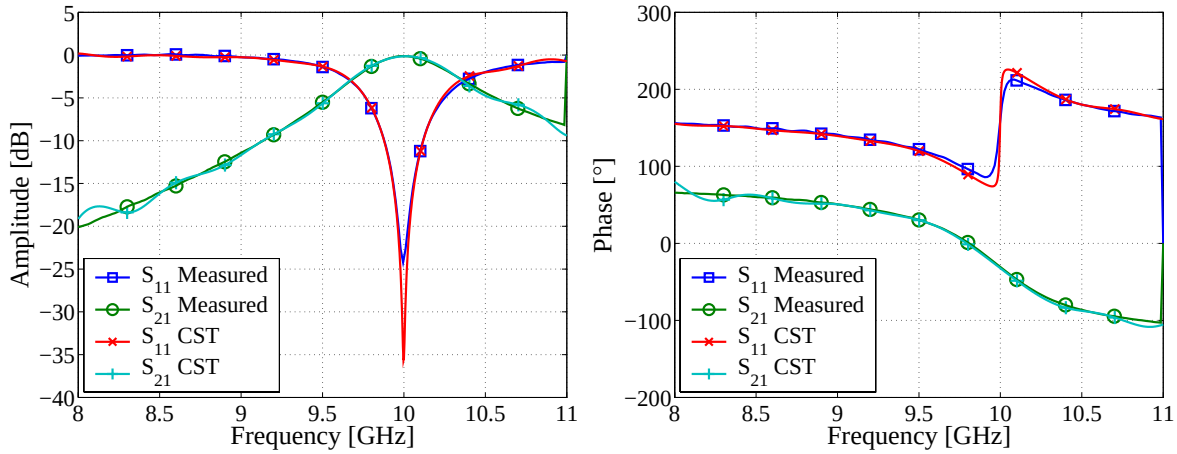


Figure 5.18: Measured Filter vs CST (0.24mm gap)

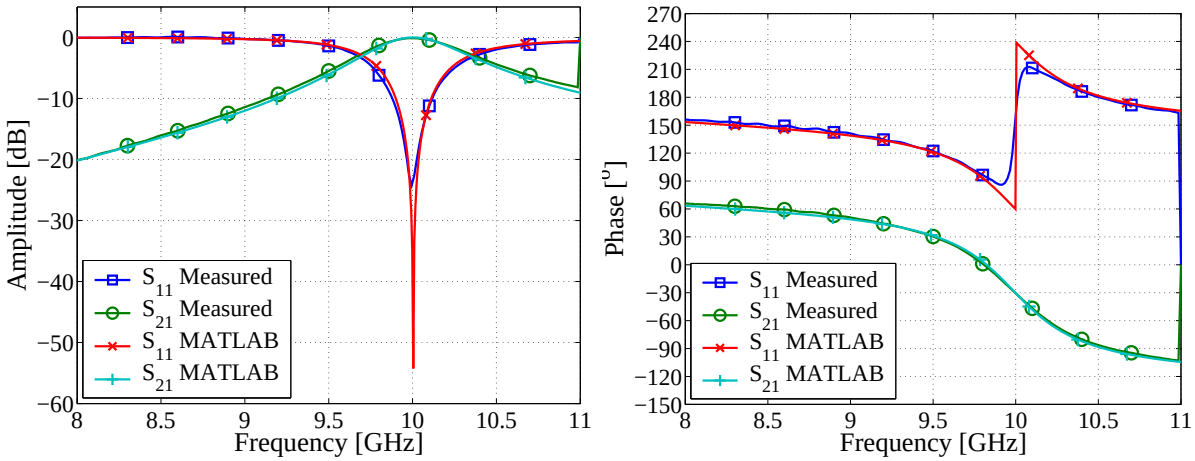
Since the centre frequencies of the measured filters do not agree precisely with the CST Microwave Studio simulations, the gap in the simulated structure is adjusted until a perfect fit is achieved on measured data. Fig. 5.19 shows a filter response with simulated gap distance of 0.408 mm, versus a measured gap distance of 0.38 mm in Fig. 5.16. The graph shows that roll-off characteristics of measured and simulated filters agree very well. A simulated gap distance of 0.34 mm is required to obtain a filter centre frequency match to the measured gap distance of 0.29 mm in Fig. 5.17. These gap differences of 28 μm and 50 μm, cause relatively large centre frequency shifts, and may be attributed to inaccuracies in the travelling microscope measurements.



(a) Magnitude (b) Phase

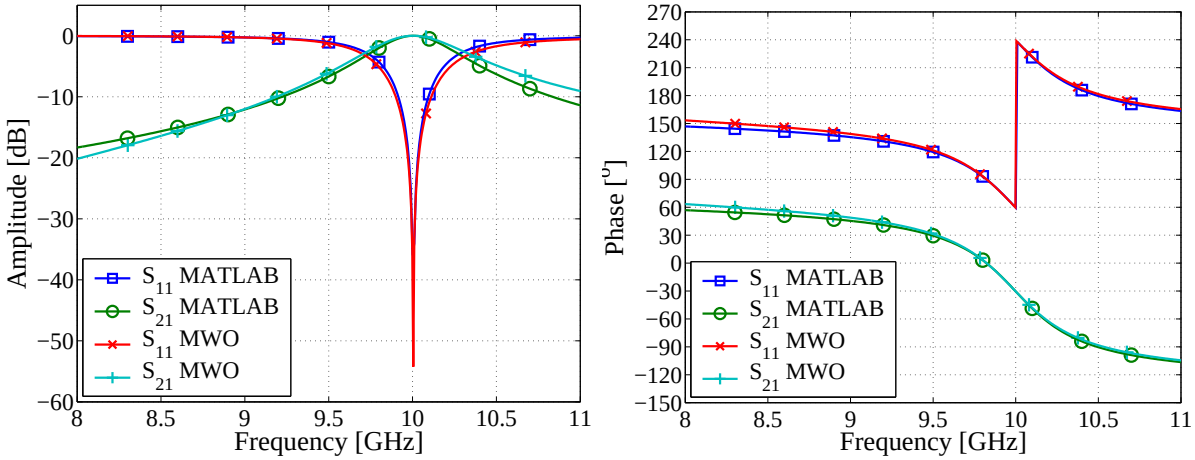
Figure 5.19: Roll-Off Characteristics: Measured Filter (0.38mm gap) vs CST (0.408mm gap)

The first order filter model is implemented in a non-linear lumped element Matlab model. When these simulations are compared to the CST Microwave Studio model, good magnitude and phase correlation is achieved, as shown in Fig. 5.20. As expected, the Matlab and CST Microwave Studio models differ only with respect to the central capacitance value of the filter. As a final comparison, the first order filter model is implemented in AWR Microwave Office with frequency-independent evanescent guide element values and port impedances determined at the centre frequency of 10 GHz. Simulations are plotted against results obtained with the Matlab model in Fig. 5.21. Both AWR and Matlab models use equal values of central capacitance, showing good agreement at the centre frequency, as expected. Subsequent AWR Microwave Office models use a frequency-dependent implementation.



(a) Magnitude (b) Phase

Figure 5.20: Measured Filter vs MATLAB



(a) Magnitude (b) Phase

Figure 5.21: MATLAB vs MWO

5.4 Conclusion

Theory outlined by Craven and Mok [3] is validated through a first order approach, which is then used to design a practical first order filter. The central capacitance of the filter is varied to shift the centre frequency, a property which will prove very useful in the first order switch design in Chapter 6. Measurements of the first order filter prototype are compared to simulations in CST Microwave Studio, ANSYS, AWR Microwave Office and Matlab. The easiest implementation and most time-efficient modelling of the filter is done in AWR Microwave Office, showing good correlation with measurements.

The central capacitive obstacle of the first order filter designed in this chapter is replaced by an active control element in Chapter 6, which may be switched to enforce transmission and reflection of the incoming signal. As mentioned in Chapter 2, PIN diodes are used and implemented in various diode mount topologies. Additional capacitance is formed as part of the diode mount to resonate in series with the PIN diode inductance. To accomplish the frequency shifting ability displayed by the filter, the additional mount capacitance is created to be tunable.

Chapter 6

First Order Switch Design

6.1 Introduction

It was seen in Chapter 2 that existing waveguide PIN diode switches suffer from various drawbacks. One negative aspect is the complex diode mount and bias structures, with tuning of resonators involving the physical deconstruction of the device, slight modification and re-construction. In this chapter, a number of new diode mount topologies are presented, some offering in-situ tuning of resonances. Each diode mount topology is presented with a complete physical model, lumped element feed model, as well as a comparison of filter and limiter measurement versus simulation.

This is followed by the use of each mounting structure in the implementation of a first order evanescent mode X-band switch, with sections of propagating guide at the input and output. Capacitive stubs are used to tune out the junction susceptances, as described in Sec. 4.3.2. The evanescent mode section is implemented in K-band waveguide with cutoff frequency $f_C = 14.047$ GHz, while the propagating section is implemented in X-band waveguide, with a cutoff frequency $f_C = 6.557$ GHz.

6.2 Proposed Switch Topology And Operation

A first order switch is obtained by replacing the central capacitance gap of the first order filter with a pair of back-to-back PIN diodes in a vertical configuration between the broad walls of the below-cutoff waveguide as shown in Fig. 6.1. When reverse biased, the capacitances of the PIN diodes C_{PIN} resonate in parallel with effective guide inductances L_G, to form the central resonator of the filter, as shown in Fig. 6.2. Resonances are

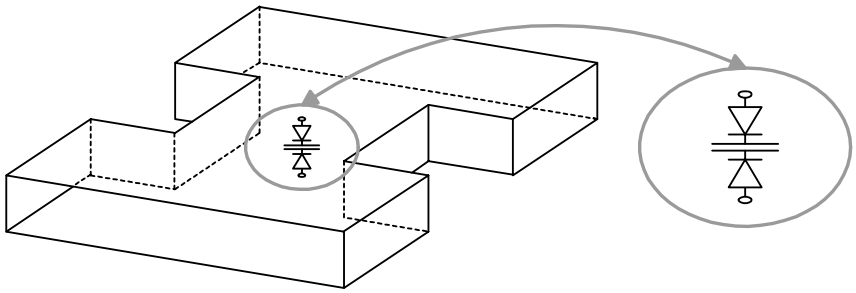


Figure 6.1: Basic Model of Evanescent Mode Waveguide Switch and PIN Diode Branch Setup

indicated by arrows. The diode mount creates additional capacitance C_C to resonate in series with the combined PIN diode inductances L_{PIN}. In the forward bias state, the series resonance between the mount capacitance C_C and combined PIN diode inductances L_{PIN}, remains as in the reverse bias state. The resistive nature of the I-region in the forward bias state results in a thoroughly detuned parallel resonator section, also shown in Fig. 6.2.

Capacitive obstacles are introduced at the junctions between propagating and evanescent mode guide to tune out junction susceptances, resulting in a third order filter response. As

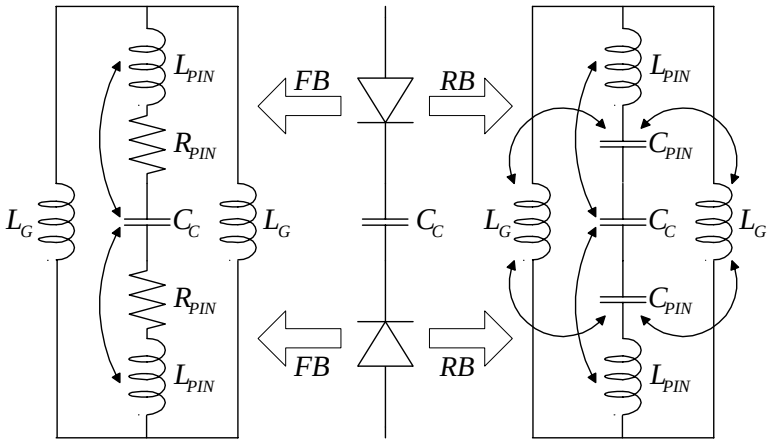


Figure 6.2: Forward and Reverse Bias Conditions of PIN diode branch

described in Sec. 4.3.3, the evanescent mode obstacle admittance is not necessarily equal to the propagating, or free-space, obstacle admittance. The element values of the AWR Microwave Office PIN diode and mount model therefore differ from the element values of the physical model of the measured structure and CST Microwave Studio model. Physical dimensions of the PIN diode and mounting structure, as well as manufacturer's data for capacitance and resistance in the reverse bias and forward bias states, is entered in the CST Microwave Studio model. The evanescent mode PIN diode model, although identical in structure to the free-space PIN diode model, employs lumped element values not equal

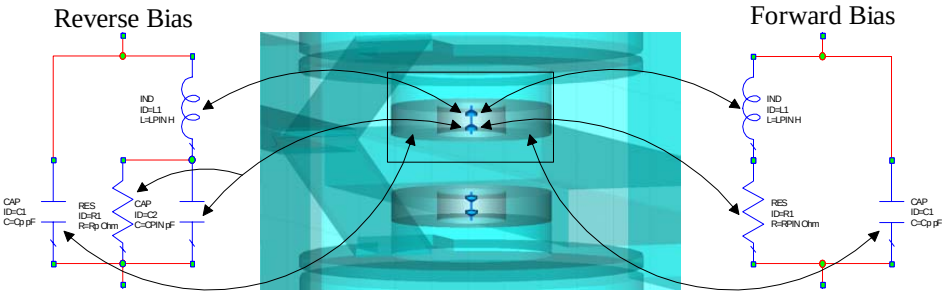


Figure 6.3: CST and AWR Model Structure for Reverse And Forward Bias

to manufacturers data. These element values are obtained as follows:

Each switch is tuned to a number of frequencies by varying mount capacitance C_C, and measured in filter and limiter states, with and without junction capacitances C_J. The PIN diode model is optimized in both bias states for an optimal AWR Microwave Office model fit to all the filter/limiter measurements for all four prototypes, by varying only the mount and junction capacitances. The best model fit over the entire range of measurements is found with PIN diode element values listed in Table 6.1. The range of measurements with AWR Microwave Office model fit are presented in Appendix A. The evanescent mode capacitance values (AWR Model) are higher than the free-space equivalents (CST Model), while the evanescent mode inductance value (AWR Model) is equal to its free-space equivalent (CST Model). AWR Microwave Office modelling of the filter in Chapter 5

PIN DIODE ELEMENT	CST MODEL	AWR MODEL
C_{PIN} (pF)	0.2	0.37
C_p (pF)	0.14	0.3
L_{PIN} (nH)	0.217	0.217
R_s (Ω)	2	1

Table 6.1: Free-Space vs. Evanescent Mode PIN Diode Element Values

proves that it is the solver package most suited to allow simple model implementation and fast simulation times. To ensure that the simulation accuracy remains the same when implementing diode mounts in forward and revere bias states, instead of the simple central capacitance of the first order filter, one of the topologies is implemented in AWR Microwave Office and CST Microwave Studio. Measurements with PIN diodes in the reverse and forward bias state, with junction rotors tuned in and out, are used to ensure an accurate fit of both simulation models. The complete CST Microwave Studio model is shown in Fig. 6.4, and simulations versus measurements are shown in Fig. 6.5 and Fig. 6.6 respectively.

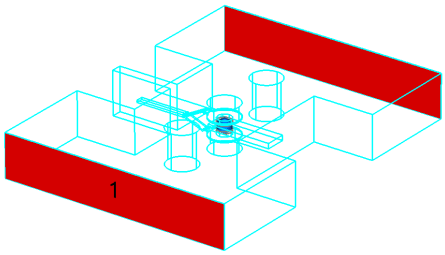


Figure 6.4: CST Microwave Studio Model (Dimensions in Appendix B)

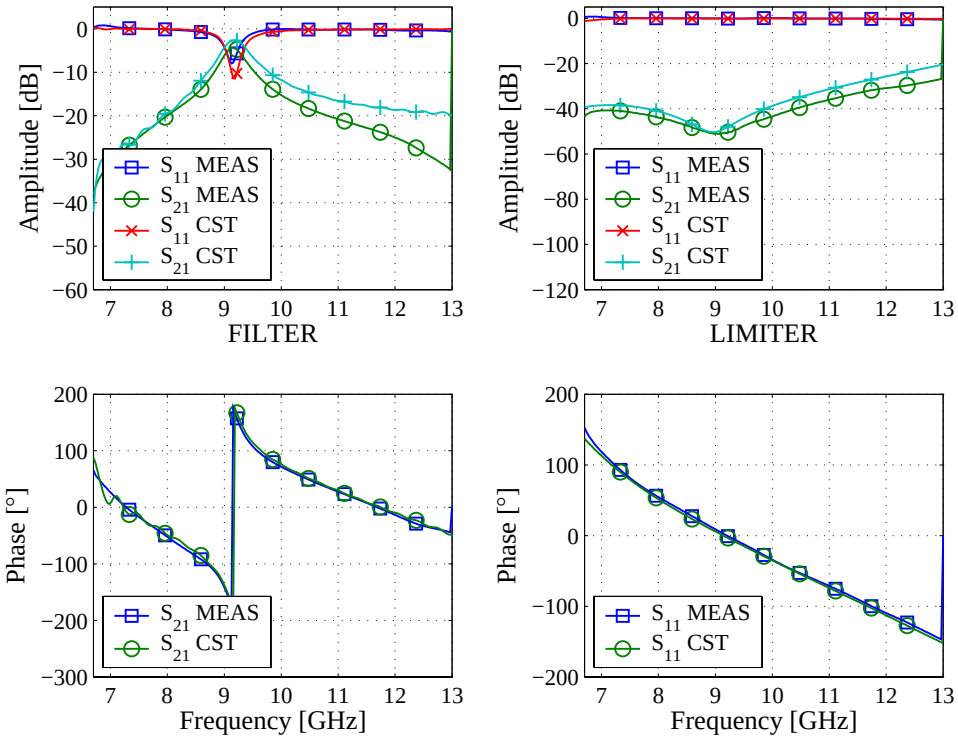


Figure 6.5: Measurement vs. CST Simulation (No Junction Tuners)

The simulation results agree fairly well with measured data at lower frequencies. In the upper part of the frequency band, above 10-11 GHz, the fit becomes less accurate, resulting in the simulated filter having a greater bandwidth than the measured filter. This behaviour occurs in filtering and limiting stages, with junction tuners tuned in and out. The same measurement is now compared to an AWR Microwave Office simulation.

The complete AWR Microwave Office models in the reverse and forward bias states are shown in Fig. 6.7, and simulations versus measurements are shown in Fig. 6.8 and Fig. 6.9. Propagating phase is added at the input and output of the model using S-parameter blocks of propagating guide simulated in CST Microwave Studio. The operation is performed in Matlab using *ABCD* parameters, since waveguide phase information could not be obtained in suitable form in AWR Microwave Office. The simulation results agree fairly well with

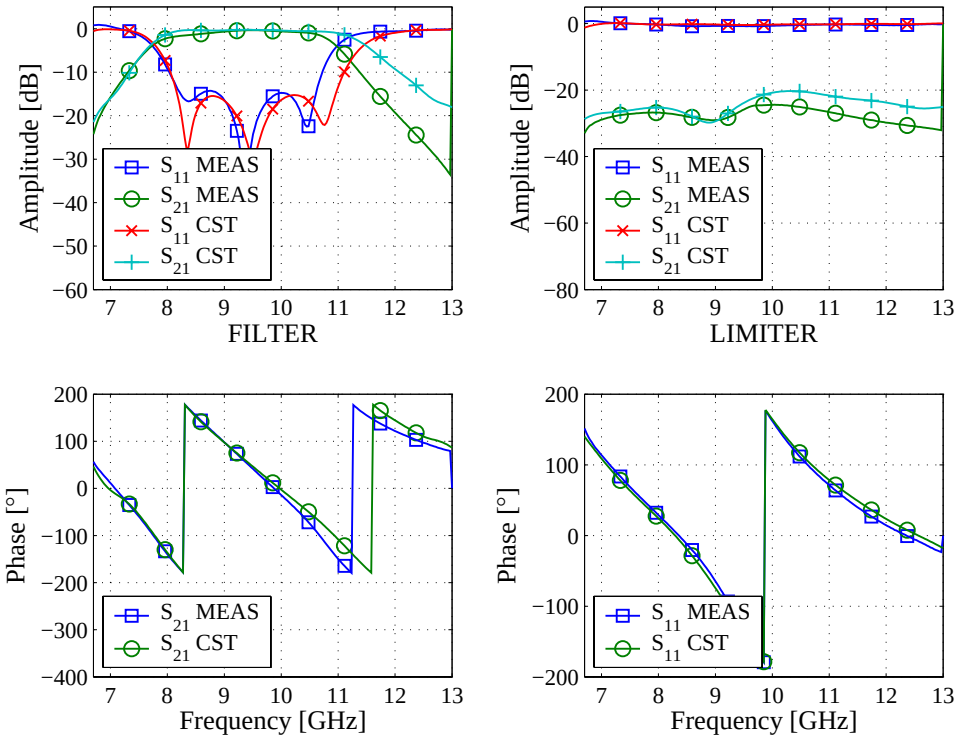


Figure 6.6: Measurement vs. CST Simulation (Added Junction Tuners)

measured data over the frequency range of interest. At higher frequencies, above 12 GHz, the fit becomes less accurate, as seen in the CST Microwave Studio model.

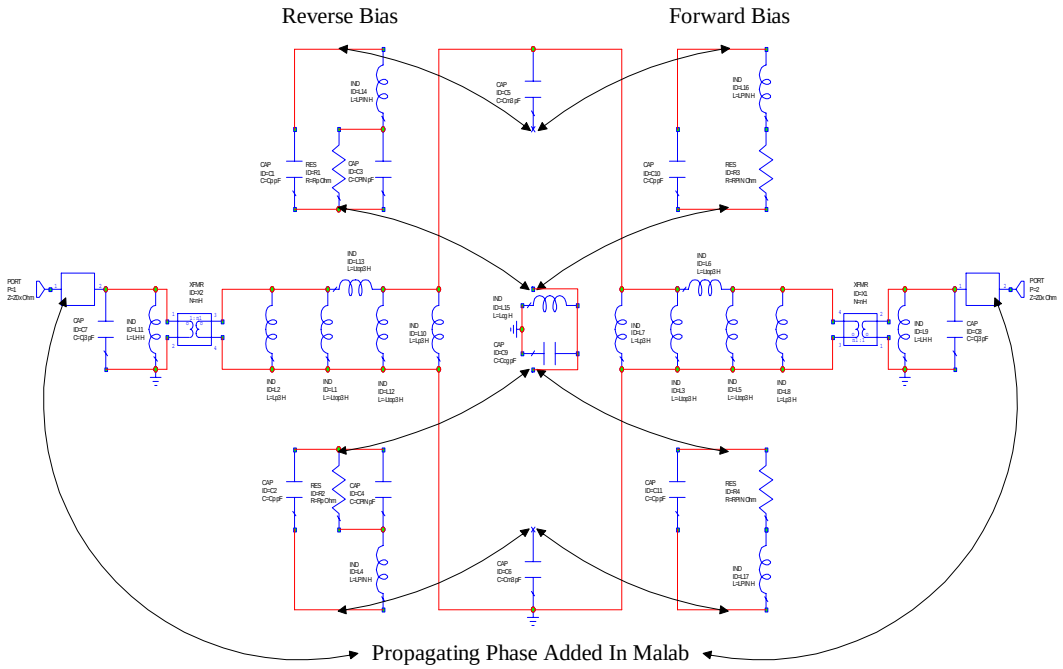


Figure 6.7: AWR Microwave Office Model

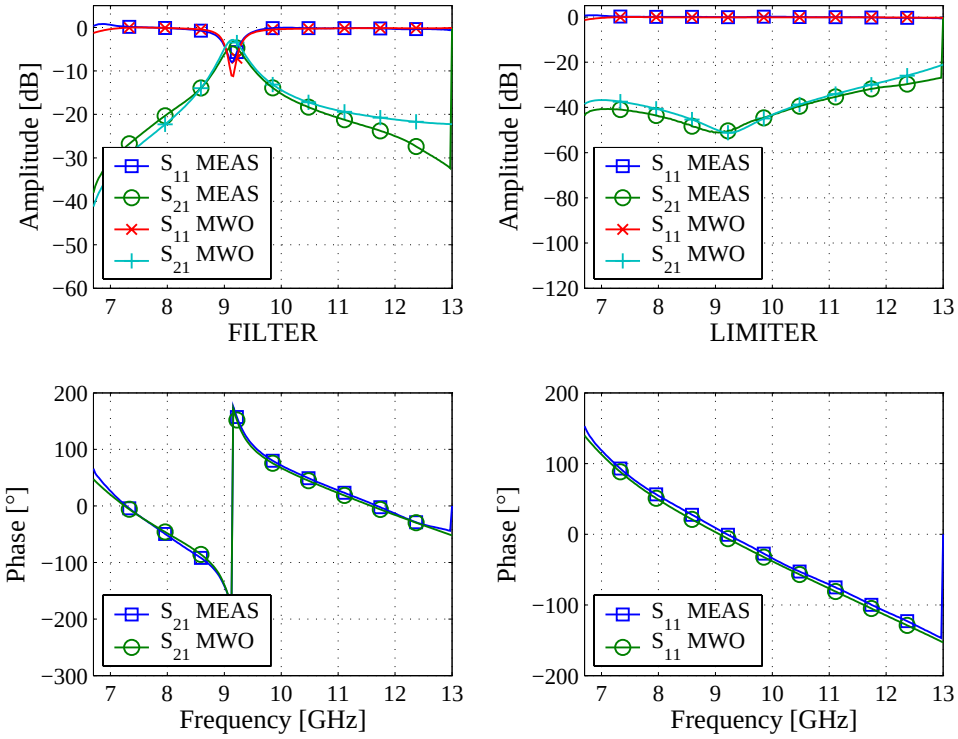


Figure 6.8: Measurement vs. AWR Simulation (No Junction Tuners)

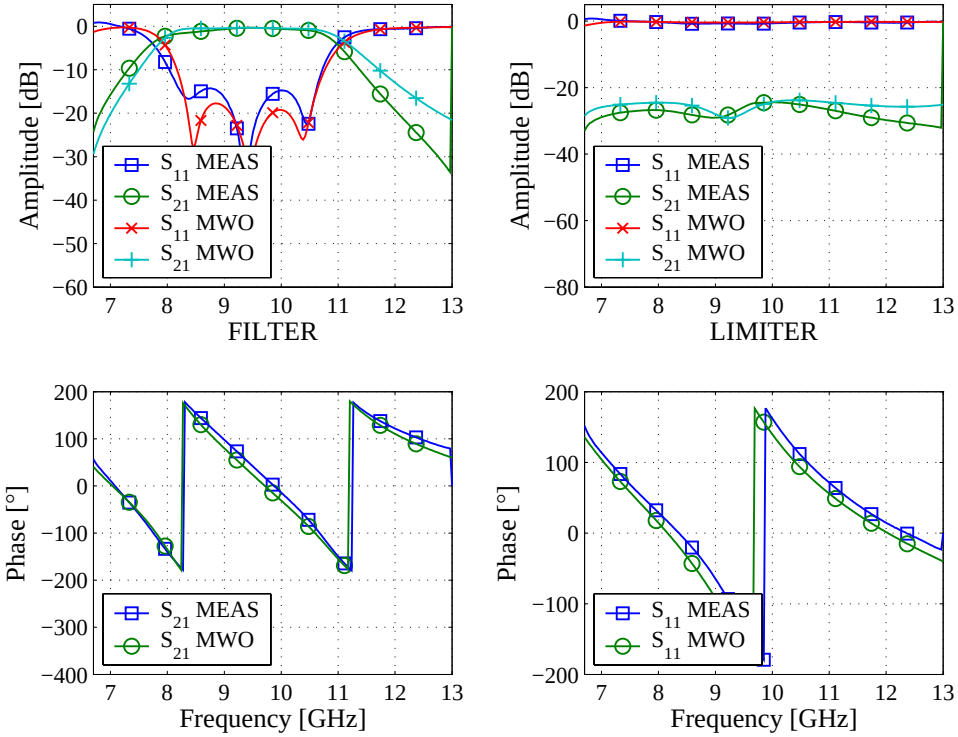


Figure 6.9: Measurement vs. AWR Simulation (Added Junction Tuners)

The linear solver used in AWR Microwave Office allows the model to be adjusted and fitted to measured data more efficiently than the CST Microwave Studio model, with

good results. It is therefore used in the subsequent modelling of all PIN diode mounting structures. Identical PIN diode element values are used in the implemented models. Various mount topology models are designed and integrated with the existing PIN diode model as shown in Section 6.3. The only variable parameters in the switches are the central capacitances C_C and junction capacitances C_J.

6.3 Diode Mount Topologies

This section presents a number of new PIN diode mount structures in waveguide, divided into four main topologies. The mounts are implemented in a first order (2-diode) switch prototype. Structures are named according to ground, feed and mount capacitance characteristics. "Vertical" refers to ground or feed lines entering through the broad walls of the waveguide, while "horizontal" refers to ground or feed lines entering through the narrow walls of the waveguide. PIN diodes are biased at -10 V in the reverse bias state and 20 mA in the forward bias state.

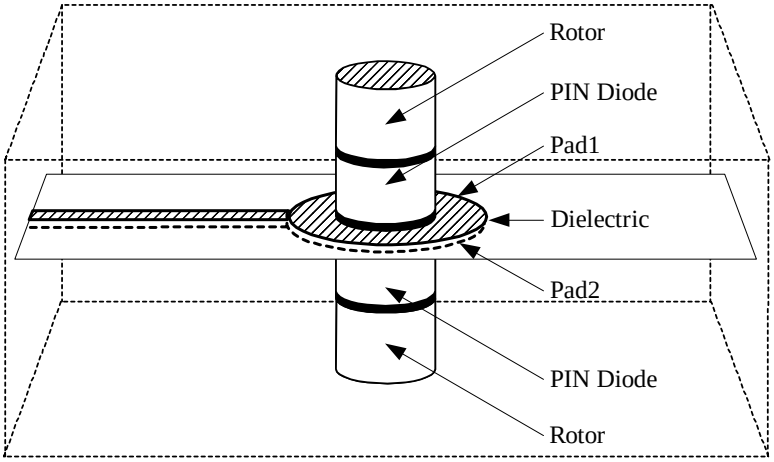
The evanescent guide length on either side of the diode may be changed to control the bandwidth of the structure. Two switches are designed for 15 and 25 % fractional bandwidths respectively. One of the mount topologies, with in-situ tuning ability, achieves a fractional bandwidth of 25.5% in the 25% BW structure, with 15 dB reflection coefficient and 1.53 dB insertion loss when filtering, and 24.4 dB isolation and 0.913 dB reflection loss when limiting. These results are very good, considering the wide bandwidth and performance figures obtained by using only two PIN diodes.

6.3.1 PIN Diode Mount Topology 1

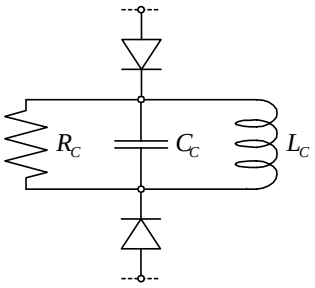
Vertical-Ground Horizontal-Feed Substrate Design

The first structure of topology 1 is shown in Fig. 6.10. The DC-feed, entering horizontally through the narrow wall of the waveguide, consists of a thin microstrip line on either side of a substrate with $\epsilon_r = 2.2$. Two etched circular pads on the ends of the lines, form the central capacitance C_C which separates the two diodes. The PIN diodes are soldered onto brass tuning rotors, which are firmly grounded to the waveguide through their housings, and entered vertically into the waveguide from the top and bottom respectively, until a firm push contact between the diodes and substrate capacitance pads is achieved. The structure is implemented in the approximate 25% fractional bandwidth switch, achieving

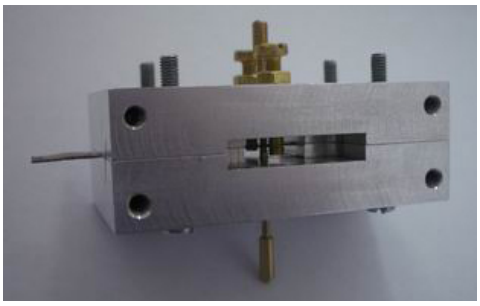
a switch fractional bandwidth of 29.4%, with 14 dB reflection coefficient and 2.37 dB insertion loss when filtering, and 17 dB isolation and 3.35 dB reflection loss when limiting, as shown in Fig. 6.11.



(a) Physical Setup



(b) Lumped Element Feed Line Model

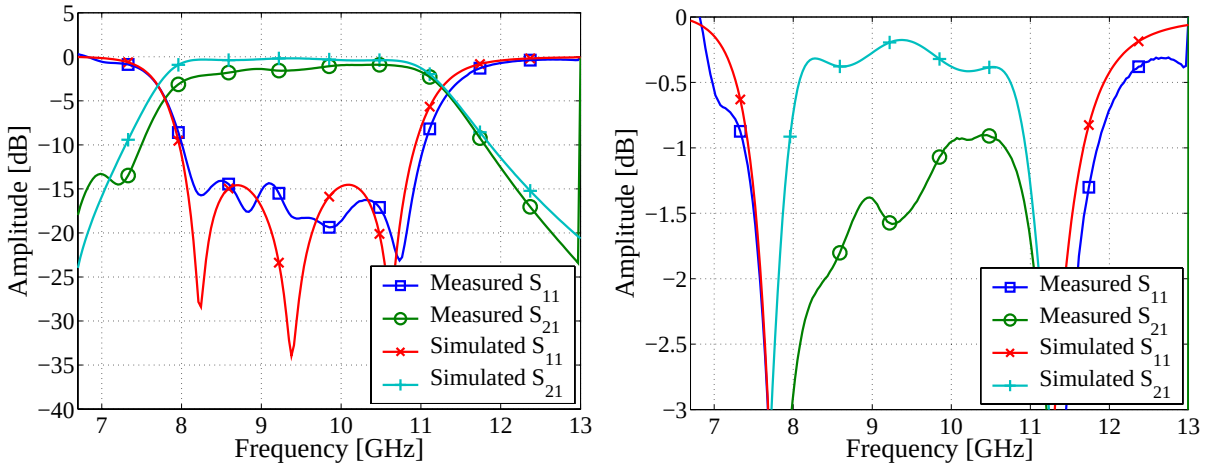


(c) Prototype

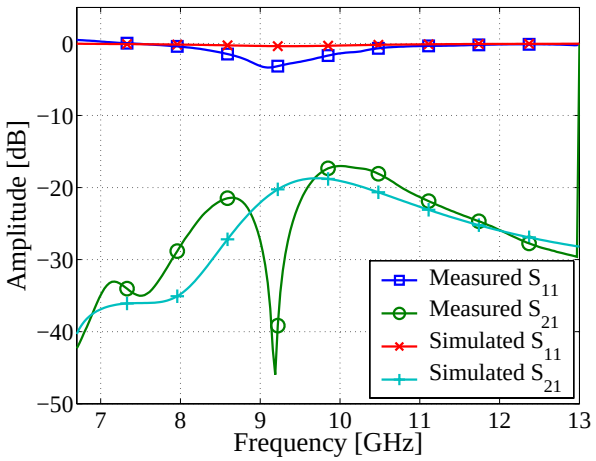
Figure 6.10: Vertical-Ground Horizontal-Feed Substrate Design (Dimensions in Appendix B)

A number of capacitance pad sizes, shifting the centre frequency of the switch between 9.27 GHz and 10.76 GHz, are measured. All measured pad sizes display effective filter and limiter states, as shown in Appendix A. Only one measurement is shown here. AWR Microwave Office modelling of the double-feed design shows inductive behaviour in parallel with the central capacitance pad, depicted by L_C, with added loss component R_C in Fig. 6.10. This phenomena may be explained with transmission line theory, showing that the input impedance of the microstrip feed line, as seen from the centre of the waveguide, displays inductive properties with the end of the line shorted, representing the low impedance of the waveguide wall.

A stepped-impedance lowpass filter, shown in Fig. 6.12, is implemented as part of the feed to ensure that no RF signal leakage occurs at the narrow wall feed exit point. This filter is housed in the wall of the switch. Top and bottom feed-line filters are insulated



(a) Filter



(b) Limiter

Figure 6.11: Measurement vs. Theory

from the waveguide by etched sections of substrate, effectively implementing a stripline environment. Switch wall dimensions limit minimum and maximum filter line widths to 0.2 mm and 2.6 mm, respectively, while the maximum filter length is limited to 22 mm. The filter is designed for a cutoff frequency of 4 GHz and 40 dB attenuation at 8 GHz, ensuring that no RF signal leakage occurs at the X-Band operating frequency.

By trimming the excess substrate around the central feeds and capacitance pads, as depicted in Fig. 6.13, the insertion loss during filtering and isolation during limiting is improved slightly, showing that the substrate suspended across the entire width of the guide causes additional attenuation.

The design displays the ability to switch effectively between filter and limiter states. Its drawbacks include high insertion loss when filtering and the inability to shift the operating frequency of the switch through simple tuning. The centre frequency can only be shifted

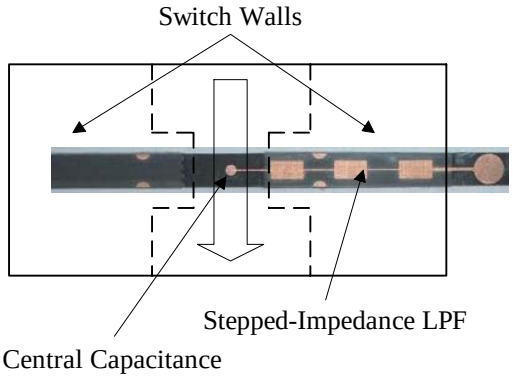
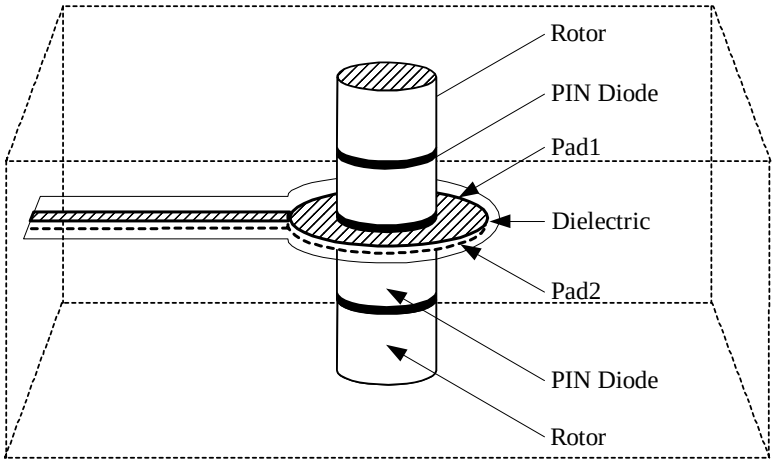
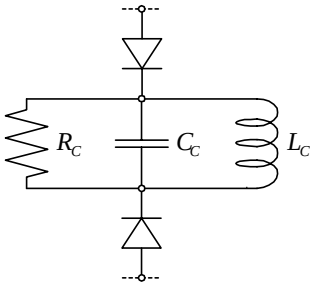


Figure 6.12: Stepped-Impedance Lowpass Filter Prototype



(a) Physical Setup



(b) Lumped Element Feed Line Model

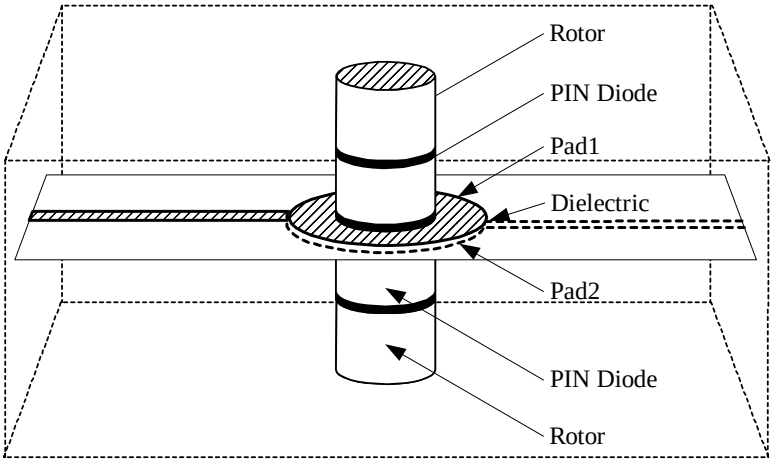
Figure 6.13: Vertical-Ground Horizontal-Feed Trimmed Substrate Design (Dimensions in Appendix B)

by varying the central capacitance pad size, a timely process involving deconstruction and reconstruction of the switch.

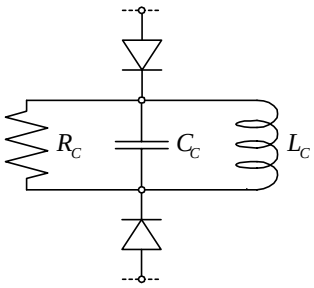
Vertical-Ground Opposing-Horizontal-Feed Substrate Design

The second structure of topology 1 is modified slightly from the first structure, as shown in Fig. 6.14. Due to a resonant peak experienced with certain central capacitance pad sizes in the limiting response of the previous design, the feed for the top and bottom PIN diodes is changed to enter from opposing sides of the guide. The diode mount is implemented in the approximate 25% fractional bandwidth switch, achieving a switch fractional bandwidth of 25.62%, with 15.3 dB reflection coefficient and 1.61 dB insertion loss when filtering, and 19.7 dB isolation and 1.94 dB reflection loss when limiting, as shown in Fig. 6.15.

Although the structure improves the resonance in the limiting response, it does not



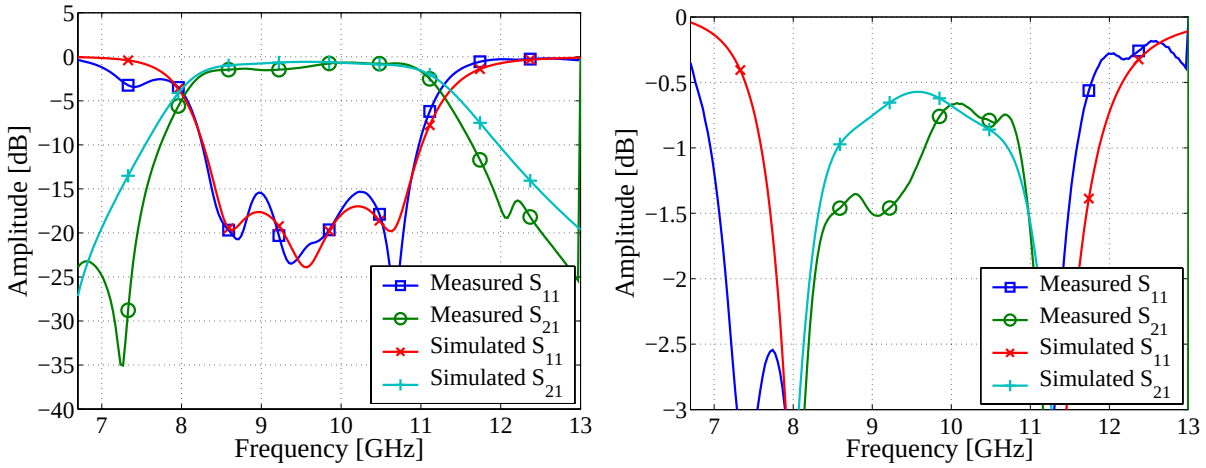
(a) Physical Setup



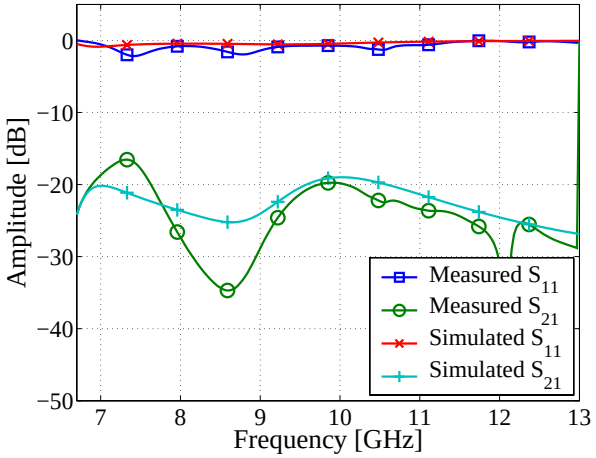
(b) Lumped Element Feed Line Model

Figure 6.14: Vertical-Ground Opposing-Horizontal-Feed Substrate Design (Dimensions in Appendix B)

eliminate it completely. The opposing-feed implementation also displays the high insertion loss characteristics of the previous structure. A further improvement to the topology is presented next.



(a) Filter



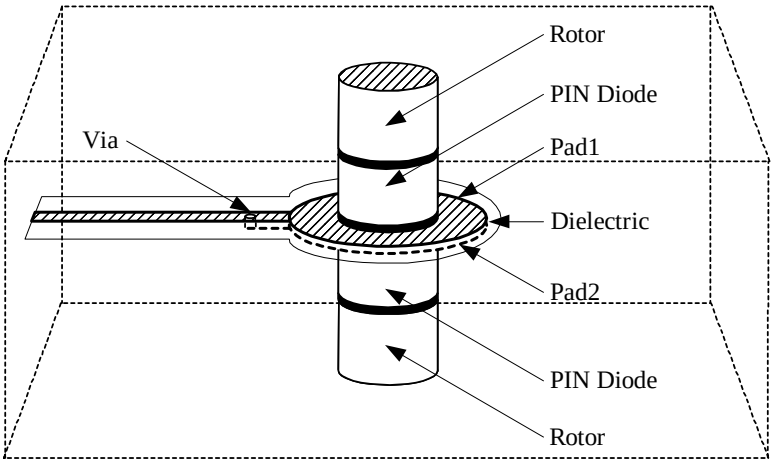
(b) Limiter

Figure 6.15: Measurement vs. Theory

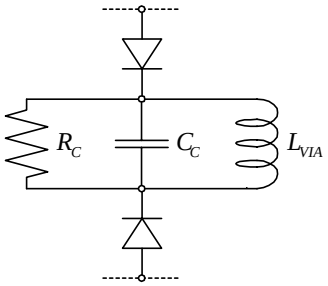
Vertical-Ground Horizontal-Feed Via Substrate Design

The third structure of topology 1 is presented in Fig. 6.16. A via transfers the bias from a single transmission line entering the waveguide to top and bottom capacitance pads. The PIN diodes are soldered onto brass tuning rotors, which are firmly grounded to the waveguide through their housings, and entered vertically into the waveguide from the top and bottom, until a firm push contact between the diodes and substrate capacitance pads is achieved. The diode mount is implemented in the approximate 25% fractional bandwidth switch, achieving a switch fractional bandwidth of 24.6%, with 16.5 dB reflection coefficient and 1.27 dB insertion loss when filtering, and 14.6 dB isolation and 1.4 dB reflection loss when limiting, as shown in Fig. 6.17.

Insertion loss during filtering is reduced from 2.36 dB in the previous design to 1.27 dB, while reflection loss during limiting is reduced from 3.34 dB to 1.4 dB. The drawbacks of



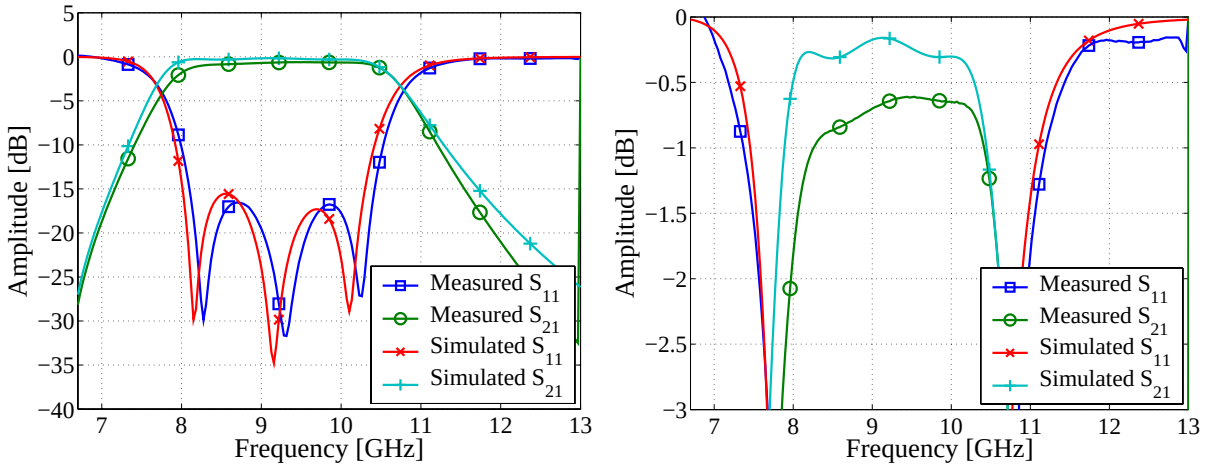
(a) Physical Setup



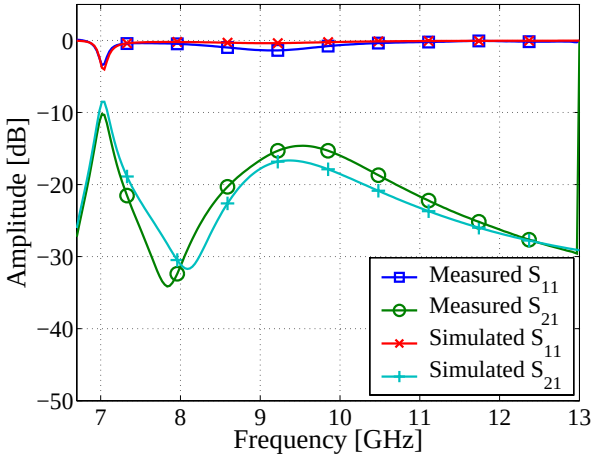
(b) Lumped Element Feed Line Model

Figure 6.16: Vertical-Ground Horizontal-Feed Via Substrate Design (Dimensions in Appendix B)

the design include a reduced isolation from 17 dB to 14.6 dB, and reduced filter bandwidth from 29.4% to 24.6%. The lumped element model of the mount/feed structure consists of a central capacitance C_C, and corresponding loss component R_C, as well as inductance L_{VIA}, to model the via. Implementation of the via proves very useful, as it offers a simple solution to improved filtering and limiting characteristics. In terms of the greater design objective, the inability to shift the operating frequency prevents it from being implemented effectively in higher order designs.



(a) Filter



(b) Limiter

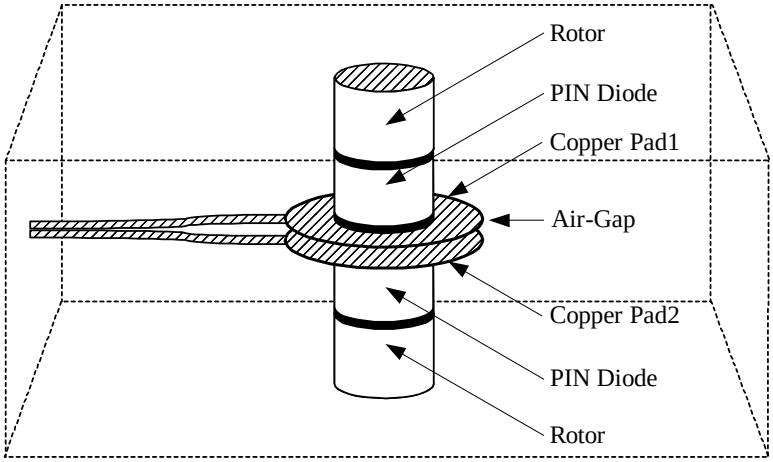
Figure 6.17: Measurement vs. Theory

6.3.2 PIN Diode Mount Topology 2

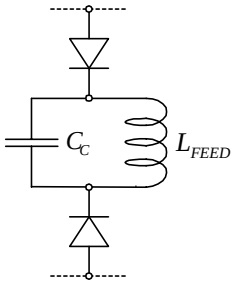
Vertical-Ground Horizontal-Feed Air-Gap Design

The second topology is shown in Fig. 6.18. By effectively "removing" the substrate of the via mount/feed structure, the central capacitance C_C has an air-dielectric between two circular pads made of 0.1 mm thick copper shimstock, which may be adjusted in height to realize a tunable central capacitor. The PIN diodes are again soldered onto brass tuning rotors, which are firmly grounded to the waveguide through their housings, and entered vertically into the waveguide from the top and bottom, until a push contact between the diodes and capacitance pads is achieved. By varying the protruding depth of the diode-mounted tuning rotors into the waveguide, the air-gap distance between the central capacitance pads may be altered, changing the central capacitance value. The diode mount is implemented in the approximate 25% fractional bandwidth switch, achieving

a switch fractional bandwidth of 23.3%, with 22 dB reflection coefficient and 0.8 dB insertion loss when filtering, and 18 dB isolation and 1.1 dB reflection loss when limiting, as shown in Fig. 6.19.



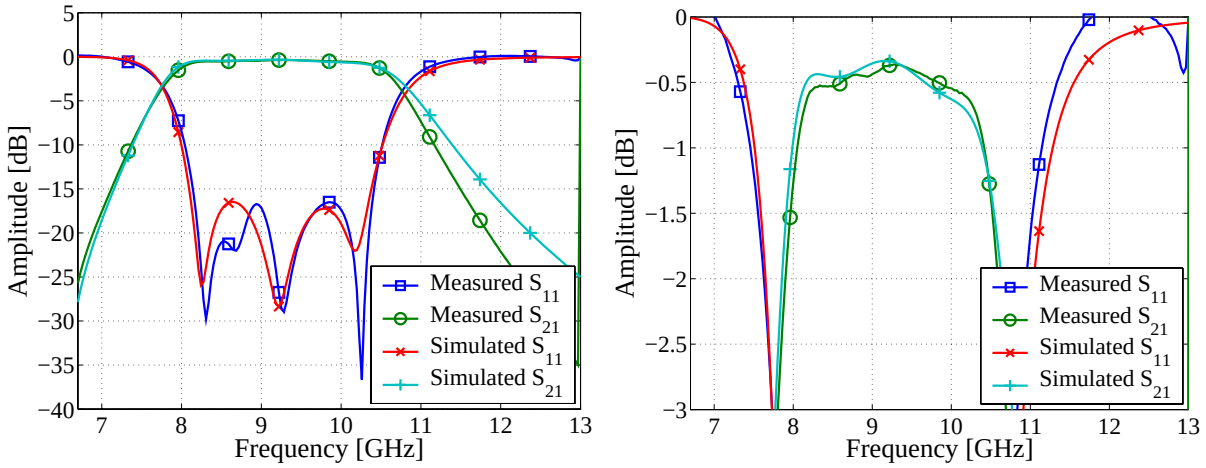
(a) Physical Setup



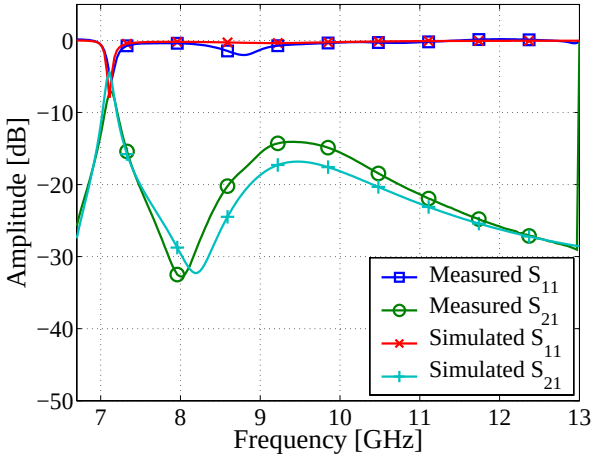
(b) Lumped Element Feed Line Model

Figure 6.18: Vertical-Ground Horizontal-Feed Air-Gap Design (Dimensions in Appendix B)

The lumped element model of the mount/feed structure consists of a central capacitance C_C, as well as inductance L_{FEED}, to model the DC-feed line. Maintaining good DC contact between the PIN diodes and the air-gap capacitance pads proves problematic due to the poor spring qualities of the copper shimstock setup and the mere push contact between PIN diodes and capacitance pads. Implementing tuning rotors with non-rotating extruding stubs can solve this problem, allowing the PIN diodes to be soldered onto the capacitance pads directly.



(a) Filter



(b) Limiter

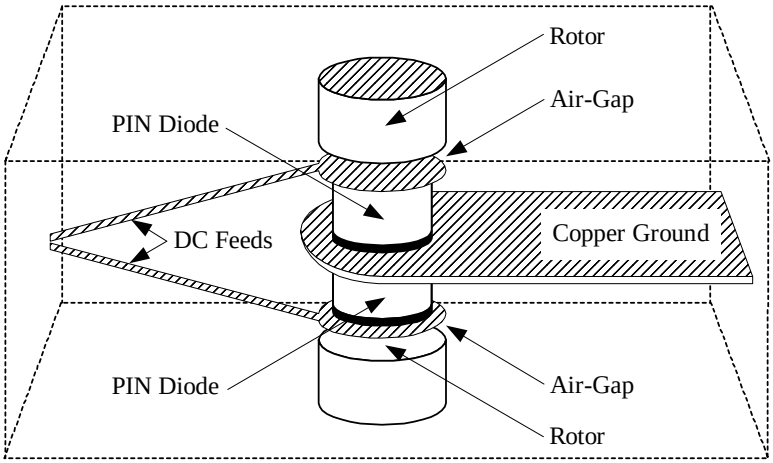
Figure 6.19: Measurement vs. Theory

6.3.3 PIN Diode Mount Topology 3

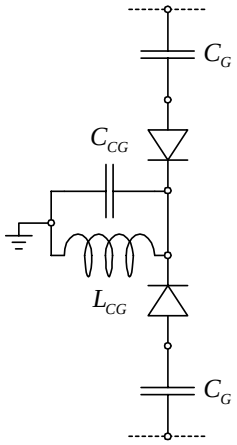
Horizontal-Ground Horizontal-Feed Air-Gap Design

The third topology is shown in Fig. 6.20. The dynamics of the setup are changed by introducing a central horizontal-ground in the waveguide, protruding from the narrow-wall of the waveguide. Two PIN diodes are soldered onto the top and the bottom of the central-ground plane respectively, thereby removing the central capacitance C_C of the previous two mount/feed structures. Feed lines, constructed from 0.1 mm copper shimstock with added circular pads at the ends, feed DC bias to the top and bottom diodes. The circular pads serve as one side of the air-gap capacitances, formed between the pads and tuning rotors protruding from the top and bottom of the waveguide. The central capacitance of the previous designs, C_C, has therefore been replaced by two tunable air-gap capacitances, C_G, as shown in Fig. 6.20. The mount is implemented in the approximate 15 and 25%

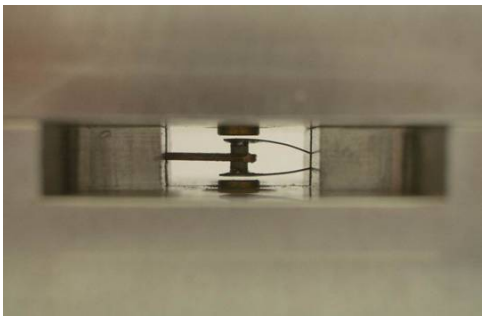
fractional bandwidth switches, achieving a switch fractional bandwidth of 15% in the 15% BW structure, with 22 dB reflection coefficient and 0.8 dB insertion loss when filtering, and 18 dB isolation and 1.1 dB reflection loss when limiting, as shown in Fig. 6.21. It also achieves a switch fractional bandwidth of 25.5% in the 25% BW structure, with 15 dB reflection coefficient and 1.53 dB insertion loss when filtering, and 24.4 dB isolation and 0.913 dB reflection loss when limiting, as shown in Fig. 6.22.



(a) Physical Setup



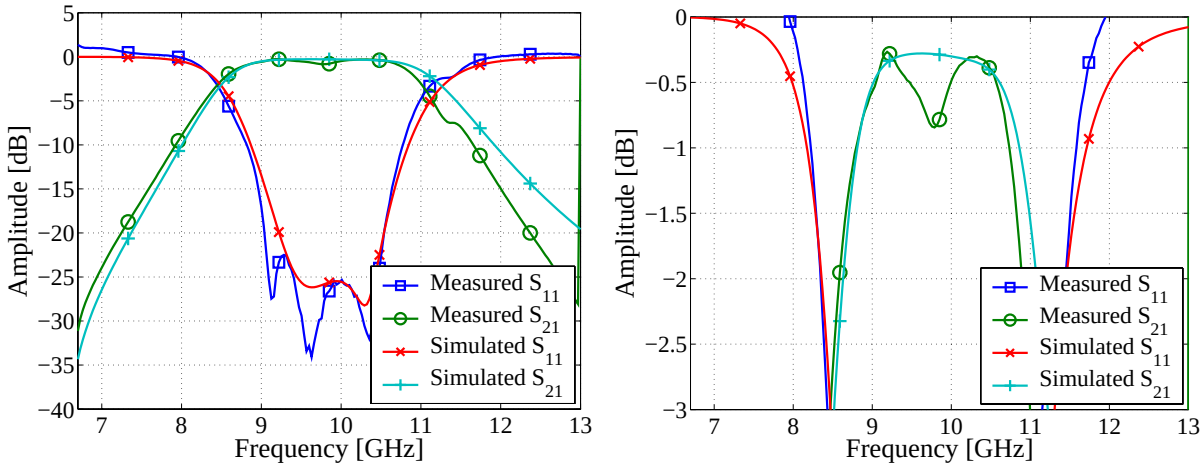
(b) Lumped Element Feed Line Model



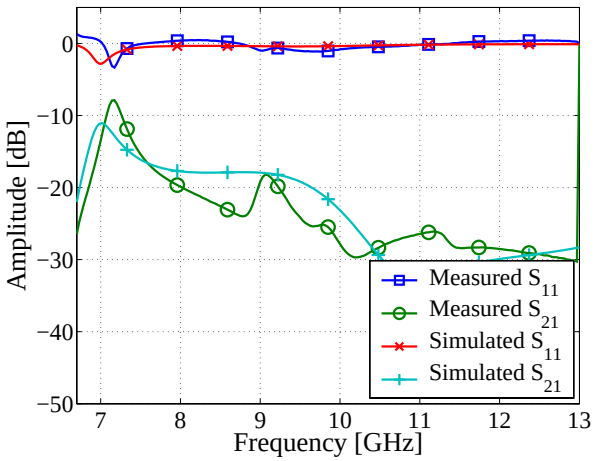
(c) Prototype

Figure 6.20: Horizontal-Ground Horizontal-Feed Air-Gap Design (Dimensions in Appendix B)

The lumped element model of the mount/feed structure consists of a two air-gap capacitances C_G, as well as a parallel combination of C_{CG} and L_{CG} to model the horizontal central-ground plane. The influence of both the ground and feed lines in the mount are reduced by having them enter through the narrow wall of the waveguide, which makes them roughly perpendicular to the electric field orientation. Improved insertion loss and reflection loss characteristics when filtering and limiting respectively, as well as the simple



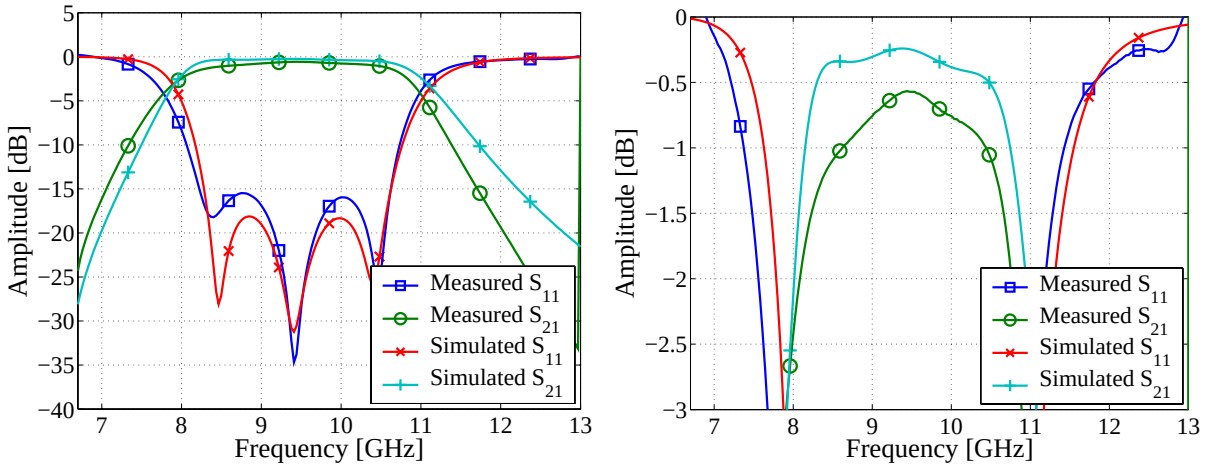
(a) Filter



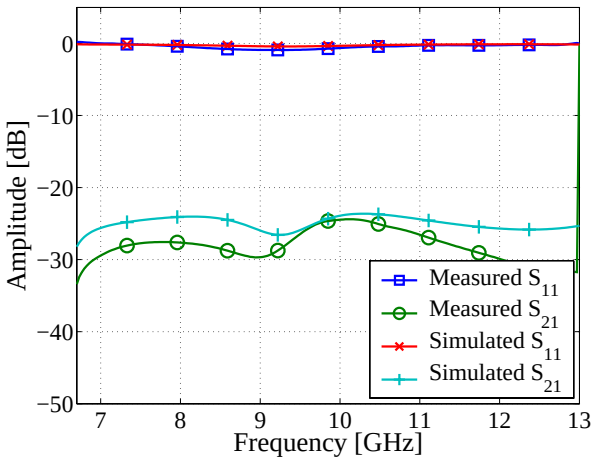
(b) Limiter

Figure 6.21: 15 % Fractional BW Structure - Measurement vs. Theory

in-situ tuning ability, ensure the central-ground design as first choice in the implementation of a higher order switch structure.



(a) Filter



(b) Limiter

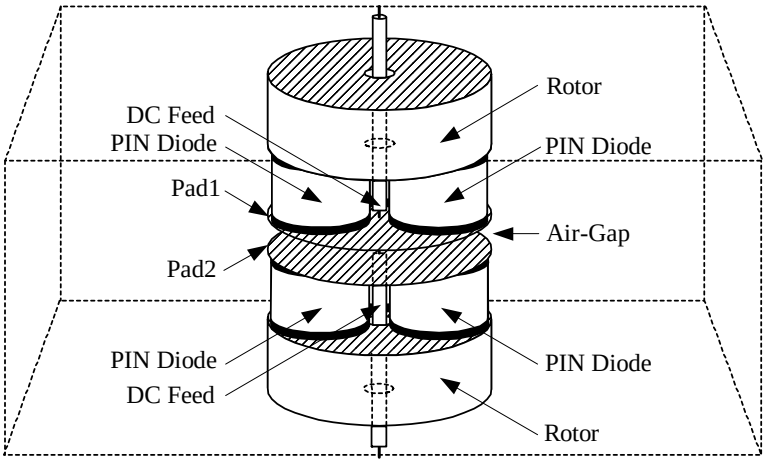
Figure 6.22: 25 % Fractional BW Structure - Measurement vs. Theory

6.3.4 PIN Diode Mount Topology 4

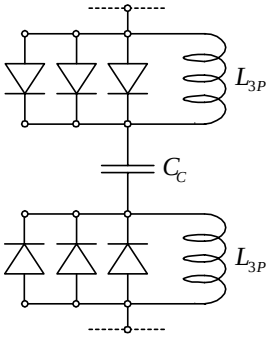
Vertical-Ground Vertical-Feed Three-Diode Design

The first structure of topology 4 is shown in Fig. 6.23. The vertical-feed diode mount allows simple diode replacement in the case of switch failure and offers in-situ tuning. Complete diode units, with integrated DC-feeds, are secured into place. Three diodes are soldered around a central feed hole in the rotor, between the rotor and a 0.1 mm copper shimstock plate. The shimstock plates of the top and bottom diode structures are indicated by Pad1 and Pad2 in Fig. 6.23. The feed runs insulated through the hole in the tuning rotor to the copper plate. The diode units are inserted vertically from the top and bottom into the guide, separated by a central air-gap capacitance C_C. The mounts are implemented in the approximate 15% fractional bandwidth switch, achieving a switch fractional bandwidth of 11.8%, with 15 dB reflection coefficient and 1.56 dB insertion loss

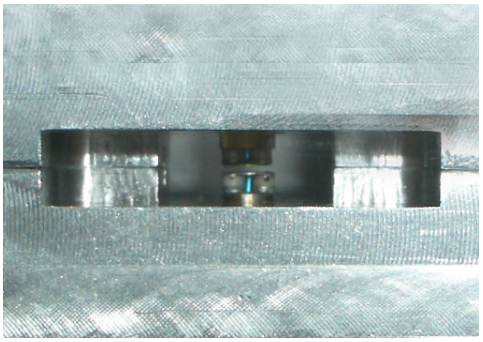
when filtering, and 6.9 dB isolation and 1.65 dB reflection loss when limiting, as shown in Fig. 6.24.



(a) Physical Setup



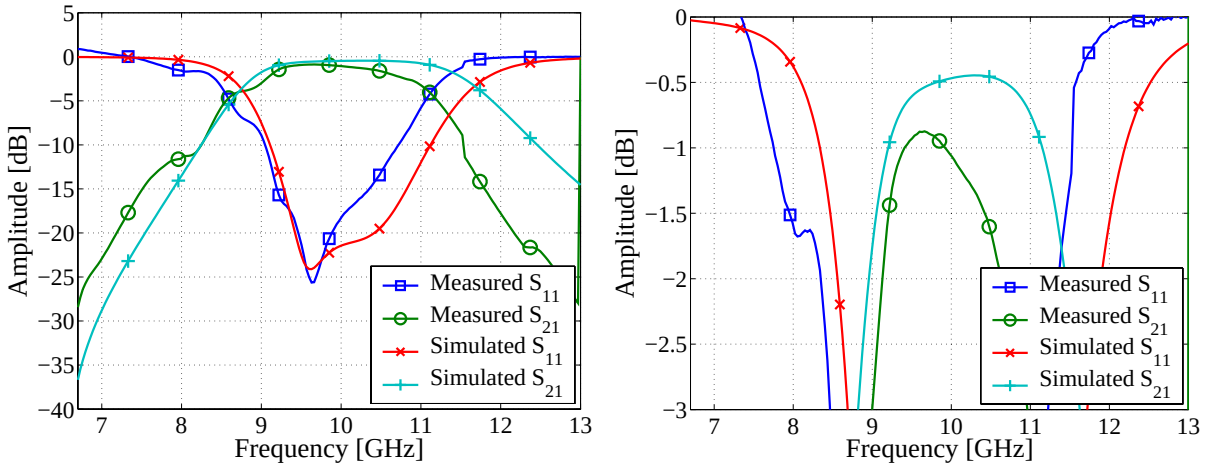
(b) Lumped Element Feed Line Model



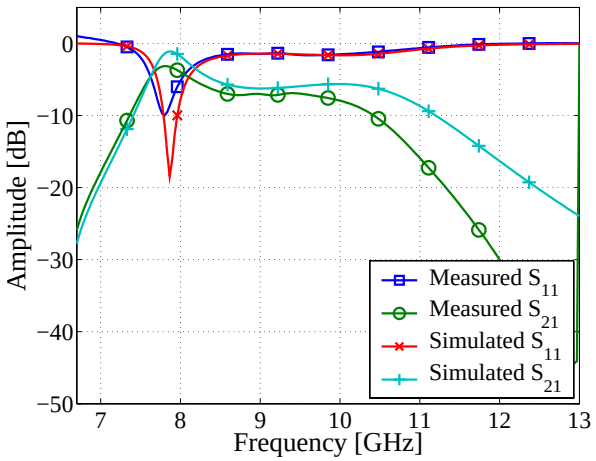
(c) Prototype

Figure 6.23: Vertical-Feed Three Diode Design (Dimensions in Appendix B)

The lumped element model of the mount/feed structure consists of a central capacitance C_C, as well as inductances L_{3P}, in parallel with the PIN diodes to model the interaction between the diodes. This interaction between PIN diodes mounted between the same tuning rotor and copper plate, causes the frequency shift between forward and reverse bias conditions to be insufficient to achieve useful limiting properties. The practical replacement advantages created by the design are overshadowed by their poor performance characteristics.



(a) Filter



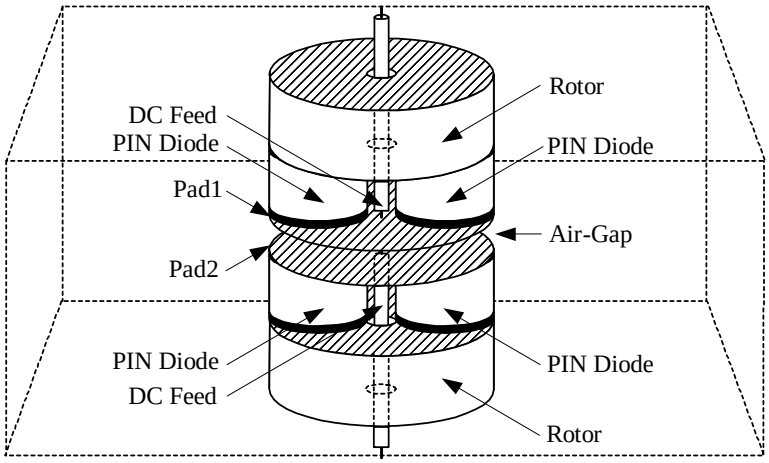
(b) Limiter

Figure 6.24: Measurement vs. Theory

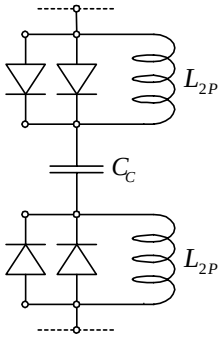
Vertical-Ground Vertical-Feed Two-Diode Design

The second structure of topology 4 is adapted from the last structure, and is shown in Fig. 6.25. The *Vertical-Feed Three-Diode* mount is changed to incorporate two diodes per mount to ensure that the diodes are on the centre line of the propagating direction in the guide to maintain symmetry. The remainder of the design is identical to the three-diode unit. The mounts are implemented in the approximate 15% fractional bandwidth switch, achieving 18.2 dB isolation and 1.2 dB reflection loss when limiting, and very poor filtering charcteristics, as shown in Fig. 6.26.

The lumped element model of the mount/feed structure consists of a central capacitance C_C, as well as inductances L_{2P}, in parallel with the PIN diodes to model the interaction between the diodes. The non-symmetrical layout of the three-diode design was initially thought to be part of the cause for the ineffective performance. However, the symmetrical



(a) Physical Setup



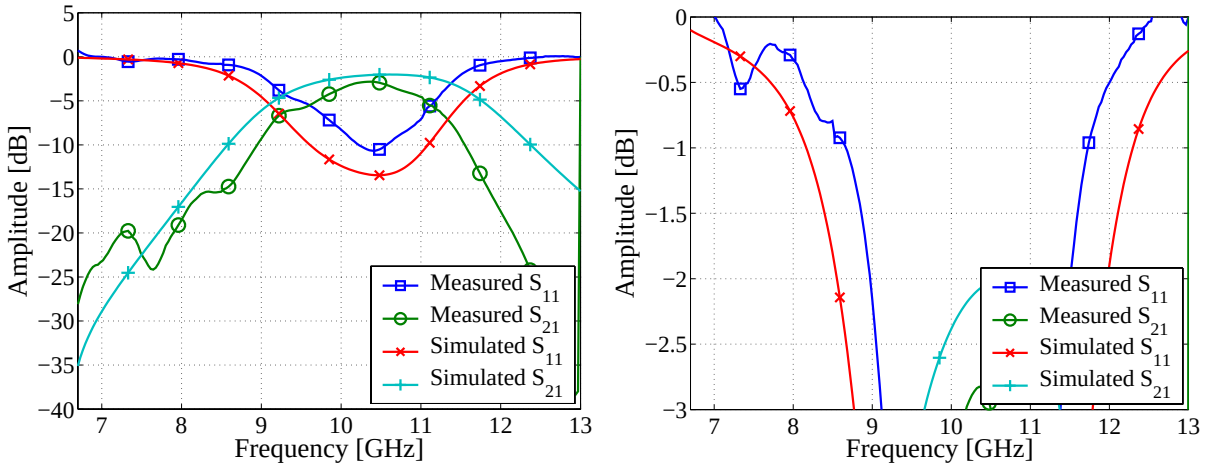
(b) Lumped Element Feed Line Model

Figure 6.25: Vertical-Feed Two Diode Design (Dimensions in Appendix B)

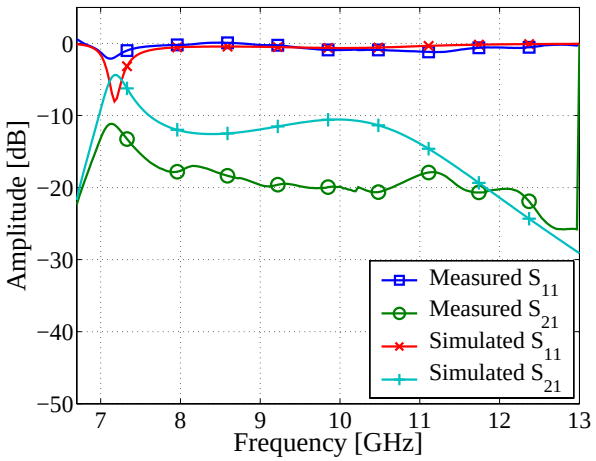
layout of the two-diode setup does not solve the problem. The vertical feed line seems to be the main problem in the topology. Time limitations did not allow further investigation of the problem. The poor filter characteristics could possibly be partially attributed to energy escaping at some point in the structure.

6.4 Conclusion

Various diode mounting topologies have been presented and implemented in two instances of the first order switch. An optimal topology, presented in Sec. 6.3.3, with horizontal-ground horizontal-feed air-gap structure allows simple in-situ tuning of the resonant frequency of the structure, employing ground and feed lines entering through the narrow walls of the waveguide, perpendicular to the electric field orientation. The design achieves a switch fractional bandwidth of 15% in the 15% BW structure, with 22 dB reflection coefficient and 0.8 dB insertion loss when filtering, and 18 dB isolation and 1.1 dB reflection loss when limiting; and achieves a switch fractional bandwidth of 25.5% in the 25%



(a) Filter



(b) Limiter

Figure 6.26: Measurement vs. Theory

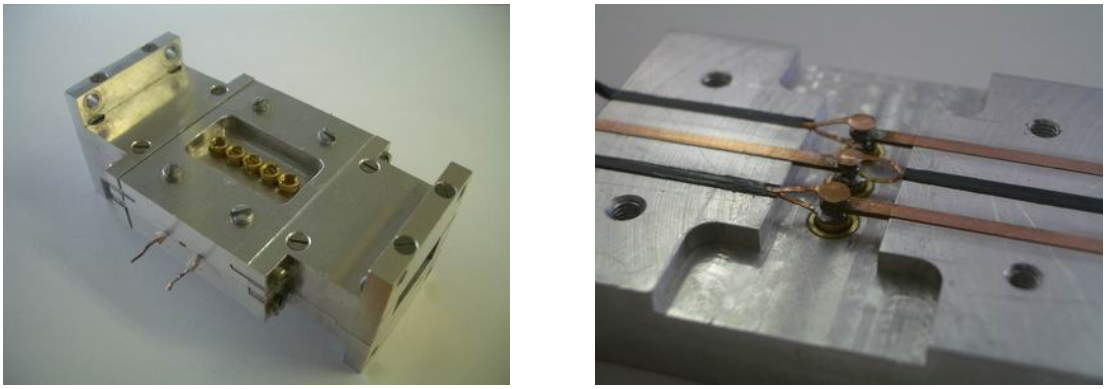
BW structure, with 15 dB reflection coefficient and 1.53 dB insertion loss when filtering, and 24.4 dB isolation and 0.913 dB reflection loss when limiting. Improved isolation conditions are anticipated with a higher order switch design, and results of a third order implementation are presented in Chapter 7.

Chapter 7

Third Order Switch Design

7.1 Introduction

The first order horizontal-ground horizontal-feed air-gap design in Chapter 6 achieves 24.4 dB isolation over the entire measured frequency band between 6.7 GHz and 13 GHz. A set of specifications for a practical X-band switch is given in Table 7.1. With a specified maximum input power of 4.5 kW, the maximum leakage signal during active limiting may not exceed 150 mW, requiring an active isolation of 44.77 dB. To obtain this level of attenuation, a third order switch is designed, incorporating a total of six diodes in three *Horizontal-Ground Horizontal-Feed Air-Gap* diode mounts. The addition of junction tuning rotors on the input and output of the switch results in a fifth order filter structure. The prototype is shown in Fig. 7.1.



(a) Complete Switch (b) Internal Feeds

Figure 7.1: Third Order Switch Prototype

CHARACTERISTIC	CONDITIONS	MIN	MAX	UNITS
POWER SPECIFICATIONS	IN BAND			
FREQUENCY	At high power	8.5	10.5	GHz
FREQUENCY	At receive power	8.5	10.5	GHz
PEAK POWER	Active Mode		4500	W
INSERTION LOSS				
HIGH POWER BAND			2.2	dB
RECEIVE BAND			2.2	dB
AMPLITUDE FLATNESS		±0.2		dB
LEAKAGE POWER				
FLAT LEAKAGE	Active Mode	150		mW
VSWR				
SOURCE	Looking to antenna	1.5:1		
LOAD		2.5:1		

Table 7.1: X-Band Switch Specification

The mechanical construction drawing of the third order prototype is shown in Fig. 7.2.

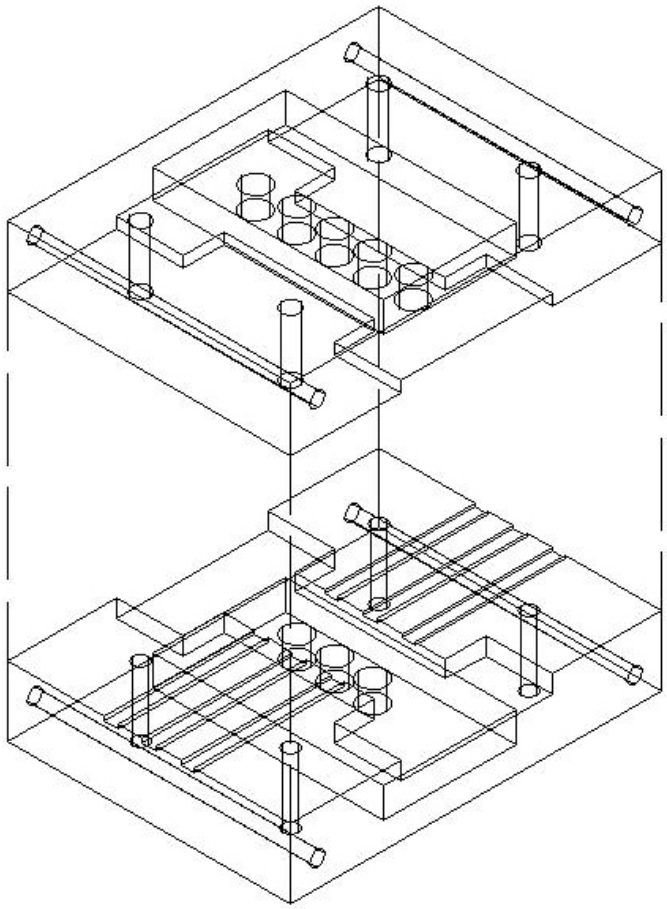


Figure 7.2: Construction Drawing Of Third Order Switch Prototype

7.2 Design and Simulation versus Measurement

Accurate models of diode mounts, as shown in Fig. 6.20, evanescent mode guide sections, as shown in Fig. 4.9 and junctions between evanescent mode and propagating guide sections, as shown Fig. 4.13, are used in the implementation of a third order switch model in AWR Microwave Office. Measured data from first order filter and switch structures is used to build up lumped element models of the various sub-structures in the design, as shown in Fig. 7.3. Instead of using classical design, an optimized approach is followed. Accurate AWR model values have been determined for all the mentioned sub-structures. Parameters which may be optimized include evanescent guide lengths ℓ, mount capacitances C_G, and junction capacitances C_J. The third order switch is tuned by hand in AWR Microwave Office through variation of these parameters, for optimal filter and limiter performance.

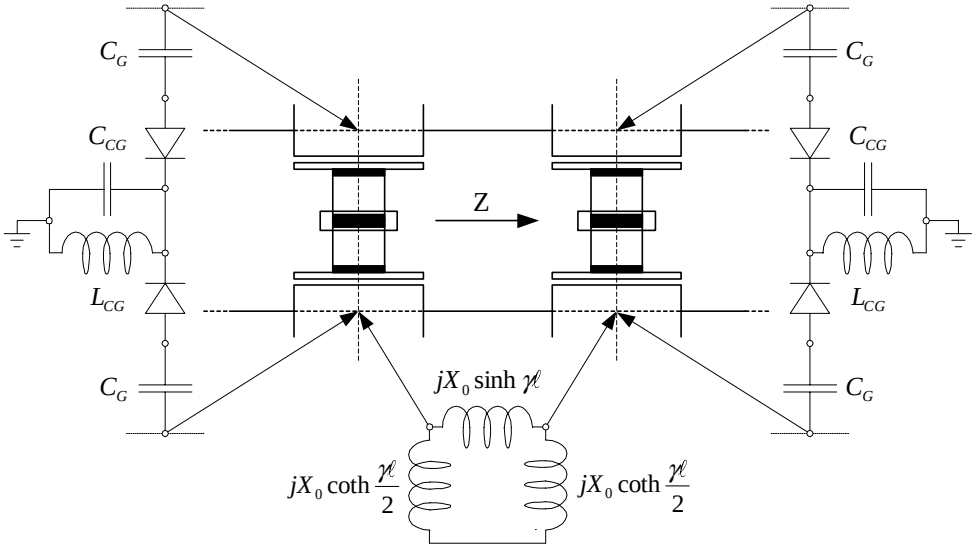


Figure 7.3: Lumped Element Sub-Models In Physical Structure

The reference plane for the diode mount model is chosen at the centre of the mount. This allows the lengths used in the AWR Microwave Office lumped element model to be implemented in the physical structure without adjustment. This is an attractive feature, allowing fast, accurate designing in a linear solver environment with resulting direct physical dimensions. The third order switch achieves the desired switch fractional bandwidth of 21%, with 15.73 dB reflection coefficient and 1.23 dB insertion loss, with a ± 0.155 dB amplitude flatness, when filtering, and 62 dB isolation and 1.29 dB receive loss when limiting, as shown in Fig. 7.5. The switch specifications of Table 7.1 and are indicated by the solid black lines in Fig. 7.5. Fig. 7.4 shows the complete AWR Microwave Office third order switch model.

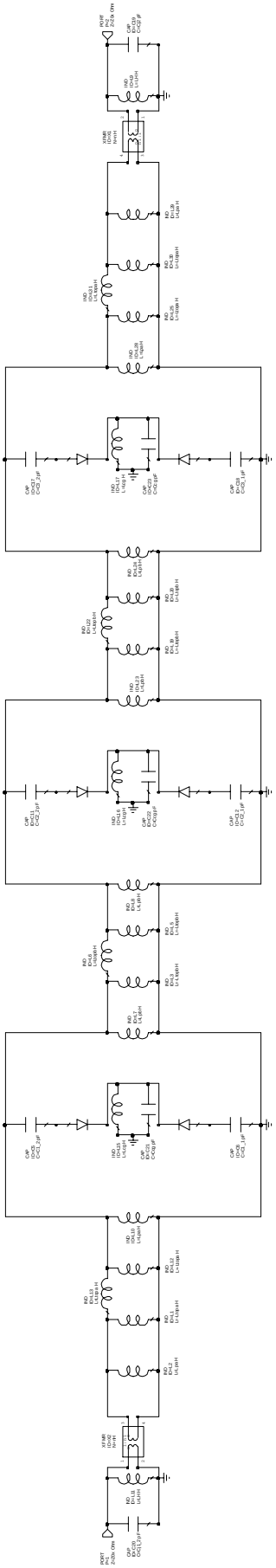


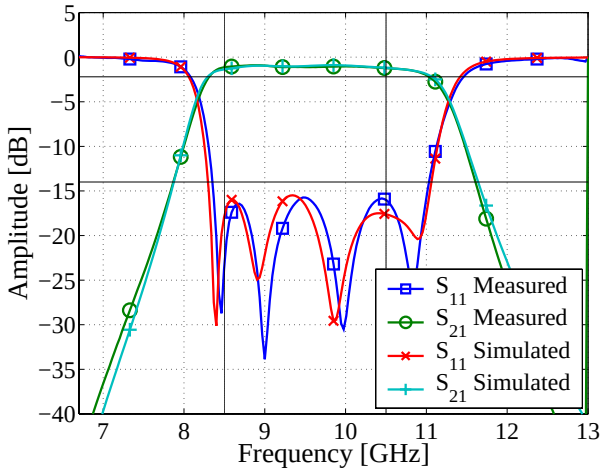
Figure 7.4: Complete AWR Microwave Office Third Order Switch Model

As Fig. 7.5 indicates, all low power specifications are achieved. The complete S-parameter measurements are shown in Fig. 7.6. The output reflection coefficient when filtering is measured as 14.84 dB and the receive loss when limiting is measured as 0.85 dB. The symmetrical nature of the structure is clearly displayed, with almost identical reflection and transmission responses at the switch input and output.

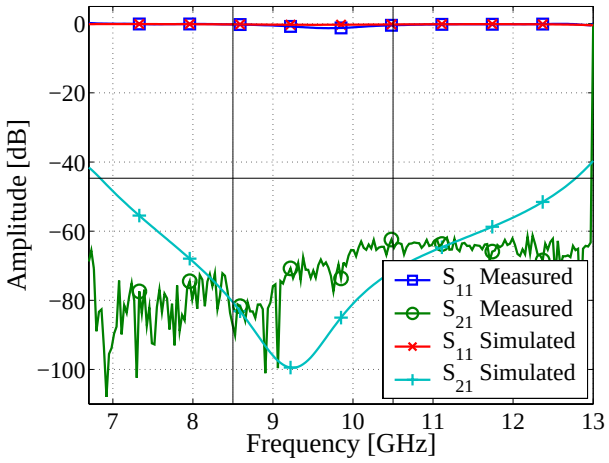
7.3 Conclusion

The developed evanescent mode PIN diode and mount model is effectively used in the design of a tunable third order switch in AWR Microwave Office, verified by measurement. The simulation of the original filter response prior to measurement is adjusted to fit the measured data more accurately, by varying only the tunable capacitances C_G, and junction capacitances C_J.

The final parameter of interest is the power handling capability of the proposed switch. This is discussed next.

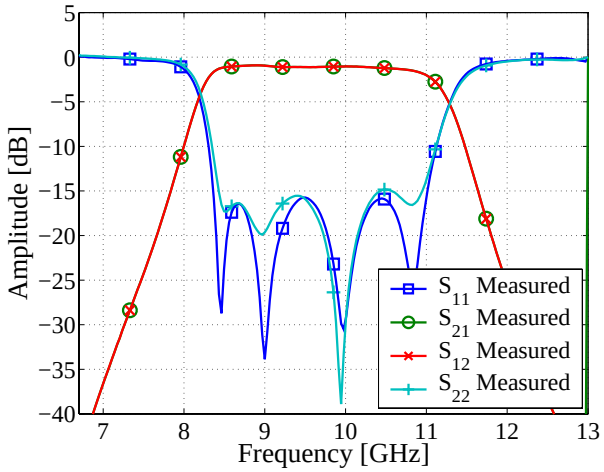


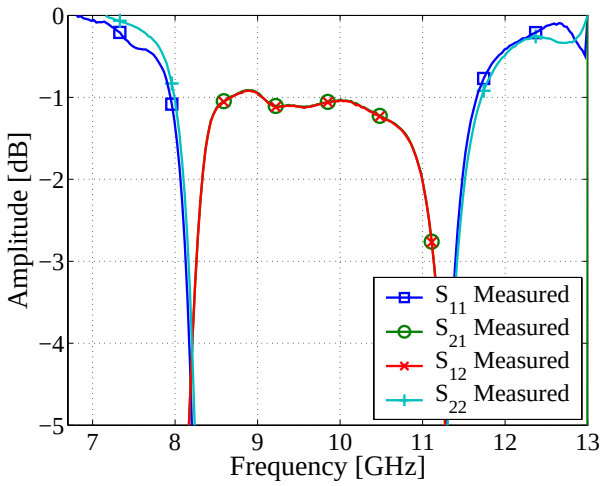
(a) Filter



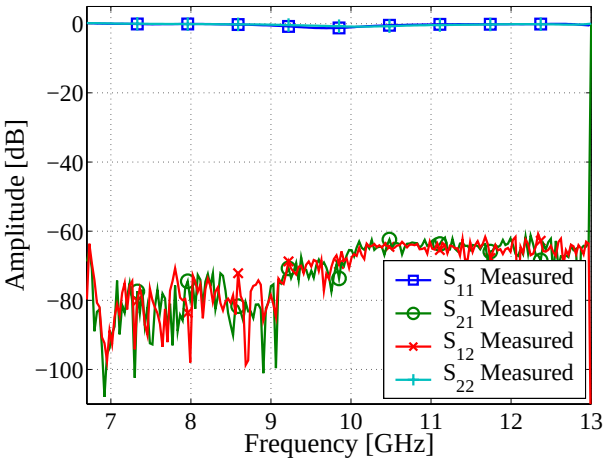
(b) Limiter

Figure 7.5: Measurement vs Theory





(a) Filter



(b) Limiter

Figure 7.6: Complete Measured S-Parameters

Chapter 8

Power Handling

8.1 Introduction

With all the low power specifications achieved in Chapter 7 in terms of S-parameters, the focus of this chapter is to test the high power handling ability of the designed switches. The design objective is shown in Table 8.1.

CHARACTERISTIC	CONDITIONS	MIN	MAX	UNITS
POWER SPECIFICATIONS	IN BAND			
FREQUENCY	At high power	8.5	10.5	GHz
PEAK POWER	Active Mode		2000	W
PULSE WIDTH			50	μs
DUTY			10	%
AVERAGE POWER			200	WATTS
PRF		1	20	kHz

Table 8.1: Switch Power Specification

Possible reasons for switch failure with high power input signals are identified as overheating PIN diodes, as well as gap sparking. The latter occurs when E-fields in excess of 3000 V/mm at sea-level are exceeded between two points in the structure. To evaluate the heating effects, a thermal model for the Micrometrics MMP7067 PIN diode and mount topology is developed from data and measurements.

As thermal models for specific diodes are mostly limited to a prediction of the average thermal resistance θ_{AVE}, the construction of this model constitutes a fundamentally important part of this discussion. The switch was successfully tested up to a peak input power level of 4 kW at 9.5 GHz, with a 24μs pulse width at 5% duty cycle. Note that the high power pulse characteristics were determined by the limits of the TWT amplifier

used in the measurement.

The reflective nature of the designed switch is displayed in the power flow diagram of Fig. 8.1, where P_{IN} is the maximum input power to the switch, P_R is the reflected power, P_D is the dissipated power within the switch and P_{OUT} is the leakage power at the output port of the switch.

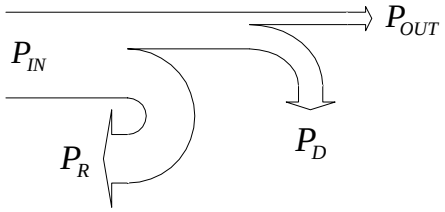


Figure 8.1: Power Flow of Reflective Switch

The dissipated power P_D, is a measure of the power dissipated in the diode branches. An AWR Microwave Office simulation of the currents in the third order switch presented in Chapter 7 is shown in Fig. 8.2, for an average input power level of 405 Watt, chosen to dissipate the maximum allowable average PIN power of 12.5 Watt, as specified by the manufacturer.

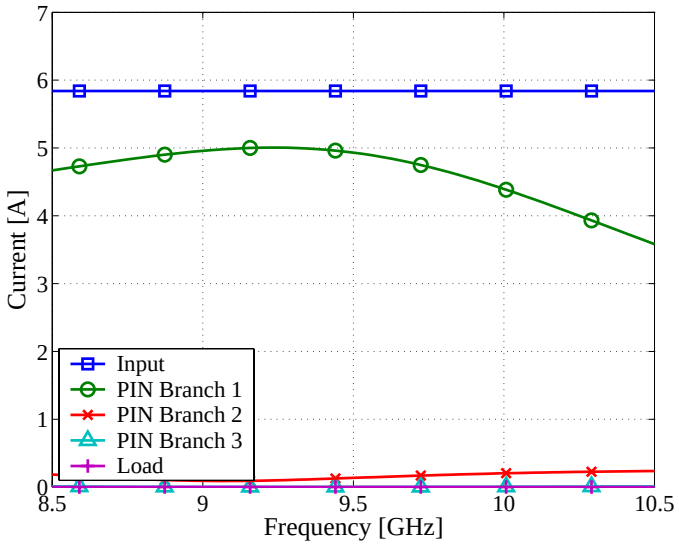


Figure 8.2: AWR MWO Current Distribution In Diode Branches Of Reflective Switch

As shown, the current through PIN Branch 1 is a factor of 20 higher than that through the second diode branch. The bulk of the dissipated power is thus absorbed by the first branch, in a ratio of 400:1 with respect to the second branch.

To investigate the heating of the diodes, it is therefore only necessary to monitor the

temperature rise of the first diode in the chain. The relationship between diode temperature and diode DC voltage is exploited for this measurement as follows: A low power signal (16 Watt in this case) is applied to the input of the switch and the DC voltage across diode 1 is monitored. To determine exactly how the measured voltage relates to the junction temperature of the diode, the voltage-temperature relationship is measured in a calibrated oven in Sec. 8.2.

The other reason for switch failure is the occurrence of gap sparking. A CST Microwave Studio simulation of a first order switch prototype is used to investigate the E-field levels in the structure. The E-field distribution inside the switch at an arbitrary frequency of 9.9 GHz, as shown in Fig. 8.3, shows the highest electric field concentration at the input junction rotor, explained by the reflective nature of the switch. The propagation axis and broad wall dimension of the waveguide is indicated by z and a, respectively.

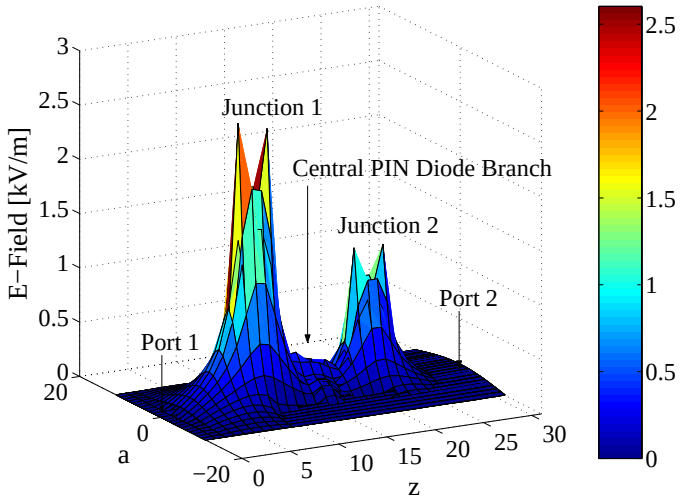


Figure 8.3: Simulated E-Fields in CST

To determine the frequency of the highest electric field concentration at the input junction rotor, E-fields at the rotor are plotted versus frequency from 8.5 GHz to 10.5 GHz at 100 MHz intervals, as shown in Fig. 8.4.

The highest E-field concentration is found at 9.5 GHz, with a level of 45 kV/m (or 45 V/mm) for an input power of 1 Watt_{RMS}. The peak power handling limit, P_P, due to gap sparking is calculated to be

$$P_P = \left(\frac{3000}{45}\right)^2 \times \left(1 \cdot \sqrt{2}\right) = 6.28\text{kW}.$$

This theoretical upper power handling limit due to gap sparking, is higher than the typical power specifications of a switch, as indicated in Table 8.1.

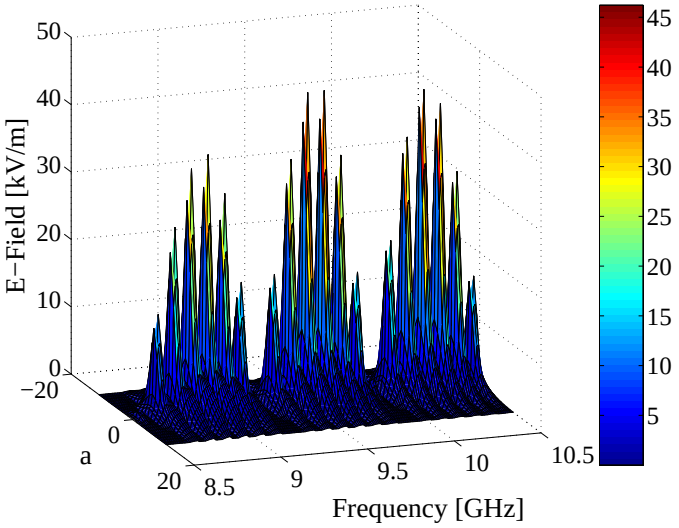


Figure 8.4: Simulated E-Field Of Input Junction Rotor Versus Frequency

In order to determine the temperature rise in the diode junction at high input power levels, the voltage change over the junction is measured. The precise relationship between junction temperature and voltage is determined in Sec. 8.2.

8.2 Temperature Calibration

To relate the diode forward voltage V_F to junction temperature T_J, a temperature calibration procedure is performed. The entire switch structure, complete with PIN diodes in their mounting structure, is placed in a temperature-calibrated oven. Sensors of a digital thermometer, monitoring the temperature to a tenth of a degree accuracy, are placed inside the switch, making contact with the waveguide walls adjacent to the diode mount. After each step in oven temperature, time is allowed before measurement, to allow the temperature to stabilize and to allow the junction temperature T_J to change to the oven temperature. A stable environment is defined as one where there is no change in thermometer and oscilloscope readings versus time. Temperature intervals are approximately 5°C. The DC forward voltage is sampled at the various temperatures at a fixed diode forward current of 150 mA, which is the value used when switching high power signals. The heat dissipation produced by this bias current in the junction and associated increase in junction temperature is therefore kept constant. The complete setup is shown in Fig. 8.5.

The measured PIN forward voltage V_F, versus junction temperature T_J, is shown in Fig. 8.6. The mV/°C value versus junction temperature T_J, is calculated from the direct

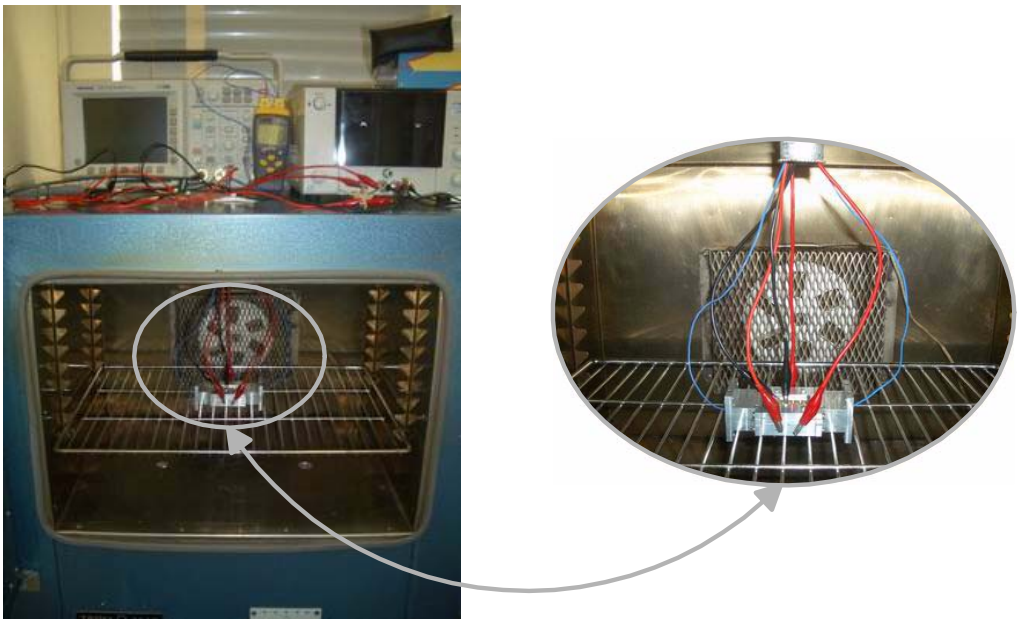
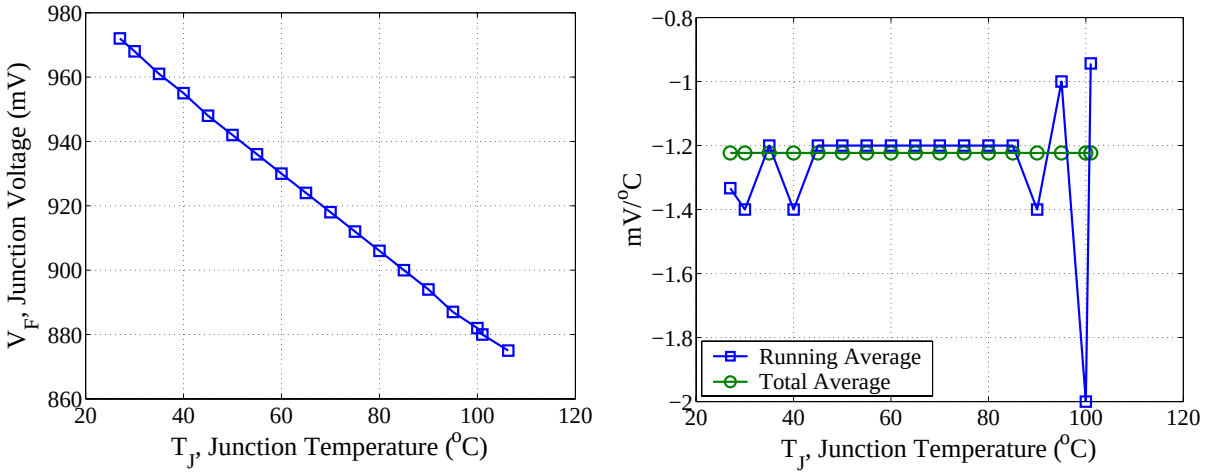


Figure 8.5: Temperature Calibration Setup

measurement. The measured mV/°C remains relatively constant over the temperature range, yielding an average value of -1.23 mV/°C. The value obtained compares very well to the typical value plot of White [4, p.105], where -1.28 mV/°C is obtained for a forward current of 100 mA. Note that this is quite different from the general figure of -2 mV/°C normally used at low bias currents.

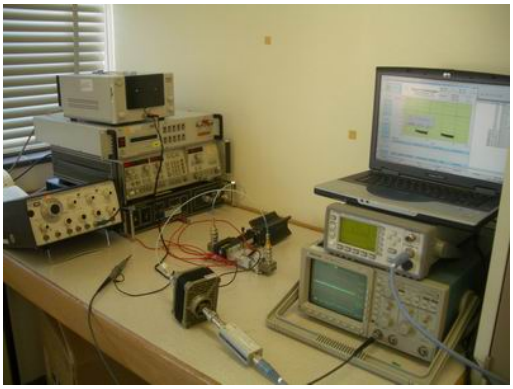


(a) V_F vs. T_J (b) mV/°C vs. T_J

Figure 8.6: Temperature Calibration Results

8.3 Low Power Measurements

8.3.1 Measurement Setup



(a) Complete Setup

(b) Circulator And Switch

Figure 8.7: Low Power Measurement Setup

The low power measurement setup shown in Fig. 8.7 is depicted in block diagram format in Fig. 8.8. A *Wavetek* 20 MHz pulse function generator is used to generate TTL signals of varying duty cycles and pulse lengths. The TTL signal enters the *HP8350B* sweep oscillator with *HP83592A* RF plug-in, which in turn generates the input signal for a *Hughes Aircraft Company 8010H* 10 Watt travelling wave tube amplifier. The output signal of the amplifier runs through a *Trak* X-band waveguide circulator from port 1 to port 2. The developed X-band switch is attached at port 2, with a *IMC 506* resistive load at port 3 absorbing all the reflected power from the switch. A *Tektronix TDS3052B* oscilloscope, calibrated against an *Agilent 34401A* $6\frac{1}{2}$ digit multimeter, is used to measure the forward voltage drop across the PIN diodes. Any signal leaving the output port of the X-band switch is attenuated by an *HP8498A* 30 dB attenuator, before being sampled by an *Agilent E9327A* power sensor connected to an *Agilent E4417A EPM-P Series* power meter. The attenuator is added to ensure that the maximum allowable input power to the power meter is not exceeded. Semi-rigid low-loss cables are used between the amplifier and circulator, as shown in Fig. 8.7(b), to ensure maximum power is delivered from the source to the switch. A transistor current source delivering 150 mA of forward current per PIN diode of branch 1 is designed to ensure that the PIN diode voltage variation caused by increasing RF input power does not lead to PIN diode bias current variation.

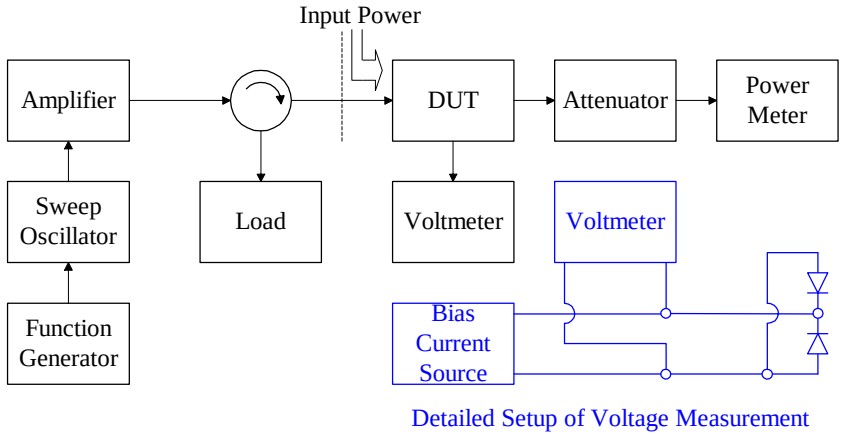


Figure 8.8: Low Power Measurement Diagram

8.3.2 Results

Initial CW measurements at a frequency of 10 GHz are conducted, monitoring the PIN diode forward voltage change versus increasing switch input power. The sweep oscillator power is varied from -5 dBm to 10 dBm, generating a switch input power range, at the plane indicated in Fig. 8.8, between 1.87 Watt and 9.9 Watt. The linear relationship between power and temperature is clearly measured in all three switch instances, namely the first order *Vertical-Ground Horizontal-Feed* switch, as shown in Fig. 8.9, first order *Horizontal-Ground Horizontal-Feed* switch, as shown in Fig. 8.10, and third order horizontal-ground horizontal-feed switch, as shown in Fig. 8.11.

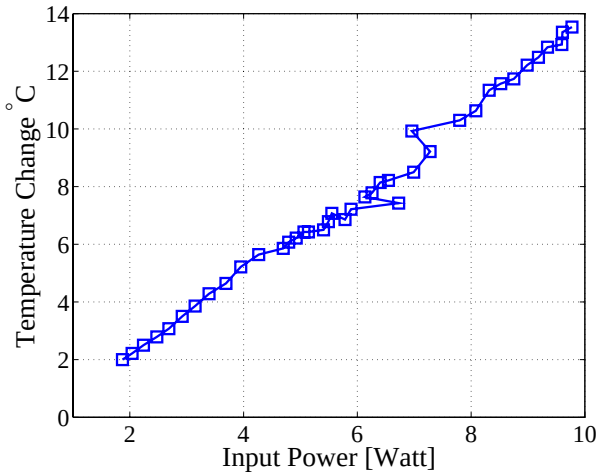


Figure 8.9: Temperature Change, ΔT, Over *Vertical-Ground Horizontal-Feed* PIN Diode Branch In First Order Switch

The power absorption distribution in a switch with more than a single PIN diode branch is verified by measuring the voltage change versus switch input power over all three diode

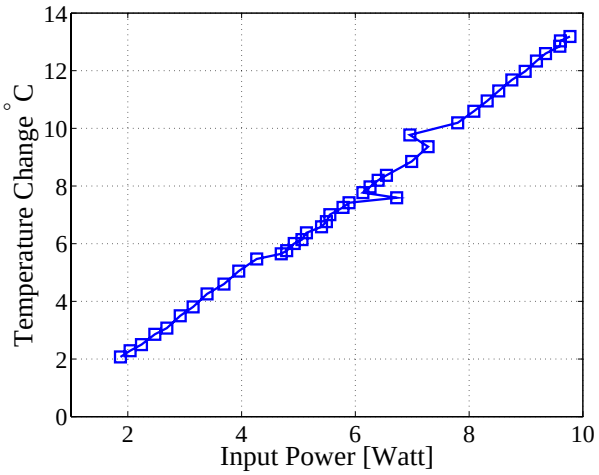


Figure 8.10: Temperature Change, ΔT, Over *Horizontal-Ground Horizontal-Feed* PIN Diode Branch In First Order Switch

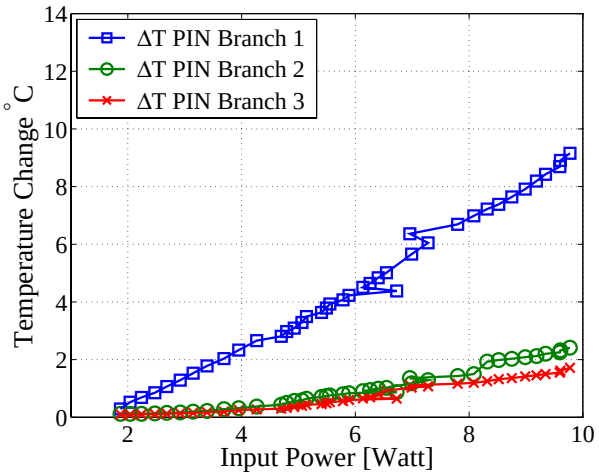


Figure 8.11: Temperature Change, ΔT, Over PIN Diode Branch 1, 2 and 3

branches of the third order switch. Power absorbed by PIN diode branch 1 is greatest, portraying the highest temperature change, ΔT, in the diode junction. With a maximum specified temperature change, $\Delta T_{max} = 150°$ over the PIN diode, the measured linear relationship between temperature and power enables a coarse prediction of maximum CW power handling to be made, using Eq. 8.1.

$$P_{max} = \frac{P_{in(max)} - P_{in(min)}}{T_{max} - T_{min}} \times \Delta T_{max} \tag{8.1}$$

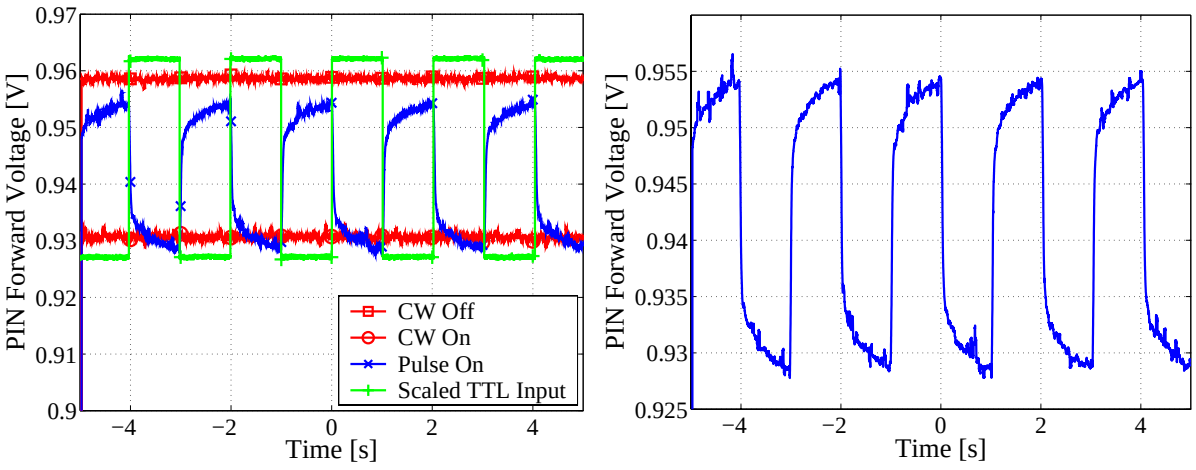
The CW power handling abilities are calculated as 108.3 Watt for the first order *Vertical-Ground Horizontal-Feed* switch, 111.2 Watt for the first order *Horizontal-Ground Horizontal-Feed* switch and 160 Watt for the third order *Horizontal-Ground Horizontal-Feed* switch. As the third order *Horizontal-Ground Horizontal-Feed* design is the topology of choice, pulsed measurements are only performed on this prototype. Furthermore, only the voltage

over the first diode branch is monitored.

Measurements are taken at the maximum available switch input power of 42 dBm with varying pulse widths at 50% and 10% duty cycles. A few points of specific interest can be observed from the graphs in Fig. 8.12 to Fig. 8.20:

- The thermal overshoot, which can be seen with the 50 μs input pulse, is a second order phenomena and is not predicted by the electric circuit analogue of the transient heating thermal model in Sec. 8.5.
- The average temperature change induced by a 10% duty cycle pulse is lower than that of a 50% duty cycle pulse, as expected, resulting in a decreased power handling ability for input signals with high duty cycles. Measurements of several input pulse widths for 50% and 10% duty cycles are shown in Fig. 8.12 to Fig. 8.18, with added CW limits and scaled TTL input signals.
- A number of thermal time constants may be seen in the measured PIN forward voltage curve as the input pulse widths change.
- To determine the relationship between the measured forward voltage curves, multiple curves of varying lengths are overlain, as shown in Fig. 8.19 and Fig. 8.20. As the pulse lengths decrease, shorter sections of the voltage curve are measured.

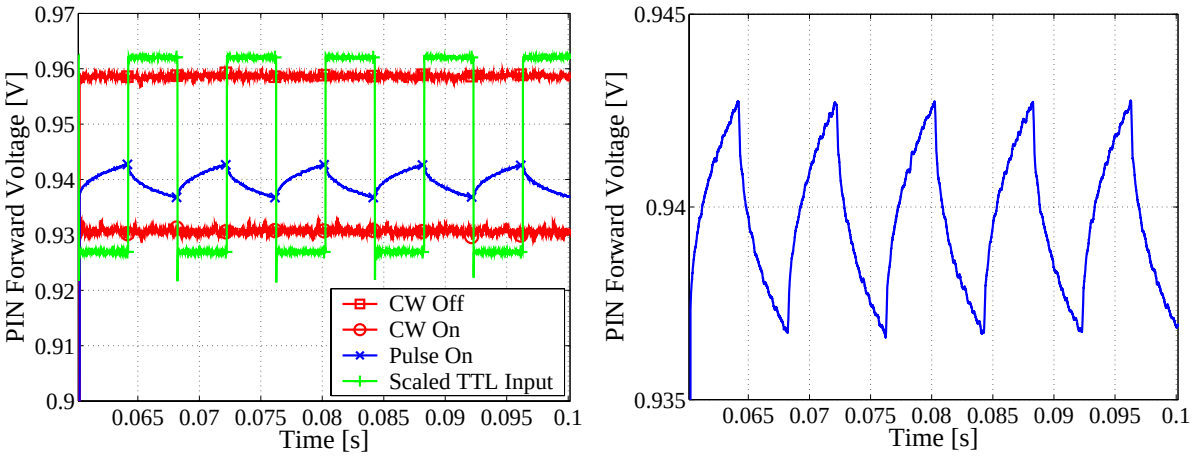
The various thermal time constants of the complete diode mount structure are explained with the aid of the practical PIN diode thermal model in Sec. 8.5.



(a) CW Limits, V_F and Scaled TTL Input

(b) PIN Forward Voltage, V_F

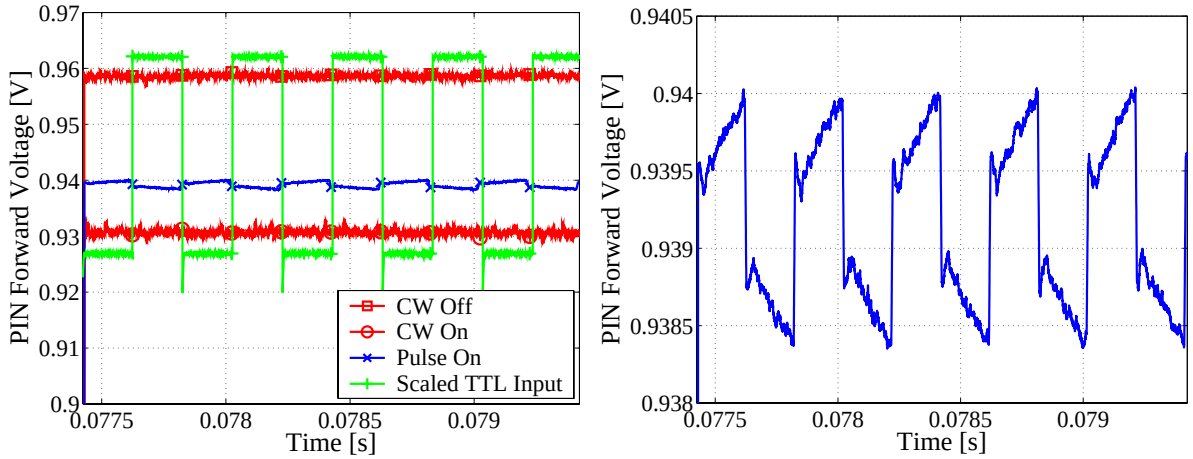
Figure 8.12: 1s Pulse Width, 50% Duty Cycle, 41.97 dBm Input Power: $\Delta V_{PIN(1s,\ 50\%)} = 26$ mV, $\Delta T = 18.57°C$



(a) CW Limits, V_F and Scaled TTL Input

(b) PIN Forward Voltage, V_F

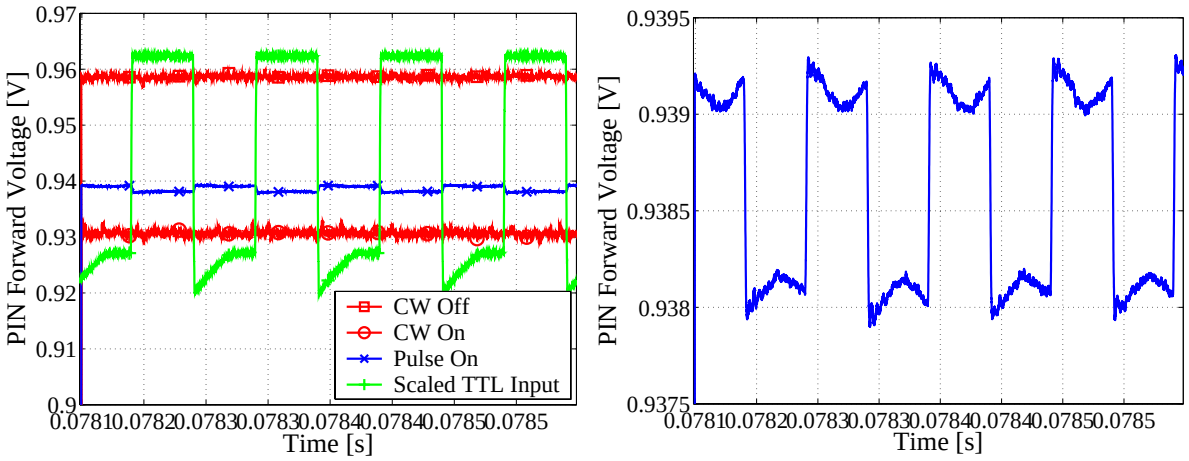
Figure 8.13: 4ms Pulse Width, 50% Duty Cycle, 41.925 dBm Input Power: $\Delta V_{PIN(4ms,\ 50\%)} = 6$ mV, $\Delta T = 4.29°C$



(a) CW Limits, V_F and Scaled TTL Input

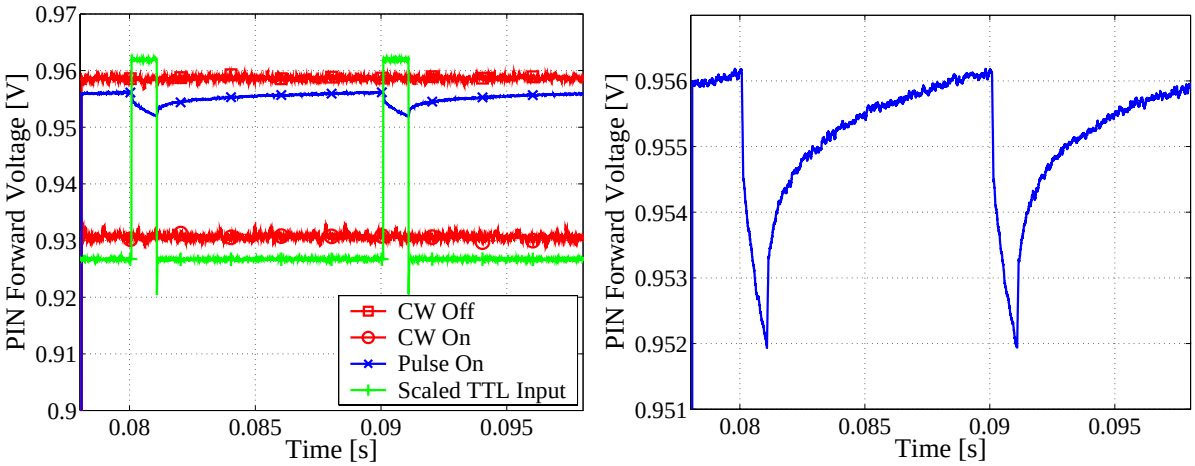
(b) PIN Forward Voltage, V_F

Figure 8.14: 200μs Pulse Width, 50% Duty Cycle, 41.92 dBm Input Power: $\Delta V_{PIN(200\mu s,\ 50\%)} = 1.5$ mV, $\Delta T = 1.07°C$



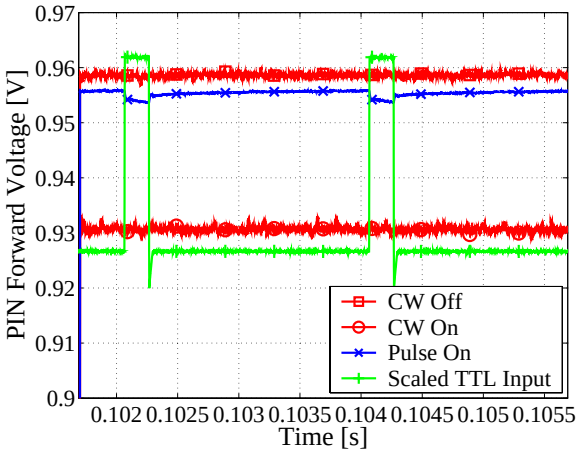
(a) CW Limits, V_F and Scaled TTL Input (b) PIN Forward Voltage, V_F

Figure 8.15: 50μs Pulse Width, 50% Duty Cycle, 41.915 dBm Input Power: $\Delta V_{PIN(50\mu s,\ 50\%)} = 1.1$ mV, $\Delta T = 0.786°C$

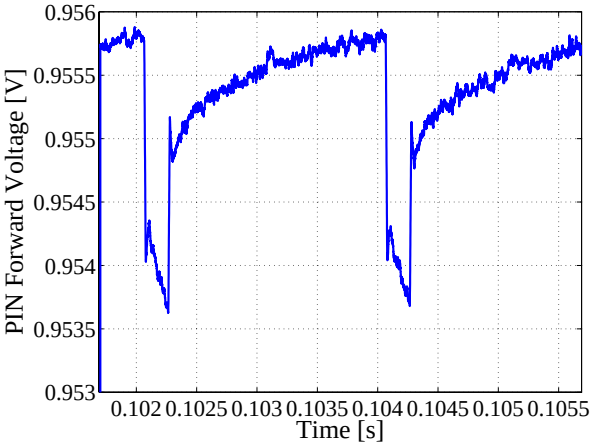


(a) CW Limits, V_F and Scaled TTL Input (b) PIN Forward Voltage, V_F

Figure 8.16: 1ms Pulse Width, 10% Duty Cycle, 41.962 dBm Input Power: $\Delta V_{PIN(1ms,\ 10\%)} = 4.1$ mV, $\Delta T = 2.93°C$

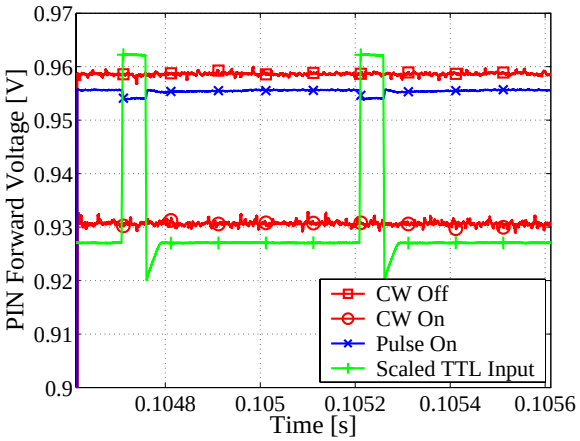


(a) CW Limits, V_F and Scaled TTL Input

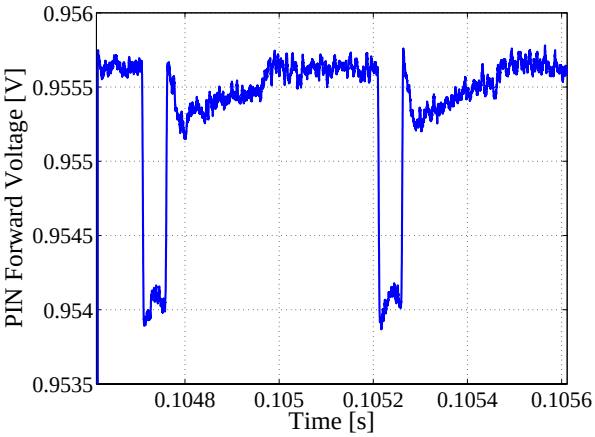


(b) PIN Forward Voltage, V_F

Figure 8.17: 200μs Pulse Width, 10% Duty Cycle, 41.97 dBm Input Power: $\Delta V_{PIN(200\mu s,\ 10\%)} = 2.1$ mV, $\Delta T = 1.5$ °C

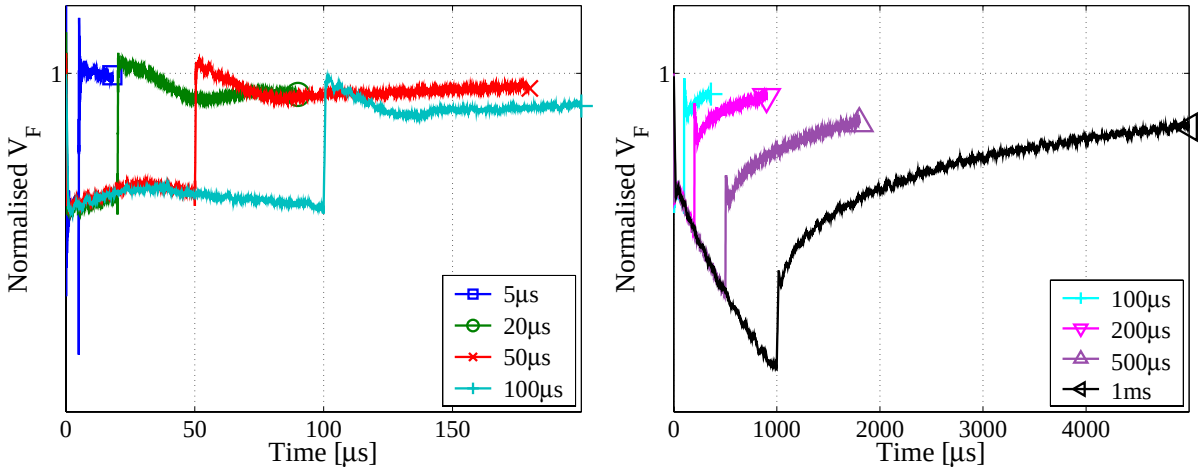


(a) CW Limits, V_F and Scaled TTL Input



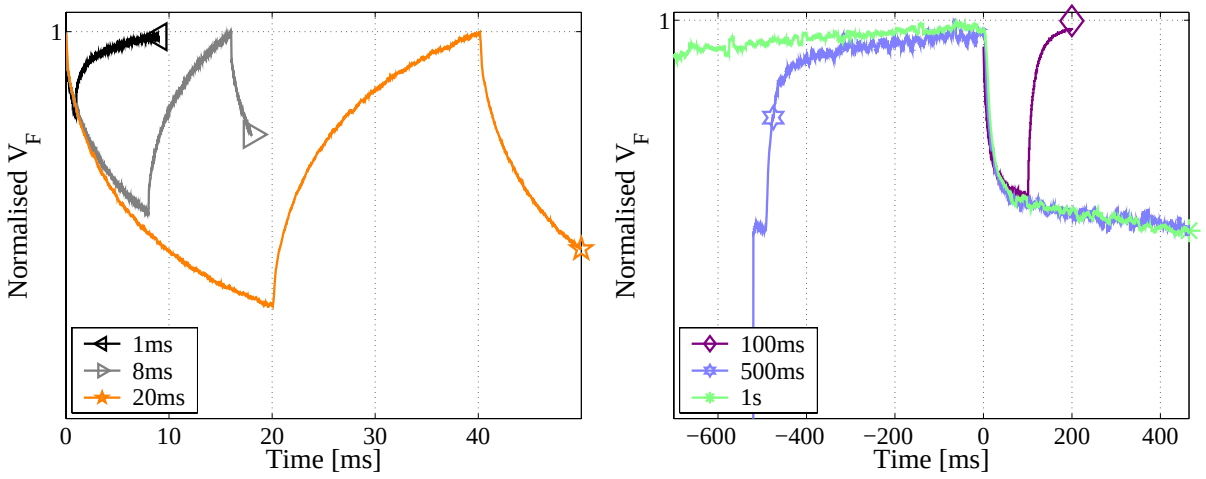
(b) PIN Forward Voltage, V_F

Figure 8.18: 50μs Pulse Width, 10% Duty Cycle, 41.975 dBm Input Power: $\Delta V_{PIN(50\mu\ s,\ 10\%)} = 1.5$ mV, $\Delta T = 1.07$ °C



(a) 5μs to 100μs (b) 100μs to 1ms

Figure 8.19: Overlain Normalised PIN Forward Voltage Curves Of Varying Pulse Widths



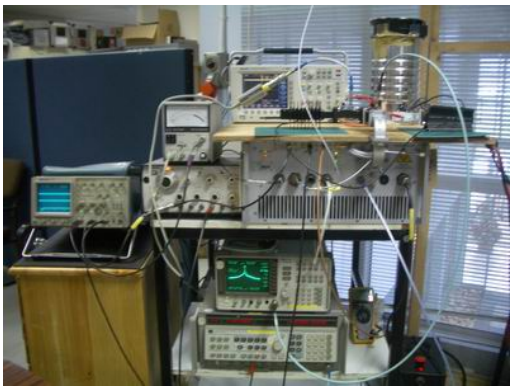
(a) 1ms to 20ms (b) 100ms to 1s

Figure 8.20: Overlain Normalised PIN Forward Voltage Curves Of Varying Pulse Widths

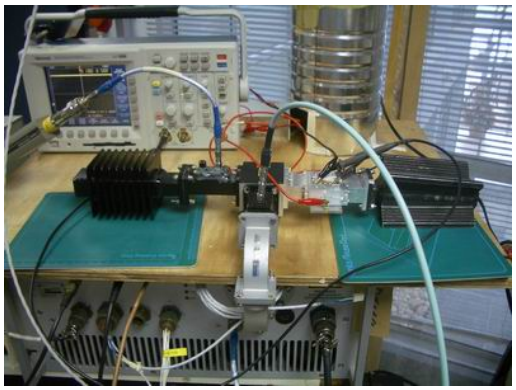
8.4 High Power Measurements

8.4.1 Measurement Setup

The high power measurement setup is shown in Fig. 8.21. A TWT amplifier, which is capable of generating peak power levels of 8 kW for a maximum pulse width of 25μs and maximum duty cycle of 5%, is used for the measurement. As in the low power measurement setup, the output signal of the amplifier runs through a circulator from port 1 to port 2. A directional coupler is used to monitor the peak input pulse level entering port 1, on a spectrum analyzer. The switch is attached at port 2. The peak reflected power from the switch is monitored by an additional directional coupler at port 3, using a power meter with a peak detector unit, followed by a resistive load to absorb the power.



(a) Complete Setup

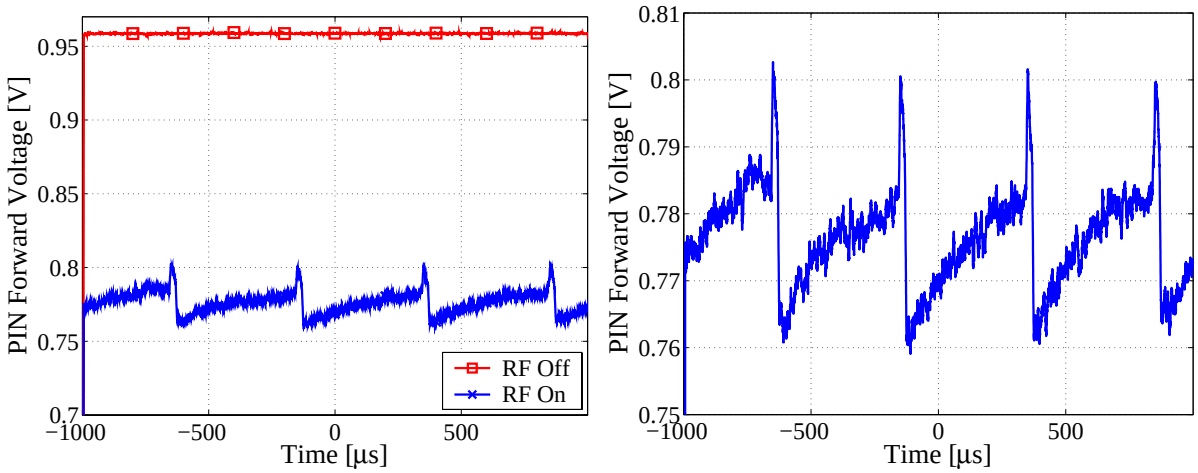


(b) Directional Couplers, Circulator, Switch and Resistive Loads

Figure 8.21: High Power Measurement Setup

8.4.2 Results

The switch successfully reflected an input pulse level of 2 kW at 8.5 GHz, 9.5 GHz and 10.5 GHz, for a 24μs pulse width at 4.8% duty cycle. The PIN diode forward voltage measured over the diode with an input pulse peak power level of 2 kW at 9.5 GHz, is shown in Fig. 8.22. The shown voltage levels imply a maximum temperature of 140°C and an average temperature of roughly 130°C. The switch also successfully reflected a 4 kW peak input power level for the same pulse characteristics at 9.5 GHz.



(a) RF Off and RF On

(b) PIN Forward Voltage, V_F

Figure 8.22: 24μs Pulse Width, 4.8% Duty Cycle, 2 kW Input Power

8.5 Practical PIN Diode Thermal Model

No thermal model or PIN diode construction information is available for the Micrometrics MMP7067 PIN diode. To predict the junction temperature behaviour of the diodes used in the switch under high power conditions, a model is developed by using manufacturers data and the power measurements. The only useful parameters which are specified by the manufacturer for determining the thermal model of the PIN diode, are listed in Table 8.2.

PARAMETER	NAME	VALUE	UNIT
Thermal Impedance	θ_{JC}	12	°C/W
Minimum Thermal Time Constant	τ_T	50.4	μs
Chip Thickness		0.254 ± 0.1	mm
CS32 Cylindrical Package Height		1.02 - 1.27	mm
CS32 Cylindrical Package Diameter		1.3 - 1.4	mm

Table 8.2: Micrometrics MMP7067 PIN Diode Parameters

The steady state temperature difference between the junction and heat sink due to continuous power dissipation P_D, is limited to 150°C before overheating will incur diode failure. Using Eq. 3.6, the maximum continuous power dissipation is P_D = 12.5 W for the MMP7067 PIN diode, with average thermal resistance $\theta_{AVE} = \theta_{JC}$ = 12°C/W. With the specified minimum thermal time constant, τ_T = 50.4 μs, the I-region heat capacity is calculated to be HC = 4.2 μJ/°C, using Eq. 3.10. With a maximum pulse length of 50 μs in the application of the proposed PIN waveguide switch, the temperature rise in a pulsed power application with low average power is limited to a maximum I-region temperature

rise above the heat sink of

$$\begin{aligned} \Delta T_M &< P_D \cdot t/HC \\ &= 12.5 \cdot \frac{50\mu}{4.2\mu} \\ &= 148.81\ ^\circ C, \end{aligned}$$

using Eq. 3.9. The more realistic temperature rise given by Eq. 3.12, outlined in Sec. 3.4, is calculated as

$$\begin{aligned} \Delta T_M &= P_D \cdot \theta_{AVE} \left[1 - e^{-t/\tau_T}\right] \\ &= 12.5 \times 12 \left[1 - e^{-50\mu/50.4\mu}\right] \\ &= 94.38\ ^\circ C, \end{aligned}$$

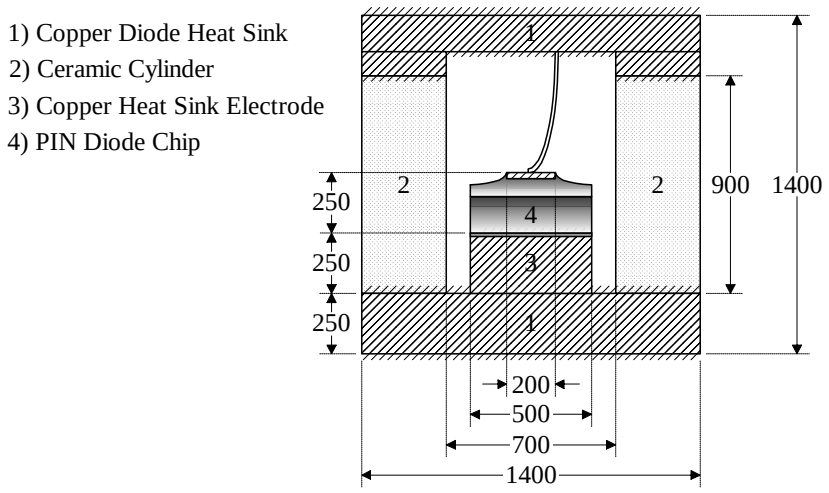
which is considerably lower than the maximum allowable I-region temperature change of 150 °C. At the maximum pulse width of 50 μs, the interpulse period is at least 500 μs at a PRF of 2 kHz. The junction temperature between pulses will theoretically cool down to a temperature of

$$\begin{aligned} T_J &= T_S + \Delta T_M e^{-t_{interpulse}/\tau_T} \\ &= 25 + 94.38 e^{-500\mu/50.4\mu} \\ &= 25.0046\ ^\circ C, \end{aligned}$$

as predicted by Eq. 3.13, therefore giving no cause for concern with regards to thermal runaway of the PIN diode. The calculated estimates of junction temperature represent upper bounds, subject to the assumption that the I-region temperature is uniform throughout. The actual T_J is likely to be lower [4], and may be predicted with the theoretical thermal model of Sec. 3.4.

Following these theoretical predictions of junction temperature behaviour, the thermal model of the MMP7067 PIN diode is developed. Since the parameters of the thermal model depend on the physical construction of diode, the PIN diode package is carefully disassembled to measure dimensions of the chip and package using a travelling microscope. The practical PIN diode construction is shown in Fig. 8.23.

The various parts of the PIN diode and mounting structure are shown in Fig. 8.24. The PIN diode mount includes the central ground, G, of the *Horizontal-Ground Horizontal-Feed Air-Gap* Design implemented in the final switch, extended between the PIN diode casings and effective heat sink (or waveguide wall) of the structure.



(a) MMP7067 Construction, μm Units

Figure 8.23: Micrometrics MMP7067 Constructional PIN Detail

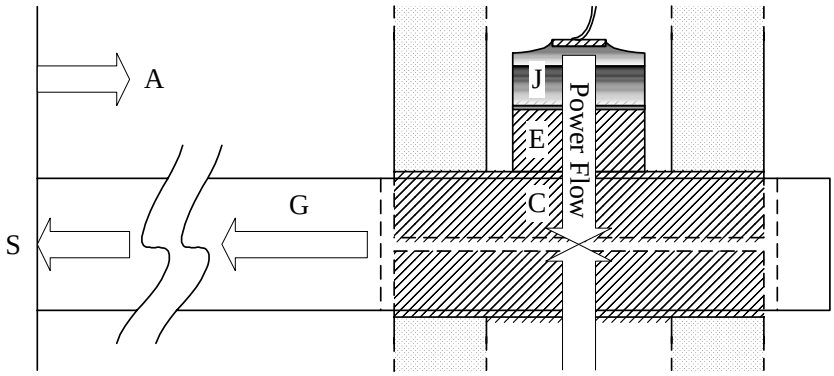


Figure 8.24: Construction Of PIN Diode and Mount

The proposed electric circuit analogue of the transient heating thermal model, shown in Fig. 8.25, is an adaptation of the model proposed by White [4] in Chapter 3. The model is simplified to exclude solder joints, peripheral silicon and top weight, and additions are made to ensure correct average temperatures within the structure. The copper central ground adds an additional thermal capacitance C_G and thermal resistance R_{GS} to the electric circuit analogue of only the PIN diode. Thermal resistance R_{JE} represents the thermal resistance of the silicon chip, between the junction and the base of the chip. R_{EC}, R_{CG} and R_{SA} refer to the thermal resistances of the heat sink electrode, case/diode heat sink and heat sink to ambient, respectively. Thermal capacitances C_T and C_{JE} represent the specific heat capacity of the I-region, or silicon chip. Capacitance C_T to ground ensures that heat must be supplied to raise the temperature of the entire silicon chip to the temperature of the base of the chip, t°_E. Capacitance $C_{JE} = 1/2C_T$ ensures that further heat is required to raise the average temperature of the silicon chip by another $1/2(t^\circ_J\text{-}t^\circ_E)$ [34]. C_E and C_C are the thermal capacitances of the heat sink electrode and case/diode

heat sink respectively. A single capacitance C_S characterizes the thermal capacitance of the heat sink, assuming that the entire heat sink is at a constant temperature.

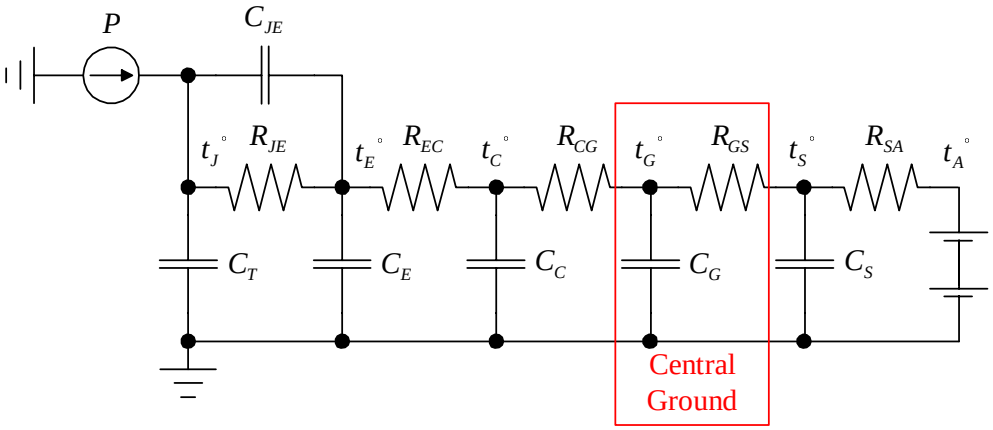


Figure 8.25: Electric Circuit Analogue

Under static conditions, the thermal capacitances are ignored and the average junction temperature, with an average dissipated power of P_D, is given by

$$t_J^\circ = P_D(R_{JE} + R_{EC} + R_{CG} + R_{GS} + R_{SA}) + t_A^\circ, \tag{8.2}$$

while under dynamic conditions, the heat capacities of the circuit must be taken into consideration. Various thermal capacitance and resistance values for the electric circuit analogue are now calculated from manufacturer's data and physical dimensions of the structure. PIN diode data sheet information is used to calculate the thermal capacitance and resistance values of the I-region of the diode. The I-region heat capacity, HC, is calculated from Eq. 3.7 as

$$\mathrm{HC} = \frac{\tau_\mathrm{T}}{\theta_{AVE}} = \frac{50.4\mu\mathrm{s}}{12^\circ\mathrm{C/W}} = 4.2\mu\mathrm{J/^\circ C}, \tag{8.3}$$

where τ_T and θ_{AVE} are specified by the manufacturer. The first values employed in the electric circuit analogue model are therefore

$$\begin{aligned} C_T &= 4.2\mu\mathrm{J/K} \\ C_{JE} &= 1/2\ C_T = 2.1\mu\mathrm{J/K} \\ R_{JE} + R_{EC} &= 12^\circ\mathrm{C/W}. \end{aligned}$$

The remainder of the thermal capacitances and resistances of the PIN diode and mounting structure are calculated with the assumption that individual objects are at a uniform

temperature. The thermal capacitance of an object with density ρ and volume V_b is given by [34],

$$C_T = \rho c_\theta V_b, \tag{8.4}$$

where c_θ is the specific heat capacity of the material. The thermal resistance of an object with length ℓ and area A is given by

$$R_T = \frac{1}{\sigma_e}\frac{\ell}{A}, \tag{8.5}$$

where σ_e is the thermal conductivity of the material. Table 8.3 lists all relevant values of the materials of interest.

Material	Density kg/m^3	Thermal Conductivity W/m·K	Specific Heat Capacity J/kg·K
Aluminium	2700	238	904
Copper	8960	397	394
Silicon	2300	148	750

Table 8.3: Thermal Properties Of Relevant Materials

To calculate the approximate value of R_{JE}, the dimensions of the intrinsic region must be determined. Using I-region heat capacity, Eq. 3.7, and junction capacitance, Eq. 3.1, the junction width W and effective diameter D may be determined. With

$$\text{HC} = \frac{1.4\text{D}^2\text{W}}{\text{cubic centimetre}} = 4.2\ \mu\text{J/°C} \qquad \text{and} \tag{8.6}$$

$$C_J = \frac{\epsilon\pi\text{D}^2}{4\text{W}} = 0.2\ \text{pF}, \tag{8.7}$$

and the relative permittivity of silicon, $\epsilon_r = 11.8$, the width and diameter of the PIN diode junction are calculated as

$$\text{W} = 35.084\ \mu\text{m} \qquad \text{and} \tag{8.8}$$

$$\text{D} = 292.42\ \mu\text{m}, \tag{8.9}$$

indicating a PIN diode with large cross-sectional area with attributed high power handling capability. The known thermal capacitance is re-calculated, validating the dimensional results obtained.

$$\begin{aligned} C_T &= \rho c_\theta V_b \\ &= 2300 \times 750 \times 35.084\mu \times \pi(146.21\mu)^2 \\ &= 4.06\ \mu\text{J/K} \approx 4.2\ \mu\text{J/K} \end{aligned}$$

$$\begin{aligned} R_{JE} &= \frac{1}{\sigma_e}\frac{\ell}{A} \\ &= \frac{1}{148} \times \frac{35.084\mu}{\pi(146.21\mu)^2} \\ &= 3.53\ ^\circ\text{C/W} \\ R_{EC} &= \theta_{AVE} - R_{JE} \\ &= 12 - 3.53 \\ &= 8.47\ ^\circ\text{C/W}. \end{aligned}$$

The copper heat sink electrode is measured to have a diameter of 500 μm and height of 250 μm, as shown in Fig. 8.23. Thermal capacitance and resistance values are calculated to be

$$\begin{aligned} C_E &= \rho c_\theta \mathrm{V_b} \\ &= 8960 \times 394 \times 250\mu \times \pi(250\mu)^2 \\ &= 173.3\ \mu\text{J/K} \\ R_{EC} &= \frac{1}{\sigma_e}\frac{\ell}{A} \\ &= \frac{1}{397} \times \frac{250\mu}{\pi(250\mu)^2} \\ &= 3.2\ ^\circ\text{C/W} \neq 8.47\ ^\circ\text{C/W}. \end{aligned}$$

The calculated thermal resistance value does not agree with results obtained earlier. Therefore, the actual resistance value, R_{EC}, is determined when the complete model is fitted to measured data and optimized to obtain the best model fit.

The next part of the transient thermal model is the diode copper heat sink. Its dimensions include a height of approximately 250 μm and diameter of 1.4 mm, resulting in thermal capacitance and resistance values of

$$\begin{aligned} C_C &= \rho c_\theta \mathrm{V_b} \\ &= 8960 \times 394 \times 250\mu \times \pi(0.7m)^2 \\ &= 1.36\ m\text{J/K} \\ R_{CG} &= \frac{1}{\sigma_e}\frac{\ell}{A} \\ &= \frac{1}{397} \times \frac{250\mu}{\pi(0.7m)^2} \\ &= 0.41\ ^\circ\text{C/W}. \end{aligned}$$

The horizontal ground mounting structure extending from the narrow wall of the waveguide is made of 0.5 mm thick copper shimstock and is a crucial piece of the diode mount.

With a length of 4.65 mm and width of 2 mm, its thermal properties are calculated as

$$\begin{aligned} C_G &= \rho c_\theta \mathrm{V_b} \\ &= 8960 \times 394 \times 4.65m \times 2m \times 0.5m \\ &= 16.4\ m\mathrm{J/K} \\ R_{GS} &= \frac{1}{\sigma_e}\frac{\ell}{A} \\ &= \frac{1}{397} \times \frac{4.65m}{2m \times 0.5m} \\ &= 11.7\ ^\circ\mathrm{C/W}. \end{aligned}$$

All the elements and their respective calculated and physical values are listed in Table 8.4. Physical values indicate optimized calculated values to ensure a good transient fit of the electric circuit analogue on the entire range of measurements.

Element	Calculated	Physical	Unit
C_T	4.2	4.2	μJ/K
C_{JE}	2.1	2.1	μJ/K
R_{JE}	3.53	3.5	°C/W
C_E	173.3	120	μJ/K
R_{EC}	8.47	11	°C/W
C_C	1.36	1.3	mJ/K
R_{CG}	0.41	1	°C/W
C_G	16.4	12	mJ/K
R_{GS}	11.7	13	°C/W
C_S	-	20	mJ/K
R_{SA}	-	20	°C/W

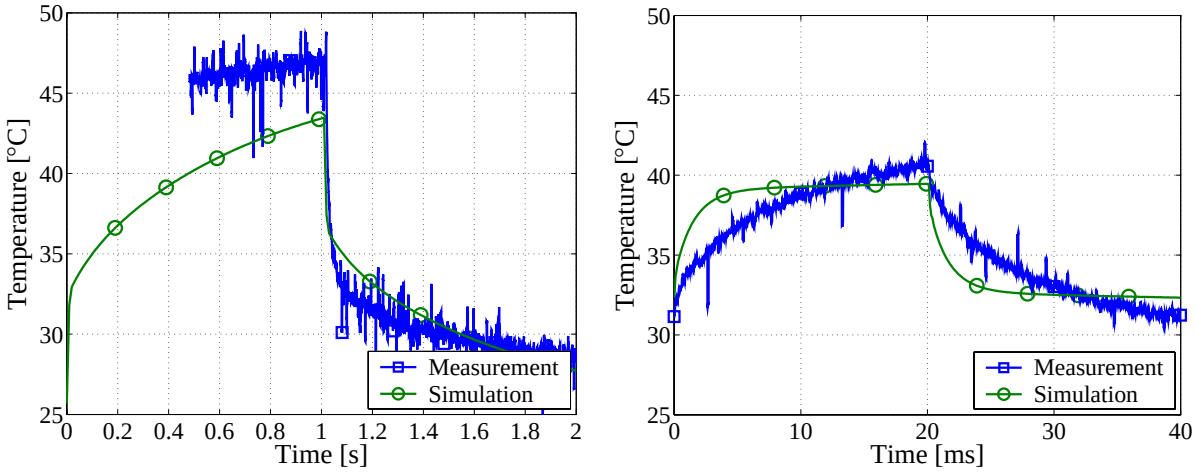
Table 8.4: Calculated and Physical Transient Thermal Model Element Values

Values for heat sink thermal capacitance C_S, and heat sink to ambient resistance R_{SA}, are obtained by optimizing the electric circuit analogue fit on measured data. The relationship between the switch input current and the diode current in PIN branch 1 predicted by the AWR Microwave Office model, as shown in Fig. 8.2, is used to determine the relationship between the switch input power and the power dissipated in the diode. The electric circuit analogue is simulated in Orcad Capture Version 9.2 using PSpice 9.2, and compared to measured data for various pulse widths.

A number of points can be observed from the graphs in Figs. 8.26 to 8.28:

- The thermal model does not predict the thermal overshoot phenomenon.

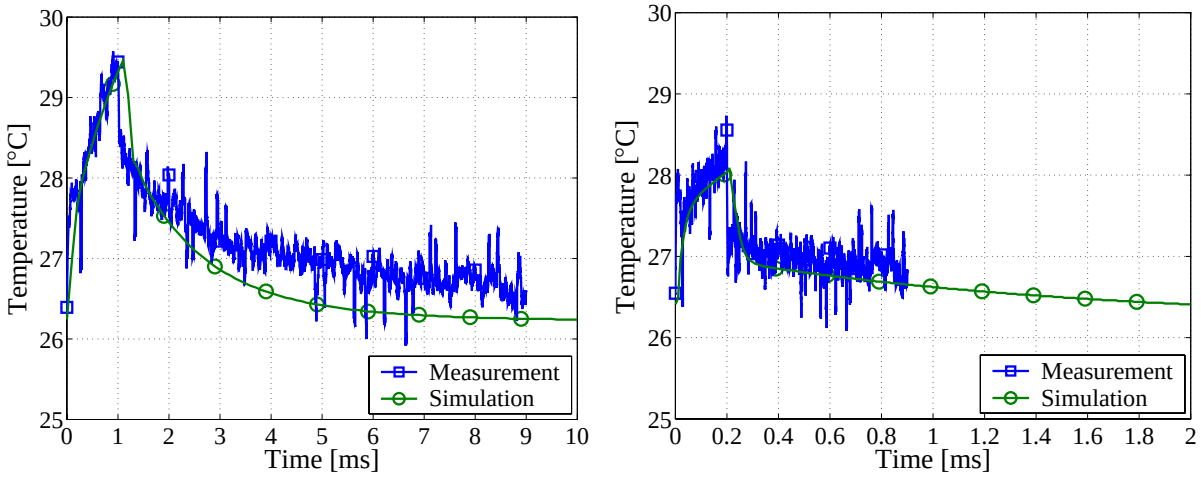
- The thermal time constants of the model agree well with measured time constants at low pulse widths. A more complex model could serve to predict the time constants at increased pulse widths more accurately.
- The thermal model predicts a far greater peak temperature deviation at high power than seen in the measurement. A possible reason might be that the I-region thermal characteristics change at increased temperatures, resulting in an increased thermal time constant and attributed lower peak temperature. A range of high power measurements at varying pulse widths and duty cycles with an increased number of data points in the region of the pulse, could aid to answer this question.



(a) 1s Pulse Width, 50% Duty Cycle, Low Power (Only a section of the pulse was captured)

(b) 20ms Pulse Width, 50% Duty Cycle, Low Power

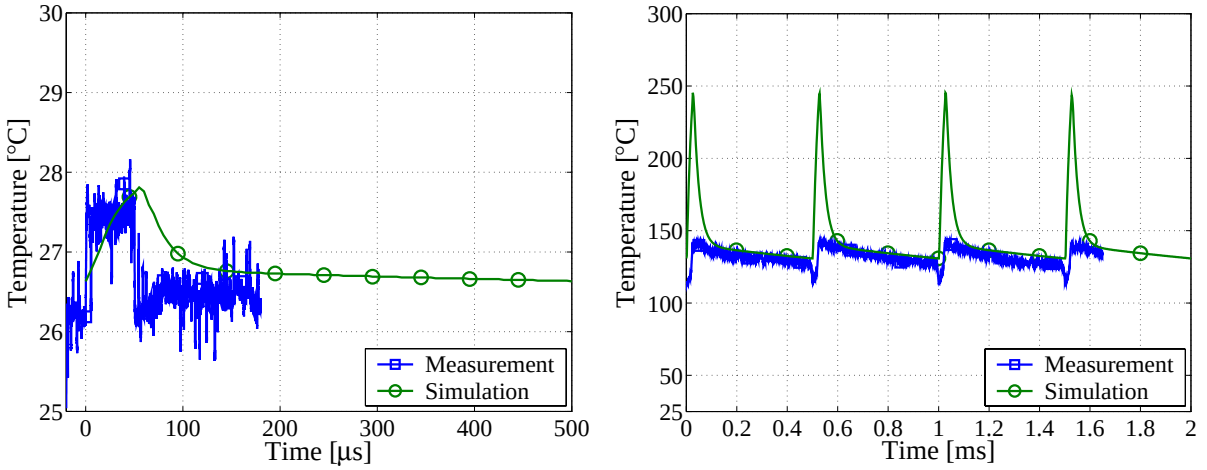
Figure 8.26: PIN Junction Temperature, Thermal Model Prediction vs Measurement



(a) 1ms Pulse Width, 10% Duty Cycle, Low Power

(b) 200μs Pulse Width, 10% Duty Cycle, Low Power

Figure 8.27: PIN Junction Temperature, Thermal Model Prediction vs Measurement



(a) 50μs Pulse Width, 10% Duty Cycle, Low Power (b) 24μs Pulse Width, 4.8% Duty Cycle, High Power

Figure 8.28: PIN Junction Temperature, Thermal Model Prediction vs Measurement

8.6 Conclusion

The temperature values and time constants of the low power measurements are predicted relatively accurately by the developed electric circuit analogue of the PIN diode transient thermal heating model. Peak temperatures predicted by the thermal model for high input power levels are not observed in the measured junction temperature response. These peak values increase the average junction temperature considerably, resulting in an inaccurate peak power prediction ability of the simple thermal model.

The average diode junction temperature is measured as roughly 130°C with a 2 kW peak input power level. During the measurement of the 4 kW pulse, the observed average diode voltage dropped by roughly 350 mV, implying an average diode junction temperature of around 230°C. This value greatly exceeds the specified average upper temperature limit of 175°C, with no signs of diode failure. The exact upper temperature at which heating will incur diode failure is therefore unknown. A further uncertainty is the exact relationship between diode voltage and diode temperature at high temperatures, since the temperature calibration of Sec. 8.2 only shows values up to a maximum temperature of 100°C.

Thermal modelling of the PIN diode leading to accurate predictions of acceptable peak power levels may be further investigated. The 4 kW peak power level at which the switch was successfully tested, exceeds the specified maximum power handling ability of 2.25 kW as specified in Table 8.1, which states a peak power handling capability in the active mode of 4.5 kW, using two switching channels to halve the power through each channel. The power handling ability can be extended using two or four waveguide switch channels in

parallel, as depicted in Fig. 8.29.

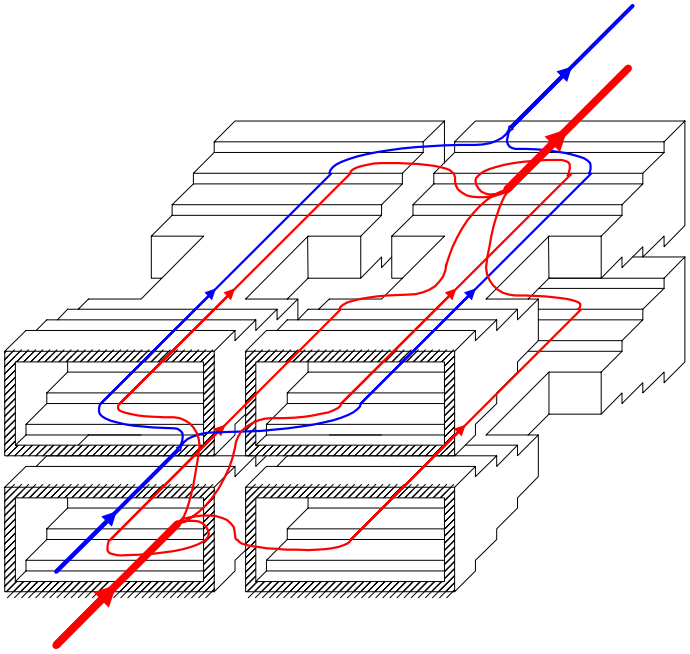


Figure 8.29: Dual- and Quadruple-Channel Power Flow

Chapter 9

Conclusion

A tunable X-band waveguide switch, which improves on the drawbacks of existing waveguide switches, has been presented in this dissertation. The proposed switch displays a wide bandwidth and very simple diode mounting structure, which additionally offers in-situ tuning. The proposed switch is implemented in evanescent mode waveguide with a novel diode mounting topology, allowing the operating frequency to be shifted after construction. This concept offers a substantial reduction in assembly costs.

Accurate modelling of the filter and limiter states of the proposed switch is possible, using an evanescent mode PIN diode and mount model. The model is developed by optimizing an AWR Microwave Office model of the first order switch with embedded PIN diode, to converge with the filter/limiter measurements, for all four first order prototypes. The model is subsequently used in the design of a third order switch with much improved isolation in the limiting state. The third order switch achieves isolation of 62 dB over a 8.5 to 10.5 GHz bandwidth in the limiting state, as well as reflection of 15.73 dB and insertion loss of 1.23$\pm$0.155 dB in the filtering state over the same bandwidth.

Thermal models of specific diodes are not available from the manufacturers. Therefore, in order to determine the heating effects of a high power input signal on the diode junction, a thermal model is developed for the particular diode used in the design, by using package dimensions and power measurements.

The switch was successfully tested at a peak power level of 4 kW, with a pulse width of 24μs at a 4.8% duty cycle.

The author anticipates that future extensions of this work could include the following:

- Thermal Modelling

  Thermal modelling of the PIN diode, leading to accurate predictions of acceptable peak power levels, may be further investigated. Further high power measurements could determine the exact upper temperature bound of the PIN diode junction. An extension of the PIN diode thermal model would allow for accurate modelling of the second order thermal overshoot phenomenon, and could prove useful for temperature predictions of shorter input pulse widths.

- Loss Minimization

  To achieve the lowest transmission loss in the structure when filtering, copper or silver plating of the interior waveguide walls is essential.

- Multiple Channel Limiter

  The next step of integrating the single switch into a multiple channel limiter structure, is the development of a driver circuit to switch between PIN diode bias states in the shortest possible time after detection of a high power input signal. This addition would allow for accurate measurement of the switching time of the device, which is an important specification in commercial limiters.

- Removable Diode Unit

  Integration of the existing diode mount topology into a completely separate removable unit would offer an improvement of the diode mounting structure, by allowing simple PIN diode replacement in the case of switch failure.

Appendix A

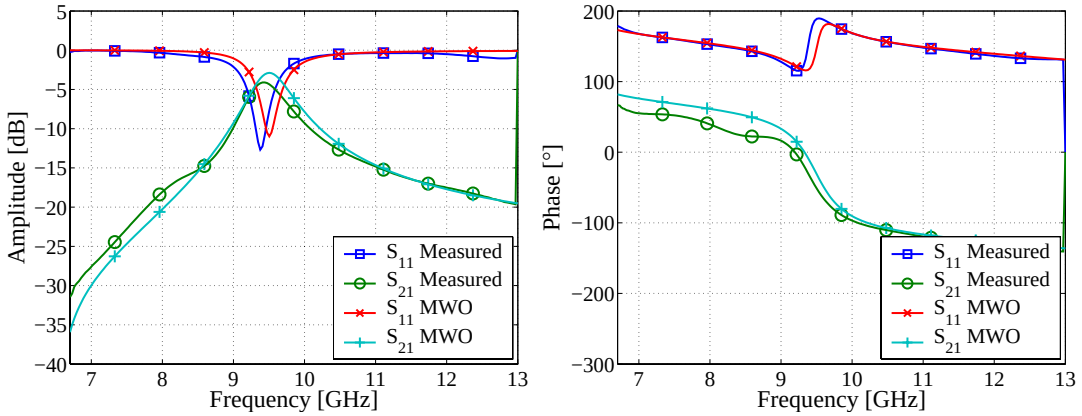
Modelling

Obstacles in evanescent mode waveguide do not necessarily have the same equivalent circuits as those applying in the propagating region [3]. The method of obstacle admittance measurement by Mok [20], presented in Chapter 4, is useful for simple obstacles. The object is placed on the plane between propagating and evanescent mode waveguide, with the propagating guide of equal dimensions as the evanescent mode guide loaded with dielectric, to allow propagation of the TE_{10} mode. This technique requires two measurement setups to be made with two input admittance measurements.

A simpler method which is more specific to the particular application, is used to obtain the lumped element circuit model parameters of the more complex PIN diode mount structure. This method solves the problem as discussed in Sec. 6.2, where a single AWR Microwave Office model is found, that fits to all the filter/limiter measurements for all four prototypes, by varying only the mount and junction capacitances. Table A.1 recalls the differences in element values used in the models of CST Microwave Studio and AWR Microwave Office. Measurements and simulations of filters and limiters, using *PIN Diode Topology 1* tuned to various frequencies, are shown in Figs. A.1 to A.19. Good correlation between simulated and measured data is achieved across the range.

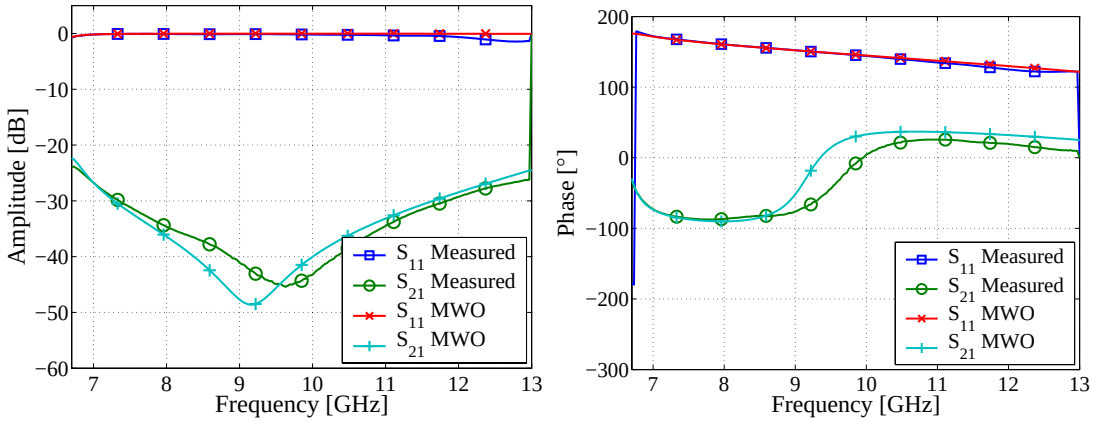
PIN DIODE ELEMENT	CST MODEL	AWR MODEL
C_{PIN} (pF)	0.2	0.37
C_p (pF)	0.14	0.3
L_{PIN} (nH)	0.217	0.217
R_s (Ω)	2	1

Table A.1: Free-Space vs. Evanescent Mode PIN Diode Element Values



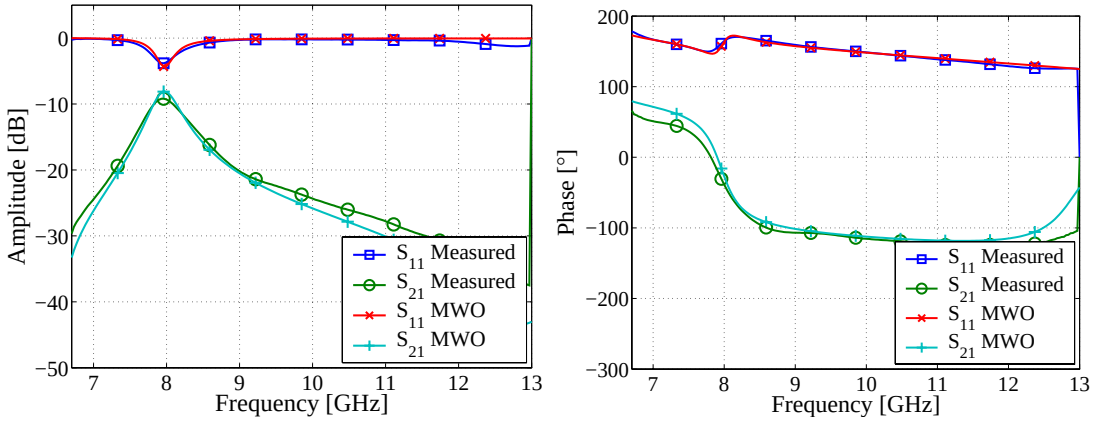
(a) Magnitude (b) Phase

Figure A.1: *Vertical-Ground Horizontal-Feed Substrate Design*: No Junction Tuners, Both Diodes Reverse Biased



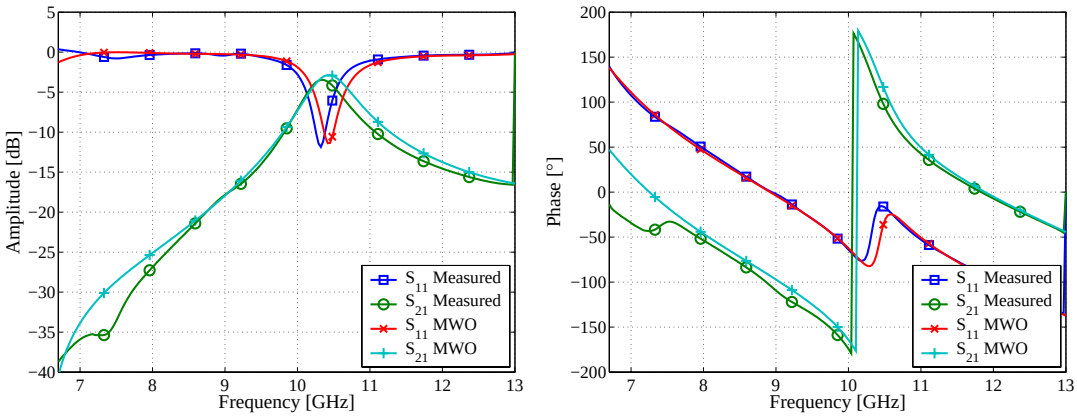
(a) Magnitude (b) Phase

Figure A.2: *Vertical-Ground Horizontal-Feed Substrate Design*: No Junction Tuners, Both Diodes Forward Biased



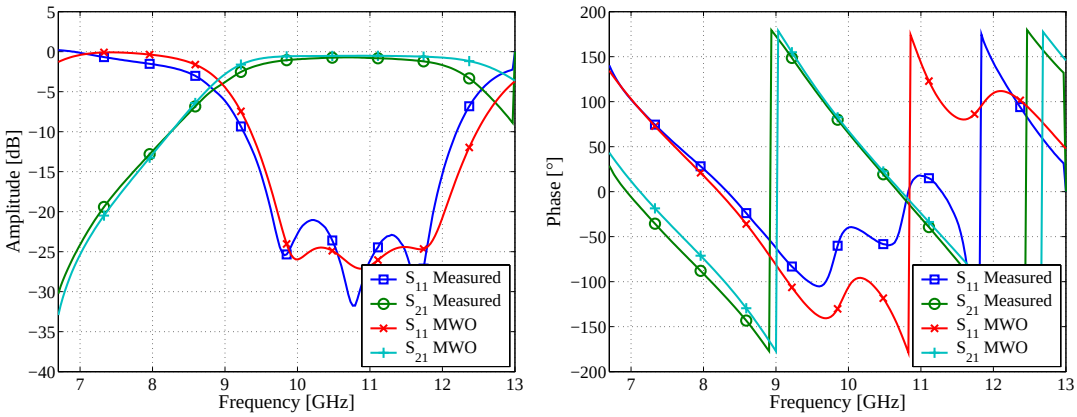
(a) Magnitude (b) Phase

Figure A.3: *Vertical-Ground Horizontal-Feed Substrate Design*: No Junction Tuners, One Diode Reverse Biased, One Diode Forward Biased



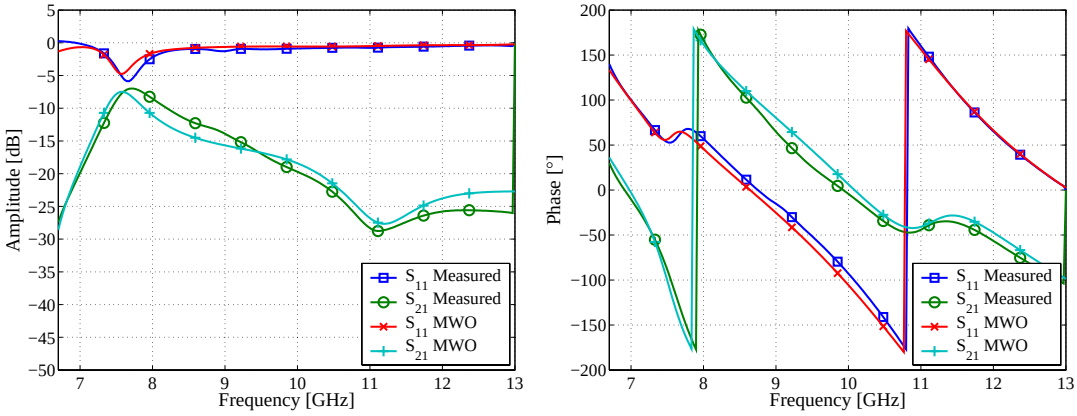
(a) Magnitude (b) Phase

Figure A.4: *Vertical-Ground Horizontal-Feed Substrate Design*: PAD1, No Junction Tuners, Filter



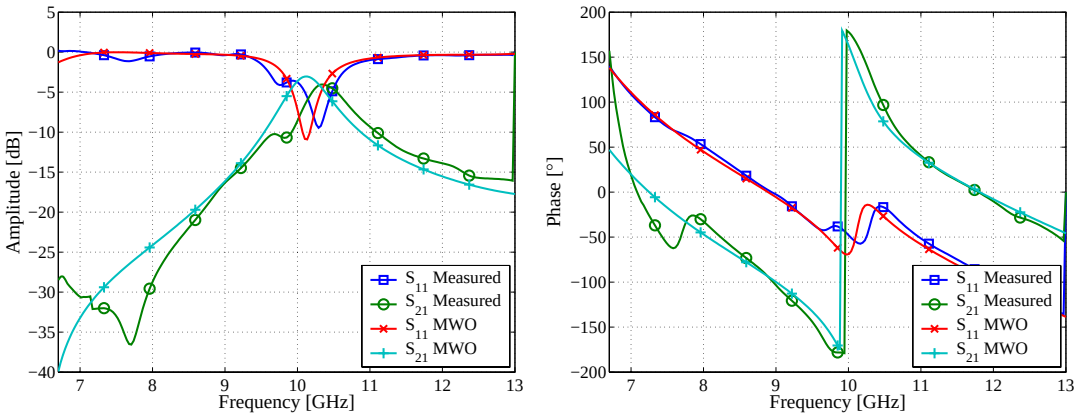
(a) Magnitude (b) Phase

Figure A.5: *Vertical-Ground Horizontal-Feed Substrate Design*: PAD1, Filter



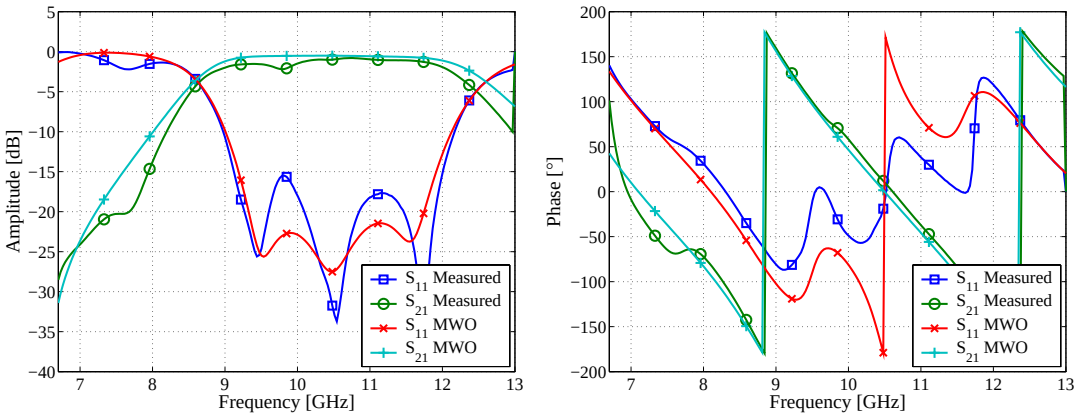
(a) Magnitude (b) Phase

Figure A.6: *Vertical-Ground Horizontal-Feed Substrate Design*: PAD1, Limiter



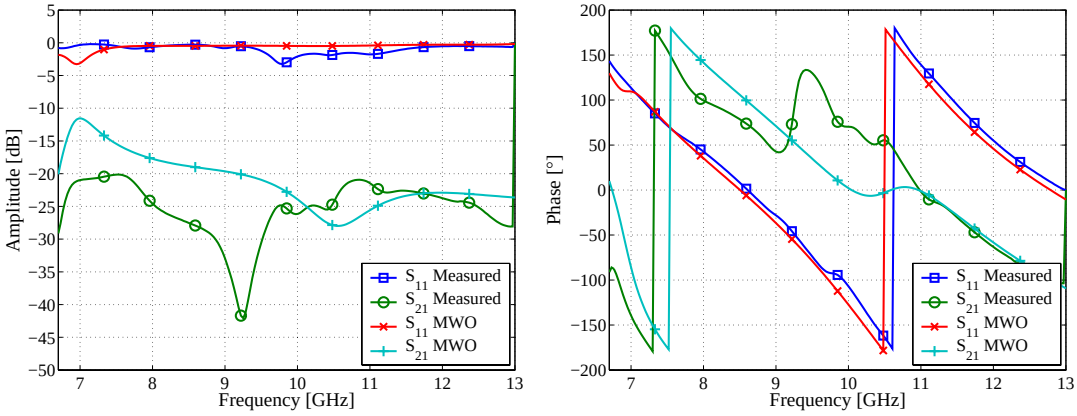
(a) Magnitude (b) Phase

Figure A.7: *Vertical-Ground Horizontal-Feed Substrate Design*: PAD2, No Junction Tuners, Filter



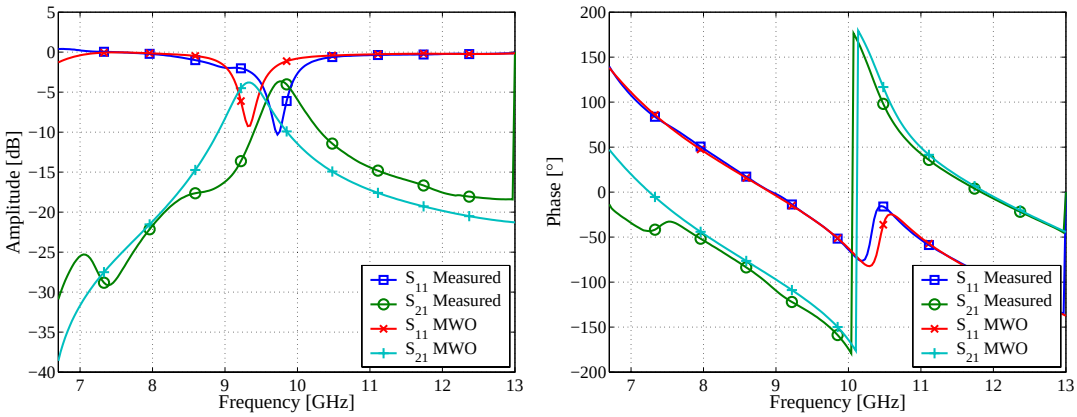
(a) Magnitude (b) Phase

Figure A.8: *Vertical-Ground Horizontal-Feed Substrate Design*: PAD2, Filter



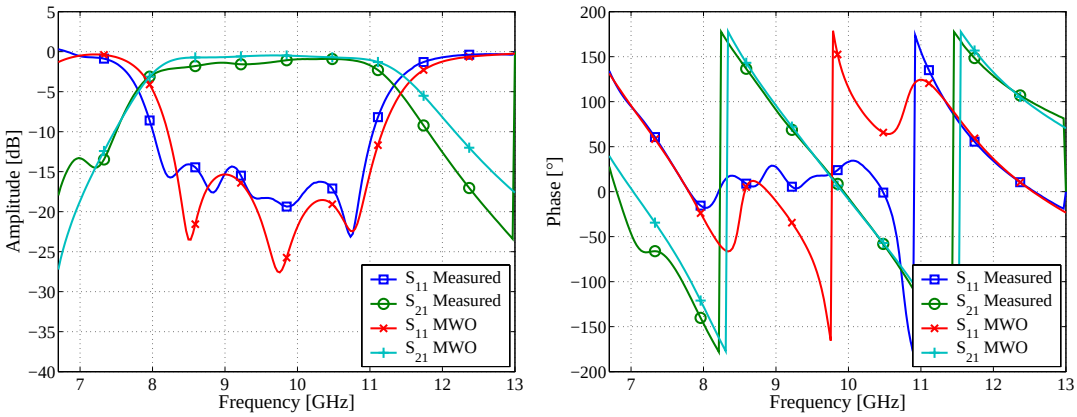
(a) Magnitude (b) Phase

Figure A.9: *Vertical-Ground Horizontal-Feed Substrate Design*: PAD2, Limiter



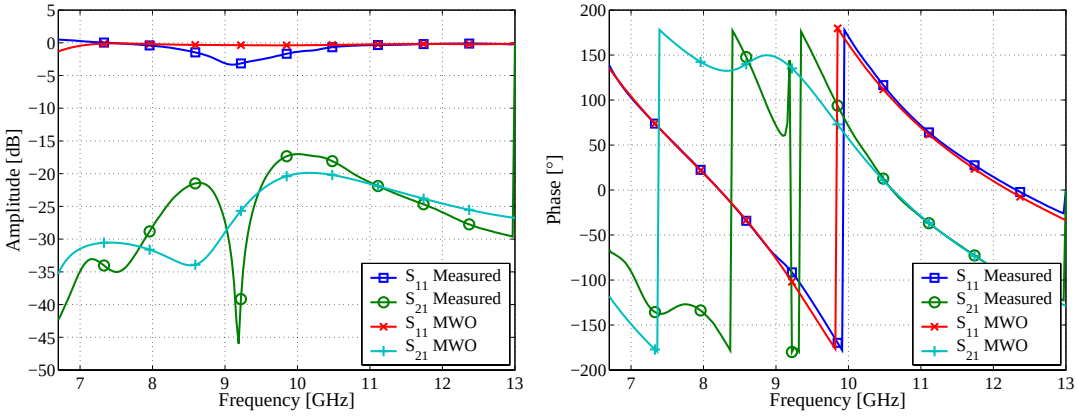
(a) Magnitude (b) Phase

Figure A.10:*Vertical-Ground Horizontal-Feed Substrate Design*: PAD3, No Junction Tuners, Filter



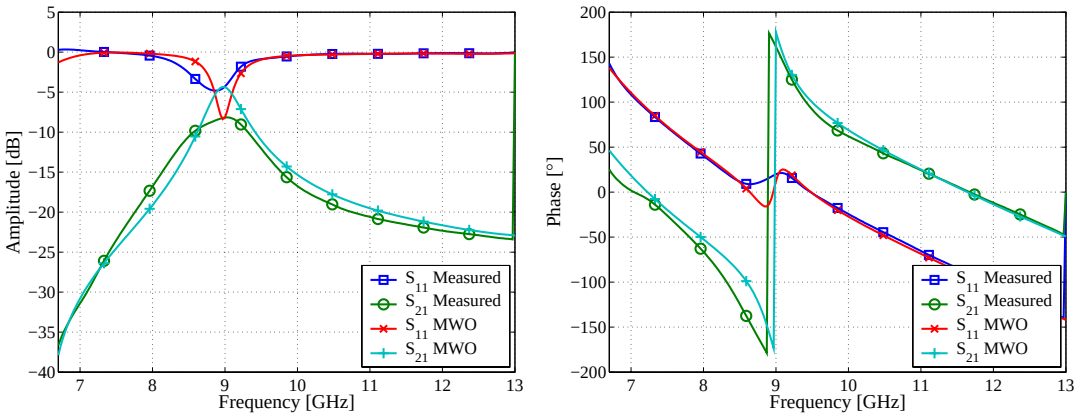
(a) Magnitude (b) Phase

Figure A.11:*Vertical-Ground Horizontal-Feed Substrate Design*: PAD3, Filter



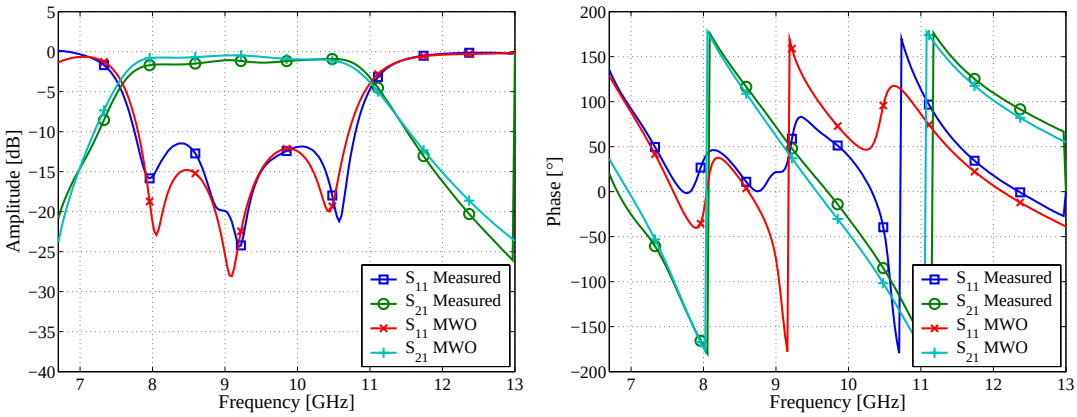
(a) Magnitude (b) Phase

Figure A.12:*Vertical-Ground Horizontal-Feed Substrate Design*: PAD3, Limiter



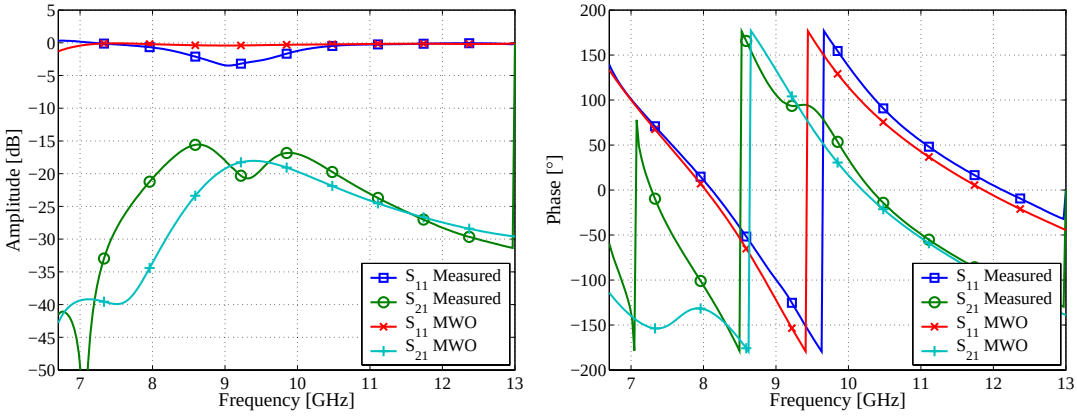
(a) Magnitude (b) Phase

Figure A.13:*Vertical-Ground Horizontal-Feed Substrate Design*: PAD4, No Junction Tuners, Filter



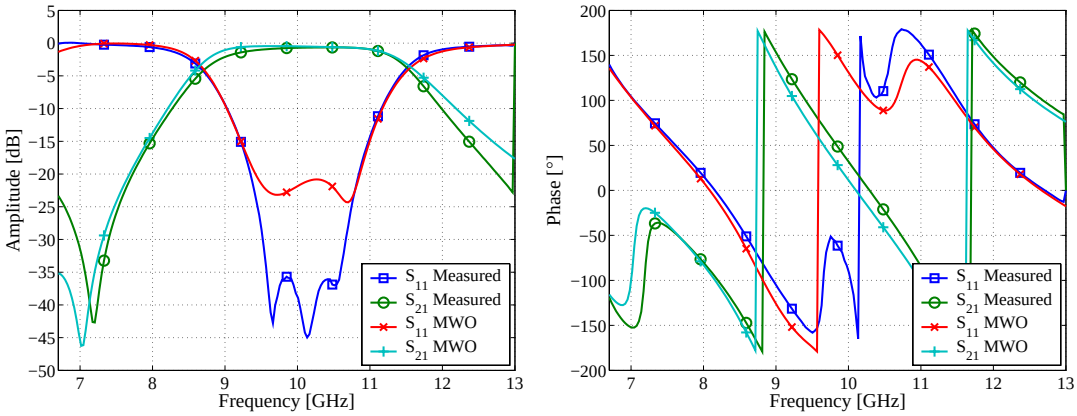
(a) Magnitude (b) Phase

Figure A.14:*Vertical-Ground Horizontal-Feed Substrate Design*: PAD4, Filter



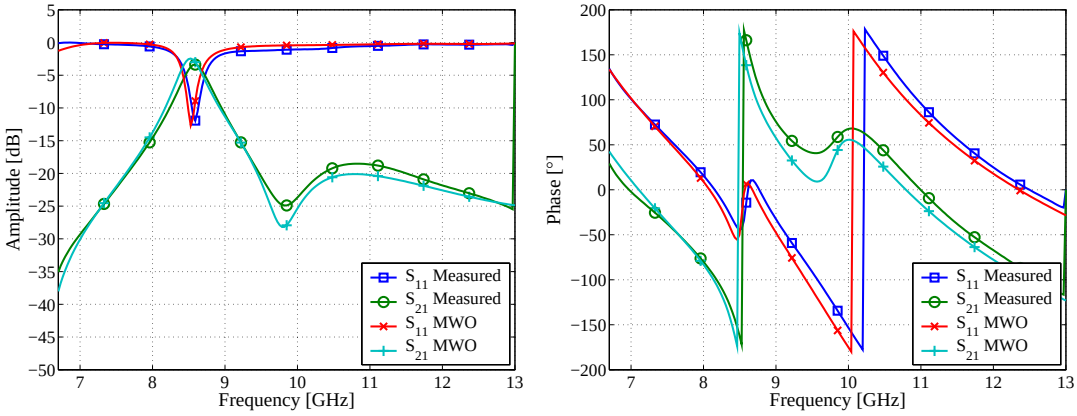
(a) Magnitude (b) Phase

Figure A.15:*Vertical-Ground Horizontal-Feed Substrate Design*: PAD4, Limiter



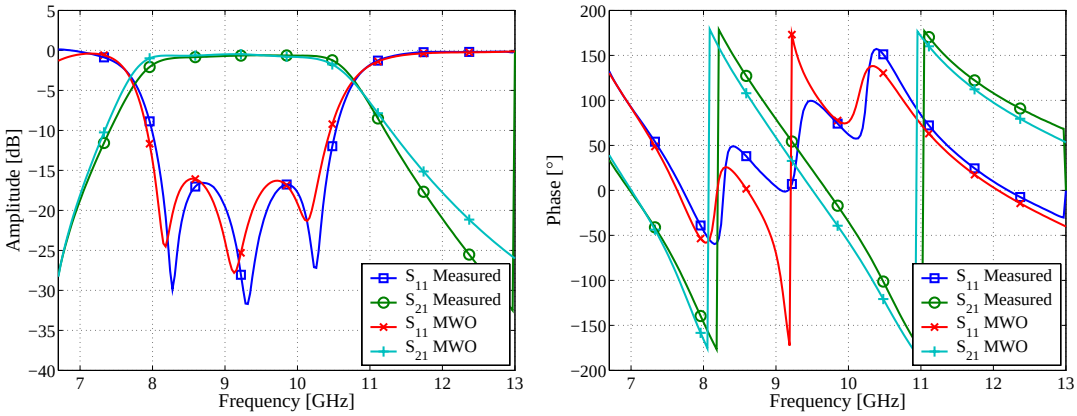
(a) Magnitude (b) Phase

Figure A.16:*Vertical-Ground Horizontal-Feed Via Substrate Design*: PAD3, Via, Filter



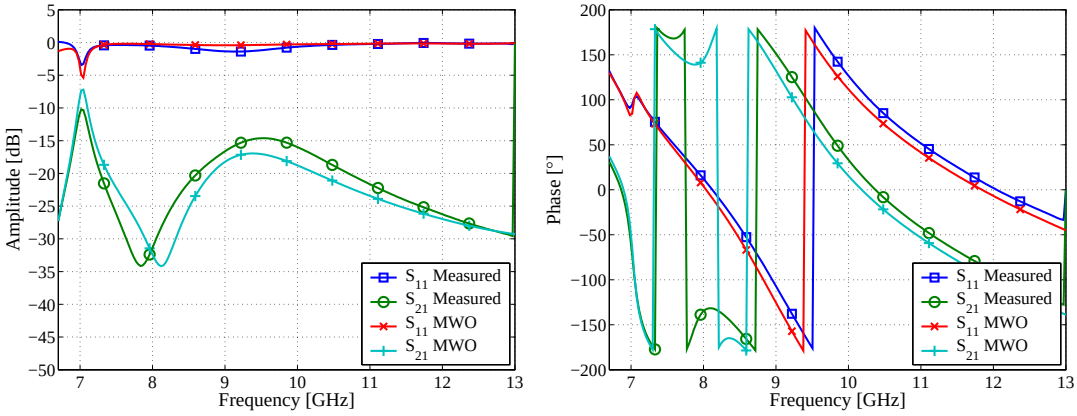
(a) Magnitude (b) Phase

Figure A.17:*Vertical-Ground Horizontal-Feed Via Substrate Design*: PAD3, Via, Limiter



(a) Magnitude (b) Phase

Figure A.18:*Vertical-Ground Horizontal-Feed Via Substrate Design*: PAD4, Via, Filter



(a) Magnitude (b) Phase

Figure A.19:*Vertical-Ground Horizontal-Feed Via Substrate Design*: PAD4, Via, Limiter

Appendix B

Dimensions

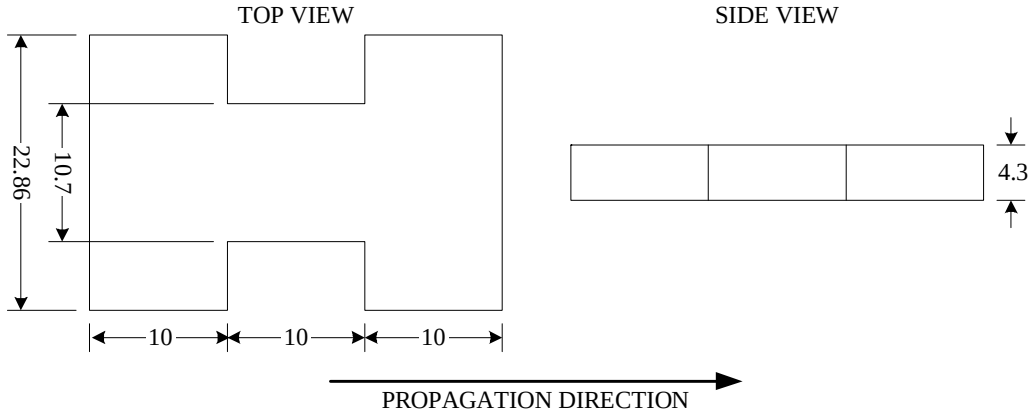


Figure B.1: Fig. 4.18(a) Dimensions [mm]

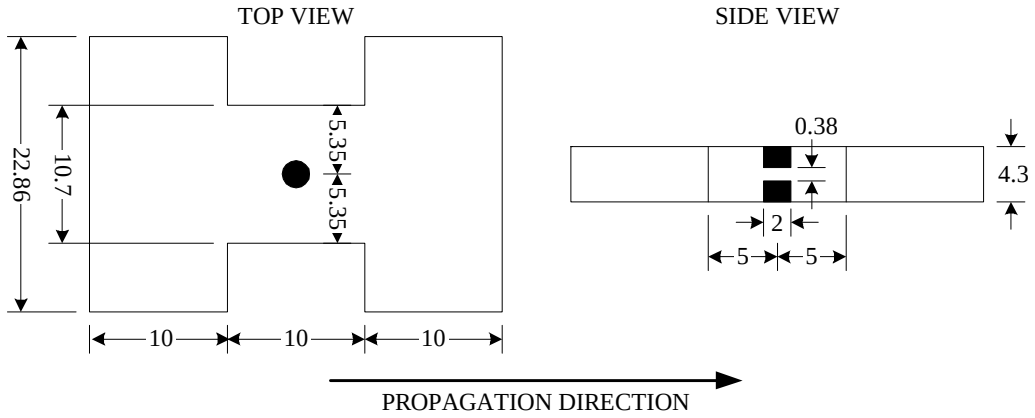


Figure B.2: Fig. 4.22(a) Dimensions [mm]

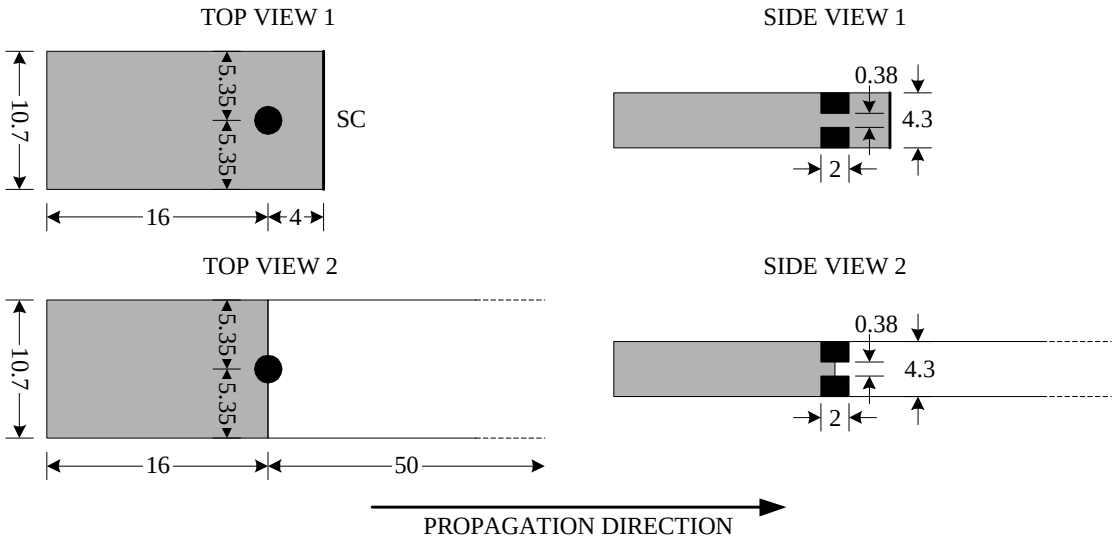


Figure B.3: Fig. 4.23 Dimensions [mm]

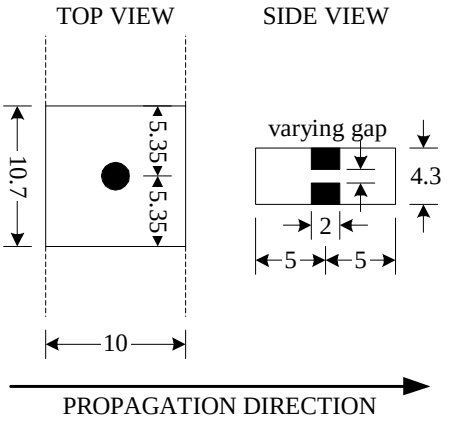


Figure B.4: Fig. 5.10 Dimensions [mm]

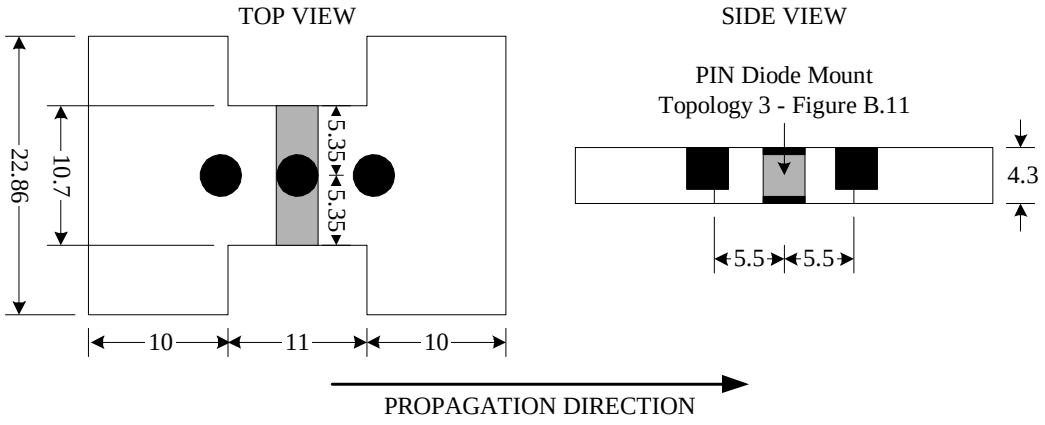


Figure B.5: Fig. 6.4 Dimensions [mm]

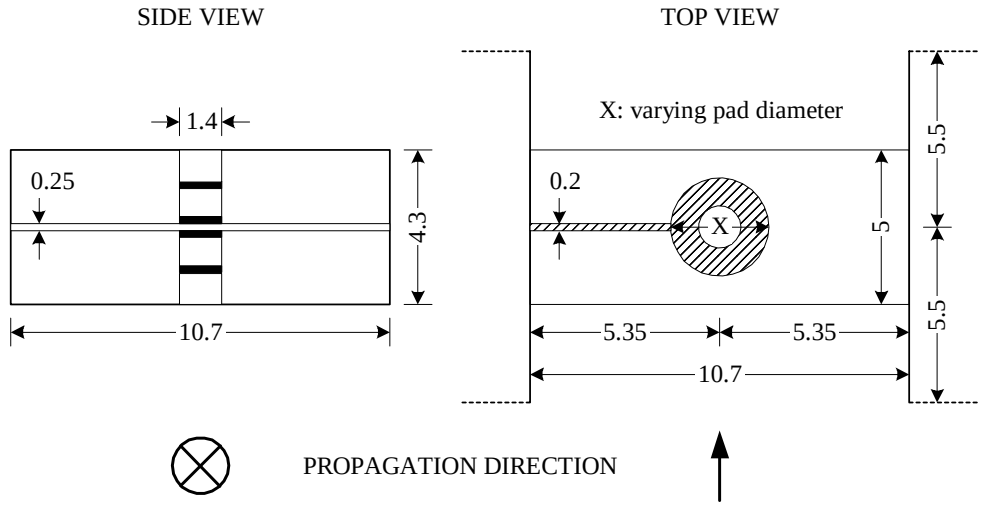


Figure B.6: Fig. 6.10 Dimensions [mm]

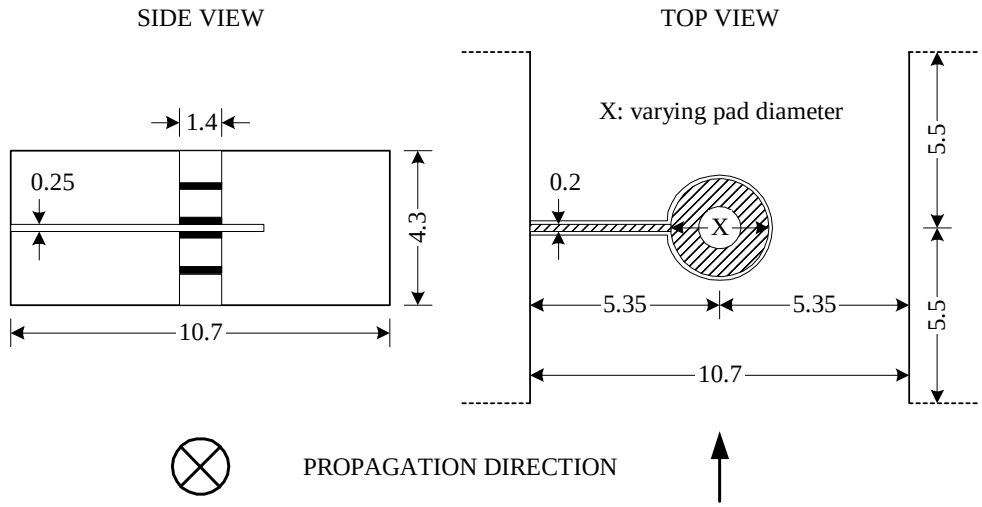


Figure B.7: Fig. 6.13 Dimensions [mm]

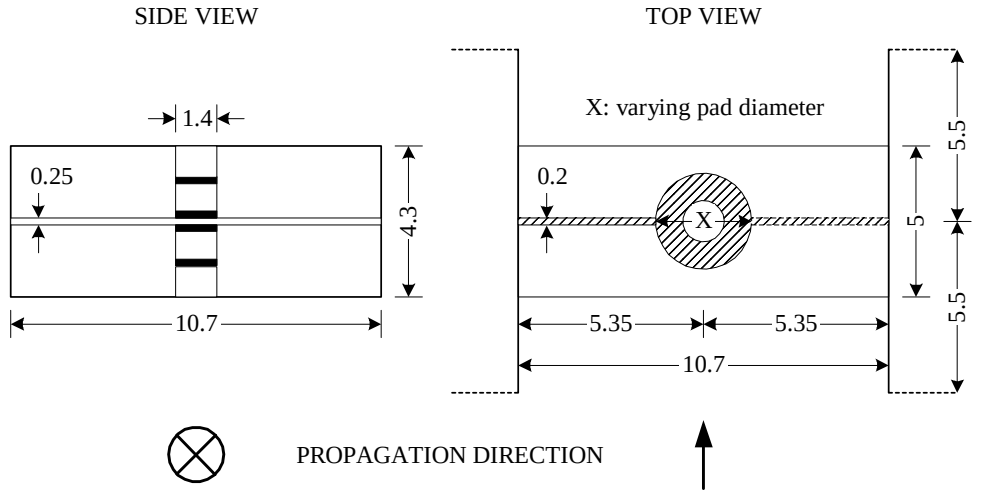


Figure B.8: Fig. 6.14 Dimensions [mm]

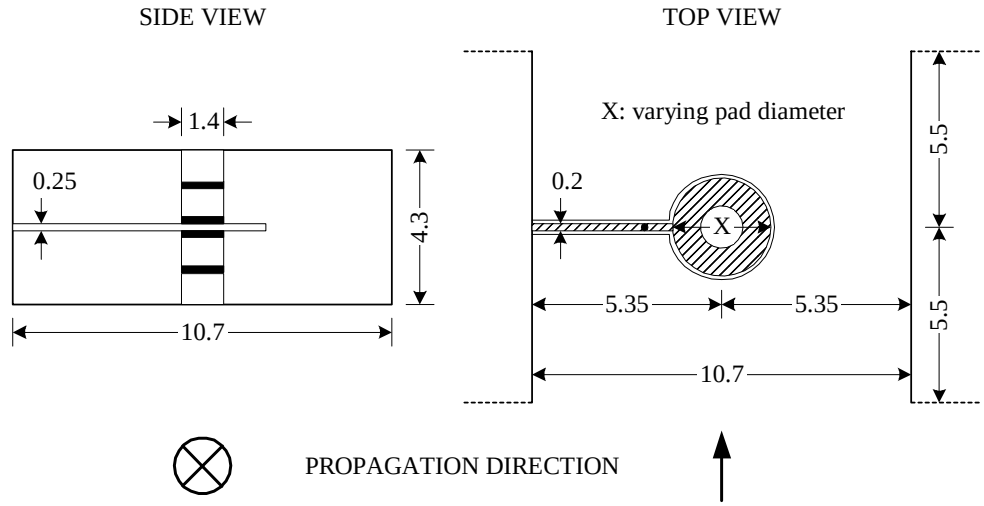


Figure B.9: Fig. 6.16 Dimensions [mm]

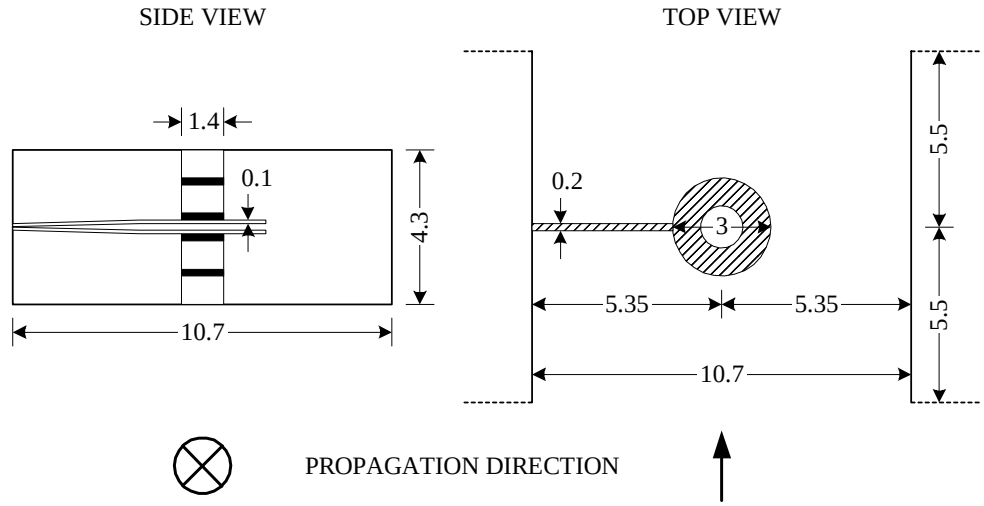


Figure B.10: Fig. 6.18 Dimensions [mm]

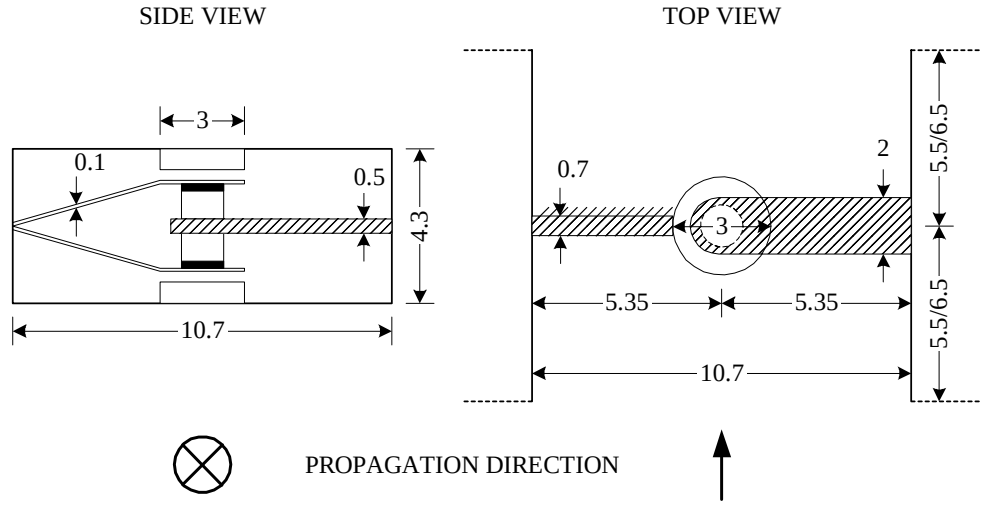


Figure B.11: Fig. 6.20 Dimensions [mm]

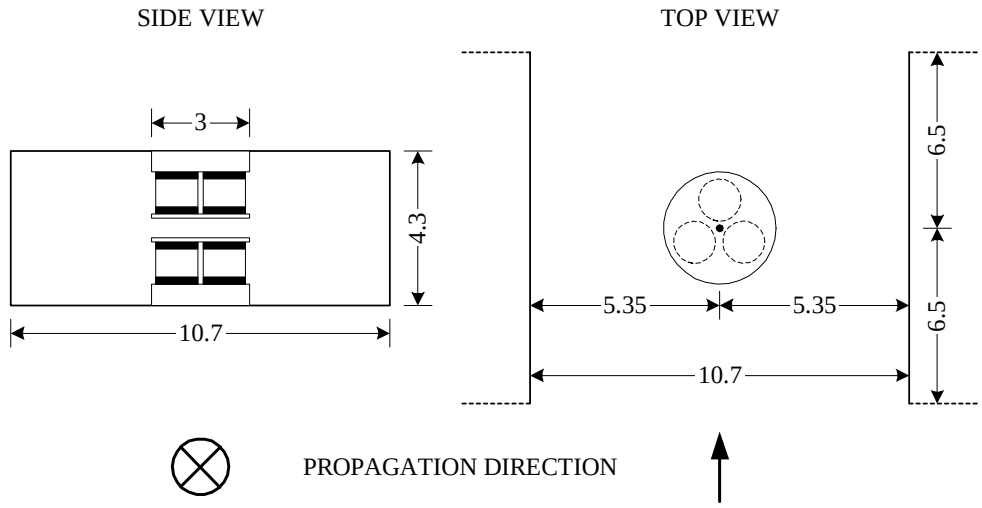


Figure B.12: Fig. 6.23 Dimensions [mm]

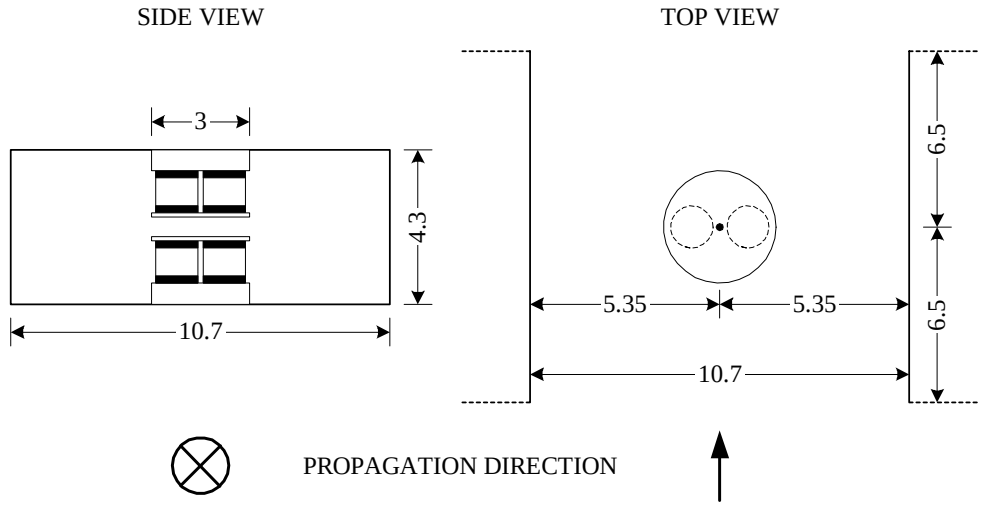


Figure B.13: Fig. 6.25 Dimensions [mm]

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