Development of a frequency synthesizer for a low-cost radio interferometer

by
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I would like to start by thanking the good Doctor Steyn. He is an exemplary human being with grace and humour to suit any situation and limitless knowledge in his field.

I would like to thank Wessel, Wendy and Johan for helping hack together some of my RF PCBs. Patchwork on an RF PCB is not a task for the non-inventive or those with unsteady hands.

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I have to thank Dean Banerjee. His textbook is an excellent first line of attack against phase noise and the phase-locked loop.

And lastly, we stand on the shoulders of giants. To the wealth of human knowledge and understanding, to all those who came before us, we all owe an unthinkable debt. May God bless us all as we continue forward.

Declaration

By submitting this thesis electronically, I declare that the entirety of the work contained therein is my own, original work, that I am the sole author thereof (save to the extent explicitly otherwise stated), that reproduction and publication thereof by Stellenbosch University will not infringe any third party rights and that I have not previously in its entirety or in part submitted it for obtaining any qualification.

December 2023

Abstract

English

This document contains a description of the basics of a phase-locked loop when used as a frequency synthesizer. The document also contains an introduction to phase noise and a description of how to model and simulate phase noise in a phase-locked loop. Three different phase-lock loops are then designed, simulated and measured with the goal of generating local oscillator signals for an array of superheterodyne receivers.

Afrikaans

Hierdie dokument bevat 'n beskrywing van die basiese beginsels van 'n fasegeslote lus wanneer dit as 'n frekwensie-sintetiseerder gebruik word. Die dokument bevat ook 'n inleiding tot fasegeraas en 'n beskrywing van hoe om fasegeraas in 'n fasegeslote lus te modelleer en te simuleer. Drie verskillende fasesluitlusse word gebou, gesimuleer en gemeet met die doel om plaaslike ossillatorseine vir 'n verskeidenheid superheterodyne-ontvangers te genereer.

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Nomenclature

Variables and functions

$\mathrm{Var}(X)$	Variance of the random variable X.
$\mathrm{Cov}(X, Y)$	Covariance of the random variable X and the random variable Y.
$\langle x, y \rangle$	Dot product of function x and function y.
$\mathscr{F}(x)$	Fourier transform of function x.
s	Laplacian variable where $s = j2\pi f$

Acronyms and abbreviations

DSM	Delta sigma modulator
EMI	Electromagnetic interference
FOM	Figure of merit
IC	Integrated circuit
IEEE	Institute of electrical and electronics engineers
LDO	Low dropout regulator
LO	Local oscillator
LVPECL	Low-voltage positive emitter–coupled logic
PCB	Printed circuit board
PLL	Phase-locked loop
RF	Radio frequency
RMS	Root mean square
SPI	Serial peripheral interface
OCXO	Oven-controlled crystal oscillator
VCO	Voltage controlled oscillator

Chapter 1

Introduction

A mid-frequency antenna array is to be deployed to measure the sky at frequencies ranging from 500 MHz to 1500 MHz. The array will consist of 16 antennae each measuring two polarizations and will be spread out over an area of $3\,\mathrm{m}^2$.

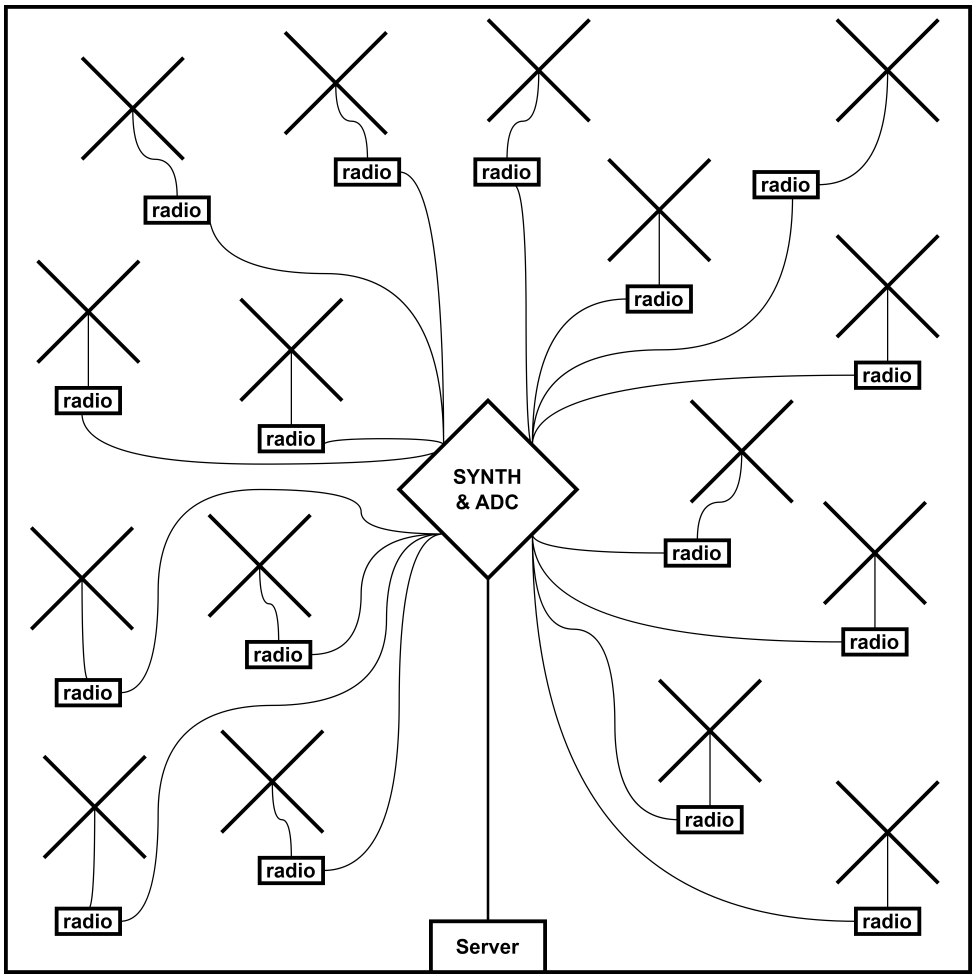


Figure 1.1: Layout of the antenna array.

Figure 1.1 shows the layout of the array: The information from each antenna is processed by the radio near it. The radios are all centrally sampled and the LOs for the radios are generated and distributed by the frequency synthesizer.

The mid-frequency array is to be used as a power combiner in early deployment and as an interferometer later on. For the array, a superheterodyne receiver has been designed. Figure 1.2 shows a common layout of a superheterodyne receiver.

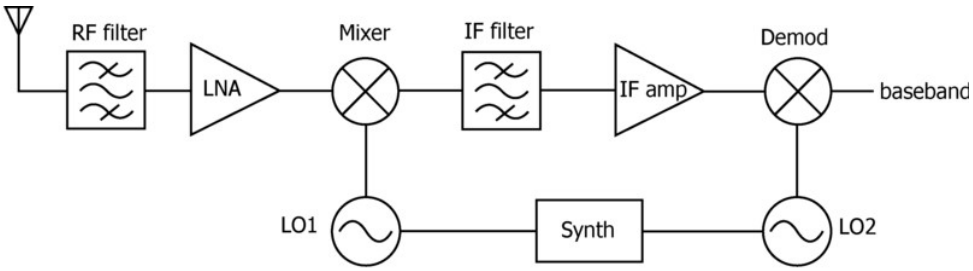


Figure 1.2: A superheterodyne receiver. [1]

This document discusses two approaches to synthesize and distribute the necessary local oscillators for the superheterodyne receivers. The LOs will be generated using phase-locked loops and the cost of the implemented clock distribution system is to be kept low.

The document will begin with an introduction to the phase-locked loop used as a frequency synthesizer and will proceed to an explanation of phase noise and phase noise in a phase-locked loop. Two different designs to deliver the required LOs will then be discussed, followed by simulations and measurements of some of the key elements of the designs.

Chapter 2

Phase-locked Loop

In this chapter the operation of a PLL will be discussed. The classical control theory models of the components that make up a PLL will be introduced. Finally, the classical control theory model of the PLL will derived and expounded upon.

2.1. The basic operation of a PLL used for frequency synthesize

The Phase-locked loop is a negative feedback loop, shown in figure 2.1. When used for frequency synthesizes the PLL is a frequency multiplier. A VCO is used to generate the output frequency. This output frequency is maintained over time by a reference oscillator. A phase detector, a charge pump circuit and a frequency divider make up the remainder of the PLL. The output of the VCO is connected to the frequency divider. The frequency divider is in the feedback path. The output of the frequency divider is fed into the phase detector. The phase detector compares the divided VCO frequency with that of the reference oscillator. The phase detector connected to the charge pump circuit and the output of the charge pump is the error signal, which is filtered and used to tune the VCO.

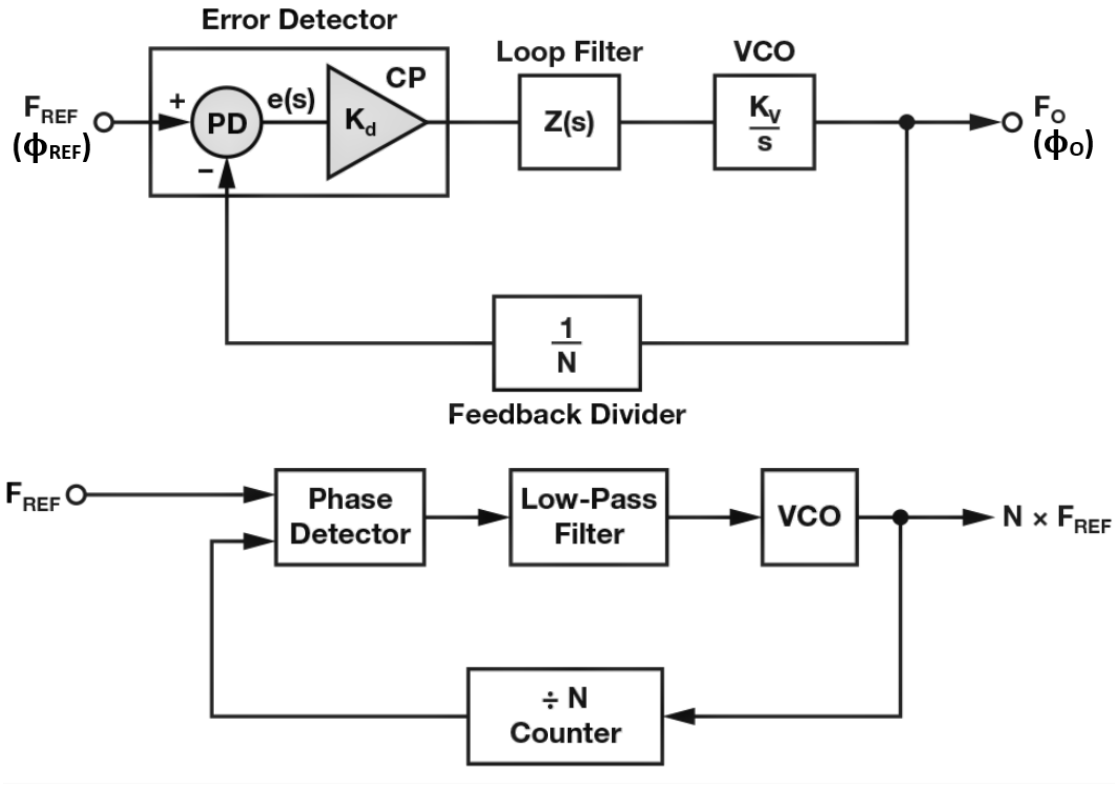


Figure 2.1: Two block diagrams representing the PLL. [2]

In figure 2.1, if the error signal is zero, the inputs to the phase detector are equal which means $f_o = Nf_{REF}$. Once the PLL output is $f_o = Nf_{\mathrm{REF}}$ the loop is locked and the time taken to reach steady state is called the lock time.

Phase locked loops are analysed in terms of phase not frequency. Frequency is the the time derivative of phase $f(t) = \frac{d\phi(t)}{dt}$ and so if $\phi(t)_o = \phi(t)_{\mathrm{REF}}$ then $f(t)_o = f(t)_{\mathrm{REF}}$ [3].

2.1.1. The Phase detector and charge pump

The phase detector and charge pump generate a pulse width modulated current output based on the phase difference between the output of reference oscillator f_R and the output of the N divider f_N as shown in figure 2.2 and figure 2.3. When the loop is locked the charge pump will still give off short pulses to avoid a dead-zone condition in the feedback loop [4].

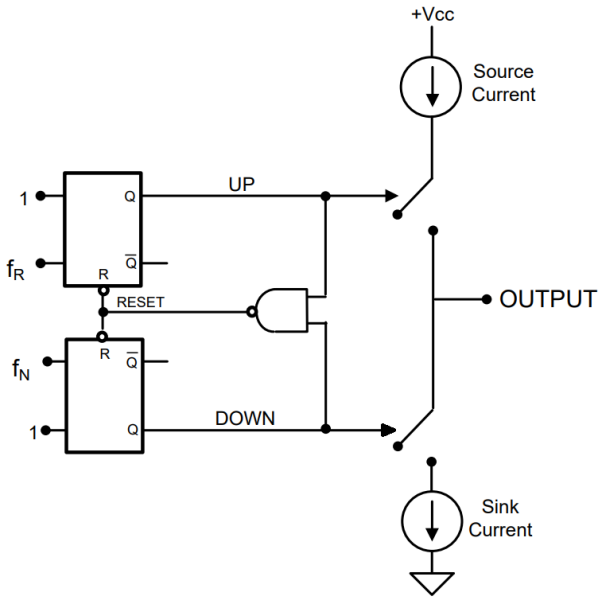


Figure 2.2: Phase detector and charge-pump circuit. [4]

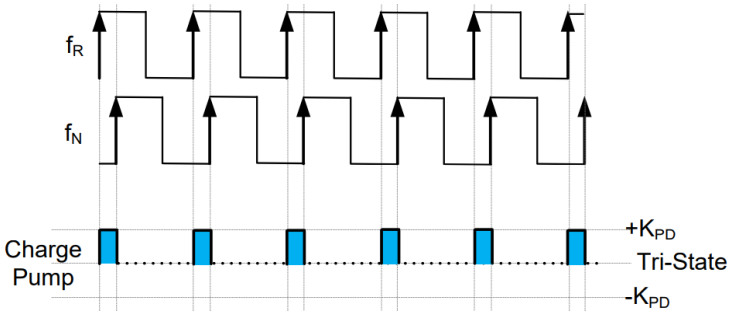


Figure 2.3: Illustration of charge pump output. [4]

To model the Charge pump as a single gain block:

The output of the charge pump is time averaged over the period between charge pump pulses, which is $\frac{1}{f_R}$.

Starting with $i_{\text{average}} = i_{\text{peak}} \frac{\Delta t}{T_{\text{R}}}$,

where Δt is the duration for which the charge pump is on;

noting that $i_{\text{peak}} = K_{\text{PD}}$

and using the relation $\frac{\Delta t}{T} = \frac{\Delta \phi}{2\pi}$. where $\Delta \phi$ is the phase difference between the reference signal and the signal from the output of the N divider.

The output of the charge pump is then modelled as $i_{\text{average}} = K_{\text{PD}} \frac{\Delta \phi}{2\pi}$.

The transfer function of the charge pump is then $\frac{i_{\text{average}}}{\Delta \phi} = \frac{K_{\text{PD}}}{2\pi}$.

2.1.2. The loop filter

The loop filter filters the output of the charge pump and provides the tuning voltage to control the VCO. Some VCO tuning ranges exceed that which can be met by the charge pump circuit and a passive filter; in such a case an active filter is used to add the necessary voltage output range to the loop filter in order to tune the VCO [4]. Third order loop filters contribute towards better spur attenuation and fourth order filters are used to achieve the same performance as third order filters with a possible improvement of lock-time [4].

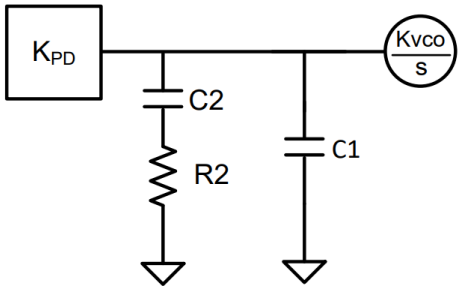


Figure 2.4: Second order passive loop filter. [4]

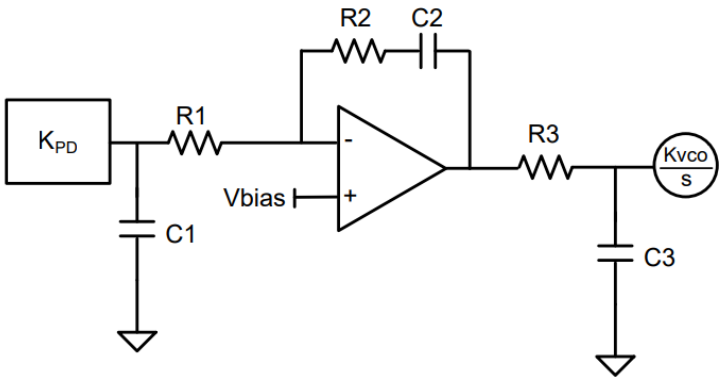


Figure 2.5: 3rd order active loop filter. [4]

The typical bode magnitude plot of the transfer function of the second order loop filter in figure 2.4 is shown in figure 2.6 and has the transfer function given in equation 2.1.

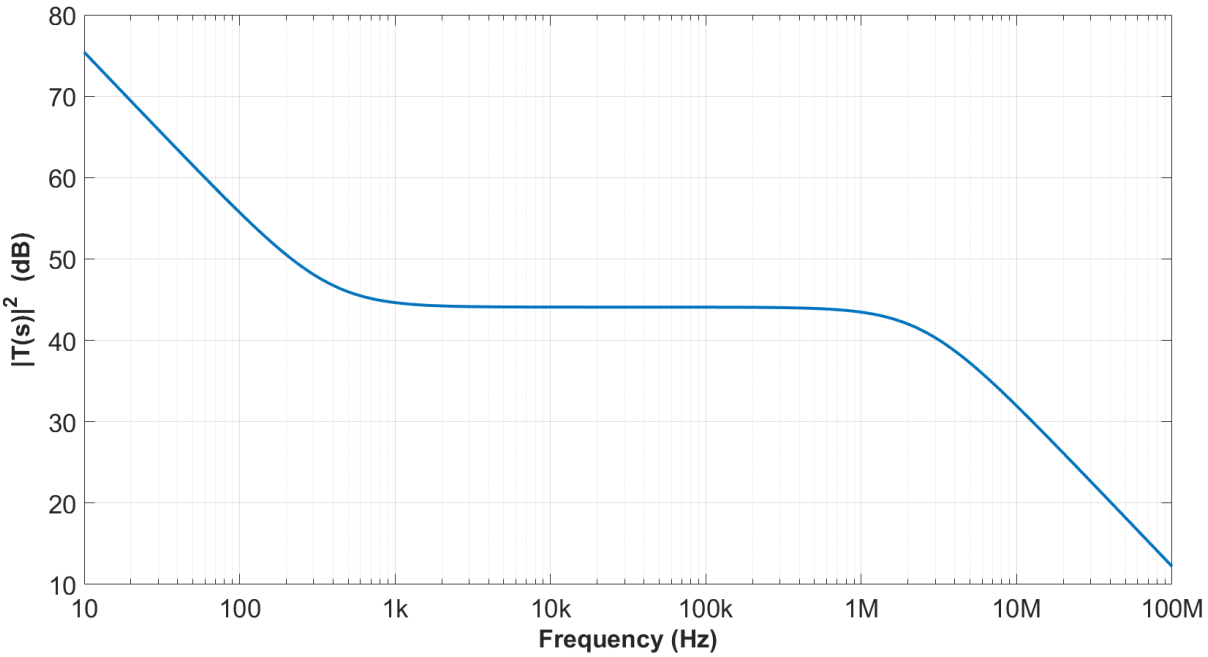


Figure 2.6: 2^{nd} order active loop filter Transfer function.

$$T(s) = \frac{sR_2C_2 + 1}{s[sR_2C_1C_2 + (C_1 + C_2)]} \tag{2.1}$$

2.1.3. The VCO

A VCO derives its characteristics from two sub-circuits: The tank circuit, three reactive elements which store and transfer energy between one another and the biasing circuitry, which provides the negative impedance required to sustain oscillations, that is, replenishes energy lost in the parasitic resistance of the tank circuit. The tank circuit determines and limits the frequency range of the VCO.

The output frequency of a VCO is changed by adjusting the capacitance of the tank circuitry which changes the frequency at which the oscillator resonates. The adjustment is made by changing the voltage bias across a varactor diode which changes the capacitance of the diode.

Expensive high-performance VCOs often have tuning ranges in the region of 12 V. To tune the full range of such a VCO requires the use of an operational amplifier. Silicon VCOs are often embedded in PLL chips. Silicon VCOs have multiple tank circuits between which the VCO can switch, providing a much larger frequency output range at the cost of the high performance of external VCOs [5] [3].

$$\Phi_{\text{VCO}} = \frac{2\pi}{s}F_{\text{VCO}} = \frac{2\pi}{s}K_V V_{\text{tune}} = \frac{K_V}{s}V_{\text{tune}} \tag{2.2}$$

$$\frac{\Phi_{\text{VCO}}}{V_{\text{tune}}} = \frac{2\pi K_V}{s} \tag{2.3}$$

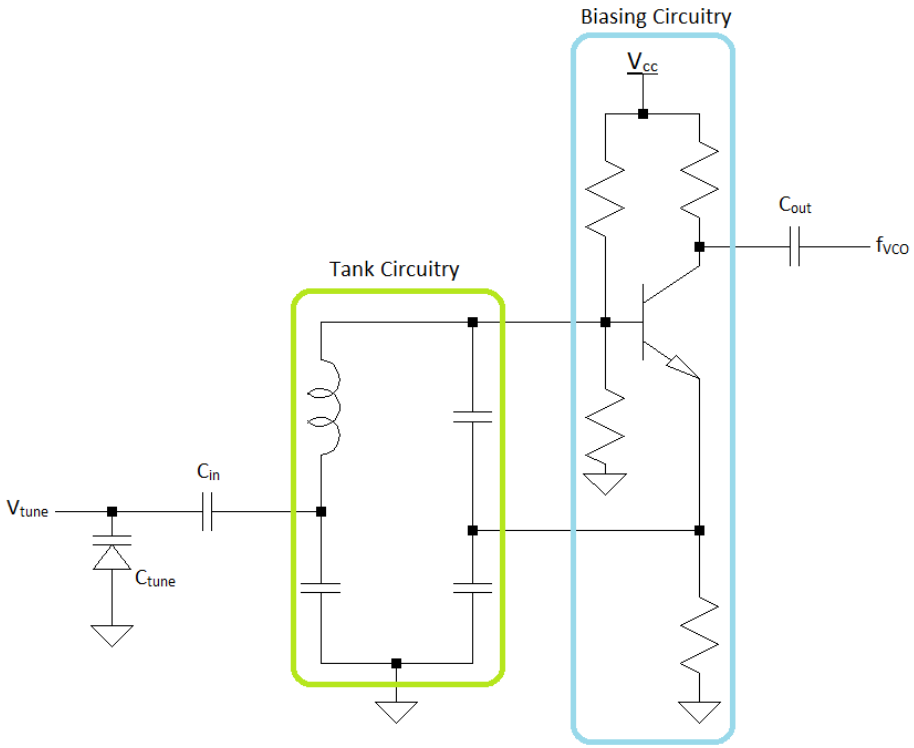


Figure 2.7: Common collector VCO.

Equation 2.2 and 2.3 show the derivation of the transfer function of the VCO. The output phase of the VCO is the time integral of the output frequency of the VCO, in the Laplace domain this conversion is the factor $\frac{1}{s}$. The tuning co-efficient, K_V is the ratio of the output frequency F_{VCO} and the input voltage V_{tune}. The VCO tuning coefficient is a function of the output frequency of the VCO. Figure 2.8 shows a typical curve for K_V vs. the tuning voltage of a VCO.

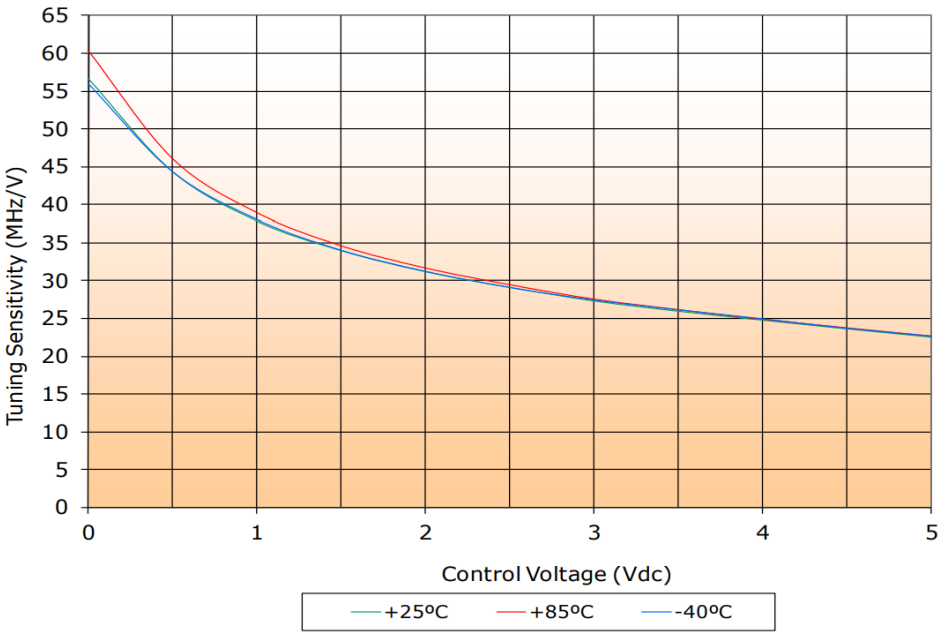


Figure 2.8: A typical curve for K_V vs. the output frequency of a VCO. [6]

2.1.4. The N divider

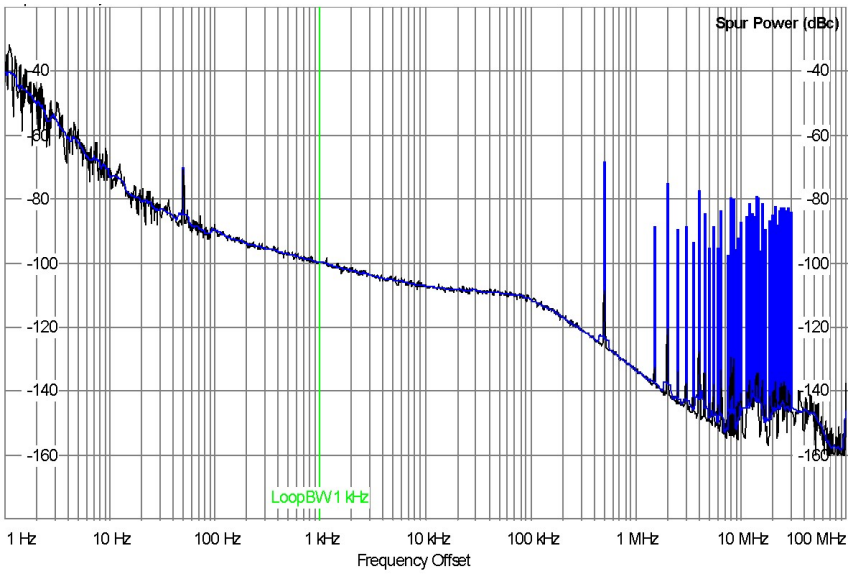
The N divider is digital circuitry that counts a number of input clock cycles and outputs a single clock cycle every n^{th} input cycle. A simple, low-frequency version can be implemented using flip-flops.

A PLL can function as either an integer PLL or a fractional PLL. A fractional PLL can achieve frequencies that aren't a direct multiple of the reference frequency. This is achieved by quickly changing the N divider between two, in the most simple case, different values.

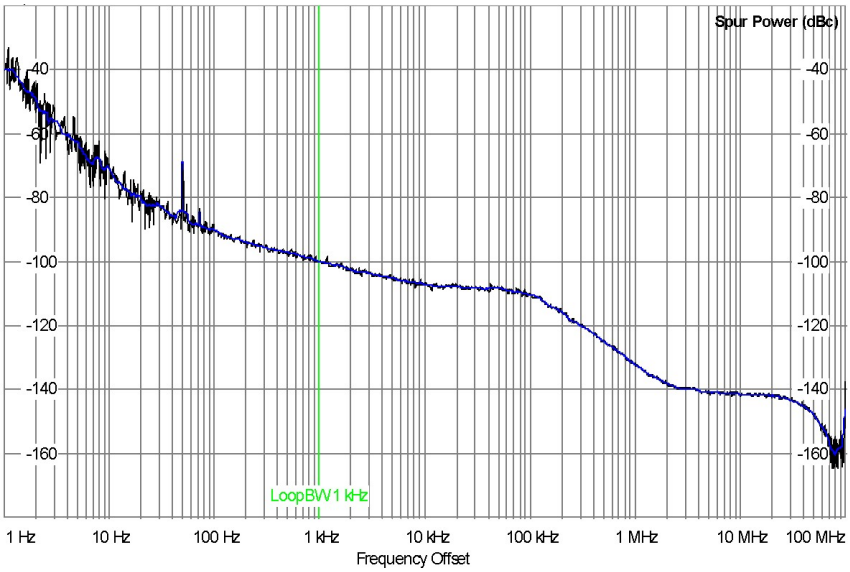
By way of example, if an N value of 100.33 were required, the N divider would be set at 100 for two cycles and 101 for the third and this pattern would repeat. This varying output is achieved using a first order delta-sigma modulator.

Higher order delta-sigma modulators achieve the desired ratio by switching N over a larger range of values. For a second order delta-sigma modulator the above example would be achieved using the sequence of values for N: $100, 100, 101, 99, 101, 101$. Spurs are introduced by using a fractional N divider. Higher order delta-sigma modulators suppress these spurs by shifting and spreading the frequency content of the spurs [7] [4].

A repeating sequence of N values is periodic. The periodicity of the delta-sigma modulator output reduces the effectiveness of the delta-sigma modulator by introducing spurs [4] for this reason the sequence can be randomized. The process of randomizing the output of the delta-sigma modulator is called dithering and is implemented on many PLL chips. An example of dithering is shown in figure 2.9



(a) Without dithering.



(b) With dithering.

Figure 2.9: A PLL using an using fractional N division.

2.1.5. PLL Transfer Function

In the locked state, and by modelling the charge pump circuit as detailed in subsection 2.1.1, the PLL can be modelled as a linear time-invariant system with respect to phase [8]. Classical control theory is used to model the PLL.

The Forward loop gain of the transfer function of the PLL is given by

$$G(s) = \frac{K_{\mathrm{PD}}}{2\pi} T(s) \frac{2\pi K_{\mathrm{V}}}{s} \tag{2.4}$$

The open loop transfer function then:

$$G_{ol}(s) = \frac{K_{\mathrm{PD}}}{2\pi} T(s) \frac{2\pi K_{\mathrm{V}}}{s} \frac{1}{N} \tag{2.5}$$

Which equals

$$G_{ol}(s) = \frac{K_{PD} T(s) K_V}{sN} \tag{2.6}$$

Using equation 2.1 to fully expand the above equation yields:

$$G_{ol}(s) = \frac{K_{PD} K_V (sRC_2 + 1)}{s^2[sRC_1C_2 + (C_1 + C_2)]N} \tag{2.7}$$

The closed loop transfer function is given in equation 2.8

$$G_{cl}(s) = \frac{G(s)}{1 + G(s)\frac{1}{N}} \tag{2.8}$$

For convention take $H = \frac{1}{N}$

$$G_{cl}(s) = \frac{G(s)}{1 + G(s)H} \tag{2.9}$$

The closed loop transfer function of the error signal is given by

$$E(s) = \frac{1}{1 + G(s)H} \tag{2.10}$$

The gain cross-over frequency, s_{wc} of the $G(s)$ is the value for s such that $G(s_{wc}) = 1$. The phase margin of the system is the difference between the $-180°$ and the phase of $G(s)$ at s_{wc}.
The bandwidth of the system is the frequency for which $|G_{cl}(s_{\mathrm{BW}})| = \frac{1}{\sqrt{2}}|G_{cl}(0)|$. Typically this would be the $-3\,\mathrm{dB}$ of the closed loop transfer function, but the closed loop transfer function has a gain of N at baseband, not a gain of $0\,\mathrm{dB}$.

The gain cross-over frequency of $G(s)$ and the bandwidth are not necessarily equal, but are often close to equal, the following relation can be given: $s_{wc} \leq s_{\mathrm{BW}} \leq 2s_{wc}$, Which allows the bandwidth lines to be drawn in the graphs below [9].

$G(s)$ is monotonically decreasing with s. This allows the following two approximations:

$$\left|\frac{G(s)}{1+G(s)H}\right| \simeq \left|\frac{1}{H}\right| = N\,; \quad s << s_{wc} \tag{2.11}$$

and

$$\left|\frac{G(s)}{1+G(s)H}\right| \simeq |G(s)|\,; \quad s >> s_{wc} \tag{2.12}$$

Figure 2.10 shows a magnitude plot of the general shape of $G_{cl}(s)$.

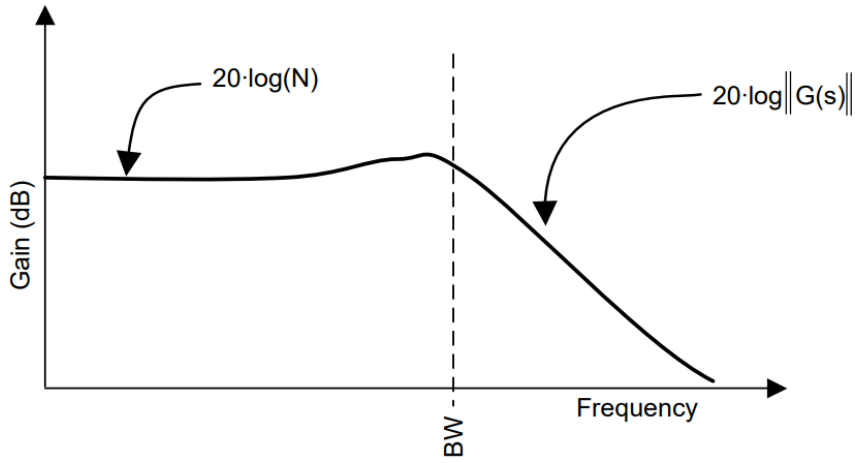


Figure 2.10: Bode magnitude plot of a Typical $G_{cl}(s)$ transfer function. [4]

Figure 2.11 shows a bode magnitude plot of $E(s)$. Again using the fact that $G(s)$ is monotonically decreasing with s yields:

$$\left|\frac{1}{1+G(s)H}\right| \simeq \frac{1}{|G(s)H|} = \frac{N}{|G(s)|}\,; \quad s << s_{BW} \tag{2.13}$$

and

$$\left|\frac{1}{1+G(s)H}\right| \simeq 1\,; \quad s >> s_{BW} \tag{2.14}$$

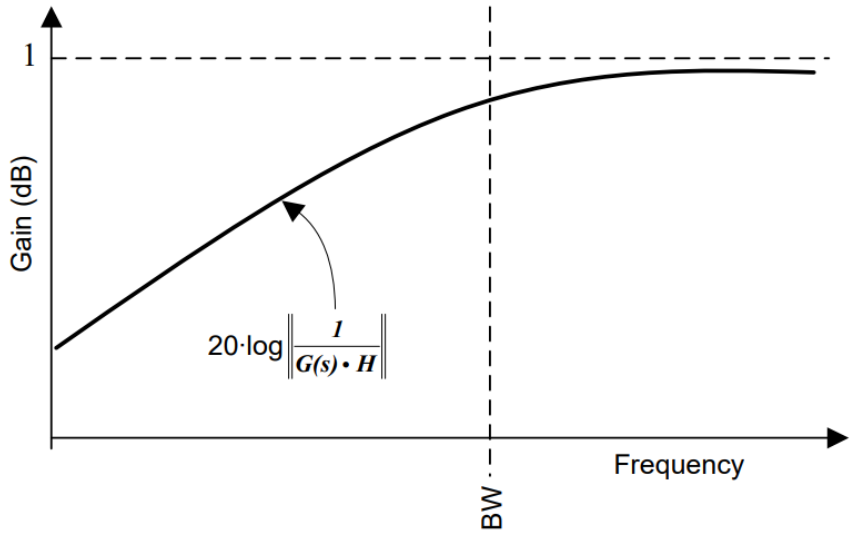


Figure 2.11: Bode magnitude plot of $E(s)$. [4]

The transfer function of $E(s)$ is worth noting because it shapes noise introduced by the VCO and the loop filter.

The loop bandwidth of the PLL is one of the most important design parameters. A PLL with a narrower loop bandwidth generally attenuates more phase noise however a broader loop bandwidth allows for a faster lock time. Lock time is of less concern for a fixed frequency LO than for a variable frequency LO. The closed loop transfer function of the PLL and the loop bandwidth both vary with N. A PLL designed to deliver a range of frequencies is designed at the geometric mean of the lowest and highest frequencies the PLL is expected to deliver, that is $f_{\text{design}} = \sqrt{f_{\text{min}} f_{\text{max}}}$. The gain of the charge pump circuit K_{PD} can be adjusted to compensate for the change of the value of the N divider should the loop bandwidth vary too much over the frequency range of the PLL.

Chapter 3

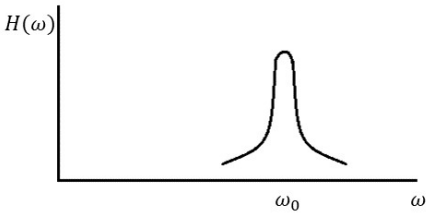
An introduction to phase noise

The following chapter will begin by introducing the concept of phase noise and then formalizing the definition of phase noise. The chapter continues describing how phase noise is modelled in the components of a PLL. Then the effect of phase noise in an interferometer is discussed.

3.1. Phase noise

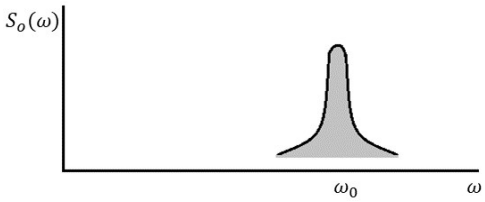
A single frequency sinusoid represented as a Dirac delta in the frequency domain is an idealisation. Any generated sinusoid or clock signal will suffer phase noise. Phase noise occurs when the spectral power of a generated clock signal is spread over a wider range than the desired frequency. Phase noise is a measure of deviation from true periodicity in a periodic signal

To see where phase noise may come from in an oscillator, consider the transfer function shown in figure 3.1a. This transfer function is a linear approximation of the closed loop transfer function of an oscillator. Standard noise present in all electronic circuits is shown in figure 3.1b. Figure 3.1c is the result of the multiplication of figure 3.1a with figure 3.1b and shows how the transfer function shapes the noise into phase noise. It is clear here that the phase noise occurs because the oscillator feedback loop is not ideal. It does not have an infinitely narrow bandwidth. More precise oscillators have a narrower closed loop transfer function [10] [8].



(a) A linear approximation of the closed loop transfer function of an oscillator.

(b) Spectral distribution of noise.



(c) Spectral output of an oscillator.

Figure 3.1: An example of how phase noise arises in oscillators

Furthermore, consider also the clock signal shown in figure 3.2. An exaggerated perturbation of the clock signal is shown. The change in the voltage of the signal shifts the phase of the clock signal, the signal then continues with the new phase offset. Thermal noise and other noise sources physically present as voltage perturbations of a clock signal and so cause small changes in the signal's phase which is phase noise.

Figure 3.3 shows the same occurrence, but in a clock signal from a ring oscillator, an oscillator with a higher slew rate. When perturbed at instance t_1 the perturbation decays before it can cause a phase shift. When perturbed at instance t_2 the perturbation causes phase noise. For this reason, clock signals with higher slew rates are less sensitive to amplitude noise becoming phase noise.

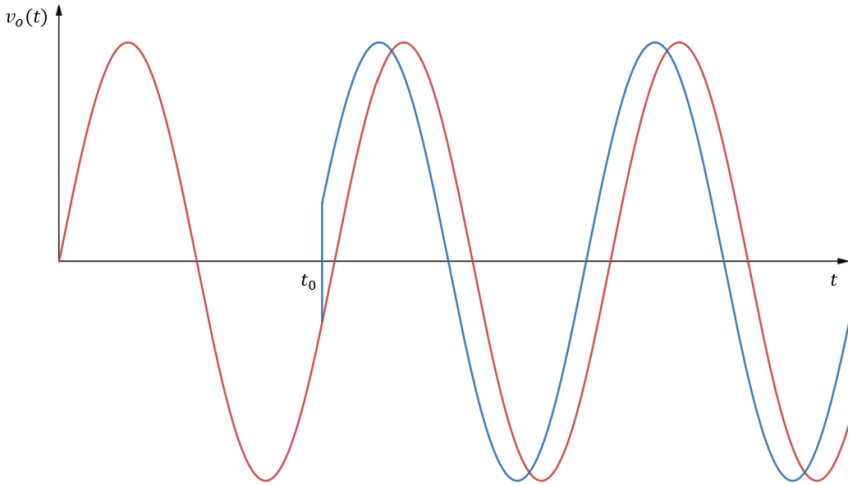


Figure 3.2: A sinusoid phase shift caused by amplitude perturbation.

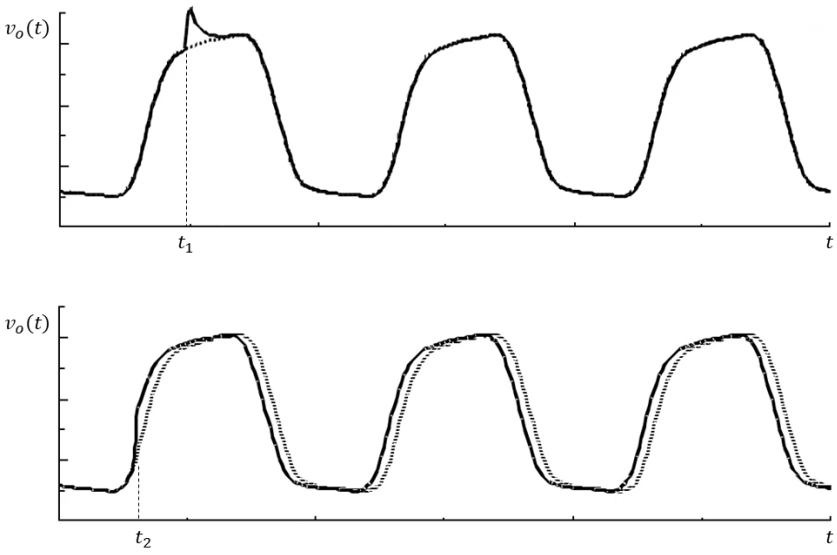


Figure 3.3: Disturbance of a high slew clock signal at two different time instances. [11]

To formalize the definition of phase noise take the generic signal.

$$c(t) = A\cos(2\pi f_c t + \phi(t)) \tag{3.1}$$

Where $\phi(t)$ is a non-stationary random process with a power spectral density $S_\Phi(f)$. As $\phi(t)$ is a real-valued signal $S_\Phi(f)$ contains the same information as $S_\Phi(-f)$ [12] For this reason phase noise is then defined as the single side band power spectral density of $\phi(t)$. Let $S'_\Phi(f)$ be the single side band power density function of $\phi(t)$. This means that $S'_\Phi(f) = 2S_\Phi(f)$ [13]. Finally the IEEE standard definition for phase noise is the power spectrum:

$$\mathscr{L}(f) = \frac{S'_\Phi(f)}{2} \tag{3.2}$$

where the factor of $\frac{1}{2}$ corrects for the fact that $S'_\Phi(f)$ represents two halves of the power spectrum of $S_\Phi(f)$. $\mathscr{L}(f)$ is expressed in dBc/Hz and represents the phase noise spectral power density relative to the carrier signal, normalized to 1 Hz bandwidth and is conventionally plotted on a log-log scale as seen in figure 3.4.

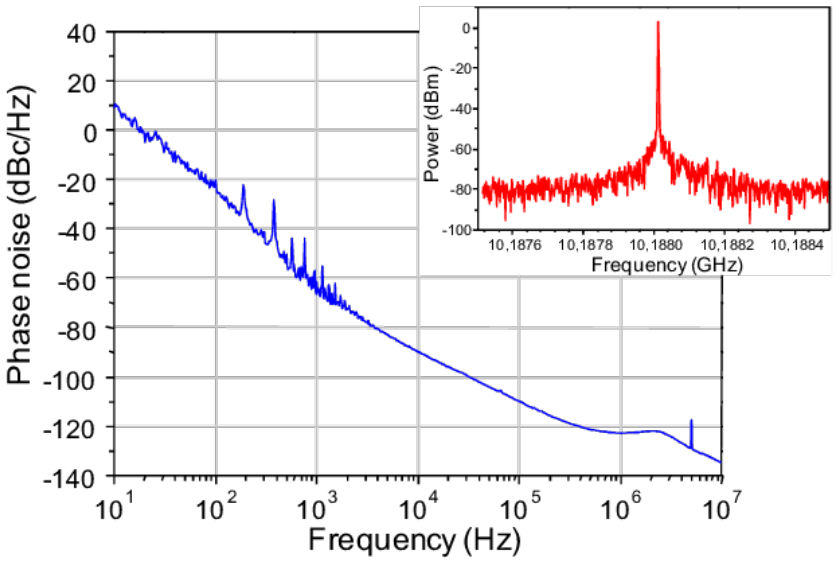
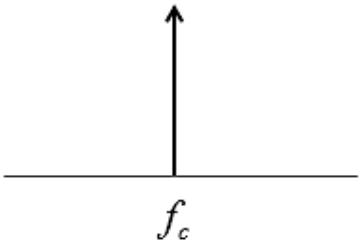


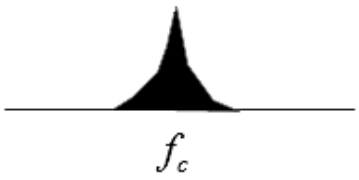
Figure 3.4: A typical phase noise spectrum with the signal spectrum shown in the corner. [14]

Figure 3.4 shows the phase noise relative to the carrier going above 0 dB. This can happen because phase noise is defined by the the power spectrum of the random process $\phi(t)$ not the power spectrum of the signal $c(t)$.

The frequency variations in $c(t)$ are the variations that cause the frequency spectrum $\mathscr{F}(c(t)) = C(f)$ to deviate from the Dirac delta idealization, illustrated in figure 3.5.



(a) Ideal clock frequency spectrum.



(b) Clock frequency spectrum with phase noise.

Figure 3.5: Frequency domain representation of phase noise

For this reason it is important to show how $\phi(t)$ modulates $c(t)$. Beginning with:

$$c(t) = A\cos(2\pi f_c t + \phi(t)) \tag{3.3}$$

expanding the trigonometric term yields,

$$c(t) = A[\cos(2\pi f_c t)\cos(\phi(t)) - \sin(2\pi f_c t)\sin(\phi(t)))] \tag{3.4}$$

Using the condition: $\phi(t) << 1$, and the small angle approximations.

$$c(t) = A[\cos(2\pi f_c t) - \phi(t)\sin(2\pi f_c t))] \tag{3.5}$$

Consider now only a narrow portion of the bandwidth of $\phi(t)$, $\phi(t) = a_m \sin(2\pi f_m t)$, yields:

$$c(t) = A[\cos(2\pi f_c t) - a_m \sin(2\pi f_m t)\sin(2\pi f_c t)] \tag{3.6}$$

$$c(t) = A\cos(2\pi f_c t) - \frac{a_m}{2}[\cos(2\pi(f_c - f_m)t) - \cos(2\pi(f_c + f_m)t)] \tag{3.7}$$

This shows how variation in $\phi(t)$ creates signal variance in $c(t)$ through phase modulation.

Phase noise represented in the time domain is called jitter, illustration in figure 3.6. Jitter is often used to deal with concerns of precision in clock signals when zero-crossing stability is of particular importance; for example sampling coherence or high-speed digital communication [15] [16]. A common graphical measure of jitter is an eye diagram, which is an overlay of multiple samples of the same clock signal over time, see figure 3.7. A broader eye diagram is caused by larger amounts of jitter than a narrower eye diagram.

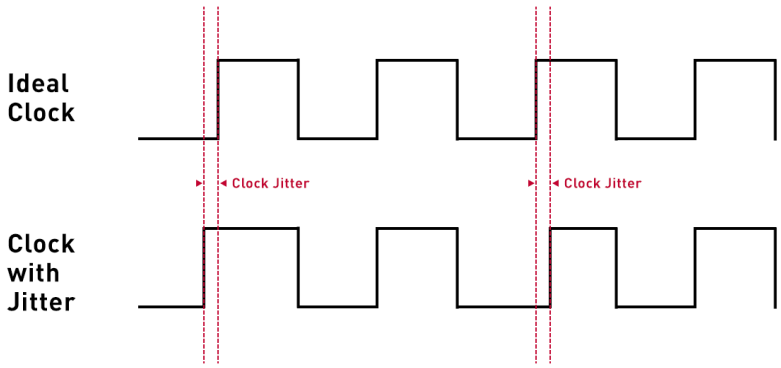


Figure 3.6: A clock signal with and without jitter. [17]

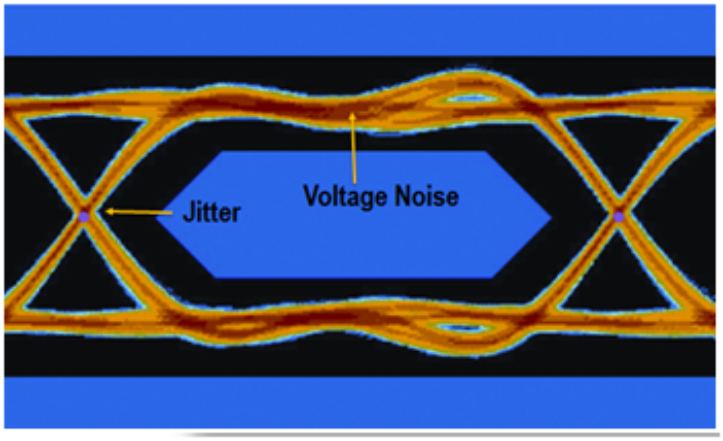


Figure 3.7: An eye diagram showing jitter. [18]

A useful measure of phase noise is integrated phase noise. The phase noise profile provides insight, but a single number can be derived for simple comparison purposes.

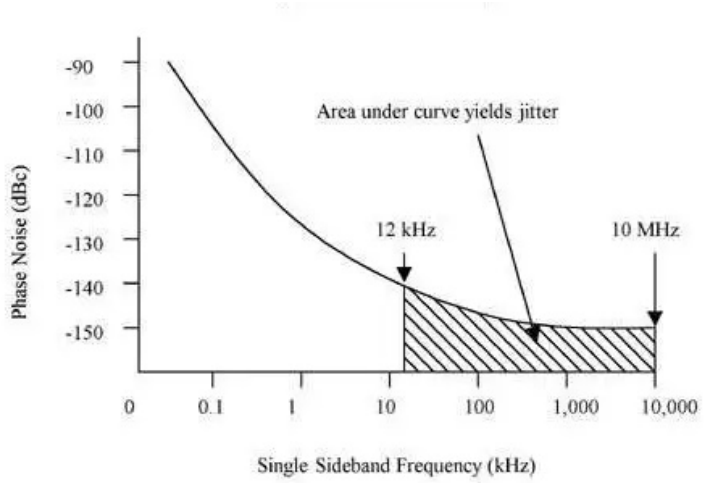


Figure 3.8: Area integrated under the phase noise curve yields jitter. [19]

To derive such a number we begin by integrating over a portion of the phase noise curve [15].

$$A = \int_a^b \mathscr{L}(f)\, df \tag{3.8}$$

$\sigma_\phi = \sqrt{A}$ represents the RMS phase error caused by the integrated phase noise. The RMS phase error can be converted to RMS time error by setting:

$$\sigma_t = \frac{\sigma_\phi}{f 2\pi} \tag{3.9}$$

The RMS time error is the jitter of the signal over the integrated bandwidth. The notation is also suggestive. It is true that cycle-to-cycle jitter is the variance of $\phi(t)$ [20].

3.2. Phase noise in a PLL

Phase noise in a Phase-locked loop is introduced by different sub-systems in the phase-locked loop. The noise introduced by each sub-system is modelled differently according to the power spectrum they introduce. The noise introduced by a given sub-system sees a specific path to the output of the PLL, the different transfer functions of the PLL shape the noise introduced by each sub-system in accordance with equation 3.10.

$$S_{\text{out}}(f) = |H(f)|^2 S_{\text{in}} \tag{3.10}$$

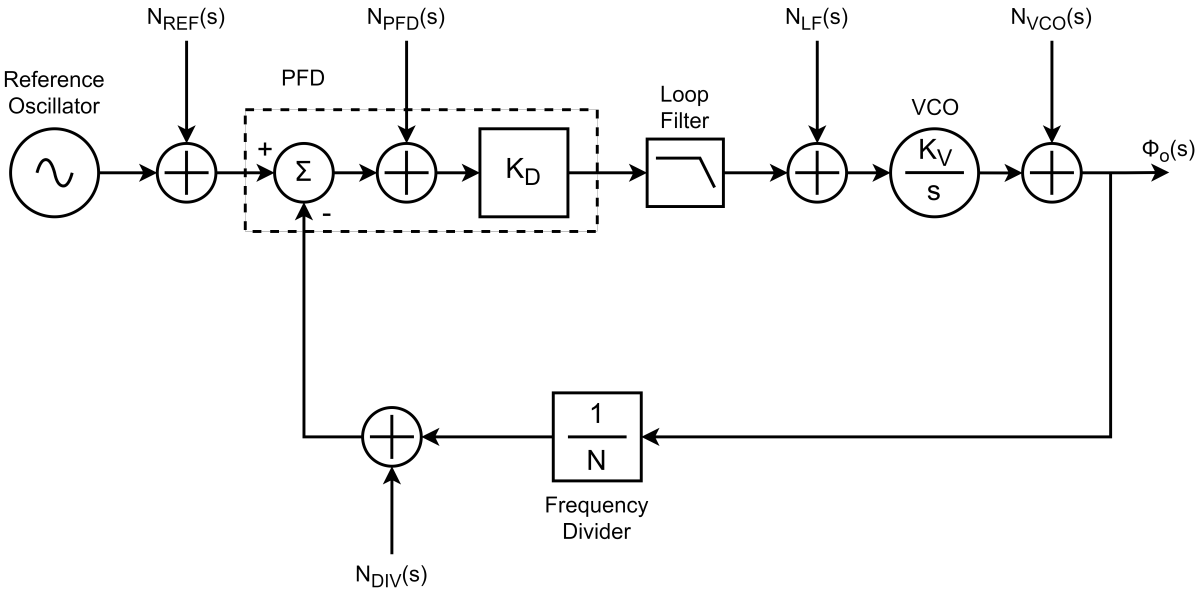


Figure 3.9: PLL modelled with injected noise sources.

The phase noise introduced by the reference oscillator, the phase frequency detector and the delta-sigma modulator are all shaped by the closed loop transfer function $G_{cl}(s)$ [21] [22]. Voltage noise introduced by the loop filter modulates the VCO and creates phase noise [23]. Both the phase noise inherent to the VCO and the phase noise created by the loop filter modulating the VCO are shaped by the error signal transfer function $E(s)$ [21] [22].

3.2.1. Reference Oscillator phase noise in a PLL

The power spectral density of an oscillator commonly takes on the shape shown in figure 3.10. Analogous to voltage flicker noise in most circuits the oscillator spectrum has multiple $\frac{1}{f^n}$ corner frequencies. As the offset from the carrier decreases the noise power per decade per decade of the phase noise increases. That is, for the $\frac{1}{f^2}$ region, there is 10 times as much noise power in the the decade between 10 Hz and 100 Hz than the decade between

100 Hz and 1000 Hz; and for the $\frac{1}{f^3}$ region there is 100 as much noise power in the decade between 1 Hz and 10 Hz than there is between the decade 10 Hz and 100 Hz [12]. This is to say the higher order $\frac{1}{f^n}$ noise dominates the phase noise at low offset frequencies.

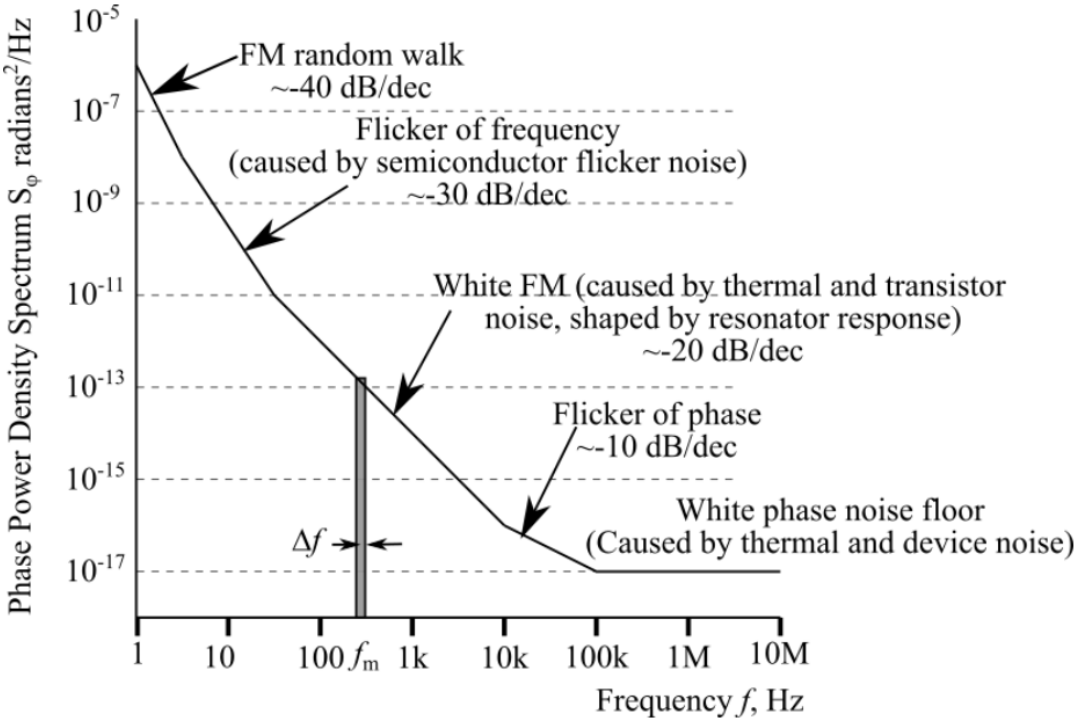


Figure 3.10: Typical power spectral density of the phase noise in an oscillator. [12]

The different noise colours are caused by the up-mixing to the carrier and inter-modulation around the carrier of different noise sources present in the oscillator circuit [12] [24].

Table 3.1: Flicker phase noise within an oscillator.

	Noise label	Noise source
f	White Phase	Thermal noise.
f^{-1}	Flicker Phase	Flicker noise that has been up-mixed to the carrier frequency.
f^{-2}	White Frequency Modulation	Thermal noise and flicker noise shaped by the oscillator transfer function.
f^{-3}	Flicker Frequency	Noise caused by the inter-modulation of Flicker phase noise and White FM noise.
f^{-4}	Random Walk	Intrinsic variance of time and temperature in the quartz crystal and electrode structure within the oscillator.

Oscillator phase noise is often modelled using the semi-empirical Leeson-Cutler model given by equation 3.11.

$$\mathscr{L}(f_m) = \frac{1}{2}\left(\frac{FkT}{P_a}\right)\left(\frac{f_0}{2Q_l f_m} + 1\right)\left(\frac{f_c}{f_m} + 1\right) \tag{3.11}$$

Where:

- F is the noise figure of the active device used to provide a negative impedance of the oscillator.
- k is Boltzmann's constant, T is the temperature.
- P_a is the signal power available at the input of the active device used in the oscillator.
- f_0 is the desired output frequency of the oscillator.
- Q_l is the loaded quality factor of the resonator within the oscillator.
- f_m is the offset frequency at which the equation is being evaluated and
- f_c is the $\frac{1}{f}$ corner frequency at which the power spectrum of the active device, in the configuration it is to be used in the oscillator, shows flicker noise.

Reference oscillator phase noise is shaped by the closed loop transfer function of the PLL. Within the loop bandwidth the reference oscillator phase noise will be multiplied by the factor N.

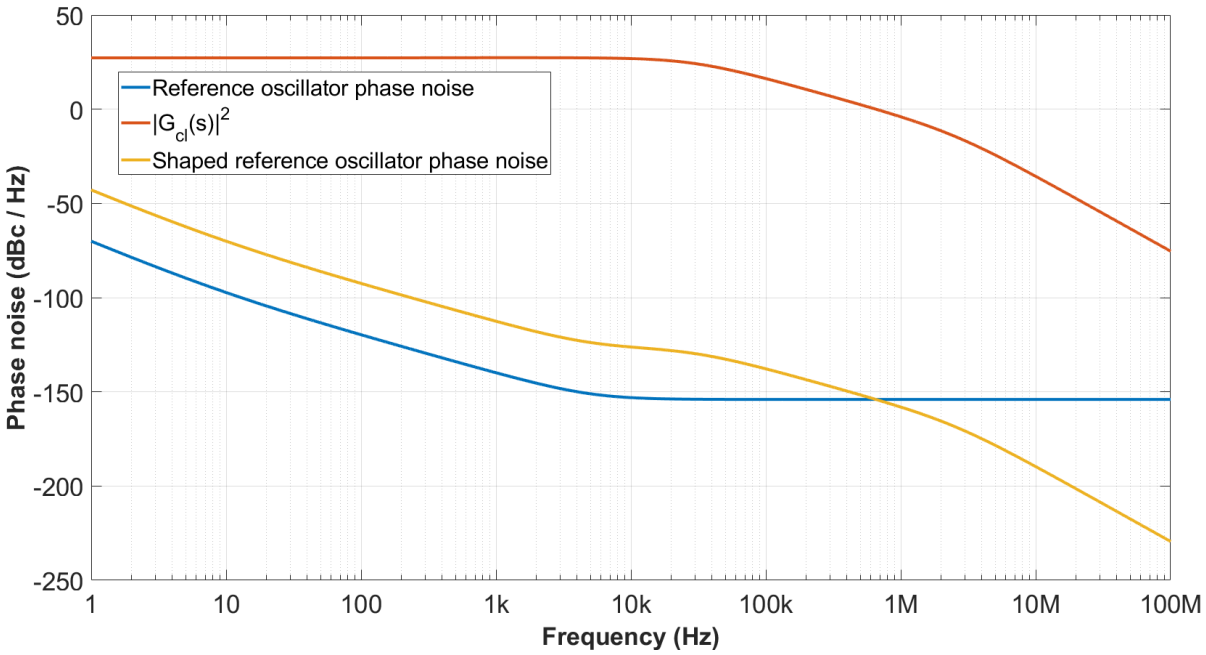


Figure 3.11: Reference oscillator phase noise being shaped by the close loop transfer function of a PLL.

3.2.2. Chip noise in a PLL

The phase noise introduced by the Phase frequency detector and the Charge pump, are modelled together as the phase noise introduced by the PLL chip: $N_{PFD}(s)$. The PLL chip noise has a phase noise floor and flicker noise.

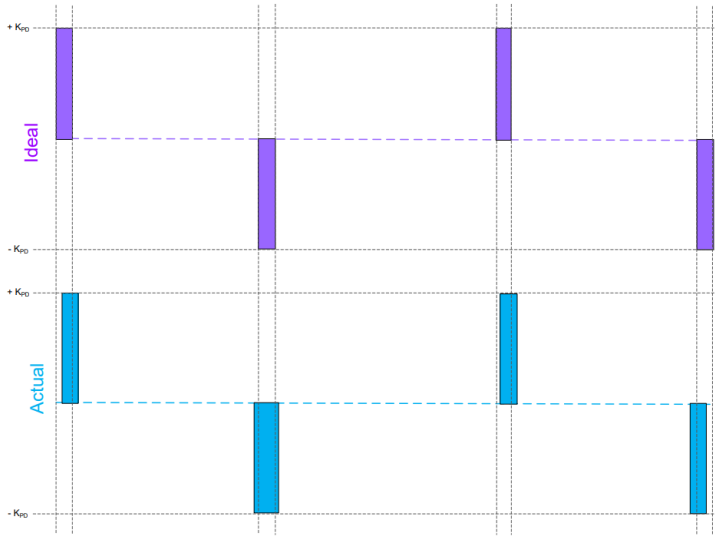


Figure 3.12: Ideal vs Actual charge pump current pulses. [4]

Chip phase noise is injected into the phase-locked loop at each pulse of the Charge pump. Each charge pump pulse introduces a portion of phase noise that is correlated with the phase noise present in other charge pump pulse instances and a portion that is uncorrelated with the phase noise present in other charge pump pulse instances [4]. Flicker phase noise is pink noise which has correlation across instances and the phase noise floor is white noise, which does not.

$$\mathrm{Var}(\sum_{i=1}^{n} X_i) = \sum_{i=1}^{n}\sum_{j=1}^{n} \mathrm{Cov}(X_i, X_j) \tag{3.12}$$

$$\sum_{i=1}^{n}\sum_{j=1}^{n} \mathrm{Cov}(X_i, X_j) = \mathrm{Var}(\sum_{i=1}^{n} X_i) + 2(\sum_{1\le i\le j\le n} \mathrm{Cov}(X_i, X_j)) \tag{3.13}$$

The sum of the variance - and therefore the sum of the energy - of n instances of a Gaussian random process can be calculated using equation 3.12. Where i and j denote an instance of the random process. In equation 3.13 if the covariance between any i and j where $i \neq j$ is zero, the equation simplifies to $\mathrm{Var}(\sum_{i=1}^{n} X_i)$ and because X_i and X_{i+1} have the same statistical properties $\mathrm{Var}(\sum_{i=1}^{n} X_i)$ becomes $n\mathrm{Var}(X_i)$. The power of the sum grows with $10\log(n)$.

If there is a correlation between any instance i and any instance j, and because any X_i and X_j have the same statistical properties, equation 3.12 becomes $n^2\mathrm{Var}(X_i)$ and the power of the sum grows with $20\log(n)$.

n is the number of noise samples between each consecutive pulse of the reference clock at the input of the phase frequency detector [4], that is $n = f_{\mathrm{PFD}}$ and $f_{\mathrm{PFD}} = f_{\mathrm{REF}}$, the noise power of uncorrelated noise power will grow at $10\log(f_{\mathrm{PFD}})$ and correlated noise power will grow at $20\log(f_{\mathrm{PFD}})$

A PLL chip will have two figures of merits (FOM) specified in its datasheet. One for the flicker noise region and one for the flat noise region. Both are determined by measuring the phase noise the chip introduces, accounting for f_{PFD} and accounting for the transfer function shaping the phase noise of the measurement. These two figures of merit characterise the chip noise.

The phase noise floor introduced by the chip before being shaped by the feedback loop is $N_{\text{chip floor}}$, with:

$$\mathscr{L}_{\text{chip floor}} = \mathrm{FOM}_{\text{chip floor}} + 10\log(f_{\mathrm{PFD}}) \tag{3.14}$$

and the flicker phase noise by the chip before being shaped by the feedback loop is $N_{\text{chip flicker}}$, with

$$\mathscr{L}(f_m)_{\text{chip flicker}} = \mathrm{FOM}_{\text{chip flicker}} + 20\log(f_{\mathrm{PFD}}) - 10\log(f_m) \tag{3.15}$$

where f_m is the offset frequency. The third term in equation 3.15 accounts for the shape of the flicker noise. Increasing the gain of the charge pump increases the signal-to-noise ratio at the output of the charge pump circuit. Both the FOM of flicker and the FOM of the floor of the chip improve as the gain of the charge pump increases.

The flicker phase noise and the phase noise floor both deteriorate as a function of f_{PFD}. The output frequency of the VCO is $f_o = Nf_{\mathrm{PFD}}$. For a set output frequency decreasing f_{PFD} requires inverse proportionally increasing N. The chip noise is shaped by the closed loop transfer function of the PLL whose baseband gain is N, which is an addition of $20\log(N)$ on the phase noise power spectrum. For this reason decreasing f_{PFD} yields no benefit in the case of the chip flicker phase noise and is of negative benefit for the chip phase noise floor.

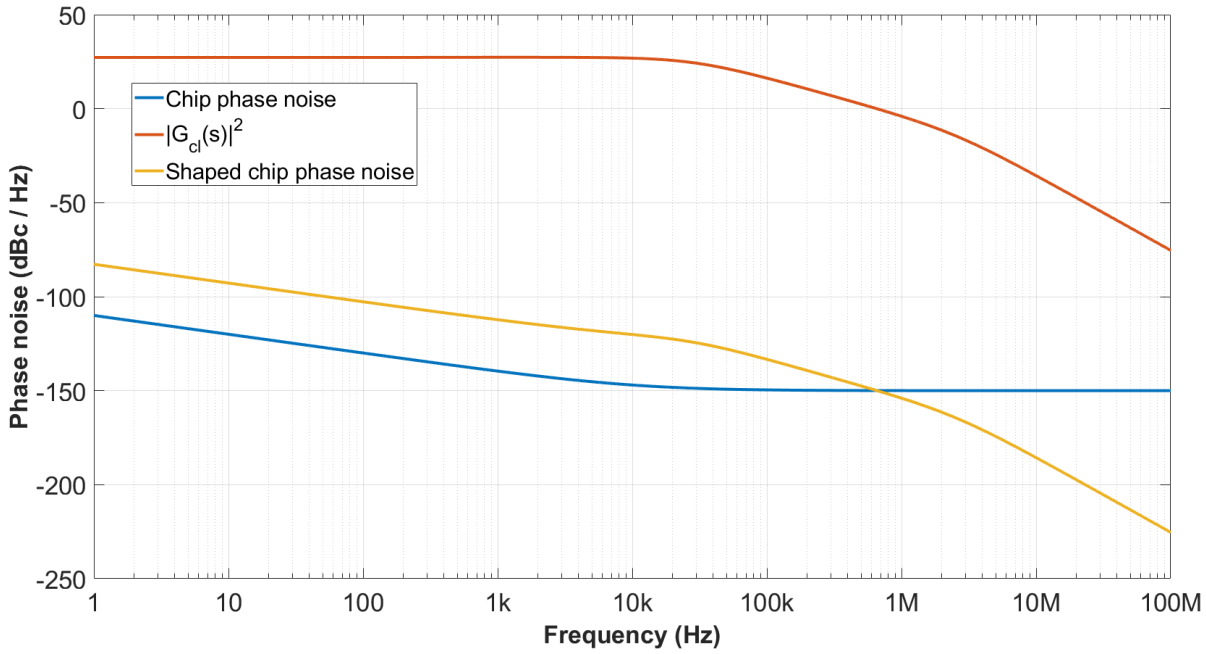


Figure 3.13: Phase noise introduced by the PLL chip being shaped by the close loop transfer function of a PLL.

3.2.3. Resistor Filter noise in a PLL

Many different filter architectures can be used to implement the loop filter in a PLL. The output of an active filter can have a larger voltage range than that of a passive filter making it suitable for use with a VCO which has a large input tuning range. The active component in an active filter will both introduce flicker noise and raise the noise floor. Additional resistors introduce additional thermal noise which introduces phase noise [23] [4]; often the simplest loop filter is the most effective [3].

The second order passive loop filter as seen in figure 2.4 is used in all the PLLs in this report. The RMS voltage caused by the thermal noise introduced by Resistor R_2 can be modelled by introducing a noise source as shown in figure 3.14. Where

$$V_{\mathrm{R2}} = \sqrt{4T_0 K \mathrm{R}_2} \tag{3.16}$$

Within a 1 Hz bandwidth.

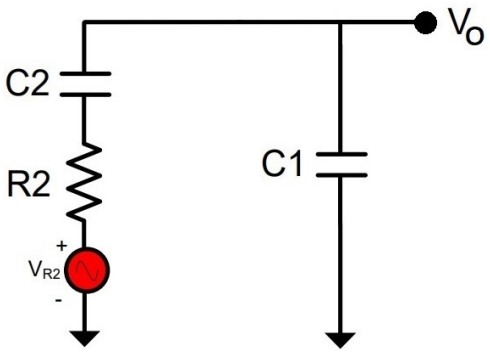


Figure 3.14: Voltage circuit for modelling the loop filter noise. [4]

The transfer function from the introduced thermal noise to the input of the VCO is:

$$\frac{V_{\mathrm{o}}(s)}{V_{\mathrm{R2}}(s)} = \frac{\mathrm{C}_2}{s\mathrm{C}_1\mathrm{C}_2\mathrm{R}_2 + (\mathrm{C}_1 + \mathrm{C}_2)} \tag{3.17}$$

An example of the voltage noise present at the input of the VCO is shown in figure 3.15

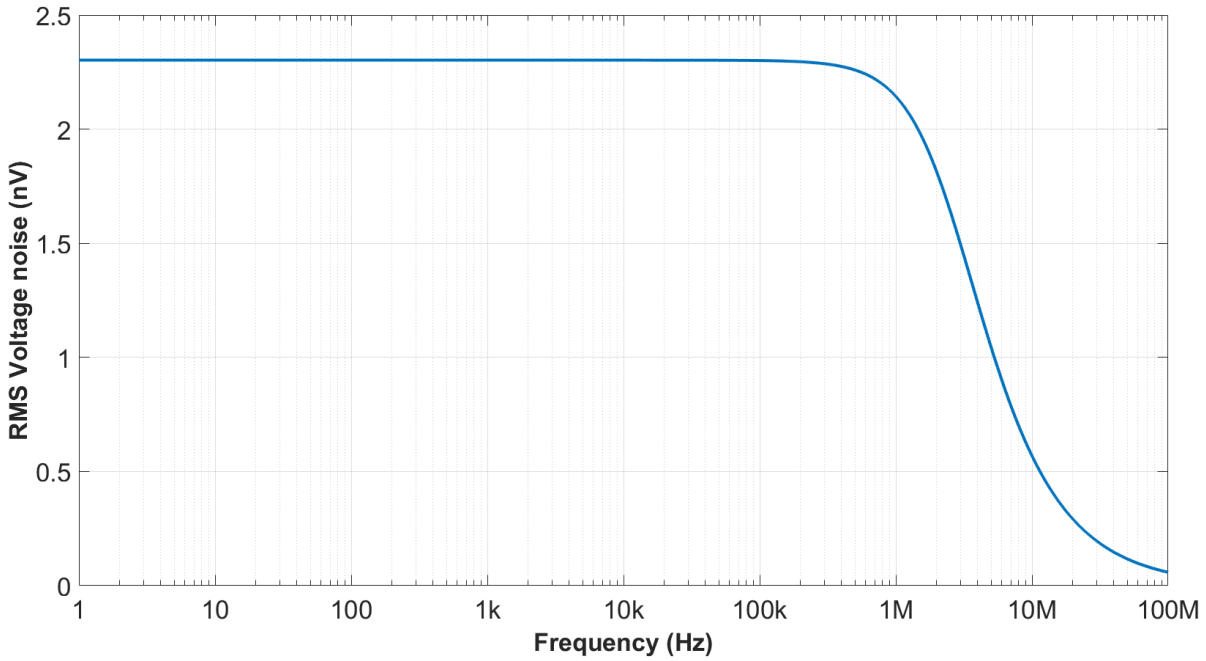


Figure 3.15: R_2 shaped by the loop filter.

The voltage noise then modulates the VCO input. Take $V_o(f_m)$, a small portion of the bandwidth of $V_o(f)$, as a single tone sinusoid with a frequency of f_m and an amplitude of $\sqrt{2}V_o(f_m)$, The modulated VCO output can then be represented with equation 3.18 [25].

$$y(t) = A_c \cos[2\pi f_c t + \frac{f_\Delta}{f_m} \sin(2\pi f_m t)] \tag{3.18}$$

With $f_\Delta = \sqrt{2}V_o(f_m)K_{\mathrm{V}}$.

For convention set $\frac{f_\Delta}{f_m} = \beta$. The Fourier decomposing of $y(t)$ is given in equation 3.19 [25].

$$y(t) = A_c \sum_{-\infty}^{\infty} J_n(\beta) \cos(2\pi f_c t + n2\pi f_m t) \tag{3.19}$$

Where J_n is the n^{th} bessel function of the first kind. For small values of β, which is guaranteed by the order of magnitude of $v_o(t)$, $J_0(\beta) \approx 1$, $J_1(\beta) \approx \frac{\beta}{2}$, and all other instances of $J_n(\beta)$ are negligibly small.

The amplitude of the carrier component is of $y(t)$ is A_c and the amplitude of the component caused by modulation is $A_c\frac{\beta}{2}$. Phase noise is defined as spectral power relative to the carrier which is then $20\log(\frac{\beta}{2})$

Finally the phase noise introduced by the resistor is $20\log(\frac{\sqrt{2}V_o(f_m)K_V}{2f_m})$.
This phase noise is then shaped by the error signal of the PLL as shown in figure 3.16.

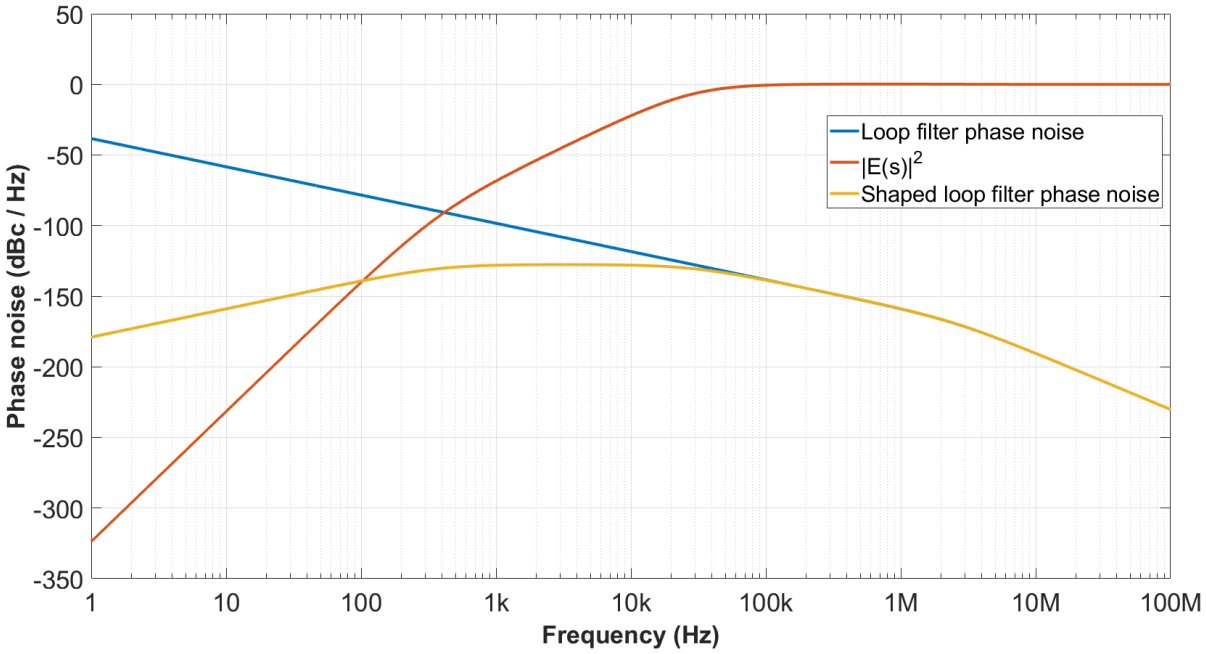


Figure 3.16: Phase noise introduced by loop filter voltage noise being modulating the output of the VCO shaped by the error transfer function of a PLL.

3.2.4. VCO phase noise in a PLL

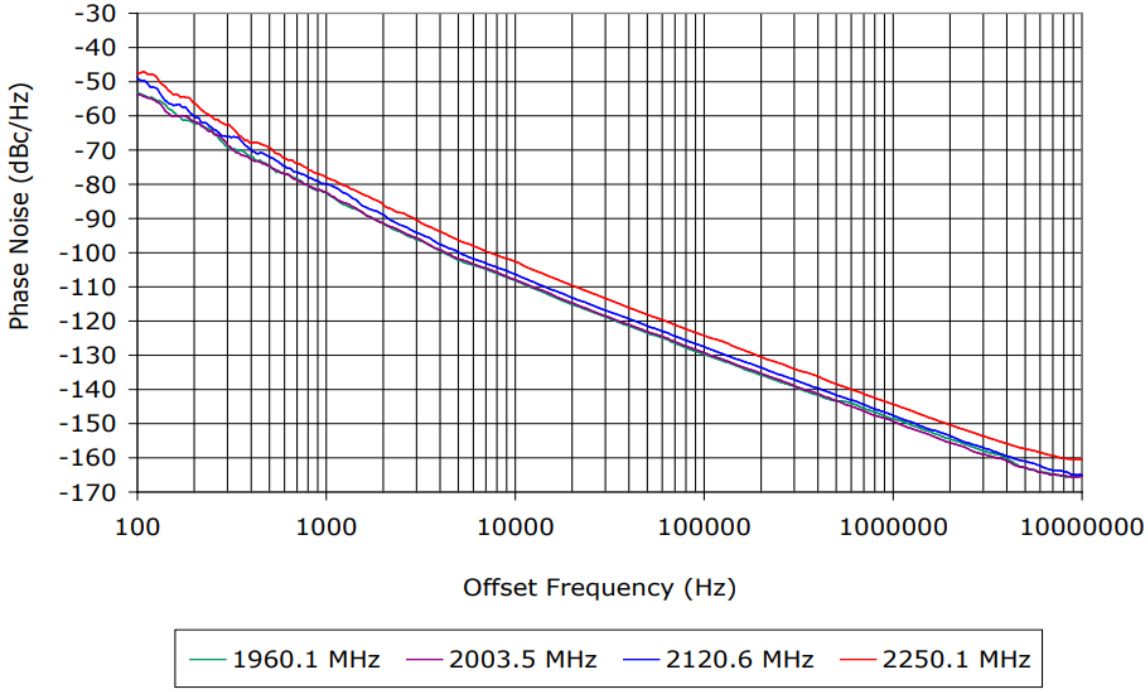


Figure 3.17: VCO phase noise. [6]

The VCO introduces phase noise of the same shape as the reference oscillator and can be modelled similarly. Figure 3.17 shows the typical phase noise graph of a VCO. The phase noise of the VCO at low offset frequencies is attenuated by the error transfer function of the PLL.

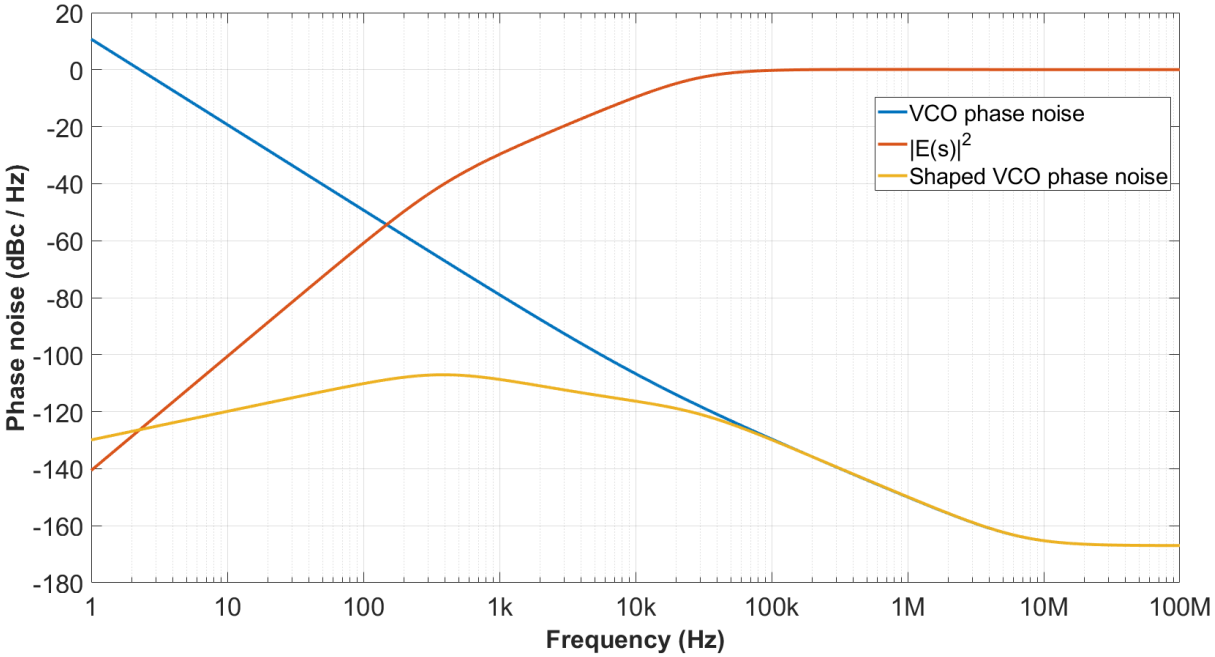


Figure 3.18: VCO phase noise being shaped by the close loop transfer function of a PLL.

3.2.5. Delta-sigma modulator noise in a PLL

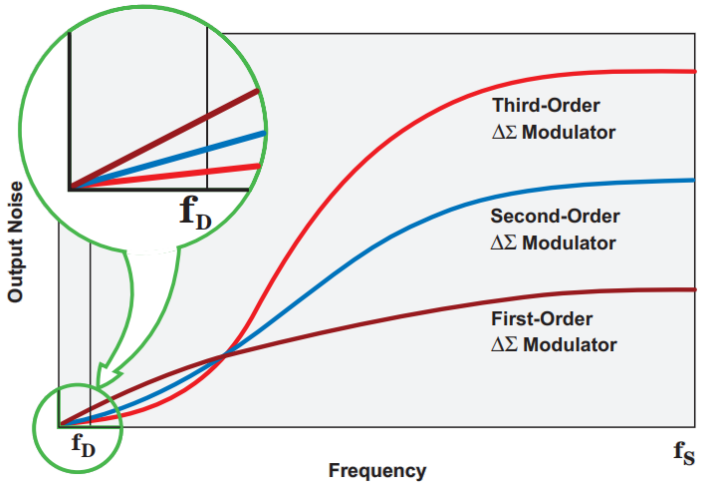


Figure 3.19: The quantization noise shaping curve of different order delta-sigma modulators. [26]

The delta-sigma modulator shapes quantization noise introduced by a fractional N division. This effectively removes quantization spurs [7]. Figure 3.19 shows the noise shaping profile of different order DSM. The DSM uses over-sampling and a high pass filtering function inherent to the DSM circuit to shift noise power introduced by fractional division to higher offset frequencies. At the higher offset frequencies the closed loop transfer function of the PLL attenuates the noise power. The noise introduced by the DSM as it removes spurs first peaks at roughly $\frac{f_{\mathrm{PfD}}}{2}$ and has a peak lobe level that can be approximated with $6(order) - 10\log(f_{\mathrm{PD}}) - 0.8$ [4]. A typical phase noise profile created by a different order DSM is shown in figure 3.20. The first lobe is typically the only one with a low enough offset frequency to present itself within the loop bandwidth.

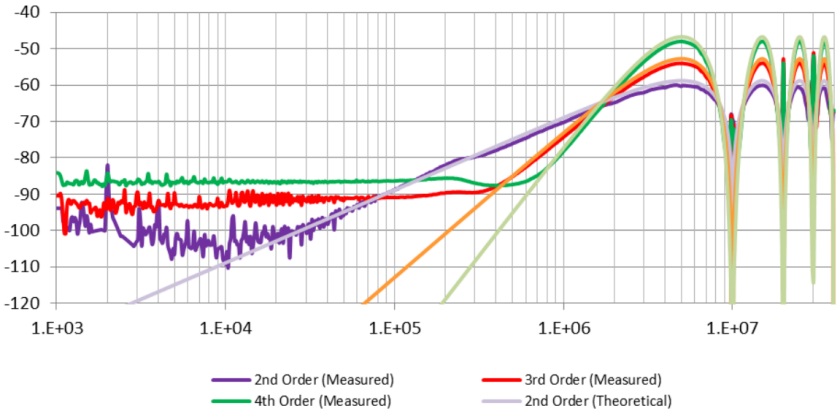


Figure 3.20: Phase noise curve created by the DSM. [4]

Selecting a reference oscillator with a high frequency has the benefit of rendering DSM phase noise close to negligible. By way of example, The noise introduced by a DSM when using a 100 MHz reference clock will be concentrated around a 50 MHz offset frequency with a peak power of around $-62.8\,\mathrm{dBc\,Hz^{-1}}$. At this offset frequency the gain of the closed loop transfer function of a PLL is usually around $-90\,\mathrm{dB}$. The total contribution of the DSM is then $-152.8\,\mathrm{dBc\,Hz^{-1}}$ which is near the phase noise floor of the VCO.

Figure 3.21 displays a typical phase noise graph with the shaped contribution of the reference oscillator, the PLL chip, the VCO and the loop filter.

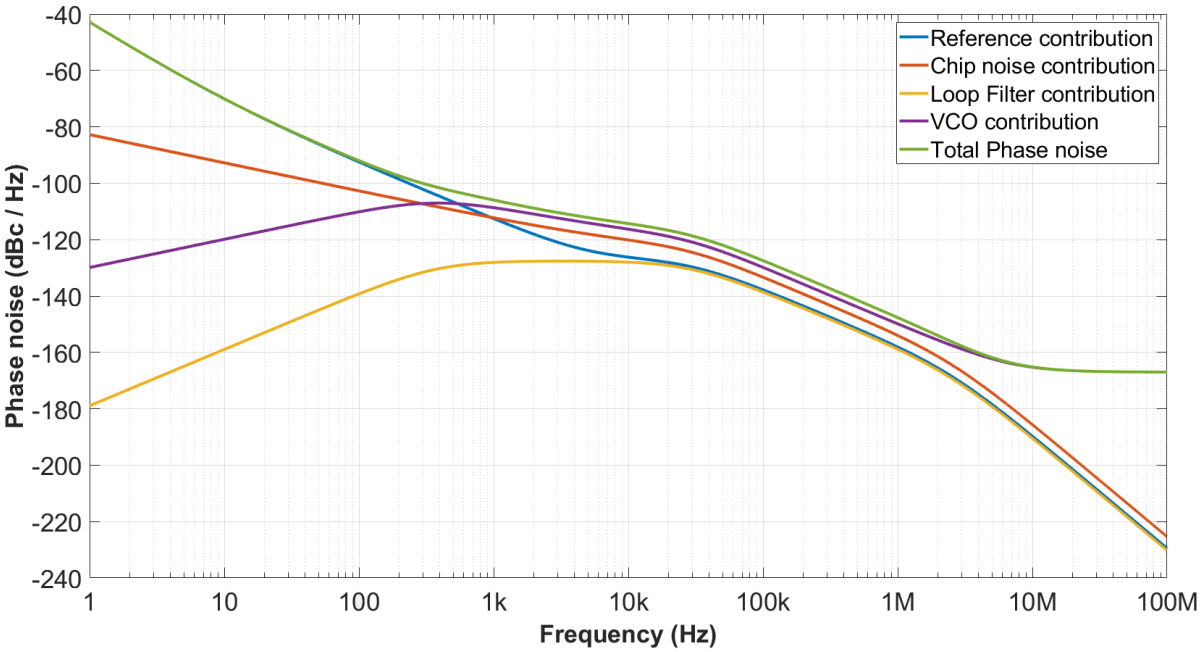


Figure 3.21: Typical phase noise curve for a PLL showing the shaped contributions of all PLL components.

3.3. Phase noise in a radiometer and interferometer

In a radiometer phase noise effectively degrades the jitter performance of the ADC sampling the output of the radiometer. It can be shown that the SNR of the receiver is degraded by $20\log(\frac{1}{2\pi f_c t_j})$ where f_c is the carrier frequency of the LO and t_j the RMS jitter of the LO [15]. Large amounts of phase noise at low frequency offsets also decrease the maximum resolution of a radiometer [15].

The output of an interferometer before image processing is the Visibility function. The visibility function is a two dimensional spatial Fourier transform of the sky brightness distribution [27].

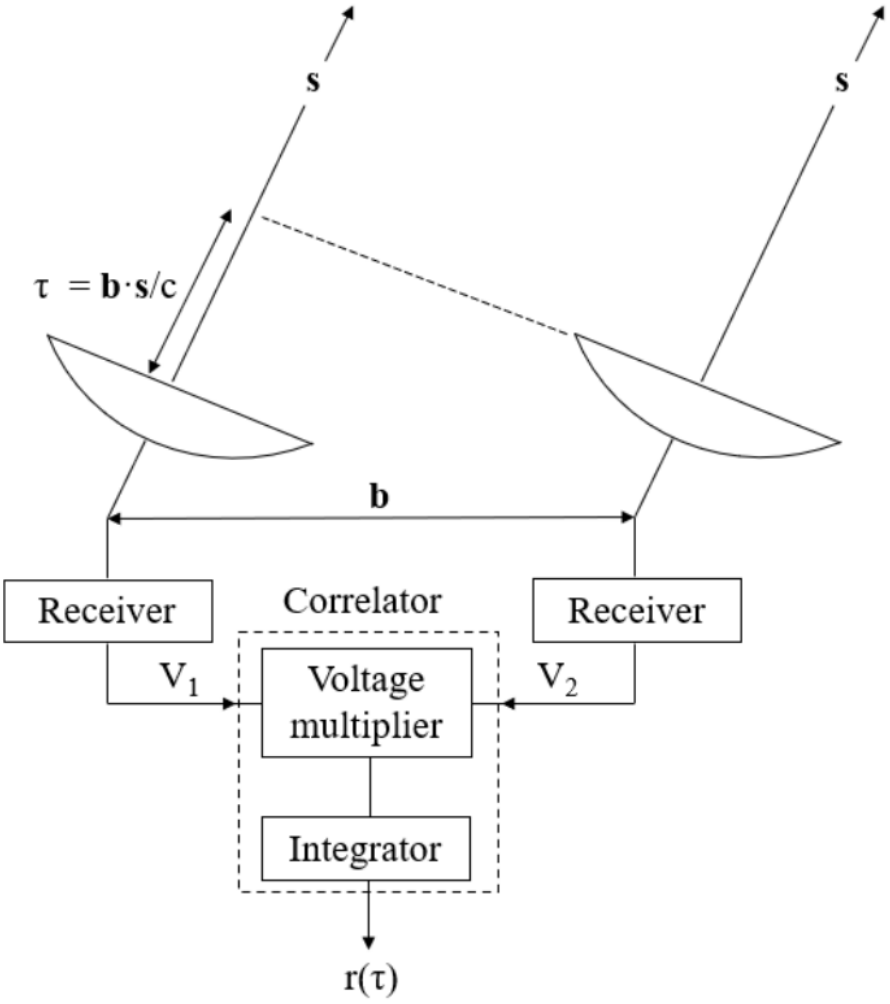


Figure 3.22: Two antenna interferometer. [28]

The visibility function between any two antennae is the complex cross-correlation of the signals received by the antenna. with:

$$V_{12} = \langle V_1(t), V_2(t) \rangle = \frac{1}{T} \int_0^T V_1(t) V_2(t)^* dt \tag{3.20}$$

With $V_1 = A_1(t) \angle e^{j\tau + j\phi_{LO1}}$ and $V_2 = A_2(t) e^{jLO2}$. with ϕ_{LO1} and ϕ_{LO2} being expanded as $\phi_{LO1} = \phi^{j2\pi f_c t + j\phi_{n1}(t)}$ and $\phi_{LO2} = \phi^{j2\pi f_c t + j\phi_{n2}(t)}$ [29] [30]. Where ϕ_{n1} is the phase noise present in LO1 and ϕ_{n2} is the phase noise present in LO2. The conjugate multiplication of $V_1(t)$ and $V_2(t)$ is then $A_1 A_2 e^{j\tau + j[\phi_{n1}(t) - \phi_{n2}(t)]}$. Phase noise correlated between LO1 and LO2 will subtract from one another and cause no image errors [30]. Uncorrelated phase noise will produce errors that distort the value of $e^{j\tau}$ [29] [30]. τ is the angle at which the beam of the two antennas is directed. Errors in τ present as errors in image location when imaging the sky with an interferometer [27]. Finally consider what happens when time averaging $\Delta\phi_n(t) = \phi_{n1}(t) - \phi_{n2}(t)$ which is:

$$\frac{1}{T} \int_0^T \phi_{n1}(t) - \phi_{n2}(t) dt \tag{3.21}$$

The integration will average out higher frequency components of $\Delta\phi_n(t)$ over a shorter integration period T [29] [30]. In an interferometer phase noise uncorrelated between radio receivers at low offset frequencies can cause large imaging errors as the phase noise is neither subtracted out nor integrated out during cross-correlation.

Commonly when using a PLL for frequency synthesis the reference oscillator signal is distributed to multiple PLL chips which each generate an instance of the desired LO. In such a scheme the reference oscillator phase noise is correlated across all LO instances and the uncorrelated phase noise at low offset frequencies is dominated by the phase noise introduced by the PLL chip, as shown in figure 3.21. If the LO signal itself is distributed, as is done in one of the designs in this report, the only uncorrelated phase noise in the system is the phase noise introduced by the clock buffers distributing the LO. Phase noise introduced by a PLL chip is scaled by the closed loop function of the PLL and will be much larger than phase noise introduced by a clock buffer.

Chapter 4

Design Considerations

This chapter details the requirements of the LO synthesizers. The chapter then introduces two designs to meet these requirements. For each LO synthesizer, some important components and design considerations are then detailed and discussed.

4.1. Overview

The antenna array will consist of 16 elements. Each element measures two polarizations; to sample both polarizations requires 32 radio channels. This requires 32 instances of the fixed frequency LO and 32 instances of the variable frequency LO. The frequency of the fixed frequency LO is 2.3 GHz and the frequency of the variable frequency LO is from 2.975 GHz to 3.975 GHz. The geometric mean of the frequency range of the variable frequency LO is 3.439 GHz; this is the frequency at which the PLLs generating the variable frequency LO are designed and measured. The active mixers used on the radio can accept an LO input power ranging from −6 dBm to 6 dBm.

4.1.1. Design 1: High frequency clock distribution

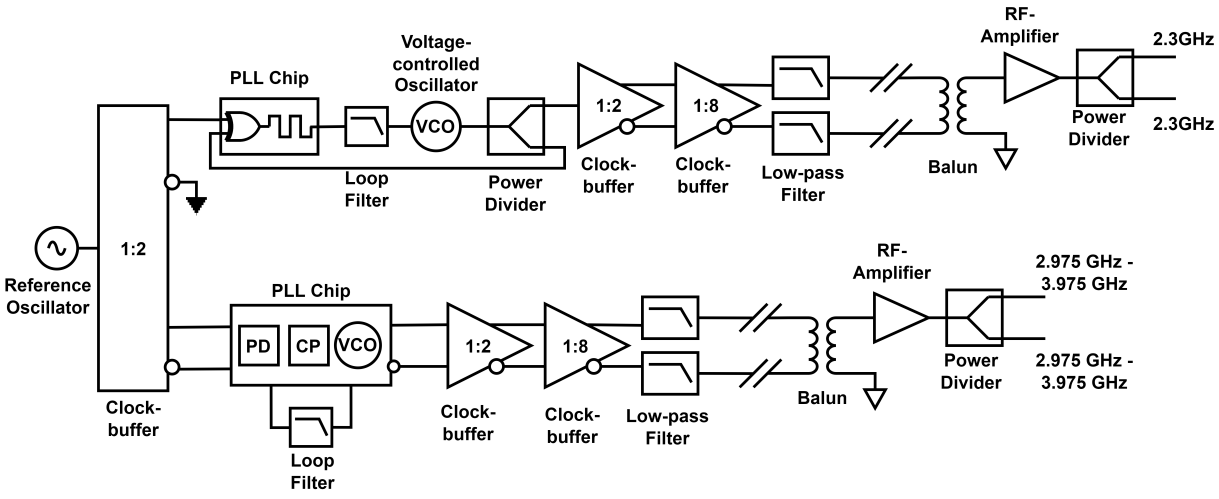


Figure 4.1: Block diagram of design 1.

In Design one, shown in figure 4.1, two different PLL chips are used to create the required LOs. The first PLL chip creates the fixed frequency LO and the second chip the variable frequency LO. The fixed frequency LO and variable frequency LO are then replicated by a cascade of clock buffers, low pass filtered and distributed along phase matched, high frequency coaxial cables to the radio receivers. After being distributed over the high frequency cables the differential clock signals are converted to single-ended signals using a balun and amplified. Finally a power divider is used to supply the required number of LO signals.

There are two main advantages of the first design: Only two PLLs are built in design one so more money can be spent on each PLL. The second is that the only uncorrelated phase noise between radio channels will be the phase noise introduced by the clock distribution chips. The disadvantage is that the maximum frequency signal that is distributed is around 4 GHz which makes phase matching in the differential pairs more difficult and increases signal attenuation throughout clock distribution network.

4.1.2. Design 2: Low frequency clock distribution

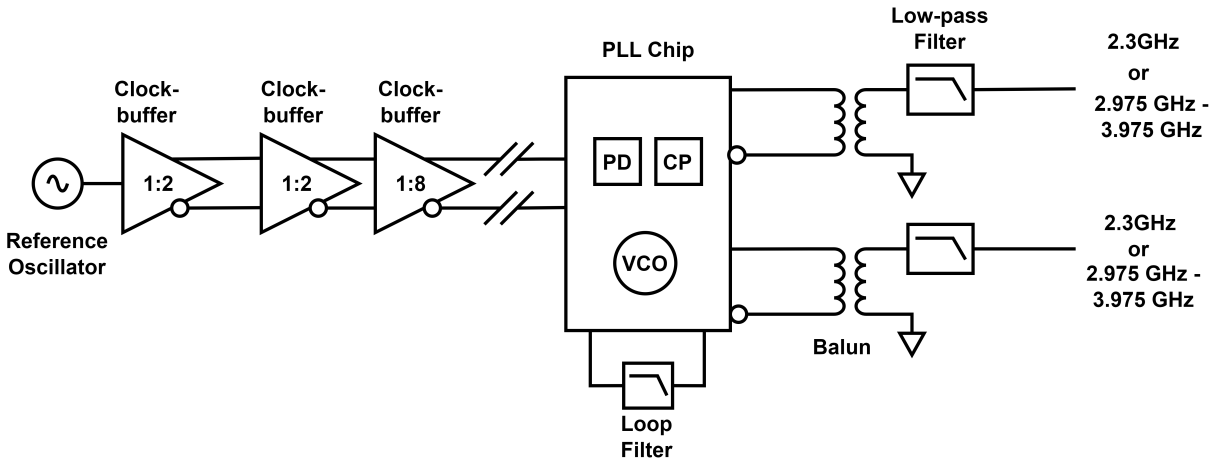


Figure 4.2: Block diagram of design 2.

In the second design, shown in figure 4.2, the reference oscillator clock signal is replicated by a cascade of clock buffers and then distributed using differential signal pairs. Two STW81200 PLL chips will be present near the receiver chain of each. One to generate the fixed frequency LO and the other to generate the variable frequency LO. Each PLL chip has two identical outputs so each PLL chip can service two channels. The advantage of this design is its simplicity. This is also the conventional way to provide an LO to an antenna array.

4.2. Elements common to both designs

4.2.1. Differential pairs, LVPECL signals and voltage regulators

Differential signals are used to transmit the clock signals between circuit boards in the design. Differential signalling removes the need for a coherent ground between circuit boards within the design and provides protection from EMI.

LVPECL(Low-voltage positive emitter–coupled logic) is a high frequency, high slew-rate signal standard often used for clock distribution. The high slew-rate of LVPECL signals helps prevent amplitude noise from converting to phase noise, as discussed in section 3.1.

Powering a PLL chip requires multiple voltage regulators. Supplying power to separate circuits within the chip using different voltage regulators isolates the noise between the circuits. The charge pump circuit, VCO, the remaining analog circuitry and the digital circuitry often each get their own voltage supply line. The STW81200 conveniently has multiple LDOs present within the STW81200 chip.

4.2.2. AOCJY-100.000MHZ Reference Oscillator

The AOCJY2 is an OCXO, an oven-controlled crystal oscillator. The oven maintains the temperature of the oscillator which keeps the frequency of the oscillator stable over fluctuations in ambient temperature. The AOCJY2 produces a 100 MHz sine-wave output at 2 dBm. This is a clock signal with a slew rate of $177\,\mathrm{V\,\mu s^{-1}}$. Of the possible frequency outputs for the AOCJY2 series the highest is chosen. A higher frequency reduces the multiplication factor, N, required to deliver the desired output frequency of a frequency synthesizer. A lower multiplication factor lowers the phase noise introduced by a phase-locked loop as discussed in section 3.2. The higher reference frequency also means that DSM noise will be centred around higher offset frequencies and so more effectively filtered by the PLL. The LTC6957, the clock buffer which succeeds the reference oscillator, performs best with respect to phase noise when the input to the clock buffer is a sine wave.

The AOCJY2 requires 1 A when warming up. To supply this power four LT3045 voltage regulators are paralleled using 20 mΩ of ballast resistances to connect the voltage supply lines. This can supply a total of 2 A which keeps the regulators from heating up.

4.2.3. LTC6957: 1- 2 clock buffer

In both designs the LTC6957 is the clock buffer which follows immediately after the reference oscillator. The buffer translates the sine-wave input of the reference oscillator

into an LVPECL clock signal, a high slew-rate clock signal, with a slew rate of 4.7 kV μs^{-1}. The clock buffer provides two identical differential outputs. The LTC6957 features input filters for low slew-rate clock signals. The input filters are set to reduce phase noise by reducing the input bandwidth to the device. The additive phase noise of the LTC6957 is shown in figure 4.3.

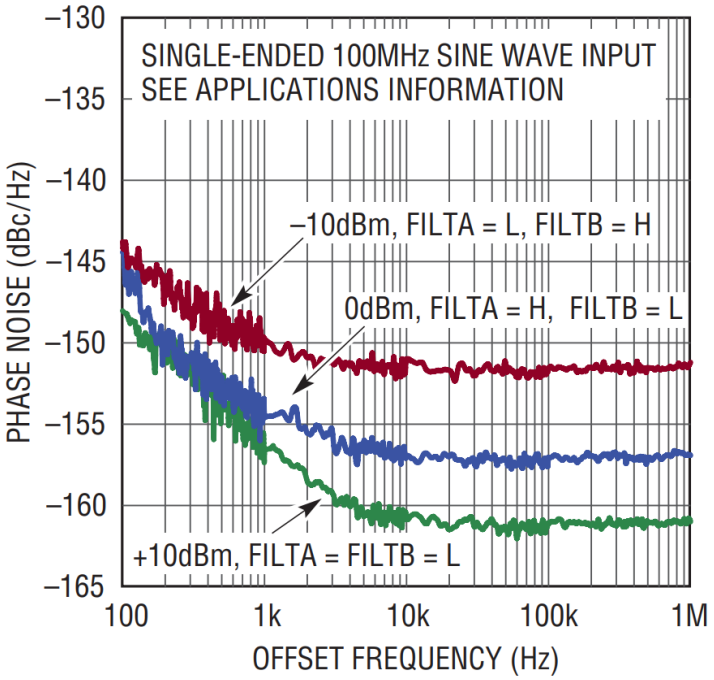


Figure 4.3: Additive phase noise of the LTC6957. [31]

4.3. Details of Design 1: Fixed frequency LO

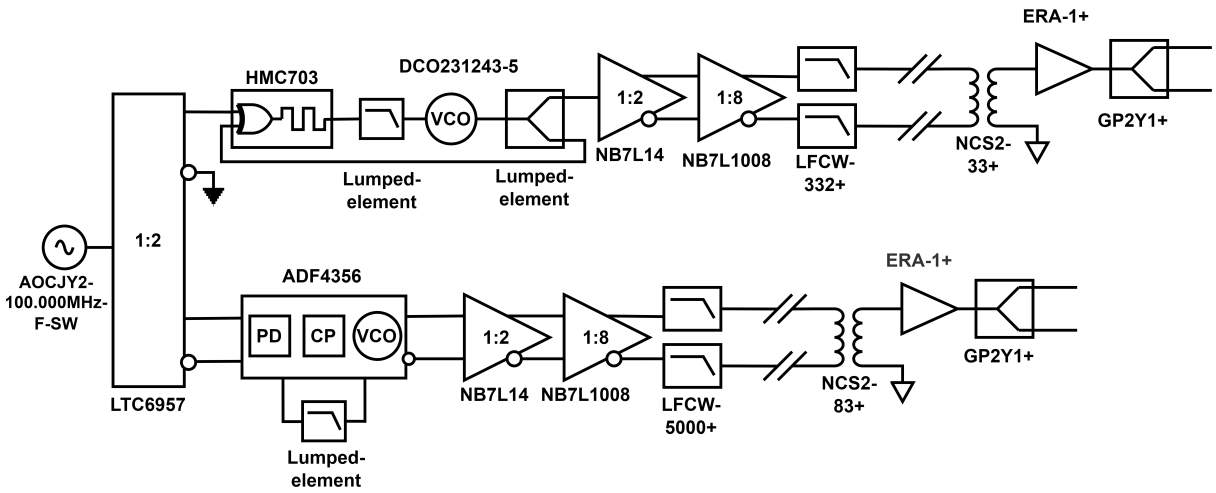


Figure 4.4: Key component annotation of design 1.

The HMC703 is the PLL chip used to generate the fixed frequency output of design one. The chip is proceeded by the lumped element loop filter shown in figure 5.4. The output of the loop filter is used to control a DCO231243-5 VCO. The power of the output of the VCO is split using a lumped element power divider. One of the outputs of the power divider returns the VCO output to the PLL chip for comparison with the reference oscillator signal, the other output of the power divider is distributed by the clock buffers.

4.3.1. VCO phase noise: DCO231243-5

The required input voltage to tune the VCO to 2.3 GHz is 2 V. At this frequency the tuning coefficient of the VCO is 10.5 MHz V^{-1}. The output power of the VCO is 4 dBm. Figure 4.5 shows the phase noise of the DCO231243-5 as specified by the datasheet of the DCO231243-5.

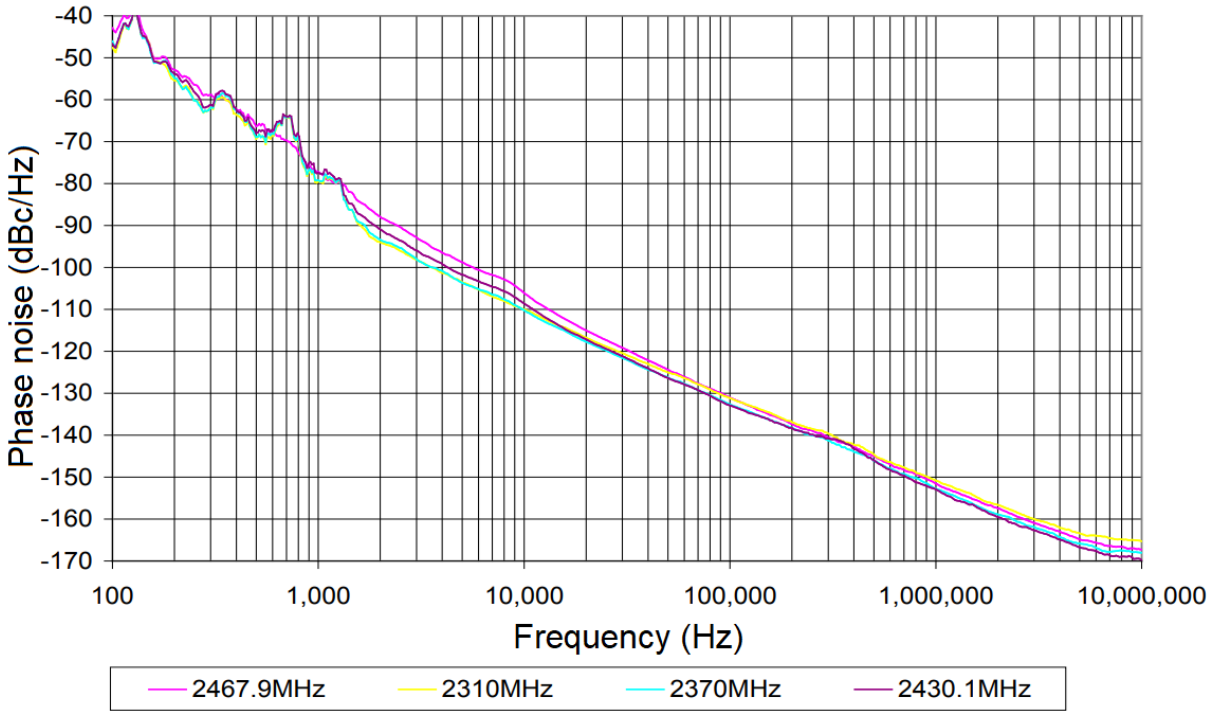


Figure 4.5: Phase noise of the DCO231243-5. [32]

4.3.2. The power divider

The feedback input of the HMC703 requires a signal with a power of −10 dBm, an input sufficiently larger or smaller than this will cause spurs on the output of the PLL [4]. The resistive power divider supplies the necessary attenuation from the output of the VCO to the input of the HMC703 PLL chip. The implemented power divider is shown in figure 4.6 and its characteristics are shown in figure 4.1.

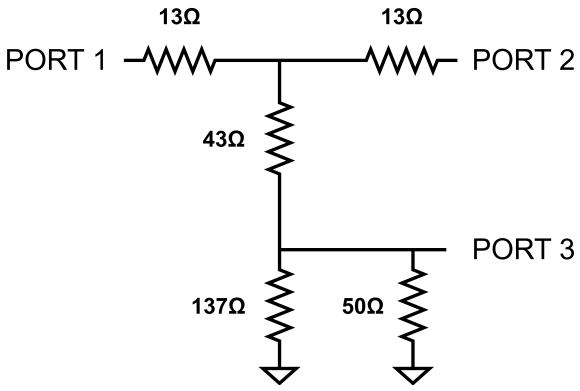


Figure 4.6: Implementation of the resistive power divider.

Table 4.1: Attenuation of the implemented power divider.

	Port connection	Total attenuation from PORT 1 to PORT N
PORT 1	Output of the VCO	N/A
PORT 2	Input to the clock buffer	5.242 dB
PORT 3	Feedback input of the HMC703	14.557 dB

4.4. Details of Design 1: Variable frequency LO

There are high quality external VCOs that can cover the output range of the variable frequency LO. The range of the tuning voltage such VCOs would require from the loop filter would exceed the 5 V maximum the charge pump circuit of the ADF4356 can achieve. An active filter would be required to tune the VCO. The phase noise introduced by an active filter with a low noise amplifier would degrade the performance of the PLL to below the performance that is achieved using the on-board VCO of the ADF4356 chip.

4.4.1. VCO phase noise: ADF4356

The ADF4356 VCO consists of four separate VCO tank circuits. The chip automatically calibrates and selects the correct VCO tank circuit. The total output bandwidth of the ADF4356 VCO is 3.4 GHz to 6.8 GHz. Frequencies lower than the output bandwidth are achieved using a selection of frequency dividers implemented at the VCO output. Figure 4.7 shows the phase noise of the embedded VCO at 3.4 GHz.

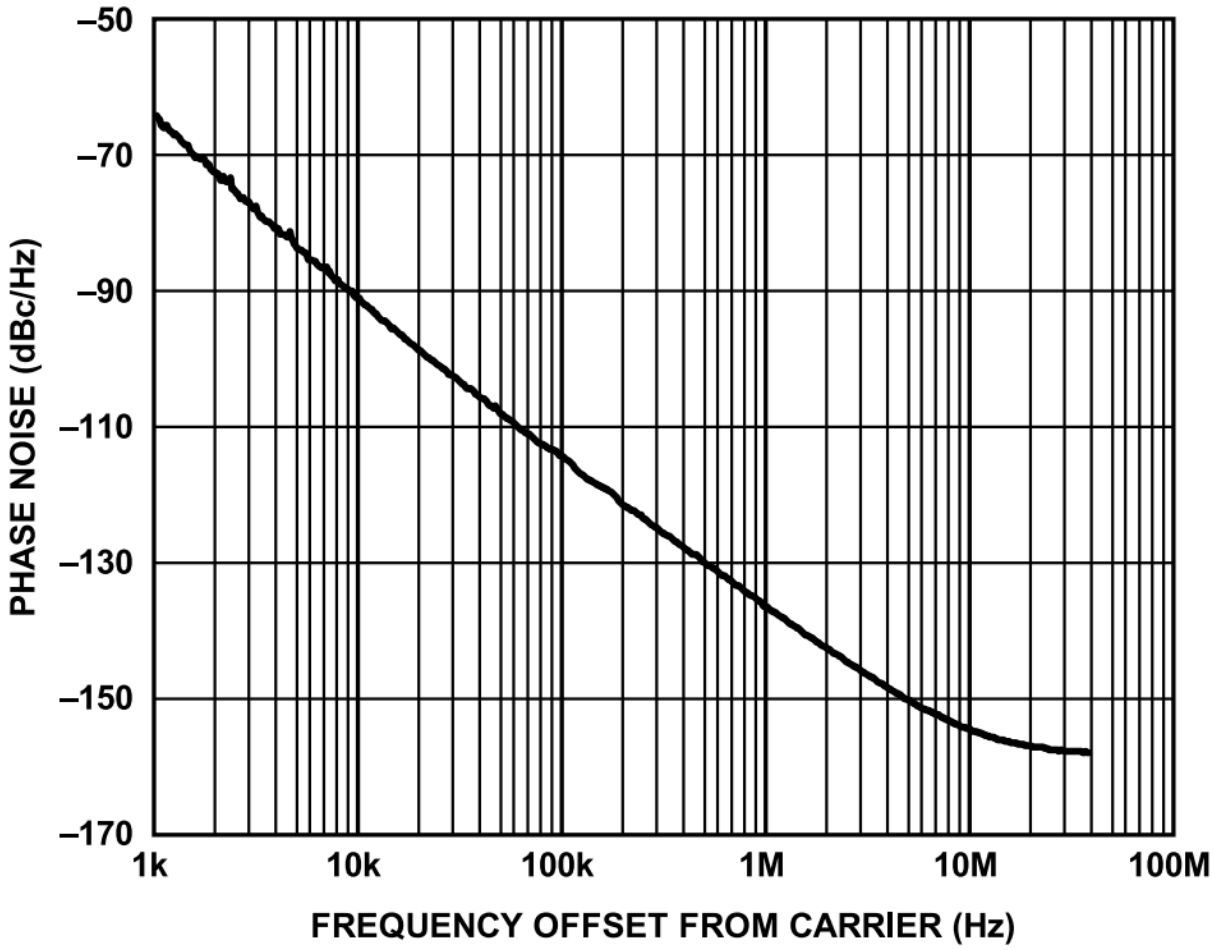


Figure 4.7: Phase noise of the ADF4356 VCO at 3.4 GHz. [33]

4.5. Design 1: elements common to both LOs

4.5.1. The NB7L14: 1-2 clock buffer and the NB7L1008: 1-8 clock buffer

The NB7L14 Clock buffer is used to distribute two LVPECL replicas of its input clock signal which is then replicated again using the NB7L1008. Both will introduce additional phase noise to the clock signal they distribute. Figure 4.8 shows the additive phase noise of the NB7L14 which is 25 fs over the band width of 12 kHz to 20 MHz and figure 4.9 shows the additive phase noise of the NB7L1008 which is 24 fs over the band width of 12 kHz to 20 MHz. The green line in figure 4.9 is the output of the NB7L1008, the blue line is the input to the NB7L1008.

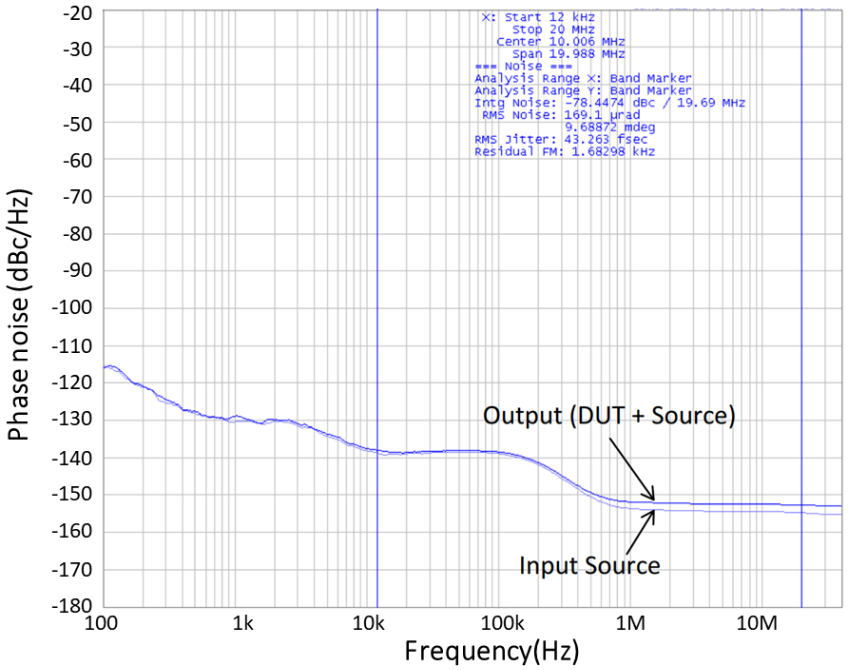


Figure 4.8: Additive phase noise of the NB7L14 at 622.08 MHz. [34]

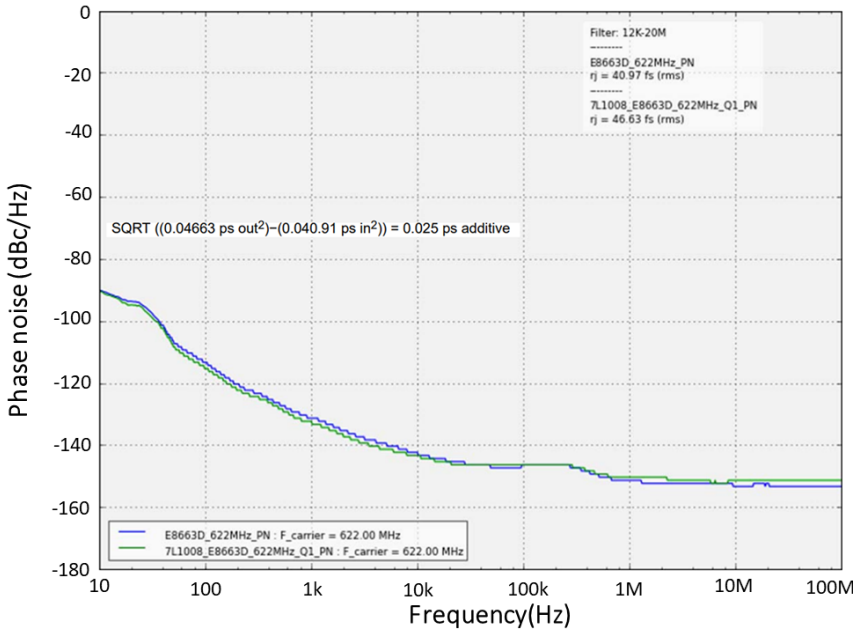


Figure 4.9: Additive phase noise of the NB7L1008 at 622 MHz. [35]

4.5.2. Final output power consideration

The final output power of the LO must be in the range −6 dBm to 6 dBm. The LVPECL output of the NB7L1008 has a voltage range of 800 $\mathrm{mV_{peak\text{-}to\text{-}peak}}$. The average power of the signal, being terminated to a 50 Ω load, is then 4.08 dBm. There could be some attenuation in the cables proceeding the filters, an absolute maximum of 2 dB. The LO signal will then be power divided which adds an additional 3 dB of attenuation. For this

reason, to safely meet the input power requirements of the mixers, an RF amplifier with a gain of at least 1 dB is required.

4.5.3. The cost of design one

Table 4.2 gives a break of the cost of the components needed for a full implementation of the first design. The total cost of the components is R9235. To distribute the fixed frequency LO 32 RG58 coaxial cables with a total cost of around R9000 is needed. To distribute the variable frequency LO cables capable of carrying a signal of a least 4 GHz are needed. These would need to be LMR240 cables. For 32 of these, the cost is R25000. The PCBs required for the design are created using an FR4 dielectric and would cost roughly R3000. In total the design costs R46235.

Table 4.2: Summary of the component cost of design one.

	Part Number	Price Per Unit	no. of units	Total price
Reference Oscillator	ACOJY2-100.000Mhz-F-SW	3747.27	1	3747.27
1:2 Clock Buffer	LTC6957-1	218.5	1	218.5
Integer-N PLL Chip	HMC703	561.00	1	561
VCO	DCRO196202-5	546.43	1	546.43
Fractional-N PLL Chip	ADF4356	561.00	1	561
1:2 Clock Buffer	NB7L14	297.54	2	595.08
1:8 Clock Buffer	NB7L1008	144.97	2	289.94
Low Pass Filter	LFCW-332+	106.4	2	212.8
Low Pass Filter	LFCW-5000+	116.66	2	233.32
Balun	NCS2-33+	25.46	16	407.36
Balun	NCS2-83+	25.46	16	407.36
Amplifier	ERA-1+	45.91	16	734.56
Power Divider	GP2Y1+	45.03	16	720.48
Total				9235.10

4.6. Details of Design 2

The clock buffers present in design two will deteriorate the phase noise of the reference signal. The phase noise added by the CDCLVP2108 clock buffer and the LTC6957 will be uncorrelated across radio channels. The phase noise introduced by these chips will also be scaled by the closed loop transfer function of the PLL.

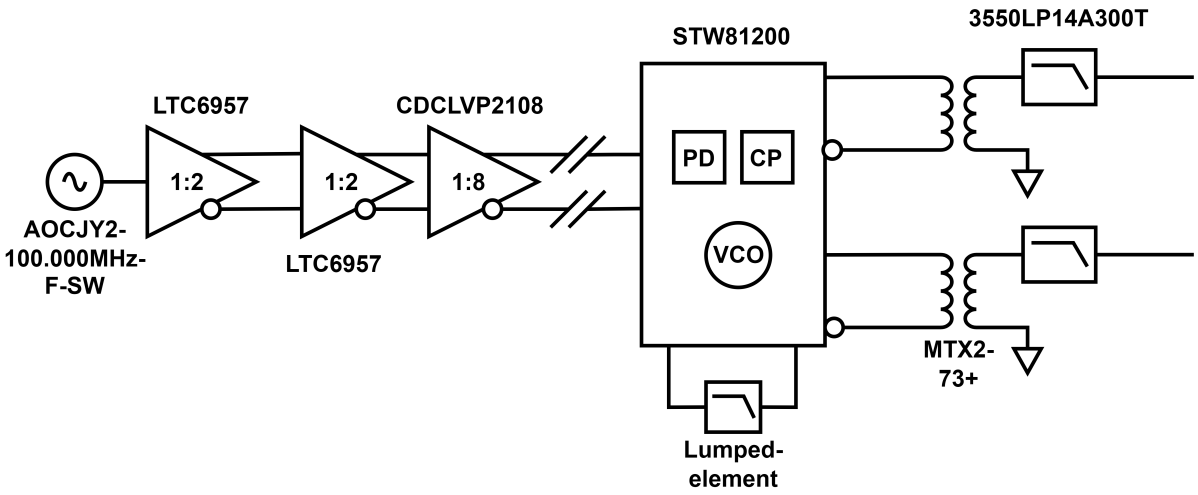
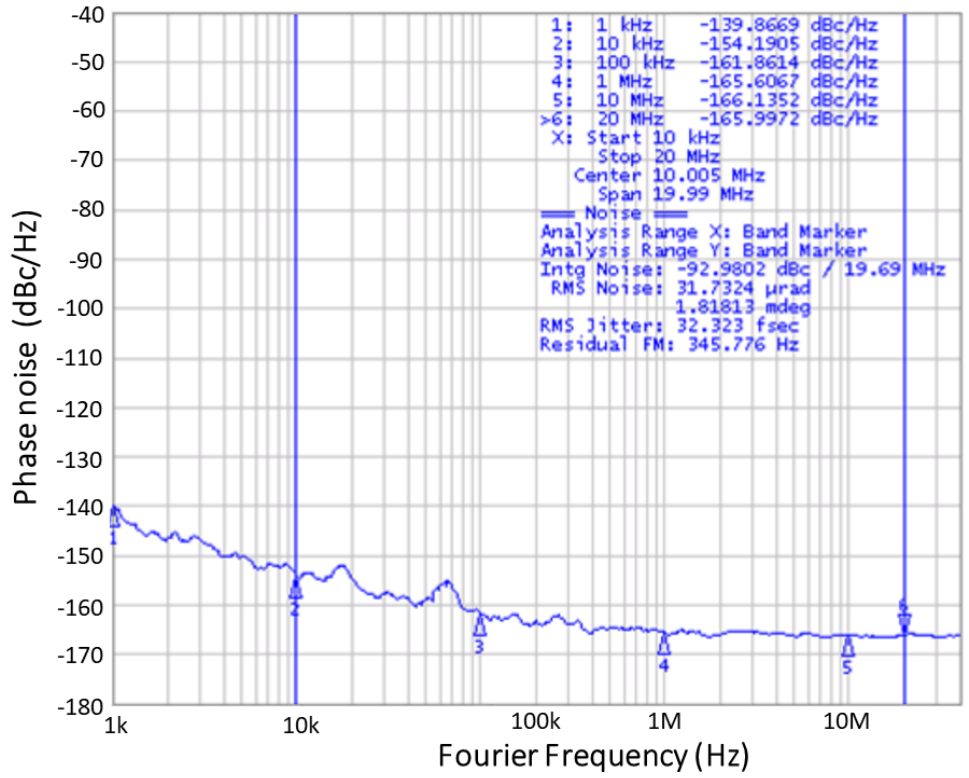


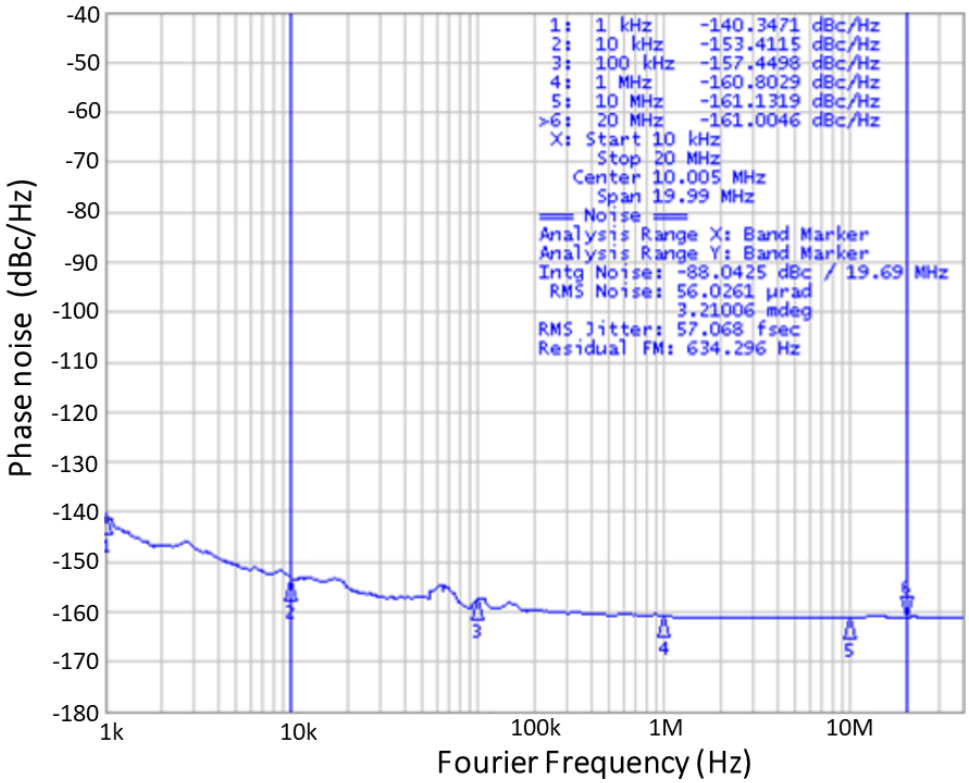
Figure 4.10: Key component annotation of design 1.

4.6.1. CDCLVP2108: 2-16 clock buffer

The CDCLVP2108 is an LVPECL clock buffer that distributes the reference clock. The CDCLVP2108 has a jitter of 47 fs measured in a bandwidth of 10 kHz to 20 MHz at a frequency of 156 MHz. Figure 4.11 shows the measurement. As with the other clock buffers, The effect of the introduced phase noise is to raise the phase noise floor at higher offset frequencies.



(a) Measurement at the input of the CDCLVP2108.



(b) Measurement at the output of the CDCLVP2108.

Figure 4.11: Phase noise measurement of the CDCLVP2108. [36]

4.6.2. VCO phase noise: STW81200

The STW81200 VCO consists of three separate VCO tank circuits. The chip automatically calibrates and selects the correct tank circuit. The total output bandwidth of the STW81200 VCO is 3 GHz to 6 GHz and lower output frequencies are achieved using a selection of frequency divider implemented after the VCO.

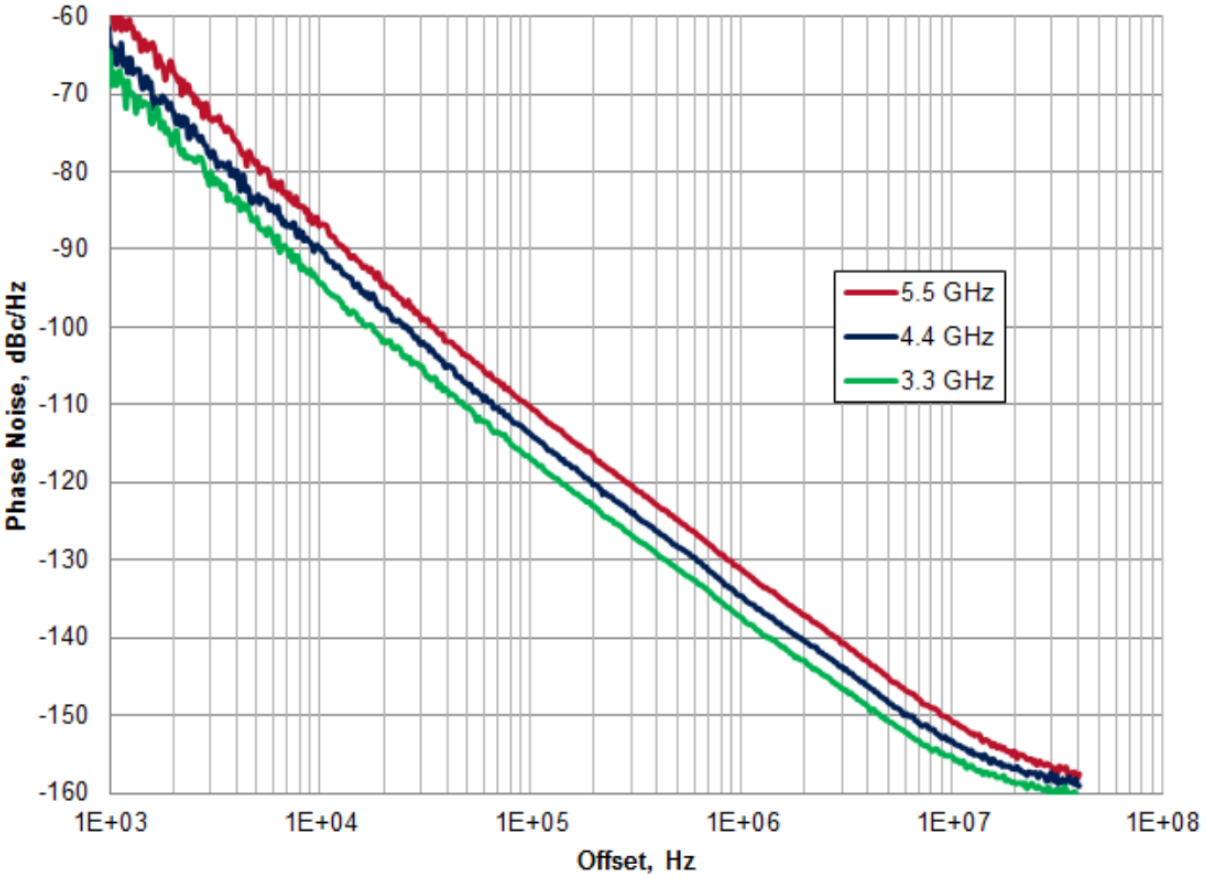


Figure 4.12: Phase noise of the STW81200 VCO at 3.4 GHz. [37]

4.6.3. The cost of design two

Table 4.3 gives a break of the cost of the components needed for a full implementation of design two. The total cost of components comes to around R17310. Standard RG58 coaxial cables can be used to distribute the reference clock signal. The cost of 64 of these cables is around R18000. The PCB on which the STW81200 chip is placed is the PCB of the radio it services. The total number and rough size of the PCBs used for both designs is the same. This is 16 radio PCBs near each antenna and one central PCB from which either the reference oscillator or the LOs themselves are distributed. This leaves the PCB cost at R3000. In total the second design costs R38310.

Table 4.3: Summary of the component cost of design two.

	Part Number	Price Per Unit	no. of units	Total price
Reference Oscillator	ACOJY2-100.000Mhz-F-SW	3747.268	1	3747.268
1:2 Clock Buffer	LTC6957-1	218.5	1	218.5
1:2 Clock Buffer	LTC6957-3	218.5	2	437
2:16 Clock Buffer	CDCLVP2108	394.82	2	789.64
Fractional-N PLL Chip	STW81200	284.43	32	9101.76
Balun	MTX2-73+	47.12	64	3015.68
Low Pass Filter	3550LP14A300T	9.956	64	637.184
Total				17309.85

Chapter 5

Results

The following chapter will display and discuss the measurement of test boards built to evaluate some aspects of the different designs. The measurements were taken using an FSUP-1166.3505.26 signal source analyzer. For each PLL the modelled phase noise sources and the transfer functions of the PLL are simulated. The final simulated phase noise is then compared with the measured phase noise.

5.1. The Reference oscillator

The Leeson-cutler model of the phase noise of the OCXO can be fit to the measured phase noise of OCXO using the parameters listed below. Figure 5.1 is a plot of both the simulated Leeson-culter model of the phase noise of the OCXO and the measured phase noise of the OCXO.

$F = 17.78\,\mathrm{dB}$

$P_a = 2\,\mathrm{dBm}$

$f_c = 35\,\mathrm{Hz}$

$Q_l = 10000$

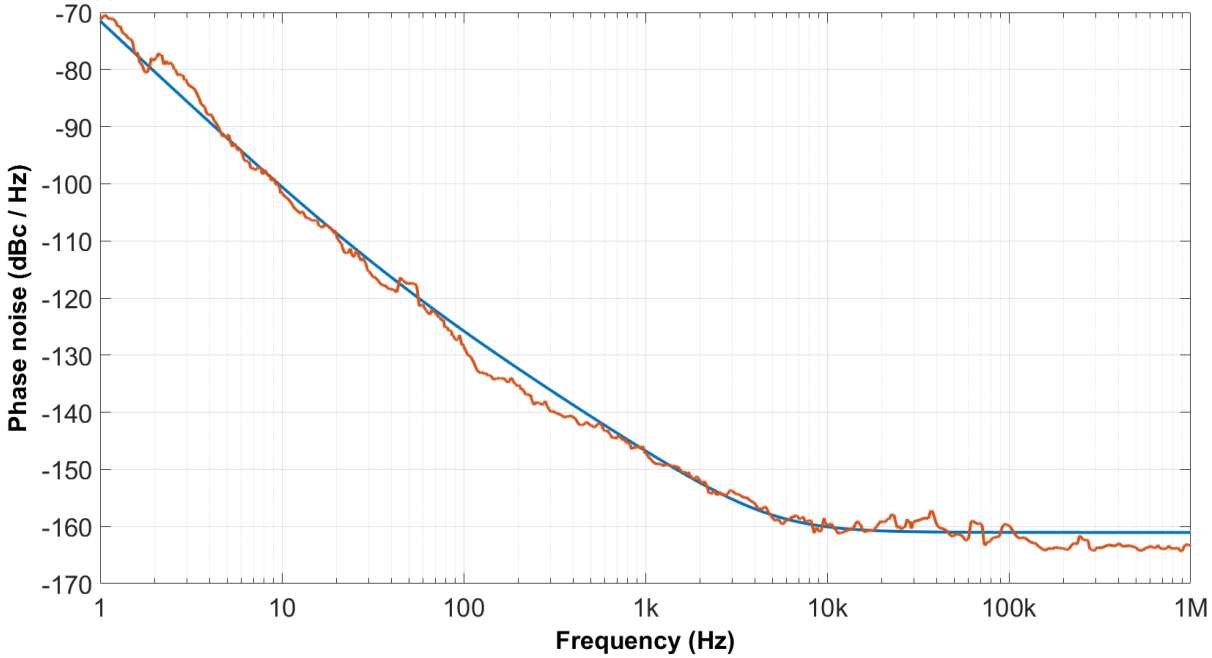


Figure 5.1: Leeson-Culter curve fit of to the phase noise of the reference oscillator.

5.2. Design 1: Fixed frequency LO

The board built to test the HMC703 and the DCO231243-5 is shown in figure 5.2.

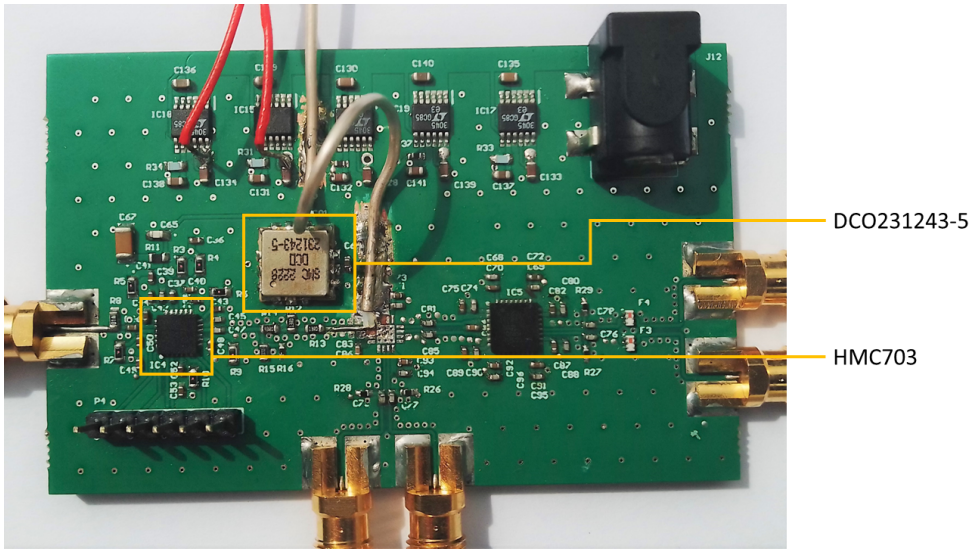


Figure 5.2: HMC703 test board.

5.2.1. Simulation

From the datasheet of the HMC703 PLL chip the figure of merit for the phase noise floor is $\text{FOM}_{\text{chip floor}} = -230\,\text{dBc}\,\text{Hz}^{-1}$ and the figure of merit for the flicker phase noise of the HMC703 chip is $\text{FOM}_{\text{chip flicker}} = -270\,\text{dBc}\,\text{Hz}^{-1}$. Which introduces the phase noise shown in figure 5.3

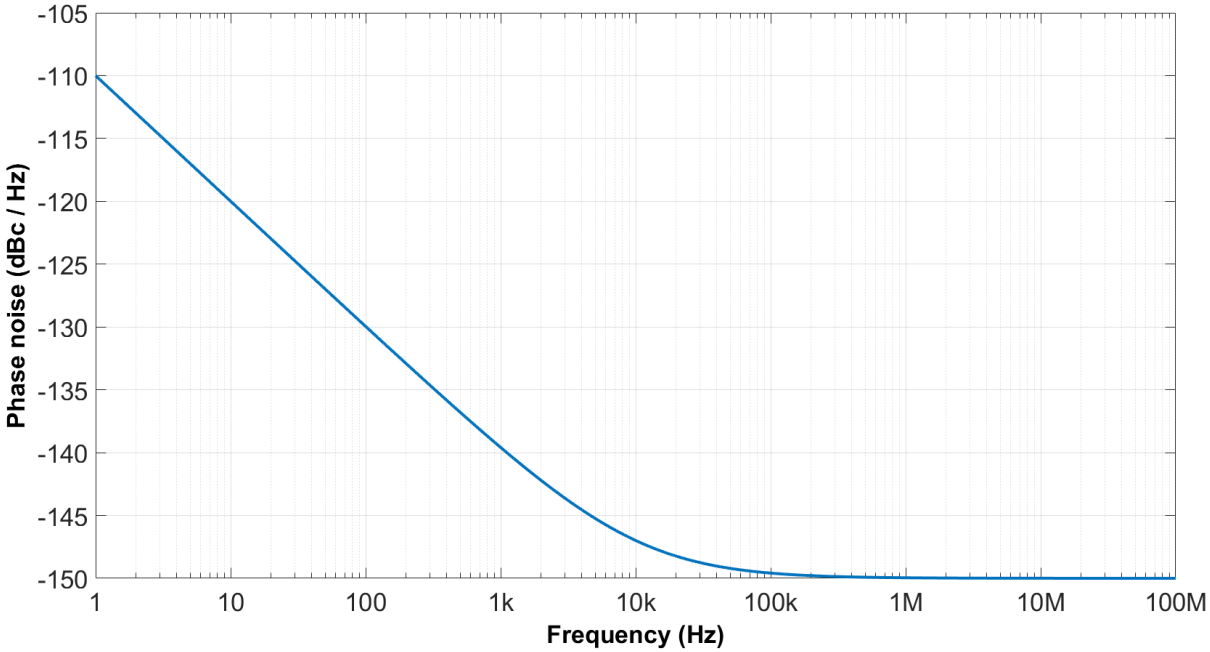


Figure 5.3: Phase noise introduced by the HMC703 PLL chip.

The loop filter used with the HMC703 PLL chip is implemented as shown in figure 5.4 and introduces the phase noise shown in figure 5.5.

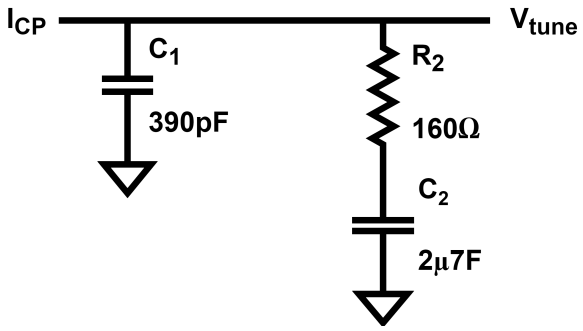


Figure 5.4: Loop filter of the HMC703 PLL.

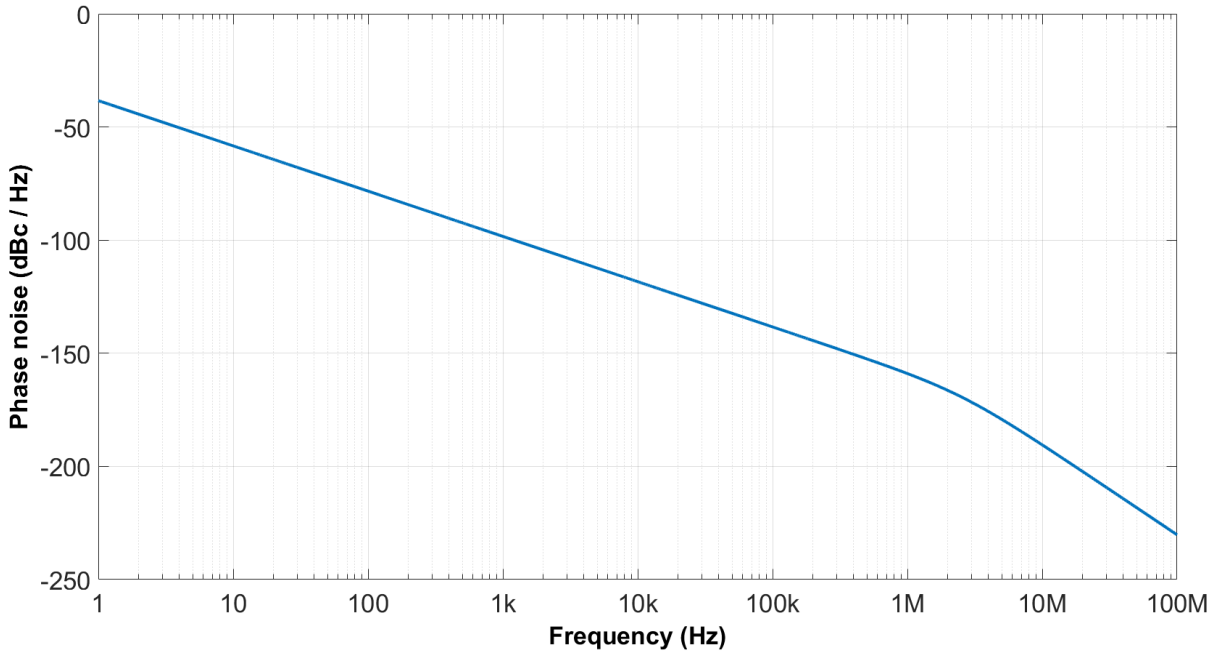


Figure 5.5: Phase noise introduced by the loop filter of the HMC703 PLL.

The phase noise of the DCO231243-5 VCO at 2.3 GHz can be fit to the Leeson-culter model using the following parameters; which is shown in figure 5.6.

$F = 11.837\,\text{dB}$

$P_a = 2\,\text{dBm}$

$f_c = 12\,\text{kHz}$

$Q_l = 164$

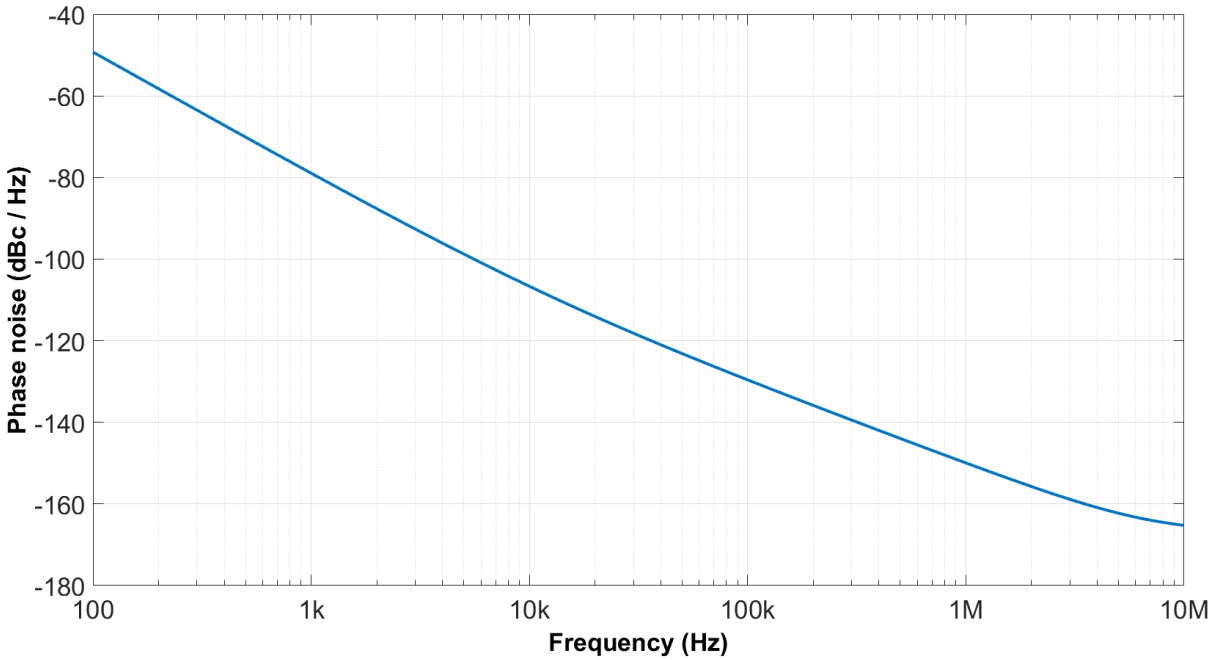


Figure 5.6: Leeson-Cutler model of the DCO231243-5 VCO.

The charge pump gain of the HMC703 is set $K_{\mathrm{PD}} = 2.5\,\mathrm{mA}$. The tuning co-efficient of the DCO231243-5 at 2.3 GHz is $10.5\,\mathrm{MHz\,V^{-1}}$. The N divider of the HMC703 is set to 23. Given the parameters, the gain cross-over frequency of the HMC703 PLL is 28.8 kHz with a phase margin of 88.5°. The closed-loop transfer function and error function of the HMC703 PLL are shown in figure 5.7.

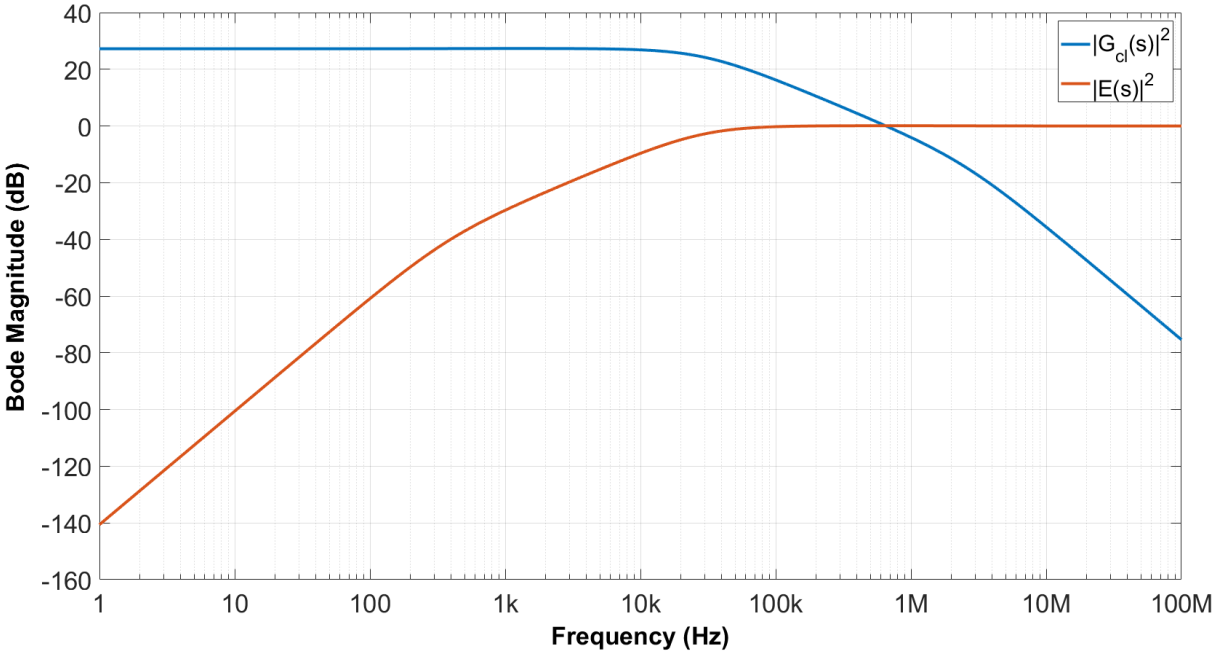


Figure 5.7: The bode magnitude plot of the closed loop and error signal transfer function of the HMC703 PLL.

Table 5.1 gives a summary of the simulation. The phase noise power of the reference oscillator and the PLL chip are added together to form the total feed-forward phase noise. The total feed-forward phase noise is then multiplied with the squared gain of the closed loop transfer function to give the feed-forward contribution. The phase noise contributed by the loop filter and the VCO are summed together and multiplied by the squared gain of the error signal transfer function to get the error signal contribution. The sum of the feed-forward contribution and the error signal contribution is the total simulated phase noise. The total RMS jitter integrated from 1 kHz to 50 MHz is 33.2 fs

Table 5.1: Summary of the simulated phase noise of the HMC703 PLL

Offset Frequency	1	10	100	1k	10k	100k	1M	10M	100M
Reference Oscillator	-70.50	-100.53	-125.76	-146.75	-160.06	-161.03	-161.05	-161.05	-161.05
PLL Chip	-110.00	-120.00	-130.00	-139.59	-146.99	-149.59	-150.00	-150.00	-150.00
Total feed-forward phase noise	-70.50	-100.49	-124.37	-138.82	-146.78	-149.29	-149.67	-149.67	-149.67
Gain of the closed loop transfer function	27.24	27.24	27.24	27.33	26.86	16.24	-4.04	-35.63	-75.37
Feed-forward contribution	-43.27	-73.25	-97.13	-111.49	-119.92	-133.04	-153.71	-185.30	-225.04
Loop filter	-38.35	-58.35	-78.35	-98.35	-118.35	-138.36	-158.97	-190.49	-230.22
VCO	10.55	-19.29	-49.26	-78.95	-106.67	-129.60	-149.95	-165.25	-166.97
Total error signal phase noise	10.55	-19.29	-49.25	-78.90	-106.38	-129.05	-149.43	-165.24	-166.96
Gain of the error signal transfer function	-140.59	-100.60	-60.89	-29.72	-9.65	-0.25	0.08	0.01	0.00
Error signal contribution	-130.05	-119.89	-110.15	-108.62	-116.03	-129.30	-149.35	-165.23	-166.96
Total phase noise	-43.27	-73.25	-96.92	-106.81	-114.54	-127.77	-147.99	-165.19	-166.96

5.2.2. Measured results

Figure 5.8 shows the measured phase noise and the simulated phase noise of the HMC703. The model is a close match near the bandwidth of the PLL. The phase noise floor of the VCO is higher than stated in figure 4.5. The excess phase noise present at the low offset frequencies also appears in figure 5.25 but in no other measurement. The reference oscillator is modelled accurately according to the Leeson-culter model as shown in figure 5.1. It is possible that the excess phase noise is caused by the random walk of the reference oscillator which is not accounted for in the Leeson-culter model. Measuring the phase noise down to an offset frequency of 1 Hz using the FSUP-1166.3505.26 takes one minute. This is enough time for the random walk of the reference oscillator to present in the phase noise measurement. In addition, at low offset frequencies, fewer samples are taken per measurement because each sample takes longer to ascertain and so the power of the signal is less accurately estimated.

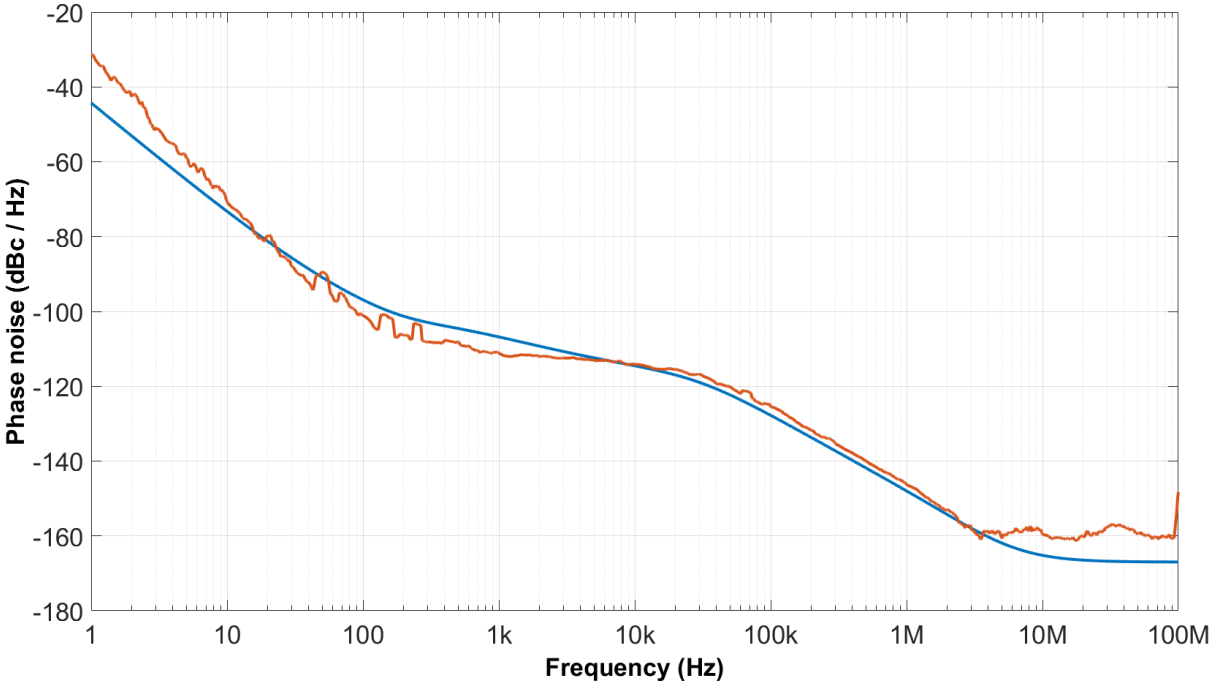


Figure 5.8: Measured phase noise of HMC703.

5.3. Design 1: Variable frequency LO

The board built to test the ADF4356, the NB7L14 and the NB7L1008 is shown in figure 5.9.

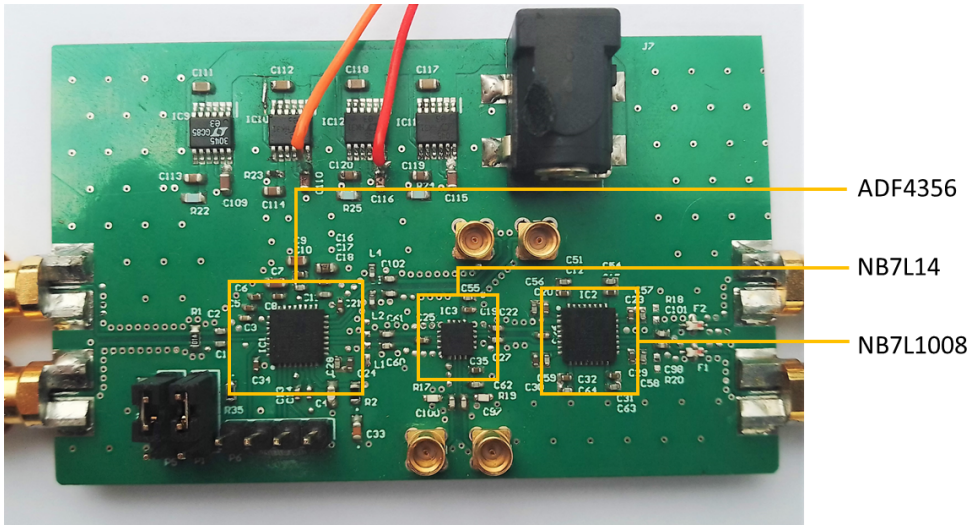


Figure 5.9: ADF4356 test board.

5.3.1. Simulation

From the datasheet for the ADF4356 the figure of merit for the phase noise floor is $\text{FOM}_{\text{chip floor}} = -225\,\text{dBc}\,\text{Hz}^{-1}$ and the figure of merit for the flicker phase noise is $\text{FOM}_{\text{chip flicker}} = -261\,\text{dBc}\,\text{Hz}^{-1}$. Which introduces the phase noise shown in figure 5.10.

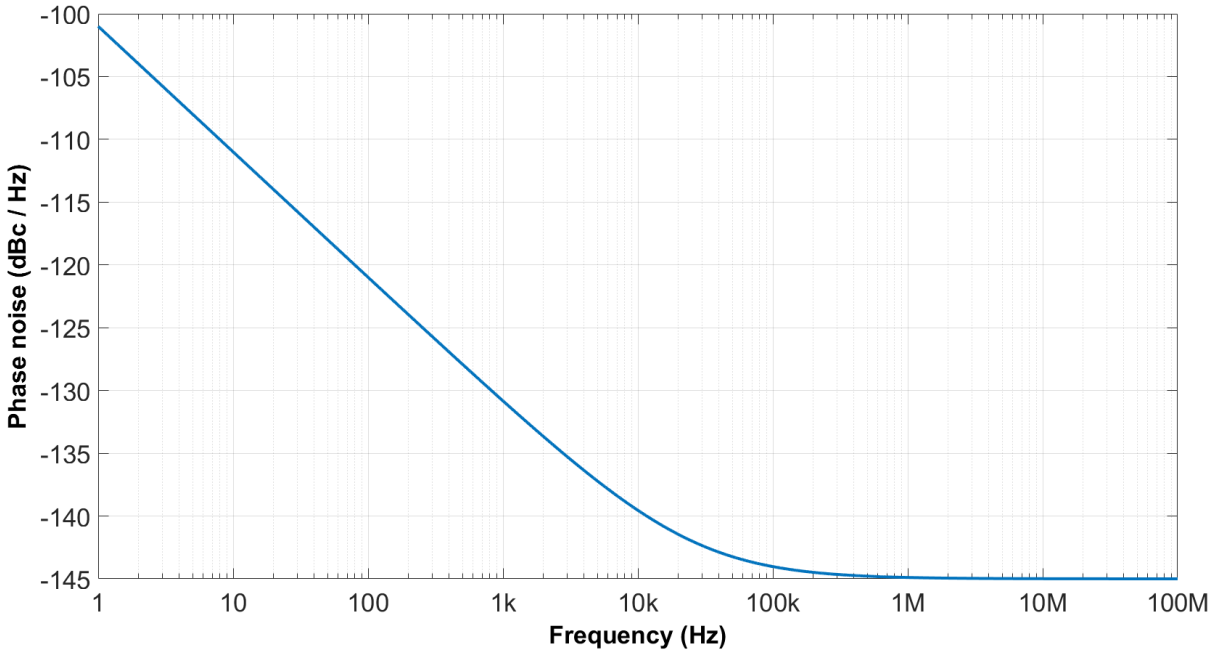


Figure 5.10: Phase noise introduced by the ADF4356 PLL chip.

The loop filter used with the ADF4356 PLL is implemented as shown in figure 5.11 and introduces the phase noise shown in figure 5.12.

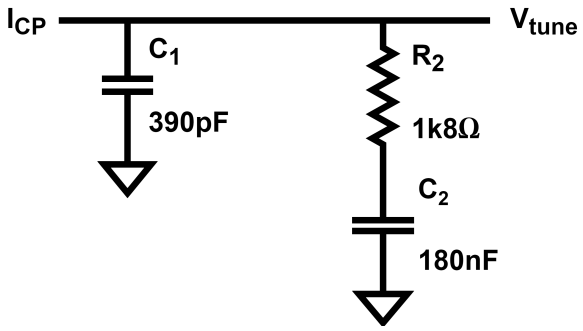


Figure 5.11: Loop filter of the ADF4356 PLL.

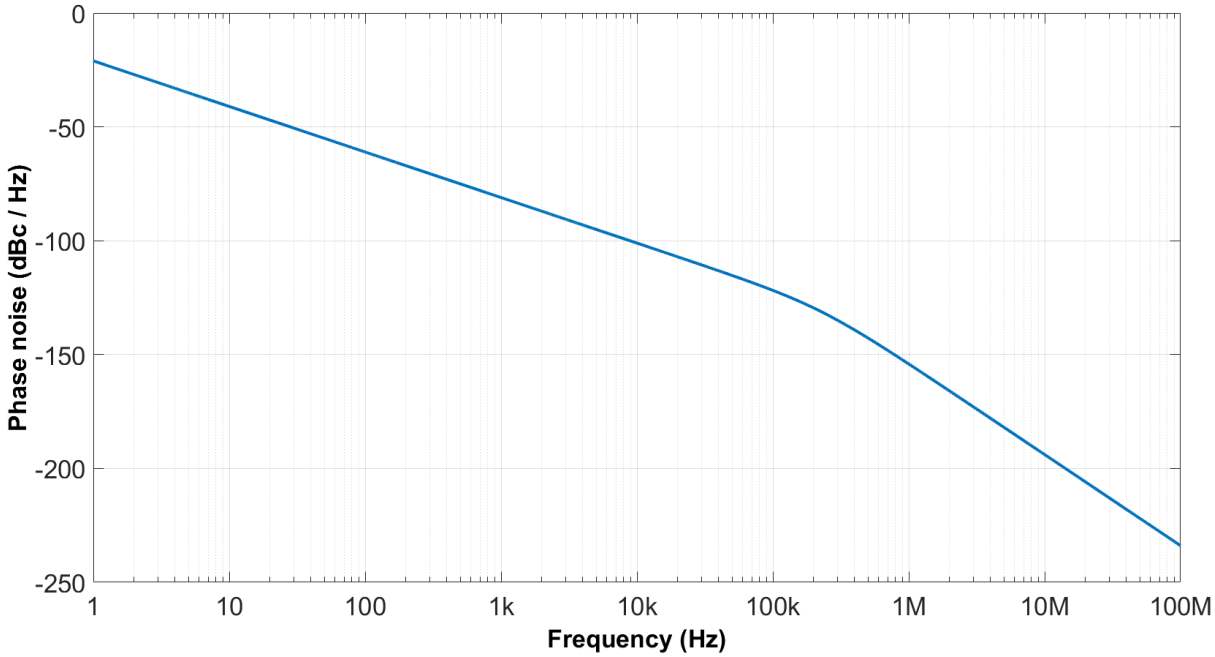


Figure 5.12: Phase noise introduced by the loop filter of the ADF4356 PLL.

The phase noise of the built in VCO of the ADF4356 at 3.439 GHz can be fit to the Leeson-culter model using the parameters below and is shown in figure 5.13.

$F = 19.777\,\text{dB}$

$P_a = 2\,\text{dBm}$

$f_c = 30\,\text{kHz}$

$Q_l = 149.351$

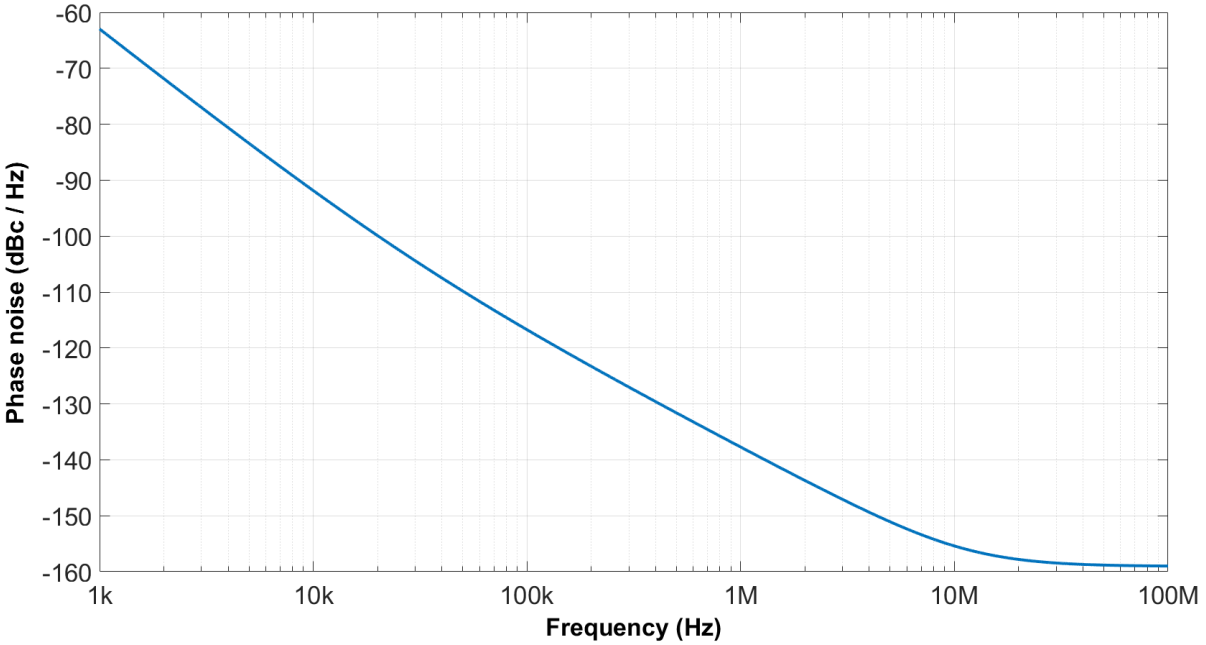


Figure 5.13: Leeson-Cutler model of the ADF4356 VCO.

The charge pump gain of the ADF4356 is set to $K_{\mathrm{PD}} = 900\,\mu\mathrm{A}$ and the tuning co-efficient of the internal VCO at 3.439 GHz is $23\,\mathrm{MHz\,V^{-1}}$. The fractional N divider of the ADF4356 is set to 34.39. With the given parameters, the gain cross-over frequency of the ADF4356 PLL is 93.9 kHz with a phase margin of 66.8°. The closed-loop transfer function and error function of the ADF4356 PLL are shown in figure 5.14.

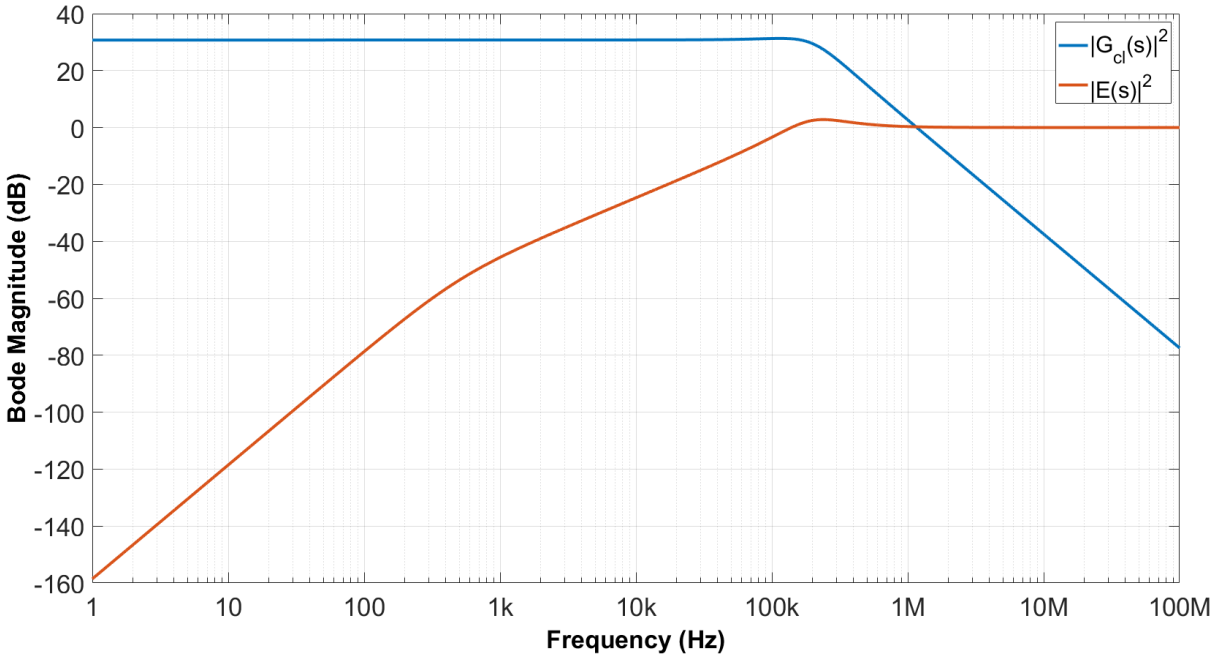


Figure 5.14: The bode magnitude plot of the closed loop and error signal transfer function of the ADF4356 PLL.

Table 5.2 shows summary of the simulation results for the ADF4356. The total RMS jitter integrated from 1 kHz to 50 MHz is 86.6 fs.

Table 5.2: Summary of the simulated phase noise of the ADF4359 PLL

Offset Frequency	1	10	100	1k	10k	100k	1M	10M	100M
Reference Oscillator	-70.50	-100.53	-125.76	-146.75	-160.06	-161.03	-161.05	-161.05	-161.05
PLL Chip	-101.00	-111.00	-121.00	-131.00	-139.55	-144.03	-144.89	-144.99	-145.00
Total feed-forward phase noise	-70.50	-100.16	-119.75	-130.89	-139.51	-143.94	-144.79	-144.88	-144.89
Gain of the closed loop transfer function	30.73	30.73	30.73	30.75	30.76	31.26	2.68	-37.43	-77.43
Feed-forward contribution	-39.77	-69.43	-89.02	-100.14	-108.75	-112.69	-142.11	-182.31	-222.32
Loop filter	-21.05	-41.05	-61.05	-81.05	-101.06	-121.08	-154.14	-193.92	-233.91
VCO	26.89	-3.11	-33.10	-62.97	-91.86	-116.74	-137.72	-155.40	-158.99
Total error signal phase noise	26.89	-3.11	-33.09	-62.90	-91.37	-115.38	-137.62	-155.40	-158.99
Gain of the error signal transfer function	-158.54	-118.54	-78.71	-45.63	-24.68	-3.42	0.33	0.00	0.00
Error signal contribution	-131.65	-121.65	-111.80	-108.53	-116.05	-118.80	-137.29	-155.40	-158.99
Total phase noise	-39.77	-69.43	-89.00	-99.55	-108.00	-111.74	-136.05	-155.39	-158.99

5.3.2. Measured Results

Figure 5.15 plots the measured phase noise along with the simulated phase noise of the ADF4356 PLL. The curves match each other well except near the loop bandwidth and in the final decade of the plot. The difference in phase noise between the measured and simulated data in the final decade of the plot is the phase noise introduced by the delta-sigma modulator.

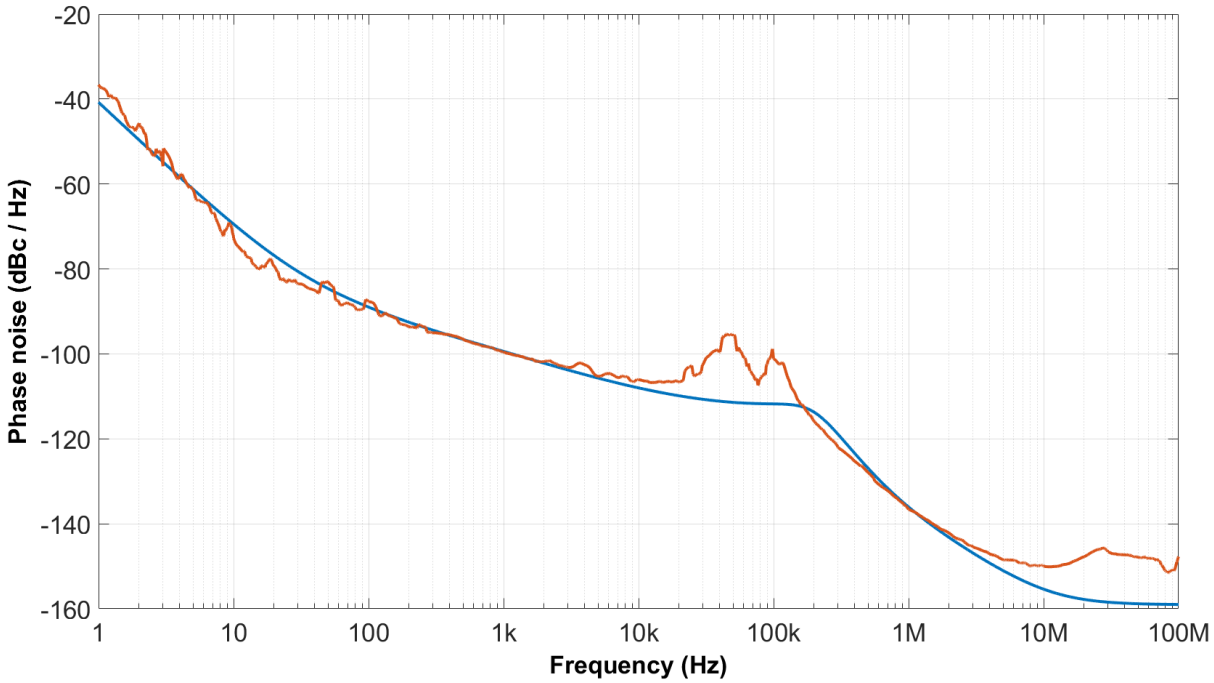


Figure 5.15: Measured phase noise of ADF4356.

Significant spurs are shown in figure 5.16. The excess phase noise in this region is a misrepresentation. The FSUP-1166.3505.26 is representing some of the power of the spurs as excess phase noise as it fails to distinguish between the two. There are offset frequencies at which spurs commonly occur and the mechanism that generated the spur can often be found by comparing measured spurs to where a possible source would place a spur. The spurs seen in figure 5.16 are not from a common spur generating mechanism in the PLL. There are also multiple spurs clustered together which is uncommon. The spurs introduced are due to noise introduced by poorly performing voltage regulators. The LT3045 voltage regulator, used on three of the test boards, often provided unstable and unpredictable output regulation.

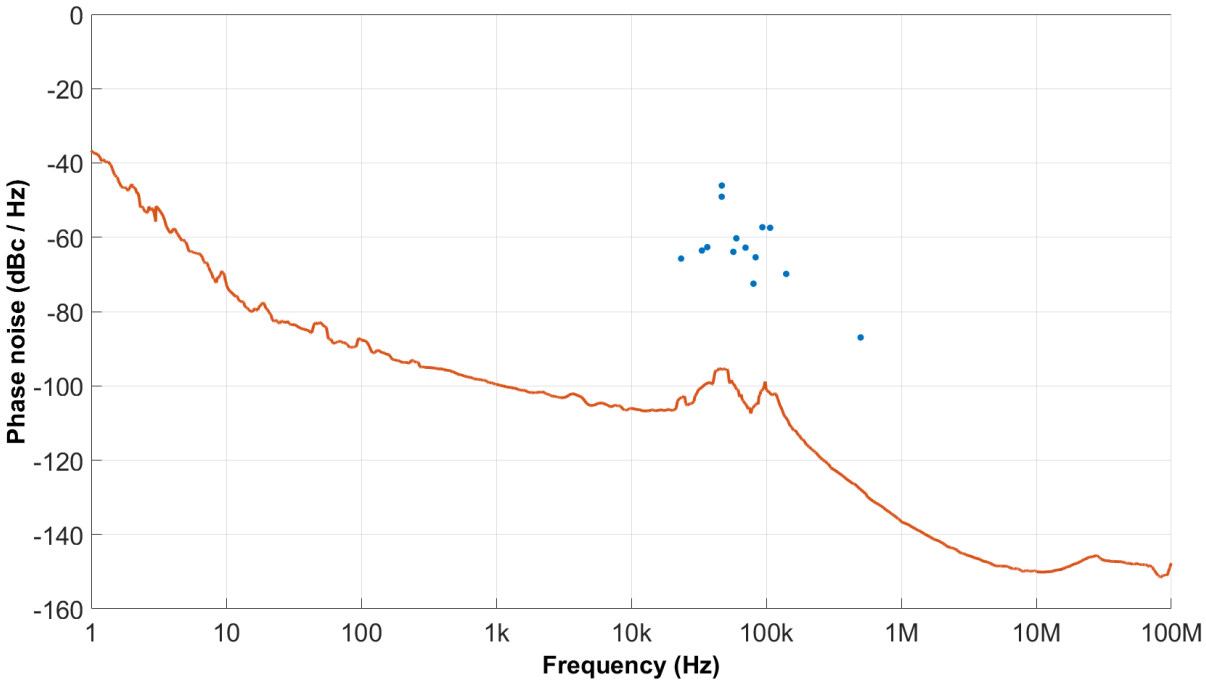


Figure 5.16: ADF4356 with spurs near the loop bandwidth.

Figure 5.17 is the phase noise before and after the NB7L1008 clock buffer and figure 5.18 shows the difference between the two. The clock buffer raises the phase noise floor around 10 MHz.

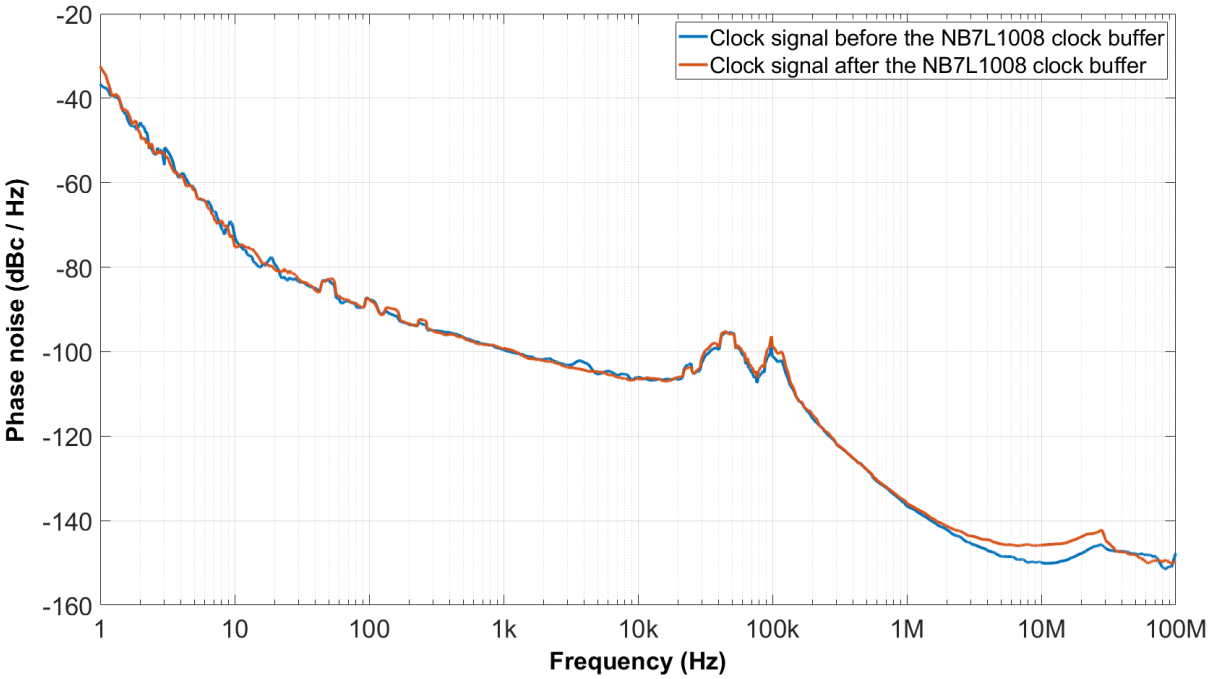


Figure 5.17: The ADF4356 clock signal before and after the NB7L1008 clock buffer.

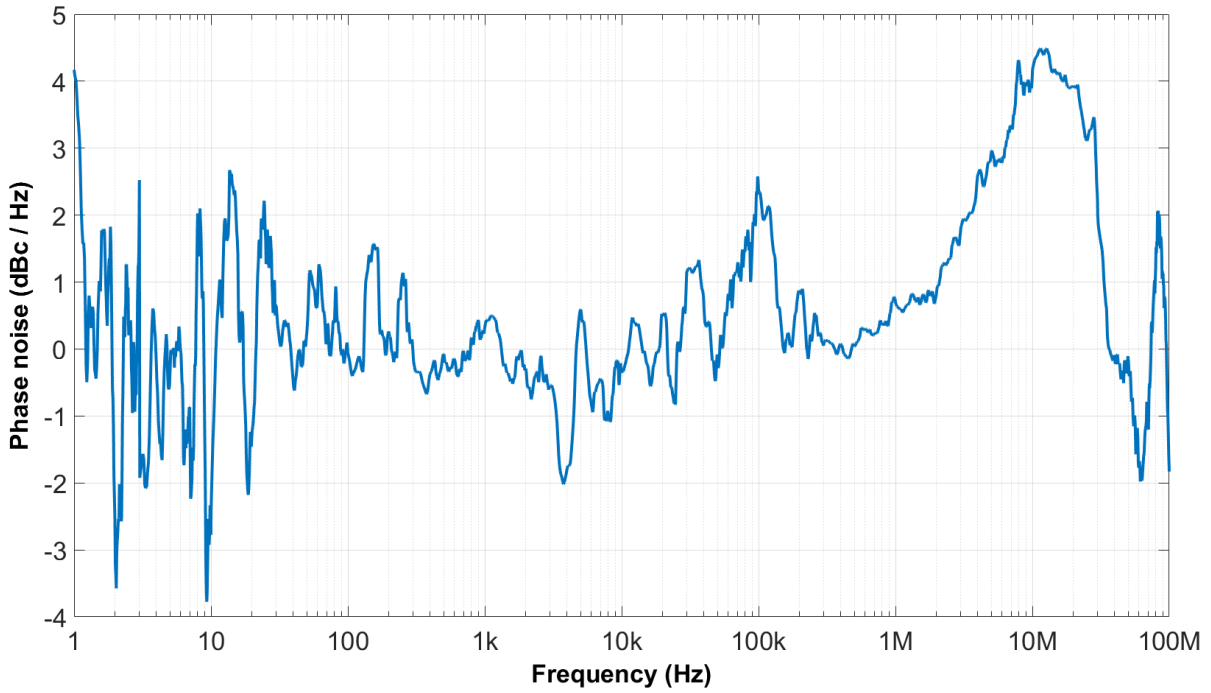


Figure 5.18: The difference between output before and after the NB7L1008 clock buffer.

5.4. Design 2

The board built to test the STW81200 is shown in figure 5.19.

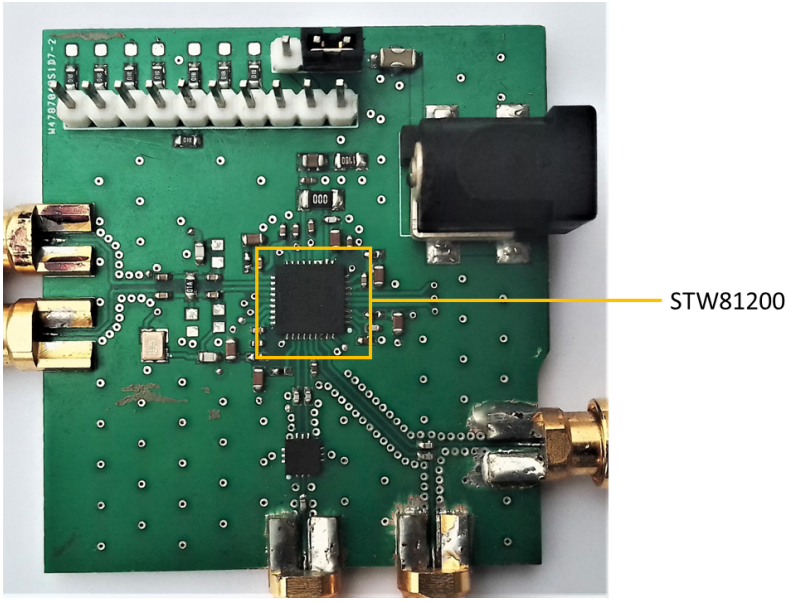


Figure 5.19: STW81200 test board.

5.4.1. Simulation

From the datasheet for the STW81200 the figure of merit for the phase noise floor is $\text{FOM}_{\text{chip floor}} = -227\,\text{dBc}\,\text{Hz}^{-1}$ and the figure of merit for the flicker phase noise is $\text{FOM}_{\text{chip flicker}} = -264\,\text{dBc}\,\text{Hz}^{-1}$. Which introduces the phase noise shown in figure 5.20.

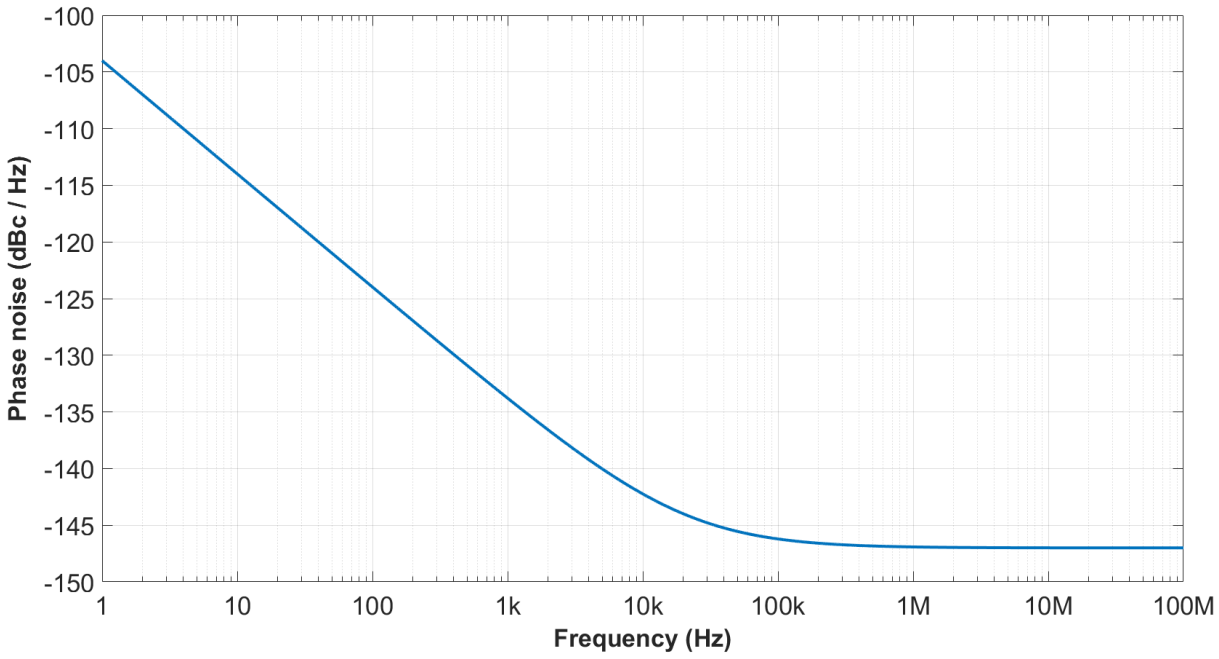


Figure 5.20: Phase noise introduced by the STW81200 PLL chip.

The loop filter used with the STW81200 PLL chip is implemented as shown in figure 5.21 and introduces the phase noise shown in figure 5.22.

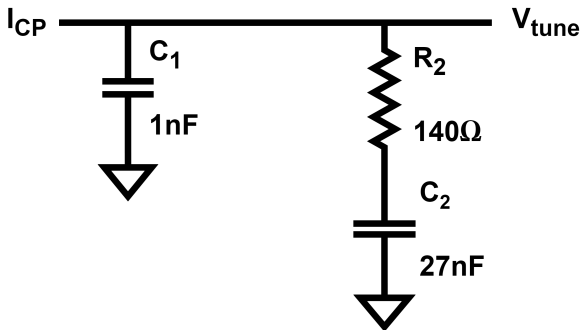


Figure 5.21: Loop filter of the STW81200 PLL.

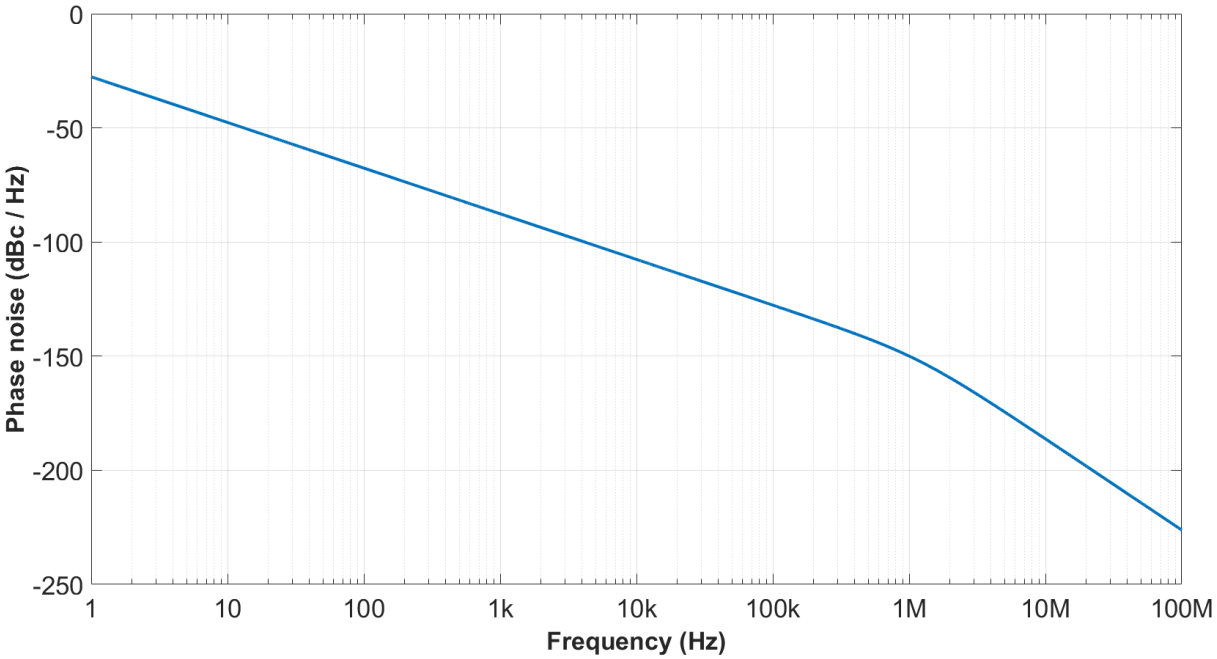


Figure 5.22: Phase noise introduced by the loop filter of the STW81200 PLL.

The phase noise of the build in VCO of the STW81200 at 3.439 GHz can be fit to the Leeson-culter model using the parameters below and is shown in figure 5.23.

$F = 18.981\,\mathrm{dB}$

$P_a = 2\,\mathrm{dBm}$

$f_c = 12\,\mathrm{kHz}$

$Q_l = 125$

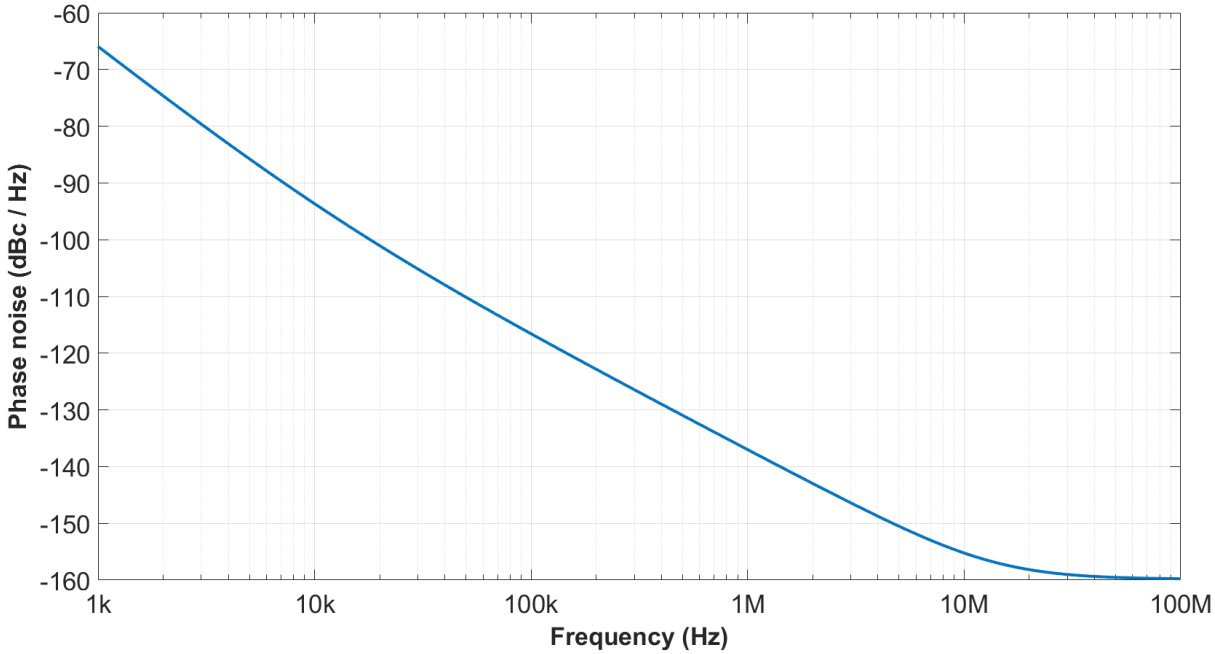


Figure 5.23: Leeson-Cutler model of the STW81200 VCO.

The charge pump gain of the STW81200 is set to $K_{\mathrm{PD}} = 4.9\,\mathrm{mA}$ and the tuning coefficient of the internal VCO at 3.439 GHz is $40\,\mathrm{MHz\,V^{-1}}$. The fractional N divider of the STW81200 is set to 34.39. With the given parameters, the gain cross-over frequency of the STW81200 PLL is 133.6 kHz with a phase margin of 65.5°. The closed-loop transfer function and error function of the STW81200 PLL are shown in figure 5.24.

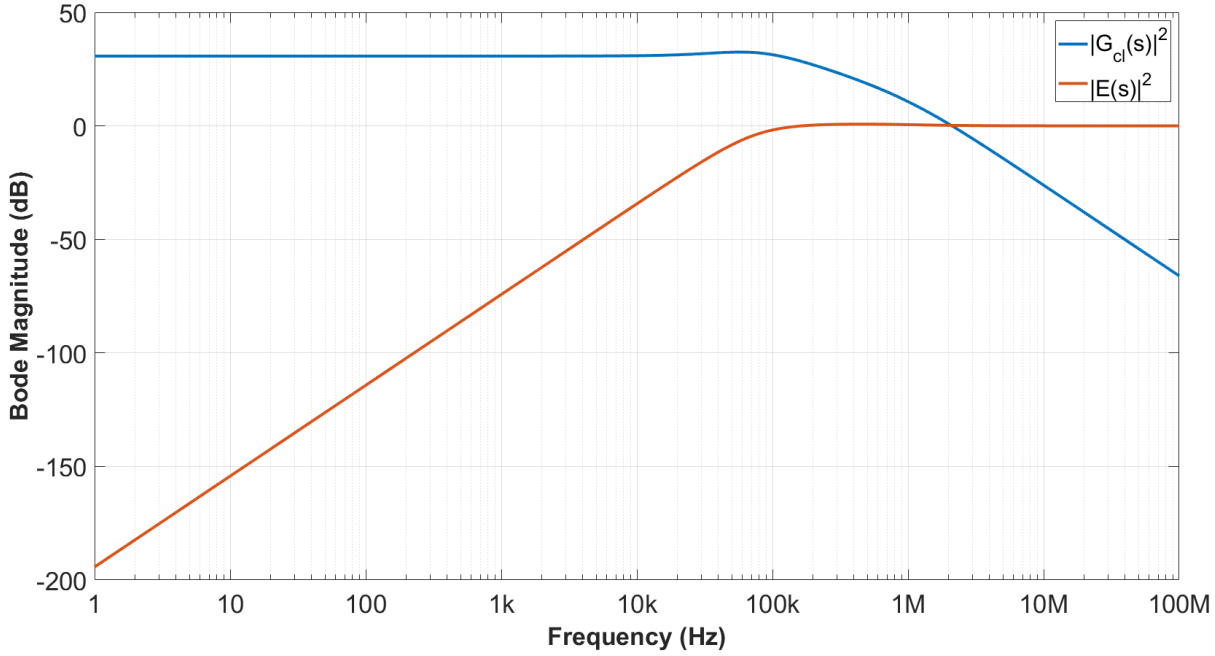


Figure 5.24: The bode magnitude plot of the closed loop and error signal transfer function of the STW81200 PLL.

Table 5.3 shows summary of the simulation results for the STW81200. The total RMS jitter integrated from 1 kHz to 50 MHz is 74.21 fs at 3.439 GHz and 57.77 fs at 2.3 GHz.

Table 5.3: Summary of the simulated phase noise of the STW81200 PLL at 3.439 GHz

Offset Frequency	1	10	100	1k	10k	100k	1M	10M	100M
Reference Oscillator	-70.50	-100.53	-125.76	-146.75	-160.06	-161.03	-161.05	-161.05	-161.05
PLL Chip	-104.00	-114.00	-123.98	-133.79	-142.24	-146.21	-146.91	-146.99	-147.00
Total feed-forward phase noise	-70.50	-100.34	-121.77	-133.57	-142.16	-146.07	-146.75	-146.82	-146.83
Gain of the closed loop transfer function	30.73	30.73	30.73	30.73	30.89	31.34	10.69	-26.13	-66.08
Feed-forward contribution	-39.77	-69.61	-91.04	-102.84	-111.27	-114.73	-136.06	-172.95	-212.92
Loop filter	-27.63	-47.63	-67.63	-87.63	-107.63	-127.66	-149.98	-186.26	-226.20
VCO	23.71	-6.28	-36.25	-65.94	-93.66	-116.59	-137.00	-155.23	-159.76
Total error signal phase noise	23.71	-6.28	-36.25	-65.91	-93.49	-116.26	-136.79	-155.23	-159.76
Gain of the error signal transfer function	-194.25	-154.25	-114.25	-74.25	-34.32	-1.83	0.55	0.01	0.00
Error signal contribution	-170.53	-160.53	-150.49	-140.16	-127.81	-118.09	-136.24	-155.21	-159.76
Total phase noise	-39.77	-69.61	-91.04	-102.84	-111.18	-113.08	-133.14	-155.14	-159.76

5.4.2. Measured results

The simulated and measured phase noise of the STW81200 PLL at an output frequency of 2.3 GHz is shown in figure 5.25. The curves are closely matched except at very low offset frequencies, this mismatch is discussed in the first paragraph of subsection 5.2.2.

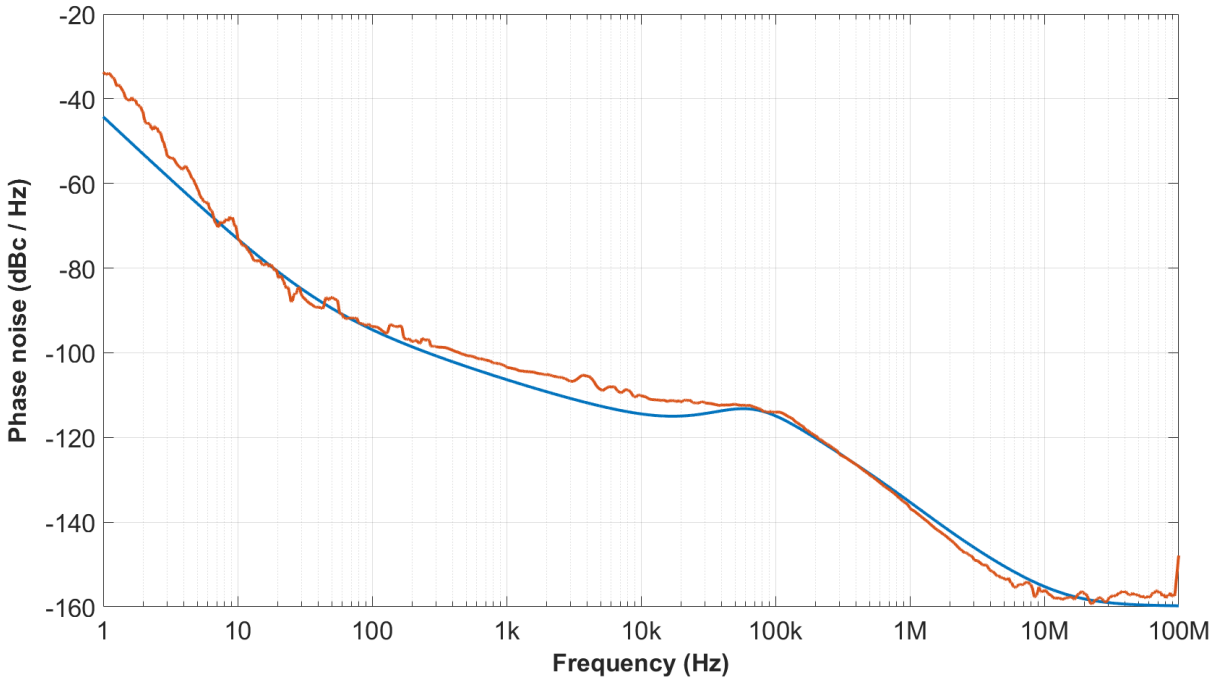


Figure 5.25: Measured phase noise of STW81200 at2.3 GHz.

Figure 5.26 shows the measured and simulated phase noise of the STW81200 PLL at an output frequency of 3.439 GHz. The phase noise introduced by the delta-sigma modulator is shown in the final decade of the plot.

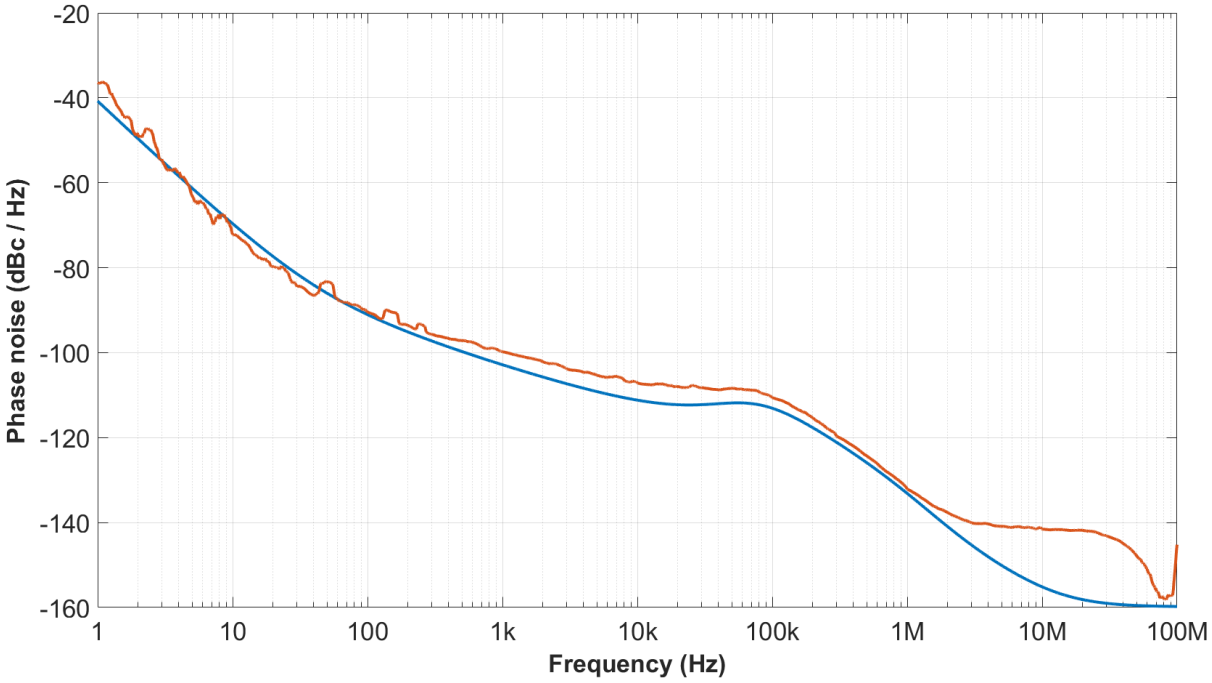


Figure 5.26: Measured phase noise of STW81200 at 3.439 GHz.

Figure 5.27 shows the effect of dithering which creates phase noise to suppress spurs.

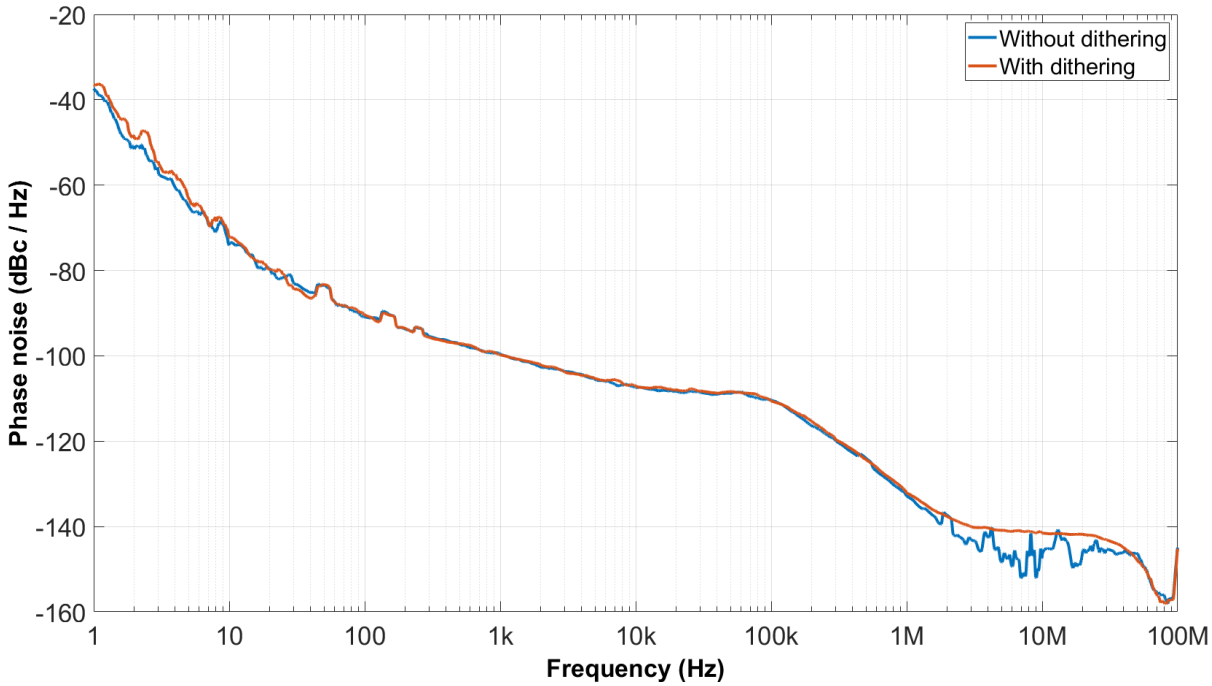


Figure 5.27: STW81200 fractional-N output with dithering and without dithering.

5.4.3. Reference oscillator clock buffers.

Figure 5.28 is the test board used to measure the phase noise of the reference oscillator and reference oscillator distribution chips.

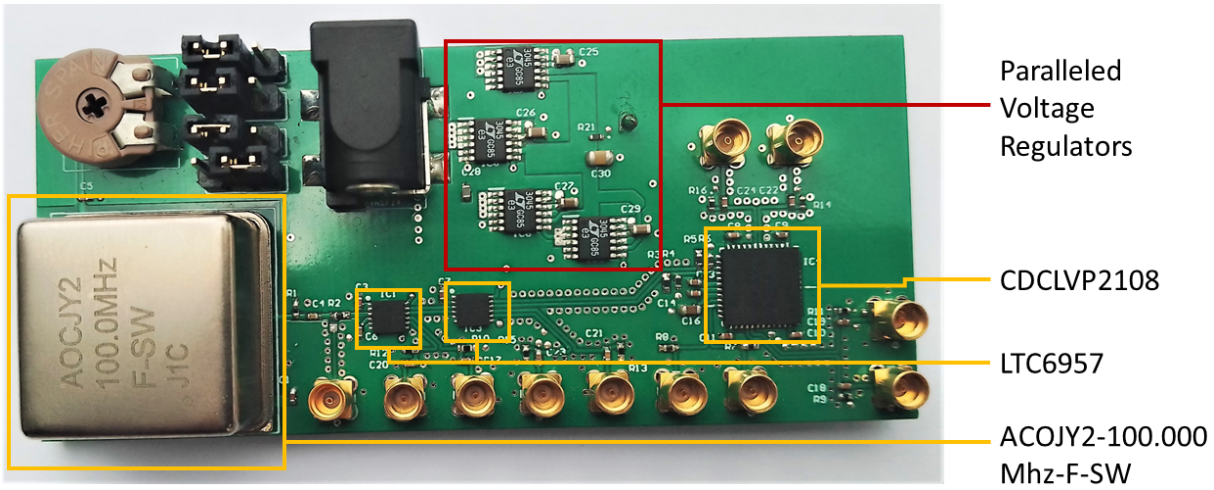


Figure 5.28: Reference Oscillator distribution board.

Figure 5.29 shows the phase noise at the outputs of each of the clock buffers used to distribute the reference oscillator in design two as well as the phase noise at the output of the reference oscillator itself. It's clear that each subsequent clock buffer degrades the phase noise floor of the reference oscillator and that at low offset frequencies the phase noise of the reference oscillator dominates the output of all the clock buffers. The first clock buffer degrades the phase noise floor of the oscillator the most. This is because the phase noise floor of the reference oscillator is much lower than the phase noise floor of any of the clock buffers.

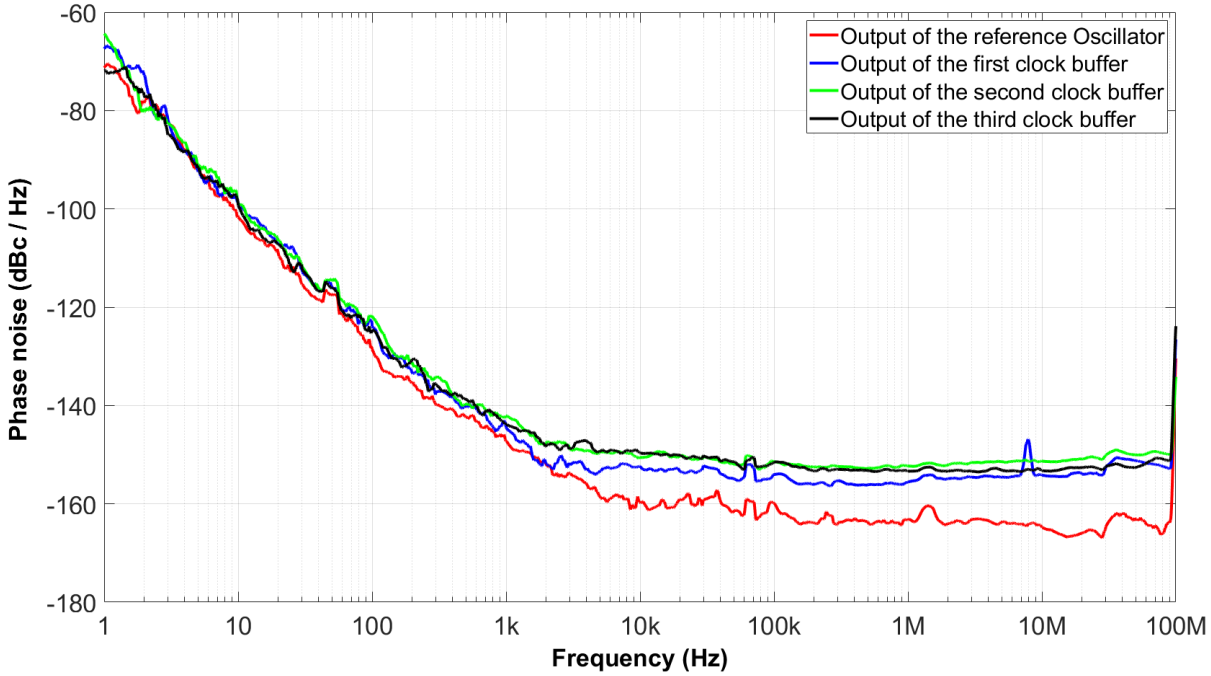


Figure 5.29: Phase noise of reference oscillator at different buffers.

Figure 5.30 shows the effect of the additive phase noise of the second LTC6957 clock buffer and the CDCLVP2108 clock buffer. The blue curve is the output of the STW81200 set to a frequency of 3.439 GHz using the reference oscillator signal after the first LTC6957 clock buffer. The orange curve is the same setup but using the reference oscillator signal after the CDCVPL2108 clock buffer. The outputs of the PLL are the same.

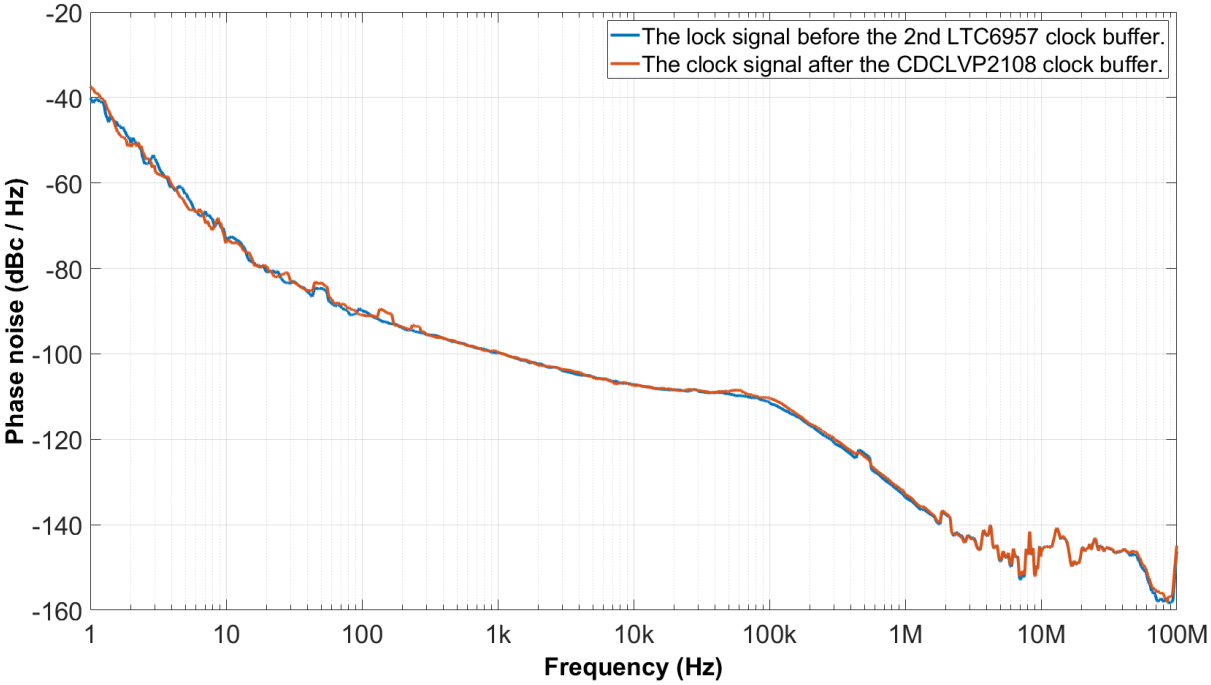


Figure 5.30: Output of STW81200 using different the reference oscillator signal from different clock buffers.

Chapter 6

Summary and Conclusion

The ADF4356 is more cumbersome to program than the STW81200. The ADF4356 also produces more phase noise than the STW81200 when achieving the same frequency, despite being more expensive. The simplicity of use of the STW81200, with its built-in LDOs and straightforward register maps, along with its phase noise performance make it a better choice than the ADF4356 in either design.

The fixed frequency LO of the first design has less phase noise than the fixed frequency LO of the second design and the first design also presents less uncorrelated phase noise to the radio channels. The second design is cheaper. The final decision largely depends on how many channels will be present on a single radio PCB in the final implementation of the array. Should two [as shown in figure1.1] to four channels be present on a PCB the first design is still cost-competitive and provides better performance.

More channels on a single radio PCB drives down the cost of the second design as fewer STW81200 chips are needed to generate all the required LO signals: With more channels on a single PCB, the output of a single PLL chip can be amplified and power divided to achieve the requisite number of LOs. If eight channels are serviced per PCB, as shown in figure 6.1,

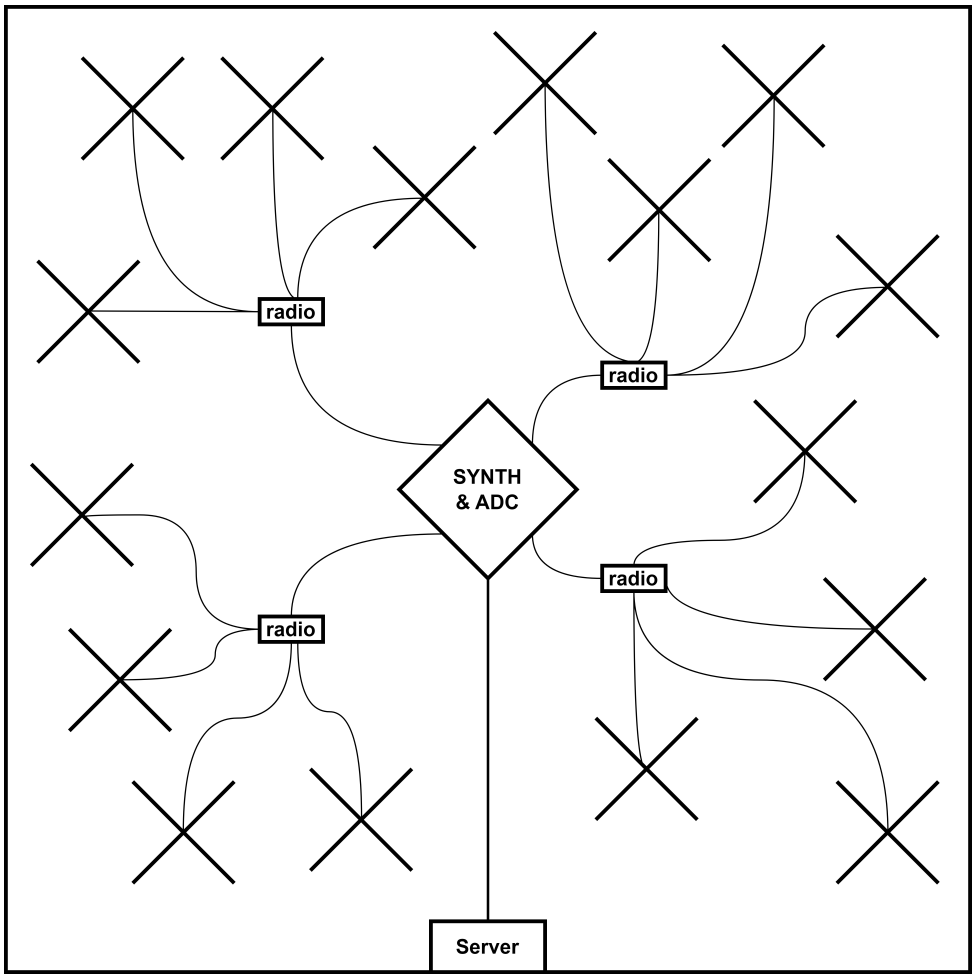


Figure 6.1: Layout of the antenna array with eight channels being serviced per radio PCB.

a hybrid between the two LO designs can be used to keep the high performance of HMC703, with an external VCO, and avoid distributing the variable frequency LO between circuit boards. The design scheme for such a frequency synthesizer is shown in figure 6.2.

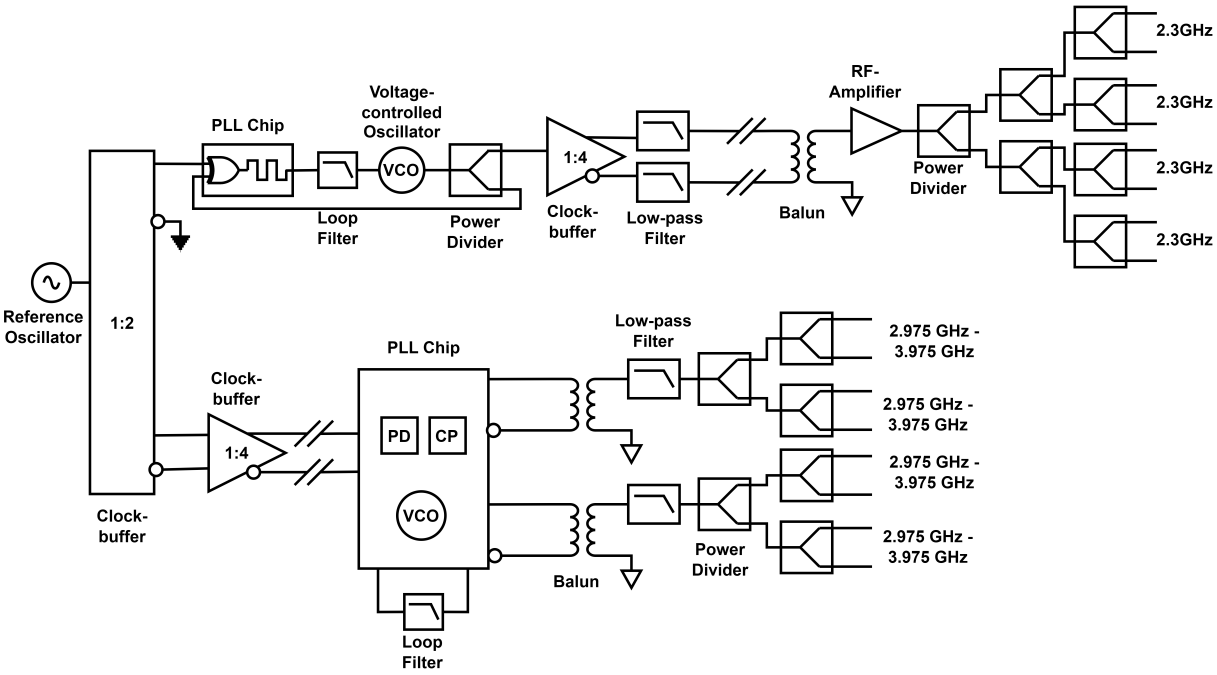


Figure 6.2: Final design proposal.

Table 6.1 shows the cost of the components of the hybrid design. The hybrid design would require 64 RG58 coaxial cables costing R18000. Although fewer PCBs are used in the layout shown in figure 6.1, each PCB is larger, so the PCB cost is still around R3000. The total cost for the hybrid design is R31089. This design is cheaper and performs better than the other two.

Table 6.1: Summary of the component cost of the proposed hybrid design.

	Part Number	Price Per Unit	no. of units	Total price
Reference Oscillator	ACOJY2-100.000Mhz-F-SW	3747.268	1	3747.268
1:2 Clock Buffer	LTC6957-1	218.5	1	218.5
Integer-N PLL Chip	HMC703	561.00	1	561
VCO	DCRO196202-5	546.43	1	546.4285714
1:4 Clock Buffer	NB7L1008	144.97	1	144.97
Low Pass Filter	LFCW-332+	106.4	2	212.8
Balun	NCS2-33+	25.46	4	101.84
Amplifier	ERA-1+	45.91	4	183.64
1:2 Clock Buffer	LTC6957-3	218.5	2	437
Fractional-N PLL Chip	STW81200	284.43	4	1137.72
Balun	MTX2-73+	47.12	8	376.96
Low Pass Filter	3550LP14A300T	9.956	8	79.648
Power Divider	GP2Y1+	45.03	52	2341.56
Total				10089.33

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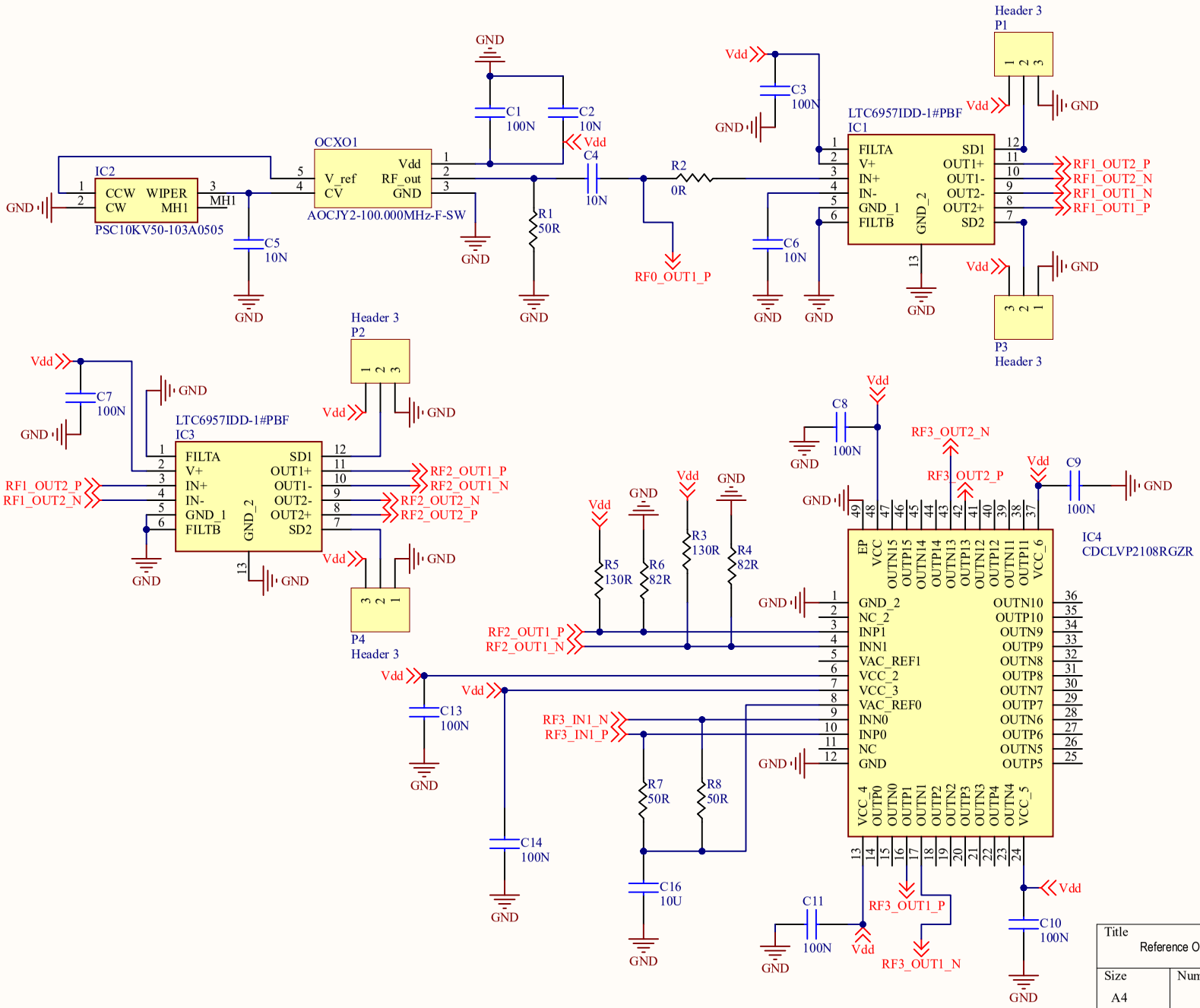
Appendix A

Circuit Diagram of the Reference Oscillator Test Board.



Title: Reference Oscillator Prototype Board

Size	Number	Revision
A4	N/A	N/A

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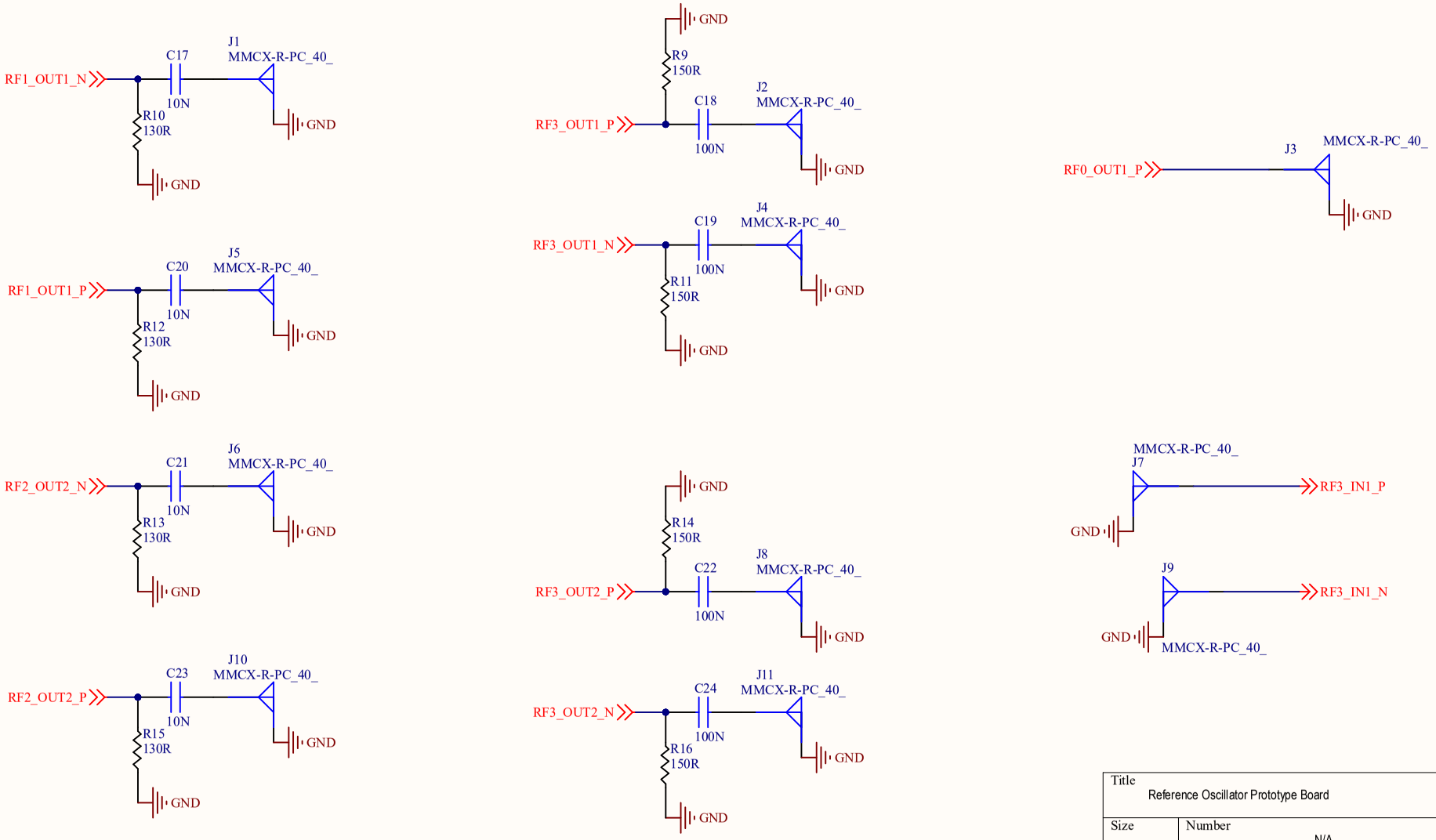
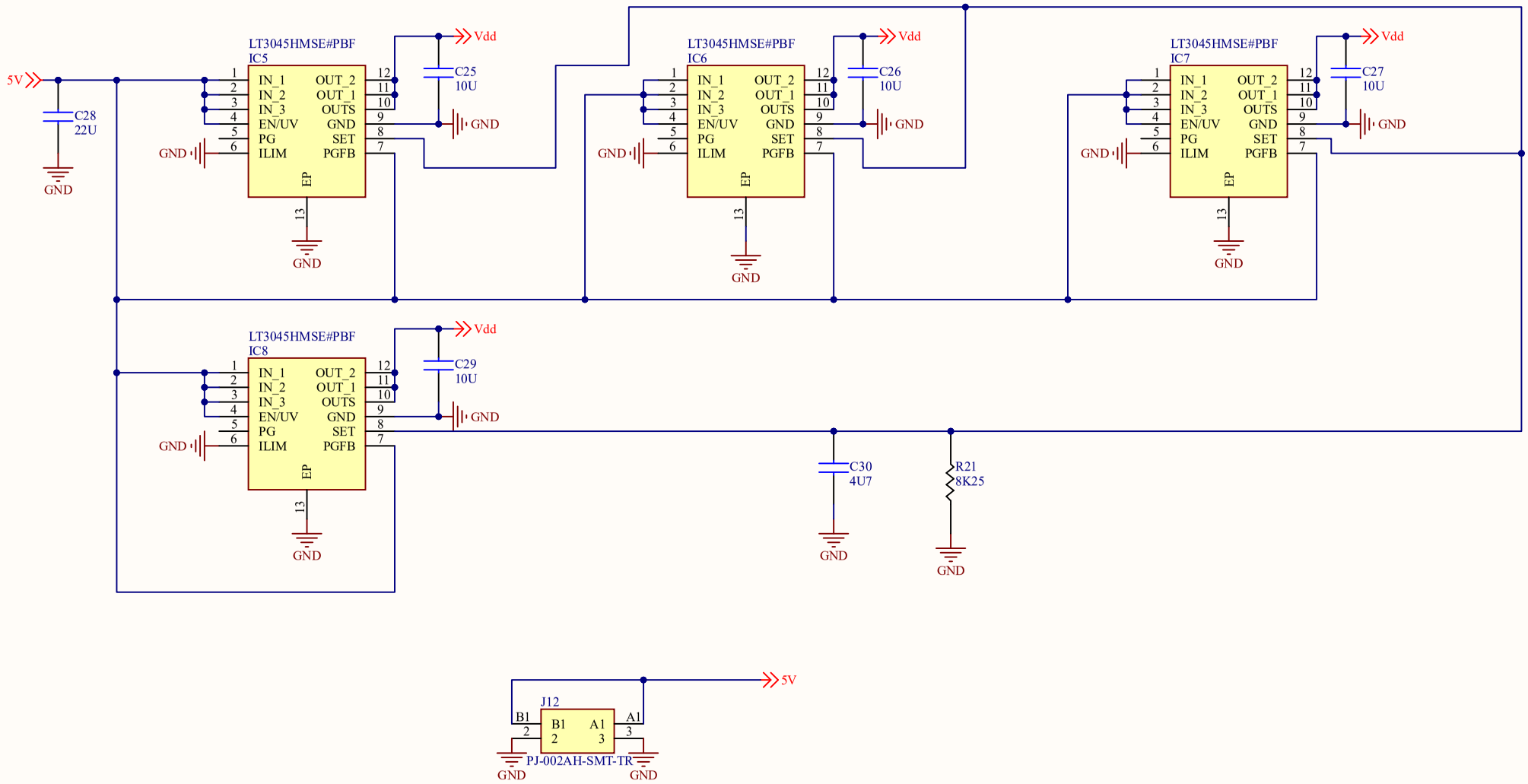


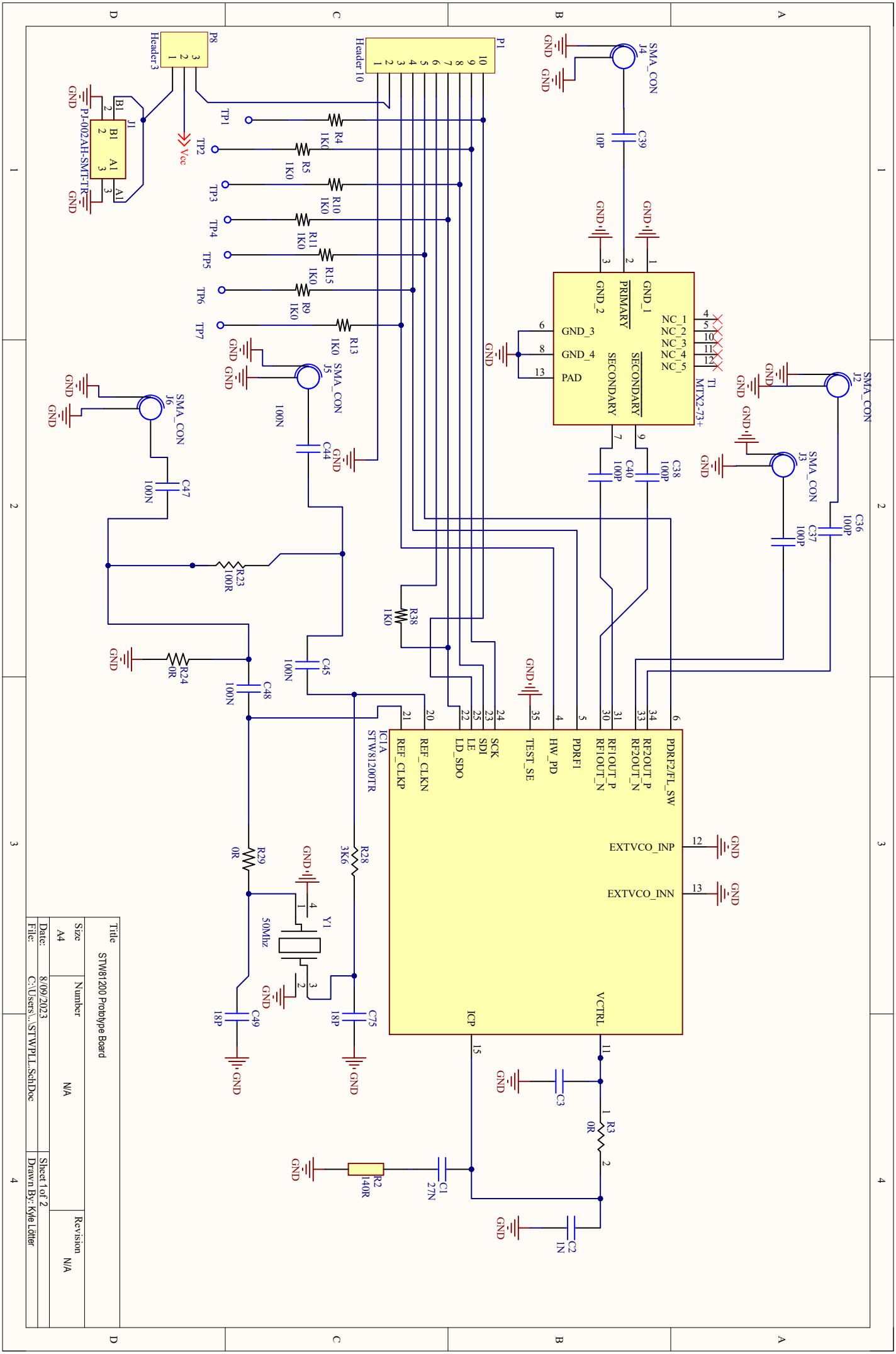
Title: Reference Oscillator Prototype Board		
Size: A4	Number: N/A	Revision: N/A
Date: 8/09/2023		Sheet 2of 3
File: C:\Users\..\Sheet2.SchDoc		Drawn By: Kyle Lötter

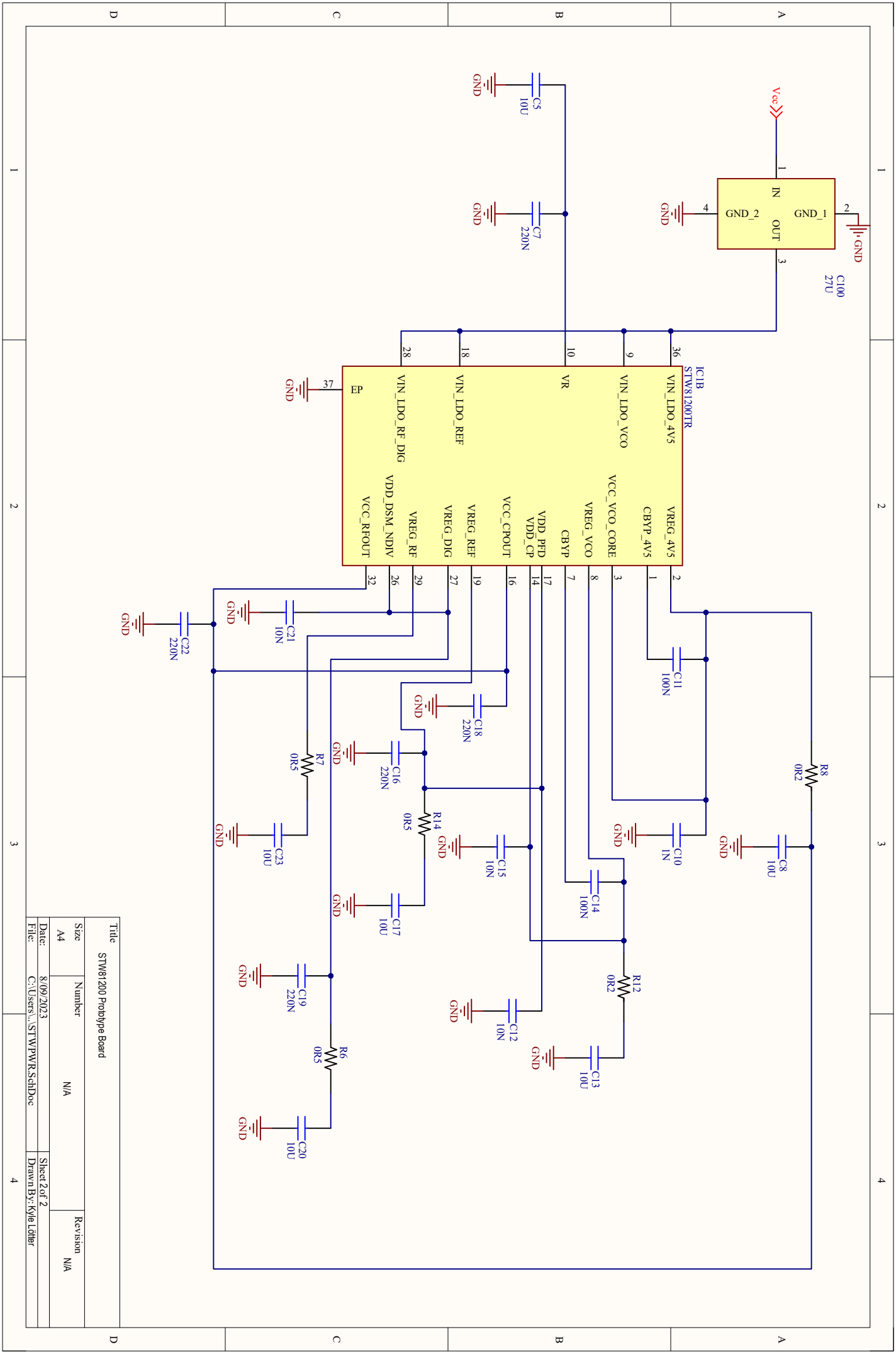


Title: Reference Oscillator Prototype Board		
Size: A4	Number: N/A	Revision: N/A
Date: 8/09/2023		Sheet 3 of 3
File: C:\Users\..\Sheet3.SchDoc		Drawn By: Kyle Lötter

Appendix B

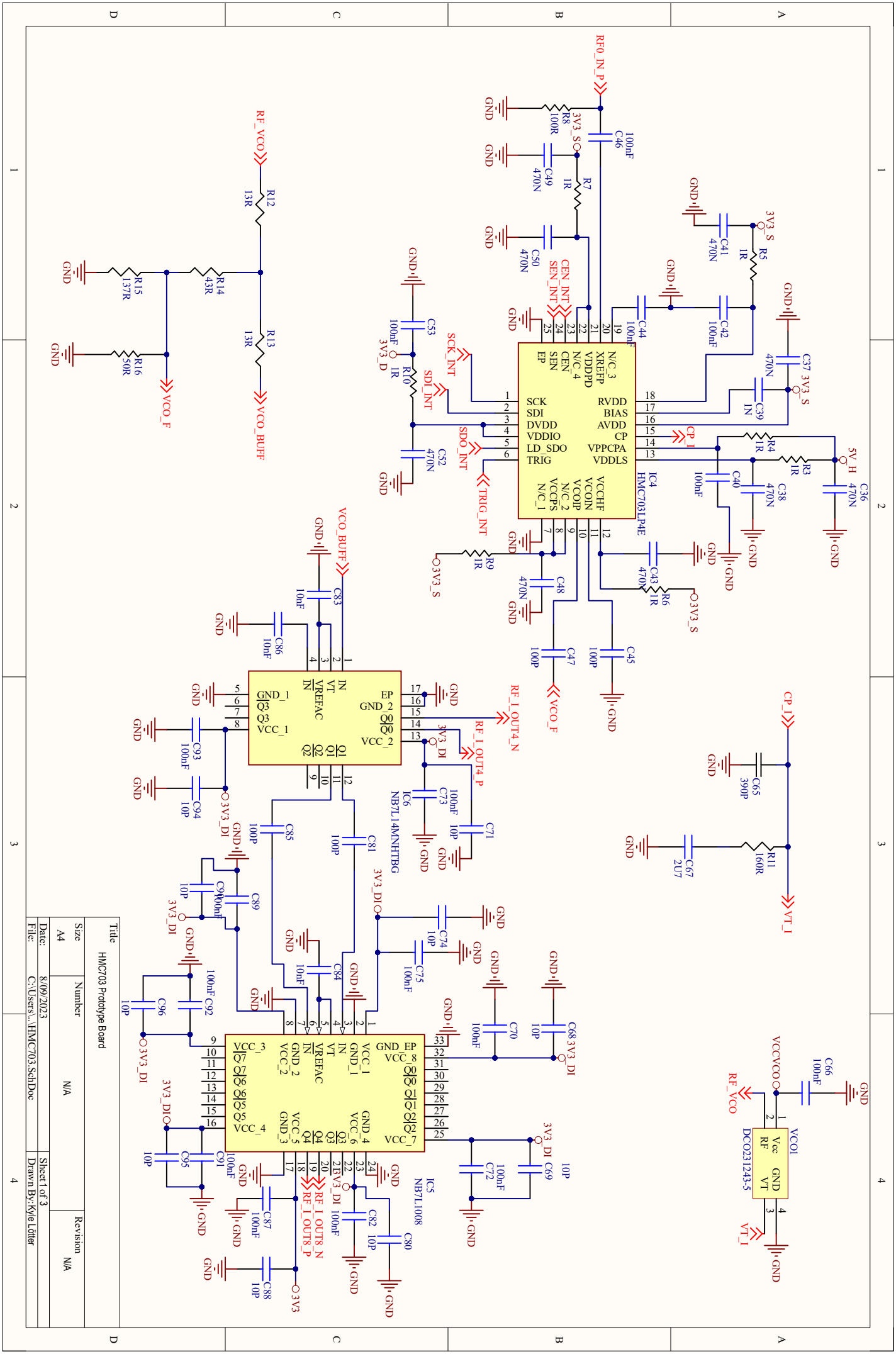
Circuit Diagram of the STW81200 Test Board.



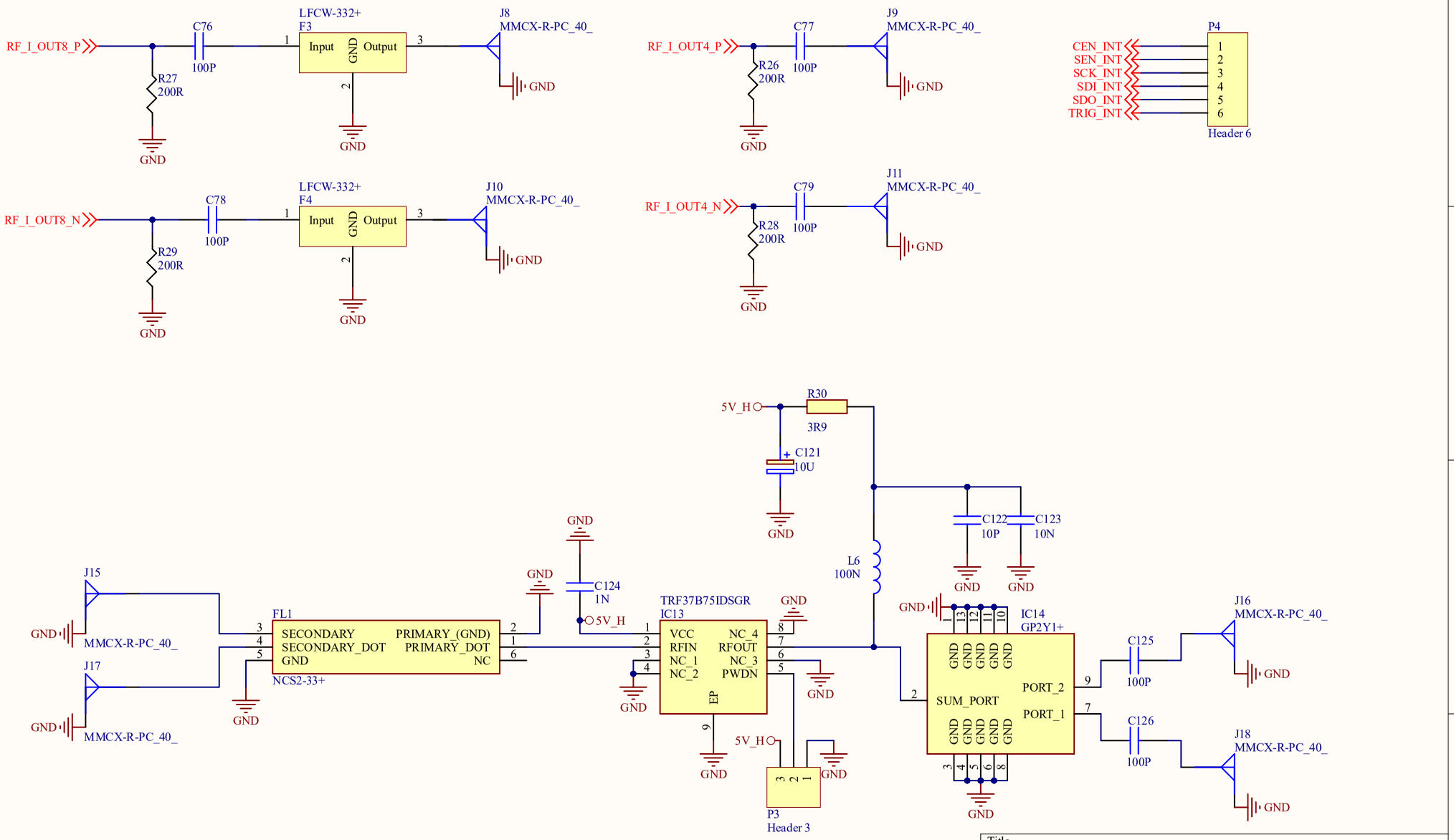


Appendix C

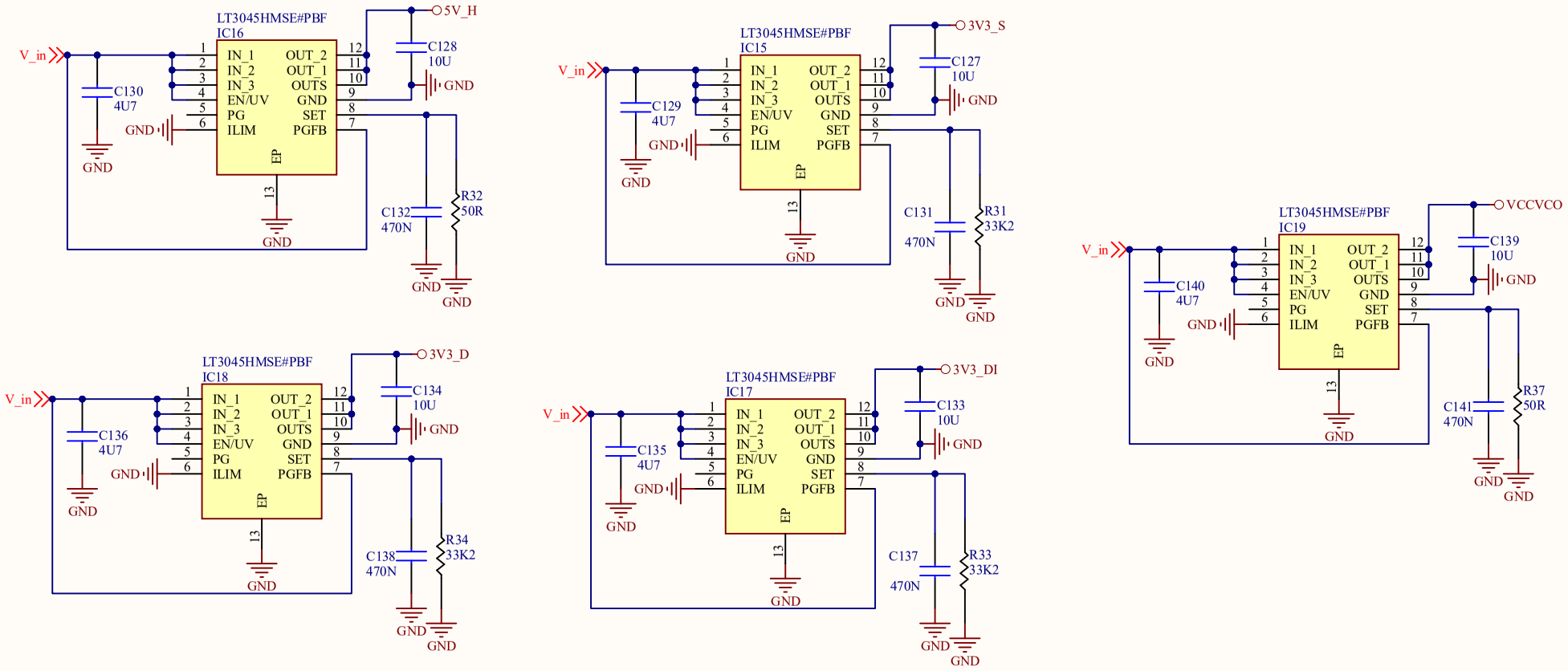
Circuit Diagram of the HMC703 Test Board.



Title	HMC703 Prototype Board		
Size	Number		Revision
A4		N/A	N/A
Date:	8/09/2023		Sheet 1 of 3
File:	C:\Users\...HMC703.SchDoc		Drawn By: Kyle Lötter



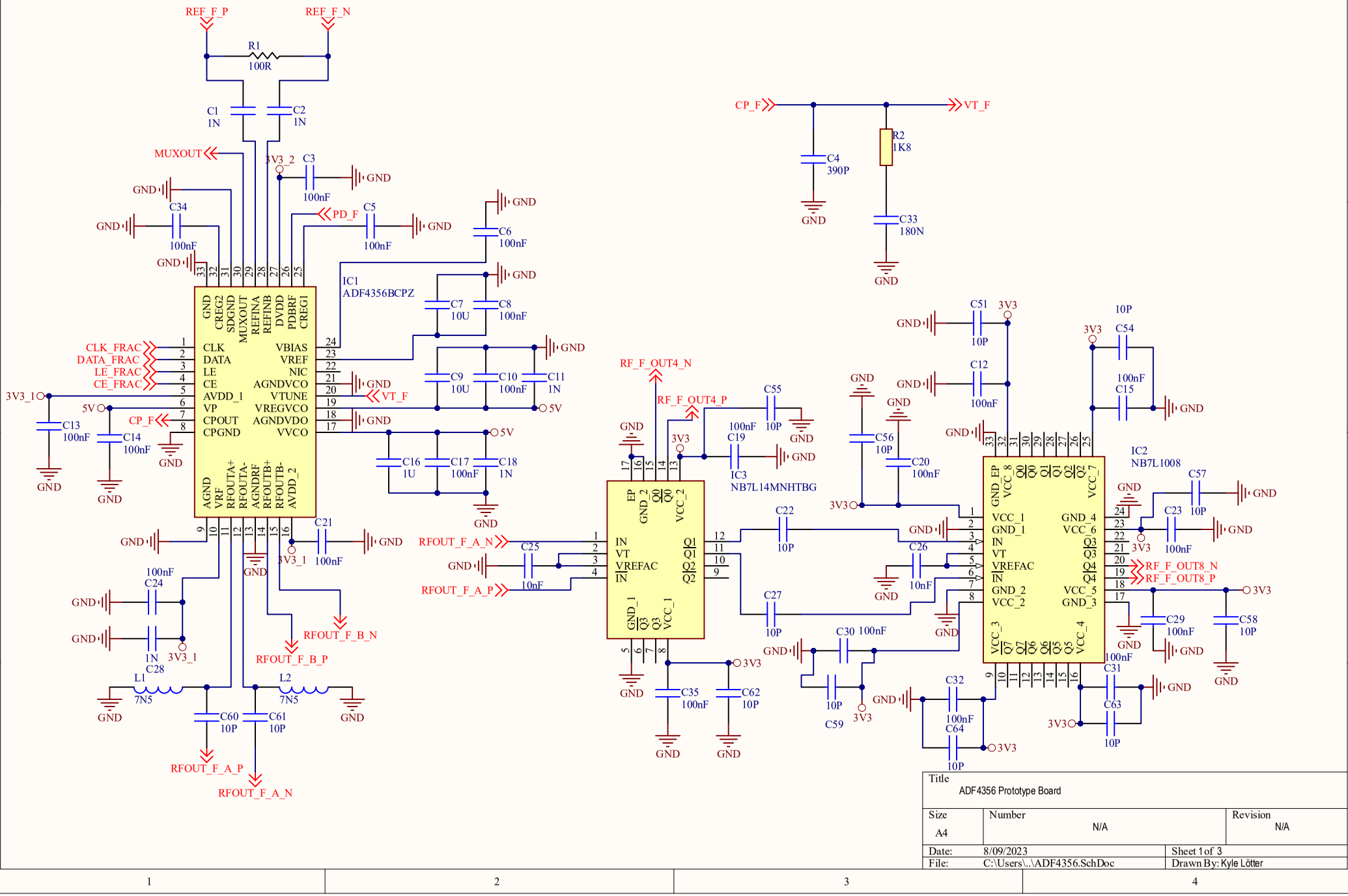
Title	HMC703 Prototype Board	
Size: A4	Number: N/A	Revision: N/A
Date: 8/09/2023		Sheet 2 of 3
File: C:\Users\...\HMCCON.SchDoc		Drawn By: Kyle Lötter

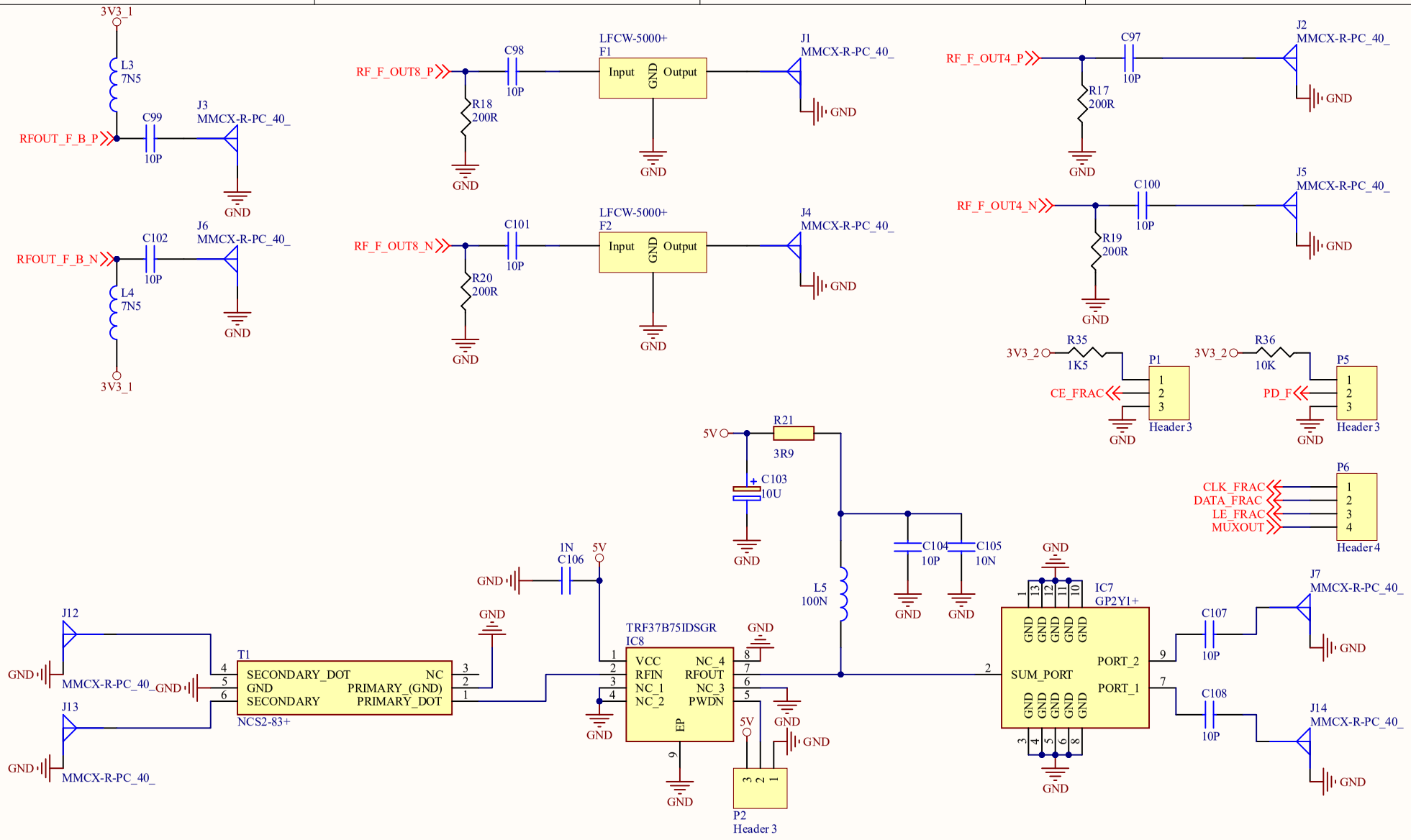


Title	HMC703 Prototype Board		
Size	Number		Revision
A4	N/A		N/A
Date:	8/09/2023	Sheet 3of 3	
File:	C:\Users\...\HMCPOW.SchDoc	Drawn By: Kyle Lötter	

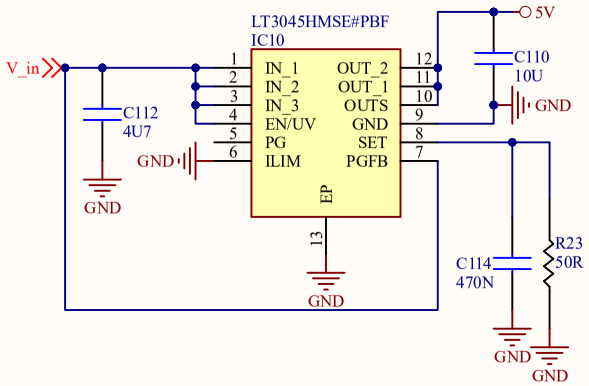
Appendix D

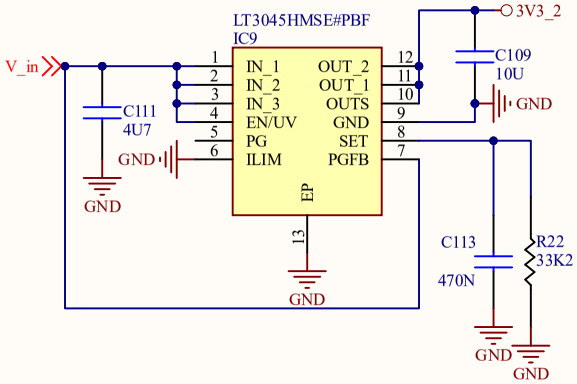
Circuit Diagram of the ADF4356 Test Board

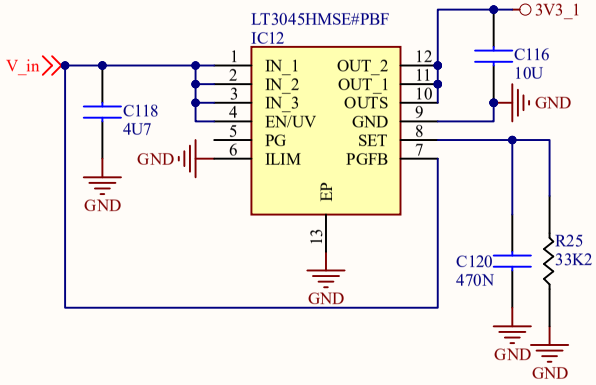


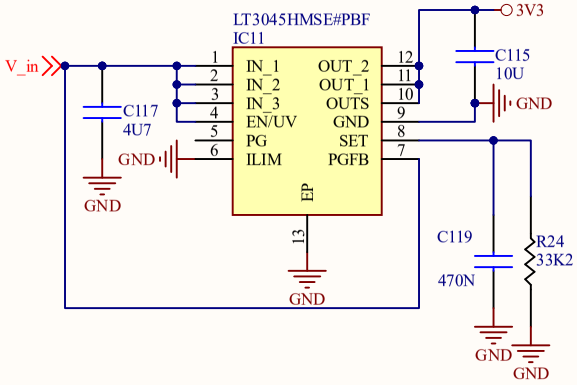


Title	ADF4356 Prototype Board	
Size: A4	Number: N/A	Revision: N/A
Date: 8/09/2023		Sheet 2 of 3
File: C:\Users\...\ADFCON.SchDoc		Drawn By: Kyle Lötter









Title: ADF4356 Prototype Board		
Size: A4	Number: N/A	Revision: N/A
Date: 8/09/2023		Sheet 3 of 3
File: C:\Users\...\ADFPOW.SchDoc		Drawn By: Kyle Lötter