Analysis and Design of a Voltage Regulator Based on an AC-to-AC Converter

By

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DECLARATION

I, the undersigned, hereby declare that the work contained in this thesis is my own original work and that I have not previously in its entirety or in part submitted it at any university for a degree.

SUMMARY

This thesis discusses the analysis and design of a voltage regulator based on an AC-to-AC converter. A background study was performed on the best topology for the purpose. The chosen topology was analysed and the converter was designed in detail. A voltage sign-detector and an over-current detector were designed and built. They were used for control and protection. Three methods of control were investigated. The first was a slow but reliable method of computing the RMS value of the input voltage and then using that value and the RMS value of the desired output voltage to compute the duty ratio of the converter. The second method was fast and is an open-loop control method, where the measured input voltage and a reference value of the desired output voltage are used to compute the duty ratio. The third method is a closed-loop control method in which the input voltage, output voltage and the same reference values used in the second method are used to compute the duty ratio. All of these methods were implemented and tested.

OPSOMMING

Hierdie tesis bespreek die analise en die ontwerp van 'n spannings reguleerder wat gebaseer is op 'n WS-na-WS omsetter. 'n Ondersoek was ingestel om die beste topologie te vind vir die doel. Die topologie wat gekies is, is toe geanaliseer en die omsetter is in detail ontwerp. 'n Spannings-teken-detektor baan as ook 'n oorstroombeskermings baan was ontwerp en is gebou. Hierdie bane word gebruik vir die beheer en die beveiliging van die stelsel. Daar is drie metodes van beheer wat ondersoek is. Die eerste metode is stadig, maar betroubaar. Die metode bereken die WGK waarde van die intree spanning en gebruik dan die waarde en die WGK van die gewenste uittree spanning om die diens siklus van die omsetter uit te werk. Die tweede metode van beheer is vinnig en is 'n oop-lus metode van beheer. Hierdie metode maak gebruik van die gemete intreespanning en 'n verwysing van die gewensde uittree spanning om die dienssiklus uit te werk. Die derde metode is 'n geslote-lus beheer wat van die gamete intreespanning, die gemete uittreespanning en die verwysing soos die in die tweede beheermetode gebruik maak on die diens siklus uit te werk. Al die metodes was geimplementeer en getoets.

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And last, but most importantly, my Creator. Without His good grace and love I would never have reached this point in my life.

Glossary

Abbreviations

ADMD	After Diversity Maximum Demand
BS	Bi-directional Switch
CVT	Constant Voltage Transformer
DSP	Digital Signal Processor
EHV	Extra-High Voltage
EMC	Electro-Magnetic Coupling
EMI	Electro-Magnetic Interference
FPGA	Field-Programmable Gate Array
HV	High Voltage
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
LV	Low Voltage
MOV	Metal Oxide Viristor
MV	Medium Voltage
PWM	Pulse Width Modulation
RMS	Root Mean Square
SWER	Single Wire Earth Return
THD	Total Harmonic Distortion

Circuit Abbreviations

C_d	Input Capacitor
C_O	Output Filter Capacitor
C_{S1}	Positive Snubber Capacitor
C_{S2}	Negative Snubber Capacitor
$D_1 - D_4$	Free-wheeling Diodes
i_d	Input Current into Converter
i_L	Load Current
i_{Ls}	Input Current from Source
i_O	Output Filter Inductor Current

Glossary

L_O	Output Filter Inductor
L_S	Input Inductor – Transformer Leakage Inductance
R	Load Resistance
r_{Lo}	Inductor's Resistance - L_O
r_{Co}	Capacitor Series Resistance – C_O
$R_{\theta ja}$	Junction-to-Ambient Thermal Resistance
$R_{\theta jc}$	Junction-to-Case Thermal Resistance
$R_{\theta ch}$	Case-to-Heat-sink Thermal Resistance
$R_{\theta ha}$	Heat-sink-to-Ambient Thermal Resistance
$S_1 - S_4$	IGBT switches
U_n	Nominal Voltage
v_C	Input Capacitor Voltage
v_{Cs1}	Positive Snubber Capacitor Voltage
v_{Cs2}	Negative Snubber Capacitor Voltage
v_d	Input Voltage - Transformer Secondary Voltage
v_L	Load Voltage
V_{LL}	Line-to-Line Voltage
V_{LN}	Line-to-Neutral Voltage
v_O	Unfiltered Output Voltage

Units

A	Ampere
°C	Degrees Celsius
F	Farad
H	Henry
Hz	Hertz
V	Volt
VA	Volt-Ampere – Apparent Power
W	Watt
Ω	Ohm

Glossary

Other symbols

D	Duty Ratio
$E_{i(cond)}$	Conduction Energy during i'th Switching Period
$E_{i(switch)}$	Switching Energy during i'th Switching Period
E_{off}	IGBT Turn-off energy
E_{on}	IGBT Turn-on energy
f_1, ω_1	Fundamental Frequency
f_S, ω_S	Switching Frequency
m_a	Modulation Index
M_P	Maximum Point of Voltage Overshoot
P_{cond}	Conduction Power Losses
$P_{cond(S1)}$	Conduction Power Losses for S_1
$P_{cond(S3)}$	Conduction Power Losses for S_3
$P_{cond(D4)}$	Conduction Power Losses for D_4
$P_{cond(D2)}$	Conduction Power Losses for D_2
P_{switch}	Switching Power Losses
P_{tot}	Total Power Losses
s	Switching Function
t_{off}	IGBT Turn-off Time
t_{on}	IGBT Turn-on Time
t_S	Settling Time
T_S	f_S's Period
$V_{on(IGBT)}$	IGBT On-State Voltage
$V_{on(diode)}$	Diode On-State Voltage
ξ	Damping Ratio
τ	DT_S

Chapter 1

Introduction

1 Introduction

1.1 The research problem

Eskom, South Africa's main utility, has a policy to supply low-cost electricity to al the people of South Africa. Most people without electricity live in rural communities far from the national power grid [4]. In some of the cases it will be more cost effective to lengthen a medium-voltage (MV) line rather than to build a longer high-voltage (HV) line. To be able to do this a reliable dynamic voltage regulator will be needed.

A wide variety of voltage regulators are available. Some of these are tap-changing transformers and variations on them. Converter-based solutions also exist and these range from phase-controlled converters to two DC-to-AC converters placed back-to-back.

These solutions are well established but, as will be discussed, they each have certain restrictions. The solution that is investigated in this report is an AC-to-AC converter based on a buck converter. Figure 1-1 shows the proposed converter topology.
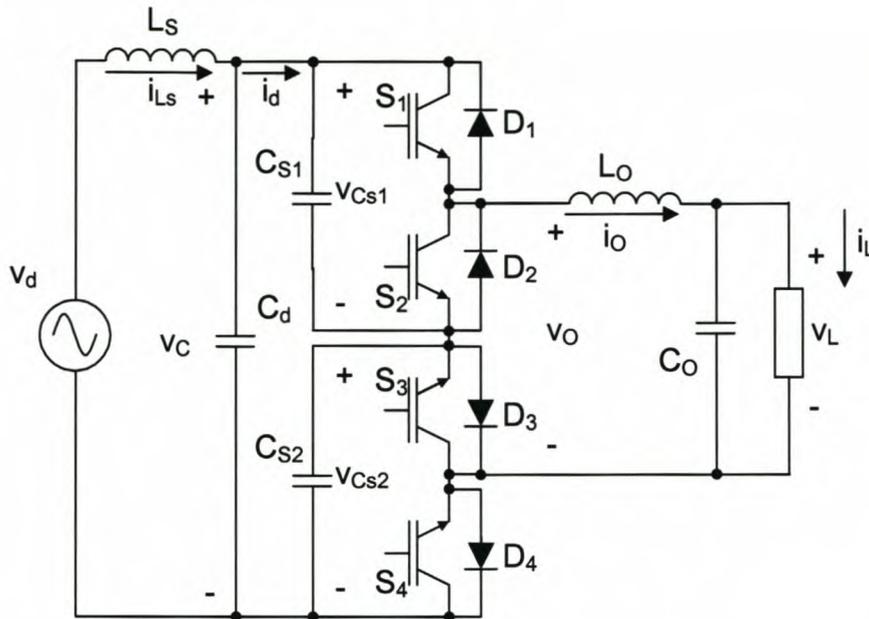
Figure 1-1: Proposed converter topology

This topology will be discussed in detail later in this report, but it needs to be said that it consists of two IGBT phase arms ($S_1 - S_4$), an input filter (L_S and C_d) and an output filter (L_O and C_O). It also has two snubber capacitors (C_{S1} and C_{S2}). The input inductor represents the step-down transformer's leakage inductance. This transformer is at the end of the MV line and v_d represents the transformer's secondary voltage.

The converter was analysed and equations were found for the voltages and currents. The equations for the output filter components and losses in the switches were derived. The unfiltered output voltage was analysed and the amplitude spectrum of both the AC-to-AC converter and the DC-to-AC converters was found. The total harmonic distortion (THD) of the voltages was computed. The current paths in the converter were considered during fault stages.

When this analysis was completed, the converter could be designed. The first component to design was the switching components with their peak voltages, currents and losses. The efficiency of the converter at various input voltages was computed. This was followed by the driver circuit design. The output filter

inductor and capacitor were designed next. The protection circuit and the sign detection circuit designs were followed by the snubber capacitor's design.

Attention was then given to the digital control. Three control methods were investigated. The first entailed measuring the input voltage v_C and computing the RMS value of this voltage over one 50 Hz signal. The converter's duty ratio (D) is the output voltage v_L divided by the input voltage v_C. The output voltage's RMS value is known; the input voltage's RMS is now computed and with this D can be found. This method is accurate but it is slow, because the duty ratio is updated only once in a 50 Hz cycle.

The second method of control is where the duty ratio is computed once every switching period. This is done by dividing a generated reference voltage by the measured input voltage, v_C. This is a type of open-loop control and is efficient, but closed-loop control will be a more accurate option. This leads to the last method of control, namely the closed-loop control. The controller used is a proportional (P) type, just a constant value multiplied with the error signal. This error signal is the generated reference voltage minus the output voltage. This is negative feedback.

The startup conditions were discussed and the heat-sinks were designed. The transformer's specifications were stated last.

An experimental setup was built and tests done to prove the theoretical design. It was found that the first type of control operates the best because the input voltage was purely sinusoidal and the control updates D only once each cycle. Both the open-loop and closed-loop had the same problem with the zero-crossing. The problem is that there is a phase shift between the voltage and current and through the zero-crossing there is a step in the current. This step leads to oscillations in both current and voltage. The problem was solved, although some research is still needed on finding a better solution the problem in the closed-loop control method.

The measured values were compared with simulation results and found to compare well. Amplitude spectrums of the measured and simulated voltages were found and the THD of the unfiltered output voltage and the filtered output voltage was found. The THD of v_L is within specifications.

The efficiency was measured and compared with the computed values. It was shown with measurements that the output voltage remains constant if the input voltage is within its limits. A non-linear load was attached to the converter and it was found that the third harmonic is a problem. The measurements concluded with the fault-detection tests.

1.2   Structure of the report

This report is divided into six main parts or chapters.

In the second chapter some existing solutions not based on AC-to-AC converters will be discussed. Initially the origin of this project and the basic design criteria for the converter are explained. Some solutions such as the well known tap-changing transformer and variations on it are described. Other types of regulators are also briefly discussed before the converter based solutions are introduced with the AC-to-DC and DC-to-AC converters.

In Chapter Three some existing AC-to-AC converters already published are investigated. A detailed discussion then follows, describing the standard AC-to-AC converter cell using current control and voltage control methods. This is then followed by a description of the differential AC-to-AC converter cell again using current control and voltage control methods. The converter is changed from a buck converter to a boost converter and the drawbacks of this type of converter are highlighted. In the final part the transformer to be used is discussed.

Chapter Four consists of the analysis and design of the converter. A detailed analysis is followed by the equations derived from it and they are then used to design the different components to be used. The designed converter is then practically implemented and tested.

In Chapter Five the results of both simulation and experimental setups are explained. Three different strategies are investigated and the results are compared. The harmonic content of the output voltage is investigated.

The last chapter contains the conclusions drawn from the project as well as suggestions on what can still be done to improve or expand the designed converter.

Chapter 2

Existing solutions

2 Existing solutions

In this chapter the research problem will be stated. Different types of solutions will be looked at, from the tap-changing transformers to DC-to-AC converters. There are several solutions to the problem and only a few of them can be investigated in the course of this thesis. Therefore the field of solutions will have to be narrowed down in this chapter. This will be done by selecting which of the proposed solutions will work best under given circumstances.

2.1 The need for voltage regulation

South Africa has a large rural community. Eskom, the main electricity supplier in Southern Africa, has dedicated itself to providing electricity to all people in South Africa at the lowest price. To achieve this objective, research was done into the different reticulation methods as well as the technologies surrounding the distribution of power.

Some communities to be served are isolated and a long distance from the existing power grid. The first decision to be made is whether extending the existing grid and high-voltage (HV) line is more cost effective than lengthening the nearest medium-voltage (MV) line [9]. Factors that influence this decision are distance, terrain, climate and future growth in the population as these all influence the type of conductor to be used and the support network required. An in depth study of these factors with case studies has been undertaken in a thesis entitled "Opportunities for in-line transistor-based technologies on MV and LV power distribution networks" [4].

In South Africa EHV, HV, MV and LV are defined as in Table 2-1. The U_n stands for nominal voltage.

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Extra-High Voltage (EHV)	220 kV < U_n ≤400 kV
High Voltage (HV)	44 kV < U_n ≤220 kV
Medium Voltage (MV)	1 kV < U_n ≤44 kV
Low Voltage (LV)	U_n ≤1 kV

Table 2-1: South African voltage definitions [42]

From [4] it can be seen that in certain cases it is better to extend the HV grid, but there are a significant number of situations in which lengthening the MV line will be the better option. Lengthening the MV line produces its own set of problems and generates some options in its own right. The obvious problem with a longer line is that the voltage drop over the line to the user will increase with each kilometre of conductor added. According to the NRS048 regulations, the variation of the voltage at the low-voltage (LV) side must not exceed ±10% of the nominal voltage, which is 230 V_{RMS}. The extra-long MV line might cause the voltage to drop beyond these limits. If a voltage regulator is placed at the end of the MV line, a drop in the voltage can be compensated for.

It has been decided that this drop will be limited to -40% of the nominal. It is not practical to have a line so long that the voltage drop over it exceeds this value. This implies that the voltage at the last transformer that changes the MV to LV should be between +10% and -40% of the nominal. The voltage regulator's location is another important consideration. One option considered in [4] is to position the regulator at the transformer. Two other options were to place it at the distribution boxes or at each customer's connection box. Each option has its own advantages and disadvantages.

There are three main categories of transformer sizes studied in [4]. They are a three-phase to three-phase transformer with ratings of 50 to 100 kVA, shown in Figure 2-1 (a). This is usually a four-wire system. The other two types can be three-phase, phase-to-phase or Single Wire Earth Return (SWER) on the primary side of the transformer. The transformer rated at 32 kVA is usually a two-phase secondary, shown in Figure 2-1 (b), and the transformer rated at

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16 kVA usually has a single-phase or SWER secondary, shown in Figure 2-1 (c).
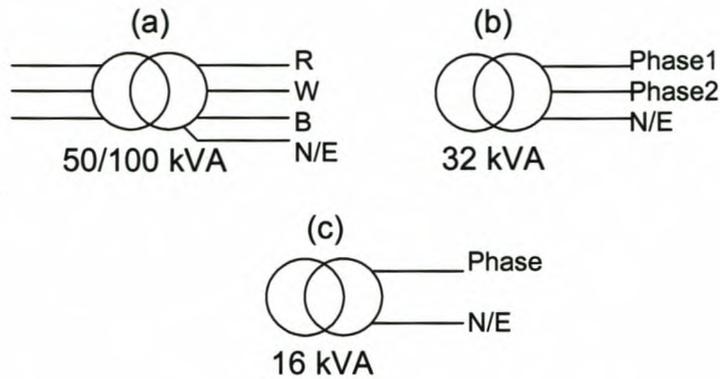
Figure 2-1: Transformers

Since the voltage regulator will be used with a long MV line connected to small loads, the two smaller transformers will be considered as the primary can be three-phase, phase-to-phase or SWER. With large three-phase motors the larger transformer will be used, but this is a special case and will not be considered in this project. With the 32 kVA and the 16 kVA transformers small single-phase motors can be used.

The problem now is what type of load can be expected to be connected to the transformer and voltage regulator. This has been investigated in [4]. Table 9 in [4] gives a summary of the more important aspects and that table is reproduced here in Table 2-2.

Densities [connections/km^2]	<200
Customer circuit-breaker [A]	2.5 or 20
After-Diversity Maximum Demand (ADMD) [kVA]	0.2-0.4
Transformer LV no-load voltage [V]	240 or 415
Transformer sizes [kVA]	16 or 32
Number of customers/service connection box	1.4-1.8

Table 2-2: Load specifications (from [4])

The After-Diversity Maximum Demand (ADMD) reflects the highest average load which a group of consumers can muster over a period in time.

The next problem to consider is the type of regulator to be used. Again there are a multitude of voltage regulators to choose from. Figure 2-2 summarises the problem thus far.
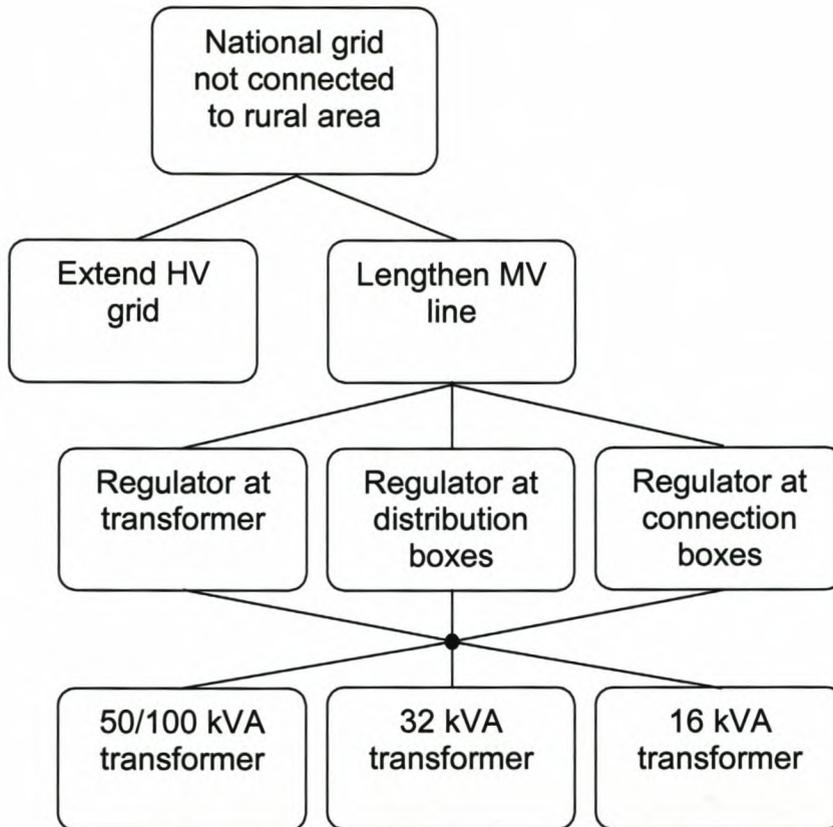
Figure 2-2: Summary of the problem position

2.2 Existing solutions

Figure 2-2 puts the situation into perspective and indicates the types of regulators that can be investigated. The more traditional types of regulators are transformers with tap-changers. This is a mechanical system where the transformer has several taps on its secondary side, each with its own voltage rating. A control system would decide which tap should be used. This system is slow and not very accurate. The mechanical tap switches have lately been

exchanged with electronic switches, which are faster but still not all that accurate since the basic idea remains the same. Figure 2-3 is a general diagram of the tap-changer. More detail on the existing system will be given later.
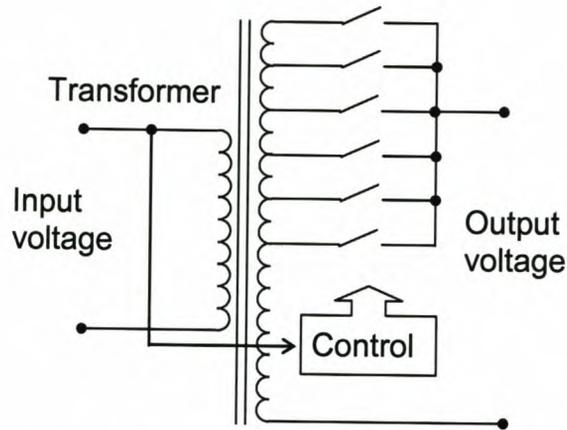
Figure 2-3: Tap-changing transformer

The next type of regulator is based on power electronic converters. Again a wide variety of converters exist, each with its own application. The more commonly used converter for voltage regulators consists of two power electronic converters. Initially it converts the AC voltage to a DC voltage and then converts the DC voltage to the desired AC value, shown in Figure 2-4. The rating of each of the converters is equal the maximum load rating. This means the power is converted twice and the total converter rating will be twice load rating, about 32 kVA for a 16 kVA load.
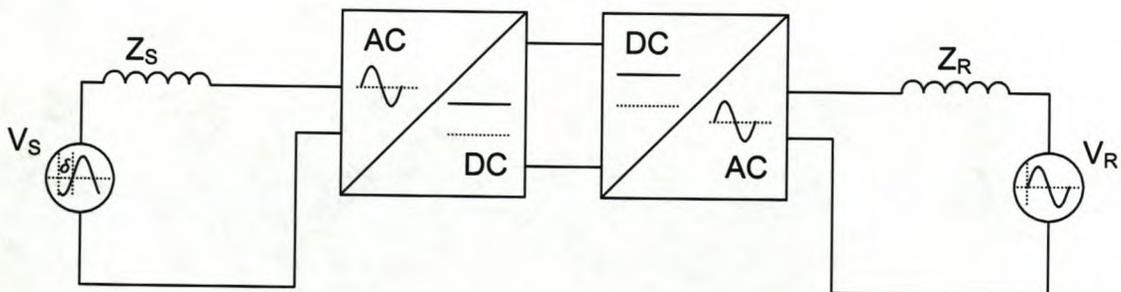
Figure 2-4: Voltage regulator based on back-to-back DC-to-AC converters

Another type of converter is the AC-to-AC converters. The AC input power is directly converted to the required AC output as shown in Figure 2-5. These have smaller ratings but pose their own problems. This topology will be discussed in the rest of this thesis.
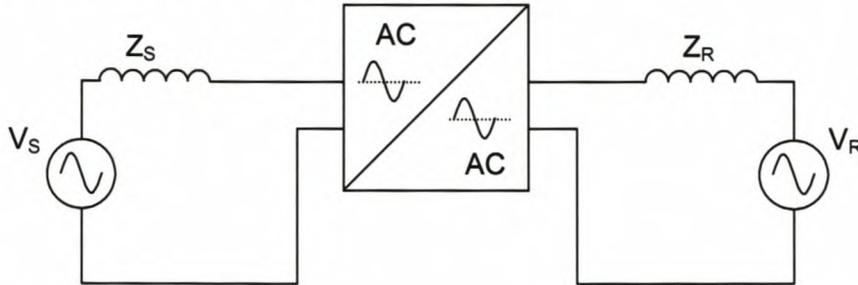
Figure 2-5: AC-to-AC converter block diagram

In section 2.1 different types of voltage regulators were mentioned. The type that has been in use the longest is the tap-changing transformer. With time and advances in technology the tap-changing transformer has evolved, but its basic operation remained the same. The rest of the section will be divided into two: first a broad explanation of how the tap-changer operates and then some changes that have occurred over time and in its use.

2.2.1 The operation of a tap-changing transformer

To help with the explanation Figure 2-3 is redrawn here with some differences.
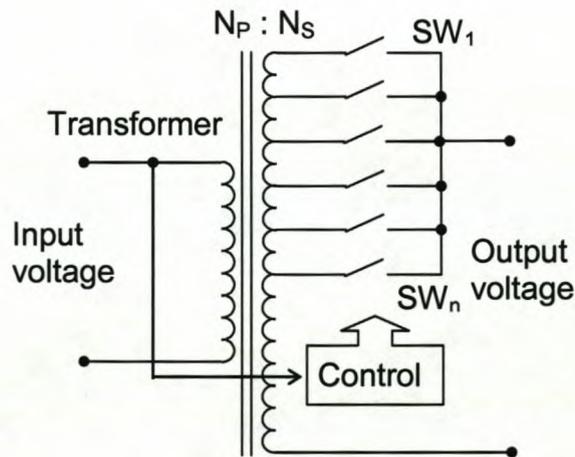
Figure 2-6: Tap-changing transformer

The idea behind a tap-changer is simple. It consists of a transformer and depending on the application it can be a step-up or step-down transformer. The secondary side of the transformer has a number of taps and again depending on where it will be used and the rating of the transformer, the number of taps as well as the percentage step (or drop) they represent will differ.

For current purposes the transformer is assumed to be a step-up transformer with n taps or switches as shown in Figure 2-6. If the input voltage is at nominal, then the switch that will make the turns-ratio of the transformer 1 (SW_{n-r}) will be closed and the output voltage will be at nominal value. If the input voltage were to decrease below nominal, the control will detect the change and switch the correct sequence of switches to reduce the transformer's turns-ratio. The turns-ratio is defined as N_P/N_S. The control can either be a feed-forward or feed-back system. Figure 2-6 has it as a feed-forward system.

There are other considerations in the control. It can be an older electromechanical system or an analog or digital system. They have a few basic functions or settings [18]. The most obvious is the setting of the voltage level; this is where the nominal voltage is set. The voltage bandwidth setting is where the controller is set to detect the allowable voltage difference; in South Africa it is ±10% of the nominal in the LV distribution network. Another integral part of the control of a tap-changer is the time delay. This setting is to ensure that the system is not too sensitive; for example, if a motor, as the load, was to start up it can, for a short period, decrease the voltage level due to its demand of up to six times the rated current. It is not practical for the control to react to such a change, since it will not last long and it will have to change back to the original setting. Figure 2-7 illustrates this; this figure and Figure 2-8 have been adapted from [18].
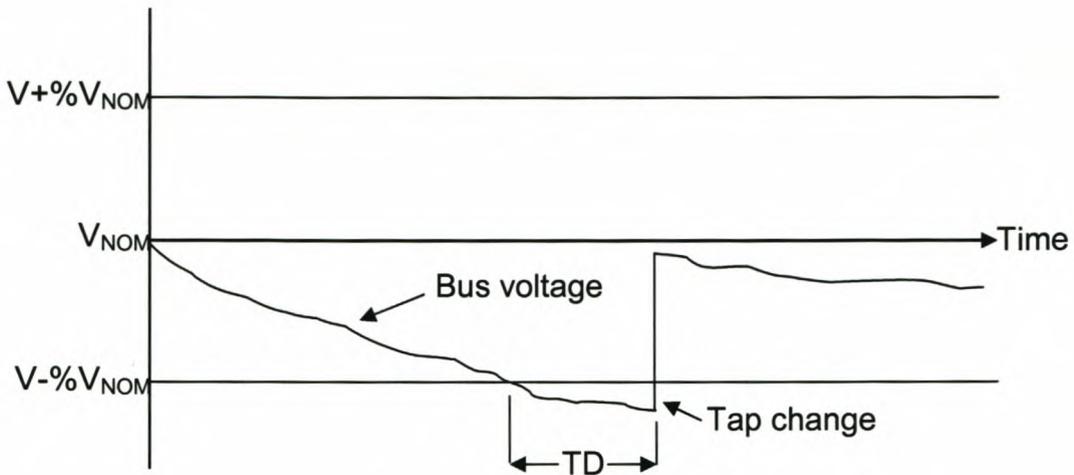
Figure 2-7: The three basic tap-changer settings

Anther problem to compensate for is the line drop from the regulator to the load. The impedance of the line is composed of two parts: the resistive and the reactive parts. This means that the voltage drop of the line from the regulator to the load consists of the two parts and, once this voltage is known, it is easy to compensate for using phasors. If V_L is the load voltage, V_B the bus voltage and V_{LD} the line voltage drop, then the compensation process is as illustrated in Figure 2-8 [18].
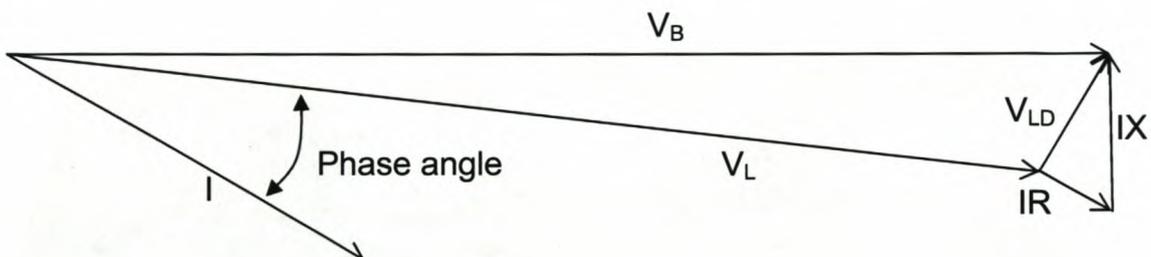
Figure 2-8: Phasor diagram of line-drop compensation

As mentioned above, the modern tap-changing transformers have electronic switches and digital controls. The most popular switch used is two back-to-back thyristors as shown in Figure 2-9.

BS
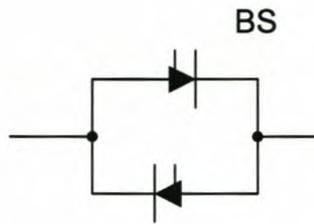
Figure 2-9: Bi-directional switch formed of two back-to-back thyristors

A reasonable response time is 1 cycle and the transformers are usually used with systems larger than 3 kVA [9]. This topology has its drawbacks. The first to be considered is that, if the user wants a high-resolution output, a large number of thyristors will be required. In a system with over 60 thyristors (±3% regulation with +10/-20% input range) the control for a fast response becomes rather complex. With motor loads this topology is susceptible to high transient current upon tap-changing and has trouble with transient voltage rejection.

2.2.2 Variations on tap-changing transformers

As can be expected with technology in use for such a long time, there are variations on the ordinary topology and use of the tap-changing transformer. With advances in silicon devices and the development of the IGBT, the obvious next step would be to exchange the mechanical switches with IGBTs. This will increase the speed at which the switches can react. Another change to realise a fast on-load tap-changing regulator is to use an injection transformer or a compensation transformer as suggested in [17]. The concept is illustrated in Figure 2-10.
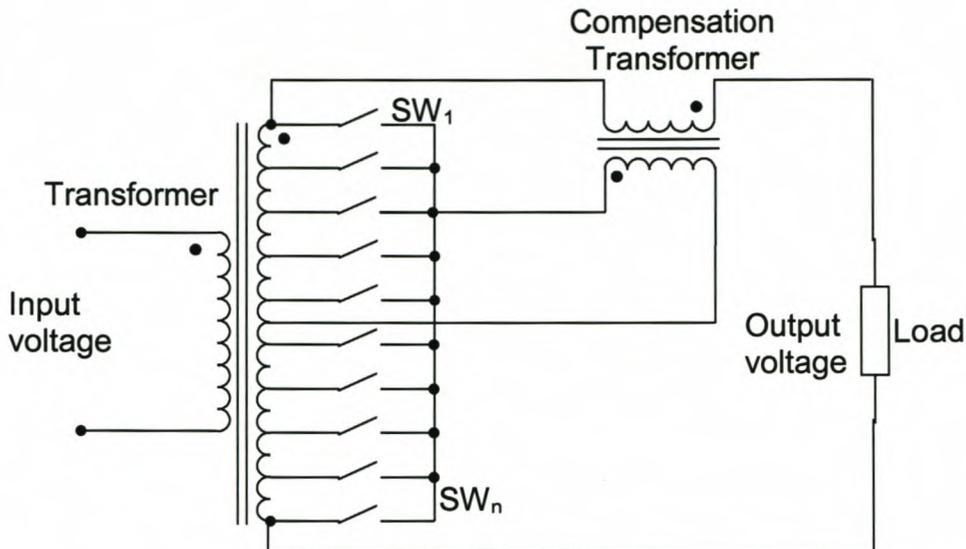
Figure 2-10: Tap-changer with compensation transformer on secondary side

The total secondary of the main transformer is connected to the load. The compensation transformer then injects the necessary voltage in series with the load. The compensation transformer obtains its primary voltage from the taps of the main transformer. This voltage can be in phase with the total secondary voltage of the main transformer, in which case it is added to the bus voltage, or it can be out of phase with it, in which case it is subtracted from the bus voltage. The response of this topology is good, in the order of a few micro-seconds if solid-state switching is used.

Another topology is Saturable Reactor Regulators [9]. Figure 2-11 shows the regulator.
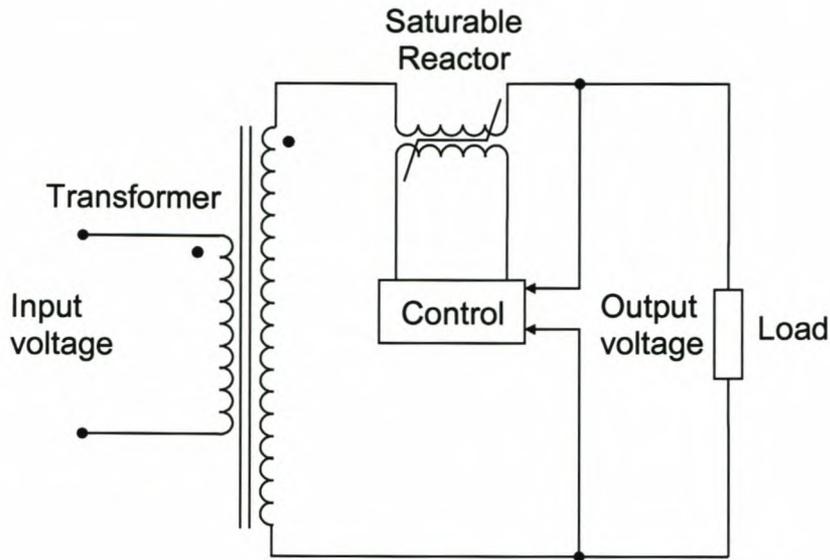
Figure 2-11: Saturable reactor regulator

The output voltage is controlled by varying the impedance of the saturable reactor. This topology has a simple concept and has a good line transient rejection, but it has a slow response time of about 10 cycles [9]. High output impedance leads to distortion with non-linear loads; it is sensitive to the load power factor, cannot handle surge currents and it cannot suppress transients from inside the plant.

Motorised variacs, as shown in Figure 2-12, are also a well-known regulator topology. They can inject or subtract voltage to the bus via the compensation transformer. This topology can handle large surge currents [9] but, as expected, the response is slow and is thus not acceptable for sensitive loads. With an increase in moving parts the maintenance requirements will also increase and, since the variac has a lot of moving parts, the maintenance on this device is substantial. Because of the slow reaction this topology also has problems with transient suppression.
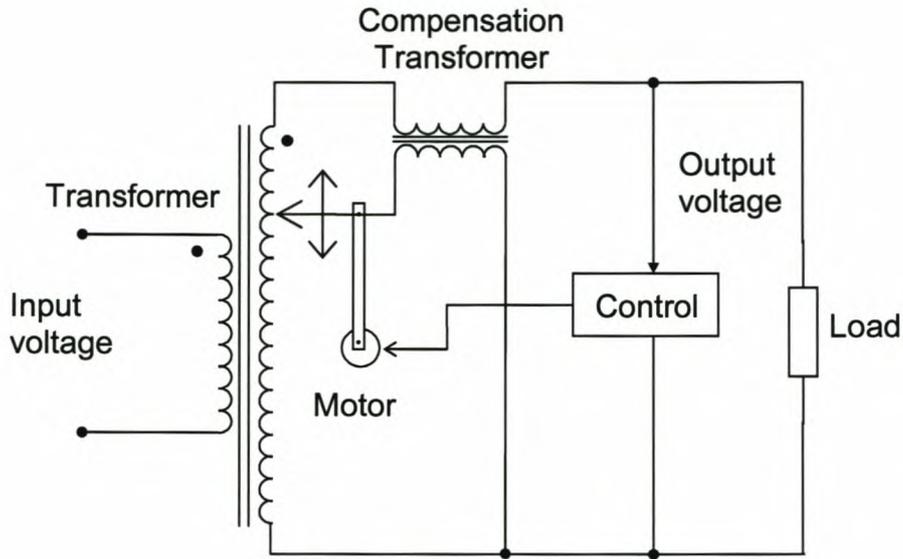
Figure 2-12: Motorised variac

Despite the drawbacks of this topology, it is applied with good results under the correct conditions. There are a number of manufacturers that produce this device; one of the providers of this device is ESP (Electronic Specialists, Inc.). The device may be configured for two situations: one is where the maximum output voltage is equal to the applied voltage and the other configuration is where the maximum output voltage is approximately 15% above the input voltage [32]. Table 2-3 and Table 2-4 show some of the models available.

Model	Output Voltage (V)	Output Current (A)	Price (2002) (U.S. $)
SVRSD-360	0-120/132	3.0	1 015
SVRSD-600X	0-120/140	5.0	1 143
SVRSD-1200	0-120/140	10.0	1 470
SVRSD-1440 (60 Hz only)	0-120/140	12.0	1 489
SVRSD-1800	0-120/140	15.0	1 636
SVRSD-3000	0-120/140	25.0	1 812

Table 2-3: 120 V Models @ 50/60 Hz

Model	Output Voltage (V)	Output Current (A)	Price 2002 (U.S. $)
SVRSD-840/240	0-240/275	3.5	1 546
SVRSD-1200/240 (60 Hz only	0-240/275	5.0	1 563
SVRSD-2280/240	0-240/275	9.5	1 659
SVRSD-2400/240	0-240/275	10	1 828

Table 2-4: 240 V Models @ 50/60 Hz

The devices listed above have low output current ratings, which limits their use.

Another topology using a compensation transformer is described in [7]. Figure 2-13 illustrates the differences. This topology is used as a dip compensator or power conditioner. Its response time is a quarter of a cycle.
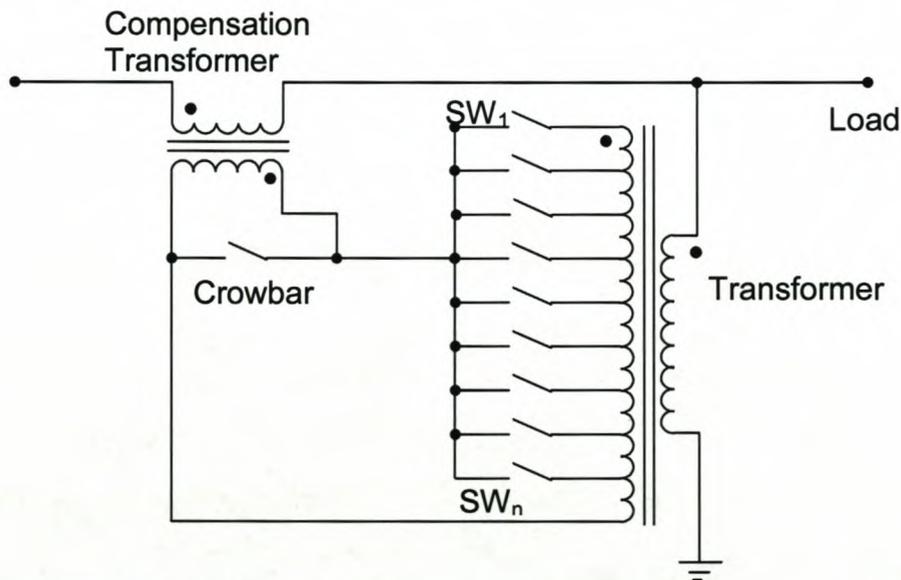
Figure 2-13: Tap-changer with compensation transformer on primary side

With the transformers above, the taps were all on the secondary side but that is not always the case, as can be seen in [10], [11] and [12].
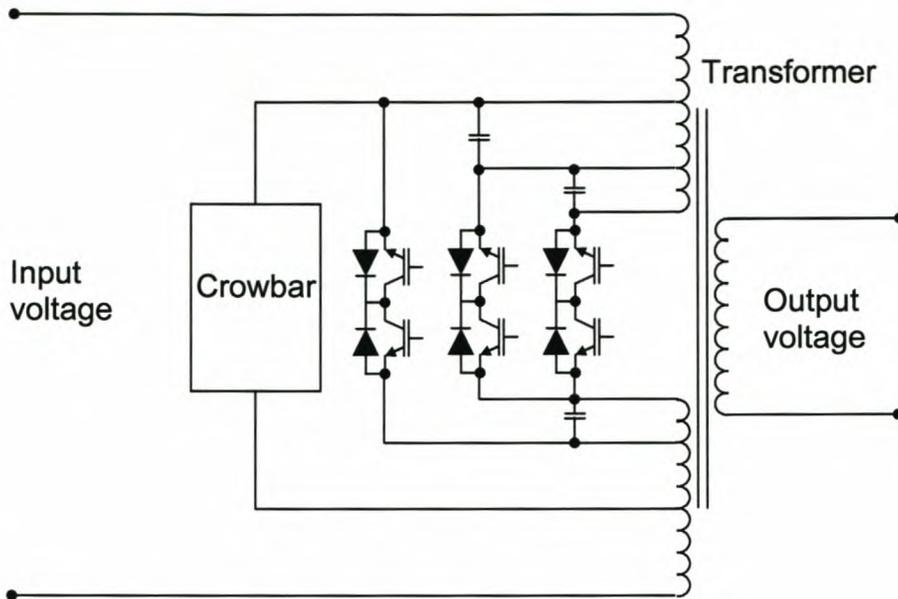
Figure 2-14: Primary tapped transformer

Figure 2-14 is a circuit diagram of the topology proposed in [10], [11] and [12]. The three pairs of IGBTs form three bi-directional switches. The amount of turns on the primary depends on which of the switches are conducting. This will change the secondary voltage to the desired level.

A Constant Voltage Transformer (CVT) or Ferroresonant Transformer is the next type of regulator to be considered. These transformers operate in their saturation region and this means that the output voltage is not sinusoidal but a square wave [9], [26]. This topology operates best with a constant or linear load; this in turn leads to sensitivity to circuit capacitance and frequency deviations. If the input voltage falls below its minimum, the output voltage will collapse to zero. The CVT must be oversized for the load to operate efficiently, because the collapse of the output voltage can also occur during overload conditions such as a motor starting and high inrush current. The benefit of this topology is that it has good line transient suppression but, like the saturable reactor, it cannot handle transients from the plant. Figure 2-15 show a typical feroresonant circuit.
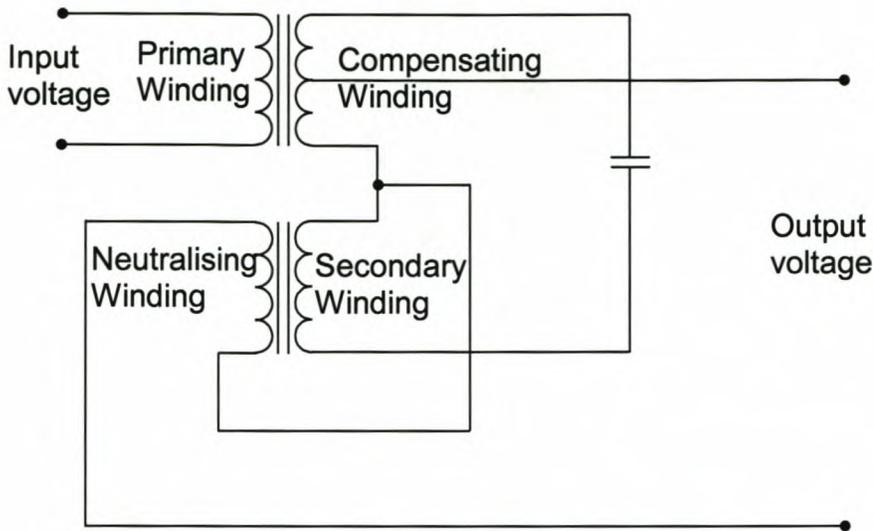
Figure 2-15: Ferroresonant transformer

As mentioned above, there are manufacturers that build and distribute some of these devices and the ferroresonant transformer is no exception. Electronic Specialists, Inc. [32] have a wide variety of models available. They market three voltage input groups: the 120 V, 240 V and the 120/240 2-phase V input. Each of the input groups can then be divided into 3 output voltage groups. Table 2-5, Table 2-6 and Table 2-7 summarise the groups with their input and output voltages as well as their power range, current range and price range. In total there are 81 models listed on their internet site [32].

Input Voltage (V)	Output Voltage (V)	Power range (W)	Current range (A)	Price range (U.S. $)
120 +15% / -25%	115 ±4%	125 – 3600	1 – 30	355 – 1 950
120 +15% / -25%	230 ±4%	125 – 3600	0.5 – 15	355 – 1 950
120 +15% / -25%	115/230 ±4% (2-phase)	125 – 3600	0.5 – 15	355 – 1 950

Table 2-5: 120 V Input @ 60/50 Hz

Input Voltage (V)	Output Voltage (V)	Power range (W)	Current range (A)	Price range (U.S. $)
240 +15% / -25%	115 ±4%	125 – 3600	1 – 30	355 – 1 950
240 +15% / -25%	230 ±4%	125 – 3600	0.5 – 15	355 – 1 950
240 +15% / -25%	115/230 ±4% (2-phase)	125 – 3600	0.5 – 15	355 – 1 950

Table 2-6: 240 V Input @ 60/50 Hz

Input Voltage (V)	Output Voltage (V)	Power range (W)	Current range (A)	Price range (U.S. $)
120/240 +15% /-25% (2-phase)	115 ±4%	125 – 3600	1 – 30	355 – 1 950
120/240 +15% /-25% (2-phase)	230 ±4%	125 – 3600	0.5 – 15	355 – 1 950
120/240 +15% /-25% (2-phase)	115/230 ±4% (2-phase)	125 – 3600	0.5 – 15	355 – 1 950

Table 2-7: 120/240 V 2-Phase Input @ 60/50 Hz

The phase controlled regulators have difficulty in handling the transients from inside the plant [9]. As with the previous regulator, they can handle line transients as well. This type uses phase-controlled thyristors with a LC filter, but they have a lot of drawbacks. First of all they have a slow response, increased distortion with non-linear loads, large filters, poor input line harmonics and cannot handle surge currents. Figure 2-16 shows the converter.
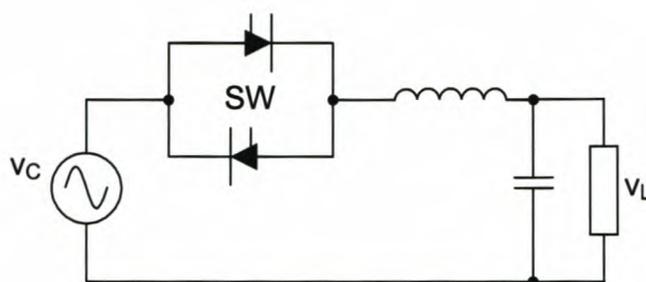
Figure 2-16: Phase-controlled converter

These are but a few of the different types of topologies for the tap-changing transformer used as a voltage regulator and conditioner. In the following section the converter-based technologies will be discussed.

2.3 Converter-based solutions

Another important class of voltage regulator is the converter-based devices. As in the case of the tap-changer, converter-based technology is a rapidly developing field and the variations on the ordinary converter are immense. In this section the AC-to-DC and DC-to-AC converters will be discussed [5]. The main advantages of these devices are:

- Fast response time;
- Unlike the tap-changer devices, they can regulate the voltage to an exact predefined value;
- They can compensate for a number of other power-quality problems as well.

One method, as mentioned in section 2.1, to regulate voltage is to convert the voltage and current. This conversion is done by using two DC-to-AC converters placed back-to-back. This indicates that the power is first converted from AC to DC using one type of converter. Whether it is a diode-rectifier or a switch-mode converter depends on the use of the rectifier. The next item that makes up the regulator is a large bus capacitor. The last stage of the regulator is a switch-mode converter. This converter converts the power from DC to AC and with its control can usually change the amplitude and

frequency of the voltage and/or current. Figure 2-17 (a) and Figure 2-17 (b) are basic block diagrams of the set of components that form the regulator.

(a)

(b)
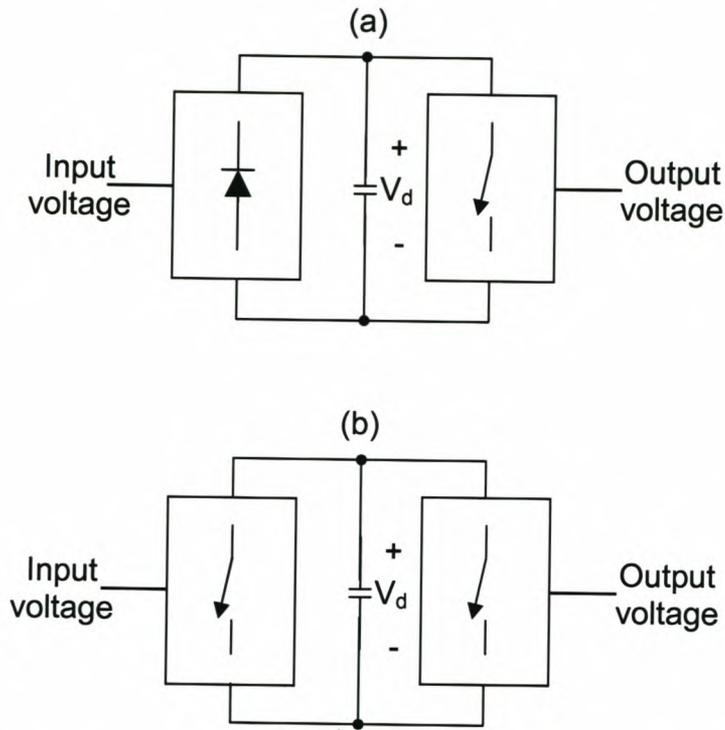
Figure 2-17: (a) Voltage regulator with diode-bridge; (b) Voltage regulator with two switch-mode converters

The regulator can be placed in series with the line as shown in Figure 2-18, but this type of connection leads to an overpriced system because of the appropriate overload capability that is needed. The main drawback, though, is the fact that it is difficult to protect the converter. The cost can be reduced to an acceptable level if the converter is used in combination with a series transformer as shown in Figure 2-19.

Plant transformer
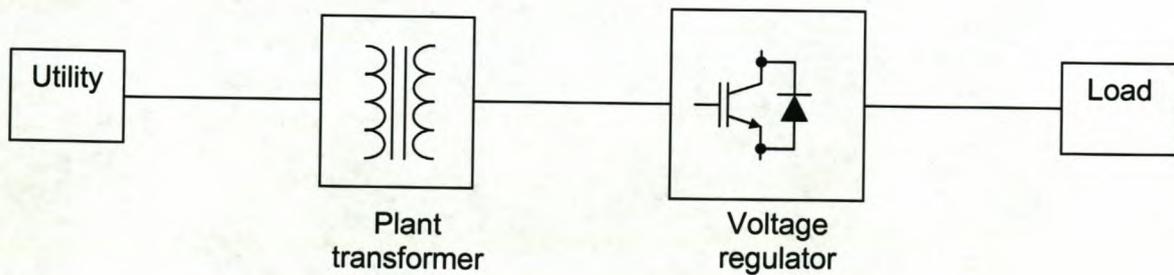
Voltage regulator

Figure 2-18: Voltage regulator in series
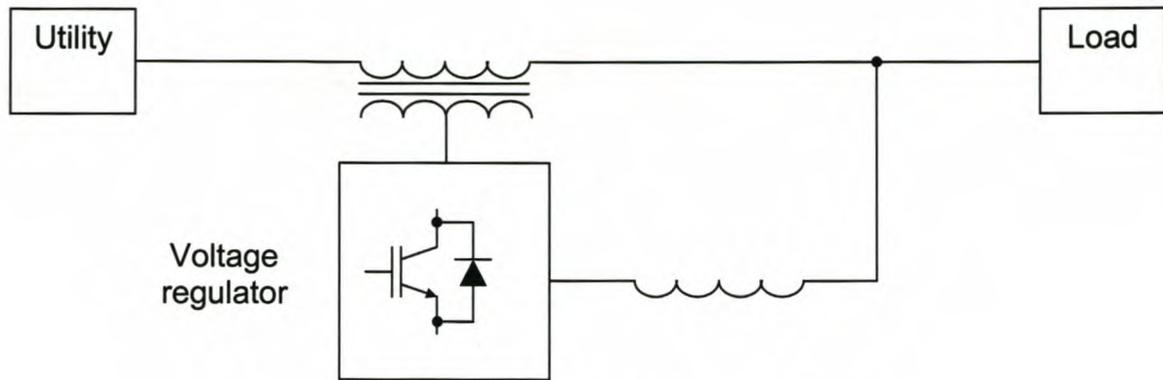
Figure 2-19: Voltage regulator with series transformer

2.3.1 AC-to-DC converter

In the previous section it was mentioned that the first block in the regulator is an AC-to-DC converter and that the converter can be a diode rectifier bridge or a switch-mode converter. The necessity for two types of rectifiers lies in the other use of the regulator topology: as AC motor drives. A major disadvantage of the diode rectifier is the fact that it draws a highly distorted current. When the motor is running normally, the power flows from the input to the output, but when the motor brakes, the power flow is reversed. This is not a problem for the switch-mode converter, because its power flow is reversible, but since the motor is now acting as a generator, it is supplying power. This energy cannot be recovered and fed back to the grid and must be dissipated in a resistor parallel with the bus capacitor. This refers to Figure 2-17 (a) and is suitable should a lot of braking not be taking place.

Should the motor need to brake often, it would make more sense to have a system where the power can be returned to the grid. This is called regenerative braking and requires a two-quadrant converter. This implies that the voltage remains positive, but has a reversible DC current. The switch-mode converter for AC-to-DC will not be considered further in this thesis as it is not necessary for the use in a voltage regulator.

The diode-rectifier is a diode bridge connected between the supply and the DC-to-AC converter. Figure 2-20 is a block diagram of a single-phase diode bridge rectifier. This rectifier only makes the voltage positive and the filter capacitor filters out the DC component; there will be a small ripple on the voltage, but this depends largely on the size of the filter capacitor.
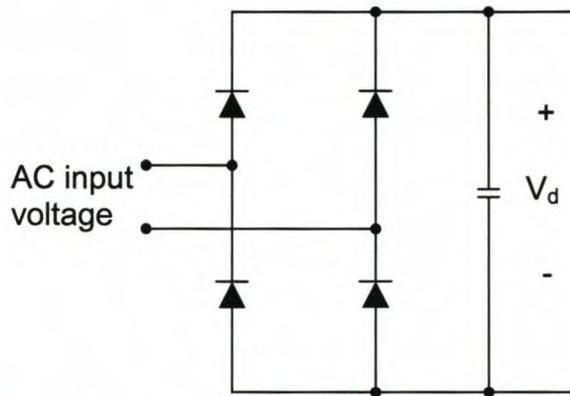
Figure 2-20: Single-phase diode bridge rectifier

2.3.2 DC-to-AC converter

The last part of these rectifiers is the switch-mode converters. In this case it is a DC-to-AC inverter, so named because of the direction of power flow and mode of operation. These inverters are powered by a DC voltage source and are thus called voltage source inverters. Current source inverters do exist, but are used for high-power AC motor drives and will not be discussed here.

For the rest of this section the PWM (pulse-width-modulated) inverter will be discussed. More detail can be found in various articles and books such as [5]. The basic requirements will have to be investigated to understand the inverter and how it operates. To achieve this, the inverter will be represented as a block diagram in Figure 2-21 (a).

The next aspect to consider is the type of load. It will almost never have a capacitive load and will most likely be inductive rather than resistive, because a motor of any type will be inductive. Inductive or capacitive loads are some of

the worst types of load a system might have, because the current now lags or leads the voltage at the output. This means that the current will flow in the opposite direction than the voltage and the inverter will have to perform like a rectifier. Figure 2-21 (b) shows the output current and voltage for an inductive load. In this figure it can be seen that there are 4 sections/quadrants in which the inverter will have to work. Sections 1 and 3 are the quadrants in which the inverter acts as an inverter because the sign of the voltage and current are the same. In the remaining sections (2 and 4) the voltage and current have opposite signs and this means the inverter is in rectifier mode and a good graphical representation of the problems occurred with an inductive load. Figure 2-21 (c) represents the four quadrants in which the inverter must operate.
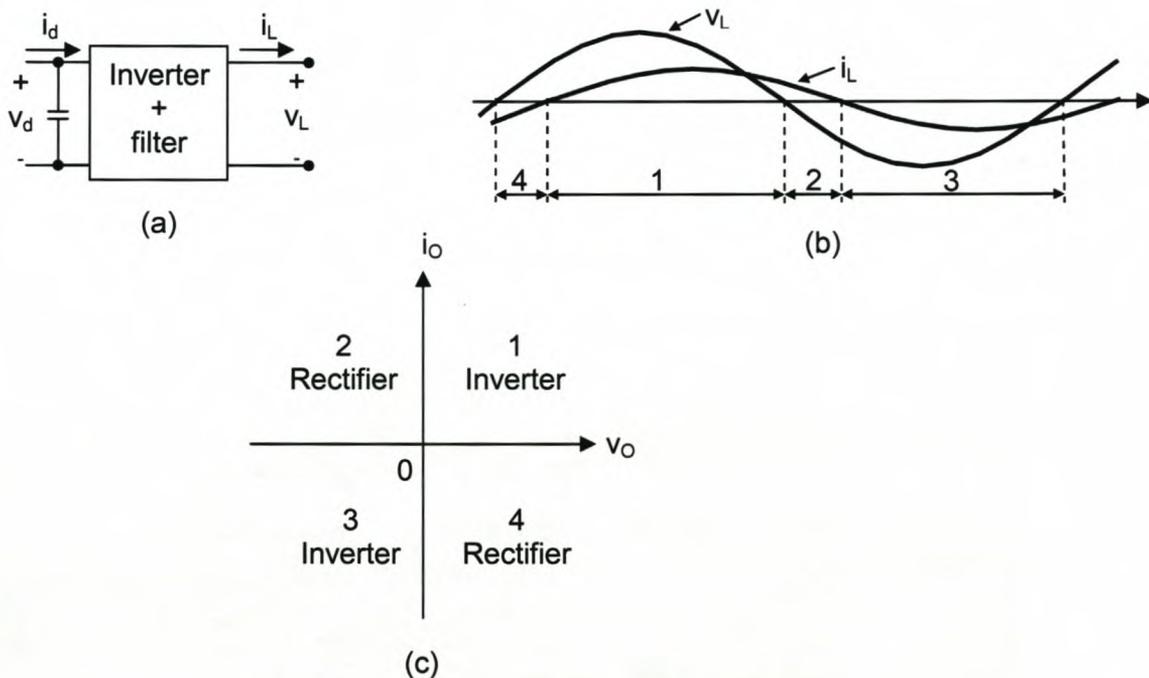
Figure 2-21: Quadrants of switch-mode inverter

The details of how PWM inverters operate can be found in [5] and many existing books on the topic.

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2.4 Summary

In this chapter the need for voltage regulation was discussed. The exact problem that needs to be addressed and where the solutions should be applied were outlined. This included the type of transformer used and how the load will be fed, whether it is SWER, phase-to-phase or three-phase systems. The research field was narrowed and the attention focused on one type and size of transformer. This was the 16 kVA SWER system.

Different methods of voltage regulation were discussed. In section 2.2 the well-known tap-changing transformer was highlighted. In this section the more modern adaptations and uses were discussed. The use of high-speed switches such as IGBTs were mentioned as well as the different types of topologies from switching at the primary side of a step-down transformer ([10], [11], [12]) to using the concept to add or subtract the right amount of voltage [7].

The last section was devoted to the converter topologies. This was two AC-to-DC converters placed back-to-back, the first to convert the voltage from AC-to-DC and the second to convert it from DC to the correct AC voltage.

Topology	Response time	Surge capability	Power-quality problems	Cost
Ordinary tap-changer	Depending on type of switch: - thyristor ~ 1 cycle	Mechanical ~ heavy surge currents Thyristor ~ device rating will limit the surge current	Sags and brownouts	Depend on number and type of switch: - up to 60 thyristors with large ratings for surge ~ costly
Tap-changer with compensation transformer on secondary side	Switches IGBTs ~ good, within a few milliseconds	IGBTs ~ device rating will limit the surge current	Sags and brownouts	One extra transformer but fewer switches: - less costly
Saturable reactor regulator	Slow ~ 10 cycles	Cannot handle large surge current like a motor starting	Sags and brownouts	Moderately priced
Motorised variac	Slow ~ 30 V/sec	Heavy surge currents	Sags and brownouts	1 015 – 1 828 U.S. $ [32]
Tap-changer	Quarter of a	Crowbar ~	Sags and	Crowbar ratings

with compensation transformer on primary side	cycle	device rating will limit the surge current, crowbar designed for large currents	brownouts	large with at least 14 thyristors ~ costly
Primary tapped transformer	Secondary voltage feedback method ~ slow response	Crowbar ~ device rating will limit the surge current, crowbar designed for large currents	Sags and brownouts	Crowbar ratings large with at least 6 IGBTs or thyristors ~ costly
Ferroresonant Transformer	Fast	Cannot handle large surge current like a motor starting or large inrush current	Sags and brownouts	355 – 1 950 U.S. $
Phase-controlled regulators	Slow	Cannot handle large surge current like a motor starting or large inrush current	Sags and brownouts	Over-sized filters - costly
Converter-based devices	1-2 milliseconds	Designed for large surge currents.	Sags, brownouts, harmonic compensation, phase correction, frequency regulation, power factor	In series – unacceptably high With series transformer – cost of more conventional regulators

Table 2-8: Summary of regulators

Table 2-8 is a summary of the regulator topologies that were discussed in this chapter. It compares the response time, surge-handling capabilities, the power-quality problems that are compensated for and the approximate cost of the system. From Table 2-8 it can be seen that a converter topology can offer the highest performance solution, but that an AC-to-DC – DC-to-AC converter system is also the most costly of the topologies. The power will also be converted twice in this system and that will increase the rating of the converters.

Another aspect to remember is that an IGBT can only handle twice the rated current where a thyristor can handle up to ten times the rated current. A mechanical switch can handle even more time the rated current than the

thyristor. This implies that if IGBTs are used, it must be rated for the over-current when a motor switches on.

In the next chapter AC-to-AC converters will be discussed. This type of converter converts the power only once and their cost is also lower, because no large DC-capacitors are needed. Again different types of converters will be discussed and the best solution for the problem will be found.

Chapter 3

Single-phase AC-to-AC converter topologies

3 Single-phase AC-to-AC converter topologies

In the previous chapter different types of voltage regulators were discussed, from the tap-changing transformer to the DC-to-AC converters. AC-to-AC converters will be introduced in this chapter.

AC-to-AC converters are not a new type of converter and have been researched for a number of years. In [19] the authors proposed an AC-to-AC converter with an injection transformer as shown in Figure 3-1.
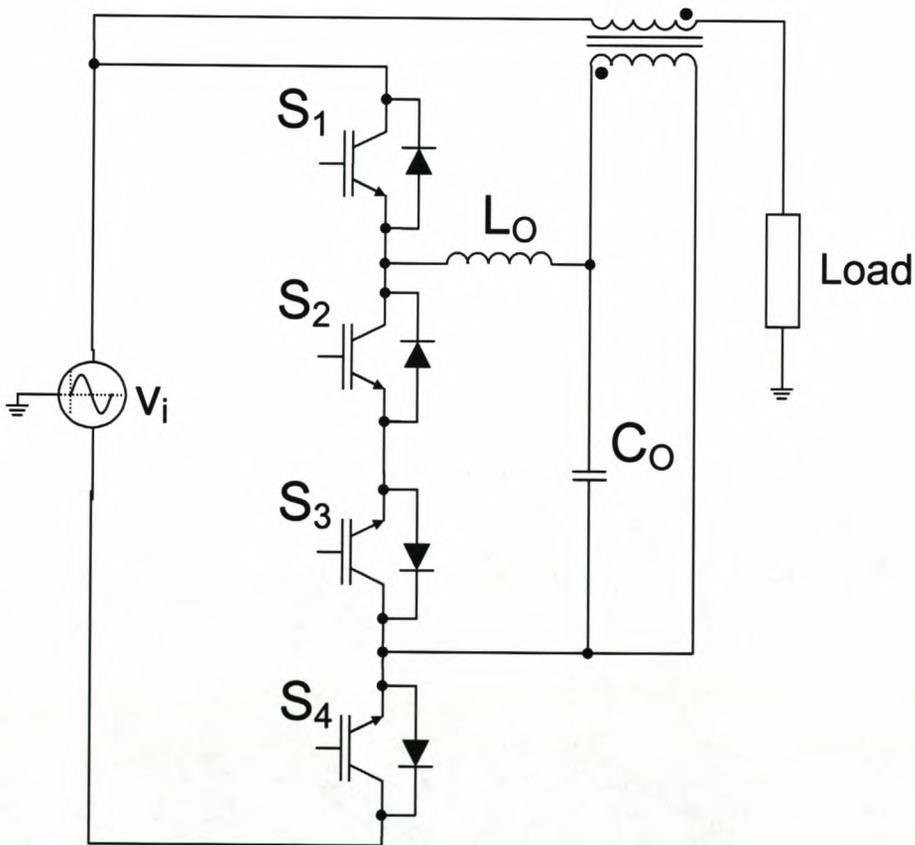
Figure 3-1: Single-phase AC-to-AC converter with injection transformer

This topology was developed for the regulation of an input voltage with sags. The converter is based on a buck converter and using IGBTs with PWM

control will produce a fast response time. In combination with a tap-changing transformer this single-phase converter can be extended into a three-phase converter. The control and operation will be discussed later.

The injection transformer is not always required and the converter can be adapted as shown in Figure 3-2 from [23]. The voltage regulator in Figure 3-1 has the advantage of smaller ratings, but this topology has a simpler design. With these topologies the output filter is small and there is no need for large DC bus capacitors. This will reduce the overall cost. The ratings of the switches must be sufficient that they can handle the required surge currents, but the protection of the switches in fault stages must be carefully evaluated. All these aspects will be discussed in detail later.
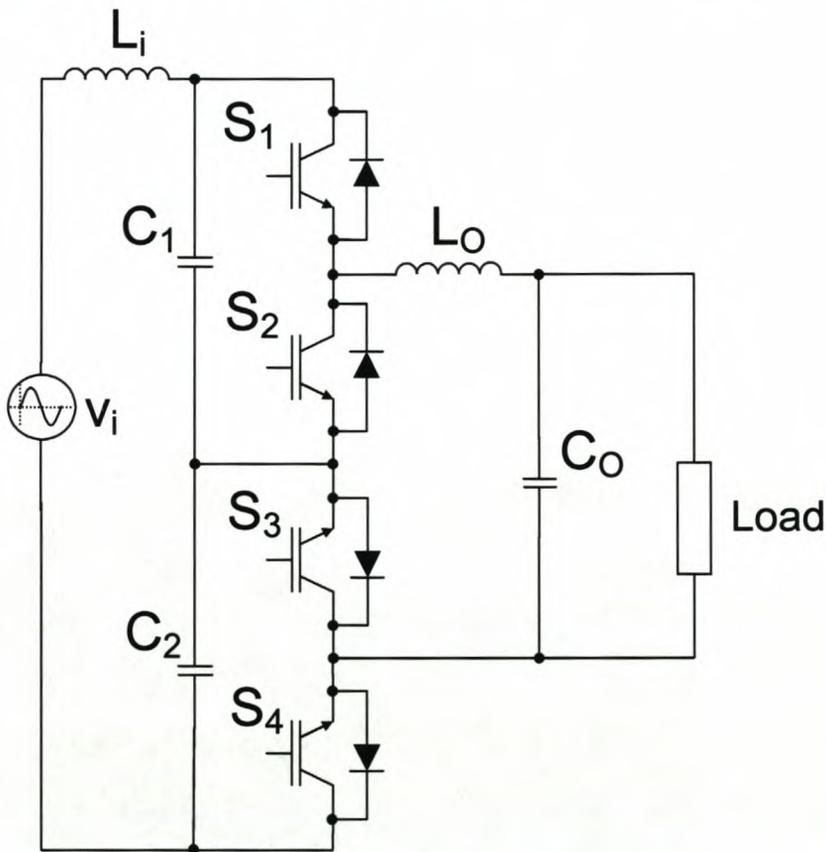
Figure 3-2: AC-to-AC converter without injection transformer

If only the sag correction is taken into account there is yet another topology that can be considered. This topology is close to the first two mentioned and is shown is Figure 3-3 taken from [25].
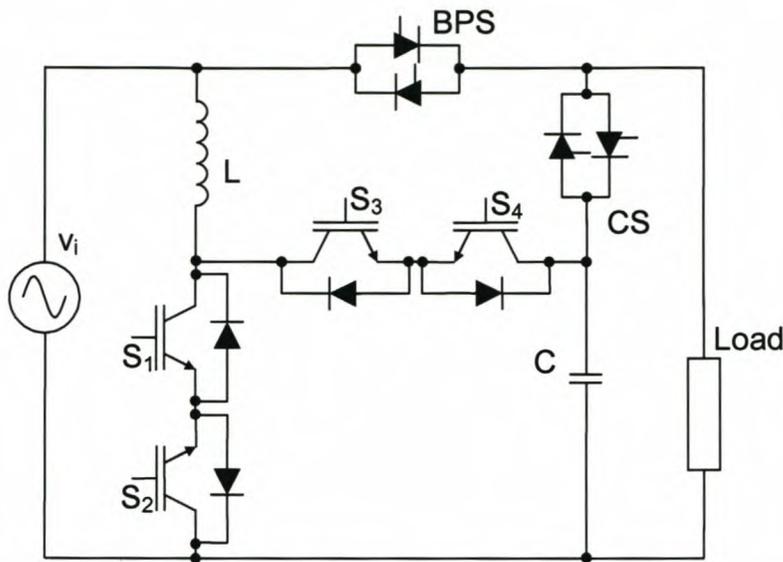
Figure 3-3: Single-phase sag compensator

The operation of this compensator is straightforward. When the input voltage is nominal the bypass switch (BPS) conducts. This switch is made up of two back-to-back thyristors and forms a bi-directional switch. Should a sag occur the connection switch (CS) will conduct and the BPS will block the current. During this stage the converter is in operation. The converter is constructed using the input inductor L, the output capacitor C and four switches. These switches are positioned in such a way that they produce two bi-directional switches that in turn are placed back-to-back. Switches 1 and 2 (S1 and S2) construct one of these bi-directional switches and switches 3 and 4 (S3 and S4) construct the other one. This type of converter will be discussed further later but [15] also describes the switches.

Another topology to be considered is described in [23] and [24] and was patented under [22]. Figure 3-4 shows the AC copper that is based on the standard commutation cell. A combination of these cells can present the user with a multilevel converter or even a three-phase converter, depending on the desired use.
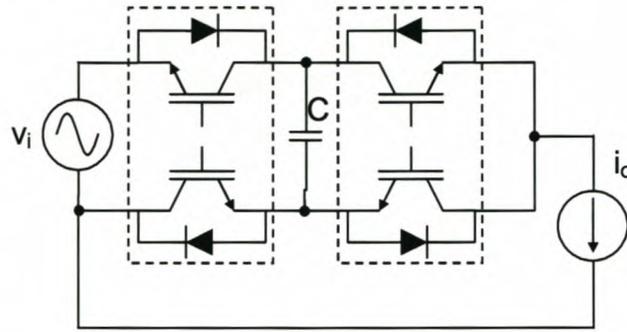
Figure 3-4: AC chopper

One of the types of AC-to-AC converters that ought to be mentioned is the matrix converter. This type of converter has been under investigation from the early 1980s and is still under development and growth as the technology involving the switches and their controls develops. In [29] the basic design of the matrix converter is discussed. It is a three-phase system and consists of 9 bi-directional-switches, three for each phase as shown in Figure 3-5.
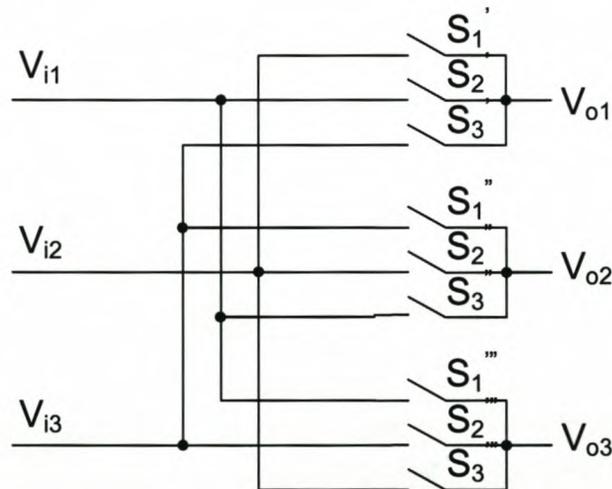
Figure 3-5: Three-phase matrix converter

Over the past few years many papers have been written on matrix converters and their adaptations; [8], [14], [20], [21], [27] and [30] are but a sample of these papers. Since this is such a wide topic on its own, the matrix converter will not be examined any further in this thesis.

It will be shown in later chapters that the AC-to-AC converters offer the user advantages in their switching losses and the harmonic content of the converters' output signal. A comparison with the DC-to-AC converter in this respect will also be made. As mentioned in [29], the single-phase AC-to-AC converter has some disadvantages when it comes to frequency and phase. In this case the output voltage has to have the same frequency and phase as that of the input voltage. This means that the power-quality applications of the converter are limited. These problems will also be examined more closely in later chapters.

3.1   The standard AC-to-AC converter cell
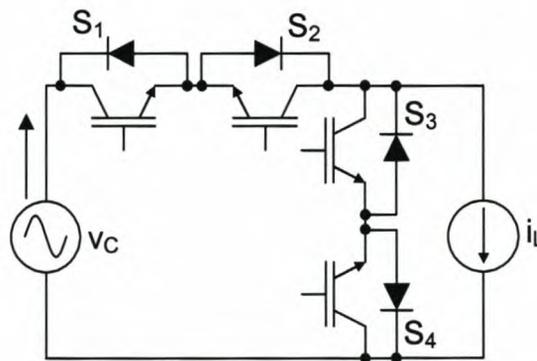
Figure 3-6: Standard AC-to-AC converter cell

Figure 3-6 is a standard AC-to-AC converter cell and the individual switches are named S_1, S_2, S_3 and S_4 with v_C as the supply voltage from the input filter capacitor. The load is represented as the current source i_L. Switches S_1 and S_2 form one bi-directional switch and S_3 and S_4 form the other bi-directional switch. One bi-directional switch can also be called a four-quadrant switch and are made up of two two-quadrant switches [15]. There are two types of two-quadrant switches, the voltage and the current two-quadrant switch. Figure 3-7 (a) represents the voltage two-quadrant switch and it is able to block voltage of both polarities and can conduct current in only one direction. This will be in quadrants 1 and 2 in Figure 3-8. Figure 3-7 (b) represents the current two-quadrant switch and this switch can conduct current in both

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directions, but can only block the voltage of the polarity of V_S. In Figure 3-8 this will be in quadrants 1 and 4. Figure 3-7 (c) and Figure 3-7 (d) show one way to implement the voltage two-quadrant switch and the current two-quadrant switch respectively.
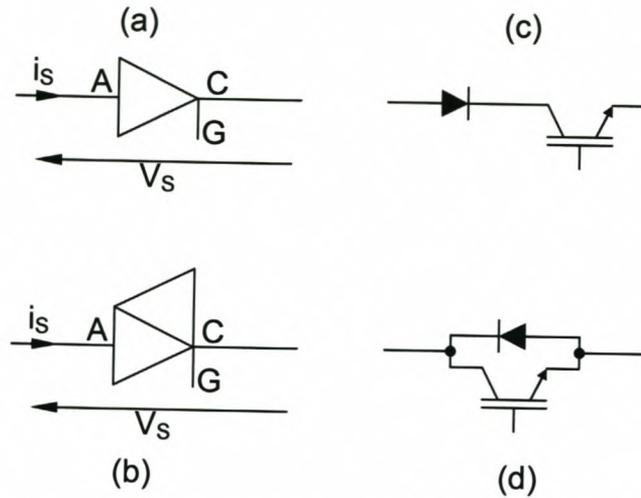
Figure 3-7: Two-quadrant switches (a) Voltage two-quadrant; (b) Current two-quadrant; (c) Implementation of voltage two-quadrant; (d) Implementation of current two-quadrant
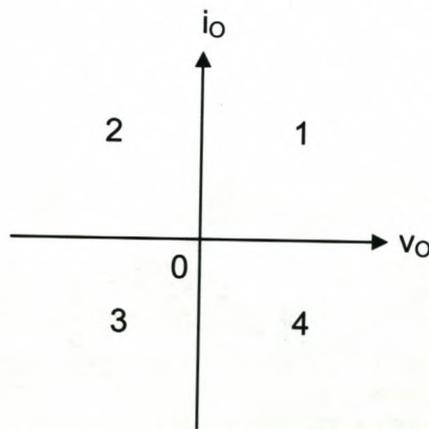
Figure 3-8: Graphic representation of quadrants

The four-quadrant switch now can be made up of voltage or current two-quadrant switches as shown in Figure 3-9.

(a) (b)
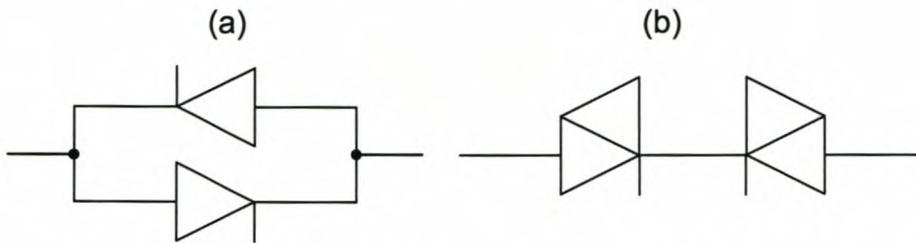
Figure 3-9: Four-quadrant switches constructed of (a) voltage two-quadrant switches; (b) current two-quadrant switches

Using the implementation as shown in Figure 3-7 (c) or (d), the bi-directional switch as shown in Figure 3-6 can be formed. The current path through the switch is shown in Figure 3-10 [10].
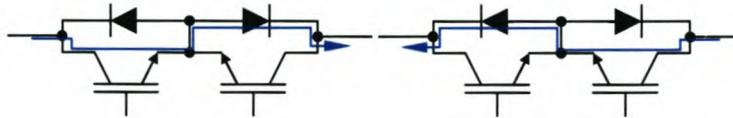
Figure 3-10: Current polarities of bi-directional switch

The control of these switches is critical and needs careful consideration. There are two basic conditions that must be adhered to:

- The voltage bus must never be short-circuited unless v_C is equal to 0 V;
- A path for the load current must always exist, unless i_L is equal to 0 A.

The only time in a cycle that this is possible is when the sinusoid goes through its zero crossing. To ensure that the conditions are met, the correct commutation strategy must be chosen. There are three different strategies or control methods:

- Sensing the capacitor voltage v_C;
- Sensing the inductor current i_L;
- A combination of the two mentioned above.

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3.1.1 Voltage detection control

In the event of voltage detection control, a sensor must be devised that is both accurate and fast. Referring to Figure 3-6, the exact switching scheme can now be discussed. With the voltage detection method the capacitor voltage (v_C) will be used to determine the sign of the voltage. During the positive half-cycle switches S_1 and S_3 will be switching and switches S_2 and S_4 will remain on. The converter is now an ordinary buck converter with the current flowing in the black components in Figure 3-11 (a) and (b) when i_L is positive with S_1 and S_4 on respectively.
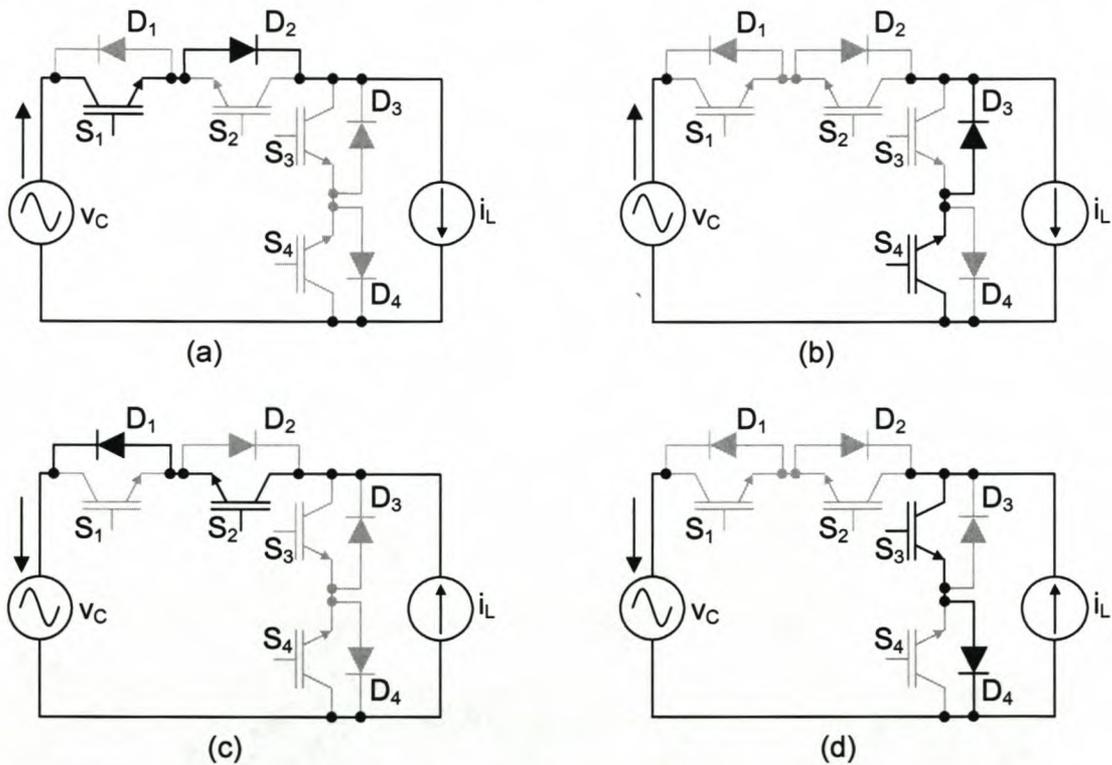
Figure 3-11: Standard AC-to-AC converter cell with voltage detection during (a) positive half-cycle, S_1 on; (b) positive half-cycle, S_4 on; (c) negative half-cycle, S_2 on; (d) negative half-cycle, S_3 on

During the negative half-cycle switches S_2 and S_4 are switching and S_1 and S_3 remain on. A short dead time is used where both switching switches are off. The converter is now the exact opposite to the one in the positive half-cycle and the current flows in the black components in Figure 3-11 (c) and (d) with S_2 and S_3 on respectively. The converter during the positive half-cycle is

symmetrical to the converter during the negative half-cycle. Figure 3-12 shows the theoretical capacitor voltage v_C, the unfiltered output voltage v_O, the inductor current i_L and the gating signals to the individual switches. Wrong detection of this voltage will lead to short-circuiting the bus. This is one of the conditions that must not be violated and will lead to an over-current in the switches. This may destroy the switching components.
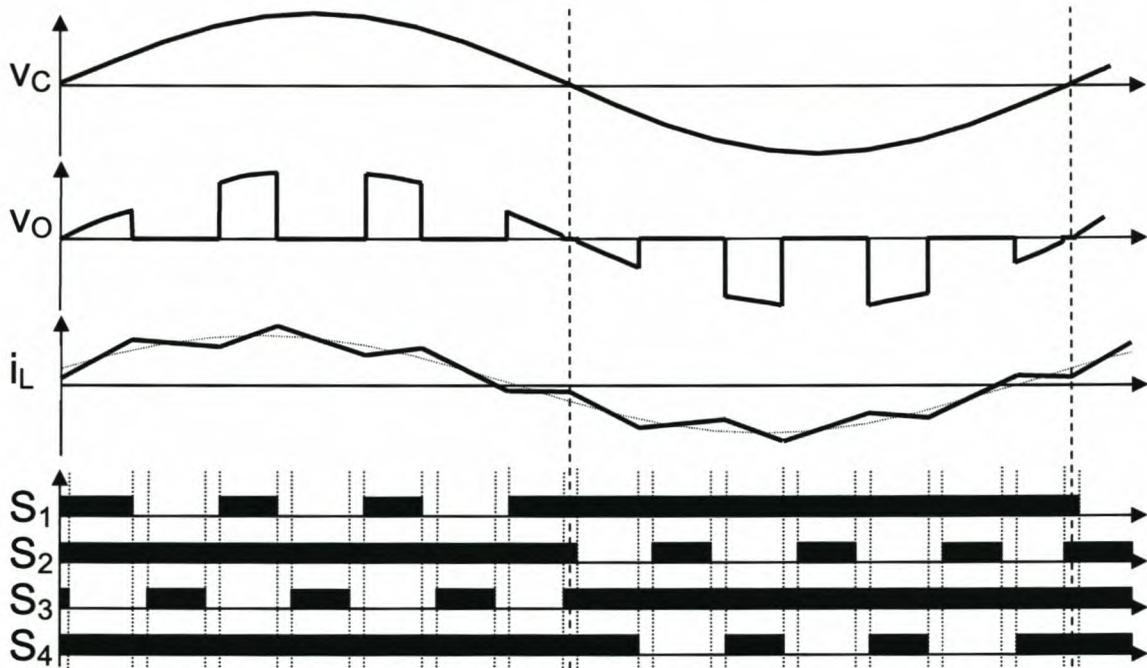
Figure 3-12: Switching scheme for voltage detection control

During the switching from positive to negative half-cycle and from the negative to positive half-cycle there will be a short time in which the capacitor is short-circuited and this can lead to over-current. At this point the voltage is very small. There is a small window around zero in the supply voltage in which all four switches may be turned on. The width of this window, t_W, is determined by the on-state voltages of the switches and the diodes. Figure 3-13 illustrates this.

From Figure 3-11 it can be seen that there will not be an interruption of i_L as during the positive half-cycle S_4 and S_3's diode provides a free-wheeling path for i_L. If i_L were to become negative and v_C is still positive, S_3 and S_4's diode will provide this path. During the negative half-cycle S_2 and S_1's diode

Chapter 3 – Single-phase AC-to-AC converter topologies

provides a free-wheeling path for i_L. If the current were to become positive now S_1 and S_2's diode will provide the free-wheeling path.
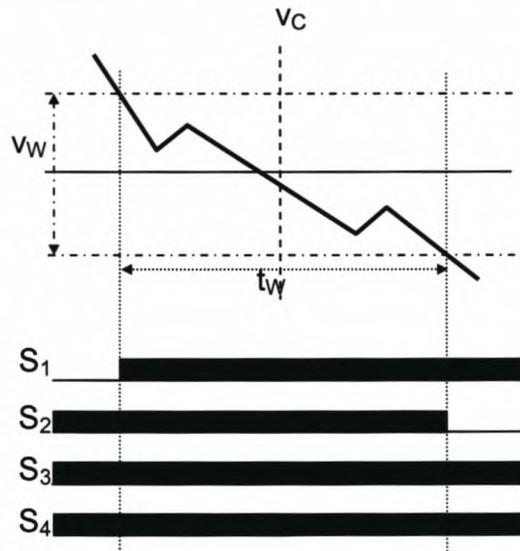
Figure 3-13: Illustration of voltage window

In [15] the author proposes a different method of switching using voltage detection. With this method each bi-directional switch will be the equivalent of one switch in an ordinary converter. Eight combinations of switching states have been identified that will not violate the two previously mentioned conditions. These combinations are shown in Table 3-1. The on or off state of the switch is denoted with 1 or 0 respectively.

Number	S_1	S_2	S_3	S_4	Sign of v_C
1	1	1	0	0	+ -
2	0	0	1	1	+ -
3	1	1	0	1	+
4	1	1	1	0	-
5	0	1	1	1	+
6	1	0	1	1	-
7	0	1	0	1	+
8	1	0	1	0	-

Table 3-1: Combinations of switching states for voltage detection control

To safely commutate between 1 and 2 the conditional combinations must be used in a specific order, depending on the sign of v_C. These commutation steps are shown in Figure 3-14. The states in this method are the same switching conditions that are used in the first method.
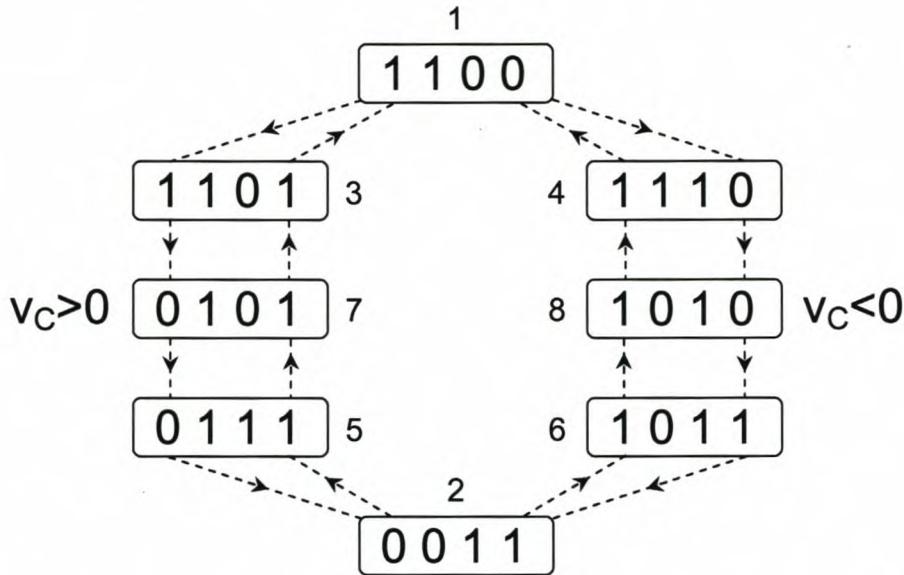
Figure 3-14: Diagram of switching conditions for voltage detection control

3.1.2 Current detection control

The inductor current, represented by the current source i_L in Figure 3-6, is detected to determine the control signals to the switches. With the wrong detection of the sign of the current, the path for i_L will be interrupted. This in turn will lead to an over-voltage that may destroy the switches.

As with the voltage detection control the switching scheme for the current detection control can be derived and represented as in Figure 3-11 and Figure 3-12. When i_L is positive S_1 and S_4 are switching but S_2 and S_3 remain off. In the voltage detection method, a short dead time is used. That gives the switches time to switch off, but it will not be used with the current control method. Instead a short over-lapping time will be needed. This implies that S_1 and S_4 will be conducting at the same time, but the capacitor will not be short-

circuited since S_2 and S_3 are not conducting. The black components in Figure 3-15 (a) and (b) show the current paths during the positive half-cycle of the current when S_1 and S_4, respectively, are on.

During i_L's negative half-cycle the opposite happens; S_2 and S_3 will be switching and S_1 and S_4 remain off as shown in Figure 3-15 (c) and (d) with S_2 and S_3 on, respectively. It can be seen that Figure 3-11 and Figure 3-15 are the same, as can be expected, since the rules mentioned must apply in all cases.

The theoretical capacitor voltage v_C, the unfiltered output voltage v_O, the inductor current i_L and the gating signals to the individual switches for current detection are shown in Figure 3-16.
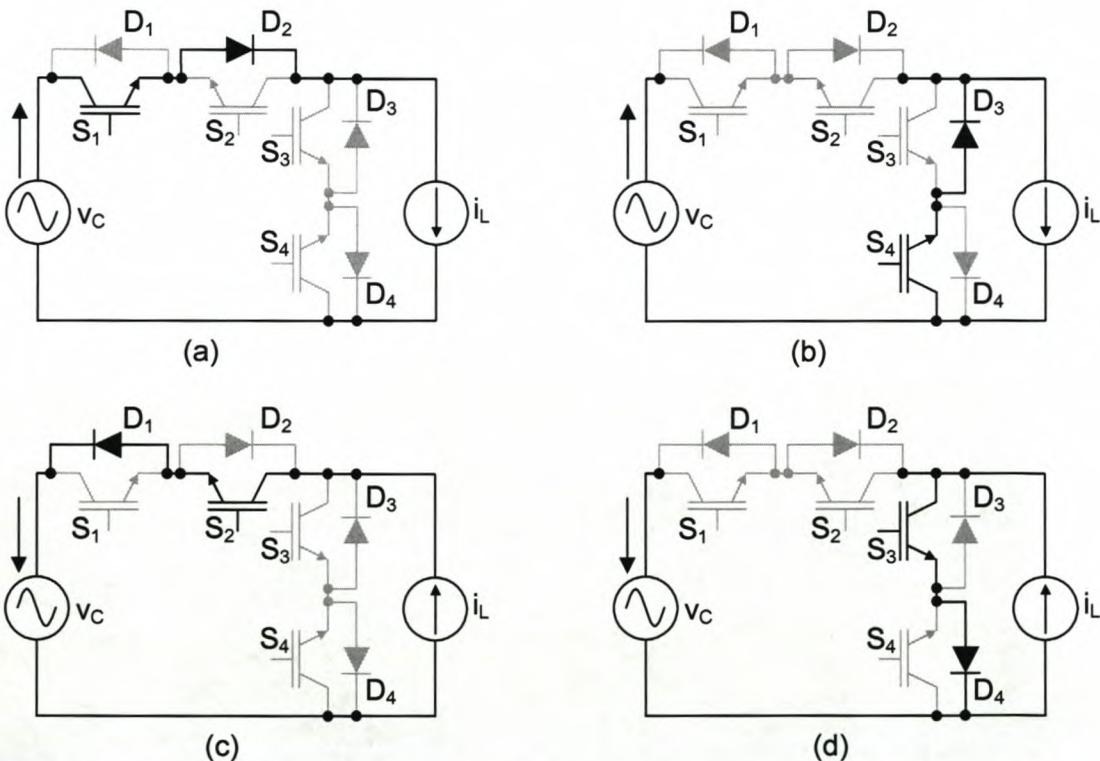
Figure 3-15: Standard AC-to-AC converter cell with current detection during (a) positive half-cycle, S_1 on; (b) S_4 on; (c) negative half-cycle, S_2 on; (d) S_3 on
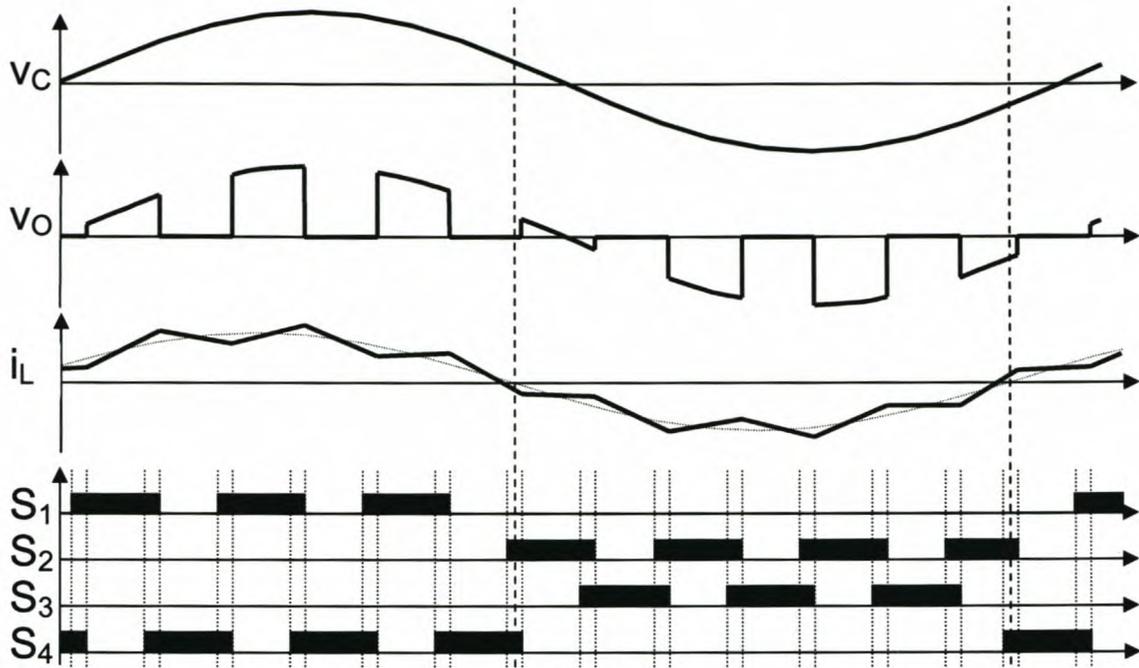
Figure 3-16: Switching scheme for current detection control

The transition between the positive and negative half-cycles in the voltage detection control were simply due to the low voltage at that point and because v_C has almost no ripple component. This is not the case with the current control method. Figure 3-16 does not indicate the full extent of this problem as the switching frequency is very low to show how v_O and i_L react to the different switching states. Should the frequency and the current ripple be of a practical size, the transition will imitate Figure 3-17. Here i_L will cross the 0 A line several times in a time window t_W with a current window i_W. The i_W depends on the ripple size and the t_W depends on i_W. A way to bypass this problem is to detect when the current enters i_W and force the switches into a safe-state combination for a short time.
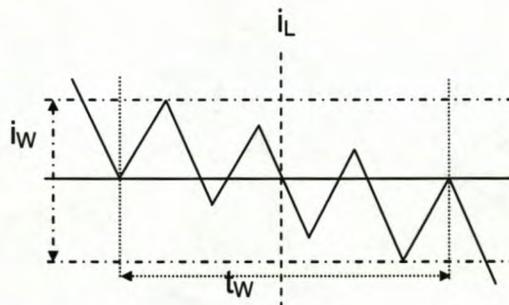
Figure 3-17: Transition of i_L with ripple

After this short time the switches will then be switched in the negative switching combinations. This also holds true for the negative to positive half-cycle transition. Should the ripple component be too large, there will be a dilemma as the window will be too large and the waiting period too long.

The author of [15] also proposes a method for the current detection control. It is similar to the voltage detection control introduced in section 3.1.1. Table 3-2 shows the legal combinations of switching states for current detection and Figure 3-18 shows the commutation method. The combinations are the same as those used above.

Number	S_1	S_2	S_3	S_4	Sign of i_L
1	1	1	0	0	+ -
2	0	0	1	1	+ -
3	1	0	0	0	+
4	0	1	0	0	-
5	0	0	0	1	+
6	0	0	1	0	-
7	1	0	0	1	+
8	0	1	1	0	-

Table 3-2: Combinations of switching states for current detection control
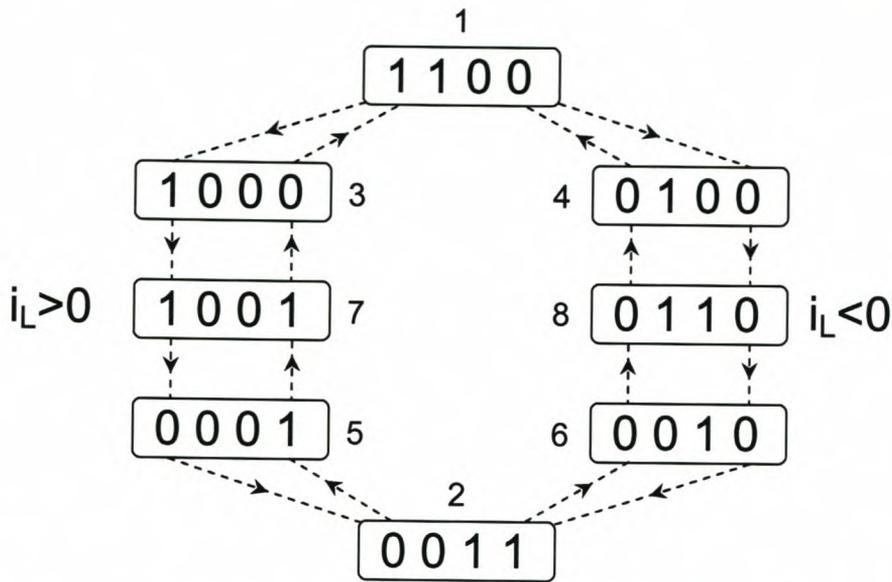
Figure 3-18: Diagram of switching conditions for current detection control

3.1.3 The full system with filters

The control strategies for the AC-to-AC converter have been discussed in sections 3.1.1 and 3.1.2. The other passive components can now be added; they are the input filter and the output filter. Figure 3-19 show the full system with the input filter made up of L_S and C_d and the output filter made up of L_O and C_O.
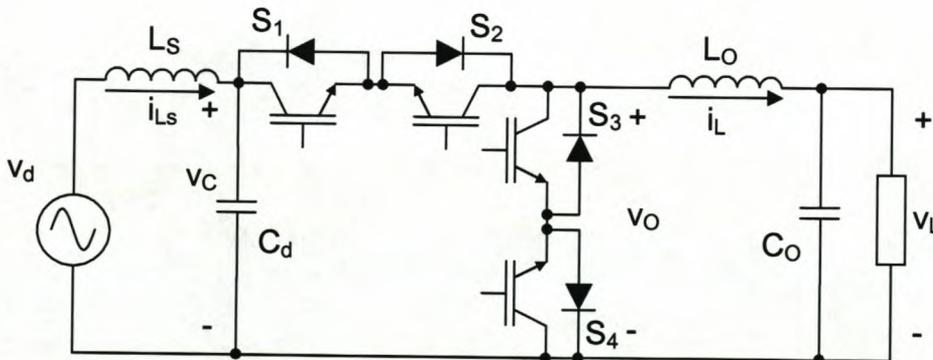
Figure 3-19: Standard AC-to-AC converter with passive components

In an ordinary buck converter the input filter will seldom be used, but in this case L_S represent the transformer's leakage inductance and in combination

with C_d they form an EMI filter. As in an ordinary buck converter, it can be shown that $v_O/v_C = D$, where D is the duty ratio of the converter.

This system has advantages such as smaller and If ewer passive components than the more traditional converters mentioned in Chapter 2 and it can react rapidly to changes in the input voltage. This topology has a drawback in that it uses non-standard switches and it has to be made up of separate switches. Using separate switches results in increased parasitic inductance: this inductance causes a voltage overshoot during the turn-off of the switches. In the next section a possible solution to this problem will be investigated.

3.2   The differential AC-to-AC converter cell

In the previous section the standard AC-to-AC converter was discussed along with the main disadvantage of non-standard switches and the resulting parasitic inductance. In this section a solution will be presented. The two control methods will also be adapted to the new topology.
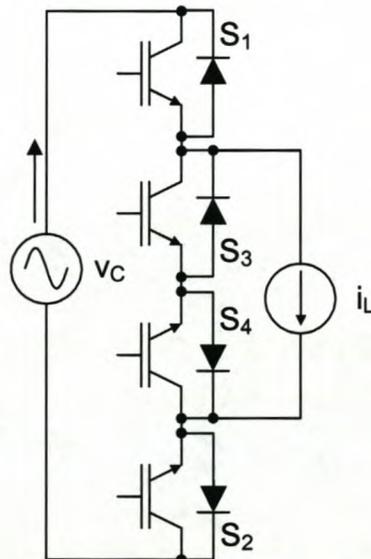
Figure 3-20: Differential AC-to-AC converter cell

Figure 3-20 shows the adapted topology. For ease of comparison the names of the switches have not been changed and it can be seen that S_2 has shifted to such a position that the converter now has two standard phase arms to form the switching components. In these phase arms the switches are close together, which minimises the parasitic inductance that in turn reduces the voltage overshoot at turn off. As before, the voltage source v_C represents the voltage over the input filter's capacitor and the current source i_L represents the current in the output filter's inductance.

The two conditions mentioned in section 3.1 still hold:

- The voltage bus must never be short-circuited unless v_C is equal to 0 V;
- A path for the load current must always exist, unless i_L is equal to 0 A.

The same three control methods apply with this topology and the main two will be discussed. They are:

- Sensing the capacitor voltage v_C;
- Sensing the inductor current i_L;

3.2.1 Voltage detection control

The discussion of the voltage control method in this topology is simple as it is similar to the voltage control method used with the standard cell. The switching scheme is as follows: if v_C is positive S_1 and S_3 switch and S_2 and S_4 remain on. If v_C is negative S_2 and S_4 switch and S_1 and S_3 remain on. The theoretical v_C, v_O, i_L and the gating signals to the individual switches with this topology is the same as in Figure 3-12. As with the standard cell, wrong detection of the voltage will short-circuit the bus and the over-current will destroy the switching devices.

The black components in Figure 3-21 (a) and (b) show where the current flows during the positive half-cycle with S_1 and S_4 on, respectively. The black components in Figure 3-21 (c) and (d) show where the current flows during

the negative half-cycle of v_C with S_2 and S_3 on, respectively. The end result is similar to the standard converter and the rules are adhered to.
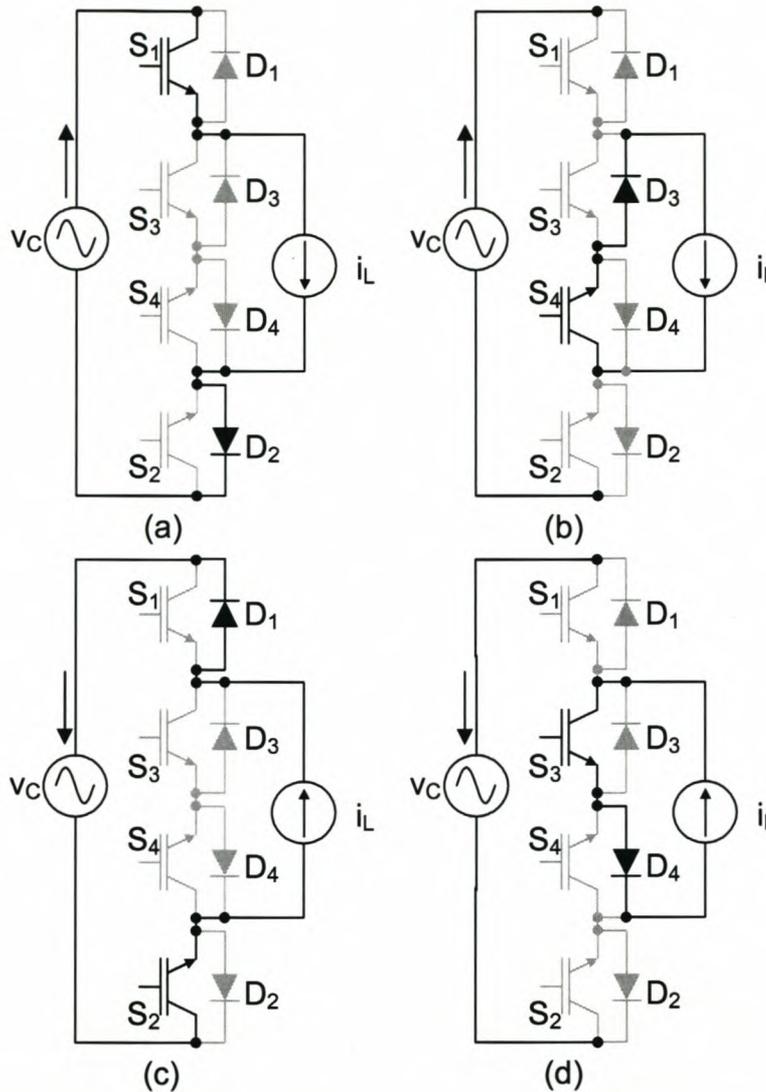
Figure 3-21: Differential AC-to-AC converter cell with voltage detection control during (a) positive half-cycle, S_1 on; (b) S_4 on; (c) negative half-cycle, S_2 on; (d) S_3 on

3.2.2 Current detection control

With the differential AC-to-AC converter the switching scheme is similar to the standard cell. When i_L is positive S_1 and S_4 are switching and S_2 and S_3 are open circuit, while during i_L's negative half-cycle S_2 and S_3 are switching and S_1 and S_4 remain off. The theoretical v_C, v_O, i_L and the gating signals to the

individual switches with this topology are similar to those shown in Figure 3-16. As with the standard AC-to-AC converter cell, the components in which the current flows during the current detection control are similar to the voltage detection control. This implies that Figure 3-21 holds true for this method of control. The switching scheme described in [15] holds for the current and voltage control methods with the differential AC-to-AC converter cell.

3.2.3 The full system with filters
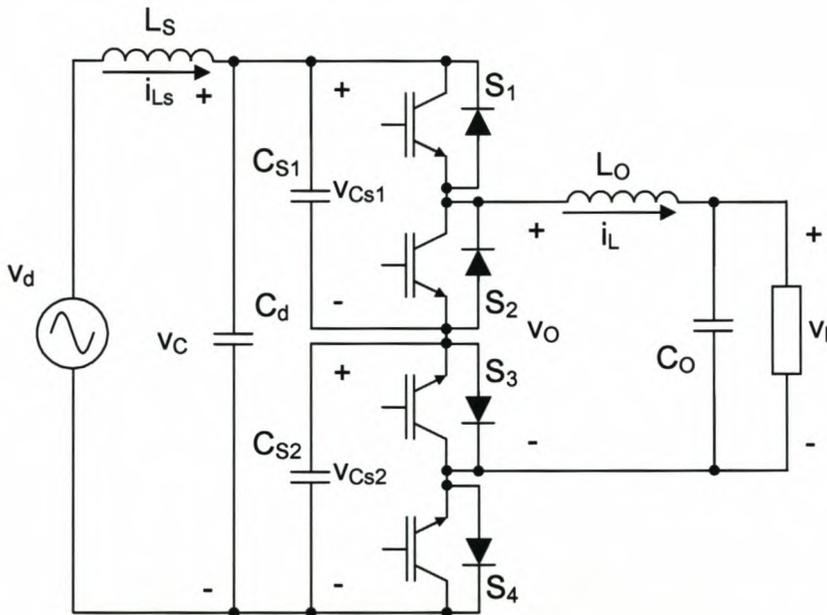
Figure 3-22: Differential AC-to-AC converter with passive components

As before the full AC-to-AC converter is shown in Figure 3-22 with all its passive components. L_S and C_d forms the input filter and L_O and C_O forms the output filter. C_{S1} and C_{S2} are two snubber capacitors. The snubber capacitors will help ensure a current path for the inductor current. The switches were also renamed to produce a more logical sequence; the change is as follows:

$$S_1 \rightarrow S_1$$
$$S_2 \rightarrow S_4$$
$$S_3 \rightarrow S_2$$
$$S_4 \rightarrow S_3$$

The main advantage of this topology and the standard AC-to-AC converter is that it is based on two standard half-bridge converter modules but it cannot be used in applications where the neutrals of the load and supply must be connected to each other.

The standard AC-to-AC converter and the differential AC-to-AC converter discussed in sections 3.1 and 3.2 are both buck converter topologies. In the next section the boost converter and its disadvantages will be discussed.

3.3   The boost AC-to-AC converter

The boost converter is in essence a buck converter with the load and supply swapped around. Figure 3-23 shows the boost converter of a standard AC-to-AC converter as represented in Figure 3-19.
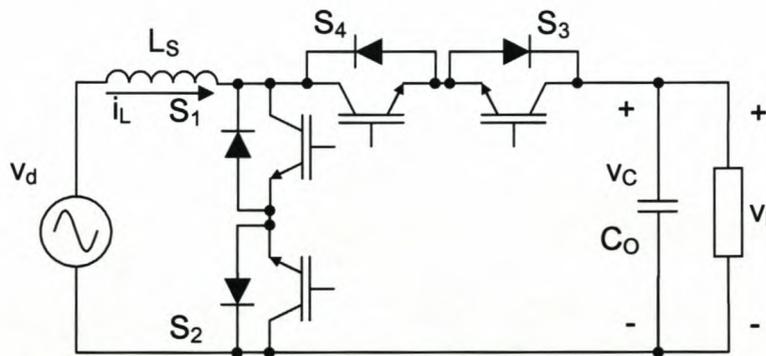
Figure 3-23: Standard boost AC-to-AC converter

The switches were named in such a way that the switching scheme and control of section 3.1 are the same with this topology. The non-standard switches are still a problem and the differential converter in Figure 3-22 can be adapted to a boost converter topology. Figure 3-24 shows this converter with the switches named in such a way that the switching scheme and control are the same as in section 3.2.
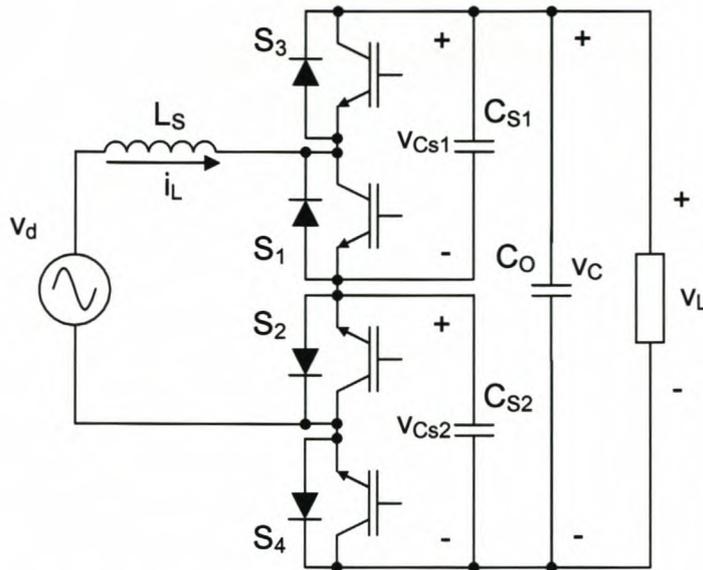
Figure 3-24: Boost differential AC-to-AC converter

The boost converter has, compared to the buck converter, some disadvantages that will make this topology undesirable. To begin with there is a non-linear relation between the ratio of the output voltage and the duty cycle of the boost converter and this complicates the design of the controller. During the converter's start-up, large inrush currents will flow through the switches and diodes, but in the buck converter the capacitors will take care of the currents.

The final important disadvantage is that the output voltage in this topology is always larger than the input voltage and this means that the load voltage cannot be decreased by reducing the duty cycle. In buck converters this can be done and is used during fault stages. Thus for protection another switch must be added. This switch can be a mechanical switch so as to handle the currents associated with faults. These switches have a lower speed than the converter's silicon switches and this means that the converter's switches must be rated to handle the large fault currents for a long period of time until the mechanical switches are fully activated. This is a costly method.

3.4 The step-down transformer

As mentioned in Chapter 2 the converter will be at the end of a long MV line at the step-down transformer that steps the medium voltage down to low voltage. This means the transformer will have to step 11 kV_{LL} down to 400 V_{LL}. Since the specific converter is single phase with a 16 kVA single-phase transformer, these values will be converted to 11 kV_{LL} and 230 V_{LN}, respectively. The primary voltage remains 11 kV because the lines feeding the transformer are three-phase with no neutral connection. Both the buck and the boost converters can be used and in this section, as the transformer is being investigated, the converter will be represented by its functional block.

The transformer winding ratio will be different for the buck and boost converters. For the buck converter it will be such that at the minimum voltage at the primary (nominal -40%), the secondary voltage will be nominal. In this case the nominal is 230 V. With the boost converter the winding ratio will be such that if the primary has the maximum voltage (nominal +10%) the secondary will be at nominal.

The question of the design of the transformer still remains. Figure 3-25 shows a centre-tapped transformer with the converter in one of the taps. This is intended to reduce the converter rating as it will not have to convert the full load power.
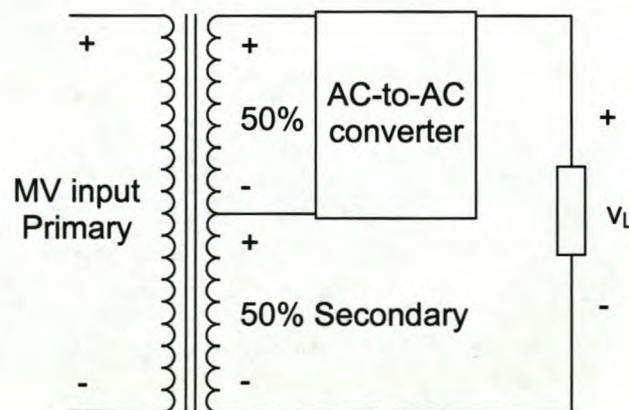
Figure 3-25: Centre-tapped transformer

The load voltage v_L in this topology will be 50% of the secondary voltage of the transformer plus the output voltage of the converter. The transformer is rated at 16 kVA and the primary voltage can vary between 12.1 kV and 6.6 kV. Table 3-3 presents the two types of converters' voltages.

Type	Secondary Max. Voltage	Secondary Min. Voltage	Converter Max. in Voltage	Converter Min. in Voltage	Converter output V for Max. in Voltage	Converter output V for Min. in Voltage
Buck	422 V	230 V	211 V	115 V	19 V	115 V
Boost	230 V	125 V	115 V	62.5 V	115 V	167.5 V

Table 3-3: Converter's input and output voltages with centre-tap

Type	Converter Max. in voltage	Converter Max. in Current	Converter Max. Rating
Buck	211 V	70 A	14.77 kVA
Boost	115 V	128 A	14.72 kVA

Table 3-4: Maximum converter rating

The subsequent maximum power converted of both the converters is half that of the transformer, 8 kVA, but if the converters' ratings are define as the maximum input voltage times the maximum input current the ratings will be as show in Table 3-4. At these voltage and power ratings there is little choice of switches on the market and when adjustments are made for inrush and fault stages, the switches are chosen to be in the 1200 V and 600 V range.

Table 3-5 indicates the voltages for the converters, if the transformer is not a centre-tapped transformer. Figure 3-26 shows the system's diagram.

Type	Secondary Max. Voltage	Secondary Min. Voltage	Converter Max. in Voltage	Converter Min. in Voltage	Converter Max. out Voltage	Converter Min. out Voltage
Buck	422 V	230 V	422 V	230 V	230 V	230 V
Boost	230 V	125 V	230 V	125 V	230 V	230 V

Table 3-5: Converter's input and output voltages without centre-tap
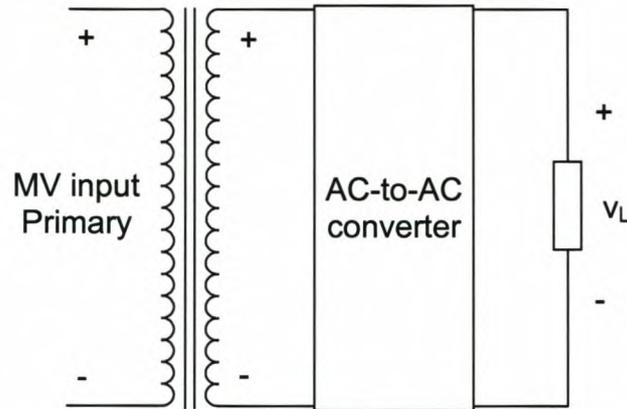
Figure 3-26: Converter without centre-tapped transformer

With these voltages and ratings the switches chosen are in the 1200 V range, because the peak voltage is 597 V. Due to the difficulty of protecting the centre-tapped topology, it will not be considered and is left for future investigation.

3.5 Summary

In this chapter the different AC-to-AC converters were discussed and two main topologies were considered: the buck and the boost converters. These were divided into two more groups: the standard cell and the differential cell. The transformer was also discussed and the decision was made to use the ordinary transformer topology as in Figure 3-26. Table 3-6 summarises the advantages and disadvantages of the topologies.

Topology	Advantage	Disadvantage
Standard Buck converter	Fast reaction to input voltage changes	Non-standard switches and parasitic inductance
Differential Buck converter	Standard half-bridge switches and snubber capacitor reduces parasitic.	Cannot use where the supply and the load's neutral must be connected
Standard Boost converter	Fewer passive components.	Difficult to control and to protect. Non-standard switches and parasitic inductance
Differential Boost converter	Fewer passive components	Difficult control and to protect. Cannot use where the supply and the load's neutral must be connected
Voltage detection control	Relatively simple switching scheme	Wrong detection leads to over-current
Current detection control	Relatively simple switching scheme	Wrong detection leads to over-voltage and more complicated control.

Table 3-6: Summary of topologies

From Table 3-6 it can be seen that voltage detection control will be a safer type of control than the current detection control and will be easier to implement. With the topology the buck converter has fewer disadvantages than the boost converter and the differential cell poses fewer problems with inductance than the standard cell. The final choice of converter to be used is a buck converter-based converter with a differential cell topology and using voltage detection for the control.

In the next chapter the converter design will be discussed.

Chapter 4

Analysis and design of the voltage regulator

4 Analysis and design of the voltage regulator

In the previous chapters the evolution of this project was sketched. Some of the existing solutions were highlighted as well as work done on the AC-to-AC converters. The decision was made as to the type of topology that will be used. The buck AC-to-AC converter was deemed the best solution to the problem stated in Chapter 2. Figure 4-1 shows the topology to be considered.
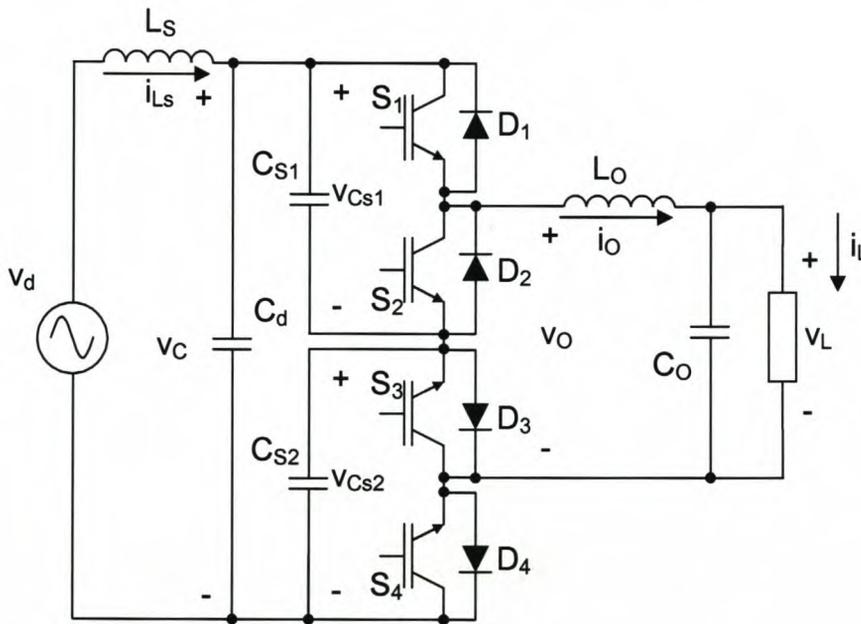
Figure 4-1: Buck AC-to-AC converter topology

The buck AC-to-AC converter topology consists of two half-bridge converters placed back-to-back with snubber capacitors, input filter and output filter. The output filter consists of an inductor (L_O) and a capacitor (C_O). The input filter consists only of a capacitor (C_d), the inductor L_S represent the leakage inductance of the step-down transformer. A power factor of 1 or almost 1 represents the ideal operating conditions; this implies a small to no phase shift between the voltages and currents. In this analysis the load is assumed to be purely resistive to obtain this power factor of 1.

4.1 Detailed analysis

For the analysis of the converter, equations must be obtained for the voltages and currents in the converter. The output voltage (v_L) and current (i_L) will be the reference point for the equations and since the load is resistive, the current and voltage are in phase with one another. From there the current through L_O (i_O) will be obtained as well as the unfiltered voltage (v_O). The snubber capacitor voltages (v_{Cs1} and v_{Cs2}) will be shown to be closely related to the input capacitor's voltage (v_C). Figure 4-1 show the voltages and currents to be obtained.

The output voltage (v_L) is known because the converter is to act as a voltage regulator. V_L in Equation (4-1) is the amplitude of the output voltage and is equal to the duty ratio, D, times V_C, the input voltage. I_L in Equations (4-2) and (4-3) is the amplitude of the current. R is the load resistance.

$$v_L = V_L \sin \omega_1 t \tag{4-1}$$
$$i_L = I_L \sin \omega_1 t \tag{4-2}$$
$$I_L = \frac{V_L}{R} \tag{4-3}$$

Assuming that the voltage drop across the filter inductor is small, the load voltage v_L is equal to Dv_C, where D is the duty ratio. The duty ratio is the percentage of the switching period that the switch is on.

From these equations and Kirchhoff's current law, it can be seen that inductor current i_O is equal to i_L plus the current through the output capacitor. The filter inductor current i_O consists of a fundamental component of the form:

$$i_{O_1} = I_{O_1} \sin(\omega_1 t) \tag{4-4}$$

as well as a ripple component. The inductor size will determine the current ripple. The current that the switching components will have to endure is equal to the peak value of i_O.

60

The unfiltered voltage v_O is a switched voltage waveform. This means that v_O is either equal to v_C when S_1 or S_4 is on or it is effectively zero (assuming there is no voltage loss over the switches) when S_2 and S_3 are on.

The snubber capacitors' voltages, v_{Cs1} and v_{Cs2}, are symmetrical. If v_C is positive then v_{Cs1} is equal to v_C and v_{Cs2} is zero (again assuming there is no voltage loss over the switches). If v_C is negative, the opposite is true. The input voltage v_C is a sinusoidal signal as shown in Equation (4-5) with V_C its amplitude. This amplitude can vary and because of this change in amplitude the converter is required. Voltages v_C and v_L have the same frequency and phase, since the converter cannot change frequency and phase.

$$v_C = V_C \sin(\omega_1 t)$$

(4-5)

The peak value of v_C will be the voltage that the switching components must be able to handle.

4.1.1 Switching component power losses

The equations for the losses in the switching components, the IGBTs and the diodes will be obtained by evaluating the conduction losses and the switching losses separately.

First the conduction losses in S_1 will be obtained over the positive half-cycle. The switching losses will then be computed.
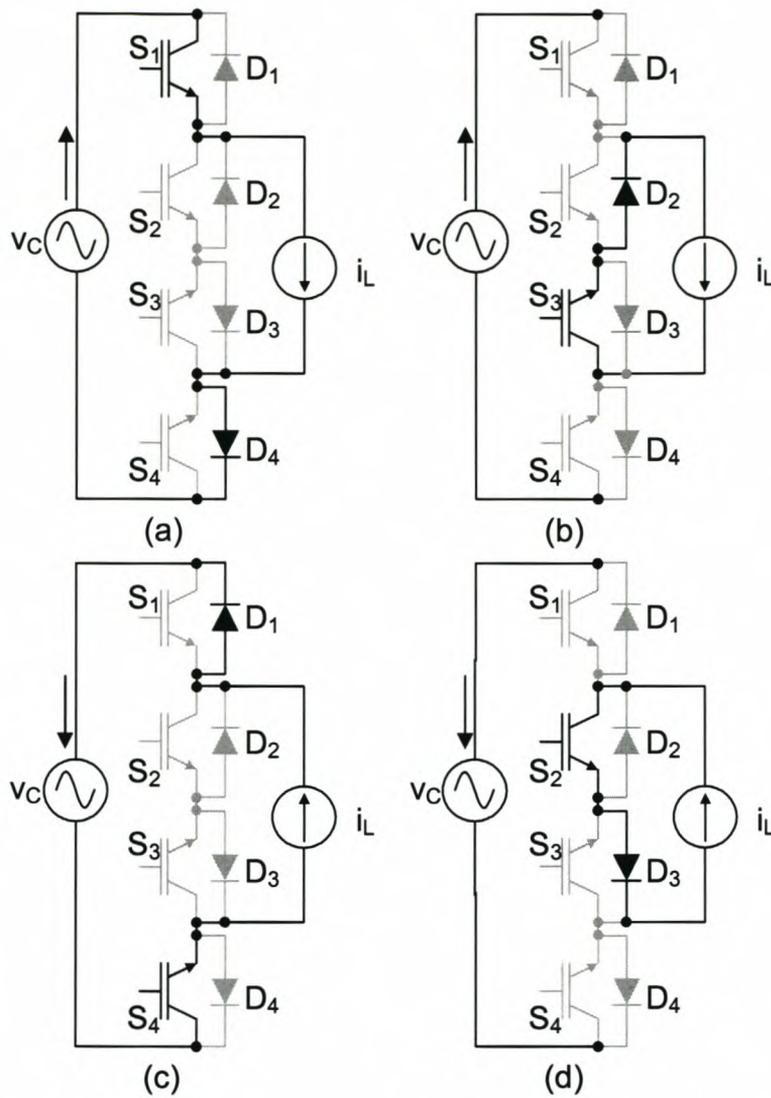
Figure 4-2: Conduction paths through switches and diodes during (a) & (b) positive half-cycle; (c) & (d) negative half-cycle

Figure 4-2 shows the conduction paths of the current during the positive and negative half-cycles. In Figure 4-2 (a) it can be seen that the current flows through S_1 and D_4 and in (b) the current flows through S_3 and D_2. In Figure 4-2 (c) the current flow through S_4 and D_1 and in (d) the current flows through S_2 and D_3. There are four basic states in which the proposed converter can be switched. The first two are where the voltage, v_C, and the current, i_O, are of the same sign with S_1 and S_4 on or S_2 and S_3 on. The other two are where v_C and i_O are of opposite signs with S_1 and S_4 or S_2 and S_3 on. The entire converter has eight states with v_C, the supply, as either positive or negative.

The positive four basic states are symmetrical to the negative four states. The states with the opposite signs are neglected because of the power factor of 1.

During the positive half-cycle of the input voltage S_3 and S_4 are continuously on and S_1 and S_2 are the switching. The saturation voltage of the IGBT and the diode are small, about 2 V, and this means that the voltage over S_3 and S_4 are also small and S_3 and S_4 can be considered as a short circuit.
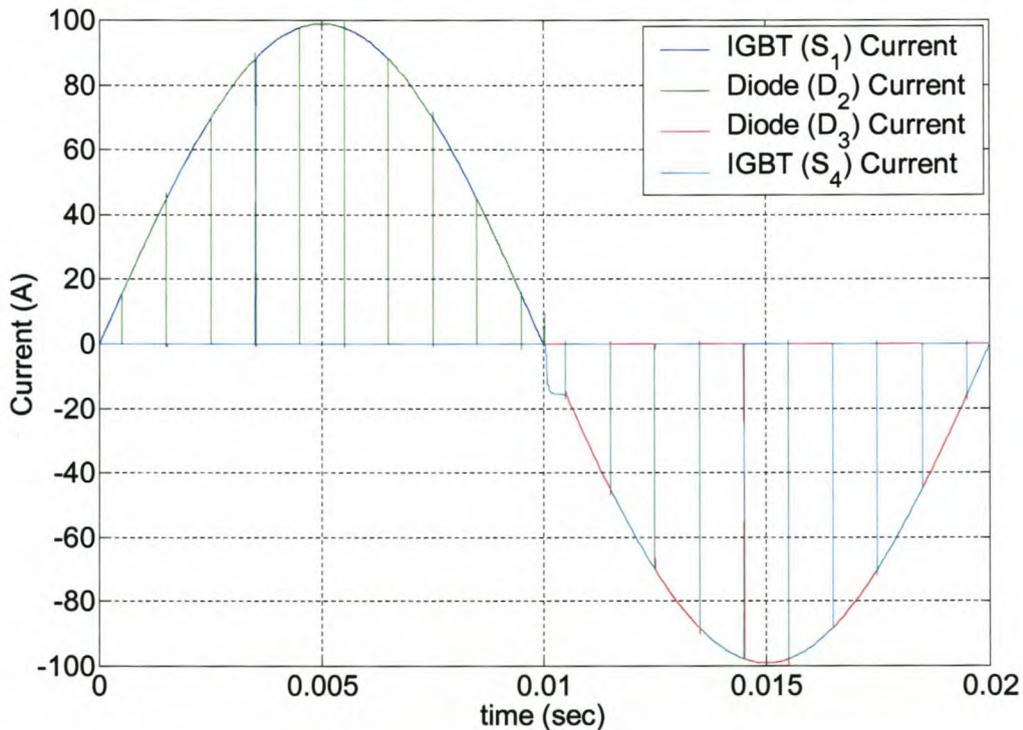
Figure 4-3: Current through IGBTs and diodes

Figure 4-3 shows the current through the components. The blue trace is the current through S_1 and D_4, the green trace is the conducted current through D_2 and S_3. Through the other components the current is zero during the positive half-cycle, if the input current is in phase with the input voltage. In Figure 4-3 the negative half-cycle can also be seen. The red trace is the current in D_3 and S_2 and the cyan trace is the current through S_4 and D_1. Again the other components have no current through them, assuming no phase shift.

Chapter 4 – Analysis and design of the voltage regulator

Figure 4-4 shows the current through S_1 compared with i_O. A few assumptions are made at this stage. To begin with, the ripple component of the output filter inductor current is ignored. The IGBT is assumed to have only an on-state voltage and no on-state resistance. Since the load is resistive and the power factor is 1, it can be assumed that the output current will always be positive when the output voltage is positive and negative when the voltage is negative. The output filter is designed in such a way that the phase difference is small. The focus is also on the positive half-cycle, because the operation of the converter during the negative half-cycle is symmetrical.

Let t_i ($1 \leq i \leq N$) be in the middle of the switching period. S_1 conducts for a duration D (duty ratio) times the switching period. To obtain the power lost, the energy lost during the i'th switching period must be found. Equation (4-6), using Equation (4-3), shows the energy being dissipated in S_1 during the i'th switching period.

$$E_{i(cond)} = V_{on(IGBT)} DT_S \, \frac{DV_C}{R} \sin(\omega_1 t_i)$$

(4-6)
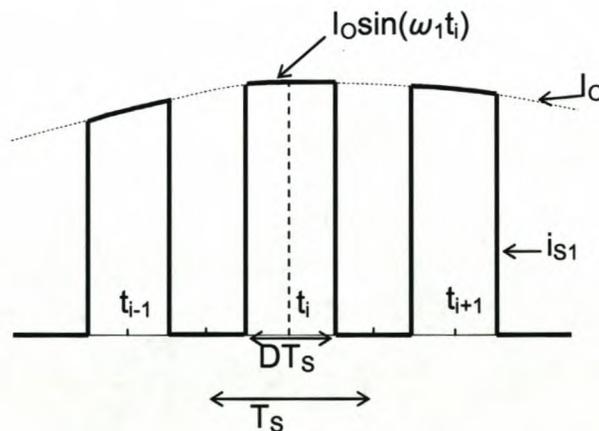
Figure 4-4: Current through S_1

The average power dissipated in S_1 over one half-cycle of the 50 Hz signal can be computed as in Equation (4-7). T_1 is the period of the 50 Hz supply voltage.

$$P_{cond} = \frac{1}{T_1} \sum_{i=1}^{N} E_{i(cond)}$$

$$= \frac{1}{T_1} \sum_{i=1}^{N} DV_{on(IGBT)} \frac{DV_c}{R} \sin(\omega_1 t_i) T_s$$

$$\approx \frac{1}{T_1} \int_{0}^{T_1/2} DV_{on(IGBT)} \frac{DV_c}{R} \sin(\omega_1 t_i) dt$$

$$= D^2 V_{on(IGBT)} \frac{V_C}{R\pi} \qquad \text{(4-7)}$$

The conduction losses in S_2 are computed in the same way as in S_1 with the percentage that the switch conducts as 1-D. Equations (4-8) and (4-9) show the energy and power dissipated.

$$E_{i(cond)} = V_{on(IGBT)} (1-D) T_s \frac{DV_c}{R} \sin(\omega_1 t_i) \qquad \text{(4-8)}$$

$$P_{cond} = \frac{1}{T_1} \sum_{i=1}^{N} E_{i(cond)}$$

$$= \frac{1}{T_1} \sum_{i=1}^{N} (1-D) V_{on(IGBT)} \frac{DV_c}{R} \sin(\omega_1 t_i) T_s$$

$$\approx \frac{1}{T_1} \int_{0}^{T_1/2} (1-D) V_{on(IGBT)} \frac{DV_c}{R} \sin(\omega_1 t_i) dt$$

$$= (1-D) DV_{on(IGBT)} \frac{V_C}{R\pi} \qquad \text{(4-9)}$$

The next equation to be found is the losses in the diodes. First the current through the diode (D_2 S_2's freewheeling diode) must be found as in Equation (4-10).

$$\bar{i}_{D2} = \bar{i}_O - \bar{i}_{S1}$$

$$= \frac{1}{T_1} \int_{0}^{T_1/2} \frac{DV_C}{R} \sin(\omega_1 t) dt - \bar{i}_{S1}$$

$$= (1-D) \frac{DV_C}{R\pi} \qquad \text{(4-10)}$$

The power lost during the diode conduction is given in (4-11).

$$P_{cond} = V_{on(Diode)}\bar{i}_{D2}$$

$$= (1-D)DV_{on(Diode)}\frac{V_C}{R\pi} \tag{4-11}$$

$V_{on(IGBT)}$ and $V_{on(Diode)}$ are the on-state voltages of the IGBT and the diode, respectively. These values are found in the IGBT's data sheet.

Equation (4-12) gives the conduction losses in D_1.

$$P_{cond} = V_{on(Diode)}\bar{i}_{D1}$$

$$= D^2 V_{on(Diode)}\frac{V_C}{R\pi} \tag{4-12}$$

The total conduction losses during the positive half-cycle can be found if the loss in the components in which the current flows is computed. The components are S_1, D_4, S_3 and D_2. The equations for the conduction losses are (4-13) to (4-16).

$$P_{cond(S_1)} = D^2 V_{on(IGBT)}\frac{V_C}{R\pi} \tag{4-13}$$

$$P_{cond(S_3)} = (1-D)DV_{on(IGBT)}\frac{V_C}{R\pi} \tag{4-14}$$

$$P_{cond(D_4)} = D^2 V_{on(Diode)}\frac{V_C}{R\pi} \tag{4-15}$$

$$P_{cond(D_2)} = (1-D)DV_{on(Diode)}\frac{V_C}{R\pi} \tag{4-16}$$

The same method is now used to obtain the switching losses. First the energy lost and then the power lost are calculated.

$E_{i(switch)}$ is the energy lost due to the switching of the IGBT and P_{switch} is the power lost during the switching. The equations for these losses can be found

in [5: pp. 20 - 24]. In Equation (4-17) v_C is given by Equation (4-5) and i_O from Equation (4-4).

$$E_{i(switch)} = \tfrac{1}{2} v_C i_O \left(t_{on} + t_{off}\right)$$

$$= \tfrac{1}{2} V_C \sin(\omega_1 t_i) {DV_C}\big/_R \sin(\omega_1 t_i)\left(t_{on} + t_{off}\right)$$

$$= \frac{DV_C^2}{4R}\left(t_{on} + t_{off}\right)\sin^2(\omega_1 t_i) \tag{4-17}$$

$$P_{switch} = \frac{DV_C^2}{4T_1 T_S R}\left(t_{on} + t_{off}\right)\int_0^{T_1/2}\sin^2(\omega_1 t_1)dt$$

$$= \frac{DV_C^2}{16T_S R}\left(t_{on} + t_{off}\right) \tag{4-18}$$

The switching losses for S_1 are given in Equation (4-18). Since S_3 and S_4 are on in the positive half-cycle, they do not have switching losses. During the positive half-cycle there is no current flowing in S_2, but there is current through D_2. The reverse recovery losses in D_2 must be computed. The best way to compute the total switching losses is to use the turn-on and turn-off energy as given in the data sheets, since this takes the reverse recovery and its effect on the turn-on losses of the IGBT into account.

$$P_{switch} = \left(E_{on} + E_{off}\right)f_S \tag{4-19}$$

Equation (4-19) gives the switching losses with E_{on} the turn-on energy and E_{off} the turn-off energy. The values given in the data sheets were measured at $V_{CC} = 600$ V and $I_C = 150$ A. These need to be scaled according to the current and voltages used. A graph of energy versus I_C, in the data sheet, is used for this scaling. The current is selected on the graph and the energy is read from it. This is then scaled to the voltage used by using Equation (4-20).

Chapter 4 – Analysis and design of the voltage regulator

$$\frac{V_{used}}{V_{given}} = \frac{E_{used}}{E_{graph}}$$

$$E_{used} = \frac{V_C}{600} \begin{cases} E_{on} = 12,2mWs \\ E_{off} = 17,7mWs \end{cases}$$

(4-20)

The total losses in the system will be as given in Equation (4-21).

$$P_{tot} = 2\left(P_{cond(S_1)} + P_{cond(D_4)} + P_{switch(S_1)} + P_{switch(S_2)} + P_{cond(D_2)} + P_{cond(S_3)}\right)$$

(4-21)

A comparison between the DC-to-AC and the AC-to-AC switching losses can now be made. The equations for the turn-on and turn-off energy of the DC-to-AC converter are given in Equations (4-22) and (4-23). The power loss is given in Equation (4-24). In these equations $i_o = I_o \sin(\omega_1 t)$.

$$E_{on} = V_C i_o k_1$$

(4-22)

$$E_{on} = V_C i_o k_2$$

(4-23)

$$P_{on} = \sum_{n=0}^{\pi} V_C i_o k_1$$

$$= \sum_{n=0}^{\pi} V_C k_1 I_o \sin(\theta)$$

$$\approx \frac{1}{T_S} V_C k_1 I_o \int_0^{\pi} \sin(\theta) d\theta$$

(4-24)

The same equations hold true for the AC-to-AC converter with the difference that V_C is now $v_C = V_C \sin(\omega_1 t)$. This gives Equation (4-27) for the power loss.

$$E_{on} = v_C i_o k_1$$

(4-25)

$$E_{on} = v_C i_o k_2$$

(4-26)

$$P_{on} = \sum_{n=0}^{\pi} v_C i_o k_1$$

$$= \sum_{n=0}^{\pi} V_C k_1 I_O \sin^2(\theta)$$

$$\approx \frac{1}{T_S} V_C k_1 I_O \int_0^{\pi} \sin^2(\theta) d\theta \qquad \text{(4-27)}$$

The constant values before the integration are the same for both converters under the same conditions and will cancel out with computing the percentage difference. Integrating the Equations (4-24) and (4-27) gives the values in Equation (4-28) and (4-29).

$$\int_0^{\pi} \sin(\theta) d\theta = \left[-\cos(\theta) \right]_0^{\pi} = 2 \qquad \text{(4-28)}$$

$$\int_0^{\pi} \sin^2(\theta) d\theta = \left[\frac{1}{2}\theta - \frac{\sin(2\theta)}{4} \right]_0^{\pi} = \frac{1}{2}\pi \qquad \text{(4-29)}$$

Dividing Equation (4-29) by (4-28) it is found that the AC-to-AC converter's switching losses are at most 79% of that of the DC-to-AC converter's. This implies that the AC-to-AC converter's efficiency will be higher than that of the DC-to-AC converters

4.1.2 Filter inductor design

The ripple of the inductor current is determined by the output filter inductor. The larger the inductor, the smaller the current ripple. The equation for ΔI_O must be found because its maximum will yield the value of L_O. Figure 4-5 (a) and (b) show the two equivalent switching circuits of the topology, one in which S_1 and S_4 are conducting and one in which S_2 and S_3 are conducting. Figure 4-5 (c) shows the voltage over the inductor and (d) shows the current through it.

From Figure 4-5 (d) the equation for ΔI_O can be obtained. The phase shift between v_C and v_L is zero because of the unity power factor.

$$\Delta I_o \approx \frac{1}{L}(v_C - v_L)DT_S \qquad \text{(4-30)}$$

Equation (4-30) can be written in more detail by inserting v_C and v_L.

$$v_C = V_C \sin \omega_1 t \qquad \text{(4-31)}$$

$$v_L = V_L \sin \omega_1 t = DV_C \sin \omega_1 t \qquad \text{(4-32)}$$

$$\Delta I_o \approx \frac{1}{L}(V_C \sin \omega_1 t - DV_C \sin \omega_1 t)DT_S \qquad \text{(4-33)}$$

$$= \frac{1}{L}D(1-D)V_C T_S \sin \omega_1 t \qquad \text{(4-34)}$$
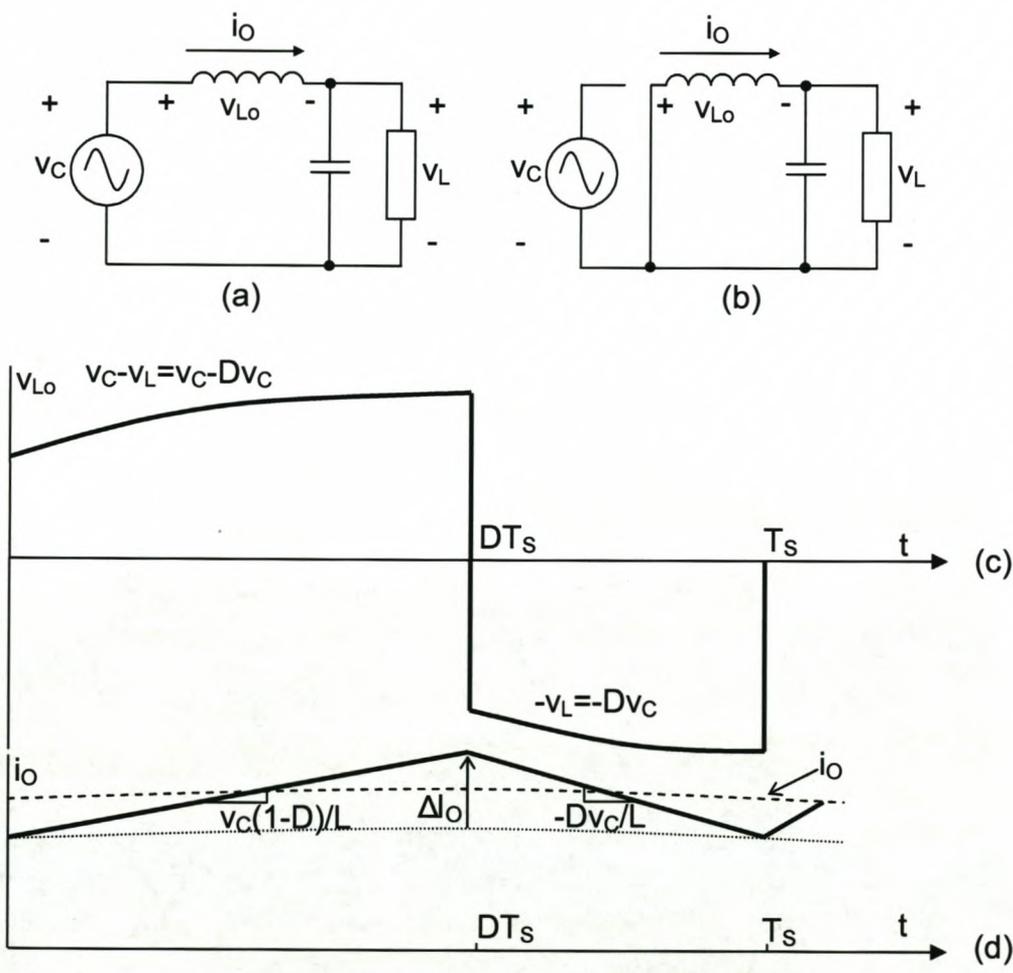
Figure 4-5: Filter inductor voltage and current

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In Equation (4-34) ω_1 is $2\pi \times 50$ rad/s and at $\omega_1 t = \pi/2$ the sinusoidal term will be at a maximum and at $\omega_1 t = 3\pi/2$ it reaches a minimum. By differentiating the equation of ΔI_O in terms of D, it is found that when $D = 1/2$ ΔI_O will be a maximum. By inserting this into Equation (4-34), L can be found. $\Delta I_{O(max)}$ is the maximum value of the current ripple.

$$L = \frac{V_c T_s}{4\Delta I_{O(max)}} \qquad\qquad \text{(4-35)}$$

It should be noted that D will be limited and this limitation will have an effect on the final value of L.

4.1.3 Filter capacitor design
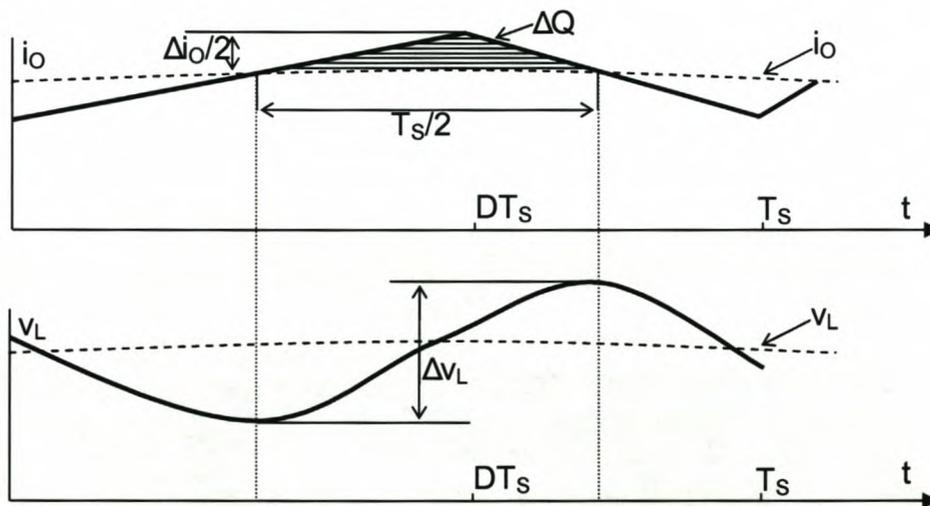
Figure 4-6: Output voltage ripple with inductor current

Figure 4-6 shows the output voltage ripple over a switching cycle. The shaded area represents the additional charge stored in the filter capacitor [5: pp. 170 - 172]. This charge and Δv_L can be written as in Equations (4-36) and (4-37).

$$\Delta Q = \frac{1}{2} \frac{\Delta i_o}{2} \frac{T_s}{2} \qquad (4\text{-}36)$$

$$\Delta v_L = \frac{\Delta Q}{C} = \frac{1}{C} \frac{1}{2} \frac{\Delta i_o}{2} \frac{T_s}{2} \qquad (4\text{-}37)$$

If Δi_O is a maximum, C will be a maximum. This means that Δi_O in Equation (4-37) will be $\Delta I_{O(max)}$ and C is as shown in Equation (4-38).

$$C = \frac{T_s \Delta I_{O(max)}}{8 \Delta V_{L(max)}} \qquad (4\text{-}38)$$

4.1.4 Unfiltered output voltage spectrum

The unfiltered output voltage, v_O, is of importance. The total harmonic distortion of v_O will be computed and in order to do this the signal will be analysed in the frequency domain. A comparison between this and the DC-to-AC converter's unfiltered output voltage will be made.

In order to write v_O in the frequency domain the Fourier series of the signal must be computed. Equations (4-39) and (4-40) give v_O and is components.

$$v_O = v_c s \qquad (4\text{-}39)$$

$$v_c = V_c \sin(\omega_1 t) \qquad (4\text{-}40)$$
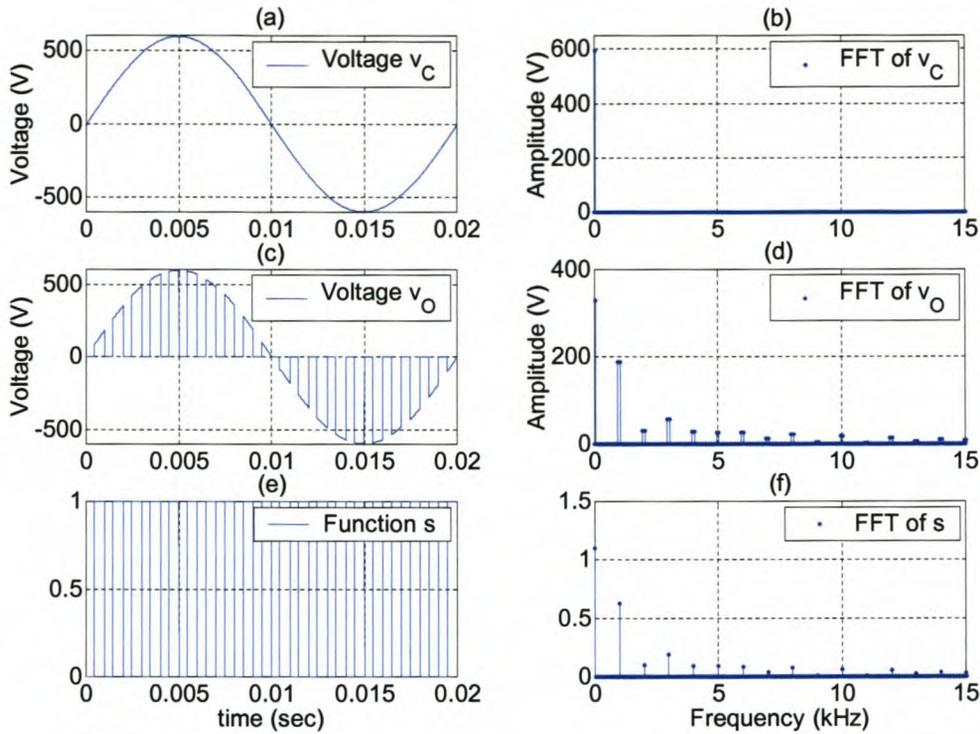
Figure 4-7: Time domain functions of (a) input voltage v_C; (c) unfiltered output voltage v_O; (e) switching function s; and amplitude spectra of (b) v_C; (d) v_O; (f) s

The other component of v_O not described in these equations is s, the switching function of the converter. The switching function is equal to 1 if one of the outer two switches is on, and it is equal to zero if both inner switches are on. Figure 4-7 shows the three functions and their amplitude spectra in the frequency domain. Table 4-1 lists the parameters of the functions used. Figure 4-7 (a) shows v_C and (b) is its amplitude spectrum. Figure 4-7 (c) is v_O and (d) is its amplitude spectrum. Figure 4-7 (e) is the switching function at 1 kHz and its amplitude spectrum is (f).

Input voltage V_C	597 V
Switching frequency f_S	1 kHz
Modulation index $m_a = D$	0.55

Table 4-1: Function parameters

The Fourier series of v_O can be found by observing that a product in the time domain results in a convolution in the frequency domain [6: pp. 33 – 43]. The definition of the complex exponential Fourier series is given in Equation (4-41) and X_n, the series' coefficients, is given in Equation (4-42). Using these equations the Fourier series for v_C and s can be computed.

$$x(t) = \sum_{n=-\infty}^{\infty} X_n e^{jn\omega_s t} \tag{4-41}$$

$$X_n = \frac{1}{T_S} \int_{t_0}^{t_0+T_S} x(t) e^{-jn\omega_s t} dt \tag{4-42}$$

Using Euler's theorem v_C can be expanded into Equation (4-43). The coefficients are given in (4-44) and (4-45). X_0 is zero in this case.

$$v_C = V_C \frac{\left(e^{j\omega_1 t} - e^{-j\omega_1 t}\right)}{2j} \tag{4-43}$$

$$X_1 = \frac{V_C}{2j} \tag{4-44}$$

$$X_{-1} = -\frac{V_C}{2j} \tag{4-45}$$

The Fourier series of s can be found by using Equations (4-41) and (4-42) and taking the integration period between $-T_s/2$ and $T_s/2$. T_S is the period of s, ω_s is the frequency and τ is D times T_S [3: pp. 237 – 238]. The zero coefficient is found first. Figure 4-8 shows the function s.
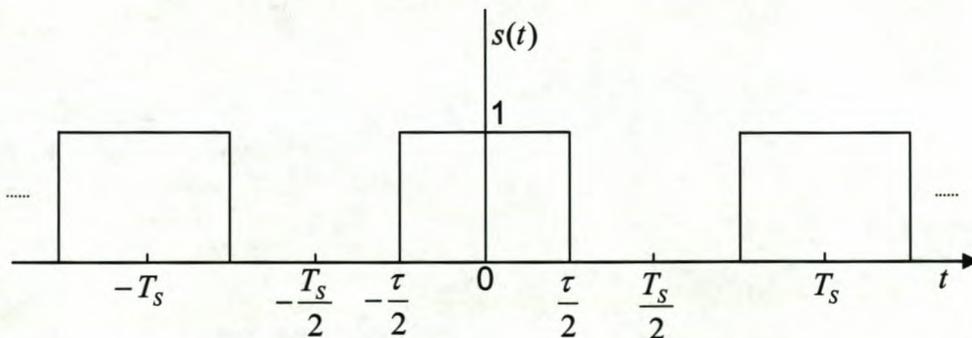
Figure 4-8: Switching function s

$$X_0 = \frac{1}{T_S} \int_{\tau/2}^{\tau/2} 1 dt \tag{4-46}$$

$$= \frac{\tau}{T_S} \tag{4-47}$$

The n'th coefficient is found next with $\omega_S = 2\pi f_S$.

$$X_n = \frac{1}{T_S} \int_{\tau/2}^{\tau/2} e^{-jn2\pi f_S t} dt \tag{4-48}$$

$$= \frac{1}{T_S} \left(\frac{e^{-j\pi n f_S \tau}}{-j2\pi n f_S} + \frac{e^{j\pi n f_S \tau}}{j2\pi n f_S} \right)$$

$$= \frac{1}{T_S \pi n f_S} \left(\frac{e^{j\pi n f_S \tau}}{j2} - \frac{e^{-j\pi n f_S \tau}}{j2} \right)$$

$$= \frac{\tau}{T_S} \frac{\sin(\pi n f_S \tau)}{\pi n f_S \tau}$$

$$= \frac{\tau}{T_S} \operatorname{sinc}(n f_S \tau) \tag{4-49}$$

Using Equations (4-41), (4-47) and (4-49) s can be reconstructed as in Equation (4-51).

$$s = X_0 + \sum_{n=1}^{\infty} X_n e^{jn\omega_S t} + \sum_{n=-\infty}^{-1} X_n e^{jn\omega_S t} \tag{4-50}$$

$$= \frac{\tau}{T_S} + \sum_{n=1}^{\infty} \frac{\tau}{T_S} \operatorname{sinc}(n f_S \tau) e^{jn2\pi f_S t} + \sum_{n=-\infty}^{-1} \frac{\tau}{T_S} \operatorname{sinc}(n f_S \tau) e^{jn2\pi f_S t} \tag{4-51}$$

As noted in Equation (4-39), v_O can be found by multiplying s and v_C and is given in Equation (4-52) with its coefficients.

$$v_O = \left(\frac{V_C \tau}{T_S 2j} \right) \left(\left(e^{j\omega_1 t} - e^{-j\omega_1 t} \right) + \sum_{n=-\infty}^{\infty} \operatorname{sinc}(n f_S \tau) \left(e^{j\omega_1 t} - e^{-j\omega_1 t} \right) e^{jn\omega_S t} \right) \tag{4-52}$$

$$X_0 = 0$$

$$X_1 = \frac{V_C \tau}{T_S \, 2j}$$

$$X_{-1} = -\frac{V_C \tau}{T_S \, 2j}$$

$$X_n = \frac{V_C \tau}{T_S \, 2j} \operatorname{sinc}(nf_s \tau)$$

The convolution between these two signals gives a sinc-function shifted in frequency so that it is centred at ω_1 and its multiples as shown in Figure 4-9. The DC value is zero and the 50 Hz (ω_1) impulse of the sine-wave appears. The parameters used for the function is given in Table 4-2.

Input voltage $V_d = V_C$	597 V
Switching frequency f_S	5 kHz
Modulation index $m_a = D$	0.55

Table 4-2: Parameters for amplitude spectrum
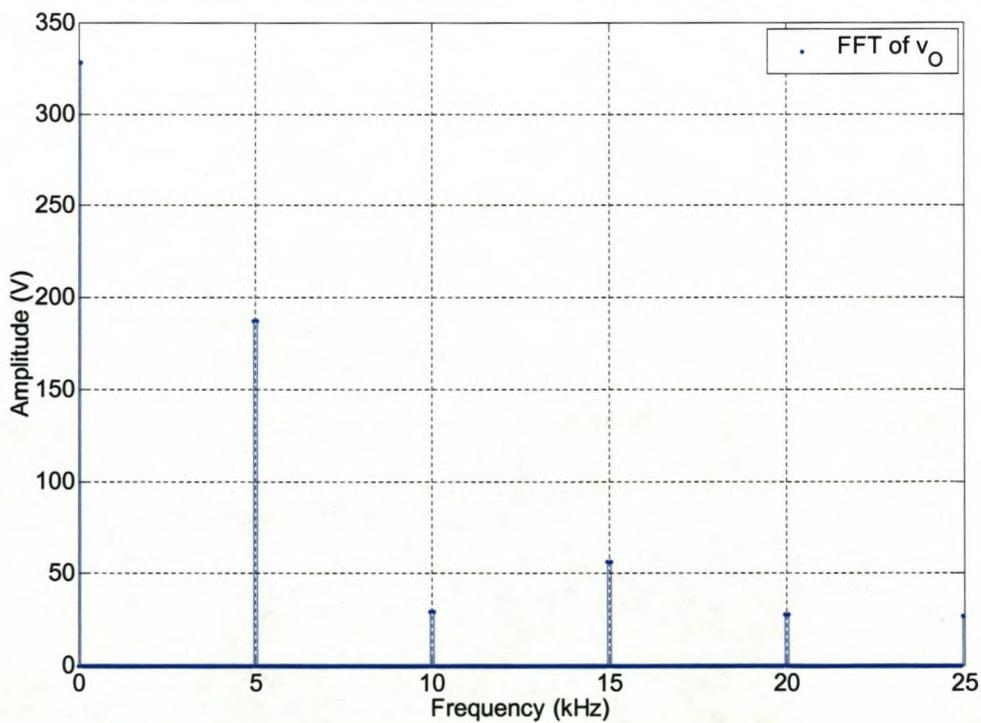
Figure 4-9: Amplitude spectrum of v_O

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The unfiltered output voltage of a DC-to-AC converter is a block wave with a PWM duty ratio and an amplitude of $\pm V_d/2$. This voltage in the time domain is shown in Figure 4-10 and in the Fourier series is shown in Figure 4-11 (b). The Fourier series of the DC-to-AC v_O is given in Equation (4-53) with Equation (4-54) giving its coefficients [1: pp. 270].

$$v_O = \frac{1}{2}A_{00} + \sum_{n=1}^{\infty}\left(A_{0n}\cos(n\omega_1 t) + B_{0n}\sin(n\omega_1 t)\right)$$
$$..... + \sum_{m=1}^{\infty}\left(A_{m0}\cos(m\omega_s t) + B_{m0}\sin(m\omega_s t)\right)$$
$$..... + \sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty}\left(A_{mn}\cos(m\omega_s t + n\omega_1 t) + B_{mn}\sin(m\omega_s t + n\omega_1 t)\right) \qquad \text{(4-53)}$$

For odd values of n and m

$$A_{mn} + jB_{mn} = \frac{V_d j}{m\pi}J_n\left(\frac{m\pi D}{2}\right)\left(1 + e^{-jm\pi}\right) = 0$$

For even values of n and m

$$A_{mn} + jB_{mn} = \frac{V_d}{jm\pi}J_n\left(\frac{m\pi D}{2}\right)\left(1 - e^{-jm\pi}\right) = 0$$

and J_n is a Bessel function of the first type

$$J_n(x) = \frac{1}{2\pi}\int_{-\pi}^{\pi}e^{j(x\sin y - ny)}dy \qquad \text{(4-54)}$$

Figure 4-11 (a) shows the amplitude spectrum of v_O in the AC-to-AC converter topology and (b) shows it in the DC-to-AC converter topology. The parameters are given in Table 4-3. It can be seen that the AC-to-AC converter has a large 50 Hz component with smaller components at the 5 kHz switching frequency and its multiples. The AC-to-AC converter does not have sideband harmonics, where the DC-to-AC converter has. The DC-to-AC converter also has a large component at 5 kHz. This is the reason that the THD of the DC-to-AC converter is very large, 226.1%, compared to the AC-to-AC converter's THD, 86.6%. The modulation index m_a is equal to the duty ratio (D) [5] and these THDs were computed at the maximum D of 0.55. If D increases then the THD will decrease.

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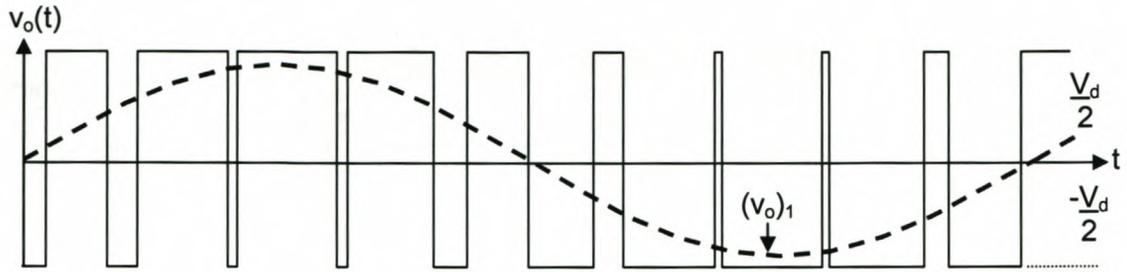
Figure 4-10: DC-to-AC converter's v_O in time domain

Input voltage $V_d = V_C$	597 V
Switching frequency f_S	5 kHz
Modulation index $m_a = D$	0.55

Table 4-3: Parameters for frequency response
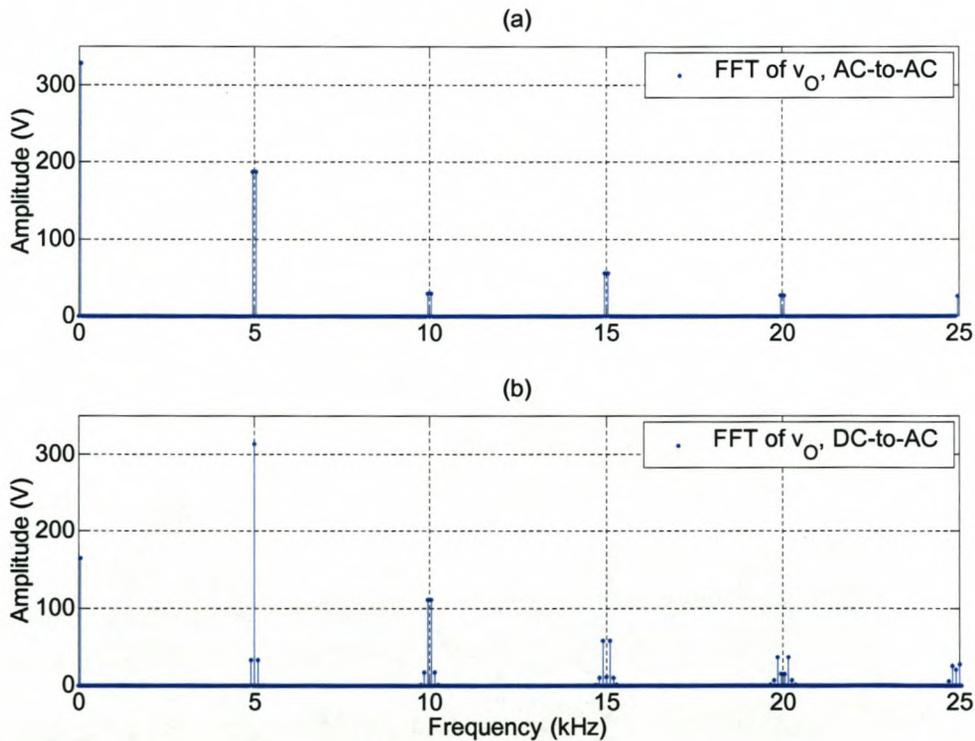
Figure 4-11: Frequency response of filter of (a) the AC-to-AC converter;
(b) the DC-to-AC converter.

4.1.5 Fault analysis
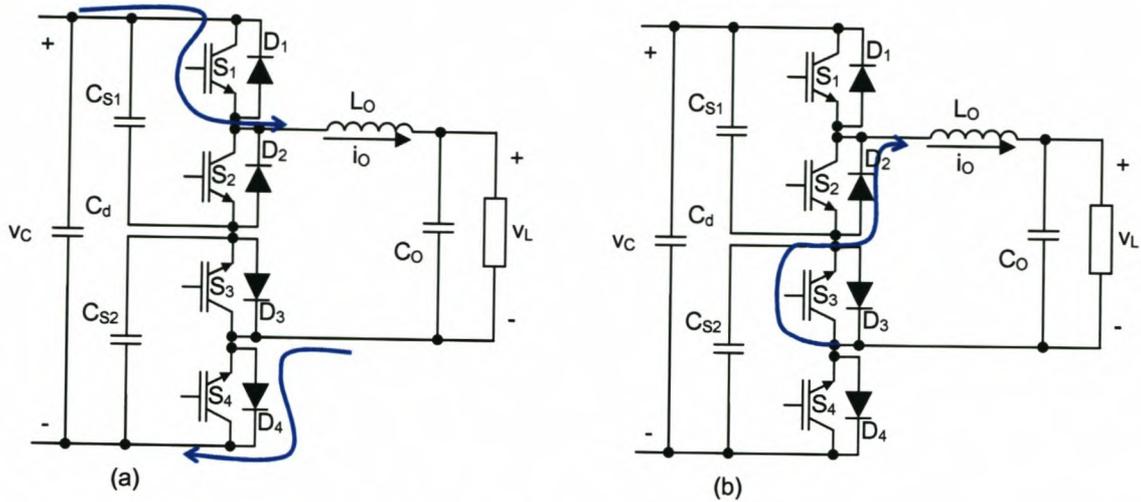
Figure 4-12: Current direction in converter with (a) S_1 conducting; (b) S_2 conducting

Figure 4-12 (a) shows the current through the components if v_C and i_L are positive and S_1 is on. Figure 4-12 (b) shows the same circuit, but S_2 is on.

If a fault were to occur in an ordinary DC-to-AC converter, the IGBTs will just be switched off. The energy stored in the filter inductor will then return to the DC-bus capacitors. With this topology, if a fault were to occur and all the switches are switched off, all the stored energy will be dumped into the snubber capacitors. This will be an undesirable situation, since this can destroy the switches.
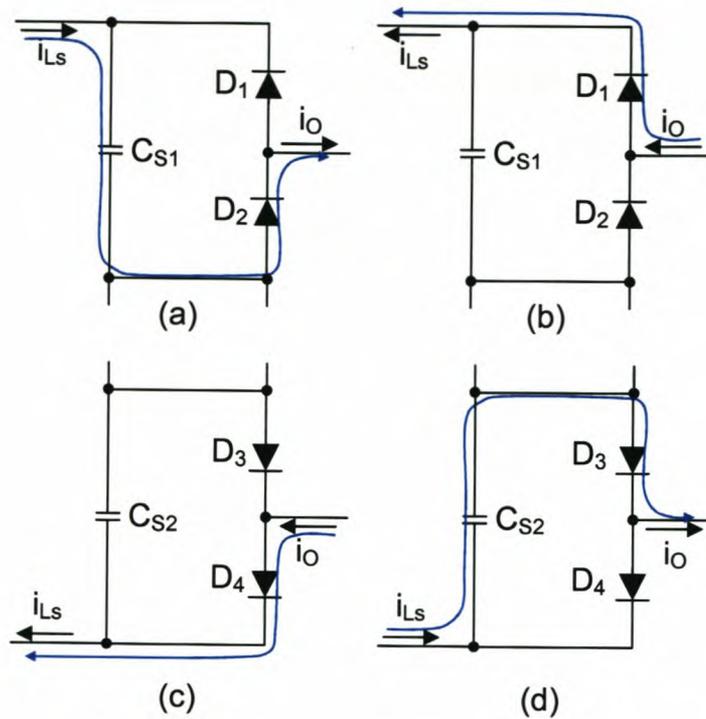
Figure 4-13: Fault current paths through snubbers without commutation

Figure 4-13 shows the path of the fault currents if all the switches are switched off. In this figure (a) and (b) are the positive phase arm with the current positive and negative, respectively. Figure 4-13 (c) and (d) is the negative phase arm with the positive and negative current, respectively. The snubber capacitor C_{S1} will charge up if the fault occurred during the positive half-cycle of the supply voltage (v_C) and C_{S2} will charge up during the negative half-cycle of v_C. This may lead to over-voltage on some of the switches.

The solution is to keep commutating the switch pairs. This implies that if the supply voltage is in the positive half-cycle, S_1 and S_2 will be open and S_3 and S_4 will be on. When the supply voltage is negative, S_3 and S_4 will be open and S_1 and S_2 will be on.

The next aspect to be considered is the current path in the converter during the fault state before the external circuit-breaker opens. With the supply voltage positive and the inductor current positive, the current will flow as shown in Figure 4-14, through S_3 and D_2.
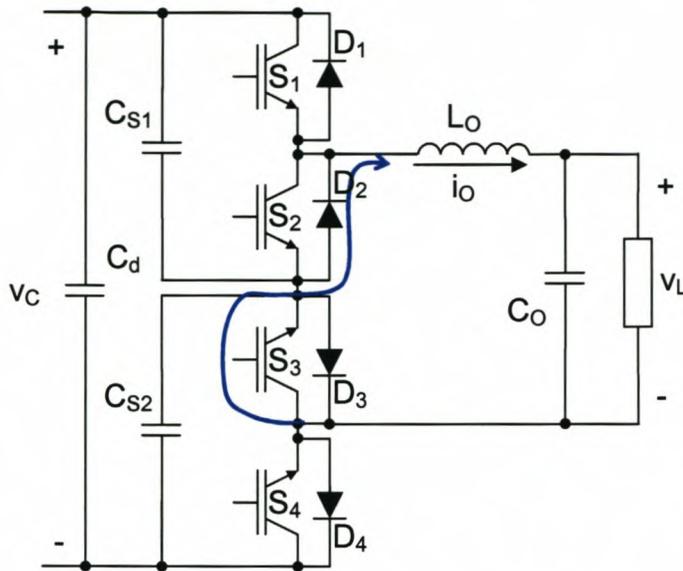
Figure 4-14: Fault current path with positive i_O

During the negative half-cycle the current will be flowing through S_2 and D_3.

As mentioned above, if a conventional DC-to-AC converter goes into an over-current condition all the switches are turned off and the diodes carry the relatively large fault current. In this case some of the switches have to carry this fault current. This implies that the switches must be rated for fault currents.

Similarly if the power to the gate-drive circuits were to fall away, the stored energy goes to the snubber capacitors. An external protection device is now needed to protect the converter until the breaker can be opened. Such a device is a metal oxide viristor (MOV) and Figure 4-15 shows how they are connected to the converter.
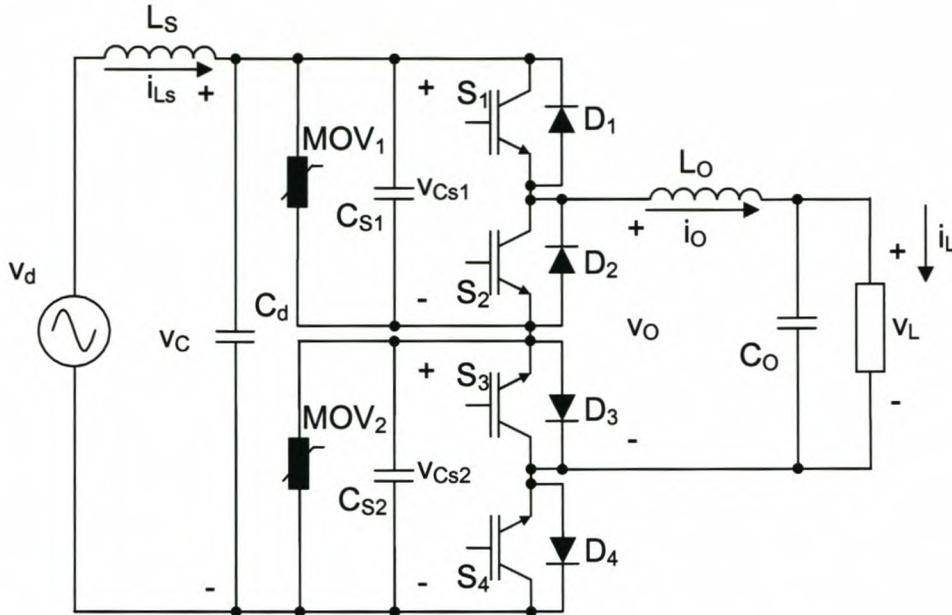
Figure 4-15: Converter with MOVs added

If the voltage over the snubber capacitors becomes too high, the resistance of the MOV will drop. With this drop, a path for the current is created and the converter is saved. The average response time of a MOV is less than 25 ns.

4.2 Synthesis and design

Converter rating	16 kVA
Input voltage range	$230\ V_{RMS} - 422\ V_{RMS}$
Output voltage	$230\ V_{RMS}$
Filter inductor current ripple	30%
Filter capacitor voltage ripple	5 V
Maximum ambient temperature	40 °C

Table 4-4: Converter specifications

In this section the design of the converter will be discussed. Table 4-4 gives the converter's specifications and the design is based on these values. Equations (4-1) and (4-2) give v_L and i_L, which is the output voltage and output current, respectively. This voltage is important and must be kept constant by

the converter. Equation (4-55) is a repeat of Equation (4-1) with its desired values.

$$v_L = V_L \sin(\omega_1 t)$$
$$= 325 \sin(2\pi 50 t) \tag{4-55}$$

The input voltage, v_C, can vary between 230 V_{RMS} and 345 V_{RMS}. This means that Equation (4-5) can be rewritten as in Equation (4-56).

$$v_C = V_C \sin(\omega_1 t)$$
$$325 \sin(2\pi 50 t) \leq v_C \leq 597 \sin(2\pi 50 t) \tag{4-56}$$

The rating of the converter is 16 kVA and this means that, with a maximum load, i_L can be computed. Figure 4-16 shows how the converter can be represented as a transformer with the turn's ratio equal to 1/D. Figure 4-17 shows the converter with the external circuits added.
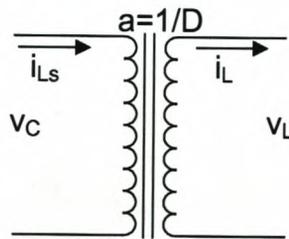
Figure 4-16: Simplified converter
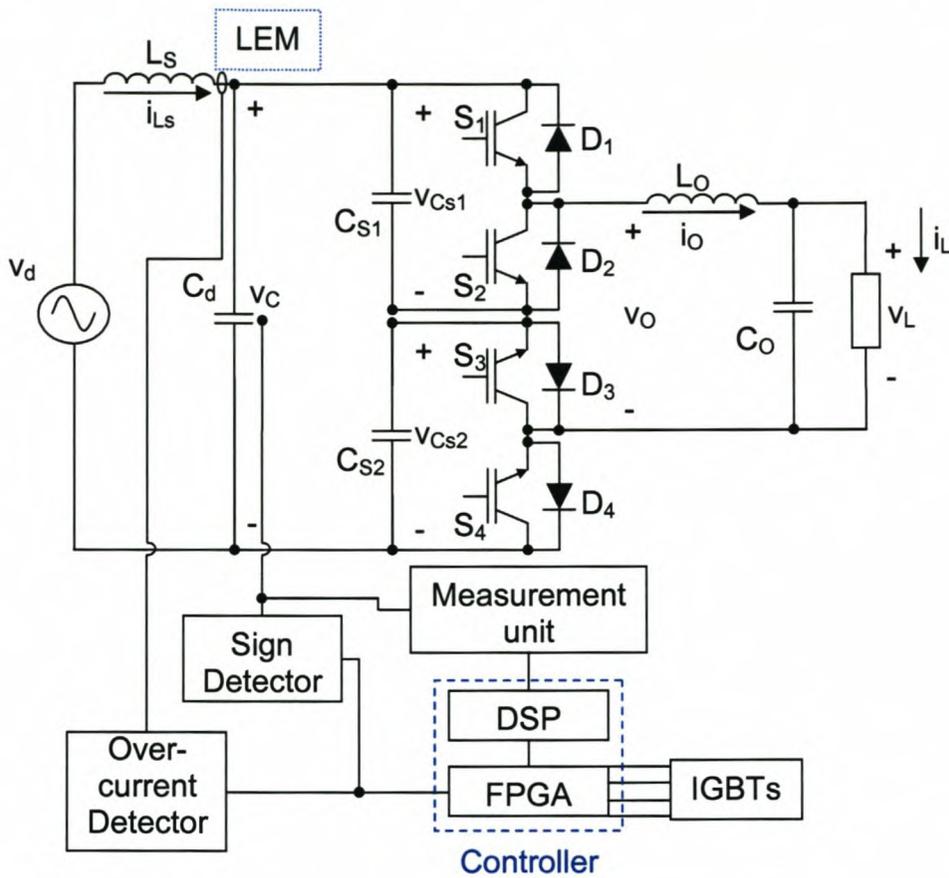
Figure 4-17: Block diagram of controller and measurement components with converter

Table 4-5 gives the RMS values of the input and output, voltages and currents as well as the load resistance.

D	v_{Ls} (V_{RMS})	i_{Ls} (A_{RMS})	v_L (V_{RMS})	I_L (A_{RMS})	R (Ω)
1	230	70	230	70	3.29
0.55	422	38	230	70	3.29

Table 4-5: Input and output, voltages and currents

4.2.1 Switching components

With the currents and voltages calculated above the maximum ratings for the switches can be obtained. The maximum voltage that the switches have to handle is equal to the maximum input voltage and in this case it is 597 V.

The maximum current that the switches will have to conduct is equal to the peak value of i_L with the ripple included. Here there are two values to be considered, the one with D = 1 and the other with D = 0.55. The last duty ratio is obtained by dividing the desired output voltage, 230 V_{RMS}, with the maximum input voltage, 422 V_{RMS}. Since the load resistance is constant, 3.29 Ω, and the output voltage is constant, the inductor current will be constant regardless of the input voltage and the duty ratio. The ripple on i_O is designed to be 30% of the peak current. Table 4-6 shows the values. It should be noted that the ripple component will become smaller as the duty ratio increases and thus the peak current will be smaller.

Input voltage (V_{RMS})	The duty ratio, D	$I_{O(max)}$ (A)
230	1	99 (no ripple)
422	0.55	129 (30% ripple)

Table 4-6: Maximum current through switches

When D = 1 there is no ripple on i_O as can be seen from Equation (4-34), repeated below.

$$\Delta I_O = \frac{1}{L} D(1-D) V_c T_S \sin \omega_1 t$$

The switching modules chosen are the "SKM 200 GB 122 D" IGBT module, manufactured by Semikron. These modules have a peak voltage of 1200 V and a current of 200 A. Table 4-7 gives some of the maximum ratings of the IGBT and Table 4-8 gives some of the characteristics of the IGBT and diode [41].

Symbol	Values
V_{CES}	1200 V
I_C	200 A
V_{GES}	±20 V
P_{tot}	1250 W

T_j	-40 … +150 °C

Table 4-7: Absolute maximum ratings

Symbol	Values
V_{CEsat}	3.7 V
V_{ECsat}	2.5 V
E_{on}	24 mWs @ 600 V V_{CC} and 150 A I_C
E_{off}	17 mWs @ 600 V V_{CC} and 150 A I_C

Table 4-8: Characteristics

The values given above together with those obtained from the module's data sheets can be used to compute the losses in the system. Equations (4-13) to (4-16), (4-19) and (4-21) are used here.

V_C	230 V	278 V	325 V	373 V	420 V
D	1.0000	0.8273	0.7077	0.6166	0.5476
P_{cond} (S_1)	116.439 W	96.335 W	82.403 W	71.799 W	63.764 W
P_{cond} (S_3)	0 W	20.105 W	34.036 W	44.640 W	52.675 W
P_{cond} (D_4)	78.675 W	65.091 W	55.678 W	48.513 W	43.084 W
P_{cond} (D_2)	0 W	13.584 W	22.997 W	30.162 W	35.591 W
P_{switch} (S_1)	81.046 W	97.960 W	114.522 W	131.436 W	147.997 W
P_{switch} (S_2)	81.046 W	97.960 W	114.522 W	131.436 W	147.997 W
P_{tot}	714.413 W	782.069 W	848.316 W	915.971 W	982.218 W
Efficiency	95.75%	95.36%	94.99%	94.61%	94.24%

Table 4-9: Losses in the system

The total losses over one 50 Hz cycle are given in Equation (4-21) and are also given in Table 4-9 for five different input voltages. The efficiency of the converter has also been computed for later comparison with the experimental setup.

4.2.2 Gate-drive circuits

The driver used to drive the switches is Mitsubishi's "M57962L". This IC has the capability to detect a fault condition, but in this application this capability will not be used. By using the recommended circuit in the data sheets, with an isolated power supply from the base of the gate-drive circuit. The circuit of the power supply is given in Appendix A.

The gating signals from the controller are supplied to the gate-drive circuit by means of a fibre optic cable. This reduces the risk of faulty switching due to Electro Magnetic Coupling (EMC). Figure 4-18 shows a block diagram of the gate-drive circuit. In this diagram the different signals can be seen.
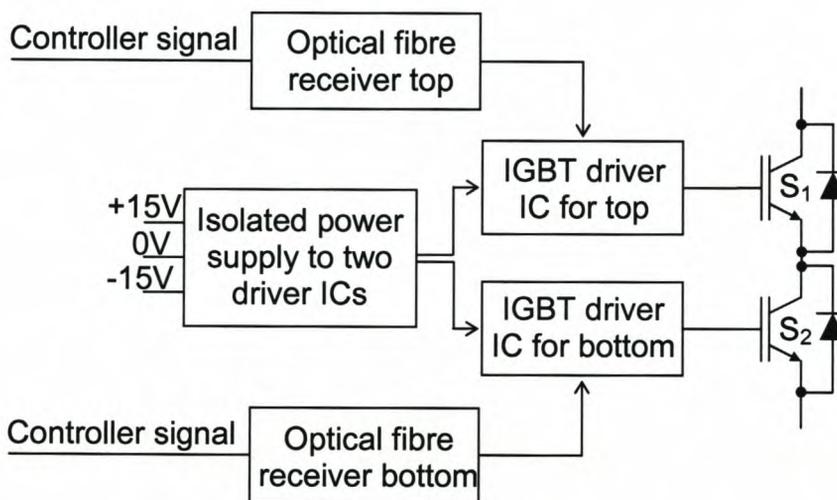
Figure 4-18: Block diagram of gate-drive circuit

4.2.3 Output filter

The values for the output filter components can be computed by using Equations (4-34) and (4-38).

$$L = \frac{V_c T_s}{\Delta I_{O(max)}} D(1 - D)$$

$$= \frac{597\left(200\times10^{-6}\right)}{99(0.3)}0.55(1-0.55)$$
$$= 995\,\mu H$$

(4-57)

The ripple on the voltage is chosen as $\Delta V_{L(max)}$ = 5 V.

$$C = \frac{T_S \Delta I_{O(max)}}{8\Delta V_{L(max)}}$$
$$= \frac{200\times10^{-6}(99)(0.3)}{8(5)}$$
$$= 148.5\,\mu F$$

(4-58)

The corner frequency of the output filter is f_C and Equation (4-59) shows this value.

$$f_C = \frac{1}{2\pi\sqrt{LC}}$$
$$= \frac{1}{2\pi\sqrt{\left(148\times10^{-6}\right)\left(995\times10^{-6}\right)}}$$
$$= 414.04\,Hz$$

$$\text{or} \quad = \frac{1}{\sqrt{\left(148.5\times10^{-6}\right)\left(995\times10^{-6}\right)}}$$
$$= 2602\,rad/s$$

(4-59)

If this is now compared with the Fourier series representation of Figure 4-9, it can be seen that the filter is sufficient for the purpose.

The inductor and capacitor will be obtained from commercial suppliers. The inductor will have to be made especially for this application.

4.2.4 Protection

The fault conditions were discussed in section 4.1.5. It has been established what is to happen if a fault were to occur, but the method of detection still needs to be explained.

An analog circuit will be used to detect an over-current from the current probe. This current probe or current transducer is a LEM "LA 205-S"; this is shown in Figure 4-17. The data sheet for the device can be found on the LEM web-site [35]. The conversion ratio of this module is 1:2000. If the maximum allowable filter inductor current is 150 A then the current delivered by the LEM is 75 mA. The over-circuit detection circuit is shown in Figure 4-19.

Component	Delay time	Source of information
LM 311	200 ns	[38]
DS75451	31 ns	[37]
HFBR1521	80 ns	[34]
FPGA	27.7 ns	Simulation (Max+plusII)
HFBR2521	4 ns	Estimated – Diode delay
Optic fiber	140 ns @ 0.5 m	[34]
M57962L	2.5 μs	[36]

Table 4-10: Table of delay times of over-current protection circuit

The total time delay for this circuit is sum of all the components' delay times. This is given in Table 4-10 and the total is 3.207 μs. The optical components appear twice in the final sum because there are two sets of fibres from the LEM sensor to the drivers. The driver's delay has also been taken into account. In the estimation of the total time delay, only the ICs have been taken. Measurements have been taken from the experimental setup and the delay was found to be 13.6 μs. The measured delay is longer than the computed delay. There are a variety of reasons for this difference; to begin with the optic fibre's delay is given for a length of 0.5 m and the experimental setup's fibres are not all of the same length; some are longer than 0.5 m. The

LEM unit's delay has not been taken into account; this delay will be less than 1 μs [35]. The combined delays of all the passive components and circuits have not been neglected.
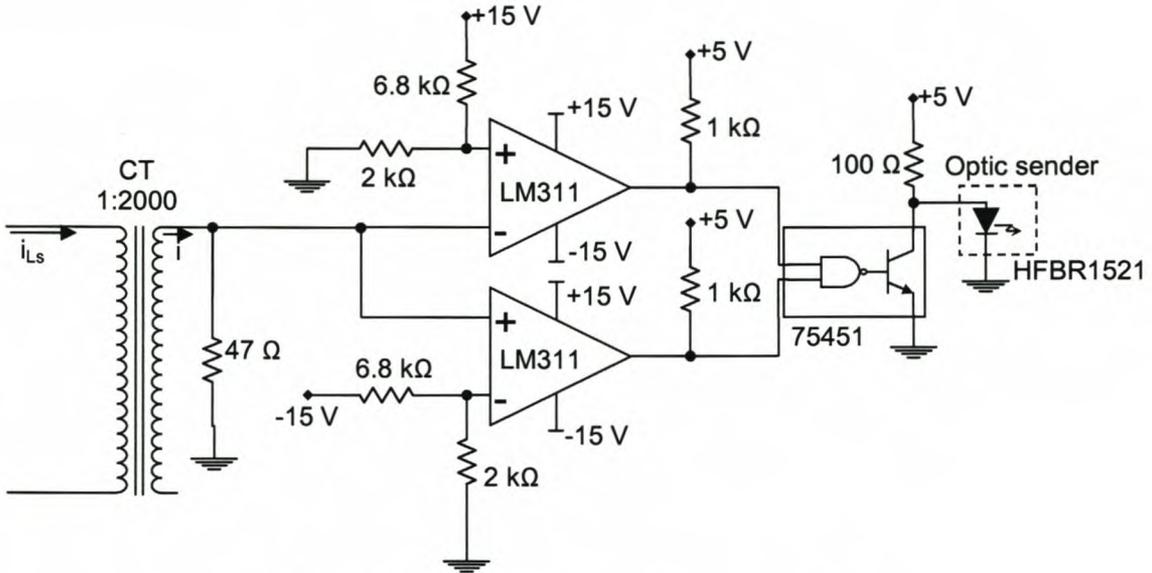
Figure 4-19: Over-current detection circuit

The circuit is relatively simple to explain. A resistor is connected to the output of LEM. With a current of 75 mA and a resistance of 47 Ω, a voltage of 3.5 V is measured over the resistor if a fault were to occur. The two comparators then compare the voltage measured with a set reference voltage of ±3.5 V. From there the output of the comparators is sent through a logical nand gate and the current is amplified with the DS75451. This IC then drives the fibre optical sender.

4.2.5 Voltage detection

As was stated before, it is very important to detect the sign of the voltage correctly. To prevent EMC from interfering with the circuit and its output signal, a metal casing, a Faraday cage, was made to house the circuit and the output was sent to the controller board's FPGA via an optic fibre. Figure 4-20 shows the circuit for this sign detector and, as can be seen, v_C is used as

indicator of the sign. The detector works on the simple principle of the on-state voltage of two diodes and a comparator is used to set the output voltage so that it can be sent through the optic fibre. The delay time from sign change to the IGBTs is 3.19 μs.

Table 4-11 shows the components of the sign detection circuit. As with the protection circuit, there are two sets of optical components and the driver circuit is taken into account.

Component	Delay time	Source of information
LM 311	200 ns	[38]
HFBR1521	80 ns	[34]
FPGA	39.1 ns	Simulation (Max+plusII)
HFBR2521	4 ns	Estimated – Diode delay
Optic fibre	140 ns @ 0.5 m	[34]
M57962L	2.5 μs	[36]

Table 4-11: Delay times of sign detector circuit
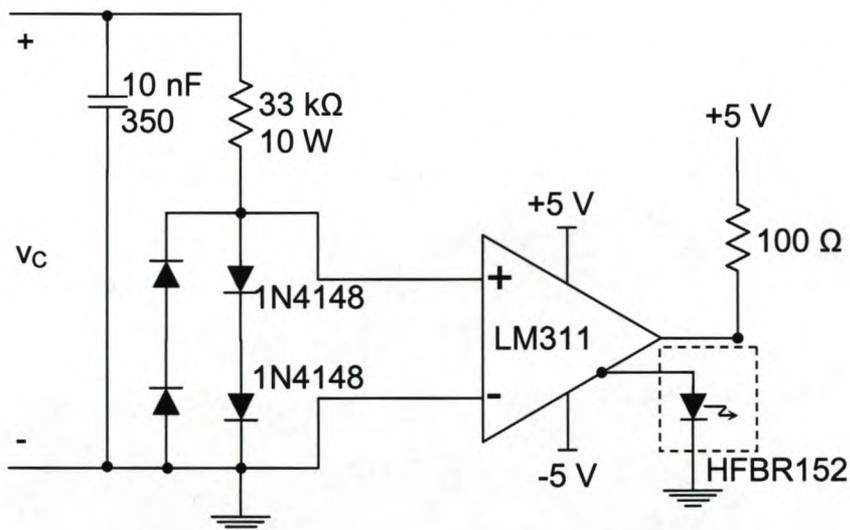
Figure 4-20: Sign detection circuit of v_C
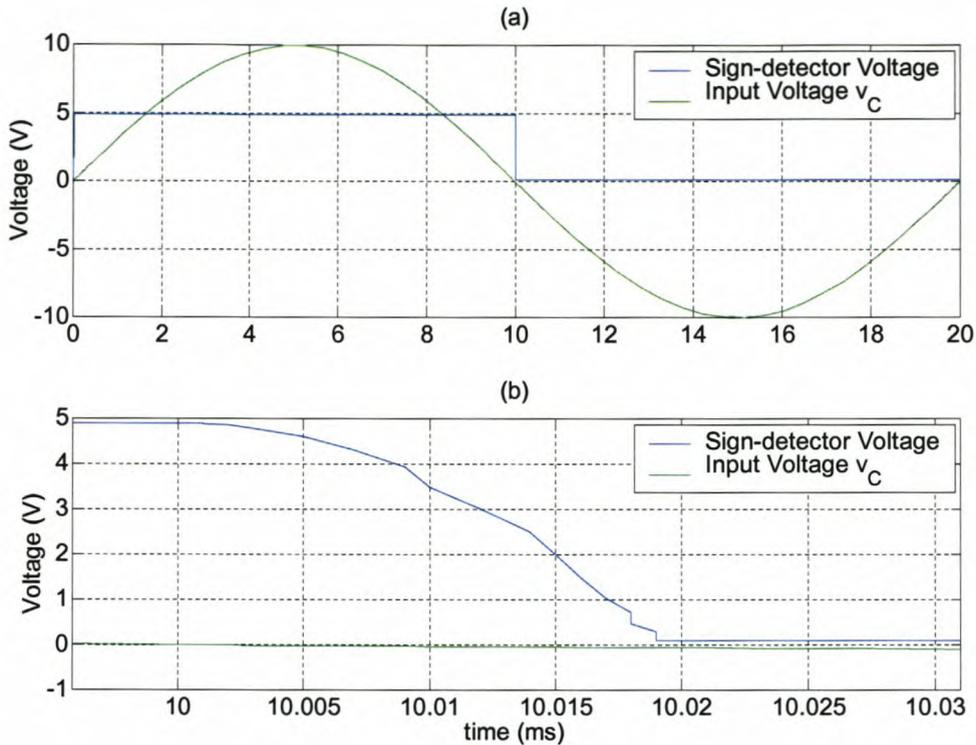
Figure 4-21: Input voltage and sign-detector voltage for (a) one cycle; (b) enlarged zero-crossing

A simulation of this circuit was done in Simplorer and the input voltage versus output voltage of this circuit was ascertained. Figure 4-21 (a) shows one 50 Hz cycle of v_C and the output of the detection circuit. The input voltage v_C has a reduced amplitude for explanation purposes.

Figure 4-21 (b) shows the same voltages as in (a) but the zero-crossing was enlarged. The delay according to the simulation is 18 μs, but this was a simulation with generic components and a more accurate delay time was established with measurements. This measured delay is 75.2 μs and the computed delay is 3.9 μs. The reasons given for this large difference between the measured and computed delays in the protection circuit apply to the sign-detection circuit. Another reason for the difference is that the delays measured are the longest delay taken from a number of measurements.

4.2.6 Snubber capacitors

The manufacturer of the IGBT modules suggests using a snubber capacitor in the micro-Farad range. That provides a good first estimate, but there are two more restrictions on the capacitor's size. The first consideration is what happens during the dead time. Figure 4-22 (a) shows the current path during the positive half-cycle with the current positive and the IGBTs are both off for the 3 μsec dead time and (b) shows the current path for negative load current. Figure 4-22 (c) and (d) show the current paths during the negative half-cycle's dead time with the current positive and negative, respectively.
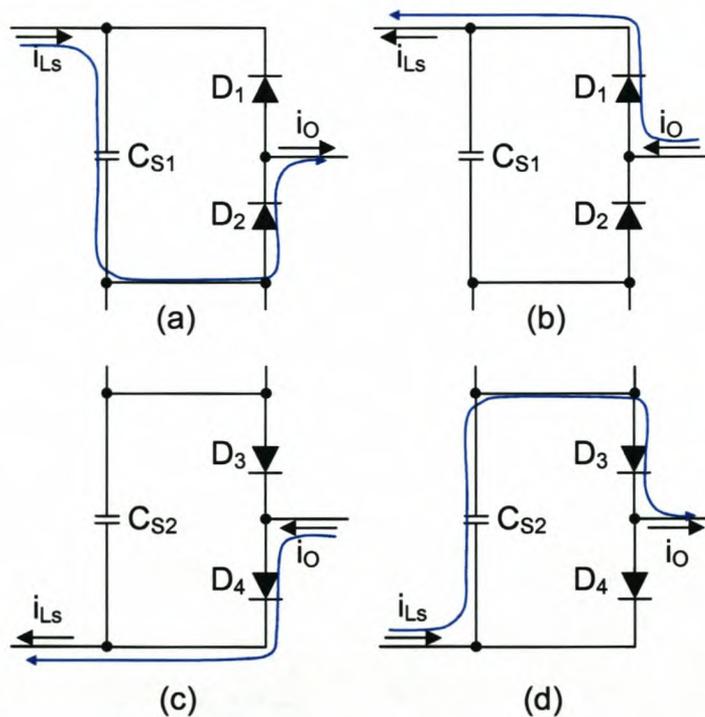
Figure 4-22: Current paths during dead time with (a) v_c+, i_o+; (b) v_c+, i_o-; (c) v_c-, i_o+; (d) v_c-, i_o-;

The current through the capacitor is given in Equation (4-60) and the capacitance can be written as in Equation (4-61). The dead time is represented as ΔT and ΔV is the maximum that the voltage can rise over the capacitor, which is equal to the maximum voltage the IGBT can handle (1000 V with safety) minus the maximum bus-voltage (597 V $\approx$600 V).

$$i_{O\,max} = C\frac{\Delta V}{\Delta T} \qquad\qquad\qquad \text{(4-60)}$$

$$C = i_{O\,max}\frac{\Delta T}{\Delta V} \qquad\qquad\qquad \text{(4-61)}$$

$$= 129\frac{3\times10^{-6}}{(1000-600)}$$

$$= 0.968\,\mu F$$

When the voltage goes through the zero crossing there will be a short time in which the switches might all be off. During this stage it is important to limit the voltage and current rise. It is also important to note that the zero-crossing dead time is the same length as the ordinary dead time. This implies that the voltage and current rise will be the same during the zero-crossing and the dead time.

The next consideration is the fault conditions. The IGBT phase arms each have a MOV, a NTE-2V480 [39], over them for protection (see Figure 4-17). The average delay time for a MOV is less than 25 nsec. The current flows in the same paths here as they do in Figure 4-22. The fault current is set at 150A and the maximum voltage to be seen by the capacitor is 1000 V. The first thing to find in this case is the rise in current ΔI from when the fault current is first detected to the MOV's activation. The converter's over-current protection will be activated if the input current i_{Ls} is 150 A. The time it takes the converter to switch off is the ΔT in Equations (4-62) and (4-63). This is the 13.6 μs measured. The voltage over the inductor will determine the current rise and the worst case here will be if the input is at maximum (597 V) and the output is at minus its maximum (-325 V). The voltage over the inductor is then 992 V. It must be remembered that this is the absolutely worst case and will most likely never happen, because it implies that the input voltage and output voltage are 180° out of phase with one another.

$$v = L_O\frac{\Delta I}{\Delta T} \qquad\qquad\qquad \text{(4-62)}$$

$$\Delta I = v \frac{\Delta T}{L_O} \tag{4-63}$$

$$= 992 \frac{13.6 \times 10^{-6}}{995 \times 10^{-6}}$$

$$= 13.56 A$$

Using Equation (4-61) with $i_{Omax}=150+\Delta I$ the capacitance is computed in Equation (4-64).

$$C = i_{O\,max} \frac{\Delta T}{\Delta V} \tag{4-64}$$

$$= 163.56 \frac{25 \times 10^{-9}}{400}$$

$$= 10.22 nF$$

The capacitance used must be larger than the two computed here. For a good safety margin a 2 μF capacitor was chosen for the snubbers; these capacitors can be mounted directly on the IGBTs.

4.2.7 Digital controller

The controller of this converter is based on the PEC31 digital signal processing board [13]. This controller contains a TMS320C31 digital signal processor as well as a FLEX10K FPGA. A number of analogue to digital and digital to analogue converters are also included. Two re-configurable digital ports are also provided; one of these will be used for the input from the error circuit and the signal-detection circuit. The DSP is mainly used for high-level control functions, while high-speed low-level control functions are implemented in the FPGA.

The decision as to which of the switches are to be open is made in the FPGA. Implemented in the FPGA's programming are two PWM blocks. An addition to this is a block which detects the sign detector's signal as well as the fault signal and a reset. In this block the PWM signals are just let through or

blocked depending on the situation. The code for this is given in Appendix B and its flow diagram is shown in Figure 4-23.
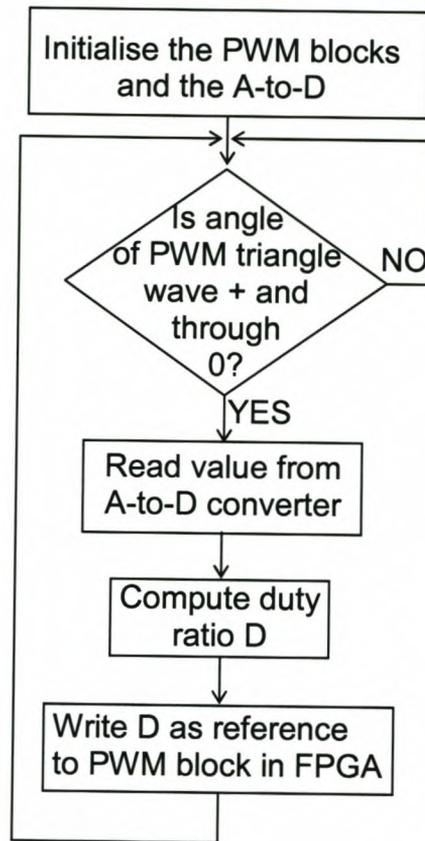
Figure 4-23: Generic flow diagram of controller code

In the DSP the duty ratio is computed and the PWM blocks are initialised and controlled. There are three different ways to obtain the duty ratio:

1. Take sampled measurements of one 50 Hz cycle of v_C and compute the RMS of the signal at that time, Equation (4-39). Dividing the required value of the output voltage (230 V) with the computed voltage gives the duty ratio.

$$V_{RMS} = \sqrt{\frac{1}{N} \sum_{n=0}^{N} V_{measure}^2}$$ (4-65)
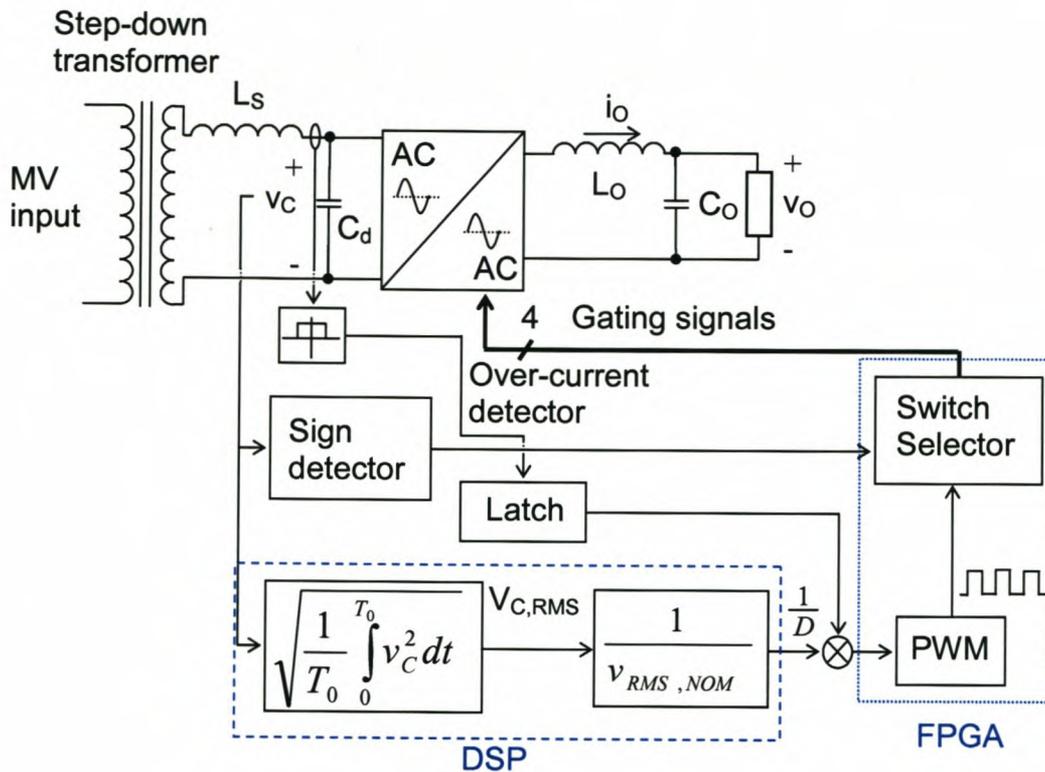
Figure 4-24: Block diagram of the RMS control

Figure 4-24 shows the block diagram of this control method. The parts implemented in the DSP and FPGA are indicated with boxes. This is a feed-forward system. The code implemented in the DSP can be found in Appendix B.

2. Construct a sinusoidal reference signal in the DSP at 50 Hz in steps of 200 μsec, 5 kHz switching frequency, and divide the reference with a measured signal of v_C. This will give the duty ratio every switching period.
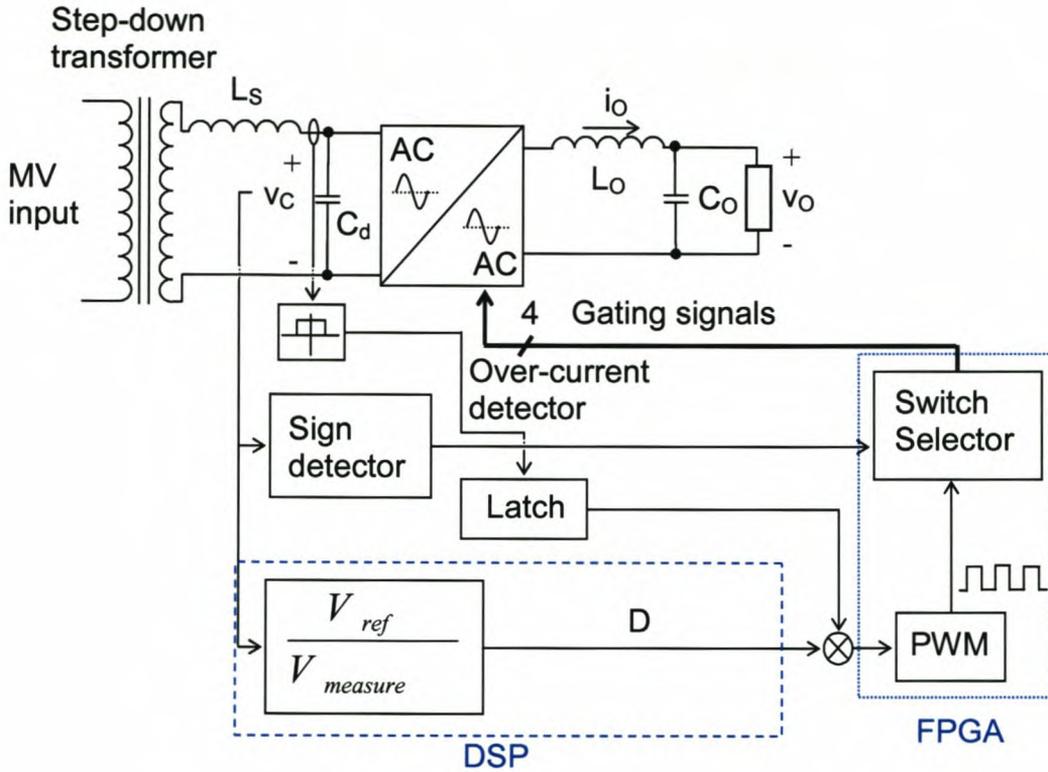
Figure 4-25: Block diagram of direct duty ratio control

Figure 4-25 gives the block diagram of this method. The code implemented to obtain this can be found in Appendix B.

3. Perform closed-loop control by adding a digital P controller in the DSP. Figure 4-26 shows the block diagram of this type of controller, the code used in the DSP can be found in Appendix B.

The design of the closed-loop control is rather more complex than the other control methods. To be able to design this control, the transfer function of the converter will be needed. Using a method developed by Middlebrook and Cúk and described in [5] the transfer function can be found.

Because the converter's positive and negative half-cycle operation is symmetrical, only the one half-cycle will be considered.
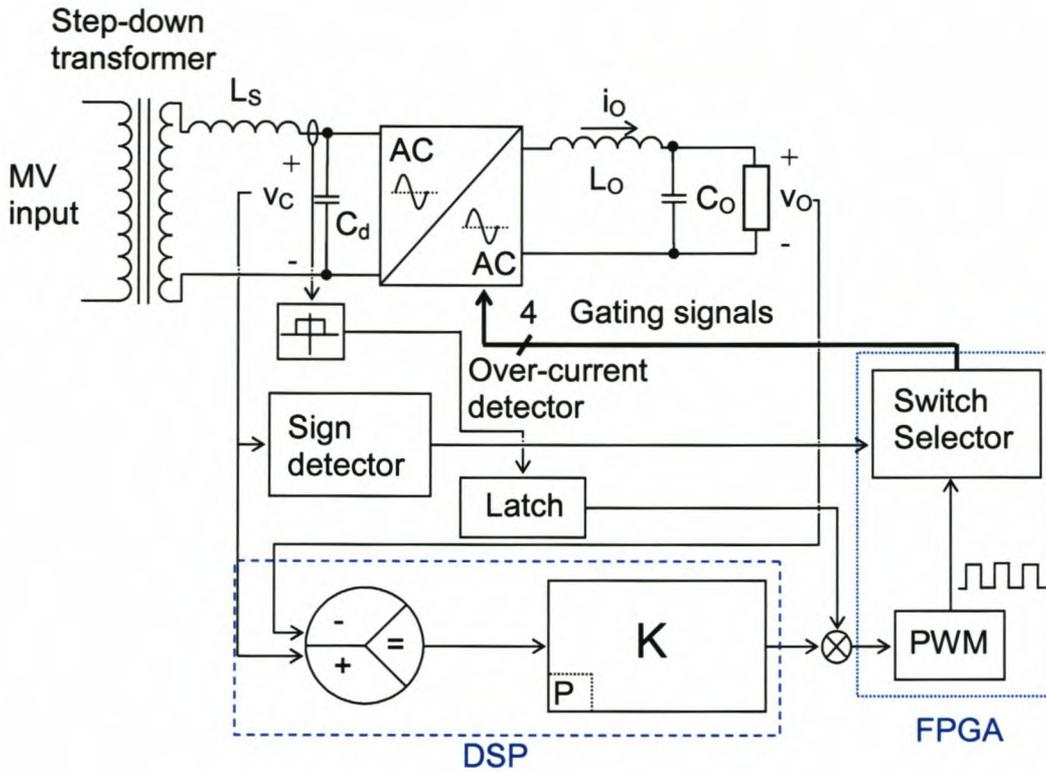
Figure 4-26: Block diagram of PI controller

Figure 4-27 (a) shows the circuit diagram of the converter and (b) of the figure show the equivalent diagram of converter when S_1 or S_4 is on and (c) is the equivalent diagram when S_2 or S_3 is on. The inductor's resistance is represented by r_{Lo}, the capacitor's series resistance is r_{Co} and R is the load resistance. Using Kirchhoff's voltage law and Figure 4-27 (b) Equations (4-66) and (4-67) are found.

$$-v_C + L_O \dot{x}_1 + r_{Lo} x_1 + R(x_1 - C_O \dot{x}_2) = 0 \qquad \text{(4-66)}$$
$$-x_2 - r_{Co} C_O \dot{x}_2 + R(x_1 - C_O \dot{x}_2) = 0 \qquad \text{(4-67)}$$

Using these equations the state-space model for the converter can be found. This model is given in Equation (4-68).
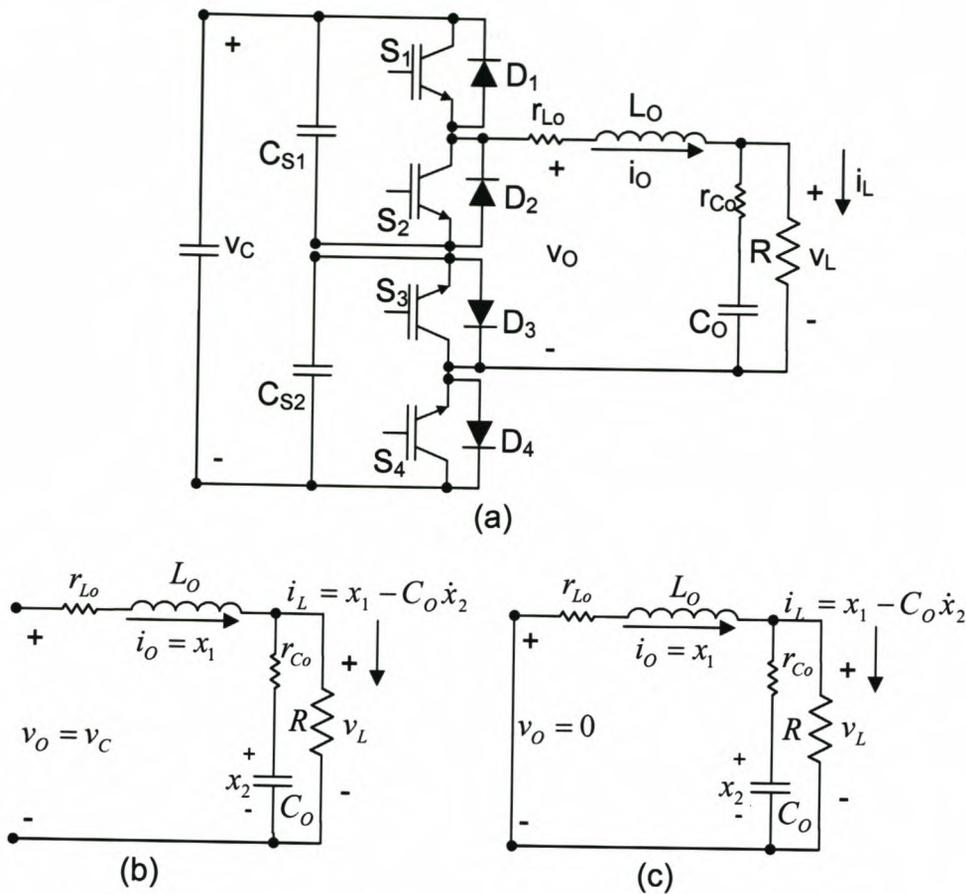
Figure 4-27: Circuit diagram of (a) converter; (b) Stage 1 with S₁ or S₄ on; (c) Stage 2 with S₂ or S₃ on

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_s \end{bmatrix} = \underbrace{\begin{bmatrix} -\dfrac{Rr_{Co} + Rr_{Lo} + r_{Co}r_{Lo}}{L_O(R+r_{Co})} & \dfrac{-R}{L_O(R+r_{Co})} \\ \dfrac{R}{C_O(R+r_{Co})} & -\dfrac{1}{C_O(R+r_{Co})} \end{bmatrix}}_{A_1} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \underbrace{\begin{bmatrix} \dfrac{1}{L_O} \\ 0 \end{bmatrix}}_{B_1} v_C \tag{4-68}$$

From Figure 4-27 (b) and (c) it can be seen that matrix A_1 of Equation (4-68) will be same as matrix A_2 of the second stage and that B_2 will be zero. The C matrix can be found by setting Equation (4-69) into Equation (4-70). This matrix is given in Equation (4-71) and like $A_1 = A_2$ so does $C_1 = C_2$.

$$\dot{x}_2 = \frac{R}{C_O(R+r_{Co})}x_1 - \frac{1}{C_O(R+r_{Co})}x_2 \tag{4-69}$$

$$v_L = R(x_1 - C_O\dot{x}_2) \tag{4-70}$$

$$= \underbrace{\left[\dfrac{Rr_{Co}}{R+r_{Co}} \quad \dfrac{R}{R+r_{Co}}\right]}_{C_1}\begin{bmatrix} x_1 \\ x_2 \end{bmatrix}$$

(4-71)

Usually R >> (r_{Co} + r_{Lo}) and, using this, the matrixes (A, B and C) can be simplified as in Equations (4-72), (4-73) and (4-74).

$$\overline{A} = \begin{bmatrix} -\dfrac{r_{Co}+r_{Lo}}{L_O} & \dfrac{-1}{L_O} \\ \dfrac{1}{C_O} & -\dfrac{1}{C_O R} \end{bmatrix}$$

(4-72)

$$\overline{B} = \begin{bmatrix} \dfrac{1}{L_O} \\ 0 \end{bmatrix}$$

(4-73)

$$\overline{C} = \begin{bmatrix} r_{Co} & 1 \end{bmatrix}$$

(4-74)

Using Equation (4-75) the transfer function as in Equation (4-76) can be found. The transfer function of the PWM is 1 in this case and thus (4-76) is the converter's transfer function.

$$T_p(s) = \frac{\tilde{v}_L(s)}{\tilde{d}(s)} = \overline{C}\left[s\overline{I} - \overline{A}\right]^{-1}\left[\left(\overline{A}_1 - \overline{A}_2\right)\overline{X} + \left(\overline{B}_1 - \overline{B}_2\right)v_C\right] + \left(\overline{C}_1 - \overline{C}_2\right)\overline{X}$$

(4-75)

$$= v_C \frac{\omega_0^2}{\omega_z} \frac{s+\omega_z}{s^2 + 2\xi\omega_0 s + \omega_0^2}$$

(4-76)

$$\omega_0 = \frac{1}{\sqrt{L_O C_O}}$$

(4-77)

$$\omega_z = \frac{1}{r_{Co} C_O}$$

(4-78)

$$\xi = \frac{\dfrac{1}{C_O R} + \dfrac{(r_{Co}+r_{Lo})}{L_o}}{2\omega_0}$$

(4-79)

From Equation (4-79) the damping ratio ξ can be computed and from that the settling time t_S of the converter can be found. The capacitor's resistance was found in its data sheets [31] and is 30 mΩ and the inductor's resistance was

measured to be 70 mΩ. The damping ratio is 0.4108. Equation (4-80) from [2 pp. 126 -131] is used to compute the settling time, which is 4.3 ms. The overshoot M_p is computed with Equation (4-81) and is 0.1861%.

$$t_S = \frac{4.6}{\xi\omega_0} \qquad \text{(4-80)}$$

$$M_p = e^{-\pi\xi/\sqrt{1-\xi}} \qquad \text{(4-81)}$$

An ordinary P controller was designed by means of inspection and it was found that a constant K of 0.3 is needed to ensure stability. Simulations were done and it was determined that the reference voltage in the DSP must be multiplied by 4.33 to obtain the correct output voltage. This value was obtained through simulation.

Figure 4-28 shows the rootlocus plots of the uncompensated system (left) and the compensated system (right). The top graphs are the full plot and the bottom graphs are the area around the poles enlarged. It is obvious that the rootlocus does not change much with compensation. It can be agued that there is no use for compensation then, but the transfer function of the converter as it was computed is not entirely correct. This is because some of the effects of the parasitic components were neglected. The input capacitors and inductors were also not taken into account.
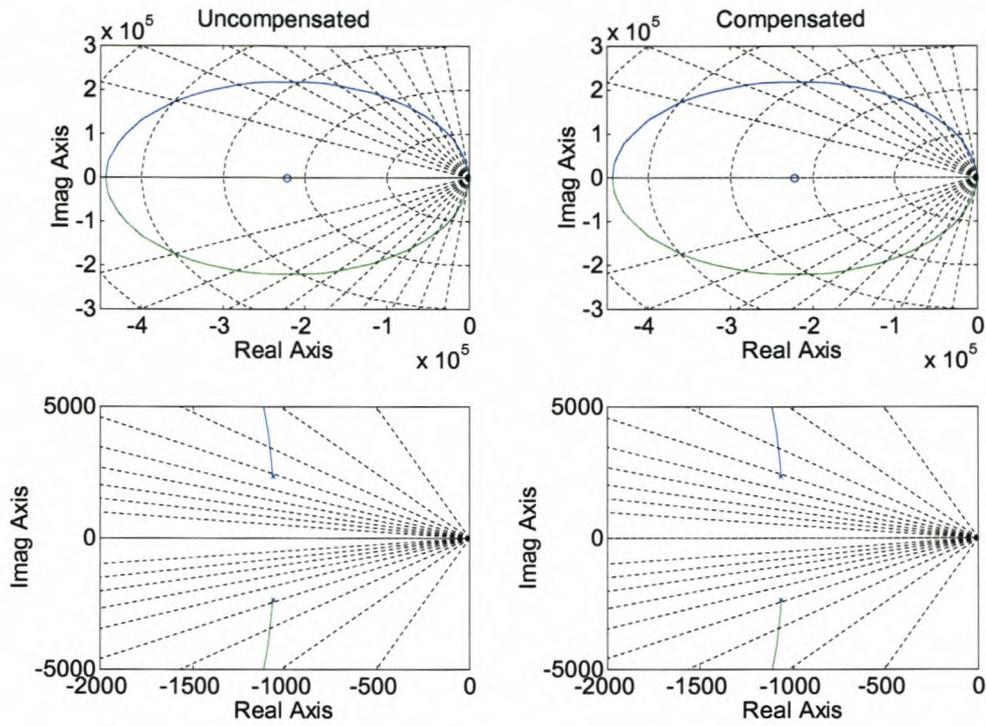
Figure 4-28: Rootlocus plots of the compensated and uncompensated system

Bode Diagrams

Frequency (rad/sec)
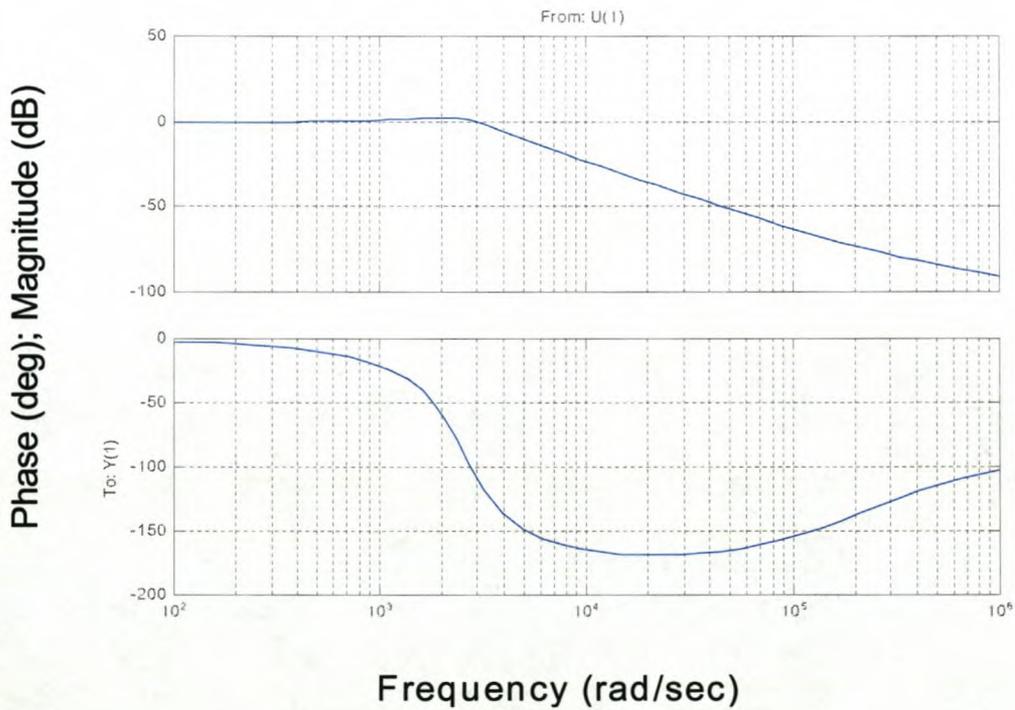
Figure 4-29: Bode plots of the system

Step Response

From: U(1)

Time (sec.)
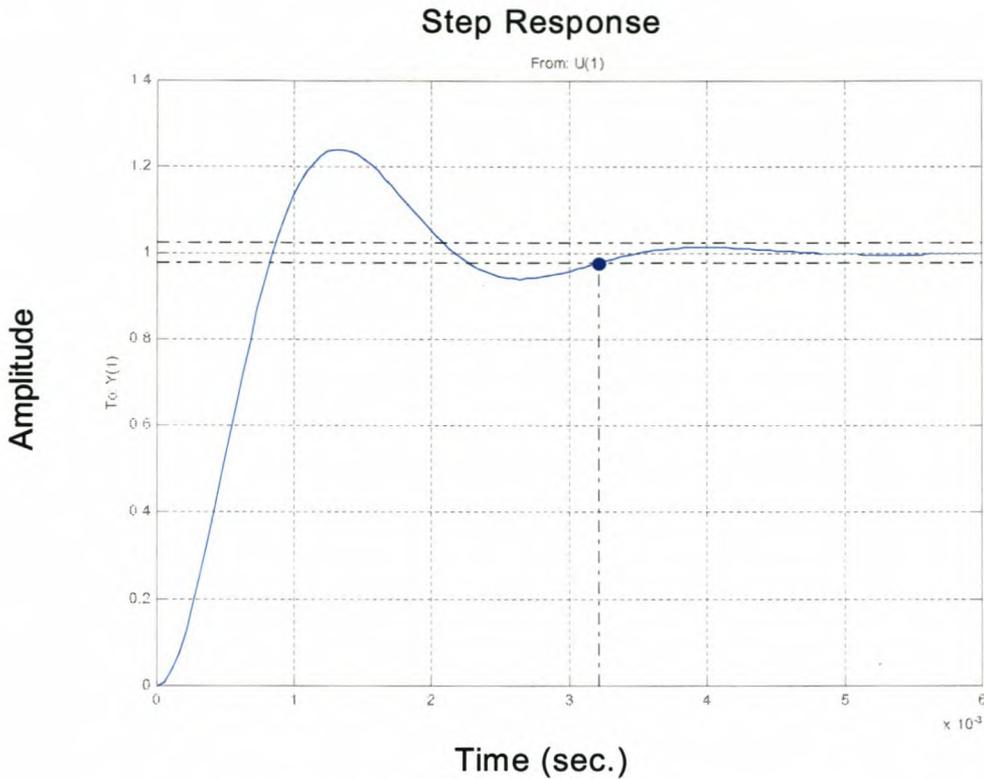
Figure 4-30: Step response of system with settling time

Figure 4-29 shows the bode plot of the compensated system. The frequency response can be seen here. Figure 4-30 shows the step response of the compensated system with the settling time indicated.

The three methods of control in the DSP will be evaluated in the next chapter. Their simulations and experimental results will be discussed.

4.2.8 Startup considerations

The program in the DSP controller has been written in such a way that the switches will all be open at startup until a zero-crossing is detected. This zero-crossing can be either in the positive or the negative direction. Because the switches are open, no current will flow into the load and it is protected against inrush currents. Figure 4-31 shows the converter before switching starts. The current cannot flow into the load via the diodes because they are reversed biased. The snubber capacitor's impedance is large and the current will not

flow through them to the load. Instead the current will flow through the input capacitor C_d. The capacitors used for C_d are designed to handle the currents that will flow through them at the startup.
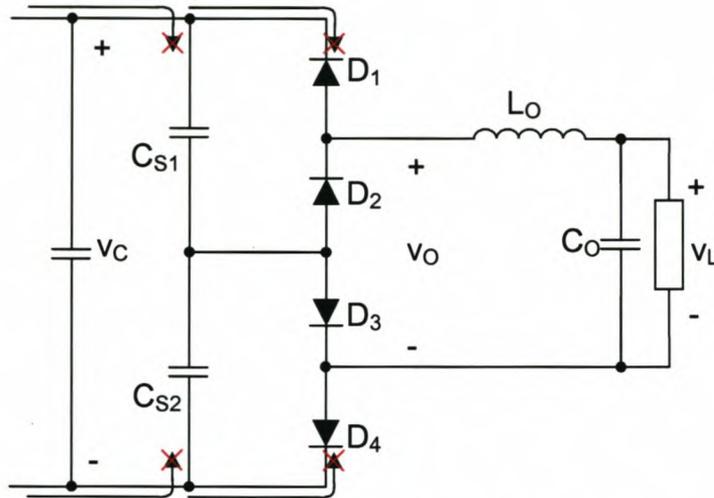
Figure 4-31: Startup circuit diagram

4.2.9 Thermal analysis and heat sink

To be able to design for the correct heat-sink a thermal analysis of the switches must be performed. Equation (4-82) gives the relationship between the junction-to-ambient thermal resistance, $R_{\theta ja}$, the total power loss of one IGBT, P_{tot}, and the maximum junction temperature, T_{jmax}, and maximum ambient temperature, T_{amax}. Equation (4-83) gives the components of $R_{\theta ja}$ [5]. $R_{\theta jc}$ is the junction-to-case thermal resistance, $R_{\theta ch}$ is the case-to-heat-sink and $R_{\theta ha}$ is the heat-sink-to-ambient thermal resistance. The latter of these resistances is the one that determines the type of heat-sink that has to be used.

$$R_{\theta ja} = \left(T_{j\max} - T_{a\max}\right)/P_{tot} \tag{4-82}$$

$$R_{\theta ja} = R_{\theta jc} + R_{\theta ch} + R_{\theta ha} \tag{4-83}$$

Using Equations (4-82) and (4-83) and the values found in the IGBTs data sheets $R_{\theta ha}$ can be computed.

$$
\begin{aligned}
R_{\theta ha} &= \left(T_{j\max} - T_{a\max}\right)/P_{tot} - \left(R_{\theta jc} + R_{\theta ch}\right) \\
&= (150 - 40)/\left(803.82\big/2\right) - (0.1 + 0.038) \\
&= 0.136\,°C/W
\end{aligned}
\tag{4-84}
$$

An appropriate heat sink with this resistance was found and the two IGBT modules were mounted on their own separate heat-sink.

4.2.10   Transformer

The transformer will, as with the inductor, be made by a commercial supplier. The specifications for this 50 Hz single-phase transformer are shown in Table 4-12. The turn's ratio will be such that when the primary voltage is a minimum, then the secondary voltage will be nominal, 230 V_{RMS}. At first it was thought that a standard transformer would be used in this application and since it will supply a 16 kVA load, the transformer will be 16 kVA. From this the secondary current was computed to be 70 A. The transformer used in the end is not a standard one and its rating has changed to accommodate the changes in the secondary voltage. The transformer rating is defined as (nominal secondary voltage) times (secondary current). The nominal secondary voltage is 379.31 V and the current is 70 A.

Power rating	26.55 kVA
Primary voltage range	6.6 – 12.1 kV
Secondary voltage range	230 – 422 V
Turns ratio (V_P/V_S)	29
Primary current	2.4 A
Secondary current	70 A

Table 4-12: Transformer specifications

4.3 Summary

In this chapter the converter was designed. The different components were designed and analysed. To start with, the equations for the losses were found and thus an equation for the total losses was found. The equations for the output filter components were derived and the voltage spectrum for both the AC-to-AC converter and the DC-to-AC converter was obtained. The fault-handling capability of the converter was then analysed.

After the analysis was completed, the design could be finalised. The switches' operating conditions were defined followed by a short description of the driver circuits. The output filter was designed and the circuits for the protection and sign detection were discussed. The snubber capacitors were designed and the control methods discussed. The start-up conditions were considered next, followed by the thermal analysis and the heat-sink design. The chapter was concluded with the transformer specifications.

In the next chapter the simulations and experimental results will be presented and discussed.

Chapter 5

Experimental results

5 Experimental results

In this chapter the converter will be evaluated. The converter was constructed according to the design specifications set out in the previous chapter. The values of the output filter components were changed slightly, because of the availability of the components. The inductor, L_O, is 1.2 mH and was designed to be 995 μH. This inductor is an air-core inductor so that the cores do not saturate and cause a non-linearity in the system. This type of inductor with this size is physically large and care must be taken that the inductor's electric field does not interfere with the operation of the converter. The inductor is made up of three smaller inductors in series. The capacitor is 150 μF, almost the designed value 148.5 μF.

The converter was tested with a purely sinusoidal input voltage. It was found that the input capacitor C_d and the variac's leakage inductance were resonating. This caused resonant frequencies at the third, fifth and seventh harmonic of the 50 Hz input voltage. It was found that by increasing the input capacitance and adding a resistor in parallel with the capacitor, the resonance was greatly reduced. The resistor now added the necessary damping to the input system. The input capacitor is 200 μF and the resistor is 37.7 Ω. The maximum current that the variac can deliver is 40 A and this leads to a load of 18 Ω. The load is almost purely resistive.

Figure 5-1 is a photo of a part of the experimental setup. Figure 5-2 shows the circuit diagram of the converter and the part in the block represents the components in Figure 5-1, except the driver circuits. The numbers in the photo correspond to the numbers in the diagram.
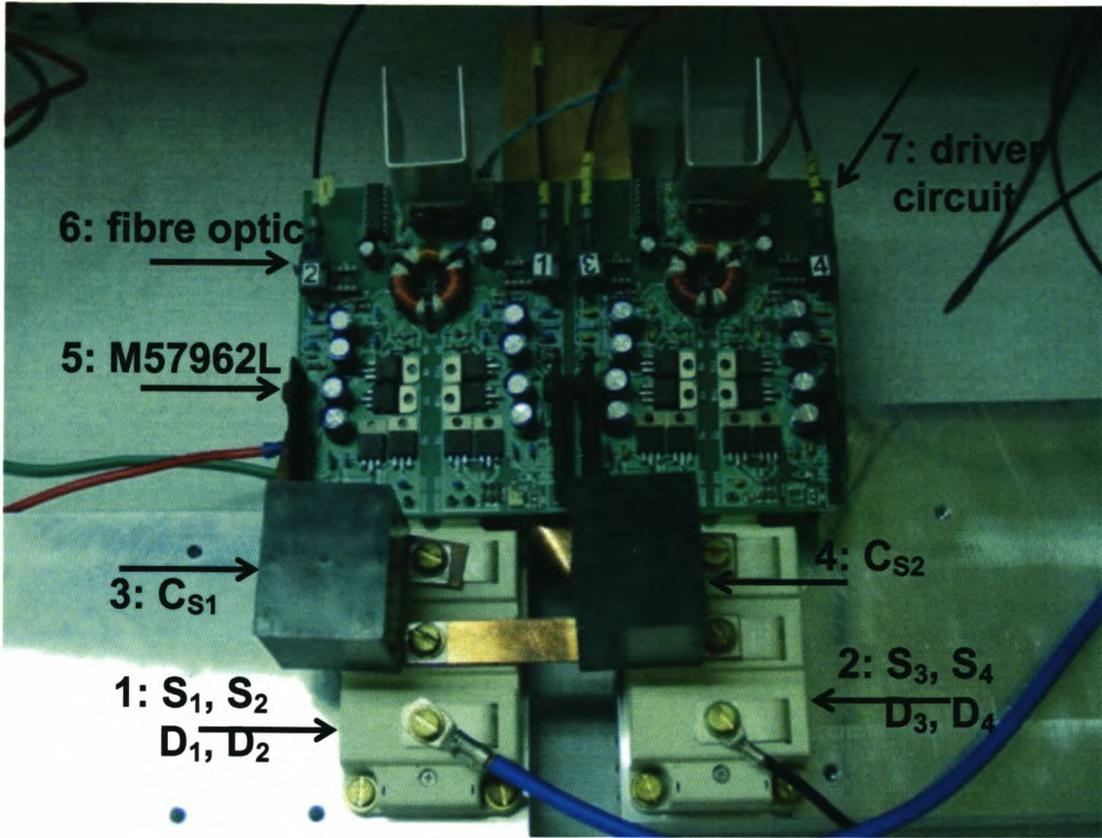
Figure 5-1: Photo of converter
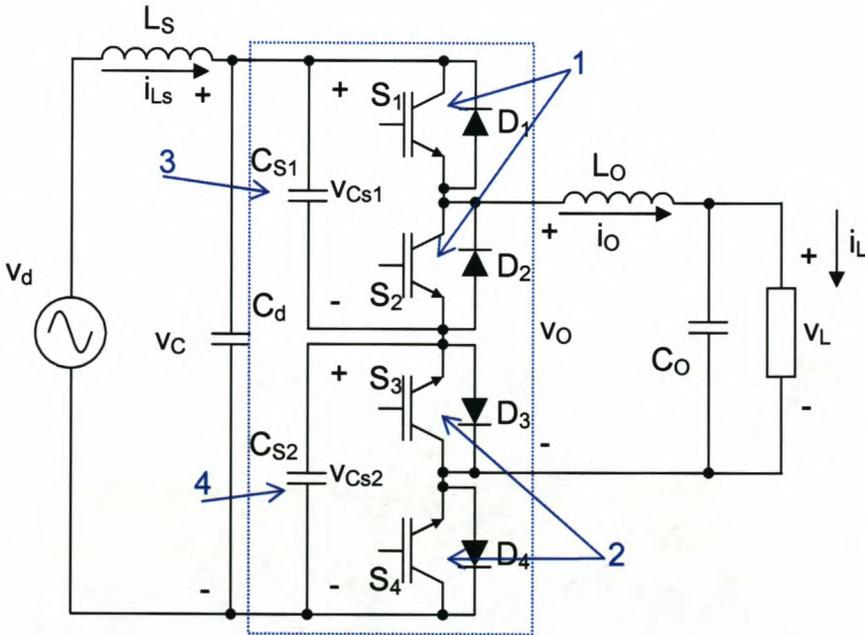
Figure 5-2: Circuit diagram of converter
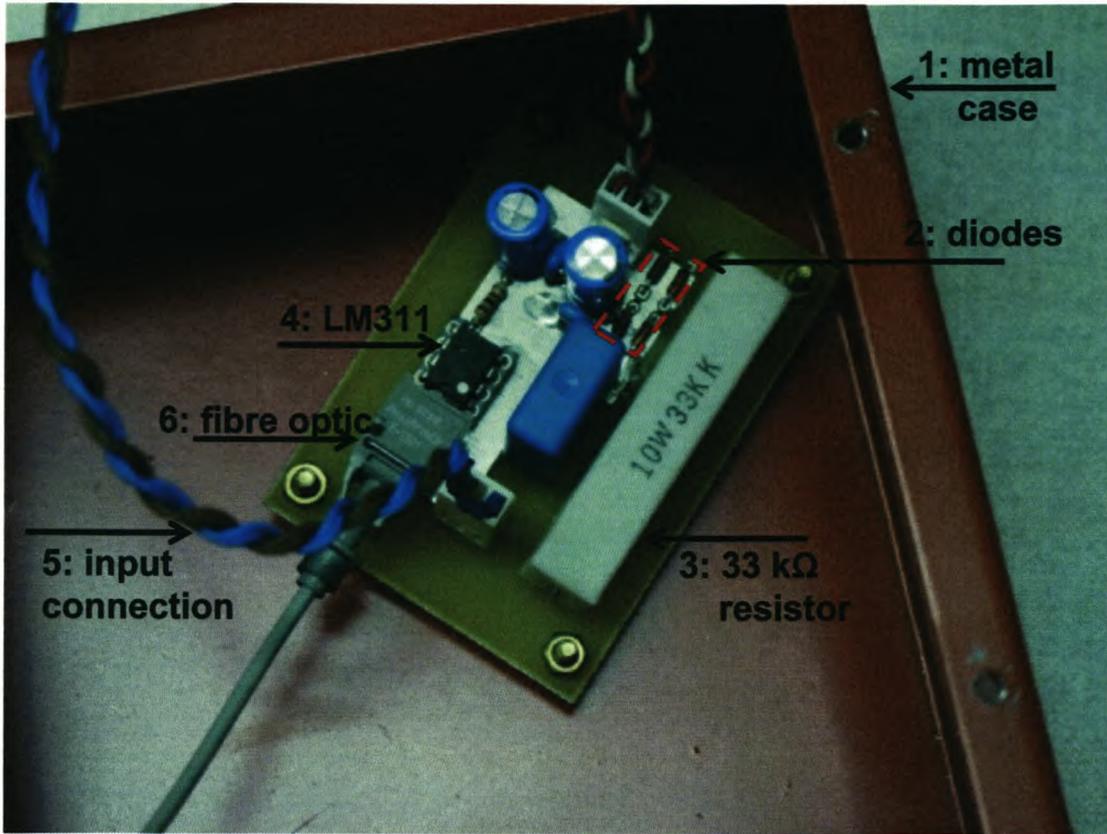
Figure 5-3: Photo of sign detection circuit
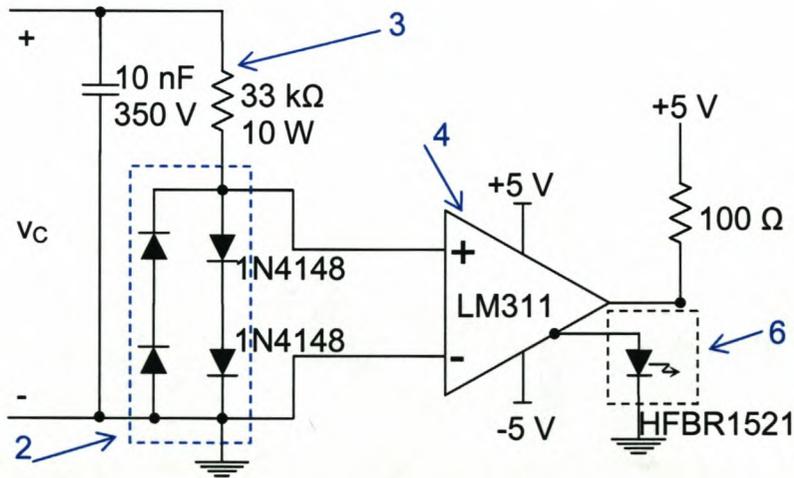
Figure 5-4: Circuit diagram of sign detection circuit

Figure 5-3 is a photo of the sign-detection circuit with Figure 5-4 its circuit diagram. The metal case is intended to prevent EMC.
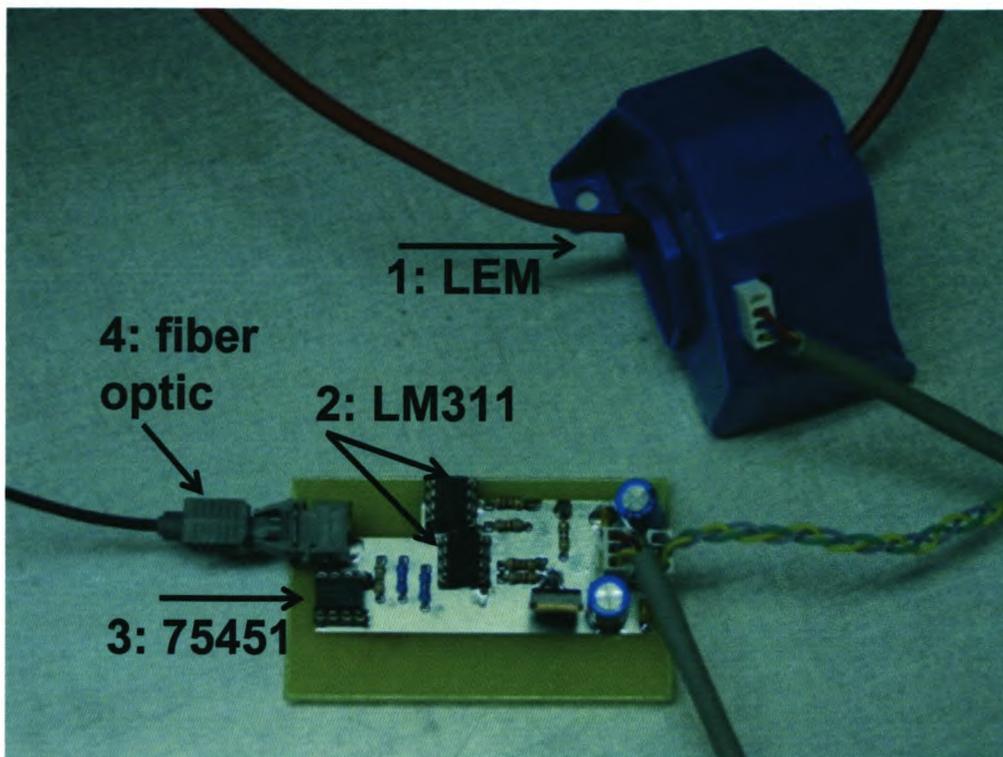
Figure 5-5: Photo of over-current detector
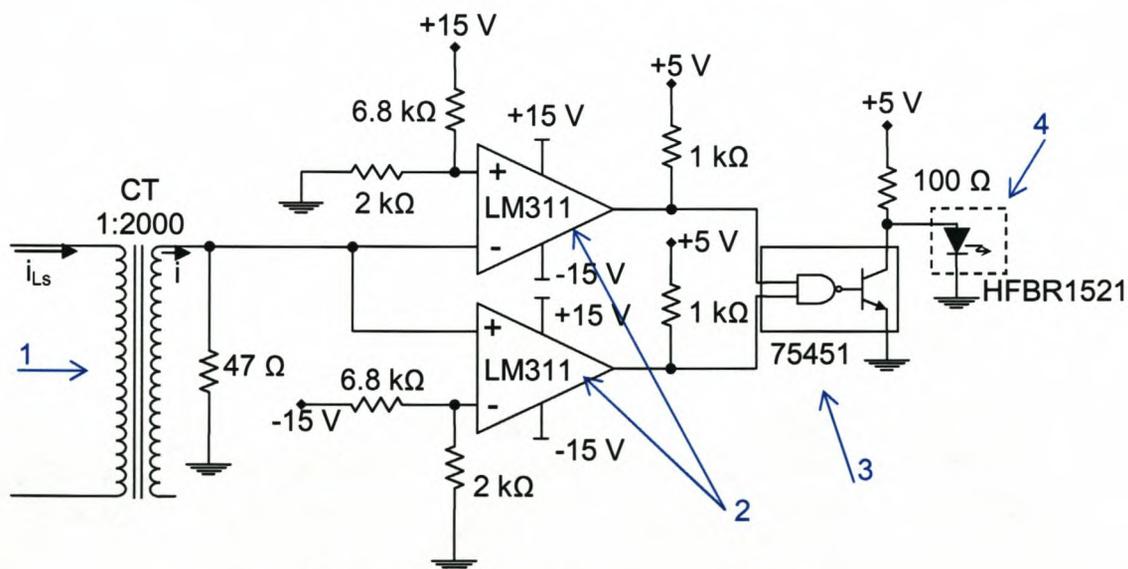
Figure 5-6: Circuit diagram of over-current detector

Figure 5-5 is a photo of the over-current detector and Figure 5-6 shows its circuit diagram.
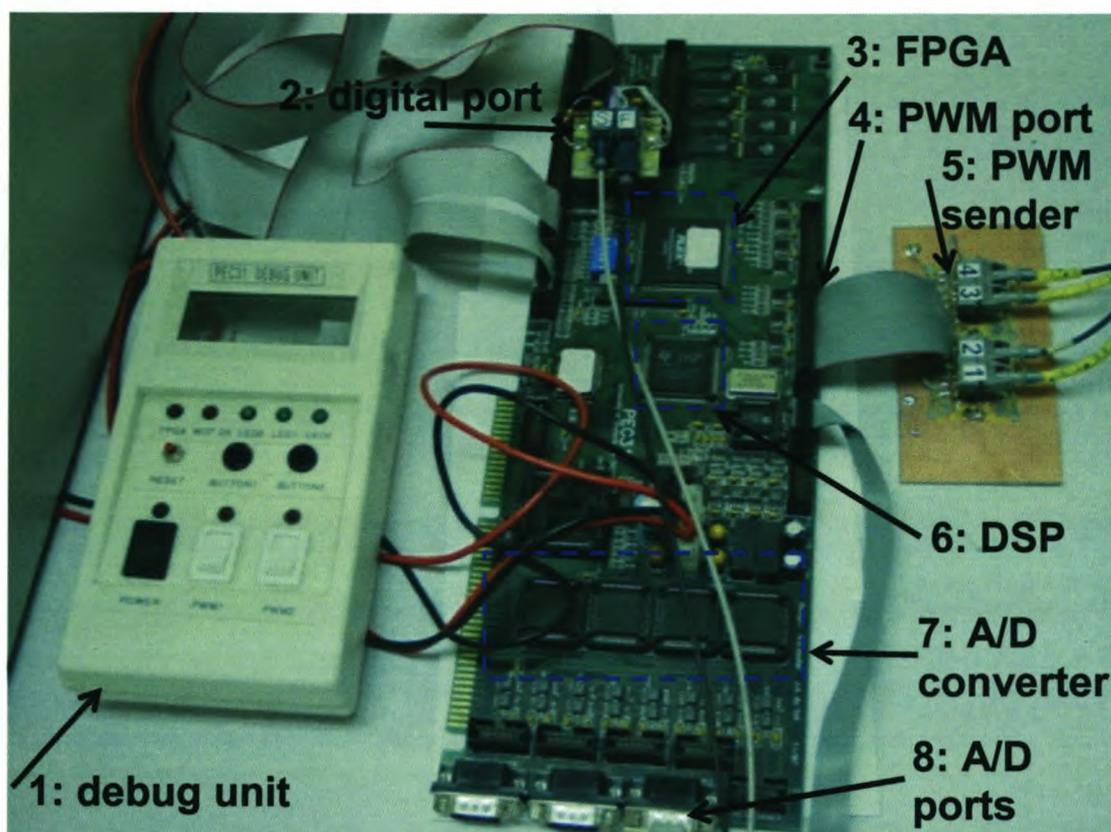
Figure 5-7: The controller board

Figure 5-7 is a photo of the PEC31 controller board [13] used in this system. The digital input port has fibre optic receivers from the sign and over-current detection circuits.

With tests it was found that the open-loop and closed-loop control methods are not as simple as first stated. The problems arose at the zero-crossing of the input current. Precautions were taken so that a 'divide by zero' cannot occur but it was found that, as the input voltage becomes very small, some problems still exist. What happened in both the open-loop and closed-loop case is that the reference (D) falls to zero and after the zero-crossing it became 1. This sudden change would not be such a problem if there was no phase shift between the input voltage and current as assumed in Chapter 4, but in a practical system this is not true. The sudden change in D results in a step in the input current and since the system's damping is relatively slow, this has a serious effect on the whole converter's performance.

The solution to this problem is relatively simple. The average duty ratio over one half-cycle is computed and for the few switching cycles during the zero-crossing this average is set as the D that is used as reference for the PWM block. This proved to be a very effective solution.

5.1 Experimental setup and simulations

The following section will compare the experimental and simulation results. The measurements were taken at the minimum input voltage (230 V_{RMS}) and at the maximum input voltage (420 V_{RMS}). The corresponding simulations were done and results obtained.

The assumption made in the design stage that there is no phase shift between the voltage and current is practically nearly impossible to obtain. This is obvious in both the simulations and the experimental results. An important difference between the simulations and the experiment is the leakage inductance of the variac. Since this inductance changes as the variac is turned to increase the voltage, it is difficult to obtain the correct value and in that sense the simulation is not entirely correct and small differences between the simulation and the measured values can be expected.

The simulation also uses near ideal components and the parasitic impedances are ignored. This will also lead to small differences.

5.1.1 Control by RMS computation

The first method of control that was investigated is the RMS computation method. This method was described in section 4.2.7 as number 1 and works by measuring v_C, computing the RMS value and dividing this value with the desired RMS value. This will then give the duty ratio at which the converter must switch.
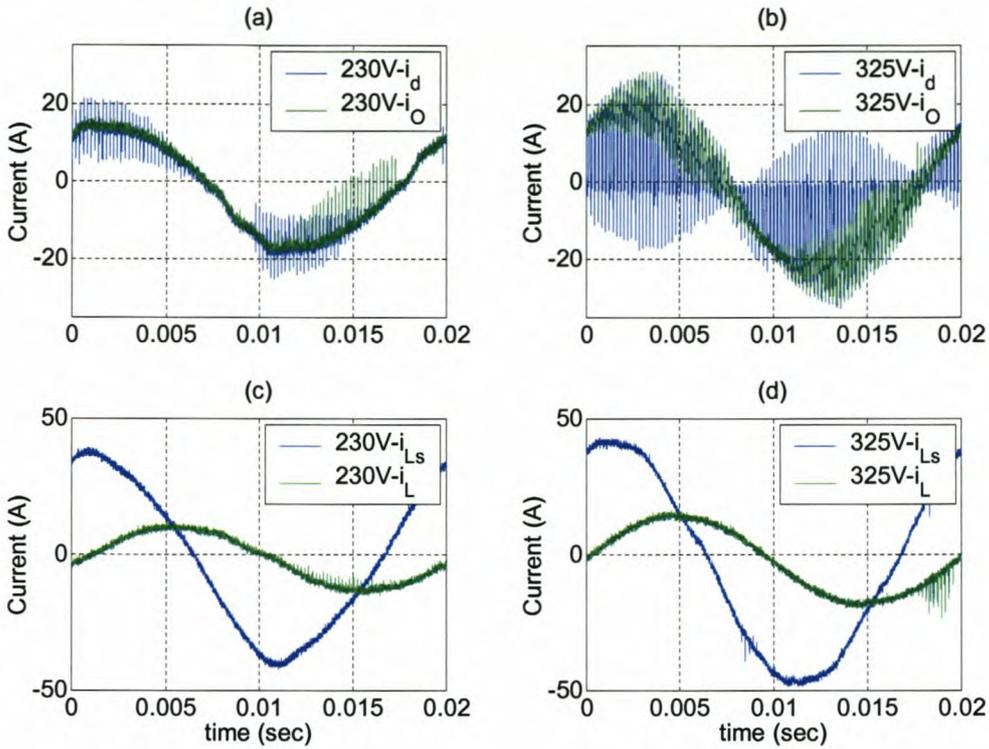
Figure 5-8: Measured currents of RMS control: (a) i_d, i_O and (c) i_{Ls}, i_L at 230 V v_C; (b) i_d, i_O and (d) i_{Ls}, i_L at 325 V v_C

Figure 5-8 shows the currents measured at 230 V and 325 V input voltage (v_C). Figure 5-8 (a) and (b) are the currents directly into (i_d) and out of the converter (i_O); and (c) and (d) are the load current (i_L) and the input current (i_{Ls}) from the variac. These currents are shown in the circuit diagram in Figure 5-10. Figure 5-9 shows the voltages measured at 230 V and 325 V v_C. Figure 5-9 (a) and (b) show the input (v_C) and output (v_L) voltages, (c) and (d) show the two snubber capacitors' voltages (v_{Cs1} and v_{Cs2}); and (e) and (f) show the unfiltered output voltage (v_O). These are shown in Figure 5-10.
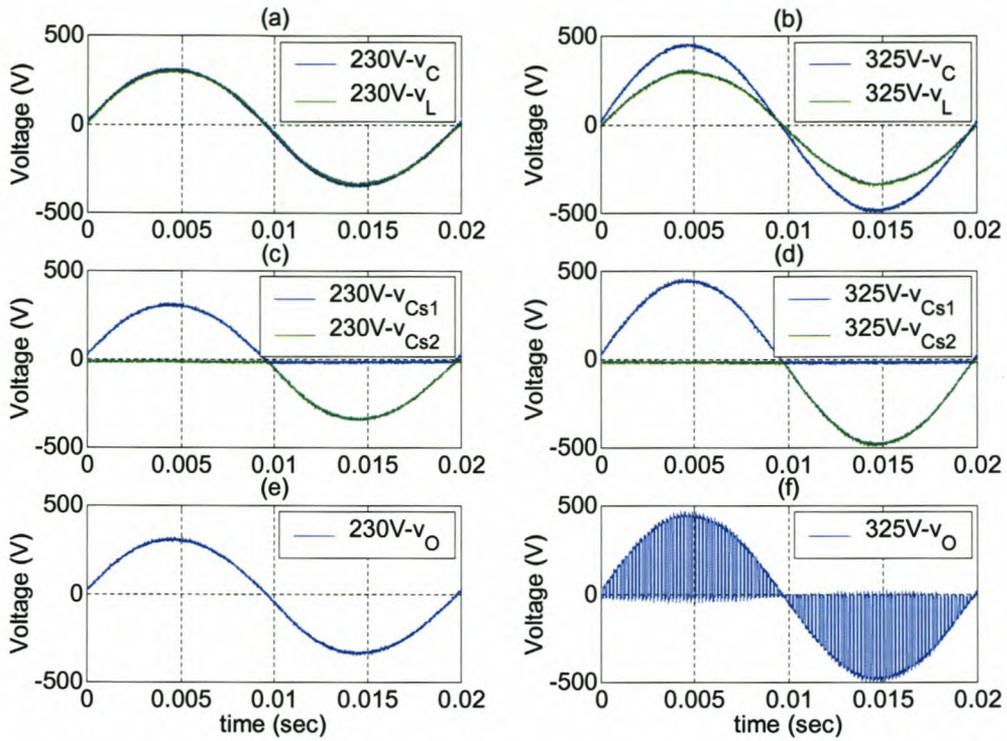
Figure 5-9: Measured voltages of RMS control: (a) v_C, v_L, (c) v_{Cs1}, v_{Cs2} and (e) v_O at 230 V v_C; (b) v_C, v_L, (d) v_{Cs1}, v_{Cs2} and (f) v_O at 325 V v_C
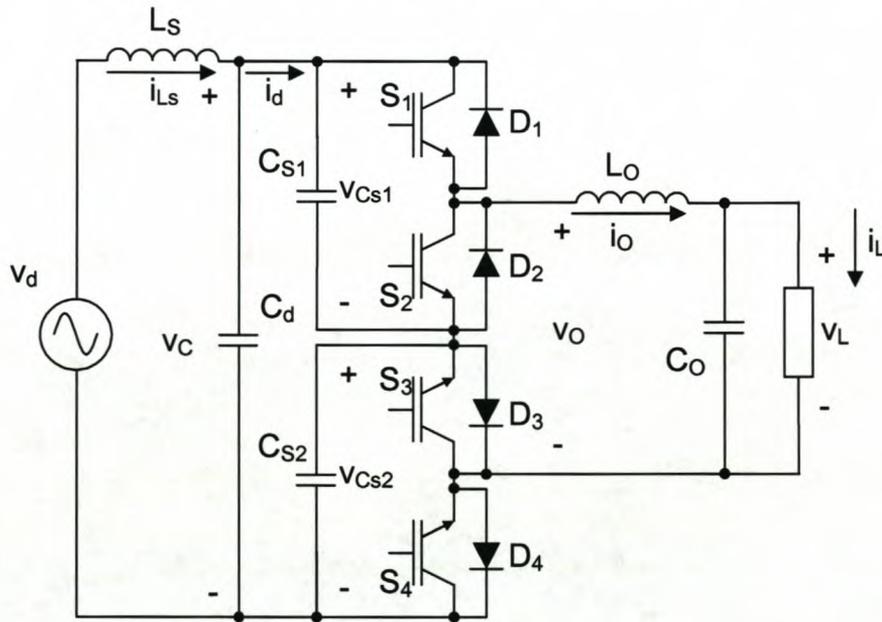
Figure 5-10: Circuit diagram of circuit

Figure 5-11 and Figure 5-12 show the measured and simulated currents and voltages taken at a v_C of 420 V, the maximum input voltage allowed. The

figures on the left are the measured graphs and on the right are the simulated graphs. In the graph legend the measured signals are shown with the prefix M- and the simulations are shown with S-. The signals are grouped as in Figure 5-8 and Figure 5-9.

From these figures it can be seen that this method of control of computing the RMS value operates well. It must be remembered, though, that this method is rather slow, since the reference (D) is only updated once each 50 Hz cycle. The input voltage to the experimental setup is purely sinusoidal and thus the output voltage will be purely sinusoidal.

Comparing the measured and simulated signals it can be seen that, as mentioned in the beginning of this section, there are small differences. The measured voltages are almost the same as the simulated voltages. The differences are with the currents. The simulated currents are a little larger than the measured currents. This is because the simulation uses ideal components and the input inductor is not exactly the same as the variac's leakage inductance. The variac was simulated as an inductor and a small resistor in series. The stray inductances and parasitic components of the components are not taken into consideration in the simulated converter.

Noise can be seen in the current measurements. This is because the current probe was not properly isolated from EMC. The circuit layout can be improved to limit this noise further.

With all of the above taken into account, it can be said that the comparison between the measured and simulated signals is good.
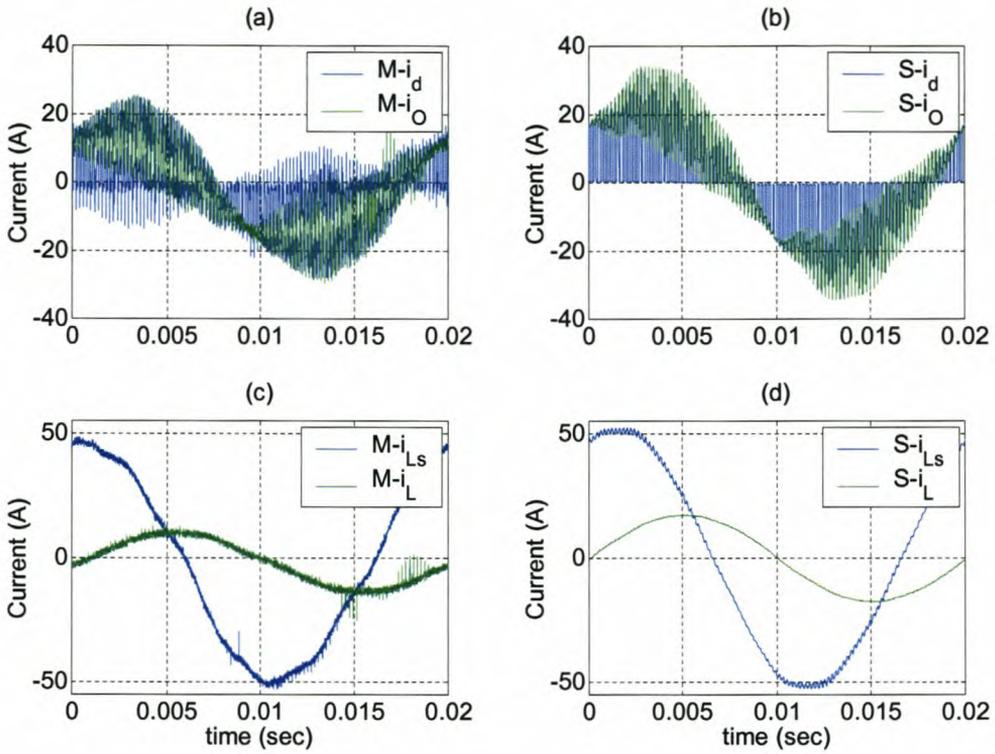
Figure 5-11: Measured currents of RMS control at 420 V v_C: (a) i_d, i_O and (c) i_{Ls}, i_L; simulated currents of RMS control at 420 V v_C: (b) i_d, i_O and (d) i_{Ls}, i_L
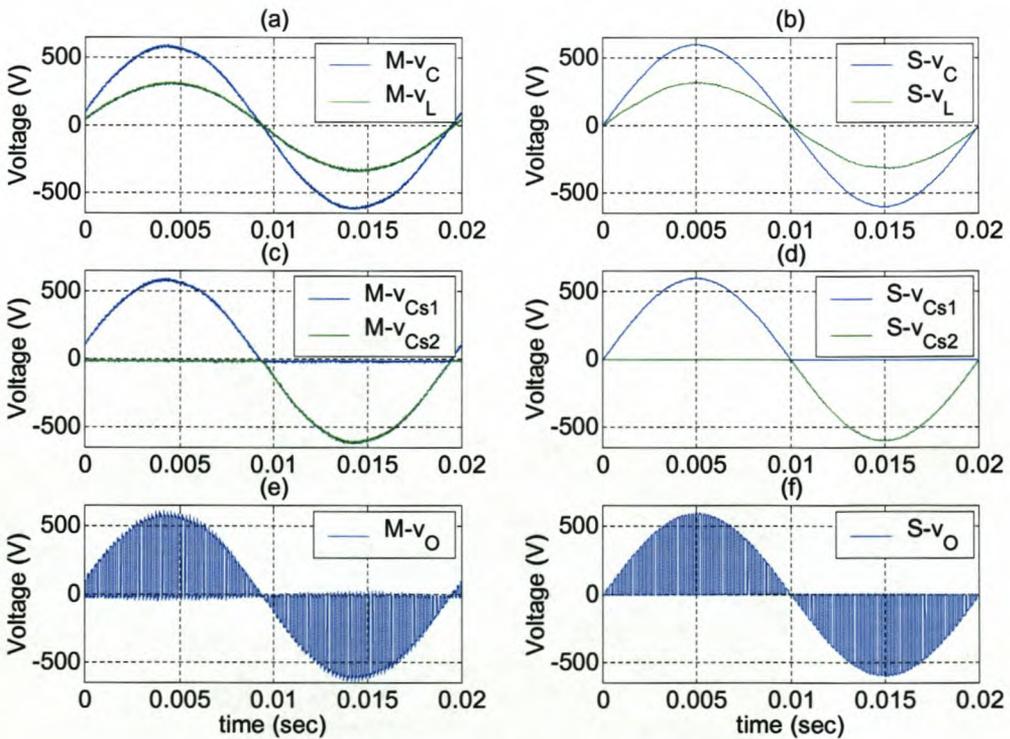
Figure 5-12: Measured voltages of RMS control at 420 V v_C: (a) v_C, v_L, (c) v_{Cs1}, v_{Cs2} and (e) v_O; simulated voltages of RMS control at 420 V v_C: (b) v_C, v_L, (d) v_{Cs1}, v_{Cs2} and (f) v_O

5.1.2 Open-loop control (reference/measured)

The following section is devoted to the open-loop control method. In this method a reference signal of the output voltage, v_L, is created in the DSP. This reference is synchronised with the input voltage, v_C, and divided by the measured value of v_C. The duty ratio is updated every switching period. This method is a lot faster than the previous one.
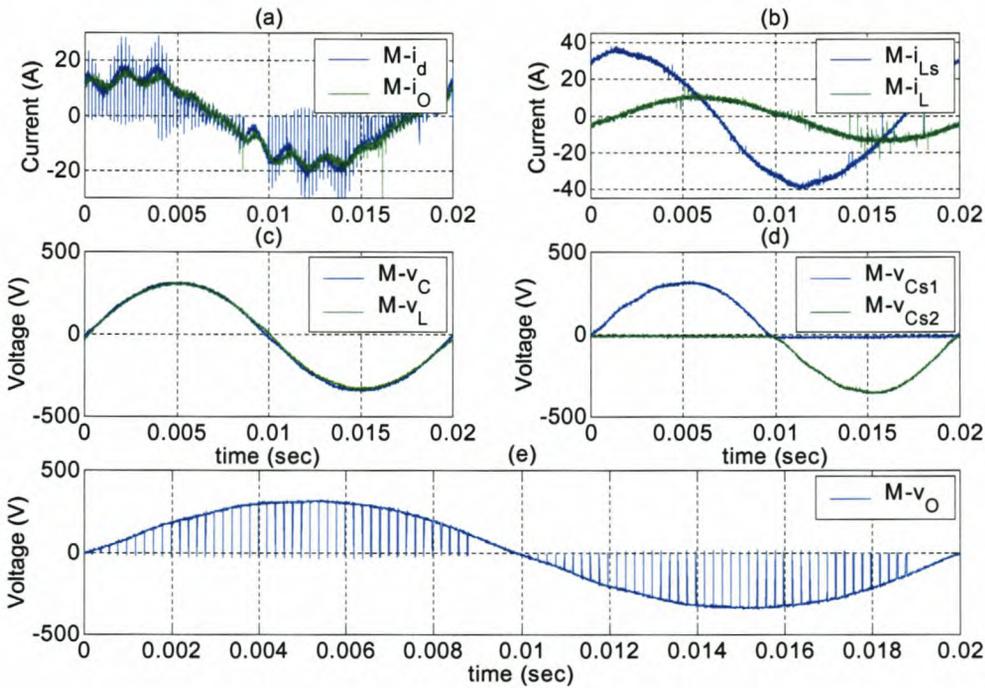
Figure 5-13: Measured currents of open-loop control at 230 V v_C: (a) i_d, i_O and (b) i_{Ls}, i_L; and measured voltages of open-loop control at 230 V v_C: (c) v_C, v_L, (d) v_{Cs1}, v_{Cs2} and (e) v_O;

Figure 5-13 shows the measured voltages and currents taken at 230 V. It can be seen that the duty ratio is still large, almost one. Some noise has been measured with the currents. Figure 5-13 (a) shows the current directly into (i_d) and out of (i_O) the converter, and (b) shows the currents from the variac (i_{Ls}) and the load current (i_L). Figure 5-13 (c) shows the input (v_C) and output (v_L) voltages; it can be seen that the voltages are almost equal in size; (d) shows the two snubber capacitors' voltages (v_{Cs1} and v_{Cs2}). Figure 5-13 (e) shows the unfiltered output voltage (v_O).
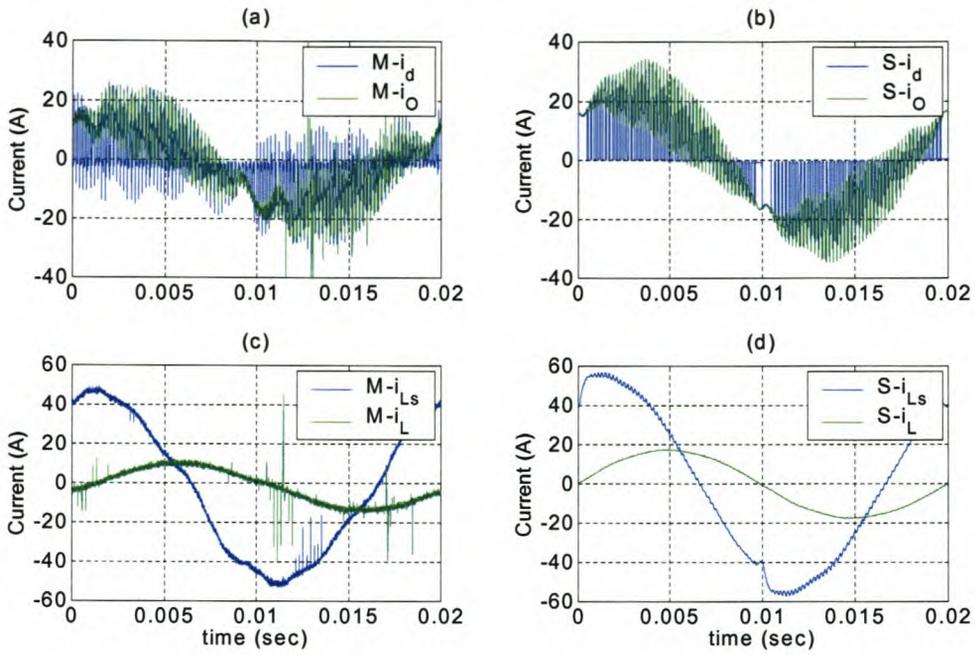
Figure 5-14: Measured currents of open-loop control at 420 V v_C: (a) i_d, i_O and (c) i_{Ls}, i_L; simulated currents of open-loop control at 420 V v_C: (b) i_d, i_O and (d) i_{Ls}, i_L
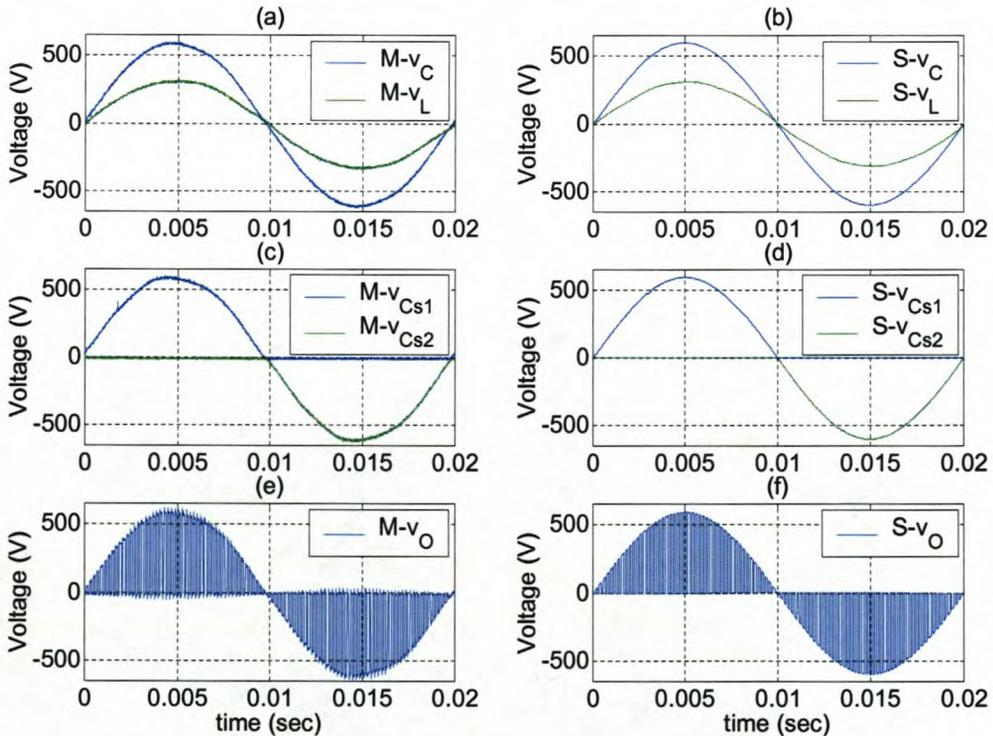
Figure 5-15: Measured voltages of open-loop control at 420 V v_C: (a) v_C, v_L, (c) v_{Cs1}, v_{Cs2} and (e) v_O; simulated voltages of open-loop control at 420 V v_C: (b) v_C, v_L, (d) v_{Cs1}, v_{Cs2} and (f) v_O

Figure 5-14 and Figure 5-15 show the measured and simulated signals of this type of control. The signals are arranged and grouped as in the previous section. Again it can be seen from the voltages and currents that the method works well. The voltages of the measured and simulated setups are the same and the currents differ in the same ways as in section 5.1.1 for the same reasons. It was mentioned in the beginning of the chapter that some problems occurred during the zero-crossing of v_C; this can be seen in the oscillation of the currents i_d and i_O measured (Figure 5-14 (a)).

The reason that the oscillations start a short time before v_C goes through zero is because of the proposed solution to the problem. This solution was to compute and insert the average duty ratio over the half-cycle into the short time, a few switching cycles, that v_C will be crossing zero. Before this insertion, reference values are small and the duty ratio will decrease. The step in the computed duty ratio to the inserted one causes a very small step in the current. The converter's damping is small and this leads to the overshoot and visible settling time. Some noise can be seen in the measured currents.

Figure 5-14 (b) and (d) shows the simulated currents. The fault mentioned above is not compensated for in the simulation. The step in the input current i_{Ls} is obvious. Because the simulated model is ideal, the effects of this step die away quickly.

5.1.3 Closed-loop control

The last method of control is the closed-loop control. An ordinary P-type controller is used. This was implemented in the DSP and Figure 5-16 shows the basic block diagram of the control. K_2 is the P controller and is a very small number and, because of this, K_1 is needed to scale the reference.
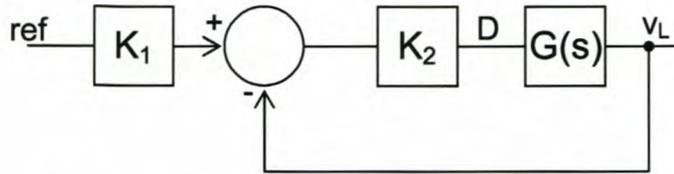
Figure 5-16: Block diagram of closed-loop control
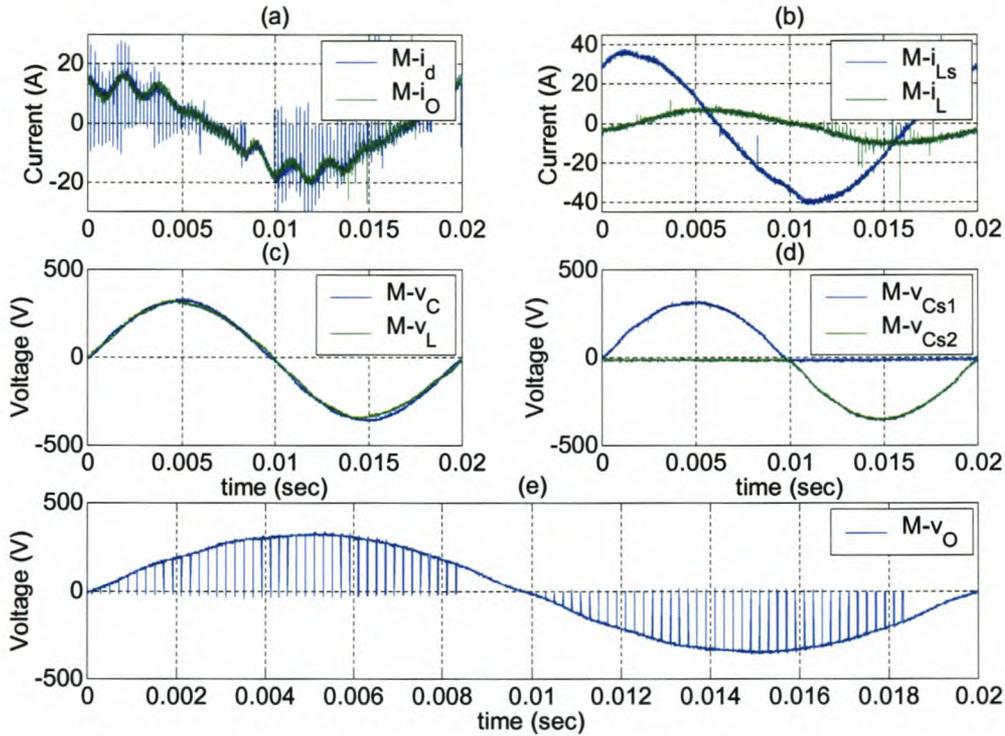
Figure 5-17: Measured currents of closed-loop control at 230 V v_C: (a) i_d, i_O and (b) i_{Ls}, i_L; and measured voltages of closed-loop control at 230 V v_C: (c) v_C, v_L, (d) v_{Cs1}, v_{Cs2} and (e) v_O;

Figure 5-17 shows the measured currents and voltages taken at 230 V input voltage. The load resistance with this method is 24 Ω instead of the 18 Ω of the other two methods of control. This is because this method required more current than the other methods and the variac used could not supply that amount of current. The signals are arranged and paired as in Figure 5-13. Again it can be seen that the duty ratio is large and the signals in Figure 5-13 and Figure 5-17 are almost alike. The most visible difference is that the oscillations caused by the zero-crossing problem are more prominent in the closed-loop control than in the open-loop control. In the measurements taken at 420 V v_C the problem is more evident.
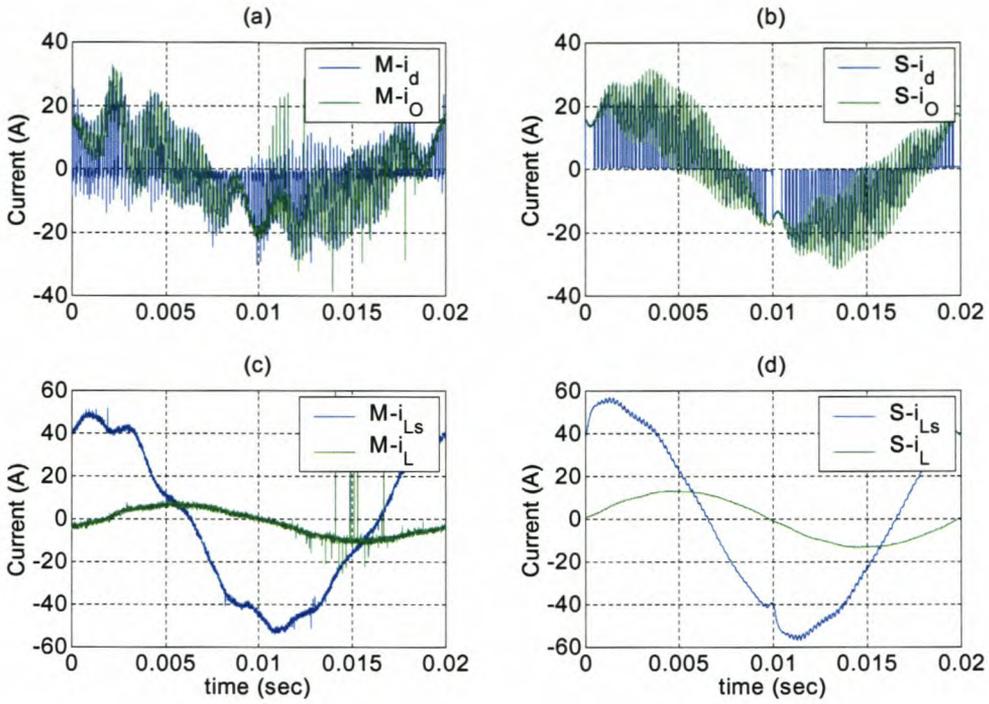
Figure 5-18: Measured currents of closed-loop control at 420 V v_C: (a) i_d, i_O and (c) i_{Ls}, i_L; simulated currents of closed-loop control at 420 V v_C: (b) i_d, i_O and (d) i_{Ls}, i_L
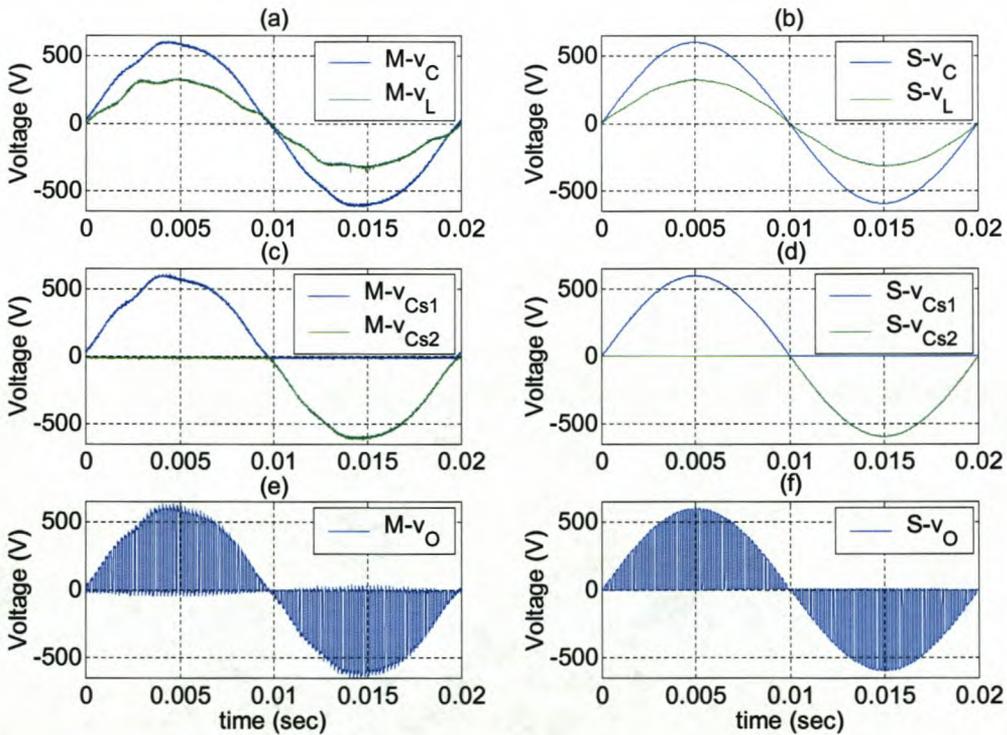
Figure 5-19: Measured voltages of closed-loop control at 420 V v_C: (a) v_C, v_L, (c) v_{Cs1}, v_{Cs2} and (e) v_O; simulated voltages of closed-loop control at 420 V v_C: (b) v_C, v_L, (d) v_{Cs1}, v_{Cs2} and (f) v_O

Figure 5-18 and Figure 5-19 are the measured and simulated signals of this type of control. The signals are arranged and grouped as in the open-loop control method. With both voltages and current it is obvious that the zero-crossing is more of a problem in the closed-loop control than in the open-loop control. This can be reduced by increasing the time that the duty ratio is kept constant at the average value during the zero-crossing. This is not desirable, however, because the idea of the closed-loop control and the converter is to have a fast-acting regulator. Further research is needed to solve this problem. One possible solution is to design a better controller, such as a PI controller and not just a P controller.

The simulated converter does not compensate for the zero-crossing problem and, as seen in Figure 5-18 (d), the step in the input current is obvious. Again the effects of this step die away quickly and have no significant effect on the voltages.

5.2 Harmonics and output voltages

In this section the converter is evaluated at a different level. This will be the harmonic spectrum of the unfiltered output voltage v_O and the filtered output voltage v_L, a non-linear load, efficiency of the converter, input voltage v_C versus output voltage v_L and the converter reaction to the over-current protection.

5.2.1 Amplitude spectrums and total harmonic distortion

The next section discusses the amplitude spectrums and the total harmonic distortion (THD) of the measured unfiltered (v_O) and output (v_L) voltages. This aspect will be considered for the three control methods with input voltages v_C at 230 V and 420 V. These voltages are the maximum and minimum of the input voltage (v_C) and v_C can be any voltage in between.

5.2.1.1   Control by RMS computation

In the next section the amplitude spectrum of v_O and v_L will be given for v_C equal to 230 V, 325 V and 420 V.
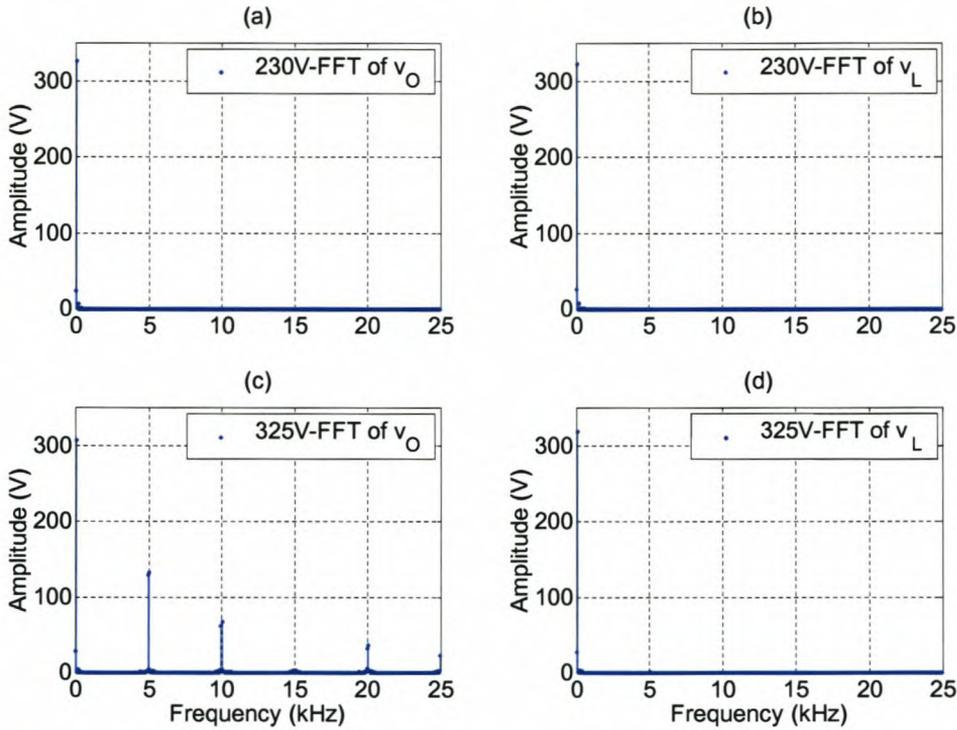
Figure 5-20: Measured amplitude spectrum at 230 V v_C: (a) v_O and (b) v_L; measured amplitude spectrum at 325 V v_C: (c) v_O and (d) v_L

The THD has been computed and will be added to the discussion. The simulated values for the 420 V case have also been added. Figure 5-20 (a) and Figure 5-20 (b) show the amplitude spectrum of v_O and v_L at 230 V v_C and (c) and (d) are the spectrum at 325 V v_C. The signals used are the measured voltages and the THD of these voltages were computed and are given in Table 5-1 with the THD of the voltages taken at 420 V v_C and the simulated voltages at 420 V v_C.
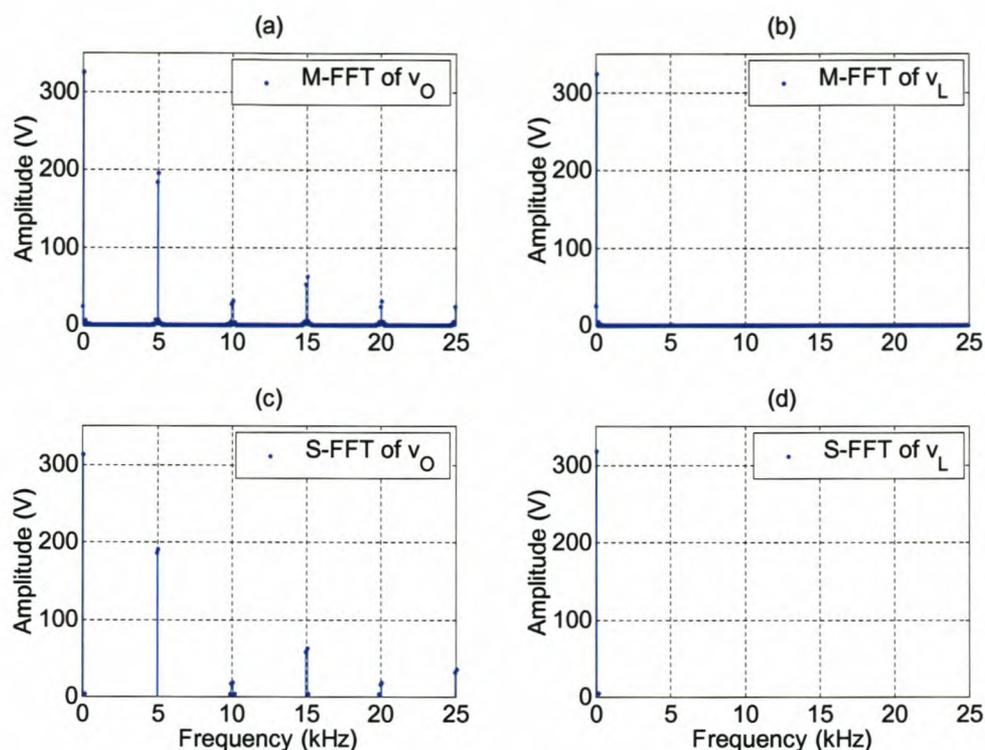
Figure 5-21: Measured amplitude spectrum at 420 V v_C: (a) v_O and (b) v_L; simulated amplitude spectrum at 420 V v_C: (c) v_O and (d) v_L;

THD of v_O at 230 V v_C (measured)	2.4337%
THD of v_L at 230 V v_C (measured)	2.7068%
THD of v_O at 325 V v_C (measured)	69.7578%
THD of v_L at 325 V v_C (measured)	1.8816%
THD of v_O at 420 V v_C (measured)	88.1874%
THD of v_L at 420 V v_C (measured)	1.8434%
THD of v_O at 420 V v_C (simulated)	93.9840%
THD of v_L at 420 V v_C (simulated)	1.3869%

Table 5-1: Total harmonic distortion of v_O and v_L - RMS

The THDs in Table 5-1 are as expected. At 230 V v_C there is almost no switching and v_L and v_C are almost the same. This is why there THDs are almost equal. With the THDs at 325 V and 420 V v_C, it can be seen that as the converter starts to switch and as the duty ratio decreases the THD of v_O will rapidly increase. This is expected and it can be seen that the THD of v_L

decreases a little from that of a non-switching converter but they are still basically the same. The simulated values are very close to the measured values. The differences can be attributed to ideal components in the simulation. The THD of v_L in all the cases is under 8%, the maximum allowed according to the regulations [43].

5.2.1.2 Open-loop control (reference/measured)
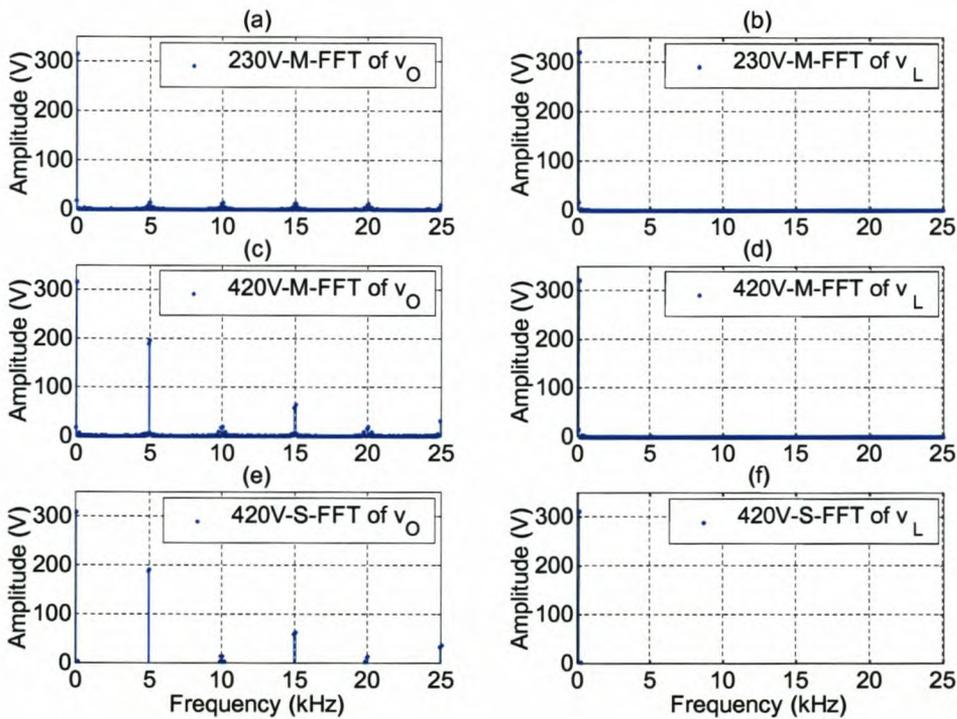
Figure 5-22: Measured amplitude spectrum at 230 V v_C: (a) v_O and (b) v_L; measured amplitude spectrum at 420 V v_C: (c) v_O and (d) v_L; simulated amplitude spectrum at 420 V v_C: (e) v_O and (f) v_L

Figure 5-22 shows the amplitude spectrum of v_O (a), (c) and (e) and v_C (b), (d) and (f). Figure 5-22 (a) and Figure 5-22 (b) are of the measured voltages at 230 V v_C; (c) and (d) are of the measured voltages at 420 V v_C; and (e) and (f) are of the simulated voltages at 420 V v_C. The THDs of these signals have been computed and are listed in Table 5-2.

THD of v_O at 230 V v_C (measured)	13.7796%
THD of v_L at 230 V v_C (measured)	1.8698%
THD of v_O at 420 V v_C (measured)	92.0016%
THD of v_L at 420 V v_C (measured)	2.0090%
THD of v_O at 420 V v_C (simulated)	95.2027%
THD of v_L at 420 V v_C (simulated)	1.3704%

Table 5-2: Total harmonic distortion of v_O and v_L – open-loop

The THDs are as expected. With this type of control there is some switching taking place at 230 V v_C. This is the reason that there is a significant difference in the THD of v_O and v_L, but the THD of v_O is still small due to the high duty ratio at this voltage. The simulated and measured voltages yield about the same THD if the tolerances are taken into account. Again the THD of the load voltage v_L is below the allowed 8% [43].

5.2.1.3   Closed-loop control

Figure 5-23 show the same amplitude spectrums as in Figure 5-22. The spectrums are arranged the same way in both figures. Table 5-3 gives the THDs of these voltages.

THD of v_O at 230 V v_C (measured)	15.3097%
THD of v_L at 230 V v_C (measured)	3.5929%
THD of v_O at 420 V v_C (measured)	92.2323%
THD of v_L at 420 V v_C (measured)	7.0089%
THD of v_O at 420 V v_C (simulated)	93.4098%
THD of v_L at 420 V v_C (simulated)	1.5497%

Table 5-3: Total harmonic distortion of v_O and v_L – closed-loop
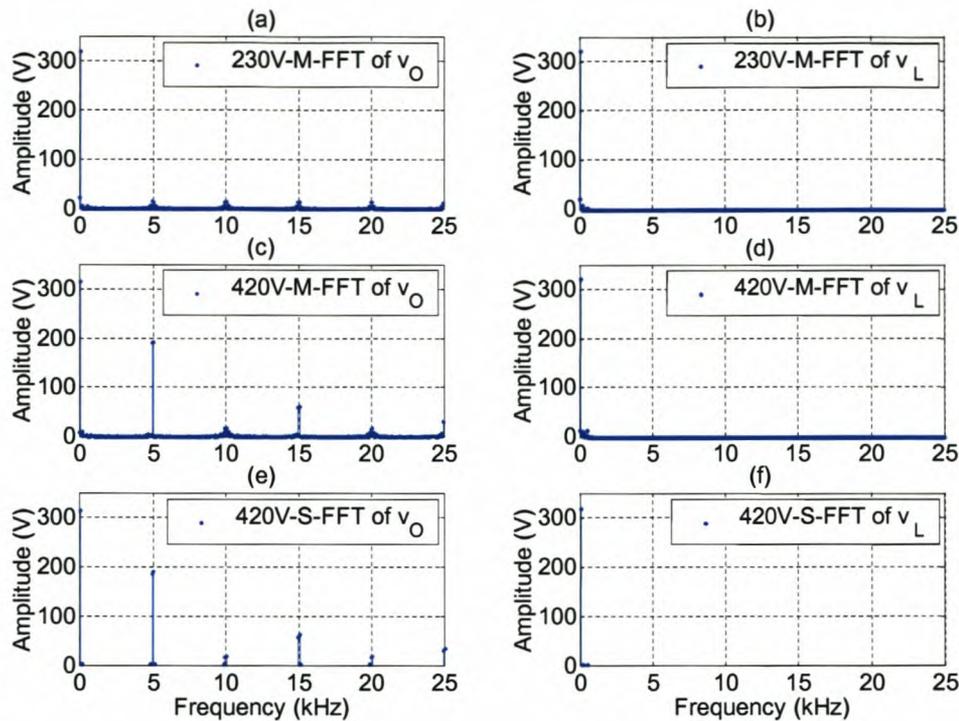
Figure 5-23: Measured amplitude spectrum at 230 V v_C: (a) v_O and (b) v_L; measured amplitude spectrum at 420 V v_C: (c) v_O and (d) v_L; simulated amplitude spectrum at 420 V v_C: (e) v_O and (f) v_L

The THDs of the measured voltages are worse than those of the simulated voltages. This is because of the oscillation at the zero-crossing. The load voltages' THD are still just under 8%. The margin with which the THD of v_L at 420 V v_C is within the specifications is small and can be improved with a better controller.

5.2.2 Extended evaluation

More information than the above comparisons is needed to be able to make a judgment on the proposed and constructed converter. One set of measurements that was hinted at in Chapter 4 is the efficiency of the converter. Figure 5-24 (a) show a comparison between the measured and computed efficiency. It can be seen that the comparison is very good.

Figure 5-24 (b) shows the input voltage v_C versus the output voltage v_L. It is shown that v_L remains almost constant, while v_C varies between the minimum and maximum values.
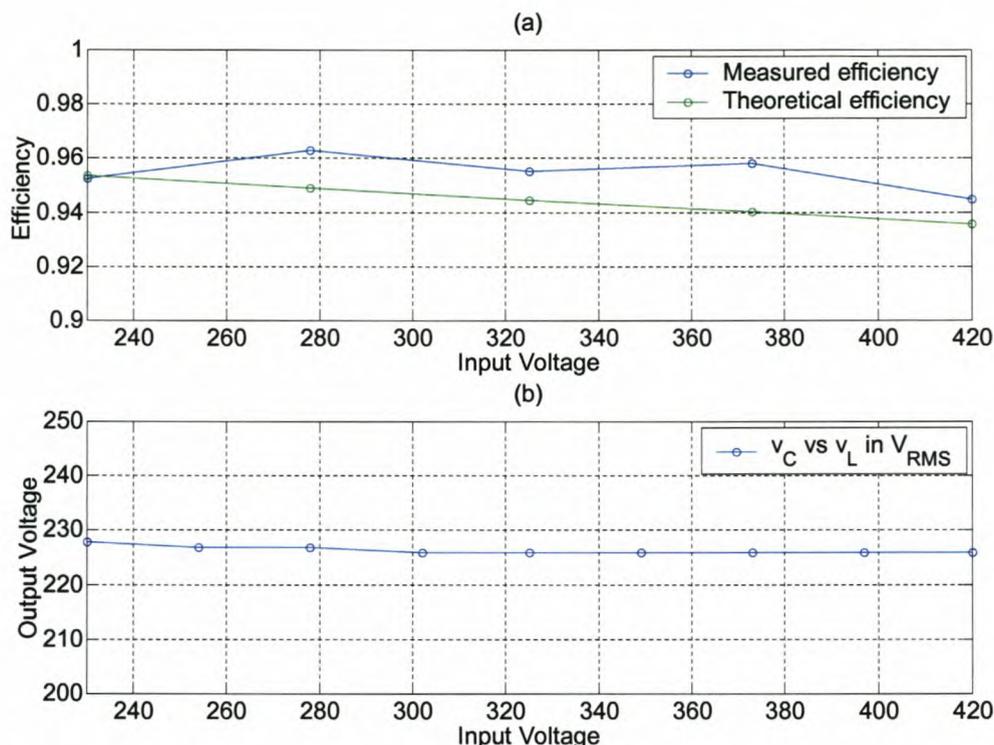
Figure 5-24: (a) Converter's efficiency, measured and computed; (b) Input voltage v_C vs. output voltage v_L

The next set of measurements was done with a purely non-linear load. The load was a diode rectifier with a large capacitor filter and a load resistance. Figure 5-25 (a) shows the output voltage v_L and (b) shows its amplitude spectrum. Figure 5-25 (c) shows the load current i_L and (d) is its amplitude spectrum. The resistor's size is 29.6 Ω; this was the load that required the highest current the variac can provide. The voltage's THD is 14.7% and the current's THD is 79.1%. The specifications in [43] say that v_L's THD must be below 8%. To be able to see which harmonic causes the problem, the amplitude spectrum of v_L is plotted together with the specified harmonics in Figure 5-26. It can be seen that the problem lay with the third harmonic, since it is at least double the specified amount. The other harmonics fall within the specifications, except the ninth which is just above.
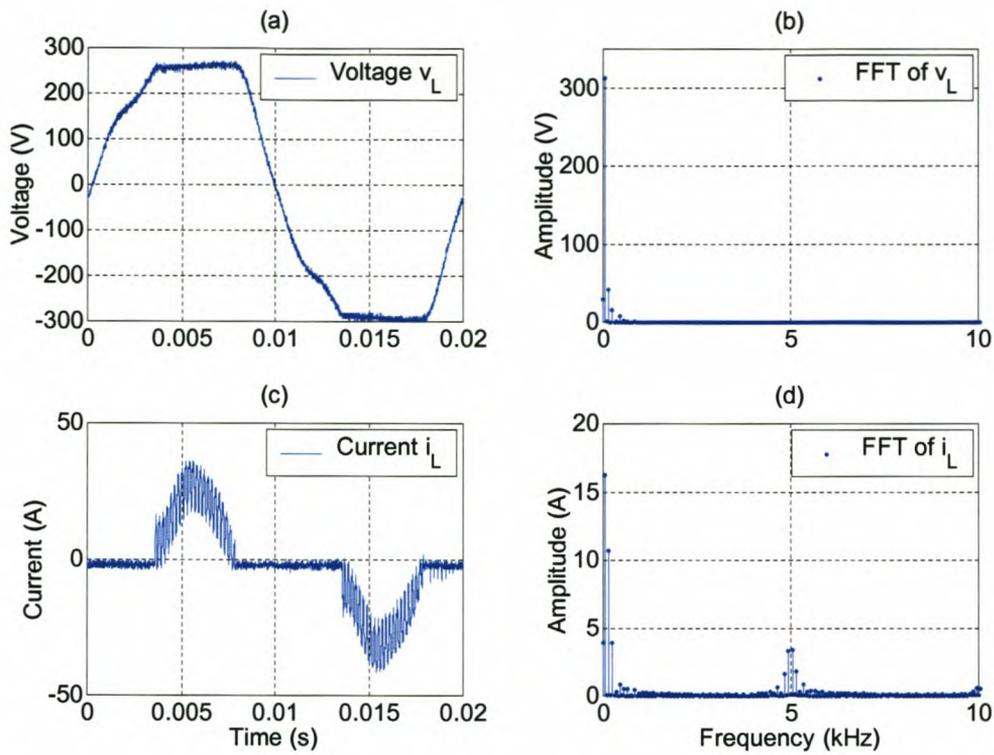
Figure 5-25: (a) Output voltage v_L with non-linear load; (b) amplitude spectrum of v_L with non-linear load; (c) load current i_L with non-linear load; (d) amplitude spectrum of i_L with non-linear load
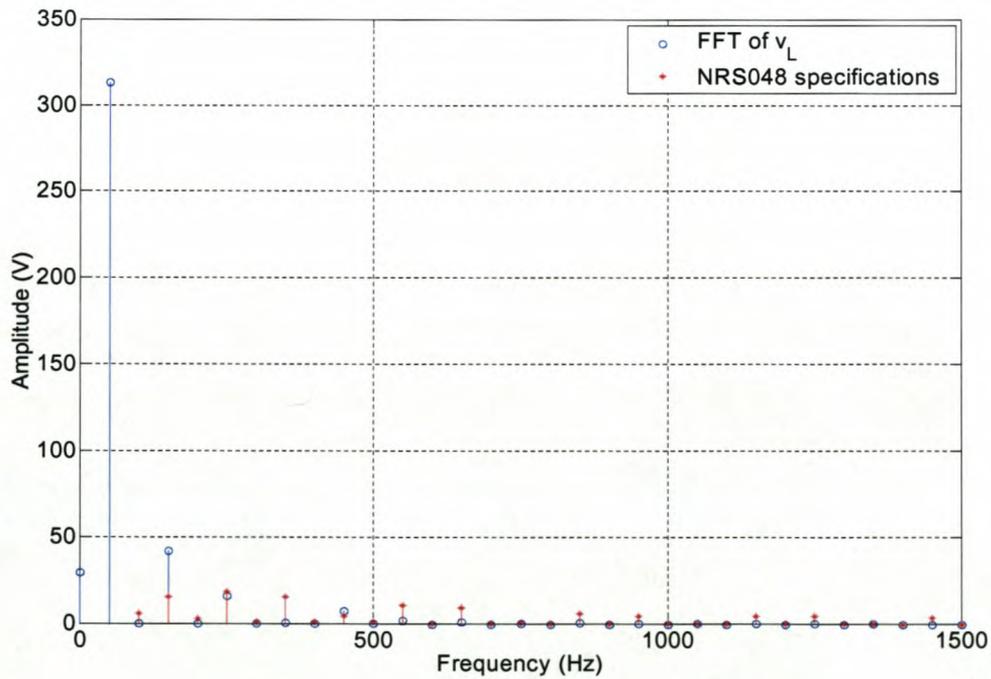
Figure 5-26: Amplitude spectrum of output voltage compared with NRS048 specifications
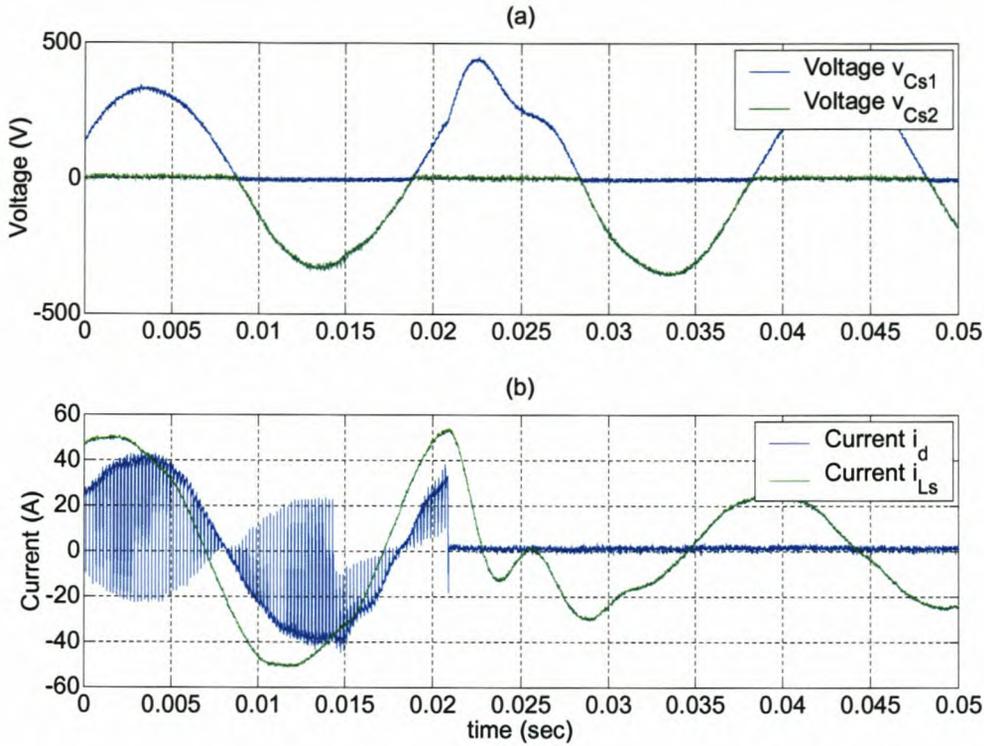
Figure 5-27: Converter's reaction to over-current protection in (a) snubber capacitors' voltage v_{Cs1}, v_{Cs2} ; (b) input currents i_d, i_{Ls}

Figure 5-27 (a) shows the voltages over the IGBT phase arms, v_{Cs1} and v_{Cs2}, and (b) shows the current into the converter i_d and the current delivered to the system from the variac i_{Ls}. In Figure 5-27 (b) the over-current detection points are shown by the red horizontal lines. The over-current detection points have been reduced to just less than 55 A; this was done because the variacs used can only deliver 40 A_{RMS}. The horizontal red line indicates the point at which a fault was detected.

This fault occurred during a positive half-cycle; the voltage over the snubber capacitor was distorted as the input current i_{Ls} settled. The voltages over the two snubbers and thus the IGBT phase arms resumed their normal trace, which is proof that the converter is still commutating according to the input voltage v_C. The current into the converter i_d becomes zero after the over-current protection is activated. This is as expected. The input current i_{Ls}, after settling, reduces in size and continues its sinusoidal trace. This current now

flows through the input capacitor C_d and the resistor that has been placed in parallel with it. The resistor was mentioned at the beginning of the chapter.

This experiment is proof that the over-current protection works as expected and will protect the converter by switching it safely.

5.3 Summary

This chapter took the converter from the design stage to an experimental setup. It discussed some of the problems encountered and the solutions for them. The three methods of control were discussed and compared with the simulation results. It was found that the closed-loop control needs more work to obtain the correct results.

The amplitude spectrum of the unfiltered output voltage v_O and the output voltage v_L were found with their THD's. These fall within the NRS048 standards. The converter's input voltage versus output voltage proved that the converter regulates the voltage. The measured efficiency matched the computed efficiency well. The converter was tested with a non-linear load and, since it was not designed for harmonic regulation, performed badly. The over-current protection was tested and it proved to operate well.

The final chapter will be a conclusion to the report.

Chapter 6

Conclusions

6 Conclusions

6.1 Summary

There is a need for a dynamic voltage regulator. This report discusses this need and different types of regulators were investigated. After the commercially available types of regulators were discussed, the focus turned to converter-based technology. It was decided that the AC-to-AC converter type will be best for this voltage regulator.

Different topologies of AC-to-AC converters were investigated and it was found that a converter based on a buck converter will be best. The voltage detection control was more reliable than the current detection control. This converter was then analysed and designed.

In the analysis of the converter, the voltages and currents were defined. The losses in the switches were defined and the equations for them found. The output filter, the inductor and capacitor were designed. The voltage spectrum of the unfiltered output voltage was investigated so that the converter's reactions will be better understood and a comparison may be made between the commonly used DC-to-AC converter and the AC-to-AC converter. The circuit was also investigated under fault conditions.

The design then followed, including the switching components and their losses. The gate-drive circuits were discussed, followed by the output filter's design using the equations found in the analysis section. The over-current protection and the sign-detection circuits were designed and discussed. The snubber capacitors were designed. The three control methods were developed and will be discussed in more detail later in this section. The last parts to be discussed were the startup conditions, the thermal analysis and the transformer design.

An experimental setup was built and tested. Simulations were done of the actual setup and the three control methods were evaluated. The voltage spectrum of the output voltages, filtered and unfiltered, were measured and evaluated. Further tests were done to see what the output voltage v_L does when the input voltage v_C is varied. The efficiency of the converter was measured and compared with the computed efficiency. A nonlinear load was attached to the converter and the effects of this evaluated. The aspect tested was the over-current protection.

The first type of control is where the RMS of the input voltage v_C is computed. This computed value is then used to find the duty ratio D. This ratio is updated once every 50 Hz cycle. The next type of control is where a reference voltage is generated within the DSP controller and used to compute the duty ratio once every switching period. The last method is an ordinary closed-loop control using a P type of controller. This is just a constant value placed in the controller's position.

6.2 Conclusions

Conclusions can only be drawn if the results of the experimental tests are investigated. This will be done for each of the control methods.

6.2.1 RMS computation control

With the RMS computation method it was found that it operated the best because a purely sinusoidal input voltage was used. This method is slow compared to the other methods and one of the design specifications is that the converter must react rapidly to changes of the input voltage.

Measurements were taken at three different input voltages: 230 V, 325 V and 420 V. Simulations were done at 420 V. The voltages of the measured and the simulated results compare well. Taking the limitations of the simulations

into account, it can be said that the measured currents compared well with the simulated currents.

The amplitude spectrum was favourable and fell within the NRS048 regulations. The THD of the unfiltered output voltage was considerably lower than that of the DC-to-AC converter.

6.2.2 Open-loop control

With the open-loop method of control an open-loop or feed-forward type of control was used. It is a lot faster than the RMS method, because it updates the duty ratio every switching period. This method had problems with the zero-crossing, but they could be solved satisfactorily.

The measurement taken was at an input voltage of 230 V and 420 V. The simulations done at 420 V compare well with the experimental results. Noise was measured on the currents.

The amplitude spectrum and the THD of the output voltages are still within the specifications.

6.2.3 Closed-loop control

The closed-loop control also updates every switching period. The problem with the zero-crossing was a lot more significant here and the load resistance had to be enlarged from 18 Ω to 24 Ω to ensure that the variac can supply the current required.

The measurements and simulations were taken at the same input voltages as the open-loop control. The output voltage's THDs were just within the regulations, but can do with improvements.

The RMS computation control method operated the best of the three, but it is slow. The open-loop control is fast enough and operates well within specifications. The closed-loop method of control did not operate as hoped and more research needs to be done on this method.

6.2.4 Other tests

The test with the input voltage v_C versus output voltage v_L proved that the regulator regulates the output voltage, because the output voltage hardly changed regardless of the input voltage.

The converter's efficiency as it was measured compared well with the computed efficiency. The switching losses of the converter are at most 79% of the ordinary DC-to-AC converter's losses. This implies that this converter's efficiency will be higher than the DC-to-AC converter's.

The converter was connected to a nonlinear load next and as expected it did not perform very well. The output voltage had a significant third harmonic that pushed the THD beyond the specifications. The converter was never designed to be able to correct the harmonic distortion that loads such as diode rectifiers produce. It will be advisable to investigate this further.

The last aspect is the over-current protection. The test performed proved that the protection scheme operates as desired.

6.3 Recommendations and future work

The next step in this project is to convert the single-phase converter to a three-phase converter. This can then open up the field of matrix converters. The converter can also be adapted for higher ratings.

The more immediate work to be done on the converter is to improve the closed-loop control method's control by using a PI type of controller or by improving the method of implementation.

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APPENDIX A
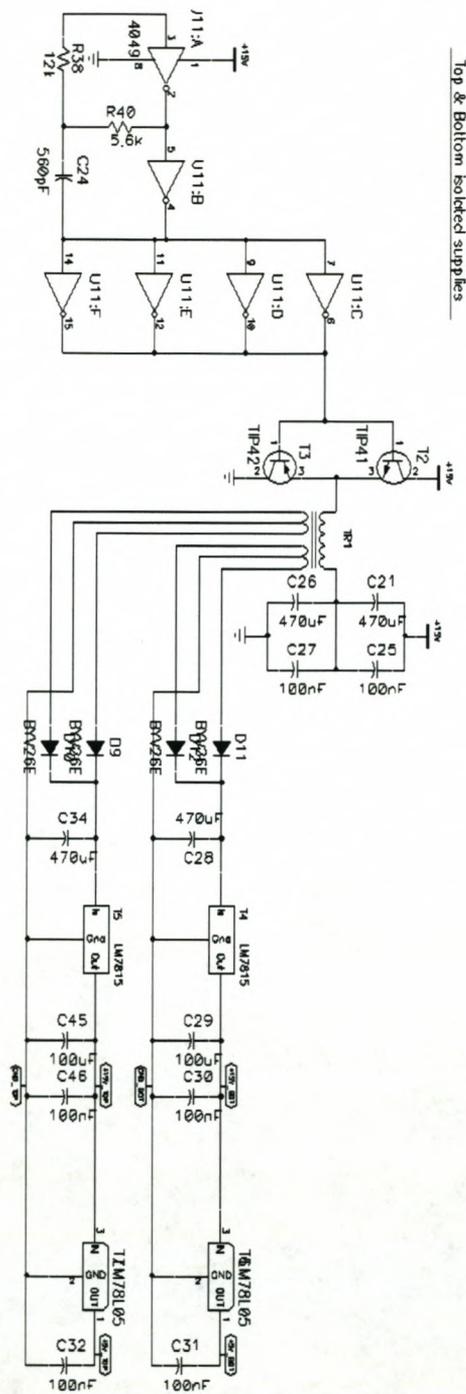
Figure A-1: Isolated power supply to the gate-drive ICs

APPENDIX B

B.1 VHDL program for sign detection and over-current protection

```
------------------------------------------------------------------------
--Fault and sign detection of AC-to-AC converter
--F&S.tdf
--C van Schalkwyk
--11/06/2002
--version 1
------------------------------------------------------------------------
--This block decides which switches should be switched by detecting
the sing detector's input and the
--fault signal.
------------------------------------------------------------------------


library IEEE;
use IEEE.std_logic_1164.all;

entity seind_if is
port (digi_sign, c_fault, clk, reset      :in   std_logic;
       PWM_TI, PWM_BI                  :in     std_logic_vector(3   downto
0);
       PWM_TO, PWM_BO                  :out    std_logic_vector(3   downto
0));
end seind_if;

architecture behavior of seind_if is
signal a, trig :std_logic := '0';

begin
  puls: process (reset, trig)
  begin
      if (trig = '1') then
             trig <= '0';
```

```
      elsif (reset'event) and (reset = '1') then
           trig <= '1';
      end if;
end process;


hoof: process (clk, trig)
begin
PWM_BO(0) <= PWM_BI(0);
PWM_TO(1) <= PWM_TI(1);
PWM_TO(2) <= PWM_TI(2);
PWM_BO(3) <= PWM_BI(3);


if (trig = '1') then
  a <= '0';
elsif (clk'event) and (clk='1') then
    if (a = '0') then
         if (c_fault = '1') then
                a <= '1';
                if (digi_sign = '1') then
                     PWM_TO(0) <= '1';
                     PWM_BO(1) <= '1';
                     PWM_BO(2) <= '0';
                     PWM_TO(3) <= '0';
                else
                     PWM_TO(0) <= '0';
                     PWM_BO(1) <= '0';
                     PWM_BO(2) <= '1';
                     PWM_TO(3) <= '1';
                end if;
        else
                if (digi_sign = '1') then
                     PWM_TO(0) <= PWM_TI(0);
                     PWM_BO(1) <= PWM_BI(1);
                     PWM_BO(2) <= '0';
                     PWM_TO(3) <= '0';
                else
                     PWM_TO(0) <= '0';
                     PWM_BO(1) <= '0';
                     PWM_BO(2) <= PWM_BI(2);
                     PWM_TO(3) <= PWM_TI(3);
```

```
                    end if;
              end if;
        else
              if (digi_sign = '1') then
                    PWM_TO(0) <= '1';
                    PWM_BO(1) <= '1';
                    PWM_BO(2) <= '0';
                    PWM_TO(3) <= '0';
              else
                    PWM_TO(0) <= '0';
                    PWM_BO(1) <= '0';
                    PWM_BO(2) <= '1';
                    PWM_TO(3) <= '1';
              end if;
        end if;
  end if;
  end process;
end behavior;
```

B.2 C program for control by RMS computation

```
/*__[ main.c ]_____

    PEC31 support library example

    - function
      - compute RMS of input voltage
        - read data from A-to-D
        - reference to PWM blocks

    written by
      A.D. le Roux

    adapted by
    C van Schalkwyk


    _____*/

#define _C_MAIN

#include <math.h>
#include <float.h>
#include <limits.h>
#include <string.h>
#include "type.h"
#include "c3x.h"
```

```
#include "dac8413.h"
#include "ad7891.h"
#include "pwm.h"
#include "lcd.h"

/*__global variables PWM_____*/
FLOAT    dA, dB, dC, dD;

FLOAT    D = 0.0;

UINT     bstate;

/*__Switching period & blanking time__*/

#define Ts    (200e-6)
#define Td    (3.0e-6)
#define Tf    (9.0909e-3)

/*__global variables RMS_____*/

int plus_min, plus_min_1;
int    N  =   0;
FLOAT    Som1  =    0.0;

/*__global variables A/D_____*/

FLOAT    meetsein;
C3X_TIMER_EVENT c3x_timer_example;
C3X_TIMER_EVENT ad7891_timer;

/*__addres for digital input_____*/

volatile int *PB = (volatile int *) 0x700089;

/*_____*/

void main()
{
    /*__run at 1 wait-state__*/
    *p_c3x_reg_pbc            =    (3<<3) | (1<<5);
    /*__enable instruction cache__*/
    asm(" or  0800h,st");

    /*__ADCs to standby__*/
    *((VUINT*)0x700000) =    (AD7891_CNTRL_STBY)<<20;
    *((VUINT*)0x700001) =    (AD7891_CNTRL_STBY)<<20;
    *((VUINT*)0x700002) =    (AD7891_CNTRL_STBY)<<20;
    *((VUINT*)0x700003) =    (AD7891_CNTRL_STBY)<<20;

    lcd_init();

    /*__startup PEC31 PWM__*/
    /*__trigger watch dog__*/
    pec31_FPGA_reg->wr.WDTimer  =    2;
    /*__init PWM__*/
    _pec31_FPGA_PWM_init( &pec31_FPGA_PWM[0], Ts, Td );
    _pec31_FPGA_PWM_init( &pec31_FPGA_PWM[1], Ts, Td );
    /*__setup timing__*/
    pec31_FPGA_PWM[0].p_reg->wr.compare[0]      =    100;
    pec31_FPGA_PWM[1].p_reg->wr.compare[0]      =    100;
    /*__setup error feedback: 0x1FF=no feedbacks checked!__*/
```

```
        pec31_FPGA_PWM[0].p_reg->wr.error_mask      =    0x01FF;
        pec31_FPGA_PWM[1].p_reg->wr.error_mask      =    0x01FF;
        /*__clear error feedback__*/
        pec31_FPGA_PWM[0].p_reg->rd.error_status;
        pec31_FPGA_PWM[1].p_reg->rd.error_status;
        /*__set all duty cycles to 50% and enable PWM__*/
        _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[0], 0, 1 );
        _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[0], 1, 0 );
        _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[0], 2, 0 );
        _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[0], 3, 1 );
        _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[1], 0, 1 );
        _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[1], 1, 0 );
        _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[1], 2, 0 );
        _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[1], 3, 1 );
         pec31_FPGA_reg->wr.PWM_control        =    0x33;


        /*__set adc_____*/

        /*  start c3x timer 0   */
        p_c3x_timer[0]->period     =    0xffffffff;
        p_c3x_timer[0]->control    =    C3X_TIMER_CONTROL_GO
                                   |    C3X_TIMER_CONTROL_nHLD
                                   |    C3X_TIMER_CONTROL_CLKSRC;

        _c3x_timer_event( &c3x_timer_example, 0 );
        _c3x_timer_event( &ad7891_timer, 0 );
        _c3x_timer_event_set_time( &c3x_timer_example, 200.0e-6 );

/*_____*/

        /*__wait for zero-crossing__*/

        /*__read digital value__*/
        plus_min_1 = *PB;
        plus_min_1 = plus_min_1&0x01;

        plus_min = *PB;
        plus_min = plus_min&0x01;

        while ( plus_min_1 == plus_min )
        {
         plus_min = *PB;
         plus_min = plus_min&0x01;
        }

        plus_min_1 = *PB;
        plus_min_1 = plus_min_1&0x01;

        /*__read A/D_____*/
        {
            /*__AD7891.0 => setup & convst__*/
            *((VUINT*)0x700002) =
(AD7891_CNTRL_SIGNED|AD7891_CNTRL_CONVST|AD7891_CNTRL_CH2)<<20;

            _c3x_timer_event_set_time( &ad7891_timer, AD7891_CONV_TIME );
            while (!_c3x_timer_event_check( &ad7891_timer ));

            meetsein =    (100)*(float)((*(VINT*)0x700002)>>20)*AD7891_CV;
        }
```

```
/*_____*/

        while (1)

        {
            /*__poll for end of PWM cycle__*/
            while ((pec31_FPGA_reg->rd.PWM_status & 0x010) != 0);
            while ((pec31_FPGA_reg->rd.PWM_status & 0x010) == 0);

                /*__calculate PWM refernce__*/
            {

                /*__read A/D_____*/


                    /*__AD7891.0 => setup & convst__*/
                * ((VUINT*)0x700002) =
    (AD7891_CNTRL_SIGNED|AD7891_CNTRL_CONVST|AD7891_CNTRL_CH2)<<20;

                    _c3x_timer_event_set_time( &ad7891_timer,
    AD7891_CONV_TIME );
                    while (!_c3x_timer_event_check( &ad7891_timer ));

                    meetsein =
    (100)*(float)((*(VINT*)0x700002)>>20)*AD7891_CV;
                    Som1 = Som1 + meetsein*meetsein;

                    /*__compute D_____*/

                    if (N == 100.0)
                    {
                        *PA = 1;
                        D = 230.0/(sqrt(Som1*0.01));
                        N = 0.0;
                        Som1 = 0.0;
                    }
                    else
                    {
                        N = N + 1;
                    }
                    dA = D;
                    dB = D;
                    dC = D;
                    dD = D;
            }

            /*__clamping of the duty-cycles are not required here,
             *   but is included for clarity since it is output to
             *   the DAC__*/
            dA  =   ( dA < 0.0 ? 0.0 : dA );
            dA  =   ( dA > 1.0 ? 1.0 : dA );
            dB  =   ( dB < 0.0 ? 0.0 : dB );
            dB  =   ( dB > 1.0 ? 1.0 : dB );
            dC  =   ( dC < 0.0 ? 0.0 : dC );
            dC  =   ( dC > 1.0 ? 1.0 : dC );
            dD  =   ( dD < 0.0 ? 0.0 : dD );
            dD  =   ( dD > 1.0 ? 1.0 : dD );
            D   =   ( D  < 0.0 ? 0.0 : D  );
            D   =   ( D  > 1.0 ? 1.0 : D  );

            /*__update FPGA PWM registers__*/
            _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[0]), 0, dA );
```

```
            _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[0]), 1, dB );
            _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[0]), 2, dC );
            _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[0]), 3, dD );
            _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[1]), 0, dA );
            _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[1]), 1, dB );
            _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[1]), 2, dC );
            _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[1]), 3, dD );


            /*__trigger the dog__*/
            pec31_FPGA_reg->wr.WDTimer   =   2;

            /*__write current phase & duty cycles to the DAC__*/
            _dac8413_update_v( &pec31_dac8413, 0, D );
            _dac8413_update_v( &pec31_dac8413, 1, dB );
            _dac8413_update_v( &pec31_dac8413, 2, meetsein/50 );
            _dac8413_update_v( &pec31_dac8413, 3, dD );
        }
}

/*_____*/
```

B.3 C program for Open-loop control

```
/*__[ main.c ]_____

   PEC31 support library example

      - function
        - open-loop control
          - read data from A-to-D
          - reference to PWM blocks

        written by
          A.D. le Roux

        adapted by
        C van Schalkwyk


   _____*/

#define _C_MAIN

#include <math.h>
#include <float.h>
#include <limits.h>
#include <string.h>
#include "type.h"
#include "c3x.h"
#include "dac8413.h"
#include "ad7891.h"
#include "pwm.h"
#include "lcd.h"
```

```
/*__global variables PWM_____*/

FLOAT    dA, dB, dC, dD;
FLOAT    D  = 0.0;
FLOAT    DO = 0.0;


/*__Switching period & blanking time__*/

#define Ts   (200e-6)
#define Td   (3.0e-6)
#define Tf   (9.0909e-3)
#define Vref_max (325.3)
#define Vref_samplenum (100)
#define pi   (3.14159)

/*__global variables D_____*/

int plus_min, plus_min_1;
FLOAT Vref[100];
int      index    =    0;
int      N        =    0;
FLOAT    ans, verskil;
FLOAT    Som1      =    0.0;
FLOAT    Som2      =    0.0;

/*__global variables A/D_____*/

FLOAT    outputv1, inputv1, meetkon, outputv, inputv;

C3X_TIMER_EVENT c3x_timer_example;
C3X_TIMER_EVENT ad7891_timer;

/*__addres for digital input/output_____*/

volatile int *PB = (volatile int *) 0x700089;

/*_____*/
void main()
{
    /*__run at 1 wait-state__*/
    *p_c3x_reg_pbc               =    (3<<3) | (1<<5);
    /*__enable instruction cache__*/
    asm(" or  0800h,st");

    /*__ADCs to standby__*/
    *((VUINT*)0x700000) =    (AD7891_CNTRL_STBY)<<20;
    *((VUINT*)0x700001) =    (AD7891_CNTRL_STBY)<<20;
    *((VUINT*)0x700002) =    (AD7891_CNTRL_STBY)<<20;
    *((VUINT*)0x700003) =    (AD7891_CNTRL_STBY)<<20;

    /*__startup PEC31 PWM__*/
    /*__trigger watch dog__*/
    pec31_FPGA_reg->wr.WDTimer   =    2;
    /*__init PWM__*/
    _pec31_FPGA_PWM_init( &pec31_FPGA_PWM[0], Ts, Td );
    _pec31_FPGA_PWM_init( &pec31_FPGA_PWM[1], Ts, Td );
    /*__setup timing__*/
    pec31_FPGA_PWM[0].p_reg->wr.compare[0]      =    100;
    pec31_FPGA_PWM[1].p_reg->wr.compare[0]      =    100;
```

Appendix B

```
/*__setup error feedback: 0x1FF=no feedbacks checked!__*/
pec31_FPGA_PWM[0].p_reg->wr.error_mask      =    0x01FF;
pec31_FPGA_PWM[1].p_reg->wr.error_mask      =    0x01FF;
/*__clear error feedback__*/
pec31_FPGA_PWM[0].p_reg->rd.error_status;
pec31_FPGA_PWM[1].p_reg->rd.error_status;
/*__set all duty cycles to 50% and enable PWM__*/
_pec31_FPGA_PWM_update( &pec31_FPGA_PWM[0], 0, 1 );
_pec31_FPGA_PWM_update( &pec31_FPGA_PWM[0], 1, 0 );
_pec31_FPGA_PWM_update( &pec31_FPGA_PWM[0], 2, 0 );
_pec31_FPGA_PWM_update( &pec31_FPGA_PWM[0], 3, 1 );
_pec31_FPGA_PWM_update( &pec31_FPGA_PWM[1], 0, 1 );
_pec31_FPGA_PWM_update( &pec31_FPGA_PWM[1], 1, 0 );
_pec31_FPGA_PWM_update( &pec31_FPGA_PWM[1], 2, 0 );
_pec31_FPGA_PWM_update( &pec31_FPGA_PWM[1], 3, 1 );
 pec31_FPGA_reg->wr.PWM_control        =    0x33;


/*  run at 1 wait-state  */
*p_c3x_reg_pbc             =    (3<<3) | (1<<5);

/*  start c3x timer 0    */
p_c3x_timer[0]->period     =    0xffffffff;
p_c3x_timer[0]->control    =    C3X_TIMER_CONTROL_GO
                           |    C3X_TIMER_CONTROL_nHLD
                           |    C3X_TIMER_CONTROL_CLKSRC;

_c3x_timer_event( &c3x_timer_example, 0 );
_c3x_timer_event( &ad7891_timer, 0 );
_c3x_timer_event_set_time( &c3x_timer_example, 200.0e-6 );
/*_____*/

    for (index = 0; index < Vref_samplenum; index++)
    {
        ans = Vref_max*sin((2.0*pi*index)/(Vref_samplenum));
        Vref[index] = ans;
    }

    index = 0;
/*_____*/

    /*__wait for zero-crossing__*/

    /*__read digital value__*/
    plus_min_1 = *PB;
    plus_min_1 = plus_min_1&0x01;

    plus_min = *PB;
    plus_min = plus_min&0x01;

    while ( plus_min_1 == plus_min )
    {
     plus_min = *PB;
     plus_min = plus_min&0x01;
    }

    if (plus_min&0x01)
    {
     index = 0;
```

```
        }
        else
        {
          index = 49;
        }

        plus_min_1 = plus_min;
/*_____*/

        /*__AD7891.0 => setup & convst__*/
        *((VUINT*)0x700001) =
(AD7891_CNTRL_SIGNED|AD7891_CNTRL_CONVST|AD7891_CNTRL_CH2)<<20;
        *((VUINT*)0x700002) =
(AD7891_CNTRL_SIGNED|AD7891_CNTRL_CONVST|AD7891_CNTRL_CH2)<<20;

        _c3x_timer_event_set_time( &ad7891_timer, AD7891_CONV_TIME );
        while (!_c3x_timer_event_check( &ad7891_timer ));
                outputv =
(100)*(float)((*(VINT*)0x700001)>>20)*AD7891_CV;
                inputv =
(100)*(float)((*(VINT*)0x700002)>>20)*AD7891_CV;

/*_____*/

        while (1)
        {

            /*__poll for end of PWM cycle__*/
            while ((pec31_FPGA_reg->rd.PWM_status & 0x01) != 0)
        {
            /*__read A/D_____*/

                /*__AD7891.0 => setup & convst__*/
                *((VUINT*)0x700001) =
(AD7891_CNTRL_SIGNED|AD7891_CNTRL_CONVST|AD7891_CNTRL_CH2)<<20;
                *((VUINT*)0x700002) =
(AD7891_CNTRL_SIGNED|AD7891_CNTRL_CONVST|AD7891_CNTRL_CH2)<<20;

                _c3x_timer_event_set_time( &ad7891_timer,
AD7891_CONV_TIME );
                while (!_c3x_timer_event_check( &ad7891_timer ));

                outputv1 =
(100)*(float)((*(VINT*)0x700001)>>20)*AD7891_CV;
                inputv1 =
(100)*(float)((*(VINT*)0x700002)>>20)*AD7891_CV;
                Som2 = Som2 + inputv1;
                N++;
        }
            while ((pec31_FPGA_reg->rd.PWM_status & 0x01) == 0)
        {
            /*__read A/D_____*/

                /*__AD7891.0 => setup & convst__*/
                *((VUINT*)0x700001) =
(AD7891_CNTRL_SIGNED|AD7891_CNTRL_CONVST|AD7891_CNTRL_CH2)<<20;
                *((VUINT*)0x700002) =
(AD7891_CNTRL_SIGNED|AD7891_CNTRL_CONVST|AD7891_CNTRL_CH2)<<20;
```

```
              _c3x_timer_event_set_time( &ad7891_timer,
AD7891_CONV_TIME );
              while (!_c3x_timer_event_check( &ad7891_timer ));

              outputv1 =
(100)*(float)((*(VINT*)0x700001)>>20)*AD7891_CV;
              inputv1  =
(100)*(float)((*(VINT*)0x700002)>>20)*AD7891_CV;
          Som2 = Som2 + inputv1;
          N++;
      }

          /*__calculate PWM refernce D__*/
      {
          inputv = Som2/N;
          N = 0.0;
          Som2 = 0.0;

          meetkon = inputv;

          plus_min = *PB;
          plus_min = plus_min&0x01;

            if (plus_min_1 < plus_min)
                {
                index = 1;
                }
                else
          {
                if (index == 99)
                {
                        index = 0.0;
                }
                else
                        {
                        index++;
                        }
          }

          plus_min_1 = plus_min;

          if (inputv == 0)
          {
                inputv = meetkon;
          }
          else
          {
                inputv = inputv;
          }

          D = Vref[index]/inputv;

          if ((index == 44.0)|(index == 94.0))
          {
                DO = Som1*0.02703;
          }

          if (((index>=44)&(index<=56))|(index>=94)|(index<=6))
          {
                D = DO;
                Som1 = 0.0;
```

```
            }
            else
            {
                  D = D;
            }

            Som1 = Som1 + D;

            dA = D;
            dB = D;
            dC = D;
            dD = D;
      }

      /*__clamping of the duty-cycles are not required here,
       *  but is included for clarity since it is output to
       *  the DAC__*/
      dA  =    ( dA < 0.0 ? 0.0 : dA );
      dA  =    ( dA > 1.0 ? 1.0 : dA );
      dB  =    ( dB < 0.0 ? 0.0 : dB );
      dB  =    ( dB > 1.0 ? 1.0 : dB );
      dC  =    ( dC < 0.0 ? 0.0 : dC );
      dC  =    ( dC > 1.0 ? 1.0 : dC );
      dD  =    ( dD < 0.0 ? 0.0 : dD );
      dD  =    ( dD > 1.0 ? 1.0 : dD );
      D   =    ( D  < 0.0 ? 0.0 : D  );
      D   =    ( D  > 1.0 ? 1.0 : D  );
      DO  =    ( DO < 0.0 ? 0.0 : DO );
      DO  =    ( DO > 1.0 ? 1.0 : DO );


      /*__update FPGA PWM registers__*/
      _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[0]), 0, dA );
      _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[0]), 1, dB );
      _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[0]), 2, dC );
      _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[0]), 3, dD );
      _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[1]), 0, dA );
      _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[1]), 1, dB );
      _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[1]), 2, dC );
      _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[1]), 3, dD );

      /*__trigger the dog__*/
      pec31_FPGA_reg->wr.WDTimer  =   2;

            _dac8413_update_v( &pec31_dac8413, 0,
Vref[index]/Vref_max );
            _dac8413_update_v( &pec31_dac8413, 1, inputv*0.01 );
            _dac8413_update_v( &pec31_dac8413, 2, D );
            _dac8413_update_v( &pec31_dac8413, 3, plus_min );
      }
}

/*_____*/
```

B.4 C program for Closed-loop control

```
/*__[ main.c ]_____

   PEC31 support library example

      - function
        - closed-loop control
          - read data from A-to-D
          - reference to PWM blocks

        written by
          A.D. le Roux

        adapted by
        C van Schalkwyk


                                                                */

#define _C_MAIN

#include <math.h>
#include <float.h>
#include <limits.h>
#include <string.h>
#include "type.h"
#include "c3x.h"
#include "dac8413.h"
#include "ad7891.h"
#include "pwm.h"
#include "lcd.h"

/*__global variables PWM_____*/

FLOAT    dA, dB, dC, dD;
FLOAT    D  = 0.0;
FLOAT    DO = 0.0;


/*__Switching period & blanking time__*/

#define Ts  (200e-6)
#define Td  (3.0e-6)
#define Tf  (9.0909e-3)
#define Vref_max (325.27)
#define Vref_samplenum (100)
#define pi   (3.14159)

/*__global variables D_____*/

int plus_min, plus_min_1;
FLOAT Vref[100];
int    index    =    0;
int    N        =    0;
FLOAT   ans, verskil;
FLOAT   Som1     =    0.0;
FLOAT   Som2     =    0.0;
FLOAT   Som3     =    0.0;
```

```
/*__global variables A/D_____*/

FLOAT    outputv1, inputv1, meetkon, outputv, inputv;

C3X_TIMER_EVENT c3x_timer_example;
C3X_TIMER_EVENT ad7891_timer;

/*__addres for digital input/output_____*/

volatile int *PB = (volatile int *) 0x700089;

/*_____*/
void main()
{

    /*__run at 1 wait-state__*/
    *p_c3x_reg_pbc                 =    (3<<3) | (1<<5);
    /*__enable instruction cache__*/
    asm(" or   0800h,st");

    /*__ADCs to standby__*/
    *((VUINT*)0x700000) =    (AD7891_CNTRL_STBY)<<20;
    *((VUINT*)0x700001) =    (AD7891_CNTRL_STBY)<<20;
    *((VUINT*)0x700002) =    (AD7891_CNTRL_STBY)<<20;
    *((VUINT*)0x700003) =    (AD7891_CNTRL_STBY)<<20;

    /*__startup PEC31 PWM__*/
    /*__trigger watch dog__*/
    pec31_FPGA_reg->wr.WDTimer  =    2;
    /*__init PWM__*/
    _pec31_FPGA_PWM_init( &pec31_FPGA_PWM[0], Ts, Td );
    _pec31_FPGA_PWM_init( &pec31_FPGA_PWM[1], Ts, Td );
    /*__setup timing__*/
    pec31_FPGA_PWM[0].p_reg->wr.compare[0]      =    100;
    pec31_FPGA_PWM[1].p_reg->wr.compare[0]      =    100;
    /*__setup error feedback: 0x1FF=no feedbacks checked!__*/
    pec31_FPGA_PWM[0].p_reg->wr.error_mask      =    0x01FF;
    pec31_FPGA_PWM[1].p_reg->wr.error_mask      =    0x01FF;
    /*__clear error feedback__*/
    pec31_FPGA_PWM[0].p_reg->rd.error_status;
    pec31_FPGA_PWM[1].p_reg->rd.error_status;
    /*__set all duty cycles to 50% and enable PWM__*/
    _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[0], 0, 1 );
    _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[0], 1, 0 );
    _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[0], 2, 0 );
    _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[0], 3, 1 );
    _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[1], 0, 1 );
    _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[1], 1, 0 );
    _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[1], 2, 0 );
    _pec31_FPGA_PWM_update( &pec31_FPGA_PWM[1], 3, 1 );
     pec31_FPGA_reg->wr.PWM_control       =    0x33;

    /* run at 1 wait-state  */
    *p_c3x_reg_pbc                 =    (3<<3) | (1<<5);

    /* start c3x timer 0  */
    p_c3x_timer[0]->period    =    0xffffffff;
    p_c3x_timer[0]->control   =    C3X_TIMER_CONTROL_GO
                                 | C3X_TIMER_CONTROL_nHLD
                                 | C3X_TIMER_CONTROL_CLKSRC;
```

```
        _c3x_timer_event( &c3x_timer_example, 0 );
        _c3x_timer_event( &ad7891_timer, 0 );
        _c3x_timer_event_set_time( &c3x_timer_example, 200.0e-6 );

/*_____*/

        for (index = 0; index < Vref_samplenum; index++)
        {
                ans = Vref_max*sin((2.0*pi*index)/(Vref_samplenum));
                Vref[index] = ans;
        }

        index = 0;

/*_____*/

        /*__wait for zero-crossing__*/

        /*__read digital value__*/
        plus_min_1 = *PB;

        plus_min_1 = plus_min_1&0x01;

        plus_min = *PB;
        plus_min = plus_min&0x01;

        while ( plus_min_1 == plus_min )
        {
         plus_min = *PB;
         plus_min = plus_min&0x01;
        }

        if (plus_min&0x01)
        {
         index = 0;
        }
        else
        {
         index = 49;
        }

        plus_min_1 = plus_min;

/*_____*/

        /*__AD7891.0 => setup & convst__*/
        *((VUINT*)0x700001) =
(AD7891_CNTRL_SIGNED|AD7891_CNTRL_CONVST|AD7891_CNTRL_CH2)<<20;
        *((VUINT*)0x700002) =
(AD7891_CNTRL_SIGNED|AD7891_CNTRL_CONVST|AD7891_CNTRL_CH2)<<20;

        _c3x_timer_event_set_time( &ad7891_timer, AD7891_CONV_TIME );
        while (!_c3x_timer_event_check( &ad7891_timer ));

/*_____*/

        while (1)
        {

            /*__poll for end of PWM cycle__*/
```

```
            while ((pec31_FPGA_reg->rd.PWM_status & 0x01) != 0)
        {
                /*__read A/D_____*/

                    /*__AD7891.0 => setup & convst__*/
                *((VUINT*)0x700001) =
(AD7891_CNTRL_SIGNED|AD7891_CNTRL_CONVST|AD7891_CNTRL_CH2)<<20;
                *((VUINT*)0x700002) =
(AD7891_CNTRL_SIGNED|AD7891_CNTRL_CONVST|AD7891_CNTRL_CH2)<<20;

                    _c3x_timer_event_set_time( &ad7891_timer,
AD7891_CONV_TIME );
                while (!_c3x_timer_event_check( &ad7891_timer ));

                    outputv1 =
(100)*(float)((*(VINT*)0x700001)>>20)*AD7891_CV;
                    inputv1  =
(100)*(float)((*(VINT*)0x700002)>>20)*AD7891_CV;
                Som2 = Som2 + inputv1;
                Som3 = Som3 + outputv1;
                N++;
        }
            while ((pec31_FPGA_reg->rd.PWM_status & 0x01) == 0)
        {
                /*__read A/D_____*/

                    /*__AD7891.0 => setup & convst__*/
                *((VUINT*)0x700001) =
(AD7891_CNTRL_SIGNED|AD7891_CNTRL_CONVST|AD7891_CNTRL_CH2)<<20;
                *((VUINT*)0x700002) =
(AD7891_CNTRL_SIGNED|AD7891_CNTRL_CONVST|AD7891_CNTRL_CH2)<<20;

                    _c3x_timer_event_set_time( &ad7891_timer,
AD7891_CONV_TIME );
                while (!_c3x_timer_event_check( &ad7891_timer ));

                    outputv1 =
(100)*(float)((*(VINT*)0x700001)>>20)*AD7891_CV;
                    inputv1  =
(100)*(float)((*(VINT*)0x700002)>>20)*AD7891_CV;
                Som2 = Som2 + inputv1;
                Som3 = Som3 + outputv1;
                N++;
        }

                /*__calculate PWM refernce D__*/
        {
                inputv = Som2/N;
                outputv = Som3/N;
                N = 0.0;
                Som2 = 0.0;
                Som3 = 0.0;

                /*__read digital value*/
                plus_min = *PB;
                plus_min = plus_min&0x01;

                    if (plus_min_1 < plus_min)
                        {
                        index = 1;
                        }
```

```
                else
        {
                if (index == 99)
                {
                        index = 0.0;
                }
                else
                        {
                        index++;
                        }
        }

        plus_min_1 = plus_min;

        if (inputv==0)
        {
                inputv = meetkon;
        }
        else
        {
                inputv = inputv;
        }
        meetkon = inputv;

        verskil = Vref[index]*4.33 - outputv;
        D = verskil*0.3/inputv;

        if ((index == 42.0)|(index == 92.0))
        {
                DO = Som1*0.03030;
        }


        if (((index>=42)&(index<=58))|(index>=92)|(index<=8))
        {
                D = DO;
                Som1 = 0.0;
        }
        else
        {
                D = D;
        }

        Som1 = Som1 + D;

        dA = D;
        dB = D;
        dC = D;
        dD = D;
}

/*__clamping of the duty-cycles are not required here,
 * but is included for clarity since it is output to
 * the DAC__*/
dA  =    ( dA < 0.0 ? 0.0 : dA );
dA  =    ( dA > 1.0 ? 1.0 : dA );
dB  =    ( dB < 0.0 ? 0.0 : dB );
dB  =    ( dB > 1.0 ? 1.0 : dB );
dC  =    ( dC < 0.0 ? 0.0 : dC );
dC  =    ( dC > 1.0 ? 1.0 : dC );
dD  =    ( dD < 0.0 ? 0.0 : dD );
```

```
        dD  =   ( dD > 1.0 ? 1.0 : dD );
        D   =   ( D  < 0.0 ? 0.0 : D  );
        D   =   ( D  > 1.0 ? 1.0 : D  );

        /*__update FPGA PWM registers__*/
        _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[0]), 0, dA );
        _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[0]), 1, dB );
        _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[0]), 2, dC );
        _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[0]), 3, dD );
        _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[1]), 0, dA );
        _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[1]), 1, dB );
        _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[1]), 2, dC );
        _pec31_FPGA_PWM_update( &(pec31_FPGA_PWM[1]), 3, dD );

        /*__trigger the dog__*/
        pec31_FPGA_reg->wr.WDTimer  =   2;

            _dac8413_update_v( &pec31_dac8413, 0, inputv/100 );
            _dac8413_update_v( &pec31_dac8413, 1, outputv/100 );
            _dac8413_update_v( &pec31_dac8413, 2, D );
            _dac8413_update_v( &pec31_dac8413, 3,
Vref[index]/Vref_max );
    }
}

/*_____*/
```