The Experimental Design and Characterisation of Doherty Power Amplifiers

Konrad Frederik Brand

Thesis presented in partial fulfilment of the requirements for the degree of Master of Science at Stellenbosch University

Study supervisor: *Dr. Cornell van Niekerk* Date: *December 2006*

Declaration: I, the undersigned, hereby declare that the work contained in this thesis is my own original work and that I have not previously in its entirety or in part submitted it at any university for a degree.

Signed:

Date:

Abstract

Modern day digital modulation techniques in communication systems produce large peak-to-average ratios. To maintain linearity, power amplifiers have to operate at backed-off levels. This results in low efficiency with consequences such as high power consumption, short battery life and excessive heat in power amplifiers. A Doherty amplifier is an efficiency enhancement technique which increases an amplifier's efficiency at backed-off levels.

This thesis presents a design procedure for a Classical Doherty amplifier. A method where S-parameter measurements from a transistor are used to predict the transistor's transmission phase response for varying input power is presented. This method is found to be accurate by comparing it to measurements done on a non-linear network analyser. The measured S-parameters are also used to design the Doherty amplifier at its predicted peak output power.

Two Classical Doherty amplifiers are designed, manufactured and characterised. The measurements are performed on a custom measurement setup using in-house developed Matlab code to automate the measurements. The first Doherty amplifier used small-signal Siemens CFY30 GaAs FETs and the second Doherty amplifier used 10W Motorola MRF282 LDMOS transistors. The performance of both amplifiers is compared to similar balanced amplifiers and shows improvements in their efficiency.

The improvement in efficiency for the 10W Doherty power amplifier in relation to a balanced amplifier is compared to results found in the literature and a good correspondence between the measured and published results were obtained.

Opsomming

Hedendaagse digitale moduleringstegnieke in kommunikasie toepassings het groot piek-tot-gemiddelde verhoudings. Om lineariteit te behou moet drywingsversterkers by laer drywingsvlakke bedryf word. Dit het ‘n verlaging in doeltreffendheid tot gevolg wat kan lei tot verkorte batteryleeftyd, hoë drywingsverkwisting en oormatige hitte in die drywingsversterker. ’n Doherty versterker is ’n metode om doeltreffendheid by verlaagde drywingsvlakke te verbeter.

Hierdie tesis bied ’n ontwerpsprosedure vir ’n Klassieke Doherty versterker. ’n Metode waar gemete S-parameters van ’n transistor gebruik word om sy transmissie fase weergawe teenoor intreedrywing te voorspel, word voorgestel. Die akkuraatheid van hierdie metode is bewys deur die voorspelde fase weergawe te vergelyk met metings wat met ’n nie-lineêre vektoranaliseerder gedoen is. Die gemete S-parameters is ook gebruik in die ontwerp van ’n Doherty versterker by sy verwagte maksimum uittreedrywing.

Twee Klassieke Doherty versterkers is ontwerp, gebou en gemeet. Die metings is gedoen op ’n spesiaal aangepaste meetopstelling met selfontwikkelde Matlab sagteware wat die metings outomatiseer. Die eerste Doherty versterker maak gebruik van klein-sein Siemens CFY30 GaAs FET transistors en die tweede Doherty versterker van 10W Motorola MRF282 LDMOS transistors. Beide versterkers se werkverrigting is vergelyk met soortgelyke gebalanseerde versterkers en toon ’n verbetering in doeltreffendheid.

Die verbetering in doeltreffendheid van die 10W Doherty drywingsversterker in vergelyking met ’n gebalanseerde versterker stem ooreen met resultate gevind in die literatuur.

Bedankings

- Die Liewe Heer wat my die krag en insig gegee het om hierdie tesis te kon skryf.
- Cornell wat altyd goeie leiding gegee het en bereid was om al my vrae te probeer antwoord.
- Wessel Croukamp en Lincoln Saunders wat ure spandeer het aan my versterkers.
- My ouers en vriende wat altyd bemoedigend was.
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Abbreviations

GaAs FET:	Gallium Arsenide Field Effect Transistor
LDMOS:	Laterally Diffused Metal Oxide Semiconductor
PEP:	peak output/envelope power (Depending whether amplitude modulation is used)
MWO:	Microwave Office©
PAE:	Power added efficiency
LINC:	Linear amplifier incorporating non-linear components
W-CDMA:	Wide-band code division multiple access

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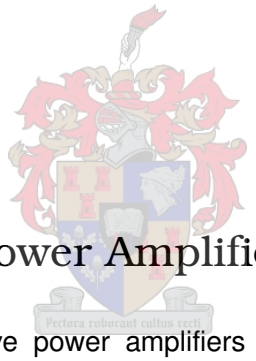
Introduction



1.1 Radio Frequency Power Amplifiers

Radio frequency (RF) and microwave power amplifiers and transmitters are utilised in various applications such as wireless communication, RF heating, jamming and radar. Each of these applications has their own unique requirements regarding frequency, bandwidth, power, load, cost, linearity and efficiency.

In communication various types of modulation are used. From basic frequency modulation (FM), amplitude modulation (AM) and phase modulation to modern day digital modulation such as wide-band code division multiple access (W-CDMA) for base-station applications. Linear amplification is required when both amplitude and phase modulation is used in a signal.

Linearity is traditionally measured by the carrier-to-intermodulation (C/I) ratio. When a power amplifier is driven with two or more tones f_1 and f_2 of equal amplitude, intermodulation products occur at frequencies corresponding to the sums and differences of multiples of the two frequencies $nf_1 \pm mf_2$.with n,m = 1, 2, 3, … . The amplitude of the third-order products occurring at $2f_1 - f_2$ and $2f_2 - f_1$ is compared to the amplitude of the tones f_1 and f_2 to obtain the C/I ratio [29].

Like linearity, efficiency is a critical factor in power amplifier design. The ratio of the RF output power to the DC power is called the drain efficiency $\eta = P_{rf}/P_{DC}$. Whereas power added efficiency (PAE) subtracts the input drive power from the output power PAE = $Prf - P_{in}/P_{DC}$. The instantaneous efficiency is the efficiency at one specific output power. The instantaneous efficiency for most power amplifiers is at its highest at its peak envelope power (PEP) and decreases as output power decreases. Amplifiers with higher efficiency are desirable for portable applications in order to extend the battery life of the system. Higher efficiency also translates to less heat being generated in an amplifier, which means smaller systems due the smaller heat sinks required. This brings along advantages such as easier installation in confined spaces such as airplanes.

Modern digital modulated signals such as W-CDMA have very large peak-to-average ratios of between 6 and 13 dB. For a power amplifier to remain linear in such a case they are operated at backed-off levels and therefore have very low efficiencies [1],[29]. Kahn's "Envelope Elimination and Restoration" (EER), Chireix outphasing method, LINC (linear amplifier incorporating non-linear components) and the Doherty amplifier are all methods to increase power amplifiers' efficiency at backed-off levels. Although all of them have higher efficiencies than the Doherty amplifier, they require much more complicated circuitry. The Doherty amplifier is therefore the best candidate, as a relatively simple efficiency enhancement technique which also complies with commercial communication standards regarding bandwidth and linearity [2].

1.2 The Scope of this Study

This thesis investigates the Doherty amplifier as an efficiency enhancement technique by designing, manufacturing and measuring two Classical[1] Doherty amplifiers.

- A literature study about Doherty amplifiers and published results is presented.
- A method of using measured S-parameters of transistors to design a Classical Doherty amplifier at the expected peak output power is proposed[2]. This method is proposed due to a lack of non-linear models which can provide accurate simulations for all modes of amplifier operation.
- The proposed method is proved to be able to predict the transmission phase response for a transistor with varying input power.
- A prototype Classical Doherty amplifier is designed and manufactured using Siemens' CFY30 small-signal GaAs FET transistors. The layout is designed so that the carrier and peaking amplifiers can be measured separately or in Doherty configuration. The carrier

[1] Classical refers two a Doherty amplifier which uses identical transistors in the carrier and peaking amplifiers [2].

[2] To the author's knowledge this method has not been described in literature

amplifier's response to load modulation is investigated by manually changing the load of the carrier amplifier.

- Finally a Doherty power amplifier using Motorola's MRF282 10W LDMOS transistors is designed, manufactured and characterised. This Doherty amplifier's measured performance is compared to published results.

1.3 Layout of this Thesis

This thesis has the following layout. Chapter 2 provides a discussion on Cripps' load-line technique. Matlab code which uses measured S-parameters to calculate the optimal load-line resistance, R_{opt}, is presented. An optimiser written in Matlab which calculates the optimal impedance, Z_{opt}, which is transformed through a transistor's external parameters is also discussed.

Chapter 3 starts with an explanation of why an amplifier's efficiency decreases with a reduction in input power. This is followed by a theoretical solution to this behaviour, and illustrates how an ideal Doherty amplifier implements this solution. A brief discussion on variations on the Classical Doherty amplifier is given, followed by an extensive discussion on the practical implications in designing a Classical Doherty amplifier.

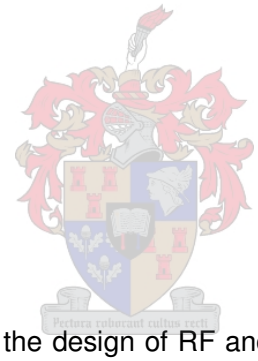
In Chapter 4 the use of measured S-parameters of a transistor to predict transmission phase response as a function of input power is explained. The design of a Classical Doherty amplifier is presented in detail. This Doherty amplifier uses small-signal GaAs FETs. The layout of the amplifier permits separate measurements of the carrier and peaking amplifier as well as in Doherty configuration. The behaviour of the carrier amplifier's compression, power, efficiency and DC curves is discussed when its load is manually interchanged with three different values. A custom measurement setup with developed software is presented. Finally the Doherty amplifier's measured performance is compared to that of a balanced amplifier.

The same design procedure presented in Chapter 4 is used in Chapter 5 to design a Classical Doherty amplifier with 10W LDMOS transistors. The measured results are compared to a balanced amplifier as well as results in existing literature.

The thesis is concluded in Chapter 6 with the final conclusions and recommendations.

Chapter 2

Load-Line Design



2.1 Introduction

Load-pull data are an integral part in the design of RF and microwave power amplifiers and shows the relationship between output power and output match. Load-pull data are normally acquired through load-pull measurements where the setup consists of a device under test with a calibrated tuneable load [1]. In 1983 Cripps showed that load-pull contours could be predicted by extending load-line principles [1]. This method is known as Cripps' load-line technique.

In this chapter the difference between load-line and conjugate matching will be explained. The use of a load-line match gives rise to the optimal resistance, R_{opt}, which will be derived through the use of Cripps' load-line technique.

Design software utilising Cripps' technique will also be introduced.

2.2Cripps' Load-Line Technique

Before we explore the load-line technique, it is necessary to repeat Cripps'[1] explanation of why conjugate matching at the output of a power amplifier is sometimes insufficient. Figure 2.2.1 shows a

source which will deliver maximum power to the load if the load impedance, R_{load}, is the conjugate of the source's internal impedance, R_{gen}. I_g is the source current and V_{out} is the voltage over the load. If it is assumed that there is no reactive part and the real parts of the load and internal impedances are equal, then it is essentially a conjugate match. Within this assumption the physical limits of the source is not taken into account. If the source has a maximum limiting current I_{max} of 1A and its internal resistance is 100 Ω, a conjugate matched load would be 100 Ω. This would require a voltage across the generator terminals of 50V. This voltage will probably exceed the maximum voltage rating, V_{max}, for a device like a transistor. Current limiting will now occur at a much lower current than its physical maximum of I_{max} (see Figure 2.2.2).

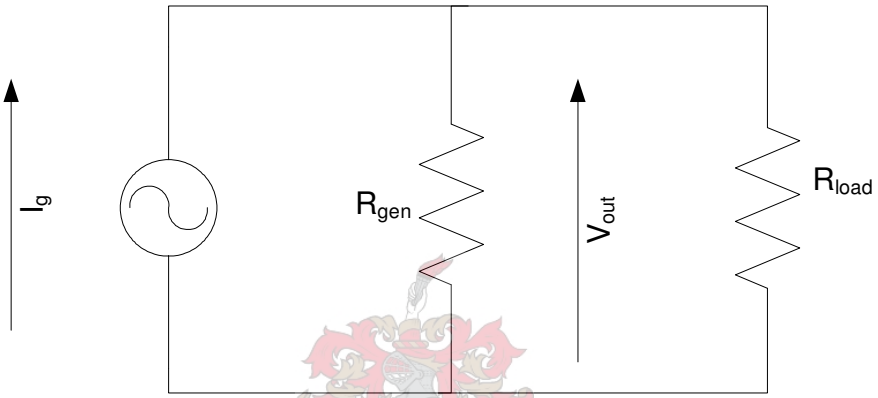


Figure 2.2.1 RF Source with an internal impedance, R_{gen} an load resistance R_{load}.

From Figure 2.2.2 it is clear that the maximum current and voltage swing of the transistor is not being used and the load resistance should be lowered. This value is known as the load-line match, R_{opt}, and is expressed as

$$R_{opt} = V_{\max} \Big/ I_{max} \tag{2.1}$$

where it is assumed that $R_{gen} >> R_{opt}$. If R_{gen} is taken into account, the equation can be solved as:

$$\frac{R_{gen}R_{opt}}{R_{gen}+R_{opt}} = \frac{V_{\max}}{I_{\max}} \tag{2.2}$$

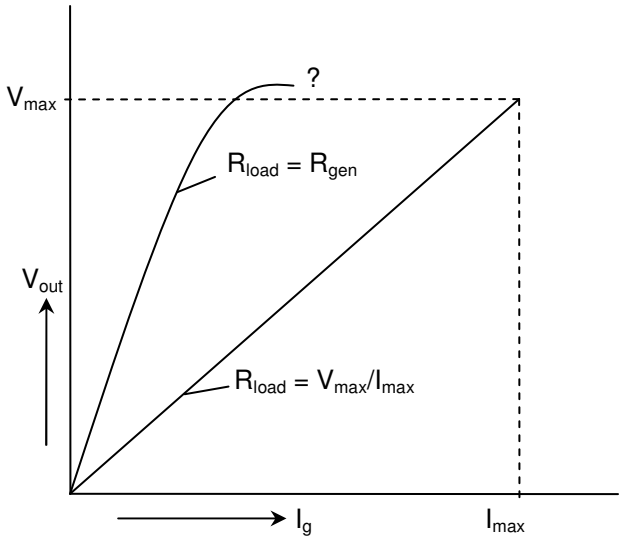


Figure 2.2.2 A conjugate match showing current limiting and load-line match utilising maximum current and voltage swing.

The conjugate match is thus for unrestricted cases, where the voltages and currents at the source terminals are unbounded by physical constraints. The load-line match is a compromise which extracts the maximum power from RF transistors by keeping the RF voltage swing within the physical limits of the device and/or the dc supply. Figure 2.2.3 shows the effect of a load-line match compared to a conjugate match. Although the load-line match has less gain than the conjugate match, the linear region is expanded.

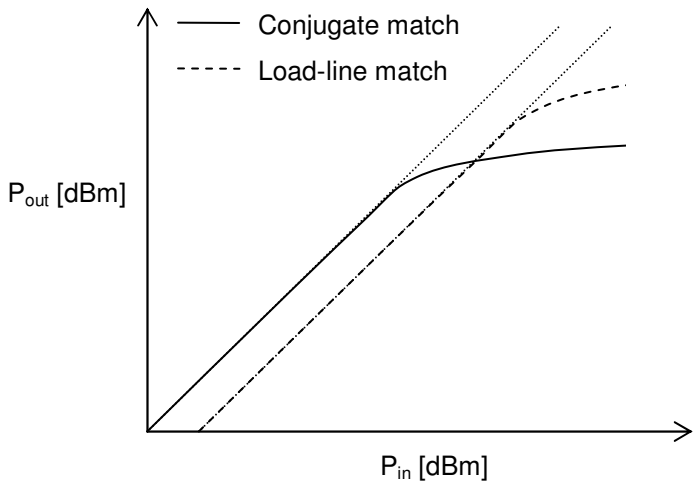


Figure 2.2.3 Load-line match vs conjugate match

Now that the use of a load-line match is explained it has to be applied to transistors. Again Cripps'[1] explanation will be provided. The idealised device model shown in Figure 2.2.4 will be used for this analysis. In the figure the device is shown as a voltage controlled current source. The transconductance is linear except for input voltages below pinch-off (V_p) and hard saturation at I_{max}. A Zero knee voltage is also assumed. At the beginning of the chapter it was explained that conjugate matching is used in the unrestricted case and that the load-line matching technique introduces a compromise in order to keep within the physical limits of the device. In this latter case the physical limits are represented by the linear region of the transconductance and thus the limits set by V_p and I_{max} may not be breached.

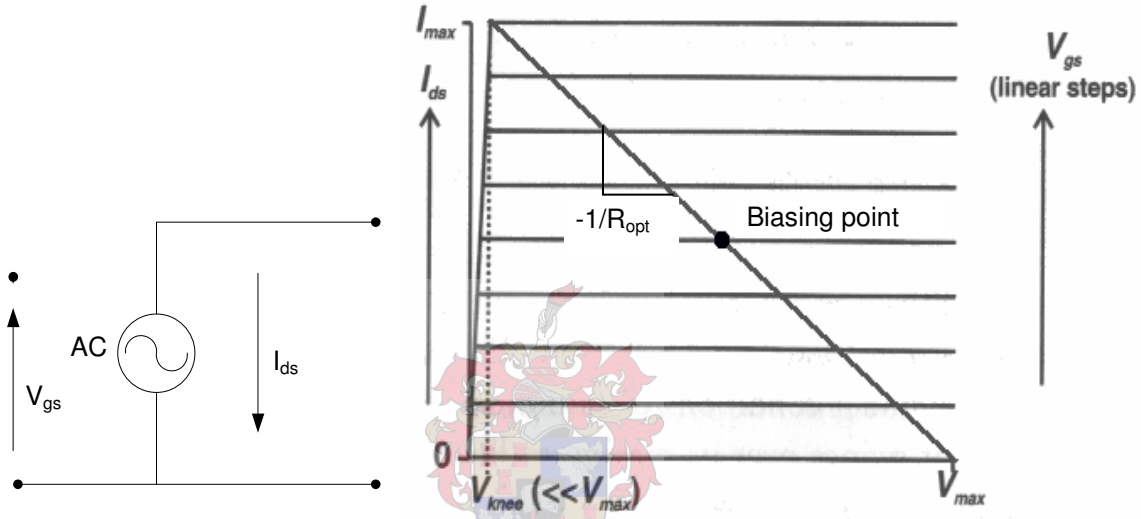


Figure 2.2.4 Ideal strongly nonlinear device model with corresponding I V-curve.

Figure 2.2.5 shows the RF circuit in which the ideal device is analyzed. The output (drain) and the RF load is AC coupled. The RF choke, through which the dc bias is fed, is assumed to have a very large reactance at the RF frequency. Unlike Cripps' method, this analysis will assume that the transistor has no output parasitics. Figure 2.2.5 also shows the RF waveforms for the device under sinusoidal excitation and optimum loading. The current swings over its maximum linear range – zero to I_{max}. That gives an amplitude of I_{max}/2. The voltage swings over its maximum range of zero to 2 V_{dc}. For this power-matched condition the load-line resistor has a value of

$$R_{opt} = \frac{V_{dc}}{I_{\max}/2} \tag{2.3}$$

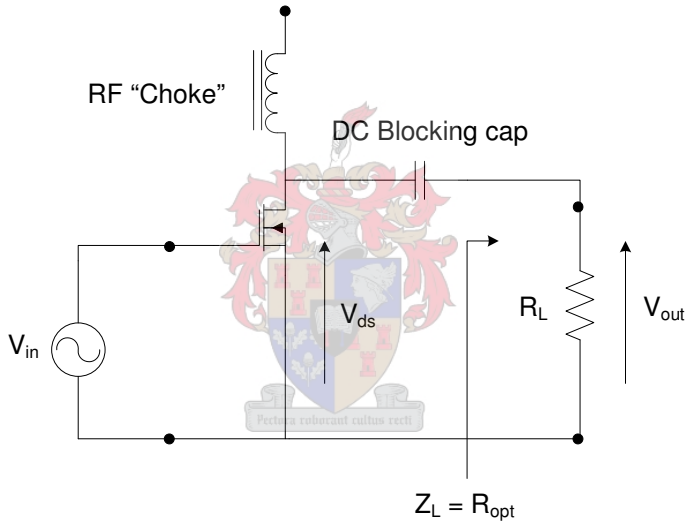
In a non ideal device, the knee voltage is not zero and the above equation becomes

$$R_{opt} = \frac{V_{dc} - V_{knee}}{I_{\max}/2} = \frac{V_{dc} - V_{knee}}{I_{dc}} \tag{2.4}$$

The load-line resistor value can be presented graphically on an I V curve as shown in Figure 2.2.4 with a gradient of -1/R_{opt}. The equations above hold only for the class A amplifier. A more general equation which is valid from class A to class C is

$$R_{opt} = \frac{V_{dc} - V_{knee}}{I_1} \tag{2.5}$$

where I_1 is the fundamental component of the drain current which differs from class to class. I_1 can be obtained by performing a Fourier analysis of the drain current waveform.



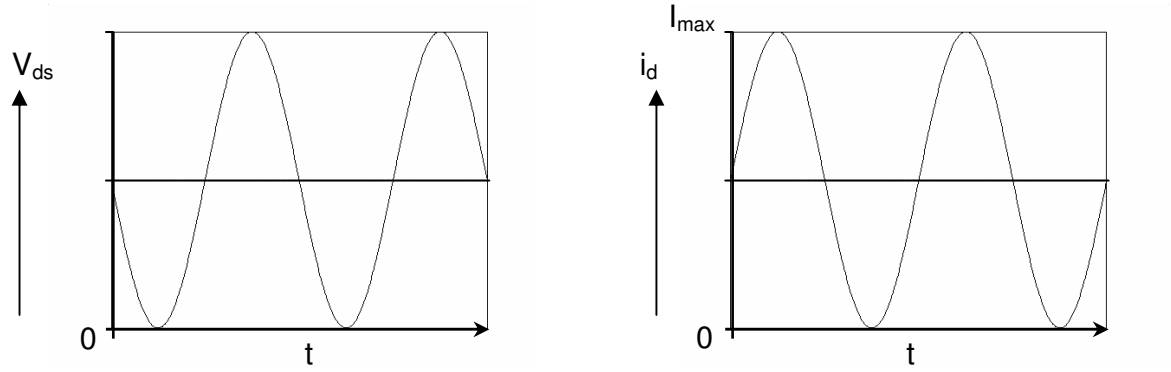


Figure 2.2.5 Class A amplifier with optimum load-line match.

2.3 Software for use with Load-Line Technique

2.3.1 Determining R_{opt} with measured I V curves

The equation for a load-line match is explained and the next step is to utilise it. If only a class A amplifier were designed, equation (2.4) would have been sufficient. The Doherty Amplifier, on the other hand, makes use of a class AB and a class C amplifier. Figure 2.3.1 shows how the different current components vary for the different classes of amplifiers – note that the fundamental component is of particular importance.

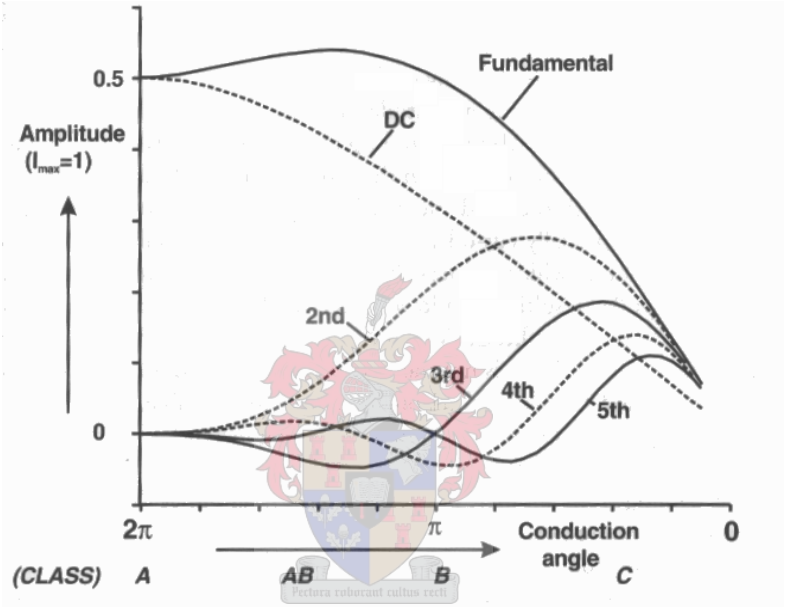


Figure 2.3.1 Current components for different class amplifiers. (after, [1])

Cripps [1] derives an equation for the fundamental component, but in this project it was approximated by using measurements of the transistor characteristics. The measurement data is processed with Matlab code and Figure 2.3.2 shows a three dimensional representation of the measurements from the Siemens CFY30 transistor. For the calculation of the fundamental current component, the I_{DS} versus V_{GS} curve at a specified drain-source voltage (V_{DS}) is used. Figure 2.3.3 shows an example of such a curve with the measured data extrapolated to the minimum rated gate voltage. The gate biasing voltage is also indicated (in this case the transistor is biased in class C mode at V_{GS} = -1.9V). The I_{DS} versus V_{GS} curve is now used as the transfer function to determine the output current waveform for a specified input voltage signal.

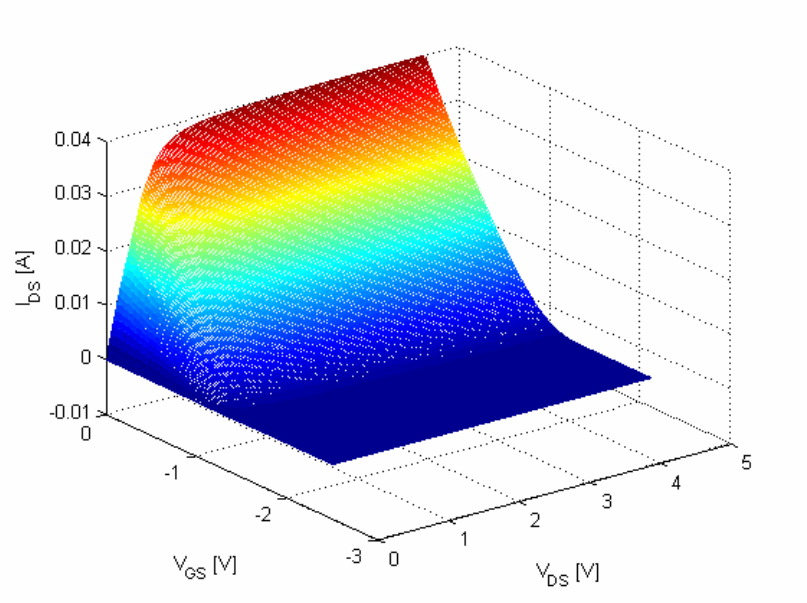


Figure 2.3.2 Measured I V-curves of a Siemens CFY30 transistor.

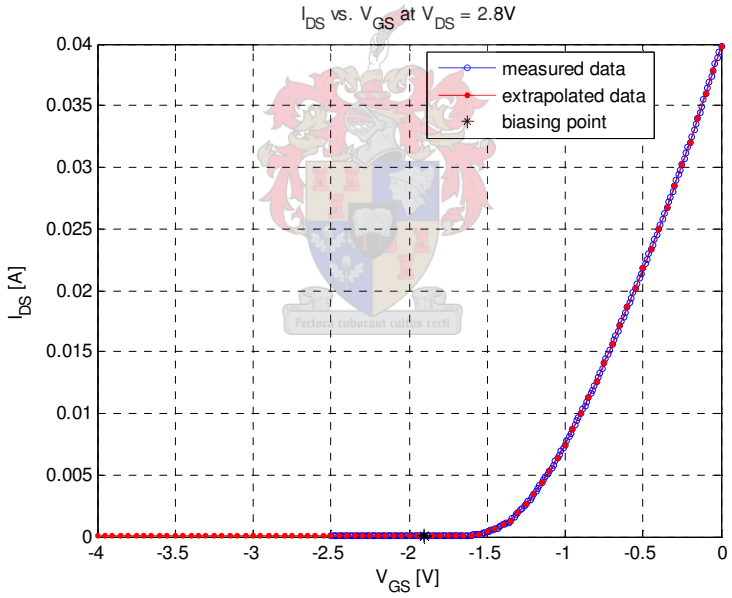


Figure 2.3.3 Measured and extrapolated I_{DS} vs. V_{GS} curve at specified V_{DS} with gate voltage indicated.

Figure 2.3.4 shows the output current for an input voltage signal with an amplitude of 1.9V. Fourier analysis is then used to determine the DC and fundamental components which is also shown in Figure 2.3.4.

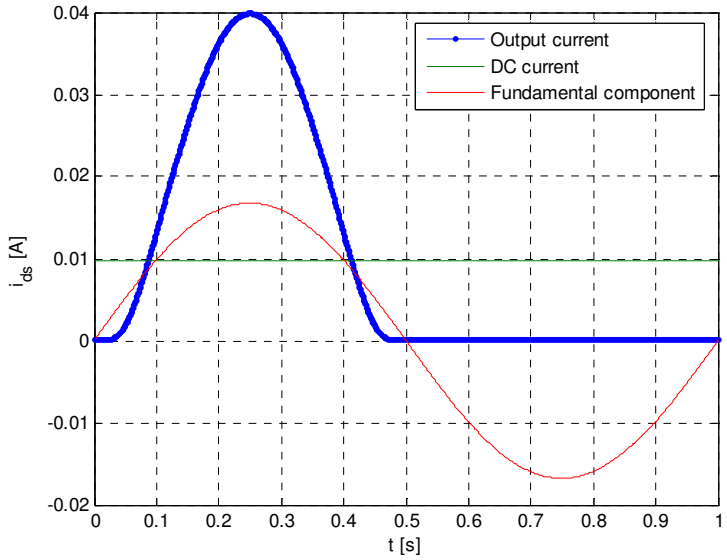


Figure 2.3.4 Output current with DC and fundamental components.

The ratio between the maximum output current and the fundamental component is calculated to be 0.4208 and the ratio between the maximum output current and the DC component may be calculated as 0.2442. These results compare well to the graph shown in Figure 2.3.1. Equation (2.5) can now be used to determine R_{opt}.

2.3.2 Determining Z_{opt} through Optimization

In Section 2.2 Cripps' load-line technique was explained at the hand of an idealised transistor model (see Figure 2.2.4). This model was said to have no parasitics. However, every transistor has parasitics, especially in RF applications.

Figure 2.3.5 shows a more practical model, with the parasitics shown as extrinsic parameters inside the dashed square. These external parameters represent the effects of the transistor packaging i.e. casing and leads. An external load and matching network is also shown. The external parameters do not change the way R_{opt} is calculated, instead, these parameters are included in the external load. To still present the current source in the model with a load of R_{opt}, the external parameters should be known and an impedance Z_{opt} must be determined that will ensure R_{opt} is seen by the current source. The extrinsic parameters are extracted using a multi-bias direct extraction method [24], where cold S-parameter data with the gate biased below pinch-off is used to determine the series extrinsic parameters.

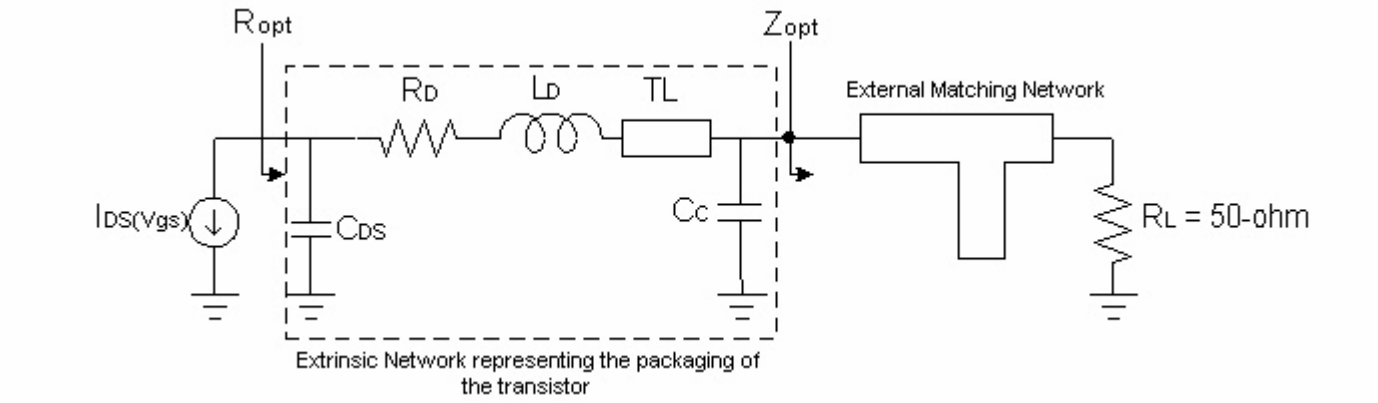


Figure 2.3.5 Transistor model with extrinsic parameters, external load and matching.

This optimal impedance is the load that the transistor package should see so that it will be transformed through the external parameters to R_{opt}, which is the load-line match the current source should see (see Figure 2.3.5). Various topologies for transistor models exist ([3]-[7]), but a resistive element in the extrinsic parameters is always present. This resistive element introduces a subtle pitfall in determining Z_{opt}. At first glance the easiest way to calculate Z_{opt} seems to be by terminating the current source's side of the extrinsic parameters with R_{opt} and then calculating the impedance seen from the other side. This impedance should then be the conjugate of Z_{opt} (see Figure 2.3.6). However, this is not entirely accurate. Because of the resistive element in the extrinsic parameters, the network is not lossless and therefore the conjugate of the calculated input impedance is only an approximation. An effective way of calculating Z_{opt} accurately is to use optimisation.

A Gauss-Newton optimisation technique as described in [8] is used. The basic theory behind any optimisation is to have a goal (in this case R_{opt}) that should be realised without the luxury of an analytical solution. This goal must now be realised by adjusting certain variables in the system (called the design variables) until the goal is met. In this case R_{opt} should be realised by adjusting R and X where $Z_{opt} = R + jX$ (see Figure 2.3.7). The biggest difference between optimisation techniques is in the way the design variables are adjusted. The Gauss-Newton method used in this project is a gradient optimisation technique. Other optimisation techniques are also described in [8].

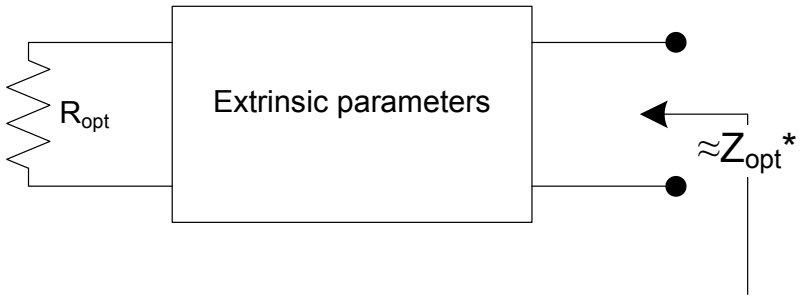


Figure 2.3.6 Determining a initial value for Z_{opt} by terminating the input with R_{opt} and taking the conjugate of the impedance seen by looking into the output.

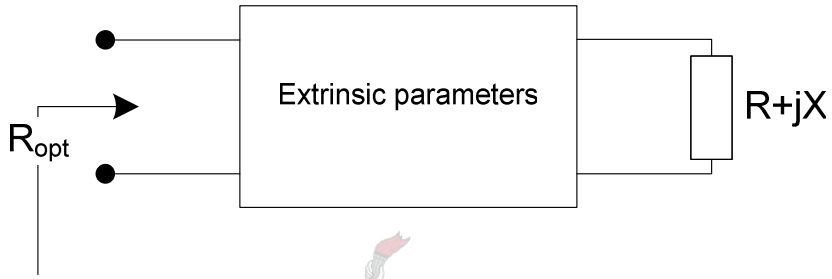


Figure 2.3.7 Optimising R_{opt}.

To start with, an error function is needed such as

$$\Phi(x) = \sum_{i=1}^{m} (P_{si} - P_{ri})^2 = \sum_{i=1}^{m} [f_i(x)]^2 \tag{2.6}$$

with $f_i = P_{si} - P_{ri}$

P_{si} is the goal or specified values and P_{ri} is the changing value of the system depending on the values of the design variables. In equation (2.6) f_i are called the residuals, i.e. the values that describe the difference between the goal and the current value of the system. The next step is to change the design variables in such a way that the system converges to the optimisation goal. For the Gauss-Newton method the change in the design variables is calculated as follows

$$[\Delta x] = -\left([J]^T [J]\right)^{-1} [J][f] \tag{2.7}$$

where $$[f]=\begin{bmatrix} f_1 \\ f_2 \\ f_3 \\ \vdots \\ f_m \end{bmatrix}$$

and $$[J]=\begin{bmatrix} \frac{\partial f_1}{\partial x_1} & \frac{\partial f_1}{\partial x_2} & \cdots & \frac{\partial f_1}{\partial x_n} \\ \frac{\partial f_2}{\partial x_1} & \frac{\partial f_2}{\partial x_2} & \cdots & \frac{\partial f_2}{\partial x_n} \\ \vdots & \vdots & & \\ \frac{\partial f_m}{\partial x_1} & \frac{\partial f_m}{\partial x_2} & \cdots & \frac{\partial f_m}{\partial x_n} \end{bmatrix}$$

[*J*] is an $m \times n$ Jacobian matrix. It is the first derivative of each of the residuals with respect to each of the design variables. A damping factor is also included to ensure forced descent and to prevent numerical instability by keeping adjustments made to the design variables small enough when the system is near the optimising goal. The equation that controls the design variables is now

$$[x]_{r+1} = [x]_r + \alpha_r [\Delta x]_r \tag{2.8}$$

where r denotes the number of iterations.

This optimisation is implemented in MATLAB. A GUI (graphical user interface) is created (see Figure 2.3.8), allowing a more user-friendly optimisation process. One of two topologies, modelling the external parameters of a transistor, can be selected. The values of the parameters should then be entered, as well as R_{opt} (as calculated with equation(2.5)), the design frequencies, normalising impedance and the minimum allowed error. The code will then optimise the system and give Z_{opt} at the centre frequency (Figure 2.3.9). Various graphs are also displayed such as the real and imaginary part of Z_{opt} across the entire frequency range (Figure 2.3.10 and Figure 2.3.11 respectively), the number of iterations and the error between the optimising goal and the value of the system at each frequency. The impedance value provided by the optimiser is verified by simulating the extrinsic topology in Microwave Office and comparing the resulting resistance value seen by the internal current source to that specified in the optimiser.

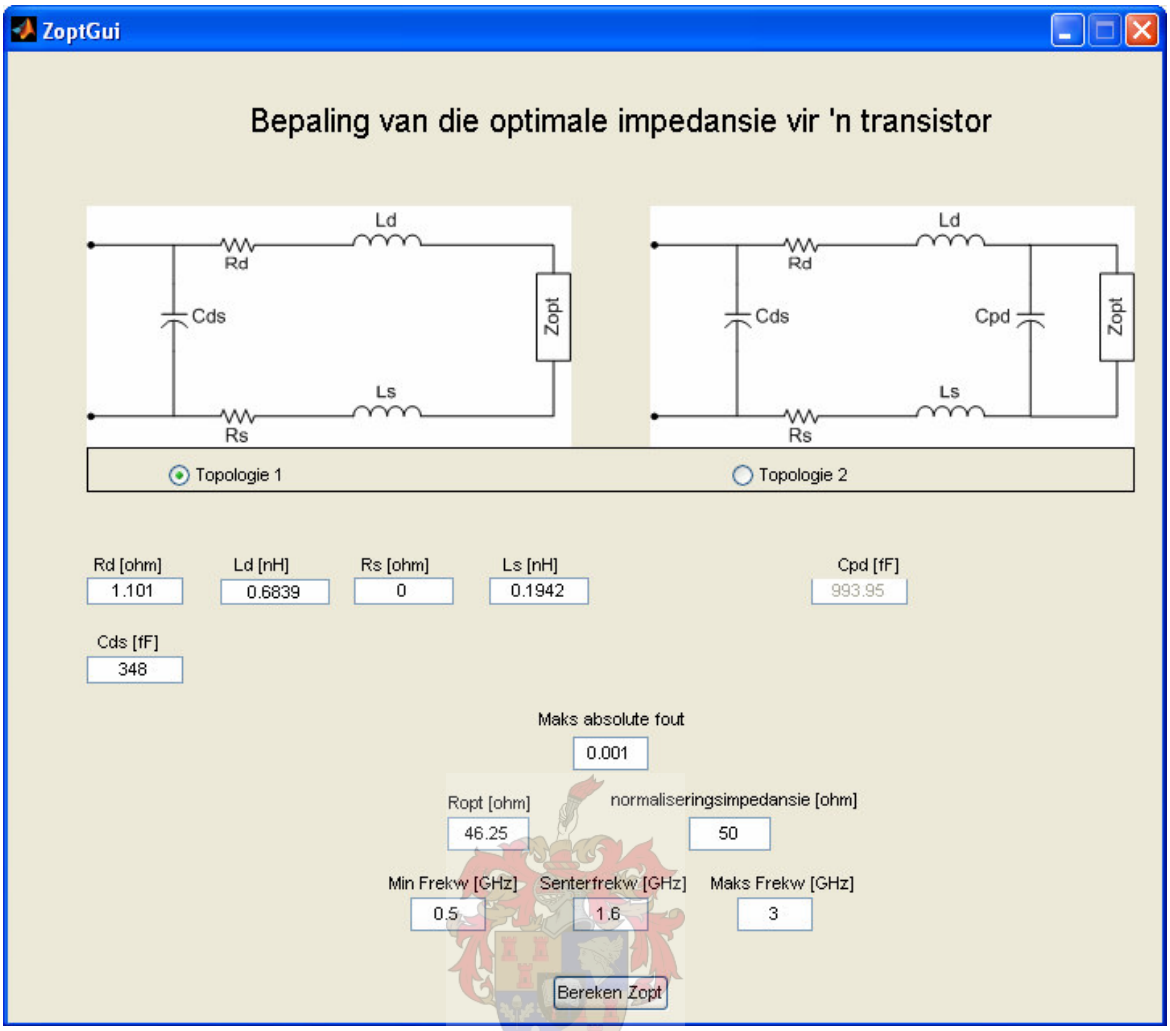


Figure 2.3.8 GUI created for optimising Z_{opt}.

Figure 2.3.9 Result from optimising code.

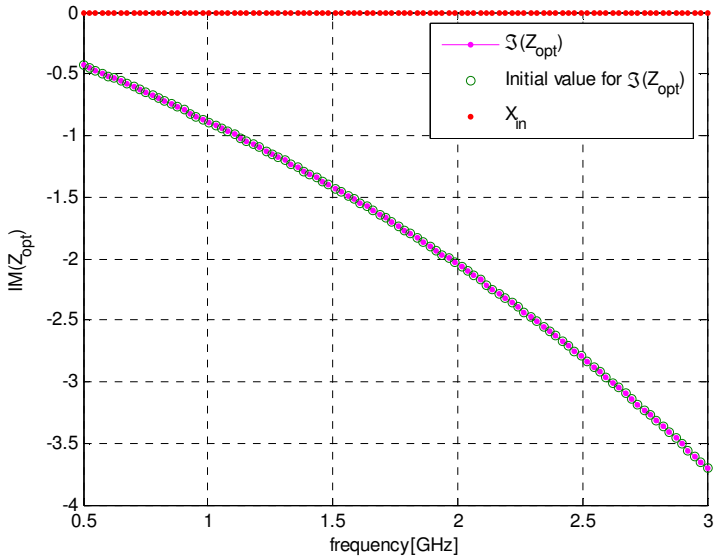


Figure 2.3.10 **Graph from the optimising code showing the initial (o) and final (•) value of the imaginary part of Z_{opt}, as well as the input reactance of the system (•).**

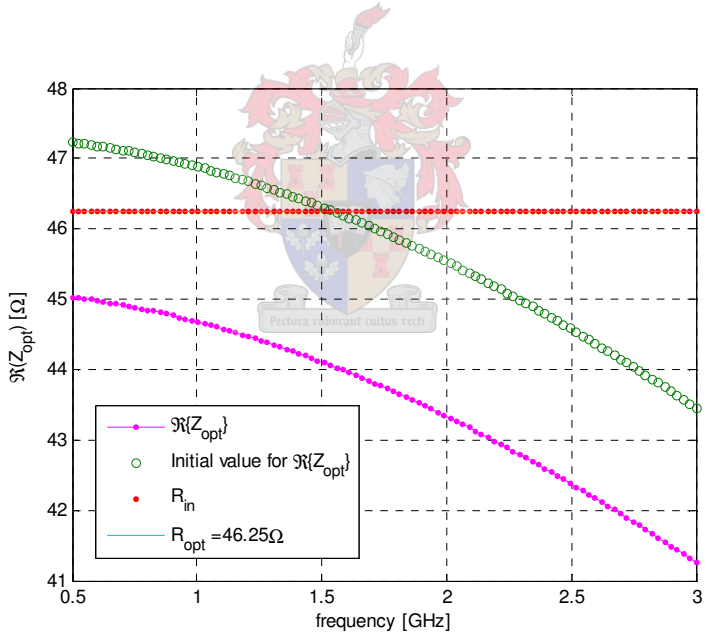


Figure 2.3.11 **Graph from the optimising code showing the initial (o) and final (•) value of the real part of Z_{opt}, as well as the input resistance of the system (•).**

2.4 Conclusions

An explanation is provided of the benefits of using a load-line match instead of a conjugate match during the design of a power amplifier.

Matlab code is implemented to calculate the resistance value of the load-line from measurements made of the current versus voltage curves of relevant transistors.

Finally, the optimiser code is tested by calculating the optimal impedance a particular transistor (a Siemens CFY30) should see to ensure the correct load-line is presented to the internal current source of the transistor. The resulting impedance value is verified numerically by running a Microwave Office simulation and comparing the resulting input resistance value seen by the internal current source.

Chapter 3

Doherty Amplifier Design Theory

3.1 Introduction

The theory surrounding Doherty amplifiers can be best introduced by supplying a description of the problem these amplifiers are designed to solve. This chapter therefore begins with a description of the efficiency problem in modern digital signals which the Doherty amplifier strives to overcome. The ideal theory behind the classical Doherty amplifier will be explained in detail, while a brief overview of some other Doherty configurations will be given. Lastly the shortcomings of the ideal theory will be discussed at the hand of practical considerations.

3.2 Ideal Theory

3.2.1 Efficiency Problem in Conventional Amplifiers

In this section Cripps' [1] explanation of the efficiency problem with reference to an idealised class B amplifier, shown in Figure 3.2.1, will be used. The device is biased to its cut-off point and the RF drive has the correct amplitude to swing the current to the device's maximum linear value of I_{max}. The output load consists of a resistance and resonator which will provide a short circuit for all harmonics.

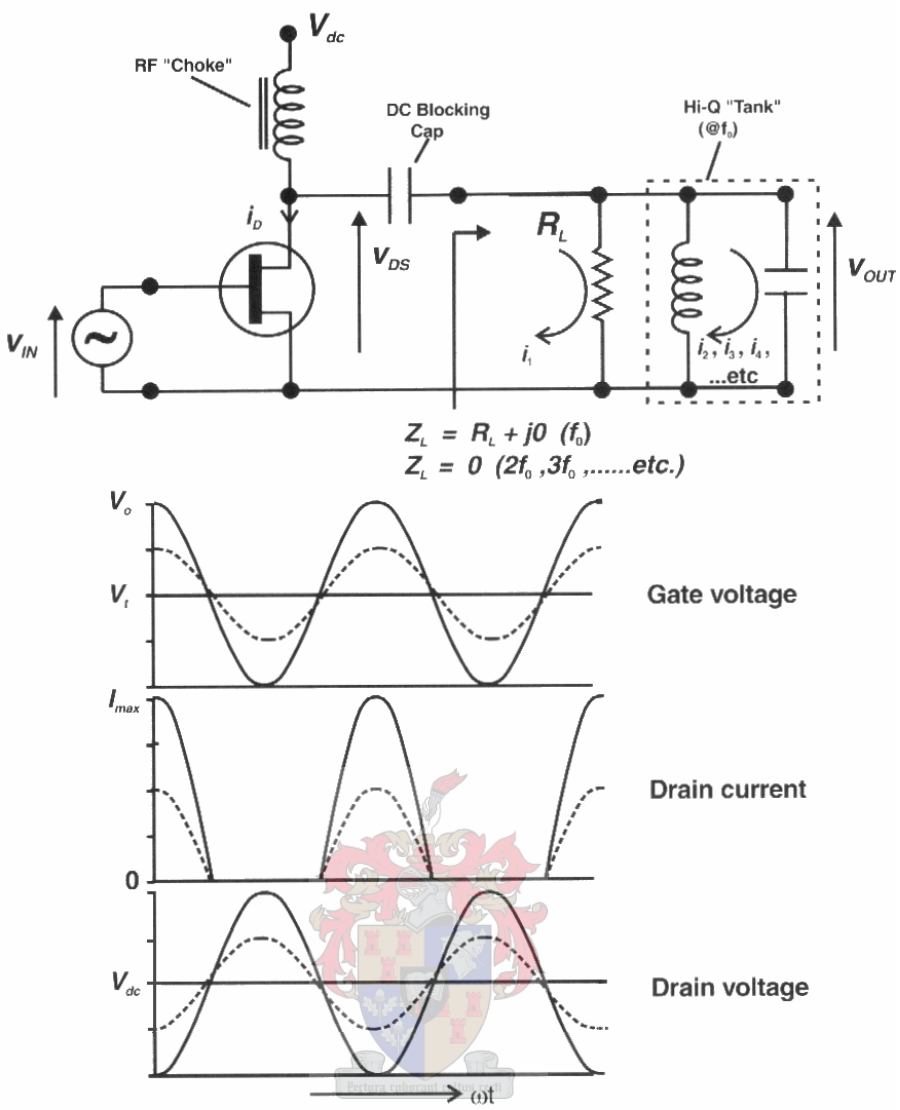


Figure 3.2.1 Class B amplifier and waveforms. Waveforms for $R_L = R_{opt}$ at maximum linear power (solid) and at 6 dB power back-off (dashed). (after [1])

The load resistance value is chosen according to the load-line technique described in Section 2.2 and because this is an idealised case with zero knee voltage the load resistance is

$$R_{opt} = 2\frac{V_{dc}}{I_{\max}}$$

Note that for a halfwave rectified sinewave with a peak value of I_{max}, its fundamental component is $I_{max}/2$ (compare with Figure 2.3.1). The RF output power is now

$$\begin{aligned} P_{RF} &= I_{rms}^2 R_{opt} \\ &= \left(\frac{1}{\sqrt{2}}\frac{I_{\max}}{2}\right)^2 \left(2\frac{V_{dc}}{I_{\max}}\right) \\ &= \frac{V_{dc} I_{\max}}{4} \end{aligned}$$

and the dc supply power is

$$P_{DC} = \frac{V_{dc} I_{\max}}{\pi}$$

The efficiency is calculated as

$$\eta = \frac{P_{RF}}{P_{DC}} = \pi/4$$

or about 78.5%.

Let us now consider what happens if the amplitude of the input RF voltage is reduced by a factor p from the ideal maximum level. Because the transconductance is assumed to be linear, the output RF current will still be a halfwave rectified sinewave with its amplitude reduced by the factor p. The fundamental component of the RF current is now

$$I_1 = \frac{I_{\max}}{2p}$$

With the original load resistance of R_{opt}, the output voltage amplitude will change to

$$V_1 = \frac{I_{\max}}{2p} R_{opt} = \frac{V_{dc}}{p}$$

thus, the RF output power is

$$P_{RF} = \frac{V_{dc} I_{\max}}{4p^2} \qquad (3.1)$$

the dc supply power is

$$P_{DC} = \frac{V_{dc} I_{\max}}{p\pi} \tag{3.2}$$

and the resulting efficiency is

$$\eta = \frac{\pi}{4p} \tag{3.3}$$

For example: a 3 dB reduction in drive power corresponds to $p = \sqrt{2}$ and a resulting 3 dB drop in RF output power (from (3.1)), but the efficiency reduces from 78.5% to 55.5%. At 6 dB back-off efficiency reduces to 39%. In Figure 3.2.1 the waveforms representing the 6 dB back-off condition is shown as dashed lines. Figure 3.2.2 shows the same maximum and reduced input drive levels, as well as their corresponding output waveforms for the calculated load resistance of R_{opt}.

The cause for the reduction in efficiency at reduced input drive levels can now be explained at the hand of these two figures. From Figure 3.2.2 it is clear that the calculated load resistance (represented by the load-line) is too small to allow maximum output voltage swing for the 6 dB back-off condition. The efficiency for the 6 dB backed-off condition can be returned to the optimum value of 78.5% if the load resistance could be increased to $2R_{opt}$ as Figure 3.2.3 shows. This means that the efficiency can be kept at its optimum by increasing the load resistance with the same factor p by which the input drive level is reduced. This can be proved mathematically by first increasing the load resistance with the factor p

$$R_L = \frac{V_{dc}}{I_{\max}} 2p \tag{3.4}$$

The RF output power with the above load resistance of R_L is

$$P_{RF} = \frac{V_{dc} I_{\max}}{4p} \tag{3.5}$$

and the DC power will be unaffected by the RF load resistance at

$$P_{DC} = \frac{V_{dc} I_{\max}}{p\pi} \tag{3.6}$$

By now calculating the efficiency using (3.5) and (3.6) it remains constant at $\pi/4$.

It should now become clear to the reader that maximum efficiency can be maintained if the load resistance can somehow be dynamically adjusted according to the relationship expressed in equation (3.4).

This is precisely what the Doherty amplifier accomplishes and the technique will be described in the next section.

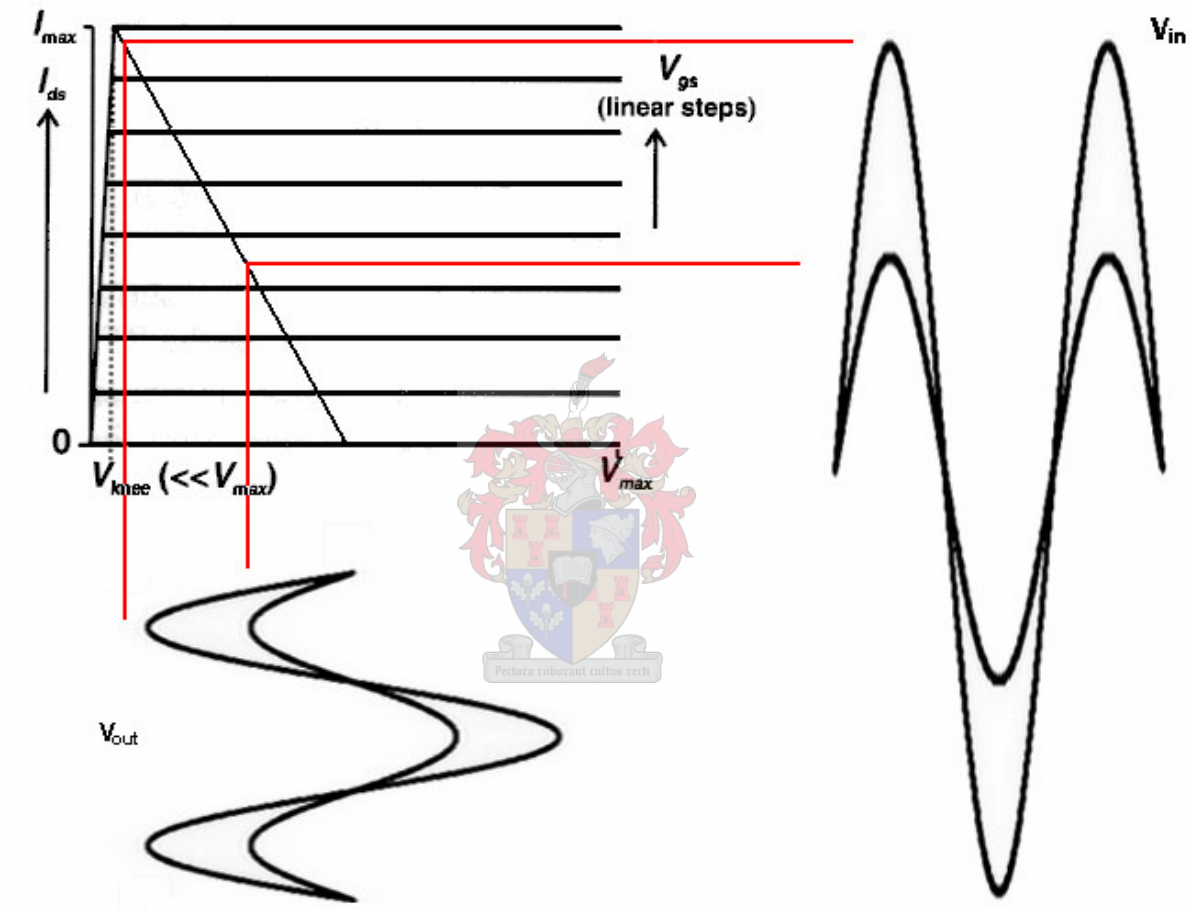


Figure 3.2.2 Reduction in efficiency is caused by the same amount of reduction in both the output current and voltage.

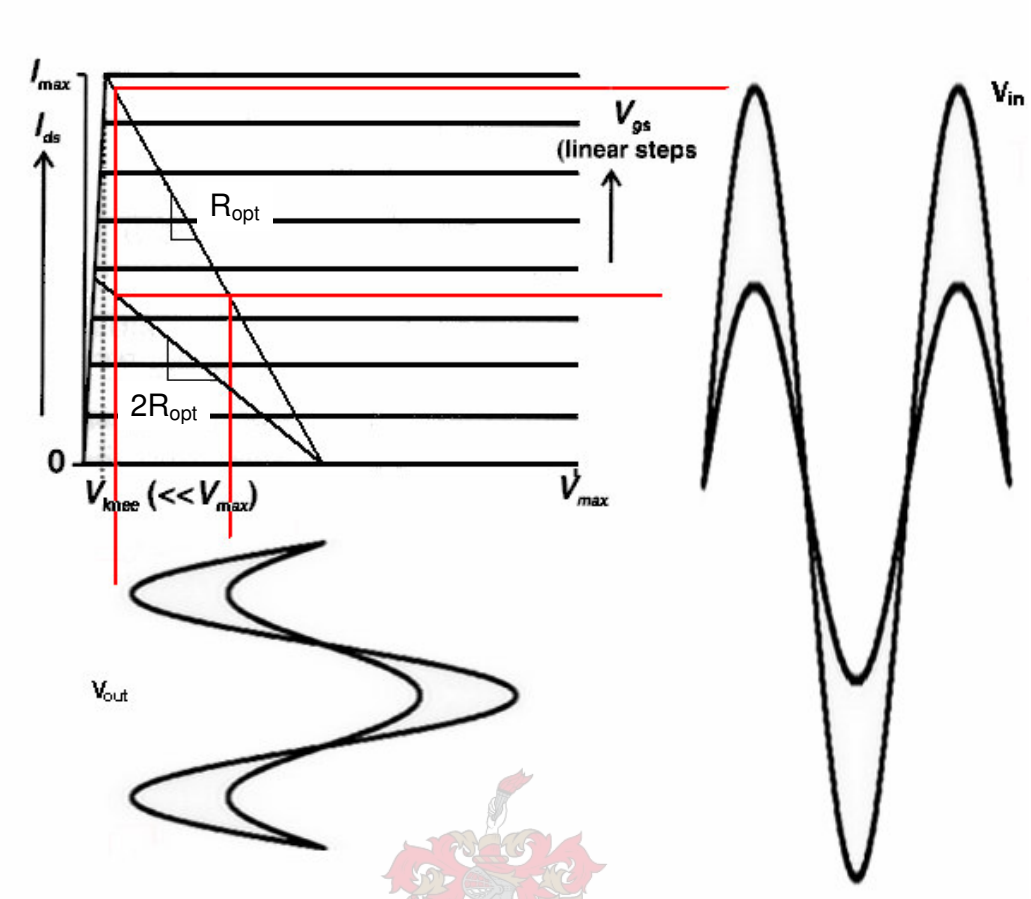


Figure 3.2.3 Example of how the output voltage swing can be increased to its maximum swing for reduced drive level by increasing the load resistance.

3.2.2 Classical Doherty Amplifier

The Doherty amplifier was first proposed in 1936 by Doherty [9] when vacuum tubes were still in use. Since then a number of authors have covered the subject and given an explanation of Doherty's theory applied to modern day transistors [1], [2], [10] - [12].

A Doherty amplifier makes use of an active load-pull technique – the concept of adjusting the impedance that a source sees by applying current from a second source [1].

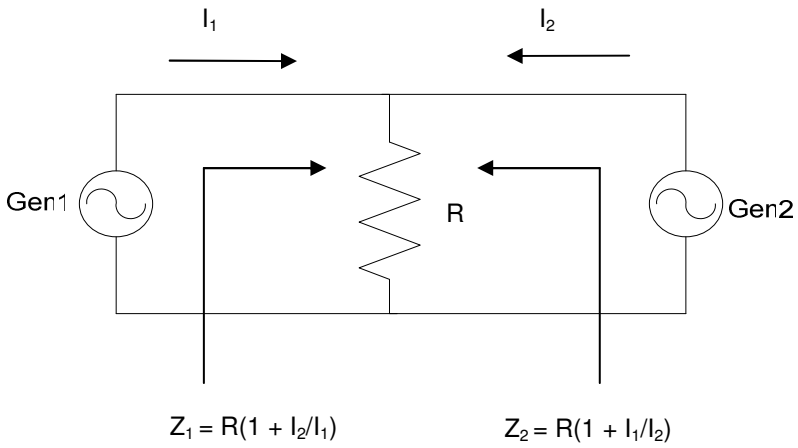


Figure 3.2.4 Active load-pull configuration

In Figure 3.2.4 generator 1 sees a load of R if generator 2 is delivering no current. If generator 2 supplies a current I_2, and generator 1 a current of I_1, Kirchoff's current law shows that the voltage appearing across the common load is

$$V_L = R_L(I_1 + I_2)$$

The load which is now seen by generator 1 can be calculated as

$$R_1 = R_L\left(\frac{I_1 + I_2}{I_1}\right) \tag{3.7}$$

At the same time generator 2 sees a load equivalent to generator 1

$$R_2 = R_L\left(\frac{I_1 + I_2}{I_2}\right) \tag{3.8}$$

(3.7) and (3.8) can be extended to complex notation to denote phase and magnitude

$$Z_1 = R_L\left(1 + \frac{I_2}{I_1}\right) \tag{3.9}$$

The above equation shows the possibility of controlling the impedance seen by generator 1 by controlling the magnitude and phase of the current I_2 supplied by generator 2. For example, Z_1 can be increased by increasing the magnitude of I_2 while being in phase with I_1.

If the two generators are now considered to be the outputs of two transistors with in-phase inputs, the load impedance seen by one of the transistors can be modified by the other [1].

Equation (3.9) is thus the key to active load modulation and solving the problem stated in Section 3.2.1. The theoretical solution in Section 3.2.1 however, was that the impedance seen by the amplifier had to increase with a decrease in input drive level, while with equation (3.9) the impedance decrease with a decrease in the current from the second generator. The active load-pull technique described by Figure 3.2.4 and equations (3.7) - (3.9) therefore accomplishes quite the opposite from what is needed to achieve maximum efficiency at backed-off conditions. To change the current load-pull technique to fit the needs described in Section 3.2.1, an impedance inverter is added. This can be in the form of a quarter-wave transformer or an equivalent T or Π network between generator 1 and the common load [1], [2], [9] - [12]. In this project only a quarter-wave transmission line was used as shown in Figure 3.2.5. Not only is Figure 3.2.5 an active load-pull configuration with an impedance inverter, but it is a representation for an ideal Doherty amplifier.

Because Figure 3.2.5 is a representation of an ideal Doherty amplifier, the symbols in Figure 3.2.5 have been changed from Figure 3.2.4 to correspond to the notation mostly used with Doherty amplifiers and which will be used further on in this thesis.

The configuration now consists of two generators, or in this case, transistor amplifiers simply represented as ideal current sources. These two amplifiers are called the “main” or “carrier” amplifier and the “peaking” or “auxiliary” amplifier. The subscripts in Figure 3.2.5 correspond to these terms, where I_p and Z_p denote the current from the peaking amplifier and the impedance seen by the peaking amplifier respectively. The current from the peaking amplifier is shown as jI_p because it has to be in phase with I'_c. In the same way I_c and Z_c represent the current and impedance at the output terminals of the carrier amplifier. I_c' and Z_c' is the current and impedance after the quarter-wave transformer.

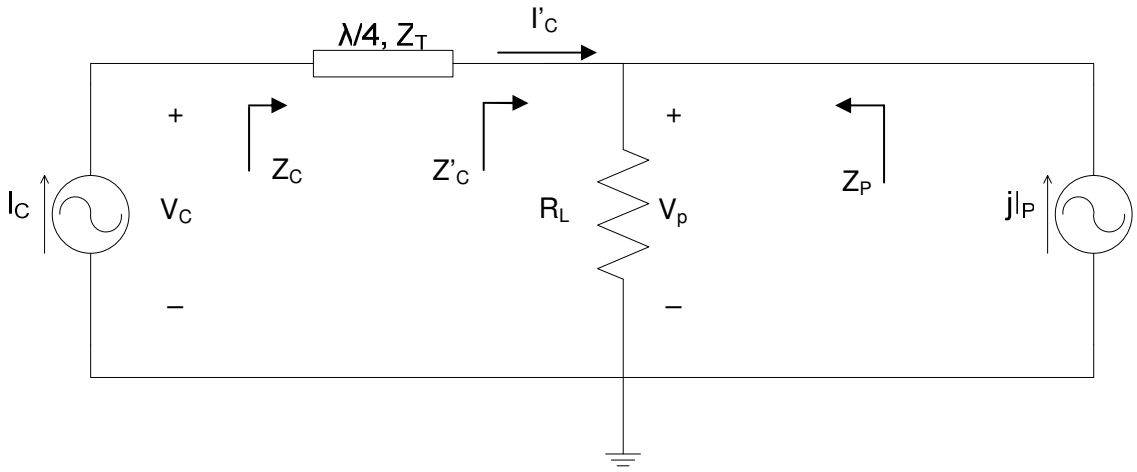


Figure 3.2.5 Active load-pull with quarter-wave transmission line acting as an impedance inverter. Sources are ideal current sources.

A brief description of the operation of an ideal system will now be provided. At low drive levels the peaking amplifier is cut off and the carrier amplifier operates as a linear class B or class AB amplifier into the common load of R_L. The quarter-wave transformer, which acts as an impedance inverter, transforms this load to present the carrier amplifier with the correct resistance which will ensure the carrier amplifier going into saturation at half of the peak envelope power or PEP. At this transition point the peaking amplifier should become active, either through biasing or external circuitry. When the peaking amplifier becomes active, the load-pulling effect causes the load, Z_c, seen by the carrier amplifier to decrease dynamically with increasing drive level. This decrease in the load impedance presented to the carrier amplifier keeps the carrier amplifier in saturation from the transition point all the way to PEP, thus maintaining maximum voltage swing and efficiency. For the classic Doherty amplifier the transition point is at half the maximum input voltage amplitude, which means that maximum efficiency is maintained from PEP to 6 dB below PEP.

The above explanation is just a general one in which the load resistance and characteristic impedance of the quarter-wave line plays a critical role. Therefore these values have to be derived to ensure correct theoretical load modulation.

Although all the current mathematical derivations - done only slightly different - arrive at the same solution [1], [2], [9], [10], [12], this discussion will mainly use the one given by Cripps [2].

The quarter-wave transmission line has the following terminal characteristics

$$\begin{bmatrix} V_2 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 & jZ_o \\ 1/jZ_o & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ I_1 \end{bmatrix} \tag{3.10}$$

and according to Figure 3.2.5 becomes

$$\begin{bmatrix} V_p \\ I'_c \end{bmatrix} = \begin{bmatrix} 0 & jZ_T \\ 1/jZ_T & 0 \end{bmatrix} \begin{bmatrix} V_c \\ I_c \end{bmatrix}$$

For this analysis it is assumed that the two amplifiers are conducting different fundamental current amplitudes, I_c and I_p, at any given input signal amplitude v_{in}, where

$$I_c = f_c(v_{in}) \text{ and } I_p = f_p(v_{in})$$

These are not necessarily linear functions of the input drive signal, v_{in}, and is a generalisation of the case considered in [1] where these functions were assumed to be linear. Ideal harmonic shorts are assumed to be placed across each amplifier, so that only fundamental voltage and current components are considered in this analysis.

By using the characteristics of the impedance inverter expressed by equation (3.10) and applying it to Figure 3.2.5 the following expressions can be derived

$$V_p = jZ_T I_c \tag{3.11}$$

$$I'_c = \left(\frac{1}{jZ_T}\right) V_c \tag{3.12}$$

as well as the remaining relation

$$I'_c = jI_p - \frac{V_p}{R} \tag{3.13}$$

Expressions for the voltages at the amplifier outputs, V_m and V_p, are required in terms of the currents I_m and I_p. Equation (3.11) already gives such a relationship and shows that the output voltage of the peaking amplifier is the same as the total output load voltage and is proportional to the carrier amplifier current, I_c, and independent to the peaking amplifier current, I_p. If the correct action of the peaking amplifier keeps the carrier amplifier's voltage below clipping levels, then the linearity of the whole system is defined only by the characteristic of the carrier amplifier $f_m(v_{in})$. The requirement for the peaking amplifier can be determined from equations (3.11) - (3.13) as

$$V_c = Z_T \left[\left(\frac{Z_T}{R_L} \right) I_c - I_p \right] \tag{3.14}$$

which highlights the possibility of keeping the carrier amplifier's output voltage below clipping levels with a suitable peaking amplifier characteristic described by $I_p = f_p(v_{in})$.

With this limiting process achieved by the characteristic of the peaking amplifier, it is remarkable that according to (3.11), the output voltage is only dependant on the current from the carrier amplifier I_c. This property verges on a linearization process [2]. Although this a remarkable property associated with the Doherty amplifier, this project focussed mainly on investigating the efficiency enhancement of Doherty amplifiers.

For further investigation into the Classical Doherty amplifier and to be able to make a clear distinction between the Classical and any other Doherty configurations a few symbols have to be clearly defined and will be done in accordance to Cripps [2].

- I_c and I_p are the amplitudes of the fundamental currents of the carrier and peaking amplifiers.
- I_C and I_P refer to the maximum values of the of the fundamental current components of the carrier and peaking amplifiers, thus

$$I_C = (I_c)_{\max}$$
$$I_P = (I_p)_{\max}$$

with their ratio being

$$\Gamma = \frac{I_P}{I_C} \tag{3.15}$$

and the input drive signal being normalised as

$$0 < v_{in} < 1$$

The "breakpoint" where the peaking amplifier starts conducting is defined as

$$v_{in} = v_{bk}$$

where

$$0 < v_{bk} < 1$$

The Classical Doherty amplifier can now be described and the values for R_L and Z_T can be derived. For the Classical Doherty configuration

$$\begin{aligned} &I_C = I_M, \quad (\Gamma = 1) \\ &I_p = f_p(v_{in}) = 2v_{in}I_P - I_P \quad 0.5 < v_{in} < 1, \\ &\qquad\qquad = 0 \qquad\qquad 0 < v_{in} < 0.5 \\ &I_c = f_c(v_{in}) = v_{in}I_M \qquad 0 < v_{in} < 1, \\ &v_{bk} = 0.5 \end{aligned}$$

From the mathematical description above and descriptions earlier in this section it is known that the peaking amplifier is inactive up to the breakpoint and that the carrier amplifier should reach its maximum allowable voltage at this point. This maximum corresponds to the DC supply voltage (refer to the drain voltage waveform in Figure 3.2.1). Because the peaking amplifier is inactive up to the breakpoint, I_p is zero and (3.14) can be written as follows for the breakpoint $v_{in} = v_{bk}$

$$V_c = V_{dc} = (0.5) I_M \left(\frac{Z_T^2}{R_L} \right) \tag{3.16}$$

As explained, the carrier amplifier's voltage amplitude V_C should be kept constant from the breakpoint, $v_{in} = v_{bk} = 0.5$, up to the maximum drive signal $v_{in} = 1$. A second relationship can now be derived for the maximum drive condition where $I_c = I_C$ and $I_p = I_P$ and (3.14) becomes

$$V_c = V_{dc} = Z_T \left[\left(\frac{Z_T}{R_L} \right) I_C - I_P \right] \tag{3.17}$$

Remembering that $I_C = I_P$, (3.16) and (3.17) can now be solved to give the values of R_L and Z_T as

$$R_L = \frac{V_{dc}}{2I_C} \text{ and } Z_T = \frac{V_{dc}}{I_C} \quad (= 2R_L) \tag{3.18}$$

If it assumed the amplifiers in the above analysis is ideal with zero knee voltage and (3.18) is compared with (2.5), the following important relationships comes to light

$$Z_T = R_{opt} \text{ and } R_L = {R_{opt}}/{2} \tag{3.19}$$

where R_{opt} is the optimal resistance for load-line matching, as derived in Section 2.2.

A general explanation of the Doherty amplifier has been given and the values for R_L and Z_T have been derived. To conclude the theory of a Classical Doherty amplifier, the operation will be explained according the three principal regions of operation using the values derived in (3.19).

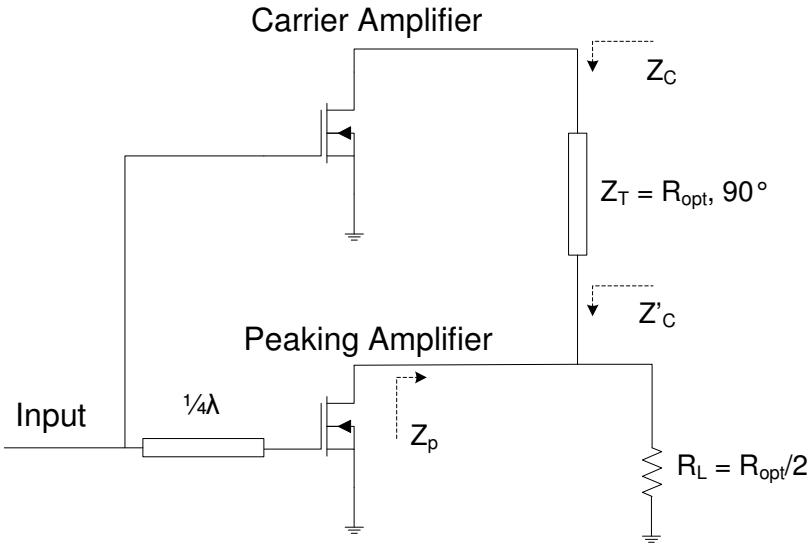


Figure 3.2.6 Classical Doherty Amplifier configuration.

Figure 3.2.6 shows the basic configuration of a Classical Doherty amplifier. The two amplifiers are termed the carrier and peaking amplifiers. The quarter-wave transmission line with characteristic impedance of $Z_T = R_{opt}$ is connected to the output of the carrier amplifier and acts as an impedance inverter. To ensure that the currents of the carrier and peaking amplifier are in phase at the common load, $R_L = 0.5R_{opt}$, an extra 90° phase delay is placed at the input of the peaking amplifier.

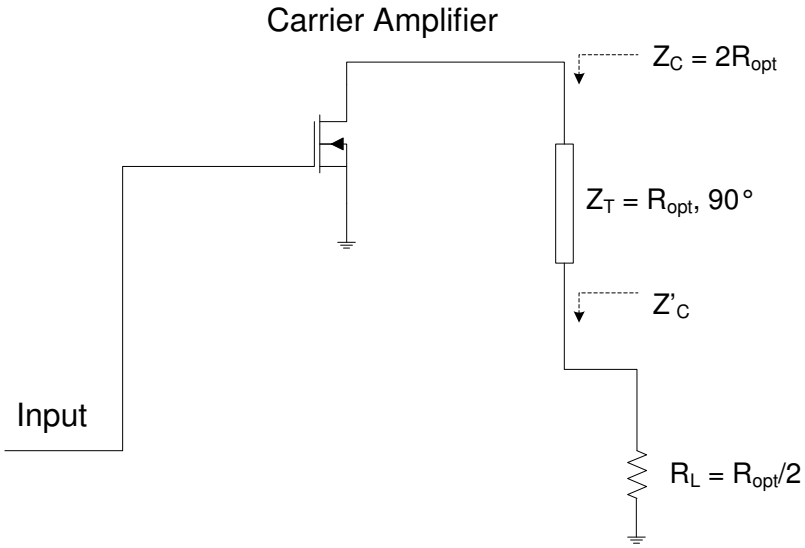


Figure 3.2.7 Doherty configuration for low input power (6 dB back-off and lower).

The first region of operation is where the input drive signal is not sufficient to turn on the peaking amplifier. For the ideal case it is assumed that the output impedance of the peaking amplifier during this operation is infinite and the basic configuration in Figure 3.2.6 can be redrawn as in Figure 3.2.7.

The output power from the carrier amplifier is now delivered entirely to the load, $R_L = 0.5R_{opt}$. However, the load, $R_L = 0.5R_{opt}$, is transformed across the quarter-wave transmission line to present the output of the carrier amplifier with an impedance of $Z_c = 2R_{opt}$. At this point $I_c = 0.5I_C$, while the voltage level is saturated and the efficiency will be at its maximum as was proven in Section 3.2.1 (see equations (3.4) - (3.6)).

For the sake of clarity it is more convenient to discuss the third region of operation before the second region is covered. This third region is where the input drive level is at its allowed maximum. The peaking amplifier is now also saturated and the power delivered to the load is evenly distributed between the carrier and peaking amplifiers. For this region of operation Figure 3.2.6 can be redrawn as Figure 3.2.8. The load-pulling relationship of (3.9) can be applied to calculate the different impedances seen by the two amplifiers as

$$\begin{aligned} Z_c^{'} &= \frac{R_{opt}}{2}\left(1+\frac{I_p}{I_c^{'}}\right) \\ &= \frac{R_{opt}}{2}\left(1+\frac{I_P}{I_C}\right) \\ &= R_{opt} \end{aligned}$$

and

$$\begin{aligned} Z_p &= \frac{R_{opt}}{2}\left(1+\frac{I_c^{'}}{I_p}\right) \\ &= \frac{R_{opt}}{2}\left(1+\frac{I_C}{I_P}\right) \\ &= R_{opt} \end{aligned}$$

Because the quarter-wave transmission line also has a characteristic impedance of $Z_T = R_{opt}$ the impedance seen by the output of the carrier amplifier is $Z_c = R_{opt}$.

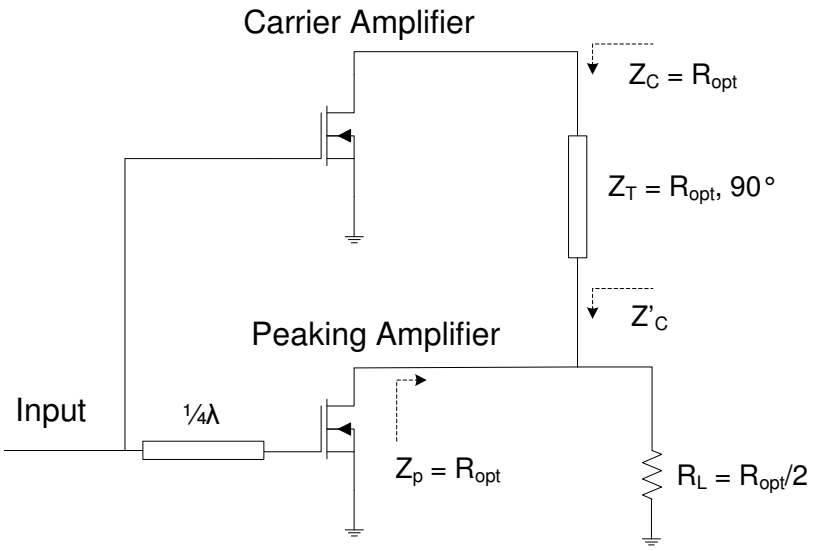


Figure 3.2.8 Doherty configuration for maximum input drive level or PEP.

The second region of operation lies between the first and the third region. It starts when the peaking amplifier begins to conduct and the carrier amplifier's output voltage goes into saturation. As the input drive is increased, the peaking amplifier's fundamental current component, I_p, increases and it delivers output power to the load. As I_p increases the load-pulling effect will become active by increasing the impedance Z'_c, and the output of the carrier amplifier will experience dynamic reduction in the impedance, Z_c, it sees. This enables the carrier amplifier to deliver more power to the load whilst maintaining a saturated voltage swing and maximum efficiency.

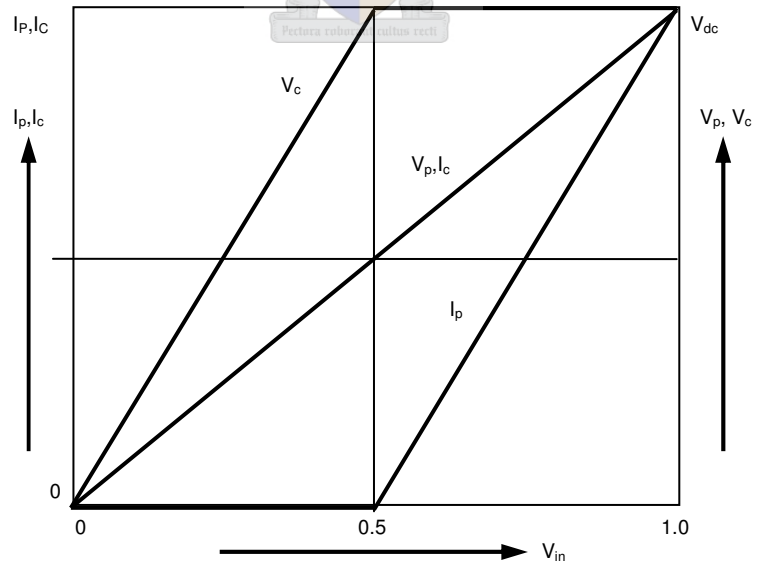


Figure 3.2.9 Characteristics of fundamental current and voltage amplitudes for the carrier and peaking amplifier plotted against the input drive amplitude.

Figure 3.2.9 gives a graphical summary of the discussion in this section, showing the characteristics of the currents and voltages (fundamental components) of both amplifiers against the input drive signal. Note the key points of operation: The carrier amplifier's voltage, V_c, saturates when the input drive signal, v_{in}, is half of its maximum amplitude. At this point in time the peaking amplifier starts conducting. Its current, I_p, increases with the input drive signal until both reach their maximum level at the same time. At this point the currents of both amplifiers are equal.

Figure 3.2.10 shows the theoretical efficiency against output power back-off for the Classical Doherty amplifier and a normal class B amplifier. Note that the Doherty amplifier's efficiency is at its maximum at 6 dB back-off and peak output power. Between these two points the efficiency is slightly less. This is because the peaking amplifier only reaches its maximum efficiency at the peak output power and therefore decreases the overall efficiency between the 6 dB back-off point and peak output power [10].

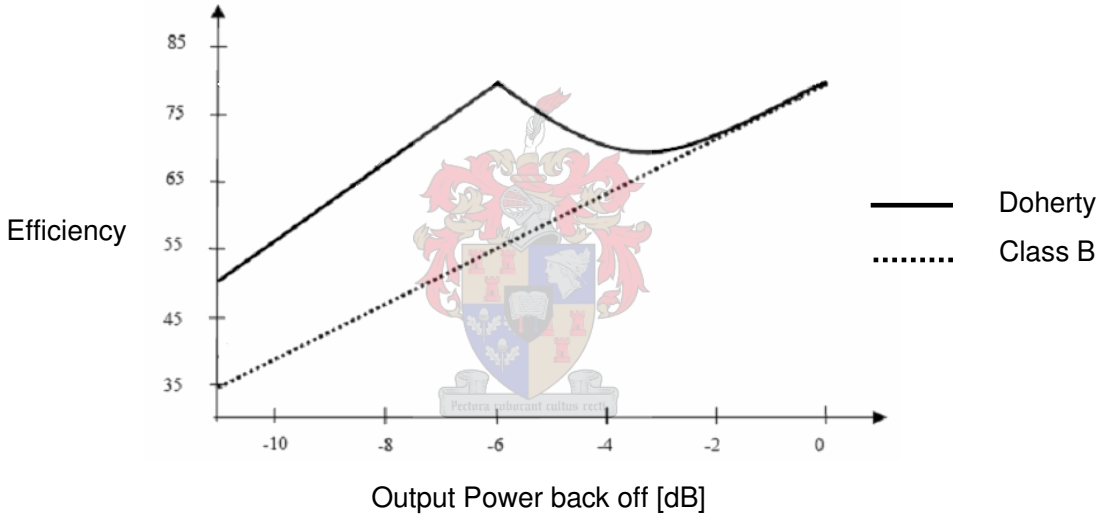


Figure 3.2.10 Theoretical efficiency of a Classical Doherty amplifier compared to a class B amplifier.

3.2.3 Doherty Lite, Asymmetrical Doherty and N-Way Doherty Amplifier

In the previous section the ideal theory of a Classical Doherty amplifier was explained, but no details were given about how to achieve the theoretical results in practice. Before the practical aspects are covered in the next section, one of the inherent problems in a Classical Doherty configuration will be highlighted to justify the need for other existing configurations.

The easiest and most popular way to achieve a peaking amplifier which remains turned off below the breakpoint is to bias the transistor to operate in class C mode, while the carrier amplifier operates in class AB or B mode. A problem arises when identical transistors (Classical Doherty amplifier) for the carrier and peaking amplifiers are used with the same input level. When the maximum input drive level is reached, the fundamental components, I_C and I_P, will not be equal as assumed in the previous section and I_P would be about $0.4I_C$ [2]. This has the consequence that the carrier amplifier doesn't experience full load modulation.

To overcome this problem a number of other configurations exist. The simplest way to alleviate this problem is to increase the impedance seen by the carrier amplifier by slightly lowering the characteristic impedance of the quarter-wave impedance inverter [2]. This configuration is termed the Doherty Lite. The fundamental purpose of the Doherty Lite is to improve the efficiency at backed-off levels with as simple a circuit configuration as possible. Another property is that the efficiency plot will not have the classical twin peaks as in Figure 3.2.10 for the ideal Classical Doherty amplifier. Unfortunately there is not much else available in the existing literature about Doherty Lite configurations or derivations on how much the characteristic impedance should be lowered.

One of the more popular configurations is the Asymmetrical Doherty amplifier. Confusion may arise as authors use this term differently. Kim [13] use this term when uneven power drive to the peaking and carrier amplifiers are implemented as a solution to the problem of uneven maximum fundamental current components, I_P and I_C. Cripps [1], [2] uses this term in the case where the maximum fundamental current components, I_P and I_C, from the peaking and carrier amplifiers are unequal. In this thesis the definition of Kim for an Asymmetrical Doherty amplifier will be used.

The solution Kim [13] and Iwamoto [15] propose to the unequal current levels is an unequal power drive to the peaking and carrier amplifiers which prevents the amplifiers from saturating to early. They have done this by including a variable attenuator before the carrier amplifier and optimizing the attenuation as well as the gate biasing of the peaking amplifier. With this uneven power drive, Kim [13] has shown through simulation, the load modulation of the symmetric Classical Doherty can be greatly improved. Their measurements have also shown a 13% improvement of drain efficiency from a symmetric Doherty amplifier. One of the disadvantages is a decrease in the gain of the total system.

Another way to increase the peaking amplifier's fundamental current component is to use a different transistor for the peaking amplifier with a larger periphery than the carrier amplifier [2], [15]. RFIC designers have the advantage of manufacturing a transistor with a larger periphery for the peaking device. However, keeping the device switched off over the desired low level input range is still a problem [2]. The periphery of the peaking amplifier can also be expanded by using more than one peaking amplifier in parallel. This is called an N-Way Doherty amplifier. An N-way Doherty amplifier

is a carrier amplifier in parallel with N – 1 peaking amplifiers to acquire a peaking amplifier which is N – 1 times larger than the carrier amplifier. The main advantages of the N-way Doherty amplifier is improved linearity and the fact that the region of higher efficiency can be extended down to -12 dB back-off [14], as shown in Figure 3.2.11. The drawback of the N-way Doherty can also be seen in Figure 3.2.11. The region of lower efficiency between the two maximum points becomes greater and the efficiency decreases considerably as more peaking amplifiers are used. However, efficiency is still better than when compared to that of a normal class B amplifier.

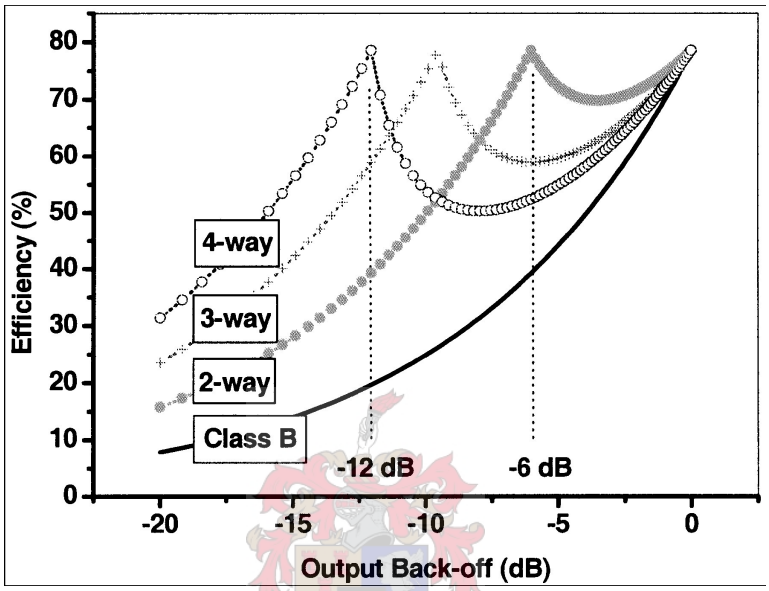


Figure 3.2.11 Ideal efficiencies of the N-way Doherty amplifiers. (after [14])

3.3 Practical Considerations

Although the differences between the ideal theory and a practical Doherty amplifier have not yet been discussed, the major stumbling block of a practical Classic Doherty amplifier was highlighted in the previous section. This fact that if two identical transistors with equal input drive power are used, the fundamental current component, I_p, from the peaking amplifier will not increase to the same level as the carrier amplifier's current, I_c. This prevents the full load modulation that it was designed for and causes the premature saturation of both amplifiers. The main reason for this is the peaking amplifier being in a fixed lower bias (class C) [2],[13],[16].

Although this problem was known earlier on in the project, none of the configurations discussed in Section 3.2.3 were implemented. It was argued that it would be best to start with the Classical Doherty amplifier in order to gain better understanding of the theory and practical aspects.

One of the most important points to remember when going from the ideal theory to designing a Doherty amplifier is that the transistors are not ideal. This means the transistors cannot be seen as ideal current sources, extrinsic parameters at the transistors' outputs come into play and these contribute to a finite output impedance. Consequently, the simple and elegant theory of an Ideal Doherty amplifier becomes more intricate.

A crucial point in the correct functioning of a Classical Doherty amplifier is that the impedance seen by the carrier amplifier varies from $2R_{opt}$ (at 6 dB back-off from PEP) to R_{opt} (at PEP). This works well in the ideal theory explained in Section 3.2.2 where the transistors were seen as ideal current sources. As explained in Section 2.3.2 this is not the case in practice. For the internal current source of the transistor to see a certain resistance, R_{opt}, an impedance, Z_{opt}, has to be determined through optimisation or load-pull measurements. Z_{opt} should be seen by the output of the transistor. To clarify this point, look at Figure 3.3.1. This schematic represents a practical Doherty amplifier, at maximum power output, which is based on the ideal theory and the few practical points covered so far. The dashed rectangles represent the transistors – including their packaging – of the carrier and peaking amplifiers. To ensure an impedance of Z_{opt} outside the transistors' packaging, a matching circuit is added which should transform R_o to Z_{opt}. In the ideal theory, i.e. without the matching circuits and extrinsic parameters, R_o would be equal to R_{opt} as in Figure 3.2.8. However, in this case R_o can basically be any resistance, as long as the matching circuit transforms it to Z_{opt}. A few considerations might influence the choice of R_o. These include the complexity of the matching circuit it will incur or basic practical aspects such as the widths of the transmission lines.

For this more practical approach there are still a few idealizations. To see these lingering idealisations one must look at both extremes of the Doherty operation: The low power operation, where the peaking amplifier is not conducting and the high power operation where both amplifiers are saturated and at maximum efficiency. The schematic for the high power region is shown in Figure 3.3.1 and for the low power region in Figure 3.3.2. These two schematics show a more practical approach, but still imply correct Doherty operation through the impedances shown. In other words, the impedances shown are the impedances necessary for full load modulation and thus correct Doherty operation.

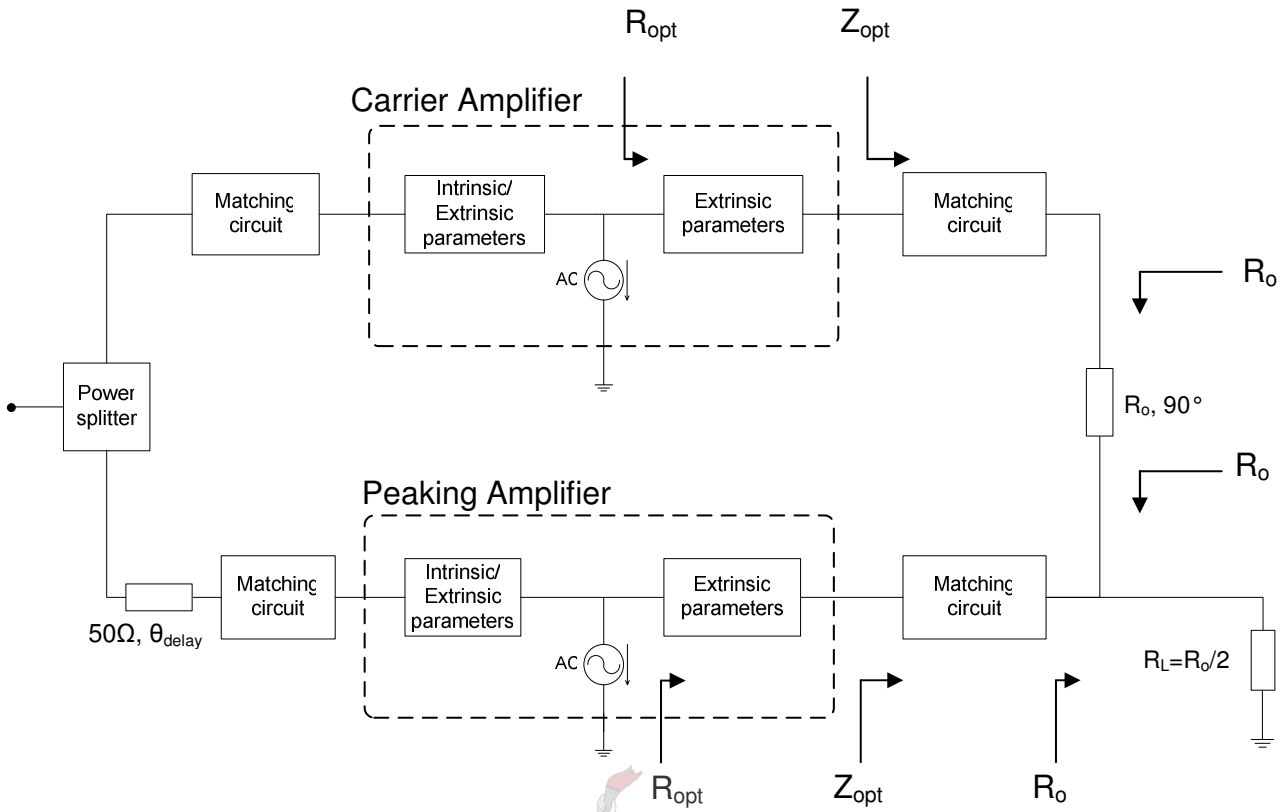


Figure 3.3.1 A more practical schematic for Classical Doherty amplifier at maximum output power showing the impedances that should be seen at various points in the circuit.

But these impedances will not be realised if a Doherty amplifier is built according to these schematics. To prove this point, the extrinsic parameters of a Siemens CFY30 GaAs FET will be used. The extrinsic parameters for this GaAs FET are shown in Figure 3.3.3. These parameters are only those used in calculating Z_{opt} and do not represent the entire small-signal model for the particular transistor. R_{opt} is calculated as 90.9 Ω and thus $2R_{opt}$ = 181.8 Ω. This in turn gives Z_{opt} = 84.16 + j13.1 Ω and Z'_{opt} = 142.66 +j65.13 Ω. If an arbitrary value of 50 Ω is chosen for R_o, a matching network (as shown in Figure 3.3.4) can be designed which will transform R_o to Z_{opt} when the Doherty amplifier is in its high power operation. This assumes implicitly that the fundamental current components of both amplifiers is adequate to transform the impedance seen into the quarter-wave impedance inverter from $2R_o$ (low power operation) to R_o (high power operation). The shortcoming of the peaking amplifier's fundamental current component at PEP, as discussed in Section 3.2.3, is thus not brought into account in this discussion.

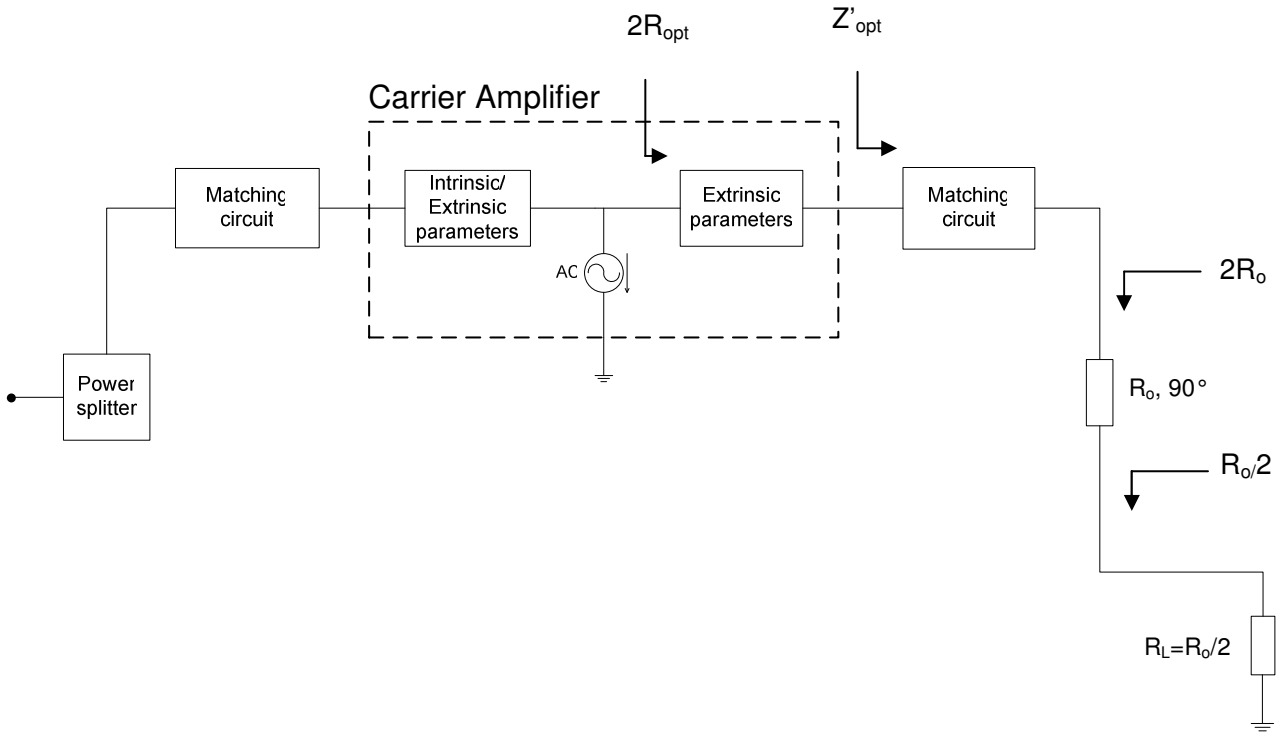


Figure 3.3.2 **A more practical schematic for Classical Doherty amplifier at low power showing the impedances that should be seen at various points in the circuit.**

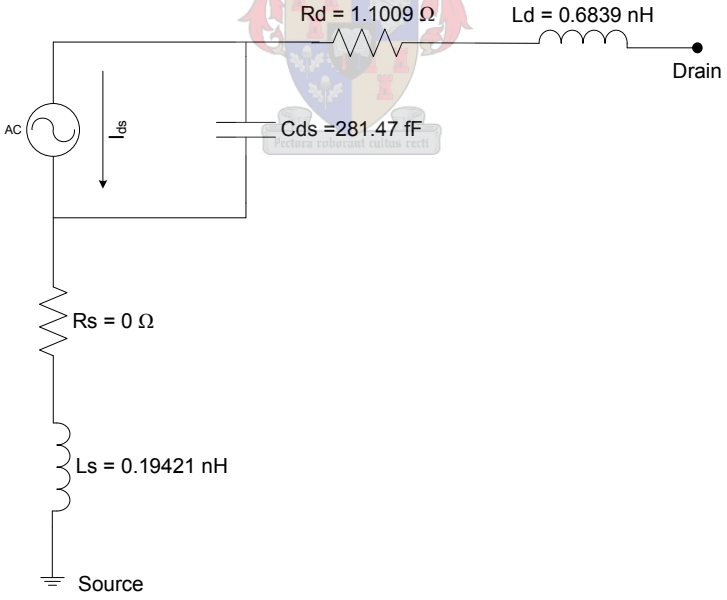


Figure 3.3.3 **Extrinsic parameters for a Siemens CFY30 GaAs FET transistor.**

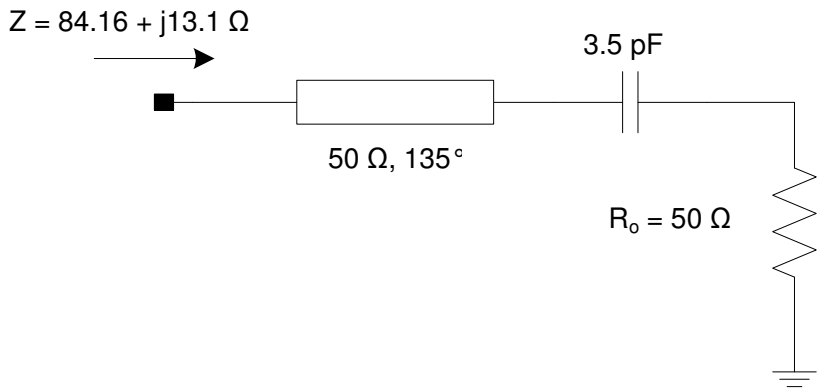


Figure 3.3.4 Matching network to match 50Ω to 84.16+*j*13.1Ω.

By simulating these extrinsic parameters with the matching section and a load of R_o = 50 Ω, an input impedance of 90.9 Ω can be achieved by small adjustments of the matching section's parameters. This circuit is shown in Figure 3.3.5. To represent the low power operation the same circuit is simulated with a load of $2R_o$ = 100 Ω and the simulated circuit is shown in Figure 3.3.6. The input impedances as simulated in Microwave Office for these two circuits are shown in Figure 3.3.7. This shows an input impedance of 90.7 – *j*1.3 Ω for the high power operation which is very close to the designed R_{opt} = 90.9 Ω. The input impedance for the low power operation is 63.3 + *j*43.7 Ω which is far from the required $2R_{opt}$ = 181.8 Ω.

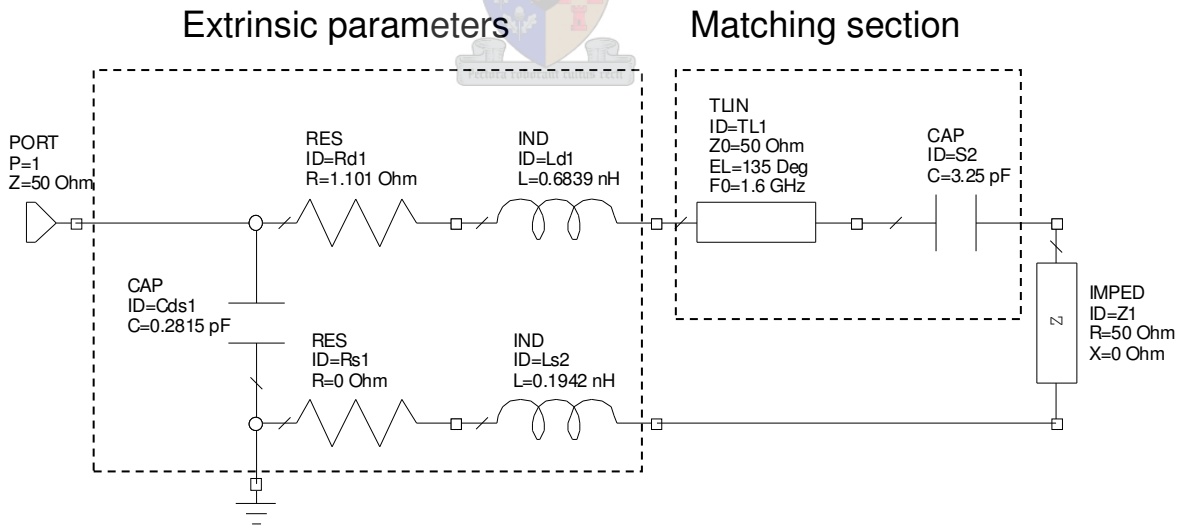


Figure 3.3.5 Extrinsic parameters with matching section and load R_o.

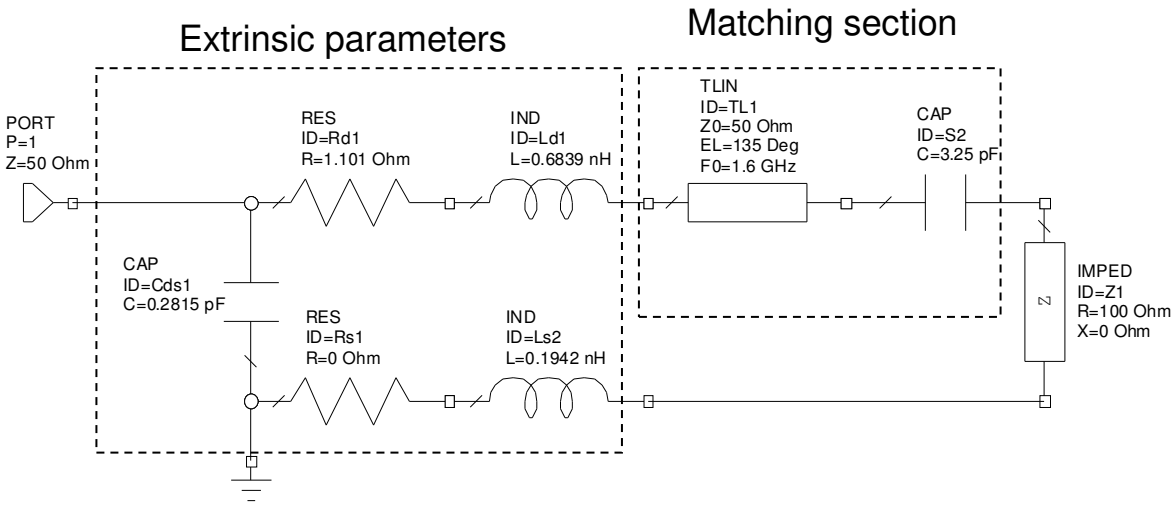


Figure 3.3.6 Extrinsic parameters with matching section and load $2R_o$.

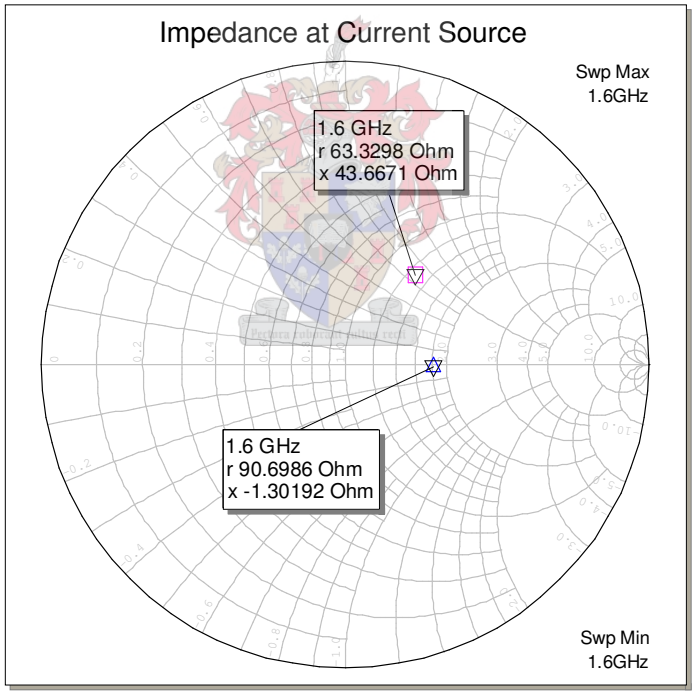


Figure 3.3.7 Impedance seen by internal current source of Siemens CFY30 GaAs FET when the designed matching circuit and load of R_o = 50Ω (Δ) and $2R_o$ = 100Ω (□) are added.

This problem was also encountered by Kim [17] and Yang [18], and led to the solution of adding an extra offset line with the same characteristic impedance as the quarter-wave impedance inverter. By using the same characteristic impedance as the impedance inverter, the matching for the low power operation can be adjusted, while the matching for the high power operation remains unaffected.

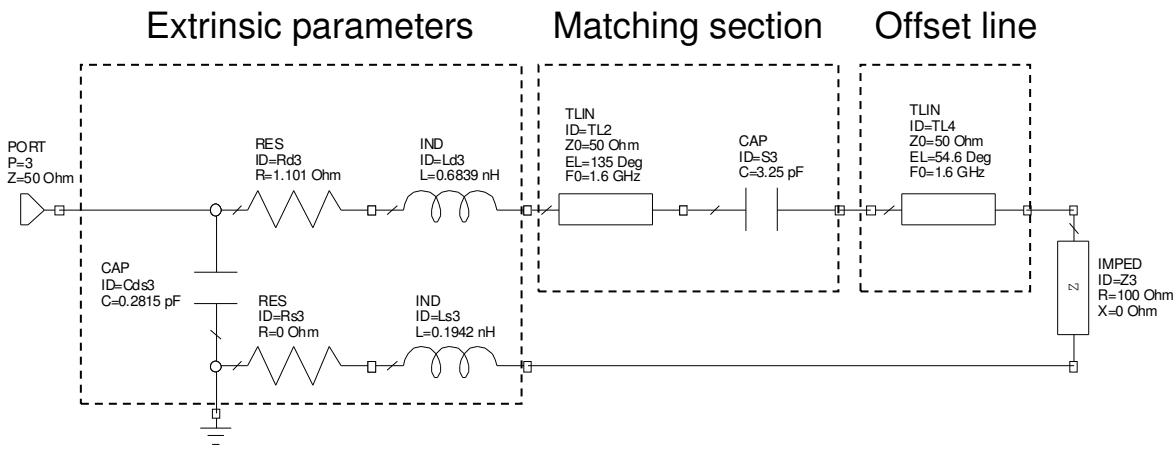


Figure 3.3.8 Extrinsic parameters with matching section, offset line and load $2R_o$.

Figure 3.3.8 shows the extrinsic parameters, matching section and extra offset line of 54.6° with characteristic impedance equal to R_o = 50 Ω. The load of 100 Ω represents the low power operation as the impedance seen at the input of the quarter-wave impedance inverter should be $2R_o$ = 100 Ω for the low power operation. The impedance that is now seen by the internal current source (shown in Figure 3.3.9) is transformed from 63.3 + *j*43.7Ω to 187.1 + *j*0.1Ω which is much closer to the desired 181.8 Ω.

It is possible that the choice of R_o may also influence the load modulation seen by the internal current source. This is because the value of R_o influences the matching section which converts R_o to Z_{opt}, which in turn influences the length of the offset line. Most of the projects in current literature make use of "partially pre-matched" transistors and therefore choose R_o = 50 Ω, but this does not necessarily mean that it is the optimal choice.

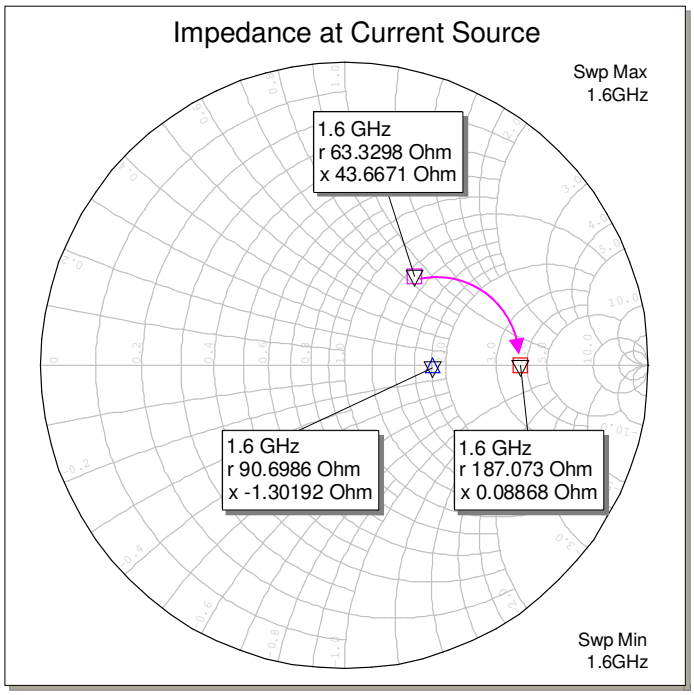


Figure 3.3.9 **Transforming the impedance seen by internal current source of Siemens CFY30 GaAs in the low power operation from 63.3 + *j*43.7Ω (□) to 187.1 + *j*0.1Ω (□) by adding an offset line with a characteristic impedance equal to that of the quarter-wave impedance inverter. The impedance for the high power operation (Δ) remains unaffected.**

An extra offset-line at the output of the peaking amplifier is also required. The reason for this is that the input and output impedance of high power LDMOS FETs is relatively low. This negates the assumption in the ideal theory that during low power operation the output of the peaking amplifier can be seen as an open circuit. This can lead to power leaking from the carrier amplifier into the peaking amplifier, which results in efficiency degradation. As in the case of the carrier amplifier, the impedance seen by the internal current source in the peaking transistor becomes complex at low power levels [15].

This problem can also be corrected by inserting an extra offset line with the same characteristic impedance as the quarter-wave impedance inverter after the output matching circuit. As with the offset line at the carrier amplifier this will only have an effect during low power operation. The length of the offset line can be determined mathematically [19], [20], or as was done in this project, by simulation using Microwave Office. To illustrate the effect of this offset line, data of an peaking amplifier using a Siemens CFY30 GaAs FET will be used. The peaking amplifier, together with its input and output matching circuits, were simulated and the output impedance, denoted by (A) in Figure 3.3.10, was obtained as 41.8 – *j*94.2 Ω. An offset line was then added and its length, θ_p was

adjusted until the impedance seen at (A') crossed the Smith Chart's real axis on the right hand side. An impedance of 305.8 - *j*0.31 Ω was obtained at (A') with the length θ_p = 155.4°

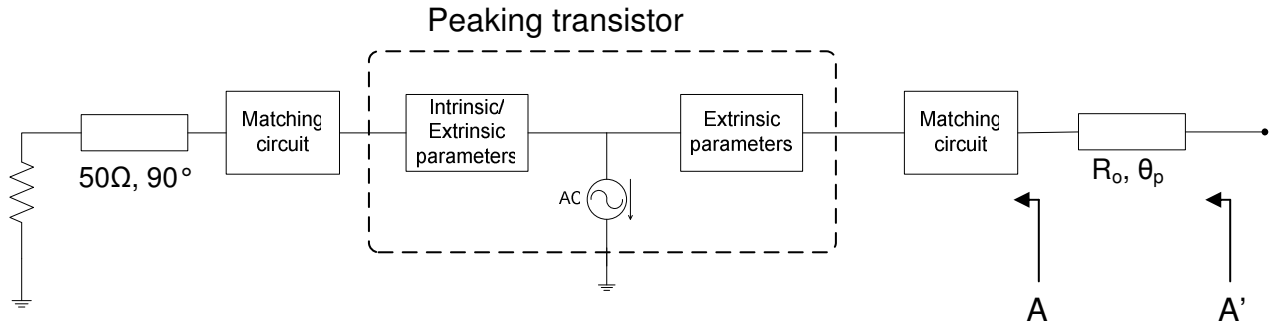


Figure 3.3.10 Determening the length of the offset line to transform the complex output impedance seen at A to a larger real impedance seen at A'.

Figure 3.3.11 shows how the output impedance of the peaking amplifier seen at (A) is transformed from 41.8 – *j*94.2 Ω to 305.8 - *j*0.31 Ω seen at (A') by adding a offset line with a length of θ_p = 155.4°

As was discussed before, the fundamental current components of the carrier and peaking amplifiers are not equal and hamper the load modulation that is needed for the efficiency enhancement. In the ideal theory, where it is assumed that the current components are equal, it follows from equation (2.5) that R_{opt} would be the same for both amplifiers. Looking at Figure 2.3.1 it is clear that a Class C amplifier will have a lower fundamental current component than a Class AB amplifier for the same input signal. The peaking amplifier will thus have a larger R_{opt} than the carrier amplifier and it will be necessary to distinguish between the two by denoting the optimal impedance for the carrier amplifier as R_{optC} and for the peaking amplifier as R_{optP}.

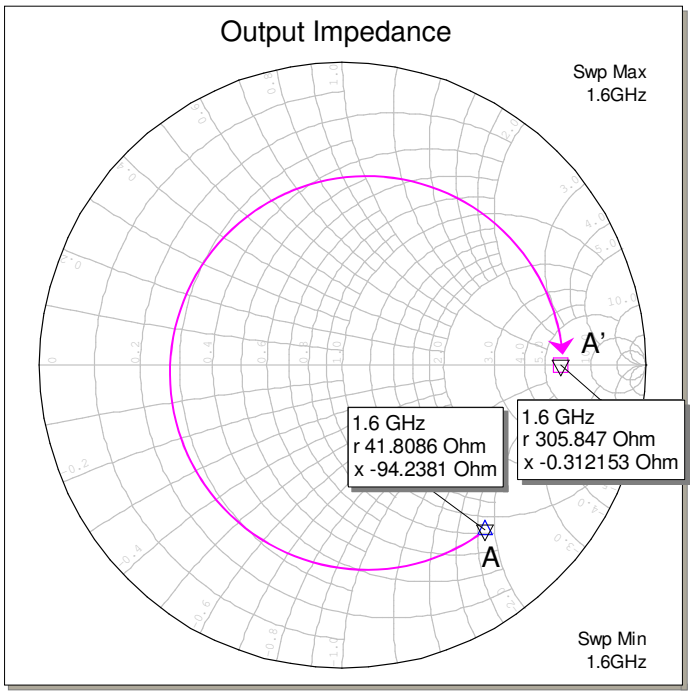


Figure 3.3.11 Output impedance of the peaking amplifier without offset line (A) and with offset line θ_p = 155.4° (A').

In the ideal theory, only a quarter-wave impedance inverter is necessary at the output of the carrier amplifier to achieve the load modulation that is needed to improve the overall efficiency of the system. To ensure that the peaking and carrier amplifiers' RF output signals are in phase at the output combiner, only a 90° delay line in front of the peaking amplifier is necessary (see Figure 3.2.6). With the extra output matching circuits and offset lines explained in this section, this 90° delay line will not necessarily be the correct length to ensure that the two amplifiers are in phase at the output. A specific length for the delay line will thus have to be calculated for different Doherty amplifiers.

Not only is it necessary to calculate a specific delay line for different Doherty amplifiers to ensure in-phase signals at the output combiner, but the peaking amplifier needs to have a relatively flat phase response to achieve in-phase signals from peak output power down to 6 dB back-off [21]. The requirement of having a flat phase response as a function of input power has an impact on the choice of the peaking amplifier's gate biasing voltage. The gate biasing voltage is also what controls the switch-on point of the peaking amplifier. Therefore a necessary trade-off has to be made to ensure a relatively flat phase response from the peaking amplifier which in turn will move the switch-on point away from the desired 6 dB back-off point.

The practical side of the Doherty amplifier has now drastically changed the simple design of the ideal theory. A schematic taking all these aspects into account would look something like Figure 3.3.12. This figure represents the low power operation when the peaking amplifier is not conducting and Figure 3.3.13 represents the high power operation when both the amplifiers is saturated and functioning at their highest efficiency.

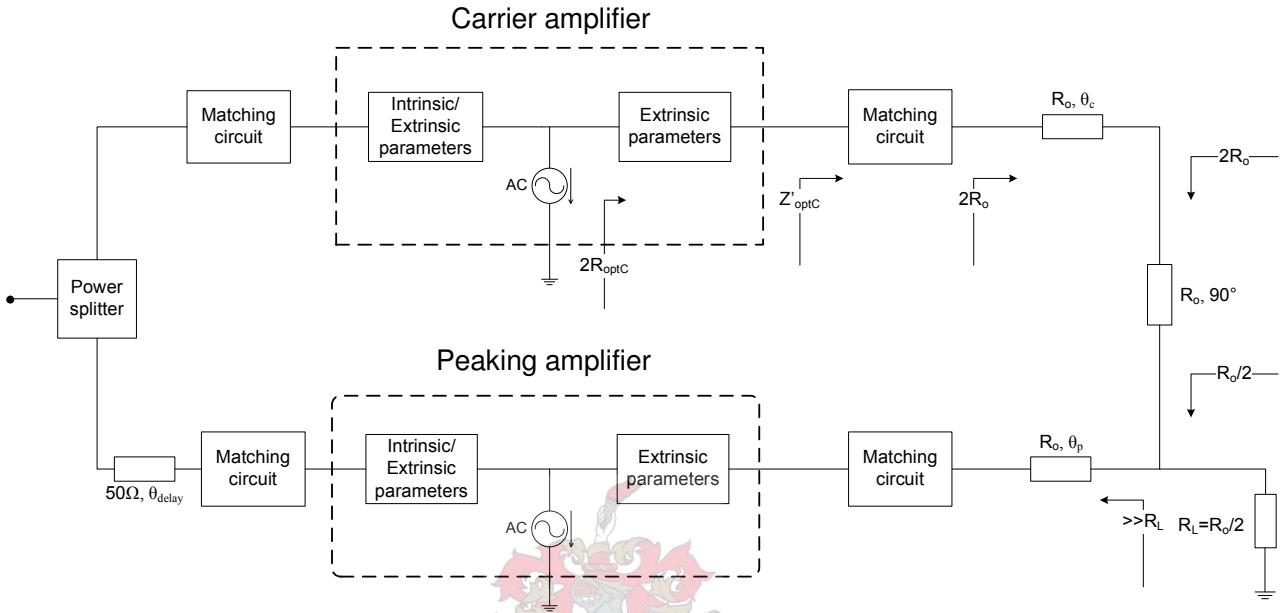


Figure 3.3.12 Classical Doherty amplifier at low power incorporating the practical aspects discussed in this section showing the impedances that should be seen at various points in the circuit.

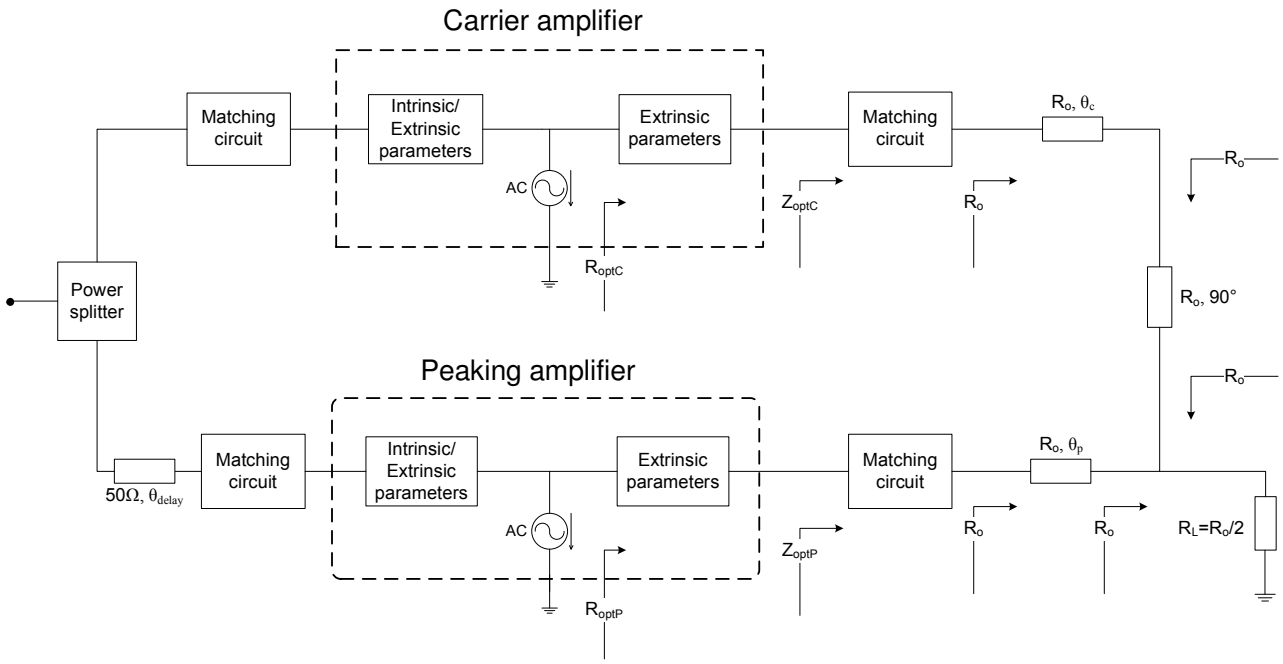


Figure 3.3.13 Classical Doherty amplifier at PEP incorporating the practical aspects discussed in this section showing the impedances that should be seen at various points in the circuit.

3.4 Conclusion

A significant number of aspects regarding the implementation of ideal Doherty Amplifier theory in practice is discussed. One of the main problems associated with the Classical Doherty is the unequal fundamental current components of the carrier and peaking amplifiers at PEP and this is discussed in Section 3.3. During most of the practical considerations discussed in this section this problem is ignored and only the extra elements contributed by the transistor packaging and matching circuits are taken into account.

In Figure 3.3.13 all the aspects that are taken into consideration during the design of a Doherty amplifier are shown. It can be seen that unequal current components have not been included, since impedances of R_o are indicated at the input and output sides of both offset-lines. In order to design a first Doherty amplifier some assumptions have to be made and during the design of the two Doherty amplifiers of Chapter 4 and Chapter 5, equal current components at PEP are assumed during the design process.

Chapter 4

Small-Signal Doherty Amplifier Design and Characterisation

4.1 Introduction

Ideal Doherty amplifier theory, as well as the practical considerations that should be taken into account during the design of a Doherty amplifier is investigated in Chapter 3. Now the design and measurement of a small-signal amplifier will be described.

In this project, two Doherty amplifiers are designed, built and measured. The first, discussed in this chapter, is a small-signal Doherty amplifier with CFY30 GaAs FET transistors from Siemens (Datasheet is provided in Appendix A) and the second (see Chapter 5) is a power amplifier using 10W MRF282 (Datasheet is provided in Appendix A) transistors from Motorola (or Freescale, as the semiconductor division is now called).

The small-signal Doherty amplifier is designed first, in order to validate the design procedure before moving on to the much larger 10W power amplifier. A custom measurement setup is described. This includes software that is developed to measure the gain, compression and efficiency curves of an amplifier. In order to verify the setup, the small-signal amplifier is measured on a non-linear network analyzer.

4.2 Design of a Small-signal GaAs FET Doherty Amplifier

4.2.1 Stability, Biasing, calculating R_{opt} and Using Small-Signal Parameters to Design for Large-Signal Operation

Before resuming the amplifier design, the stability of the transistor used must be ensured. Carson's [23] method of using the admittances of the transistor is used to design the necessary stabilising network. This method's stability criteria are:

$$g_i > 0$$
$$g_o > 0 \quad and$$
$$g_i g_o > \frac{P+M}{2}$$

where

$$g_i = \Re\{y_{11}\}$$
$$g_o = \Re\{y_{22}\}$$
$$y_{12}y_{21} = P + jQ = M\angle\theta$$

Adding a shunt RC network at the gate terminal with values of 18 pF and 270 Ω satisfies the stability criteria as shown by the graphs in Figure 4.2.1 and Figure 4.2.2. Figure 4.2.3 shows the CFY30 transistor with the stabilising network together with bias decoupling networks. The bias decoupling networks consist of quarter-wave transmission lines which are grounded through capacitors where the DC sources are connected. This has the effect of presenting the RF signals at the gate and drain terminals with an open circuit. A 2k2 Ω resistor is placed at the gate terminal to protect the transistor's gate terminal against possible DC current.

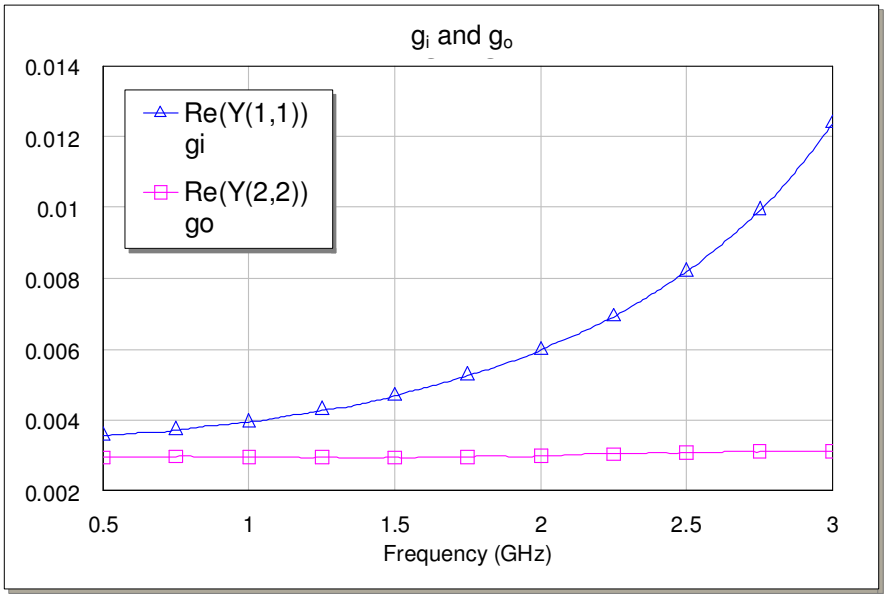


Figure 4.2.1 Stability conditions g_i (Δ) and g_o (□).

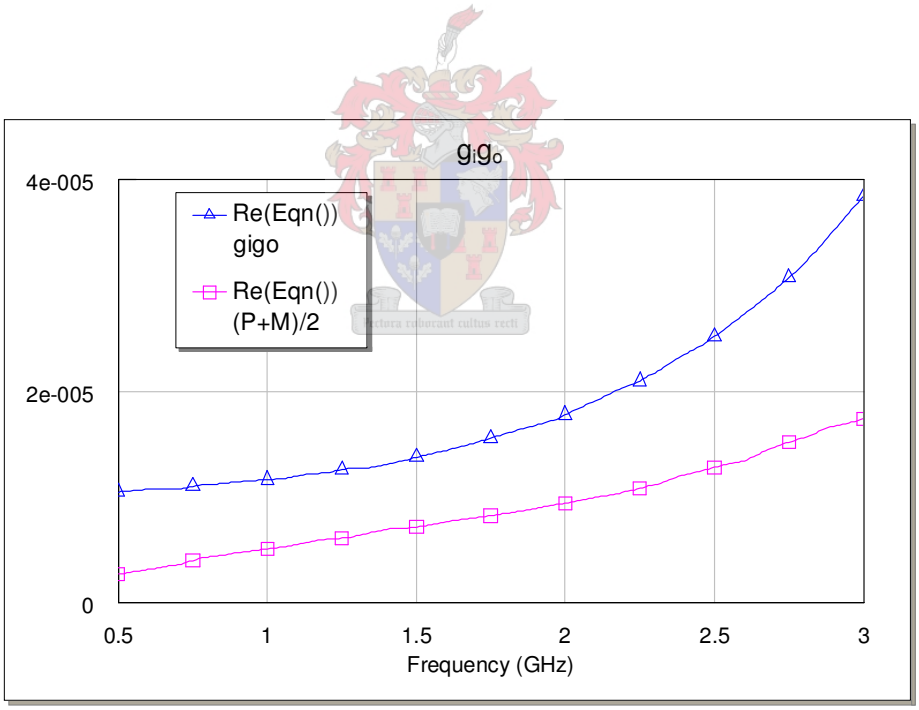


Figure 4.2.2 Stability condition $g_i g_o$ (Δ) and $(P+M)/2$ (□).

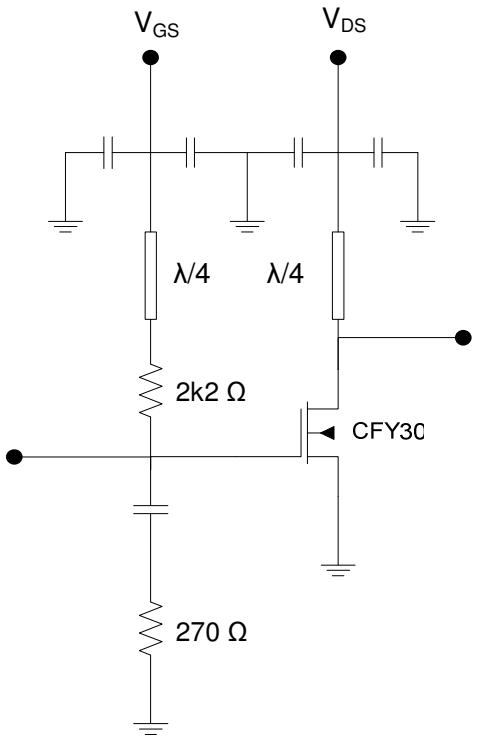


Figure 4.2.3 CFY30 transistor with stabilising network and biasing networks.

The design of the Doherty amplifier is initiated by choosing the bias points for the class AB and class C amplifiers of which the Doherty amplifier will consist. The drain voltage is chosen as V_{DS} = 2.8V to permit maximum voltage swing, being halfway between the rated knee voltage, V_k = 1V, and the rated maximum DC voltage, V_{DCmax} = 5V. After choosing the drain voltage, the gate voltages are determined.

The carrier amplifier's gate voltage is determined first. The carrier amplifier will be biased for class AB operation which fits between class A and class B operation [1]. Cripps [1] defines the input DC bias point for 'mid' class AB condition as V_q = 0.25V, where V_q represents a normalised input DC biased point between 0 (cut-off or pinch-off) and 1 (saturation or open channel). With the CFY30's pinch-off voltage and saturation being between -1.3V and 0V respectively, V_q = 0.25V relates to a gate voltage of V_{GS} = -0.975V. The final gate voltage was chosen as V_{GS} = -1.1V which gives a 'deeper' class AB condition.

The peaking amplifier will be biased for class C operation to achieve the behaviour discussed in Chapter 3. Cripps [1] defines the input DC bias point for 'mid' class C condition as V_q = -0.5V, which relates to a gate voltage of V_{GS} = -1.95V. As explained in Section 3.2.2, Doherty operation requires that the peaking amplifier must start conducting 6 dB below PEP (peak output / envelope power). The exact gate voltage is determined according to this requirement. Because the Doherty configuration also influences the linearity of the system [18], [22], the exact peak output power

cannot be known beforehand. To determine the peaking amplifier's gate voltage, the amplifier's input voltage is used. If it is assumed that the linearity is not influenced, then the peaking amplifier should start conducting when the input voltage amplitude is half of the maximum input voltage amplitude [1], [2]. To determine the maximum input voltage amplitude, the I_D versus V_{GS} curve is used. This curve is calculated in the manner explained in Section 2.3.1, with the biasing voltages for the carrier amplifier being V_{DS} = 2.8V and V_{GS} = -1.1V. The curve is shown in Figure 4.2.4. In this case, the allowed maximum input voltage is 0V. With the carrier amplifier's gate biased at V_{GS} = -1.1V, the maximum input voltage amplitude is 1.1V. The peaking amplifier should then start conducting with an input voltage amplitude of 0.55V. This means the peaking amplifier's gate biasing voltage should be 0.55V below pinch-off. From Figure 4.2.4 the pinch-off voltage is taken as V_p = -1.35V and the peaking amplifier's gate bias voltage is V_{GS} = -1.35 – 0.55 = -1.9V.

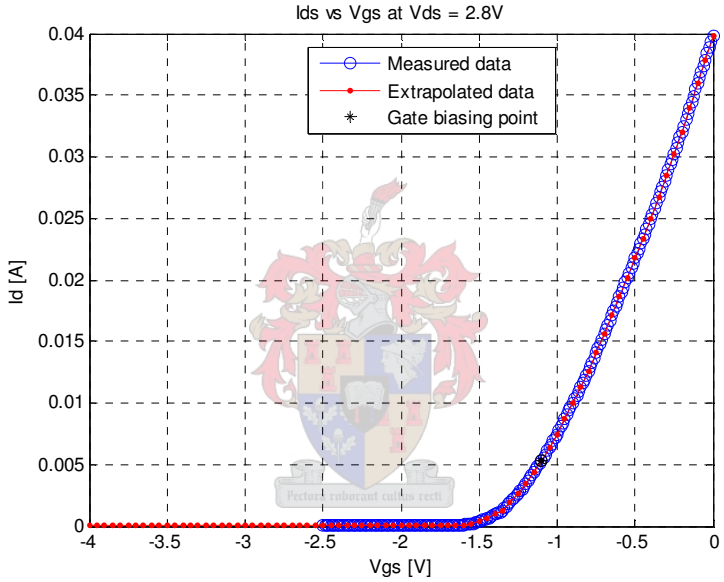


Figure 4.2.4 **I_d vs V_{gs} curve for CFY30 transistor at V_{DS} = 2.8V. Gate voltage of V_{GS} = -1.1V is also indicated.**

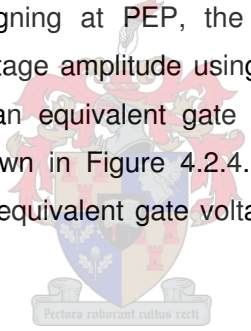
The next step is to use equation (2.5) in calculating the optimal resistance for carrier and peaking amplifiers as explained in Sections 2.2 and 2.3.1. The MATLAB code implemented gives a fundamental current component of I_{1C} = 19.63 mA for the carrier amplifier with the maximum input voltage amplitude of 1.1V. With a knee voltage of V_k = 1V equation (2.5) gives an optimal resistance of

$$R_{optC} = \frac{2.8-1}{0.01963} = 91.7\Omega$$

For the peaking amplifier with the maximum input voltage amplitude of 1.1V a fundamental current component of I_{1P} = 4.9 mA is obtained. This gives an optimal resistance of

$$R_{optP} = \frac{2.8-1}{0.0049} = 367.3\Omega$$

Since the Doherty amplifier theoretically enhances efficiency from PEP down to 6 dB back-off, it changes from a small-signal amplifier to a large signal amplifier at PEP, this is because the transistor is not operating in its linear region anymore. A large signal model would thus have been ideal for use in the design, but large signal models are not widely available and when available, not always reliable [26]. The carrier and peaking amplifiers will initially be designed at PEP. Peak output power will be taken as the output power of the amplifier's 1 dB compression point. A method to utilise small-signal measurements to design an amplifier for large signal operation had to be found. Small-signal measurements are relatively easy to acquire and is used to plot the figures in Section 2.3.1. As the input signal to an amplifier increases, the output signal will also increase (if biased properly) and depending on the shape of the output signal, the DC current component will change. To use small-signal measurements for designing at PEP, the output DC current component will be calculated for the maximum input voltage amplitude using the method described in Section 2.3.1. Using this DC current component, an equivalent gate voltage V'_{GS} can be obtained from the transistor's I_D versus V_{GS} curve, shown in Figure 4.2.4. The small-signal measurements at the designed drain voltage, V_{DS}, and the equivalent gate voltage V'_{GS} will then be used for the design calculations.



With a maximum input voltage amplitude of 1.1V, the DC current component for the carrier and peaking amplifiers are calculated to be 12.7 mA and 2.7 mA respectively. These values then respectively give equivalent gate voltages of -0.8V and -1.25V.

The rest of the design will be split up for the carrier and peaking amplifier and handled individually. The carrier and peaking amplifiers will also be manufactured separately, so that they can be measured separately. Their layouts will be designed in such a way that it will be possible to combine them manually into a Doherty amplifier. The Doherty amplifier is designed for a centre frequency of 1.6 GHz. The design of the carrier amplifier will be explained first.

4.2.2 Carrier Amplifier Design

Now that the optimal resistance for the carrier amplifier is known, and the use of small-signal measurements for designing at PEP has been explained, the carrier amplifier can be designed.

Before the output matching can be designed, the optimal impedance, Z_{optC}, has to be determined. Using the optimiser from Section 2.3.2. Z_{optC} = 84.16 + j13 Ω is calculated to ensure the optimal resistance of R_{optC} = 91.7 Ω. Looking at Figure 3.3.13, the matching section has to convert R_o to Z_{optC}. The choice for R_o is arbitrary at this stage (although in Section 3.3 the possible influence of R_o on the overall load modulation is mentioned) and in the ideal theory it would be equal to R_{optC} . The logical choice would then be to set R_o = R_{optC} = 91.7 Ω. Unfortunately, for the substrate used, a line with a characteristic impedance of 91.7 Ω would be 0.5 mm thick. Even though this is within manufacturing limits, it might pose a problem in the manual combining of the carrier and peaking amplifiers after manufacturing. R_o is therefore chosen as R_o = 50 Ω which gives a reasonable width of 1.6 mm.

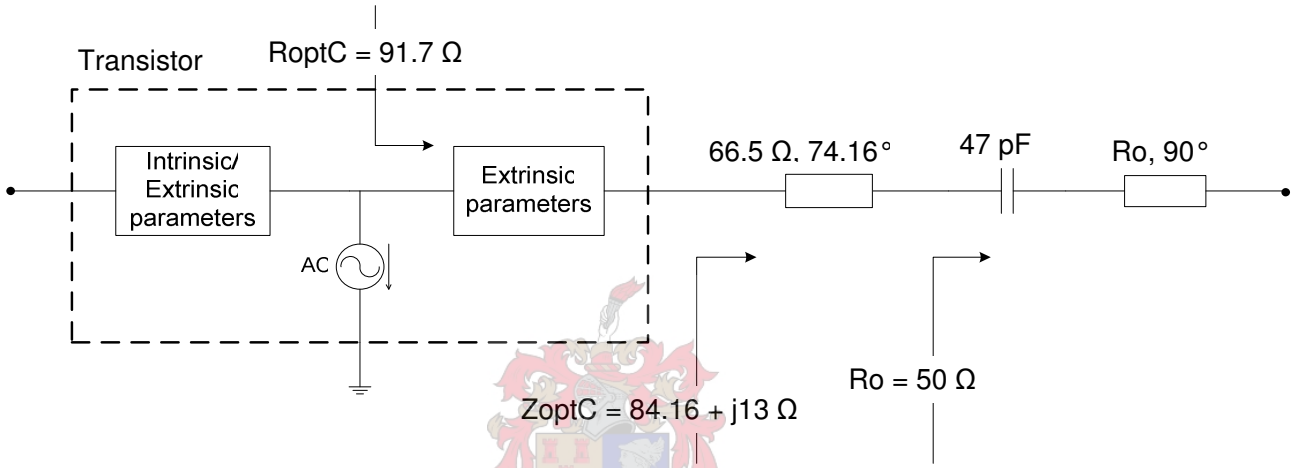


Figure 4.2.5 Carrier amplifier design with matching line, blocking capacitor and impedance inverter.

A matching circuit to convert R_o to Z_{optC} is achieved through the use of a series transmission line with a characteristic impedance of 66.5 Ω and a length of 74.16°. A DC blocking capacitor with a value of 47 pF is placed after the matching section. The quarter-wave impedance inverter with a characteristic impedance equal to R_o is placed after the blocking capacitor and the design at this stage is shown in Figure 4.2.5. The effects of the biasing and stabilising networks are ignored at this stage.

According to the theory explained in Section 3.3, the load impedance seen by the carrier amplifier will increase from 0.5R_o, at 6 dB back-off, to R_o at PEP. Simultaneously the impedance seen by the internal current source should decrease from 2R_{opt} to R_{opt}, but as explained in Section 3.3 this does not necessarily happen and therefore requires an extra offset line. The characteristic impedance of this offset is equal to that of the quarter-wave impedance inverter, Z_T = R_o = 50 Ω. To calculate the length of the offset line, the impedances seen by the internal current source at 6 dB back-off and PEP is simulated in Microwave Office. The schematic in Figure 4.2.6 is simulated twice, first with the load impedance equal to 0.5R_o = 25 Ω and S-parameters of the transistor at the bias point to

represent the low power operation at 6 dB back-off. A second simulation with the load impedance equal to R_o = 50 Ω and S-parameters at the equivalent gate voltage, V'_{GS}, to represent the high power operation at PEP is also performed. At this stage the drain biasing network was added to the simulation and the matching line's length had to be slightly adjusted to 64°. This can also be seen in Figure 4.2.6. An offset line is then added in the simulation. Its length is varied until the impedance seen by the internal current source during low power operation is as close as possible to $2R_{opt}$ = 181.8 Ω. Figure 4.2.7 shows the schematic with the extra offset line.

Figure 4.2.8 shows the impedances seen by the internal current source with and without an offset line. For low power operation the impedance seen is 46.6 – *j*13.6 Ω and for the high power operation it is 88.1 – *j*0.03 Ω. When an offset line of length θ_c = 100° is added, the impedance seen during low power operation transforms to 168.5 + *j*0.2 Ω. The impedance seen during high power operation has undergone a slight change to 86.8 – *j*6.2 Ω, because the CFY30 source inductance L_s = 0.1942 nH is effectively part of the load impedance.

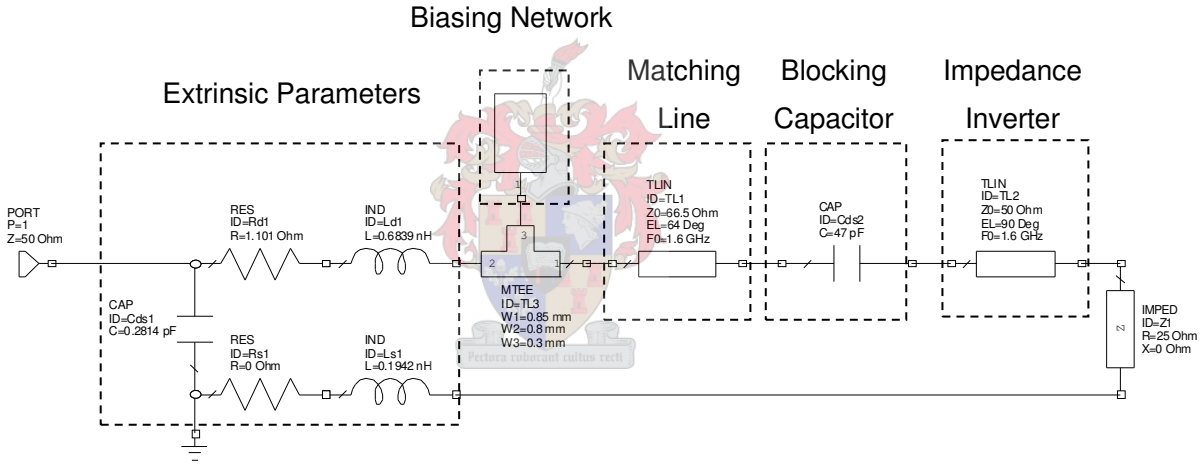


Figure 4.2.6 Extrinsic parameters with drain biasing network, matching section, impedance inverter and load 0.5R_o = 25Ω.

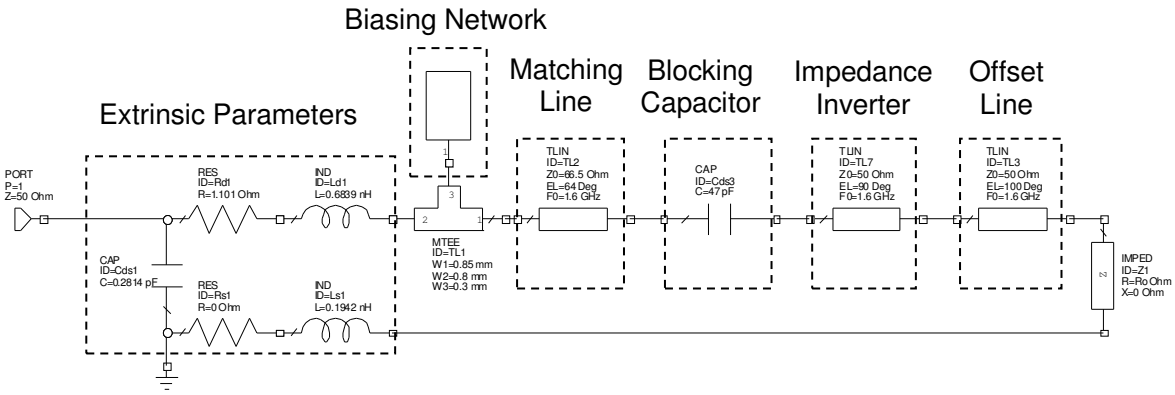


Figure 4.2.7 Extrinsic parameters with drain biasing network, matching, offset line and load R_o.

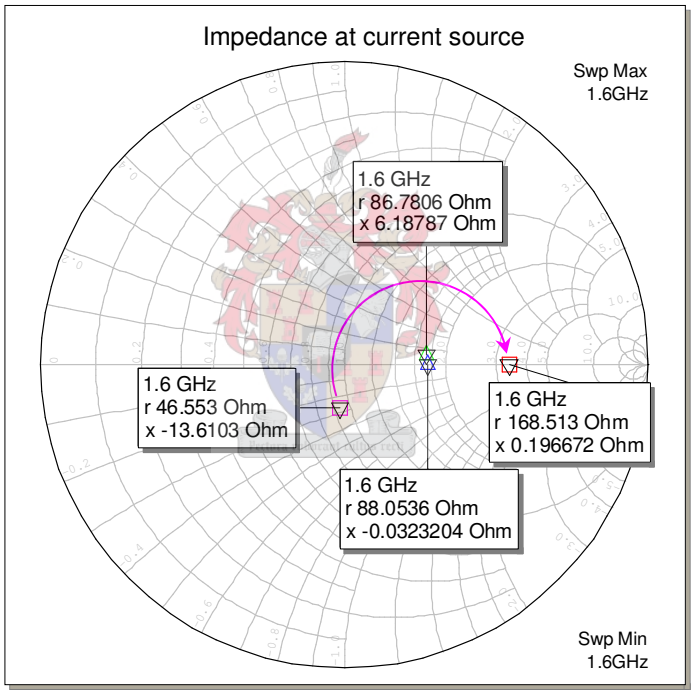


Figure 4.2.8 Transforming the impedance seen by internal current source of the Siemens CFY30 GaAs FET in the low power operation from 46.6 – j13.6Ω (□) to 168.5 + j0.2Ω (□) by adding an offset line with a characteristic impedance equal to that of the quarter-wave impedance inverter and a length of θ_c = 100°. The impedance for the high power operation changes slightly from 88.1 – j0.03Ω (Δ) to 86.8 – j6.2Ω (Δ).

The input matching is also done at PEP. To calculate the input impedance, the S-parameters for the transistor at the equivalent gate voltage, V'_{GS} = -0.8V (as defined in Section 4.2.1) is used. The load resistance also has to correspond to the high power operation and is therefore R_o = 50 Ω. Figure 4.2.9 shows the schematic used to determine the input impedance of the amplifier in order to design

the input matching network. The input impedance is simulated to be 12.5 – *j*26.2 Ω. An input matching circuit consisting of a series transmission line with a length of 94.3° and characteristic impedance of 51.4 Ω, together with a series capacitor of 1 pF, is designed and shown in Figure 4.2.10.

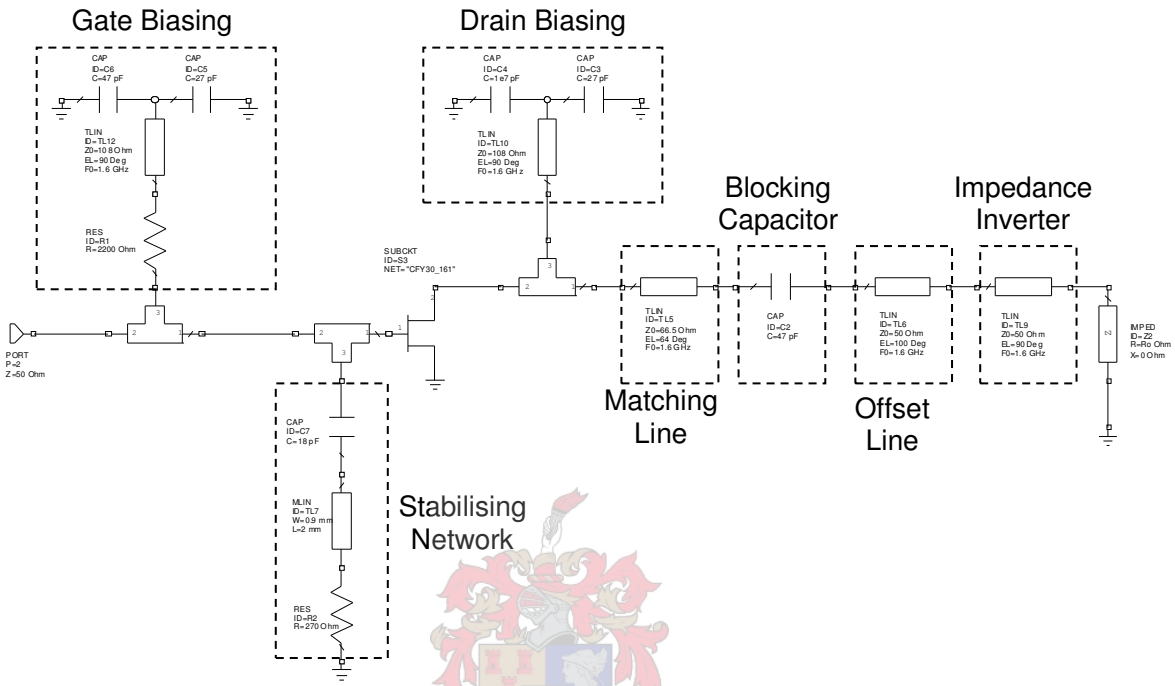


Figure 4.2.9 Schematic used to determine the amplifier's input impedance in order to design the input matching.

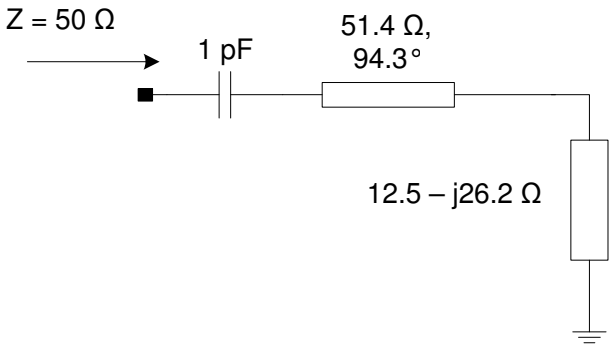


Figure 4.2.10 Input matching for carrier amplifier.

Figure 4.2.11 shows the simulated reflection coefficient for the carrier amplifier with the input matching circuit in Figure 4.2.10 and load impedance of R_o = 50. Two curves are shown in the figure.

One uses the S-parameters for the transistor at the equivalent gate voltage and one using S-parameters at the biasing gate voltage. It can be seen that the design was done using the S-parameters at the equivalent gate voltage, since the point of resonance is at exactly at 1.6 GHz, while the point of resonance for the simulation done at the biasing gate voltage is at 1.62 GHz. This shows that there is a slight difference between using the S-parameters at the equivalent gate voltage and using the S-parameters at the biasing point.

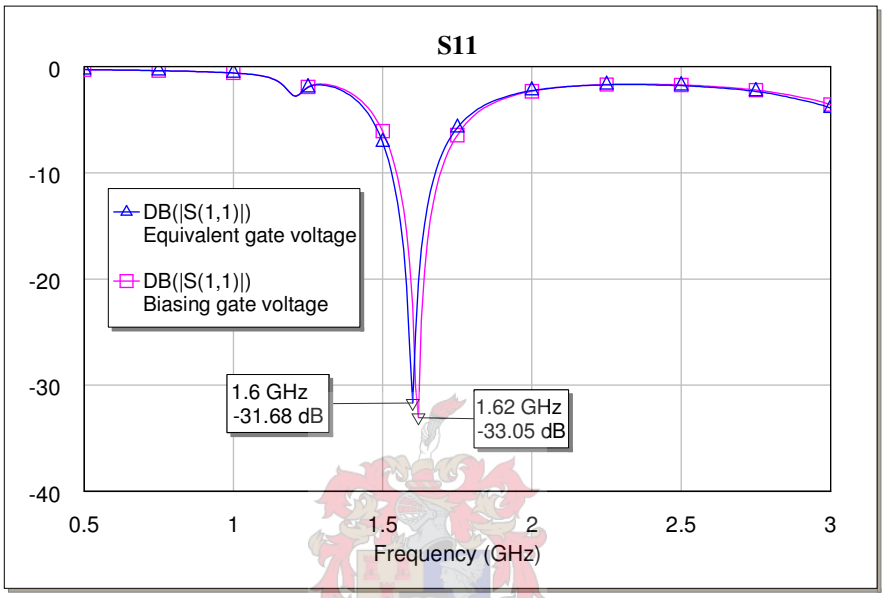


Figure 4.2.11 S_{11} **for carrier amplifier using S-parameters for the transistor at the equivalent gate voltage (Δ) and the biasing gate voltage (□).**

Figure 4.2.12 shows the simulated S_{21} for the carrier amplifier with the two different sets of S-parameters for the transistors. The gain given by the equivalent gate voltage is deceptively high. This is because the S-parameters are a linear representation of the device response and does not account for any clipping and compression due to a large input signal. The maximum gain is at the centre frequency, 1.6 GHz.

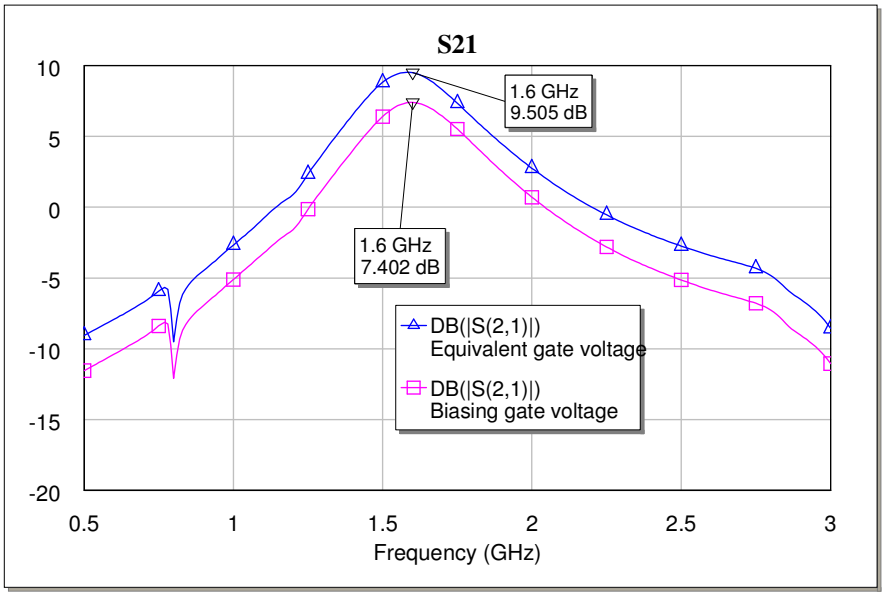


Figure 4.2.12 S_{21} **for carrier amplifier using S-parameters for the transistor at the equivalent gate voltage (Δ) and the biasing gate voltage (□).**

4.2.3 Peaking Amplifier Design

In Section 4.2.1 the optimal resistance for the peaking amplifier, R_{optP} is calculated to be 367.3 Ω. The optimiser described in Section 2.3.2 gives an optimal impedance of Z_{optP} = 162.4 + j170.4 Ω. R_o is already chosen as 50 Ω in Section 4.2.2. Looking at Figure 3.3.13, the matching circuit should convert R_o to Z_{optP}. Figure 4.2.13 shows the matching section, which consists of two series transmission lines with lengths of 71.4°, 90.1° and characteristic impedances of 101.3 Ω and 36.7 Ω respectively. Between these two transmission lines is a 47 pF series capacitor, which mainly acts as a DC block.

According to the ideal theory, the peaking amplifier should show an open circuit at its output during low power operation when the transistor is not conducting. In Section 3.3 it was explained that in practice, this is not necessarily true and that the use of an extra offset line can raise the output impedance. The input of the peaking amplifier is terminated with a 50 Ω load and the output impedance is simulated to be 41.8 – j94.2 Ω. Because the peaking amplifier is not conducting at low input power, the small-signal S-parameters at the biasing gate voltage are used.

By adding a series transmission line with a characteristic impedance equal to R_o = 50 Ω and with a length, θ_p = 155.4°, the output impedance is raised to 305.8 - j0.3 Ω, as shown in Figure 4.2.14. Figure 4.2.15 shows a schematic of the peaking amplifier with the biasing networks, stabilising

network, matching section and the offset line. It also shows how the offset line transforms the output impedance in the whole system.

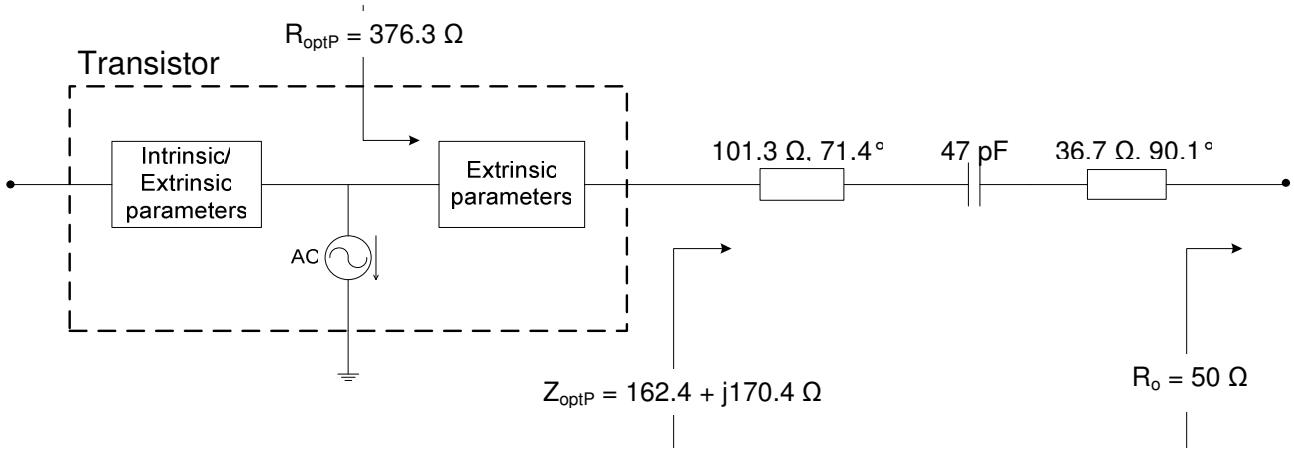


Figure 4.2.13 Peaking amplifier design with matching lines, and capacitor. The capacitor mainly serves as a DC block.

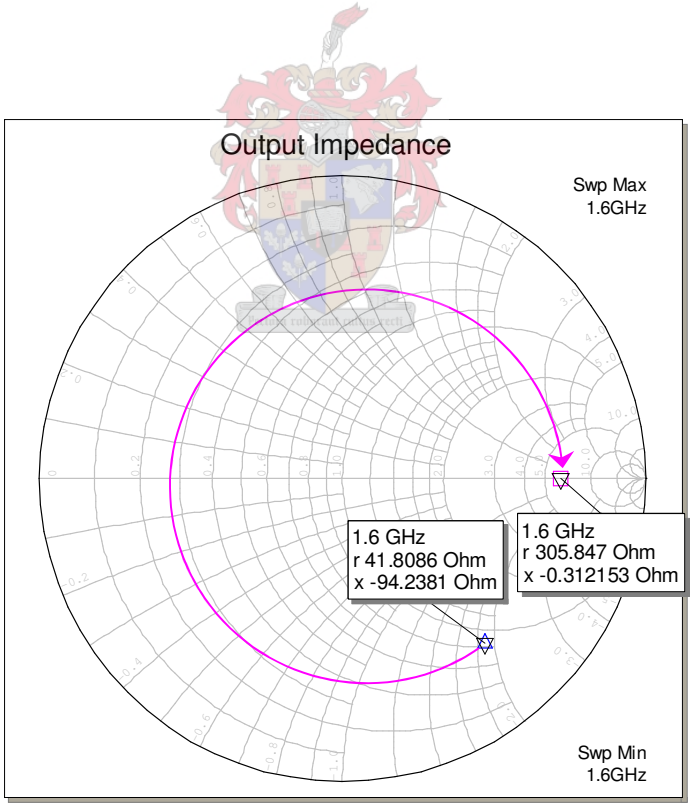


Figure 4.2.14 The output impedance of the peaking amplifier is converted from 41.8 – *j*94.2Ω (Δ) to 305.8 – *j*0.3Ω (□) with an offset line of length θ_p = 155.4°.

To finish the design of the peaking amplifier, only the input matching network is still needed. As in the case of the carrier amplifier, a load of R_o = 50 Ω is added to represent high power operation and

the corresponding S-parameters at the equivalent gate voltage is used for the transistor. An input impedance of 12.7 – *j*25.2 Ω is simulated as shown in Figure 4.2.16. The input matching network consists of a series transmission and capacitor. The transmission line has a characteristic impedance of 52.2 Ω and a length of 91.2°. The capacitor has a value of 1 pF. The input matching circuit is shown in Figure 4.2.17.

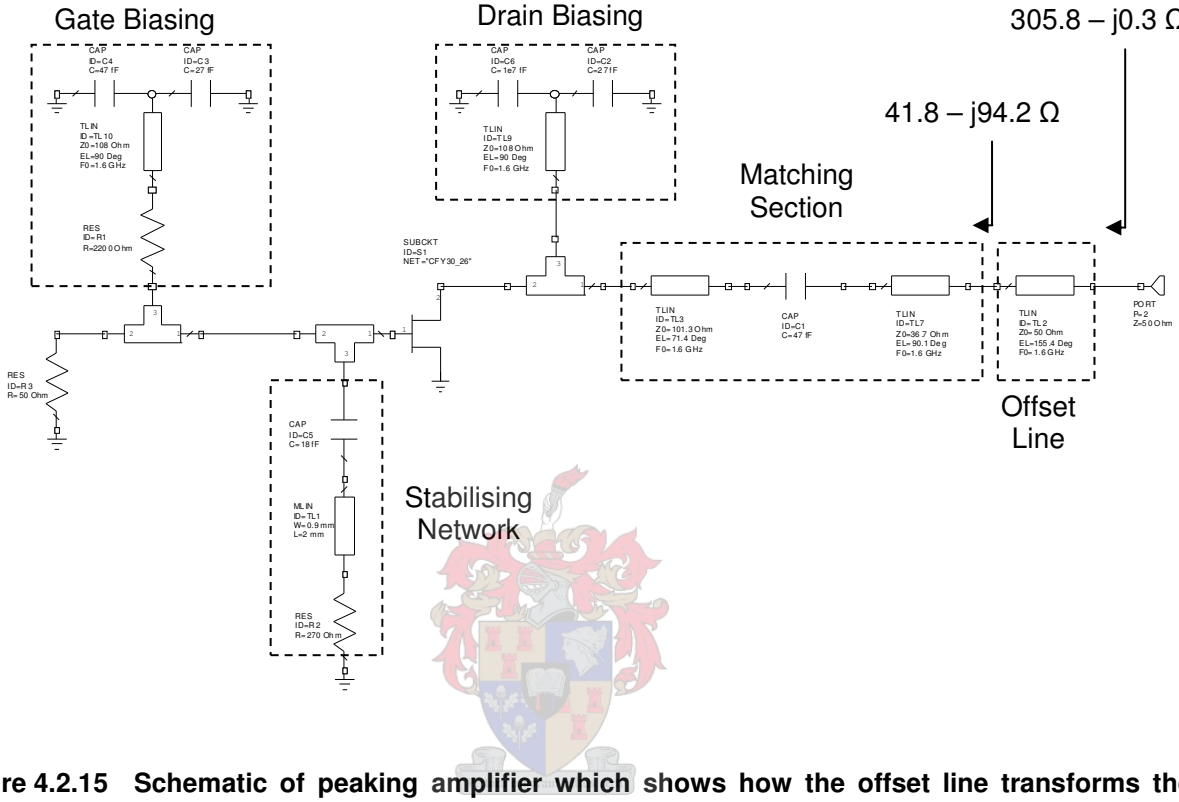


Figure 4.2.15 Schematic of peaking amplifier which shows how the offset line transforms the output impedance to a high resistive value.

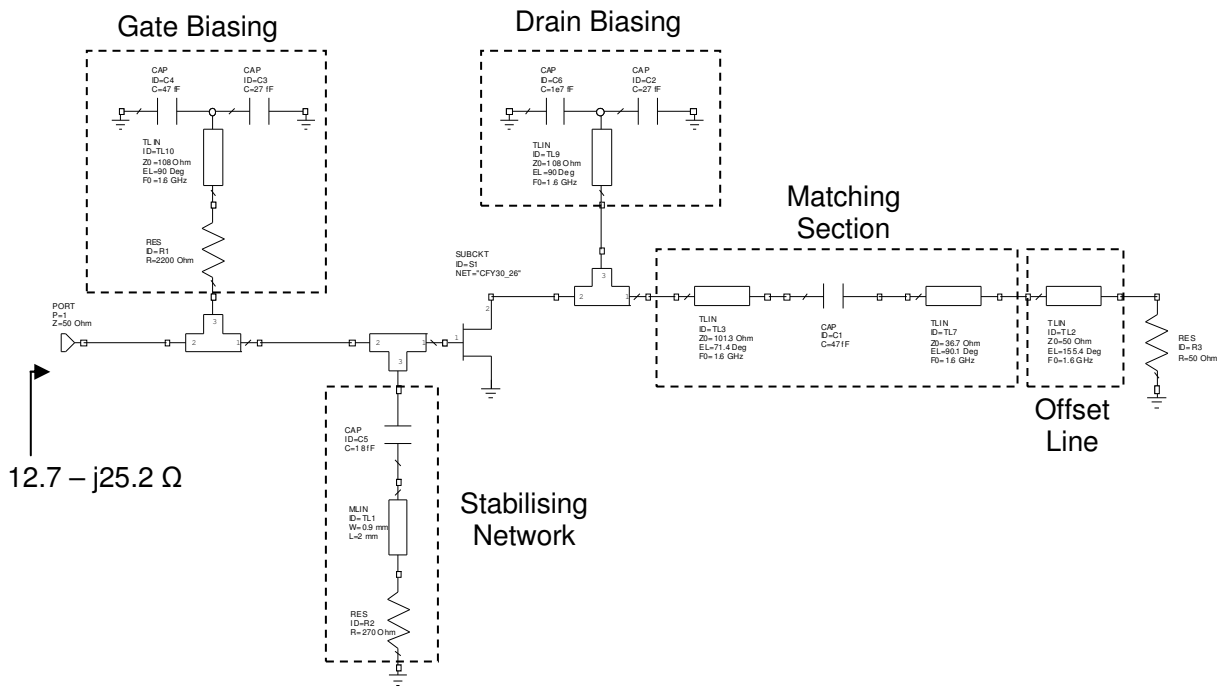


Figure 4.2.16 Schematic used to determine the amplifier's input impedance in order to design the input matching.

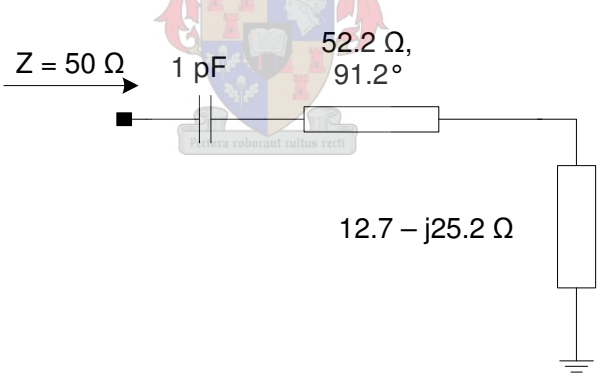


Figure 4.2.17 Input matching for peaking amplifier.

Figure 4.2.18 and Figure 4.2.19 shows the simulation results of S_{11} and S_{21} for the peaking amplifier. Both show two simulations – one uses the S-parameters for the transistor at the equivalent gate voltage and the other the S-parameters at the biasing gate voltage. Since the design is done using the S-parameters from the equivalent gate voltage, the point of resonance is at 1.6 GHz. The point of resonance using the S-parameters at the biasing voltage is 1.68 GHz. This shift in the resonant point is a result of the fact that the peaking amplifier is biased in class C mode. The transistor therefore does not necessarily have a flat phase response and the quality of the input match will thus change with varying input power.

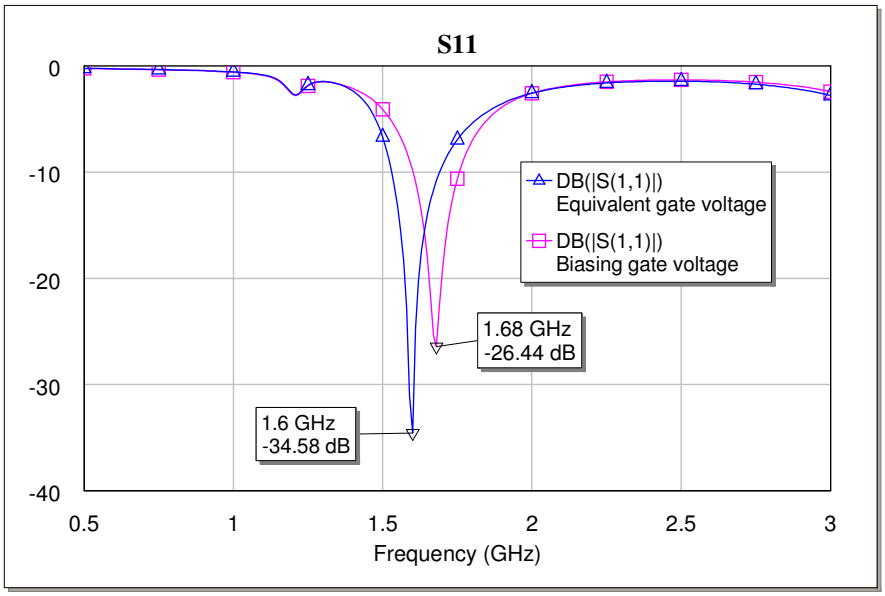


Figure 4.2.18 S_{11} **for peaking amplifier using S-parameters for the transistor at the equivalent gate voltage (Δ) and the biasing gate voltage (□).**

In Figure 4.2.19 there is not a significant change in frequency for the maximum gain. It is only the magnitude of the gain that differs significantly. Since the amplifier is biased in class C mode it will not have any small-signal gain. This is confirmed with the simulation in Figure 4.2.19, showing a gain of -15.96 dB at 1.6 GHz. The simulation with the S-parameters from the equivalent gate voltage shows a much larger gain of 7.87 dB at 1.6 GHz. The gain for the peaking amplifier will be higher at its peak envelope power, because of gain expansion. The magnitude of the gain might be overoptimistic, since linear S-parameters are used. In this design, it is the frequency point for the maximum gain that is considered important and it should lie at the centre frequency of 1.6 GHz.

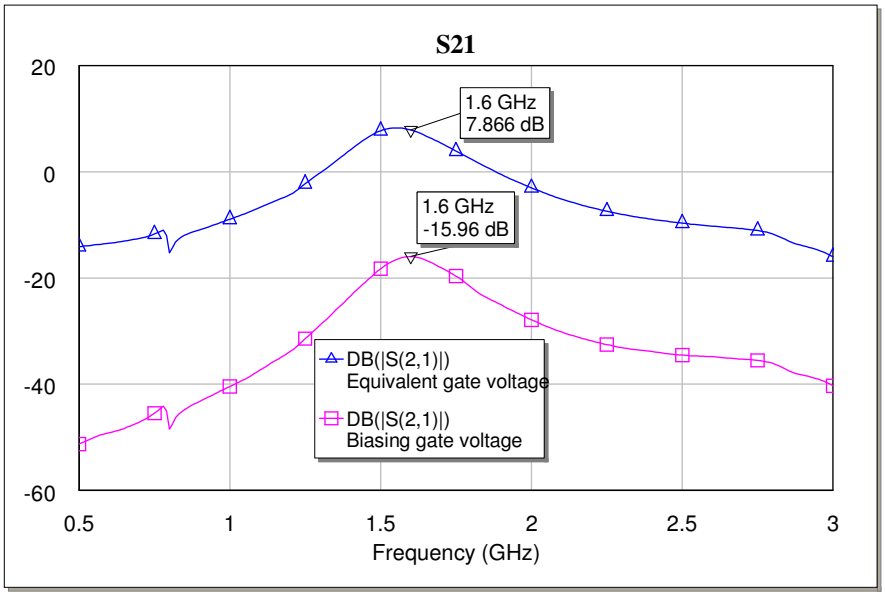


Figure 4.2.19 S_{21} **for peaking amplifier using S-parameters for the transistor at the equivalent gate voltage (Δ) and the biasing gate voltage (□).**

4.2.4 Input Power Divider Design

According to the ideal theory, the peaking and carrier amplifiers' outputs will be 90° out of phase because of the quarter-wave impedance inverter at the carrier amplifiers output. This constitutes the need for phase compensation at the input of the peaking amplifier to ensure in-phase signals at their outputs.

In practice, the amplifiers' output will not necessarily be 90° out of phase due to the matching networks and extra offset lines (Section 3.3). To determine the phase difference between the two amplifiers at PEP, they are simulated using their respective S-parameters at the calculated equivalent gate voltage to represent high power operation. The carrier amplifier's total phase delay at the centre frequency is simulated as 305.62° and the peaking amplifier's as 346.1°. The peaking amplifier's output is thus lagging the carrier amplifier's output by 40.48°.

A 90° hybrid power divider is used at the input of the Doherty amplifier. The carrier amplifier's input will be connected to the lagging port of the divider. The signal entering the carrier amplifier should only be lagging the signal entering the peaking amplifier by 40.48°. Therefore a 49.52° transmission line is added between the peaking amplifier and the divider, as shown in Figure 4.2.20.

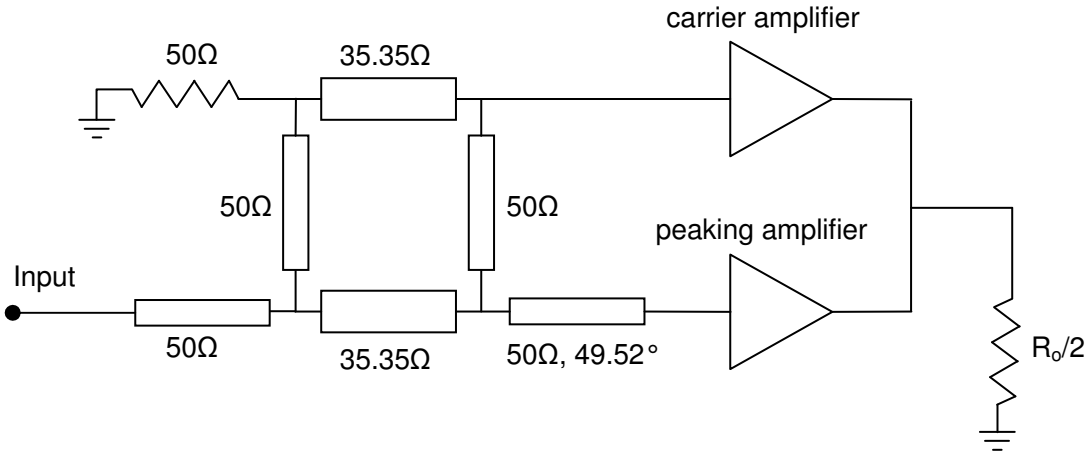


Figure 4.2.20 Schematic showing the extra 49.52° delay line between the divider and peaking amplifier to ensure the input signal at the carrier amplifier is lagging the input signal at the peaking amplifier with 40.48°. The output combining network is not explicitly shown and any matching networks and offset lines are considered to be included in the amplifier symbols.

4.2.5 Load Design

At this stage the carrier and peaking amplifiers and the power divider designs are complete. To be able to measure the amplifiers on their own, they will be manufactured separately. The power splitter and combiner will also be manufactured separately.

Looking at Figure 3.3.12 and Figure 3.3.13, the impedance at the output of the quarter-wave impedance inverter looking towards the load should increase from $0.5R_o$ = 25 Ω during low power operation, to R_o = 50 Ω during high power operation. By manufacturing the amplifiers separately, it is also possible to manufacture different loads for the amplifiers. Three loads are manufactured: a 25 Ω, a 35 Ω and a 50 Ω load. These loads will represent the increase in resistance due to the Doherty load modulation effect when the carrier amplifier is measured on its own. The carrier amplifier can thus be measured with these three loads. The amplifier's individual response can then be compared to its response when used together with the peaking amplifier in a Doherty configuration. Since the measurements are performed in a 50 Ω system, the loads will be realised by using quarter-wave lines to convert 50 Ω to both 35 Ω and 25 Ω.

By simply joining the offset lines of the carrier and peaking amplifiers, the power combiner is formed. Phase compensation is applied at the input side of the amplifiers, as explained in Section 4.2.4. The load now seen by the Doherty configuration is R_L = $0.5R_o$, as shown in Figure 3.3.12 and Figure 3.3.13. In other words, with R_o = 50 Ω (as previously chosen in Section 4.2.2), the load becomes

R_L = 25 Ω. Since the Doherty amplifier will be tested in a 50 Ω system, a quarter-wave line with characteristic impedance of 35.35 Ω is added to convert 50 Ω to 25 Ω, as shown in Figure 4.2.21.

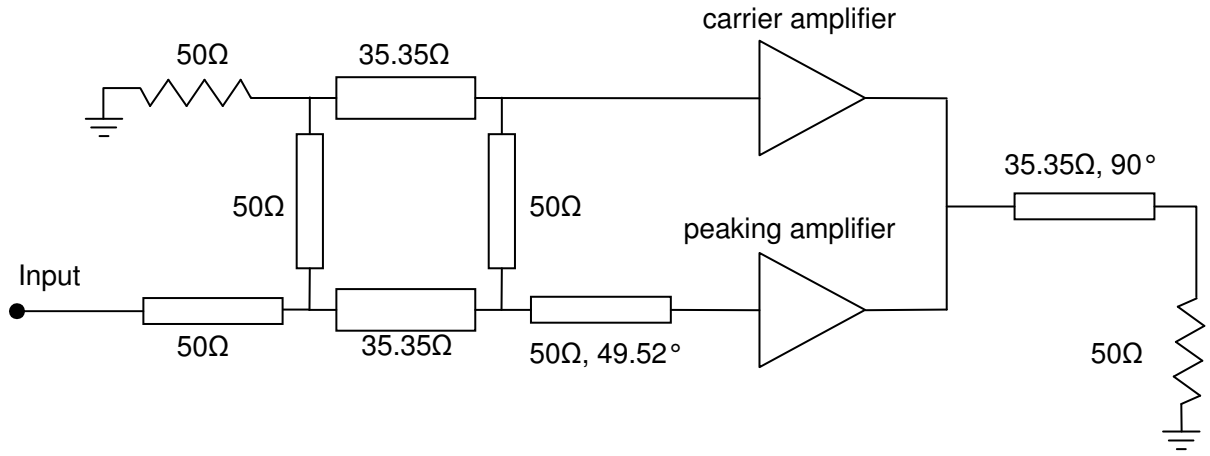


Figure 4.2.21 Schematic showing the 35.35Ω quarter-wave line at the output, which converts the 50Ω load to a 25Ω load. The output combining network is not explicitly shown and any matching networks and offset lines are considered to be included in the amplifier symbols.

4.2.6 Design Layout

The amplifiers are fabricated on 0.778 mm-thick GILL substrate with a relative permittivity of 3.86 and conductor thickness of 22 μm.

Figure 4.2.22 and Figure 4.2.23 respectively show the layouts of the carrier and peaking amplifiers. The offset lines do not form part of their layouts, but is incorporated in the power combiner and joint load layout shown in Figure 4.2.24. The layout for the 90° hybrid power divider with the phase compensation lines is shown in Figure 4.2.25. These four layouts can be combined on an aluminium plate to form a Doherty configuration, as shown in Figure 4.2.26.

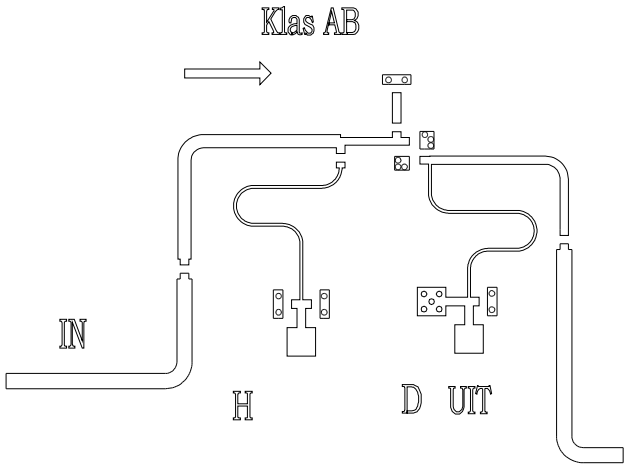


Figure 4.2.22 Layout of the carrier amplifier.

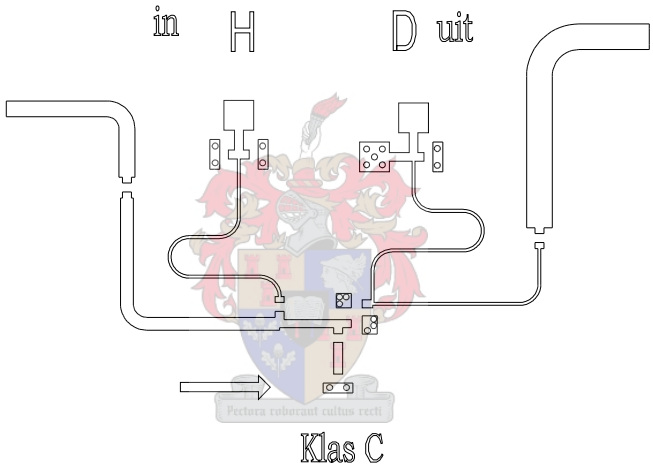


Figure 4.2.23 Layout of the peaking amplifier.

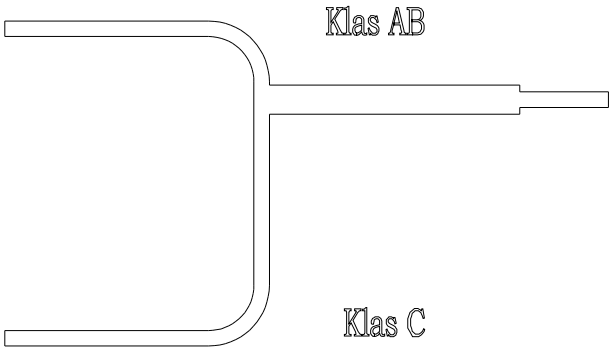


Figure 4.2.24 Layout for carrier and peaking amplifier offset lines combined at joint load.

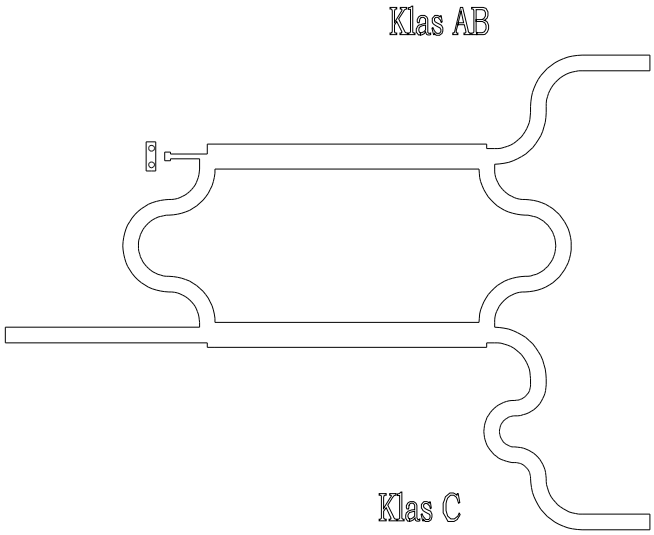


Figure 4.2.25 Layout for 90° hybrid power divider with phase compensation lines.

The three load conversions discussed in Section 4.2.5 are manufactured for both the carrier and peaking amplifiers. Because the offset lines do not form part of the amplifiers' layouts, they are also incorporated as part of the load layouts shown in Figure 4.2.27. These layouts consist of the offset lines and quarter-wave transformers to achieve the three different loads. These load conversion layouts can now also be used together with the amplifiers. This makes it possible to measure the carrier and peaking amplifiers separately, with three different loads (25 Ω, 35 Ω and 50 Ω). For instance, if the carrier amplifier is to be measured with a 25 Ω load, the layouts will be joined together, as shown in Figure 4.2.28. Note that an extra input line is added in front of the amplifier. This is done so that the power divider and combiner used for the Doherty configuration (Figure 4.2.26) can simply be replaced with the input line and load conversion, whilst still using the same aluminium plate as a base.

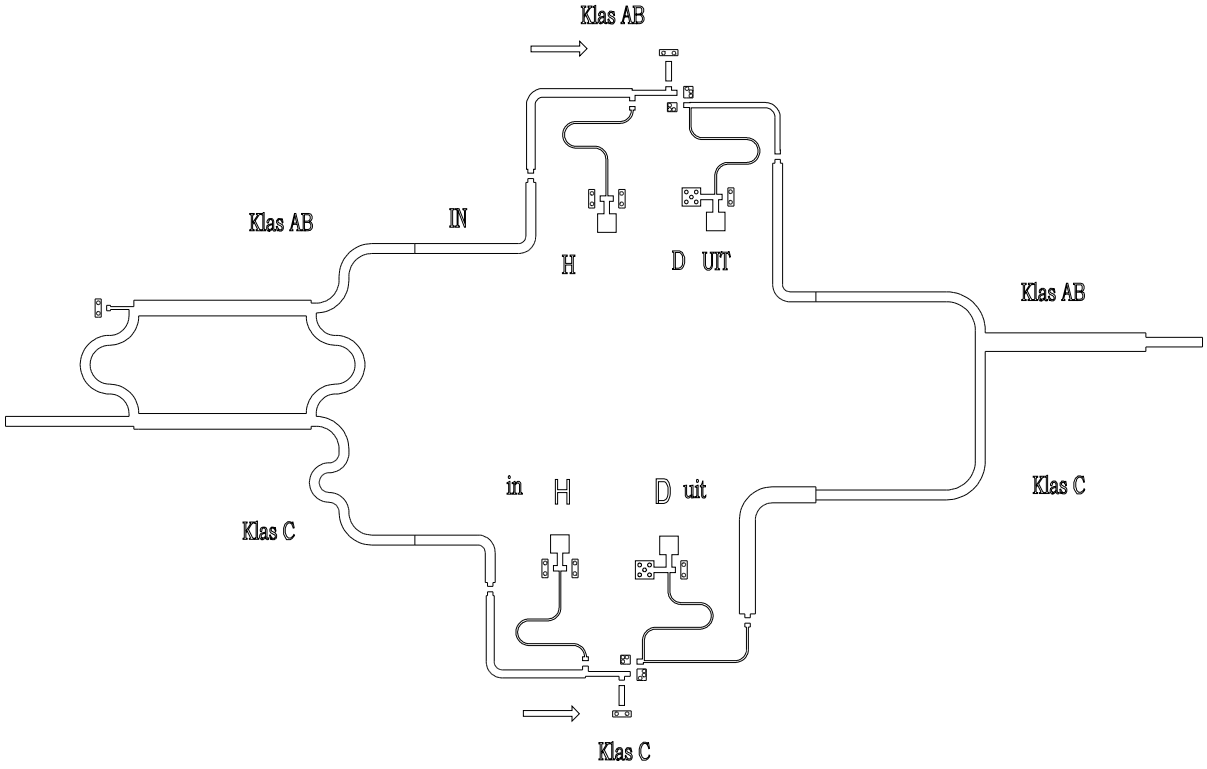


Figure 4.2.26 Joining the layouts to form a Doherty configuration.

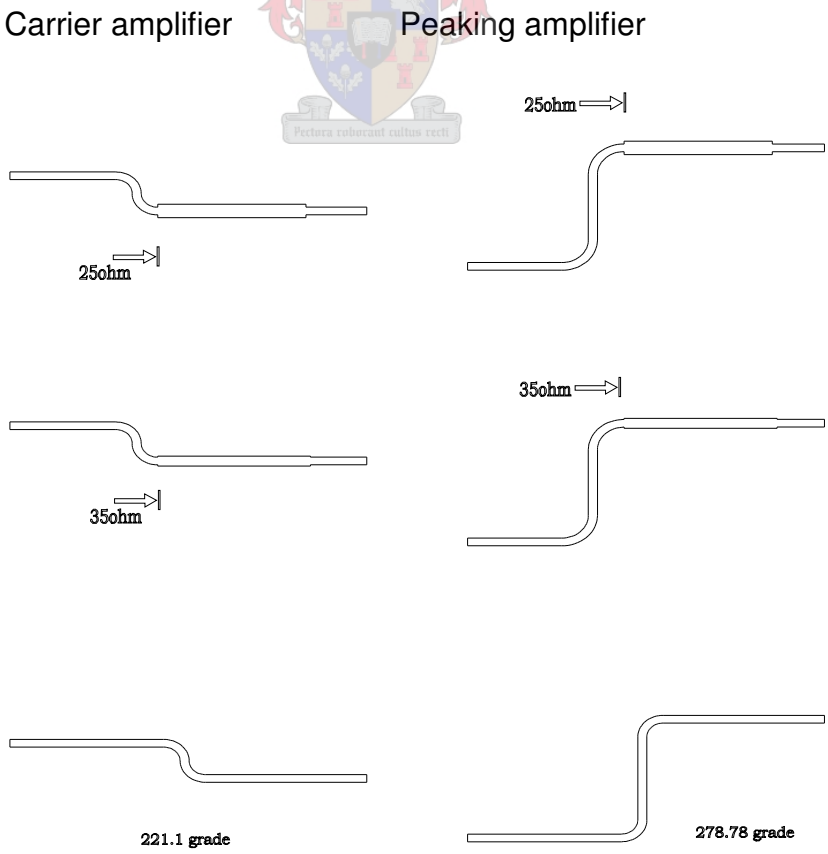


Figure 4.2.27 Layouts for load conversions for the carrier and peaking amplifiers. The offset lines form part of the layouts.

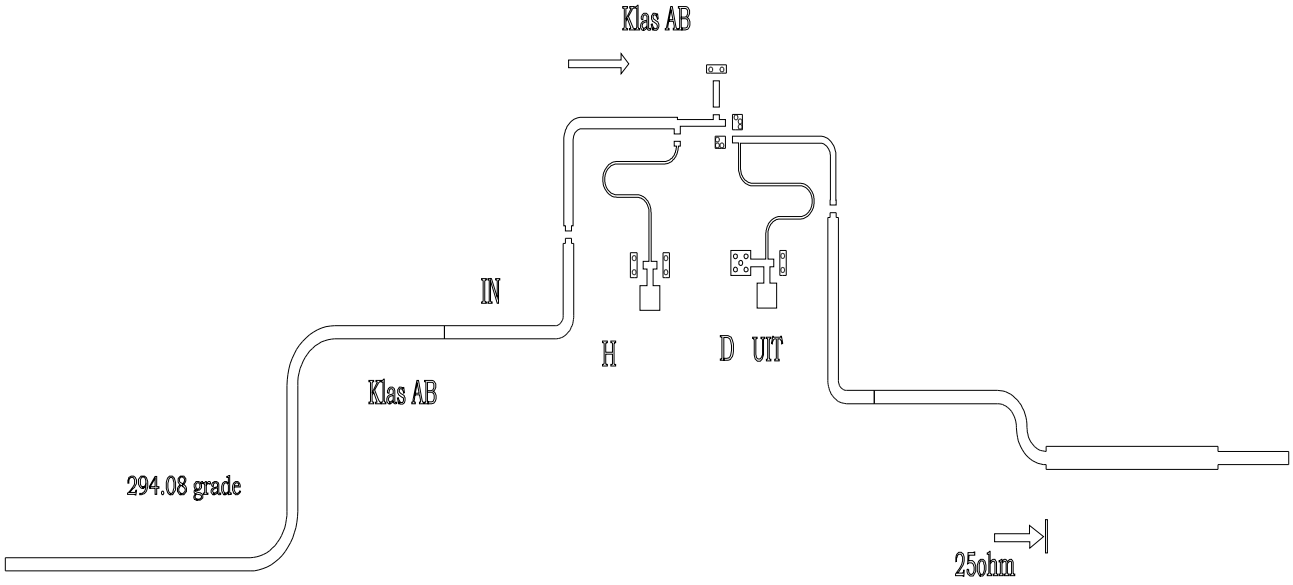


Figure 4.2.28 Layout configuration to measure the carrier amplifier on its own wit a 25Ω load.

The performance of the Doherty configuration is compared to a balanced class AB amplifier. By joining two carrier amplifiers in parallel, a balanced class AB amplifier is formed. Two of the designed 90° hybrids are used: one at the input, which serves as a power divider and one at the output, which serves as a power combiner. The balanced class AB amplifier is shown in Figure 4.2.29.

A photo of the manufactured design in Doherty configuration, together with the extra load conversions and input lines, is shown in Figure 4.2.30.

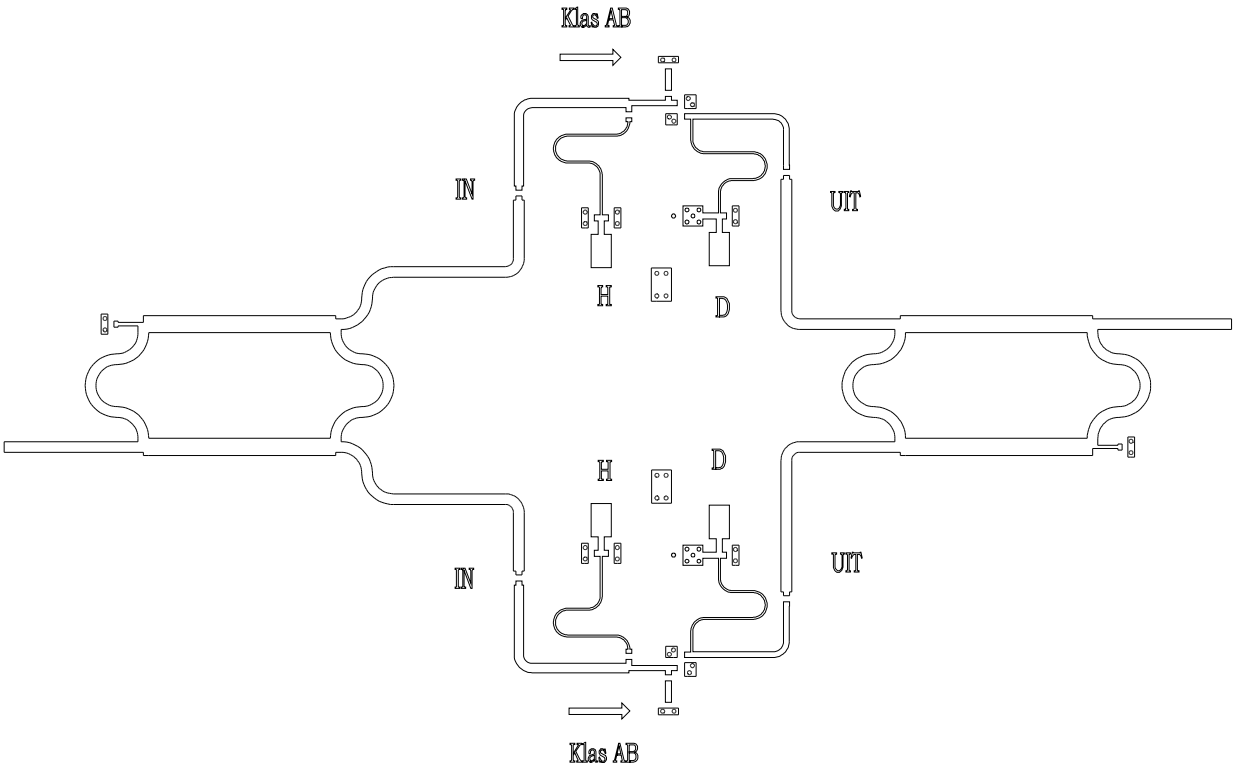


Figure 4.2.29 Layout of the balanced class AB amplifier.

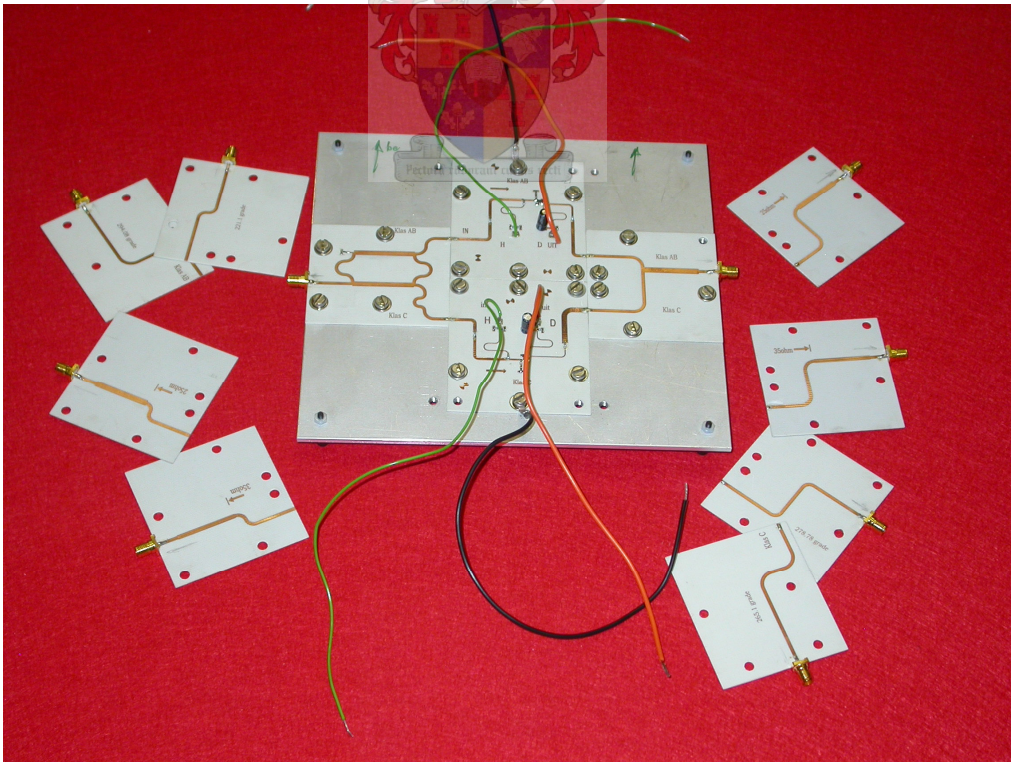


Figure 4.2.30 Photo of the manufactured design in Doherty configuration with extra load conversions and input lines also shown.

4.3 Measurement Setup and Software

4.3.1 Setup and Software

This thesis focuses mainly on the efficiency enhancement characteristic of the Doherty amplifier. It is therefore important to be able to drive the amplifier into saturation and to accurately measure the amplifier's gain during large signal operation. A linear network analyser measures small-signal gain. Measurements will thus have to be made with the use of a signal generator and spectrum analyser. To eliminate the effects of any cable losses, a calibration procedure is needed.

The automated measurement process with the use of the GPIB control interface as described in [25] is used, but different code was written to control the equipment.

For a final measurement setup, as shown in Figure 4.3.1, a calibration procedure is needed to calculate the gain between point B and C. Calibration is performed in three steps.

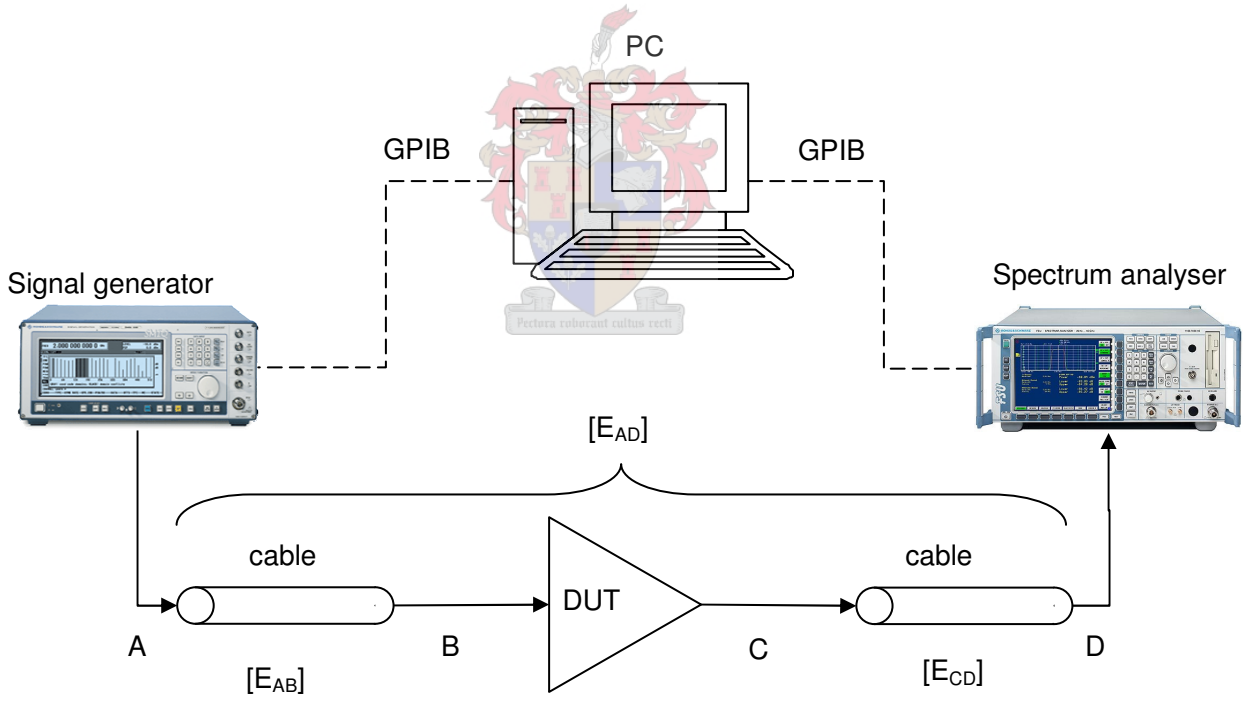


Figure 4.3.1 Measurement setup controlled with GPIB interface. All error matrices are shown.

First, the error matrix [E_{AB}] between point A and B is determined by measuring the power at point B, as shown in Figure 4.3.2. This measurement is done by specifying a vector of input powers and frequencies for the signal generator at point A. The power meter measures the output power at point

B. The columns of the error matrix, [E_{AB}], contain the difference between the specified input power vector, at point A, and the measured power vector, at point B, for each specified frequency.

The second step is the calculation of the error matrix [E_{CD}]. However, it cannot be measured directly as in the case of [E_{AB}], because it would implicitly (and incorrectly) assume that the signal generator is accurate and has no compression. Therefore, point B and C is connected together and the total error matrix, [E_{AD}], between point A and D is measured. Once again, a power vector and frequency vector is specified for the signal generator. The output power at point D is measured with a spectrum analyzer. [25] explains how the measurements can be kept as accurate as possible, by keeping the resolution and video bandwidth as well as the attenuation constant, whilst adjusting the reference level to the measured peak power. [E_{AD}] is constructed in the same way as [E_{AB}] by using the difference between the specified power at point A and the measured power at point D. Since [E_{AB}] is known, the power at point C can be calculated. Now the error matrix between point C and D, [E_{CD}], can be constructed by using the difference between the calculated power at point C and the measured power at point D.

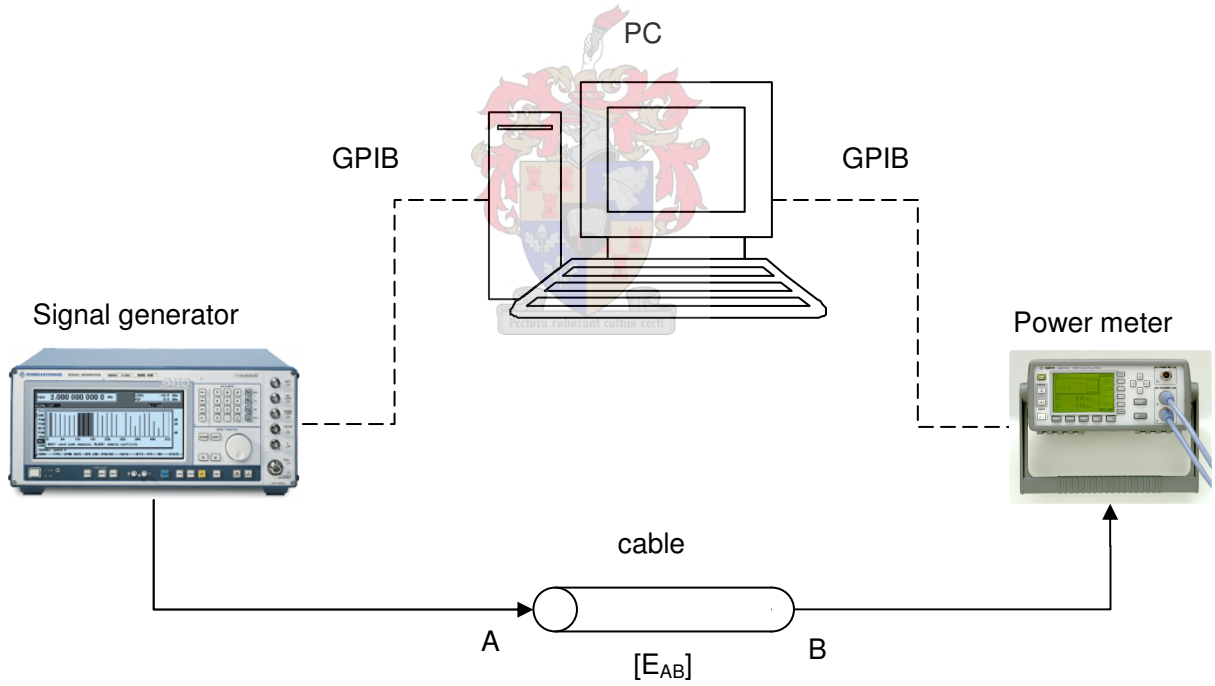


Figure 4.3.2 Setup to calculate error matrix [E_{AB}] between point A and B.

The amplifier under test can now be measured, as shown in Figure 4.3.1. Specified power and frequency vectors are supplied to the signal generator. The specified power at point A and the measured power at point D are then corrected with the use of the error matrices [E_{AB}] and [E_{CD}]. After this calibration, the actual input power which the amplifier receives at point B and the actual power that exits the amplifier at point C can be determined. The amplifier's gain can now be calculated accurately, since the effects of the cables are taken into account.

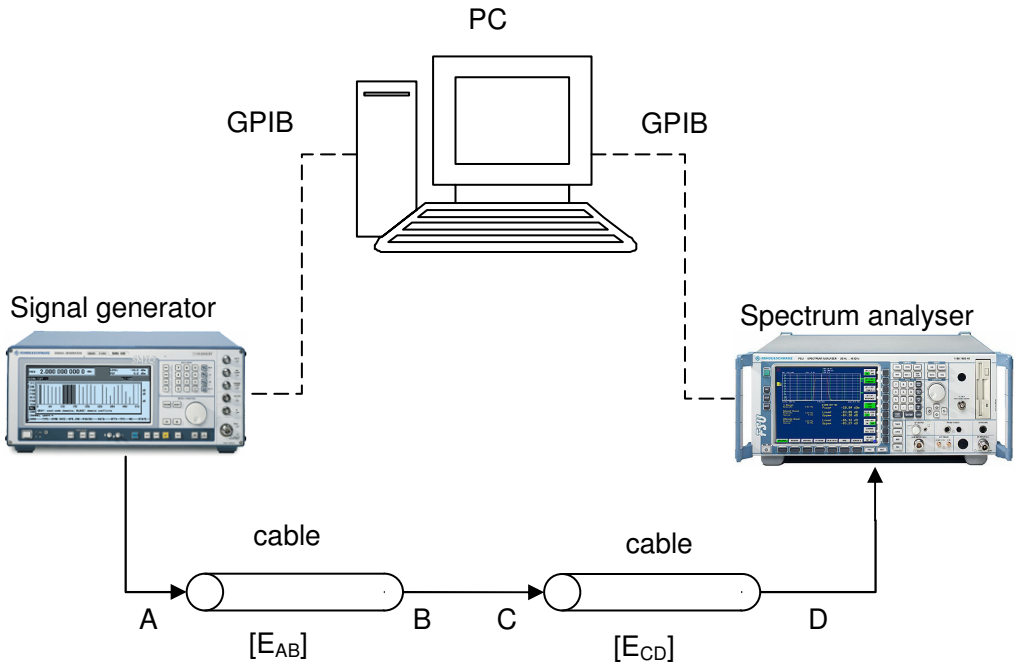


Figure 4.3.3 Setup to calculate error matrix [E_{AD}] between point A and D.

The setup also uses programmable DC sources for the amplifier's biasing. These DC sources are controlled through the GPIB interface and measures the DC current for every specified input power. By multiplying the DC current, I_{DS}, with the drain voltage, V_{DS}, the amplifier's DC power dissipation, P_{DC}, is obtained. The amplifier's drain efficiency is then calculated as

$$\eta = \frac{P_{RF}}{P_{DC}}$$

where P_{RF} is the amplifier's output power at point C, converted to Watt.

The amplifier's power added efficiency, PAE, is calculated as

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}}$$

where $P_{out} = P_{RF}$ and P_{in} is the amplifier's input power at point B, converted to Watt.

4.3.2 Measurement Verification using Non-Linear Measurements

The transmission phase response versus input power of each of the transistors used in the Doherty amplifier is predicted from simulation, using measured S-parameters at an equivalent gate voltage. An important part of the design procedure is to verify these predicted phase responses against measurements. Not only do the simulated results need to be verified, but also the calibration procedure described in Section 4.3.1.

The measurements used to verify the simulation technique and calibration procedure were performed on a large-signal network analyser (also known as a non-linear network analyser) at the Katholieke Universiteit Leuven (K.U.Leuven), Leuven, Belgium.

A non-linear network analyser measures the amplitude and phase of all the specified harmonics of a signal. This is achieved by capturing both the incident and scattered travelling voltage waves at the ports of the device being measured [30]. Therefore, the system allows calibrated measurements to be made of transmission phase response versus input power. In addition, output versus input power at a particular harmonic can be measured. In this project, measurements are made at the fundamental frequency (1.6GHz) only.

Figure 4.3.4 and Figure 4.3.5 show comparisons between measured and simulated phase versus input power for the CFY30 transistor.

Figure 4.3.4 shows the phase for the transistor, biased in class AB mode with a quiescent gate voltage of V_{GS} = -1.1V, which is relatively flat with variation of less than 5° in both the measured and simulated results. This figure shows an excellent comparison between the simulated and measured phase, with a maximum difference of 3° between them.

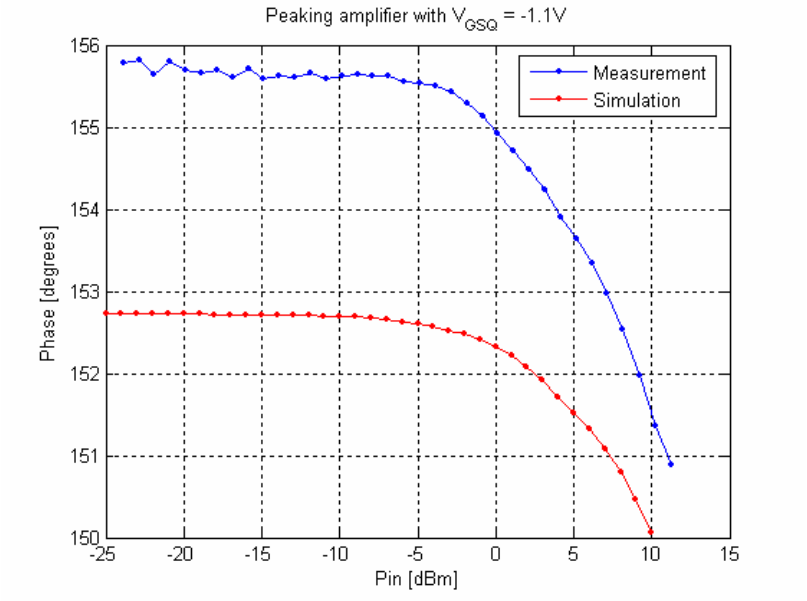


Figure 4.3.4 Comparison of measured and simulated phase of CFY30 transistor with a gate voltage of V_{GS} = -1.1V.

Figure 4.3.5 shows the phase for the transistor biased in class C mode with a quiescent gate voltage of V_{GS} = -1.7V. This figure shows a phase response which varies approximately 50° for both the measured and simulated results. Once again, the simulated phase compares very well with the measured phase, with a maximum difference of 7°.

It can therefore be concluded that the prediction of phase response versus input power using the small-signal parameters at an equivalent gate voltage, is accurate and useful during the first stages of designing a Doherty amplifier.

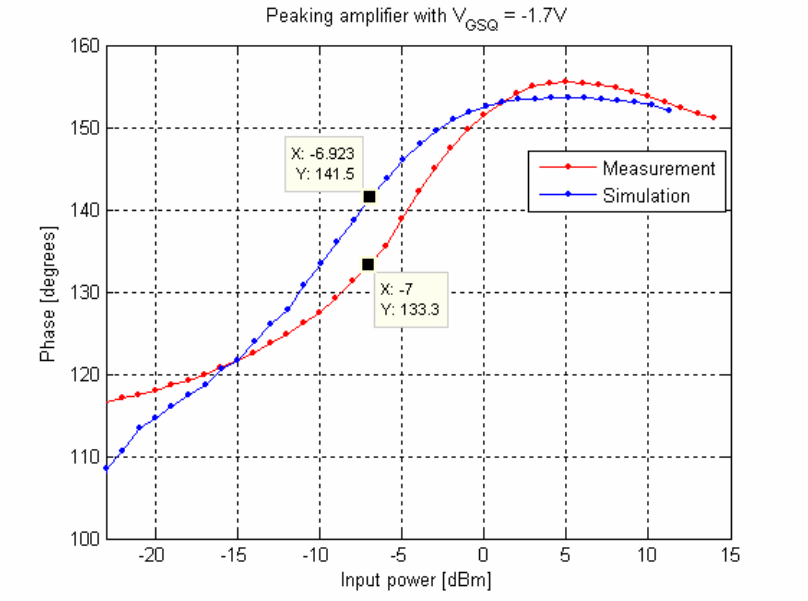


Figure 4.3.5 Comparison of measured and simulated phase of CFY30 transistor with a gate voltage of V_{GS} = -1.7V.

Figure 4.3.6 and Figure 4.3.7 show measurements made of the peaking amplifier and Doherty amplifier made utilising the non-linear network analyser and the custom setup described in Section 4.3.1. To verify the custom setup's validity, comparisons are made of output versus input power and DC drain current versus input power. The measurements of the peaking amplifier are shown in Figure 4.3.6. The peaking amplifier is biased with a gate voltage of V_{GS} = -1.9V. The peaking amplifier in the Doherty configuration, of which measurements are shown in Figure 4.3.7, is also biased with a gate voltage of V_{GSP} = -1.9V and the carrier amplifier with a gate voltage of V_{GSC} = -1.1V. The differences between the two measurement methods are small, with a maximum difference of respectively 1.4 dBm and 1 mA.

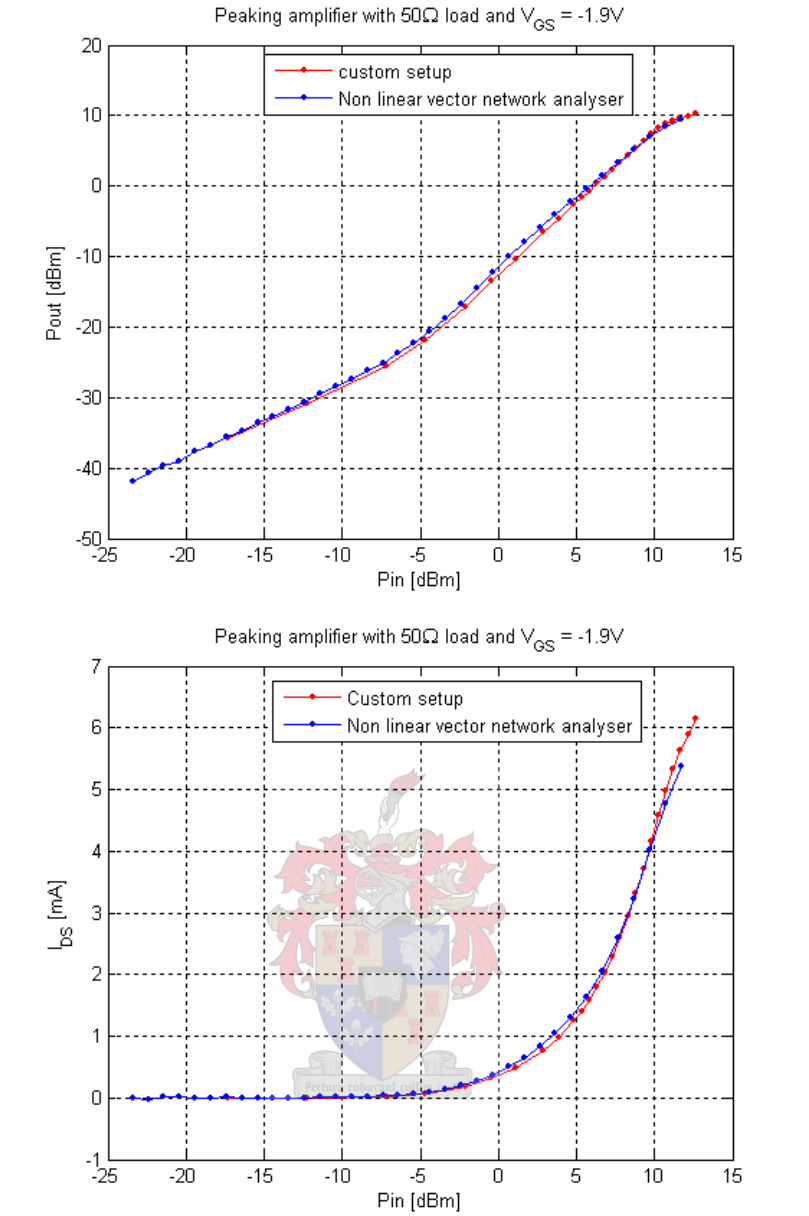


Figure 4.3.6 Comparison between measurements made with the non-linear network analyser and the custom setup on the peaking amplifier with a 50Ω load and a quiescent gate voltage of V_{GS} = -1.9V in terms of output power versus input power and DC drain current versus input power.

Excellent comparisons between measurements made on a non-linear network analyser and the custom setup and calibration explained in 4.3.1, is proof that the custom setup is reliable and accurate.

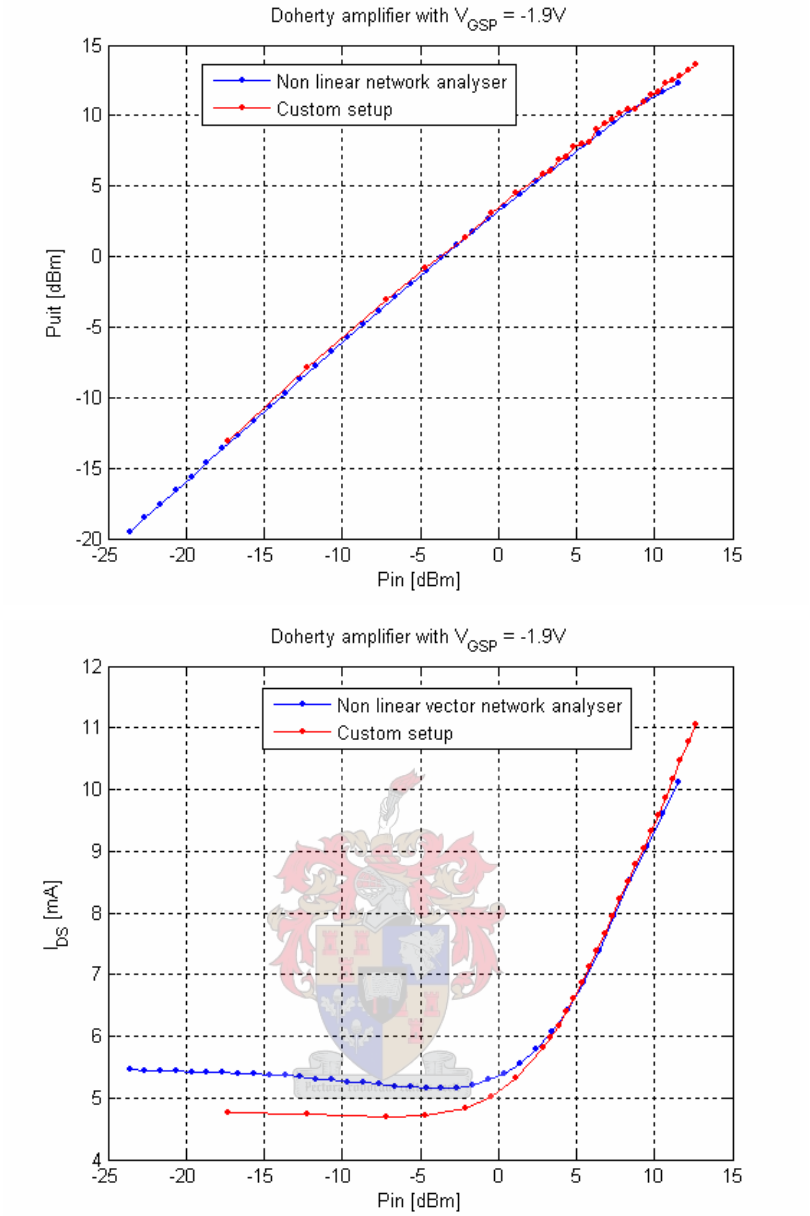


Figure 4.3.7 **Comparison between measurements made with the non-linear network analyser and the custom setup on the Doherty amplifier with a peaking amplifier gate voltage of V_{GSP} = -1.9V and carrier amplifier gate voltage of V_{GSC} = -1.1 V, in terms of output power versus input power and DC drain current versus input power.**

4.4 Measurement Results

4.4.1 Carrier Amplifier

The purpose of first designing a Doherty amplifier using the small-signal CFY30 FET transistor is twofold. On the one hand, greater insight is gained regarding the design of a Doherty amplifier and on the other hand, it must be established that the proposed design procedure is viable. As explained

in Section 4.2.6, the carrier and peaking amplifiers, as well as the power divider and power combiner are manufactured separately. This is done so that the carrier and peaking amplifiers can be measured either separately, or in a Doherty configuration. In addition to the power combiner, three different load conversions are made to present the amplifiers with either a 25 Ω, 35 Ω or 50 Ω load. In addition to the power divider, separate input lines are made for both the carrier and peaking amplifiers.

Even though the large-signal operation of the amplifiers is of greater importance, the small-signal simulations have to be verified with small-signal measurements to identify any possible manufacturing errors as soon as possible. Figure 4.4.1 shows S_{11} for the carrier amplifier as simulated in Microwave Office and the measured S_{11}. A first observation is that the simulated point of resonance shifts to 1.632 GHz, whilst in Figure 4.2.11 it is at 1.6 GHz. This shift is due to the extra input and output lines that are added to permit the measurement of the carrier amplifier on its own.

The simulated and measured resonance frequency in Figure 4.4.1 differs with 52 MHz. For a first iteration, this is a good comparison. The comparison between the simulation and measurement of S_{21} shows similar results.

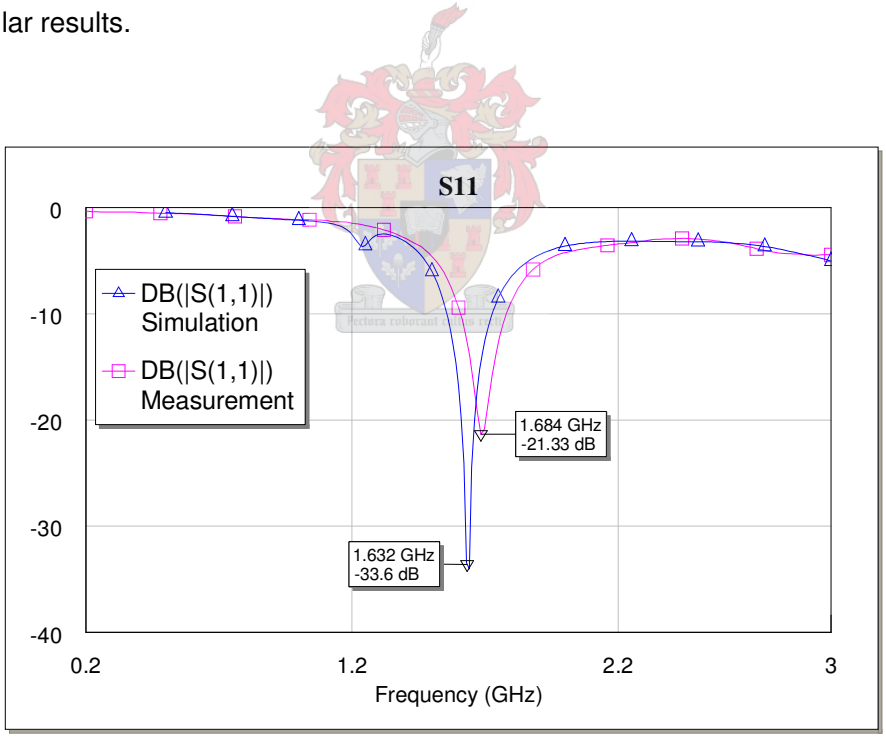


Figure 4.4.1 Simulated (Δ) and measured (□) S_{11} of the carrier amplifier.

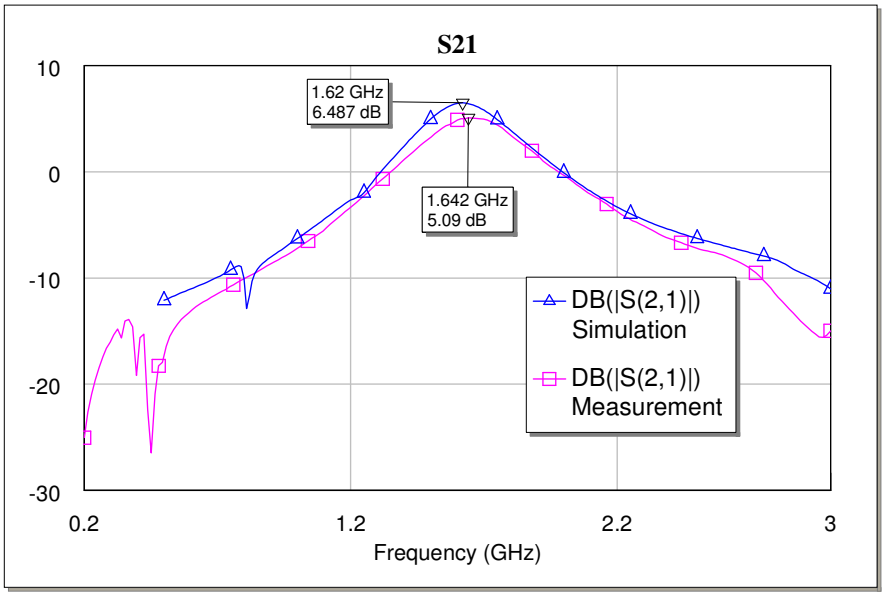


Figure 4.4.2 Simulated (Δ) and measured (□) S_{21} of the carrier amplifier.

Before measurements of the carrier amplifier with the different loads are shown, the expected behaviour will be discussed at the hand of the CFY30's measured IV-curves and the designed load-lines shown in Figure 4.4.3.

According to the explanation in Section 3.3, if the carrier amplifier sees a load of $0.5R_o$ during low power operation, the transistor's internal current source is presented with an impedance of $2R_{optC.}$ During high power operation the carrier amplifier should see R_o and the internal current source R_{optC}.

In Section 4.2.1 and 4.2.2 R_{optC} and R_o are defined as R_{optC} = 90.9 Ω and R_o = 50 Ω respectively. Simulation predicts that the impedance presented to the internal current source will change from 168.5 + j0.2 Ω to 86.8 – j6.2 Ω. The steeper of the two load-lines in Figure 4.4.3 represents the impedance of 86.8 + j6.2 Ω due to the 50 Ω load, while the other load-line represents the impedance 168.5 + j0.2 Ω due to the 25 Ω load. The bias point of V_{DSQ} = 2.8V, V_{GSQ} = -1.1V and a quiescent current of I_{DSQ} = 5.3 mA are also indicated. On the right hand side, two input voltage signals are shown. The larger of these represents the maximum input voltage signal and the smaller one half of the maximum input voltage, which constitutes the 6dB drop in input power.

Looking at Figure 4.4.3, it is apparent that the output voltage and current of the carrier amplifier with a 25 Ω load will be affected by the knee voltage at a lower input voltage than they will in the case of a 50 Ω load. It can thus be expected that the carrier amplifier with a 25 Ω load will go into compression at a lower input power than it will with a 50 Ω load. The carrier amplifier with a 25 Ω

load should, however, have a larger small-signal gain, since it permits a greater output voltage swing than it will with the 50 Ω load. The measurements in Figure 4.4.4 and Figure 4.4.5 confirm this.

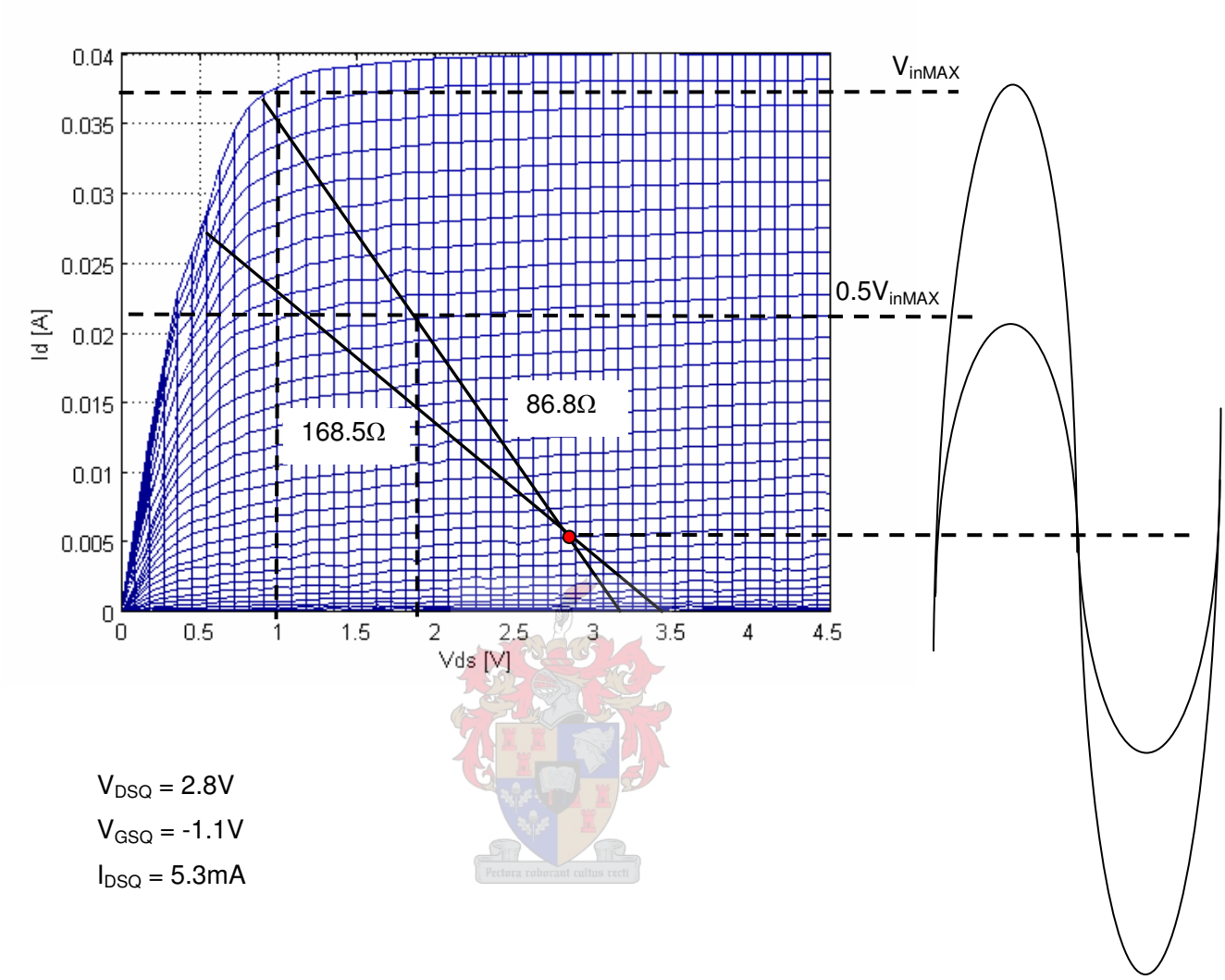


Figure 4.4.3 Measured IV-curve of the CFY30 transistor with the two designed load-lines. The steep load-line represents a resistance of 86.8Ω seen by the transistors current source and the other a resistance of 168.5Ω.

Figure 4.4.4 shows the measured compression for the carrier amplifier with the three different loads. The carrier amplifier with a 25 Ω load reaches its 1 dB compression point at an input power of 0.6 dBm less than with a 50 Ω load, and its 2 dB compression point at an input power of 2.3 dBm less than with a 50 Ω load. The carrier amplifier with a 25 Ω load also has a measured small-signal gain of 6.7 dB, which is 0.9 dB more than with a 50 Ω load.

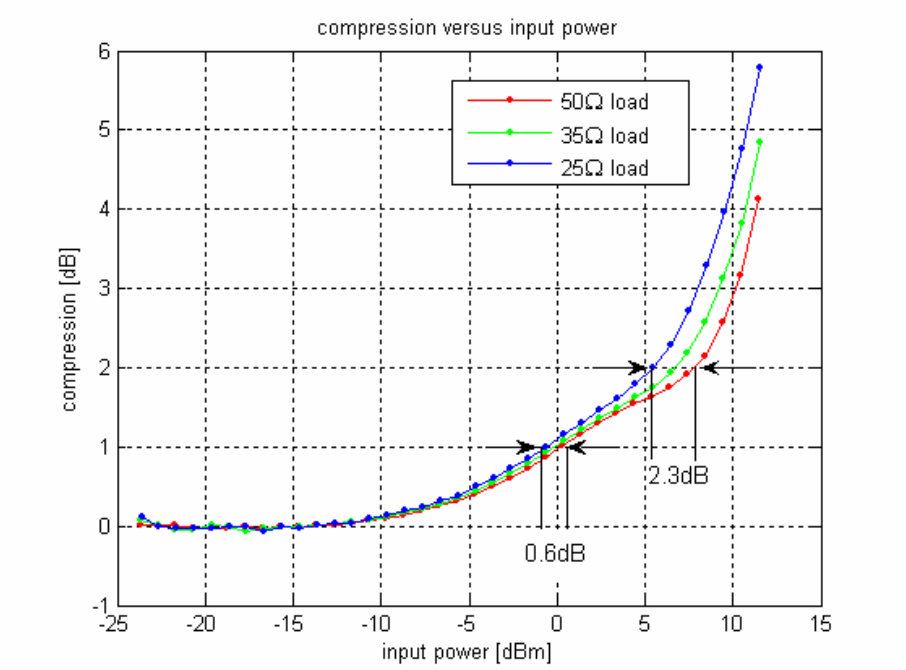


Figure 4.4.4 Compression versus input power for the carrier amplifier with a 25, 35 and 50Ω load.

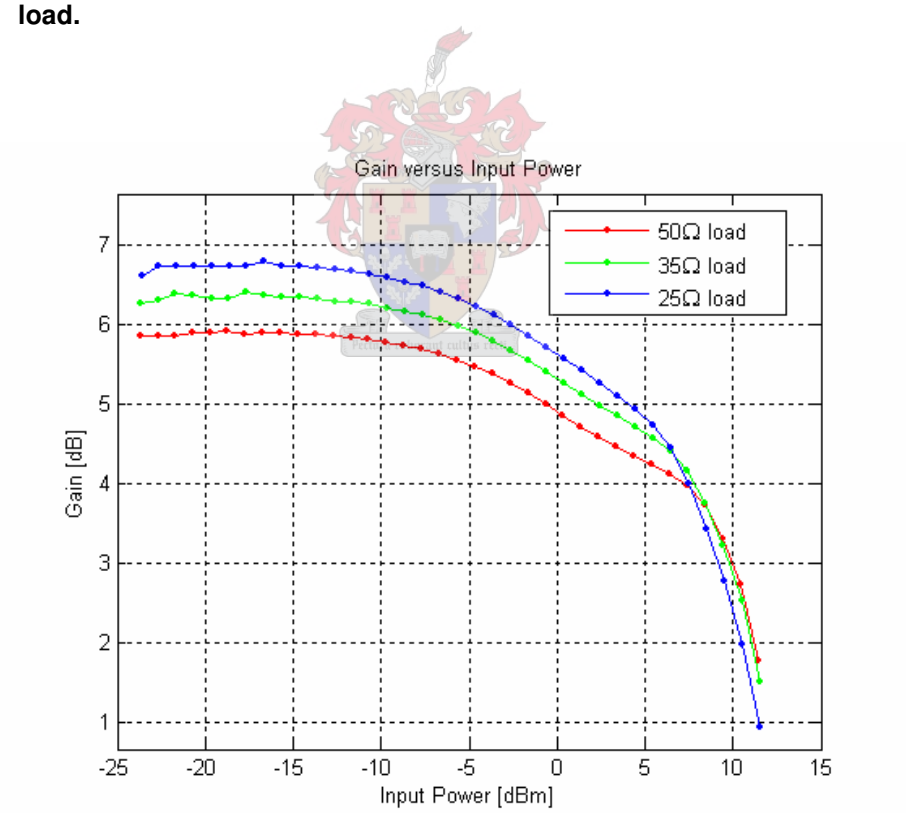


Figure 4.4.5 Gain versus input power for the carrier amplifier with a 25, 35 and 50Ω load.

Since the carrier amplifier is biased in class AB mode, the DC current at the drain will begin to increase when the drain current, i_{ds}, starts to clip on the negative cycle. The DC component for the carrier amplifier with a 50 Ω load will be larger than with a 25 Ω load, because the drain current will start clipping on the positive cycle at a lower input power with a 25 Ω load. Figure 4.4.6, which shows

the measured DC current for the carrier amplifier with all three loads, verifies this. At low input power, the DC current is the same for the carrier amplifier for every load. However, when the DC current starts to increase, it is larger with a 50 Ω load.

Looking at Figure 4.4.3, the carrier amplifier with a 25 Ω load and an input signal of half the maximum input voltage signal, should have the same drain efficiency as it would have with a 50 Ω load and the maximum input signal[3]. This means that, at the maximum input voltage, the carrier amplifier with a 50 Ω load should be at its most efficient and it should have the same drain efficiency with a 25 Ω load at 6 dBm less input power. Figure 4.4.7 shows the drain efficiency of the carrier amplifier for the three different loads. It is clear from the figure that a particular drain efficiency can be achieved by the carrier amplifier with both a 25 Ω and a 50 Ω load, but that the input power will always be lower in the case of the 25 Ω load. The maximum difference measured is 3 dBm and not the expected 6 dBm.

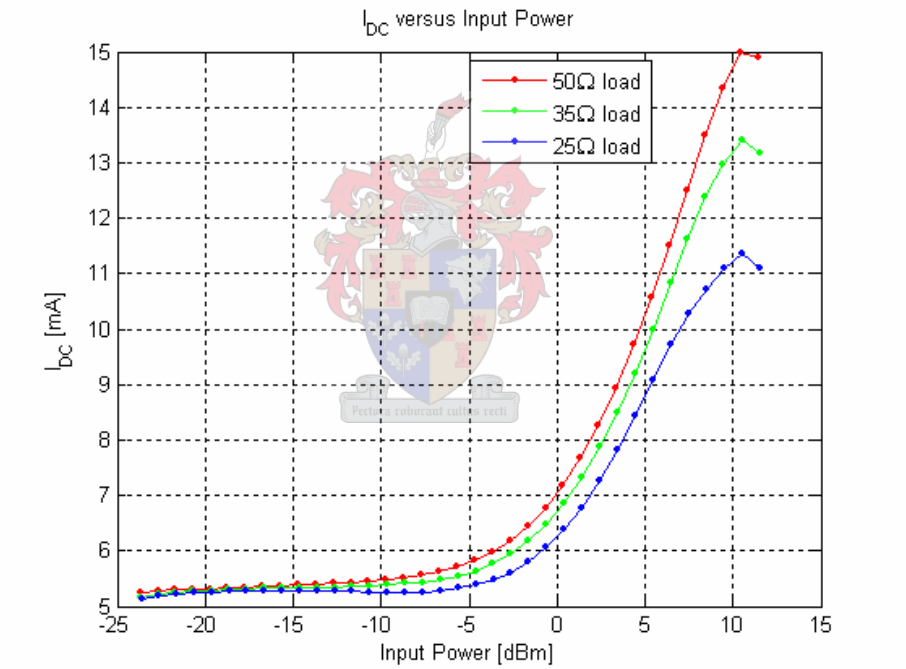


Figure 4.4.6 DC component of the drain current, i_{ds}, versus input power for the carrier amplifier with a 25, 35 and 50Ω load.

[3] This is a brief repetition of the discussion in Section 3.2.1.

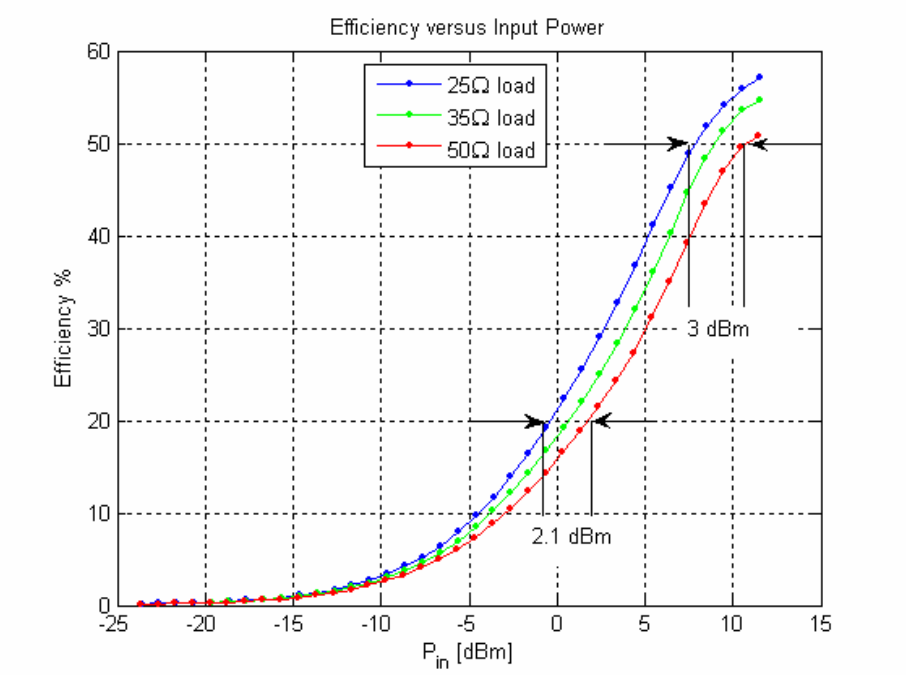


Figure 4.4.7 Drain efficiency versus input power for the carrier amplifier with a 25, 35 and 50Ω load.

In Section 4.2.1 the gate voltage for the carrier amplifier is defined as V_{GSC} = -1.1V. Looking at the measured IV-curves of the CFY30 transistor (see Figure 2.3.2, Figure 2.3.3 and Figure 4.4.3), a maximum input voltage amplitude of 1.1V seems achievable. Stated differently, if the load-line corresponding to the 50 Ω load is used, it seems that compression will be reached at an input voltage amplitude of 1.1V. Since the amplifier's input is matched to a 50 Ω system, a sinusoidal signal with a voltage amplitude of 1.1V into a 50 Ω load relates to 10.83 dBm.

Looking at Figure 4.4.4, the carrier amplifier is at its 1dB compression point at an input power of approximately 0 dBm with any of the three loads. At an input power of 10.8 dBm the compression for the amplifier with a 25 Ω load is already 5.1 dB and with a 50 Ω load it is 3.5 dB. The reason for this early compression is the clipping of the output current on the negative cycle when the input signal's voltage amplitude is about 0.25V or -2 dBm. The compression starts to increase even more when the output current starts clipping on the positive cycle as well. As previously explained, this occurs at a lower input power for the carrier amplifier with a 25 Ω load than it would with a 50 Ω load. This also explains why the 1 dB compression point for all three of the loads are relatively close together, since clipping of the output current on the negative cycle happens at the same input power for all three of the loads.

As previously stated, a particular drain efficiency can be achieved by the carrier amplifier with both a 25 Ω and a 50 Ω load, but the input power will always be lower in the case of the 25 Ω load (see Figure 4.4.7). However, the maximum difference measured is 3 dBm and not the expected 6 dBm. A

possible explanation for this is the fact that the internal current source is not presented with 90.9 Ω and 181.8 Ω as designed for the 50 Ω and 25 Ω loads respectively, but instead sees 86.8 Ω and 168.5 Ω. This causes steeper load-lines than those that were designed for. The knee voltage is also not a constant as is assumed in Section 2.3.1 during the design of R_{optC} for the two load-lines shown in Figure 4.4.3. Instead, the knee voltage looks more like a curved line through the transistor's IV-curve, as shown in Figure 4.4.8. This means that the desired impedance for the load-line due to the 25 Ω load should be more than $2R_{optC}$.

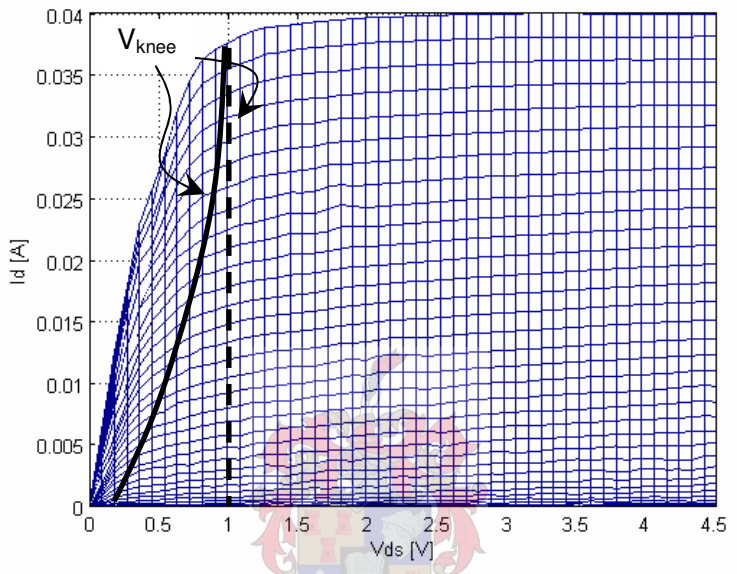


Figure 4.4.8 CFY30 transistor's IV-curve with the knee voltage as a constant (– –) and as a function of gate voltage (—).

These measurements will serve as a reference to determine to what extent the Doherty configuration is successful, since the load of the Doherty carrier amplifier is dynamically modulated from 25 Ω to 50 Ω, according to theory.

4.4.2 Peaking amplifier

Figure 4.4.9 shows the simulation and measurement results of S_{11} for the peaking amplifier on its own. The simulation's resonant point, however, is not at 1.6 GHz, due to a few factors. First of all, the design is done at the expected PEP and this figure shows results for small-signal operation. Secondly, extra input and output lines are added to enable measurement of the peaking amplifier on its own. These additional lines will contribute a small offset if they are not exactly 50 Ω. The measurement shows a good input match of -33 dB and has a phase shift of 54 MHz compared to the simulation.

The simulation and measurement data of S_{21} in Figure 4.4.10 compare just as well. The frequency where the maximum gain occurs differs with 50 MHz.

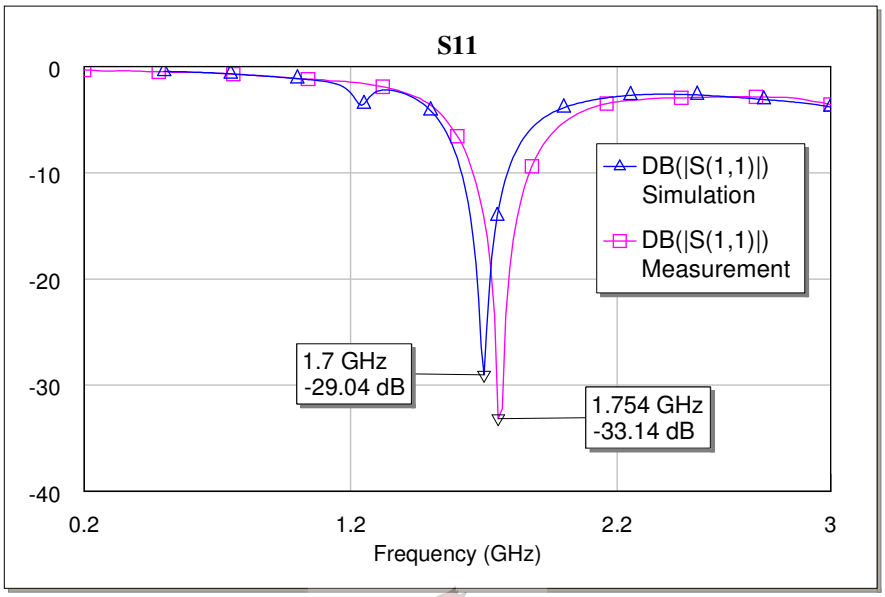


Figure 4.4.9 Simulated (Δ) and measured (□) S_{11} of the peaking amplifier.

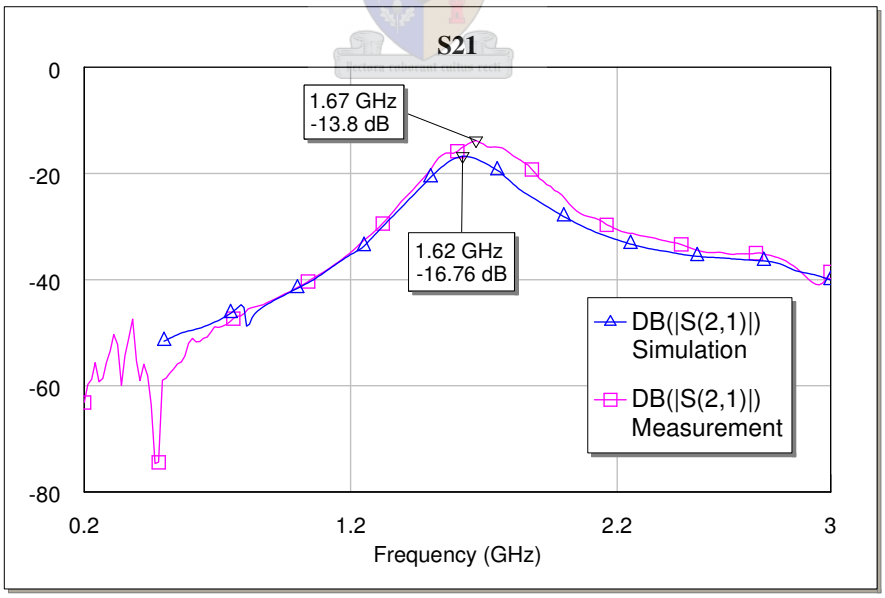


Figure 4.4.10 Simulated (Δ) and measured (□) S_{21} of the peaking amplifier.

4.4.3 Balanced Class AB amplifier

As explained in Section 4.2.6, the balanced class AB amplifier simply consists of two carrier amplifiers in parallel, joined together with two 90° hybrids at both the input and output. The purpose of the balanced class AB amplifier is to have a benchmark against which the Doherty amplifier's performance can be compared.

Figure 4.4.11 shows the small-signal simulation of S_{11} for the balanced amplifier together with the measured S_{11}. The simulation compares extremely well with the measurement – both having a reflection coefficient below -20 dB at the centre frequency of 1.6 GHz. Figure 4.4.12 shows the simulation and measurement of the balanced amplifier's S_{21}. Once again, the comparison between simulation and measurement data is excellent, with both showing a gain of 6.26 dB at the centre frequency and a similar response over the rest of the frequency band.

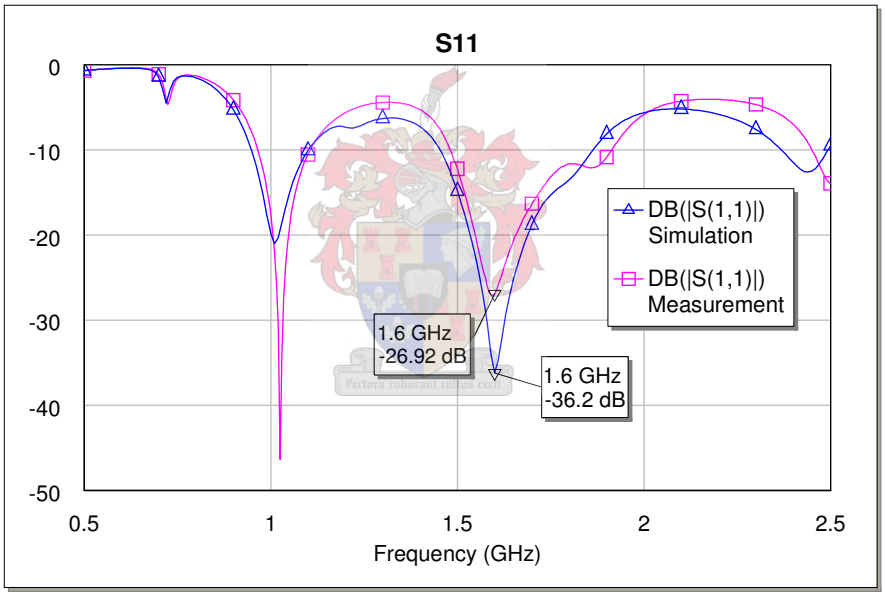


Figure 4.4.11 Small-signal simulation (Δ) and measurement (□) of S_{11} for the balanced amplifier.

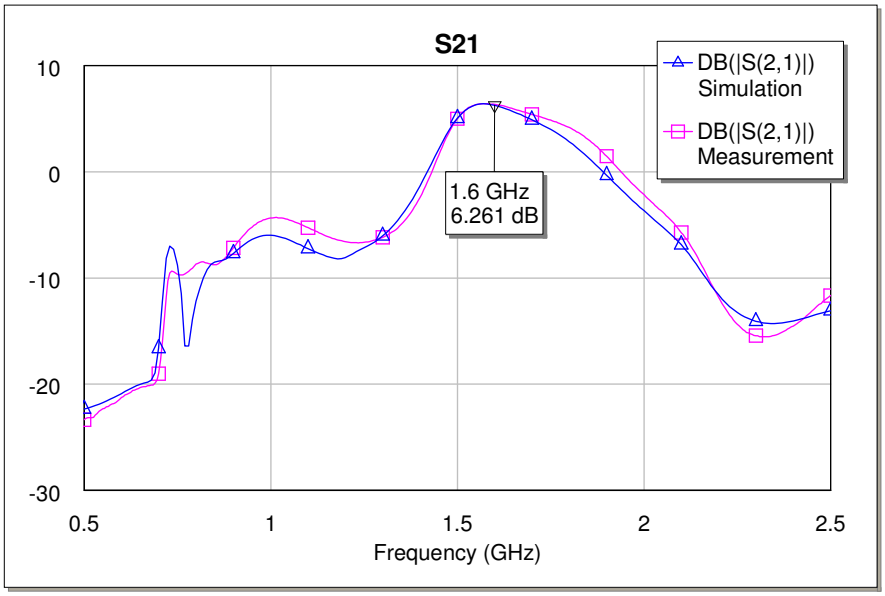


Figure 4.4.12 Small-signal simulation (Δ) and measurement (□) of S_{21} for the balanced amplifier.

Since both the amplifiers in the balanced configuration see a 50 Ω load, its measurements will also be compared against measurements of the carrier amplifier with a 50 Ω load. The balanced amplifier and carrier amplifier should have the same gain. The input power of the balanced amplifier is split evenly with the 90° hybrid power divider. Therefore, its 1 dB compression point should be at an input power of 3 dBm more than the single carrier amplifier.

Figure 4.4.13 shows the measured gain for the balanced and carrier amplifiers. With a difference in the small-signal gain of only 0.7 dB, their gain is essentially the same. The difference is probably due to manufacturing imperfections in the transistors and circuit, while a slight difference in biasing voltages can also influence the gain.

Figure 4.4.14 shows the compression for the balanced and carrier amplifier. It can be seen that the difference in input power is approximately 3 dBm over the input range from where compression starts.

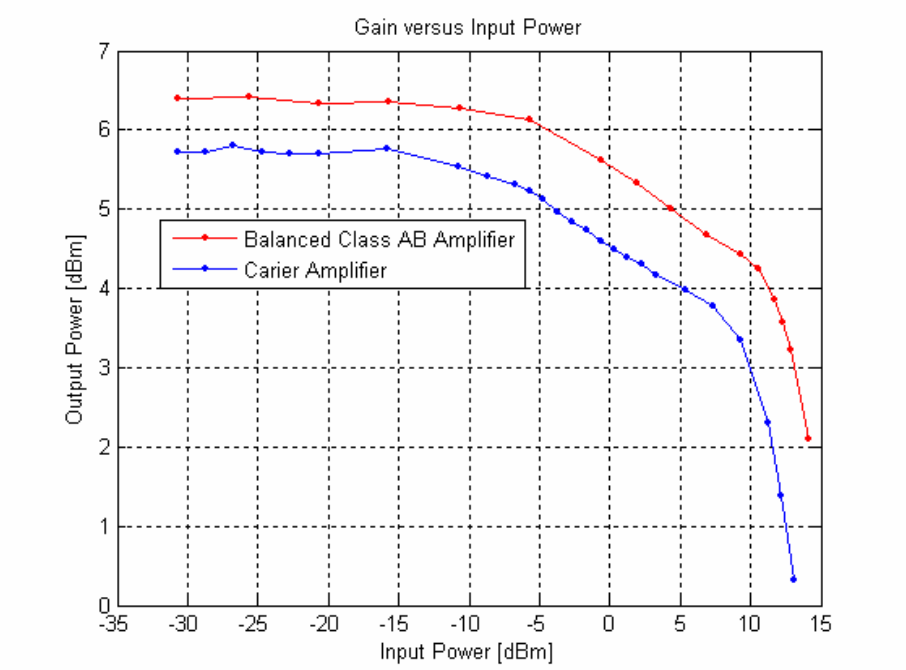


Figure 4.4.13 Measured gain for the balanced amplifier and carrier amplifier.

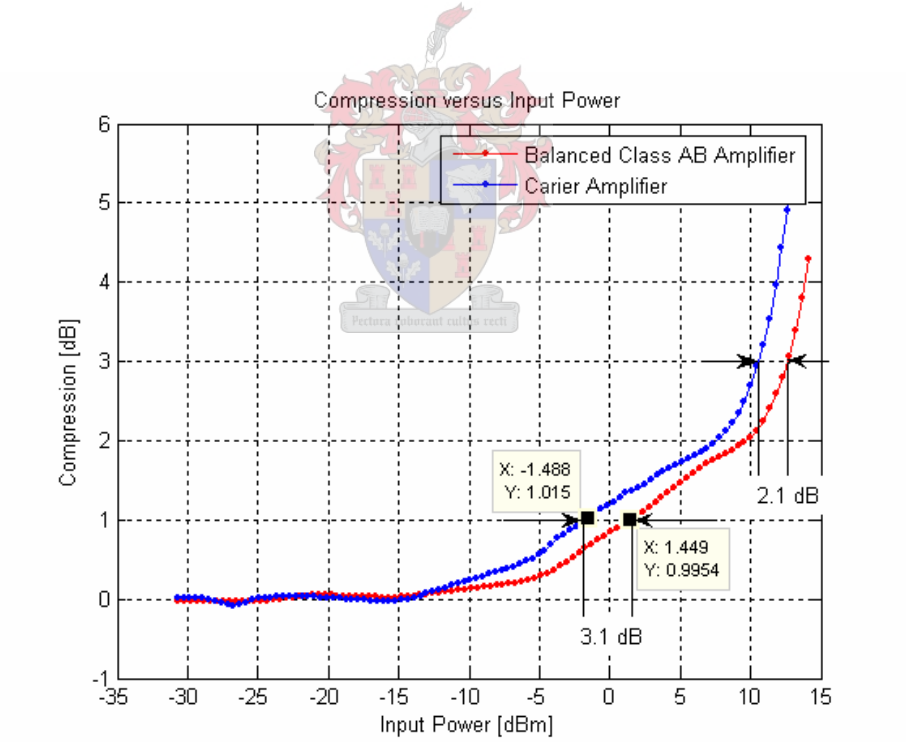


Figure 4.4.14 Measured compression for the balanced and carrier amplifier.

4.4.4 Doherty Configuration

In Section 4.2.1 the drain bias voltage is defined as V_{DS} = 2.8 V for both the carrier and peaking amplifiers, while their respective gate voltages are V_{GSC} = -1.1 V and V_{GSP} = -1.9 V. The

measurements of the Doherty configuration are, however, done at various peaking amplifier gate voltages to determine the best performance levels. The gate voltages used will be clearly indicated for every measurement shown.

The performance, especially the gain, compression, drain efficiency and power added efficiency (PAE) of the Doherty amplifier will be compared to the balanced class AB amplifier. The balanced class AB amplifier has the same quiescent bias point as the Doherty carrier amplifier.

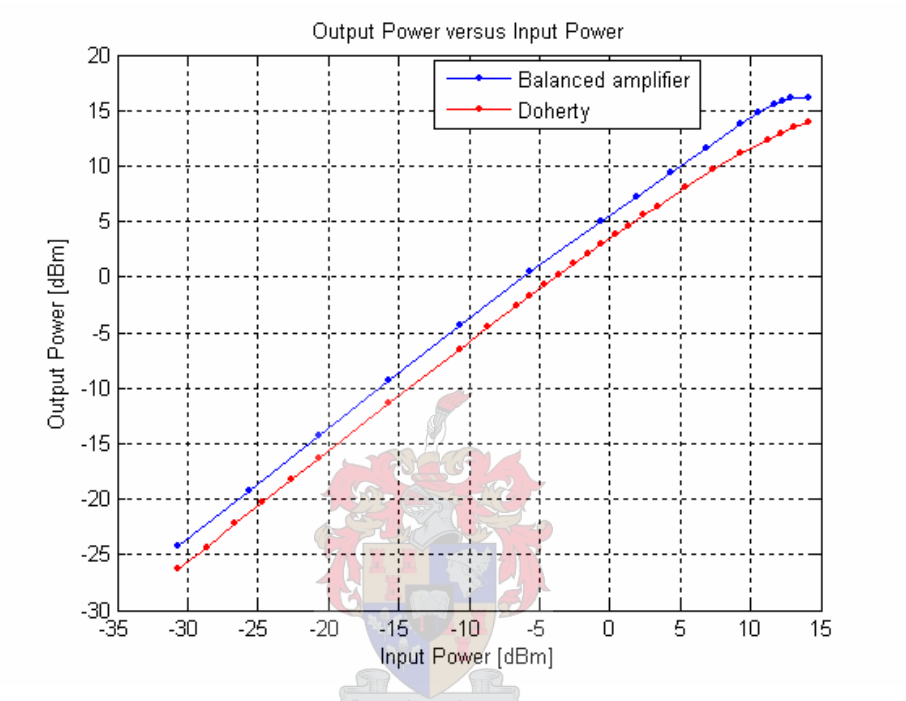


Figure 4.4.15 Measured output power versus input power for the balanced amplifier and Doherty amplifier with V_{GSC} = -1.1 V and V_{GSP} = -1.9 V.

Figure 4.4.15, Figure 4.4.16 and Figure 4.4.17 shows the measured output power, gain and compression for the balanced and Doherty amplifier with V_{GSP} = -1.9 V. The Doherty amplifier has 2.1 dB less gain than the balanced amplifier, due to the fact that the peaking amplifier is biased in class C mode. There is no significant difference in the two amplifiers' 1 dB compression point at approximately 1 dBm input power. According to the ideal theory, the peaking amplifier's increasing fundamental current component modulates the load of the carrier amplifier, which keeps the carrier amplifier's voltage in saturation. The load which the carrier amplifier sees is designed to dynamically increase from 25 Ω during low power operation, to 50 Ω during high power operation or PEP. As the 1 dB compression point is a common figure of merit it will also be taken as the point of PEP. Figure 4.4.18 shows the DC component of the drain current of the balanced and Doherty amplifiers. There are two traces shown for the balanced amplifier, since it consists of two amplifiers in parallel. Even though this does not show the fundamental current component, if the carrier amplifier's load was fully modulated to 50 Ω it should have the same DC current as the two class AB amplifiers making

up the balanced class AB amplifier at PEP. Comparing the DC current of the carrier amplifier with the balanced amplifier at the 1 dB compression point of 1 dBm input power, it is apparent that the peaking amplifier is just beginning to conduct. Therefore, there can be no significant load modulation.

Figure 4.4.19 shows the drain efficiency versus input power for the balanced and Doherty amplifier with V_{GSP} = -1.9 V. At the 1 dB compression point, the Doherty amplifier has a drain efficiency that is 3.7% greater than the balanced amplifier's drain efficiency. In literature it is common practice to plot the drain efficiency against output power or backed-off output power.

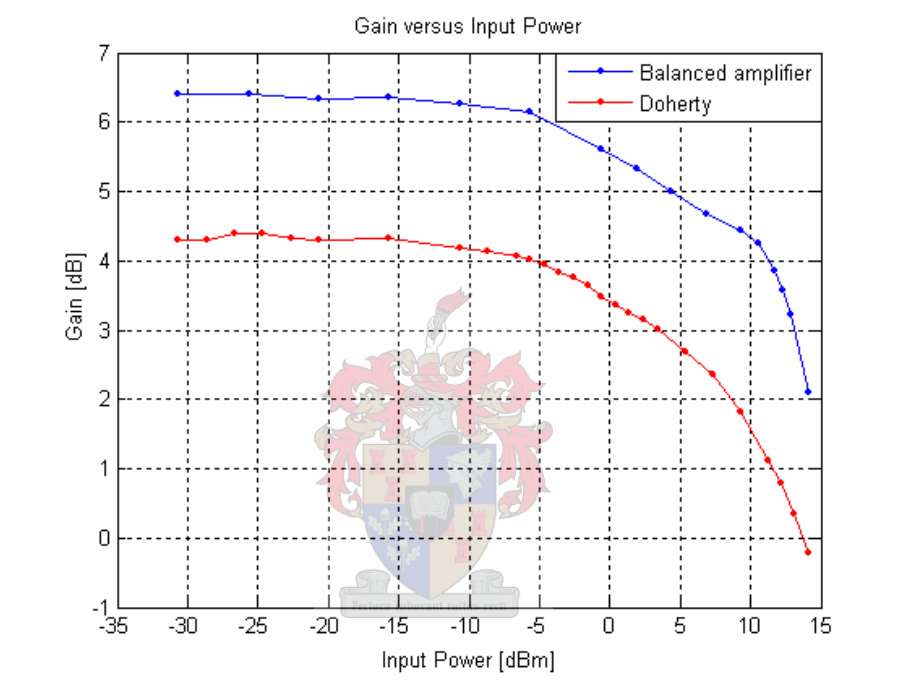


Figure 4.4.16 Measured gain for the balanced and Doherty amplifier with V_{GSP} = -1.9 V.

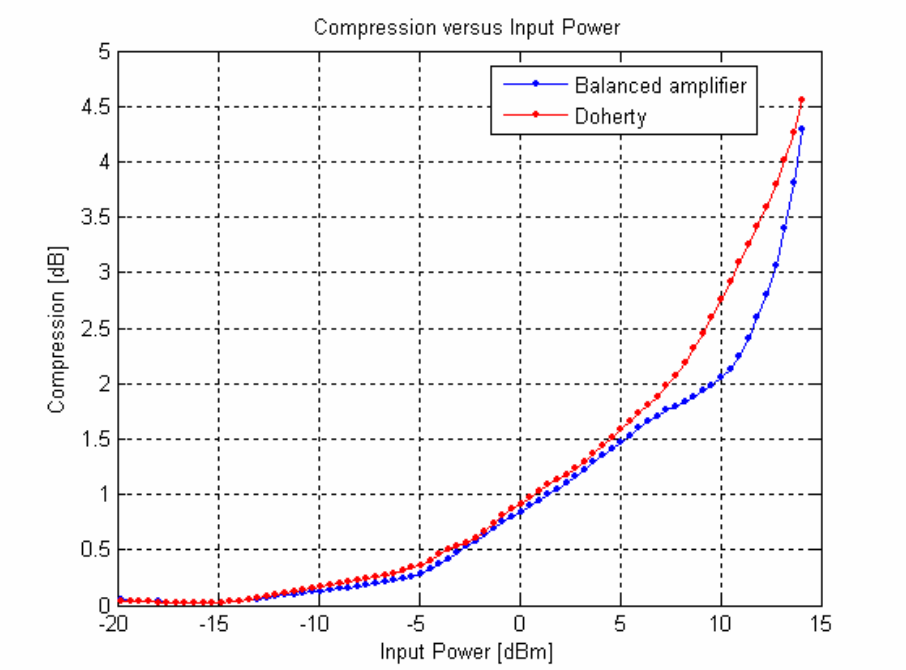


Figure 4.4.17 Measured compression versus input power for the balanced amplifier and Doherty amplifier with V_{GSP} = -1.9 V.

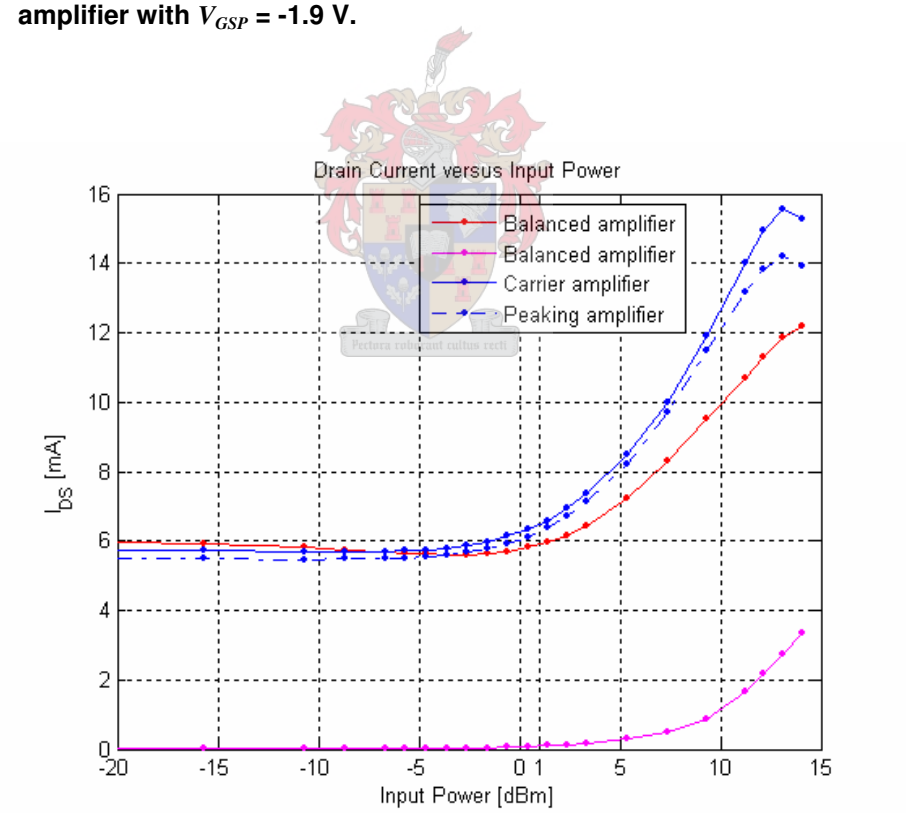


Figure 4.4.18 Measured drain current for the balanced amplifier and Doherty amplifier with peaking amplifier gate voltage, V_{GSP} = -1.9 V.

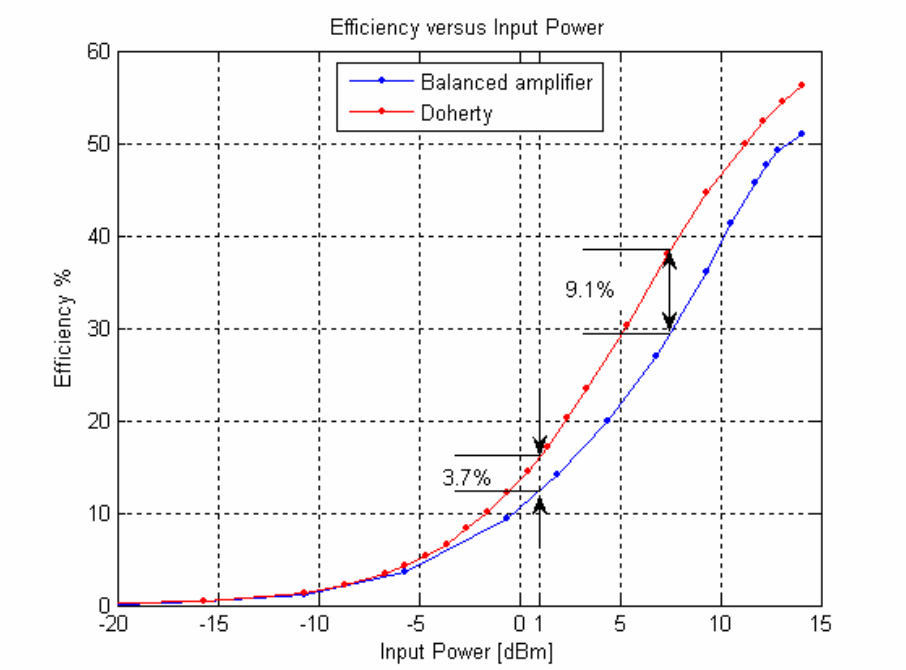


Figure 4.4.19 Measured drain efficiency versus input power for the balanced amplifier and Doherty amplifier with V_{GSP} = -1.9 V.

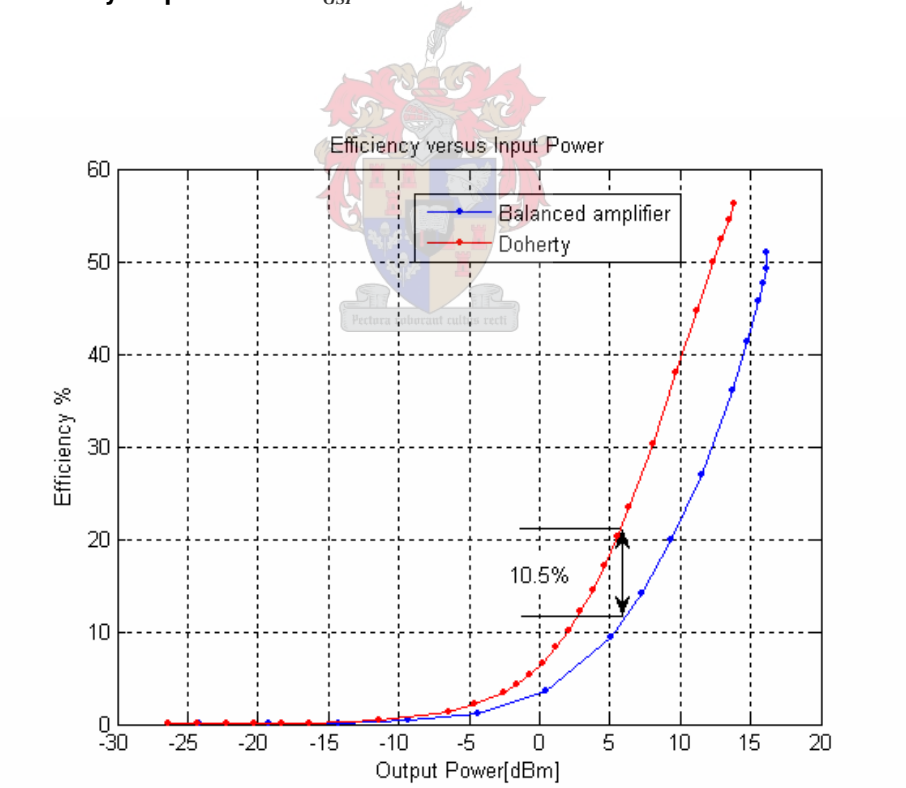


Figure 4.4.20 Measured drain efficiency versus output power for the balanced amplifier and Doherty amplifier with V_{GSP} = -1.9 V.

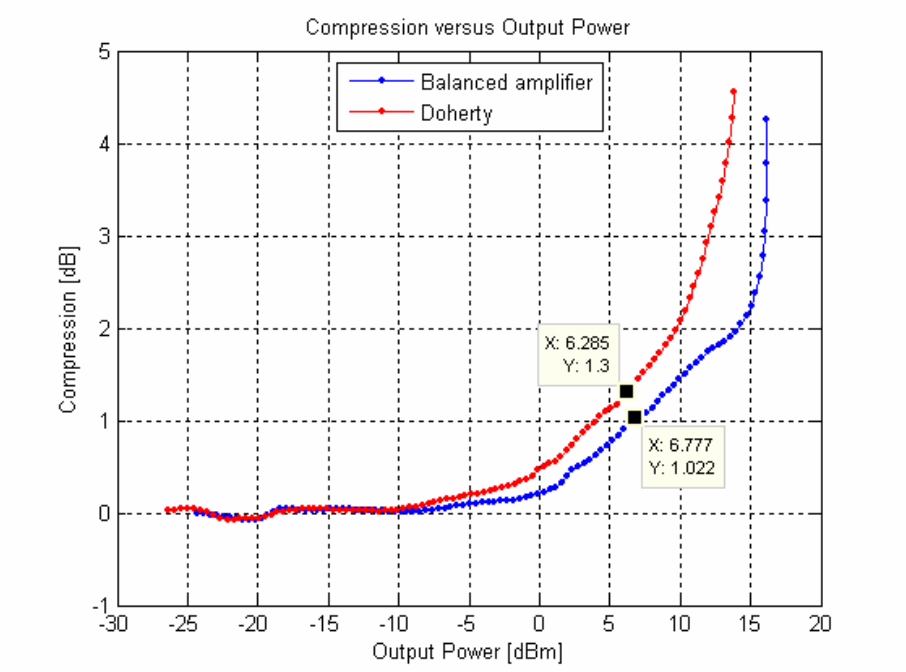


Figure 4.4.21 Measured compression versus output power for the balanced amplifier and Doherty amplifier with V_{GSP} = -1.9 V.

The drawback of plotting the drain efficiency against output power, especially when comparing two or more amplifiers' efficiencies on one graph, is that the effect of different gains and 1 dB compression points is lost. To illustrate this, Figure 4.4.20 shows the drain efficiency versus output power for the balanced and Doherty amplifier with V_{GSP} = -1.9 V. With both amplifiers' 1 dB compression point at approximately 1 dBm input power and gains of 6.4 and 4.3 dB respectively, their efficiencies are compared at 6 dBm output power (see Figure 4.4.20), which gives a difference of 10.5%. However, if their compression curves are plotted against output power, as shown in Figure 4.4.21, it can be noted that at 6 dBm output power, the Doherty amplifier is already at 1.3 dB compression. When plotting the efficiencies versus backed-off output power, the X-axis is normalised to each amplifier's output power at its 1 dB compression point. As shown in Figure 4.4.22[4], the difference in drain efficiency is now just 4.2%.

[4] 0 dB on the X-axis represents the peak output power for each amplifier.

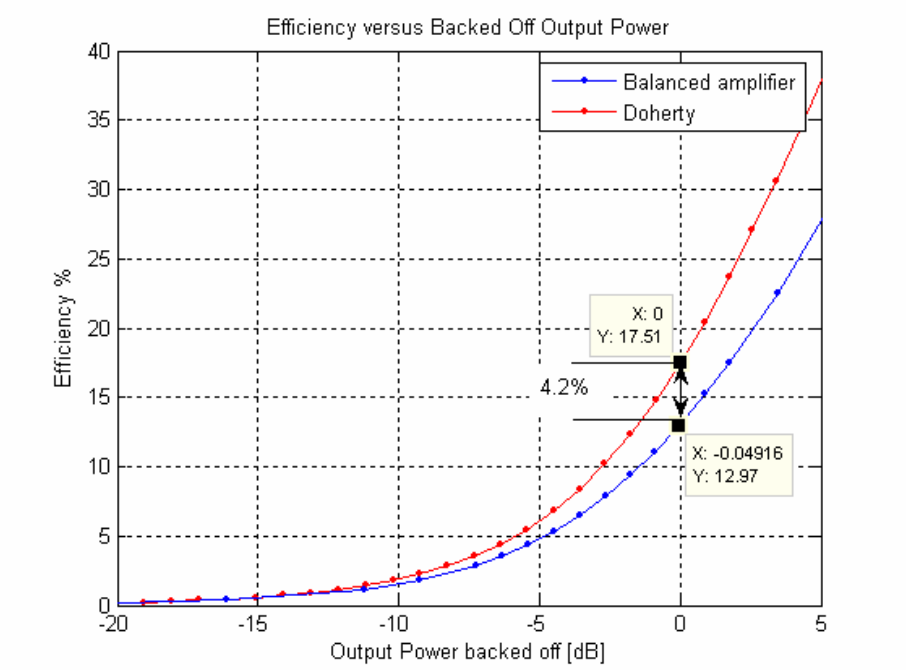


Figure 4.4.22 Measured drain efficiency versus backed-off output power for the balanced amplifier and Doherty amplifier with peaking amplifier gate voltage, V_{GSP} = -1.9 V.

By raising the peaking amplifier's gate voltage to V_{GSP} = -1.7 V, it will start conducting at a lower input power, thus generating a higher fundamental current component at PEP and in turn modulating the carrier amplifier's load closer to the designed 50 Ω. Figure 4.4.23 shows the DC component of the drain current for the balanced and Doherty amplifier with V_{GSP} = -1.7 V. It is evident that the peaking amplifier's conduction begins at a much lower input power than in Figure 4.4.18. Figure 4.4.24 shows the compression for the balanced and Doherty amplifier with V_{GSP} = -1.9V and V_{GSP} = -1.7V. The input power for the Doherty amplifier's 1 dB compression point shifts to approximately 2 dBm with V_{GSP} = -1.7V. The carrier amplifier's DC current component at 2 dBm input power in Figure 4.4.23 shows no significant change from that in Figure 4.4.18 at 1 dBm input power. It is, however, difficult to comment on the fundamental current component at this relatively low input power. What may be said, is that load modulation does occur to a greater extent with the peaking amplifier biased at V_{GSP} = -1.7V than at V_{GSP} = -1.9V, at higher input power. The load modulation can be seen in the carrier amplifier's DC current component, which reaches a higher level in Figure 4.4.23 than in Figure 4.4.18. The other proof is in the compression curves. Although there was not a significant change in the input power at the Doherty amplifier's 1 dB compression point, the compression curve did undergo a shift and the 2 dB and 3 dB compression points now occur at a few dBm higher input power, as shown in Figure 4.4.24. In Section 4.4.1, the same effects were observed by physically changing the carrier amplifier's load.

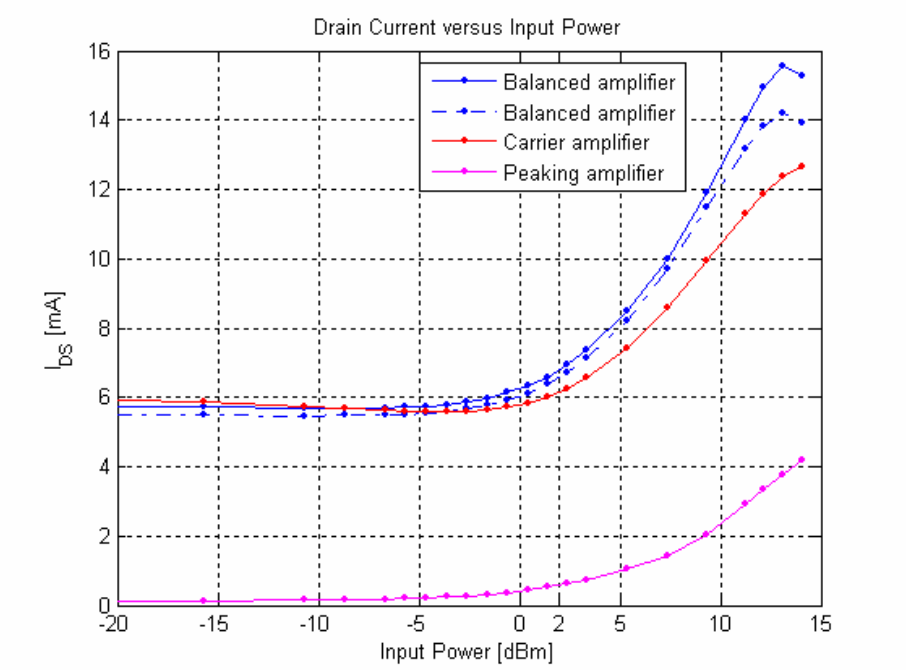


Figure 4.4.23 Measured drain currents for the balanced amplifier and Doherty amplifier with peaking amplifier gate voltage, V_{GSP} = -1.7 V.

Figure 4.4.25 shows the measured gain for the balanced and Doherty amplifier with V_{GSP} = -1.7V and V_{GSP} = -1.9V. The gain for the Doherty amplifier with the two different peaking amplifier gate voltages is the same up to approximately 0 dBm input power. From 0 dBm upwards, the Doherty configuration with V_{GSP} = -1.7V shows a slower gain compression than with V_{GSP} = -1.9V. In Figure 4.4.23 – which shows the DC current component for the Doherty amplifier with V_{GSP} = -1.7V – the peaking amplifier starts to conduct just before 0 dBm. The slower compression rate in the Doherty amplifier's gain from 0 dBm upwards can thus be attributed to the peaking amplifier, which starts to contribute to the Doherty amplifier's overall gain.

By increasing the peaking amplifier's gate voltage from V_{GSP} = -1.9V to V_{GSP} = -1.7V, the drain efficiency of the Doherty amplifier at its 1 dB compression point increases with another 2.4% and is 6.6% more efficient than the balanced class AB amplifier, as shown in Figure 4.4.26.

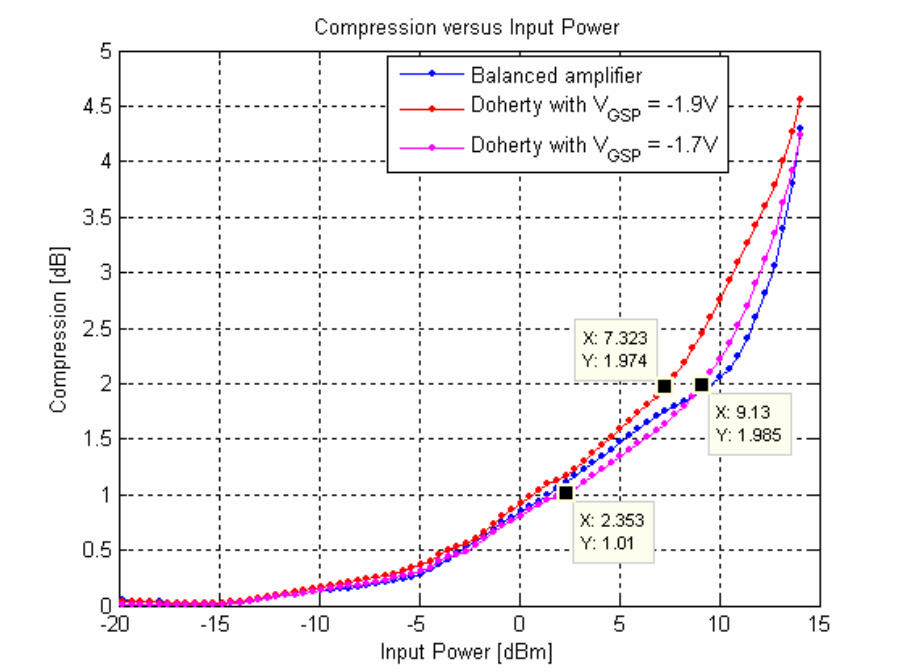


Figure 4.4.24 Measured compression power for the balanced amplifier and Doherty amplifier with V_{GSP} = -1.9V and V_{GSP} = -1.7V.

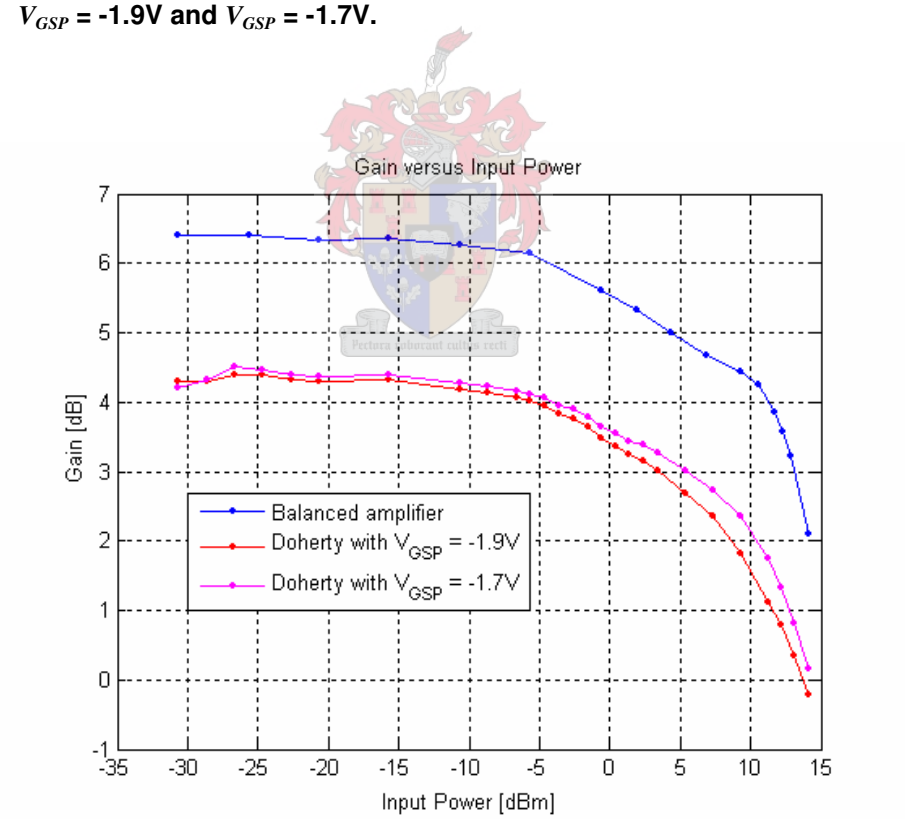


Figure 4.4.25 Measured gain for the balanced amplifier and Doherty amplifier with V_{GSP} = -1.9V and V_{GSP} = -1.7V.

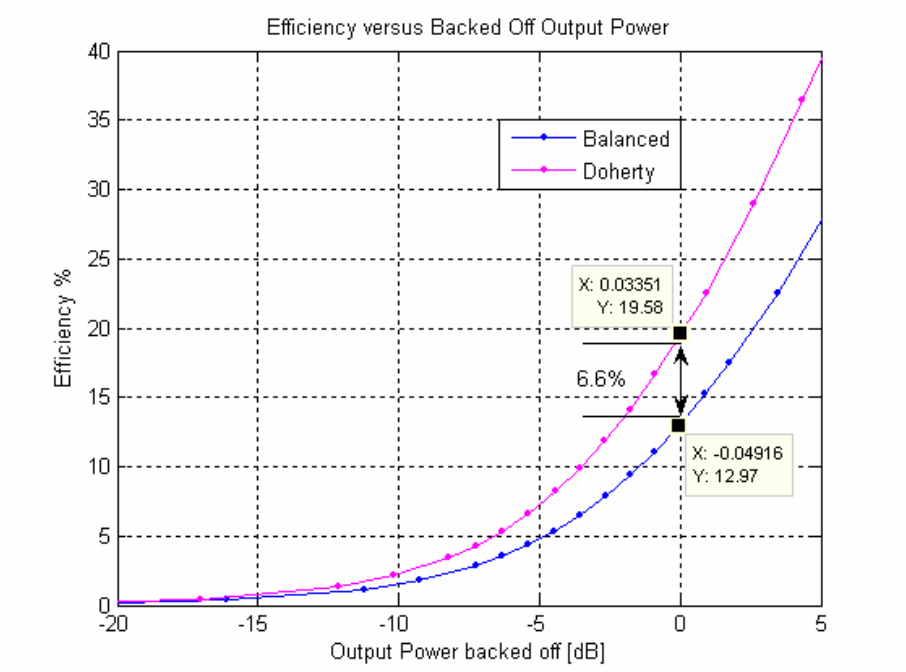


Figure 4.4.26 Measured drain efficiency versus backed-off output power for the balanced amplifier and Doherty amplifier with V_{GSP} = -1.7 V.

Another important factor which is easily forgotten, is the separate phase response of the carrier and peaking amplifiers. In Section 3.3 it is stated that a flat phase response for the peaking amplifier is important and in Section 4.3.2 it is shown that small-signal measurements could be used to predict the phase response for both the peaking and carrier amplifiers for varying input power. This means that, although the carrier and peaking amplifiers can be designed to be in phase at PEP, the peaking amplifier's gate voltage may need to be adjusted to achieve in-phase signals down to 6 dBm back-off. This effect can be seen in Figure 4.4.27, which shows the phase of the peaking amplifier with V_{GSP} = -1.9V and V_{GSP} = -1.7V measured on the non-linear network analyser. The phase response for the designed gate voltage of V_{GSP} = -1.9V is only flat for the upper 5 dBm of input power, which is already above the input power for the 1 dB compression point. The carrier and peaking amplifiers are therefore not in phase, especially at 6 dB back-off. With a gate voltage of V_{GSP} = -1.7V, the amplifier's phase response is flat from about 0 dBm and upward. The peaking and carrier amplifiers are thus only in phase down to about 3 dB back-off.

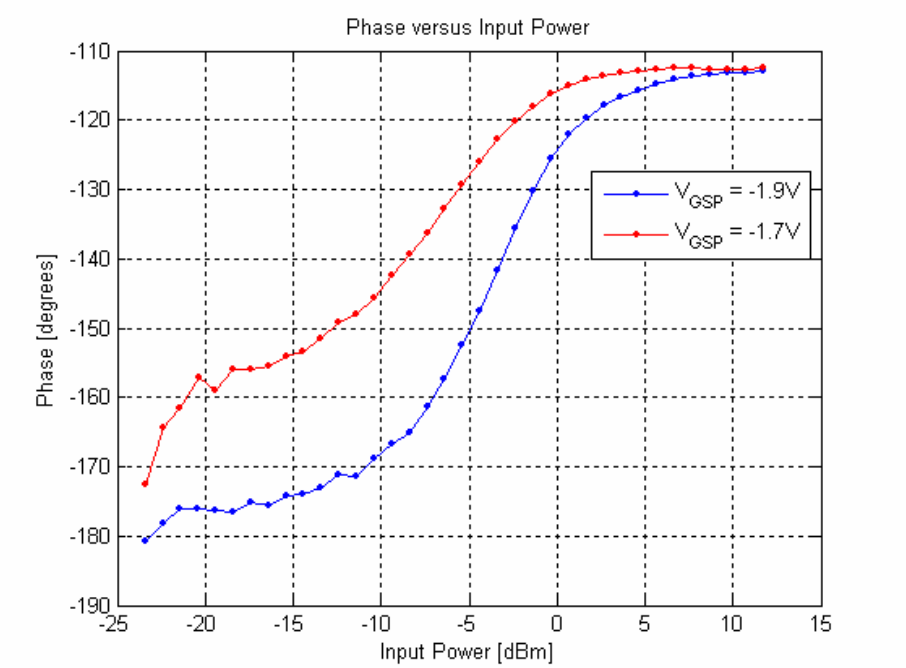


Figure 4.4.27 Measured phase at the fundamental frequency of 1.6 GHz for the peaking amplifier with V_{GSP} = -1.9V and V_{GSP} = -1.7V.

4.4.5 Conclusions

A Classic Doherty amplifier is designed using a small-signal Siemens CFY30 GaAs FET transistor. The Doherty amplifier consists of a carrier amplifier biased in class AB mode and a peaking amplifier biased in class C mode. The layout and manufacturing of the Doherty amplifier is done in such a way that the carrier and peaking amplifiers can be measured separately, with three different loads. A balanced class AB amplifier is also manufactured and essentially consists of two carrier amplifiers in parallel.

The amplifiers are designed at their expected PEP. The PEP corresponds to the maximum input signal at the 1 dB compression point. This input signal is estimated using a measured I_{DS} versus V_{GS} curve. As this is outside any of the amplifier's linear operating regions, measured small-signal S-parameters could not be used directly in the design process. The DC current component is calculated at the estimated PEP. This DC current component has a corresponding gate voltage on the I_{DS} versus V_{GS} curve and measured S-parameters of the transistor at this equivalent gate voltage are used in designing the amplifiers. The accuracy with which the transmission phase of the amplifiers can be predicted is of particular importance, so that appropriate phase compensation can be made to ensure in-phase signals for the carrier and peaking amplifier.

A custom setup and software were developed to measure the designed amplifiers power, gain, compression curves and DC current component.

To verify the validity of the use of measured small-signal S-parameters at an equivalent gate voltage, and the accuracy of the custom setup and software, the transistor and amplifiers are measured on a non-linear network analyser.

The measurements show that this use of S-parameters predicts the transistors phase accurately to within 10°. The custom measurement setup and software also prove to be accurate when compared with the measurements of the non-linear network analyser.

The carrier amplifier is measured on its own with three different loads. The predicted behaviour of the amplifier in terms of its DC current component, gain and compression curves due to the change in load is compared to these measurements. It is found that the measured behaviour of the amplifier corresponds to its predicted behaviour. However, the measured effects are less pronounced than those predicted in each case.

The 1 dB compression point is measured at a much lower input power than that which is expected. The reason given for this is the clipping of the output current waveform on the negative cycle.

The balanced amplifier's simulated small-signal S_{11} and S_{22} are verified with small-signal measurements which show excellent results with the simulations and measurements comparing very well.

Finally, the Doherty configuration is measured, first with V_{GSC} = -1.1V and V_{GSP} = -1.9V. An expected lower gain is measured. The peaking amplifiers DC current component indicates that full load modulation is not achieved, but this is a known drawback of the Classical Doherty amplifier. This serves to confirm what is already mentioned in Section 3.2 and 3.3. There is no significant change in the 1 dB compression point. Overall, the Doherty amplifier shows an increase of 4.2% in drain efficiency over the balanced amplifier at the output power of the 1 dB compression point.

It is shown that the peaking amplifier with V_{GSP} = -1.9V does not have a flat phase response and that it only starts conducting at the point where the overall Doherty amplifier reaches its 1 dB compression point. To increase the fundamental current component of the peaking amplifier and obtain a flatter phase response from it, the gate voltage is increased to V_{GSP} = -1.7V.

Comparing the changes in the DC current component (of the carrier amplifier), gain and compression curves of the Doherty amplifier to that of the separate carrier amplifier in Section 4.4.1, the effect of load modulation can be seen. This load modulation, however, is more evident beyond

the 1 dB compression point. The important point is that dynamic load modulation is achieved. The Doherty amplifier shows an increase of 6.6% in drain efficiency to that of the balanced amplifier.

These results are satisfactory and provide a great deal of additional insight into the operation of a Doherty amplifier. Although the limited load modulation is proven to be due to insufficient current contribution from the peaking amplifier, an increase in drain efficiency is still possible and therefore justifies the use of the design procedure for the development of a 10W Doherty power amplifier.

Chapter 5

10W Doherty Power Amplifier Design

5.1 Introduction

A procedure for designing a Doherty amplifier is proposed and described in the previous chapter using a Siemens CFY30 GaAs FET transistor. The results are satisfactory and a great deal of insight was gained. This design procedure will now be used to design a Doherty power amplifier using a 10 W Motorola MRF282 LDMOS transistor (Datasheet can be found in Appendix A).

Since the same design procedure used in the previous chapter is followed it will be discussed in less detail. The same setup and software are used with only minor modifications. These modifications will be singled out.

At the end of the chapter the measurements will be compared to those found in existing literature.

5.2 Design of a 10W LDMOS Doherty Amplifier

5.2.1 Stability, Biasing and Calculating R_{opt}

The 10W Doherty power amplifier will be designed at a centre frequency of 1.643 GHz. The biasing network is designed utilising the same procedure implemented in the small-signal Doherty amplifier analysis. The same applies to the stabilising network. Stabilisation networks were added to the gate

and drain terminals of the MRF282. Figure 5.2.1 shows the MRF282 transistor with biasing and stabilising networks.

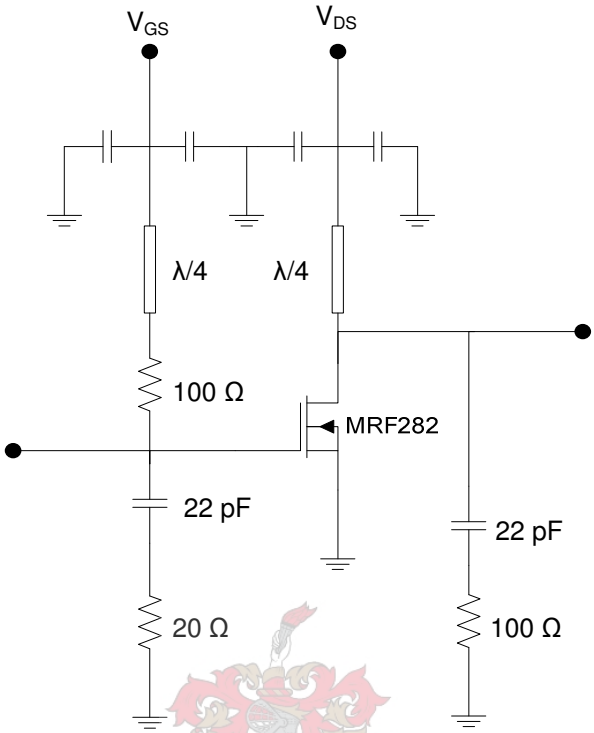


Figure 5.2.1 MRF282 transistor with stabilising and biasing networks.

The next step is to choose the biasing voltages for the carrier and peaking amplifiers.. The rated maximum drain voltage according to the datasheet is V_{DSmax} = 65V. With a knee voltage of V_{knee} = 6V, maximum voltage swing will be permitted with a drain voltage of

$$V_{DS} = \frac{V_{\max} - V_{knee}}{2} + V_{knee} = 35.5V$$

However, the DC sources to be used have a maximum voltage rating of 20V. The drain voltage is therefore chosen to be V_{DS} = 20V. This lower drain voltage will degrade the rated performance of the transistor in terms of gain, 1 dB compression and output power.

Using the same method as in Section 4.2.1 with the MRF282's measured I_{DS} versus V_{GS} curve, shown in Figure 5.2.2, the gate voltage for the carrier and peaking amplifiers is defined as V_{GSC} = 5V and V_{GSP} = 1.9V respectively. The carrier amplifier will have a quiescent drain current of I_{DSQ} = 350 mA and will permit an input voltage signal with an amplitude of 4V before saturation. A voltage signal with an amplitude of 4V will dissipate 22 dBm of power in a 50 Ω load. Peak envelope power is thus expected at approximately 22 dBm input power.

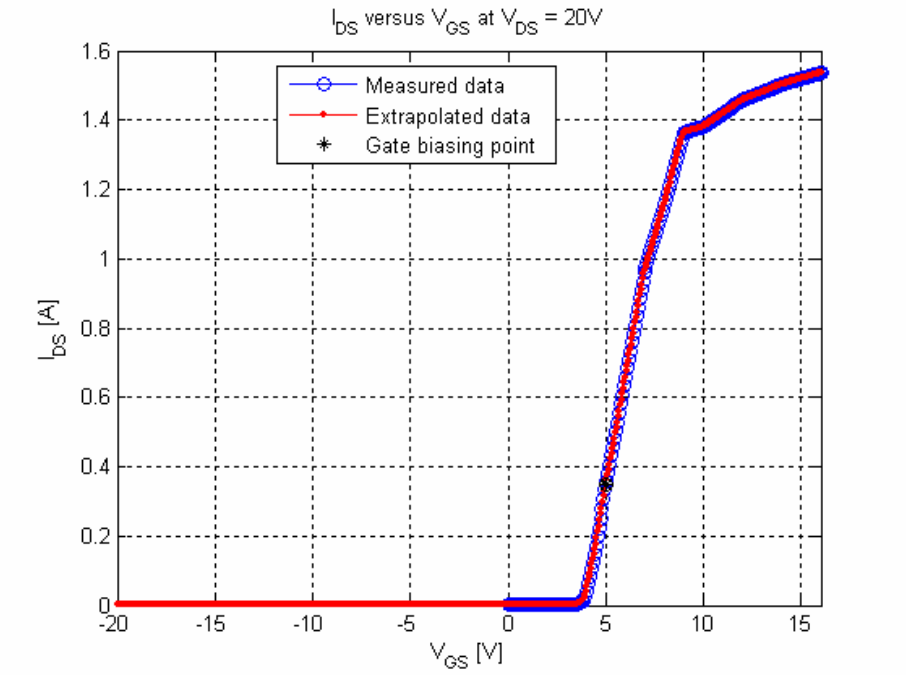


Figure 5.2.2 **I_d vs V_{gs} curve for MRF282 transistor at V_{DS} = 20V. Gate voltage of V_{GS} = 5V is also indicated.**

Figure 5.2.3 shows the predicted phase response for the MRF282 transistor by using the equivalent gate voltage method described in Section 4.2.1. The phase response is shown for three different quiescent gate voltages: V_{GS} = 1.9V, 3V and 5V. For V_{GS} = 5V the transistor has a flat phase response, but for V_{GS} = 1.9V there is a phase change of approximately 80° between 12 dBm to 17 dBm input power. The third phase response is for V_{GS} = 3V. This phase response has a change of approximately 65°, but is flat for the upper 20 dBm of input power.

By using a gate voltage of V_{GSP} = 1.9V for the peaking amplifier and assuming 1 dB compression occurs at 22 dBm input power, the peaking amplifier will only be in phase with the carrier amplifier for the upper 5 dBm of input power. In order to achieve phase correspondence at lower input power levels, a higher gate voltage is necessary. On the other hand, a higher gate voltage will lower the input power where the peaking amplifier starts conducting, thus moving away from the designed 6 dB back-off point. Therefore, the proposed peaking amplifier gate voltage (V_{GSP} = 1.9V) is satisfactory.

With a maximum input voltage of 4V, the carrier and peaking amplifiers will each have a DC current component of 0.533A and 0.136A respectively, which respectively gives an equivalent gate voltage, V'_{GS}, of 5.62V and 4.36V.

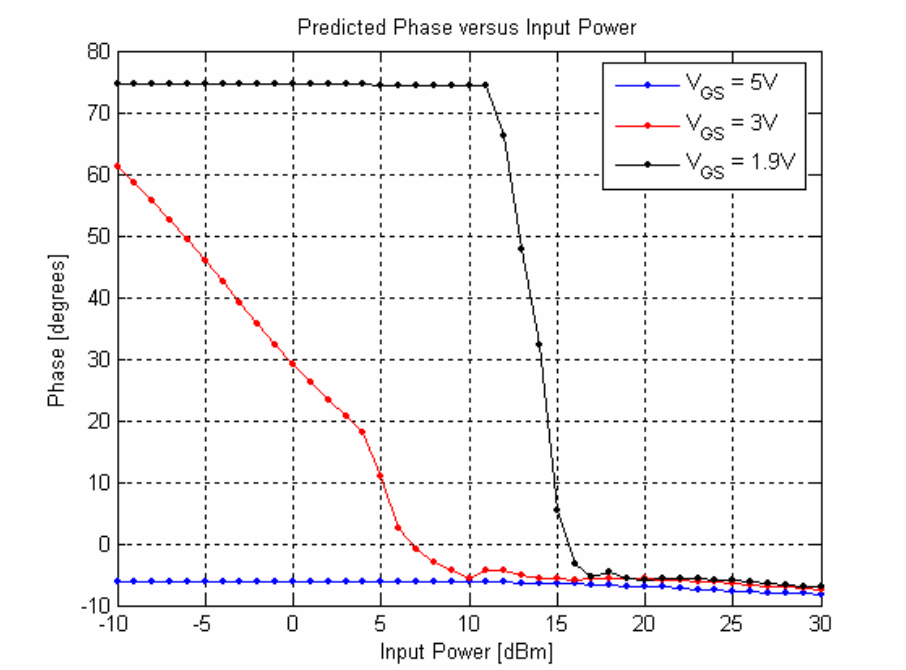


Figure 5.2.3 Predicted phase response versus input power for MRF282 transistor at three different gate voltages.

In order to determine the optimal resistance for the carrier and peaking amplifiers, the fundamental current components for both amplifiers with a 4V input voltage signal are calculated using the MATLAB code explained in Section 2.3.1. For the MRF282 the knee voltage was not taken as a constant but as a curve, as shown in Figure 5.2.4. Calculating the optimal resistance for the maximum input voltage, the knee voltage is taken as V_{knee} = 6V which corresponds to high gate voltages. The fundamental current component for the carrier amplifier is calculated to be I_{1C} = 0.75A. Using equation (2.5) the optimal resistance for the carrier amplifier is calculated to be

$$R_{optC} = \frac{20-6}{0.75} = 18.7\Omega$$

The peaking amplifier has a calculated fundamental current component of I_{1P} = 0.24 A and an optimal resistance of

$$R_{optP} = \frac{20-6}{0.24} = 57.4\Omega$$

An initial R_o is chosen to be equal to R_{optC} and thus $R_o = R_{optC}$ = 18.7 Ω.

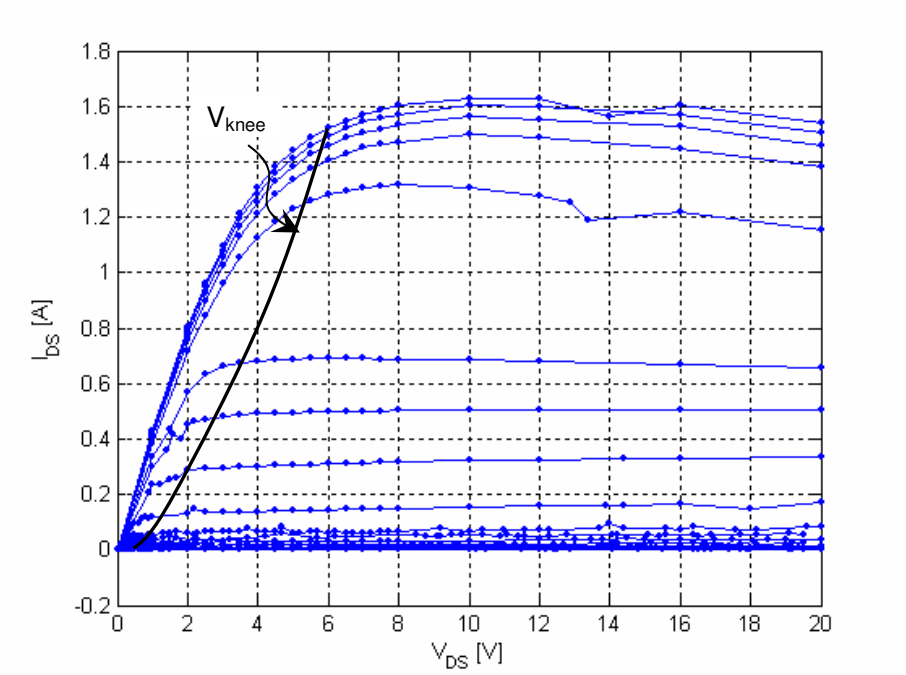


Figure 5.2.4 MRF282's measured IV-curve and knee voltage.

5.2.2 Carrier Amplifier Design

For the small-signal amplifier an optimal impedance Z_{optC} was calculated with the aid of an optimiser in MATLAB. The Z_{optC} impedance is the load the output of the transistor has to see to ensure the internal current source sees the optimal load-line resistance. According to the optimiser this impedance for the MRF282 is $Z_{optC} = 8 - j1.16\ \Omega$. The CFY30 transistor has a stabilising network at the gate terminal only. The MRF282 also has a stabilising network at the drain terminal and this has to be taken into account. Looking at Figure 5.2.5 it is clear that an additional optimal impedance Z'_{optC} has to be calculated. The MATLAB code could have been modified to incorporate the effect of the stabilising network, but Microwave Office's optimiser offered a fast solution and calculated an equivalent optimal impedance, $Z'_{optC} = 8.9 - j1.8\ \Omega$.

The matching network required to convert R_o to Z'_{optC} consists of a series transmission line and capacitor. The transmission line has a characteristic impedance of 18.7 Ω and a length of 48.6°. The capacitor has a value of 6.7 pF and the matching circuit is shown in Figure 5.2.6.

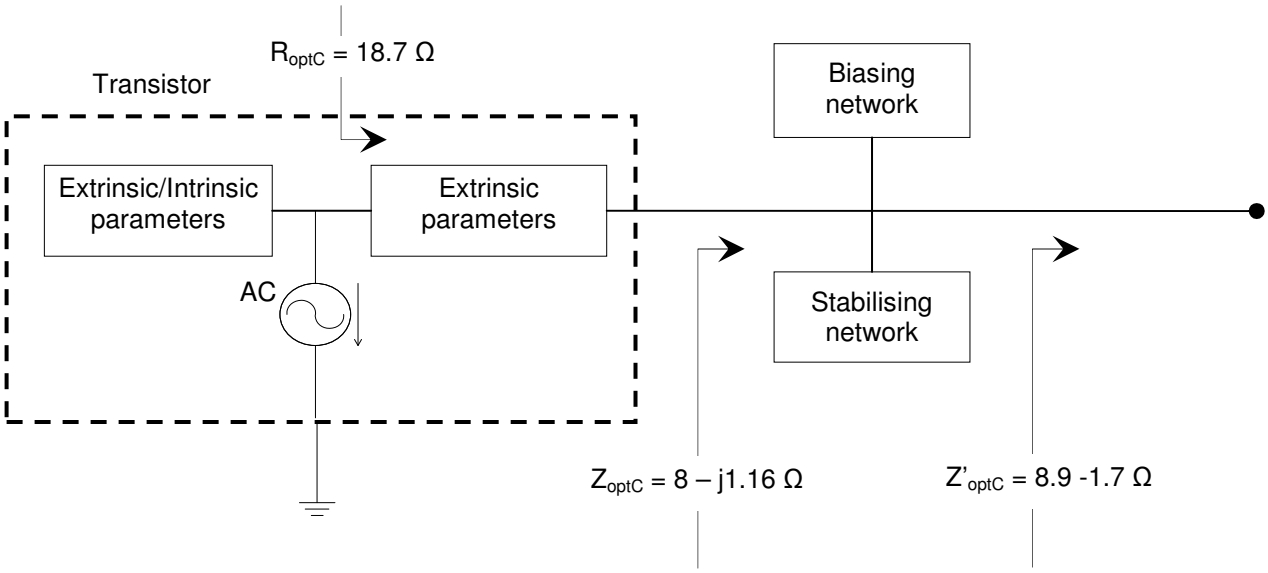


Figure 5.2.5 Carrier amplifier with biasing and stabilising network showing position of optimal load-line resistance, R_{optC}, impedance, Z_{optC}, and equivalent impedance, Z'_{optC}.

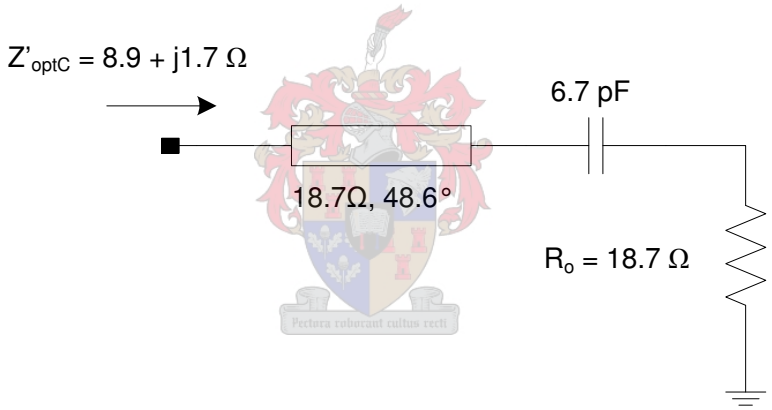


Figure 5.2.6 Matching network to match 18.7Ω to 8.9 + j1.7Ω.

During the design of the carrier amplifier (Section 4.2.2) of the small-signal Doherty amplifier, the length of the offset line was determined by adding the quarter-wave transmission line and a load of $0.5R_o$ in the simulation. The length of the offset line was then varied until the impedance seen by the internal current source was as close as possible to $2R_{optC}$. Since the characteristic impedance of the quarter wave impedance inverter and offset line is equal, it was decided to combine these two lines in the design of the Doherty power amplifier. This means that no offset line is added in the simulation, but the length of the quarter-wave transmission line is optimised in Microwave Office until the impedance seen by the internal current source is as close as possible to $2R_{optC}$. In addition to the quarter-wave impedance inverter, the value of R_o is also optimised, having an initial value of 18.7 Ω. The final combined length of the quarter-wave impedance inverter and offset line is 0° and the value for R_o is R_o = 15.7 Ω. Figure 5.2.7 shows the initial output network with R_o = 18.7 Ω and quarter-wave impedance inverter, together with the output matching, extrinsic parameters, biasing and stabilising

networks. Figure 5.2.8 shows the final output network with R_o = 15.7 Ω and without any quarter-wave impedance inverter or offset line.

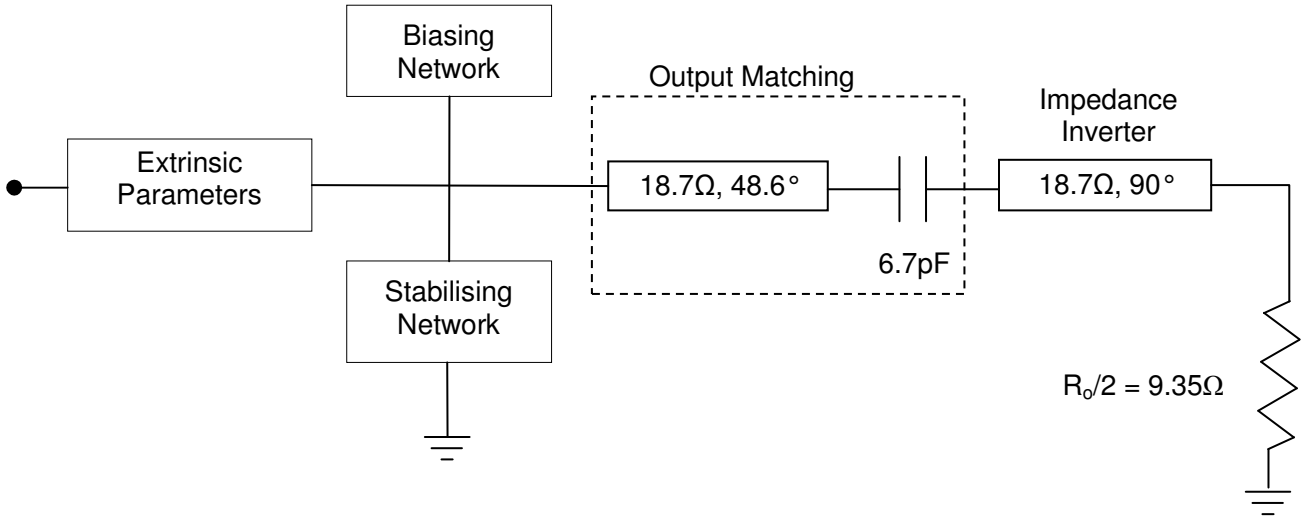


Figure 5.2.7 Carrier amplifier with extrinsic parameters, biasing and stabilising networks, output matching, quarter-wave impedance inverter and 0.5R_o = 9.35Ω load.

Figure 5.2.9 shows the simulated impedance seen by the internal current source for the low and high power operation, before and after optimising R_o and the combined length of the impedance inverter and offset line. R_{optC} was calculated as 18.7 Ω, which is the impedance the internal current source should see at PEP. Theoretically, the internal current source should see $2R_{optC}$ = 37.4 Ω during low power operation to keep the transistor at the point of saturation. To calculate a more accurate resistance for low power operation, the varying knee voltage (see Figure 5.2.4) is taken into account and a new fundamental current component of I_1 = 0.52A is calculated with an input voltage amplitude of 2V, which is half of the maximum input voltage amplitude calculated in Section 5.2.1. Using equation (2.5), V_{knee} = 3V, I_1 = 0.52A and V_{DS} = 20V, the impedance for low power operation is calculated to be 32.6 Ω. The simulation results of 19.6 Ω for the high power operation and 33.76 + j0.56 Ω for the low power operation shown in Figure 5.2.9 are very close to the desired values with.

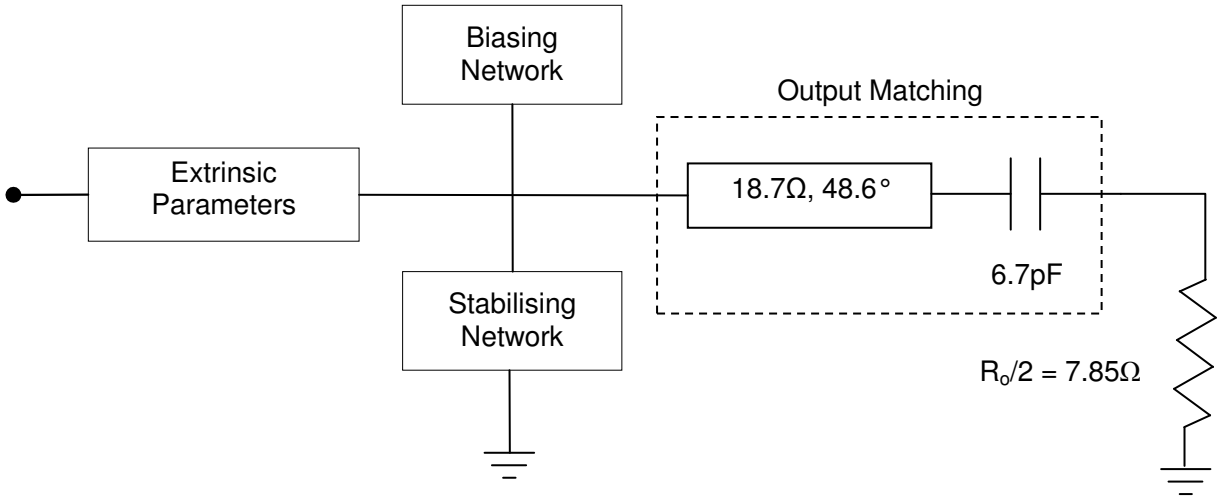


Figure 5.2.8 **Final output network of the carrier amplifier. Extrinsic parameters, biasing and stabilising networks, output matching, and 0.5R_o = 7.85Ω load are shown. Note that there is no quarter-wave impedance inverter.**

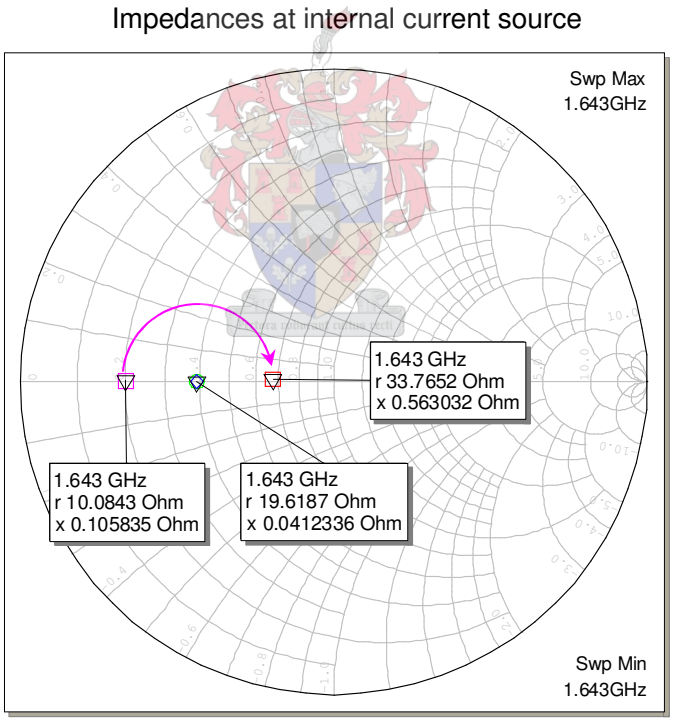


Figure 5.2.9 **Transforming the impedance seen by internal current source of the Freescale MRF282 in the low power operation from 10.1 + j0.1Ω (□) to 33.8 + j0.6Ω (□) by removing the quarter-wave impedance inverter and changing R_o from 18.7Ω to 15.7Ω. The impedance for the high power operation stays the same at 19.6 + j0.04Ω (Δ and o).**

The design of the input matching network is carried out following the same method used in Section 4.2.2 during the design of the small-signal amplifier. For the carrier amplifier with a maximum input

voltage amplitude of 4V, a DC current of 0.53 mA is calculated, which in turn correspond to an equivalent gate voltage of V'_{GS} = 5.6 V. The amplifier's input impedance at PEP was calculated to be 2.46 – j5.35 Ω. The input matching network consists of a series transmission line with a characteristic impedance of 20 Ω and length of 64.4° in series with a 1.2 pF capacitor. The matching network is shown in Figure 5.2.10.

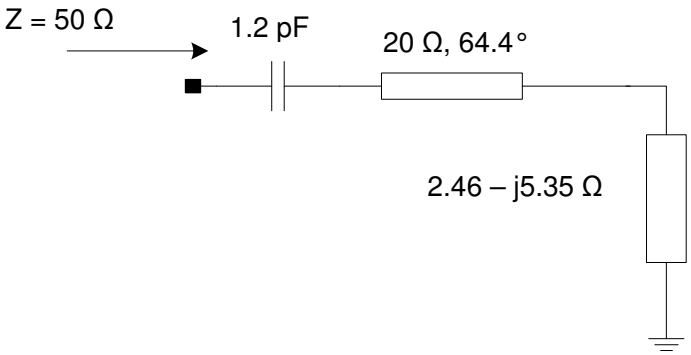


Figure 5.2.10 Input matching network for the carrier amplifier.

Simulated S_{11} and S_{21} are shown in Figure 5.2.11 and Figure 5.2.12 respectively. The simulations are done with the transistor S-parameters at the equivalent gate voltage as was used in the design process and the output port termination equal to R_o = 15.7 Ω. The simulations show a good input match of below -35 dB and a gain of 11.7 dB at the centre frequency of 1.643 GHz. Figure 5.2.13 shows a simplified schematic for the final carrier amplifier design.

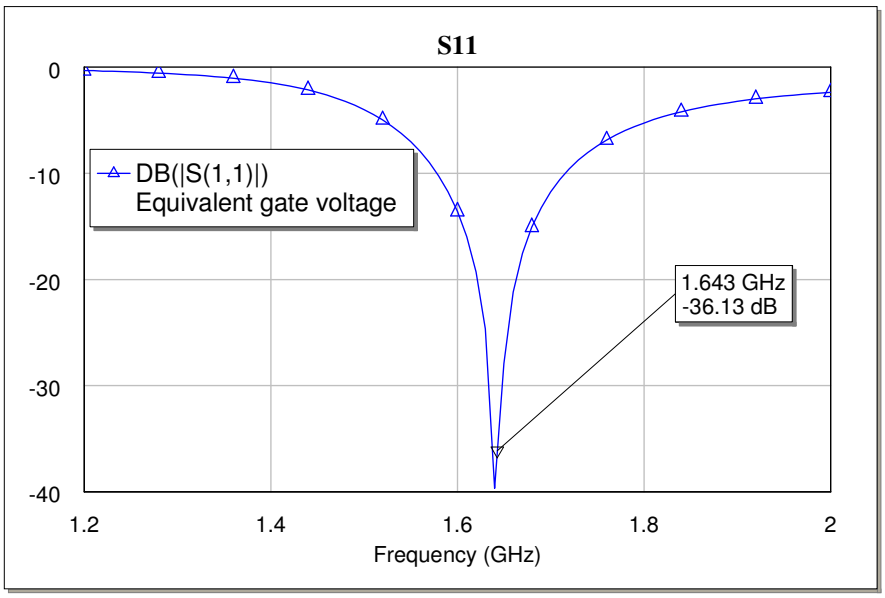


Figure 5.2.11 S_{11} for carrier amplifier using S-parameters for the transistor at the equivalent gate voltage (Δ) and an output termination of R_o = 15.7 Ω.

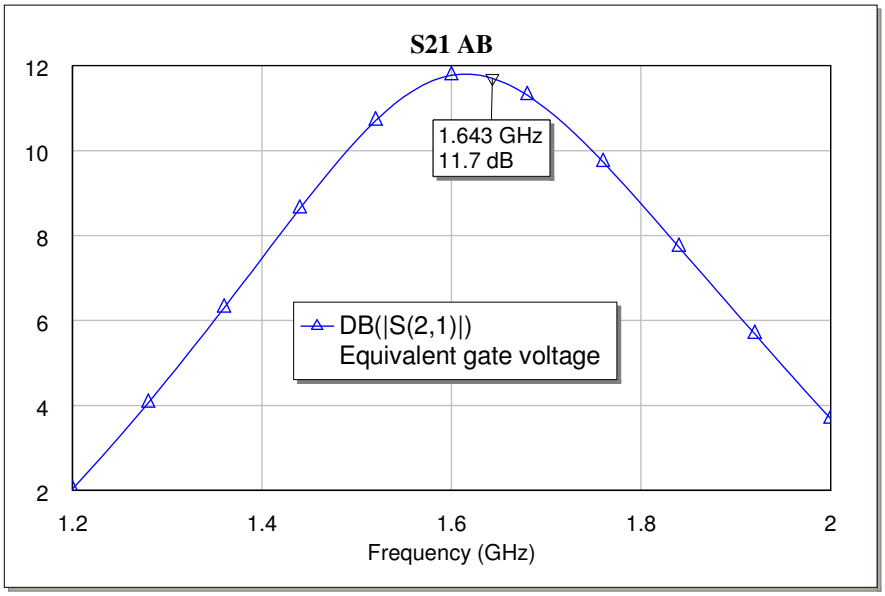


Figure 5.2.12 S_{21} **for carrier amplifier using S-parameters for the transistor at the equivalent gate voltage (Δ) and an output termination of** R_o **= 15.7 Ω.**

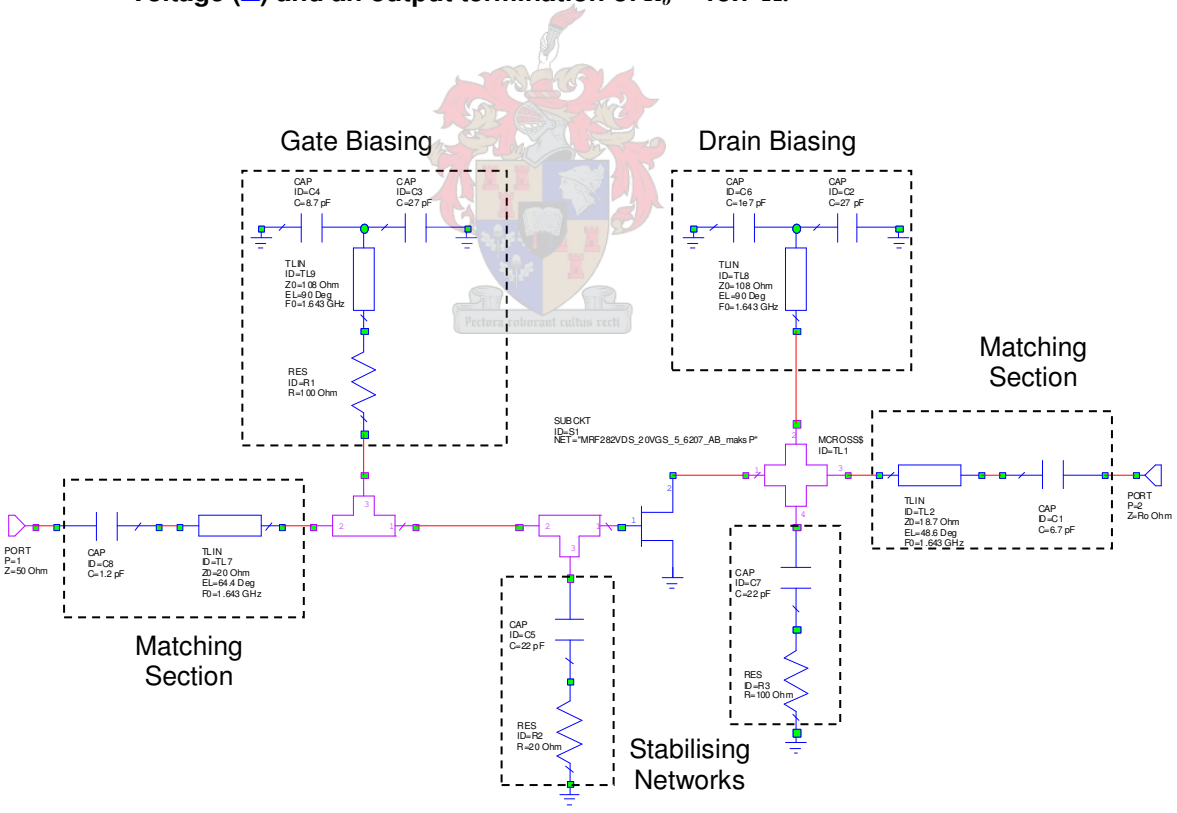


Figure 5.2.13 A simplified schematic of the carrier amplifier design.

5.2.3 Peaking Amplifier Design

In Section 5.2.1 the optimal resistance for the peaking amplifier, R_{optP}, is calculated to be 57.4 Ω. An optimal impedance of Z_{optP} = 3.6 + j4.9 Ω is calculated and an additional optimal impedance of Z'_{optP} = 3 + j4.4 Ω to compensate for the stabilising network. The output matching circuit which converts R_o to Z'_{optP} is shown in Figure 5.2.14 and consists of a series transmission line with characteristic impedance of 16.2 Ω and a length of 91° in series with a 2.2 pF capacitor.

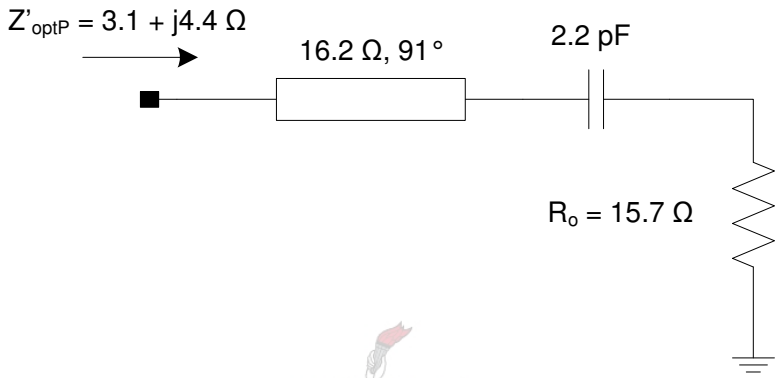


Figure 5.2.14 Output matching circuit for the peaking amplifier.

The output impedance of the peaking amplifier at its bias point is simulated to be 22.1 – j101.2 Ω. By adding an offset line of characteristic impedance equal to R_o = 15.7 Ω and length 171.6°, the output impedance of the peaking amplifier is converted to 495.8 – j7.4 Ω. This conversion is illustrated on a smith chart in Figure 5.2.15.

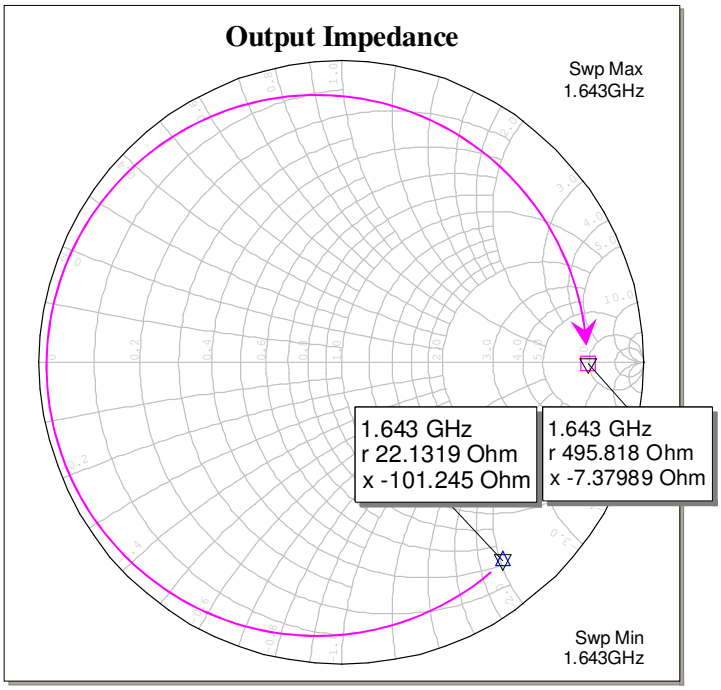


Figure 5.2.15 The output impedance of the peaking amplifier is converted from 22.1 – j101.2Ω (Δ) to 495.8 – j7.4Ω (□) with an offset line of length θ_p = 171.6°.

The input impedance of the peaking amplifier, with the S-parameters for the transistor at the equivalent gate voltage, V'_{GS} = 4.36V, is simulated to be 1.64 + j4.67 Ω. The input matching circuit consists of a series transmission line with a characteristic impedance of 20 Ω and a length of 67.7° in series with a 1 pF capacitor. The matching circuit is shown in Figure 5.2.16.

Simulated S_{11} and S_{21} is shown in Figure 5.2.17 and Figure 5.2.18 respectively. The simulations are done with the transistor S-parameters at the equivalent gate voltage, V'_{GS} = 4.36V, and the output port termination equal to R_o = 15.7 Ω. The simulation results show a good input match below -20 dB and a gain of 15.18 dB at the centre frequency of 1.643 GHz. As in the S_{21} simulation of the small-signal peaking amplifier in Section 4.4.2, the gain is very high due to the linear S-parameters being used. Figure 5.2.19 shows a simplified schematic for the final peaking amplifier design.

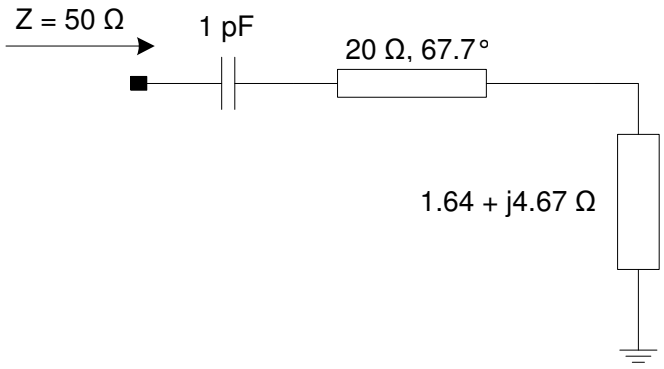


Figure 5.2.16 Input matching circuit for the peaking amplifier.

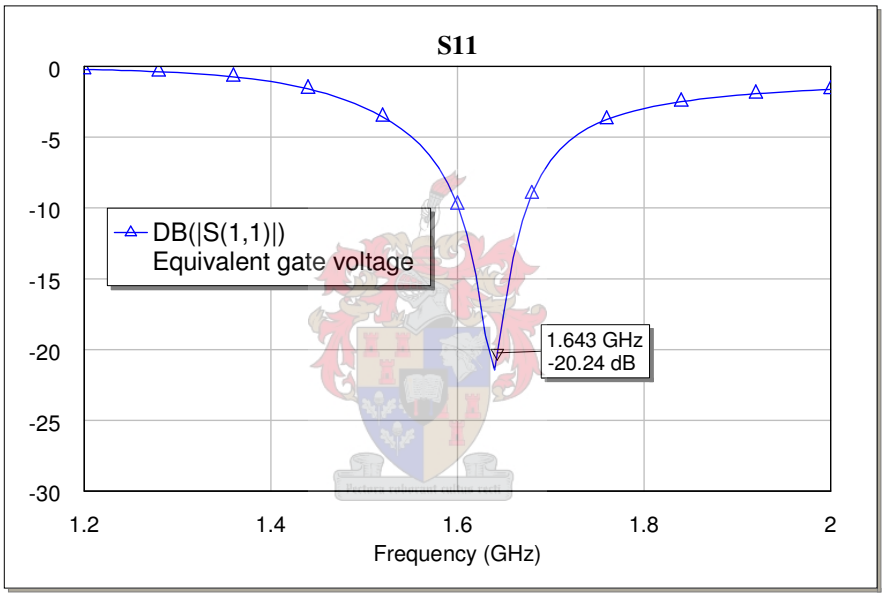


Figure 5.2.17 S_{11} for the peaking amplifier using S-parameters for the transistor at the equivalent gate voltage (Δ) and an output termination of R_o = 15.7 Ω.

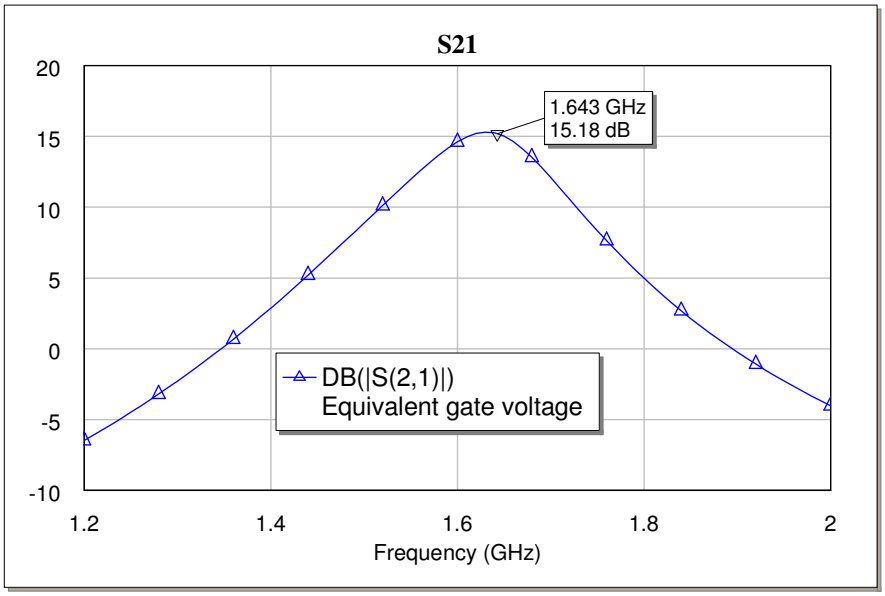


Figure 5.2.18 S_{21} **for the peaking amplifier using S-parameters for the transistor at the equivalent gate voltage (Δ) and an output termination of** R_o **= 15.7 Ω.**

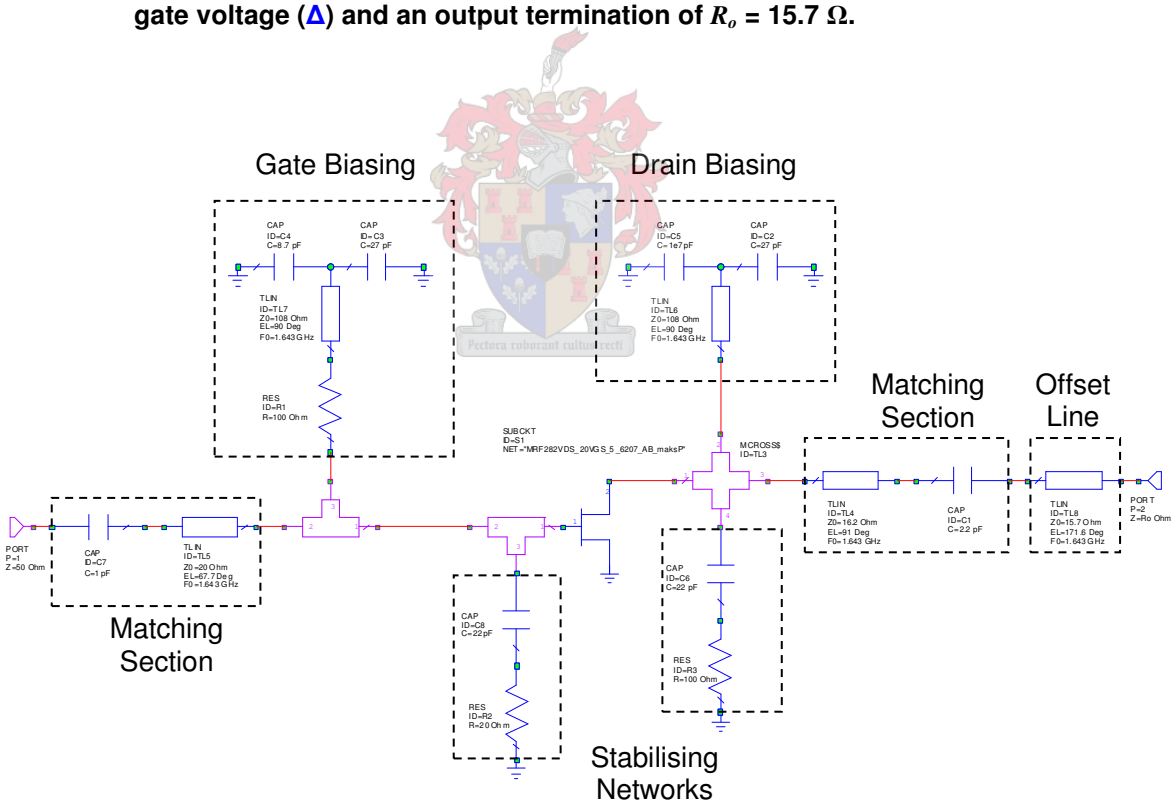


Figure 5.2.19 A simplified schematic of the peaking amplifier design.

5.2.4 Input Power Divider Design, Combined Load, Layout and Balanced Amplifier

In the ideal theory the carrier amplifier's output lags the peaking amplifier's output with 90°. In the small-signal Doherty amplifier design of Chapter 4, the peaking amplifier lags the carrier amplifier by 40.48°. In the current design the peaking amplifier lags the carrier amplifier by 194.33°. A 90° power divider will be used at the input of the Doherty amplifier. The carrier amplifier's input will be connected to the lagging port of the divider with an extra 104.33° delay line. The input signal to the carrier amplifier should then lag the input signal to the peaking amplifier by 194.33°.

R_o is defined as 15.7 Ω, and the combined load of the Doherty amplifier as $0.5R_o$ = 7.5 Ω. The amplifier will be measured in a 50 Ω system, and therefore a quarter-wave transformer is needed at the output to convert 50 Ω to 7.5 Ω. This quarter-wave transformer has a characteristic impedance of 20 Ω.

Figure 5.2.20 illustrates the use of the 90° hybrid power divider and 104.33° delay line before the carrier amplifier and the quarter-wave transformer at the output. The output combining network is not explicitly shown, and any matching networks and offset lines form part of the carrier and peaking amplifier symbols.

The amplifiers were fabricated on 0.51 mm-thick Rogers RO4003 substrate with a permittivity of 3.38 and conductor thickness of 35 μm. The datasheet is given in Appendix A.

Figure 5.2.21 show the final layout for the Doherty amplifier. The carrier amplifier is at the top and the peaking amplifier at the bottom. Figure 5.2.22 shows a photo of the manufactured Doherty amplifier.

As during the small-signal Doherty amplifier analysis, a control amplifier to which the Doherty amplifier's performance can be compared is needed. This control amplifier is a balanced class AB amplifier consisting of two carrier amplifiers joined together in parallel with a 90° hybrid divider/combiner at the input and output. Figure 5.2.23 shows the layout of the balanced class AB amplifier and Figure 5.2.24 shows the manufactured amplifier.

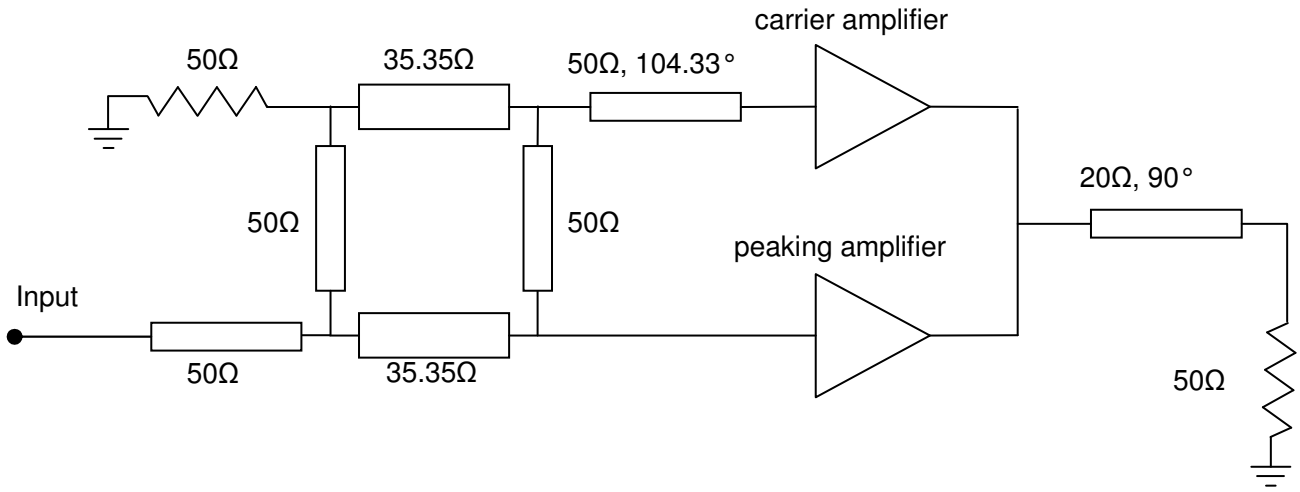


Figure 5.2.20 Schematic showing the extra 104.33° delay line between the divider and carrier amplifier to ensure the input signal at the carrier amplifier is lagging the input signal at the peaking amplifier with 194.33°. The 20 Ω quarter-wave transformer at the output is also shown.

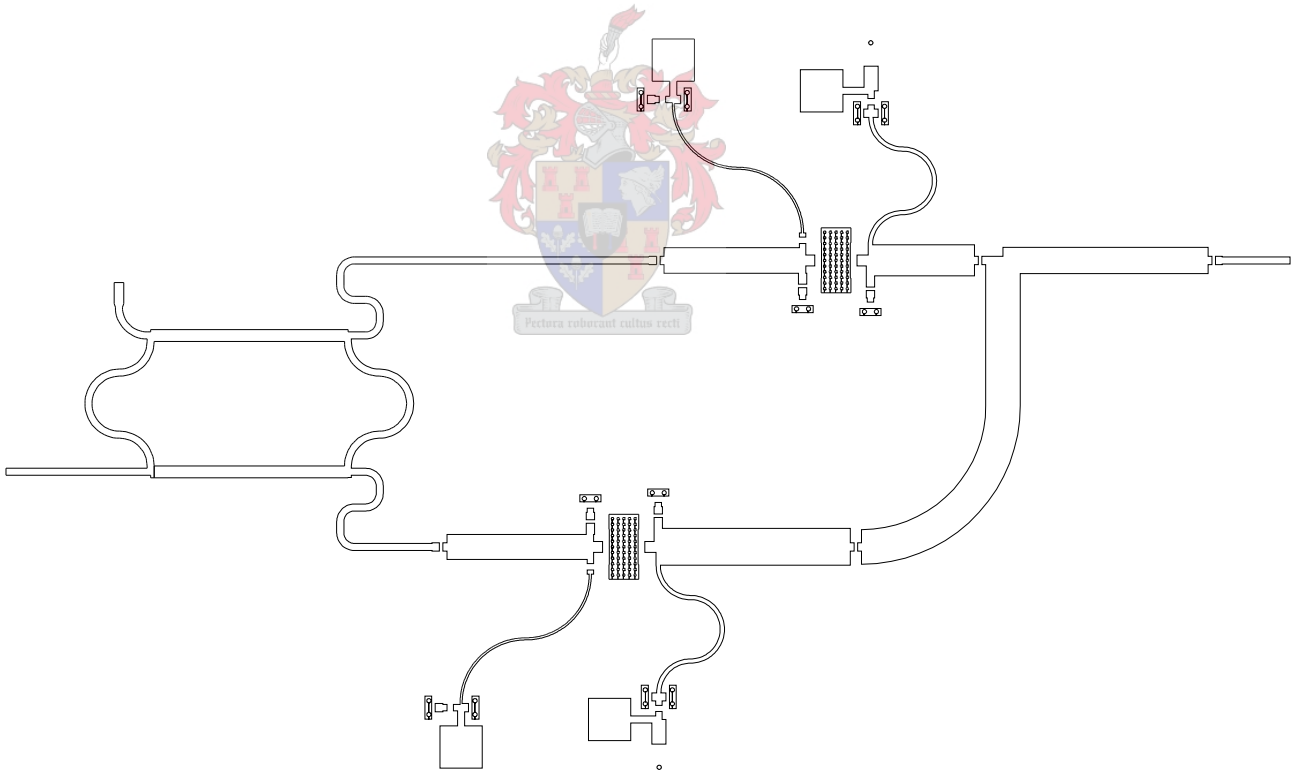


Figure 5.2.21 Layout for the Doherty amplifier. The carrier amplifier is at the top, and the peaking amplifier at the bottom.

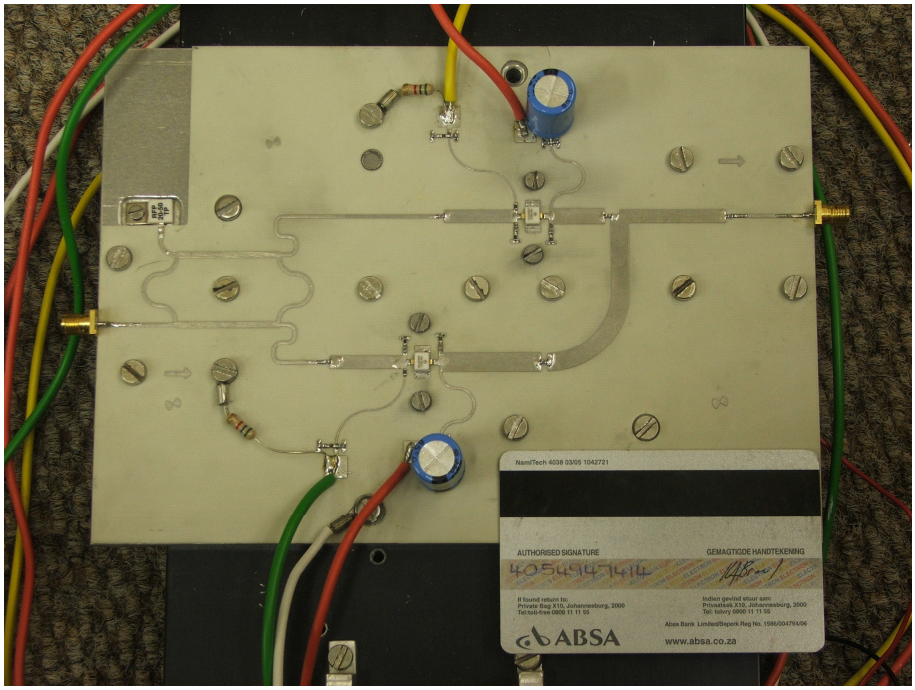


Figure 5.2.22 Photo of the manufactured Doherty amplifier.

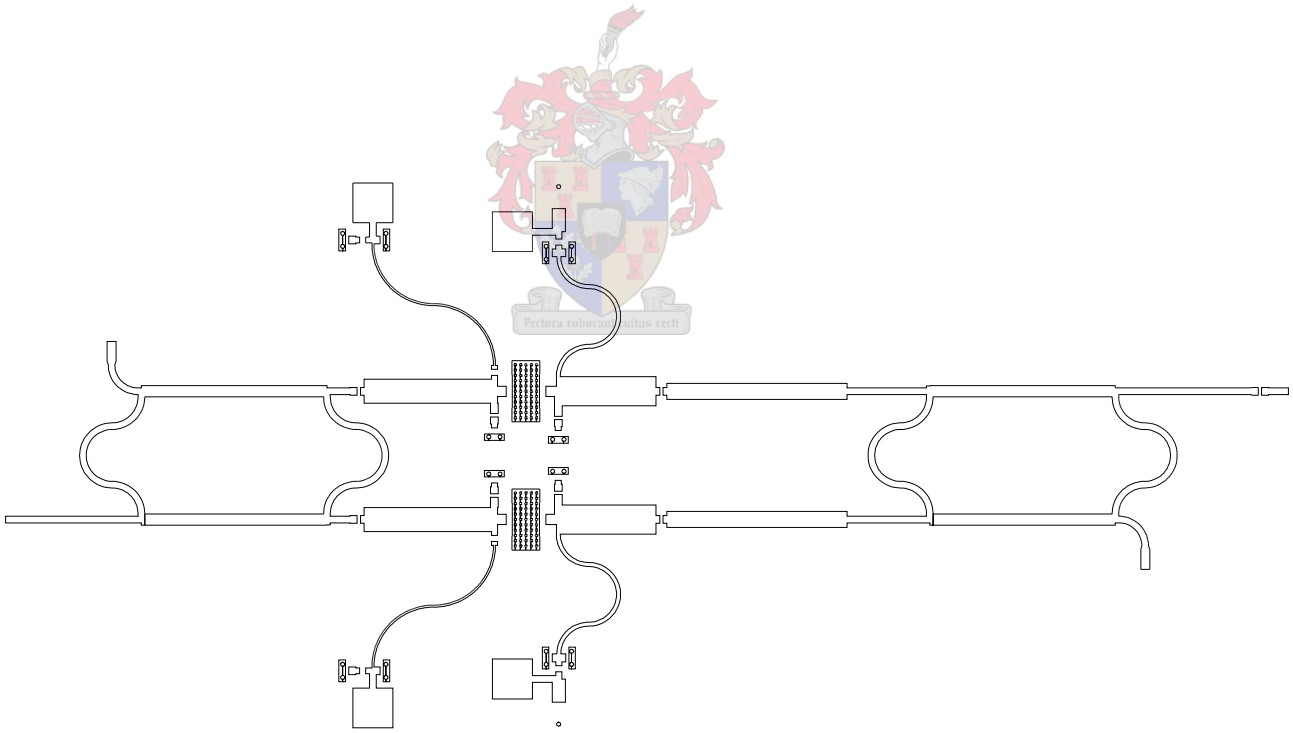


Figure 5.2.23 Layout of the balanced class AB amplifier.

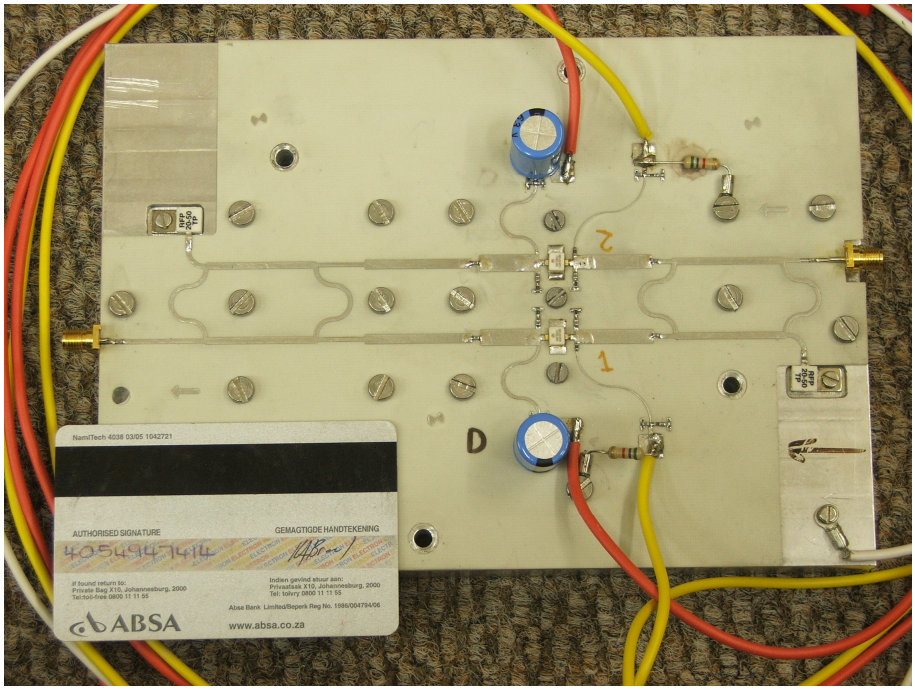


Figure 5.2.24 Photo of manufactured balanced amplifier.

5.3 Measurement Setup and Software

The measurement setup and software used in Section 4.3.1 is now utilised to measure the Doherty power amplifier. The only difference is that an additional driver amplifier is needed to push the Doherty power amplifier into saturation. A circulator is added at the driver amplifier's output to protect the driver amplifier and a low pass filter is added to filter out any unwanted harmonics generated by the driver amplifier. The 30 dB attenuator between the DUT and the spectrum analyser protects the spectrum analyser from the power amplifiers being characterised.

Although there are extra components in this measurement setup, the calibration procedure is the same as that used and described in Section 4.3.1. The effect of the driver amplifier, circulator, low pass filter and any cables connecting them together will form part of the error matrix [E_{AB}]. The effect of the 30 dB attenuator and the cables used to connect it between the DUT and spectrum analyser will form part of the error matrix [E_{CD}]. Figure 5.3.2 shows a photo of the measurement setup.

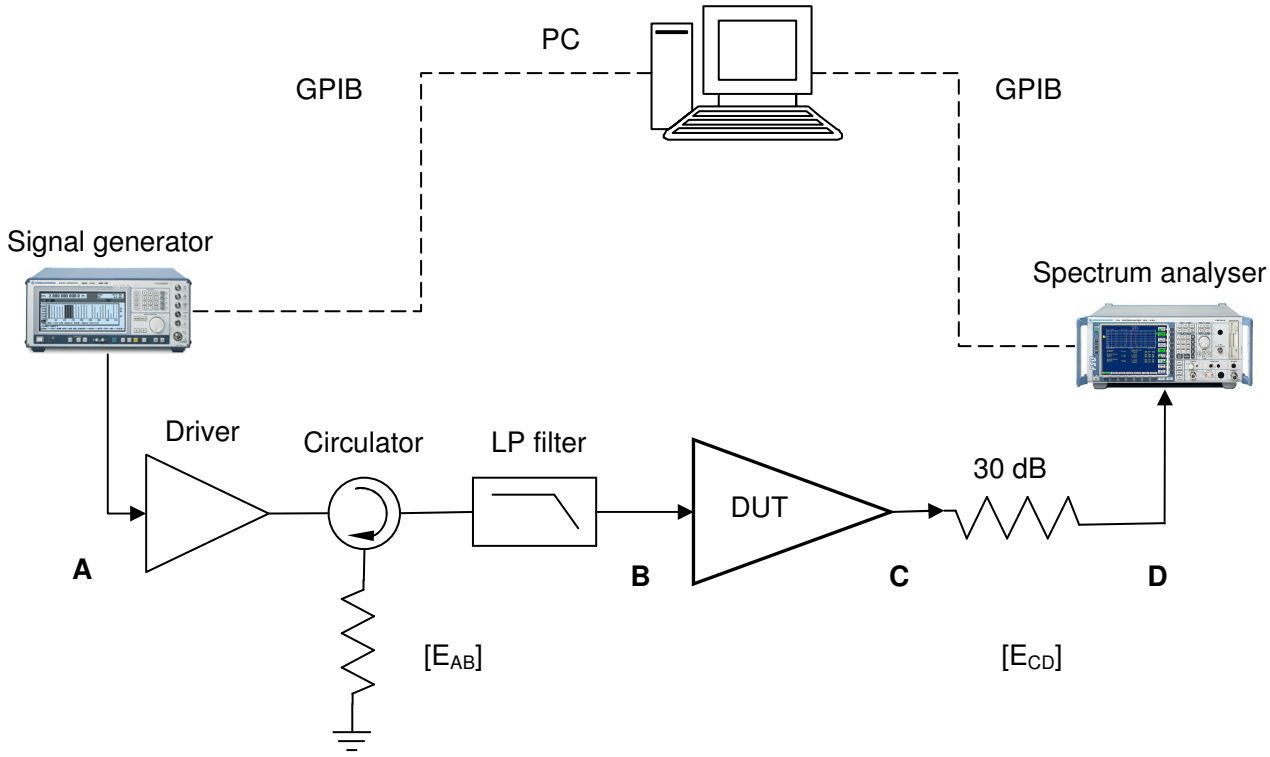


Figure 5.3.1 GPIB controlled measurement setup.

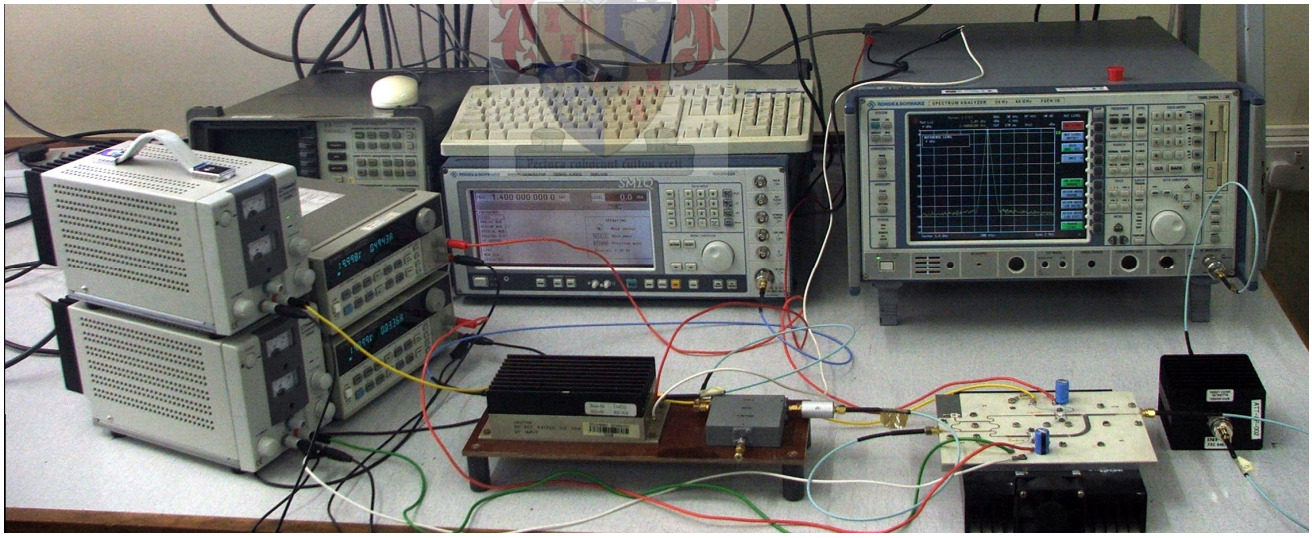


Figure 5.3.2 Photo of the measurement setup.

5.4 Measurement Results

5.4.1 Small-signal Measurements

Before investigating the compression, power and efficiency curves, small-signal measurements are performed on the Doherty and balanced class AB amplifiers. These measurements are carried out with the defined biasing drain and peaking amplifier gate voltages. V_{DSQ} = 20V, V_{GSP} = 2V. The defined carrier amplifier gate voltage is V_{GSC} = 5V with a resulting DC current component of I_{DS} = 0.35A. The gate voltages for the carrier amplifier and balanced amplifier are therefore adjusted to achieve a quiescent drain current of 0.35A before starting a measurement. These measurements will then be compared against simulations done in Microwave office where the S-parameters at the biasing points for the transistor were used. Figure 5.4.1 to Figure 5.4.4 shows the comparison between the S_{11} and S_{21} measurements and simulations for the Doherty and balanced amplifier. In all of the figures the simulation results are frequency shifted by 200 MHz in relation to the measured results.

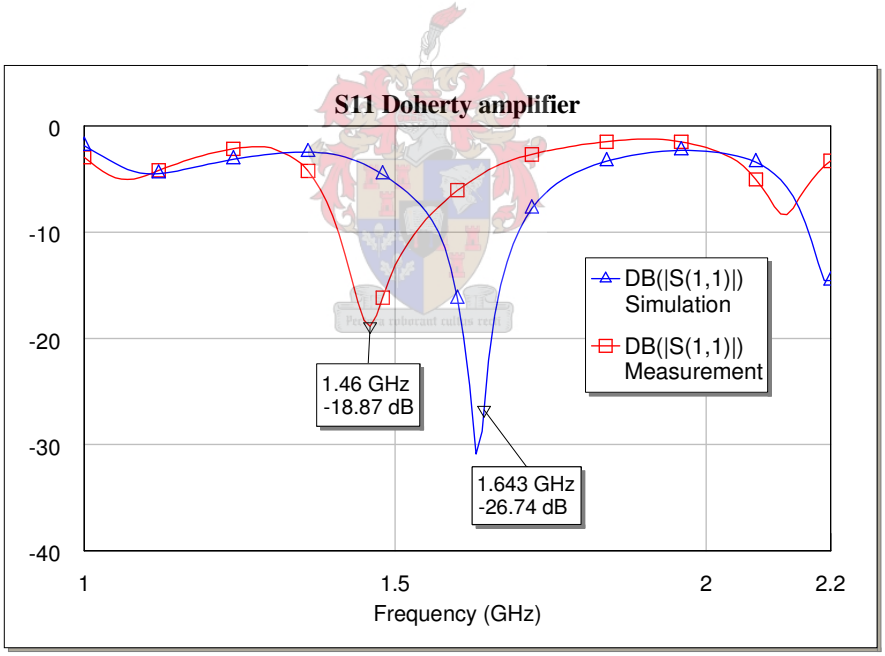


Figure 5.4.1 Simulated (Δ) and measured (□) S_{11} of the Doherty amplifier.

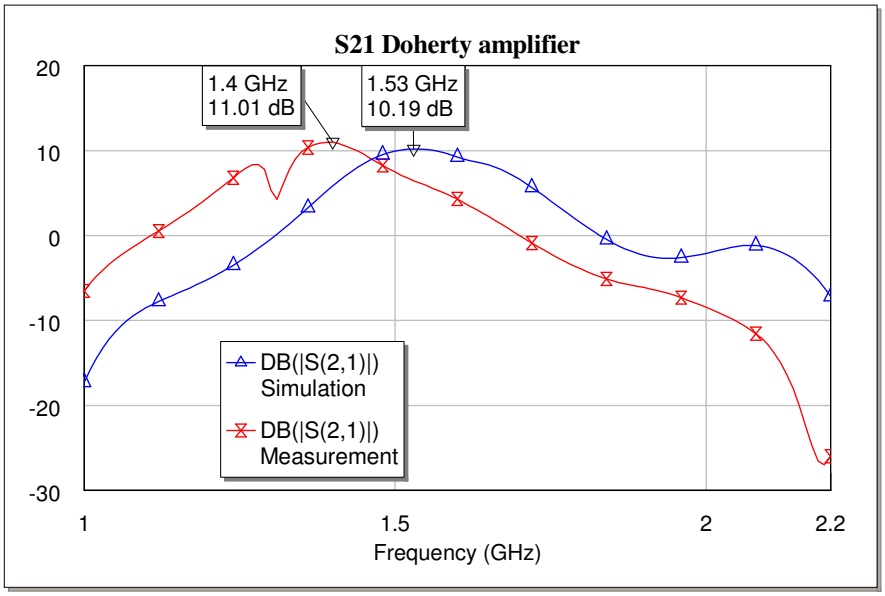


Figure 5.4.2 Simulated (Δ) and measured (□) S_{21} of the Doherty amplifier.

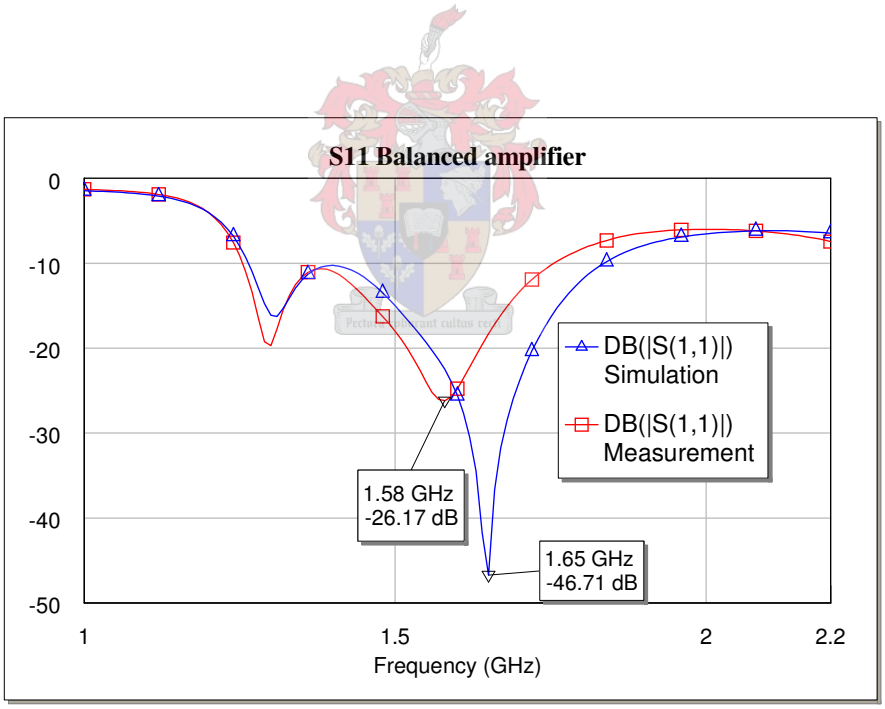


Figure 5.4.3 Simulated (Δ) and measured (□) S_{11} of the balanced amplifier.

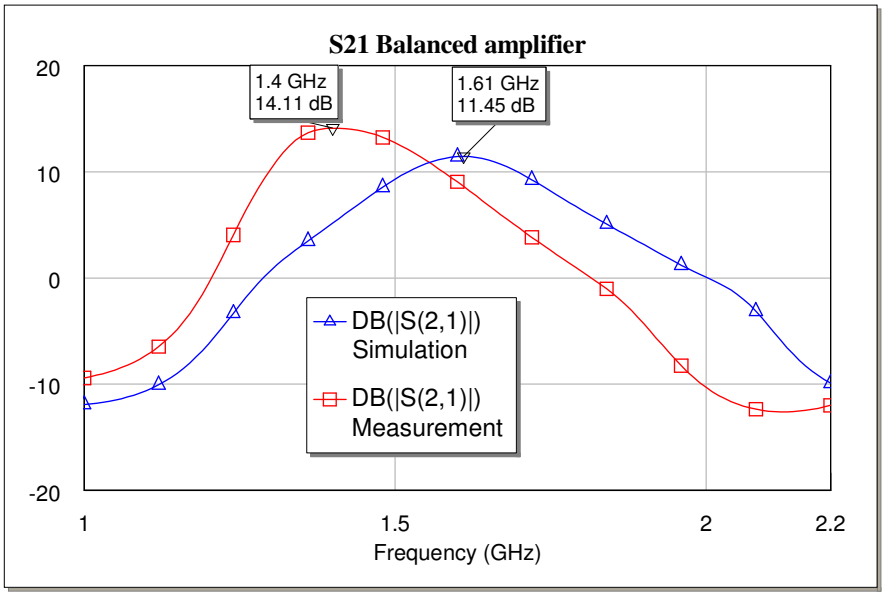


Figure 5.4.4 Simulated (Δ) and measured (□) S_{21} of the balanced amplifier.

This difference can be attributed to various uncertainties, such as the fact that the models used for the capacitors are extracted by the manufacturer using a different substrate. The effect of the substrate on a capacitor's response is described in [27]. It is unclear if the effect of the layout footprints supplied by the capacitors' manufacturer is incorporated in the models of the capacitor. In addition, no RF models for the resistors used in the designs could be obtained. In spite of the difference, the results are good enough for a first iteration design and any further measurements will be done at 1.4 GHz.

5.4.2 Measurement Results Compared to Literature

The first measurements are done at the designed bias points. The peaking amplifier gate voltage being V_{GSP} = 1.9V. The carrier amplifier gate voltage and the gate voltages for the two transistors in the balanced amplifier are adjusted until a quiescent drain current of I_{DSQ} = 350 mA is measured. For the sake of clarity the peaking amplifier gate voltage and the carrier amplifier quiescent drain current is provided in the figure captions. The quiescent drain current of the two transistors in the balanced amplifier will always be the same as the quiescent drain current of the carrier amplifier in the Doherty amplifier, when compared against each other.

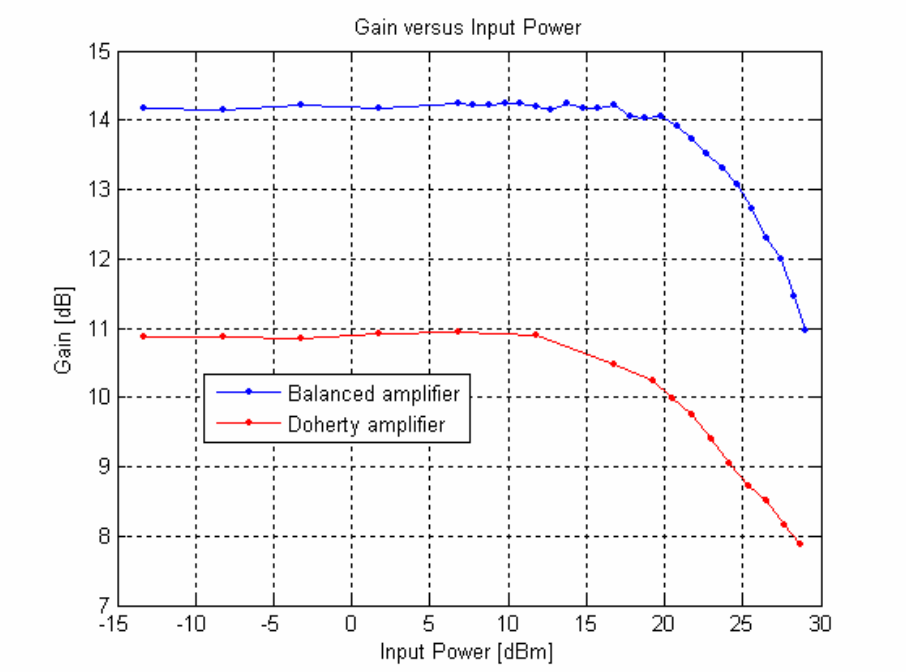


Figure 5.4.5 Measured gain for the balanced amplifier and Doherty amplifier with I_{DSQ} = 350 mA and V_{GSP} = 1.9 V.

Figure 5.4.5 shows the measured gain of the Doherty and balanced amplifier. The balanced amplifier has a small-signal gain of 14.2 dB whereas the Doherty amplifier has a small-signal gain of 10.9 dB. Figure 5.4.6, which shows the measured compression for the two amplifiers indicate that the Doherty amplifier reaches its 1 dB compression point at 20.93 dBm input power, which is 3.17 dBm less than the value at which the balanced amplifier reaches compression.

The peak envelope power (PEP) was expected to be at approximately 22 dBm input power. The measured input power at the balanced amplifiers 1 dBm compression point is 24.1 dBm. Since a 3 dB power divider is used at the input of the balanced amplifier the power reaching each of the two class AB amplifier of which the balanced amplifier comprises is 21.1 dBm input power. The predicted maximum input power for the 10W amplifiers is therefore much more accurate than for the small-signal amplifiers in Chapter 4.

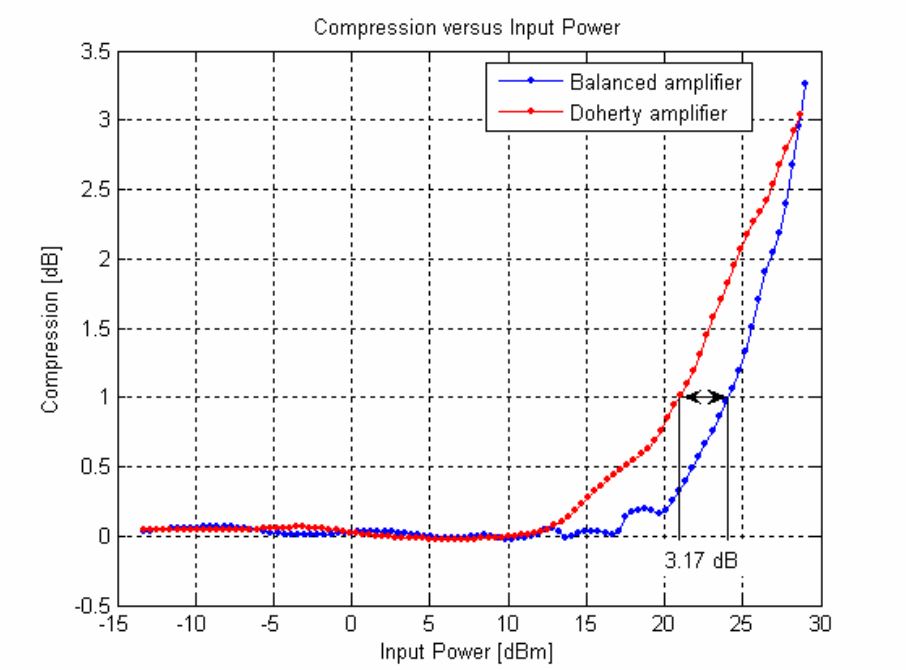


Figure 5.4.6 Measured compression for the balanced and Doherty amplifier with I_{DSQ} = 350 mA and V_{GSP} = 1.9 V.

Figure 5.4.7 shows the DC current components of the balanced and Doherty amplifiers. Although the carrier and balanced amplifiers has the same quiescent current, the carrier amplifier's drain current starts increasing before the two amplifiers of the balanced amplifier. The peaking amplifier is not conducting at this point and can therefore not have an influence. The load-line the amplifier sees when the peaking amplifier is not conducting should have a limiting effect on the DC current. (See discussion of the effect of the load-line on DC current, gain and compression in Section 4.4.1).

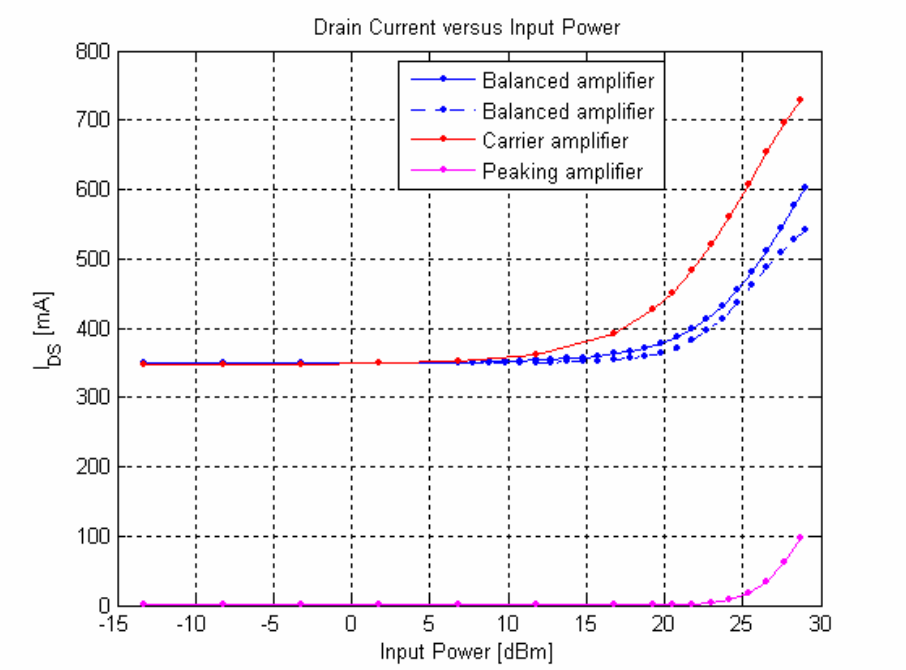


Figure 5.4.7 Measured drain current for the balanced and Doherty amplifier with I_{DSQ} = 350 mA and V_{GSP} = 1.9 V.

Figure 5.4.8 shows the drain efficiency for the balanced and Doherty amplifiers against backed-off output power. It can be seen that the balanced amplifier is much more efficient than the Doherty amplifier. This is because of the Doherty amplifiers lower gain, the carrier amplifier's unexpected high DC current and the peaking amplifier which switches on to late.

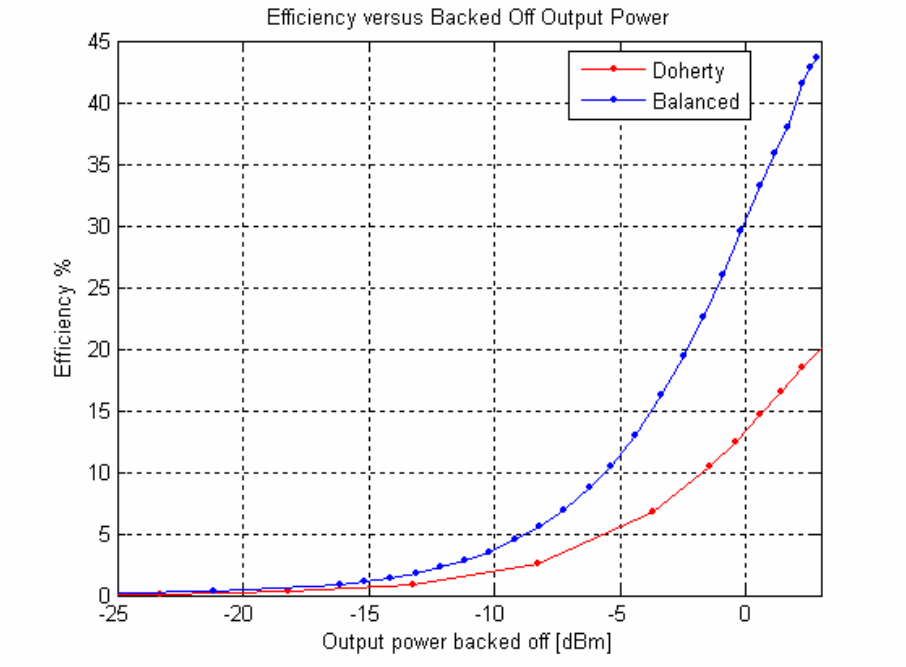


Figure 5.4.8 Measured drain efficiency versus backed-off output power for the balanced amplifier and Doherty amplifier with I_{DSQ} = 350 mA and V_{GSP} = 1.9 V.

In Section 4.4.4 it was found that the peaking amplifier gate voltage, V_{GSP}, had to be adjusted to achieve the highest efficiency. The peaking amplifier gate voltage was therefore adjusted until the best efficiency was measured. The best efficiency was measured with V_{GSP} = 3.6V. This increased the gain of the Doherty amplifier to 11.7 dB and input power at the 1 dB compression point increased to 25.5 dBm. The peaking amplifier has a quiescent drain current of 10 mA which means it is not biased in class C mode anymore, but in a slight class AB mode. The drain efficiency curve in Figure 5.4.9 shows that this higher peaking amplifier gate voltage increased the Doherty amplifier's drain efficiency at its peak envelope power (PEP) with 13 %. However, this is still less efficient than the balanced amplifier. At 6 dB backed-off power the Doherty amplifier with V_{GSP} = 3.6V is 2.9 % more efficient than the balanced amplifier.

This confirms that the peaking amplifier gate voltage, V_{GSP} is one of the most critical parameters to achieve the maximum efficiency in a Doherty amplifier design [20]. However these results are not satisfactory and the drain bias for the carrier amplifier and the two amplifiers of the balanced amplifier are now also adjusted to illustrate a more significant difference between the Doherty and balanced amplifier.

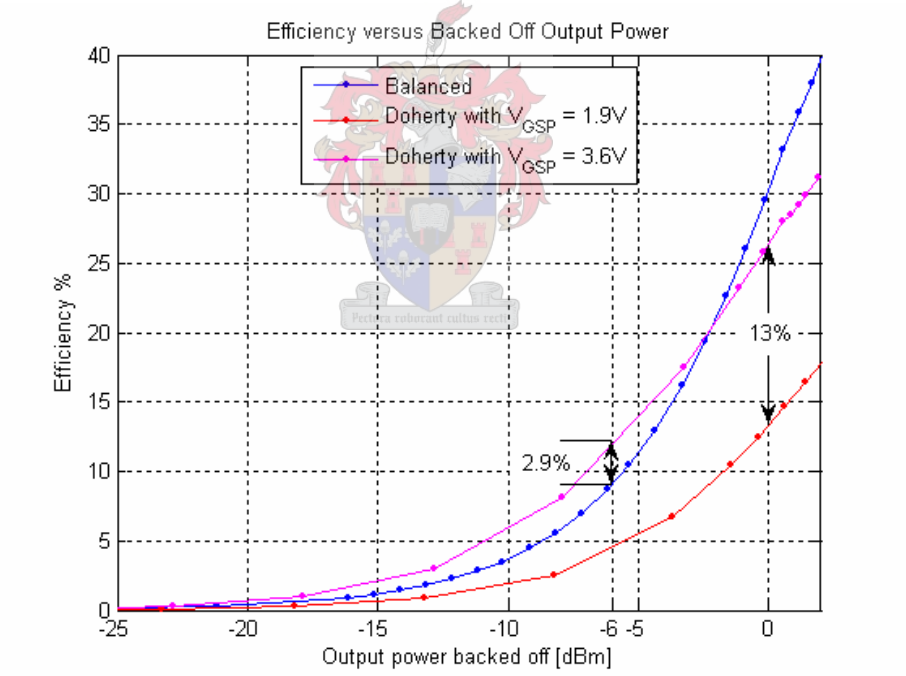


Figure 5.4.9 Measured drain efficiency versus backed-off output power for the balanced amplifier and Doherty amplifier with I_{DSQ} = 350 mA, V_{GSP} = 1.9 V and V_{GSP} = 3.6V.

The best results are achieved with the carrier and balanced amplifier still biased in class AB mode, but with a lower quiescent drain current of I_{DSQ} = 170 mA. The gain for the balanced and Doherty amplifier is shown in Figure 5.4.10 and the output power versus input power is shown in Figure 5.4.11. The small-signal gain for the balanced amplifier is 13.72 dB, whereas the Doherty amplifier has a gain of 9.91 dB. 40 dBm output power is achieved for the balanced amplifier, but the

compression curve in Figure 5.4.12 shows that it has already reached its 3 dB compression point at this stage. The 1 dB compression point is of more importance and the Doherty amplifier's 1 dB compression point occurs at 28.5 dBm input power which is 6.5 dBm higher than for the balanced amplifier. Looking at the compression versus output power in Figure 5.4.13, the Doherty amplifier's 1 dB compression point is increased by almost 3 dBm to 37.4 dBm (5.5W) output power.

With a peaking amplifier gate voltage of V_{GSP} = 3V, the peaking amplifier is no longer biased in class C but class B mode with a quiescent drain current of 1.4 mA. Figure 5.4.14 shows the measured DC currents for the balanced and Doherty amplifiers.

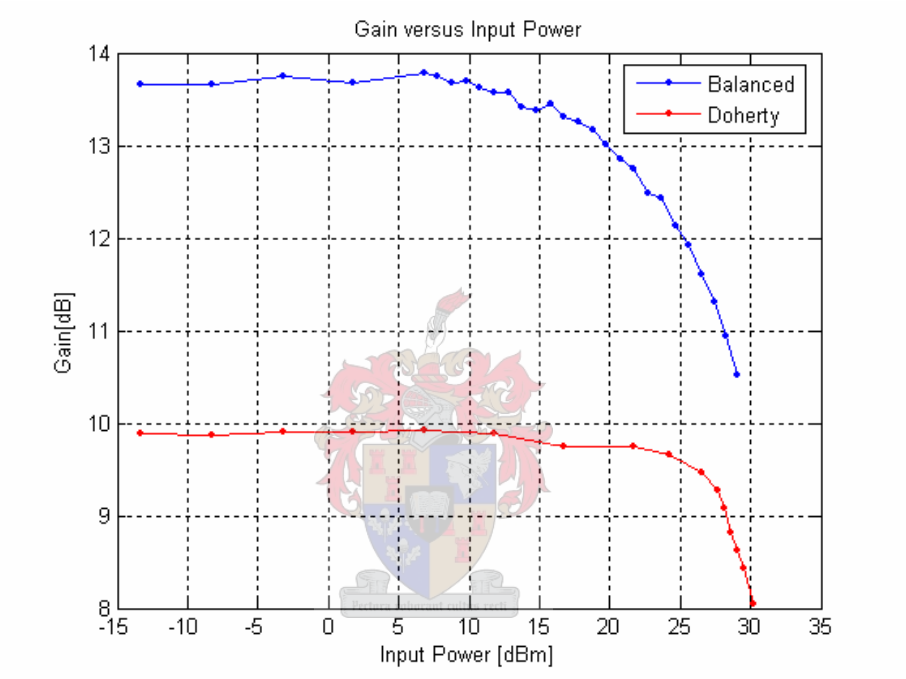


Figure 5.4.10 Measured gain for the balanced amplifier and Doherty amplifier with I_{DSQ} = 170 mA and V_{GSP} = 3 V.

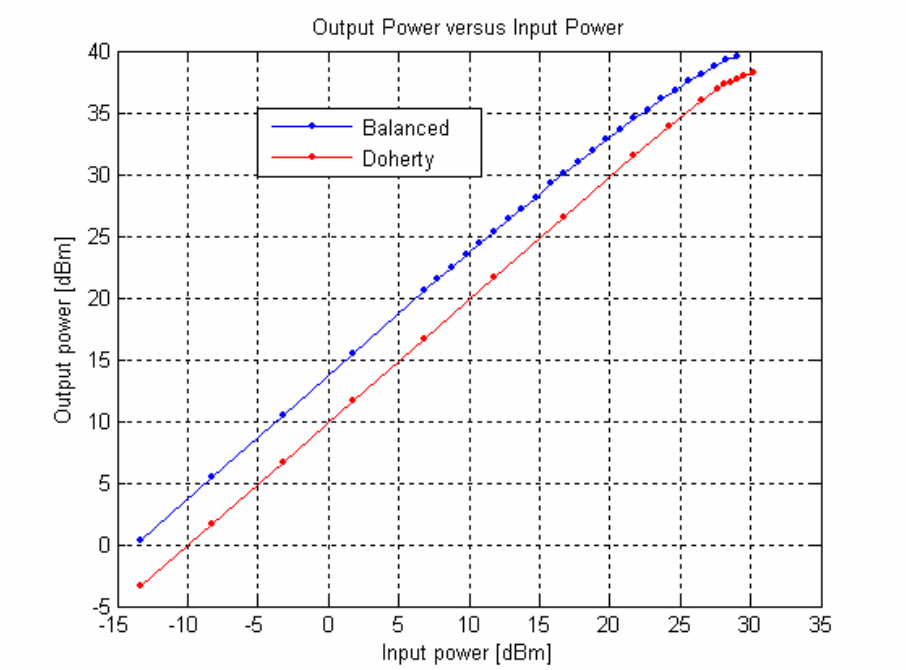


Figure 5.4.11 Measured output power versus input power for the balanced amplifier and Doherty amplifiers with I_{DSQ} = 170 mA and V_{GSP} = 3 V.

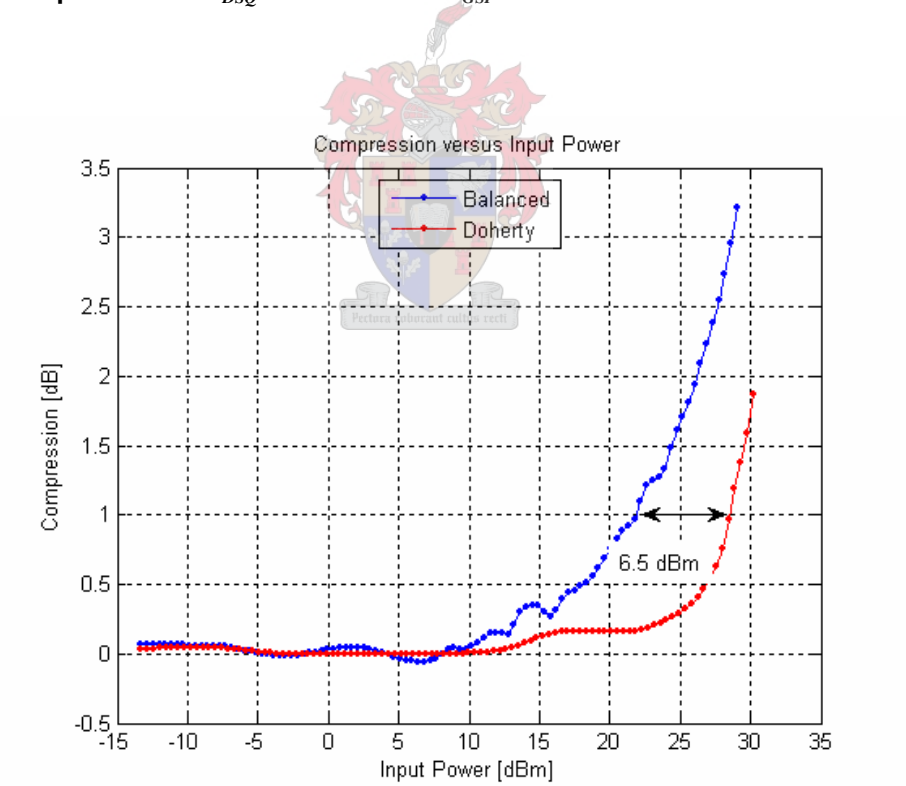


Figure 5.4.12 Measured compression versus input power for the balanced amplifier and Doherty amplifier with I_{DSQ} = 170 mA and V_{GSP} = 3V.

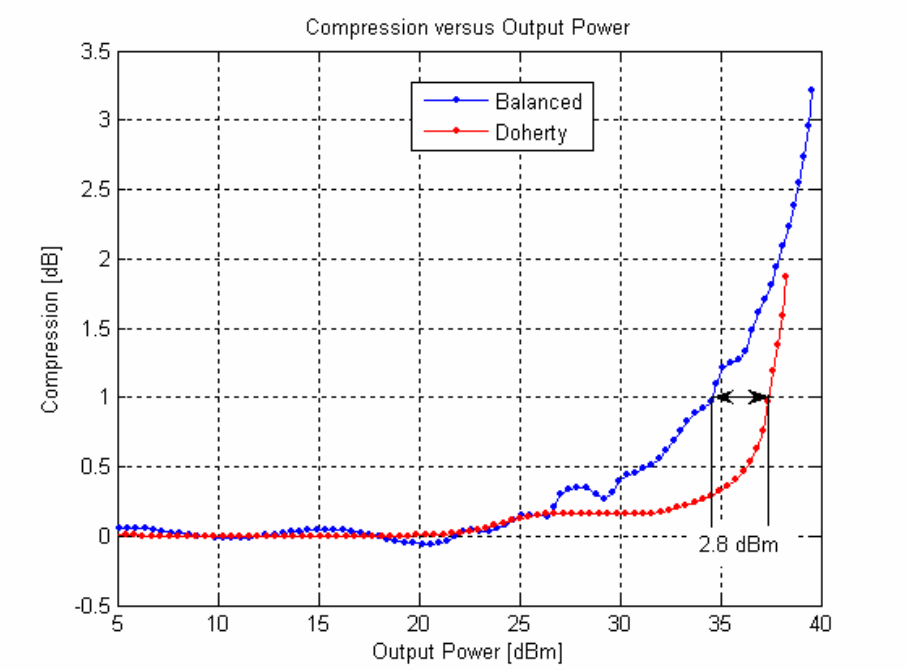


Figure 5.4.13 Measured compression versus output power for the balanced amplifier and Doherty amplifier with I_{DSQ} = 170 mA and V_{GSP} = 3V.

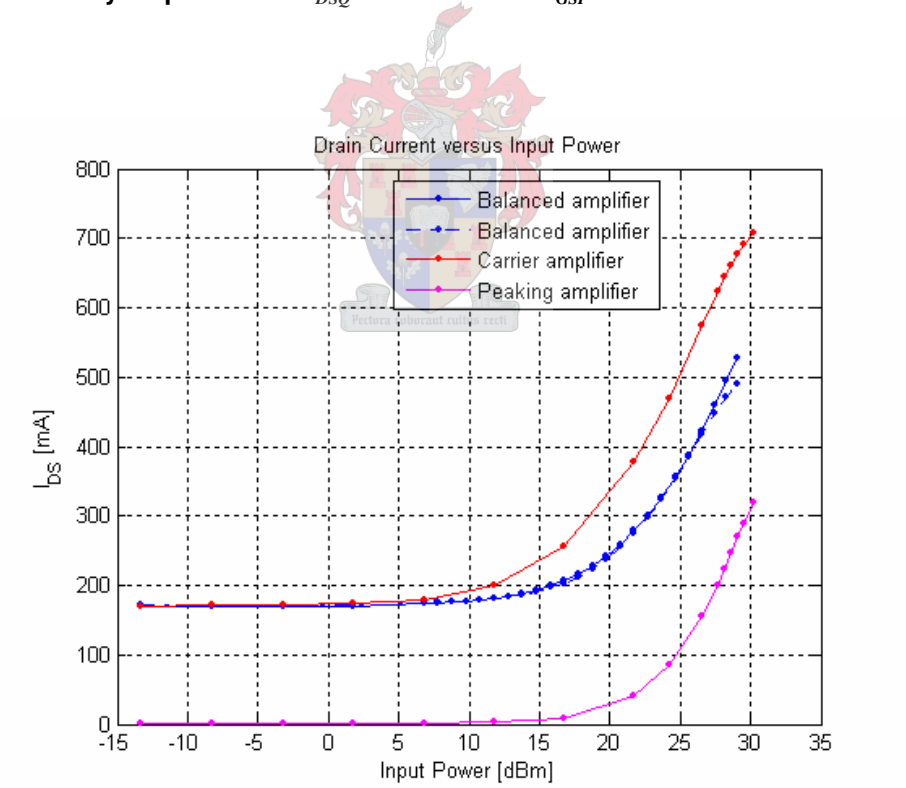


Figure 5.4.14 Measured drain current for the balanced and Doherty amplifiers with I_{DSQ} = 170 mA and V_{GSP} = 3 V.

Figure 5.4.15 and Figure 5.4.16 respectively show the drain efficiency and power added efficiency for the balanced and Doherty amplifier against backed-off output power. The Doherty amplifier has an increase of 7.4 % drain efficiency and 6 % PAE to that of the balanced amplifier at 6 dB back-off.

At the peak output power (which is taken as the output power at 1 dB compression) the Doherty amplifier has an increase of 5.3 % drain efficiency and 2.3 % PAE to that of the balanced amplifier.

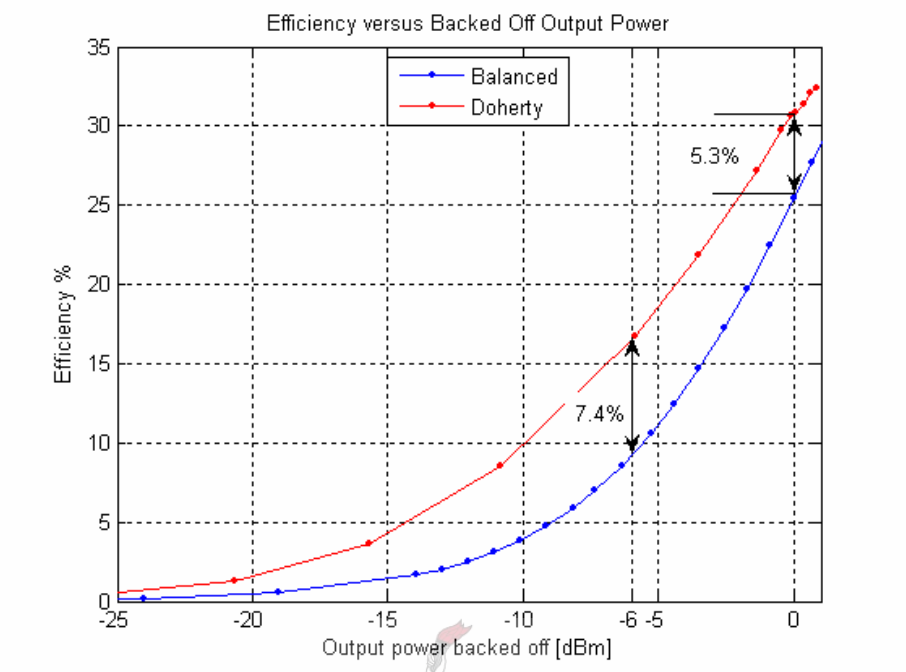


Figure 5.4.15 Measured drain efficiency versus backed-off output power for the balanced amplifier and Doherty amplifier with I_{DSQ} = 170 mA and V_{GSP} = 3 V.

The PAE curve is shown to compare it to existing literature. Figure 5.4.17 show results from [20] which achieved an increase of 10 % in PAE at 6 dB back-off with their Doherty amplifier. This increase is almost twice as much as that shown in Figure 5.4.16. [20], however had the benefit of being able to optimise the peaking amplifier's compensation line and gate voltage, V_{GSP}, in simulation and during measurements. This means that they had access to a reliable large signal model for the transistor used.

Figure 5.4.18 shows a comparison from [28] between a single-ended, balanced and Doherty amplifier. At 6 dB back-off an increase of approximately 6.2 % in PAE is measured. This is basically the same increase measured in Figure 5.4.16.

Figure 5.4.19 shows a comparison from [15] between a single-ended and an extended Doherty amplifier. At 8 dB back-off the extended Doherty amplifier shows an improvement in PAE of 25% to the single-ended amplifier. Results of other methods can be found in [13], [14] and [16].

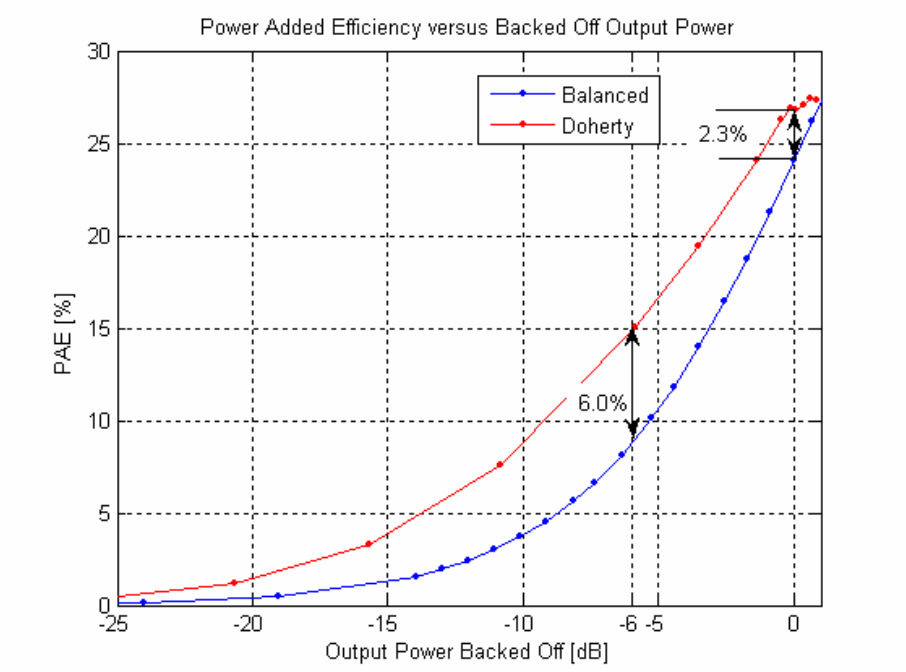


Figure 5.4.16 Measured power added efficiency versus backed-off output power for the balanced amplifier and Doherty amplifier with I_{DSQ} = 170 mA and V_{GSP} = 3 V.

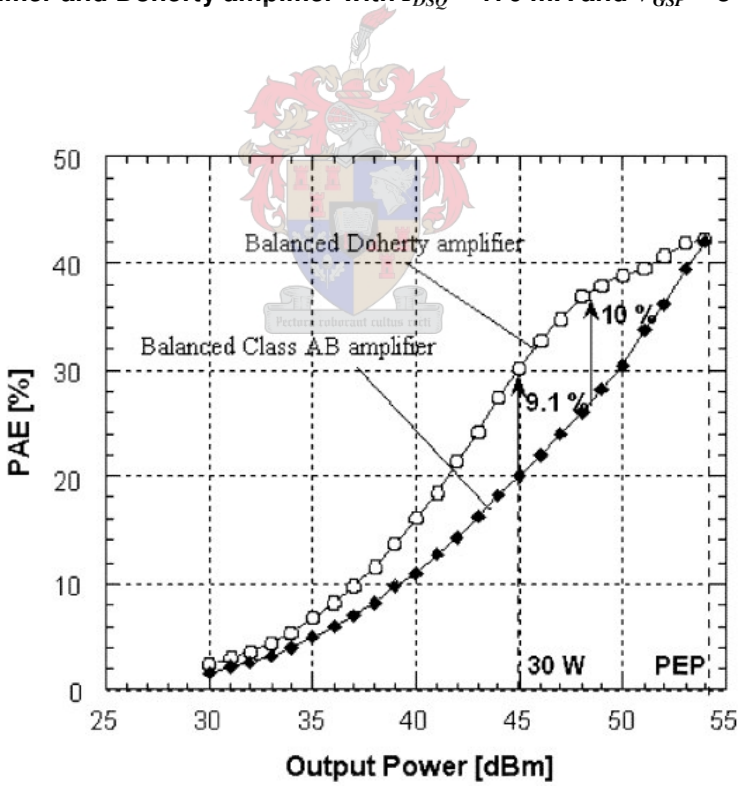


Figure 5.4.17 Measured PAE of a balanced class AB amplifier and Doherty amplifier. (after [20])

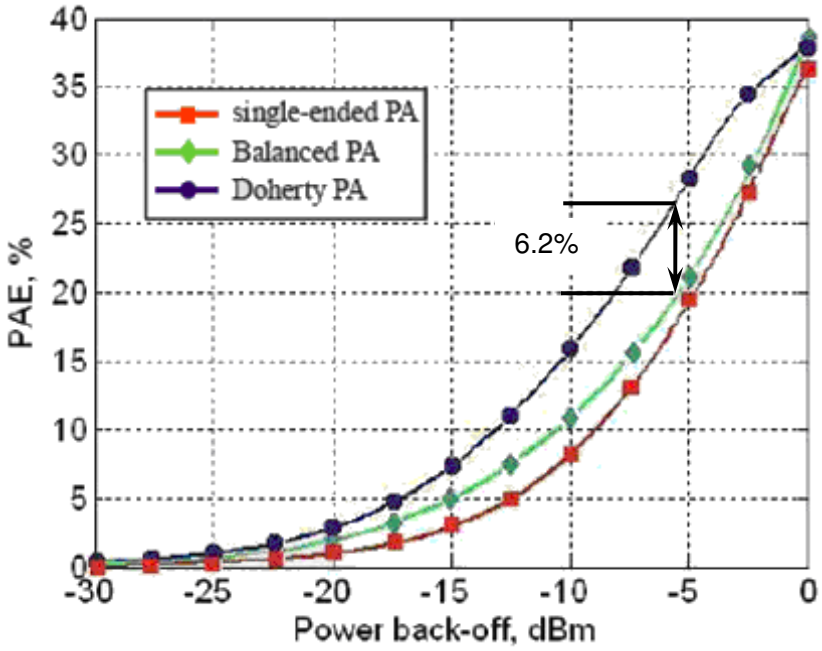


Figure 5.4.18 Measured PAE versus backed-off power for a single-ended, balanced and Doherty amplifier. (after [28])

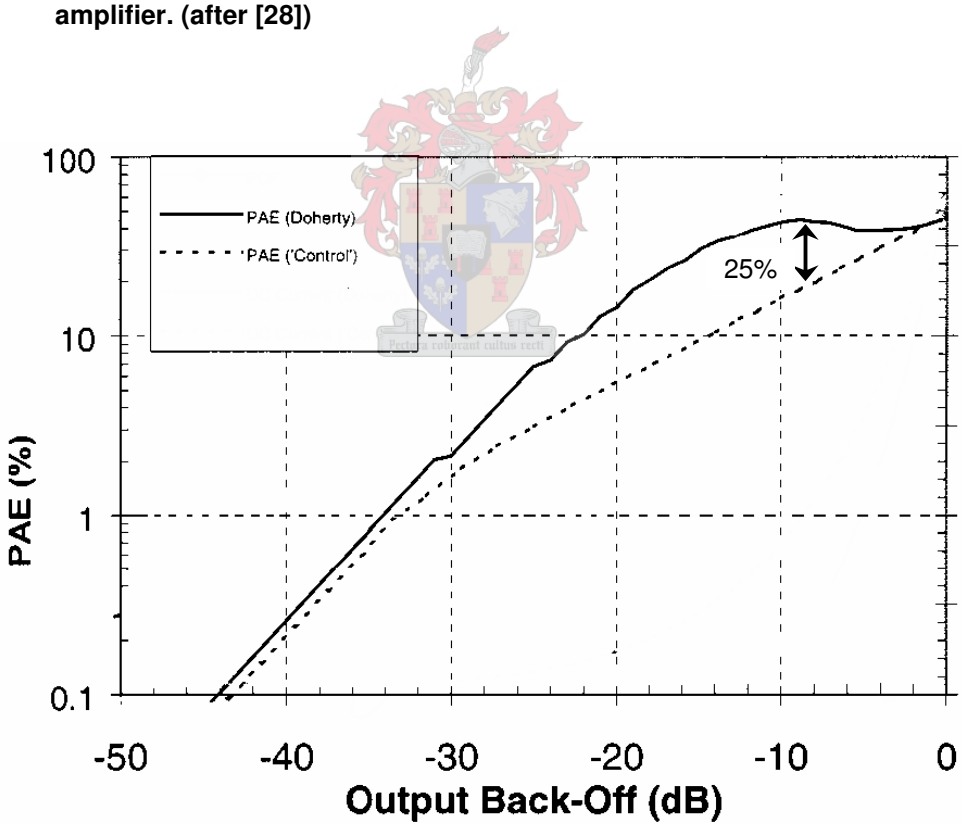


Figure 5.4.19 Measured PAE versus backed-off power for a single-ended and a extended Doherty amplifier. (after [15])

5.5 Conclusions

A Doherty power amplifier is designed using 10W Freescale MRF282 LDMOS transistors. The designed amplifier consists of a carrier amplifier operating in class AB mode and a peaking amplifier

operating in class C mode. A balanced amplifier, consisting of two carrier amplifiers in parallel is also designed.

The amplifiers are designed at their expected peak envelope power (the output power at the amplifier's 1 dB compression point). The same design process is followed as the one in Chapter 4 for the small-signal Doherty amplifier. The only difference is that the quarter-wave impedance inverter and offset line at the carrier amplifier's output are combined as one transmission line, after which the combined length is optimised.

Both the Doherty and balanced amplifiers' small-signal simulations are verified with small-signal measurements done on a linear network analyser. The measurements are frequency shifted by approximately 200 MHz in relation to one another, which can be attributed to various factors.

The measurement setup and software used to measure output power versus input power, gain, compression and efficiency is the same as that used to measure the small-signal amplifiers. The setup for the power amplifiers require an extra driver amplifier to drive the Doherty and balanced amplifiers into compression. A circulator is needed to protect the driver amplifier and a filter to get rid of any unwanted harmonics from the driver amplifier. An attenuator is also included to protect the spectrum analyser. Although this is a great deal of extra equipment included in the setup, their effects are simply incorporated in the error matrices and therefore the setup is basically the same as that used for the small-signal amplifiers.

The prediction of the input power at the balanced 1 dB compression point is much more accurate than for the small-signal amplifier in Chapter 4.

The measurements of the Doherty amplifier, at the designed biasing point, do not yield good results, and the Doherty amplifier is less efficient than the balanced amplifier. The reason is believed to be tolerances in the threshold voltage and gain of the LDMOS transistors. The carrier amplifier has a much higher DC current than the two amplifiers of the balanced amplifier, even when the peaking amplifier is not conducting. The peaking amplifier also starts to conduct at a higher input power than expected. The peaking amplifier gate voltage is therefore adjusted to a higher voltage to lower the input power at which the peaking amplifier starts to conduct. This raises the drain efficiency of the Doherty amplifier with between 7% and 13% in the upper 6 dB output power range, but the Doherty amplifier is still less efficient than the balanced amplifier in the upper 3 dB output power.

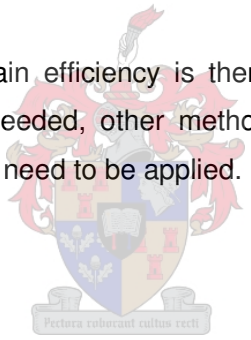
Statements made in existing literature [20] regarding the fine tuning of the peaking amplifier gate voltage to achieve peak efficiency are thus confirmed.

The carrier amplifier gate voltage is also varied to get a suitable comparison between the efficiencies of the Doherty and balanced amplifier. The best results are obtained with the carrier and balanced amplifiers' gate voltages adjusted to yield a quiescent drain current of I_{DSQ} = 170 mA and a peaking amplifier gate voltage of V_{GSP} = 3 V. Compared to the balanced amplifier, this gives an increase in drain efficiency of 5.3% and 7.4% at peak output power and 6 dB back-off, respectively, and an increase in PAE of 2.3% and 6% respectively.

Two results of similar Doherty amplifiers from the literature ([20], [28]) are shown and these gave 6.2% to 10% increase in PAE at 6 dB back-off. The results of the amplifier designed in this thesis thus shows similar results and it can be concluded that the design procedure used is successful for designing a Doherty amplifier with higher efficiency than a balanced amplifier with the same biasing as the carrier amplifier.

A comparison from literature between a single-ended and extended Doherty amplifier is also shown. The extended Doherty amplifier shows an improvement of 25% PAE to the single-ended amplifier at 8 dB back-off.

Limited improvement in PAE and drain efficiency is therefore possible with a Classical Doherty amplifier. If further improvement is needed, other methods such as the extended configuration, uneven power drive or bias adaptation need to be applied.



Chapter 6

Conclusions and Recommendations

6.1 Conclusions

The objective of this thesis is the investigation of the operation of a Doherty amplifier by combining the work in existing literature in one design procedure for a Classical Doherty amplifier.

Initially, the advantages of a load-line match in a power amplifier design are presented. The resistance value for the load-line is successfully calculated using MATLAB code. The code uses the measured IV-curves of a transistor as a transfer function to calculate the fundamental component of the output current for a certain gate bias and input signal.

An optimisation algorithm written in MATLAB is implemented to determine the impedance a transistor should see to ensure that the calculated load-line resistance is presented to the internal current source of the transistor.

Following discussions on ideal Doherty amplifier theory, an investigation of practical considerations during the design as well as construction of a practical amplifier in Chapter 2 and Chapter 3, two separate Doherty amplifiers are designed.

Firstly, in Chapter 4, a Classical Doherty amplifier is designed using a small-signal transistor. The design is done at the expected 1 dB compression point. To do this, S-parameters for the transistor at an equivalent gate voltage are used. The equivalent gate voltage is determined by calculating the DC current component at the expected 1 dB compression point and taking the corresponding gate voltage on the measured IV-curve. The main reason for using S-parameters at an equivalent gate

voltage is to predict the phase response of the carrier and peaking amplifiers to ensure relatively flat phase responses. In this way, sufficient compensation can be made for in-phase output signals. The rest of the design makes use of the extra offset lines at the outputs of the carrier and peaking amplifiers to enhance load modulation and to increase the output impedance of the peaking amplifier. These amplifiers are manufactured in such a way that measurements can be made on either the carrier or peaking amplifiers separately, or in Doherty configuration. A balanced amplifier, which consists of two carrier amplifiers in parallel, is also manufactured. The balanced amplifier serves as a benchmark to determine the Doherty amplifier's performance.

The transistor (CFY30) used in the manufactured amplifiers is characterised on a non-linear network analyser. These measurements are used to verify the predicted phase response of the transistor. The predicted phase response is illustrated to be accurate within 10°.

A custom measurement setup with calibration software is developed to measure the manufactured amplifiers' gain, output power, compression and efficiency curves. Measurements performed on the non-linear network analyser prove the accuracy of this measurement setup.

Load modulation is successfully illustrated on the carrier amplifier by manually changing the carrier amplifier's load resistance with discrete values.

In the Doherty configuration, the peaking amplifier gate voltage, V_{GSP}, has to be adjusted from the designed -1.9 V to -1.7 V to achieve maximum efficiency.

Although the peaking amplifier cannot deliver the same current amplitude as the carrier amplifier at the Doherty amplifier's 1 dB compression point (the 1 dB compression point is taken as the amplifier's peak output power), the Doherty amplifier shows an improvement of 6.6 % in drain efficiency when compared to the balanced amplifier at the peak output power.

After satisfactory results are achieved with the small-signal Doherty amplifier, the design procedure is used again in Chapter 5 to design a Doherty power amplifier using 10W transistors. A balanced amplifier is also manufactured along with the Doherty amplifier, for the purposes of comparative analysis. The peaking amplifier gate voltage, V_{GSP}, is adjusted from the designed 1.9V to 3V for optimal efficiency. Even though the peaking amplifier cannot supply the same amount of current as theory predicts, an improvement in performance to the balanced amplifier is measured. The 10W Doherty amplifier's 1 dB compression point is improved with 2.8 dBm output power. Improvements in drain efficiency of 5.3% and 7.4% at peak output power and 6 dB back-off are measured, respectively. In the same way, improvements in PAE of 2.3% and 6% at peak output power and 6 dB back-off are measured respectively.

The known drawbacks of a Classical Doherty amplifier include limited load modulation due to the utilisation of identical transistors for the peaking and carrier amplifiers. It can be concluded that, in spite of this, the use of additional output offset lines can still provide efficiency improvement when compared to a balanced amplifier. If further improvement in efficiency is needed, additional methods such as N-way or extended configurations, uneven power drive or bias adaptation can possibly be implemented.

6.2 Recommendations

It is stated in [20] that the peaking amplifier gate voltage and the additional offset lines are the most critical parameters in achieving maximum efficiency. In practice it is easy to adjust the gate voltage, but the same does not apply for the offset lines. To be able to adjust these two parameters during simulation, reliable large-signal models for the transistors are necessary.

Further research is needed to determine the effect of the value of R_o on the output matching sections, offset lines and consequent load modulation.

It is widely known that the peaking amplifier in a Classical Doherty amplifier cannot reach the same fundamental current amplitude as the carrier amplifier. Even so, the equations ((3.16) - (3.18)) used to determine the relationship between the load resistance and the characteristic impedance of the output lines assume equal current amplitudes. It is worthwhile to look at the possibility of calculating the expected relationship between the fundamental current amplitudes for the carrier and peaking amplifiers, and then calculating separate characteristic impedances for the carrier and peaking amplifiers' output lines.

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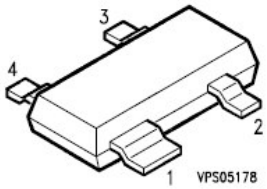
Appendix A

SIEMENS GaAs FET **CFY 30**

Datasheet

* Low noise (F_{min} = 1.4 dB @ 4 GHz)
* High gain (11.5 dB typ. @ 4 GHz)
* For oscillators up to 12 GHz
* For amplifiers up to 6 GHz
* Ion implanted planar structure
* Chip all gold metallization
* Chip nitride passivation



ESD: **E**lectro**s**tatic **d**ischarge sensitive device, observe handling precautions!

Type	Marking	Ordering code (tape and reel)	Pin Configuration 1	2	3	4	Package 1)
CFY 30	A2	Q62703-F97	S	D	S	G	SOT-143

Maximum ratings	Symbol	Value	Unit
Drain-source voltage	V_{DS}	5	V
Drain-gate voltage	V_{DG}	7	V
Gate-source voltage	V_{GS}	-4 ... +0.5	V
Drain current	I_D	80	mA
Channel temperature	T_{Ch}	150	°C
Storage temperature range	T_{stg}	-40...+150	°C
Total power dissipation (TS ≤ 70°C) 2)	P_{tot}	250	mW
Thermal resistance			
Channel-soldering point 2)	R_{thChS}	<320	K/W

1) Dimensions see chapter Package Outlines
2) T_s is measured on the source 1 lead at the soldering point to the PCB.

SIEMENS GaAs FET **CFY 30**

Electrical characteristics at T_A = 25°C, unless otherwise specified

Characteristics	Symbol	min	typ	max	Unit
Drain-source saturation current V_{DS} = 3.5 V, V_{GS} = 0 V	I_{DSS}	20	50	80	mA
Pinch-off voltage V_{DS} = 3.5 V I_D = 1 mA	$V_{GS(P)}$	-0.5	-1.3	-4.0	V
Transconductance V_{DS} = 3.5 V I_D = 15 mA	g_m	20	30	-	mS
Gate leakage current V_{DS} = 3.5 V I_D = 15 mA	I_G	-	0.1	2	µA
Noise figure V_{DS} = 3.5 V I_D = 15 mA f = 4 GHz f = 6 GHz	F	- -	1.4 2.0	1.6 -	dB
Associated gain V_{DS} = 3.5 V I_D = 15 mA f = 4 GHz f = 6 GHz	G_a	10 -	11.5 8.9	- -	dB
Maximum available gain V_{DS} = 3.5 V I_D = 15 mA f = 6 GHz	MAG	-	11.2	-	dB
Maximum stable gain V_{DS} = 3.5 V I_D = 15 mA f = 4 GHz	MSG	-	14.4	-	dB
Power output at 1 dB compression V_{DS} = 4 V I_D = 30 mA f = 6 GHz	$P_{1\,dB}$	-	16	-	dBm

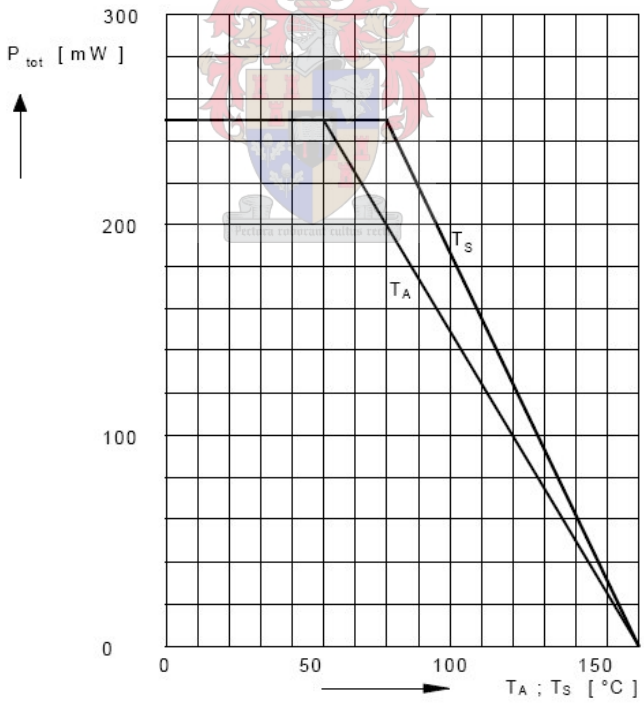
SIEMENS GaAs FET **CFY 30**

Typical Common Source Noise Parameters

I_D = 15 mA V_{DS} = 3.5 V Z_0 = 50 Ω

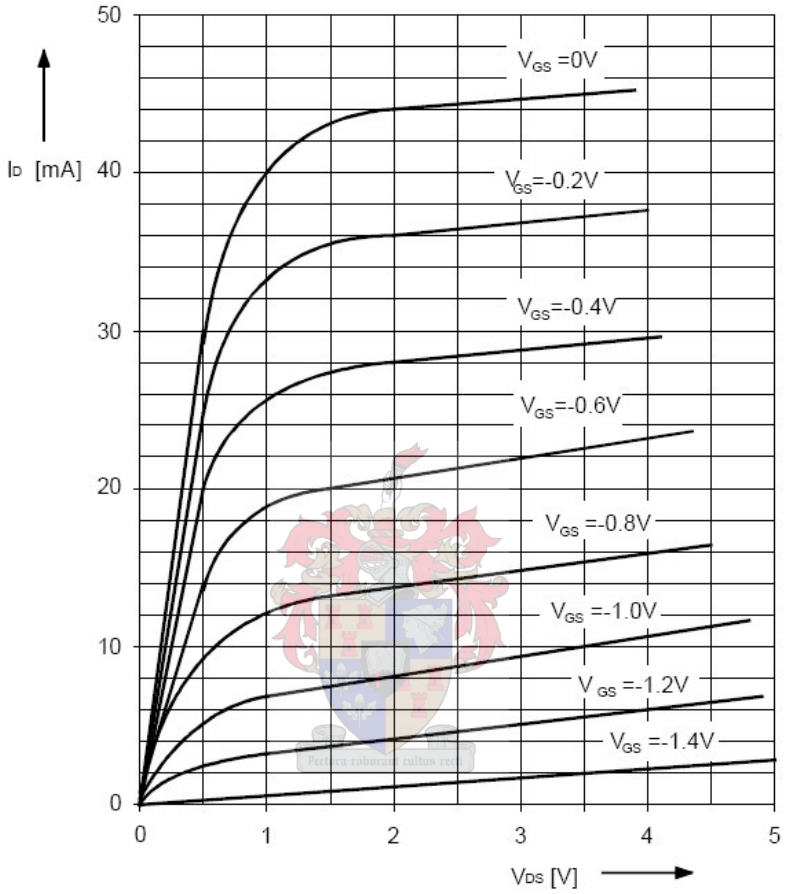
f	F_{min}	G_a	Γ_{opt}		R_n	N	$F_{50\Omega}$	$G(F_{50\,\Omega})$
GHz	dB	dB	MAG	ANG	Ω	-	dB	dB
2	1.0	15.5	0.72	27	49	0.17	2.9	10.0
4	1.4	11.5	0.64	61	29	0.17	2.7	9.3
6	2.0	8.9	0.46	101	19	0.30	2.8	7.5
8	2.5	7.1	0.31	153	9	0.31	2.8	6.4
10	3.0	5.8	0.34	-133	14	0.38	3.4	4.2
12	3.5	5.0	0.41	-93	28	0.42	4.1	2.9

Total Power Dissipation $P_{tot} = f(T_s;T_A)$



SIEMENS GaAs FET **CFY 30**

Output characteristics $I_D = f(V_{DS})$



SIEMENS GaAs FET **CFY 30**

Typical Common Source S-Parameters

I_D = 15 mA U_D = 3.5 V Z_0 = 50 Ω

f	S11		S21		S12		S22	
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
0.1	1.00	-1	2.43	178	0.003	87	0.70	-1
0.4	1.00	-6	2.43	171	0.010	23	0.69	-5
0.8	0.99	-14	2.43	162	0.020	78	0.68	-11
1.2	0.98	-21	2.43	154	0.030	72	0.67	-15
1.6	0.97	-28	2.44	145	0.040	66	0.66	-20
2.0	0.96	-36	2.45	137	0.050	60	0.65	-26
2.4	0.93	-44	2.47	129	0.058	55	0.64	-30
2.8	0.90	-53	2.49	120	0.066	50	0.62	-35
3.2	0.87	-62	2.50	111	0.074	45	0.60	-41
3.6	0.83	-72	2.50	102	0.082	39	0.57	-47
4.0	0.80	-82	2.50	93	0.090	32	0.54	-54
4.4	0.77	-92	2.51	83	0.097	25	0.50	-61
4.8	0.74	-104	2.49	73	0.103	18	0.46	-67
5.2	0.70	-115	2.45	64	0.108	12	0.43	-73
5.6	0.66	-127	2.41	54	0.112	6	0.40	-80
6.0	0.63	-139	2.36	45	0.114	0	0.36	-88
6.4	0.60	-150	2.30	37	0.115	-6	0.31	-98
6.8	0.57	-162	2.24	27	0.116	-11	0.27	-110
7.2	0.55	-174	2.19	17	0.116	-17	0.24	-122
7.6	0.54	172	2.14	8	0.116	-22	0.21	-137
8.0	0.53	160	2.08	-2	0.115	-27	0.19	-154
8.4	0.54	147	2.00	-11	0.113	-32	0.18	-173
8.8	0.55	135	1.92	-21	0.111	-37	0.18	171
9.2	0.56	124	1.83	-30	0.109	-42	0.19	155
9.6	0.57	114	1.72	-40	0.107	-46	0.21	141
10.0	0.58	106	1.61	-48	0.104	-50	0.23	128
10.4	0.59	98	1.51	-56	0.102	-53	0.26	118
10.8	0.60	91	1.42	-62	0.101	-56	0.29	108
11.2	0.61	85	1.35	-69	0.099	-58	0.32	100
11.6	0.62	79	1.30	-75	0.098	-60	0.34	93
12.0	0.62	74	1.25	-81	0.096	-63	0.36	85

SIEMENS GaAs FET **CFY 30**

Typical Common Source S-Parameters

I_D = 30 mA U_D = 3.5 V Z_0 = 50 Ω

f	S11		S21		S12		S22	
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
0.1	1.00	-2	3.23	178	0.002	85	0.71	-1
0.4	1.00	-8	3.21	171	0.009	79	0.70	-6
0.8	0.99	-16	3.19	162	0.017	73	0.69	-11
1.2	0.97	-24	3.18	153	0.025	70	0.67	-16
1.6	0.95	-32	3.17	143	0.034	65	0.66	-21
2.0	0.92	-40	3.17	135	0.042	61	0.65	-26
2.4	0.90	-48	3.17	127	0.051	56	0.63	-31
2.8	0.87	-58	3.17	119	0.059	50	0.61	-36
3.2	0.83	-68	3.16	109	0.067	45	0.58	-42
3.6	0.79	-79	3.12	99	0.073	40	0.55	-48
4.0	0.75	-91	3.08	88	0.079	34	0.52	-54
4.4	0.71	-102	3.04	78	0.084	28	0.50	-60
4.8	0.67	-114	3.00	68	0.089	21	0.47	-66
5.2	0.63	-126	2.95	58	0.092	15	0.43	-73
5.6	0.60	-138	2.87	49	0.094	10	0.38	-81
6.0	0.57	-150	2.77	40	0.096	4	0.34	-89
6.4	0.54	-162	2.68	31	0.097	-1	0.30	-99
6.8	0.52	-174	2.58	22	0.098	-6	0.27	-109
7.2	0.51	173	2.50	14	0.099	-11	0.24	-121
7.6	0.50	160	2.43	5	0.099	-16	0.21	-134
8.0	0.50	147	2.36	-4	0.099	-20	0.18	-148
8.4	0.51	135	2.26	-13	0.099	-24	0.16	-164
8.8	0.52	125	2.15	-22	0.099	-29	0.16	176
9.2	0.54	115	2.04	-30	0.099	-33	0.17	158
9.6	0.55	107	1.93	-39	0.099	-37	0.19	142
10.0	0.57	99	1.82	-47	0.099	-41	0.22	128
10.4	0.59	91	1.71	-54	0.100	-44	0.25	118
10.8	0.60	85	1.60	-62	0.101	-47	0.27	109
11.2	0.61	79	1.51	-69	0.102	-49	0.30	100
11.6	0.62	73	1.44	-75	0.103	-52	0.32	92
12.0	0.62	68	1.38	-82	0.104	-55	0.34	85

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SEMICONDUCTOR TECHNICAL DATA

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The RF Sub–Micron MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF282SR1
MRF282ZR1

Designed for Class A and Class AB PCN and PCS base station applications with frequencies up to 2600 MHz. Suitable for FM, TDMA, CDMA, and multicarrier amplifier applications.

- Specified Two–Tone Performance @ 2000 MHz, 26 Volts
  Output Power — 10 Watts PEP
  Power Gain — 10.5 dB
  Efficiency — 28%
  Intermodulation Distortion — –31 dBc
- Specified Single–Tone Performance @ 2000 MHz, 26 Volts
  Output Power — 10 Watts CW
  Power Gain — 9.5 dB
  Efficiency — 35%
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 2000 MHz, 10 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R1 Suffix = 500 Units per 12 mm, 7 inch Reel.

2000 MHz, 10 W, 26 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETs

CASE 458B–03, STYLE 1
(NI–200S)
(MRF282SR1)

CASE 458C–03, STYLE 1
(NI–200Z)
(MRF282ZR1)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	60 0.34	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.2	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 10 µAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0)	I_{DSS}	—	—	1.0	µAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1.0	µAdc

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 12

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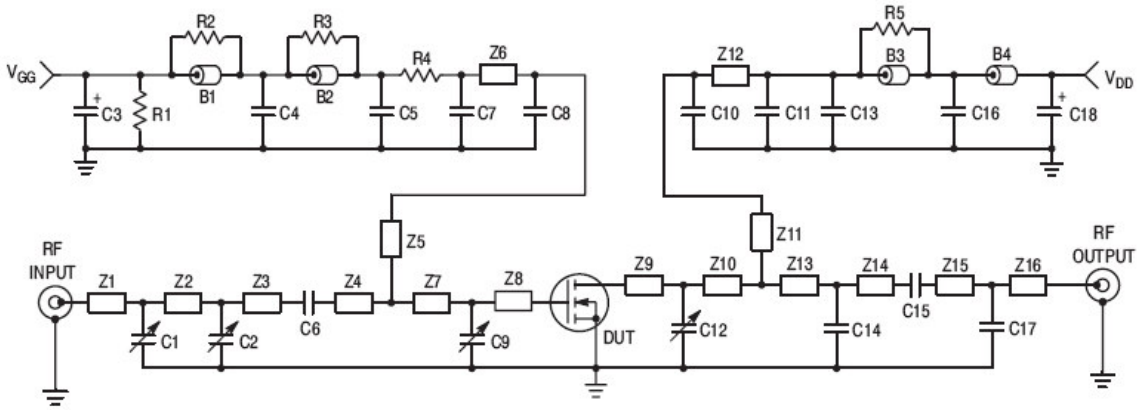
ELECTRICAL CHARACTERISTICS continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 50 µAdc)	$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 0.5 Adc)	$V_{DS(on)}$	—	0.4	0.6	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 75 mAdc)	$V_{GS(q)}$	3.0	4.0	5.0	Vdc
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	15	—	pF
Output Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	8.0	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	0.45	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Power Gain (V_{DD} = 26 Vdc, P_{out} = 10 W PEP, I_{DQ} = 75 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	G_{ps}	10.5	11.5	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 10 W PEP, I_{DQ} = 75 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	η	28	—	—	%
Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 10 W PEP, I_{DQ} = 75 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	IMD	—	–31	–28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 10 W PEP, I_{DQ} = 75 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz)	IRL	—	–14	–9	dB
Common–Source Power Gain (V_{DD} = 26 Vdc, P_{out} = 10 W PEP, I_{DQ} = 75 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	G_{ps}	10.5	11.5	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 10 W PEP, I_{DQ} = 75 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	η	28	—	—	%
Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 10 W PEP, I_{DQ} = 75 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	IMD	—	–31	–28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 10 W PEP, I_{DQ} = 75 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz)	IRL	—	–14	–9	dB
Common–Source Power Gain (V_{DD} = 26 Vdc, P_{out} = 10 W CW, I_{DQ} = 75 mA, f = 2000.0 MHz)	G_{ps}	9.5	11.5	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 10 W CW, I_{DQ} = 75 mA, f = 2000.0 MHz)	η	35	40	—	%
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 10 W CW, I_{DQ} = 75 mA, f1 = 2000.0 MHz, f2 = 2000.1 MHz, Load VSWR = 10:1, All Phase Angles at Frequency of Test)	Ψ	No Degradation In Output Power			



Z1	0.491″ x 0.080″ Microstrip	Z11	0.636″ x 0.055″ Microstrip
Z2	0.253″ x 0.080″ Microstrip	Z12	0.303″ x 0.055″ Microstrip
Z3	0.632″ x 0.080″ Microstrip	Z13	0.463″ x 0.080″ Microstrip
Z4	0.567″ x 0.080″ Microstrip	Z14	0.105″ x 0.080″ Microstrip
Z5	1.139″ x 0.055″ Microstrip	Z15	0.452″ ± 0.085″ x 0.080″ Microstrip
Z6	0.236″ x 0.055″ Microstrip	Z16	0.910″ ± 0.085″ x 0.080″ Microstrip
Z7	0.180″ x 0.325″ Microstrip	Raw Board Material	0.030″ Glass Teflon®, 2 oz Copper, 3″ x 5″ Dimensions, Arlon GX0300–55–22, ε_r = 2.55
Z8	0.301″ x 0.325″ Microstrip		
Z9	0.439″ x 0.325″ Microstrip		
Z10	0.055″ x 0.325″ Microstrip		

Figure 1. 1.93 – 2.0 GHz Broadband Test Circuit Schematic

Table 1. 1.93 – 2.0 GHz Broadband Test Circuit Component Designations and Values

Designators	Description
B1, B4	Surface Mount Ferrite Beads, 0.120″ x 0.333″ x 0.100″, Fair Rite #2743019446
B2, B3	Surface Mount Ferrite Beads, 0.120″ x 0.170″ x 0.100″, Fair Rite #2743029446
C1, C2, C9	0.8–8.0 pF Variable Capacitors, Johanson Gigatrim #27291SL
C3	10 μF, 35 V Tantalum Surface Mount Chip Capacitor, Kemet #T495X106K035AS4394
C4, C5, C13, C16	0.1 μF Chip Capacitors, Kemet #CDR33BX104AKWS
C6	200 pF Chip Capacitor, B Case, ATC #100B201JCA500X
C7	18 pF Chip Capacitor, B Case, ATC #100B180KP500X
C8	39 pF Chip Capacitor, B Case, ATC #100B390JCA500X
C10	27 pF Chip Capacitor, B Case, ATC #100B270JCA500X
C11	1.2 pF Chip Capacitor, B Case, ATC #100B1R2CCA500X
C12	0.6–4.5 pF Variable Capacitor, Johanson Gigatrim #27271SL
C14	0.5 pF Chip Capacitor, B Case, ATC #100B0R5BCA500X
C15	15 pF Chip Capacitor, B Case, ATC #100B150JCA500X
C17	0.1 pF Chip Capacitor, B Case, ATC #100B0R1BCA500X
C18	22 μF, 35 V Tantalum Surface Mount Chip Capacitor, Kemet #T491X226K035AS4394
R1	560 kΩ, 1/4 W Chip Resistor, 0.08″ x 0.13″
R2, R5	12 Ω, 1/4 W Chip Resistors, 0.08″ x 0.13″, Garrett Instruments #RM73B2B120JT
R3, R4	91 Ω, 1/4 W Chip Resistors, 0.08″ x 0.13″, Garrett Instruments #RM73B2B910JT
WS1, WS2	Beryllium Copper Wear Blocks 0.010″ x 0.235″ x 0.135″ NOM
	Brass Banana Jack and Nut
	Red Banana Jack and Nut
	Green Banana Jack and Nut
	Type "N" Jack Connectors, Omni–Spectra # 3052–1648–10
	4–40 Ph Head Screws, 0.125″ Long
	4–40 Ph Head Screws, 0.188″ Long
	4–40 Ph Head Screws, 0.312″ Long
	4–40 Ph Rec. Hd. Screws, 0.438″ Long
RF Circuit Board	3″ x 5″ Copper Clad PCB, Glass Teflon®

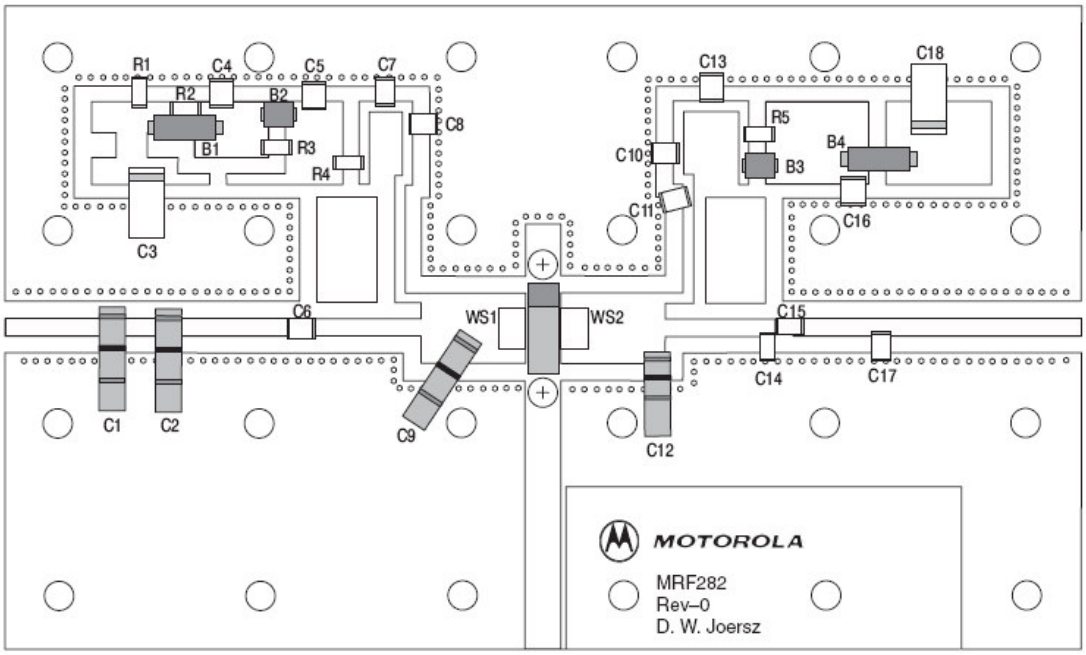


Figure 2. 1.93–2.0 GHz Broadband Test Circuit Component Layout

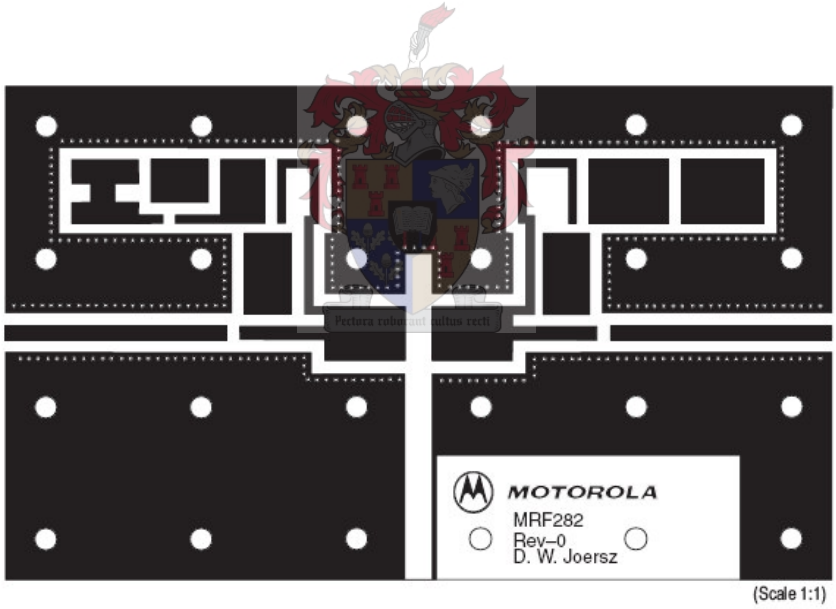
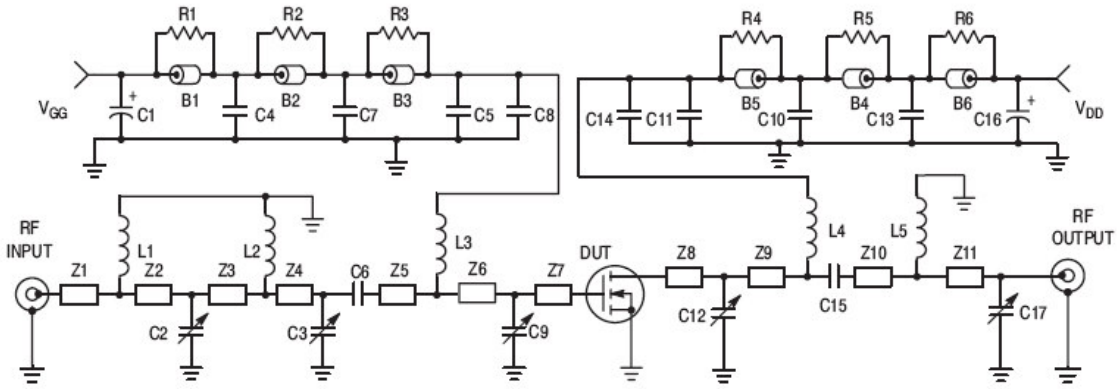


Figure 3. MRF282 Test Circuit Photomaster
(Reduced 18% in printed data book, DL110/D)

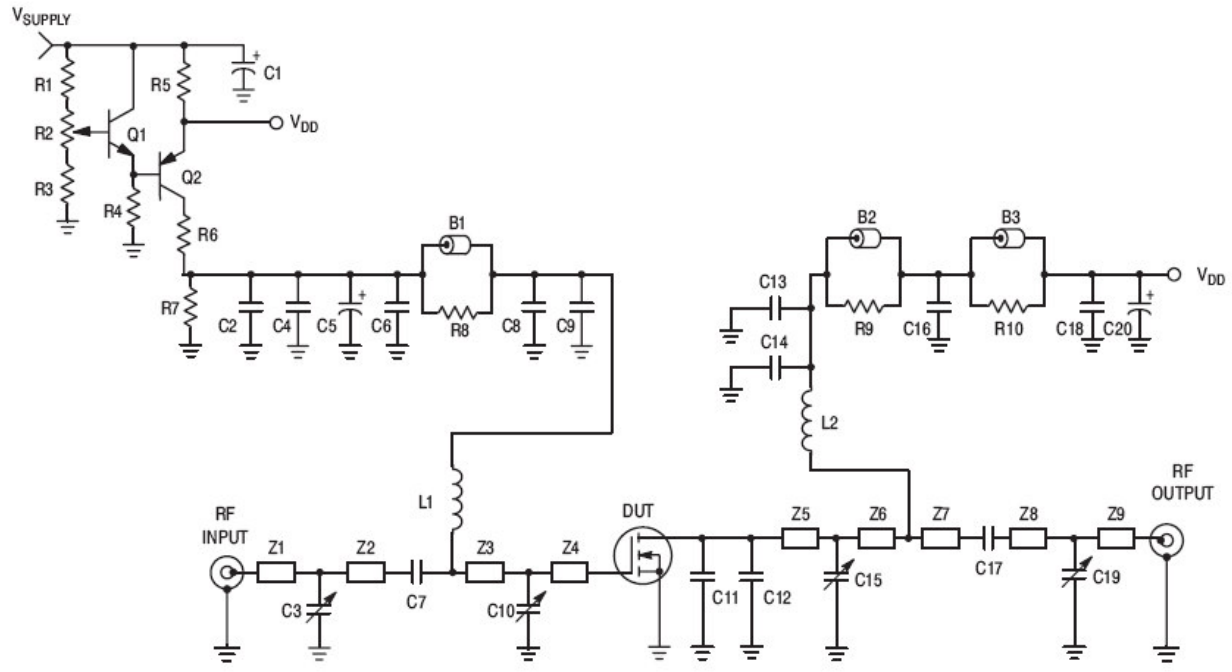


Z1	0.122″ x 0.08″ Microstrip	Z8	0.414″ x 0.330″ Microstrip
Z2	0.650″ x 0.08″ Microstrip	Z9	0.392″ x 0.08″ Microstrip
Z3	0.160″ x 0.08″ Microstrip	Z10	0.070″ x 0.08″ Microstrip
Z4	0.030″ x 0.08″ Microstrip	Z11	1.110″ x 0.08″ Microstrip
Z5	0.045″ x 0.08″ Microstrip	Raw Board Material	0.030″ Glass Teflon®, 2 oz Copper, 3″ x 5″ Dimensions, Arlon GX0300–55–22, ε_r = 2.55
Z6	0.291″ x 0.08″ Microstrip		
Z7	0.483″ x 0.330″ Microstrip		

Figure 4. 1.81 – 1.88 GHz Broadband Test Circuit Schematic

Table 2. 1.81 – 1.88 GHz Broadband Test Circuit Component Designations and Values

Designators	Description
B1, B2, B3, B4, B5, B6	Surface Mount Ferrite Beads, 0.120″ x 0.170″ x 0.100″, Fair Rite #2743029446
C1, C16	470 µF, 63 V Electrolytic Capacitors, Mallory #SME63UB471M12X25L
C2, C9, C12, C17	0.6–4.5 pF Variable Capacitors, Johanson Gigatrim #27271SL
C3	0.8–8.0 pF Variable Capacitor, Johanson Gigatrim #27291SL
C4, C13	0.1 µF Chip Capacitors, Kemet #CDR33BX104AKWS
C5, C14	100 pF Chip Capacitors, B Case, ATC #100B101JCA500X
C6, C8, C11, C15	12 pF Chip Capacitors, B Case, ATC #100B120JCA500X
C7, C10	1000 pF Chip Capacitors, B Case, ATC #100B102JCA50X
L1	3 Turns, 27 AWG, 0.087″ OD, 0.050″ ID, 0.053″ Long, 6.0 nH
L2	5 Turns, 27 AWG, 0.087″ OD, 0.050″ ID, 0.091″ Long, 15 nH
L3, L4	9 Turns, 26 AWG, 0.080″ OD, 0.046″ ID, 0.170″ Long, 30.8 nH
L5	4 Turns, 27 AWG, 0.087″ OD, 0.050″ ID, 0.078″ Long, 10 nH
R1, R2, R3	12 Ω, 1/8 W Fixed Film Chip Resistors, Garrett Instruments #RM73B2B120JT
R4, R5, R6	0.08″ x 0.13″ Resistors, Garrett Instruments #RM73B2B120JT
W1, W2	Beryllium Copper 0.010″ x 0.110″ x 0.210″

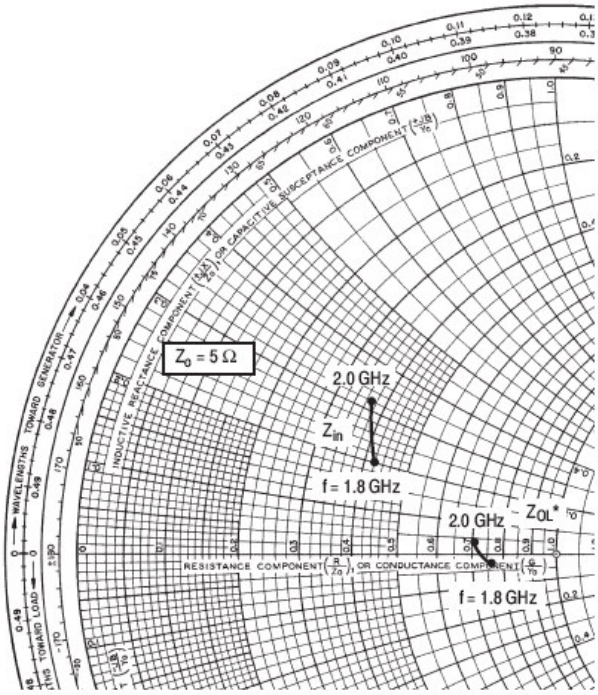


Z1	0.624″ x 0.08″ Microstrip	Z7	0.408″ x 0.08″ Microstrip
Z2	0.725″ x 0.08″ Microstrip	Z8	0.990″ x 0.08″ Microstrip
Z3	0.455″ x 0.08″ Microstrip	Z9	0.295″ x 0.08″ Microstrip
Z4	0.530″ x 0.330″ Microstrip	Raw Board Material	0.030″ Glass Teflon®, 2 oz Copper, 3″ x 5″ Dimensions, Arlon GX0300–55–22, ε_r = 2.55
Z5	0.280″ x 0.330″ Microstrip		
Z6	0.212″ x 0.330″ Microstrip		

Figure 5. Class A Broadband Test Circuit Schematic

Table 3. Class A Broadband Test Circuit Component Designations and Values

Designators	Description
B1, B2, B3	Ferrite Beads, Ferroxcube #56–590–65–3B
C1, C20	470 µF, 63 V Electrolytic Capacitors, Mallory #SME63V471M12X25L
C2	0.01 µF Chip Capacitor, B Case, ATC #100B103JCA50X
C3, C10, C15	0.6–4.5 pF Variable Capacitors, Johanson #27271SL
C4, C16	0.02 µF Chip Capacitors, B Case, ATC #100B203JCA50X
C5	100 µF, 50 V Electrolytic Capacitor, Mallory #SME50VB101M12X256
C6, C7, C9, C14, C17	12 pF Chip Capacitors, B Case, ATC #100B120JCA500X
C8, C13	51 pF Chip Capacitors, B Case, ATC #100B510JCA500X
C11, C12	0.3 pF Chip Capacitors, B Case, ATC #100B0R3CCA500X
C18	0.1 µF Chip Capacitor, Kemet #CDR33BX104AKWS
C19	0.4–2.5 pF Variable Capacitor, Johanson #27285
L1	8 Turns, 0.042″ ID, 24 AWG, Enamel
L2	9 Turns, 0.046″ ID, 26 AWG, Enamel
Q1	NPN, 15 W, Bipolar Transistor, MJD310
Q2	PNP, 15 W, Bipolar Transistor, MJD320
R1	200 Ω, 1/4 W Axial Resistor
R2	1.0 kΩ, 1/2 W Potentiometer, Bourns
R3	13 kΩ, 1/4 W Axial Resistor
R4, R6, R7	390 Ω, 1/8 W Chip Resistors, Garrett Instruments #RM73B2B391JT
R5	1.0 Ω, 10 W 1% Resistor, Dale #RE65G1R00
R8, R9, R10	12 Ω, 1/8 W Chip Resistors, Garrett Instruments #RM73B2B120JT
Input/Output	Type N Flange Mount RF55–22 Connectors, Omni–Spectra



V_{DD} = 26 V, I_{DQ} = 75 mA, P_{out} = 10 W (PEP)

f MHz	Z_{in} Ω	Z_{OL}^* Ω
1800	2.1 + j1.0	3.8 – j0.15
1860	2.05 + j1.15	3.77 – j0.13
1900	2.0 + j1.2	3.75 – j0.1
1960	1.9 + j1.4	3.65 + j0.1
2000	1.85 + j1.6	3.55 + j0.2

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at given output power, voltage, IMD, bias current and frequency.

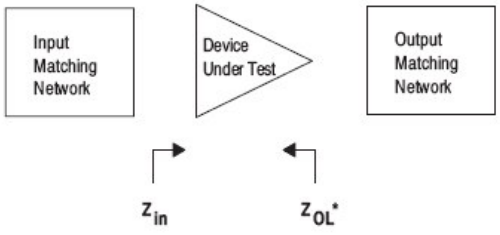
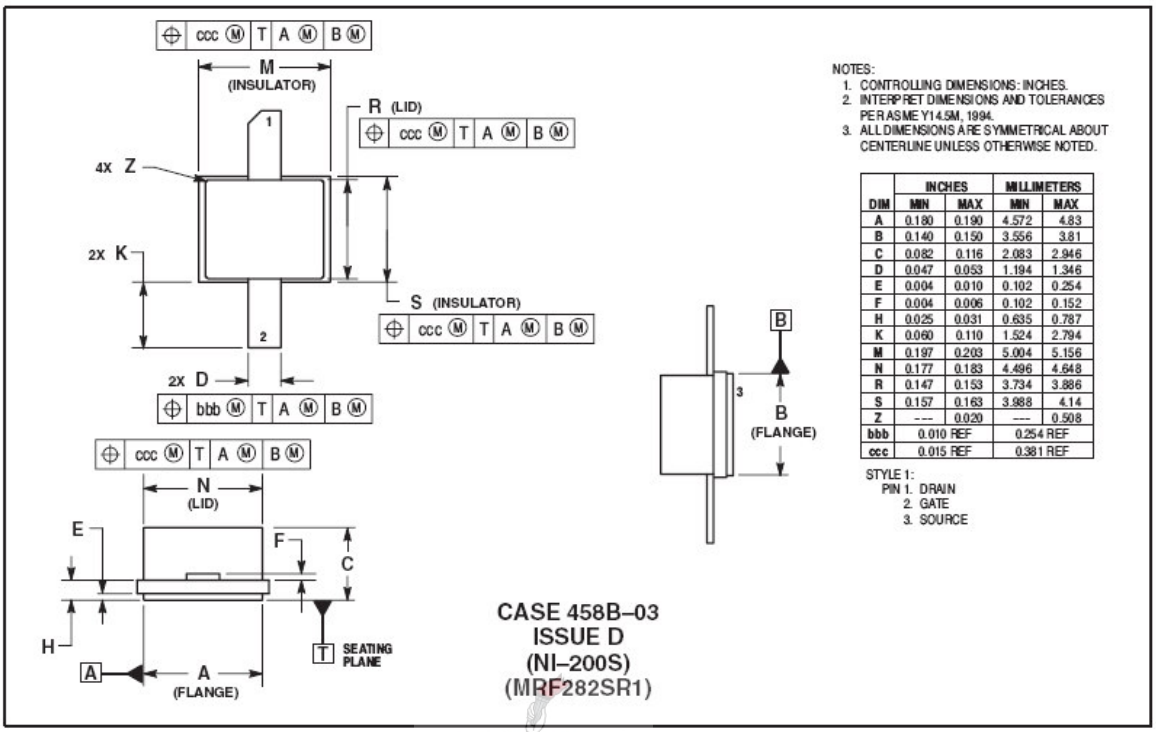


Figure 6. Series Equivalent Input and Output Impedence

NOTES

PACKAGE DIMENSIONS

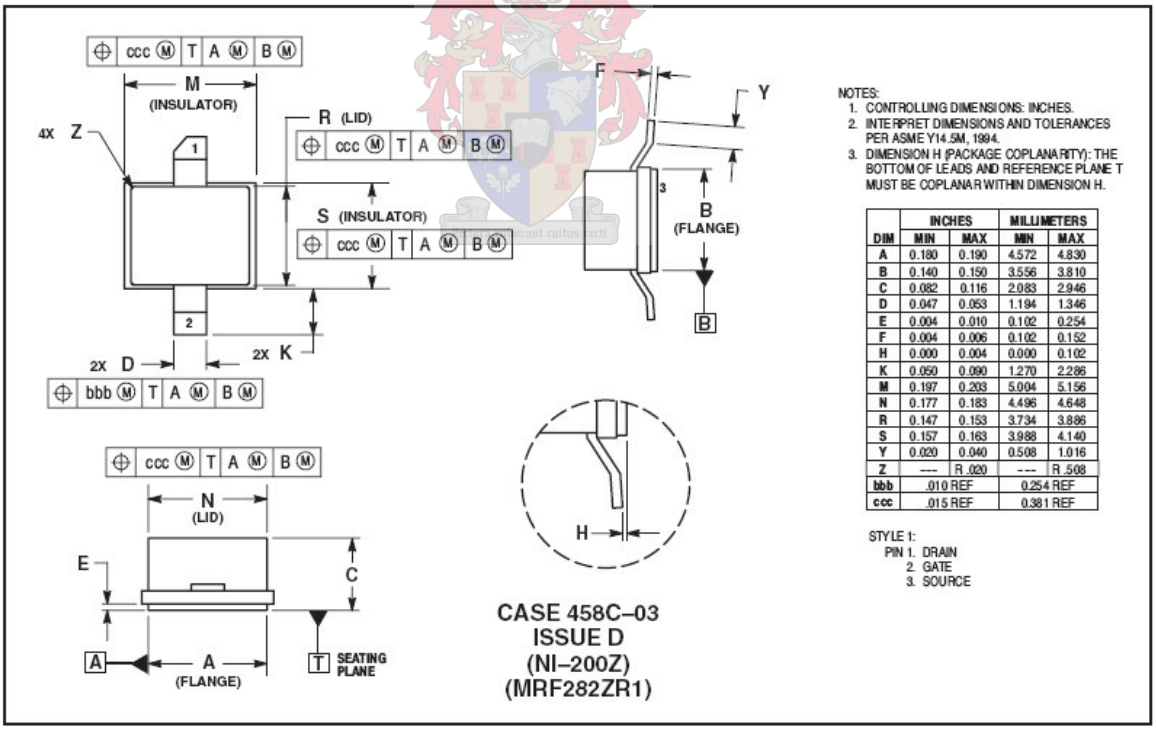


NOTES:
1. CONTROLLING DIMENSIONS: INCHES.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. ALL DIMENSIONS ARE SYMMETRICAL ABOUT CENTERLINE UNLESS OTHERWISE NOTED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.180	0.190	4.572	4.83
B	0.140	0.150	3.556	3.81
C	0.082	0.116	2.083	2.946
D	0.047	0.053	1.194	1.346
E	0.004	0.010	0.102	0.254
F	0.004	0.006	0.102	0.152
H	0.025	0.031	0.635	0.787
K	0.060	0.110	1.524	2.794
M	0.197	0.203	5.004	5.156
N	0.177	0.183	4.496	4.648
R	0.147	0.153	3.734	3.886
S	0.157	0.163	3.988	4.14
Z	---	0.020	---	0.508
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 458B–03
ISSUE D
(NI–200S)
(MRF282SR1)



NOTES:
1. CONTROLLING DIMENSIONS: INCHES.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION H (PACKAGE COPLANARITY): THE BOTTOM OF LEADS AND REFERENCE PLANE T MUST BE COPLANAR WITHIN DIMENSION H.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.180	0.190	4.572	4.830
B	0.140	0.150	3.556	3.810
C	0.082	0.116	2.083	2.946
D	0.047	0.053	1.194	1.346
E	0.004	0.010	0.102	0.254
F	0.004	0.006	0.102	0.152
H	0.000	0.004	0.000	0.102
K	0.050	0.090	1.270	2.286
M	0.197	0.203	5.004	5.156
N	0.177	0.183	4.496	4.648
R	0.147	0.153	3.734	3.886
S	0.157	0.163	3.988	4.140
Y	0.020	0.040	0.508	1.016
Z	---	R .020	---	R .508
bbb	.010 REF		0.254 REF	
ccc	.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 458C–03
ISSUE D
(NI–200Z)
(MRF282ZR1)

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado 80217. 1–303–675–2140 or 1–800–441–2447

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center, 3–20–1, Minami–Azabu. Minato–ku, Tokyo 106–8573 Japan. 81–3–3440–3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong. 852–26668334

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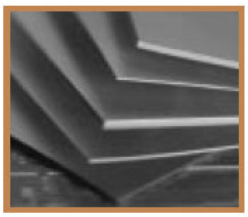
◊ MRF282/D



High Frequency
Circuit Materials

Rogers Corporation
Microwave Materials Division
100 S. Roosevelt Avenue
Chandler, AZ 85226 U.S.A.
Tel: 480 961-1382
Fax: 480 961-4533
Website: http://www.rogers-corp.com/mwu/
litmwu@rogers-corp.com

DATA
RO 1.4000

RO4000® Series
High Frequency Circuit Materials

RO4000® Series High Frequency Circuit Materials are glass reinforced hydrocarbon/ceramic laminates (**Not PTFE**) designed for performance sensitive, high volume commercial applications.

RO4000 laminates are designed to offer superior high frequency performance and low cost circuit fabrication. The result is a low loss material which can be fabricated using standard epoxy/glass (FR4) processes offered at competitive prices.

The selection of laminates typically available to designers is significantly reduced once operational frequencies increase to 500 MHz and above. RO4000 material possesses the properties needed by designers of RF Microwave circuits. Stable electrical properties over environmental conditions allow for repeatable design of filters, matching networks and controlled impedance transmission lines. Low dielectric loss allows RO4000 series material to be used in many applications where higher operating frequencies limit the use of conventional circuit board laminates. The temperature coefficient of dielectric constant is among the lowest of any circuit board material (Chart 1), making it ideal for temperature sensitive applications. RO4000 materials exhibit a stable dielectric constant over a broad frequency range (Chart 2). This makes it an ideal substrate for broadband applications.

RO4000 material's thermal coefficient of expansion (CTE) provides several key benefits to the circuit designer. The expansion coefficient of RO4000 material is similar to that of copper which allows the material to exhibit excellent dimensional stability, a property needed for mixed dielectric multilayer board constructions. The Z-axis CTE provides reliable plated through-hole quality, even in severe thermal shock applications. RO4000 series material has a Tg of >280°C (536°F) so its expansion characteristics remain stable over the entire range of circuit processing temperatures.

RO4000 series laminates can easily be fabricated into printed circuit boards using standard FR4 circuit board processing techniques. Unlike PTFE based high performance materials, RO4000 series laminates do not require specialized processes such as sodium etch. This material is a rigid laminate that is capable of being processed by automated handling systems and scrubbing equipment used for copper surface preparation.

RO4003 laminates are currently offered in two styles, which indicate the type of glass reinforcement used.

Style A - The original RO4003 product configuration. All plies utilize 1080 glass reinforcement.

Style C - Coarser 1675 glass reinforcement is used for some plies, while 1080 glass is used as required to meet overall thickness requirements. Some dielectric thicknesses may not be available in Style C.

Regardless of the style chosen, all electrical properties are held constant. RO4003 Style C exhibits improved dimensional stability and flatness

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RO 1.4000
Page 2 of 4

RO4000® Series Laminate Product Information:

PROPERTY	TYPICAL VALUES		DIRECTION	UNITS	CONDITION	TEST METHOD
	RO4003	RO4350				
Dielectric Constant ε_r	3.38 ± 0.05	3.48 ± 0.05	Z	–	10 GHz/23 C	IPC-TM-650 2.5.5.5
Dissipation Factor	0.0027	0.0040	Z	-	10 GHz/23 C	IPC-TM-650 2.5.5.5
Thermal Coefficient of ε_r	+40	+50	Z	ppm/ C	-100 C to 250 C	IPC-TM-650 2.5.5.5
Volume Resistivity	1.7×10^{10}	1.2×10^{10}	-	MΩ	COND A	IPC-TM-650 2.5.17.1
Surface Resistivity	4.2×10^{9}	5.7×10^{9}	-	MΩ	COND A	IPC-TM-650 2.5.17.1
Electrical Strength	25.6 (650)	31.5 (800)	Z	KV/mm (V/mil)	0.51mm (0.020")	IPC-TM-650 2.5.6.2
Tensile Modulus	26,889 (3900)	11,473 (1664)	Y	MPa (kpsi)	RT	ASTM D638
Tensile Strength	141 (20.4)	175 (25.4)	Y	MPs (kpsi)	RT	ASTM D638
Flexural Strength	276 (40)	255 (37)	-	MPa (kpsi)	-	IPC-TM-650 2.4.4.
Dimensional Stabiltiy	<0.3	<0.5	X,Y	mm/m (mils/inch)	After etch +E2/150	IPC-TM-650 2.24
Coefficient of Thermal Expansion	11 14 46	14 16 50	X Y Z	ppm/ C	-55 to 288 C	IPC-TM-650 2.1.4.1
Tg	>280	>280	-	C	-	TMA
Thermal Conductivity	0.64	0.62	-	W/m/ K	100 C	ASTM F433
Specific Gravity	1.79	1.86	-	-	23 C	ASTM D792
Water Absorption	0.06	0.06	-	%	48 hrs. immersion 0.060" sample Temperature 50 C	ASTM D570
Copper Peel Strength	1.05 (6.0)	0.88 (5.0)	-	N/mm (pli)	after solder float	IPC-TM-650 2.48
Flammability	N/A	UL 94V-O	-	-	-	-

Chart 1: RO4000 Series Materials
Dielectric Constant vs. Temperature

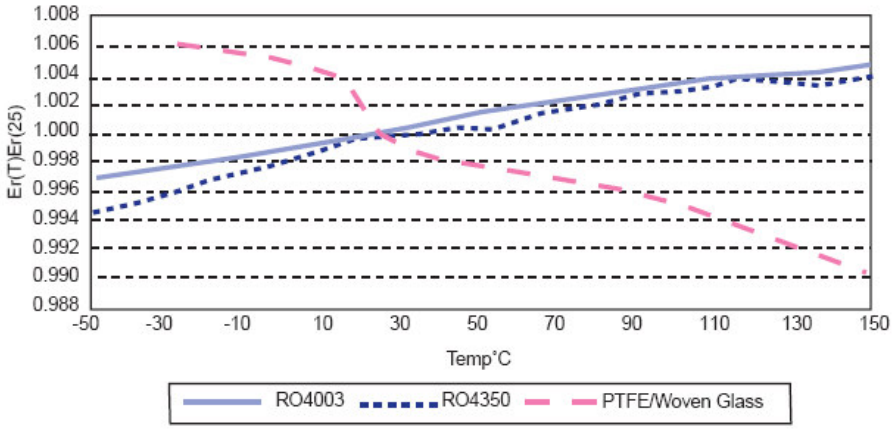


Chart 2: RO4000 Series Materials
Dielectric Constant vs. Frequency

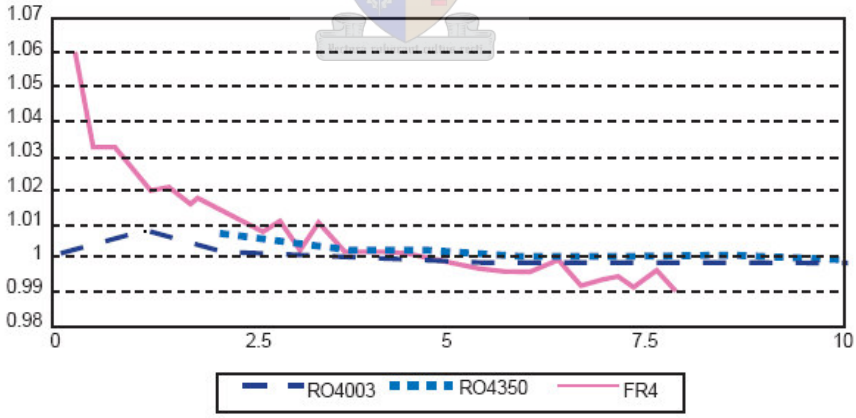
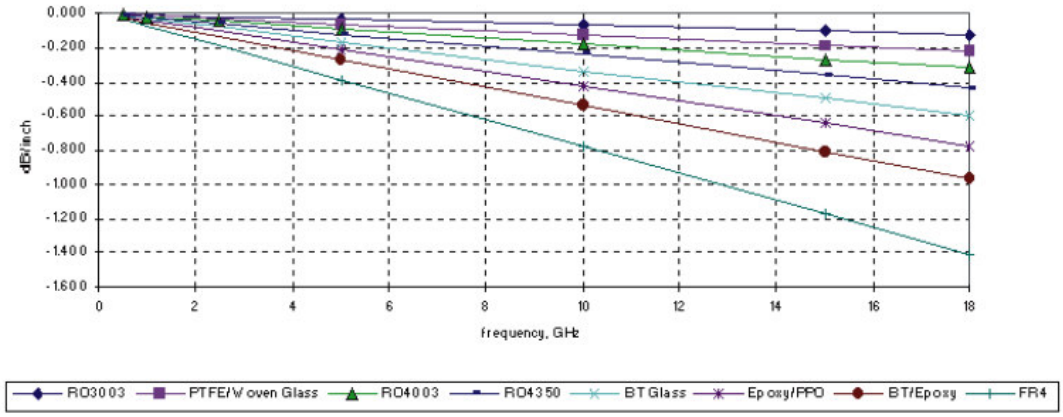


Chart 3: Microstrip Insertion Loss
(0.030" Dielectric Thickness)



Ordering Information:

Standard Thicknesses and Tolerances:

RO4003 Materials:	**RO4350 Materials:**
0.0080 ± 0.0010 (0.20 ± 0.03 mm)	0.0100 ± 0.0010 (0.25 ± 0.03 mm)
0.0200 ± 0.0015 (0.51 ± 0.04 mm)	0.0200 ± 0.0015 (0.51 ± 0.04 mm)
0.0320 ± 0.0020 (0.81 ± 0.05 mm)	0.0300 ± 0.0020 (0.76 ± 0.05 mm)
0.0600 ± 0.0040 (1.52 ± 0.10 mm)	0.0600 ± 0.0040 (1.52 ± 0.10 mm)

Standard Claddings:

½ ounce (17 µm) electrodeposited copper.
1 ounce (35 µm) electrodeposited copper.

Standard Panels Sizes:
The standard panel sizes are 24 x 18" (610 x 457 mm) and 12 x 18" (305 x 457 mm).

Information on other thicknesses, claddings and panels sizes available call your Customer Service Representative at Tel: 480 961-1382 or Fax: 480 961-4533.

ROGERS
SINCE 1832

Rogers Corporation
Microwave Materials Division
100 S. Roosevelt Avenue
Chandler, AZ 85226-3415 U.S.A.
Tel: 480 961-1382 Fax: 480 961-4533
Toll Free: 877 643-7701
http://www.rogers-corp.com/mwu/

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In Japan:
Rogers Japan Inc., Tokyo 116 Japan
Tel: 03-3807-6430 Fax: 03-3807-6319
In Hong Kong:
Rogers Southeast Asia, Sheung Wan, Hong Kong
Tel: 852-2549-7806 Fax: 852-2549-8615
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