Miniaturised Multilayer RF AND Microwave Circuits

by

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Declaration

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Abstract

Keywords - Multilayered technology, Miniaturised circuits, Substrate Integrated Waveguides, Printed Circuit Boards, Low Temperature Co-fired Ceramics, Liquid Crystalline Polymer, Folded Waveguides, Ridge Waveguides, Analog Polyphase Filters, PIN Diodes, LTCC limiter-switch

Ceramic and laminate multilayered technologies are explored in the design of novel circuit topologies and in novel implementations of classical circuit topologies.

A cross-slot coupled filter topology implemented in folded substrate integrated waveguide (FSIW) is proposed and is shown to exhibit properties that make it favourable for diplexer design. A C-Band diplexer design is presented. The diplexer is fabricated in both Liquid crystalline Polymer (LCP) and Printed Circuit Board (PCB) multilayed technology. The viability of both processes for this type of circuit is analysed and performance is verified by simulation and measurement.

A 'ridge-like' folded substrate integrated waveguide resonator is proposed. A comparative analysis of this resonator and a traditional ridge waveguide resonator structure in substrate integrated technology is presented. For rectangular waveguide resonators with identical outer dimensions, the former is shown to achieve lower operational frequencies relative to the latter. Two X-band filters are designed using the 'ridge-like' FSIW resonator. Both filters are fabricated in PCB multilayered technology and performance is verified by both simulation and measurement. The measurement results of the first, a second order filter, show a maximum insertion loss of 2.23 dB for the primary band and a wide frequency range of 7.5 GHz between the first passband and the second. The second filter is a fourth order filter which achieves a maximum measured insertion loss of 4.7 dB for the primary passband with the second passband occuring over 8.5 GHz away.

A classical sequence asymmetric RC polyphase filter (PPF) is implemented in low temperature co-fired ceramics (LTCC) technology. The novel implementation realises a miniaturised structure comprising embedded components interconnected using planar transmission lines. Verification of the structure's performance is by simulation of a three segment PPF. The LTCC PPF is shown to achieve an image suppression of 35 dB over a frequency range of 100 MHz to 300 MHz and a gain error of 0.14dB between its quadrature outputs.

The final design is a novel implementation of a miniaturised two-stage PIN Diode limiter-switch in LTCC. The structure comprises both embedded components and surface mount components interconnected using planar transmission lines and vias. Circuit viability is assessed through simulation

of a multilayered L-Band limiter-switch design. An insertion loss of 0.25 dB and a return loss of 25.34 dB at a center frequency of 1.3 GHz are obtained when the switch is in its off-state. When a large 1 μs input pulse signal of 45 dBm is applied at the input of the limiter-switch, the resulting output pulse has a flat leakage of approximately 16.4 dBm.

Opsomming

Sleutelwoorde: Multilaag tegnologie, Miniatuur stroombane, Substraat Geïntegreerde Golfleiers, Gedrukte Stroombaanborde, Lae Temperatuur Ko-gevuurde Keramieke, Vloeibare Kristalyne Polimere, Gevoude Golfleier, Rif-Golfleiers, Analoog Polifase Filters, PIN diodes, LTKK Beperker

Keramiese en gelamineerde tegnologieë word in hierdie werk ondersoek vir die ontwerp van nuwe stroombaantopologieë en nuwe implementerings van klassieke stroombaantopologieë.

‘n Gekruisde gleuf filter topologie, geïmplementeer in Gevoude Substraat Geïntegreerde Golfleier, word voorgestel. Dit word aangetoon dat hierdie topologie eienskappe besit wat dit nuttig maak vir gebruik in diplekser ontwerp, en ‘n C-band diplekser word ontwerp. Die ontwerp word in beide Vloeibare Kristalyne Polimeer tegnologie en gedrukte stroombaanbord tegnologie implementeer, en die geskiktheid van hierdie tegnologieë word bespreek. Die werkverrigting van die ontwerpe word met simulasie en metings geverifieer.

‘n Rif Gevoude Substraat Geïntegreerde Golfleier resoneerder word voorgestel. ‘n Vergelykende studie van hierdie resoneerder en ‘n tradisionele Rif Golfleier resoneerder in Substraat Geïntegreerde Golfleier word gedoen. Vir reghoekige golfleier resoneerders met identiese buite-afmetings, word getoon dat eersgenoemde laer gebruiksfrekwensies toon . Twee X-band filters word ontwerp met die nuwe resoneerder. Beide filters word vervaardig in multilaag stroombaanbord tegnologie, met die werkverrigting geverifieer met metings en simulasie. ‘n Tweede-orde filter wys ‘n maksimum insetverlies van 2.23 dB vir die primêre band, en ‘n 7.5 GHz stopband tussen die eerste en tweede deurlaatband. ‘n Vierde-orde filter toon ‘n insetverlies van 4.7 dB vir die primêre deurlaatband, en ‘n 8.5 GHz stopband.

‘n Klassieke asimmetriese RC-polifase filter word geïmplementeer in Lae Temperatuur Ko-gevuurde Keramiek tegnologie. Die nuwe implementering realiseer ‘n miniatuur struktuur bestaande uit ingeslote komponente, verbind met planêre transmissielyne. Verifikasie van die struktuur word gedoen deur middel van ‘n drie-segment polifase filter, met ‘n beeldverwerping van 35 dB oor die 100 MHz tot 300 MHz band, en ‘n aanwinsfout van kleiner as 0.14 dB tussen die kwadratuur uitreespannings.

Die finale ontwerp is ‘n implementering van ‘n geminiaturiseerde twee-stadium PIN diode beperker in Lae Temperatuur Ko-gevuurde Keramiek tegnologie. Die struktuur bestaan uit beide ingeslote en oppervlak-gemonteerde komponente, wat verbind word met planêre transmissielyne en vias.

‘n L-band beperker word ontwerp en met simulasie geverifieer. ‘n Insetverlies van 0.25 dB en ‘n weerkaatskoëffisiënt van 25 dB by 1.3 GHz word behaal in die af-toestand. Met’n groot 1 mikrosekonde intreepuls van 45 dBm wat aangelê word by die intree, word ‘n uittree verkry met ‘n plat pulsvorm van 16.4 dBm.

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In the years spent pursuing this degree, I have come to learn that support and good friendship are very necessary to provoke a healthy thought process, to steer one back in the right direction when the tough gets going and to inspire one to want to do better. During this period, I have met new friends and made new acquaintances, and I have been educated on aspects of my field that I was unaware of. I have also grown fonder of those I already knew, appreciating how much I continue to learn from them. For all the experiences, I would like to thank:

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Contents

List of Figures

Chapter 1

Introduction

1.1 Background

Over the last few decades, the RF and Microwave industry has seen an evolution in the implementation of electronic circuits. To satisfy the stringent requirements that modern communication systems demand, present day designs have had to transition from bulky sizes to miniaturised equivalents with higher performance specifications, lower losses, better power handling capability and lighter weight. In addition to this, space restrictions have also facilitated the integration of different functionalities, traditionally unique to separate devices, into single chips. One of the major developments that enabled these achievements was the introduction of multilayer circuits.

Different substrate technologies exist in modern day for the realisation of multilayer circuits, with the main ones being formed of ceramic materials and laminates.

The origin of multilayer ceramic substrate technology dates back to the late 1950s in developments at RCA corporation [58]. It is also during this period that the current process technologies such as green sheet fabrication, via forming and multilayer laminate technology using the doctor blade method were discovered [58]. This progress paved way for the development of multilayer boards for IBM's mainframe computer which were commercialised in the early 1980s [58]. These were developed in high temperature cofired ceramic (HTCC). Low temperature cofired ceramic (LTCC) substrates were only developed later and some of the first boards were only manufactured in the early 1990s by Japanese and American electronics and ceramic manufacturers [58]. LTCC had the advantage of using low electrical resistance materials such as copper, gold and silver for wiring, which was beneficial in applications that required high wiring density to reduce the associated electrical resistance and signal attenuation. From the later half of the 1990s to present day, the focus of multilayer ceramic substrate technology has shifted to high frequency applications such as mobile communications.

PCB multilayer products date back from 1961 with the Hazeltyne Patent [70]. Differerent industries such as aerospace, computing, telecommunication, as well as defense systems all began to take advantage of the space saving that a multi-layer circuit board provided.

In present day, multilayer circuits offer impressive flexibility in the design of RF and microwave

designs and continue to inspire the development of new topologies with improved functionality. Most of these have been motivated by traditional implementations of specific structures like waveguides and coaxial lines, which have been modified to allow for their implementation in multilayered technologies. As such, integration of several different types of transmission media and electronics components into single compact structures has been facililated.

The choice of one multilayer substrate technology over another is dependent on the achievable capabilities of each with regard to desired functionality. There are always tradeoffs to be considered in terms of performance, costs, complexity levels and manufacturability, and in the end, compromise is always made to select the best suited option.

1.2 Motivation and Contributions

The design and manufacture of multilayer circuits certainly still has the potential for further development for many more years. In this dissertation, three classes of microwave circuits are investigated for implementation in multilayer technology. The classes are: pure transmission-line structures, hybrid structures with lines and passive etched components, and hybrid structures with lumped/active components. For each class, a circuit or circuits are designed and implemented in the relevant multilayer technology. For the circuits implemented in PCB laminates, verification is by simulation and measurement, while for those implemented in LTCC, verification is by simulation only.

For the first class, the author studies structures that have been implemented in substrate integrated waveguide (SIW), one of the platforms that have found great application in multilayer circuit environment. The specific research on these SIW revolves around filter structures and the fabrication of these is in PCB laminates, taking advantage of their cost effectiveness for less complicated toplogies. Minimal analysis has been presented on the performance of these devices from the angle of interacting electromagnetic fields inside the devices. This dissertation therefore seeks to provide a more in depth analysis of these structures and proposes topologies to achieve alternative and improved performance characteristics.

For the second class, an analog RC polyphase filter is presented in LTCC technology. In this case, the possibility of creating planar, etched capacitors and resistances in LTCC is exploited. It is also shown that because this class of device only utilises resistive and capacitive components, it offers significant possibilities for vertical integration. It therefore lends itself very well to multilayer implementation. Polyphase filters find use in communications channels using orthogonal (I and Q) channels, and are often designed in CMOS technology. Because of process tolerances, parasitic effects and low quality factors for passive components, CMOS unfortunately often has sub-optimal analog performance. In addition, due to size constraints, RC components for low RF frequencies are difficult to implement, therefore most of the reported RC polyphase filters in CMOS operate in the lower gigahertz frequencies.

For the final class, the good thermal properties of LTCC is exploited for the design of a PIN diode limiter/switch, with size reduction due to the multilayer construction. The PIN diode limiter

has the flexibility to operate as a switch when a DC bias is applied. The dissertation then outlines various advantages of LTCC that make it suitable for design of miniaturised versions of PIN diode limiters.

Within the theme of multi-layer technology, the original contributions of this dissertation are both novel circuit topologies, and novel implementations of classical topologies. These contributions are:

1. Design of a novel cross slot-coupled folded substrate integrated waveguide (FSIW) filter.
2. Design of a folded substrate integrated waveguide diplexer using cross slot-coupled FSIW filters.
3. In depth comparative analysis of a ridge-like FSIW resonator topology, in comparison to a ridge SIW resonator.
4. Implementation of an LTCC analog RC polyphase filter.
5. LTCC implementation of a PIN diode limiter with switching capabilities.

In the case of 1 and 2, the originality lies in the design itself, while in 4 and 5, the contribution lies in the implementation in multilayer technology. As a secondary contribution, a circuit model for both a slot-coupled and cross-slot coupled (FSIW) second order filter is proposed to model the device performance in a circuit environment.

1.3 Outline of the Dissertation

Chapter 2 of the dissertation presents an overview of multilayer substrate technologies with specific focus of LTCC, PCB and Liquid Crystalline Polymer (LCP). This chapter outlines the characteristics of these technologies as well as the associated manufacturing processes. It also provides brief discussions on their limitations. It serves as a reference chapter for the chapters following it to aid in understanding why specific technologies are chosen for specific designs.

In chapter 3, a brief discussion on substrate integrated waveguides (SIW) is presented. The chapter addresses the design of folded SIW (FSIW) resonators and analyses a quarter wavelength FSIW resonator and filter realised through slot-coupling. A cross slot-coupled FSIW filter is then proposed and using this a C-Band Diplexer is designed and analysed.

Thereafter, in chapter 4, the dissertation presents a comparative analysis of a ridge SIW (RSIW) resonator and an FSIW resonator, denoted ridge-like FSIW resonator, to study their structural and performance similarities and/or differences with regard to stopband performance. The chapter also presents the design of two X-band filters designed using the ridge-like FSIW resonators.

In Chapter 5, a theoretical discussion of analog RC polyphase filters is presented. Implemention of such filters in LTCC is proposed and a minaturised three-segment polyphase filter is designed to operate in a frequency range of 100 MHz to 300 MHz, offering image signal suppression of over 35 dB.

The final design chapter is chapter 6 which outlines the theoretical aspects of PIN diode limiter and switch design. An LTCC-based PIN diode limiter with switching capabilities is proposed and performance is verified using a three dimensional structure designed to operate at a center frequency of 1.3 GHz.

The dissertation then concludes with a summary of the work that has been presented and the results that have been achieved.

The design and analysis of the microwave multilayer circuits is made easier by the availability of commercial electromagnetic solvers based on well-established numerical methods for solving Maxwell's equations. Full-wave three dimensional electromagnetic simulation is an important part of a microwave engineer's workflow. It allows the engineer to analyse the effects of interaction of components with the layout such as unwanted coupling, box resonances, parasitic radiation etc. Full-wave three dimensional electromagnetic simulation softwares are often used in concurrence with circuit-theory-based CAD. In this dissertation, Sonnet, Agilent's ADS and CST Microwave Studio are used for full-wave electromagnetic analysis, where as AWR's Microwave office is used for the equivalent circuit simulations.

Chapter 2

Multilayer Substrate Technology

2.1 Introduction

The RF and Microwave industry has recently been trending towards miniaturisation of components to be able to meet the stringent size requirements for smaller sized systems. In the design of these miniaturised components, designers have to take into account a number of factors. Among these are: the substrate technology to be employed for the design, material properties of the substrate, available manufacturing technology and related costs of processing, and process reliability. It is also important to consider the possible effects of integrating different materials with different properties, the guidelines and design recommendations associated with a specific substrate technology and the functionality of the design.

Several substrate technologies exist currently that allow for the realisation of 3D multilayered structures. The ability of an electrical design to be built in a vertical direction with conductors printed in different layers and interconnected using electrical vias has hugely aided in the reduction of horizontal footprint of components. These substrate technologies are used in the packaging of Multi-chip Modules (MCM) in which several components can be integrated into a single compact module.

MCM is a technology which has revolutionised the electronics industry in recent years. It eliminates discrete packaging of individual integrated circuits (ICs) hence replacing the system that connected packages which were much larger than the chips they enclosed, with monolithic substrate structures that integrate several unpackaged chips and/or discrete components in one package. This concept is referred to as system in package (SiP). SiP has greatly aided in the reduction of the size of an assembly of components transforming from the traditional larger footprint printed wire boards (PWBs) to this sophisticated packaging system while considering four features [76]:

- Active components are removed from their packages and are assembled directly to the SiP making use of flip chip assembly (FCA). Components that are not designed for FCA can be converted to make it possible for them to be assembled as flip chips.

- As many passive components as possible are embedded within the layers of a multi-layered

SiP. Resistors with values ranging from 15 ohms to 30 kilo-ohms can be embedded efficiently as well as bypass/decoupling capacitors of values up to 0.1 microfarads [76].

- The component area on the top and bottom layers need to be balanced. Given that most passive components can be embedded in the inner layers, it becomes easier to freely place the active components on the top and bottom layers in flip chip form without having a significant impact on the total height of the SiP.

- The more efficiently the connector area can be used, the better. Strategic placement of connector minimises the loss of functional area.

Three principal technologies exist for fabricating MCM substrates [95]. The first is MCM-L with the L standing for laminates. MCM-L is an advanced form of printed circuit board (PCB) technology used for mid-range performance and for low cost applications [95]. The other two are MCM-C (C stands for ceramic), a co-fired ceramic hybrid circuit technology that used thick film screen printing, and MCM-D which is similar to integrated circuit manufacturing with thin film deposited over silicon or a metal base [95].

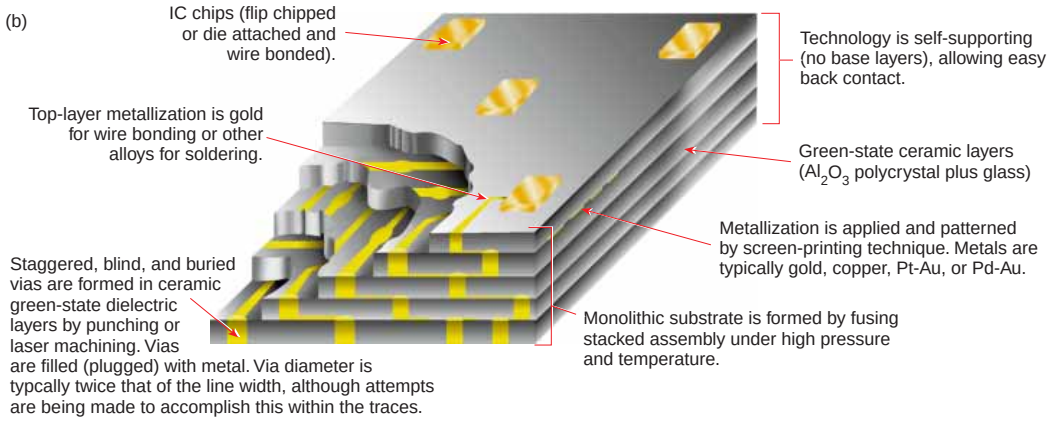
In this dissertation, microwave devices are designed in ceramic substrate technology and in laminates, while applying the principles of the MCM concept . Passive Components are embedded within a multilayer structure, implemented in the form of distributed components, which additional chip components are mounted on the surface layers.

Figure 2.1 shows a diagramatic definition of MCM-C and MCM-L.

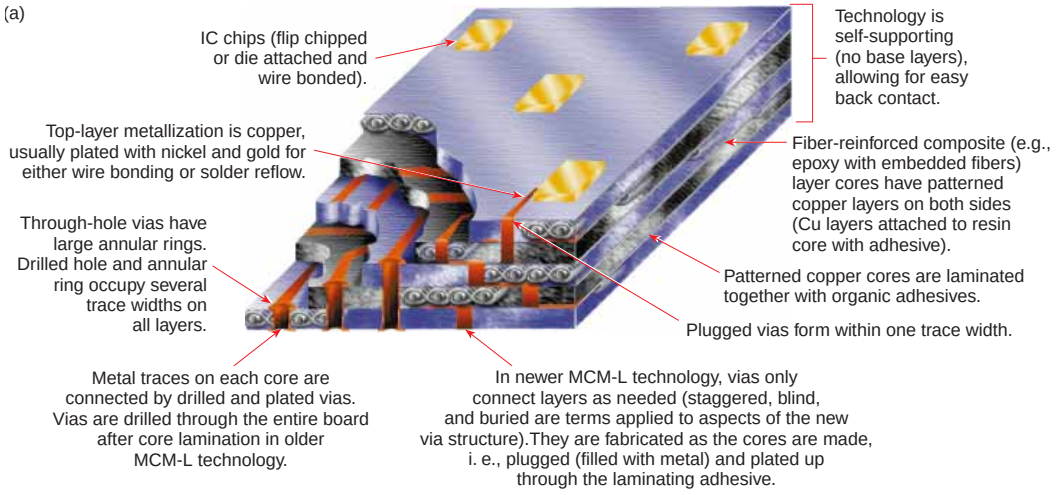
In designs that follow in subsequent chapters, three multilayer substrate technologies are employed: Low Temperature Co-fired Ceramics (LTCC) - an MCM-C substrate technology, PCB multilayer technology utilising laminates and Liquid Crystalline Polymer (LCP) , also an MCM-L substrate technology. All of these have good electrical properties making them suitable for RF and microwave applications. The choice of one over the other is dependent on the application and what it demands in terms of performance and cost-effectiveness. These technologies are briefly discussed the following subsections, with a general overview of each, the manufacturing process associated with it and the limitations of the technology.

This chapter also briefly presents a section on embedded components to discuss their implementation in multilayer circuits.

Finally, a brief outline is also given on how these technologies are to be applied in the designs presented in this dissertation.



(a) MCM-C[21]



(b) MCM-L [21]

Figure 2.1: MCM-C and MCM-L Substrate Technologies

2.2 Low Temperature Co-fired Ceramics (LTCC)

LTCC is a ceramic substrate system applied in electronic component circuits as a cost effective substrate technology. The name emanates from the fact that LTCC circuits are fired at relatively low temperatures of less than 900^0C. It is a composition of recrystallised glass and ceramic powder in binders and organic solvents[64]. LTCC is a very attractive substrate for applications in microwave and millimeter wave frequencies that has found applications in some of the more active areas including Bluetooth modules, front end modules of mobile phones, wireless local area networks (WLAN), collision avoidance radar, etc. [88]. The technology allows for low conductor loss, low substrate loss and for as many as 50 laminated layers of substrate tape enabling high density integration of microwave and millimeter wave components within a single module. Figure 2.2 shows a complex

LTCC module with a variety of embedded components as well as surface mounted components. It also shows buried conductor lines and vias for connection of conductors in different layers as well as for grounding purposes.

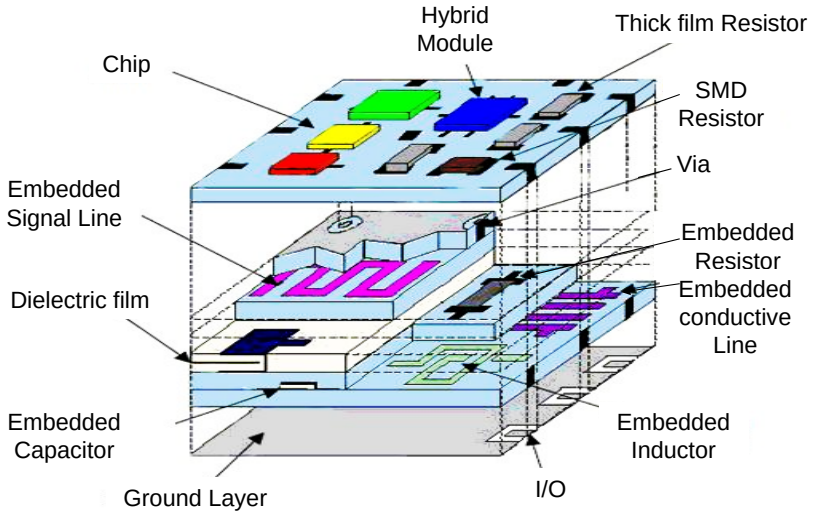


Figure 2.2: Complex LTCC Circuit [16]

Metal conductors, usually gold (Au) and silver (Ag) or alloys with platinum (Pt) and palladium (Pd), are screen printed layer by layer on unfired (green) ceramic tape, then are inspected before they are stacked together, aligned on top of each other and laminated. The low firing temperature of LTCC enables gold (Au) and silver (Ag) conductors, which have melting points of 960 ^{0}C and 1100 ^{0}C respectively, to be co-fired with the ceramics.

LTCC has the advantage of having low line losses at high frequencies and competitive manufacturing costs. This substrate technology has been in competition with PCBs (printed circuit boards) like FR4, a well established substrate with low manufacturing and production costs. The disadvantage that FR4 has is that it is less suitable for high frequency applications, only being usable for frequencies of up to a few gigahertz. For higher frequency applications, the option of other PCB designed for high frequency use (relatively expensive in comparison to FR4) is recommended, or ceramic substrates is recommended.

Other than the related costs, physical and electrical properties of materials must also be considered in choosing a suitable substrate system. Table 2.1 , derived from [64], compares different properties of PCB/PTFE (polytetrafluorethylene) to those of LTCC from DuPont and Ferro. TCE and TC in the table stand for thermal coefficient of expansion and thermal conductivity respectively. The relative price is computed on the assumption of medium volume of approximately 10 000 modules annually and for an approximate circuit area of 5 to 7 cm^2 at an application frequency of 24 GHz.

Supplier & Material	**Substrate**	**Thickness** µm	**Dielectric Constant,** ε_r	**Dissipation Factor, tan(δ) (10 GHz)**	**(TCE)** ppm/K	**TC** W/mK	**Relative Price**
Rogers	RO3006	760	3	0.0013	17	0.5	1.2
	RO3006	635	6.15	0.0025	17	0.61	2.2
	RO3006	1270					3.7
	RO3010	635	10.2	0.0035	17	0.66	2.4
	RO3010	1270					4.1
Arlon	AR 600	635	6	0.0035	12	0.43	6.1
	AR 1000	635	10	0.0035	14	0.65	4.8
Taconic	RF-60	635	6.15	0.0028	12	0.5	1.1
	CER-10	635	10	0.0035	14	0.3	1.8
Dupont	951-AX, **Au**	210	7.8	0.005	5.8	3	1.5
	951-AX, **Ag**						1.0
Ferro	A6M, **Au**	185	5.9	0.002	7	2	2.2
	A6S, **Ag**				8		0.6

Table 2.1: Comparison of a Selection of RF-PCB/PFTE Vs. LTCC

Other than its comparatively low manufacturing costs, it is clear that LTCC has better thermal conductivity than the PCBs/PTFE. However, this is still low for applications that require good dissipation of heat. The substrate makes up in the form of embedded metal thermal vias that create high conductivity paths which transfer heat to a heat sink. Kulke et. al.[64] summarises the advantages of LTCC as:

- low tolerance in dielectric constant (DuPont 951)
- better thermal conductivity
- low thermal coefficient of expansion
- excellent for multilayer circuit design
- high degree of integration due to cavities and buried passive elements
- low material costs for silver systems
- low production costs for medium and high quantities

Apart from those, the high dielectric constant of LTCC allows for reduced sizes of distributed line components. LTCC tapes also have a low loss tangent and can tolerate high temperatures making them well suited for use in harsh environments.

There are a number of LTCC materials available in on the market. Some suppliers offers full LTCC material systems qualified for RF and microwave applications that have conductor pastes and

resistive pastes that are compatible with their respective LTCC substrates. Examples of these are: DuPont (951 and 943 (low loss tape)), Ferro (A6M (microwave tape) and A6S (low cost microwave tape)) and Heraeus (CT700, CT800 and CT2000) and Electro-Science Laboratories (ESL). Some of the other LTCC tapes available in the market have to use conducting pastes from the suppliers with full systems. Table 2.2 compares the properties of LTCC tapes from different suppliers.

LTCC Supplier	**Products**	**Dielectric Constant, e_r**	**1/tanδ**	**Thermal Expansion Coefficient (ppm/^{0}C)**	**Thermal Conductivity (w/m × K)**	**Flexural Strength (MPa)**
Kyocera	G55	5.7	800 (10 GHz)	5.5	2.5	200
	GL660	9.5	300 (10 GHz)	6.2	1.3	200
DuPont	951	7.8	300 (3 GHz)	5.8	3.3	320
	943	7.4	500 (40 GHz)	6.0	4.4	230
Ferro	A6-M A6-S	5.9	500 (3 GHz)	7.0	2.0	170
		5.9	500 (3 GHz)	8.0	2.0	160
Heraeus	CT700	7.5	450 (1 MHz)	6.7	4.3	240
	CT2000	9.1	1000 (450 MHz)	5.6	-	310

Table 2.2: Different Suppliers of LTCC and Respective Tape Properties

The conductive pastes used with LTCC materials have to be compatible with the resistive and conductive layers. They must also have low square resistance and should be able to create electrical and mechanical fine binding and stick well to the substrate. Gold and silver pastes have the lowest specific resistance where as some of the alloys like Pt-Au pastes have the highest. The difference between gold and silver pastes is not much in terms of properties. The main reason why silver is used more than gold is in the prices; gold is more expensive. LTCC suppliers such as Ferro and DuPont provide advice on which pastes are better suited for specific LTCC tapes.

2.2.1 LTCC Manufacturing Process

The manufacturing process for LTCC (see figure 2.3) entails the screen printing of individual layers of flexible, unfired (green) ceramic tape with a suitable conductor. The process starts with the definition of the substrate size and the number of layers required for a design. The via holes for individual sheets are then drilled usually using laser or by mechanical punching. These holes are then filled with an appropriate conducting paste by either screen printing or an analogous stencil masking process [21]. The conductors are then screen printed on individual layers, a process which is achieved by a mesh geometry that limits the achievable line widths and spaces.

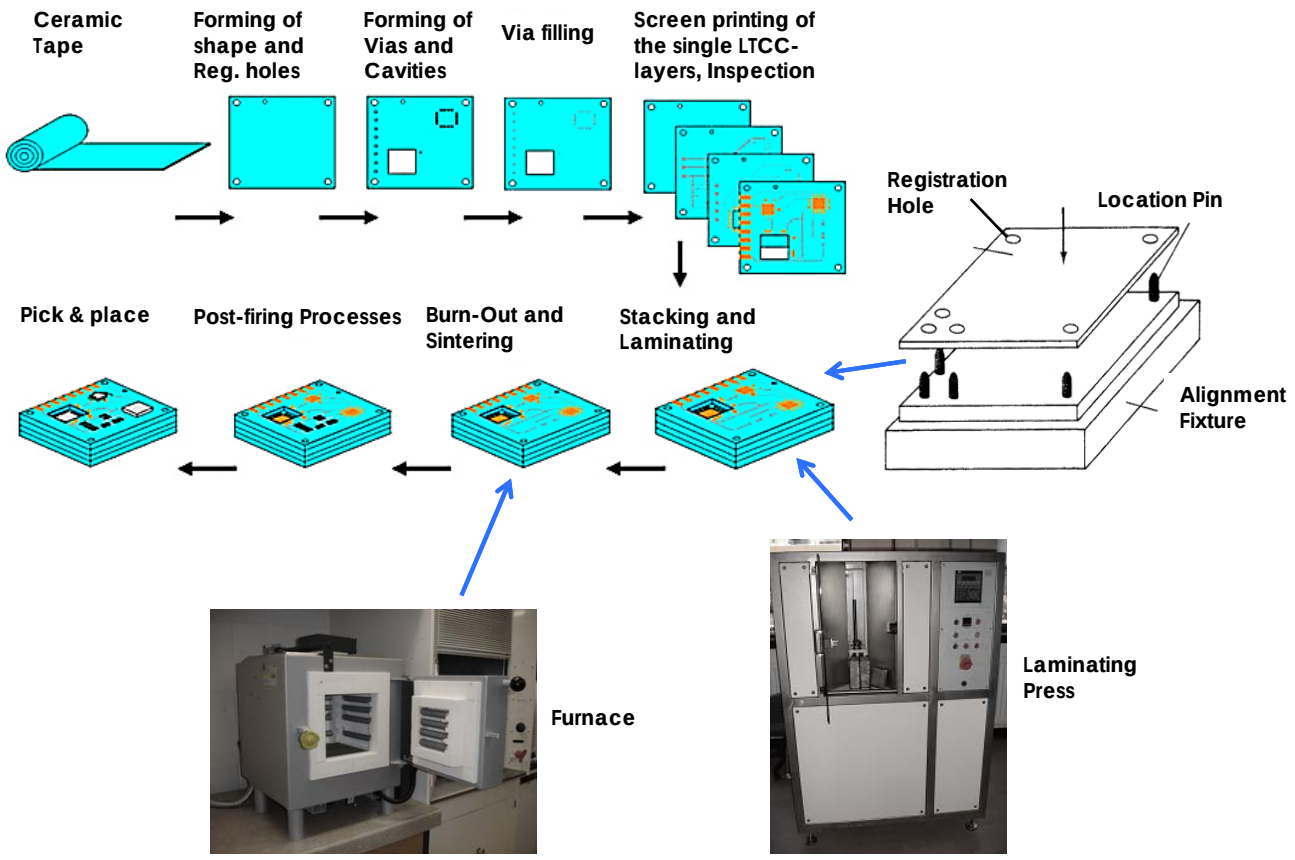


Figure 2.3: LTCC Manufacturing Process

The screen printing process utilises four essential items: The printing medium (thick film paste), a screen defining the desired patterns, the substrate onto which the pattern is made and a squeegee with which to force the paste through the screen. Resistive paste is also printed to form buried resistors. Apart from the resolution of the printed elements, the viscosity of the thick film paste, the ability of the emulsion (see figure 2.4) to form a good gasket with the substrate and the squeegee speed and pressure also play a role in determining the resolution of the printed elements[21]. By combining and optimising all these parameters, vias of 200 µm or smaller and line and spaces of about 125 µm can be achieved [21].

The different layers are then aligned using an alignment fixture and laminated using a lamination press at a pressure of 3000 psi and a temperature of 150 ^{0}C for about 8 to 10 minutes [81]. The lamination process temporarily binds all the layers into a single structure. The next step is to fire the laminated structure at temperatures of about 900 ^{0}C. The exact firing profile varies from vendor to vendor based on the substrate properties. Figure 2.5 shows the firing profile for Ferro A6 system which is used in the designs in this dissertation.

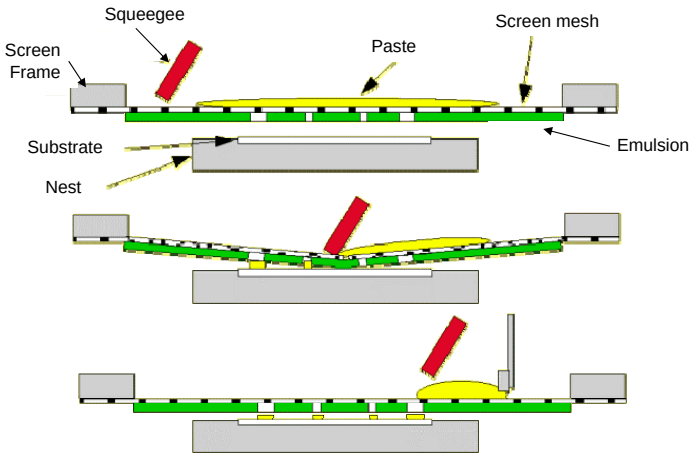
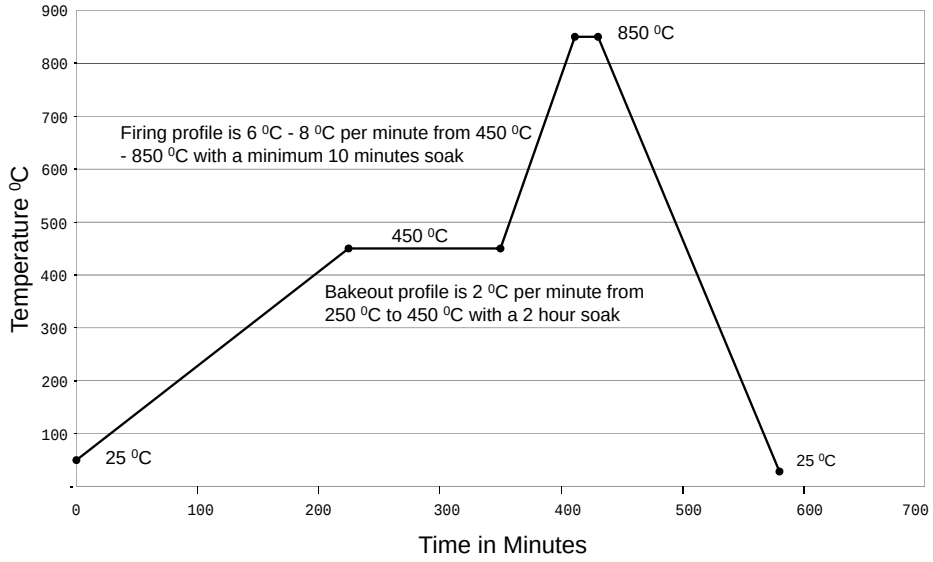
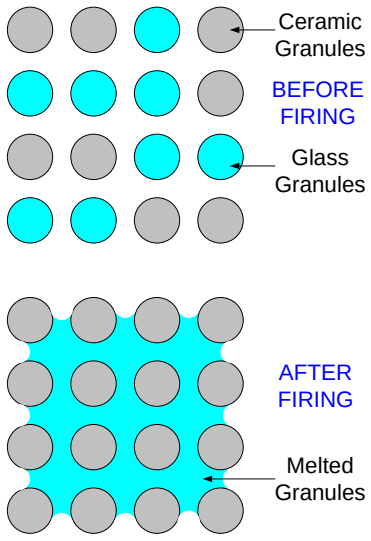


Figure 2.4: Screen Printing [52]

The initial stage in which the temperature rises from $250\,^0C$ to $450\,^0C$ at the slow rate of $2\,^0C$ per minute over a duration of about 2 hours is called the bake-out stage or the stage where the organic materials burnout. At the temperature of $850\,^0C$, the glass granules melt and encapsulate the ceramic granules forming a homogeneous structure (see figure 2.5b) across all individual layers[81].



(a) Ferro A6 Bake Out and Firing Profile [2]



(b) Binding as Glass Melts in LTCC Glass Ceramic Structure

Figure 2.5: LTCC Bake Out and Firing Profile

Organic material constitute about 15 percent of the total composition of LTCC green tape [81]. The fired ceramic also undergoes shrinkage in both the x-y direction and in the z-direction. The burning out of the organic material results in a proportional shrinkage in the overall dimensions of the LTCC structure in all three dimensions. The estimated shrinkage for specific LTCC tape is usually provided in the substrate data sheets.

2.2.2 LTCC Limitations

LTCC has a couple of drawbacks, some of those being [3]:

- Metallisation is screen printed giving limited definition compared to thin film
- Substrate is not polished and poor surface roughness can result in higher losses
- Care must be taken during the design process to avoid substrate warping
- The process is more expensive than multi-layer laminate processes like LCP manufacturing
- Processing lead times are longer than multi-layer laminate processes

Although LTCC has a thermal conductivity that is higher than organic laminate materials, its thermal conductivity is still lower than would be desired for MCM designs that need to dissipate many watts of power. The package must be able to conduct and spread the heat to maintain product reliability [4].

2.3 Printed Circuit Boards (PCB)

A properly designed PCB stackup can improve manufacturability of a circuit.

Multilayered PCB designs that utilise high performance materials present more fabrication challenges than standard epoxy glass FR4. This is due to significant material differences between the two types of PCB materials. High performance materials usually require higher processing temperatures and require special surface treatments to facilitate proper hole and surface plating. They also possess different expansion properties making layer-to-layer registration more difficult to control.

Like with other manufacturing technologies, PCB circuits are designed while considering the limits and guidelines of manufacturing and the capabilities of the chosen manufacturer. It is easy for a designer to come up with a complex circuit that operates well within a software environment, but it can be impractical to build if the circuit does not comply with PCB manufacturing fundamentals.

In this section, some common design problems are outlined.

2.3.1 PCB Multilayer Manufacturing Process

In preparation for manufacturing, the designer prepares the layout and converts the data into a format requested by the manufacturer. The PCB industry has developed a standard output format which defines the copper tracking layers as well as the solder masks and component notations.

The manufacturer then checks the data to confirm that the track widths, the space between tracks, the copper pads around holes and hole sizes, among other aspects, meet the manufacturing requirements. The files are then converted to tool files needed to drive machines that make and test the PCB.

The masks or films used to image the circuit patterns on the PCB are then prepared. Once this is done, precise registration holes are punched into each sheet of the films. These registration holes aid in ensuring perfect alignment of different PCB layers when stacking them up.

The PCB laminates usually come either with a single clad of copper or double cladding (with copper foil pre-bonded on each side). Before imaging the laminates, the copper is cleaned. Then, in a clean room, the cleaned panel of laminate is coated with a layer of photo-sensistive film called photo resist.

To transfer the patterns of the inner layers on both sides of a doubly-clad panel, the operator loads the film with the first pattern onto a printer. The bed of the printer often has registration pins that match the registration holes in the films. The panel coated with photo resist is then loaded, and the film with the pattern for the other side of the panel. The printer uses powerful UV lamps to harden the photo resist through the clear parts of the film. By doing this, the copper pattern is defined. The areas under the black parts of the film remain unhardened.

The next step is to spray the panel with a powerful alkali solution which removes the unhardened photo resist.

The panel is then pressure-washed and dried leaving the desired copper pattern covered under the hardened resist. Unwanted copper can now be etched away using a powerful alkaline solution to dissolve the exposed copper. The process is carefully controlled to achieve conductor widths matching those used for the simulated design.

Once the operator has confirmed that all unwanted copper has been etched away, the hardened photo resist is stripped off exposing the desired copper pattern.

The process of forming the patterns on the panel is depicted in figure 2.6.

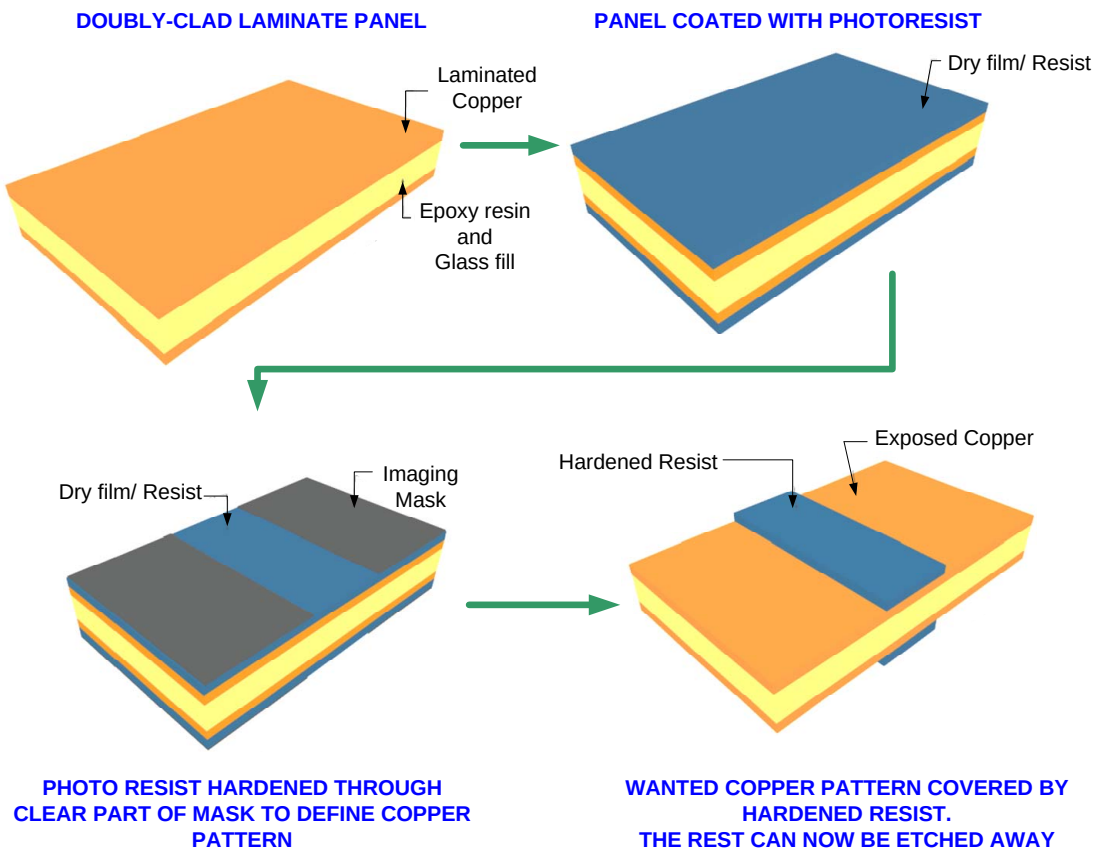


Figure 2.6: Copper Pattern formation on PCB Panel

The next step is then to punch registration holes on the panels that are used to align the inner stack-up layers to the outer layers.

After this, the layers are aligned and laminated. Lamination is achieved by means of bonding the layers to each other following a specific pressure and temperature profile. For the polytetrafluoroethylene (PTFE) based PCB laminates, there are three general types of bonding systems: thermoplastic films, thermoset prepregs and direct bonding.

Thermoplastic Films

This is the most commonly used of the three options. A thermoplastic film with a lower melting point than the core layers is interleaved between every two core layers. The assembly is then clamped to press the layers together. The assembly is then heated under uniform pressure. Once the melting point of the thermoplastic film is surpassed, the film flows laterally and fills between the copper features, under the uniformly applied pressure. This causes the different layers to bond together. Examples of thermoplastic bonding films are Rogers 3001 and Dupont Fluorinated Ethylene Propylene (FEP). Rogers recommends the bonding cycle in figure 2.7 for Rogers 3001 bonded stack-ups.

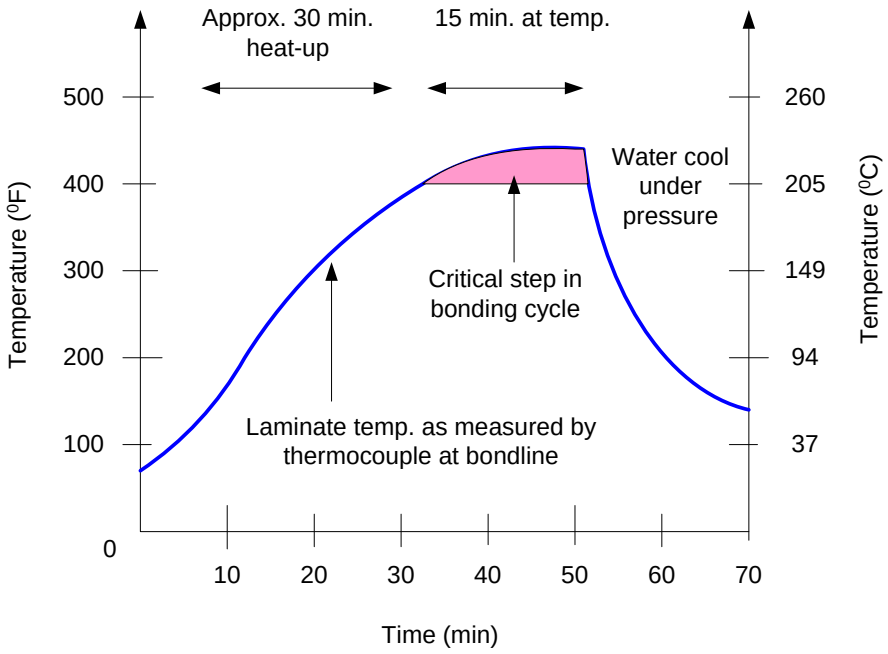


Figure 2.7: Recommended Bonding Profile for Rogers 3001.

Thermoset Prepregs

A prepreg (from pre-impregnated) is a fibreglass that is pre-impregnated with pre-dried but unhardened resin. Prepregs can also be defined as fibreglass strengthened by an adhesive layer (similar to FR4 material) [5].

For a recommended bonding profile, the lamination process is similar to that of a thermoplastic film, with the thermoset prepregs interleaved with the core layers. These are mostly used in mixed constructions where FR4 and PTFE based laminated are bonded together [6]. Thermoset prepregs traditionally have lower melting temperatures than the PTFE core laminates.

Direct Bonding

This method, also referred to as fusion bonding, can be more difficult than the former two. It omits the film in the assembly and requires temperatures above the melting point of the core material to directly fuse together the softened PTFE surfaces. This method requires careful control of the clamp stress as well as the high temperature press capability.

Selection of a suitable bonding system is dependent on the final application, available lamination equipment and subsequent post lamination thermal exposures of the bonded assembly.

After lamination, holes are drilled into the structure for attachment of leaded components and to serve as via holes connecting copper layers together.

Next, the copper patterns on the outer layers are etched in a process similar to the one that was used for inner layers.

Following this step, the structure is copper plated. The plated panels are then tested to ensure that the copper plating is the correct thickness.

The multilayer PCB production process ends with the electrical testing of the PCB against original board data.

2.3.2 Common Design Problems

2.3.2.1 Poor Material Choice

When choosing a material for an electrical design, several material properties are usually considered. Among those are the dissipation factor, the dielectric constant, coefficient of thermal expansion, thermal conductivity, dimensional stability and the smoothness of the copper finish.

From a design point of view, a material with a low dissipation factor is preferable to minimise dielectric losses. However, from a manufacturing perspective, materials with the lowest dissipation factors tend to be the most difficult to build [7]. They can also drive up the manufacturing costs of a multilayer construction and minimise the material supplier base.

The dielectric constant, on the other hand, can be impacted by moisture and can also be affected by temperature changes. Moisture absorption can cause the effective dielectric constant to vary dramatically. Materials that absorb moisture also tend to be susceptible to absorption of other chemicals during the fabrication process. Very low moisture absorption is preferable for critical applications. Teflon/PTFE is known to be less vulnerable to moisture than ceramic-loaded substrates and polymides. It is also important to select a material which does not have a dielectric constant that changes dramatically with temperature. Such materials can cause performance issues that are difficult to isolate.

The coefficient of thermal expansion (CTE) becomes an important property when stacking up materials with different expansion rates. To prevent fabrication problems and to ensure design reliability, it is recommended that stacked materials have CTE that do not differ greatly.

The quality of the surface finish is very important at high frequencies where conductive losses due to skin effect are a significant component of overall loss. For such applications, a smooth surface finish should be chosen.

2.3.2.2 Losses in the Signal Path

The total loss in a signal path is a combination of four components namely conductor loss, dielectric loss, radiation loss and design-induced loss.

Conductor losses result from resistance of the conducting metallic signal and paths and can be minimised by ensuring a smooth surface finish.

Dielectric losses are contributed by the dielectric material and can be reduced by choosing materials with low loss tangent.

Radiation losses are due to the type of transmission lines, for example, microstrip lines have more radiation losses than co-planar waveguides and striplines have even less.

Design-induced losses are associated with discontinuities on the signal paths. These can be minimised by ensuring better transitioning between different types of lines.

2.3.2.3 Impractical Stack-Ups

At times a fabricator can receive data that specifies a stack-up that is not practical to build. The design might have components that require specialised fabrication techniques that a manufacturer does not have the ability to fabricate. to avoid this, it is better for a designer to consult with a manufacturer, prior to design, if unsure of such aspects.

2.3.2.4 Stack-Up Symmetry

It is important to strive to achieve a near symmetrical distribution of the elements that make up a stack-up design. This symmetry should be maintained about the PCB center plane and should aim to achieve a balance based on both material type and thickness.

Unbalanced stack-ups can result in fabrication deformities such as warpage and cracked barrels of plated through-holes due to possible added stress. As a result, fabrication yields can be impacted negatively.

2.3.2.5 Distribution and Use of Blind and Buried Vias

It is common for designers to design a stack-up with a combination of blind and buried vias that is impractical from a manufacturing perspective. To avoid redesign and to manage fabrication costs more effectively, it is advisable to consult with a fabricator prior to design.

2.3.2.6 Unrealistic Tolerances

Designers often aim to achieve the best performance possible by working with dimensions specified to a number of decimals. They then specify very tight tolerances for the manufacturing process that can be unachievable because manufacturer's equipment may not have adequate capabilities.

To avoid delays and possible additional cost implications of such unnecessary delays, it is recommended that designers get familiar with the capabilities of chosen fabricators prior to design.

2.3.2.7 Hole Aspect Ratios

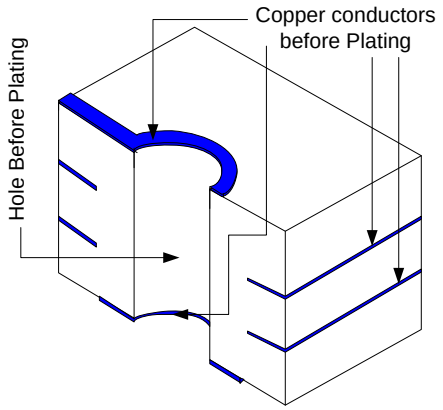
It is important for a designer to find out the acceptable hole size to PCB thickness ratio and to keep this in mind throughout the design process.

2.3.2.8 Hole-to-Conductor Clearance

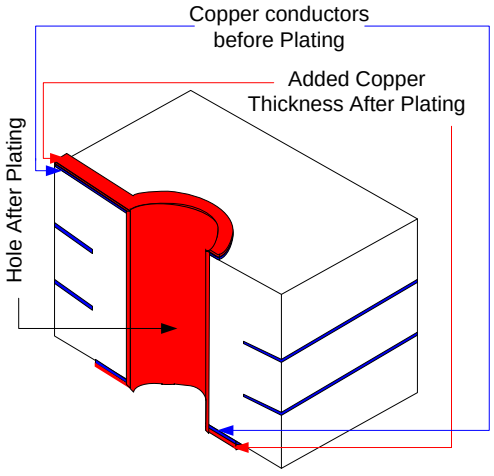
Hole-to-copper features should not be tightly placed and minimum clearances are often specified for certain materials. It is important for designers to familiarise themselves with all dimensional and component distribution guidelines and recommendations.

2.3.2.9 Added Copper Thickness After Plating

Often, the measured results of a component differ from those of the simulated structure. One of the reasons for this can be that a designer does not account for additional copper thickness after the conductors are plated. When plating drilled through holes, for instance, an entire board is immersed into the plating chemical bath and in addition to plating the hole, the plating also gets added on the outer surfaces. This is illustrated in figure 2.8. The blue parts are the copper tracks existing prior to plating and the red parts show the additional deposited copper thickeness after the plating process.



(a) Before Plating



(b) After Plating

Figure 2.8: Additional Copper Thickness Due to Plating

If the surface tracks are made of a copper cladding of 0.017 mm and a plating of approximately 0.025 to 0.030 mm is added, then the conductors could end up being approximately 0.040 - 0.042 mm thick. If this is not accounted for in the simulations, then measured results of the manufactured product can differ from those of the simulation.

2.4 Liquid Crystalline Polymer (LCP)

LCP is a relatively new thermoplastic polymer material with barrier properties similar to those of ceramic crystal [73]. It is made of aligned molecule chains with crystal-like spatial regularity[63]. Pham et. al. [73] refer to it as a 'Holy Grail' which could hold the key to a packaging revolution.

Since its introduction to the microwave world just over a decade and a half ago, LCP has become very attractive as a substrate and as a packaging material due to its unique electrical and mechanical properties [81]. Being a plastic, the cost of processing LCP is low. It exhibits low electrical losses, it is near-hermetic, and has low moisture absorption and mechanical flexibility properties because of its crystal properties [73]. When LCP is heated to its liquid crystal state, rigid segments of the molecules align next to one another in the direction of shear flow, a structure which persists even after the LCP is cooled to temperatures below the melting point; the unique electrical and strong mechanical and chemical properties result from this uniform makeup [63]. Its flexibility has enabled the emergence of conformal electronics. Sensors and communication devices can be fabricated on LCP and integrated onto fabric for use in military uniforms or personal health monitoring systems [63]. Antenna arrays have also been designed and fabricated on LCP [26] and in some instances bent into a cylindrical shape [57]. The ability to wrap electronics around curved surfaces opens the door for many more improvements in modern systems. Low loss integrated waveguide passive circuits have also been fabricated in LCP [92].

At high frequencies, LCP competes with ceramic materials like alumina and LTCC. However, LCP has the advantage of costing less and having lower melting temperatures that make it possible to embed devices that are sensitive to high temperature. LCP also has dielectric stability from DC to 110 GHz which makes it applicable to almost every consumer and military frequency band [63]. However, LCP cannot match the hermetic properties of the ceramic substrates.

Among the other advantages of LCP are [63]:

- It is light weight. It has a density of 1.4 g/cm^3 making it 40 percent lighter than silicon, 65 percent lighter than alumina and 30 percent lighter than FR4. This makes LCP well suited for air and space-borne applications.
- It is radiation resistant. It resists the harmful effects of radiation making it advantageous for space-borne applications.
- Thickness variety with sheets as thin as 25 µm . This makes LCP ideal for antenna applications where the substrate thickness is determined by the tradeoff between wide bandwidth and low profile.
- It has a high dielectric strength of approximately 21.65 MV/m making it suitable for high voltage and high power devices.
- It is easy to process. It can easily be laser cut or plasma processed and can also be drilled and machined with ease.

- Its low permittivity of approximately 3 makes it advantageous for packaging.
- It maintains constant permittivity even in humid environments.
- It also has a customised CTE; the CTE can be tuned by changing the chemical formula with values ranging from 3 to 30 ppm/^{0}C. However, standard CTE is 17 ppm/^{0}C to match that of copper. This is also closer to the CTE range of commonly used PCB materials making the match between LCP and PCB better than that of LTCC (5.5 to 8.0 in table 2.2) and PCB (see table 2.1).
- It has good chemical resistance and can therefore withstand prolonged exposures to harsh chemicals, even under high temperatures.

2.4.1 LCP Manufacturing Process

The LCP fabrication process begins with the cutting on the tape into the required sizes. It is important to do this in a dark room because the sheets are usually covered in photo resist. These pieces are then exposed and the photo resist is removed using a photo resist stripper solution leaving only the desired pattern on the substrate pieces. It is important to ensure that all of the photo resist material is removed after the etching and stripping processes. The drilling of the via holes using laser can then be done. The film pieces are cleaned and dried in an oven for about 2 hours at a recommended temperature of 125 ^{0}C. The dried pieces are stacked together vertically, alternating between the core films and the bonding films as shown in figure 2.9 and are aligned using an alignment fixture.

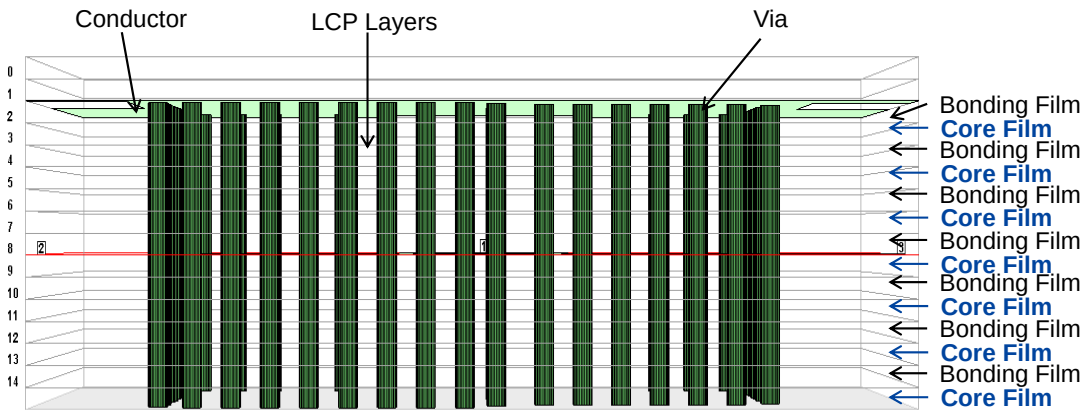


Figure 2.9: Multilayer LCP Films Arrangement

The process that follows is the lamination process during which the layers of LCP are pressed together at a defined temperature and pressure over defined periods of time. Rogers offers two inhomogeneous LCP substrate material, one used as the core film (Rogers ULTRALAM 3850)

and the other (Rogers ULTRALAM 3908) as the bonding film. These two materials have identical electrical and mechanical properties, but have different melting temperatures; the bonding ply melts at a temperature of 280^0C while the core film melts at 315^0C hence allowing the bonding ply to melt at temperatures above its melting point but below the melting point of the core film, resulting in the chemical bonding of the solid core film layers. A properly done lamination results in a structure that is nicely compact and cannot be separated. Lamination should be done carefully, avoiding dusty surfaces so that there are no undesired inclusions in between the layers.

When cavities are required, cavity cut-outs are made in the films - both core and bonding - prior to the lamination process.

2.4.2 Limitations of Liquid Crystal Polymer (LCP)

Being a polymer, LCP cannot be truly hermetic. The material itself absorbs very little moisture and micro-cracks in LCP packages are effective at repelling liquid, but not moisture (such as vapour), hence being referred to as being near-hermetic [63].

Although LCP has been used for over a decade and a half, it is still considered a new material and is still experimental in many aspects.

As an organic material, LCP is sensitive to strong bases. A piece of it can, for example, be dissolved if exposed to photo resist remover with a pH of 12 in less than 24 hours if heated to 60 ^{0}C [63]. LCP is however chemically resistant to acids.

It also has poor thermal conductivity, so any heat generated within an LCP package will not dissipate quickly. However, it also provides a thermal barrier to any heat sources outside of the LCP package. This can therefore either be an advantage or a disadvantage depending on the application.

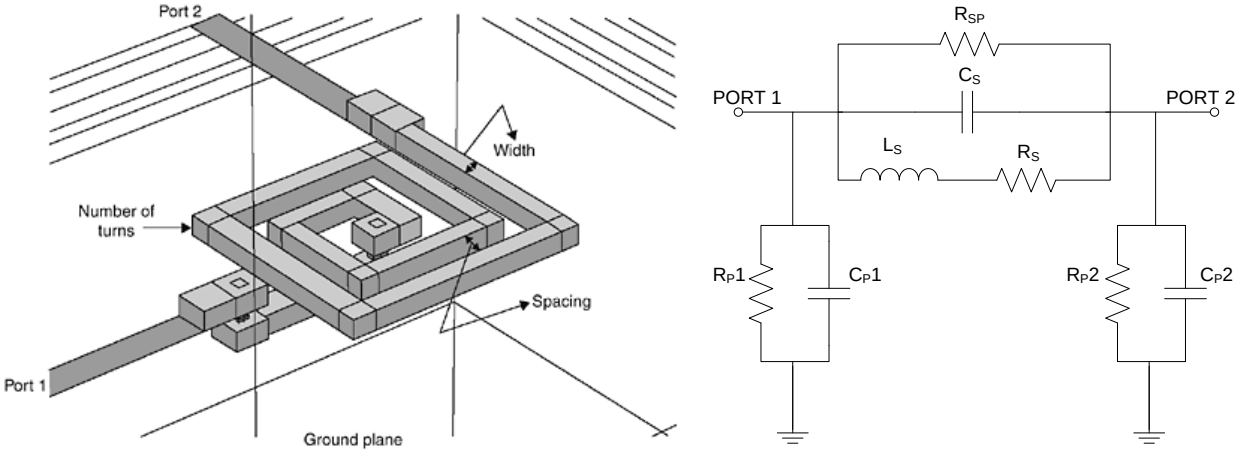
LCP has a natural surface roughness of a couple of microns [63]. Polishing is therefore required for applications that require smoother surfaces.

2.5 Embedded Components

The ability to embed discrete passive components using the concept of lumped elements within the layers of multi-layered ceramic and laminate structures has greatly improved the levels on miniaturisation that can be achieved in electronics. However, with the reduction of horizontal footprint comes the disadvantage of increased parasitics. In cases where parasitics to ground are undesirable, placement of the structure at a distance from the ground plane(s) results in values of parasitic reactances that are negligible. Ground planes can also be trimmed off for such sections as long as it does not affect the design. It is also possible to minimise the effects of parasitics by designing the passive elements so that they occupy more than one layer e.g. a multi-layered spiral inductor or a multi-layered parallel plate capacitor.

Figure 2.10 shows a two port spiral inductor implemented between layers of substrate and its equivalent electrical circuit. L_S is the total inductance, R_S is the series resistance and C_S represents the coupling capacitance between the input and output ports. The capacitance to ground

is represented as C_P1 and C_P2 and the dielectric loss as R_P1 and R_P2. Resistor R_{SP}'s role is the optimisation of the circuit model based on the simulated and measured data.



(a) Embedded Inductor [8] (b) Equivalent Circuit of Inductor [8]

Figure 2.10: Embedded Inductor and its Equivalent Circuit

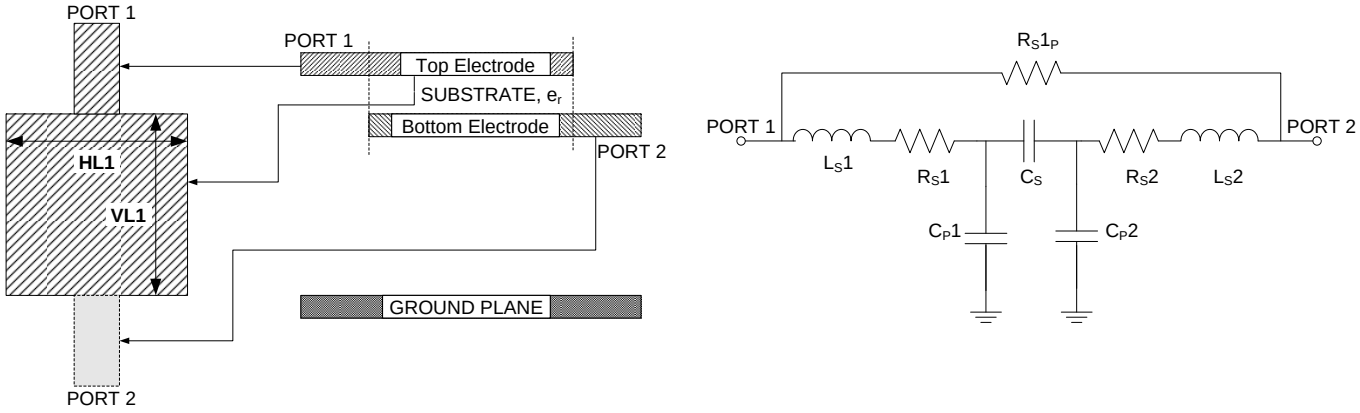
The effective inductance and the Q-factor of the two port model circuit model are computed as [8]:

$$L_{eff} = \text{Imag}\left(\frac{1}{2\pi f Y_{nn}}\right) \quad n = 1, 2 \tag{2.1}$$

$$Q = \left|\frac{\text{Imag}\,(Y_{nn})}{\text{Real}\,(Y_{nn})}\right| \quad n = 1, 2 \tag{2.2}$$

where Y represents the admittance parameters at the ports and f is the frequency. The effective inductance changes as a function of frequency because of the parasitic capacitance.

An embedded parallel plate capacitor can be implemented with substrate layers as shown in figure 2.11 along with its equivalent two port electrical circuit model. The electrodes of the capacitor are placed at a substrate thickness apart at times using more than one layer to obtain the required thickness for a set effective surface area of the electrodes.



(a) Embedded Capacitor (b) Equivalent Circuit of Capacitor [8]

Figure 2.11: Embedded Capacitor and its Equivalent Circuit

Single metal layers can also be used to create interdigital capacitors but the parallel plate geometry is preferable due to its smaller size and minimisation of conductor loss. Additional electrodes can be strategically placed to increase the capacitance if necessary. C_S in the electrical equivalent circuit is the capacitance between the electrodes, C_P1 and C_P2 are parasitic capacitances to ground and L_S1 and L_S2 are the series inductances due to the electrode plates. The series resistance due to the electrode plates is represented as R_S1 and R_S2. These are due to conductor loss. The dielectric loss on the other hand is denoted R_S1_P. The effective capacitance and the Q of the capacitor are obtained as [8]:

$$C_{eff} = \left(\frac{1}{2\pi f \text{Imag}\left(\frac{1}{Y_{nn}}\right)} \right) \quad n = 1, 2 \tag{2.3}$$

$$Q = \left| \frac{\text{Imag}\left(Y_{nn}\right)}{\text{Real}\left(Y_{nn}\right)} \right| \quad n = 1, 2 \tag{2.4}$$

where Y represents the admittance parameters at the plane of the ports and f is the frequency. These values can also be obtained from simulation done in electromagnetic simulators.

Buried resistors are formed by depositing resistive paste in between two conducting pads as shown in figure 2.12 in the middle of substrate layers. Manufacturers of multilayered substrates usually provide information regarding the best resistive pastes that can integrate well with the chosen substrate. The pastes come with different resistivity values per square which aid in further miniaturisation upon proper choice of paste.

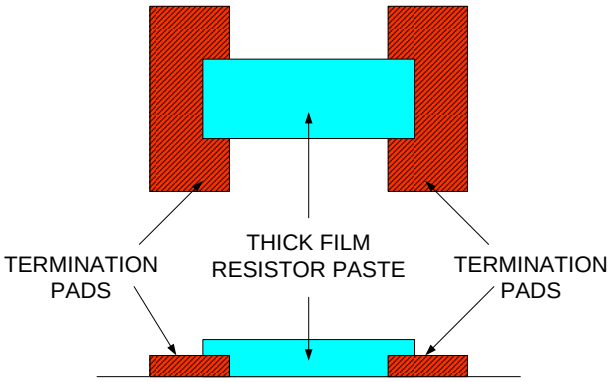


Figure 2.12: Buried Discrete Resistor

Table 2.3 shows a comparison of resistor paste properties between two ceramic material systems: DuPont and Ferro A6M.

COMPANY	Type	Surface Resistance, Ω/Square	Tolerance, %	Temperature coefficient of resistance, ppm/^{0}C
DuPont	CF011	10	±20	±200
	CF021	100	±20	±200
	CF031	1K	±20	±200
	CF041	10K	±20	±200
DuPont	HF010	10	±20	±150
	HF020	100	±20	±100
	HF030	1K	±20	±100
	HF040	10K	±20	±100
Dupont	2011B	10	±10	≤50 HTCR; ≤100 CTCR
	2021	100	±10	≤50 HTCR; ≤75 CTCR
	2031	1K	±10	≤50 HTCR; ≤75 CTCR
	2041	10K	±10	≤50 HTCR; ≤75 CTCR
	2051	100K	±10	≤50 HTCR; ≤75 CTCR
	2061	1M	±10	≤50 HTCR; ≤75 CTCR
	2071	10M	±20	≤125 HTCR; ≤100 CTCR
Ferro	87-011	10	±30	-
	87-101	100	±30	±450
	87-102	1K	±30	±200
	87-103	10K	±30	±200

Table 2.3: Resistive Paste Properties for DuPont and Ferro A6 Ceramic Material Systems [9, 10].

A detailed description of resistive pastes, design of both surface and buried film resistors and their design considerations can be found in [11].

2.6 LTCC, PCB and LCP in this Dissertation

Each of the multilayer technologies that has been presented is the preferred option for different applications. With LTCC, up to 50 layers can be stacked-up in a relatively reliable process creating much flexibility in design. For small scale manufacture, however, the process can be taxing and not as cost effective as the other two options. Manufacturing of LTCC circuits also requires more special expertise to carefully manage the fabrication process. LCP and other laminate PCB materials are relatively easier to manufacture, but are limited in the number of layers that can be assembled and in the complexity that can be achieved with the circuits. Most also require additional bonding ply or prepreg layers sandwiched in between core substrate layers which makes the lamination process

a bit challenging.

The LTCC designs in this dissertation use a 250 um (unfired thickness) Ferro A6M tape. In chapter 5, a three section polyphase filter is designed in LTCC with a passband frequency range of 100 MHz to 300 MHz and in chapter 6, a two-stage PIN diode power limiter is designed in LTCC and operated at a center frequency of 1.3 GHz with a bandwidth of 200 MHz. LTCC is chosen to first of all aid in the miniaturisation of these components and for ability to self-package (no need for a metallic housing to contain the electromagnetic energy). The Ferro LTCC materials used are: Ferro A6M tape which has a stable dielectric constant and loss tangent over a wide frequency range from DC to up to 100 GHz as shown in figure 2.13 and a resistive paste FX 87-102 for buried resistors with a resistance/square of 1000 ohms/square. The FX 87-102 unfortunately has high tolerances specification of +/- 30 percent as do all the resistive pastes that are recommended for the FERRO A6M tape. While following all the design rules specified for LTCC design using FERRO materials, a sensitivity analysis is also performed to note how the performance of the devices is affected by different parameters based on defined tolerances.

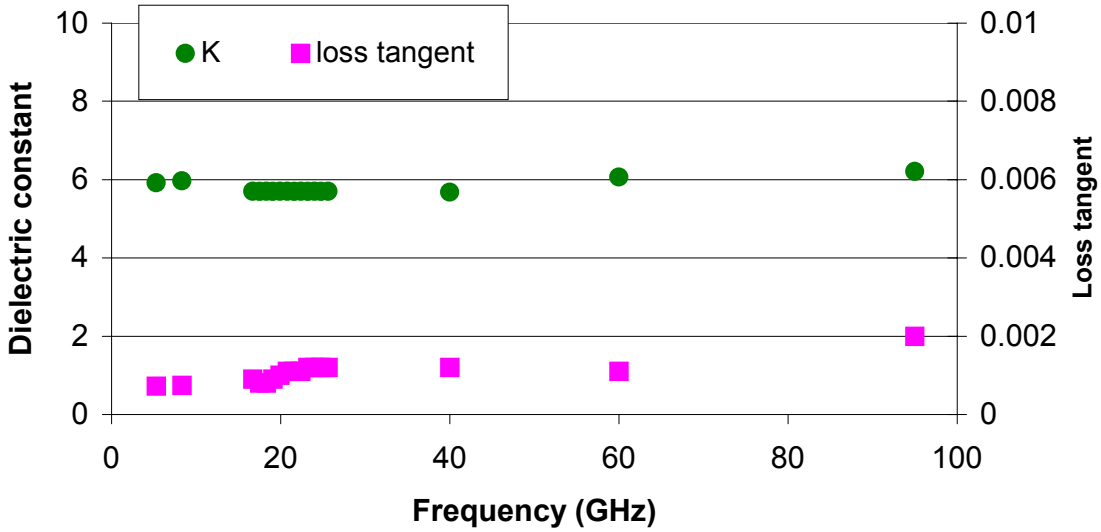


Figure 2.13: Dielectric Constant and Loss Tangent of Ferro A6 System [1]

Design rules for Ferro LTCC designs can be found in [2].

In chapter 3, a second order cross-slot coupled folded substrate integrated waveguide (FSIW) filter is designed in both LCP and Rogers 4003c, a PCB laminate material. Based on this filter, a diplexer is also designed.

Sandwiched in between vertically adjacent core layers of Rogers 4003c are Rogers 3001 layers which are used as bonding ply. These specific materials are chosen based on their low cost and availability is the local manufacturing companies. The multilayer fabrication process is also better

suited for these materials as opposed to higher dielectric constant materials like Rogers 6002 which tend to clog the drill bits when creating via holes.

Rogers ULTRALAM 3850 laminate circuit materials are used as highly temperature resistant LCP core dielectric films. These products were developed specifically for single layer and multilayer substrate constructions [12]. They are adhesive-less laminates that are well suited for high speed and high frequency applications in telecommunication network equipment, high speed computer data links and other high performance applications [12]. The circuits are characterised by low and stable dielectric constant and dielectric loss over a very wide frequency range from DC up to about 110 GHz [63]. These are important considerations for high frequency and high speed applications. ULTALAM 3850 comes in panels of double copper clad laminates. The Bonding film used is ULTALAM 3908. These materials also have reduced bake times and maintain stable electrical, mechanical and dimensional properties in humid environments. They are Halogen-free hence meeting the WEEE (Waste Electrical and Electronic Equipment) regulations.

Various 3D and 2.5 D electromagnetic software like SONNET now have these LTCC, PCB laminates and LCP materials incorporated into their material libraries.

2.7 Conclusion

This chapter set out to present and discuss characteristics of different multilayer circuit technologies which are employed in RF anf Microwave designs in chapters that follow. Other than the characteristics, the manufacturing process for each of the technologies has been outlined and the limitations associated with each have also been pointed out.

Chapter 3

SIW Diplexer in PCB Laminates

3.1 Introduction

At microwave and millimeter wave frequencies, one of the challenges encountered in circuit design is the realisation of low-loss devices with high quality factors. At these frequencies, planar circuits are fundamentally limited in performance, as conductor losses for these circuits increases with frequency thereby decreasing the quality factor. A better option is to use non-planar structures such as metallic waveguides which have higher quality factors. Conventional metallic waveguides, however, despite having high power handling capability and high quality factors, are bulky.

Hybrid integration of microwave and millimeter wave circuits offers a compromise between the types of technology and plays an important role in modern day communication systems. Therefore, it has become increasingly attractive to designers. A number of techniques for planar circuit integration with rectangular waveguides have been reported that are attractive for widespread applications [86]. These hybrid structures, however, posed the complication of finding and implementing the best suited transitions between the two platforms.

Over the years, dielectric waveguides were also developed, effectively reducing the size of the waveguide. The inherent losses due to the dielectric were small. However, they still received little attention because of high radiation losses due to discontinuities and difficult modal transition to planar circuits.

Subsequently, to address the problem of high radiation loss in dielectric waveguides, non-radiative dielectric (NRD) waveguide was proposed in [93]. In early designs incorporating NRDs, integration was achieved by inserting the planar sections directly into an air gap of the NRD guide along its axial propagation direction, causing a number of design and integration problems [86]. The solution to this problem came in the form of substrate integrated circuits (SICs) [87] which is a concept that allows for the waveguide to be synthesised within the same substrate on which the planar circuits are also made.

SICs have become popular in the design of low-cost and high quality factor passive circuits such as resonators, filters, couplers, power dividers, circulators and antennas. They can be used to synthesise all kinds of dielectric-based (or filled) waveguides by simply using holes (air-filled or

material-filled) and metallised holes. Among the different SIC platforms existent, the substrate integrated waveguide (SIW) platform is the most popular and most developed option. Several models have also been developed that define the different parameters of an SIW structure, using techniques used for conventional metallic waveguides.

This chapter presents the following contributions to SIW filter design:

1. A folded quarter-wavelength SIW structure with a slot used to split two resonant frequency modes. A crossed-slot is introduced for a better control of the position of a transmission null resulting from the slot-coupled topology.

2. A circuit model representation of the proposed structure to accurately model the characteristics of the structure in a circuit simulator.

3. A filter and diplexer using the proposed structure.

3.2 Substrate Integrated Waveguides (SIW)

Substrate Integrated Waveguides (SIW), also known as post-wall waveguides or laminated waveguides, are an interpretation of a conventional waveguide realised in the form of two periodic rows of vias connecting the top and the bottom ground planes on a dielectric substrate as shown in figure 3.1. In this way, a synthetic dielectric-filled rectangular metallic waveguide is constructed in planar form allowing for a complete integration of the waveguide with other planar transmission-line circuits. An inherent advantage that SIWs have over conventional waveguides is the size reduction by a factor of $1/\sqrt{\varepsilon_r}$, with ε_r as the relative dielectric constant. Furthermore, the waveguide height is typically only one substrate thickness.

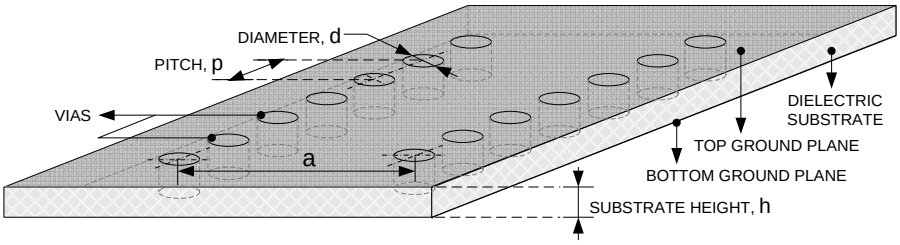


Figure 3.1: Substrate Integrated Waveguide (SIW)

SIW exhibit propagation characteristics similar to a classical/conventional waveguide [23]. Similarly, the field distributions of $TEn0$ modes of an SIW nearly coincide with those of a classical rectangular waveguide, with $n = 1, 2, \ldots$. TM modes, however, cannot exist in an SIW due to the presence of the gaps between the metal vias which form the effective walls of the guide; longitudinal

surface current causes radiation through the gaps which in turn prevents the propagation of TM modes [91]. Figures 3.2 and 3.3 illustrate the similarity in electric and magnetic energy distribution within a conventional rectangular waveguide cavity and an SIW cavity for the $TE10$ mode. The location of the vias for the SIW is marked by the dashed white rectangles for respective fields.

The cutoff frequency of an SIW is is defined as [23]

$$f_c = \frac{c}{2\sqrt{\varepsilon_r}} \left(a - \frac{d^2}{0.95p} \right)^{-1} \tag{3.1}$$

where c is the speed of light in a vacuum, ε_r is the relative dielectric constant of the substrate, d is the diameter of the vias, p is the longitudinal spacing between the vias and a is the transverse spacing between the two rows of vias as shown in figure 3.1. The accuracy of the formula is $\pm 5\%$ and is valid for [23]

$$p < \frac{\lambda_0}{2\sqrt{\varepsilon_r}} \quad ; d < p < 4d \tag{3.2}$$

where λ_0 is the wavelength in free space.

The dimensions of the via parameters p and d must, in addition be chosen to minimise the radiation loss as well as the return loss [40]. A parametric study of the relation between p and d and the resultant effect on the insertion loss primarily due to radiation is presented in [40]. The authors show that the pitch size must be small in order to reduce the radiation loss, but since the diameter of the posts also has an effect on the overall loss, a ratio between the two is considered as a better approach to approximate dimensions for the via-walls. In [39], it is recommended, that for negligible radiation losses, the dimensions be chosen as follows

$$d < \frac{\lambda_g}{5} \tag{3.3}$$

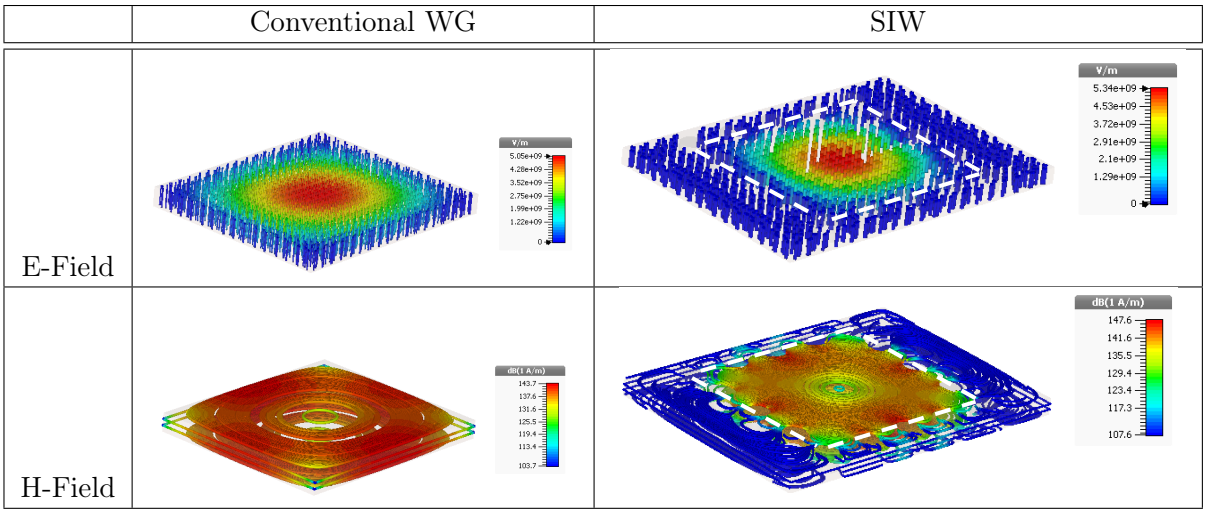
$$d < p < 2d \tag{3.4}$$

where λ_g is the guide wavelength.

For faster and less complex modelling of an SIW structure, it is usually easier to work with a rectangular waveguide whose modes exhibit the same propagation characteristics as those of an SIW and then to replace that with substrate integrated waveguides at a later stage of design. The equivalent width of the rectangular waveguide, denoted a_{eff} here, relates to that of the SIW, a (see figure 3.1), as [23]

$$a_{eff} = a - \frac{d^2}{0.95p} \tag{3.5}$$

This formula also holds only under the conditions of equation 3.2 and the physical explanation relies on the idea that due to the finite size of the metal vias, the fields in the SIW are confined to a region whose width is narrower than the dimension a.



(a) $TE101$ E- and H-Field Lines

Figure 3.2: Electric and Magnetic Field Lines for TE_{101} in a Conventional Rectangular Cavity and in a closed Rectangular SIW cavity.

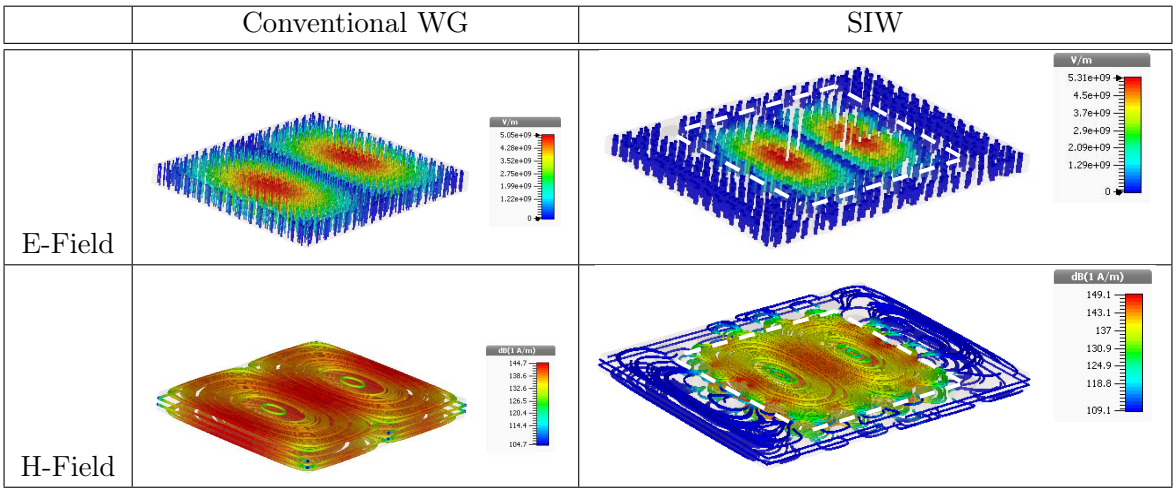


Figure 3.3: Electric and Magnetic Field Lines for $TE102$ Mode in a Conventional Rectangular Cavity and in a closed Rectangular SIW cavity.

SIW components have become increasingly popular due to their ease of design, relatively simple fabrication (depending on the fabrication media) and the advantages that emanate from combining the favourable properties of planar and rectangular waveguides. They are also compact, light-weight and cost-effective depending on which technology is used for the implementation and fabrication of the designs. SIWs can also be implemented in multilayered structures creating even greater design

flexibility. These advantages have to be weighed primarily against the increase in losses compared to normal waveguide.

One of the first reported SIWs dates back to 1998 and was referred to as a 'laminated waveguide' [80] owing to the fact that the waveguide was manufactured using lamination technologies. Since then, a number of passive and active components have been designed using SIW. Among those are different topologies of filters, including a 3-pole chebyshev filter centered at 26 GHz with inductive posts and constructed in RT/Duroid 5880 substrate [40], and a millimeter-wave 62 GHz filter fabricated in alumina for its high dielectric constant property. Design of filters implemented in circular SIW cavities to investigate the optimal angle for placement of input and output ports is reported in [79]. In [32], negative coupling is investigated in K-Band filters designed with source-load coupling to achieve finite transmission zeros. A C-Band fourth-order elliptic filter with four folded multilayered SIW cavities is designed in [49] to realise positive and negative vertical coupling by strategically placing apertures between stacked resonators. This technology manages to reduce the footprint of the filter, miniaturising it by about half of what it would be with a single layered structure.

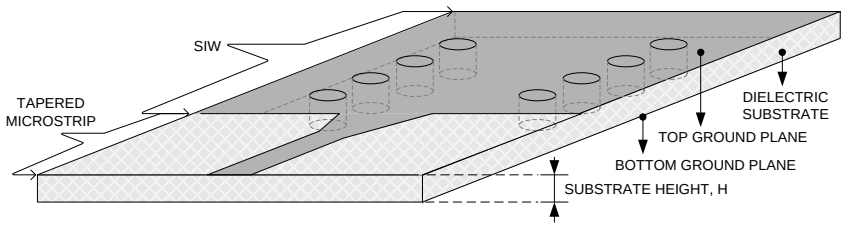
Other SIW miniaturisation techniques that have taken advantage of multilayered possibilities are variants of SIWs namely folded SIW (FSIW), half-mode SIW (HMSIW) and ridge SIW (RSIW). A number of publications have presented compact structures using these techniques. Among these are [44] in which an out-of-phase power division is achieved entirely with $\lambda/2$ folded substrate integrated waveguides and HMSIWs without using phase shifters. In [94], compact 3 dB double-slot and single-slot couplers are proposed and implemented in folded HMSIW further reducing the size from that of an HMSIW. Folded HMSIW are also used in [83] to design a varactor-loaded tunable phase shifter with varactor diodes loaded on the top metal surface of the folded HMSIW.

In [18], Hong et. al. use the folding technique to realise a quarter wavelength resonator filter based on a folded waveguide structure previously presented in [55], in which Hong demonstrates how standing waves in sectors of a $TE101$ rectangular cavity can be maintained by strategic folding of the structure. Whilst maintaining the footprint of a quarter-wavelength resonator, Hong et. al. demonstrate in [17] how a slot can be used to achieve a split mode response whilst maintaining the resonant frequency. The structure also introduces an interesting characteristic in the occurrence of a transmission zero which is controlled by varying the length and the width of the slot, achieving either positive and negative coupling in the process.

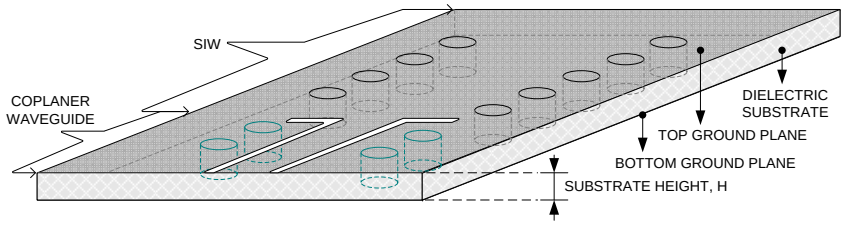
This factor is very useful in realising interesting filtering characteristics, one of which is explored in the design of a C-Band diplexer in section 3.8 of this chapter. This chapter also presents an extension of the work presented in [17], with the introduction of a cross-slot for more controlled variation of the position of the transmission zero. An accurate circuit model is derived based on the electromagnetic field properties of the filters to enable the modelling of the behaviour of the filter in circuit simulators. The filters realised using this cross-slot coupling technique are presented in section 3.5 and are in turn employed in the design of the diplexer in section 3.8.

3.3 SIW to Planar Structures Transition

An efficient transition between planar and non-planar structures is a key circuit element that ensures circuit and system integration. A number of solutions have been proposed in literature for this purpose, including microstrip to substrate integrated waveguide [37] and SIW to CPW with a ground plane added at the bottom of the substrate for a better match with the waveguide fields in the SIW [38]. These two examples are shown in figures 3.4a and 3.4b respectively. An additional row of vias (coloured teal in figure 3.4b) is added on each side of the grounded CPW (GCPW) to suppress unwanted parallel-plate modes which may cause resonance in the operating bandwidth.



(a)



(b)

Figure 3.4: Transitions from SIW to (a) Microstrip and (b) CPW-to-Ground

Substrate thickness plays an important role in determining how much losses are incurred in an integrated structure. The attenuation due to conductor losses for the $TE10$ mode in a waveguide (with the applied width as the equivalent width relative to an SIW, a_{eff}) is defined as [74]

$$\alpha_c = \frac{R_s}{a_{eff}^3 b\beta k\eta}\left(2b\pi^2 + a_{eff}^3 k^2\right) \quad Np/m \tag{3.6}$$

where R_s is the wall surface resistance given by [74]

$$R_s = \sqrt{\frac{\omega\mu}{2\sigma}} \tag{3.7}$$

and b is the substrate height (denoted h in figure 3.1), η is the intrinsic impedance of the dielectric material, β is the propagation constant which corresponds to a propagation mode when the wave number, k, is greater than the cut-off wave number, k_c. It is clear that loss is inversely proportional to b.

For this reason, substrate thickness should be increased in order to reduce the conductor losses in

a waveguide. However, for a microstrip line, radiation losses are proportional to substrate thickness and this can create integration problems between the two technologies. A possible solution for this problem is to use a multilayered microstrip line, making use of thinner substrate layers which are then laminated to form a thicker substrate thickness for the SIW. However, this topology increases manufacturing complexity, and also increases circuit sensitivity and production costs.

The performance of a CPW line is less susceptible to significant performance changes due to variations in substrate thickness. This makes CPW well suited for hybrid integration with SIW structures. When a ground plane is introduced on the other side of the substrate, the electric field lines of a CPW approximate those of a waveguide more closely and this allows for a better matched transition. This can be seen in figure 3.5 which shows electric field patterns at the interface of different transitions. Stripline to SIW transitions can also be utilised especially in folded SIW structures where the external coupling lines are connected to internal conductors [47, 17].

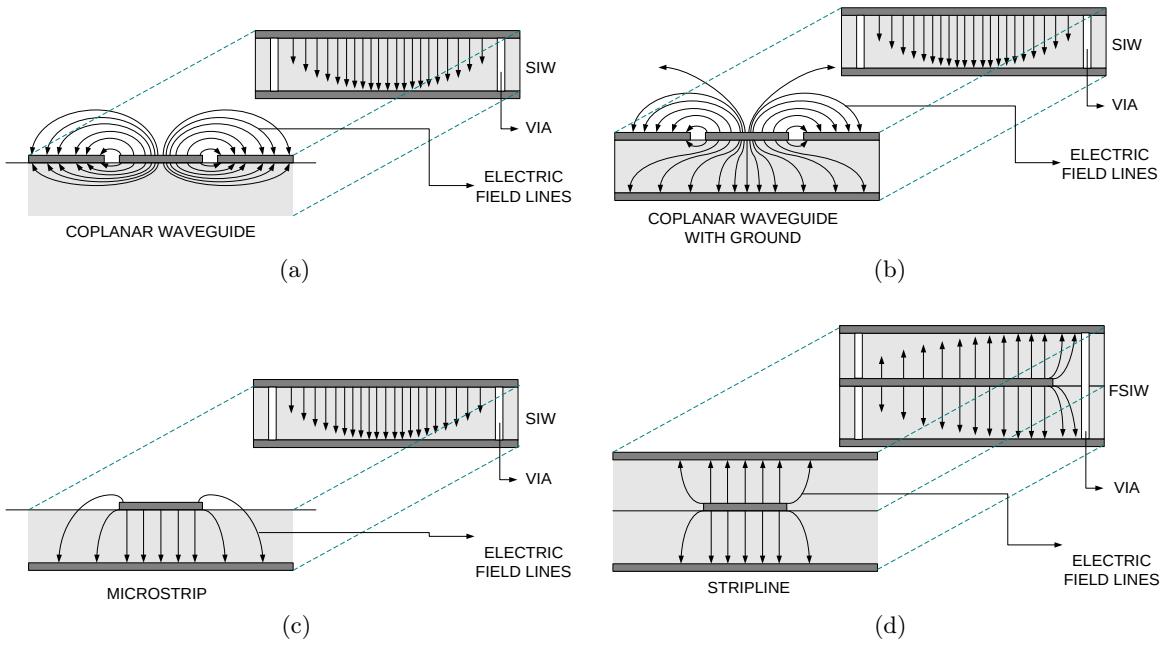


Figure 3.5: Electric Field Lines at the Interface of Transitions

A current probe transition from Grounded Coplanar waveguide to an SIW is reported in [41] and is shown in figure 3.6. The coupling to the SIW is achieved by using a metallic post (dark red in figure 3.6) through which current from the GCPW flows, thus creating a magnetic field. This field in turn couples to the TE_{10} magnetic field inside the SIW.

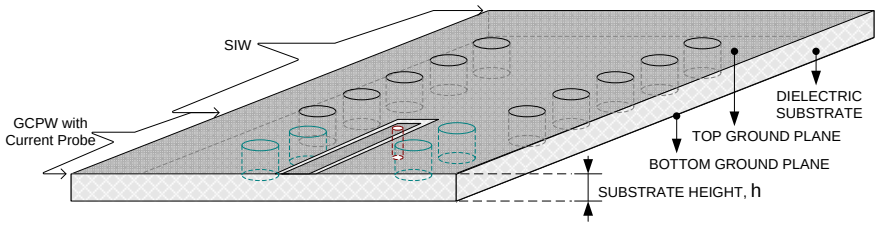


Figure 3.6: GCPW to SIW Current Probe Transition

The particular transition will be applied in designs in chapter 4.

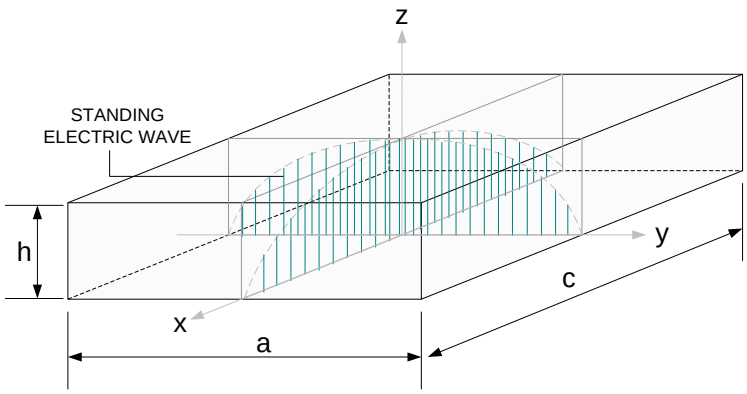
3.4 Folded Quarter Wavelength Resonator

Substrate-integrated waveguides (SIWs) offer a width reduction by the order of the square root of the substrate's dielectric constant in comparison to the size of a conventional air-filled waveguide. However, despite the favourable size reduction, for most wireless applications operating at low frequencies, SIW components still prove to be too large to be integrated in front-end modules. The capability to fold such structures along lines that maintain the integrity of the standing waves becomes advantageous in this instance.

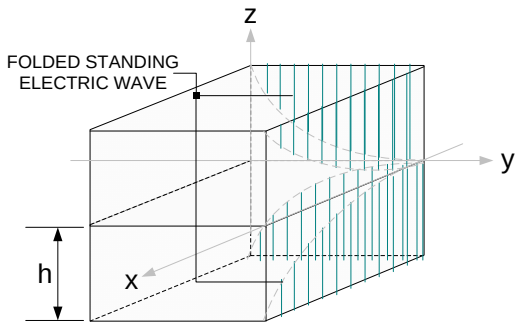
Folded waveguide resonators use the concept of folding standing waves of the dominant TE101 waveguide mode of a rectangular cavity resonator. In [17] Hong et. al present a slot-coupling technique that realises a second order filter response in a quarter wavelength resonator. The realised filter response is obtained from a structure that maintains the small dimensions of the quarter wavelength resonator.

A quarter-wavelength waveguide resonator has approximately 25% of the footprint of a conventional waveguide resonator. Figure 3.7a shows the distribution of standing waves in a normal waveguide and figure 3.7b illustrates how the standing waves are distributed within a quarter wavelength resonator. Figure 3.7c shows the implementation of the quarter-wavelength resonator as presented in [55] with a conducting plate inserted between two layers of dielectric material with two orthogonal slots open on sides of the common-plate to act as magnetic walls . These slots allow for electromagnetic fields to be transferred between the upper and lower sections of the guide. The folding technique is illustrated in figure 3.8. The rectangular cavity is folded along its x-axis realising a half wavelength form. A slot is introduced to the side to allow electromagnetic energy to be transferred between the top and bottom halves of the resonator. A green center-line in the third structure in figure 3.8 shows a symmetry axis along the y direction. The resonator is 'cut' at this point to obtain a quarter wavelength structure. To this, a slot is also introduced in the y-axis to realise the final implementation.

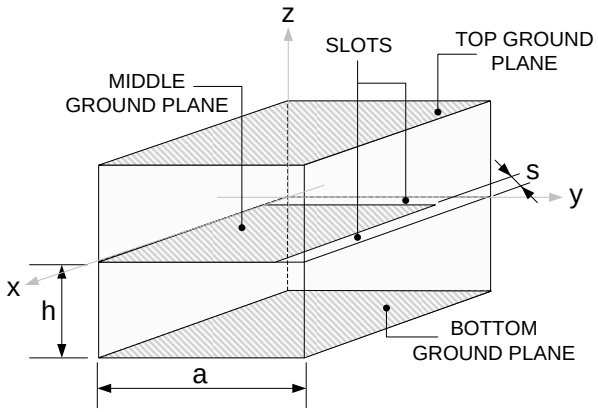
However, due to the asymmetric placing of the slots in the middle metallic plate relative to the centre of the quarter wavelength resonator,as shown in figure 3.7, an asymmetric distribution of the electromagnetic fields is expected and this is confirmed in with the simulated energy densities shown in figure 3.9.



(a) Standing Waves in a Waveguide



(b) Folded Standing Waves in a Quarter-wavelength waveguide



(c) Realisation of Folded Waveguide Quarter-Wavelength Resonator

Figure 3.7: Standing Waves and realisation of Quarter-wavelength Resonator

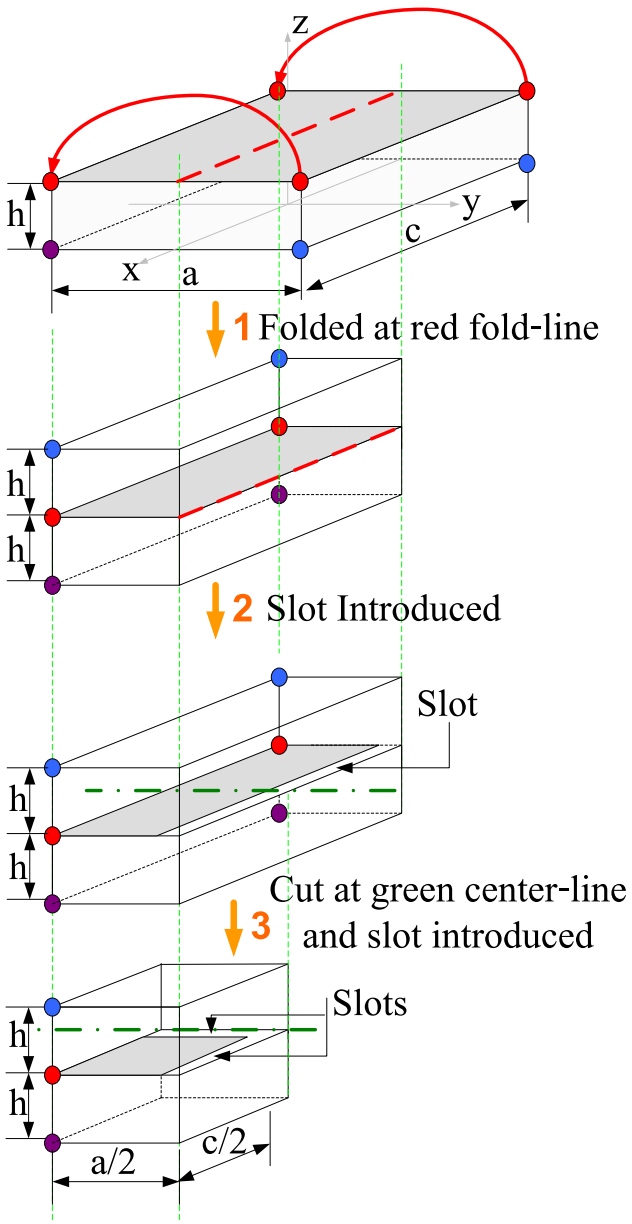


Figure 3.8: Folding steps to realise a quarter-wavelength cavity resonator

In comparison to the electromagnetic energy distribution of the conventional waveguide shown in figure 3.2, the distribution of both the electric and magnetic energy densities in the quarter wavelength resonator clearly has a pattern corresponding to one quadrant of the conventional resonator. The electric energy is strongest at the open corner of the middle plate of the folded waveguide resonator, which would correspond to the center of a conventional waveguide resonator. The magnetic energy is strongest at the shorted ends on the perpendicular slots. These are illustrated in figure 3.9.

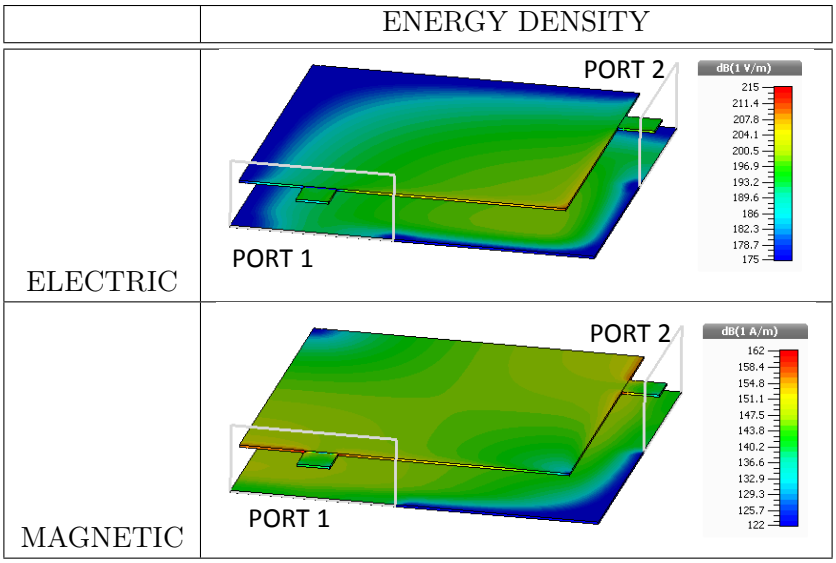


Figure 3.9: Electric and Magnetic Energy Densities in Quarter-wavelength Resonator

To feed the resonator, [55] proposes the use of stripline feedlines as shown in figure 3.9. The position of the stripline ports relative to the shorted ends of the middle plate, t (see figure 3.10c) determines the external quality factor . For a doubly loaded lossless resonator, the magnitude of the transmission coefficient relates to the external quality factor, Q_e, in the formula [54]

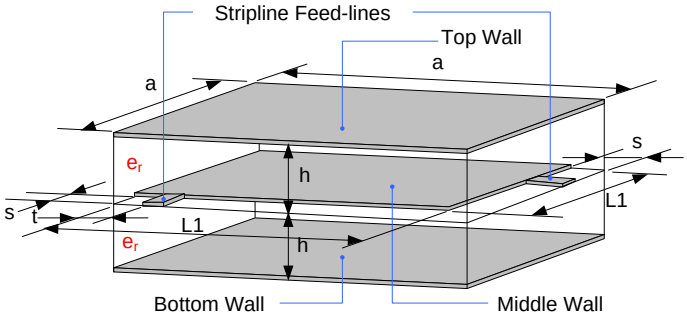
$$|S_{21}| = \frac{1}{\sqrt{1 + (Q_e \cdot {}^{\triangle\omega}/_{\omega_0})^2}} \tag{3.8}$$

The external quality factor in turn relates to the 3 dB bandwidth of a doubly loaded resonator in the equation [54]

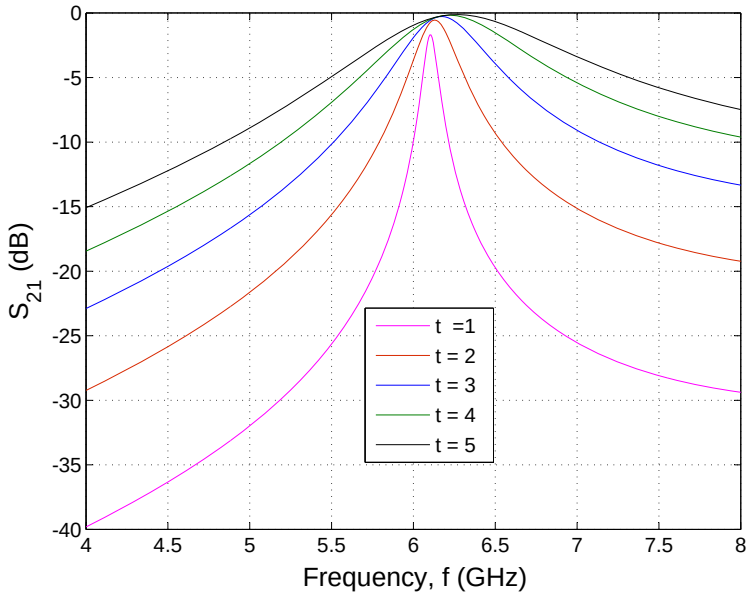
$$Q_e = \frac{\omega_0}{\triangle\omega_{3dB}} \tag{3.9}$$

for $Q_e \ll Q_u$.

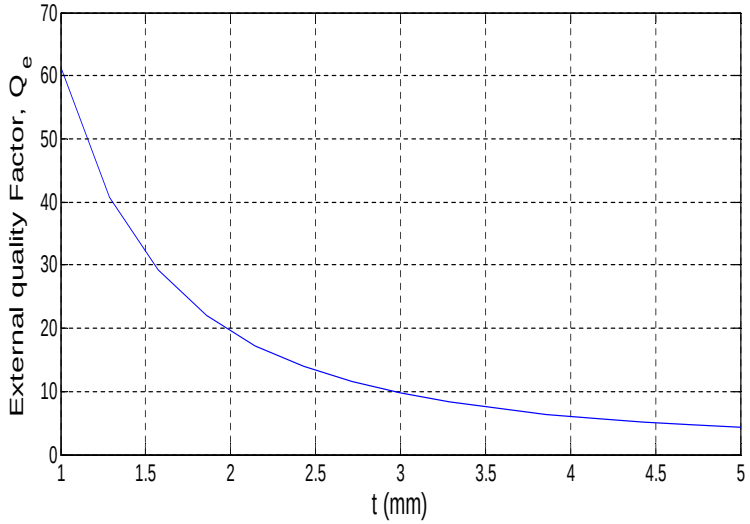
As an example, the variation of the external quality factor with the distance t, for a quarter wavelength square resonator (see figure 3.10a) using a substrate with a dielectric constant, $e_r = 3.55$, and a height, $h = 0.254\,mm$, is shown in figure 3.10c. The change in bandwidth and the insertion loss due to the variation in the distance t is depicted in figure 3.10b. The external quality factor decreases as the distance t increases and subsequently increases the 3 dB bandwidth while the insertion loss decreases.



(a) Quarter Wavelength Resonator with Stripline Feed-lines



(b) Change in Insertion Loss and Bandwidth due to a variation in t.

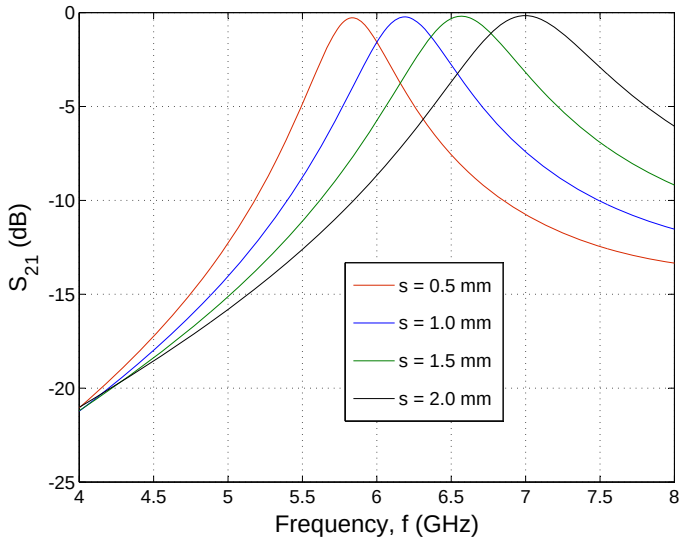


(c) External Quality Factor, Q_e, Versus t.

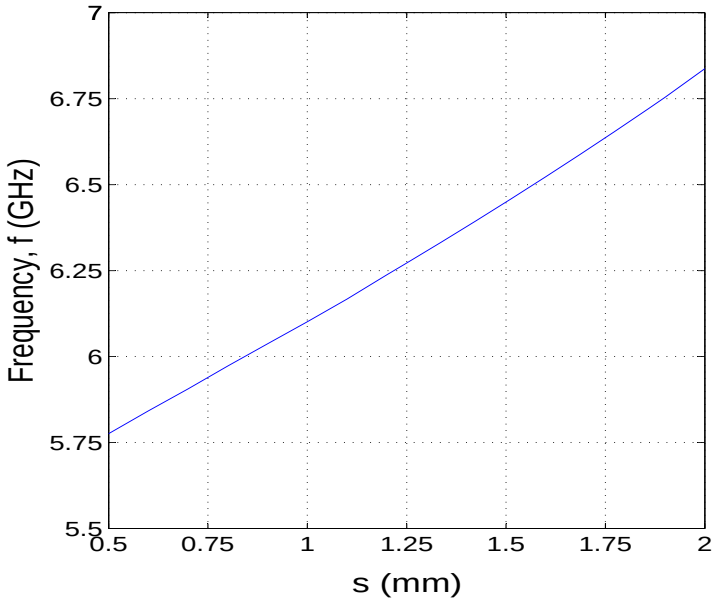
Figure 3.10: Effects of variation of t from $t = 1\,mm$ to $t = 5\,mm$; $a = 10\,mm$, $s = 1\,mm$, *and* $L1 = a - s = 9\,mm$; $e_r = 3.55$; $h = 0.254\,mm$

The other physical dimensions in figure 3.10c are the length of the folded waveguide a, the width of the slots s, and the length $L1$ which is the difference between the length a and the slot width s. For this simulation, the other physical dimensions were set to: $a = 10\,mm$, $s = 1\,mm$, *and* $L1 = a - s = 9\,mm$, for an unloaded resonant frequency, $f_0 = 6$GHz.

By decreasing the width of the slot s, and thereby increasing the length $L1$ (structure is a square and therefore symmetrical about the diagonal axis), the effective area of the middle plate overlapping with the top and bottom ground planes increases. This is in an area of high electric energy, and the increase in $L1$ results in an increase in the total capacitance within the guide and a subsequent increase in the amount of electric energy. Capacitance has inverse proportionality to the resonant frequency of the resonator; therefore, by making the width s smaller, the resonant frequency of the resonator can be decreased and vice versa. This property is shown in figure 3.11 for a change of s from 0.5 mm to 2 mm. For this simulation, the strip-lines for external coupling are placed at a distance $t = 3$ from the shorted edges on the middle plate.



(a)



(b)

Figure 3.11: Variation of slot width s with frequency f. [$s = 0.5\,mm$ *to* $s = 2.0\,mm$; $t = 3\,mm$; $a = 10\,mm$; $e_r = 3.55$; $h = 0.254\,mm$]

The next section discusses the application of the quarter wavelength resonator in filter design. Two slot coupling techniques are discussed in which slots are symmetrically placed along and across a diagonal division plane of a quarter wavelength FSIW resonator. The symmetrical division plane is shown in figure 3.13a and is denoted G-G'.

Section 3.5 analyses a quarter wavelength structure with a single diagonal slot introduced along the G-G' axis (see figure 3.13b). This structure was first proposed by Hong and Al-Otaibi in [17].

It has the advantage of realising a second order filter response whilst maintaining the dimensions of the quarter wavelength resonator.

In section 3.6, we propose the use of a cross-slot, placed perpendicular to the first diagonal slot to offer an alternative option for tuning the resonant frequency.

3.5 Single Slot-Coupled Folded SIW (FSIW) Resonator Filters

In this section, a single slot-coupled FSIW filter configuration shown in figure 3.13b is analysed in more detail than has previously been presented. The section presents an in depth analysis of the structure in terms of the interaction of the electromagnetic fields within the filter. The analysis sets a foundation for the explanation of the functioning of a proposed cross slot-coupled FSIW filter in section 3.6. Then in section 3.7, an equivalent lumped element circuit model is derived to aid in modelling the behaviour of both filters. A basic field analysis is presented in this section to observe the circuit behaviour in terms of electromagnetic fields within the structure.

The quarter wavelength structure discussed in this section uses a diagonal slot placed in the middle plate of the folded waveguide resonator to obtain a second order filter response. The slot enables the excitation of a pair of resonant modes resonating at the same frequency. The second-order slot-coupled filter has an asymmetric response and introduces some interesting characteristics. By varying the length of the slot as well as the width of the slot, the coupling between the two resonators can be varied. The filter response also shows the occurrence of a transmission zero, the position of which can be altered by varying the length or the width of the slot. Hong and Al-Otaibi [17] attribute the origin of this transmission zero to a complex coupling structure in which the load couples to the first resonator and the source couples to the second resonator as shown in figure 3.12. The two resonators are labelled 1 and 2, the source is denoted S and the load, L. The direct coupling between the resonators is denoted k_{12}, and the coupling between the source and the first and second resonators are named k_{S1} and k_{S2} respectively. The couplings between the load and the first and second resonators are named k_{L1} and k_{L2} respectively.

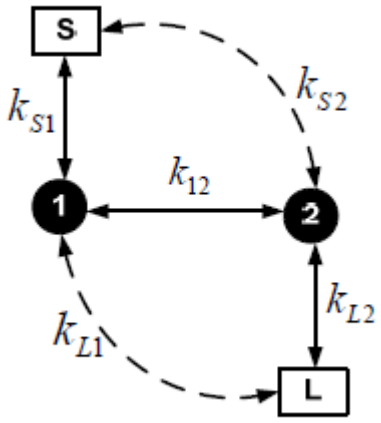


Figure 3.12: Coupling diagram describing the coupling mechanism in [17]

The $n+2$ coupling matrix , also referred to as an 'extended' coupling matrix for the filter is

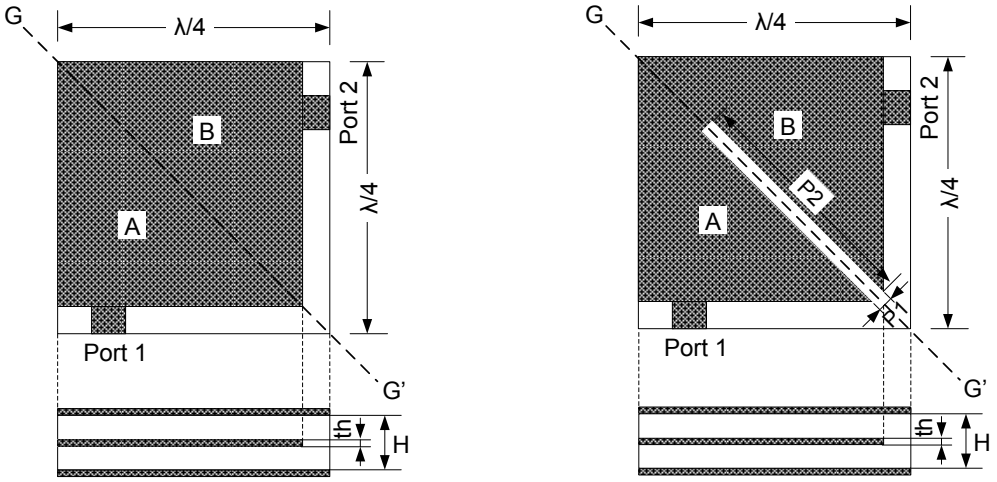
$$[m] = \begin{bmatrix} 0 & m_{S1} & m_{S2} & 0 \\ m_{1S} & 0 & m_{12} & m_{1L} \\ m_{2S} & m_{21} & 0 & m_{2L} \\ 0 & m_{L1} & m_{L2} & 0 \end{bmatrix} \tag{3.10}$$

where m_{xy} represent the coupling coefficients, k_{xy}, either between two resonators or between a resonator and the source or load, denormalised to the fractional bandwidth, FBW, i.e.

$$m_{xy} = k_{xy} \times FBW \tag{3.11}$$

This section along with sections 3.6 and 3.7 present an alternative theory to explain the coupling within the structure and to explain the origin of the transmission zero.

The analysis begins with the observation that the diagonal slot is placed in a position that divides the quarter wavelength FSIW resonator symmetrically along the symmetry plane marked G-G' in figures 3.13a and 3.13b. This way, the electromagnetic energy density (see figure 3.9) on either side of the slot is distributed symmetrically with respect to the slot. The view presented in these figures is of the middle metallic plate between two substrate layers of equal thickness. Stripline ports are used at the input and output of the structures.



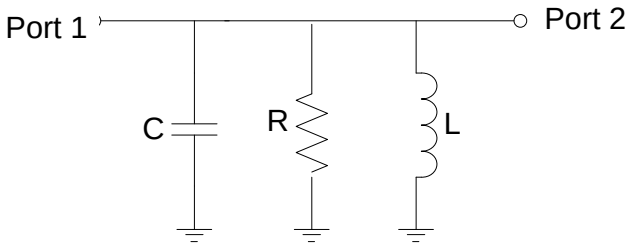
(a) Diagonal Symmetry of Quarter Wavelength Resonator

(b) Single Diagonal Slot configuration

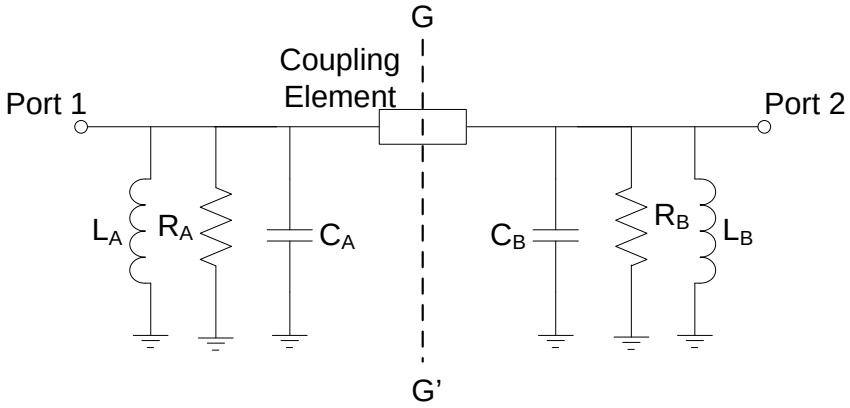
Figure 3.13: Quarter Wavelength FSIW Resonator and Second Order Filter

The quarter wavelength resonator can be represented as an equivalent lumped element circuit model shown in figure 3.14a. Owing to the electromagnetic energy symmetry about plane G-G', a circuit model that presents the two halves A and B (see figure 3.13a) as two separate halves and as individual resonant structures derived from figure 3.14a is shown in figure 3.14b. This then presents a possibility of achieving a second order filtering response if a suitable coupling structure is

introduced within the quarter wavelength FSIW resonator in a manner that maintains the energy symmetry. The diagonal slot in figure 3.13b does just that.



(a) Lumped Element Equivalent of FSIW Resonator



(b) Equivalent Lumped Element Model of Divided FSIW Resonator along G-G' Plane

Figure 3.14: Equivalent Lumped Element Circuit Models for Figures 3.13a and 3.13b respectively.

With the slot as an inter-resonator coupling structure, the filtering characteristic is then analysed with respect to the slot length P2 and the slot width P1 to identify the effect of these on the resonant frequency, the amount of coupling, and type of coupling, between the resonators represented by a coupling coefficient, k.

The 3D electromagnetic behaviour is analysed for fixed structure parameters of: $a = 10\,mm$, $s = 1\,mm$, $and\,L1 = a - s = 9\,mm$; $e_r = 3.55$; $h = 0.254\,mm$, where all dimensions correspond to those previously depicted in figure 3.10c. Initially, the effect of a variation in the length of the coupling slot, denoted P2 (see figure 3.13b) on the frequency response of the quarter wavelength FSIW filter is simulated and is presented in figure 3.15. P2 is varied in steps of 1 mm from $P2 = 6\,mm$ to $P2 = 12\,mm$. For this simulation, the width of the slot if fixed to $P1 = 0.2\,mm$.

A number of observations can be made from figure 3.15:

- Firstly, the occurrence of a transmission zero is observed.
- Secondly, the transmission zero is observed to shift to lower frequencies with an increase in the length of the slot, P2.

- Thirdly, a shift in the position of the transmission zero with respect to the passband, from the upper side of the passband to its lower side is noted between the lengths $P2 = 8\,mm$ and $P2 = 9\,mm$ indicating a change in the type of coupling between the resonators at a length between $P2 = 8\,mm$ and $P2 = 9\,mm$.

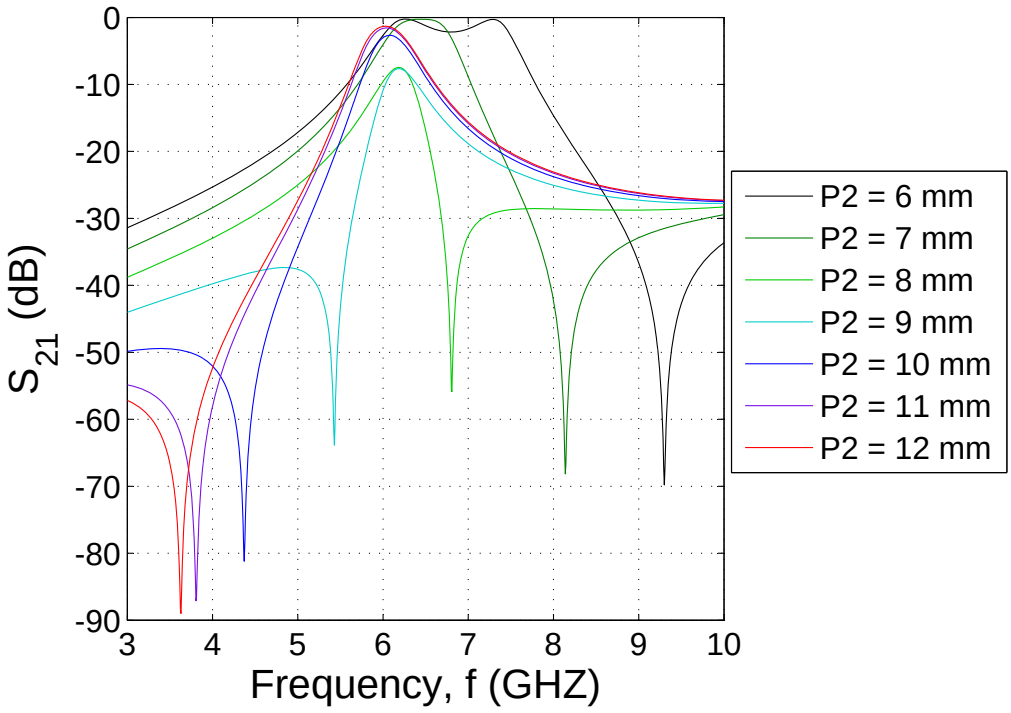


Figure 3.15: Variation of Coupling with P2; $P1 = 0.2\,mm$

The type of coupling that occurs when the transmission zero frequency is above the passband frequency appears to be stronger than the type of coupling for the case where the transmission zero occurs below the passband frequency for equal steps of $P2$.

To investigate the coupling mechanism in more detail, the electromagnetic fields within the filter structure are analysed for two conditions: $P2 = 8\,mm$ and $P2 = 11\,mm$. These values are chosen to produce two types of coupling for situations on either side of $P2 \approx 8.54\,mm$, for a fixed $P1 = 0.2\,mm$.

Condition 1: $P2 = 8\,mm$

Figure 3.16 shows the distribution of the electric and magnetic field lines for the two split-mode resonant frequencies. Looking at electric and magnetic field lines for mode 1, it can be seen that the field pattern is such that a magnetic wall can be inserted in the symmetry plane between the two sides of the filter divided by the slot. The opposite is seen for mode 2, where an electric wall replaces the magnetic wall.

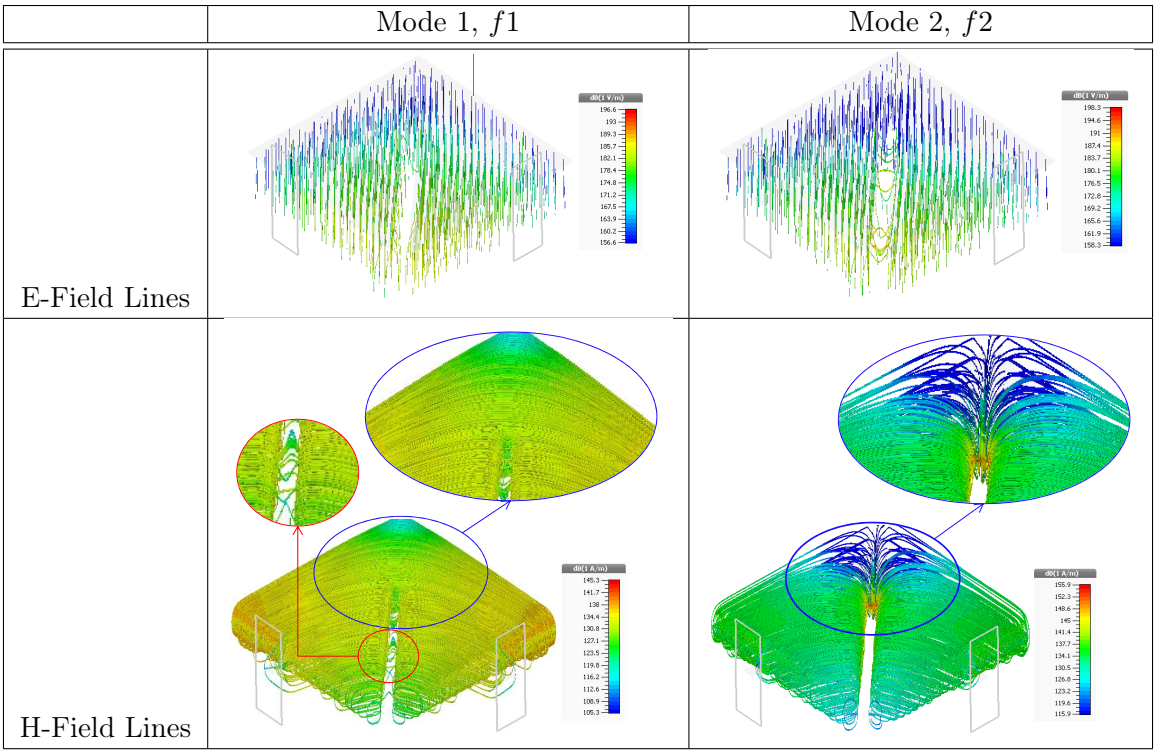


Figure 3.16: Condition 1: $P2 = 8\,mm$; $P1 = 0.2\,mm$

If the split mode frequencies are defined as f_m and f_e respectively, where the subscripts m and e denote the cases where a magnetic wall and electric wall are inserted respectively, the coupling coefficient, k_{c1}, for $P2 \lesssim 8.54\,mm$ can now be written as:

$$k_{c1} = \frac{f_e^2 - f_m^2}{f_e^2 + f_m^2} \tag{3.12}$$

where the subscript $c1$ represents condition 1.

Condition 2: $P2 = 11\,mm$

For the second condition, for the value of $P2 \gtrsim 8.54\,mm$, the electric and magnetic field lines for mode 1 and mode 2 are shown in figure 3.17.

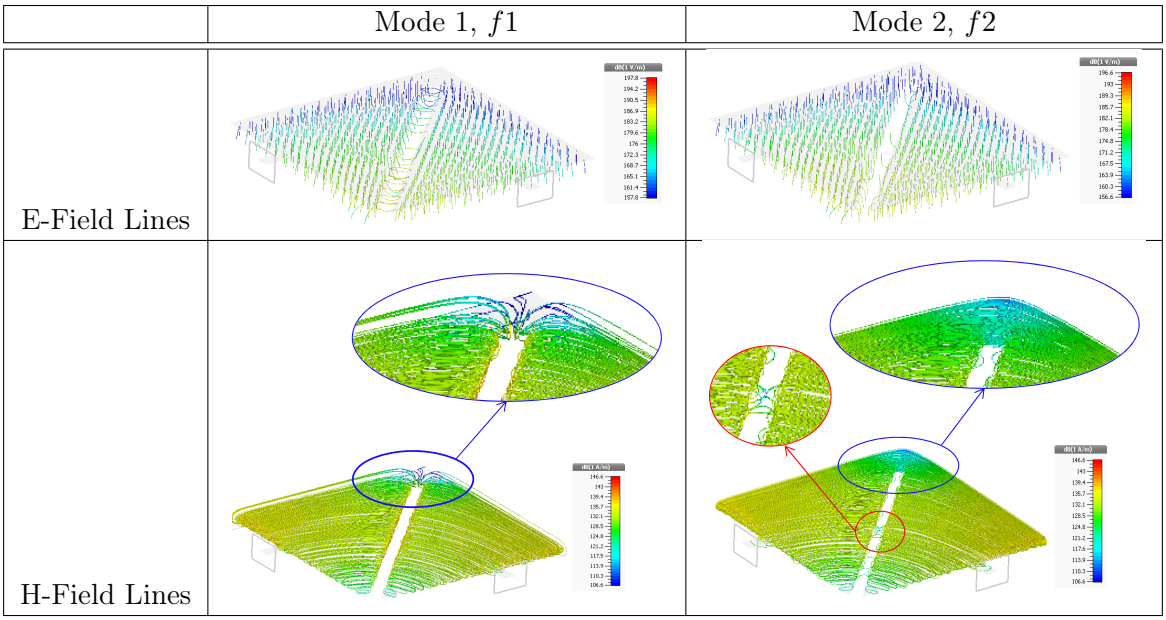


Figure 3.17: Condition 2: $P2 = 11\,mm$; $P1 = 0.2\,mm$

An electric wall is inserted at the diagonal symmetry plane along the diagonal slot for the first mode and a magnetic wall replaces this for the second mode. The coupling coefficient in this instance, k_{c2}, for $P2 \gtrsim 8.54\,mm$ is negative i.e

$$k_{c2} = -\left(\frac{f_e^2 - f_m^2}{f_e^2 + f_m^2}\right) \tag{3.13}$$

The subscript $c2$ represents condition 2.

The formulas for computing the coupling coefficient 3.12 and 3.13, only differ in sign to show a change in the type of coupling in the structure. A general definition for the coupling coefficient can then be written as

$$k = \frac{f_e^2 - f_m^2}{f_e^2 + f_m^2} \tag{3.14}$$

This is plotted, for $P2 = 6\,mm$ to $P2 = 12\,mm$ in figure 3.18. The clear change in the type of coupling can be observed at an approximate slot length of $P2 \approx 8.54\,mm$. For synchronously tuned coupled-resonator filters, when the coupling coefficient defined by formula 3.14 is a positive value, then the dominant type of coupling is magnetic coupling and when it has a negative sign, then the dominant type coupling is electric coupling.

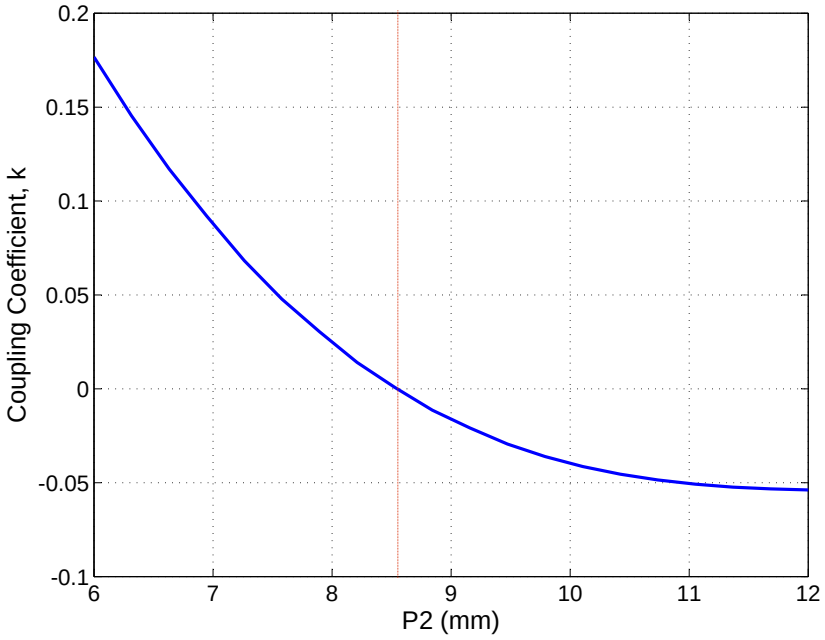


Figure 3.18: Coupling Coefficient,k, vs slot length, $P2$; $P1 = 0.2\,mm$

From figures 3.16 nd 3.17, it can also be seen that both magnetic and electric coupling are present for either condition., so that the inter-resonator coupling can now be referred to as mixed coupling.

For both of the two conditions above, the current flow on the middle slotted plate is such that the magnetic field lines form loops that go through the slot. As can be seen, for both even and odd modes in either case, magnetic coupling does not occur directly across the slots. However, it can also be noted that there are some magnetic field lines visible in the areas marked with the red circles for mode 1 in the first condition and mode 2 for the second condition. These field lines are attributed to a magnetic coupling between the source and the load ports.

In the next subsection, a lumped element circuit is proposed to model the effects that have been observed in this subsection.

3.6 Proposed Cross-Slot Coupled FSIW Resonator Filter

The single-slot coupled FSIW resonator allows the designer to set the coupling coefficient using the slot length, and the resonant frequency using the waveguide dimensions. However, it is often useful to have the ability to set the resonant frequency by another means as well. This section proposes a new topology that introduces a crossed-slot coupling structure shown in figure 3.19 with the aim of achieving this.

It is shown that the proposed cross-slot acts as an additional tuning element during the design process by either varying its position relative to the open end of the main diagonal slot, or its length, or width. It is also shown that the cross-slot becomes highly important as an alternative tuning

element for the center frequency of two filters used in the construction of a diplexer. The topology of this filter is shown in figure 3.19.

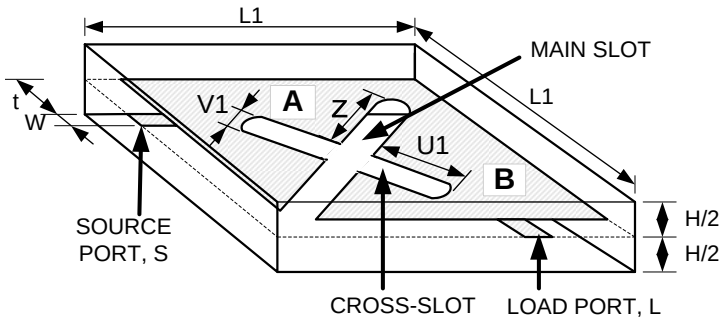
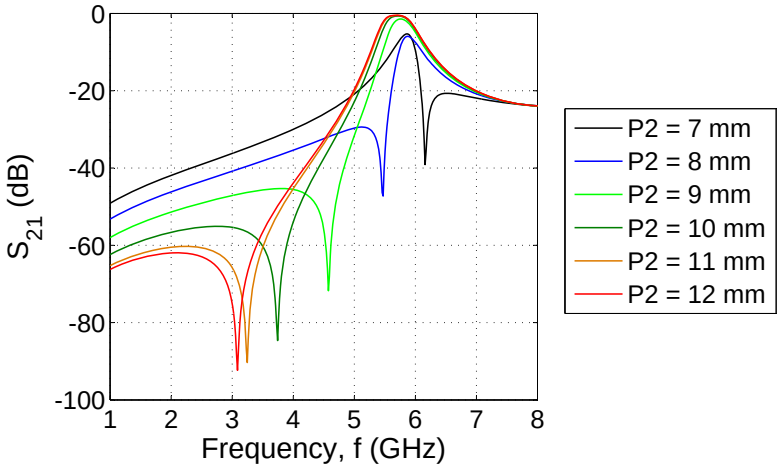


Figure 3.19: Topology of slot-coupled second order folded waveguide filter.

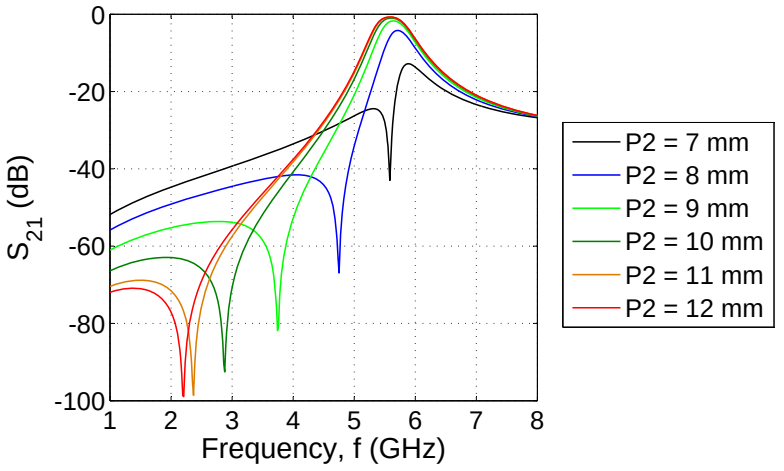
The cross-slot lengths on either side of the diagonal slot are equal so that the structure is symmetrical about the diagonal axis along the center of the diagonal slot.

The cross-slot introduces additional capacitance in the two resonators separated by the main diagonal slot and this shifts the resonant frequencies of individual resonators. The position of the slot has an effect on the type of coupling and value of the coupling coefficient achievable by the filter. Figure 3.20 shows how the insertion loss varies against the full length of the main slot, $P2$, for three positions of the cross-slot, z (see figure 3.19): $z = 3\,mm$, $z = 5\,mm$ and $z = 7\,mm$. $P2$ is varied in the range $7\,mm \leq P2 \leq 12\,mm$ in steps of $1\,mm$. When $z = 3\,mm$, lower values of $P2$ can still realise magnetic coupling that is dominant over electric coupling in the filter. Figure 3.20 also shows that, depending on the position of the cross-slot, the position of the transmission zero below the filter passband can be shifted to lower frequencies than previously achievable by the topology without the cross-slot (see figure 3.15).

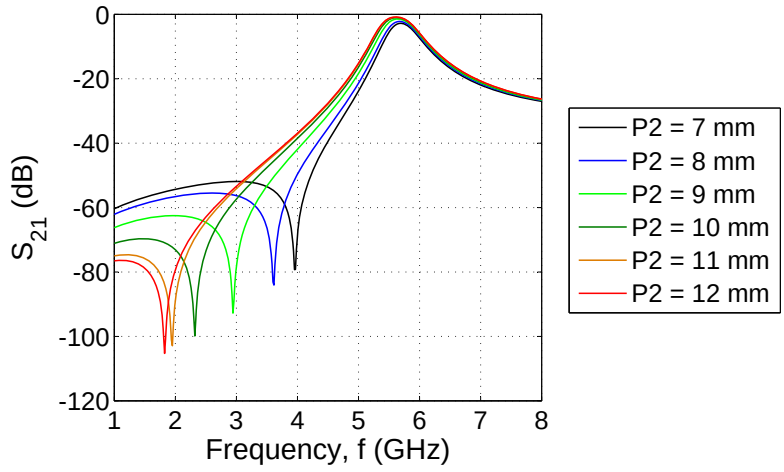
The change in coupling coefficient against $P2$ when the cross-slot is located at $z = 3\,mm$, $z = 5\,mm$ and $z = 7\,mm$ is shown in figure 3.21. A change in the sign of the total coupling can be seen in the case where $z = 3\,mm$, when $P2 \approx 7.7\,mm$. The coupling for the other two cases is seen to be dominantly electric throughout the tuning range of $P2 = 7\,mm$ to $P2 = 12\,mm$.



(a) $z = 3\,mm$

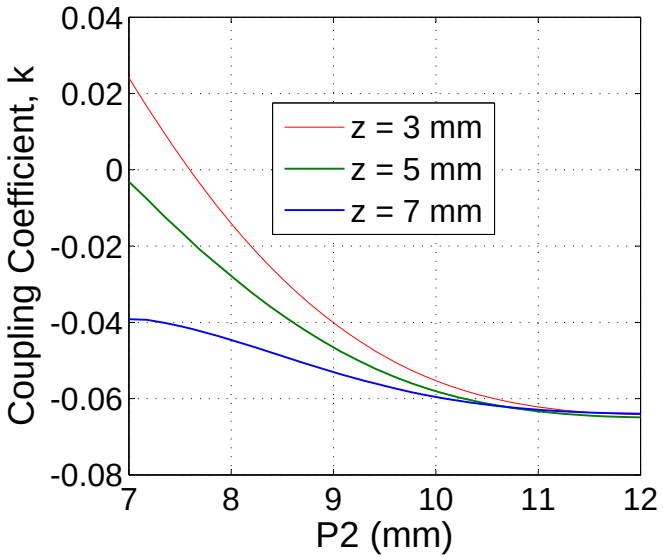


(b) $z = 5\,mm$



(c) $z = 7\,mm$

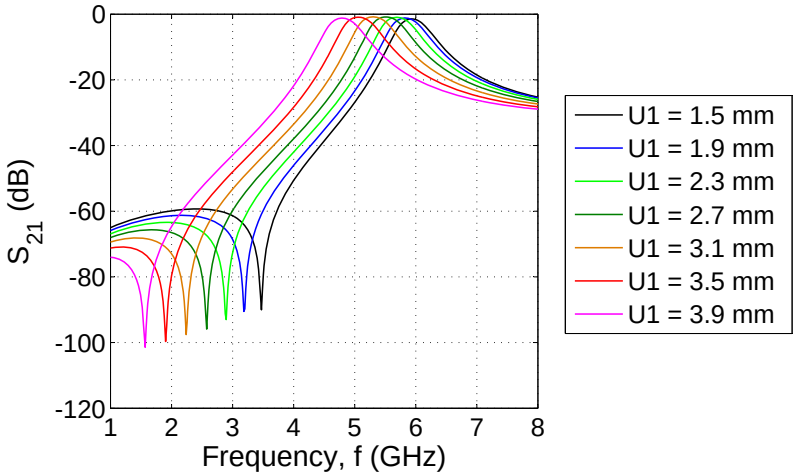
Figure 3.20: Insertion Loss for varying slot length: $P2 = 7\,mm$ to $P2 = 12\,mm$ in steps of $1\,mm$ when the position of the cross-slot is fixed at (a) $z = 3\,mm$, (b) $z = 5\,mm$ and (c) $z = 7\,mm$; $U1 = 2.5\,mm$; $V1 = 0.1\,mm$.



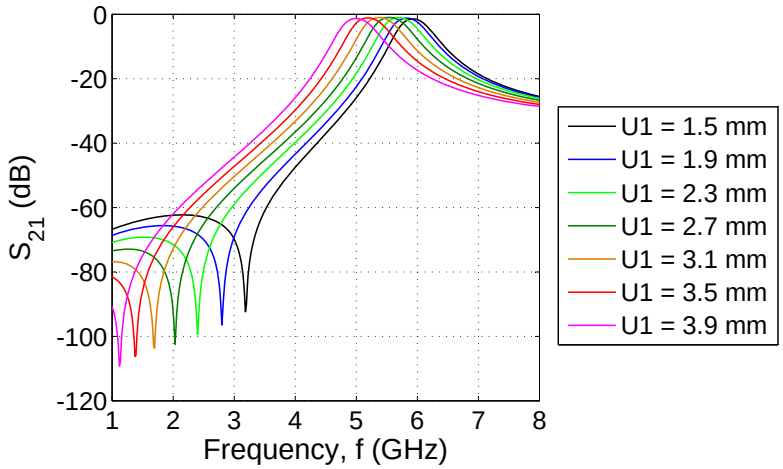
(a) Coupling coefficient, k

Figure 3.21: Coupling coefficient, k

Another advantage of the topology is that changes in the length of the main slot (see figure 3.20a) results in smaller changes in the frequency at which transmission zeros occur so that sensitivity is reduced. The filter also realizes an asymmetric response which is an advantage when designing diplexers in which the two filter bands are close together. For diplexers, rejection requirements are usually less severe on the outer sides of the filter bands, so that by using filters with asymmetric characteristics, the insertion losses, the overall mass, volume and complexity are minimised [27]. If the first transmission zero of the first filter can be positioned at the center frequency of the second filter or as close as possible so that the roll-off gives a high selectivity and vice versa, then a desirable isolation between the two channels can be achieved.



(a) $z = 5\,mm$



(b) $z = 7\,mm$

Figure 3.22: Insertion Loss for varying cross-slot length: $U1 = 1.5\,mm$ to $U1 = 3.9\,mm$ in steps of $0.4\,mm$ when the position of the cross-slot is fixed at (a) $z = 5\,mm$ and (b) $z = 7\,mm$; $P2 = 11\,mm$; $V1 = 0.11\,mm$.

3.7 Coupling Equivalent Circuit Model

A lumped element circuit model is proposed as an equivalent circuit model to model all the effects observed in sections 3.5 and 3.6 near resonance. The same model is used for both the single-slot coupled filter and the cross-slot coupled filter. This is shown in figure 3.23. The corresponding coupling diagram is shown in figure 3.24.

The two resonators in the circuit are directly coupled through a mixed series coupling made up of parallel J-inverters, one with a inductive elements ($J = 1/\omega L_x$) and the other with capacitive elements ($J = \omega Cx$) to model magnetic and electric coupling respectively. In the proposed circuit

model, the J-inverter formed from inductive elements is modelled with a negative sign inductive series element and a positive sign shunt inductive element on either side of the series inductor to realise the negative coupling characteristic. The proposed circuit model also includes a series inductive coupling between the source and the load. This coupling is in parallel with the direct coupling elements.

The transmission zero in the filter occurs as a result of phase cancellation in all three series-coupling elements: the direct inductive path, the direct capacitive path and the inductive source-load component. It is well known that the phase of a signal through a series inductive element tends towards -90^0 and that through a series capacitive tends to $+90^0$. It can therefore be deduced that for a filter with a transmission zero realised through the mixed coupling mechanism in figure 3.23, a passband occurring below the transmission zero frequency indicates that the filter is predominantly magnetically coupled. By the same logic, a filter with a passband frequency higher than the transmission zero resonant frequency can be said to have a capacitive coupling as the dominant inter-resonator coupling.

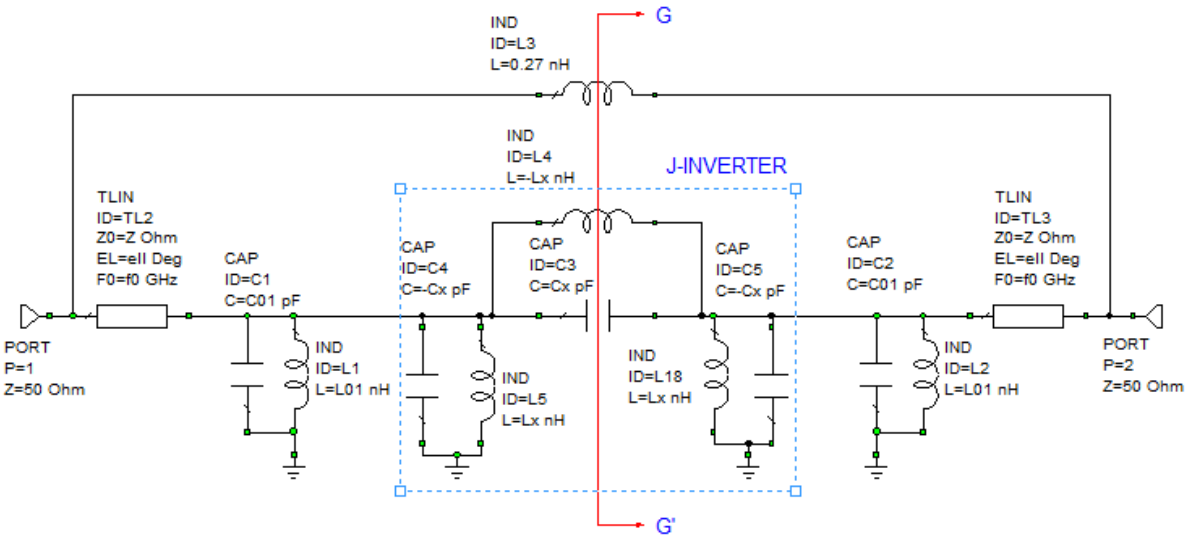


Figure 3.23: Proposed FSIW Equivalent Lumped Circuit Model

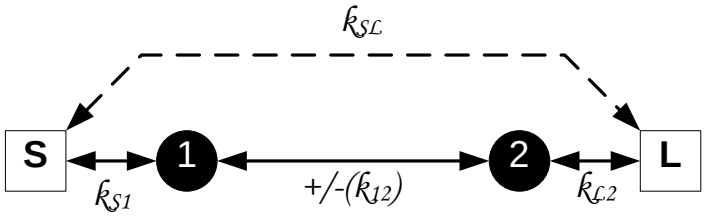


Figure 3.24: Coupling Diagram for Circuit in Figure 3.23

The $n+2$ coupling matrix for the elements of the coupling diagram in figure 3.24 is shown in equation

$$[m] = \begin{bmatrix} 0 & m_{S1} & 0 & m_{SL} \\ m_{1S} & 0 & m_{12} & 0 \\ 0 & m_{21} & 0 & m_{2L} \\ m_{LS} & 0 & m_{L2} & 0 \end{bmatrix} \tag{3.15}$$

where m_{xy} represent the coupling coefficients, k_{xy}, either between two resonators or between a resonator and the source or load, denormalised to the fractional bandwidth (see equation 3.11). The difference between this alternate explanation for the coupling behaviour of the circuits, and that presented in [17] can now be seen by comparing the $n+2$ coupling coupling matrices in equations 3.10 and 3.15.

The input and output coupling elements, $m_{S1} = m_{1S}$ and $m_{L2} = m_{2L}$ respectively, relate to the external quality factor, Q_e, and the fractional bandwidth, FBW, of the filter through the equations [54]

$$Q_{e,\,S1} = \frac{1}{m_{S1}^2 \cdot FBW} \tag{3.16}$$

$$Q_{e,\,L2} = \frac{1}{m_{L2}^2 \cdot FBW} \tag{3.17}$$

For a given desired bandwidth, the input and output coupling can be controlled by varying the external quality factor. In this chapter, the other elements of the coupling matrix will be obtained through optimisation.

To derive the coupling coefficient for the inter-resonator direct coupling in the lumped element equivalent circuit in figure 3.23 two conditions are considered: the first being when an electric wall replaces the symmetry plane G-G' and is used to compute the odd-mode resonant frequency. For the second case, a magnetic wall replaces the symmetry plane G-G' and this is used to compute the even-mode resonant frequency. An electric wall is the equivalent of a short circuit and when this replaces the symmetry plane G-G', either one of the symmetrical synchronously tuned halves can be represented as shown in figure 3.25a. This resultant circuit has a resonant frequency

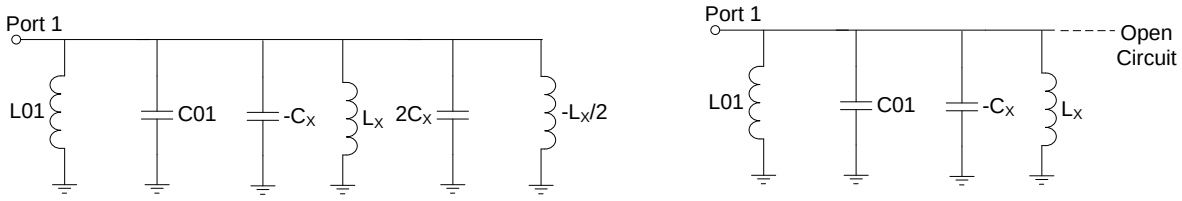
$$f_e = \frac{1}{2\pi\sqrt{(C01 + C_x)\left(\frac{L01 \cdot L_x}{L_x - L01}\right)}} \tag{3.18}$$

where the subscript e denotes the electric wall.

The other values represent the elements in figure 3.23. Simulation values will be specified for every set of results that is to be presented. Equation 3.18 can be re-written as

$$f_e^2 = f_0^2 \cdot \frac{1}{\left(1 + \frac{C_x}{C01}\right)\left(\frac{1}{1-\frac{L01}{L_x}}\right)} \tag{3.19}$$

where $f_0 = {}^1\!/_{2\pi\sqrt{L01 \cdot C01}}$.



(a) Electric Wall Resultant Circuit

(b) Magnetic Wall Resultant Circuit

Figure 3.25: Mixed Coupling Single-Resonant Section Equivalent Circuits when the Symmetry Plane in Figure 3.23 is replaced by (a) an Electric Wall and (b) a Magnetic Wall

When a magnetic wall replaces the symmetry plane G-G' instead, the resultant circuit can be represented as shown in Figure 3.25b and for this case, the circuit has a resonant frequency

$$f_m = \frac{1}{2\pi\sqrt{(C - C_x)\left(\frac{L \cdot L_x}{L + L_x}\right)}} \tag{3.20}$$

where the subscript m denoted the magnetic wall and the other values represent the elements in figure 3.23. Equation 3.20 can the be re-written as

$$f_{m^2} = f_0^2 \cdot \frac{1}{\left(1 - \frac{C_x}{C}\right)\left(\frac{1}{\frac{L}{L_x}+1}\right)} \tag{3.21}$$

If the ratios $\frac{C_x}{C}$ and $\frac{-L}{L_x}$ are now defined by electric and magnetic coupling coefficients namely $k_{El} = \frac{C_x}{C}$ and $k_{Mg} = \frac{-L}{L_x}$ respectively, then equations 3.19 and 3.21 can now be re-written as

$$f_e^2 = f_0^2 \cdot \frac{1 + k_{Mg}}{1 + k_{El}} \tag{3.22}$$

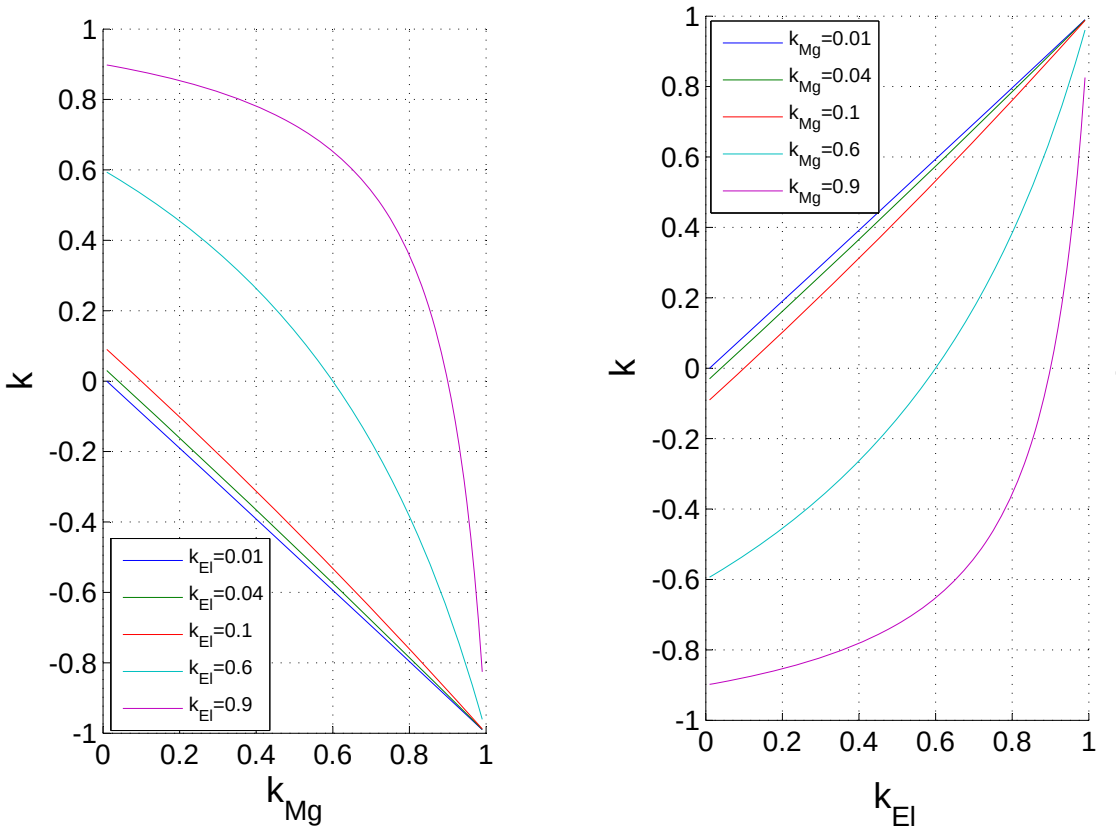
and

$$f_e^2 = f_0^2 \cdot \frac{1 - k_{Mg}}{1 - k_{k_{El}}} \tag{3.23}$$

respectively. The mixed coupling coefficient due to the direct inter-resonator coupling can now be defined as

$$k = \frac{f_m^2 - f_e^2}{f_m^2 + f_e^2} = \frac{k_{El} - k_{Mg}}{1 - k_{El}k_{Mg}} \tag{3.24}$$

Equation 3.24 is now plotted in figure 3.26 to confirm the viability of the lumped element equivalent circuit as a valid circuit representation for a single-slot coupled quarter wavelength FSIW filter. Figure 3.26a is a plot of the mixed coupling coefficient, k, versus the magnetic coupling coefficient, k_{Mg}, for different values of electric coupling coefficient, $k_{El} = 0.01, 0.04, 0.1, 0.6, 0.9$. Figure 3.26b on the other hand, is a plot of the mixed coupling coefficient, k, versus the electric coupling coefficient, k_{El}, for different values of magnetic coupling coefficient, $k_{Mg} = 0.01, 0.04, 0.1, 0.6, 0.9$. From equation 3.24, it can be seen that when k_{El} is constant, an increase in k_{Mg} results in an increase in the mixed coupling coefficient, k, for $k_{Mg} > k_{El}$. For a constant k_{Mg}, the mixed coupling coefficient increases with and increase in k_{El} for $k_{El} > k_{Mg}$. The sign difference only indicates a change in the type of dominant coupling.



(a) k Versus k_{Mg} for $k_{El} = 0.01, 0.04, 0.1, 0.6, 0.9$ (b) k Versus k_{El} for $k_{Mg} = 0.01, 0.04, 0.1, 0.6, 0.9$

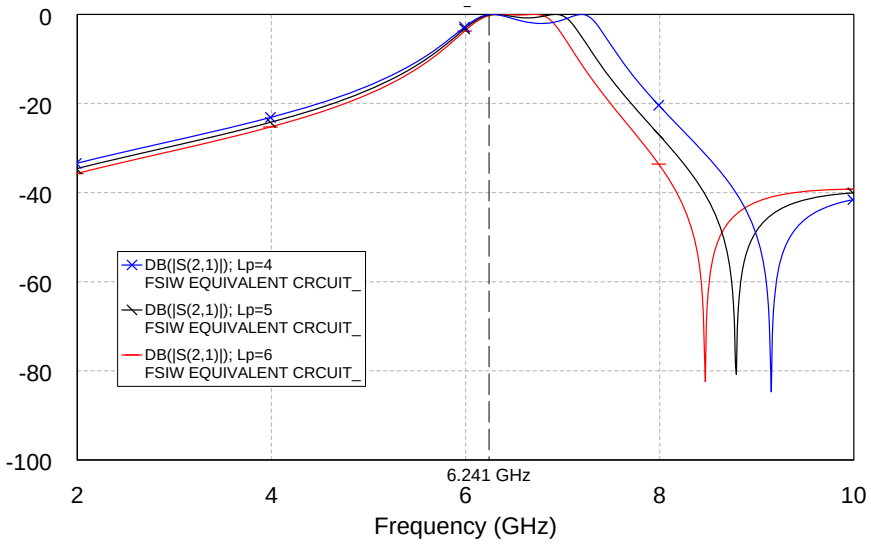
Figure 3.26: Coupling coefficient, k, calculated from Equivalent Circuit Model in figure 3.23

It has also been seen in figure 3.15, that for both the case where electric coupling is dominant and that which magnetic coupling is dominant, a change in coupling only shifts one of the two split-mode resonant frequencies while the other is hardly shifted. In the case where magnetic

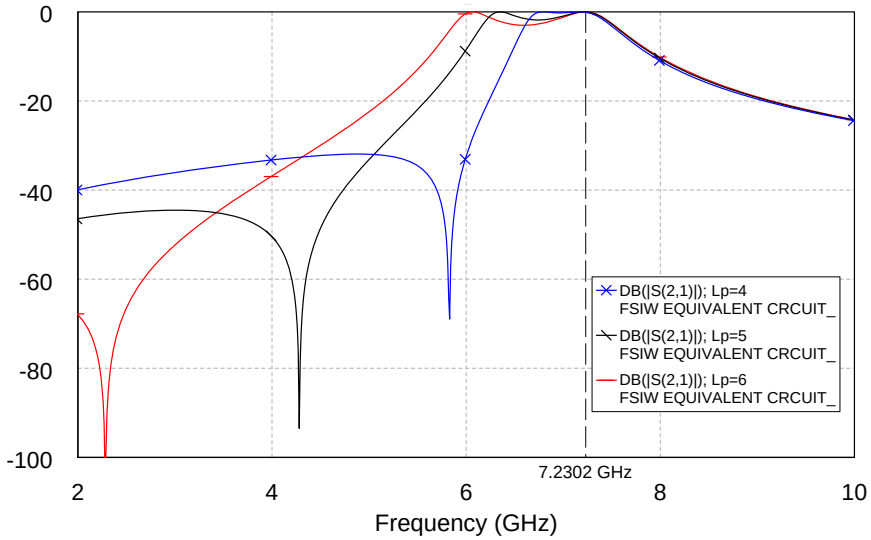
coupling dominates, the odd-mode frequency shifts while the even-mode frequency almost remains constant, where as when the electric coupling is dominant, the even-mode frequency shifts while the odd-mode frequency remains nearly constant. The circuit model must therefore also emulate this characteristic. This is achieved by only varying the source-load coupling element, L_p, in figure 3.23 for either the dominant electric coupling case or the magnetic coupling case. The effect of this is plotted in figure 3.27 for $L_p = 4\,nH$, $5\,nH\,and\,6\,nH$. The following element values in table 3.1 were chosen for an uncoupled resonant frequency of 5.99 GHz.

	L_x (nH)	C_x (pF)
Dominant Magnetic Coupling	4	0.208
Dominant Electric Coupling	0.33	0.259

Table 3.1: Element Values for Plots in figure 3.27



(a) $Lp = 4, 5, 6$; $Lx = 4$; $Cx = 0.208$; *Single resonator resonant frequency*, $f_r = 5.99\,GHz$; All Inductances in nH and all Capacitances in pF



(b) $Lp = 4, 5, 6$; $Lx = 0.33$; $Cx = 0.259$; *Single resonator resonant frequency*, $f_r = 5.99\,GHz$; All Inductances in nH and all Capacitances in pF

Figure 3.27: Insertion Loss Of Circuit in Figure 3.23 for (a) Dominant Magnetic Coupling and (b) Dominant Electric Coupling

Figure 3.28 shows a wideband phase response of S_{21} for two conditions: dominant capacitive coupling and dominant electric coupling. A step in phase is noted at the positions of the transmission zeros. For two filters with a centre frequency of approximately at 5.6 GHz designed to have electric (capacitive) and magnetic (inductive) dominant coupling, the change in phase about the transmission zero frequencies relative to the centre frequency confirms that when the passband occurs below the transmission null resonant frequency, the inter-resonator coupling is predominantly

magnetic. Capacitive coupling dominance is then evident when the passband occurs at a frequency higher than that where the transmission zero occurs.

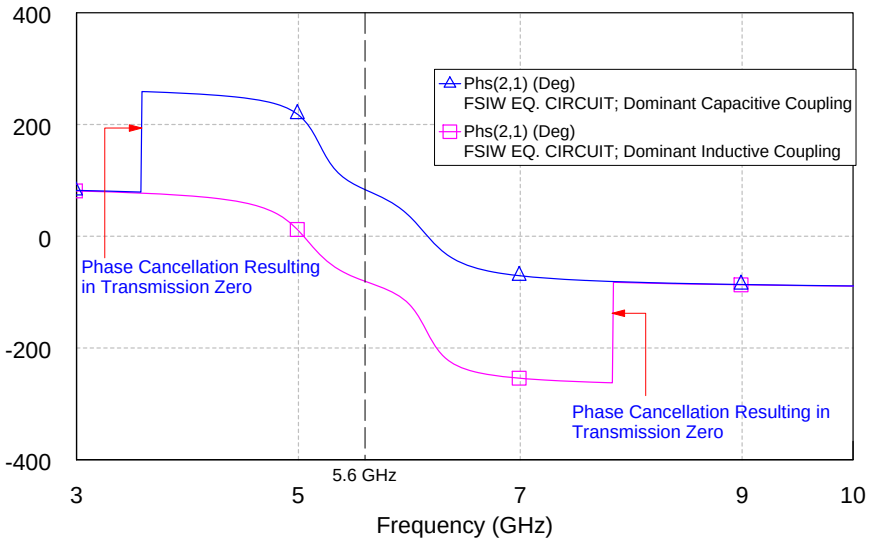


Figure 3.28: Phase of $S_{21}$for the Circuit in Figure 3.23 when Capacitive Coupling is Dominant with $Lp = 4$ and when Inductive Coupling is Dominant with $Lp = 4$; All inductance in nH.

Until now, the analysis has focused on effects resulting for a variation in the slot length, $P2$. A change in the slot width, $P1$, has a more straight forward effect of either increasing or decreasing the capacitive coupling element in the mixed direct inter-resonator coupling. This can be seen in figure 3.29 in which the insertion loss for different slot width, $P1$, are plotted for a fixed slot length of $P2 = 11\,mm$.

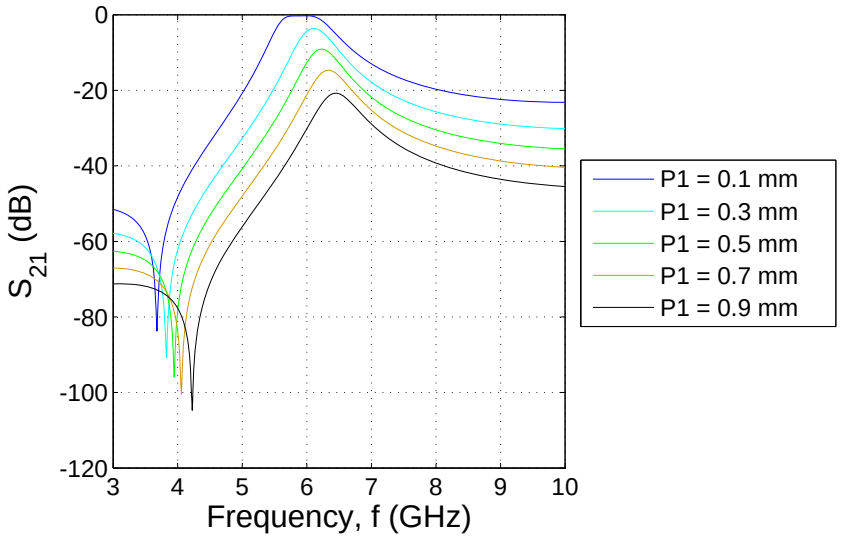


Figure 3.29: Variation of Coupling with P1; P2 = 11 mm

The smaller the width, the more the capacitance and consecutively, the more the inter-resonator coupling.

3.8 2nd Order C-Band SIW Diplexer

Microwave diplexers typically comprise of two bandpass filters with two input ports and a common output port realized through a three-port junction architecture as shown in figure 3.30. This topology allows two different devices to share a common communications channel, thereby creating flexibility for the flow of communication traffic in an environment shared by different users. Most common use is in transceivers behind wideband and multifrequency antennas where they are employed to separate transmit and receive frequency bands so that a common antenna is shared for both receive and transmit signals.

Different guided wave and planar transmission line structures have been used to implement microwave diplexers in the past, the choice of media always reliant on the specifications set by the end user.

Diplexers became widely explored in the early 1960s by Matthaei [69, 68] and Wenzel [84]. The focus of the studies were microstrip diplexers that used bandpass or bandstop configurations and waveguide diplexers. Waveguides found wider use in the late 1960s due to their very low insertion loss and high isolation in comparison to microstrip structures. Waveguides, however, have the disadvantage of requiring rather complex manufacturing processes and the overall attainable size for a given set of specifications may not be desirable. For this reason, substrate integrated waveguide diplexers become an attractive option because they merge the advantages of the two transmission media on a single platform resulting in miniaturised structures with reasonable manufacturing costs.

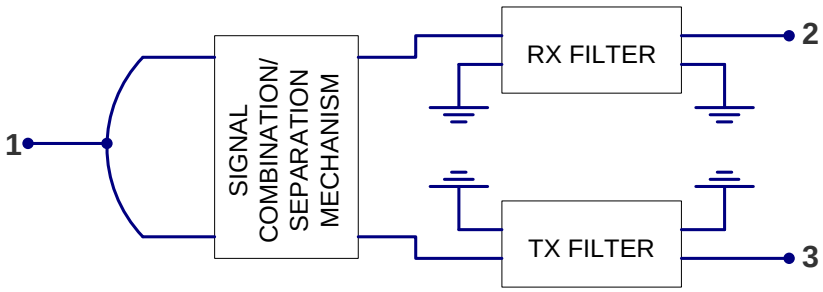


Figure 3.30: General Architecture of a Diplexer

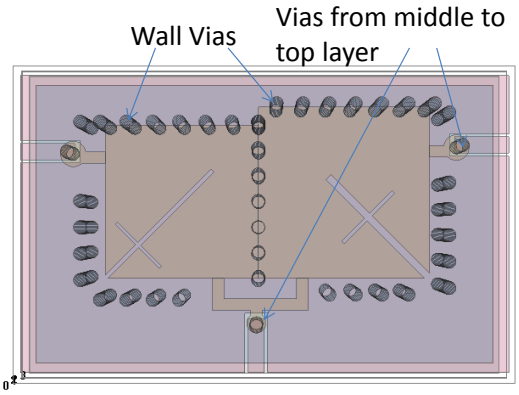
Effective design of diplexers involves the use of special procedures to ensure that the interconnection of the two filters operating at separate desired frequency bands does not result in undesirable interaction effects. At the frequency of operation of the first filter, the input impedance looking into input port of the second filter should be very high in comparison to the input impedance looking into the input port of the first filter so that the signal passes through the first filter. It is desirable to obtain a good match in this path, as well as a good isolation between the two paths. At its operating frequency, the signal passing through the first filter has a very low insertion loss and very high attenuation at the frequency of operation of the second filter. The same applies at the frequency of operation of the second filter where this filter should register very low signal insertion loss and the signal should be considerably attenuated at the frequency of operation of the first filter.

When diplexer band frequencies are too close to each other, the combination of the two signals can become very difficult due to interference. At near resonant frequencies where the magnetic energy is nearly equal to the electric energy, the input impedance looking into a resonant circuit is proportional to the power lost in the transmission circuit and the angular frequency and inversely proportional to the square of the magnitude of the current flowing through the circuit. The wider the difference in the angular frequency between the two diplexer bands, the larger the difference in the input impedances looking into the two filters so that the interference between the two bands is minimal and the isolation obtained is acceptable.

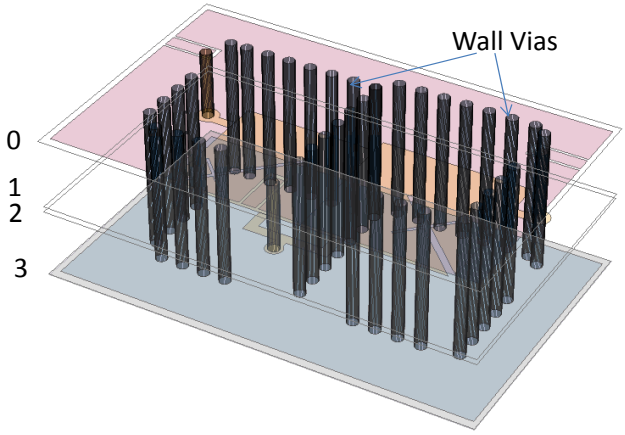
In section 3.6, it was established that the asymmetric property of the filtered response of a cross-slot coupled FSIW filter makes it a suitable candidate for diplexing functions. By properly positioning the transmission zero of the first filter within the range of frequencies of the passband for the second filter or closely placed to those, the insertion loss of the second filter about its center frequency is reduced. Two of those cross-slot coupled FSIW filters are now used in a multilayered structure to achieve an SIW diplexer with transmission bands centered about 4.12 GHz and 4.57 GHz. The fabrication of the diplexer is done using two multilayered technologies: PCB using Rogers 4003c as the core layers and Rogers 3001 bonding ply as the adhesive layer, and LCP (Liquid Crystalline Polymer) as an alternative fabrication technology to see if it is viable for overall substrate thicknesses of over 0.5 mm. The following sections discuss the design process, the fabrication processes and the challenges encountered during both processes.

3.9 Diplexer design and Analysis

One of the main design parameters in diplexer design is to achieve a good isolation between the signals from the two filters. A good design also embodies simplicity as one of the key characteristics so that fabrication becomes easier. The proposed diplexer topology uses two filters of the structure shown in figure 3.19 and the common port is realised through a simple T-junction as shown in figure 3.31 and 3.32. A stripline to co-planar line transition is implemented through a via connection to a different substrate layer for the PCB diplexer (see figure 3.31), where as a same layer stripline to microstrip transition is used for the LCP fabrication (see figure 3.32). The choice of transition is dependent on the capabilities of the fabrication technology, ease of manufacture and reduction of manufacturing costs. The transition must also be able to achieve desirable input coupling properties and have a good match between the joint sections.



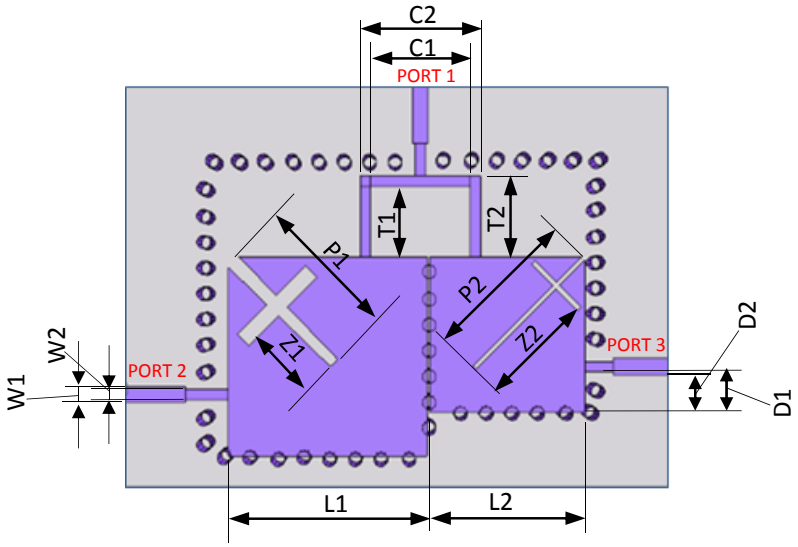
(a) Top View showing Via walls



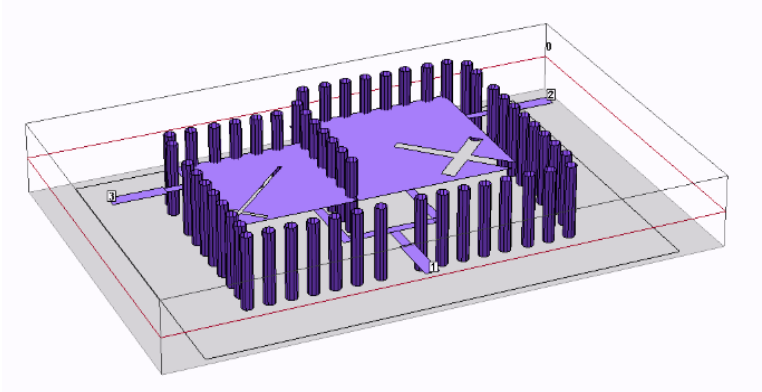
(b) Perspective view

Figure 3.31: Proposed PCB Diplexer Structure with Stripline to Co-Planar Waveguide Transition

The circuit model for the slot-coupled and cross-coupled FSIW filters was presented in figure 3.23. A physical filter can be constructed from the circuit model with coupled resonator being tuned initially using the group delay method with one of the two ports short circuited. For this, the direct source-load coupling is excluded in the circuit since the load no longer exists in the model. The physical constructuon of the filter is then tuned until the group delay response overlaps in a close match with that of the circuit model. Once this is achieved, then by re-introducing the load and hence the source-load coupling, the physical filter can now be tuned by adjusting the lengths and/or widths of the slots to achieved a final response that compares closely with the circuit model results.



(a) Top View with Via Walls



(b) Perspective View

Figure 3.32: Proposed Diplexer Layout in LCP with Stripline to Microstrip Transition

A diplexer circuit model formed out of two cross-slot coupled FSIW filters with center frequencies of 4.12 GHz and 4.57 GHz is shown in figure 3.33 with transmission line sections representing the common port junction. The phase of the common port feed-line can be adjusted to obtain a good correlation between the circuit model and the three dimensional physical filter. A comparison of

the transmission coefficient, reflection coefficient, isolation and phase of the circuit model and the three dimansional structure in figure 3.31 are presented in figure 3.36.

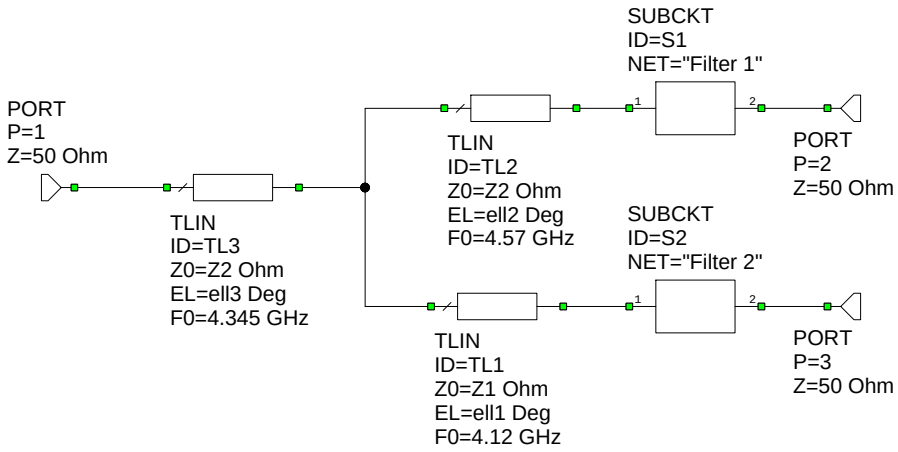


Figure 3.33: Diplexer Circuit Model

A close comparison is noted for all three responses, confirming viability of the circuit model. The dimensions of the simulated three dimensional physical structure are presented in figure 3.34 and related values are tabulated in table 3.2. The 3D structure comprises three copper metal layers clad on two 0.508 mm Rogers 4003c substrate with a 38 µm Rogers 3001 bonding ply in between the two dielectric layers.

Figure 3.35 shows the distribution of metal and dielectric layers for the PCB diplexer. The modelling layers in figure 3.35 are labelled 0 to 3 with layers 0, 1 and 3 containing metal circuitry. Layer 0 hosts the three diplexer ports in the form of co-planar waveguide feed-lines. The transition from these feed-lines to stripline connections on layer 1 is through copper vias connecting layers 0 and 1. Each stripline connection is then connected to the middle plate of the respective FSIW filter through a simple stripline to FSIW filter transition.

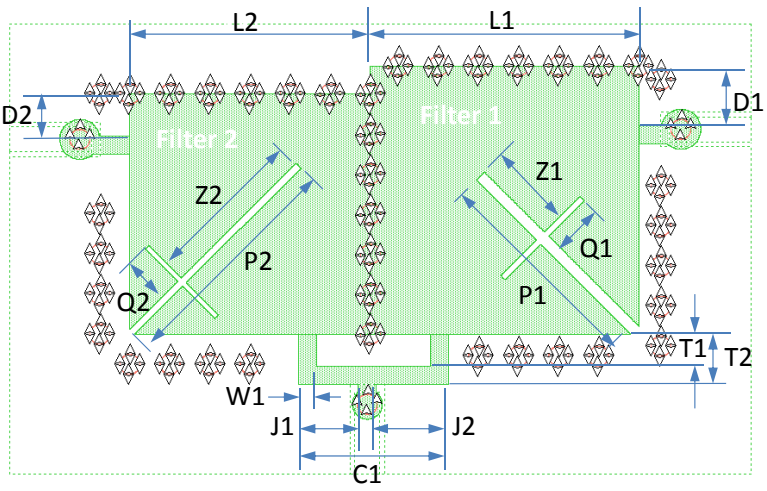
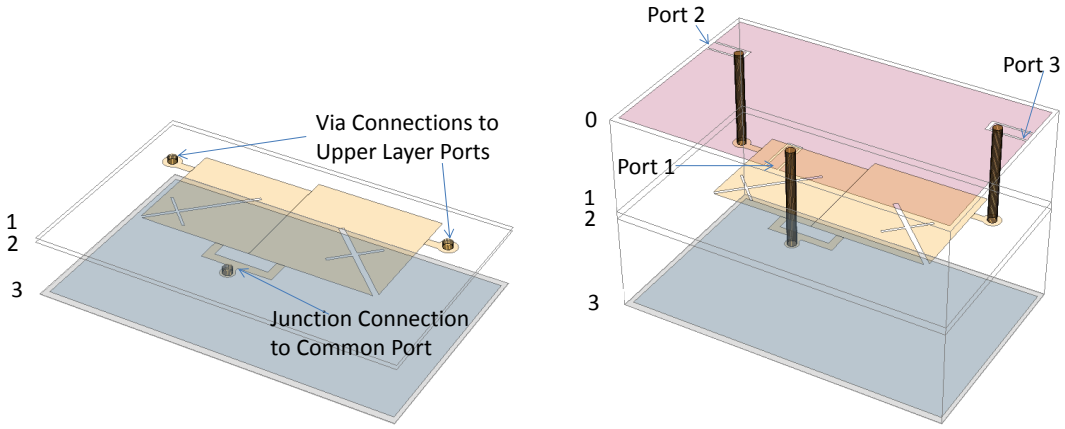


Figure 3.34: Dimensions of PCB 3D Diplexer Model

Parameter	Value (mm)
C1	7.50
D1	2.10
D2	3.00
J1	3.00
J2	3.60
L1	13.4
L2	12.00
P1	10.89
P2	11.74
Q1	2.52
Q2	2.28
T1	1.60
T2	2.50
W1	0.90
Z1	4.24
Z2	8.11

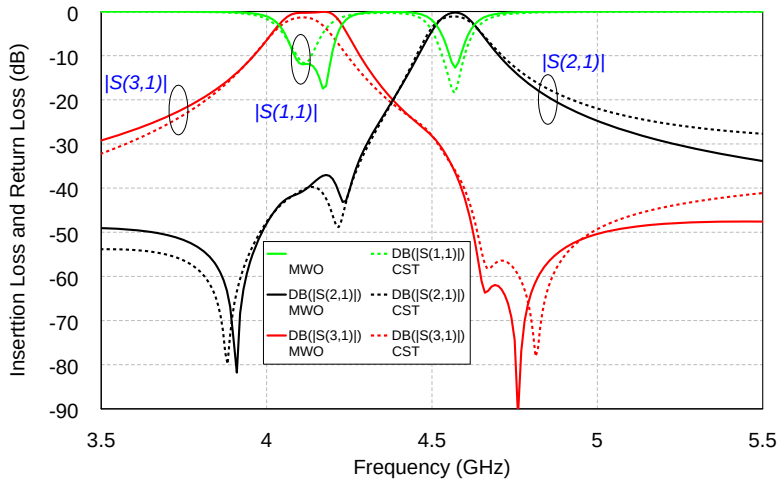
Table 3.2: Table of Values of Diplexer Dimensions

Layer 3 is fully covered with copper cladding that acts as a ground plane for the circuit. The via walls seen in figure 3.31 (b) connect layers 0,1 and 3 so that all three layers contain grounded elements that represent equivalent waveguide walls. All vias are 1 mm in diameter. The equal diameters reduce manufacturing costs by removing the need to change the drilling bits, while the specific size is chosen in accordance with the recommended via diameter to substrate thickness ratio to enable proper plating of the via holes.

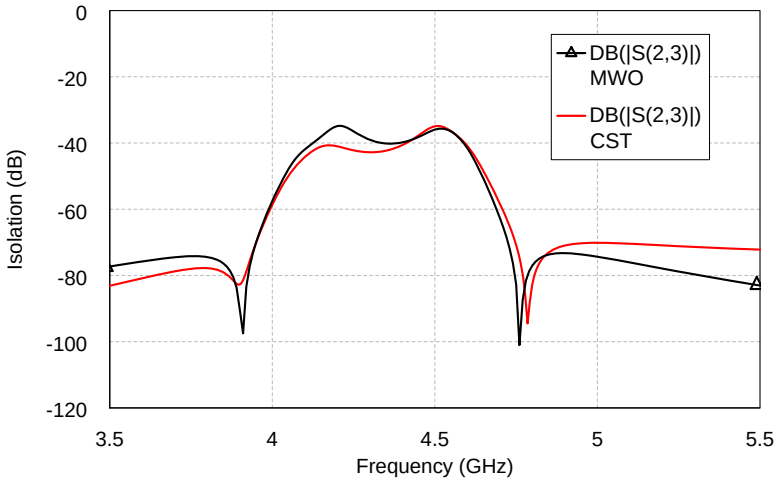


(a) (b)

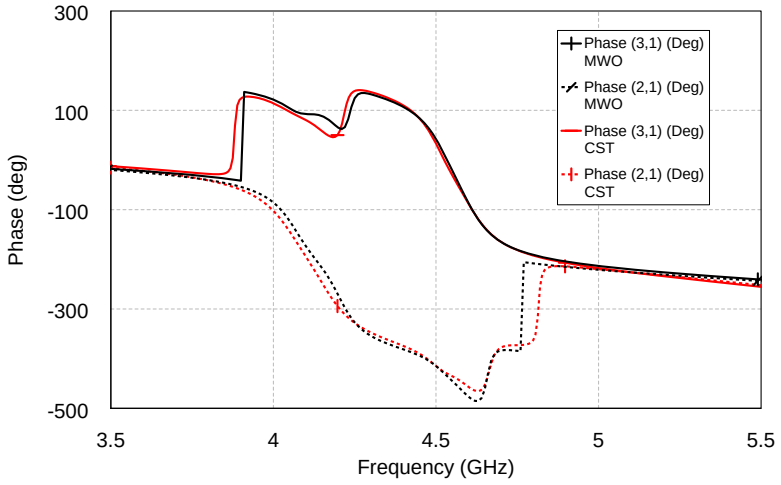
Figure 3.35: 3D Layout of Metal and Substrate Layers of PCB Diplexer



(a) Transmission and Reflection Coefficients in Decibels



(b) Isolation in Decibels



(c) Phase in degrees

Figure 3.36: A comparison of Diplexer Responses from MWO and CST

Fabrication of the diplexer is discussed in the next section for both PCB and LCP fabrication together with the challenges incurred for the respective processes.

3.10 PCB Multilayered Fabrication of SIW Diplexer

The process of fabricating multilayered circuits using PCB substrates has been discussed in chapter 2. This section focuses of the specific observations, challenges and recommendations relevant to the SIW diplexer designed. Manufacture of multilayered circuits involves a combination of different processes all carefully performed to achieve set design tolerances. Most multilayered circuits are miniaturised circuit versions that have very thin transmission lines that require great process accuracy if desired results are to be obtained. Distribution of these lines on any given circuit layer must be so that the small line dimensions are achieved and as many conducting lines can make use of the available footprint whilst leaving allowances for other circuit elements to be placed and enough space for the tools to operate without damage to the circuits. For each process, therefore, there are a set of rules and/or recommendations that are prescribed usually by manufacturers and material suppliers to aid designers in designing well. With regard to the manufacture of the SIW diplexer, some of the challenges encountered can be categorised as follows:

Circuit Complexity Vs. Manufacturer's Capabilities

A designer lays out design concepts based on the functionality that is required subject to a set of provided specifications. Designers always attempt to integrate as many elements of a circuit within a small footprint while achieving the simplest possible form at the same time. However, even a designer's simple version may not be simple enough from a manufacturer's point of view. As mentioned earlier, for any given process, a set of rules and recommendations exist to guide designers with the design process so as to design with manufacturing in mind. These can often be obtained online but it becomes immediately apparent that there are variations in recommendations provided by suppliers, for instance, based on the choice of material to be used as a dielectric. It also becomes evident that manufacturers prefer to work with certain materials based on availability and also ease of fabrication.

Circuit Complexity Vs. Cost Factor

Cost reduction is always one of the factors given the most attention in a design process. Depending on the end use of a manufactured device, whether it is a prototype or a final design for small scale or large scale production, factors that could minimise overall costs are always analysed. From a manufacturer's point of view, total costs comprise direct and indirect labour costs, tooling costs and other specific company fixed costs. Most microwave circuits require very tight dimensional tolerances and multilayered circuits in particular require many changes in machinery for the different stages in

manufacture. If on top of that there should be many different sizes of vias and very many buried vias, then the manufacturing of the circuit becomes taxing to the manufacturer and costly. Consultations with the manufacturers can usually result in recommendable adjustments in the design that make the manufacturing process easier and results in an overall decrease in costs.

Design Requirements Vs. Material Availability

The best choice for a dielectric material for a design may not be the easiest material for a manufacturer to work with. Some materials clog the machinery during drilling and are slippery or too flexible to work with and manufacturers ten to avoid such. Manufacturers usually keep a stock of the materials they prefer to work with and usually recommend to clients the use of these if they can meet their specifications. Otherwise, the client usually has to provide their own material which may be available locally or may need to be imported. Compromises must always be made within the design and manufacturing process.

Manufacturing Steps

The initial 3D FSIW diplexer designed utilises only two copper clad substrate boards. The fabrication instructions presented to the manufacturers were as follows with reference to figure 3.37:

STEP 1: Metal Layer 0 and 1 to be on either side of top 0.508 mm Rogers 4003c substrate board with relevant etching done and vias connecting metallised layers 0 and 1 are to be drilled and plated. Layer 1 will be an internal/buried metal layer and is etched prior to lamination.

STEP 2: Copper cladding (0.017 mm) on top side of substrate board 2 or on layer 2 is to be completely removed leaving copper only on layer 3.

STEP 3: Substrates are stacked together and aligned with 38 um of RO3001 bonding ply in between boards 1 and 2.

STEP 4: The structure is then laminated.

STEP 5: Through vias are drilled and plated and the remaining etching is done.

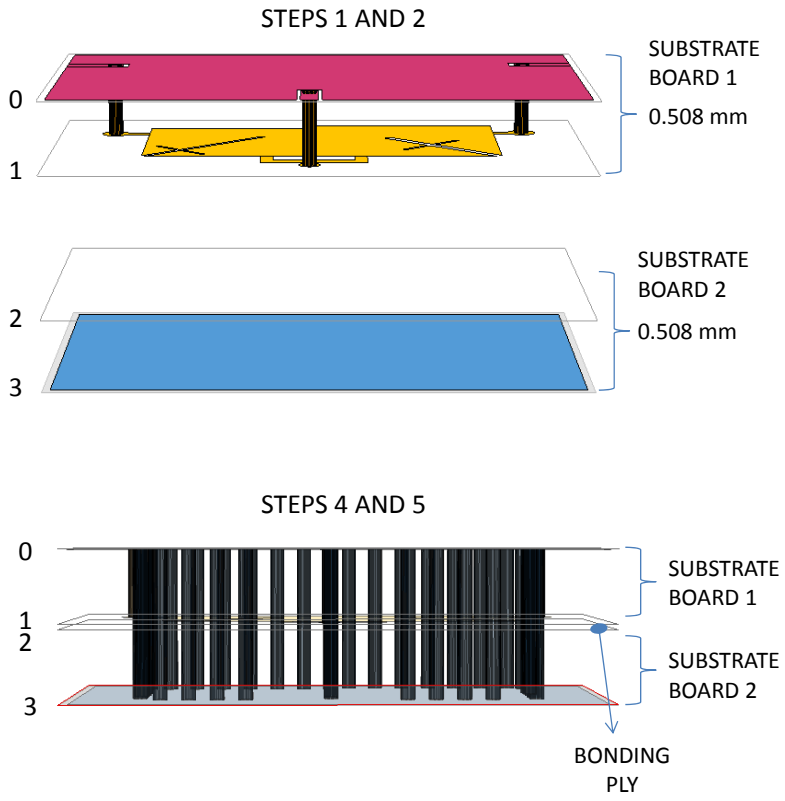
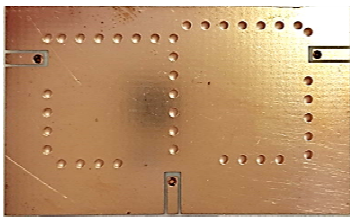
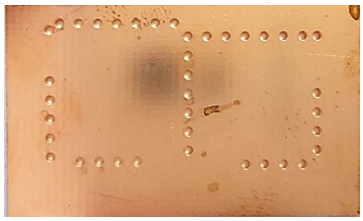


Figure 3.37: Reference figure for Fabrication instructions

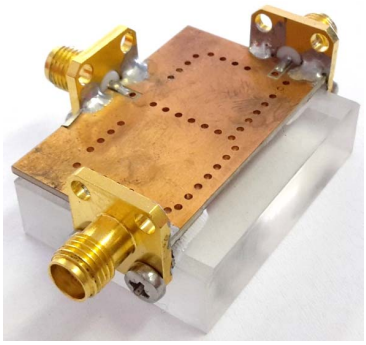
Figure 3.38 shows pictures of one of the fabricated diplexers. The copper plated via holes are all clearly visible and using a multimeter continuity between the top and bottom metal plates was confirmed as well as between the ports and all the grounded plates. The perspective view with SMA connectors attached for measurement purposes is also shown. The measurement results are presented in the next section.



(a) Top View



(b) Bottom View



(c) Perspective view with SMA Connectors

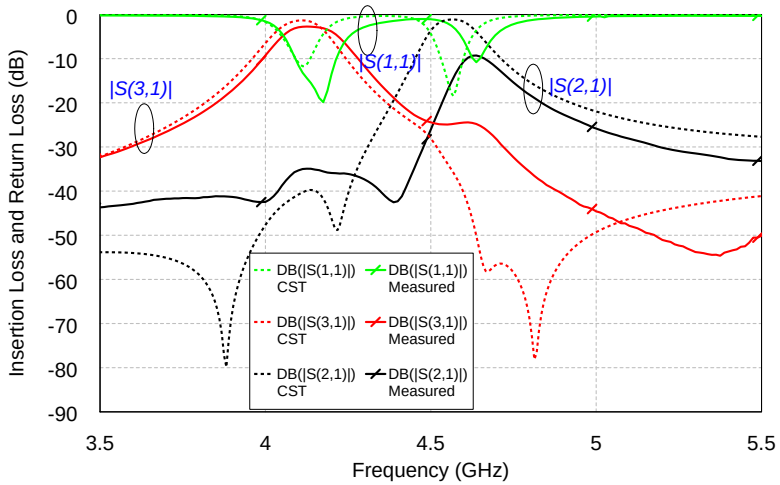
Figure 3.38: Fabricated RO 4003c Diplexer

3.11 Measurements

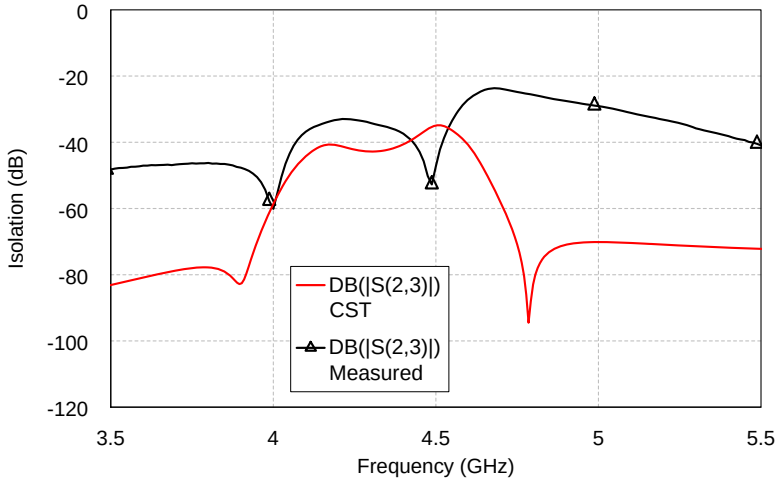
Three square flange SMA connectors with a flat pin were edge connected to the PCB diplexer for measurement purposes (see figure 3.38c). The PCBs are mounted on a thick plastic slab/block so that the SMAs can be stable when connected through 50 ohm cables to the VNA and to avoid breaking off the PCB.

In order to ensure that the outer conductor of the SMA is connected to the ground on both the top and bottom of the PCB, a thin foil of epoxy is used that can be placed between the lower side of the PCB and the plastic slab/block. This epoxy foil is very sensitive to temperature increase and when heat is applied on the open top side, the bottom side also melts electrically connecting the PCB grounds to the SMA ground.

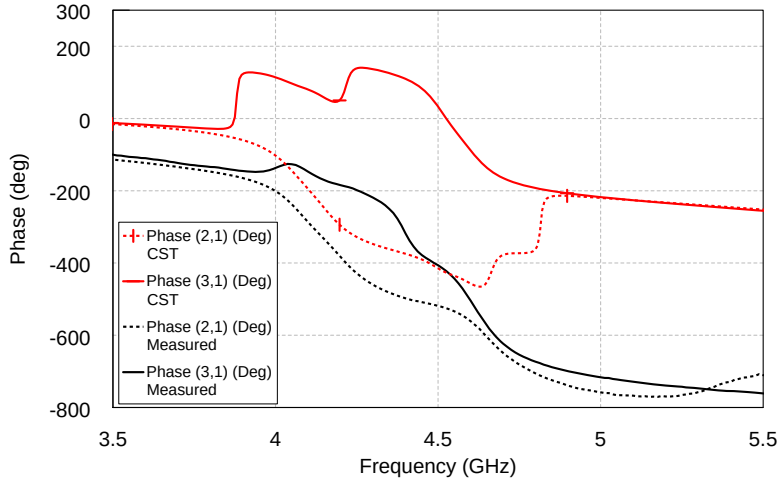
An Agilent HP8510C Vector Network Analyser is used for the measurements with an ability to make broadband measurements in a range of 45 MHz up to 50 GHz in 2.4 mm coaxial cables. The measurement results are compared to the 3D simulated results in figure 3.39. The measured results clearly show the two diplexer passbands. However, these are shifted upwards in frequency and while the lower frequency passband compares more closely within the CST simulated results up to about 4.5 GHz, the upper frequency band registers a rather high insertion loss of approximately 9.3 dB in comparison to about 1.13 dB obtained in the simulated results. Possible reasons for this would be some cracking in the inner circuit layer, specifically on the higher resonant frequency filter.



(a) Insertion Loss and Return Loss



(b) Isolation in Decibels



(c) Phase in Degrees

Figure 3.39: Measurement Results for PCB Diplexer Compared against Simulated Results from CST Microwave Studio

The simulated insertion loss for the lower passband is approximately 1.36 dB whereas the measured one is approximately 2.75 dB. Possible reasons for this would be surface roughness and/or shrinkage of the substrate material after the lamination process. An isolation of >20 dB is obtained over the entire range of operational frequencies of the diplexer. An appreciable change in phase can also be noted. Figure 3.40 shows the broadband measurements of the diplexer's transmission and reflection coefficients. An out-of-band rejection of over 30 dB can be seen between about 5.1 GHz to 8 GHz.

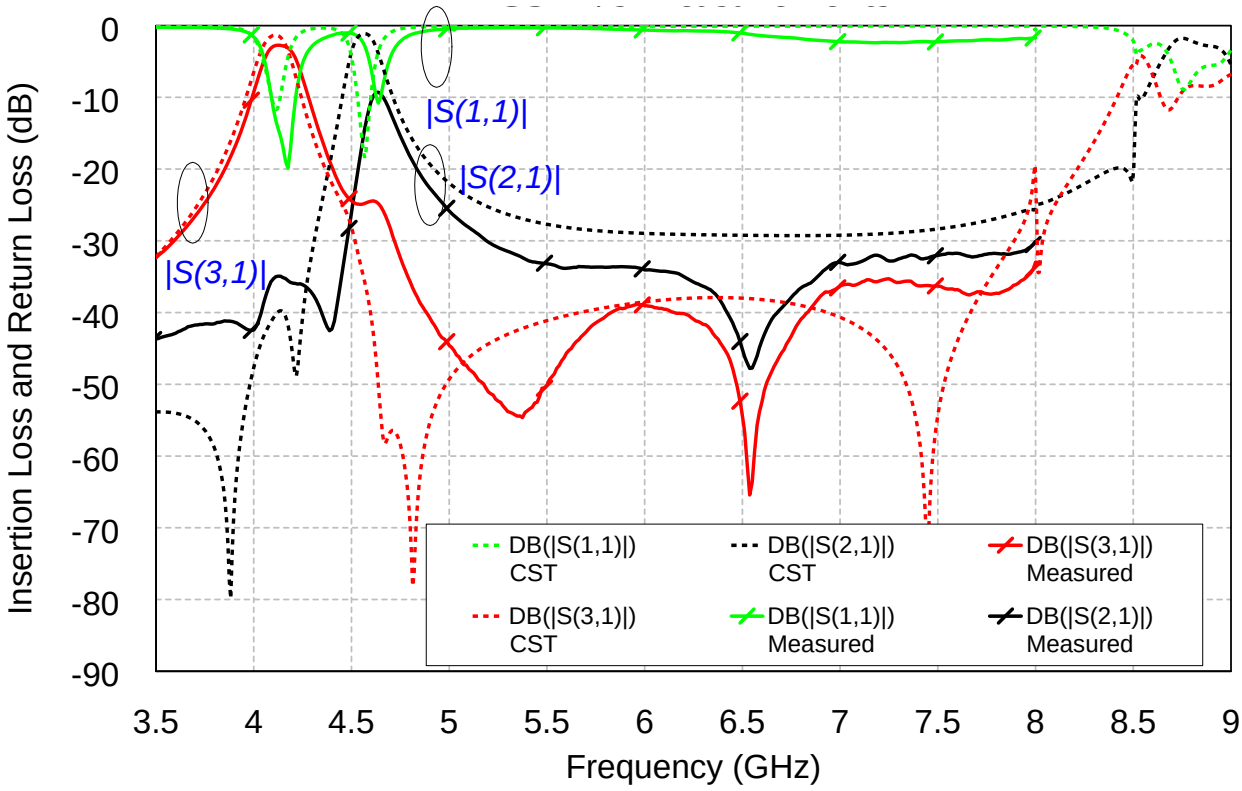


Figure 3.40: Broadband Measurement Results for PCB Diplexer Compared against Simulated Results from CST Microwave Studio

3.12 LCP Multilayered Fabrication of SIW Diplexer

As best known, until now most of the publications of successful LCP multilayered microwave circuits have been of circuits whose overall thicknesses were under 0.5 mm. With this diplexer, thicker circuits are attempted with thicknesses of 1 mm and 0.7 mm.

During the LCP fabrication process, lamination is arguably the most critical stage of fabrication. Lamination follows a specific temperature and pressure profile to achieve a single solid structure from a stack-up of alternating layers of core films and bonding films. Different lamination machines

can be used and the quality of a piece of laminated work can be attributed to the accuracy of the machine in terms of uniformity in the distribution of both temperature and pressure.

The diplexer was fabricated using Rogers Ultralam 3850 core of 100 µm and 50 µm, and the bonding ply used was Rogers Ultralam 3908 of 50 µm thicknesses. The best arrangement of inter-changing cores and bonding plies that was used to realise the 1 mm thick stackup is shown in figure 3.41.

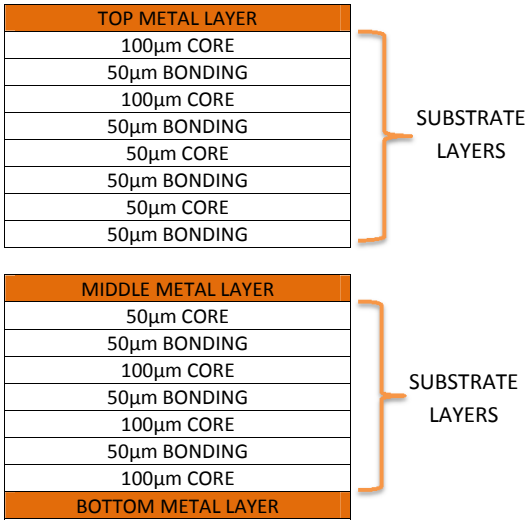


Figure 3.41: LCP Layers Stackup for Diplexer Fabrication

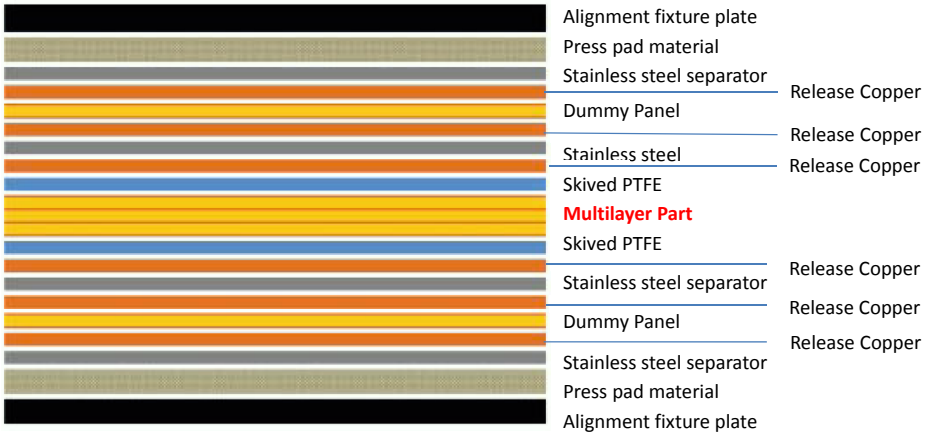
Rogers recommends extra layers of additional materials to be added to the stackup for multilayer bonding as shown in figure 3.42a. Proper lamination is dictated in large part by the ability of the lamination press to achieve uniform plate temperature during the high temperature portion of the bonding process. The larger the variation in temperature across the plates of the alignment fixture, the larger the variation in resin flow and inter-layer adhesion within the multilayer panel. A hot oil press should be used for best results. Care should be taken so as not to overshoot the target product temperature if an electrically heated press is used. The press cycle recommended for use by Rogers that has been shown to produce ideal lamination results is shown in figure 3.42b.

Some of the limitations encountered during the lamination of the diplexer were:

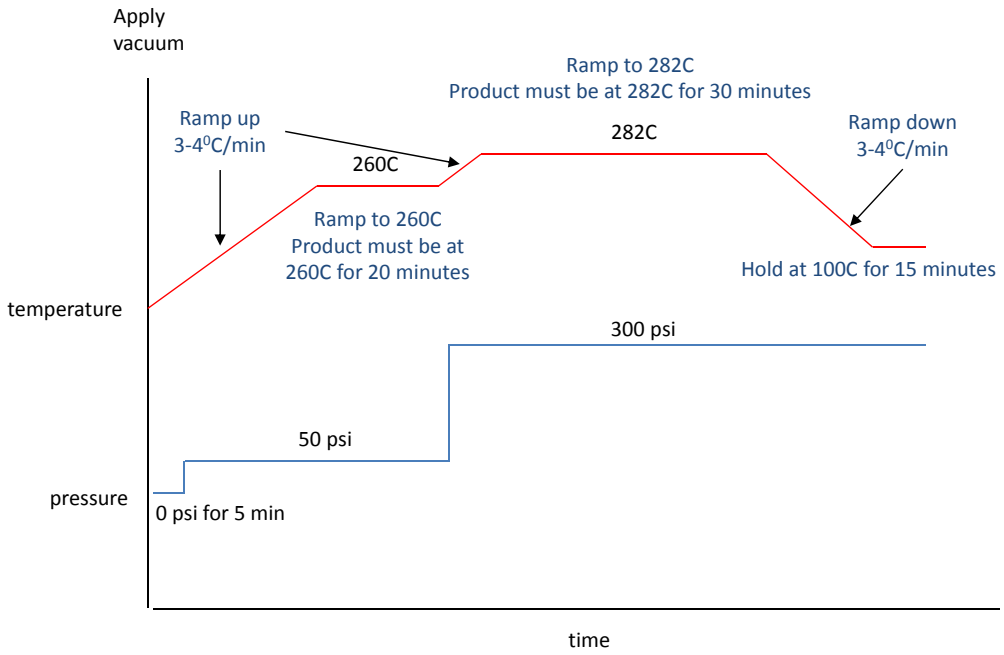
1. A manual lamination oil press was used that needed very close monitoring in order to regularly readjust the pressure whenever it dropped.

2. Several elements of the stackup recommended by Rogers were missing in the lamination stackup due to no availability. In fact, the multilayer part was placed directly in between

cleaned plates of the alignment fixture. However, circuits of lesser thicknesses have been fabricated successful with this limited arrangement.



(a) Rogers Recommended Stackup for Multilayer Bonding



(b) Recommended Temperature and Pressure Press Profile

Figure 3.42: Rogers Recommended Stackup for Multilayer Bonding and the Recommended Temperature and Pressure Press Profile

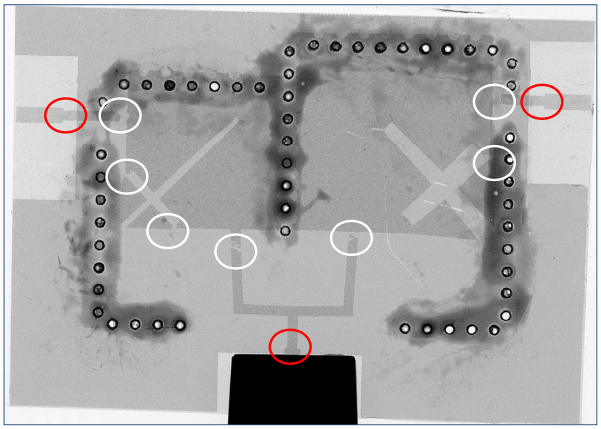
In acknowledging these limitations, the following aspects were of concern:

1. Whether the temperature within the stackup would be distributed uniformly enough to avoid non-uniform melting of the bonding ply which would affect the inter-layer adhesion of the core films.

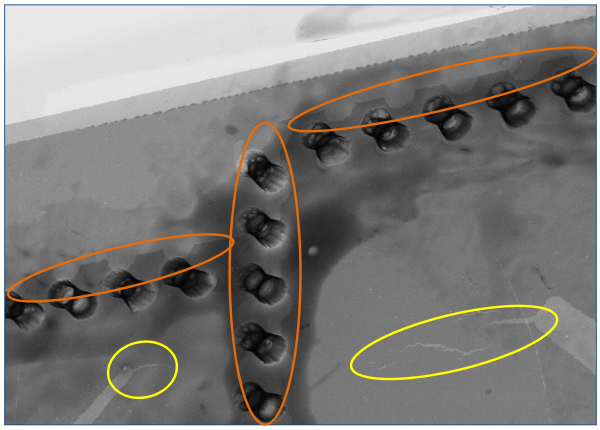
2. The effect that non-uniform pressure distribution would have on circuit performance, if the bonding film melts and flows in some areas before others. To avoid breaking of the circuit in the inner layers, a uniform pressure distribution is important.

3. The modulus of elasticity follows a very steep curve against temperature increase beyond the melting point of both Rogers Ultralam 3850 and 3908 and therefore very slight changes in temperature can result in undesirable effects. This is especially since the behaviour of these LCP films is so that they start to soften and at times become molten at temperatures of even 20 ^0C below the melting point.

The via holes of the diplexer were laser-drilled after lamination and were filled with conductive paste using a vacuum suction machine. The circuit was then dried in an electric oven set at 160 ^0C for approximately 40 minutes.



(a) Full View from the Top



(b) Slightly Tilted view of Vias

Figure 3.43: X-rays of the First Fabricated LCP Diplexer Circuit

The first measurement registered no continuity between all the ports when checked using a multimeter suggesting break points in the internal circuitry. As expected, the S-parameters measured on a VNA show a very high insertion loss and the two expected diplexer passbands could hardly be registered.

The circuit was x-rayed to gain better visibility of the inner circuit layer and breakages can clearly be seen in the x-rays which are shown in figure 3.43.

The white ovals show detachments of some parts of the circuit from others, the yellow ones show cracks in the circuit and orange ones show shifts of the vias from their intended positions or shifts in the metal cladding so that the via holes did not coincide with their slots in the metal layer. Red ovals clearly show shifts in the port lines. All these are most probably due to non-uniform melting of the bonding film and uneven flow of the resin resulting in uneven pressure distribution.

Subsequent fabrications sought to investigate the following aspects:

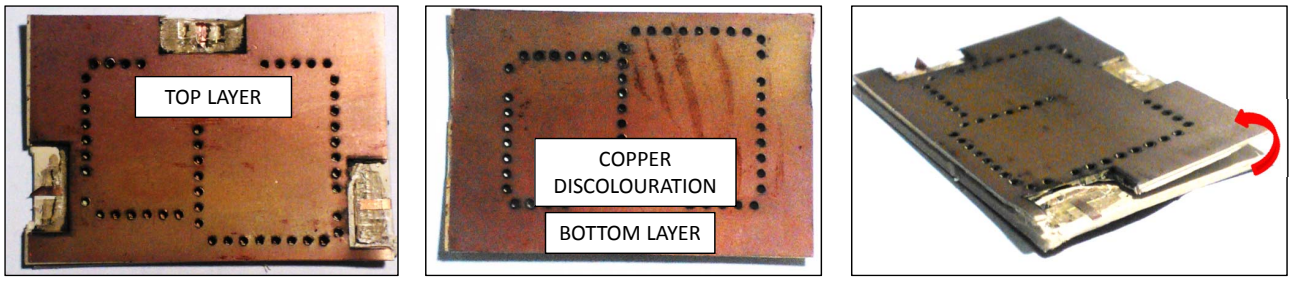
1. Whether a substrate height change to 0.7 mm would yield better results
2. Whether a slight change in the lamination profile would make a difference supposing:

- the pressure over a set time span is reduced
- the time span at a set pressure is reduced so that the pressure is applied for a lesser time period while maintaining temperature as per the original Rogers press profile.

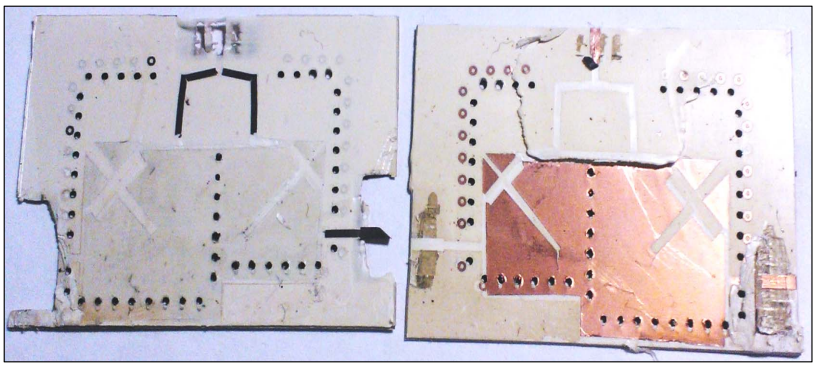
An initial fabrication on a 0.7 mm substrate-only stackup, following the recommended Rogers press profile, also registered breakages in the internal circuitry. The same happened when two different lamination profiles were attempted based on the two points above. It became evident that whilst it could not be concluded that fabrication of thicker LCP multilayer circuits (> 0.5 mm) was impossible, realisation of a working lamination profile could take many iterations.

With all this in mind, it is important to acknowledge that LCP, as a multilayer circuit technology, is in contention with other multilayer technology systems such as PCB which also produces low cost circuits. Depending on material choices, these alternative multilayer circuit technologies can also exhibit good electrical and mechanical properties. Furthermore, these technology systems are already better established and offer better guarantee of fabrication success. It therefore becomes impractical to spend a lot of resources working on obtaining a viable LCP lamination profile for thicker circuits if a different, better established, system can be employed.

Some images showing the breaks and cracks in the other fabricated circuits are shown in figure 3.44. In the absence of an x-ray machine, the circuits were slit open horizontally to expose the inner conducting layer.



(a) Fabricated LCP Diplexer cut horizontally to view breakage points



(b) Middle Metal Layer

Figure 3.44: Images of Breaks and Cracks in Failed Fabrications

3.13 Conclusion

This chapter has presented a folded SIW filter with a second order response obtained through a cross-slot coupling technique. The structure has been analysed in detail by studying the behaviour of its simulated electromagnetic field patterns and densities to understand its performance properties.

A circuit model has been derived to aid in the modelling of the filter and has been shown to approximate the behaviour of the 3D model of the filter satisfactorily.

Different characteristics of the filter have been presented and a diplexer has been designed using two of the filters. Diplexer results have been presented for two multilayered circuit technologies: PCB and LCP. PCB multilayered fabrication has been shown to been successful in producing a working circuit. Resulting passbands have been seen to have shifted upwards in frequency from the design center frequencies an aspect that can be attributed to possible shrinkage of the circuit during fabrication. A high insertion loss of approximately 9.3 dB is also obtained for the second passband whereas the first passband registers a better insertion loss of about 2.75 dB. The poor insertion loss for the second passband has been attributed to possible cracking of the metal in the internal layer.

LCP fabrication is shown to have been unsuccessful and would possibly require a lengthy experimental period to come up with a lamination profile suitable for substrate thicknesses greater than

0.5 mm.

It has also been concluded that in the presence of other fabrication technologies that can achieve similar electrical and mechanical properties as those sought from LCP as a dielectric material, it is preferable to choose those.

Chapter 4

Ridge-like FSIW Filters with Wide Stopbands

4.1 Introduction

In filter design, both passband and stopband performance are typically specified by system designers. In particular, certain applications require very wide stopbands with high attenuation. In such instances, filters such as ridge waveguide filters whose first spurious response appears at appreciable distances from the main passband become attractive.

Ridge waveguide filters, as the name suggests, are formed from conventional waveguide structures with a metallic ridge strategically placed within the waveguide. This ridge manipulates the electromagnetic fields within the waveguide in a manner that enables the cutoff frequencies of the modes to be changed. By doing this, the width of the stopband can either reduce or increase substantially. The increase or decrease is dependent on the shape of the ridge and its position within the waveguide with regard to the electromagnetic field distribution of the different modes.

Substrate integrated waveguides have been introduced in chapter 3 as a technology for the miniaturisation of waveguide components. They offer the advantages of lower insertion loss, higher quality factor and higher power handling capability in a planar-like platform.

Chapter 3 also discussed the folding of SIW structures into a quarter wavelength structure to reduce the overall footprint of a conventional SIW to 25 percent of its original size.

SIWs have also been shown to be realisable in multilayered circuit technology allowing for more flexible and creative design options. The presented quarter wavelength resonators and the filters designed from them, however, had a narrow stopband between the fundamental passband and the first spurious response. This chapter discusses the application of SIWs in realising a different waveguide structure - a ridge-like folded SIW that results in a wider stopband. The structure resembles that of a ridge substrate integrated waveguide, but the differences between the two are investigated later on in the chapter.

Ridge SIWs (RSIWs) were first reported in [31] where a metal ridge in the form of a series of

periodic metallised posts along the center line of an SIW was proposed with the aim of improving the bandwidth of an SIW. Simulations in full-wave electromagnetic software confirmed the increase in SIW bandwidth. Since then, RSIWs have been applied in the design of different RF and microwave structures such as hybrid ring couplers [43], antennas [66][42], power dividers [62] and filters [45][90][89]. In these structures, the basic structure of a ridge in waveguide is utilised.

The chapter presents a folded SIW (FSIW) topology that has the characteristics of a folded waveguide and will be denoted 'Ridge-like FSIW'. This topology results in a cutoff frequency of the fundamental mode that is lowered more than that of a conventional ridge waveguide while maintaining that same size of waveguide. A comparative analysis of the two waveguide structures is presented, focusing mainly on the effects of changes in their cross-sectional dimensions on the cutoff frequency of the first two modes. By doing this, the possible operational frequencies of these two waveguides can then be established.

Based on the ridge-like FSIW cross-sectional properties, and bearing in mind the electromagnetic field distribution and strength within a waveguide, two cavity resonators with these cross-sectional properties are compared. The first is a substrate integrated equivalent of a waveguide folded using a technique that was first proposed in [65] and is to be discussed in later sections. The second, is a new topology that is proposed in this chapter. This new topology seeks to further increases the width of the stopband as well as the unloaded quality factor beyond that achievable by the former mentioned topology. The new shape takes advantage of the field distribution within a ridged cavity and allows for constructive overlap reducing the frequency shift of the second resonant mode to lower frequencies. The two resonators are compared in terms of resonant frequency and unloaded quality factor achievable by either.

The sections that follow discuss the application of the proposed ridge-like FSIW resonator topology in filter design. Two X-band miniaturised filters are presented - a second order one and a fourth order one. All the circuit models in this chapter are implemented and analysed in AWR's Microwave Office. The three dimensional equivalents are simulated in CST, a full wave electromagnetic simulation software.

Similar to chapter 3, PCB multilayered technology is chosen for the fabrication of the designs in this chapter due to its lower costs and relatively easy fabrication. Measured results verify the properties of the ridge-like FSIW filters and these are presented and analysed before concluding the chapter.

4.2 Ridge waveguides

The field distribution for the first 4 modes of a rectangular dielectric filled waveguide resonator is shown in figure 4.1. The colour scales define the parts of the cavity in which the fields are strongest. From the general description of resonant frequency

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{4.1}$$

it can be deduced that when the electromagnetic fields within the cavity are perturbed, an increase in either the overall equivalent inductance or capacitance relating to the electric and magnetic fields respectively within the cavity for a specific resonant mode will decrease its resonant frequency.

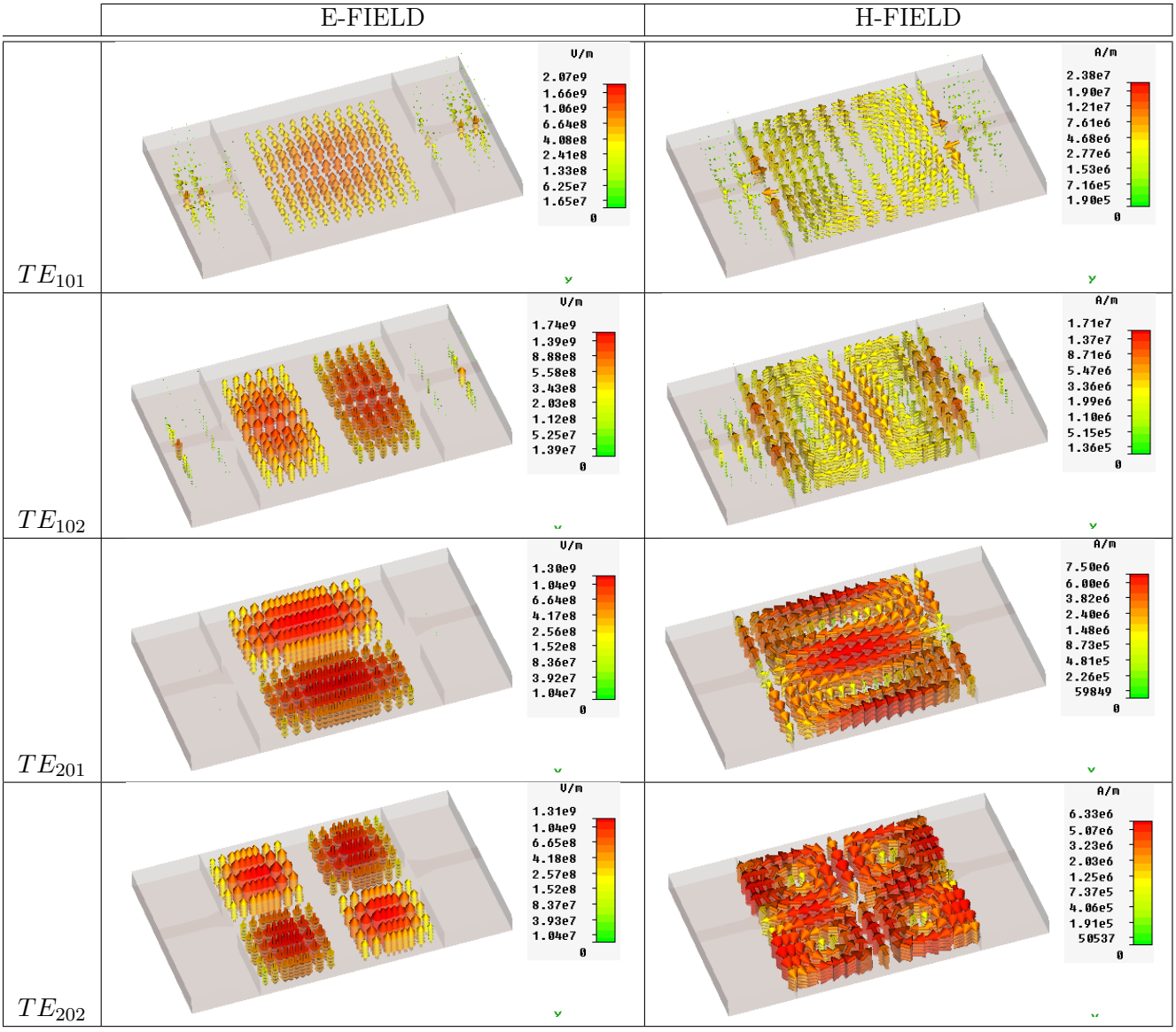


Figure 4.1: Electromagnetic Fields of the First Four Square Cavity Resonator Modes in a Standard Substrate-Loaded Waveguide Cavity

These field distributions of the different resonant modes can also be seen to overlap at certain regions in the cavity and therefore, if a ridge is placed within the cavity, it is expected that depending on its position, shape and its size, it can have an effect on the resonant frequency of several resonant modes.

Figure 4.2 shows the real part of E_y for the first few TE_{mnl} modes, with the subscripts m, n and l defining the number of half cycles of a mode's equivalent standing wave in the x, y and z axes of the resonator respectively.

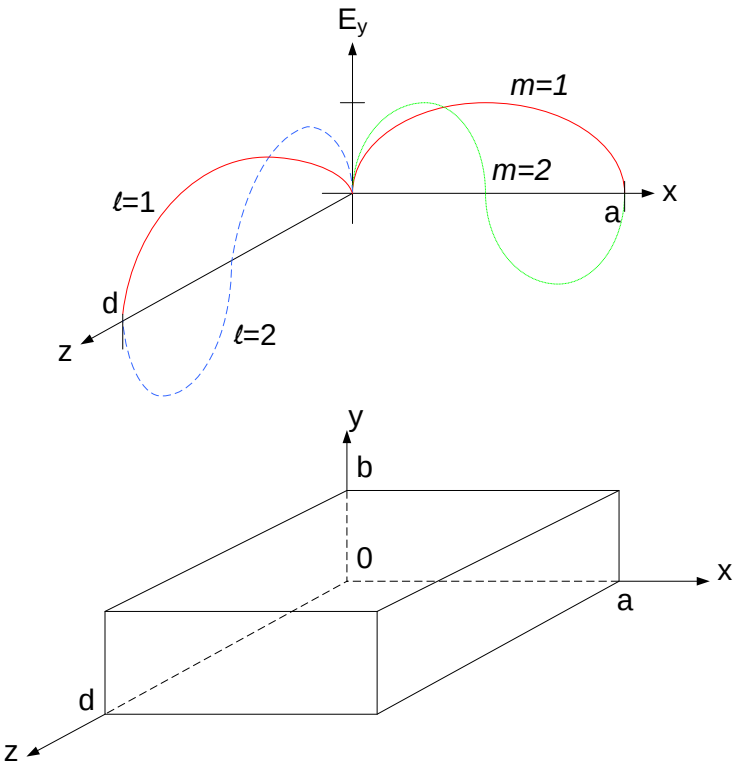


Figure 4.2: Rectangular/Square Cavity Resonator and the Variations of the Electric Field for the TE_{101}, TE_{102} and TE_{201} Resonant Modes

Figure 4.3 shows an approximated figure demonstrating the overlapping of the first 3 rectangular/square cavity resonant modes previously shown in figure 4.1. In order to only reduce the resonant frequency of the fundamental mode, a very small square ridge would be positioned in the center red region of the cavity. This would be expected to reduce the distance between the top and the bottom walls of the cavity. By doing that, the cutoff frequency of the $TE101$ mode can be reduced so that a lower resonant frequency can also be achieved.

However, as has been shown, the strengths of the electric field for different modes varies within the cavity and is only strongest in specific regions. For the $TE101$ resonant mode, the intensity of the electric field is highest at the center of the cavity ($\lambda/4$ from the edge) and reduces sinusoidally to null at the shorted ends of the cavity. For the $TE102$ mode, the electric field intensity is highest at the 0.125λ and 0.375λ points of the $TE101$ resonant mode in the z-axis and at the quarter wavelength point of the fundamental mode, in the x-axis. As the overlapping surface area of the ridge increases to cover the other modes, their cutoff frequencies can also be expected to decrease. The size of the ridge must therefore be chosen depending on the minimum width of the stopband that is being sought as well as the desired fundamental mode resonant frequency.

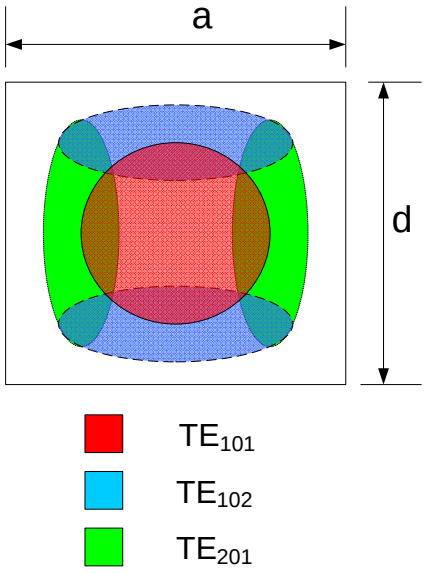


Figure 4.3: Overlapping of Electric Energy for the First Four Square Resonator Cavity Modes

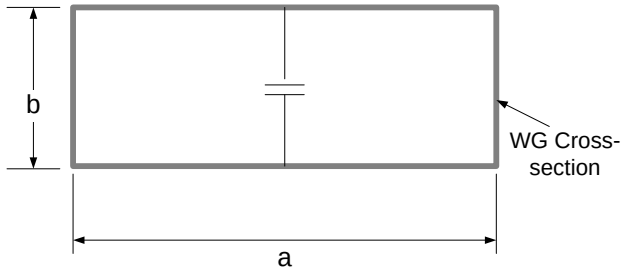
Figure 4.4 shows a conventional waveguide, a ridge waveguide made up of a uniform rectangular waveguide and a double ridge waveguide.

The discussions in this chapter lead towards the development of a new topology of a ridge-like folded waveguide resonator realised in a substrate integrated circuit platform. To arrive at that point, the conventional ridge waveguide will be briefly discussed and there after the substrate integrated equivalent will be analysed before developing our specific design.

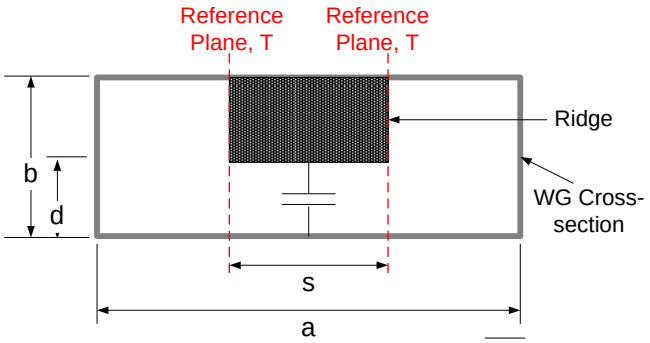
4.2.1 Closed Form Expressions for Dominant Mode Ridge Waveguide Characteristics

As with a conventional waveguide, the characteristics of a ridge waveguide can usually be defined in terms of the propagation constant and the characteristic impedance for each mode. The characteristic impedance can be represented in the form of a voltage-current relationship, power-voltage relationship or a power-current relationship.

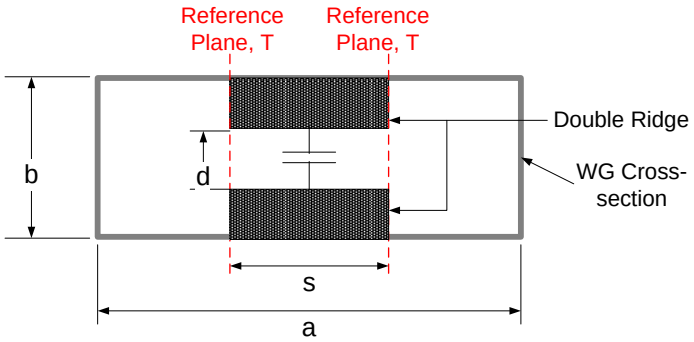
The cutoff frequency of the modes in a ridge waveguide can be altered by adjusting the dimensions d and s while maintaining the outer dimensions a and b (see figure 4.4).



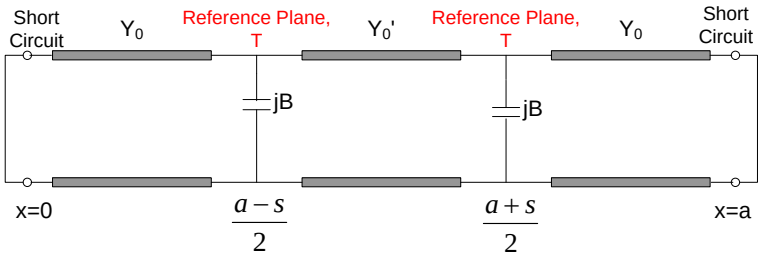
(a) Conventional Waveguide



(b) Ridge Waveguide



(c) Double Ridge Waveguide



(d) Equivalent Ridge Waveguide Cross-section Circuit Model

Figure 4.4: Concept of a Ridge Waveguide

Various field-theory approaches exist in literature for the characterization of ridge waveguides [22]. However, most of the presented techniques are either based on approximate equations defining the field distribution in the ridge waveguide or they ignore the effect of the finite metallization thickness [22]. Both of these, however, are important for reliable filter designs.

The propagation constant can be adequately defined if the wave cutoff number of each mode in the guide is known.

4.2.1.1 Cutoff Condition

In [50], the cutoff frequency of the fundamantal mode of a waveguide is established by applying the transverse resonance method (TRM). TRM is based on the condition that if wave propagation is considered to be in the x direction, an inhomogeneous waveguide cross-section can be regarded as a transmission line divided into homogenous sub-regions [22]. An equivalent circuit representing three different line sections of the cross-section of a ridge waveguide is shown in figure 4.4d.

If the cross-sectional area in figure 4.4b and 4.4c and vertical symmetry about the center are considered, the equivalent transverse network for the dominant mode comprises a shunt junction capacitance at the reference plane, T, and two transmission lines on either side of the junction - one short circuited and the other open circuited. The cutoff condition of the dominant mode can then be determined by the resonance condition at the plane, T, which requires that the sum of all the admittances at a shunting node of a circuit be zero. This is determined by [67]

$$\frac{Y_0'}{Y_0}\tan\frac{\pi}{\lambda}s + \frac{B}{Y_0} - \cot\frac{\pi}{\lambda_c}(a-s) = 0 \tag{4.2}$$

where

$$\frac{Y_0'}{Y_0} = \frac{b}{d} \tag{4.3}$$

$$Y_0 = \frac{k_c}{\omega\mu_0}\left(\frac{1}{b}\right) \tag{4.4}$$

$$Y_0' = \frac{k_c}{\omega\mu_0}\left(\frac{1}{d}\right) \tag{4.5}$$

Equation 4.2 yields the same λ_c for both single- and double-ridge guides if the gap height d of the single-ridge is one half the gap height d of the double-ridge guide. The equivalent network is only valid in the wavelength range $^{2b}/_{\lambda_c} < 1$ for the single-ridge and $^{b}/_{\lambda_c} < 1$ for the double-ridge.

In equations 4.4 and 4.5, k_c is the cutoff wave number and is related to the cutoff wavelength by

$$k_c = \frac{2\pi}{\lambda_c} \tag{4.6}$$

and $^{B}/_{Y_{01}}$, in equation 4.2, represents the step discontinuity on either side of the ridge. Its approximation in the case of a single ridge waveguide is given as [50]

$$\frac{B}{Y_{01}} \approx 4\left(\frac{b}{a}\right)\left(\frac{a}{\lambda_c}\right)\ln\csc\left(\frac{\pi d}{2b}\right) \tag{4.7}$$

and for the case of a double ridge waveguide, the corresponding result is

$$\frac{B}{Y_{01}} \approx 2\left(\frac{b}{a}\right)\left(\frac{a}{\lambda_c}\right)\ln\csc\left(\frac{\pi d}{2b}\right) \tag{4.8}$$

A closed form approximation for the cut-off wavelength of the dominant mode in a double ridge dielectric-filled waveguide is presented in [53] as

$$\begin{aligned}\frac{b}{\lambda_c} &= \frac{b}{2\sqrt{\varepsilon_r}\,(a-s)}\left[1+\frac{4}{\pi}\left(1+0.2\sqrt{\frac{b}{a-s}}\right)\left(\frac{b}{a-s}\right)\ln\csc\left(\frac{\pi d}{2b}\right)\right. \\ &\quad \left.+\left(2.45+0.2\frac{s}{a}\right)\left(\frac{sb}{d(a-s)}\right)\right]^{-\frac{1}{2}}\end{aligned} \tag{4.9}$$

The corresponding approximate single ridge solution is obtained by replacing b with $2b$ in the coefficient multiplying the log term [50]

$$\begin{aligned}\frac{b}{\lambda_c} &= \frac{b}{2\sqrt{\varepsilon_r}\,(a-s)}\left[1+\frac{4}{\pi}\left(1+0.2\sqrt{\frac{2b}{a-s}}\right)\left(\frac{2b}{a-s}\right)\ln\csc\left(\frac{\pi d}{2b}\right)\right. \\ &\quad \left.+\left(2.45+0.2\frac{s}{a}\right)\left(\frac{sb}{d(a-s)}\right)\right]^{-\frac{1}{2}}\end{aligned} \tag{4.10}$$

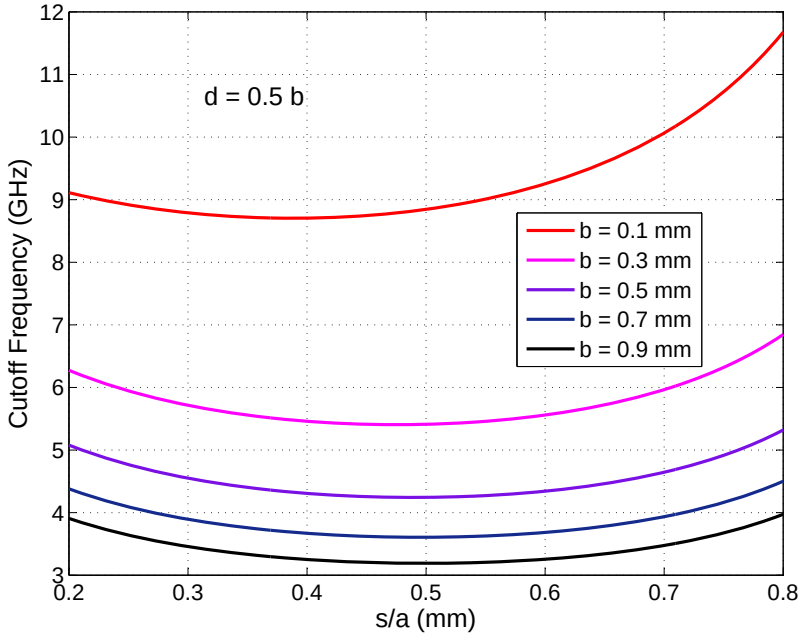
These representations agree with full wave numerical methods within 1% provided that

$$0.01 \leq \frac{d}{b} \leq 1 \tag{4.11}$$

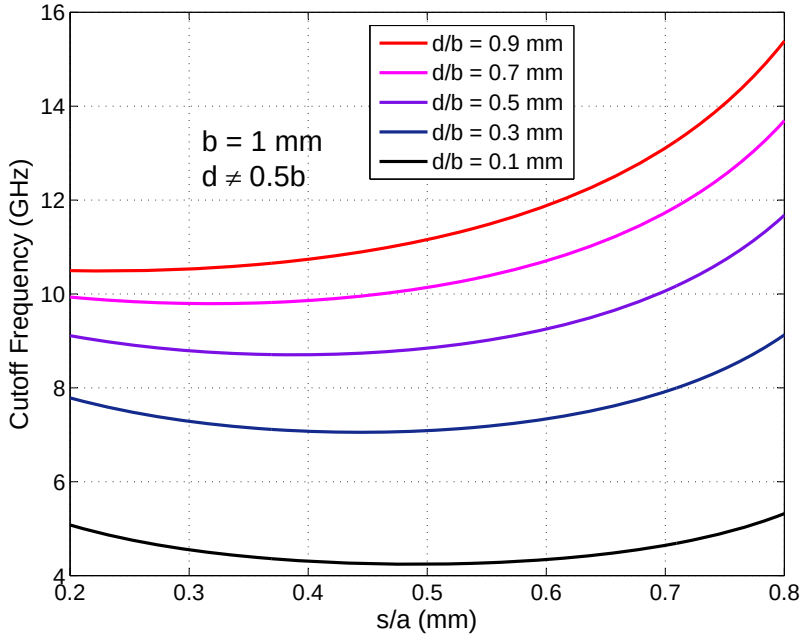
$$0 \leq \frac{b}{a} \leq 1 \tag{4.12}$$

$$0 \leq \frac{s}{a} \leq 0.45 \tag{4.13}$$

For a waveguide with a fixed width of $a = 7.47\,mm$, the cutoff frequency is plotted against the aspect ratio s/a for two cases in a single ridge waveguide: $d/b = 0.5$ and $d \neq 0.5b$. The width is chosen to match an SIW equivalent width of 8 mm that is used for filter designs later in the chapter. The dimensions a, b, s and d match those in figure 4.4b. These plots are shown in figure 4.5.



(a) Case 1: $d = 0.5b$



(b) Case 2: $d \neq 0.5b$

Figure 4.5: Dominant Mode Cutoff Frequency of Single Ridge Waveguide Versus Aspect Ratio s/a

The plots show that the cutoff frequency decreases with an increase in the height of the waveguide, for a gap dimension $d = 0.5b$. When the gap dimension, d, varies in relation to a fixed height, b, of the waveguide i.e $d \neq 0.5b$ (see figure 4.5b), then a decrease in the gap dimension, d, results in a lower cutoff frequency.

The results of the curves are subject to the conditions in equations 4.11, 4.12 and 4.13 and are

used in comparisons in later sections.

The equations in this subsection provide good initial values for variables in equation 4.2, and it can then be solved for specific unknowns.

4.2.1.2 Power Flow

The power flow in a ridge waveguide at infinite frequency can be described, for both a single ridge and a double ridge, as [50]

$$P_t = \left(\frac{E_0^2 d^2}{2\pi\eta_0}\right)\left\{\left(\frac{d}{b}\right)\left(\frac{b}{a}\right)\left(\frac{2ma}{\lambda_c}\right)\ln\csc\left(\frac{\pi d}{2b}\right)\cos^2\theta_2 + \frac{\theta_2}{2} + \frac{\sin 2\theta_2}{4}\right. \tag{4.14}$$

$$\left. + \left(\frac{d}{b}\right)\left(\frac{\cos\theta_2}{\sin\theta_1}\right)^2\left[\frac{\theta_1}{2} - \frac{\sin 2\theta_1}{4}\right]\right\}\left(\frac{a}{b}\right)\left(\frac{b}{d}\right)\left(\frac{\lambda_c}{a}\right) \tag{4.15}$$

and at finite frequency

$$P_t(\omega) = P_t(\infty)\left(\frac{\lambda_0}{\lambda_g}\right) \tag{4.16}$$

where λ_g is the guided wavelength and is given by

$$\lambda_g = \frac{\lambda_0}{\sqrt{\varepsilon - \left(\frac{\lambda_0}{\lambda_c}\right)^2}} \tag{4.17}$$

In equation 4.14, the lumped element susceptances of single and double ridge waveguides are accounted for by setting $m = 2$ and $m = 1$ respectively. The peak electric field intensity at the center of the waveguide, E_0, is computed as

$$E_0 = \frac{V}{d} \qquad (V/m) \tag{4.18}$$

4.2.1.3 Characteristic Impedance

As mentioned earlier, the characteristic impedance of a ridge waveguide can be defined using a voltage-current formulation, a power-voltage definition and power-current definition. The detailed derivation of these can be obtained in [50], but the equations are summarised for a single ridge waveguide in terms of the gap-factor d/b with an aspect ratio of $s/a = 0.50$ as

$$Z_{VI} = -226.57\left(\frac{d}{b}\right)^4 + 414\left(\frac{d}{b}\right)^3 - 201.51\left(\frac{d}{b}\right)^2 + 279.86\left(\frac{d}{b}\right) + 0.6237 \tag{4.19}$$

$$Z_{PV} = -274.75\left(\frac{d}{b}\right)^4 + 495\left(\frac{d}{b}\right)^3 - 168.5\left(\frac{d}{b}\right)^2 + 286.73\left(\frac{d}{b}\right) + 0.5054 \tag{4.20}$$

$$Z_{PI} = -192.67\left(\frac{d}{b}\right)^4 + 368.41\left(\frac{d}{b}\right)^3 - 241.38\left(\frac{d}{b}\right)^2 + 274.11\left(\frac{d}{b}\right) + 0.717 \tag{4.21}$$

The formulas above relate to a conventional ridge waveguide.

For a substrate integrated equivalent, the vertical solid walls of the cavity are replaced by a row of vias, dimensions of which were previously discussed in chapter 3. The horizontal walls of the cavity are realised using conducting plates, usually in the form of metal cladding for PCB substrates. The rectangular/square ridge is also realised using a row of vias arranged to form a rectangle/square, with one end shorted on the lower wall of the cavity and the other on a top plate that forms the top surface of the ridge. It is shown in the next section that depending on the position of these vias below the 'ridge-plate', the structure will either be an SIW or a 'ridge-like' FSIW.

4.3 Comparison of RSIW and Ridge-like FSIW

The properties of ridge waveguide and RSIW are well documented. The ridge-like FSIW was first introduced by [65] in the form of a doubly folded structure as shown in figure 4.6, but very little detail is supplied on the structure. This section presents a detailed study of the properties of this type of structure in comparison with RSIW.

The proposed folding concept suggests that a conventional waveguide is folded from all sides while maintaining symmetry as shown and the resulting structure in then implemented with a flat plate inside a cavity with equal slots all around and a vertical standing post as shown. The top and side views for the two topologies are shown in figures 4.7 and 4.8 respectively for solid ridges and their via wall equivalents.

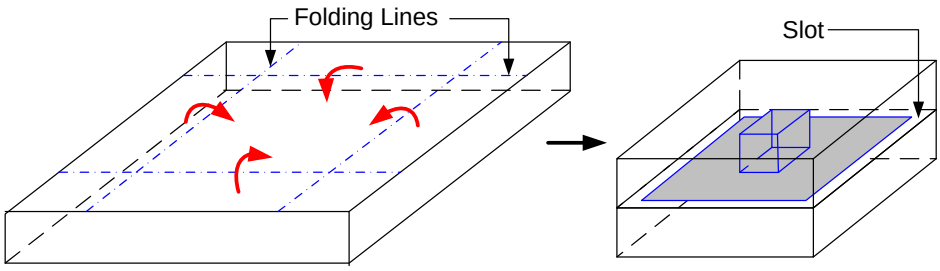
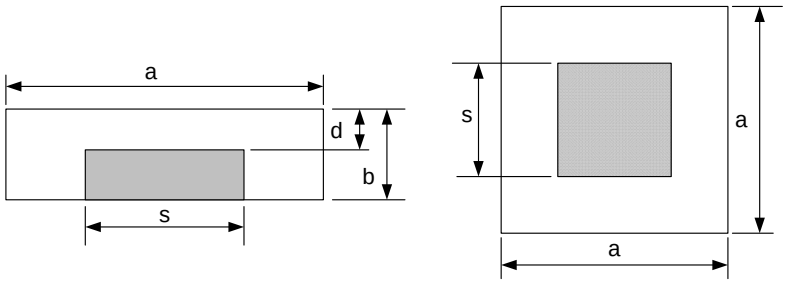


Figure 4.6: Folding of Ridge-like Waveguide

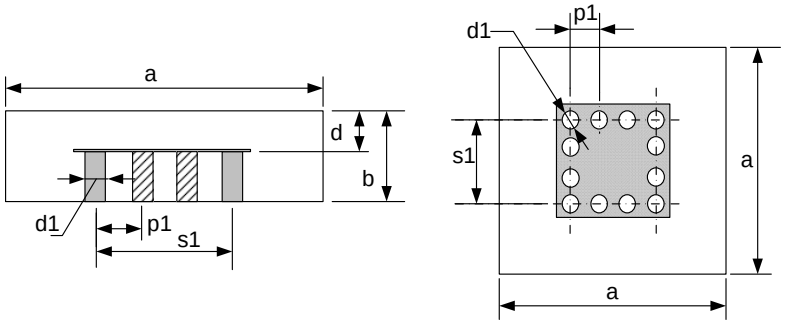
The width of the solid ridge, s, is computed in relation to the SIW equivalent, s1, using equation 4.22 [32]

$$s = s1 - 1.08 \times \frac{d^2}{p1} + 0.1 \times \frac{d^2}{s1} \tag{4.22}$$

where d is the gap dimension between the ridged part of the waveguides and the top wall of the waveguide and p1 is the pitch between two adjacent vias.

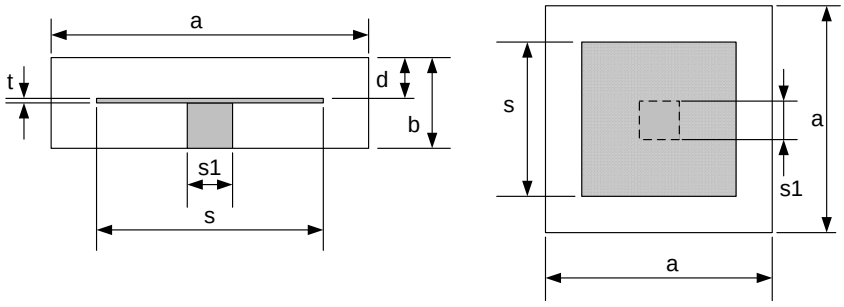


(a) Solid Ridge - Side View (b) Solid Ridge - Top View

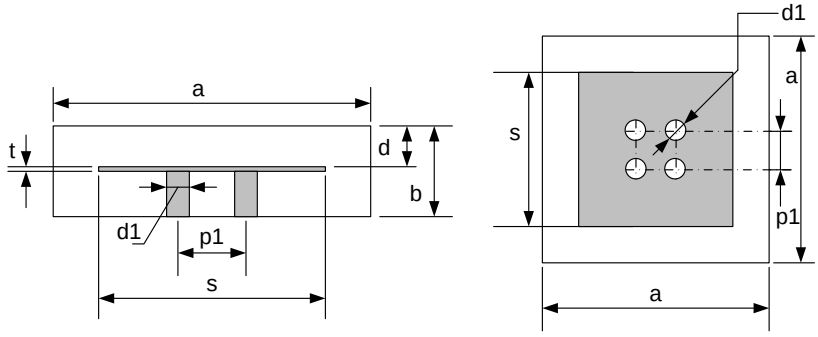


(c) Via Walls - Side View (d) Via Walls - Top View

Figure 4.7: Realisation of Square Ridge SIW



(a) Solid Post - Side View (b) Solid Post - Top View



(c) Via Walls - Side View (d) Via Walls - Top View

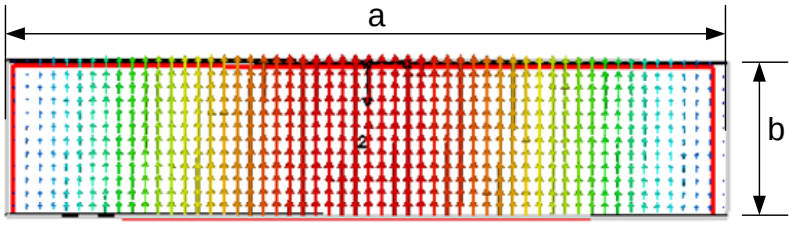
Figure 4.8: Realisation of Square/Rectangular Ridge-like FSIW

The top views of both waveguides are similar but the side view defines the difference between the two. The square ridge waveguide uses a block of cube-shaped metal to form the ridge whereas the square ridge-like folded waveguide uses a thick rectangular post that supports a flat metal plate. The difference can also be seen for the SIW equivalent which replaces the central vertical standing perturbing sections with via walls. The cutoff frequency of the square ridge-like folded waveguide is lowered by increasing the size of the plate about the supporting post. The post also grounds the plate and the magnetic field is strongest about the post.

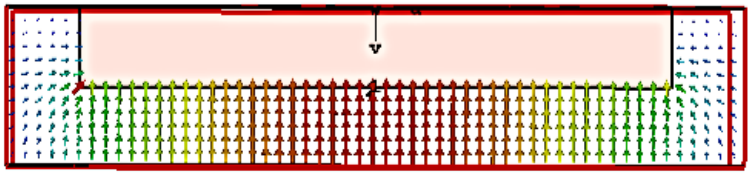
The electric field is strongest at the center of the waveguide and between the top of the central perturbing sections and the top wall of the waveguide. The field lines bend about the corners in both cases as shown in figure 4.9. Figure 4.9 also shows the electric field lines on a cross-sectional view of a conventional waveguide of identical outer dimensions to the other two.

The simulated cutoff frequency for the conventional waveguide with the dimensions $a = 7.47\,mm$ and $b = 1.016\,mm$ and filled in dielectric with a relative permittivity of 3.38 is 10.64 GHz and the calculated one is 10.92 GHz.

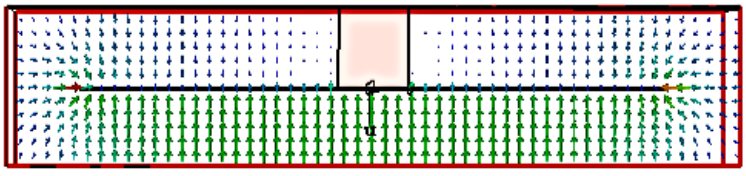
The other two resonators are analysed to determine the effect of dimensional changes on the cutoff frequencies of the first two modes.



(a) Conventional Waveguide



(b) Square Ridge Waveguide



(c) Square Ridge-like Folded Waveguide

Figure 4.9: Cross-Section View of Bending Electric Field Lines at the Centre of Waveguides

4.3.1 Effects of Dimensional Variations on Cutoff Frequency

The effects of dimensional variations on the cutoff frequency are investigated using CST full-wave electromagnetic simulations and are presented in the following subsections. The analysed waveguide topologies have the cross-sectional views shown in figure 4.8a and 4.7a respectively. These are depicted in figure 4.10. In the waveguides, the ridge extends throughout the length of the waveguide. The cutoff frequency is computed based on the cross-sectional topology and dimensions of the waveguide at the open-circuited ends. The electric field of electromagnetic waves travelling longtudinally along a half wavelength waveguide is maximum at the open-circuited ends. In a rectangular resonator, the electric field is maximum at the centre of the resonator. For this reason, the lowest operational frequency of ridge and ridge-like resonators discussed in this chapter are based on cutoff frequencies of waveguides with ridge structures corresponding to the shape and centre dimensions of the perturbation in the resonators.

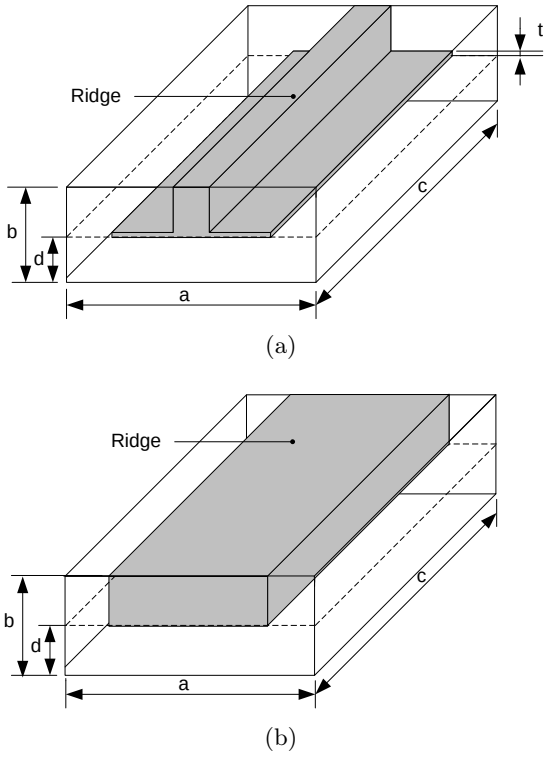


Figure 4.10: Ridge structures in rectangular waveguides

4.3.1.1 Cutoff Frequency Versus height, b - For $d = 0.5b$

The ridge-like FSIW is shown to achieve lower cutoff frequencies (more than 3 GHz lower) than those achievable by the RSIW, for the fundamental mode. The width s is set to 6 mm and the waveguide width, a, is 7.47 mm.

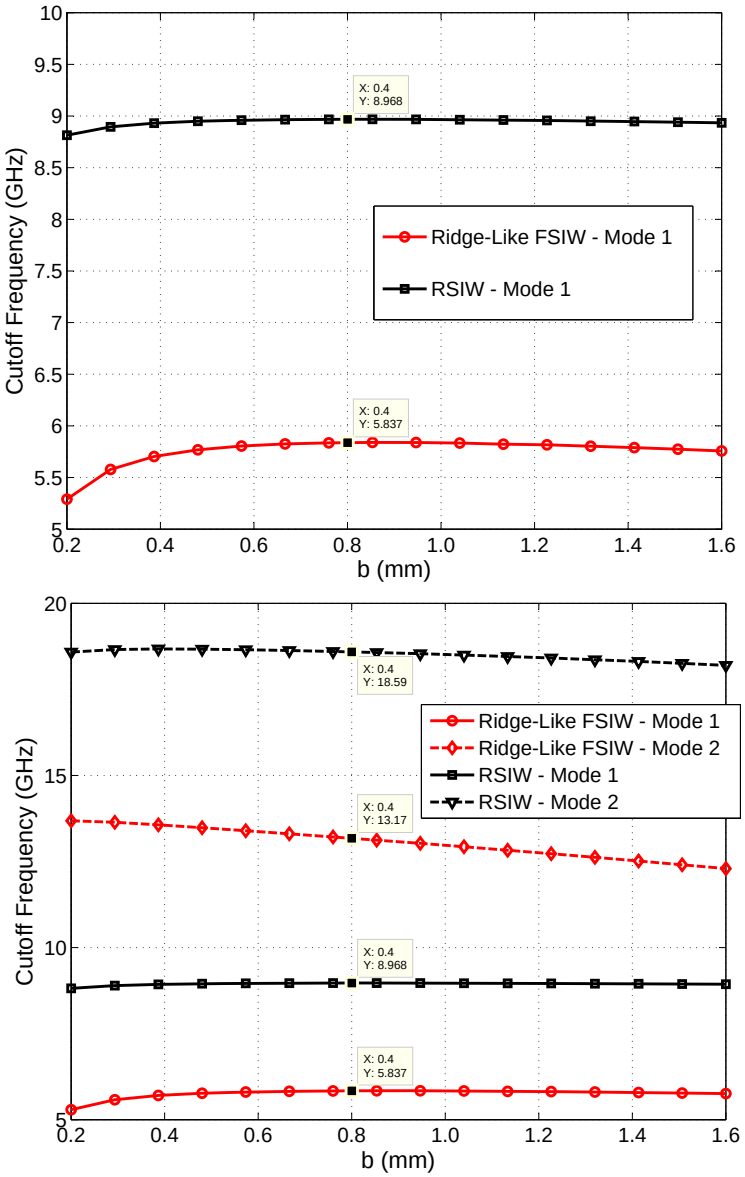


Figure 4.11: Cutoff Frequency of Mode 1 and 2 Versus height, b - For $d = 0.5b$

For either topology, the second mode's cutoff frequency is greater than twice that of the fundamental mode for the range of $0.2\,mm \leq b \leq 1.6\,mm$.

The plotted results also show, that for a fixed ratio $d/b = 0.5$, the cutoff frequency for both modes doesn't change significantly with an increase in the guide height.

4.3.1.2 Cutoff Frequency Versus Gap Size, d, for fixed b

For a set ridge width, $s = 6\,mm$ and a waveguide width, $a = 7.47\,mm$, the cutoff frequency is plotted against the gap dimension, d, for a fixed waveguide height of $b = 1.6\,mm$.

It is shown that the cutoff frequency of the first mode decreases with a decrease in the gap size. It is also shown that the ridge-like FSIW achieves lower cutoff frequencies for both the first and

second resonant modes for the equivalent RSIW values of d.

The cutoff frequency for the second resonant mode for the ridge-like FSIW decreases with an increase in the gap size, d, with a very mild slope. The RSIW equivalent, however, increases with an increase in d.

These observations aid in choosing a resonator that can resonate at low frequencies and is of a small size that would normally have a much higher cutoff frequency in the case of a conventional waveguide. A cutoff frequency of less than 2 GHz can be achieved with a Ridge-Like FSIW structure if a very thin gap of 0.1 mm is chosen, which is more than 8 GHz lower than the cutoff frequency of a conventional waveguide of the same size.

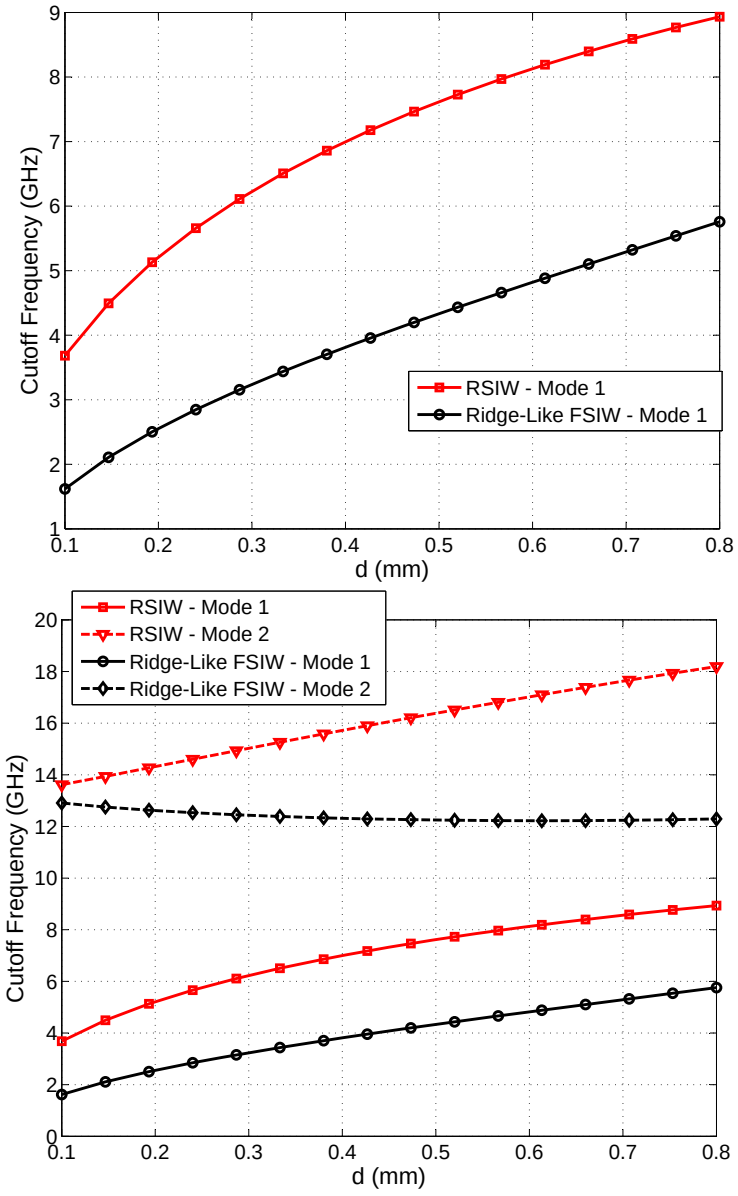


Figure 4.12: Cutoff Frequency of Mode 1 and 2 Versus Gap Size, d, for fixed $b = 1.6\,mm$

4.3.1.3 Cutoff Frequency Versus width, s, for fixed a, b, s1 and d

With the dimensions, a, b and d fixed to $a = 7.47\,mm$, $b = 1.016\,mm$ and $d = 0.5b$, and the width of the post for the ridge-like FSIW, s1, set to $s1 = 0.72\,mm$, the cutoff frequency is plotted, in figure 4.13, against the dimension, s.

The cutoff frequency of the fundamental mode for the RSIW has a minima when the ratio $s/a \approx 0.45\,mm\,to\,0.5\,mm$. The Ridge-Like FSIW cutoff frequency for mode 1, on the other hand, decreases gradually with an increase in s over the simulated range of $1\,mm \leq s \leq 6\,mm$. It is also shown that for this range of variation, the Ridge-Like FSIW achieves a lower cutoff frequency with the difference becoming more significant from that of an RSIW as s increases.

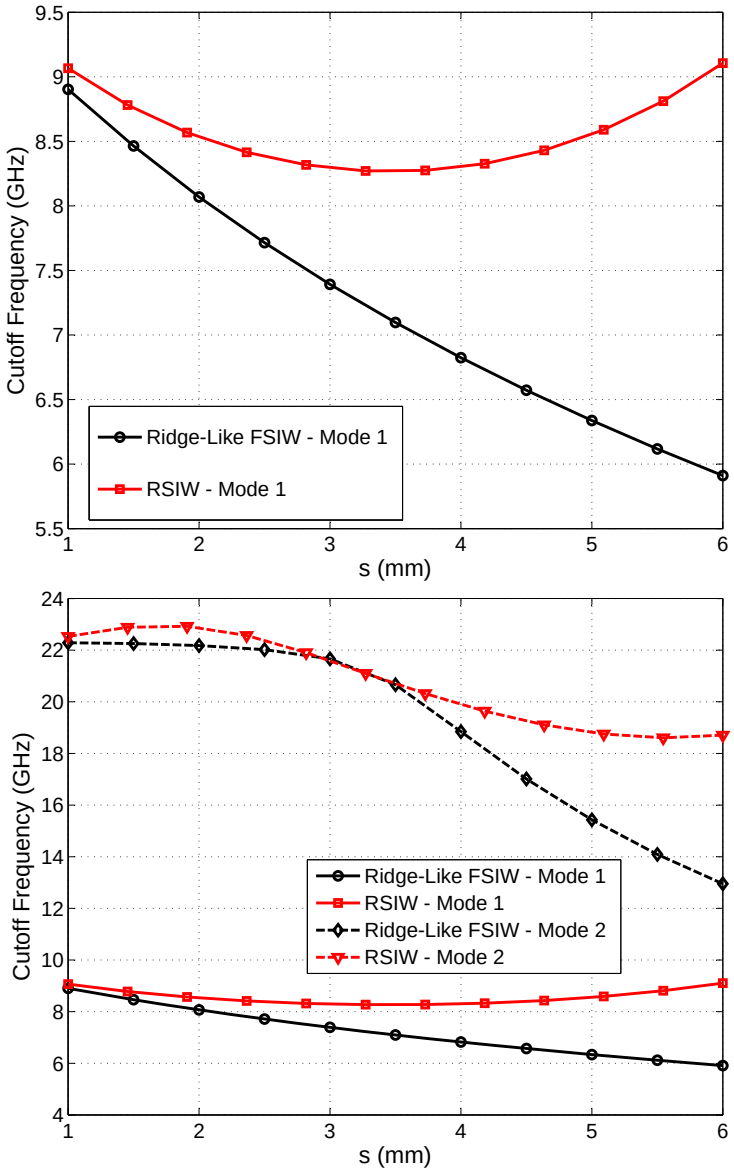


Figure 4.13: Cutoff Frequency of Mode 1 and 2 Versus Width, s, for fixed $b = 1.016\,mm$, $a = 7.47\,mm$, $s1 = 0.72\,mm$ and $d = 0.5b$

For $s >\approx 3.5\,mm$ the cutoff frequency of the second resonant mode for both topologies decreases faster with a change in s than in does for lower values of s.

4.3.1.4 Cutoff Frequency Versus width of Square Post, s1, for fixed a, b, s and d

For a ridge-like waveguide with fixed dimensions $b = 1.016\,mm$, $a = 7.47\,mm$, $s = 6\,mm$ and $d = 0.5b$, it is shown that both the cutoff frequencies of the first two resonant modes increase gradually with an increase in the size of the square post. This is observed for a variation range of $0.5\,mm \leq s1 \leq 6\,mm$. At $s1 = 6\,mm$, the structure becomes a full ridge waveguide.

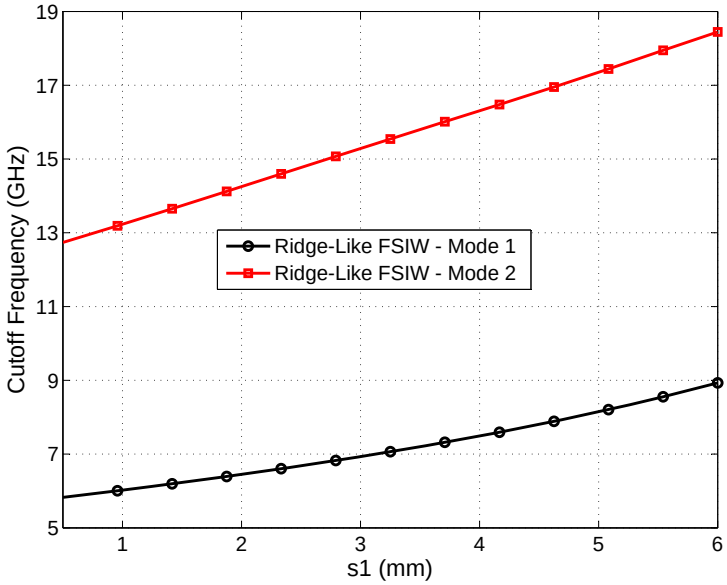


Figure 4.14: Cutoff Frequency of Mode 1 and 2 Versus Width of Square Post, s1, for fixed $b = 1.016\,mm$, $a = 7.47\,mm$, $s = 6\,mm$ and $d = 0.5b$

It has been shown from the graphs of the two topologies discussed above that a ridge-like folded waveguide can achieve lower cutoff frequencies than a conventional ridge waveguide for the same outer dimensions of waveguide. This has the advantage of realising smaller sized resonators and filters with the former topology that resonate at lower microwave frequencies.

The graphs also offer a guideline to dimensional changes that will aid in extending the stopband.

In figure 4.13, it has been shown that as s increases, the difference in the cutoff frequency for both topologies decreases.

In design, the option to vary certain dimensions of a structure can at times be limited due to certain factors such as tight fabrication-related dimensional tolerance for certain design features. In the case of multilayered structures, the thickness of available layers can also affect aspects of the design.

It is preferable to have more than one possible way of decreasing the cutoff frequency in a single topology. Once other options have been exploited, increasing the dimension s can lower the cutoff frequency of the fundamental mode even further. The only limitation then is that with an increase

beyond the aspect ratio $s/a \approx 0.45\,mm\,to\,0.5\,mm$, the cutoff frequency of the second resonant mode increases its rate of decrease. This is because the overlap between the top of the perturbing block and the top wall of the waveguide increasingly overlaps with the electric field of the higher order mode.

In the next section, a new shape of the perturbing structure is proposed with the aim of reducing the effects of the overlap of the capacitive plates with the first two higher order modes. The aim of the new topology is to lower the resonant frequency of the fundamental mode as much as possible without decreasing that of the first spurious resonance significantly. It also aims to increase the width of the stopband beyond that achievable by the square/rectangular ridge-like waveguide that has been discussed in this section.

4.4 Cross-Shape Ridgelike FSIW Resonator

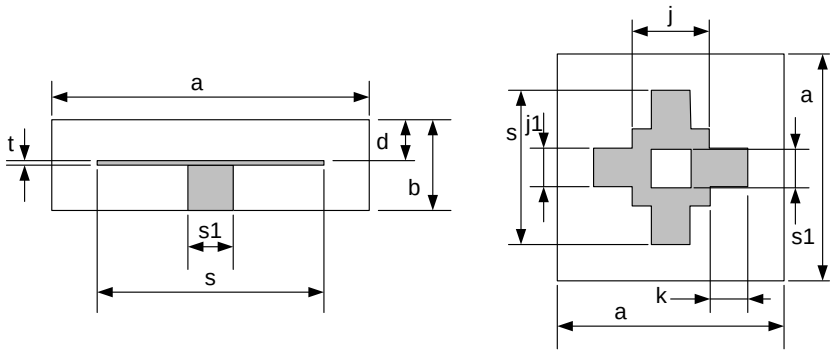
In this section a new topology of resonator is proposed. This is shown in figure 4.15 for both a case where a horizontal conducting plate is supported by a vertical rectangular/square post and for the equivalent structure where the walls about the solid post are replaced by vias.

The side views for this topology are identical to those of the structure in figure 4.8.

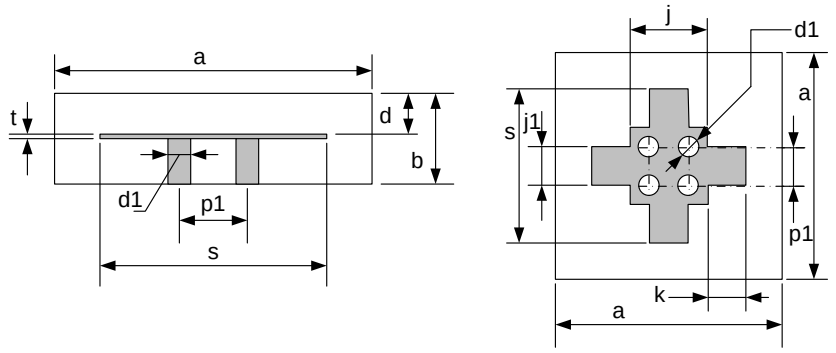
The cutoff frequency if calculated from the cross-section of both the structures in figures 4.8 and 4.15 at the center of the cavities, i.e. where the electric field is strongest. This would be the same if the widths of the horizontal plates across this point are identical. To differentiate between the two, in this section the former will be referred to as the rectangular plate cavity whereas the latter will be named the cross-shaped plate cavity.

The motivation for the shape difference of the perturbation in the resonator in figure 4.15 relative to that in figure 4.8 is to show that the lowest achievable resonant frequency for a resonator can be improved by adjusting the shape of the perturbation within the resonator; the best shape is chosen relative to the distribution of the electromagnetic fields within the resonator.

The cross-shaped plate aims to avoid a capacitive plate overlap in the areas circled in brown in figure 4.16, hence the cross-like shape.



(a) Solid Post - Side View (b) Solid Post - Top View



(c) Via Walls - Side View (d) Via Walls - Top View

Figure 4.15: Proposed Cross-Shaped Resonator

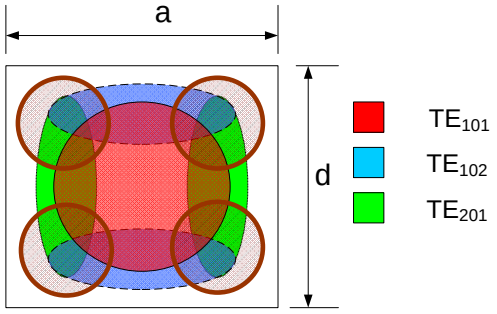


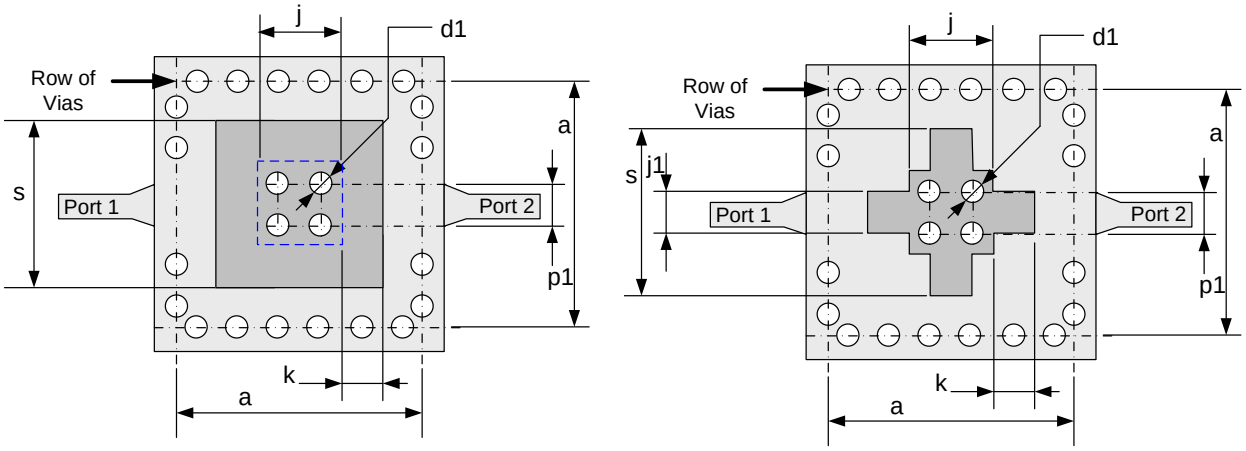
Figure 4.16: Overlap Areas to be Avoided

The performance of the two will be compared in terms of the resonant frequency and the unloaded quality factor attainable by each cavity. The results of this analysis are presented in the subsections that follow.

4.4.1 Structure of SIW Resonators

To compare the resonant frequencies of the first two modes of the two topologies when implemented in SIW, energy is coupled into the cavities using a microstrip line connected to the top wall of the waveguide. The walls of the cavity are formed by a row of vias as shown in figure 4.17.

The full-wave electromagnetic simulations focus on effects of variations in the dimension k on the resonant frequencies as well as the unloaded quality factor. In figure 4.17a, the blue dashed line represents a virtual square of width, j, similar to that in figure 4.17b. This acts as a baseline from which the dimension k in figure 4.17a can be measured to match the k in figure 4.17b.



(a) Rectangular Plate Resonator

(b) Cross-shaped Plate Resonator

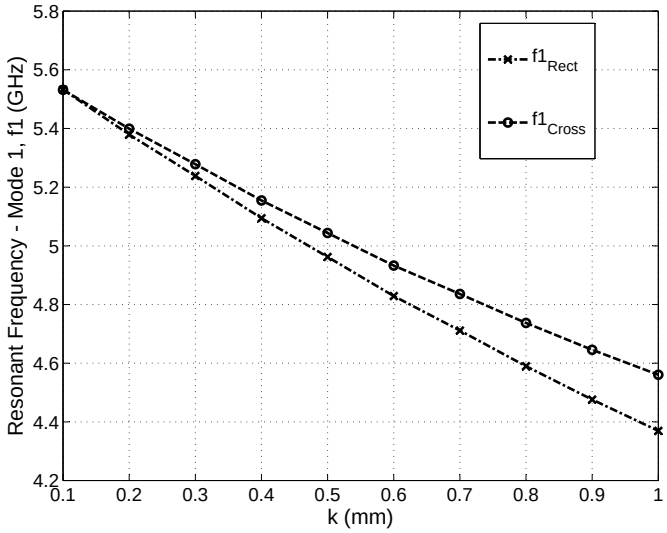
Figure 4.17: Ridge-like SIW Resonator Topologies

4.4.2 Effect of Dimensional Variations on the Resonant Frequency

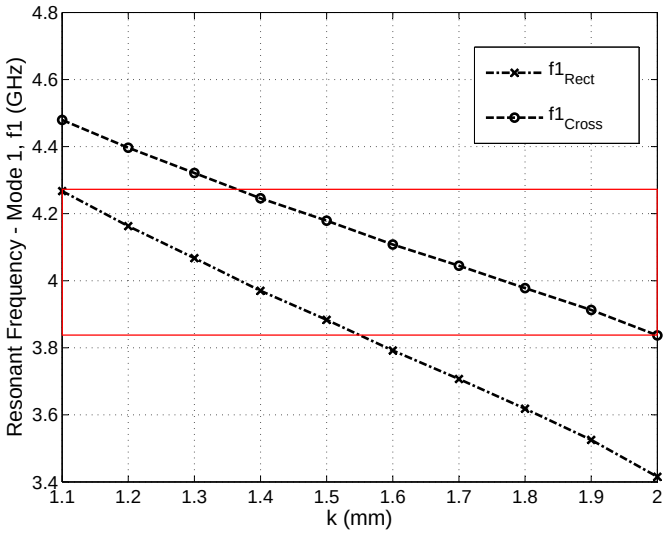
4.4.2.1 Resonant Frequency of Mode 1 Versus Dimension k

For a fixed $a = 10.7$ mm, and a relative dielectric constant of $\varepsilon_r = 3.38$, the resonant frequency of the first mode is simulated for both resonators against two ranges of the dimension k: $0.1\,mm \leq k \leq 1\,mm$ and $1.1\,mm \leq k \leq 2\,mm$. Two graphs are used for clearer observation of the results in the plots.

In this section, the subscripts *Rect* and *Cross* will be used to represent the rectangular plate resonator and the cross-shaped plate resonator respectively.



(a) $0.1\,mm \leq k \leq 1\,mm$

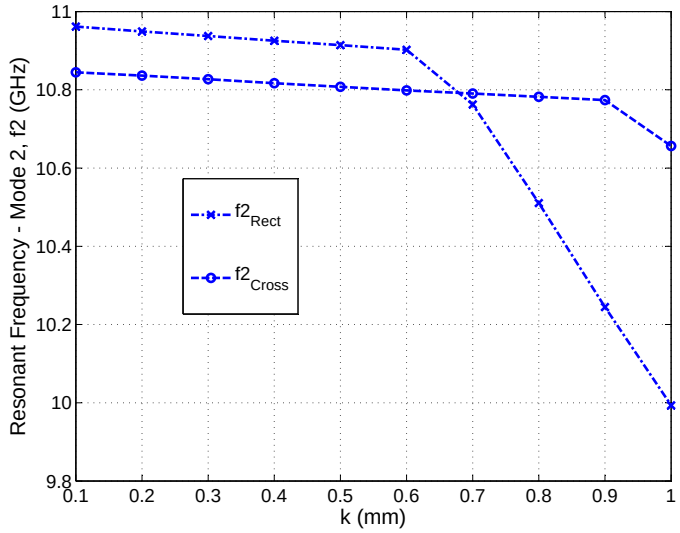


(b) $1.1\,mm \leq k \leq 2\,mm$

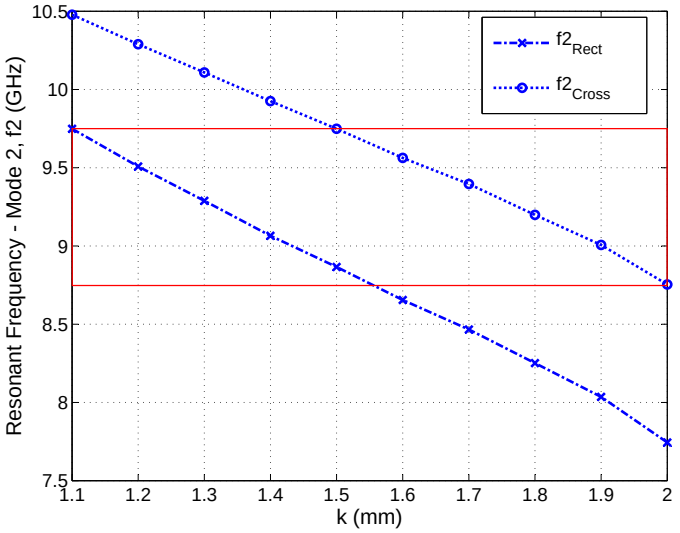
Figure 4.18: Resonant Frequency of Mode 1 against Dimension k

It is shown that for smaller values of k, the resonant frequency of the fundamental mode for resonators converges to a uniform value. However, as the dimension k increases, a divergence can be observed obtaining a difference of about 420 MHz in the resonant frequencies for a value of $k = 2\,mm$. The rectangular plate resonator achieves a lower resonant frequency over the entire range of k. This is because the cross-shaped plate resonator reduces the effective overlap area between the plate and top wall of the waveguide.The red rectangle covers an area within which values of k can be chosen for either resonator to have the same resonant frequency for both resonators. This can enable the comparison of the stopband width gauging from how far placed the second resonant frequency for either resonator is from a common fundamental resonant frequency.

4.4.2.2 Resonant Frequency of Mode 2 Versus Dimension k



(a) $0.1\,mm \leq k \leq 1\,mm$



(b) $1.1\,mm \leq k \leq 2\,mm$

Figure 4.19: Resonant Frequency of Mode 2 against Dimension k

For lower values of k, up to about $k = 0.7$mm, the rectangular plate resonator is found to have a higher resonant frequency than the cross-shaped plate resonator.

However, as the dimension k increases, the difference in the resonant frequency of the second resonant mode of the two resonators starts to increase with the cross-shaped plate resonator having a higher resonant frequency. At $k = 2\,mm$, a difference of approximately 1 GHz is obtained.

4.4.2.3 Comparing the Width of the Stopband for a Common Fundamental Mode Resonance

As has been mentioned above, the red rectangles indicated values of resonant frequency for which individual values of k can be chosen to get a common resonant frequency.

For a fundamental resonance of 4.0 GHz and 4.6 GHz, the values of k are chosen as $k_{Rect} = 1.369\,mm$, $k_{Cross} = 1.767\,mm$ and $k_{Rect} = 0.792\,mm$, $k_{Cross} = 0.954\,mm$ respectively.

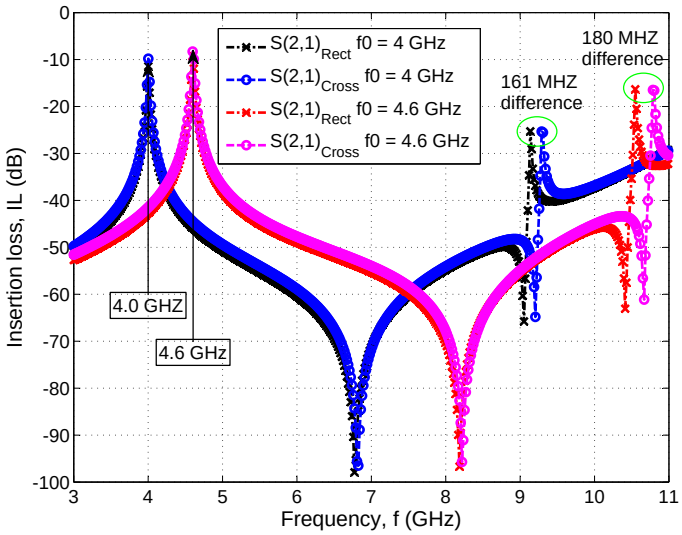
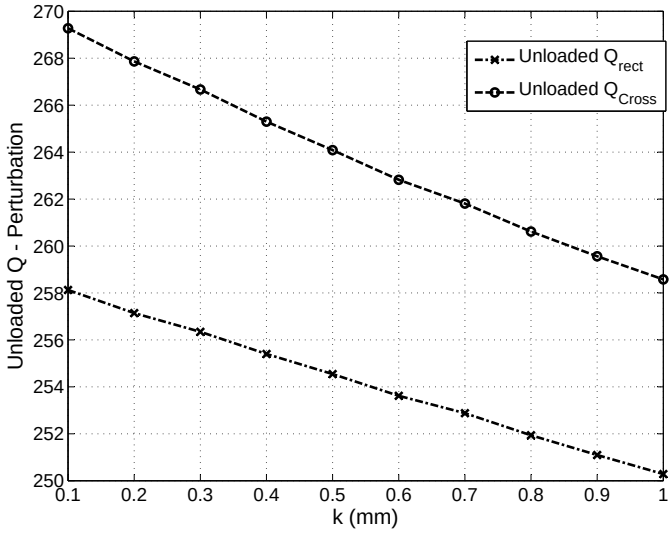


Figure 4.20: Insertion Loss of a Rectangular Plate Resonator and a Cross-Shaped Plate Resonator with a fundamental resonance at 4 GHz and 4.6 GHz

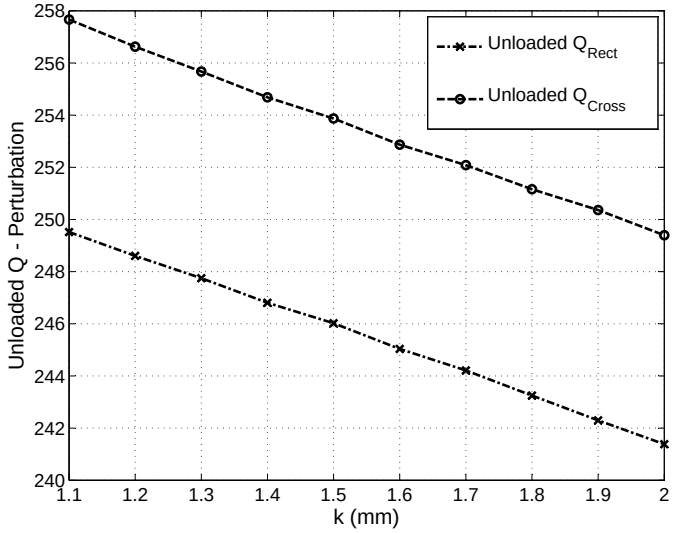
The difference between the resonant frequencies of the first spurious response increases for higher first mode resonant frequencies. The stopband for the cross-shaped plate resonator is 161 MHz wider than that for the rectangular plate resonator for a fundamental mode resonance at 4 GHz, and it is 180 MHz wider when the fundamental mode resonates at 4.6 GHz.

4.4.2.4 Unloaded Quality Factor Versus Dimension k

Due to the effective volume of the perturbing structure of the post and conducting plate of the cross-shaped plate resonator being less than that of the rectangular shaped resonator for the same values of k, the unloaded quality factor of the former resonator is found to be higher throughout the full range of k up to $k = 2\,mm$. The difference is, however, very small and is not a significant factor.



(a) $0.1\,mm \leq k \leq 1\,mm$



(b) $1.1\,mm \leq k \leq 2\,mm$

Figure 4.21: Unloaded Quality Factor Versus Dimension k

4.5 Filter Design Using Proposed Resonator

In this section, two filters are designed using the proposed cross-shaped plate resonator: a second order filter and a fourth order filter. The design process starts with the design of a single resonator and comparing the group delay of S_{11} of a circuit model with that of a three dimensional implementation. The input/output coupling is chosen to achieve the needed external quality factor.

Two resonators are then coupled to each other using magnetic coupling. The required coupling coefficient is established from the circuit model and is compared to that of the full-wave simulation until a reasonable match is established.

The extraction of the quality factor and the couplings within a filter are discussed briefly in this

section as the designs are progressively developed.

The physical filters are implemented on a multilayered structure using two 0.508 mm core layers of Rogers 4003 substrate with a relative permittivity of 3.38. In between the two is a bonding ply of 0.038 mm Rogers 3001.

4.5.1 Extracting the External Quality Factor, Q_e

The external quality factor of a resonator can be extracted using two different setups: as a singly loaded resonator or as a doubly loaded resonator.

4.5.1.1 Singly Loaded Resonator

Figure 4.22a shows a physical model of a substrate integrated waveguide resonator using the proposed cross-shaped plate perturbation. The input coupling structure comprises a short-circuited via/post transitioning to a 50 Ω coplanar waveguide feed-line. This coupling technique is chosen because it can provide enough coupling to realise the required external quality factor for the filter circuits in following sections. It provides magnetic input coupling and varies the value of the external quality factor depending on the position of the post relative to the strength of the magnetic field at the position of the post.

A singly loaded resonator can be represented using the equivalent circuit shown in figure 4.22b where G is an external conductance attached to a lossless LC resonator.

The input admittance of the resonator is computed as

$$Y_{in} = j\omega C + \frac{1}{j\omega L} = j\omega_0 C\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right) \tag{4.23}$$

where $\omega_0 = \frac{1}{\sqrt{LC}}$ is the resonant frequency.

Equation 4.23 can be simplified using the approximation $\frac{\omega^2-\omega_0^2}{\omega} \approx 2\triangle\omega$ to get [54]

$$Y_{in} = j\omega_0 C \cdot \frac{2\triangle\omega}{\omega_0} \tag{4.24}$$

The reflection coefficient S_{11} at the input of the circuit is defined as

$$S_{11} = \frac{G - Y_{in}}{G + Y_{in}} = \frac{1 - {}^{Y_{in}}/_{G}}{1 + {}^{Y_{in}}/_{G}} \tag{4.25}$$

If the external quality factor, Q_e, is defined as

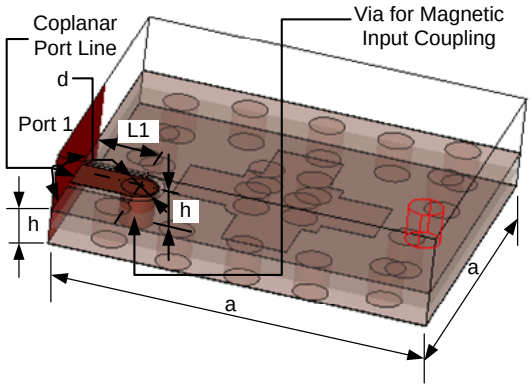
$$Q_e = \frac{\omega_0 C}{G} \tag{4.26}$$

then S_{11} can be rewritten as

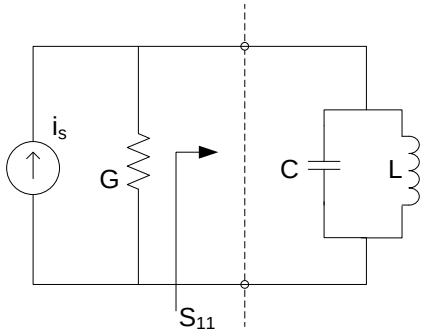
$$S_{11} = \frac{1 - jQ_e \cdot ({}^{2\triangle\omega}/_{\omega_0})}{1 + jQ_e \cdot ({}^{2\triangle\omega}/_{\omega_0})} \tag{4.27}$$

For a lossless resonator, the magnitude of S_{11} is equal to 1, but the phase response varies against frequency.

Figure 4.23 shows a plot of the phase of S_{11} as a function of frequency, $f = \frac{\omega}{2\pi}$, in GHz.



(a) Physical Model



(b) Equivalent Circuit

Figure 4.22: Singly Loaded Resonator

The absolute bandwidth between the $\pm 90^0$ points is defined as [54]

$$\triangle\omega_{\pm 90^0} = \triangle\omega_+ - \triangle\omega_- = \frac{\omega_0}{Q_e} \tag{4.28}$$

From this, the external quality factor can be extracted to get

$$Q_e = \frac{\omega_0}{\triangle\omega_{\pm 90^0}} \tag{4.29}$$

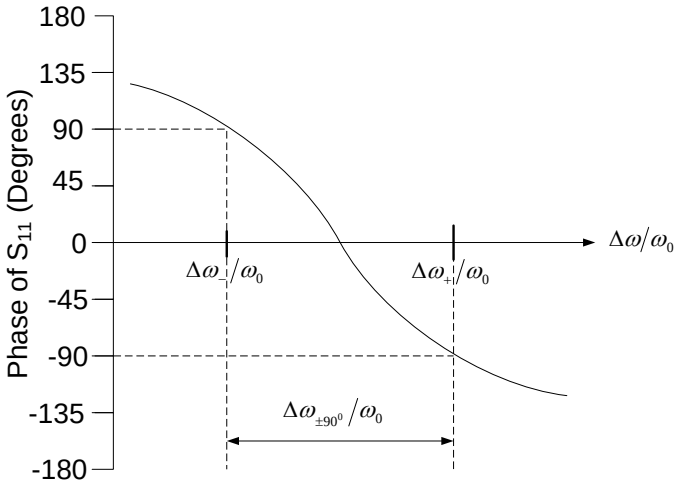


Figure 4.23: Phase of S_{11}

The external quality factor can also be defined in terms of the group delay of S_{11} at resonance, $\tau_{S_{11}}(\omega_0)$, as [54]

$$Q_e = \frac{\omega_0 \cdot \tau_{S_{11}}(\omega_0)}{4} \tag{4.30}$$

4.5.1.2 Doubly Loaded Resonator

When a resonator is symmetric about the center, another symmetrical feed-line can be added to the structure in figure 4.22 to form a two port network.

The circuit equivalent can be represented as shown in figure 4.24 with the LC resonator separated into two parallel LC combinations divided by a symmetry plane T-T'.

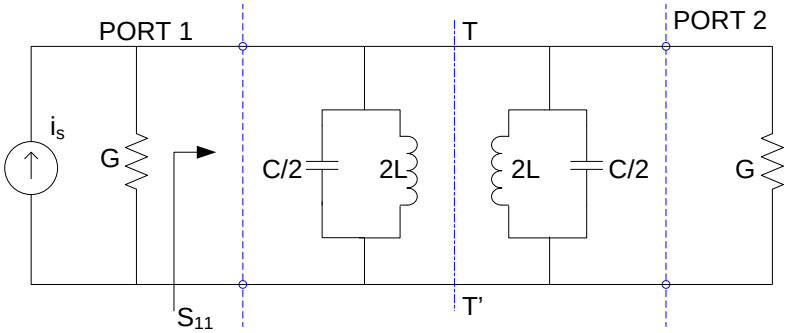


Figure 4.24: Equivalent Circuit for a Doubly Loaded Resonator

The odd-mode input admittance, Y_{ino}, and the input reflection coefficient, S_{11o}, of the network are attained by replacing the T-T' plane with a short circuit and are given by

$$Y_{ino} = \infty \tag{4.31}$$

$$S_{11o} = \frac{G - Y_{ino}}{G + Y_{ino}} = -1 \tag{4.32}$$

for a lossless resonator.

The corresponding parameters for the even-mode are obtained by replacing the T-T' plane with an open circuit to get

$$Y_{ine}\left(\omega_0 + \triangle\omega\right) = j\omega_0 C^{\triangle\omega/\omega_0} \tag{4.33}$$

$$S_{11e} = \frac{G - Y_{ine}}{G + Y_{ine}} = \frac{1 - jQ_e{}^{\triangle\omega/\omega_0}}{1 + jQ_e{}^{\triangle\omega/\omega_0}} \tag{4.34}$$

where $\omega_0 = 1/\sqrt{LC}$ and the approximation $\frac{\omega^2 - \omega_0^2}{\omega} \approx 2\triangle\omega$ is assumed with $\omega = \omega_0 + \triangle\omega$.

The transmission coefficient can be expressed in terms of the odd-mode and even-mode reflection coefficients, S_{11o} and S_{11e}, respectively as [54]

$$S_{21} = \frac{1}{2}\left(S_{11e} - S_{11o}\right) = \frac{1}{1 + jQ_e{}^{\triangle\omega/\omega_0}} \tag{4.35}$$

The magnitude of S_{21} is then

$$|S_{21}| = \frac{1}{\sqrt{1 + \left(Q_e{}^{\triangle\omega/\omega_0}\right)^2}} \tag{4.36}$$

At resonance, the magnitude of S_{21} is at its maximum which equals 1 for a lossless resonator.

The magnitude of S_{21} falls to its -3 dB value when

$$Q_e \frac{\triangle\omega_{\pm}}{\omega_0} = \pm 1 \tag{4.37}$$

The 3 dB bandwidth (see figure 4.25) can then be defined as [54]

$$\triangle\omega_{3dB} = \triangle\omega_+ - \triangle\omega_- = \frac{\omega_0}{Q_e} - \left(-\frac{\omega_0}{Q_e}\right) = \frac{2\omega_0}{Q_e} \tag{4.38}$$

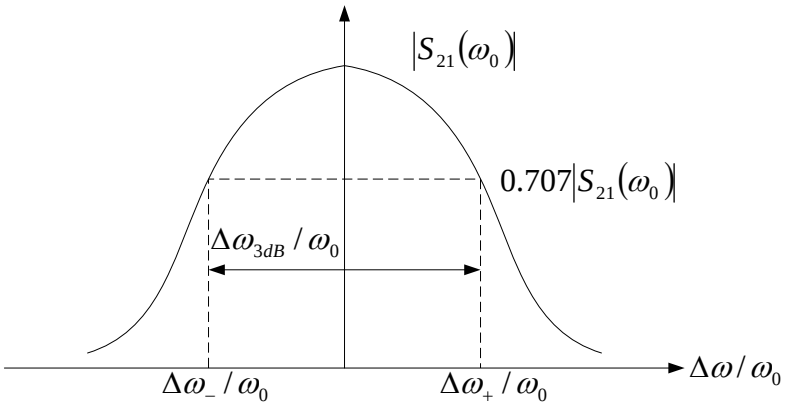


Figure 4.25: Insertion Loss of a Doubly Loaded Resonator

The external quality factor of a doubly loaded resonator can also be defined as being half the external quality of a singly loaded resonator, i.e.

$$Q_{e_{double}} = \frac{Q_{e_{single}}}{2} \tag{4.39}$$

4.5.1.3 Group Delay Simulation Results

A singly loaded resonator is simulated in the circuit simulator and the corresponding three dimensional implementation shown in figure 4.22a is analysed in a full-wave electromagnetic simulation tool. The group delay responses of both are compared in figure 4.26.

The two results match well with a resonant frequency of the resonator of 8.852 GHz. At this frequency, the group delay of S_{11} is 3.21 ns corresponding to an external quality factor of 44.6. The unloaded quality factor of the resonator obtained from the full-wave simulation is 288.2.

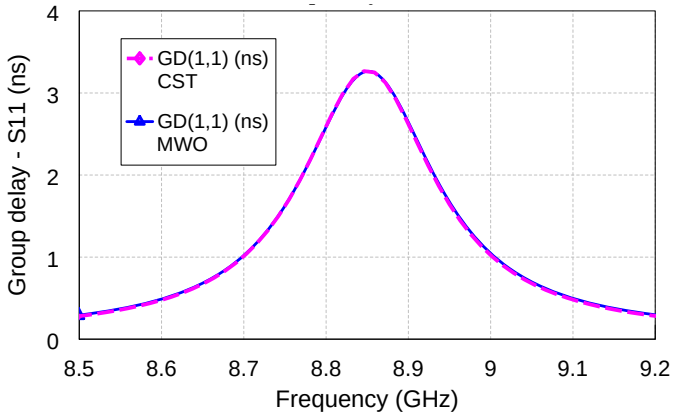


Figure 4.26: Group Delay of S_{11}- Full-wave Simulation (CST) Vs Circuit Simulator (Microwave Office)

4.5.2 Inter-Resonator Coupling

The coupling coefficient of coupled resonators can be defined in terms of the ratio of coupled energy to stored energy as [54]

$$k = \frac{\int\int\int \varepsilon \underline{E}_1 \cdot \underline{E}_2 dv}{\sqrt{\int\int\int \varepsilon \left|\underline{E}_1\right|^2 dv \times \int\int\int \varepsilon \left|\underline{E}_2\right|^2 dv}} + \frac{\int\int\int \mu \underline{H}_1 \cdot \underline{H}_2 dv}{\sqrt{\int\int\int \mu \left|\underline{H}_1\right|^2 dv \times \int\int\int \mu \left|\underline{H}_2\right|^2 dv}} \tag{4.40}$$

where $\underline{E}$ and $\underline{H}$ represent the electric and magnetic field vectors respectively.

The first term on the right hand side of the equation represents the electric coupling while the second term is the magnetic coupling component.

Mathematically, energy transfer between resonators is described using a dot operation of the space vector fields. This results in the coupling value having either a positive or negative sign. A positive sign implies that the coupling enhances the stored energy of the uncoupled resonator whereas a negative sign indicates a reduction in the stored energy[54].

Direct evaluation of the coupling coefficient from equation 4.40 requires knowledge of the field distributions as well as the performance of the space integrals [54]. Unless analytical solutions for these exist, analysis using that formula is not an easy task.

Full-wave electromagnetic simulations can be performed on three dimensional coupled structures to obtain characteristic frequencies that can be used to easier define and compute the coupling coefficient between two coupled resonators. For synchronously tuned RF/microwave resonators, the electric coupling coefficient is given by [54]

$$k_E = \frac{f_m^2 - f_e^2}{f_m^2 + f_e^2} = \frac{C_m}{C} \tag{4.41}$$

where $f_m = \frac{1}{2\pi\sqrt{L(C-C_m)}}$ and $f_e = \frac{1}{2\pi\sqrt{L(C+C_m)}}$. C and L are the self-capacitance and self-inductance of a resonator respectively, where as C_m is the mutual capacitance between two coupled resonators. These are shown in figure 4.27 which represents a simplified electric coupled resonator circuit.

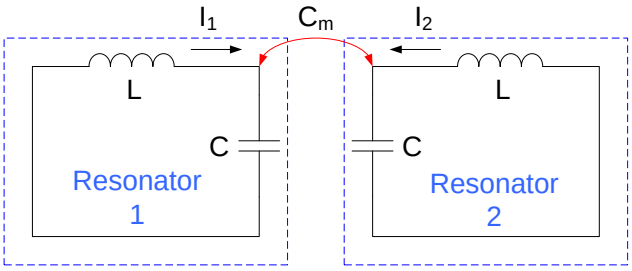


Figure 4.27: Coupled Resonator Circuit with Electric Coupling

The magnetic coupling coefficient on the other hand is given by

$$k_M = \frac{f_e^2 - f_m^2}{f_e^2 + f_m^2} = \frac{L_m}{L} \tag{4.42}$$

where $f_e = \frac{1}{2\pi\sqrt{C(L-L_m)}}$ and $f_m = \frac{1}{2\pi\sqrt{C(L+L_m)}}$. C and L are the self-capacitance and self-inductance of a resonator respectively, where as L_m is the mutual inductance between two coupled resonators. These are shown in figure 4.28 which represents a simplified magnetic coupled resonator circuit.

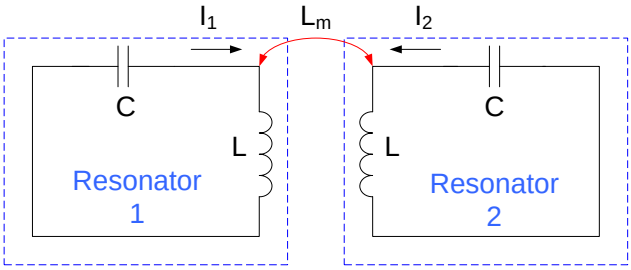


Figure 4.28: Coupled Resonator Circuit with Magnetic Coupling

The universal formula for extracting the coupling coefficient of two synchronously tuned resonators is

$$k = \pm\frac{f_{p2}^2 - f_{p1}^2}{f_{p2}^2 + f_{p1}^2} \tag{4.43}$$

where f_{p1} and f_{p2} are characteristic frequencies that correspond to either f_e or f_m in equations 4.41 and 4.42.

4.5.3 Proposed Second Order X-Band Filter

In this section, a second order filter is designed by magnetically coupling two of the resonators shown in figure 4.22a. The three dimensional implementation is shown in figure 4.29a along with the circuit equivalent in figure 4.29b.

The circuit equivalent uses quarter wavelength lines to represent the coupling elements; J inverters could be use in their place and would attain the same results.

The filter is designed for a fractional bandwidth of 4.8 % and a center frequency of 8.85 GHz. The other parameters are calculated from normalised 3 dB k and q values obtained from tables in [96] for a Chebychev filter with a maximum passband ripple of 0.01 dB.

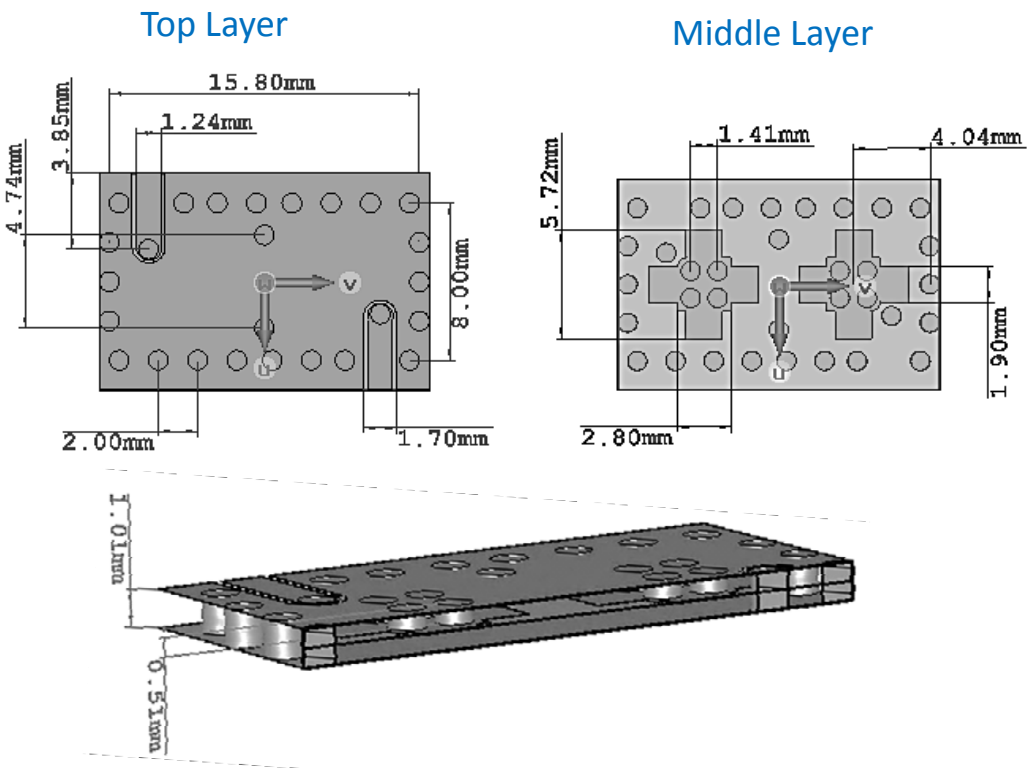
For a second order filter the k and q values are:

q_1	1.483
q_2	1.483
k	0.7075

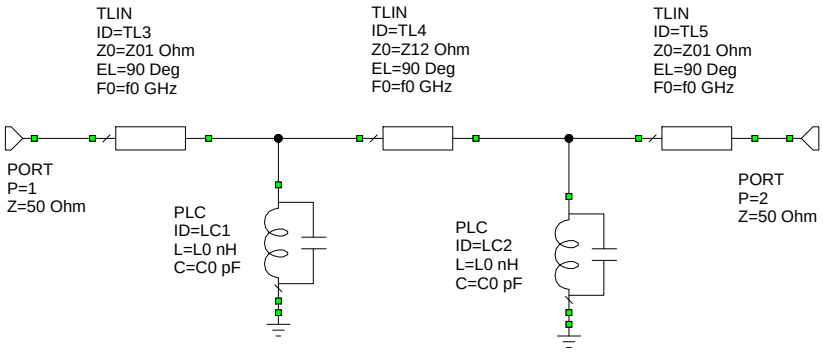
The denormalised external quality factor is then

$$Q_e = \frac{q_1}{fBw} = \frac{q_2}{fBw} = 30.7$$

where fBw is the fractional bandwidth.



(a) Three Dimensional Implementation



(b) Circuit Equivalent

Figure 4.29: Second Order Filter

The denormalised coupling coefficient, M_{12} is calculated as

$$M_{12} = k_{12} \times fBw = 0.0342$$

The line impedances in figure 4.29 (b) are computed as follows [54]

$$Z12 = \frac{Z01}{Q_e \times M_{12}} \tag{4.44}$$

where $Z01 = Z$ is the port impedance.

The LC components of the parallel resonators, $L0$ and $C0$ are calculated as [54]

$$L0 = \frac{Z}{Q_e \times \omega_0} \tag{4.45}$$

$$C0 = \frac{Q_e}{Z \times \omega_0} \tag{4.46}$$

where ω_0 is the angular resonant frequency.

In the three dimensional structure, coupling is achieved by varying the width of the window between the two resonators to vary the magnetic coupling. The coupling coefficient is computed using equation 4.43 with the characteristic frequencies being computed using the eigenmode solver in CST.

The group delay method is used to compare the circuit model to the three dimensional model at different stages of design to try and obtain a good match between the two. The group delay of S_{11} is obtained when the circuit is singly loaded and is shorted at the output port.

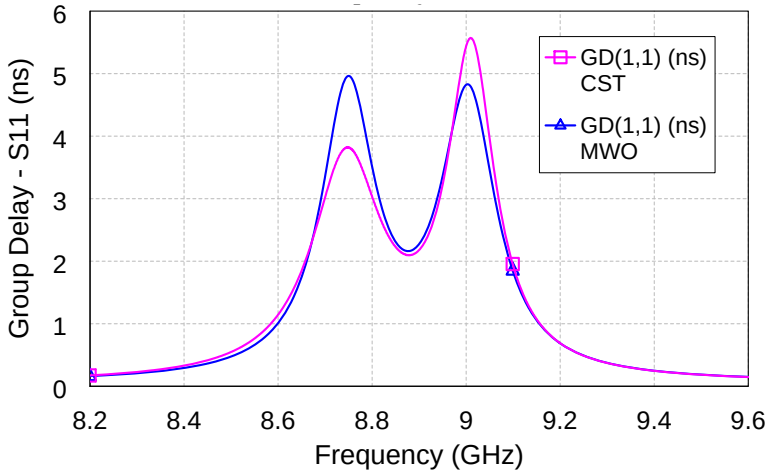


Figure 4.30: Group Delay of S_{11} with port 2 shorted - Second Order Filter

The S-parameter results of the circuit simulation and the full-wave electromagnetic simulation are compared in figure 4.31

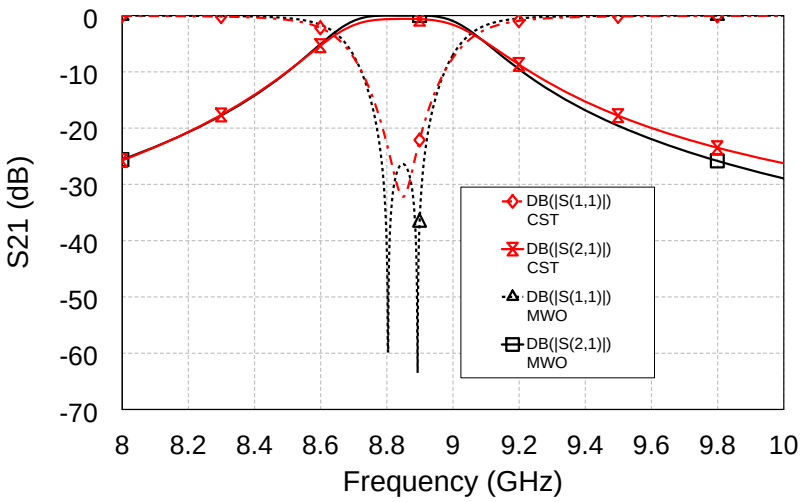


Figure 4.31: S-Parameter Results of Simulated Second Order Filter

The curve shows that the results compare well. The dimensions of the three dimensional implementation for this comparison are used as the final dimensions for fabrication which is discussed in a later section. All vias have a diameter of 1 mm. The simulated unloaded quality factor for the resonators is 274.

4.5.4 Proposed Fourth Order X-Band Filter

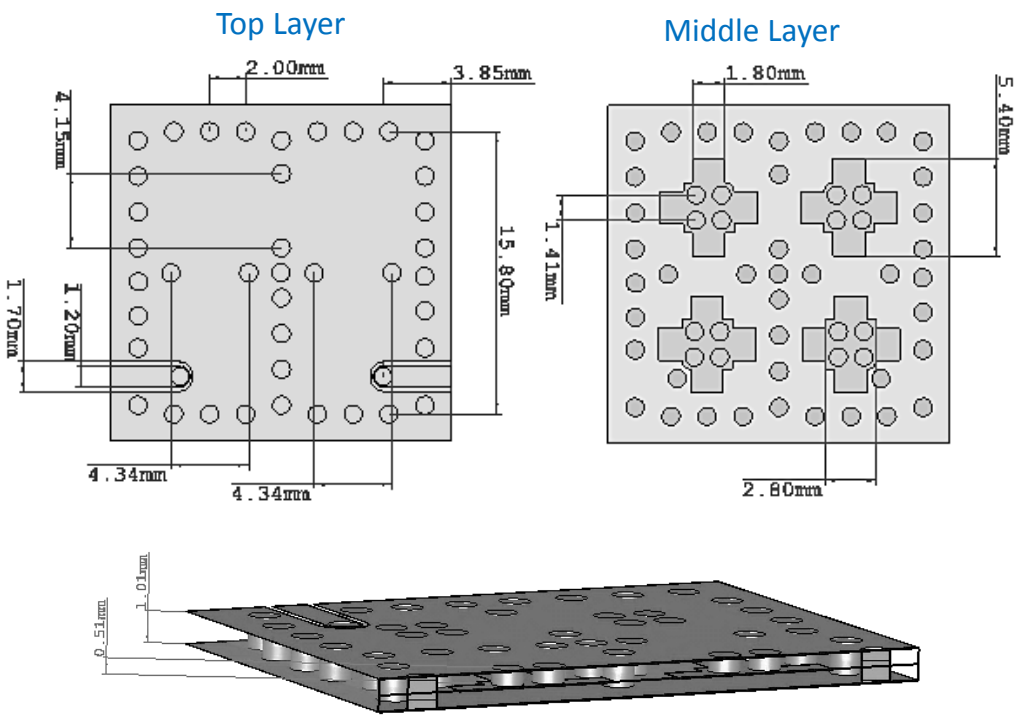
In this section, a fourth order filter is designed for a slightly higher frequency of 9.1 GHz and a fractional bandwidth of 4 percent. Similar to the previous section, normalised 3 dB k and q obtained from [96] for a 0.01 dB Chebychev ripple are used for the circuit design. For a fourth order filter these are:

q_1	1.0460
q_2	1.0460
k_{12}	0.7369
k_{23}	0.5413
k_{34}	0.7369

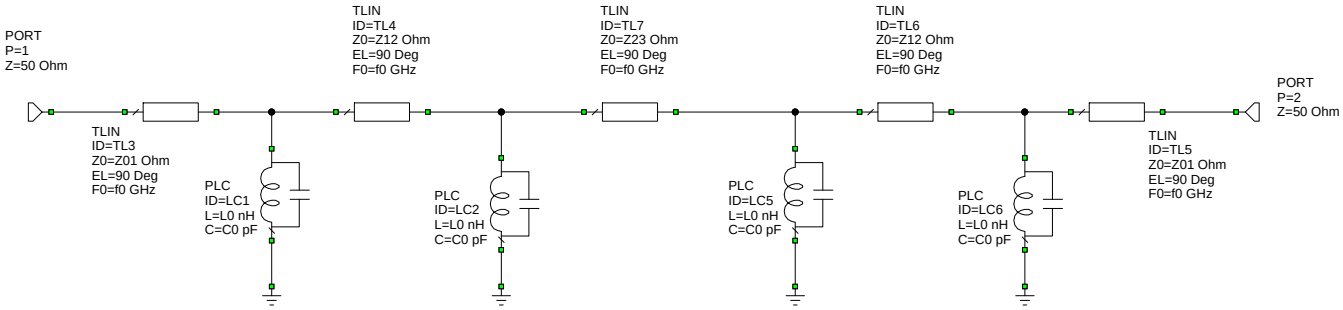
The denormalised equivalents, calculated in a similar manner to calculations in subsection 4.5.3 are:

Q_{e1}	25.512
Q_{e2}	25.512
M_{12}	0.0302
M_{23}	0.0222
M_{34}	0.0302

The three dimensional implementation as well as the circuit equivalent are shown in figure 4.32. The line impedances for the inter-resonator coupling elements are computed as [54]



(a) Three Dimensional Implementation



(b) Circuit Equivalent

Figure 4.32: Fourth Order Filter

$$Z12 = \frac{Z01}{Q_e \times M_{12}} \tag{4.47}$$

$$Z23 = \frac{Z01}{Q_e \times M_{34}} \tag{4.48}$$

$$Z34 = \frac{Z01}{Q_e \times M_{34}} \tag{4.49}$$

where Z is the port impedance and $Q_e = Q_{e1} = Q_{e2}$. The LC parallel resonator elements are calculated using equations 4.45 and 4.46.

The results of the circuit equivalent and those of the full-wave electromagnetic simulation of the three dimensional equivalent are presented below.

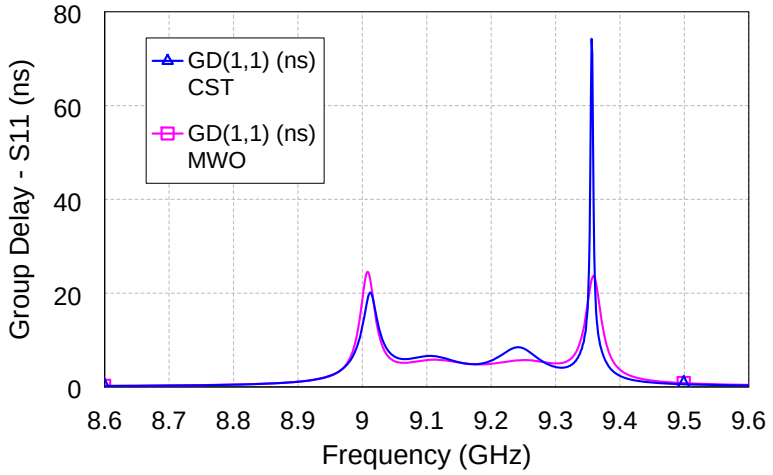


Figure 4.33: Group delay of S_{11} with port 2 shorted - fourth Order Filter

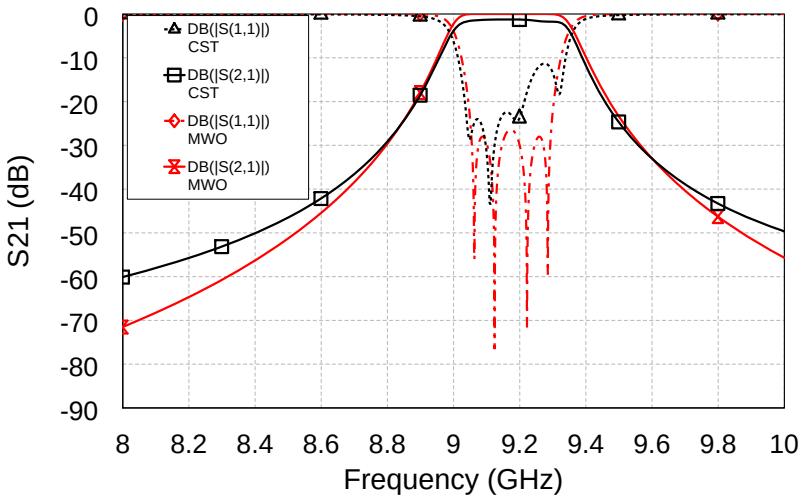


Figure 4.34: S-Parameter Results of Simulated Fourth Order Filter

These are seen to also compare well and the final dimensions shown in figure 4.32 (a) are chosen as the final dimensions for the filter fabrication. The vias all have the same diameter of 1 mm. the simulated Q factor of the filter is 281.

4.6 Fabrication of the Proposed Filters

The filters in the preceding sections are fabricated in PCB multilayered technology and the same considerations that were discussed in the previous chapter apply.

Figure 4.35 is a diagrammatic description of the different layers of the fourth order filter aiming to outline different fabrication steps. Since the number of layers of this filter are identical to those of the second order filter and the conducting layers are also the same, all discussion pertaining to fabrication apply to both filters.

Four layers labelled 0, 1, 2 and 3 are shown. Layers 0, 1 and 3 are conductor layers and layer 2 has not metal components.

Two sheets of 0.508 mm thick Rogers 4003c substrate with double copper cladding are used. Layers 0 and 1 are formed on opposite surfaces of one of the sheets, where as layers 2 and 3 are formed on the other sheet.

The first step in the fabrication of the structures involves the etching of defined shapes on the metallised surfaces. The metal cladding on layer 2 is completely removed.

Thereafter, vias connecting metallised layers 0 and 1 are drilled and copper plated using electroplating.

The following step entails the stacking together and vertically aligning of the substrates with 38 um of RO3001 bonding ply in between sheets 1 and 2. The structure is then laminated. Through vias are then drilled or punched through the laminated structure and electroplated.

Relevant testing is then done to analyse the integrity of the fabricated product.

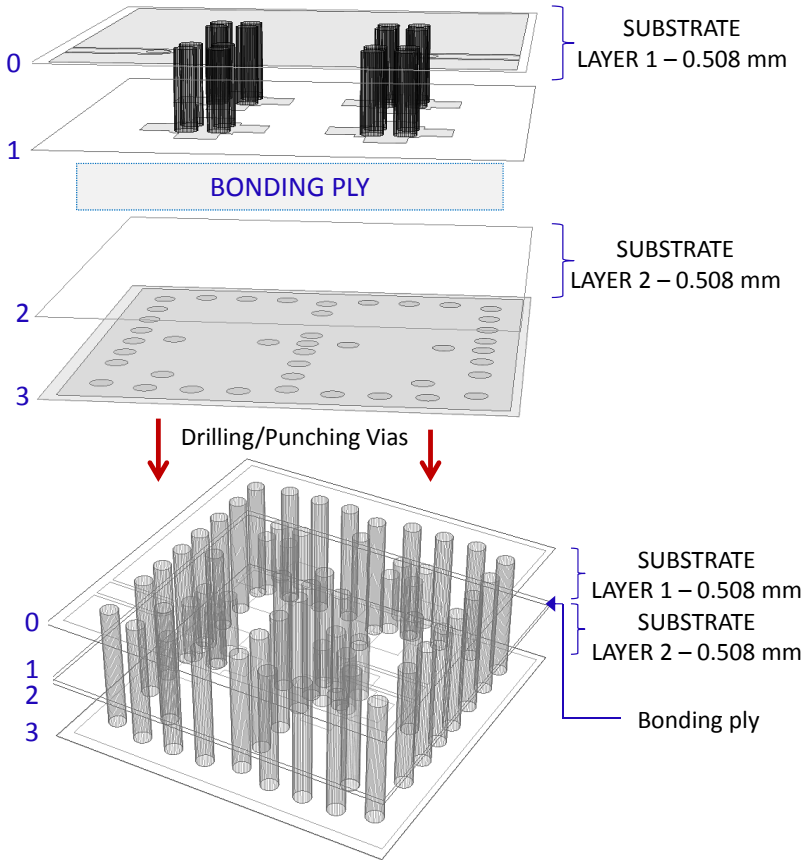
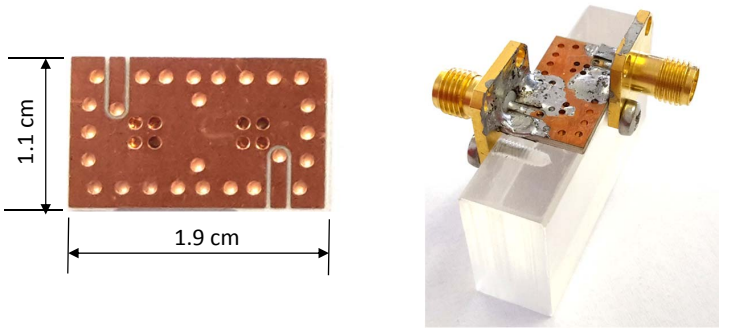


Figure 4.35: Reference figure for Fabrication instructions

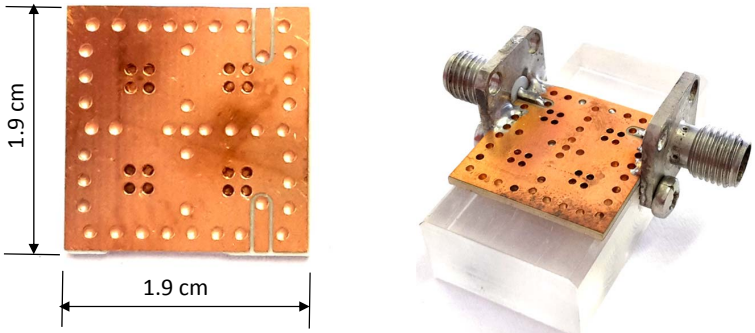
The fabricated filters are shown in figures 4.36 and 4.37. SMA connectors are attached to the co-planar waveguide feed-lines for measurements. The filters are both 1.00 mm thick so they are mounted on a plastic slab for support and to aid in proper attachment of the connectors. The dimensions of the second order and the fourth order filter are $1.1\,cm \times 1.9\,cm$ and $1.9\,cm \times 1.9\,cm$

respectively.



(a) Top view (b) Perspective View with SMA Connectors

Figure 4.36: Fabricated Second Order Filter



(a) Top view (b) Perspective View with SMA Connectors

Figure 4.37: Fabricated Fourth Order Filter

The measurement results for the two filters are presented in the next section.

4.7 Measurement Results

For the measurements, two square flange SMA connectors with a flat pin are edge connected to the feed-lines of the PCB filters for measurement purposes as was shown in figures 4.36 and 4.37.

An Agilent HP8510C Vector Network Analyser is used for the measurements with an ability to make broadband measurements in a range of 45 MHz up to 50 GHz in 2.4 mm coaxial cables. The measurement results are compared to the 3D simulated results in figures 4.38 and 4.39.

The results for the second order filter shows a resonant frequency shift of approximately 0.64 GHz from the simulated resonant frequency. The measured maximum insertion loss is 2.23 dB which is almost 2 dB higher than the simulated filter possibly due to dimensional inaccuracies in

the fabrication process, surface roughness and a mismatch at transition of SMA connector to the feed-lines. The second resonance is measured at a frequency of approximately 17 GHz which is over 7.5 GHz from the first resonant frequency. A stopband rejection of over 30 dB is obtained from a frequency of about 10.3 GHz to 15.5 GHz.

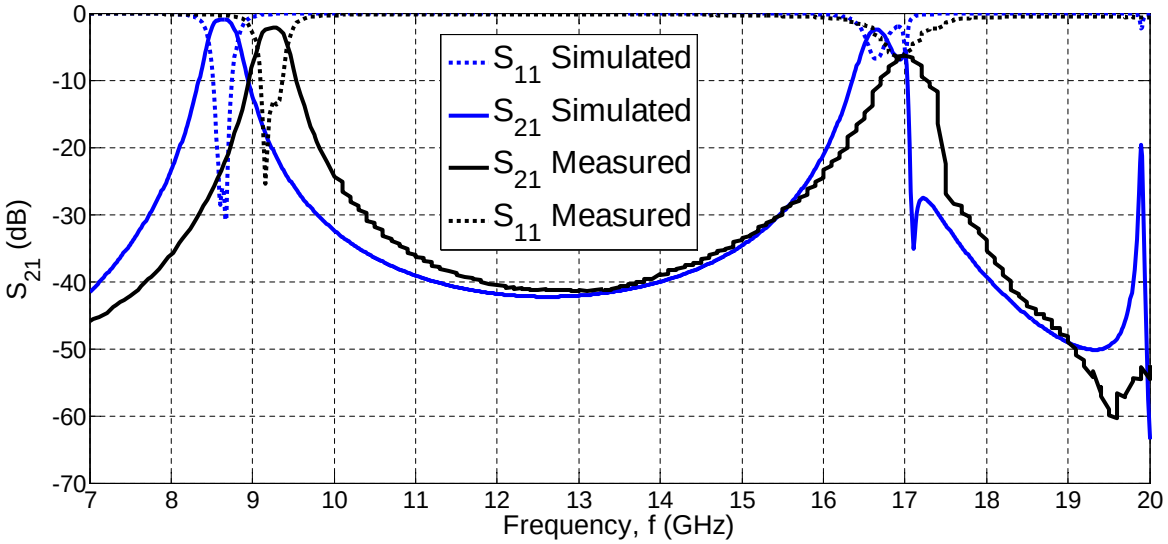


Figure 4.38: Broadband Measurement Results for the Second Order Filter

For the fourth order filter, a frequency shift of approximately 0.113 GHz of the fundamental mode resonance is measured from the simulated fundamental mode resonant frequency. For similar reasons to those that were mentioned for the possible increase in insertion loss of the second order filter, that of the fourth order filter also increases from a simulated maximum of approximately 2.3 dB to a measured maximum of 4.7 dB.

The measured frequency of the second resonant mode occurs at a frequency of over 8.5 GHz higher than that of the fundamental mode resonance with a good rejection in the stopband.

The measured 3 dB bandwidth reduces slightly from the simulated bandwidth of about 368 MHz to a measured bandwidth of 365 MHz.

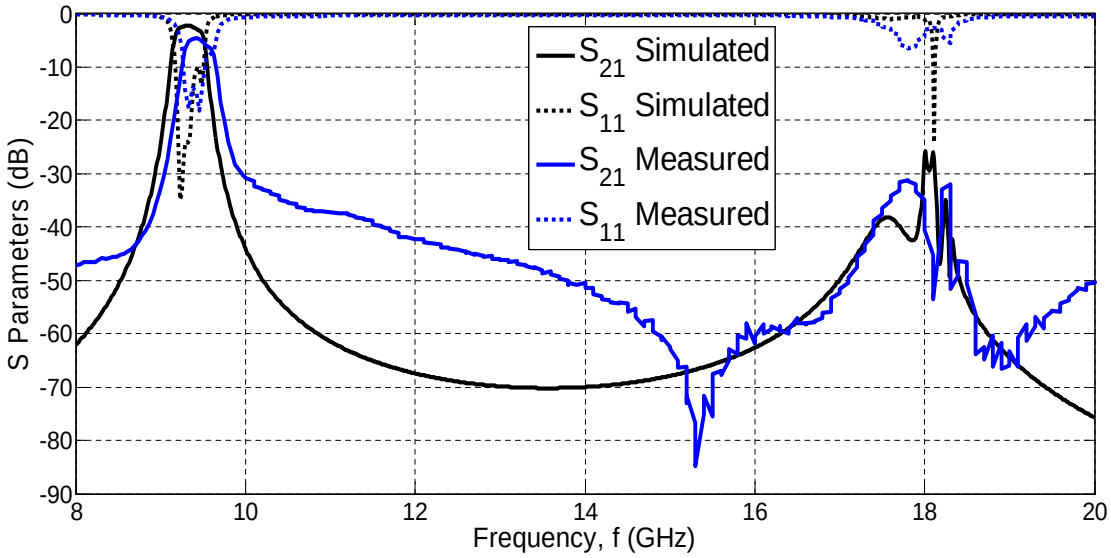


Figure 4.39: Broadband Measurement Results for the Fourth Order Filter

4.8 Conclusions

The aim of this chapter was to present a detailed study of an RSIW and to present an improved resonator structure which was denoted 'ridge-like' FSIW. The two are investigated in terms of cutoff frequency to establish that for similar waveguide outer dimensions, the latter topology can achieve lower cutoff frequencies. This means that devices designed using the latter resonator can operate at lower frequencies for the same dimensions as the former resonator.

A new resonator topology has also been proposed and presented. It has been shown to achieve a wide stopband, wider than that achievable by other resonators also discussed in the chapter. This resonator has been used for the design of two filters: a second order filter and a fourth order one. Simulation results from a circuit simulator have been compared to those of a full-wave electromagnetic simulation as part of the design process to model a three dimensional circuit to match the performance of a lumped element circuit equivalent.

The fabrication process in PCB multilayered technology has been briefly outlined and finally, the measurement results have been presented and compared to the simulated results from the full-wave electromagnetic simulation. Good results have been obtained confirming the simulated properties of the proposed resonator.

Chapter 5

LTCC Based Sequence Asymmetric Polyphase Filter

5.1 Introduction

In most RF transmitters and receivers, quadrature components of a local oscillator are used for vector modulation and demodulation and for image rejection. The accuracy of these components in terms of gain and phase is critical to the performance of these systems.

Modern transceiver systems have very tight constraints on the allocation on bandwidths. Image signals must therefore be suppressed to acceptable limits so that they don't cause interference within applicable frequency bands. Image rejection may be achieved either by filtering prior to down-conversion or by signal cancellation. It is difficult to build filters with sufficient selectivity and operation range at high frequencies prior to final downconversion [19]. It is therefore more practical to cancel the image by mixing quadrature phases of RF with the local oscillator (LO), or vice versa, and following this with a Hilbert filter at the intermediate frequency (IF) [19].

Downconversion is an essential operation in RF receivers and involves the translation of an incoming RF signal to a lower frequency, the intermediate frequency (IF) by mixing the amplified RF signal with the local oscillator (LO) signal. The frequency of resulting IF signal is given by

$$f_{IF} = |f_{RF} - f_{LO}| \tag{5.1}$$

After downconversion, the desired signal and an image lie at an equal frequency on either side of the RF frequency due to their conjugate complex representations. A Hilbert filter is suitable in such an instance for the rejection of the image signal. It responds to the complex representation of a signal as opposed to just the magnitude. A Hilbert filter response is shown in figure 5.1b. It is achieved by translating the poles of a high pass frequency response shown in figure 5.1a by applying a shift transform, $\omega \mapsto (\omega + \omega_0)$[19]. The resulting Hilbert filter frequency response is not mirrored about zero-frequency; the desired frequency may lie in the filter passband while the image frequency lies in its stopband. This filter can therefore be synthesized to null the image signal while

transmitting the desired signal.

A Hilbert filter circuit is realised through a connection of input signals in differential and quadrature form. This is connected to additional controlled sources through a network of resistors and capacitors. A four-phase Hilbert filter circuit is shown in figure 5.2b. The prototype high pass RC network from which it is transformed is shown in figure 5.2a.

The relation between the input and out voltages of the high pass RC network can be represented as

$$(V_{in} - V_0)\, j\omega RC = V_0 \tag{5.2}$$

The network realises a notch at DC. When the shift transform $\omega \mapsto (\omega + \omega_0)$ is applied to equation 5.2, we get

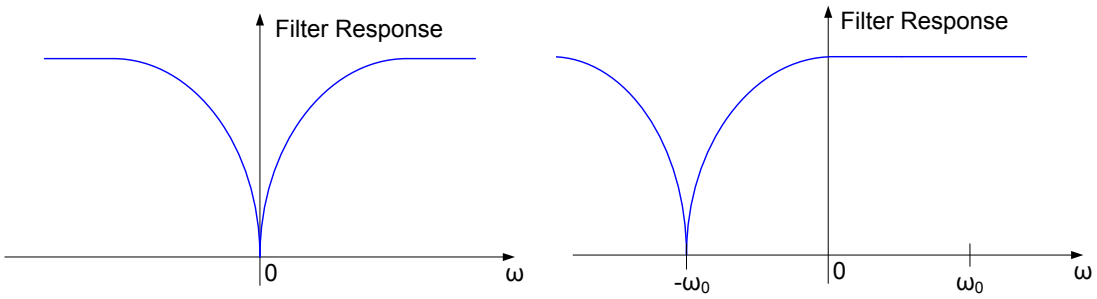


Figure 5.1: (a) High Pass Filter Response and (b) Hilbert Filter obtained by transforming the response in (a) on the frequency axis

$$(V_{in} - V_0)\, j\,(\omega + \omega_0)\, RC = V_0 \tag{5.3}$$

which realises a notch when $\omega + \omega_0 = 0$, i.e. when $\omega = -\omega_0$. Equation 5.3 can be rewritten as

$$j\,(V_{in} - V_0)\,\omega C = j\frac{(V_{in} - V_0)}{R}\omega_0 RC + \frac{V_0}{R} \tag{5.4}$$

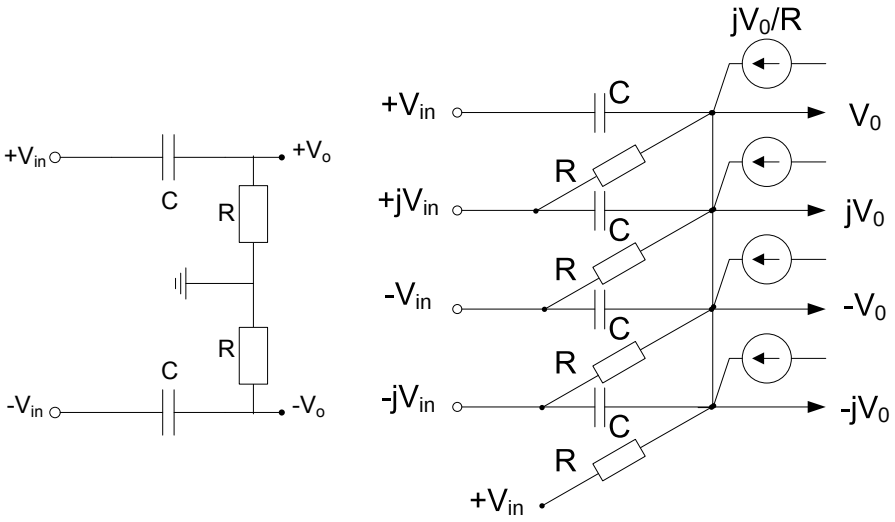
which simplifies to

$$j\,(V_{in} - V_0)\,\omega C = j\frac{(V_{in} - V_0)}{R} + \frac{V_0}{R} \tag{5.5}$$

when $\omega_0 RC = 1$. Equation 5.5 can now be rewritten as

$$j\,(V_{in} - V_0)\,\omega C = \frac{(V_0 - jV_{in})}{R} + j\frac{V_0}{R} \tag{5.6}$$

where the second term on the right hand side of the equation, $j\frac{V_0}{R}$, represents the additional controlled current sources in figure 5.2b.



(a) (b)

Figure 5.2: (a)High Pass Prototype Network (b)Four-phase Hilbert Filter Circuit

At the image frequency centre frequency, the voltage at the output of the filter is zero, i.e. $V_0 = 0$. Therefore, the four controlled sources carry zero current. Equation 5.6 then becomes

$$jV_{in}\omega C = -j\frac{V_{in}}{R} \tag{5.7}$$

so that

$$\omega C = -\frac{1}{R} \tag{5.8}$$

Therefore, $\omega RC = -1 = -\omega_0 RC$.

Therefore, the filter null is unaffected if these sources are deleted from the circuit [19]. After deleting these sources, the circuit that remains is the classic passive RC polyphase filter network which is discussed in the next section.

Ultimate image rejection within a Hilbert filter is limited by quadrature accuracy of the mixer input phases, gain matching of the mixers and the accuracy of the phase shifts within the filter. While only up to about 40 dB of repeatable image rejection can be achieved with this filter, a carefully designed polyphase filter can repeatedly reject the image by 60 dB [19] .

Polyphase filter networks were invented in 1971 by Gingell and were used to generate quadrature signals in audio applications. They were first implemented using discrete components [61].

These networks provide efficient solutions to two main problems in the design of RF integrated transceivers:

1. They generate highly matched wide-band quadrature signals which are not susceptible to components mismatch.

2. They suppress image signals without requiring highly selective RF filters and without utilising image-rejection mixing techniques.

This chapter presents the design of a miniaturised three stage analog polyphase filter implemented in low temperature co-fired ceramics (LTCC). The RF and Microwave industry has taken advantage of the numerous advantages offered by this technology that allows for high integration of embedded and mounted components into a single compact multilayered chip. To the author's knowledge, most of the reported miniaturised polyphase filters have been realised in CMOS [19][48][60] for frequencies above 1 GHz and no implementation in LTCC has been reported yet. A major challenge in implementing passive structures in CMOS is the high costs incurred especially due to additional modifications made to reduce the overall effects of parasitic elelments.

This chapter proposes the use of LTCC as a substrate choice for implementation of a polyphase filter operating at low frequencies - 100 MHz to 300 MHz. The motivation for this study is to analyse the viability of LTCC for the implementation of such a passive structure. The chapter seeks to present a successful design and to analyse the challenges associated with the design and manufacture of the device.

Validation of the design is by way of full wave electromagnetic simulation by Sonnet.

5.2 Polyphase Networks

A polyphase signal as the name suggests is a signal comprising a set of two or more vectors. These vectors usually correspond to voltages of equal frequencies but different phase.

Polyphase signals are defined as symmetric if all vectors are equal in magnitude and are equally spaced in phase. Asymmetric polyphase signals, on the other hand, comprise n unbalanced vectors differing in magnitude. An asymmetric signal can be represented as the sum of n symmetric polyphase signals. Any polyphase signal has a sequence with a polarity dependent on the phase order of the signal vectors with respect to each other.

A polyphase network generally consists of n input terminals and n output terminals. The network is symmetrical in the sense that the path from each input to its corresponding output is identical to the paths from the other inputs to their respective outputs.

To drive a polyphase network, a polyphase signal with n vectors equal in number to the number of inputs is applied at the input of the network. The order by which the signal vectors are applied to adjacent inputs defines the phase sequence of the polyphase signal. Figure 5.3 shows the four vectors of a symmetrical four-phase signal with all vectors spaced 90^0 in phase. Each vector represents an alternating voltage of magnitude, V, and angular frequency, ω.

The phase order of the signal vectors determines whether the signal vector into the first input port leads or lags that into the second input port. In the same manner, it also determines whether the vector into the second port leads or lags the signal vector applied at port three etc. In figure 5.3, the positive phase sequence is seen to have a clockwise phase rotation. The signal vector into port one of a four-input-port network leads the signal vector into the second port by 90^0 . The

reverse is true for the negative phase sequence that follows an anti-clockwise phase order; in this case, the signal vector into port one lags the signal vector into port two by 90^0 .

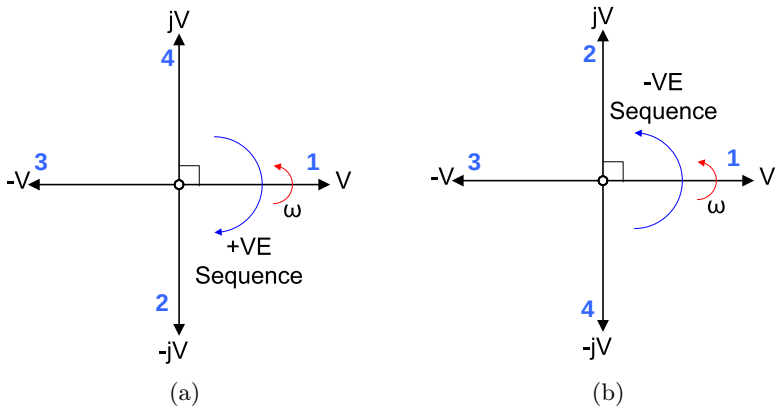


Figure 5.3: Four phase signal with (a) Positive sequence and (b) Negative Sequence

The four-phase representation of one stage of an RC sequence asymmetric polyphase network comprising a combination of symmetrical single phase sections is shown in figure 5.4.

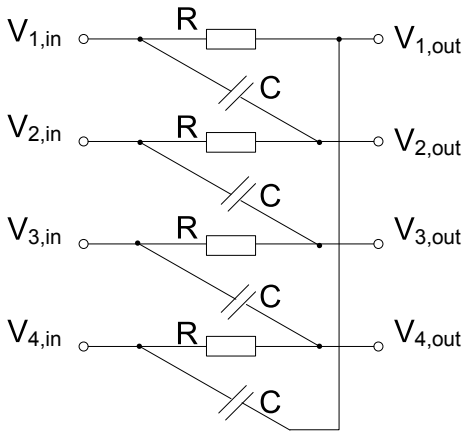


Figure 5.4: One Stage Network of RC Sequence Asymmetric Polyphase Networks

The chain matrix for a single phase of the network in figure 5.4 is derived to relate the input voltage and current to the output voltage and current as

$$\begin{bmatrix} V_{k,in} \\ I_{k,in} \end{bmatrix} = \frac{1}{1 - jsRC} \begin{bmatrix} 1 + sRC & 1 \\ 2sC & 1 + sRC \end{bmatrix} \begin{bmatrix} V_{k,out} \\ I_{k,out} \end{bmatrix} \tag{5.9}$$

for a positive phase sequence. A negative sequence network is then represented as

$$\begin{bmatrix} V_{k,in} \\ I_{k,in} \end{bmatrix} = \frac{1}{1 + jsRC} \begin{bmatrix} 1 + sRC & 1 \\ 2sC & 1 + sRC \end{bmatrix} \begin{bmatrix} V_{k,out} \\ I_{k,out} \end{bmatrix} \tag{5.10}$$

From these, the respective open-circuit ($I_{k,out} = 0$) voltage transfer functions for a positive and

negative sequence can be expressed as

$$H(\omega) = \frac{V_{k,out}}{V_{k,in}} = A\frac{1+\omega RC}{1+j\omega RC} = \frac{\omega_p+\omega}{\omega_p+j\omega} \tag{5.11}$$

and

$$H(-\omega) = \frac{V_{k,out}}{V_{k,in}} = A\frac{1-\omega RC}{1+j\omega RC} = \frac{\omega_p-\omega}{\omega_p+j\omega} \tag{5.12}$$

where A is an amplification factor and $\omega_p = \frac{1}{RC}$ is the unity gain frequency. Zero gain is expected when $\omega = -1/RC$ for the positive sequence and when $\omega = 1/RC$ for the negative sequence. It should be noted that $H(\omega) \neq H(-\omega)$.

Polyphase networks may have physical symmetry, but they exhibit asymmetrical frequency response due to input sequences of different polarities. For a setting where a desired passband and its mirrored image occur at an IF frequency relative to DC, either the passband or the image signal will be transmitted while the other is attenuated depending on the polarity of the vector sequence of the input signal. It is this discrimination based on sequence-dependent insertion loss characteristics that leads to the name 'sequence asymmetric' polyphase networks.

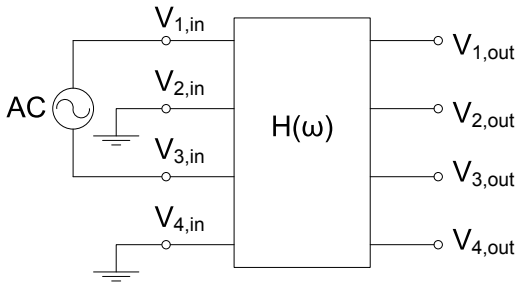
If the input has a positive sequence, the resulting output will also be a positive sequence, and in a similar manner, a negative input sequence will result in a negative output sequence.

The designs in this chapter use the generalised four-phase polyphase network segment shown in figure 5.4 to realise a three segment polyphase filter network. As has been stated, the four phases are symmetric and owing to this, the chain matrix of a single phase suffices as a chain matrix representation of the four-phase network.

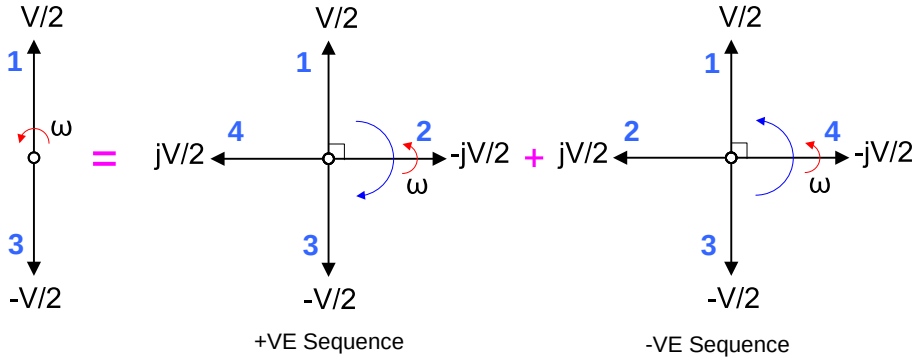
5.3 Quadrature Signal Generation

Supposing a four-phase polyphase network is driven by only two phases in the form of a differential input signal as shown in figure 5.5a, while the other two inputs are grounded, it can be shown that this setup is sufficient to generate quadrature outputs with good gain matching.

The two vector input signals can be represented as a summation of two symmetrical four-phase input sequences of opposite polarity as shown in figure 5.5b. Using superposition, the overall output of the network can then be represented as the summation of the outputs due to each sequence separately.



(a) Circuit diagram



(b) Decomposing a two-phase input sequence into two four-phase symmetric vector sequences

Figure 5.5: Quadrature Signal Generation using Four-phase Polyphase Network

The network's transfer function, $\frac{V_{k,out}}{V_{k,in}}$, for the positive phase sequence is denoted $H(\omega)$ while that for the negative phase sequence will be $H(-\omega)$. Pairing up the components of the two symmetrical four-phase sequences in the numerical order labelled in blue gives

Component	Positive Sequence	Negative Sequence
V_1	$\frac{V}{2}$	$\frac{V}{2}$
V_2	$-j\frac{V}{2}$	$j\frac{V}{2}$
V_3	$-\frac{V}{2}$	$-\frac{V}{2}$
V_4	$j\frac{V}{2}$	$-j\frac{V}{2}$

Substituting these values of input voltage in

$$V^{+}_{k,out} = H(\omega) \cdot V_{k,in}$$

$$V^{-}_{k,out} = H(-\omega) \cdot V_{k,in}$$

and summing the resulting output voltages due to the opposite sequences gives the four outputs as

$$V_{1,out} = \frac{V}{2}\left[H(\omega) + H(-\omega)\right] \tag{5.13}$$

$$V_{2,out} = -j\frac{V}{2}\left[H\left(\omega\right) - H\left(-\omega\right)\right] \tag{5.14}$$

$$V_{3,out} = -\frac{V}{2}\left[H\left(\omega\right) + H\left(-\omega\right)\right] \tag{5.15}$$

$$V_{4,out} = j\frac{V}{2}\left[H\left(\omega\right) - H\left(-\omega\right)\right] \tag{5.16}$$

These comprise two in-phase signals, $V_{1,out}$ and $V_{3,out}$, and two quadrature signals $V_{2,out}$ and $V_{4,out}$. If the total output voltage due to the four ports is expressed as

$$V_{out} = V_{I,out} + V_{Q,out} \tag{5.17}$$

where I and Q denote 'in-phase' and 'quadrature' components respectively, then $V_{I,out} = V_{1,out} - V_{3,out}$ and $V_{Q,out} = V_{2,out} - V_{4,out}$ can be presented as

$$V_{I,out} = V\left(H\left(\omega\right) + H\left(-\omega\right)\right) \tag{5.18}$$

$$V_{Q,out} = -jV\left(H\left(\omega\right) - H\left(-\omega\right)\right) \tag{5.19}$$

The gain ratio due to the quadrature outputs can be computed from these as the ratio of the quadrature-phase outputs to the in-phase outputs, $\frac{V_Q(s)}{V_I(s)}$.

For a single stage RC four-phase polyphase network, the transfer functions for the positive and negative phase sequences have been presented in equations 5.11 and 5.12 in terms of the R and C components. The gain ratio for a single stage network is then given by

$$\frac{V_Q\left(s\right)}{V_I\left(s\right)} = j\omega RC \tag{5.20}$$

This network has a limited frequency range within which good gain matching can be achieved between the two quadrature outputs. This is because the two quadrature outputs only have equal amplitudes at a single frequency $\omega = {}^1/_{RC}$ limiting its use to narrowband applications. The ratio of the two outputs is purely imaginary showing that the phase difference between the two is 90^0 at all frequencies. A plot of this can be seen in figure 5.6 for a single stage polyphase network centred at 100 MHz. At this point, the gain is unity and follows a gradient determined by the product RC.

Addition of extra polyphase network stages achieves broadband quadrature response with better gain and phase matching. For each additional stage, the gain ratio is reduced further within the band of interest. The transfer function for a network with more than a single stage is calculated as the product of the chain matrices of the individual stages. The gain ratio can then be computed from the open-circuit voltage transfer matrices. For a two-stage four-phase polyphase network, the gain ratio is derived to obtain

$$\frac{V_Q(s)}{V_I(s)} = \frac{j\omega(R_1C_1 + R_2C_2)}{1 + \omega^2(R_1R_2C_1C_2)} \tag{5.21}$$

The quadrature generating network in this case has two unity gain frequencies at $f_1 = 1/2\pi R_1C_1$ and $f_2 = 1/2\pi R_2C_2$. Within this band of frequencies, the quadrature outputs are highly matched in terms of gain and phase. The frequency at which the maximum gain ratio occurs is computed as the geometric mean of the unity gain frequencies as follows

$$f_{max} = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}} \tag{5.22}$$

The magnitude of the maximum gain ratio at this frequency is then calculated as

$$\left|\frac{V_Q(s)}{V_I(s)}\right|_{f_{max}} = \frac{R_1C_1 + R_2C_2}{2\sqrt{R_1C_1R_2C_2}} \tag{5.23}$$

For a polyphase response with two unity gain at 100 MHz and 173 MHz, the gain ratio of a two-stage polyphase filter is plotted in figure 5.6. The maximum gain ratio is calculated using equation 5.23 to obtain 0.3222 dB which corresponds to that in the curve at the geometric mean frequency of 131.53 MHz.

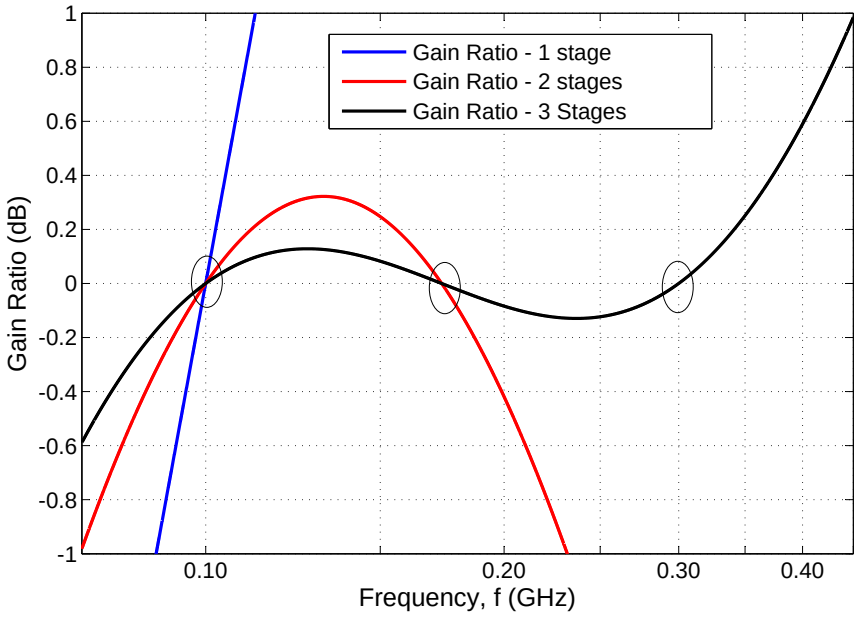


Figure 5.6: gain ratio of One-, Two- and Three-Stage Sequence Asymmetric Polyphase Filters

Figure 5.6 also shows the gain ratio for a three-stage polyphase network with the unity gain frequencies of the three segments/stages as $100MHz$, $173MHz$ and $300MHz$. The gain matching is even better due to the addition of the third segment. The centre unity frequency should be the geometric mean of the outer unity gain frequencies if an equal ripple response is desired. The gain ratio for a three-stage polyphase network can be expressed as

$$\frac{V_Q(s)}{V_I(s)} = \frac{j\left(\omega\left(R_1C_1 + R_2C_2 + R_3C_3\right) - \omega^3\left(R_1R_2R_3C_1C_2C_3\right)\right)}{1 + \omega^2\left(R_1R_2C_1C_2 + R_1R_3C_1C_3 + R_2R_3C_2C_3\right)} \tag{5.24}$$

The ratio is seen to be purely imaginary again indicating a phase difference of exactly 90^0 between the two outputs.

5.4 Image Rejection

Image rejection ratio (IRR) or suppression is defined as the ratio of the magnitude of the transfer function of the positive frequency response to that of the negative frequency response. It is mathematically expressed, from equations 5.11 and 5.12, as

$$IRR(\omega) = \frac{|H(\omega)|}{|H(-\omega)|} = \frac{\omega_p - \omega}{\omega_p + \omega} \tag{5.25}$$

The phase error of a polyphase network, δ, defined as the deviation from quadrature, or 90^0, is a very important parameter in the design of a polyphase network. It relates to the image rejection ratio through the relationship [72]

$$IRR = -20\log\left(\tan\left(\frac{1}{2}\delta\right)\right) \tag{5.26}$$

For the same parameter specifications used to plot figure 5.6, the phase error for three polyphase networks of one, two and three segments/stages respectively is plotted in figure 5.7. It can be noted that the phase error decreases with the number of stages/segments of the four-phase polyphase network.

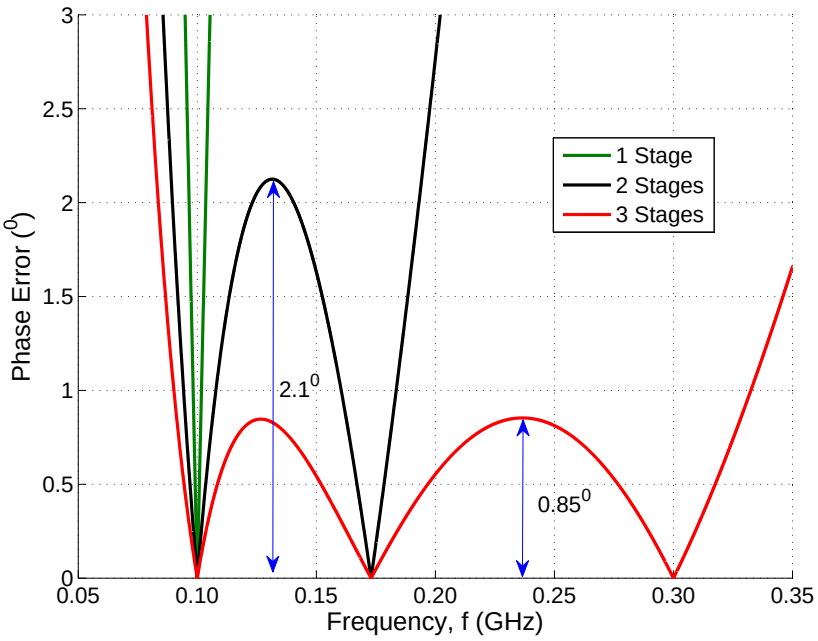


Figure 5.7: Phase Error of One-, Two- and Three-Stage Sequence Asymmetric Polyphase Filters

A plot of the magnitudes of the transfer function for networks driven by both positive and negative phase sequences is shown in figure 5.8. The image rejection in decibels for any given number of stages is the difference, in decibels, of the magnitude of the positive frequency response and the negative frequency response. The more the number of stages/segments the larger the image suppression. The bandwidth over which strong image rejection is achieved also increases.

The image rejection ratio of physically implemented polyphase networks is expected to be degraded from the theoretically calculated values majorly because of components mismatch. Components mismatch results in gain mismatches and can be accounted for in a generalised transfer function given by [72]

$$H_m(s) = \frac{A\omega_p\left(1-\frac{\triangle A}{2A}\right)\left(1-\frac{\triangle\omega_p}{2\omega_p}\right)}{s+\omega_p\left(1-\frac{\triangle\omega_p}{2\omega_p}\right)} + j\frac{A\left(1+\frac{\triangle A}{2A}\right)s}{s+\omega_p\left(1+\frac{\triangle\omega_p}{2\omega_p}\right)} \tag{5.27}$$

where $\triangle A$ is the gain mismatch and $\triangle\omega_p$ is the deviation in unity gain frequency from that of a network with no components imbalance.

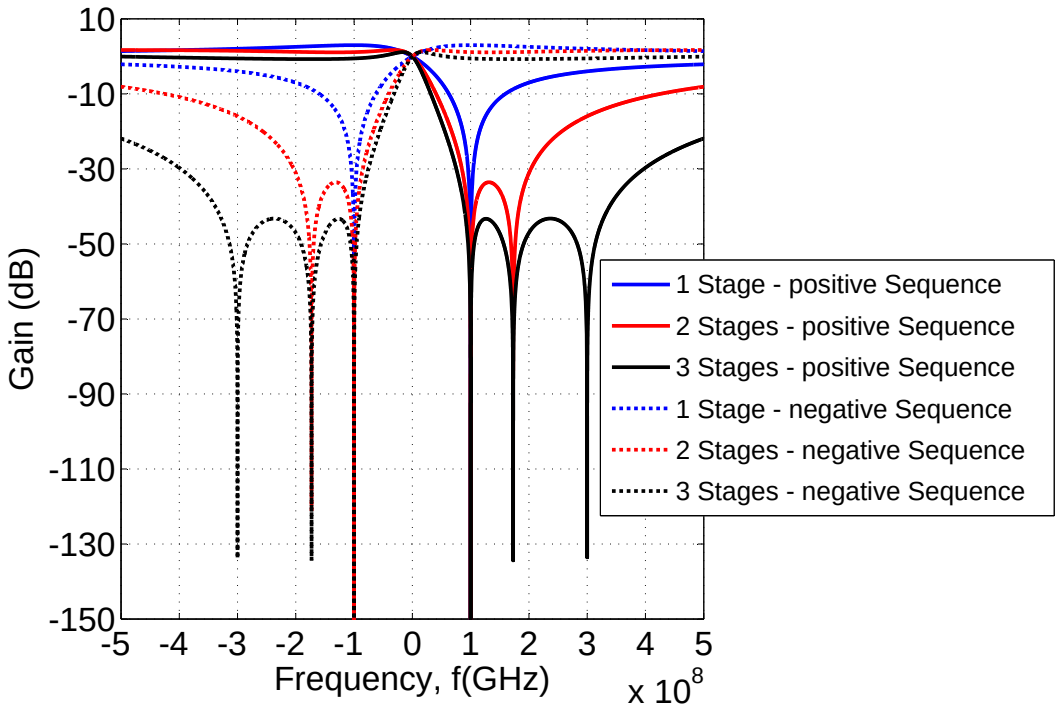


Figure 5.8: Complex Frequency Response of One-, Two- and Three-Stage Sequence Asymmetric Polyphase Filters

For N multiple cascaded stages, the IRR is computed as the product of the IRR of each of the single-stage polyphase network segments and can be expressed as

$$IRR_N(\omega) = \prod_{n=1}^{N} IRR_n(\omega)$$

5.5 Design of a 3-Section Polyphase Filter

5.5.1 Important Design Aspects

Some of the important aspects that have to be considered in the design of a polyphase filter are outlined below.

5.5.1.1 Number of Segments

The number of segments, N, necessary to achieve a minimum suppresion, S, can be computed as [72]

$$N = \log_2\left(\frac{F_{max}}{10 \times F_{min}}\right) + \frac{S}{10} \tag{5.28}$$

where F_{max} and F_{min} are the maximum and minimum frequency of the operational band for the network.

5.5.1.2 Per Segment RC Values

Once the number of required segments is known, it is recommended to choose RC values that result in unity gain frequencies that are spaced equidistant from each other between the first and the last frequency points, on a logarithmic scale.

For N segments, a formula for computing the product of the RC components for each segment is given as [72]

$$R_x C_x = \frac{\left(\sqrt[N-1]{\frac{F_{max}}{F_{min}}}\right)^{(1-x)}}{2\pi F_{min}}; \quad x = 1, 2, ..., N \tag{5.29}$$

5.5.1.3 Distribution of Components

In a network comprising same value resistors for all segments, maximum gain is obtained when the smallest capacitors are placed at the output segment of the network, giving the smallest RC product.

On the other hand, a network comprising same value capacitors in each section will achieve maximum gain if the largest resistors are placed at the output of the network so that the largest RC product is at the output.

The RC products for each section should either increase or decrease from input to output in order to maximise the gain.

5.5.1.4 Symmetry of Network

Due to the symmetical number of inputs and outputs, it is advisable to design the physical layout of the polyphase circuit so that it is also symmetrical.

5.5.2 Filter Specifications

A passive sequence asymmetric polyphase filter is designed based on the following specifications:

Operational Bandwidth	100 MHz - 300 MHz
Maximum gain ratio	0.5 dB
Maximum Phase Error	1^{o}
Minimum Image Suppression	41 dB

As a starting point, formulas presented in the preceding sections are used to compute the number of sections required to meet the given set of specifications. The implementation of this filter is initially done with a circuit model implemented in AWR Microwave Office (MWO) to analyse the response for the polyphase filter with the determined number of segments.

5.5.3 Circuit Design

A three segment network (see figure 5.9) is found to provide the desired image suppression required. The image suppression and gain ratio measurements are done by feeding the network in two different ways:

1. To determine the image suppression due to the network, two differential input signals feed the network as shown in figure 5.10a. The voltages into adjacent inputs of the four phase network are at 90^{0} relative to each other. Two input sequences, positive and negative, are both assessed and the response at the output due to both is plotted in figure 5.11.

2. To determine the gain ratio between the quadrature outputs of the four-phase network, the in-phase inputs of the network are fed by a differential 180^{0} input signal (see figure 5.10b). The other two inputs are grounded. The resulting gain ratio is plotted in figure 5.12.

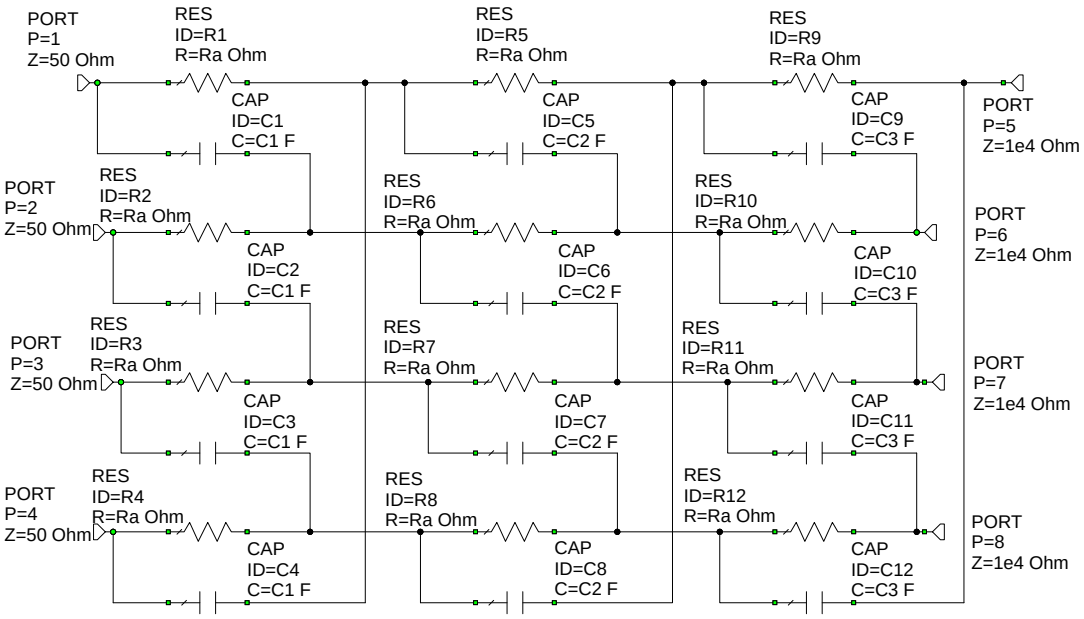


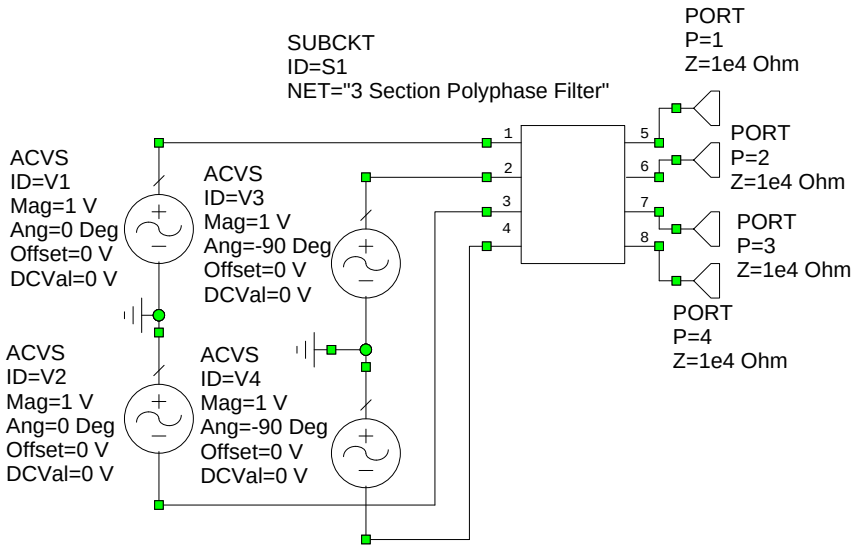
Figure 5.9: Three-stage MWO Circuit Model

An image suppression of 42 dB is achieved with this network with a maximum gain ratio of approximately 0.064 dB across the frequency range of interest - 100 MHz to 300 MHz.

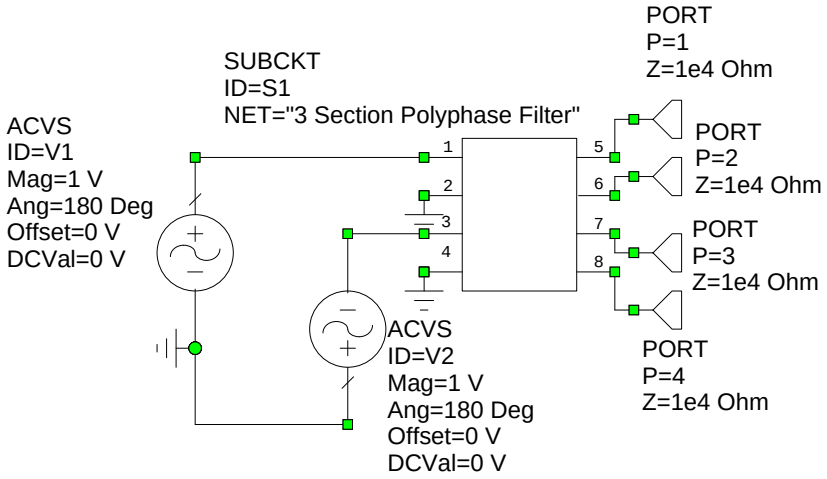
It can also be seen from figure 5.11 that the centre unity gain frequency is positioned at the geometric mean of the unity gain frequencies of the two outer unity gain frequencies (173 MHz), on a logarithmic scale. This achieves an approximate equiripple response.

The less the gain achieved within the network, the less the cumulative gain of the signal as it goes through the subsequent stages of a transceiver network.

In figure 5.13 the output voltage at port one relative to an input voltage of 1 V is compared for different values of terminating impedance, Rl.



(a) Image Suppression Measurement



(b) Gain Ratio Measurement

Figure 5.10: Driving PPF Network

For the network in figure 5.9, the component values in table 5.1 are chosen:

Component	Value
Ra	1.000 kΩ
C1	1.592 pF
C2	0.919 pF
C3	0.531 pF

Table 5.1: Component Values for Circuit in figure 5.9

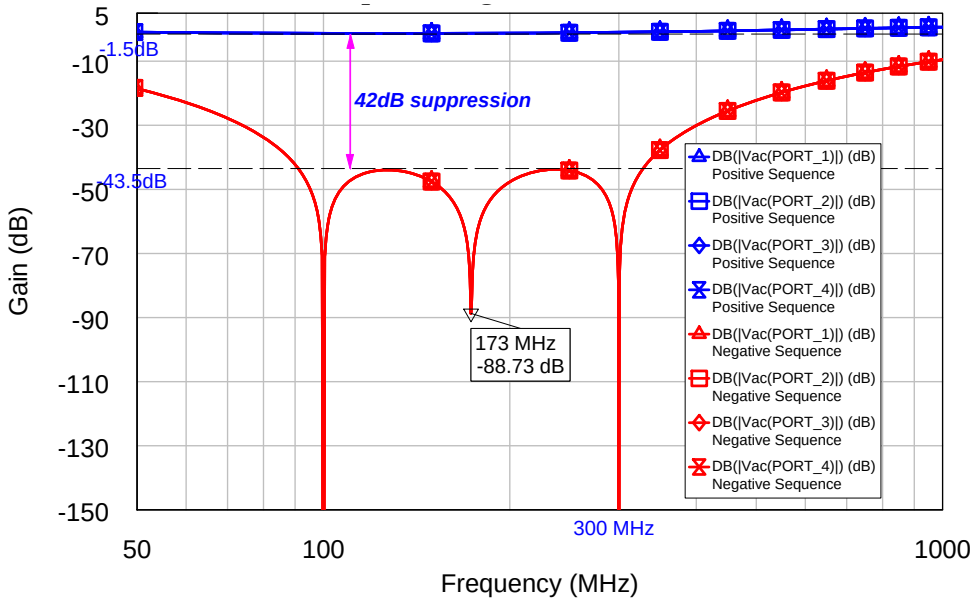


Figure 5.11: Image Suppression of 3-Segment Polyphase filter network

The resistors are chosen to have an equal value for all three segments because their LTCC implementation would otherwise require different resistive pastes for each value. The resistor pastes as will be seen later are engineered to provide set values of resistance per square. It will also be shown that since the resistors are realised in distributed circuit form, reactive parasitics are encountered, resulting in variation of the resistor values with frequency.

The capacitors are realised using the same conductive paste regardless of their value so it is easier to set this as the component with varying values from one segment to the next.

Component mismatch is to be expected in the three dimensional realisation of the polyphase filter due to different factors such as the layout of the components and the resultant parasitic reactances due to the distribution of the components in the layout.

The manufactured device can be expected to exhibit more significant effects of component mismatch due to dimensional inaccuracies as a result of the fabrication process. It is therefore important to conduct a sensitivity analysis to establish possible explanations for certain changes in the filter response.

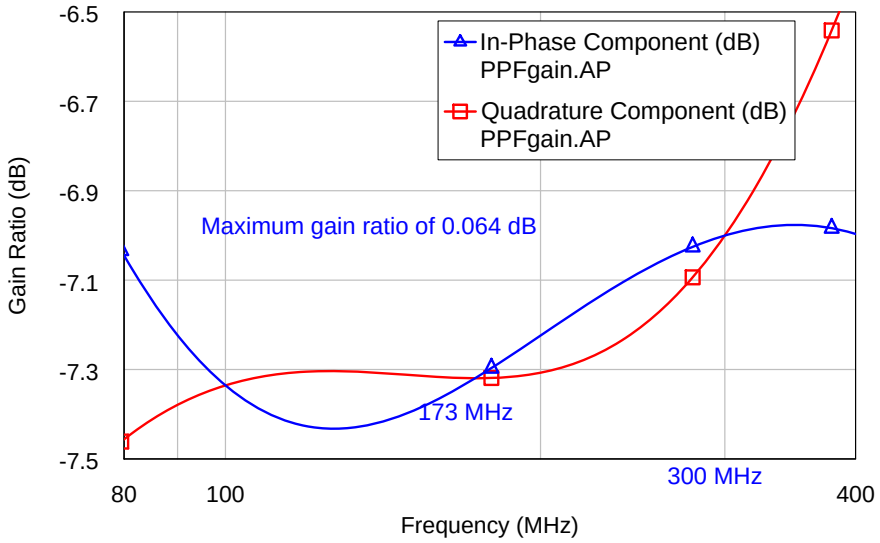


Figure 5.12: Gain Ratio of 3-Segment Polyphase filter network

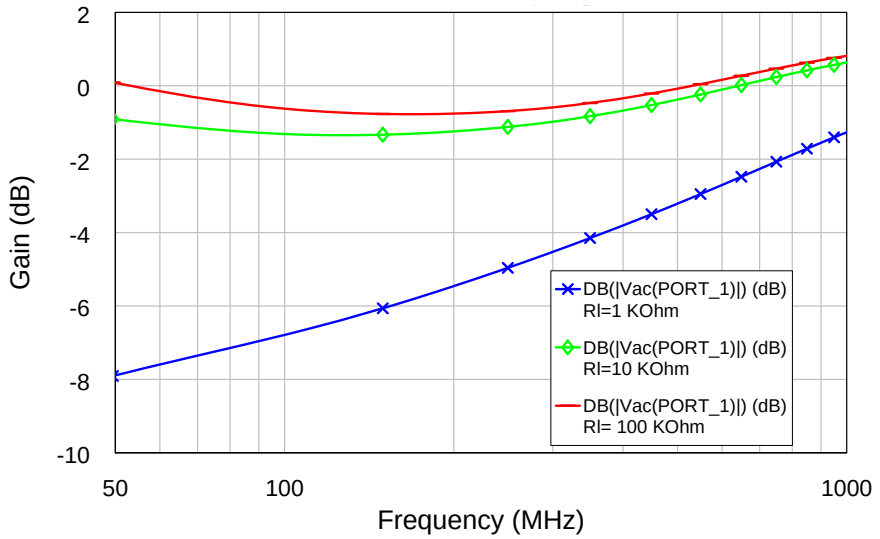


Figure 5.13: Effect of Terminating Impedance on the Output Voltage of Polyphase Filter

5.5.4 Sensitivity Analysis

In this subsection, the RC product resulting in the first unity gain frequency at 100 MHz is deviated from its original value by ±1%, ±2% and ±5%. For each of these deviations, the gain due to a positive input phase sequence is analysed and the results are shown in figure 5.14.

A positive deviation results in a decrease in the insertion loss of the network relative to the original RC product curve plotted in blue. The biggest decrease is registered for the largest percentage deviation of 5 percent.

The gain due to the negative phase sequence is also analysed to observe the shift in frequency of the first unity gain frequency, $\triangle f_{p1}$, from 100 MHz and the resulting variation in the maximum

gain obtained in the 100 MHz to 300 MHz frequency range. A shift to a lower frequency is observed for a positive deviation in the RC product while a negative deviation results in a positive frequency shift. The magnitude of frequency shift increases with the value of deviation so that a 1 % deviation will result in less of a unity gain frequency shift than a 5 % deviation on the RC product. A plot displaying this is presented in figure 5.15.

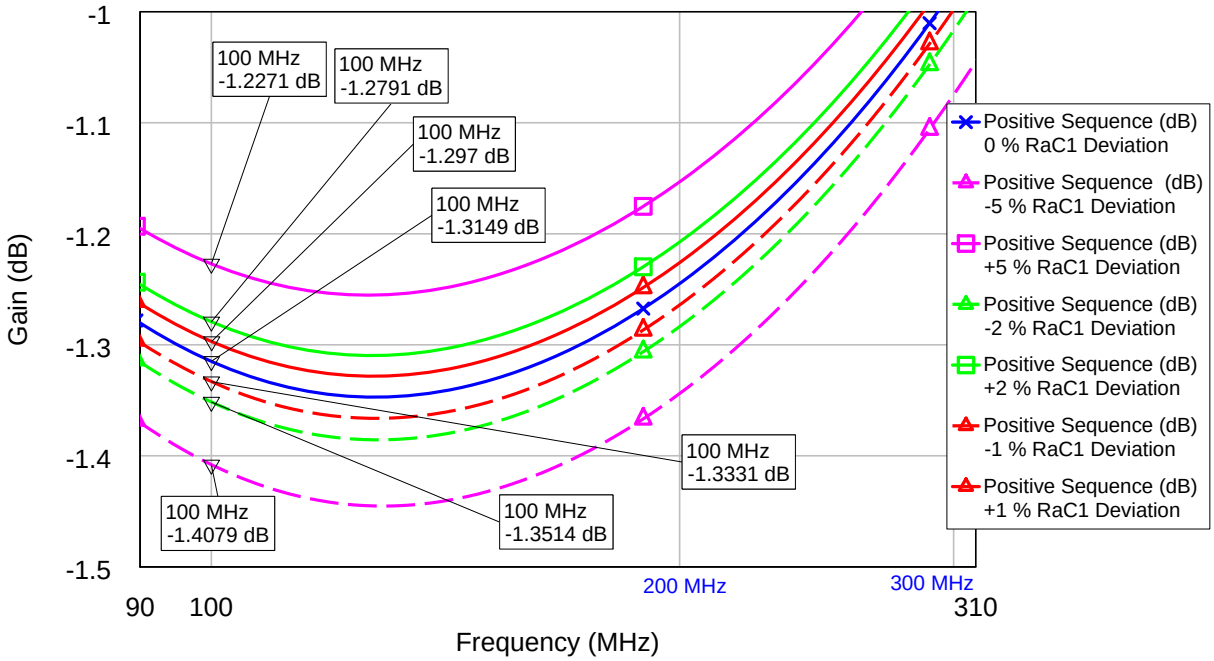
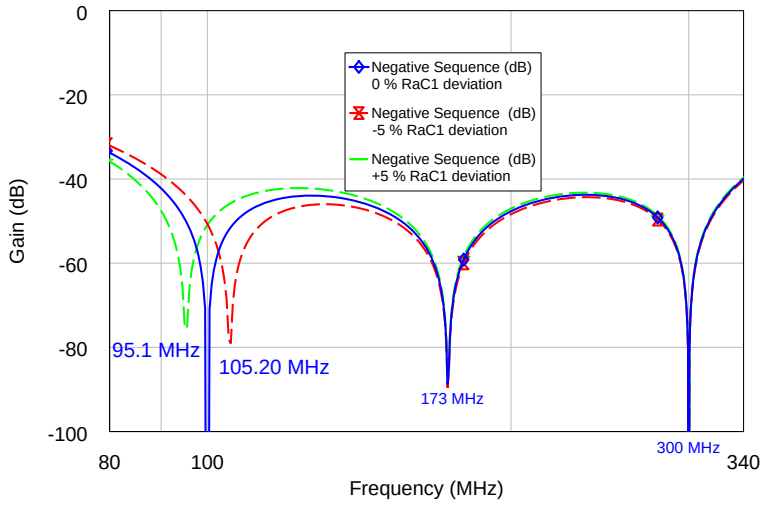


Figure 5.14: Positive Sequence Gain Variation due to (+/-)1%, (+/-)2% and (+/-)5% Variations in the RC Product of the First Unity Gain Frequency

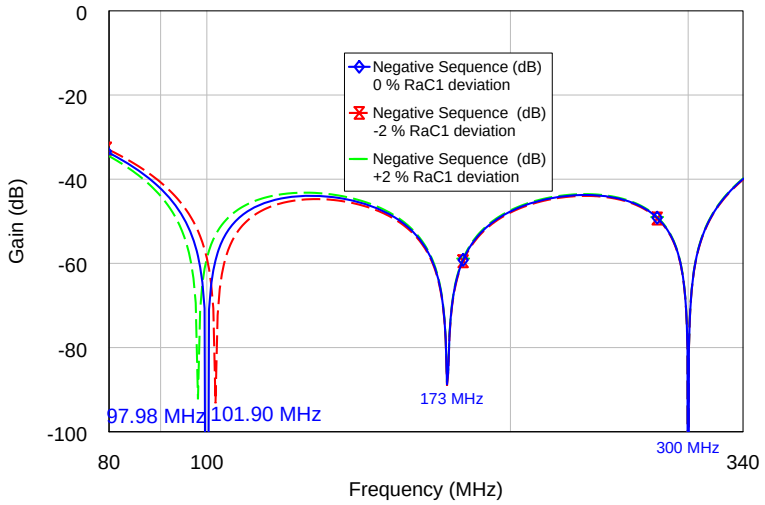
When the circuit is driven at the input as was shown in figure 5.10b, the gain ratio can is also be analysed to see how it varies with the different percentage deviations. Gain ratio is seen to increase with percentage deviation.

Percentage RaC1 Deviation	+ 5 %	+ 2 %	+ 1 %	- 1 %	- 2 %	- 5 %
Positive Sequence Output Voltage (dB) @ 100 MHz	1.227	1.279	1.297	1.333	1.351	1.408
Change in Unity Gain Frequency, $\triangle f_{p1}$ (MHz), from 100 MHz	-4.90	-2.02	-1.00	1.00	1.90	5.20
Minimum -ve Sequence Output Voltage (dB) Deviation from 0 %	1.70	0.40	0.05	-0.73	-1.10	-2.20
gain ratio (dB); [Note: gain ratio at 0 % Deviation = 0.064 dB]	0.0785	0.0695	0.0667	0.620	0.056	0.051

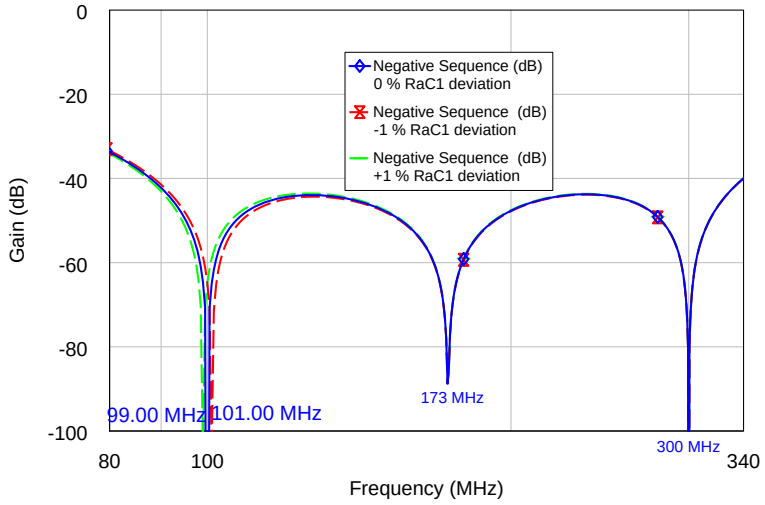
Table 5.2: Approximate Deduced Results from figures 5.14,5.15 and 5.16.



(a) 5 % Deviation

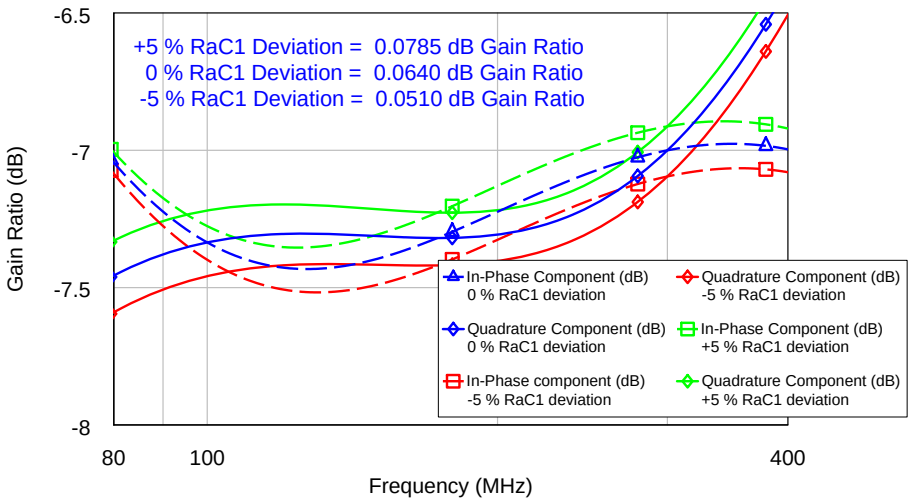


(b) 2 % Deviation

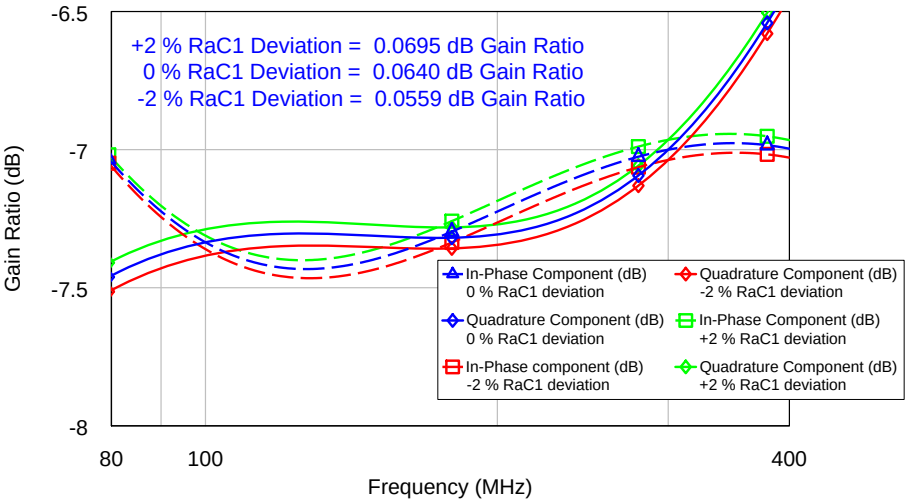


(c) 1 % Deviation

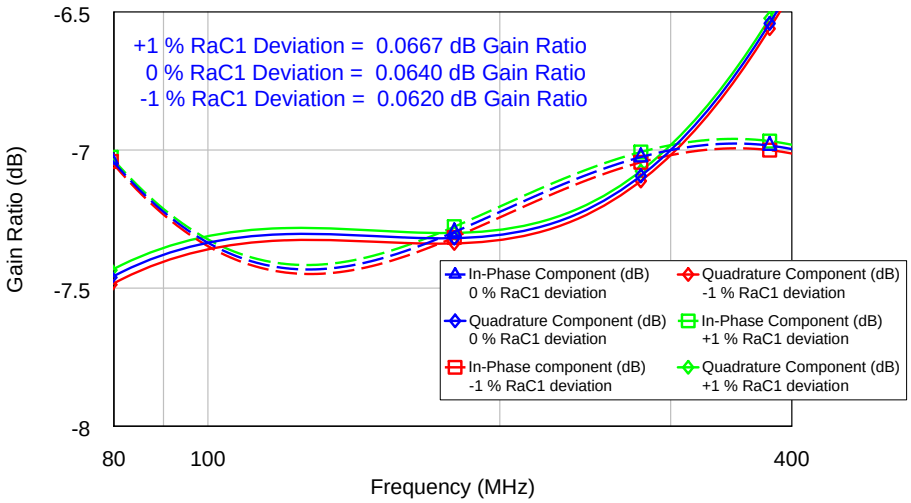
Figure 5.15: Negative Sequence Gain Variation due to (+/-)1%, (+/-)2% and (+/-)5% Variations in the RC Product of the First Unity Gain Frequency



(a) 5 % Deviation



(b) 2 % Deviation



(c) 1 % Deviation

Figure 5.16: Change in Gain Ratio due to (+/-)1%, (+/-)2% and (+/-)5% Variations in the RC Product of the First Unity Gain Frequency

In the simulated 3D version of this circuit, the RC product of any of or of all the unity gain frequencies can deviate from the design value resulting in several of the changes seen in figures 5.14,5.15 and 5.16. Even though changes due to RC product of only one unity gain frequency have been analysed, they are expected to aid in understanding performance changes in a full three-stage filter 3D full wave simulation responses. A sensitivity analysis due to all three unity gain frequencies would have many degrees of freedom and becomes taxing.

A summary of the results obtained from figures 5.14,5.15 and 5.16 is given in the table below.

The next section presents the description of the three dimensional implemenation of the 4-phase 3-segment polyphase filter in LTCC.

5.6 3D Implementation in LTCC

Three dimensional LTCC design considers a number of important factors relating to the distribution of the electrical components, the LTCC tape system to be used and the compatibility of different materials used as dielectrics, conductors and resistors.

At the beginning of the design process, some of the most important problem descriptions to bear in mind are among others:

1. Upon identification of an LTCC laboratory to fabricate the circuits, which materials are readily available so that the design can be implemented based on those. This determines the design thickness of the layers of the multilayered circuit and the total number of layers necessary to reduce the footprint as much as possible. It also determines the overall fired thickness of the circuit so as to gauge if it is acceptable in advance. Additionally, this also determines the choice of conductive and resistive pastes based on their compatibility with the available LTCC tape, as well as high dielectric constant fills for parallel-plate capacitors should those be needed. Most LTCC tape vendors usually recommend the right conductive and resistive materials for use with their tapes.

2. Given the total number of required components as derived from the circuit model, the layout that would best incorporate parasitic components and still realise minimal footprint should be identified. The component distribution should preferably be symmetrical to the best of the designer's ability.

3. Even though components must be packed compactly, there are a number of LTCC design rules that need to be heeded in terms of the placement of some elements of the circuit relative to others. Design rules and recommendations are mostly unique to specific LTCC tapes based on the electrical, chemical and mechanical properties of the materials to be used; however, many rules are also common to all materials. Often the fabricating laboratory would have additional recommendations to make the process easier for them. These must also be taken into account.

The 3 dimensional analysis is done in Sonnet EM software. The LTCC tape chosen for the design is the FERRO A6M tape and the thick film resistors are realised using the Ferro FX 87-102 resistive paste. Ferro A6M has a relative dielectric constant of 5.9 and a dissipation factor of 0.002. Ferro FX 87-102 has a resistivity per square of 1000 Ω/Sq. Conductive parts of the structure use gold as the conductive material.

The subsections that follow discuss different elements of three dimensional design.

5.6.1 Embedded Components

The resistive and capacitive components in the three segment polyphase filter are realised using embedded components.

Each component can be represented as an equivalent circuit model comprising other parasitic elements present due to the distribution of the transmission lines within the structure. The values of the three dimensional equivalents of components can, for this reason, differ from the ideal values used in the circuit model simulation.

Several iterations are required in the three dimensional structure to achieve a performance close to that of the circuit model.

Capacitive Components

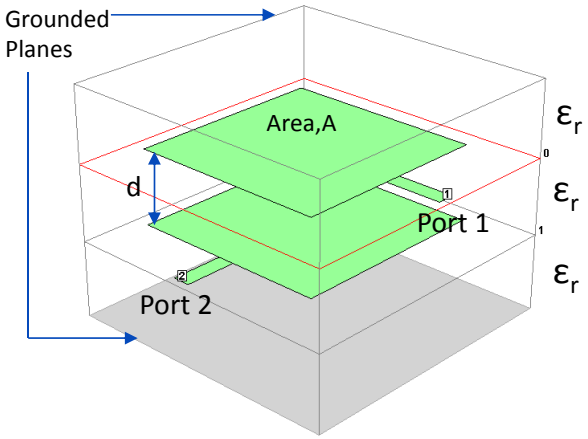
For the design in this chapter, the capacitive elements are realised through a parallel plate formation with a dielectric thickness, d = 185 μm. This thickness corresponds to the expected fired thickness of Ferro A6M tape. The design accounts for a z-axis shrinkage of approximately 27%. Each of the plates of the capacitor also forms a parasitic shunt capacitor with the ground planes on the opposite faces of the plate. For this reason, the plates are placed at a distance twice that separating the parallel plates of the main capacitive element away from the closest ground plane. Increasing this distance can further reduce the capacitance to ground and in effect increase the impedance of the parasitic paths, but that depends on the maximum allowable thickness of the overall structure.

The embedded parallel plate capacitor and its approximate equivalent circuit are shown in figure 5.17. Cs in the electrical equivalent circuit is the capacitance between the electrodes, Cp denotes parasitic capacitances to ground and the inductors and L represents the series inductances due to the electrode plates. The series resistance due to the electrode plates represents conductor loss and is denoted $Rs2$. The dielectric loss on the other hand is represented by the resistive element $Rs1$.

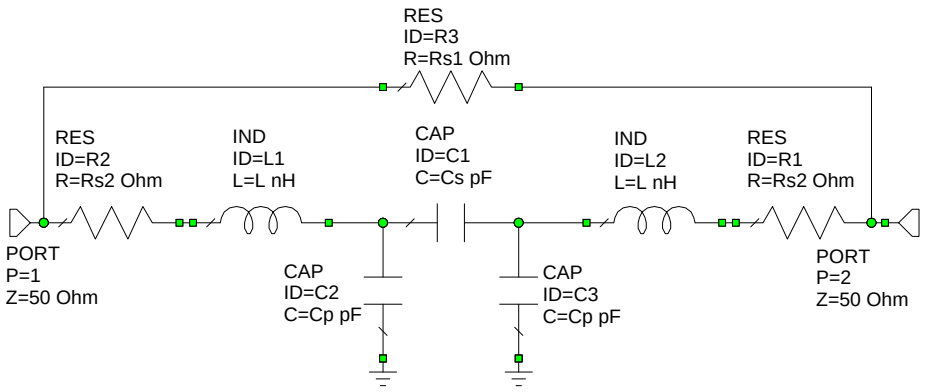
For an overlapping surface area of $(2.5\,mm \times 2.5\,mm)$, a ideal value of $Cs = 1.765\,pF$ can be calculated for the relative dielectric constant of Ferro A6M of 5.9. These particular dimensions are of interest for a polyphase filter segment with a unity gain frequency at 173 MHz.

A comparison between the real and imaginary parts of the structure analysed in Sonnet and the equivalent curves due to the circuit model are shown in figure 5.18. The real component comprises both frequency dependent and frequency independent elements. If $Rs1$ is assumed to be negligibly high. then for a fixed Cs, Cp, L and $Rs2$ can all the varied to change the real component so as to get a relatively good narrowband overlap about 173 MHz.

A better match over a wider frequency range from 50 MHz to 500 MHz can be seen for the imaginary part which is for the most part affected by varying Cp for a fixed Cs. Once this match is obtained, then the real part can be tuned by varying just L and $Rs2$ to obtain an overlap at 173 MHz.



(a) 3D Sonnet Structure of Parallel Plate Capacitor



(b) Equivalent Circuit Model of a Parallel Plate Capacitor

Figure 5.17: Embedded Capacitor

Resistive Components

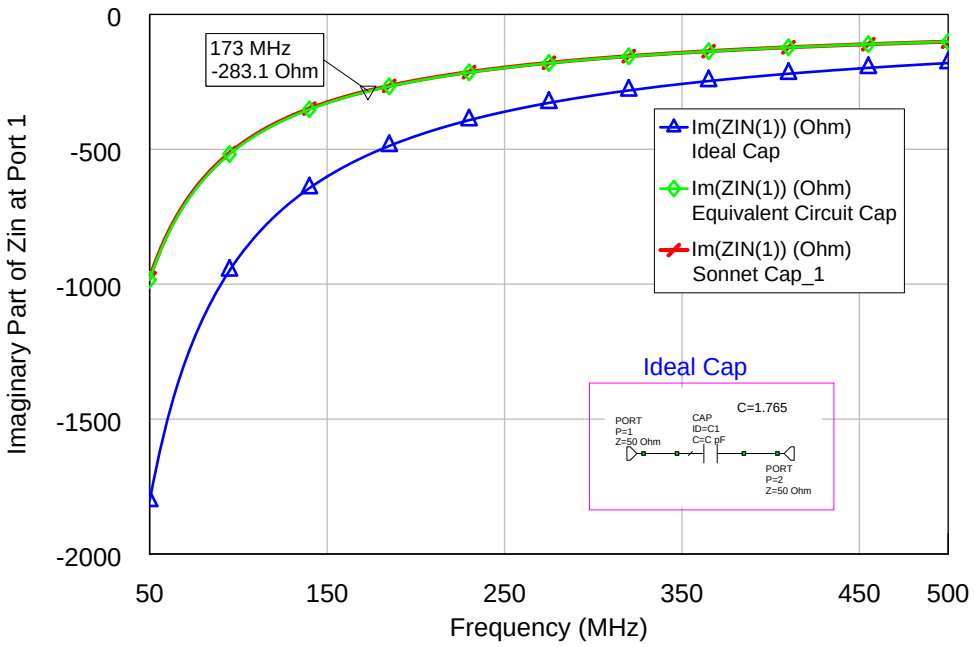
An LTCC thick film embedded resistor comprises a resistive paste screen printed in between two conductive termination pads on either end as shown in figure 5.19. The ideal resistor value is calculated from the resistivity per square, R_0, of the resistive paste and the dimensions of the printed resistor as follows

$$R = R_0 \cdot \frac{L}{W} \tag{5.30}$$

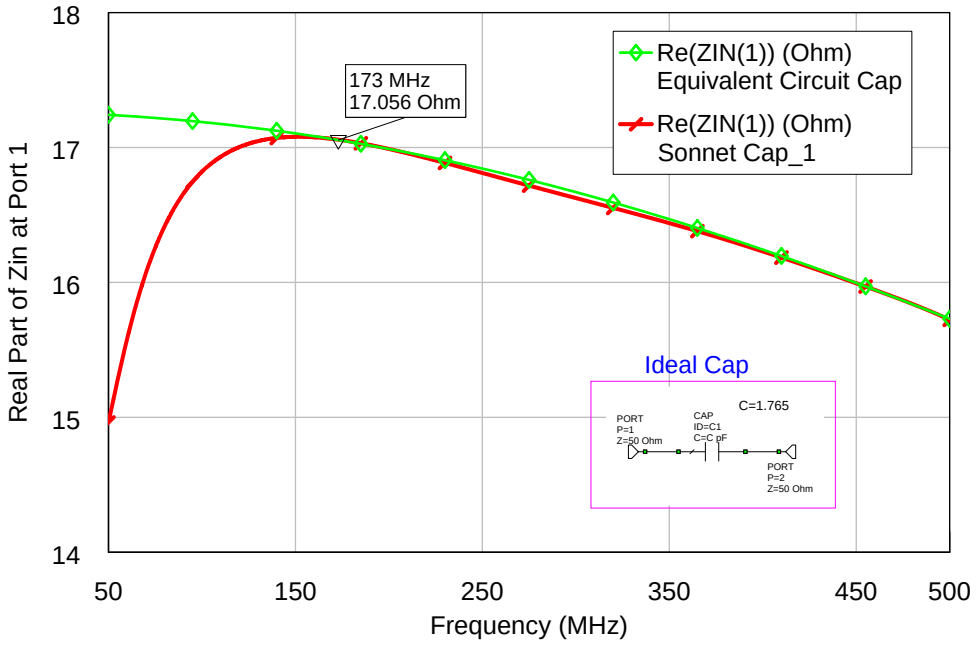
Ferro FX 87-102 has a resistivity per square of 1000 Ω/Sq. The approximate value of resistance required to achieve a unity gain frequency at 173 MHz is 521 Ω for a capacitance of 1.765 pF. An

L/W ratio of 0.5 will result in a resistance of 500 Ω. FX 87-102 has a tolerance of +/- 30%. The fired value of the resistance is therefore subject to variation within these tolerance values. It is however easier to model the resistor using dimensions as per equation 5.30 and then to tune the dimensions of the parallel plate capacitor to achieve a unity gain frequency at the required frequency.

The dimensions L and W are shown in figure 5.19.

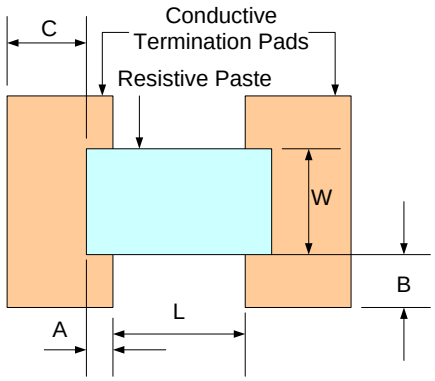


(a) Imaginary Part



(b) Real Part

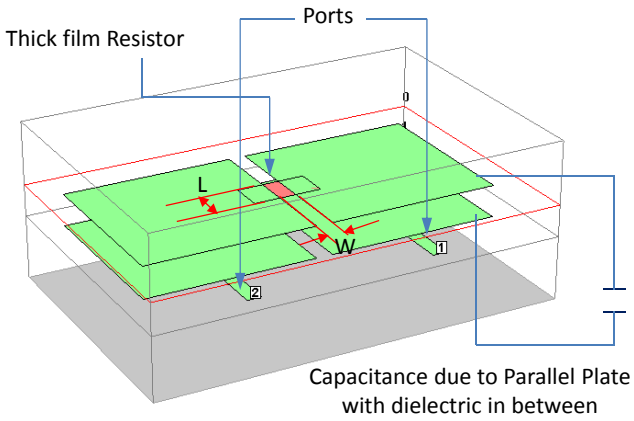
Figure 5.18: Input Impedance at Port 1 of Parallel Plate Capacitor in Figure 5.17



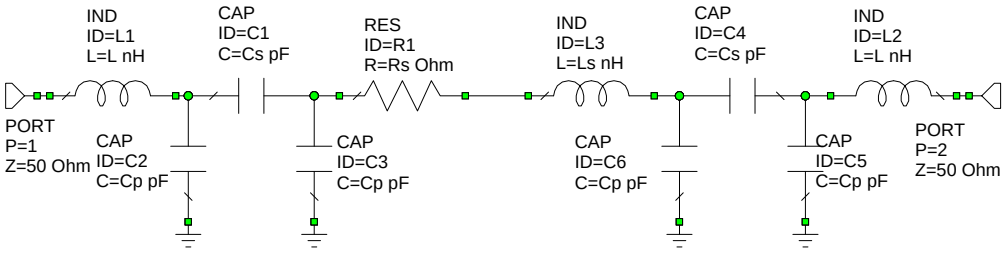
Layout	Minimum Spacing (mils)	Maximum Spacing (mils)
A	10	15
B	15	20
C	10	10

Figure 5.19: Embedded Resistor Design Guidelines from FERRO

The recommended overlap of the termination pads on either end of the thick film resistor and the resistive paste should conform to recommendations provided by Ferro as shown in figure 5.19.



(a) 3D Model in Sonnet



(b) Equivalent Circuit Model

Figure 5.20: Capacitors Realised from conducting End Pads of Resistor

The termination pads also have an overlapping area with the closest parallel ground planes resulting in parasitic capacitance.

To minimise the effect of this parasitic capacitance, the capacitors of the single segment polyphase filter are achieved by modelling a parallel plate capacitor directly on either end of the resistor as shown in figure 5.20a. Figure 5.20b shows a simplified circuit equivalent for the three dimensional structure.

5.6.2 Single-Stage 3D Implementation

Using this configuration, a single segment polyphase filter is realised in the form presented in figure 5.21. This structure has the advantage of symmetry as well as reduced parasitic influence on the performance due to the absence of additional connection lines between the resistors and capacitors.

One disadvantage of this structure, however, is that the ports are on different internal layers. If they are to transition to the outer layers, same length of lines can only be achieved by positioning the resultant ports on opposite ends of the structure. Otherwise, if they must be on the same side, then the vias used for the transitions would be of different lengths resulting in a slight phase delay in four of the paths.

An equivalent approximate circuit model representation of the three dimensional single stage polyphase filter comprising parasitics is shown in figure 5.22. The mathematical analysis of this structure becomes very complex and for most of the result comparisons that follow, an ideal circuit model is used instead. Variation of either the capacitance, C, or the resistance Rs, is still sufficient to tune the circuit model response to overlap with the three dimensional response.

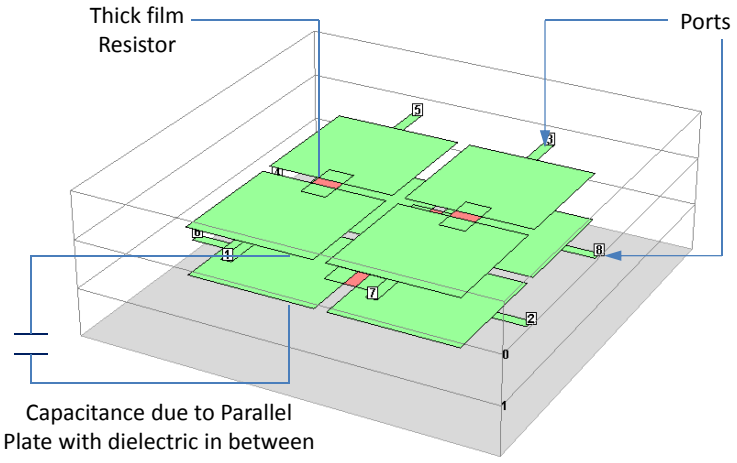


Figure 5.21: 3D Implementation of 4-Phase One-Segment Polyphase Filter Sonnet

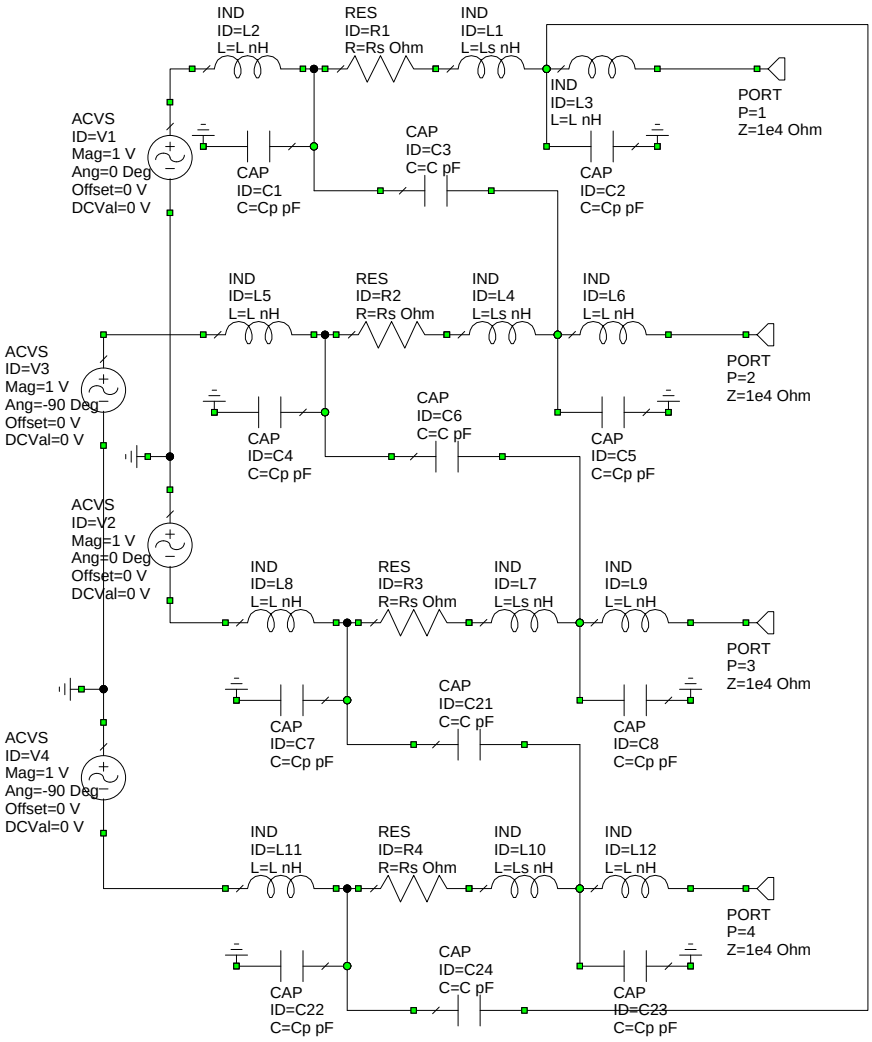


Figure 5.22: Equivalent Circuit Model of One-Segment Four-Phase Polyphase Filter

The simulated 8-port S-parameters of the sonnet structure are imported into Agilent's Microwave Office and the 4 input ports are driven differentially as was shown in figure 5.10a. The output ports are terminated in very high impedances of 10 kΩ. The gain measurement presented in figure 5.23 shows a unity gain frequency of 178.5 MHz, 5.5 MHz above the desired unity gain frequency.

The plate capacitors comprise square plates with a length of 2.5 mm and resistor dimensions, $L = 0.25\,mm$ and $W = 0.5\,mm$. The size of the parallel plates must therefore be increased in order to increase the parallel-plate capacitance and in doing so the unity gain frequency shifts down to the desired frequency.

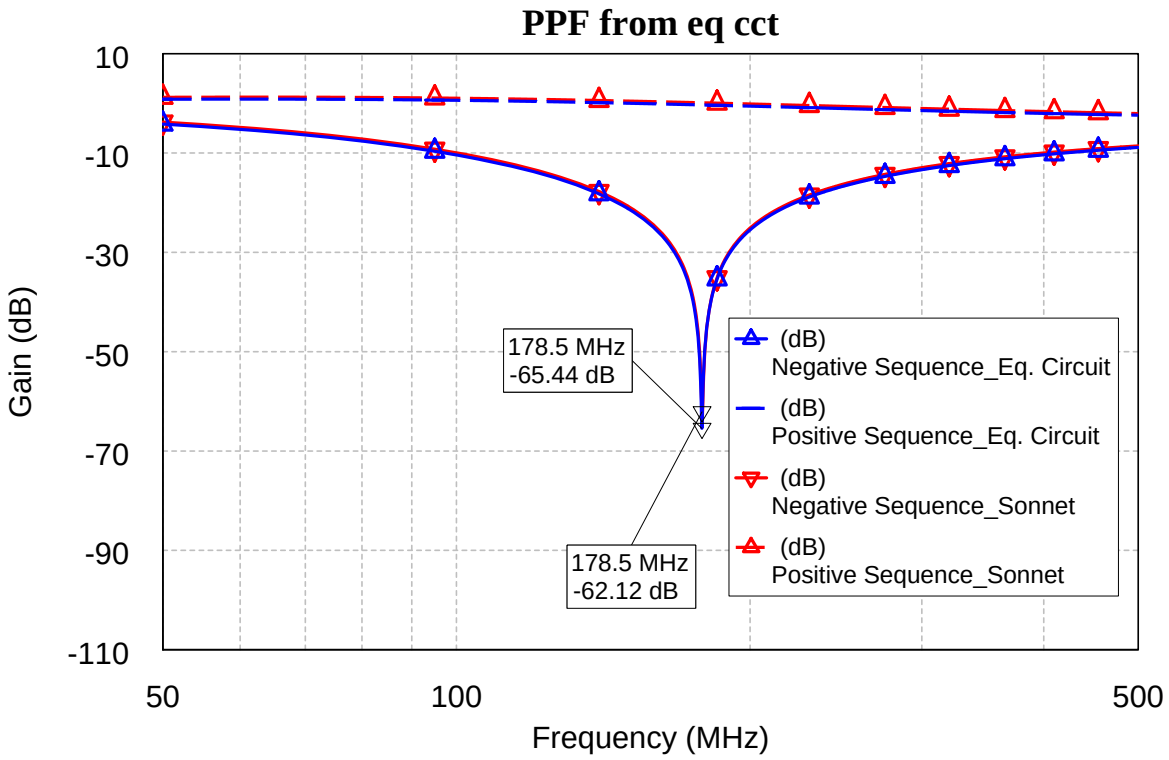


Figure 5.23: Gain of 1 Stage Polyphase Filter - Circuit Model Versus Sonnet Structure

5.6.3 Design Layout of 3-Stage Polyphase Filter

The dimensions of the three segments of polyphase filter are chosen to correspond with three unity gain frequencies - 100 MHz, 173 MHz and 300 MHz. The dimensions of the resistors remain constant for all three stages for an ideal value of 500 Ω whereas the dimensions of the parallel plate capacitors are different for the various segments.

The segments are vertically stacked with ground planes places in between each of them and the next. The desired component distribution is outlined in figure 5.24.

The port numbers are shown in squares and single or double apostrophes indicate which output ports in one segment connect to the inputs of the next.

The ground planes must be gridded so that the tape in the layers on either side of the plane can adhere to each other during lamination. The grid spacing recommended by Ferro is 0.381 mm for conductor thickness of 0.254 mm.

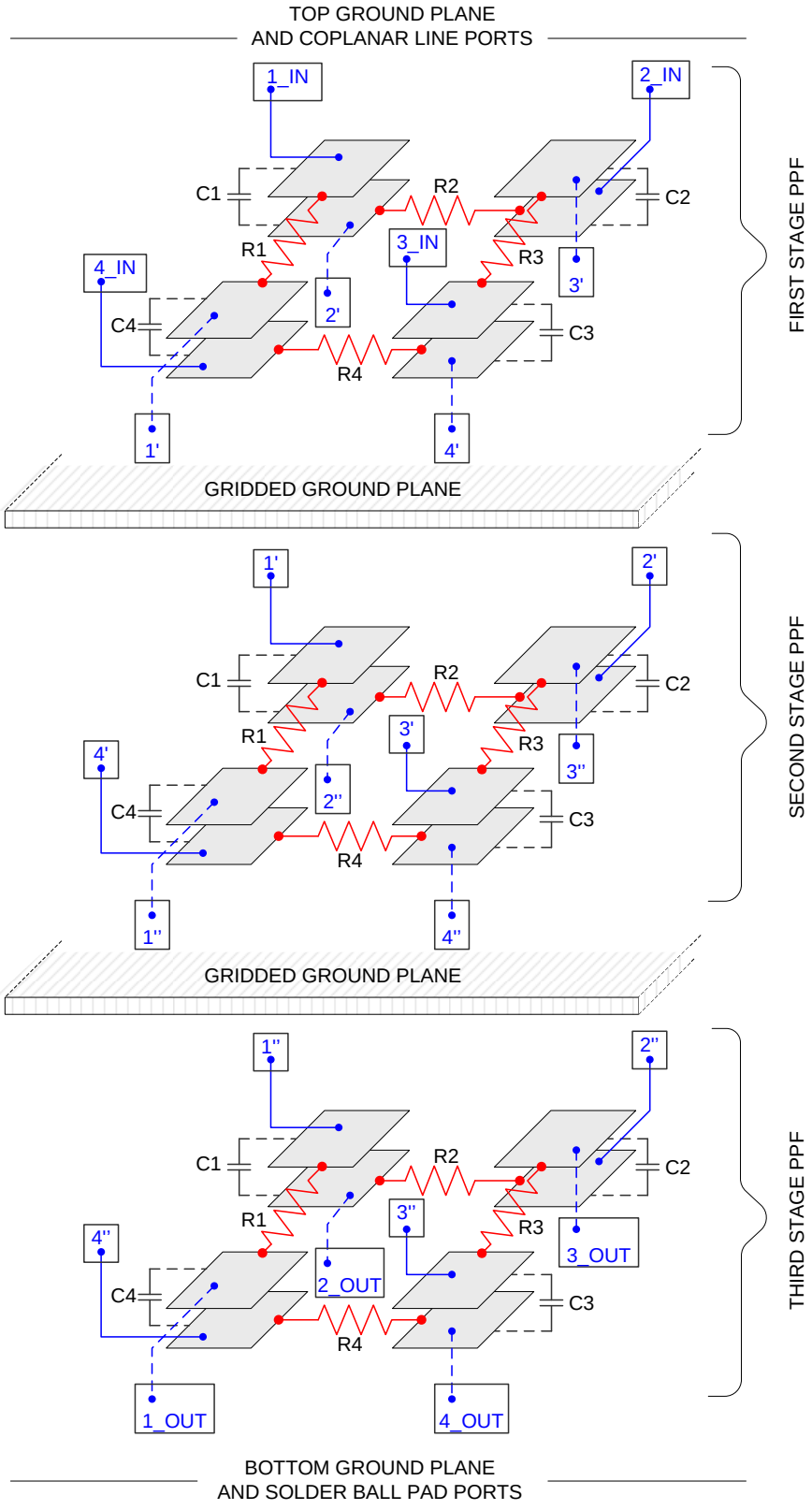


Figure 5.24: 3 Dimensional Component Distribution

Additional segments are added to the single segment structure one at a time and are then simulated and compared to the ideal circuit model response. The simulations involve several iterations to achieve acceptable results. A two segment structure is shown in figure 5.25. The spacing between the plates is $d = 0.185\,mm$. The thicknesses of $2d$ are achieved using two layers of $254\,um$ Ferro A6M tape. This is the unfired thickness of the tape. The corresponding approximate fired thickness which is also the simulation thickness is $2d = 0.370\,mm$.

Equal dimension vias with a diameter, $dia = 200\,\mu m$, are used for the entire circuit. This value was the largest acceptable value after consultation with the intended manufacturer. Ferro recommends different via diameters for different layer thickness and corresponding via-hole creation methods. These are summarised in the table below. The distance between a via and the edge of the substrate is denoted A.

Thickness	Via Diameter (µm)	A min (µm)	Recommended Punch Method
50.8 µm	$<$ 101.6	635	Punch
	101.6 - 127.0	508	Punch
	$>$127.0	508	Laser
127 µm	$<$ 101.6	635	Punch
	101.6 - 127.0	508	Punch
	$>$127.0	508	Laser
254 µm	$<$ 101.6	635	Punch
	101.6 - 127.0	508	Punch
	$>$127.0	508	Laser

When the required via length extends to more than two layers, the vias are staggered. The clearance between via catch pads and the ground plane must also conform to the recommendations from Ferro. A clearance of at least 508 µm is recommended on all sides.

The ground plane simulated in figure 5.25 is initially maintained as a solid ground plane for simplicity as is shown. Apart from gridding the ground plane, the edges - even those for the through allowances - should be castellated when possible. The point is to have an approximate ratio of the area covered by conductors to exposed tape area of about 1:1 to ensure good adhesion of the layers.

To try and maintain symmetry, the sections of the ground plane overlapping with the parallel plates are maintained as fully solid. However, this poses the challenge of insufficient exposed total area of the tape for proper adhesion during lamination. For this reason the tape area surrounding the structure is increased beyond the conductors to increase the surface area of exposed tape. This is done for the final design before sending it out for manufacturing.

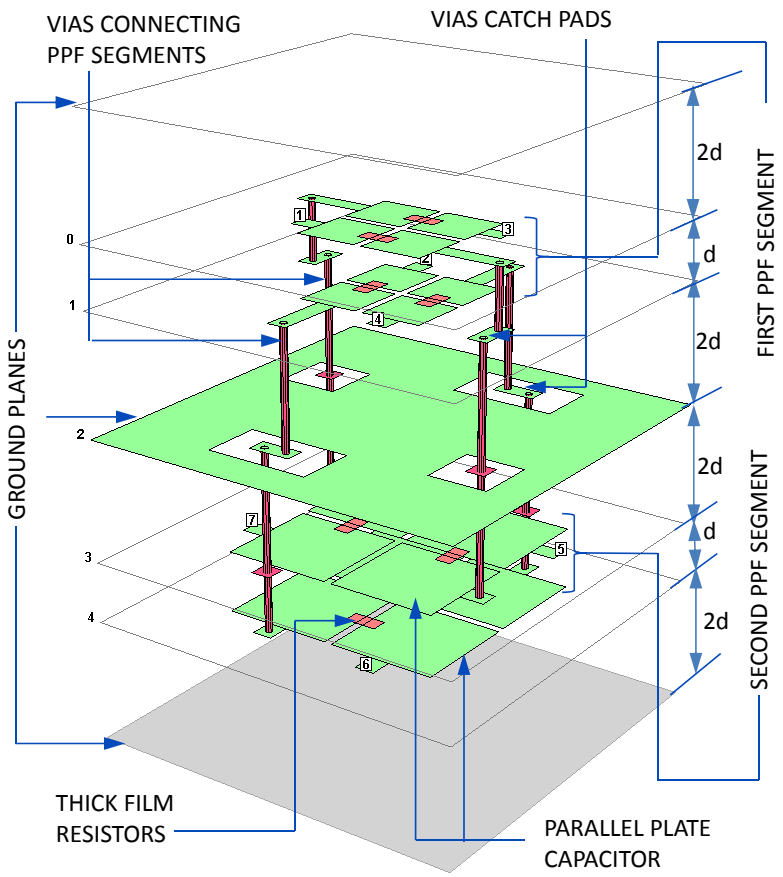


Figure 5.25: Two Segment Polyphase Filter in Sonnet

The Sonnet structure comprising all three segments is shown in figure 5.26. It has a total of ten metallic layers to be realised through screen printing with FX 30-025 as the gold paste.

RF vias with a diameter of 0.20 mm are distributed all around the edges of the structure to provide electromagnetic shielding. These are staggered from one layer to the next. They also connect the ground planes on all the layers to those on adjacent layers. Additionally,these vias achieve a self-packaging property for the resulting chip.

The resistors are to be screen printed after the conductors have been printed onto the green tape. These resistive elements occupy six layers out of the ten.

The transitions to the outer surface ports places four ports on the upper surface in the form of coplanar waveguide. The other four transition to the lower surface as conducting solder pads for solder balls that will attach the chip to a PCB layout for measurement. The top surface ports are also to be wire-bonded to an elevated PCB layout with the aim of using the shortest possible wires.

A total chip height of 2.777 mm is achieved for this design with a footprint of $1\,cm^2$, i.e $L = W = 1\,cm$.

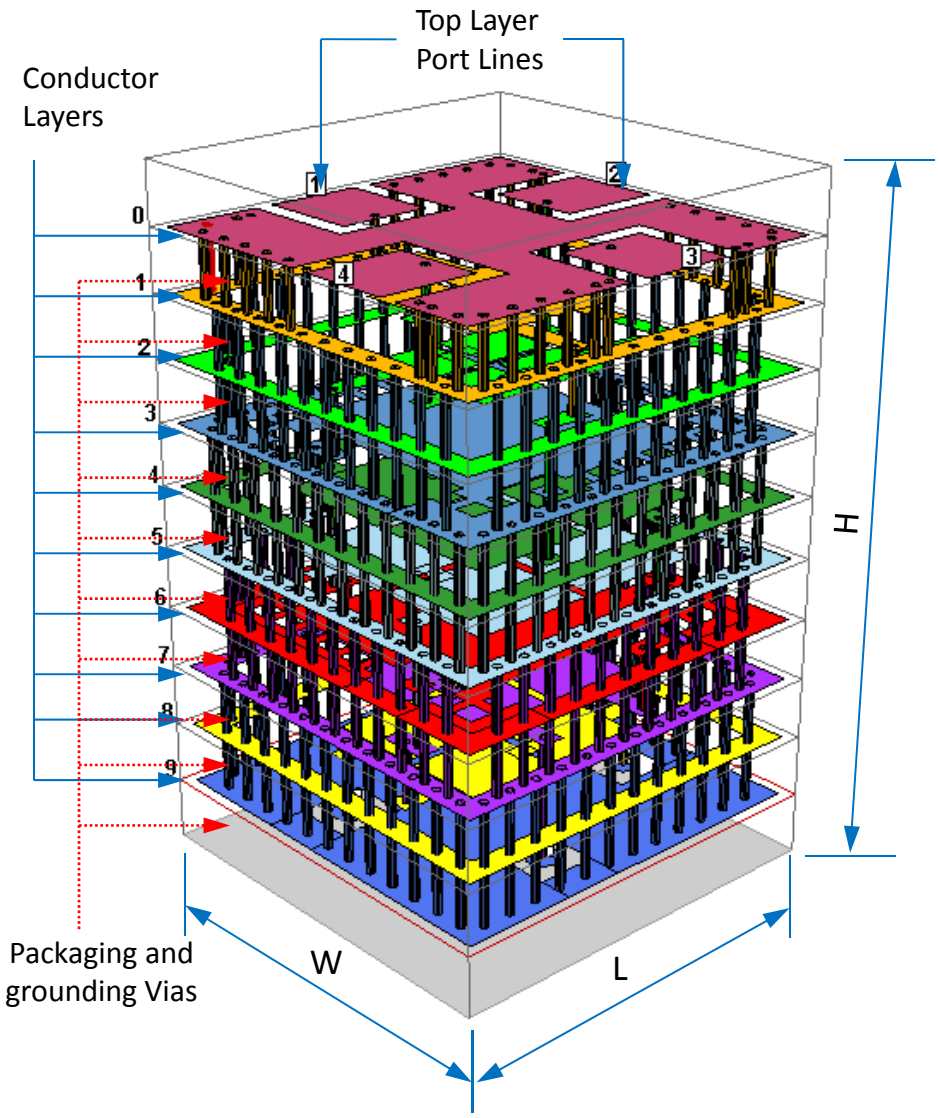


Figure 5.26: 3D Structure of 3-Segment LTCC Polyphase Filter

The conductor distribution on the different layers can be seen in figure 5.27 from the top layer labelled Layer 0 to the bottom layer labelled Layer 9.

The resulting simulation results are presented in figure 5.28. This implementation results in a maximum image suppression of approximately 35 dB across the desired frequency range of 100 MHz to 300 MHz. This is 6 dB lower than the 41 dB required in the specifications. However, one major aim of this project was to establish LTCC as a viable technology for the realisation of miniaturised polyphase filters. For this particular purpose, the obtained simulation results are acceptable and as part of future work, an additional stage can be added to obtain a larger image suppression.

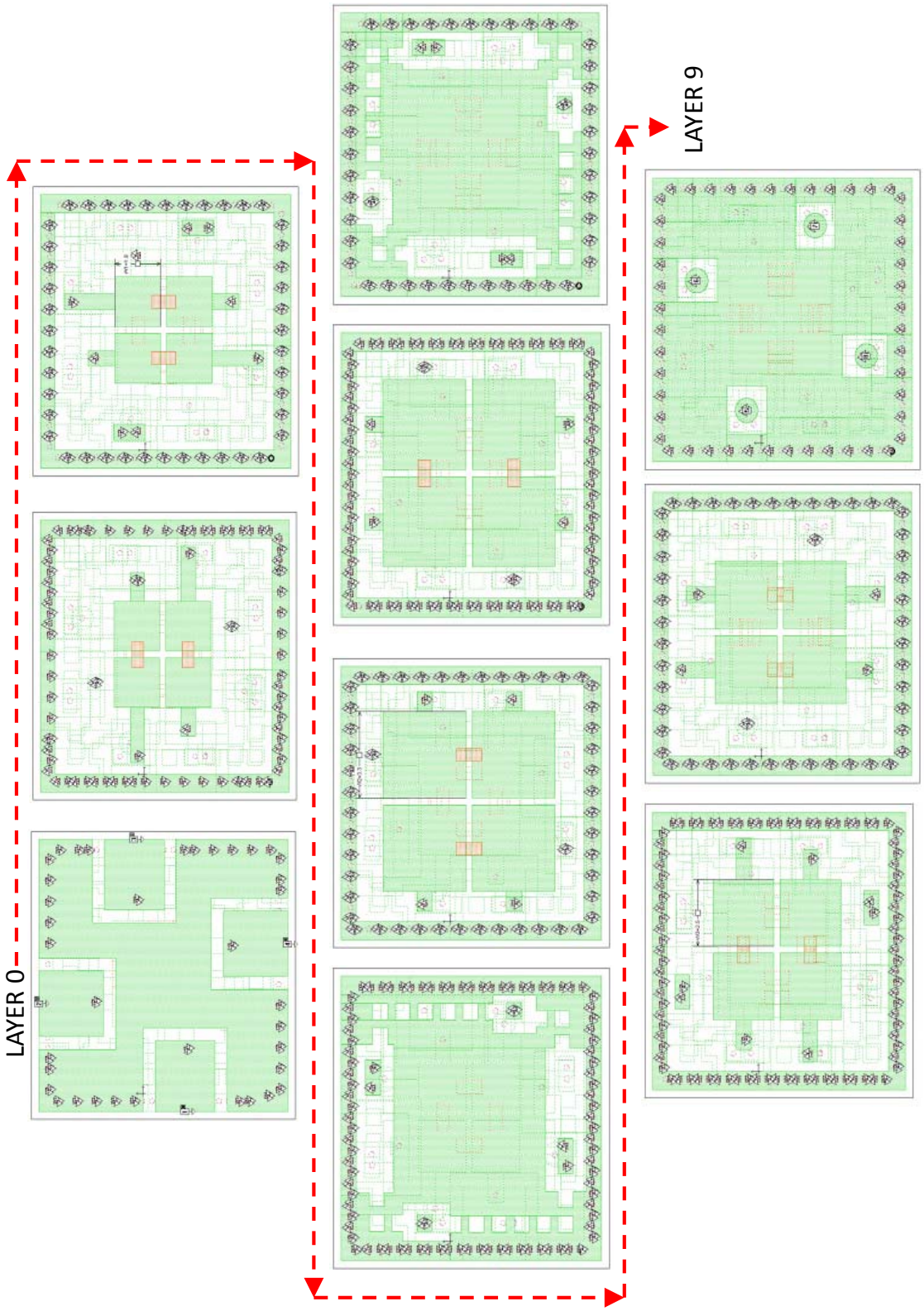
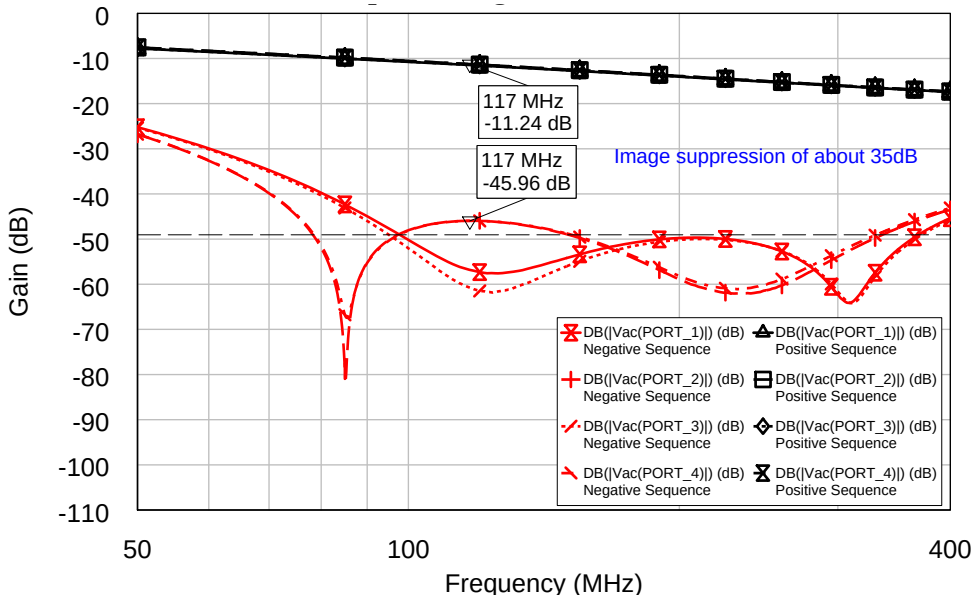
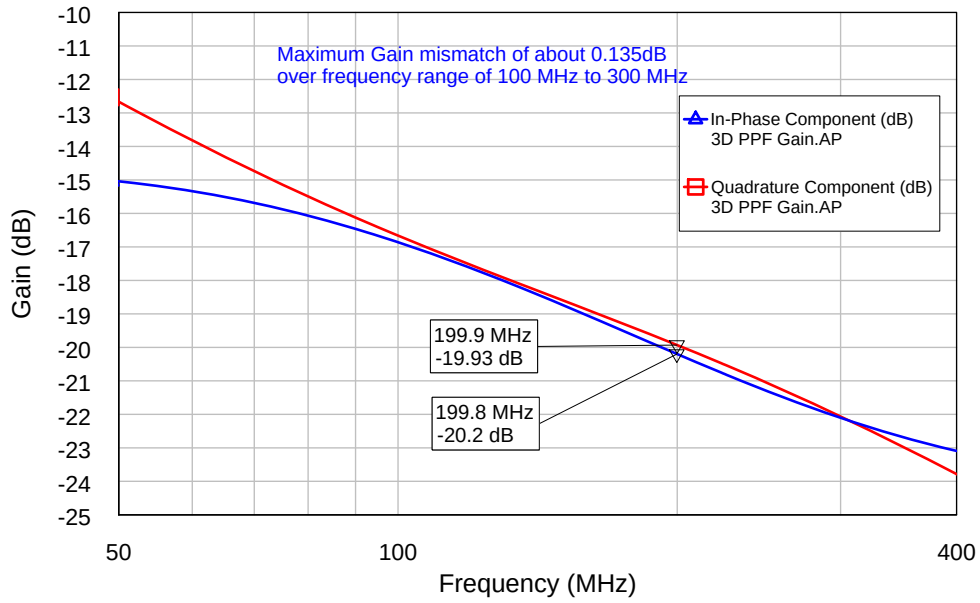


Figure 5.27: PPF Filter Layers



(a) Gain when Circuit is Driven in a Positive Sequence and a Negative Sequence



(b) Gain mismatch between Quadrature Outputs

Figure 5.28: Simulation Results of Three Dimensional Polyphase Filter Structure in figure 5.27

The bandwidth of the polyphase filter is also larger than that of the ideal three segment polyphase filter circuit simulation; the first unity gain frequency has been shifted to a lower frequency while the third unity gain frequency has been shifted to a higher frequency. The in-phase (port 1 and 3) and quadrature (port 2 and 4) outputs of the negative sequence are also seen not to overlap as would be ideal. It can also be noted that only two of the expected three unity gain frequencies are visible. These deviations from ideal can be attributed to component mismatches due to both the distribution of the components within the structure and the parasitic interference within the

structure.

A gain mismatch between the quadrature outputs of approximately 0.l4 dB is obtained. This is less that the 0.5 dB required as per the specifications and is therefore satisfactory.

5.7 Conclusion

This chapter presents the design of a 3-segment polyphase filter and analysed the results of its three dimensional structure implemented in low temperature co-fired ceramics. From a design point of view, it has been shown that a practical size of a polyphase filter is feasible and acceptable performance levels can be obtained with the designed structure.

From a manufacturing point of view, however, a design with several layers poses the challenge of being relatively expensive in its realisation. This specific design requires a total of 26 screens and stencils each of which must be loaded on a frame of its own. This corresponds to 26 individual screen printing runs, and follow-up individual drying stages. The process is also time consuming and requires skilled hands to achieve accuracy.

The above observations do not however rule out the viability of this substrate as a suitable choice. It can be recommended that for cost-efficiency, thinner substrates be used instead. This has the potential of either reducing the overall footprint by an appreciable factor while maintaining the same difficulties as the design presented in this chapter or, a nearly similar footprint can be achieved for a much smaller number of layers of a different layout. This is to be tested as part of future work.

Chapter 6

Passive PIN Diode Power Limiters and Switches

6.1 Introduction

Microwave and RF receivers and transceivers are often prone to damage occurring due to input power signals that have high amplitudes exceeding a certain threshold. To protect these sensitive front-end components against damage due to the high power signals, microwave limiters and switches have to be used. An example of such use can be seen in the simplified transceiver block diagram in figure 6.1.

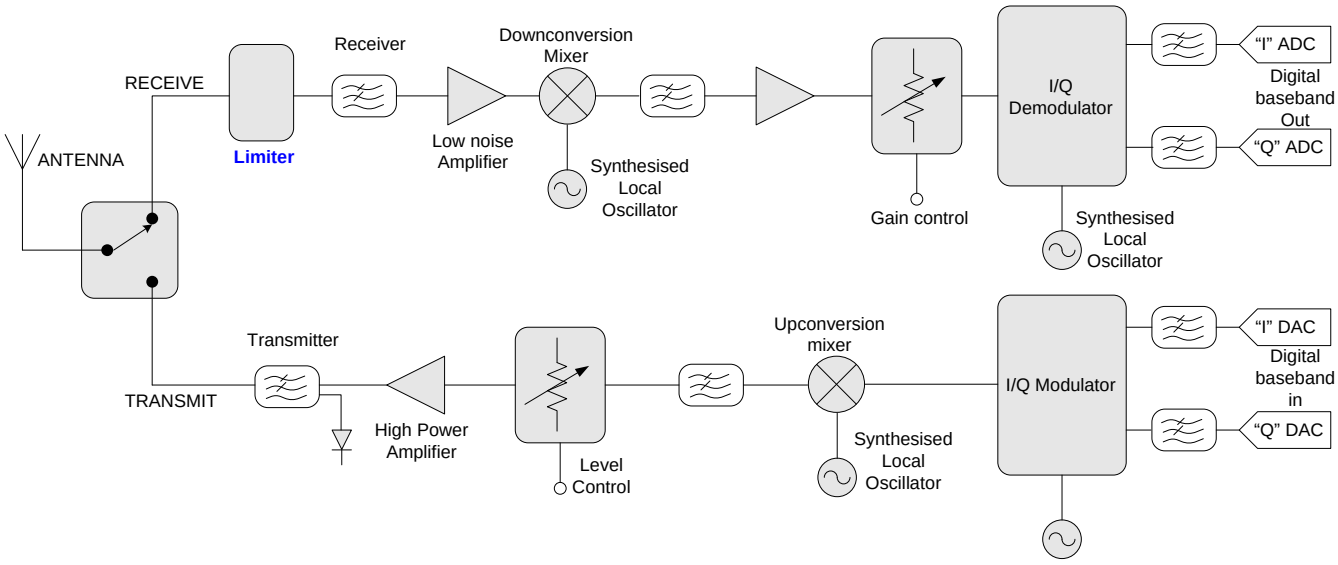


Figure 6.1: Simplified transceiver

While a switch is normally defined as a control circuit that utilises the flexible impedance control of PIN diodes to direct the flow of signals, a passive limiter is defined in [46] as a self-activating switch that is activated by a high-level incident power. It is a two-port network which passes low power signals but attenuates high power signals [85]. For both types of control circuits, PIN diodes act as the RF control element in the circuit.

In terms of construction, a PIN diode is similar to a standard diode, but has an additional layer, the intrinsic layer (I), between the P and N layers as shown in the simplified structure in figure 6.2.

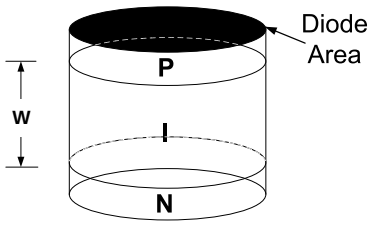


Figure 6.2: Simplified PIN diode structure

The diode characteristics and the amount of charge that is stored in the intrinsic layer determine the diode impedance to input RF and Microwave signals.

This chapter proposes the implementation of a PIN diode limiter circuit, that also integrates the functionality of a single pole single throw (SPST) switch, in LTCC substrate technology. For this reason, throughout the chapter, the circuit is referred to as PIN limiter-switch.

While PIN diode limiters have traditionally been implemented in waveguides, coaxial lines and planar, laminate circuit enviroments [35], LTCC offers many advantages for the implementation of PIN diode limiter circuits. Different advantages of LTCC have been outlined in chapter 2. It offers multilayer circuit capability and compact size in comparison to waveguides and coaxial lines. This means that passive components in a circuit can be embedded within different internal layers of a multilayer ensemble as buried components, while chip components like diodes can be surface mounted on the outer layers. LTCC substrates also offer low dissipation factor hence reducing dielectric associated loss. In addition to this, they can tolerate high temperatures making circuits implemented in the substrates suited for harsh temperature environments.

The advantage LTCC has over many laminate technologies which can also be built into multilayer circuits, is better thermal conductivity. Typically, during the limiting state of RF and microwave PIN diode limiters, power is reflected back to the input, but not all; some is dissipated in the diode due to heating produced by the RF signal voltage across the diode resistance. A surface mounted diode therefore requires a substrate material with good thermal conductivity to provide good heat sinking. LTCC also has the added advantage that thermal vias can be embedded in a circuit construction to provide additional high conductivity paths to a heat sink.

The chapter begins with a brief discussion on the PIN diode relevant to the designs to be presented. More detailed discussions on PIN diodes can be found in [85].

The section thereafter presents the theory of operation of passive PIN diode RF limiters, as well as a shunt single pole single throw switch. A set of specifications is then used to design an L-Band PIN limiter-switch. The circuit model of this is analysed in Agilent Technologies' ADS software. Following this is the description of the implementation and analysis of the physical structure, which is done in Sonnet.

6.2 Basic PIN Diode Theory

A PIN diode is a current-controlled device that operates as a variable resistor at RF and microwave frequencies. It is a semi-conductor diode in which a high-resistivity intrinsic region, I, is sandwiched between a p-type and an n-type region [36].

When the forward bias current of a PIN diode is varied continuously, the diode can be used for attenuation of signals, leveling and for amplitude modulation of RF signals. It can also be used for switching, pulse modulation and phase shifting of RF signals if the control current is switched on and off in discrete steps. PIN diodes are ideal for use in miniature, broadband and RF signal control circuits owing to their small physical size relative to wavelength. They also have high switching speeds and low package parasitic reactances.

During the forward-bias state, holes from the P region and electrons from the N region are injected into the I-layer of the PIN diode. The charge does not recombine immediately; rather, the holes and electrons take a finite average time, called the carrier lifetime (τ) before the recombination. This charge acts as a conducting element with a resistance that varies with the diode current. When the PIN diode is reverse-biased (zero-bias), there is no charge stored in the I-region and the diode acts like a large capacitor (C_T) in parallel with a resistor (R_P).

The performance characteristics of a PIN diode are dependent on the chip geometry and the semi-conductor material in the intrinsic layer.

Typical parameters usually specified for PIN diodes are shown in table 6.1.

Parameter	**Description**	**Units**
R_S	Series resistance under forward bias	Ω
C_T	Total capacitance at zero bias or reverse bias	pF
R_P	Parallel resistance at zero bias	Ω
V_R	Maximum Dc reverse bias voltage	V
τ	Carrier lifetime	ns
ϑ_{JC}	CW thermal resistance	^{0}C/W
ϑ_P	Peak Thermal Resistance	^{0}C/W
P_D	CW power dissipation	W
I_F	Forward Current	A
W	I region thickness	μm

Table 6.1: Typical Specified PIN Diode Parameters

6.2.1 Electrical Models of PIN Diodes

Accurate time-domain modelling of RF and microwave designs that use PIN diodes requires accurate Spice models for the PIN diodes. In recent years, a number of PIN diode models have been developed that predict the forward bias and reverse bias characteristics of the PIN diode. These adequately model important characteristics such as I-region charge storage and junction effects. In [28], Caverly et. al. present a time domain simulation model for the PIN diode that includes both junction effects as well as low and high frequency I-region storage and current-dependent lifetime effects. To verify the model, they use a commercial version of SPICE as well as a full one dimensional semiconductor device simulator to compare the resistive and reactive impedance components to those obtained using analytical models. The carrier lifetime measurements are also compared with Spice models and are shown to have good agreement.

Circuit simulators such as AWR Microwave Office and Agilent ADS have since included PIN diode elements based on the Caverly model in their element libraries and strongly recommend the use of this advanced model in all types of PIN diode circuit designs. The equivalent circuits for the PIN diodes for the two simulation packages differ only slightly, with the ADS model including a shunt resistor in parallel with the junction capacitor C_j(sometimes C_T) as seen in figure 6.3.

The parameters in the model are defined as follows:

- I_s is the saturation current or reverse saturation current
- *Lbond* is the package parasitic inductance
- *Cpkg/Cpack* is the package parasitic capacitance
- *Rlim* is the minimum series resistance
- *Repi* is the zero-bias resistance/epi leakage resistance
- *Cj* is the zero-bias capacitance/reverse capacitance
- R_p is the junction parallel resistance.

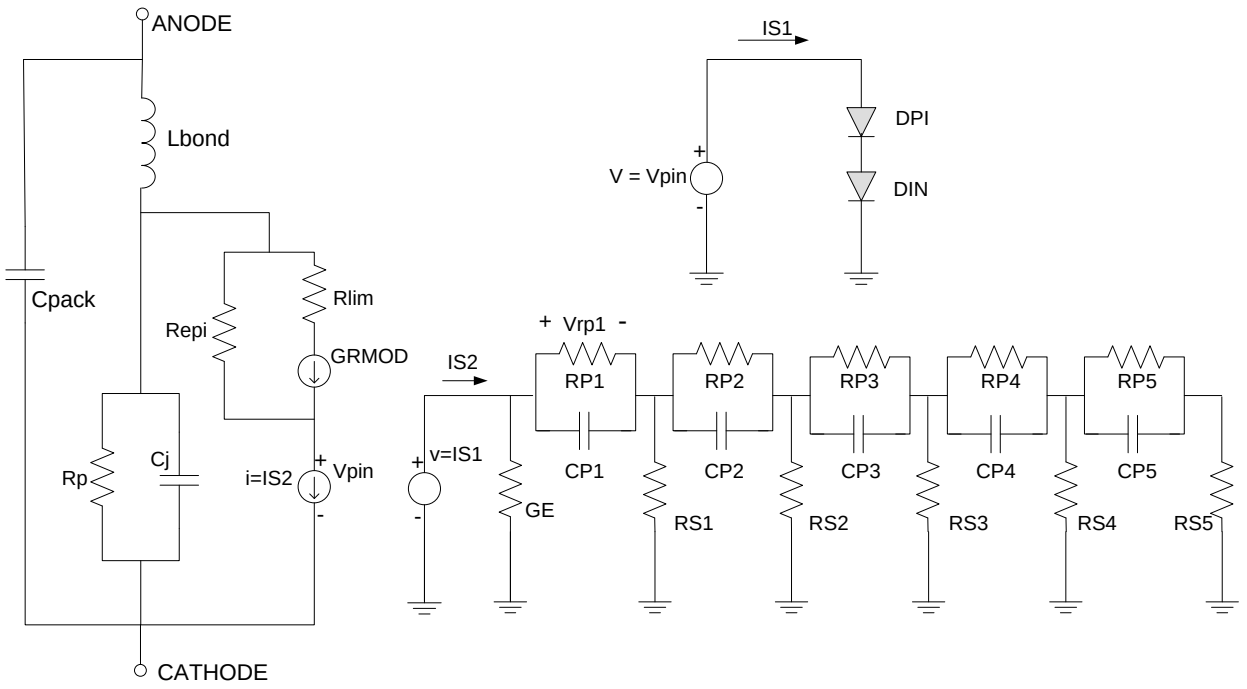


Figure 6.3: ADS Equivalent Circuit Model of a PIN Diode

While time-domain models are necessary to simulate transient PIN diode behaviour, in many cases only the steady-state models are required.

To characterise the steady-state PIN diode behaviour when in either the ON-state or the OFF-state, two models, the forward bias model and the reverse bias model, can be derived from the main equivalent model in figure 6.3.

Forward Bias Model

The series resistance under forward bias, seen in figure 6.4a can be defined as [36]

$$R_S = \frac{W^2}{(\mu_n + \mu_p)\, Q} \quad (Ohms) \tag{6.1}$$

where:

Rs = RF series resistance (Ω)

Q = DC stored charge = $I_F \times \tau$ (C)

W = I layer thickness (m)

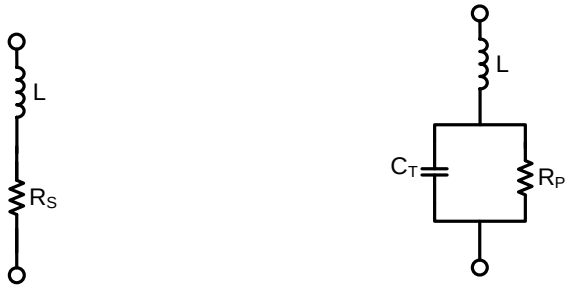
I_F= DC forward bias current (A)

μ_n= Electron mobility $[m^2/(V \times s)]$

μ_p= Electron mobility $[m^2/(V \times s)]$

It is important to note that this equation is only valid at frequencies higher than the I region transit time frequency, $f > \frac{1300}{W^2}$ (where frequency is in MHz and W is in µm) [36]. The parasitic

resistance of the diode package in a practical diode, and the contacts of the diode, limit the minimum resistance value.



(a) Forward Bias Equivalent Circuit (b) Reverse Bias Equivalent Circuit

Figure 6.4: Forward and Reverse Bias Equivalent Circuits

The lowest total impedance also includes the parasitic inductance, but this inductance value is typically less than 1nH.

Reverse Bias Model

From [36] the total parallel capacitance C_T(also C_j in some books) can be computed as

$$C_T = \frac{\varepsilon A}{W} \tag{6.2}$$

where:
C_T = Total capacitance (F)
ε = Dielectric constant = $\varepsilon_R + \varepsilon_0$
A = Diode area (m^2)
W = Thickness of the depletion layer $\approx$ thickness of the I layer (m)

The validity of this equation only holds for frequencies above the dielectric relaxation frequency of the I region, that is $f > \frac{1}{2\pi\rho\varepsilon}$ [36], with ρ as the resistivity of the I region. Equation 6.2 is also only valid at frequencies higher than the I region transit time, $f > \frac{1300}{W^2}$ (where frequency is in MHz and W is in μm) [36].The value of the parallel resistance R_P is proportional to the voltage and inversely proportional to the frequency. In most RF and microwave applications, the value is significantly larger than the reactance of the parallel capacitance, C_T, and therefore does not affect the total impedance resulting from the two significantly. It is also assumed that the diode is operated under small signal conditions so that the RF signal does not affect the stored charge. Otherwise, equation 6.2 would not be valid.

6.2.2 Switching Speed

A PIN diode can be switched from the conducting state to the non-conducting state and vice versa, each of these transitions having its own switching speed. The transition speed from conducting to non-conducting (T_{FR}) is typically slower than that from non-conducting to conducting (T_{RF}) [36]. The switching speed during the transition from forward bias to reverse bias, T_{FR}, can be computed using equation 6.3 [36] and is illustrated in figure 6.5.

$$T_{FR} = \tau \ln\left(1 + \frac{I_F}{I_R}\right) \tag{6.3}$$

and is illustrated in figure 6.5.

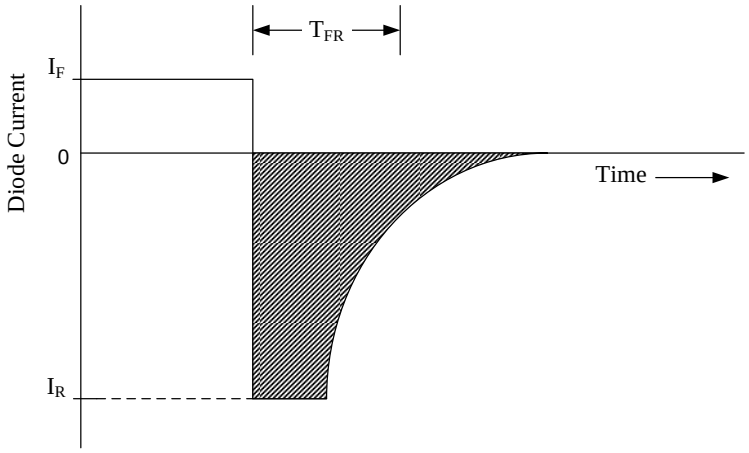


Figure 6.5: Diode Current vs Time

It can be seen that, if the carrier lifetime of the diode (τ) is constant, the transition speed is dependent only on the ratio of the forward bias current to the peak reverse current (for relatively small magnitudes of forward current). This reverse current is composed of charge carriers that were previously injected into and stored in the I layer during the forward bias state; it is not a leakage current or the diode reverse saturation current [36]. It then follows that the switching time during the reverse bias to forward bias transition, T_{RF}, is primarily dependent on the I region width of the PIN diode.

6.2.3 Thermal Model

For high power applications of PIN diodes, knowledge of the diode's thermal properties is important since the two distinct regions of the PIN diode (junctions and conductivity-modulated I region) are governed by temperature dependent parameters such as carrier mobility and carrier lifetime [29]. For such applications, the diode is expected to operate over a wide range of temperatures due to both ambient conditions and self-heating. The PIN diode thermal properties influence its operational factors such as the forward bias and reverse bias impedances and the DC bias current at fixed DC

voltage [29]. This in turn influences insertion loss, attenuation and the isolation.

PIN diode manufacturers usually provide values of the diode parameters typically measured at room temperature. They also provide the minimum and maximum ratings to provide designers with an idea of temperature limits beyond which the operation of a device using the specific diode is not reliable and is susceptible to damage. Time domain circuit simulators such as *Microwave Office* and *ADS* have the ability to simulate complex circuits comprising PIN diodes. However, they are unable to model dynamic variations in the temperature of the device and as a result, they do not accurately predict the device behaviour, potentially resulting in serious discrepancies between modelled and measured circuit performance. It becomes important then for an RF and microwave engineer designing for high power applications to obtain a thermal model that can be used in SPICE-like circuit simulators.

In [29], a novel electrothermal model is presented that builds on previously available time domain models and adds to those a thermal component that uses parameters easily obtained from manufacturer's datasheets such as thermal resistance, operating temperature, case temperature and the temperature at which the device parameters were established.

Thermal Resistance, ϑ, is defined as the ratio of the steady state temperature (^{0}C) rise of the junction, ΔT, per watt of steady state power dissipation, P_D, within it i.e.

$$\theta = \frac{\triangle T}{P_D} \tag{6.4}$$

The PIN diode has limited capability of dissipating energy in chip form, and the value of thermal resistance is normally measured by mounting the chip diode on a metal base [85]. Thermal resistance measurements for diodes which are ultimately to be used in chip form can be evaluated only on a sample basis by mounting representative chips in suitable packages for the measurements [85]. The two more commonly used constructions of PIN diodes shown in 6.6 are planar construction and mesa construction. The Skyworks limiter diodes used in the design here, CLA4607 and CLA4608 are planar designs (in Skyworks die package 149-815 shown in figure 6.6a) designated for high-power and mid-range applications and are available in basic chip form or encapsulated in Skyworks hermetic ceramic packages. Planar constructed PIN diodes have the advantage of having lower series resistance while conducting and when fairly large levels of power dissipation are involved, planar designs are better adapted to mounting on a heat sink [75].

Thermal resistance, ϑ, can also be defined as the ratio of the minimum thermal time constant, τ_T, to the I region heat capacity, HC [85].

$$\theta = \frac{\tau_T}{HC} \tag{6.5}$$

The I region heat capacity, HC, is defined as the amount of energy required for a unit increase (1^0C) in the I region temperature in the absence of heat flow from the diode [85]. In other words, it is a measure of the amount of heat which can be absorbed by the diode during operation at very short pulses that result in little heat flowing out of the diode into the heat sink during the length

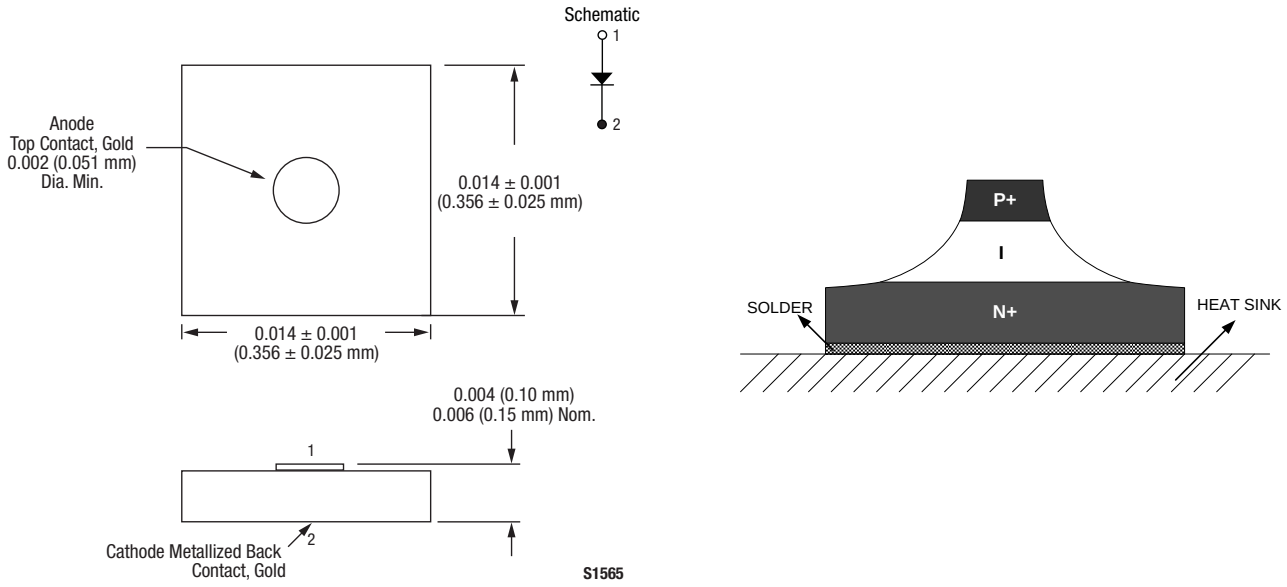
of the pulse. This can be calculated as a product of the specific heat and density of silicon and the volume of the equivalent I region cylinder, $V_{Iregion}$ [85]

$$HC = (Specific\ heat\ \times\ density)_{silicon} \cdot V_{Iregion} \tag{6.6}$$

or in an alternative form (comprising data readily available in PIN diode data sheets) as [85]

$$HC = \frac{(1.4D^2W)}{cubic\ centimeter} \quad (joules/^0Celcius) \tag{6.7}$$

D is the effective I region diameter and W is the I region width. The CLA4607 has a top contact diameter of 0.089 mm and an I region width of 7 µm. The CLA4608 other the other hand has a top contact diameter of 0.19 mm and also an I region width of 7 µm. Using equation 6.7, the respective heat capacities are 0.078 $\mu J/^0C$ and 0.354 $\mu J/^0C$. For a temperature rise of no more than 1^0C, these PIN diodes can absorb 0.078 Watts and 0.354 Watts of heat dissipation respectively for 1 µs.



(a) Planar Construction (Skyworks 149-815 die package) [77] (b) Mesa Construction

Figure 6.6: Types of PIN Diode Structures

From the I region heat capacity calculated in this way, the maximum I region temperature rise, ΔT_M can be computed and is limited to [85]

$$\Delta T_M < P_D \cdot t/HC \tag{6.8}$$

P_D is the pulse power dissipation within the I region and t is the pulse length. This equation refers to the temperature rise during each short pulse length with the assumption that the heat from previous pulses has been dissipated. Given that the heat in the PIN diode is not all developed in the I region and the heat dissipated in the I region is not really equally distributed [85],the use of

junction temperature T_J as the peak junction temperature is an approximation of the actual value which could be somewhat higher.

Two models have been seen so far that define the maximum temperature rise, ΔT_M ; the first, derived from equation 6.4, defines the steady-state maximum beyond which pulses with longer lengths do not have an effect on the temperature rise. The second model, for shorter pulses, is based on equation 6.8 and holds until the steady-state temperature rise is reached. The pulse length, t, obtained from substituting the steady-state power dissipated (given in the datasheet) and the maximum temperature rise calculated from equation 6.4 is the length of pulse that results in the steady state. Table 6.2 below shows the estimated shortest pulse length that results in maximum temperature rise, based on values obtained from Skyworks datasheets.

Diode	**Maximum Power Dissipation, P_D (W)**	**Thermal resistance $\vartheta_{JC}(^0C/W)$**	**Pulse length, t (μs)**
CLA4608	2	29	$0 < t < 10.266$
CLA4607	3	54	$0 < t < 4.212$

Table 6.2: Calculated Pulse Length for Maximum Temperature Rise

This situation, for both diodes is presented in figure 6.7.

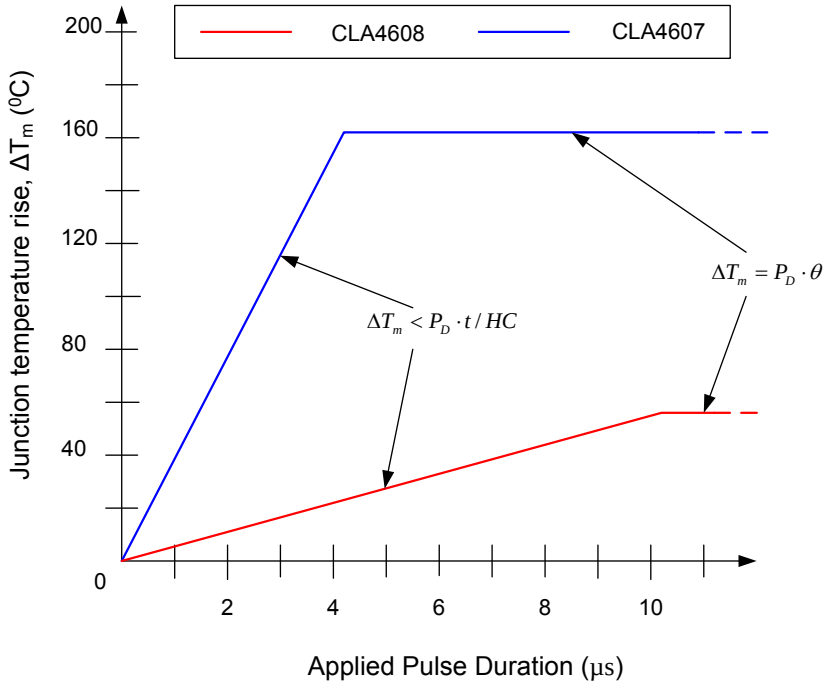
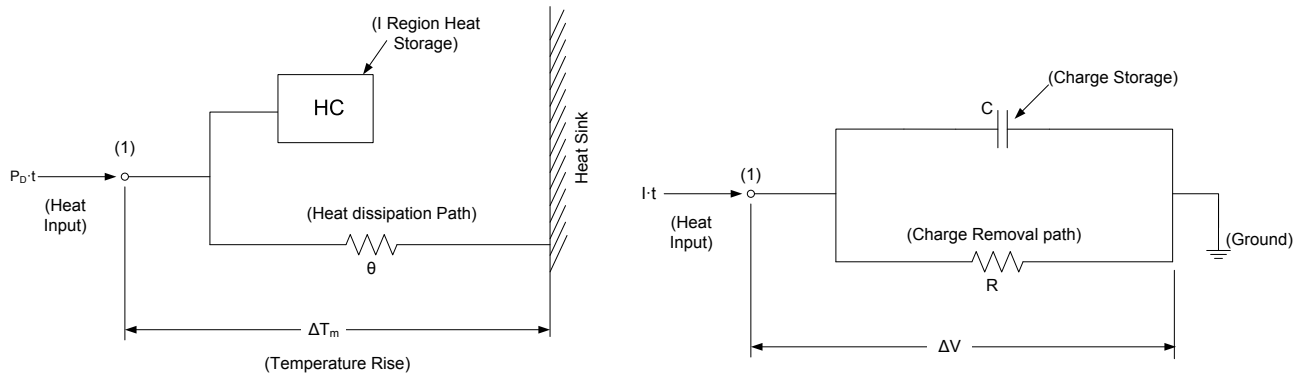


Figure 6.7: CLA4608 and CLA4607 Diode Temperature Rise Estimated using ϑ and Heat Capacity for $P_D = 2\,W$ and $P_D = 3\,W$ respectively.

The Skyworks datasheets describe the maximum temperature rise as the difference between the maximum junction temperature, T_J, and the case temperature. The maximum junction temperature is given as 175^0C and the maximum operating temperature as 150^0C for both diodes. the datasheets also explicitly state that performance is not guaranteed over the full operating or storage temperature ranges stated. Figure 6.7 suggests a linear rate of increase of junction temperature with time change which is not a very realistic approximation. White [85] considers a simplified diode thermal model (see figure 6.8a), nearly similar to that in [29, 30] to estimate a more realistic contour.



(a) Simplified Diode Thermal Model

(b) Analogous Electric Circuit Model

Figure 6.8: Simplified Thermal and Electric Models for Transient Diode Heating

Temperature rise due to dissipated power causes heat flow out of the I region through the thermal resistance path labelled ϑ. The instantaneous heat flow input at node 1 is a sum of the change in heat stored, $HC \cdot \frac{d(\Delta T_M)}{dt}$ and the heat lost $\frac{\Delta T_M}{\theta}$ in the thermal path to the heat sink i.e.

$$P_D = HC \cdot \frac{d(\Delta T_M)}{dt} + \frac{\Delta T_M}{\theta} \tag{6.9}$$

The electrical analogous model to this is defined by the equation

$$I = C\frac{d\,(\Delta V)}{dt} + \frac{\Delta V}{R} \tag{6.10}$$

and is shown in figure 6.8b. The heat produced due to the power dissipated (P_D.t) at temperature node (1) of the thermal model corresponds to the charge input I.t at the voltage node (1) of figure 6.8b. Similarly, the capacitor, C, corresponds to the heat storage HC and the resistor, R, is analogous to the thermal resistance, ϑ. It can also be seen from equations 6.9 and 6.10 that the voltage rise, ΔV, at node (1) of the electric analog model corresponds to the temperature rise, ΔT_M, in the thermal model. In [85], White derives the exponential form of the equation defining temperature rise based on a well known form for the voltage rise, ΔV, in the electric analog model. The equation takes the form

$$\Delta T_M = P_D \cdot \theta \left[1 - e^{-t/\tau_T}\right] \tag{6.11}$$

The importance of the minimum thermal time constant, τ_T, previously seen in equation 6.5, can now be appreciated in the plot shown in figure 6.9

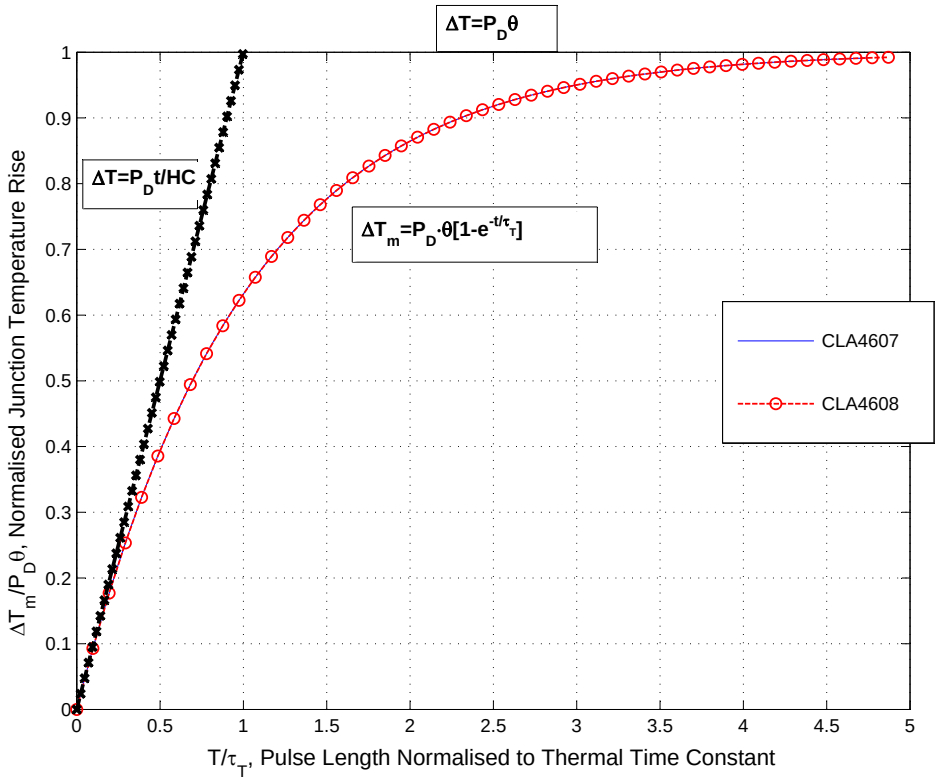


Figure 6.9: Temperature rise Profile of Pin diodes Using Minimum Time Constant Model

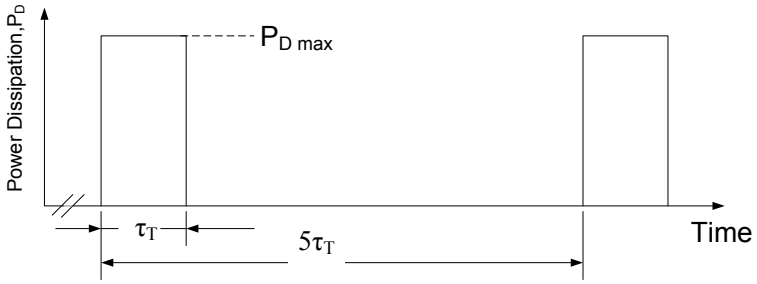
which shows a more realistic approximation to the maximum junction temperature profile previously given in figure 6.7. Since both the transient temperature rise and the pulse length have been normalised to the steady state temperature rise, $P_D\vartheta$ and the thermal time constant respectively, the plot shows a general profile that can be applied to any diode. The CLA407 and CLA4608 plots therefore overlap but have different individual denormalised data sets.

White [85] explains that for a train of pulses incident upon the diode, if the pulse width is approximately equal to or less than the diode's thermal time constant, and if the period between pulses is more than five times the thermal time constant, the junction temperature, T_J, will cool down between the pulses to the temperature of the heat sink, T_A(within 1% of ΔT_M). Figure 6.10 shows a sample temperature characteristic with a pulse train with pulses of length τ_T and an inter-pulse period of $5\tau_T$. The diode temperature following the heating pulse decays exponentially with a time constant, τ_T. This relates to the maximum temperature rise ΔT_M and the temperature of the heat sink, T_A, by [85]

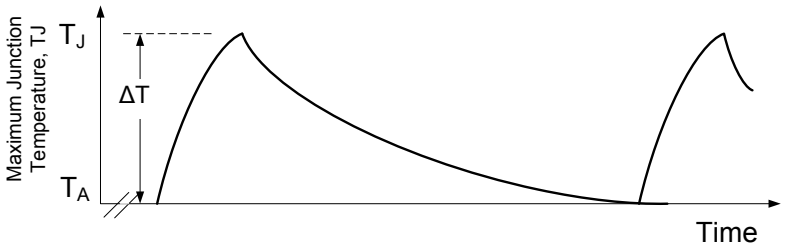
$$T_J = T_S + \Delta T_M e^{-t/\tau_T} \tag{6.12}$$

The thermal models discussed are important for designs that include PIN diodes and estimate

the temperature bounds within which the design can survive thermal stresses. It is important to note though that the actual junction temperature of a PIN diode is likely to be less than that approximated using equation 6.12.



(a) Power Dissipation



(b) Junction Temperature

Figure 6.10: Power Dissipation and Junction Temperature vs Time

6.2.4 Diode Packaging

PIN diodes come in a variety of packages, configurations of which are dependent on the requirements of the end application. Skyworks Limiting diodes are available in plastic Surface Mount Technology (SMT) packages as well as Ceramic-Metal Packages. The Skyworks CLA series limiting diodes used for the designs here (CLA4607-085LF and CLA4608-085LF) are surface-mount diodes designed in a quad flat no-leads (QFN) package. Plastic SMTs have the advantage of being inexpensive and compatible with modern pick and place assembly techniques. This form of packaging minimises the parasitic reactances due to the package. These reactances tend to reduce the bandwidth over which the diodes can be used and can also affect the insertion loss and isolation of the diode. Plastic SMT packages also add some thermal resistance to the diode die resulting in a reduced power dissipation.

The QFN package for the CLA46XX-085LF diodes produces lower thermal resistance than other SMT packages and also reduces the effects of parasitic inductance of the anode bond wires.

Figure 6.11 is a cross-sectional view of CLA46XX-085LF diodes showing how the planar constructed diode die is mounted in the package.

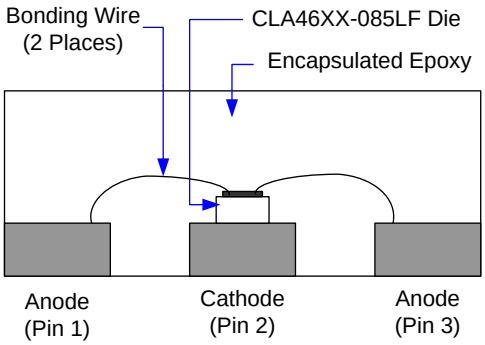


Figure 6.11: Cross-Sectional View of CLA46XX-085LF diodes

The cathode of the diode is soldered directly to the top of an exposed copper paddle labelled *Pin 2*. This copper paddle minimises the total thermal resistance between the I layer and the surface to which the diode package is mounted. In turn, the reduced thermal resistance between the I layer and the external environment minimises the junction temperature.

Figure 6.12 shows the CLA46XX-085LF QFN typical case markings (a), the electrically equivalent circuit (b) and the bottom view of the package showing the anode and cathode pads (c). Pins 1 and 3 of the 3-PIN QFN package are the anode pins and PIN 2 is the cathode pin and these correspond to pads 1,3 and 2 on the bottom view of the package respectively.

In the electrically equivalent circuit, the inductances of Pins 1 and 2 are in series with the input and output transmission lines of the external circuitry. This is also the case with the inductances of the bond wires. This is different from other configurations that usually have the inductances of the bond wires in series with the shunt PIN diode.

6.3 Passive RF Limiters

The function of limiters is to protect sensitive front-end components in RF receivers and transceivers from high level signals that might impinge on the receiver of transceiver. In an ideal situation, a limiting circuit would approximate a short circuit in the presence of a high power signal so that all incident power would be reflected back. Most limiter circuits employ the use of PIN diodes to achieve passive protection.

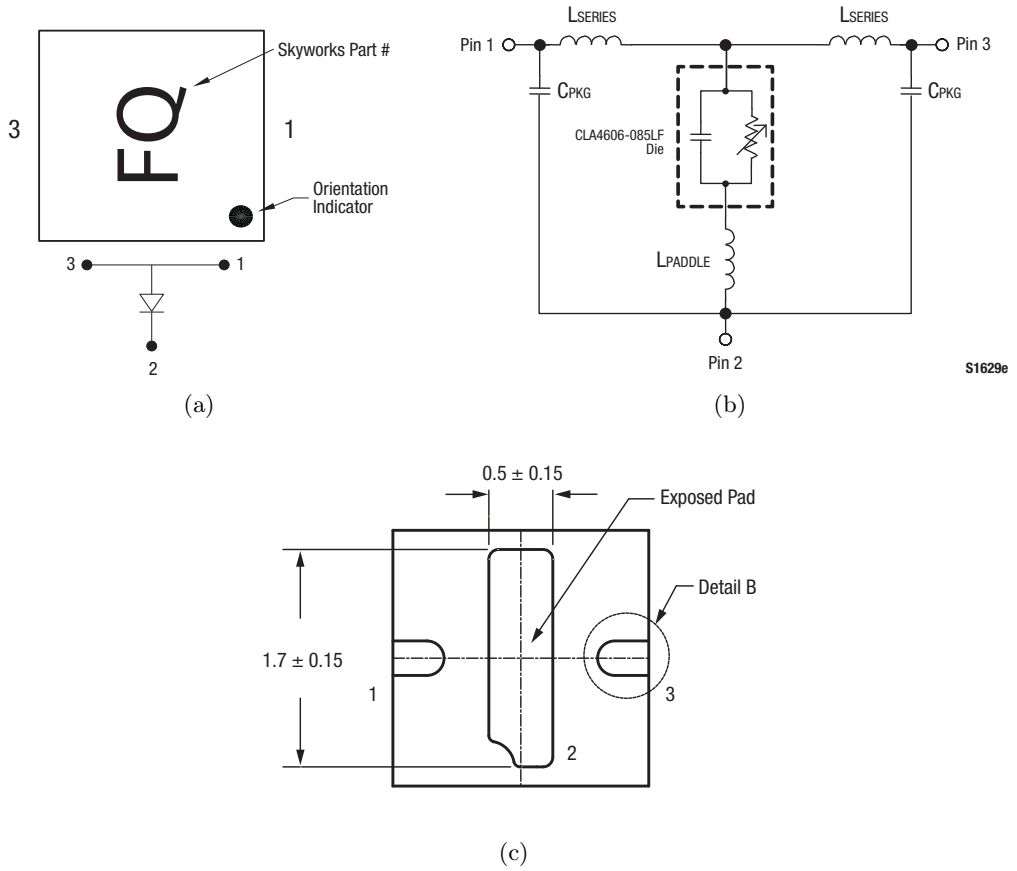


Figure 6.12: Skyworks CLA46XX-085LF QFN Package Drawings

A limiter should provide very low insertion loss to the desired input small signals so that the noise figure of the receiver remains as low as possible. However, for larger input signals with power levels that exceed the danger threshold, a limiter should provide very high losses. Such large signals tend to arise from a variety of sources such as jamming signals, the presence of other transmitters in the area and leakages between the transmit and receive channels of a transceiver. When a large signal is incident, a limiter needs to respond very fast (in the order of nano seconds) in order to provide fast protection against damage by the input signal. A properly designed limiter is self-activated and does not require any external bias signals. It must also survive the thermal stresses that it is exposed to due to the highest incident power after which it returns to the low-loss state.

Self-activation of a PIN diode results from the accumulation of charge over successive pulses. During forward bias of a PIN diode, positive and negative charge carriers are injected into the I-region and these are withdrawn during reverse bias. However, not all of the charge is withdrawn from the I region and after a few RF cycles of large enough signals, this results in an accumulation of charge in this region enabling conductivity. The holes and electrons in the I region continually undergo recombination. This recombination produces a dc current for which a return path must be provided in order for the limiter to function properly. Figure 6.13 shows a single stage passive

limiter with a single diode in shunt with an inductor which provides a dc return path.

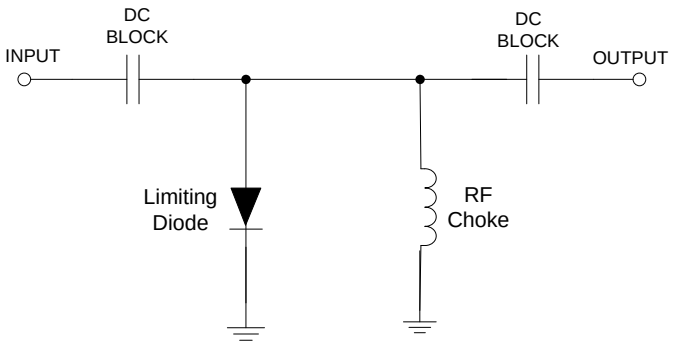
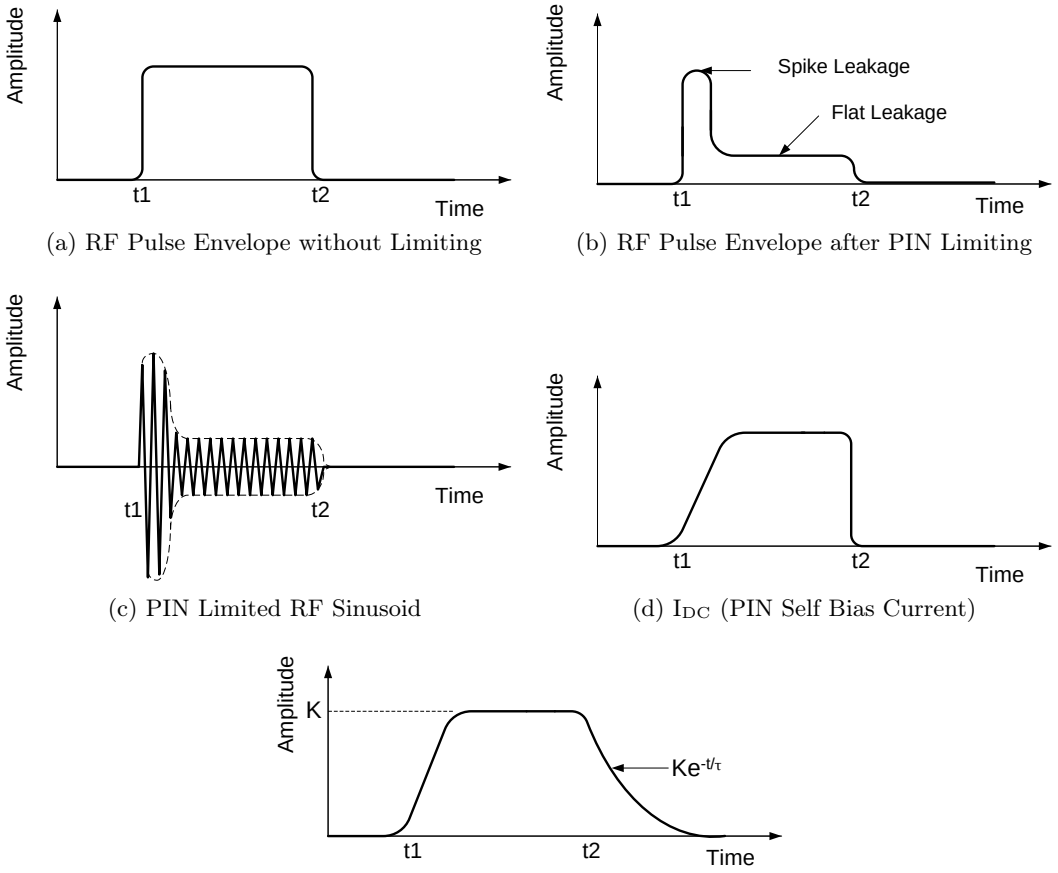


Figure 6.13: Single Stage Limiter Circuit

The limiter is quasi-linear in nature meaning, that the same limiting is provided to both the positive and the negative half cycles of the RF signal. During the time period in which charge is built up in the I-region, little limiting is provided by the PIN diode limiter, so that the high power RF signal passes through with little attenuation. The portion of the signal that passes through during this period is referred to as the spike leakage. When the I region starts conducting, a relatively high attenuation is achieved resulting in the flat leakage which is the threshold level above which limiting occurs.

Figure 6.14a and 6.14b show an RF envelope prior to limiting and after limiting. It is important to note that for every limiter design, a maximum input signal amplitude limit within which it can operate is defined. If a signal is too large and the choice of PIN diode is not such that the limiting process is fast, the device can be damaged. Figure 6.14c shows the quasi-linear modulation meaning that the diode presents substantially the same conductivity to both forward and reverse-going halves of the RF cycle [85].

The recombination process of the holes and electrons after the high power microwave signal follows an exponential curve with a time constant that equals the average carrier lifetime, τ. This is the recovery period during which the insertion loss of the limiter is very high and the receiver/transceiver components are more protected from incoming signals.



(a) RF Pulse Envelope without Limiting

(b) RF Pulse Envelope after PIN Limiting

(c) PIN Limited RF Sinusoid

(d) I_{DC} (PIN Self Bias Current)

(e) Average Carrier concentration in the I-region

Figure 6.14: Microwave Limiting due to Conductivity Modulation of PIN Diode

This recovery time is defined as the time required for the limiter's insertion loss to return to within 3 dB of its low level insertion loss following the cessation of the high power pulse [85].

In [24], Brown measures the recovery time of a single diode mounted in shunt with a $50\,\Omega$ transmission line as a function of peak incident RF power and pulse width. The plot, shown in figure 6.15, indicates that the diode recovery time is proportional to the peak power and to the pulse width.

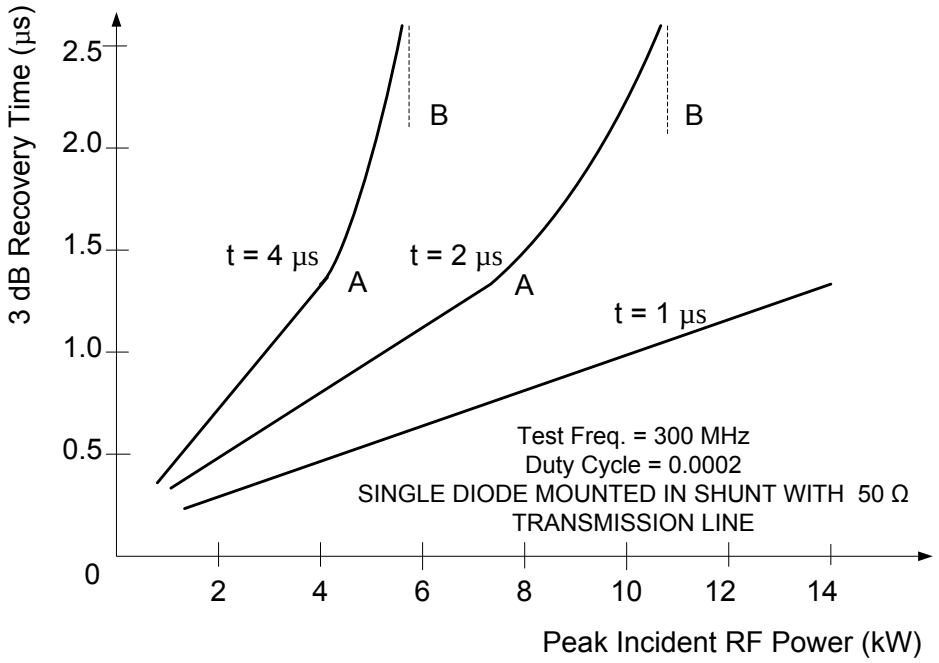


Figure 6.15: Recovery Time vs Peak Incident RF Power [24]

Point A indicates the stage at which the change in recovery time with peak incident RF power ceases to be linear. This change is considered to be due to excessive thermal heating of the diode. Beyond point A, the rate of increase in recovery time is faster until point B where the graph approaches a vertical curve. Point B is considered to be a point of catastrophic failure due to a runaway temperature condition [24].

The measurement of recovery time is important in monitoring the power handling capacity of a self-actuated PIN limiter. White [85] describes the measurement set-up as shown in the block diagram in figure 6.16. The recovery time measurement is performed by injecting a constant level, low power, microwave signal into the high power test set of figure 6.16.

Brown [24] also shows using equation 6.13 that for a maximum allowable junction capacitance, C_j,the heat capacity, HC, is proportional to the I region thickness, W, squared. This illustrates the need for thick I region thickness for maximum power handling.

$$HC = 11 C_j W^2 \quad watt - microseconds/^0C \tag{6.13}$$

However, at any given operating frequency there is a maximum usable I region width. The same applies when the I region width of diode is known; the maximum frequency at which it can be used can be determined.

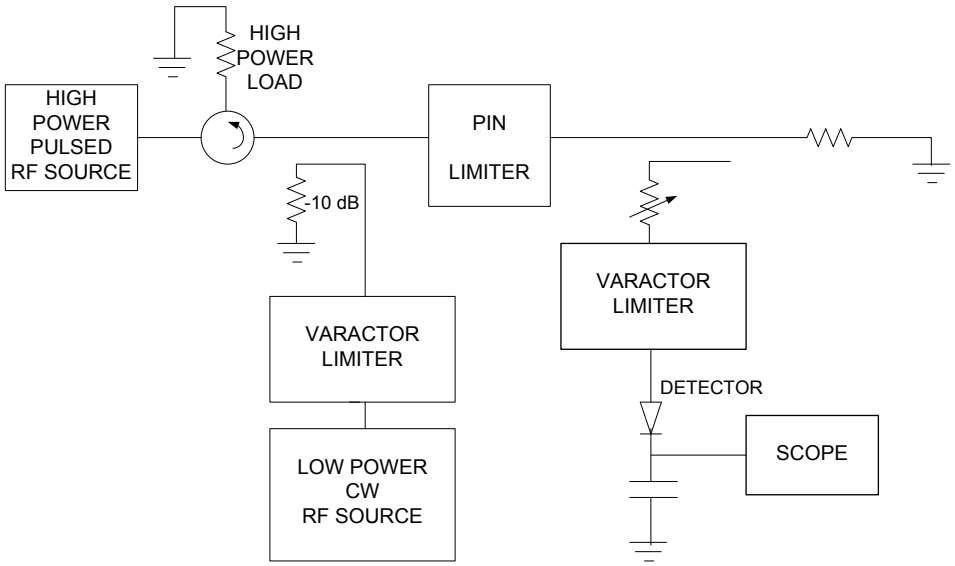


Figure 6.16: Measurement of PIN Limiter Recovery Time

Figure 6.17 shows data given for four diodes with I region widths of approximately 0.1 mils, 0.5 mils, 1 mil and 1.4 mils over a frequency range of up to 10 GHz. Both the Skyworks diodes used here (CLA4607-085LF and CLA4607-085LF) are designed for high power limiter applications over a frequency range of 10 MHz up to 6 GHz.

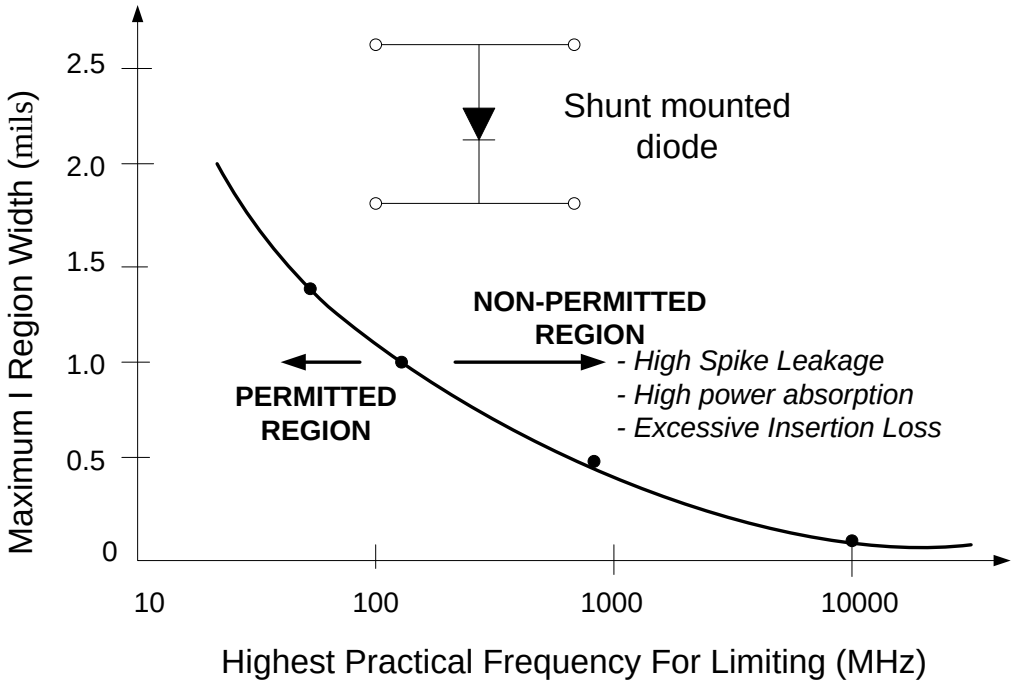


Figure 6.17: PIN Limiter Data Showing I Region Width vs. Highest Practical Frequency of Use [24]

Multi-stage Limiters

Practical limiters may be required to obtain a higher level of high power isolation than is achievable with a single stage PIN diode limiter. In such cases, a low power limiting stage (clean-up stage) can be added to the circuit separated by a 50 Ω quarter wavelength transmission line from the higher power limiting (coarse limiter) stage. This has the effect of broadening the receive bandwidth [24].

By adding additional diode stages in parallel each separated by a quarter wavelength transmission line from the next, it is possible to obtain current sharing hence enhancing the power handling capability of the limiter. The resulting power handling increase for a limiter with N shunt diodes varies directly with the power dissipation, P_D, of the diode, line impedance, Z_0, and the square of the number of diodes used, and inversely with the forward bias series resistance, R_S. This is given by[24]

$$P_{L_{SH}} = P_D \frac{N^2 Z_0}{4R_s} \tag{6.14}$$

The insertion loss resulting from the use of multiple diodes is proportional to the number of diodes and the line impedance and inversely proportional to the shunt capacitance, R_P, during the diodes' off-state, and is computed as [24]

$$Insertion\ Loss_{shunt} = N \frac{Z_0}{R_P} \tag{6.15}$$

The isolation that results from the use of multiple diode stages increases by a factor of N^2[24].

6.4 Passive Shunt Single Pole Single Throw (SPST) Switch

A simple untuned SPST switch can be designed using diodes in shunt to, or series with, the transmission line in the main signal path. For the purposes of the designs in this dissertation, a brief overview will be given of the shunt configuration only.

An SPST switch that employs a shunt PIN diode produces higher isolation values than one using a series connected diode across a wide range of frequencies. The diode is electrically and thermally grounded resulting in a design capable of handling more power because it is easier to heat sink. This configuration shown in figure 6.18 offers approximately 20 dB isolation [71].

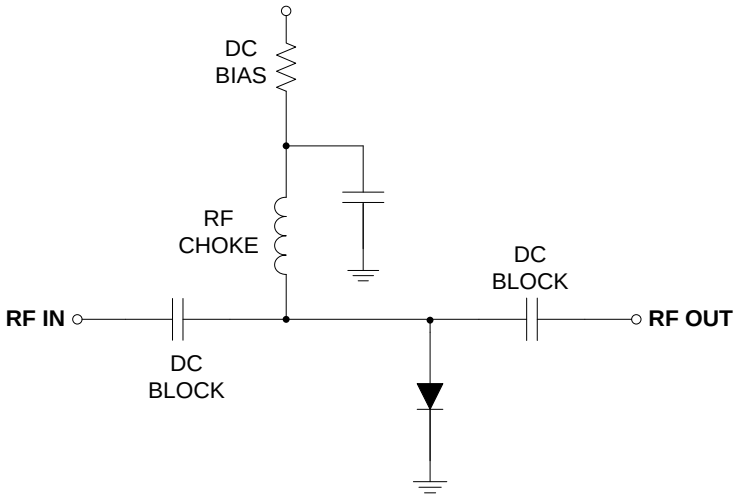


Figure 6.18: Shunt SPST Switch

The insertion loss of this switch is mainly dependent on the diode junction capacitance C_j and is given as [71]

$$IL = 10\log\left\{1 + (\pi f C_j Z_0)^2\right\} \quad dB \tag{6.16}$$

Z_0 is the line impedance of the transmission line to which the diode is connected. The forward bias power dissipation, P_D, and isolation are both functions of the forward bias series resistance of the diode and are computed as [71]

$$P_D = 4R_s Z_0 / \left(Z_0 + 2R_s\right)^2 P_{av} \quad Watts \tag{6.17}$$

$$Isolation = 20log\left\{1 + Z_0/2R_S\right\} \quad dB \tag{6.18}$$

where P_{av} is the maximum available power. The reverse bias power dissipation is related to the diode reverse bias shunt resistor, R_P, and the maximum average power, P_{av} , is given as [71]

$$P_D = \left\{Z_0/R_p\right\} P_{av} \quad Watts \tag{6.19}$$

Peak RF current, I_P, and peak RF voltage, V_P, are given by [71]

$$I_P = \sqrt{pP_{av}/Z_0} \quad amps \tag{6.20}$$

$$V_P = \sqrt{2Z_0 P_{av}} \quad Volts \tag{6.21}$$

In practice it is difficult to achieve high isolations with just a single diode. To overcome this, switches can be designed to use resonant structures and are then referred to as tuned switches. A

tuned switch (see figure 6.19) using shunt diodes is constructed by spacing two shunt diodes placed one quarter wavelength apart from each other. In the absence of a DC bias, this configuration can also operate as a two stage limiter.

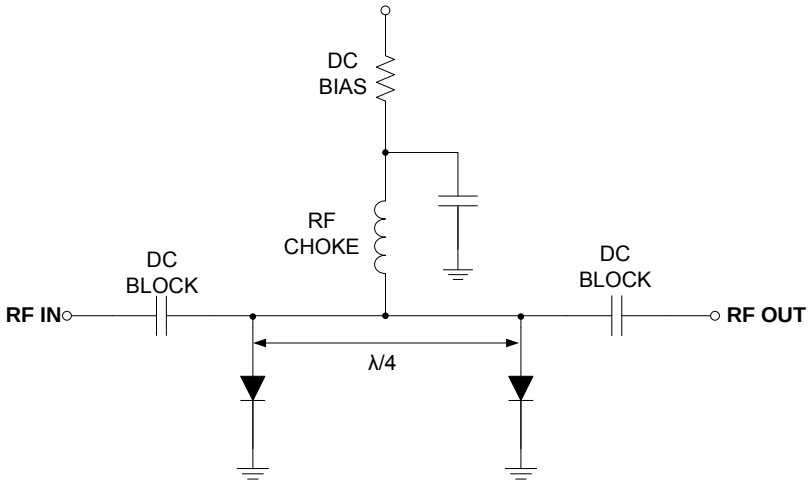


Figure 6.19: Tuned Shunt Switch

The insertion loss of this configuration may be lower than that obtained from a single diode shunt SPST because of a resonant effect of the spaced diode capacitances [78]. Tuned circuit techniques are mostly effective in applications having bandwidths in the order of 10 percent of the center frequency [78].

6.5 L-Band Passive Limiter-Switch Circuit Design

To test the viability of LTCC as a multilayer substrate option for the design of operational limiters and switches with desirable performance, a circuit is designed for the specifications shown in table 6.3.

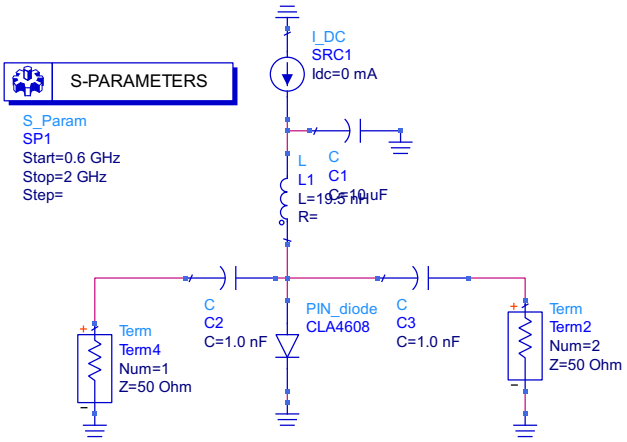
Center Frequency (GHz)	1.3
Operational Bandwidth (MHz)	200
Flat Leakage Power (dBm)	15
Maximum Input Power (dBm)	45
Rise Time (ns)	50
Insertion Loss (dB) @ Center Frequency	0.5

Table 6.3: Specifications for Limiter-Switch Design

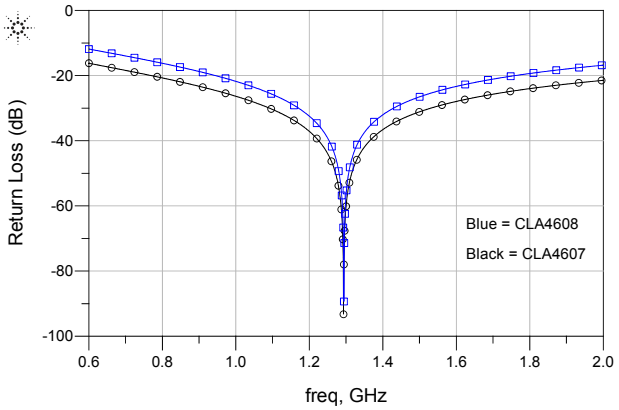
Initially a single stage limiter-switch in a setup shown in figure 6.20a is tested using different diodes to observe how much the output power can be reduced if a 45 dBm input signal is applied.

The topology in figure 6.20a also includes a DC current source to apply a DC bias signal when the circuit is to be used as a switch instead of as a self-biasing power limiter.

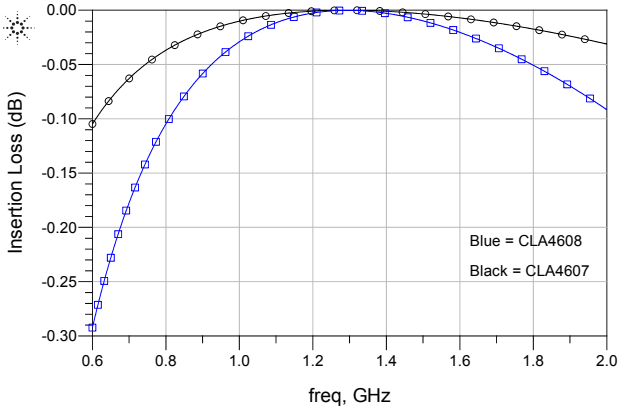
Using this setup, both an S-parameter analysis and a transient analysis are performed for circuits using two skyworks diodes, a CLA4608 and a CLA4607. In figure 6.20, S-parameters of the circuit are shown and compared for the two diodes with the inductor in the DC return path chosen to obtain a resonance at the center frequency of 1.3 GHz. This ensures that minimum insertion loss is obtained at this frequency. In this case the insertion loss is less than 0.001 dB.



(a) Single Stage Limiter-Switch



(b) Return Loss of Single Stage PIN diode Limiter using CLA4607-085LF and CLA4608-085LF



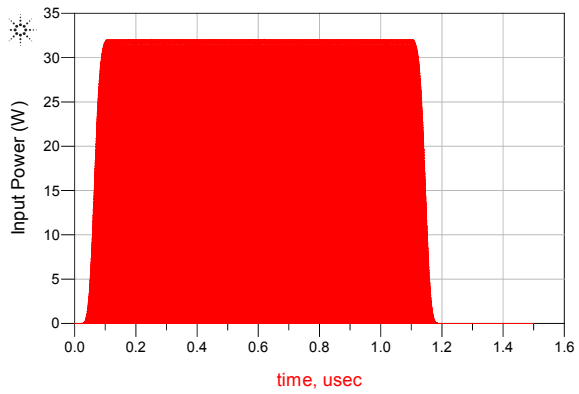
(c) Insertion Loss of Single Stage PIN diode Limiters using CLA4607-085LF and CLA4608-085LF

Figure 6.20: Single Stage Limiter-Switch and it's S-Parameters

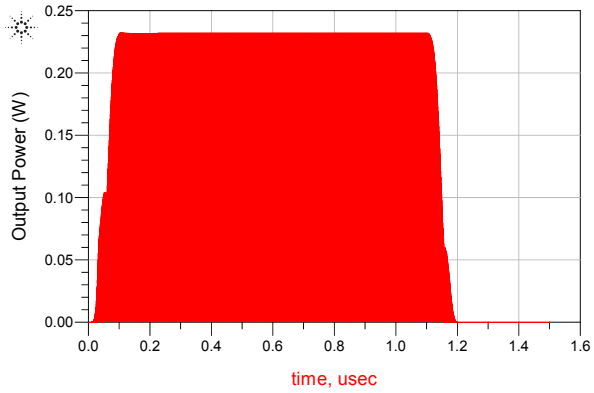
The comparison of the insertion loss obtained using each of the two diodes (see figure 6.20c) shows the CLA4608-085LF diode realising higher losses than the CLA4607-085LF diode at frequencies

outside of the desired frequency range, but this is still less than 0.5 dB even at bandwidths greater than 50 percent.

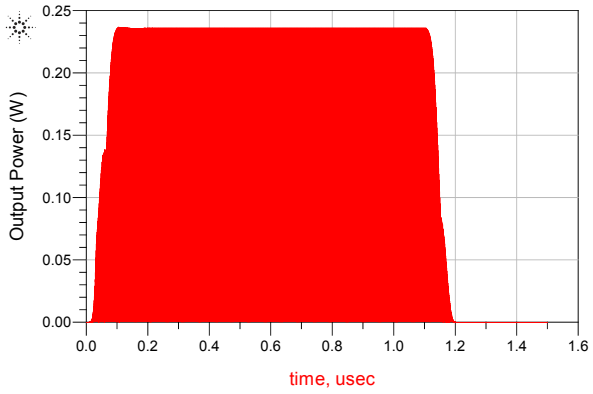
A transient analysis of the single-stage limiters using the two diodes with an 1 µs RF input pulse with an input power of 45 dBm, equivalent to 31.6 Watts, (see figure 6.21a) gives the output power results shown in figures 6.21b and 6.21c.



(a) Input Pulse - 1 µs, 45 dBm (31.6 W)



(b) CLA4608-085LF Diode Limiter-Switch Output Pulse



(c) CLA4607-085LF Diode Limiter-Switch Output Pulse

Figure 6.21: Input and Output pulse for Single Stage Limiter-Switch - Left axis in Watts

The flat leakage output power for a single stage limiter-switch using the CLA4608 diode is approximately 0.233 W (23.7 dBm), and when using the CLA4607, a flat leakage output power of 0.237 W (23.8 dBm) is obtained. In either case the power is only limited by just over 20 dBm.

The required isolation is 30 dBm making it necessary to add an extra diode stage to the limiter in order to achieve this.

The choice of PIN diode is very important in the design because the characteristics and the amount of charge that is stored in the intrinsic layer of the diode determine the diode impedance to input RF and Microwave signals. The diode characteristics in turn determine how much insertion loss and isolation the limiter will have during the reverse bias state of the diode, as well as the carrier lifetime, which also affects the limiting action. The diode with the smaller maximum series resistance in the forward bias state is used as the 'coarse' limiter PIN diode and that with the larger series resistor is the 'clean-up' limiter PIN diode. These diodes are usually placed one-quarter wavelength apart from each other. The 'clean-up' diode also turns on faster than the 'coarse' limiter diode. When a a high power RF pulse is applied at the input of the limiter-switch, for a brief period the signal passes through with little reflection. Then the 'clean-up' diode turns on first creating a standing wave on the transmission line which has a voltage minimum at the 'clean-up' diode node. Being a quarter wavelength apart, the coarse limiter diode node will have a voltage maximum. This forces charge carriers into the I region of the PIN diode resulting in reduced diode impedance. The coarse limiter diode is then forward biased and increases the circuit insertion loss as most of the power is reflected back to the input.

A two stage limiter is now designed using a CLA4608-085 diode for the coarse limiting stage and a CLA4607-085 for the clean-up stage. The setup for the two stage limiter-switch is shown in figure 6.22. When the switch is in off-state, the device circuit acts as a limiter and in its on-state, it is a tuned switch utilising the topology previously shown in figure 6.19.

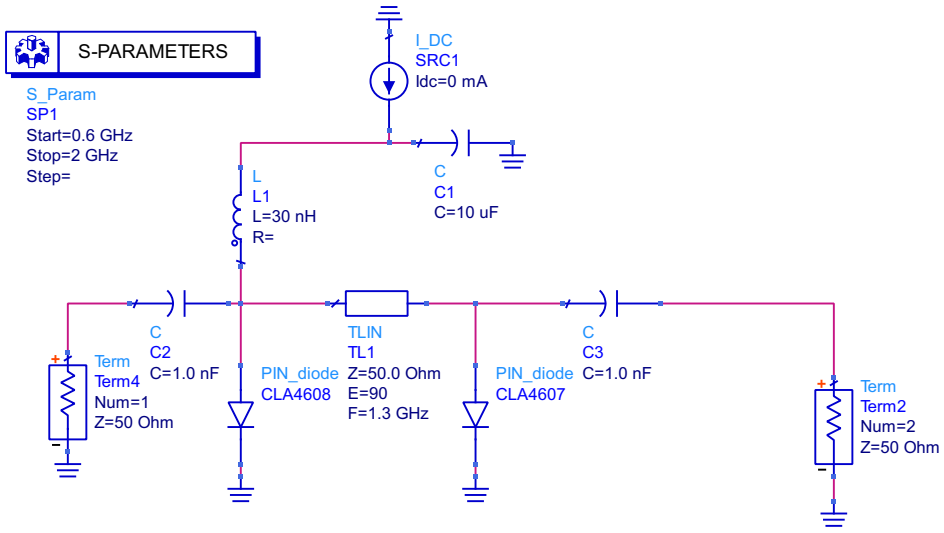
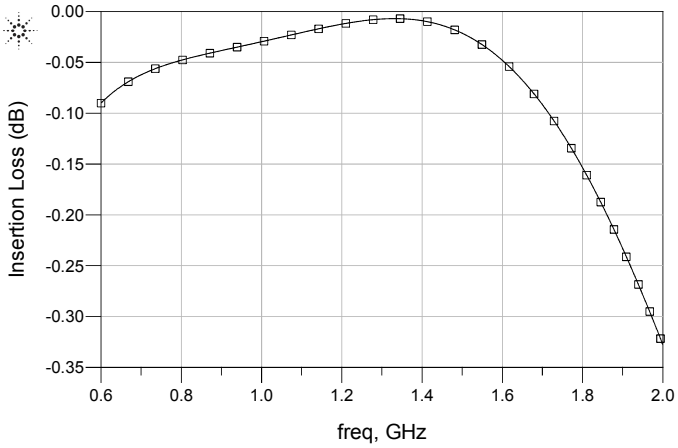
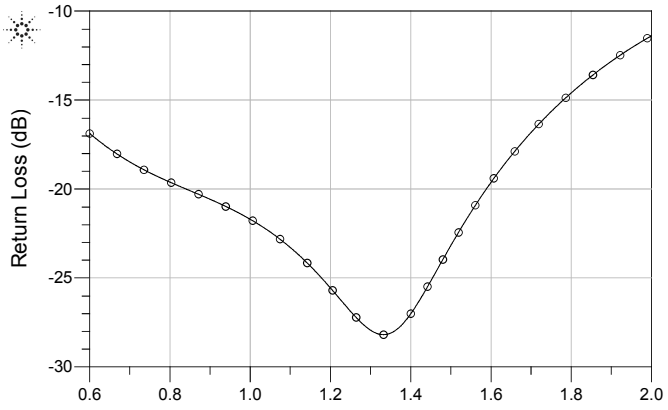


Figure 6.22: ADS Circuit Model of a 2-Stage PIN Diode Limiter

An S-parameter analysis is performed on the circuit in figure 6.22 for a case where the switch is in the off-state and when it is in the on state. Figure 6.23 shows that an insertion loss of 0.007 dB and a return loss of 27.94 dB are obtained at the center frequency of 1.3 GHz.



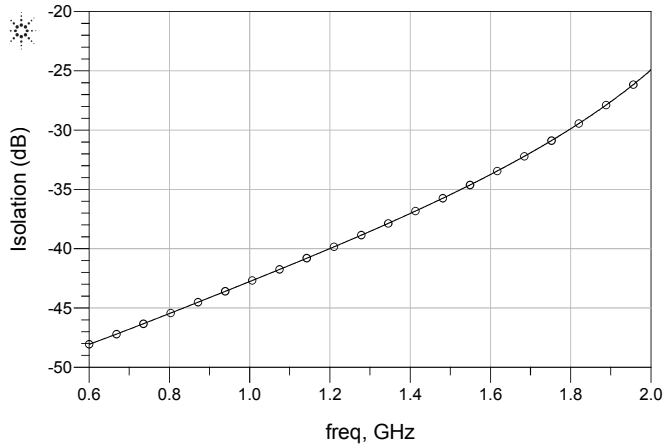
(a) Insertion Loss



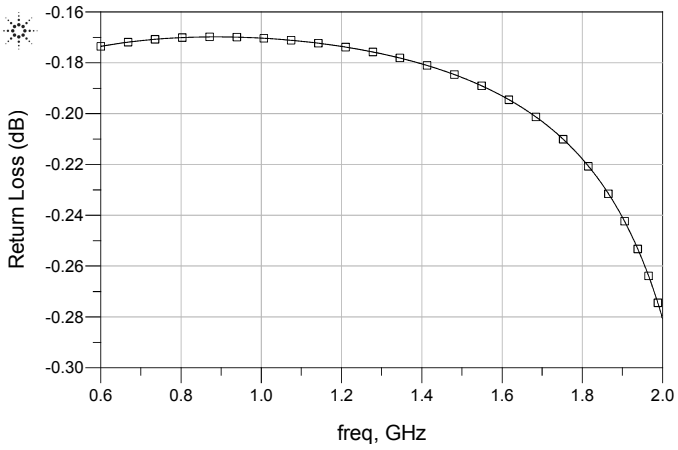
(b) Return Loss

Figure 6.23: S-Parameter Simulation Results of a 2 stage PIN Limiter-Switch when switch is in the Off-State

When the switch is in the on-state with a DC bias current of 10 mA applied, an isolation of 38.54 dB is noted as well as a return loss of 0.176 dB at the center frequency of 1.3 GHz. The plots for the two characteristics are presented in figure 6.24.



(a) Isolation



(b) Return Loss

Figure 6.24: S-Parameter Simulation Results of a 2 stage PIN Limiter-Switch when switch is in the On-State

The next section uses the circuit model in figure 6.22 as a baseline from which the parameters of a physical structure are derived. A multilayer approach in LTCC substrate is proposed and a physical structure designed in the technology is then analysed to verify viability.

6.6 Implementation of Limiter-Switch in LTCC

To the author's knowledge, a PIN diode limiter, with the ability to be used as a switch, and implemented in LTCC has not been reported in literature. A T/R (transmit/receive) switch has been fabricated in LTCC in a configuration that that uses both shunt and series PIN diodes [82]. The structure comprises two surface mount plastic packaged PIN diodes separated by a lumped element equivalent of $\lambda/4$ transmission line comprising a series inductor and two shunt capacitors. The

structure has a total six reactive elements all realised as distributed line elements. The limiter/switch design in this chapter comprises two shunt PIN diodes separated by a $\lambda/4$ transmission line realised as a distributed line element. A total of four reactive elements are used in the circuit - three surface mount chip capacitors and a distributed line inductor. In comparison with the capacitors used in the T/R switch [82], larger capacitance values are used in the limiter/switch design making it difficult to implement as distributed line elements. However, multilayer chip capacitors (MLCC) exist in industry that provide larger capacitance values in miniaturised surface mount chips. These are used in the limiter/switch design. This section seeks to show that the circuit can be implemented in LTCC to achieve a compact structure.

Detailed properties of LTCC have been presented in chapter 2. The advantages that specifically make LTCC suitable for the implementation of this component have also been outlined in section 6.1 of this chapter.

Section 6.5 has presented the design of the circuit equivalent to the desired limiter-switch design. This section now seeks to describe how the circuit is translated into a multilayer stack-up. In figure 6.22, it has been shown that acceptable results for the given set of specifications are obtained when a two-stage limiter-switch circuit is used. The circuit comprises two Skyworks PIN diodes (CLA4607 and CLA4608), an inductor serving as a DC return path in shunt with the main signal path, a capacitor providing a path to ground when zero current flows from the DC bias current source, a quarter wavelength transmission line between the two diode shunt connections and DC block capacitors at the input and output.

The physical construction of the limiter-switch circuit is implemented in a miniaturised 4 layer assembly shown in figure 6.25. The top layer is denoted layer 0, while the bottom layer is labelled as layer 3 in the figure.

The construction was chosen to achieve the following:

- To effectively distribute the elements so that a compact structure is achieved.
- Where the use of embedded elements could potentially be very large is size, available small sized chip elements would be used.
- To have all three port connections (input, output and DC bias) on a single outer layer for easier flipping of the final packaged chip.
- To incorporate sufficient thermal conductivity paths to the PCB layout onto which the chip is to be flipped.

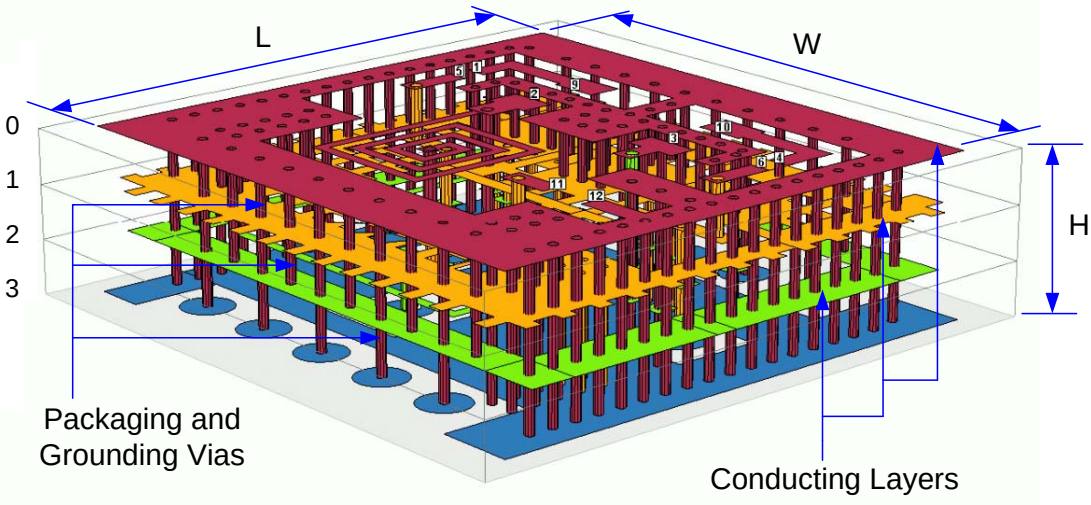


Figure 6.25: Three dimensional Layout of Limiter-Switch

It is decided that the inductor is to be implemented in spiral form. The theoritical aspects of a spiral inductor were discussed in section 2.5. In addition to the PIN diodes, the DC block capacitors are also chosen as chip elements. The distributed equivalents would otherwise be large, increasing the overall footprint. An alternative would be to insert very high permittivity dielectric materials between the two plates of a parallel-plate capacitor. This would, however, increase the circuit complexity and associated costs. The structure is shown to have packaging vias all around that shield the electromagnetic fields within the circuit from leaking out and from external interference.

The chip elements and the inductor are placed on layer 0 and are distributed as shown in figure 6.26.

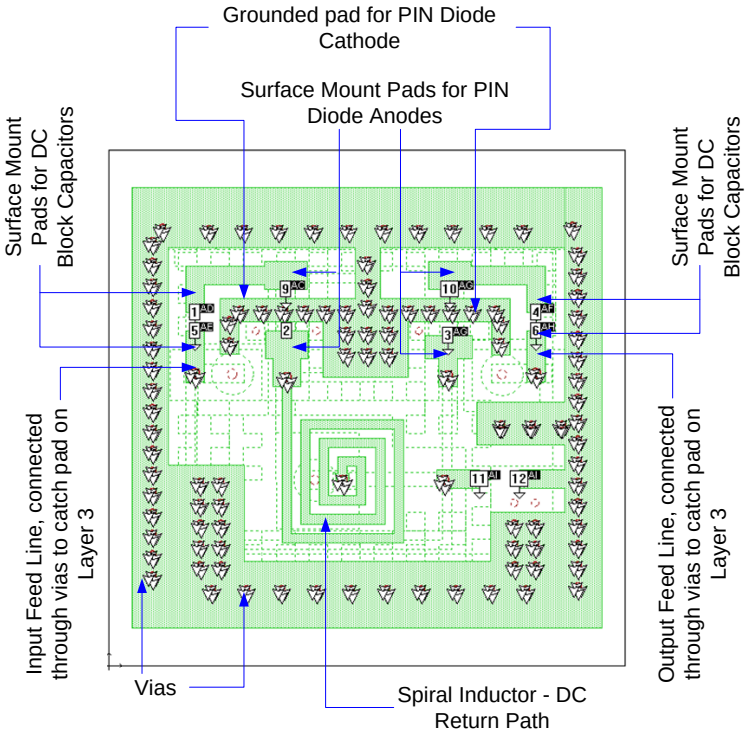


Figure 6.26: Layer 0

The conductor pads for the mounting of the diodes are arranged in a manner that conforms with the Skyworks suggested mounting shown in figure 6.27. Several thermal vias as connected to the conducting pad that is connected to the cathode to provide sufficient thermal paths for heat sinking.

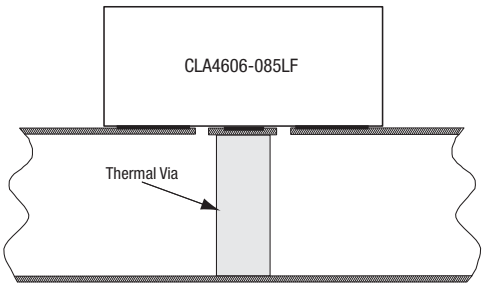


Figure 6.27: Cross-Sectional View of Suggested Mounting for CLA46XX-085LF PIN diodes

Layer 1 is a gridded ground plane with clearances for vias that connect from layer 0 to lower layers in a staggered manner. The ground plane is also given castellated edges on the outer edges and on the clearance edges. This creates enough exposed substrate for the bonding of vertically adjacent layers. This is shown in figure 6.28.

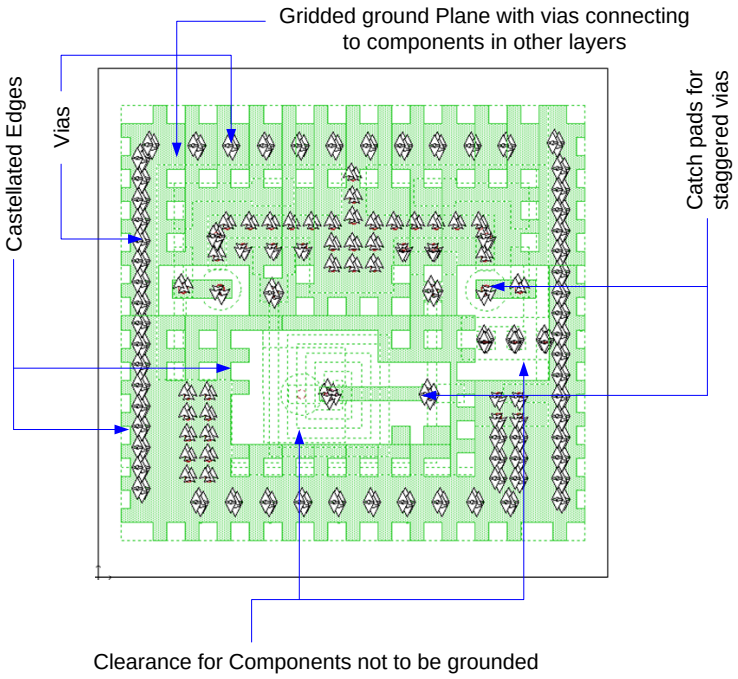


Figure 6.28: Layer 1

Layer 2 (see figure 6.29) hosts the quarter wavelength tramsmission line and a ground plane around the edges to ground the packaging vias. It also has catch pads to vias that connect the signal paths between different layers.

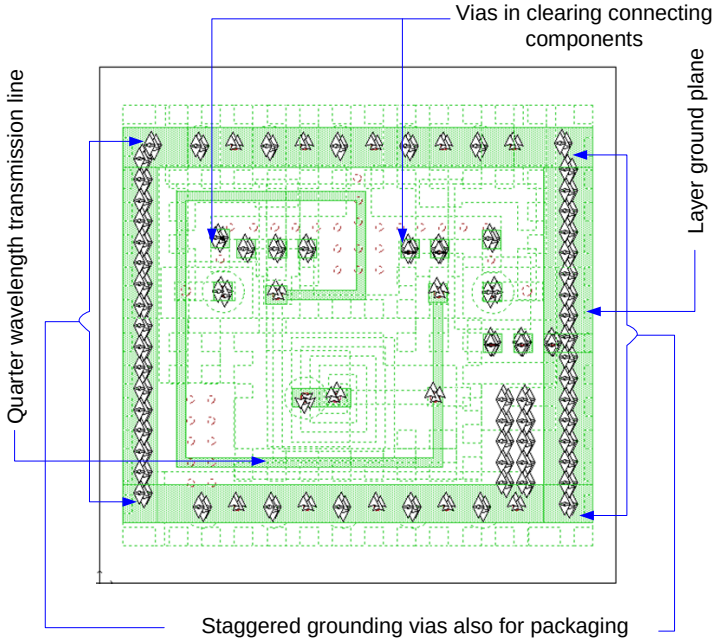


Figure 6.29: Layer 2

The input, output and DC bias signals are to be fed to the circuit through copper balls soldered

onto circular solder pads on layer 3, when the circuit is flipped onto a PCB. Layer 3 also houses other circular solder pads through which the circuit ground is to be connected to the PCB ground.

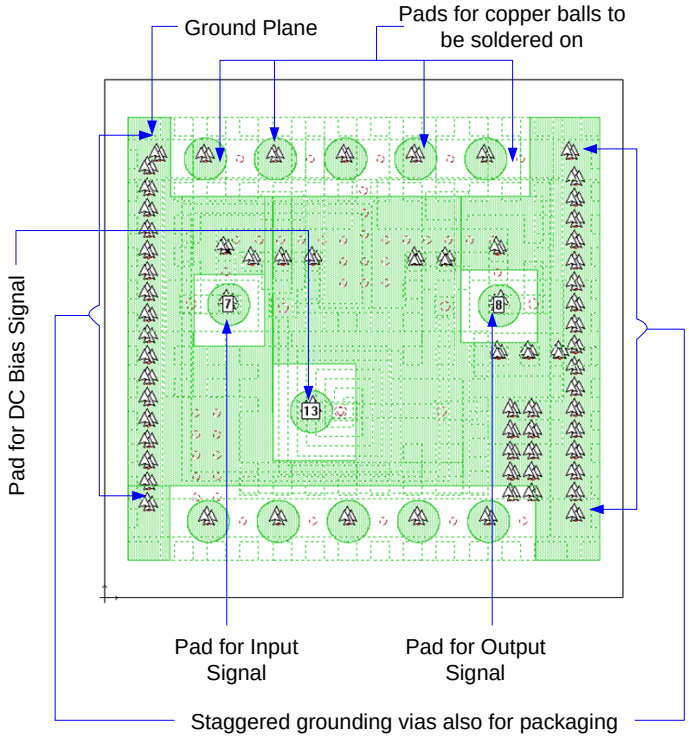


Figure 6.30: Layer 3

In designing the layers presented above, numerous iterations had to be performed to arrive at acceptable results. Such a circuit presents the challenge of having many parasitic effects that are difficult to isolate due to the number of different elements in the circuits and their proximity to each other. Minimum dimensional recommendations were avoided in anticipation of tape shrinkage during the fabrication process which would then possibly affect the measured results.

In the subsection that follows, simulation results for the physical structure are presented to verify the operation of the circuit.

Simulation Results

The physical structure of the limiter-switch is simulated in Sonnet to verify the performance of the three dimensional implementation of the device. Several ports are assigned and an S-parameter simulation is run in the absence of the the chip elements. The S-parameter file is then imported into Agilent Technologies' ADS and the diodes and capacitors are connected to relevant ports as shown in figure 6.31.

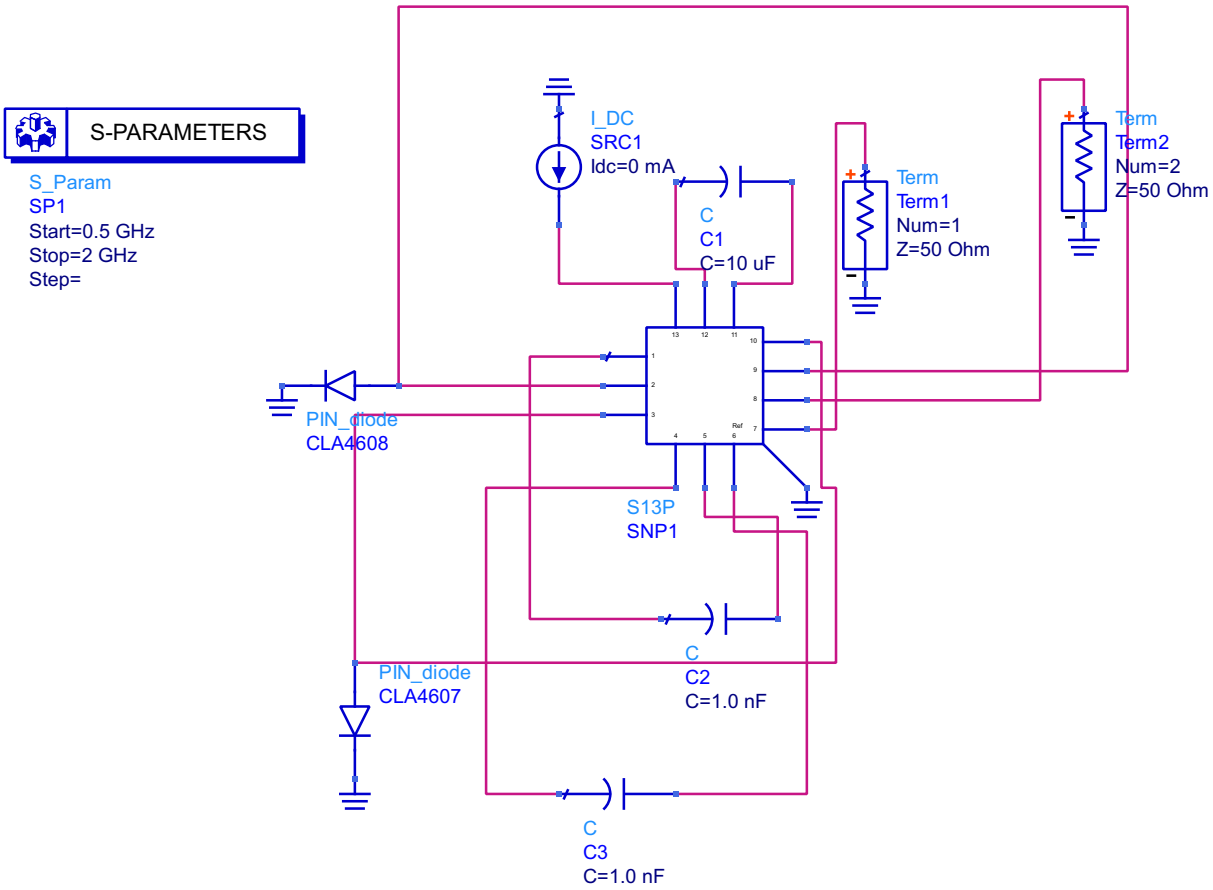
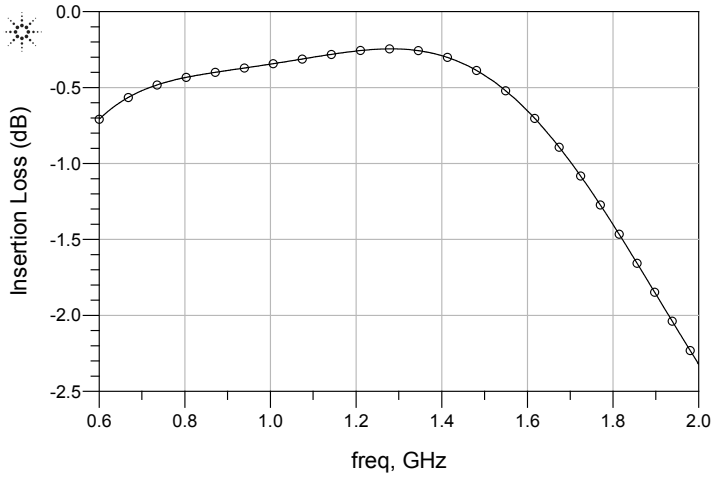
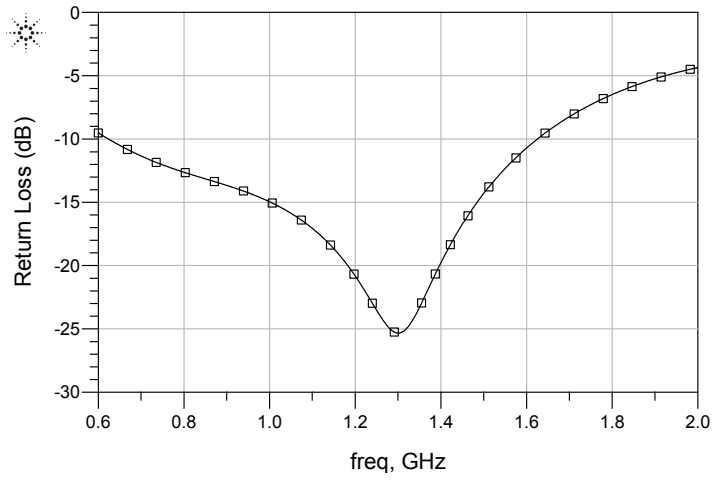


Figure 6.31: ADS circuit with PIN diodes and DC block connected to imported S-Parameter File of three dimensional structure analysed in Sonnet

From this setup, an insertion loss of 0.25 dB and a return loss of 25.34 dB at a center frequency of 1.3 GHz are obtained when the switch is in its off-state so that the circuit behaves like filter. These results are shown in figure 6.32.



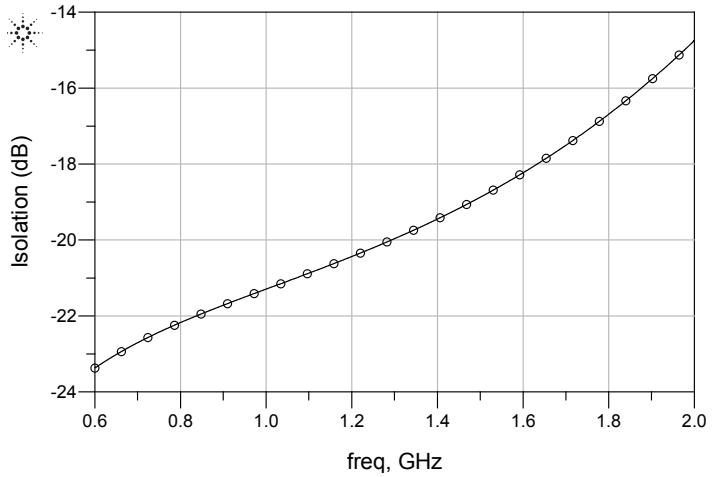
(a) Insertion Loss



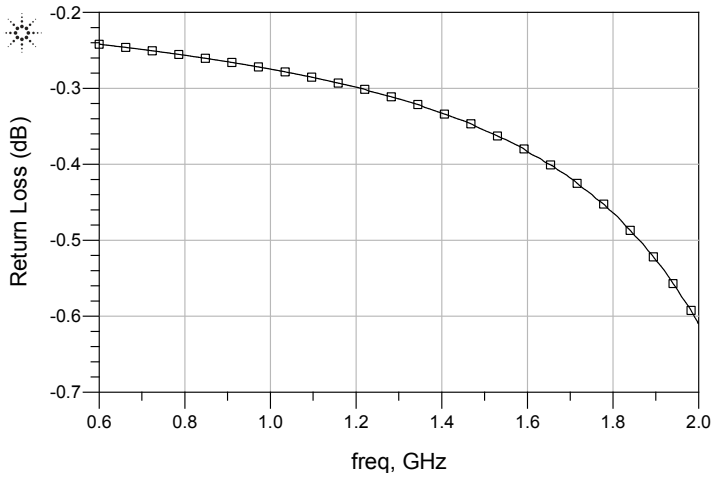
(b) Return Loss

Figure 6.32: S-Parameters for the circuit in figure 6.31 when switch is in Off-State.

When a DC bias current of 10 mA is applied and the switch is in the on-state, an isolation of 19.96 dB and a return loss of 0.314 dB are obtained. This is shown in figure 6.33.



(a) Isolation



(b) Return Loss

Figure 6.33: S-Parameters for the circuit in figure 6.31 when switch is in On-State.

A transient analysis is also performed in the off-state of the switch where a large 1 µs input pulse signal of 45 dBm is applied at the input of the limiter-switch. This is equivalent to 31.6 Watts. The resulting output pulse shown in figure 6.34. It shows a flat leakage of approximately 45 mW of power corresponding to 16.4 dBm.

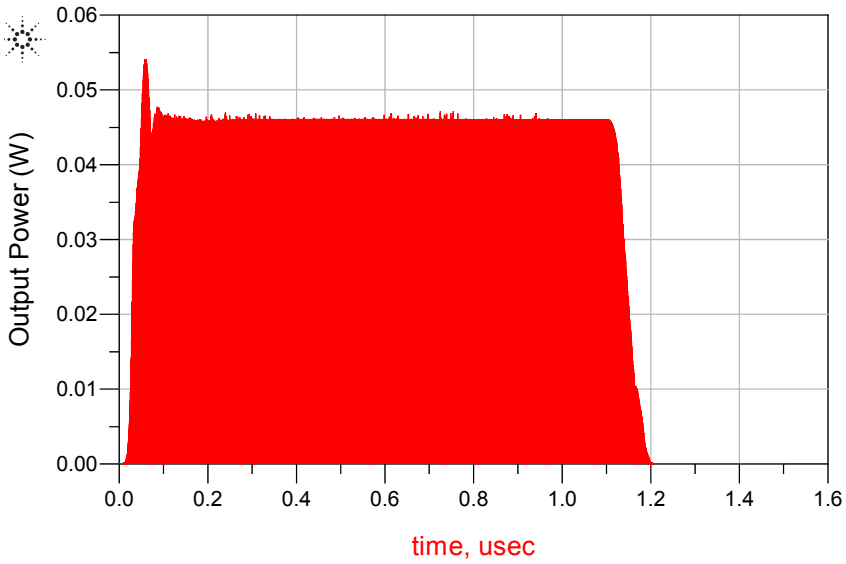
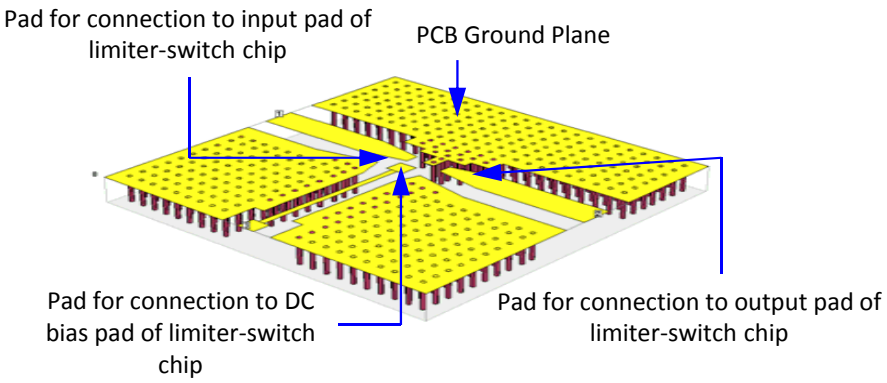


Figure 6.34: Output pulse for the circuit in figure 6.31; Left axis is in Watts

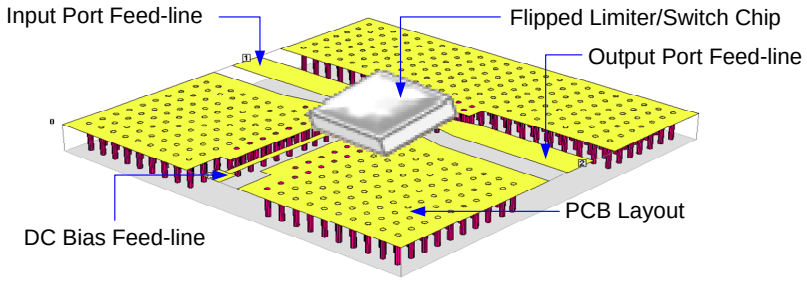
6.7 Future Work

As part of future developments to the work that has been presented in this chapter, the circuit is to be fabricated and the measurement results are then to be analysed to confirm those of the simulated physical structure.

The circuit to be fabricated is to have dimensions of 1 cm by 1 cm with a fired thickness of 0.55 mm. Once the circuit has been fabricated, it is to be flipped onto a PCB board for measurements, due to its small size. Figure 6.35a shows the PCB layout that is designed for this purpose and figure 6.35b illustrates how the final limiter-switch chip is expected to fit on the board.



(a) PCB layout



(b) PCB with flipped chip

Figure 6.35: Limiter-Switch Chip Flipped on a PCB

SMA connectors are to be connected to the input and output feed-lines so that S-Parameters can be measured on a Vector Network Analyser, and a DC current source is to be connected to the DC-bias feedline. The measurements are then to be documented and analysed.

6.8 Conclusion

An implementation of a LTCC-based PIN diode limiter-switch has been proposed. The properties that make LTCC well suited for the design of limiters and switches have been discussed. Designs of both a circuit equivalent and the physical structure of an L-Band LTCC limiter-switch have been presented.

The physical implementation has been shown to yield a flat leakage of 16.4 dBm when an input power of 45 dBm is applied at the input of the limiter-switch when the switch is in off-state. An insertion loss, also simulated in the switch off-state, of 0.25 dB is obtained at the center frequency of 1.3 GHz, which is less than that provided in the design specifications. When the switch is in the on-state, an isolation of 19.98 dB is noted.

The analysis of the physical structure has shown LTCC to be a viable alternative for the construction of limiters and/or switches with the advantage of miniaturised size. A chip size of 1 cm by 1 cm is achieved.

While not all the specifications have been met, the obtained results are acceptable for purposes of confirming performance viability.

As part of future work, the limiter is to be manufactured and measured to analyse the challenges associated with manufacturing and its cost implications.

Chapter 7

Conclusion

This dissertation aimed at presenting different RF and microwave circuit designs that exploit the advantages of multilayer substrate technologies. It has presented designs implemented in printed circuit board, liquid crystalline polymer and low temperature cofired ceramics, all of which have been verified through full-wave electromagnetic simulations or through simulation and measurement.

Chapter 3 has presented a new topology of a cross slot-coupled folded SIW filter with a second order response obtained through a cross-slot coupling technique. The structure has been analysed in detail by studying the behaviour of its simulated electromagnetic field patterns and densities to understand its performance properties. A circuit model has been derived to aid in the modelling of the filter performance and has been shown to approximate the behaviour of the 3D model of the filter satisfactorily. Different characteristics of the filter have been presented and a C-band diplexer has been designed using two of the filters. A diplexer has been manufactured and results have been presented for two multilayered circuit technologies: PCB and LCP. PCB multilayered fabrication has been shown to be successful in producing a circuit with good performance. Resulting passbands have been seen to have shifted upwards in frequency from the design center frequencies - an aspect that can be attributed to possible shrinkage of the circuit during fabrication. A high insertion loss of approximately 9.3 dB is also obtained for the second passband whereas the first passband registers a better insertion loss of about 2.75 dB.

LCP fabrication is shown to have been unsuccessful and would possibly require several more iterations to come up with a lamination profile suitable for substrate thicknesses greater than 0.5 mm.

In chapter 4, a detailed study of RSIW has been presented and an improved resonator structure which was denoted 'ridge-like' FSIW has been proposed. The waveguide structures from which the resonators are formed have been comparatively investigated in terms of cutoff frequency to establish that for similar waveguide outer dimensions, the latter topology can achieve lower cutoff frequencies. This means that devices designed using the latter resonator can operate at lower frequencies for the same dimensions as the former resonator.

A new resonator topology has also been proposed and presented. This has been shown to achieve a wide stopband, wider than that achievable by other resonators also discussed in the chapter. This

resonator has been used for the design of two X-band filters: a second order filter and a fourth order one. Simulation results from a circuit simulator have been compared to those of a full-wave electromagnetic simulation as part of the design process to model a three dimensional circuit to match the performance of a lumped element circuit equivalent. The fabrication of these circuits in PCB multilayer technology has been briefly outlined and finally, the measurement results have been presented and compared to the simulated results from the full-wave electromagnetic simulation. Good results were obtained confirming the simulated properties of the proposed resonator.

The first LTCC based device was a 3-segment polyphase filter presented in chapter 5. The analog RC polyphase filter in LTCC has been proposed as an alternative to CMOS-based analog equivalents. The LTCC-based circuits have been suggested as better options for lower frequency implementation and to verify viability, a polyphase filter operating at a frequency range of 100 to 300 MHz has been designed. The simulation of the physical structure has yielded an image suppression of 35 dB over this frequency range. From a design point of view, it has been shown that a practical size of a polyphase filter is feasible and acceptable performance levels can be obtained with the designed structure.

From a manufacturing point of view, however, a design with several layers poses the challenge of being relatively expensive in its realisation. This specific design requires a total of 26 screens and stencils each of which must be loaded on a frame of its own. This corresponds to 26 individual screen printing runs, and follow-up individual drying stages. The process is also time consuming and requires skilled hands to achieve accuracy.

The above observations do not, however, rule out the viability of this substrate as a suitable choice. It can be recommended that for cost-efficiency, thinner substrates be used instead.

In chapter 6, an implementation of an LTCC-based PIN diode limiter-switch has been proposed. The properties that make LTCC well suited for the design of limiters and switches have been discussed. Designs of both a circuit equivalent and the physical structure of an L-Band LTCC limiter-switch operating at a frequency of 1.3 GHz have been presented.The physical implementation has been shown to yield a flat leakage of 16.4 dBm when an input power of 45 dBm is applied at the input of the limiter-switch when the switch is in off-state. A desirable insertion loss, also simulated in the switch off-state, of 0.25 dB has been obtained at the center frequency of 1.3 GHz. This has satisfied the design specifications. When the switch is in the on-state, an isolation of 19.98 dB has be achieved.

The analysis of the physical structure has shown LTCC to be a viable alternative for the construction of limiters and/or switches with the advantage of miniaturised size. A chip size of 1 cm by 1 cm has been achieved.

While not all the specifications have been met, the obtained results are acceptable for purposes of confirming performance viability.

Intended future work included manufacturing and measuring the limiter to analyse the challenges associated with manufacturing and related cost implications.

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