

DYNAMIC DIGITAL CONTROL SCHEMES FOR THREE-PHASE UPS INVERTERS

By

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degree of Master of Science in Engineering at the University of
Stellenbosch

The crest of the University of Stellenbosch is centered behind the text. It features a shield with various symbols, topped by a crown and a banner.

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Declaration

I, the undersigned, hereby declare that the work contained in this thesis is my own original work and that I have not previously, in its entirety or in part, submitted it at any university for a degree.

28 November 2002

Summary

This thesis presents the design and implementation of a voltage controller for an Uninterruptible Power Supply (UPS) Inverter. The inverter is capable of producing a nearly sinusoidal output voltage waveform, thereby keeping the Total Harmonic Distortion (THD) to a minimum.

Digital controllers introduce a time delay in the control law that causes system instability. Various control techniques, which includes Pade approximations and system augmentation, are investigated to eliminate the effect of the time delay. These controllers employ classical control as well as modern control techniques. The selection of the various control parameters is verified by mathematical equations. A load-disturbance compensation scheme, implementing feed-forward and gain scheduling, is also developed to improve voltage distortion when varying loads, such as non-linear loads, are connected to the system. It is shown that the constructed pulse-width modulated (PWM) control scheme can achieve fast dynamic response as well as a low THD.

Opsomming

Hierdie verhandeling ondersoek die ontwerp en implementering van 'n spannings-beheerder vir 'n ononderbroke kragtoevoer omsetter. Die stelsel produseer 'n uittree spanningsgolfvorm met 'n lae Totale Harmoniese Distorisie (THD).

Digital beheerders veroorsaak 'n tydvertraging in die beheerwet wat stelsel onstabieleit kan veroorsaak. Verskeie beheertegnieke wat gebaseer is op die Pade benaderings van die tydvertraging en stelsel aanpassings, is ondersoek. Hierdie beheerders maak gebruik van klassieke en moderne beheertegnieke. Die seleksie van die verskeie beheerderveranderlikes word gestaaf deur wiskundige vergelykings. Spanningsvervorming word tot 'n minimum beperk deur gebruik te maak van 'n lasveranderings-kompensasietegniek wat onderskeidelik vorentoe-voer en aanwinstskedulering implementeer. Verder word daar bewys dat die pulswydte modulاسie (PWM) beheerskema vinnige dinamiese gedrag asook 'n lae THD bewerkstellig.

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Nomenclature

Abbreviations

dc-bus	Direct current bus
dc-link	Direct current link
DOF	Degree-of-freedom
DS	Dynamic stiffness
DSP	Digital Signal Processor
emf	Electromotive force
FFT	Fast Fourier Transform
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronic Engineers
IGBT	Insulated Gate Bipolar Transistor
K-vector	Vector gain for deadbeat controller
LHP	Left-hand plane
NER	National Electricity Regulator
NRS	National Regulatory Service
PCC	Point of common coupling
PI controller	Proportional / Integral controller
PI variables	Proportional / Integral variables
PWM	Pulse Width Modulated
rms	Root mean square
S(s)	Sensitivity function

T(s)	Complementary sensitivity function
THD	Total Harmonic Distortion
UPS	Uninterruptible Power Supply
VSI	Voltage Source Inverter
ZOH	Zero-order hold
z-plane	Discrete plane

System Variables

L	Filter inductor
C	Filter capacitor
V	Voltage
I	Current
I_p	Positive-sequence current
I_n	Negative-sequence current
I_0	Zero-sequence current
A, B, C	Indicating a phase quantity
α	Alpha-plane
β	Beta-plane
0	Zero-plane
N	Negative dc-bus
n	Load neutral
f_s	Switching frequency
T	Switching period
mT	Fraction of switching period

t	Time
V_{dc}	dc-bus value
s	Frequency domain
z	Discrete-time domain
\mathbf{x}	Vector
\dot{x}	Time derivative
φ	Phase

Classical Controller

V_c	Output voltage
i_o	Output current
$*$	Reference signal
R_a	Proportional current gain
K_i	Integral gain for PI controller
K_v	Proportional gain for PI controller
w	Disturbance signal

Modern Controller

V_c	Output voltage
I_L	Filter inductor current
I_o	Load current
\mathbf{x}	State vector

Δx	Error in state
A	State matrix in continuous time
B	Input matrix in continuous time
C	State output matrix in continuous time
U	Control signal
C	Controllability matrix
Φ	Discrete state matrix
Γ	Discrete input matrix
Γ_i	Discrete input matrix for load current
Φ_{del}	Discrete state matrix with included time delay
Γ_{del}	Discrete input matrix with included time delay
I	Unity matrix
F	Feed-forward gain
N_u	Scalar to eliminate steady-state error
N_x	Vector to eliminate steady-state error
K	Control matrix gain for modern controller
*	Indicating reference value

Chapter 1

Introduction

1 Introduction

1.1 Power quality

Power quality is defined in various ways, depending on the frame of reference. For instance, the supplier will see power quality as supplying a “high-quality, reliable” voltage waveform. Alternatively, the customer will see it as receiving an “always present” voltage waveform [40]. The definition of power quality given by various sources may differ in terminology, but what all of them have in common is the interaction between the power system and the connected load. The definition of power quality adopted in this thesis is stated as follows: *Any power problem manifested in voltage, current, or frequency deviations that results in failure or malfunction of customer equipment* [41].

Over the years, customers have become used to a high quality of supply, and often did not realize that there are imperfections present that are very hard to compensate for, or even eliminate. Electronic and power electronic devices became much more sensitive, and require a clean, consistent voltage waveform in order to function correctly. These devices are not only sensitive to voltage disturbances, but also cause disturbances for other customers connected to the same utility. Examples of such devices can be non-linear loads, such as converter-driven equipment and rectifier loads. The utility can only control the quality of the voltage, and because of the close relationship between voltage and current, these non-sinusoidal currents will introduce harmonic components in the supply voltage, which in turn will cause problems such as voltage flickering and voltage distortion [40]. The South African NRS 048, North American IEEE 519 and European IEC 1000-3 were developed because it is technically impossible to keep voltage waveforms at a constant frequency and magnitude. These standards will be discussed.

1.1.1 South African NRS 048

The NRS 048 document [46] was developed for the National Electricity Regulator (NER) to set the standards to which licensed utilities should adhere. It sets the

minimum standards for the quality of power supplied to the end-users by the South African utilities. The maximum harmonic levels, as specified by NRS 048, are given in Table 1.1. The magnitude of each harmonic is determined by sampling each phase every 3 seconds for a total period of 10 minutes. This is done for 24 hours and the maximum 10 minute rms value which does not exceed 95% is then recorded. This test is done continuously for at least 7 days.

The Total Harmonic Distortion (THD) of the supply voltage includes all the harmonics up the 40th, and may not exceed 8%.

Table 1.1: NRS 048 Maximum Harmonic Values

Odd Harmonics		Odd Harmonics		Even Harmonics	
Order	%	Order	%	Order	%
5	6	3	5	2	2
7	5	9	1.5	4	1
11	3.5	15	0.3	6	0.5
13	3	21	0.2	8	0.5
17	2	>21	0.2	10	0.5
19	1.5			12	0.2
23	1.5			>12	0.2
25	1.5				
>25	$0.2 + 1.3 \times 25/h$				

1.1.1.1 Voltage regulation

The voltage regulation of a system is defined as *the ability for the steady-state rms voltage to remain between the upper and lower voltage limits* [46]. The voltage regulation, as specified by NRS 048, is given in Table 1.2. All measurements taken to determine the voltage regulation should be taken at the extremities, in other words, the near and far ends of the feeders.

Table 1.2: Maximum deviation from standard voltages

Voltage Level [V]	Compatibility Level [%]
< 500	± 10
≥ 500	± 5

1.1.1.2 Voltage dips

A voltage dip is defined as *a sudden reduction in the rms voltage for a period of between 20 ms and 3 s of any of the three phases* [46]. The duration is measured from the time that the rms voltage drops beneath 0.9 per unit of the standard voltage until the time that it rises above 0.9 per unit of the standard voltage. Such a voltage dip is shown in Figure 1.1.

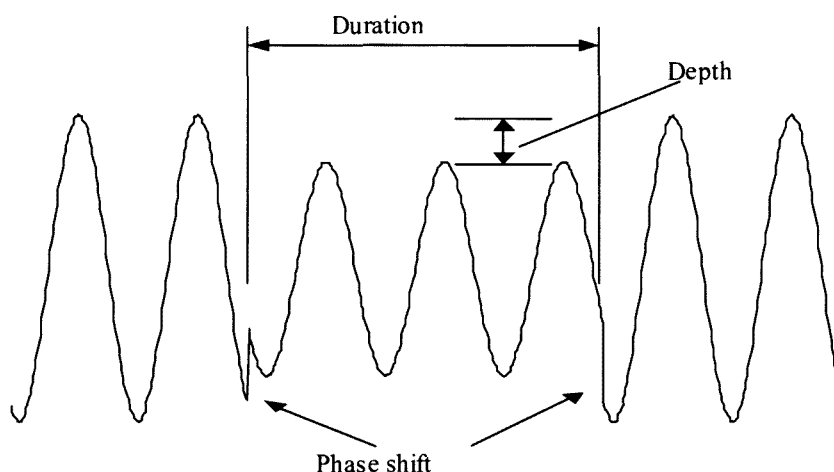


Figure 1.1: Definition of a voltage drop

1.1.2 North American IEEE 519

The IEEE 519 [47] is an American standard that limits the amount of harmonic emissions injected into the utility by the customer. It is the responsibility of the utility to maintain the quality of the supplied voltage waveform. The IEEE 519 standard for voltage distortion is given in Table 1.3.

Table 1.3: IEEE 519 Standard for Voltage Distortion at the PCC

Voltage at PCC	Individual Voltage Component Distortion	Maximum THD (%)
$V_{PCC} < 69 \text{ kV}$	3.0%	5.0%
$69 \text{ kV} < V_{PCC} < 132 \text{ kV}$	1.5%	2.5%
$V_{PCC} > 132 \text{ kV}$	1.0%	1.5%

1.1.3 European IEC 1000-3

The European IEC 1000-3 [48] focuses on the end-user equipment level. The standard is split into various categories: IEC 1000-3-2 limiting low power equipment (up to 16 A), IEC 1000-3-4 limiting equipment up to 75 A and IEC 1000-3-6 limiting medium to high voltage equipment.

The harmonic levels are the same as the NRS 048, and are given in Table 1.1.

1.2 Problem definition

As can be seen from the previous section, the electric supply waveform is often not of acceptable quality, mainly due to the voltage distortion that arises from distorted currents passing through the series impedance of the power delivery system. The installation of an uninterruptible power supply (UPS) system is therefore accepted as being a vital element in the protection of sensitive equipment, as it supplies power to the load in the event of a power outage. Furthermore, with the right switching strategy, the quality of the supply can be kept at allowable levels. It is desirable that the output voltage stays sinusoidal over all loading conditions, or if not that, at least inside the allowable limits of operation. Industry tends to use passive LC-filters connected to the UPS-style inverters. These filters are necessary due to the distorted pulse width modulated (PWM) waveform that is generated by the inverter [4]. In lower power devices, it is possible to increase the switching frequency to eliminate the need for filtering. However, at higher power levels, this is impossible, as the

switching losses vary linearly with the switching frequency: $P_s = \frac{1}{2} V_{dc} I_L f_s (t_{on} + t_{off})$ [38].

Therefore, when using high-power devices, different types of loads will cause the transfer function of the load-filter combination to change, and the output voltage will no longer be sinusoidal.

1.3 Possible solution to the problem

With the increase in sensitive devices, companies have also become more sensitive to any loss in production time, affecting their profit margins. The quality of the supply certainly seemed to be degrading, either being caused by bad power quality or end-user equipment. Therefore, much research has been done in the development of devices which would improve the quality of supply [2], [9], [15], [40]. These devices implement various switching strategies and control techniques to ensure output waveforms of acceptable quality.

Extensive research has been done on single-phase and balanced three-phase power converters [1] - [3], [8] - [11]. These converters are usually low-power converters implementing high switching frequencies, which improves the output waveforms significantly. The output waveforms are thus within the specifications, presumably controlled by good control techniques. With higher-power devices it is impossible to use a high switching frequency due to losses in the switching devices, and therefore it would produce outputs that are usually of lower quality than low-power devices. The three-phase converters that are used are three-wire systems that are unable to handle neutral currents, thus unable to supply unbalanced loads. The output waveforms of these converters differ in magnitude under unbalanced conditions, because the three phases are coupled and cannot produce independent voltage waveforms. When open-loop controllers are used to produce the output voltage waveforms, the controllers are capable of maintaining the desired average voltage, but have a very slow (several cycles) response to step changes [1]. Various closed-loop controllers implementing different control variables, such as filter

inductor current, filter capacitor current, load current and filtered output voltage, try to improve performance [1], [28]. These closed-loop controllers are often extended to deadbeat controllers [2], [3], [8] - [11] or repetitive controllers [18] - [20]. With these controllers, it is possible to generate a waveform with a much lower THD.

1.4 Research focus

The PWM inverter plays an important role in converting dc to ac voltages, and therefore the performance of these systems depend highly on the dynamics of the PWM inverter. As the controllers are usually implemented in the digital domain, the pulse width is limited by the computation time of the digital signal processor (DSP). The controller is designed with these dynamics in mind, to ensure it is stable for all system conditions. This thesis presents such a controller designed to control a high-power, three-phase PWM inverter with an LC output filter. The classical control design, where transform methods are used, is evaluated to find a controller that would produce output voltage waveforms of high quality. Controller schemes that are explored, are filter inductor and load current decoupling, back electromotive force (emf) decoupling as well as load disturbance decoupling. Non-linear effects such as PWM and sampling are modeled by means of appropriate s-domain functions. These control methods will be optimized by various control laws and will be compared to find the best control algorithm. Thereafter, modern control techniques, where state space methods are utilized, will be used to evaluate different closed-loop topologies. Deadbeat control is investigated, as this type of control tries to get the output voltage equal to the reference voltage as fast as possible [7]. Load current feed-forward is also implemented to ensure a system that is unaffected by various load conditions, and to render an output voltage waveform that is of good quality, implying a low THD.

1.5 Structure of this report

Chapter 2 gives the different circuit configurations used in power electronic devices, with the three-phase, four-wire configuration being used to handle neutral currents. This configuration is adopted as the UPS configuration to provide a system that would be able to produce output voltage waveforms that are unaffected by various loading conditions. Control system theory used to design stable, closed-loop controllers that are insensitive to loading conditions, will also be discussed in this chapter. Augmentation of the system equations to include time delays, which arise when using digital controllers, will also be discussed.

Chapter 3 explains the design of a classical closed-loop controller. The time delay, which is introduced by using DSP's, is represented by a Pade approximation [36], which transforms the system to second order. System stability could be lost as the poles are pushed to the right-hand side of the frequency domain when the wrong controller gains are used. System sensitivity is improved by implementing feed-forward control, which provides a decoupling effect for the disturbance caused by the load current. Finally, a PI controller is used to eliminate any steady-state error in the output voltage waveform. Stability checks are done to ensure the poles remain to the left-hand side of the frequency plot.

Chapter 4 deals with the design of a controller using modern control techniques. Deadbeat control is implemented to move the system poles to the origin in the discrete domain, thereby ensuring fast response, thus attaining a sinusoidal output voltage waveform. The system equations are augmented to include the time delay caused by calculations of the DSP. By doing this, the dimension of the state variables is increased, but stability is ensured. The load current is treated as if it is a disturbance affecting the plant, and is compensated for by using feed-forward control. Non-linear loads produce output voltage waveforms that do not comply with the limits as set out in the standards discussed [46], [47] and [48]. An explanation is provided why low THD waveforms cannot be obtained. These factors include switching frequency, dead time and calculation delay, and are all fixed due to the high-power device that is used, and the speed of the digital controller. An auto-tuning algorithm is used to calculate the feedback gains, which constantly shifts the poles to

the origin as the system changes with varying loads. Simulations are given to show how the closed-loop controller performs compared to an open-loop controller.

Chapter 5 evaluates the designed controller by comparing practical results using an existing open-loop controller, with the results of the designed closed-loop controller.

Chapter 6 concludes the thesis by giving a summary of the results achieved. Suggestions for improving controller performance are given, focusing on the concept of active power filtering and improving measurement systems to increase controller bandwidth. This will improve system performance, producing higher quality output voltage waveforms.

Chapter 2

Background Information

2 Background Information

2.1 Introduction

In this chapter various circuit configurations are discussed. It is shown that a four-legged VSI (voltage-source inverter) is able to handle any neutral currents that may flow due to unbalanced or non-linear loads. This topology is adopted for the UPS inverter as unbalanced loads are very common, with unbalance varying from no load to full load. The rest of this chapter introduces control system theory to design a stable, closed-loop controller for the inverter. Section 2.4.3 explains state augmentation to ensure sustained system stability. This is done by expanding the system equations to include previously applied control signals to eliminate any calculation delays caused by using DSP controllers. Section 2.4.4 explains deadbeat control, which is used as a pole-placement technique in a linear feedback control law, Section 2.4.5. Section 2.4.8 introduces feed-forward control to eliminate disturbances that influence the output of a system negatively.

2.2 Definition of unbalanced loads

Fortescue [44] developed the method of symmetrical components in 1918 to analyze unbalanced three-phase systems. With this method, an unbalanced three-phase variable is decomposed into three balanced sequence networks that are connected at the points of unbalance [44]. Symmetrical component analysis can now be used to describe arbitrary three-phase currents with three sets of balanced three-phase currents, being zero-sequence, positive-sequence and negative-sequence networks. The three unbalanced currents are defined as follows:

$$I_a \angle \phi_a, I_b \angle \phi_b, I_c \angle \phi_c \quad (2-1)$$

The sequence components can be calculated from the a-b-c currents using Equation (2-2) and the inverse transform is given by Equation (2-3), as follows:

$$\begin{bmatrix} I_0 \\ I_p \\ I_n \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & \mathbf{a} & \mathbf{a}^2 \\ 1 & \mathbf{a}^2 & \mathbf{a} \end{bmatrix} \begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} \quad (2-2)$$

$$\begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & \mathbf{a}^2 & \mathbf{a} \\ 1 & \mathbf{a} & \mathbf{a}^2 \end{bmatrix} \begin{bmatrix} I_0 \\ I_p \\ I_n \end{bmatrix} \quad (2-3)$$

where $\mathbf{a} = e^{j2\pi/3} = 1\angle 120^\circ$, $\mathbf{a}^2 = 1\angle 240^\circ$

The IEC defines the load unbalance in terms of the sequence components. Equation (2-4) and Equation (2-5) give the two unbalance definitions.

$$Unbalance_0 = \frac{\text{zero sequence component}}{\text{positive sequence component}} \quad (2-4)$$

$$Unbalance_N = \frac{\text{negative sequence component}}{\text{positive sequence component}} \quad (2-5)$$

2.3 Circuit configurations

Various circuit configurations are investigated to find the best possible solution in controlling the output voltage waveform. These sine-wave inverter topologies consist of a voltage-source inverter with an LC filter to produce the sinusoidal output voltages. Voltage-source inverters are the preferred option due to fewer losses compared to current-source inverters and the high development status of IGBT technology. From [12] it is found that an M-leg inverter with an M-dimensional leg-voltage space can only produce an (M-1)-dimensional output-voltage space. With this in mind, a three-leg inverter can produce only 2 independent output voltages, making it necessary to use a four-leg inverter to produce three independent output voltages when unbalanced loads are used.

2.3.1 Single-phase inverters

Single-phase inverters are divided into half-bridge and full-bridge inverters. The advantages of the full-bridge inverter show that these inverters are usually preferred.

2.3.1.1 Half-bridge inverter

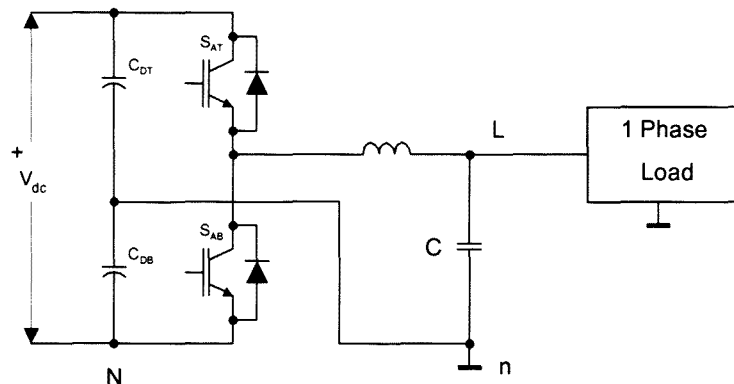


Figure 2.1: 1 ϕ Half-bridge inverter

The inverter shown in Figure 2.1 consists of only 1 leg and is called a half-bridge inverter. The switch voltage rating equals the dc-bus voltage. The output voltage of this inverter is half the dc-bus voltage, and is therefore usually preferred in low power applications. The full load current flows through the switches, which makes paralleling of devices necessary.

2.3.1.2 Full-bridge inverter

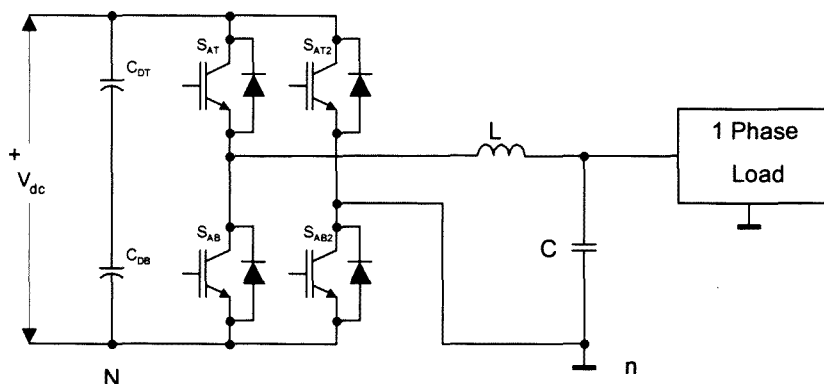


Figure 2.2: 1 ϕ Full-bridge inverter

The inverter shown in Figure 2.2 consists of 2 legs and is called a full-bridge inverter. This configuration is preferred in high-power applications, as the maximum output voltage equals the dc-bus voltage. For the same power level, the output current, and therefore the switch current, is less than other single-phase configurations, which would make paralleling of devices unnecessary.

2.3.2 Three-phase, three-wire inverter

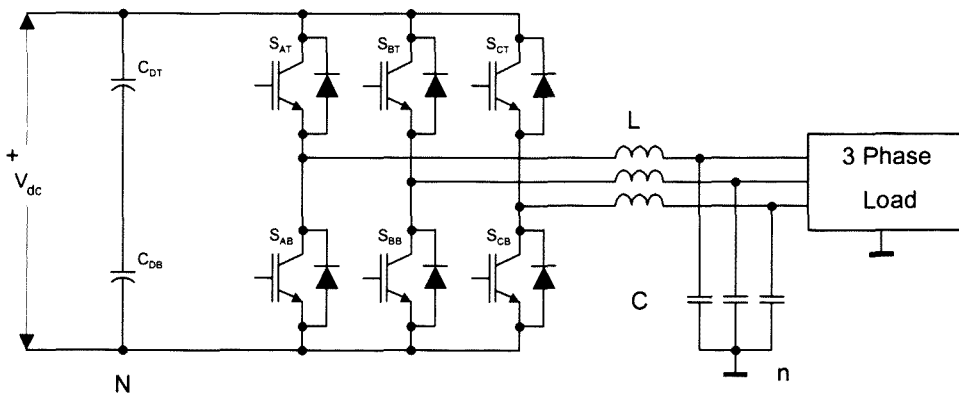


Figure 2.3: 3 ϕ Inverter with coupled outputs

This is the most popular converter topology used in industry today since loads at high power are predominantly three-phase. The three-leg inverter can generate only two independent output voltages, as the three phases are coupled. For this reason, this type of inverter is used when balanced three-phase loads are connected. There would be no path for any zero sequence currents to flow, implying that only balanced loads can be used. It should be noted that any load variations in the three-wire load configuration affects the entire dc-link and its capacitors. The coupling effect will cause the star-point to float, depending on the state of the switches. There are eight converter states, two of which are zero states that would force zero volts. This happens when either all the top (all ones) or all the bottom (all zeros) switches are on. The zero states help in minimizing the current ripple. Depending on the state of the switches, the forcing voltage can be any one of five values, 0 , $\pm \frac{1}{3}V_{dc}$ or $\pm \frac{2}{3}V_{dc}$, given in [12].

The inverter phase voltages (inverter output voltages, V_A , V_B and V_C), with respect to the load neutral, n , can be expressed as

$$V_{kn} = V_{kN} - V_{nN} \text{ with } k = A, B, C \quad (2-6)$$

If each load is represented by its simplified equivalent circuit with respect to the load neutral, and the induced back-emf's as e_{An} , e_{Bn} and e_{Cn} , Equation (2-6) can be expressed as

$$V_{kn} = L \frac{di_k}{dt} + e_{kn} \text{ with } k = A, B, C \quad (2-7)$$

In a balanced three-phase system it is known that

$$i_A + i_B + i_C = 0 \quad (2-8)$$

$$\frac{d}{dt}(i_A + i_B + i_C) = 0 \quad (2-9)$$

$$e_A + e_B + e_C = 0 \quad (2-10)$$

Substituting Equations (2-8), (2-9) and (2-10) into Equation (2-7), it is found that

$$\sum V_{kn} = L \sum \frac{di_k}{dt} + \sum e_{kn} \quad (2-11)$$

and therefore

$$V_{An} + V_{Bn} + V_{Cn} = 0 \quad (2-12)$$

Substituting Equation (2-12) into Equation (2-6), the load-neutral with respect to the negative dc-bus is

$$V_{nN} = \frac{1}{3}(V_{AN} + V_{BN} + V_{CN}) \quad (2-13)$$

From Equations (2-13) and (2-6), the inverter output voltages with respect to the load neutral can be converted to be measured with respect to the negative dc-bus as

$$\begin{bmatrix} V_{An} \\ V_{Bn} \\ V_{Cn} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} = \mathbf{T}_{ln3} \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} \quad (2-14)$$

Equation (2-14) shows that the maximum output of this configuration is equal to

$$\frac{2}{3}V_{dc}.$$

The leg voltages of the inverter are depicted using three orthogonal axes, representing a three-degree-of-freedom (3-DOF) system. This is shown in Figure 2.4.

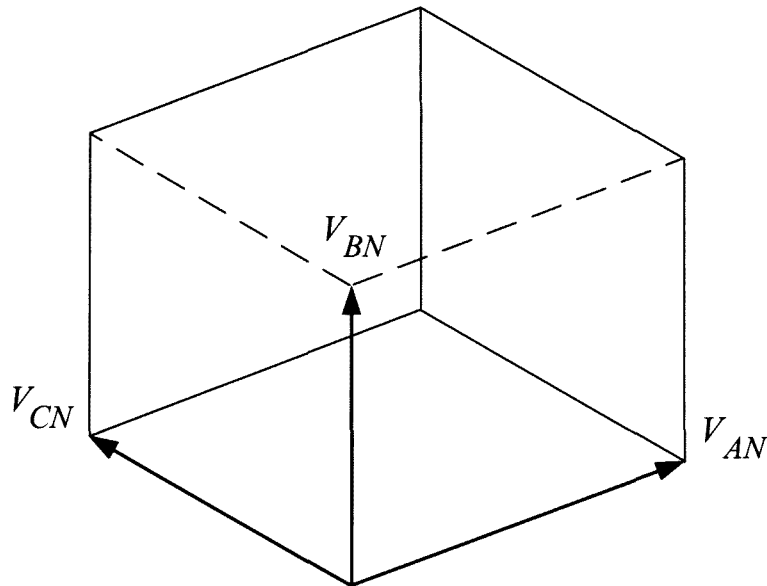


Figure 2.4: Leg-voltage space of a three-leg inverter

Because the 3-leg inverter can produce only 2 independent output voltages, the leg voltages are projected onto the stationary, 2-DOF, $\alpha\beta$ output-voltage space, shown in Figure 2.5. These voltages are now given with respect to the load neutral, n .

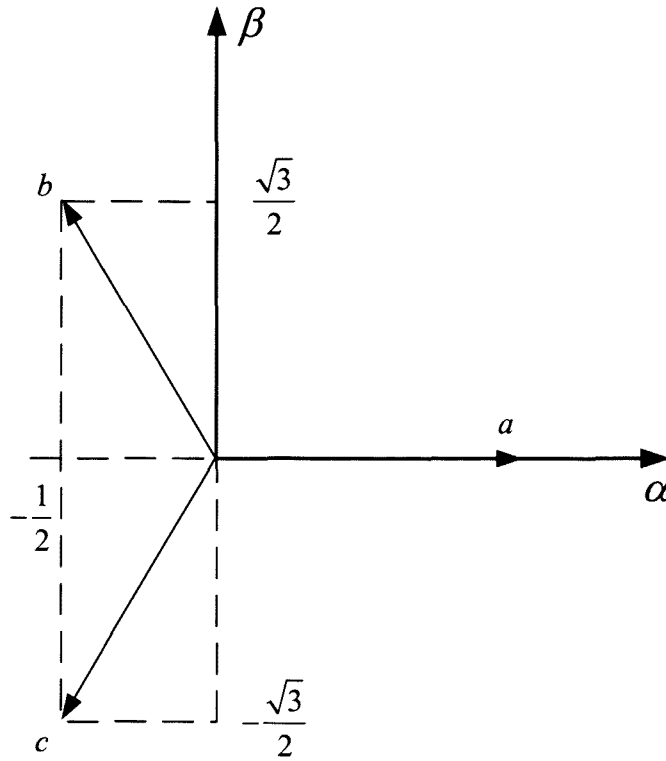


Figure 2.5: Primary voltage vectors in $\alpha\beta$ -plane

Mathematically, this is represented as

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} V_{An} \\ V_{Bn} \\ V_{Cn} \end{bmatrix} = \mathbf{T}_{\alpha\beta 0} \begin{bmatrix} V_{An} \\ V_{Bn} \\ V_{Cn} \end{bmatrix} \quad (2-15)$$

with V_0 being a placeholder to develop a square, invertible matrix, and to represent the loss of 1 degree-of-freedom. Furthermore, combining Equations (2-14) and (2-15), the leg-voltages are transformed to the $\alpha\beta$ -plane by using

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} = \mathbf{T}_{lg3} \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} \quad (2-16)$$

To calculate the necessary modulation values to produce the desired output voltages, the inverse of \mathbf{T}_{lg3} should be used to calculate the leg-voltages. In fact, \mathbf{T}_{lg3} is non-invertible. [12] suggests that the inverse of $\mathbf{T}_{\alpha\beta 0}$ could be used to perform this action. Then, manipulating Equation (2-16), the leg-voltages are found as

$$\begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} = [\mathbf{T}_{\alpha\beta 0}]^{-1} \begin{bmatrix} V_\alpha^* \\ V_\beta^* \\ V_0^* \end{bmatrix} \quad (2-17)$$

This is verified as

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_0 \end{bmatrix} = \mathbf{T}_{\alpha\beta 0} \mathbf{T}_{ln3} [\mathbf{T}_{\alpha\beta 0}]^{-1} \begin{bmatrix} V_\alpha^* \\ V_\beta^* \\ V_0^* \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_\alpha^* \\ V_\beta^* \\ V_0^* \end{bmatrix} \quad (2-18)$$

Equation (2-18) proves that the phase voltages are decoupled and that two independent single-phase circuits, as shown in Figure 2.6, can be used to represent a three-leg inverter. The values of L and C are given as $L = L_\alpha = L_\beta$ and $C = C_\alpha = C_\beta$ [12].

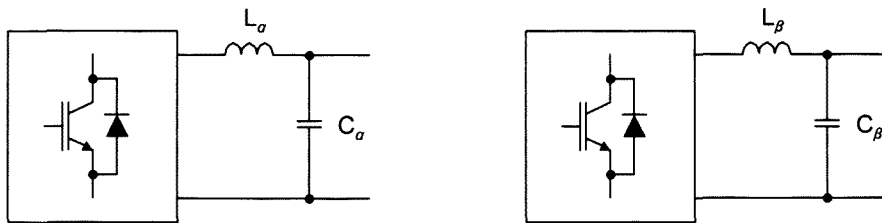


Figure 2.6: $\alpha\beta$ independent circuits

2.3.3 Three-phase, four-wire inverter

Connecting arbitrary loads, which may include balanced/unbalanced or linear/non-linear loads to the inverter, will cause zero-sequence currents to flow. These loads would therefore require a return ground connection. There are many configurations implementing a return ground path [12] - [14], each having its own advantages and disadvantages. These configurations include:

- a) splitting the dc-bus capacitors and using the centre point as the neutral,
- b) adding a fourth leg and using the centre point of the leg as the neutral, and
- c) a combination of the previous two.

In order to utilize the dc-bus voltage to maximum and to have better control (zero states) over the inverter, the four-leg configuration (b) is the preferred option.

2.3.3.1 Four-phase inverter with switched neutral

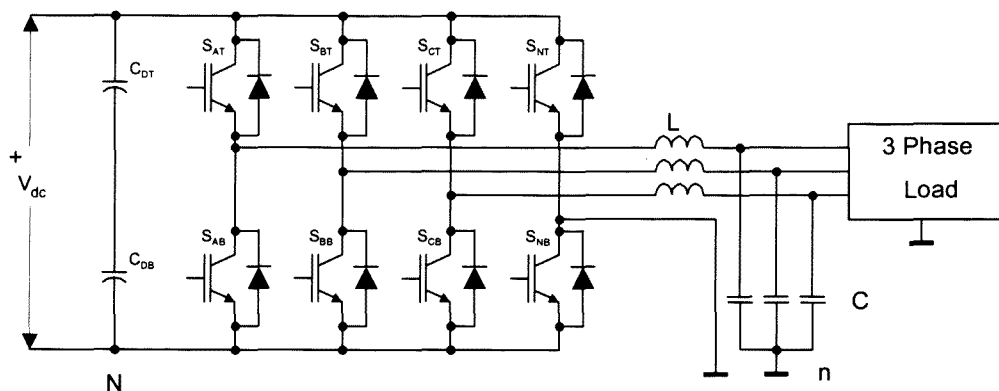


Figure 2.7: 3 ϕ Inverter with decoupled outputs

The star-point of the load/filter combination is connected to the output of a fourth phase-arm. It is therefore possible to force the star-point to any predetermined voltage, making the outputs of the three main phase-arms completely de-coupled, and therefore each phase can be controlled independently. The inverter output voltages with respect to the load neutral are converted to be measured with respect to the negative dc-bus with

$$\begin{bmatrix} V_{An} \\ V_{Bn} \\ V_{Cn} \\ V_{Nn} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & -1 \\ 0 & 1 & 0 & -1 \\ 0 & 0 & 1 & -1 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \\ V_{NN} \end{bmatrix} = \mathbf{T}_{ln4} \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \\ V_{NN} \end{bmatrix} \quad (2-19)$$

This time, V_{Nn} is used as the placeholder for the loss of 1 degree-of-freedom. The primary voltage vectors are projected onto the stationary, 3-DOF, $\alpha\beta 0$ output-voltage space, shown in Figure 2.8. These voltages are now given with respect to the load neutral, n .

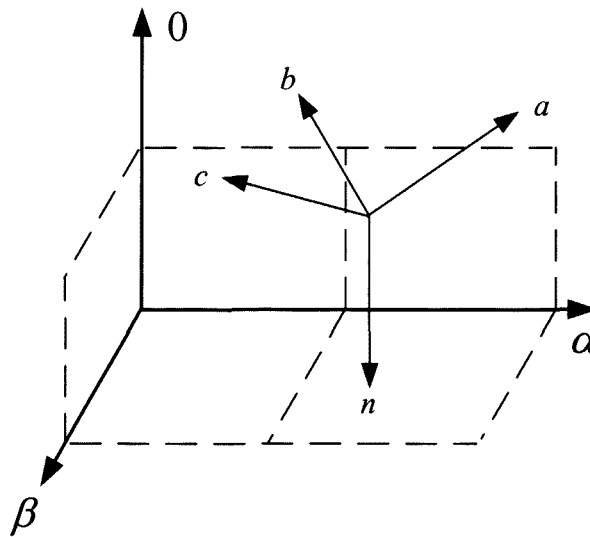


Figure 2.8: Primary voltage vectors in $\alpha\beta 0$ -plane

[12] showed that an extension of the $\alpha\beta$ -theory could be used to find a 4×4 matrix similar to the 3×3 matrix in Equation (2-15) as

$$\begin{bmatrix} V_{\alpha} \\ V_{\beta} \\ V_0 \\ V_z \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \\ \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & -\frac{3}{2\sqrt{2}} \\ \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} \end{bmatrix} \begin{bmatrix} V_{An} \\ V_{Bn} \\ V_{Cn} \\ V_{Nn} \end{bmatrix} = \mathbf{T}_{\alpha\beta 0z} \begin{bmatrix} V_{An} \\ V_{Bn} \\ V_{Cn} \\ V_{Nn} \end{bmatrix} \quad (2-20)$$

The bottom row of Equation (2-20) is found by completing the square where the row and column vectors are formed to be orthonormal. The leg-voltages of the 4-leg inverter are transformed to the $\alpha\beta 0$ -plane by combining Equations (2-19) and (2-20) to obtain

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_0 \\ V_z \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \\ \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & -\frac{3}{2\sqrt{2}} \\ \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & \frac{\sqrt{3}}{2\sqrt{2}} & -\frac{3\sqrt{3}}{2\sqrt{2}} \end{bmatrix} \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \\ V_{NN} \end{bmatrix} = \mathbf{T}_{lg4} \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \\ V_{NN} \end{bmatrix} \quad (2-21)$$

To calculate the necessary modulation values, which will produce the desired output voltages, [12] shows that the inverse of $\mathbf{T}_{\alpha\beta 0z}$ could be used to find the leg-voltages as

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_0 \\ V_z \end{bmatrix} = [\mathbf{T}_{\alpha\beta 0z}]^{-1} \begin{bmatrix} V_\alpha^* \\ V_\beta^* \\ V_0^* \\ V_z^* \end{bmatrix} \quad (2-22)$$

which can be verified by

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_0 \\ V_z \end{bmatrix} = \mathbf{T}_{\alpha\beta 0z} \mathbf{T}_{ln4} [\mathbf{T}_{\alpha\beta 0z}]^{-1} \begin{bmatrix} V_\alpha^* \\ V_\beta^* \\ V_0^* \\ V_z^* \end{bmatrix} \quad (2-23)$$

Due to the independency of the phases, the $\alpha\beta 0$ -values are controlled as three single-phase circuits. This is shown in Figure 2.9. The values of L and C are given as $L = L_\alpha = L_\beta = L_0$ and $C = C_\alpha = C_\beta = C_0$ [12].

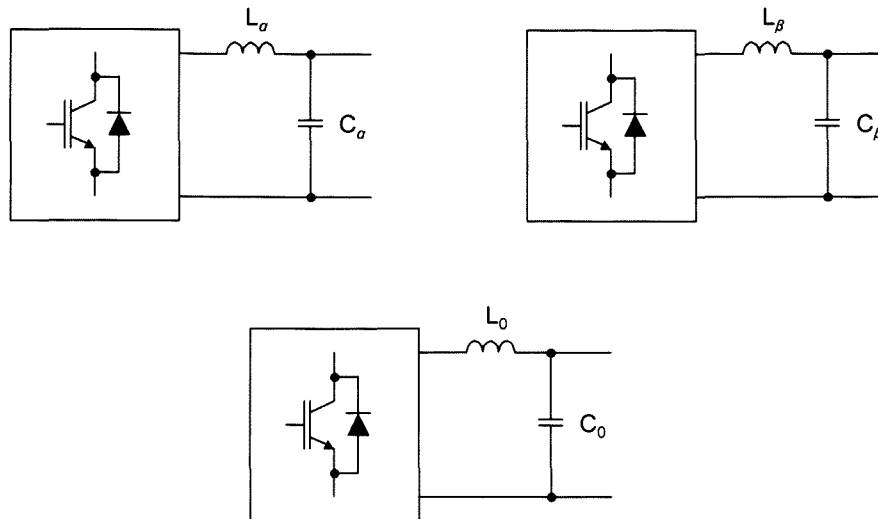


Figure 2.9: Independent phase-controllers

The converter can handle zero-sequence currents and the addition of the fourth phase-arm allows for smaller values of dc-bus capacitors, as the neutral current does not have to be absorbed by the dc-bus capacitors.

2.4 Control system theory

It was discovered long ago that control is necessary to achieve satisfactory response from a process often referred to as a plant. By “satisfactory response” is meant that the output of the plant follows the reference input, in spite of any disturbances that might be present, or any error that may occur in the sensors [42]. Furthermore, the robustness of a system depends on how well disturbances are rejected and how sensitive the system is to parameter variations. It is shown in [34] - [36] and [42] that the use of feedback has many advantages in designing a robust control system. In spite of this, many controllers are still based on the open-loop control strategy. By this is meant that the control action is independent of the output, as the output is neither measured nor fed back to be compared to the input, forming an error signal. In other words, there will only be one operating condition for every reference input, and the controller would thus be prone to any internal or external disturbances. Having said this, it is seen that open-loop controllers apply a single corrective effort

and assume that the desired results will be achieved. The principal drawback of open-loop control is loss of accuracy. Without feedback, there is no guarantee that the control inputs applied to the process will actually have the desired effect.

In contrast with the open-loop controller, a closed-loop control system is one in which the output signal has a direct effect on the control action. The output is fed back to create an actuating error signal by subtracting the output from the reference input. This error signal is fed to the controller in an effort to reduce the error and get the output of the system as close to the desired value as possible. A big advantage of a closed-loop controller is that by using feedback, the system response is less prone to any disturbances. But with this advantage comes a few disadvantages. Stability can be a big problem, as the controller can overcorrect errors, which may cause oscillations [35]. A feedback controller also has to wait until the effects of its latest efforts are measurable before it decides on the next appropriate control action that can be a great drawback when time is very critical. Care has to be taken to ensure that measurements are taken at the right time to ensure the best possible output for the system.

Thus, it is clear that a closed-loop controller would ensure the best possible output for a certain system. The rest of this thesis is devoted to combining various control strategies and finally finding a controller that would result in a system with a voltage waveform having as low as possible THD. The following sections will give the background on the techniques required to understand the design of the controller.

2.4.1 Controllability

A system is said to be controllable at $t = t_0$, if for any initial state, $x(t_0) = x_0$ and desired final state x_f , there exists a finite time t_f and a control $u(t)$ - where t lies in $[t_0, t_f]$ and $u(t)$ is an unconstrained control vector - which transfers the state of the system from $x(t_0) = x_0$ to $x(t_f) = x_f$ [35]. A control law can therefore be used to shift the poles of a system to any location in order to achieve the desired specifications. If the system is uncontrollable, it would be unaffected by the control.

Consider the continuous-time system

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}u \quad (2-24)$$

where

\mathbf{x} = state vector

u = control signal

\mathbf{A} = $n \times n$ matrix

\mathbf{B} = $n \times 1$ matrix

For simplicity's sake, assume that the initial time is zero, and that the final state is the origin. Now, the solution of Equation (2-24) is [34]

$$\mathbf{x}(t) = e^{\mathbf{A}t} \mathbf{x}(0) + \int_0^t e^{\mathbf{A}(t-\tau)} \mathbf{B}u(\tau) d\tau \quad (2-25)$$

Applying the given conditions

$$\mathbf{x}(t_1) = 0 = e^{\mathbf{A}t_1} \mathbf{x}(0) + e^{\mathbf{A}t_1} \int_0^{t_1} e^{-\mathbf{A}\tau} \mathbf{B}u(\tau) d\tau$$

$$\mathbf{x}(0) = - \int_0^{t_1} e^{-\mathbf{A}\tau} \mathbf{B}u(\tau) d\tau \quad (2-26)$$

[35] and [36] showed that the function $e^{\mathbf{A}t}$ can be converted into a polynomial of the matrix \mathbf{A} as follows:

$$e^{\mathbf{A}t} = \alpha_0(t)\mathbf{I} + \alpha_1(t)\mathbf{A} + \alpha_2(t)\mathbf{A}^2 + \dots + \alpha_{n-1}(t)\mathbf{A}^{n-1} \quad (2-27)$$

and, manipulating Equation (2-27)

$$e^{-\mathbf{A}\tau} = \sum_{k=0}^{n-1} \alpha_k(\tau) \mathbf{A}^k \quad (2-28)$$

Now, substituting Equation (2-28) into Equation (2-26)

$$\mathbf{x}(0) = - \sum_{k=0}^{n-1} \mathbf{A}^k \mathbf{B} \int_0^{t_1} \alpha_k(\tau) u(\tau) d\tau \quad (2-29)$$

In order to simplify the equation, substitute

$$\beta_k = \int_0^{t_1} \alpha_k(\tau)u(\tau)d\tau \quad (2-30)$$

and then

$$\mathbf{x}(0) = -\sum_{k=0}^{n-1} \mathbf{A}^k \mathbf{B} \beta_k$$

$$\mathbf{x}(0) = -\begin{bmatrix} \mathbf{B} & \mathbf{A}\mathbf{B} & \dots & \mathbf{A}^{n-1}\mathbf{B} \end{bmatrix} \begin{bmatrix} \beta_0 \\ \beta_1 \\ \dots \\ \beta_{n-1} \end{bmatrix} \quad (2-31)$$

From Equation (2-31), $\begin{bmatrix} \mathbf{B} & \mathbf{A}\mathbf{B} & \dots & \mathbf{A}^{n-1}\mathbf{B} \end{bmatrix}$ is defined as the controllability matrix. The system is completely state controllable if the controllability matrix has a rank of n . This means that that the controllability matrix has n linearly independent rows or columns.

2.4.2 Stability

A system that always gives the appropriate response to a certain control signal is considered to be stable [36]. The system has to remain in a state of operating equilibrium under normal operating conditions and regain an acceptable state of equilibrium after being subjected to a disturbance. For all systems, linear and non-linear, there exist a variety of stability checks that can be performed to ensure stable working conditions. The stability checks that will be utilized in this thesis will now be discussed.

2.4.2.1 Routh's Stability criterion

The characteristic equation of any system is defined in [36] as

$$a(s) = s^j + a_1s^{j-1} + a_2s^{j-2} + \dots + a_{j-1}s + a_j \quad (2-32)$$

or, equivalently

$$a(s) = (s + c_0)(s + c_1)...(s + c_{j-1})(s + c_j) \quad (2-33)$$

where a_j is the co-efficients and c_j is the roots of the characteristic equation.

The roots of this polynomial will give the poles of the system. A necessary condition for a system to be stable is that all poles have negative real parts, therefore lying in the left-hand plane of an s-plane plot. This translates to the condition where all the a_j 's in Equation (2-32) are positive and non-zero. If any coefficients were zero or negative the system would become unstable.

Routh's Stability criterion requires the computation of a triangular array that is a function of the a_j 's in Equation (2-32). This will give an indication of the stability without actually computing the roots.

Table 2.1: Routh's array

row n	s^j	1	a_2	a_4	...
row $(j - 1)$	s^{j-1}	a_1	a_3	a_5	...
row $(j - 2)$	s^{j-2}	b_1	b_2	b_3	...
row $(j - 3)$	s^{j-3}	c_1	c_2	c_3	...
:	:	:	:	:	*
row 2	s^2	*	*	*	
row 1	s	*	*		
row 0	s^0	*			

The elements of row $(j - 2)$ and below, (b_j, c_j, \dots), are formed by finding the determinant, which consists of the two elements in the first column and elements from successive columns of the previous two rows. Routh showed that a necessary and sufficient condition for stability is that the elements in the first column of the triangular array are all positive. If these elements were not all positive, the number of sign changes would equal the number of poles in the right-hand plane.

2.4.2.2 Pole-Zero map

It was already shown in Section 2.4.2.1 that a system would be stable if the real part of the poles is negative. It is given in [36] that the relationship between the frequency domain and the discrete domain is $z = e^{sT}$. This means that the left hand plane of a frequency plot would translate to a circle of radius equal to one in the discrete domain, as shown in Figure 2.10. The system would therefore be stable if the poles are confined within the circle.

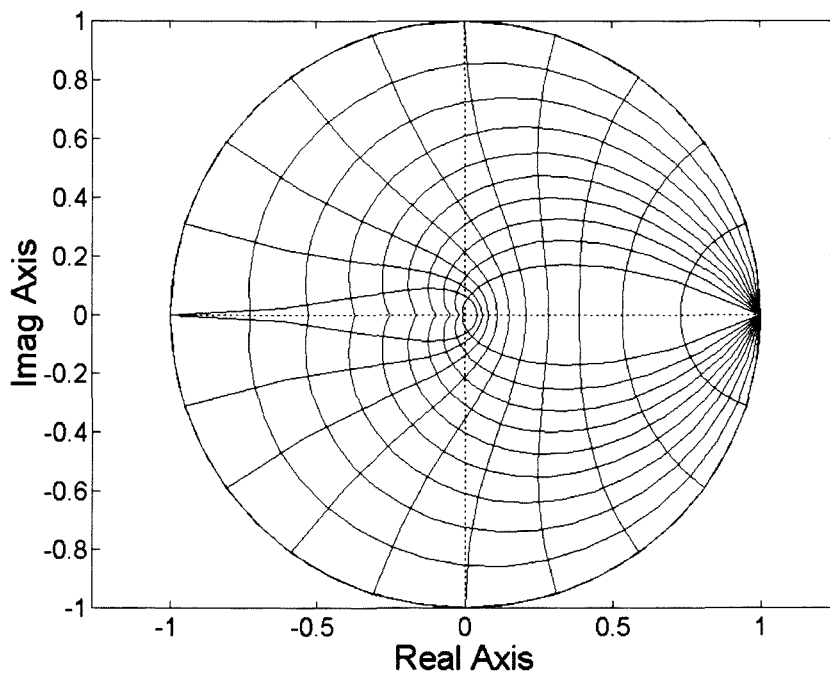


Figure 2.10: Pole-Zero map

2.4.3 State-space models for systems with delay

In the discrete time domain, the digital system operates on the samples of the sensed plant output. A zero-order hold (ZOH) is used to maintain a specific voltage throughout a sample period, defined mathematically as

$$u(\tau) = u(kT), \quad kT \leq \tau \leq kT + T \quad (2-34)$$

With the inclusion of the time delay, it will be shown how the state-space representation of the system has to be modified to accommodate this. It is assumed

that the time delay is present in the control signal, $u(t)$. The state equations will now be

$$\begin{aligned}\dot{\mathbf{x}}(t) &= \mathbf{A}\mathbf{x}(t) + \mathbf{B}u(t - \tau) \\ y &= \mathbf{C}\mathbf{x}\end{aligned}\tag{2-35}$$

To get the solution of Equation (2-35), Equation (2-25) is modified to include the time delay, such that

$$\begin{aligned}\mathbf{x}(kT + T) &= e^{\mathbf{A}T}\mathbf{x}(kT) + \int_{kT}^{kT+T} e^{\mathbf{A}(kT+T-\tau)}\mathbf{B}u(\tau - \lambda)d\tau \\ t_0 &= kT, \quad t = kT + T\end{aligned}\tag{2-36}$$

Substituting $\eta = kT + T - \tau$ for τ , Equation (2-36) is modified to

$$\begin{aligned}\mathbf{x}(kT + T) &= e^{\mathbf{A}T}\mathbf{x}(kT) + \int_0^T e^{\mathbf{A}\eta}\mathbf{B}u(kT + T - \lambda - \eta)d\eta \\ &\text{with } d\tau = -d\eta\end{aligned}\tag{2-37}$$

To consider any delay shorter than one sample period, the system delay, λ , can be taken as a fraction of a sample period, mT . Therefore,

$$\begin{aligned}\lambda &= mT \\ 0 &\leq m \leq 1\end{aligned}\tag{2-38}$$

Equation (2-37) is updated to give the new discrete system as

$$\mathbf{x}(kT + T) = e^{\mathbf{A}T}\mathbf{x}(kT) + \int_0^T e^{\mathbf{A}\eta}\mathbf{B}u(kT + T - mT - \eta)d\eta\tag{2-39}$$

The integral in Equation (2-39) is explained using Figure 2.11.

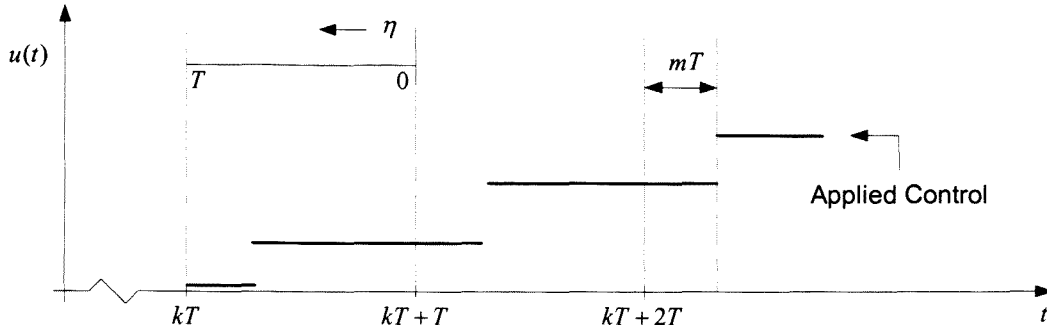


Figure 2.11: Piecewise control input with time delay

The integral is taken from $\eta = 0$ to $\eta = T$, which corresponds to $t = kT + T$ taken backwards to $t = kT$. Therefore, as the control signal is a piecewise defined quantity in the discrete domain, Equation (2-39) can be split into two parts:

$$\mathbf{x}(kT + T) = e^{AT} \mathbf{x}(kT) + \int_0^{T-mT} e^{A\eta} \mathbf{B}u(kT) d\eta + \int_{T-mT}^T e^{A\eta} \mathbf{B}u(kT - T) d\eta$$

$$\mathbf{x}(kT + T) = \mathbf{\Phi} \mathbf{x}(kT) + \mathbf{\Gamma}_1 u(kT - T) + \mathbf{\Gamma}_2 u(kT) \quad (2-40)$$

by defining

$$\mathbf{\Phi} = e^{AT}$$

$$\mathbf{\Gamma}_1 = \int_{T-mT}^T e^{A\eta} \mathbf{B} d\eta$$

$$\mathbf{\Gamma}_2 = \int_0^{T-mT} e^{A\eta} \mathbf{B} d\eta \quad (2-41)$$

The equation in (2-40) can be evaluated. It is seen that the states are only affected by the previous and present sample, respectively. Thus, the system is said to be causal, as defined in [43]: A system is said to be causal if *the output at any time depends only on present and previous inputs*. To get the state-space form, it is necessary to evaluate the equations in (2-41). $\mathbf{\Gamma}_1$ is converted to the form of $\mathbf{\Gamma}_2$ by setting $\sigma = \eta - T + mT$, and then factorising out the constant matrix, \mathbf{B}

$$\mathbf{\Gamma}_1 = e^{A(T-mT)} \int_0^{mT} e^{A\sigma} d\sigma \mathbf{B} \quad (2-42)$$

For notational purposes, define, for any positive nonzero scalar number, a , the two matrices

$$\Phi(a) = e^{Aa}, \quad \Psi(a) = \frac{1}{a} \int_0^a e^{A\sigma} d\sigma \quad (2-43)$$

By combining Equation (2-41) and Equation (2-43), Γ_1 and Γ_2 are found in terms of Φ and Ψ . Therefore

$$\begin{aligned} \Gamma_1 &= e^{A(T-mT)} \int_0^{mT} e^{A\sigma} d\sigma \mathbf{B} \\ &= \left[e^{A(T-mT)} \right] [mT] \left[\frac{1}{mT} \int_0^{mT} e^{A\sigma} d\sigma \right] \mathbf{B} \\ &= [\Phi(T-mT)] [mT] [\Psi(mT)] \mathbf{B} \\ &= mT \cdot \Phi(T-mT) \cdot \Psi(mT) \cdot \mathbf{B} \end{aligned} \quad (2-44)$$

and

$$\begin{aligned} \Gamma_2 &= \int_0^{T-mT} e^{A\eta} d\eta \mathbf{B} \\ &= [T-mT] \left[\frac{1}{T-mT} \int_0^{T-mT} e^{A\eta} d\eta \right] \mathbf{B} \\ &= [T-mT] [\Psi(T-mT)] \mathbf{B} \\ &= (T-mT) \cdot \Psi(T-mT) \cdot \mathbf{B} \end{aligned} \quad (2-45)$$

Further, by using a modification of Equation (2-27), and expanding Equation (2-43), the following equations are obtained:

$$\Phi(a) = e^{Aa} = \sum_{k=0}^{\infty} \frac{\mathbf{A}^k a^k}{k!} \quad (2-46)$$

$$\begin{aligned}
 \Psi(a) &= \frac{1}{a} \int_0^a \sum_{k=0}^{\infty} \frac{\mathbf{A}^k \sigma^k}{k!} d\sigma \\
 &= \frac{1}{a} \sum_{k=0}^{\infty} \frac{\mathbf{A}^k}{k!} \frac{a^{k+1}}{k+1} \\
 &= \sum_{k=0}^{\infty} \frac{\mathbf{A}^k a^k}{(k+1)!}
 \end{aligned} \tag{2-47}$$

Equation (2-27) can also be written as

$$\Phi(a) = \mathbf{I} + \sum_{k=1}^{\infty} \frac{\mathbf{A}^k a^k}{k!} \tag{2-48}$$

Substituting $k = j + 1$, Equation (2-48) becomes

$$\begin{aligned}
 \Phi(a) &= \mathbf{I} + \sum_{j=0}^{\infty} \frac{\mathbf{A}^{j+1} a^{j+1}}{(j+1)!} \\
 &= \mathbf{I} + \sum_{j=0}^{\infty} \frac{\mathbf{A}^j a^j}{(j+1)!} a \mathbf{A} \\
 &= \mathbf{I} + a \Psi(a) \mathbf{A}
 \end{aligned} \tag{2-49}$$

Therefore, using Equation (2-43) and Equation (2-49), the two matrices are given as

$$\begin{aligned}
 \Phi(a) &= e^{\mathbf{A}a} \\
 \Phi(a) &= \mathbf{I} + a \Psi(a) \mathbf{A}
 \end{aligned} \tag{2-50}$$

Now, for $0 \leq m \leq 1$, the discrete state equation is represented as

$$\mathbf{x}(k+1) = \Phi \mathbf{x}(k) + \Gamma_1 u(k-1) + \Gamma_2 u(k) \tag{2-51}$$

It is desirable to eliminate the $u(k-1)$ term from the right hand side of Equation (2-51), which is done by defining a new state variable, $\epsilon(k) = u(k-1)$. The new state equations, with an increased dimension of the states, are

$$\begin{aligned}
 \begin{bmatrix} \mathbf{x}(k+1) \\ \epsilon(k+1) \end{bmatrix} &= \begin{bmatrix} \Phi & \Gamma_1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \mathbf{x}(k) \\ \epsilon(k) \end{bmatrix} + \begin{bmatrix} \Gamma_2 \\ 1 \end{bmatrix} u(k) \\
 y(k) &= [\mathbf{H} \quad 0] \begin{bmatrix} \mathbf{x}(k) \\ \epsilon(k) \end{bmatrix}
 \end{aligned} \tag{2-52}$$

To summarize, by including a time delay in the control action of a system will change the state-space equations to those defined in Equation (2-52), with variables being calculated as

$$\Phi(a) = e^{Aa}$$

$$\Psi(a) = \frac{1}{a} [\Phi(a) - \mathbf{I}] \mathbf{A}^{-1}$$

$$\Gamma_1 = mT \cdot \Phi(T - mT) \cdot \Psi(mT) \cdot \mathbf{B}, \quad \Gamma_2 = (T - mT) \cdot \Psi(T - mT) \cdot \mathbf{B} \quad (2-53)$$

2.4.4 Deadbeat control

The idea of controlling systems that evolve in time is found everywhere. These controllers are implemented using high-speed digital signal processors, and therefore calculations are done in the discrete time domain. Many of these processes are dependent on the time in which a certain variable can be controlled, and for this reason much research has been done on time optimal control systems [7]. One such technique is known as *deadbeat control*. With this type of control it is necessary to *find a constant state feedback control that drives any state to the origin in a minimum number of time steps*. In the digital time domain the stability of a system is confined within a circle of radius equal to one [35] - [37]. The settling time is found to be inversely proportional to the magnitude of the real part of the pole, which maps to the radius of the pole in the z-plane [42]. Therefore, the fastest response that can be achieved would be for the poles to lie in the middle of the circle, or $z^n = 0$. A deadbeat controller would thus drive any error to zero in at most n sampling periods, with the settling time at most nh , with h being the sampling period. One disadvantage of a deadbeat controller is that the magnitude of the control signal is inversely proportional to the sampling period [7], [37]. This is because when the sampling period decreases, the time available for deadbeating will also decrease. The control effort, or signal, will therefore increase to eliminate the error in the shorter amount of time. Consequently, the only design parameter in a deadbeat controller is the sampling period, and a trade-off between the minimization of the deadbeat steps and the optimization of robustness should be made.

2.4.5 The control law, $u = -\mathbf{K}\mathbf{x}$

The mentioned control law is the feedback of a linear combination of the state variables. The control law is necessary to assign a set of pole locations to a closed-loop system that would result in satisfactory dynamic response. An n -th order system would require a K -vector of length n to be able to arbitrarily select the desired pole locations. If the desired poles are given as $s = s_1, s_2, \dots, s_n$, \mathbf{K} is determined by matching the coefficients of the characteristic equation of the poles,

$$a_c(s) = (s - s_1)(s - s_2)\dots(s - s_n) = 0 \quad (2-54)$$

with the characteristic equation of the closed-loop system [36],

$$\det[s\mathbf{I} - (\mathbf{A} - \mathbf{BK})] = 0 \quad (2-55)$$

This would effectively force the system's characteristic equation to equal the desired characteristic equation, and consequently, the closed-loop poles will be placed at the desired locations.

2.4.6 The reference input

When introducing a reference into the system, the control will change to $u = -\mathbf{K}\mathbf{x} + r$. This will result in a non-zero steady-state error on the output when introducing a step input. It is therefore necessary to compute the steady-state values of the control input as well as the states, which will give zero output error, and then force the control and the states to take these values. The desired final values are now defined as u_{ss} and \mathbf{x}_{ss} , which will give a new control law,

$$u = u_{ss} - \mathbf{K}(\mathbf{x} - \mathbf{x}_{ss}) \quad (2-56)$$

From Equation (2-56) it is seen that if there is no error, $\mathbf{x} = \mathbf{x}_{ss}$, the control signal, u , will be $u = u_{ss}$. Now for any control input, the steady-state system equations are given as

$$\mathbf{x}_{ss} = \Phi \mathbf{x}_{ss} + \Gamma \mathbf{u}_{ss} \Rightarrow (\Phi - \mathbf{I}) \mathbf{x}_{ss} + \Gamma \mathbf{u}_{ss} = \mathbf{0}$$

$$\mathbf{y}_{ss} = \mathbf{H} \mathbf{x}_{ss} \tag{2-57}$$

For the system to have zero error for any applied input, the output must be $\mathbf{y}_{ss} = \mathbf{r}_{ss}$.

This is done by defining $\mathbf{x}_{ss} = \mathbf{N}_x \mathbf{r}_{ss}$ and $\mathbf{u}_{ss} = \mathbf{N}_u \mathbf{r}_{ss}$. Equation (2-57) is now updated to:

$$(\Phi - \mathbf{I}) \mathbf{N}_x \mathbf{r}_{ss} + \Gamma \mathbf{N}_u \mathbf{r}_{ss} = \mathbf{0}$$

$$\mathbf{y}_{ss} = \mathbf{H} \mathbf{x}_{ss} \tag{2-58}$$

Equation (2-58) shows that the relation will hold for any applied control input. Now, to put Equation (2-58) in matrix form, it is found that

$$\begin{bmatrix} \Phi - \mathbf{I} & \Gamma \\ \mathbf{H} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \mathbf{N}_x \\ \mathbf{N}_u \end{bmatrix} = \begin{bmatrix} \mathbf{0} \\ \mathbf{1} \end{bmatrix} \tag{2-59}$$

Finally, to get the N-vector

$$\begin{bmatrix} \mathbf{N}_x \\ \mathbf{N}_u \end{bmatrix} = \begin{bmatrix} \Phi - \mathbf{I} & \Gamma \\ \mathbf{H} & \mathbf{0} \end{bmatrix}^{-1} \begin{bmatrix} \mathbf{0} \\ \mathbf{1} \end{bmatrix} \tag{2-60}$$

The complete control system is given in Figure 2.12.

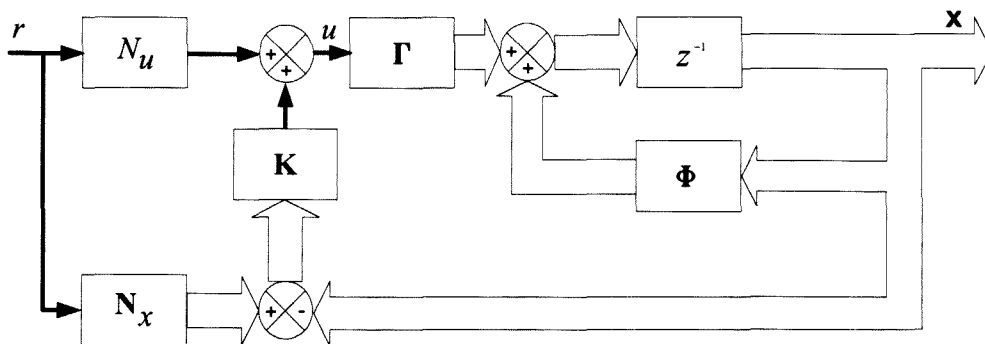


Figure 2.12: The reference input with full-state feedback

2.4.7 PI Controller

Another way of ensuring that the steady-state error is eliminated is by using a PI controller, also known as a lag compensator [36]. A lag compensator will reduce the steady-state error, as past errors will charge up the integrator to some value that will remain, even if the error becomes zero. It is thus possible to cancel disturbances with zero error (e), as e no longer has to be finite to produce a control that will counteract the (constant) disturbance. The transfer function of a PI controller is given in [34]:

$$PI_{tf} = \frac{K_i + sK_v}{s} \quad (2-61)$$

and is included in the system as shown in Figure 2.13.

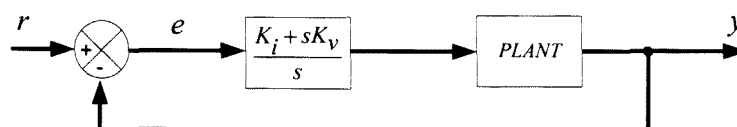


Figure 2.13: PI Controller eliminating the steady-state error

It is mentioned in [36] that proportional feedback control can reduce error responses to disturbances, but that a non-zero steady-state error will still be present and has to be compensated for. Proportional feedback, K_v , also increases the speed of response, but has a much larger transient overshoot. By including a term proportional to the integral of the error, K_i , it is possible to eliminate the steady-state error, with the disadvantage of a further deterioration in the dynamic response. These effects of increasing the different control variables, K_v and K_i , on a closed-loop system, are summarized in Table 2.2. It should be noted that these correlations are only to be used as a reference, as variables are dependent on each other, and changing one may affect the other.

Table 2.2: Effects of the different control variables on a closed-loop system

CL Response	Rise Time	Overshoot	Settling Time	S-S Error
K_v	Decrease	Increase	Small Change	Decrease
K_i	Decrease	Increase	Increase	Eliminate

There are 4 basic steps in designing a PI controller, which include the following:

- 1) Find the open-loop transfer function of the plant
- 2) Introduce a step input to the open-loop plant
- 3) Add the PI controller and close the loop
- 4) Find values for K_v and K_i to get the desired response.

2.4.8 Disturbance elimination

A disturbance is defined as *a signal that tends to adversely affect the value of the output of a system* [35]. It can also be seen as a change in a specific signal, which would deteriorate the performance of the plant. A disturbance affecting the plant is shown in Figure 2.14.

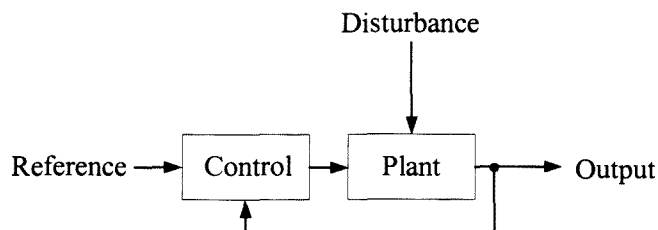


Figure 2.14: Disturbance affecting plant

Disturbances are usually sensed at the output after they happened, due to various time delays through the system. The controller would therefore not react until an error is detected, and it may happen that a specific value cannot be brought back into allowable limits. These undesirable conditions can be eliminated in various ways [3], [15], with feed-forward control being considered as a useful method in accomplishing this [35]. With feed-forward control, the error is compensated for before it happens.

This is advantageous, as corrective measures are usually taken after the output has been affected, which is not the case here. As soon as a disturbance occurs, the corrective measure is taken simultaneously, and the output is not affected.

Such a disturbance eliminator is shown in Figure 2.15. Suppose that the plant transfer function, $G(s)$, and the disturbance transfer function, $G_n(s)$, are both known. With a controller transfer function, $G_c(s)$, which can be designed using a variety of control techniques, it is possible to design a disturbance feed-forward transfer function, $G_1(s)$, that will eliminate the disturbance effect.

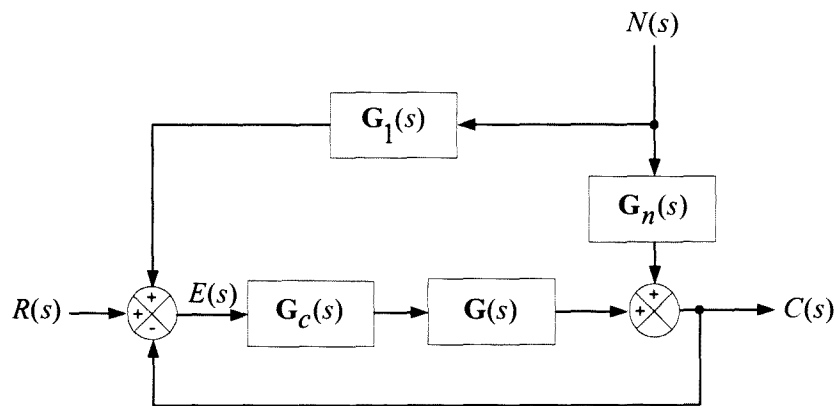


Figure 2.15: Disturbance eliminator

From the diagram in Figure 2.15 it is seen that the output, $C(s)$, is given by

$$C(s) = G_c(s)G(s)E(s) + G_n(s)N(s) \quad (2-62)$$

where

$$E(s) = R(s) - C(s) + G_1(s)N(s) \quad (2-63)$$

Substituting (2-63) in (2-62), the output is given as

$$C(s) = G_c(s)G(s)[R(s) - C(s)] + [G_c(s)G(s)G_1(s) + G_n(s)]N(s) \quad (2-64)$$

The effect that $N(s)$ has on the output can therefore be eliminated if $G_c(s)$ is chosen such that

$$G_c(s)G(s)G_1(s) + G_n(s) = 0 \quad (2-65)$$

or, similarly

$$G_1(s) = -\frac{G_n(s)}{G_c(s)G(s)} \quad (2-66)$$

If the controller transfer function, $G_c(s)$, is now properly designed, the system will give the desired performance. The disturbance feed-forward transfer function, $G_1(s)$, can thus be obtained by Equation (2-66).

2.5 Summary

Chapter 2 showed various circuit configurations that are used in inverter applications. Three-phase, three-wire systems are commonly used, but are unable to produce three independent voltages, and can therefore not be used for supplying power to zero-sequence unbalanced loads. This drawback is overcome by implementing a three-phase, four-wire configuration that has a fourth leg to handle neutral currents, which would arise when unbalanced loads are used. It was further shown that both these configurations could be converted to the $\alpha\beta 0$ -plane to produce respectively two and three independent, single-phase circuits. A system model is thus found by converting the given system into the $\alpha\beta 0$ -plane. Separate single-phase controllers, all with the same circuit parameters, are then used to control both the three-wire and four-wire circuits.

Section 2.4 onwards combines various control strategies to finally find a controller that would result in a system with a voltage waveform with a low THD.

In this thesis classical and modern control techniques have been investigated to develop control systems. Both classical and modern control techniques have their advantages and disadvantages, and depending on the application, either design technique will render satisfactory results. The following factors may help on determining which type of control technique should be used:

- Classical transfer functions relates the input / output characteristics of a system. Any internal behavior between system variables is lost. Alternatively, modern control uses the state-space approach, which provides a complete interrelationship between the system variables. Higher-order systems can therefore be handled easier by implementing modern control.
- Due to the interrelationship of the system variables modern controllers are more dependent on the accuracy of the system model. There exist techniques to apply model-uncertainties, whereby a more robust system can be designed.

- In modern control techniques, higher-order systems are represented as first order differential equations, whereas in classical control techniques higher-order differential equations is used. Because first order differential equations are easily analysed with computer packages they are usually preferred to simplify the operations needed for development of the controller.
- Pure time delays are easily handled in the classical techniques because it can be represented by a transfer function. Alternatively, with modern control techniques it is more difficult to represent the time delay because the system equations must be changed.
- Controllers developed with the classical techniques can be implemented in the analog as well as the digital domain, whereas controllers developed with the modern control techniques are usually implemented in the digital domain.

Thus, the above-mentioned factors show that the type of control technique implemented is dependent on the system that has to be controlled. For completeness, both design techniques are investigated in this thesis. Although the classical control technique is usually implemented in the analog domain, both controllers are represented in the digital domain to be implemented in a DSP.

Design using the classical control techniques is investigated in Chapter 3, whereas modern control techniques are handled in Chapter 4.

Chapter 3

Design Using Classical Control Techniques

3 Design Using Classical Control Techniques

3.1 Introduction

Classical control techniques use transfer functions to design an appropriate control system. Figure 3.1 shows the basic feedback configuration for a stable or unstable system. It consists of a plant, G , and a disturbance signal, w . A compensator, D , needs to be designed and driven by a reference signal, r , which is to be followed by the plant output, y . The output is measured, including any sensor noise, n , which in turn is subtracted from the reference signal. Disturbance signals get reflected to the output.

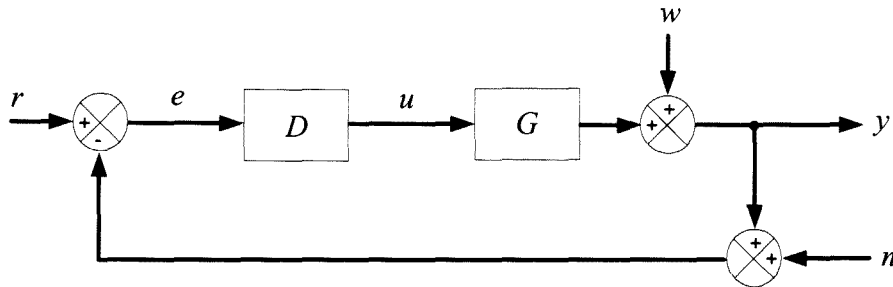


Figure 3.1: Basic feedback configuration

In order to develop a control system that is insensitive to noise and disturbances, it is necessary to define special functions to incorporate the sensitivity of a closed-loop control system. One of the main objectives of the control system in Figure 3.1 is to keep the tracking error, $e = r - y$, small for a reference input excitation and to keep the output, y , small for a disturbance input, w . With Figure 3.1, the input-output relationship is found to be

$$\begin{aligned} y &= w + DG(r - n - y) \\ &= DG(1 + DG)^{-1}(r - n) + (1 + DG)^{-1}w \end{aligned} \quad (3-1)$$

and the tracking error

$$e = r - y = (1 + DG)^{-1}(r - w) + DG(1 + DG)^{-1}n \quad (3-2)$$

From Equations (3-1) and (3-2) the sensitivity function, S , and the complementary sensitivity function, T , is defined as:

$$S(s) = (1 + DG)^{-1}$$

$$T(s) = (1 + DG)^{-1} DG \tag{3-3}$$

The sensitivity function relates to disturbance rejection properties, while the complementary sensitivity function provides a measure of set-point tracking performances. Equations (3-1), (3-2) and (3-3) shows that the sensitivity function is the transfer function from r to e , and that the complimentary sensitivity function is the transfer function between r and y , in other words, the closed-loop transfer function. These transfer functions are calculated assuming that w and n both equal zero. It is also noted from Equation (3-2) that the error due to the reference signal and the disturbances can be made small, or even close to zero, if the sensitivity can be made small. It is thus possible to ensure that reference signal tracking, disturbance rejection and robustness of the system can be kept at a desired value if the magnitude of $1 + D(j\omega)G(j\omega)$ can be made large, thus minimizing the error, e . Summing $S(s)$ and $T(s)$ in Equation (3-3), gives the relationship

$$S(s) + T(s) = 1 \tag{3-4}$$

which shows a contradiction between the sensitivity and the operation, because it is only possible to design at a certain frequency. Therefore, a working point has to be chosen, which would give a satisfactory response.

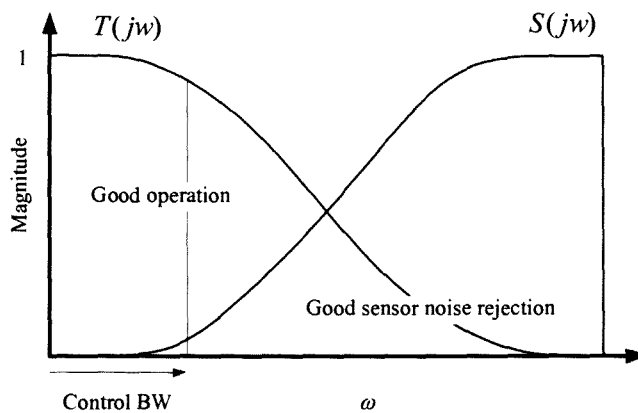


Figure 3.2: Relationship between $S(j\omega)$ and $T(j\omega)$

Figure 3.2 shows the relationship between the sensitivity and the complementary sensitivity functions. For frequencies lower than the control bandwidth, $T(s)$ is at a high value, which would imply improved operation, because good tracking is possible, thus minimizing errors. Alternatively, at frequencies above the control bandwidth $S(s)$ is high, therefore good sensor noise rejection is possible.

As mentioned earlier, the sensitivity function has an effect on disturbances and parameter changes, thus design for acceptable steady-state errors can be thought of as placing a lower bound on the very-low-frequency gain of the system.

Sensitivity is also influenced by the high-frequency portion of the system. It is desirable that the system output is not affected by sensor-noise, therefore the high frequency-gain has to be kept low. PWM switching typically occurs at frequencies of 1 – 10 kHz. High-frequency dynamics can thus have an impact on the stability of the system. A standard approach to make a system robust against unknown high-frequency dynamics is to keep the high-frequency gain low, in the same manner as in sensor-noise reduction [36].

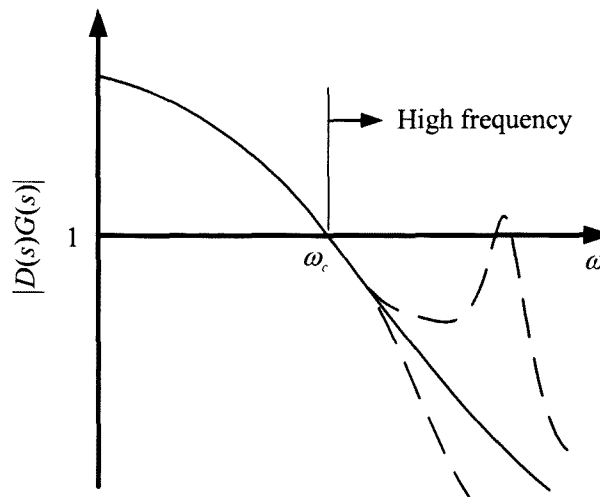


Figure 3.3: Effect of high-frequency uncertainty

Figure 3.3 shows that high-frequency instability can occur when there is an unknown high-frequency component that will increase the magnitude to exceed 1. Instability will also occur when the phase goes through 180° .

The remainder of this chapter explains the implementation and development of a single-phase UPS controller.

Full state feedback is used, using the filter inductor current as the state command. A feed-forward controller is used to compensate for external disturbance signals. An additional PI controller eliminates any steady-state error. Through stability checks done on the transfer function of the plant, and due to time delays that are present in the control algorithm, it is shown that system zeros are located in the right hand plane of the frequency plot. Incorrect control gains can force the system poles to the right half plane, resulting in an unstable system. The time delay is expressed using a Pade [36] approximation. The necessary conditions for system stability are achieved by selecting the correct PI variables. Performance tuning is done afterwards to ensure fast response and little overshoot.

3.2 System description

A block diagram of a typical single-phase UPS system is shown in Figure 3.4. A battery stack is connected to the dc-link of an inverter to supply power in the case of an outage. The output voltage, V , is generated with PWM switching IGBTs, which is filtered with a LC-filter to produce the 50 Hz waveform.

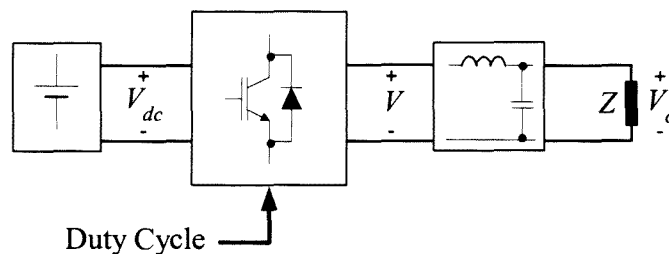


Figure 3.4: Single-line representation of inverter connected to passive LC-filter and load

3.3 Development of a system model

The circuit under investigation is the single-phase, full-bridge inverter, shown in Figure 3.5.

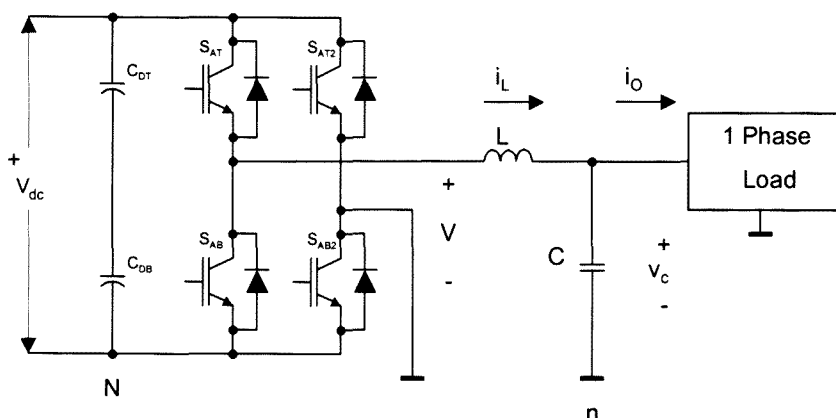


Figure 3.5: Full-bridge inverter

The transfer function of the load/filter combination, which can be defined as the output voltage measured over the capacitor, V_c , divided by the input voltage measured between the two legs of the full-bridge inverter, V , can be derived by using Kirchhoff's current law and voltage law as follows:

$$\begin{aligned} i_L &= i_c + i_o \\ &= C \frac{dv_c}{dt} + \frac{v_c}{Z} \end{aligned} \quad (3-5)$$

and

$$\begin{aligned} V &= v_L + v_c \\ &= L \frac{di_L}{dt} + v_c \end{aligned} \quad (3-6)$$

Manipulating the Laplace transforms of Equations (3-5) and (3-6), the filter-inductor current is expressed in two ways as follows:

$$I_L = V_C \left(sC + \frac{1}{Z} \right) \quad (3-7)$$

and

$$I_L = \frac{V - V_C}{Ls} \quad (3-8)$$

Equations (3-7) and (3-8) are manipulated to give the transfer function as:

$$\frac{V_C}{V} = \frac{1}{s^2 LC + s \frac{L}{Z} + 1} \quad (3-9)$$

with Z representing an arbitrary load.

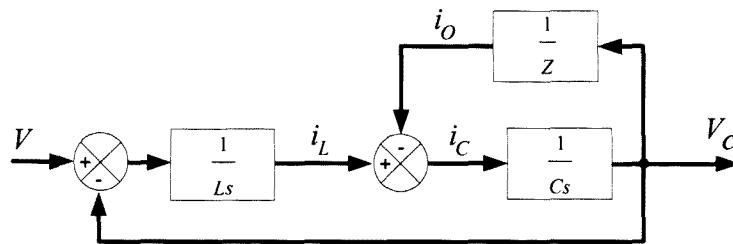


Figure 3.6: Model of an LC-filter connected to a variable load

3.4 Designing the controller

In order to improve waveform quality, the output voltage waveform should be controlled instantaneously, rather than on an average (or rms) basis. There are many advantages for using instantaneous controllers, including better THD, faster transient response, and improved disturbance rejection because of lower output impedances [1].

The controller under investigation is called the Filter Inductor Current Regulator. It works on the basis that the inductor current is measured and load current decoupling is used, ensuring that the output voltage waveform is not affected by this disturbance. The controller consists of an inner current loop and an outer voltage loop.

3.4.1 The Inner-loop controller

The inner loop controller, as shown in Figure 3.7, controls the inductor current. It consists of a PWM block, a compensator, which is the proportional gain, R_a , and the inductor.

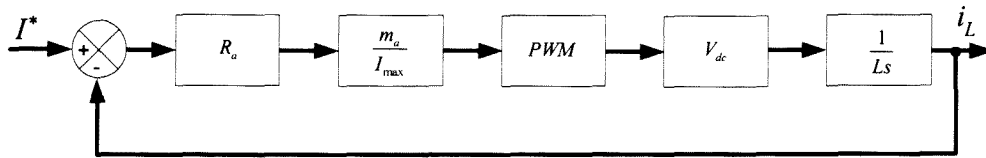


Figure 3.7: Inner-loop current controller

The PWM block produces a duty cycle from the control signal. A digital controller or any fixed-frequency PWM controller introduces a time delay, because the control signal can only be updated every switching cycle. In the s-domain this delay is represented by a Pade approximation [36], with the transportation delay equal to one switching period, giving the second order equation as in Equation (3-10).

$$e^{sT} = e^{\frac{1}{f_s}s} \cong \frac{s^2 - 6f_s s + 12f_s^2}{s^2 + 6f_s s + 12f_s^2} \quad (3-10)$$

The root locus plot, shown in Figure 3.8, is drawn up from the open-loop system, with the proportional gain closing the loop and shifting the poles to the desired locations. The delay introduces two open-loop zeros in the right-hand plane. When the gain is chosen too high, the closed-loop poles are shifted into the right-hand side, creating an unstable system. Thus, for the system to remain stable, the poles need to stay in the left-hand side of the root locus plot. Because R_a sets the bandwidth of the system, it is designed to shift the poles to the imaginary axis to ensure that the system stays in a stable region and that the highest bandwidth is achieved.

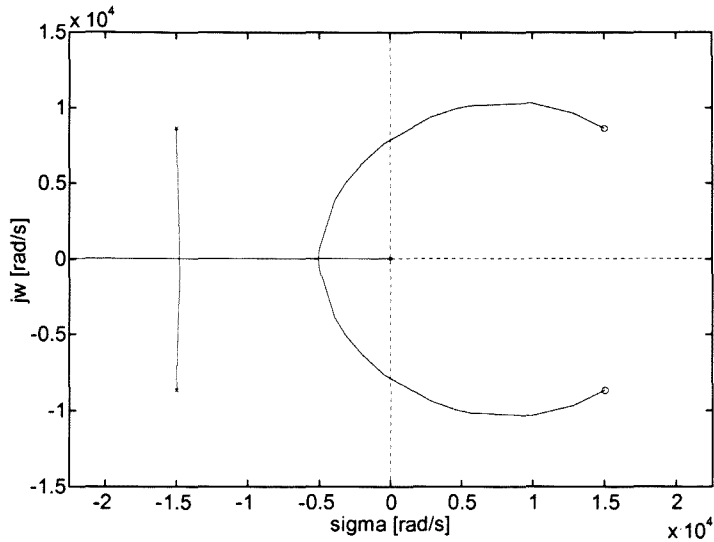


Figure 3.8: Root locus of system with the included time delay

The poles of the system are shifted to be just left of the imaginary axis because R_a must be as high as possible to ensure that the controller will react quickly, and small enough to ensure stability. The bandwidth will be the highest with this pole placement and the output of the current controller will be stable. This filtered inductor current is shown in Figure 3.9.

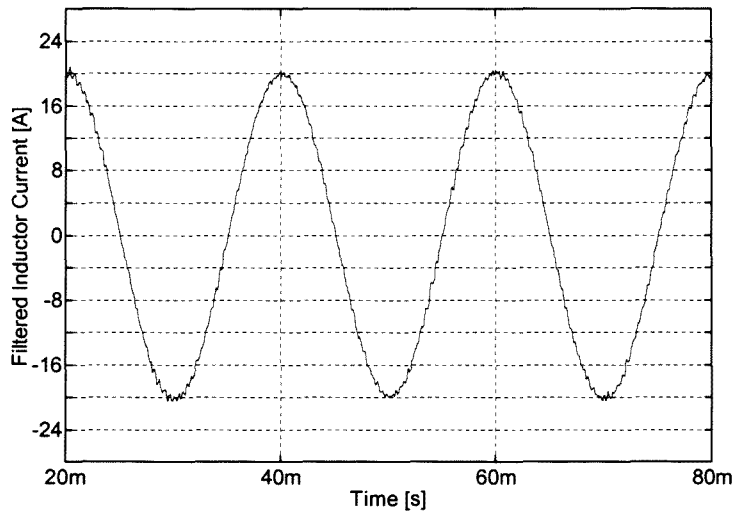


Figure 3.9: Stable current-controller output

Choosing R_a high would shift the poles to the right-hand side of the root locus plot. This would produce a controller that is unstable, as shown in Figure 3.10.

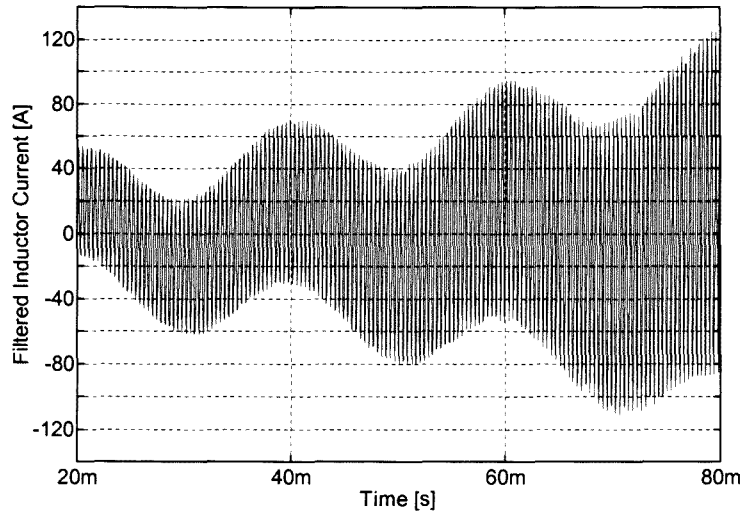


Figure 3.10: Simulation showing unstable current-controller output

3.4.2 Output voltage and load current disturbance decoupling

Decoupling of a certain system variable could have beneficial effects on the output of the system. Therefore output voltage decoupling is combined with load current disturbance decoupling to improve the output voltage waveform of the system.

The current drawn by the load will increase the voltage drop over the filter inductor, producing an output voltage waveform that would be smaller in magnitude than the reference voltage. This is shown in Figure 3.11, where a load change has taken place at time-instant 50 ms.

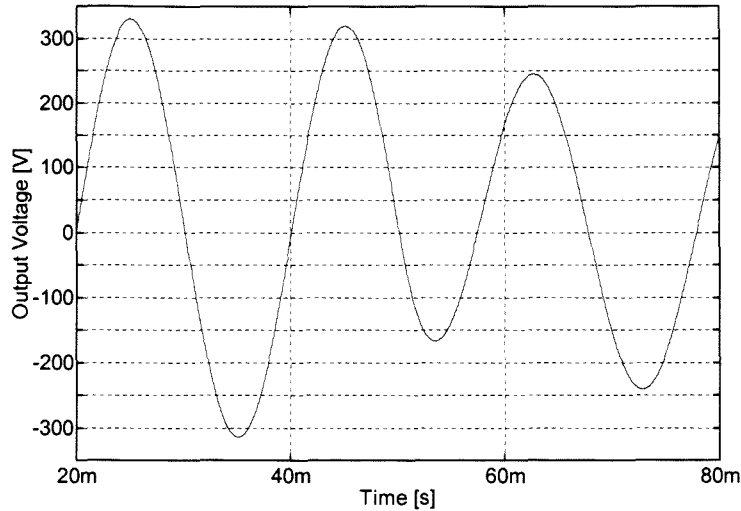


Figure 3.11: Simulation showing the output voltage when no load-current feed-forward is used

Section 2.4.8 explained how a disturbance, or a change in a certain variable, could be compensated for. This would result in an output voltage waveform that would be less prone to the disturbance and would therefore have a lower THD and a magnitude closer to the reference voltage. Equation (2-66) showed that it is possible to find a transfer function that would completely eliminate any disturbances present in a signal or measured quantity. Changing load conditions would produce a change in load current, which would be eliminated by using load-current disturbance rejection. The transfer function is calculated using Figure 3.12.

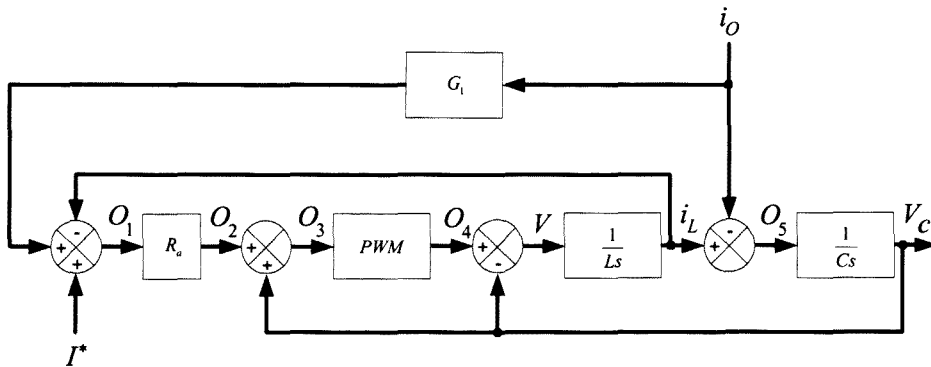


Figure 3.12: Block diagram showing transfer function for disturbance rejection

Mathematical expressions for the different signals, defined O_1 through O_5 , will be calculated to determine an expression for G_1 . If K is defined as the gain of the PWM-block, i_L in Figure 3.12 can be calculated as follows:

$$i_L = \frac{O_3 K - V_c}{sL} \quad (3-11)$$

i_L can also be expressed as:

$$i_L = \frac{O_1 K R_a + V_c (K - 1)}{sL} \quad (3-12)$$

The output, V_c , is calculated as:

$$\begin{aligned} V_c &= \frac{\frac{V}{sL} - i_o}{sC} \\ &= \frac{\frac{K(R_a O_1 + V_c) - V_c - i_o}{sL}}{sC} \\ &= \frac{K R_a O_1 + K V_c - V_c - sL i_o}{s^2 LC} \end{aligned} \quad (3-13)$$

Equation (3-13) is simplified to:

$$V_c = \frac{K R_a O_1 - sL i_o}{s^2 LC + 1 - K} \quad (3-14)$$

From the reference side, the error signal can be obtained as:

$$O_1 = G_1 i_o + I^* - \frac{O_1 K R_a + V_c (K - 1)}{sL} \quad (3-15)$$

Rearranging Equation (3-15), Equation (3-16) can be obtained as:

$$O_1 = \frac{sL}{sL + K R_a} \left[G_1 i_o + I^* + \frac{V_c (1 - K)}{sL} \right] \quad (3-16)$$

For simplicity, define

$$H = \frac{sK R_a L}{(sL + K R_a)(s^2 LC + 1 - K)} \quad (3-17)$$

Substituting Equation (3-16) into Equation (3-14), the output, V_c , is given as:

$$V_c = i_o \left[HG_1 - \frac{sL}{s^2LC + 1 - K} \right] + HI^* + HV_c \left[\frac{1 - K}{sL} \right] \quad (3-18)$$

To eliminate the load-current disturbance, it is necessary that

$$\left[HG_1 - \frac{sL}{s^2LC + 1 - K} \right] = 0 \quad (3-19)$$

Therefore

$$\frac{sLKR_aG_1}{(sL + KR_a)(s^2LC + 1 - K)} = \frac{sL}{s^2LC + 1 - K} \quad (3-20)$$

From Equation (3-20) the disturbance rejection transfer function is calculated as:

$$G_1 = \frac{sL + KR_a}{KR_a} \quad (3-21)$$

The transfer function calculated in Equation (3-21) is an improper transfer function, as there is only a zero in the numerator, but no poles in the denominator. The Bode plot is shown in Figure 3.13.

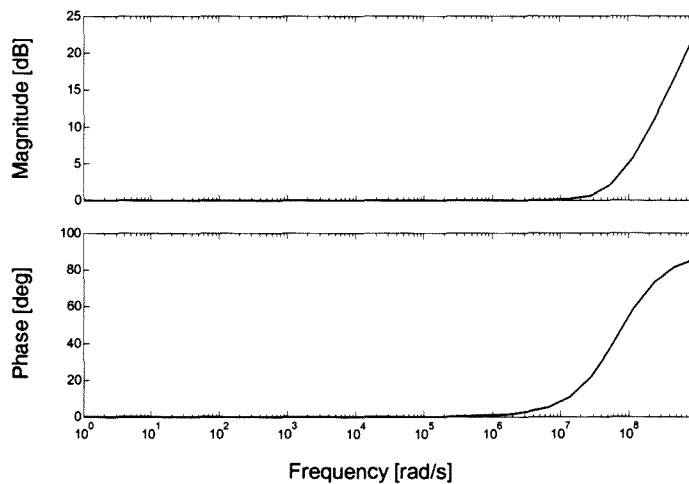


Figure 3.13: Bode plot of decoupling transfer function

The magnitude is unity between 1 rad/s and 1 Mrad/s. As the bandwidth of the controller is much lower than 1 Mrad/s, it is possible to represent the decoupling transfer function, G_1 , with a unity gain. With load-current compensation the output voltage stays close to the reference voltage as shown in Figure 3.14.

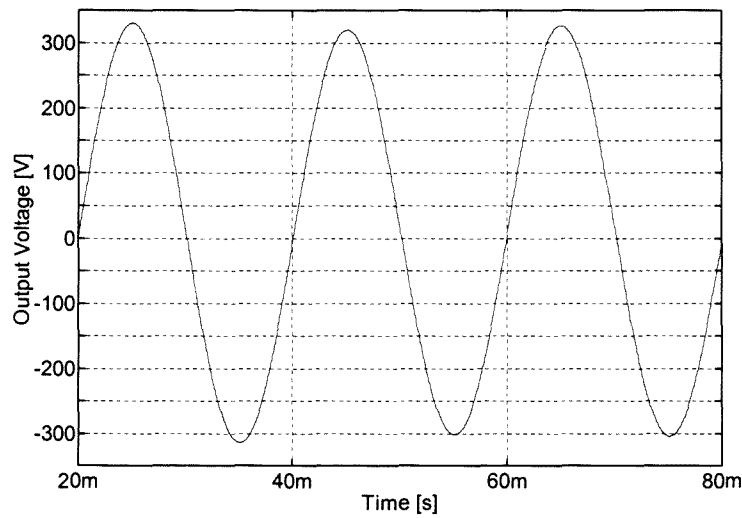


Figure 3.14: Output voltage when load-current feed-forward is used

3.4.3 The Outer-loop controller

A stable inner-loop current controller is developed, although output-current waveforms in Figure 3.15 shows that there is still a phase lag in the output current.

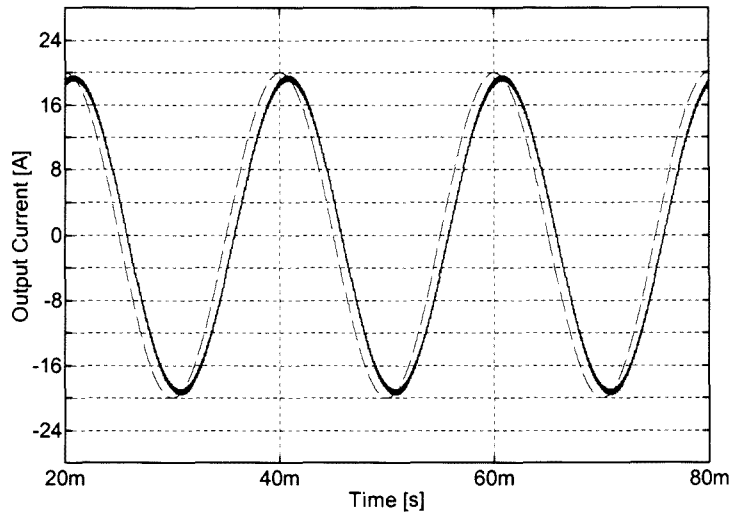


Figure 3.15: Output current lags reference current

An outer voltage-loop is added to ensure an output voltage that has zero steady-state error and a current waveform with no phase lag. This is done by adding a closed-loop PI controller. The outer-loop controller is shown in Figure 3.16.

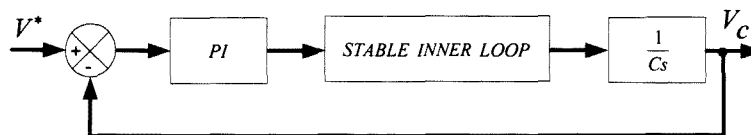


Figure 3.16: Outer-loop voltage controller

Section 2.4.7 explained the design of a PI controller. The four steps mentioned will be followed to determine the PI variables.

3.4.3.1 Finding the open-loop transfer function of the current-controller

The open-loop transfer function of the current controller is calculated by using Figure 3.17.

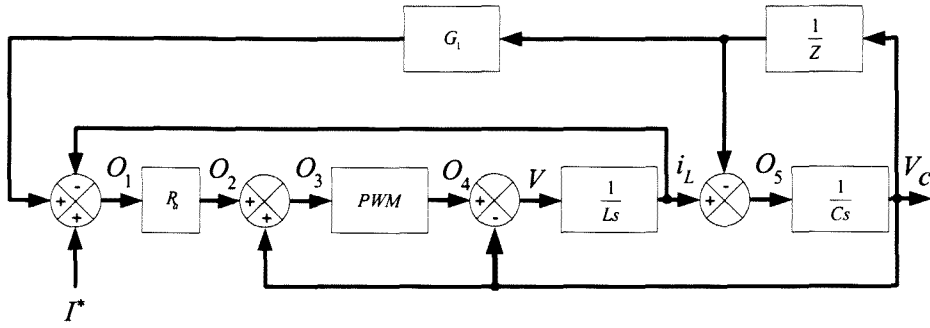


Figure 3.17: Block diagram showing transfer function of open-loop current controller

The signals, defined O_1 through O_5 , and the output, V_c , is calculated as

$$O_5 = i_L - \frac{V_c}{Z} \quad (3-22)$$

$$V_c = \frac{O_5}{sC} \quad (3-23)$$

$$\begin{aligned} i_L &= O_5 \left(1 + \frac{1}{sCZ} \right) \\ &= \frac{O_4 - V_c}{sL} \end{aligned} \quad (3-24)$$

$$O_4 = K(O_2 + V_c) \quad (3-25)$$

$$O_2 = R_a O_1 \quad (3-26)$$

To introduce the reference, Equations (3-22) to (3-26) are used to determine the ratio $\frac{V_c}{I^*}$, which is equal to the open-loop transfer function of the current controller.

$$\begin{aligned} O_1 &= I^* + G_1 \left(\frac{V_c}{Z} \right) - i_L \\ &= I^* + V_c \left[\frac{G_1}{Z} - sC - \frac{1}{Z} \right] \end{aligned} \quad (3-27)$$

$$I^* = \frac{sLi_L + V_c}{KR_a} + V_c \left[sC + \frac{1}{Z} - \frac{G_1}{Z} - \frac{1}{R_a} \right] \quad (3-28)$$

$$I^* = V_c \left[\frac{s^2 LC}{KR_a} + \frac{1}{KR_a} + sC - \frac{1}{R_a} \right] \quad (3-29)$$

The open-loop transfer function is determined as:

$$\frac{V_c}{I^*} = \frac{1}{s^2 \left(\frac{LC}{KR_a} \right) + sC + \left(\frac{1}{KR_a} - \frac{1}{R_a} \right)} \quad (3-30)$$

3.4.3.2 Introducing a load step to the open-loop transfer function

The system in Figure 3.17 is excited with a unit-step reference to view the open-loop response.

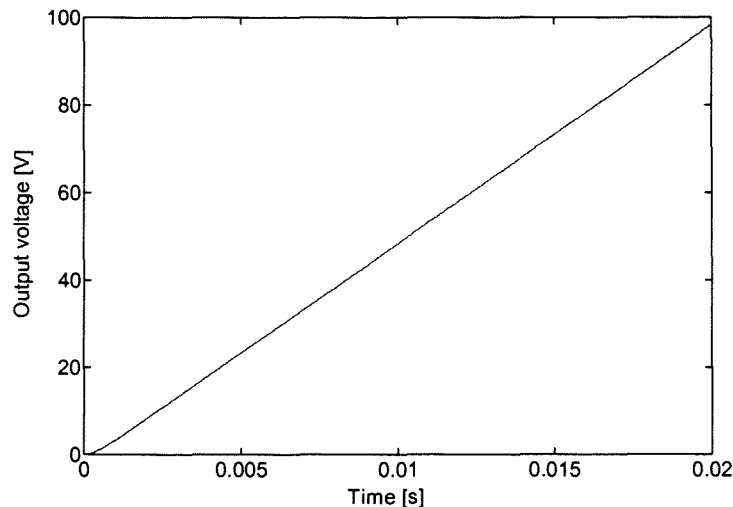


Figure 3.18: Open-loop step response

Figure 3.18 shows that the output voltage does not represent a unit-step at all, which justifies the addition of a PI controller to eliminate the steady-state error and to avoid system instability. The PI controller is essentially a low-pass filter [34], having high gain at low frequencies and low gain at high frequencies. Therefore, the steady-state error will improve, while system instability will be avoided by limiting high frequency components.

3.4.3.3 Adding a PI controller

The transfer function of a PI controller is defined in [34] as:

$$\frac{K_i + sK_v}{s} \quad (3-31)$$

Therefore, replacing the reference current in Figure 3.17 with a voltage reference and implementing the PI controller, the system as shown in Figure 3.19 is created.

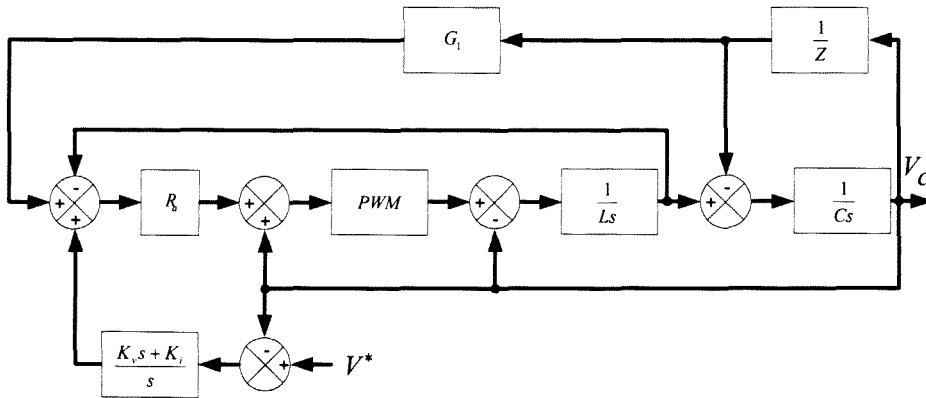


Figure 3.19: Block diagram of the complete controller

The current reference in Figure 3.17 becomes:

$$I^* = \frac{V^* - V_c}{s} (K_v s + K_i) \quad (3-32)$$

The new transfer function for the controller with the closed-loop current controller incorporated, Figure 3.19, is calculated as:

$$\frac{V_c}{V^*} = \frac{K_v s + K_i}{s^3 \left(\frac{LC}{KR_a} \right) + s^2 C + s \left(\frac{1}{KR_a} - \frac{1}{R_a} + K_v \right) + K_i} \quad (3-33)$$

The PI variables are obtained by using Routh's Stability Criterion, Section 2.4.2.1. Equation (3-33) is used to calculate the necessary triangular array. The characteristic equation is defined as the denominator of Equation (3-33), and is represented as

$$\begin{aligned}
 a(s) &= s^3 \left(\frac{LC}{KR_a} \right) + s^2 C + s \left(\frac{1}{KR_a} - \frac{1}{R_a} + K_v \right) + K_i \\
 &= s^3 + s^2 \frac{Con_2}{Con_1} + s \left(\frac{K_v + Con_3}{Con_1} \right) + \frac{K_i}{Con_1}
 \end{aligned}
 \tag{3-34}$$

with

$$\begin{aligned}
 Con_1 &= \frac{LC}{KR_a} \\
 Con_2 &= C \\
 Con_3 &= \frac{1-K}{KR_a}
 \end{aligned}
 \tag{3-35}$$

The triangular array is calculated as:

Table 3.1: Routh's triangular array

s^3 :	1	$\frac{K_v + Con_3}{Con_1}$
s^2 :	$\frac{Con_2}{Con_1}$	$\frac{K_i}{Con_1}$
s^1 :	$\frac{1}{Con_2} \left[\frac{Con_2 (K_v + Con_3)}{Con_1} - K_i \right]$	
s^0 :	$\frac{K_i}{Con_1}$	

For the system to remain stable, the following conditions from Table 3.1 apply:

$$\frac{1}{Con_2} \left[\frac{Con_2 (K_v + Con_3)}{Con_1} - K_i \right] > 0
 \tag{3-36}$$

and

$$\frac{K_i}{Con_1} > 0 \quad (3-37)$$

Since the coefficients are all positive and bigger than zero, and Con_3 can be made equal to zero if $K = 1$, a relationship between K_v and K_i can be found to keep the system at a stable operating point. Using Equations (3-36) and (3-37), the relationship is found as:

$$\frac{R_a}{L} > \frac{K_i}{K_v} \quad (3-38)$$

3.4.3.4 Calculation of K_v and K_i

Now that the conditions for stability are known, values for the PI variables should be chosen to give the desired response. Various factors can influence the output waveform quality, two of which are the settling time and the output impedance. A shorter settling time will enable the output voltage to follow the reference more quickly, whereas an output impedance of zero ohms would make the system less prone to any disturbance due to changing loads. These two factors are combined to find the values of K_v and K_i that would give the best response.

a) Dynamic stiffness

The dynamic stiffness of a UPS system is defined as the magnitude of the output load current that causes a unit deviation in output voltage magnitude [1], represented as

$$DS = \left| \frac{I_o(s)}{E_o(s)} \right|_{s=j\omega} \quad (3-39)$$

which is also equal to the inverse of the output impedance of the controller. If the output impedance can be made as close to zero as possible, any type of load can be connected to the system without affecting the output voltage waveform. This is due to the fact that a smaller impedance is connected in parallel with a higher impedance. There will be no voltage drop over the output of the filter and load combination, and the output will follow the reference exactly. In other words, if the dynamic stiffness

can be made equal to infinity with any type of load, it will be possible to eliminate the effect of load changing on the output voltage. The reference input can be made equal to zero, because it will have no effect on the output impedance. The constant of the PWM modulation is set to unity. By doing this, Figure 3.19 is simplified, as shown in Figure 3.20. This is done to calculate the output impedance of the controller.

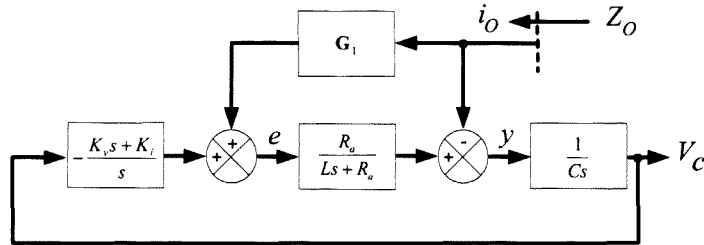


Figure 3.20: Simplified block diagram to calculate the dynamic stiffness

The signals e and y are defined as

$$e = G_1 i_o - K_c V_c \quad (3-40)$$

$$y = \left(\frac{R_a}{sL + R_a} \right) e - i_o \quad (3-41)$$

with

$$K_c = \frac{sK_v + K_i}{s} \quad (3-42)$$

Combining Equations (3-40) and (3-41) gives

$$\begin{aligned} V_c &= \frac{y}{sC} \\ &= \left(\frac{1}{sC} \right) \left[\left(\frac{R_a}{sL + R_a} \right) [G_1 i_o - K_c V_c] - i_o \right] \end{aligned} \quad (3-43)$$

which is then simplified to

$$V_c \left[1 + \frac{R_a K_c}{sC(sL + R_a)} \right] = i_o \left[\frac{R_a G_1}{sC(sL + R_a)} - \frac{1}{sC} \right] \quad (3-44)$$

Finally, using Equations (3-39) and (3-44), the dynamic stiffness is calculated as:

$$DS = \left| \frac{I_o}{E_o} \right| = \left| \frac{s^3 LC + s^2 CR_a + sK_v R_a + K_i R_a}{s^2 L(R_a - 1)} \right| \quad (3-45)$$

It is desirable that the dynamic stiffness at 50 Hz be as high as possible, ensuring a low voltage drop and therefore a sinusoidal output voltage waveform. Therefore

$$DS(j\omega) = \frac{(K_i R_a - \omega^2 CR_a) + j(\omega K_v R_a - \omega^3 LC)}{-\omega^2 L(R_a - 1)} \quad (3-46)$$

and

$$|DS(j\omega)| = \frac{\sqrt{(K_i R_a - \omega^2 CR_a)^2 + (\omega K_v R_a - \omega^3 LC)^2}}{\omega^2 L(R_a - 1)} \quad (3-47)$$

For $|DS|$ to be as high as possible, the numerator of Equation (3-47) should be as high as possible. It is calculated from Equation (3-47) that

$$\begin{aligned} num^2 = & K_v^2 (\omega^2 R_a^2) + K_v (-2\omega^4 LCR_a) + K_i^2 R_a^2 + K_i (-2\omega^2 CR_a^2) + \dots \\ & \omega^6 (LC)^2 + \omega^4 (CR_a)^2 \end{aligned} \quad (3-48)$$

The constants in Equation (3-48) all differ in magnitude and are defined in Equation (3-49) with greater sign values representing greater magnitudes.

$$num^2 = K_v^2 (+) + K_v (-) + K_i^2 (+) + K_i (-) + (+) \quad (3-49)$$

Equation (3-49) shows that terms subtracted are $K_i(-)$ and $K_v(-)$ respectively. Thus, in order for DS to be as large as possible, K_v has to be small and K_i has to be large.

b) Minimizing the settling time

In order for the system to respond quickly to step changes, it is desirable that the system have a very fast settling time. Choosing the correct values for K_v and K_i , the settling time can be minimized. Combining the inner- and outer-loop, the transfer function of the complete controller is calculated. It will be shown that various gains

will have big influences on the stability of the system. The closed loop transfer function is given by:

$$SYS_{CL} = \frac{KK_v[s^3 + K_1s^2 + K_2s + K_3]}{Cs^5 + C(6f_s + K)s^4 + K_4s^3 + K_5s^2 + KK_vK_2s + KK_vK_3} \quad (3-50)$$

with

$$K = \frac{V_{dc}R_a m_a}{I_{max}L}$$

$$PI = \frac{K_i}{K_v}$$

$$K_1 = PI - 6f_s$$

$$K_2 = 12f_s^2 - 6PI.f_s$$

$$K_3 = 12PI.f_s^2$$

$$K_4 = C(12f_s^2 - 6f_sK) + KK_v$$

$$K_5 = C(12Kf_s^2) + KK_vK_1 \quad (3-51)$$

The poles and zeros of Equation (3-50) are shifted when the values of K_v and K_i , respectively, are changed.

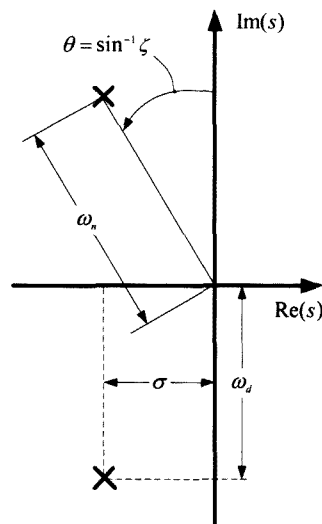


Figure 3.21: s-plane plot of a pair of complex poles

In Figure 3.21 a pair of complex poles are shown. The natural response of the system is governed by $e^{-\sigma t}$ and will decay if the poles stay in the LHP [36]. The closed-loop transfer function in (3-50) is a 5th order equation, in other words, there will be five poles in the LHP. The poles closest to the origin will contribute the most to the settling time, as can be seen from the settling time of a 2nd order system, represented by [36]

$$t_s = \frac{4.6}{\sigma} \tag{3-52}$$

with σ being smaller the closer it gets to the origin. Equations (3-38) and (3-51) are used to plot various values of K_i for constant values of K_v , to show the effect on the settling time.

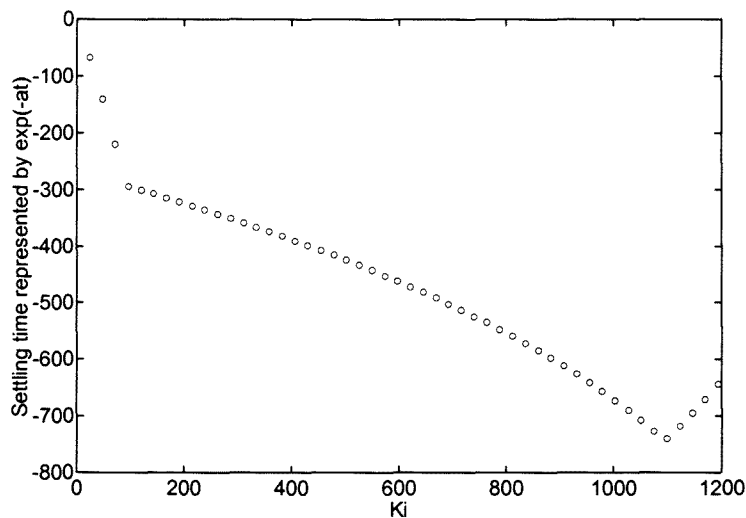


Figure 3.22: Choosing K_v and K_i for fastest settling time

From Figure 3.22 one can see that the settling time will decrease until the fastest response is achieved. Thereafter the settling time will increase with bigger values of K_i .

3.5 Evaluation of the controller

The system used for evaluating the controller is a full-bridge inverter supplied by a dc-bus of 750 V. The switching frequency is set to 5 kHz. The filter inductor is 400 μH and the filter capacitor is 200 μF , with a load of 25 kW.

With these circuit variables, the controller gains are calculated as:

$$\begin{aligned}R_a &= 1.13 \\K_v &= 0.8 \\K_i &= 2090\end{aligned}\tag{3-53}$$

These gains will shift the poles towards the zeros. All the poles are located in the left-hand side of the s-plane plot, therefore system stability is ensured. Controller performance is increased with low output-impedance, which can be achieved by using a high control bandwidth. Factors limiting the control bandwidth include the time delay introduced due to calculations and measurements that limit the frequency components in the measured quantities. Increasing the switching frequency will extend the control bandwidth, but with the higher switching frequency, the ratio of dead time to duty ratio will become larger. Increased dead time will degrade the output voltage waveforms, because the voltages are uncontrollable during the dead time.

The output impedance will determine how well the controller will perform under various load conditions. Substituting the controller gains given in Equation (3-53) into Equation (3-47), the output impedance can be calculated as:

$$Z_o = \frac{1}{DS} = 0.0022 \Omega\tag{3-54}$$

The output current will therefore have a negligible effect of the output voltage, due to the small impedance calculated in Equation (3-54). The simulated output voltage is shown in Figure 3.23.

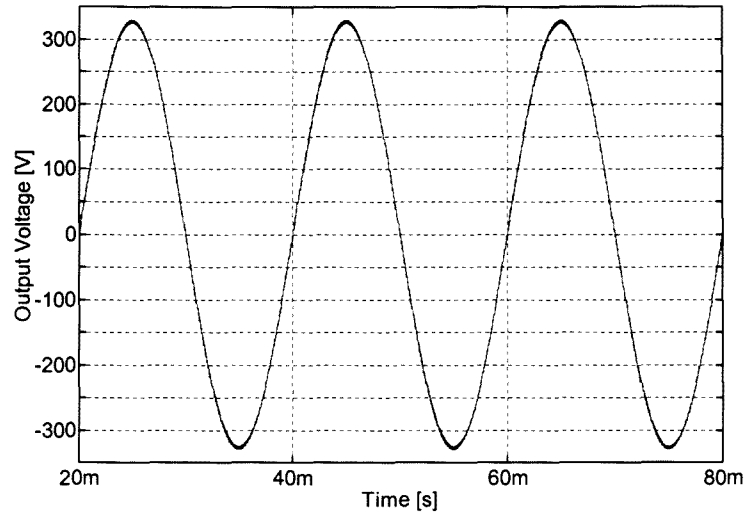


Figure 3.23: Output voltage with closed-loop controller

The output voltage is of equal magnitude to the reference voltage and the phase delay is close to zero degrees.

3.6 Summary

This chapter explained the development of a closed-loop voltage controller using classical control techniques. The time delay that is introduced by the DSP causes the system zeros to be located in the right-hand side of the frequency plot. The controller gains will shift the poles to the zeros; therefore, incorrect controller gains could shift the system poles to the right-hand side, which would render an unstable system. A Pade [36] approximation was used to develop a model of this delay to ensure the design of a stable voltage controller. Feed-forward was implemented to compensate for the changes in the load current, which improves the voltage waveform quality. A PI controller was used to eliminate any steady-state error.

Chapter 4

Design Using Modern Control Techniques

4 Design using modern control techniques

4.1 Introduction

Design using modern control techniques, commonly known as state-space design, have been used ever since computer-aided control systems were developed. The system is represented by differential equations, which is then described as first-order differential equations organized in the vector-valued state of the system. The dynamic compensation is designed by working directly with the state-variables. These can then be represented using difference equations and programmed into a digital controller.

This chapter explains the development of the control system, implementing deadbeat control. Deadbeat control was chosen because the supply will follow the applied control signal in a minimum amount of time steps, as explained in Section 2.4.4. The design is done starting with the model of a single-phase, full-bridge inverter, supplying an arbitrary load. This is done as shown in Section 2.3 that a four-wire inverter can be represented by three independent single-phase circuits. The state equations of the complete system are calculated and a control law, with no load connected to the inverter, is developed. Thereafter, the load current is treated as if it is a disturbance affecting the plant, and the control law is updated using feed-forward control, as given in Section 2.4.8, to eliminate this disturbance. Finally, the controller is evaluated on a three-phase, four-wire system, making the three phases independent of each other, so that each phase can be controlled separately, without affecting each other.

4.2 Development of a system model

Section 2.3.3.1 explained how it is possible to represent a three-phase, four-wire inverter with three independent, single-phase circuits. Therefore Figure 4.1 will be used to develop the system model.

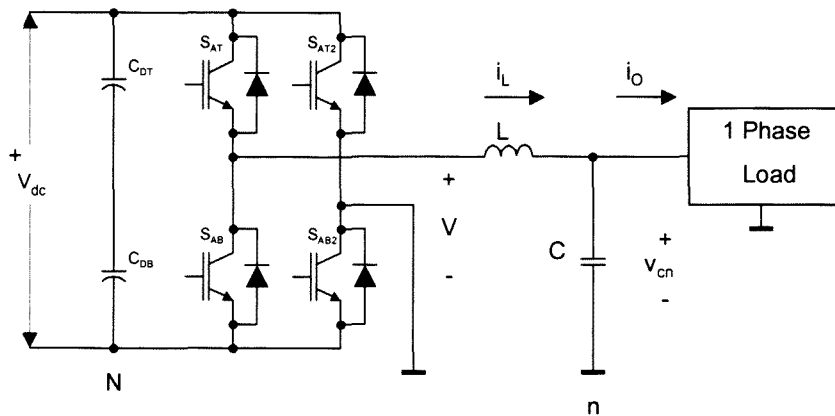


Figure 4.1: A single-phase representation of the three-phase inverter

The differential equations of the system in Figure 4.1, with V being the inverter phase voltage relative to the load neutral, n , i_L being the inductor current, i_o being the load current and v_{cn} being the capacitor voltage, is found as

$$i_L = C \frac{dv_{cn}}{dt} + i_o$$

$$V = L \frac{di_L}{dt} + v_{cn} \quad (4-1)$$

Equation (4-1) is now written in vector form as

$$\frac{d\mathbf{V}_c}{dt} = \frac{1}{C} (\mathbf{I}_L - \mathbf{I}_o)$$

$$\frac{d\mathbf{I}_L}{dt} = \frac{1}{L} (\mathbf{V} - \mathbf{V}_c) \quad (4-2)$$

with the vectors representing the voltages and currents for the three separate circuits. Finally, in matrix form, Equation (4-2) is converted to

$$\frac{d\mathbf{x}}{dt} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{V} + \mathbf{B}_i\mathbf{I}_o \quad (4-3)$$

where

$$\mathbf{x} = \begin{bmatrix} \mathbf{V}_c \\ \mathbf{I}_L \end{bmatrix}, \mathbf{A} = \begin{bmatrix} 0 & \frac{1}{C} \\ -\frac{1}{L} & 0 \end{bmatrix}, \mathbf{B} = \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix}, \mathbf{B}_i = \begin{bmatrix} -\frac{1}{C} \\ 0 \end{bmatrix} \quad (4-4)$$

4.3 Discretization of continuous-time state equations

It is desired that the state $\mathbf{x}(t)$ be computed by a digital processor, making it necessary that the continuous-time state equations be converted to discrete-time state equations. The inputs \mathbf{V} and \mathbf{I}_o can be assumed constant between two sampling instants kT and $(k+1)T$, since sampling is much faster than the dynamics of the fundamental load current and the dc-link voltage. The following discrete-time state equation follows [34]:

$$\mathbf{x}(k+1) = \Phi \mathbf{x}(k) + \Gamma \mathbf{V}(k) + \Gamma_i \mathbf{I}_o(k) \quad (4-5)$$

with

$$\Phi = e^{\mathbf{A}T} = \mathcal{L}^{-1} \left[(s\mathbf{I} - \mathbf{A})^{-1} \right]$$

$$\Gamma = \left(\int_0^T e^{\mathbf{A}t} dt \right) \mathbf{B}, \Gamma_i = \left(\int_0^T e^{\mathbf{A}t} dt \right) \mathbf{B}_i$$

$$T = \frac{1}{f_s} \quad (4-6)$$

In Equation (4-6), Φ is the state matrix, Γ is the input matrix with input equal to the inverter phase voltage and Γ_i being the input matrix with the load current being the only input.

Following from (4-6), the matrices are calculated as:

$$\Phi = \begin{bmatrix} \cos(\omega_0 T) & \frac{1}{\omega_0 C} \sin(\omega_0 T) \\ -\frac{1}{\omega_0 L} \sin(\omega_0 T) & \cos(\omega_0 T) \end{bmatrix}, \Gamma = \begin{bmatrix} 1 - \cos(\omega_0 T) \\ \frac{1}{\omega_0 L} \sin(\omega_0 T) \end{bmatrix},$$

$$\Gamma_i = \begin{bmatrix} -\frac{1}{\omega_0 C} \sin(\omega_0 T) \\ 1 - \cos(\omega_0 T) \end{bmatrix}, \omega_0 = \frac{1}{\sqrt{LC}} \quad (4-7)$$

4.4 The Reference vector

For the reference vector to be calculated, the system given in Equation (4-3) is manipulated to exclude the effects of the load current. u is defined as the input and is equal to the inverter phase voltage, V . The system is now given as

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}u$$

$$y = \mathbf{C}\mathbf{x} \quad (4-8)$$

with the discrete representation being

$$\mathbf{x}(k+1) = \Phi \mathbf{x}(k) + \Gamma u(k) \quad (4-9)$$

The variable that needs to be controlled is the output voltage, or capacitor voltage. Since the converter cannot synthesize these voltages, the reference has to be transformed to inverter output voltages, \mathbf{V}_n^* , (measured with respect to the load neutral) and then finally to inverter voltages with respect to the negative dc-bus, \mathbf{V}^* . For sinusoidal variations, the reference capacitor voltage in the $\alpha\beta$ -plane is found as [3]

$$\begin{aligned} \mathbf{V}_c^*(k+1) &= |\mathbf{V}_c| e^{j(k+1)\omega T} \\ &= e^{j\omega T} \mathbf{V}_c^*(k) \\ &= q \mathbf{V}_c^*(k) \end{aligned} \quad (4-10)$$

with

$$q = e^{j\omega T} \quad (4-11)$$

Now, define

$$\mathbf{x}(k) = \mathbf{x}^*(k) + \Delta\mathbf{x}(k) \quad (4-12)$$

with

$$\mathbf{x}^*(k) = \text{Reference value}$$

$$\Delta\mathbf{x}(k) = \text{Error value} \quad (4-13)$$

it is found using Equation (4-8) that

$$\begin{bmatrix} \mathbf{V}_c^*(k+1) \\ \mathbf{I}_L^*(k+1) \end{bmatrix} = \begin{bmatrix} \Phi_{11} & \Phi_{12} \\ \Phi_{21} & \Phi_{22} \end{bmatrix} \begin{bmatrix} \mathbf{V}_c^*(k) \\ \mathbf{I}_L^*(k) \end{bmatrix} + \begin{bmatrix} \Gamma_{11} \\ \Gamma_{21} \end{bmatrix} \mathbf{V}^*(k) \quad (4-14)$$

Combining Equation (4-10) and (4-14) and simplifying,

$$[q - \Phi_{11}] \mathbf{V}_c^*(k) = \Phi_{12} \mathbf{I}_L^*(k) + \Gamma_{11} \mathbf{V}^*(k) \quad (4-15)$$

and

$$[q - \Phi_{22}] \mathbf{I}_L^*(k) = \Phi_{21} \mathbf{V}_c^*(k) + \Gamma_{21} \mathbf{V}^*(k) \quad (4-16)$$

Substituting the current reference in Equation (4-16) into Equation (4-15), the inverter voltage reference is given as

$$\mathbf{V}^*(k) = \mathbf{V}_c^*(k) \left[\frac{q^2 - q\Phi_{22} - q\Phi_{11} + \Phi_{11}\Phi_{22} - \Phi_{12}\Phi_{21}}{q\Gamma_{11} - \Gamma_{11}\Phi_{22} + \Phi_{12}\Gamma_{21}} \right] \quad (4-17)$$

4.5 Calculating the control law, assuming no load

The first step in designing the controller is to assume that the system is not drawing load current. The system equations are then as given in Equation (4-8) and (4-9). The switching frequency is set at 5 kHz. The filter inductor has a value of 400 μH and the filter capacitor has a value of 200 μF . The system poles can be situated at any location in the discrete plane (z -plane), and therefore it is possible to have an unstable system. The open-loop poles are shown in Figure 4.2.

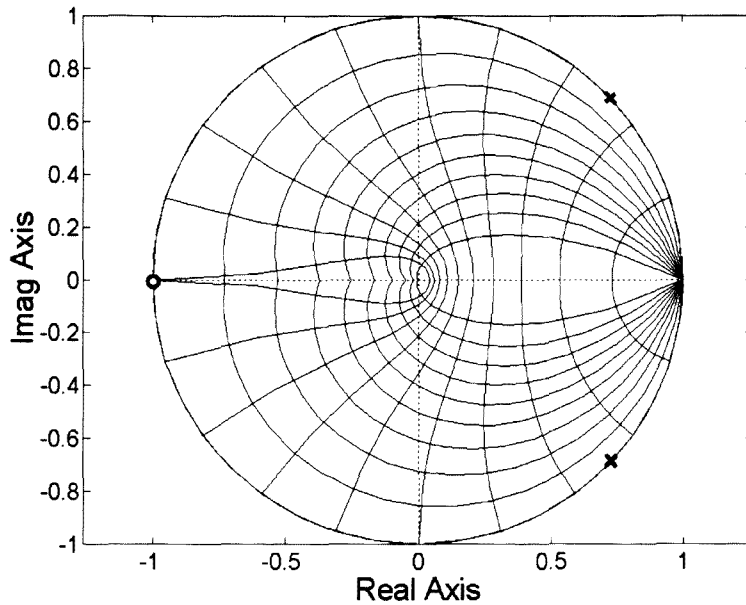


Figure 4.2: Pole-zero map of open-loop system

From Figure 4.2 it is clear to see that the system poles are situated on the border of the circle, and that any system variation could make the poles move outside the circle and would cause instability. It is thus advantageous to introduce a closed-loop controller that will ensure stability. The control law consists of a linear combination of the states, effectively moving the poles to any desired location. For the deadbeat controller, the poles are all moved to the origin of the z -plane, as stated in Section 2.4.4. Thus, for the given system, a K -vector of length equal to 2 will be required to move the poles to the origin. A controller, as depicted in Figure 4.3, is used to calculate the K -vector with the help of Ackermann's formula [36].

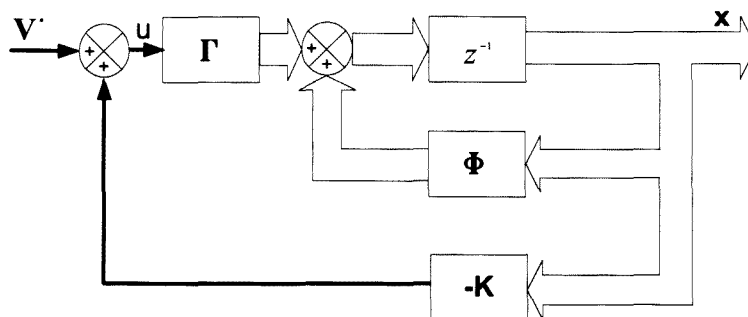


Figure 4.3: The control law - a linear combination of the state variables

4.6 Eliminating the calculation delay

The simulation in Figure 4.4 shows the three-phase output waveforms of the controller depicted in Figure 4.3. Extreme instability is observed, which is caused by the time delay that is not included in the model of the system.

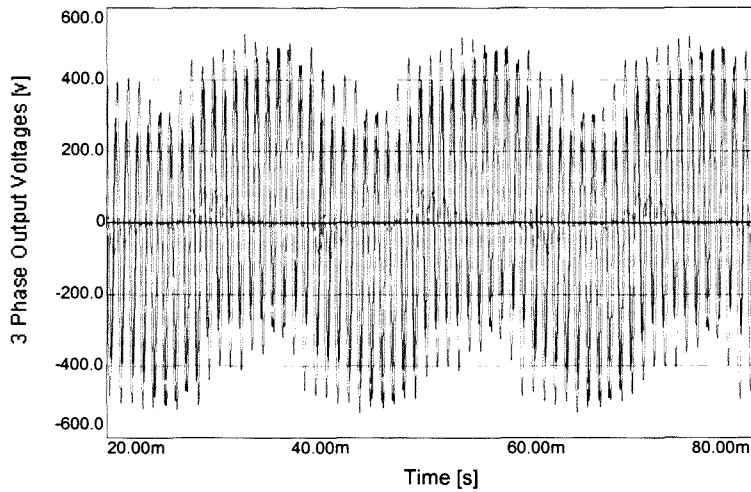


Figure 4.4: Output waveforms of second order controller

The poles of the second order system are shown in Figure 4.5. Both poles are situated outside the unity circle, which causes the system instability.

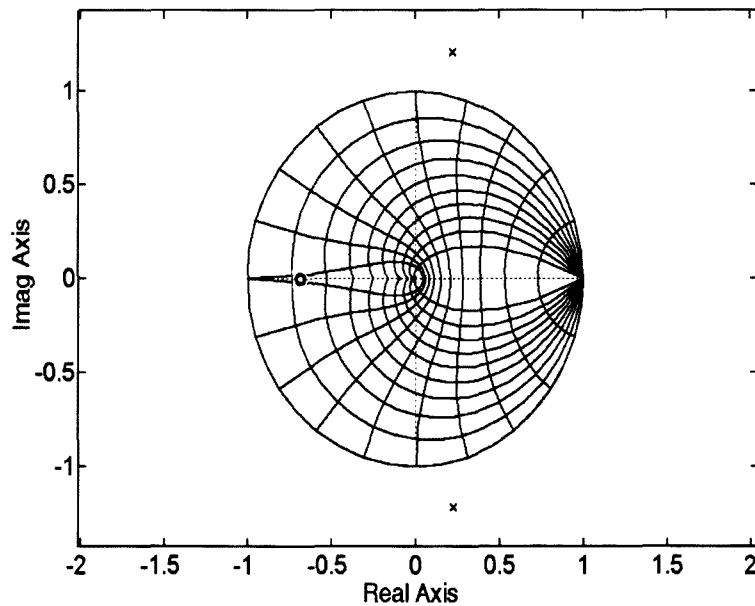


Figure 4.5: Pole-zero map of the unstable system

The system is implemented using a DSP, resulting in a computational delay. This is shown in Figure 4.6, with the time delay represented by mT_s . The measurements are done at sampling instant kT , but in a practical system this takes a finite time. The time that the final measurement finishes is assumed to be the same time that the calculations start. It is also assumed that all calculations are completed within this remaining time, mT_s , and that the control signal $v = u(k-1)$ is applied to the filter during this time. The applied control would therefore produce an error in the output voltage waveform.

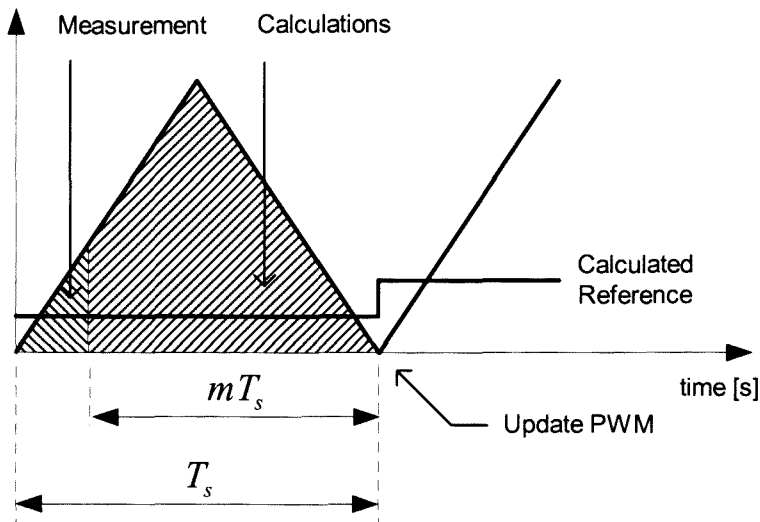


Figure 4.6: Sampling instant with computational delay

This was explained in Section 2.4.3, where it was stated that augmenting the system with the time delay would increase the order of the system and result in stabilizing the controller. The system equations are augmented to include a new variable, $\varepsilon(k) = u(k-1)$. Equation (2-52) and (2-53) are used to give the new system equations as

$$\begin{bmatrix} \mathbf{x}(k+1) \\ \varepsilon(k+1) \end{bmatrix} = \begin{bmatrix} \Phi(T) & \Gamma_1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \mathbf{x}(k) \\ \varepsilon(k) \end{bmatrix} + \begin{bmatrix} \Gamma_2 \\ 1 \end{bmatrix} u(k)$$

$$y(k) = \begin{bmatrix} \mathbf{H} & 0 \end{bmatrix} \begin{bmatrix} \mathbf{x}(k) \\ \varepsilon(k) \end{bmatrix} \quad (4-18)$$

or, equivalently

$$\begin{aligned} \mathbf{z}(k+1) &= \Phi_{del} \mathbf{z}(k) + \Gamma_{del} \mathbf{u}(k) \\ y(k) &= \mathbf{H}_{del} \mathbf{z}(k) \end{aligned} \quad (4-19)$$

where the modified system matrices are

$$\Phi_{del} = \begin{bmatrix} \Phi(T) & \Gamma_1 \\ 0 & 0 \end{bmatrix}, \Gamma_{del} = \begin{bmatrix} \Gamma_2 \\ 1 \end{bmatrix}, \mathbf{z} = \begin{bmatrix} \mathbf{x} \\ \mathcal{E} \end{bmatrix} \quad (4-20)$$

The control law will only affect the system in (4-19) if the system is controllable. It is therefore necessary to calculate the controllability matrix. From Equation (2-31), the controllability matrix is given as

$$\mathbf{C} = \begin{bmatrix} \Gamma_{del} & \Phi_{del} \Gamma_{del} & \Phi_{del}^2 \Gamma_{del} \end{bmatrix} \quad (4-21)$$

When the controllability matrix is non-singular, in other words invertible, the system in Equation (4-19) is said to be controllable. From Equation (4-20) it is seen that the system changed to third order. A variation on Ackermann's formula states that if the system is controllable, it is possible to get the K -vector using

$$\mathbf{K} = [0 \ 0 \ 1] \mathbf{C}^{-1} \alpha_c(\Phi) \quad (4-22)$$

where

$$\alpha_c(\Phi) = \Phi^n + \alpha_1 \Phi^{n-1} + \alpha_2 \Phi^{n-2} + \dots + \alpha_n \Phi \quad (4-23)$$

with α_n being the coefficients of the desired characteristic polynomial, calculated by using the desired pole locations. Again the system poles are shifted to the origin of the z -plane to achieve deadbeat control, depicted in Figure 4.7.

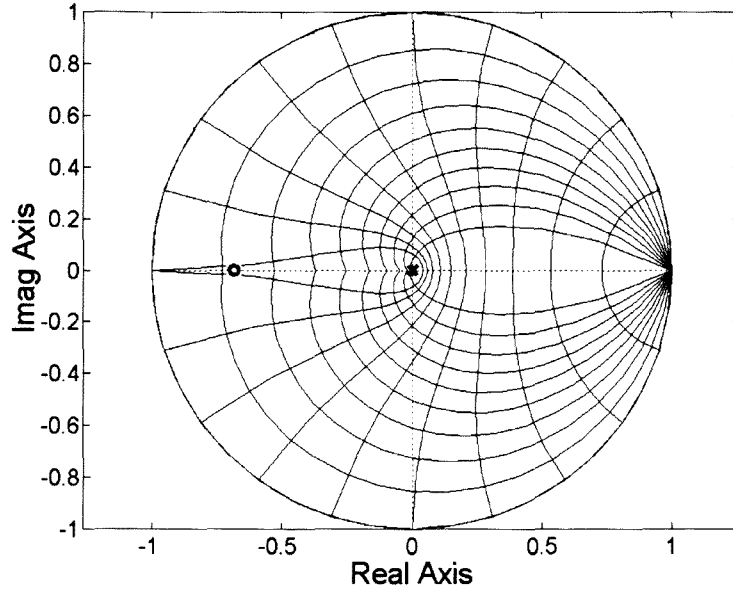


Figure 4.7: Pole-zero map with the poles shifted to the origin

The updated controller is simulated to show that the system is stable.

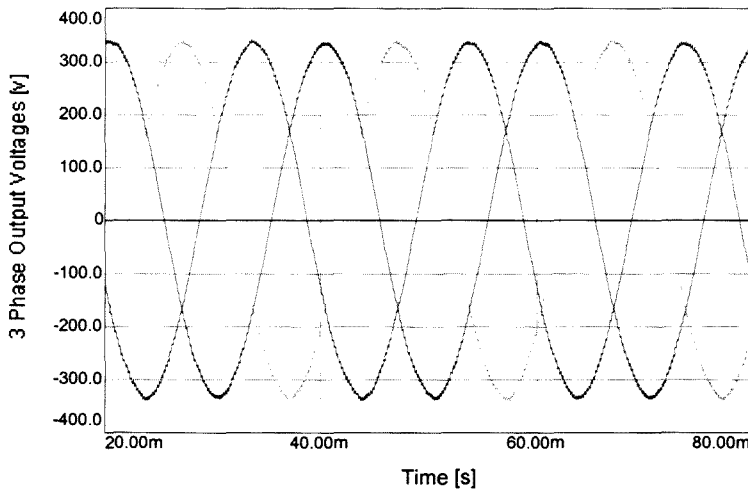


Figure 4.8: Output waveforms with time-delay compensation

Figure 4.8 shows that by modelling the hardware correctly, in this case, including the processor delay, a stable controller could be designed. An output voltage waveform with low distortion could therefore be produced.

4.7 Nullifying the steady-state error

Section 2.4.6 explained that a step input should render an output with zero steady-state error. With the controller as shown in Figure 4.3, the simulated output waveforms are smaller in magnitude than the reference voltages, depicted in Figure 4.9. The reason for this is that when there is an increase in load current, there will be an increase in the voltage drop over the filter inductor, resulting in an output voltage that is of smaller magnitude than the reference voltage.

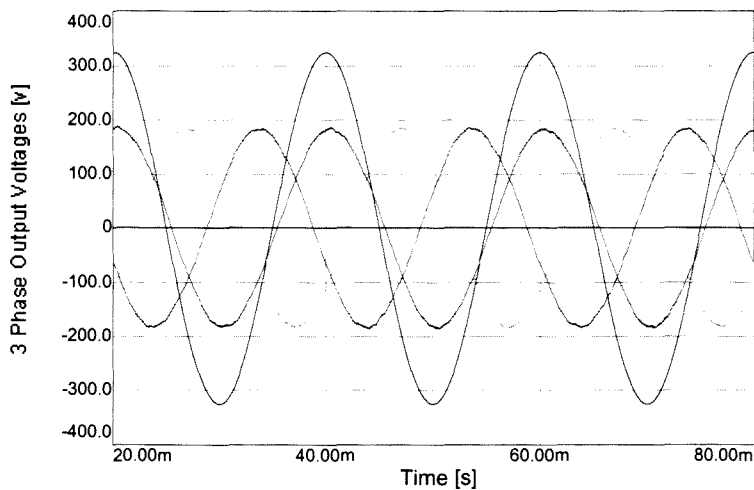


Figure 4.9: Output waveforms showing steady-state error

Therefore, a further extension to the control law would be to get the magnitude of a step input equal to one, in other words, to have a zero steady-state error. Section 2.4.6 explained the development of the N_u scalar and N_x vector. The control system is then given as depicted in Figure 4.10.

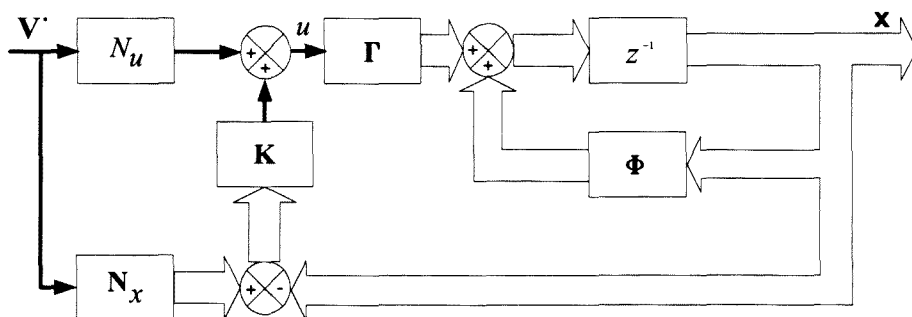


Figure 4.10: Control law updated to eliminate the steady-state error

Figure 4.11 shows that with the inclusion of N_u and N_x , the output waveforms are equal in magnitude and equal to the various reference voltages. The reference for phase A is shown as the black trace.

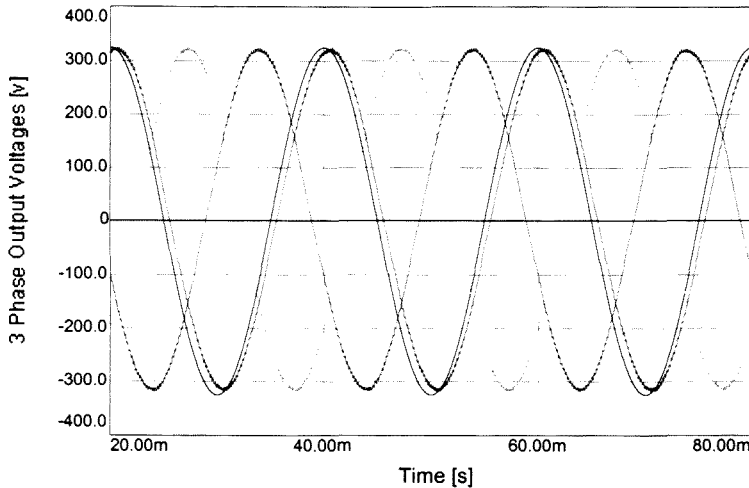


Figure 4.11: Steady-state error compensated for

4.8 Deadbeat control with various loads

Connecting a load to the system would give the system equation as

$$\mathbf{x}(k+1) = \Phi \mathbf{x}(k) + \Gamma \mathbf{V}(k) + \Gamma_i \mathbf{I}_o(k) \quad (4-24)$$

which would make the controlled system different from the one that the controller was designed for. The load is represented by $\mathbf{I}_o(k)$ in Equation (4-24) and its influence on the state matrix is given by Γ_i . The change in load current can be represented by the voltage over the capacitor and could therefore be included in the other system matrices, effectively changing the system. This will result in the output waveforms deviating from the reference vector, as depicted in Figure 4.12.

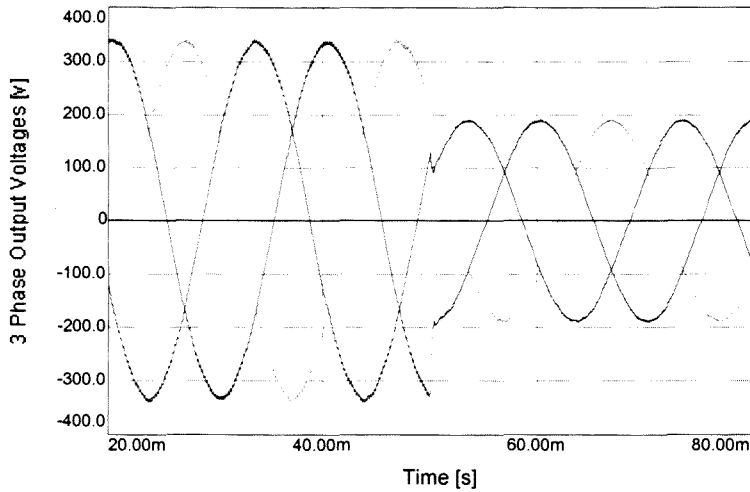


Figure 4.12: Error in the output waveforms due to load current

For the control system to be insensitive to these current variations, the system equation in Equation (4-24) is used to update the controller. This is shown in Figure 4.13.

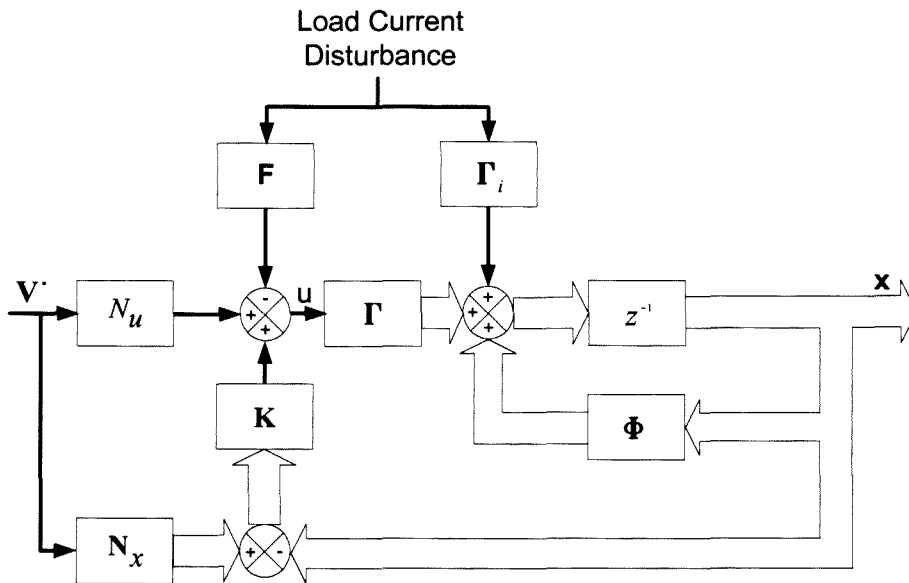


Figure 4.13: Load current feed-forward control

Now, define a vector, F that are used as a feed-forward matrix that would be used to update the control law, thus eliminating the loading effect. The new control law is

$$u = N_u V^* + K(N_x V^* - x) - F I_o \quad (4-25)$$

Substituting (4-25) into (4-5), it is found that

$$x(k+1) = \Phi x(k) + \Gamma(N_u V^* + K(N_x V^*(k) - x(k)) - F I_L(k)) + \Gamma_i I_o(k) \quad (4-26)$$

which is manipulated to be

$$x(k+1) = (\Phi - \Gamma K)x(k) + \Gamma N_u V^*(k) + \Gamma K N_x V^*(k) + (\Gamma_i - \Gamma F)I_o(k) \quad (4-27)$$

For the system to be unaffected by the load current, the term in Equation (4-27) that is multiplied by the load current, should equal zero. Thus,

$$\Gamma_i - \Gamma F = 0 \quad (4-28)$$

And, therefore

$$F = \frac{\Gamma_i}{\Gamma} \quad (4-29)$$

The same balanced load as used in Figure 4.12 is used to show the effect of the load current disturbance compensator. The output voltage waveforms are as shown in Figure 4.14.

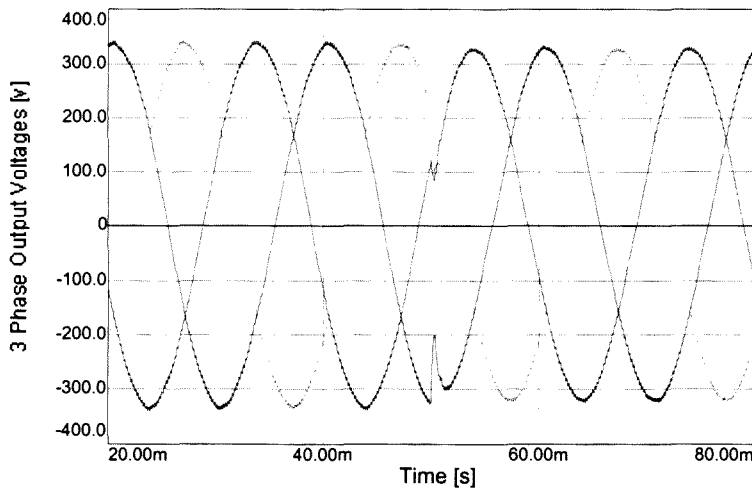


Figure 4.14: Compensation for load current fixes the magnitude difference

It is noted that the voltages are different in magnitude before and after the load transition. This is due to parasitic components in the system that are not included in

the system model. These mainly include the equivalent series resistance of respectively the filter inductor and filter capacitor. Voltage drops are induced over the filter inductors, which are increased by the increased load currents, resulting in a lower output voltage. A further explanation is that with the change in load, the open-loop system poles are situated at different locations than initially used in designing the **K**-vector. The designed **K**-vector will no longer shift the poles to the origin of the *z*-plane, but will shift it past the origin. The deadbeat algorithm would not react that quickly anymore, thus it could compromise the response of the system. Section 4.11 will introduce a technique called Auto-tuning. Here the load current is used to actively change the values of **K** that would keep the system poles located at the origin.

4.9 Evaluating the designed controller under various load conditions

Adding a fourth leg to the three-leg inverter, a four-leg inverter, as shown in Figure 4.15, is created. Connecting the load neutral to the midpoint of this fourth leg makes it possible to control the neutral point voltage, enabling the inverter to handle neutral currents that are caused by unbalanced loads or single-phase, non-linear loads. The four-leg inverter can therefore produce three independent output voltages [12], and it would be possible to keep these output voltages sinusoidal.

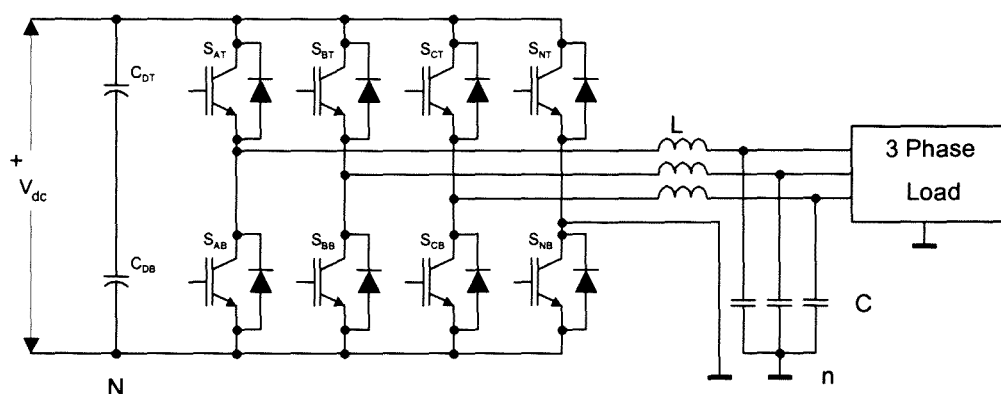


Figure 4.15: A three-phase, four-wire inverter with an output LC-filter

The rest of this section is devoted to giving simulated results of an open-loop controller and a closed-loop controller. Various loading conditions, including balanced, unbalanced and non-linear loads are used to evaluate the controllers, showing that a closed-loop controller gives better output voltage waveforms. The system under investigation produces three-phase output voltages of magnitude equal to $325 V_{\text{peak}}$, and delivers power of up to 250 kVA.

4.9.1 No load

The three phases of the inverter are left opened to see the performance of the system under no-load. It is first controlled using an open-loop controller, with the results given in Figure 4.16. It is seen that the three phases are all equal to the reference value of 325 V_{peak}.

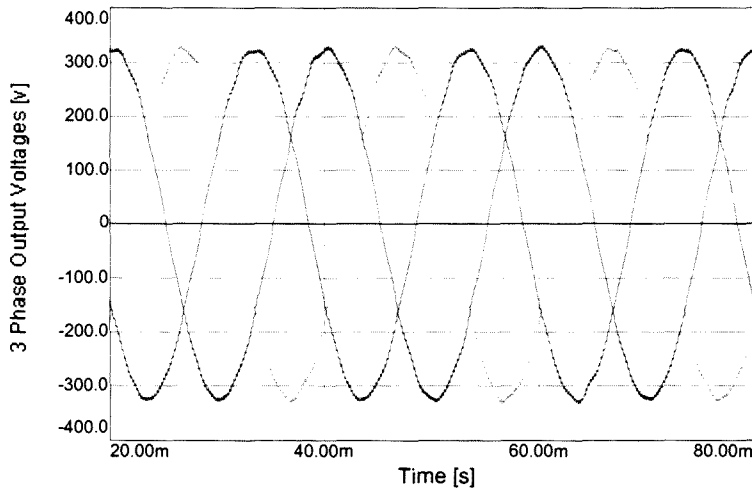


Figure 4.16: Balanced three-phase, 0 W load (Open-loop controlled)

The FFT is shown in Figure 4.17. The distortion on the peaks of the output waveforms in Figure 4.16 amounts to the THD being calculated as 1.5%.

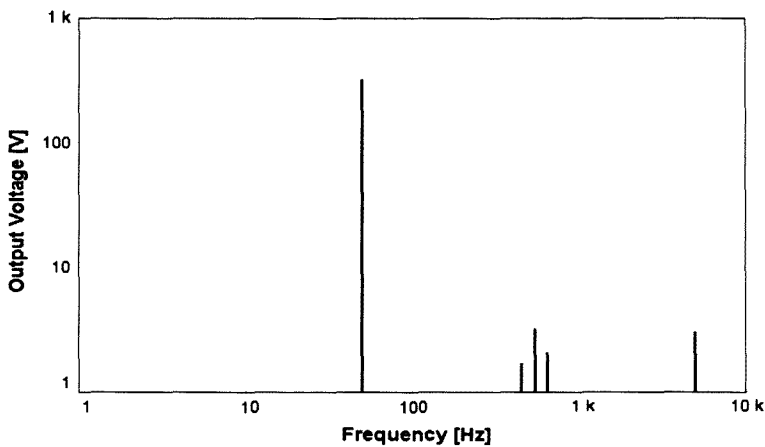


Figure 4.17: FFT, Balanced three-phase, 0 W load (Open-loop controlled)

The results when using the closed-loop controller are given in Figure 4.18. The three phases have equal magnitudes equalling $330 V_{\text{peak}}$, which amounts to a 1.5% steady-state error.

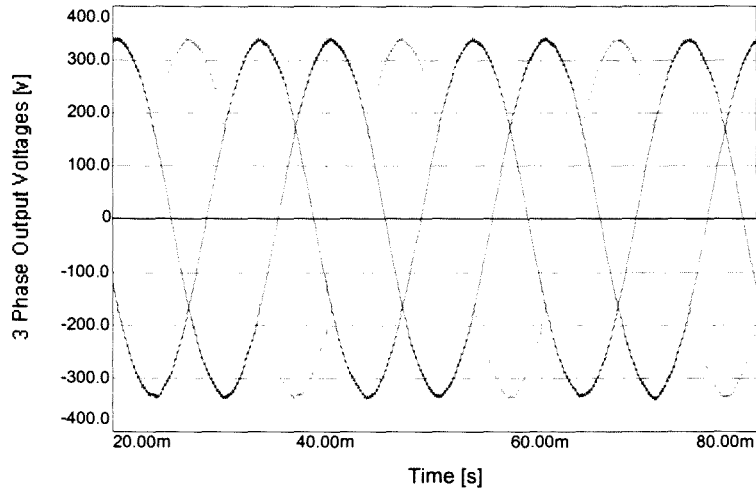


Figure 4.18: Balanced three-phase, 0 W load (Closed-loop controlled)

The FFT is shown in Figure 4.19, with the THD calculated as 0.8%. Comparing the THD of the open-loop and closed-loop controllers shows that the closed-loop controller produces voltages that have lower harmonic content than the open-loop controller.

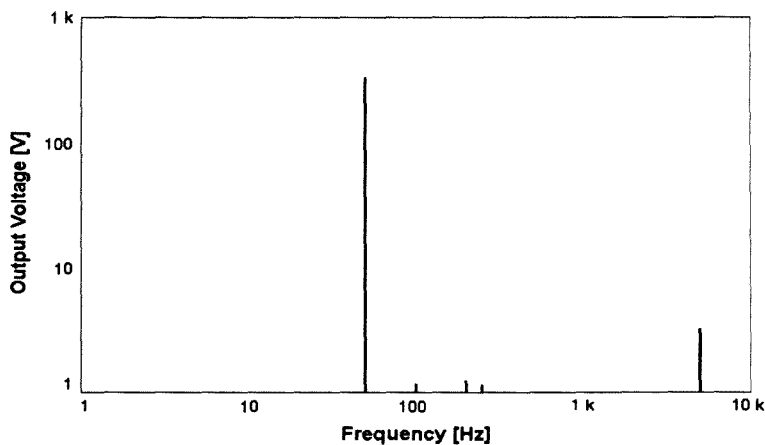


Figure 4.19: FFT, Balanced three-phase, 0 W load (Closed-loop controlled)

4.9.2 Balanced loads

A balanced linear load, each being 0.64Ω , totalling 250 kW three-phase power, was used to do the simulations. The three-phase output voltages of the open-loop controller are shown in Figure 4.20. The outputs have equal magnitudes equalling $320 V_{\text{peak}}$, which amounts to a 1.5% steady-state error.

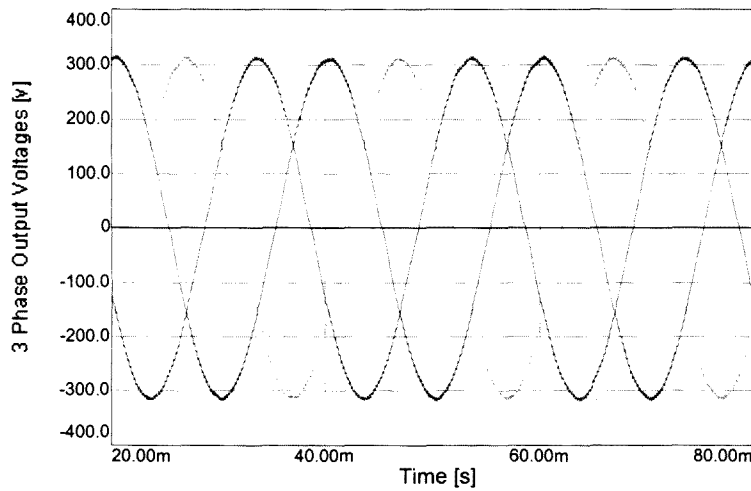


Figure 4.20: Balanced three-phase, 250 kW load (Open-loop controlled)

The FFT are given in Figure 4.21, with the output voltage THD calculated as 1.6%.

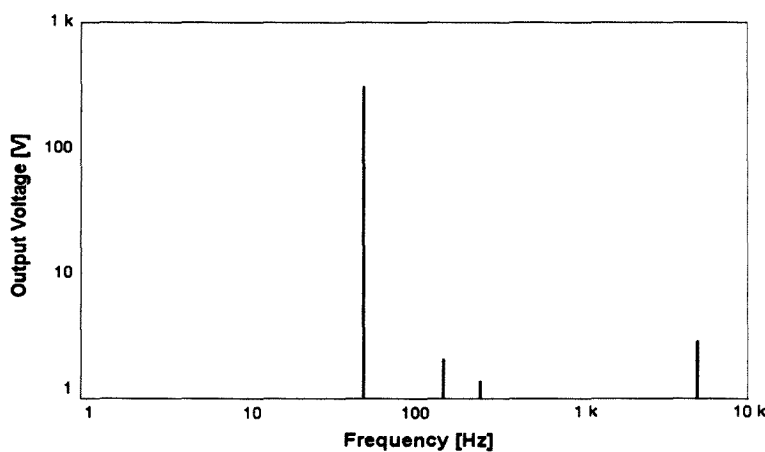


Figure 4.21: FFT, Balanced three-phase, 250 kW load (Open-loop controlled)

The results using the closed-loop controller are given in Figure 4.22. All three phases have equal magnitudes equalling $325 V_{\text{peak}}$, which amounts to a 0% steady-state error.

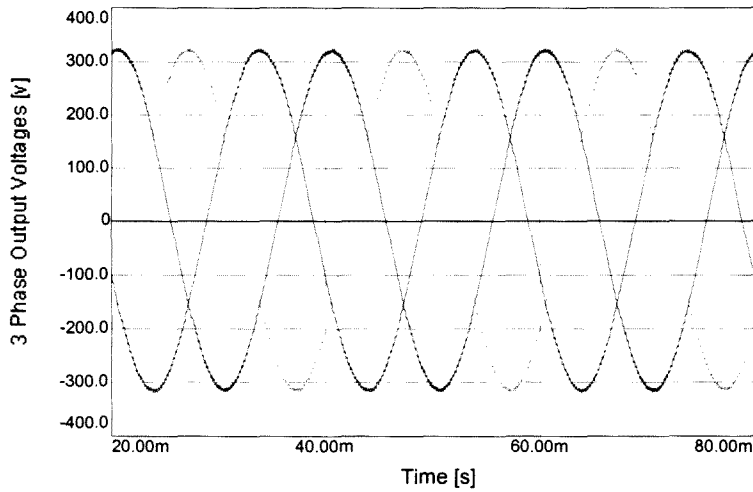


Figure 4.22: Balanced three-phase, 250 kW load (Closed-loop controlled)

The FFT is shown in Figure 4.23, with the THD calculated as 0.7%. It is also noted that the magnitude of the fundamental component equals only $315.8 V_{\text{peak}}$, which is smaller than the reference value. The harmonic components superimposed to the fundamental give the $325 V_{\text{peak}}$ as shown in Figure 4.22.

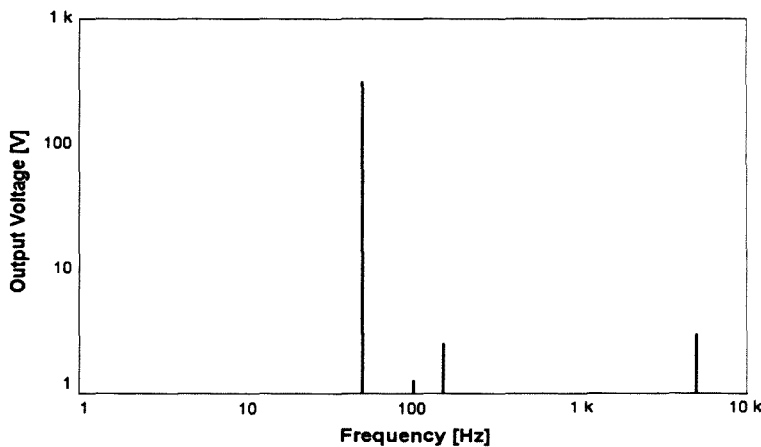


Figure 4.23: FFT, Balanced three-phase, 250 kW load (Closed-loop controlled)

4.9.3 Unbalanced loads

4.9.3.1 Unbalance of 25%

An unbalance of 25% would induce a neutral current with a peak magnitude of 220 A. The open-loop controlled output voltages, shown in Figure 4.24, are 300 V_{peak} for phase A, and 317 V_{peak} for phases B and C. This amounts to respectively a 7.7% and 2.5% steady-state error.

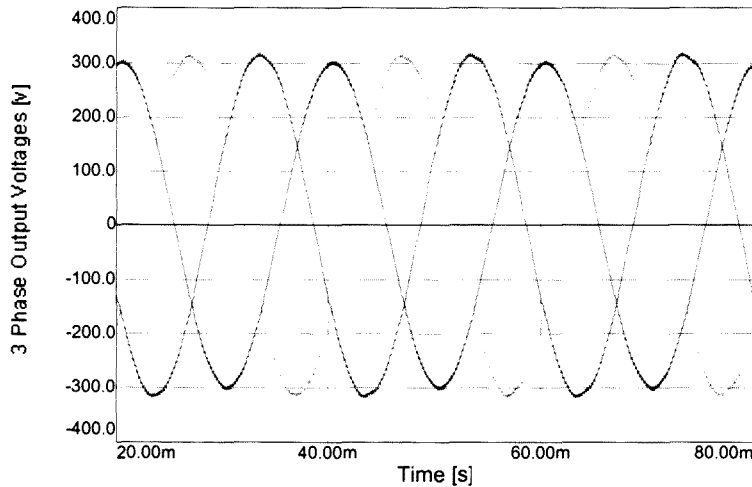


Figure 4.24: Unbalanced (25%), 100 kW load (Open-loop controlled)

The FFT is shown in Figure 4.25, with the THD calculated as 0.8%.

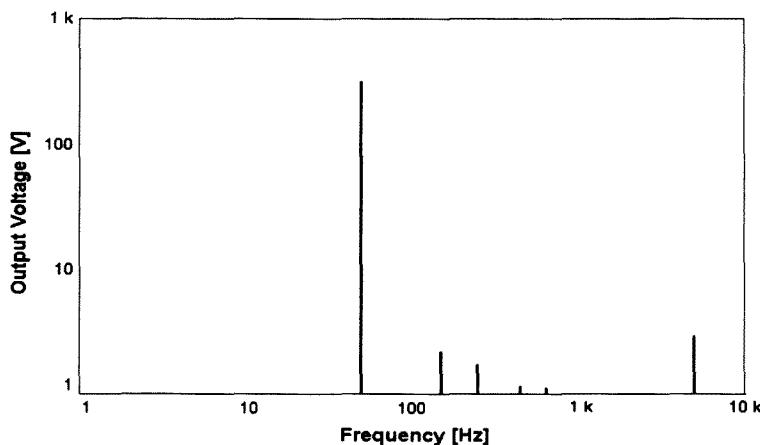


Figure 4.25: FFT, Unbalanced three-phase, 100 kW load (Open-loop controlled)

The closed-loop controller gives output voltages as shown in Figure 4.26. The magnitude of phase A is $318 V_{\text{peak}}$, and phases B and C's magnitudes are $324 V_{\text{peak}}$. This amounts to respectively 2.2% and 0.3% steady-state error.

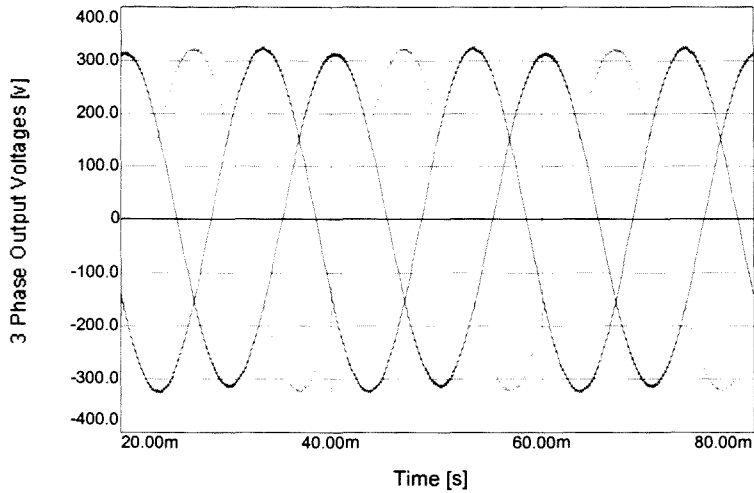


Figure 4.26: Unbalanced (25%), 100 kW load (Closed-loop controlled)

The FFT is given in Figure 4.27, with the THD calculated as 0.6%. The closed-loop controller produces outputs that have less voltage variation between the phases.

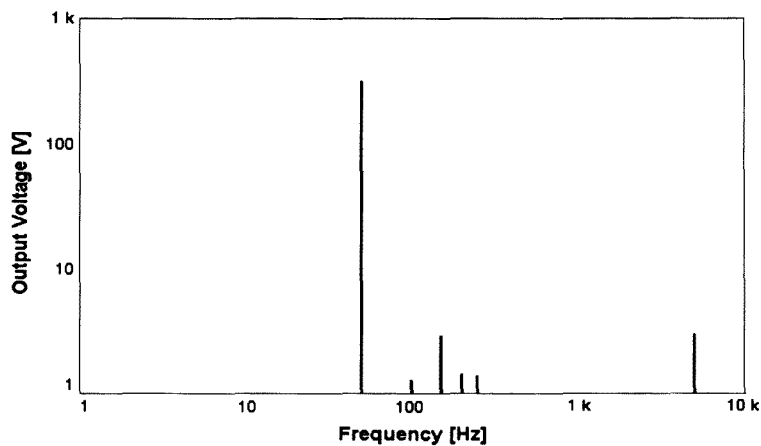


Figure 4.27: FFT, Unbalanced three-phase, 100 kW load (Closed-loop controlled)

4.9.3.2 Unbalance of 100%

100% unbalance was simulated with a single-phase, linear load connected to phase A. The output waveforms for the open-loop controller are as shown in Figure 4.28. The magnitude of phase A is equal to 298 V_{peak} and phase B and C are equal to 334 V_{peak}, which amounts to respectively a 8.3% and 2.8% steady-state error.

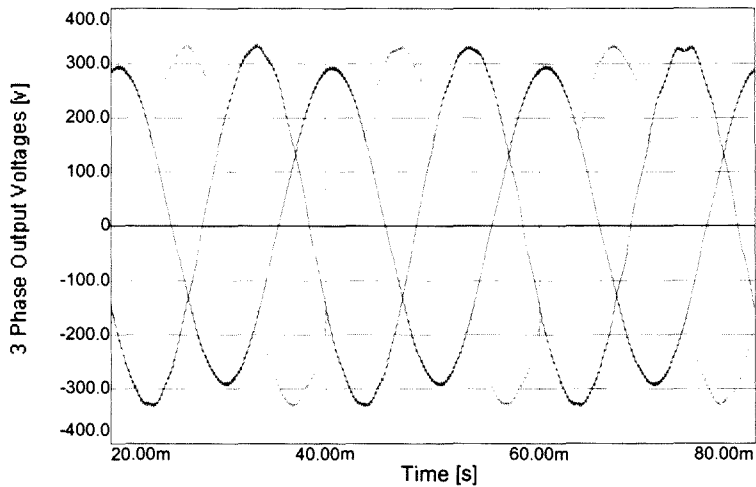


Figure 4.28: Unbalanced (100%), 65 kW load (Open-loop controlled)

The FFT are shown in Figure 4.29. The distortion observed in Figure 4.28 amounts to a THD calculated as 1.1%.

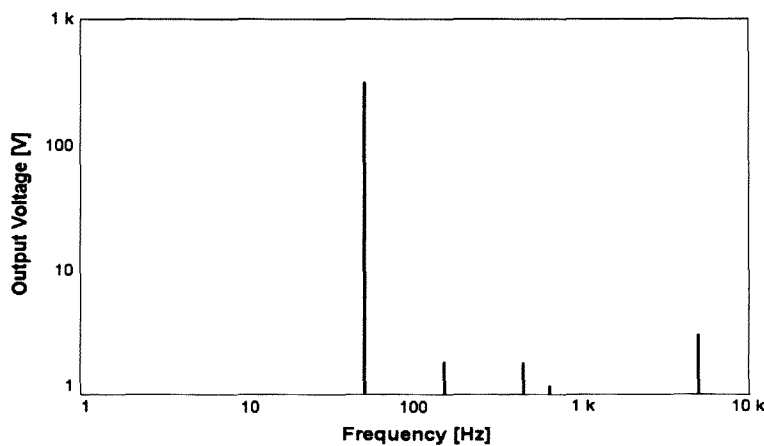


Figure 4.29: FFT, Unbalanced three-phase, 65 kW load (Open-loop controlled)

100% unbalance simulated with the closed-loop controller gives the output waveforms as shown in Figure 4.30. Here it is seen that the phase-magnitudes are much closer together, with phase A being $325 V_{\text{peak}}$ and phase B and C equal to $335 V_{\text{peak}}$, which amounts respectively to a 0% and 3% steady-state error. There is an 11.1% variation in the open-loop waveforms, with only a 3% variation in the closed-loop waveforms.

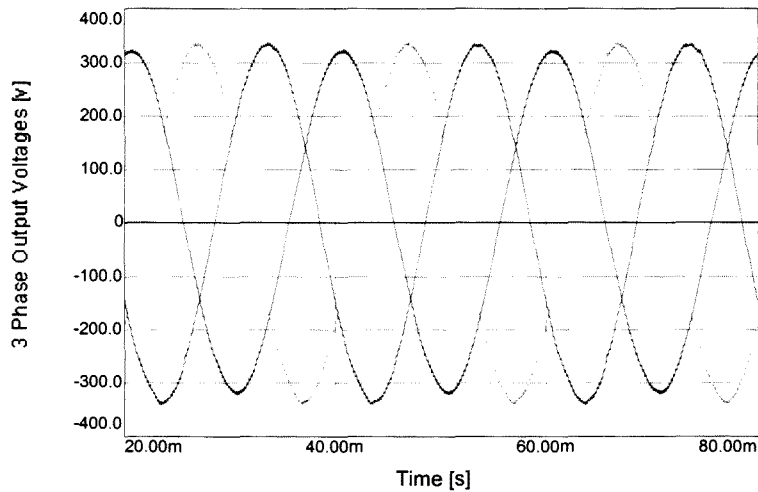


Figure 4.30: Unbalanced (100%), 65 kW load (Closed-loop controlled)

The FFT is given in Figure 4.31, with the THD calculated as 1%. The fundamental component of phase A is $320 V_{\text{peak}}$, which gives a 1.5% steady-state error.

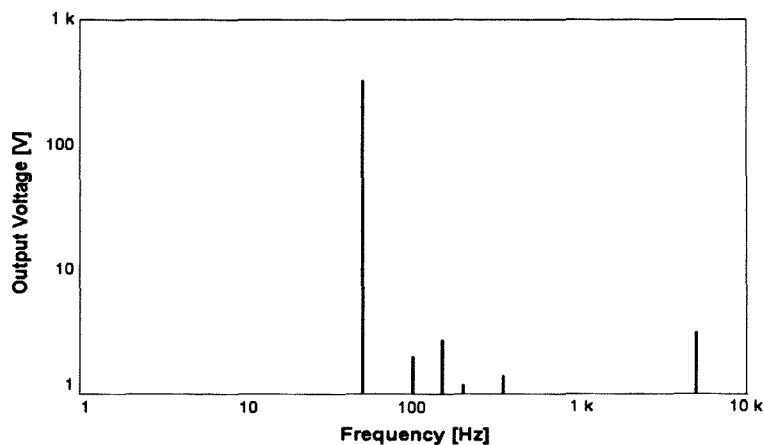


Figure 4.31: FFT, Unbalanced three-phase, 65 kW load (Closed-loop controlled)

4.9.4 Loads with a lagging power factor

For an inductive load with the current lagging the voltage by 25° , the output voltages of the open-loop controller are as shown in Figure 4.32. Phase A current is shown as the green trace. The magnitudes of all the phases are equal to $310 V_{\text{peak}}$, which amounts to a 4.6% steady-state error.

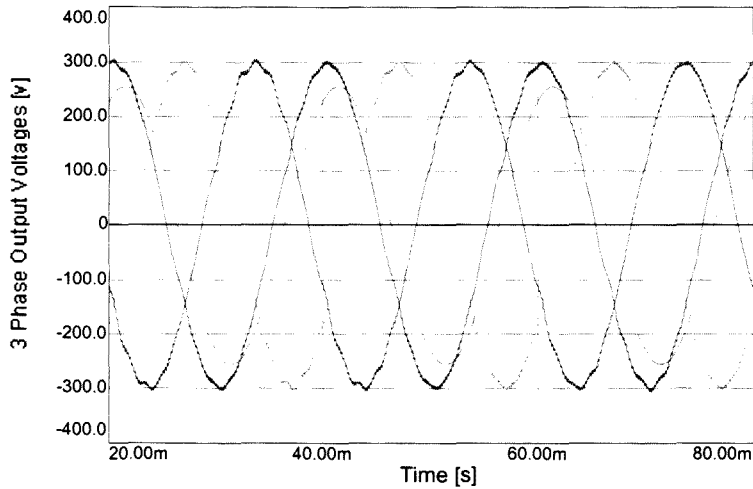


Figure 4.32: Balanced, inductive load, 150 kW (Open-loop controlled)

The FFT is shown in Figure 4.33, with the THD calculated as 1.8%.

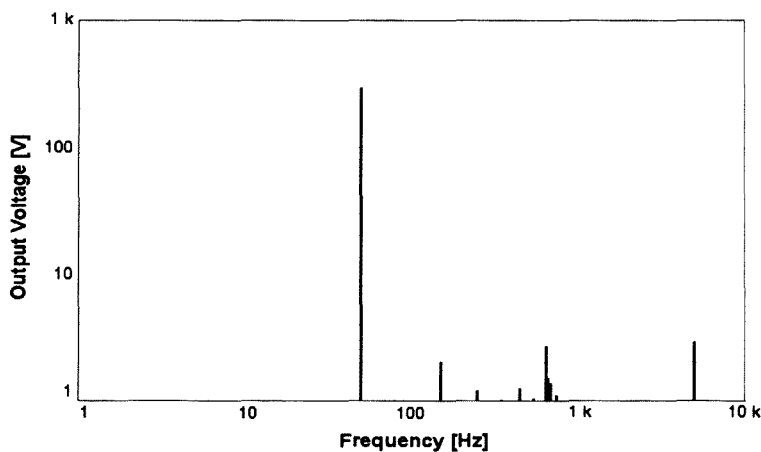


Figure 4.33: FFT, Balanced, inductive load, 150 kW (Open-loop controlled)

The closed-loop controller gives the output voltages as shown in Figure 4.34. Phase A current is again shown as the green trace. The output voltages have equal magnitudes equalling $322 V_{\text{peak}}$. This amounts to a 0.9% steady-state error.

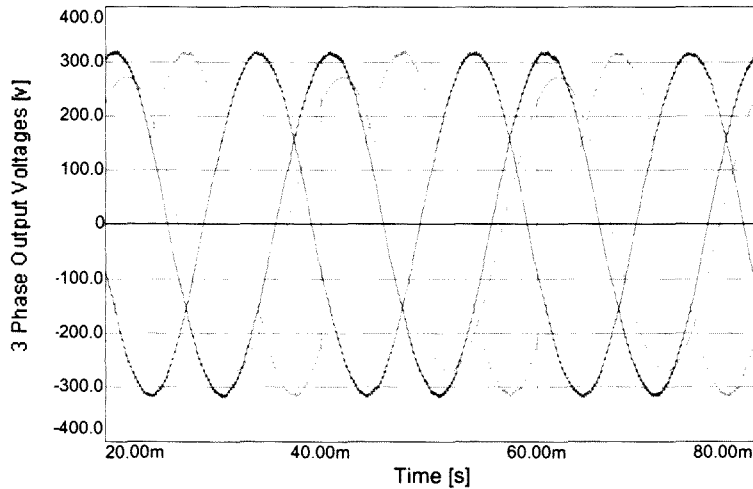


Figure 4.34: Balanced, inductive load, 150 kW (Closed-loop controlled)

The FFT is given in Figure 4.35, with the THD calculated as 1%. The closed-loop controller produces output waveforms with little harmonics, thus having a lower THD than the open-loop controller.

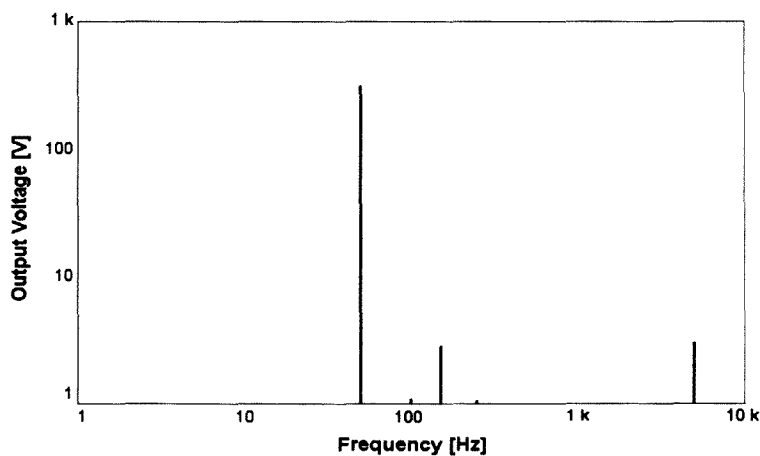


Figure 4.35: FFT, Balanced, inductive load, 150 kW (Closed-loop controlled)

4.9.5 Non-linear loads

The current that the load draws can be represented by current sources, including the fundamental and harmonic components, as shown in Figure 4.36. Thus, when the load is such that it draws currents caused by linear and non-linear loads, it is desirable that the output voltage waveform stays undistorted. Due to these various harmonic currents, voltage-drops of different frequencies will be over the series equivalent source impedance, which would result in the output voltage, V_o , being non-sinusoidal.

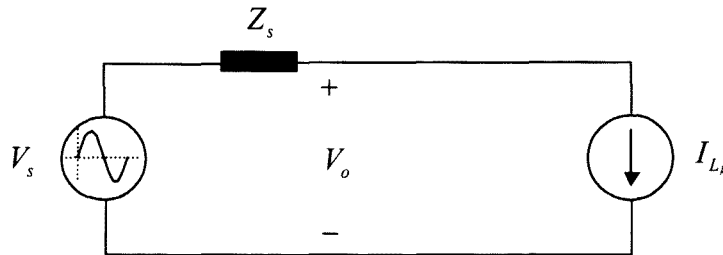


Figure 4.36: Non-linear load representation

The following section will show the differences in output waveforms between the open-loop and closed-loop controller. Both controllers still produce output waveforms that have a high harmonic content that is still higher than the allowed specifications [46], [47], [48]. The green traces in the figures show phase A current drawn by the load.

4.9.5.1 Open-loop controller

A three-phase diode rectifier with a L/C dc-link filter was used to simulate a non-linear load. The power rating is 45 kW. The current THD increases with an increasing capacitance. The capacitance for this simulation was chosen as 3.3 mF, the inductance as 1.2 mH and the resistive load as 7.7 Ω , producing a load current that has a crest factor of 1.6. The output waveforms are shown in Figure 4.37, with each phase equalling 330 V_{peak}. This amounts to a 1.5% steady-state error.

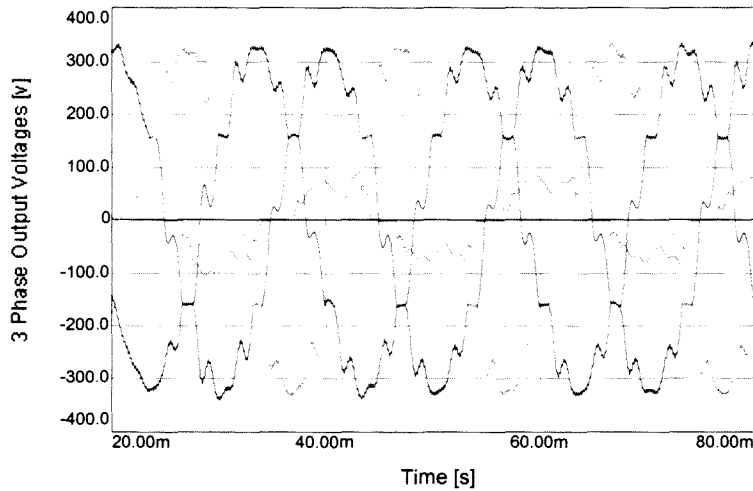


Figure 4.37: Non-linear, three-phase rectifier outputs, 45 kW (Open-loop controlled)

The FFT is shown in Figure 4.38, with the THD calculated as 8.2%.

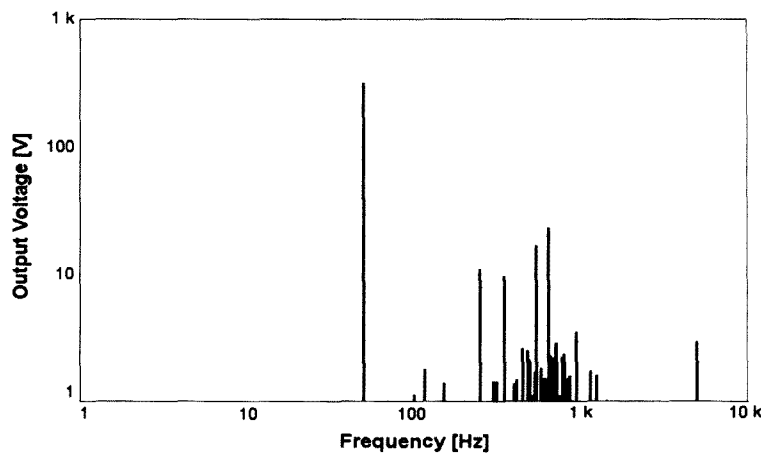


Figure 4.38: FFT of non-linear rectifier load, 45 kW (Open-loop controlled)

4.9.5.2 Closed-loop Controller

The closed-loop controller produces output waveforms as shown in Figure 4.39. All three phases have a magnitude equal to $323 V_{\text{peak}}$, which amounts to a 0.6% steady-state error.

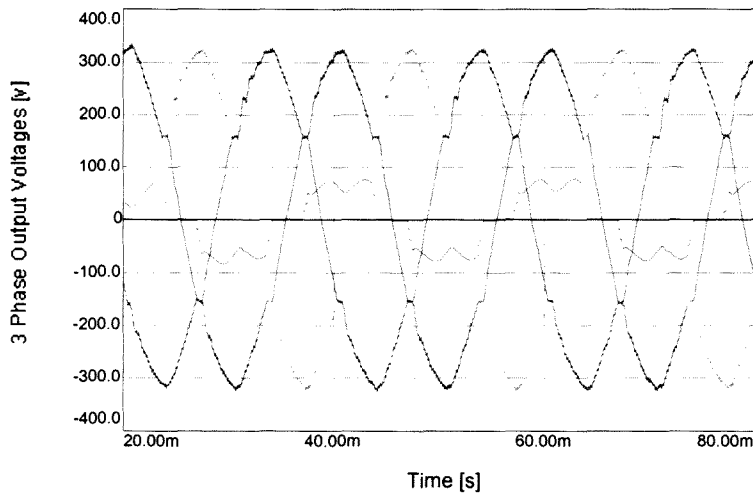


Figure 4.39: Non-linear, three-phase rectifier outputs, 45 kW (Closed-loop controlled)

The FFT is shown in Figure 4.40, with the THD calculated as 5.5%. The closed-loop controller renders waveforms with fewer harmonic components, therefore the THD is lower than that of the open-loop controlled counterpart.

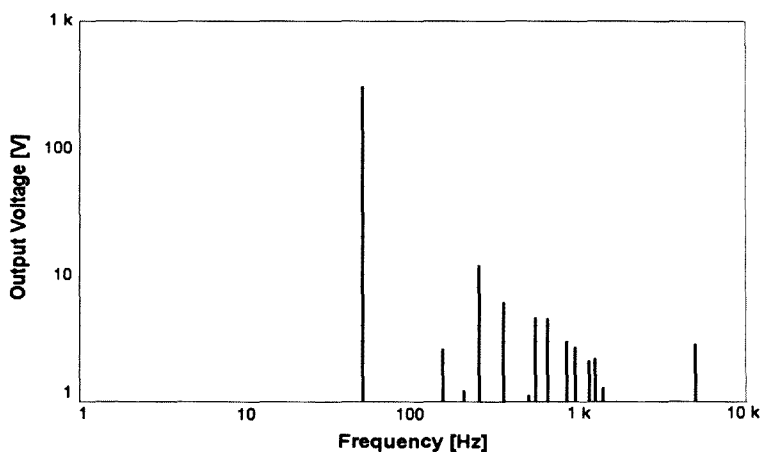


Figure 4.40: FFT of non-linear rectifier load, 45 kW (Closed-loop controlled)

4.10 Factors limiting the controller performance

High-power applications have the tendency to limit the switching frequency due to the power dissipation in the switching devices. This is shown in Equation (4-30) [38].

$$P_s = \frac{1}{2} V_{dc} I_L f_s (t_{on} + t_{off}) \quad (4-30)$$

It is obvious that the losses vary linearly with the switching frequency, and that it is not practical to switch at a very high frequency due to the overpowering switching losses. This is one of the reasons why it is impossible to achieve an output voltage waveform with a low THD. Other factors include dead time needed for switches to commutate and the calculation delay that gets introduced when using DSP's for digital control. Dead time is a function of the turn-off time of the switching devices and is conservatively chosen to avoid cross-conduction current through an inverter leg. A longer dead time would thus protect the switching devices, but with the disadvantage of increasing the THD due to the output voltage being uncontrollable for these time instants. The DSP calculation time can be minimized by using a faster DSP, but would bring extra costs, as different sampling equipment has to be used to improve the sampling and to avoid aliasing. Simulations will show the effect that these various factors have on the quality of the output voltage waveform.

4.10.1 Using a switching frequency of 20 kHz

Ignoring the losses introduced by using a higher switching frequency, it can be shown that it would be possible to increase the quality of the output voltage waveform by increasing the switching frequency.

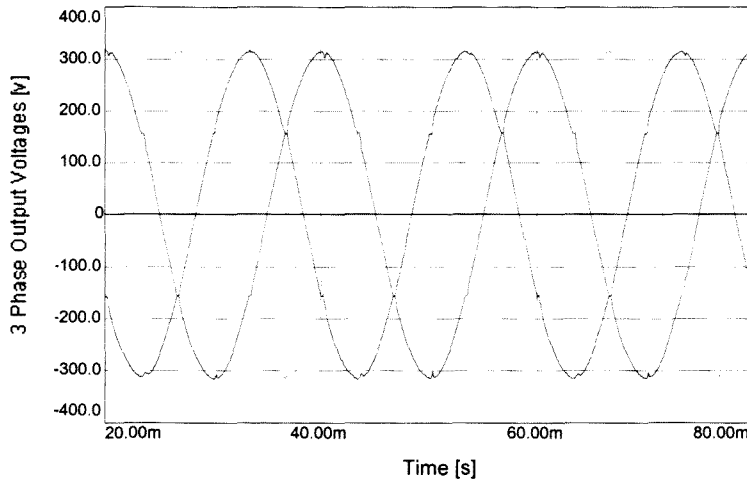


Figure 4.41: Output voltage waveforms of a non-linear load with a high switching frequency

From Figure 4.41 it is clear that the waveform is of better quality, compared to Figure 4.39, where a switching frequency of 5 kHz was used. The ratio of calculation time versus switching period is kept constant to give a proper comparison between the various switching frequencies. The THD is calculated as 0.9%, with the FFT shown in Figure 4.42.

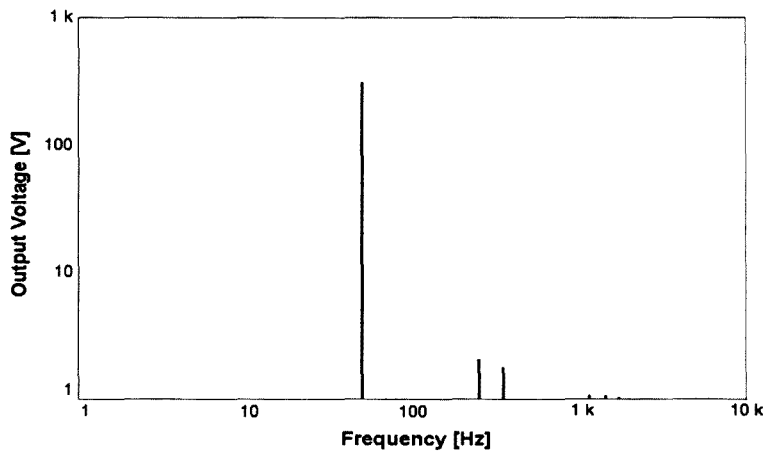


Figure 4.42: FFT of output voltage

4.10.2 The effect of dead time

Dead time is implemented to ensure that both switches in a phase arm are not simultaneously on. This would short the dc-bus, with drastic effects. No voltage is applied for this time, and this would result in an error in the output voltage. The error depends on the direction of the load current, as is shown in Figure 4.43 [38]. The output voltage waveform will have a higher THD when a longer dead time is used, because, for this time, the voltage is uncontrollable. The following simulations show the effect of using different dead times.

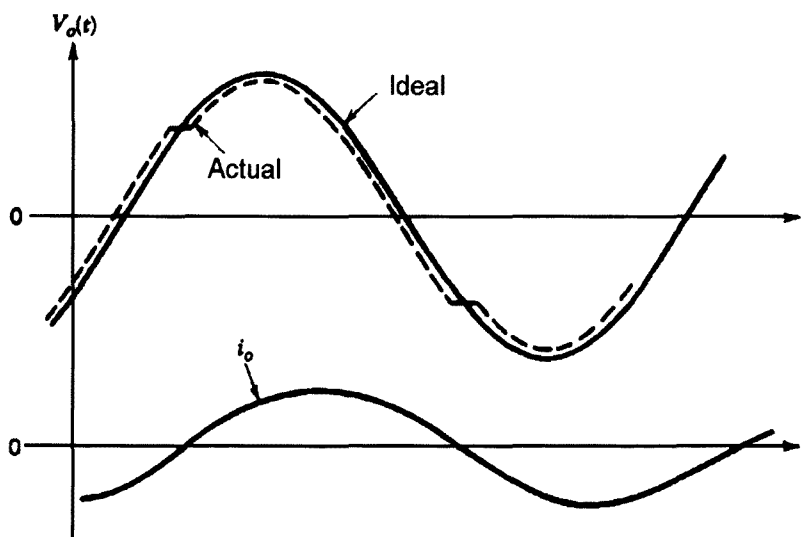


Figure 4.43: Distortion in output voltage due to dead time

4.10.2.1 Dead time equal to $1 \mu\text{s}$

For the first simulation a dead time equal to $1 \mu\text{s}$ was chosen, with the system power equal to 250 kW. The output voltage of a linear, balanced load is shown in Figure 4.44. The magnitude of the output voltage is equal to $320 V_{\text{peak}}$, which amounts to a 1.5% steady-state error.

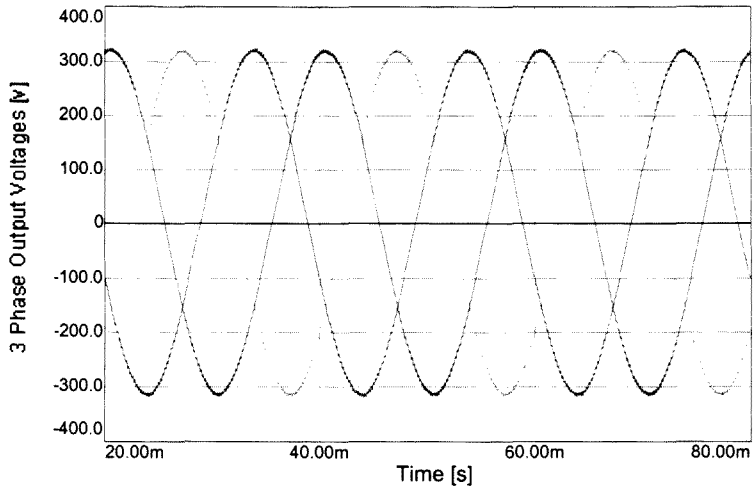


Figure 4.44: Output voltage with dead time equal to $1\mu\text{s}$

The FFT is shown in Figure 4.45, with the THD calculated as 0%.

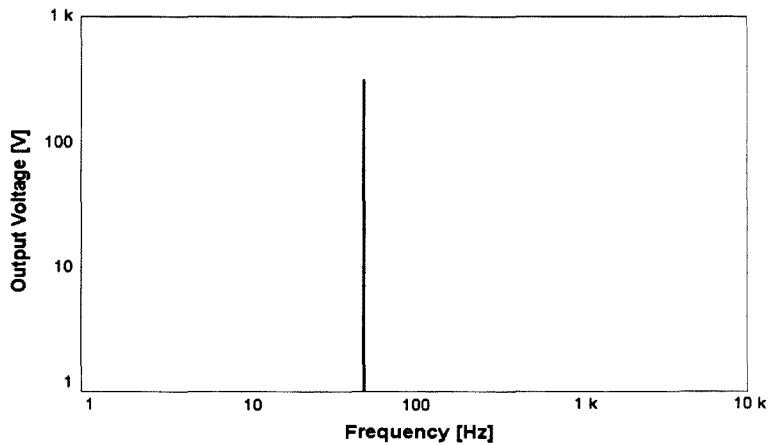


Figure 4.45: FFT of output voltage

4.10.2.2 Dead time equal to $10\mu\text{s}$

A longer dead time, equal to $10\mu\text{s}$, is used to show the effect on the output voltage. Again, a linear, balanced load is used to do the comparison. Figure 4.46 shows the output voltage when the dead time is increased to $10\mu\text{s}$.

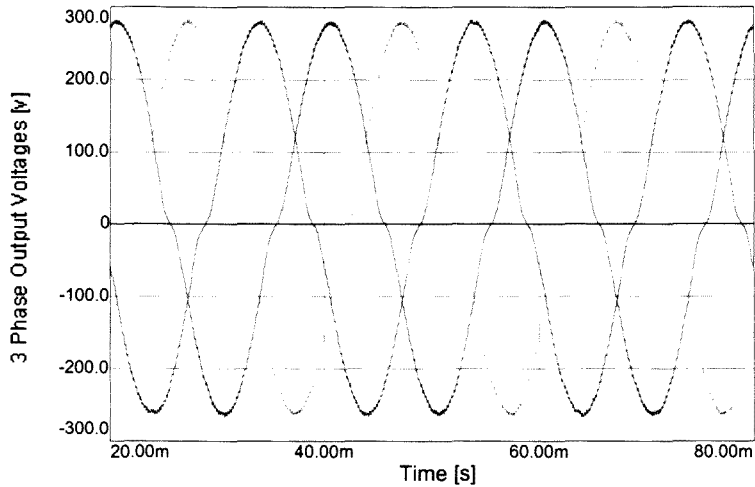


Figure 4.46: Output voltage with dead time equal to $10\mu\text{s}$

The FFT is shown in Figure 4.47.

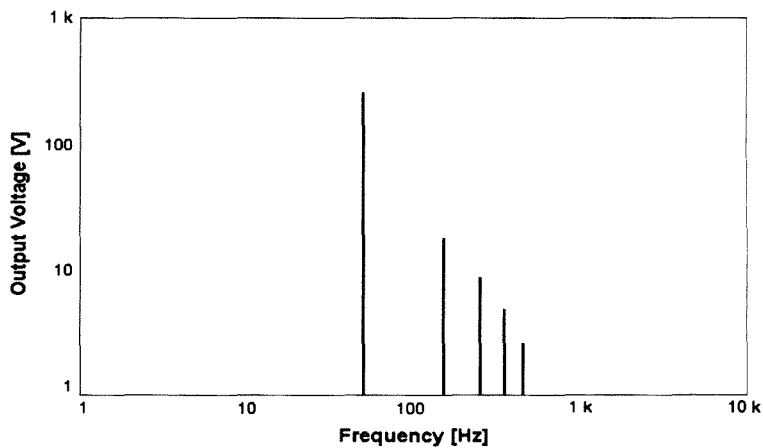


Figure 4.47: FFT of output voltage

It is noted that the output voltage waveform is distorted, with an increase in the 3rd, 5th, 7th and 9th harmonics. This would add to the harmonics when non-linear loads are used, resulting in an even worse output voltage waveform. The magnitudes of the output voltages are $280 V_{\text{peak}}$, which amounts to a 14% steady-state error. Therefore, appropriate switching devices should be used to guarantee short enough dead time to minimize the voltage distortion and to minimize the steady-state error.

4.10.3 Calculation time

With the speed of DSP devices changing constantly, it would be possible to design a new controller that could react more quickly to any change in voltage. This would ensure a voltage with much less distortion, and would therefore have a lower THD. The control gains are updated to include the different calculation delay.

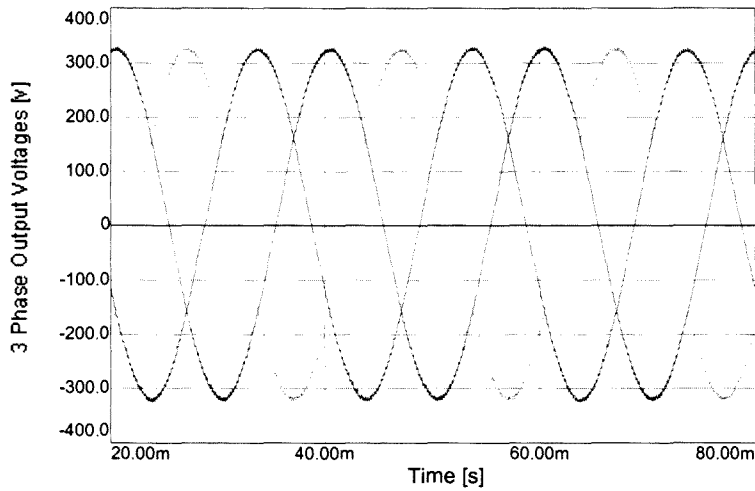


Figure 4.48: Output voltage with a reduced calculation delay

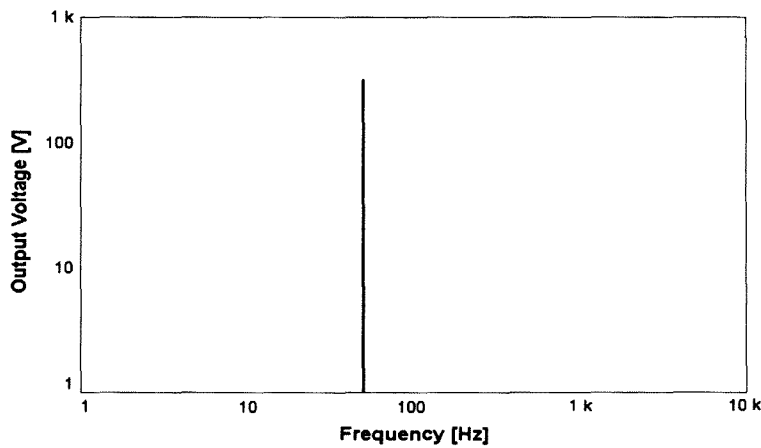


Figure 4.49: FFT of the output voltage with less calculation delay

The output voltage waveform is still of acceptable quality with the THD 0%. The magnitude is now $321 V_{\text{peak}}$, which amounts to a steady-state error of only 1%. There is better control over the output voltage, as compared to Figure 4.44, therefore the output is closer to the reference.

4.11 Auto-Tuning

The controllers for the various loads in Section 4.9 are all designed with a fixed \mathbf{K} -vector, depending on the load condition. Variations in the load conditions will produce a system that is different from the one that the \mathbf{K} -vector was designed for. The pole-placement technique used to shift the poles to the origin will now actually shift the poles past the origin. A typical situation is illustrated in Figure 4.50.

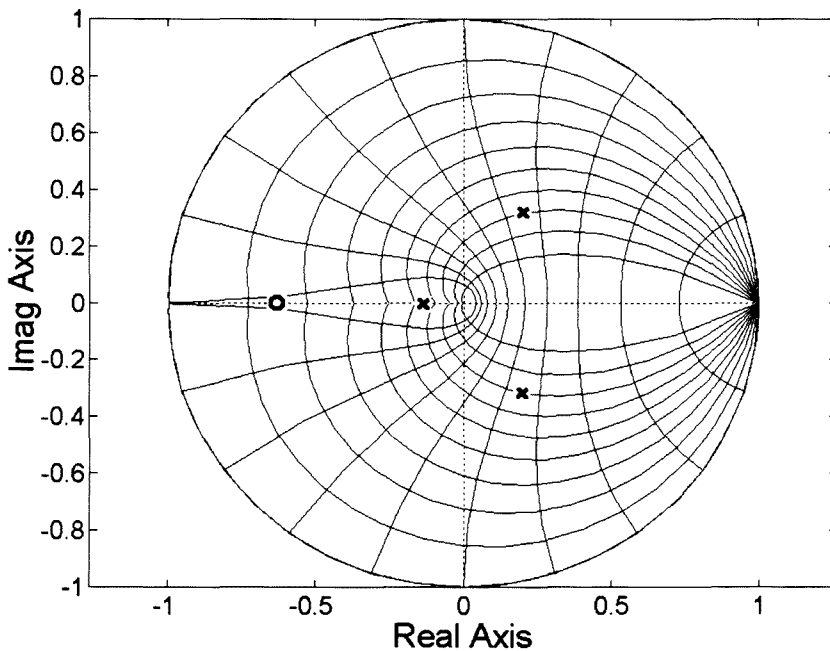


Figure 4.50: Pole and zero locations of a system with the wrong \mathbf{K} -vector

An algorithm had to be developed to compensate for these changes to keep the poles situated at the origin. It is possible to eliminate the effect associated with a change in the system dynamics by using a gain scheduler [37]. This controller tunes its own parameters such that the controller parameters are changed to counteract any changes in the plant. Such a scheduler is shown in Figure 4.51.

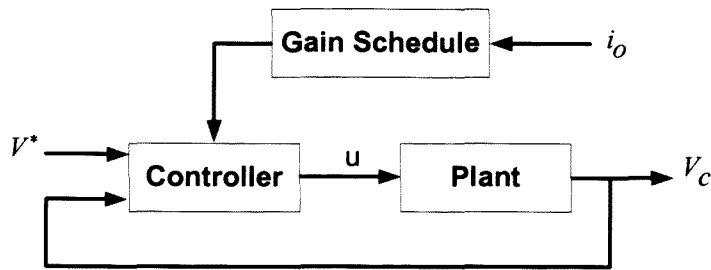


Figure 4.51: Parameter variations are eliminated by gain scheduling

The **K**-vector changes according to the peak current that is drawn by the load. The **K**-vector for a system with a filter inductance of 400 μH and a filter capacitance of 200 μF , which draws currents ranging from 0 A_{peak} to 650 A_{peak} , is given in Table 4.1. These values are calculated assuming a resistive load, with the **K**-vector moving the poles to the origin in the discrete plane. Table 4.1 is used to interpolate three different functions such that a **K**-vector can be calculated for arbitrary load currents drawn by the system.

Table 4.1: **K**-values for varying loads

Current, I_{max} [A]	K -vector
650	[-0.4226 1.7018 0.8452]
325	[-0.6178 1.9458 0.9688]
163	[-0.6294 2.3295 1.1143]
109	[-0.5760 2.5336 1.1836]
82	[-0.5301 2.6553 1.2232]
65	[-0.4949 2.7355 1.2487]
55	[-0.4678 2.7921 1.2665]
47	[-0.4465 2.8343 1.2796]
41	[-0.4294 2.8668 1.2896]
36	[-0.4155 2.8927 1.2975]
33	[-0.4039 2.9138 1.3040]
0	[-0.2799 3.1187 1.3654]

The polynomial that fits K_1 the best is a third-order polynomial. The calculated and interpolated functions are shown in Figure 4.52.

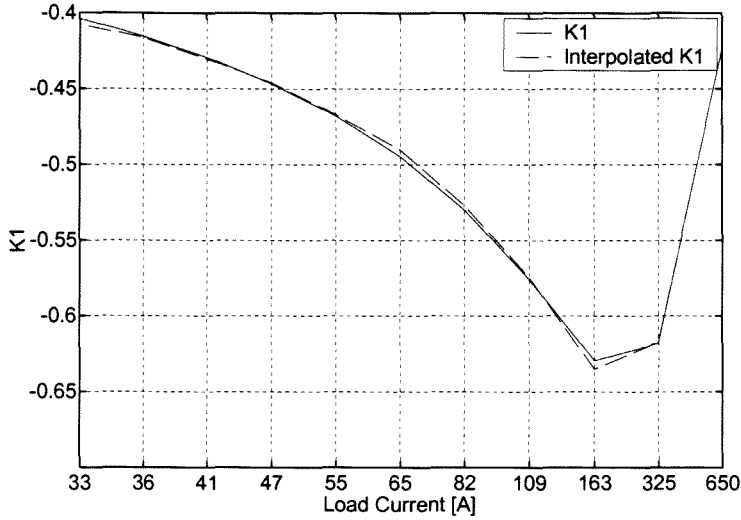


Figure 4.52: Calculated and interpolated K_1 versus load current

Both functions for K_2 and K_3 are interpolated using a second-order polynomial. The calculated and interpolated functions for respectively K_2 and K_3 are shown in Figure 4.53 and Figure 4.54.

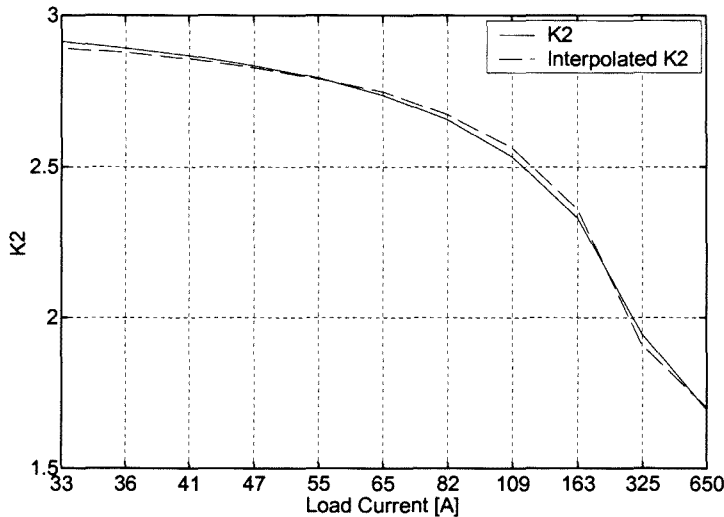


Figure 4.53: Calculated and interpolated K_2 versus load current

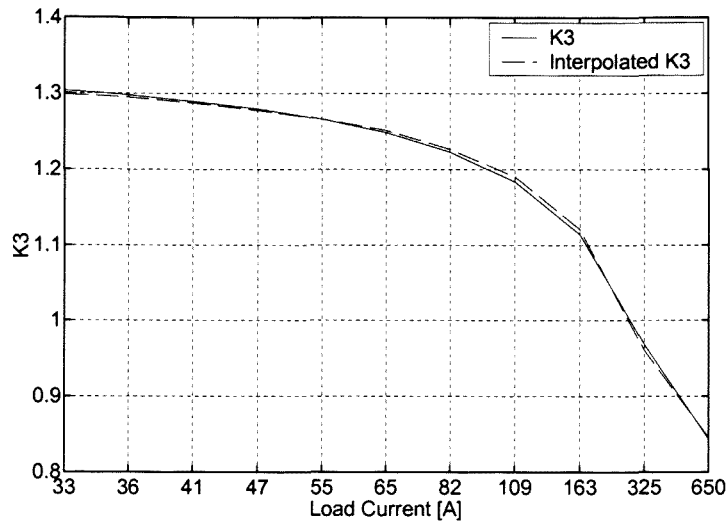


Figure 4.54: Calculated and interpolated K_3 versus load current

The calculated polynomials are given in Equations (4-31) through (4-33).

$$K_1 = -8.7241 \times 10^{-9} I_{avg}^3 + 1.0921 \times 10^{-5} I_{avg}^2 - 0.0036 I_{avg} - 0.3004 \quad (4-31)$$

$$K_2 = 4.4424 \times 10^{-6} I_{avg}^2 - 0.0049 I_{avg} + 3.0508 \quad (4-32)$$

$$K_3 = 1.3055 \times 10^{-6} I_{avg}^2 - 0.0016 I_{avg} + 1.3516 \quad (4-33)$$

A three-phase, 75 kW, resistive load was used to simulate the effectiveness of the gain scheduler. Figure 4.55 shows the change in controller gains at 40ms.

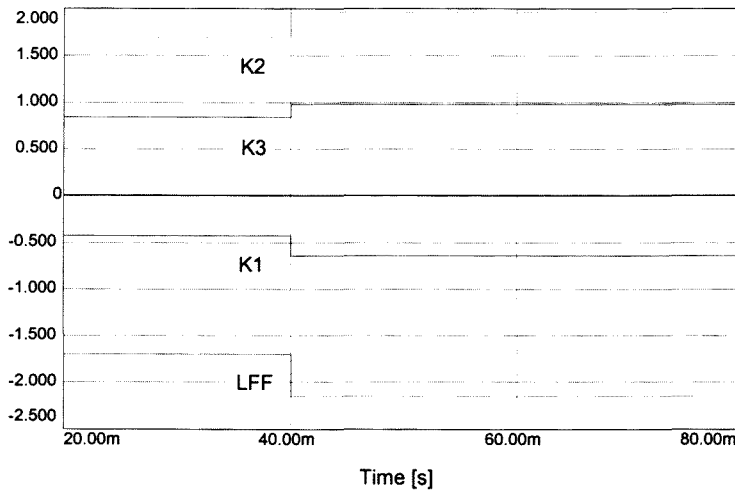


Figure 4.55: Auto-tuning of controller gains

The change in the output voltage waveforms is seen in Figure 4.56. Before the auto-tuning is done, the output voltage is $300\text{ V}_{\text{peak}}$, which amounts to a 7.7% steady-state error. After the auto-tuning is done, the output voltages are of magnitude $325\text{ V}_{\text{peak}}$. This amounts to a 0% steady-state error.

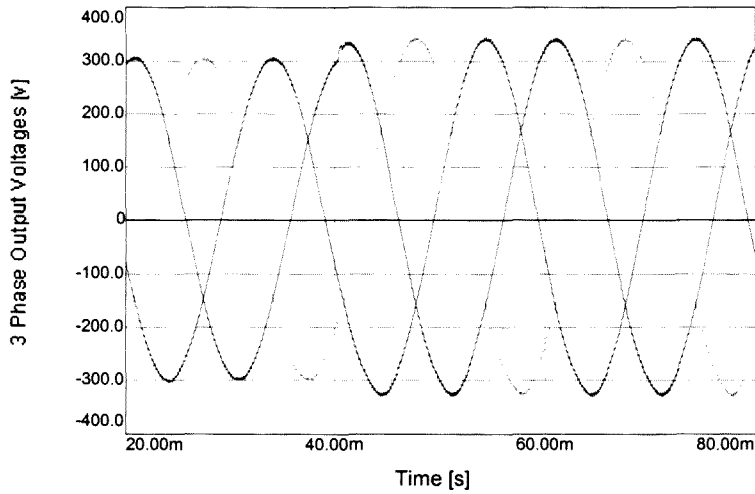


Figure 4.56: Output voltage waveforms with auto-tuner implemented

4.11.1 Different loading conditions with auto-tuning

Figure 4.57 shows a simplified system diagram and the equivalent phase-diagram representation. The red lines represent a resistive load, while the blue lines represent an inductive load. Depending on the type of load, the supply voltage, V_{sr} or V_{si} , would have different magnitudes to produce the same magnitude output voltage, although the same magnitude current is drawn. The controller gains are calculated assuming a resistive load, which would result in the output voltage, V_o , being smaller if the phase angle of the load is not considered in the calculation of the gains. One way of achieving this is to amplify the load current feed-forward gain, effectively increasing the reference.

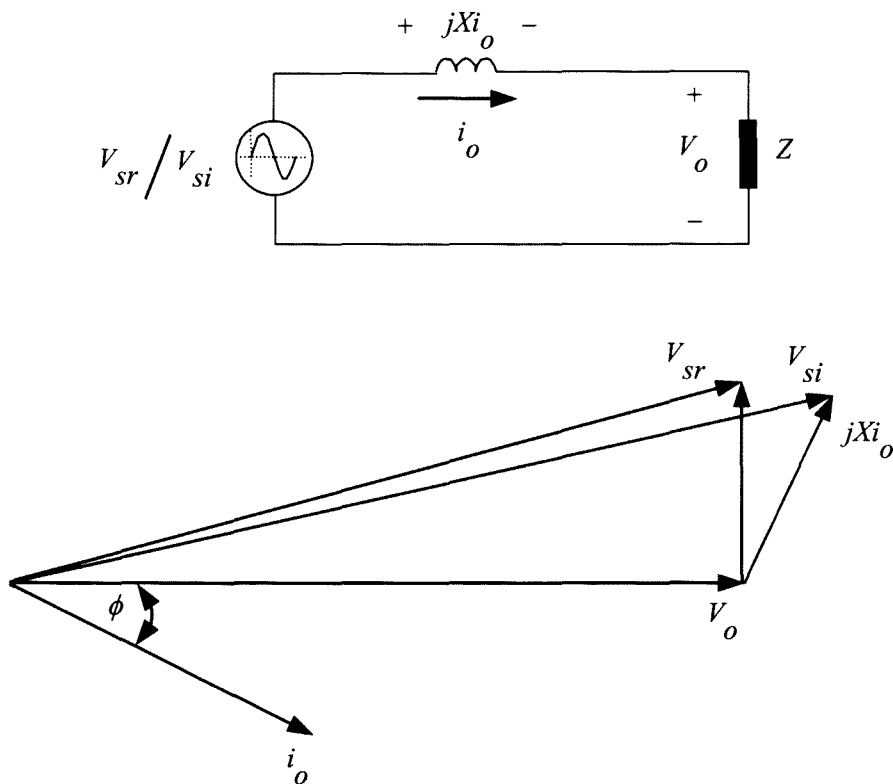


Figure 4.57: Simplified system diagram and phase-diagram representation

A mathematical expression to relate the magnitude of V_{sr} to the magnitude of V_{si} can be used to assist in finding an equation that would give the error in the output voltage waveforms as the load current increases. Figure 4.58 is used to find this equation.

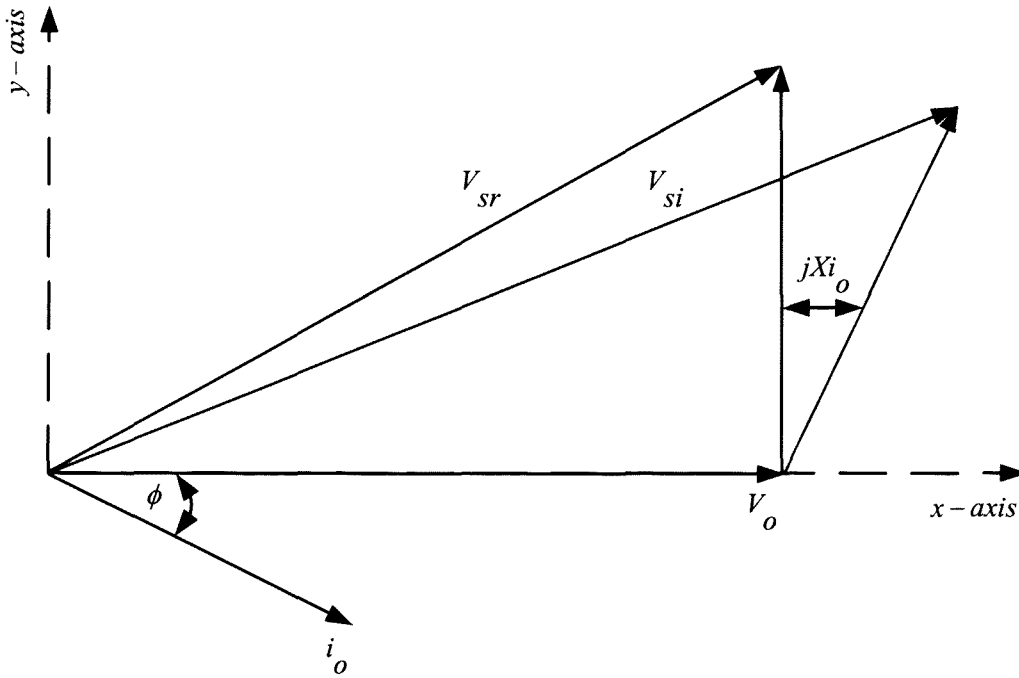


Figure 4.58: Amplification of phase-diagram

A resistive load would produce an output current, i_o , which is in phase with the output voltage, V_o . In Cartesian co-ordinates, these vectors are expressed as:

$$\mathbf{V}_o = \begin{bmatrix} \mathbf{V}_{ox} \\ \mathbf{V}_{oy} \end{bmatrix} = \begin{bmatrix} |\mathbf{V}_o| \\ 0 \end{bmatrix} \quad (4-34)$$

$$\mathbf{I}_o = \begin{bmatrix} \mathbf{I}_{ox} \\ \mathbf{I}_{oy} \end{bmatrix} = \begin{bmatrix} |\mathbf{I}_o| \\ 0 \end{bmatrix} \quad (4-35)$$

The voltage drop over the filter inductor, V_x (expressed as $jX_i i_o$ in Figure 4.58) leads the output current by 90° . Therefore, the current i_o has to be rotated counter-clockwise by 90° . A linear transformation, given as Equation (4-36) [45], is used to rotate each point on the current vector by 90° .

$$\mathbf{T}_{lin} = \begin{bmatrix} \cos \phi & -\sin \phi \\ \sin \phi & \cos \phi \end{bmatrix} \quad (4-36)$$

With ϕ being 90° , Equation (4-36) is now given as Equation (4-37).

$$\mathbf{T}_{lin} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \quad (4-37)$$

The voltage drop over the filter inductor is then

$$\mathbf{V}_L = \omega L \mathbf{T}_{lin} \mathbf{I}_o = \omega L \begin{bmatrix} 0 \\ |\mathbf{I}_o| \end{bmatrix} \quad (4-38)$$

The reference is calculated as

$$\mathbf{V}_{sr} = \mathbf{V}_o + \mathbf{V}_L = (|\mathbf{V}_o|)_{x-axis} + (\omega L |\mathbf{I}_o|)_{y-axis} \quad (4-39)$$

Similarly, for the inductive case, the vectors are given as

$$\mathbf{V}_o = \begin{bmatrix} \mathbf{V}_{ox} \\ \mathbf{V}_{oy} \end{bmatrix} = \begin{bmatrix} |\mathbf{V}_o| \\ 0 \end{bmatrix} \quad (4-40)$$

$$\mathbf{I}_o = \begin{bmatrix} \mathbf{I}_{ox} \\ \mathbf{I}_{oy} \end{bmatrix} = \begin{bmatrix} |\mathbf{I}_o| \cos \phi \\ -|\mathbf{I}_o| \sin \phi \end{bmatrix} \quad (4-41)$$

The voltage drop over the filter inductor is then

$$\mathbf{V}_L = \omega L \mathbf{T}_{lin} \mathbf{I}_o = \omega L \begin{bmatrix} |\mathbf{I}_o| \sin \phi \\ |\mathbf{I}_o| \cos \phi \end{bmatrix} \quad (4-42)$$

The reference for the inductive case is calculated as

$$\mathbf{V}_{si} = \mathbf{V}_o + \mathbf{V}_L = (|\mathbf{V}_o| + \omega L |\mathbf{I}_o| \sin \phi)_{x-axis} + (\omega L |\mathbf{I}_o| \cos \phi)_{y-axis} \quad (4-43)$$

The magnitude difference is calculated by dividing V_{si} with V_{sr} , which is given in Equation (4-44).

$$\mathbf{AMP} = \frac{\mathbf{V}_{si}}{\mathbf{V}_{sr}} = \left(\frac{|\mathbf{V}_o| + \omega L |\mathbf{I}_o| \sin \phi}{|\mathbf{V}_o|} \right)_{x-axis} + \left(\frac{\omega L |\mathbf{I}_o| \cos \phi}{\omega L |\mathbf{I}_o|} \right)_{y-axis} \quad (4-44)$$

For an inductive load with a lagging power factor of 0.9, the percentage voltage error that would arise by not including the effect of Equation (4-44) is plotted against peak load current, as shown in Figure 4.59. The linear relationship is clearly seen.

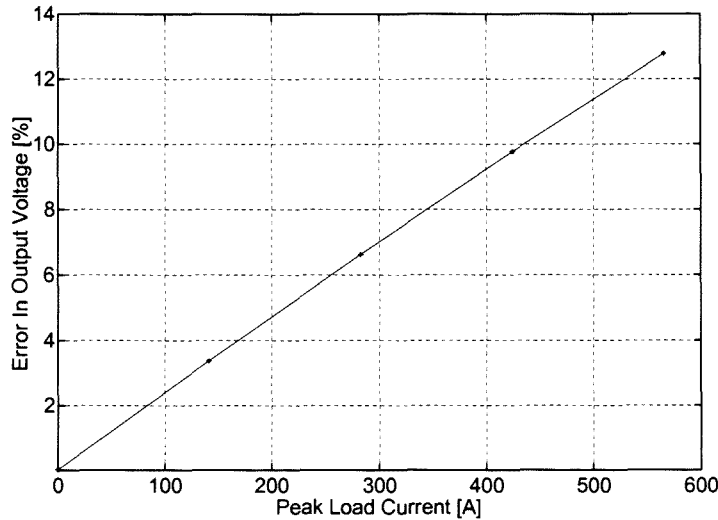


Figure 4.59: Plot of output voltage error versus peak load current

Further simulations show that by increasing the power level, the output voltage error would increase, as shown in Figure 4.60.

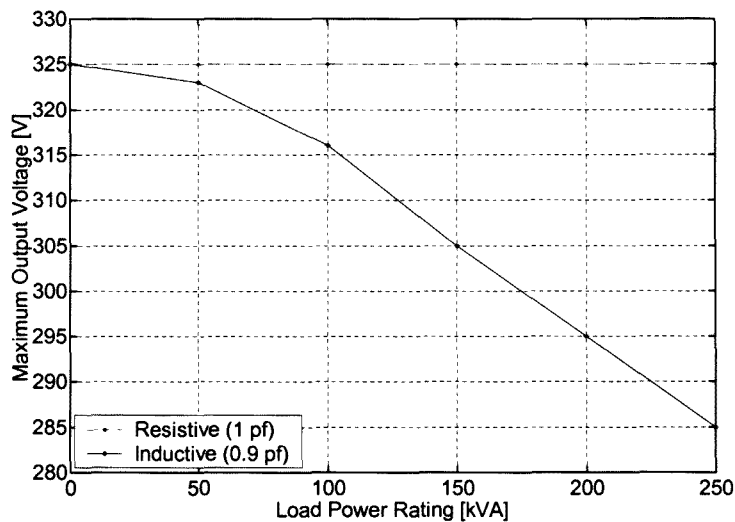


Figure 4.60: Error in output voltages due to lagging power factor

Figure 4.61 is an extension of Figure 4.60 that shows the percentage error with the inductive load. There is a linear relationship for power ratings higher than 50 kVA (a phase current of 100 A_{peak}).

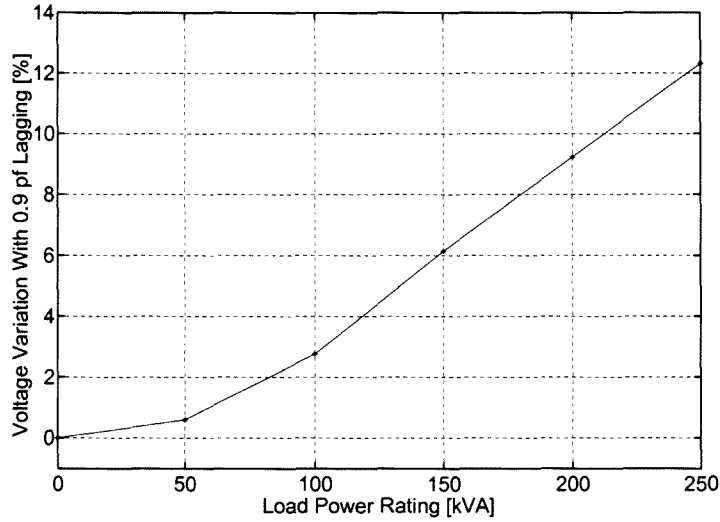


Figure 4.61: Percentage error in output voltage with inductive load

The amount that the feed-forward term has to be increased to is interpolated using a second-order polynomial. The equation is given as Equation (4-45), with the plot shown in Figure 4.62.

$$AMP = 2.225 \times 10^{-7} I_{avg}^2 - 0.0002 I_{avg} + 1.0113 \quad (4-45)$$

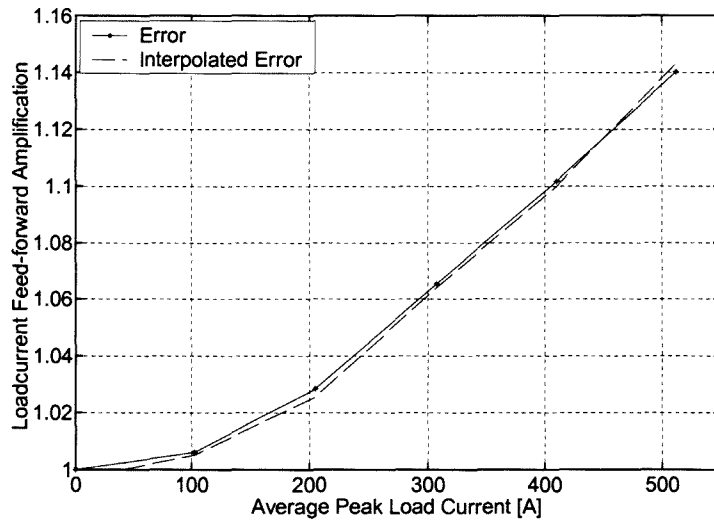


Figure 4.62: Feed-forward amplification at various load currents

In doing so, the magnitudes of the output voltages are corrected. Before the compensation was done, the magnitude was $295 V_{\text{peak}}$, and after compensation it is $320 V_{\text{peak}}$, which amounts to a 1.5% steady-state error. This is shown in Figure 4.63.

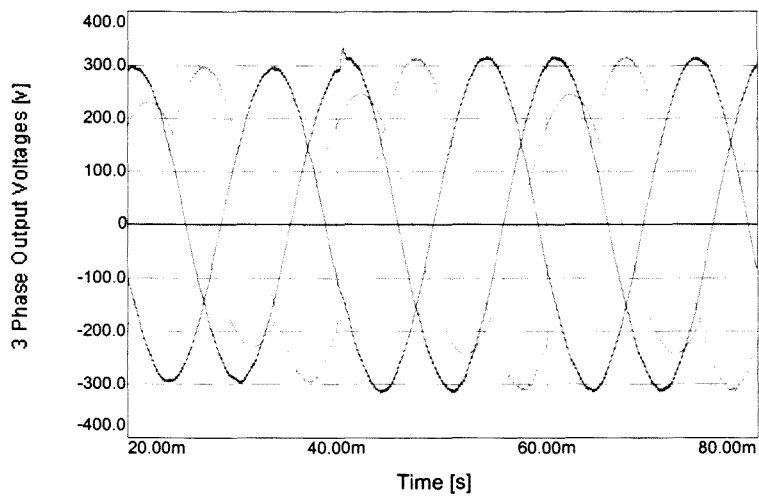


Figure 4.63: Output voltage waveforms corrected with feed-forward amplification

Figure 4.64 shows the output voltage magnitude when using the gain scheduler at various power levels.

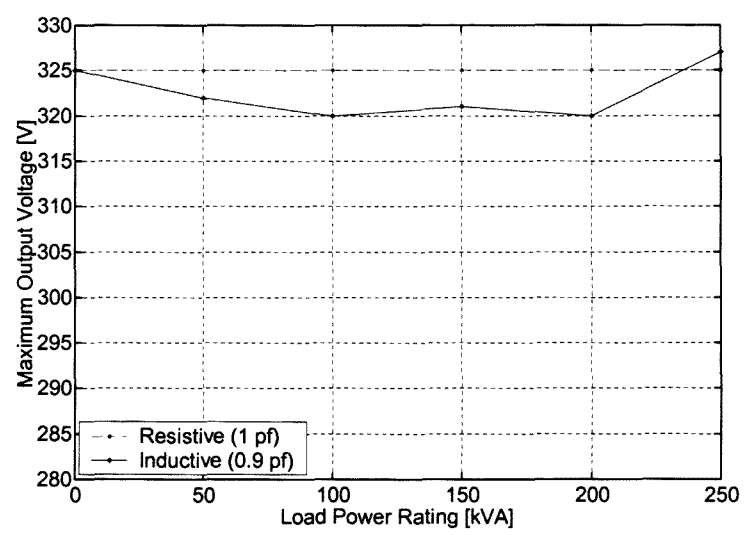


Figure 4.64: Output voltage after compensation

The output voltage error is minimized to only 2% with the use of the gain scheduler.
Figure 4.65 shows the error for various power levels.

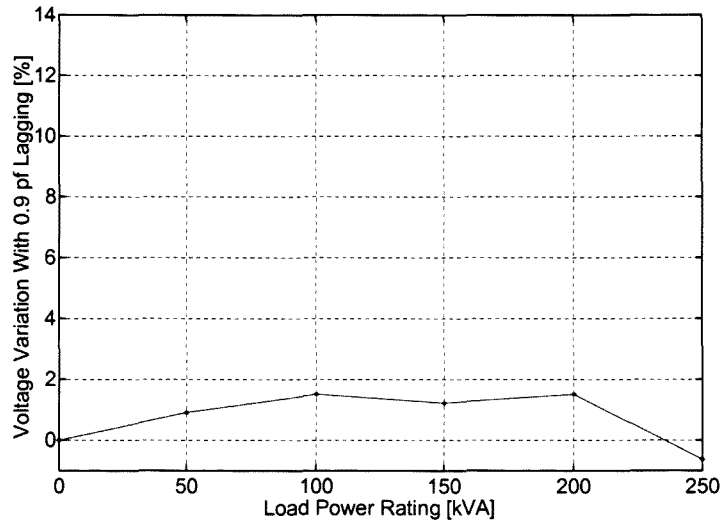


Figure 4.65: Output voltage error after compensation

4.12 Summary

The purpose of a voltage controller is to produce stable three-phase output voltages with low distortion under all loading conditions. Chapter 4 explained the design of such a three-phase, closed-loop voltage controller. A DSP is used to implement the digital closed-loop control algorithms. This, together with delays introduced by sampling the analog quantities, introduces a delay in the control law that causes system instability. The system model is updated to include the dynamics, ensuring stability. Load current feed-forward is used to compensate for changes in the load current before the output voltages become distorted, producing output voltage waveforms that are of higher quality. Simulation results show that the designed voltage controller can produce output voltage waveforms that can meet the specifications for balanced and unbalanced loads. Non-linear loads, however, produce undesirable harmonics that cause large distortion in output voltage. A summary of the steady-state error and the THD for respectively the open-loop and closed-loop controller is given in Table 4.2.

Table 4.2: Comparison between open-loop and closed-loop controllers

Load	Open-loop Controller		Closed-loop Controller	
	S-S [%]	THD [%]	S-S [%]	THD [%]
No Load	0	1.5	1.5	0.8
Balanced	-1.5	1.6	0	0.7
Unbal. (25%)	-7.7, -2.5	0.8	-2.2, -0.3	0.6
Unbal. (100%)	-8.3, 2.8	1.1	0, 3	1
Inductive	-4.6	1.8	-0.9	1
Non-Linear	-1.5	8.2	-0.6	5.5

No load:

The open-loop controller produced output voltage waveforms with a steady-state error of 0%. The closed-loop controller produced output voltage waveforms that have 1.5% steady-state error. By comparing the THD it is shown that the closed-loop controller produced voltages that have lower harmonic content than the open-loop controller.

Balanced loads:

There is a 1.5% steady-state error when using the open-loop controller. The steady-state error for the closed-loop controllers is 0%, with the THD for the closed-loop controller being lower than that of the open-loop controller.

Unbalanced loads:

All the unbalanced simulations showed that the closed-loop controller produced voltages with lower voltage variation between the three phases. The harmonics of the closed-loop controller are fewer than those of the open-loop controller, therefore a lower THD.

Inductive loads:

The closed-loop controller produced output waveforms with fewer harmonics than the open-loop controller, thus having a lower THD than the open-loop controller. The voltages produced by the closed-loop controller have a steady-state error of only 0.9% compared to the 4.6% produced by the open-loop controller.

Non-linear loads:

Both controllers produced output waveforms that have high harmonic content. The closed-loop controller however produced output voltages with much fewer harmonics than the open-loop controller, with a steady-state error of only 0.6%.

It is therefore clear that the closed-loop controller produces output voltage waveforms that are of a higher quality than the open-loop controller. Non-linear loads however produce output voltages that are not within the specifications as stipulated in [46], [47] and [48].

Chapter 5

Practical Results

5 Practical Results

5.1 Introduction

The digital controller, designed in Chapter 4, was tested on a practical system to show the functionality of the controller under various load conditions. The system consists of a three-phase, four-wire inverter supplied by a dc-bus of 750 V. The setup depicted in Figure 5.1 was used for the high-power experimental results and has the following specifications:

- Maximum output power: 250 kVA
- Output voltage: 325 V peak per phase
- Output frequency: 50 Hz
- Switching frequency: 5 kHz
- Filter inductance: 400 μH
- Filter capacitance: 200 μF

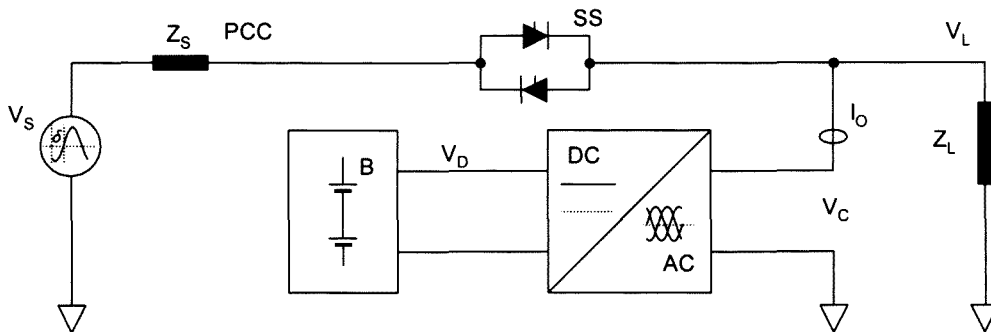


Figure 5.1: Simplified diagram of power quality compensator

Various load conditions were evaluated to make a comparison between an existing open-loop controller versus the closed-loop controller in order to prove that it is possible to design a stable, robust closed-loop controller for the system discussed.

The results will be presented as follows:

- The measured outputs will include a figure showing the output voltages in the time domain.
- The magnitudes of the three separate phases will be measured and compared to the 230 V_{rms} (325 V_{peak}), 50 Hz reference voltage.
- An FFT will be given to show the magnitudes of the various frequency components and to calculate the THD.

In order to evaluate the controller under extreme circumstances, the following load conditions were used for the experiments:

- No load.
- Balanced loads.
- Unbalanced loads (25%).
- Unbalanced loads (100%).
- Inductive loads.
- Non-linear loads, being a rectifier with an LC dc-link filter.

5.2 Practical Results

5.2.1 No load

Under no load the open-loop controller produced output voltage waveforms as shown in Figure 5.2. The magnitudes of the phases are equal to 232 V_{rms} (328 V_{peak}), which amounts to a 1% steady-state error.

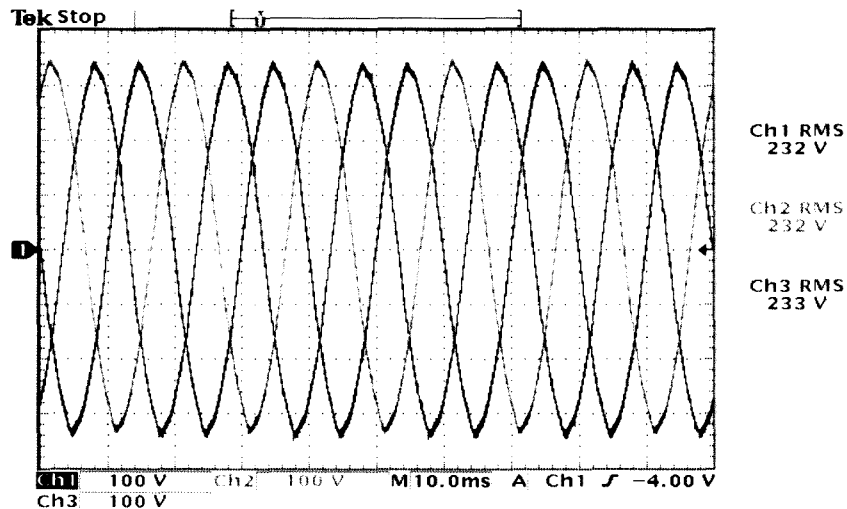


Figure 5.2: Balanced three-phase, 0 W load (Open-loop controlled)

The FFT is shown in Figure 5.3, with the THD calculated as 2.3%.

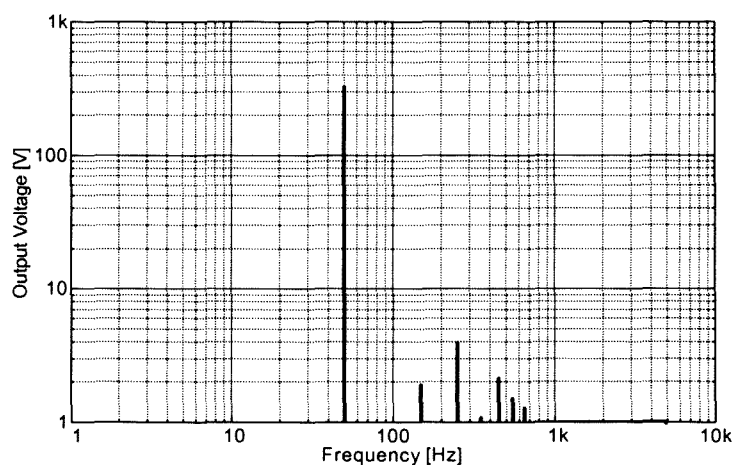


Figure 5.3: FFT, Balanced three-phase, 0 W load (Open-loop controlled)

The closed-loop controller produced output voltage waveforms as shown in Figure 5.4. Phases A and C are equal to $223 V_{\text{rms}}$ ($315 V_{\text{peak}}$), which amounts to a 3% steady-state error. Phase B has a magnitude equal to $226 V_{\text{rms}}$ ($320 V_{\text{peak}}$), which amounts to a 1.7% steady-state error.

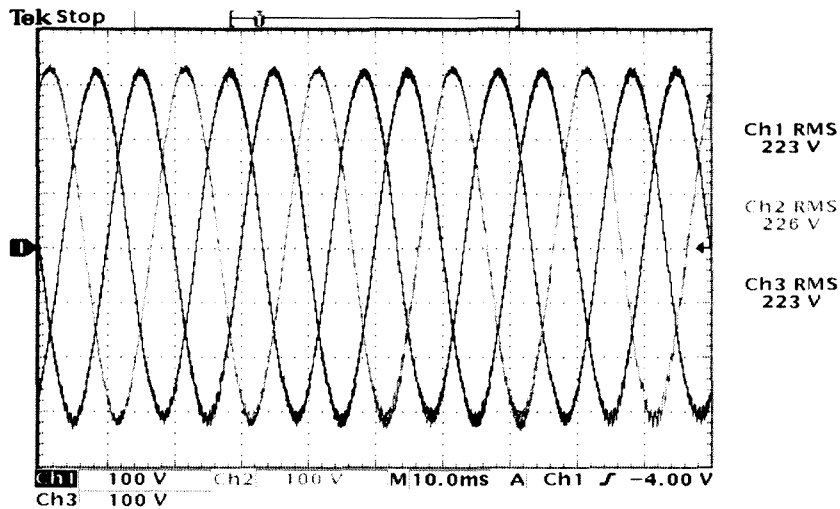


Figure 5.4: Balanced three-phase, 0 W load (Closed-loop controlled)

The FFT is shown in Figure 5.5. The THD is calculated as 1.8%.

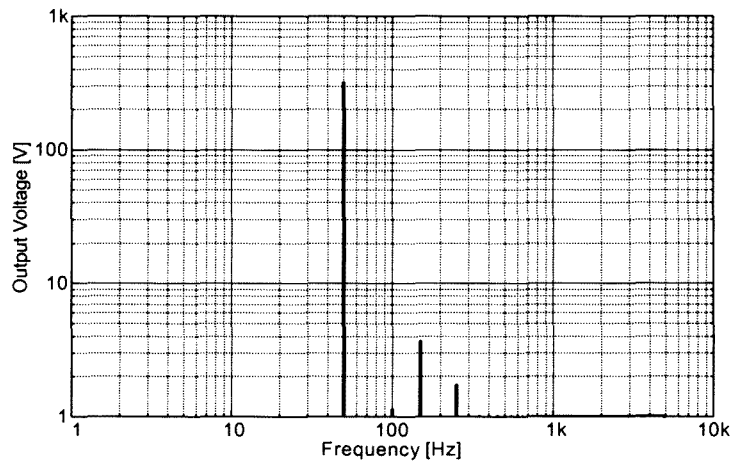


Figure 5.5: Balanced three-phase, 0 W load (Closed-loop controlled)

5.2.2 Balanced Loads

A three-phase, balanced, 250 kW, resistive load was used to evaluate the ability of the controller under balanced conditions. The open-loop controller produced output voltage waveforms that are of equal magnitude, being 224 V_{rms} (316 V_{peak}), which amounts to a 2.8% steady-state error.

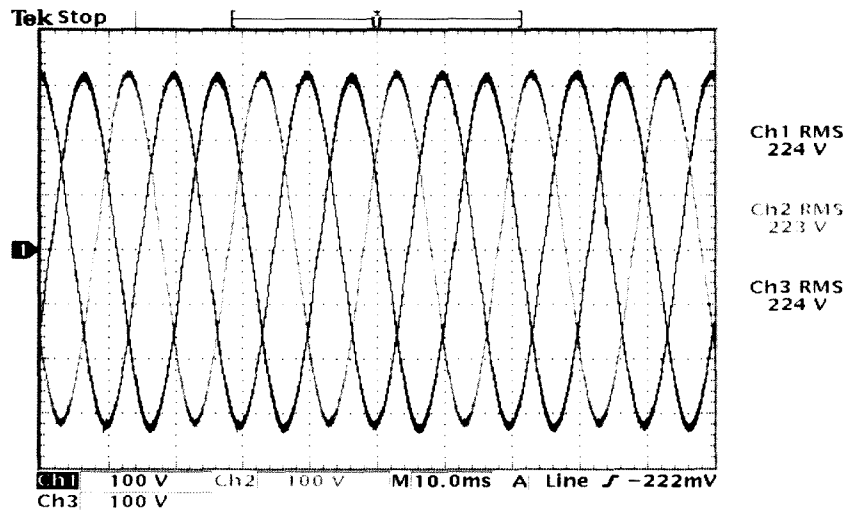


Figure 5.6: Balanced three-phase, 250 kW load (Open-loop controlled)

The FFT, shown in Figure 5.7, is used to calculate the THD as 2.2%.

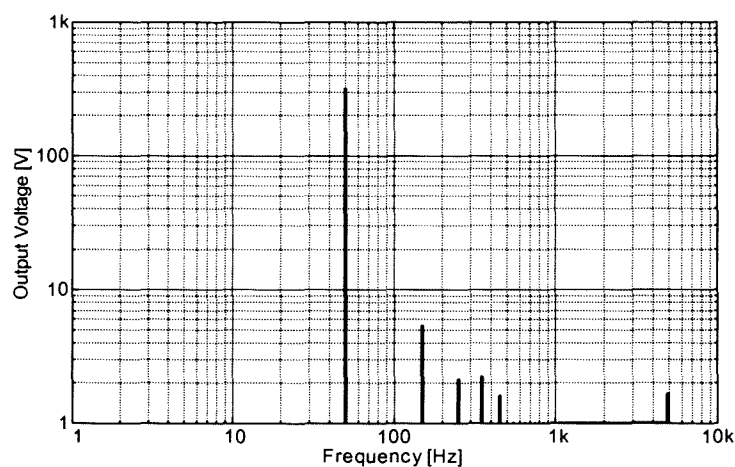


Figure 5.7: FFT, Balanced three-phase, 250 kW load (Open-loop controlled)

The closed-loop controller produced outputs that are all equal in magnitude, being 222 V_{rms} (314 V_{peak}), which amounts to a 3.4% steady-state error. This is shown in Figure 5.8.

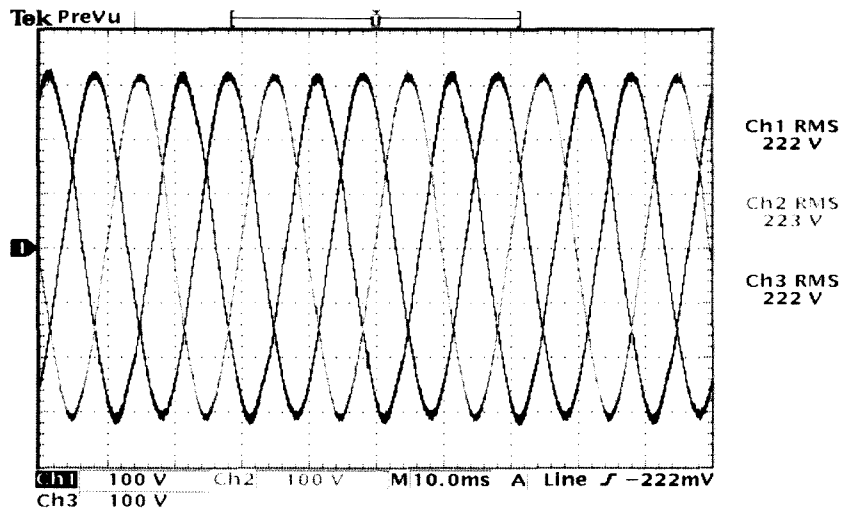


Figure 5.8: Balanced three-phase, 250 kW load (Closed-loop controlled)

The FFT, shown in Figure 5.9, is used to calculate the THD as 2.8%.

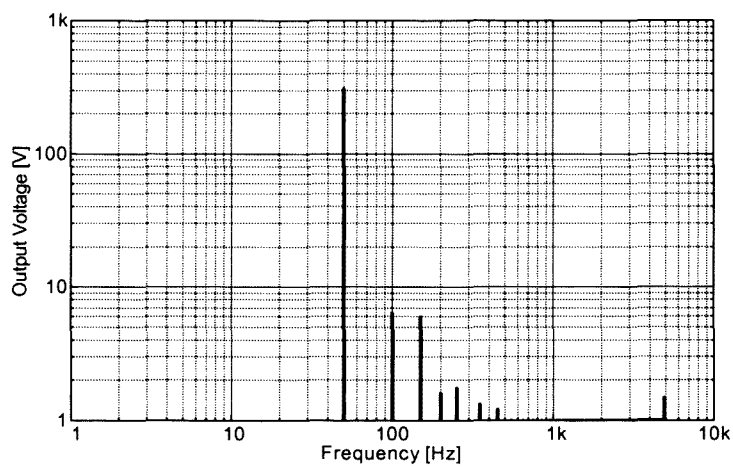


Figure 5.9: FFT, Balanced three-phase, 250 kW load (Closed-loop controlled)

5.2.3 Unbalanced Loads

5.2.3.1 Unbalance of 25%

An unbalance of 25% would induce a neutral current with a peak magnitude of 150 A. The open-loop controller produced output voltages as shown in Figure 5.10. The magnitudes for phases A through C are 214 V_{rms} (302 V_{peak}), 224 V_{rms} (317 V_{peak}) and 227 V_{rms} (321 V_{peak}), respectively. This amounts to respectively a 7%, 2.6% and 1.3% steady-state error.

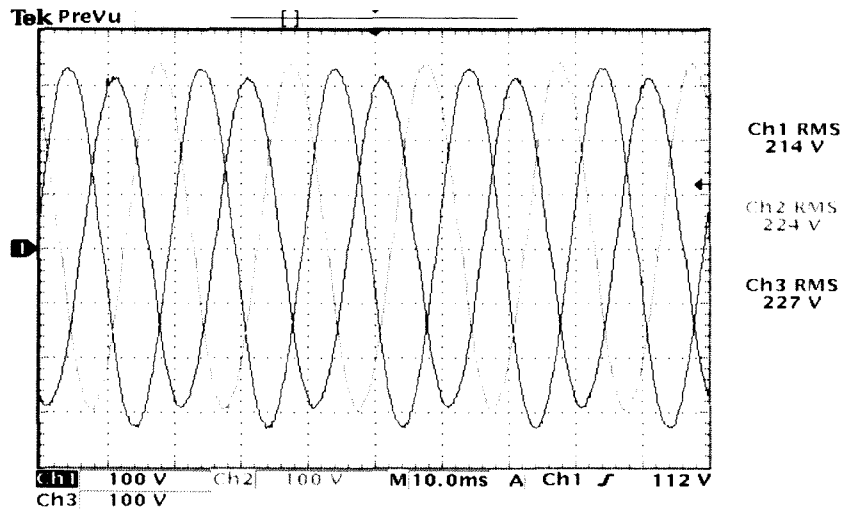


Figure 5.10: Unbalanced (25%), 100 kW load (Open-loop controlled)

The FFT is shown in Figure 5.11. The THD is calculated as 2%.

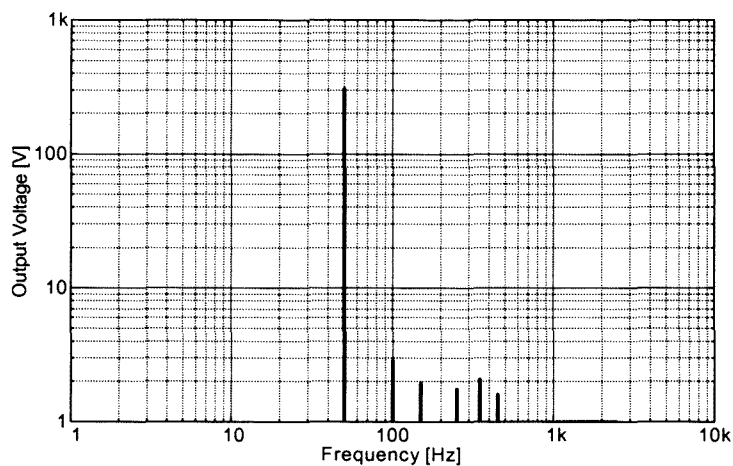


Figure 5.11: FFT, Unbalanced (25%), 100 kW load (Open-loop controlled)

The closed-loop controller gives output voltages as given in Figure 5.12. The magnitudes of the three phases are respectively 219 V_{rms} (310 V_{peak}), 224 V_{rms} (317 V_{peak}) and 224 V_{rms} (317 V_{peak}). This amounts to respectively 4.6% and 2.5% steady-state error.

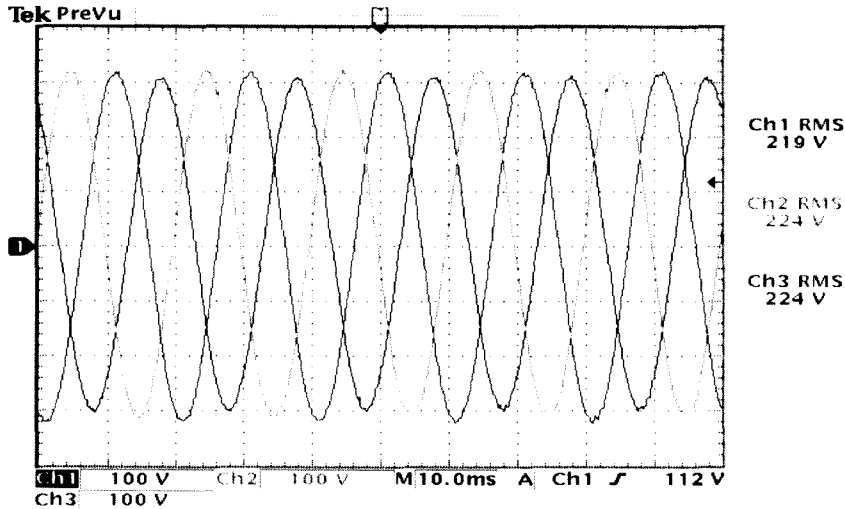


Figure 5.12: Unbalanced (25%), 100 kW load (Closed-loop controlled)

The FFT is shown in Figure 5.13. The THD is calculated as 1.6%.

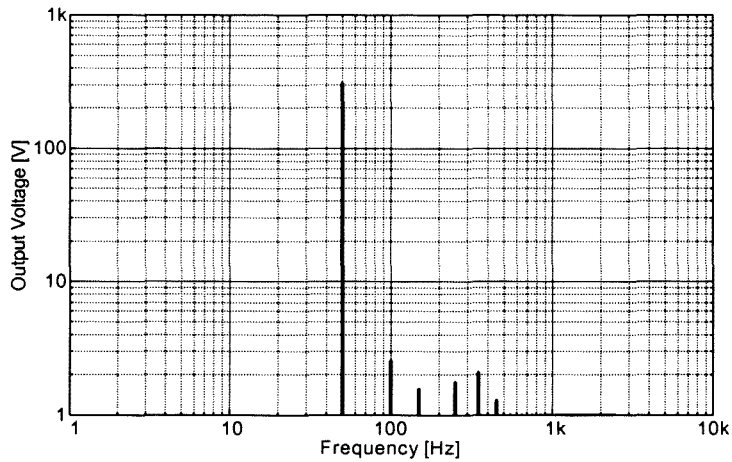


Figure 5.13: FFT, Unbalanced (25%), 100 kW load (Closed-loop controlled)

5.2.3.2 Unbalance of 100%

A single-phase load, with a power rating of 65 kW was connected to the three-phase system. The three output voltages are shown in Figure 5.14. The magnitude of phase A equals 190 V_{rms} (269 V_{peak}), phase B equals 223 V_{rms} (315 V_{peak}) and phase C equals 247 V_{rms} (349 V_{peak}). These amount to steady-state errors of respectively 17.3%, 3% and 7.5%.

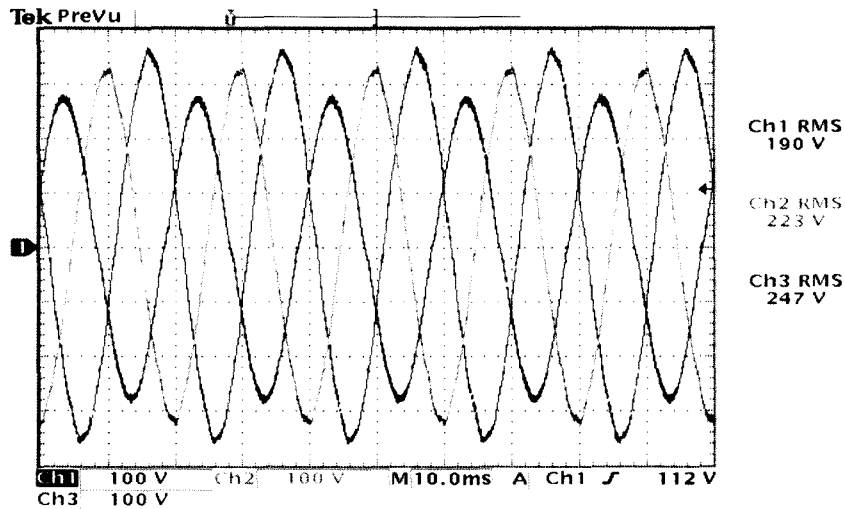


Figure 5.14: Unbalanced (100%), 65 kW load (Open-loop controlled)

The FFT is shown in Figure 5.15. The THD is calculated as 3.7%.

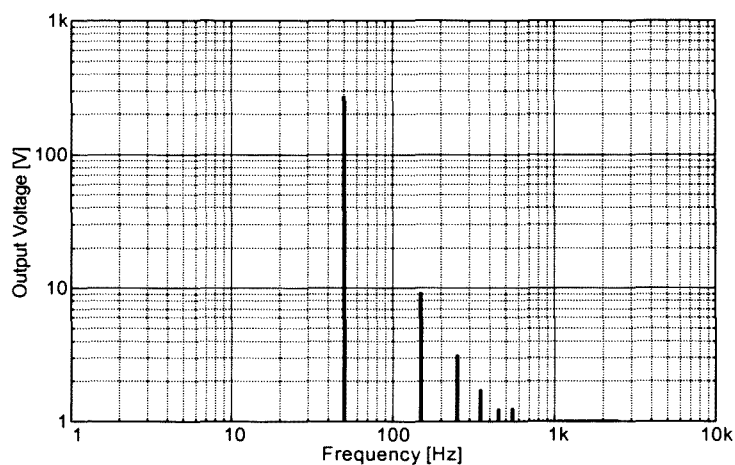


Figure 5.15: FFT, Unbalanced (100%), 65 kW load (Open-loop controlled)

The closed-loop controller produced output voltage waveforms as shown in Figure 5.16. The magnitudes of the three phases equal 200 V_{rms} (283 V_{peak}) for phase A, 224 V_{rms} (317 V_{peak}) for phase B and 227 V_{rms} (321 V_{peak}) for phase C. These amount to respectively a 13%, 2.5% and 1.2% steady-state error.

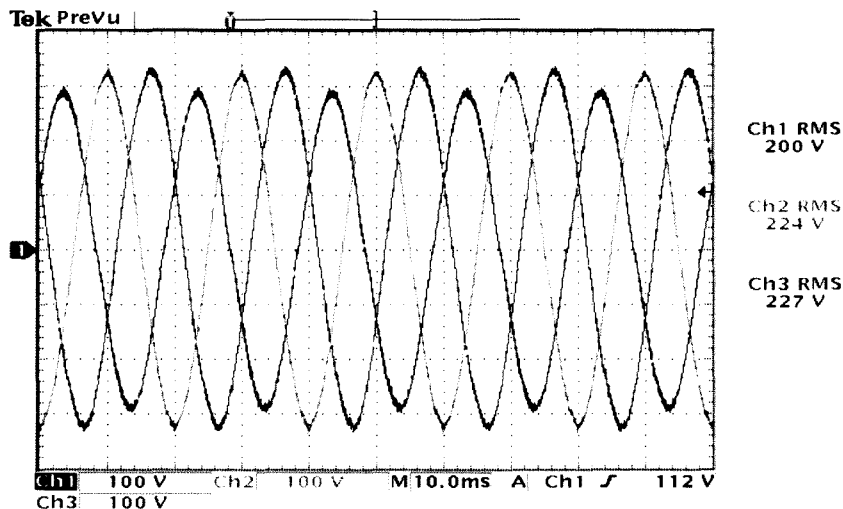


Figure 5.16: Unbalanced (100%), 65 kW load (Closed-loop controlled)

The FFT is shown in Figure 5.17. The THD is calculated as 2.6%.

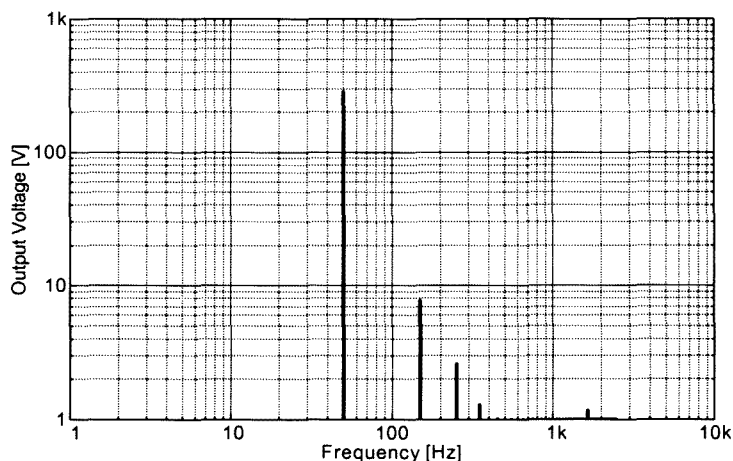


Figure 5.17: FFT, Unbalanced (100%), 65 kW load (Closed-loop controlled)

5.2.4 Loads with a lagging power factor

An inductive load with a power factor of 0.9 was used to evaluate the controllers for inductive loads. The open-loop controller produced output voltage waveforms as shown in Figure 5.18. The magnitude for phase A equals 221 V_{rms} (315 V_{peak}), phase B equals 220 V_{rms} (315 V_{peak}) and phase C equals 222 V_{rms} (315 V_{peak}). These amount to respectively a 3.9%, 4.3% and 3.5% steady-state error.

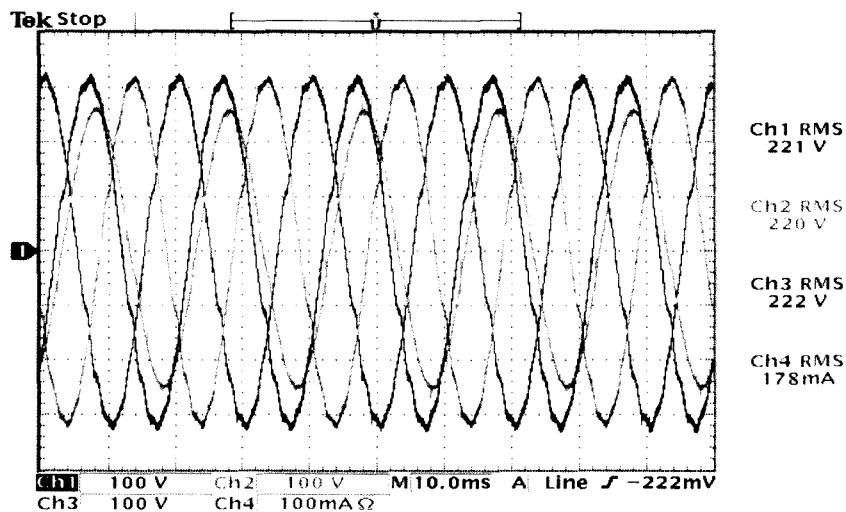


Figure 5.18: Inductive load, 150 kW, pf 0.9 (Open-loop controlled)

The FFT is shown in Figure 5.19. The THD is calculated as 3.2%.

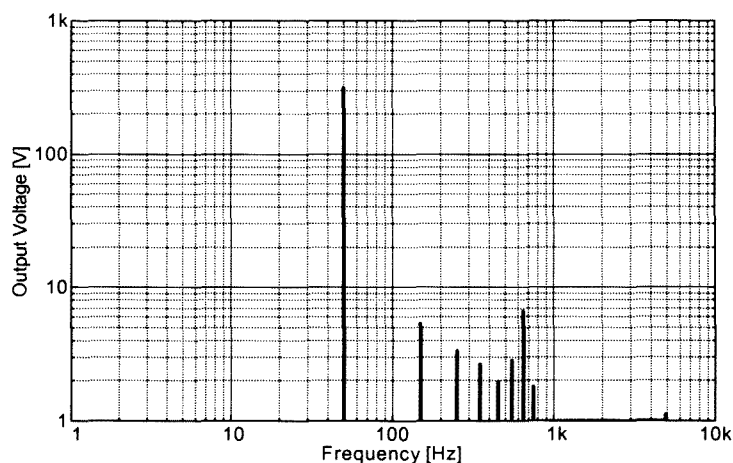


Figure 5.19: FFT, Inductive load, 150 kW, pf 0.9 (Open-loop controlled)

The closed-loop controller produced output voltage waveforms as shown in Figure 5.20. The magnitudes for phases A and B equal $217 \text{ V}_{\text{rms}}$ ($310 \text{ V}_{\text{peak}}$) and phase C equals $218 \text{ V}_{\text{rms}}$ ($310 \text{ V}_{\text{peak}}$). These amount to respectively a 5.6% and 5.2% steady-state error.

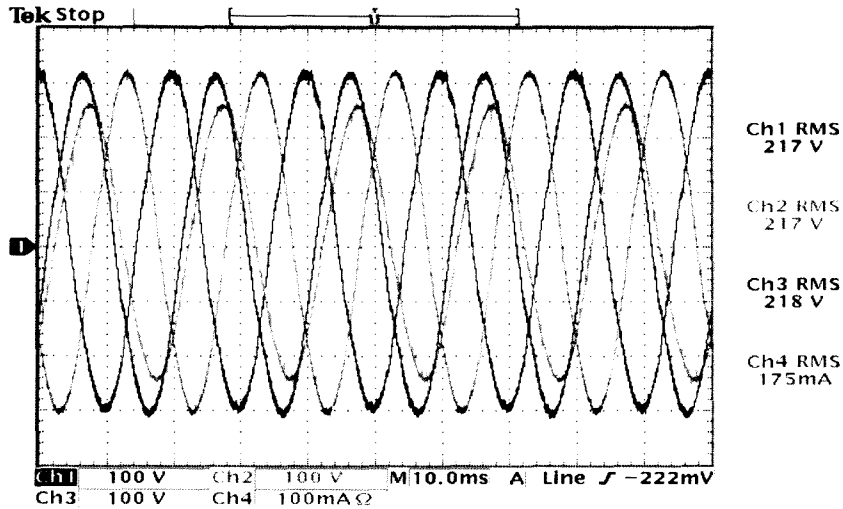


Figure 5.20: Inductive load, 150 kW, pf 0.9 (Closed-loop controlled)

The FFT is shown in Figure 5.19. The THD is calculated as 2.7%.

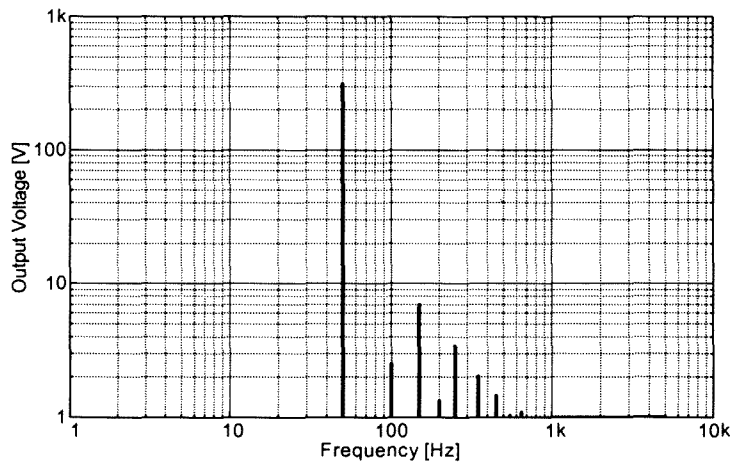


Figure 5.21: FFT, Inductive load, 150 kW, pf 0.9 (Closed-loop controlled)

5.2.5 Non-Linear Loads

A three-phase diode rectifier with an L/C dc-link filter, with a power rating of 45 kW, was used as a non-linear load. The dc capacitance is 3.3 mF, the inductance is 1.2 mH and the resistive load is 7.7 Ω , producing a load current that has a crest factor of 1.6. The output voltage waveforms produced by the utility is shown in Figure 5.22. The magnitude for phase A equals 225 V_{rms} (305 V_{peak}) and phases B and C equal 225 V_{rms} (315 V_{peak}). This amounts to a 2.2% steady-state error. The slight unbalance in the phase voltages is due to an unbalance in the resistive part of the load. Phase A current, shown as the green trace, has a magnitude of 55.2 A_{rms} (88 A_{peak}).

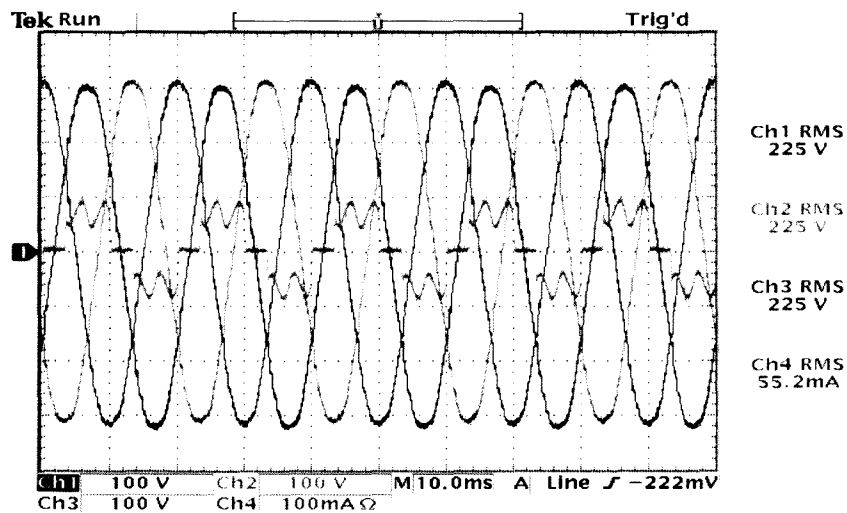


Figure 5.22: Utility waveforms for a three-phase rectifier load, 45 kW

The open-loop controller produced output waveforms as shown in Figure 5.23, with each phase equalling $222 \text{ V}_{\text{rms}}$ ($340 \text{ V}_{\text{peak}}$). This amounts to a 4.6% steady-state error.

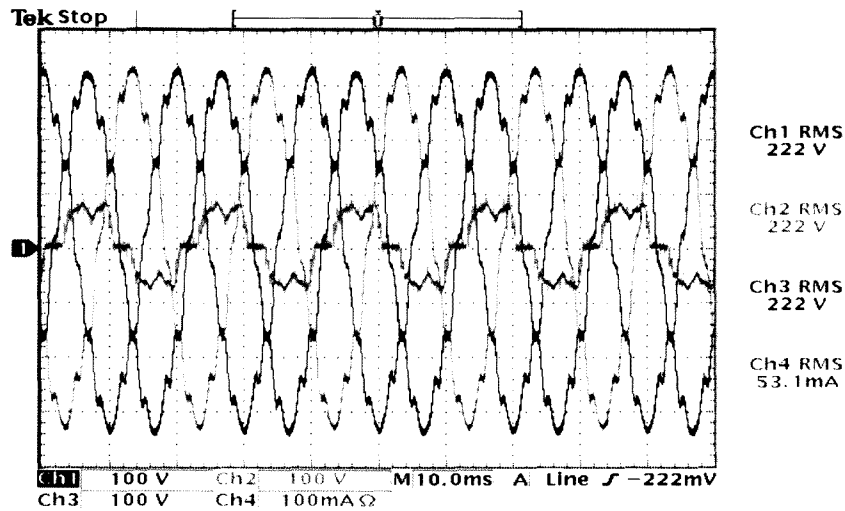


Figure 5.23: Three-phase rectifier load, 45 kW (Open-loop controlled)

The FFT is shown in Figure 5.24. The THD is calculated as 8.8%.

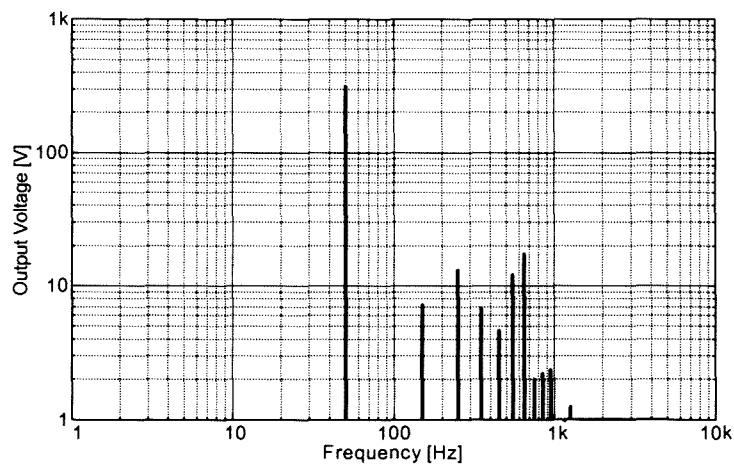


Figure 5.24: FFT, Three-phase rectifier load, 45 kW (Open-loop controlled)

The closed-loop controller produced output waveforms as shown in Figure 5.25. The magnitude for phase A equals $212 V_{rms}$ ($320 V_{peak}$), phase B equals $213 V_{rms}$ ($325 V_{peak}$) and phase C equals $211 V_{rms}$ ($325 V_{peak}$). These amount to respectively a 7.8%, 7.4% and 8.2% steady-state error.

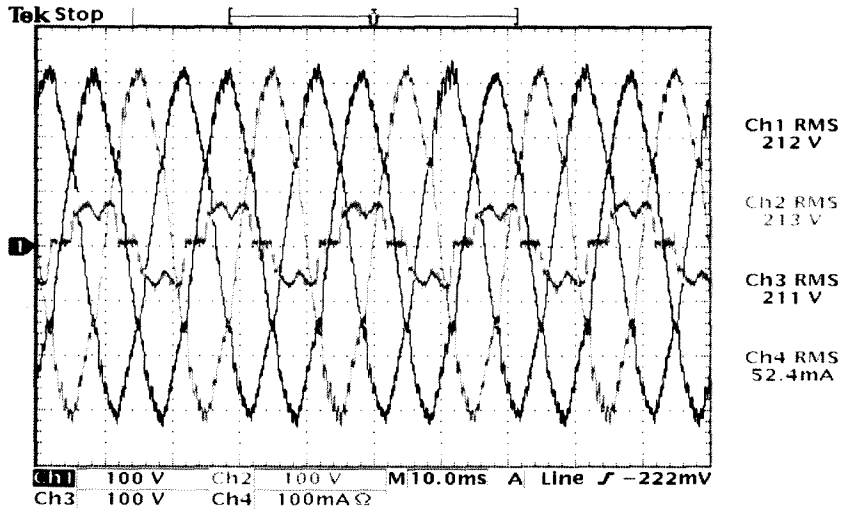


Figure 5.25: Three-phase rectifier load, 45 kW (Closed-loop controlled)

The FFT is shown in Figure 5.26. The THD is calculated as 6.3%.

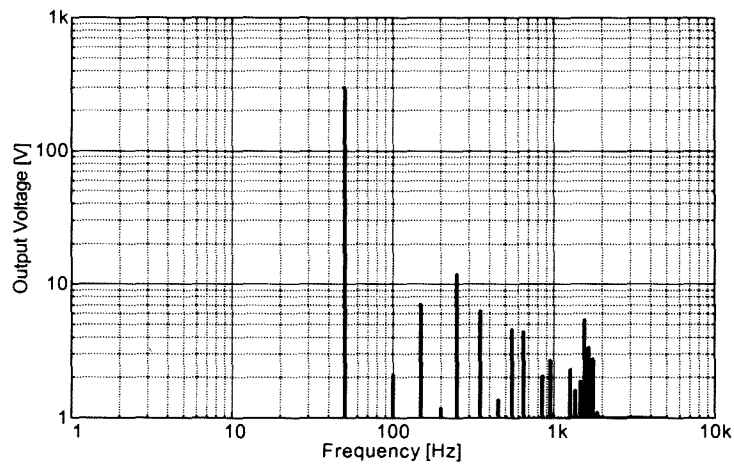


Figure 5.26: FFT, Three-phase rectifier load, 45 kW (Closed-loop controlled)

5.3 Summary

This chapter presented output voltage waveforms produced by a closed-loop, deadbeat controller. Auto-tuning of the load current feed-forward is used to compensate for changes in the load conditions. This produces output voltage waveforms that have smaller steady-state error and are of higher quality. Practical results show that the designed voltage controller can produce output voltage waveforms that can meet the specifications for balanced and unbalanced loads. Non-linear loads, however, produce undesirable harmonics that cause large distortion in the output voltages, but are still within allowable levels when the output power is at lower levels. A summary of the steady-state error and the THD for respectively the open-loop and closed-loop controller is given in Table 5.1.

Table 5.1: Comparison between open-loop and closed-loop controllers

Load	Open-loop Controller		Closed-loop Controller	
	S-S [%]	THD [%]	S-S [%]	THD [%]
No Load	1	2.3	-3, -1.7	1.8
Balanced	-2.8	2.2	-3.4	2.8
Unbal. (25%)	-7, -1.3	2	-4.6, -2.5	1.57
Unbal. (100%)	-17.3, 7.5	3.7	-13, -1.2	2.6
Inductive	-4.3, -3.5	3.2	-5.6, -5.2	2.7
Non-Linear	4.6	8.8	-8.2, -7.4	6.3

No load:

The open-loop controller produced output voltage waveforms with a steady-state error of 1%, while the closed-loop controller produced output voltage waveforms that have 1.5% steady-state error. Comparing the THD shows that the closed-loop controller produced voltages that have lower harmonic content than the open-loop controller.

Balanced loads:

There is a 2.8% steady-state error when using the open-loop controller. The steady-state error for the closed-loop controllers is 3.4%, with the THD for the closed-loop controller being lower than that of the open-loop controller.

Unbalanced loads:

All the unbalanced results showed that the closed-loop controller produced voltages with lower voltage variation between the three phases. In both cases the closed-loop controller produced output voltage waveforms with a lower THD.

Inductive loads:

The closed-loop controller produced output waveforms with lower harmonic content than the open-loop controller, thus having a lower THD than the open-loop controller. The voltages produced by the closed-loop controller have a steady-state error of 5.6% compared to the 4.3% of those produced by the open-loop controller.

Non-linear loads:

Both controllers produced output waveforms that have high harmonic content. The closed-loop controller however produced output voltages with much fewer harmonics than the open-loop controller, with a steady-state error of only 8.2%.

From the results it is seen that the closed-loop controller produces output voltage waveforms that are of a higher quality than the open-loop controller. Output voltage waveforms when low harmonic loads are connected are within the specifications stipulated in [46], [47] and [48].

Chapter 6

Conclusions and Recommendations

6 Conclusions and recommendations

6.1 Inverter topology selection and modelling

Unbalanced and non-linear load conditions are widespread in a power supply utility. Three-phase, three-wire inverters are commonly used, but are unable to produce three independent voltages, and can therefore not be used for supplying power to zero-sequence unbalanced loads. A four-wire configuration, implementing a fourth leg to handle neutral currents that flow when unbalanced loads are connected, is effective in controlling the three-phase output voltages. The four-wire configuration is converted to the $\alpha\beta 0$ -plane to produce three independent, single-phase circuits. Separate single-phase controllers, all with the same circuit parameters, are used to control the four legs of the inverter, producing three balanced output voltage waveforms.

6.2 Control system design

High-speed, digital controllers are popular for controlling high-power inverters. These controllers introduce time delays in the controlled variables, and produce unstable situations due to calculation delays. Control techniques are developed implementing open-loop and closed-loop controllers. Open-loop controllers normally produce low-quality system outputs. System instability occurs when closed-loop controllers are designed without taking the time delays into consideration. This thesis presented the design of such a closed-loop controller implementing classical control and modern control techniques. The classical controller used Pade approximations to model the time delay, whereas the modern controller used model augmentation to include the introduced time delay. Deadbeat control is used, with the controller gains shifting the system poles to the origin of the z-plane to ensure fast control of all the system variables. A feed-forward control scheme helps in producing higher-quality waveforms that compensates for the disturbance caused by the load current. A gain scheduler compensates for variations in load conditions by implementing an auto-tuning algorithm. Thus, a stable closed-loop controller was developed.

6.3 Evaluation of the control system

High control-loop bandwidth ensures good tracking, disturbance rejection and robustness. However, at high power levels, the control bandwidth is limited by the low switching frequency, selected due to the overpowering switching losses, which vary linearly with the switching frequency. Further limitations include the dead time needed for switches to commutate and the calculation delay introduced by digital signal processors.

Practical results are shown in Table 6.1.

Table 6.1: Controller performance under various load conditions

Load	Open-loop Controller		Closed-loop Controller	
	S-S [%]	THD [%]	S-S [%]	THD [%]
No Load	1	2.3	-3, -1.7	1.8
Balanced	-2.8	2.2	-3.4	2.8
Unbal. (25%)	-7, -1.3	2	-4.6, -2.5	1.57
Unbal. (100%)	-17.3, 7.5	3.7	-13, -1.2	2.6
Inductive	-4.3, -3.5	3.2	-5.6, -5.2	2.7
Non-Linear	4.6	8.8	-8.2, -7.4	6.3

The open-loop controller and the closed-loop controller produced output voltage waveforms that have a THD lower than the specification of 8% for balanced and unbalanced loads. The closed-loop controller, however, produced output voltage waveforms that have lower harmonic content than the open-loop controller. Load unbalance introduced high variations in phase voltage magnitudes, with a maximum of 24.8% variation when open-loop controlling a single-phase load. The closed-loop controller, however, produced output voltage waveforms that vary only 11.8% for a single-phase load. Non-linear loads, however, produced undesirable harmonics that cause large distortion in output voltage.

6.4 Recommendations and future work

The deviation in measured results and simulated results is due to the limitation set by the controller hardware. The current DSP is running at 33 MHz. Increasing the DSP clock frequency would decrease calculation delays and would therefore shorten the time delay. Therefore, the output voltage waveforms would improve if the clock frequency could be made higher. A further improvement can be made to the measurement system by increasing the cutoff frequency, thus increasing the bandwidth of the system. By doing this, higher-order voltage harmonics could be compensated for, improving good tracking, disturbance rejection and robustness.

The steady-state error produced by the closed-loop controller is due to the voltage drop over the equivalent series resistance of the filter inductor. The system model was developed without including any parasitic components, hence the small variation in output voltage magnitude. The contactors used for isolating the UPS from the power supply utility introduce a further voltage drop. Thus, to get a more realistic model, the system model should be updated to include these parasitic components, thereby ensuring output voltage waveforms with 0% steady-state error.

In order to have high performance under non-linear load conditions, a gain scheduler with higher precision should be developed. The system will be more robust, rejecting measurement noise that would cause incorrect control efforts. A further solution could be to connect a low-power inverter in parallel with the main inverter. This inverter would only supply the harmonic currents demanded by the load and the load would see a linear load, producing higher-quality output voltage waveforms.

6.5 Summary

This thesis showed that it is possible to design a closed-loop, digital controller, and that by augmenting the system model with the time delay, a stable controller is ensured. Practical results showed satisfactory response for various load conditions.

Chapter 7

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Appendix A

MATLAB[®] Code for a Modern Controller

A MATLAB[®] Code for a Modern Controller

```

% ----- %
% A CONTROLLER FOR A 3PHASE INVERTER WITH AN OUTPUT LC FILTER IS
% DESIGNED USING DEADBEAT CONTROL. DEADBEAT CONTROL IS USED TO MAKE
% THE ERROR EQUAL TO ZERO IN AS SHORT AS POSSIBLE TIME (EG. ONE
% TIMESTEP). LINEAR FEEDBACK,  $u = -Kx$ , IS USED IN THE COMPENSATOR.
% ----- %

close all;
clc;

% -----
% System Parameters
% -----

Lf = 400e-6; % Filter Inductor
Cf = 200e-6; % Filter Capacitor
Vs = 750; % dc-bus
Vm = 325; % Peak Of Output Voltage
fs = 5000; % Switching Frequency
Ts = 1/fs; % Switching Period
R = 0.63; % Nominal Load
y = 0.9; % Percentage/100 Calculation Time
m = y; % Percentage/100 Calculation Time

% -----
% System Matrices
% -----

%  $\dot{x} = A.x + B.u + B_i.I_l$ 
%  $y = C.x + D.u$ 

% --> When no load is connected, the system equation will be
%  $\dot{x} = A.x + B.u$ 

% These are the continuous time matrices
A = [0 1/Cf ; -1/Lf 0];
B = [0 ; 1/Lf];
Bi = [-1/Cf ; 0];
C = [1 0];
D = [0];

U = [1 0 ; 0 1]; % Unity Matrix

% -----
% Discretization
% -----

% Discrete system matrices are calculated using Equation (2-52)
Phi = expm(A*Ts); % Phi
FphiTs = expm(A*m*Ts); % Phi @ time = (mT)
FphiTmTs = expm(A*(Ts-m*Ts)); % Phi @ time = (T - mT)
FGammamTs = (1/(m*Ts))*(FphiTs-eye(2))*inv(A); % Gamma @ time = (mT)
FGammaTmTs = (1/(Ts-m*Ts))*(FphiTmTs-eye(2))*inv(A); % "
Gammal = m*Ts*FphiTmTs*FGammamTs*B; % Gamma including time delay

```

```

Gamma2      = (Ts-m*Ts)*FGammaTmTs*B;      % Gamma including time delay
Gamma       = Gamma1 + Gamma2;              % Gamma with no time delay
GammaI      = inv(A)*(Phi - U)*Bi;          % Gamma for current

% ----- %
% THE DESIGN IS DONE IN A FEW STEPS.  THE FIRST STEP IS TO DESIGN A
% CONTROLLER FOR A SYSTEM WITH NO LOAD CONNECTED.  THE SECOND STEP WILL
% INCLUDE THE TIME DELAY INTRODUCED BY THE CALCULATION TIME.  STEP 3
% WILL INCLUDE COMPENSATION FOR AN UNKNOWN LOAD.
% ----- %

% -----
% Step 1 - No Load
% -----

% Determine K-vector

sysc        = ss(A,B,C,D);
sysd        = c2d(sysc,Ts);
[Phi,Gamma,H,J] = ssdata(sysd);
sysopen     = tf(sysd);

KStep1 = acker(Phi,Gamma, [0 0]); % DB Control - poles at z = [0,0]

% Determine Reference Input Constant : For the control, u = -Kx, no
% reference input is necessary.  The transient response of the pole-
% placement design is affected by the reference input.  The control is
% now, u = -Kx + r.  A vector, N, will be calculated to create a
% nonzero steady-state error. %

NVec1 = inv([Phi-eye(2), Gamma ; H J])*[0;0;1];
Nx1    = NVec1(1:2,1);
Nul    = NVec1(3,1);
N1     = Nul + (KStep1*Nx1);

Ac     = A - Gamma*KStep1;

% Discrete transfer function of closed-loop system
[num1,den1] = ss2tf(Ac,N1*Gamma,[1 0],0);

% In discrete form, therefore this is z tf!
s1      = tf(num1,den1,1/5000);

% -----
% Step 2 - Calculation Delay
% -----

% The time delay has a big effect on the output voltage.  The delay
% will now be included in the system equations to compensated for it.

% New system equation, including time delay -- zdot = Phie.z + B.u
% (Error)

Phidel    = [Phi Gamma1 ; 0 0 0];
Gammadel  = [Gamma2 ; 1];
Hdel      = [H 0];
Jdel      = 0;
syscalcopen = tf(sysd);

```



```

syscalc      = ss(Phidel,Gammadel,Hdel,Jdel,Ts);
syscalcopen = tf(syscalc);

% Determine K-vector
Con = [Gammadel Phidel*Gammadel (Phidel)^2*Gammadel];

% Controllability Matrix
K    = [0 0 1]*inv(Con)*((Phidel)^3);

% Determine Reference Input constant
NuNx = inv([Phidel-eye(3), Gammadel ; Hdel Jdel])*[0;0;0;1];
Nu    = NuNx(4);
Nx    = NuNx(1:3);
N2    = Nu + (K*Nx);

% Closed Loop matrices
Phic  = Phidel - Gammadel*K;
Gammac = Gammadel*Nu + Gammadel*K*Nx;
Hc    = Hdel;
Jc    = 0;

sysclosed   = ss(Phic,Gammac,Hc,Jc,Ts);
sysclosedtf = tf(sysclosed);

% -----
% Step 3 - Unknown Load
% -----

% Now that the new K-vector is calculated, we have a closed loop
controller. The error that arises from connecting an unknown load
and drawing an unknow current, is compensated for by using Feed-
forward control

% Note : Calculating F by first simplifying with N-vector, gives the
equations as used here.
FF1 = (GammaI(1,1) - Gammadel(1,1)*K(1,2))/Gammadel(1,1);
FF2 = (GammaI(2,1) - Gammadel(2,1)*K(1,2))/Gammadel(2,1);
FF3 = (0 - Gammadel(3,1)*K(1,2))/Gammadel(3,1);

% -----
% Reference Functions
% -----

% For NO-LOAD, this is the reference!
q    = exp(j*2*pi*50*(1/fs));

a11 = Phi(1,1);
a12 = Phi(1,2);
a21 = Phi(2,1); a22 = Phi(2,2);
b11 = Gamma(1,1);
b21 = Gamma(2,1);

VrefXNL = ((q^2 - q*a22 - q*a11 + a11*a22 - a12*a21)/(q*b11 - b11*a22
+ a12*b21));
IrefXNL = ((q*b21 - a11*b21 + a21*b11)/(q*b11 - b11*a22 + a12*b21));

```

Appendix B

C++[®] Code for a Modern Controller

B C++[®] Code for a Modern Controller

```
/* Closed Loop variables */
```

```
extern double ukkAm1;  
extern double ukkBm1;  
extern double ukkZm1;
```

```
extern double tuA;  
extern double tuB;  
extern double tuC;  
extern double minduty;  
extern double maxduty;  
extern double zs;
```

```
extern double IAV;  
extern double k1;  
extern double k2;  
extern double k3;  
extern double LFF;  
extern double Loadamp;  
extern double PeakAvgCurrent;
```

```
/* */
```

```
static inline void CalcUPSref()
```

```
{  
  double rVa, rVb, rVc;  
  double VAref, VBref;  
  double VArefk, VBrefk;  
  double Valpha, Vbeta, Vzero, Ialpha, Ibeta, Izero, dukkA, dukkB, dukkZ;  
  double Iloadalpha, Iloadbeta, Iloadzero;  
  double ukkA, ukkB, ukkZ;  
  double eA, eB, eZero;  
  double uAnew, uBnew, uZeroneu;  
  double SWAlimit, SWBlimit, SWZlimit;
```

```

/* Generate Reference Variables */
VAref = prm_Supply_Vups*Refconst*coswtu; /* Voltage Reference d */
VBref = prm_Supply_Vups*Refconst*sinwtu; /* Voltage Reference q */

/* Reference converted to voltage. No space-vector, therefore no cAD */
VArefk = VAref*VrefXa - VBref*VrefXb;
VBrefk = VAref*VrefXb + VBref*VrefXa;

/* Calculate the 4x4 matrix quantities using voltage and current */
/* Measured (digital) values are firstly converted to voltage and current */

/* Load Voltage */
Valpha = cDV*(Space4d(ADC->Vla,ADC->Vlb,ADC->Vlc));
Vbeta = cDV*(Space4q(ADC->Vla,ADC->Vlb,ADC->Vlc));
Vzero = cDV*(Space40(ADC->Vla,ADC->Vlb,ADC->Vlc));

/* Filter Current */
Ialpha = cDI*(Space4d(ADC->Ifa,ADC->Ifb,ADC->Ifc));
Ibeta = cDI*(Space4q(ADC->Ifa,ADC->Ifb,ADC->Ifc));
Izero = cDI*(Space40(ADC->Ifa,ADC->Ifb,ADC->Ifc));

/* Load Current */
Iloadalpha = cDI*(Space4d(ADC->Ila,ADC->Ilb,ADC->Ilc));
Iloadbeta = cDI*(Space4q(ADC->Ila,ADC->Ilb,ADC->Ilc));
Iloadzero = cDI*(Space40(ADC->Ila,ADC->Ilb,ADC->Ilc));

/* Calculate Control Variables */

/* Calculate controller gains k1 through k3 and LFF using loadcurrent measurements */
IAV = PeakAvgCurrent; /* Peak average current calculated from controller */

Loadamp = 0.00000023547078*IAV*IAV + 0.00021847822154*IAV + 1.07024927805023;
k1 = -0.00000000872426*IAV*IAV*IAV + 0.00001092114822*IAV*IAV -
      0.00360070652937*IAV - 0.30040954190857;
k2 = 0.00000444241043*IAV*IAV - 0.00496298262790*IAV + 3.05077609453910;
k3 = 0.00000130551308*IAV*IAV - 0.00162756799734*IAV + 1.35157889076053;
LFF = k2*Loadamp;

```

/ Limit Control Variables */*

if (k1 < -0.6294)

k1 = -0.6294;

if (k1 > -0.4039)

k1 = -0.4039;

if (k2 < 1.6950)

k2 = 1.6950;

if (k2 > 2.9138)

k2 = 2.9138;

if (k3 < 0.8438)

k3 = 0.8438;

if (k3 > 1.3040)

k3 = 1.3040;

if (LFF < 1.6950)

LFF = 1.6950;

if (LFF > 3.3882)

LFF = 3.3882;

/ */*

/ Deadbeat Controller */*

dukkA = ukkAm1;

dukkB = ukkBm1;

dukkZ = ukkZm1;

ukkA = (-k1*(Valpha-VArefk) - k2*lalpha - k3*(dukkA-VArefk));

ukkB = (-k1*(Vbeta-VBrefk) - k2*lbeta - k3*(dukkB-VBrefk));

ukkZ = (-k1*Vzero - k2*lzero - k3*dukkZ);

/ Control Reference, including Neutral Wire switching*/*

r_Vd = VArefk + ukkA + (LFF)*Iloadalpha;

r_Vq = VBrefk + ukkB + (LFF)*Iloadbeta;

r_V0 = ukkZ + (LFF)*Iloadzero;

```
/* Calculate zero-state switching */
```

```
tuA = (2.0)*((r_Vd) + (0.35355339)*(r_V0))*imVdc*cVD;
```

```
tuB = (2.0)*((-0.5)*(r_Vd) + (0.866025403)*(r_Vq) + (0.35355339)*(r_V0))*imVdc*cVD;
```

```
tuC = (2.0)*((-0.5)*(r_Vd) - (0.866025403)*(r_Vq) + (0.35355339)*(r_Vq))*imVdc*cVD;
```

```
maxduty = tuA;
```

```
minduty = tuA;
```

```
if (tuB > maxduty)
```

```
    maxduty = tuB;
```

```
if (tuC > maxduty)
```

```
    maxduty = tuC;
```

```
if (tuB < minduty)
```

```
    minduty = tuB;
```

```
if (tuC < minduty)
```

```
    minduty = tuC;
```

```
zs = (-0.5*(maxduty + minduty));
```

```
/* */
```

```
/* Calculated Applied Signals */
```

```
SWAlimit = r_Vd;
```

```
SWBlimit = r_Vq;
```

```
SWZlimit = r_V0;
```

```
if (r_Vd > Vapplied)
```

```
    SWAlimit = Vapplied;
```

```
if (r_Vd < -Vapplied)
```

```
    SWAlimit = -Vapplied;
```

```
if (r_Vq > Vapplied)
```

```
    SWBlimit = Vapplied;
```

```
if (r_Vq < -Vapplied)
```

```
    SWBlimit = -Vapplied;
```

```
if (r_V0 > Vapplied)
    SWZlimit = Vapplied;
if (r_V0 < -Vapplied)
    SWZlimit = -Vapplied;
/* */

/* Store variables */
ukkAm1 = SWAlimit;
ukkBm1 = SWBlimit;
ukkZm1 = SWZlimit;

r_Vd = SWAlimit;
r_Vq = SWBlimit;
r_V0 = SWZlimit;
}
```