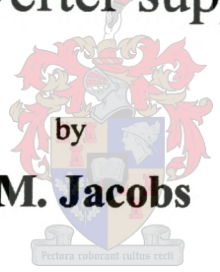
University of Stellenbosch

Voltage control of medium to high power three-phase inverter supply systems



by

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Thesis presented in partial fulfilment of the requirements for the degree of M.Sc.Eng (Electrical) at the University of Stellenbosch

Supervisor: Prof. M.J. Kamper

Date: December 2001.

Declaration

I, the undersigned, hereby declare that the work contained in this thesis is my own original work, unless otherwise stated, and has not previously, in its entirety or in part, been submitted at any university for a degree.

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December 2001.

Summary

In this thesis a new voltage control method is developed for a three-phase inverter supply system. The inverter supply system consist of a Permanent Magnet Generator, a three-phase rectifier, a three-phase inverter plus LC-filter and a three-phase transformer in series. This system supplies power to a network or to a stand-alone load. The main focus of this thesis is on the control aspects of the inverter and the LC-filter.

Different voltage control systems are investigated and compared to each other. From these methods the proposed voltage control method is developed where only the output voltages are measured to establish good voltage control. All these voltage control methods are also simulated with a software package. The proposed voltage control method compares very well with other voltage control methods. The results that are obtained in the simulations are satisfactory. The proposed voltage control method is also implemented in an 8 kW laboratory scale model and, again, very good practical results are obtained. A TMS320F240 DSP controller is used to implement the proposed voltage control method. The controller compensates well for load steps, and these results compare well to an alternative voltage control method, which was also evaluated practically.

Opsomming

In hierdie tesis is 'n nuwe spanningsbeheermetode ontwikkel vir 'n drie-fase wisselrigter kragtoevoerstelsel. Die wisselrigter kragtoevoerstelsel bestaan uit 'n Permanent Magneet Generator, 'n drie-fase gelykrigter, 'n drie-fase wisselrigter plus LC-filter, en 'n drie-fase transformator in serie. Hierdie stelsel voorsien krag aan 'n netwerk sowel as aan 'n alleenstaande las. Die hooffokus van hierdie tesis is op die beheeraspekte van die wisselrigter en LC-filter.

Verskillende spanningsbeheermetodes is deeglik ondersoek en vergelyk met mekaar. Uit hierdie metodes is dan die voorgestelde beheermetode ontwikkel waar slegs die uittreespanning gemeet word om goeie spanningsbeheer te kan doen. Al hierdie spanningsbeheermetodes is dan gesimuleer met 'n sagteware pakket. Die voorgestelde spanningsbeheermetode vergelyk baie goed met die ander spanningsbeheermetodes. Die resultate verky in die simulasies is ook baie bevredigend. Die voorgestelde beheermetode is ook geïmplementeer op 'n 8 kW laboratorium skaalmodel en weereens is baie goeie praktiese resultate verky. 'n TMS320F240 DSP-beheerder is gebruik om die voorgestelde beheermetode mee te implementeer. Die beheerder kompenseer baie goed vir lastrappe en vergelyk ook goed met 'n ander spanningsbeheermetode wat prakties ge-evalueer is.

Acknowledgements

I would like to express my sincere appreciation to the following:

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2. My supervisor, Prof. M.J. Kamper for his assistance, advice and encouragement, and also proof-reading of this thesis.

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List of Abbreviations

PMG – Permanent Magnet Generator

DC – Direct Current

AC – Alternating Current

HVDC – High Voltage Direct Current

DSP – Digital Signal Processor

AFPMG – Axial Flux Permanent Magnet Generator

IGBT – Insulated Gate Bipolar Transistor

A/D – Analogue to Digital

PWM – PulsWidth Modulation

PC – Personal Computer

1 INTRODUCTION

Renewable energy has become more and more important today with the ever-increasing demand for electricity. As the demand for electricity increases, alternative ways of generating electricity should be investigated. In this thesis, an inverter-based power supply system is evaluated and tested to deliver power to both a three-phase network grid and/or a stand-alone configuration.

1.1 Biomass as an alternative energy source

The total annual production of biomass-energy is estimated to be more than four times the total annual world consumption of energy from all current sources [1]. That is a huge amount of energy that can be used and converted into electrical power. Today biomass contributes to about 13% of the world's primary energy supply [2]. The biomass is used as the main source of energy, which is converted into heat energy. This heat energy is then converted into mechanical energy with a heat engine. The mechanical energy from the heat engine is then converted to electrical energy with the use of a generator.

1.2 Problem Statement

This thesis focuses on the control aspects of an thermo-electrical power supply system. A block diagram of the system is shown in Figure1-1 below. The main focus of this project is highlighted in dotted lines, that is the **Power conversion and Control** part of the system.

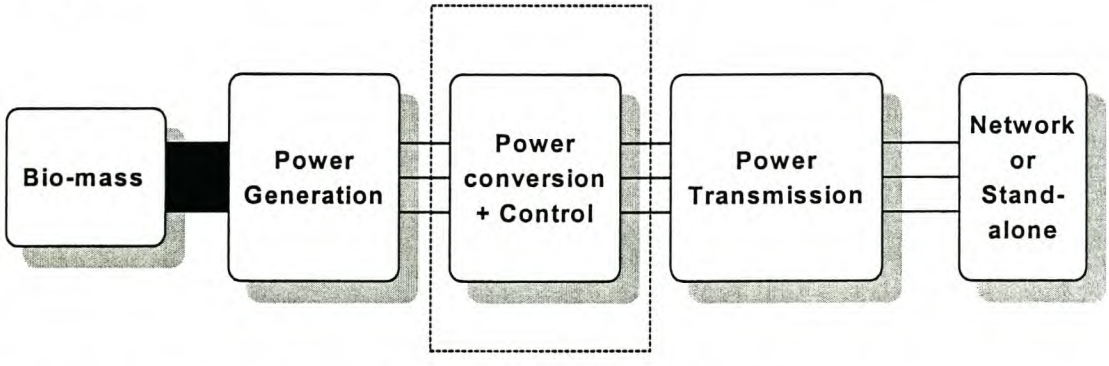


Figure 1-1: Block diagram of the power supply system.

The source of energy for the generation system is planned to be biomass, which is converted into heat energy to power a heat engine. The mechanical power of the heat engine is converted into electrical energy through a Permanent Magnet Generator

(PMG). The three-phase output voltages of the PMG are designed to be 620 $V_{l\text{-}l}$, which is the supply for the rest of the Power Supply system of Figure 1-1.

The output voltages of the Permanent Magnet Generator is then rectified to a DC voltage with a high-power rectifier. The DC-bus feeds the inverter, which produces the output voltage at 50 Hz. The output power is then fed through transmission lines/high-power cables to either a stand-alone load or a grid supply point.

The power supply system has to meet the following requirements:

- It has to deliver 300 kW power to a network grid or to a stand-alone load.
- The output voltages and frequency have to be constant.
- Compensation for voltage dips in stand-alone applications when current load steps are applied to the system, is required.
- Compensation for unbalanced conditions when delivering power to a single-phase load is also required.
- Power supply systems should be able to work in parallel to increase the power level of the system.

1.3 Approach to solving problem

Rotating generator systems are very dominant in generating electricity in earlier years. Recently when micro-controllers became very fast and also the power handling capabilities of IGBT's became higher, solid-state converters, together with unconventional generators, became more popular nowadays, although rotating generator systems are still widely used in the industry.

Initially an induction machine was considered as a generator for the power supply system in Figure 1-1. It has numerous advantages like robustness, simple construction, and relatively low cost, which is very feasible, especially if the system is connected to a grid. There are, however, some drawbacks of which the main one is the unsatisfactory voltage and frequency regulation, especially in stand-alone applications. Also, a power electronic converter should be used to control the output power dynamically [3,4]. The latter, however, is not necessarily a disadvantage.

A rectifier-inverter-filter-transformer combination is considered to be the best option, because it could supply rated power to a grid connection and also perform well under load steps in stand-alone applications [5,6,7]. This is made possible by the revolutionary development in DSP controllers [8] and also the improvement in the control techniques to regulate the output voltages of such a system in Figure 1-1.

1.4 Layout of thesis

This thesis basically consists of three main parts. The layout of the whole power supply system is given as an introduction. Then the proposed voltage control method is developed to control the output voltage dynamically, and finally the results obtained with this control method are described. The proposed voltage control method is also practically evaluated using a laboratory scale model. The thesis layout is described in the following chapters:

- **Chapter 2**: In this chapter the description and layout of the power supply system is given and the important parts are discussed in detail.

- **Chapter 3**: This chapter describes different voltage control methods considered and focuses in detail on the proposed voltage control method with simulation results in the analogue domain.

- **Chapter 4**: The proposed voltage control method is evaluated in the digital domain with simulation results.

- **Chapter 5**: The DSP controller used in this application is discussed and also how the proposed voltage control method is digitally implemented.

- **Chapter 6**: The proposed voltage control method is implemented and practically evaluated on a laboratory model.

- **Chapter 7**: Some conclusions are made in chapter 7 and recommendations are given for further work.

2 DESCRIPTION OF POWER SUPPLY SYSTEM

In this chapter the proposed power supply system of Figure 1-1 of Chapter 1 is discussed in detail. Different options of each component of the proposed power supply system are thoroughly discussed.

2.1 Power supply system layout

First, several layout possibilities to implement the power supply system are discussed, and then the proposed layout is motivated. Although the main focus of this thesis is the inverter-filter-transformer part, which is shown as the **Power Conversion and Control** part in Figure 1-1, the other sections are also briefly discussed to give background information about the power supply system as a whole power supply unit.

2.1.1 Layout possibilities

To deliver the power to a network or stand-alone load, it can either be transmitted through AC or DC transmission. In this section, different layout topologies for transmitting the power through either AC or DC transmission are discussed. First, a High Voltage Direct Current transmission (HVDC) system is considered as a possible power supply topology. The system block diagram is shown in Figure 2-1.

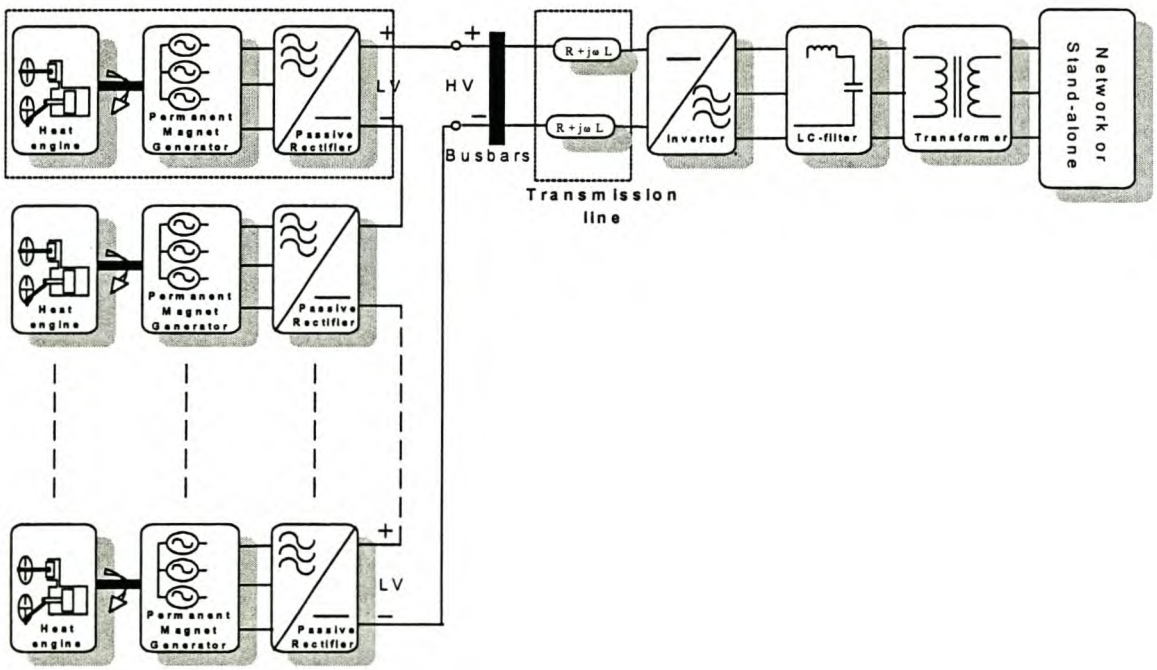


Figure 2-1: Block diagram of HVDC transmission system.

Each power supply unit, which is highlighted in dotted lines in Figure 2-1, consists of a heat engine, a Permanent Magnet Generator and a high-power passive (diode) rectifier. These units can be build separately and connected in series to a common busbar to create a HVDC power supply system shown in Figure 2-1. From the high-voltage busbars, transmission of the power can be done with high-power cables. An advantage of this topology is that the different units of the power supply system can be easily connected in series to realise a HVDC transmission system. The power can be transmitted with a single high-voltage cable. A disadvantage of the system is that all the units must run under all load conditions. If one unit fails (goes open-circuit), the whole system is shut down. Another disadvantage is that the Permanent Magnet Generators are not grounded and therefore very high voltages appear across the windings and the casings of the generators. This requires a special design of the generator that can make it expensive. After the transmission of the power, the DC voltage has to be converted to an AC supply voltage. To convert the DC voltage to a 50 Hz AC voltage, a high power DC-AC converter must be used. Although there are IGBT's available that can handle high voltages, these are very expensive. Thyristors are also capable of switching such high voltages, and is less expensive than IGBT's, but the switching frequency is limited. This can have a significant influence on the dynamics of the system, especially when it is a stand-alone supply. To upgrade the HVDC system to a higher power level, more units can be put in series with the existing units. As more units are connected in series, the DC-bus voltage increases, and therefore the transformer taps have to be adjusted to the required output voltage. The inverter, LC-filter, and transformer also have to be upgraded to handle the higher power flow.

Another possibility of power supply with multiple units is shown in Figure 2-2. Here, all the units (heat engine, PMG, active rectifier) are connected in parallel, and the DC voltage is converted into an AC voltage before the power is transmitted. This is done with the inverter, LC-filter and step-up transformer. So, besides using a parallel connection, the power is transmitted in AC quantities and thus instead of using a single DC power cable to transmit the power, a more expensive three-phase power cable is used. Again, all the units should be connected to a common AC busbar. Also, active rectifiers have to be used to establish the DC bus voltage and to ensure equal division of

power. One big concern in this case is the cross-currents that can flow between the units because of the parallel configuration.

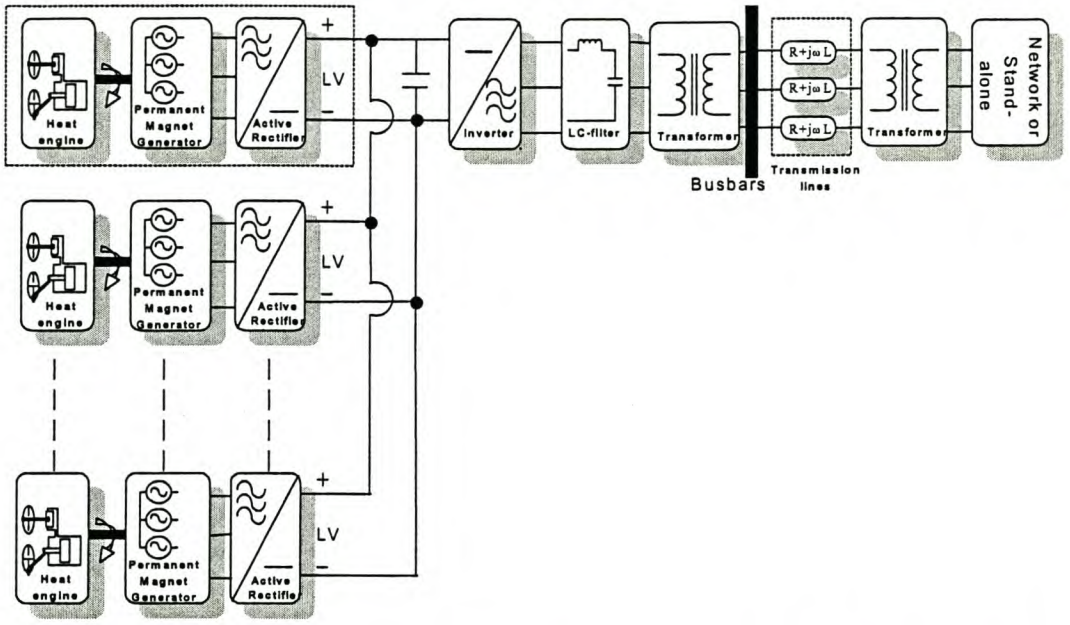


Figure 2-2: Block diagram of system with units in parallel and AC transmission.

An advantage of this configuration is that the units can be easily connected in parallel. Also, each Permanent Magnet Generator operates at a low voltage, which make the machine less expensive. To increase the power level, more units can be connected in parallel. However, with the use of active rectifiers, the whole system becomes more expensive. Also, if more units are put in parallel, the inverter and filter have to be upgraded to handle the higher power level.

A variation of the topology of Figure 2-2 is that instead of transmitting AC power with a three-phase AC transmission line, a high power DC-DC converter can be used to step up the DC voltage and transmit the DC power with a direct current and voltage transmission line. The configuration is shown in Figure 2-3.

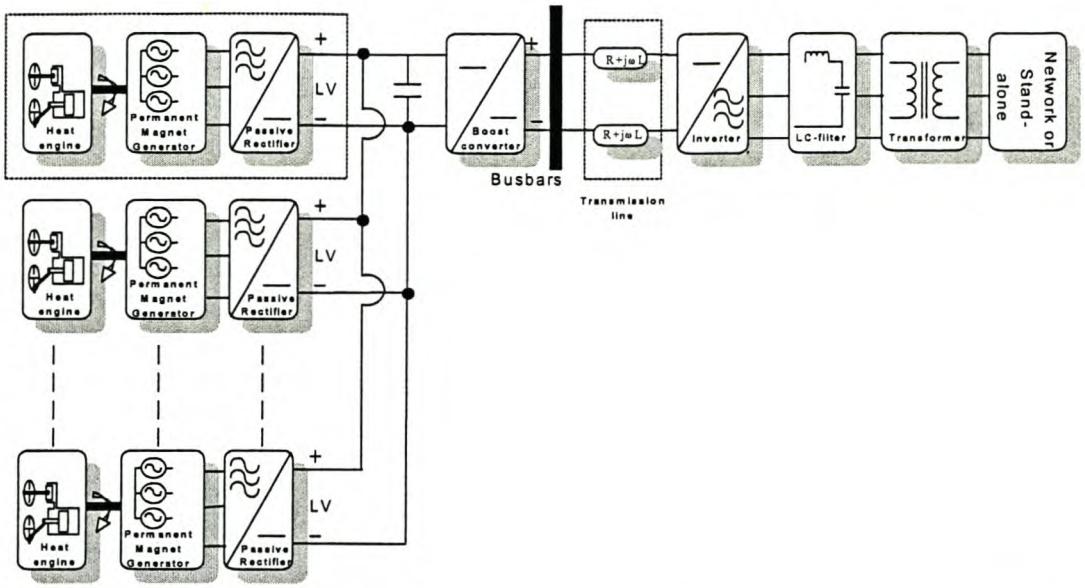


Figure 2-3: Block diagram of system with power units in parallel with DC transmission.

This configuration is also not very attractive from a cost point of view. The extra boost converter to step up the voltage for DC transmission, makes the whole system much more expensive.

After considering all the above topologies from Figures 2-1 to 2-3, a much more cost effective and versatile topology is proposed as is shown in Figure 2-4.

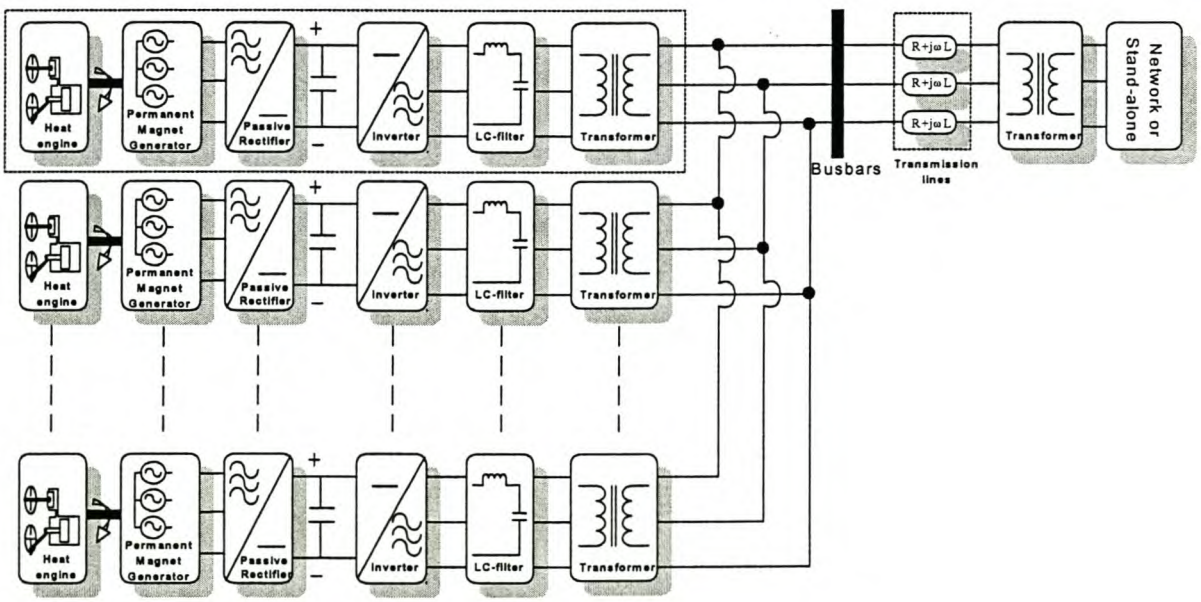


Figure 2-4: Proposed layout topology.

A big advantage of the system in Figure 2-4 over the systems in Figure 2-2 and 2-3 is that, if the systems in Figure 2-2 and 2-3 are upgraded, the inverter, filter, DC-DC converter, and transformer also have to be upgraded to handle the higher power flow. With the layout in Figure 2-4, all the units (heat engine, Permanent Magnet Generator, Passive rectifier, Inverter, LC-filter, and transformer) can just be connected in parallel to increase the power level. Also, the units in Figure 2-4 can in general be less expensive, because no active rectifiers are used and standard units can be manufactured in a mass production. A more detailed block diagram is shown in Figure 2-5 for a single power supply unit.

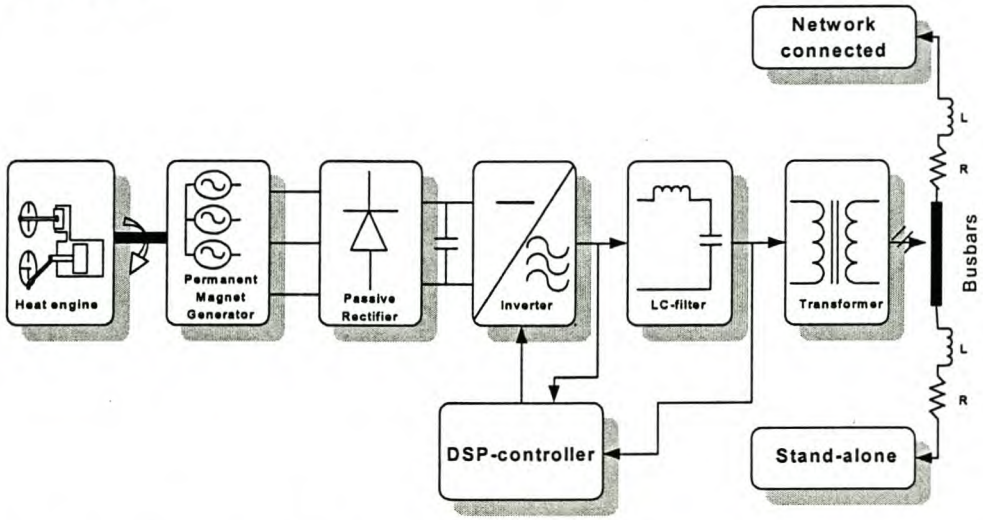


Figure 2-5: Detailed block diagram of proposed topology for a single power supply unit.

In this application, a Stirling engine is used as the heat engine. A passive (diode) rectifier is used instead of an active rectifier, because the Stirling engine's speed will be more-or-less constant due to a high inertia and fuel control, and therefore large fluctuations in the rectified DC voltage will not occur. The microprocessor used in this application can compensate for the fluctuations in the DC voltage by adjusting the modulation index of the controller. Also a passive rectifier is much cheaper than an active one. The use of a transformer is basically to isolate the three-phase output and also to step up the supply voltage if needed. The LC-filter is put before the transformer. If the LC-filter is put after the transformer, and the voltage is stepped up, the inductor and capacitor has to handle high voltages, which is not desirable. This will make the LC-filter also more expensive. Another advantage of putting the LC-filter before the transformer is that the supply to the transformer is sinusoidal (not PWM) and thus the

iron losses of the transformer is standard and a standard commercial available transformer can be used. An advantage of putting the LC-filter after the transformer is that the series leakage inductance of the transformer can be used as the filter inductance. In the following sections every block in Figure 2-5 is discussed in detail.

2.2 Stirling engine

A Stirling engine is planned to be used to generate the mechanical power, which in turn, is used to drive the Permanent Magnet Generator. The use of a Stirling engine in power supply applications has been successfully implemented [9].

2.3 Permanent Magnet Generator

An Axial Flux Permanent Magnet Generator (AFPMG) is developed as part of the proposed power supply system of Figure 2-4 and Figure 2-5. This was done at the University of Stellenbosch as part of a postgraduate research project. Figure 2-6 shows a picture of the PMG. An induction machine is initially used to get the generator up to the rated speed for load tests. The chair in the background of Figure 2-6 gives an indication of the physical size of the generator. The height of the generator is about 1,2 m.

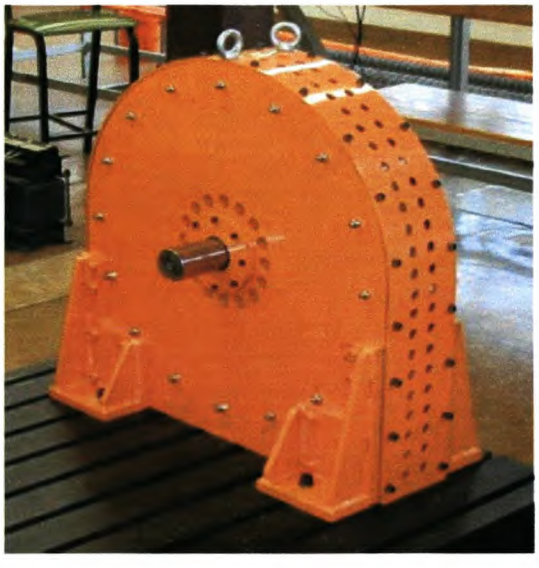


Figure 2-6: Picture of the 300 kW Permanent Magnet Generator.

Some rated values of the generator are given in Table 2-1.

Table 2-1: Design data of a 300 kW AFPM Generator

Generator	Data
Output power	300 kW
RMS rated phase voltage	360 V
Rated speed	2300 r/min
Rated torque	1420 Nm

2.4 Rectifier

A standard three-phase passive (diode) rectifier is used to rectify the three-phase output voltages from the Permanent Magnet Generator to the required DC voltage. The DC voltage is used as the source voltage for the three-phase inverter, which is discussed in the next section.

2.5 Inverter topologies

For the inverter part of the generation system of Figure 2-4, two inverter topologies are considered and is discussed in detail in the following two sections.

2.5.1 Conventional three-phase inverter

A block diagram of a conventional three-phase inverter topology, with bipolar switching, and LC-filter is shown in Figure 2-7.

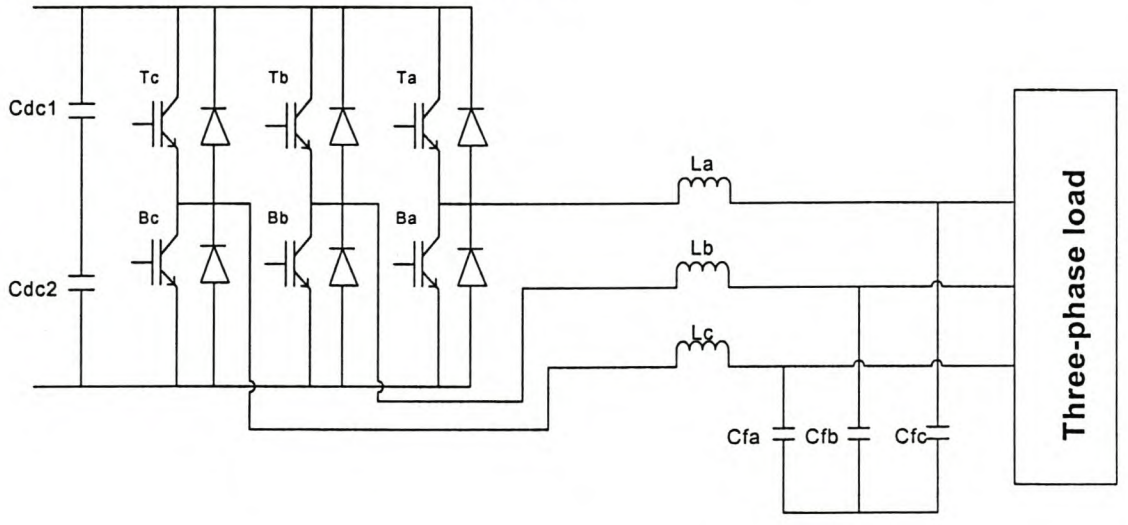


Figure 2-7: Conventional three-phase inverter topology and LC-filter.

With the bipolar switching scheme, the switches in each phase of the inverter are switched complementary by comparing a sinusoidal reference to a triangle waveform for each phase. Depending on the reference signal of each phase, either the top switches (Ta, Tb and Tc) or the bottom switches (Ba, Bb, and Bc) in each phase arm are switched. This results in a pulswidth-modulated (PWM) voltage at the output of each phase [10]. The output voltages of the inverter change between the positive DC-bus voltage and the negative DC-bus voltage. An LC-filter shown in Figure 2-7 is used to produce a relatively harmonic-free 50 Hz sinusoidal output voltage of the system.

2.5.2 *Three single-phase inverters*

The use of three single-phase inverters with a unipolar switching scheme is another inverter topology considered as is shown in Figure 2-8.

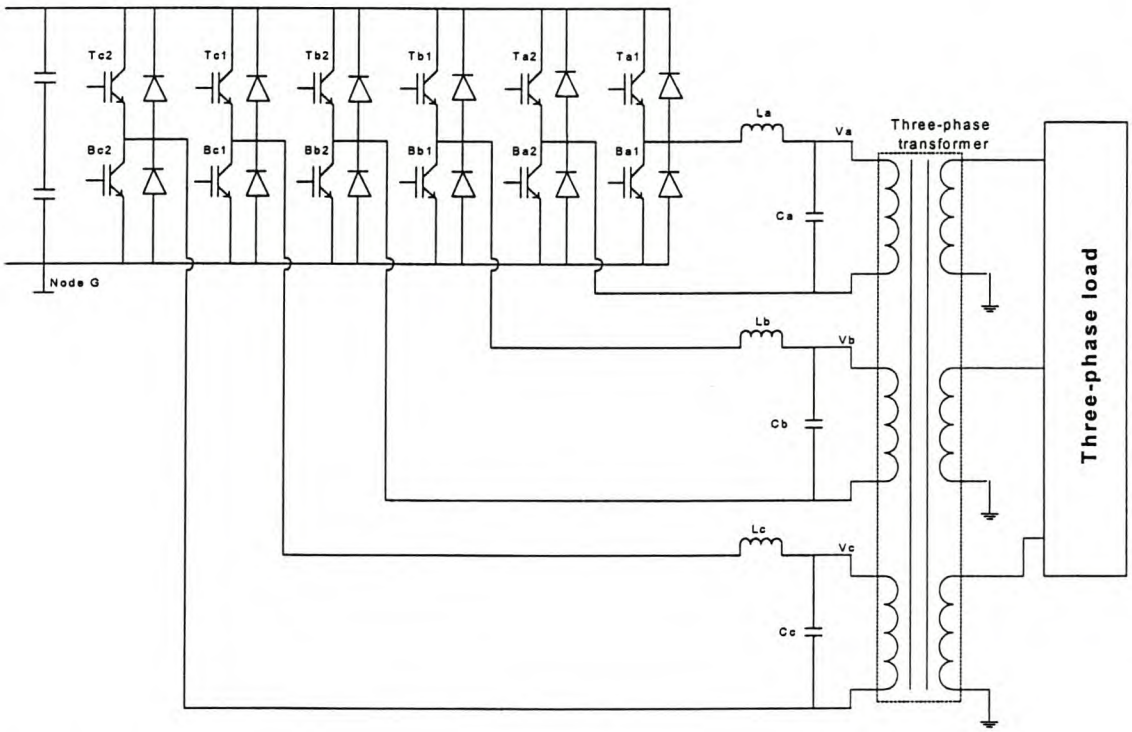


Figure 2-8: Inverter topology with three single-phase full-bridge inverters, LC-filter and transformer.

When switching unipolar, each phase is connected in a full-bridge configuration shown in Figure 2-8 where switches Ta1, Ta2, Ba1, and Ba2, for example, switches one phase. One phase-arm, Ta1 and Ba1, is switched by comparing a sinusoidal reference with a triangle waveform. The other phase-arm, Ta2 and Ba2 are switched by comparing the negative of the sinusoidal reference with the same triangle waveform. This results in a

unipolar switching scheme whereby the output voltage of the inverter changes between the positive DC-bus voltage, zero voltage, and the negative DC-bus voltage [10].

For a full-bridge unipolar voltage switching scheme, the maximum inverter output voltage is given by equation 2-1.

$$V_{rms/phase} = \frac{Vdc}{\sqrt{2}} \qquad (2\text{-}1)$$

$$= 565.69V \ (Vdc = 800\ V).$$

A larger inverter output voltage can be achieved with the same DC-bus if a unipolar switching scheme for the full-bridge configuration in Figure 2-8 is implemented, but this comes at the expense of using a transformer at the output of the LC-filter. Also twice the amount of IGBT's are needed to implement the full-bridge switching scheme. The transformer is also used to step the voltage up to the required voltage at the secondary (typical 11 kV or 22 kV). For the same output power (300 kW), the inverter current is reduced by the increased supply voltage of the full-bridge inverter, which in turn, reduce the current handling capabilities of the IGBT's. For the full-bridge unipolar switching scheme, the output switching frequency is doubled, which reduces the size of the output LC-filter. The switching losses in the inductor and capacitor for the unipolar switching scheme is less than the half-bridge bipolar switching scheme. With the use of a transformer, the load is also isolated from the power supply units shown in Figure 2-4.

2.6 LC-filter

In this section, the LC-filter values are calculated using basic calculation principles. The calculated values are just an example of what the values for the LC-filter can be. When calculating the LC-filter values, the voltage drop over the inductor and the ripple current through the capacitor have to be taken into account. A block diagram of the filter connection for a conventional three-phase inverter layout is shown in Figure 2-9.

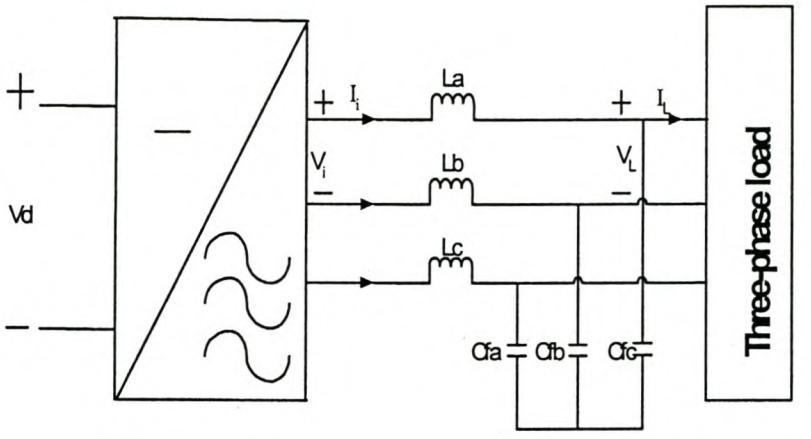


Figure 2-9: Block diagram of a conventional LC-filter connection.

For the three-phase system in Figure 2-9, the load specifications are as follows: V_L = 400 V, $P_{L(max)}$ = 300 kW, and 0,8 ≤ PF ≤ 1, where PF is the power factor. Thus at the rated power of 300 kW, the current will vary according to the power factor, i.e. $I_L = \frac{300\ kW}{\sqrt{3}V_L PF}$ and this current variation is between 433 A and 541 A. A phasor diagram and electrical circuit for one phase of the LC-filter are shown in Figure 2-10.

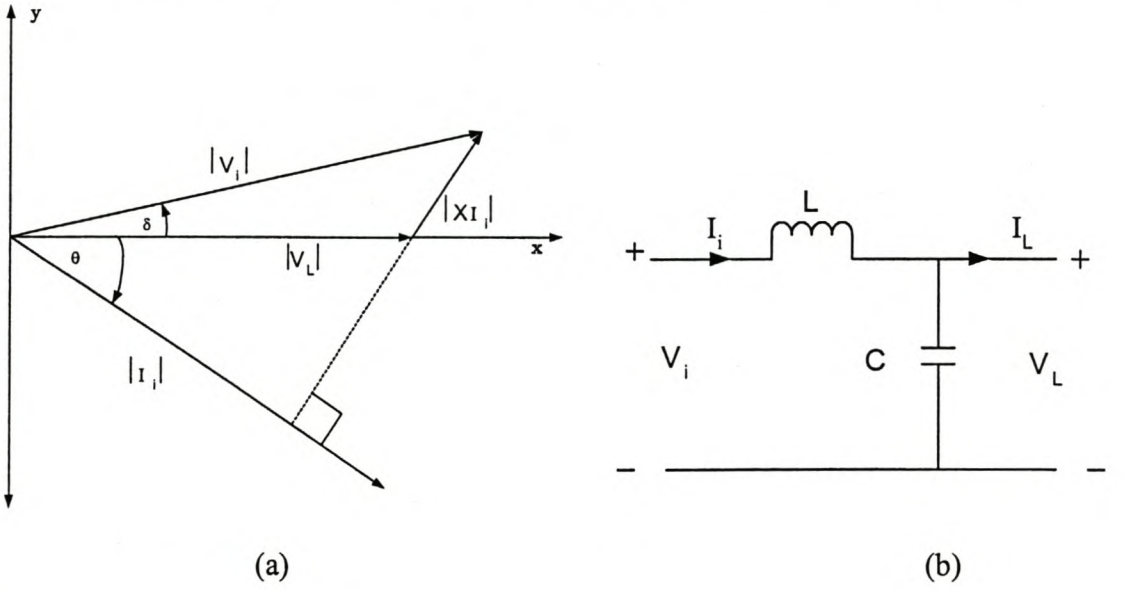


Figure 2-10: (a) Phasor diagram of system. (b) Electrical circuit for one phase of the LC-filter.

From Figure 2-10(b), the voltage equation that describes the circuit is given by

$$V_i\angle\delta = V_L\angle 0° + I_i\angle\theta.X_i\angle 90°. \qquad (2\text{-}2)$$

$$\Rightarrow \quad X_i = \frac{V_i\angle\delta - V_L\angle 0°}{I_i\angle\theta}, \qquad \text{where,} \qquad |V_L| = 230V, \qquad |I_i| \approx |I_L| = 541\ A, \qquad \text{and}$$

$\theta = \cos^{-1}(0{,}8) = 36{,}87°$ for a 0,8 power factor load.

Now, $|V_i|$ can be taken, for example, as the maximum output voltage of the inverter under full-load conditions. Thus:

$$|V_i| = \frac{0{,}612V_d}{\sqrt{3}}. \ (V_d = 800\ V) \qquad (2\text{-}3)$$

The impedance voltage drop $|XI|$ can then be determined through trigonometry as $|XI| = 76{,}6\ V$. Thus $X_i = 0{,}1416\ \Omega$ and thus $L = 450\,\mu H$. These calculations give an indication of the inductance value and the typical rated current of the filter-inductor.

The inductor can cause a very large voltage drop and there is much concern about the dynamic performance of the system under load conditions. The IGBT's also have to handle the current rating at full-load. The IGBT's that are commercially available could handle a current of 400 A peak, and it is therefore decided to use two IGBT's in parallel if a conventional inverter topology is used. Paralleling IGBT's at such a high power level could cause some problems, especially when trying to parallel IGBT's which are not manufactured from the same batch [11].

For the bipolar switching scheme, thus the maximum inductance is taken as 500 μH using equation 2-2 and 2-3 and following the calculation principles discussed in previous paragraphs. 1200 V, 400 A IGBT's are chosen which, according to the data sheets, are designed to switch up to 20 kHz. The switching frequency is decided to be 5 kHz in this application. The cut-off frequency of the LC-filter is given by:

$$f_c = \frac{1}{2\pi\sqrt{LC}} \qquad (2\text{-}4)$$

The cut-off frequency is chosen much lower (10 times) than the switching frequency, thus, the capacitor value is calculated to be 300 μF in the case where a half-bridge bipolar switching scheme is chosen.

In the full-bridge configuration, the switching frequency is kept at 5 kHz in each phase-arm, but because of the unipolar switching scheme implemented, the effective output frequency is doubled to 10 kHz. This significantly reduces the output filter to a 250 μH inductor and a 150 μF capacitor, calculated according equation 2-4. The half-bridge bipolar switching scheme and the full-bridge unipolar switching scheme are discussed in the previous sections and compared against each other and a summary is tabulated in Table 2-2.

Table 2-2: Half-bridge bipolar switching vs. Full-bridge unipolar switching – some calculated values.

Parameters	Half-bridge Bipolar switching	Full-bridge Unipolar switching	Units
Maximum output voltage of inverter (DC-bus = 800 V)	282.7	565.7	Vrms/ph
Maximum output current of inverter	442	221.0	Arms/ph
Filter inductor	500	250	μH
Filter capacitor	300	150	μF
KVA-capability of inverter	375	375	KVA
Max. volt drop over inductor	85.4	21.3	V
Ripple current in inductor	205	51.25	A p-p

From Table 2-2, it can clearly be seen that a full-bridge unipolar switching scheme has more advantages over the half-bridge bipolar switching scheme. Again, by doubling the applied voltage, the current handling capabilities of the IGBT's are reduced by half for the same output power. No paralleling of IGBT's is required as in the case with the half-bridge inverter topology. Also, by switching unipolar, the output filter is significantly reduced. This also reduces the rating of the inverter. The ripple in the inductor current is also reduced substantially. The advantages and disadvantages of the two switching schemes are summarised in Table 2-3.

Table 2-3: Summary of the half-bridge bipolar switching scheme and the full-bridge unipolar switching scheme.

Half-bridge bipolar switching		**Full-bridge unipolar switching**	
Advantages	Disadvantages	Advantages	Disadvantages
Less IGBT's needed	Expensive IGBT's	Cheaper IGBT's	Twice the number of IGBT's needed
	Filter voltage drop large	Filter voltage drop small	
No transformer cost (if not required)	Output filter large	Reduced output filter	Cost of transformer
	High-current cables (but only three)	Lower-current cables (but six)	

An air-core inductor is chosen over an iron-core inductor in the LC-filter design, because of the following reasons:

- the flux remains linear, thus it does not saturate
- no iron losses
- weight is less than a iron-core inductor
- cost less than a iron-core inductor

Also, if an air-core inductor is used, more copper is used than the iron-core inductor for the same inductance and that will increase the copper losses, but in general the total losses of the air-core inductor will be less than an iron-core inductor.

A disadvantage of the air-core inductor is that the flux is widely diffused (wide-spread)

around the inductor, while with the iron-core inductor it is concentrated in the core. This implies less interference with sensitive surrounding equipment.

A 250 μH inductor with a current rating of 280 A rms is designed by using [23] and the dimensions of the air-core inductor is shown in Figure 2-11 using the MATLAB program in Appendix D. Although the high-power inductor is designed, it was not built and tested. However, a test coil of 1 mH is designed and built and good correlation is found between the design equations and the measured inductance. The inductor is shown to give an indication of a typical design of a 250 μH, 280 A air-core inductor for an LC-filter of a 125 kVA single-phase inverter power supply system.

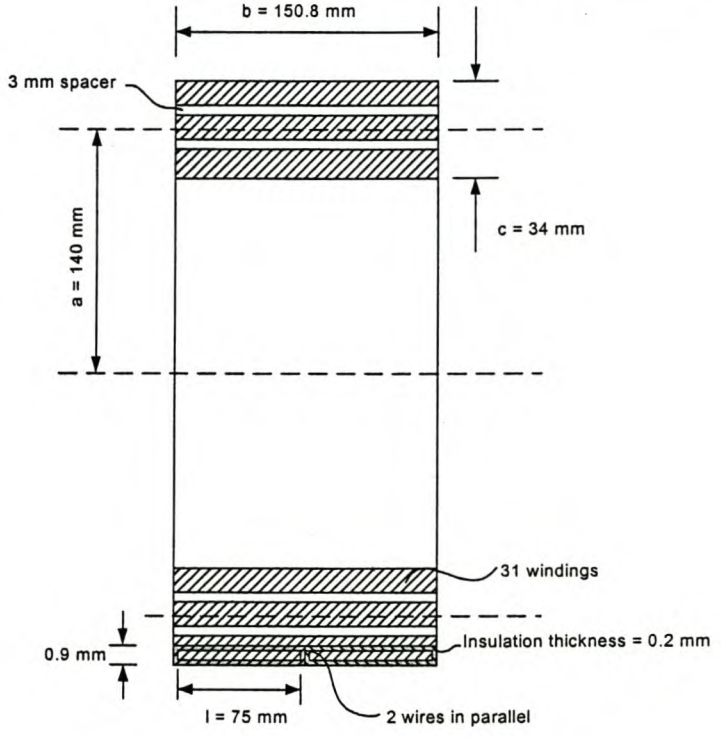


Figure 2-11: Physical dimensions of a 250 μH air-core inductor (see Appendix D).

The capacitance is calculated by equation 2-4 to be 150 μF. Caution is taken not to make the capacitor too large, because by increasing the capacitance, the impedance of the capacitor is reduced, and higher reactive current flow through the capacitors. This, in turn, could make the capacitor bank more expensive as more capacitors have to be put in parallel to handle the capacitor current.

2.7 Power Transformer

As power transformers form a very important part in power distribution, it is essential that all the important factors have to be considered when choosing such a power transformer like:

- Voltage regulation

- No-load and full-load losses
- Noise interference
- Reliability

Also, different transformer configurations have to be considered in this application. The two basic transformer configurations considered are (i) three-single-phase transformers and (ii) the conventional three-phase transformer. These two transformer configurations with their advantages and disadvantages are discussed in the following subsections.

2.7.1 Three single-phase transformers

The power supply system can be easily modified to supply power to three single-phase loads by connecting the output through single-phase transformers. When a three-phase supply is to be implemented, the secondary of the three single-phase transformers can be connected in star with the supply voltages 120° out of phase with each other. Figure 2-12 shows a block diagram of the three single-phase configuration with a three-phase load. The rating of such a single-phase transformer is typical 125 kVA for a 100 kW power supply unit, where a power supply unit is defined as the rectifier, inverter and LC-filter combined.

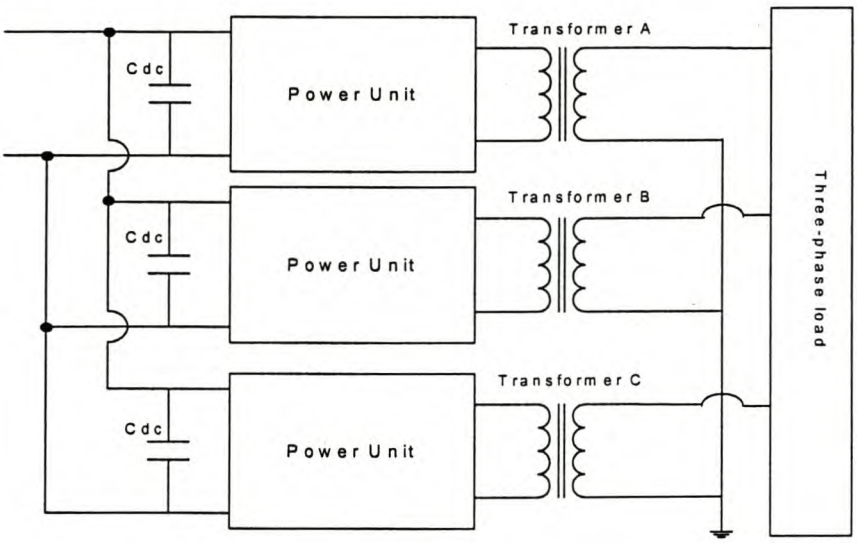


Figure 2-12: Three power supply units with three single-phase transformers connected in star to supply a three-phase load.

An advantage of this type of connection is that, if one single-phase transformer fails, only that particular transformer has to be replaced. Also, for maintenance purposes, each single-phase transformer can be serviced separately. Another advantage of this

type of transformer configuration is that you can supply three independent single-phase loads, typical in a rural area application. This makes the power supply system more redundant.

2.7.2 Conventional three-phase transformers

Another configuration is to connect a three-phase supply to a three-phase transformer with a single core. The core can be a conventional three-legged (E)-type core. A block diagram is shown in Figure 2-13. The rating of the transformer is typical 400 kVA for this application.

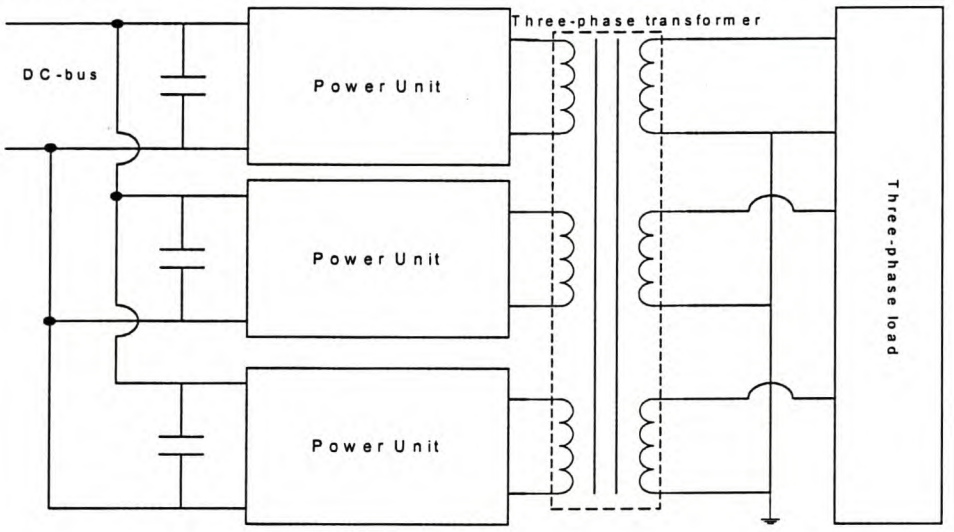


Figure 2-13: Three-phase transformer connection.

The advantages of the single core three-phase transformers are:

- contains less iron than three single-phase units
- cost less than three single-phase transformers
- weight is less than three single-phase transformers
- require less floor space
- has a higher efficiency

The biggest disadvantage if a failure would occur, is that the whole three-phase transformer has to be replaced. Also, if three separate single-phase loads have to be supplied, unbalanced conditions can exist if a single three-phase transformer is used. The following chapter will discuss the control method used to control the output voltages of the power supply system.

3 DEVELOPMENT OF CONTROL METHOD

Many voltage control methods for controlling three-phase inverters together with an LC-filter exist today, especially in UPS applications [5,6,12,13,14]. Most of these voltage control methods involve measuring the output voltages, inductor currents, and also the load currents of a three-phase system. To measure all these parameters in a three-phase system, very fast analogue to digital (A/D) converters should be used to still have a short loop-time in the control loop. To avoid this, methods are investigated to control the output voltage dynamically, but with less system parameters measured.

3.1 Control methods considered

Two voltage control methods [13,14] are evaluated in this thesis from which a proposed voltage control method is developed. Each voltage control method is discussed in detail and compared against each other in the *analogue* domain. The proposed voltage control method is further evaluated in the *digital* domain in the next chapter. An alternative voltage control method [15] is also evaluated and compared to the proposed voltage control method in the *digital* domain.

Although this thesis mainly focuses on the **generation** of power, it is important that some power quality issues also have to be discussed. The main power quality issues are voltage regulation, harmonic levels, and also load unbalance. The other power quality issues like voltage flicker, the number of forced interruptions and also the number of voltage dips per year are not considered in this thesis. A summary of the relevant standards of the NRS 048 is given in Table 3-1 below.

Table 3-1: NRS 048 summary of standards

Standard	Limit
Voltage regulation	± 10 %
Voltage unbalance	± 3% (3 phase), ± 2% (single-phase)
THD	≤ 8%
Frequency	± 2.5%

3.1.1 Current-regulated voltage control method

The first voltage control method considered in this thesis is a current-regulated voltage control method [13] shown in the block diagram of Figure 3-1. The load currents, the inductor currents and the output voltages are measured to control the three-phase output voltages of the power supply system. Although this method performs very well under load conditions, the reliability of the system decreases, because transducers are used to measure the output voltages, inductor currents, and the load currents. The trend in the industry is to have the minimum sensors in a power supply system, but the system should still achieve good dynamical characteristics. Also, by measuring all these parameters with a Digital Signal Processor (DSP), it can have a significant influence on the control loop-time of the control algorithm.

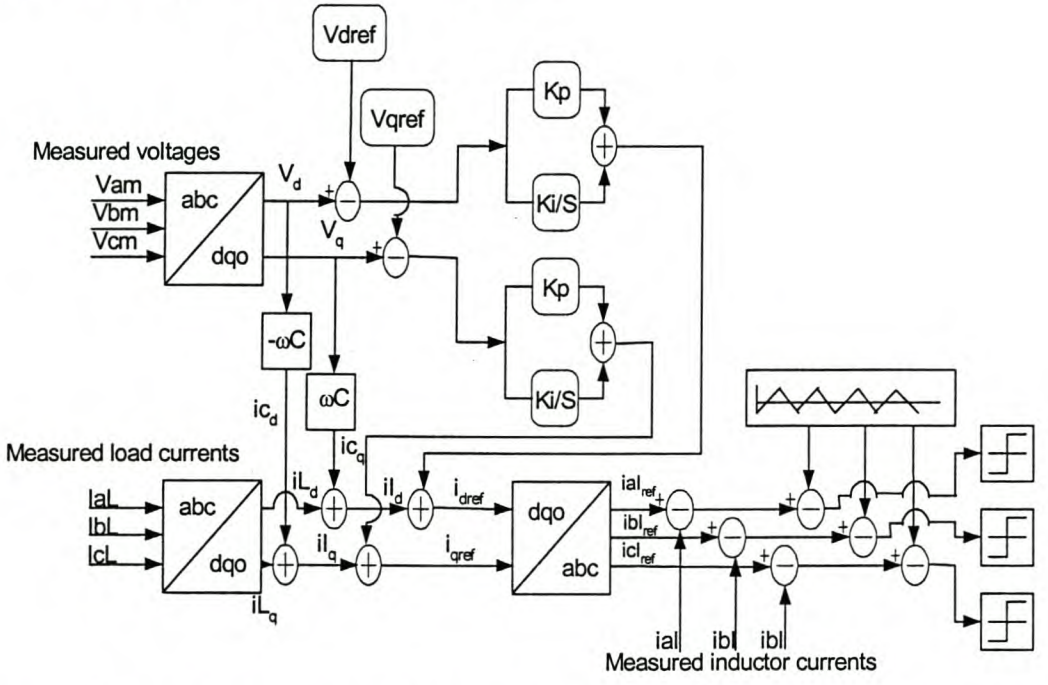


Figure 3-1: Block diagram of the current-regulated voltage control method [13].

From Figure 3-1 the output voltages, the load currents and the inductor currents are first measured and transformed into the *dq*-axis reference frame. The d-axis and q-axis voltages are then decoupled by adding and subtracting a decoupling term, ωCV_{dq}, which will be explained later in section 3.2. The d-axis and q-axis voltages are also compared to d-axis and q-axis reference voltages respectively. The errors are then fed to PI controllers. The outputs of these PI controllers are current references, which are added to the inductor current references. These references are then transformed back to the *abc* reference frame and compared to the measured inductor currents. The errors between

the measured inductor currents and the inductor reference currents are compared to a triangular waveform to generate the PWM voltage switching signals. Instead of using the hysteresis current controller as in [13], a PWM controller has been used in the simulation merely because the PWM controller could more easily be implemented in the DSP controller that is used in this thesis for the concerned power supply system.

Figure3-2 shows the inverter configuration used for the system, together with the LC-filter and the output transformer. All the differential equations are derived of the system, and are then transformed into the Laplace domain to realise a control block diagram of the system. This is done as follows:

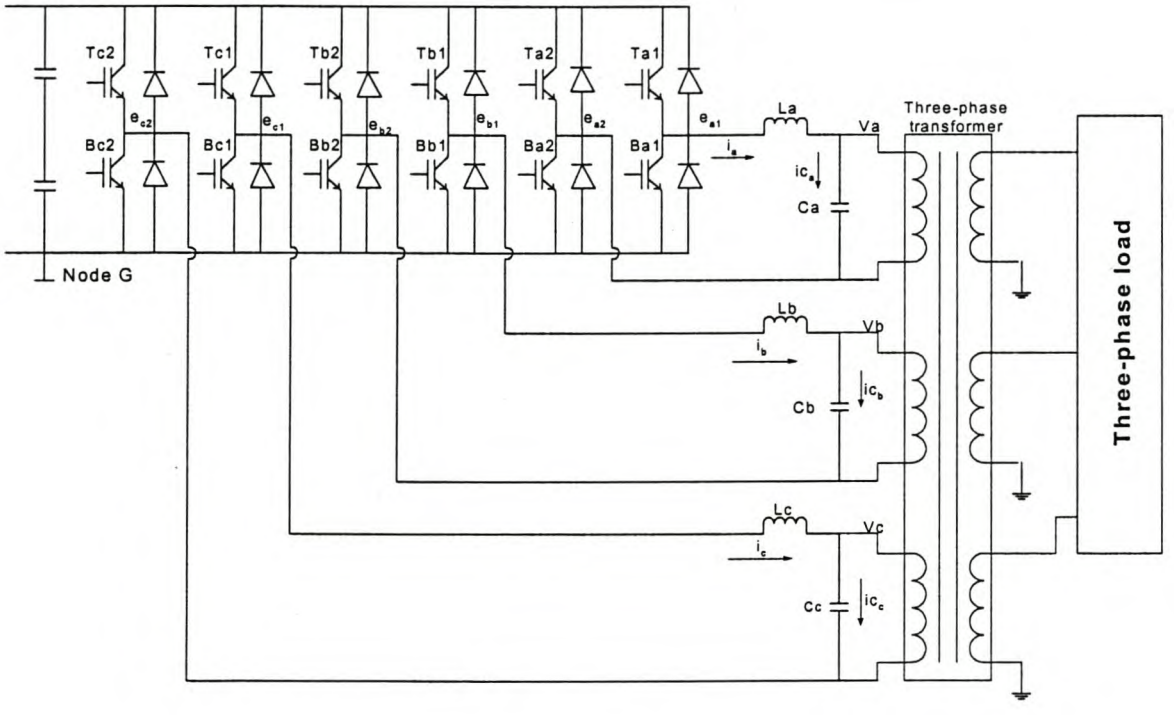


Figure 3-2: Detailed block diagram of system with unipolar switching scheme.

The voltage equations for the three phases in Figure 3-2 are:

$$e_{a1} - e_{a2} = L_a \frac{di_a}{dt} + i_a R_d + v_a, \qquad (3\text{-}1)$$

where R_d is the inductor resistance and $e_{a1} - e_{a2} = e_a$ with respect to node G in Figure 3-2.

$e_{b1} - e_{b2} = L_b \frac{di_b}{dt} + i_b R_d + v_b$, where $e_{b1} - e_{b2} = e_b$, and

$e_{c1} - e_{c2} = L_c \frac{di_c}{dt} + i_c R_d + v_c$ where $e_{c1} - e_{c2} = e_c$.

These voltages are then transformed into the synchronous reference frame by the following transformation matrix.

$$\begin{bmatrix} f_d \\ f_q \\ f_o \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos(\theta - 120°) & \cos(\theta + 120°) \\ \sin\theta & \sin(\theta - 120°) & \sin(\theta + 120°) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \quad (3\text{-}2)$$

Applying (3-2) to (3-1) yields:

$$e_d = \omega L i_q + L \frac{di_d}{dt} + i_d R_d + v_d \quad (3\text{-}3)$$

$$e_q = -\omega L i_d + L \frac{di_q}{dt} + i_q R_d + v_q \quad (3\text{-}4)$$

$$e_o = L \frac{di_o}{dt} + i_o R_d + v_o, \text{ where } L_a = L_b = L_c = L. \quad (3\text{-}5)$$

The capacitor currents are given by:

$$ic_a = C \frac{dv_a}{dt} \quad (3\text{-}6)$$

$$ic_b = C \frac{dv_b}{dt} \quad (3\text{-}7)$$

$$ic_c = C \frac{dv_c}{dt}, \text{ where } C_a = C_b = C_c = C. \quad (3\text{-}8)$$

Applying again equation (3-2) to equation (3-6) - (3-8) give the following:

$$ic_d = C \frac{dv_d}{dt} + \omega C v_q \quad (3\text{-}9)$$

$$ic_q = C \frac{dv_q}{dt} - \omega C v_d \quad (3\text{-}10)$$

$$ic_o = C \frac{dv_o}{dt}. \quad (3\text{-}11)$$

When only a resistive load is connected to the system and the transformer is assumed to be ideal and part of the load, the following equations describes the load in the synchronous reference frame:

$v_d = iL_d R$

$v_q = iL_q R$

$v_o = iL_o R$, where iL_d, iL_q, and iL_o are the *dqo*-axis components of the load currents.

All the above equations can easily be described in a block diagram by transforming all the system equations to the Laplace domain. Figure 3-3 shows the *dqo*-equivalent model of the system in the synchronous reference frame.

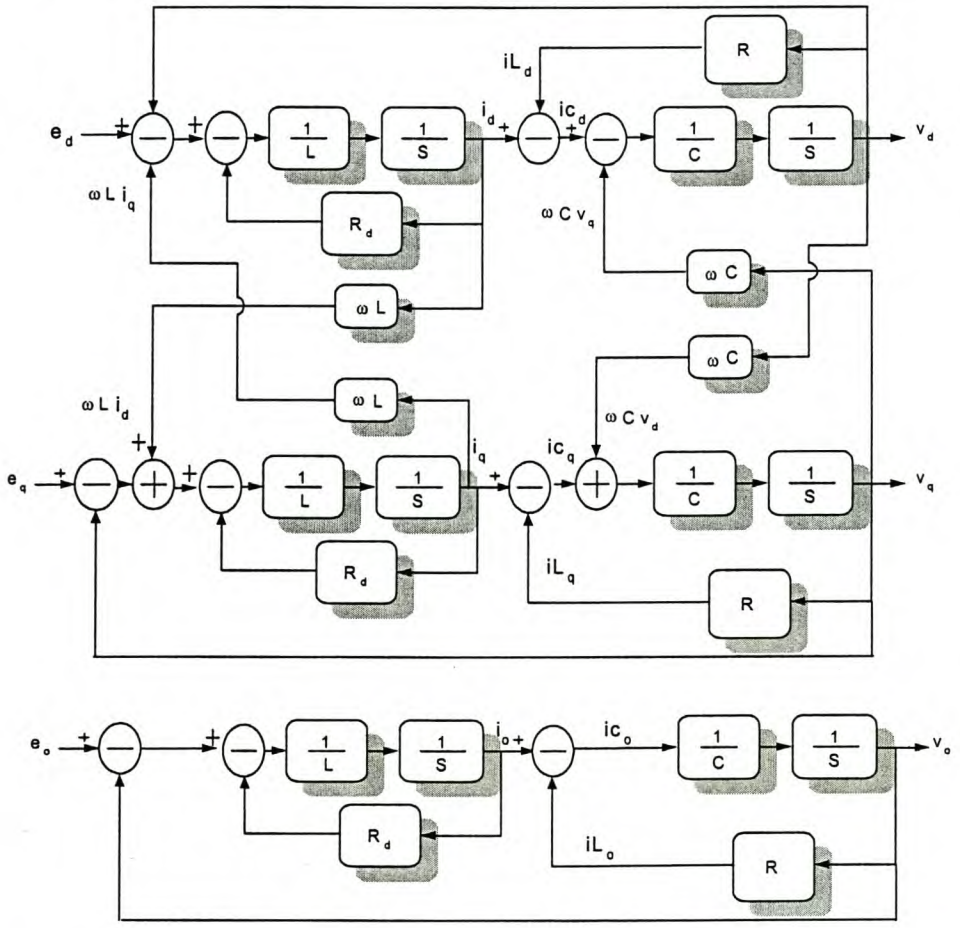


Figure 3-3: A *dqo*-equivalent model of the LC-filter and resistive load.

There are various options to control the output voltages as described in [13], but only the decoupling feedback control scheme is studied in detail as this control method is favoured to be the most attractive. With the decoupling feedback control, the output voltages are controlled by regulating the inductor currents (see Figure 3-1). To design the PI controller, it is assumed that the current controller exhibits no amplitude and phase error. This means that the inductor currents track the reference currents perfectly. The PI controller then only has to react on the $\frac{1}{Cs}$ part of the *dqo*-equivalent model as

the ωC and ωL coupling terms are decoupled by the control system as shown in Figure 3-1. The control block diagram for the d-axis voltage controller is shown in Figure 3-4.

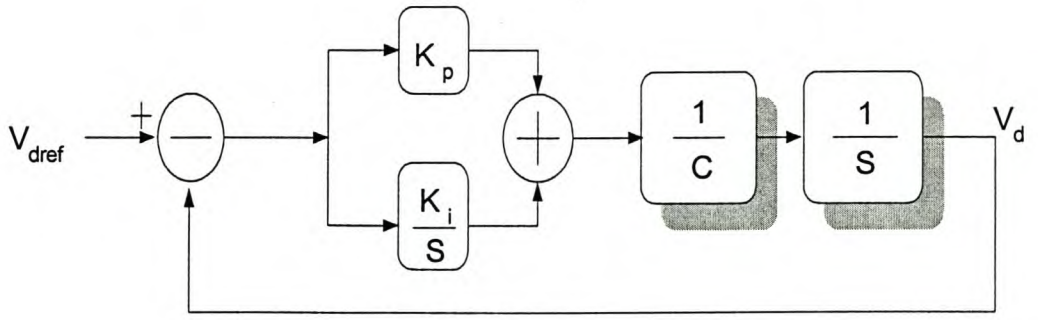


Figure 3-4: Control block diagram of d-axis voltage controller of Figure 3-1.

The closed loop transfer function is then given by:

$$\frac{V_d}{V_{dref}} = \frac{\frac{K_p}{C}s + \frac{K_i}{C}}{s^2 + \frac{K_p}{C}s + \frac{K_i}{C}}$$

This is a 2nd order system and the PI controller can easily be designed using 2nd order equations. Although the controller can easily be realised, it requires the output voltages, inductor currents, and the load currents to be measured.

3.1.2 Capacitor current feedback voltage control method

Another voltage control method for single-phase systems that was proposed by [14] is studied. Although [14] proposes various single-phase control methods, only the voltage control method where the capacitor current is fed back in the control loop is studied in detail. The control method of [14] can easily be extended to a three-phase system, because the three phases are controlled independently. This method is called in this thesis the capacitor current feedback voltage control method. A block diagram of this controller for phase *a* is shown in Figure 3-5.

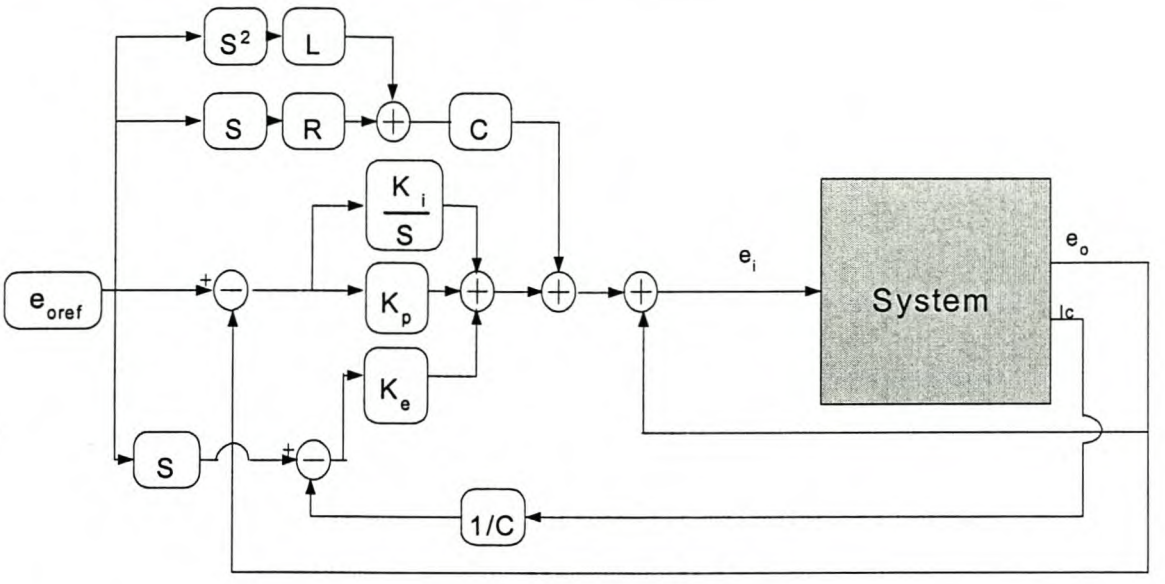


Figure 3-5: Voltage control block diagram of a single-phase system with capacitor current feedback [14].

In this method, only the capacitor currents and the output voltages are measured. The system block, which is highlighted in Figure 3-5, is the LC-filter. The LC-filter transfer function is given by:

$\frac{e_o}{e_i} = G(s) = \frac{1}{LCs^2 + RCs + 1}$, where e_o is the output voltage of the filter and e_i is the input voltage to the filter. From the transfer function, $e_{iref} = e_{oref}LCs^2 + e_{oref}RCs + e_{oref}$ where $(e_{oref}LCs^2 + e_{oref}RCs)$ is the feedforward term and e_{oref} is a decoupling term. This can be seen in the block diagram in Figure 3-5. It is assumed that $e_{oref} = e_o$. In the steady state, the feedforward terms and the decoupling term, produce the shape of the output voltage. When transients occur, the PI controller and the capacitor feedback term (K_e) compensate for a deviation in the output voltage. Instead of measuring the capacitor current directly, the capacitor voltage can be measured, differentiated and divided by the capacitor value and then fed back as the capacitor current. This control method could cause some problems when implemented with a digital controller, because of the differentiating terms in the feedforward loop and also the differentiation of the output voltages.

3.1.3 Proposed voltage control method

Instead of regulating the inductor current to control the output voltages as in Figure 3-1, the output voltages can be directly controlled with only a voltage controller. This is done by decoupling the feedback voltages (v_d and v_q) of the LC-filter and also the decoupling of the d- and q-axis voltages and currents, that is ωLi_{dq} and ωCv_{dq} (see Figure 3-3). This decoupling feedback scheme is shown in Figure 3-6.

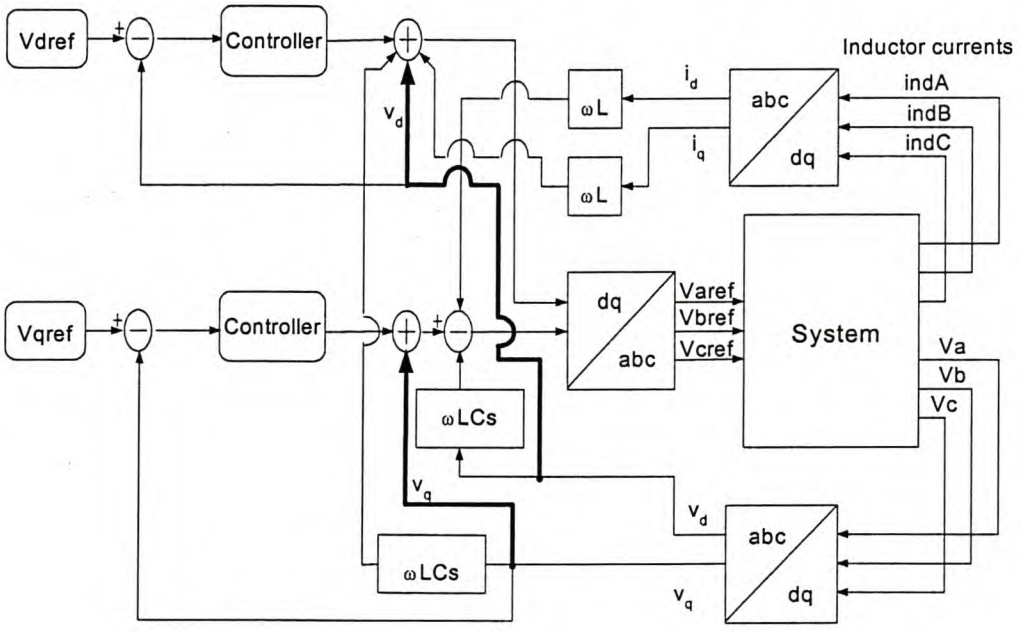


Figure 3-6: Block diagram of the proposed voltage control method.

The output voltages, which are the voltages over the capacitors (see Figure 3-2), and inductor currents are measured and transformed into the *dq* synchronous reference frame. Then the coupling terms shown in Figure 3-3, ωLi_d, ωLi_q, $\omega LCsv_d$, and $\omega LCsv_q$ are added in the control system to decouple the d- and q-axis voltages and currents. Also, the feedback voltages of the LC-filter (v_d and v_q) are also added to the control system to decouple the back-emf voltage of the LC-filter of each d- and q-axis circuit. This is shown in a bolted line in Figure 3-6. The controllers can then easily be designed if the d- and q-axis voltages are decoupled. By using the decoupling scheme, the inductor currents and the output voltages have to be measured. Later in this chapter it will be shown that, by introducing a voltage compensation technique, **only** the output voltages have to be measured to dynamically control the output voltages of the power supply system. This makes it a very attractive control scheme, because no inductor

currents or load currents have to be measured. In the next section the coupling between the d- and q-axis components of the system in Figure 3-6 is discussed in detail.

3.2 Decoupling of circuit parameters

The coupling parameters between the d- and q-axis are only briefly discussed in the previous section. In this section detail attention is given to the coupling voltages and currents. First an analogue case is discussed which is then extended to a digital control system in the next chapter to show the effect of the coupling parameters.

In Figure 3-3 all the coupling parameters are shown. These are the ωLi_q, ωLi_d voltages and the ωCv_q and ωCv_d currents. To decouple the ωLi_q and ωLi_d voltages, these only have to be added and subtracted respectively in the control system. To decouple the ωCv_q and ωCv_d currents as voltages in the control system, they have to be multiplied by the term $Ls + R_d \approx Ls$ (assume $R_d \approx 0$) as is clear from Figure 3-3. Thus, these decoupling voltages to be added and subtracted respectively are $\omega LCsv_d$ and $\omega LCsv_q$ as is shown in Figure 3-6. The voltage controller then only takes action over the $\frac{1}{Ls+R_d}$ and the $\frac{1}{Cs}$ part of the system. A block diagram of the d-axis voltage control system using a PID controller is shown in Figure 3-7. The choice and design of a PID controller is discussed further in this section. Note that in Figure 3-7 the d- and q-axis load currents are assumed constant or zero as the PID controller is designed to have good response on input d- and q-axis step voltages.

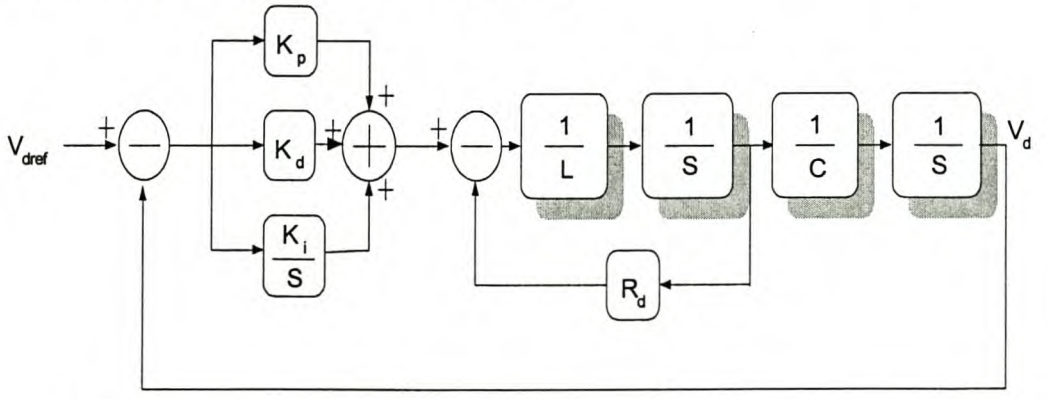


Figure 3-7: Block diagram of the d-axis voltage controller of the system of Figure 3-6.

Although PI controllers are used in most UPS applications [5,6,7,13,14,15], a PID controller is used in this application to get a faster response. PID controllers have their advantages and disadvantages. One of the important advantages is the extra zero that is added to the control system, which makes the response of the system faster. The PID controller is designed using the root-locus method. The transfer function of the PID controller is given by:

$$G_{con}(s) = \frac{(Kps + Ki)(s + A)}{s}.$$

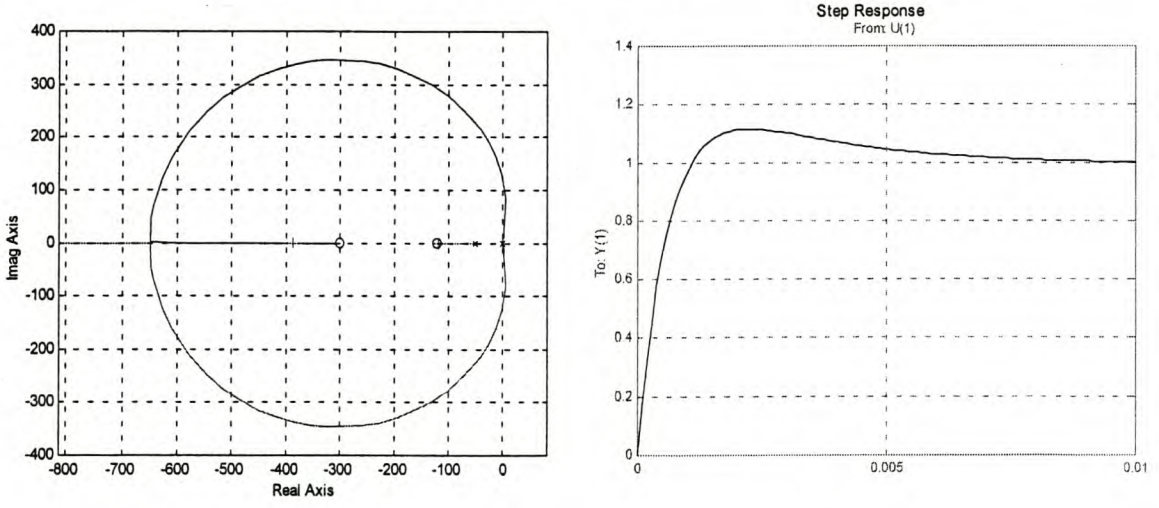
The open loop transfer function of the sub system is given by:

$$G_{sub}(s) = \frac{1}{LCs^2 + R_dCs}.$$

Therefore the open loop transfer function of the sub system with the controller is given by:

$$G_{ol}(s) = \frac{(Kps + Ki)(s + A)}{s(LCs^2 + R_dCs)}.$$

An analogue controller of the PID type is designed in MATLAB for the system. The program listing of the MATLAB program is given in Appendix C1. The design is only done to illustrate the decoupling feedback method and how well it compares to other control schemes. The root-locus and the closed loop step response of the analogue system are shown in Figure 3-8 (a) and (b) respectively.



(a) (b)

Figure 3-8: (a) Root-locus of the open loop system of Figure 3-7 and (b) Closed loop step response of d-axis voltage.

The controller is designed for a 10% overshoot and 10 ms settling time as can be seen in the simulated step response in Figure 3-8(b). All the simulations of this thesis are done with a software package called SIMUWIN, that is developed at the University of Stellenbosch.

The PID controller response is also simulated with the complete *dqo*-model of the system in Figure 3-3 and the step response results with and without the decoupling terms ($\omega Cv_d, \omega Cv_q, \omega Li_d, \omega Li_q$) are shown in Figure 3-9.

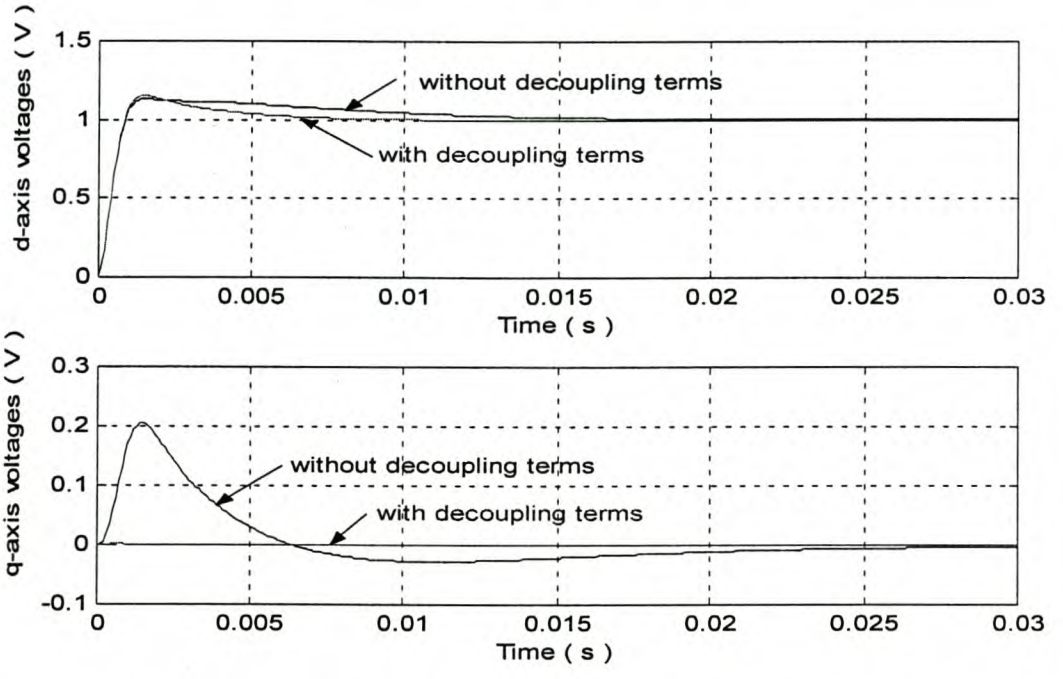


Figure 3-9: Simulated d-axis voltage response with and without decoupling terms.

From Figure 3-9 it can be seen that the d-axis voltage response is much slower without the decoupling terms. The overshoot is about the same as what has been designed for in Figure 3-8 (b). Figure 3-9 shows that with all the decoupling terms in the control loop, the system compares well with the designed d-axis voltage response. Without the decoupling terms in the control system, the controller sees these coupling terms between the d- and q-axis circuits as disturbances, therefore trying to compensate for it, but it is not designed for that. Also, when load steps are applied, the controller response is much slower without the decoupling parameters in the control loop. With the decoupling terms in the control system and a load step is applied to the system, the controller response compares well with what it was designed for.

The controller is also put into the actual three-phase system with the *dq*-transformations, but without the inverter, hence assuming an infinite switching frequency. The response is given in Figure 3-10, again with and without the decoupling terms.

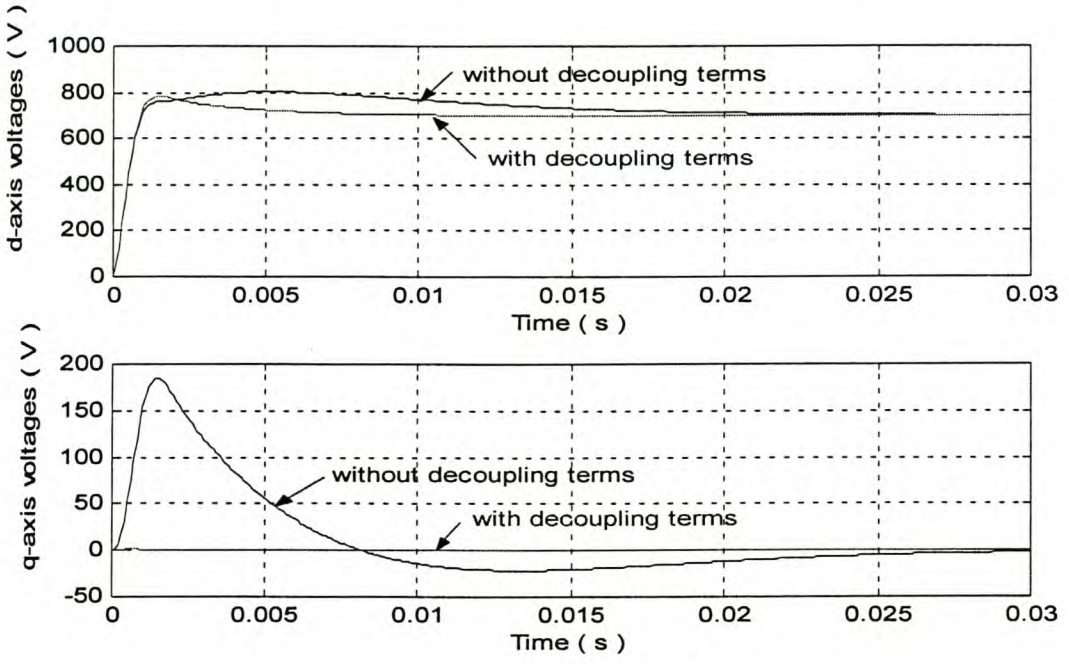


Figure 3-10: Simulated d-axis voltage step response of the actual three-phase system with and without decoupling terms.

In the actual system with the analogue PID controller, it can again be seen that the d- and q-axis coupling terms have a significant effect on the d- and q axis voltage response of the system. The d-axis reference voltage is set at 700 V peak. The q-axis voltage is not zero without the decoupling terms. The d-axis voltage of the system without the decoupling terms has a higher overshoot than the voltage response with the decoupling terms and the settling time is also much slower.

Including the decoupling terms in the control program of the microprocessor can have a significant effect on the control loop-time of the control system. The calculations of the decoupling terms of the system are real values, which can be time consuming using a fixed-point controller to calculate the decoupling terms. If the controller is a floating-point processor, the decoupling terms can easily be calculated and added or subtracted in the control loop, without having an effect on the control loop-time, but it is more expensive than a fixed-point microprocessor. A fixed-point microprocessor can be used and, instead of calculating the decoupling terms, a compensation loop can be introduced

to establish the decoupling of the d- and q-axis currents and voltages without having a significant effect on the control loop-time. It will be shown in the following section how the compensation loop, not only decouples the d- and q-axis voltages and currents, but it also dynamically compensates for load steps.

3.3 Compensation technique

Many compensation techniques exist today to compensate for disturbances which the main controller is not designed to compensate for. In power quality compensation there are many proposed techniques of which the auto- and cross correlation techniques are the most popular [16]. A compensation technique that is used successfully in many variable-speed drive applications [17,18] is introduced to compensate for disturbances that the controller is not designed for. Thus, instead of calculating the decoupling terms in the control system, which means measuring the inductor currents shown in Figure 3-6, the compensation technique in [17,18] is used to decouple the coupling terms in the system of Figure 3-6. The compensation technique is also introduced to improve the dynamic response of the system for load steps. A block diagram of the compensation loop for the d-axis control system is shown in Figure 3-11.

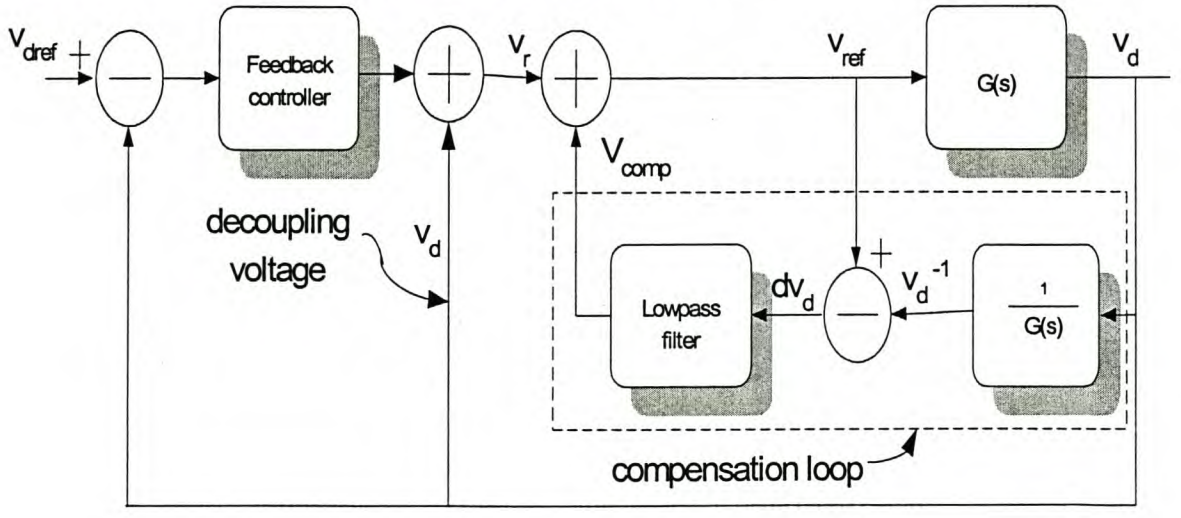


Figure 3-11: Block diagram of the compensation loop.

From Figure 3-11, $G(s) = \dfrac{1}{LCs^2 + R_dCs}$, which is the transfer function of the LC-filter without the back-emf feedback voltage (v_d). The inverse transfer function of the LC-

filter is given by: $\frac{1}{G(s)} = LCs^2 + R_dCs$. The compensation loop in Figure 3-11 only acts on disturbances on the output voltage and thus on disturbances in and to the system [17, 18,19]. If a disturbance is caused at V_r in Figure 3-11, the compensation loop does not react. This is because the error between V_{ref} and V_d^{-1} is zero and hence no compensation voltage is fed back through the lowpass filter and added to the control loop. However, if a disturbance is caused in or to the system and thus on V_d, this would produce an error between V_{ref} and V_d^{-1}. This error is fed back through the lowpass filter and is added in the control loop to compensate for the disturbance at the output voltage. The lowpass filter is added to filter high frequency noise signals due to the differentiation of the output voltage. However the time constant of the filter should be fast enough to make the compensation loop much faster than the voltage control loop, therefore helping to compensate for voltage disturbances. The compensation loop then effectively decouples the d- and q-axis terms of the system by compensating for the disturbances caused by the coupling terms. An advantage of implementing the compensation loop, is that it not only decouples the d- and q-axis circuits, but also eliminates the need to measure the inductor currents. Only the output voltages have to be measured. The final proposed voltage control block diagram is shown in Figure 3-12.

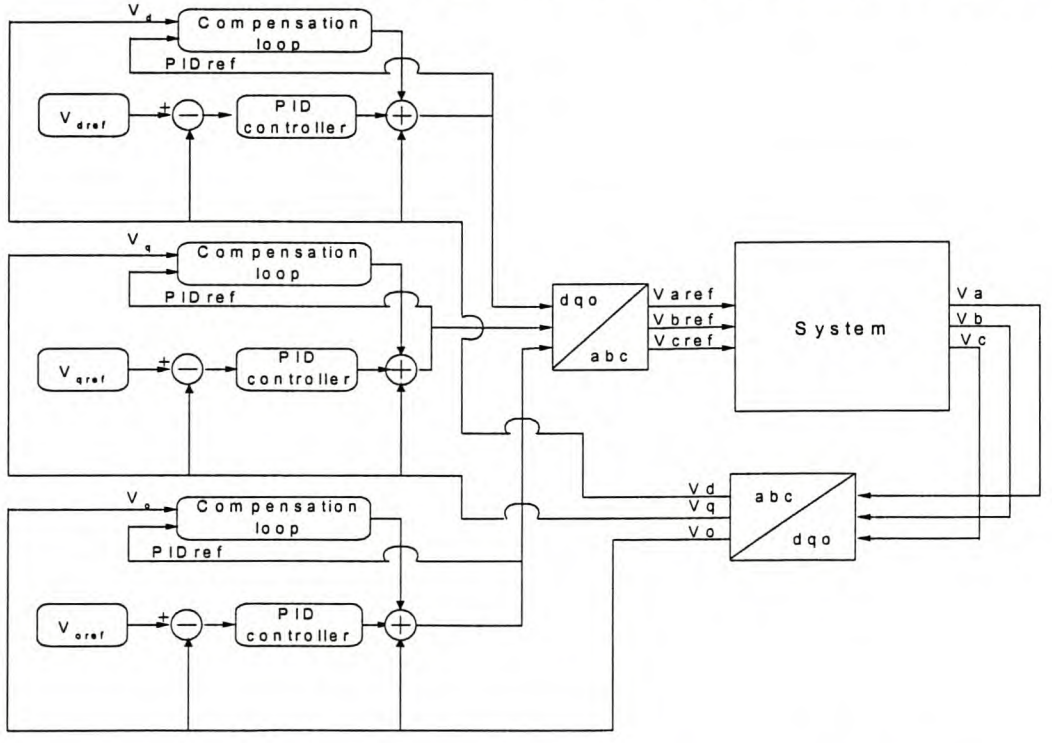


Figure 3-12: Block diagram of the final proposed voltage control method.

A simulation was done on the proposed voltage control method with and without the compensation loop and the results are shown in Figure 3-13. The PID controller designed in Figure 3-8 is used in the simulation.

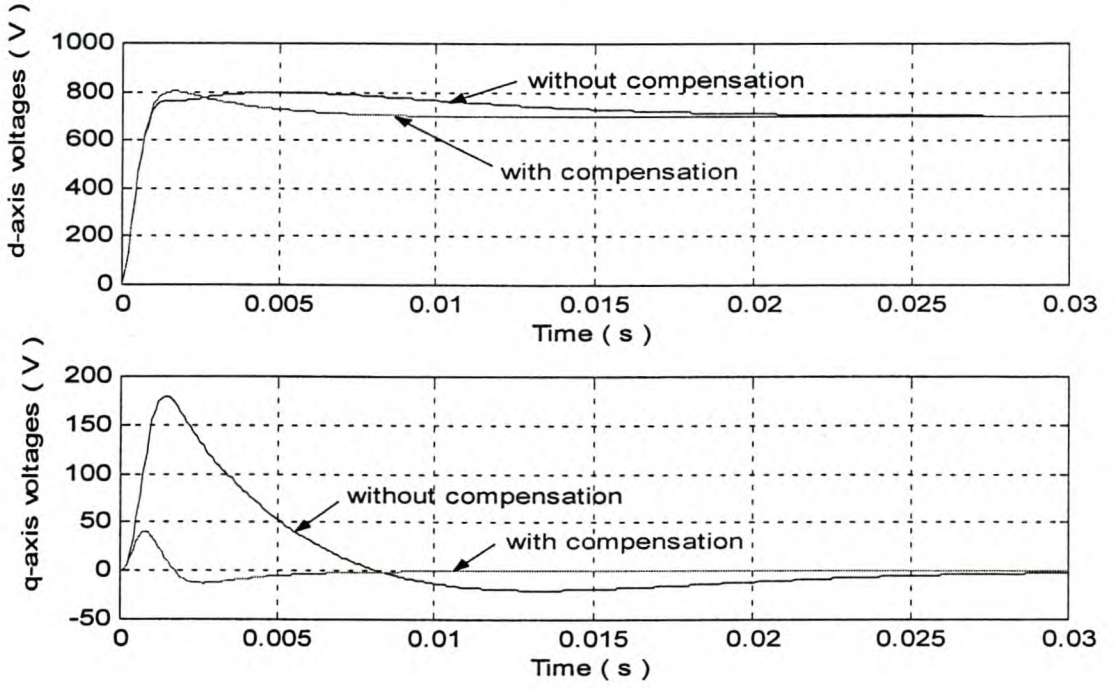


Figure 3-13: Proposed voltage control method with and without the compensation loop for a d-axis voltage step input.

Figure 3-10, and Figure 3-13 shows that the d- and q-axis voltage responses, with and without decoupling, is the same for both simulations for a d-axis voltage step input. Thus, as mentioned, instead of measuring the inductor currents (see Figure 3-6 and Figure 3-10) to decouple the coupling terms in the control system, only the output voltages shown in Figure 3-12 have to be measured to decouple the d- and q-axis circuits. Figure 3-13 shows that, with the compensation loop in the control system, the desired response is achieved.

3.4 Simulation Results

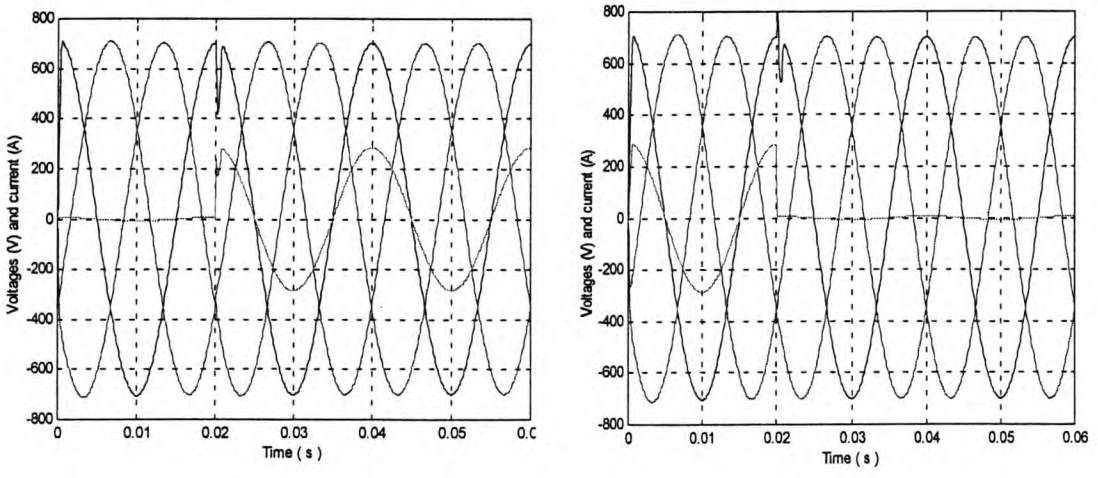
EMTDC, another simulation package, is also used but only for analogue simulations. Much difficulties, however, was experienced when trying to simulate the digital control system with EMTDC. Hence all the simulations were later done using SIMUWIN. This software is specifically designed for digital control systems.

An analogue comparison is made between the three control methods discussed in section 3.1. This is to show how the proposed voltage control method compares to other voltage control methods. The digital simulations of the proposed voltage control method are dealt with in the next chapter.

For the simulation results of section 3.4.1, a **positive** load step implies that the load is **connected** to the power supply system, and a **negative** load step implies that the load is **disconnected** from the system. Also, the voltages on the primary side of the transformer are referred to as **control** voltages, which are measured, and the voltages on the secondary side of the transformer are referred to as the **supply** voltages.

3.4.1 Load step response results

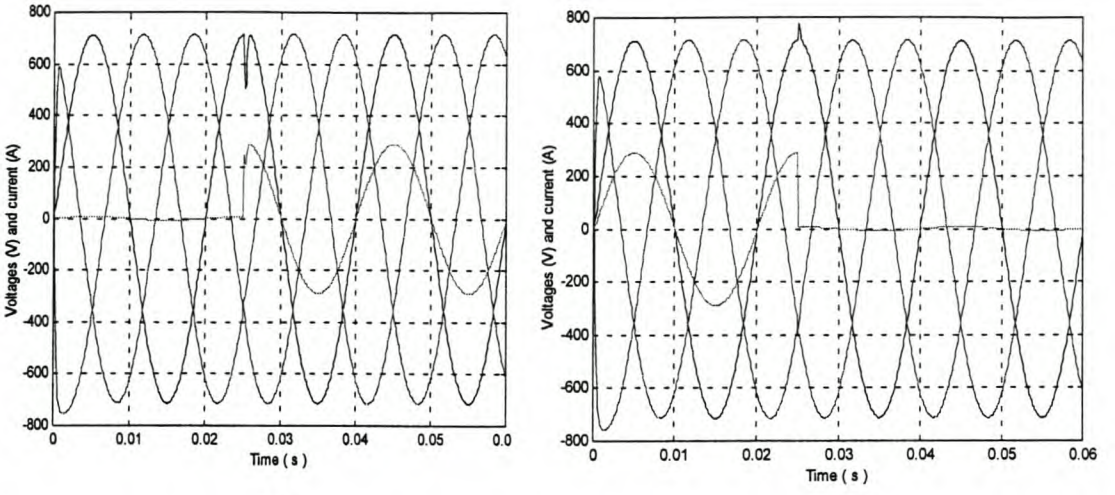
First, the current-regulated control method is simulated and a positive and negative full-load step is applied to the system. Only the phase *a* current is shown, but note that a balanced three-phase load step is applied. The results are shown in Figure 3-14.



(a) (b)

Figure 3-14: Simulated three-phase step response of the current-regulated voltage control method with (a) a positive full-load step and (b) a negative full-load step.

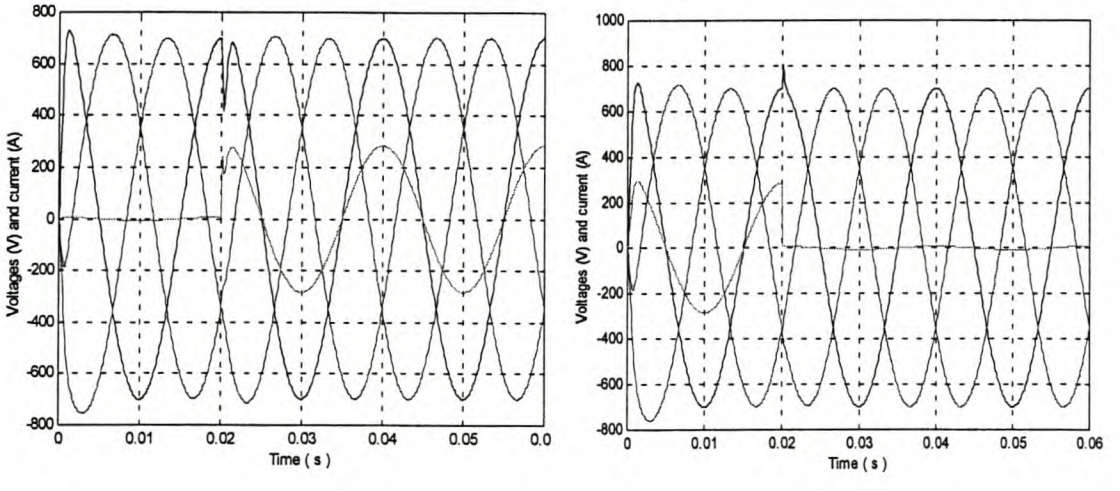
The capacitor current feedback control method discussed in section 3.1 is next simulated and the results are shown in Figure 3-15.



(a) (b)

Figure 3-15: Simulated three-phase step response of the capacitor current feedback voltage control method with (a) a positive full-load step and (b) a negative full-load step.

The proposed voltage control method with the compensation technique implemented is also finally simulated and the results are shown in Figure 3-16.



(a) (b)

Figure 3-16: Simulated three-phase step response of the proposed voltage control method with (a) a positive full-load step and (b) a negative full-load step.

In all the simulations, the three-phase currents are switched in and out at a point when the phase *a* voltage is a maximum, therefore a worst case scenario is established in phase *a*. From Figures 3-14 to 3-16, it can be seen that the proposed voltage control method compares well with the other two control methods. The response time for the

proposed control method is just over 1 ms when a full-load step is applied to the system. The voltage overshoot on the output voltage when the load is disconnected also compares well with the other simulated voltage control methods. As mentioned before, an important advantage with the proposed voltage control method is that only the output voltages have to be measured. In the capacitor current feedback voltage control method, the output voltage also have to be measured only, but when realised in a digital control system, especially with a fixed-point DSP controller, the feed-forward terms can be very time consuming on the control loop-time. This is because of the floating-point operations that have to be performed. Another disadvantage of the capacitor current feedback scheme is the differentiation terms in the control loop, especially the feed-forward terms in the control loop.

3.4.2 Unbalanced conditions

Unbalanced conditions were also investigated, connecting a single-phase load to the three-phase supply. When there is unbalance in the three-phase supply voltages, it can have a huge negative effect on the three-phase loads, which are mainly three-phase induction motors. The unbalance in the voltage can cause negative sequence currents to flow in the motor. This can cause a reduction of the torque of the motor and the motor can also start to heat up very quickly.

As before, the simulations are done using the three discussed voltage control methods in section 3.1. In all three control methods, the system is started up at half load (balanced), and then a single-phase load is connected to phase *a* to draw full-load current, while the other phases still draw half the full-load current.

The voltage unbalance can be calculated by the following equation [20]:

$$UB = \sqrt{\frac{1-\sqrt{6\beta}}{1+\sqrt{6\beta}}} \times 100, \qquad (3\text{-}12)$$

where $\beta = \frac{V_{12}^4 + V_{23}^4 + V_{31}^4}{(V_{12}^2 + V_{23}^2 + V_{31}^2)^2}$ and V_{12}, V_{23} and V_{31} are the rms line-line voltages. All the voltage unbalance calculations were done using a MATLAB program. The program listing is shown in Appendix F.

The simulation results obtained with the current-regulated voltage control method are shown in Figure 3-17. The voltage unbalance is calculated to be 0,75%. The capacitor current feedback voltage control method is also simulated with the same conditions above. The results are shown in Figure 3-18. The voltage unbalance using the capacitor current feedback voltage control method is calculated to be 0,185%. Finally, the proposed voltage control method is also simulated with the same unbalanced conditions and is shown in Figure 3-19. The voltage unbalance is calculated to be 0,194%. From the above simulations it can be seen that the controller with the capacitor current feedback method and the proposed voltage controller performs very well under the unbalanced load conditions. The current-regulated voltage controller, however, did not perform that well under the unbalanced load conditions.

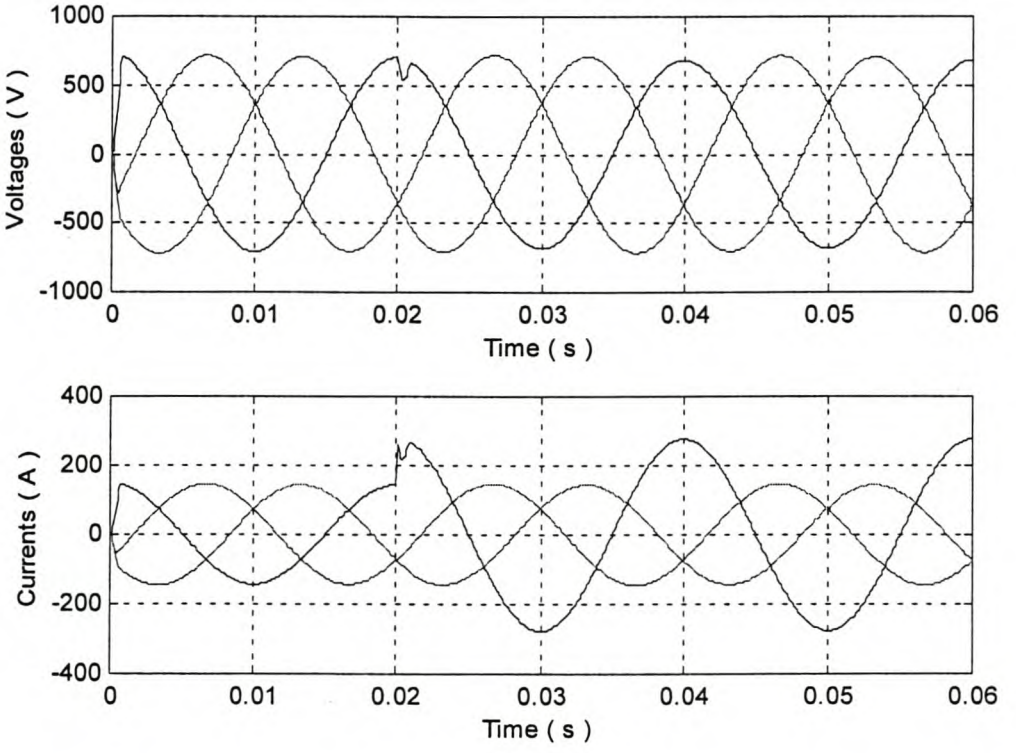


Figure 3-17: Current-regulated voltage control method with an unbalanced load.

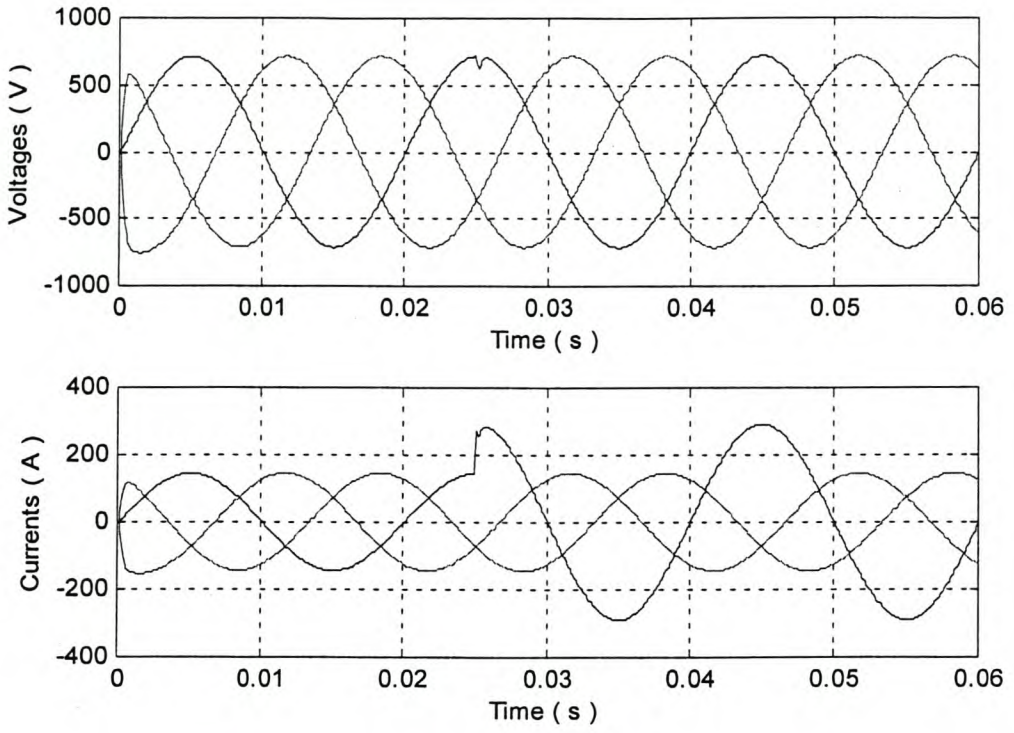


Figure 3-18: Capacitor current feedback voltage control method with an unbalanced load.

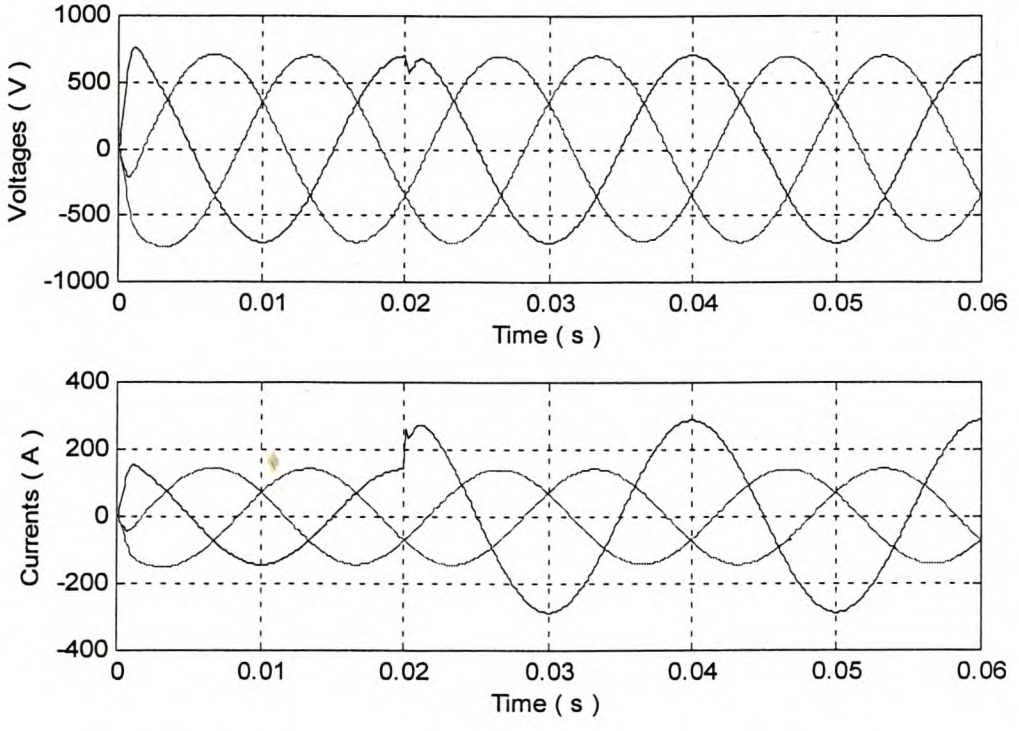


Figure 3-19: Proposed voltage control method with an unbalanced load.

A summary of the three control methods is given in Table 3-2 below. The response time on load steps for the proposed voltage control method is slower than the other two voltage control methods. The total harmonic distortion (THD) of the proposed voltage control method compares well with the current-regulated voltage control method and the capacitor current feedback voltage control method. The unbalance in the three-phase control voltages of the proposed voltage control method also compares well with the other two voltage control methods in Table 3-2. Overall, the proposed voltage control method compares well with the current-regulated and capacitor current feedback control methods.

Table 3-2: Summary of the performance of the control methods.

	Current-regulated controller	**Capacitor current feedback controller**	**Proposed voltage controller**
Initial volt drop for full-load step	283 V (40,43%)	195 V (27.8%)	275 V (39.3%)
Response time for full-load step	0,9 ms	0,8 ms	1,2 ms
THD of control voltages	1,02%	0,99%	0,94%
Voltage unbalance	0,75%	0,18%	0,2%

4 ANALYSIS OF CONTROL METHOD IN DIGITAL DOMAIN

In this chapter the proposed voltage controller of Chapter 3 is evaluated in the digital domain. The detail design of the PID controller is discussed. Simulations are done for load steps and also unbalanced conditions. The proposed voltage control method is also compared to an alternative voltage control method. The system parameters are given in Table 4-1.

Table 4-1: System parameters for 300 kW system.

Parameter	Value	Units
Switching frequency	4	kHz
Nominal DC Bus voltage	800	V
Rated output voltage	230	V_{rms}
Rated output frequency	50	Hz
Rated output power	400	kVA
Rated output current	577	A_{rms}
Filter inductor	500	μH
Inductor resistance	25	mΩ
Filter capacitor	150	μF

4.1 Design of PID controller

The proposed analogue voltage controller of Chapter 3 is of the PID type and is given in the Laplace transform as:

$G_c(s) = K_p + \frac{K_i}{s} + K_d s$, where K_p is the proportional constant, K_i is the integral constant and K_d is the differential constant. Transforming this into the z-domain with a sampling period of T, the transfer function is given by:

$G_c(z) = \frac{z^{-1}(\frac{K_d}{T}) + z(K_p + K_i T + \frac{K_d}{T}) - (K_p + \frac{2K_d}{T})}{z-1}$, where $T = 250\ \mu s$. The block diagram of the digital controller is given in Figure 4-1.

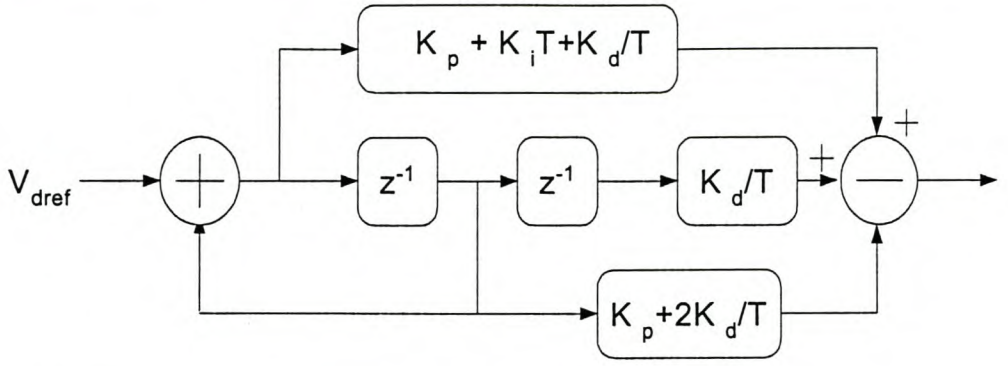


Figure 4-1: Block diagram of PID controller in z-domain.

To get the desired response, the 2nd order closed loop poles of the system described in Figure 3-7 should be dominant. The 2nd order equations are given as follows [21]:

$$t_s = \frac{4}{\delta\omega_n}, \tag{3-13}$$

where $\delta = 0,9$, the damping coefficient, and the settling time, $t_s = 10\text{ms}$. This implies from (3-13) that the natural frequency of the system $\omega_n = 444,4\ \text{rad/s}$.

Further,

$$\omega_d = \sqrt{1-\delta^2} \tag{3-14}$$

$= 193,729\ \text{rad/s}$, where ω_d is the damping frequency of the system. Also

$$\omega_s = \frac{2\pi}{T} \tag{3-15}$$

where ω_s is the sampling frequency and $T = 250\mu\text{s}$, the sampling period. Hence

$\omega_s = 25132,74\ \text{rad/s}$.

The magnitude of the desired closed loop poles are given by:

$$|z| = e^{-\left(\frac{2\pi\delta\omega_d}{\sqrt{1-\delta^2}\omega_s}\right)} \tag{3-16}$$

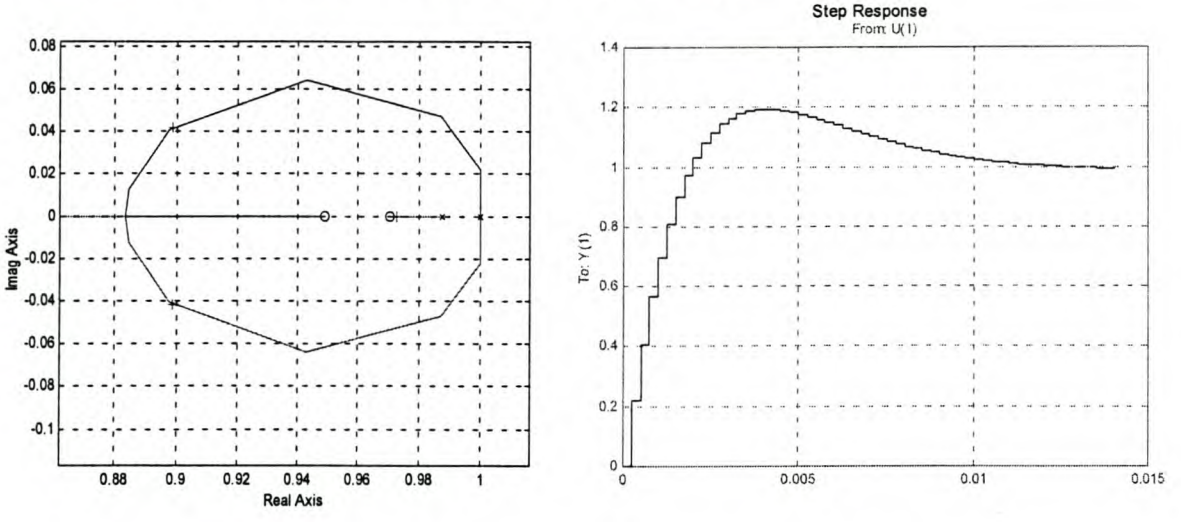
$= 0,90484$.

The angle of the desired closed loop poles can be calculated using the following equation:

$$\angle z = 2\pi\frac{\omega_s}{\omega_d} \tag{3-17}$$

$= 0,0484°$.

This means that the desired closed loop poles lie at $0{,}90378 + j0{,}0438$ for a 10% overshoot and a 10 ms settling time. These calculations are done to get a first idea of where to put the closed loop poles of the system to get the desired response. The root-locus of the open loop system described in Figure 3-7 is given in Figure 4-2 (a) and the closed loop response of the system is given in Figure 4-2 (b).



(a) (b)

Figure 4-2: (a) Root-locus of the digital system. (b) Closed loop digital response.

By choosing the zeros at the desired locations, the closed loop poles can be placed to get the desired response of the system. The position of the zeros causes the closed loop response to have an overshoot of 20%, although it is designed for about 10% overshoot.

To implement the compensation loop digitally in the control system, the inverse of the plant transfer function should be written in the z-transform. The inverse of the LC-filter transfer function with the decoupling terms in the control system is given by:

$G'(s) = \dfrac{1}{LCs^2 + RCs}$, and the inverse transfer function is given by:

$$\frac{1}{G'(s)} = LCs^2 + RCs .$$

Writing this equation in the z-domain becomes:

$\dfrac{1}{G'(z)} = \dfrac{(LC + RCT)z^2 - (2LC + RCT)z + LC}{T^2 z^2}$ with $T = 250\ \mu s$, L the inductance, C the capacitance and R the resistance of the inductor. The compensation loop can easily be implemented in a block diagram and is shown in Figure 4-3.

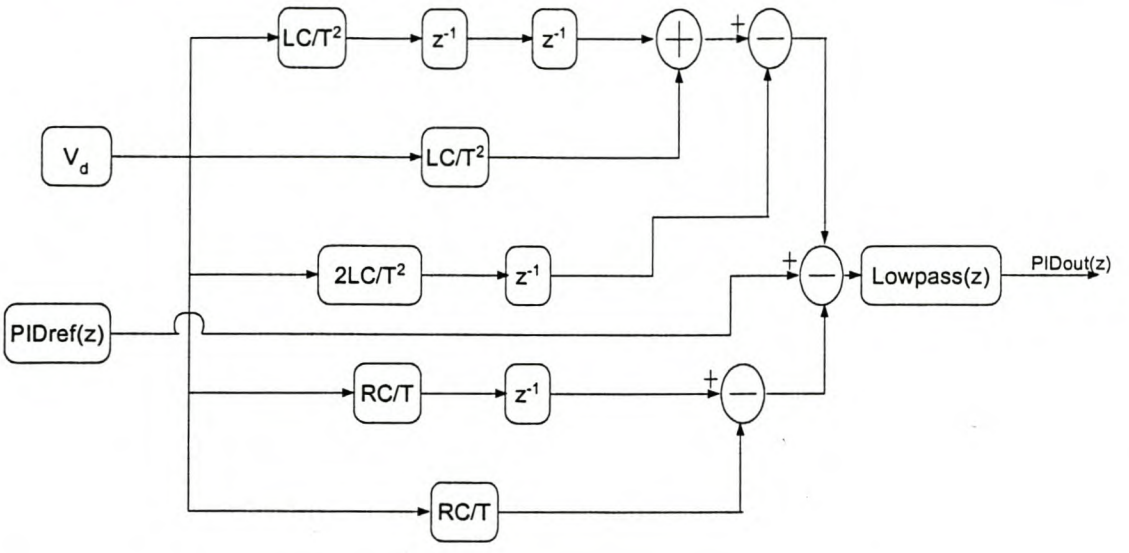


Figure 4-3: Block diagram of the d-axis compensation loop in the z-transform (see also Figure 4-4).

The complete block diagram of the digital controller with compensation and decoupling is given in Figure 4-4. Only the decoupling of the feedback voltages (shown in a bolted line) of the LC-filter is done in the control system.

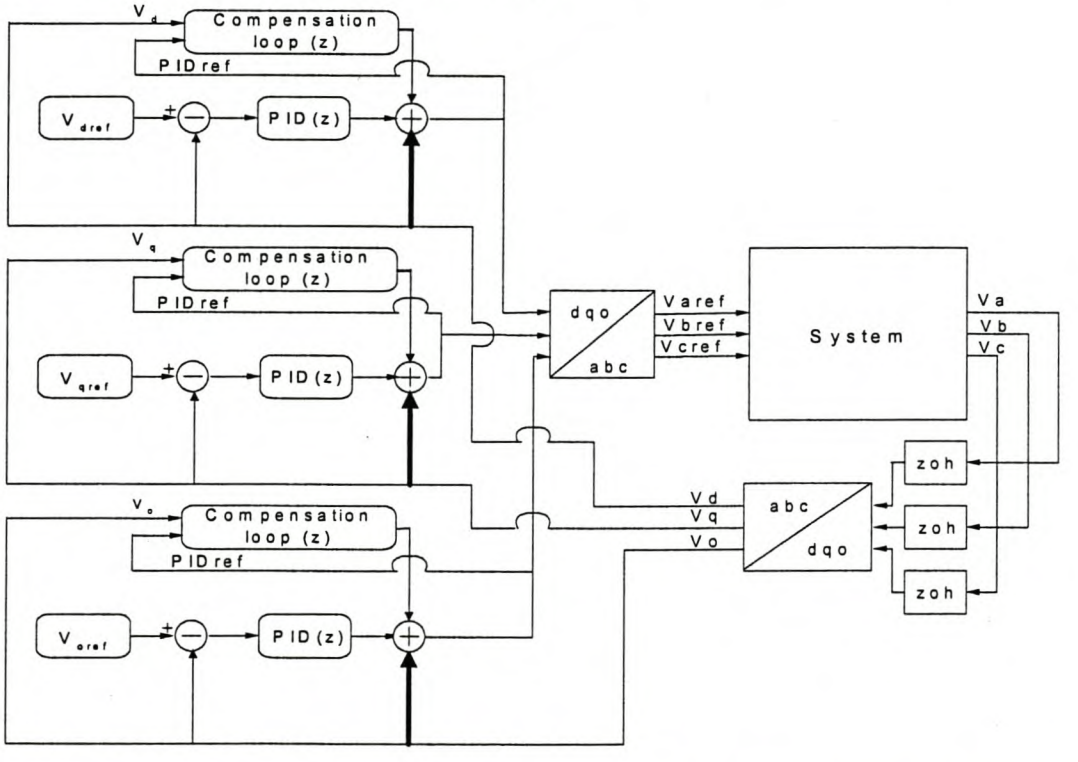


Figure 4-4: Block diagram of the proposed system with digital PID controller and compensation loop.

4.2 Simulation results

The system with the digital PID controller and compensation loop in Figures 4-1 and 4-3 respectively is then simulated with the simulation package SIMUWIN. The d- and q-axis voltage step response of the system with a sampling period of 250 μs is shown in Figure 4-5 and the no-load - and full-load steady state three-phase voltages in Figure 4-6.

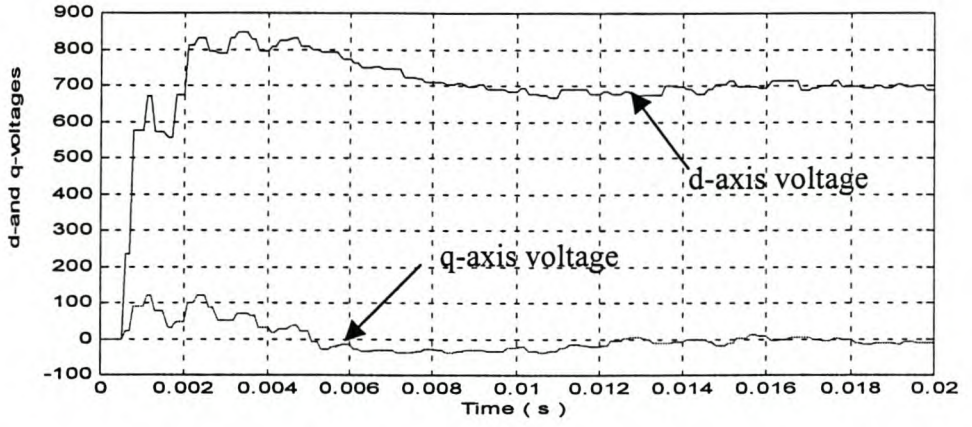


Figure 4-5: Simulated d- and q-axis voltage response of the digital system with d-axis step voltage of 700 V.

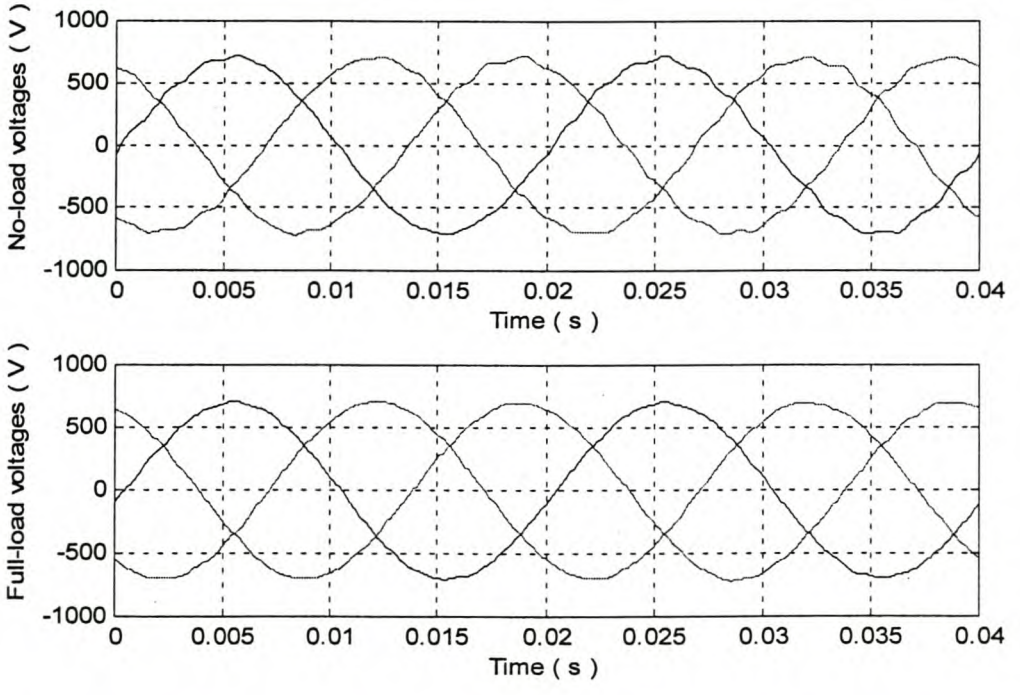


Figure 4-6: Simulated no-load – and full-load control voltages of the system with digital controller and compensation loop in the steady state.

The total harmonic distortion (THD) is calculated using the MATLAB program as given in Appendix E. The THD of the no-load voltages are calculated to be 2,06% and the THD of the full-load voltages as 1,03%. The system is very lightly damped at no-load as the resistance of the inductor is very small. The resistance is estimated as 0,025 Ω. When full-load current is drawn, the system is more damped and therefore the THD at full-load is less than the THD at no-load.

4.2.1 Effect of sampling period on decoupling

Before the effects of load steps on the response of the system are investigated, the effect of the sampling period on the decoupling terms, without the compensation technique, is going to be discussed. PID controllers were designed for the same response (10 ms settling time, and 10% overshoot), but with different sampling periods. The PID controllers were designed to only react on the LC-part as shown in Figure 3-7 and the decoupling of the d- and q-axis voltages and currents is established by adding or subtracting the d- and q-axis coupling terms in the control system in Figure 3-6. The different controllers were simulated with SIMUWIN and the results are shown in Figure 4-7.

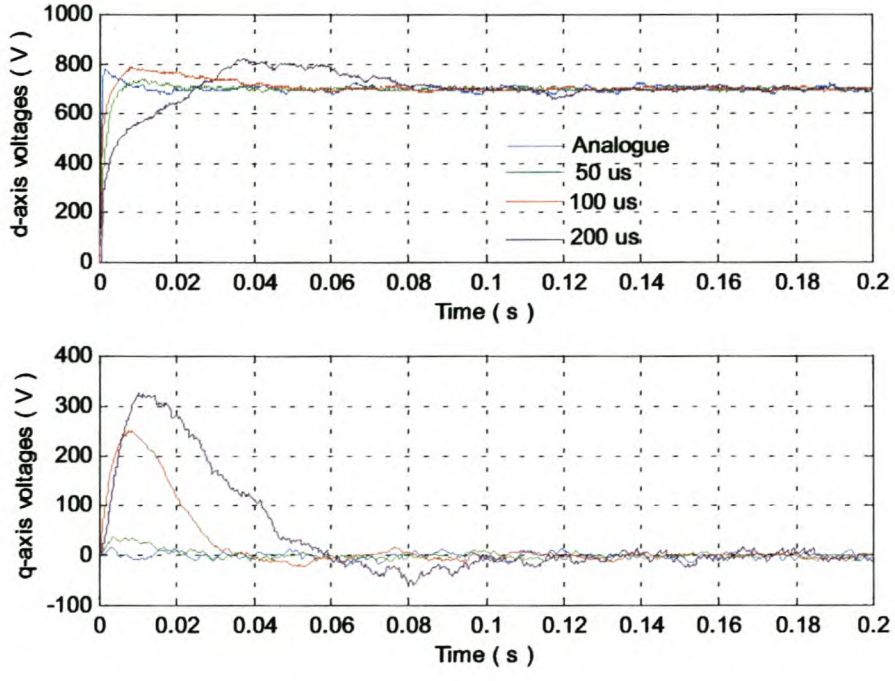


Figure 4-7: Simulated d- and q-axis voltage response with sampling periods as a parameter.

It can be seen from Figure 4-7 that the sampling period has a significant effect on the d- and q-axis voltage responses. The responses of the d- and q-axis voltages for a voltage step input with a 200 μs sampling period, is much slower than the analogue response. By sampling, thus, at 200 μs decoupling of the d- and q-axis voltages and currents is not perfect. The PID controller therefore sees the coupling voltage and current terms as disturbances and tries to compensate for it, but it was not designed for this. With the analogue simulation, which represents an infinite short sampling period, the decoupling of the d- and q-axis circuits are complete and the controller exhibits the designed response for a step input voltage. Therefore, as the sampling period is increased, the decoupling of the d- and q-axis voltages and currents are more established, and the controller then only reacts on the LC-part as designed for as shown in Figure 3-7.

The above also has a significant effect when load steps are applied. The PID controller designed for longer sampling periods, will react slower on load steps than a controller designed for much shorter (50 μs) sampling periods. Therefore, ideally one would have a high as possible sampling frequency for the controller to react dynamically on load steps.

With the actual implementation of the digital PID controller in this application, the sampling period was limited by the control loop-time, which is 250 μs. This means a sampling period of 250 μs is chosen to synchronise with the control loop-time. The sampling period of 250 μs was found to be sufficient, as the compensation loop of section 3.3 in the control system compensates for the coupling terms and completely decouples the d- and q-axis circuits, and gives the response that was designed for. With the simulations shown in Figure 4-7 and the discussions in the previous paragraphs it is shown that, although a much faster sampling period is preferred which decouples the d- and q-axis circuits, hence getting a faster dynamic response of a system, a much slower sampling period can also be used, together with the compensation loop to achieve the same dynamic performance in a system (shown in Figure 4-5). A case study is done in section 4.4 to show the response of the power supply system when a 100 μs sampling period is used in the control loop of the system.

4.2.2 Load steps

A positive and negative full-load step, as defined in section 3.4, was applied to the system and the results obtained are shown in Figure 4-8 and Figure 4-9. The proposed voltage control method with a PID controller and compensation loop as shown in Figure 4-4 is used in the simulations. The sampling period was taken as 250 μs.

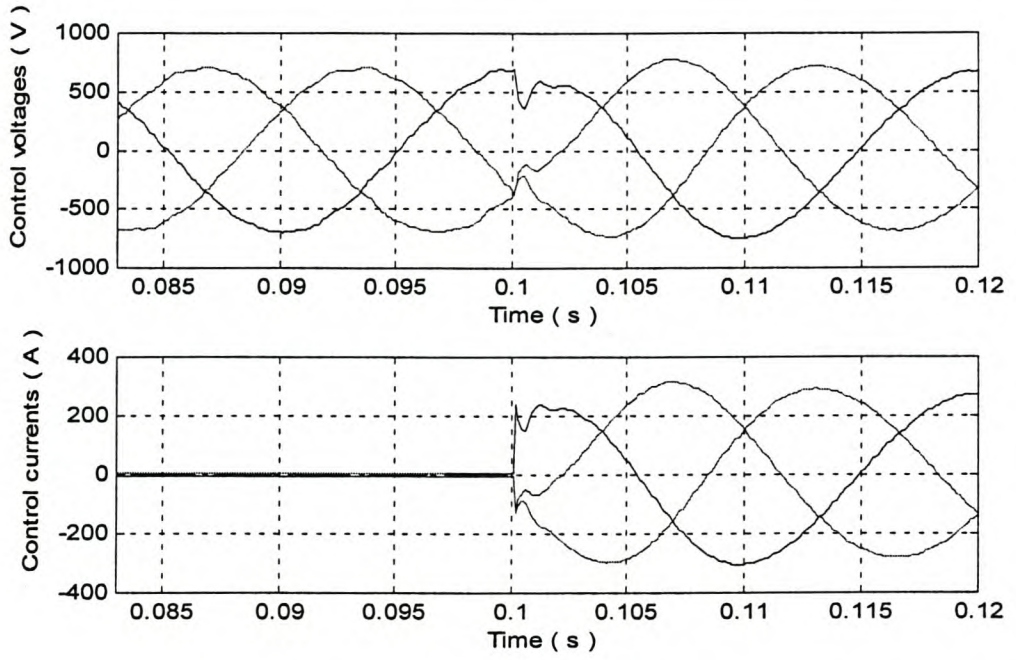


Figure 4-8: Simulated control voltages and currents for a positive full-load step with the proposed voltage control method (see Figure 4-4).

The initial voltage drop is 350V (50%) and the controller reacts within 2 ms to bring the output voltage within 5% of the reference voltage (700 V). The output voltage becomes stable after 10 ms. A negative full-load step is then applied to the system and the results are shown in Figure 4-9.

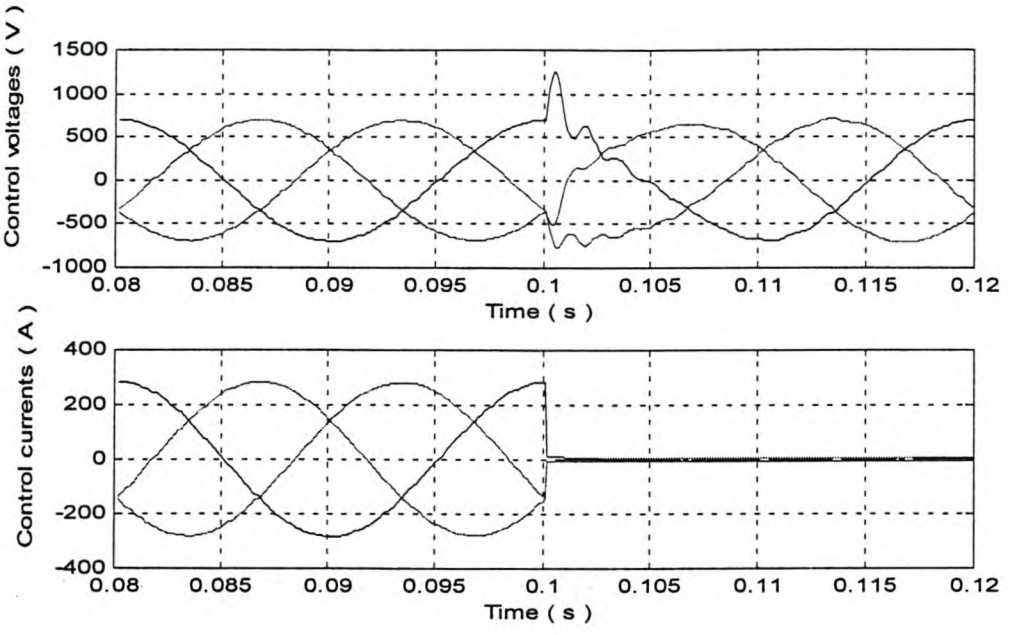


Figure 4-9: Simulated control voltages and currents for a negative full-load step with the proposed voltage control method.

When the load is disconnected, it caused an overshoot in the output voltage. This is because of the energy stored in the inductor, and the controller cannot react fast enough to prevent the overshoot in the control voltages. The output voltage rises to over a 1000 V, that is more than 40% above the reference voltage, but the controller stabilises the control voltage within 1 ms. The d- and q-axis voltage responses are shown in Figure 4-10 and 4-11.

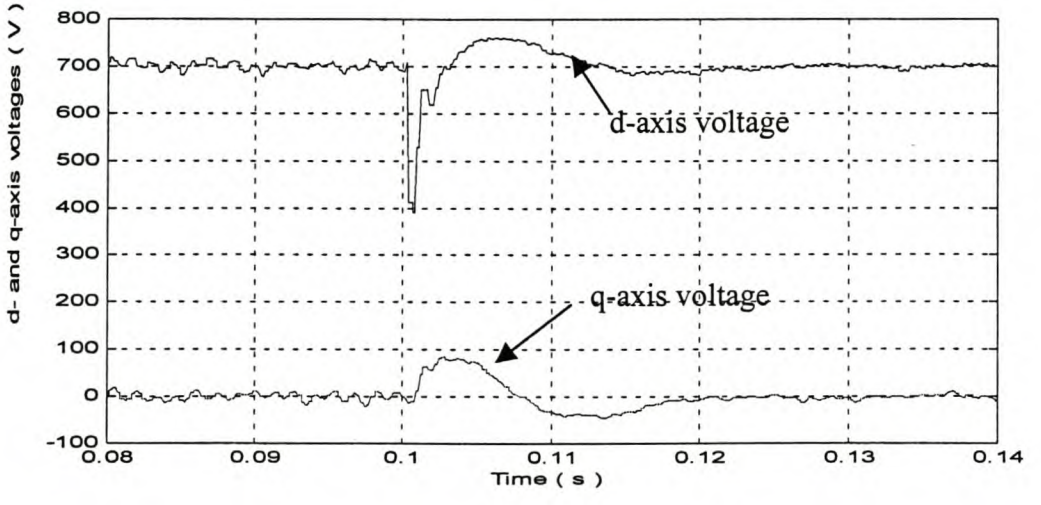


Figure 4-10: Simulated d- and q-axis voltages for a positive full-load step with the proposed voltage control method.

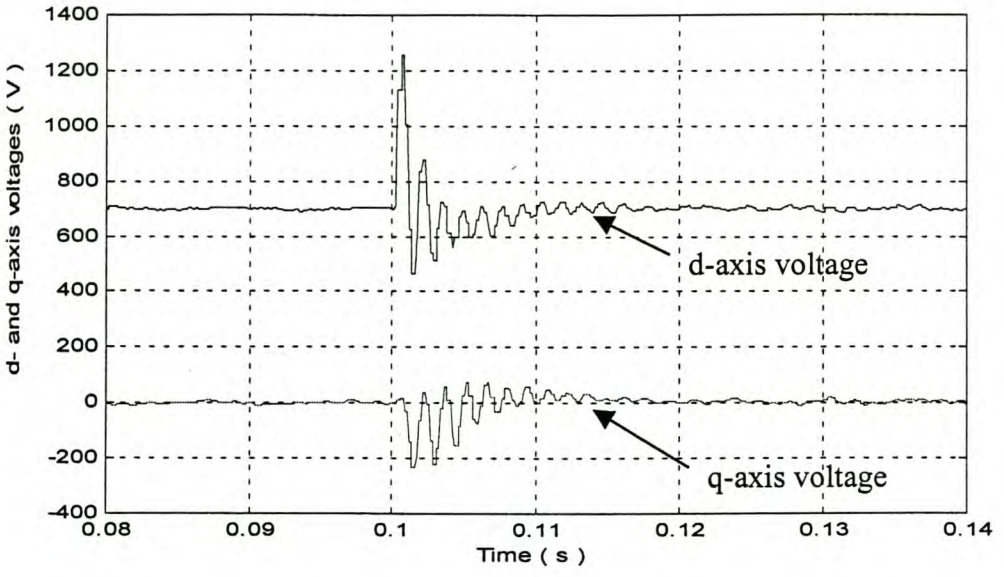


Figure 4-11: Simulated d- and q-axis voltages for a negative full-load step with the proposed voltage control method.

When a positive load step is applied to the system, it causes a significant dip in the d-axis voltage. The controller reacts very fast and brings the control voltages within 5% of the reference voltage in just over 3 ms. The d-axis voltage then shows a 10% overshoot and stabilises in about 12 ms. When the load is disconnected from the system, a high overshoot is caused in the d-axis voltage that reflects the overshoot in the three-phase voltages of Figure 4-9. The oscillations occur due to the now highly undamped system. The controller stabilises the system voltage within 10 ms.

4.2.3 Unbalanced conditions

The proposed voltage control method is also simulated under unbalanced conditions, which represent a single-phase load connected to the three-phase supply. The system is started up at half the full-load current on all three phases, and then full-load current is drawn from phase *a*. The d- and q-axis voltages are shown in Figure 4-12 and the three-phase voltages are shown in Figure 4-13. Again, a sampling period of 250 μs is used in the simulations. The compensation loop with the PID controller designed as described in section 4.1 are used.

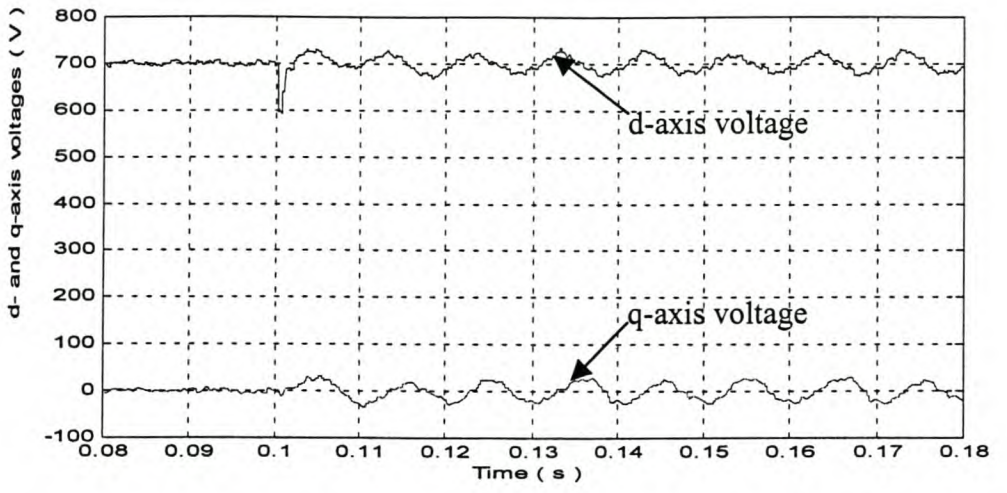


Figure 4-12: Simulated d- and q-axis voltages for an unbalanced load with the proposed voltage control method.

The single-phase load is connected at the time equal to 100 ms. The d- and q-axis voltages have a 100 Hz component when the load is drawing unbalanced currents as is shown in Figure 4-12. It is clear that the controller cannot fully compensate for the unbalance that is caused when a single-phase load is applied to the supply. The unbalance in the three-phase voltages is calculated according equation 3-12 as 2% using the MATLAB program given in Appendix F. This is within the limits of the NRS 048 standards given in Table 3-1. Figure 4-13 shows the effect the single-phase load has on the three-phase control voltages and currents.

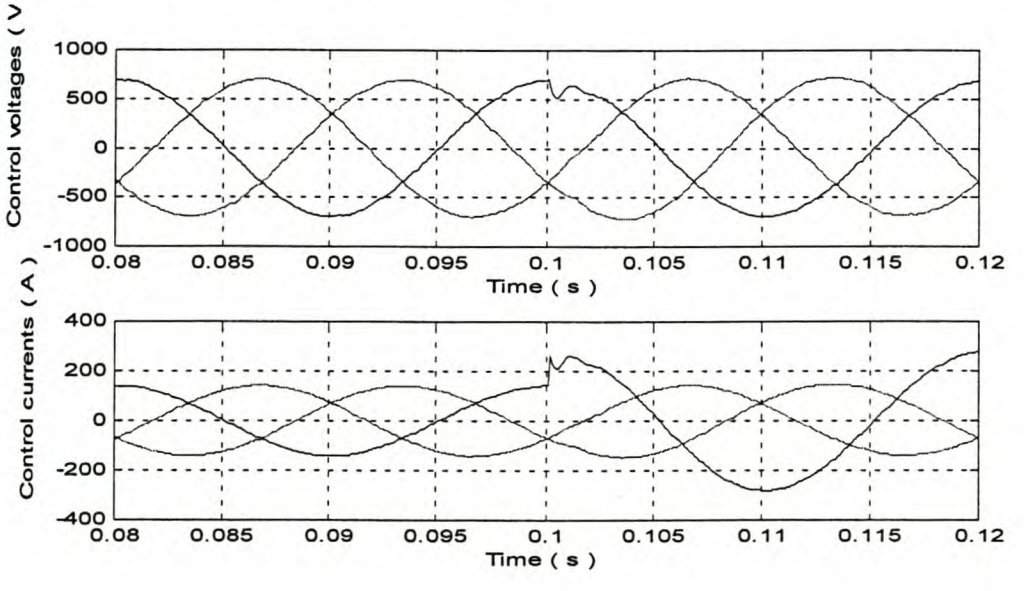


Figure 4-13: Simulated control voltages for an unbalanced load with the proposed voltage control method.

4.2.4 *Effect of different power factor loads*

All the above simulation results showed the voltages and currents of the primary side of the transformer, which is defined as the **control** voltages. The **supply** voltages of the secondary side of the transformer with different power factor loads are shown in the following Figures. Figure 4-14 shows the supply voltages and currents of the system with only a resistive load. Figure 4-15 shows the supply voltages and currents for a 0,8 power factor load.

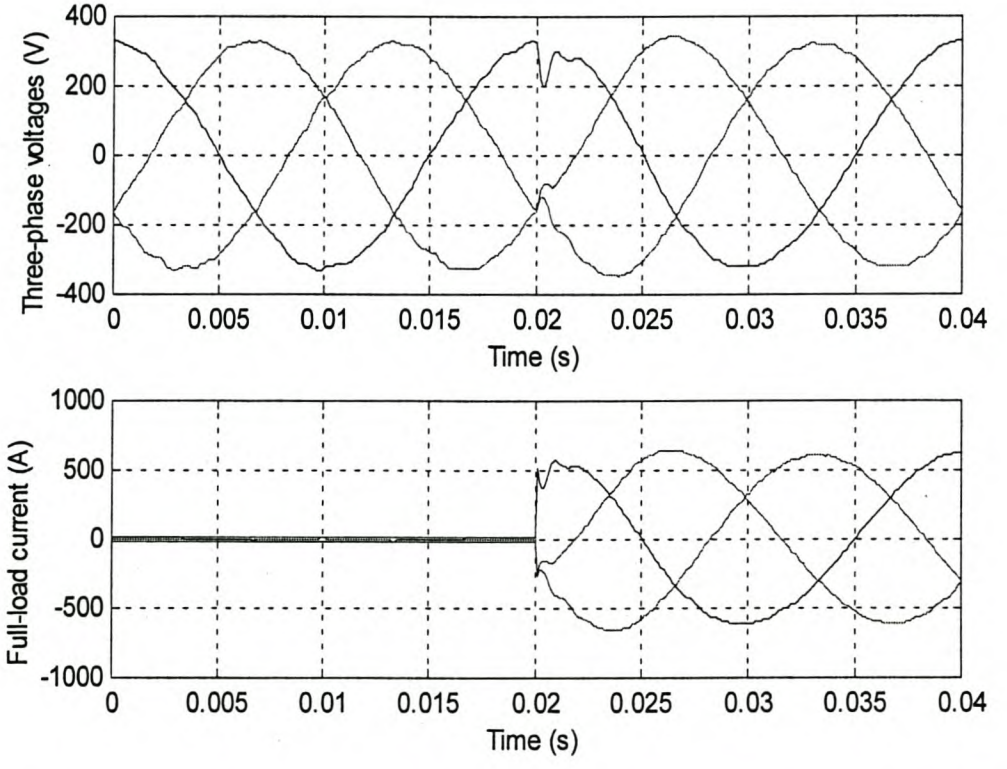


Figure 4-14: Simulated supply voltages and currents with a resistive load with the proposed voltage control method.

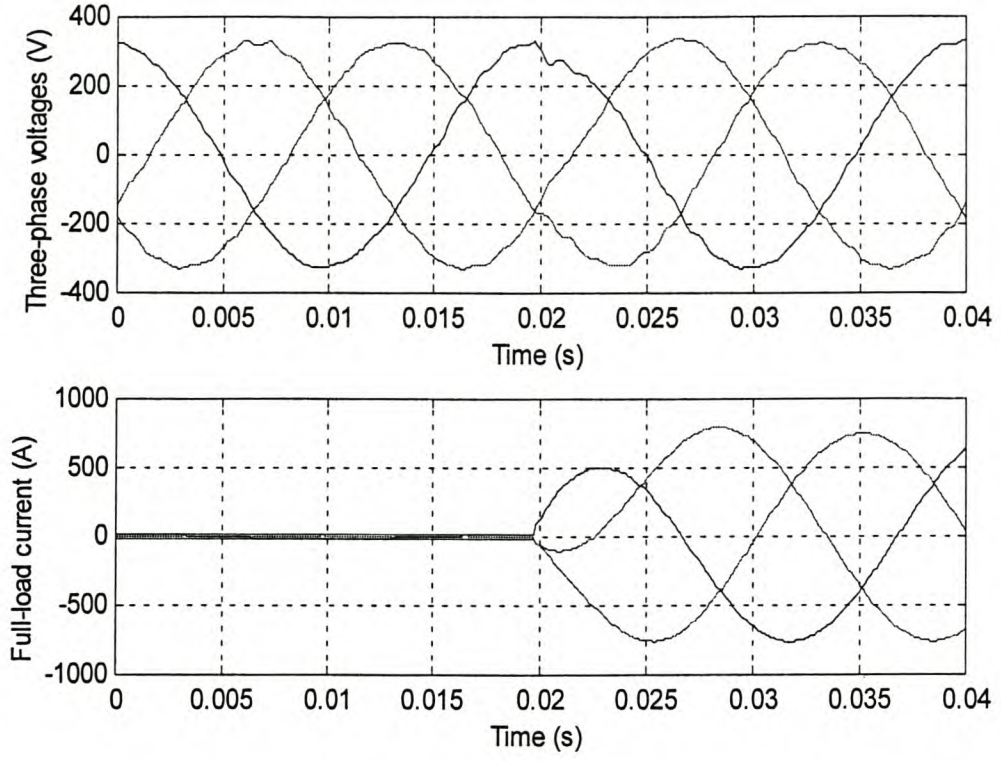


Figure 4-15: Simulated supply voltages and currents for a 0,8 power factor load with the proposed voltage control method.

From Figure 4-15 the response to a full-load current step has a much smoother effect on the three-phase voltages than the response with only a resistive load. The supply voltages show little effect when a full-load current step is applied at the peak voltage of phase *a*.

4.3 Alternative voltage control method

A voltage control method is investigated by [15] and is evaluated in the digital domain. In this thesis, it is called the alternative voltage control method. Instead of using the proposed decoupling feedback control method, where the feedback voltage (v_d and v_q) of the LC-filter (see Figure 3-3) is not included in the PID controller design, the controller is designed with the feedback voltages (v_d and v_q) included in the controller design. The control block diagram of this is shown in Figure 4-16.

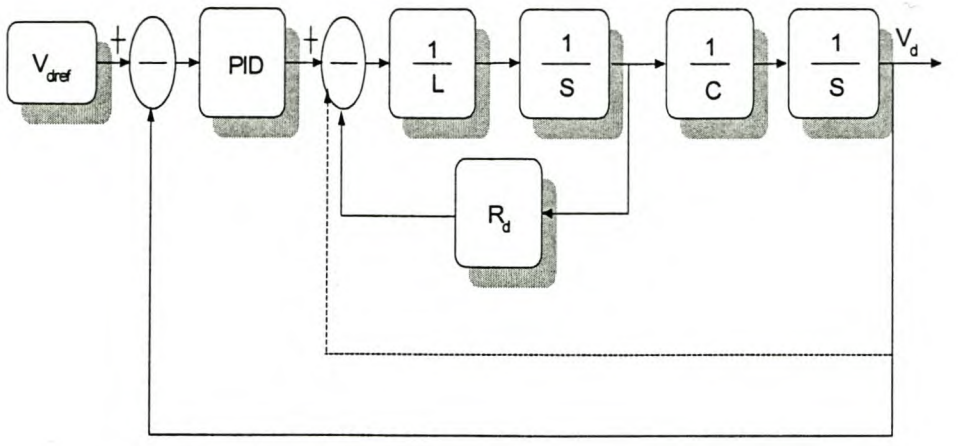


Figure 4-16: Block diagram of the alternative voltage control method.

With the decoupling feedback control method discussed in section 3.2, the feedback voltage (dashed line) is not part of the control block diagram (see Figure 3-7). The feedback voltages (v_d and v_q) can be seen as the back-emf voltage of the LC-filter. The alternative voltage control method includes the feedback voltages (v_d and v_q) as part of the control block diagram. The ωLi_{dq} and ωCv_{dq} terms shown in Figure 3-3 were ignored in the control system as it was found from simulations that these coupling terms have little effect on the designed response of the PID controller. A block diagram of the power supply system with the alternative voltage control method is shown in Figure 4-17.

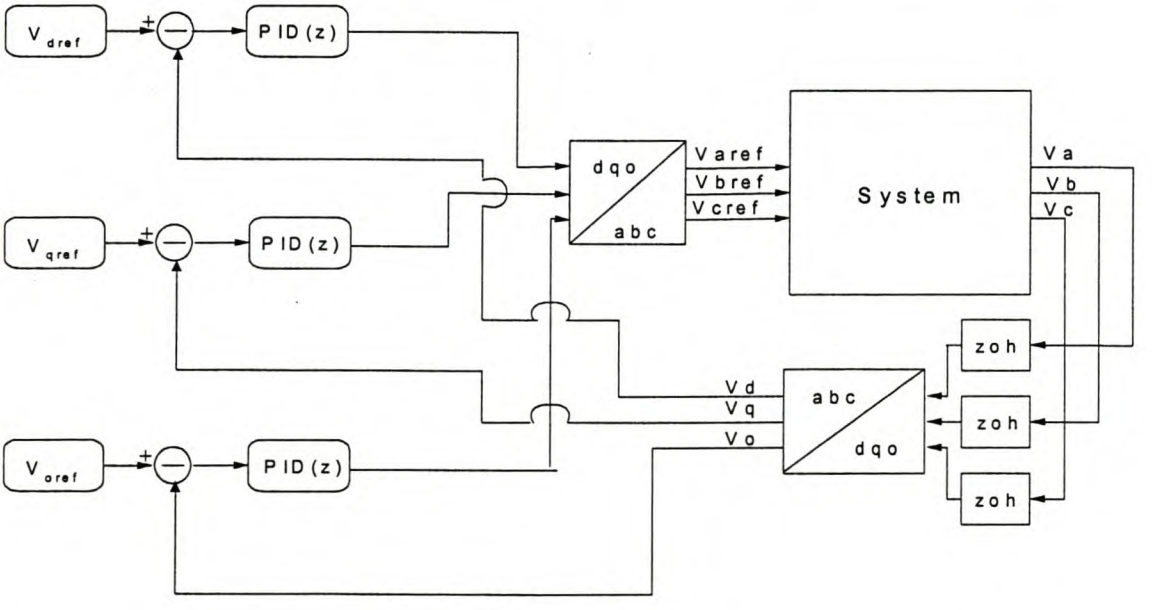


Figure 4-17: Block diagram of power supply system with alternative voltage control method.

When the feedback voltage is included in the control block diagram, the system has complex poles. A PID controller is designed for the system using the root-locus method. The controller is designed for a 100 ms critically damped response. The Matlab program is given in Appendix C3. The root-locus is shown in Figure 4-18.

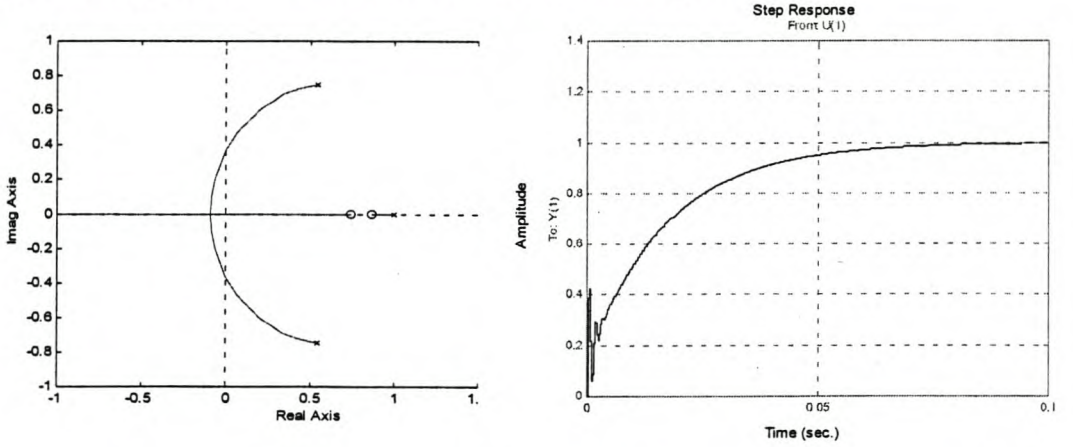


Figure 4-18: Diagram of the root-locus and step response of alternative voltage control method with a d-axis step input voltage.

By choosing the closed loop poles, one can get the desired response of the system. The step response of the system is shown in Figure 4-18. The ossilations in the step response is due to the weakly damped poles of the system.

Simulations were done with Simuwin and the following results are obtained shown in Figure 4-19. First, simulations are shown of the step response of the system. Then positive and negative load steps are applied to the system to observe the system's performance. Only resistive loads are considered in evaluating the system.

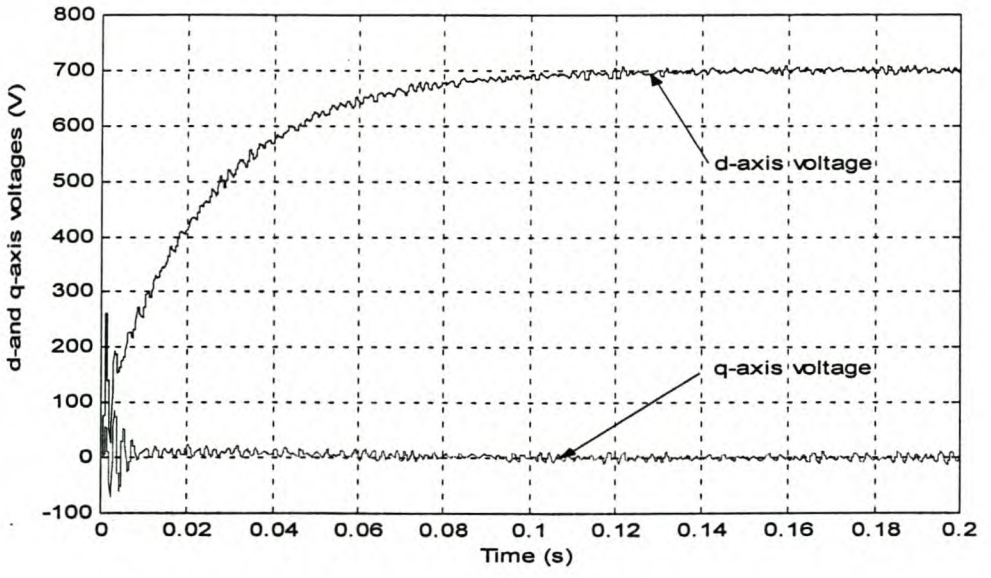


Figure 4-19: Simulated d- and q-axis step responses with alternative voltage control method.

The controller is designed for a 100 ms critically damped response and when simulated, it corresponds well with the designed response in Figure 4-18. Again, because of the feedback voltage in the control block diagram of the controller, the controller exhibits some initial oscillations. Another reason for the lightly damped system, especially under no-load conditions, is that the resistance of the inductor is very small, about 25 mΩ. As the step response is not a very important design aspect, these initial oscillations are considered as not important. The important issue, however, is the response of the controller when load steps are applied to the system.

First, the no-load and full-load voltages are shown in Figure 4-20 below. It can be seen that the no-load voltages are significantly more distorted than the full-load voltages. When full-load current is flowing, the system becomes more damped and therefore the full-load voltages will have fewer harmonic. The total harmonic distortion (THD) in the no-load voltages is calculated to be 1,8% and the THD of the full-load voltages is calculated to be 1,02%. These calculations of the THD are well within the specified limit of 8%.

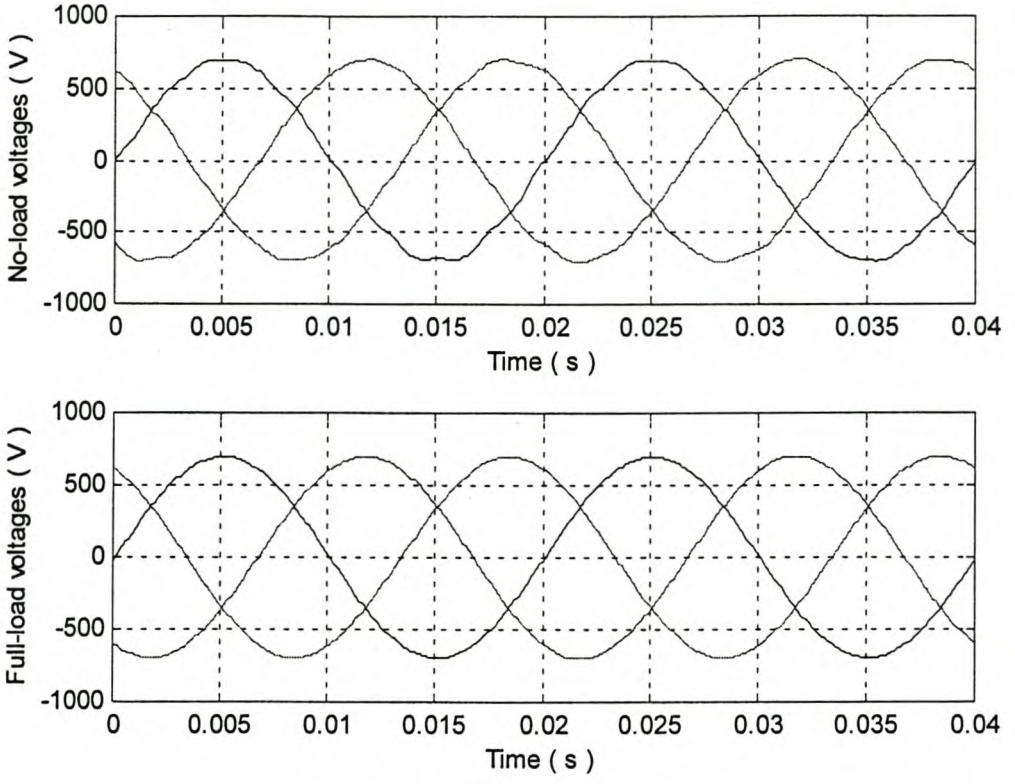


Figure 4-20: Simulated no-load and full-load control voltages of the system with alternative voltage control method.

4.3.1 Load steps

Load steps are applied to the system to evaluate the system's performance under various load conditions. Positive-and negative load steps are applied to the system, and the results are shown in Figure 4-21 and 4-22. The effect of the load steps on the voltages can also be seen in the d- and q-axis voltages. This is shown in Figures 4-23 and 4-24.

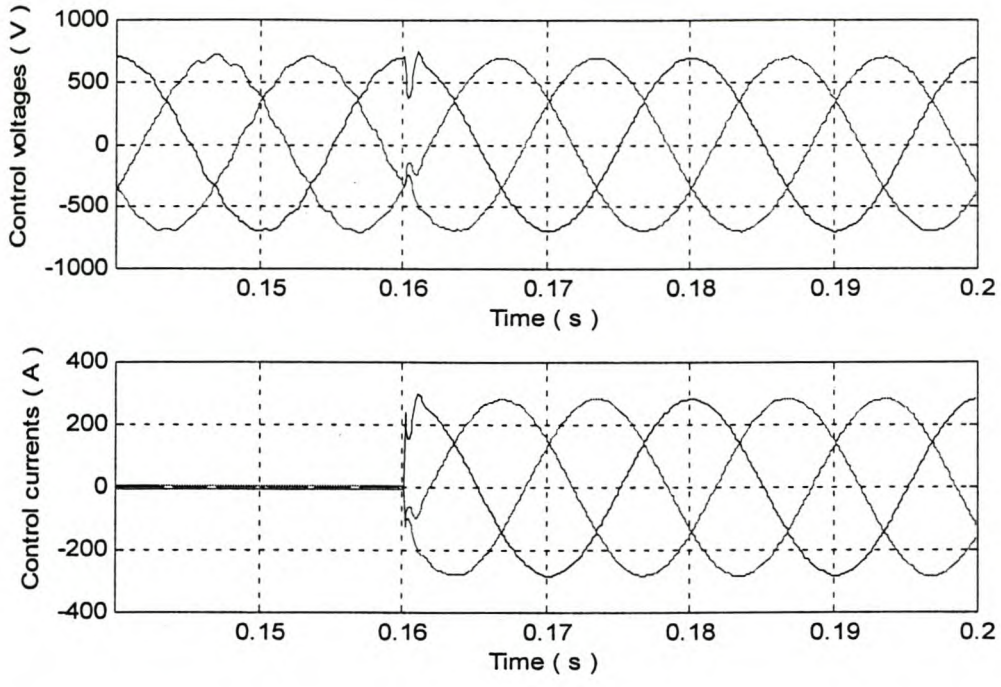


Figure 4-21: Simulated response with alternative voltage controller for a positive full-load step with a resistive load.

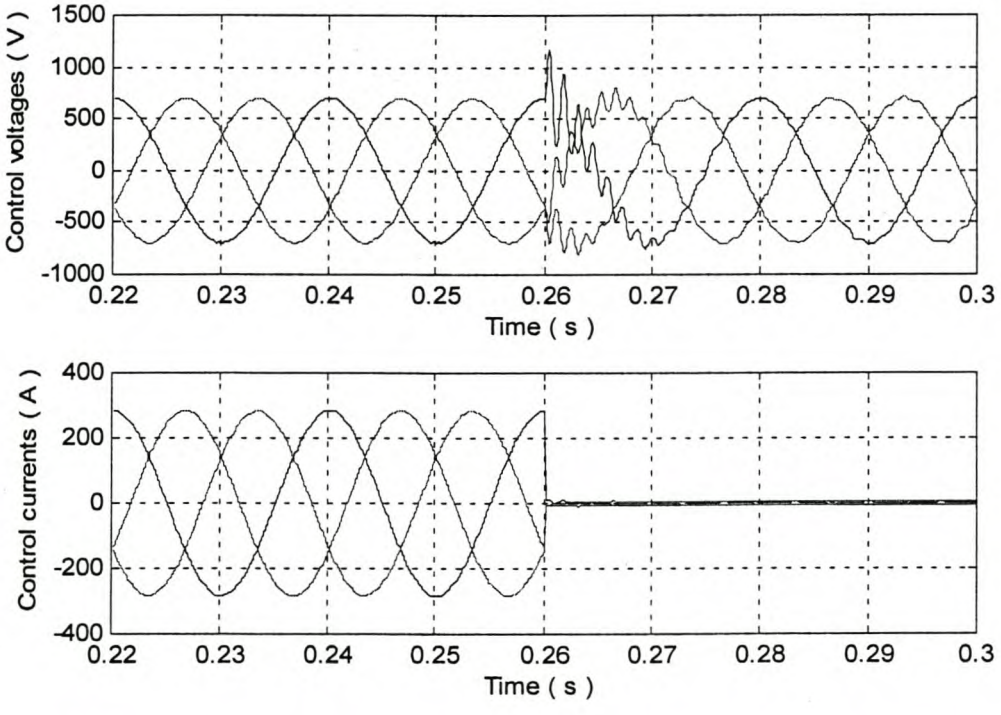


Figure 4-22: Simulated response with alternative voltage controller for a negative full-load step with a resistive load..

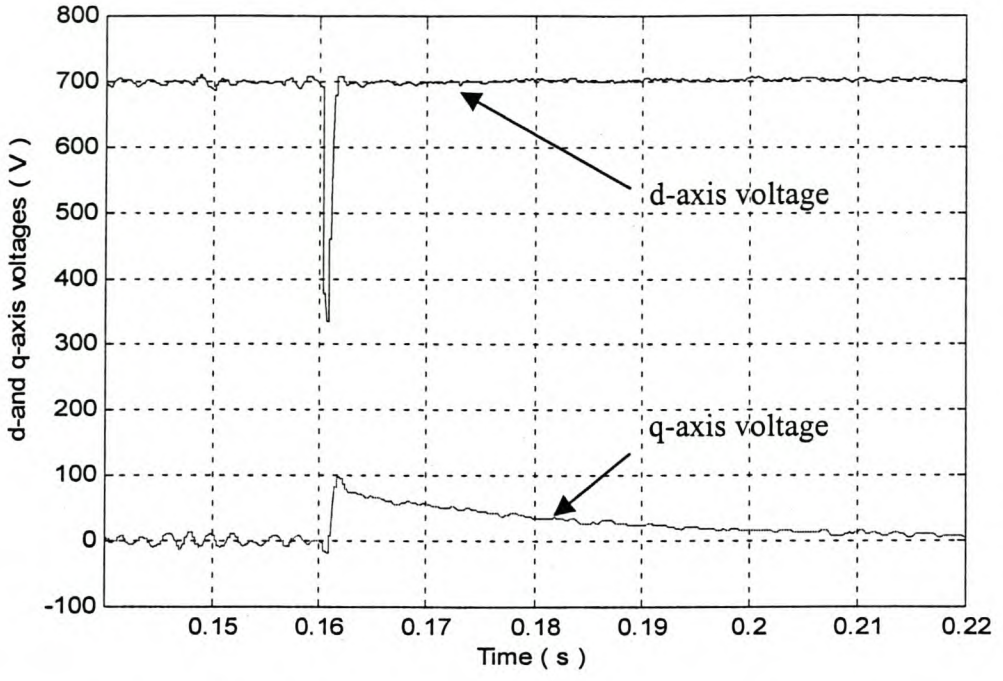


Figure 4-23: Simulated d- and q-axis voltages with a positive resistive load (alternative voltage control method).

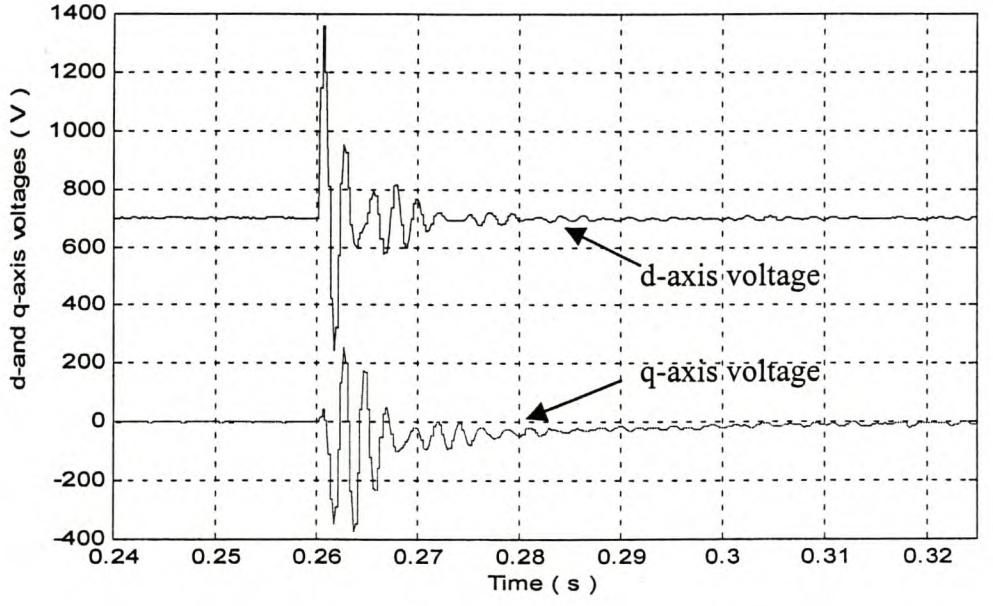


Figure 4-24: Simulated d- and q-axis voltages with a negative resistive load step (alternative voltage control method).

At a positive full-load step, the voltage drops to 335 V (Figure 4-21), that is nearly 50%. The controller, however, restores the voltage within 1,5 ms. From Figure 4-21, when the

full-load step is applied, the current in phase *a* rises instantly. This causes the huge voltage drop in the phase *a* voltage. The voltage drop would be considerably less in loads with a power factor less than 1. When a negative full-load step is applied, the voltage has an overshoot of nearly twice the control voltage. The controller stabilizes the control voltage within 10 ms. Again the load is switched out of the system when the current in phase *a* is a maximum, causing a high voltage overshoot, especially in the phase *a* voltage.

The performance of the alternative voltage control method is also simulated with a 0,8 power factor load step. The results for positive and negative full-load steps are shown in Figure 4-25 and 4-26 respectively. The responses of the d- and q-axis voltages are shown in Figure 4-27 and 4-28.

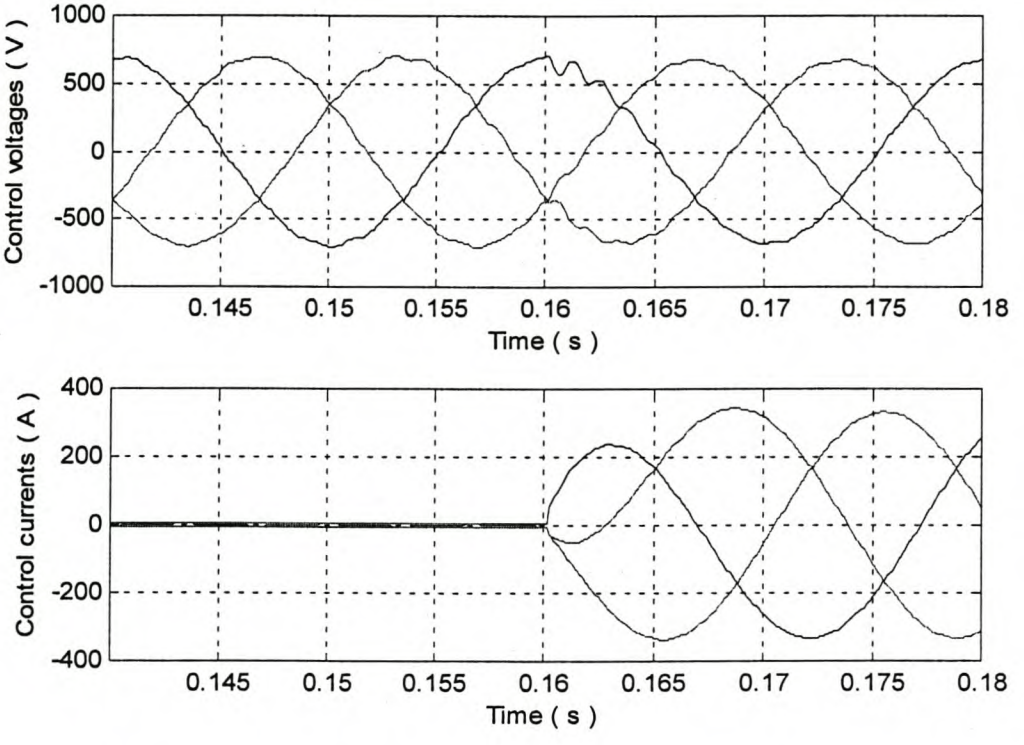


Figure 4-25: Control voltages for a positive full-load current load step.

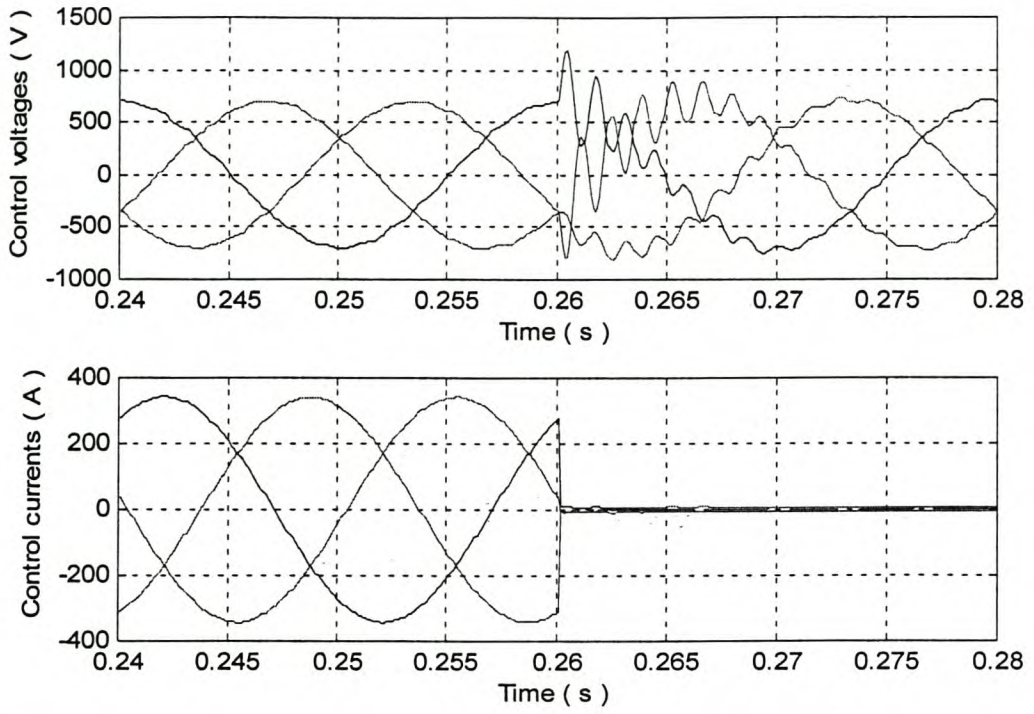


Figure 4-26: Control voltages for a negative full-load current step.

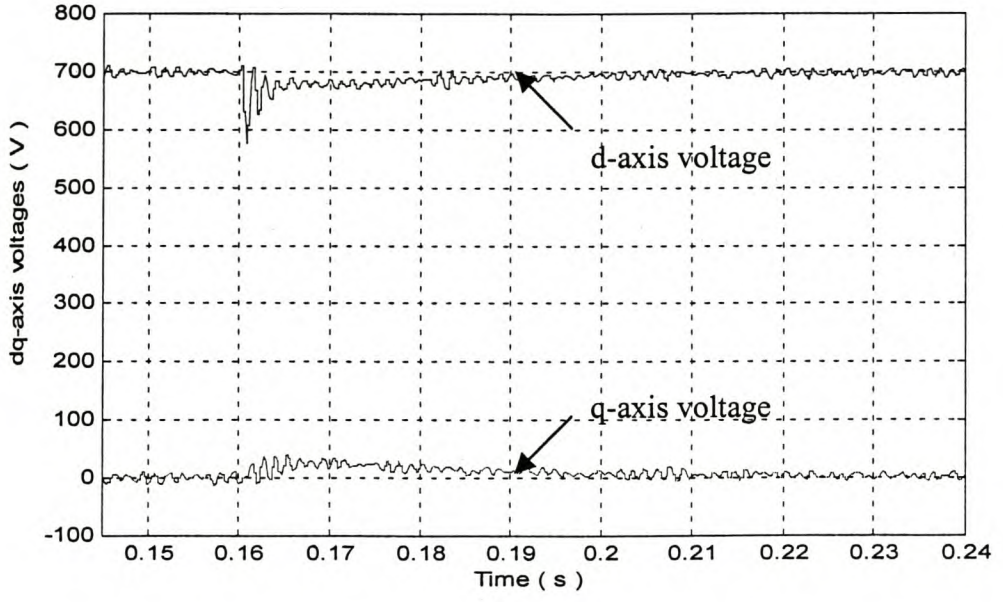


Figure 4-27: Simulated responses of d- and q-axis voltages response with a positive 0,8 power factor load step (alternative voltage control method).

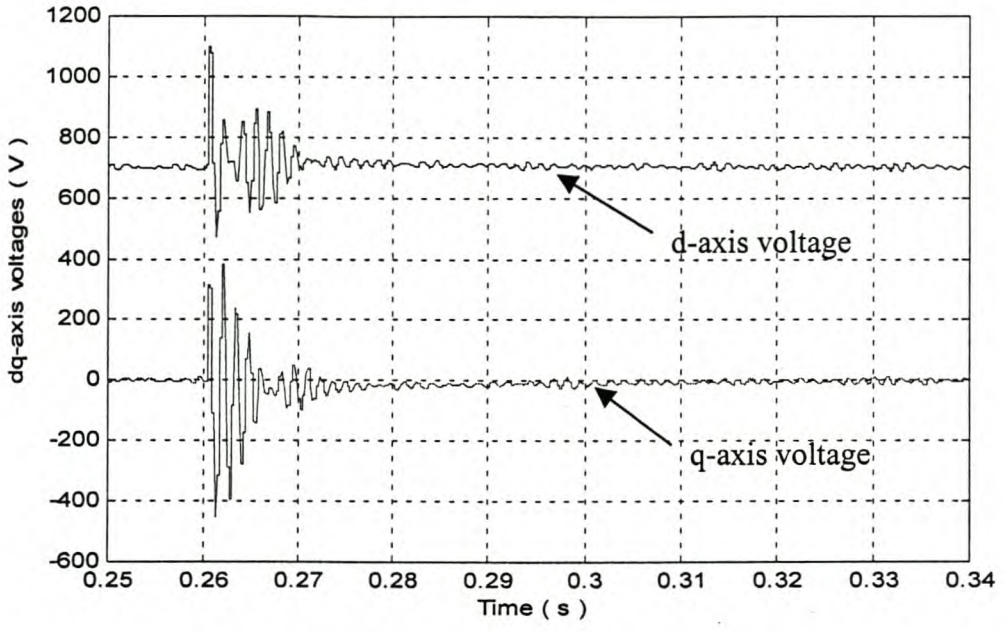


Figure 4-28: Simulated responses of d- and q-axis voltages response with a negative 0,8 power factor load step (alternative voltage control method).

As can be seen from Figures 4-25 and 4-27, the voltage dip with a 0,8 power factor load step is less than with a resistive load step shown in Figure 4-22 and Figure 4-24. However, with the 0,8 power factor load switched off, the voltage overshoots and oscillations are the same as in Figure 4-26 and 4-28, as is expected.

The alternative voltage control method is also verified with a practical evaluation on a laboratory set-up. This is shown and discussed in chapter 6.

4.4 A case study

Much attention is given in the previous sections about (i) the effect of the sampling period on the decoupling of the d- and q-axis circuits and (ii) the effect of the load steps on the response of the system. A fixed-point Digital Signal Processor (DSP) is practically used (see Chapter 5), and due to all the calculations, the control loop-time could only be minimised to 250 μs. With a floating-point DSP, the sampling period could be much less than 250 μs. A simulation case study is done with a sampling period of 100 μs to see what responses can be obtained if a floating-point DSP is used. The digital controller is designed for 100 μs sampling period. The proposed voltage controller with the decoupling feedback control and compensation loop (see Figure 4-4)

was used in the case study simulation. The switching frequency is kept constant at 4 kHz. Simulations are done with positive and negative load steps with a resistive load and also with a 0,8 power factor load. The voltage and current responses are shown in Figures 4-29 and 4-30 for a positive load step and Figures 4-31 and 4-32 for a negative load step. The d- and q-axis voltage responses are given in Figures 4-33 and 4-34 for a positive load step and Figures 4-35 and 4-36 for a negative load step.

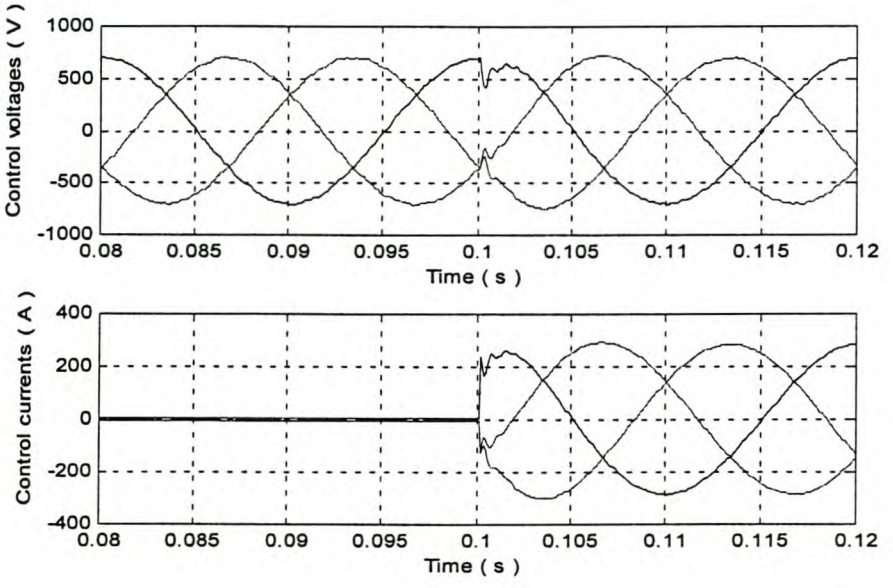


Figure 4-29: Simulated control voltages and currents for a positive full-load step with 100 μs sampling period and resistive load.

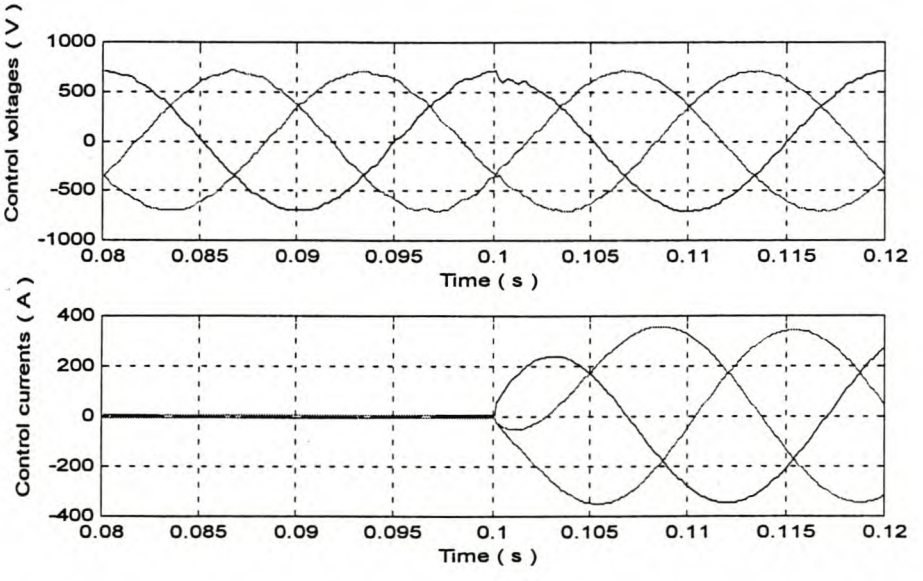


Figure 4-30: Simulated control voltages and currents for a positive full-load step with 100 μs sampling period and 0,8 power factor load.

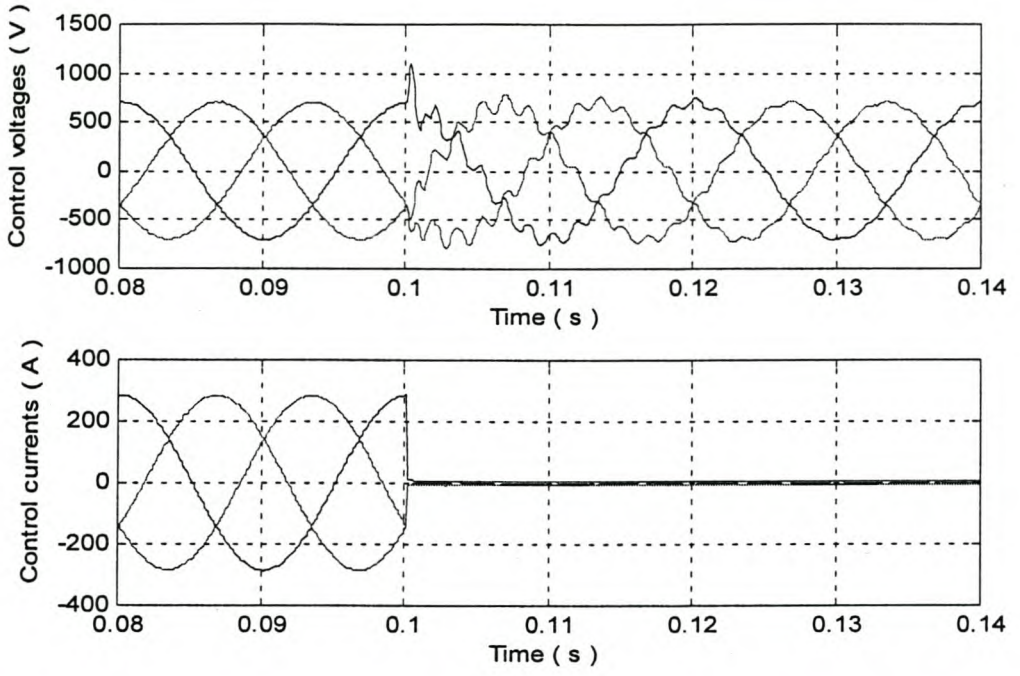


Figure 4-31: Simulated control voltages and currents for a negative full-load step with 100 μs sampling period and resistive load.

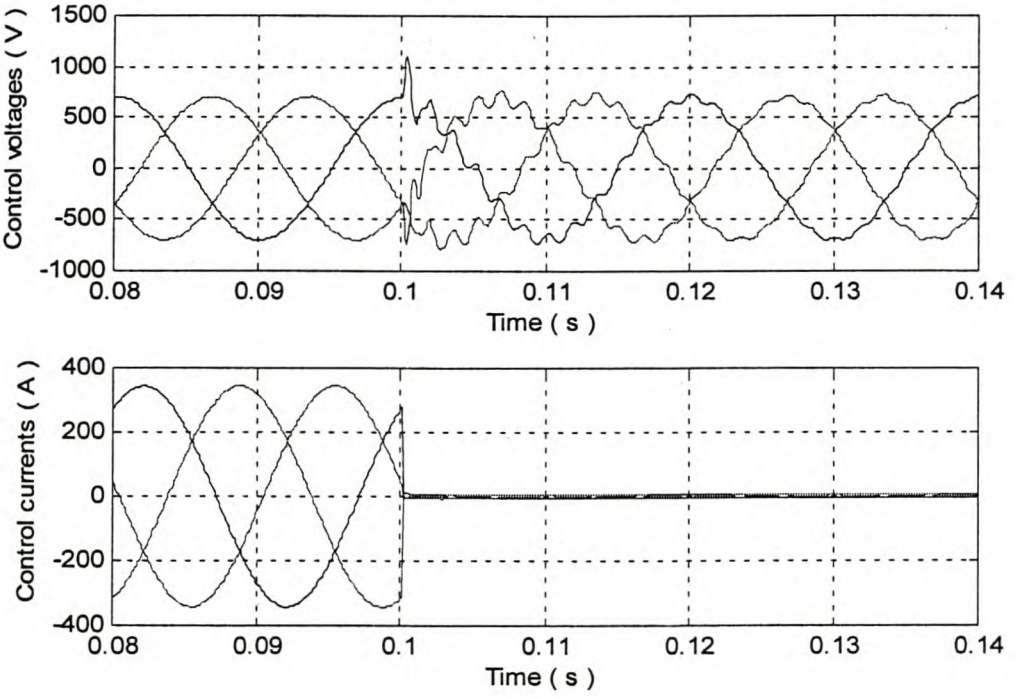


Figure 4-32: Simulated control voltages and currents for a negative full-load step with 100 μs sampling period and 0,8 power factor load.

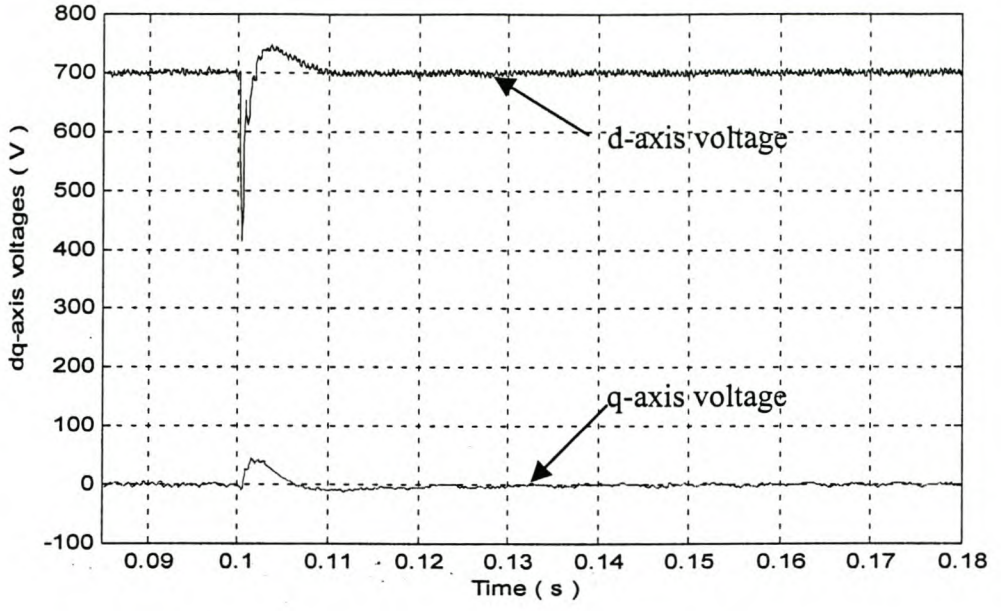


Figure 4-33: Simulated d- and q-axis voltage responses for a positive full-load step with 100 μs sampling period and resistive load.

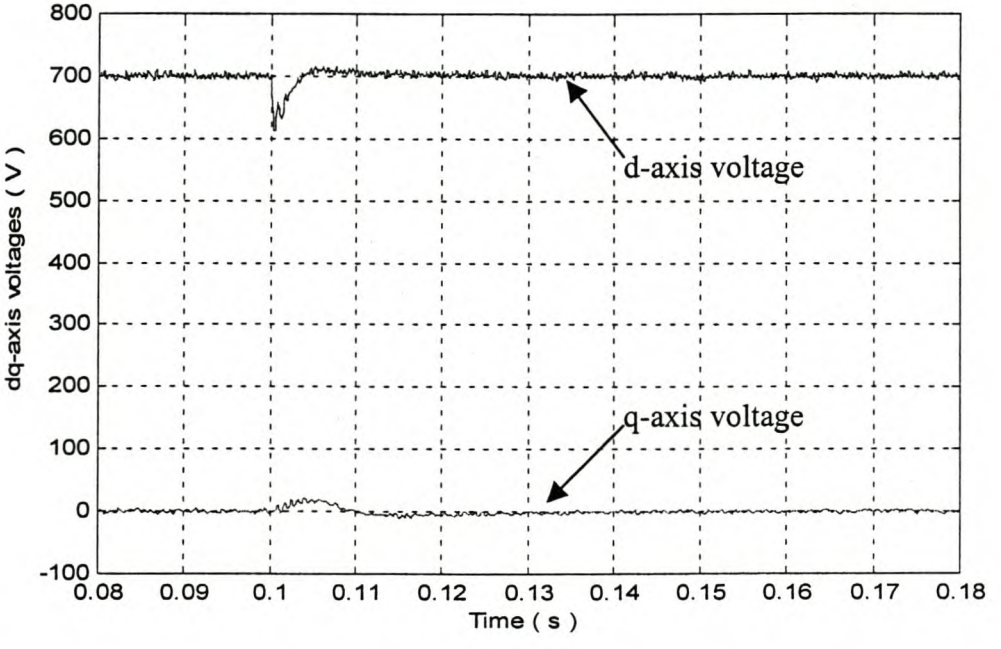


Figure 4-34: Simulated d- and q-axis voltage responses for a positive full-load step with 100 μs sampling period and 0,8 power factor load.

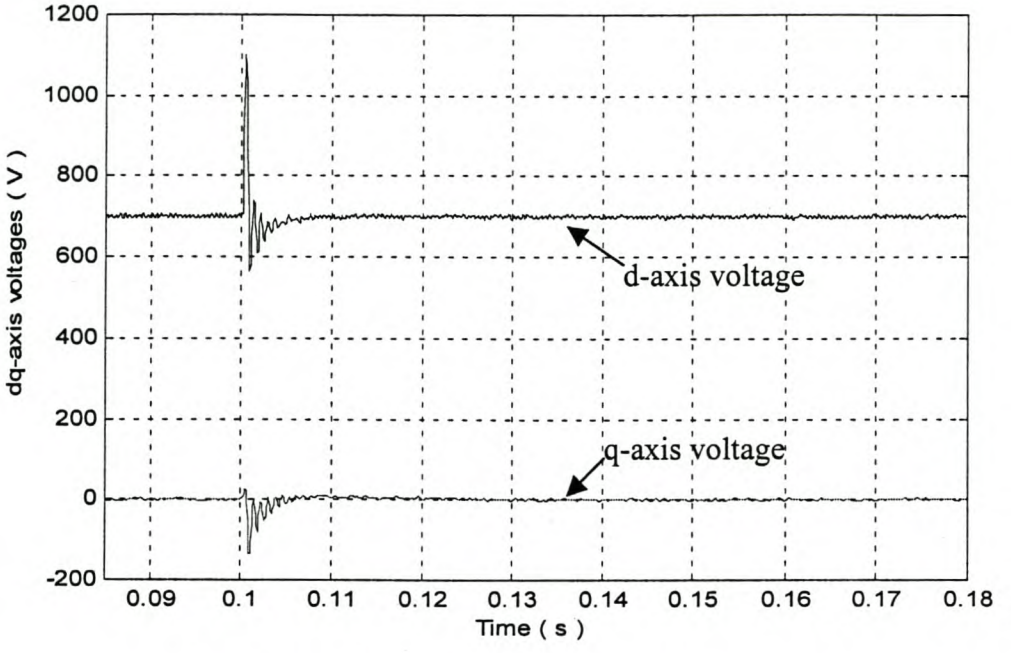


Figure 4-35: Simulated d- and q-axis voltage responses for a negative full-load step with 100 μs sampling period and resistive load.

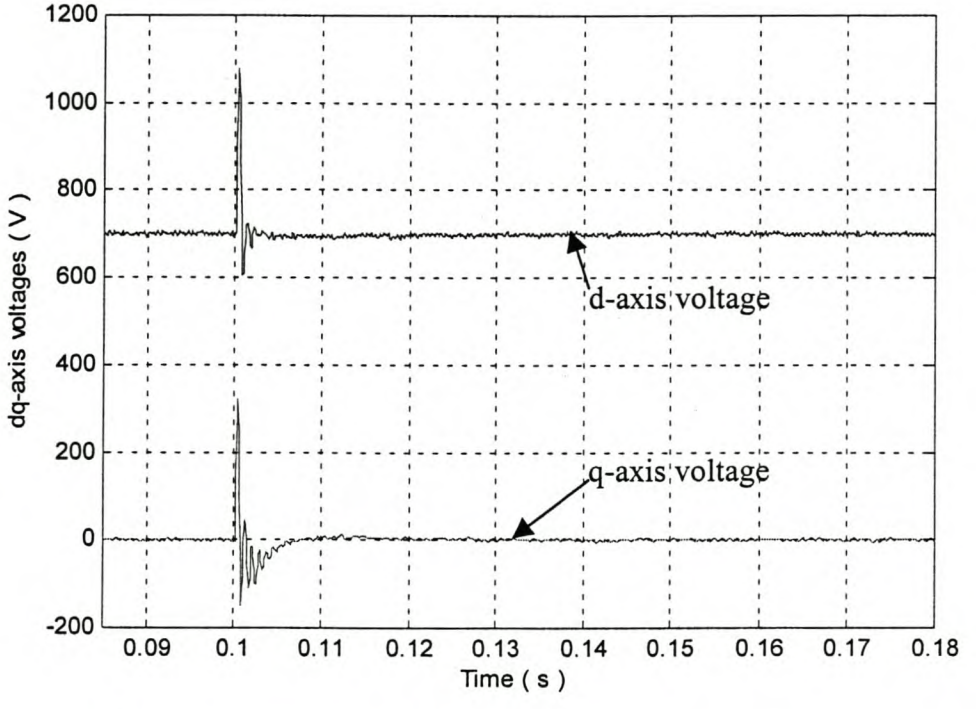


Figure 4-36: Simulated d- and q-axis voltage responses for a negative full-load step with 100 μs sampling period and 0,8 power factor load.

The results that are obtained from Figures 4-29 to 4-36 showed that with a faster sampling period, the response of the system for load steps could be improved. The response of the d-q axis voltages for a positive full-load step is less than 2 ms for a resistive load and less than 3 ms for a 0,8 power factor load. The reflection on the three-phase voltages is very little. The initial voltage drop is very high with a resistive load, but the controller reacts very fast, and within 1 ms the d-axis voltage is within 90% of the reference. With the 0,8 power factor load the initial voltage drop is about 10%, and the d-axis voltage is completely stabilised after 3 ms.

With negative load steps, however, the oscillation in the control voltages is much more severe. The initial overshoot of the d-axis voltage when the load at rated current is disconnected, is more than 60%, but the controller stabilise the voltages within 3 ms. The oscillation in the three-phase voltages continues for about 20 ms.

The results obtained from Figure 29 to 4-36 do not show a significant improvement to the results obtained in Figure 4-8 to 4-11. The initial voltage drop is about the same for both sampling periods (250 μs and 100 μs) when a full-load current step with a resistive load is applied to the system. Also, the response time for the control system with a 250 μs sampling period in Figure 4-10 is about 15 ms and the response time for the control system with a 100 μs sampling period in Figure 4-33 is about 10 ms. When the load is disconnected to the power supply system, the effect on the three-phase voltages are worse for a 100 μs sampling period (Figure 4-31) than for a 250 μs sampling period shown in Figure 4-9. The latter does not make sense from a digital control point of view and has to be investigated further. It is however clear that the LC-circuit is resonating at 581 Hz (see Figure 4-31 and 4-32) which is the cut-off frequency of the LC-filter.

5 DSP CONTROLLER

In this chapter, it is shown in detail how the proposed voltage control algorithm is implemented digitally. Also, some key features are given of the TMS320F240 DSP used for this application. This Digital Signal Processor (DSP) makes it very attractive in implementing the proposed voltage control scheme. The controller hardware is also briefly discussed.

DSP controllers today form an essential part in implementing digital control algorithms. With DSP technology developing very fast, DSP's are capable of executing over 40 million instructions per second (MIPS) nowadays. The TMS320F2407 is capable of running at a clock frequency of 40 MHz, but is not yet available on the market at that clock frequency. The DSP controllers have numerous advantages over analogue controllers such as:

1. In DSP controllers, the control is done entirely by a software program.
2. DSP controllers do not need complex hardware circuitry.
3. The DSP control system can be upgraded by upgrading only the software - no hardware upgrading is needed.

As mentioned already above, for the control of the voltages of the three-phase inverter generation system, a TMS320F240 fixed-point DSP is used. This DSP is capable of executing 20 MIPS. What makes this DSP attractive for the inverter power supply systems, is that it has several advantageous features such as:

- Dual 10-bit A/D channels
- Built in PWM signal generator with dead-time
- Three 16-bit timers with six modes of operation - to do *dq-abc-dq* transformations
- Six compare units - to switch each phase of the inverter

A block diagram of the DSP control system is shown in Figure 5-1.

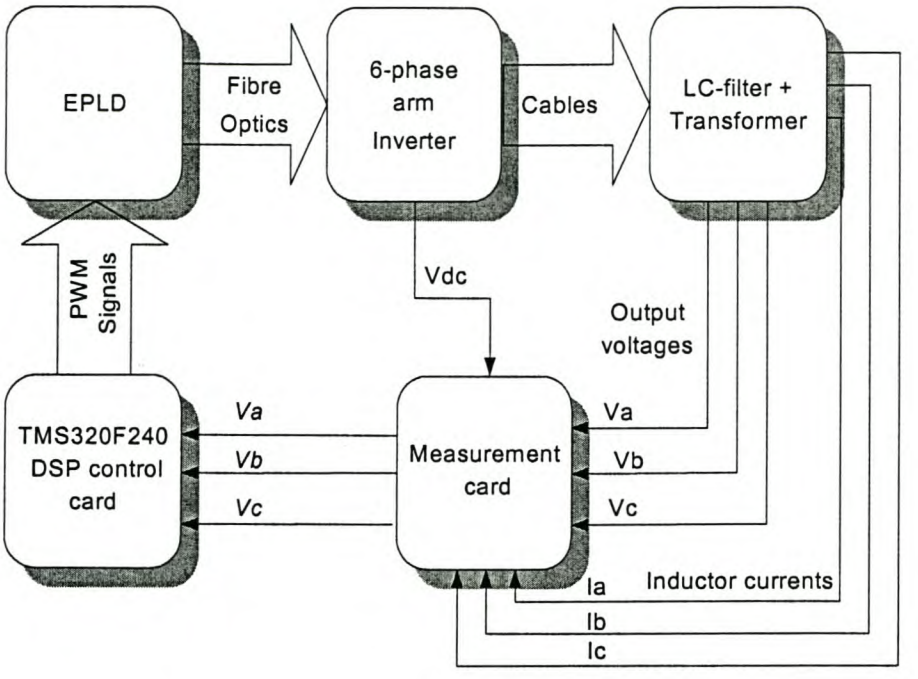


Figure 5-1: Block diagram of the DSP controller system.

The output voltages, the inductor currents, and the DC-bus voltage are measured by means of a measurement card. The DSP controller card then only samples the measured voltages and executes the control algorithm. The PWM signals are electrically connected to an EPLD (erasable programmable logic device). The EPLD creates a complimentary signal for every PWM signal to switch the top and bottom IGBT's of each phase arm. This is because there are not enough PWM lines to switch the six phase-arms of the inverter. The switching is done via fibre optic cables. The EPLD also does the over voltage an over current protection.

5.1 Software description

The source code for the control of the power supply system of Figure 5-1 is written in C-programming language and is given in Appendix A1. A flow diagram of the control program is shown in Figure 5-2.

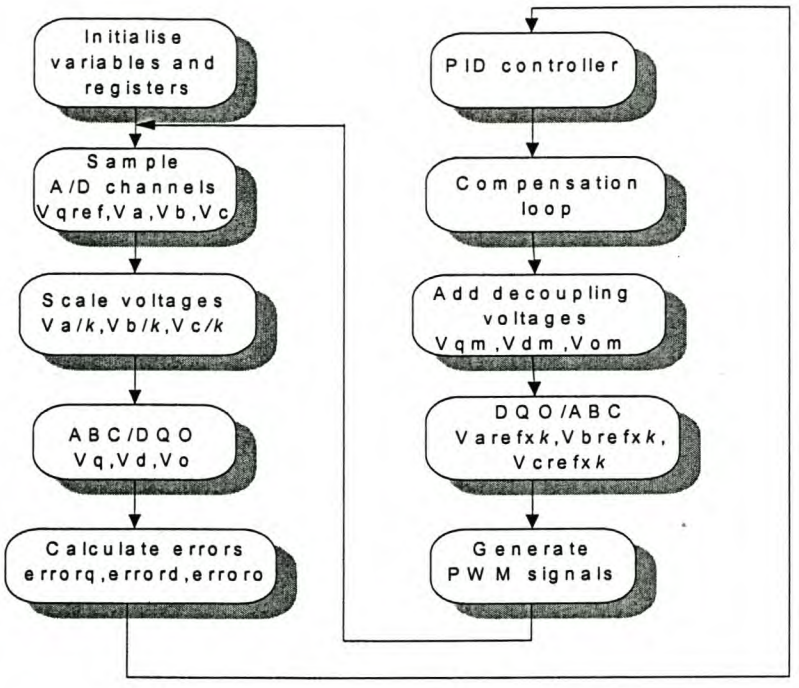


Figure 5-2: A flow diagram of the proposed voltage control method realised in the DSP.

First, all the registers are initialised and also the initial variables are set to zero. Then the control voltages are sampled with the A/D unit. The TMS320F240 can sample two A/D channels simultaneously within 6,2μs. The three-phase voltages A and B are sampled simultaneously, and then voltage C and the reference voltage are sampled, also simultaneously. This makes the A/D conversion time less and, thus, makes the control loop much faster. The values of the voltages are then stored in two reserved registers FIFO1 and FIFO2. The inductor currents and the DC-bus voltage are also measured with the measurement card, but is not sampled with the DSP. It is only used in the hardware protection (overcurrent and over voltage protection).

After the voltages are stored in the registers, the voltages have to be divided by a factor, for example *k (*see Figure 5-2), to prevent overflow of registers when the voltage values are transformed into the *dqo* reference frame and also multiplied with other variables in the control loop. This is a common problem in fixed-point DSP's. After all the calculations have been done to calculate the reference voltages, and the *dqo-abc* transformation have been done, the voltage values have to be multiplied again with the same factor which it was divided with to keep the gain in the control loop constant.

The *abc-dq* conversion is also done with down-scaled values. To generate the Sine and Cosine functions, a look-up table is used. To realise the angle of the *abc-dq* transformation, a second timer (T2PR) is used to count from 0-5000. The index of the look-up table is 5000, because the counter counts from 0-25000 in 20 ms, which is the fundamental period of the output voltages. The counter value is then divided by five to count from 0-5000 in 20 ms. The index of the look-up table is generated with a PASCAL program, which is given in Appendix A2. Figure 5-3 shows how the Sine function is realised. The Cosine is realised by using the same look-up table, but simply shifting the angle by 90°.

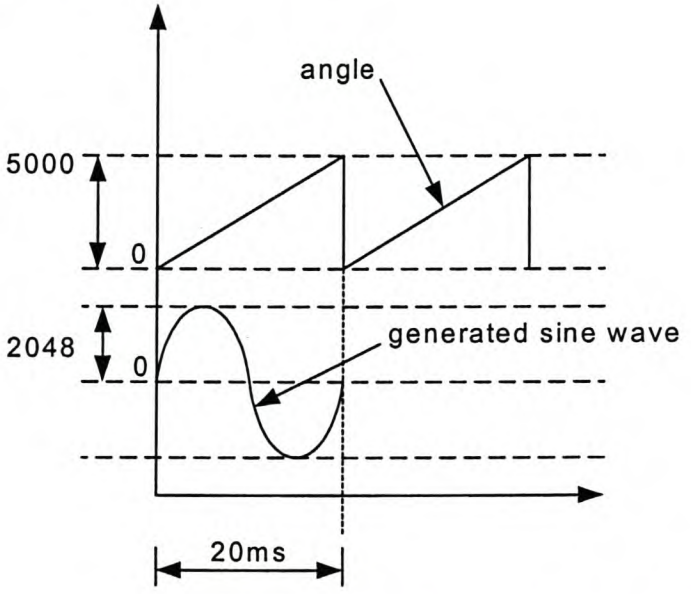


Figure 5-3: Generated Sine wave realised with look-up table (index is from 0-5000).

For every step that the timer counts, the program looks up the value from the Sine table and then uses these values for the calculations in the *abc-dq* or *dq-abc* transformations.

Although there is Sine and Cosine functions built in the DSP, it takes quite a lot of time to execute, up to several clock cycles. A look-up table is a much faster way (only one clock cycle) of generating the Sine and Cosine function and this makes the control loop faster.

The error voltages, in Figure 5-2, are then calculated by subtracting the measured voltages from the reference voltages. These error voltages are then fed to a PID controller. The PID controller real-time equation is given below for the d-axis voltage,

$$PIDd_{out}(T) = (K_p + K_i T + \frac{K_d}{T})error(T) + (K_p + \frac{2K_d}{T})error(T-1) + (\frac{K_d}{T})error(T-2),$$

where T is the sample period and equal to: $T = 250\mu s$. The response of the system is very sensitive to the controller coefficients K_p, K_i, and K_d, that's why these calculations have to be done with floating-point calculation registers. This calculation takes several cycles of the clock to complete, as the TMS320F240 DSP is a fixed-point processor. After the floating-point calculations, the output of the PID controller is converted to integer values to be used in the rest of the control loop.

The compensation loop, which is described in section 3.3 and shown in Figure 5-2, is done with only fixed-point calculations, although the coefficients of the inverse transfer function of the system are real values. This had no effect on the dynamic performance of the compensation loop. Matsui [18] also showed that the same dynamic performance could still be achieved even if the coefficients of the inverse transfer function are not the same as the coefficients of the actual power supply system. A flow diagram of how the compensation is digitally implemented is shown in Figure 5-4.

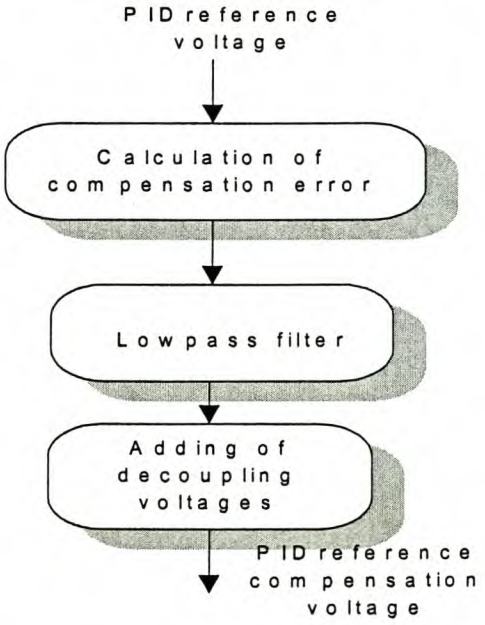


Figure 5-4: Flow diagram of compensation loop.

The PID reference signal in Figure 5-4 is the output of the PID controller. The compensation error is calculated by merely subtracting the reference voltage (which is the output of the PID controller) from the output of the inverse transfer function of the power supply system. This is described in detail in Chapter 3, section 3.3.

The compensation error is then put through a lowpass filter as shown in Figure 5-4. The filter is digitally implemented by the following equation:

$V_{out}(T) = V_{out}(T-1) - \frac{V_{out}(T)}{aT} + \frac{V_{in}(T)}{aT}$, where aT is the cut-off frequency of the filter. The decoupling voltages are then added to the output of the lowpass filter to generate the controller compensation reference voltage, i.e the PID reference compensation. This PID reference compensation voltages are then transformed into the *abc* reference frame and the three-phase reference voltage signals are generated. These three-phase voltage signals are then compared to a timer output, which is an up-and-down counter. When a match is made between the reference voltage and the up-and-down counter, the switching voltages of the IGBT's changes state, either from a logical 1 to 0 or vice versa, thus realising PWM switching. A sketch is shown in Figure 5-5 to explain the latter.

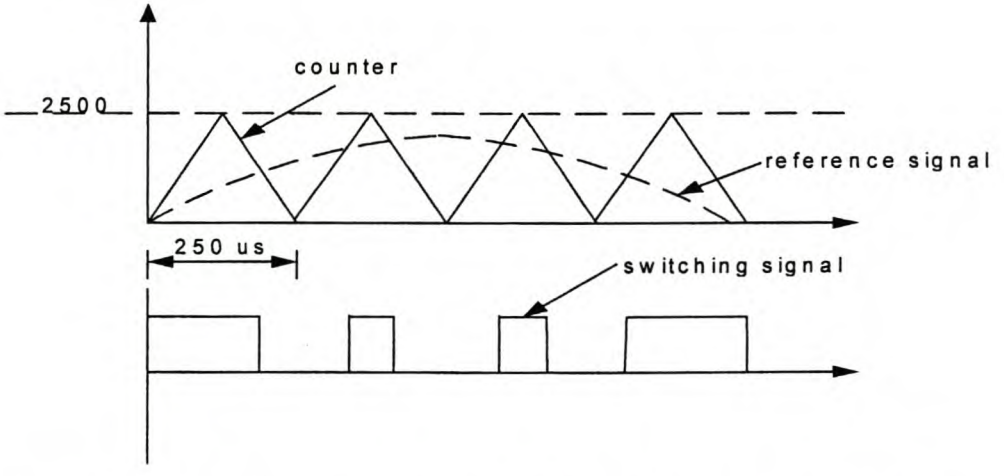


Figure 5-5: Up-and down counter output and voltage reference signal.

The counter is set to count up from 0-2500 and down from 2500-0 in 250 μs, by adding a specified value in register TPR1. Register TPR1 is used to establish the switching frequency, thus, by adding the value 2500 in register TPR1, a switching frequency of 4 kHz is realised.

To realise unipolar switching with the TMS320F240, six compare registers are used namely three full compare registers (COMP1, COMP2, COMP3) and three simple compare registers (SCOMP1, SCOMP2, SCOMP3). For each phase-arm, the six registers compare a reference signal with the up-and-down counter, and if a match is made, the registers give a logic high output. These outputs are then written to the output data register and the PWM signals are generated. These six outputs from the DSP controller are then electrically connected to an EPLD which is used to generate the complementary signals to switch the top and bottom IGBT in each phase-arm, thus realising the unipolar switching scheme.

5.2 Hardware description

The control voltages and inductor currents are measured with voltage and current transducers. The inductor currents are measured only for protection purposes and are not sampled by the A/D converter of the DSP.

The DSP controller is built into a Euro-rack, which consists of a backplane for connections between the different cards. A separate power-supply is also built for the controller. The different components of the controller are discussed further in this section.

5.2.1 DSP control card

The first prototype DSP control card was designed and developed at the University of Stellenbosch as part of a postgraduate research project. The control card was modified after that to suit the application of this project. The PCB layout is also modified and the schematics of the control cards are shown in Appendix B6 – B8.

The TMS320F240 device has an on chip 16Kword flash array, for use as program memory. The Flash array is programmed via a JTAG interface. The serial boot loader is designed to program the flash memory array by making use of the Serial Communication Interface (SCI). The F240 can then be programmed using a standard RS232 serial communication port from a host PC communication port via an appropriate RS232 driver circuit. This serial boot loader provides a convenient technique to program the flash array through the serial interface.

The EPLD, which is on the same card as the DSP, is used to generate the PWM signals for unipolar switching. It is also programmed for over current and -voltage protection. The EPLD also provides a visual interface with the user.

5.2.2 Measurement card

A schematic diagram of the measurement card is shown in Appendix B1 and B4. The voltages and currents are measured by voltage and current transducers respectively. The outputs of these transducers are current signals that flow through resistors on the measurement card. The voltages across these resistors are then the input to the operational amplifiers. The second amplifier adds an offset of 2,5 V. This shifts the measured voltage signals between 0-5 V, as the A/D channels of the DSP can only sample voltages between 0-5V.

In Appendix B3, the over current protection is done by comparing the measured three-phase inductor currents with a positive and a negative DC-current level. The output is fed through a level detector. When a fault occurs, the output of the level detector is active low. The output of these level detectors (AF_+, AF_-, BF_+, BF_-, CF_+, CF_-), is then fed through logic gates, which generates the error signal. The same is done for the over voltage protection on the DC-bus. The positive and negative DC-bus is first scaled down with a voltage divider. The output is then put through a difference amplifier and compared to a reference. The output again is active low when a fault occurs.

5.2.3 Fibre optics card

The fibre optics schematic is shown in Appendix B5. Only six of the twelve fibre optic outputs are used in this application. The driver boards of the inverter generate the compliment of the input signals, therefore generating the twelve switching signals needed to realise unipolar switching. All the switching signals are active low.

The fibre optic card also has three fibre optic inputs for error signals generated by the inverter. These three signals are combined with a logic gate and are fed to the EPLD as an error signal.

6 EXPERIMENTAL RESULTS

The proposed voltage control method is tested and evaluated on an 8 kW laboratory system according to the specifications laid down in Chapter 3, Table 3-1. In the first section of this chapter, the laboratory set-up is briefly discussed. Then the open loop results are shown with a harmonic analysis of the three-phase supply voltages. The control loop is then closed and the results are shown for load steps with and without the compensation technique. The proposed voltage control method is also compared to the alternative voltage control method described in section 4.3. The proposed voltage control method is then finally evaluated under unbalanced conditions and also with a non-linear load.

All the measurements in this chapter are done with a Tektronix TDS 460A 400 MHz digital oscilloscope. The voltage measurements are done using the oscilloscope's own probes which ratio is 100:1. The Tektronix TMS02A current amplifier and current probe is used to measure all the currents. The harmonic analysis is done using a software package, WaveStar, which is used to download all the measured waveforms from the oscilloscope to a PC.

6.1 Laboratory set-up

Figure 6-1 shows the laboratory set-up. All the important parts in the set-up are discussed in the following sub-sections.

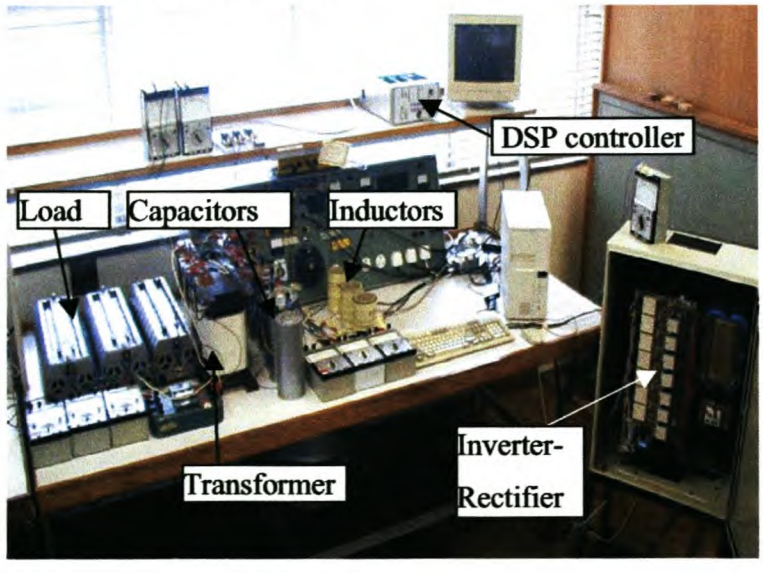


Figure 6-1: Picture of laboratory set-up.

The system parameters are given in Table 6-1.

Table 6-1: Laboratory model system parameters.

Parameter	Value	Units
Switching frequency	4	kHz
Nominal DC Bus voltage	420	V
Rated output voltage	230	V_{rms}
Rated output frequency	50	Hz
Rated output power	8	kW
Rated output current	12	A_{rms}
Filter inductor	500	μH
Inductor resistance	300	mΩ
Filter capacitor	140	μF

6.1.1 Rectifier-inverter

A three-phase supply voltage from the network is connected to the three-phase rectifier of the rectifier-inverter hardware shown in Figure 6-2. The three-phase voltages from the network are rectified and this establishes the DC-bus voltage. A seven-phase inverter, earlier developed by [19] for a motor drive, is used for this application. Only six of the phase-arms are used to realise a unipolar switching scheme. As can be seen, the rectifier and inverter are built in one compartment.

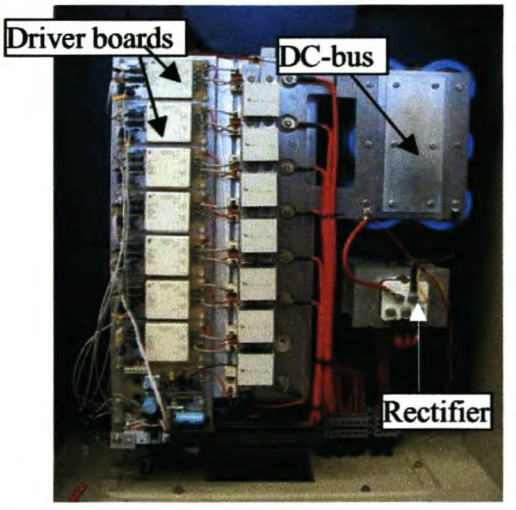


Figure 6-2: Picture of the rectifier-inverter hardware.

6.1.2 DSP controller

The TMS320F240 DSP controller is used in the laboratory set-up. A PC is used to load the written software algorithm in the DSP via a serial cable. The DSP controller is thoroughly tested with test programs before it is used for this application. A picture of the DSP controller is shown in Figure 6-3.

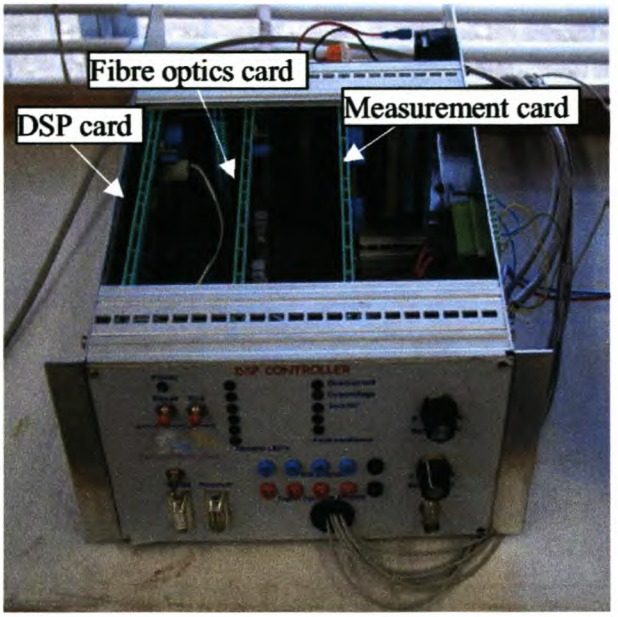


Figure 6-3: Picture of the DSP controller.

6.1.3 LC-filter

The LC-filter is developed in the laboratory. A 500 μH inductor is used in the set-up. The inductor is designed according to the design calculations discussed in Chapter 2 and also with the design program in Appendix D. The inductor can handle a maximum current of 12 A_{rms}. A 230 V, 460 μF, and a 230 V, 230 μF capacitor is put in series to get an equivalent capacitance of 140 μF.

6.1.4 Transformer

A 10 kVA three-phase transformer is connected at the output of the LC-filter. The transformer is shown in Figure 6-1. The winding ratio of the transformer is 1:1. The secondary of the transformer is connected in star and the neutral connection is grounded. The laminations of the transformer should be tightly clamped to ensure that the high frequency PWM voltages would not cause vibrations of the laminations and therefore cause mechanical noise.

6.1.5 Load

A three-phase resistive load is connected through a three-phase switch to the secondary of the transformer. The resistors are connected in star and the neutral point is grounded. In the laboratory set-up, no inductive or capacitive loads are used.

6.2 Open loop results

First, some open loop tests are conducted on the 8 kW power supply system. The system is just given a d- and q-axis voltage reference with no voltages fed back. The voltages over the capacitors of the filters are referred to as ***control voltages***, and the voltages on the secondary of the transformer are referred to as ***supply voltages***. The sample period is taken as 250 μs. The control- and supply three-phase voltages are shown in Figures 6-4 and 6-5 respectively.

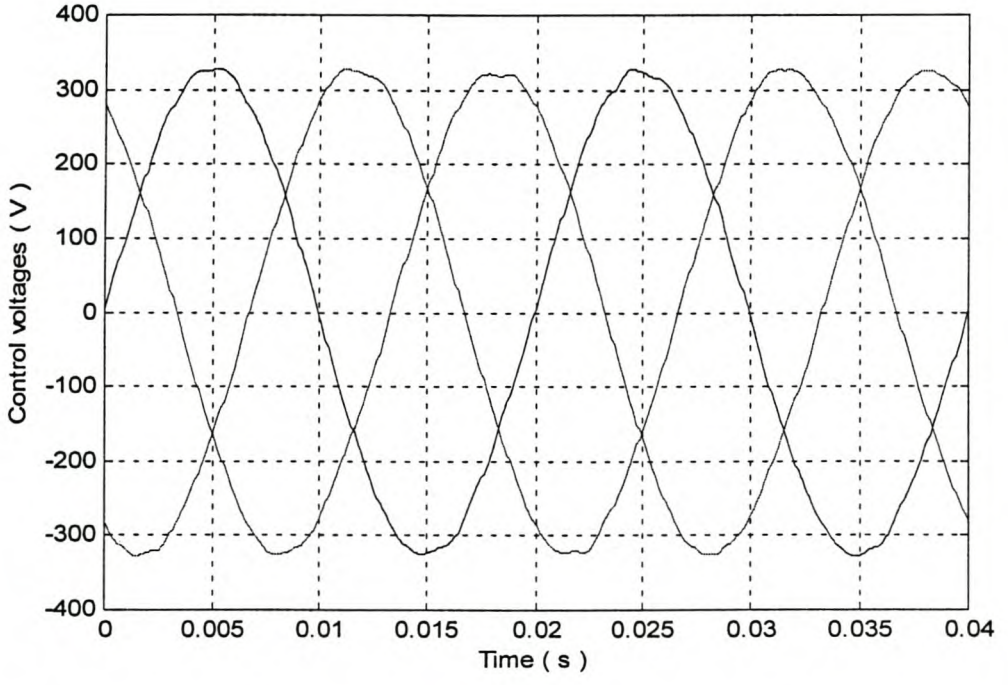


Figure 6-4: Measured three-phase open loop control voltages in the steady state.

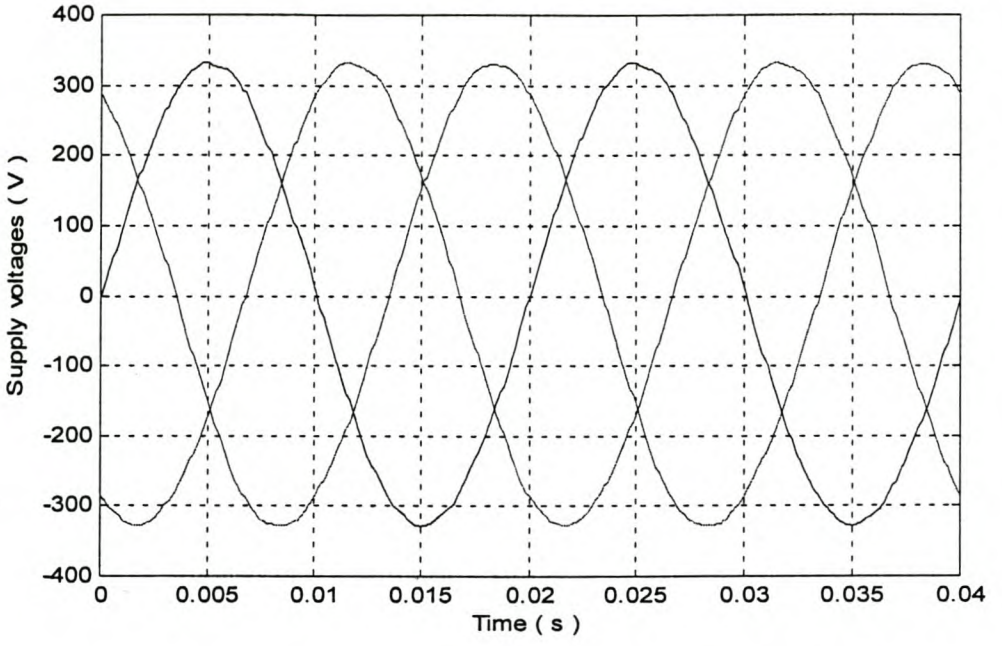


Figure 6-5: Measured three-phase open loop supply voltages in the steady state.

The d-axis voltage response of the system with a positive full-load step is given in Figure 6-6. The ΔV of 34 V is equivalent to a voltage drop of 10,4% in the control voltage.

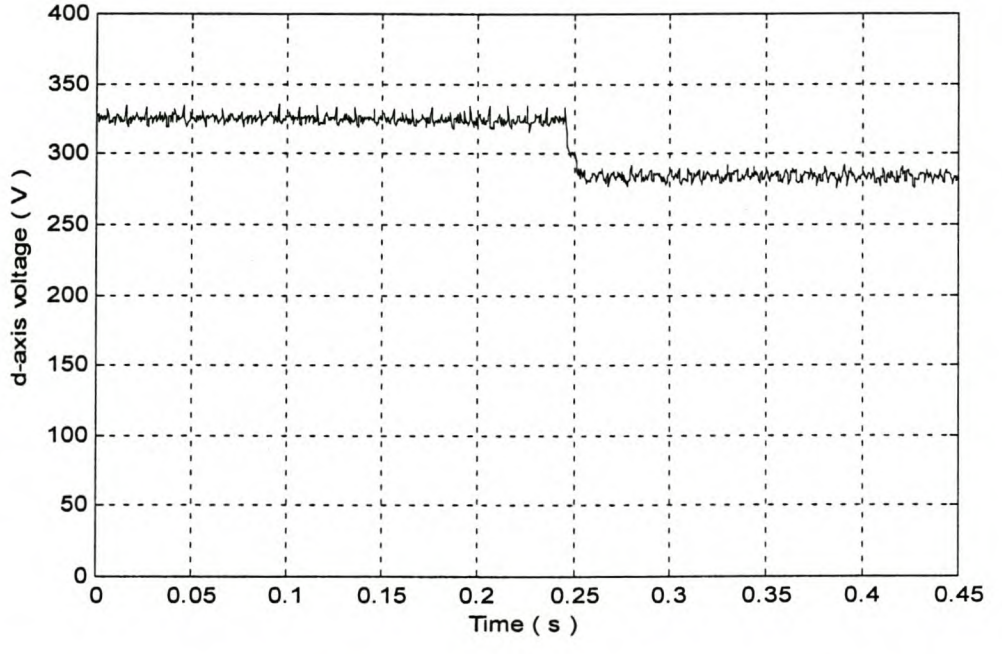


Figure 6-6: Measured open loop d-axis control voltage response to a positive full-load step.

A harmonic analysis is done on the measured supply voltages with the results shown in Figure 6-7. The total harmonic distortion (THD) is calculated as 1,18%. This is well below the required limit of 8%.

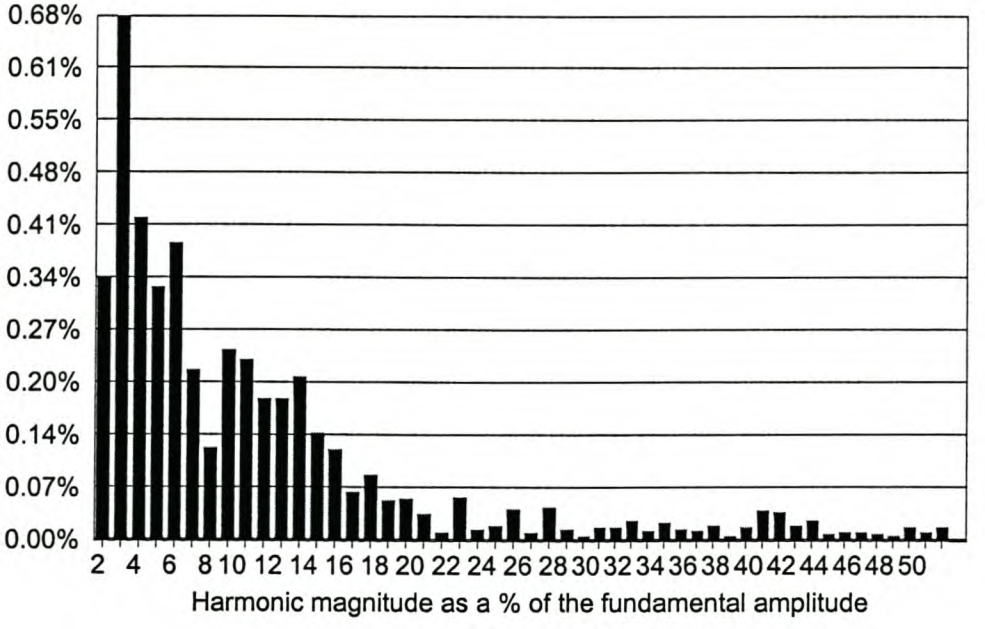


Figure 6-7: Harmonic content of the measured open loop supply voltages.

6.3 Closed loop results

The proposed voltage control method is further evaluated by closing the feedback loop. The closed loop system shown in Figure 4-4 is practically evaluated with and without the compensation loop. In the closed loop control system, with and without the compensation loop, no decoupling of the ωLi_{dq} and ωCv_{dq} voltages and currents were done, as it was found to have little effect on the system response. The same PID controller, with and without compensation, is used in the control loop and the sampling period is taken as 250 μs. Also, no *o*-axis voltage control is done in the implementing of the control algorithm as the transformer is sensitive to DC offsets and therefore the control system can easily become unstable [15].

6.3.1 Without compensation

The proposed voltage control method without compensation is then implemented and the measured and simulated responses for the d- and q-axis voltages are shown in Figure 6-8. In the control loop, no decoupling of the ωLi_{dq} voltages and the ωCv_{dq} currents are

done, but only decoupling of the d- and q- axis voltages of the LC-filter. The coupling voltages (ωLi_{dq}) and currents (ωCv_{dq}) are seen as disturbances. From Figure 6-8 it can be seen that the simulated and measured results compare well with each other.

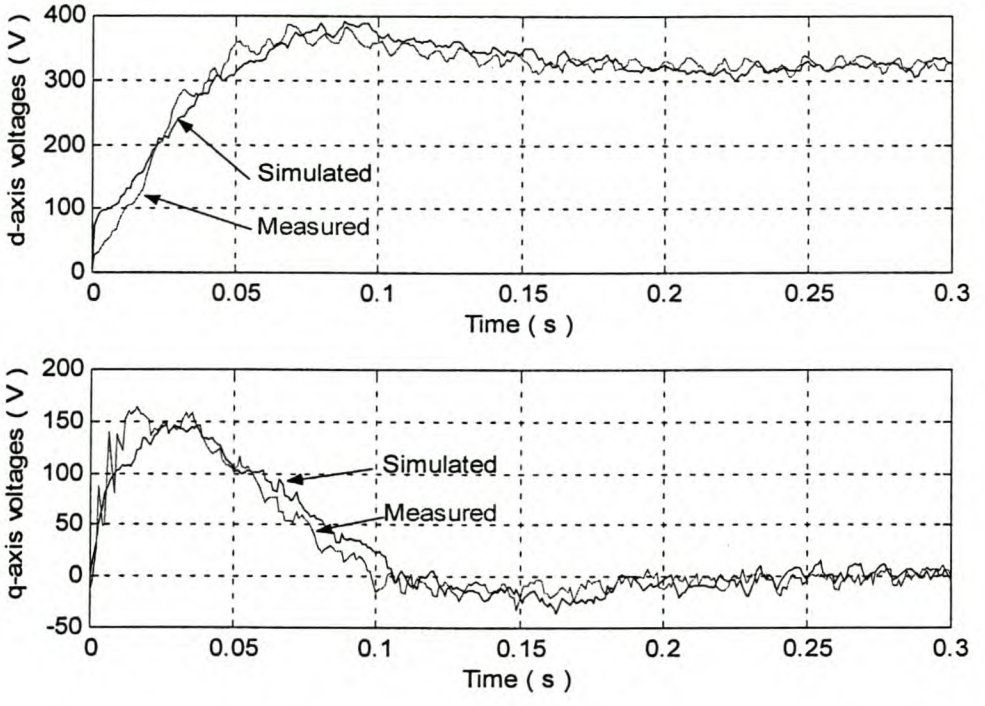


Figure 6-8: Simulated and measured responses of the d- and q -axis voltages to a d-axis voltage step input.

The system is designed for a settling time of 20 ms with an overshoot of 15%. From Figure 6-8 it can be seen clearly that the response is much slower than what is designed for. Because of the slow sampling period, no effective decoupling of the feedback voltages could be established. The PID controller therefore sees the feedback voltages of the LC-filter (v_d and v_q) and the coupling voltages and currents (ωLi_{dq} and ωCv_{dq}) as disturbances. This is why the response is much slower than what was designed for. The latter is discussed in Chapter 3.

With the closed loop control, a positive full-load step is applied to the system. The measurements are conducted to give an indication of how well the simulated and measured results compared. The simulated and measured results are shown in Figure 6-9. Again the measured results compare well with the simulated results, although the responses of the d- and q-axis voltages are very slow. The dip in the voltage of the

measured d-axis voltage is slightly lower than the simulated voltage, but the settling time is nearly the same.

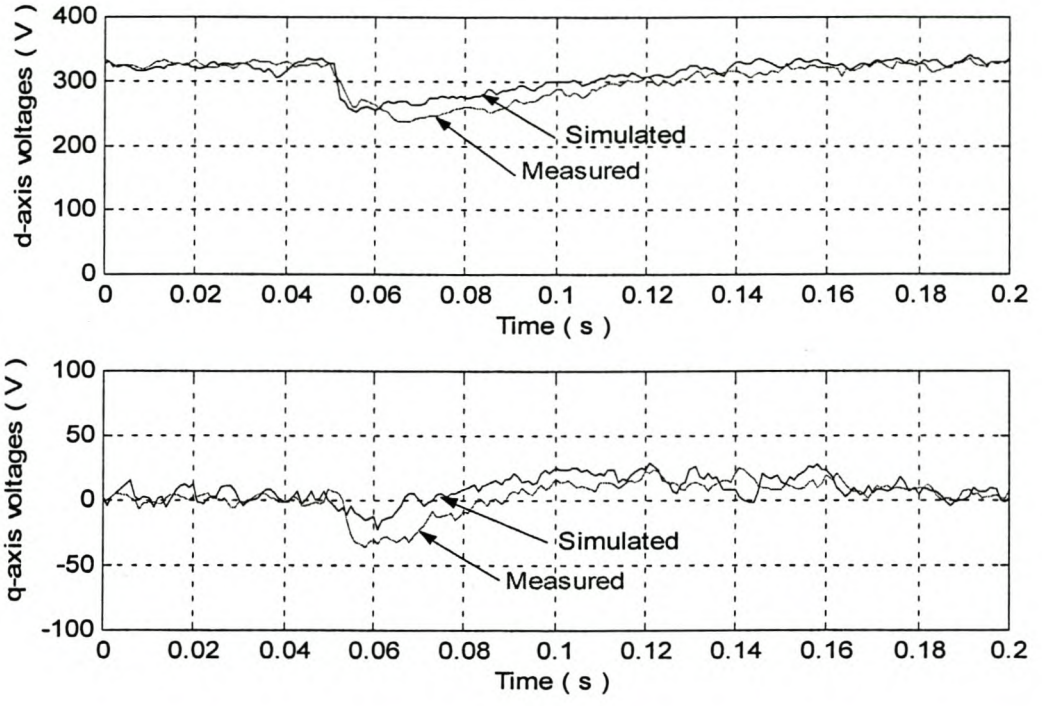


Figure 6-9: Simulated and measured results with a positive load step without compensation.

6.3.2 With compensation

The compensation loop is then added to the control system and a step in the d-axis voltage is applied to the system. The q-axis voltage is kept zero. The results are shown in Figure 6-10.

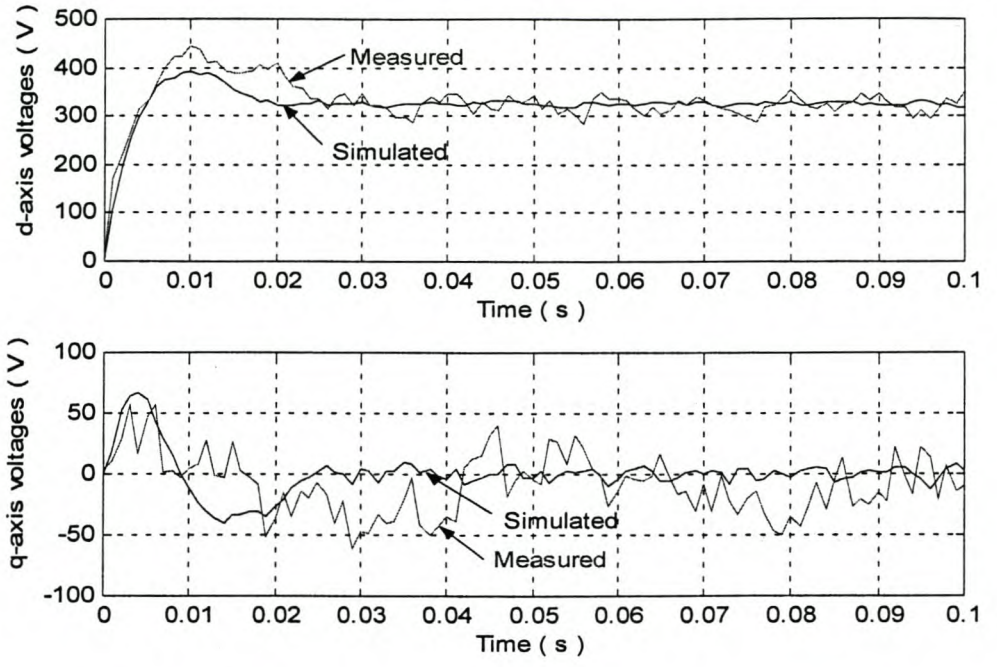


Figure 6-10: Simulated and measured responses of the d- and q-axis voltages with compensation on to a d-axis voltage step input.

From Figure 6-10 it can be seen that with the compensation loop the response of the system is the same as what has been designed for. Also, the measured results compare very well with the designed and simulated results. Figure 6-8 shows that the system response without compensation is much slower than what has been designed for, i.e. 20 ms settling time.

A positive and negative load step is again applied to the system using the compensation loop in the control algorithm. The results are shown in Figures 6-11 and 6-12. The load step was applied at time = 25 ms.

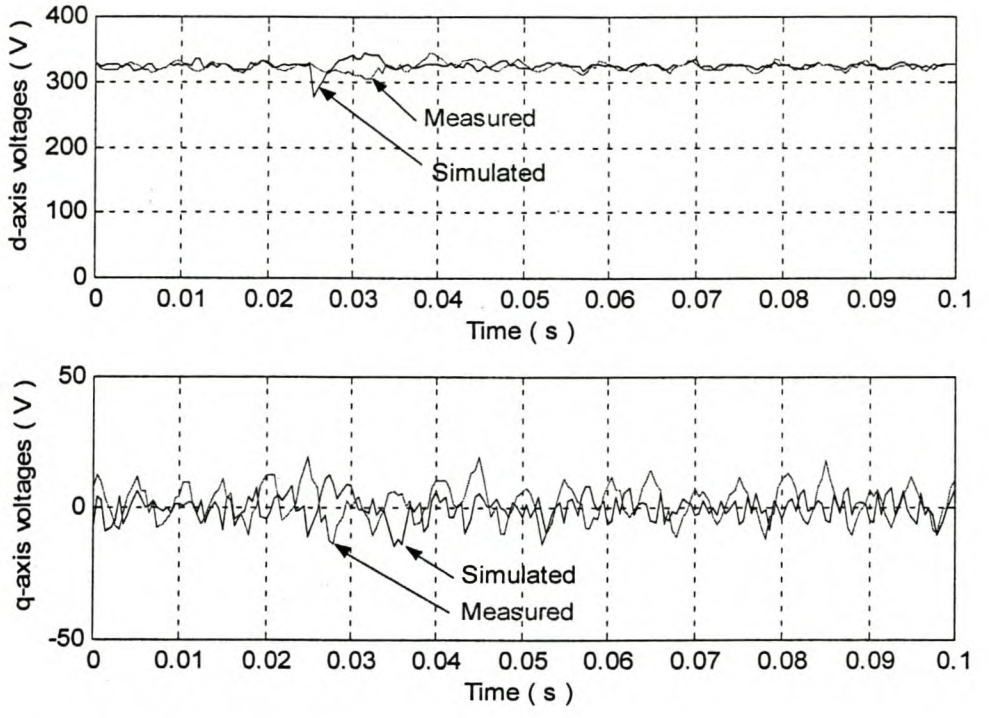


Figure 6-11: Simulated and measured results of the d- and q-axis voltages with compensation with a positive load step.

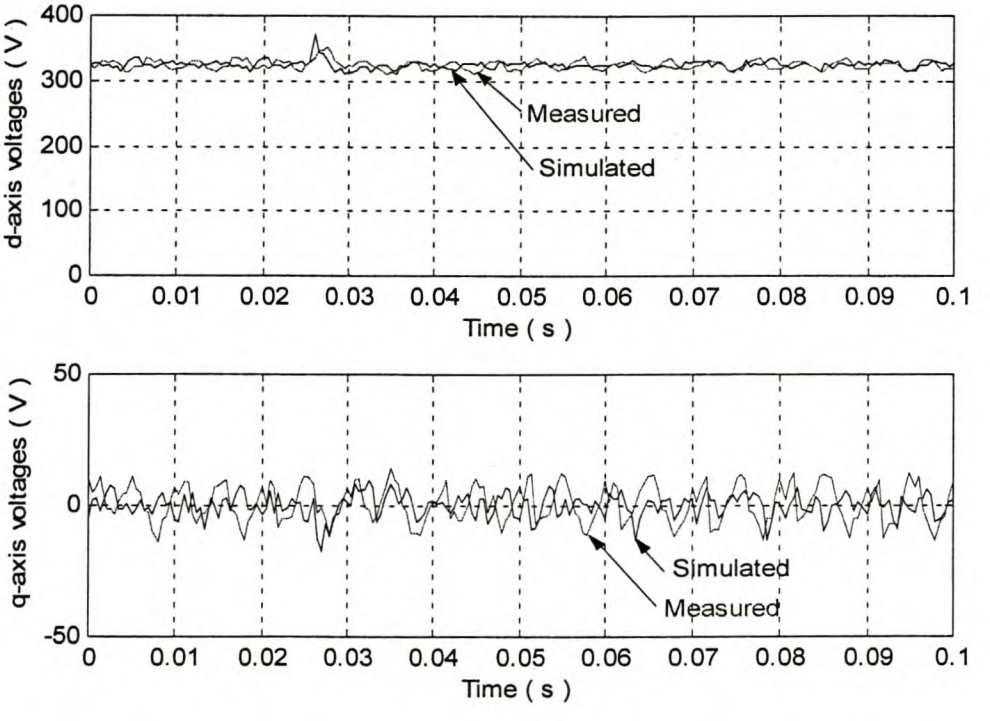


Figure 6-12: Simulated and measured results of the d- and q-axis voltages with compensation with a negative load step.

With the compensation loop in the control loop, the responses of the d- and q-axis voltages are very fast. The settling time of the d-axis voltage is about 8 ms. Also, the initial voltage drop in the d-axis voltage is 5,5% for a positive load step. For the negative load step, the settling time is also 8 ms. The d-axis voltage shows an overshoot of 10%. The q-axis voltage shows no change when a load step is applied to the system. Figure 6-9 shows that the settling time of the d-axis voltage when a full-load step is applied, is about 100 ms. This is more that 10 times slower than the settling time shown in Figure 6-11 with the compensation loop in the control system.

Much difficulty was experienced to measure the effect of a positive full-load step on the three-phase voltages with the oscilloscope. A simulation was done instead to show the effect of a positive full-load step on the three-phase control voltages, as it was shown that there is good correlation between the simulated and measured results. This is shown in Figure 6-13. Initially, 2 A is drawn from the load and at time = 0,1 s, a 10 A current step is applied to the system. The full-load current of the load is 12 A.

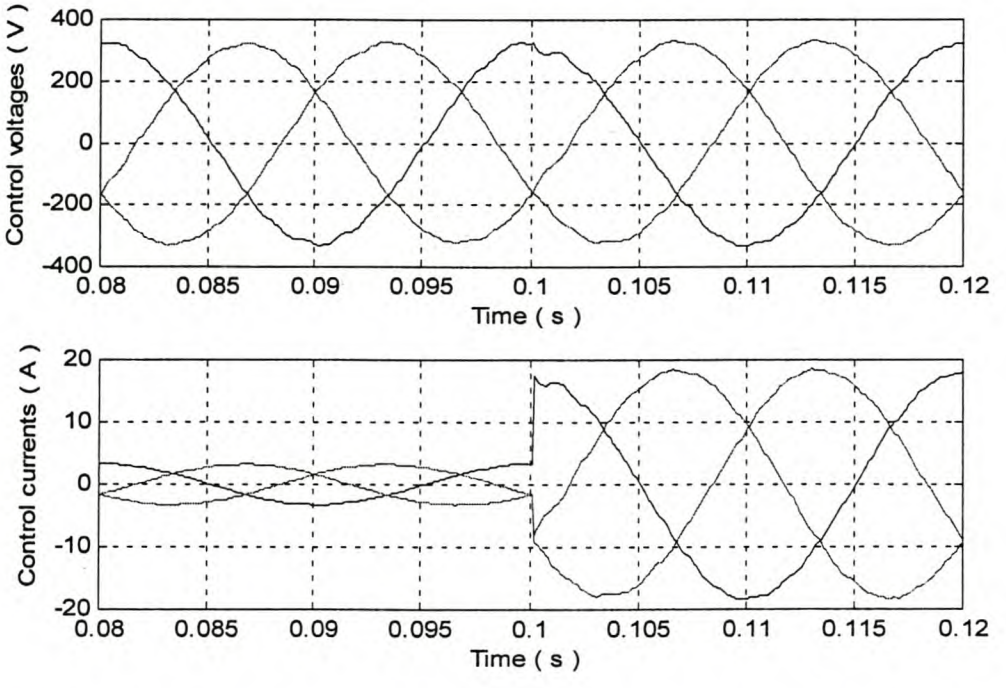


Figure 6-13: Effect of positive full-load step on control voltages and currents (simulated).

The three-phase control voltages and the three-phase supply voltages with compensation are shown in the steady state in Figures 6-14 and 6-15 respectively. A harmonic analysis is also done on one phase of the supply voltages and the THD is calculated as 1,2%.

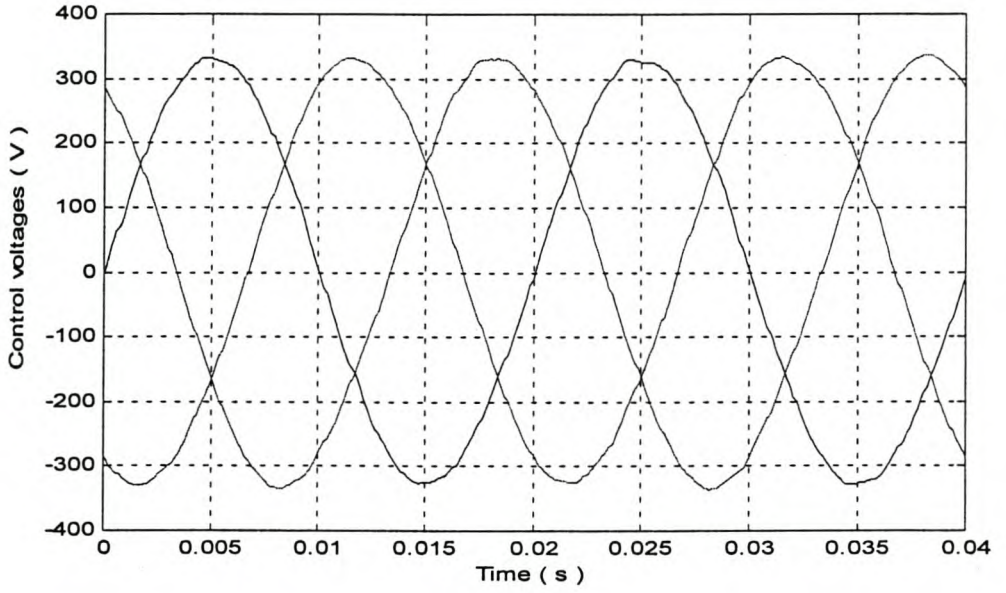


Figure 6-14: Measured three-phase control voltages with compensation in the steady state.

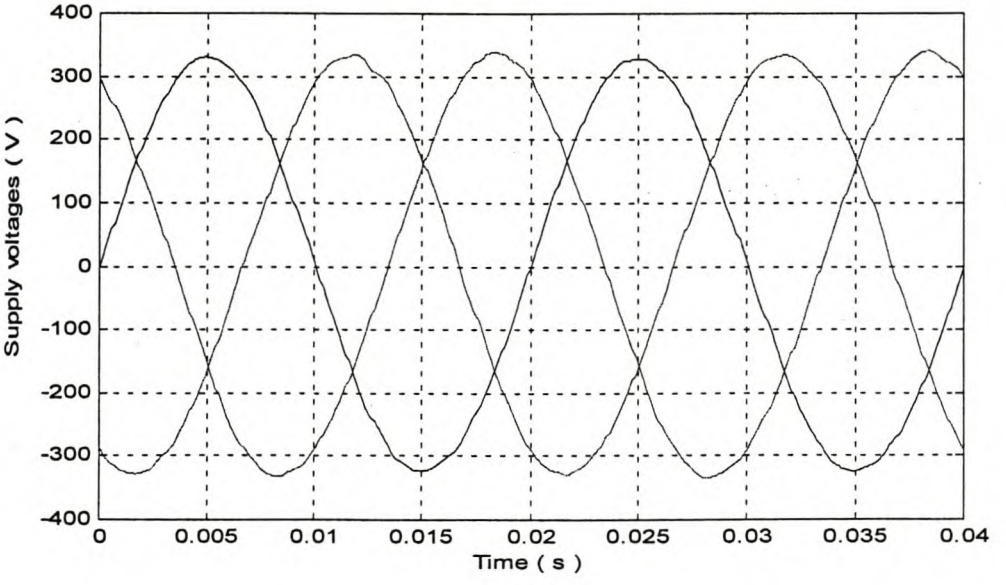


Figure 6-15: Measured three-phase supply voltages with compensation in the steady state.

6.4 Alternative voltage control method

The alternative voltage control method is discussed in detail in Chapter 4, section 4.3. This voltage control method involves the feedback loop of the LC-filter in the design of the control system and is shown in Figure 4-16 and Figure 4-17. The alternative voltage control method is also practically evaluated and compared to the proposed voltage control method where the feedback loop of the LC-filter is not included in the design of the PID controller, but decoupled in the control system (see Figure 3-7 and Figure 4-4). The simulated and measured responses are shown in Figure 6-16 for a step input in the d-axis voltage. The q-axis voltage was kept zero.

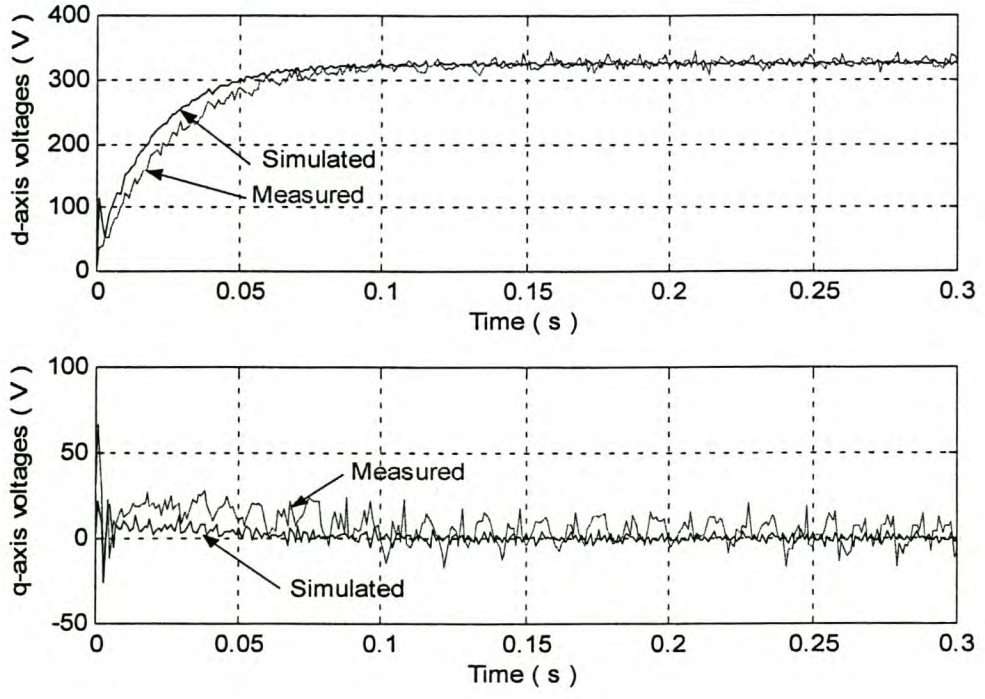


Figure 6-16: Simulated and measured response of the alternative voltage control method with a step input in d-axis voltage.

The closed loop poles of the alternative voltage control method are very weakly damped, and a much slower response has to be designed for because of oscillations in the d- and q-axis voltages for a step input in the d-axis voltage. The alternative voltage control method is designed for a 100 ms settling time for a step input voltage in the d-axis voltage, where the proposed voltage control method is designed for a 20 ms response for step input in the d-axis voltage.

The alternative voltage control method is further evaluated with load steps. A positive and negative load step is applied to the system and the simulated and measured results are given in Figure 6-17 and 6-18 respectively. The response to load steps, however, is very fast for the alternative voltage control method. Although the simulations show a very fast response with load steps, the measured results are much slower. The settling time for positive and negative load step is 40 ms, that is two voltage cycles. The initial voltage drop, however, is about 6% when a positive load step is applied to the system. The voltage overshoot is about 7% for a negative load step. Overall, however, the measured and simulated results compare well.

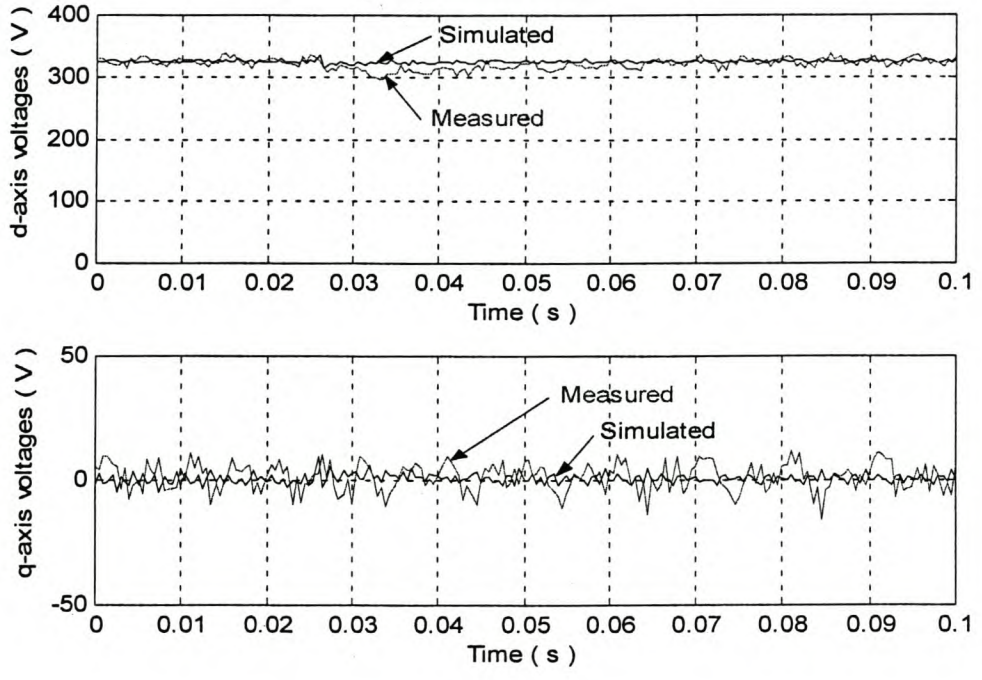


Figure 6-17: Simulated and measured responses with alternative voltage control method for a positive load step.

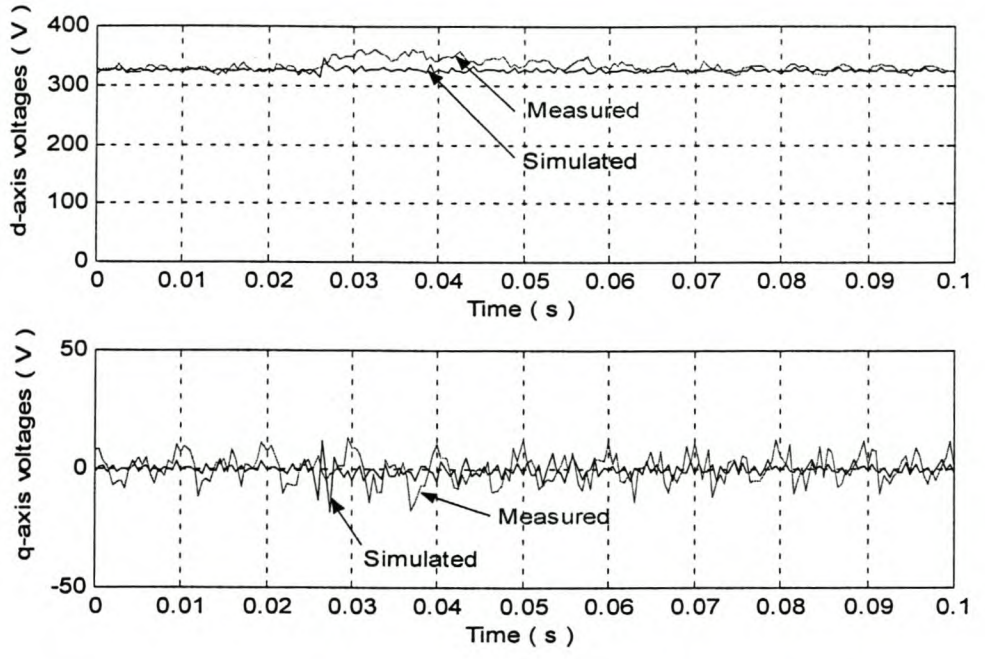


Figure 6-18: Simulated and measured responses with alternative voltage control method for a negative load step.

The three-phase control voltages and three-phase supply voltages are also measured and are shown in Figure 6-19 and 6-20 respectively. The total harmonic distortion (THD) was calculated for one phase of the control voltages as 1,8% and for the supply voltage, the THD was calculated as 2%.

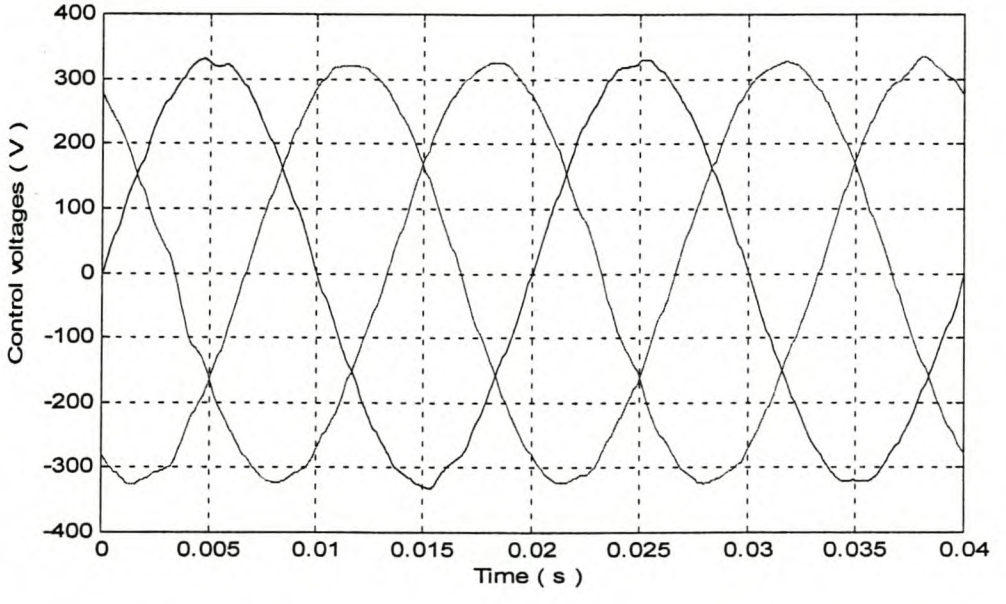


Figure 6-19: Measured three-phase control voltages with the alternative control method in the steady state.

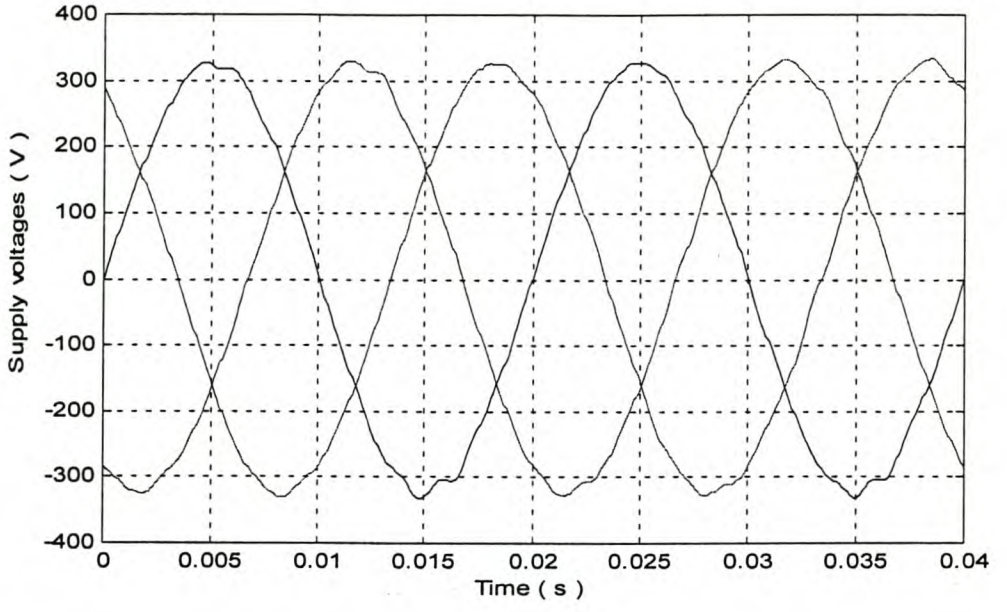


Figure 6-20: Measured three-phase supply voltage with alternative control method in the steady state.

From Figures 6-11 to 6-15 it is clear that the proposed voltage control method gives better results than the alternative voltage control method shown in Figures 6-17 to 6-20. The measured settling time of the proposed voltage control method is about 8 ms on load steps. The initial voltage drop is 5,5%. The alternative control method has a measured settling time of 40 ms. The initial voltage drop is 6%. Also, the THD of the control voltages of the proposed voltage control method is calculated as 1,2% and the total harmonic distortion for the control voltages of the alternative voltage control method is calculated as 1,8%. Both THD calculations for the control voltages of the two voltage control methods are well within the limits of the NRS048 specifications of SABS shown in Table3-1.

6.5 Unbalanced conditions

The proposed voltage control method was further evaluated under unbalanced conditions. The voltage unbalance is calculated with equation 3-12 in chapter 3. With a balanced three-phase load, the unbalance in the control voltages is calculated as 0,7%. The measured three-phase supply voltages and currents in the steady state are shown in Figure 6-21.

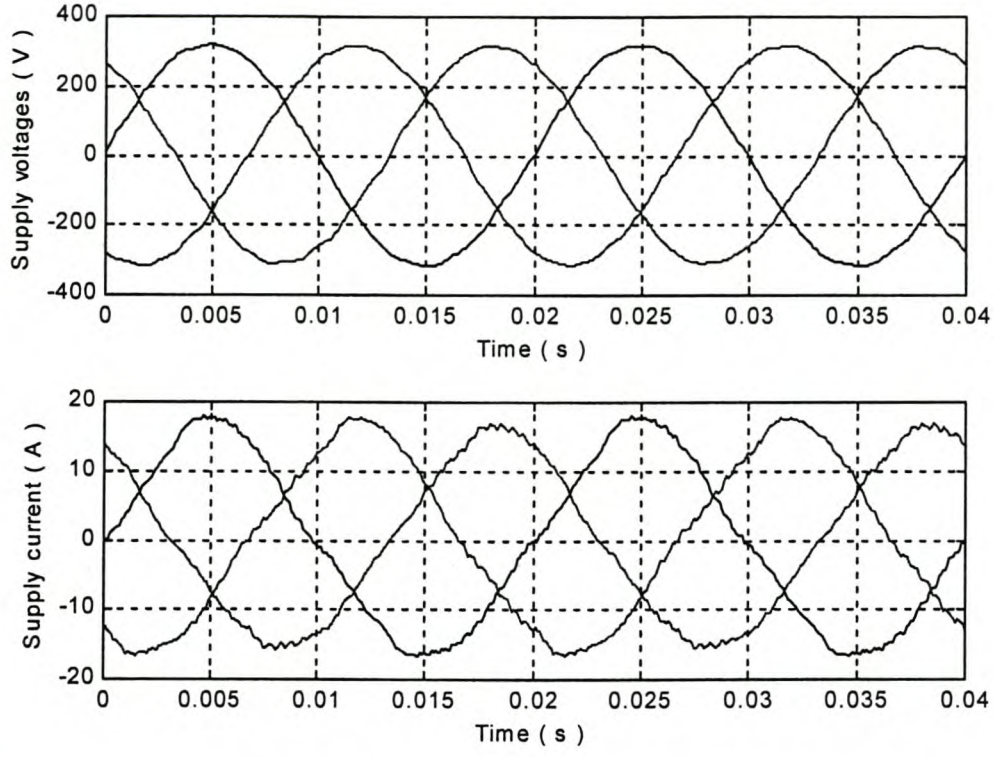


Figure 6-21: Measured three-phase supply voltages and currents of the secondary of the transformer with a balanced three-phase load.

A 40% unbalance was created by increasing the load resistance in phase *a*. With this load, the current in phase *a* is half that of phase *b* and *c*. The load currents are shown in Figure 6-22.

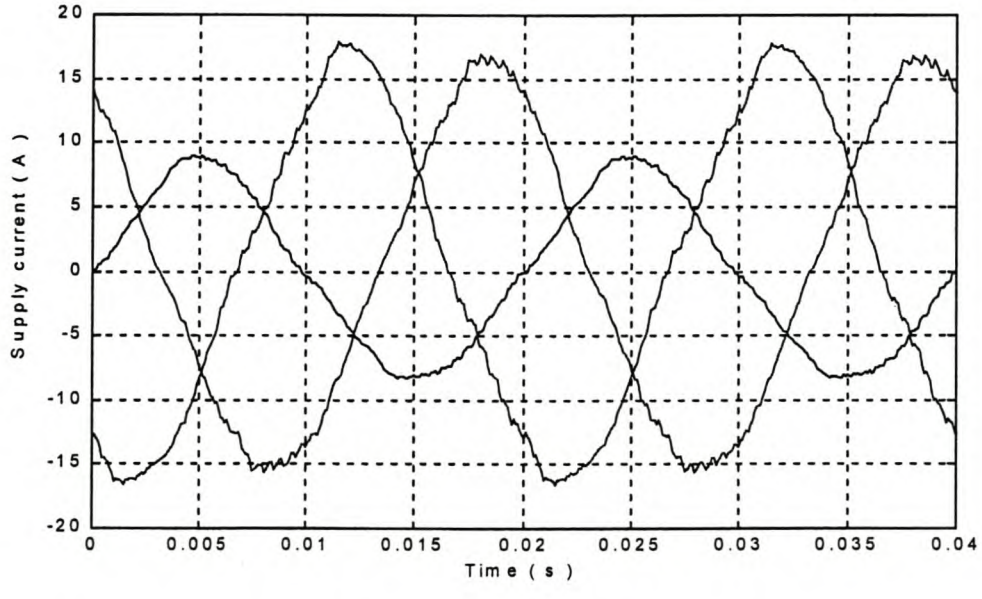


Figure 6-22: Measured unbalance in three-phase supply load current.

This 40% unbalance in the load currents causes a 2,69% unbalance in the supply voltages with an open loop voltage control method. With the proposed voltage control method and compensation loop applied, the unbalance in the supply voltages is reduced to 2%. This is a reduction of about 28% in the unbalance of the control voltages. The measured supply voltages are shown in Figure 6-23.

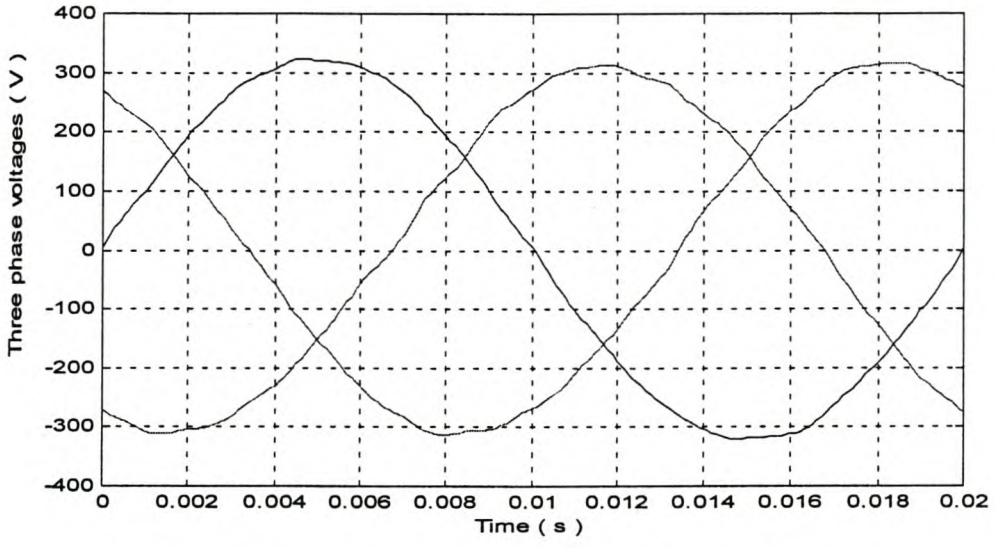


Figure 6-23: Three-phase supply voltages under unbalanced conditions using the proposed feedback control method.

Simulations were also done with the unbalanced load conditions and showed the same results as measured. The simulations also showed that, with the o-axis control included in the control system, the controller could also not completely compensate for the unbalance in supply voltages.

6.6 Non-linear loads

A 5,7 kW diode rectifier was further connected to the supply. The dc-voltage at the output of this rectifier was 520 V and the dc load current was 11 A. The measured supply voltage and current are shown in Figure 6-24.

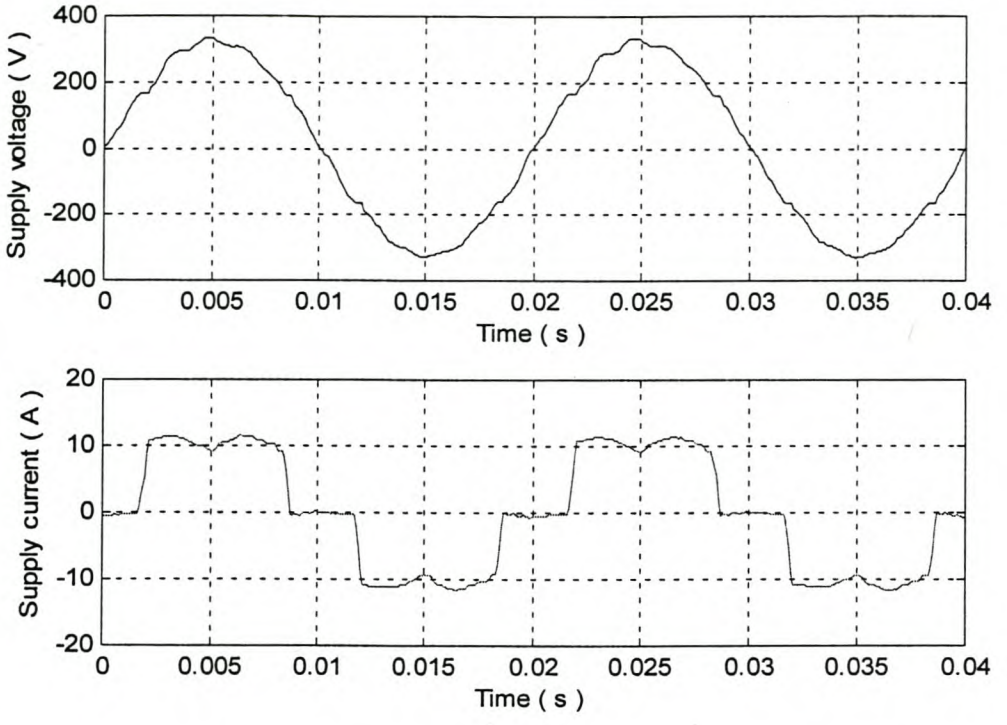


Figure 6-24: Phase *a* supply voltage and current with a diode rectifier as load.

A harmonic analysis is done on the supply voltage waveform and the results are shown in Figure 6-25. The total harmonic distortion (THD) is calculated as 3,14%, which is well within the specified limit of 8%.

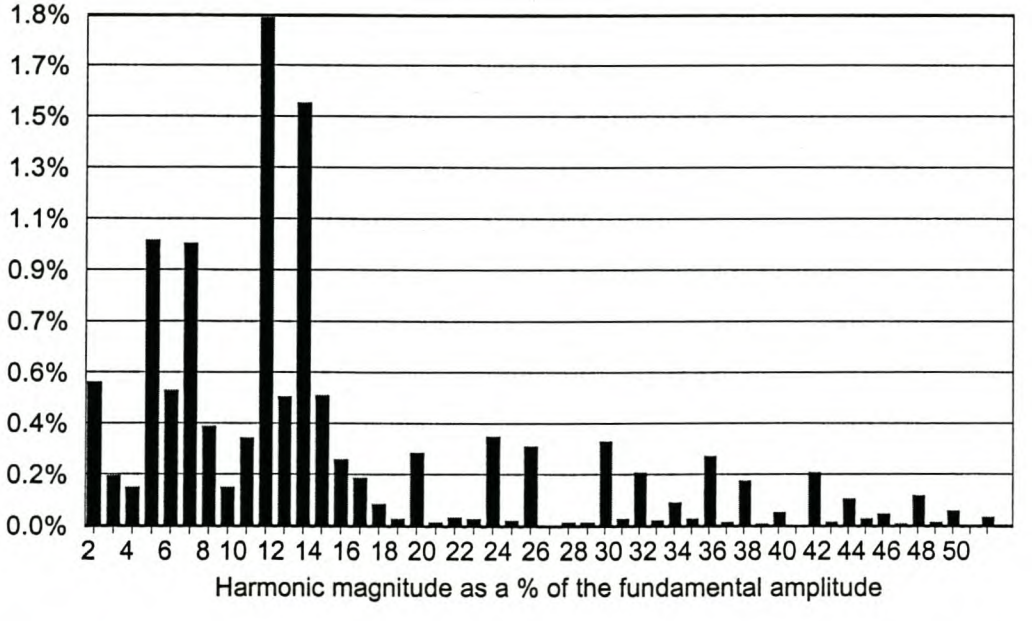


Figure 6-25: Harmonic analysis of the supply voltage waveform with a diode rectifier as load.

The results are summarised in Table 6-2 below. A significant difference in the settling time can be seen in Table 6-2 for the two voltage control methods. The alternative voltage control method shows a much slower settling time than the proposed voltage control method. Overall the alternative voltage control method and the proposed control method compare well with each other.

Table 6-2: Comparison of proposed voltage control method vs. alternative voltage control method.

	Proposed voltage control method	**Alternative control method**
THD (%)	1,2	1,8
Initial voltage drop (%)	5,5	6,5
Voltage overshoot (%)	10	10
Settling time (ms)	8	40

7 SUMMARY WITH CONCLUSIONS AND RECOMMENDATIONS

In this thesis, a new voltage control method is developed to control the output voltages of a power supply system. Different voltage control methods were studied, and from these different control methods, the proposed voltage control method is developed.

The different layout possibilities are discussed and the proposed layout topology is thoroughly motivated. The inverter topology chosen is also thoroughly motivated and compared to another inverter topology. The calculation of the filter values is done on basic calculation principles. Different transformer configurations are also discussed to show the flexibility of the system to meet the specifications demanded.

The current-regulated voltage control method and the capacitor current feedback voltage control methods are discussed and from the discussions of the two voltage control methods, the proposed voltage control method is derived. The simulation results obtained, showed that the proposed voltage controller compares very well with the current-regulated voltage control method and the capacitor current feedback voltage control method in the analogue domain.

The proposed voltage control method is also analysed in the digital domain. The decoupling terms are thoroughly discussed and by introducing a compensation loop, only the output voltages of the power supply system have to be measured. Simulations with load steps for different power factor loads were done with the digital control system and satisfactory results were obtained. The THD of the output voltages is well within the specified limit. Simulations are also done with unbalanced conditions and it was found that the proposed voltage control method did not completely compensate for the unbalanced condition, but the unbalance of the control voltages were still within the specified limits. The proposed voltage control method was compared to an alternative voltage control method and it was found that the proposed voltage control method showed better performance in general. By investigating the effect of the sampling period on the voltage responses, a case study was done with a sampling period of 100 μs to see if the performance of the system can be improved. It was found that no significant improvement on the response time of the system could be achieved if a 100 μs sampling period is used.

The digital implementation of the proposed voltage control method was discussed in detail. Some features of the TMS320F240 DSP were highlighted and the software implementation of the control algorithm was discussed in detail. A TMS320F240 DSP controller can be successfully implemented to control the output voltages of such a power supply system.

Finally, the proposed voltage control method is compared to the alternative voltage control method practically. The proposed voltage control method showed a better performance in general than the alternative voltage control method, especially under load conditions. The proposed voltage control method is also practically evaluated under unbalanced conditions and also with a non-linear load and, again, the results obtained were within the specified limits. Overall, the measured and simulated results of the proposed voltage control method and the alternative voltage control method compare in general very well. This gives confidence in the simulation method.

Some recommendations proposed are the following:

1. The proposed voltage control method should be practically evaluated at a 300 kW power level.
2. A more detailed investigation should be done to see the effect of unbalanced conditions in a three-phase power supply. A closer look should be taken to the effect of negative and zero sequence currents.
3. Simulations with a rectifier as load should also be done.
4. Ways to minimise the control loop-time in the control algorithm should be investigated to see what effect it practically has on the performance of the system.
5. Parallel operation of the power supply systems should also be investigated.
6. An investigation should be done on soft magnetic composite material to be used as the core of the inductor, as an alternative to an air-core inductor.

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9 APPENDICES

Appendix A1: Software control algorithm in C++

```
/*****************************************************************/
This program does voltage control with a high-order compensation loop
/*****************************************************************/
#include "F240.h"
volatile unsigned int *ACTR = (volatile unsigned int *) 0x7413;/* declare variables*/
volatile unsigned int *SACTR = (volatile unsigned int *) 0x7414;
volatile unsigned int *DBTCON = (volatile unsigned int *) 0x7415;
volatile unsigned int *COMPR1 = (volatile unsigned int *) 0x7417;
volatile unsigned int *COMPR2 = (volatile unsigned int *) 0x7418;
volatile unsigned int *COMPR3 = (volatile unsigned int *) 0x7419;
volatile unsigned int *COMCON = (volatile unsigned int *) 0x7411;
volatile unsigned int *GPTCON = (volatile unsigned int *) 0x7400;
volatile unsigned int *T1CON = (volatile unsigned int *) 0x7404;
volatile unsigned int *T2CON = (volatile unsigned int *) 0x7408;
volatile unsigned int *T3CON = (volatile unsigned int *) 0x740C;
volatile unsigned int *Dataout = (volatile unsigned int *) 0x8000;
volatile unsigned int *SCMPR1 = (volatile unsigned int *) 0x741A;
volatile unsigned int *SCMPR2 = (volatile unsigned int *) 0x741B;
volatile unsigned int *SCMPR3 = (volatile unsigned int *) 0x741C;
extern sine();
int fase_ap,fase_an,fase_bp,fase_bn,fase_cp,fase_cn;
int Vam,Vbm,Vcm,Va,Vb,Vc;
int indeks_cos,cos_theta,sin_theta,theta;
int indeks_cos120,indeks_cos240,indeks_sin120,indeks_sin240;
int cos_theta120,cos_theta240,sin_theta120,sin_theta240;
int theta120,theta240,stheta120,stheta240;
int Vamtempp,Vamtemp,Vbmtempp,Vbmtemp,Vcmtempp,Vcmtemp;
int Vdm,Vqm,Vom;
int errorq,errorq_1,errorq_2,errord,errord_1,errord_2;
int cos_thetat,cos_theta120t,sin_thetat,sin_theta120t;
```

```
int cos_theta240t,sin_theta240t,aT;
int Varef,Vbref,Vcref,gs,gst,Vgst_1,Vgsref,Vgsref_1,aTgs,Vgst;
int Vaol,Vbol,Vcol,Vdol,Vqol,Vtest;
float PIDoutdd,PIDoutqq;
int PIDoutd,PIDoutq;
int InvGzd,InvGzq;
int Refcompd,Refcompq;
int Vcompd_1,Vcompdf,Vcompd,Vcompq_1,Vcompqf,Vcompq;
int Vdm_1,Vdm_2,Vqm_1,Vqm_2;
int Vddref,Vdreff,Vqreff;
int Vdref,Vqref;
float PIDd_1,PIDq_1;
int Piddd,Pidqq,Pidd,Pidq,Timer1,Timer2,Timer3;
int d;
void main(void)

/************************ Main Program Starts **********************/
{
  int indeks,indeks_a,indeks_b,indeks_c;

  *OCRA = 0x0705;                    /*select multiplexed channels*/
  *PBDATDIR |= 0x7878;               /* disable all D2A channels */
  *DBTCON = 0x0;                     /* Deadtime = 0us*/
  *COMCON = 0x0307;                  /* set compare control register*/
  *COMCON = 0x8307;                  /* initialise register */
  *ACTR = 0x0666;                    /* Make PWM1/3/5 active high */
  *SACTR = 0x002A;
  *GPTCON = 0x0055;
  *T1PR = 0x09C4;                    /* switching frequency = 4 kHz*/
  *T1CMPR = 0x0;                     /* active in compare mode */
  *T1CNT = 0x0;                      /* initialise counter */
  *T2PR = 0x61A8;                    /* set-up look-up table counter */
  *T2CON = 0xD4C2;                   /* initialise register - prescaler x/16*/
```

```
*T2CNT = 0x0;
*T3PR = 0x036B;                    /* counter to synchronise loop-time*/
*T3CON = 0xEAC2;                   /* initialise register - prescaler x/4*/
*T3CNT = 0x0;                      /* initialise counter*/
*T3CMPR = 0x02EE;                  /* active in compare mode */
*T1CON = 0xE803;                   /* set timer control register*/
*T1CON = 0xE843;                   /* initialise register*/
ADCTRL2 -> ADCPSCALE = 0;          /* Prescale value = 0 */
ADCTRL2 -> ADCEVSOC = 0;
ADCTRL2 -> ADCEXTSOC = 0;
ADCTRL1 -> ADCIMSTART = 0;         /* no immediate start*/
ADCTRL1 -> ADCINTEN = 1;           /* disable interrupt */
ADCTRL1 -> ADCCONRUN = 0;          /* single conversion */
ADCTRL1 -> ADC2EN = 0;             /* en/dis(0)-able ADC2 */
ADCTRL1 -> ADC1EN = 0;             /* enable ADC1 */
ADCTRL1 -> suspend_free = 0;       /*  */
ADCTRL1 -> suspend_soft = 1;       /* complete conversion before halting*/

/********************** Initialise variables **********************/
Vdm_1 = 0;
Vdm_2 = 0;
Vqm_1 = 0;
Vqm_2 = 0;
errorq_1 = 0;
errorq_2 = 0;
errord_1 = 0;
errord_2 = 0;
PIDd_1 = 0;
PIDq_1 = 0;
Vcompd_1 = 0;
Vcompq_1 = 0;
Vcompd = 0;
Vcompq = 0;
```

```
Vgsref = 0;
Vgsref_1 = 0;
Vdol = 0;
Vqol = 0;
Vqref = 0;
 ADCTRL1 -> ADC2EN = 1;              /* en/dis(0)-able ADC2 */
ADCTRL1 -> ADC1EN = 1;               /* enable ADC1 */
for(;*T1CNT != 0;)                   /* start when  counter is zero*/
{};
for (;;)
{
      *PBDATDIR &= 0xFFF7;           /* select D2A channel */
      *Dataout = 0;                  /* puts data on databus */
      *PBDATDIR |= 0x0008;           /* set write_enable */
   ADCTRL1 -> ADC1CHSEL = 0;         /* select channel to be sampled*/
   ADCTRL1 -> ADCSOC = 1;            /* start conversion*/
   while (ADCTRL1 -> ADCINTFLAG == 0);
      ADCTRL1 -> ADCINTFLAG = 1;
      gst = *ADCFIFO1;               /* data in ADCFIF01/2 */
      gs = gst>>6;                   /*Shifts 6 places to right-10 bit decoder*/
      gs &= 0x03FF;                  /* clear 6 MSB*/
      Vdol = gs;
   Vdref= Vdol;
ADCTRL1 -> ADC1CHSEL = 2;     /* select channel to be sampled*/
   ADCTRL1 -> ADC2CHSEL = 5;         /* select channel to be sampled*/
   ADCTRL1 -> ADCSOC = 1;            /* start conversion*/
   while (ADCTRL1 -> ADCINTFLAG == 0);
      ADCTRL1 -> ADCINTFLAG = 1;
      Vamtempp = *ADCFIFO1;          /* data in ADCFIF01/2 */
   Vbmtempp = *ADCFIFO2;             /* data in ADCFIF01/2 */
      Vamtemp = Vamtempp>>6;         /* Shift 6 places to right-10 bit decoder*/
      Vamtemp &= 0x03FF;             /* clear 6 msb*/
   Vam = Vamtemp - 512;
```

```
    Vbmtemp = Vbmtempp>>6;          /* Shift 6 places to right-10 bit decoder*/
      Vbmtemp &= 0x03FF;            /* clear 6 msb*/
    Vbm = Vbmtemp - 512;
    ADCTRL1 -> ADC1CHSEL = 3;       /* select channel to be sampled*/
      ADCTRL1 -> ADCSOC = 1;        /* start conversion*/
    while (ADCTRL1 -> ADCINTFLAG == 0);
      ADCTRL1 -> ADCINTFLAG = 1;
      Vcmtempp = *ADCFIFO1;         /* data in ADCFIF01/2 */
    Vcmtemp = Vcmtempp>>6;          /* Shift 6 places to right-10 bit decoder*/
      Vcmtemp &= 0x03FF;            /* clear 6 msb*/
    Vcm = Vcmtemp - 512;
    Vam = Vam;
    Vbm = Vbm;
    Vcm = Vcm;

indeks = *T2CNT/5;                  /* Begin to generate references */
    indeks_cos = indeks + 1250;     /* shifts 120 degrees*/
    if (indeks_cos > 5000)
    { theta = indeks_cos - 5000;}
    else
    {theta = indeks_cos;}
    indeks_cos120 = indeks + 2917;  /* shifts 120 degrees*/
    if (indeks_cos120 > 5000)
    { theta120 = indeks_cos120 - 5000;}
    else
    {theta120 = indeks_cos120;}
    indeks_sin120 = indeks + 1667;  /* shifts 120 degrees*/
    if (indeks_sin120 > 5000)
    { stheta120 = indeks_sin120 - 5000;}
    else
    {stheta120 = indeks_sin120;}
    indeks_cos240 = indeks + 4584;  /* shifts 120 degrees*/
    if (indeks_cos240 > 5000)
```

```
{ theta240 = indeks_cos240 - 5000;}
else
{theta240 = indeks_cos240;}
indeks_sin240 = indeks + 3334;          /* shifts 120 degrees*/
if (indeks_sin240 > 5000)
{ stheta240 = indeks_sin240 - 5000;}
else
{stheta240 = indeks_sin240;}
cos_thetat = sine(theta);
cos_theta120t = sine(theta120);
sin_thetat  = sine(indeks);
sin_theta120t = sine(stheta120);
cos_theta240t = sine(theta240);
sin_theta240t = sine(stheta240);
cos_theta =  cos_thetat/32;
cos_theta120 = cos_theta240t/32;
sin_theta  = sin_thetat/32;
sin_theta120 = sin_theta240t/32;
cos_theta240 = cos_theta120t/32;
sin_theta240 = sin_theta120t/32;
   Timer2 = *T2CNT/8;
   Timer3 = *T3CNT;

Va = Vam/16;                            /* Scale values to do conversion */
Vb = Vbm/16;
Vc = Vcm/16;
Vdm = (Va*cos_theta + Vb*cos_theta120 + Vc*cos_theta240); /* ABC to DQO
Vdm = (Vdm*2)/3;
Vdm = Vdm/4;
Vqm = (Va*sin_theta + Vb*sin_theta120 + Vc*sin_theta240); /* ABC to DQO */
Vqm = (Vqm*2)/3;
Vqm = Vqm/4;
Va = Va*16;                             /* scale back after conversion*/
```

```
    Vb = Vb*16;
    Vc = Vc*16;
    errord = (Vdref - Vdm)*4;              /* error D */
      errorq = (Vqref - Vqm)*4;            /* error Q */
 /********************* floating-point calculations ********************/
PIDoutdd=0.18161*errord-0.33599*errord_1+0.155051*errord_2+ PIDd_1;
PIDoutqq = 0.18161*errorq - 0.33599*errorq_1 + 0.155051*errorq_2 + PIDq_1;
PIDd_1 = PIDoutdd;                         /* Update variables*/
PIDq_1 = PIDoutqq;
errorq_2 = errorq_1;
erorq_1 = errorq;
erord_2 = errord_1;
erord_1 = errord;
PIDoutd = (int) PIDoutdd;                  /* Convert from floating to integer*/
PDoutq = (int) PIDoutqq;
Piddd = PIDoutd;
Pidqq = PIDoutq;
InvGzd = (Vdm*3)/5 - Vdm_1 + (Vdm_2*2)/5;      /* Inverse of G(z) */
InvGzq = (Vqm*3)/5 - Vqm_1 + (Vqm_2*2)/5;      /* Inverse of G(z) */
Vdm_2 = Vdm_1;                             /* update variables*/
Vdm_1 = Vdm;
Vqm_2 = Vqm_1;
Vqm_1 = Vqm;
      Refcompd = Piddd + Vcompd;           /* Initial d-compensation */
      Refcompq = Pidqq + Vcompq;           /* Initial q-compensation */
      Vcompdf = Refcompd - InvGzd;         /* compensation d-error */
     Vcompqf = Refcompq - InvGzq;          /* compensation q-error */
      aT = 2;
      Vcompd = Vcompd_1 - ((Vcompd - Vcompdf)/aT); /* d lowpass flter*/
      Vcompq = Vcompq_1 - ((Vcompq - Vcompqf)/aT); /* q lowpass flter*/
      Vcompd_1 = Vcompd;
      Vcompq_1 = Vcompq;
      Refcompd = Piddd + Vcompd + Vdm;     /* Add decoupling voltages*/
```

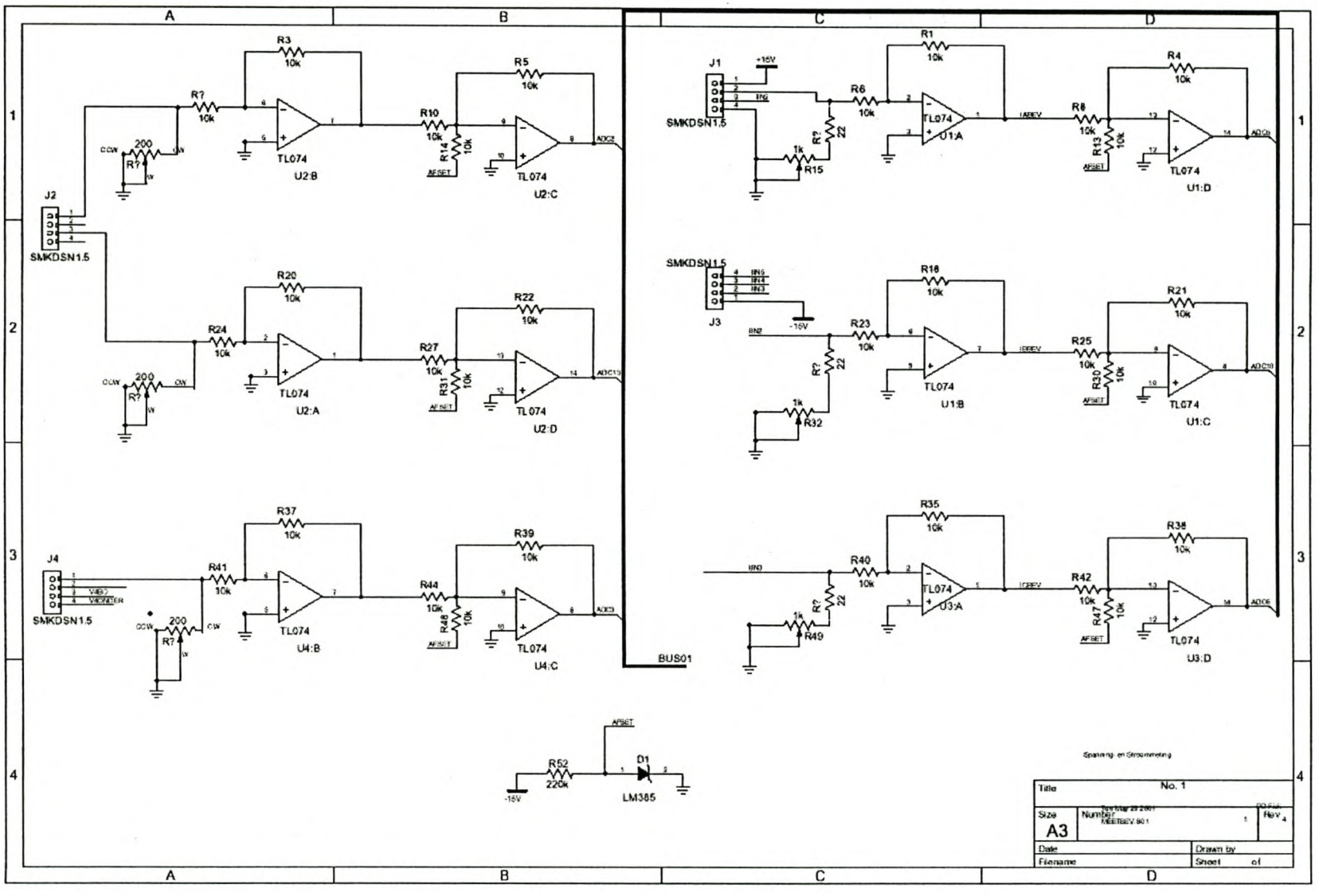
```
    Refcompq = Pidqq + Vcompq + Vqm;        /* Add decoupling voltages*/
    Refcompd = Refcompd/4;
    Refcompq = Refcompq/4;
      Varef = (Refcompd*cos_theta + Refcompq*sin_theta);/* phase A reference */
    Varef = Varef/16;
    Vbref = (Refcompd*cos_theta120 + Refcompq*sin_theta120); /* phase B
reference */
    Vbref = Vbref/16;
    Vcref = (Refcompd*cos_theta240 + Refcompq*sin_theta240); /* phase C
reference */
    Vcref = Vcref/16;
    Refcompd = Refcompd*4;
    Refcompq = Refcompq*4;
    fase_ap = Varef + 1250;                 /* set offset */
    if (fase_ap > 2490)
    { fase_ap = 2490;}
    if (fase_ap < 10)
    { fase_ap = 10;}
    *COMPR1 = fase_ap;                      /* set duty cycle*/
    fase_an = -Varef + 1250;                /* set offset */
    if (fase_an > 2490)
    { fase_an = 2490;}
    if (fase_an < 10)
    { fase_an = 10;}
    *SCMPR1 = fase_an;                      /* set duty cycle*/
    fase_bp = Vbref + 1250;                 /* set ofset */
    if (fase_bp > 2490)
    { fase_bp = 2490;}
    if (fase_bp < 10)
    { fase_bp = 10;}
    *COMPR2 = fase_bp;                      /* set duty cycle*/
    fase_bn = -Vbref + 1250;                /* set ofset */
    if (fase_bn > 2490)
```

```
        { fase_bn = 2490;}
        if (fase_bn < 10)
        { fase_bn = 10;}
        *SCMPR2 = fase_bn;              /* set duty cycle*/
        fase_cp = Vcref + 1250;         /* set offset*/
        if (fase_cp > 2490)
        { fase_cp = 2490;}
        if (fase_cp < 10)
        { fase_cp = 10;}
        *COMPR3 = fase_cp;              /* set duty cycle*/
        fase_cn = -Vcref + 1250;
        if (fase_cn > 2490)
        { fase_cn = 2490;}
        if (fase_cn < 10)
        { fase_cn = 10;}
        *SCMPR3 = fase_cn;
for(;*T1CNT > 5;)                       /* wait until loop is finished*/
        {};
        *PBDATDIR &= 0xFFF7;                    /* select D2A channel */
          *Dataout = 2000;                      /* puts data on databus */
          *PBDATDIR |= 0x0008;                  /* set write_enable */
        *PBDATDIR &= 0xFFEF;                    /* select D2A channel */
          *Dataout = Vdm*2;                     /* puts data on databus */
          *PBDATDIR |= 0x0010;                  /* set write_enable */
        *PBDATDIR &= 0xFFDF;                    /* select D2A channel */
          *Dataout = Vqm*2 + 1000;              /* puts data on databus */
          *PBDATDIR |= 0x0020;                  /* set write_enable */
        *PBDATDIR &= 0xFFBF;                    /* select D2A channel */
          *Dataout = Vdref*4;                   /* puts data on databus */
          *PBDATDIR |= 0x0040;                  /* set write_enable */
    }
}
```

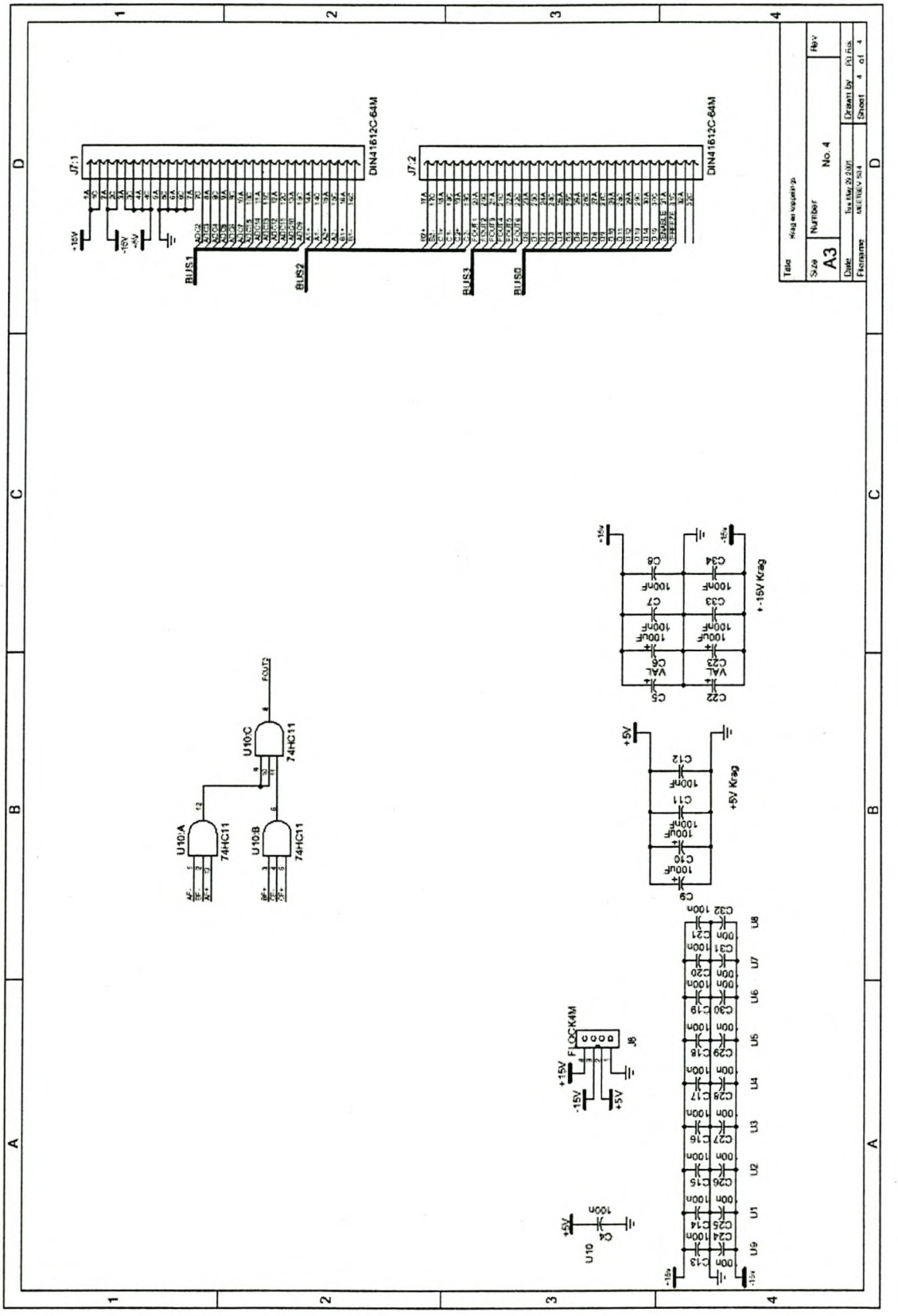
Appendix A2: Program to calculate look-up table.

```
program leer;
uses Crt;
var F: Text;
   i,k : integer;
   x,y : real;
begin
 Assign(F, 'c:\dspprog\sin.tab');
 Rewrite(F);
 for i := 0 to 5000 do
    begin
     x := i/795.7747156;
     y := 2000*sin(x);
     k := round(y);
     Writeln(F, '    .int  ',k);
    end;
 Close(F);
end.
```

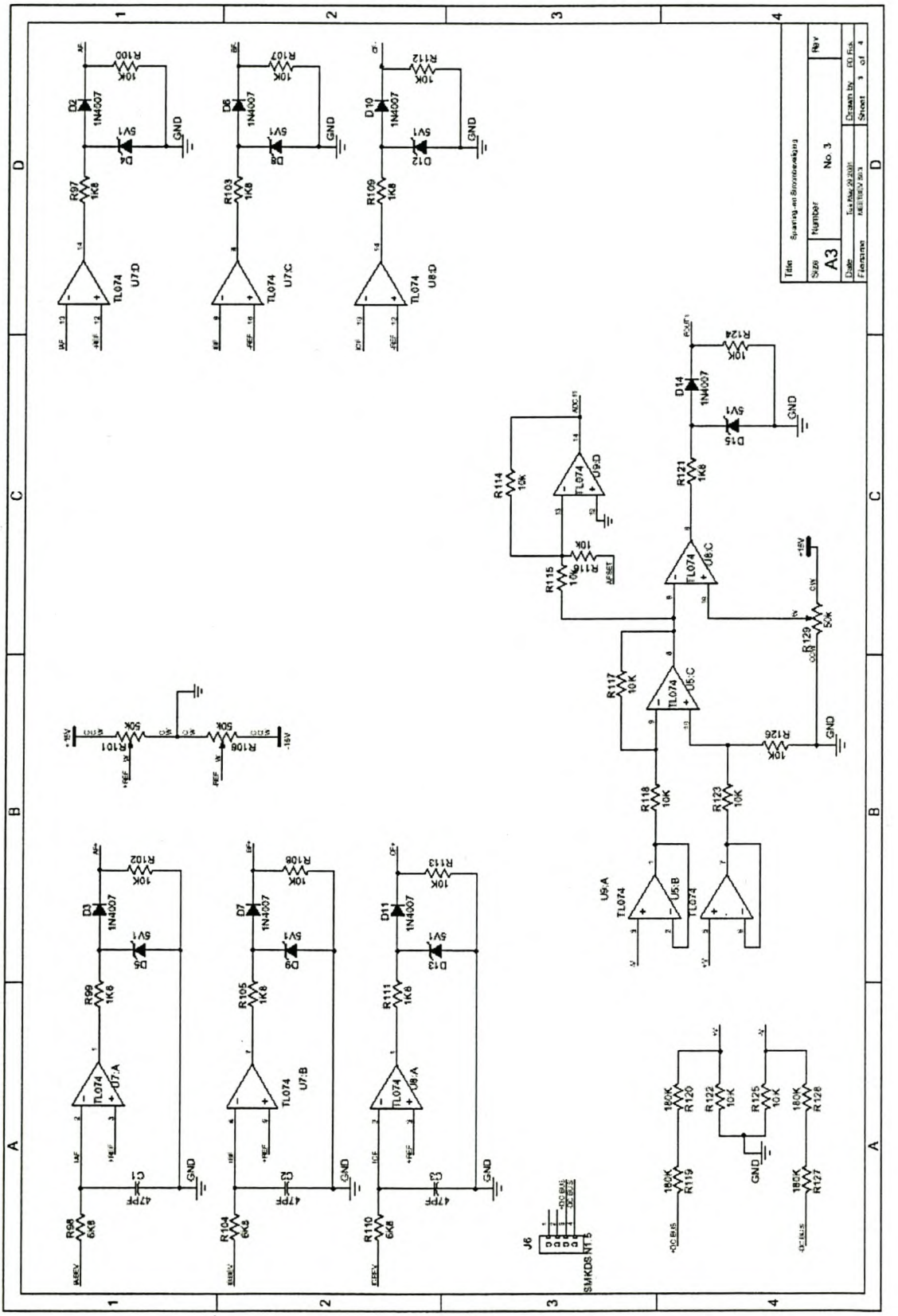
Appendix B1: Schematic of measurement card.



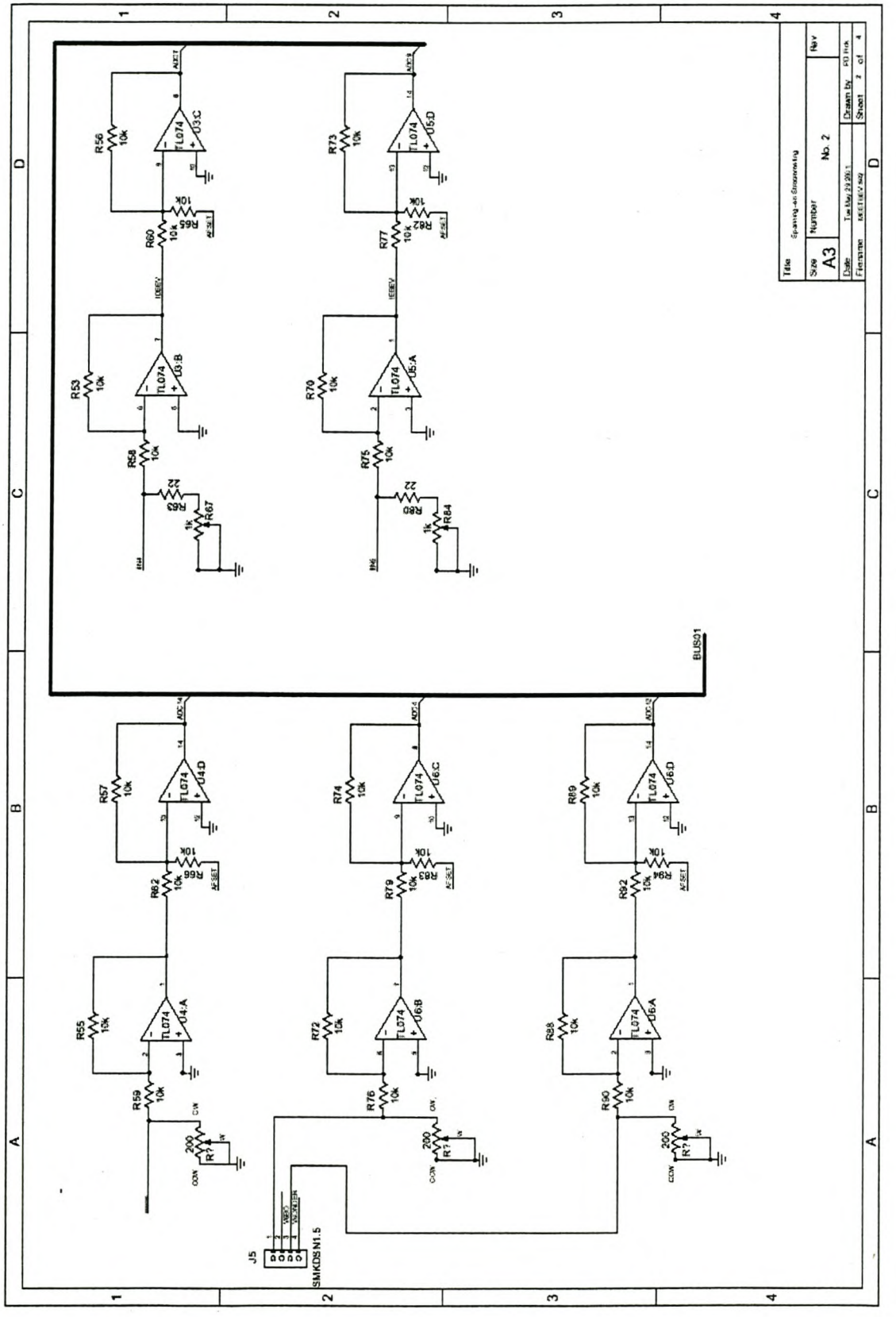
Appendix B2: Schematic of measurement card– logic gates.



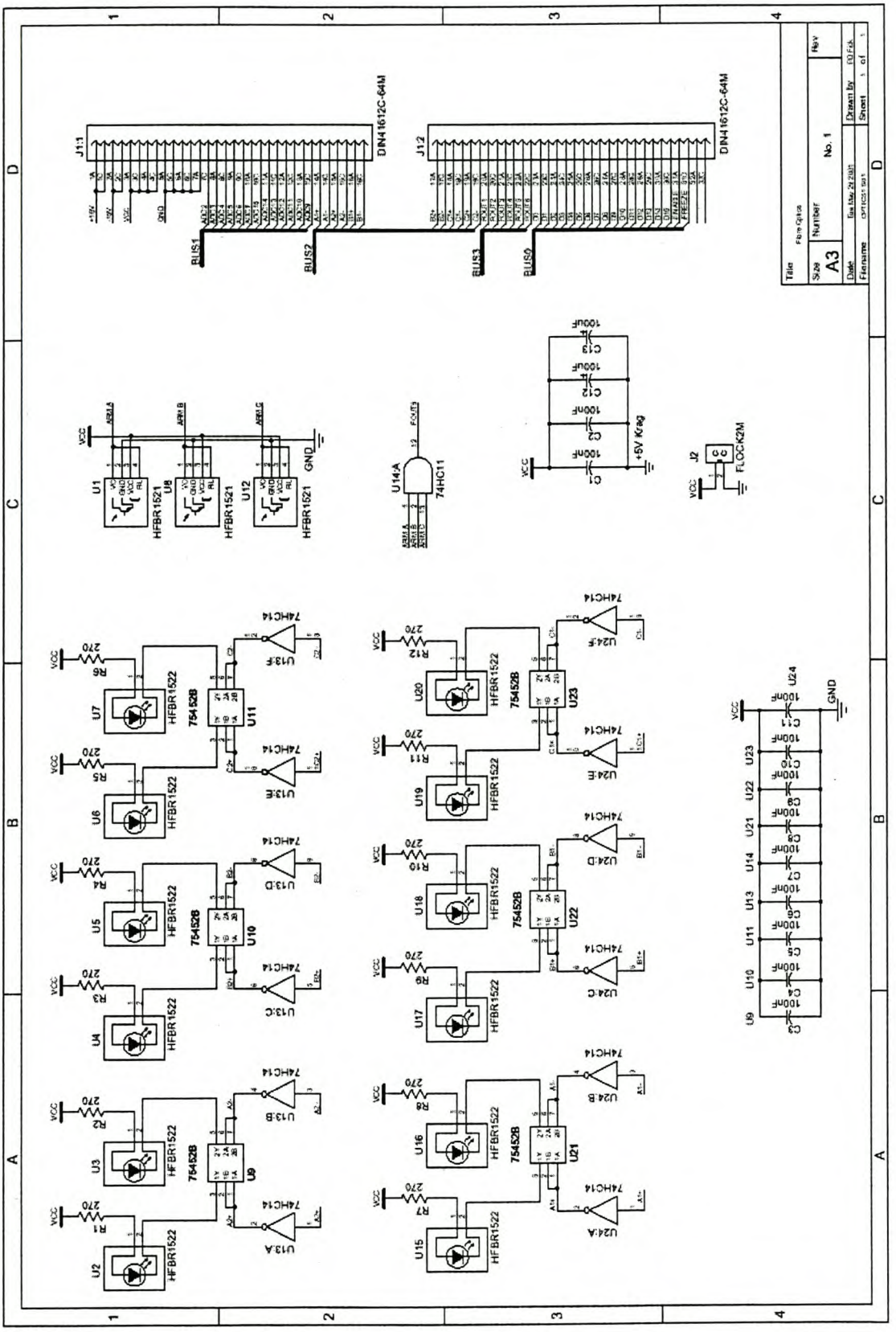
Appendix B3: Schematic for measurement card – over current-and voltage protection.



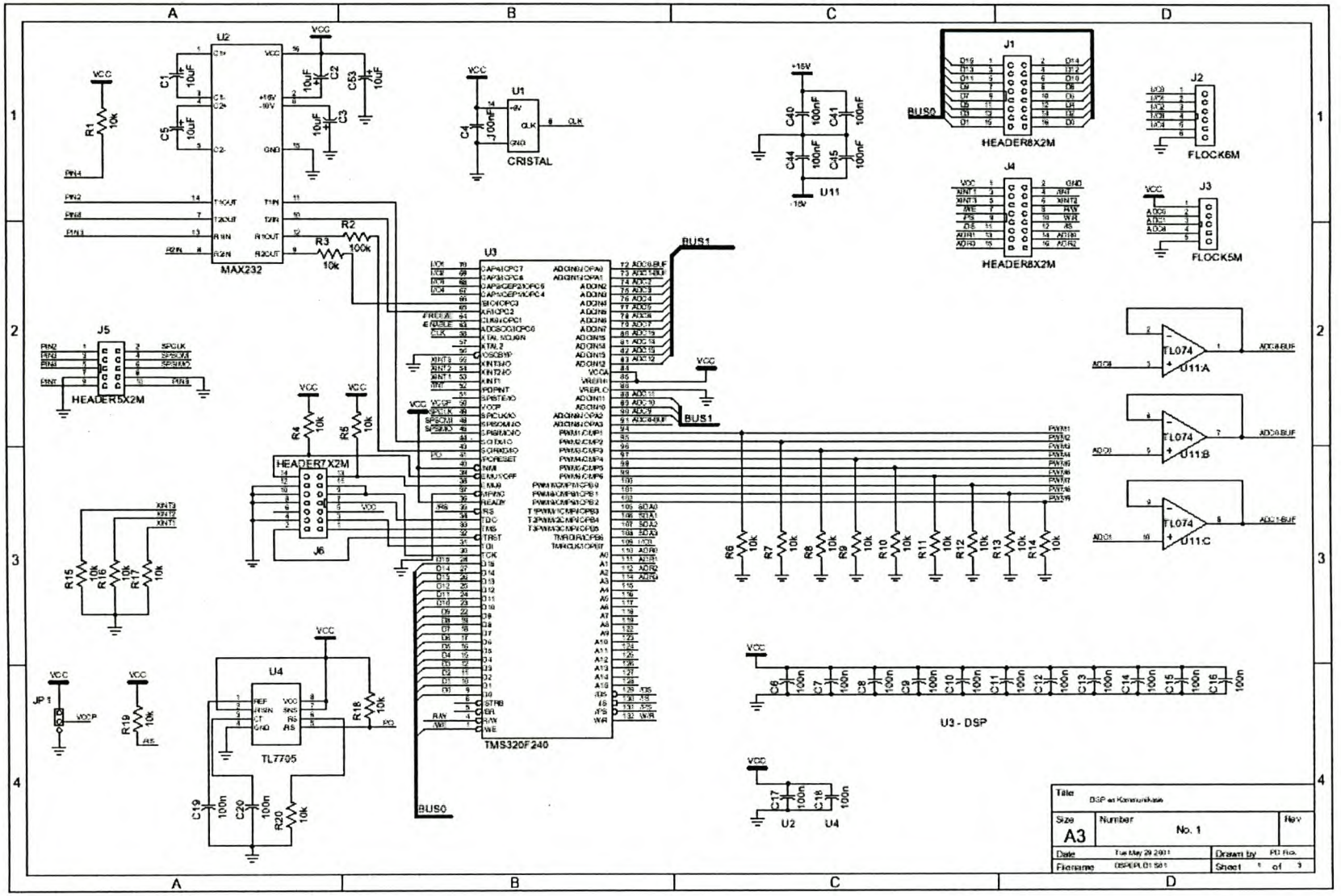
Appendix B4: Schematics of measurement card – voltage- and current measurements.



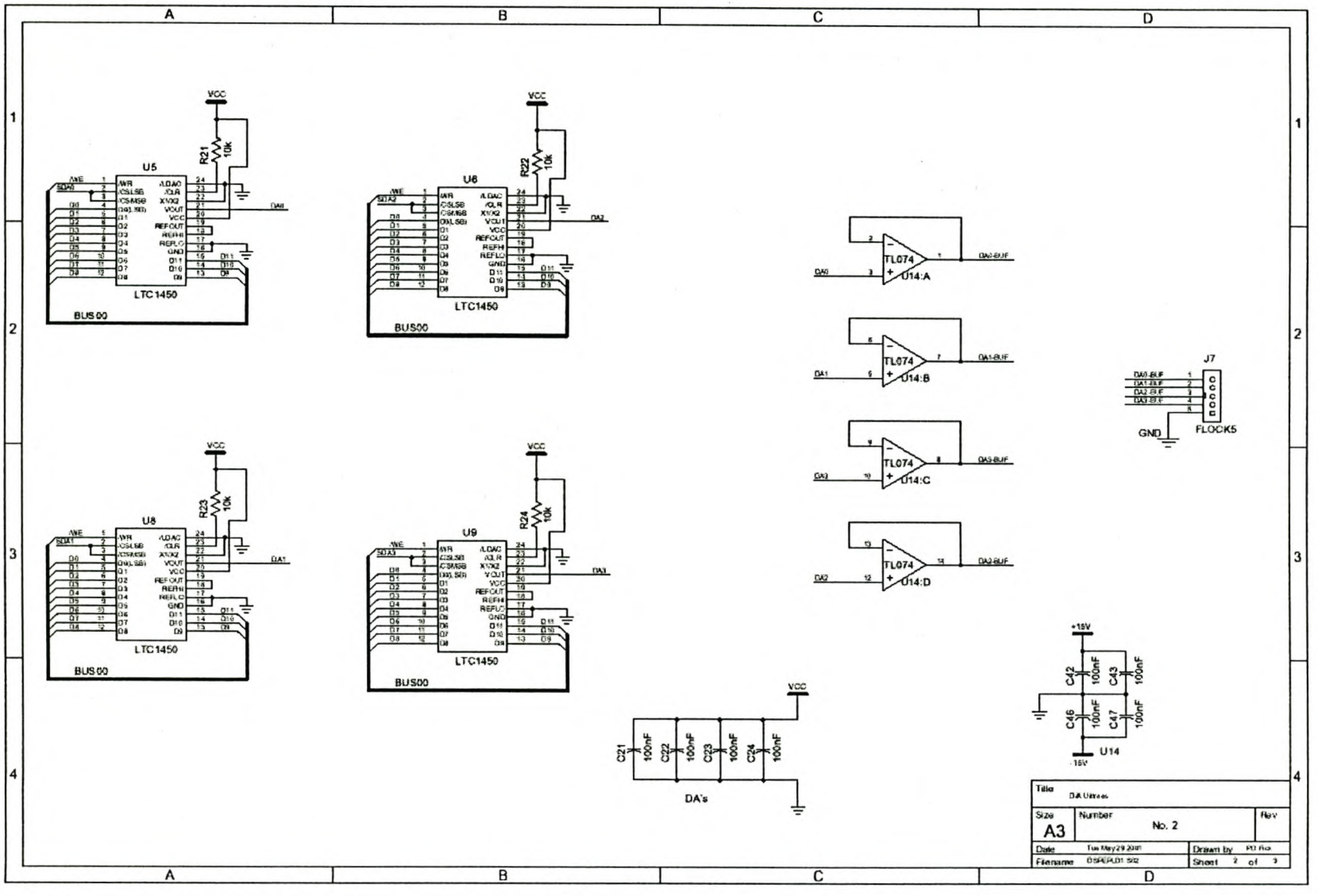
Appendix B5: Schematics of fibre-optics card



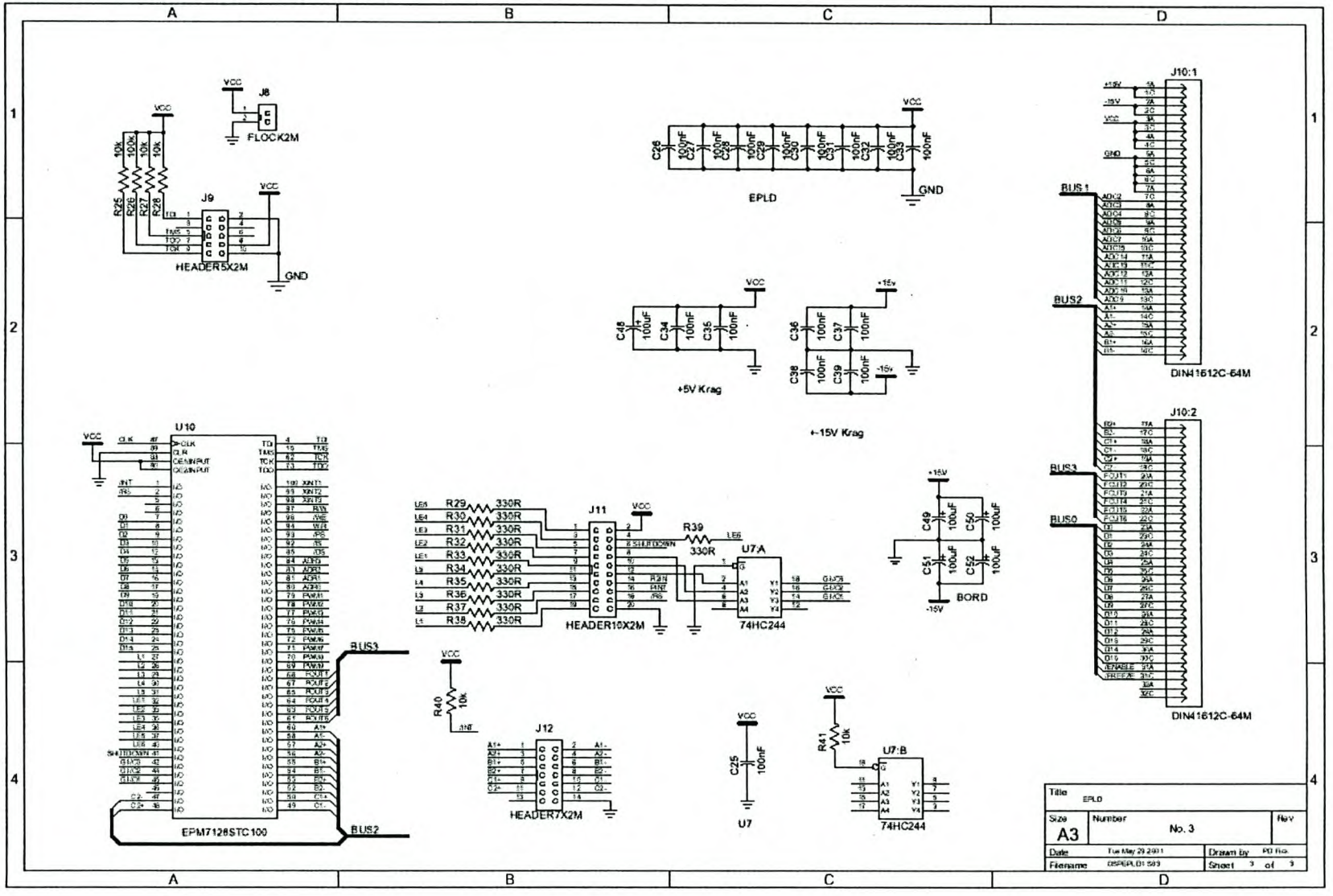
Appendix B6: Schematic of DSP control card



Appendix B7: Schematic of DSP card – D/A



Appendix B8: Schematics of DSP card – EPLD.



Appendix C1: Matlab program to design analogue PID controller.

```
C = 140e-6;
L = 500e-6;
R = 0.025;
k = 0;
Kp = 1;
Ki = 400;
A = 120;
while k ~= 1;
numGG = [Kp ((A*Kp)+Ki) (Ki*A)];
denGG = [(L*C) (R*C) 0 0];
HGG = tf(numGG,denGG);
rlocus(HGG);
grid;
pause;
[K,po] = rlocfind(HGG);
pause;
Kpl = K;
disp([‘                    ‘])
disp([‘ Kd = ‘,num2str(Kpl*Kp)])
disp([‘ Ki = ‘,num2str(Kpl*A*Ki)])
disp([‘ Kp = ‘,num2str(Kpl*((Kp*A)+Ki))])
disp([‘                    ‘])
HGK = Kpl*HGG;
HGfb = feedback(HGK,1,-1);
step(HGfb);
pause;
close;
k = input(‘Terminate program? - press "1" and then ENTER: ‘);
end
disp([‘End of program...’])
```

Appendix C2: Matlab program to design digital PID controller.

```
C = 140e-6;
L = 500e-6;
R = 0.025;
k = 0;
Kpt = 1;
Kit = 300;
A = 100;
Ts = 250e-6;
Zcomp = exp(-Ts*(Kit/Kpt))
Pcomp = exp(-Ts*(A))
while k ~= 1;
numGG = [Kpt ((A*Kpt) + Kit) (Kit*A)];
denGG = [(L*C) (R*C) 0 0];
HGG = tf(numGG,denGG);
HGGz = c2d(HGG,Ts,'zoh');
rlocus(HGGz);
zoom on;
pause;
grid;
[Kt,po] = rlocfind(HGGz);
pause;
Kpl = Kt;
Kds = Kpl*Kpt;
Kis = Kpl*A*Kit;
Kps = Kpl*((Kpt*A)+Kit);
disp([‘                ‘])
disp([‘ Z = ‘,num2str(Zcomp)])
disp([‘ P = ‘,num2str(Pcomp)])
disp([‘                ‘])
disp([‘ Kd = ‘,num2str(Kds)])
```

```
disp([' Ki = ',num2str(Kis)])
disp([' Kp = ',num2str(Kps)])
disp(['                    '])
disp([' Z = ',num2str((Kps+(Kis*Ts)+(Kds/Ts)))])
disp([' Z0 = ',num2str((Kps+((2*Kds)/Ts)))])
disp([' Z_1 = ',num2str((Kds/Ts))])
disp(['                    '])
close;
pause;
HGzK = Kpl*HGGz;
HGfb = feedback(HGzK,1,-1);
step(HGfb);
grid;
pause;
close;
k = input('Terminate program? - press "1" and then ENTER: ');
end
disp(['                    '])
disp(['End of program...'])
```

Appendix C3: Matlab program to design digital PID controller with feedback loop.

```
C = 140e-6;
L = 0.5e-3;
R = 0.3;
k = 0;
Kpt = 1;
Kit = 1000;
A = 600;
Ts = 250e-6;
while k ~= 1;
numGG = [Kpt ((A*Kpt) + Kit) (Kit*A)];
denGG = [(L*C) (R*C) 1 0];
HGG = tf(numGG,denGG);
HGGz = c2d(HGG,Ts,'zoh');
rlocus(HGGz);
zoom on;
pause;
grid;
[Kt,po] = rlocfind(HGGz);
pause;
Kpl = Kt;
Kds = Kpl*Kpt;
Kis = Kpl*A*Kit;
Kps = Kpl*((Kpt*A)+Kit);
disp([‘                ‘])
disp([‘ Kd = ‘,num2str(Kds)])
disp([‘ Ki = ‘,num2str(Kis)])
disp([‘ Kp = ‘,num2str(Kps)])
disp([‘                ‘])
disp([‘ Kds/Ts = ‘,num2str(Kds/Ts)])
disp([‘ KiTs = ‘,num2str(Kis*Ts)])
```

```
disp([' Kps = ',num2str(Kps)])
disp(['                    '])
disp([' Z = ',num2str((Kps+(Kis*Ts)+(Kds/Ts)))])
disp([' Z0 = ',num2str((Kps+((2*Kds)/Ts)))])
disp([' Z_1 = ',num2str((Kds/Ts))])
disp(['                    '])
close;
pause;
HGzK = Kpl*HGGz;
HGfb = feedback(HGzK,1,-1);
step(HGfb);
grid;
pause;
close;

k = input('Terminate program? - press "1" and then ENTER: ');
end
disp(['                    '])
disp(['End of program...'])
```

Appendix D: Matlab program for inductor design.

```
%%%%%%  Claculate the number of turns required%%%%%%%%%%%%%%%
length_wire = 75.4e-3;                  % length of wire (m) - with insulation
par = 3;                                % Number of wires in parallel
b = [length_wire*par*100];              % radial dimension
cdb = [0.1];                            % choose for size of coil
cd2a = [0.1];                           % choose for size of coil
thick_wire = 0.9e-3;                    % thickness of wire (m) - with insulation
thick = 0.5;                            % thickness of wire (mm) - without insulation
lenth = 75;                             % length of wire (mm) - without insulation
coils = 1;                              % Number of coils
k = [0.0608];                           % k compensates for the decrease in inductance
                                        % due to the separation of the windings
p20 = 1.673e-8;                         % Resistivity (ohm.m) - 20 degrees celsius
K = [0.688123];                         % Nagaoka's constant
L = 250;                                % required inductance (uH)
c = b.*cdb;                             % axial dimension of cross section
a = c./(2*cd2a);                        % mean radius of turns
bd2a = b./(2*a);                        % from this, choose K - Nagaoka's constant
a2db = 1/bd2a;
fs = 10000;                             % switching frequency
Imaks = 250;                            % Maximum 50 Hz RMS current
Imaks_fs = 42.26;                       % maximum 10 kHz RMS current
faktor = 2.*a./b;                       % define ratio
K_aks = K - k;                          % Compensating factor
N = sqrt(L/(0.019739.*faktor.*a.*K_aks));  % number of turns for a given inductance

%%%%%% Calculate the 50 Hz losses and 10 kHz losses in the inductor%%%%%%
Yt = 0.0039;                            % change of resistivity per degrees celsius
Rated_temp = 75;                        % rated temperature
p75 = p20*(1 + Yt*(Rated_temp - 20));       % Resistivity at rated temperature
radius = a;                             % mean radius of coil
l = (2*pi*radius*N)/100;                % mean length of conductor
```

```
Area_plate = thick_wire*length_wire;        % Total area of copper plate - with insulation
insulation = 0.2e-3;                        % thickness of insulation
windings_coil = round(N/coils);             % Number of windings per coil
Tot_area = (b*10*c*10);                     % Total area of conductors - with insulation
Copper_area = ((lenth*par*coils)*(windings_coil*thick)); % Total copper area - without insulation
Cop_area = ((lenth*1e-3*par)*(thick*1e-3)); % Copper area of one conductor
Kf = Copper_area/Tot_area;                  % Fill factor
R50 = ((p75*l)/Cop_area)*1000;              % equivalent dc-resistance;
Uo = 4*pi*1e-7;                             % permeability of air
Ur = 1.00745;                               % relative permeability of copper
roo = 5.8e7;                                % conductivity of copper
skin_depth = sqrt((2/(2*pi*fs*Uo*Ur*roo))); % skin depth at 10 kHz - m
skin_depth50 = sqrt((2/(2*pi*50*Uo*Ur*roo))); % skin depth at 50 Hz - m
R2000 = R50;
P2000 = (((Imaks_fs^2)*R2000)/Kf);          % Losses due to switching frequency
P50 = (((Imaks^2)*(R50/1000))/Kf);          % 50 Hz losses in Watts
Ptot = P50*1000 + P2000;                    % Total losses

%%%%%%%%%% Calculate the mass of the inductor %%%%%%%%%%%%
r1 = a + (c/2);                             % outer radius of coil
r2 = a - (c/2);                             % innner radius of coil
Volume1 = pi*r1^2*b;
Volume2 = pi*r2^2*b;
Volume_tot = Volume1 - Volume2;             % Total volume of the conductor area
density_copper = 8.92;                      % mass density of copper (g/cm^3)
C_J = Copper_area/N;                        % Copper area of one conductor
J = Imaks/C_J;                              % Current density - A/mm^2
mass = (density_copper*Volume_tot/1000);    % Mass of inductor
koste = 22;                                 % R/kg
tot_koste = koste*mass;                     % Cost of inductor
```

```
c_needed = windings_coil*thick*1e-3*100;  % The value of c needed to fit
                                          % in the windings
c_neededd = windings_coil*thick_wire*100;% The value of c with insulation
Copper_volume = (Ptot/Volume_tot)*Kf;
Ta = 30;
deltaT = Rated_temp - Ta;
A1 = 2*pi*(r1/100)*(b/100);
A2 = 2*pi*(r2/100)*(b/100);
A3 = 2*pi*((r1/100-r2/100))^2;
A_outside = A1 + A2 + A3;                 % Outside surface area
```

Appendix E: Matlab program to calculate harmonics.

```
clear all;
tic;
echo on;
load thd.out;                          % load Simuwin - outputfile
echo off;
ptemp = thd(:,2);                      % voltage matrix
N_har = 8;
begin = 20000;
param = ptemp(begin-10000:begin);
parameter = param;
aantal_harmonics = 0;
n = 0;                                 % initial values
p = 0;                                 % initial values
k=0;
x = length(parameter);                 % number of points
tpar=[1:10001];
plot(tpar,parameter);
grid;
zoom on;
pause;
[xt,yt]=ginput;
close;
par=ptemp(round(xt)-5000:round(xt));
part = par;
t = [1:5001];
plot(t,part);
grid;
zoom on;
pause;
close;
k = input('Terminate program? - press "1" and then ENTER: ');
if k == 1
```

```
  quit;
end
disp('            ');
disp(' Begin calculation of THD...');
%************************ Fourier analysis ************************
N = length(part);                          % number of points in one cycle
                                           % cycle.
w=2*pi/N;                                  % angular frequency
lasta=0;                                   % initial values
lastb=0;
for  h=1:N_har                              % number of harmonics
  for a=0:N-1;
    ah(h)=(2/N)*part(a+1).*cos(h*w*a)+lasta;% Calculate
    bh(h)=(2/N)*part(a+1).*sin(h*w*a)+lastb;% harmonics
    lasta=ah(h);
    lastb=bh(h);
  end
lasta=0;
lastb=0;
end
last=0;
for h=1:N_har
  aantal_harmonics = aantal_harmonics + 1;
  disp([' Number of harmonics = ',num2str(aantal_harmonics)])
  for b=0:N-1;
   fa(h,b+1)=ah(h)*cos(w*b*h);             % Calculate
   fb(h,b+1)=bh(h)*sin(w*b*h);             % fundamental
   F(h,b+1)=fa(h,b+1)+fb(h,b+1);           % component and
   end                                     % harmonics
 end
last=0;
for h=1:5
  f=F(h,:)+last;
```

```
  last=f;
end
 aantal_harmonics = 0;
 fund_ampl = max(F(1,:));
 a_harmonics = ah;
 b_harmonics = bh;
  ah_harmonics_tot = (a_harmonics(2:length(a_harmonics)));
 bh_harmonics_tot = (b_harmonics(2:length(b_harmonics)));
 tot_harmonics_t = (ah_harmonics_tot + bh_harmonics_tot);
 tot_harmonics_tot = abs(tot_harmonics_t);
  T = (tot_harmonics_tot./fund_ampl);
 Ts = T.^2;
 Tsum = sum(Ts);
 TOT_harmonics = 100*sqrt(Tsum);
  Nrms = length(part);
 rms_value = sqrt((1/Nrms*(sum(part.^2))));
 nh = [2:N_har];
stem(nh,tot_harmonics_tot);
xlabel('Number of harmonics');
ylabel('Amplitude of harmonics');
grid;
pause;
close;
plot(t,part,t,F(1,:));
xlabel('Number of points.');
ylabel('Fundamental component and actual waveform ');
grid;
pause;
disp('                    ');
tm = toc;
disp(' End of calculation...');
```

Appendix F: Matlab program to calculate unbalance in voltages.

```
clear all;
tic;
echo on;
load ubva.out;                    % load Simuwin - outputfile
load ubvb.out;                    % load Simuwin - outputfile
load ubvc.out;                    % load Simuwin - outputfile
echo off;
ptempa = ubva(:,2);               % voltage matrix
ptempb = ubvb(:,2);               % phase b volage
ptempc = ubvc(:,2);               % phase c volage
begin = 2000;
param = ptempa(1:begin);
parameter = param;
k=0;
time_step = 1e-3;
time = time_step*200;
x = length(parameter);            % number of points
tpar=[1:begin];
plot(tpar,parameter);
grid;
zoom on;
pause;
[xtt,yt]=ginput;
xt = xtt;
close;
para=ptempa(round(xt)-200:round(xt));
parb=ptempb(round(xt)-200:round(xt));
parc=ptempc(round(xt)-200:round(xt));
t = [0:time_step:time];
plot(t,para,t,parb,t,parc);
```

```
grid;
zoom on;
pause;
k = input('Terminate program? - press "1" and then ENTER: ');
if k == 1
  quit;
end
disp('              ');
disp(' Begin calculation of unbalance...');
Narms = length(para);
arms = sqrt((1/Narms*(sum(para.^2))));
Nbrms = length(parb);
brms = sqrt((1/Nbrms*(sum(parb.^2))));
Ncrms = length(parc);
crms = sqrt((1/Ncrms*(sum(parc.^2))));

V12 = arms;
V23 = brms;
V31 = crms;

beta = ((V12^4+V23^4+V31^4)/((V12^2+V23^2+V31^2)^2));
unbalance = sqrt(((1-(sqrt((3-(6*beta))))))/((1+(sqrt((3-(6*beta))))))))*100;
disp([' Unbalance =',' ',num2str(unbalance),' ','%']);
```