Analysis and synthesis of an active resonant snubber for high-power IGBT converters

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Declaration

I, the undersigned, hereby declare that the work contained in this thesis is my own original work, unless stated otherwise, and has not previously, in its entirety or in part, been submitted at any university for a degree.

Frederik Wilhelm Combrink
November 22, 2001

Summary

This thesis describes the study of two soft-switching inverter topologies that are well suited to high-power applications. For the first topology, namely an active resonant turn-off snubber, the existing theory is expanded with a detailed study into operation strategies and topology protection.

This is followed by an investigation into the second topology, which is a combined snubber that reduces both turn-off and turn-on losses. The investigation involves a detailed analysis of the losses in the snubber components and main devices, as well as a study into the effects of parasitic components and diode reverse recovery on the operation of the snubber. Based on this theory a snubber optimisation procedure is also developed. Possible operation strategies and protection techniques were also evaluated for this topology. Single-phase experimental inverters were used to verify the basic operation theory and switching loss prediction for both topologies.

The thesis is concluded by the design and construction of a practical soft-switching three-phase inverter. After implementation the experimental inverter is used for theory verification.

Opsomming

Hierdie proefskrif beskryf die ondersoek na twee saggeskakelde omsetter topologieë wat veral geskik is vir hoë-drywing toepassings. Die bestaande teorie aangaande die eerste topologie, naamlik 'n aktiewe, resonante, afskakel gapser, word uitgebrei met 'n deeglike studie oor bedryfstegnieke en beskermingsmetodes.

Vervolgens word 'n gekombineerde gapser topologie, wat beide aanskakel- en afskakelverliese verminder, ondersoek. Die studie behels 'n volledige analise van die verliese in die omsetter en gapser komponente en die invloed van parasitêre komponente en diode tru-herstel. Hierdie teorie word ook gebruik om 'n optimale gapser ontwerp prosedure te ontwikkel. Die moontlikke bedryfstegnieke en beskermingsmetodes word ook vir hierdie topologie evalueer. In albei gevalle is eksperimentele, enkelfase omsetters gebruik om die teorie oor basiese werking en skakelverlies vermindering te verifieer.

Die ondersoek word afgesluit deur die ontwerp en konstruksie van 'n praktiese, saggeskakelde, drie-fase omsetter te beskryf. Na implimentering van die omsetter word volledige eksperimentele verifikasie uitgevoer.

Acknowledgements

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Glossary

ARCP	Auxiliary Resonant Commutated Pole
CSI	Current Source Inverter
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
EPLD	Electronic Programmable Logic Device
ESR	Effective Series Resistance
FPGA	Field Programmable Gate Array
GTO	Gate Turn-off Thyristor
IGBT	Insulated Gate Bipolar Transistor
IPM	Intelligent Power Module
LC	Inductor Capacitor
MOSFET	Metal-oxide-semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PEBB	Power Electronic Building Block
PWM	Pulse Width Modulation
RCD	Resistor Capacitor Diode
SOA	Safe Operating Area
VSI	Voltage Source Inverter
ZCS	Zero Current Switching
ZCT	Zero Current Transition
ZVS	Zero Voltage Switching
ZVT	Zero Voltage Transition

A_m	Main IGBT Tail Current Ratio
B	Magnetic Flux Density
B_a	Auxiliary Switch Tail Voltage Ratio
B_m	Main IGBT Tail Voltage Ratio
c	Specific Heat
C_D	Diode Output Capacitance
C_r	Snubber Capacitor
D	Diode
D_{max}	Maximum Duty Cycle
F	Water Flow Rate

f_m	Modulation Frequency
f_s	Switching Frequency
g	Core Air Gap
G	Main IGBT
η	Energy Flow Rate
H	Magnetic Field
i_b	Bus Inductor Current
i_c	Collector Current
i_C	Capacitor Current
i_{drr}	Diode Reverse Recovery Current
I_F	Diode Forward Current
I_{min}	Reference Current
i_o	Output Current
$I_{o_{max}}$	Maximum Output Current
I_p	Phase Current
i_r	Resonant Inductor Current
I_{rr}	Peak Diode Reverse Recovery Current
J	Current Density
k_{box}	Container Thermal Resistance
k_{fc}	Copper Fill Factor
k_R	ESR Coefficient
L_b	Bus Inductor
L_{bpp}, L_{bnp}	Parasitic Bus Inductance
l_c	Effective Magnetic Core Length
L_m	Parasitic IGBT Module Inductance
L_r	Resonant Inductor
L_s	Parasitic Turn-off Snubber Loop Inductance
N	Number of Turns
P_{max}	Maximum Output Power
Q_{rr}	Total Reverse Recovery Charge
ρ	Density
ρ	Resistivity
R_{bpp}, R_{bnp}	Parasitic Bus Resistance
R_C	Capacitor ESR
R_D	Diode On-state Resistance
R_{Gp}, R_{Gn}	Main IGBT On-state Resistance
R_L	Inductor ESR

R_m	Parasitic IGBT Module Resistance
R_{rpp}, R_{rnp}	Parasitic Resonant Inductor Path Resistance
R_S	Auxiliary Switch On-state Resistance
R_{spp}, R_{snp}	Parasitic Turn-off Snubber Loop Resistance
S	Diode Snappiness
S_r	Auxiliary Switch
τ	Time Constant
t_b	Blanking Time
t_{br}	Time Instant When I_{rr} Occurs
t_{cr}	Current Rise Time
t_{cz}	Current Fall Time
t_i	Beginning of Cycle Time
t_{fim}	Main IGBT Current Fall Time
t_{fva}	Auxiliary Switch Voltage Fall Time
t_{fvm}	Main IGBT Voltage Fall Time
t_{rr}	Reverse Recovery Time
t_{tim}	Main IGBT Current Tail Time
t_{tva}	Auxiliary Switch Voltage Tail Time
t_{tvm}	Main IGBT Voltage Tail Time
t_{vr}	Voltage Rise Time
t_{vz}	Voltage Fall Time
T	Temperature
T_j	Junction Temperature
μ_o	Permeability Constant
μ_r	Relative Permeability
v_C	Capacitor Voltage
v_{ce}	Collector-Emitter Voltage
$V_{ce(sat)}$	Collector-Emitter Saturation Voltage
V_d	Bus Voltage
$V_{D(on)}$	Diode On-state Voltage
$V_{G(on)}$	Main IGBT On-state Voltage
V_{init}	Initial Snubber Capacitor Voltage
V_{ll}	Line Voltage
v_o	Output Voltage
V_{rr}	Peak Reverse Recovery Voltage
$V_{S(on)}$	Auxiliary Switch On-state Voltage
ω	Radial Frequency

Chapter 1

Introduction

1.1 Soft-switching topologies

The voltage source pulse-width modulated (PWM) inverter is a popular choice for high-power dc to ac conversion. These inverters are commonly used in ac motor drives (for instance, electrical propulsion drives [28], [50]), uninterruptible power supplies, active power filters [39] and other utility applications. The reason for the popularity of the inverter lies in its simple control schemes and robustness. The PWM technique also leads to negligible output energy at frequencies substantially lower that the switching frequencies.

The availability of new high-voltage, high-current IGBTs has made it the device of choice in PWM converters with ratings up to the low megawatt range. The popularity stems from the fast switching behaviour, square SOA, simplicity of the gate drive and effective protection. For inverters with higher power ratings GTOs are still employed due to long-term reliability problems with package to silicon bonds in IGBTs [44].

In high-power IGBT converters the usable switching frequency is usually limited to a few kilohertz (few hundred hertz for GTO converters), mainly due to excessive switching losses and the associated thermal problems. However, the possibility of increasing the switching frequency has to be investigated to obtain the following desirable effects:

1. Increased control bandwidth that improves the dynamic response of the inverter;
2. Improved modulation quality;
3. Smaller and lighter filter components resulting in higher power density and lower cost;
4. Reduction in audible noise if ultrasonic switching frequencies (higher that 18 kHz) can be used;
5. Smaller current ripple and lower torque ripple in drive applications.

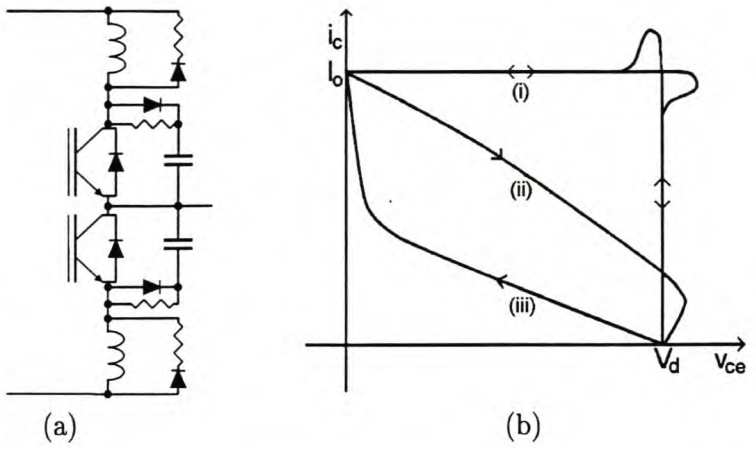


Figure 1.1: (a) Conventional phase-arm snubber. (b) Switching loci for power devices: (i) hard-switching; (ii) turn-off with snubber; (iii) turn-on with snubber.

Beside the large switching losses and low efficiency encountered when high switching frequencies are used in a normal hard-switching PWM inverter, the power devices are also exposed to high switching stresses. The large voltages and currents encountered during switching necessitate switches with a large SOA. High $\frac{di}{dt}$ and $\frac{dv}{dt}$ in the inverter during normal hard-switching PWM operation also causes EMI.

The addition of passive snubbers to the standard PWM voltage source phase-arm can alleviate some of the above-mentioned problems. When GTOs are used as the main switches, a series inductive snubber and a parallel capacitive snubber have to be added to limit $\frac{di}{dt}$ and $\frac{dv}{dt}$ respectively [2], [5], [15]. In Figure 1.1a a phase-arm with a series inductive turn-on and parallel capacitive turn-off snubber is shown [5], [56]. The addition of the snubbers alters the switching transients to limit the SOA requirements of the devices. In Figure 1.1b switching loci are shown for the hard-switching case as well as the modified behaviour due to the addition of the snubbers (taken from [9]). The snubbers also reduce $\frac{di}{dt}$ and $\frac{dv}{dt}$ encountered in the inverter.

Although switching losses in the main devices are reduced, energy remains trapped in the reactive snubber components. The trapped energy is usually dissipated in resistors, as shown in Figure 1.1a. The addition of the snubber circuit therefore does not reduce the overall losses in the inverter. Extra circuits can be added to recover the trapped energy instead of dissipating it in resistors [3], [6], [12], [27], [44], [42]. The auxiliary circuits needed to achieve the energy recovery are usually elaborate and greatly increase component count and complexity.

As an alternative to the basic snubbers, various other soft-switching topologies have been introduced over the years. All of them alleviate some of the problems associated with high switching frequencies by turning-on and turning-off devices at zero-current or zero-voltages. However, these topologies require additional active and/or passive components, special control

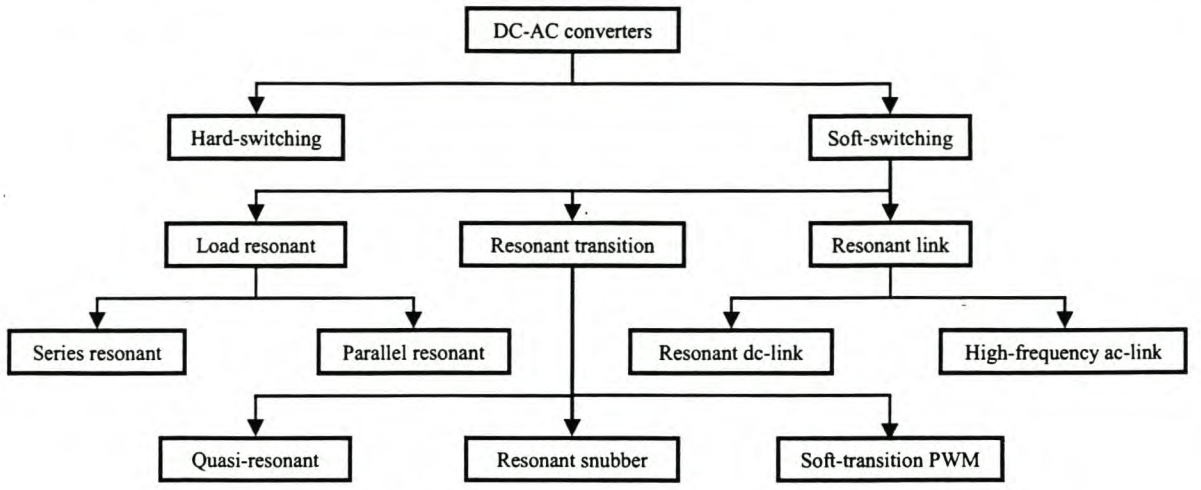


Figure 1.2: Classification of dc-ac converters.

and in some cases introduce extra voltage and current stresses on the main devices.

In Figure 1.2 a classification of dc to ac converters is shown [33], [56]. In general the dc to ac converters can be divided into hard-switching and soft-switching converters. In the soft-switching topologies a resonant network is added to a conventional hard-switching converter. The resonant network can consist of only passive components (capacitors and inductors), but depending on the topology additional auxiliary switches and diodes can also be necessary. These networks provide periods of zero-voltage or zero-current when soft-switching of devices can be achieved. Depending on the location of the resonant network, soft-switching converters can be divided into three classes.

1. **Load resonant.** These converters achieve soft-switching by introducing a LC resonant tank to the load side of the converter. This LC tank resonates along the entire switching period and the oscillating load voltage and current waveforms create ZVS and/or ZCS conditions for the main devices. The class can be divided in basically two groups, namely series resonant and parallel resonant. In the series resonant case the inverter bridge supplies a square-wave voltage to the resonant circuit that is connected in series with the inverter. For the parallel resonant case a square wave current is supplied to the resonant circuit that is connected in parallel with the inverter. In both cases the load itself can be connected in series or parallel to the resonant circuit. The operation of a load resonant converter is very sensitive to parameter variation due to aging or manufacturing tolerance. This class is also more suitable for constant load applications, for instance, induction heating [29]. Variations of these topologies are used extensively in dc-dc converters [8],[25], [31], [36], [37].

2. **Resonant transition.** For the resonant transition dc-ac converter the input bus voltage

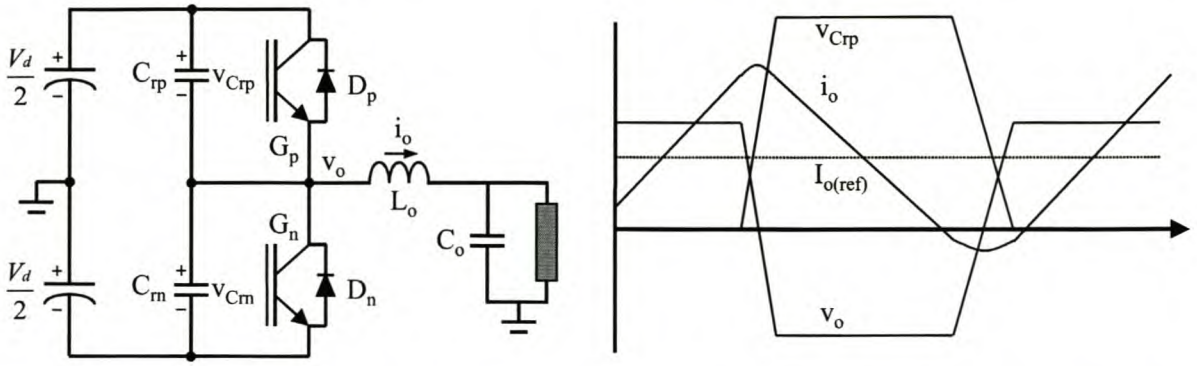


Figure 1.3: Resonant pole inverter topology and typical waveforms during large positive output current.

(VSI) or current (CSI) is fixed and the resonant network is added to the inverter phase-arms. The resonant circuit is only activated during the switching transient intervals to create zero-current or zero-voltage conditions for the inverter switches. An advantage of these converters is that the resonant network is not involved in the main power flow. The energy involved in resonance is therefore kept as low as possible, but still sufficient to ensure soft-switching under full load variation. This class can be divided roughly into three groups, namely quasi-resonant converters, resonant snubber converters and soft-transition PWM converters.

(a) Quasi-resonant converters

The resonant pole inverter (also known as the quasi-resonant ZVS inverter) is an example of a quasi-resonant converter. The idea was first proposed for dc-dc converters, but it was found to be also suited to dc-ac conversion [56]. The basic topology and typical waveforms obtained with a large positive output current reference value is shown in Figure 1.3. The resonant pole inverter consist of a conventional inverter phase-arm with the addition of two snubber capacitors (C_{rp} and C_{rn}) and an output filter. The filter consist of a capacitor C_o and a small inductor L_o.

In Figure 1.3 it can be seen that a large enough ripple current is allowed in the output inductor to ensure that both main switches conduct current at turn-off. This will not only ensure that the opposite main device will turn-on at zero-voltage due to the conduction of its free-wheeling diode, but zero-voltage turn-off is also achieved due to the snubber capacitors. The control of the topology is relatively simple and a current-mode delta modulation scheme is used to synthesise the low-frequency output. The main problem with this topology is the large current stress on the main switches and large current ripple in L_o. The peak current rating of the switches should be at least twice that of the peak output current, resulting in very poor

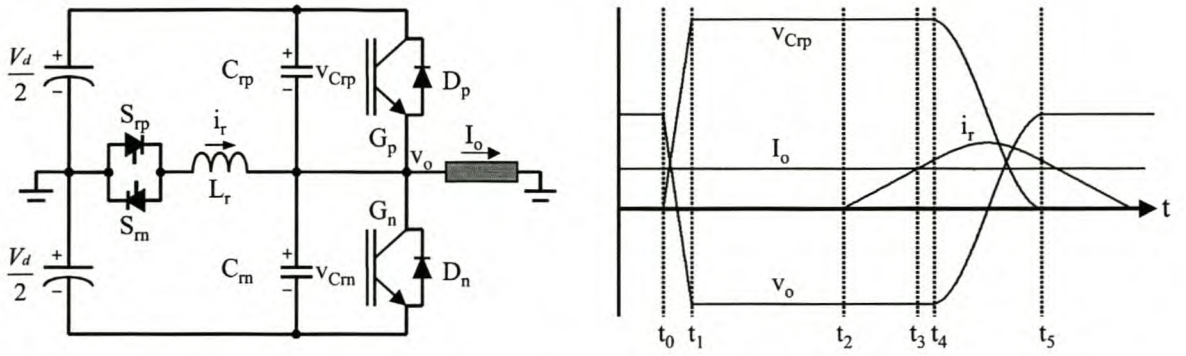


Figure 1.4: ARCP topology and typical waveforms during large positive output current.

switch utilisation.

(b) Resonant snubber converters

The auxiliary resonant commutated pole (ARCP) inverter was introduced [15] as a modified resonant pole schemes to limit current stresses on the main devices. The ARCP inverter can be classified as a resonant snubber converter. In Figure 1.4 the basic topology and typical waveforms obtained during large positive output current can be seen. The ARCP inverter also uses a conventional inverter phase-arm as the base circuit, but extra snubber capacitors (C_{rp} and C_{rn}), a resonant inductor L_r and a set of bi-directional switches (S_{rp} and S_{rn}) are added for each phase.

In Figure 1.4 waveforms for a complete switching cycle under a large positive output current condition is shown. For time $t \leq t_0$ G_p conducts the load current. At t_0 G_p is switched off at zero-voltage and the output current charges snubber capacitor C_{rp} and discharges C_{rn}. At time t_1 the pole voltage reaches the negative bus voltage and free-wheeling diode D_n takes over the load current. G_n can then be switched on at zero-voltage. Under small output current conditions $t_1 - t_0$ becomes excessive and a charge assistance scheme is used. This is done by triggering auxiliary switch S_{rn} at t_0 and the resulting resonance between L_r, C_{rp} and C_{rn} will speed up the pole voltage transition. At t_2 S_{rp} is triggered and a linear current rise occurs in L_r. This continues until the inductor current equals the load current at $t = t_3$. D_n commutates and G_n starts conduction. If G_n is now switched off at t_4, resonance between L_r and the snubber capacitors will result in the discharge of C_{rp} and the charging of C_{rn}. At t_5 the pole voltage swing is complete and D_p will conduct. G_p can now be switched on at zero-voltage. The inductor current boost interval $t_4 - t_3$ is allowed to overcome losses during resonance and therefore ensuring that G_p will have a zero-voltage turn-on condition. It is interesting to note that the auxiliary switches also have zero-current turn-on and turn-off.

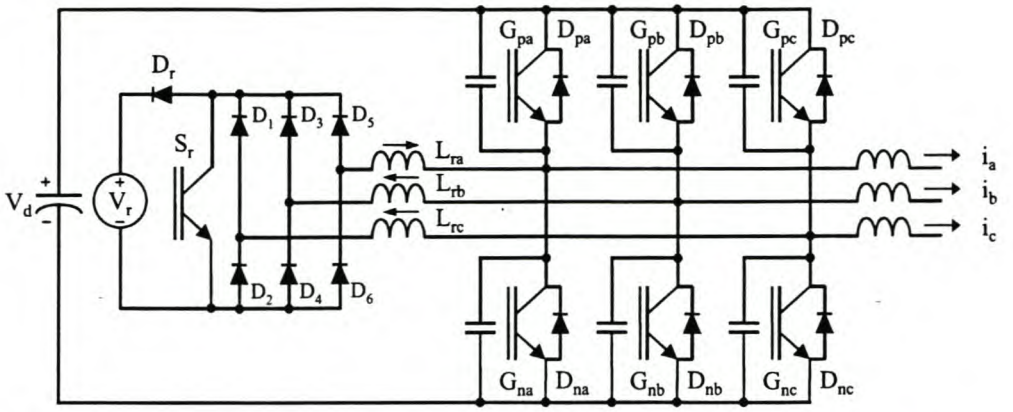


Figure 1.5: ZVT soft-transition (resonant transition) inverter topology.

The control of the ARCP inverter is complicated. To ensure zero-voltage switching under all load conditions and to minimise the conduction losses in the auxiliary components, the inductor current boost stage should be carefully controlled. To achieve this high bandwidth measurements of the inductor current, output current and main device voltages are necessary [51]. Simpler control schemes have been used [49], but with the penalty of reduced efficiency. Another disadvantage of the topology is that the peak current rating of the auxiliary switches is larger than that of the main switches.

Despite the control complexities of the topology, it has received a great deal of attention in the literature. The attention stems from the high efficiency of the ARCP inverter and the possibility of true PWM operation of the inverter. The popularity of this circuit is also evident from the attention it receives from the U.S. Navy's PEBB initiative [51]. A very important improvement on the basic ARCP topology was introduced in [24], [28] and [46]. In these topologies, called the Y-configured and Δ-configured resonant snubber inverters, only one auxiliary switch per phase is used.

(c) Soft-transition PWM converters

Soft-transition PWM converters were initially used in ac-dc and dc-dc conversion, but the techniques were extended to dc-ac conversion [45]. Two types of soft-transition inverters are found in the literature, namely the zero-voltage transition (ZVT) converter and later on also the zero-current transition (ZCT) converters. The ZVT converter, which will be discussed here, is also referred to in literature as the resonant transition inverter [28].

In Figure 1.5 the ZVT three-phase dc-ac converter is shown. The auxiliary circuit consists of a low-power diode bridge ($D_1 - D_6$), auxiliary inductors (L_{ra}, L_{rb} and

L_{rc}), an auxiliary switch S_r, a clamping diode D_r and an auxiliary voltage source V_r. In its simplest for V_r can be implemented as a leaky capacitor. The auxiliary components are turned on at zero current, while the main switches are subjected to zero-voltage switching.

For the purpose of describing the basic operation of the topology, assume i_a is positive and i_b and i_c are negative. It is further assumed that the phase currents are carried by G_{pa}, D_{pb} and G_{nc}. In order to achieve a soft-switching state change in phase b, both G_{pa} and G_{nc} are switched off at zero-voltage. The phase currents will charge the snubber capacitors and diodes D_{na} and D_{pc} will take over the respective phase currents. If S_r is now switched on, the current in the auxiliary inductors will increase linearly (current directions as indicated in Figure 1.5). As the magnitudes of the inductor currents increase beyond those of the respective phase currents, the various free-wheeling diodes will commutate and G_{na}, G_{pb} and G_{pc} will conduct. After all the free-wheeling diodes are commutated and an extra inductor current boost period is allowed, the switches can be turned off. Resonance between the auxiliary inductors and snubber capacitors will create the temporary zero-voltage turn-on conditions for G_{pa}, G_{nb} and G_{nc}.

It is clear that all active devices have to undergo a ZVT switching cycle when one phase has to undergo a change of state. More switching sequences are therefore used than necessary in a conventional PWM inverter. ZVT can also not be achieved when all the top or bottom switches are on simultaneously, which necessitate the use of complicated non-standard control techniques.

3. **Resonant link.** With resonant link inverters the resonant network is shifted to the dc bus. Two types of resonant link converters exist, namely resonant ac-link converters and resonant dc-link converters.

   For a number of years research has been done on high-frequency resonant ac-link converters [1], [4], [7]. An example of such an inverter, namely the parallel resonant ac-link converter, is shown in Figure 1.6. The high-frequency LC resonant tank, consisting of L_r and C_r, is connected between the dc bus and the inverter phase-arms. It produces a sinusoidal voltage waveform across the inverter phase-arms. Zero-voltage switching conditions are therefore available for the bi-directional switches twice every resonance interval. In a series resonant ac-link converter a high frequency sinusoidal current is generated and the switches are subjected to zero-current switching. In both cases discrete pulse modulation are used to synthesise the low-frequency reference value.

   As in the previous case, a resonant network is added between the dc bus and the inverter phase-arms in the resonant dc-link converters. However, the oscillating dc-link does not

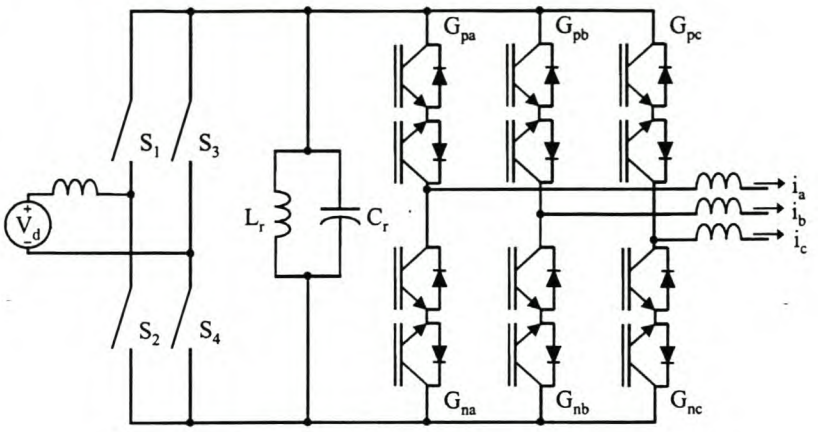


Figure 1.6: Parallel resonant ac-link inverter topology.

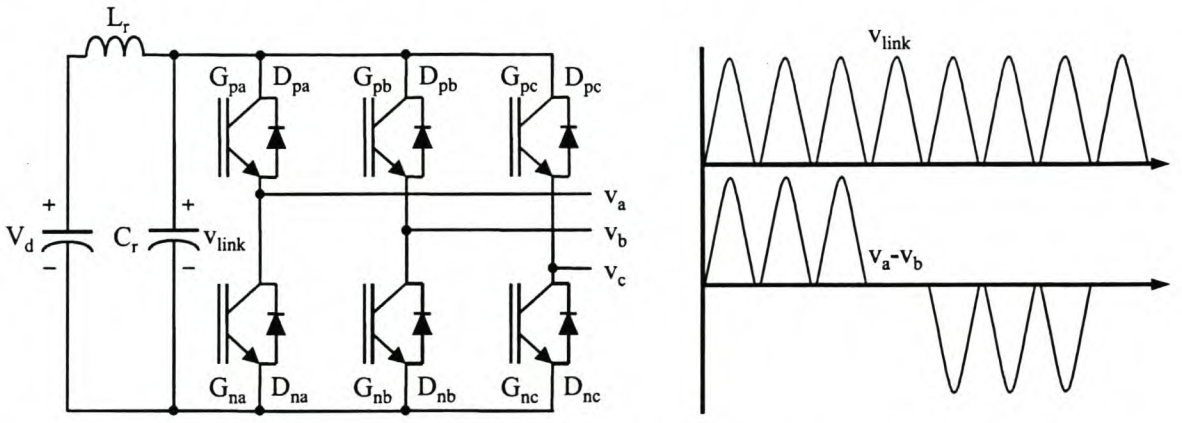


Figure 1.7: Parallel resonant dc-link inverter topology.

change polarity and only uni-directional switches in the inverter phase-arms are necessary. Again both series and parallel resonant dc-link converters are found in literature.

The basic parallel resonant dc-link converter was introduced in [9]. This topology, together with basic waveforms, is shown in Figure 1.7. The resonance between L_r and C_r causes zero crossings in v_{link} and provides zero-voltage switching conditions for the phase-arms. As was the case with the ARCP inverter, the inductor current has to be boosted before every resonance cycle to overcome losses and ensure that zero-voltage switching conditions will be available for the next cycle. This is done during zero crossing by keeping both switches in a phase arm on for a controllable boost period. The major disadvantages of this basic parallel resonant dc-link converter are the complexities in the optimised boost period calculations and the large voltage stresses on the main switches. The harmonic content of the discrete pulse modulation output waveforms is also only comparable with PWM inverters if 3-4 times the switching frequency is used [14].

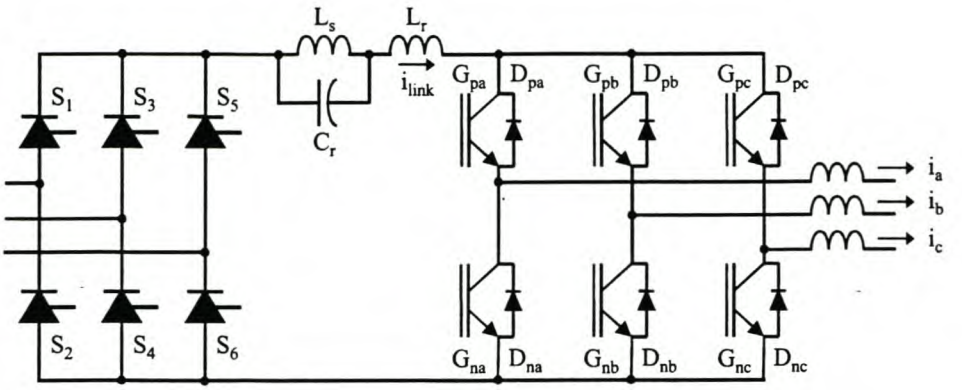


Figure 1.8: Series resonant dc-link inverter topology.

Many variations on the basic parallel resonant dc-link were proposed to solve the voltage stress problem, for instance, the passively clamped converter [11], [34], actively clamped converter [11], [18] and the source voltage clamped converter [40]. Many topologies have also been introduced to obtain PWM operation, for instance, the quasi-resonant, notch-commutated and auxiliary resonant tank dc-link inverters [13], [16], [22], [34].

In Figure 1.8 the basic series resonant dc-link inverter topology is shown [17], [19]. It is the dual of the parallel resonant dc-link inverter in the respect that resonance between L_r and C_r causes zero crossings in i_{link}. The main switches therefore operate under zero-current switching conditions. As was the case with the parallel resonant dc-link inverter, this topology also suffers from control complexities and the limitations of pulse density modulation. Large peak currents also occur in the link that reduces switch utilisation. Improvements on the basic series resonant dc-link topology have also been suggested to achieve PWM operation and to limit current peaks [21], [41].

1.2 Project description

In [52] a new active resonant snubber topology was introduced. This topology can be viewed as a variation of the basic ARCP topology and can therefore also be classified as a resonant snubber dc-ac inverter. With the addition of this active resonant snubber to a standard phase-arm, zero-voltage turn-off of the main devices can be achieved. This is done by introducing a standard turn-off snubber for every main device. To recover energy trapped in the turn-off snubbers, a resonant energy recovery circuit controlled by small auxiliary switches also forms part of the topology. The main advantage of the snubber is that the rating of the auxiliary switches is very small compared to the main devices. The auxiliary switches also operate under ZCS conditions. Although the basic form of this snubber only alleviates turn-off losses, the benefits are still high in relation to the low cost and simplicity of the auxiliary circuit.

An analysis of this topology was made and reported in [58]. This analysis included the development of an design optimisation procedure and a study of the influence of parasitic components on the operation of the topology. The possibility of the integration of a turn-on snubber with the basic active resonant turn-off snubber was also proposed and is reported in [54] and [58].

The active resonant turn-off snubber and the proposed integrated snubber topology are the subjects of this thesis. The contents of this thesis can be expressed as follows:

1. Firstly, the research done on the basic resonant turn-off snubber is extended by investigating additional operation strategies and protection schemes. Implementation of an experimental 22 kVA single-phase inverter, fitted with an active resonant turn-off snubber, is also carried out. The design of the auxiliary circuit of this inverter was done by Prof. H. du T. Mouton according to the procedures developed in [58]. In conjunction with Prof. Mouton experimental verification of system operation is done and loss measurements are taken.

2. The second part of the thesis involves a complete analysis of the integrated active resonant turn-on/turn-off snubber topology. Operation strategies are evaluated and protection of phase-arm and auxiliary devices is investigated. Analytical expressions are derived for loss mechanisms in the auxiliary circuit and main devices. The loss expressions are then used as the basis of a design optimisation procedure. This procedure is subsequently applied to the design of a loss-optimised single-phase soft-switching inverter. In order to verify basic system operation and to investigate the effect of parasitic components and other unmodeled effects, the single-phase inverter is implemented. Loss measurements on the experimental inverter are done and compared to predictions from developed models.

3. The last part of the thesis investigates the expansion of the topology to a three-phase inverter. An experimental 100 kVA three-phase inverter, fitted with the resonant turn-off snubber, is designed and constructed. For the design of the three-phase turn-off snubber circuitry the optimisation procedure developed for the integrated snubber is adapted and refined further. Experimental system verification and loss measurements on the three-phase inverter are done.

The three parts of the thesis will be treated separately in different chapters, followed by a chapter with the major conclusion drawn from the different parts of the investigation.

Chapter 2

Turn-off snubber

2.1 Introduction

In [52] a new resonant turn-off snubber was introduced and further studies on the topology were reported in [58]. The topology forms part of the class of active resonant transition dc-ac converters discussed in Chapter 1. The main advantage of this topology is that the peak current rating of the auxiliary switches is small compared to the rating of auxiliary switches used in other active resonant topologies.

In [58] a complete analysis of this active resonant turn-off snubber topology was performed. This analysis included the basic operation principles, evaluation of snubber losses and the effect of parasitic components. An optimisation procedure was also developed and certain implementation considerations were discussed. Only one operating strategy, however, was mentioned and protection schemes for the topology were not considered.

This chapter will start with a brief discussion on the basic operation principles of the active resonant turn-off snubber topology. This discussion is based on the description of the operation principles found in [58]. It will be followed by a discussion on different operation strategies and possible protection schemes for the topology. This chapter will be concluded with additional experimental results not reported in [58].

2.2 Basic operation principles

The topology of the active resonant turn-off snubber is shown in Figure 2.1. The main IGBTs G_p and G_n, together with free-wheeling diodes D_p and D_n, form a standard phase-arm. The dc bus capacitor bank is formed by capacitors C_{dp} and C_{dn}. Capacitor C_{rp} and diode D_{rp} act as a turn-off snubber for G_p, while capacitor C_{rn} and diode D_{rn} form the turn-off snubber for G_n. Unlike a passive turn-off snubber, the energy in the capacitors is not dissipated in bleeding resistors, but is returned to the bus during a resonance cycle with the inductors. The discharge of C_{rp} is achieved when resonance with inductor L_{rp} is initiated and C_{rn} is discharged through

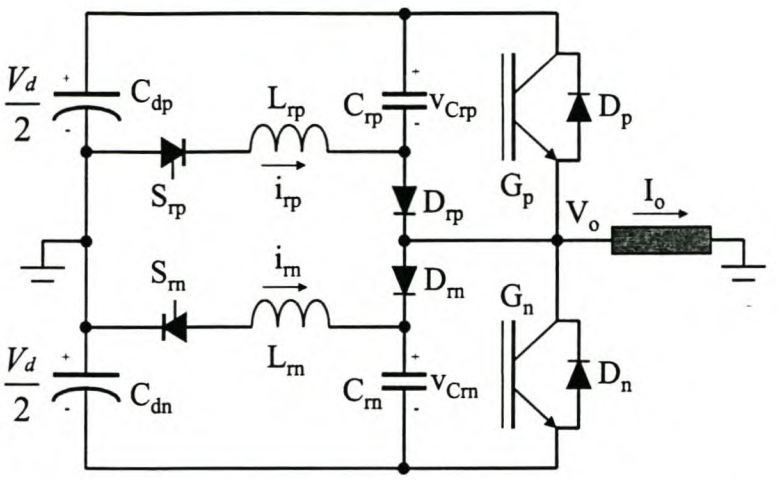


Figure 2.1: Active resonant turn-off snubber topology.

resonance with L_{rn}. The values of capacitors C_{rp} and C_{rn} are equal and this value will be referred to as C_r. L_{rp} and L_{rn} will likewise be referred to as L_r.

Auxiliary switches S_{rp} and S_{rn} are used to control the resonance between the snubber capacitors and the discharge inductors. Although the auxiliary switches are shown as thyristors, any semiconductor switching device is suitable. The auxiliary switches do, however, need a reverse voltage blocking capability. If a device like an IGBT or MOSFET is used, reverse voltage blocking can be achieved be connecting extra diodes in series with the switches.

For the purpose of describing the operation of the topology, a number of assumptions are made:

1. The main IGBTs, the auxiliary switches and the diodes are ideal. This implies that the transitions between states are immediate and that there is no on-state voltage drop across these devices.

2. All the passive snubber components are ideal.

3. All parasitic capacitance, inductance and resistance are ignored.

4. It is assumed that the output current remains constant during a switching cycle. The load is therefore modelled as a current source I_o.

5. An infinite dc bus is assumed.

6. A fixed blanking time t_b is used in the converter.

The operation for positive load current will be described. This will be done by dividing the switching cycle into different time intervals as indicated in Figure 2.2. Each of these time intervals will be discussed separately.

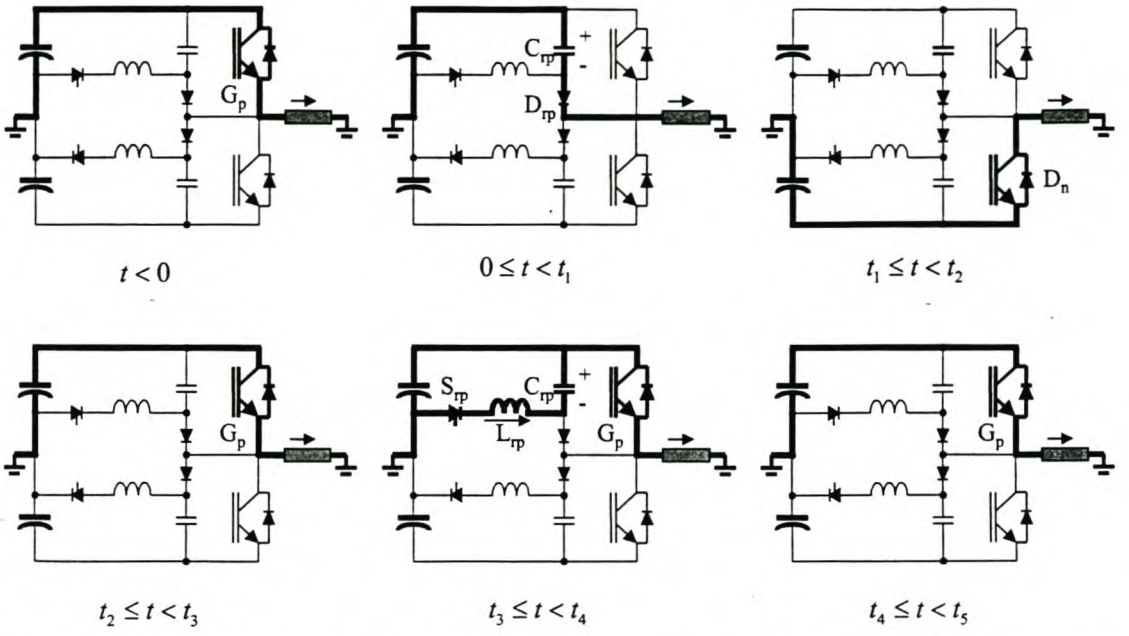


Figure 2.2: Active parts of the turn-off snubber topology during different time intervals.

Time interval $t < 0$:

The full load current is carried by the top IGBT G_p.

Time interval $0 \leq t < t_1$:

At $t = 0$ G_p turns off instantaneously. The load current I_o is taken over by the top snubber capacitor C_{rp}. The voltage across the capacitor is given by

$$v_{Crp} = \frac{I_o t}{C_r}. \tag{2.1}$$

This voltage also appears across G_p and as a result the main IGBT is switched off at a zero-voltage condition. The time it takes for the voltage at the pole to swing from the positive rail to the negative rail is a function of I_o. Depending on the magnitude of I_o, two cases are possible. Firstly, if the time necessary for v_{Crp} to reach the bus voltage is less than the blanking time of the converter, the charging time t_1 can be calculated by

$$t_1 = \frac{V_d C_r}{I_o}. \tag{2.2}$$

The second case occurs if I_o is too small to fully charge C_{rp} during the blanking time. In this case the main IGBT G_n will switch on before v_{Crp} has reached V_d. This will result in large peak currents in C_{rp}, D_{rp} and G_n. In the next section possible operation strategies that can be followed to avoid this undesirable effect will be discussed.

Time interval $t_1 \leq t < t_2$:

The full load current is now carried by the free-wheeling diode D_n. This continues until G_p is switched on again at time t_2.

Time interval $t_2 \leq t < t_3$:

At t_2 the output voltage swings instantly from $-\frac{V_d}{2}$ to $\frac{V_d}{2}$ and the full load current is carried by G_p. The voltage across the snubber capacitor v_{Crp} is still equal to V_d.

Time interval $t_3 \leq t < t_4$:

Triggering of the auxiliary switch S_{rp}, at time t_3, starts the resonant discharge cycle of the turn-off snubber capacitor C_{rp}. It is important to note that the auxiliary switches also turn-on at a zero-current condition due to the series inductance. C_{rp} starts to discharge through L_{rp} and i_{rp} is given by

$$i_{rp} = \frac{V_d}{2}\sqrt{\frac{C_r}{L_r}}\sin\omega\left(t - t_3\right), \tag{2.3}$$

where $\omega = \sqrt{\frac{1}{C_r L_r}}$. The corresponding voltage across C_{rp} is given by

$$v_{Crp} = \frac{V_d}{2}\left(1 + \cos\omega\left(t - t_3\right)\right). \tag{2.4}$$

The period comes to an end when v_{Crp} and i_{rp} reaches zero at $t_4 = t_3 + \frac{\pi}{\omega}$.

Time interval $t_4 \leq t < t_5$:

The state of the converter is identical to the period $t < 0$. The switching cycle can now be repeated.

For negative output current the operation of the snubber is symmetrical. In this case C_{rn} will be charged at the turn-off cycle of G_n and the auxiliary switch S_{rn} will control the resonant discharge cycle between C_{rn} and L_{rn}.

It should be noted that an inverter fitted with this turn-off snubber can only be operated with a maximum duty cycle smaller than 1. To ensure that a snubber capacitor has enough time to fully discharge, the main IGBT that conducts current during this discharge period has to be on for a duration of at least $t_4 - t_3 = \frac{\pi}{\omega}$ seconds. For a specific selection of switching frequency, blanking time and maximum duty cycle (D_{max}) the constrains on the value of C_r and L_r can be expressed as

$$L_r C_r < \frac{\left(\frac{1}{f_s} - 2t_b\right)^2 \left(1 - D_{max}\right)^2}{\pi^2} \tag{2.5}$$

where f_s is the switching frequency.

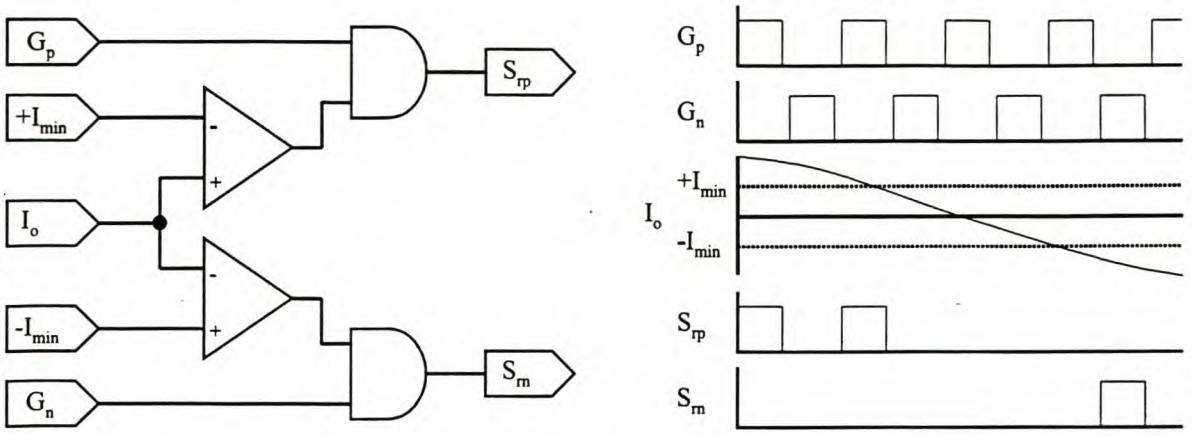


Figure 2.3: Discontinuous snubber operation.

2.3 Operation strategies

In the description of the basic operation principles of the turn-off snubber it was mentioned that special control strategies at low output current conditions are necessary. The reason for this is that during periods of low output current the snubber capacitors are not fully charged in the blanking time of the inverter. The turn-on of the opposite main IGBT under these conditions will result in large peak currents in the snubber capacitors and diodes as well as the main devices.

In order to avoid this undesirable effect, a number of operation strategies can be followed. These strategies will be briefly discussed.

2.3.1 Discontinuous snubber operation

In [58] this operation strategy was described and also used in an experimental inverter. For this strategy the output current of the inverter is measured and the discharging of snubber capacitors discontinued at low output current conditions. The snubber capacitors therefore remain charged during periods of low output current and the inverter is operating as a normal hard-switching inverter. Possible control circuitry to implement this strategy, as well as timing diagrams, is shown in Figure 2.3. The reference current I_{min} in Figure 2.3 can be calculated by substituting t_b for t_1 in equation 2.2 that results in

$$I_{min} = \frac{V_d C_r}{t_b}. \tag{2.6}$$

From Figure 2.3 it is clear that during periods of large output current essentially the same gate signals are uses for the main IGBTs and auxiliary switches. In contrast it was shown in the previous section that there is a delay of $t_3 - t_2$ seconds before the auxiliary switches are turned on. This delay was allowed to ensure that the voltage across the main IGBT has sufficient time

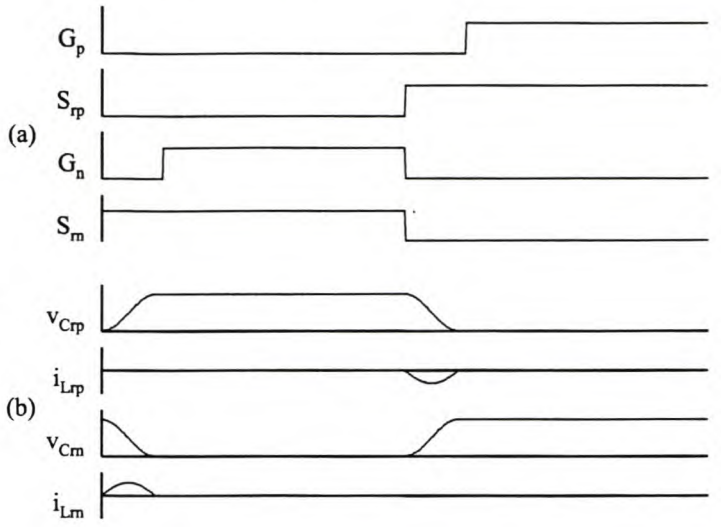


Figure 2.4: Simulation results showing topology behaviour under uni-directional charge assistance operation (I_o=0): (a) Gate signals for main and auxiliary switches; (b) Current and voltage waveforms in snubber circuit.

to fall to the on-state value before the snubber capacitor is discharged. However, in a practical inverter the voltage fall time of the main IGBT will typically be an order of magnitude shorter that the snubber capacitor discharge time. No provision was therefore made in the proposed control circuitry to implement this delay.

2.3.2 Non-linear operation

To limit the magnitude of peak currents that can occur under low output current conditions, it is essential to ensure that the snubber capacitor voltage is as close as possible to V_d before the opposite main IGBT is switched on. A possible operation strategy is therefore to postpone the turn-on instant of the opposite main IGBT to a later stage or even leave it off altogether. This implies a dynamic adjustment of the blanking time and an over-all modification of the control scheme for the inverter. The non-linearities introduced by this variation in blanking time greatly complicates the control algorithm for the inverter.

2.3.3 Uni-directional charging assistance

Another way of ensuring that the snubber capacitor voltage is close to V_d before the opposite main IGBT is switched on is to assist the charging of the active snubber capacitor during the blanking time. This assistance, for small load current, can be achieved by triggering S_{rn} just after G_p is turned off. The resulting resonance between C_{rp}, C_{rn} and L_{rn} will charge C_{rp}. A problem is, however, encountered when G_p is turned on again, because C_{rn} will discharge in the process of charging C_{rp}. The symmetrical action of charging C_{rn}, just after G_n is switched

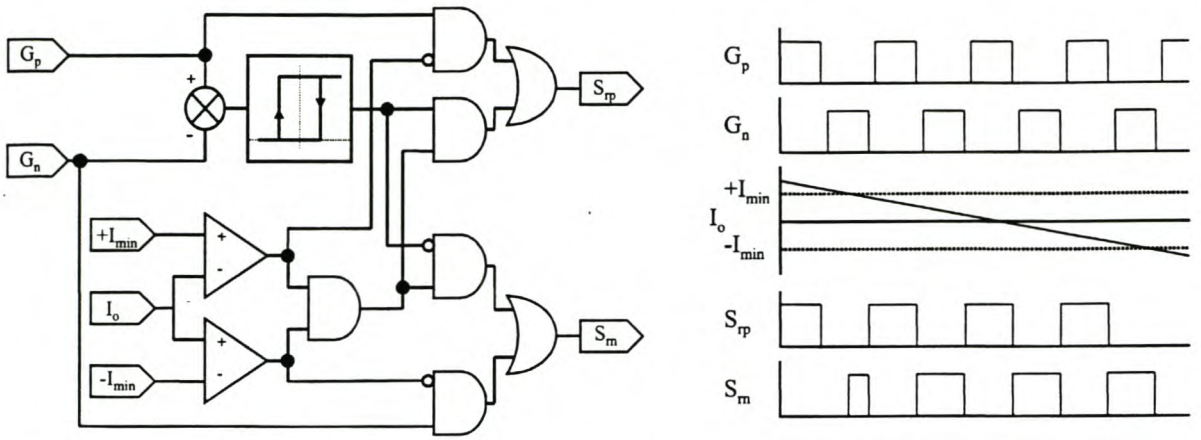


Figure 2.5: Uni-directional charging assistance

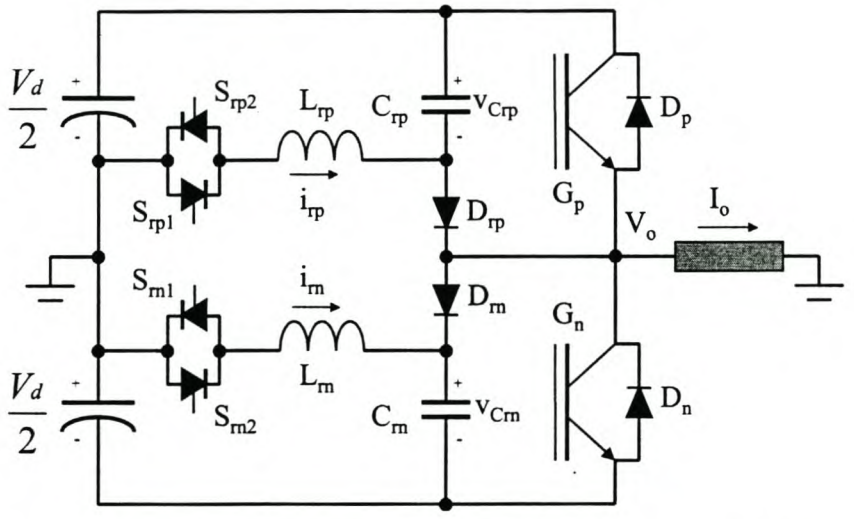


Figure 2.6: Topology expansion to provide for bi-directional charging assistance.

off, is therefore necessary. This can be done by triggering S_{rp} and the resulting resonant cycle between C_{rp}, C_{rn} and L_{rp} will leave C_{rn} charged and C_{rp} discharged. At low output current condition the snubber capacitors are therefore charged and discharge before any of the main IGBTs are switched on. This is similar to the charge assistance scheme used in an ARCP inverter. During periods of large output current the charge assistance can be discontinued. In Figure 2.4 simulated waveforms under zero output current conditions are shown. Possible control circuitry to implement this strategy and associated timing diagrams are shown in Figure 2.5.

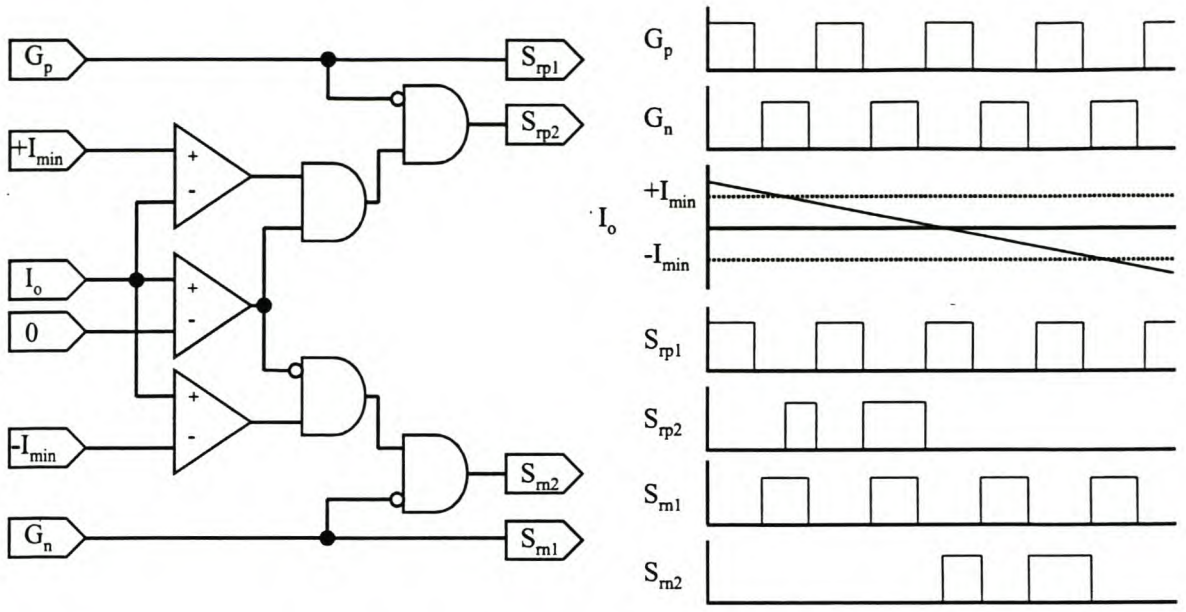


Figure 2.7: Bi-directional charging assistance.

2.3.4 Bi-directional charging assistance

Similarly to the previous case, the bi-directional charging assistance strategy assists the charging of snubber capacitors during the blanking time by means of resonance. To avoid the seesaw action of the previous case, the auxiliary switches are expanded to have bi-directional current flow as shown in Figure 2.6. This addition enables one therefore to charge and discharge either C_{rp} or C_{rn} in isolation from the other capacitor. Possible control circuitry to implement this strategy and associated timing diagrams are shown in Figure 2.7.

2.4 Protection strategies

An important aspect of modern inverters is reliability and robustness. In order for a new soft-switching inverter topology to be of practical interest, protection against dangerous operating temperatures, short-circuit conditions and over-current faults should be as effective as strategies used in hard-switching inverters. The added complexities of soft-switching inverter topologies do, however, complicate this task.

In this section possible protection strategies for the new turn-off snubber will be evaluated. The strategies are, however, dependent on the control strategy that is followed and the type of auxiliary switches that are used. For simplicity discontinuous snubber operation is assumed. It is further assumed that the auxiliary switches can be actively switched off.

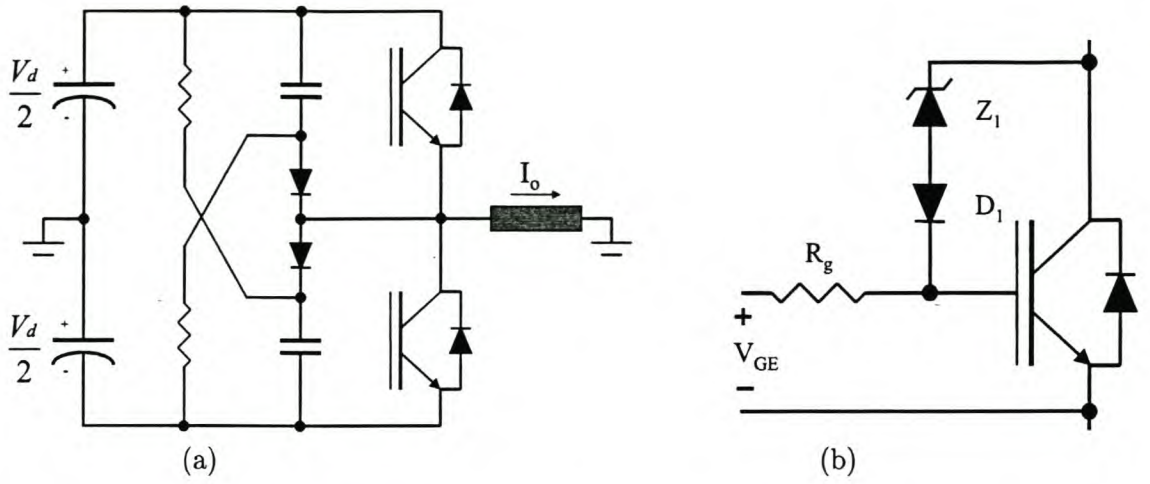


Figure 2.8: (a) RCD voltage clamp. (b) Active zener voltage clamp.

2.4.1 Over-current and short-circuit protection

To protect power devices when large fault or short-circuit currents are present in an inverter, fast detection of such a condition is essential. Various techniques can be used to achieve this, for instance, desaturation detection, direct measurement of device current or current estimation based on the integration of voltage differences between the Kelvin emitter and power emitter of an IGBT [35]. After dangerous current levels are detected, current-carrying power devices have to be shut down within a few microseconds to prevent thermal destruction.

Large voltage overshoot across devices can occur during fault current turn-off due to energy trapped in parasitic inductance. The magnitude of the voltage overshoot is proportional to the total parasitic loop inductance and $\frac{di}{dt}$ at turn-off. Due to the very fast switching characteristics of modern IGBT devices, destruction due to excessive voltage overshoot during fault current turn-off is a major threat to the reliability and effectiveness of fault current protection schemes.

As a preventive measure parasitic inductance should be kept as low as possible when bus-bar design is carried out. High-frequency polymer decoupling capacitors, with low internal lead inductance, should also be placed directly across power module terminals to damp voltage overshoot. Although these measures can greatly contribute to successful protection in high-power IGBT converters, they are seldom sufficient to reliably prevent destructive voltage overshoot during standard short-circuit current turn-off.

Three methods are commonly used to ensure rapid current turn-off and to prevent destructive voltage overshoot.

1. **RCD voltage clamp.** In Figure 2.8a a possible RCD voltage clamp topology is shown [32]. When voltage overshoot occurs during turn-off, the snubber diodes get forward biased and the snubber capacitors damp the voltage overshoot. The result of this energy

absorption is a slight voltage increase on the capacitors above their steady-state bus voltage value. Slow discharge of the capacitors then prepares them for the next turn-off cycle. In [32] it is shown that, for a constant voltage rise, the size of the snubber capacitors should be proportional to the square of the maximum fault current. The cost and size of the snubber capacitor required for effective protection during large short-circuit current turn-off often makes this topology impractical. The addition of this RCD clamp can also not protect the device against overshoot caused by internal module inductance.

2. **Soft turn-off.** Various topologies have been proposed to achieve soft turn-off of IGBTs under fault current conditions [32], [35], [38]. Soft turn-off techniques are also very common in IPM drive circuitry [60]. The technique involves the control of voltage overshoot by slowing down the fault current turn-off behaviour of the IGBT. This can be done by actively controlling the gate voltage or by using a pre-set gate voltage turn-off waveform that will limit voltage overshoot to safe levels. The major drawback of this technique is the complexity of the required driver circuitry.

3. **Active zener clamp.** An active zener clamp voltage protection scheme is shown in Figure 2.8b. When a fault current is detected, the gate driver can immediately turn off the device. If excessive voltage overshoot occur, the zener diode avalanche current will raise the gate-emitter voltage to keep the IGBT in its conduction state and therefore reduce $\frac{di}{dt}$ and voltage overshoot. The feedback mechanism will regulate the voltage overshoot until all the parasitic energy is absorbed.

From the discussion above it is clear that an inverter fitted with the active resonant turn-off snubber is better equipped to protect phase-arm power devices than a normal hard-switching inverter. The reason for this is that the added circuitry itself acts as an RCD voltage clamp. The addition of the snubber circuitry also does not exclude the use of any of the preventive design measures, or fault current turn-off techniques, described in the previous paragraphs.

Although the protection of main phase-arm devices is not negatively influenced by the addition of the active resonant turn-off snubber, extra protection schemes are necessary for the auxiliary switches. Two aspects need to be considered: firstly, when a fault current condition is detected in an auxiliary device and, secondly, the protection of auxiliary devices when the phase-arm shuts down under fault current conditions.

Fault current in an auxiliary switch can, for instance, be caused by incorrect control signals, for example, if S_{rp} is turned on while G_n is on. Turn-off of the auxiliary devices after an over-current condition is detected will lead to very large voltage overshoot across the device due to the series inductance. If the auxiliary switches are, however, not turned-off, the magnitude of the auxiliary switch fault current can become greater than the load current. To prevent

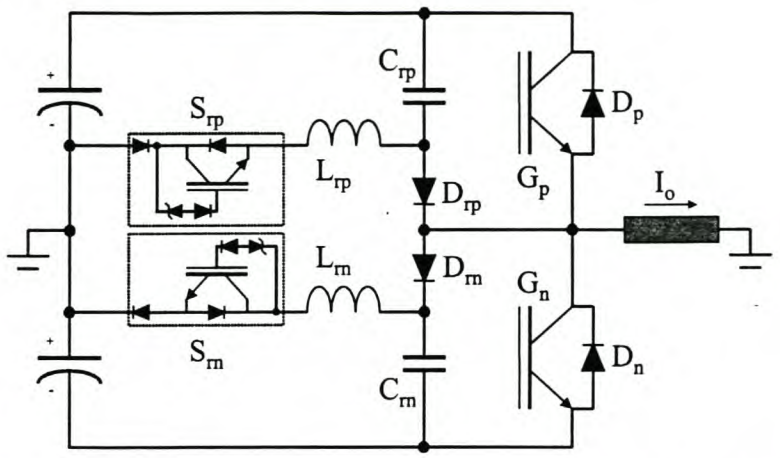


Figure 2.9: Topology with active zener voltage clamp protection for auxiliary switches.

thermal destruction, a fault current turn-off procedure with effective voltage overshoot limiting is necessary.

The other aspect of auxiliary device protection involves strategies when fault current conditions in the main IGBTs occur. For instance, when a fault current condition is detected in G_p, it is very likely that S_{rp} will also be on at that stage. If not, due to insufficient output current at the start of G_p's on-state period, protection of the auxiliary device poses no problem. However, when the auxiliary switch is on during the fault current detection, two states are possible. Firstly, the auxiliary switch can carry current due to snubber capacitor discharge or, secondly, the discharge cycle can be over and no auxiliary device current can be present. For the latter case the auxiliary switches can be shut down directly after main device fault current detection. This action will be sufficient to ensure that the auxiliary switches will not be damaged during inverter shutdown. For the case where the capacitor is still discharging, immediate auxiliary devices shutdown can cause destructive voltage overshoot. The auxiliary device can also not be left on or the turn-off postponed, because, if this is done and the fault current originates from the load side, the auxiliary device current can potentially reach values greater that the main device fault current.

To keep the protection strategy for the auxiliary switches as simple as possible, different actions for different cases should be avoided. A possible unified protection scheme can be to shut down the operation of the active resonant snubber when fault current within an auxiliary device is detected and always to shut down all the switches, main and auxiliary, when fault current is detected in a main device. To solve the problem of possible voltage overshoot during auxiliary switch turn-off, an active zener voltage clamp can be used to provide a simple but effective solution. This unified protection scheme also ensures that integration with IPMs does not pose any problems. In Figure 2.9 the proposed topology with the active zener voltage clamps is shown.

2.4.2 Over-temperature protection

To protect power devices against dangerous operating temperatures, the device and heatsink temperatures are commonly monitored. To prevent thermal destruction, the inverter operation is suspended when dangerous temperatures are detected. Over-temperature protection is also a common feature of most IPM devices [60]. The suggested protection strategy for fault current handling in an inverter fitted with an active resonant snubber enables one to safely switch off all active devices at any stage of operation. The thermal protection of an inverter fitted with the turn-off snubber can therefore be handled like a normal hard-switching inverter.

2.5 Loss evaluation and optimal design

A key consideration in the implementation of the turn-off snubber is to find an optimal trade-off point between the reduction of losses in the main IGBTs and the introduction of new losses in the snubber components. In [58] a detailed analysis of the loss mechanisms in the topology was made. Analytical expressions were derived to describe losses in the main IGBTs and all the snubber components. These expressions were then used as the basis of an optimisation procedure. The aim of this procedure was to determine the size of snubber capacitors and inductors that will lead to the lowest overall losses in an inverter under certain operating conditions.

The process of loss quantification and design optimisation followed in [58] will not be discussed in this thesis. Results obtained with the optimisation procedure will, however, be used in section 2.6. In Chapter 3 a similar approach will be followed for the new integrated topology with turn-off and turn-on snubbing action.

2.6 Design of experimental turn-off snubber

In conjunction with Prof. H. du T. Mouton, a single-phase inverter, fitted with a turn-off snubber, was constructed. The design of the inverter was done by Prof. Mouton and was based on the optimisation procedure developed in [58]. The detailed design of this experimental inverter was also reported in [58] and will not be repeated. The design parameters for this inverter are shown in Table 2.1.

2.7 Experimental results

The constructed inverter was used to obtain experimental results that were reported in [58]. These experimental results included v_{Gp}, v_{Crp} and v_{Drp} waveforms at turn-off and i_{rp} and v_{Crp}

System Parameters		
Nominal DC bus Voltage	V_d	800 V
Peak Output Current	$I_{o(max)}$	200 A
Switching Frequency	f_s	10 kHz
Blanking Time	t_b	5 μs
Maximum Duty Cycle	D_{max}	0.85
Main IGBT Module (Powerex PM200DSA120)		
Current Fall Time	t_{fim}	250 ns
Current Tail Time	t_{tim}	500 ns
Tail Current Ratio	A_m	0.2
Snubber Diode (Semikron SKR48F12)		
On-state Resistance	R_{Dr}	22 mΩ
On-state Voltage	$V_{on(D_r)}$	1.2 V
Snubber Capacitor		
Capacitance	C_r	5 $\times$ 33 nF
ESR Coefficient	$k_{R_{Cr}}$	$3.4 \times 10^{-12}\Omega F$.
Auxiliary IGBT (Fuji 1MBH60D-090A)		
Voltage Fall Time	t_{fva}	17 ns
Voltage Tail Time	t_{tva}	40 ns
Tail Voltage Ratio	B_a	0.06
On-state Resistance	R_{Sr}	0.017 Ω
On-state Voltage	$V_{S_r(on)}$	1.5 V
Peak Current Rating	$I_{r(max)}$	75 A
Auxiliary Diode (IXYS DSEI60)		
On-state Voltage	$V_{D_{Sr}(on)}$	2 V
On-state Resistance	$R_{D_{Sr}}$	8.3 mΩ
Reverse Recovery Time	t_{rr}	40 ns
Resonant Inductor (Philips P30/19 3F3 Core)		
Inductance	L_r	12 μH
ESR Coefficient	k_{R_L}	1.8 kΩ/H

Table 2.1: Parameters for experimental inverter.

waveforms during the capacitor discharge period. Preliminary efficiency measurements were also given. In this thesis additional efficiency measurements are reported.

Although the experimental inverter was designed for a dc voltage of 800 V, experimental measurements on the system were made with a dc bus voltage of 600 V. This value of V_d was chosen because the data sheet values of switching losses are given for a 600 V dc bus.

2.7.1 Efficiency measurements

The inverter losses were measured under two operating conditions. Firstly, a square wave output voltage was used with an inductive load. Under these conditions the IGBTs turn on at

Figure 2.10: Experimental inverter inside wooden container.

zero voltage and zero current. For this reason the turn-on losses can be ignored. Secondly the inverter was operated under normal PWM conditions. In the square wave output voltage case the peak output current was 200 A and switching frequencies of 5 kHz and 10 kHz were used. For the normal PWM operation a sinusoidal output current of 125 A_{rms}, 100 Hz was used. The switching frequency in this case was 7.5 kHz.

A calorimetric technique was used to measure the total inverter losses. The technique is similar to that used in [47]. The whole converter, including the bus-bar structure and snubber components, was mounted in a wooden box lined with thermal insulation material. The main IGBT module was mounted on a water-cooled heatsink. The snubber components and bus capacitors were kept cool with small electric fans. To restrict the temperature rise inside the box, forced circulation of the air was necessary to improve thermal coupling with the water-cooled heatsink. In Figure 2.10 the experimental inverter inside the wooden box is shown.

To determine power dissipation in the inverter, it was assumed that energy can leave the box by only two methods. Firstly, by thermal conduction through the walls of the box and, secondly, by the temperature increase of the water flowing through the heatsink. During a loss measurement the ambient temperature T_a, the temperature inside the box T_b and the temperature of the water entering T_{in} and leaving T_{out} the box were measured over a two hour period. Great care was also taken to keep the flow rate of the water through the heatsink (F) constant.

The rate of energy flow at a specific time during the measurement can be expressed as

$$\eta = k_{box}\,(T_b - T_a) + \rho_{(H_2O)}\,c_{(H_2O)}\,F\,(T_{out} - T_{in}) \tag{2.7}$$

Power dissipated W	T_b-T_a K	k_{box} WK^{-1}
21	14.6	1.44
27	14.8	1.82
33	19.4	1.70
39	22.4	1.72
44	26.2	1.68

Table 2.2: Measurements to determine the thermal resistance of the isolated container.

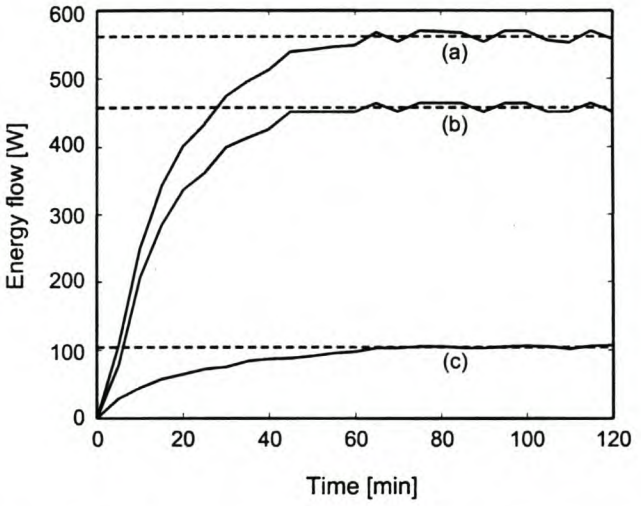


Figure 2.11: Energy flow out of the wooden container during a hard-switching PWM measurement: (a) Total energy flow; (b) Energy flow due to water temperature increase; (c) Energy flow due to thermal conduction.

where k_{box} is the thermal resistance of the wooden container, $\rho_{(H_2O)}$ the density of water and c_{H_20} is the specific heat of water (see [57], p. 553). The thermal resistance of the container was determined by placing a resistor with known dissipation inside the box. There was no water flow and the temperature difference between T_a and T_b was measured after thermal equilibrium had been reached. These measurements are shown in Table 2.2.

Results obtained from a measurement made under normal hard-switching PWM conditions are shown in Figure 2.11. The energy flow out of the container is shown as a function of time. The contribution of thermal conduction, water temperature increase and the total energy flow is shown. The thermal time constant (τ_s) of the system is approximately 16 minutes. The two-hour measuring period is therefore more than $7\,\tau_s$, which is sufficient to reach thermal equilibrium.

Tables 2.3 and 2.4 give a comparison of the calculated and measured converter losses. Every value for the measured losses was obtained by averaging results from at least three two-hour measurements. The main IGBT module turn-on losses were calculated making use of the data

	5 kHz Square Wave		10 kHz Square Wave	
	Hard Switching	Soft Switching	Hard Switching	Soft Switching
Calculated Losses [W]				
Main IGBT Turn-off Losses	250	50	500	100
Main IGBT Turn-on Losses	0	0	0	0
Main IGBT Conduction Losses	105	105	105	105
Freewheeling Diode Losses	120	120	120	120
Snubber Circuit Losses	0	9	0	18
DC Bus Capacitor Losses	144	144	144	144
Total	619	428	869	487
Measured Losses [W]				
Total	664	432	940	550

Table 2.3: Theoretical and measured converter losses with square wave output voltage.

	Modulation	
	Hard Switching	Soft Switching
Calculated Losses [W]		
Main IGBT Turn-off Losses	108	20
Main IGBT Turn-on Losses	124	124
Main IGBT Conduction Losses	101	101
Freewheeling Diode Losses	123	123
Snubber Circuit Losses	0	6
DC Bus Capacitor Losses	120	120
Total	576	494
Measured Losses [W]		
Total	544	476

Table 2.4: Theoretical and measured converter losses under normal PWM operation.

sheet values. The main IGBT module turn-off losses for the hard-switching case were also calculated by this approach. The turn-off losses during snubber operation were calculated in [58]. The theoretical and measured losses correspond well, with a maximum difference of about 10%.

For the square wave output voltage case the predicted reduction in turn-off losses in the main IGBT is 80%, while the predicted reduction in effective turn-off losses is 76%. For the case were normal PWM was used, the predicted reductions are 81% and 76% respectively. Measurements results suggest that the effective reduction in turn-off losses under normal PWM modulation is 63%.

2.8 Conclusion

The basic operation principles of a new active resonant turn-off snubber were discussed. The main advantage of this topology is that the peak current rating of the auxiliary switches is small compared to auxiliary switches used in other active resonant topologies. The overall cost of the added components is also low if compared to the cost of just the main IGBTs. Additional operation strategies were discussed and it was shown that the new topology can easily and effectively be protected against fault currents and dangerous operating temperatures.

An experimental one-phase inverter was constructed in conjunction with Prof. Mouton. A complete set of loss measurements were reported and compared to predicted values. Measurements suggest that the effective reduction in turn-off losses under normal PWM modulation is 63%.

Chapter 3

Combined turn-on and turn-off snubber

3.1 Introduction

In this chapter the integration of a turn-on snubber with the existing turn-off snubber is investigated. The first steps towards this combination are reported in [54] and [58]. Firstly, the basic operation of the combined snubber will be described. This will be followed by a discussion on operation strategies and protection schemes. Analytical expressions, describing the losses in the snubber and main IGBT module, will be derived. These expressions will then be used as the basis of an optimisation procedure. An experimental 1-ϕ inverter, fitted with a combined turn-on and turn-off snubber, will be designed and constructed to verify the theoretical models.

3.2 Basic operation principles

In Figure 3.1 the topology for the combined snubber is shown. This is identical to the turn-off snubber case, except for the addition of two bus inductors L_{bp} and L_{bn}. The role of these inductors is to limit current rise in the main IGBTs during turn-on. As in the turn-off snubber case, the values of C_{rp} and C_{rn} are equal and will be referred to as C_r. The inductor sets L_{bp} and L_{bn} and L_{rp} and L_{rn} will likewise be referred to as L_b and L_r respectively.

The following assumptions are again made for the purpose of describing the operation of the snubber:

1. The main IGBTs, the auxiliary switches and the diodes are ideal. This implies that the transitions between states are immediate and that there is no on-state voltage drop across them.

2. All the passive snubber components are ideal.

3. All parasitic capacitance, inductance and resistance are ignored.

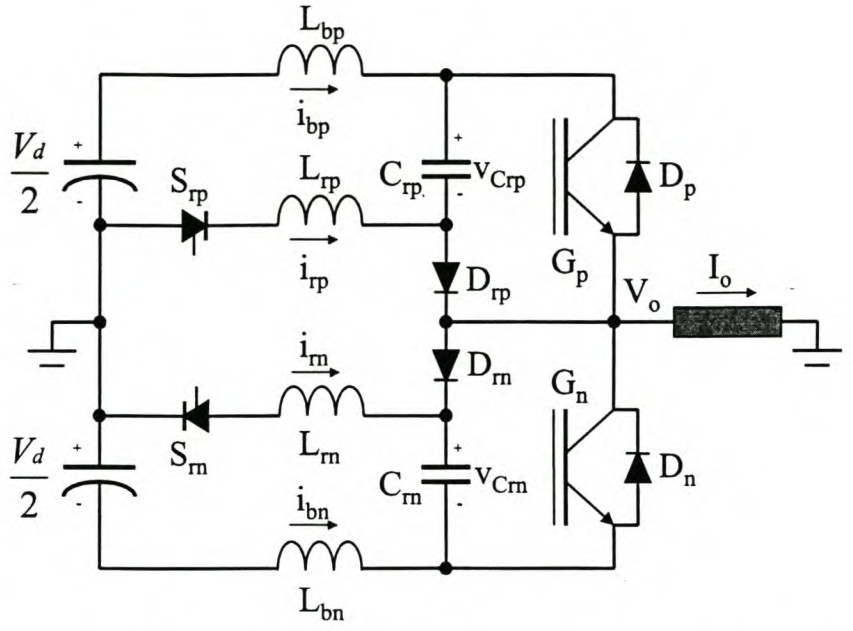


Figure 3.1: Combined turn-on and turn-off snubber topology.

4. It is assumed that the output current remains constant during a switching cycle. The load is therefore modeled as a current source I_o.

5. An infinite dc bus is assumed.

6. A fixed blanking time t_b is used in the converter.

The basic operation of the snubber for positive output current will be described. As was the case for the turn-off snubber, the operation during periods of negative output current is symmetrical and will not be discussed. The operation of the circuit will be divided into different time intervals, as shown in Figure 3.2.

Time interval $t < 0$

The full load current is carried by the top IGBT G_p.

Time interval $0 \leq t < t_1$

At $t = 0$ G_p turns off instantaneously. The load current I_o is taken over by the top snubber capacitor C_{rp}. The voltage across the capacitor is given by equation 2.1. As was mentioned in the turn-off snubber topology case, the time it takes for the voltage at the pole to swing from the positive rail to the negative rail is a function of I_o. Depending on the magnitude of I_o two cases are possible. Firstly, if the time t_1 necessary for v_{Crp} to reach the bus voltage is less than the blanking time of the converter, t_1 can be calculated by equation 2.2. At t_1 the free-wheeling diode D_n becomes forward biased and a period of

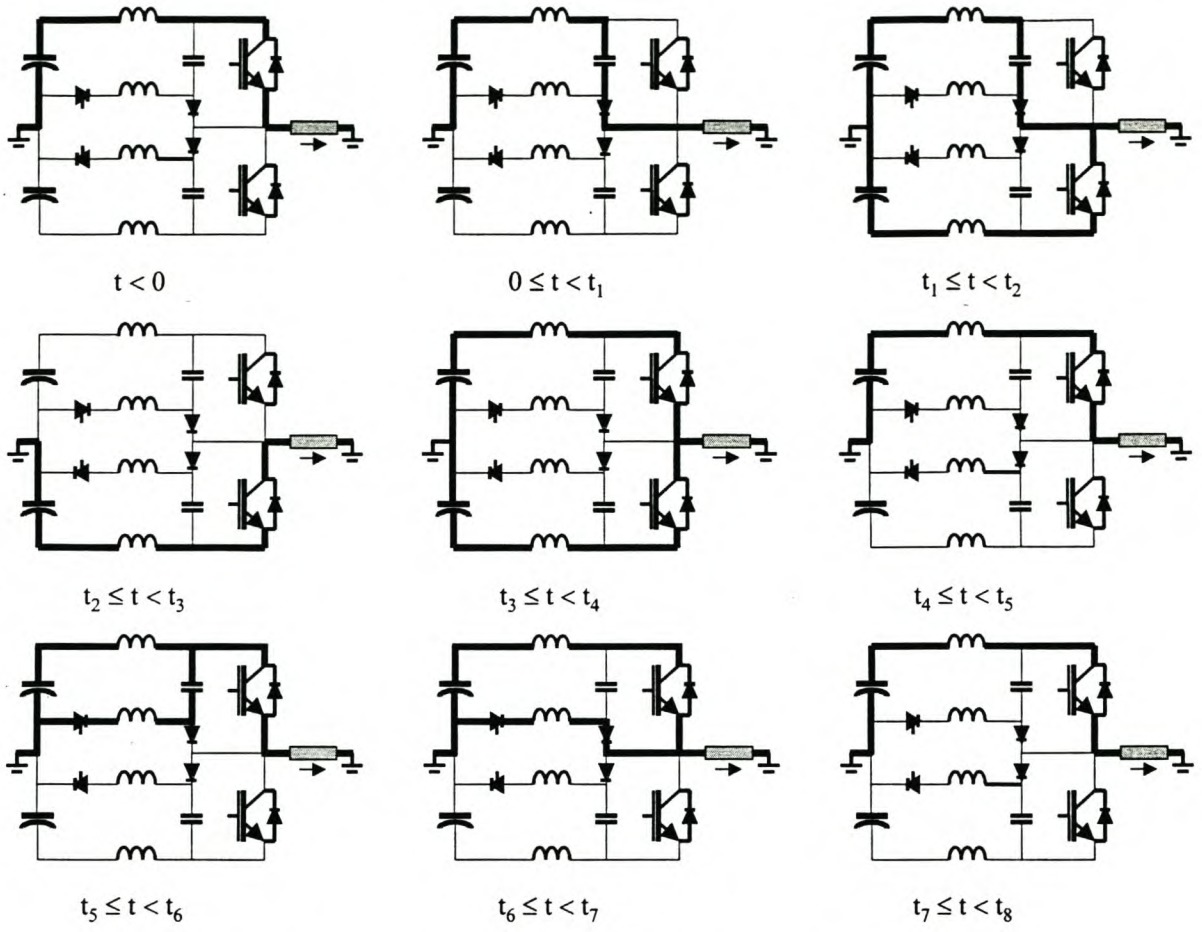


Figure 3.2: Active parts of the snubber topology during different time intervals.

resonance between the bus inductors (L_{bp} and L_{bn}) and the snubber capacitor C_{rp} starts. If I_o is, however, to small to charge the snubber capacitor to the bus voltage before the blanking time expires, the resonance cycle is started after the blanking time expired and G_n is switched on. In this case $t_1 = t_b$. The initial value of v_{Crp}, at the start of resonance for the two different cases, can be expressed as

$$\begin{aligned} \text{Case 1} &: \quad v_{Crp}(t_1) = V_d \\ \text{Case 2} &: \quad v_{Crp}(t_1) = \frac{I_o t_b}{C_r}. \end{aligned} \tag{3.1}$$

Time interval $t_1 \leq t < t_2$

At time t_1 the resonant cycle starts. The current in the top bus inductor i_{bp} is given by

$$i_{bp} = I_o \cos\omega_1 (t - t_1) + \frac{(V_d - v_{Crp}(t_1))}{2L_b\omega_1} \sin\omega_1 (t - t_1), \tag{3.2}$$

where $\omega_1 = \sqrt{\frac{1}{2L_bC_r}}$. The voltage across C_{rp} during this period is

$$v_{Crp} = v_{crp}(t_1) + \frac{I_o}{C_r\omega_1}\sin\omega_1(t-t_1) + (V_d - v_{Crp}(t_1))(1-\cos\omega_1(t-t_1)). \tag{3.3}$$

It is important to note that this voltage also appears across G_p, therefore extra voltage stresses on the main IGBTs are introduced. The resonant cycle continues until time t_2 when i_{bp} reaches zero and D_{rp} turns off. At this instant the maximum voltage across the snubber capacitor is also reached. The value of t_2 can be calculated by

$$t_2 = t_1 - \frac{\arctan\left(\frac{2I_oL_b\omega_1}{V_d - v_{Crp}(t_1)}\right)}{\omega_1}. \tag{3.4}$$

Time interval $t_2 \leq t < t_3$

The full load current is now carried by the bottom bus inductor L_{bn} and free-wheeling diode D_n. This continues until G_p is switched on again at time t_3.

Time interval $t_3 \leq t < t_4$

The output current, which was carried by the bottom bus inductor, shifts to the top bus inductor at a rate determined by the value of these inductors. The current in the top bus inductor i_{bp} can be expressed as

$$i_{bp} = \frac{V_d(t-t_3)}{2L_b}. \tag{3.5}$$

This is also the current in G_p, therefore the presence of the inductance creates a zero-current switch-on condition for the main IGBTs. The interval of current transfer between the inductors comes to an end when the full load current is taken over by L_b at time t_4. This instant can be calculated by

$$t_4 = t_3 + \frac{2L_bI_o}{V_d}. \tag{3.6}$$

Time interval $t_4 \leq t < t_5$

Between times t_4 and t_5 I_o is carried by L_{bp} and G_p.

Time interval $t_5 \leq t < t_6$

Triggering of the auxiliary switch S_{rp} at time t_5 starts the resonant discharge cycle of the turn-off snubber capacitor C_{rp}. C_{rp} starts to discharge through L_{rp} and i_{Crp} is given by

$$i_{Crp} = \sqrt{\frac{C_r}{L_b+L_r}}\left(\frac{V_d}{2} - v_{Crp}(t_2)\right)\sin\omega_2(t-t_5), \tag{3.7}$$

where $\omega_2 = \sqrt{\frac{1}{C_r(L_b+L_r)}}$. The corresponding voltage across C_{rp} is

$$v_{Crp} = v_{Crp}(t_2) + \left(\frac{V_d}{2} - v_{Crp}(t_2)\right)(1-\cos\omega_2(t-t_5)). \tag{3.8}$$

The period comes to an end when v_{Crp} reaches zero at time

$$t_6 = t_5 - \frac{\arccos\left(\frac{V_d}{V_d - 2v_{Crp}(t_2)}\right)}{\omega_2}. \tag{3.9}$$

Time interval $t_6 \leq t < t_7$

At time t_6 the voltage across C_{rp} reaches zero and is clamped to that value by D_{rp}. The current in L_{rp} continues to decrease until it reaches zero at t_7. For this period i_{rp} can be expressed as

$$i_{rp} = -\sqrt{\frac{C_r}{L_b + L_r}}\left(\frac{V_d}{2} - v_{Crp}(t_2)\right)\sin\omega_2\left(t_6 - t_5\right) - \frac{V_d\left(t - t_6\right)}{2\left(L_b + L_r\right)} \tag{3.10}$$

and t_7 can be calculated as

$$t_7 = t_6 - \frac{2\sqrt{C_r\left(L_b + L_r\right)}\left(\frac{V_d}{2} - v_{Crp}(t_2)\right)\sin\omega_2\left(t_6 - t_5\right)}{V_d}. \tag{3.11}$$

Time interval $t_7 \leq t < t_8$

G_p once again carries the full load current. The state of the snubber is identical to the state for time smaller than zero. The switching cycle can now start over again.

In Figure 3.3 simulation results based on equations 2.1, 2.2 and 3.1-3.11 can be seen. Waveforms for two different I_o magnitudes are shown. The specific magnitudes were chosen close to the boundary between case 1 and 2 to demonstrate the difference between the two cases.

3.3 Operation strategies

Similar to the turn-off snubber, different operation strategies can be followed. These different options will be described in this section. Before the different strategies are described, however, base values for L_b and C_r will be defined. These values will be functions of the inverter parameters like peak output current and dc bus voltage. For consistency the parameters of the inverter used to verify the single-phase operation of the combined snubber will be used. The basic design parameters for this experimental inverter are shown in Table 3.7. The Powerex PM200DSA120 integrated IGBT module was used for the main switches. Basic parameters for this module are shown in Table 3.6. The base value of C_r, namely C_{rb}, will be defined as

$$C_{rb} = \frac{I_{o(max)}t_{C(off)}}{V_d} = 200\,nF, \tag{3.12}$$

with the value of $I_{o(max)}$ and V_d as shown in Table 3.7 and $t_{C(off)}$ as in Table 3.6. The base value of L_b is chosen to be numerically equal to C_{rb}, namely $L_{bb} = 200\,nH$.

Five operation strategies were considered.

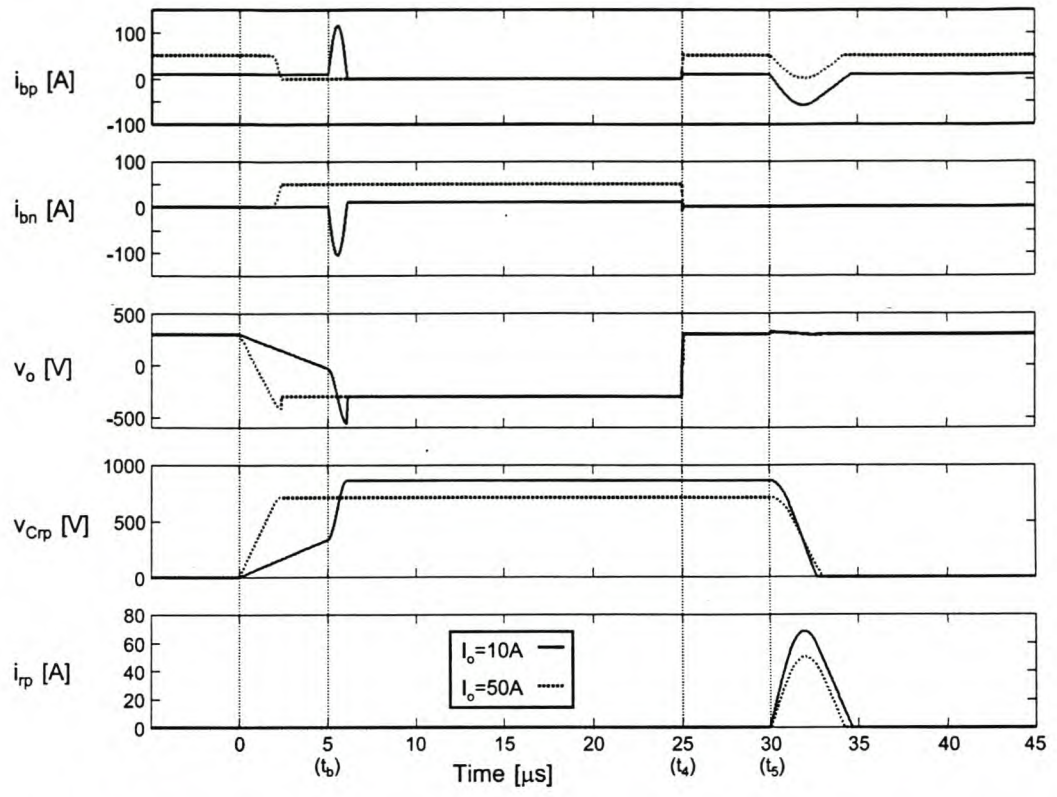


Figure 3.3: Simulation results for the combined snubber topology during a complete switching cycle ($V_d = 600\,V$, $f_s = 20\,kHz$, $C_r = 150\,nF$, $L_b = 400\,nH$, $L_r = 10\,\mu H$ and $t_b = 5\,\mu s$).

3.3.1 Continuous snubber operation

Discontinuous snubber operation was shown to be very effective for the turn-off snubber case. The discharge of the snubber capacitors were discontinued at low output current conditions to prevent large peak currents in the snubber capacitors, snubber diodes and main IGBTs. For the combined snubber topology, however, the added bus inductors will limit these peak currents. For this topology a continuous snubber operation strategy, where the snubber capacitors are discharged even at low output current, can therefore be considered. The snubber capacitors, which will always be in a discharged state at the main IGBT turn-off instant, will also help to limit voltage overshoot caused by the large bus inductance. Possible control circuitry to implement this continuous operation strategy and timing diagrams are shown in Figure 3.4.

In order to evaluate the strategy, estimates should be made of the peak snubber capacitor current and voltage that will occur at low output current conditions. Equations 3.1-3.4 were used for this purpose. For the experimental inverter described in section 3.7, the peak snubber capacitor current that will occur during turn-off is shown in Figure 3.5-1. The peak current in the main IGBT, which turns on after the blanking period expires, will be equal to the snubber capacitor current minus the output current. It can be seen that for large I_o (case 1) the peak

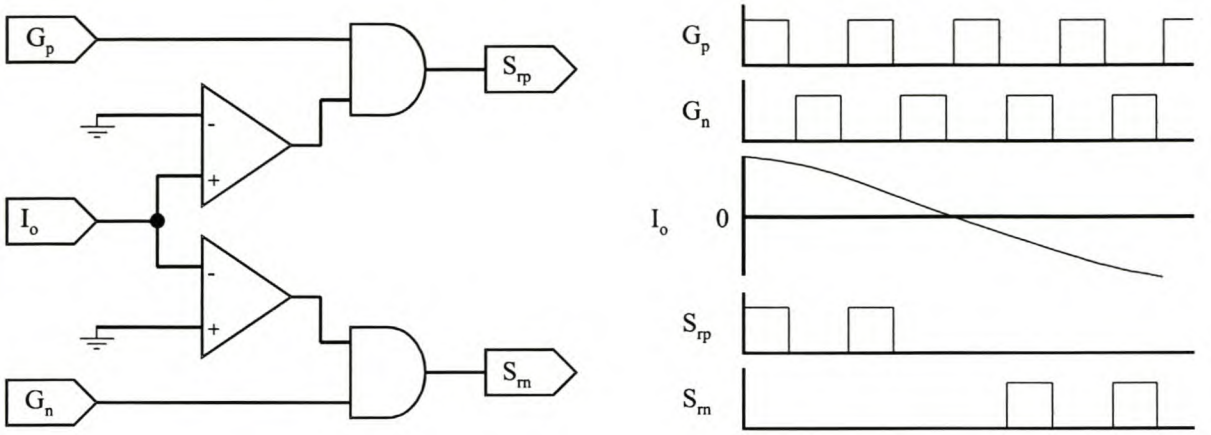
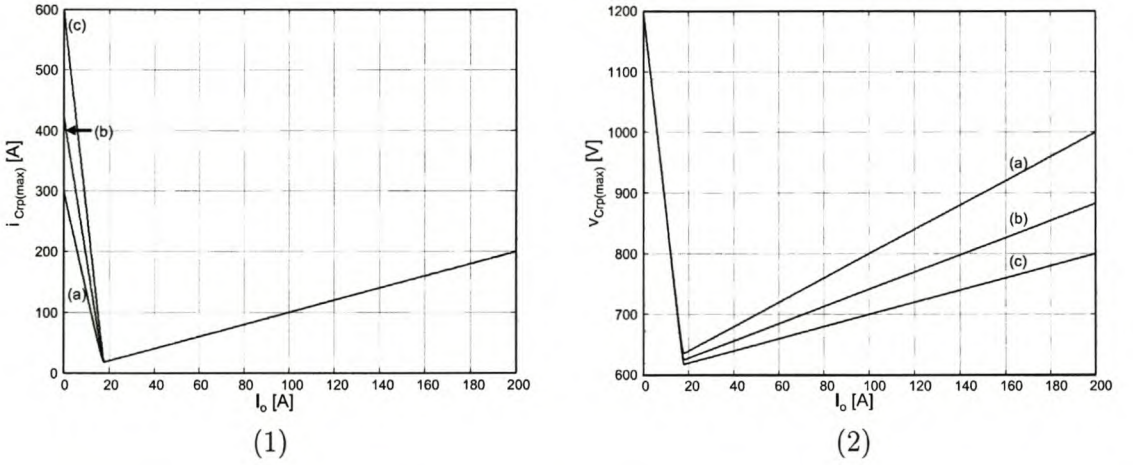


Figure 3.4: Continuous snubber operation.



(1) (2)

Figure 3.5: Peak snubber capacitor current (1) and voltage (2) as function of I_o for continuous snubber operation ($V_d = 600\,V$, $C_r = C_{rb}$): (a) $\frac{L_b}{C_r} = 2$; (b) $\frac{L_b}{C_r} = 1$ (c); $\frac{L_b}{C_r} = \frac{1}{2}$.

current in C_{rp} is just equal to I_o. For small I_o (case 2) the peak current increases until it reaches a maximum at $I_o = 0$. Only with the highest inductance to capacitance ratio (trace (a)) the peak current in the main IGBTs is smaller that the rating given in Table 3.6. If a smaller bus inductance is used, the main IGBTs might desaturate. In Figure 3.5-2 the maximum voltage across the snubber capacitor is shown. This peak voltage will also appear across the main IGBTs. It is clear that for output current levels corresponding to case 1, the voltage overshoot increases as the magnitude of I_o increases. The maximum overshoot can also be controlled by the ratio of L_b to C_r. However, for small output currents (case 2) the voltage overshoot is excessive. It is also not possible to manipulate the overshoot to a significant extent with a variation of snubber component values. At $I_o = 0$, independent of the snubber component values, a voltage overshoot that equals the bus voltage will always occur.

In a practical circuit the voltage overshoot and peak currents will be lower due to damping, non-ideal switching behaviour and extra stray inductance. However, experimental results shown in section 3.8 indicate that over-rated main devices will still have to be used if continuous snubber operation is allowed.

3.3.2 Discontinuous snubber operation

In a standard hard-switching inverter main IGBTs experience voltage overshoot at turn off. This is due to resonance between the parasitic bus inductance and the output capacitance of the device itself. With an inverter fitted with bus inductors but no snubber capacitors, the peak voltage overshoot will be very large due to the high ratio of bus inductance to output capacitance. However, in the combined snubber topology the snubber capacitors will damp the voltage overshoot as soon as it is high enough to forward bias, depending on the sign of the output current, D_{rp} or D_{rn}. The result will be a voltage rise on a snubber capacitor after each turn-off cycle.

Under discontinuous snubber operation (see Figure 2.3) the snubber capacitors are not discharged during low output current levels. Charge buildup on the capacitors during these periods will raise their voltage and compromise the level of damping they can provide. The result is that, although discontinues snubber operation is suitable for the turn-off snubber topology, it cannot necessarily by used for the combined snubber.

To evaluate the usefulness of this operation strategy, an estimate of the extent of this charge buildup during small output current periods should be made. For the estimate it is assumed that, for small positive output current for instance, all the energy stored in L_{bp} will be dumped in C_{rp} at the turn-off of G_p. In Figure 3.6 sinusoidal output current is shown with the corresponding periods of soft- and hard-switching. It can be seen that the longest period with no snubber capacitor discharge, for a given current direction, is

$$\Delta t_1 + \Delta t_2 = \frac{\Delta t_{hard}}{2} \tag{3.13}$$

with

$$\Delta t_{hard} = \frac{4 \arcsin(k)}{\omega_m}, \tag{3.14}$$

$$\omega_m = 2\pi f_m \tag{3.15}$$

and k and f_m as defined in Figure 3.6. The extent of this voltage rise can be approximated by

$$v_{Crp2}^2 = \frac{2 I_o^2 f_s L_b}{C_r} \int_0^{\frac{\Delta t_{hard}}{4}} \sin^2(\omega_m t)\, dt + v_{Crp1}^2 \tag{3.16}$$

with v_{Crp2} and v_{Crp1} at the beginning and at the end of the hard-switching period respectively. The effective voltage rise for the experimental inverter as function of the modulation frequency

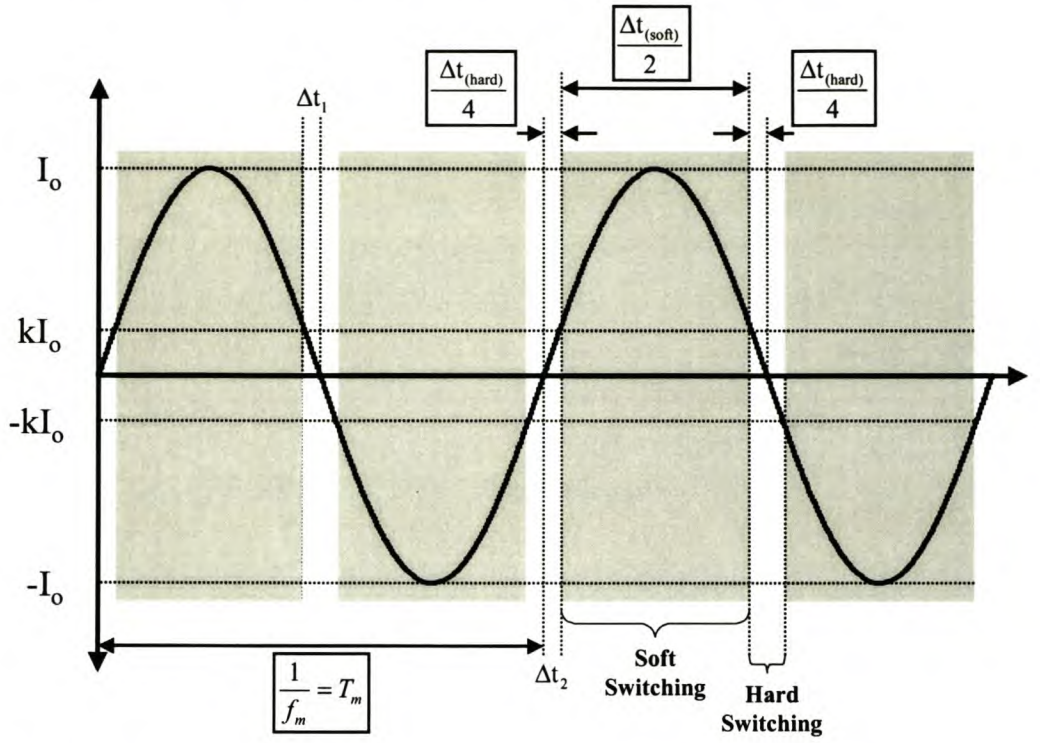


Figure 3.6: Output current and corresponding time intervals of soft- and hard-switching during discontinuous snubber operation.

and the $\frac{L_b}{C_r}$ ratio is shown in Figure 3.7 for $v_{Crp1} = V_d$, $k = 0.1$ and $C_{rp} = C_{rb}$. It can be seen that the charging of the capacitor in the hard-switching period will not result in any dangerous over-voltage problems.

3.3.3 Non-linear operation

As was the case with the turn-off snubber, a possible operation strategy is to postpone the turn-on instant of the opposite main IGBT to a later stage or even leave it off altogether. Although this dynamic adjustment of the blanking time will improve the voltage overshoot and peak current stresses at turn-on, the non-linearities introduced by this strategy complicate the control algorithm of the inverter.

3.3.4 Uni-directional charging assistance

A uni-directional charge assistance strategy, as described in section 2.3.3 for the turn-off snubber topology, can also be used for the combined snubber. In Figure 2.5 a control circuit and timing diagrams for this strategy were shown. The applicability of this control strategy to the combined snubber topology was proven experimentally. The results of this experimental verification can

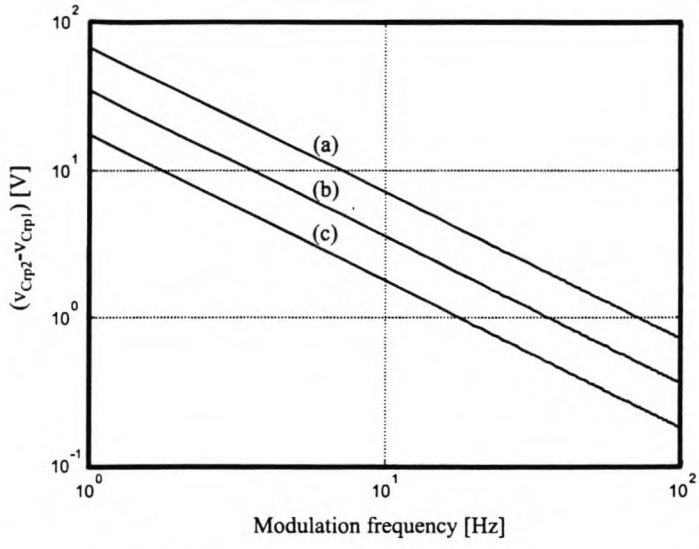


Figure 3.7: Voltage rise in snubber capacitor during hard-switching period with $v_{Crp1} = V_d$, $k = 0.1$ and $C_{rp} = C_{rb}$: (a) $\frac{L_b}{C_r} = 2$; (b) $\frac{L_b}{C_r} = 1$; (c) $\frac{L_b}{C_r} = \frac{1}{2}$.

be found in section 3.8.

3.3.5 Bi-directional charging assistance

Like uni-directional charge assistance, the bi-directional charge assistance strategy (described in section 2.3.4 for the turn-off snubber) can also be used for the combined snubber topology. In Figure 3.8 the expanded combined snubber topology to allow for bi-directional current flow in the auxiliary switches is shown. A possible control circuit was shown in Figure 2.7.

3.3.6 Conclusion

Although all the above-mentioned strategies have certain advantages and disadvantages, the simplest strategy is discontinuous snubber operation. This strategy requires no additions to the existing topology and it was shown theoretically that it is very effective. The special case where the inverter should be able to switch off quickly in a short circuit condition does, however, pose a problem in all of these control strategies, including the discontinuous snubber operation method. In the next section protection of the main and auxiliary switches will be investigated.

3.4 Protection

It was mentioned in section 2.4 that, without effective protection strategies, a soft-switching topology has limited practical value. However, compared to a normal hard-switching inverter,

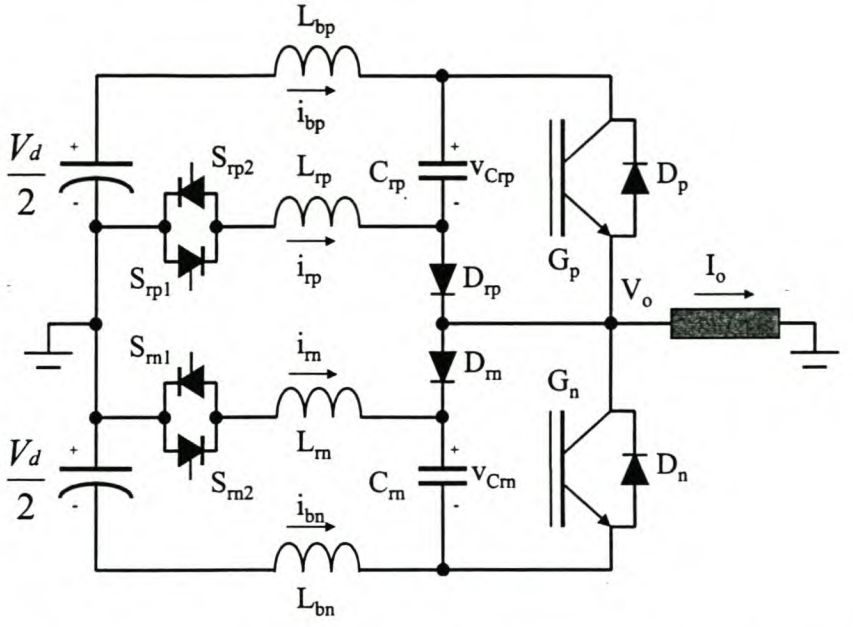


Figure 3.8: Topology expansion for the combined snubber to provide for bi-directional charge assistance.

providing reliable protection is very challenging for most soft-switching topologies.

In section 2.4 possible protection strategies for the turn-off snubber were evaluated. Protection against over current faults, short-circuit conditions and dangerous operating temperatures were treated. In this section a similar evaluation of protection strategies for the combined snubber topology will be conducted. Discontinuous snubber operation and actively controllable auxiliary switches are again assumed.

3.4.1 Over-current and short-circuit protection

In section 2.4 detection techniques for fault and short-circuit current were discussed. It was also mentioned that destructive voltage overshoot, due to the combination of large $\frac{di}{dt}$s and loop inductance, is a major threat when devices carrying large fault currents are switched off. Three methods were also discussed to overcome this problem. They were RCD voltage clamps, soft turn-off and active zener clamps. It was further shown that no special techniques are necessary to protect the main IGBTs in the turn-off snubber topology. However, for the effective protection of the auxiliary switches extra measures are necessary.

The protection strategy for the auxiliary switches was to shut down the devices immediately after the detection of any fault current condition. To limit dangerous voltage overshoot, active zener clamps were added to the switches. This modification was shown in Figure 2.9. This protection strategy can also be directly applied to the auxiliary switches in the combined snubber topology.

Allowable Voltage Overshoot	Normalised Effective Switching Losses
$0.05V_d$	1.63
$0.1V_d$	1.46
$0.2V_d$	1.21
$0.4V_d$	1

Table 3.1: Lowest effective switching losses as function of allowable voltage overshoot under normal load conditions for the experimental inverter.

Unlike the case for the turn-off snubber, protection of the main devices in the combined snubber topology is very difficult. The reason for this is the large bus inductors than will cause severe voltage overshoot at fault current turn-off. The presence of the bus inductors also excludes the use of polymer decoupling capacitors and additional RCD voltage clamps. On the other hand, the bus inductors will restriction fault current growth in the inverter. Thus, compared to a hard-switching or turn-off snubber inverter, smaller fault current levels will occur in the combined snubber topology.

To prevent under-utilisation of IGBTs under normal load conditions, the maximum voltage overshoot at fault current turn-off should not be more than around $0.5V_d$. If it is assumed that C_{rp} will be discharged when G_p has to switch off fault current, it can be seen form equation 3.3 that the voltage overshoot across G_p will be directly proportional the magnitude of this current. If provision for fault currents with a magnitude of up to three times the load current is made, it is clear that the maximum allowable voltage overshoot under normal load conditions should be restricted to around $0.15V_d$. However, with such a relatively low allowable voltage overshoot the effectiveness of the combined snubber topology in reducing switching losses is compromised. A trade-off between reliable protection and reduction in switching losses therefore exists.

The experimental inverter developed in section 3.7 will be used to demonstrate this trade-off. In Table 3.1 the lowest effective switching losses, as function of allowable voltage overshoot under normal load conditions, are listed. The effective switching losses are defined as the actual switching losses in the main IGBTs plus the extra losses in the added snubber components. The values are normalised with respect to the effective switching losses obtainable at an allowable voltage overshoot of $0.4V_d$. The optimisation procedure described in section 3.6 were used to obtain these theoretical values. It is clear that, although there is a improvement in losses with a higher allowable voltage overshoot, the effect is relatively small. This is highlighted even more when the reduction in effective switching losses, compared to the hard-switching case, are calculated. For an allowable voltage overshoot of $0.01V_d$ it is 65% and for $0.4V_d$ it is 76%.

In the above argument is was assumed that the relevant snubber capacitor is discharged when the main IGBT has to switch off under fault current condition. This assumption, depending on the control and the time needed to discharge the capacitors, is not always valid. Without a

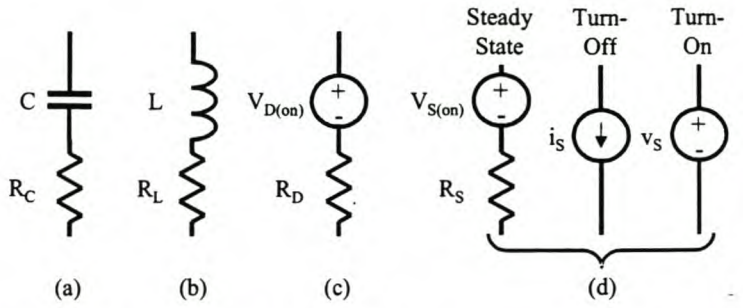


Figure 3.9: Summary of models used for the snubber components and the main switches: (a) Capacitor; (b) Inductor; (c) Diodes; (d) Main and auxiliary switches.

discharged snubber capacitor for damping, the voltage overshoot problem becomes more severe. It is therefore recommended that, together with an moderate allowable voltage overshoot under normal load conditions, extra protection techniques for the main IGBTs should also be used. Both soft turn-off techniques and active zener clamps will provide effective solutions.

3.4.2 Over-temperature protection

The protection of the topology against dangerous operating temperatures can be handled in the same manner as was recommended for the turn-off snubber topology.

3.5 Evaluation of snubber losses

In this section the different loss mechanisms in the main devices and all the added snubber components are studied. Although parasitic capacitive and inductive components have a major influence on the effectiveness of the snubber (see [58]), the dependence of these parasitics on actual component values and snubber construction complicates modeling considerably. All parasitics are therefore ignored in the loss evaluation process.

A number of studies on the switching behaviour of IGBTs under soft-switching conditions can be found in the relevant literature [23], [26], [30]. The accurate prediction of the behaviour of an IGBT under such conditions does, however, involve complicated simulations requiring device parameters not readily available. As a first step tail-forming characteristics are assumed to model both the turn-off and turn-on switching behaviour of the main and auxiliary switches [20]. It is further assumed that the snubber does not alter the switching behaviour of the main IGBTs. After optimisation and construction the modified switching behaviour can be measured. The optimisation process can then be repeated with the adjusted parameters to obtain more accurate values.

As an alternative to numerical simulation, general analytical expressions were derived to describe the losses in the main and auxiliary inverter components. The process of deriving

these loss expressions can be summarised as follows:

1. Expressions describing relevant circuit voltages and currents for different conditions and time intervals were obtained. In this process parasitics were neglected and diodes and passive components were assumed to be ideal. It was further assumed that both the main and auxiliary switches have linear, tail-forming switching behaviour and no on-state voltage. Positive load current was also assumed throughout and the symmetry of the topology was later used to handle negative output current.

2. The voltage and current expressions were then used together with more complete models for the snubber components and main switches to derive loss expressions. In Figure 3.9 a summary of these component models is shown. Capacitors and inductors are modelled as ideal passive components with an ESR and diodes are modelled as an on-state voltage in series with a resistance. All switches are modelled as a current source during turn-off, a voltage source during turn-on and during conduction the auxiliary switches are modelled as an on-state voltage with a series resistance.

3. The loss expressions were obtained with a process of symbolic integration. Due to the complexity involved, Maple V was used as a tool to perform this task.

The switching cycle is divided into different time intervals that are treated separately. The time intervals will be grouped into three major categories, namely main IGBT turn-off, main IGBT turn-on and the snubber capacitor discharge cycle. The time instances that define the boundaries between time intervals are listed in Table 3.2. It is important to note that the definitions for time instances used in this section are not the same as the ones used in section 3.2. The derived expressions for voltages, currents and other variables will be listed separately for each specific case and time interval. The loss expressions will not be given in this chapter, but a complete listing can be found in Appendix A.

3.5.1 Main IGBT turn-off

The collector current of the main device G_p during turn-off is described by

$$\begin{aligned} i_{c_{(G_p)}} &= I_o\left(1-(1-A_m)\frac{t}{t_{fim}}\right) \text{ for } 0 \le t < t_{fim} \\ i_{c_{(G_p)}} &= A_m I_o\left(1-\frac{t-t_{fim}}{t_{tim}}\right) \text{ for } t_{fim} \le t < (t_{fim}+t_{tim}) \end{aligned} \tag{3.17}$$

where $A_m I_o$ is the knee-point current, t_{fim} is the current fall duration and t_{tim} is the current tail duration. This collector current is shown in Figure 3.10a. The active part of the circuit during turn-off and the equivalent circuit used for loss calculations are shown in Figure 3.11. Only three cases that can occur at discontinuous snubber operation are considered. The occurrence

Time Instance	Description
0	Beginning of switching cycle - G_p turns off.
t_1	Current fall time for G_p expires ($t_1 = t_{fim}$).
t_2	Current tail time for G_p expires ($t_2 = t_1 + t_{tim}$).
t_3	Blanking time expires and G_n switches on ($t_3 = t_b$).
t_4	Turn-on instant of G_p.
t_5	Voltage fall time of G_p expires ($t_5 = t_4 + t_{fvm}$).
t_6	Voltage tail time of G_p expires ($t_6 = t_5 + t_{tvm}$).
t_7	Snubber capacitor discharge is started - S_{rp} is triggered.
t_8	Voltage fall time of S_{rp} expires ($t_8 = t_7 + t_{fva}$).
t_9	Voltage tail time of S_{rp} expires ($t_9 = t_8 + t_{tva}$).
t_{10}	Voltage across C_{rp} reaches zero.
t_{11}	Current in L_{rp} reaches zero.
t_{12}	End of switching cycle ($t_{12} = \frac{1}{f_s}$).

Table 3.2: Description of time instances used for the loss evaluation of the combined snubber.

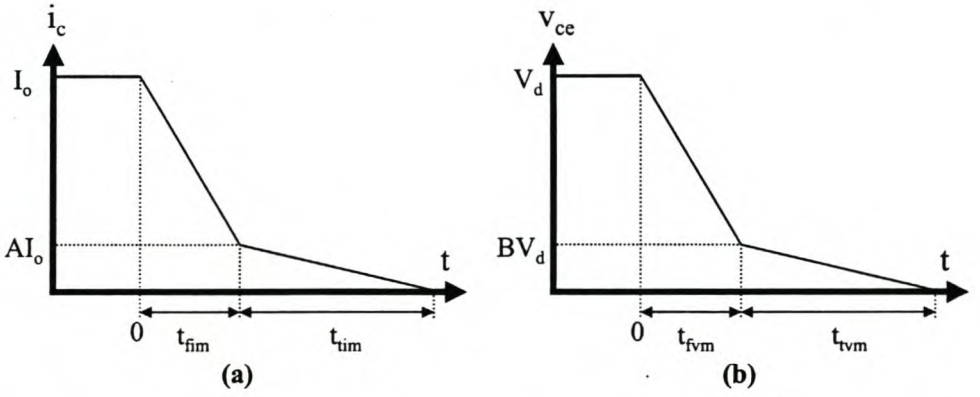


Figure 3.10: Models for switching behaviour of main IGBTs: (a) Turn-off; (b) Turn-on.

Case	t_{vr}	t_{cz}
1	$t_1 \leq t_{vr} < t_2$	$t_{cz} < t_2$
2	$t_1 \leq t_{vr} < t_2$	$t_2 \leq t_{cz}$
3	$t_2 \leq t_{vr} < t_3$	

Table 3.3: Definition of three cases at main IGBT turn-off.

of a specific case depends on snubber component values and output current magnitude. To distinguish between the three cases, the capacitor voltage rise time t_{vr} is defined as the time when v_{Crp} reaches V_d and t_{cz} is defined as the time when resonance between the bus inductors and C_{rp} is complete. In Table 3.3 the three cases are classified with respect to these two parameters. In Figure 3.12 simulation results for examples of these three different cases are shown.

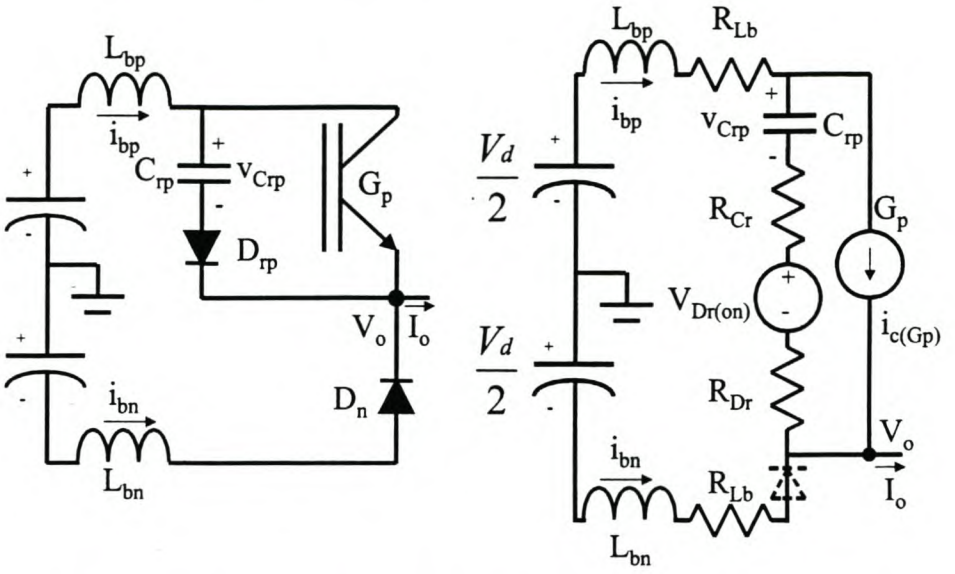


Figure 3.11: Active part of the combined snubber topology during turn-off and the equivalent circuit used for loss calculations.

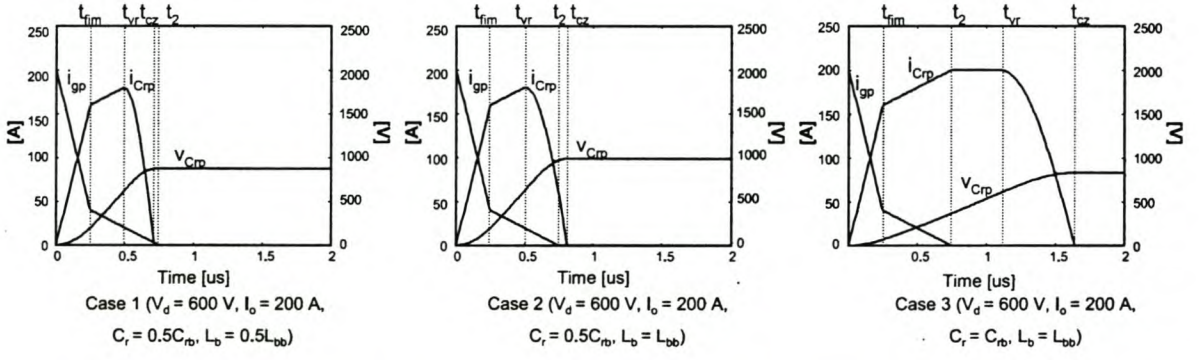


Figure 3.12: Three cases of combined snubber operation during main IGBT turn-off.

$0 \leq t < t_1$ $(t_1 = t_{fim})$

In this period the various voltages and currents in the relevant components can be described by the same equations for all the cases. The current in the main IGBT is as described in equation 3.17. The currents in L_{bp} and C_{rp} and the voltage across the snubber capacitor are given by

$$i_{bp} = I_o \tag{3.18}$$

$$i_{Crp(a)} = \frac{I_o\,(1 - A_m)\,t}{t_{fim}} \tag{3.19}$$

$$v_{Crp(a)} = \frac{1}{C_r}\int_0^t i_{Crp(a)}\,(\tau)\,d\tau$$

$$= \frac{I_o\,(1-A_m)\,t^2}{2\,C_r\,t_{fim}} \tag{3.20}$$

$t_1 \leq t < t_2\ (t_2 = t_{fim} + t_{tim})$

For this interval the collector current of G_p is also given in equation 3.17. The possible cases are divided into two groups. The first group consists of case 3 and the second group consists of cases 1 and 2. Case 3 corresponds to an output current that satisfies

$$I_o < \frac{2\left(V_d - v_{Crp(a)}(t_1)\right)C_r}{(2-A_m)\,t_{tim}}. \tag{3.21}$$

For case 3 i_{bp}, i_{Crp} and v_{Crp} are given by

$$i_{bp} = I_o \tag{3.22}$$

$$i_{Crp(b)} = I_o - A_m I_o\left(1 - \frac{t-t_{fim}}{t_{tim}}\right) \tag{3.23}$$

$$\begin{aligned} v_{Crp(b)} &= \frac{1}{C_r}\int_{t_1}^{t} i_{Crp(b)}\,(\tau)\,d\tau + v_{Crp(a)}(t_1) \\ &= \frac{\frac{I_o A_m\left(t^2-t_{fim}^2\right)}{2t_{tim}} + I_o\,(t-t_{fim}) - A_m I_o\left(1+\frac{t_{fim}}{t_{tim}}\right)(t-t_{fim})}{C_r} + \\ &\quad v_{Crp(a)}(t_1). \end{aligned} \tag{3.24}$$

For the second group a new variable is defined, namely t_{vr}. This is the time instant when v_{Crp} reaches V_d and D_n becomes forward biased. For both the cases in this group t_{vr} can be expressed as

$$t_{vr} = t_2 + \frac{\sqrt{I_o^2 t_{tim}^2\,(A_m-1)^2 + 2I_o A C_r t_{tim}\left(V_d - v_{Crp(a)}(t_1)\right)} - I_o t_{tim}}{I_o A}. \tag{3.25}$$

Equations 3.22, 3.23 and 3.24 are also valid for this group for time $t_1 \leq t < t_{vr}$. After t_{vr} a period of resonance is started. The current in the bus inductors and the snubber capacitor current and voltage for this period of resonance are

$$i_{bp} = c_1 \cos\omega_1\,(t-t_{vr}) + c_2 \sin\omega_1\,(t-t_{vr}) - \frac{AI_o t}{t_{tim}} + AI_o\left(1+\frac{t_{fim}}{t_{tim}}\right) \tag{3.26}$$

$$i_{bn} = I_o - i_{bp} \tag{3.27}$$

$$i_{Crp(c)} = c_1 \cos\omega_1\,(t-t_{vr}) + c_2 \sin\omega_1\,(t-t_{vr}) \tag{3.28}$$

$$\begin{aligned} v_{Crp(c)} &= \frac{1}{C_r}\int_{t_{vr}}^{t} i_{Crp(c)}\,(\tau)\,d\tau + v_{Crp(b)}(t_{vr}) \\ &= \frac{c_1 \sin\omega_1\,(t-t_{vr}) - c_2\cos\omega_1\,(t-t_{vr}) + c_2}{C_r\omega_1} + V_d \end{aligned} \tag{3.29}$$

with

$$c_1 = I_o\,(1-A_m) + \frac{I_o A_m\,(t_{vr}-t_{fim})}{t_{tim}} \tag{3.30}$$

$$c_2 = \frac{A_m I_o}{\omega_1 t_{tim}} \tag{3.31}$$

and ω_1 as defined in section 3.2. For the first case a second variable is also defined. This variable, t_{cz}, is the time when resonance is completed and the current in C_{rp} reaches zero. For case 1 this time is smaller than t_2 and can be expressed as

$$t_{cz} = t_{vr} - \frac{\arctan(\frac{c_1}{c_2})}{\omega_1}. \tag{3.32}$$

The relevant current and voltage expressions for case 1 during $t_{cz} \leq t < t_2$ are

$$i_{bp} = i_{c_{(G_p)}} = A_m I_o \left(1 - \frac{t - t_{fim}}{t_{tim}}\right) \tag{3.33}$$

$$i_{bn} = I_o - A_m I_o \left(1 - \frac{t - t_{fim}}{t_{tim}}\right) \tag{3.34}$$

$$v_{ce_{(G_p)}} = V_d + \frac{2L_b A_m I_o}{t_{tim}} \tag{3.35}$$

$$v_{Crp(max)} = v_{Crp(c)}(t_{cz}). \tag{3.36}$$

For the second case t_{cz} is larger than t_2.

$t_2 \leq t < t_4$

The different cases, as defined in Figure 3.12 and Table 3.3, will be treated separately. The time period will also be further sub-divided into smaller intervals for clarity.

Case 3

For $t_2 \leq t < t_{vr}$:

The expressions for i_{bp}, i_{bn}, i_{Crp} and v_{Crp} before v_{Crp} reaches V_d are

$$i_{bp} = i_{Crp(d)} = I_o \tag{3.37}$$

$$i_{bn} = 0 \tag{3.38}$$

$$\begin{aligned} v_{Crp(d)} &= \frac{1}{C_r}\int_{t_2}^{t} i_{Crp(d)}(\tau)\, d\tau + v_{Crp(b)}(t_2) \\ &= \frac{I_o(t - t_2)}{C_r} + v_{Crp(b)}(t_2). \end{aligned} \tag{3.39}$$

The time instant when v_{Crp} reaches the bus voltage can be expressed as

$$t_{vr} = t_2 + \frac{C_r\left(V_d - v_{Crp(b)}(t_2)\right)}{I_o}. \tag{3.40}$$

For $t_{vr} \leq t < t_{cz}$:

At t_{vr} resonance between the bus inductors and C_{rp} starts. The expressions for i_{bp}, i_{bn}, i_{Crp} and v_{Crp} during this period of resonance are

$$i_{bp} = i_{Crp(e)} = I_o \cos\omega_1 (t - t_{vr}) \tag{3.41}$$

$$i_{bn} = I_o (1 - \cos\omega_1 (t - t_{vr})) \tag{3.42}$$

$$\begin{aligned} v_{Crp(e)} &= \frac{1}{C_r}\int_{t_{vr}}^{t} i_{Crp(e)}(\tau)\, d\tau + v_{Crp(d)}(t_{vr}) \\ &= \frac{I_o \sin\omega_1 (t - t_{vr})}{C_r\omega_1} + V_d. \end{aligned} \tag{3.43}$$

The resonant cycle continues until time t_{cz} when the full load current is carried by L_{bn} and D_n. This time can be expressed as

$$t_{cz} = t_{vr} + \frac{\pi}{2\omega_1}. \tag{3.44}$$

For $t_{cz} \leq t < t_4$:
The constant bus inductor currents and snubber capacitor voltage and current are

$$\begin{aligned} i_{bp} &= i_{Crp} = 0 && (3.45)\\ i_{bn} &= I_o && (3.46)\\ V_{Crp(max)} &= v_{Crp(e)}(t_{cz}) && (3.47) \end{aligned}$$

Case 2

For $t_2 \leq t < t_{cz}$:
At t_2 the resonance between the bus inductors and snubber capacitor is still in progress. The resonant cycle continues until time t_{cz}. For this period the expressions for i_{bp}, i_{bn}, i_{Crp} and v_{Crp} are

$$\begin{aligned} i_{bp} &= i_{Crp(f)} = c_{12}\cos\omega_1(t-t_2) + c_{13}\sin\omega_1(t-t_2) && (3.48)\\ i_{bn} &= I_o - c_{12}\cos\omega_1(t-t_2) - c_{13}\sin\omega_1(t-t_2) && (3.49)\\ v_{Crp(f)} &= \frac{1}{C_r}\int_{t_2}^{t} i_{Crp(f)}(\tau)\,d\tau + v_{Crp(c)}(t_2) \\ &= \frac{c_{12}\sin\omega_1(t-t_2) - c_{13}\cos\omega_1(t-t_2) + c_{13}}{C_r\omega_1} + v_{Crp(c)}(t_2) && (3.50) \end{aligned}$$

with

$$\begin{aligned} c_{12} &= c_1\cos\omega_1(t_2-t_{vr}) + c_2\sin\omega_1(t_2-t_{vr}) && (3.51)\\ c_{13} &= \frac{AI_o}{\omega_1 t_{tim}} - c_1\sin\omega_1(t_2-t_{vr}) + c_2\cos\omega_1(t_2-t_{vr}) && (3.52) \end{aligned}$$

and t_{cz} can be expressed as

$$t_{cz} = t_2 - \frac{\arctan\left(\frac{c_{12}}{c_{13}}\right)}{\omega_1}. \tag{3.53}$$

For $t_{cz} \leq t < t_4$:
The constant bus inductor currents and snubber capacitor voltage and current are

$$\begin{aligned} i_{bp} &= i_{Crp} = 0 && (3.54)\\ i_{bn} &= I_o && (3.55)\\ V_{Crp(max)} &= v_{Crp(f)}(t_{cz}). && (3.56) \end{aligned}$$

Case 1

At time instant t_2 the full load current is already carried by L_{bn} and D_n. The expressions

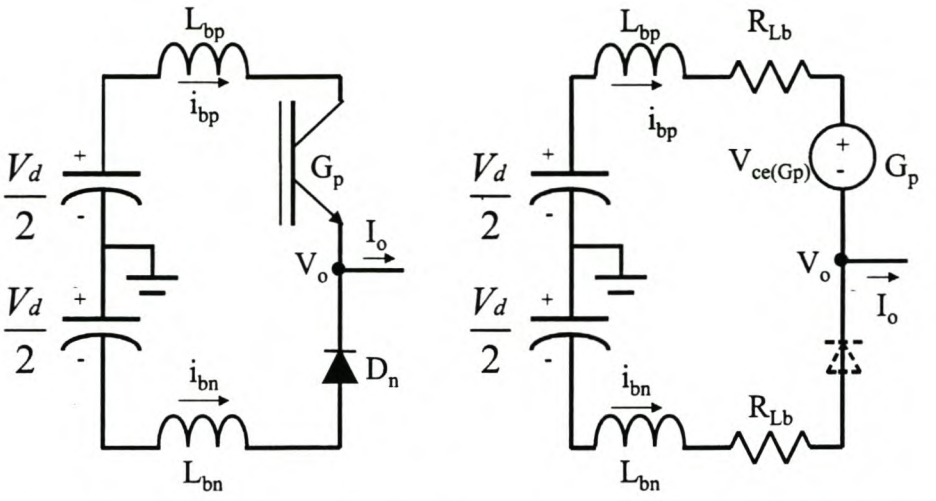


Figure 3.13: Active part of the snubber topology during turn-on and equivalent circuit used for loss calculations.

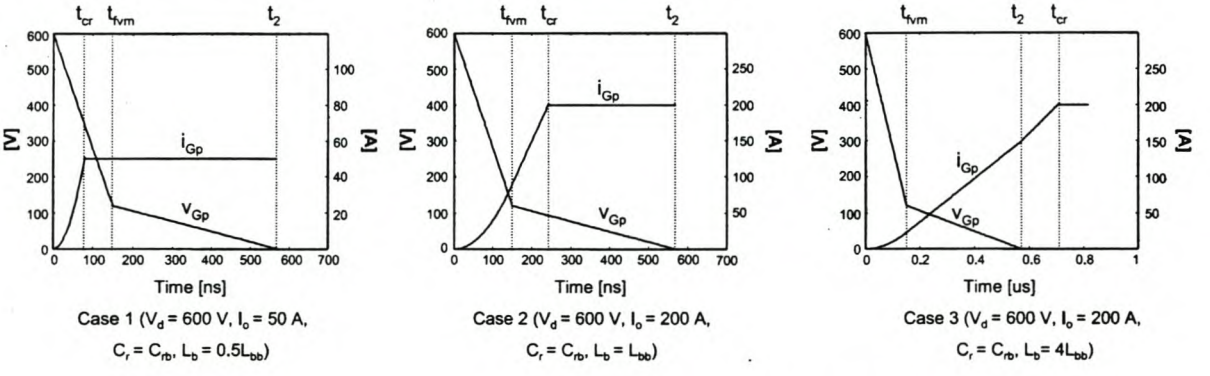


Figure 3.14: Three cases of combined snubber operation during main IGBT turn-on.

for the relevant currents and voltages are

$$i_{bp} = i_{Crp} = 0 \tag{3.57}$$

$$i_{bn} = I_o \tag{3.58}$$

$$V_{Crp(max)} = v_{Crp(c)}(t_{cz}) \tag{3.59}$$

with t_{cz} as defined in equation 3.32.

3.5.2 Main IGBT turn-on

The collector-emitter voltage of the main devices during turn-on is described by

$$v_{ce_{(G_p)}} = V_d \left(1 - (1 - B_m)\frac{t - t_4}{t_{fvm}}\right) \text{ for } t_4 \leq t < (t_4 + t_{fvm})$$

Case	t_{cr}
1	$t_4 \leq t_{cr} < t_5$
2	$t_5 \leq t_{cr} < t_6$
3	$t_6 \leq t_{cr}$

Table 3.4: Definition of three cases at main IGBT turn-on.

$$v_{ce(G_p)} = B_m V_d \left(1 - \frac{t - (t_4 + t_{fvm})}{t_{tvm}}\right) \text{ for } (t_4 + t_{fvm}) \leq t < (t_4 + t_{fvm} + t_{tvm}) \quad (3.60)$$

where $B_m V_d$ is the knee-point voltage, t_{fvm} is the voltage fall duration and t_{tvm} is the voltage tail duration. In Figure 3.10b this collector-emitter voltage model is illustrated. In Figure 3.13 the active part of the circuit during turn-on, as well as the equivalent circuit used for loss calculations, is shown. Simulation results for examples of three different cases that are considered are shown in Figure 3.14. The occurrence of a specific case again depends on snubber component values and output current magnitude. To distinguish between the cases, t_{cr} is defined as the time instant when the full load current is carried by G_p. In Table 3.4 the three cases are classified with respect to this parameter.

The different cases will once again be treated separately. The expressions for the relevant currents, voltages, time instances and constants will be listed for each sub-interval.

$t_4 \leq t < t_5$ $(t_5 = t_4 + t_{fvm})$

For this period the collector-emitter voltage of G_p is given in equation 3.60. The possible cases are divided into two groups. The first group consists of case 1 and the second group consists of cases 2 and 3. The currents in the bus inductors for the second group can be expressed as

$$i_{bp(a)} = \frac{V_d (1 - B_m) (t - t_4)^2}{4 L_b t_{fvm}} \quad (3.61)$$

$$i_{bn(a)} = I_o - \frac{V_d (1 - B_m) (t - t_4)^2}{4 L_b t_{fvm}} \quad (3.62)$$

for the whole interval. For case 1 equations 3.61 and 3.62 are also valid until time instant t_{cr} when the full load current is carried by G_p. This time instant can be expressed as

$$t_{cr} = t_4 + \frac{\sqrt{4 V_d I_o L_b t_{fvm} (1 - B_m)}}{V_d (1 - B_m)}. \quad (3.63)$$

After this time instant the bus inductor currents are constant with values of

$$i_{bp} = I_o \quad (3.64)$$

$$i_{bn} = 0. \quad (3.65)$$

$t_5 \leq t < t_6$ $(t_6 = t_5 + t_{tvm})$

The collector-emitter voltage of G_p is also given in equation 3.60.

Case 3

The bus inductor currents for this period are

$$i_{bp(b)} = \frac{V_d(1-B_m)(t-t_5)}{2L_b} + \frac{B_m V_d (t-t_5)^2}{4L_b t_{tvm}} + i_{bp(a)}(t_5) \tag{3.66}$$

$$i_{bn(b)} = I_o - \frac{V_d(1-B_m)(t-t_5)}{2L_b} - \frac{B_m V_d (t-t_5)^2}{4L_b t_{tvm}} - i_{bp(a)}(t_5). \tag{3.67}$$

Case 2

For $t_5 \leq t < t_{cr}$:

Expressions 3.66 and 3.67 are also valid for case 2 for $t_5 \leq t < t_{cr}$ where t_{cr} can be expressed as

$$t_{cr} = t_6 - \frac{V_d t_{tvm} \pm \sqrt{V_d^2 t_{tvm}^2 (1-B_m)^2 + 4V_d B_m L_b t_{tvm}\left(I_o - i_{bp(a)}(t_5)\right)}}{V_d B_m}. \tag{3.68}$$

For $t_{cr} \leq t < t_6$:

After G_p takes over the full load current and D_n turns off, the constant bus inductor currents are expressed by equations 3.64 and 3.65.

Case 1

For the whole period equations 3.64 and 3.65 describe the bus inductor currents.

$t_6 \leq t < t_7$

At time t_6 the collector-emitter voltage of G_p has reached its on-state value. The period comes to an end when the discharge cycle of the snubber capacitor is initiated at t_7.

Case 3

For $t_6 \leq t < t_{cr}$:

At t_6 part of the load current is still carried by L_{bn} and D_n. The bus inductor currents are described by

$$i_{bp(c)} = \frac{V_d(t-t_6)}{2L_b} + i_{bp(b)}(t_6) \tag{3.69}$$

$$i_{bn(c)} = I_o - \frac{V_d(t-t_6)}{2L_b} - i_{bp(b)}(t_6) \tag{3.70}$$

and the end of this period can be expressed as

$$t_{cr} = t_6 + \frac{2L_b\left(I_o - i_{bp(b)}(t_6)\right)}{V_d}. \tag{3.71}$$

For $t_{cr} \leq t < t_7$:

Equations 3.64 and 3.65 describe the constant bus inductor currents.

Cases 1 and 2

For the whole period equations 3.64 and 3.65 describe the bus inductor currents.

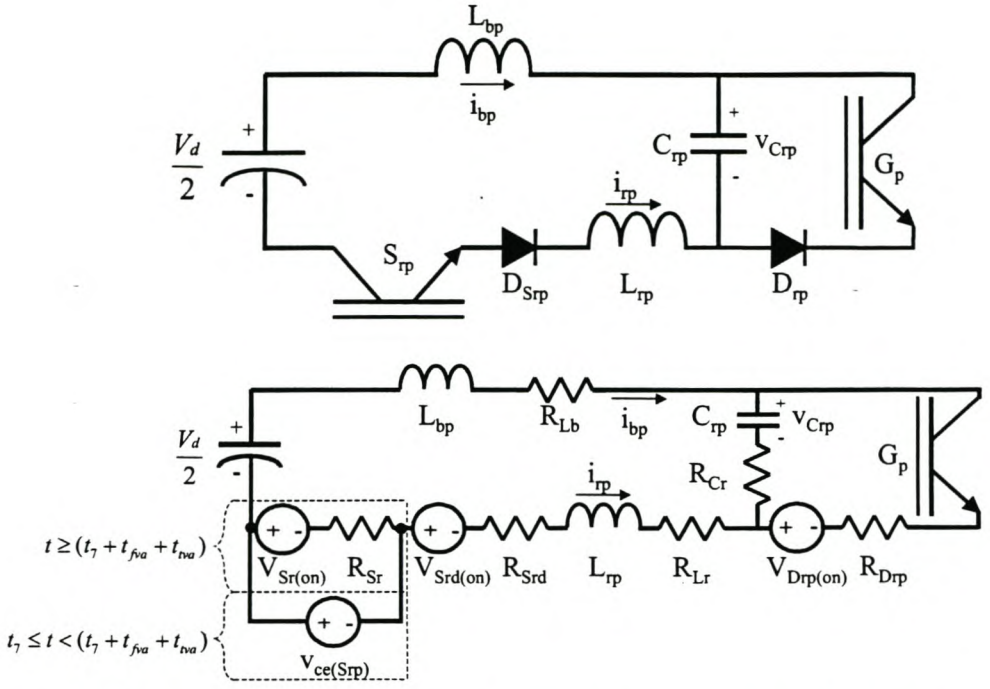


Figure 3.15: Auxiliary discharge circuit with the equivalent circuit used for loss calculations.

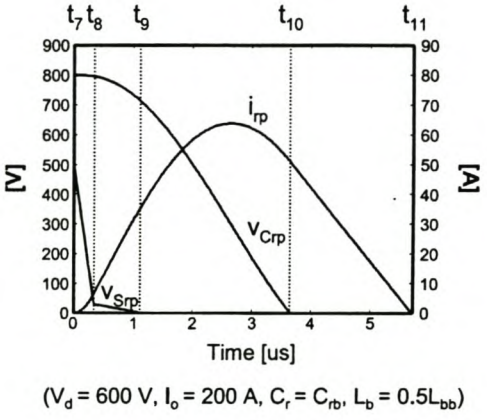


Figure 3.16: Simulation results illustrating the capacitor discharge cycle.

3.5.3 Snubber capacitor discharge

The collector-emitter voltage of the auxiliary switch during the start of capacitor discharge is described by

$$v_{ce(Srp)} = V_{init}\left(1-(1-B_a)\frac{t-t_7}{t_{fva}}\right) \text{ for } t_7 \le t < (t_7+t_{fva})$$
$$v_{ce(Srp)} = B_a V_{init}\left(1-\frac{t-(t_7+t_{fva})}{t_{tva}}\right) \text{ for } (t_7+t_{fva}) \le t < (t_7+t_{fva}+t_{tva}) \quad (3.72)$$

Cases at main IGBT turn-off.	$V_{init} = V_{Crp(max)} - \frac{V_d}{2}$ with $V_{Crp(max)}$ as defined in equation:
1	3.36
2	3.56
3	3.59

Table 3.5: Definition of V_{init} for the three cases that occur at main IGBT turn-off.

with V_{init} the difference between the peak voltage overshoot on the snubber capacitor during the main IGBT turn-off and half the bus voltage. In Table 3.5 the expressions for V_{init} is given for the three different cases that occur at main IGBT turn-off. $B_a V_{init}$ is once again the knee-point voltage, t_{fva} is the voltage fall duration and t_{tva} is the voltage tail duration. In Figure 3.15 the auxiliary discharge circuit and the equivalent circuit used for loss calculations are shown. Although the auxiliary switch is shown as an IGBT in series with a blocking diode, the model is completely general and can be used for any other suitable power electronic device. However, it is assumed that the turn-on time of the auxiliary switches are always shorter that the time necessary to discharge the snubber capacitor. Only one case is therefore considered. In Figure 3.16 simulation results illustrating the capacitor discharge cycle are shown. Also indicated in Figure 3.16 are time instances defined in Table 3.2 that are relevant to the discharge cycle.

$t_7 \leq t < t_8 \ (t_8 = t_7 + t_{fva})$

The collector-emitter voltage of S_{rp} is given in equation 3.72. The current in inductor L_{rp} and the snubber capacitor voltage and current are given by

$$i_{rp(a)} = -i_{Crp(g)} = c_{14} \cos \omega_2 (t - t_7) + c_{15} \tag{3.73}$$

$$\begin{aligned} v_{Crp(g)} &= \frac{1}{C_r} \int_{t_7}^{t} i_{Crp(g)}(\tau)\, d\tau + V_{Crp(max)} \\ &= -\left(\frac{c_{15}\omega_2 (t - t_7) + c_{14} \sin \omega_2 (t - t_7)}{C_r \omega_2} \right) + V_{Crp(max)} \end{aligned} \tag{3.74}$$

with

$$c_{15} = -c_{14} = \frac{C_r \left(V_{Crp(max)} - \frac{V_d}{2} \right) (1 - B_a)}{t_{fva}} \tag{3.75}$$

and ω_2 as defined in section 3.2. The expression for $V_{Crp(max)}$ will depend on the case that occurred at main IGBT turn-off (see Table 3.5).

$t_8 \leq t < t_9 \ (t_9 = t_8 + t_{tva})$

The collector-emitter voltage of S_{rp} is also given in equation 3.72. The current in L_{rp} and the snubber capacitor voltage and current are given by

$$i_{rp(b)} = -i_{Crp(h)} = c_{16} \cos \omega_2 (t - t_8) + c_{17} \sin \omega_2 (t - t_8) + c_{18} \tag{3.76}$$

$$\begin{aligned} v_{Crp(h)} &= \frac{1}{C_r}\int_{t_8}^{t} i_{Crp(h)}(\tau)\, d\tau + v_{Crp(g)}(t_8) \\ &= \frac{1}{C_r\omega_2}\left(c_{17}\left(\cos\omega_2(t-t_8)-1\right) - c_{16}\sin\omega_2(t-t_8) - \right. \\ &\quad \left. c_{18}\omega_2(t-t_8)\right) + v_{Crp(g)}(t_8) \end{aligned} \tag{3.77}$$

with

$$c_{16} = c_{14}\cos\omega_2(t_8-t_7) + c_{15} - c_{18} \tag{3.78}$$

$$c_{17} = -c_{14}\sin\omega_2(t_8-t_7) \tag{3.79}$$

$$c_{18} = \frac{B_a C_r\left(V_{Crp(max)} - \frac{V_d}{2}\right)}{t_{tva}}. \tag{3.80}$$

$t_9 \leq t < t_{10}$

At t_{10} v_{Crp} reaches zero and D_{rp} clamps it to that value. The expressions for the relevant voltages and currents before this event are

$$i_{rp(c)} = -i_{Crp(k)} = c_{19}\cos\omega_2(t-t_9) + c_{20}\sin\omega_2(t-t_9) \tag{3.81}$$

$$v_{Crp(k)} = \frac{1}{C_r}\int_{t_9}^{t} i_{Crp(k)}(\tau)\, d\tau + v_{Crp(h)}(t_9) \tag{3.82}$$

$$= -\frac{c_{20}\left(1-\cos\omega_2(t-t_9)\right) + c_{19}\sin\omega_2(t-t_9)}{C_r\omega_2} + v_{Crp(h)}(t_9) \tag{3.83}$$

with

$$c_{19} = c_{16}\cos\omega_2(t_9-t_8) + c_{17}\sin\omega_2(t_9-t_8) + c_{18} \tag{3.84}$$

$$c_{20} = -c_{16}\sin\omega_2(t_9-t_8) + c_{17}\cos\omega_2(t_9-t_8). \tag{3.85}$$

The expression for time instant t_{10} is

$$t_{10} = t_9 + \frac{\arctan(a_1, a_2)}{\omega_2} \tag{3.86}$$

with

$$\begin{aligned} a_1 &= \frac{\pm\sqrt{c_{20}^2\left(c_{19}^2 - v_{Crp(h)}^2(t_9)C_r^2\omega_2^2 + 2c_{20}v_{Crp(h)}(t_9)C_r\omega_2\right)}}{c_{19}^2+c_{20}^2} + \\ &\quad \frac{v_{Crp(h)(t_9)}C_r\omega_2 c_{19} - c_{19}c_{20}}{c_{19}^2+c_{20}^2} \end{aligned} \tag{3.87}$$

$$a_2 = 1 - \frac{v_{Crp(h)}(t_9)C_r\omega_2}{c_{20}} + \frac{c_{19}a_1}{c_{20}} \tag{3.88}$$

and $\arctan(a_1, a_2)$ defined as

$$\arctan(a_1, a_2) = i\ln\left(\frac{a_2 + ia_1}{\sqrt{a_2^2+a_1^2}}\right). \tag{3.89}$$

$t_{10} \leq t < t_{11}$

At t_{11} the current in L_{rp} reaches zero and this marks the end of the capacitor discharge cycle. The current in L_{rp} for this final part of the discharge cycle is described by

$$i_{rp(d)} = i_{rp(c)}(t_{10}) - \frac{V_d\,(t - t_{10})}{2L_r}. \tag{3.90}$$

Time instant t_{11} can be expressed as

$$t_{11} = t_{10} + \frac{2i_{rp(c)}(t_{10})L_r}{V_d}. \tag{3.91}$$

$t_{11} \leq t < t_{12}$

After t_{11} the resonant cycle is completed. The full load current is carried by G_p and L_{bp} and all the various currents and voltage levels in the circuit remains constant until the next switching cycle starts at t_{12}. The constant values are

$$i_{rp} = 0 \tag{3.92}$$

$$i_{bp} = I_o \tag{3.93}$$

$$v_{Crp} = 0. \tag{3.94}$$

3.6 Optimal snubber design procedure

In the previous section analytical expressions were derived to describe the losses in the snubber components and the switching losses in the main IGBTs. These expressions will be used in this section as the basis of an optimisation algorithm. In [55] this design optimisation of the combined snubber topology was also reported. The aim of the optimisation algorithm is to determine snubber component values that will result is the lowest overall losses in an inverter fitted with the combined snubber. Before the optimisation can be done, certain parameters must be decided upon. They are:

1. **The blanking time.**
   The minimum blanking time in a converter is determined by the switching behaviour of the main devices. It is usually chosen to be as small as possible to limit non-linearity in the control of the inverter. In an inverter fitted with the combined snubber, the blanking time will also determine the magnitude of the load current where snubber operation is ceased. The blanking time is therefore also a parameter that can be varied in an optimisation process to achieve lower losses. Due to the relatively small effect of such a variation and the extra complexity introduced by a fourth optimisation parameter, it is suggested that t_b should be kept fixed at a value indicated by device data sheets.

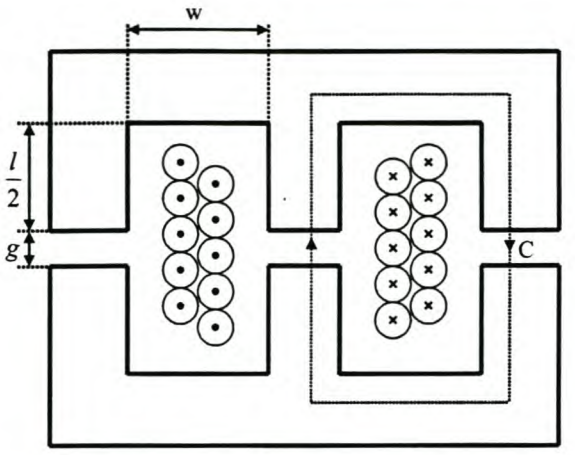


Figure 3.17: Cross-section of ferrite core winding area.

2. **Switching frequency and the maximum duty cycle.**
   The switching frequency and maximum duty cycle will determine the actual time available for the snubber capacitor discharge cycle. It will therefore also influence the peak current rating of the auxiliary switches and will place upper bounds on the snubber capacitor and resonant inductor values. The switching frequency and maximum duty cycle are usually determined by external factors like filter size and dc bus voltage.

3. **Maximum voltage overshoot and peak current ratings.**
   Before optimisation a decision has to be made regarding the maximum allowable voltage overshoot on the main IGBTs and the peak current rating of the auxiliary switches. The maximum allowable voltage overshoot will depend on the ratings of the main devices and the desired dc bus voltage. Similar to a normal hard-switching inverter, a maximum voltage overshoot of $\frac{V_d}{2}$ can usually be tolerated. The peak current rating of the auxiliary switches is typically chosen to be $\frac{I_{o(max)}}{3}$. For an inverter with smaller f_s and D_{max} an even lower rating will be suitable.

4. **ESR of snubber components as function of their value.**
   In order to implement the optimisation algorithm, an estimate of the ESR for the capacitor and inductors as function of their values should be calculated. These relationships will be developed in the following paragraphs.

In Figure 3.17 a view of a general winding area for a magnetic core is shown. The use of such a core, made of high-frequency magnetic materials like ferrite, will minimise the size of the inductors and limit the stray fields. Consider now the integration path shown in Figure 3.17. Ampere's integral law applied to this contour for the electroqausistatic case

gives

$$\oint_C \bar{H} \cdot d\bar{s} = \oint \bar{J} \cdot d\bar{a} \tag{3.95}$$

$$H_{core} l_c + 2H_{gap} g = Ni \tag{3.96}$$

with

$$H_{core} = \frac{B_{core}}{\mu_o \mu_r} \text{ and } H_{gap} = \frac{B_{gap}}{\mu_o} \tag{3.97}$$

and l_c the total length of the integration path inside the ferrite core. If it is assumed that the typical air gap size will be much smaller than the dimensions of the core, the effect of spray fields at the air gap can be ignored. It is therefore assumed that $B_{core} = B_{gap}$. This simplification results in

$$N = \frac{B}{\mu_0 i}\left(\frac{l_c}{u_r} + 2g\right). \tag{3.98}$$

In soft ferrite data books (see for instance [62], p. 117) a parameter A_l is usually defined in order to express the inductance as

$$L = A_L N^2 \tag{3.99}$$

$$\text{with } A_L = a(g)^b \tag{3.100}$$

and where a and b are parameters dependent on the ferrite material and the core shape. If the air gap width g in equation 3.100 is replaced with the expression for g obtained from equation 3.98, a new expression for the inductance is obtained as

$$L = N^2 a \left(\frac{N\mu_0 \hat{i}}{2\hat{B}} - \frac{l_c}{2\mu_r}\right)^b \tag{3.101}$$

where $\hat{B}$ and $\hat{i}$ indicate the peak allowable flux density and maximum current in the inductor respectively. If a copper fill factor of k_{fc} is assumed for the winding area, it can be seen from Figure 3.17 that the copper area per winding will be

$$A_{wire} = \frac{(l+g)wk_{fc}}{N}. \tag{3.102}$$

By assuming the use of Litz wire and ignoring the proximity effect, the ESR for the inductor can therefore be expressed as

$$R = \rho_{cu}\frac{Nl_{wire}}{A_{wire}} = \frac{\rho_{cu} l_{wire} N^2}{k_{fc}(l+g)w}, \tag{3.103}$$

where ρ_{cu} is the resistivity of copper. For each inductance value that is considered in the optimisation process the number of turns necessary is calculated with equation 3.101 and the ESR is then calculated with equation 3.103.

To establish a relationship between the value and the ESR of the snubber capacitor,

Parameter	Symbol	Value
Collector-Emitter Voltage	v_{CES}	1200 V
Collector Current	i_C	200 A
Peak Collector Current	i_{CP}	400 A
Supply Voltage	v_{CC}	900 V
Collector Dissipation	P_C	1140 W
Collector Turn-on Time	$t_{C(on)}$	400 ns
Collector Turn-off Time	$t_{C(off)}$	600 ns

Table 3.6: Parameters for Powerex PM200DSA120 integrated IGBT module.

it is assumed in the optimisation process that the optimal snubber capacitor can be implemented with smaller capacitors in parallel. The reason for the assumption is that good-quality, high-voltage polymer capacitors are not readily available in values high enough to implement the snubber capacitors with only a single capacitor. The ESR of the snubber capacitors are therefore expressed as

$$R = \frac{k_{RC_r}}{C_r}. \tag{3.104}$$

The core losses are estimated using data sheet values at the resonant frequencies of the relevant snubber components.

The optimisation algorithm calculates the total losses over a fundamental modulation period for various values of C_r, L_b and L_r. For periods in the fundamental cycle with snubber operation the expressions derived in the previous section are used. For periods of small output current when the snubber is not operational, the turn-off switching losses in the main devices can be estimated with data sheet values. Extra losses proportional to the bus inductors, however, should be added for this hard-switching case due to the increase in turn-off losses with higher bus inductance. Every combination of snubber components is checked against the maximum voltage overshoot, maximum discharge time and peak current rating of auxiliary switches constraints to ensure that the specific combination is valid. The minimum value in the three-dimensional matrix constructed in this process is then chosen and the corresponding snubber component values are then the optimal combination.

3.7 Design of an experimental inverter

The optimisation procedure developed in the previous section will now be used to design a combined snubber for a 20 kVA single-phase inverter. After construction of this soft-switching inverter, it will be used to verify theoretical models and to investigate the effect of parasitic components and other non-idealities.

The inverter will be designed around 1200 V, 200 A main IGBTs as found in the POWEREX PM200DSA120 IPM. The basic parameters of this module are shown in Table 3.6 and the

System Parameters		
DC Bus Voltage	V_d	600 V
Peak Output Current	$I_{o(max)}$	180 A
Switching Frequency	f_s	7.5 kHz
Blanking Time	t_b	8 μs
Maximum Duty Cycle	D_{max}	0.85
Maximum Voltage Overshoot		240 V
Main IGBT Module (PM200DSA120)		
Current Fall Time	t_{fim}	250 ns
Current Tail Time	t_{tim}	500 ns
Tail Current Ratio	A_m	0.2
Voltage Fall Time	t_{fvm}	180 ns
Voltage Tail Time	t_{tvm}	180 ns
Tail Voltage Ratio	B_m	0.37
Auxiliary IGBT (1MBH60D-090A)		
Voltage Fall Time	t_{fva}	17 ns
Voltage Tail Time	t_{tva}	40 ns
Tail Voltage Ratio	B_a	0.06
On-State Resistance	R_{Sr}	17 mΩ
On-State Voltage	$V_{on(S_r)}$	1.5 V
Peak Current	$I_{r(max)}$	60 A
Auxiliary Diode (DSEI60)		
On-State Resistance	$R_{D_{Sr}}$	8.3 mΩ
On-State Voltage	$V_{on(D_{Sr})}$	1.75 V
Snubber Diode (SKR48F12)		
On-State Resistance	R_{D_r}	22 mΩ
On-State Voltage	$V_{on(D_r)}$	1.2 V
Snubber Capacitor (Acrotronics R73)		
Capacitance	C_r	5 x 33 nF
ESR Coefficient	$k_{R_{Cr}}$	16.5x10^{-12} ΩF
Bleeding Resistor		90 kΩ
Resonant Inductor (P30 3F3 Core)		
Inductance	L_r	12 μH
Copper Resistance	R_{L_r}	5.6 mΩ
Bus Inductor (P30 3F3 Core)		
Inductance	L_b	135 nH
Copper Resistance	R_{L_b}	60,4 $\mu\Omega$

Table 3.7: Parameters for the experimental inverter.

switching characteristics of the IGBTs are listed in Table 3.7. The parameters describing the turn-off behaviour were obtained from [58] and the turn-on parameters were measured after the construction of the inverter. The bus-bar structure and water-cooled heatsink used for the inverter fitted with the turn-off snubber were also used in this case. However, slight modifications were necessary to accommodate the differences in the topologies.

Before design optimisation can proceed, an initial selection of snubber components and inverter operating conditions has to be made. These choices, which can also be seen in Table 3.7 where the optimisation and inverter parameters are summarised, will now be discussed.

1. **Inverter operating conditions.** Due to the experimental nature of the topology, it is important to have large safety margins. Therefore, although 1200 V main IGBTs were used, a bus voltage of 600 V was chosen. The expected losses in the main IGBTs are also only given at $V_d = 600\,V$ in [60]. Comparisons between measured and expected losses are therefore simplified by this choice. The maximum allowable voltage overshoot was set at $0.4V_d = 240\,V$.

   The maximum output current was chosen 20 A lower than the peak IGBT current to allow for current ripple. A relatively small air-core inductor was constructed and used as a load. With a modulation frequency of 100 Hz a maximum duty cycle of 0.85 was necessary to obtain the desired output current level. The relatively low duty cycle ensures that sufficient snubber capacitor discharge time is available for a wide range of C_r and L_r values. The larger than necessary blanking time of $8\,\mu s$ was a constrain of the TMS 320C50 DSP-based controller.

2. **Auxiliary switches.** The auxiliary switches were implemented as an IGBT in series with a blocking diode. This ensures fast turn-on times and rapid turn-off under fault current conditions. The 1MBH60D-090A IGBT from Fuji, together with the DSEI60 diode from IXYS, were used. The IGBT has a voltage rating of 900 V and a continuous current rating of 60 A. The diode is a 1200 V, 52 A device. The on-state voltage and resistance of the IGBT and diode shown in Table 3.7 were derived from $v_{ce} - i_c$ graphs or directly obtained from data sheets. The parameters describing the turn-on waveforms were measured when the device was used as an auxiliary switch in the experimental turn-off snubber. A peak allowable current in the auxiliary switch was chosen as 60 A, which is a third of the maximum output current. This is considerably less than the peak current capabilities of the specific IGBT and diode.

3. **Snubber capacitors.** The R73 KP series film-foil polypropylene capacitors from Arcotronics were selected as snubbers capacitors. The choice is based on the availability, the low cost and the high peak current rating of these capacitors. At the desired voltage level the highest capacitor value obtainable was 33 nF. The snubber capacitors will therefore

be implemented with a number of these components in parallel. The maximum $\frac{dv}{dt}$ for this specific capacitor is given as 11 kV.μs^{-1}. This implies a peak current of 363 A per capacitor, which is more that sufficient to handle the maximum output current.

The dissipation factor of a capacitor is strongly dependent on the operating temperature and frequency. The resonance frequency of the bus inductors and snubber capacitors will be typically an order of magnitude higher that the resonance frequency of the snubber capacitor and the discharge inductors. Capacitor ESR estimation is therefore extremely difficult. As a worst case, the dissipation factor at 1 MHz is used. This corresponds to an ESR of approximately 500 $\mu\Omega$ and a $k_{R_{C_r}}$ of 16.5x10^{-12} ΩF.

The need for bleeding resistors, the values of which are shown in Table 3.7, will be explained in section 3.8.2.

4. **Snubber diodes.** The SEMIKRON SKR48F12 was selected as snubber diode. This 1200 V device has high peak current capabilities and showed good reverse recovery characteristics when it was used in the experimental turn-off snubber. The on-state voltage and ESR values of the diode shown in Table 3.7 were obtained directly from data sheets.

5. **Resonant discharge and bus inductors.** For both the bus and resonant discharge inductors a P30/19 ferrite core was used to minimise size and to limit stray fields. The Philips 3F3 material was used for both cases due its availability and good performance factor at high frequencies ([61], p. 39). To prevent saturation, a peak flux density $\hat{B}$ of 300 mT was allowed in the core. A relatively low copper fill factor of 0.3 was assumed. This makes provision for sufficient voltage isolation between the closely spaced windings of the inductors. For this core shape, specific ferrite material and copper fill factor equations 3.98, 3.101 and 3.103 can be rewritten as

$$g = \left(\frac{2\,\mathrm{x}\,10^{-6}\pi N\hat{i}}{3} - 11,3\,\mathrm{x}\,10^{-6}\right) \tag{3.105}$$

$$L = 0.368\,\mathrm{x}\,10^{-9}N^2g^{-0.898} \tag{3.106}$$

$$R = \frac{7\,\mathrm{x}\,10^{-7}N^2}{(11\,\mathrm{x}\,10^{-3}+g)}. \tag{3.107}$$

During optimisation the estimates of core losses, as a function of snubber component value, were also taken into account. To facilitate the large frequency range found during the optimisation process, the loss estimates were based on extrapolation of data sheet values.

In Figure 3.18 the selected snubber components and main IGBT module are shown. The optimisation procedure developed in the previous section makes provision for at least three parameters that can be varied to determine the optimal snubber components. They are C_r, L_b

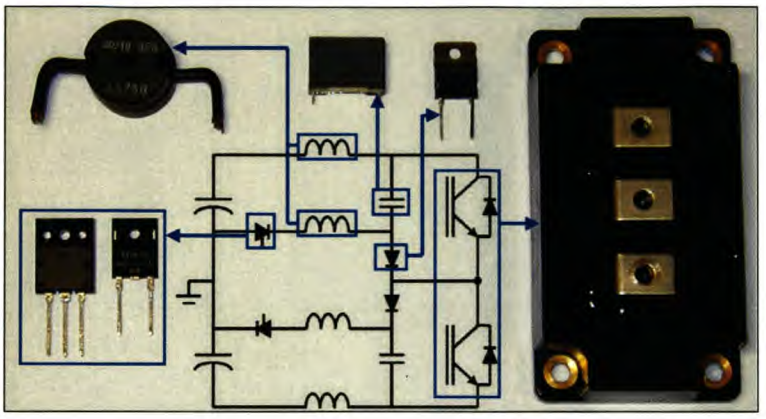


Figure 3.18: Main IGBT and snubber components used in the experimental combined snubber inverter.

and L_r. Such a three-dimensional optimisation procedure suggest that the lowest losses in the experimental inverter will occur at a very large value of L_r (approximately $18\,\mu H$). However, due to thermal constrains, this value cannot be implemented with the selected core. The highest practical inductance value achievable with the P30 core, at the specific current requirements, is about $12\,\mu H$. L_r was therefore chosen equal to this value and the optimisation process repeated with only L_b and C_r as parameters.

The results of the optimisation procedure are shown in Figure 3.19. Main IGBT turn-off losses, main IGBT turn-on losses and the losses in the snubber components are shown in Figure 3.19a, b and c respectively. The combination of total switching losses in the main IGBTs and total losses in the snubber components are shown in Figure 3.19d. As seen in Figure 3.19a, variation of C_r directly influences the turn-off losses, while variation of L_b in Figure 3.19b has a major influence on the turn-on losses. In Figure 3.19d the flat dark blue areas correspond to combinations that result in excessive voltage overshoot, auxiliary switch current or snubber capacitor discharge time. The optimal snubber component values are $L_b = 135\,nH$ and $C_r = 150\,nF$. The total predicted losses with these component values are only about 1% higher that the lowest losses predicted when the three-dimensional optimisation process was used. In Table 3.8 a summary of the losses in the different components is given.

The snubber capacitor was implemented as five 33 nF capacitors in parallel, resulting in a total capacitance of 165 nF. For the bus inductors equations 3.105-3.107 give values of N = 1, g = 0.58 mm and $R_{L_b} = 60,4\,\mu\Omega$. For the resonant discharge inductors these parameters are N = 10, g = 1.5 mm and $R_{L_r} = 5,6\,\mathrm{m}\Omega$.

In Figures 3.20 and 3.21 the constructed snubber is shown. The snubber components were divided into two groups and placed on two separate PCBs. In Figure 3.20 the top snubber board, containing the auxiliary switches, the drivers with their isolated power supplies and

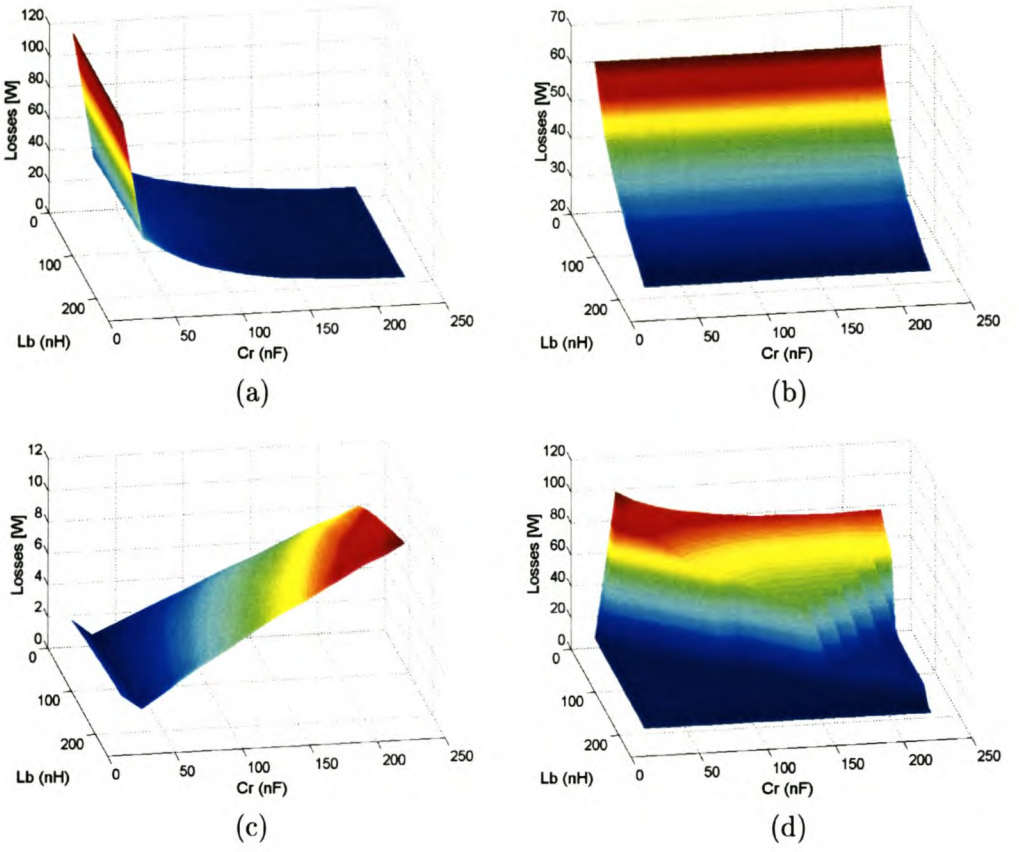


Figure 3.19: Optimisation results for experimental inverter ($L_r = 12\,\mu H$): (a) Main IGBT turn-off losses; (b) Main IGBT turn-on losses; (c) Losses in auxiliary switches and passive snubber components; (d) Total losses.

Total Main IGBT Turn-on Loss	34 W
Total Main IGBT Turn-off Loss	14 W
Snubber Diode Loss	3.2 W
Snubber Capacitor Loss	13 mW
Resonant Inductor Loss	240 mW
Auxiliary Switch Loss	2.2 W
Auxiliary Diode Loss	2.2 W
Bus Inductor Loss	1.2 W

Table 3.8: Summary of theoretical losses in the experimental inverter over a fundamental modulation cycle.

the auxiliary switch control circuitry, is shown. Two versions were constructed. In Figure 3.20a the first version is shown with basic logic gates for controlling the auxiliary switches. Only discontinuous snubber operation was achievable with this version. In Figure 3.20b the second version is shown with an Altera EPLD as controller. This device provides programming

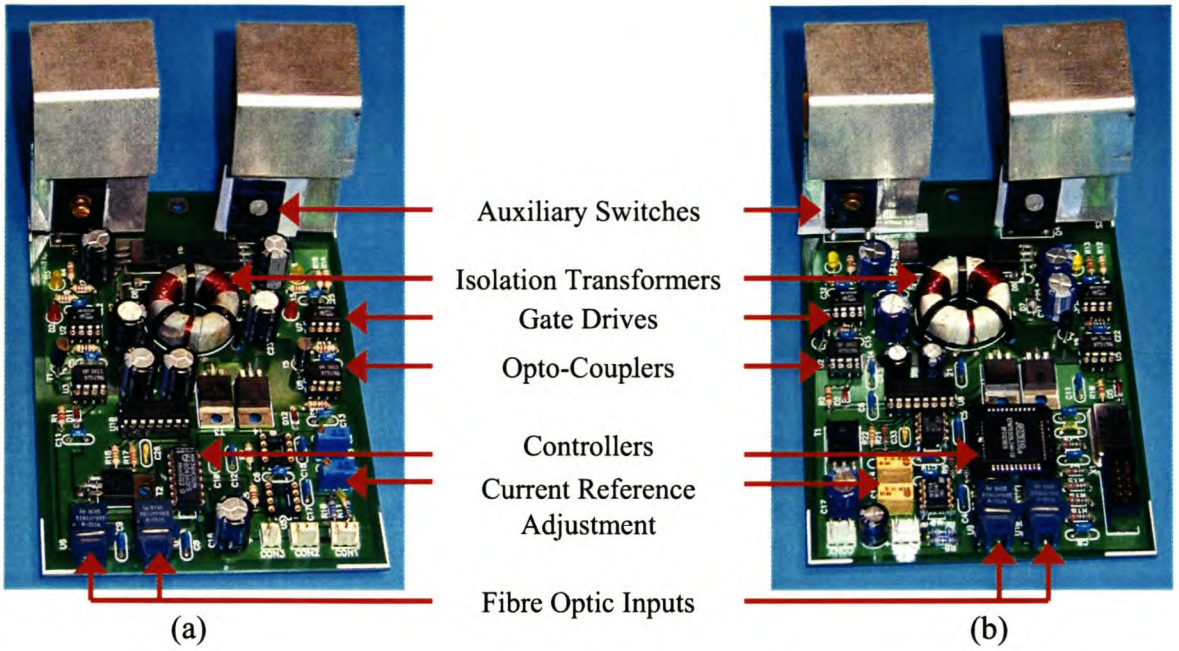


Figure 3.20: Constructed top snubber PCBs: (a) First version; (b) Second version.

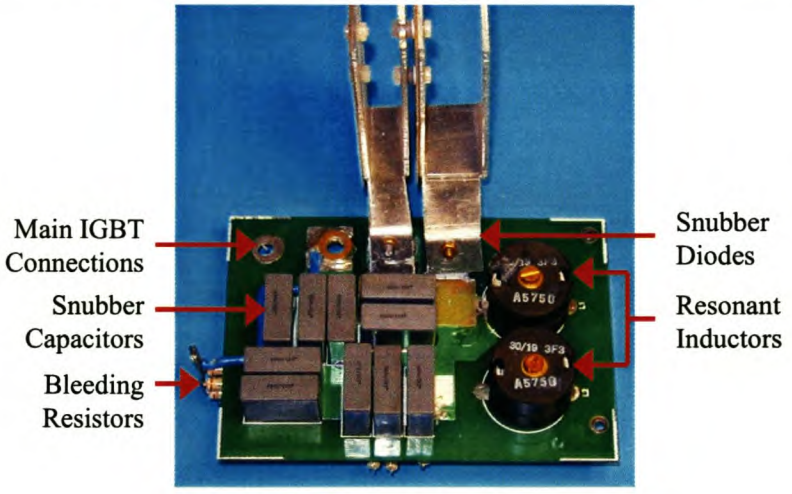


Figure 3.21: Constructed bottom snubber PCB.

versatility that allow for more options in auxiliary switch control. In Figure 3.21 the bottom snubber board with the snubber capacitors, snubber diodes and resonant inductors is shown.

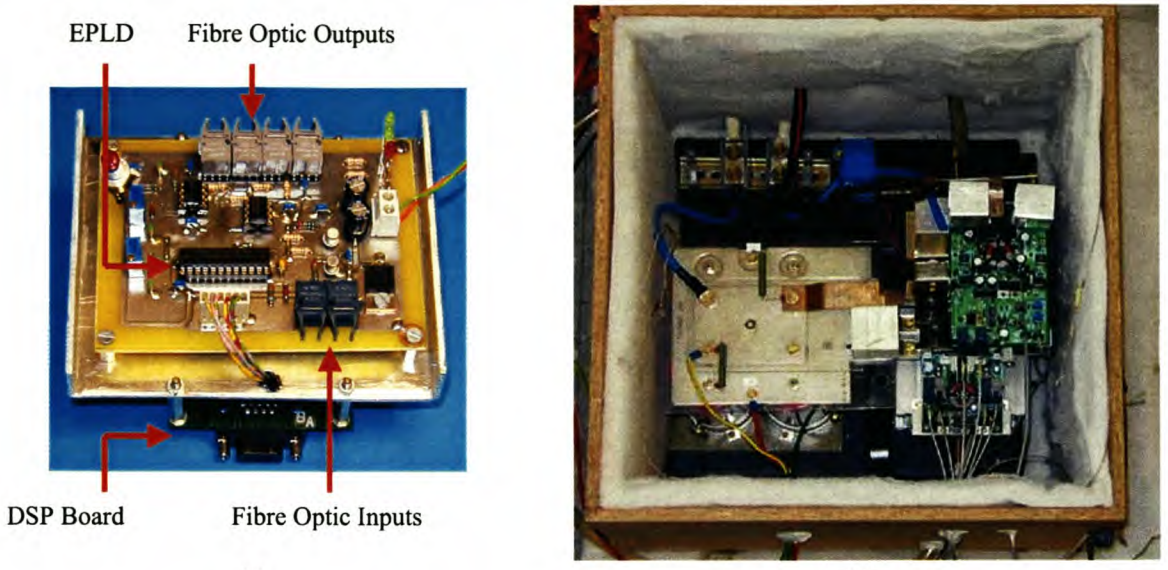


Figure 3.22: (a) DSP-based controller with EPLD protection interface and (b) experimental inverter inside wooden container.

3.8 Experimental results

In this section waveforms obtained from the experimental inverter will be compared to theoretical models. Three different cycles, namely main IGBT turn-off, main IGBT turn-on and snubber capacitor discharge will be discussed. Efficiency measurements will also be compared to results obtained from the optimisation procedure. All the experimental results were obtained with a large inductive load and normal open-loop PWM operation.

In Figure 3.22a the TMS 320C50 DSP-based PWM controller is shown. This processor was used to generate the appropriate PWM signals that were then sent, via fibre optic link, to the main IGBTs and auxiliary switch controllers. An additional EPLD stage is also used for fast error signal processing. The complete experimental inverter is shown in Figure 3.22b. A wooden container, to facilitate calorimetric loss measurement, was again used.

3.8.1 Main IGBT turn-off cycle

In this section measured waveforms obtained from the experimental inverter at the turn-off instant of a current carrying main IGBT will be discussed and compared to predictions by theoretical models. To obtain accurate waveform predictions it is essential to use theoretical models that include secondary effects like parasitic components and diode reverse recovery. An analysis of the snubber circuit at turn-off, taking these effects into account, will therefore firstly

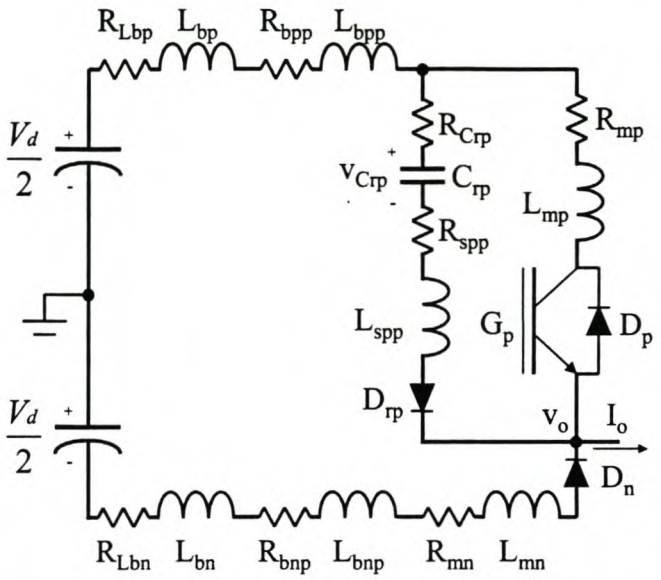


Figure 3.23: Complete snubber circuit as used in the detailed analysis of the main IGBT turn-off cycle.

be performed. In this detailed analysis tail-forming switching behaviour for the main IGBTs, as described in equation 3.17, is again assumed.

Figure 3.23 shows the complete snubber circuit that comes into play at the main IGBT turn-off cycle (large positive output current is assumed). The following parasitic components are included:

1. The parasitic inductance L_{bpp} and resistance R_{bpp} of the positive rail bus-bar.
2. The parasitic inductance L_{bnp} and resistance R_{bnp} of the negative rail bus-bar.
3. The parasitic inductance L_{mp} and resistance R_{mp} between the pole and positive rail connections of the main IGBT module.
4. The parasitic inductance L_{mn} and resistance R_{mn} between the pole and negative rail connections of the main IGBT module.
5. The parasitic inductance L_{spp} and resistance R_{spp} of the turn-off snubber loop.
6. The ESR of the bus inductors (R_{Lbp} and R_{Lbn}) and the snubber capacitor R_{Crp}.
7. The ESR of diode D_n and D_{rp} (R_{Dn} and R_{Drp}) are not shown in Figure 3.23. They are, however, also taken into account during certain periods of operation. In Figure 3.25 the diode model during different stages is illustrated.

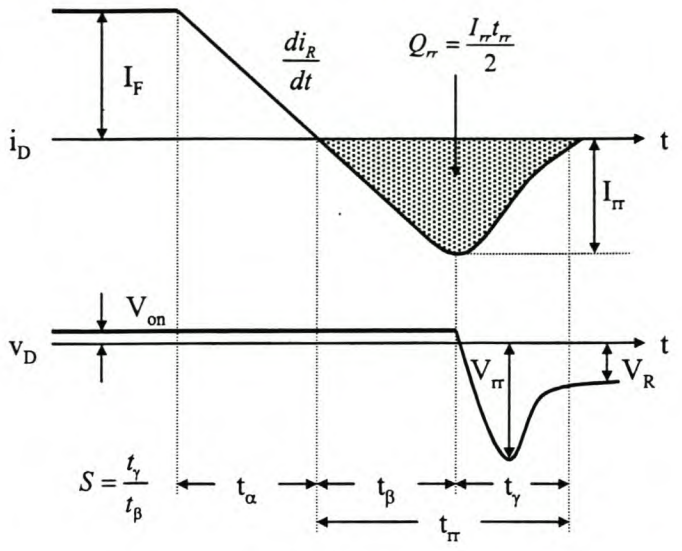


Figure 3.24: Typical reverse recovery behaviour of a power diode.

To simplify the analysis of the circuit, parasitic components are combined as follows:

$$\begin{aligned} L_p &= L_{bpp} + L_{bp} \\ L_n &= L_{bnp} + L_{bn} \\ R_p &= R_{Lbp} + R_{bpp} \\ R_n &= R_{Lbn} + R_{bnp} \\ R_s &= R_{Crp} + R_{Drp} + R_{spp}. \end{aligned}$$

It is also further assumed that the parasitic components of the positive and negative rail busbars are equal. This assumption leads to the following definitions:

$$R_b = R_p = R_n \tag{3.108}$$

$$L_b = L_p = L_n. \tag{3.109}$$

The reverse recovery behaviour of diode D_{rp} is also included in the analysis of the snubber circuit, but the forward recovery of D_n is neglected. Typical reverse recovery behaviour of a power diode is shown in Figure 3.24 [56]. Initially the diode carries a forward current of I_F and there is a on-state voltage drop V_{on} across it. At turn-off the current starts to decrease at a rate determined by the external circuitry. The time it takes to reach zero current is shown in Figure 3.24 as t_α. In period t_β the voltage across the device remains essentially the same as the current in the device becomes negative. This reverse current will continue to grow for as long as it takes for the excess carriers to be swept out. At the end of this interval the reverse recovery current will reach its peak value of I_{rr}. During the last stage of turn-off the current will decrease to zero and after a large initial reverse voltage overshoot of V_{rr}, the reverse blocking

voltage V_R will be reached. In power diode data sheets the reverse recovery time ($t_{rr} = t_\beta + t_\gamma$) and I_{rr} are commonly given as function of $\frac{di_R}{dt}$.

From Figure 3.24 it is clear that the reverse recovery behaviour of a diode can be accurately described by $\frac{di_R}{dt}$, t_{rr} and I_{rr} if $\frac{di_R}{dt}$ is constant. These parameters are, however, not sufficient to describe the reverse recovery of D_{rp}, because $\frac{di_R}{dt}$ is not constant for this diode. Although for most of the cases the current in D_{rp} during interval t_α and t_β can be reasonably well approximated with linear curves, different parameters were used to model the reverse recovery. These parameters are the total recovery charge Q_{rr} and the so called "snappiness" S of the diode. The reverse recovery model that is used in the analysis can be summarised as follows:

1. The diode is modeled as an on-state voltage $V_{Drp(on)}$ and ESR R_{Drp} during forward current conduction and intervals t_α and t_β.

2. At the end of period t_α the value of $\frac{di_R}{dt}$ is determined. From the data sheets of the power diode estimates of I_{rr} and t_{rr} for this specific $\frac{di_R}{dt}$ are obtained.

3. The total reverse recovery charge Q_{rr}, S and the charge that should be depleted during interval t_β are then calculated with the following expressions:

$$Q_{rr} = \frac{I_{rr} t_{rr}}{2} \tag{3.110}$$

$$S = \left(\frac{t_{rr}}{I_{rr}}\right) \frac{di_R}{dt} - 1 \tag{3.111}$$

$$Q_{t_\beta} = \frac{Q_{rr}}{S+1}. \tag{3.112}$$

4. The charge depletion is integrated from the beginning of interval t_β and compared to Q_{t_β}. Interval t_γ starts when this charge quantity is reached. At the end of interval t_β the true value of I_{rr} can also be obtained.

5. The diode current during the last interval t_γ is not determined by external circuitry as in the previous intervals, but modeled as a linear current source. A diode output capacitance C_{Drp}, in parallel with the current source i_{drr}, is also included in the model during this interval. In Figure 3.25 the diode model during different intervals is summarised. The duration of the last interval can be calculated from the knowledge of the duration of interval t_β and S. The true value of t_{rr} can now also be calculated.

For the detailed analysis the turn-off process will be divided into three stages. These stages will now be treated separately. Time is defined as $t = 0$ at the start of the t_{fim} phase in $i_{c(G_p)}$. The definitions of time instances shown in Table 3.2 are still valid.

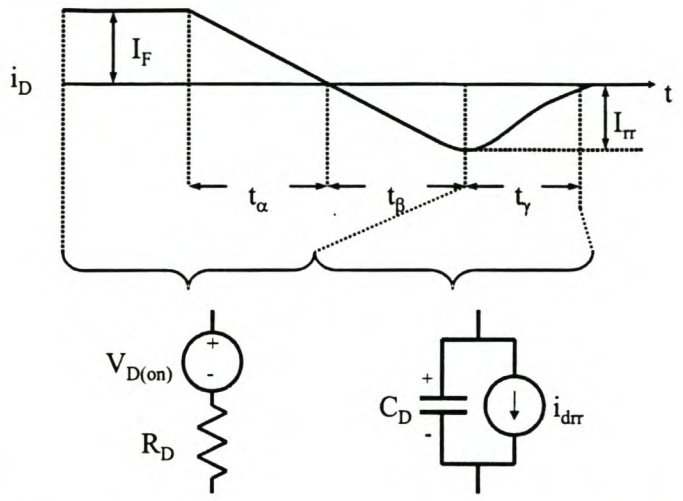


Figure 3.25: Diode model used for detailed analysis.

Stage 1: $0 \leq t < t_{vr}$

At t_{vr} v_o reaches $-\frac{V_d}{2}$ and D_n turns on. As in section 3.5.1, it is assumed that $t_1 \leq t_{vr} < t_b$. This implies that the collector current of G_p can be in any of its three phases during this stage (see Figure 3.10 and equation 3.17). The expressions for the pole and the ideal snubber capacitor voltages (as defined in Figure 3.23) during these phases are:

$0 \leq t < t_1$ $(t_1 = t_{fim})$

$$v_{Crp(a)} = \frac{I_o\,(1 - A_m)\,t^2}{2C_r t_{fim}} \tag{3.113}$$

$$v_{o(a)} = \frac{V_d}{2} - I_o R_b - V_{Drp(on)} - \left(\frac{I_o\,(1 - A_m)}{t_{fim}}\right)\left(L_{rpp} + R_s t + \frac{t^2}{2C_r}\right) \tag{3.114}$$

$t_1 \leq t < t_2$ $(t_2 = t_{fim} + t_{tim})$

$$\begin{aligned} v_{Crp(b)} &= v_{Crp(a)}(t_1) + \frac{I_o\,(t - t_{fim})}{C_r}\left(1 - A_m\left(1 + \frac{t_{fim}}{t_{tim}}\right)\right) \\ &\quad + \frac{I_o A_m\left(t^2 - t_{fim}^2\right)}{2C_r t_{tim}} \end{aligned} \tag{3.115}$$

$$\begin{aligned} v_{o(b)} &= \frac{V_d}{2} - I_o R_b - V_{Drp(on)} - I_o R_s\left(1 - A_m\left(1 - \frac{t - t_{fim}}{t_{tim}}\right)\right) \\ &\quad - \frac{I_o A_m L_{rpp}}{t_{tim}} - v_{Crp(b)}(t) \end{aligned} \tag{3.116}$$

$t_2 \leq t$

$$v_{Crp(c)} = v_{Crp(b)}(t_2) + \frac{I_o\,(t - t_2)}{C_r} \tag{3.117}$$

$$v_{o(c)} = \frac{V_d}{2} - I_o\,(R_b + R_s) - V_{Drp(on)} - v_{Crp(c)}(t). \tag{3.118}$$

Stage 2: $t_{vr} \leq t < t_{cz} + t_\beta$

After time instance t_{vr} diode D_n becomes forward biased and a period of resonance starts in the snubber circuit. At t_{cz} the snubber capacitor current reaches zero and after the reverse recovery of D_{rp} resonance stops. During this period the circuit can be described by

$$\frac{d^2 i_{bp}}{dt^2} + \left(\frac{\alpha}{\beta}\right)\frac{di_{bp}}{dt} + \left(\frac{1}{C_r\beta}\right) i_{bp} = \left(\frac{L_{rpp}}{\beta}\right)\frac{d^2 i_{c(G_p)}}{dt^2} + \left(\frac{R_s}{\beta}\right)\frac{di_{c(G_p)}}{dt} + \left(\frac{1}{C_r\beta}\right) i_{c(G_p)} \tag{3.119}$$

with

$$\alpha = 2R_b + R_s + R_{mn} + R_{Dn} \tag{3.120}$$

$$\beta = 2L_b + L_{rpp} + L_{mn}. \tag{3.121}$$

The solution of i_{bp} can be expressed as

$$i_{bp} = c_1 e^{m_1 t} + c_2 e^{m_2 t} + At + B \tag{3.122}$$

with

$$m_1, m_2 = -\frac{\alpha}{2\beta} \pm \sqrt{\left(\frac{\alpha}{2\beta}\right)^2 - \frac{1}{C_r\beta}}. \tag{3.123}$$

The constants c_1, c_2, A and B are dependent on the initial conditions and the status of the collector current in G_p. The expressions for these constants during the different phases in collector current are:

$t_1 \leq t < t_2$

$$A = \frac{-A_m I_o}{t_{tim}} \tag{3.124}$$

$$B = \frac{I_o A_m \left(t_2 + C_r \left(2R_b + R_{mn} + R_{Dn}\right)\right)}{t_{tim}} \tag{3.125}$$

$t_2 \leq t$

$$A = B = 0 \tag{3.126}$$

The expressions for c_1 and c_2 for both phases are

$$c_1 = \frac{i'_{bp}(t_i) + m_2\left(t_i A + B - i_{bp}(t_i)\right) - A}{\left(m_1 - m_2\right) e^{m_1 t_i}} \tag{3.127}$$

$$c_2 = \frac{i'_{bp}(t_i) + m_1\left(t_i A + B - i_{bp}(t_i)\right) - A}{\left(m_2 - m_1\right) e^{m_2 t_i}} \tag{3.128}$$

were t_i denotes the initial time. The pole voltage v_o during stage 2 can be expressed as

$$v_o = -\frac{V_d}{2} + (i_{bp} - I_o)(R_b + R_{mn} + R_{Dn}) + \frac{di_{bp}}{dt}(L_b + L_{mn}) - V_{Dn(on)}. \quad (3.129)$$

Stage 3: $t_{cz} + t_\beta \leq t < t_{cz} + t_{rr}$

During stage 3 diode D_{rp} is modeled as a linear current source i_{drr} in parallel with a parasitic output capacitance C_{Drp} (see Figure 3.25). R_s is also redefined during stage 3 as $R_s = R_{Crp} + R_{spp}$. The differential equation that describes the circuit is

$$\frac{d^2 i_{bp}}{dt^2} + \left(\frac{\alpha}{\beta}\right)\frac{di_{bp}}{dt} + \left(\frac{C_r + C_{Drp}}{\beta C_r C_{Drp}}\right) i_{bp} = \left(\frac{L_{rpp}}{\beta}\right)\frac{d^2 i_{c(G_p)}}{dt^2} + \left(\frac{R_s}{\beta}\right)\frac{di_{c(G_p)}}{dt} + \left(\frac{C_r + C_{Drp}}{\beta C_r C_{Drp}}\right) i_{c(G_p)} + \frac{i_{drr}}{\beta C_{Drp}}. \quad (3.130)$$

The general solution to this equation is

$$i_{bp} = c_3 e^{m_3 t} + c_4 e^{m_4 t} + Ct + D \quad (3.131)$$

with

$$m_3, m_4 = -\frac{\alpha}{2\beta} \pm \sqrt{\left(\frac{\alpha}{2\beta}\right)^2 - \left(\frac{C_r + C_{Drp}}{\beta C_r C_{Drp}}\right)} \quad (3.132)$$

and the other constants again dependent on the initial conditions and the status of the collector current in G_p. The expressions for C and D during the different phases in collector current are:

$t_1 \leq t < t_2$

$$C = \frac{I_{rr} C_r (1 + S)}{S t_{rr} (C_r + C_{Drp})} - \frac{A_m I_o}{t_{tim}} \quad (3.133)$$

$$D = \frac{C_r C_{Drp} (\gamma - \alpha C)}{(C_r + C_{Drp})} \quad (3.134)$$

with

$$\gamma = \frac{A_m I_o (C_r + C_{Drp})\left(1 + \frac{t_{fim}}{t_{tim}}\right)}{C_r C_{Drp}} - \frac{R_s I_o A_m}{t_{tim}} - \frac{I_{rr}\left(1 + \frac{(1+S)t_{br}}{S t_{rr}}\right)}{C_{Drp}} \quad (3.135)$$

$$t_{br} = t_{cz} + t_\beta \quad (3.136)$$

$t_2 \leq t$

$$C = \frac{I_{rr} C_r (1 + S)}{S t_{rr} (C_r + C_{Drp})} \quad (3.137)$$

$$D = \frac{C_r C_{Drp} (\gamma - \alpha C)}{(C_r + C_{Drp})} \quad (3.138)$$

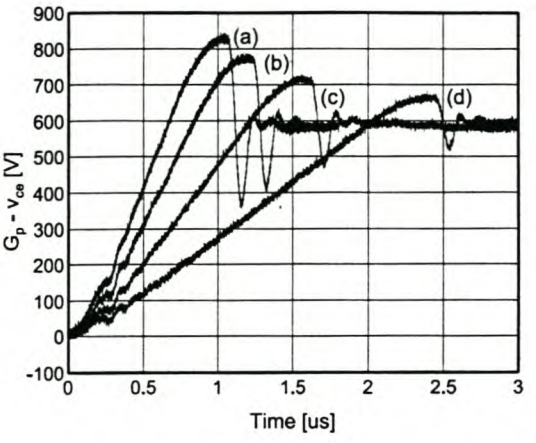


Figure 3.26: Measured waveforms during turn-off: (a) $I_o = 180$ A; (b) $I_o = 135$ A; (c) $I_o = 90$ A; (d) $I_o = 45$ A.

with

$$\gamma = -\frac{I_{rr}\left(1 + \frac{t_{br}(1+S)}{St_{rr}}\right)}{C_{Drp}}. \tag{3.139}$$

The expressions for c_3 and c_4, for both phases, are

$$c_3 = \frac{i'_{bp}(t_i) + m_4\left(t_i C + D - i_{bp}(t_i)\right) - C}{\left(m_3 - m_4\right)e^{m_3 t_i}} \tag{3.140}$$

$$c_4 = \frac{i'_{bp}(t_i) + m_3\left(t_i C + D - i_{bp}(t_i)\right) - C}{\left(m_4 - m_3\right)e^{m_4 t_i}}. \tag{3.141}$$

The pole voltage during stage 3 is also described by equation 3.129.

In Figure 3.26 measured v_{ce} waveforms for G_p during turn-off are shown. Traces a, b, c and d correspond to output current levels of 180, 135, 90 and 45 A respectively. The dependence of the voltage rise time, the maximum voltage overshoot and the reverse recovery behaviour of D_{rp} on the magnitude of the output current is well illustrated. It can be seen that the maximum voltage overshoot at 180 A is marginally lower than the 240 V that was allowed for in design of the experimental inverter (see Table 3.7).

Figure 3.27 shows the comparison between the model that was used for loss calculations (model 1) and the complete model that was developed in this section (model 2). A list of parasitic component values is given in Table 3.9. In Figure 3.27a the collector current model and the predicted turn-off v_{ce} waveforms for G_p at $I_o = 90\,A$ are shown. In Figure 3.27b the output current is $I_o = 180\,A$. There are two areas where the predicted waveforms are substantially different. The first major difference occurs during the current fall time of i_c where model 2 predicts a higher value for v_{ce} than model 1. This can be mainly attributed to the voltage drop across L_{spp} due to the rapid increase of snubber capacitor current during this

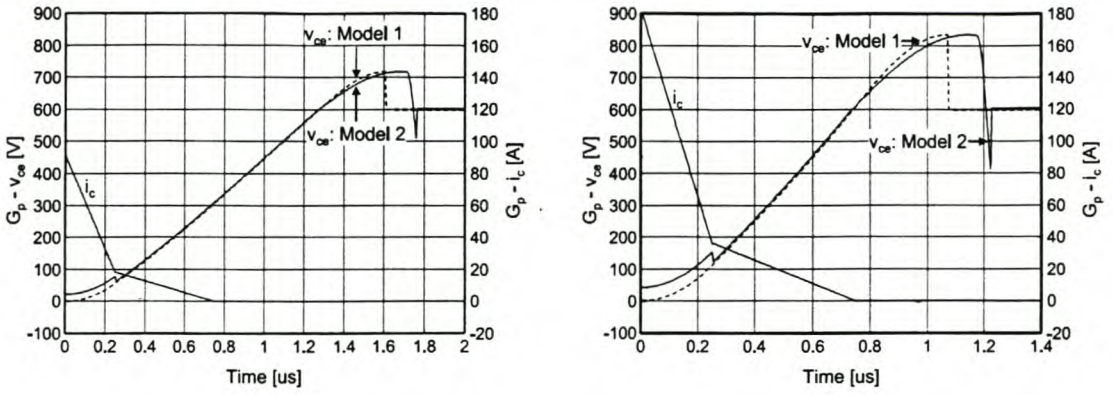


Figure 3.27: Comparison of theoretical models during main IGBT turn-off.

period. The rate of snubber capacitor current increase during the tail time of i_c is much lower and the small effect on v_{ce} cannot clearly be seen in Figure 3.27. The second area where the two models differ considerably is during the resonance cycles ($t > 1.3\,\mu s$ for $I_o = 90\,A$ and $t > 0.7\,\mu s$ for $I_o = 180\,A$). The effect of damping and the reverse recovery of D_{rp} are clearly visible in the predicted waveform of model 2. The result is a longer resonance period compared to the prediction by model 1 and a negative voltage overshoot when D_{rp} snaps off.

The effects of parasitic components and diode reverse recovery, as illustrated by model 2, suggest that the losses calculated using model 1 are lower than what can be expected in a practical system. The increased v_{ce} of G_p during the current fall time is of particular importance, because of the high collector current during that time. The effects of parasitic resistance and diode reverse recovery during the resonance cycle does not come into play with the current experimental inverter. Even with the lowest voltage rise time that occur at the maximum output current of 180 A, the collector current is already zero before the resonant cycle starts.

Waveforms measured during the turn-off of G_p are compared to model 2 in Figure 3.28. The collector current model and the predicted and measured v_{ce} waveforms are shown for output currents of 45, 90, 135 and 180 A. The correlation between measured waveforms and theoretical predictions are generally good, except for two periods where noticeable differences occur.

The first period where major differences can be seen is again during the collector current fall time. This can be attributed to inaccuracies in the collector current model. The collector current waveform was, however, not measured to improve the model, because of the difficulty in obtaining accurate, high bandwidth current measurements without affecting the layout and parasitics of the circuit dramatically.

The second period where major differences occur is during the reverse recovery of diode D_{rp}. The resonance cycle in the practical system is shorter than predicted by the model and

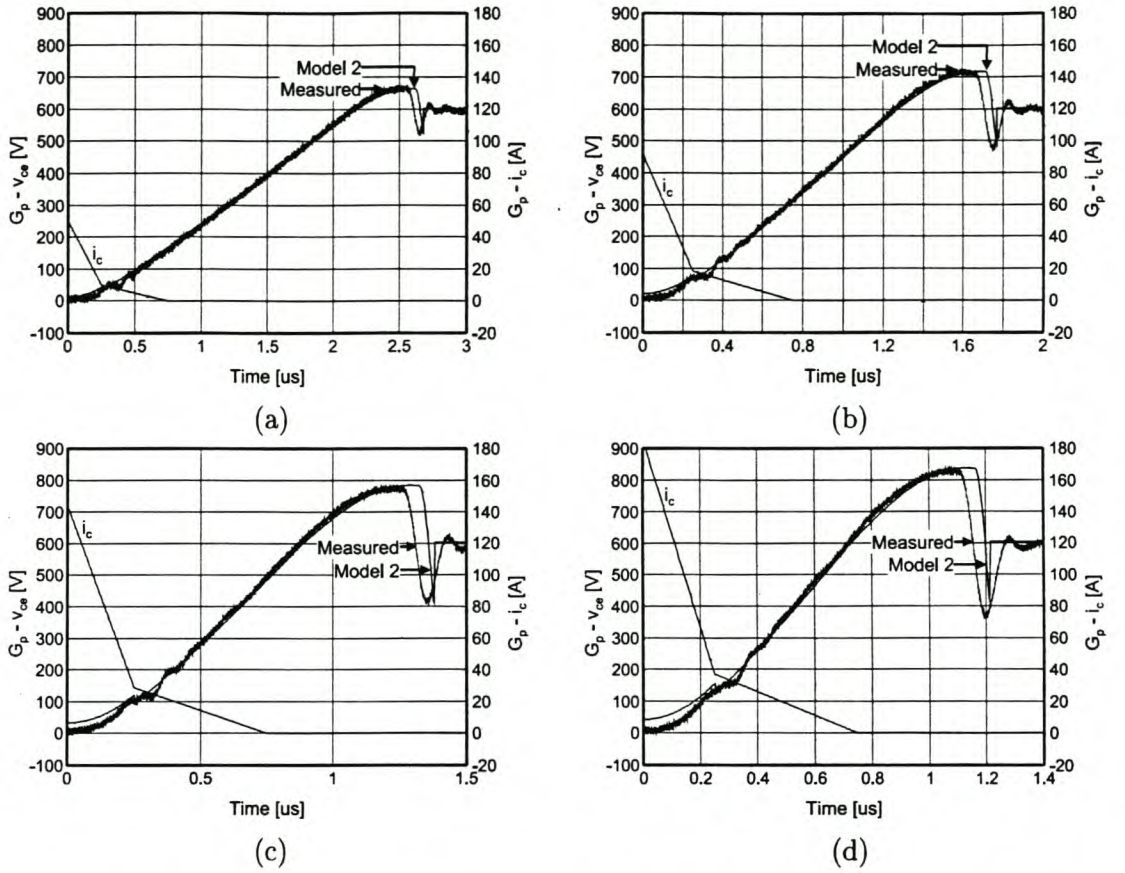


Figure 3.28: Comparisons between predicted and measured waveforms at main IGBT turn-off: (a) $I_o = 45\,A$; (b) $I_o = 90\,A$; (c) $I_o = 135\,A$; (d) $I_o = 180\,A$.

the reverse recovery spike is smoother and damped. The discontinuous nature of the reverse recovery spike predicted by model 2 can be attributed to the linear current source model used during period t_γ of the reverse recovery cycle. To obtain a better prediction a more accurate current model can be used during this period. Extensive data on the reverse recovery behaviour of power diodes, during soft-switching applications, are also not readily provided by manufacturers and only approximate values can be obtained.

In section 3.3.1 the high peak current and high voltage overshoot problem associated with the continuous operation strategy were discussed. Under the ideal circuit assumption of section 3.2 a maximum voltage overshoot of 600 V was predicted for the experimental inverter at $I_o = 0\,A$, if the continuous operation strategy was used. It was, however, mentioned that the severity of the problem might decrease in a practical converter due to parasitic resistance, stray inductance and non-ideal switching behaviour. In Figure 3.29 measured and predicted voltages across C_{rp} are shown for two cases where the output current is not large enough to charge the snubber capacitors within the blanking time and a continuous snubber operation strategy is

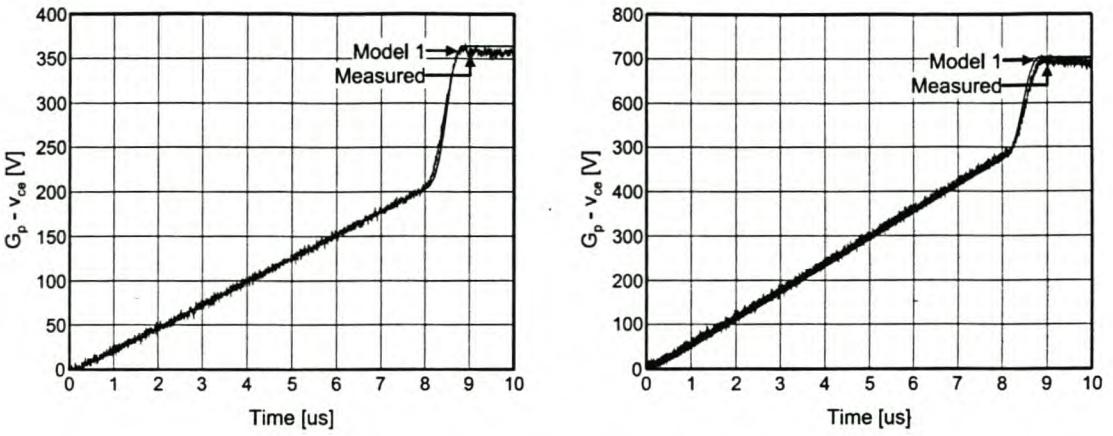


Figure 3.29: Comparisons of predicted and measured waveforms at low output current under continuous snubber control: (a) $V_d = 300\,V$, $I_o = 4\,A$; (b) $V_d = 600\,V$, $I_o = 10\,A$.

used. In Figure 3.29a $V_d = 300\,V$, $I_o = 4\,A$ and $V_d = 600\,V$, $I_o = 10\,A$ in Figure 3.29b. Model 1 was used to obtain the predicted waveforms. There are good correlations between the predicted and measured waveforms, even though parasitic components are not included in this model. This suggests that the maximum voltage overshoot in the experimental inverter will be close to the value predicted by model 1 of 520 V.

In section 3.3.4 the possibility of using an uni-directional charge assistance operation strategy for the combined snubber was discussed. Due to the complexity of the active circuit during such a charge assistance cycle, a general analysis to prove the concept was not done. Basic circuit simulations were, however, performed and the strategy was tested experimentally. The experimental results obtained are shown in Figure 3.30. The snubber capacitor voltage v_{Crp}, the resonant inductor current i_{rp} and the collector-emitter voltage v_{ce} of IGBT G_p are shown in Figure 3.30a, c and e. The time period shown in these graphs is the blanking time that occurs just after G_n is switched off. In Figure 3.30b, d and f the snubber capacitor voltage v_{Crp} and the collector-emitter voltage v_{ce} of G_p are shown during the blanking time that occurs just after G_p is switched off. The waveforms are shown for $I_o \approx 0\,A$ in Figure 3.30a and b, $I_o \approx 18\,A$ in Figure 3.30c and d and $I_o \approx -18\,A$ in Figure 3.30e and f. For the experimental inverter the boundary for unidirectional charge assistance was set at $I_o = 18\,A$; therefore the best and the worst cases are covered in Figure 3.30.

At negligible output current the discharging (Figure 3.30a) and charging (Figure 3.30b) of C_{rp} are effective. In Figure 3.30b v_{ce} drifts slightly after C_{rp} has reached V_d. This is due to a very small negative output current. As a result of propagation delays in the control and internal circuitry of the IPM, the response of the auxiliary switches to control signals are about a microsecond faster that of the main IGBTs. The effect of this can be clearly seen in Figure

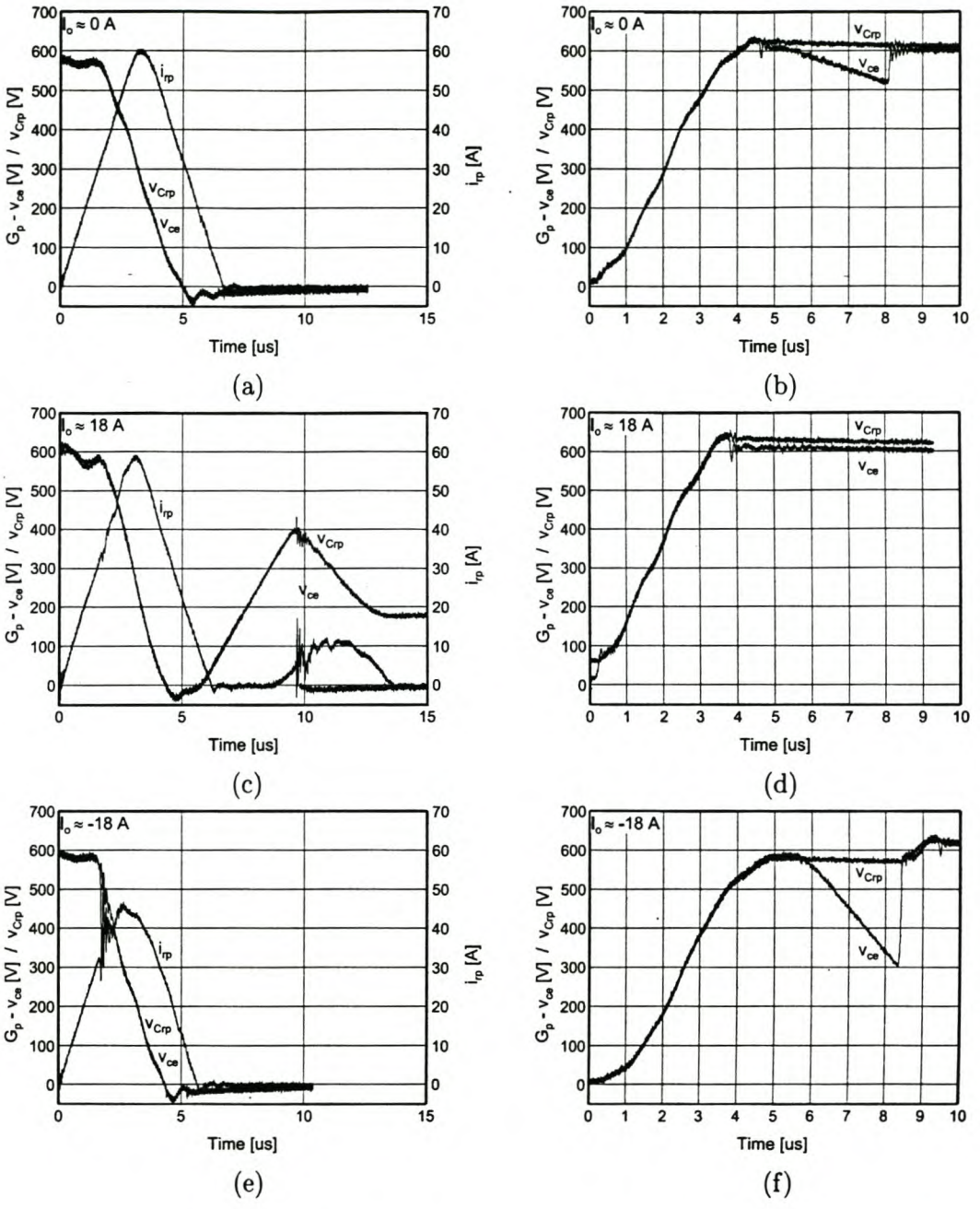


Figure 3.30: Experimental results obtained with uni-directional charge assistance.

3.30a, c and e. For instance, in Figure 3.30a it is expected that the discharge of C_{rp} should start immediately when the current in L_{rp} grows. The snubber capacitor voltage is, however, clamped to the bus voltage for just over a microsecond. Only after switch G_n switches off, the capacitor starts to discharge. The mismatch in the propagation delays of the main and auxiliary switches therefore causes a boost period in i_{rp}. This boost in inductor current will

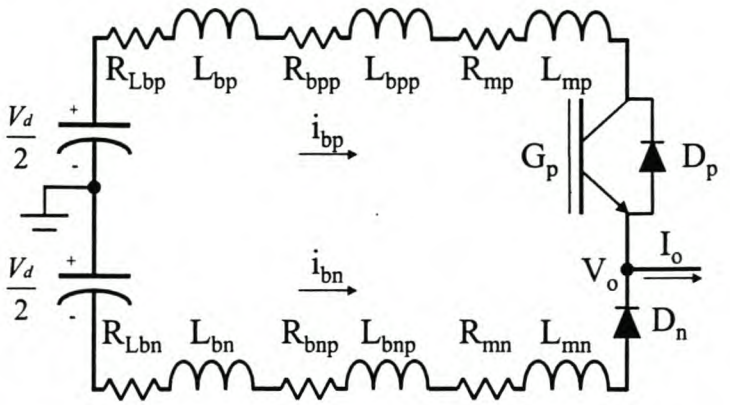


Figure 3.31: Complete snubber circuit as used in detailed analysis of the main IGBT turn-on cycle.

help to ensure complete pole voltage transitions under a wider output current range.

In Figure 3.30c the inductor current boost stage can again be seen. The boost current ensures that C_{rp} are completely discharged at $5\,\mu s$, even though $I_o = 18\,A$ is the worst case for the discharge of C_{rp}. Ideally G_p should be switched on at this time instant when the voltage across it is zero. If a voltage monitoring system and the ability to dynamically adjust the blanking time is not implemented, the capacitor will start to charge again as soon as i_{rp} drops below 18 A. The voltage across the capacitor will continue to grow until switch G_p is switched on. In Figure 3.30c this growth in v_{Crp} can clearly be seen. At around $9\,\mu s$ v_{Crp} is even high enough to start a second resonant cycle with L_{rp}, as seen in the i_{rp} waveform. After G_p is switched on the resonance continue and v_{Crp} has a final value of about 180 V. Although this non-zero value is not detrimental to the system, the effectiveness of the snubber during the next turn-off cycle is reduced. As can be expected, no problems are encountered to charge C_{rp} again after G_n is switched off, as indicated by Figure 3.30d. The non-zero value of v_{Crp} and the resulting rapid increase in v_{ce} at the start of the cycle can also be seen in this graph.

The effective discharging of C_{rp} at $I_o = -18\,A$ is shown in Figure 3.30e and the charging of C_{rp} at $I_o = -18\,A$ is shown in Figure 3.30f. It can be seen that C_{rp} is not fully charged during the resonant cycle. It has an value of approximately 580 V before v_{ce} start to drift back again at around $6\,\mu s$. When G_p is switched on, C_{rp} is forced to charge completely. This will lead to slightly more turn-on losses in G_p.

3.8.2 Main IGBT turn-on cycle

In this section measured waveforms obtained from the experimental inverter at the turn-on instant of a main IGBT will be discussed and compared to predictions by theoretical models. An analysis of the snubber circuit at turn-on, taking the parasitic components and the reverse recovery behaviour of the free-wheeling diode into account, will also be performed.

Figure 3.31 shows the complete snubber circuit that comes into play at main IGBT turn-on (large positive output current is assumed). In the analysis tail-forming switching behaviour for G_p at turn-on is again assumed. This model was described in equation 3.60. After G_p is completely on, the device is modeled with an on-state voltage $V_{G_p(on)}$ and an ESR R_{G_p}. The model used for D_n is the same as described in the previous section (see Figure 3.25) with on-state voltage $V_{D_n(on)}$, ESR R_{D_n} and parasitic output capacitance C_{Dn}. All parasitic components that are included in the circuit were described in the previous section. However, new definitions for the lumped components are used. They are:

$$\begin{aligned} L_p &= L_{bpp} + L_{bp} + L_{mp} \\ L_n &= L_{bnp} + L_{bn} + L_{mn} \\ R_p &= R_{Lbp} + R_{bpp} + R_{mp} \\ R_n &= R_{Lbn} + R_{bnp} + R_{mn}. \end{aligned}$$

The definitions for R_b and L_b, as shown in equation 3.108 and 3.109, are still valid. For the detailed analysis of the turn-on process, it will be divided into two stages. These stages will now be treated separately. Time is defined as $t = 0$ at the start of the t_{fvm} phase of $v_{ce(G_p)}$.

Stage 1: $0 \leq t < t_{cz} + t_\beta$

At t_{cz} i_{bn} reaches zero. During this first stage the current shifts to G_p and the collector-emitter voltage of this IGBT can be in any of its three phases (see Figure 3.10 and equation 3.60). The circuit can be described by

$$\frac{di_{bp}}{dt} + \left(\frac{\alpha}{\beta}\right) i_{bp} = \frac{V_d + V_{D_n(on)} + I_o\left(R_b + R_{D_n}\right) - v_{ce(G_p)}}{\beta} \tag{3.142}$$

with

$$\beta = 2L_b \tag{3.143}$$

$$\alpha = 2R_b + R_{D_n} \quad \text{for} \quad t \leq \left(t_{fvm} + t_{tvm}\right) \tag{3.144}$$

$$\alpha = 2R_b + R_{D_n} + R_{G_p} \quad \text{for} \quad t > \left(t_{fvm} + t_{tvm}\right). \tag{3.145}$$

The general solution for i_{bp} is

$$i_{bp} = c_1 e^{-\left(\frac{\alpha}{\beta}\right)t} + At + B. \tag{3.146}$$

The expressions for A and B during the different phases of $v_{ce(G_p)}$ are:

$0 \leq t < t_1$ $(t_1 = t_{fvm})$

$$A = \frac{\left(V_d + I_o\left(R_b + R_{D_n}\right)\right)\left(1 - B_m\right)}{\alpha t_{fvm}} \tag{3.147}$$

$$B = \frac{V_{D_n(on)} - 2AL_b}{\alpha} \tag{3.148}$$

$t_1 \leq t < t_2 \ (t_2 = t_{fvm} + t_{tvm})$

$$A = \frac{B_m \left(V_d + I_o \left(R_b + R_{Dn}\right)\right)}{\alpha t_{tvm}} \tag{3.149}$$

$$B = \frac{V_{D_n(on)} - 2AL_b + \left(V_d + I_o \left(R_b + R_{D_n}\right)\right)\left(1 - B_m \left(1 + \frac{t_{fvm}}{t_{tvm}}\right)\right)}{\alpha} \tag{3.150}$$

$t_2 \leq t$

$$A = 0 \tag{3.151}$$

$$B = \frac{V_d + V_{D_n(on)} - V_{G_p(on)} + I_o \left(R_b + R_{Dn}\right)}{\alpha}. \tag{3.152}$$

The constant c_1 can be expressed as

$$c_1 = \frac{i_{bp}(t_i) - At - B}{e^{-\left(\frac{\alpha}{\beta}\right)t}}. \tag{3.153}$$

Stage 2: $t_{cz} + t_\beta \leq t < t_{cz} + t_{rr}$

During stage 2 D_n is modeled as a linear current source i_{drr} in parallel with a parasitic output capacitance C_{D_n}. The differential equation that describes the circuit is

$$\frac{d^2 i_{bp}}{dt^2} + \left(\frac{\alpha}{\beta}\right)\frac{di_{bp}}{dt} + \left(\frac{1}{\beta C_{D_n}}\right) i_{bp} = \frac{1}{\beta}\left(\frac{I_o - i_{drr}}{C_{D_n}} - \frac{dv_{ce(G_p)}}{dt}\right) \tag{3.154}$$

with

$$\beta = 2L_b \tag{3.155}$$

$$\alpha = 2R_b \quad \text{for} \quad t \leq (t_{fvm} + t_{tvm}) \tag{3.156}$$

$$\alpha = 2R_b + R_{G_p} \quad \text{for} \quad t > (t_{fvm} + t_{tvm}). \tag{3.157}$$

The general solution of i_{bp} is in the form of

$$i_{bp} = c_2 e^{m_2 t} + c_3 e^{m_3 t} + Ct + D \tag{3.158}$$

with

$$m_2, m_3 = -\frac{\alpha}{2\beta} \pm \sqrt{\left(\frac{\alpha}{2\beta}\right)^2 - \frac{1}{\beta C_{D_n}}}. \tag{3.159}$$

The constants for the different phases in $v_{ce(G_p)}$ are:

$0 \leq t < t_1 \ (t_1 = t_{fvm})$

$$D = \frac{C_{Dn}\left(V_d + I_o\left(R_b + R_{Dn}\right)\right)\left(1 - B_m\right)}{t_{fvm}} + I_o + I_{rr} - C\left(2C_{Dn}R_b + t_{br}\right) \quad (3.160)$$

$t_1 \leq t < t_2 \ (t_2 = t_{fvm} + t_{tvm})$

$$D = \frac{C_{Dn}B_m\left(V_d + I_o\left(R_b + R_{Dn}\right)\right)}{t_{fvm}} + I_o + I_{rr} - C\left(2C_{Dn}R_b + t_{br}\right) \quad (3.161)$$

$t_2 \leq t$

$$D = I_o + I_{rr} - C\left(C_{Dn}\left(2R_b + R_{G_p}\right) + t_{br}\right). \quad (3.162)$$

For all three phases in the $v_{ce(G_p)}$ waveform the constants C, c_2 and c_3 can be expressed as

$$C = -\frac{I_{rr}}{t_\gamma} \quad (3.163)$$

$$c_2 = \frac{i'_{bp}(t_i) + m_3\left(Ct_i + D - i_{bp}(t_i)\right) - C}{\left(m_2 - m_3\right)e^{m_2 t_i}} \quad (3.164)$$

$$c_3 = \frac{i'_{bp}(t_i) + m_2\left(Ct_i + D - i_{bp}(t_i)\right) - C}{\left(m_3 - m_2\right)e^{m_3 t_i}}. \quad (3.165)$$

Figure 3.32 shows the comparison between the model that was used for loss calculations (model 1) and the complete model that was developed in this section (model 2). A list of parasitic component values is given in Table 3.9. In Figure 3.32a the collector-emitter voltage v_{ce} and the predicted turn-on i_c waveforms for G_p at $I_o = 90\,A$ are shown. In Figure 3.32b the output current is $I_o = 180\,A$. For $i_c < I_o$ the difference between the i_c waveforms predicted by model 1 and 2 are negligible. This implies that the effect of parasitic resistance and stray inductance during the turn-on cycle is very small. However, when i_c becomes equal or bigger that I_o, a significant difference between the models is observed. Model 1, not taking the reverse recovery of D_n into account, keeps the collector current constant and equals to I_o once it has reached that value. However, the collector current continues to grow according to model 2 in order to supply the reverse recovery current of D_n. The bus inductors will also try to maintain the reverse recovery current even after D_n is completely off.

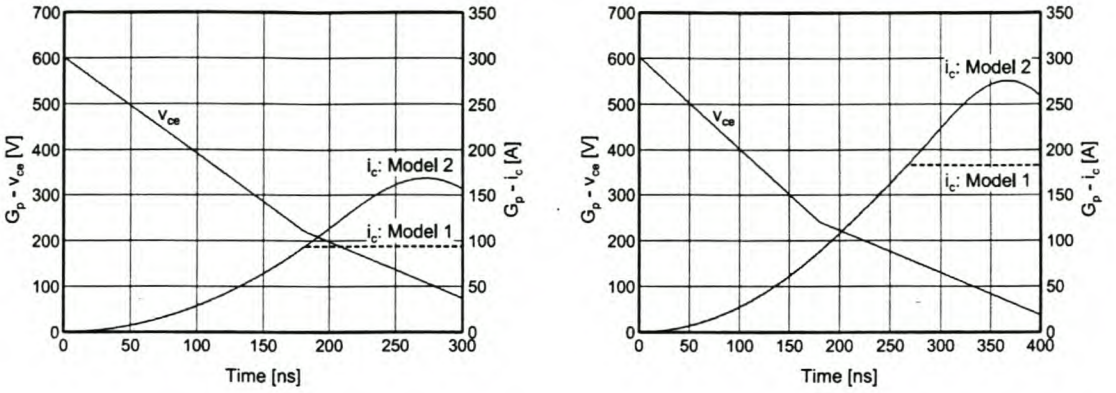


Figure 3.32: Comparison of theoretical models during main IGBT turn-on: (a) $I_o = 90\,A$; (b) $I_o = 180\,A$.

It is clear that the reverse recovery of D_n will lead to higher turn-on losses than predicted by model 1. In the experimental inverter the extra collector current predicted by model 2 will always, independent of the magnitude of I_o, occur during a stage were v_{ce} is still bigger than its on-state value. Unlike the turn-off cycle, parasitic components do not influence the turn-on losses significantly.

Measured waveforms during the turn-on of G_p are compared to theoretical models in Figure 3.33. The tail-forming turn-on model for v_{ce} is compared to measured v_{ce} waveforms and the predicted i_c waveforms are compared to measured i_c waveforms. These comparisons are done at output currents levels of 45, 90, 135 and 180 A. It should be noted that the collector current shown was not measured directly. An estimate of the collector current waveform was obtained by integrating the voltage across L_{bp}. Given this inaccurate method of current measurement, the correlation between the measured i_c waveforms and the predicted waveforms are acceptable. The model provides a good estimate of the peak collector current that will occur in a specific case.

In Figure 3.33 it can be seen that the tail-forming v_{ce} model fits the measured v_{ce} waveforms fairly accurately. The period where the largest differences occur is during the v_{ce} tail period (around 300-350 ns), especially at higher output current levels. The v_{ce} waveforms show clear "tail bumps" that are discussed in [23], [26] and [30]. It was stated in section 3.5 that the linear tail-forming switching model is a first order approach and that it is chosen due to the complexities involved in predicting the switching behaviour under soft-switching condition. It should be noted that the t_{fvm}, t_{tvm} and B_m parameters were adjusted for every output current level to optimise the correlation between the model and the measured waveforms. To improve the accuracy of the optimisation procedure, the dependence of these parameters on the output currents should be incorporated into the optimisation procedure.

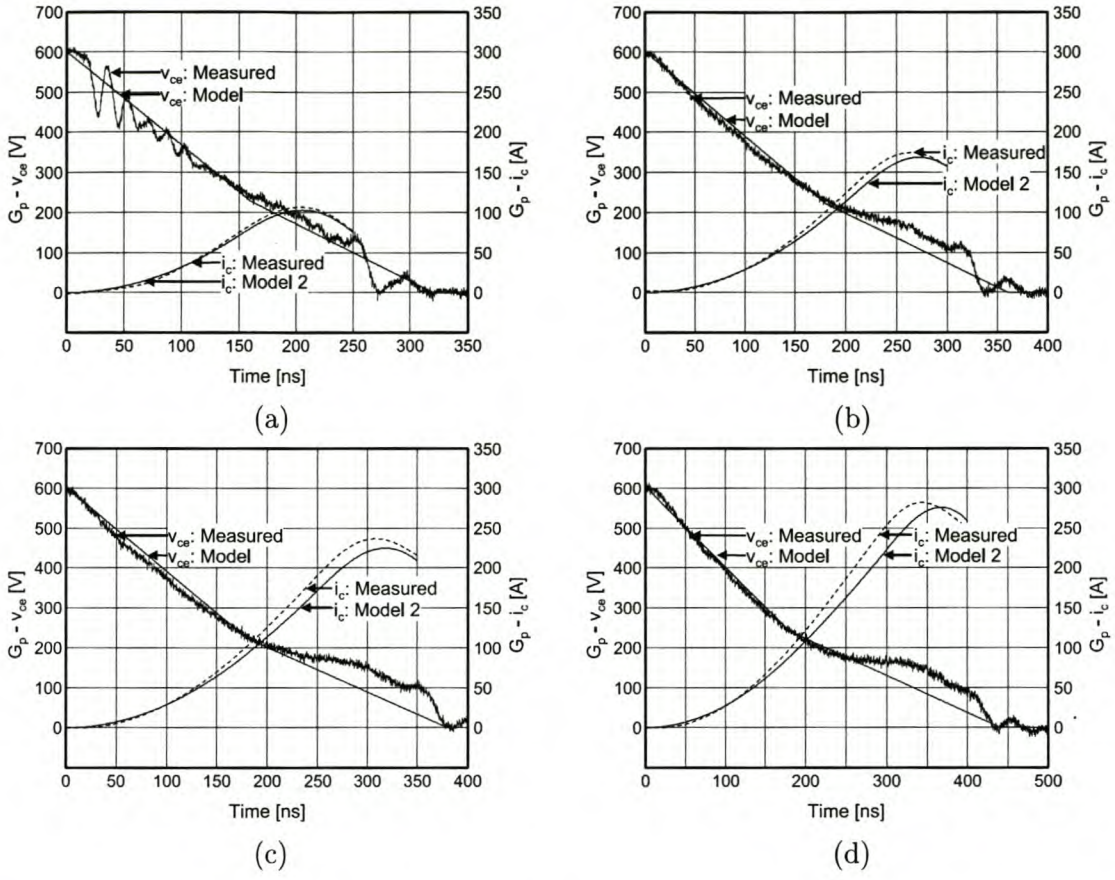


Figure 3.33: Comparisons between predicted and measured waveforms during main IGBT turn-on: (a) $I_o = 45\,A$; (b) $I_o = 90\,A$; (c) $I_o = 135\,A$; (d) $I_o = 180\,A$.

In Figure 3.34 the predicted voltage waveforms across G_p, during the reverse recovery of D_p, are compared to measured waveforms. This is done at output current levels of -45 A, -90 A, -135 A and -180 A. Also shown in Figure 3.34 are the measured collector current of G_n and v_{Crp}. The reverse recovery of D_n starts as soon as $i_c > |I_o|$. Depending on the magnitude of the output current, the voltage across the diode remains essentially constant for another 50 ns before it starts to rise. This corresponds to the transition between periods t_β and t_γ of the reverse recovery process as illustrated in Figure 3.24. The growth in v_{ce} continues until it reaches the level of v_{Crp}. At this stage D_{rp} becomes forward biased and v_{ce} is clamped to v_{Crp}.

For all the cases shown in Figure 3.34 the collector current of G_n is still considerably bigger than the output current when D_{rp} clamps v_{ce} to v_{Crp}. The result is that part of the extra energy stored in the bus inductors will be transferred to C_{rp}. This process will continue for the whole negative output current cycle. Under discontinuous snubber operation C_{rp} is never discharged during the negative output current cycle and it is only discharged for limited periods under a charge assistance scheme. A steady voltage rise across C_{rp} and C_{rn} can therefore be expected

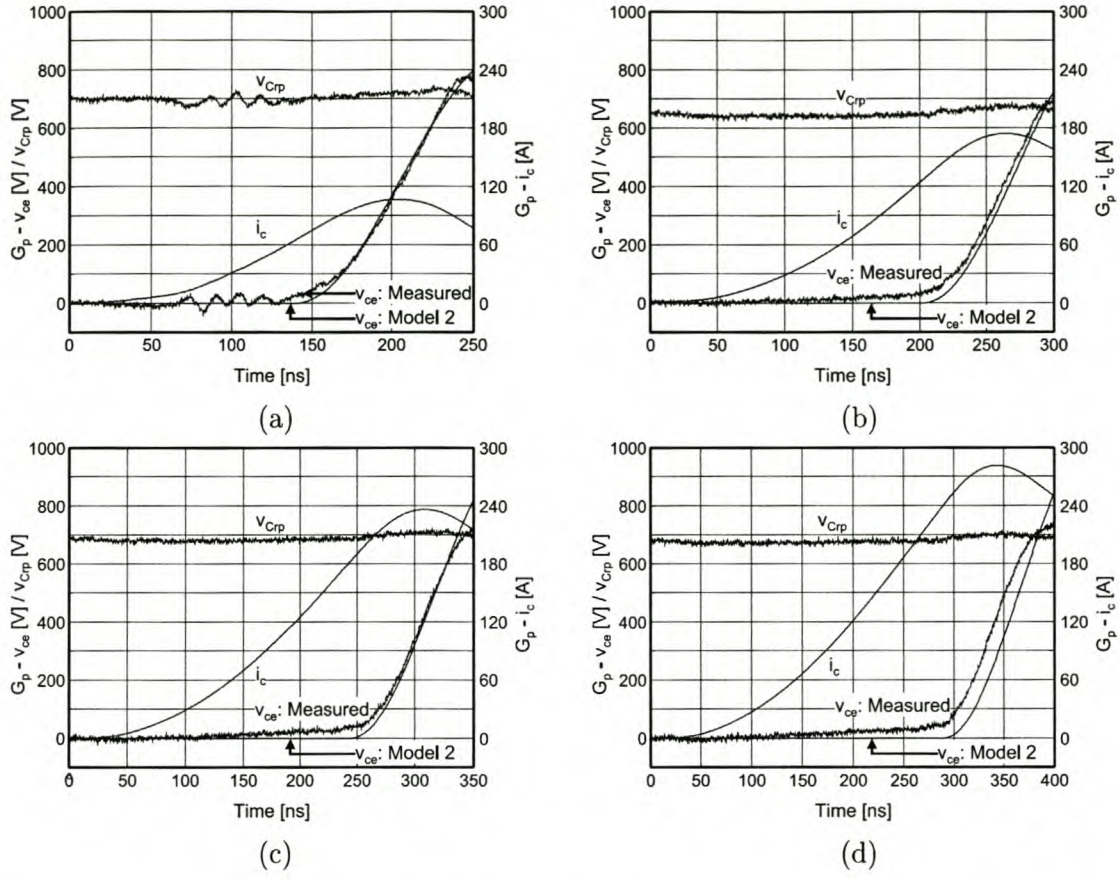


Figure 3.34: Comparisons between predicted and measured waveforms at the reverse recovery of a free-wheeling diode D_n: (a) $I_o = -45\,A$, (b) $I_o = -90\,A$, (c) $I_o = -135\,A$, (d) $I_o = -180\,A$.

during negative and positive output currents respectively. The extent of this voltage rise was measured for the experimental inverter. It was found to be excessive and could have led to the destruction of main or auxiliary devices. To limit the voltage rise 70 kΩ bleeding resistors were connected across the snubber capacitors.

In Figure 3.35 v_{Crp} and I_o are shown for a complete fundamental cycle. During large positive output current the constant charging and discharging of C_{rp} can be seen. During negative output current there is a voltage rise on C_{rp}, but it is clear that the 70 kΩ bleeding resistors are sufficient to limit this voltage rise to a safe level.

3.8.3 Snubber capacitor discharge cycle

In this section measured waveforms obtained from the experimental inverter during the snubber capacitor discharge cycle will be discussed and compared to predictions by theoretical models. A complete analysis of this discharge cycle will also be performed.

Figure 3.36 shows the circuit that comes into play during the snubber capacitor discharge

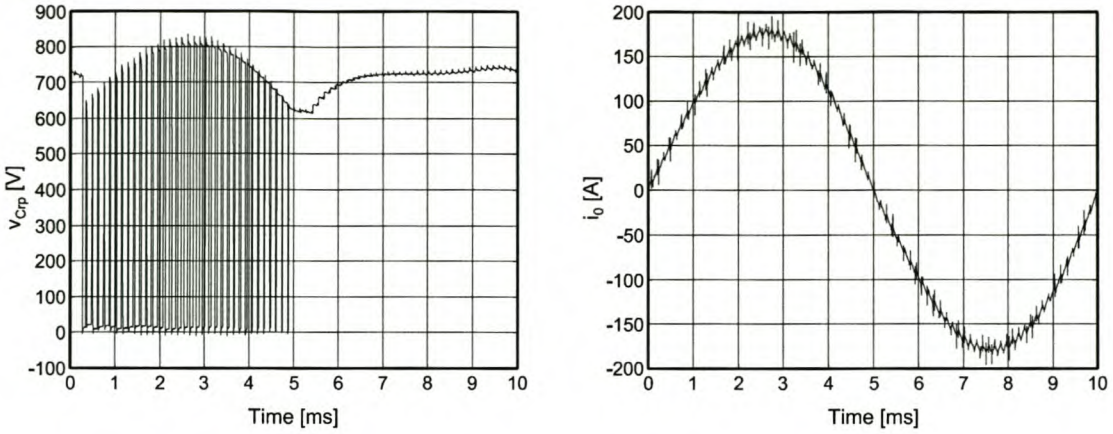


Figure 3.35: Snubber capacitor voltage (a) and output current (b) for a fundamental modulation period.

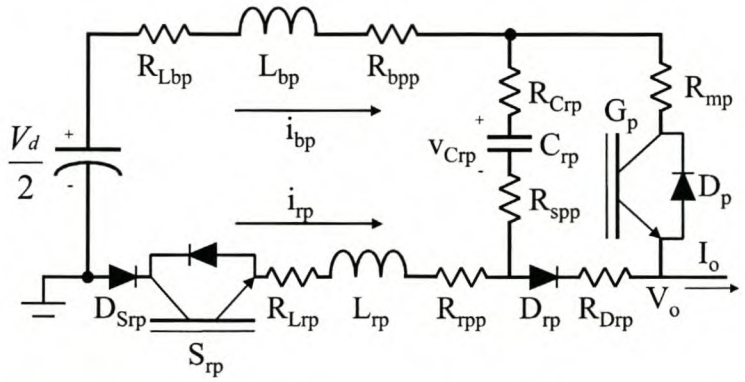


Figure 3.36: Complete snubber circuit as used in the detailed analysis of the snubber capacitor discharge cycle.

cycle (large positive output current is assumed). In the analysis tail-forming switching behaviour for S_{rp} at turn-on is assumed. This model was described in equation 3.72. After S_{rp} is completely on, the device is modeled with an on-state voltage $V_{S_{rp}(on)}$ and an ESR R_{Srp}. Due to very low $\frac{di_R}{dt}$ experienced by D_{Srp} at its turn-off, the reverse recovery of the diode is not included in the analysis. During current conduction its on-state voltage is $V_{D_{Srp}(on)}$ and its ESR is $R_{D_{Srp}}$. Due to the large value of L_{rp}, the effect of parasitic inductance is small and can be neglected. Parasitic components, which have not been previously discussed, are R_{Lrp}, the ESR of L_{rp}, and the parasitic resistance of the auxiliary switch and resonant inductor path R_{rpp}. Definitions for lumped components that are used in the analysis are:

$$R_b = R_{Lbp} + R_{bpp}$$
$$R_s = R_{Crp} + R_{spp}$$

$$R_r = R_{Lrp} + R_{rpp}$$
$$R_G = R_{Gp} + R_{mp}.$$

For the detailed analysis of the turn-on process, it will be divided into two stages. These stages will be now be treated separately. Time is defined as $t = 0$ at the start of the t_{fva} phase of $v_{ce(S_{rp})}$.

Stage 1: $0 \leq t < t_{vz}$

At t_{vz} $v_{Crp} = 0$. Before this time the differential equation that describes the circuit is

$$\frac{di_{rp}^2}{dt^2} + \left(\frac{\alpha}{\beta}\right)\frac{di_{rp}}{dt} + \left(\frac{1}{\beta C_{rp}}\right) i_{rp} = -\left(\frac{1}{\beta}\right)\frac{dv_{ce(S_{rp})}}{dt} \tag{3.166}$$

with

$$\beta = L_{bp} + L_{rp} \tag{3.167}$$
$$\alpha = R_b + R_s + R_r + R_{D_{Srp}} \quad \text{for} \quad t \leq (t_{fva} + t_{tva}) \tag{3.168}$$
$$\alpha = R_b + R_s + R_r + R_{D_{Srp}} + R_{S_{rp}} \quad \text{for} \quad t > (t_{fva} + t_{tva})\,. \tag{3.169}$$

The general solution for i_{rp} is in the form of

$$i_{rp} = c_1 e^{m_1 t} + c_2 e^{m_2 t} + A \tag{3.170}$$

with

$$m_1, m_2 = -\frac{\alpha}{2\beta} \pm \sqrt{\left(\frac{\alpha}{2\beta}\right)^2 - \frac{1}{\beta C_r}}. \tag{3.171}$$

The expression for A during the different phases in $v_{ce(S_{rp})}$ is:

$0 \leq t < t_1$ $(t_1 = t_{fva})$

$$A = -\frac{V_{init}\,(1 - B_a)\,C_{rp}}{t_{fva}} \tag{3.172}$$

$t_1 \leq t < t_2$ $(t_2 = t_{fva} + t_{tva})$

$$A = -\frac{V_{init} B_a C_{rp}}{t_{tva}} \tag{3.173}$$

$t_2 \leq t$

$$A = 0 \tag{3.174}$$

with V_{init} the voltage across S_{rp} at the start of the discharge cycle. This voltage is equal to the difference between the snubber capacitor voltage, at the start of the discharge cycle, and half the bus voltage. For all the phases the constants c_1 and c_2 can be expressed as

$$c_1 = \frac{i'_{rp}(t_i) + m_2\left(A - i_{rp}(t_i)\right)}{(m_1 - m_2)\, e^{m_1 t_i}} \tag{3.175}$$

$$c_2 = \frac{i'_{rp}(t_i) + m_1\left(A - i_{rp}(t_i)\right)}{(m_2 - m_1)\, e^{m_2 t_i}}. \tag{3.176}$$

Stage 2: $t_{vz} \leq t < t_{cz}$

At t_{cz} i_{rp} reaches zero and the discharge cycle is complete. For the period before this time instant the circuit is described by

$$\frac{di_{rp}}{dt} + \left(\frac{\alpha}{\beta}\right) i_{rp} = \frac{1}{\beta}\left(I_o\left(R_b + R_g\right) - \frac{V_d}{2} + V_{tot(on)}\right) \tag{3.177}$$

with

$$\alpha = R_b + R_g + R_r + R_{D_{rp}} + R_{S_{rp}} + R_{D_{Srp}} \tag{3.178}$$

$$\beta = L_{rp} + L_{bp} \tag{3.179}$$

$$V_{tot(on)} = V_{G_p(on)} - V_{D_{rp}(on)} - V_{S_{rp}(on)} - V_{D_{Srp}(on)}. \tag{3.180}$$

The solution for i_{rp} is

$$i_{rp} = c_3 e^{-\left(\frac{\alpha}{\beta}\right)t} + B \tag{3.181}$$

with

$$c_3 = \frac{i_{rp}(t_i) - B}{e^{-\left(\frac{\alpha}{\beta}\right)t_i}} \tag{3.182}$$

$$B = \frac{1}{\alpha}\left(I_o\left(R_b + R_g\right) - \frac{V_d}{2} + V_{tot(on)}\right). \tag{3.183}$$

Figure 3.37a shows the comparison between the model that was used for loss calculations (model 1) and the complete model that was developed in this section (model 2). The snubber capacitor voltage v_{Crp} and inductor current i_{rp} are shown at an output current level of 90 A. It is clear that the parasitic resistance, incorporated in model 2, provides considerable damping to the resonant discharge cycle. The peak value of i_{rp} predicted by model 2 is therefore smaller and the discharge cycle takes longer than predicted by model 1.

In Figure 3.37b measured waveforms during the discharge cycle of C_{rp} are compared to predicted waveforms obtained from model 2. The correlation between the measured and the

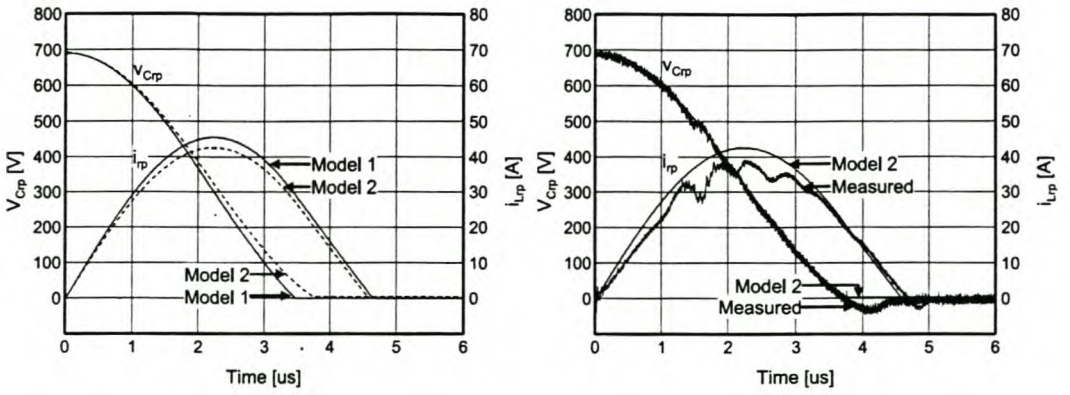


Figure 3.37: (a) Comparison of theoretical models for the snubber capacitor discharge cycle ($I_o = 90\,A$); (b) Comparison of predicted and measured waveforms for the snubber capacitor discharge cycle ($I_o = 90\,A$).

Bus-Bar Inductance	L_{bpp}, L_{bnp}	19 nH
Bus-Bar Resistance	R_{bpp}, R_{bnp}	1 mΩ
Module Stray Inductance	L_{mp}, L_{mn}	25 nH
Snubber Stray Inductance	L_{spp}	70 nH
Main IGBT On-State Voltage	$V_{G_p(on)}$	1.5 V
Main IGBT On-State Resistance	R_{G_p}	4 mΩ
Free-wheeling Diode On-State Voltage	$V_{D_n(on)}$	0.8 V
Free-wheeling Diode On-State Resistance	R_{D_n}	5 mΩ

Table 3.9: Summary of parasitic component values and on-state parameters for the main IGBTs used in the experimental inverter.

predicted v_{Crp} waveforms is excellent. The measured current waveforms, however, are noisy. This can be attributed to high $\frac{dv}{dt}$s in the inverter during this interval that is caused by the turn-on of G_p. In Table 3.9 a summary of parasitic component values for the experimental inverter is shown. The on-state voltage and resistance for the main IGBTs and free-wheeling diodes are also given. For the auxiliary components similar parameters were listed in Table 3.7. The values shown in Table 3.9 were obtained from component data sheets and from measurements made in [58] on the same basic experimental inverter.

3.8.4 Efficiency measurements

The total converter losses were measured at conditions specified in Table 3.7. The calorimetric technique, described in section 2.7.1, was used for this purpose. The wooden container used for the inverter with the turn-off snubber was adapted for the combined snubber inverter. The thermal resistance of the modified container was measured as 3 WK^{-1}.

Switching Method:	Hard Switching	Turn-off Snubber	Combined Snubber
Calculated Losses [W]			
Main IGBT Turn-off Loss	108	30	30
Main IGBT Turn-on Loss	124	124	34
Main IGBT Conduction Loss	101	101	101
Free-wheeling Diode Loss	123	123	123
Snubber Circuit Loss	0	7	8
Bleeding Resistor Loss	0	0	10
DC Bus Capacitor Loss	120	120	120
Total	576	505	426
Measured Losses [W]			
Total	544	476	450

Table 3.10: Comparison of measured and calculated losses in the experimental inverter.

In Table 3.10 the results of these measurements are shown. Values for measured losses were obtained by averaging at least three two-hour measurements. The thermal time constant of the system was similar to that shown in section 2.7.1. It should be noted that the predicted turn-off losses are calculated with a more complete model. This model, which incorporates the effect of parasitic components in the turn-off snubber, was described in [58].

It can be seen that the measured losses in the inverter, fitted with the combined snubber, are higher than predicted. This difference can be mainly attributed to the extra turn-on losses due to the reverse recovery of the free-wheeling diodes. Although not as high as predicted, the measurements still suggest an improvement in total switching losses of 48% and an improvement in total effective switching losses of 41%. For the turn-off snubber case the improvement in total switching losses was 32% and the improvement in total effective switching losses was 29%.

3.9 Conclusion

The basic operation principles of the combined resonant snubber were discussed. Operation strategies were evaluated and topology protection schemes were investigated. Analytical expressions, describing the losses in the snubber components and the main IGBTs, were derived. An optimisation procedure, based on these expressions, was then developed and used to design an experimental 1-ϕ inverter. This inverter was constructed and used to verify theoretical models.

It was shown experimentally that both a discontinuous and a uni-directional charge assistance operation strategy can be used for the combined snubber topology. The influences of parasitic components were also illustrated. It was shown that the reverse recovery of the free-wheeling diodes has a negative influence on the turn-on losses and that it also causes charge

build-up on the snubber capacitors. The latter introduces the need for bleeding resistors that increase the effective snubber losses considerably. It was measured that the combined snubber can reduce the switching losses in the main IGBTs by 48%.

Chapter 4

Design of a three-phase soft-switching inverter

4.1 Introduction

In this chapter the development of a high-power, soft-switching, 3-ϕ IGBT inverter is described. The chapter will start off with a comparison between the active resonant turn-off and the active resonant combined snubber. Based on this comparison the most suitable topology for a practical 3-ϕ inverter will be selected. After the selection is made, the experimental soft-switching inverter will be designed. This process will be separated into two parts. Firstly, a normal hard-switching 3-ϕ inverter will be designed which will then be followed by the design of an appropriate snubber. To determine optimal values for the snubber components, the optimisation procedure developed in section 3.6 will be used. However, further refinements to this procedure will be made. Changes will also be implemented to make the procedure more applicable to the selected topology. The experimental inverter will be constructed and the chapter will be concluded with experimental results.

4.2 Selection of topology

In Chapter 2 the **active resonant turn-off snubber** was discussed. It was shown that the addition of this snubber to a standard hard-switching inverter can reduces turn-off losses considerably. If bus inductors are also added, a reduction in both turn-on and turn-off switching losses can be achieved. This topology was discussed in Chapter 3 and it was called the active resonant combined snubber. Basic operation principles and operation strategies for both topologies were discussed in Chapters 2 and 3 respectively. Analytical loss expressions for the combined snubber topology were also derived and used as the basis of an optimisation procedure. The effects of parasitic components and diode reverse recovery in this topology were also studied. In [58] similar detailed studies on the turn-off snubber were performed. For both topologies

Switching Method:	Hard Switching	Turn-off Snubber		Combined Snubber	
	[W]	[W]	%	[W]	%
Turn-off Losses	108	33	30.6	33	30.6
Effective Turn-off Losses	108	40	37.0	40	37.0
Turn-on Losses	124	124	100	87	70.2
Effective Turn-on Losses	124	124	100	98	79.0
Total Switching Losses	232	157	67.7	120	51.7
Effective Total Switching Losses	232	164	70.7	138	59.5

Table 4.1: Measured main IGBT switching losses in the experimental single-phase inverters.

the theoretical models were verified with experimental results and the achievable reduction in switching losses were measured under exactly the same inverter conditions.

Based on the experienced gained and the data collected in [58] and the previous chapters, the two topologies will be compared in order to determine the one which is most suitable to a practical 3-ϕ inverter. Aspects like cost, effectiveness, complexity and reliable protection schemes will be considered. For this purpose, it will be assumed that a three-phase soft-switching inverter is in effect just three one-phase soft-switching inverters with a common bus. However, this is not necessarily the only implementation option available. For instance, there is a possibility that only one set of bus inductors can be used in the combined snubber topology. No detailed studies on such 3-ϕ topology simplification have been performed and will therefore not be taken into account.

1. **Effectiveness.** In section 3.8.4 loss measurements obtained for both topologies under exactly the same conditions were given. In Table 4.1 the measured main IGBT switching losses are summarised. These values are derived directly from Table 3.10. The effective switching losses are again defined as the actual switching losses in the main IGBTs plus extra losses introduced by the snubber. Also shown in Table 3.8.4 are the losses expressed as a percentage of the hard-switching losses.

   The main IGBT collector-emitter voltage and the collector current during turn-off, as obtained from the experimental 1-ϕ inverter, were shown in Figure 3.28. In this figure it can be seen that, even at the maximum allowable output current, the voltage rise time is larger than the sum of the collector current fall and tail time. Thus, the extra voltage overshoot across these devices, due to the bus inductor resonance, does not have a major influence on the turn-off losses. In calculating the values shown in Table 4.1 it was therefore assumed that the addition of the bus inductors in the combined snubber does not influence the turn-off losses. On the other hand, it is anticipated that the reverse recover losses in the free-wheeling diodes are strongly influenced by the addition of the bus inductors. However, this was not studied in detailed or experimentally verified. Extra

measured losses in the combined topology, due to these or any other unforeseen ways, are therefore treated as main IGBT turn-on losses.

It is clear from Table 4.1 that the turn-off losses are more effectively reduced than the turn-on losses. The turn-off snubber achieves a reduction in main IGBT turn-off losses of 69.4% while the turn-on snubber only reduces the turn-on loses by 29.8%. Due to the extra losses in the bleeding resistors, the performance of the turn-on snubber is even worst if effective switching losses are compared. Although not as effective, the combined snubber does improve the reduction in main IGBT switching losses by a further 16% compared to just using the turn-off snubber.

2. **Complexity.** Complexities involved in three aspects of the topologies will be compared. They are control methods, design procedures and construction.

   With respect to control, the two topologies are identical. The possible control strategies for the two are exactly the same. It was also shown that the simplest control option for both these topologies is the discontinuous snubber operation strategy.

   The design procedure of the combined snubber is more complex than the design of the turn-off snubber. The reason for this lies in the extra design parameter of the combined snubber topology. The extra parameter also introduces new trade-offs and complex restrictions that the designer need to keep in mind.

   With respect to construction, a large percentage of the effort in the implementation of the combined snubber topology goes into the turn-off snubber. This is because the majority of the snubber components are involved in this topology and all the hardware necessary to control and drive the auxiliary switches have to be implemented. The effect of layout and the associated parasitic components are also very important in the turn-off snubber. The placement of the snubber capacitors and diodes are critical if low stray inductance needs to be achieved. However, the implementation of the bus inductors are not as critical. Although there is not a big difference in construction complexity, it is very important to note that the turn-off snubber can, in most cases, just be added to a existing hard-switching inverter. For the combined snubber, alterations to or a different bus-bar structure is necessary.

3. **Cost.** The cost comparison is strongly dependent on the specific implementation and will vary considerably with the choice of snubber components and the power level of the inverter. The costs of the snubbers used in the experimental inverters of Chapters 2 and 3 are therefore only rough indications. The extra control requirements of the snubbers are also included in the cost analysis.

   In Table 4.2 the costs involved in the two snubber topologies are shown. It can be seen

Item	Cost [R]	Cost [R]
Snubber Capacitors	25	25
Resonant Inductors	35	35
Bus Indcutors	-	35
Snubber Diodes	190	190
Auxiliary Switches	146	146
Control and Drive Circuits	138	138
PCBs	160	160
TOTAL:	694	729

Table 4.2: Cost comparison between turn-off and combined snubber.

that the price difference between the two topologies is very small, only about 5%. The total cost of the snubber is about half of the cost of the main IGBT module.

4. **Protection.** It was shown in section 2.4 that, for the turn-off snubber topology, no additional protection for the main IGBTs is necessary. However, additional protection schemes for the auxiliary switches were necessary. These protection strategies were discussed in detail in section 2.4. For the combined snubber it was shown that the protection requirements for the auxiliary switches are identical to the turn-off snubber, but extra provision has to be made for the main IGBTs. A very slow fault current turn-off and the use of active zener voltage clamps were mentioned in section 3.3.6. However, a major drawback of these protection strategies is that they cannot be used in conjunction with standard IPMs.

If only the cost, complexity and effectiveness are compared, the ratio of advantages to disadvantages for the two topologies are very similar. The combined snubber can lower the switching losses substantially for only a small increase in the snubber cost, while the turn-off snubber is simpler and can be added to a standard inverter. However, the major difference between the topologies lies in reliable protection. No extra strategies are necessary to protect the main IGBTs in the turn-off snubber, while there is a need for extra methods to make device protection in the combined snubber reliable. The trend in power electronics is also more and more towards integration. The fact that the protection schemes for the combined snubber topology are not compatible with standard hard-switching IPMs is therefore a great disadvantage. The trench gate IGBTs selected for the the 3-ϕ inverter also have far more turn-off losses than turn-on losses, further reducing the advantages the combined snubber have. It was therefore decided to use the turn-off snubber topology for the 3-ϕ inverter.

4.3 Design optimisation procedure

The design optimisation procedure developed in section 3.6 will be used as a basis for designing the turn-off snubber in this chapter. However, a few changes and refinements will be made to make this procedure, which was originally developed for the combined snubber, more applicable to the current topology. These alterations will be briefly discussed.

1. In the design optimisation procedure of section 3.6, the value of the bus inductor can be varied as an optimisation parameter. This cannot be done for the turn-off snubber, because no extra bus inductance is added. However, even though great care is usually taken to minimise it, parasitic inductance is always present in a bus-bar structure. For the inverter developed in this chapter the parasitic bus inductance will be measured after the construction of the basic hard-switching inverter. This value will then be used as bus inductance in the procedure of section 3.6 and optimisation will be carried out with only C_r and L_r as parameters.

2. The parameters describing the turn-off waveforms of the PM200DSA120 IGBT module were not directly measured, but values for A_m, t_{fim} and t_{tim} were obtained form [59]. In Chapter 3 it was also assumed that the switching behaviour at turn-off is constant and not dependent on the snubber capacitance or output current level. In this chapter three CM300DU-24F dual IGBT module are used to implement the main switches of the inverter. No data regarding the turn-off behaviour of these devices are available. It was therefore necessary to measure the turn-off waveform parameters for these devices. The dependence of these parameters on snubber capacitance and output current level were also investigated and the design optimisation procedure was adapted to incorporate these dependencies.

3. Measurements were also carried out to obtain parameters describing the turn-on waveform of the CM300DU-24F module. The dependence off these parameters on the output current were also investigated and incorporated into the design optimisation procedure. Although the effect this refinement has on the accurate prediction of optimal snubber components is very small, more accurate predictions of total switching losses are obtained.

4.4 Design of an experimental hard-switching three-phase inverter

As a first step towards developing a 3-ϕ soft-switching inverter, a standard hard-switching 3-ϕ inverter will be designed and constructed. After this has been done, the design and implementation of a snubber will be undertaken. The snubber can then be fitted to the hard-switching

inverter to achieve the desired soft-switching topology.

Different aspects of the development of the hard-switching inverter will be treated in this section. Firstly, a suitable rating for the inverter will be determined, after which a choice of main devices will be made. The bus capacitors will be designed and the requirements for the inverter enclosure will be described. Lastly, the control of the inverter will be discussed.

4.4.1 Inverter rating

As was mentioned in the introduction, the aim of this chapter is to develop a practical, high-power 3-ϕ IGBT inverter. It is therefore essential that the soft-switching inverter developed in this chapter should have voltage and current ratings comparable to a hard-switching inverter based on the same main IGBTs. Due to the experimental nature of the 1-ϕ inverters constructed to verify the turn-off snubber and combined snubber operation, this requirement was not important and therefore not met. The low bus voltage used in these cases provided a large safety margin and simplified comparisons with data sheet values. For the 3-ϕ inverter such under-utilisation of IGBTs cannot be allowed. Therefore, a higher and more practical nominal bus voltage has to be used - a value that will be comparable to the 800 V found in a large number of hard-switching inverters with 1.2 kV devices. This will ensure that an output voltage of 400 V_{ll} can easily be achieved with enough headroom for quick dynamic response. A target power level for the inverter of 100 kVA was set.

To obtain the desired bus voltage, the output of a three-phase variable auto transformer (variac) was rectified after a further step-up transformer stage. This allows for easily adjustable voltage levels during testing phases and a method to achieve soft starting. However, a reactive load had to be used because of the limited power ratings of the available variacs. A 1.2 mH, 50 Hz, 3-ϕ load inductor was available. To facilitate the use of a practical bus voltage and a realistic duty cycle, and not to exceed the desired power level, the modulation frequency had to be increased. At $f_m = 110\,\text{Hz}$ and $V_{ll} = 315\,V$ the phase current was 184 A_{rms} and the total power was 100 kVA. The desired output voltage was achieved with a bus voltage value of 750 V and a D_{max} of 0.85. A 5 kHz switching frequency and a 5 μs blanking time were selected. The inverter parameters are listed in Table 4.3.

4.4.2 Main IGBTs

The CM300DU-24F dual IGBT module from Powerex was chosen for the 3-ϕ inverter. The IGBTs found in this module are punched through device with a trench gate structure. The main advantage of this new technology, compared to standard third-generation planar IGBTs, is the low $V_{ce(sat)}$ values obtainable. At $T_j = 25\,℃$, $I_c = 300\,A$ the CM300DU-24F IGBTs has a $V_{ce(sat)}$ of 1.8 V, while $V_{ce(sat)} = 2.9\,V$ for the third-generation CM300DU-24H devices. This reduction can mainly be attributed to the increased cell density obtainable with the vertical

Parameter	Symbol	Value
Nominal DC Bus Value	V_d	750 V
Maximum Output Power	P_{max}	100 kW
Maximum Duty Cycle	D_{max}	0.85
Line Voltage	V_{ll}	315 V_{RMS}
Phase Current	I_p	184 A_{RMS}
Load Impedance	Z_l	0.99 Ω
Switching Frequency	f_s	5 kHz
Blanking Time	t_b	5 μs

Table 4.3: Design parameters for the experimental three-phase inverter.

Parameter	Symbol	Value
Collector-Emitter Voltage	V_{CES}	1200 V
Collector Current	I_C	300 A
Peak Collector Current	I_{CM}	600 A
Collector Dissipation	P_C	960 W
Turn-on Rise Time	t_r	80 ns
Turn-off Fall Time	t_f	300 ns
Collector-Emitter Saturation Voltage (25 $^\circ$C)	$V_{ce(sat)}$	1.8 V

Table 4.4: Parameters for the CM300DU-24F dual IGBT module.

channels of the trench structure and the use of local lifetime control to increase on-state carrier concentration [53]. A substantial reduction in turn-on losses was also achieved with new fast-recovery free-wheeling diodes. New packaging techniques developed for this modules also led to a reduction of module stray inductance. The only disadvantage of these IGBTs, compared to third-generation devices, is a slightly higher input capacitance. Basic parameters for this IGBT module are listed in Table 4.4.

IPM modules were not considered because of the inferior IGBT technology currently available in these modules. The flexibility with protection and drive circuitry with normal IGBT modules also allow for the expansion of the 3-ϕ system to accommodate a combined snubber in future.

The driver circuits for the CM300DU-24H modules were based on the Powerex M57962L hybrid IC driver in combination with an extra current boost stage. The driver boards have on-board isolated power supplies, and gating signals are received and error signals are sent via optic fibre links. In Figure 4.3 the developed driver board is shown.

4.4.3 Bus capacitors

For the design of the bus capacitance it was assumed that the inverter will be used with a 100 kW load. This load condition places maximum strain on the bus capacitors in terms of ripple

Frequency [Hz]	Simulation result [A_{RMS}]	Capacitor rating [A_{RMS}]
150	118.5	129.6
300	20.5	156.0
4700	33.1	172.2
5000	96.7	172.2
5300	33.1	172.2
10000	17.0	172.2

Table 4.5: Bus capacitor ripple current in the three-phase inverter.

current and ride-through capability. However, it was assumed that the 3-ϕ load is balanced. This implies that the low-frequency ripple current in the phases cancel each other and that only high frequency (around the switching frequency) ripple current is present in the load. However, low-frequency ripple current (150 Hz and harmonics) is present in the capacitors due to the charging of the bus via the six pulse rectifier. PSpice simulations were used to quantify the ripple currents and to determine voltage regulation and ride-through capabilities. A line impedance of 5% was assumed in all simulations.

The Intelcond AYX-HR 3300 μF, 450 V capacitors were chosen as bus capacitors due to availability and low price. Two capacitor banks, C_{dp} and C_{dn}, will be connected in series to provide a centre point and to achieve the desired voltage rating. With six capacitors per bank (12 in total) the six most prominent capacitor ripple current components are listed in Table 4.5. The ripple current ratings of the capacitor bank at 40℃ are also given.

From Table 4.5 it is clear that the selected number of bus capacitors are sufficient for the application. All the ripple current components fall within the capability of the capacitor bank and simulations show that the bus voltage regulation is better than 2%. The expected lifetime of the bus capacitors at 40℃ is 140 kH. To ensure that voltage sharing across the capacitor banks takes place, 33 kΩ sharing resistors were placed across all the bus capacitors. The complete bus-bar structure can be seen in Figure 4.1.

4.4.4 Inverter construction and enclosure

In the construction of the inverter a main consideration was to make provision for calorometric loss measurements. This technique was also used for both single-phase experimental inverters. The technique requires water cooling and an inverter enclosure with a high thermal resistance. A wooden box, as was used for the single-phase inverters, is a practical option for such an container and was again utilised. The main devices were mounted on a custom made water-cooled aluminium heatsink. In order to keep auxiliary components and bus capacitors cool, a radiator was used to achieve heat exchange between the air in the box and the water circulating

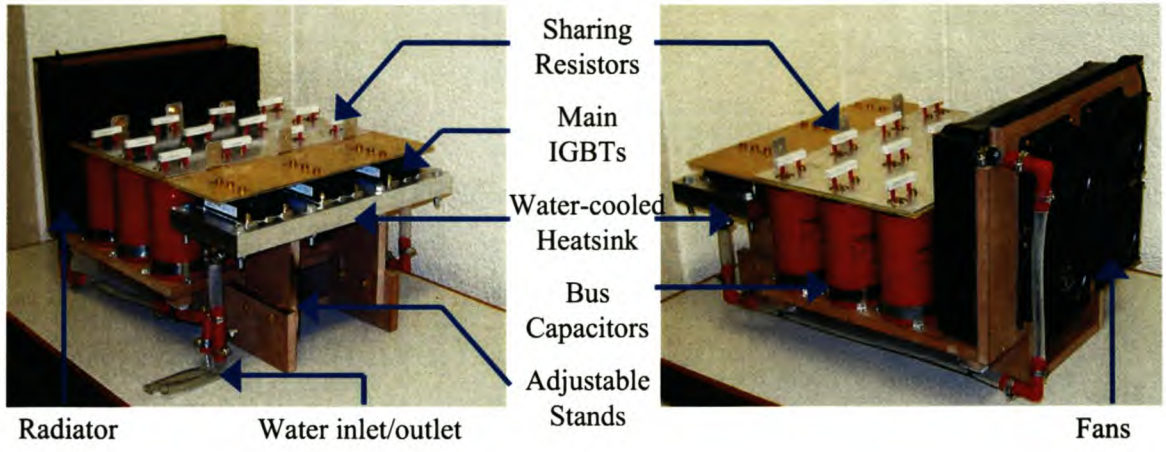


Figure 4.1: Basic constructed three-phase inverter.

through the radiator. Cold water was pumped through the radiator, after which it passed through the heatsink. In-line water temperature sensors were placed in the water pipes where they passed through the container walls.

Four fans were used to force air through the radiator. Great care was taken in creating an air flow path so that all relevant heat-generating auxiliary components and PCBs were exposed to a constant flow of cool air. In Figure 4.1 the basic structure for the inverter can be seen. The hardware shown in Figure 4.1 was placed inside the wooden container. The container is just big enough so that the sides of the radiator and the bus-bar touches the box. This ensures that the air forced through the radiator by the fans have to move over sharing resistors or through the bus capacitors. The air moving over the bus-bar also exposes the PCBs with snubber components and the main IGBT driver boards to cool air. All the air return to the fans via an air-flow path created by the bottom of the wooden container, the inverter stands and the bus capacitor mounting surface. In Figure 4.1 it can also be seen that the heatsink was mounted on adjustable stands. This allows for easy adaptation of the layout in future to accommodate a combined snubber topology.

The complete inverter, with the snubber and driver PCBs fitted, can be seen in Figure 4.13. All the cable and optic fibre holes in the wooden box were sealed to minimise heatloss. Power cable terminals were fitted outside the box on a separate mounting plate. The LEM current sensors were mounted above these terminals. The tight fitting lid of the container can be seen on Figure 4.13 in the background.

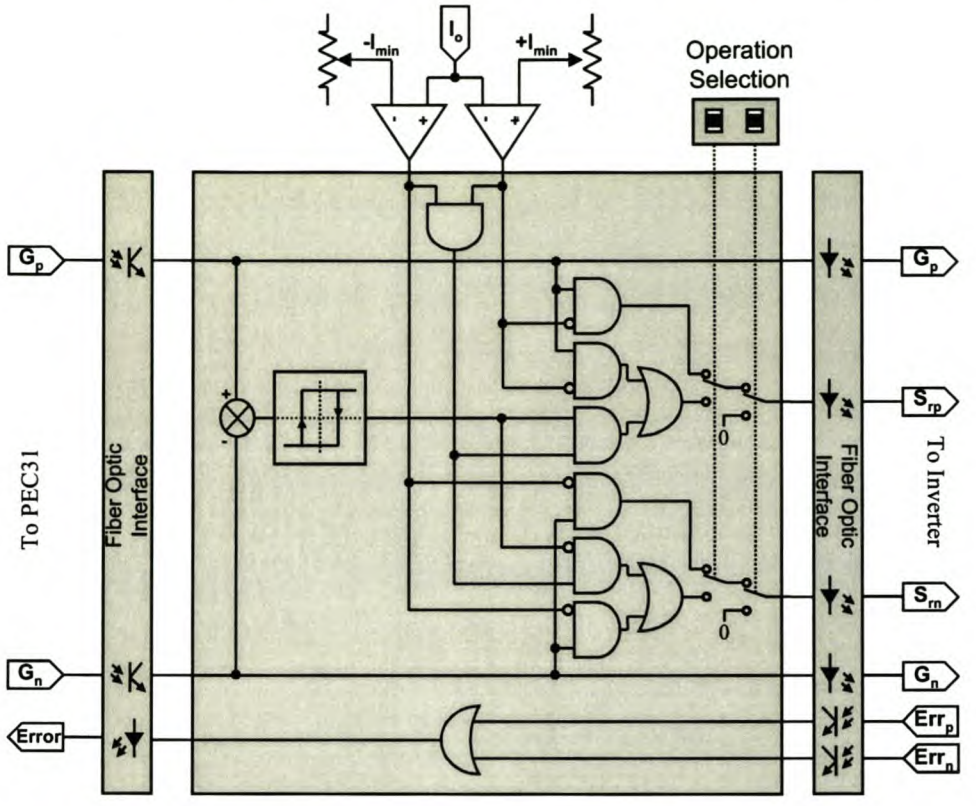


Figure 4.2: High-level schematic diagram of the auxiliary switch controller for a single phase.

4.4.5 Controller

The open-loop PWM control signals for the main IGBTs were generated by a PEC31 controller board. This is a DSP/FPGA-based controller with a Texas Instruments TMS320C31 floating-point digital signal processor and an ALTERA EPM81500 FPGA. This generic controller board was developed by D.D. Bester within the Power Electronic Research Group of the University of Stellenbosch. The function of the DSP is to execute the required control algorithms, while the FPGA is used for high-speed, low-level tasks. The main IGBT error signals were fed back to the controller for error handling and protection. An additional optic fibre interface was used in conjunction with this controller to facilitate optical communication.

For the soft-switching topology an additional controller is necessary. A secondary controller was therefore developed to generate the appropriate auxiliary switch control signals. With the main IGBT gating signals and the phase current measurements as inputs to the controller, the auxiliary switch gating signals are generated. An ALTERA EPM7064SLC44 EPLD was used to perform the necessary logic functions. With dip-switch settings on the controller board it is possible to select between normal hard-switching, discontinuous snubber operation and

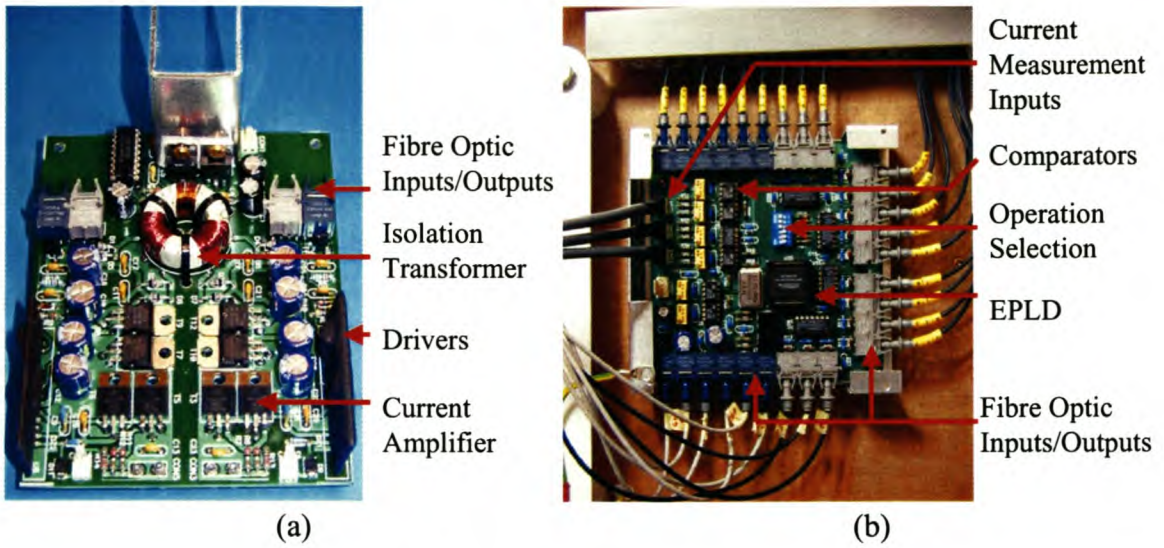


Figure 4.3: (a) Main IGBT driver board; (b) EPLD base auxiliary switch controller.

uni-directional snubber operation on a per phase basis. The current reference values for each phase can also be set independently.

In Figure 4.2 a high-level schematic diagram of the secondary controller can be seen (only one phase shown). The developed PCB can be seen in Figure 4.3b and in Figure 4.13 the secondary controller board is visible as it is mounted on the side of the wooden container housing the experimental inverter.

4.5 Design of an optimal snubber

In the previous section the development of a hard-switching 3-ϕ inverter with a power rating of 100 kVA was described. In this section an optimal turn-off snubber for this inverter will be designed. The snubber will be constructed in a modular form that can be easily added to the hard-switching inverter. Before optimal values for snubber components can be determined, the parameters describing the main IGBT switching behaviour and the parasitic bus inductance have to be measured. This process will be described and will be followed by a brief discussion on the choice of snubber components. The section will be concluded with results obtained from the refined optimisation procedure.

4.5.1 Measurement of main IGBT switching behaviour

As explained in section 4.3, parameters describing the turn-off switching behaviour of the PM200DSA120 IGBT module were not directly measured, but obtained from [59]. It was also

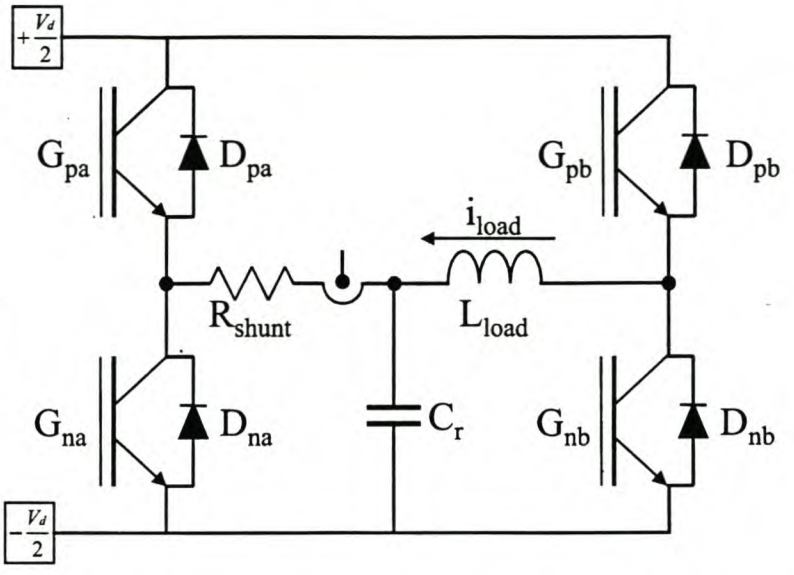


Figure 4.4: Experimental setup to measure main IGBT turn-off current.

assumed in Chapter 3 that these parameters are not functions of collector current or snubber capacitance, but that they are constant. For the IGBT module used in the 3-ϕ inverter, no such parameter data are available. The switching behaviour was therefore measured and the influence of factors like collector current and snubber capacitor values on these parameters was investigated. Where parameters were found to be dependent on any of these factors, the dependency was incorporated into the optimisation procedure.

Accurate high bandwidth measurements of IGBT collector current, without drastically affecting the circuit layout and associated parasitic components, are very difficult to obtain. The dual module packaging of the CM300DU-24F devices further complicates this task. To avoid structural changes to the bus-bars, the experimental setup shown in Figure 4.4 was used. The procedure followed in collector current measurement was to firstly raise the bus voltage to the nominal value and then G_{na} and G_{pb} were switched on. This resulted in linear current growth in L_{load}. The current was monitored with a LEM current sensor and at the desired level G_{na} was switched off. If parasitic capacitances are ignored, the measured pole current of phase A is equal to the collector current of G_{na} until that instant when the pole voltage reaches $+\frac{V_d}{2}$. Diode D_{pa} is then forward biased and takes over the pole current.

Just as in the final layout of the turn-off snubber, it is essential to keep the parasitic inductance of the turn-off snubber loop small. Therefore, the current measuring device has to be as small as possible to avoid long wires or a large snubber structure. Two devices were considered for the current measurement, namely a resistive shunt and a Pearson current monitoring transformer (model 110). The Pearson meter has a bandwidth of 20 MHz and an usable rise time of 20 ns. No data for the resistive shunt were available, except the precise

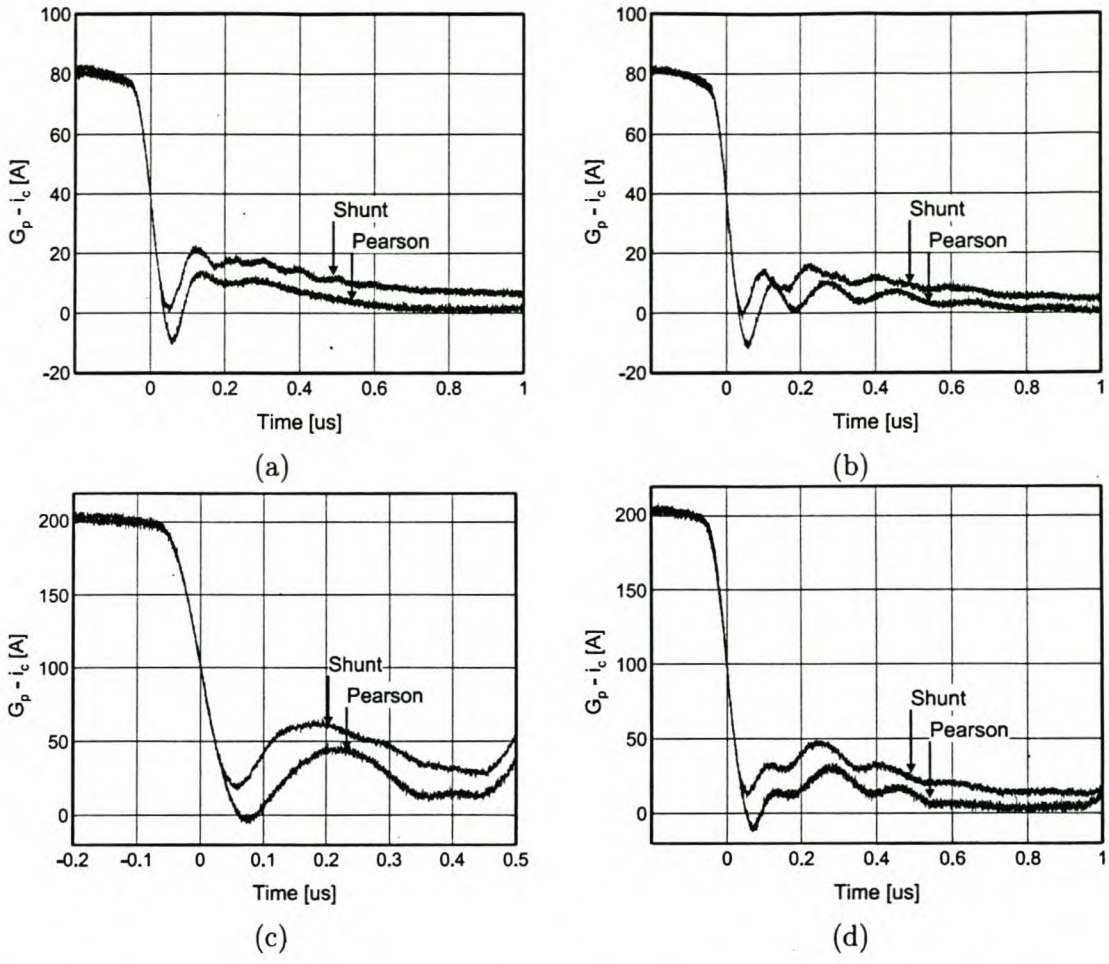


Figure 4.5: Comparisons of current measurements made with a shunt resistor and a Pearson current monitoring transformer: (a) $C_r = 100\,nF$, $I_o = 80\,A$; (b) $C_r = 233\,nF$, $I_o = 80\,A$; (c) $C_r = 100\,nF$, $I_o = 200\,A$; (d) $C_r = 233\,nF$, $I_o = 200\,A$.

resistance value of $2.536\,m\Omega$. However, collector current measurements with the shunt suggest a measuring bandwidth similar to the Pearson meter. Available current transformers and hall effect sensors were too bulky and therefore not used.

In Figure 4.5 the differences between current measurements made by the Pearson meter and the resistive shunt are illustrated. In Figure 4.5a and b the load current is 80 A and in Figure 4.5c and d it is 200 A. For both load currents measurements are shown with $C_r = 100\,nF$ and $C_r = 233\,nF$. It can be seen that the dynamic responses of the two sensors are very similar. It is also clear that the bandwidth achievable with these sensors is not sufficient for precise turn-off current measurements, but only provides limited information on the current fall time, the current tail time and the current tail bump. It is also clear that, for all the cases shown, the shunt measurements have a current offset after the IGBT is completely off. This current

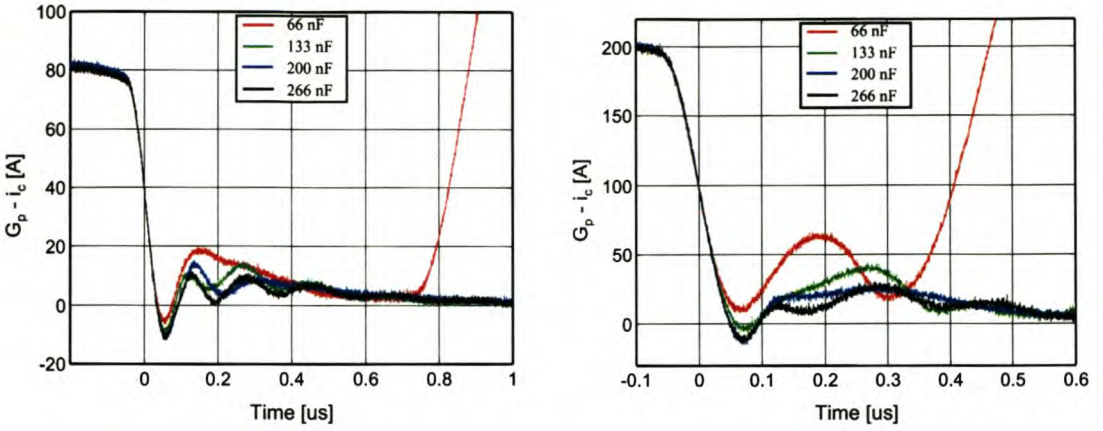


Figure 4.6: The influence of snubber capacitor value on the turn-off behaviour: (a) $I_o = 80\,A$; (b) $I_o = 200\,A$.

offset is not measured by the Pearson meter and it is also substantially larger that what can be attributed to parasitic capacitance charging current. However, given the small signals from the shunt ($2.536\,mV.A^{-1}$) compared to the signal level from the Pearson meter ($100\,mV.A^{-1}$), it can be attributed to measurement offset in the digital oscilloscope and the noise proneness of the shunt measurement. The Pearson meter was therefore primarily used as current sensor.

The dependency of the collector current turn-off waveform on snubber capacitance and current level were measured at currents from 40 A to 240 A with 40 A intervals and with snubber capacitor values of 66 nF to 266 nF with 33 nF intervals. Smaller snubber capacitor values and larger load currents were not used, because for these combinations the period of valid collector current measurement is too small and the measured waveforms have limited value. This problem is illustrated in Figure 4.5c, where the measured current shows a sharp increase at 450 ns. This is the instant when the snubber capacitor voltage reaches $\frac{V_d}{2}$ and D_{pa} takes over the pole current. Therefore, the measured current is only equal to the collector current for the period before this instant.

The influence of the snubber capacitor value on the turn-off switching behaviour is illustrated in Figure 4.6. In Figure 4.6a the turn-off behaviour at various snubber capacitor values with a load current of 80 A is shown, while measurements at the same capacitor values with 200 A load current are shown in Figure 4.6b. Even though the limited bandwidth of the measurements place restrictions on the accuracy of model fitting to these curves, it is clear that especially the tail bump is influenced by the snubber capacitor value. Useful tail current duration dependencies were also observed, but the current fall duration showed very limited variation.

In Figure 4.7 the switching behaviour as function of output current is illustrated. In Figure 4.7a the turn-off behaviour at various load current values with a 166 nF subber capacitor are

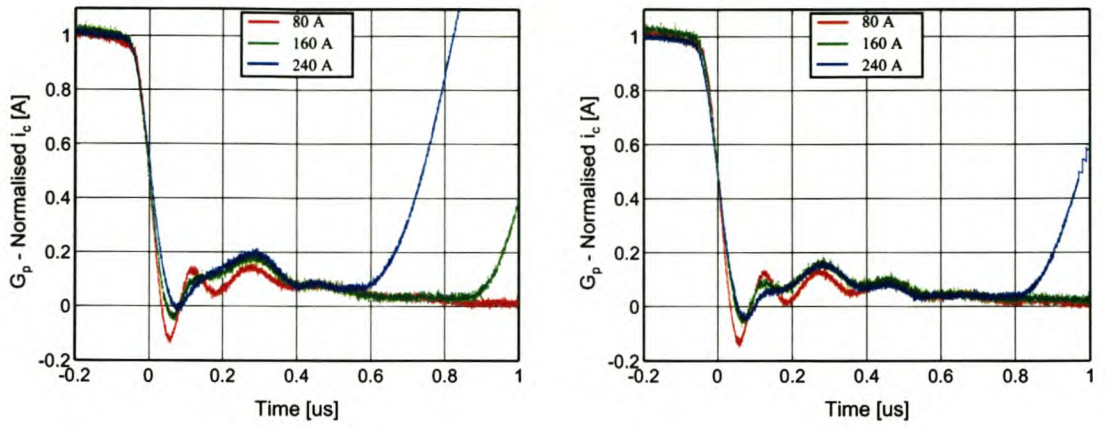


Figure 4.7: The influence of snubber capacitor value on the turn-off behaviour: (a) $C_r = 166\,nF$; (b) $C_r = 233\,nF$.

shown, while measurements at the same current levels with a 233 nF capacitor are shown in Figure 4.7b. Within the limited accuracy of the measurements, no clear and apparent parameter dependencies on current level could be observed.

To quantify the observed dependencies discussed in the previous paragraphs, the piece-wise linear model parameters, best describing the measured curves, had to be determined. On the measured waveforms the current fall slopes are always well defined and the end of the tail current duration could also be obtained fairly accurately. However, this is not enough information to determine the three parameters describing the model. It was therefore necessary to further estimate the slope of the tail current. In Figure 4.8 the fitted curves for snubber capacitor values of 66, 133, 200 and 266 nF are shown. The complete parameter set is shown in Table 4.6.

C_r [nF]	66	100	133	166	200	233	266
A_m	0.21	0.18	0.18	0.15	0.13	0.12	0.1
t_{fim} [ns]	65	67	67	69	68	70	70
t_{tim} [ns]	800	800	850	900	950	1000	1100

Table 4.6: Parameters describing turn-off collector current.

The turn-on collector-emitter voltage waveforms for the IGBT were also measured at different current levels. The obtainable bandwidth with voltage measurements was higher and small variations in parameters were observed. The same procedure as described in the previous paragraph was used to determine these parameter values. Examples of fitted curves are shown in Figure 4.9 and the complete parameter set is given in Table 4.7.

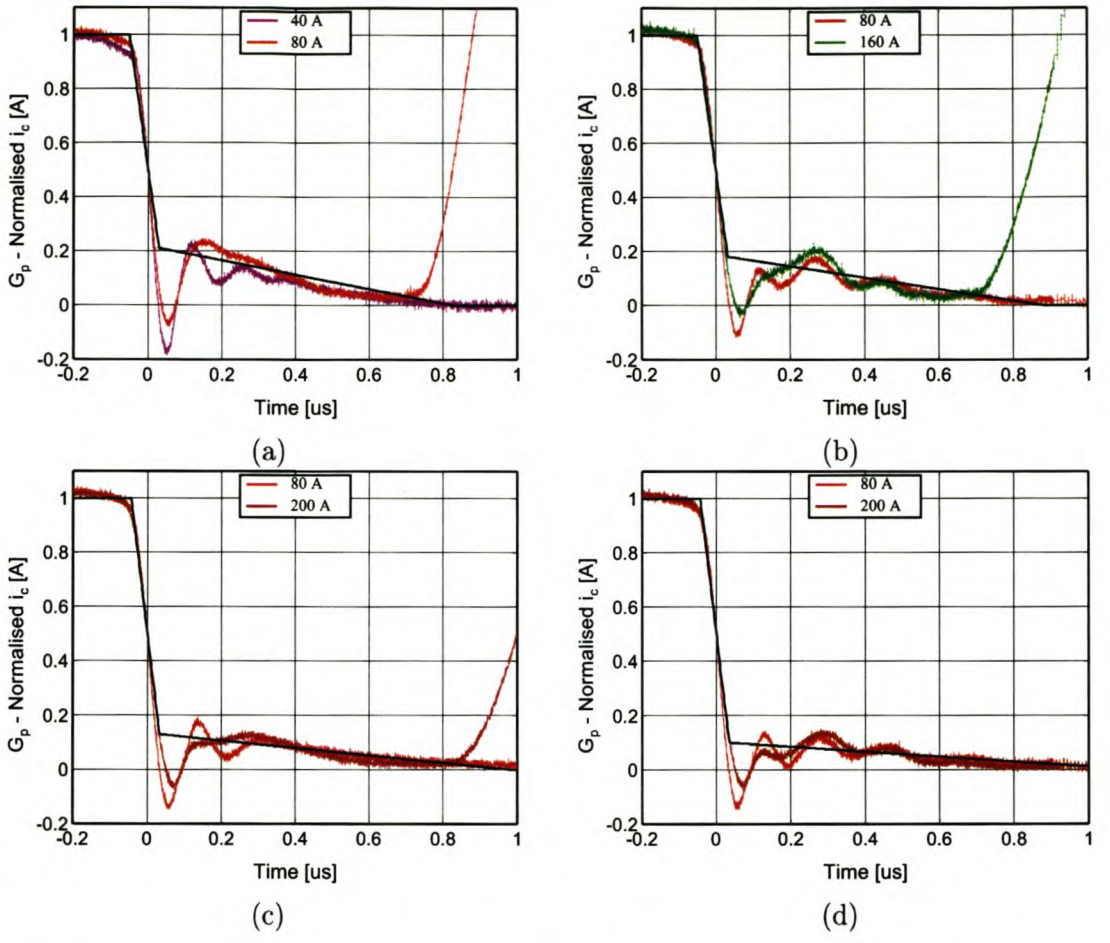


Figure 4.8: Examples of piece-wise linear switching approximations during turn-off: (a) $C_r = 66\,nF$; (b) $C_r = 133\,nF$; (c) $C_r = 200\,nF$; (d) $C_r = 266\,nF$.

4.5.2 Measurement of parasitic bus inductance

To determine the parasitic bus inductance the voltage overshoot during turn-off across a main IGBT, at various output current levels, was measured. During the measurement a good-quality polymer snubber capacitor ($2\mu F$), with low internal inductance, was placed directly across the IGBT. The measured waveforms were then compared to predicted waveforms. These predicted waveforms, at various parasitic bus inductance values, were obtained with the model developed in section 3.8.1. It was found that the best correlation between the measured and predicted waveforms are achieved with a bus inductance value of 40 nH. In Figure 4.10 the correlation at 80 and 240 A are shown.

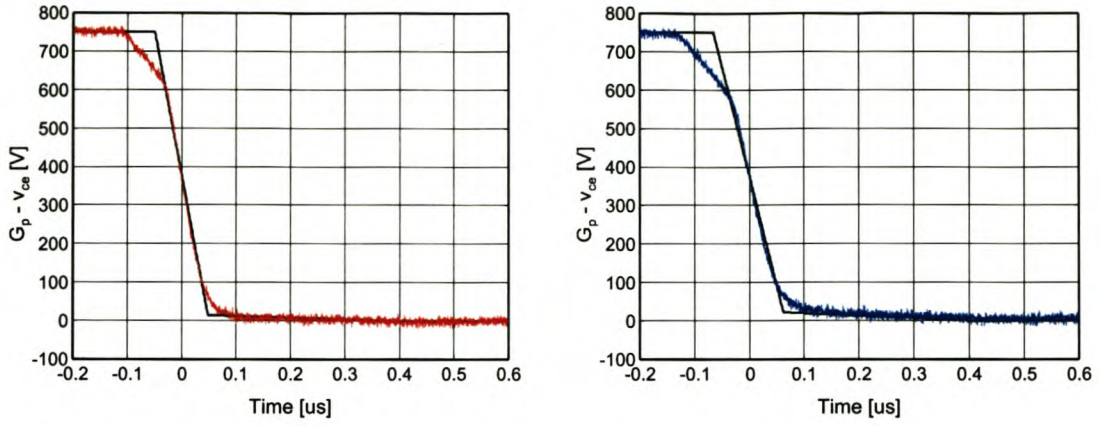


Figure 4.9: Examples of piece-wise linear switching approximations during turn-on: (a) $I_o = 80\,A$; (b) $I_o = 240\,A$.

I_o [A]	40	80	120	160	200	240
B_m	0.02	0.02	0.02	0.02	0.03	0.03
t_{fvm} [ns]	90	98	100	107	117	127
t_{tvm} [ns]	300	350	350	350	350	350

Table 4.7: Parameters describing turn-on collector-emitter voltage.

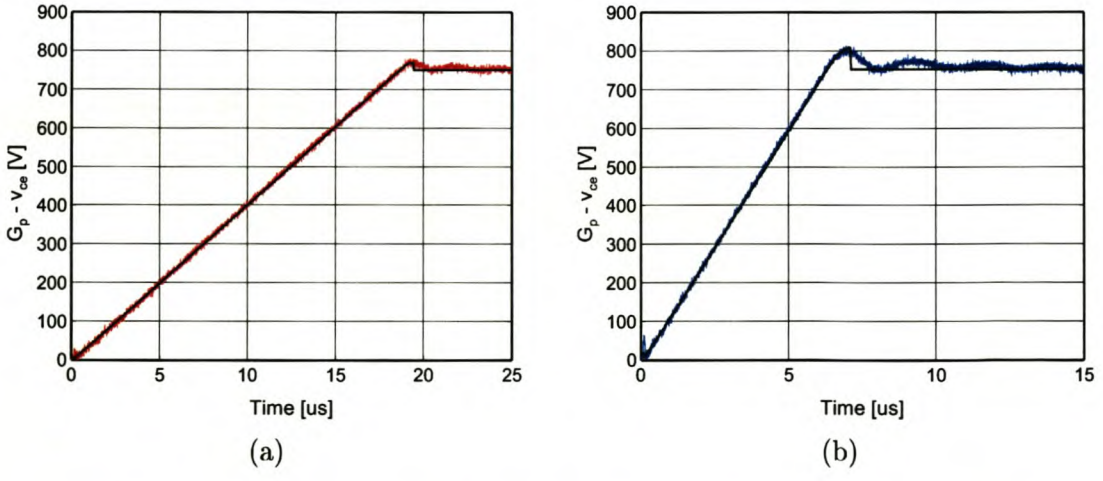


Figure 4.10: Comparison between predicted voltage overshoot at turn-off with a leakage bus inductance of $L_{bpp} = 40\,nF$ and measured voltage overshoot: (a) $I_o = 80\,A$; (b) $I_o = 240\,A$.

4.5.3 Choice of snubber components

The choice of snubber components used to implement the turn-off snubber modules will be briefly discussed.

1. **Auxiliary switches.** The auxiliary switches were once again implemented as an IGBT in series with a blocking diode. This choice ensures fast and easily controllable auxiliary switches. As in the construction of the snubbers for the single-phase systems, the 1MBH60D-090A IGBT from Fuji, together with the DSEI60 diode from IXYS, was used. The parameters of these components were shown in Table 3.7. The peak allowable current in the auxiliary switch was chosen as 75 A. This is less than a third of the maximum output current. Compared to the single-phase experimental inverters, the auxiliary IGBT and blocking diode are also better utilised.

2. **Snubber capacitors.** The R76 KP series film-foil polypropylene capacitors from Arcotronics were selected as snubber capacitors. The choice is based on the low cost and the relatively high peak current rating of these capacitors. At the desired voltage level the highest value capacitor obtainable was 100 nF. The snubber capacitors will therefore be implemented with a number of these components in parallel. The maximum $\frac{dv}{dt}$ is given as 1600 V.μs^{-1}. This implies a peak current of 160 A per capacitor. It is therefore important that at least two of these capacitors should be used to implement a specific snubber capacitor in order to handle the maximum output current. Capacitors from the R73 KP series, which were used for the single-phase inverters, were not considered for the three-phase system. Although this series has superior current-handling capabilities, the obtainable values are smaller and a large number of component are necessary to obtain the desired value. This complicates the snubber structure and increase the parasitic inductance.

   The dissipation factor of a capacitor is strongly dependent on the operating temperature and frequency of operation. Therefore estimates of these operating parameters have to be made in order to determine a realistic ESR coefficient. Preliminary optimisation results, which neglected the ESR of passive auxiliary components, suggested that a typical resonance frequency will be in the order of 75 kHz. An operating temperature of not more than 40℃ was also assumed, because of the effective water-cooling methods used in the three-phase system. The dissipation factor at this frequency and temperature corresponds to an ESR of approximately 60 $\mu\Omega$ and a $k_{R_{C_r}}$ of 6x10^{-12} ΩF. These parameters are summarised in Table 4.8.

3. **Snubber diodes.** The SEMIKRON SKR48F12 was again selected as snubber diode. This diode showed good reverse recovery characteristics when it was used in the experimental single-phase inverters and has a high enough peak current capability to support the maximum output current of the three-phase system. The parameters of this diode were shown in Table 3.7.

4. **Resonant discharge inductors.** As in the single-phase systems, the P30/19 ferrite

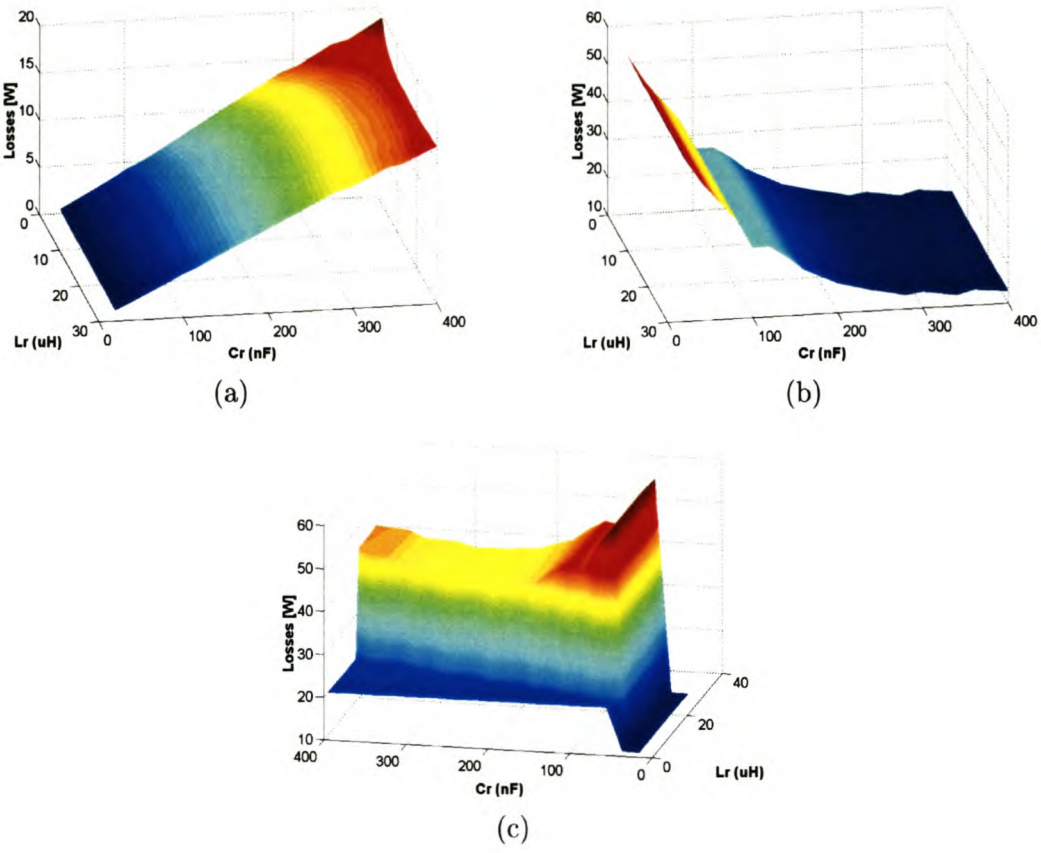


Figure 4.11: Optimisation results for experimental 3-ϕ inverter: (a) Losses in auxiliary switches and passive snubber components; (b) Main IGBT turn-off losses; (c) Total losses.

core shape was used to implement the resonant discharge inductors. The same Philips 3F3 material was also used due the good performance factor at high frequencies. With respect to peak flux density, copper fill factor and isolation, an identical design philosophy was followed. In equations 3.105, 3.106 and 3.107 the expressions given in equations 3.98, 3.101 and 3.103 were rewritten for the specific core shape, ferrite material and copper fill factor. The same procedure for core loss estimations were also followed. In Table 4.8 the resonant inductor parameters are summarised.

4.5.4 Optimisation results

The optimisation procedure developed in section 3.6, with the additions and modification described in section 4.3, was used to determine the optimal snubber component values. The results of this modified optimisation procedure are shown in Figure 4.11. In Figure 4.11a the losses in the auxiliary switches and passive snubber components are illustrated and in Figure

Snubber Capacitor (Acrotronics R76)		
Capacitance	C_r	2 x 100 nF
ESR Coefficient	$k_{R_{C_r}}$	$6x10^{-12}\,\Omega F$
Resonant Inductor (P30 3F3 Core)		
Inductance	L_r	15 μH
Copper Resistance	R_{L_r}	23 mΩ
Peak Current	$I_{r(max)}$	75 A

Table 4.8: Parameters for the auxiliary components in the experimental 3-ϕ inverter.

4.11b the main IGBT turn-off losses are shown. The discontinuous variation of the turn-off switching parameters as function of the snubber capacitor value is clearly illustrated by the uneven nature of this graph. The total losses in a soft-switching phase arm are shown in Figure 4.11c. In this figure the dark blue areas correspond to snubber component combinations that result in excessive voltage overshoot, auxiliary switch current or snubber capacitor discharge time.

The combinations of snubber components that result in the lowest overall losses are $L_r = 16\,\mu H$ and $C_r = 280\,nF$. Due to the limited space available between modules and the disadvantages of having a large snubber structure, it was decides to limit the snubber capacitor value to 200 nF. The values for the resonant inductors were practical and no changes were made. After the construction of these inductors their values were measured and found to be marginally smaller at around $L_r = 15\,\mu H$. The snubber component combination that was implemented will result in around 1.6% more effective switching losses that the optimal combination. Table 4.8 gives a summary of the snubber component parameters.

In Figure 4.12 the constructed snubber modules are shown. Two PCBs per phase were used. In Figure 4.12a the first PCB with the auxiliary switches and their drivers is shown, while the second PCB with the snubber capacitors, snubber diodes and resonant inductors is shown in Figure 4.12b. The first PCB is mounted on top of the second one, while the latter is directly connected to the terminals of the main IGBT module.

4.6 Experimental results

In this section waveforms obtained from the experimental 3-ϕ inverter will be discussed and compared to theoretical models. The main IGBT turn-off cycle, turn-on cycle and the capacitor discharge cycle will be treated. This will be followed by comparisons between measured and predicted losses in the inverter. In Figure 4.13 the experimental setup is shown.

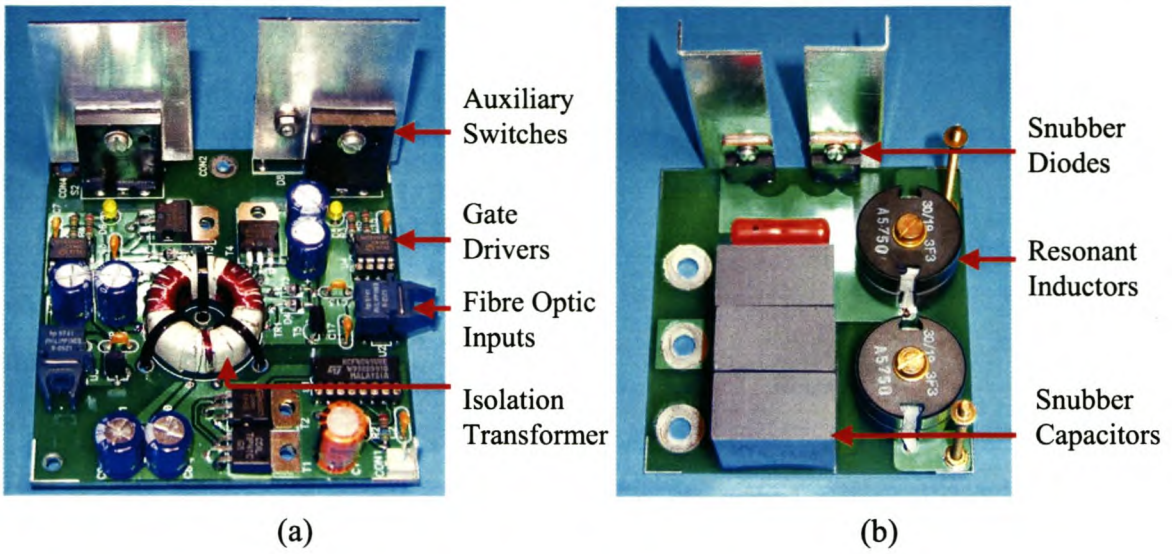


Figure 4.12: (a) Auxiliary switches with drivers and isolated power supplies; (b) Snubber capacitors, snubber diodes and resonant inductors.

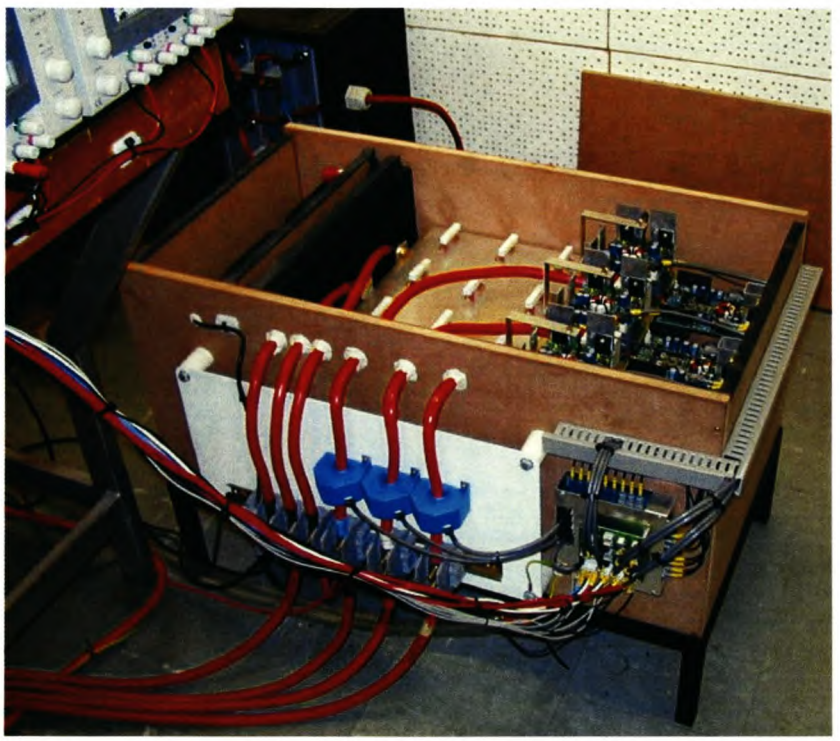


Figure 4.13: Experimental inverter inside wooden container.

4.6.1 Main IGBT turn-off

In this section measured main IGBT turn-off waveforms, obtained form the experimental 3-ϕ soft-switching inverter, will be compared to theoretical models. The model developed in section 3.8.1 (model 2) will be used for this purpose.

In Figure 4.14 measured waveforms at turn-off are compared to the model. Measured and predicted v_{ce} waveforms are shown for output currents of 60, 120, 180 and 240 A. A summary of the parasitic component values used in the model is given in Table 4.9. The correlation between the measured waveforms and the predictions are generally good. As in the case of the single-phase inverter fitted with the combined snubber, the periods where the greatest differences between predicted and measured waveforms occur are during the collector current turn-off time and during the snubber diode reverse recovery. For the first period the inaccuracies can mainly be attributed to the approximation current model. This is especially clear at t_0 and t_{fim} where the piece-wise linear model predicts discontinuous waveforms. This stands in contrast to the gradual transitions of the measured waveforms. For the resonance and diode reverse recovery period, the main differences are the smoother measured reverse recovery behaviour and the marginally shorter resonance period of the measured waveform. The approximate linear current model used at the end of the reverse recovery period is once again the cause of the discontinuous predicted waveform during this period.

4.6.2 Main IGBT turn-on

In section 3.8.2, where the main IGBT turn-on cycle of the combined snubber topology is described, it was shown that C_{rp} and C_{rn} have a steady voltage build-up during large negative and positive output current respectively. This was due to energy trapped in the bus inductors as a result of the free-wheeling diode reverse recovery current. Therefore, to prevent dangerous snubber voltage levels, it was necessary to add bleeding resistors to the snubber capacitor banks.

Even though the current topology does not have added bus inductors, the parasitic inductance may cause similar charge build-up. To investigate this, $v_{C_{rp}}$ of one phase was measured **over a fundamental modulation** cycle. In Figure 4.15a the waveform can be seen. The corresponding output current of the phase is shown in Figure 4.15b. During large positive output current the charging and discharging of the snubber capacitor are clearly visible. During negative output current, the snubber capacitor voltage remains constant at about 30 V above the bus voltage. Therefore, Figure 4.15a clearly illustrates that the energy trapped in the parasitic bus inductance is not sufficient to cause dangerous charge build-up and that no precautionary measures are necessary.

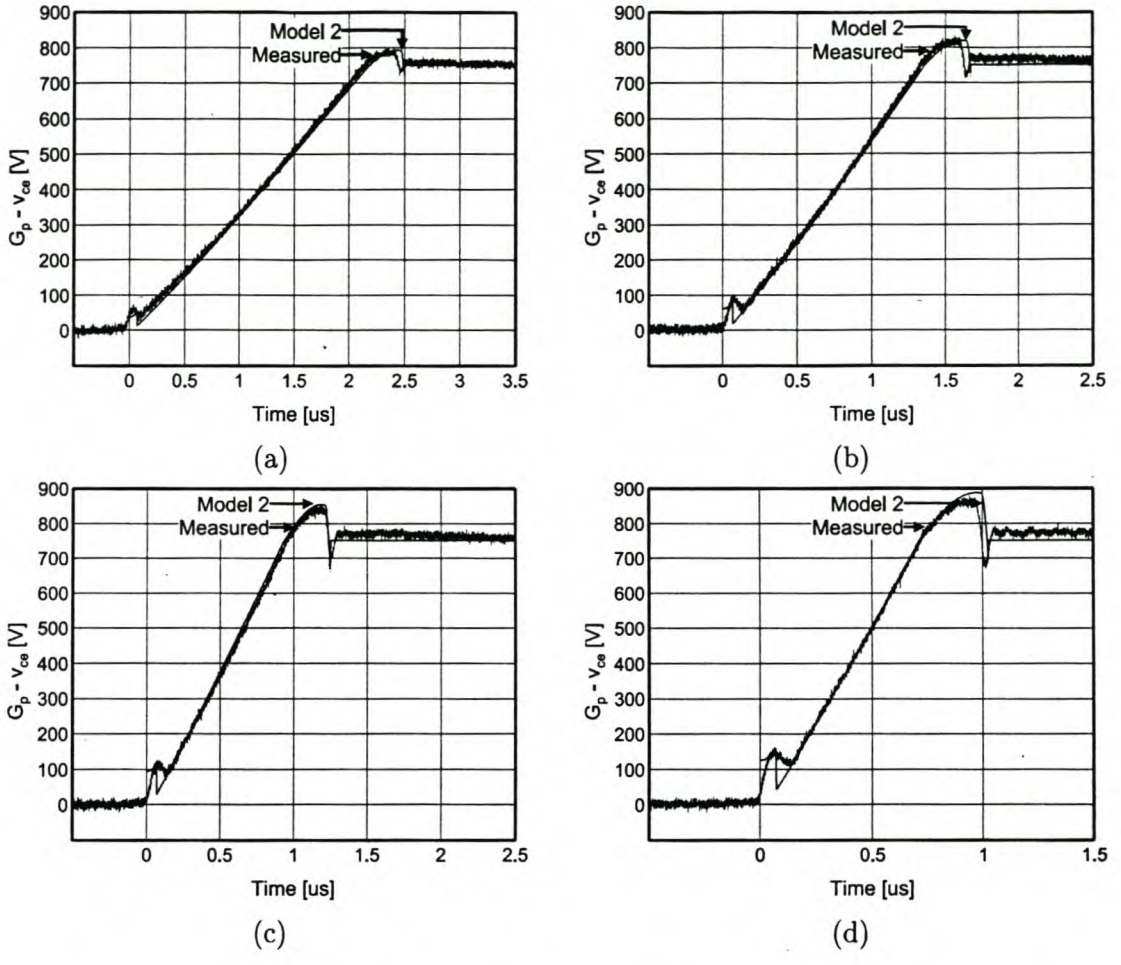


Figure 4.14: Comparisons between predicted and measured waveforms at main IGBT turn-off: (a) $I_o = 60\,A$; (b) $I_o = 120\,A$; (c) $I_o = 180\,A$; (d) $I_o = 240\,A$.

4.6.3 Capacitor discharge

In Figure 4.16 the measured and predicted capacitor discharge waveforms are shown. Both the resonant inductor current and the snubber capacitor voltage are displayed. The correlation between the predicted and measured snubber capacitor voltage is very good, except for the reverse recovery period of the auxiliary switch that starts at around $4.3\,\mu s$. No provision for auxiliary switch reverse recovery was made in the model developed in section 3.8.3 due to the relatively low $\frac{di}{dt}$ experienced by the switch. The measured inductor current also corresponds fairly well, although the signal is very noisy. This can be attributed to high $\frac{dv}{dt}$s in the inverter during this period as a result of the main IGBT turn-on cycle.

Table 4.9 shows a summary of the parasitic components in the three-phase inverter. The on-state voltage and resistance of the main IGBTs and free-wheeling diodes are also given. Table 3.7 and Table 4.8 list similar parameters for the auxiliary components. The values shown in

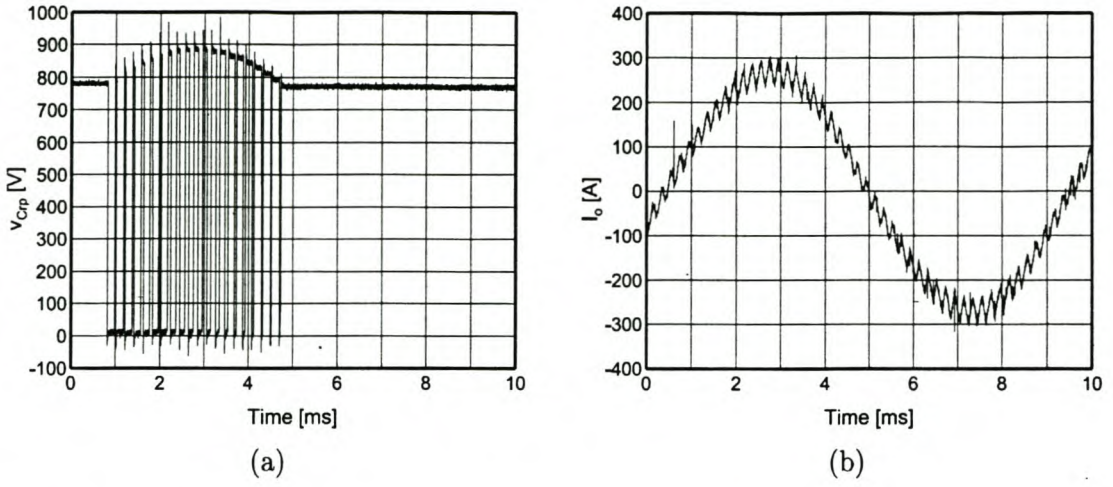


Figure 4.15: Snubber capacitor voltage (a) and output current (b) over a fundamental switching cycle.

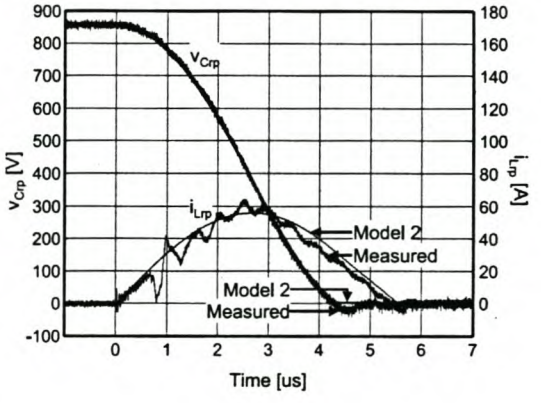


Figure 4.16: Comparison of predicted and measured waveforms for the snubber capacitor discharge cycle ($I_o = 120\,A$).

Bus-Bar Parasitic Inductance	L_{bpp}, L_{bnp}	40 nH
Bus-Bar Parasitic Resistance	R_{bpp}, R_{bnp}	1 mΩ
Module Stray Inductance	L_{mp}, L_{mn}	15 nH
Snubber Stray Inductance	L_{spp}	40 nH
Main IGBT On-State Voltage	$V_{G_p(on)}$	1.2 V
Main IGBT On-State Resistance	R_{G_p}	2 mΩ
Free-Wheeling Diode On-State Voltage	$V_{D_n(on)}$	1 V
Free-Wheeling Diode On-State Resistance	R_{D_n}	4 mΩ

Table 4.9: Summary of parasitic component values and on-state parameters for the main IGBTs used in the experimental 3-ϕ inverter.

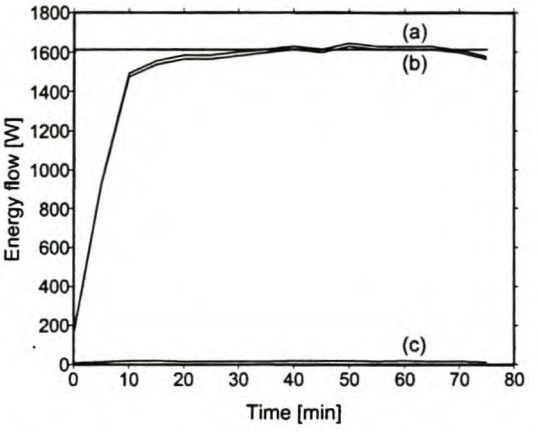


Figure 4.17: Energy flow out of the inverter container during a hard-switching measurement: (a) Total energy flow; (b) Energy flow due to water temperature increase; (c) Energy flow due to thermal conduction.

Table 4.9 were mostly obtained from component data sheets, while the parasitic bus inductance was indirectly measured. This process was described in section 4.5.2. Similar measurements were performed to obtain estimates for L_{spp} and R_{bpp}.

4.6.4 Efficiency measurements

The total inverter losses were measured at operating conditions specified in Table 4.3. A calorimetric technique, as described in sections 2.7.1 and 3.8.4, was again used for this purpose. The implementation of the wooden enclosures and water-cooling mechanisms necessary for this technique was discussed in section 4.4.4. The thermal resistance of the container was measured as $6\,WK^{-1}$.

A typical loss measurement is show in Figure 4.17. For this specific case the inverter was operated under normal hard-switching conditions. Illustrated in Figure 4.17 is the total energy flow out of the wooden container as a function of time. The total flow is also separated into contributions made by thermal conduction and water temperature increase. The thermal time constant (τ_s) of the system is approximately 6 minutes. The total measuring period of 75 minutes ($12.5\,\tau_s$) is therefore sufficient to ensure thermal equilibrium. It is also clear from Figure 4.17 that the contribution of heat loss through the walls of the container is minimal. This is the result of the effective water cooling that kept the air temperature inside the container to less than 5 K above the ambient temperature.

In Table 4.10 the results of the loss measurements are compared to the losses predicted by the optimisation procedure. The values for measured losses were obtained by averaging the results of at least three 75-minute measurements. The main IGBT turn-on and conduction losses, as well as the free-wheeling diode losses, were directly obtained from data sheet values.

	Modulation	
	Hard-Switching	**Soft-Switching**
Calculated Losses [W]		
Main IGBT Turn-off Losses	358	68
Main IGBT Turn-on Losses	239	239
Main IGBT Conduction Losses	398	398
Free-wheeling Diode Losses	392	392
Snubber Circuit Losses	0	27
Fans	76	76
Auxiliary Circuitry	16	20
Sharing Resistors	51	51
DC Bus Capacitor Losses	135	135
Total	1665	1406
Measured Losses [W]		
Total	1586	1372

Table 4.10: Theoretical and measured converter losses under normal PWM operation.

For the hard-switching case the main IGBT turn-off losses were also obtained from device data sheets. The approximate bus capacitor losses were obtained from PSpice simulations.

The measured and the predicted losses correspond well, with a maximum difference of approximately 5%. For both cases the measured losses are also slightly less than the predicted losses. The measurements suggest that the reduction in main IGBT turn-off losses is 68.4%, while the reduction in effective turn-off losses is 59.8%. The measured turn-off losses are substantially higher than what is predicted by the optimisation procedure, illustrating the negative influence parasitic components have on the effectiveness of the snubber.

4.7 Conclusion

In this chapter the development of a high-power, soft-switching, 3-ϕ IGBT inverter was described. To determine the most suitable soft-switching topology for a practical three-phase inverter, the active resonant turn-off snubber was compared to the combined snubber with respect to effectiveness, complexity, cost and protection schemes. The turn-off snubber topology was selected because of the simple and reliable protection schemes and the ability to integrate the snubber with standard IPMs. As a first step towards the soft-switching inverter, the design of a 100 kVA hard-switching inverter was described. Special emphasis was placed on practical operating conditions and construction that suits calorimetric loss measurement. A snubber module that can be easily added to the hard-switching inverter was subsequently developed. To determine optimal snubber component values, the optimisation procedure developed in the pre-

vious chapter was further refined and adapted for the turn-off snubber topology. Refinements included main IGBT turn-off waveform parameters that are dependent on snubber capacitor size. After construction, measured waveforms taken during the main IGBT turn-off cycle and the capacitor discharge cycle were compared to theoretical models. The total inverter losses were also measured. It was shown that the snubber can reduce the effective turn-off losses by 59.8% and the overall effective switching losses by 35.8%.

Chapter 5

Summary and conclusions

In this final chapter the contents of the thesis will be briefly summarised. The major contributions and conclusions of the study will be outlined and possible further studies on the topic will be identified.

5.1 Contributions and conclusions

1. In Chapter 1 soft-switching topologies were classified and examples of the different classes were given. Basic operation principles of these topologies were described and the advantages and disadvantages of each class were discussed. It was clear that all of these topologies alleviate some problems associated with hard-switching inverters, but at the expense of complexity, extra control requirements and in some cases extra current and voltage stresses on the main devices.

2. Chapter 2 dealt with the active resonant turn-off snubber. This topology, which is based on the ARCP inverter, was introduced by Prof. H. du T. Mouton. The main advantage of this snubber is the low ratings of the auxiliary switches compared to those of the main devices. The following aspects were looked at:

   (a) The basic operation theory, as derived by Prof. H. du T. Mouton, was verified and used to describe the operation principles of the topology.

   (b) An evaluation of various operation strategies, which can be used to avoid high peak currents in the snubber topology during low output current conditions, were carried out. It was concluded that discontinuous snubber operation provides a simple and effective way to avoid this problem.

   (c) Protection strategies for the main IGBTs and auxiliary switches were developed. It was shown that no extra protection for the main IGBTs is necessary and that the auxiliary switches can be effectively protected with standard techniques.

(d) An experimental 40 kVA single-phase inverter, fitted with a turn-off snubber, was constructed. A calorimetric technique was used to measure inverter losses with and without the turn-off snubber. Measurements suggest that the effective reduction in turn-off losses with normal PWM modulation was 63%.

3. In Chapter 3 the integration of a turn-on snubber with the standard turn-off snubber was investigated. Extra bus inductance was added to limit current rise at turn-on and therefore to reduce turn-on losses. The major disadvantage of this combined snubber is, however, the extra voltage stresses introduced on the main devices. The following aspects were dealt with:

   (a) Basic operation theory was derived and used to demonstrate the operation principles. It was clear that special control methods for the snubber are necessary to avoid large peak currents and excessive voltage overshoot during small output current operation.

   (b) Various operation strategies for the combined snubber were investigated. It was shown that both discontinuous snubber operation and a uni-directional charge assistance strategy are effective ways to deal with small output current conditions. Both strategies were also proven experimentally.

   (c) Protection strategies for the combined snubber were evaluated. Although the protection of the auxiliary switches can be handled in the same way as for the turn-off snubber, effective protection of the main devices requires special techniques that are not compatible with standard IPMs.

   (d) Analytical expressions describing the losses in the combined snubber topology, as function of snubber component values, were derived. Simple tail-forming switching behaviour for the main and auxiliary devices was assumed and parasitic components were neglected.

   (e) The loss expressions were used as the basis of an optimisation procedure. The aim of the procedure is to determine the combination of snubber component values that will result in the lowest overall losses in a specific inverter.

   (f) An experimental 20 kVA single-phase inverter, fitted with a combined snubber, was designed and constructed. The developed optimisation procedure was used to determine optimal snubber component values.

   (g) The operation theory of the topology was further refined to include the effects of parasitic components and diode reverse recovery. Similar to the detrimental effects parasitic inductance has on the turn-off snubber, it was shown that the efficiency of the turn-on snubber is compromised by the reverse recovery of the free-wheeling diodes.

(h) Correlations between measured and predicted turn-off, turn-on and snubber capacitor discharge waveforms were good. Minor differences can be attributed to inaccuracies in the simple tail-forming switching model and the approximate diode reverse recovery modeling.

(i) A calorimetric technique was used to measure the losses in the experimental inverter with and without the snubber. Measurements suggest a 48% reduction in main IGBT switching losses and a reduction of 41% in the effective switching losses.

4. The design of a three-phase, soft-switching inverter was undertaken in Chapter 4. Emphasis was placed on practical operation conditions and good utilisation of main devices. The following aspects were looked at:

   (a) The turn-off and combined snubber topologies were compared with respect to effectiveness, complexity, cost and protection to determine the most suitable topology. The turn-off snubber was selected due to effective protection methods and easy integration with standard hard-switching inverters.

   (b) As a first step towards the soft-switching inverter, a standard hard-switching three-phase inverter was designed and constructed. Emphasis was placed on ways to facilitate the calorimetric loss measurement technique.

   (c) The optimisation procedure developed in the previous chapter was refined to incorporate snubber component and output current level dependent switching models.

   (d) The revised optimisation procedure was used to design turn-off snubbers that can be easily fitted to the constructed hard-switching inverter.

   (e) Measured waveforms taken after the implementation of the complete soft-switching inverter showed good correlation with predicted waveforms.

   (f) The results obtained from the calorimetric loss measurements correspond well with predicted losses with a maximum difference of 5%. The measurements suggest a reduction in turn-off losses of 68.4% and a reduction in effective turn-off losses of 59.8%. The effective reduction in the overall switching losses was 35.8%.

5. In general the reduction in switching losses achieved with the experimental inverters were not sufficient to make the topologies more attractive than hard-switching inverters. The extra complexity and cost do not, in general, justify the use of any of the two topologies. In special applications where EMI and size constraints are critical, however, the topologies can be valuable.

5.2 Future work

1. The possibility of topology simplification for a three-phase combined snubber can be investigated and experimentally verified. A detailed study on the effects of free-wheeling diode reverse recovery in the combined snubber topology can also be undertaken in an attempt to minimise the negative effects this has on the efficiency of the snubber.

2. Snubber integration with main devices and an investigation into construction and layout methods to minimise parasitic inductance can be undertaken to maximise the efficiency of the turn-off snubber.

3. Detailed EMI studies on the two snubber topologies can be carried out to quantify the EMI benefits.

4. The applicability of the turn-off snubber to the isolated high-frequency half-bridge dc-dc converter topology should be investigated.

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Appendix A

Expressions for losses in combined snubber.

A.1 Main IGBT turn-off

$\underline{0 \leq t < t_1}$

The losses in L_{bp}, G_p, C_{rp} and D_{rp}, for all the cases, are given by

$$\begin{aligned} W_{Lbp} &= \int_0^{t_1} i_{bp}^2 R_{Lb} dt \\ &= I_o^2 R_{Lb} t_{fim} \end{aligned} \tag{A.1}$$

$$\begin{aligned} W_{Gp} &= \int_0^{t_1} i_{c_{(G_p)}} v_{Crp(a)} dt \\ &= \frac{I_o^2 (1 - A_m) t_{fim}^2}{6C_r} - \frac{I_o^2 (1 - A_m)^2 t_{fim}^2}{8C_r} \end{aligned} \tag{A.2}$$

$$\begin{aligned} W_{Crp} &= \int_0^{t_1} i_{Crp(a)}^2 R_{Cr} dt \\ &= \frac{I_o^2 (1 - A_m)^2 t_{fim} R_{Cr}}{3} \end{aligned} \tag{A.3}$$

$$\begin{aligned} W_{Drp} &= \int_0^{t_1} i_{Crp(a)}^2 R_{Dr} dt + \int_0^{t_1} i_{Crp(a)} V_{Dr(on)} dt \\ &= \frac{I_o^2 (1 - A_m)^2 t_{fim} R_{Dr}}{3} + \frac{I_o (1 - A_m) t_{fim} V_{Dr(on)}}{2}. \end{aligned} \tag{A.4}$$

$\underline{t_1 \leq t < t_2}$

For case 3 the losses in L_{bp}, G_p, C_{rp} and D_{rp} are given by

$$\begin{aligned} W_{Lbp} &= \int_{t_1}^{t_2} I_o^2 R_{Lb} dt \\ &= I_o^2 R_{Lb} t_{tim} \end{aligned} \tag{A.5}$$

$$\begin{aligned} W_{Gp} &= \int_{t_1}^{t_2} i_{Gp} v_{Crp(b)} dt \\ &= \frac{I_o t_{tim} A_m \left(12 v_{Crp(b)}(t_1) C_r + 4 I_o t_{tim} - 3 I_o t_{tim} A_m\right)}{24 C_r} \end{aligned} \tag{A.6}$$

$$\begin{aligned} W_{Crp} &= \int_{t_1}^{t_2} i_{Crp(b)}^2 R_{Cr} dt \\ &= \frac{I_o^2 R_{Cr} t_{tim} \left(A_m^2 - 3A_m + 3\right)}{3} \end{aligned} \tag{A.7}$$

$$\begin{aligned} W_{Drp} &= \int_{t_1}^{t_2} i_{Crp(b)}^2 R_{Dr} dt \\ &= \frac{I_o t_{tim} \left(I_o R_{Drp} \left(2A_m^2 - 6A_m + 6\right) - 3A_m V_{Dr(on)} + 6V_{Dr(on)}\right)}{6} \end{aligned} \tag{A.8}$$

For cases 1 and 2 the losses in L_{bp}, L_{bn}, G_p, C_{rp} and D_{rp} for this time interval are

$$\begin{aligned} W_{Lb} &= \int_{t_1}^{t_{vr}} I_o^2 R_{Lb} dt + \int_{t_{vr}}^{t_{cz}} i_{bp}^2 R_{Lb} dt + \int_{t_{cz}}^{t_2} i_{bp}^2 R_{Lb} dt \\ &= \frac{R_{Lb}}{6t_{tim}^2 \omega_1^2} \left(3t_{tim}^2 \omega_1^2 \left(\left(c_1^2 - c_2^2\right) \cos\omega_1 \left(t_{cz} - t_{vr}\right) \sin\omega_1 \left(t_{cz} - t_{vr}\right) + \left(c_1^2 + c_2^2\right)\right.\right. \\ &\quad \left.\left(t_{cz} - t_{vr}\right)\right) + 12c_1 I_o A_m t_{tim} \left(\omega_1 \sin\omega_1 \left(t_{cz} - t_{vr}\right) \left(t_2 - t_{cz}\right) - \right. \\ &\quad \left.\cos\omega_1 \left(t_{cz} - t_{vr}\right) + 1\right) - 12c_2 I_o A_m t_{tim} \left(\sin\omega_1 \left(t_{cz} - t_{vr}\right) + \omega_1 \left(t_2 - t_{cz}\right)\right) \\ &\quad \left(\cos\omega_1 \left(t_{cz} - t_{vr}\right) - 1\right) + 6c_1 c_2 t_{tim}^2 \omega_1 \left(1 - \cos^2\omega_1 \left(t_{cz} - t_{vr}\right)\right) + \\ &\quad \left.6I_o^2 \omega_1^2 t_{tim}^2 \left(t_{vr} - t_{fim}\right) + 2A_m^2 I_o^2 \omega_1^2 \left(t_2 - t_{vr}\right)^3\right) \end{aligned} \tag{A.9}$$

$$\begin{aligned} W_{Ln} &= \int_{t_{vr}}^{t_{cz}} i_{bn}^2 R_{Lb} dt + \int_{t_{cz}}^{t_2} I_o^2 R_{Lb} dt \\ &= \frac{R_{Lb}}{6t_{tim}^2 \omega_1^2} \left(2I_o^2 A_m^2 \omega_1^2 \left(t_2 - t_{vr}\right)^3 - 6I_o^2 A_m \omega_1^2 t_{tim} \left(t_2 - t_{vr}\right)^2 + \right. \\ &\quad 6I_o^2 \omega_1^2 t_{tim}^2 \left(t_2 - t_{vr}\right) + 12c_2 I_o t_{tim}^2 \omega_1 \left(\cos\omega_1 \left(t_{cz} - t_{vr}\right) - 1\right) + 12c_2 I_o A_m t_{tim} \\ &\quad \left(\omega_1 \left(t_2 - t_{vr}\right) + \omega_1 \cos\omega_1 \left(t_{cz} - t_{vr}\right) \left(t_{cz} - t_2\right) - \right. \\ &\quad \left.\sin\omega_1 \left(t_{cz} - t_{vr}\right)\right) + 3t_{tim}^2 \omega_1^2 \left(c_1^2 + c_2^2\right) \left(t_{cz} - t_{vr}\right) \\ &\quad + 3t_{tim}^2 \omega_1 \left(c_1^2 - c_2^2\right) \cos\omega_1 \left(t_{cz} - t_{vr}\right) \sin\omega_1 \left(t_{cz} - t_{vr}\right) + 12c_1 I_o A_m t_{tim} \\ &\quad \left(\omega_1 \sin\omega_1 \left(t_{cz} - t_{vr}\right) \left(t_2 - t_{cz}\right) - \cos\omega_1 \left(t_{cz} - t_{vr}\right) + 1\right) - 6c_1 c_2 t_{tim}^2 \omega_1 \\ &\quad \left.\left(\cos^2\omega_1 \left(t_{cz} - t_{vr}\right) - 1\right) - 12c_1 I_o t_{tim}^2 \omega_1 \sin\omega_1 \left(t_{cz} - t_{vr}\right)\right) \end{aligned} \tag{A.10}$$

$$\begin{aligned} W_{Gp} &= \int_{t_1}^{t_{vr}} i_{Gp} v_{Crp(c)} dt + \int_{t_{vr}}^{t_{cz}} i_{Gp} v_{Crp(c)} dt + \int_{t_{cz}}^{t_2} i_{Gp} \left(V_d + 2\frac{L_b A_m I_o}{t_{tim}}\right) dt \\ &= \frac{A_m I_o}{24t_{tim}^2 C_r \omega_1^3} \left(24c_2 t_{tim} \left(\cos\omega_1 \left(t_{cz} - t_{vr}\right) - \omega_1 \sin\omega_1 \left(t_{cz} - t_{vr}\right) \left(t_2 - t_{cz}\right) - 1\right) + \right. \\ &\quad 24c_1 t_{tim} \left(\omega_1 \cos\omega_1 \left(t_{cz} - t_{vr}\right) \left(t_{cz} - t_2\right) + \omega_1 \left(t_2 - t_{vr}\right) - \sin\omega_1 \left(t_{cz} - t_{vr}\right)\right) + \\ &\quad 24C_r \omega_1^3 L_b A_m I_o \left(t_2 - t_{cz}\right)^2 + 12C_r \omega_1^3 V_d t_{tim} \left(t_2 - t_{vr}\right)^2 + 12c_2 \omega_1^2 t_{tim} \left(t_{cz} - t_{vr}\right) \\ &\quad \left(2t_2 - t_{cz} - t_{vr}\right) - 3\omega_1^3 I_o A_m \left(t_{fim} - t_{vr}\right)^2 \left(2t_{tim} + t_{fim} - t_{vr}\right)^2 - \\ &\quad 12\omega_1^3 v_{Crp(b)}(t_{vr}) C_r t_{tim} \left(t_{fim} - t_{vr}\right) \left(2t_{tim} + t_{fim} - t_{vr}\right) + 4\omega_1^3 I_o t_{tim} \left(6t_{fim} t_{vr}^2 - \right. \\ &\quad \left.\left.6t_{fim}^2 t_{vr} - 6t_{tim} t_{fim} t_{vr} + 3t_{tim} t_{vr}^2 + 3t_{tim} t_{fim}^2 - 2t_{vr}^3 + 2t_{fim}^3\right)\right) \end{aligned} \tag{A.11}$$

$$
\begin{aligned}
W_{Crp} &= \int_{t_1}^{t_{vr}} i_{Crp(c)}^2 R_{Cr} dt + \int_{t_{vr}}^{t_{cz}} i_{Crp(c)}^2 R_{Cr} dt \\
&= \frac{R_{Cr}}{6t_{tim}^2\omega_1}\Big(2I_o^2\omega_1 A_m^2\left(t_{vr}-t_{fim}\right)\left(t_{fim}^2-2t_{fim}t_{vr}+3t_{fim}t_{tim}+t_{vr}^2+3t_{tim}^2-\right. \\
&\quad 3t_{tim}t_{vr}\Big)+6I_o^2\omega_1 A_m t_{tim}\left(t_{fim}-t_{vr}\right)\left(t_{fim}+2t_{tim}-t_{vr}\right)+6I_o^2\omega_1 t_{tim}^2\left(t_{vr}-t_{fim}\right) \\
&\quad +3t_{tim}^2\left(c_1^2-c_2^2\right)\cos\omega_1\left(t_{cz}-t_{vr}\right)\sin\omega_1\left(t_{cz}-t_{vr}\right)+3t_{tim}^2\left(c_1^2+c_2^2\right)\omega_1\left(t_{cz}-t_{vr}\right) \\
&\quad \left.-6t_{tim}^2 c_1 c_2\left(\cos^2\omega_1\left(t_{cz}-t_{vr}\right)-1\right)\right) \qquad \text{(A.12)} \\
W_{Drp} &= \int_{t_1}^{t_{vr}} i_{Crp(c)}^2 R_{Dr} dt + \int_{t_1}^{t_{vr}} i_{Crp(c)} V_{Dr(on)} dt + \int_{t_{vr}}^{t_{cz}} i_{Crp(c)}^2 R_{Dr} dt \\
&\quad + \int_{t_{vr}}^{t_{cz}} i_{Crp(c)} V_{Dr(on)} dt \\
&= \frac{1}{12t_{tim}^2\omega_1}\Big(12I_o\omega_1 V_{Dr(on)} t_{tim}^2\left(t_{vr}-t_{fim}\right)\left(1-A_m\right)+6I_o\omega_1 V_{Dr(on)} t_{tim} A_m \\
&\quad \left(t_{vr}-t_{fim}\right)^2+12V_{Dr(on)} t_{tim}^2 c_2\left(1-\cos\omega_1\left(t_{vr}-t_{cz}\right)\right)-12V_{Dr(on)} t_{tim}^2 c_1 \\
&\quad \sin\omega_1\left(t_{vr}-t_{cz}\right)+3R_{Dr} t_{tim}^2\left(c_2^2-c_1^2\right)\sin 2\omega_1\left(t_{vr}-t_{cz}\right)+6R_{Dr} t_{tim}^2 c_1 c_2 \\
&\quad \left(1-\cos 2\omega_1\left(t_{vr}-t_{cz}\right)\right)-4I_o^2\omega_1 A_m^2 R_{Dr}\left(t_{fim}-t_{vr}\right)\left(t_{fim}^2+3t_{fim}t_{tim}\right. \\
&\quad \left.-2t_{fim}t_{vr}+t_{vr}^2-3t_{tim}t_{vr}+3t_{tim}^2\right)+12I_o^2\omega_1 A_m R_{Dr} t_{tim}\left(t_{fim}-t_{vr}\right) \\
&\quad \left(t_{fim}-t_{vr}+2t_{tim}\right)-12I_o^2\omega_1 R_{Dr} t_{tim}^2\left(t_{fim}-t_{vr}\right)+ \\
&\quad 6R_{Dr} t_{tim}^2\omega_1\left(c_1^2+c_2^2\right)\left(t_{cz}-t_{vr}\right)\Big) \qquad \text{(A.13)}
\end{aligned}
$$

with t_{cz} replaced by t_2 for case 2.

$\underline{t_2 \le t < t_4}$

Case 3

For $t_2 \le t < t_{vr}$:

$$
\begin{aligned}
W_{Lbn} &= \int_{t_2}^{t_{vr}} i_{bn}^2 R_{Lb} dt = I_o^2 R_{Lb}\left(t_{vr}-t_2\right) \qquad \text{(A.14)} \\
W_{Crp} &= \int_{t_2}^{t_{vr}} i_{Crp(d)}^2 R_{Cr} dt = I_o^2 R_{Cr}\left(t_{vr}-t_2\right) \qquad \text{(A.15)} \\
W_{Drp} &= \int_{t_2}^{t_{vr}} i_{Crp(d)}^2 R_{Dr} dt + \int_{t_2}^{t_{vr}} i_{Crp(d)} V_{Dr(on)} dt \\
&= I_o^2 R_{Dr}\left(t_{vr}-t_2\right)+I_o V_{Dr(on)}\left(t_{vr}-t_2\right) \qquad \text{(A.16)}
\end{aligned}
$$

For $t_{vr} \leq t < t_{cz}$:

$$\begin{aligned}
W_{Lbp} &= \int_{t_{vr}}^{t_{cz}} i_{bp}^2 R_{Lb} dt \\
&= \frac{I_o^2 R_{Lb}}{2\omega_1} \left(\cos\omega_1 (t_{cz} - t_{vr}) \sin\omega_1 (t_{cz} - t_{vr}) + \omega_1 (t_{cz} - t_{vr})\right) \qquad \text{(A.17)} \\
W_{Lbn} &= \int_{t_{vr}}^{t_{cz}} i_{bn}^2 R_{Lb} dt \\
&= \frac{I_o^2 R_{Lb}}{2\omega_1} \left(\cos\omega_1 (t_{cz} - t_{vr}) \sin\omega_1 (t_{cz} - t_{vr}) + 3\omega_1 (t_{cz} - t_{vr})\right. \\
&\quad \left. -4\sin\omega_1 (t_{cz} - t_{vr})\right) \qquad \text{(A.18)} \\
W_{Crp} &= \int_{t_{vr}}^{t_{cz}} i_{Crp(e)}^2 R_{Cr} dt \\
&= \frac{I_o^2 R_{Cr}}{2\omega_1} \left(\cos\omega_1 (t_{cz} - t_{vr}) \sin\omega_1 (t_{cz} - t_{vr}) + \omega_1 (t_{cz} - t_{vr})\right) \qquad \text{(A.19)} \\
W_{Drp} &= \int_{t_{vr}}^{t_{cz}} i_{Crp(e)}^2 R_{Dr} dt + \int_{t_{vr}}^{t_{cz}} i_{Crp(e)} V_{Dr(on)} dt \\
&= \frac{I_o}{2\omega_1} \left(I_o R_{Dr} \cos\omega_1 (t_{cz} - t_{vr}) \sin\omega_1 (t_{cz} - t_{vr}) + I_o R_{Dr} \omega_1 (t_{cz} - t_{vr}) + \right. \\
&\quad \left. 2V_{Dr(on)} \sin\omega_1 (t_{cz} - t_{vr})\right) \qquad \text{(A.20)}
\end{aligned}$$

For $t_{cz} \leq t < t_4$:

$$W_{Lbn} = \int_{t_{cz}}^{t_4} i_{bn}^2 R_{Lb} dt = I_o^2 R_{Lb} (t_4 - t_{cz}) \qquad \text{(A.21)}$$

Cases 1 and 2

For $t_2 \leq t < t_{cz}$:

$$\begin{aligned}
W_{Lbp} &= \int_{t_2}^{t_{cz}} i_{bp}^2 R_{Lb} dt \\
&= \frac{R_{Lb}}{2\omega_1} \left(\left(c_{12}^2 - c_{13}^2\right) \cos\omega_1 (t_{cz} - t_2) \sin\omega_1 (t_{cz} - t_2) + \omega_1 \left(c_{12}^2 + c_{13}^2\right) (t_{cz} - t_2)\right. \\
&\quad \left. +2c_{12}c_{13} \left(1 - \cos^2\omega_1 (t_{cz} - t_2)\right)\right) \qquad \text{(A.22)} \\
W_{Lbn} &= \int_{t_2}^{t_{cz}} i_{bn}^2 R_{Lb} dt \\
&= \frac{R_{Lb}}{2\omega_1} \left(\left(c_{12}^2 - c_{13}^2\right) \cos\omega_1 (t_{cz} - t_2) \sin\omega_1 (t_{cz} - t_2) + \omega_1 \left(2I_o + c_{12}^2 + c_{13}^2\right)\right. \\
&\quad (t_{cz} - t_2) + 2c_{12}c_{13} \left(1 - \cos^2\omega_1 (t_{cz} - t_2)\right) - 4c_{12} I_o \sin\omega_1 (t_{cz} - t_2) + \\
&\quad \left. 4c_{13} I_o (\cos\omega_1 (t_{cz} - t_2) - 1)\right) \qquad \text{(A.23)}
\end{aligned}$$

$$
\begin{aligned}
W_{Crp} &= \int_{t_2}^{t_{cz}} i_{Crp(f)}^2 R_{Cr} dt \\
&= \frac{R_{Cr}}{2\omega_1}\left(\left(c_{12}^2 - c_{13}^2\right)\cos\omega_1\left(t_{cz}-t_2\right)\sin\omega_1\left(t_{cz}-t_2\right) + \omega_1\left(c_{12}^2 + c_{13}^2\right)\left(t_{cz}-t_2\right)\right. \\
&\quad \left. +2c_{12}c_{13}\left(1-\cos^2\omega_1\left(t_{cz}-t_2\right)\right)\right) \qquad \text{(A.24)} \\
W_{Drp} &= \int_{t_2}^{t_{cz}} i_{Crp(f)}^2 R_{Dr} dt + \int_{t_2}^{t_{cz}} i_{Crp(f)} V_{Dr(on)} dt \\
&= \frac{1}{4\omega_1}\left(R_{Dr}\left(c_{12}^2 - c_{13}^2\right)\sin 2\omega_1\left(t_{cz}-t_2\right) + 2R_{Dr}\omega_1\left(c_{12}^2 + c_{13}^2\right)\left(t_{cz}-t_2\right)\right. \\
&\quad +2R_{Dr}c_{12}c_{13}\left(1-\cos 2\omega_1\left(t_{cz}-t_2\right)\right) + 4V_{Dr(on)}\left(c_{12}\sin\omega_1\left(t_{cz}-t_2\right)+\right. \\
&\quad \left.\left. c_{13}\cos\omega_1\left(t_{cz}-t_2\right)\right) + 4V_{Dr(on)}c_{13}\right) \qquad \text{(A.25)}
\end{aligned}
$$

For $t_{cz} \leq t < t_4$:

$$
W_{Lbn} = \int_{t_{cz}}^{t_4} i_{bn}^2 R_{Lb} dt = I_o^2 R_{Lb}\left(t_4 - t_{cz}\right) \qquad \text{(A.26)}
$$

For case 1 $t_{cz} = t_2$ in equations A.22 to A.26.

A.2 Main IGBT turn-on

$t_4 \leq t < t_5$

Case 2 and 3

$$
\begin{aligned}
W_{Lbp} &= \int_{t_4}^{t_5} i_{bp(a)}^2 R_{Lb} dt = \frac{R_{Lb} V_d^2 t_{fvm}^3 \left(1-B_m\right)^2}{80 L_b^2} \qquad \text{(A.27)} \\
W_{Lbn} &= \int_{t_4}^{t_5} i_{bn(a)}^2 R_{Lb} dt \\
&= \frac{R_{Lb} t_{fvm}}{240 L_b^2}\left(3V_d^2 t_{fvm}^2\left(1-B_m\right)^2 - 40 V_d I_o L_b t_{fvm}\left(1-B_m\right) + \right. \\
&\quad \left. 240 I_o^2 L_b^2\right) \qquad \text{(A.28)} \\
W_{Gp} &= \int_{t_4}^{t_5} i_{bp(a)} v_{ce_{(Gp)}} dt = \frac{V_d^2 t_{fvm}^2\left(1-B_m\right)\left(1+3B_m\right)}{48 L_b} \qquad \text{(A.29)}
\end{aligned}
$$

Case 1

For $t_4 \leq t < t_{cz}$:

$$W_{Lbp} = \int_{t_4}^{t_{cz}} i_{bp(a)}^2 R_{Lb} dt = \frac{V_d^2 R_{Lb} (1 - B_m)^2 (t_{cz} - t_4)^5}{80 L_b^2 t_{fvm}^2} \tag{A.30}$$

$$\begin{aligned} W_{Lbn} &= \int_{t_4}^{t_{cz}} i_{bn(a)}^2 R_{Lb} dt \\ &= \frac{R_{Lb} (t_{cz} - t_4)}{240 L_b^2 t_{fvm}^2} \left(3V_d^2 (t_{cz} - t_4)^4 (1 - B_m)^2 - 40 V_d I_o L_b t_{fvm} (t_{cz} - t_4)^2 (1 - B_m)\right. \\ &\quad \left. + 240 I_o^2 L_b^2 t_{fvm}^2\right) \end{aligned} \tag{A.31}$$

$$\begin{aligned} W_{Gp} &= \int_{t_4}^{t_{cz}} i_{bp(a)} v_{ce_{(Gp)}} dt \\ &= \frac{V_d^2 (t_{cz} - t_4)^3 (1 - B_m)}{48 L_b t_{fvm}^2} (4 t_{fvm} - 3 (t_{cz} - t_4) (1 - B_m)) \end{aligned} \tag{A.32}$$

For $t_{cz} \leq t < t_5$:

$$W_{Lbp} = \int_{t_{cz}}^{t_5} i_{bp}^2 R_{Lb} dt = I_o^2 R_{Lb} (t_5 - t_{cz}) \tag{A.33}$$

$$\begin{aligned} W_{Gp} &= \int_{t_{cz}}^{t_5} i_{bp} v_{ce_{(Gp)}} dt \\ &= \frac{I_o V_d (t_5 - t_{cz})}{2 t_{fvm}} (2 t_{fvm} + (2 t_4 - t_5 - t_{cz}) (1 - B_m)) \end{aligned} \tag{A.34}$$

$t_5 \leq t < t_6$

Case 3

$$\begin{aligned} W_{Lbp} &= \int_{t_5}^{t_6} i_{bp(b)}^2 R_{Lb} dt \\ &= \frac{R_{Lb} t_{tvm}}{240 L_b^2} \left(V_d^2 t_{tvm}^2 \left(8 B_m^2 - 25 B_m + 20\right) + 240 L_b^2 i_{bp(a)}(t_5)^2\right. \\ &\quad \left. - 40 V_d L_b t_{tvm} i_{bp(a)}(t_5) (2 B_m - 3)\right) \end{aligned} \tag{A.35}$$

$$\begin{aligned} W_{Lbn} &= \int_{t_5}^{t_6} i_{bn(b)}^2 R_{Lb} dt \\ &= \frac{R_{Lb} t_{tvm}}{240 L_b^2} \left(V_d^2 t_{tvm}^2 \left(8 B_m^2 - 25 B_m + 20\right) + 240 L_b^2 \left(i_{bp(a)}(t_5) - I_o\right)^2\right. \\ &\quad \left. - 40 V_d L_b t_{tvm} \left(i_{bp(a)}(t_5) - I_o\right) (2 B_m - 3)\right) \end{aligned} \tag{A.36}$$

$$\begin{aligned} W_{Gp} &= \int_{t_5}^{t_6} i_{bp(b)} v_{ce_{(Gp)}} dt \\ &= \frac{V_d t_{tvm} B_m \left(V_d t_{tvm} (4 - 3 B_m) + 24 i_{bp(a)}(t_5) L_b\right)}{48 L_b} \end{aligned} \tag{A.37}$$

Case 2

For $t_5 \leq t < t_{cz}$:

$$\begin{aligned} W_{L_bp} &= \int_{t_5}^{t_{cz}} i_{bp(b)}^2 R_{Lb} dt \\ &= \frac{R_{Lb}}{240 L_b^2 t_{tvm}^2} \left(240 i_{bp(a)}(t_5)^2 L_b^2 t_{tvm}^2 (t_{cz} - t_5) + 120 V_d i_{bp(a)}(t_5) L_b t_{tvm}^2 (1 - B_m) \right. \\ &\quad (t_{cz} - t_5)^2 + 40 B_m V_d i_{bp(a)}(t_5) L_b t_{tvm} (t_{cz} - t_5)^3 + 20 (1 - B_m)^2 (t_{cz} - t_5)^3 \\ &\quad \left. +15 B_m (1 - B_m) (t_{cz} - t_5)^4 + 3 B_m^2 (t_{cz} - t_5)^5 \right) \end{aligned} \tag{A.38}$$

$$\begin{aligned} W_{Lbn} &= \int_{t_5}^{t_{cz}} i_{bn(b)}^2 R_{Lb} dt \\ &= \frac{R_{Lb}}{240 L_b^2 t_{tvm}^2} \left(240 \left(i_{bp(a)}(t_5) - I_o\right)^2 L_b^2 t_{tvm}^2 (t_{cz} - t_5) + 120 V_d \left(i_{bp(a)}(t_5) - I_o\right) \right. \\ &\quad L_b t_{tvm}^2 (1 - B_m) (t_{cz} - t_5)^2 + 40 B_m V_d \left(i_{bp(a)}(t_5) - I_o\right) L_b t_{tvm} (t_{cz} - t_5)^3 \\ &\quad +20 (1 - B_m)^2 (t_{cz} - t_5)^3 + 15 B_m (1 - B_m) (t_{cz} - t_5)^4 \\ &\quad \left. +3 B_m^2 (t_{cz} - t_5)^5 \right) \end{aligned} \tag{A.39}$$

$$\begin{aligned} W_{Gp} &= \int_{t_5}^{t_{cz}} i_{bp(b)} v_{ce_{(Gp)}} dt \\ &= \frac{V_d B_m}{48 L_b t_{tvm}^2} \left(48 i_{bp(a)}(t_5) L_b t_{tvm}^2 (t_{cz} - t_5) - 24 i_{bp(a)}(t_5) L_b t_{tvm} (t_{cz} - t_5)^2 \right. \\ &\quad +12 V_d t_{tvm}^2 (1 - B_m) (t_{cz} - t_5)^2 - 4 V_d t_{tvm} (2 - 3 B_m) (t_{cz} - t_5)^3 \\ &\quad \left. -3 V_d B_m (t_{cz} - t_5)^4 \right) \end{aligned} \tag{A.40}$$

For $t_{cz} \leq t < t_6$:

$$W_{Lbp} = \int_{t_{cz}}^{t_6} i_{bp}^2 R_{Lb} dt = I_o^2 R_{Lb} (t_6 - t_{cz}) \tag{A.41}$$

$$W_{Gp} = \int_{t_{cz}}^{t_6} i_{bp} v_{ce_{(Gp)}} dt = I_o B_m V_d \left(\left(1 + \frac{t_5}{t_{tvm}}\right) (t_6 - t_{cz}) - \frac{(t_6^2 - t_{cz}^2)}{2 t_{tvm}} \right) \tag{A.42}$$

Case 1

$$W_{Lbp} = \int_{t_5}^{t_6} i_{bp}^2 R_{Lb} dt = I_o^2 R_{Lb} t_{tvm} \tag{A.43}$$

$$W_{Gp} = \int_{t_5}^{t_6} i_{bp} v_{ce_{(Gp)}} dt = \frac{V_d B_m I_o t_{tvm}}{2} \tag{A.44}$$

$t_6 \leq t < t_7$

Case 3

For $t_6 \leq t < t_{cz}$:

$$\begin{aligned} W_{Lbp} &= \int_{t_6}^{t_{cz}} i_{bp(c)}^2 R_{Lb} dt \\ &= \frac{R_{Lb}}{12L_b^2}\left(V_d^2\left(t_{cz}^3 - t_6^3\right) + 6V_d L_b\left(i_{bp(b)}(t_6) - \frac{V_d t_6}{2L_b}\right)\left(t_{cz}^2 - t_6^2\right) + \right. \\ &\quad \left. 12L_b^2\left(i_{bp(b)}(t_6) - \frac{V_d t_6}{2L_b}\right)^2 (t_{cz} - t_6)\right) \qquad \text{(A.45)} \\ W_{Lbn} &= \int_{t_6}^{t_{cz}} i_{bn(c)}^2 R_{Lb} dt \\ &= \frac{R_{Lb}}{12L_b^2}\left(V_d^2\left(t_{cz}^3 - t_6^3\right) - 6L_b V_d\left(I_o + \frac{V_d t_6}{2L_b} - i_{bp(b)}(t_6)\right)\left(t_{cz}^2 - t_6^2\right) + \right. \\ &\quad \left. 12L_b^2\left(I_o + \frac{V_d t_6}{2L_b} - i_{bp(b)}(t_6)\right)^2 (t_{cz} - t_6)\right) \qquad \text{(A.46)} \end{aligned}$$

For $t_{cz} \leq t < t_7$:

$$W_{Lbp} = \int_{t_{cz}}^{t_7} i_{bp}^2 R_{Lb} dt = I_o^2 R_{Lb}\left(t_7 - t_{cz}\right) \qquad \text{(A.47)}$$

Case 1 and 2

$$W_{Lbp} = \int_{t_6}^{t_7} i_{bp}^2 R_{Lb} dt = I_o^2 R_{Lb}\left(t_7 - t_6\right) \qquad \text{(A.48)}$$

A.3 Snubber capacitor discharge

$t_7 \leq t < t_8$

$$\begin{aligned} W_{Lbp} &= \int_{t_7}^{t_8} i_{bp}^2 R_{Lb} dt \\ &= \frac{R_{Lb}}{2\omega_2}\left(c_{14}^2 \cos\omega_2\left(t_8 - t_7\right)\sin\omega_2\left(t_8 - t_7\right) + \omega_2\left(c_{14}^2 + 2\left(c_{15} - I_o\right)^2\right)\left(t_8 - t_7\right)\right. \\ &\quad \left. + 4c_{14}\left(c_{15} - I_o\right)\sin\omega_2\left(t_8 - t_7\right)\right) \qquad \text{(A.49)} \\ W_{Crp} &= \int_{t_7}^{t_8} i_{rp(a)}^2 R_{Cr} dt \\ &= \frac{R_{Cr}}{2\omega_2}\left(c_{14}^2 \cos\omega_2\left(t_8 - t_7\right)\sin\omega_2\left(t_8 - t_7\right) + \omega_2\left(c_{14}^2 + 2c_{15}^2\right)\left(t_8 - t_7\right)\right. \\ &\quad \left. + 4c_{14}c_{15}\sin\omega_2\left(t_8 - t_7\right)\right) \qquad \text{(A.50)} \end{aligned}$$

$$
\begin{aligned}
W_{Lrp} &= \int_{t_7}^{t_8} i_{rp(a)}^2 R_{Lr} dt \\
&= \frac{R_{Lr}}{2\omega_2}\left(c_{14}^2 \cos\omega_2 (t_8 - t_7)\sin\omega_2 (t_8 - t_7) + \omega_2\left(c_{14}^2 + 2c_{15}^2\right)(t_8 - t_7)\right. \\
&\quad \left. +4c_{14}c_{15}\sin\omega_2 (t_8 - t_7)\right) \qquad \text{(A.51)} \\
W_{Srp} &= \int_{t_7}^{t_8} i_{rp(a)} v_{ce_{(Srp)}} dt \\
&= \frac{1}{2\omega_2^2 t_{fva}}\left(2c_{14}\omega_2 t_{fva}\left(v_{Crp(max)} - \frac{V_d}{2}\right)\sin\omega_2 (t_8 - t_7) - 2c_{14}\left(v_{Crp(max)} - \frac{V_d}{2}\right)\right. \\
&\quad (1 - B_a)\left(\cos\omega_2 (t_8 - t_7) + \omega_2 (t_8 - t_7)\sin\omega_2 (t_8 - t_7) - 1\right) \\
&\quad \left. +c_{15}\omega_2^2\left(v_{Crp(max)} - \frac{V_d}{2}\right)\left(2t_{fva}(t_8 - t_7) - (1 - B_a)(t_8 - t_7)^2\right)\right) \qquad \text{(A.52)} \\
W_{Srpd} &= \int_{t_7}^{t_8} i_{rp(a)} V_{Srd(on)} dt + \int_{t_7}^{t_8} i_{rp(a)}^2 R_{Srd} dt \\
&= \frac{1}{2\omega_2}\left(c_{14}^2 R_{Lr}\cos\omega_2 (t_8 - t_7)\sin\omega_2 (t_8 - t_7) + \omega_2 R_{Lr}\left(c_{14}^2 + 2c_{15}^2\right)(t_8 - t_7)\right. \\
&\quad +4c_{14}c_{15}R_{Lr}\sin\omega_2 (t_8 - t_7) + 2V_{Srd(on)}c_{14}\sin\omega_2 (t_8 - t_7) + \\
&\quad \left. 2V_{Srd(on)}c_{15}\omega_2 (t_8 - t_7)\right) \qquad \text{(A.53)}
\end{aligned}
$$

$\underline{t_8 \leq t < t_9}$

$$
\begin{aligned}
W_{Lbp} &= \int_{t_8}^{t_9} i_{bp}^2 R_{Lb} dt \\
&= \frac{R_{Lb}}{2\omega_2}\left(\left(c_{16}^2 - c_{17}^2\right)\cos\omega_2 (t_9 - t_8)\sin\omega_2 (t_9 - t_8) + \omega_2\left(2I_o (I_o - 2c_{18}) + c_{16}^2 + \right.\right. \\
&\quad \left.\left. c_{17}^2 + 2c_{18}^2\right)(t_9 - t_8) - 4c_{16}(I_o - c_{18})\sin\omega_2 (t_9 - t_8) + 4c_{17}(I_o - c_{18})\right. \\
&\quad \left.(\cos\omega_2 (t_9 - t_8) - 1) + 2c_{16}c_{17}\left(\cos^2\omega_2 (t_9 - t_8) - 1\right)\right) \qquad \text{(A.54)} \\
W_{Lrp} &= \int_{t_8}^{t_9} i_{rp(b)}^2 R_{Lr} dt \\
&= \frac{R_{Lr}}{2\omega_2}\left(\left(c_{16}^2 - c_{17}^2\right)\cos\omega_2 (t_9 - t_8)\sin\omega_2 (t_9 - t_8) + \omega_2\left(c_{16}^2 + c_{17}^2 + 2c_{18}^2\right)\right. \\
&\quad (t_9 - t_8) + 2c_{16}c_{17}\left(1 - \cos^2\omega_2 (t_9 - t_8)\right) + 4c_{16}c_{18}\sin\omega_2 (t_9 - t_8) \\
&\quad \left. -4c_{17}c_{18}(\cos\omega_2 (t_9 - t_8) - 1)\right) \qquad \text{(A.55)} \\
W_{Crp} &= \int_{t_8}^{t_9} i_{rp(b)}^2 R_{Cr} dt \\
&= \frac{R_{Cr}}{2\omega_2}\left(\left(c_{16}^2 - c_{17}^2\right)\cos\omega_2 (t_9 - t_8)\sin\omega_2 (t_9 - t_8) + \omega_2\left(c_{16}^2 + c_{17}^2 + 2c_{18}^2\right)\right. \\
&\quad (t_9 - t_8) + 2c_{16}c_{17}\left(1 - \cos^2\omega_2 (t_9 - t_8)\right) + 4c_{16}c_{18}\sin\omega_2 (t_9 - t_8) \\
&\quad \left. -4c_{17}c_{18}(\cos\omega_2 (t_9 - t_8) - 1)\right) \qquad \text{(A.56)}
\end{aligned}
$$

$$
\begin{aligned}
W_{Srp} &= \int_{t_8}^{t_9} i_{rp(b)} v_{ce(Srp)} dt \\
&= \frac{1}{2\omega_2^2 t_{tva}} \left(2B_a c_{16} \left(v_{Crp(max)} - \frac{V_d}{2} \right) (1 - \cos \omega_2 (t_9 - t_8)) \right. \\
&\quad + 2B_a c_{17} \left(v_{Crp(max)} - \frac{V_d}{2} \right) (\omega_2 t_{tva} - \sin \omega_2 (t_9 - t_8)) + \\
&\quad \left. B_a c_{18} \omega_2^2 \left(v_{Crp(max)} - \frac{V_d}{2} \right) (t_9 - t_8) (2t_{tva} - t_9 + t_8) \right) \qquad \text{(A.57)} \\
W_{Srpd} &= \int_{t_8}^{t_9} i_{rp(b)} V_{Srd(on)} dt + \int_{t_8}^{t_9} i_{rp(b)}^2 R_{Srd} dt \\
&= \frac{V_{Srd(on)}}{\omega_1} (c_{16} \sin \omega_2 (t_9 - t_8) + c_{17} (1 - \cos \omega_2 (t_9 - t_8)) + c_{18} \omega_2 (t_9 - t_8)) \\
&\quad + \frac{R_{Srd}}{2\omega_2} \left(\left(c_{16}^2 - c_{17}^2 \right) \cos \omega_2 (t_9 - t_8) \sin \omega_2 (t_9 - t_8) + \omega_2 \left(c_{16}^2 + c_{17}^2 + 2c_{18}^2 \right) \right. \\
&\quad (t_9 - t_8) + 2c_{16} c_{17} \left(1 - \cos^2 \omega_2 (t_9 - t_8) \right) + 4c_{16} c_{18} \sin \omega_2 (t_9 - t_8) \\
&\quad \left. + 4c_{17} c_{18} (1 - \cos \omega_2 (t_9 - t_8)) \right) \qquad \text{(A.58)}
\end{aligned}
$$

$\underline{t_9 \leq t < t_{10}}$

$$
\begin{aligned}
W_{Lbp} &= \int_{t_9}^{t_{10}} i_{bp}^2 R_{Lb} dt \\
&= \frac{R_{Lb}}{2\omega_2} \left(\omega_2 \left(2I_o^2 + c_{19}^2 + c_{20}^2 \right) (t_{10} - t_9) - 4c_{20} I_o (1 - \cos \omega_2 (t_{10} - t_9)) - \right. \\
&\quad 4c_{19} I_o \sin \omega_2 (t_{10} - t_9) + \left(c_{19}^2 - c_{20}^2 \right) \cos \omega_2 (t_{10} - t_9) \sin \omega_2 (t_{10} - t_9) \\
&\quad \left. + 2c_{19} c_{20} \left(1 - \cos^2 \omega_2 (t_{10} - t_9) \right) \right) \qquad \text{(A.59)} \\
W_{Lrp} &= \int_{t_9}^{t_{10}} i_{rp(c)}^2 R_{Lr} dt \\
&= \frac{R_{Lr}}{2\omega_2} \left(\omega_2 \left(c_{19}^2 + c_{20}^2 \right) (t_{10} - t_9) + \left(c_{19}^2 - c_{20}^2 \right) \cos \omega_2 (t_{10} - t_9) \sin \omega_2 (t_{10} - t_9) \right. \\
&\quad \left. + 2c_{19} c_{20} \left(1 - \cos^2 \omega_2 (t_{10} - t_9) \right) \right) \qquad \text{(A.60)} \\
W_{Crp} &= \int_{t_9}^{t_{10}} i_{rp(c)}^2 R_{Cr} dt \\
&= \frac{R_{Cr}}{2\omega_2} \left(\omega_2 \left(c_{19}^2 + c_{20}^2 \right) (t_{10} - t_9) + \left(c_{19}^2 - c_{20}^2 \right) \cos \omega_2 (t_{10} - t_9) \sin \omega_2 (t_{10} - t_9) \right. \\
&\quad \left. + 2c_{19} c_{20} \left(1 - \cos^2 \omega_2 (t_{10} - t_9) \right) \right) \qquad \text{(A.61)} \\
W_{Srp} &= \int_{t_9}^{t_{10}} i_{rp(c)} V_{Sr(on)} dt + \int_{t_9}^{t_{10}} i_{rp(c)}^2 R_{Sr} dt \\
&= \frac{V_{Sr(on)}}{\omega_2} (c_{19} \sin \omega_2 (t_{10} - t_9) - c_{20} \cos \omega_2 (t_{10} - t_9) + c_{20}) + \frac{R_{Sr}}{2\omega_2} \left(\omega_2 \left(c_{19}^2 + c_{20}^2 \right) \right. \\
&\quad \left. (t_{10} - t_9) + \left(c_{19}^2 - c_{20}^2 \right) \cos \omega_2 (t_{10} - t_9) \sin \omega_2 (t_{10} - t_9) + 2c_{19} c_{20} \right.
\end{aligned}
$$

$$\left(1-\cos^2\omega_2\left(t_{10}-t_9\right)\right)\Big) \tag{A.62}$$

$$\begin{aligned} W_{Srpd} &= \int_{t_9}^{t_{10}} i_{rp(c)} V_{Srd(on)}\,dt + \int_{t_9}^{t_{10}} i_{rp(c)}^2 R_{Srd}\,dt \\ &= \frac{V_{Srd(on)}}{\omega_2}\left(c_{19}\sin\omega_2\left(t_{10}-t_9\right) - c_{20}\cos\omega_2\left(t_{10}-t_9\right)+c_{20}\right)+ \\ &\quad \frac{R_{Srd}}{2\omega_2}\Big(\omega_2\left(c_{19}^2+c_{20}^2\right)\left(t_{10}-t_9\right)+\left(c_{19}^2-c_{20}^2\right)\cos\omega_2\left(t_{10}-t_9\right)\sin\omega_2\left(t_{10}-t_9\right)+ \\ &\quad 2c_{19}c_{20}\left(1-\cos^2\omega_2\left(t_{10}-t_9\right)\right)\Big) \end{aligned} \tag{A.63}$$

$\underline{t_{10} \le t < t_{11}}$

$$\begin{aligned} W_{Lbp} &= \int_{t_{10}}^{t_{11}} i_{bp}^2 R_{Lb}\,dt \\ &= \frac{V_d^2 R_{Lb}\left(t_{11}^3-t_{10}^3\right)}{12L_r^2} + \frac{\left(I_o - i_{rp(c)}(t_{10}) - \frac{V_d t_{10}}{2L_r}\right)V_d R_{Lb}\left(t_{11}^2-{t_{10}}^2\right)}{2L_r} + \\ &\quad \left(I_o - i_{rp(c)}(t_{10}) - \frac{V_d t_{10}}{2L_r}\right)^2 R_{Lb}\left(t_{11}-t_{10}\right) \end{aligned} \tag{A.64}$$

$$\begin{aligned} W_{Lrp} &= \int_{t_{10}}^{t_{11}} i_{rp(d)}^2 R_{Lr}\,dt \\ &= \frac{V_d^2 R_{Lr}\left(t_{11}^3-t_{10}^3\right)}{12L_r^2} - \frac{\left(i_{rp(c)}(t_{10}) + \frac{V_d t_{10}}{2L_r}\right)V_d R_{Lr}\left(t_{11}^2-t_{10}^2\right)}{2L_r} + \\ &\quad \left(i_{rp(c)}(t_{10}) + \frac{V_d t_{10}}{2L_r}\right)^2 R_{Lr}\left(t_{11}-t_{10}\right) \end{aligned} \tag{A.65}$$

$$\begin{aligned} W_{Srp} &= \int_{t_{10}}^{t_{11}} i_{rp(d)} V_{Sr(on)}\,dt + \int_{t_{10}}^{t_{11}} i_{rp(d)}^2 R_{Sr}\,dt \\ &= \left(i_{rp(c)}(t_{10}) + \frac{V_d t_{10}}{2L_r}\right)V_{Sr(on)}\left(t_{11}-t_{10}\right) - \frac{V_d V_{Sr(on)}\left(t_{11}^2-t_{10}^2\right)}{4L_r} + \\ &\quad \frac{V_d^2 R_{Sr}\left(t_{11}^3-t_{10}^3\right)}{12L_r^2} - \frac{\left(i_{rp(c)}(t_{10}) + \frac{V_d t_{10}}{2L_r}\right)V_d R_{Sr}\left(t_{11}^2-t_{10}^2\right)}{2L_r} + \\ &\quad \left(i_{rp(c)}(t_{10}) + \frac{V_d t_{10}}{2L_r}\right)^2 R_{Sr}\left(t_{11}-t_{10}\right) \end{aligned} \tag{A.66}$$

$$\begin{aligned} W_{Srpd} &= \int_{t_{10}}^{t_{11}} i_{rp(d)} V_{Srd(on)}\,dt + \int_{t_{10}}^{t_{11}} i_{rp(d)}^2 R_{Srd}\,dt \\ &= \left(i_{rp(c)}(t_{10}) + \frac{V_d t_{10}}{2L_r}\right)V_{Srd(on)}\left(t_{11}-t_{10}\right) - \frac{V_d V_{Srd(on)}\left(t_{11}^2-t_{10}^2\right)}{4L_r} + \\ &\quad \frac{V_d^2 R_{Srd}\left(t_{11}^3-t_{10}^3\right)}{12L_r^2} - \frac{\left(i_{rp(c)}(t_{10}) + \frac{V_d t_{10}}{2L_r}\right)V_d R_{Srd}\left(t_{11}^2-t_{10}^2\right)}{2L_r} + \\ &\quad \left(i_{rp(c)}(t_{10}) + \frac{V_d t_{10}}{2L_r}\right)^2 R_{Srd}\left(t_{11}-t_{10}\right) \end{aligned} \tag{A.67}$$

$$\begin{aligned} W_{Drp} &= \int_{t_{10}}^{t_{11}} i_{rp(d)} V_{Dr(on)} dt + \int_{t_{10}}^{t_{11}} i_{rp(d)}^2 R_{Dr} dt \\ &= \left(i_{rp(c)}(t_{10}) + \frac{V_d t_{10}}{2L_r}\right) V_{Dr(on)} \left(t_{11} - t_{10}\right) - \frac{V_d V_{Dr(on)} \left(t_{11}^2 - t_{10}^2\right)}{4L_r} + \\ &\quad \frac{V_d^2 R_{Dr} \left(t_{11}^3 - t_{10}^3\right)}{12L_r^2} - \frac{\left(i_{rp(c)}(t_{10}) + \frac{V_d t_{10}}{2L_r}\right) V_d R_{Dr} \left(t_{11}^2 - t_{10}^2\right)}{2L_r} + \\ &\quad \left(i_{rp(c)}(t_{10}) + \frac{V_d t_{10}}{2L_r}\right)^2 R_{Dr} \left(t_{11} - t_{10}\right) \end{aligned} \tag{A.68}$$

$\underline{t_{11} \leq t < t_{12}}$

$$W_{Lbp} = \int_{t_{11}}^{t_{12}} I_o^2 R_{Lb} dt = I_o^2 R_{Lb} \left(t_{12} - t_{11}\right) \tag{A.69}$$