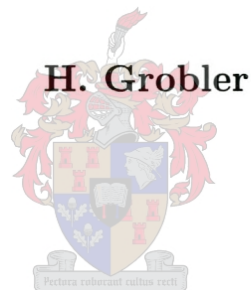

ASPECTS AFFECTING THE DESIGN OF A LOW EARTH
ORBIT SATELLITE ON-BOARD COMPUTER



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SUPERVISOR: PROF. P.J. BAKKES

Declaration

I, the undersigned, hereby declare that the work contained in this thesis is my original work, and has not previously been submitted at any University (in part or in its entirety) towards the achievement of a degree.

H. Grobler

Abstract

Satellites are not all made equal. The large number of possible orbits, desired functionality and budget constraints are but a few of the factors that influence the design of a satellite. Given a particular set of design requirements, a number of designs may meet these requirements. Each of these designs will typically entail a trade-off between a number of (conflicting) parameters, whilst still satisfying the system requirements.

The On-Board Computer (OBC) of a satellite, the satellite subsystem primarily responsible for the operational control of a satellite, can consequently be designed in any of a number of different ways. As the factors that influence the flight performance of an OBC differs to those of a terrestrial computer, the OBC design will therefore be significantly different. A high-level overview of the factors that impact OBC design and operation is presented. Improvements to the existing designs are proposed. In conclusion, a number of guidelines for a future OBC design also are given.

Opsomming

Elke satelliet het unieke eienskappe wat bepaal word deur onderandere, die teiken wentelbaan, verwagte funksionaliteit en koste oorweegings. Vir 'n spesifieke stelsel ontwerp bestaan daar 'n aantal moontlike ontwerpe wat aan die stelsel vereistes voldoen. Elk van hierdie ontwerpe sal tipies behels dat verskillende parameters teen mekaar afgespeel word, terwyl die stelsel vereistes steeds aan voldoen word.

Die Aanboord Rekenaar (AR) van 'n satelliet, die satelliet substelsel hoofsaaklik verantwoordelik vir die beheer van die satelliet, kan vervolgens uit een van veele moontlike ontwerpe bestaan. Aangesien die faktore wat die werkverrigting van 'n AR beïnvloed verskil van die van 'n rekenaar wat op die aard oppervlak gebruik word, sal die AR ontwerp dienoreenkomstig verskil. 'n Hoeflak oorsig van die faktore wat AR ontwerp beïnvloed sal gegee word. Verbeteringe wat aan die huidige AR ontwerpe gedoen kan word sal bespreek word. Ter afsluiting sal 'n aantal riglyne vir toekomstige AR ontwerpe gegee word.

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- The many students who have contributed to the **SUNSAT** project.

Chapter 1

Introduction

In 1991 c. the **SUNSAT** Project was initiated. The product of this project, the **SUNSAT** microsatellite, has since been launched and been in orbit for almost two years. Many lessons have been learned during the development, integration, launch and operation of **SUNSAT**.

Given that **SUNSAT** was the first product of its kind to be developed locally, it is understandable that a number of the original design requirements did not accurately reflect the in-orbit requirements. Similarly, a number of the design choices and final implementations were less than ideal. To derive maximum benefit from **SUNSAT**, it is important to analyse the in-orbit characteristics of **SUNSAT** in order to optimize any subsequent designs.

For the purpose of this investigation, aspects influencing the launch and operational performance of a satellite on-board computer will be examined. These represent a subset of the aspects influencing the satellite as a whole. The aspects which impact other subsystems of a satellite will in some cases be mentioned, but not discussed in detail.

1.1 Satellite On-Board Computers

Modern satellites employ a computer system that is responsible for necessary housekeeping tasks and execution of the application software which performs the satellite's functions. The tasks the On-Board Computer (OBC) must perform depends on the system control architecture chosen for the satellite. Certain satellites implement a control architecture where the OBC is responsible for almost all control actions. These include, the decoding of external telecommands, attitude control, payload management, *etc.* In such satellites, the term Command and Data Handling (C&DH) is often used to refer such a OBC subsystem.

In other satellites, control is delegated to intelligent controllers in each of the satellite subsystems. In this case the OBC is only responsible for the high level control and certain logical services (data management, operations scheduling, *etc.*). The term C&DH is therefore not applicable in the conventional sense. This is the architecture that best describes the control architecture of **SUNSAT**.

The control architecture is an integral part of the larger system architecture. The system architecture in turn depends on the mission objectives, budget constraints and so forth. Given these parameters, the design philosophy chosen to a large extent determines the final implementation of the system.

1.2 Design Philosophy

Although the underlying principles of electronic design are fundamental (to all design problems entailing electronic systems), the approach used during the design can vary greatly. For example, the design of “mission critical systems” generally assigns highest priority to two design criteria, namely *reliability* and *availability*. On the other hand, the design of “econo systems” assigns the highest priority to *cost*. Note that in both designs the *core* or *required* functionality is attained.

One of the dominant design priorities of **SUNSAT** was that of low cost. The primary result of this requirement has been the use of relatively inexpensive commercial components (versus expensive military and/or space qualified components). A trade-off was thus made between reliability and cost (*i.e.* when faced with a component selection choice, a “sufficiently” reliable component was chosen instead of the “most” reliable component).

During the design process, additional design priorities were also given attention and the aim was to find the optimal balance between these priorities. These priorities include:

- System reliability
- Optimal system performance
- Optimal system flexibility
- Software compatibility
- Component availability
- Acceptable component radiation tolerance
- Minimal mass requirements
- Minimal volume requirements
- Minimal power requirements

As happens with many products, with time, a number of design changes were made that can best be described as “nice-to-have’s” (also known as *feature creep*). In other cases, additions/changes were made to the original design in order to accommodate new payloads and to meet the requirements of new launch vehicles. To initiate the study of the On-Board Computers of **SUNSAT**, the following section will describe the basic structure of the Flight Model (FM) of **SUNSAT** microsatellite.

1.3 Overview of the Sunsat Microsatellite

SUNSAT [54] is a cubical Low Earth Orbit (LEO) microsatellite with sides of approximately 45 cm in length and weight 63 kg. The orbit configuration is polar and slightly elliptical with perigee 650 km, apogee 850 km and inclination 96.7°. The orbital period is approximately 97 minutes and the satellite is therefore only visible over South Africa 3 to 4 times per day (for approximately 14 minutes per over-flight). SUNSAT was one of two secondary payloads of an Argos/P91-1 Delta II mission. The other secondary payload was a Danish satellite ØRSTED [5].

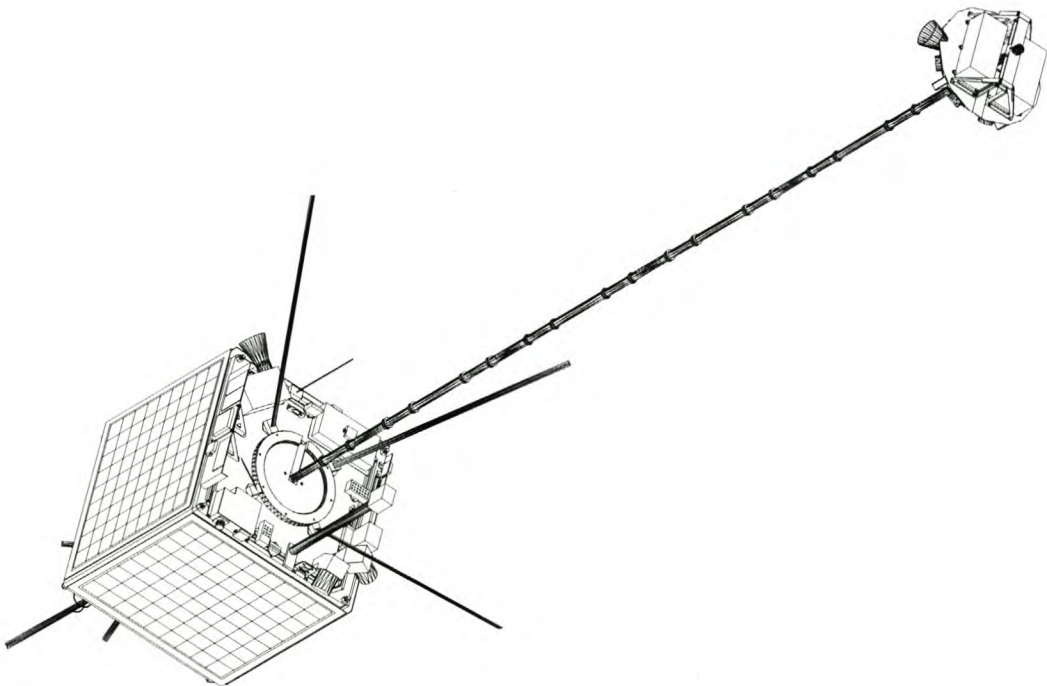


Figure 1.1: The SUNSAT microsatellite, viewed after boom deployment.

The skeleton of the satellite consists of machined aluminum alloy components and is divided into a number of layers (each layer referred to as a *tray*). The satellite systems have been divided into a number of subsystems and each subsystem has been assigned to a specific tray. The tray a subsystem has been assigned to is determined by the nature of the subsystem and its interface requirements. In the FM, the trays are bolted together to form a rigid cube. The solar panels are then attached to four sides of the cube. Under normal operating conditions, the satellite has a continual spin about its Z-axis (which is in the direction of the boom) in order to maintain an even thermal distribution.

The major digital subsystems of the SUNSAT satellite are (with their respective reference

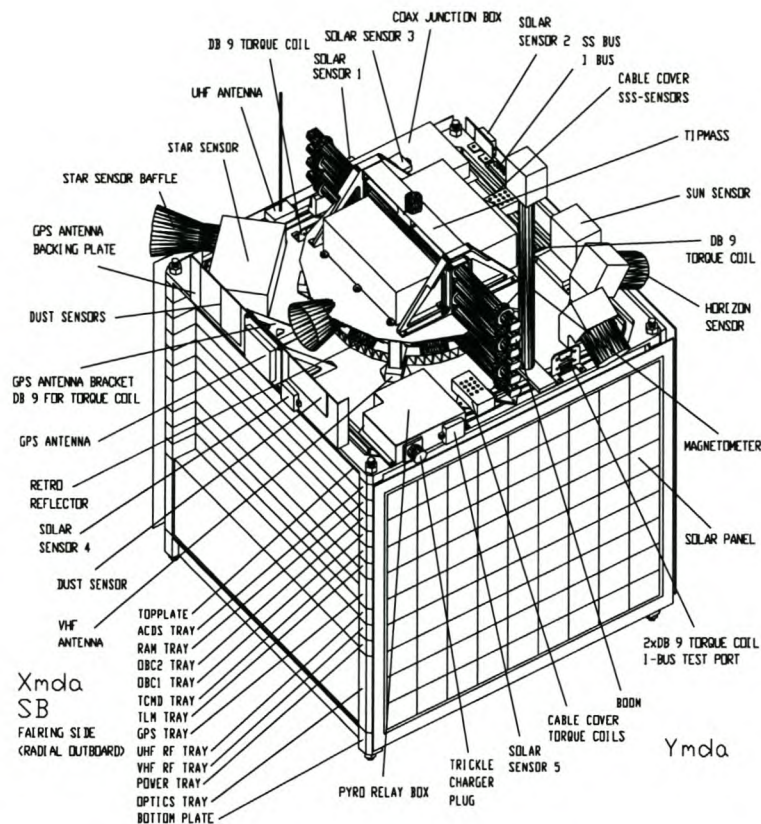


Figure 1.2: The SUNSAT microsatellite, subsystem view.

names highlighted):

- ① **ADCS** → Attitude Determination and Control Subsystem
- ② **RAMTRAY** → 64 MB Mass Memory
- ③ **OBC1** → First On-Board Computer
- ④ **OBC2** → Second On-Board Computer
- ⑤ **TTMS** → Telecommand and Telemetry Modem Subsystem
- ⑥ **POWER** → Power Management Subsystem

In addition to the major subsystems that form the “satellite bus”, SUNSAT also contains a number of payloads:

- ① **IMAGER** → 3 band linear CCD imager
- ② **GPS** → NASA TurboRogue GPS receiver

- ③ **DSP** → Digital Signal Processor
- ④ **SCHEXP** → School experiments
- ⑤ **EEV** → EEV solar cell experiment
- ⑥ **MAG** → High accuracy magnetometer

The subsystems in the trays of the satellite are interconnected by means of a *cable harness*. This harness consists of a few hundred electrical connections. Note that no optical or galvanic isolation has been implemented between any of the subsystems.

There are two types of signals that are exchanged between trays: slow changing signals and fast changing signals. These two groups of signals are separated as far as possible from each other by placing them on opposite sides of the satellite. This separation minimizes the interference caused by cross-talk.

Subsequent chapters will discuss particular aspects of **SUNSAT** in some detail. In order to place the references to the **SUNSAT** subsystems in context, a short overview of each subsystem follows. The overview and analysis of the OBCs, the focus of this study, will be presented in a later chapter.

1.3.1 Telemetry, Telecommand and Modem Subsystem

All core subsystems on **SUNSAT** have a minimum of two interfaces. One of these interfaces, the Telecommand interface, connects the subsystem to the Telecommand subsystem (TCMD). The TCMD subsystem consists of a large number of discrete registers, the output of which are used to control the other subsystems of the satellite. The state of the registers can be changed by control frames received from a groundstation (via the satellite communication receivers). The OBCs can also set or clear bits in the TCMD registers.

To minimize the power requirements of **SUNSAT**, unused subsystems are switched off under the control of the TCMD subsystem. The TCMD subsystem can also supply control lines to a subsystem that can be used for any subsystem specific control. Due to the limited number of TCMD registers and the limited switching rate, the TCMD subsystem is generally not used as a communication mechanism between subsystems.

Another interface that all core subsystems have is the Telemetry interface. This interface allows the Telemetry Subsystem (TLM) to obtain information about the current state of the subsystem. This information can be analog values sampled with an Analog-to-Digital Converter (ADC) on each subsystem, or the information can be status bits (logical 0 or 1 states). The Telemetry subsystem samples data from all the satellite subsystems by cycling in sequence through all the telemetry sources (called *telemetry channels*).

1.3.2 Attitude Detection and Control Subsystem

The Attitude Detection and Control Subsystem (ADCS) [79] is responsible for the attitude control of the satellite. The ADCS system can be divided into three parts: sensors, low-level control and high-level control. The ADCS sensor components include, amongst other, star sensors, horizon sensors and magnetometers.

The low-level control is performed by a 8031 microcontroller which commands magneto-torquers and reaction wheels. The high-level control is performed by a T800 Transputer. Redundancy has been incorporated into *SUNSAT* in that one of the on-board computers (OBC2) can implement the high-level control provided by the T800 Transputer. Furthermore, both the T800 and OBC2 can directly access the sensors, magneto-torquers and reaction wheels (by what is known as the *reaction wheel bus*).

Passive attitude control is achieved by means of a 2.3 m gravity boom with a tip mass of 6 kg. On the tip of this boom a number of sensors are located, one of which is a 3-axis Fluxgate magnetometer.

1.3.3 64 MB Mass Memory

The RAMTRAY [10] is designed to store image and miscellaneous other data (such as Telemetry Whole Orbit Data). In order to successfully handle the image data, there is very close integration between the RAMTRAY and the IMAGER. So much so that the RAMTRAY contains a fair portion on the IMAGER electronics.

To further support the imaging operations of *SUNSAT*, the RAMTRAY contains a FPGA to be used for real-time compression. The FPGA used is a SRAM based Xilinx XC3000. The configuration of the FPGA occurs via telecommand signals. No flight data is available about the performance of the compressor as this component has yet to be activated on *SUNSAT*.

The RAMTRAY is based on Static RAM technology. and is organized as 8 daughter-boards of 8 MB each. Each daughter-board can be independently activated/deactivated. The RAMTRAY has been designed to support a maximum transfer rate of ≈ 4.5 MB/s. To store WOD data, the OBC can create a filesystem in the Mass Memory. This is referred to as the *RAMDISK*. Image data is stored as received from the linear CCD's (one byte per band per pixel).

1.4 Outline

- Chapter 1 has introduced the thesis subject and given an overview of the *SUNSAT* microsatellite.
- Chapter 2 gives an overview of the environmental aspects which potentially influence the design and operation of an on-board computer.

- Chapter 3 discusses radiation effects. Radiation effects are the primary environmental effect and a separate chapter is dedicated to the study of these effects.
- Chapter 4 gives an overview of the Flight Management System of **SUNSAT**. Problems areas that were identified during the design, implementation, integration and operation of **SUNSAT** will be highlighted.
- Chapter 5 describes an attempt at system level modeling, which aims to reduce the cost of producing an OBC.
- Chapter 6, the concluding chapter, describes shortly a new, simpler architecture for the OBCs. Design guidelines that can significantly improve the performance of a low cost, low earth orbit microsatellite are also highlighted.



Chapter 2

Environmental Aspects

The environment in which an electronic system must operate dictates constraints on the design of the system. In the following sections a number of aspects relevant to the satellite environment are discussed. Aspects such as aerodynamic drag and microgravity are not considered relevant to digital system and/or on-board computers and will not be discussed.

2.1 Transient Launch Environment (TLE)

The TLE consists largely of mechanical components and can be subdivided into the following elements:

- ✘ launcher (quasi-static) acceleration loads - necessary to reach orbit
- ✘ launcher dynamic loads caused by solid-booster ignition, passage through zones of high winds and engine-thrust termination (both solid boosters and liquid stage)
- ✘ launcher-separation shocks
- ✘ acoustic pressure mainly caused by engine noise reflecting from the ground

To minimize the impact of the TLE on the launch vehicle payloads, a protective cover (referred to as the *fairing*) encloses the payload area. The fairing is typically lined with a damping blanket to absorb the launch and level flight acoustic pressure. The blanket also protects the payloads from the high temperatures the fairing reaches due to atmospheric friction. During launch the maximum acceleration the satellite is subjected to is typically 10 *g* [15]. In the case of **SUNSAT**, the components of the satellite (e.g., reaction wheels, IMAGER) were designed to withstand 20 *g* accelerations. Electronic components are generally not sensitive to acceleration, except for their attachment to the PCB. If correctly soldered by personnel qualified to perform soldering for space environment, no mechanical failures should be experienced. The type of internal failures that could occur when an electronic component is subjected to vibration are:

- ✘ Internal structural damage due to faulty bonds: silicon to electrical contact or silicon to packaging.
- ✘ Internal short circuit due to metalization residue (that becomes dislodged by the vibration).

Modern semiconductor manufacturing processes have attained relatively high standards of quality and therefore component level mechanical failures seldom occur. Further, components should be solder in and no unsoldered (in sockets) components should be permitted unless the electrical contact stability can be guaranteed. To ensure that no components are used that contain manufacture faults, component lot qualification is often done. To qualify **SUNSAT** for the TLE, two types of tests were conducted: Shock tests [85] (emulating the launcher-separation shocks) and vibration tests [86] (emulating the lift-off and level flight acoustic/random induced vibrations). During these tests, no component failures were encountered.

2.2 Vacuum

The components selected must be able to perform adequately in a vacuum environment. The primary effect a vacuum environment has on components is that of *out-gassing* (i.e. the emission of vapour(s) trapped inside the component). These vapour(s) can deposit on optical components (such as mirrors, prisms and/or lens) and degrade their performance. The majority of components manufactured using modern fabrication techniques do not exhibit significant out-gassing.

There are however particular components that, due to their construction, out-gas. The electrolytic capacitor is one such component and cannot therefore be safely used in space (tantalum capacitors are typically used as replacement). To ensure that no components that suffer from manufacture defects could cause out-gassing, vacuum tests are performed. These tests should highlight any such defective components. The environmental tests of **SUNSAT** included vacuum qualification tests [87, 71].

2.3 Thermal Environment

Electronic components do not function within specification when exposed to extreme temperatures. The thermal environment must therefore be taken into account during the design of the satellite. The external, thermally insulated portions of a satellite can typically experience temperature variations from $-263\text{ }^{\circ}\text{C}$ (no solar illumination) to over $+100\text{ }^{\circ}\text{C}$ (full illumination).

Initial thermal modeling of **SUNSAT** [18] evaluated the use of Z-axis spin for thermal control. Given a successful thermal design, the internal temperatures of a satellite are more hospitable to electronic components. The thermal extremes experienced inside a LEO

Table 2.1: Thermal maximums measured on SUNSAT

Sensor	Temperature
ADCS T800	64 °C
ADCS ambient	56 °C
OBC1 80C188	58 °C
UHF ambient	48 °C
Bottom plate	61 °C

satellite are thus typically specified as $-15\text{ }^{\circ}\text{C}$ and $+45\text{ }^{\circ}\text{C}$ [87, 71], depending on the orbit and thermal design. The initial specification of SUNSAT [54] required that the majority of the digital systems be designed for an operational temperature range of -30 to $+55\text{ }^{\circ}\text{C}$.

The effects thermal cycling has on digital electronics are (similar to vibration effects): component cracking (at lead entry points) and solder joint degradation. Due to the greater mismatch in coefficient of thermal expansion (CTE) between ceramic packages and PCB's (as compared to plastic packages), ceramic packages fail much earlier. For this reason (and where possible) plastic packaging should therefore be used instead of ceramic packages.

In order to maximize reliability, Dual-Inline Packages (DIP) or J-lead packages are recommended wherever possible. J-lead packages have been found to be the most reliability packaging format with respect to thermal cycle solder joint degradation [9, 13]. Other packaging formats such as Surface Mount Technology (SMT) have also been found to survive LEO missions, although these formats fail at half the thermal cycles (as compared to DIP) [24]. Ball Grid Array packaging is currently being investigated by NASA and ESA. There are indications that these packaging formats are comparable to SMT with respect to thermal cycling related failure.

To ensure that the satellite structure and components can survive the thermal stresses placed on them, a satellite is typically subjected to thermal cycle tests as part of the final qualification procedure (see [19] for a thermal test standard). The environmental tests performed on SUNSAT included a burn-in test with thermal extremes of $-25\text{ }^{\circ}\text{C}$ and $+55\text{ }^{\circ}\text{C}$. Tests with multiple cycles with thermal extremes of $-15\text{ }^{\circ}\text{C}$ and $+45\text{ }^{\circ}\text{C}$ were also be done [42]. The final thermal qualification consisted of a vacuum test at room temperature was done, as well as a vacuum test at $+45\text{ }^{\circ}\text{C}$ [41]. During these tests, RF communication anomalies were experienced (which were also experienced in-orbit on numerous occasions). None of the digital systems exhibited any anomalous behaviour.

Table {2.1} gives the maximum temperatures measured inside SUNSAT (from launch to end Oct 2000). The minimum temperature measured was $+8\text{ }^{\circ}\text{C}$, which was measured shortly after launch. The final thermal vacuum qualification test was thus the most representative of the orbital extreme thermal environment SUNSAT was subjected to. The non-vacuum thermal tests did however not stress the satellite to the levels experience in orbit. It is therefore recommended that the thermal vacuum tests of future satellites be done to the same limits as the burn-in test.

2.4 Corrosion and Atomic Erosion

All materials in LEO are subject to erosion from particles (single atoms and more complex molecules) [78, 7]. Atomic oxygen, created by the dissociation of molecular oxygen by ultraviolet radiation, is the primary corrosive agent in LEO [89]. The Mass-Spectrometer-Incoherent-Scatter (MSIS) neutral atmosphere model is currently the primary model used to predict the composition of the upper atmosphere [29, 30].

Inside a satellite, the densities of corrosive agents are relatively low due to the shielding provided by the satellite structure. Even these low levels can cause system failure when an unprotected device lead, PCB track or wire connection is corroded. Metal areas that have been weakened by cutting or bending are particularly prone to corrosion and a “conformal coating” is therefore applied to all PCB to protect them from contamination and corrosion. This coating covers all components and all sections of the PCB.

2.5 Spacecraft Charging

Satellites in all earth orbits experience various levels of charging [69, 21, 7]. The primary sources of spacecraft currents is the ambient space plasma and the solar extreme ultraviolet (EUV) flux. The ambient space plasma consists of electrons, protons and other ions. These can originate from the sun, outer space, or can be formed in that upper atmosphere due to ionization (see Chapter 3). A spacecraft in this environment will accumulate charges until an equilibrium is reached in which the net current is zero. The net current is the sum of currents due to ambient electrons and ions, secondary electrons and photo-electrons.

Two types of spacecraft charging is normally found. The first, called *absolute charging*, occurs when the entire spacecraft potential relative to the ambient space plasma is changed uniformly by the charging environment. The second type, called *differential charging*, occurs when certain parts of a satellite are charged to different potentials relative to each other. The primary effect of charging is sporadic electro-static discharge (ESD). Depending on the nodes between which the discharge occurs, the ESD can cause failure of subsystems, or the deterioration of spacecraft structure surfaces. In extreme cases, the discharges can cause spacecraft attitude disturbances.

To minimize charging on spacecraft, all conducting elements, surface and interior, should be tied to a common electrical ground. This can either be done directly (by ensuring that the contact DC impedance is less than $2.5 M\Omega$ [69]) or by means of a charge bleed-off resistor. Wherever possible, external surface material should be conductive.

For SUNSAT, no specific precautions were taken to limit charging. The structure of the satellite (cubical and made from a good conductor, aluminium) inherently limits charging on the main body of the satellite. The tipmass was also grounded with respect to the body of the satellite.

2.6 Micro-meteoroids and orbital debris

There are currently about 8,500 orbiting artificial objects [66]. These orbiting objects are however not the only objects that can impact a satellite. These object can contribute to secondary objects (e.g., lens caps, booster upper stages, nuts, bolts, paint chips, bits of foil, etc.). In addition, solid rocket motors spray out billions of tiny aluminum particles. Most artificial space objects are too small to be detected from the ground using conventional satellite tracking techniques. The smallest of the more than 8,500 objects in the USSPACECOM (formerly NORAD) catalog are about 10 *cm* across. There are estimated to be about 20 untrackable 1 *cm* objects and nearly 1×10^4 untrackable 1 *mm* objects for every trackable object. Artificial objects as small as 1 μm could number 1×10^{15} .

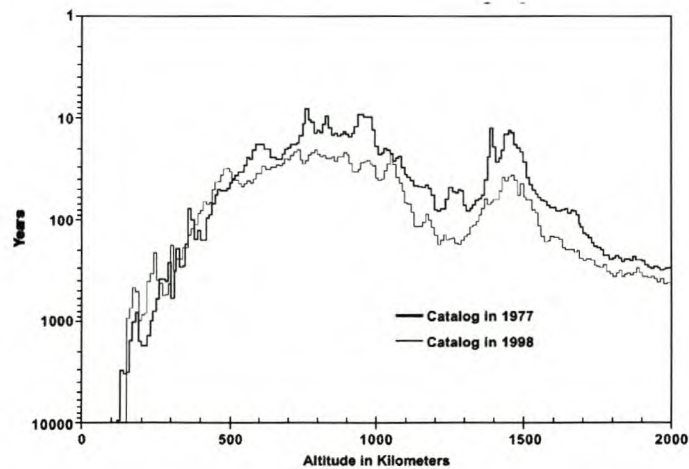


Figure 2.1: Rate that a Catalogued Object is Expected to Pass within about 100 meters of an Orbiting Spacecraft ([66], Fig 1).

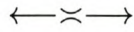
Fig. [2.1] gives an indication of the altitude dependency of the probability that catalogued objects will pass near or collide with a spacecraft. All of these objects have the potential to collide with other objects. The average speed of collision in LEO is $\approx 10 \text{ km/s}$. At that speed, a 1 *cm* object massing a few grams has sufficient kinetic energy to destroy a microsatellite. In GEO speeds are slower and the volume of space is larger, but objects stay in orbit in for longer periods of time.

The aluminium structure of SUNSAT (which is at a minimum 2 *mm* thick) was designed to provide sufficient protection against damage caused by micro-meteoroids [87]. Due to the lower probability of collision with large meteoroids, no special precautions were taken to protect against them. In the domain of low cost microsatellites, the primary defense against micro-meteoroids is the addition of redundancy to core subsystems. An additional precaution that can help minimize the damage of micro-meteoroids is to spacially distribute redundant subsystems and communication pathways. The damage from a micro-meteoroid impact may thus be limited to one subsystem, leaving the backup subsystem functional.

2.7 Comments

Various standards (MIL-SPEC, NASA, ESA, *etc.*) exist which specify procedures, design constraints, component selection criteria for satellites. The majority of these have been developed in a domain where relatively large budgets make large safety margins feasible. The fundamental motivation behind these standards can be of significant value for the design of an equivalent local/in-house standard, given that the standard can not be used directly due to budget constraints.

Such in-house standards are only of use if they are consistently applied. In the low cost domain, consistency can be a significant problem in its own right. The applicability of standards, whilst obviously being of great importance, should be determined during the system design phase as part of the system risk analysis.



Chapter 3

Radiation Effects on Semiconductors

The previous chapter discussed various environmental factors that could influence the design and operational performance of a satellite OBC. This chapter investigates the typical radiation environment in which a LEO satellite OBC will operate. As will be seen, the effect of radiation on the components from which an OBC is constructed can be significant.

For the subsequent discussion, a natural radiation environment is assumed. The impact of nuclear weapons on satellite systems will not be discussed. The hardening of satellite systems against nuclear weapons exceeds the scope/budget of small scale satellite projects (*i.e.* microsattellites).

3.1 Types, Origin and Effects of Radiation

The emission of energy as electromagnetic waves or as moving particles is referred to as radiation. The generic term “radiation” is used to describe a number of different kinds of radiation. To distinguish between these different kinds, a qualifier is normally used. The term “electromagnetic radiation” is therefore used to refer to the propagation of electromagnetic energy. Similarly, “proton radiation” refers to an incident flux of protons.

The different types of radiation can be grouped into two classes: *non-ionizing* and *ionizing* radiation. Ionizing radiation tends to cause the formation of ions (which change the densities of charge carriers) as it strips electrons from their parent atoms. Non-ionizing radiation, on the other hand, tends to cause structural defects. Unwanted radiation generally has disruptive effects on electronic systems [53]. The effect of radiation can be either “hard” (permanent damage) or “soft” (temporary damage, normally only results on loss of system state, *i.e.* information).

A concept often encountered when radiation is discussed is that of the process of *annealing*. This process refers to the partial or total self-healing of materials after irradiation. This process entails the recombination of ions particles (in the case of ionizing radiation damage) or the recombination of vacancy-interstitial atoms (in the case of neutron radiation damage, see Section 3.1.6). The first is generally a positive effect in that the device characteristics

return to their pre-radiation state. The latter can have either a positive (the recombination results in the restoration of the lattice integrity to pre-radiation levels) or negative effect (the recombination can result in the formation of stable impurity defects which can further degrade the device characteristics, see Section 3.1.6).

The following sections will examine the types of radiation that effect electronic systems. The nature, sources and effects of each will be discussed. Fig. [3.1] gives an indication of the relative radiation intensities that will typically be found inside a LEO microsatellite.

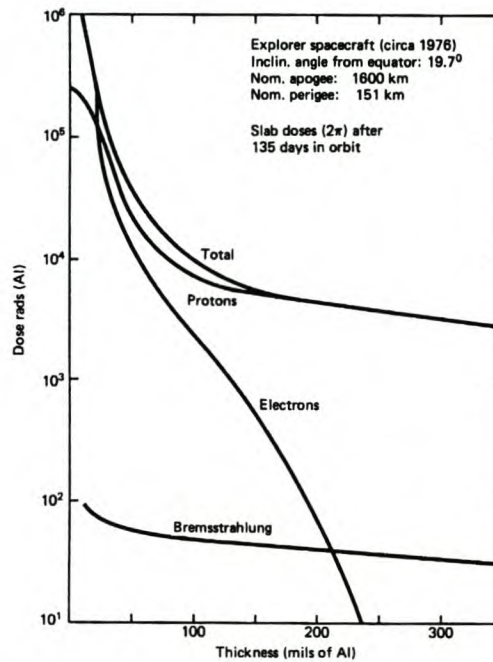


Figure 3.1: Dose-depth curves for the Explorer Spacecraft showing the penetration relationship between the various types of radiation ([53], Fig 13.2A).

3.1.1 X-Ray Radiation

X-rays are photons of a particular energy (and thus wavelength) and travel at the speed of light. These photons originate in two primary ways:

Firstly, they can originate when electrons fall into vacancies in the $n = 1$ or $n = 2$ levels of an atom. The vacancies themselves are normally created by high energy electrons which knock out electrons from the $n = 1$, $n = 2$ or $n = 3$ levels. The x-rays so generated have wave-lengths characteristic of the energy differences between the various levels within the atom. That is, the emitted photons carry an energy equal to the difference in energies between the two levels which act as the starting point and end point for the electron which falls into the vacancy. X-rays emitted by this process is referred to as *characteristic x-rays*.

Another type of x-ray is emitted from a target when it is bombarded by electrons and

is referred to as *bremstrahlung*, from the German “braking radiation”. This radiation is caused by the deceleration of a moving charge, which produces radiation similarly to that caused by accelerating charges. Unlike characteristic x-rays, *bremstrahlung* has a continuous range of wavelengths, reflecting the fact that deceleration can occur in a nearly infinite number of ways. As x-rays and γ -rays are similar, refer to Section 3.1.2 for further insight.

X-radiation is an ionizing radiation (*i.e.* charged particles are produced). Photons (X-rays and gamma rays) interact with atoms through the following three processes [53, 32, 90]:

- ① A photon can strike an electron, lose all its energy to it, and simply disappear. This is called the *photo-electric effect*.
- ② The photon can also collide with an electron and be scattered to one side. This is known as the *Compton effect*.
- ③ The last and most complex is called the *pair production*. Under certain conditions a photon in the vicinity of a nucleus will disappear. In its place will appear two particles, an electron and a positron.

The material changes produced are: conductivity increases through the production of excess charged carriers (electrons and holes), trapped charges in insulators, production of electric and magnetic fields and chemical effects.

In the LEO satellite environment the ambient intensity of x-rays is generally low. Characteristic x-rays can however be produced as the by-product of other forms of radiation. For example, it is possible that gamma radiation could cause electrons in the $n = 1$ and $n = 2$ levels to be knocked out (from the atoms in the satellite materials). This creates a situation where characteristic x-rays can be produced, as described above. During a solar flare, x-rays can also be produced, but at relatively low intensity levels. X-rays can therefore be considered of relatively minor importance in the satellite environment and are typically not included in LEO radiation studies.

3.1.2 Gamma (γ) Radiation

Gamma radiation also consists of high energy photons, similar to x-rays. However, in the case of gamma radiation, the photons are caused by energy level changes within the nucleus of the atom. Gamma radiation is therefore produced by unstable atomic nuclei (*isotopes*).

In the satellite environment, the Sun is the primary source of gamma radiation and is created during the fusion reactions inside the Sun. The photons in gamma radiation can undergo similar interactions with materials as does x-rays (photoelectric effect, Compton scattering and pair production). The effects of gamma radiation are therefore similar to that of x-rays, the only differences being related to the high energy levels of gamma photons.

3.1.3 Alpha (α) Radiation

The nucleus of a helium atom (*i.e.* helium ion: He^{++}) is called an *alpha* (α) *particle* (for historic reasons). When an unstable heavy atomic nuclei decays, one of the by-products is radiation consisting of alpha particles. It has been shown [52, 43] that trace amounts of radioactive uranium and thorium in IC packaging decay to produce high energy alpha particles. The occurrence of this decay is however rare compared to the flux densities of external radiation sources. In the LEO environment, the primary source of alpha radiation is the secondary radiation produced by Galactic Cosmic Rays (Section 3.1.7).

Due to the charged nature of alpha particles (double that of a proton), alpha radiation is a highly ionizing form of radiation. This implies that alpha radiation tends to have relatively low penetration ability as the particles lose energy rapidly due to the ionization. Due to the limited penetration ability, alpha radiation is not of significant concern in LEO orbits (a typical satellite skeleton will attenuate alpha radiation to very low dose levels).

3.1.4 Beta (β) Radiation

Beta radiation is simply high energy electrons. The source of these electrons however defines their being called beta radiation. These electrons are created inside the nucleus when a proton transforms into a neutron. A *neutrino* (neutral particle with \sim zero mass) is also emitted during this transformation. Due to the low mass of electrons, they are relatively easily deflected in materials. Their penetration ability is therefore limited (see Fig. [3.1]).

3.1.5 Proton (H^+) Radiation

Proton radiation consists of, as the name implies, protons moving at high speed. Proton radiation originates from radioactive decay and nuclear reactions (typically the fusion reactions inside stars). Proton radiation is a highly ionizing form of radiation. Due to the significant mass of protons, they also have considerable penetration ability. Proton radiation is the primary form of radiation that affects satellites in LEO.

3.1.6 Neutron Radiation

Neutron radiation originates from radioactive decay and nuclear reactions (typically the fusion reactions inside stars). A neutron, because it is uncharged, does not undergo Coulomb-type (electro-static) collisions. Neutron radiation is thus the primary form of non-ionizing radiation found. For a neutron to be deflected, it must strike a nucleus or other particle, not just interact with it from a distance. As a result, neutrons travel long distances between collisions.

The damage caused by neutron radiation consists of displacement damage and secondary ionization [32]. Displacement damage results when a neutron collides with the lattice atoms of a semiconductor, dislodging or displacing whole atoms from their lattice sites, causing

them to take up interstitial positions within the crystal [53]. The former site of the now displaced atom in the lattice is called a vacancy. The interstitial-vacancy pair are called a *Frenkel defect*. If the energy of the incident neutron is sufficiently large, it can impart enough energy to the displaced atom for it, in turn, to displace other atoms in the lattice. The vacancies created can combine with impurity atoms, donor atoms, or other vacancies present to produce stable defects that can effect recombination rates (which effects carrier lifetimes) and cause resistivity changes.

Neutrons, being uncharged, cannot directly cause ionization. However, they can indirectly cause ionization through secondary processes such as (and is said to cause *secondary radiation*):

- ① Neutron collisions that produce recoil atoms or ions, which in turn produce ionization,
- ② Neutron collisions that excite atomic nuclei, which de-excite by emitting gamma rays that can ionize,
- ③ Neutron collisions where the neutron is absorbed by a target atomic nucleus, which (now being an isotope) decays by emitting a charged particle (in silicon this results in either α particles or protons being emitted).

On bipolar transistors, the effect neutron radiation is linked with displacement damage. Neutron radiation results in changes in minority carrier densities by altering the minority carrier lifetimes. As bipolar transistors are minority carrier devices, this causes the current gain of bipolar transistors to degrade. Leakage current is largely unaffected by neutron radiation. MOS transistors, being majority carrier devices are largely unaffected by neutron radiation. Neutron radiation therefore is not of primary concern for CMOS based electronics in LEO environments. The effect on bipolar devices can however prove to be significant and the use of these devices must take into account the possible device changes induced by neutron radiation.

3.1.7 Cosmic Radiation

The term “Cosmic Radiation” is a generic term that refers to high speed/energy particles that are found in different intensities throughout the universe. This type of radiation is also referred to as *Galactic Cosmic Rays* (GCRs). These high energy particles are created by the fusion reactions inside distant stars [11].

The composition of cosmic rays is as follows: 85 percent are protons, 14 percent are alpha particles, and 1 percent are heavy ions. The flux 1 AU from the Earth is $\approx 4 \text{ particles.cm}^{-2}.s^{-1}$ during solar minimum (Section 3.2.2) and $\approx 2 \text{ particles.cm}^{-2}.s^{-1}$ during solar maximum [83], with energies from almost 0 to over 10 *GeV*. Hydrogen, carbon and oxygen ions are the bulk of the heavy ions, peaking at energies around 1 *GeV*, while ions with atomic numbers above 26 are rarely observed.

Due to the charged nature of the radiation ions, cosmic rays can cause direct ionization similar to protons. In addition, if a high energy cosmic radiation particle strikes an atom it normally produces a shower or cascade of particles and secondary radiation (*i.e.* it can shatter the atom). The effect is therefore an extreme case of the ionization produced by the preceding radiation types. This kind of radiation therefore tends to be extremely disruptive. Due to their high energy, cosmic rays are difficult to shield against.

3.2 Radiation Regions

There are a number of areas near the Earth that have unique radiation characteristics. The following section will examine these regions and discuss the types of radiation found in each. The orbit of a satellite may intersect more than one of these regions. Section 3.7 will describe the radiation nature of the common orbit types.

3.2.1 Solar Wind

The solar wind consists primarily of low-energy (keV) protons and high-energy electrons [82] ejected by the Sun. The time variations in the density and velocity of the solar wind protons are relatively small. During a solar flare however, a flux of high energy protons (MeV) is emitted (See Section 3.2.2). The intensity of the solar wind generally increases subsequent to periods of intense solar flares and can remain high for a number of weeks. Fig. [3.2] gives a diagrammatical representation of the solar wind and how it interacts with the Earth's magnetosphere (see Section 3.2.3).

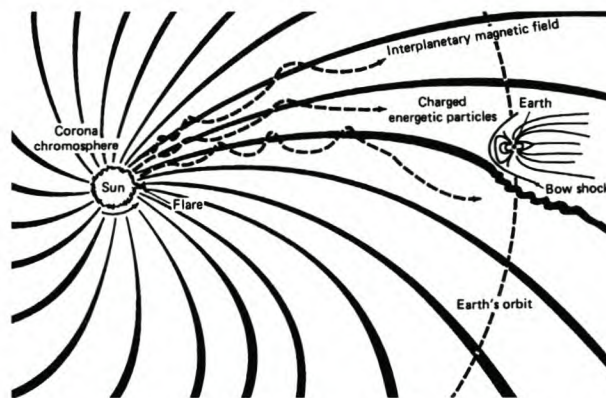


Figure 3.2: The Earth's magnetosphere in the solar wind, showing the interplanetary magnetic field and the emanating solar wind particles ([53], Fig. 12.29A).

3.2.2 Solar Flares

Solar flares are the result of periodic variations in the nuclear reactions of the chromosphere of the Sun. At times of high chromosphere activity, large quantities of particles are released and these events are called Coronal Mass Ejection (CME) events. Solar flare particles are largely protons ($> 90\%$) together with alpha particles and some heavier nuclear components (C, N, O group prominent). These large, sudden fluxes occur sporadically, at about three times per year. The heaviest doses occur 10 to 12 years apart, according to the solar flare cycle [82, 92]. In a typical burst, the flux peak occurs between 2 and 24 hours after its origin and decays over a period of a few days. Heavy ion fluxes from solar flares are usually far below the nominal galactic background radiation levels, but they can be up to four orders of magnitude above the background during some flares.

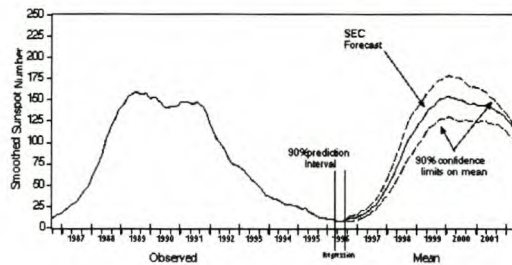


Figure 3.3: Predicted sunspot activity based on 1996 data (obtained from Space Effects Center, NASA).

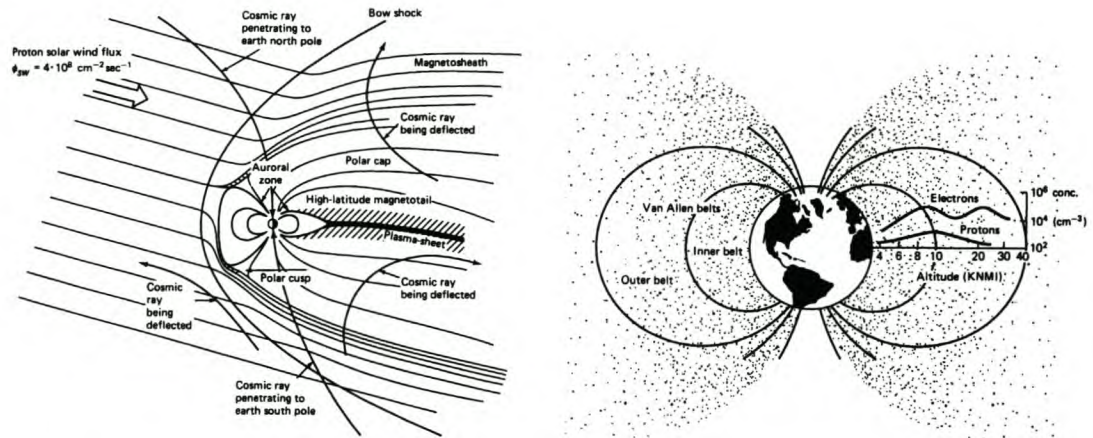
As can be seen from Fig. [3.3], a period of increased sunspot activity has recently been entered. The increase in sunspot activity effects the Earth's magnetosphere in such a way as to maximize the shielding effect of the magnetosphere ([53], p437).

3.2.3 The Van Allen Belts

The Van Allen belts (see Fig. [3.4](b)) consist of electrons and protons trapped in the geomagnetic fields (called the *magnetosphere*) of the Earth. The Van Allen Belts also contain low concentrations of heavy ions. The belts occupy a distorted toroid volume of space about the Earth (see Fig. [3.4](a)), from about 300 km to about 59,000 km altitude. The distortion of the magnetic field is caused by the solar wind.

Particles that approach the Van Allen belts are either deflected, or are captured by the belts and become trapped. These particles oscillate north-south along the field-lines of the magnetosphere. This occurs because the converging field-lines at the magnetic poles act as a magnetic mirror, reflecting the particles back and forth [83, 81].

The trapped electrons are classified into inner and outer zones, divided at a distance of about 2.5 Earth radii from the Earth's surface (see Fig. [3.4](b)). The flux of electrons in the outer zone is about 10 times that of the inner zone, with outer zone electron energies of about 7 MeV and inner zone energies of less than 5 MeV. Proton energies vary



(a) The magnetosphere in the noon-midnight meridian plane showing cosmic ray trajectories and the solar wind ([53], Fig. 12.29).

(b) Van Allen belts showing the trapped electrons and protons ([53], Fig. 12.30B).

Figure 3.4: The magnetosphere containing the Van Allen belts

approximately inversely with altitude and can have energies over 400 MeV close to the Earth (and are therefore the most important component of the inner Van Allen belt).

In the southern hemisphere, the Earth's magnetic field is offset by approximately 11 degrees from the Earth's axis, and displaced about 500 km toward the Western Pacific. Hence, there is a polar-like dip in the magnetic field in the vicinity of Brazil, wherein the magnetic field lines reenter the Earth. This not only produces a singularity in the magnetic field for cosmic rays to intrude, but also allows the Van Allen belts to extend down into the atmosphere of the Earth. This *South Atlantic Anomaly* (SAA, see Fig. [3.5]) is responsible for most of the Van Allen Belt radiation received by spacecraft in low and very low Earth orbit altitudes [56]. In the last 10 years the size of the SAA has increased and drifted westward [16, 32].

3.3 Overview of Effects

Most materials used for the construction of satellites are relatively unaffected by radiation exposure. Passive electronic components such as resistors and capacitors (with chip capacitors being an exception) generally do not experience any degradation in characteristics due to radiation exposure. Components that are manufactured using similar techniques to those used to produce integrated circuits are however susceptible to effects such as trapped charges in insulators. These effects may or may not result in a change in the electrical characteristics of the devices.

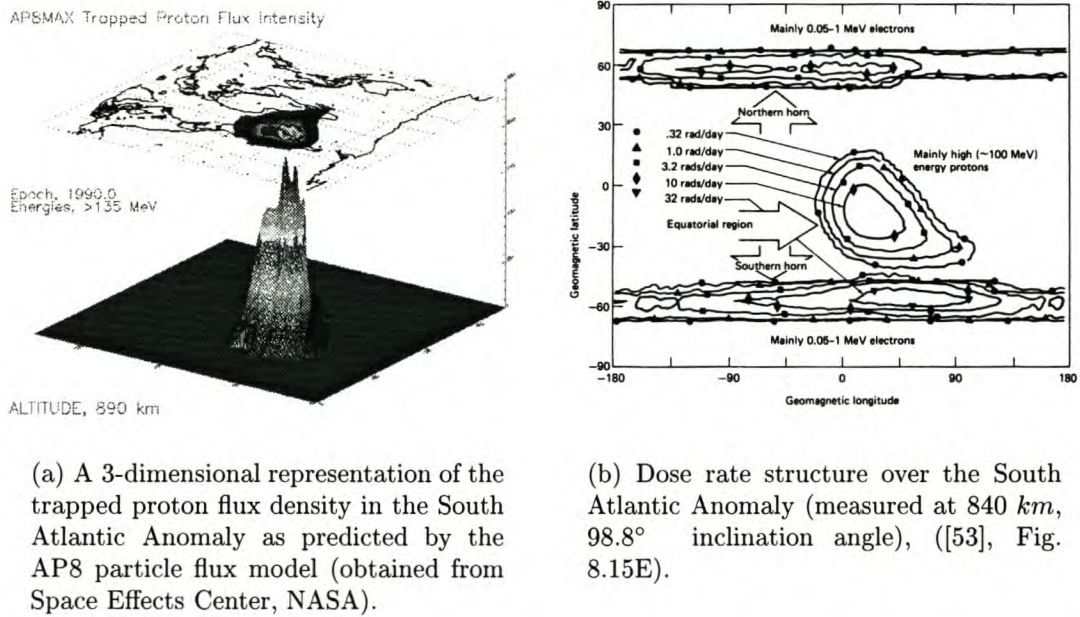


Figure 3.5: The South Atlantic Anomaly

3.4 Field Effect Transistors

The FET family of semiconductor transistors form the dominant transistor used in digital circuits. For a better understanding of the effect of radiation on these devices, this section presents a brief revision of the basic structure and characteristics of FET devices. The most basic form of FET device is the n -channel JFET (Fig. [3.6]) and this will therefore serve as starting point.

Physically a n -channel JFET consists of a channel of n -type semiconductor with a *source* S at one end and a *drain* D at the other end. The drain source current, I_D , flows through the channel. The n -channel lies between two p -type regions whose common terminal is called the *gate*, G . These two p -type regions form two $p-n$ junctions, one on either side of the channel. For a common source configuration, the two gate-channel $p-n$ junctions are reversed biased. For a positive source-drain voltage, a source to drain current flows. This current consists only of majority carriers (electrons in the case of a n -channel JFET). The magnitude of this current is controlled by the electric field across the gate-channel interface.

The charge typically induced by sporadic ionizing radiation is comparatively small compared to the charges involved in the normal operation of the device. JFET devices are therefore not significantly affected by the nominal ionization radiation found in typical satellite environments. Large impulses of ionization radiation can however cause brief current impulses in the devices. Non-ionizing radiation similarly does not have a significant effect on JFET devices as the resultant characteristic changes are minor.

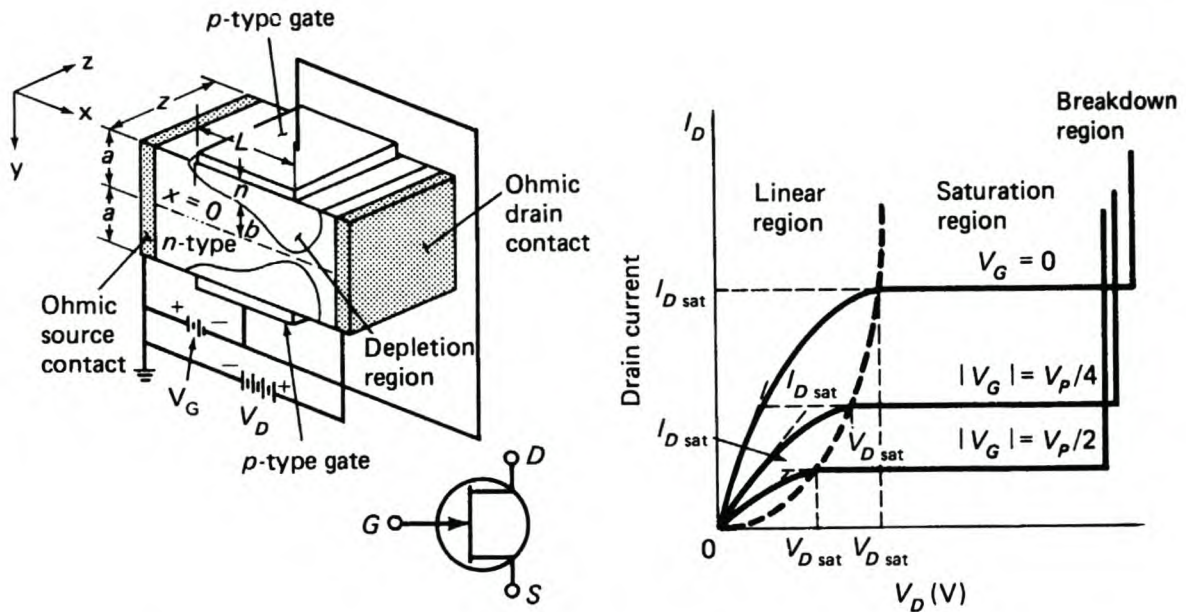


Figure 3.6: *N*-channel JFET depicting its structure and characteristic curves ([53], Fig. 6.4).

Another type of FET is the insulated gate FET or MOSFET (metal-oxide semiconductor field effect transistor). There are two types MOSFET, the depletion mode device and the enhancement mode device, and each can possess a *p*-channel or a *n*-channel. The important characteristic of the MOSFET is that in the depletion mode, the built-in channel is normally on. Of central importance is the silicon dioxide (SiO_2) insulator layer parallel to and astride the length of the channel called the gate oxide, upon which is deposited a metal contact. This is called the gate terminal and the gate system is referred to as a *metal gate*. A *polysilicon gate* uses heavily doped polysilicon as the gate terminal instead of metal. When a positive bias is applied to the gate, it induces an electric field in the oxide layer of such polarity that it repels (depletes) the holes in the normally-on channel below. This decreases the effective conductivity of the channel.

The enhancement mode MOSFET differs from the depletion mode MOSFET in that it does not have a built-in channel and is normally off with zero gate bias. Instead, the gate electric field ($+V_G$ for *n*-channel, $-V_G$ for *p*-channel) enhances the conductivity of the substrate directly under the oxide layer, to induce a channel there by attracting corresponding mobile carriers from the substrate. The term *threshold voltage* refers to the gate voltage required to initiate conduction.

The most widely used implementation of FET devices is the Complementary MOS (CMOS) device (see Fig. [3.7]). This device combines a *p* and *n* channel (enhancement mode) transistor pair on the same substrate. This arrangement, as used in high speed circuitry, dissipates significant power only during change of state.

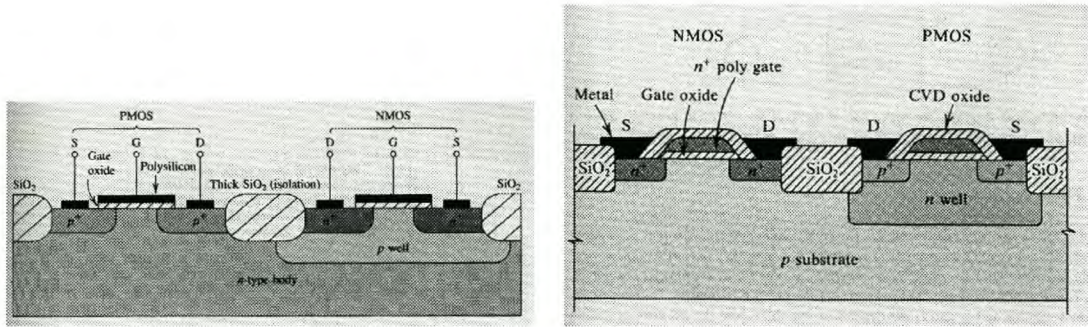
(a) *p*-well technology ([74], Fig. 5.8).(b) *n*-well technology ([74], Fig. A.11).

Figure 3.7: Cross section of a CMOS integrated circuit showing the PMOS and NMOS transistors

The primary effect of ionizing radiation on MOSFET devices is on the threshold voltage. If radiation such as gamma rays, x-rays, or electrons, is incident on an insulator, the injected electrons, or those produced within the material through ionization result in the buildup of trapped charges (holes and electrons) in the insulator. The electrons are rapidly swept out due to their mobility. The holes undergo a relatively slow transport through the insulator. These charges and their neutralizing charge counterparts, which are manifest on the nearby conductors, result in the generation of an electric field. As the electric field strength increases with the production of these charges, electrical breakdown of the insulator can occur. In insulators, these trapped charges can persist for days. These trapped charges thus have two effects: shifts in the threshold voltage and the possibility of electric breakdown of the insulator. The former causes changes in the electrical characteristics of the device. The latter can lead to latchup (Section 3.5.1).

In a typical CMOS digital device, two FET transistors are normally found in a totem pole configuration (Fig. [3.8]). Normally one of the transistors is inactive whilst the other is active. The threshold voltage shift can cause an increase in the leakage current in the inactive transistor. This effectively creates a path from V_{CC} to V_{SS} , albeit with a high resistance. The increase in leakage current is relatively small and the functional characteristics are not significantly altered. Due to the large number of such totem pole configurations in a typical integrated circuit, the accumulative effect of the increased leakage current I_K is therefore a noticeable increase in power consumption of the device. As the voltage drift increases, the power consumption of the device continues to rise. As the power consumption of the device continues to increase, the functional characteristics of the device eventually begin to degrade. There is therefore a limit to the functional lifetime of CMOS devices in the space radiation environment.

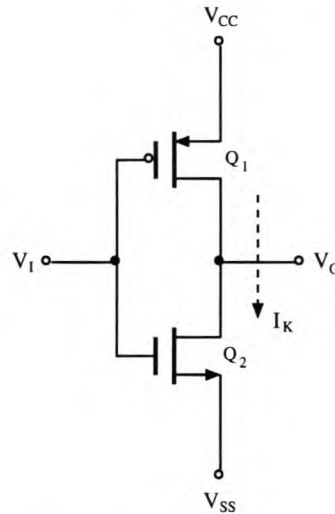


Figure 3.8: Totem pole configuration commonly found in the output stage of logic gates in CMOS integrated circuits

3.5 Macro Effects on Semiconductors

The previous section has provided a brief overview of the effect of radiation at the microscopic device level. The macro, perceived effects that radiation can have on semiconductors are normally classified into groups and these classification groups are described in the following section. Note that some of these groups are supersets of other groups mentioned.

3.5.1 Single Event Latchup (SEL)

The general definition of latchup is that the semiconductor device of interest is transformed to an anomalous state in which it no longer responds to input signals. If this anomalous state does not cause device burn-out due to excessive current flow within the device, the device can be restored to its functional state by power cycling. In integrated circuits, the cause of latchup is typically parasitic transistors formed by the real transistor and the device substrate. Under certain conditions (*e.g.*, significant shifts in threshold voltage) this parasitic transistor can become switched on and cause excessive current flow. These currents flow in localized regions where the latchup is triggered and can rapidly heat that section to high temperatures [38].

3.5.2 Single Event Upset (SEU)

In the context of electronic devices, an upset is taken to mean the unwanted change of state or transient functionality of the device. Upsets fall in the group of “soft errors”. In the case of a memory device, an upset implies the unwanted change of information stored in the memory devices. Upsets cause no damage or degradation in the device.

The term *Single Event Upset* refers to random, isolated, logic upset errors. Their random nature stems from their source: they are caused by the spurious charge produced by the transit of a single ionizing particle passing through the device. The single event upset frequency or single event upset bit error rate increases with the packaging density of the particular device. To enhance performance, especially to increase speed of operation, manufacturers tend to produce smaller devices, thereby increasing the packaging density. This in turn increases the SEU susceptibility of the device.

3.5.3 Single Event Functional Interrupt (SEFI)

This refers to a subclass of SEU where the upset occurs in the control circuitry of a devices. The device subsequently halts normal operation; going into a test mode, a halt or undefined state. Often the device requires a power reset to recover.

3.5.4 Single Event Dielectric Rupture (SEDR)

These errors are specific to anti-fuse cells they will be discussed in Section 3.10.3.3.

3.5.5 Single Event Disturb Errors (SEDE)

These errors are specific to 4-Cell SRAM's they will be discussed in Section 3.9.3.

3.5.6 Single Event Hard Error (SEHE)

This refers to an event that results in permanent damage of the device. Subsequent to such an event, the device ceases to function according to specification. A common example would be a stuck bit in a memory devices. Power cycling does not restore the damage.

3.5.7 Single Event Gate Rupture (SEGR)

In the case of high power MOSFET's, an intense pulse of ionizing radiation can cause currents to flow in the device that can cause destructive burn-out of the gate insulator [58].

3.5.8 Single Event Multi-Bit Effects (SEMBE)

Under certain conditions the passage of a single ion through a device can cause multiple upsets. This could happen, for instance, in the case of a memory device when the angle of incident of the particle track is such that it intercepts multiple memory cells. Fortunately it has been found that in the LEO environment, the occurrence of SEMBE is very rare.

3.5.9 Single Event Induce Dark Currents (SEIDC)

This SEE is specific to Charge-Coupled Devices (CCD) and causes an increase in dark currents, which causes certain pixels in the CCD to become unusable. The Tipmass Star Camera of *SUNSAT* exhibits an effect that appears to be typical of SEIDC.

3.5.10 Single Event Transients (SET)

In addition to the effect on storage cells, single event interactions can produce transient output pulses in combinatorial logic circuits that do not contain internal storage elements [57]. These transients are usually of short duration (≈ 1 ns), but may indirectly produce changes in the state of other circuits if they occur at critical time periods (such as during clock or data transitions).

3.6 Radiation Hardness Definitions

The radiation tolerance of components and systems are typically given with respect to three primary response domains. This section provides a brief definition of these three response domains as used in subject literature.

3.6.1 Total Ionization Dose (TID)

The total dose hardness of an integrated circuit is a measure of its ability to withstand accumulated doses of radiation. As was mentioned in Section 3.4, the ionizing radiation causes trapped charges in the insulation oxide. These charges results in shifts in the threshold voltage V_{TH} of the device. As these charges may remain trapped in the oxide for extended periods, the amount of trapped charge tends to increase with time. This causes a gradual increase in the power consumption of the device (Section 3.4). For example, a *total dose hardness* of 10 *krad(Si)* indicates that the devices will experience negligible radiation related power consumption variation until a total dose of 10 *krad(Si)* has been absorbed. Beyond this point the power consumption increases significantly. For reference, Table {3.1} gives the typical yearly dose rate for the standard orbits of space vehicles. Note that these rates vary with solar output.

The devices which are most susceptible (in a LEO environment) to total dose effects are precision reference devices [70, 4]. The effect seen is a gradual increase in inaccuracy in the device and occurs even in low dose rate environments (there are indications that low dose rates are particularly degrading to linear devices (bipolar, BiCMOS and CMOS) such as operational amplifiers [37, 47, 60, 45, 62]).

On *SUNSAT*, slight increases in average supply current has been seen in the Telemetry subsystem (< 10% increase). No other subsystems showed any increase in average supply currents.

Table 3.1: Typical Dose Rate in Various Orbits [50]

Orbit	Height	Inclination	Dose Rate (per year)
Low Earth	200 – 1000 km	< 28°	100 – 1k rad(Si)
Low Earth	200 – 1000 km	> 28°	1k – 10k rad(Si)
Medium Earth	1000 – 4000 km	any	100 krad(Si)
High Earth	≈ 36000 km	any	> 10 krad(Si)
Interplanetary	n/a	n/a	5k – 10k rad(Si)

3.6.2 Transient Dose

Transient dose refers to the radiation dose rate. High radiation dose rates are responsible for SEL (Section 3.5.1). High dose rates can also cause data corruption in storage elements due to the inability of the power rail to hold up the voltage on a node sufficiently to maintain the data (called *power rail collapse*). The power rail voltage drop is as a result of the transient photo-current pulse generated by a burst of ionization. A dose rate of 1 krad (Si).s⁻¹ therefore indicates that the device will perform within specification (both functional and physical) when a dose of 1 krad (Si) is absorbed per second.

3.6.3 Single Event Effects (SEE)

The rate at which SEE occur is used as a measure of the sensitivity of a device to radiation. For cosmic rays, SEEs are typically caused by its heavy ion component. These heavy ions cause a direct ionization SEE, i.e., if an ion particle traversing a device deposits sufficient charge an event such as a memory bit flip or transient may occur.

Protons, usually trapped in the earth's radiation belts or from solar flares, may cause direct ionization SEEs in very sensitive devices. However, a proton may more typically cause a nuclear reaction near a sensitive device area, and thus, create an indirect ionization effect potentially causing an SEE.

3.7 Orbit Environments

There are extremely large variations in the levels of SEE inducing flux levels that a given spacecraft encounters depending on its trajectory through the radiation sources. Some of the typical orbit configurations are discussed below.

3.7.1 Low Earth Orbits (LEOs)

The most important characteristic of the environment encountered by satellites in LEOs is that several times each day they pass through the particles trapped in the Van Allen belts [84]. The amount of protection that the geomagnetic field provides a satellite from the cosmic ray and solar flare particles is also dependent on the inclination and to a smaller degree the altitude of the orbit. As altitude increases, the exposure to cosmic ray and solar flare particles gradually increase.

The greatest inclination dependencies occur in the range of $0^\circ < i < 30^\circ$. For inclinations over 30° , the fluxes rise more gradually until about 60° . Over 60° , the inclination has little effect on the flux levels. As the inclination increases, the satellite spends more and more of its time in regions of high particle concentration. As the inclination reaches polar regions, it is beyond the geomagnetic field lines and is fully exposed to cosmic ray and solar flare particles for a significant portion of the orbit.

The largest altitude variations occur between 200 to 600 *km* where large increases in flux levels are seen as altitude increases. Over 600 *km* the flux increase with altitude increase is more gradual. The location of the peak fluxes depends on the energy of the particle. For protons with $E > 10 \text{ MeV}$, the peak is at about 3000 *km*. For normal geomagnetic and solar activity conditions, the flux levels drop rapidly at altitudes over 3000 *km*.

Under normal magnetic conditions, satellites with inclinations below 45° will be completely shielded from solar flare protons. During large solar events, the pressure on the magnetosphere will cause the magnetic field lines to be compressed resulting in solar flare and cosmic ray particles reaching previously unattainable altitudes and inclinations. The same can be true for cosmic ray particles during large magnetic storms.

3.7.2 Highly Elliptical Orbits (HEOs)

Highly elliptical orbits are similar to LEO orbits in that they pass through the Van Allen belts each day. However, because of their high altitude, they also have long exposures to the cosmic ray and solar flare environments regardless of their inclination. The levels of trapped proton fluxes that HEOs encounter depend on the perigee position of the orbit including altitude, latitude, and longitude. If this position drifts during the course of the mission, the degree of drift must be taken into account when predicting proton flux levels.

3.7.3 Geostationary Orbits (GEOs)

At geostationary altitudes, the only trapped protons that are present are below energy levels necessary to initiate the nuclear events in materials surrounding the sensitive region of the device that cause SEEs. However, GEOs are almost fully exposed to the galactic cosmic ray and solar flare particles. Protons below about 40 – 50 *MeV* are normally geomagnetically attenuated, however, this attenuation breaks down during solar flare events and geomagnetic storms. Field lines that are at about 7 earth radii during normal con-

ditions can be compressed down to about 4 earth radii during these events. As a result, particles that were previously deflected have access to much lower latitudes and altitudes.

3.8 Predicting SEU, SEL and TID

Due to the impact of the SEU, SEL and TID on electronic systems, there have been extensive studies into predicting the SEU, SEL and TID rates that space vehicle electronics will be exposed to. From these studies a number of models [65, 63]¹ have been derived that attempt to predict the these effects on electronic systems.

In order to predict the effect of radiation on a satellite subsystem, the following procedure is typically followed:

- ① By means of a numerical model, predict the expected radiation fluence in the target orbit during the satellite lifetime.
- ② Calculated the estimated radiation fluence incident on the subsystem. This is done by using a nuclear particle transportation model with a finite element model (FEM) of the satellite structure (to incorporate the shielding effects of the structure) and the external fluence as inputs.
- ③ Determine the expected TID, SEU and SEL rates using experimental data from the lot radiation characterization of the components that constitute the subsystem (given the incident fluence).

It should be clear from the above that the prediction of radiation effects requires considerable modeling effort, is numerically intensive, and relies on the availability of suitable fluence prediction models. Furthermore extensive experimental data on the components must be available. This procedure can therefore only be applied for some projects and is considered infeasible for others.

Models for the prediction of fluence have been implemented in computer code and are available for general use. Some of these computer models are given in Table {3.2}. These models are the result of decades of studies and the models have widely varying confidence levels. Commercial software application exists which can perform steps one and two of the radiation analysis procedure. Three such application are: Environmental Workbench (from NASA), SimEnv (from Microcosm) and Space Radiation (from Severn Communication Corp.). These implement various of the models given in Table {3.2}.

Recent studies [84] have however found that the accuracy of a number of the models have been significantly overestimated (particularly with regards to dynamic events such as the 11-yearly solar maximum). The models for Galactic Cosmic Radiation are also

¹[63] is considered a reference paper with regards to the nature and effects of proton radiation. As proton radiation is the primary cause of radiation related LEO anomalies, this paper is of particular importance (“classical paper”) when proton related studies are initiated.

Table 3.2: Computer based Radiation Models

Source	Models	Solar Effects	Variations	Orbits Affected
Trapped Protons	AP8-MIN AP8-MAX	Solar Min - Higher; Solar Max - Lower	Geomagnetic Field, Solar Flares, Geomagnetic Storms	LEO, HEO, Transfer Orbits
Trapped Electrons	AE8-MIN AE8-MAX	Solar Min - Lower; Solar Max - Higher	Geomagnetic Field, Solar Flares, Geomagnetic Storms	LEO, GEO, HEO, Transfer Orbits
Galactic Cosmic Ray Ions	CREME CHIME	Solar Min - Higher; Solar Max - Lower	Ionization Level, Orbit Attenuation	LEO, GEO, HEO, Interplanetary
Solar Flare Protons	KING JPL92	During Solar Max Only	Distance from Sun; Outside 1 AU, Orbit Attenuation; Location of Flare on Sun	LEO ($I > 45^\circ$), GEO, HEO, Interplanetary
Solar Flare Heavy Ions	CREME JPL92 CHIME	During Solar Max Only	Distance from Sun; Outside 1 AU, Orbit Attenuation; Location of Flare on Sun	LEO, GEO, HEO, Interplanetary

now considered outdated and should be used with care [64]. Similarly, the empirical solar cycle models have had limited accuracy and have been supplemented by a statistical model [92]. These developments reduce the usefulness of the results of predictions based on these models. New models are therefore required and work is underway to update the existing models and to develop new models (e.g., [93]).

The models used in Step 2 primarily solve the transportation problem by means of a numeric approximation of the Boltzmann transport equation [48, 91, 90]. A number of these numeric approximations exist (semi-analytical, Monte Carlo MC [76], etc.) and the particular approximation used is determined by the resultant characteristics desired and the available computation resources. The MC based methods are particularly computationally intensive, requiring massively parallel processors and systolic arrays to produce results in realistic time. These models require as input extensive data sets that describe the cross-sectional response of various elements to various incident particles (protons, neutrons, photons, electrons).

No radiation related modeling was done during the design of SUNSAT. The creation of a complete radiation model exceeds the scope of most small scale microsatellite projects. This is further complicated by the fact that the LET and SEU Cross Sections of the devices used (low cost, non-radiation, commercial grade) in the designs are generally not known. If the availability and reliability, as well as time and budget impact are sufficiently stringent, the creation of such a model may be necessitated.

3.9 Semiconductor Memory Devices

In the preceding sections the effects of radiation has been discussed. This discussion has been fairly general with respect to the CMOS family. If one examines the CMOS family itself, one finds that there are certain devices that are considerably more sensitive to SEE than others. In particular, CMOS memory devices are of particular importance as they form a significant part of OBCs and are the most SEE sensitive devices in an OBC. This section gives a short overview [74] of selected CMOS Memory devices and describes how they are effected by radiation.

3.9.1 Standard DRAM devices

A Dynamic RAM device is an example of a high density memory device. The binary data is stored in the form of charge on the cell capacitor (see Fig. [3.9](a)). A logic 1 is represented by the presence of charge (hence voltage); a logic 0 is represented by the absence of charge (hence 0 V). The transistor is called the *access transistor* and is used to access the information stored in the memory cell.

Due to the various leakage effects that are present, the capacitor charge will leak off. The charge must therefore be continually restored. This process is called a memory *refresh*. The refresh is performed by reading the cell contents and rewriting it to the cell.

Due to the simplicity of the memory cell, a typical DRAM package can contain a very large amount of cells. The small size of the memory cell makes DRAM devices very sensitive to SEU. Ionizing particles that pass through the capacitor will induce charge that will disrupt the charge stored on the capacitor and will lead to information corruption. The data retention times of DRAM devices also decrease with radiation [75]. DRAM devices can there not be safely used in space unless special precautions are taken to improve the radiation tolerance of the device (or compensate for the resultant degradation). One way in which this is done is to add an Error Detecting and Correcting (EDAC) circuit to the design.

Next generation DRAMs show improved SEU characteristics and the primary reason for this is the reduced oxide thickness due to device scaling [46]. Unfortunately, recent experiments have shown evidenced of a new type of radiation damage, that particularly effects newer generations of DRAM devices. This effect, microdose, is largely due to the increased scaling of devices (high density, low feature size). It has been postulated [4] that the microdose effect is similar to the total dose effect, affecting a particular cell permanently. Another effect, that will ultimately limit the use of scaled devices in space, is a variation on the SEDR and SEGR effect seen [36] (this effect is also significant for on-chip capacitors, which also exhibit SEDR).

Low density DRAM devices can therefore, when suitable precautions have been taken, be used in a LEO satellite environment. Due to the required refresh cycles, the average power requirements of DRAM devices can be considerably higher than that of other memory devices. The new 3.3V devices are particularly attractive and deserve serious consideration

in during the design of solid state mass storage devices for LEO satellite use (see [22] for examples of use).

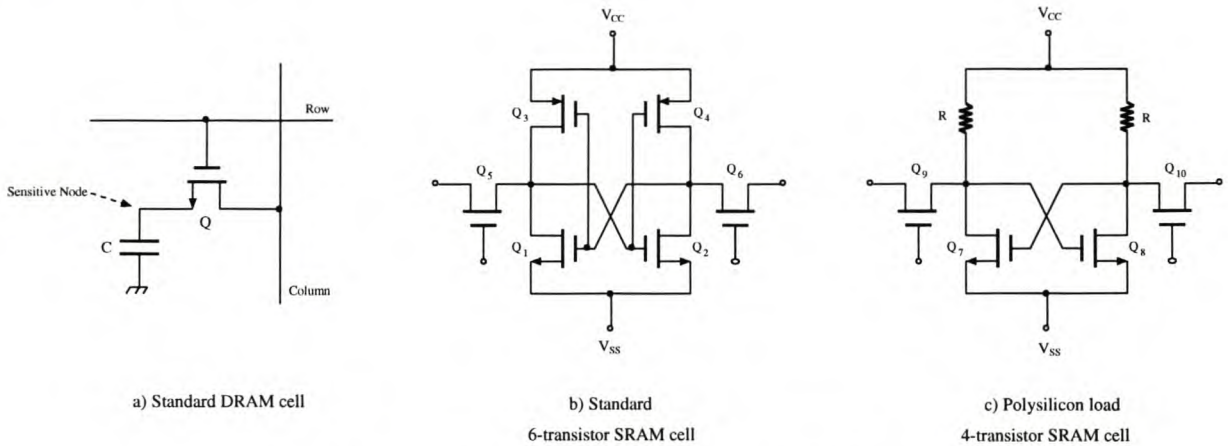


Figure 3.9: Dynamic and Static Memory Cell Configuration.

3.9.2 6-cell SRAM devices

The Static RAM device utilizes storage cells consisting of a flip-flop formed by cross-coupling two inverters (see Fig. [3.9](b)). Two access transistors allow the data to selectively accessed. The current state of the SRAM will remain constant unless an external signal causes the state to change.

SRAM devices are susceptible to SEU caused by the power rail collapse phenomenon as described in Section 3.6.2. The more common upset is caused by the passage of an ionizing particle through one of the inactive transistors in the SRAM cell. The induced charged caused by the passing particle can cause shifts in the threshold voltage and these shifts may be sufficient to activate the transistor (cell state change).

3.9.3 4-cell SRAM devices

The polysilicon load SRAM is similar to the 6-cell SRAM discussed in the previous section. Fig. [3.9](c) depicts the structure of this type of SRAM. Two of the transistors are replaced by load resistors formed in the polysilicon layer via an additional processing step. Large-valued resistors can be obtained in this way, with result that the power dissipation per cell is low. The 4-cell SRAM device has similar radiation tolerance characteristics to the 6-cell SRAM.

This type of SRAM cell is also susceptible to a special form of SEE, called *single event disturb errors* (SEDE) [14]. This upset is caused by the passage of a single particle through the cell during the sensitive period after each write operation. This period is particularly sensitive to disturbances due to the slow recovery from procedure that discharges storage

nodes in order to reset the cell to the '0' state. The 4-cell SRAM device is thus sensitive to single particles that would not have effected a 6-cell device. In order to lower the susceptibility of these devices, the access times must be degraded considerably. Another problem is that the unstable error state persists for a longer period of time. The last troublesome effect is that if steps are taken to reduce SEU in these cells, these same steps tend to increase SEDE. One way in which to decrease SEU susceptibility is to decrease the load resistance, which in turn causes an increase in standby current.

3.9.4 EPROM devices

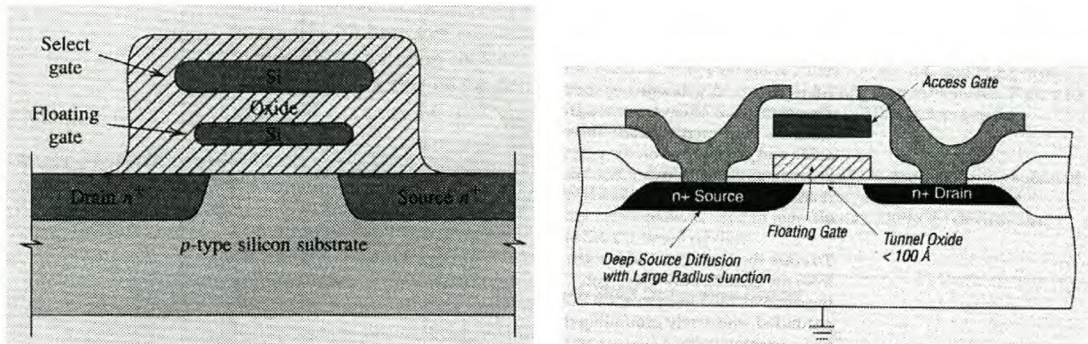
EPROM devices use variants of the memory cell whose cross section is shown in Fig. [3.10] (a). The memory cell consists of an enhancement-type n -channel MOSFET with two gates made of polysilicon material. One of the gates is not connected to any other part of the circuit. It is left floating and is therefore called a *floating gate*. The other gate, called a *select gate*, functions in the same manner as the gate of a regular enhancement MOSFET.

In the unprogrammed state, the floating gate contains no charge. If a large voltage (typically $+15\text{ V}$) is applied the drain, with the source at 0 V , electrons are accelerated across the channel. As these electrons reach the drain they acquire sufficiently large kinetic energy and are called *hot electrons* (or *hot carriers*). If a large voltage (typically $+25\text{ V}$) is now applied to the select gate, a large electric field is established in the insulating oxide. This electric field attracts the hot electrons and accelerates them towards the floating gate. These electrons charge the floating gate and the charge that accumulates on it becomes trapped.

The charge that accumulates on the floating gate reduces the strength of the electric field in the oxide and the accumulation of charge slowly reduces until no further charge is accumulated on the floating gate. The programming voltages are now removed. The trapped charge on the floating gate now induces an inversion layer in the channel. This implies that there is now a change in the threshold voltage of the device. In this way information is stored in an EPROM cell.

To return the EPROM cell to its unprogrammed state, the charged stored on the floating gate must be removed. This *erasure* process can be accomplished by illuminating the cell with ultraviolet light of the correct wavelength. The ultraviolet light photons impart sufficient energy to the trapped electrons, allowing them to overcome the inherent energy barrier and thus to be transported through the oxide, back to the substrate.

Incident ionization tends to oppose the above charge states by reducing or increasing electrons corresponding to the high and low states respectively. This results in an intermediate charge state, destroying the information stored. Floating gate devices are primarily affected by total dose effects, dose rate and SEU playing only a minor role ([53], p781). The relative immunity of floating gate devices to SEU stems from the relatively low levels of additional charges caused by an incident ionizing particle. Even the highest energy (LET) cosmic rays will not cause a significant change in the state of the floating gate transistor cell. Floating gate memories however have a long-term memory retention problem as charge tends to



(a) EPROM cell ([74], Fig. 13.46a).

(b) FLASH cell ([2], Fig. 7).

Figure 3.10: Cross sections of Floating Gate Memory Devices

leak off the floating gate. It is therefore advisable that a refresh procedure be implemented (similar to that of DRAM, the refresh frequency being lower).

3.9.5 EEPROM devices

The EEPROM, being a floating gate device has similar radiation characteristics to that of EPROM. Floating gate devices are most sensitive to radiation effects during programming as a high voltage is applied across the insulator (which produces a high field strength in the insulator). If a burst of ionizing radiation were to pass through the insulator whilst the high field strength exists, large current pulses can flow across the insulator. These can cause destruction of the insulation layer. The macro effect would then be a large, permanent increase in the supply current of the device. Designs using floating gate devices should therefore limit programming these devices to periods where the probability of incident radiation pulses is low (*i.e.* programming a floating gate device when a LEO satellite passes through the SAA would be consider a high risk activity).

3.9.6 Flash devices

Flash devices [72] have, apart from the width of the oxide layer, a similar physical structure to that of EEPROM (Section 3.9.5 and Section 3.9.4). In Flash the width of the oxide layer is relatively thin, $\sim 100 \text{ \AA}$, compared to EEPROM with an oxide thickness of $> 150 \text{ \AA}$. The difference in oxide thickness results in a device that is less susceptible to total dose effects as less trapped charge can be accumulated in the oxide.

Modern flash devices implement an internal controller to make device operation transparent to the user, and to improve write and erase times. This controller unfortunately significantly increases the susceptibility of the device to SEU and SEL. It has been found [72, 73] that during SEU in modern flash devices, the internal controller state is corrupted.

In most cases, the effects can only be removed by power cycling the device. It was also found that part of the flash contents could be written due to the controller state corruption. Abrupt steps in power supply current have also been observed. Corruption of the internal controller has also been found to subsequently cause total device destruction.

Furthermore, single supply devices implement an internal charge pump to generate the required 12 to 20 V required to write or erase cells. As for the controller, the charge pump is also susceptible to SEU. The charge pump is also susceptible to TID [36] and changes in the charge pump can cause the write time to increase from less than 1 second to more than 600 seconds at 20 krad(Si) and supply currents from a few mA to over 1 A. Error recovery of Flash devices is therefore complex, requiring reprogramming and power cycling capabilities. The high rate of scaling that Flash devices are undergoing is an additional cause for concern.

3.9.7 Fuseable-link PROM devices

A *Programmable Read-Only Memory* (PROM) [31] device consists of a number of row lines and column lines. Where the row and column lines cross a tiny fusible link is connected between the two lines. With the correct addressing of the row and column lines, this matrix appears similar to DRAM. In the case of the PROM the information is stored in the status of the fusible link. This link can be vaporized by selecting it using the PROM's address and data lines, and then applying a high voltage pulse to the device through a special input pin.

These devices are often used in satellite On-Board Computers to store the initial startup code. On *SUNSAT*, the HM-6617 fuse link PROMs are used for this purpose. If the correct programming procedure is followed, the information stored in a PROM can remain valid for the lifetime of the device. By their nature these devices are not susceptible to SEU, making them ideally suited for use in radiation environments. They are however, being CMOS devices, susceptible to total dose effects.

3.10 Field Programmable Gate Arrays (FPGA)

These devices have become popular in terrestrial applications due to their low cost, flexibility and high densities. Their use in space applications is also being considered. A Field Programmable Gate Array can be described as an array of functional blocks along with an interconnection network. Both the specific function of each block and the interconnection of the blocks can be configured. The configuration of a FPGA is stored in a *configuration cell*. A number of manufacturers are producing FPGA devices and each implement a different functional block and interconnection network architecture.

A number of Input/Output Blocks are also provided that enable the interface of external signals with the interconnection network inside the FPGA. The functional block (often called a *Configurable Logic Block*, CLB) normally consists of a combinatorial function and

one or more flip-flops. The number and nature of the CLBs and the architecture of the interconnection network determines the characteristics of the FPGA.

3.10.1 CLB Primitives

The CLB's found in FPGAs are made up of one or more of the following primitive components:

RAM lookup tables: In this component the input variables are used to select values from a RAM memory that has been preloaded with values representing the truth table of the function to be implemented. Thus all possible functions of the input variables can be implemented. This structure offers area efficiency and predictable delays which scale well as the number of inputs are increased.

Multiplexers: This style of function unit is based on observation that all functions of n input variables can be implemented by a single $n : 1$ multiplexer. The main advantage this type of structure is that it can be implemented in high densities.

Fixed functions: This primitive provides one specific function. The single fixed function has the advantage of simplicity and low delay per stage. The principle disadvantage is that larger numbers of these primitives are required in order to implement user designs.

Flip-flops: These are used to synchronize signals and are also used to form registers.

3.10.2 Interconnection Network

The interconnection network of FPGA generally consists of short and long (local and global) interconnect lines, as well as switches. Long lines generally cross the entire array structure, although variations in which only half the array is crossed are also useful. The connections between the CLBs and the interconnection network are achieved means of switches, which allow signals to pass in both directions. The interconnection network does not pose a problem in radiation environments.

3.10.3 Configuration Elements

The configuration of the FPGA is stored in memory cells that resemble those of standard CMOS Memory devices. The most commonly found configuration cell technologies are SRAM, EPROM, EEPROM/Flash and Anti-Fuse.

3.10.3.1 SRAM

Some FPGAs implement configuration elements based on the 6-cell SRAM memory cells. The state of the configuration elements needs to be *downloaded* into the FPGA before the device can be used and this download process must occur after each power-down. The most common approach is to store the configuration in a serial EPROM. The FPGA can then automatically clock the serial configuration data into the configuration cells. The configuration data can also be downloaded from a microcontroller or microprocessor. The primary advantage of this configuration element is the reconfigurability it affords (and hence design flexibility).

This feature is however a disadvantage with respect to space applications where the risk of SEU is significant (similar to that of SRAM). Note that as the density of configuration cells is considerably lower than that of a typical SRAM, the SEU cross section is correspondingly smaller. On the other hand, the effect of configuration corruption can be disastrous and can lead to severe damage or total destruction of the system (the amount of damage is determined by the application). SRAM based FPGAs are therefore generally not considered suitable for use in radiation environments except when their use is limited to small periods of time (and they remain unpowered for the majority of the orbit).

3.10.3.2 EPROM/EEPROM/Flash

Devices based on these technologies use configuration cells that are nearly identical to that of EPROM, EEPROM and Flash memory devices. These configuration cells are also affected by radiation in a fashion similar to that of the memory devices. See Sections 3.9.4, 3.9.5 and 3.9.6 for details.

Research on the use of FPGAs with these types of configuration cells in space applications was inconclusive. No references could be found that would indicate that these devices have ever been used in a space radiation environment, or that they have undergone any form of radiation qualification tests. Their use is therefore unwise and should currently not be considered.

3.10.3.3 Anti-Fuse Configuration Elements

The Actel FPGAs' silicon real estate is about half devoted to logic modules and half to an interconnection matrix (ignoring peripheral circuitry for programming and control functions). The matrix consists of horizontal and vertical conductors with an *anti-fuse* (see Fig. [3.11]) at the intersections. The anti-fuse dielectric is a thin sandwich of oxide-nitride-oxide (ONO) measuring ≈ 80 to 90 \AA oxide-equivalent thickness. At maximum, a FPGA design will have a few percent of these connected via electrically induced dielectric breakdown (or rupture), followed by pulses to achieve the desired resistance. An unprogrammed anti-fuse will be biased when the logic levels on the two crossing conductors differ, which obviously depends on the duty cycle and the phase of the two signals. There are many unprogrammed anti-fuses ($\approx 650,000$ for a AH1280 device).

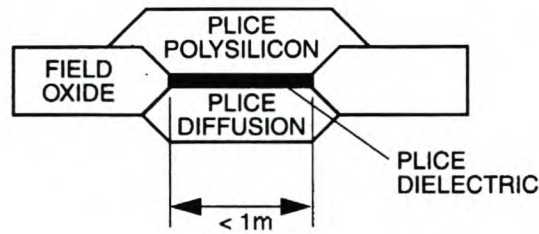


Figure 3.11: Cross section of a PLICE anti-fuse as used in Altera devices

FPGAs are now also being produced that make use of Metal-to-Metal (M2M) anti-fuses. The M2M anti-fuses have a lower programmed resistance than the ONO anti-fuses ($\sim 20 - 50\Omega$ versus $\sim 100 - 500\Omega$). Devices using these anti-fuses appear to be more radiation tolerant (inconclusive).

The primary effect that radiation has on anti-fuse type devices is known as *Single Event Dielectric Rupture* [80]. The electric field strength over the insulating ONO of biased anti-fuse is sufficiently large so that radiation induced dielectric rupture can occur. An undesired partial connection is formed, the symptoms of which are: a) a small current increase only, b) an intermittent fault due to reduced timing and voltage margins, or c) a hard fault. Experimental work [80] indicates that the risk of SEDR is relatively small (on the order of 3×10^{-5} per device-year. Overall, the A1280A appears to be the most suitable non-radiation hardened FPGA for use in the LEO environment [39, 40].

3.10.4 I/O Block

The I/O blocks of FPGAs typically support one or more of the following requirements:

- Support both TTL and CMOS voltage levels at inputs.
- Support bi-directional, input, output, open-collector and three-state output modes.
- Provide high drive current on output interface.
- Limit output drive to reduce power consumption, prevent overshoot, and reduce supply noise.
- Provide slew rate adjustable outputs.

None of these elements contribute significantly to the radiation performance of the device.

3.11 Microprocessors

Microprocessors form the core of typical On-Board Computers. These devices contain various elements such as combinational logic, registers, *etc.* These elements have similar radiation characteristics to that of the discrete equivalents. Modern microprocessors also make use of an instruction and/or data cache to ensure that the instructions and data are always available for processing. The presence of cache on the processor however, immediately lowers the useability of the processor for space applications [55].

3.12 Techniques for System Radiation Hardening

Radiation hardness describes the ability of an integrated circuit to retain function and performance after being exposed to a specified amount of radiation. A circuit that does retain specified function and performance is often called rad-hard. The techniques used to minimize this degradation can be divided into: component level techniques and system level techniques.

3.12.1 Component Level Techniques

Unhardened commercial electronics can frequently survive 3 – 10 *krad* (*Si*) TID without significant parametric degradation [8]. They can also remain functional (although degraded) from 10 – 30 *krad* (*Si*) but will be increasingly more sensitive to SEE and SEL.

Radiation hardening almost always implies a different fabrication process to that of non-radiation hardened components [49]. A dedicated fabrication line is therefore required and this greatly increases the cost of radiation hardened components. The cost of radiation hardened components can typically exceed that of commercial components by a factor 10 to 100. The most common techniques are:

Thinning of gate oxide layers

By decreasing the width of the oxide layer, the volume where charges can be trapped is decreased. This in turn implies a lower threshold voltage shift after radiation and therefore improve the device total dose characteristics.

Electron Traps

To offset the effect of trapped holes in the insulating layers, electron-trapping materials (the details are proprietary) can be distributed through the insulating layers. When the ionizing radiation then produces the electron-hole pairs and the holes become trapped in the insulating layer, the electrons become trapped in the added electron traps, keeping the the threshold voltages nearly unchanged.

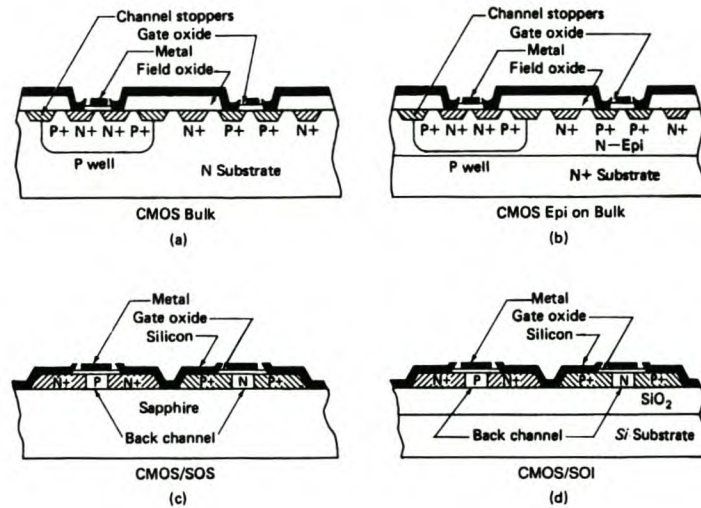


Figure 3.12: Comparison of CMOS Bulk, CMOS Epi-on-Bulk, CMOS/SOS and silicon on insulator (SOI) structures curves ([53], Fig. 6.31).

SOS and SOI technologies

In SOS (Silicon-on-Sapphire, Fig. [3.12]) technologies, each transistor is made on an individual silicon island. These islands are isolated from each other by removing the epitaxial silicon from non-active areas, leaving only an insulating sapphire substrate. This removes the possibility of any parasitic structures existing between the transistors, and thus completely prevents latchup (giving the devices an infinite SEL tolerance).

SOS is a subset of Silicon-on-Insulator (SOI) technologies, the latter being the generic class. These technologies are also less susceptible to the effects of photo-current. This flows from the fact that the junction area is confined to only the thin epitaxial layer rather than the much larger junction and well depletion volumes which occur in conventional CMOS processes. SOS technologies also have better SEU performance than conventional CMOS. As the junction areas are considerably smaller, the effective SEU cross-section is considerably smaller. CMOS SOS retains the high neutron radiation tolerance as it is a majority carrier technology.

Enlarged Power Rails

As was mentioned in Section 3.6.2, power rail collapse is a possible cause of information corruption. In order to reduce or eliminate the probability of power rail collapse, the power and ground rails can be enlarged.

Cross section adjustment

The transistor sizes of memory and register cells can be adjusted in order to alter the SEU cross section in order to improve SEU characteristics.

3.12.2 System Level Techniques

The application of component level techniques are largely limited to project with large budgets. System level techniques can be relatively inexpensive and can therefore be used by small-scale microsatellite designers to improve the radiation hardness of a satellite. The most commonly used techniques are:

EDAC to counteract SEU

The use of Error Detection and Correction circuits can be used to correct data errors caused by SEU. It should be noted that in LEO orbits, most SEU occur during the passage through the SAA (*i.e.* in ≈ 10 minutes once every orbit). Depending on the sensitivity of the memory being protected, the EDAC system must be designed to cope with high wash rates during the SAA transit in order to prevent SEU accumulating (resulting in MBEs occurring).

Reset and Watchdog

A system reset refers to the process of resetting or restarting an electronic system after a temporary malfunction. A recovery mechanism is typically incorporated into the system software. This recovery software must take corrective actions to compensate for the side effects of the system malfunction (*e.g.*, lost time, lost sensor data, rollback of incomplete actions, restoration of state, *etc.*). The recovery software must therefore restore the system into such a state that the nominal flight software can be restarted.

In order to recover from anomalous conditions, a “watchdog” device is often added to microprocessor and microcontroller systems. The watchdog device consist of a timer, which counts down from a predefined initial count value. Once the count value reach zero, the watchdog triggers a system reset, which reinitializes the system. The software executing on the microprocessor / microcontroller must continually reset the watchdog counter to prevent the system reset being triggered. This ensures that “soft” errors in the microprocessor / microcontroller will be recovered from within a short period of time.

Triple Modular Redundancy

Triple Modular Redundancy entails the use of three distinct modules for each logical operation. The logic result of each of the three modules is compared and the majority result is asserted. TMR helps to mitigate SEUs and is now extensively used in space applications.

Shielding

Radiation shielding is an integral part of any spacecraft design due to the inherent shielding provided by the spacecraft structure. The packaging of components can also contribute to shielding and additional shielding can supplement the existing shielding.

Low-energy particles are trivial to shield against, whereas high-energy particles become much more difficult to shield against. Shielding consisting of materials with low atomic number, such as carbon and aluminium, exhibit desirable radiation attenuation characteristics. Electrons can be effectively attenuated by aluminium shielding even at high energies.

While aluminium shielding is effective for low-energy protons, it is ineffective against high-energy protons ($> 30 \text{ MeV}$). Designers often sculpt shields to work in conjunction with the spacecraft's inherent shielding, thereby minimizing mass. Shields that consist of layers of carefully chosen low Z and high Z materials are being developed and tested for use in space qualified components [20, 56, 76] and for additional external shielding. A number of aerospace orientated manufacturers are designing IC packages with shielding [77].

The combined effect of shielding is to lower the TID of the shielded components. Shielding does however not significantly lower the SEU rates of devices [32, 44]. This is due to the fact that particles energetic enough to cause SEEs typically require shields several centimeters thick to be adequately attenuated. Unfortunately, shielding may also enhance TID and SEEs by slowing fast particles into energy ranges of SEE or TID sensitivity.

Component Screening

Another technique often used to ensure the sufficient reliability of electronic components is screening. Components that are to be used usually entails the extensive testing of selected components from a specific lot. If the results indicate that the particular lot has sufficient radiation tolerance (as defined by the screening criteria), that lot is certified for used.

Unfortunately, screening results are only valid for a particular lot. When a new lot is to be used, the lot *must* be re-certified. This can be a very lengthy and expensive procedure. Testing under realistic radiation conditions of representative samples is therefore seldomly possible.

3.13 Comments

There is no total solution to the problem of system radiation hardening. The management of the results from radiation induced system degradation must therefore be an integral part of the overall system design. There remains a great deal of uncertainty with regards to the effects of radiation on systems (*i.e.* the ability to accurately control the effects of radiation on a particular system implementation).

There has been an awareness of this uncertainty for close to two decades [61]. Although the

understanding of radiation and its effects have greatly increased, this uncertainty remains. The continued scaling of semiconductors has now begun to significantly worsen the situation. This uncertainty impacts all players in the space game and has forced the creation of workgroups to attempt to counteract this trend. These workgroups have however had limited success. Thus, from a radiation perspective, the space environment thus remains a high risk environment.



Chapter 4

The Sunsat OBCs

The OBCs of SUNSAT are considered to be part of the Flight Management System (FMS). The original FMS specification (see Section B.1) was based on the original mission specification of SUNSAT. With time, the mission specification was altered to cater for changes in launch vehicles, payloads and desired functionality. The overall functional targets of the FMS have however remained unchanged. These targets have been successfully achieved.

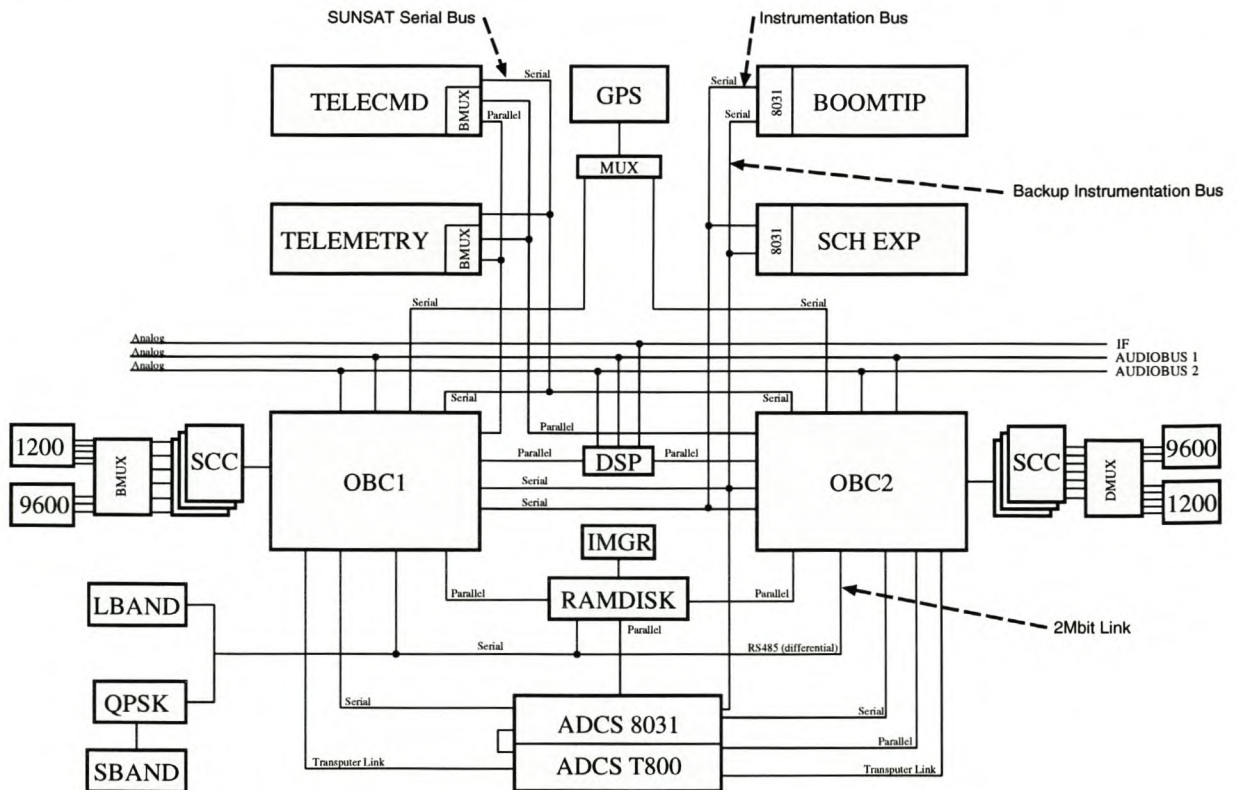


Figure 4.1: Diagrammatical representation of the SUNSAT Core Architecture

Fig. [4.1] shows the current SUNSAT core architecture (which will be discussed in subse-

quent sections). The FMS is composed of two flight computers, OBC1 and OBC2, together with the Mass Storage Module (RAMDISK). The final specification of the FMS from which this architecture was derived can be found in Section B.2.

4.1 First On-Board Computer

OBC1 [17] is the primary on-board computer and is responsible for the operational control of the satellite. The primary computer must therefore active for the majority of the time and low power consumption is critically important.

The general devices used (logic gates, buffers, *etc.*) were chosen from the AC and ACT device families. The exception was the inter subsystem interfaces where HC components was used (due to EMI considerations). Fig. [4.2] and Fig. [4.3] give a block diagrammatical representation of the address and data bus hierarchy of OBC1.

4.1.1 Processor

OBC1 is designed around an Intel 80C188 16-bit processor (operating at 13 *MHz*). The 80C188 is an embedded version of the 8088 processor. The 80C188 processor was selected due to its high level of integration and low power requirements. Some of features of the 80C188 are:

- ➔ 8-bit external bus (16-bit internal),
- ➔ Power down and Idle modes,
- ➔ 8259 compatible interrupt controller,
- ➔ Timer/Counter unit,
- ➔ Chip-select unit,
- ➔ 4 channel DMA unit,
- ➔ Serial communication unit (UART),
- ➔ Refresh control unit,
- ➔ Watchdog unit.

At the time **SUNSAT** was designed, radiation effects data on the 80C188 did not exist. There were however experiments performed on the 80186 [51] and these tests indicated that under worst case conditions (large solar flares) one upset could be expect every 5 hours. This estimate was based on an orbit of 1330 *km* with 200 *mils* aluminium shielding. The radiation tolerance of the 80C188 was estimated to be sufficient for **SUNSAT**. During

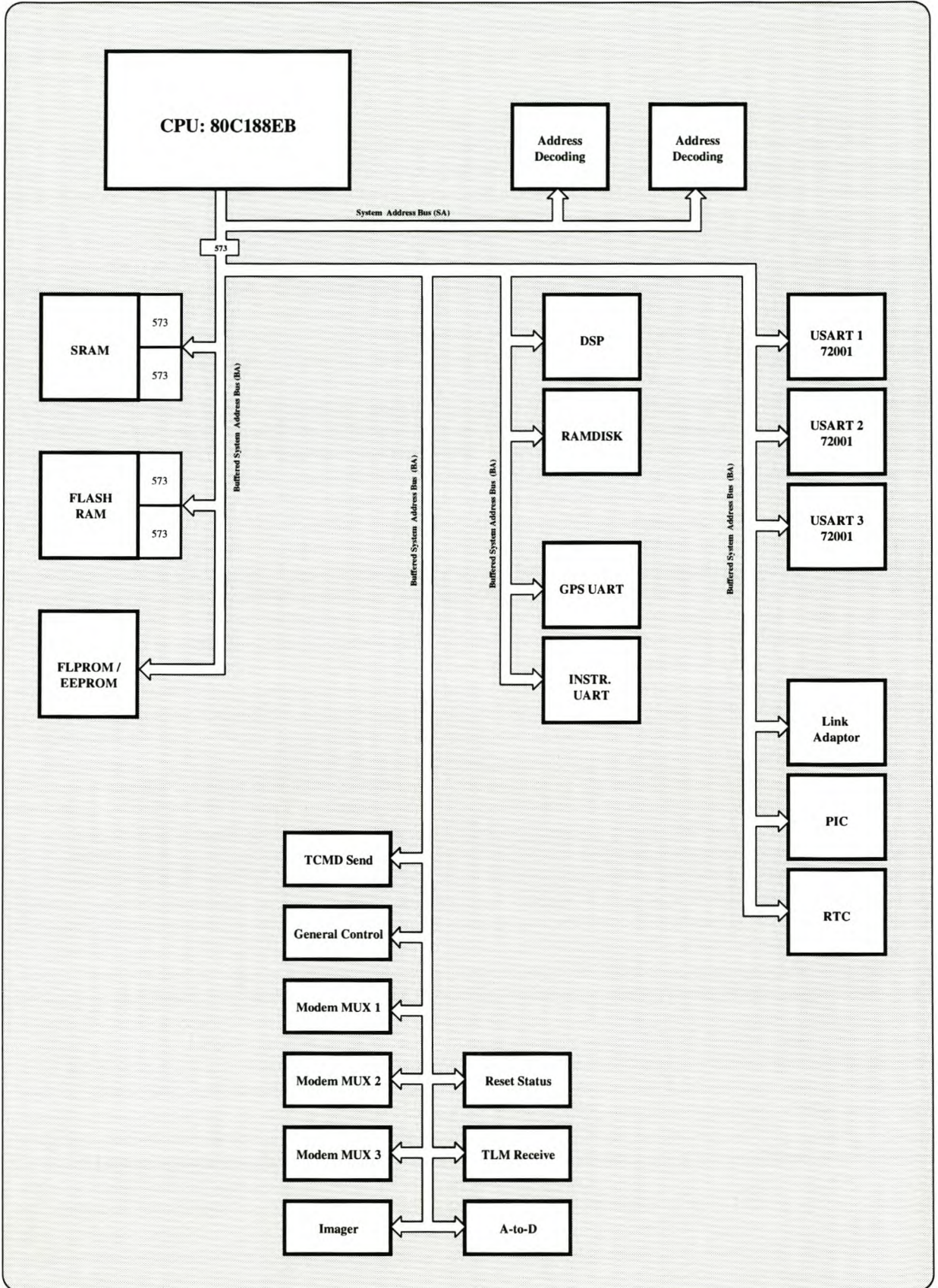


Figure 4.2: OBC1 Address Bus architecture

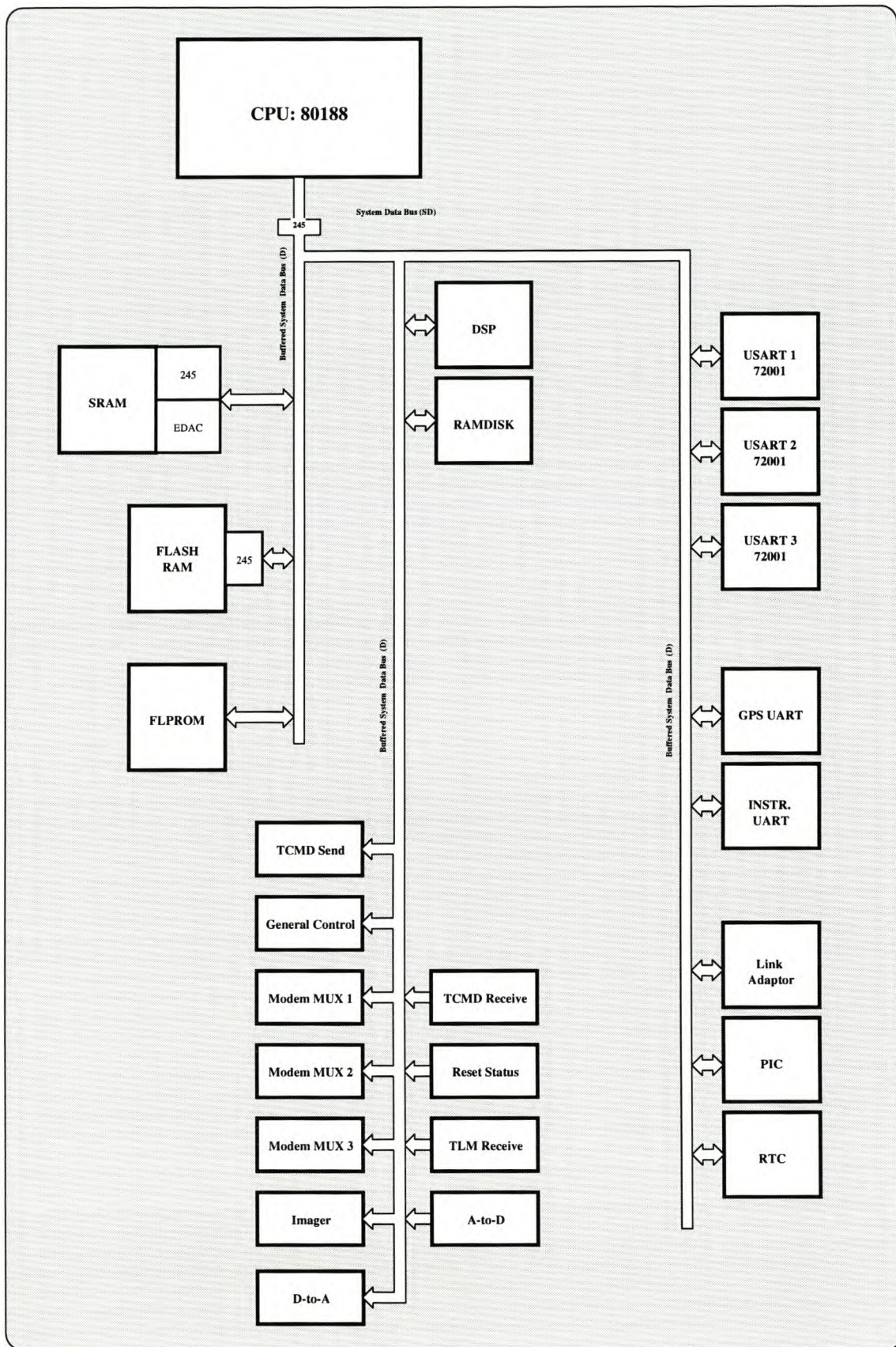


Figure 4.3: OBC1 Data Bus architecture

the almost two years of in-orbit operation, OBC1 has not experienced any anomalies that could be traced directly to upsets in the CPU. After particularly intense solar flares during June and November 2000, the OBC did however not respond as expected and generally became unstable. A subsequent power cycle restored the OBC to a fully functional state. It is conceivable that an upset, SEFI, in the CPU could be the cause of this instability. Due to the fact that increased power consumption accompanied these times of instability, it is also possible that one of the SRAM devices experienced SEFI.

4.1.2 Fuse-Link PROM

After a reset, the processor begins execution at address FFFF:FFF0 (hex). A stable source of initial code must be mapped into this region during reset. Due to the critical nature of this code (the loss of this code results in an unusable OBC), the code is stored in a Fuse-Link PROM. The rugged nature of these devices are sufficient to ensure a high probability of the reset code being available. Since launch, OBC1 has been rebooted (which makes use of the PROMs) numerous times and no anomalies were encountered.

4.1.3 Flash RAM

The satellite software is stored in 256 *KB* Flash-RAM. Initially, the 28F020 component made by Intel was used. This component proved to be very sensitive to variations in programming sequence and timing (and a number of devices were destroyed during the original prototype debugging). An equivalent replacement device from AMD was subsequently used and no further problems were encountered. Note that the Flash devices used are 12 *V* programmable devices. The programming voltage was designed to be switchable. During normal operation, the programming voltage is removed and this decreases the possibility of radiation induced failures (Section 3.9.6). Since launch, the Flash devices have been reprogrammed eight times. No in-orbit anomalies directly related to the Flash memory have been encountered.

The ADCS subsystem also makes use of Flash RAM to store the ADCS flight software. In that subsystem, sufficient Flash was added to allow multiple versions of the ADCS software to be stored. This proved to be very useful whilst testing (in-orbit) new versions of the software. For a next generation OBC, it would also be desirable to have sufficient Flash to store two versions of the Flight Software (*i.e.* 2×256 *KB*).

4.1.4 SRAM

OBC1 has 1 *MB* of EDAC protected Hitachi HM628512 SRAM. The SRAM has been organized (for redundancy) into two banks of 512 *KB* each. In the original design, each bank was individually powered and could be disabled/isolated from the system bus. The motivation for this was uncertainty with regards to the power consumption of the SRAM after being subjected to radiation. Based on SRAM radiation performance trends noted

(on other satellites) during the production of the FM, the power consumption increases were considered to be of the same order as the rest of the OBC components. The power switches were therefore removed.

4.1.5 Error Detection And Correction (EDAC)

To protect against SEU in the SRAM, an EDAC system was added to OBC1. The EDAC is implemented in discrete logic and each data byte is protected by a 4-bit correction code. The code is based on a Hamming (8,12) code, with distance 3, which can detect and correct single bit errors. The EDAC system implement corrects errors in the data read from the SRAM components, but does not automatically write the corrected data back to the SRAM. A critical problem encountered with the EDAC design was the lack of testability. The only way in which the EDAC could be tested (in the final design) was to short the data bus pins.

When the FM OBC1 was assembled and tested, the EDAC was not tested sufficiently. As the components of the FM was soldered directly into the PCB for mechanical stability, shorting the data bus pins was considered high risk. Once the satellite was in orbit, attempts were made to activate the EDAC. Unfortunately, the EDAC proved to be non-functional. Due the insufficient integration testing, it is not known if the EDAC was functional before launch, or if it failed during launch.

The OBC1 was therefore left without EDAC. A number of modifications were made to the Flight Software to increase its robustness against SEU. Amongst other, the Flight Software was modified so that SEU induced corruption would trigger a reset within a relatively short time (to limit error propagation). Furthermore, the Flight Software was modified so that an OBC reboot was now an acceptable operation (the Flight Software would automatically recover from the reset and reconfigure itself into a stable, semi-normal operational state).

The in-orbit performance has proved to be surprisingly good given the EDAC failure (OBC1 uptimes, without watchdog reset or crash, were as high as 80 days). It is therefore conceivable that a new OBC could be designed without an EDAC. If an EDAC is to be included in future OBCs, design for testability is of utmost importance. This can be as simple as jumpers inserted into the data bus. A more complex, built-in self test (BIST) may also be consider after the increase in complexity has been assessed.

4.1.6 Watchdog

The integrated watchdog of the 80188 proved to be of greater importance due to EDAC failure. Under normal circumstances, a watchdog is added to protect against the inevitable latent bugs in software. Due to EDAC failure, program variables would be corrupted and this would causes unpredictable software behaviour. Thus, even though the software were to be relatively bug-free, the corruption of data variables would within a finite time cause the software to crash. The subsequent reset caused by the watchdog would then reinitialize the system into a cleared, fresh state.

4.1.7 Real-Time Clock (RTC)

The DP8572AM RTC made by National Semiconductor was used due to its low power consumption. The resolution of the RTC was adequate and the built-in calendar is important for the satellite dairy software. The configurable alarm interrupt can also be used to schedule events. The addition of a RTC is required as CPU timer based time keeping is insufficiently accurate. Due to unpredictable IRQ load, variability in timer IRQ servicing and CPU dependent clock distribution variations, drifts on the order of seconds per hour are not uncommon. During the almost two years in orbit, no anomalies or upsets related to the RTC were encountered.

4.1.8 Programmable Interrupt Controller (PIC)

The standard 82C59A CMOS PIC made by Intel augmented the 188's internal interrupt controllers. This component was also characterized by low power consumption and its interface compatibility with the microprocessor.

In the original OBC1 design, the INTA# signal was used to support the standard interrupt acknowledge cycles of the PIC. In subsequent revisions, this signal was removed. In retrospect, this change was most unfortunate and caused a significant increase in the complexity of the interrupt service routines (ISRs). If the INTA# were available, the USART interrupt identification could be done in hardware (the USART has support for interrupt acknowledge cycles) instead of the status poll loops needed in the current flight software ISRs.

4.1.9 Serial Communication Controllers (USART)

The NEC μ PD72001 SCC Universal Synchronous/Asynchronous Receiver/Transmitters (USART) provide the interface to the communication system of the satellite. These units are configured into 6 channels, through which most of the OBC1 external communication traffic passes. The advanced nature of the μ PD72001 (supporting a wide range of protocols, in particular HDLC) and the low power requirement were the primary motivation for their use. These devices will be discussed further in Section 4.3.

4.1.10 Transputer Link Adapter

In order for the flight management software to initiate predetermined attitude changes, OBC1 requires a communication interface with the ADCS. This is provided by the IMS C012 Transputer link adapter.

In the original design, an OBC controlled switch was added to allow control over the link adapter power. This was done as a power saving measure as the link adapter power consumption is relatively high. An anomaly was found to occur sporadically in-orbit, during which no data could be transfer to the ADCS via the link adapter. The engineering

model (EM) did not exhibit this anomaly. Other, potentially related, anomalies were however found in the EM.

In the majority of cases, a hardware reset (via the link adapter **RESET** input) was not sufficient to restore the link adapter to a functional state. A power cycle of the link adapter was fortunately sufficient. The Flight Software was therefore modified to perform a link adapter power cycle when a loss of communication with the ADCS T800 was detected.

The cause of this anomaly is still not clear. It is suspected that the problem could lie with the clock input of the link adapter. The clock input is fed from the ADCS T800 via differential drivers. The link adapter is however able to do its own synchronization if a local clock is directly connected to the clock inputs. This configuration reflects the designs of a number of the T800 debugging systems also developed (and these do not exhibit link adapter anomalies).

In future versions of the current OBC design, it is therefore recommended that the clocking circuitry be changed. Furthermore, it is recommended that an alternate backup path to the ADCS T800 be investigated. The loss of the link adapter has significant implications for the control of the satellite and can be considered to be a single point of failure. A relatively simple alternate path can be created if the T800 were to be connected to the OBC ↔ ADCS ICP bus. This bus would need to be modified to support multi-node operation.

4.2 Second On-Board Computer

OBC2 [25] is the secondary on-board computer and is the backup computer for both the primary on-board computer (OBC1) and the ADCS Transputer. OBC2 has not been used significantly since launch and there are two reasons for this. Firstly, the Flight Software has not yet been fully ported to OBC2. The severe lack of time and programmer resources was the primary cause for this. The effort required to complete the low level drivers for OBC1 was considerable, due to the large number of unique interfaces. Secondly, the engineering model of OBC2 proved to be unstable. A new version of the engineering model has since been constructed and appears to be stable.

The technical specification of OBC2 required a system that could interface directly with most of the satellite systems. The subsystem interconnections of OBC2 are therefore similar to that of OBC1 (with the ADCS being an exception). The majority of peripheral components of OBC are identical or similar to those used on OBC1. The motivation of their use is also similar (see Section 4.1). These components are:

- ➔ Real-Time Clock - DP8572AM
- ➔ Programmable Interrupt Controller - 82C59A
- ➔ Serial Communication Controllers - μ PD72001
- ➔ Transputer Link Adapter

4.2.1 Central Processing Unit

OBC2 is based on the 80386EX embedded processor (operating at 20 *MHz*). The 386EX processor was found to provide optimal performance whilst still requiring minimal support components. Unfortunately, the 386EX proved to generally more problematic than the 188 used in OBC1.

The 386EX processor does not have any on-chip cache (not referring to the instruction prefetch cache). This lowers the radiation susceptibility (at the cost of lower performance). Tests [55] have shown the 386 class of processors to be immune to SEL (or have a SEL threshold $> 24 \text{ MeV/mg/cm}^2$). The SEU threshold is $LET_{TH} \sim 4.0 \text{ MeV/cm}^2$. These devices have been used in a number of spacecraft and are considered acceptable in a radiation environment. This component is currently the highest integration non-radiation hardened CPU that has been used extensively in the space environment.

During the implementation of OBC2 it was noticed that the multi-function pins of the 386EX pass through (or remain) in a high impedance state (depending on the pin refer to) during and immediately after a device reset/powerup. Examination of the 386EX User Manual confirmed this observation ([34]; pp 5-21, 5-23, 13-3, 13-7, *etc.*).

As a number of these pins are used as chip select signals, the effected chips could be selected at inappropriate times. In the case of OBC2, this caused bus contention and pull-up resistors had to be added in order to ensure successful processor power-up. The boot software of OBC2 also had to be modified in order to configure all multiplexed pins into a sane state. On OBC2 the absence of the resistors also resulted in floating signals and this in turn caused above normal power consumption in some of the glue logic. In some of the logic gates oscillation was noticed as well.

The Errata Data Sheet ([35], p23) pointed out that some of the 386EX's output pins suffer from a floating output condition. Unused outputs were therefore also terminated correctly (by adding a pull-up or pull-down resistor depending on the default state of the particular output). Note that this error has been fixed in the C Stepping of the 386EX. It was however decided that the extra precaution of terminating unused outputs was warranted.

A timing problem was also encountered during the EM debugging and was also acknowledged as an error in the processor ([35], p30). This error causes the address hold time after the **WR#** signal goes high to be insufficient. Some peripheral thus release incorrect data during read accesses. This errata has fortunately been fixed in the C Stepping of the 386EX.

4.2.2 System Bus Architecture

Due to the large number of peripheral components, a fairly complex bus structure was used in order to limit the component output loading. The bus architecture implemented ensured that no component had a loading of more than 45 *pF* (*i.e.* an output drives at most 4 inputs). The grouping of components on the separate buses was dictated by their nature. There are three main buses: the System Bus, the Memory Bus and the I/O Bus.

Fig. [4.4] and Fig. [4.5] give a block diagrammatical representation of the address and data bus hierarchy of OBC2. If one compares the bus structures of OBC2 with those of OBC1, the primary difference is the large number of additional buffers required in OBC2. The stringent timing requirements imposed by the CPU were the primary reason for the complex bus.

4.2.3 Maths Co-processor

In order for OBC2 to serve as backup processor for the ADCS Transputer, The Intel 387SX co-processor was required as the 386 family of processor do not have adequate numerical performance (floating-point operations are not supported by the processor). The 387SX processor connects directly to the 386EX without the need of any additional components.

4.2.4 Volatile Memory

The Volatile Memory Block provides 3 *MB* SRAM data memory with 3 *MB* EDAC checkbit memory. The EDAC function is performed by the AMD2960A 16-Bit EDAC. The implementation allows the detection and correction of single bit errors and the detection of multiple bit errors. If a single bit error is detected, the corrected data is placed onto the memory bus and an interrupt is generated. Note that the corrected data is not written back to the memory device. The satellite software must therefore periodically read and write back all data stored in the SRAM components. Multiple bit errors have been configured to trigger a processor reset. The reset circuit has been design so that the source of the reset is latched.

4.2.5 Non-Volatile Memory

The Non-Volatile memory block is made up of Fusible Link PROM and Flash RAM devices. The PROM devices (2×2 *KB*) contain the satellite software boot loaders. The boot loaders are executed upon processor startup and must load the satellite software.

The satellite software is stored in 1 *MB* of Flash-RAM. In order to detect the presence of errors use is made of duplication (*i.e.* there is an extra 1 *MB* of Flash RAM). During any read action from the Flash RAM a comparison is made between the two banks of Flash. A difference indicates an error and triggers a Non Maskable Interrupt (NMI). The satellite software is thus informed of the error condition and can take the appropriate steps. This duplication of non-volatile memory was not done for OBC1. In the almost two years in orbit, no upsets were encountered in the Flash memory. It would therefore be feasibly to design without such duplication.

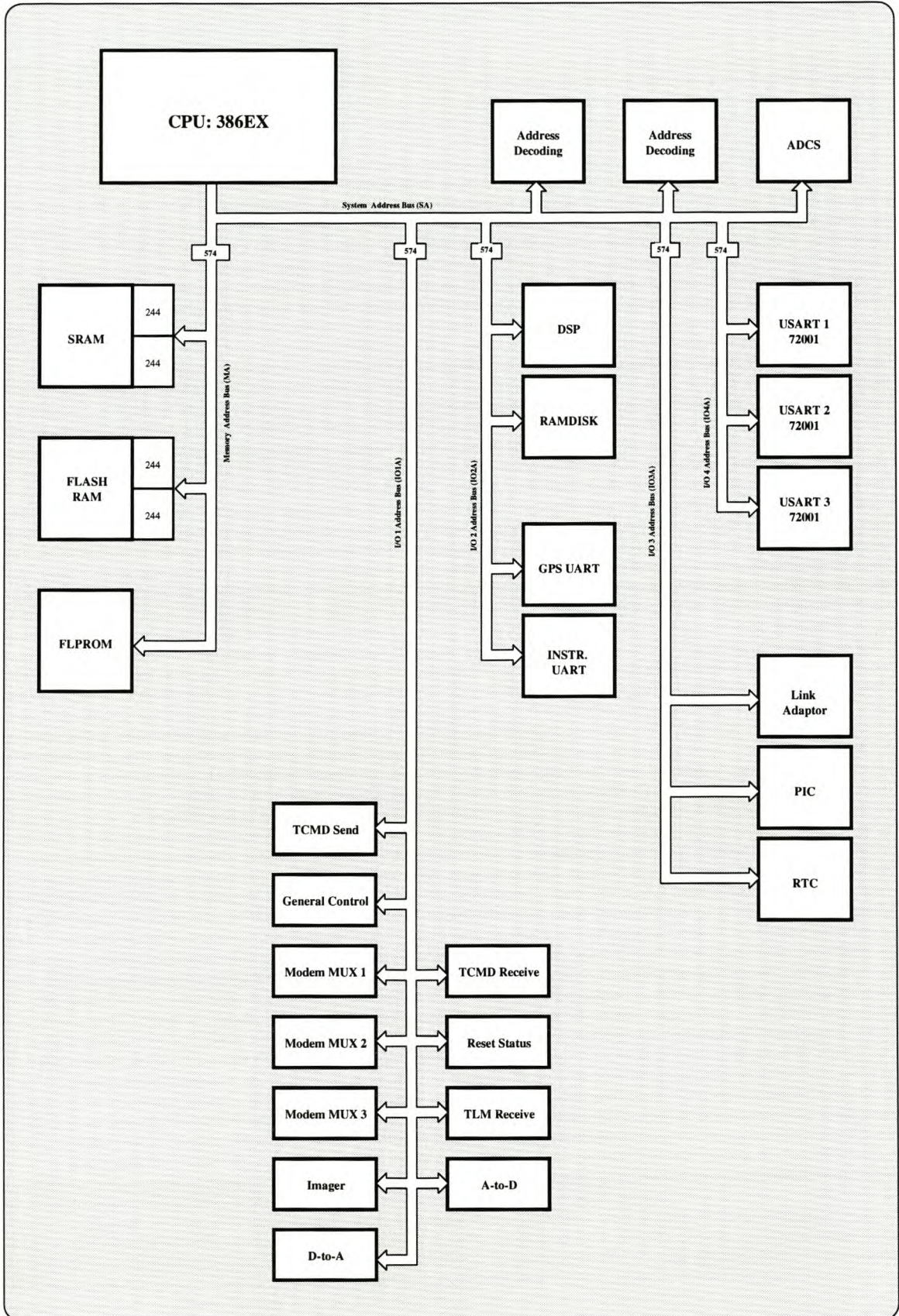


Figure 4.4: OBC2 Address Bus architecture ([25], Fig 4.2)

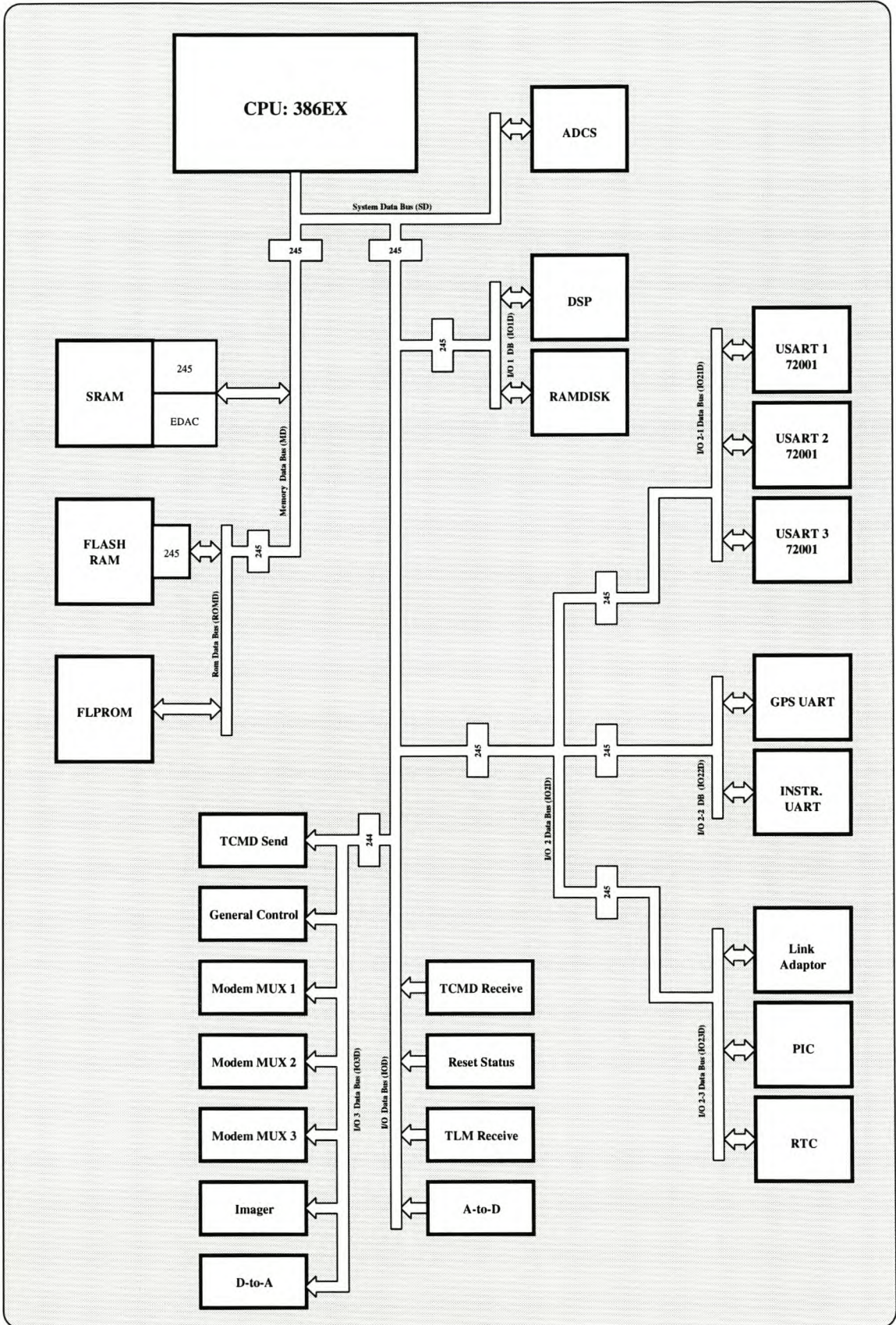


Figure 4.5: OBC2 Data Bus architecture ([25], Fig 4.3)

4.3 **Sunsat** Communication Interfaces

The communication systems (Fig. [4.1]) of **SUNSAT** can be divided into two primary groups: external and internal (with respect to the satellite). These two main groups can be further sub-divided into the following types: Parallel communication channels, Asynchronous serial channels and Synchronous serial channels. Interrupt based communication control has been used in both of the OBCs. Although interrupt systems (versus polling systems) have lower software overhead, the frequency of interrupts significantly affect the performance of microprocessor based systems. In particular, if the interrupt service routines are complex and the interrupt frequency is high, the time taken to service interrupts can consume all or nearly all processor cycles. This has been found to be a very real problem in **SUNSAT**. A number of interrupt services routines were rewritten in Assembler in order to reduce the interrupt processing time. The frequency of interrupts will therefore be noted in the following discussions.

4.3.1 Internal Parallel Bus Interfaces

A number of subsystems have been designed so that they can be independently activated and deactivated. Each interface to such subsystems required the design of isolation mechanisms so that no inactive logic is driven when subsystems are deactivate. This generally implied the use of a “power good” signal from the receiving subsystem, and vice versa. Unfortunately, the isolation mechanism used was not sufficient and in some cases a number of subsystems had to be simultaneously powered down in order to obtain the desire system power cycle.

4.3.2 External Asynchronous SCC Channels

SUNSAT has a total of 7×1200 baud FSK modems and 3×9600 baud modems. μ PD72001 Serial Communications Controllers can connected though multiplexers to the 1200 and 9600 channels. Each of the OBCs incorporate three μ PD72001 units. Each μ PD72001 has two independent full-duplex channels, each OBC thus has a maximum of six SCC Channels available at any one time. Redundancy is ensure as any of the three μ PD72001's can connect to any of the modem channels. The μ PD72001 is an advanced multi-protocol serial controller and has, amongst other, the following characteristics:

- ➔ functional superset of industry standard 8530 UART
- ➔ Asynchronous and Synchronous operation
- ➔ Character-oriented operation
(BISYNC/MONO-SYNC)
- ➔ Bit-oriented operation (SDLC/HDLC)

- Interrupt, Polling and DMA based host-system interfaces
- DC to 2.2 *Mb/s* data rate.
- NRZ, NRZI and FM encoding/decoding. Manchester decoding.
- Standby mode for reduced power consumption (Supply current of 20 *mA* versus 1 *mA* in Standby mode).

On **SUNSAT**, the μ PD72001's are configured to use the HDLC protocol and are used in interrupt driven mode. The μ PD72001 units have been connected in such a way as to enable the optional use of DMA on certain of the μ PD72001 units.

Provision has also been made to connect one or more of the available μ PD72001 channels to the L/S band bus (L-Band = 2-30 *Mb/s* uplink, S-Band = 65 *Mb/s* downlink). This allows the creation of a 51200 baud channel that allows the high speed upload of new flight software.

During the normal operations (after the system startup has been completed) of an OBC, the worst case would be the simultaneous use of three 9600 baud channels and three 1200 baud channels. The 1200 and 9600 baud modes are well within the capabilities of the μ PD72001's. The predominate limiting factor in the performance of the SCC channels will thus be the interrupt hardware and software overhead.

The HDLC protocol defines a data packet that has an initial start frame byte, N bytes of data, two CRC bytes and an end frame byte. An interrupt will be generated for each byte received/transmitter by the μ PD72001's. At 9600 baud and 8 bits/data byte, this translates to 1200 interrupts per second. At 1200 baud and 8 bits/data byte, this translates to 150 interrupts per second.

During the integration of **SUNSAT**, it was discovered that the Data-Carrier-Detect (DCD) signals provided by the modems did not function correctly. The ideal would be to use the DCD to switch on the μ PD72001 receivers only when a valid external signal is detected. Due to the problem with the DCD signal, the μ PD72001 had to be placed into a hunt mode. In this mode, the μ PD72001 continually scans the incoming bitstream for the HDLC framing start flag. When the starting flag is detected, the μ PD72001 generates an interrupt and the OBC initiates the frame receive sequence. When listening to receiver noise, the μ PD72001 will spuriously detect these flags, causing a continual interrupt load that wastes processor time. In subsequent designs, it is recommended that the problem with the DCD be analysed and corrected.

4.3.3 Internal Asynchronous Serial Channels

A number of *intra-satellite asynchronous channels* (ISAC) are used in **SUNSAT**. These are normally driven by KS82C52 UART units (the internal UART's of the Embedded processors are also used). These UART's are functionally identical to the industry standard 8252.

Amongst other, the ISAC connect to the **Sunsat Serial Bus** (SSB). This half-duplex bus connects the OBC to the telemetry and telecommand systems. The bus is used to send serial telecommand instructions (which allow control of the satellite) and receive telemetry data. The SSB runs in 9600 baud 8N1 mode (8 data bits, no parity, one stop bit). The maximum data rate is thus 960 B/s (and interrupt frequency of 960 Hz). The telecommand packets have a maximum length of 9 bytes, whilst the telemetry packets have a maximum length of 256 bytes. There is no redundancy for this bus. An unfortunately, this resulted in a single-point failure with regards to the power system. The power management system connects as a node to this bus. If this bus were to fail, all communication with the Power Management System would be lost.

A number of ISAC also connect to form what is known as the **Instrumentation Bus** (consisting of a primary and backup channel \rightarrow redundancy). The two Instrumentation Bus channels use the RS485 electrical protocol (multi-drop, differential transmission) in order to improve noise immunity. Both channels are configured for 19200 8P1 (8 data bits, 1 parity bit, 1 stop bit). This translates to a maximum interrupt rate of 1.75 kHz . The absolute maximum data rate is thus 1.7 KB/s . The Instrumentation Bus connects the magnetometer, the star camera on the gravity boom and the school experiments to both OBC's.

The software protocol implemented is a variation on the CSMA/CD protocol. A data packet size of 34 bytes has been chosen to optimally use the data channel capacity. The driver software that runs on the 8031 processors connected the Instrumentation Bus defines a maximum useful data rate of 1.23 KB/s (as mentioned above, the maximum is 1.7 KB/s). This represents a 72% protocol efficiency. The data packets from the magnetometer can arrive at a maximum of 450 B/s and are 9 bytes in size. The data packets from the star camera can range from 4 to 490 KB in size.

Lastly, the ISAC also connect to the GPS receiver. The GPS interface was designed to meet the predefined interface requirements of the NASA supplied GPS receiver. This link is configured for 19200 8N1 (8 data bits, 0 parity bits, 1 stop bit). The maximum data rate is thus 1.87 KB/s . This implies a worst case interrupt rate of 1.87 kHz . The **GPS serial channel** is only be used to receive "science" data from the GPS receiver. This data will arrive in the form of 2 KB bursts of data every 10 s .

4.3.4 Internal Parallel TCMD Interfaces

The TCMD interface consists of two unidirectional parallel data paths. A telecommand execution entails the output of a sequence of data words to the data port. Once the TCMD system has verified the command, the appropriate *command latch* is set and a return status sequence is sent to the OBC's. An interrupt signal is used to latch the return status sequence for processing by the OBC's. The telecommand execution rate is thus dependent primarily on the processor cycle time and the control software overhead.

In the final flight configuration, measurements indicated that the maximum telecommand execution rate for OBC2 is 7.2 kHz (versus 3.2 kHz for OBC1). The original specification

for the TCMD system required a minimum telecommand execution rate of 1 *Hz*.

4.3.5 Internal Parallel RAMDISK Interface

The RAMDISK interface consists of an unidirectional address bus and a bidirectional data bus. This interface is used by the OBC's to read or write data to the RAMDISK. The interface consists of an address latch and a data bus buffer and thus the data rate is largely dependent on the CPU and control software. The RAMDISK has been design to support transfer rates of ≤ 4.5 *MB/s*.

Initial measurements find the maximum data transfer rate to be 200 *KB/s* on OBC2. Evaluation of the control software revealed excessive procedure call overhead. A rewrite of the code in Assembler allowed a new maximum data transfer rate of 833 *KB/s*. This rate represents the effective maximum data rate through any 8 bit parallel interface on OBC2.

The RAMDISK generates an interrupt for every 8 *MB* of data transferred (when a memory bank has been filled). At 833 *KB/s*, this translates to a maximum interrupt frequency of 9.6 *Hz* on OBC2. The corresponding interrupt frequency on OBC1 will be considerably lower, due to the slower clock frequency of the processor. The current Flight Software does not make use of this interrupt.

4.3.6 Internal Parallel IMAGER Interface

Although the RAMDISK system provides all control signals for the IMAGER system, either of the OBC's can request RAMDISK/IMAGER to initiate an image scan. The IMAGER interface consists of an unidirectional data bus and two address lines (data flow towards IMAGER). The maximum data transfer rate of this interface is dependent largely on the CPU and control software. Due to the nature of the interface and the intended use, the maximum data rate is however of little concern. Interrupts are generated at 700 *Hz* (determined by the IMAGER) and allow OBCs to add in-line telemetry data to the image being captured.

4.3.7 Internal Parallel DSP Interface

The DSP has been added to **SUNSAT** in order to perform digital modulation experiments. The DSP interface consists of a bidirectional data bus and an unidirectional address bus. One possible application of the DSP would be to implement 5×9600 baud modems. This would require a data transfer rate of approximately 6 *KB/s*. The maximum rate at which the DSP could generate data is 150 *KB/s* (due to the DSP system design). A 150 *KB/s* data rate translates to an interrupt frequency of 150 *kHz*, which far exceeds the possible interrupt frequency of either of the OBC's. It was found in practice that polled mode operation, together with large FIFO buffers, was the most effective communication mode for OBC \leftrightarrow DSP data exchanges.

4.3.8 Internal Parallel ADCS Interface

In order to increase the redundancy of **SUNSAT**, a parallel interface to the primary ADCS control bus has been added to OBC2. The purpose of this bus is to allow direct access to all the satellite sensors in event of the ADCS T800 failing. This bus can also be used to directly control the reaction wheels and magneto torquers. Under normal conditions, OBC2 will however not use this bus.

The interface consists of an unidirectional address bus and a bidirectional data bus. Due to the length of the address and data path from OBC2 to the sensors, the maximum data rate is dependent on the wait states configured for this memory mapped interface. The wait states are in turn dependent on the signal propagation delays along the communication channel (the extensive parallel reaction wheel bus) and the target device limits.

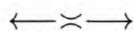
4.3.9 Internal ADCS T800 Transputer Interface

The T800 Transputer is part of the ADCS system and is responsible for the control of the satellite. Under normal conditions, the T800 receives data from the attitude sensors and performs the required orbital calculations. The actual control of the satellite is performed by the ADCS 8031 which controls the reaction wheels and magneto-torquers. The OBCs use the ADCS T800 interface to send high level control commands to the T800 (e.g., to change the Z-axis spin rate). The T800 also sends configurable sensor and filter data to the OBC's via this interface. The OBCs log this data in the WOD files for later analysis on the ground.

4.3.10 Discussion

The communication system of **SUNSAT** represents a significant load on the OBC's with respect to the processing of communication system interrupts. The efficient coding of interrupt service routines has improved the situation. During normal operation, it has been found that the interrupt load on the OBC1 has been manageable. In a few cases, special steps had to be taken to combat data loss due high interrupt loads. More specifically, during the gathering of GPS data, the SCC interrupts were disabled.

Another side effect of the communication structure described is the complex cable harness required to link the subsystems of **SUNSAT** together. This hardness proved to be a source of hard to find anomalies. The useability of the engineering model of **SUNSAT** is also seriously hampered by the cable harness. It is therefore recommended that an alternate communications architecture be investigated for subsequent satellites.



Chapter 5

Logic Modeling

Due to the enormous costs involved in producing design prototypes, there is a trend towards computer simulation. Most developers find it convenient to define a model of their designs and subsequently using computers to verify the accuracy of their models. Costly errors can thus be eliminated before the design is physically realized. The design can also be altered at a fraction of the cost, whilst the results of these modifications can be studied in near real-time.

In the context of digital design, the models used are not of a mathematical nature but rather logic models. They can however be analysed by means of computer simulation in the same fashion as mathematical models. Logic models can also be used for the synthesis of optimized logic. In the order to optimize the future design processes of locally developed satellite subsystems, it was decided that an attempt would be apply logic modeling to a sample OBC design.

This chapter presents an overview of logic modeling principles and practices. The chapter also details background work done aimed at creating a logic model of an on-board computer design. This attempt was made in order to reduce the development cost of an on-board computer system.

5.1 Concepts

Logic modeling can be either a design tool, a verification tool or both. The usefulness of a model is determined by how closely it can represent the corresponding physical design. It is therefore important to analyse all models carefully in order to ensure that they are indeed of value. Not all models are worthless when their behaviour deviates from the physical design. If the deviation is properly understood, even inaccurate models can be of some use. The concepts involved in Logic modeling will now be examined.

All engineers have encountered the concepts of “top-down” and “bottom-up design. These concepts are also found in logic modeling, although encapsulated in different terms. Under the logic modeling paradigm, the description on a design can be done in three possible do-

mains. The primary tool used during logic modeling is the high-level description language (HDL). The three description domains are:

- ① **Structural:** The design is described in terms of modules and symbols interconnected by lines/names (design is done by means of schematics and/or HDL).
- ② **Physical:** The design is described in terms of blocks and cells interconnected with lines (design done at artwork and/or fuse map level).
- ③ **Behavioral:** The design is described in terms of modules interconnected by named (design done in HDL).

Most practical logic models describe designs using at least two of the description domains. A physical description, by its nature, cannot be optimized by an CAD tool. Behavioral description, on the other hand, being a high level description can be optimized by a CAD tool based on certain constraints. Therefore, when creating a logic model, the behavioral description of a design should be used wherever possible. Another advantage of a high level description is the technology portability that is obtained. In all cases, the designer is however required to have a thorough understanding digital design principles. In particular the correction partitioning of synchronous and asynchronous logic is crucial to successful and optimal design.

5.2 Modeling Tools

New and ever more advanced modeling tools are continually entering the electronic design market. The following tools were locally available when this attempt at system level modeling was initiated:

- ① Synopsys, together with the Smartmodels Library.
- ② Altera Maxplus II.
- ③ Xilinx Foundation Series.

The last two tools mentioned above are designed to support the development of FPGA based designs and do not have system level modeling capabilities. The modeling of the on-board computer was therefore undertaken using the Synopsys environment.

5.3 Modeling the Intel386 Processor

It was decided that an on-board computer based on the design of OBC2 would be an ideal test environment in which to evaluate the useability of modeling tools. The CPU being

central to the design of an OBC, a model of the CPU was required in order to verify the design. The Smartmodel Libraries (part of the Synopsys package) makes available predefined models of the following members of the 80x86 family of processors:

- ① 80386DX (12MHz, 16MHz, 20MHz, 25MHz, 33MHz)
- ② 80386SX (16MHz, 20MHz, 25MHz, 33MHz)
- ③ 80486DX (25MHz, 33MHz, 50MHz)

In all cases, only hardware verification models were available¹. As the CPU chosen was the 386EX, the lack of a suitable model proved problematic. After a thorough examination of the 80386 processor family, it was found that the 80386EX was fundamentally a 80386SX packaged together with selected peripheral devices. It was initially thought that the 80386SX could form the core of a 80386EX model. The primary disadvantage of this approach stems from the limitations of the hardware verification model.

After an attempt was made at emulating a 386EX, it became evident that this emulation would require significant development effort. The 80386EX has a number of outputs which are not present on the other members of the x86 family of processors (for example: `WR#`). These signals are synchronized with the bus interface unit (BIU) of the 386 core. When a Smartmodel Model is used, there is no way in which the BIU states can be directly accessed. Any emulation of the additional signals would therefore require an external bus state follower. The timing of some of the additional signals are however critical to the 386EX functionality and can not be adequately emulated without direct access to the internal BIU states. For example, `WR#` must be deasserted before the end of the last non-idle bus state of the BIU. Due to, amongst other misaligned accesses, code prefetches, bus hold requests, DRAM refresh cycles, wait states and combinations of the previous, the creation of an adequate external bus follower rivals the complexity of fully functional BIU.

Another approach would be to create a VHDL 80386EX model. At the point in time when this stage of the investigation was reached, no local knowledge about the creation of a complex logic models existed. It was therefore decided that the implementation of such a model would prove to be an instructive exercise. Although this turned out to be an extensive task, the effort led to a better understanding of the processor. The following section describes the 386 processor core and the core models created for this project.

5.3.1 Overview of the Intel386 processor core

Fig. [5.1] gives a block diagram representation of the 386 class processors. The full implementation of a 386 core was consider to be beyond the scope of this project. In particular, the protect mode extensions (*i.e.* segmentation and paging) represent a considerable amount of work. As `SUNSAT` software exclusively uses real-mode, and the processor mode

¹Hardware verification models provide a basic timing verification model. These model are not fully functional and are normally controlled via PCL (Processor Control Language) script.

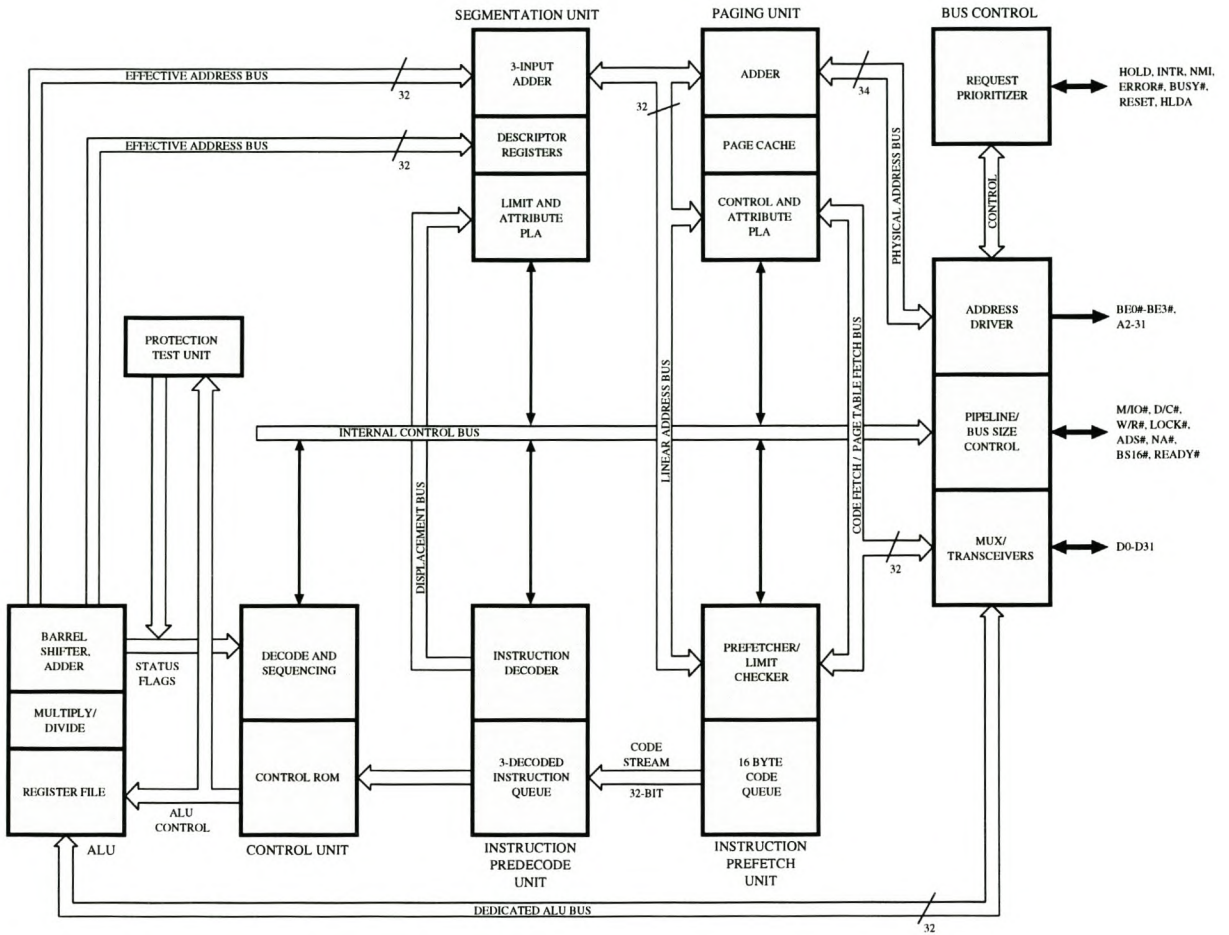


Figure 5.1: Intel386DX Block Diagram [33].

does not influence the interface characteristics of the processor, it was decided that protect mode extensions would not be attempted. Therefore, with reference to Fig. [5.1], the following modules were implemented:

- ① Bus Interface Unit (Address Driver, Pipeline/Bus Size Control, Mux/transceivers).
- ② Instruction Prefetch Unit (16 byte code cache)
- ③ Instruction Decode and Execute Unit

5.3.2 The Instruction Decode and Execute Unit

The detailed nature of the IDEU in the 80386 processors is unknown and no documentation could be obtained. It has been claimed by some that clone producers used clean-room reverse engineering in order to obtain their respective implementations. For the purpose of this project, a minimal version of the IDEU was implemented.

5.3.3 The Instruction Prefetch Unit

The 80386 family of processors implement a 16 byte code prefetch unit. This unit functions in parallel with other units in the processor and continually fills the instruction queue with instructions by initiating code fetch cycles in the Bus Interface Unit (BIU). The Instruction Decode and Decode unit accesses the IPU to obtain the next instruction to decode and execute.

5.3.4 The Bus Interface Unit

The state definition of each bus cycle is given by three definition signals: $M/IO\#$, $W/R\#$ and $D/C\#$. At the same time, a valid address is present on the enable signals $BHE\#$ and $BLE\#$ and the other address signals $A1-A25$. A status signal, $ADS\#$ indicates when the processor issues a new bus cycle definition. Collectively, the address bus, data bus and all associated control signals are referred to as “the bus”.

When active, the bus performs one of the bus cycles below:

- ① read from memory space
- ② locked read from memory space
- ③ write to memory space
- ④ locked write to memory space
- ⑤ read from I/O space

- ⑥ write to I/O space
- ⑦ interrupt acknowledge
- ⑧ indicate halt, or indicate shutdown

When the processor is not performing one of the listed bus cycles, it is either in Idle (**Ti**) or in the Hold Acknowledge state (**Th**). The shortest time unit of bus activity is a bus cycle. A bus state (called a T-state) is one processor clock period (two CLK/2 periods) in duration. A complete transfer occurs during a bus cycle, composed of two or more bus states. Every bus cycle continues until it is acknowledged by the external system hardware (using the **READY#** signal). Acknowledging the bus cycle at the end of the first **T2** results in the shortest bus cycle, requiring only **T1** and **T2**. If **READY#** is not immediately asserted, however, **T2** states are repeated indefinitely until the **READY#** is sampled asserted.

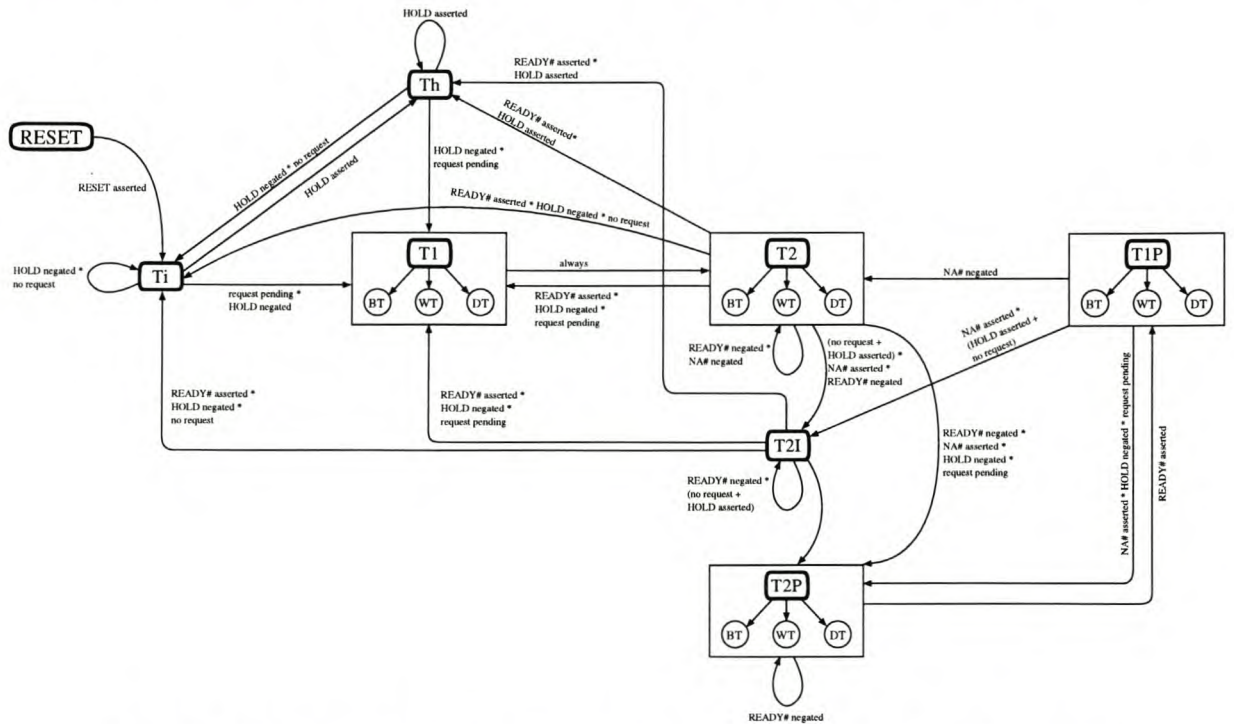


Figure 5.2: Intel386 Generic Core - Bus T-State Machine Flow Diagram

Fig. [5.2] gives a flow diagram of the possible bus states. Note that the circles with **BT**, **WT**, **DT** refer to Byte Transfers, Word Transfers and Double Word Transfers. Fig. [5.3], Fig. [5.4], Fig. [5.5] depicts the bus state changes required for the different transfer modes (for the 80386DX processor). In these figures, the signal assertion/assignment is shown for each of the states (in the square boxes). “W:” and “R:” designate the assignments for the Write and Read accesses respectively.

Note that some of the bus cycles require a number of T-state cycles in order to complete the data transfer. For example, a double word transfer from a misaligned address across

Table 5.1: Legend: Signal Definitions

Name	Description
BE	Byte Enable
EDATA	External Data Bus
MUXDATA	Internal Data Bus
BS16#	16-bit Bus Select
EADDR	External Address Bus
MUXADDR	Internal Address Bus

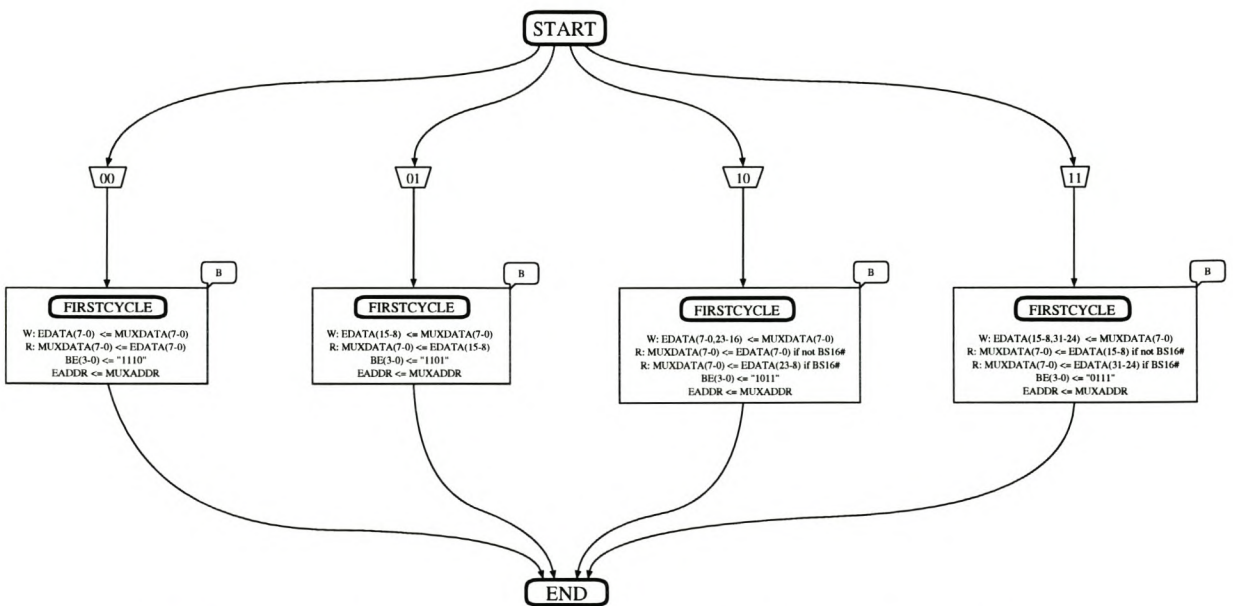


Figure 5.3: Intel386DX - Byte Access State Machine Flow Diagram

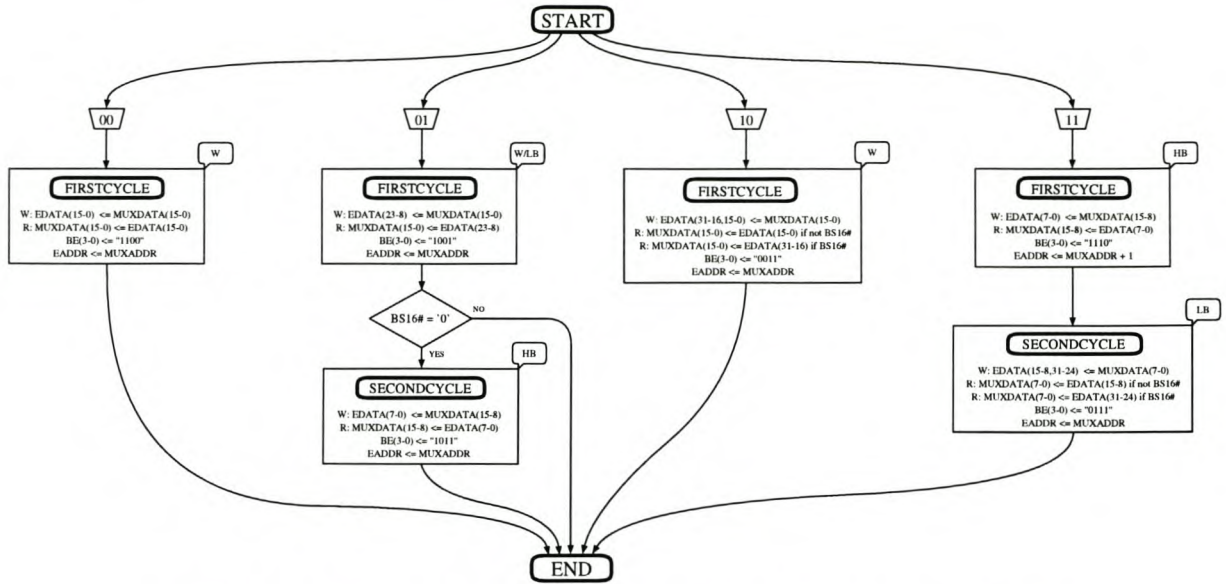


Figure 5.4: Intel386DX - Word Access State Machine Flow Diagram

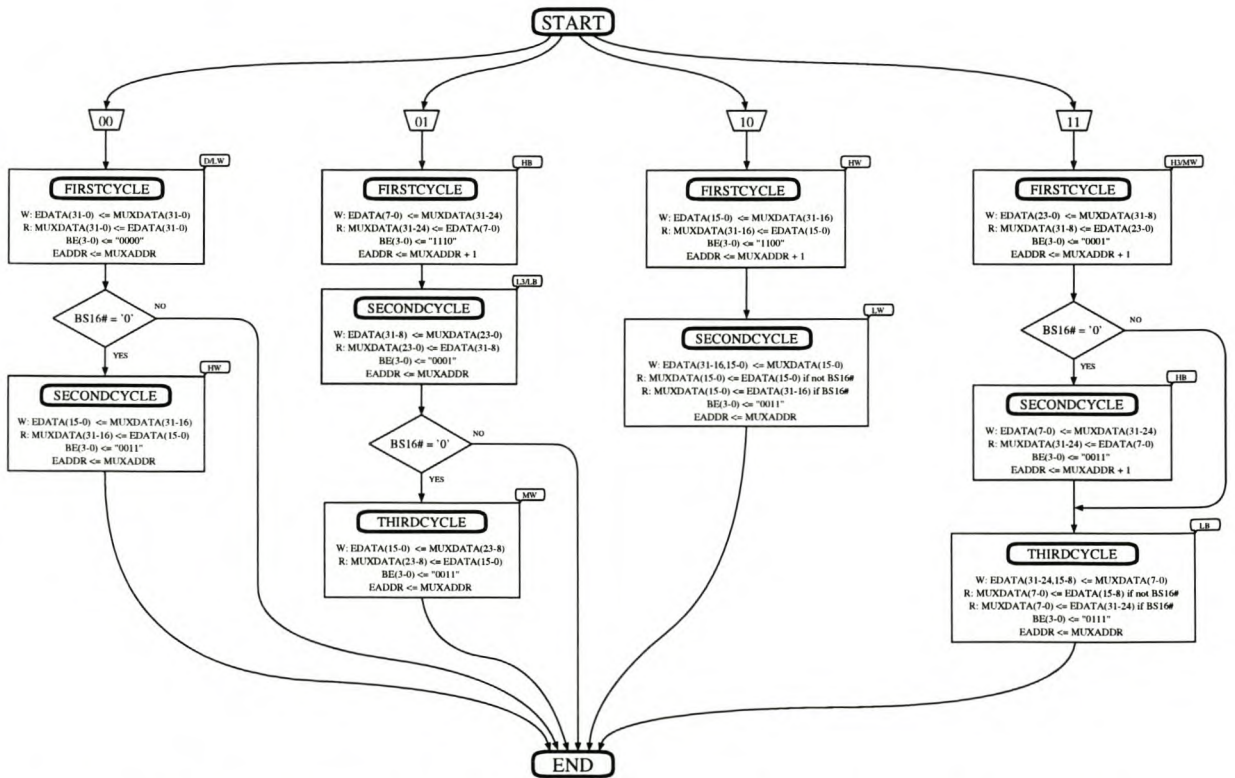


Figure 5.5: Intel386DX - Double Word Access State Machine Flow Diagram

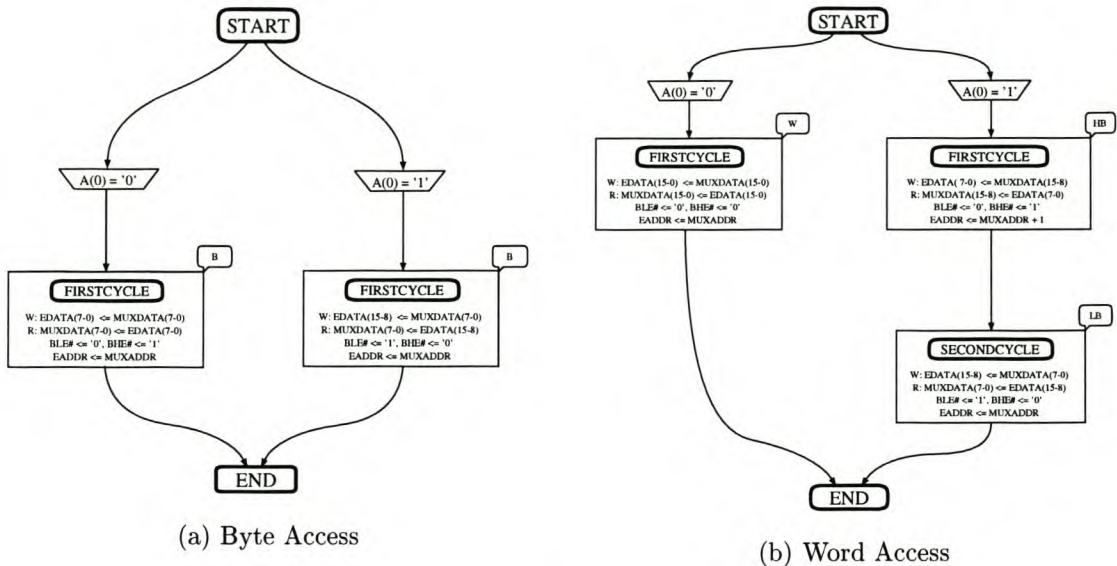


Figure 5.6: Intel386SX - BIU State Machine Flow Diagram

a 16-bit bus requires at least three bus T-states to complete the transfer. The MW, HB, LB, etc. indicate the Middle Word, High Byte and Low Byte.

The BIU of the 80386SX processor is very similar to that of the 80386DX, the primary difference being the width of the data bus (always 16-bit). The transfer modes of the 80386SX BIU can therefore be obtained from the 80386DX transfer modes by removing the BS16 branches. Fig. [5.6] and Fig. [5.7] show the resultant flow diagrams.

The 80386EX goes one step further in that it makes provision for 8-bit transfers. Flow diagrams of 80386EX transfer modes are given in Fig. [5.8] and Fig. [5.9]. As can be seen, these transfer modes differ substantially from that of the 80386SX. The BIU of the SX and EX processors are thus sufficiently different to prevent the emulation of an EX through the use of a SX processor.

5.3.5 The partial Intel386EX Functional Model

As originally designed, the 386 core relies on the **READY#** signal to terminate processor controlled bus cycles. This implies that all peripherals attached to any processor based on the 386 core are responsible for the generation/control of the **READY#** when being accessed by the processor. This increased the complexity of designs based on the 386 core.

In order to simplify designs based on the 386EX, Intel added the on-board chip select unit. This unit, programmable via software, allows the selection of external devices based on the current address on the processor bus. It also automatically handles the generation of the **READY#** signal.

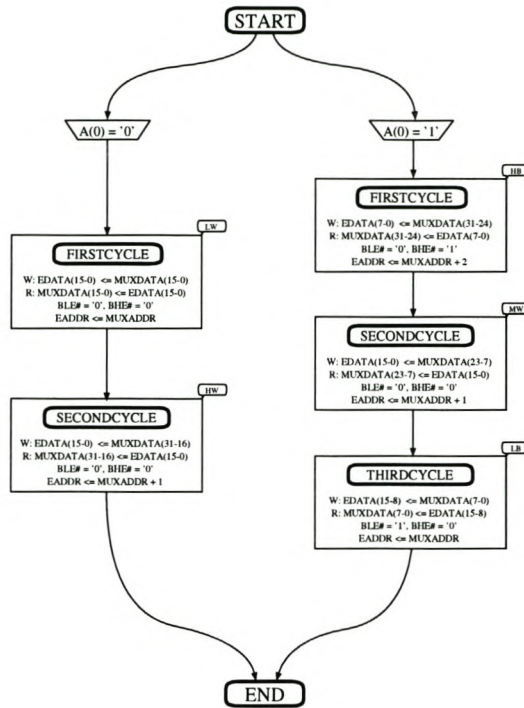


Figure 5.7: Intel386SX - Double Word Access State Machine Flow Diagram

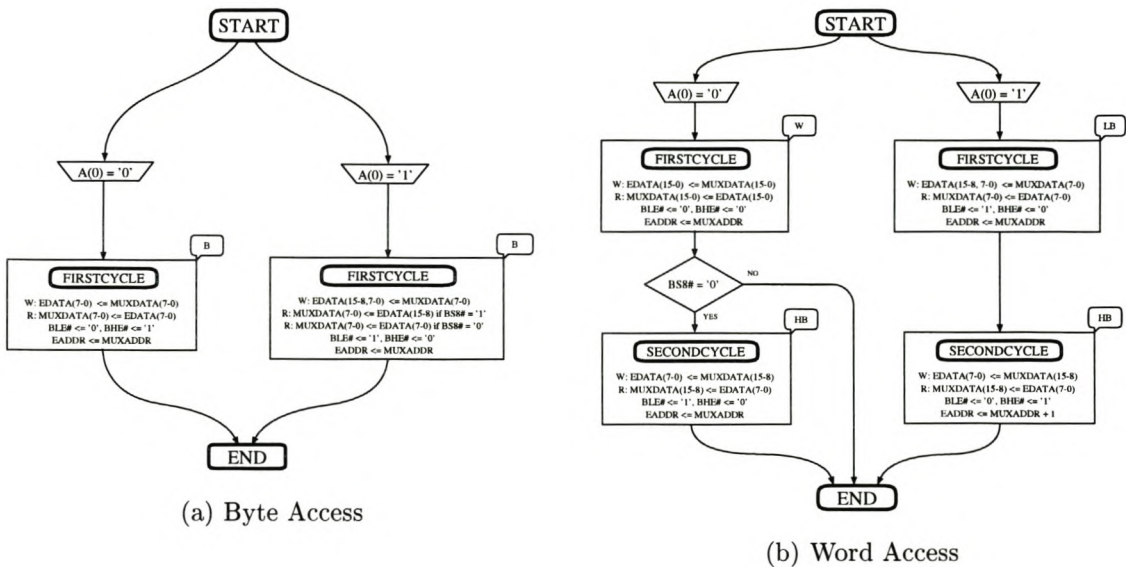


Figure 5.8: Intel386EX - BIU State Machine Flow Diagram

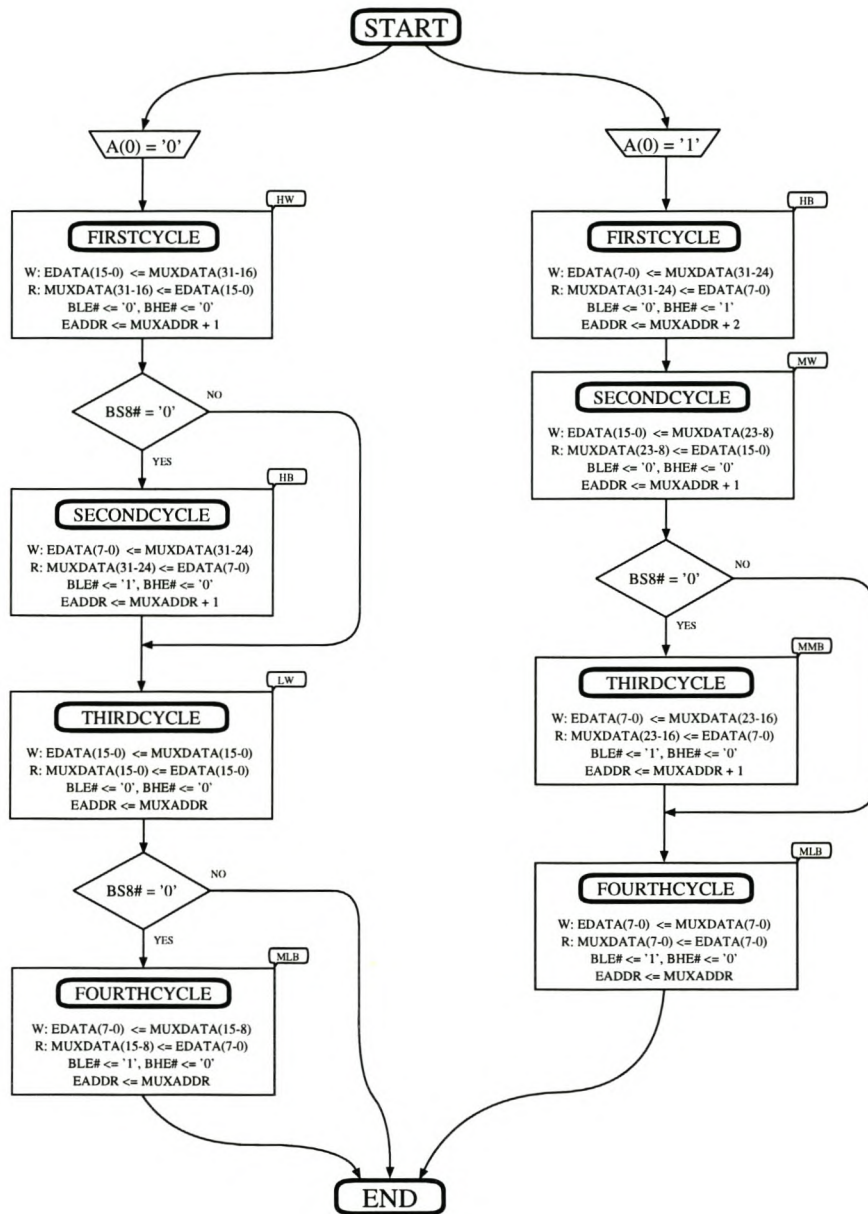


Figure 5.9: Intel386EX - Double Word Access State Machine Flow Diagram

The implemented model consists of a number of programmable registers (whereby the chip select lines are mapped) and a state machine. The state machine follows the 386 BIU states and, depending on the configured wait states, generates the `READY#`.

5.4 Comments

Once a basic implementation of the CPU was completed, a primitive system level model of the sample on-board computer was constructed. It soon became evident that the locally available computational resources (for Synopsys development) would prove to be problematic; each simulation became a lengthy process. A full synthesis/elaboration cycle was soon requiring several hours. A simulation run (controlled by scripts), was similarly requiring close to a hour of setup and simulation time. Thus, from a resource perspective, a medium or large scale system level simulation is not feasible given the available resources.

The development of the 386EX model required considerable effort. The result was less than ideal in that the model did not support the full 386 instruction set. Furthermore, the lack of the protect mode implementation contributes to the final conclusion: the logic model did not accurately reflect a real-world 386EX. It is therefore doubtful that many of the more subtle problems experienced during OBC2 integration would have been detected by modeling.

The total cost of system level modeling (powerful computational resources, costly software, experienced designers and considerable modeling time) is therefore relatively high. When compared with the cost of a multiple prototype based development process (whereby `SUNSAT` was developed), system level model is not currently an economically feasible methodology for small scale projects.



Chapter 6

Conclusion

In the previous chapters, an overview of some of the aspects which influence the design and in-orbit performance of an OBC has been presented. In conclusion this chapter presents a compendium of selective design and implementation guidelines for a LEO satellite and in particular the On-Board Computer. The guidelines given below are based upon the experiences with **SUNSAT** and the experience of another satellite developer [6].

6.1 General Design Methodology

6.1.1 KISS (Keep it simple, stupid)

This rule should be considered fundamental. Examine thoroughly the task and environment of each subsystem and specify components/techniques that will accommodate the task with a suitable, realistic safety margin. The functionality of each subsystem should be the minimum required to obtain the core satellite requirements. All experimental and additional functionality should be delegated to secondary payload modules. Following this rule will allow the rapid deployment of the core system, the end effect of which will be greatly reduced risk.

6.1.2 Base core on proven designs

The essential core subsystems responsible for the base operations of the satellite should use standard, proven designs and hardware. The core should be designed conservatively, resisting the incorporation of any technology that has not been verified to be acceptable in the space environment (as evident by its successful application on a locally build satellite).

6.1.3 Redundancy for core

Redundant paths and subsystems should be added for all critical systems. At a minimum, two reliable paths should be available between the nodes of the core system. With the appropriate care, less proven designs or technologies may be used for additional redundant paths (provided that these paths are not associated with potential single point failure nodes).

6.1.4 Redundancy via diversity

Redundant paths should use diversity rather than duplication. This helps guard against subtle design errors or technology flaws that are triggered in rare, untested situations. For example, in the case of UARTs, pin compatible components from more than one manufacturer should be used. If pin compatible components are not available, the device under consideration may not be suitable for the design (if only one manufacturer produces the component, it should not be considered a standard component).

6.1.5 Use simple interfaces

The simpler the interfaces between subsystems, the easier they are to design, verify, implement, adapt and test. As a bonus, they will typically require less interconnects, thus produce less EMI, weigh less and require less power during operation.

6.1.6 Distributed design

Subsystems should run independently of other subsystems even if that entails duplicated hardware (unless there is an overwhelming advantage to be gained from intimate subsystem interaction). There should be no dependence of the core system on any non essential subsystem. This allows these non-essential subsystems to be powered down during low power conditions (which occur for most LEO satellites).

6.2 The Core

In the satellite business, the term “satellite bus” is often used to reference the satellite structure and core satellite systems required to support “payloads”. The power management system, communication system, the attitude control subsystem and the flight management system are the primary components of the satellite bus.

In Chapter 4, the architecture of **SUNSAT** was described. One of the lessons learned from **SUNSAT** was that parallel interfaces between subsystems and high interface counts are highly undesirable. For this reason, it is recommended that parallel interfaces be avoided

for a revised satellite bus. A limited number of standard asynchronous serial interconnects, used in conjunction with bus standards such as RS485, are the recommended inter subsystem link fabric (and these are found on the majority of microsatellites).

The RS485 standard is a well established and pervasive serial bus implementation. A wide selection of RS485 driver components are available from a number of manufacturers. These devices therefore easily obtainable and low cost. Furthermore, their use in harsh environments has led to the development of exceedingly robust versions (with features such as $15kV$ ESD protection, thermal shutdown and short circuit protection). There also exists micro-power versions of the RS485 drivers that have standby supply currents down to $2 nA$ and operation supply currents of $30 \mu A$.

Modern alternatives to standard serial buses, such as CAN and USB, have been available and are becoming established. These serial buses, whilst having distinct advantages over the older serial buses in their target domains, do not necessarily offer significant gains in the FMS design domain. Furthermore, as neither of these technologies have been locally qualified for use in space, they should therefore not be used in a new satellite bus. In order to qualify them for future use, it is recommended that selected secondary payloads be designed to use CAN. Once the new technologies have been proven (on a locally built satellite), they can be integrated into the satellite core.

6.3 Selected guidelines

During the design of future OBCs, the aspects listed below should be kept in mind. Their application will not guarantee that a new design will work flawlessly, but should help minimize the number of design iterations and the number of late nights spent getting it to work...

6.3.1 Component Selection

Design essential systems around established, industrial, high-grade, volume production components. If a component has been in volume production it is highly likely that any 'bugs' have been removed. Use exotic technologies only in non-essential or redundant systems (if at all). In order to ensure the correct selection of components, an organized approach to component selection should be followed. A formal component selection procedure should be therefore be developed and consistently applied for the core satellite systems.

Military standard components are available that have extended thermal and electrical specifications. If required, these components should be investigated. It should be noted that MIL-SPEC components may not necessarily imply higher reliability. It has been found that in certain cases [88] MIL-SPEC components were responsible for most of the component failures recorded. A number of manufactures produce radiation hardened components [23, 28] that may be investigated, subject to budget constraints.

The following aspects should form part of a component selection specification:

- Components must have acceptable radiation tolerance (Chapter 3).
- Components must have acceptable thermal tolerance and characteristics.
- In most cases the use of CMOS devices is mandatory (versus bipolar). This criteria stems from the low power consumption of CMOS logic. Furthermore, bipolar devices are more sensitive to radiation dose effects as well as accumulated neutron damage.
- Wherever possible, components with power saving facilities (standby, idle, sleep modes) are advised.
- High integration components are only to be selected after due consideration of the increased risk.
- The out-gassing characteristics of the component must be evaluated.
- J-lead or DIP packaging is recommended (SMT can also be used, although considered less ideal).
- Component availability must be taken into account during the selection. Choose components that are produced by more than one supplier. Components produced by only one supplier will inevitably cause logistical problems (higher costs, more difficult to obtain, more likely to be discontinued, *etc.*).
- Component reliability as witnessed by a history of successful use, must be considered. The use of very new and untested technologies is strongly discouraged. For complex integrated circuits, use of early versions of the component, is strongly discouraged.

6.3.2 Component Derating

The AC and DC specifications of components are normally given with respect to an earth based environment, room temperature and typical supply voltage. If the component is used in an environment that differs from the typical, the specifications of the component differs accordingly. This variation in component specification must therefore be taken into account.

The most common way in which component specification variations are taken into account is by *derating* the maximum and/or minimum specifications of the component. By derating a components parameters by these factors, an adequate safety margin is ensured. The derating policy reduces the occurrence of stress related failures and helps ensure long term reliability.

A number different guidelines could conceivable be used for such derating. Both NASA [67] and ESA [68] have published derating guidelines for different component classes. In the design of *SUNSAT*, the ESA derating were applied. For the design of a new FMS, the derating specification of the target satellite should be used. This derating specification should be defined before any of the satellite subsystems are designed (and it is recommended that both the NASA and ESA specification be used as a templates).

6.3.3 System clock design

The clock design must be checked to ensure that it will reliably work correctly under various conditions (temperature extremes, vibration, after low power conditions). Clock gating is an exceedingly bad practice and significantly increases the risk of timing hazards. The resultant design is also considerably more sensitive to component variations, PCB layout and temperature. Ensure that no clock gating has been inadvertently added to either discrete logic or to any programmable device (FPGAs, CPLDs, *etc.*)

When the system clock is used to drive multiple devices in the system, ensure that the traces from the clock source to each device is of equal length. When large numbers of ICs comprise a synchronous logic block, such as a large state machine, be very careful of clock tree layout. All logic must be fed by the same clock and the clock should be routed so each input receives the clock at the same moment (*i.e.* minimize clock skew). When multiple legs of a clock tree are required to feed a synchronous block because of loading, ensure that clock signals required by a particular block are driven by the same IC, the traces are of equal length and are equally loaded. The check must be done for DC loads (fanout) and AC loads (wiring and input capacitance).

6.3.4 Memory and I/O design

SRAM is the recommended volatile memory technology for an OBC. The HM638512 device is the recommended SRAM device and combines a number of features that make it the optimal choice: low power consumption, acceptable (medium) access speed and the fact that it has been used successfully on **SUNSAT**.

For non-volatile memory, Flash memory still remains the optimal choice. Dual supply Flash devices should be used, as was done in **SUNSAT**. Single supply devices should be avoided due to the danger of upset in the charge pump. The programming power of the device should be switchable. There should be sufficient software “slots” (areas that are large enough to store the entire flight software). This allows one “working copy” to be kept whilst testing a new version. The flight software (written in C and Assembler) of a microsatellite of **SUNSAT**’s nature will require approximately 256KB per image. When sufficient flash memory is available, the number of flash erase cycles are reduced.

A processor that provides an internal chip select unit greatly reduces the additional decoding required and it is advisable. Some processors provide automatic termination of memory and I/O cycles while others require external hardware to terminate the cycle. If at all possible, select a processor that provides an internal bus control unit where the bus cycle termination is programmable. Care should also be taken to ensure that the bus buffers are correctly controlled. In certain processors, a number special cycles are defined that are used to manage registers inside the processor (*e.g.*, page table load cycles). These cycles are problematic in that read/write cycles can follow unusually close to each other as these cycles are caused by a single CPU instruction. To prevent unexpected surprises, an evaluation board for the CPU should be purchased (or a simple prototype built) and these cycles examined using a high speed logic analyzer. Further, it should be noted that these

special instructions (and many related to the control of the CPU memory management unit), require writable memory.

Ensure that all memory and I/O port widths match CPU, DMA and software requirements. Many processors, DMA, and bus masters require data port widths to be a fixed width, such as 32 bits. While it is possible to map an 8-bit device onto a 32-bit bus, be careful that the implications are acceptable to software engineers and compatible with alternate bus masters. The bus access cycles of each peripheral should be checked for any special sequence requirements that may not be possible given a particular OBC design.

6.3.5 Interrupt system design

Most microprocessors allow an interrupting device to supply a vector number when an interrupt is acknowledged. This vector number is used by the processor to point to a unique interrupt handler for the interrupting device. This method speeds interrupt processing by eliminating the need to poll multiple interrupt sources that may be sharing the same interrupt request. In **SUNSAT**, this was not done and resulted in unnecessarily complex interrupt handlers. It is recommended that all peripheral devices are connected so that this interrupt processing technique can be used.

Normally a unique bus cycle is provided by the processor during the interrupt acknowledge. In this cycle, the interrupting device provides the vector number as data to the processor and must terminate the cycle via a cycle end acknowledge signal. Provisions must be made to terminate this cycle if no interrupting device ends the cycle. In this case, the interrupt may have been caused by noise on the interrupt request. If hardware does not terminate the cycle, the processor may be hung indefinitely. Care should also be taken to ensure that the bus buffers are correctly controlled during this cycle. Due to the unique nature of this cycle, the CPU bus control signals do not sequence as for memory or I/O accesses. The bus buffers control will therefore need to explicitly make provision for interrupt cycles.

Microprocessors and microcontrollers generally have interrupt and exception vectors mapped to a fixed area of memory. These areas are generally at the bottom or top of memory space. Real memory must be mapped into these spaces for all possible vectors. If an unexpected exception occurs and memory does not exist in the space allocated for this vector, the processor may corrupt data and crash.

Ensure that interrupt and DMA devices are assigned to appropriate IRQ and DMA levels to meet latency requirements. Microprocessor subsystems (e.g., communications) should also be optimized for performance and latency requirements. By assigning time-critical data movement to higher priority DMA levels, bus master priority, or interrupt levels, the subsystem latency may be met.

6.3.6 Multiple drivers

List all nets that have multiple drivers. Use calculated maximum and minimum paths to verify that multiple drivers are never enabled, even when one path to disable is maximum and another path to enable is minimum. Driver contention may cause intermittent RF noise due to high-speed, high-current fluctuations and over time may actually damage the contending drivers. The best method for driver control is via state machine. A state may be inserted between driver tenure to ensure that contention does not exist.

6.3.7 Real-Time Clock

In Chapter 4, the motivation for the inclusion of a RTC was given. The component selected is not critical, but should have the desired characteristics as described in Section 6.3.1. Note that RTCs which include an internal backup battery are not acceptable due to the likelihood of out-gassing.

6.3.8 EDAC

To minimize the SEU rate of a LEO OBC, an EDAC should be added. The well known Hamming code, such as the (8, 12) code, based EDAC design is generally considered to be acceptable for use in an OBC. Given that the primary OBC of **SUNSAT** has functioned without EDAC since launch, the EDAC is not considered to be a mission critical component of the OBC. For this reason, a single-chip solution is recommended to minimize space.

Based on experience with **SUNSAT**, EDAC should be designed so that it can be disabled. Furthermore, the design must be such that the EDAC is testable. Not only must you have the ability to test the EDAC in the design prototypes, it must also be testable in a live production system. Adding the ability to change the contents of the main memory and the check memory separately allows any anomalies / failures to be diagnosed. This gives valuable data that can be used to improve the performance and reliability of the EDAC design.

6.3.9 Source termination

Avoid lengthy high speed logic signal lines. If their avoidance is not possible, the high speed signal line must be correctly terminated to prevent reflections. The recommended termination technique [1] consists of a series resistor located as close as possible to the source of the digital signal (hence the name *source termination*). This technique is only useful if the receiving logic are clustered near the end of the signal line. If this is not the case, the PCB layout must be changed to minimize reflections. A high-speed PCB expert should be consulted.

6.3.10 Powerup and reset

The DC-to-DC converters used to connect the OBC to the satellite power bus do not all have "soft-start" circuitry. The power transients caused by the converters must be examined. If necessary, clamping circuitry must be provided. Note that the clamping circuitry may produce secondary effects, such as oscillation.

Verify that all flip-flops, latches, microprocessors, and other memory-based logic are provided with a power on reset state. All states should be clearly defined and mutually exclusive of any other state. Map any unused states to the idle state. Proper state machine etiquette requires that the machine return to idle at a reset. All conditions for transfer to another state must be mutually exclusive. If these conditions are not met, a "catch-all" should map all other cases to a defined state. If possible, design the reset state to be the "all-zero" state (where all the state memory elements have a logical '0' value).

All logic should be provided with a software-driven reset state. This will help minimize the scope of the recovery steps required to restore the system to a functional state after an upset or software bug. A major system reset/power cycle can thus be averted (which would typically imply a greater loss of state).

6.3.11 Signal termination

Good design practice never allows unused floating input pins. If a pullup or pulldown resistor is shared by several input pins, ensure that no pin in the net is bidirectional. Bidirectional pins must have dedicated pullup or pulldown resistors. When available, follow the manufacturers specification for terminating signals from a device. Note that in many cases pins that are used also need to be terminated.

Many embedded controllers and microprocessors allow DMA and IRQ requests to be masked in software. It is still advisable to pullup or pulldown unused DMA and IRQ inputs for safety. Allocate a resistor per unused, never share the pull up/down resistor. Since these inputs are generally tri-state or open-collector driven, a simple wire add can allow expansion by incorporating one of these inputs (and minimize changes when you need to use the pin).

Open-collector and tri-state driven nets require a pullup or pulldown resistor to ensure that inputs on the net do not see a floating input voltage level. If the net floats at the ICs switching threshold voltage, the ICs outputs may change. Ground bounce causes this input voltage to appear slightly lower and the outputs may again change. This may escalate into wild oscillations, generate drastic RF emissions, and possibly cause system failure.

If power considerations are important, the bus-holder technique should be evaluated [3] as an alternative to pull-up or pulldown resistors in tristate buses. This technique makes use of an active bus termination. Certain manufactures produce bus driver components that incorporate bus-holders. These components should specifically be considered when selecting bus drivers.

6.3.12 Minimize logic

There should be no more than one set of buffers between the CPU and each peripheral. If a static analysis shows that the output loading exceeds the accepted limits, the design should be considered to be complex and analysed in order to find simpler alternatives. If at all possible, the OBC design should be such that HC devices can be used. AC devices contribute to the EMI of the system as they cause excessive ringing and will require additional PCB layout effort [1].

6.3.13 Bypass capacitors

Each IC should be supplied by a 100 nF capacitor. Ensure that the bypass capacitors are rated at 150% of standard supply voltage. This is a rule of thumb based on the possibility of a power-on surge from the supply DC-to-DC converter. Some supplies may specify this value and duration for a given load and provide a possibility to reduce the capacitor ratings closer to the maximum supply voltage.

Verify any microprocessor is bypassed according to manufacturer's recommendations. Verify at least one bulk bypass capacitor of at least 4.7 μF per 20 ICs. Locate at least one bulk bypass at the power supply feed pin for each supply to the PCB. Very-high-speed logic (less than 1 ns rise time) will require special RF filter caps. See high-speed logic manufacturers' recommendations.

6.3.14 Timing and static analysis

To ensure that the design will function correctly, the time consuming static and timing analysis must be done. Analyze and verify setup, hold and access times for data, control and address buses. Check the timing of little used logic such as reset or the watchdog.

6.3.15 External I/O signals

Telecommand signals are typically used to drive control inputs on the OBC. For example, telecommand signals are used to switch on/off the programming power to the Flash memory devices. Check that the inputs are properly filtered from noise on the telecommand signals. The majority of RF emissions in a shielded enclosure escape through the external I/O signals. Keeping clocks and other fast changing signals well clear of these traces and providing filtering on I/O traces will significantly reduce RF emissions.

6.3.16 Inter subsystem communication links

For communication between subsystems, redundant serial communications are recommended. A shared RS485 bus, as used with great success on SUNSAT, would be an ideal

choice. Ensure that there are at least two serial links between the satellite bus master to all slaves that form part of the core (satellite bus). To interface these buses to the CPU, the standard PC 16550 UARTs can should be used. These devices have on-board FIFOs which greatly improve the performance of the system under high interrupt loads.

One positive side-effect of using standard bus drivers is that problems with inter subsystem isolation is avoided. The problem found on **SUNSAT** where certain sub-systems were driving dead logic is thus eliminated. Ensure that any I/O driver of a cable is rated for the maximum cable length and drive requirements. Never assume that a cable driver IC will meet all aspects of a standardized I/O path. Always check the standard (e.g., EIA-485) and be sure the design fully complies.

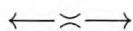
6.4 The Art Of Engineering

“There is no silver bullet”. This saying has lately seen considerable use and is the single most significant lesson the author has learned during his involvement with **SUNSAT**.

In the media, certain technologies are often touted as being the solution to all problems. Engineers are specifically the focus of these claims. Fortunately, engineers are trained to understand the reality of real-world design. In this reality, there are design parameters that are inherently conflicting. A technology or implementation that would optimize one parameter, would, by the laws of nature, cause other parameters to degrade.

Another aspect that engineers are well familiar with is the concept of “unknowns”. In many cases, and in particular in the domain of space exploration, there are many parameters that we are not yet aware of. In other cases, the interaction between parameters are not clearly understood.

To allow the development of new technologies / products, the engineer is equipped with a number of tools, in the generic sense, that allow him/her to design where uncertainty exists. Some of these tools include the abstract tools (knowledge of fundamentals, models, methodologies, *etc.*) and the physical tools (measurement tools, computers, prototypes, *etc.*). These in themselves, are still just tools and require an intelligence to orchestrate their activities.



Appendix A

Nomenclature

This chapter lists the abbreviations and acronyms found in this text and in literature that relates to the topics that will be discussed.

Acronym	Description
188EC	See 80C188
386EX	See 80386EX
387SX	See 80387SX
8252	Intel Standard UART
8031	Intel Micro-controller
8086	Standard 16-bit Intel Microprocessor (16-bit data bus)
8088	Standard 16-bit Intel Microprocessor (8-bit data bus)
80186	Embedded 16-bit Intel Microprocessor (16-bit data bus)
80C188	Embedded 16-bit Intel Microprocessor (8-bit data bus)
80386EX	Embedded 32-bit Intel Microprocessor
80387SX	Intel 386 compatible Maths co-processor
AC	Alternating Current or Advanced CMOS
ADC	Analog to Digital Converter
ADCS	Attitude Determination and Control System
AIAA	American Institute of Aeronautics and Astronautics
ASIC	Application Specific Integrated Circuit
AU	Astronomical Unit
bps	Bits per second
BGA	Ball Grid Array
BIST	Built-In Self-Test
BIU	Bus Interface Unit
C&DH	Command and Data Handling
CAD	Computer-Aided Design
CCD	Charge Coupled Device

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Acronym	Description
CLB	Configurable Logic Block
CMOS	Complementary Metal Oxide Semiconductor
CMOS/SOI	CMOS on insulator (<i>Si</i> on SiO_2)
CMOS/SOS	CMOS on sapphire (<i>Si</i> on Al_2O_3)
CPU	Central Processing Unit
CRC	Cyclic Redundancy Code
CSMA/CD	Carrier-Sense-Multiple-Access with Collision Detection
CTE	Coefficient of Thermal Expansion
dB	decibel
DC	Direct Current
DIP	Dual-Inline Package
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
DSP	Digital Signal Processor
EDAC	Error Detection And Correction
EEPROM	Electrically Erasable PROM
EM	Engineering Model
EMI	Electro-Magnetic Interference
EPROM	Erasable PROM
ESA	European Space Agency
ESD	Electrostatic Discharge
EUV	Extreme Ultraviolet
FET	Field Effect Transistor
FIFO	First-In First-Out
FLASH	Product class, non-volatile memory device
FM	Flight Model or Frequency Modulation
FMS	Flight Management System
FPGA	Field Programmable Gate Array
FPU	Floating Point Unit
FSK	Frequency Shift Keying
GCR	Galactic Cosmic Radiation
GEO	Geostationary/Geosynchronous Earth Orbit
GPS	Global Positioning System
HC	High Speed CMOS
HDL	Hardware Description Language
HDLC	High-level Data Link Control
HEO	High Elliptical Orbit
IC	Integrated Circuit
ICP	Interface Control Processor
IDEU	Instruction Decode and Execute Unit
IEEE	Institute of Electrical and Electronics Engineers
<i>continued on next page</i>	

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Acronym	Description
I/O	Input / Output
IMAGER	SUNSAT support electronics for CCD camera
IPU	Instruction Prefetch Unit
IRQ	Interrupt Request
ISAC	Intra-Satellite Asynchronous Channel
ISR	Interrupt Service Routine
JPL	Jet Propulsion Laboratory, NASA
LA	Link Adaptor
LBAND	2 – 30 Mb/s uplink of SUNSAT
LEO	Low Earth Orbit
LET	Linear Energy Transfer
Mb/s	Millions of Bits per second
MB/s	Millions of Bytes per second
MBE	Multi-bit Error
MEU	Multiple Event Upset
MODEM	Modulator / Demodulator
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSIS	Mass-Spectrometer-Incoherent-Scatter
MUX	Multiplexer
NASA	North American Space Administration
NMI	Non-Maskable Interrupt
NMOS	N-Channel MOS
NORAD	North American Aerospace Defense Command
NRZ	Non-Return-to-Zero signal encoding
NRZ-L	Non-Return-to-Zero Level signal encoding
NRZI	Non-Return-to-Zero-Invert-on-1s signal encoding
OBC	On-Board Computer
OBC1	First On-Board Computer of SUNSAT
OBC2	Second On-Board Computer of SUNSAT
ØRSTED	Danish Satellite launched with SUNSAT
PAL	Programmable Array Logic
PCB	Printed Circuit Board
PIC	Programmable Interrupt Controller
PLD	Programmable Logic Device
PLICE	Programmable Low-Impedance Circuit Element
PROM	(One-time) Programmable ROM
RAD	SI unit of radiation
RAM	Random Access Memory
RAMDISK	Mass storage device of SUNSAT
RF	Radio Frequency
<i>continued on next page</i>	

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Acronym	Description
ROM	Read-Only Memory
RS485	Industry Standard Differential Transmission protocol
RTC	Real Time Clock
SAA	South-Atlantic Anomaly
SBAND	65 Mb/s downlink of SUNSAT
SCC	Serial Communication Controller
SEB	Single Event Burn-out
SEDE	Single Event Disturb Error
SEDR	Single Event Dialectic Rupture
SEE	Single Event Effect
SEFI	Single Event Functional Interrupt
SEGR	Single Event Gate Rapture
SEIDC	Single Event Induced Dark Current
SEL	Single Event Latchup
SEMBE	Single Event Multi-Bit Error
SET	Single Event Transient
SEU	Single Event Upset
SHE	Single Hard Error
SMT	Surface Mount Technology
SOI	Silicon on insulator (<i>Si</i> on SiO_2)
SOS	Silicon on sapphire (<i>Si</i> on Al_2O_3)
SPE	Solar-Particle Event
SPICE	Simulation Program with IC Emphasis
SRAM	Static RAM
SSB	SUNSAT Serial Bus
SUNSAT	Stellenbosch University Satellite
T800	Inmos Transputer
T-STATE	Unit bus cycle period
TCMD	Tele-command
TLE	Transient Launch Environment
TLM	Telemetry
TID	Total Ionization Dose
TMR	Triple Modular Redundancy
TTL	Transistor-Transistor Logic
TTMS	Telecommand, telemetry and modem subsystem
UART	Universal Asynchronous Receiver Transmitter
USART	Universal Synchronous/Asynchronous Receiver Transmitter
USB	Universal Serial Bus
UV	UltraViolet
VCC	Digital Supply Voltage, normally 5V
VHDL	VHSIC Hardware Description Language
<i>continued on next page</i>	

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Acronym	Description
VHF	Very High Frequency
VHSIC	Very High Speed Integrated Circuit
WOD	Whole Orbit Data

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Appendix B

SUNSAT Technical Specification

B.1 FLIGHT MANAGEMENT SYSTEM - Initial Version

B.1.1 Purpose and composition

The flight management system (FMS) comprises the hardware and software needed to provide the computer control of the total spacecraft function. It shall:

- i). be able to control all the other subsystems on board to fulfill a successful mission.
- ii). be able to command power on/off to all subsystems for power management.
- iii). provide all computational capabilities to other subsystems except where a subsystem has local computational capability.
- iv). provide a mass storage for data processing and storage.
- v). provide a real time operating system to upload and enable events in the whole orbit for the next 100 orbits.

B.1.2 Performance required

B.1.2.1 Flight Management Software

The flight management software system shall:

- i). provide the basic operating system for all other applications using the OBC.
- ii). provide a real time diary for the scheduling of all applications running on the OBC.

- iii). provide for a mechanism to schedule and upload new tasks to the OBC while in flight.
- iv). provide reliable computing facilities for all applications running on OBC.

B.1.2.2 Flight Management Hardware

The system shall meet the following requirements:

- i). Power consumption of the subsystem must not exceed an average of 5 *W*.
- ii). Processors must be able to operate in four different modes:
 - Operational - draw full power and use maximum clock speed.
 - Operational degraded - use lower clock speed and therefore use less power.
 - Standby - processor stopped and power removed from it, but memory is in data retention mode.
 - Off - all power to processor and memory turned off.
- iii). All devices must be:
 - (a) CMOS for low power consumption and
 - (b) radiation tolerant.
- iv). Both processors must be able to reboot from the ground station.
- v). A real time clock must be supplied to both processors.
- vi). An A/D and D/A must be available to both CPU's sampling baseband audio signals.
- vii). The RAM DISC storage unit must be at least 32 Mbyte with provision for 64 Mbyte.

B.1.3 Subsystem definition - Software

The software components are:

- i). Communication harness.
- ii). On-Board Scheduler.
- iii). Offline Scheduler and resourch allocator.
- iv). Built in tests.
- v). Software loaders.

The communication harness must provide reliable communication for any of the application tasks to any of the subsystems on SUNSAT with communication capabilities.

The on-board scheduler is responsible for scheduling the tasks accepted and allocated by the offline scheduler according to their deadlines and power consumption. It must further provide a calendar for the running of tasks at least 100 orbits into the future.

The offline scheduler would typically run at the ground station to verify that the arriving tasks would actually be schedulable according to deadlines and power requirements.

The built in tests will provide for the self testing of the complete on board computer system and the baseband switch. It will provide basic telemetry output, but also detailed information with regard to the state of the onboard computers system on request.

The software loaders is responsible for keeping SUNSAT reprogrammable under all circumstances. It is here where the lifespan of SUNSAT could be extended and the quality of the services enhanced. It will be able to reload the whole of the SUNSAT software as well as the acceptance of tasks under normal operation.

B.1.4 Subsystem definition - Hardware

B.1.4.1 Possible Configurations

The computer system can be designed as either a two or a three board system.

i). System with two PC boards:

The primary and secondary functions processors can be placed on one PC board and the RAM DISC on a second. The 80C186 is suggested for the primary processor and the T800 (or T9000) for the secondary processor.

ii). System with three PC boards:

A third auxiliary PC board can be added to the above configuration containing non critical experimental computer circuitry *e.g.*, 80386 and T9000 processors, qualifying components, the best school experiment, a FPGA experiment to test its reliability in space, *etc.* Systems already designated for this board include a DSP modem and the communication switch area.

B.1.4.2 Primary Computer

Processor The primary processor is chosen to be a 80C186 for the following reasons:

- It has already been used successfully in space.
- Software is compatible with a large base of PC software.

Start up mechanism The primary processor should be able to start up in three modes *i.e.*

i). Cold start

Load the memory from the ground via the telecommand system and then start up the processor. A basic boot loader, residing in PROM, will be running on the processor to facilitate loading. The boot loader program will also include a built-in test routine and will test the integrity of the current application program when necessary.

ii). Warm start from non volatile memory

Part of the processor memory will be non volatile memory *i.e.* FLASH memory or continuously powered SRAM. This part of the memory will be used to store the current application program.

iii). Warm start from standby mode

After the primary computer system has been placed in low power standby mode, it can be restarted without reloading the memory.

Memory The main memory of the primary computer will consist of CMOS static RAM with EDAC. The size of the memory is recommended to be either 512k or 1 Mbyte. As this computer will have to run most of the time, the smaller memory is advisable to lower the power consumption.

For improved fault tolerance against permanent IC failure, the memory should be organized into two rows of 256k-byte each and 16 (+ 6 for EDAC) vertical columns. The necessary isolation should be provided so that each row can be totally isolated from the address and data bus, its power turned off and the remaining row remapped if necessary. A subdivision of the memory into two rows should be close to optimum if the trade off between reliability, circuit complexity and circuit board space is taken into account.

Memory chips, presently available, contains up to 4 Mbits per chip so that the above memory sizes can be implemented with 22 chips per row. One bit chips with EDAC enables one permanent device failure to be masked out.

B.1.4.3 Secondary Computer

Processor The secondary processor is provisionally chosen to be a T800 transputer for the following reasons:

i). It has already been used successfully in space.

ii). It provides for high speed (10 MIPS and 1,5 MFLOPS) processing power necessary for some of the processing envisaged.

Consideration to the new generation T9000 transputer will be given when more information about it becomes available towards the end of the year.

Start up mechanism (as for 80C186) The secondary processor should be able to start up from two sources *i.e.*

- Cold start

The built in boot-from-link mechanism of the transputer must be exploited for this purpose.

- Warm start from standby mode

The secondary processor must only be turned on when high speed computation is needed in order to conserve power (the T800 consumes 1 W). There for four modes of operation can be provided *i.e.*

- i). Power off.
- ii). Low speed operation with lowered clock frequency.
- iii). Full speed operation.
- iv). Standby mode with the processor power turn off, but the memory placed in data retention mode. After the secondary computer system has been placed in low power standby mode, it can be restarted without reloading the memory.

Memory The main memory of the secondary computer must be provided with EDAC. Furthermore it must be organized having only one bit of the word in one physical integrated circuit (IC) to make it more resistant to single transient errors.

To maintain functionality in the case of permanent faults, the two row scheme proposed for the 80C186 will be implemented as well.

The size of the memory can be either 2 or 8 Mbyte. RAM chips, presently available, contains up to 4 Mbits per chip so that the above memory sizes can be implemented with 39 chips of either 256k x 1 or 512k x 1 bits including 7 EDAC bits.

B.1.4.4 Intermodule Communication

Communication amongst the different subsystem modules, excluding the single line telecommand and telemetry signals, falls into four categories.

- i). Low speed general purpose.
- ii). Low speed dedicated.
- iii). High speed point to point parallel bus.
- iv). High speed point to point serial.

It is suggested that the following communication mechanisms provide for the above needs:

- i). To cater for the setting up of fault tolerant circuit switched communication channels, the interconnection of subsystems can be modeled as a cross bar switch. This can either be implemented with multiplexers, actual switches, hard wired connections or in a cross bar switch. See communication block diagram.
- ii). The low speed dedicated connections *e.g.*, from the Attitude control subsystem to the primary computer can be implemented with bidirectional serial interfaces (UART).
- iii). High speed parallel coupling *e.g.*, between the CCD sensors and the RAM DISC, can be provided by three 8-bit parallel connections. In order to maximize EMC the CCD tray and the computer tray must be adjacent.
- iv). High speed serial coupling is necessary *e.g.*, between the RAM DISC and the high speed down link. This can be implemented with a serial differential line using a special purpose synchronous protocol.

B.1.4.5 Processors in other subsystems

It is recommended that the program memory of any of the other subsystems should also be reloadable from the ground. A basic reloadable module will be designed which can be applied in any module needing a reloadable processor.

B.1.4.6 RAM DISC

Access to the RAM DISC must be provided for both the primary and the secondary computers, the CCD sensors and the fast serial link to the transmitters. Taking into account the size of this memory and the accompanied logic, it will have to be housed on a second PC board in the computer tray.

Static CMOS RAM chips of 4 Mbit is presently available (*e.g.*, Hitachi, Cypres). It is suggested that chips with a 512k x 8 organization are used with software based EDAC. The three CCD sensors will each have an 8-bit data path to an 8 bit wide column of the memory. A fourth column can be added for compatibility with the 16 and 32 bit busses of the processors giving a total data path width of 32 bits. This fourth column can also be useful for storing *e.g.*, position information from the CCD camera.

As power consumption of this memory is high, provision has to be made to subdivide it into different horizontal blocks so that only that block which is being accessed is turned on - the rest being in either standby or retention mode.

It will be attempted to provide 64 Mbyte of memory. If 512k x 8 chips are used, 32 horizontal blocks can be provided. Therefore only one of these 32 blocks, *i.e.* four chips, have to be turned on at any particular time.

The typical power consumption for Hitachi components are as follows:

- Selected mode with a data rate of 1.3 MHz uses 200 mW per chip *i.e.* 800 mW for one 4 chip row.

- Deselected mode consumes typically $10 \mu W$ ($500 \mu W$ maximum) *i.e.* $40 \mu W$ typical for a 4 chip row.
- Data retention mode (with 3 V supply voltage) consumes typically $5 \mu W$ ($250 \mu W$ maximum) *i.e.* $20 \mu W$ typical for a 4 chip row.

From these figures it is concluded that it is not necessary to implement the data retention mode as little is gained relative to the deselected mode. The total power consumption of the memory (excluding buffers and decoding logic) is thus a maximum of $830 mW$ which is considered a reasonable fraction of the total allowed consumption of $5 W$

In order to increase the tolerance for permanent failure of the chips, the horizontal blocks can be isolated with tristate buffers and separate power lines can be provided to each block so that any block can be totally removed from the system. The selection line of each row can then be reprogrammed as to effectively move the disabled memory to the edge of the image being recorded. This can simply be implemented with a dynamic reconfigurable mapping mechanism.

B.2 FLIGHT MANAGEMENT SYSTEM - Last Version

B.2.1 Purpose and composition

The flight management system (FMS) comprises the hardware and software needed to provide the computer control of the total spacecraft function. It shall:

- i). be able to control all the other subsystems on board to fulfill a successful mission.
- ii). be able to command power on/off to all subsystems for power management.
- iii). provide all computational capabilities to other subsystems except where a subsystem has local computational capability.
- iv). provide a mass storage for data processing and storage.
- v). provide a real time operating system to upload and enable events in the whole orbit for the next 100 orbits.

B.2.2 Performance required

B.2.2.1 Flight Management Software

The flight management software system shall:

- i). provide the basic operating system for all other applications using the OBC.
- ii). provide a real time diary for the scheduling of all applications running on the OBC.
- iii). provide for a mechanism to schedule and upload new tasks to the OBC while in flight.
- iv). provide reliable computing facilities for all applications running on OBC.

B.2.2.2 Flight Management Hardware

The system shall meet the following requirements:

- i). Power consumption of the subsystem must not exceed an average of 5 *W*.
- ii). Processors must be able to operate in four different modes:
 - Operational - draw full power and use maximum clock speed.
 - Operational degraded - use lower clock speed and therefore use less power.
 - Standby - stop the clock to the processor (internally under software control) and therefore have only leakage currents flowing to the processor.
 - Off - all power to processor and memory turned off.
- iii). All devices must be:
 - (a) CMOS for low power consumption and
 - (b) radiation tolerant.
- iv). Both processors must be able to reboot from the ground station.
- v). A real time clock must be supplied to both processors.
- vi). An A/D and D/A must be available to both CPU's sampling baseband audio signals.
- vii). The RAM DISC storage unit must be able to handle 8, 16, 32 or 64Mbyte.

B.2.3 Subsystem definition - Software

The software components are:

- i). Communication harness.
- ii). On-Board Scheduler.
- iii). Offline Scheduler and resourch allocator.
- iv). Built in tests.

- v). Software loaders.

The communication harness must provide reliable communication for any of the application tasks to any of the subsystems on **SUNSAT** with communication capabilities.

The on-board scheduler is responsible for scheduling the tasks accepted and allocated by the offline scheduler according to their deadlines and power consumption. It must further provide a calendar for the running of tasks at least 100 orbits into the future.

The offline scheduler would typically run at the ground station to verify that the arriving tasks would actually be schedulable according to deadlines and power requirements.

The built in tests will provide for the self testing of the complete on-board computer system and the baseband switch. It will provide basic telemetry output, but also detailed information with regard to the state of the on-board computers system on request.

The software loaders is responsible for keeping **SUNSAT** reprogrammable under all circumstances. It is here where the lifespan of **SUNSAT** could be extended and the quality of the services enhanced. It will be able to reload the whole of the **SUNSAT** software as well as the acceptance of tasks under normal operation.

B.2.4 Subsystem definition - Hardware

B.2.4.1 Possible Configurations

The computer system can be designed as either a two or a three board system.

- i). System with two PC boards:

The primary and secondary functions processors can be placed on two PC boards and the RAM DISC on a separate tray. The 80C188EC is suggested for the primary processor and a 386 + 387 for the secondary processor.

- ii). System with three PC boards:

A third auxiliary PC board can be added to the above configuration containing non critical experimental computer circuitry *e.g.*, 80386 and T9000 processors, qualifying components, the best school experiment, a FPGA experiment to test its reliability in space, *etc.* Systems already designated for this board include a DSP modem and the communication switch area.

B.2.4.2 Primary Computer

Processor The primary processor is chosen to be a 80C188EC for the following reasons:

- It has already been used successfully in space.
- Software is compatible with a large base of PC software.

Start up mechanism The primary processor should be able to start up in three modes *i.e.*

- Cold start

The processor will initially boot from a fusible-link PROM whereafter the system will be booted from FLASHRAM, EPROM, RAMDisk or the ground.

- Warm start from standby mode

The four modes of operation the primary computer can provide is :

- i). Power off.
- ii). Low speed operation at clock frequencies of a $\frac{1}{4}$, $\frac{1}{8}$, $\frac{1}{16}$, $\frac{1}{32}$ and $\frac{1}{64}$.
- iii). Full speed operation at 16 *MHz*
- iv). Standby mode with the clock stopped and the SRAM powered. After the secondary computer system has been placed in standby mode, operation can be resumed without reloading the memory.

Memory The main memory of the primary computer will consist of CMOS static RAM with EDAC. The size of the memory is recommended to be either 512k or 1 Mbyte. As this computer will have to run most of the time, the smaller memory is advisable to lower the power consumption.

For improved fault tolerance against permanent IC failure, the memory should be organized into two blocks, each containing two 512k-byte SRAM chips. One is used for the storage of the 8-bit data and the other one is used for the storage of the EDAC data. The necessary isolation should be provided so that each block can be totally isolated from the address and data bus, its power turned off and the remaining row remapped if necessary. A subdivision of the memory into two blocks should be close to optimum if the trade off between reliability, circuit complexity and circuit board space is taken into account.

Memory chips, presently available, contains up to 4 Mbits per chip so that the above memory sizes can be implemented with 4 chips for the two blocks. The EDAC will be used to correct one bit faults, while detecting two bit faults.

B.2.4.3 Secondary Computer

Processor The secondary processor is chosen to be a 386 + 387 processor for the following reasons:

- i). It consumes very low power.
- ii). It provides for high speed processing power necessary for some of the processing envisaged.

Start up mechanism (as for 80C188EC) The secondary processor should be able to start up from two sources *i.e.*

- Cold start

The processor will initially boot from ROM whereafter FLASH memory or the EPROM will be used for the bulk of start-up information.

- Warm start from standby mode

The secondary processor must only be turned on when high speed computation is needed in order to conserve power (typically the 386 consumes 1 W). There for four modes of operation can be provided *i.e.*

- i). Power off.
- ii). Low speed operation at clock frequencies of a $\frac{1}{2}$, $\frac{1}{4}$ and $\frac{1}{8}$.
- iii). Full speed operation at 20 MHz
- iv). Standby mode with the clock stopped and the SRAM powered. After the secondary computer system has been placed in standby mode, operation can be resumed without reloading the memory.

Memory The main memory of the secondary computer must be provided with EDAC. To maintain functionality in the case of permanent faults, the two row scheme proposed for the 80C188 will be implemented as well.

The size of the memory will be 4Mbyte. RAM chips, presently available, contains up to 4 Mbits per chip so that the above memory sizes can be implemented with 16 chips of 512k x 8 bits including 10 EDAC bits.

B.2.4.4 Intermodule Communication

Communication amongst the different subsystem modules, excluding the single line telecommand and telemetry signals, falls into four categories.

- i). Low speed general purpose.
- ii). Low speed dedicated.
- iii). High speed point to point parallel bus.
- iv). High speed point to point serial.

It is suggested that the following communication mechanisms provide for the above needs:

- i). The low speed general purpose communications bus between the two OBCs, the telemetry system and the telecommand system is called the **SUNSAT** Serial Bus (SSB). The protocol used, the systems connected to it, how these systems are connected to it and whether these systems read or write to the bus will be described below.

The telecommand system will not transmit on the SSB. It only listens for valid telecommand commands from the OBCs. The telemetry system can transmit and receive on the SSB and is used as a back-up for data transfers between the OBCs and the telemetry system when the parallel ports are not operational. The OBCs can transmit and receive on the SSB, sending data between the two OBCs, sending/receiving telemetry information to/from the telemetry system or issuing commands to the telecommand system (A back-up when the parallel telecommand port is not operational.).

Data can only be sent/received to/from the telemetry and the telecommand systems when the Processor on the particular subsystem's board is functional.

It is possible to have 3 masters on the bus *i.e.* the telemetry system and the 2 OBCs. The protocol used on the SSB must therefore accommodate multiple masters and slaves on a single bus. This situation will not arise very often, because the telemetry system will only send data on the SSB when the parallel port to one of the OBCs is not functional. Under normal situations, only one OBC will be switched on at a time.

Protocol used on the SSB :-

The protocol which will be used to send an address, data or parity byte is as follows :

1 START-bit (0),

8 DATA-bits,

a programmable 9th bit and

1 STOP-bit (1) bit. (Mode 2 & 3 on the 80C188EC, telecommand's 8031 and telemetry's 8031.)

Modes 2 & 3 are used for multi-processor communication on a single serial bus. When the master processor wants to transmit data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is a 1 in an address byte and a 0 in a data byte. Data bytes will not interrupt a slave. An address byte, however, will interrupt all the slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will then prepare to receive the data which will be coming.

The above mentioned protocol assumes that there is only one master on the SSB. To accommodate more than one master, bus collision detection must be added to the protocol. This is done by listening to the data you have send and when it is different, re-send the data/information after a random time. The hardware used for the SSB must also accommodate multiple bus drivers.

When there is no activity on the bus, the logical level is high. Each system writing to the bus must have a pull-up resistor. All the systems must use open-collector drivers to drive the bus. This is to avoid destroying the bus drivers and buffers when more than one system transmits data simultaneously. When this open-collector driver is used to drive the SSB, the logical level of the transmitted signal is inverted. An inverter must therefore be inserted before the open-collector transistor to correct the logical level. A systems whose power can be switched on and off e.g. the Processors, must AND the signal received from the SSB with the logical level of the power supply of that system. This must be done to prevent the destruction of the device receiving the data on that system. The device will be destroyed, because the input voltage to the device will be higher than the supply voltage. The AND-gate must be built with discrete components and must be powered from the telemetry's power supply, which is never switched off.

The baudrate which is going to be used on the SSB is 9600 baud.

The protocol used is expanded further by sending the data in packets. These packets must contain the following bytes :

- 1) Destination Address,
- 2) Source Address,
- 3) Packet Length,
- 4) Data (Length equal to the packet length specified.)
- 5) Parity byte and
- 6) Source Address.

The address byte's 9-th bit must be a '1' and that of the data and parity byte a '0', as was mentioned earlier. When data is transmitted, the parity is calculated by XOR-ing all the data bytes transmitted with each other. This calculated parity byte is then send after all the data bytes is send. In the slave or receiver, all the received data bytes are XOR-ed. The result is then XOR-ed with the parity bit received from the master or transmitter. When the value is '0', the data received is valid, but if it is not, the slave must request the master to re-send the data.

The addresses for the different subsystems are as follow:

- 1) Telecommand 1 - 0011 1100 - 3Ch
 - 2) Telecommand 2 - 0111 1111 - 7Fh
 - 3) OBC1 - 0001 1111 - 1Fh
 - 4) OBC2 - 0000 0111 - 07h
 - 5) Telemetry - 0000 0001 - 01h
- ii). The low speed dedicated connections e.g., from the Attitude control subsystem to the primary computer can be implemented with bidirectional serial interfaces (UART).

- iii). High speed parallel coupling *e.g.*, between the CCD sensors and the RAMDisk, can be provided by three 8-bit parallel connections. In order to maximize EMC the CCD tray and the computer tray must be adjacent.
- iv). High speed serial coupling is necessary *e.g.*, between the RAMDisk and the high speed down link. This can be implemented with a serial differential line using a special purpose synchronous protocol.

B.2.4.5 Processors in other subsystems

It is recommended that the program memory of any of the other subsystems should also be reloadable from the ground. A basic reloadable module will be designed which can be applied in any module needing a reloadable processor.

B.2.4.6 RAM DISC

Access to the RAM disc must be provided for both the primary and the secondary computers, the CCD sensors and the fast serial link to the transmitter and receiver. Taking into account the size of this memory and the accompanied logic, it will have to be housed in a separate tray. The imager will be housed on this board too.

More detail about the RAMdisk can be found in the RAMdisk section.

B.3 Computer Tray Specification - Final Version

The computer assembly consists of two trays *i.e.* the primary computer and secondary computer tray.

B.3.1 Scope

This specification gives characteristics and performance requirements that, unless otherwise specified, shall be met under all laboratory integration and space environmental conditions until ten years after launch.

B.3.2 Location and purpose

B.3.2.1 Microcomputer tray

This tray will contain the primary and secondary computers.

The primary computer will use a 80C188EC processor and will be responsible for the normal operation of the satellite. This includes the packet radio service and other control functions including coarse and fine orientation control.

The secondary computer will use a 386 + 387 processor and will provide a backup for the primary onboard computer and the T800 (in control of the reaction wheels), and serve as a platform for various experiments.

B.3.3 Functional description

Note : The description in this section is based on the existing flight computer design. It shall be considered a binding requirement.

B.3.3.1 Microcomputer tray

The primary and secondary computers are situated on this tray.

Primary computer

The processor used shall be the INTEL 80C188EC processor. This processor will be clocked by a 32 *MHz* crystal. The internal clock frequency is 16 *MHz*. This frequency can be divided down internally under software control to save power.

This processor shall include a built-in watchdog to reset the computer if it halts for some unforeseen reason. Provision is also made so to reset the processor manually for testing purposes, on power-up, by telecommand and by a memory error.

The 8 interrupt inputs on the processor are used to monitor important events in the computer system and then to service the appropriate software subroutines when one or more of these events occur. One of the interrupt inputs are connected to a slave Programmable Interrupt Controller (PIC), expanding the number of interrupts to the processor.

One of the two serial ports on the processor is connected to 8031 on the ADCS board and the other is used as the SUNSAT Serial Bus. The primary and secondary computers as well as the Telemetry subsystem is connected to this bus.

The processor has a built-in Chip Select Unit (CSU) which is used to map the available memory. To increase the total number of Chip Select outputs, two of the CSU outputs are used together with the address line to create 16 more Chip Select outputs.

The microprocessor's internal DMA controller can also be used to sample and store data from the AD-Converter (Parrot radio) or writing data to the DA-Converter (Parrot radio). The DMA controller can also be used to read the 2 asynchronous serial ports on the microprocessor.

Discrete logic is used to generate memory and I/O read and write signals.

The Data/Address- and Status bus is latched and the Data bus is buffered.

A real time clock is used by the primary computer to keep track of the time of day. The

accuracy which can be achieved with this real time clock chip is 100ths of a second.

This is necessary, because time is very critical when a photograph of certain part of earth must be taken. This chip is powered directly from the power supply and can therefore not be switched on or off like some of the components the board. This real time clock chip also has its own crystal clock.

The processor can be booted from a 2kB fusable link PROM, 64kB EPROM, the 256kB FLASHRAM or the RAMDisk. The source from which the processor computer must be booted, is selected by telecommand. Code in the PROM consist of a very simple bootstrap loader. This code can also reload the FLASHRAM with new program code.

The static memory of the computer is divided into two blocks of 512kB SRAM. The power to each of these blocks can be switched on and off by the processor. A block can be switched off when it starts to use too much power or when the data cannot be stored in a block safely without errors.

Each of these blocks has an additional 512kB of memory in which the EDAC correction data is stored. All the control, data and address lines to the two SRAM chips in each of the SRAM blocks is isolated by tri-state buffers.

The number of errors detected by the EDAC is counted and can be used to determine if a memory block cannot be used to save data safely.

The computer can control the switches which supplies the supply voltage to the two SRAM blocks, as well as the supply voltage to FLASHRAM, including the programming voltage. The telecommand controls the switches for the power to the whole computer tray.

The A/D-converter is used to continuously monitor the most important currents. This is done by converting the currents to voltages so that it can be read by the A/D-converter. This converter is also used to monitor the 2 audio channles (Parrot radio).

The inputs monitored by the A/D-converter are as follows :

- i). total current drawn by the primary computer,
- ii). current drawn by each of the two blocks of SRAM,
- iii). current drawn by the FLASHRAM,
- iv). current drawn when the FLASHRAM is programmed,
- v). current drawn by the RAMDisk (x10, for each block, the PAL and logic),
- vi). current drawn by the DSP processor and
- vii). audio signal from the 2 audio busses (Used for the parrot radio).

The D/A-converter is used to convert the stored digitized speech to analog signals so that it can be sent via the modems back to earth. This is used for the parrot radio.

Three UARTS are used, providing 6 channels. The 7 1200 baud receiver modems and 2 9600 baud receive modems are multiplexed and fed to the UARTS. This is done for redundancy. The transmit channels to the 2 9600 baud modems and the 4 1200 baud modems are also multiplexed for redundancy.

All signals on I/O ports which goes via connectors to other trays, are buffered.

These ports include the ports to the DSP-processor, modems, secondary computer, telecommand, telecommand monitoring, telemetry, communications switches, attitude control and mass memory.

Secondary computer

The secondary processor will use a 16/32 bit INTEL 80386SL 20 *MHz* microprocessor.

Two blocks of memory will provide a total of 4 M-byte of SRAM to the transputer. Each block of 2 M-Byte can be isolated from the processor in the case of permanent failure.

The external memory will be protected against single bit errors by an IDT49C460 Error Detection And Correction (EDAC) circuit. Double bit errors will also be detectable. Special provision has to be made in the design for the following possibilities:

- i). 32 bit write,
- ii). 32 bit read,
- iii). 8 or 16 bit write,
- iv). EDAC disabled.

In order to provide for the above, two programmable devices will be used as an implementation with discrete logic will need too many components. The risk of using these in space is justified because of the secondary nature of the OBC2 system.

The 386 microprocessor will also have access to the following peripherals:

- i). real time clock,
- ii). two UART's,
- iii). parallel port to RAMDisk,
- iv). parallel port to Attitude Control Tray.

An EPROM will contain a default boot program through which it will be possible to start the processor and load more software.

Provision will also be made to halt the clock of the 386 processor while still retaining the information in the memory in low power standby mode. The microprocessor must then be able to resume its duties at a later stage without reloading the memory.

The 386 can control the switches which provide the two SRAM blocks with power. The telecommand controls the switches for the power to the whole computer tray.

An A/D-converter is used to continuously monitor the most important currents. This is done by converting the currents to voltages so that it can be read by the A/D-converter. The converter is also used to monitor the 2 audio channels (Parrot radio).

The inputs monitored by the A/D-converter are as follows :

- i). total current drawn by the secondary computer,
- ii). current drawn by each of the two blocks of SRAM,
- iii). current drawn by the RAMDisk.

B.3.4 Characteristics

B.3.4.1 Microcomputer tray

The items contained in the tray shall meet their individual specifications when integrated together.

B.3.5 Performance

B.3.5.1 Microcomputer tray

Processor The primary processor shall be a 80C188EC from INTEL. This processor will run at a clock frequency of 16 *MHz*. To save power, this clock frequency can be divided down to lower frequencies.

Power consumption The primary computer will use less than 2.5 *W* of power. The secondary computer will use another 2.0 *W* at peaklevel, but will only be switched on on demand.

B.3.6 Electrical interfaces

B.3.6.1 Microcomputer tray

The microcomputer tray is connected to the rest of the system via 10 connectors. All these connectors consists of a plug and a socket which must be screwed together. The socket will be on the microcomputer tray.

With the connectors, connections are made to the ADCS board, RAMDisk, Telecommand, telemetry, modems and the power supply unit. The primary computer tray has a con-

nection with the secondary computer which connects the secondary computer to the DSP subcircuit.

B.3.7 Mechanical parameters and interfaces

B.3.7.1 Microcomputer tray

Mass Total mass shall be between ? and ? kg.

Volume restriction This tray shall fit into the following dimensions : $177\text{ mm} \times 257\text{ mm} \times 15\text{ mm}$.

B.3.8 Reliability

The unit shall only use parts from the SUNSAT Approved Parts List, or for which approval has been given by the QA officer.

Parts selected shall include consideration of the vacuum, radiation, and temperature cycling environment the unit shall be subjected to.

Worst case design calculations include allowance for component tolerance and drift shall be presented.

Acceptance tests shall be defined to verify that no detectable malfunctions are present in the unit.

Development, assembly and test of the unit shall comply with the general QA guidelines in the technical specification.

B.3.9 Maintainability

The design of the unit shall make allowance for extensive integration tests.

The unit shall be designed to ensure that no damage occurs if the power supply line is shorted or if a reverse polarity supply of between 0 and 25 volts is connected.

B.3.10 Environmental specifications

B.3.10.1 Temperature

Operating temperature : $-30\text{ }^{\circ}\text{C}$ to $+55\text{ }^{\circ}\text{C}$

Storage temperature : $-35\text{ }^{\circ}\text{C}$ to $+55\text{ }^{\circ}\text{C}$

B.3.10.2 Vibration

The unit shall pass vibration tests specified.

B.3.11 Transportability and storage

Not applicable.

B.3.12 Design and construction standards

Design and construction shall be according to accepted good practices.

Sufficient internal test point shall be provided to enable correct operation of important subsections of the unit to be monitored.

B.3.13 Materials, processes, parts, surface finishes

All materials selected shall be suitable for space use.

Conformal surface coatings on PCB's is required.

B.3.14 Electromagnetic compatibility

The unit must operate in conjunction with transmitters and receivers operating at thermal noise limits, and must comply with the following requirements.

Emitted and conducted interference

- i). The fields radiated from the unit shall not cause a signal of more than -140 *dBm* measured in any 1 *MHz* bandwidth by a dipole antenna at a half wavelength from the unit.
- ii). The unit shall not inject a current of more than 1 *mA* RMS AC into the supply at any frequency above 100 *kHz*.

Susceptibility : The unit shall meet all performance requirements while subjected to :-

- i). A RF field strength of 10 *W* at 0.5 *m* at any frequency from 25 *MHz* to 2.5 *GHz*.
- ii). 0.5 *V* RMS at any frequency from 25 *MHz* to 2.5 *GHz* applied between earth and any electrical line.

B.3.15 Name plates and markings

All non-flight models shall be so marked.

B.3.16 Workmanship

This will be to accepted professional standards.

B.3.17 Interchangeability

Units will be interchangeable without adjustment to other connected units or re-alignment.

B.3.18 Safety

No unsafe materials or voltages shall be used.

B.3.19 Human performance and engineering

Not applicable.

B.3.20 Acceptance tests

A full set of acceptance tests shall be defined and executed. The acceptance criteria shall be so selected that an unit passing the test will meet performance requirements at temperature and life extremes.

B.3.21 Qualification

A qualification test programme shall be defined that over stresses the qualification model to sufficient an extreme to explore potential design weaknesses, and assure adequate design margins exist. The tests shall if necessary, monitor internal test points.

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Glossary

A

annealing: The process of partial or total self-healing of materials after irradiation and entails the recombination of ions particles or the recombination of vacancy-interstitial atoms. The process typically implies a complete or partial restoration of the electrical/material characteristics to pre-radiation state. Temperature changes can cause annealing in addition to the natural self-healing due to the passage of time. In some cases, annealing can leave the device in a state that is less desirable than the pre-radiation state. 16

Application Specific Integrated Circuit (ASIC): An integrated circuit that is designed according to the needs of a particular system. Since most space systems are produced in low volume, their ASICs are also necessarily fabricated in low volume. 64

B

bremsstrahlung: X-ray radiation (consisting of high energy photons) produced by the rapid deceleration of moving charge (typically fast moving electrons striking a metal). 17

burnout: A catastrophic failure of a (high power) transistor caused by transient radiation. Typically causes a permanent low resistance path between the gate and the substrate of a transistor. In the space environment a single ion can induce a degenerative feedback current in the transistor that will lead to its failure due to excessive current. 27

C

Complementary Metal-Oxide Semiconductor (CMOS): CMOS is a logic design style using combinations of PMOS and NMOS transistors. Under DC or low frequency conditions, this logic design style allows steady state current to dissipate only through leakage. Relatively large power is dissipated only during transistor switching at mid-to high-frequencies when there are brief periods where both types of devices are on simultaneously. 24

Compton effect: The Compton effect is a collision between an incident photon and an electron which is free or relatively weakly bound to an atom. In the Compton effect, only part of the photon energy is transferred to the electron, which even if weakly bound can be propelled out of the atom, thus ionizing it. The scattered photon (from

the collision) careens in a new direction, with much lower energy level and longer wavelength. 17

Computer-Aided Design (CAD): Any of a number of computer-based tools which assist a designer. CAD tools are vital for a number of phases in designing integrated circuits because they greatly facilitate entering, verifying, tracking, and storing massive amounts of complex information required. 64

CSMA/CD: A method used to control access to a shared transmission medium to which a number of stations are connected. A station wishing to transmit a message first senses (listens to) the medium and transmits the message only if the medium is inactive. Then, as the message is being transmitted, the station monitors the actual signal on the transmission line. If this is different from the signal that is being transmitted, a collision is said to have occurred and been detected. The station then ceases transmission and tries again later. 60

D

design verification: A variety of computer simulation procedures used to determine whether a design conforms to its specification. These tools verify the function, performance, testability, radiation hardness, and other specified aspects of a design. 64

displacement damage: The damage that occurs to a material, which has a well-ordered crystalline lattice structure, that is disturbed by radiation displacing some of the lattice elements. 19

dose: The energy absorbed per unit mass from any radiation in any material. This indicates the amount of energy transferred to the material through which the radiation is passing. The most common unit is the *rad*, which is the deposition of 100 ergs per gram of material. The SI unit, however, is the Gray (Gy), which is 1 J/kg or 100 rad. 16

F

fluence: The number of particles passing through a given area. The fluence is the time integrated flux. Typical unit is cm^{-2} . 16

flux: The number of particles passing through a given area per unit time. Typical units are $cm^{-2}.sec^{-1}$. 16

G

gate: The semiconductor region in a MOS transistor, located between its source and drain regions and having the opposite doping polarity to them. The gate forms a conducting path from source to drain when exposed to an electrical field of sufficient magnitude. 23

gate oxide: The thin layer of dielectric between n- and p-type materials in a CMOS transistor. In many CMOS processes capable of building 1 micron channel-length transistors, this oxide thickness is on the order of one hundred angstroms. 23

gate rupture: see *burnout*

27

H

Hardware Description Language (HDL): A CAD tool used for description and simulation of system and part microelectronics hardware at three major levels of abstraction: behavioral or algorithmic, register transfer level (RTL), and gate. ASIC HDL models at the RTL level are frequently automatically compiled into ASIC vendor's cell libraries to avoid manual gate-level design time and improve accuracy relative to high-level system modeling. 64

high-level design: The process of determining and documenting overall system structure including the division of large systems into smaller subsystem. 64

hot carrier: A charge-carrying particle with sufficient energy to pass over a diode barrier. In CMOS transistors, these particles are electrons (hot electrons) that cross over the semiconductor-metal junction. Repeated occurrences of this phenomenon can lead to device failure. Hot carriers are used in EPROM devices to store information by trapping them in the floating gate of the EPROM cells. 35

L

latchup: A parasitic effect on CMOS devices where sufficient current is injected into a substrate to cause the occurrence of a pnpn or npnp silicon-controlled rectifier (SCR)-type structure. When this structure forms a low-impedance path from power to ground, the resulting high current flow can stop a device from functioning and may permanently damage or destroy it. Latchup may be induced through a number of ways including unusually high supply voltages and currents induced by passing high-energy charged particles (galactic cosmic rays, *etc.*) through a circuit substrate. 26

leakage current: All undesirable stray current in a microcircuit. 25

logic gate: Physically, a logic gate is a transistor circuit which allows voltages to pass through based on simple logic rules applied to its inputs. These structures include logic functions such as NAND, NOR, AND, OR, XOR, XNOR, NOT, *etc.* In CAD simulation, a logic gate may be represented by its Boolean equivalent or by more complex representations which include delay and other parametric information. 64

lot: The quantity of microelectronic devices built at the same time. It is typical for an ASIC lot to consist of all parts built from a certain set of wafers. Typical wafer sets range in size from five wafers to twenty five wafers and are physically moved through the vendor's fabrication facility at the same time. 31

low-level design: The process of determining and documenting the detailed system design which acts as bridge from the high-level design to the implementation. 64

M

memory refresh: The cells of dynamic memory consist of small capacitors. Information is stored in the dynamic memory as the presence or absence of charge. These cells

slow discharge due to leakage effects and must be recharged continually to prevent information loss. 33

O

oxide layer: A layer of an integrated circuit created to provide isolation between conductive layers. See also gate oxide. 23

P

pair production: Pair production occurs when a very high energy photon approaches an atom sufficiently closely. The photon can then be spontaneously annihilated. In its place appears a fast moving electron and a fast moving positron. 17

photoelectric effect: The photoelectric effect occurs when a photon of low energy (a few *KeV*) penetrates the innermost electron shell structure of an atom and gives up all its momentum and energy, thereby being annihilated. The energy so released excites the atom, causing it to eject one of its innermost shell electrons. The atom is thus ionized in the process. The ejected electron therefore carries off the energy of the annihilated photon as kinetic energy. Another electron in the atom now de-excites the atom by dropping into the energy vacancy in the electron shell previously occupied by the expelled electron. The energy difference (of this electron) between its original state and new state is expelled from the atom as a newly formed photon. This photon has much less energy than the initial one. 17

positron: A positron (e^+) is the anti-matter equivalent of the electron in that it has the same mass, but has a positive charge. 17

R

rad-hard: Terminology that indicates the electronic component design was modified to ensure radiation reliability and survivalability. 44

rad-tolerant: Terminology that indicates the electronic component design was not modified, but the component inherently has a significant level of tolerance to radiation in its design. 44

radiation hardness: The ability of an integrated circuit to retain function and performance after being exposed to a specified amount of radiation. A circuit that does retain specified function and performance is often called rad hard. 41

S

Silicon-On-Insulator (SOI): Microelectronics process technologies used for radiation-hardened applications. Two types of SOI technology are Silicon on Sapphire (SOS) and Separation by IMplanted OXYgen (SIMOX). 42

Silicon-On-Sapphire (SOS): See silicon-on-insulator. 42

- simulator:** A computer-based system used for designing and testing one or more aspects of a model, be it a model of hardware or software. 64
- Single Event Burnout (SEB):** see *burnout* 27
- Single Event Effects (SEE):** Undesirable effects on an integrated circuit caused by energy transferred to its active area by the passage of a charged particle through it. 26
- Single Event Latchup (SEL):** A type of single event effect due to radiation. See *latchup*. 26
- Single Event Upset (SEU):** A type of single event effect (SEE) that causes a temporary change in the logical state of a transistor input or output node. SEUs are most hazardous when they change the state of a structure, such as a register or a memory cell, causing an incorrect value to be stored. 26

T

- temperature or thermal cycling:** A test that involves exposing parts to alternate extremes of high and low temperature. This is done to detect and discard parts that would otherwise fail from temperature changes experienced during their target applications. 11
- top-down design methodology:** A method of controlling the complexity of design development. Top down design begins with the most abstract description of a system, and breaks this into sub-descriptions. 64
- total ionizing dose (TID):** The accumulated amount of ionizing radiation a microelectronics device receives. 28
- trapped charges:** Charges (carriers) that exist in the dielectric portions (insulation layers) of semiconductor devices can remain trapped for extended periods. They are trapped due to the low carrier mobilities in the insulator material. These charges and their neutralizing counterparts that manifest on nearby conductors result in the generation of an electric field. 17

V

- very high speed integrated circuit (VHSIC):** A series of government programs designed to stimulate development and standardize complex microcircuit technology. 64

W

- wafer:** A disk of semiconductor material that forms the base on which a number of identical integrated circuits are built. In some cases, two or more designs may be built on the same wafer. In most facilities, five or more wafers are brought through each fabrication step simultaneously in a group known as a wafer lot. 31

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