

Microwave Data Transmission by means of an Optimal Bandwidth Multichannel QPSK System

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Declaration

I, the undersigned, hereby declare that the work contained in this thesis is my own original work and has not previously in its entirety or in part been submitted at any university for a degree.

Ek, die ondergetekende verklaar hiermee dat die werk gedoen in hierdie tesis my eie oorspronklike werk is wat nog nie voorheen gedeeltelik of volledig by enige universiteit vir 'n graad aangebied is nie.

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Synopsis

The increase in the complexity and functionality of new satellites leads to a growing demand for a digital communication system operating at a much higher bit rate than before. The main purpose of this thesis is to address precisely this problem.

The theory as well as a practical high speed system are custom-developed. The goal of this thesis is not to reinvent the wheel, but to use off-the-shelf products as far as possible. This system demonstrates that a very high data rate is not out of reach for a developer with limited funds.

The secondary goal is to understand the operation of this communication system. The emphasis is on the inaccuracies in the system. A design tool is created to act as a vehicle for understanding the influence of a single variable on the performance of the entire system.



Opsomming

Die toename in die kompleksiteit en funksionaliteit van nuwe satelliete lei tot die groeiende behoefte aan 'n digitale kommunikasiestelsel wat teen 'n heelwat hoër spoed funksioneer. Die hoofdoel van hierdie tesis is om juis hierdie probleem aan te spreek.

Die teorie en 'n praktiese hoëspoed stelsel is ontwikkel. Die doel van die tesis is nie om die wiel te herontdek nie maar om sover moontlik bestaande produkte in die ontwerp van die stelsel te gebruik. Die stelsel demonstreer dat 'n hoëspoed datatempo nie buite die bereik van 'n ontwikkelaar met beperkte fondse is nie.

'n Verdere doelwit is om die funksionering van die kommunikasie stelsel te begryp. Klem is gelê op die onakkuraathede in die kommunikasiestelsel. Ontwikkeling sagteware is geskep as 'n metode om die invloed van 'n enkele veranderlike op die werkverrigting van die stelsel as geheel te begryp.

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Glossary

Acronyms & Abbreviations

A	Ampere
AGC	Auto Gain Control Integrator Value
AM	Amplitude Modulation
BER	Bit Error Ratio
bps/Hz	bits per second per hertz
BPSK	Binary Phase Shift Keying
BR	Bit rate
BW_{LPF}	Bandwidth of Low-pass Filter
CD	Compact Disk
CF	Carrier Found
CFR	Carrier Frequency Register
CLDI	Carrier Lock Detector Register
dB	Decibel
dBm	Decibel with reference to 1 mW
DC	Direct Current
DDS	Direct Digital Synthesis
DIP	Dual Inline Package
DVB	Digital Video Broadcast
DVB-C	DVB Cable
DVB-S	DVB Satellite
DVB-T	DVB Terrestrial
ERRCNT	Error Count Register
FDM	Frequency Division Multiplex
FM	Frequency Modulation
FPGA	Field-Programmable Gate Array
GHz	Gigahertz
hex	Hexadecimal notation
HF	High Frequency Range (3 - 30 MHz)
Hz	Hertz
I	In-phase Component
I^2C	Inter-IC bus
IC	Integrated Circuit
ISI	Intersymbol Interference
LED	Light Emitting Diode
LO	Local Oscillator
LPF	Low-pass Filter
LSB	Least Significant Bit
M-AM	M symbol Amplitude Modulation
Mbps	Mega bits per second
MHz	Megahertz

M-PSK	M symbol Phase Shift Keying
M-QAM	M symbol Quadrature Amplitude Modulation
MSB	Most Significant Bit
MSK	Minimum Shift Keying Modulation
Msp/s	Mega symbols per second
MUX	Multiplex
NIR	Noise Indicator Register
PCB	Printed Circuit Board
PM	Phase Modulation
PSK	Phase Shift Keying
<i>Q</i>	Quadrature Phase component
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RTF	Timing Frequency Register
SER	Symbol Error Rate
SNR	Signal-to-Noise Ratio
sps	Symbols per second
SR	Symbol Rate
SSB	Single Sideband
TLIR	Timing Lock Indicator Register
UHF	Ultrahigh Frequency Range (300 MHz - 3 GHz)
V	Volt
VERRO	Viterbi Errors
VHF	Very High Frequency Range (30-300 MHz)
W	Watt
XOR	Exclusive-Or

Variables

α	Roll-off / Excess Bandwidth Factor
A	Channel Amplitude
ϕ	Phase Error
f_c	Carrier Frequency
f_d	Data Frequency
$I(t)$	In-phase channel (time domain) before modulation
$I_{\text{Dem}}(t)$	In-phase channel (time domain) after demodulation
i_n	In-phase channel (time domain) before internal low-pass filter in demodulator
k	Quadrature phase error at the I/Q channel
λ	Phase error in a quadrature mixer's local oscillator signal
$M_I(t)$	In-phase Local Oscillator Component
$M_Q(t)$	Quadrature-phase Local Oscillator Component
$Q(t)$	Quadrature-phase channel (time domain) before modulation
$Q_{\text{Dem}}(t)$	Quadrature-phase channel (time domain) after demodulation
q_n	Quadrature-phase channel (time domain) before internal low-pass filter in demodulator
$S(t)$	RF output after QPSK Modulation (time domain)
S_x	RF output, modulated with digital I/Q value x
S_i	I component of QPSK modulated signal
S_q	Q component of QPSK modulated signal
t	Continuous Time
T_s	Symbol Period
ω_c	Angular Carrier Frequency [radians per second]
ω_d	Angular Frequency of Data [radians per second]
V_{pp}	Peak-to-Peak Voltage
$y(t)$	RF output after QPSK Modulation (time domain)
ρ	Amplitude deviation in an I/Q channel
$x(t)$	Input data stream of channel
$x'(t)$	Output data stream of channel

Operations

$\Im\{\cdot\}$	Imaginary part of a complex value
$\Re\{\cdot\}$	Real part of a complex value

1 Introduction

Communication is at least as old as civilization, but electrical communication effectively started with the telegraph in the early 19th century. The telegraph revolutionized long-distance communications almost everywhere. The early telegraph was a very simple device. It used a direct current cell to operate an electromagnet. Morse code, a system of dots and dashes representing letters, was often used to send messages. As the circuit only had two states (*on* or *off*), the telegraph was essentially a digital apparatus [15].

As we enter the twenty-first century, we find ourselves in a world in which digital communication is commonplace. However, the importance of such communication in today's world is so crucial that modern society is unimaginable without it. As the population of the world expands, so does the demand for better, faster and cost-effective communication systems.

1.1. Problem Statement

The main goal of this thesis is the development of an affordable, high speed, digital communication system. The modulator and demodulator are usually the main components responsible for the speed limit of a communication system. Thus, the choice of modulation scheme influences the speed and cost of a system. A relatively simple modulation scheme has the advantage of low cost and high availability, but has a low data rate. As the complexity of a modulation scheme increases (for a fixed occupied bandwidth), so does the data rate. The costs of such a commercial component (if it exists at all) are high. The time required for developing a custom modulator and demodulator is not always cost-effective. Therefore, the problem can be formulated as a simple question: how to find a cost-effective modulator and demodulator which operate at a high data rate.

1.2. Proposed Solution

There are several solutions to consider if a trade-off is accepted between speed and cost. Several modulation possibilities exist on the cost side. To qualify for this a modulator and demodulator must be commercially available at relatively low cost. The possibilities are: FM, BPSK, QPSK, AM and QAM. The best option among these would be QPSK, offering modulation with four symbols and a wide range of availability.

A high data rate can be achieved if a modulator and a demodulator are custom-made. Options for this are M-PSK and M-AM, which offer modulation with M symbols. It might be tedious and expensive to design and build these [20].

This thesis proposes the construction of a high speed communication system with the use of a simple modulation technique, such as QPSK. This system implements a special case of frequency division multiplexing where a number of QPSK channels are placed in parallel, each operating at a different carrier frequency. This solves the problem of speed as well as cost.

1.3. Thesis Outline

In order to find a starting point and for the sake of completeness of this thesis, chapter 2 explains the fundamental concepts regarding a digital communication system. Among these are bandwidth and symbol rate. The QPSK modulation and demodulation processes (and terminology regarding these) are explained. The concept of frequency division multiplexing is also explained.

In the discussion of the modulation process in chapter 2, it is assumed that no non-idealities are present. Chapter 3 extends this modulation process to accommodate non-idealities. The non-idealities considered are amplitude deviation, DC-offset, oscillator leakthrough, error in phase angle and limited bandwidth. The influence of these non-idealities on the performance of a system is investigated. These inaccuracies are dealt with on a theoretical basis in order to find a way to compensate for each inaccuracy in a physical system. A simulation tool is custom-developed in Matlab in order to visualize the effect of different non-idealities on the system.

In chapter 4 a QPSK transmitter is custom-developed. This transmitter consists of a data generator and a divider to split the data into four similar modulation channels. Each channel can be disabled. A combiner combines the output of the channels. Each channel consists of two line drivers, baseband filters and a QPSK modulator. The modulator's carrier frequency is generated by a frequency synthesizer. The QPSK transmitter is designed to be as flexible as possible. The data rate and carrier frequency are controlled by custom-developed software from a personal computer. It is possible to tune the transmitter in order to compensate for modulator inaccuracies.

In chapter 5 the Sancy DVB receiver is characterized. In order to do this, it is necessary to understand the operation of the DVB unit. Software was custom-developed to program the DVB's registers and to read the status of the demodulation process from the DVB to a user-friendly interface on a personal computer. Carrier

frequency, received power, different symbol rates, sample frequency and the influence of noise on the receiver's performance are among the characteristics which are investigated.

The QPSK transmitter and receiver are connected in chapter 6. Furthermore, the performance of the complete system is investigated. The transmitter is used in different configurations and the DVB receiver is used as a measure to gauge the performance of the system. One of the communication channels is enabled and the system's performance is measured. This is extended to a double- and later to a triple channel system. The influence of baseband shaping is investigated for each of these cases.

In chapter 7 the outcome of the thesis is summarized. This thesis produces a solid foundation for further development. The hardware and software were custom-developed and can be used in further studies. Some recommendations are made for this.

2. Background Information

It is important to understand several aspects regarding digital communication systems. Some of these will be dealt with in this chapter. The first is the phasor diagram. This will help to understand the modulation scheme. The QPSK modulator and demodulator will be discussed in detail. The subject of bandwidth will also be touched.

2.1. Polar Diagram

A simple way to view amplitude and phase simultaneously is with the polar diagram. The carrier signal becomes an amplitude and phase reference and the signal is interpreted relative to the carrier. The signal can be expressed in polar form as a magnitude and a phase [19]. The phase is relative to the reference signal, the carrier in most communication systems. The magnitude is either an absolute or a relative value. Both are used in digital communication systems. Polar diagrams form the basis of many displays used in digital communications, although it is common to describe the signal vector by its rectangular coordinates of I (in-phase) and Q (quadrature phase). A simple polar diagram is shown in Figure 1 [1].

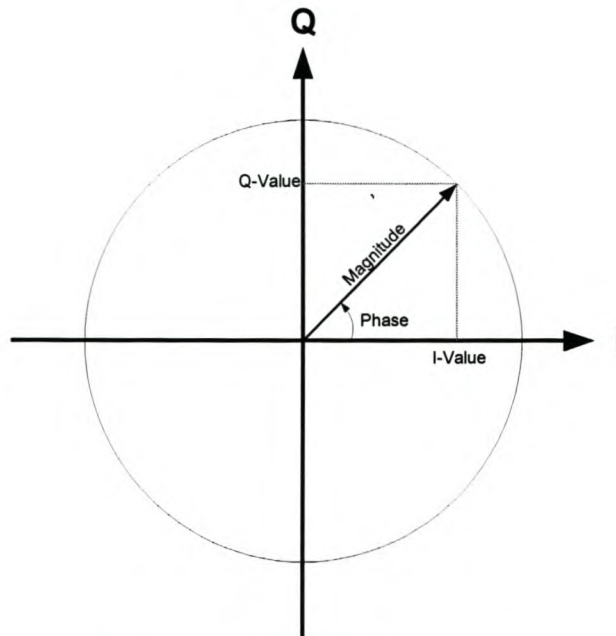


Figure 1 Polar Diagram

As shown in Figure 1, magnitude is represented as the distance from the centre and phase is represented as the angle. Amplitude modulation (AM) changes only the magnitude of the signal. Phase modulation (PM) changes only the phase of the signal. Amplitude and phase modulation can be used together. Frequency modulation (FM) looks similar to phase modulation, though frequency is the controlled parameter, rather than relative phase. This thesis focuses on the use of phase modulation.

In digital communication, modulation is often expressed in terms of I and Q . This is a rectangular representation of the polar diagram. As shown in Figure 1, the I -axis lies on the zero degree phase reference, and the Q -axis is rotated by 90° . The signal vector's projection onto the I -axis is its I component and the projection onto the Q -axis is its Q component.

2.2. Bandwidth and Related Terminology

When a carrier wave is modulated, it is no longer a single frequency but is spread out over a range of frequencies. The bandwidth of the modulated carrier wave is the range from lowest to highest frequency, with the original carrier frequency in the center [1].

One of the design parameters in any communication system is the bandwidth occupied for the transmission of data. The goal of a modulation scheme is to increase the data rate and decrease the occupied bandwidth. In order to understand and compare different modulation scheme efficiencies, it is important to first understand the difference between bit rate and symbol rate.

2.2.1. Bit Rate and Symbol Rate

The signal bandwidth needed for the communications channel depends on the symbol rate, not on the bit rate. Bit rate is the frequency of a system bit stream (the extra bits required for synchronization, error correction, etc. are ignored). As shown in equation (2.1), the symbol rate is the bit rate divided by the number of bits that can be transmitted with each symbol.

$$\text{Symbol Rate} = \frac{\text{Bit Rate}}{\text{Number of bits transmitted with each Symbol}} \quad [\text{sps}] \quad (2.1)$$

If one bit is transmitted per symbol (as with BPSK modulation), then the symbol rate would be equal to the bit rate. If two bits are transmitted per symbol (as in QPSK modulation), then the symbol rate would be half of the bit rate. Symbol rate is sometimes called *baud rate*. These terms are often confused. Note that baud rate is not always equal to the bit rate. If more bits can be sent with each symbol, then the same amount of data can be sent in a narrower bandwidth. This is why modulation formats that are more complex and use a higher number of states, can send the same information over a narrower RF bandwidth.

2.2.2. Theoretical Bandwidth Efficiency Limits

The principle measure of performance for the various modulation schemes is the probability of error. This measure indicates how a given modulation scheme performs. Another measure is the bandwidth occupancy of the modulated signal, specifically, the data rate in bits per second that can be achieved by a given modulation scheme through a channel of a given bandwidth in hertz. The measure of effective bandwidth is open to several possibilities. Two of these are [7]:

- the half-power bandwidth - the bandwidth such that the power spectrum of the signal is within 3 dB of its peak value (inside the main lobe),
- the null-to-null bandwidth - the width of the main spectral lobe.

The definition of half power bandwidth will be adopted for the purpose of this thesis. The effective bandwidth of such a system is indicated in Figure 2 on the spectrum of a QPSK modulated signal. The carrier frequency, bit rate and symbol rate are indicated by f_c , BR and SR respectively.

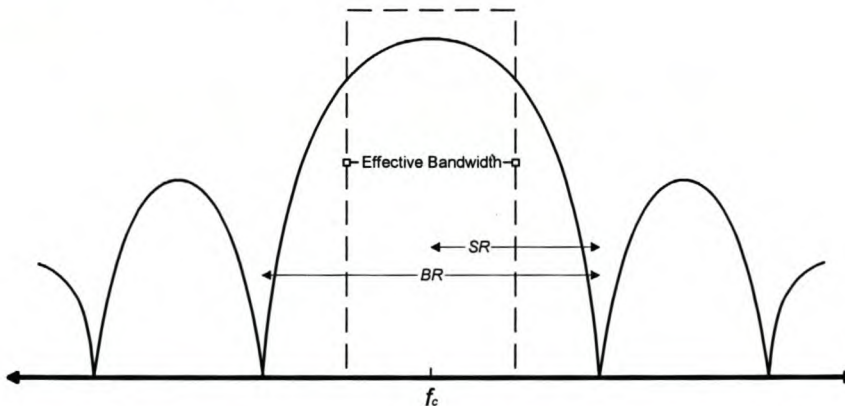


Figure 2 Effective Bandwidth of a QPSK Modulated Signal

Table 1 shows the theoretical bandwidth efficiency limits (half-power bandwidth) for the main modulation types. Note that these figures cannot actually be achieved in practical systems since they require perfect modulators, demodulators, filters and transmission paths [1].

Table 1 Effective Bandwidth

Modulation format	Theoretical Bandwidth Efficiency Limits
MSK	1 bps/Hz
BPSK	1 bps/Hz
QPSK	2 bps/Hz
8PSK	3 bps/Hz
16 QAM	4 bps/Hz
32 QAM	5 bps/Hz
64 QAM	6 bps/Hz
256 QAM	8 bps/Hz

According to Table 1 the bandwidth efficiency for a QPSK system is 2 bps/Hz. Stated differently, the bandwidth required for the transmission of 50 Mbps is 25 MHz.

2.3. QPSK Modulation

Modulation is the process whereby a carrier wave of a particular frequency is modified (or modulated) by the message signal, so that the modulated carrier wave can be used to carry the message over a distance.

A QPSK modulator modulates the phase of the carrier rather than using the amplitude or the frequency to convey information. The carrier is forced into four different phase states, each presenting a data symbol. Each symbol presents two data bits, thus doubling the potential quantity of data that is transmitted in a given bandwidth.

The digital data stream is divided into two parallel data streams at half the rate of the original bit rate and mapped to symbols. Each symbol is represented by an I/Q combination. A block diagram of the modulation process is shown in Figure 3 [25, 19,11].



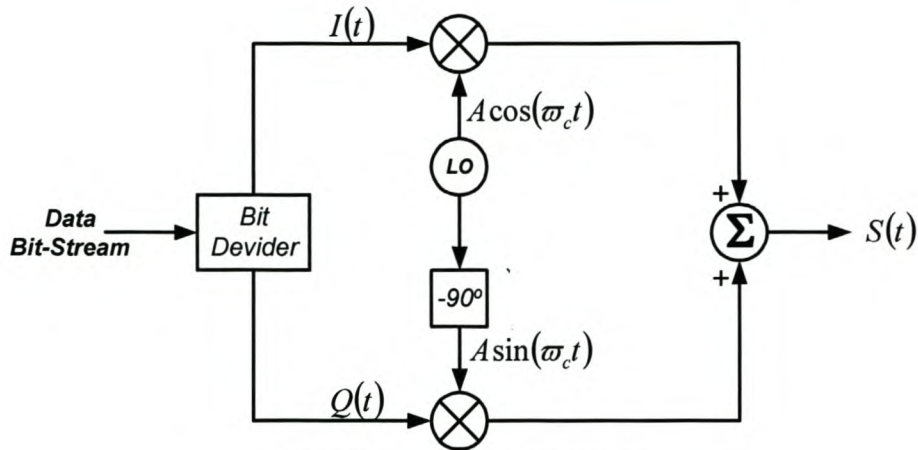


Figure 3 QPSK Modulator

The modulator mixes the I and Q value with an in-phase and a quadrature-phase (90°) carrier signal respectively. The carrier signal's angular frequency is indicated by ω_c . The mixing product is added to generate the modulated signal. The modulation process is mathematically represented in equation (2.2).

$$S(t) = I(t) A \cos(\omega_c t) + Q(t) A \sin(\omega_c t) \quad (2.2)$$

If a digital $(1,0)$ is to be modulated, the mathematical expression follows in equation (2.3). An I/Q channel amplitude of A and $-A$ represents a digital 1 and 0 respectively.

$$\begin{aligned} S_{10} &= A \cos(\omega_c t) - A \sin(\omega_c t) \\ &= A\sqrt{2} \cos(\omega_c t + 45^\circ) \end{aligned} \quad (2.3)$$

If the simplification in equation (2.3) is followed, the signal of $(0,1)$ is given by equation (2.4).

$$\begin{aligned} S_{01} &= -A \cos(\omega_c t) + A \sin(\omega_c t) \\ &= -[A \cos(\omega_c t) - A \sin(\omega_c t)] \\ &= A\sqrt{2} \cos(\omega_c t - 135^\circ) \end{aligned} \quad (2.4)$$

The signal of $(0,0)$ is given by equation(2.5).

$$\begin{aligned}
 S_{00} &= -A \cos(\omega_c t) - A \sin(\omega_c t) \\
 &= -[A \cos(-\omega_c t) - A \sin(-\omega_c t)] \\
 &= -A\sqrt{2} \cos(\omega_c t - 45^\circ) \\
 &= A\sqrt{2} \cos(\omega_c t + 135^\circ)
 \end{aligned} \tag{2.5}$$

If the simplification in equation (2.5) is followed, the symbol of $(1,1)$ is shown in equation (2.6).

$$\begin{aligned}
 S_{11} &= A \cos(\omega_c t) + A \sin(\omega_c t) \\
 &= A\sqrt{2} \cos(\omega_c t - 45^\circ)
 \end{aligned} \tag{2.6}$$

These result are summarized in Table 2.

Table 2 Summary of QPSK Modulation Technique

I/Q Digital Input Data	I/Q Input Voltage	Modulated Output Signal
0,0	(-A,-A)	$A\sqrt{2} \cos(\omega_c t + 135^\circ)$
0,1	(-A,A)	$A\sqrt{2} \cos(\omega_c t - 135^\circ)$
1,0	(A,-A)	$A\sqrt{2} \cos(\omega_c t + 45^\circ)$
1,1	(A,A)	$A\sqrt{2} \cos(\omega_c t - 45^\circ)$

The modulated symbols (as calculated in equations (2.3), (2.4), (2.5) and (2.6)) are shown in Figure 4. The channel amplitude used was $A=1$. The four modulated time domain symbols and corresponding signal space representation are shown in Figure 4.

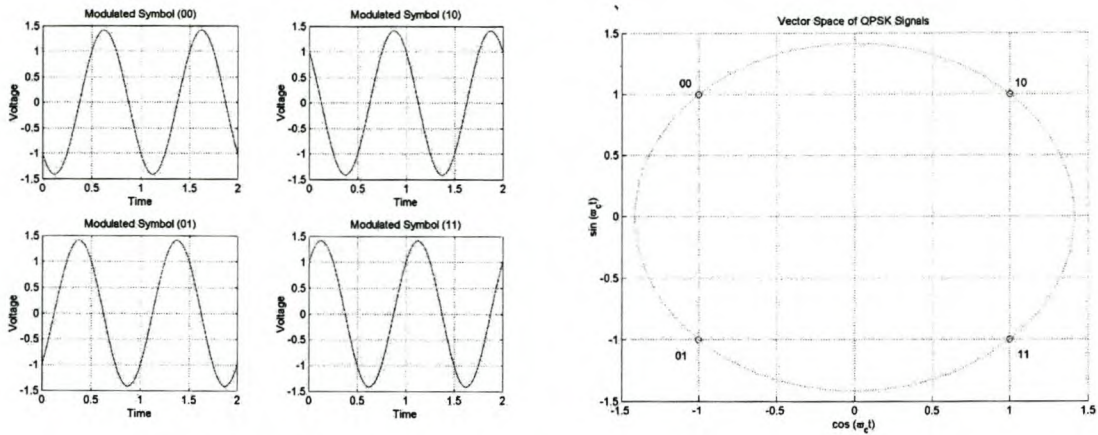


Figure 4 QPSK Modulated Symbols and Signal Space

2.4. QPSK Demodulation

The quadrature demodulator mixes the input signal with an in-phase and quadrature-phase carrier signal to produce the analogue I and Q signals. The received signal is thus multiplied by $A\cos(\omega_c t + \phi)$ and $A\sin(\omega_c t + \phi)$, where ϕ is the phase difference between the received and the locally generated carrier frequency. After multiplication, the signal is low-pass-filtered to remove the unwanted mixing products. The bandwidth of this filter is equal to the symbol rate. A block diagram of the demodulation process is shown in Figure 5.

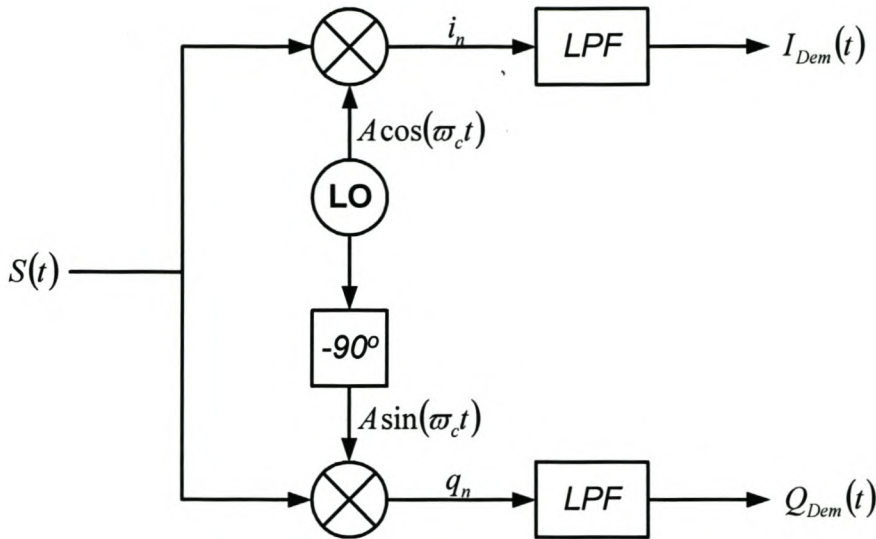


Figure 5 QPSK Demodulator

If the phase error ϕ is zero, the demodulation process is mathematically expressed in equation (2.7). The low-pass filter is replaced by the mathematical integrator, integrating over one symbol period [34].

$$I_{dem}(t) = A \int_{t_0}^{t_0+T_s} S(t) \cos(\omega_c t) dt$$

$$Q_{dem}(t) = A \int_{t_0}^{t_0+T_s} S(t) \sin(\omega_c t) dt$$
(2.7)

2.4.1. Phase Ambiguity

For a non-zero phase difference ($\phi \neq 0$), the phasor diagram is shown in Figure 6 and the demodulated output I/Q channels are given by equations (2.8).

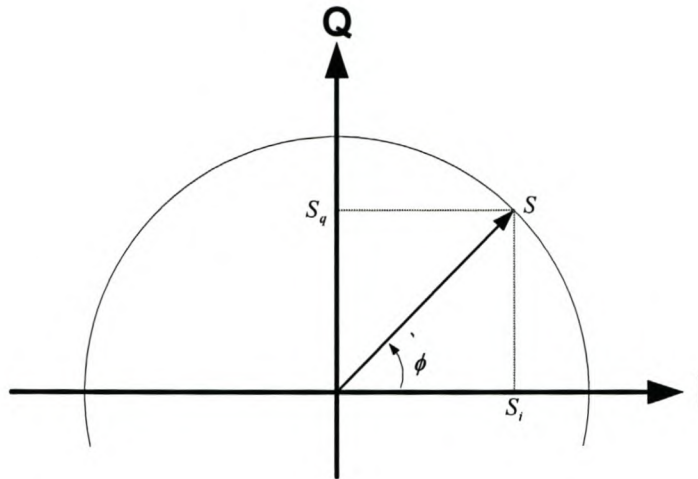


Figure 6 Polar Diagram when $\phi \neq 0$

$$\begin{aligned} I_{dem}(t) &= S_i(t) \cos \phi + S_q(t) \sin \phi \\ Q_{dem}(t) &= S_q(t) \cos \phi + S_i(t) \sin \phi \end{aligned} \quad (2.8)$$

For values different from $\phi = 0^\circ \pm k90^\circ$, the $\cos \phi$ and $\sin \phi$ terms in equation (2.8) represent crosstalk. There will be no crosstalk between the I and Q channels if expression (2.9) is true.

$$\phi = 0^\circ \pm k90^\circ \quad \text{where } k = 0, 1, 2, 3, \dots \quad (2.9)$$

Expression (2.9) shows that four combinations are possible with no crosstalk: $I_{dem}(t) = \pm S_i(t)$ or $\pm S_q(t)$ and $Q_{dem}(t) = \pm S_i(t)$ or $\pm S_q(t)$. These combinations are listed in Table 3. This table shows that the constellation diagram is rotated by 90° each time. This effect is known as the phase ambiguity of 90° . Phase ambiguity is inherent in PSK systems and must be removed by coding or other means.

Table 3 Combinations of Phase Ambiguity

ϕ	I_{dem}	Q_{dem}	Signal Space						
0°	$S_i(t)$	$S_q(t)$	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">$^{00}\star$</td> <td style="text-align: center;">Q \star^{10}</td> </tr> <tr> <td colspan="2" style="text-align: center;">I</td> </tr> <tr> <td style="text-align: center;">$^{01}\star$</td> <td style="text-align: center;">\star^{11}</td> </tr> </table>	$^{00}\star$	Q \star^{10}	I		$^{01}\star$	\star^{11}
$^{00}\star$	Q \star^{10}								
I									
$^{01}\star$	\star^{11}								
90°	$-S_q(t)$	$S_i(t)$	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">$^{10}\star$</td> <td style="text-align: center;">Q \star^{11}</td> </tr> <tr> <td colspan="2" style="text-align: center;">I</td> </tr> <tr> <td style="text-align: center;">$^{00}\star$</td> <td style="text-align: center;">\star^{01}</td> </tr> </table>	$^{10}\star$	Q \star^{11}	I		$^{00}\star$	\star^{01}
$^{10}\star$	Q \star^{11}								
I									
$^{00}\star$	\star^{01}								
180°	$-S_i(t)$	$-S_q(t)$	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">$^{11}\star$</td> <td style="text-align: center;">Q \star^{01}</td> </tr> <tr> <td colspan="2" style="text-align: center;">I</td> </tr> <tr> <td style="text-align: center;">$^{10}\star$</td> <td style="text-align: center;">\star^{00}</td> </tr> </table>	$^{11}\star$	Q \star^{01}	I		$^{10}\star$	\star^{00}
$^{11}\star$	Q \star^{01}								
I									
$^{10}\star$	\star^{00}								
270°	$S_q(t)$	$-S_i(t)$	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td style="text-align: center;">$^{01}\star$</td> <td style="text-align: center;">Q \star^{00}</td> </tr> <tr> <td colspan="2" style="text-align: center;">I</td> </tr> <tr> <td style="text-align: center;">$^{11}\star$</td> <td style="text-align: center;">\star^{10}</td> </tr> </table>	$^{01}\star$	Q \star^{00}	I		$^{11}\star$	\star^{10}
$^{01}\star$	Q \star^{00}								
I									
$^{11}\star$	\star^{10}								

The carrier recovery loop should ensure that $\phi = 0^\circ \pm k90^\circ$ in order to minimize crosstalk for static values as well as fluctuations (phase jitter). When using the convolutional encoder and decoder, ambiguity is always resolved automatically [3].

2.5. Frequency Division Multiplexing

Frequency division multiplexing (FDM) is a multiplexing technique whereby several data signals are modulated to different spectral locations and combined to form a baseband signal. The data signals might have originated from separate sources or one single source split up [13]. Several different modulation schemes can be used to form the baseband. The carrier frequencies used to form the baseband are usually referred to as *subcarriers*. The baseband signal can be transmitted over a single channel using a single modulation process. This modulator is sometimes omitted.

The block diagram of a FDM modulator and demodulator with three channels is shown in Figure 7 [34].

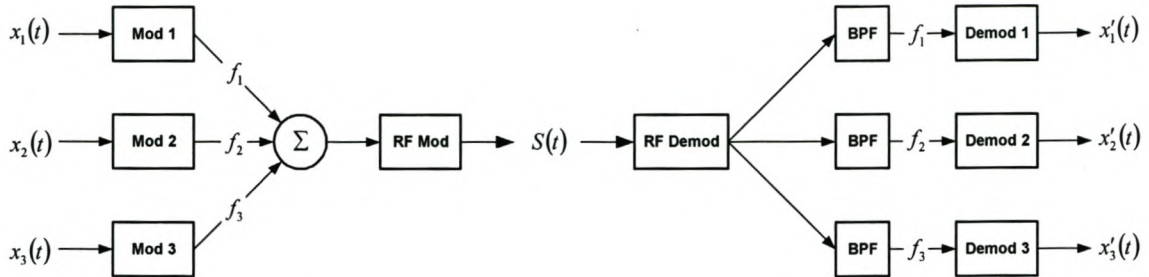


Figure 7 Block Diagram of FDM Modulator and Demodulator

The baseband frequency spectrum of the combined signal is shown in Figure 8. The modulated spectrum of all the channel modulators is not similar since different modulators were used as an example.

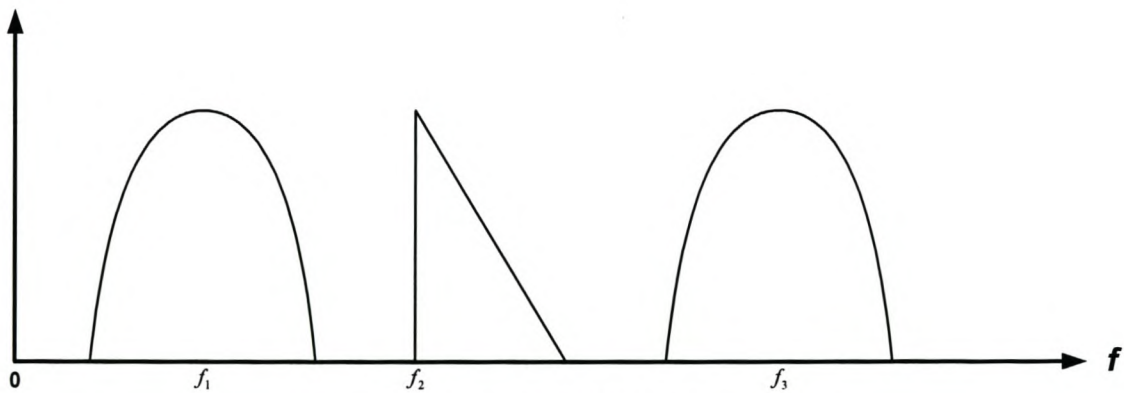


Figure 8 Baseband FDM Spectrum

3. Inaccuracies in a QPSK System

The QPSK modulator and demodulator discussed in chapter 2 were assumed ideal. In a physical system several inaccuracies might occur. These and their influence on the performance of a system will be examined by way of theory and simulation.

3.1. Amplitude Deviation

It is possible that the I and Q output channels do not produce signals with perfectly matched amplitudes [19]. This effect can typically be caused by low-pass filters with poorly matched amplitude responses in the passband. Imperfections in the mixing circuit could also produce a slight discrepancy in the amplitudes of the two local oscillator signals. Whatever the source of mismatch, we will assume that the mismatch is constant. The influences of this possible mismatch will be investigated in this section.

3.1.1. Theoretical Analysis of a Single Sideband System

The theoretical method followed will be to determine the influence of amplitude mismatch on a single sideband system. This is where the Q channel is delayed by 90° in respect to the I channel. The influence of mismatch will be investigated on a system with a single sideband sinusoidal signal as input. The results will then be extended to a rectangular, single sideband, signal as input. This will be accomplished with the use of Fourier series, to construct a rectangular wave by adding a number of sinusoidal signals together.

As mentioned previously, there are several places where amplitude mismatch might occur. The first is amplitude mismatch in a channel. This mismatch is mathematically expressed in equation (3.1). The amplitude mismatch is represented by ρ . The angular frequency, ω_d , is chosen as half the symbol rate. The reason for this will become apparent later in this section.

$$\begin{aligned} I(t) &= (A + \rho) \cos(\omega_d t) \\ Q(t) &= A \sin(\omega_d t) \end{aligned} \quad (3.1)$$

The second possible amplitude mismatch is in one of the local oscillator signals. This is mathematically expressed in equation (3.2). The carrier angular frequency is represented by ω_c .

$$\begin{aligned} M_I(t) &= (A + \rho) \cos(\omega_c t) \\ M_Q(t) &= A \sin(\omega_c t) \end{aligned} \quad (3.2)$$

Regardless of whether the amplitude deviation is present in the I/Q input channel or in the local oscillator signal, the resultant RF output signal can be written in the form as shown in equation (3.3).

$$y(t) = (A + \rho) \cos(\omega_d t) \cos(\omega_c t) + A \sin(\omega_d t) \sin(\omega_c t) \quad (3.3)$$

Without loss of generality, the rest of this section will therefore only consider the effects of amplitude deviation at the I/Q inputs.

When amplitude mismatch is present, a plot of the I/Q phasor locus produces an ellipse instead of a circle, as illustrated in Figure 9.

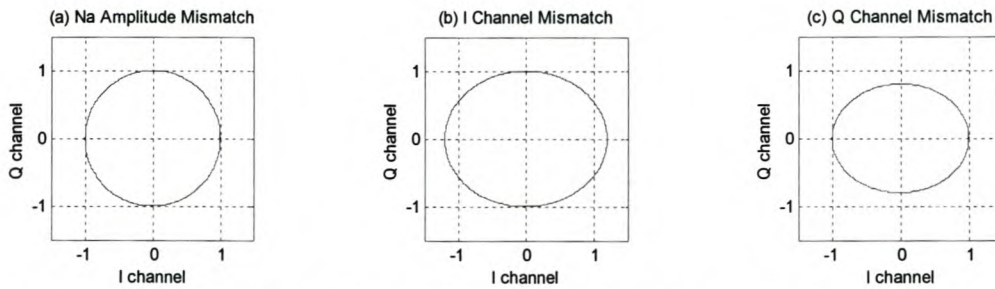


Figure 9 Influences of Amplitude Mismatch in a System with SSB Sinusoidal Signals as Input

The ellipse's main axes coincide with the I/Q axes, and the major axis of the ellipse corresponds to the channel with the largest amplitude [31]. In Figure 9(b) the I channel's amplitude is increased with 20%, whereas in Figure 9(c) the Q channel's amplitude is decreased with 20%.

Effect on Spectrum

Before the effect of amplitude mismatch is considered further, the case of no mismatch ($\rho=0$) will be investigated. Equation (3.3) is simplified to equation (3.4).

$$\begin{aligned} y(t) &= A \cos(\omega_c t) \cos(\omega_d t) + A \sin(\omega_c t) \sin(\omega_d t) \\ &= A \cos(\omega_c - \omega_d)t \end{aligned} \quad (3.4)$$

The frequency spectrum of equation (3.4) is shown in Figure 10. The input frequency is at 50 MHz and the carrier frequency is at 2 GHz.

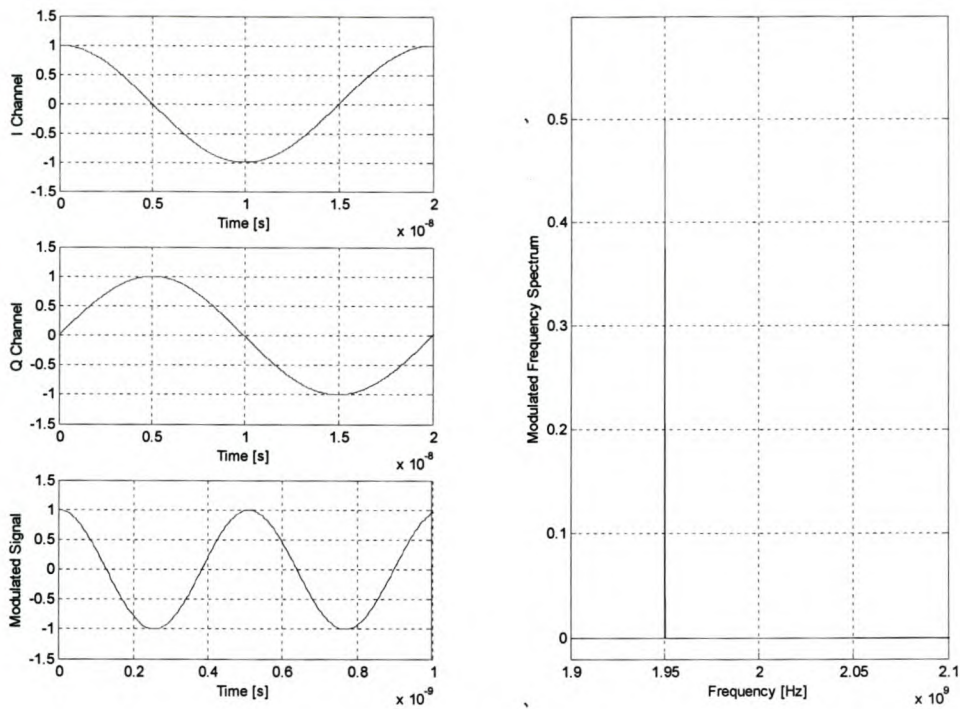


Figure 10 Frequency Spectrum of a Transmitter with a SSB Sinusoidal Signal as Input where No Amplitude Mismatch Occur

When the I and Q channel is similar and mixed with the carrier frequency, two frequency components will be present; one above and one below the carrier frequency. As shown in Figure 10 the only frequency component is below the carrier frequency, thus the term *single sideband*.

The effect of amplitude mismatch can now be taken into account. Equation (3.3) can be expanded as shown in equation (3.5).

$$\begin{aligned}
 y(t) &= \rho \cos(\omega_d t) \cos(\omega_c t) + A \cos(\omega_d t) \cos(\omega_c t) + A \sin(\omega_d t) \sin(\omega_c t) \\
 &= \rho \cos(\omega_d t) \cos(\omega_c t) + A \cos(\omega_c - \omega_d) t
 \end{aligned} \tag{3.5}$$

When comparing equation (3.4) with equation (3.5), the $\rho \cos(\omega_d t) \cos(\omega_c t)$ term is clearly the spurious mismatch. The frequency spectrum of equation (3.5) is shown in Figure 11. A mismatch of 10% is present in the I channel.

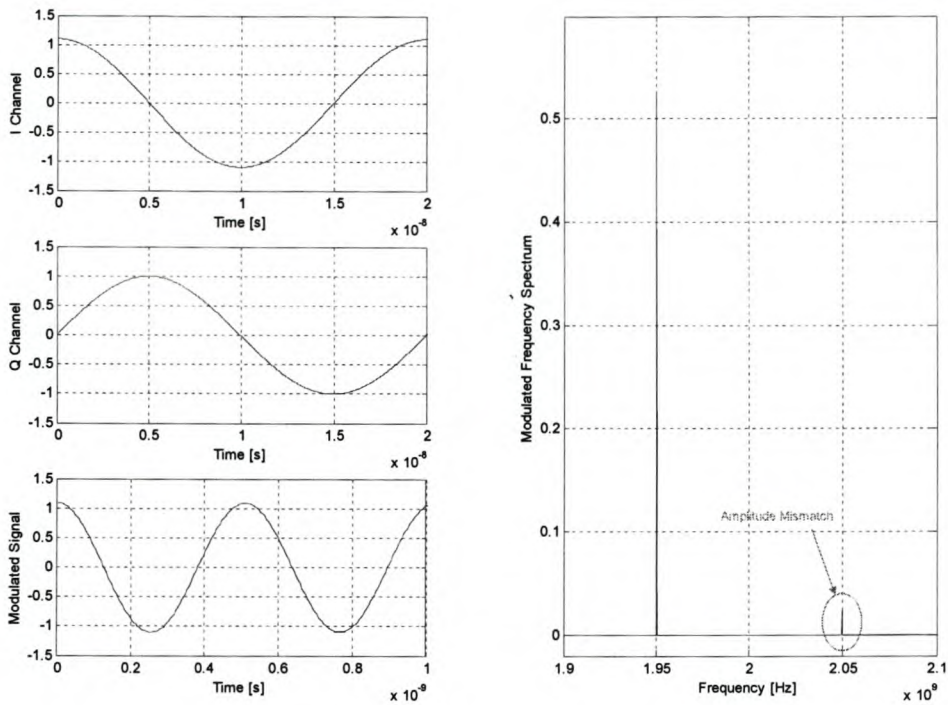


Figure 11 Frequency Spectrum of a Transmitter with a SSB Sinusoidal Signal as Input where Amplitude Mismatch Occur

Figure 11 shows that a mismatch causes a spurious frequency component to appear. This component has an amplitude of $\rho/4$; the desired and the spurious frequency components appear at positions that are symmetric around the carrier frequency. A component of amplitude $\rho/4$ is also added to the desired component. This means that the desired component is somewhat amplified for positive ρ (but attenuated for negative ρ).

Since it is simple to generate a rectangular single sideband wave with a FPGA, theorem must be developed to accommodate for such a signal. The same principles are extended to a rectangular wave. According to Fourier's theorem, a block wave can be approximated by a number of sinusoidal signals added together [35]. The series for the I channel is shown in equation (3.6). T_0 is the period of two symbols, a binary 01.

$$\begin{aligned}
 x(t) &= \begin{cases} -\frac{A}{2} & \text{for } \frac{T_0}{4} \leq t \leq \frac{3T_0}{4} \\ \frac{A}{2} & \text{elsewhere} \end{cases} & 0 \leq t \leq T_0 \text{ and } x(t) = x(t+T_0) \\
 x(t) &= \sum_{n=1}^{\infty} A \operatorname{sinc}\left(\frac{n}{2}\right) e^{j(n\omega_0)t} \\
 &= A \frac{2}{\pi} \sin\left(\frac{1}{2}\pi\right) e^{j(\omega_0)t} + A \frac{2}{3\pi} \sin\left(\frac{3}{2}\pi\right) e^{j(3\omega_0)t} + \dots \\
 \Re\{x(t)\} &= A \frac{2}{\pi} \sin\left(\frac{1}{2}\pi\right) \cos(\omega_0 t) + A \frac{2}{3\pi} \sin\left(\frac{3}{2}\pi\right) \cos(3\omega_0 t) + \dots \\
 &= 0.637 A \cos(\omega_0 t) - 0.212 A \cos(3\omega_0 t) + \dots
 \end{aligned} \tag{3.6}$$

The same can be applied for the Q channel, where a phase delay of 90° is present. This series is shown in equation (3.7)

$$\begin{aligned}
 x(t) &= \begin{cases} \frac{A}{2} & \text{for } 0 \leq t \leq \frac{T_0}{2} \\ -\frac{A}{2} & \text{elsewhere} \end{cases} & 0 \leq t \leq T_0 \text{ and } x(t) = x(t+T_0) \\
 x(t) &= \sum_{n=-\infty}^{\infty} \frac{A}{2} \operatorname{sinc}\left(\frac{n}{2}\right) e^{j\left(n\omega_0 t - \frac{\pi n}{2}\right)} \\
 \Re\{x(t)\} &= \sum_{n=1}^{\infty} A \operatorname{sinc}\left(\frac{n}{2}\right) \cos\left(n\omega_0 t - \frac{\pi n}{2}\right) \\
 &= A \left(\frac{2}{\pi}\right) \sin\left(\frac{\pi}{2}\right) \cos(\omega_0 t - 90^\circ) + A \left(\frac{2}{3\pi}\right) \sin\left(\frac{3\pi}{2}\right) \cos(3\omega_0 t - 270^\circ) + \dots \\
 &= 0.6366 A \sin(\omega_0 t) + 0.2122 A \sin(3\omega_0 t) + \dots
 \end{aligned} \tag{3.7}$$

The rectangular wave will be approximated by only the first two terms of equations (3.6) and (3.7). If an amplitude mismatch is present in the new I channel of equation (3.6) and used as input to the modulator, the modulated signal is represented by equation (3.8)

$$\begin{aligned}
 y(t) &= [(0.637A + \rho_A) \cos(\omega_d t) + (-0.212A + \rho_B) \cos(3\omega_d t)] \cos(\omega_c t) \\
 &\quad + [0.637A \sin(\omega_d t) + 0.212A \sin(3\omega_d t)] \sin(\omega_c t) \\
 &= [(A' + \rho_A) \cos(\omega_d t) + (-B' + \rho_B) \cos(3\omega_d t)] \cos(\omega_c t) \\
 &\quad + [A' \sin(\omega_d t) + B' \sin(3\omega_d t)] \sin(\omega_c t) \\
 &= \rho_A \cos(\omega_d t) \cos(\omega_c t) + A' \cos(\omega_c - \omega_d)t \\
 &\quad + \rho_B \cos(3\omega_d t) \cos(\omega_c t) - B' \cos(3\omega_d + \omega_c)t
 \end{aligned}
 \tag{3.8}$$

Figure 12 shows the frequency spectrum of the signal represented by equation (3.8), with a 10% mismatch in the *I* channel. The carrier frequency is at 2 GHz and the channel frequency is at 50 MHz.

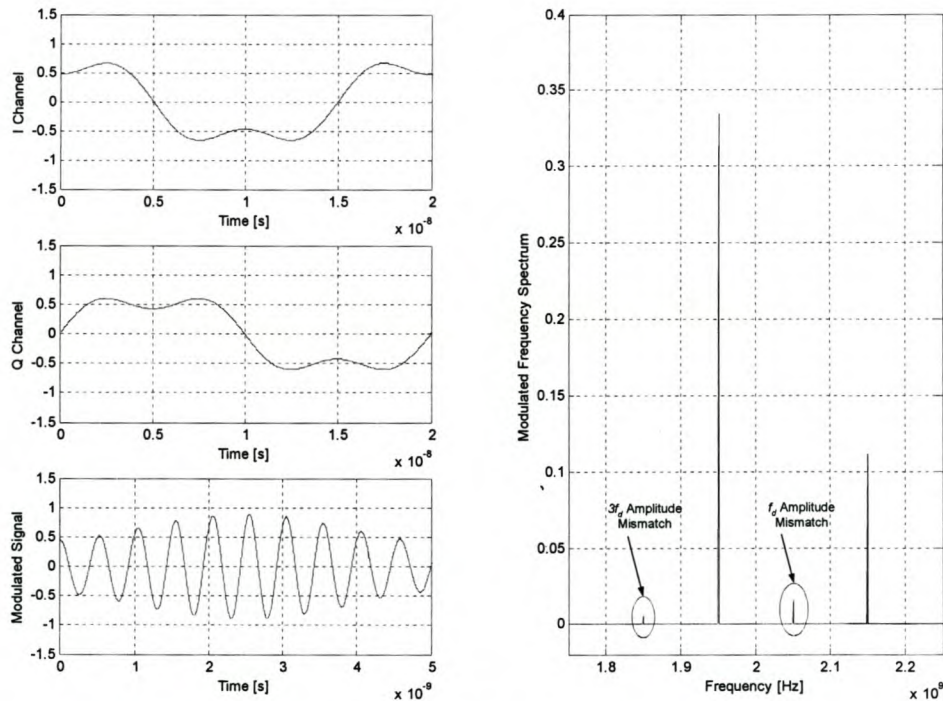


Figure 12 Frequency Spectrum of a Transmitter with a SSB Block Wave Signal as Input where Amplitude Mismatch Occur

It can be seen that the spurious mismatch terms are added at the mirror frequency of each sinusoidal term. The same is true when a true rectangular wave is approximated by adding infinite sinusoidal signals.

3.1.2. Random Data

As with a single sideband system with sinusoidal input, the amplitude of the input I and Q channels are varied. The influence of this variation on the constellation diagram is shown in Figure 13.

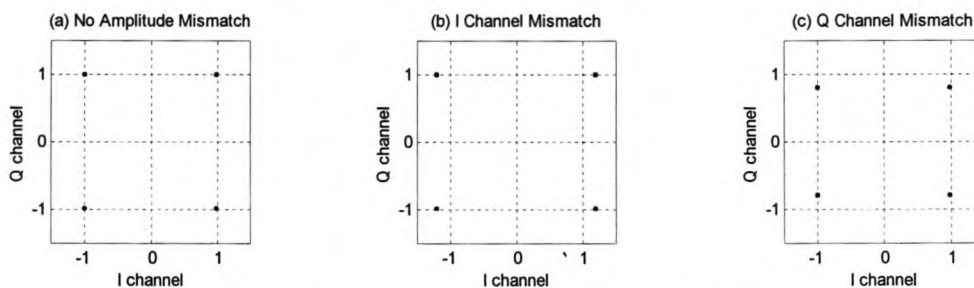


Figure 13 Influences of Amplitude Mismatch in a System with Random Data as Input

The constellation diagram of a system with no amplitude mismatch is shown in Figure 13(a). If the amplitude of the I channel is increased, the constellation diagram stretches in the I direction, as shown in Figure 13(b). A decrease in the Q channel amplitude causes the constellation diagram to compress in the Q direction as shown in Figure 13(c).

3.2. DC-Offset and Oscillator Leakage

In a practical system it is possible that the input I and Q channel might have a DC-offset relative to signal ground. Also, when a non-ideal mixer is used to up convert the channels, some oscillator leakage will be present [19]. The assumption will be made that both non-idealities are constant. The influences of these possible mismatches will be investigated in this section.

3.2.1. Theoretical Analysis of a Single Sideband System

The analysis will be done for a sinusoidal I/Q channel input and later extended to a rectangular wave input. When a DC-offset is present at the single sideband sinusoidal I/Q channels, the channel signals can be written as in equation (3.9).

$$\begin{aligned} I(t) &= A \cos(\omega_d t) + \varepsilon_i \\ Q(t) &= A \sin(\omega_d t) + \varepsilon_q \end{aligned} \quad (3.9)$$

When DC-offset occurs, a plot of the I/Q phasor locus produces a shift, as illustrated in Figure 14.

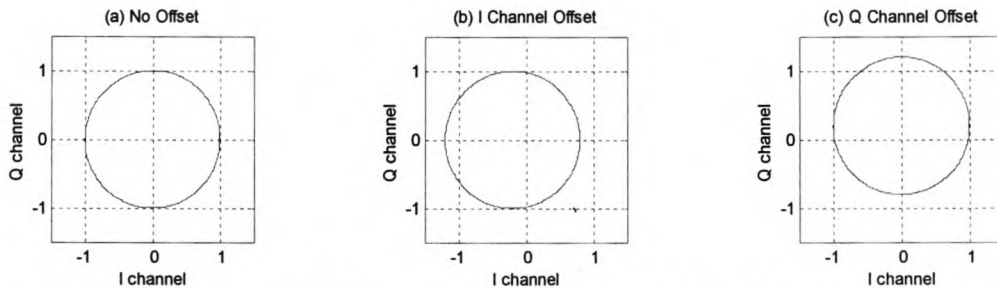


Figure 14 Influence of DC-offset in a system with a SSB Sinusoidal Signal as Input

The shift is in the direction of the I and/or the Q axis, depending on the channel where the offset occurs. In Figure 14(b) the I channel has a negative offset of 20%, whereas in Figure 14(c) the Q channel has a positive offset of 20%.

When these displaced signals are upconverted by the quadrature mixer, the RF output signal can be written in the form as shown in equation (3.10).

$$\begin{aligned}
 y(t) &= [A \cos(\omega_d t) + \varepsilon_i] \cos(\omega_c t) + [A \sin(\omega_d t) + \varepsilon_q] \sin(\omega_c t) \\
 &= A \cos(\omega_d t) \cos(\omega_c t) + A \sin(\omega_d t) \sin(\omega_c t) \\
 &\quad + \varepsilon_i \cos(\omega_c t) + \varepsilon_q \sin(\omega_c t) \\
 &= A \cos(\omega_c - \omega_d)t + \alpha \cos(\omega_c t + \gamma)
 \end{aligned}
 \tag{3.10}$$

where

$$\alpha = \sqrt{\varepsilon_i^2 + \varepsilon_q^2} \quad \text{and} \quad \gamma = \arctan\left(\frac{\varepsilon_q}{\varepsilon_i}\right)$$

From equation (3.10) it is clear that when a DC-offset occurs on one or both of the I/Q channels, a spurious signal of constant amplitude and frequency is added to the RF output. This spurious signal's frequency is equal to the carrier frequency and its amplitude is equal to the displacement in the phasor diagram. Its phase, relative to the I axis, is determined by the direction in which the locus is displaced from the origin. Local oscillator leakthrough and DC-offset in the I/Q channels have exactly the same type of effect on the output signal. This is illustrated in the I/Q phasor in Figure 15 [31].

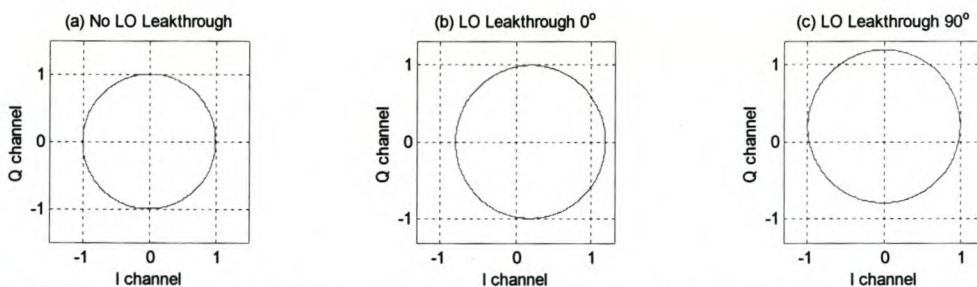


Figure 15 Influence of LO Leakthrough in a System with a SSB Sinusoidal Signal as Input

In Figure 15(b) an oscillator leakage of 20% is present with phase 0° . The shift is in the direction of the phase, measured anticlockwise from the I axis. This is illustrated when the phase is 90° , as in Figure 15(c).

Figure 16 shows the frequency spectrum of the signal represented by equation (3.10). The DC-offset in the I channel is 10% of the channel's amplitude. The carrier frequency is at 2 GHz and the frequency generated in each channel is at 50 MHz.

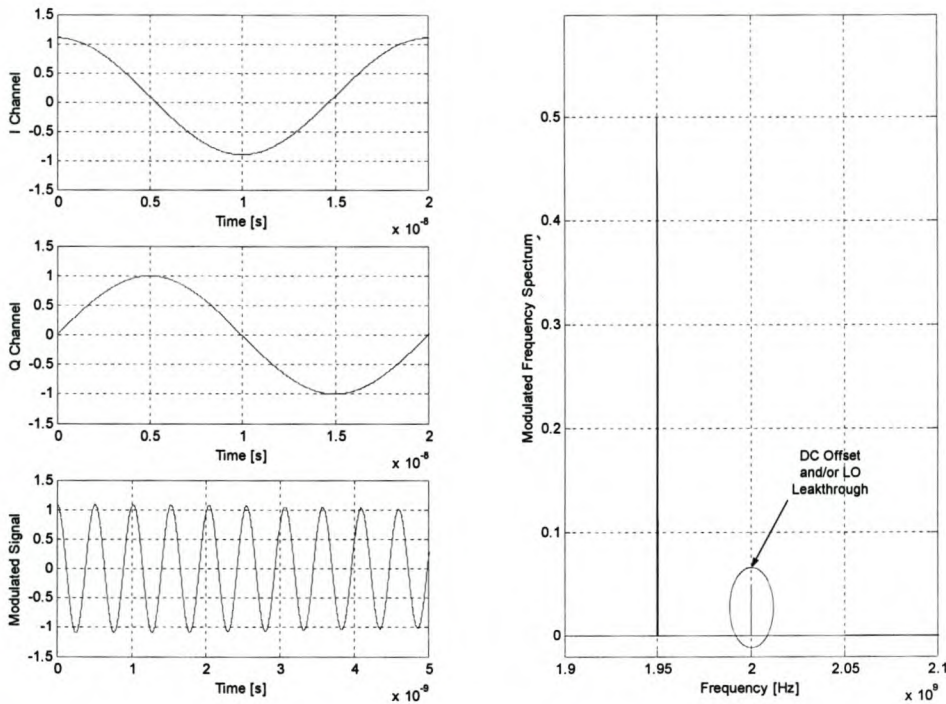


Figure 16 DC-offset and/or LO Leakage

As shown in Figure 16, a single frequency component, with amplitude and phase, as in equation (3.10) appears at the centre frequency.

When the sinusoidal I/Q channel input is extended to a rectangular wave, the same spurious frequency is present. The only difference in the frequency spectrum of the RF signal is the extra frequency components that are created when a rectangular wave is constructed by adding sinusoidal signals together. This concept was explained in equations (3.6) and (3.7).

It is reasonable to suspect, however, that a purposely generated DC-offset in the I/Q channels could in some way be used to compensate for an unwanted oscillator leakthrough in the mixing circuit.

In a physical modulator, even with compensation, some leakthrough will occur. The amount of carrier measured in dB below the desired output signal when a single sideband signal is applied to the I/Q ports is called *carrier rejection* [19]. This parameter is graphically shown in Figure 17.

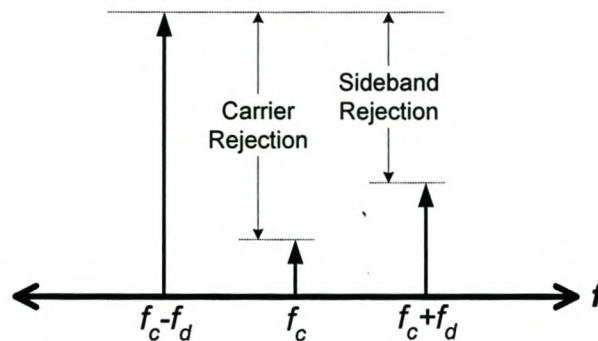


Figure 17 Measurement of Carrier and Sideband Rejection

3.2.2. Random Data

As with a single sideband system with sinusoidal input, the DC-offset of the input I and Q channels were varied. The influence of this variation on the constellation diagram is shown in Figure 18.

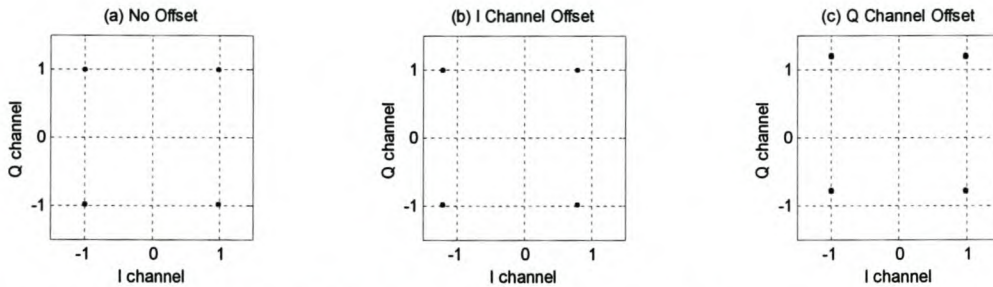


Figure 18 Influence of DC-offset in a System with Random Data as Input

As with a single sideband sinusoidal signal, the shift is in the direction of the I and/or the Q axis, depending on the channel where offset occurs. In Figure 18(b) the I channel has a negative offset of 20%, whereas in Figure 18(c), the Q channel has a positive offset of 20%.

To prove that the same effect is present for oscillator leakthrough, leakthrough was added to a system with random input data. The influence of this variation on the constellation diagram is shown in Figure 19.

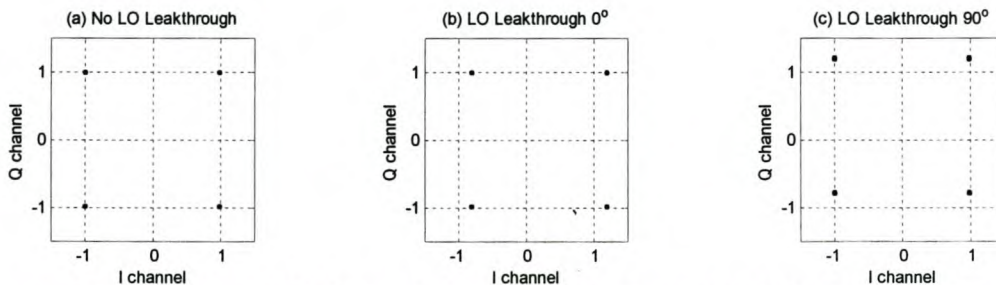


Figure 19 Influence of LO Leakthrough in a System with Random Data as Input

In Figure 19(b) an oscillator leakage of 20% is present with phase 0° . The shift is in the direction of the phase. This is illustrated when the phase is 90° , as in Figure 19(c).

As was suspected earlier, it is possible to cancel an oscillator leakthrough by adding a DC-offset. This is visually explained in Figure 20.

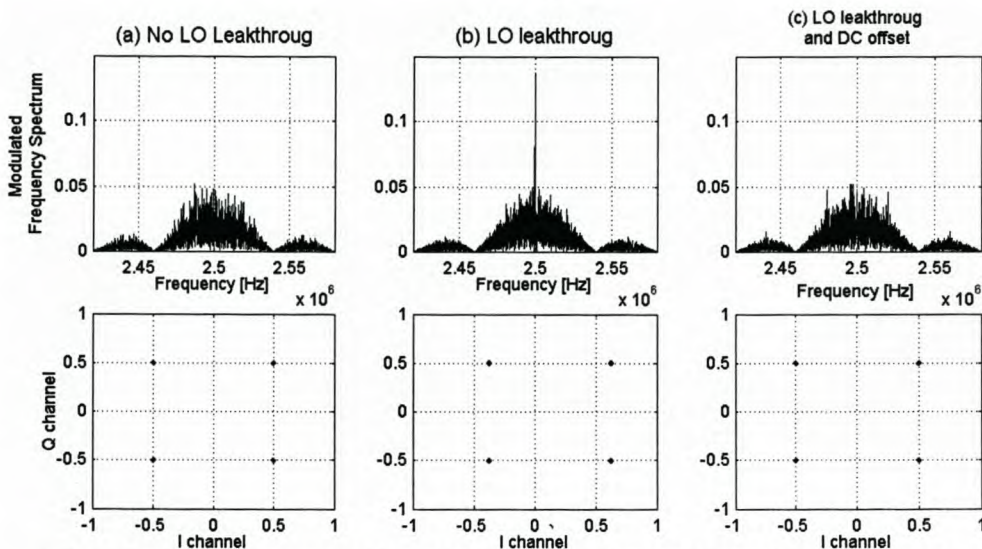


Figure 20 Compensation of LO Leakthrough with DC-Offset

As shown in Figure 20(b), the local oscillator leakthrough causes a shift in the state space. As shown in Figure 20(c), the leakthrough is compensated for by generating a DC-offset in the I channel.

3.3. Error in Phase Angle

In QPSK, the term *quadrature* implies that a system uses two sinusoidal signals, exactly 90° out of phase. In a physical system, such a perfect phase relationship is almost impossible to achieve [19].

3.3.1. Theoretical Analysis of a Single Sideband System

It is likely that a phase error could occur at either the I/Q channels, or in the quadrature carrier waves generated by the mixing circuit. It is more likely for a fairly

large phase error to be present in the quadrature carrier signals generated by the mixing circuit. It is reasonable to suspect, however, that a purposely generated phase error in the I/Q channels could in some way be used to compensate for an unwanted phase error in the mixing circuit.

Phase Deviation with Sinusoidal Input

The phase error in the I/Q channels will be investigated first. The phase deviation is defined as in equation (3.11) when single sideband sinusoidal signals are used.

$$\begin{aligned} I(t) &= A \cos(\omega_d t) \\ Q(t) &= A \sin(\omega_d t - \kappa) \end{aligned} \quad (3.11)$$

Figure 21(b) and (c) demonstrates the effect of the 10° phase error on the quadrature phasor's locus. No phase error is present in Figure 21(a).

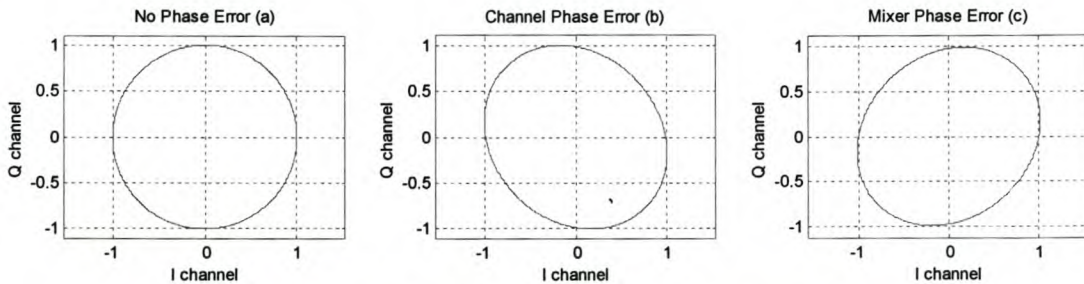


Figure 21 Effect of Phase Error on the I/Q Phasor's Locus

As was the case for amplitude deviation, the locus turns into an ellipse, but for phase error, the ellipse's major axis is rotated anticlockwise through 45° (for $\kappa > 0$) or clockwise through 45° (for $\kappa < 0$). Stated differently, the major axis of the ellipse lies either on the line $Q(t) = I(t)$ or on the line $Q(t) = -I(t)$. The larger the phase error, the greater the ellipse's eccentricity; at $\kappa = 90^\circ$ the ellipse collapses to a straight line.

If the phasor locus in Figure 9 is compared with that in Figure 21, it can be seen that the prior is a scaled rotation of the latter. It can be deduced that amplitude and

angular deviation cause similar disturbances. If the signals in equation (3.11) is modulated, the upconverted signal of equation (3.12) is created.

$$y(t) = A \cos(\omega_d t) \cos(\omega_c t) + A \sin(\omega_d t - \kappa) \sin(\omega_c t)$$

$$\text{for small } \kappa: \sin \kappa \approx \kappa \quad \cos \kappa \approx 1$$

$$y(t) \approx A \cos(\omega_c - \omega_d)t + A\kappa \cos(\omega_d t) \sin(\omega_c t)$$
(3.12)

As suspected, the spurious signal, caused by phase error, in a sinusoidal input is similar to that caused by amplitude mismatch. [31]

Phase Compensation

It was stated previously that it is worth investigating the possibility of purposely introducing a phase error in the I/Q channels, to compensate for phase inaccuracies in the quadrature mixer. The next few paragraphs will formally develop the theory for phase compensation.

Assume that a quadrature phase error of κ radians occurs at the in-phase input, $I(t)$. Also - the quadrature mixer has a phase inaccuracy of λ radians at the quadrature output, $Q(t)$. The resultant RF signal is shown in equation (3.13).

$$y(t) = A \cos(\omega_d t + \kappa) \cos(\omega_c t) + A \sin(\omega_d t) \sin(\omega_c t + \lambda)$$

$$= A \left[\cos(\omega_d t) \cos(\kappa) - \sin(\omega_d t) \sin(\kappa) \right] \cos(\omega_c t)$$

$$+ A \sin(\omega_d t) \left[\sin(\omega_c t) \cos(\lambda) + \cos(\omega_c t) \sin(\lambda) \right]$$
(3.13)

$$= A \cos(\kappa) \cos(\omega_d t) \cos(\omega_c t) + A \cos(\lambda) \sin(\omega_d t) \sin(\omega_c t)$$

$$+ \left[\sin(\lambda) - \sin(\kappa) \right] \sin(\omega_d t) \cos(\omega_c t)$$

Equation (3.13) can be compared to the desired error-free RF output of equation (3.4). If the phase error at the I/Q input were to be adjusted so that the equation $\kappa = -\lambda$ is satisfied in equation (3.13), the following is noted:

- The desired cosine and sine products match in amplitude, because $\cos(-a) = \cos(a)$.
- The spurious component disappears completely, because $\sin(-a) = -\sin(a)$.
- The RF signal amplitude is attenuated by the cosine of the phase error.

It is therefore shown to be possible to compensate for quadrature phase error. The quadrature baseband signals and the quadrature carrier signals must have the same phase error. This condition is only valid when sinusoidal signals are used as input.

The same technique as before will be used to determine if the same is true for a single sideband rectangular wave. These waves will be constructed with a number of sinusoidal signals. The rectangular waves will be approximated by only the first two sinusoidal terms of equations (3.6) and (3.7). Assume that a quadrature phase error of κ radians occurs at the in-phase input, $I(t)$. The channel signals with phase deviation is defined in equation (3.14).

$$\begin{aligned} I(t) &= 0.6366 A \cos(\omega_d t + \kappa) - 0.2122 A \cos(3\omega_d t + \kappa) \\ Q(t) &= 0.6366 A \sin(\omega_d t) + 0.2122 A \sin(3\omega_d t) \end{aligned} \quad (3.14)$$

Also - the quadrature mixer has a phase inaccuracy of λ radians at the quadrature output, $Q(t)$. The resultant RF signal is shown in equation (3.15).

$$\begin{aligned}
y(t) &= [0.6366 A \cos(\varpi_d t + \kappa) - 0.2122 A \cos(3\varpi_d t + \kappa)] \cos(\varpi_c t) \\
&\quad + [0.6366 A \sin(\varpi_d t) + 0.2122 A \sin(3\varpi_d t)] \sin(\varpi_c t + \lambda) \\
&= 0.6366 A \cos(\kappa) \cos(\varpi_d t) \cos(\varpi_c t) - 0.6366 A \sin(\kappa) \sin(\varpi_d t) \cos(\varpi_c t) \\
&\quad + 0.6366 A \cos(\lambda) \sin(\varpi_d t) \sin(\varpi_c t) + 0.6366 A \sin(\lambda) \sin(\varpi_d t) \cos(\varpi_c t) \\
&\quad - 0.2122 A \cos(\kappa) \cos(3\varpi_d t) \cos(\varpi_c t) + 0.2122 A \sin(\kappa) \sin(3\varpi_d t) \cos(\varpi_c t) \\
&\quad + 0.2122 A \cos(\lambda) \sin(3\varpi_d t) \sin(\varpi_c t) + 0.2122 A \sin(\lambda) \sin(3\varpi_d t) \cos(\varpi_c t) \\
&= [0.6366 A \cos(\kappa)] \cos(\varpi_d t) \cos(\varpi_c t) \\
&\quad + [0.6366 A \sin(\lambda)] \sin(\varpi_d t) \sin(\varpi_c t) \\
&\quad + 0.6366 A [\sin(\lambda) - \sin(\kappa)] \sin(\varpi_d t) \cos(\varpi_c t) \\
&\quad - [0.2122 A \cos(\kappa)] \cos(3\varpi_d t) \cos(\varpi_c t) \\
&\quad + [0.2122 A \cos(\lambda)] \sin(3\varpi_d t) \sin(\varpi_c t) \\
&\quad + 0.2122 A [\sin(\kappa) + \sin(\lambda)] \sin(3\varpi_d t) \cos(\varpi_c t)
\end{aligned} \tag{3.15}$$

In order to get rid of all spurious signals, both entities of equation (3.16) must be satisfied.

$$\begin{array}{ccc}
\text{for } \varpi_d : & \text{and} & \text{for } 3\varpi_d : \\
\sin(\lambda) = \sin(\kappa) & & \sin(\lambda) = -\sin(\kappa)
\end{array} \tag{3.16}$$

It is possible to get rid of one spurious signal at a time, but impossible to get rid of both spurious signals. It is therefore shown to be impossible to compensate for quadrature phase error for a rectangular wave.

3.3.2. Random Data

Channel Phase Delay

The time delay of the input Q channel is varied with respect to the I channel before modulation. The influence of this delay on the state space and eye diagrams is shown in Figure 22.

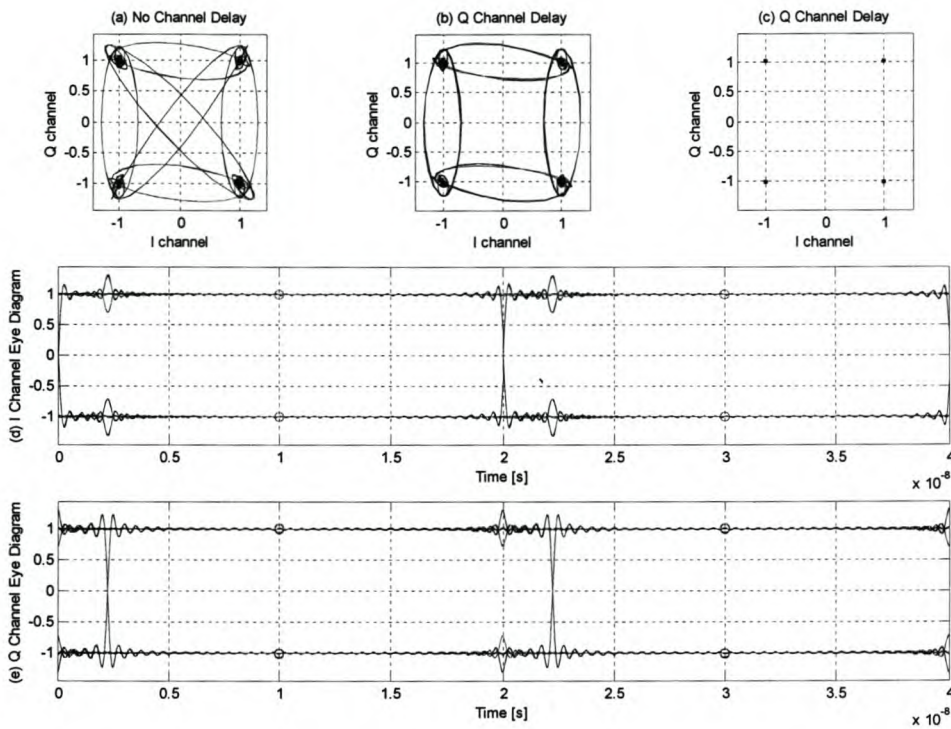


Figure 22 Influence of Channel Delay on State Space

Figure 22(a) shows the continuous state space of a modulator with no distortion. As seen in the eye diagram of Figure 22(d) and (e), for a modulator with wide bandwidth, the time spend between symbol positions is very little, thus the time spend between symbol positions in (a) is also very small. If the channels are aligned as in (a), the signal may jump to any symbol position, causing the cross in a box figure. If the channels is not aligned, it is impossible for both channels to change their state simultaneously. As shown in Figure 22(a), for any phase ambiguity, a simultaneous change of both channel states will cause a cross shape. Because this is not possible for a system with channel delay, only a box shape is visible in the continuous state space, as shown in Figure 22 (b).

As indicated in Figure 22(d) by a circle, the symbol sampling occurs exactly between two symbol changes. If the channel delay does not exceed the half- symbol mark, the sampled state space will not deform and no error will occur for a system with infinite bandwidth. This is shown in Figure 22(c). The probability of error will

increase for a system with a combination of channel delay and limited channel bandwidth.

Oscillator Phase Delay

The phase error in the modulator and demodulator are varied. The influence of this variation on the state space is shown in Figure 23.

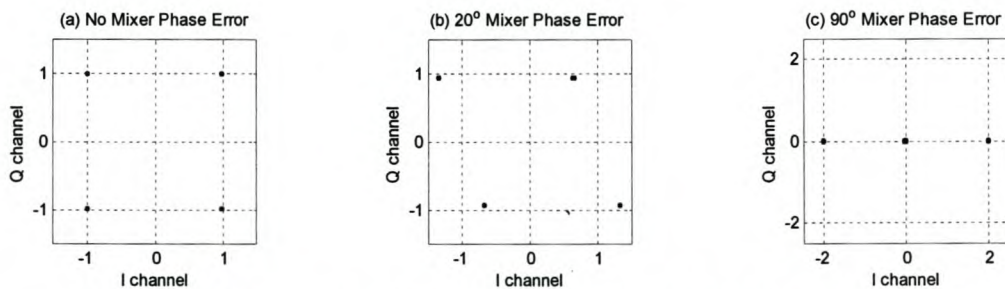


Figure 23 Influence of Phase Distortion on the State Space

As shown in Figure 23 (b), a phase distortion of 10° in the modulator causes a skew distortion in the I direction, whereas the same phase distortion in the demodulator causes a skew distortion in the Q direction. As shown in Figure 23(c), the constellation collapses at phase error of $\pm 90^\circ$.

Since oscillator phase distortion and channel phase distortion do not cause the same error for random data, it is the only non-ideality that compensation is not possible for. Thus, the influence of oscillator phase distortion on the bit error rate is investigated in Figure 24.

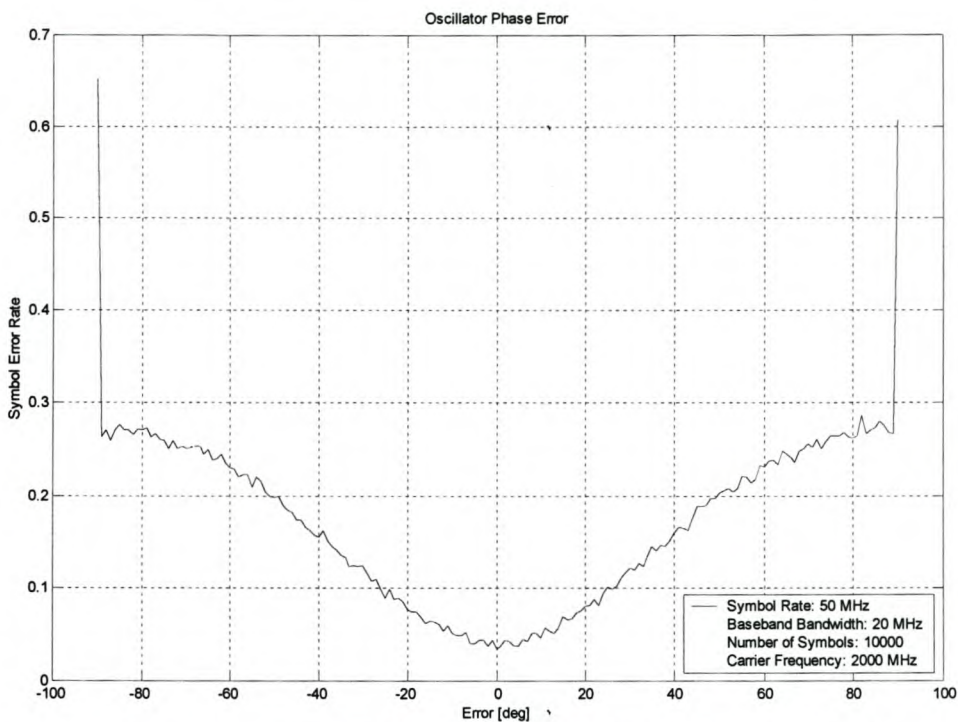


Figure 24 Influence of Oscillator Phase Distortion on the Bit Error Rate

Figure 24 confirms that the constellation collapses at $\pm 90^\circ$. Also, the error rate is relative low for a phase error of $\pm 10^\circ$.

3.4. Bandwidth

Filtering allows the transmitted bandwidth to be significantly reduced without losing the content of the digital data. This improves the spectral efficiency of the signal.

There are many different varieties of filtering. The most common are: raised cosine, square-root raised cosine and gaussian filters

Any fast transition in a signal, whether it is amplitude, phase, or frequency, will require a wide occupied bandwidth. Any technique that helps to slow down these transitions will narrow the occupied bandwidth. Filtering serves to smooth these transitions (in I and Q). Filtering reduces interference because it reduces the tendency of one signal or one transmitter to interfere with another on a nearby

frequency. On the receiver end, reduced bandwidth improves sensitivity because more noise and interference are rejected.

Some tradeoffs must be made. One is that some types of filtering cause the trajectory of the signal (the path of transitions between the states) to overshoot in many cases. This overshoot can occur in certain types of filters such as Nyquist. This overshoot path represents carrier power and phase. Carrier power cannot be clipped or limited (to reduce or eliminate the overshoot) without causing the spectrum to spread out again. Since narrowing the spectral occupancy was the reason the filtering was inserted in the first place, it becomes a very fine balancing act [1].

Filtering can also create Intersymbol Interference (ISI) [33]. This occurs when the signal is filtered enough so that the symbols blur together and each symbol affects those around it. This is determined by the time domain response or impulse response of the filter.

3.4.1. Filter Bandwidth Parameter Alpha

The sharpness of a raised cosine filter is described by alpha (α). Alpha gives a direct measure of the occupied RF bandwidth of the system and is shown in equation (3.17).

$$\text{Occupied RF Bandwidth} = \text{Symbol Rate}(1 + \alpha) \quad (3.17)$$

The filter response for different values of alpha is shown in Figure 25 [1].

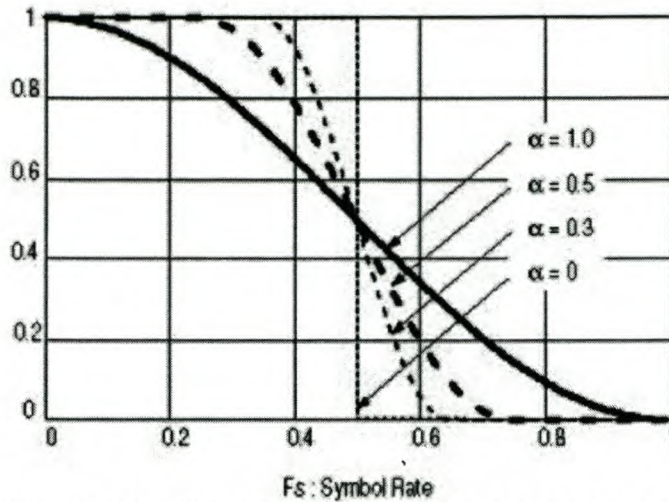


Figure 25 Filter Bandwidth Parameter Alpha

If the filter had a perfect (brick wall) characteristic with sharp transitions and an alpha of zero, the occupied bandwidth would be equal to the symbol rate, but this is not practical. An alpha of zero is impossible to implement. Alpha is sometimes called the *excess bandwidth factor* as it indicates the amount of occupied bandwidth that will be required in excess of the effective bandwidth (from equation (3.17) it is equal to the symbol rate).

At the other extreme, take a broader filter with an alpha of one, which is easier to implement. An alpha of one uses twice as much bandwidth as an alpha of zero. In practice, it is possible to implement an alpha below 0.2 and make a good, compact, practical system. Typical values range from 0.35 to 0.5, though some video systems use an alpha as low as 0.11 [1].

3.4.2. Filter Bandwidth Effects

Different filter bandwidths have different effects on the QPSK signal. The state space of a signal, filtered by a rectangular filter with different bandwidths, is shown in Figure 26.

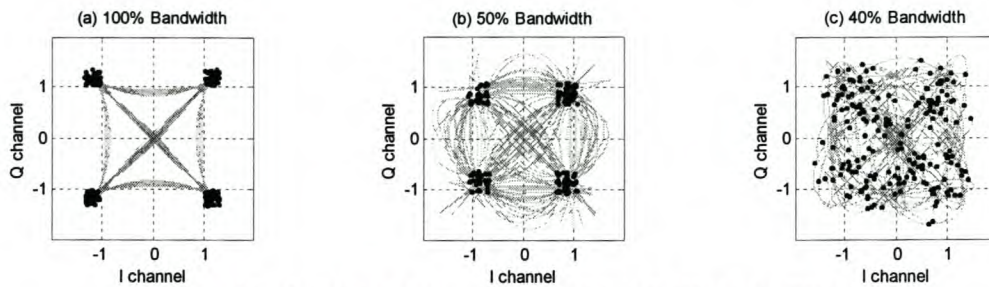


Figure 26 State space, Filtered by Different Filters

Figure 26(a) shows the state space of a signal filter with a rectangular filter with baseband bandwidth equal to the symbol rate, the transitions between states are almost instantaneous. No filtering means an alpha of infinity.

Figure 26(b) shows the state space of a signal with RF bandwidth equal to the symbol rate¹. The symbol grouping is still very good.

Figure 26(c) shows the signal, filtered by a rectangular filter with a baseband bandwidth of 40% the symbol rate. The error rate increases as the bandwidth decreases.

As was mentioned before, different filter bandwidths also affect the transmitted power. In the case of the unfiltered signal, with an alpha of infinity, the maximum, or peak power, of the carrier is equal to the nominal power at the symbol states. No extra power is required due to the filtering.

If an alpha of 1.0 is used, the transitions between the states are more gradual than for an alpha of infinity. Less power is needed to handle those transitions. Using an alpha of 0.5, the transmitted bandwidth decreases from the symbol rate to 0.75 times the symbol rate. This results in a 25% improvement in occupied bandwidth. The smaller alpha takes more peak power because of the overshoot in the filter's step

¹ This bandwidth is also the effective bandwidth of a QPSK modulated signal

response. This produces trajectories which loop beyond the outer limits of the constellation.

At an alpha of 0.2 there is a need for significant excess power beyond that needed to transmit the symbol values themselves [1].

3.5. Combined Effect

Thus far, only the individual effects of amplitude deviation, offset error, carrier leakthrough, phase inaccuracies and limited bandwidth have been considered. In a practical system, all these effects are compounded.

To minimize the effect of the combined inaccuracies, it is important to compensate for each inaccuracy separately. For example, to compensate for local oscillator leakthrough in the mixer, the offset in the I and Q channel must be adjusted so that the error signal has an amplitude equal to that of the leakthrough signal, and opposite in phase. If each inaccuracy is minimized as far as possible, the combined effect will also be small.

In order to determine the compounded effect of inaccuracies, a simulation tool has been created in Matlab. This allows you to specify the different inaccuracies and visually determine the effect on the system. The simulation tool will be discussed in more detail.

3.5.1. Simulation Tool

The QPSK Simulation Tool is created with Matlab². The user interface for the simulation tool is shown in Figure 27.

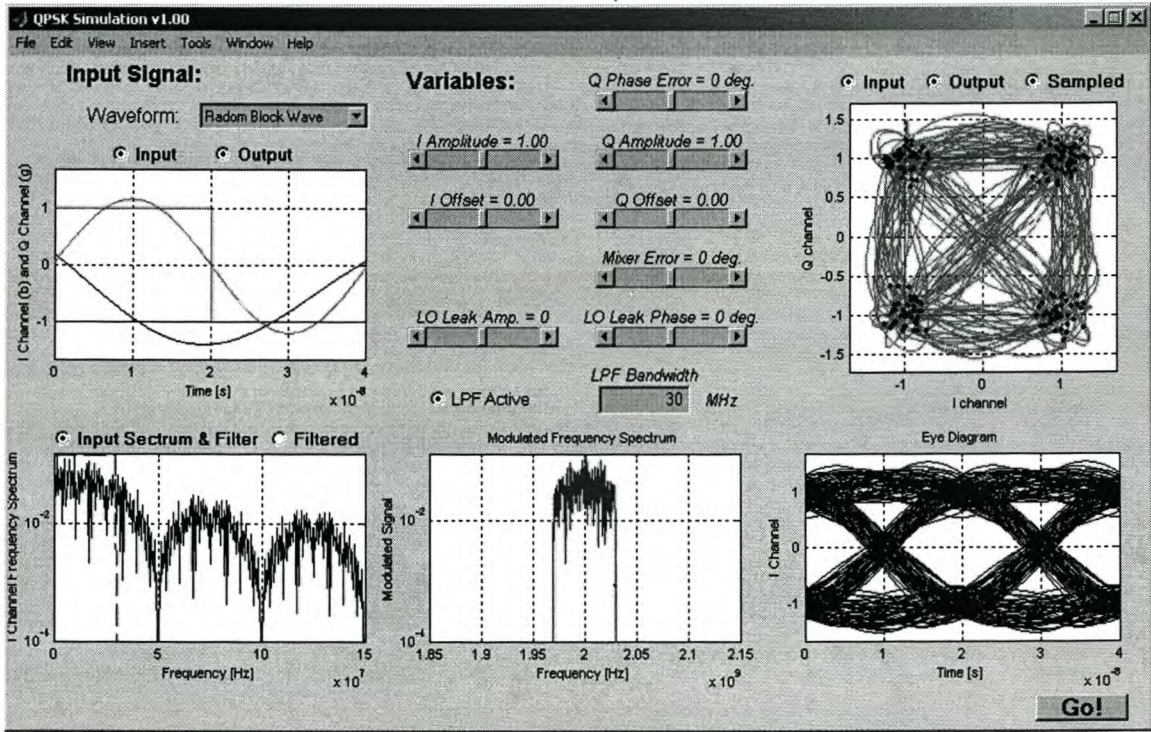


Figure 27 User Interface of Matlab Simulation Tool

The parameters that are fixed in the simulation are shown in Table 4.

Table 4 Parameters of QPSK Simulation Tool

Parameter	Value	Unit
Carrier Frequency	2	GHz
Symbol Rate	50	Mbps
Number of Symbols	200	

² Matlab 6.0.0.88 by MathWorks

The simulation's Matlab code structure is as shown in Figure 28. Each block represents a function. The complete source code is included in the accompanying CD.

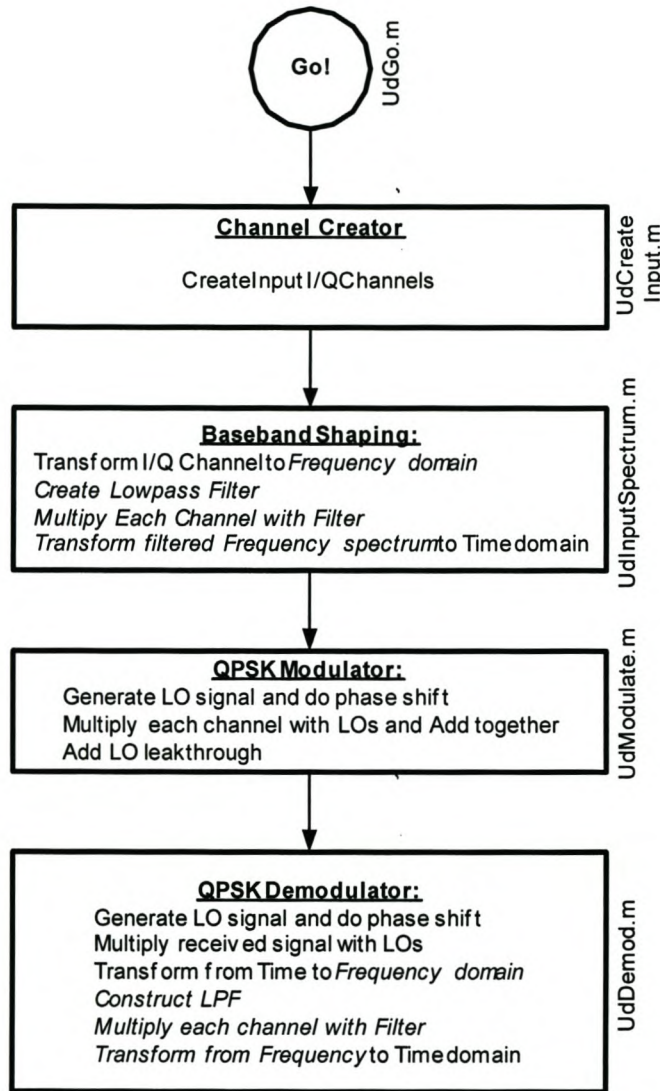


Figure 28 Code Structure of Simulation Tool

4. QPSK Transmitter

The transmitter is required to generate a QPSK signal. One of the transmitter's requirements is to compensate for the inaccuracies in the system. The transmitter must also be able to generate a number of QPSK modulated signals, each at a different frequency. This will be used to test the influence of adjacent signals on the performance of a system.

4.1. System Requirements

The receiver is proven to be the most complicated component in a communication system and thus needs to be located first. When a receiver is found, the transmitter can be designed. A DVB receiver from Sancy Electronics was chosen [28]. This choice will be discussed in chapter 5. The receiver's characteristics, relevant to the transmitter, are summarised as follows:

- Receiving Frequency Range: 950 MHz – 2.15 GHz
- Symbol Rate: 1 – 45 Msps

A transmitter will be designed to operate with the same specifications as the receiver.

4.2. System Overview

The transmitter consists of the following building blocks:

- Clock Generator
- Data Generator
- Driver
- Baseband Attenuator and Filter
- RF Synthesizer
- QPSK Modulator
- Combiner

The block diagram of the transmitter is shown in Figure 29. Note the four similar channels.

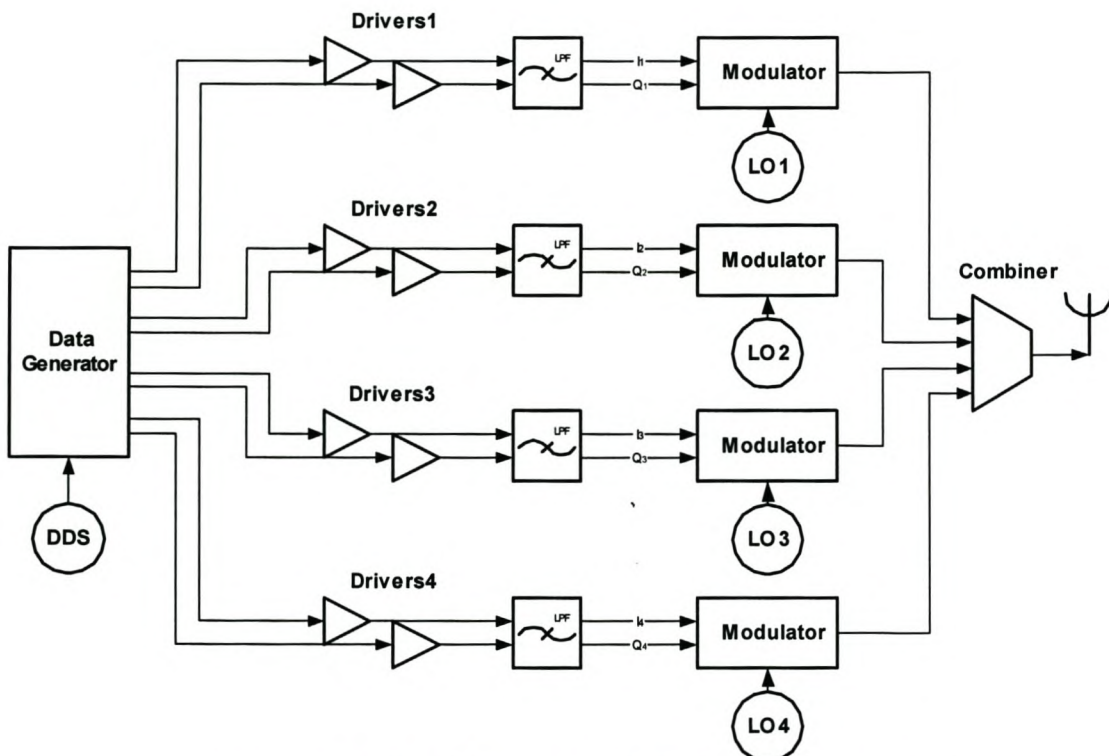


Figure 29 Block Diagram of QPSK Transmitter

The clock generator provides a digital clock for the data generator. This unit generates, encodes and splits up a data stream into four different I and Q channels. The four channels are identical, except for different local oscillator frequencies. The I and Q channel paths are also identical. Each are equipped with a buffer (or driver), attenuator and low-pass filter for baseband shaping. After modulation, all four channels are combined by a four port combiner.

A photograph of the custom-developed QPSK transmitter is shown in Figure 30. The different blocks are indicated on the photograph. Three of the four similar channel have been constructed.

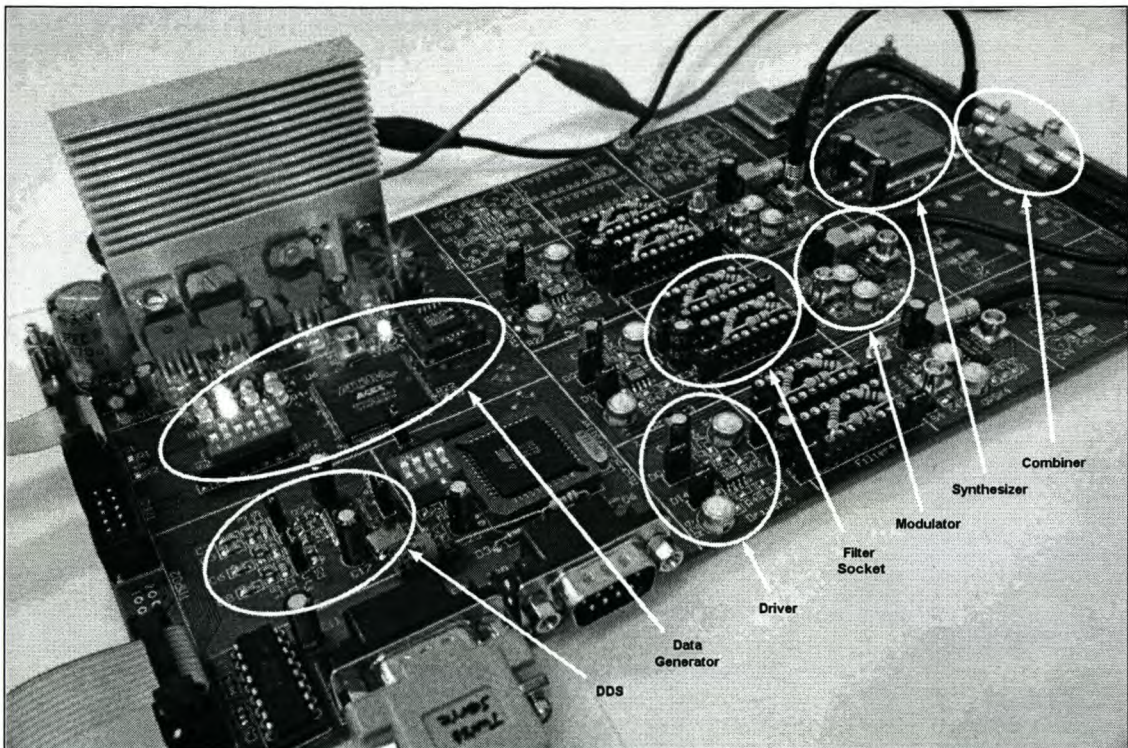


Figure 30 Photograph of QPSK Transmitter

The design and operation of each block will be better explained in the next section.

4.3. Clock Generator

The data generator requires a digital clock to operate. The data rate will be the same as the digital clock frequency. In order to test the effect of different bit rates, a variable clock is required. This is done by Analog Device's digital data synthesizer (DDS).³

When the DDS's registers is programmed, a sinusoidal signal between DC and 180 MHz is generated. Several spurious frequencies are also generated [6]. This is filtered by a 70 MHz elliptical low-pass filter. The filter schematic was obtained from the DDS's data sheets [6]. The filtered sinusoidal signal is fed back into an internal comparator, generating a rectangular signal. This signal is used as digital clock. A photograph of this section is shown in Figure 31.

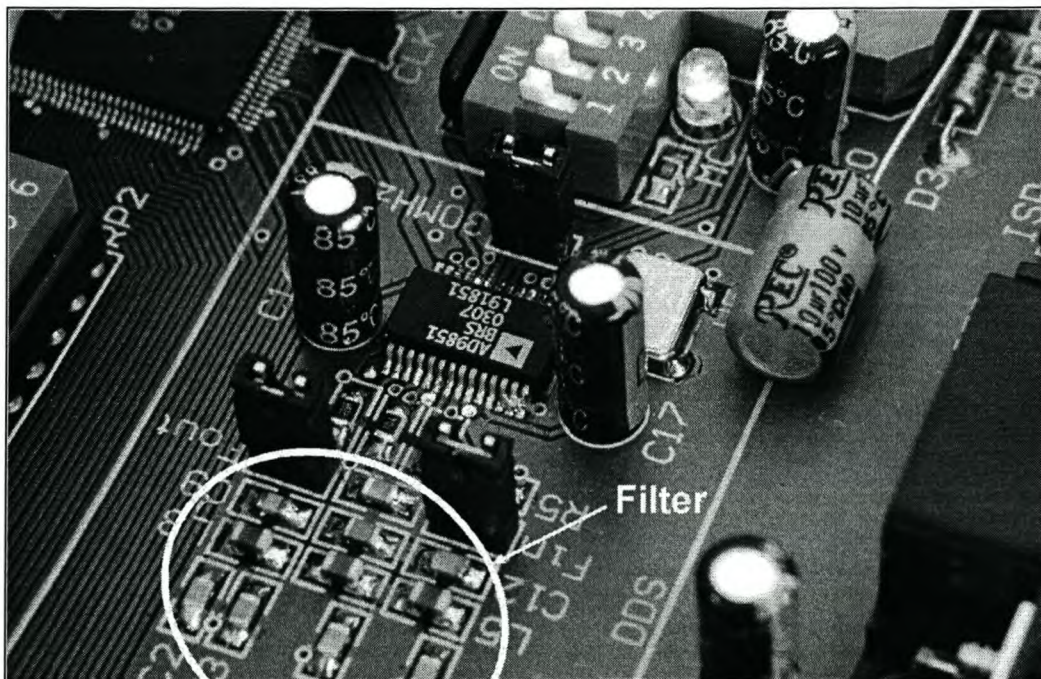


Figure 31 Photograph of Clock Generator Section

³ Part number: AD9851

The DDS is programmed serially by means of three wires: clock, data and enable. If a new frequency value is required, the computer generates the DDS's register value and transmits this to the microcontroller on the circuit board. The microcontroller, in return, programs the DDS's register.

4.4. Data Generator

The purpose of the data generator block is to generate several test data streams, or to select data from an external source. This is done for each of the four channels.

Each channel can be disabled through switch one to four of the DIP-Switch, S_1 . The *ON* position of each switch enables data generation. The corresponding yellow LED, $Y1$ to $Y4$, indicate the status of each channel.

A field programmable gate array (FPGA) was used to implement the above-mentioned functions. The block diagram of one channel is shown in Figure 32.

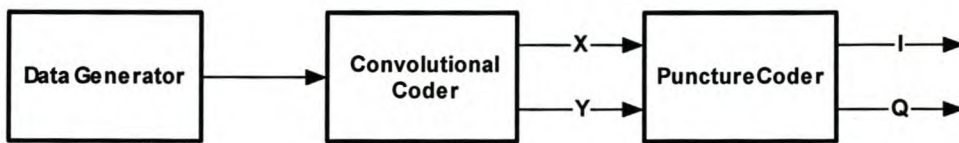


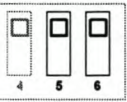
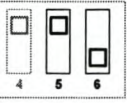
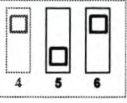
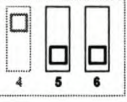
Figure 32 Block Diagram of Data Generator Section

The operation of each block in Figure 32 is explained in more detail in the next section.

4.4.1. Data Generator Block

The data generator block is able to generate three different encoded data streams: random data, a digital constant and an external data stream. A fourth mode exists and is slightly different than shown in Figure 32; a single sideband signal (SSB) is generated, but not encoded. The four modes are selected by switch five and six of DIP-Switch, S_1 . The switch configurations are summarized in Table 5.

Table 5 DIP Switch Positions for Data Generator Modes

DIP-Switch S_1	Data Generator mode
	Random Data
	Repeated Constant
	Single Sideband
	External Input

Each mode will be discussed in more detail:

Random Data

The data stream generated is true random. This is achieved by connecting the output from a *NOT* gate to its input. The *NOT* gate will toggle state as quick as possible. When the output is sampled every clock cycle, a random logic state is achieved. If this configuration is repeated, a different random value will result. This is because each gate is located on a different position on the FPGA, thus resulting in different time delays caused by different path lengths. To generate a true random state, a number of *NOT* configurations are combined with an *XOR* gate and then latched every clock cycle [17]. The FPGA's schematic diagram is shown in Figure 33.

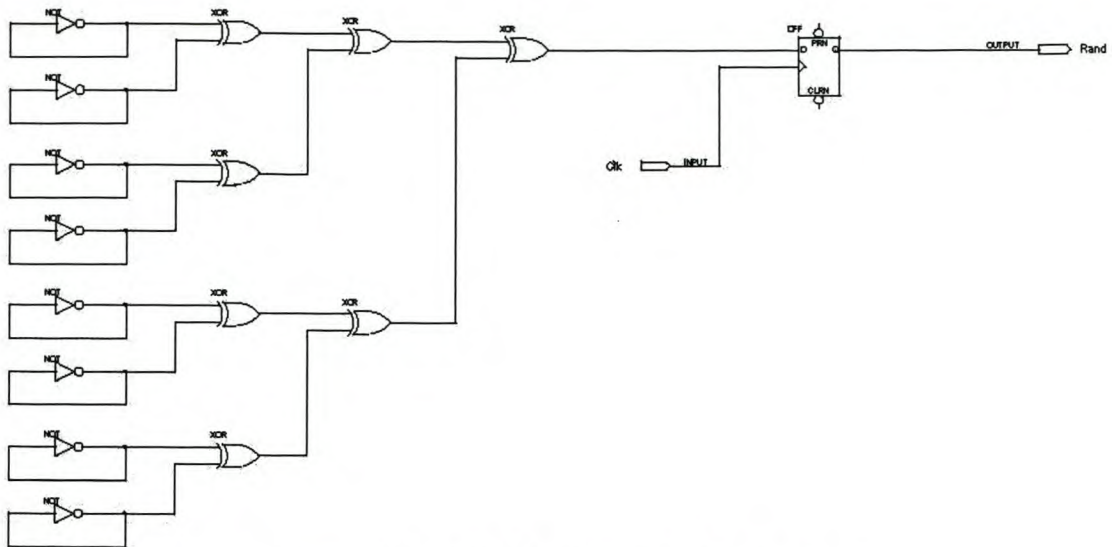


Figure 33 FPGA Schematic Diagram

Repeated Digital Constant

If this mode is selected, the output from the data generator is a continuous repetition of a serial data stream, with the most significant bit first. The data stream is randomly chosen and are digital $1101\ 0010\ 1001\ 1101_{Bin}$. This stream can easily be extended and varied.

Single Sideband Signal

The data generator generates a rectangular clock wave for the I channel. For the Q channel, this rectangular clock signal is delayed by 90° . This is done at a new symbol frequency at half the original frequency. For this mode no encoding is present. The FPGA's source code is included in the accompanying CD.

External Data Input

Data from an external source can be selected. This data is obtained through connector J14. The data are modulated and duplicated for each channel. This can be expanded on a later stage by dividing the data between the four channels.

4.4.2. Convolutional Encoding

The probability of error can be reduced by transmitting more bits than required to represent the information being sent, and convolving each bit with neighbouring bits so that if one transmitted bit got corrupted, enough information is carried by the neighbouring bits to estimate what the corrupted bit was. This approach of transforming a number of information bits into a larger number of transmitted bits is called channel coding, and the particular approach of convolving the bits to distribute the information is referred to as convolution coding. The ratio of information bits to transmitted bits is the code rate (less than 1) and the number of information bits over which the convolution takes place is the constraint length. [11, 14, 18].

For example, suppose a message is channel encoded, using a convolution code. Two bits are transmitted for every information bit (code rate = $\frac{1}{2}$) and a constraint length of three is used. The coder would send out 16 bits for every 8 bits of input, thus doubling the data rate. Each output pair would depend on the present and the past two input bits (constraint length of three).

Since information about each input bit is spread out over three transmitted bits, one can usually reconstruct the correct input, even with several transmission errors.

A block diagram of the convolution coder that was implemented is shown in Figure 34.

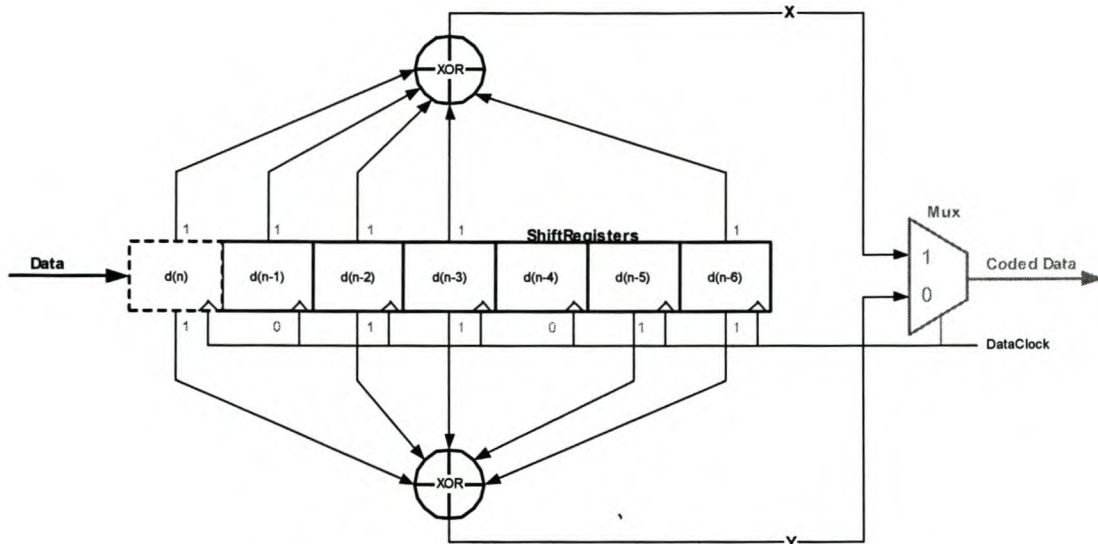


Figure 34 Convolutional Encoder

In Figure 34 the constraint length is seven and the code rate is $\frac{1}{2}$. This means there are two output bits for each input bit and each output pair would depend on the present and the past six input bits each. For BPSK modulation, the output bits are transmitted one after the other, two per clock cycle. This combining is done by the multiplexer. For a QPSK modulator, two data lines are required; an *I* and *Q* channel. The multiplexer is therefore omitted for this particular application.

The output of each channel is constructed by using a series of shift registers and exclusive-or gates. The present bit is represented by $d(n)$, where the previous bit is represented by $d(n-1)$ and so forth. The input connections to the exclusive or gates can be written as binary vectors, $G_X = [1\ 1\ 1\ 1\ 0\ 0\ 1]$ and $G_Y = [1\ 0\ 1\ 1\ 0\ 1\ 1]$, this are known as the generating vectors or generating polynomials for the code [11]. The output equations are shown in equation (4.1).

$$\begin{aligned} X &= d(n) \oplus d(n-1) \oplus d(n-2) \oplus d(n-3) \oplus d(n-6) \\ Y &= d(n) \oplus d(n-2) \oplus d(n-3) \oplus d(n-5) \oplus d(n-6) \end{aligned} \tag{4.1}$$

The convolutional encoder was implemented in FPGA. The schematic is shown in Appendix E.

4.4.3. Puncture Code

Each code rate has a different amount of bits generated. For example, the $2/3$ code rate has three output bits for every two input bits. A QPSK modulator requires only two inputs. Thus, a code called the puncture code is used to truncate the number of convolutional coded output to two. The scheme for the DVB's supported code rates is shown in Table 6 [11].

Table 6 Puncture Codes

Convolutional Code			Code Rates				
			$1/2$	$2/3$	$3/4$	$5/6$	$7/8$
K	G_x	G_y	P	P	P	P	P
7	171_8	133_8	X: 1 Y: 1 I = X_1 Q = Y_1	X: 1 0 Y: 1 1 I = X_1, Y_2, Y_3 Q = Y_1, X_3, Y_4	X: 1 0 1 Y: 1 1 0 I = X_1, Y_2 Q = Y_1, X_3	X: 1 0 1 0 1 Y: 1 1 0 1 0 I = X_1, Y_2, Y_4 Q = Y_1, X_3, X_5	X: 1 0 0 0 1 0 1 Y: 1 1 1 1 0 1 0 I = X_1, Y_2, Y_4, Y_6 Q = Y_1, Y_3, X_5, X_7
NOTE: 1 = transmitted bit 0 = non transmitted bit							

According to Table 6, for a code rate of $1/2$, the X and Y channels are mapped directly to the I and Q channels. This was implemented in FPGA code, as shown in Appendix E.

4.5. Driver

The function of the driver circuit is to provide a buffer between the FPGA and the load of the attenuator or filter. The circuit offers an adjustable gain in order to compensate for amplitude mismatch inside the modulator. A non-inverting operational amplifier circuit with variable gain has been implemented. The circuit schematic is shown in Appendix C.

When a physical circuit is constructed, unwanted inductance and capacitance are included. These components might be responsible for overshoot in a digital system. A 100Ω series resistor has been inserted before the driver (and one after the driver) in order to change the time constant of the circuit and thus decrease overshoot. The effect of this resistor has been examined for no load condition in Figure 35. The input and output signal, with- and without a series resistor, have been plotted. It is clear that the overshoot has been reduced.

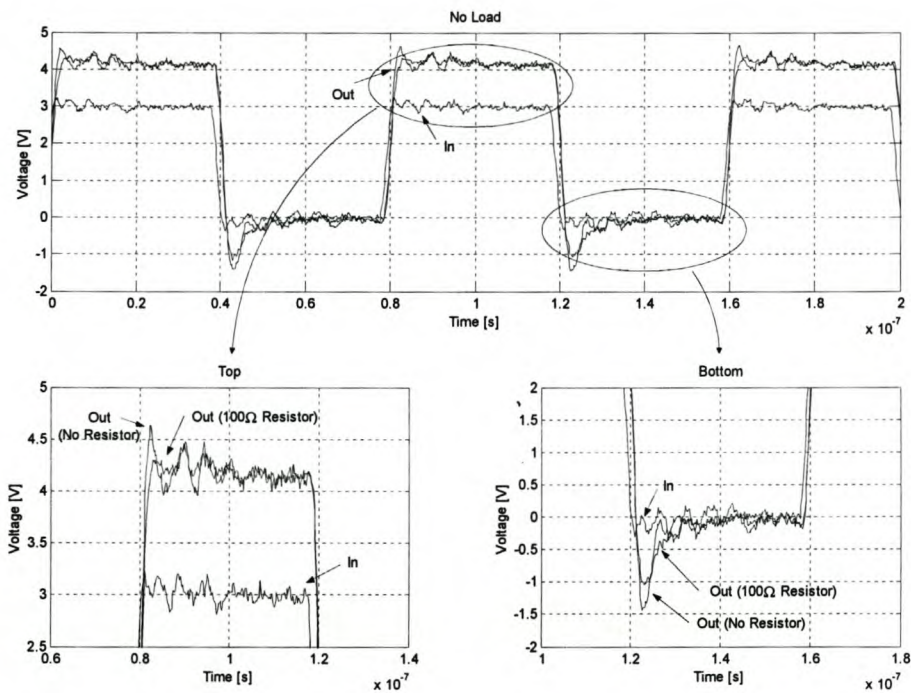


Figure 35 Influence of a Series Resistor on the Driver under No-Load Condition

Since a resistor is placed in the series with a load, voltage division will cause an attenuation of the input signal. This is illustrated in Figure 36 for various loads.

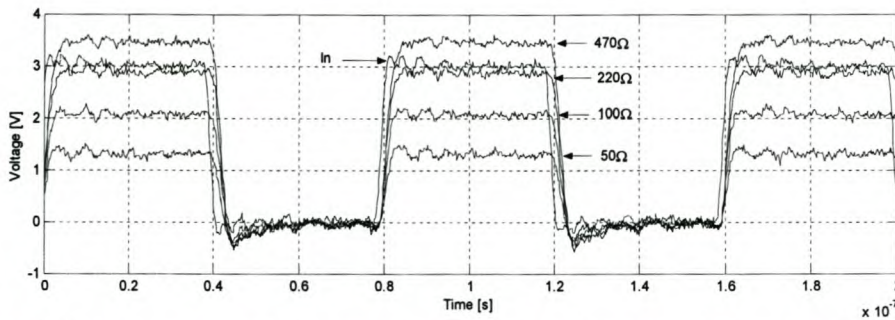


Figure 36 Influence of Series Resistor on Signal with Various Loads

When a 50 Ω load is present, the gain of the driver can be varied from 0.41 to 0.57, a voltage variation of almost 500 mV. When the gain is varied past a certain value, the driver operates in its non-linear region. This is illustrated in Figure 37.

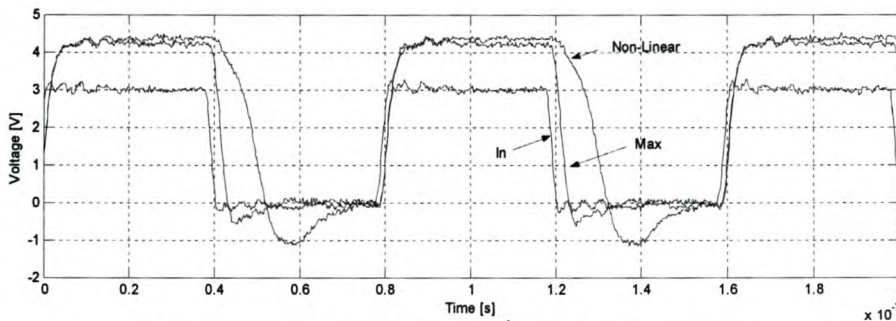


Figure 37 Driver Transformed Waveform

4.6. Baseband Attenuator

The modulator requires an input baseband signal of no more than $2 V_{pp}$ [26]. It is thus necessary to attenuate the signal from the driver. A 50 Ω π resistor network was used to attenuate the signal with 7.5 dB. The circuit schematic and Microwave Office⁴ S-parameter simulation are shown Figure 38 and Figure 39 respectively.

⁴ Microwave Office 2002, version 5.51

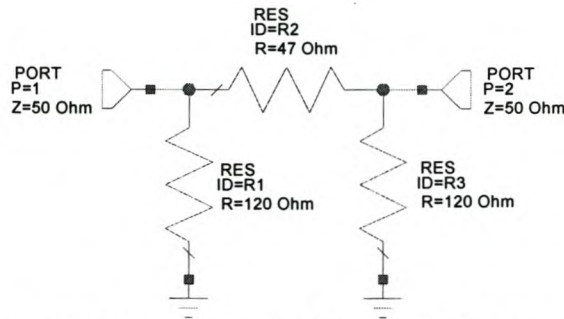


Figure 38 Attenuator Circuit Schematic

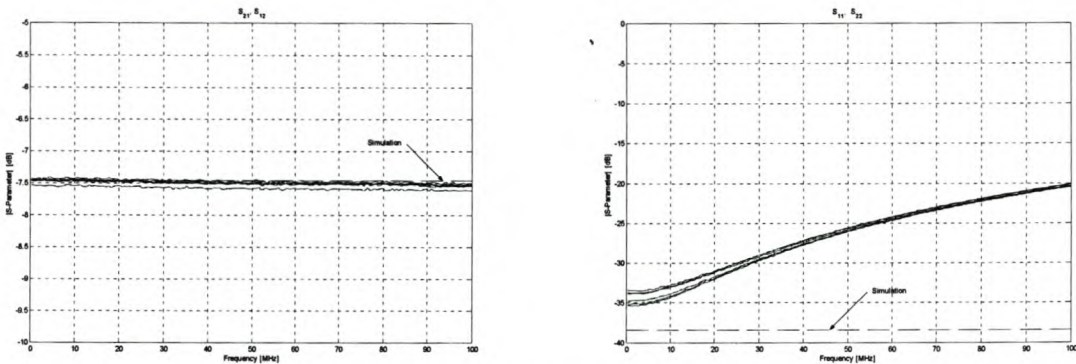


Figure 39 Simulated and Measured Attenuator S-Parameters

From Figure 39 it is clear that the attenuation is 7.46 dB and the input and output reflection coefficients are below -20 dB up to 100 MHz.

4.7. Baseband Filter

When a frequency band is allocated for transmission it is very important to transmit all the power, or as much as possible, in the allowed frequency band. Strong regulations exist on the power transmitted outside the frequency band. In order to shape the transmitted frequency spectrum, two options exist.

Band shaping can be done at high frequency by a bandpass filter, with centre frequency at the system carrier frequency. The design of this filter might be a tedious task because of the small percentage bandwidth and the high Q -factor required.

A better solution is to shape the baseband before modulation. The design of a low-pass filter at low frequency is much easier than a bandpass filter at high frequency. It is possible to design a high order filter with a high Q -factor. A drawback is that one filter is necessary for each I/Q channel, thus two similar filters for each modulation channel.

A fifth order Chebyshev filter configuration was chosen as first iteration because of the high Q -factor. The cutoff frequency was chosen at 25 MHz, right in the middle of the operating range of the receiver. A passband ripple of 1 dB was chosen in the filter synthesis. The filter synthesis was executed in Microwave Office⁵. The filter schematic diagram is shown in Figure 40.

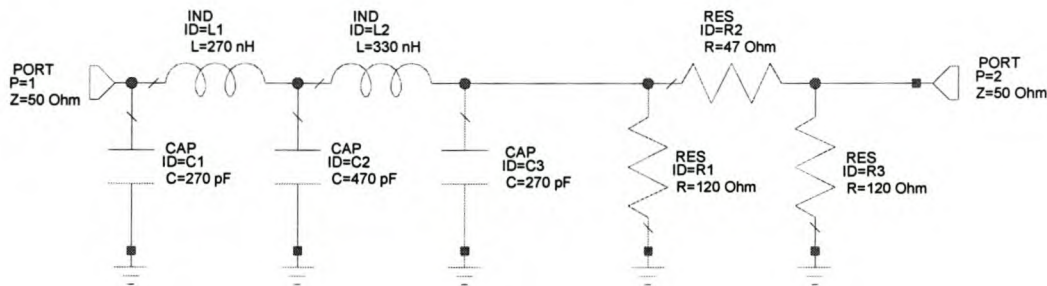


Figure 40 Schematic Diagram of 25 MHz Chebyshev Filter and Attenuator

In order to test the influence of a baseband filter on the performance of the system, the filter was made removable. If necessary, it is possible to omit the filter, or replace it with a different filter. Four similar filters are constructed on different

⁵ Microwave Office 2002, version 5.51

printed circuit boards, designed to fit in a DIP socket. A removable Chebyshev filter is shown in Figure 41(C).

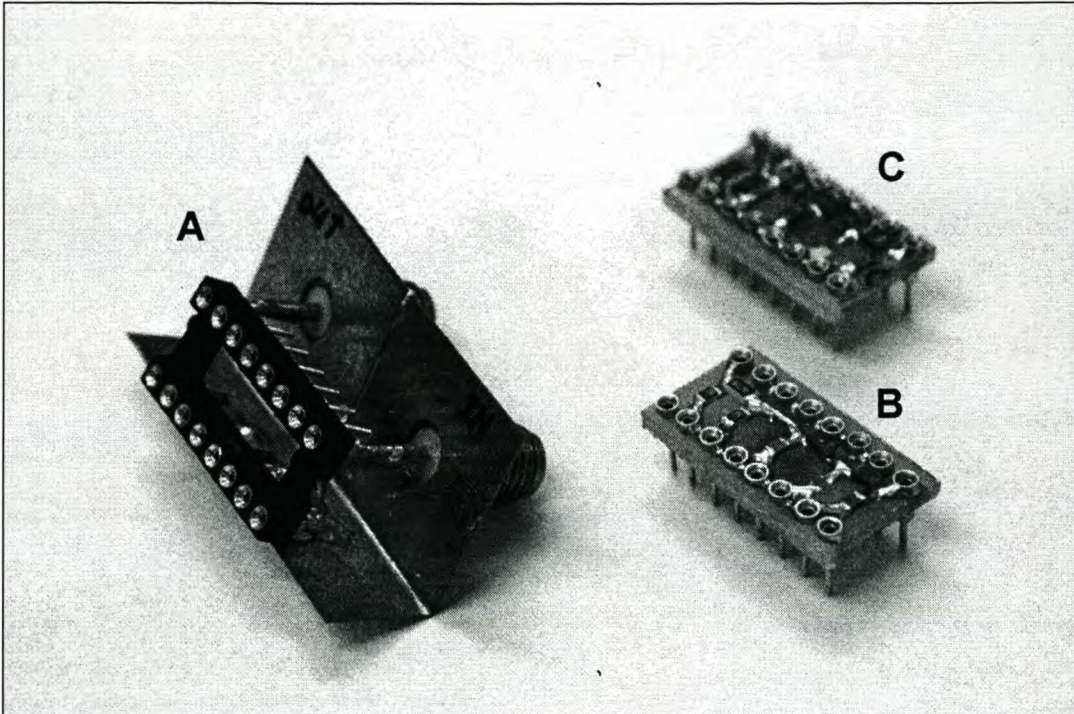


Figure 41 Photograph of Measurement Jig(A), Filter 1(B) and Filter 2(C)

It is necessary to use similar filters for all four channels in order to test the influence on the system. The measuring jig in Figure 41(A) was constructed to connect to a network analyzer⁶ in order to measure the S-parameters of each filter. The simulated and measured filter parameters for all four filters are plotted in Figure 42 and Figure 43.

⁶ HP85047A Vector Network Analyzer

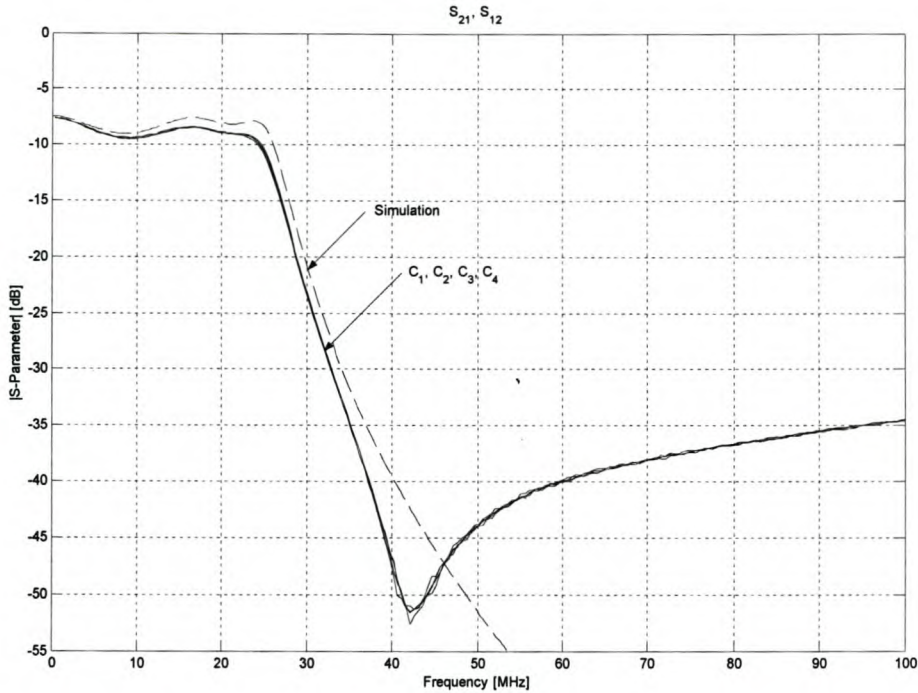


Figure 42 Simulated and Measured Forward S-Parameters of Chebyshev filter and Attenuator

In Figure 42 the measured and simulated S-parameters are almost alike. The deviation from the simulation might be caused by the additional inductance and capacitance added by the DIP socket. The cutoff frequency of the measured filters is slightly lower than simulated but all four filters are identical.

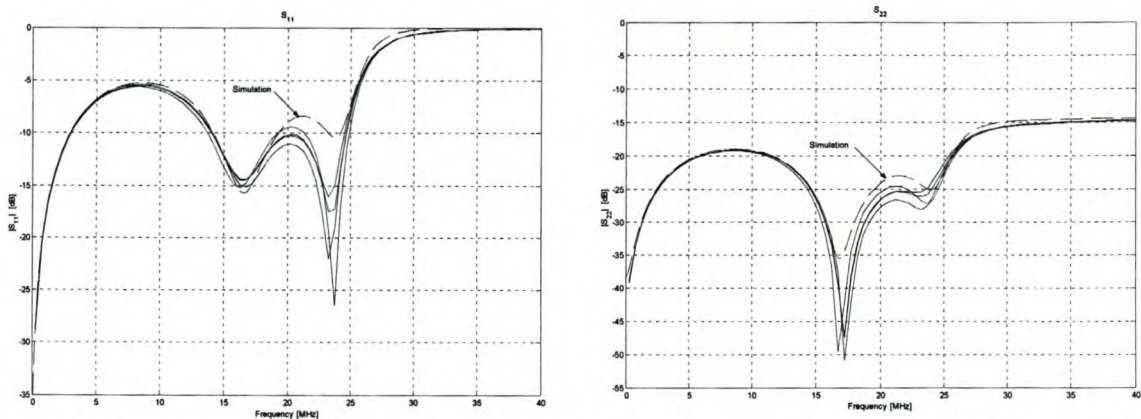


Figure 43 Simulated and Measured Reflection Coefficients of Chebyshev Filter and Attenuator

The input matching of all four filters is below -5 dB in the passband. Since the output matching is determined by the attenuator, a better matching of below -17 dB in the passband is measured.

A second filter was designed. The Bessel-Thomson filter type was chosen because of the flat phase response. This is ideal for digital signal shaping since the inter symbol interference is minimized.

Since an increase in the order of the filter does not increase the Q-factor much, a third order Bessel-Thomson filter was designed. The cutoff frequency is designed at 6 MHz. Thus a symbol rate of up to 12 Msps can be accommodated. The filter synthesis was executed in Microwave Office and the filter's schematic diagram is shown in Figure 44. Six similar filters were constructed and a photograph of such a filter is shown in Figure 41(B).

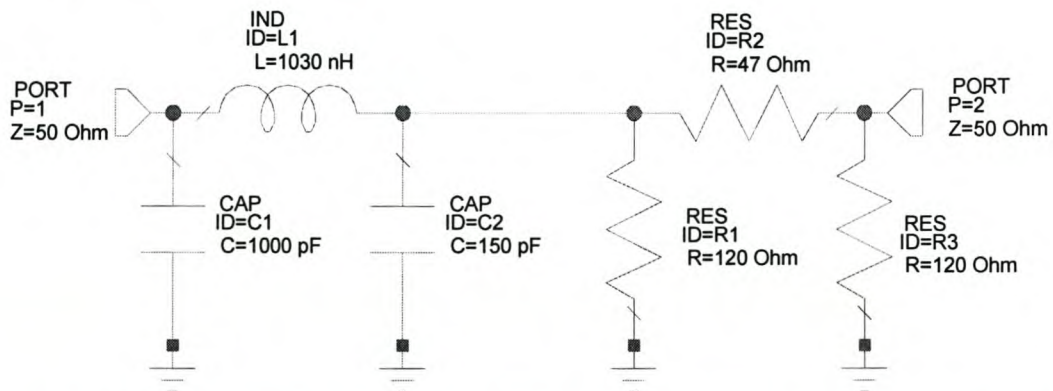


Figure 44 Schematic Diagram of Bessel-Thomson Filter and Attenuator

The simulated and measured filter parameters for all six filters are plotted in Figure 45 and Figure 46.

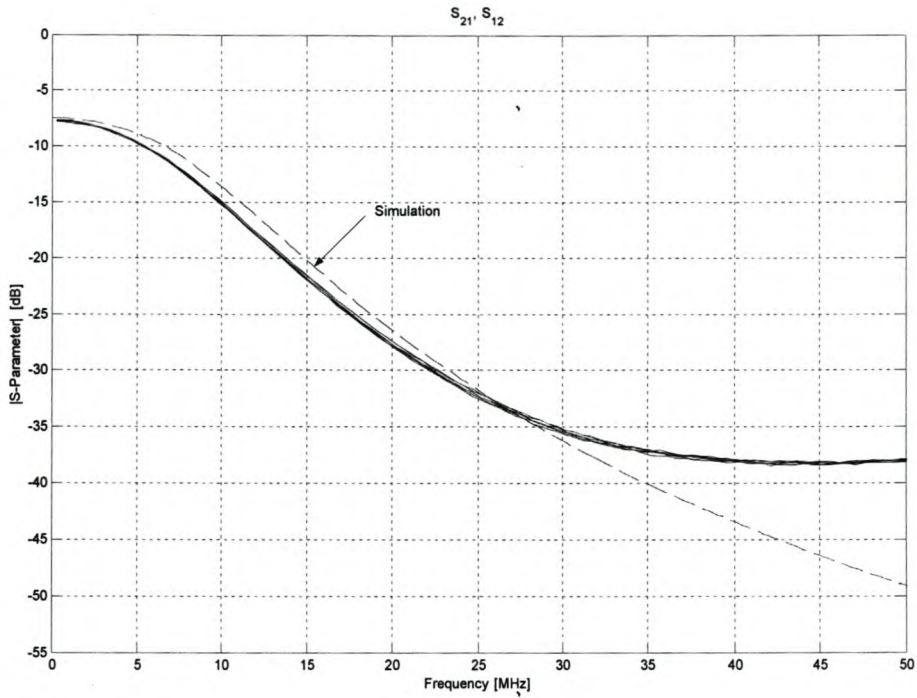


Figure 45 Simulated and Measured Forward S-Parameters of Chebyshev Filter and Attenuator

In Figure 45 the cutoff frequency of the measured filters is slightly lower than simulated but all six filters are identical.

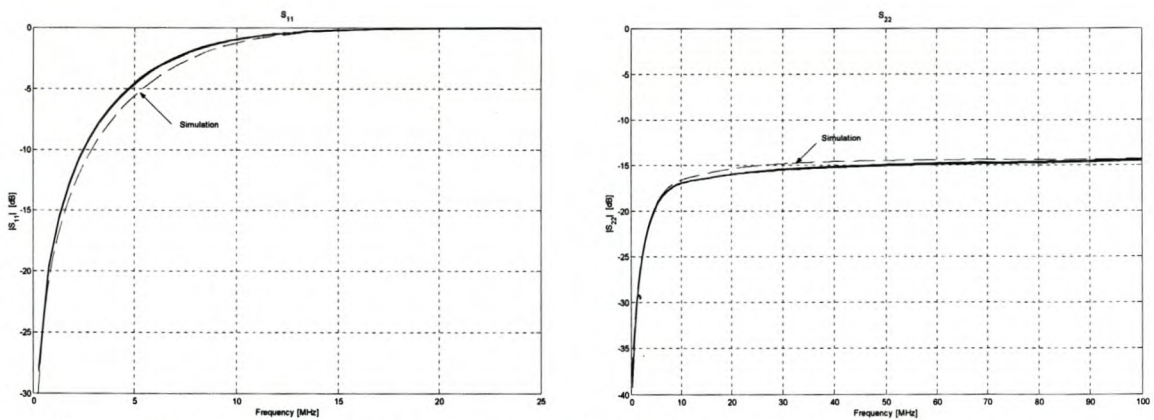


Figure 46 Simulated and Measured Reflection Coefficients of Chebyshev Filter and Attenuator

The input matching of all six filters is below -5 dB in the passband. Since the output matching is determined by the attenuator, a matching of below -17 dB in the passband is measured.

4.8. Baseband Spectrum

The baseband frequency spectrum of the I channel before modulation, is shown in Figure 47. The symbol rate is 25 Msps.

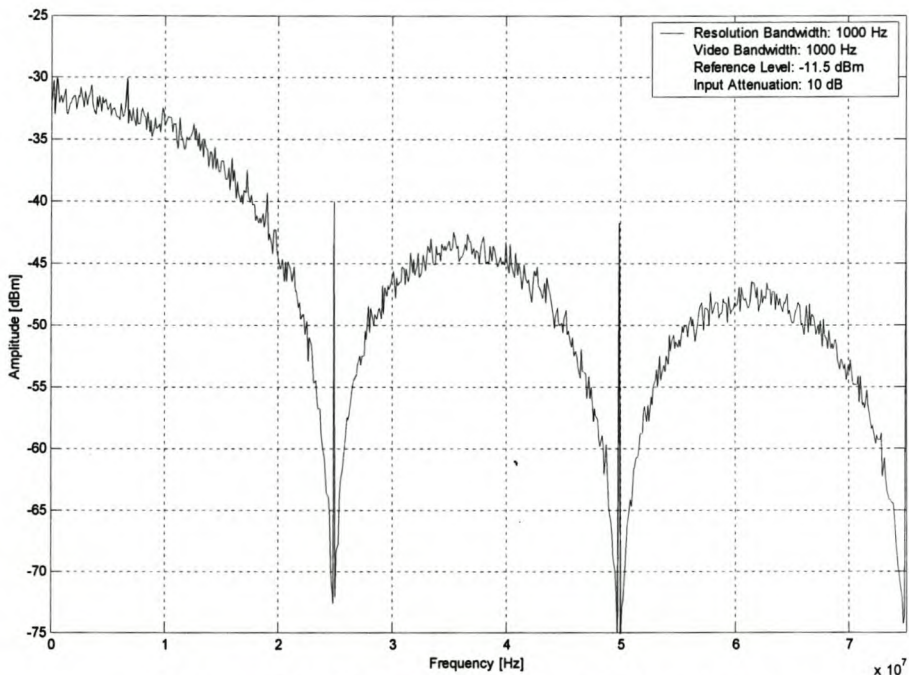


Figure 47 I Channel Baseband Spectrum

The frequency components present at multiples of 25 MHz are caused by leakthrough from the digital clock. It was noted that the amplitude of this components increased as the DDS's frequency increased.

4.9. Synthesizer

For QPSK modulation the baseband I/Q channel is modulated on a carrier frequency. In order to vary the carrier frequency, a frequency synthesizer by Synergy

was used⁷. The synthesizer has a frequency range of 1 GHz to 2 GHz, with a step size of 1 MHz [30].

The synthesizer is programmed serially by tree lines: clock, data and enable. If a new carrier frequency is required, the computer generates the synthesizer register values and transmits it to the microcontroller on the circuit board. The microcontroller programs the synthesizer's registers. The green LEDs (*G1* to *G4*) indicate if the respective synthesizer is locked to the correct frequency.

The frequency spectrum of the synthesizer programmed at 1.5 GHz, is shown in Figure 48.

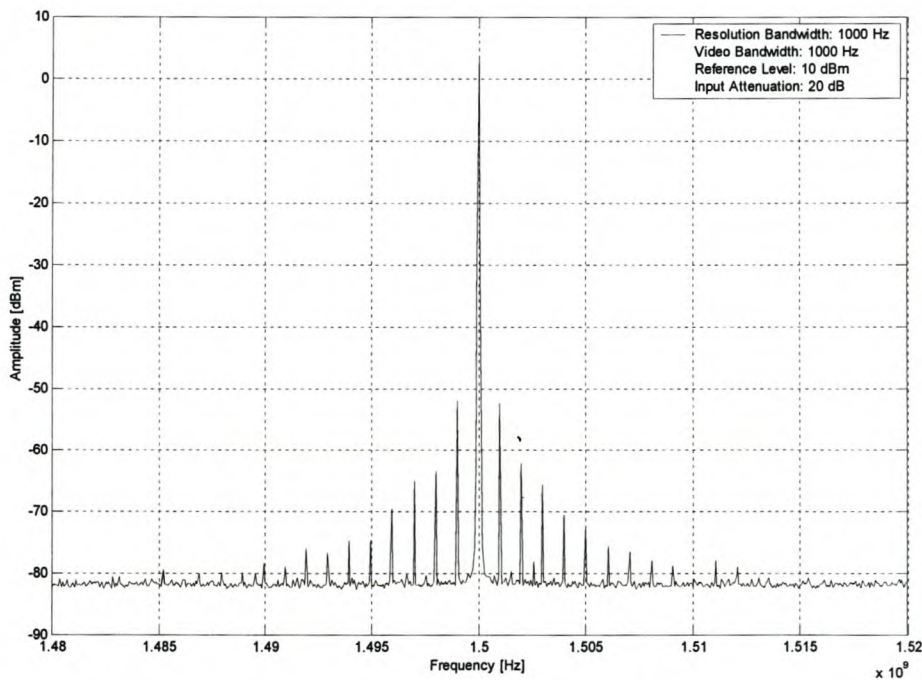


Figure 48 Synthesizer Frequency Spectrum

⁷ Part number: SPLH1000SB

Next to the required frequency at 1.5 GHz are spurious frequencies present, spaced 1MHz apart, equal to the step frequency. The peak power level of these spurious frequencies is 50 dB below the main frequency's peak power level.

When the frequency is varied, the peak power level is measured⁸. This is plotted in Figure 49.

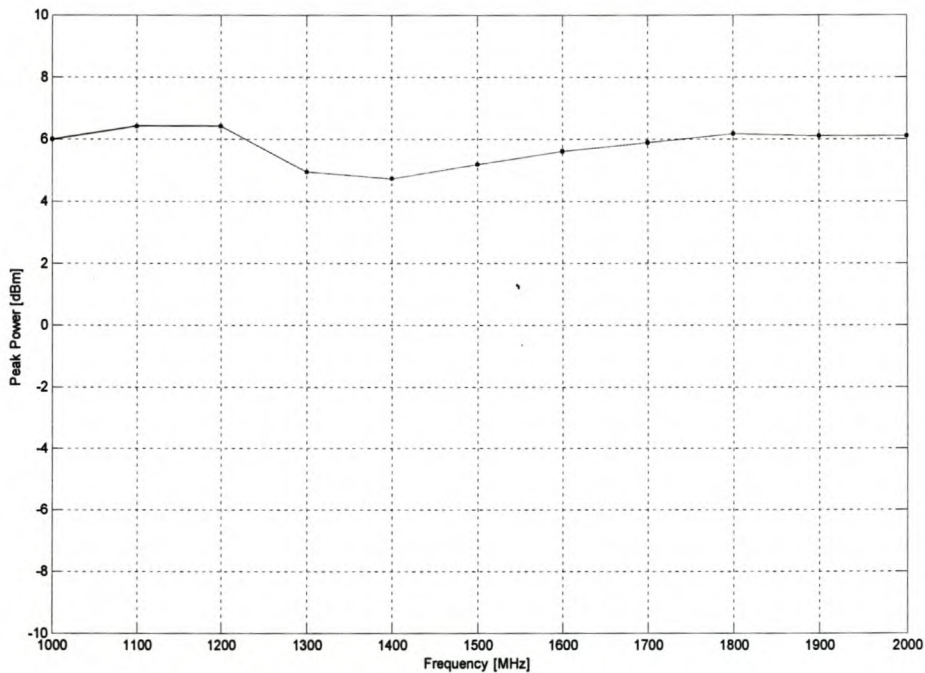


Figure 49 Synthesizer Peak Power

The synthesizer's peak power level is on the maximum power limit allowed by the QPSK modulator.

The frequency synthesizer is connected to the modulator with a *LMR100* coaxial cable and *MCX* connectors. The connectors are capable of supporting frequencies of up to 6 GHz [10].

⁸ The peak power level was measured with a WaveTek peak power meter model 8501A.

The modulated single sideband frequency spectrum is compared when an external local oscillator and the synthesizer is used. This is shown in Figure 50(a) and (b) respectively. The spectrum will be discussed in section 4.13.

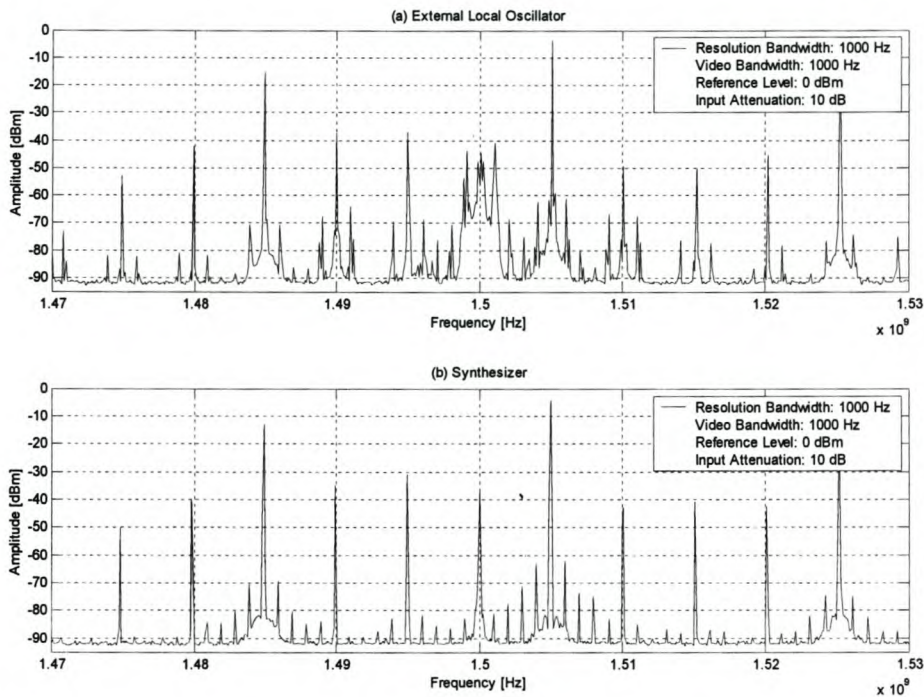


Figure 50 Single Sideband Frequency Spectrum where an External Oscillator is used and a Synthesizer

The synthesizer produced a cleaner spectrum than the external oscillator used⁹.

When the bit error rate was compared to a system where the synthesizer was replaced with an external local oscillator¹⁰, the external oscillator produced a better bit error rate. It is suspected that the performance of the synthesizer depends on the load driven. In order to determine if power is received from the modulator as load, a

⁹ Agilent E4401B 9kHz-1.5GHz Esa-E Series Spectrum Analyser

¹⁰ Rohde&Schwarz SML03 9kHz-3.3GHz Signal Generator

circulator¹¹ has been used to measure the received power. The measurement setup is shown in Figure 51.

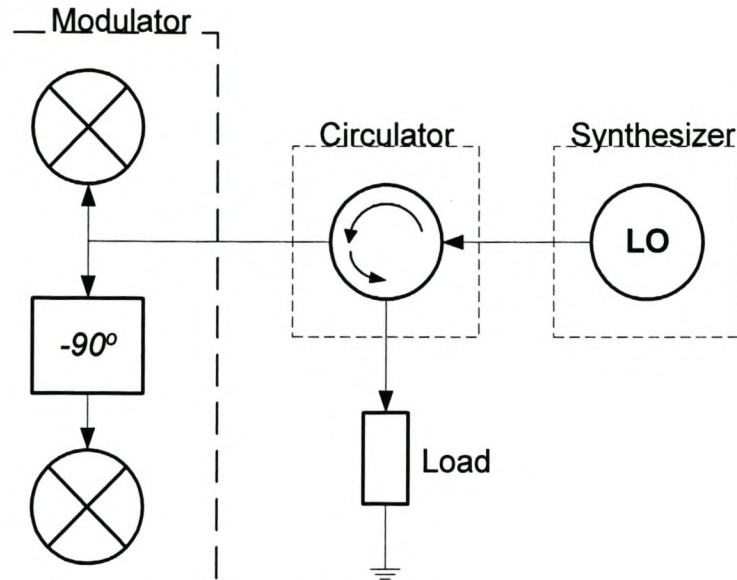


Figure 51 Circulator Setup

A single sideband signal was modulated by the modulator and the reflected signal captured by a spectrum analyzer. The modulated spectrum and spectrum of the received signal is shown in Figure 52.

¹¹ Return Loss Bridge RLB150x5 by Eagle

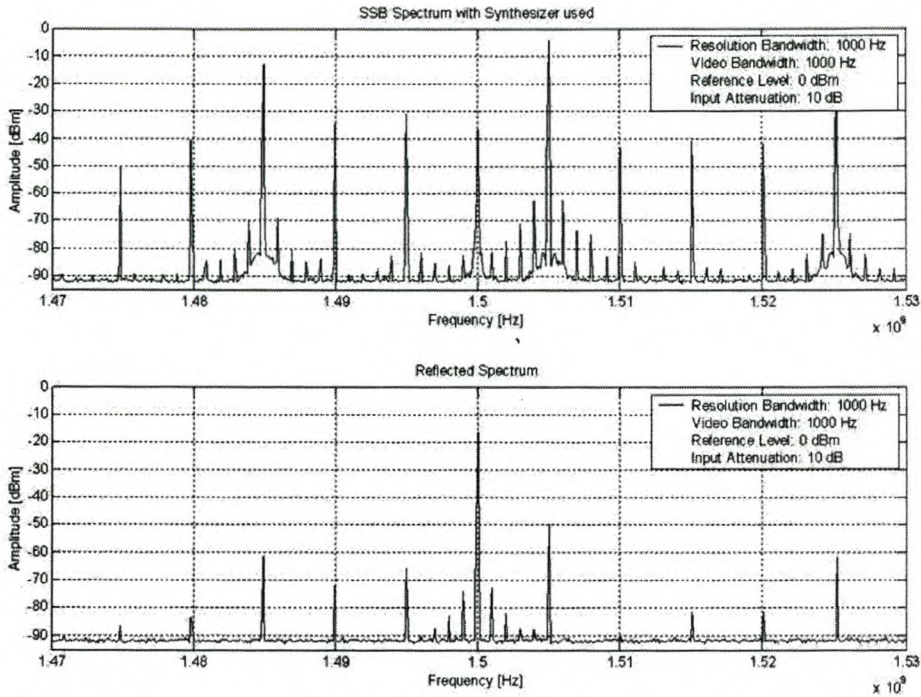


Figure 52 Reflected SSB Spectrum

It is clear that the synthesizer receives power from the modulator.

When random data is modulated, the reflected signal's frequency spectrum is shown in Figure 53.

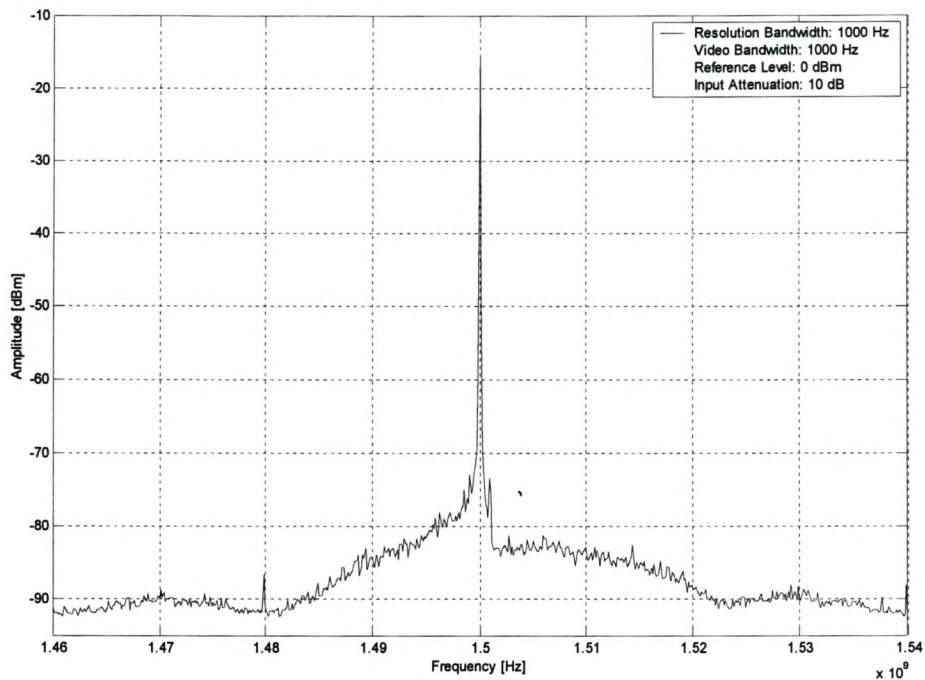


Figure 53 Reflected QPSK Spectrum

In order to improve the isolation between the synthesizer and the modulator, it is recommended that a circulator should be used. An attenuator would also increase this isolation but decrease the synthesizer's power level.

4.10. Modulator

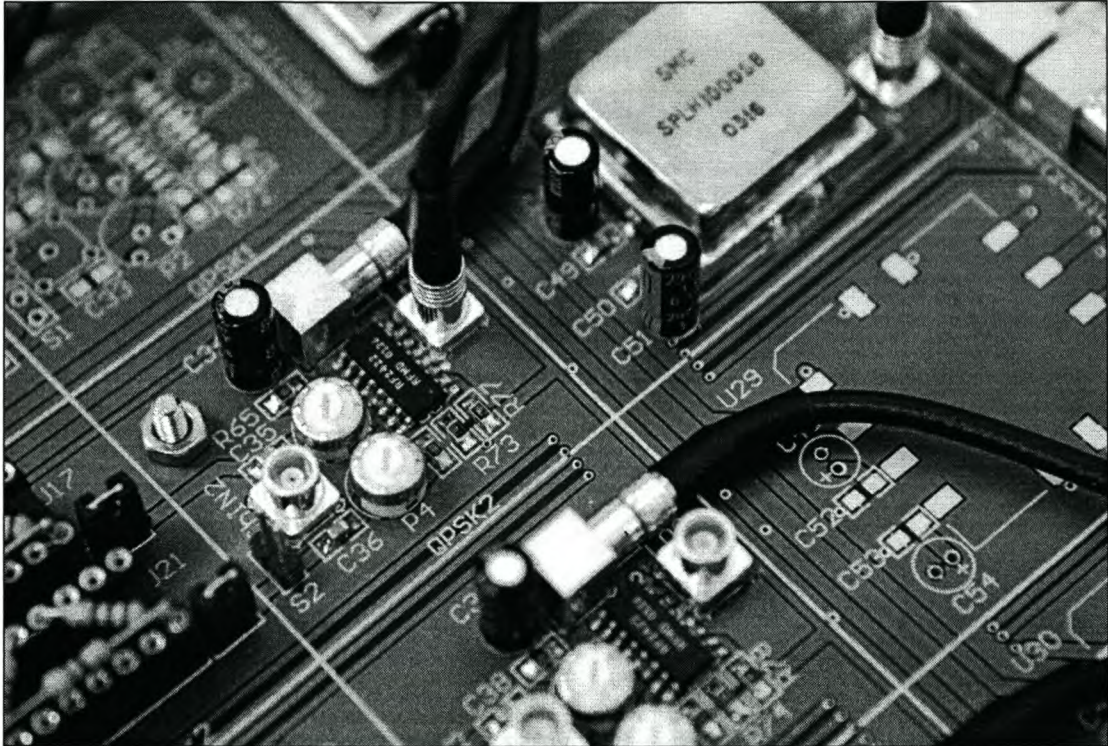


Figure 54 Photograph of QPSK Modulator

The modulation of data is done by a QPSK modulator by RF Micro Devices¹². Some of the specifications are summarized in Table 7 [26].

Table 7 RF2422 QPSK Modulator Specifications

Parameter	Specification	Unit
Carrier Frequency	800 – 2500	MHz
Input Frequency Fange	DC-250	MHz
Reference Voltage (V_{ref})	3	V
Maximum Modulation	$V_{ref} \pm 1$	V
Phase Error	3	°
Amplitude Error	0.2	dB
Input Resistance	30	k Ω
Output Impedance	50	Ω
Carrier Suppression	30	dB
Sideband Suppression	25	dB

¹² Model number: RF2422

The I and Q input signals of the modulator must be centred on the reference voltage, V_{ref} . In order to simulate the effect of a DC-offset in the I and Q channel, the DC is filtered by a capacitor and a bias network with a variable resistor used to add a variable offset. The circuit schematic and a photograph of modulator number 2 is shown in Figure 55 and Figure 54 respectively.

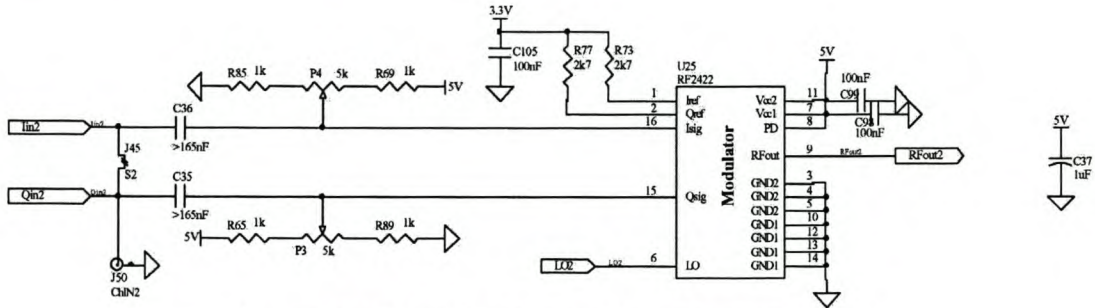


Figure 55 Circuit Schematic of Modulator 2

4.11. Combiner

When two or more modulators are used to generate several modulated signals, the output must be combined. This is done by a four channel combiner by Mini-Circuits¹³. The frequency range is from 1000 MHz to 2000 MHz [21].

The combiner's ports are defined as four input ports, numbered one to four and an output port, numbered five. A photograph of the combiner is shown in Figure 56.

¹³ Model number: SCA-4-20

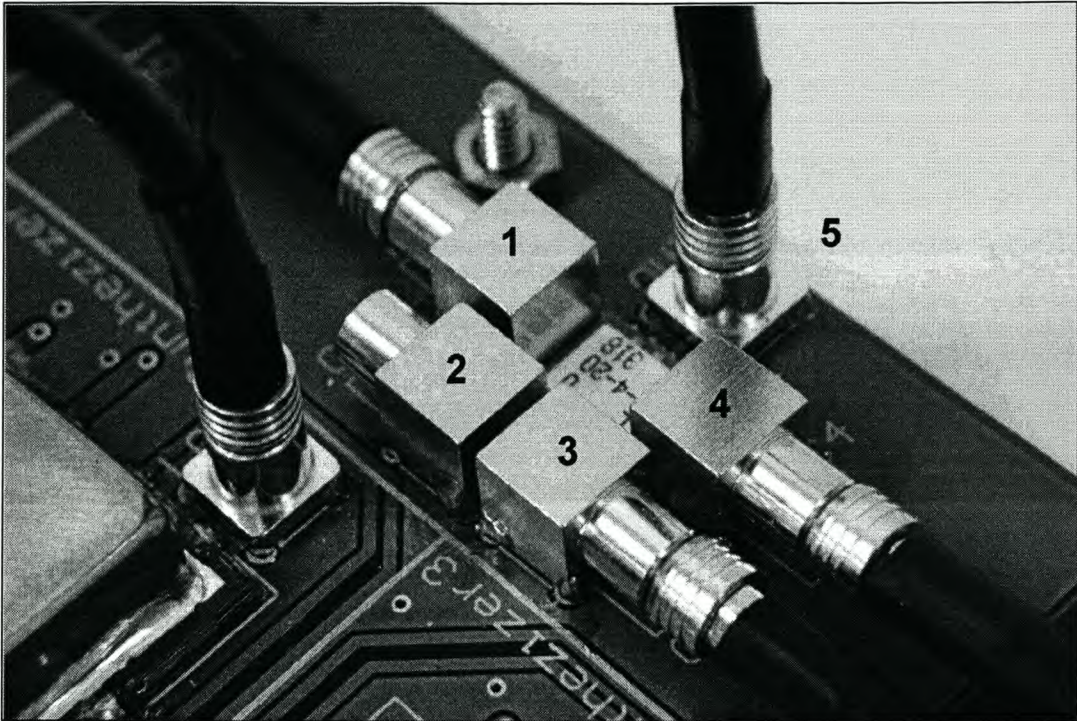


Figure 56 Photograph of Combiner

The combiner's forward and reverse S-parameters are plotted in Figure 57.

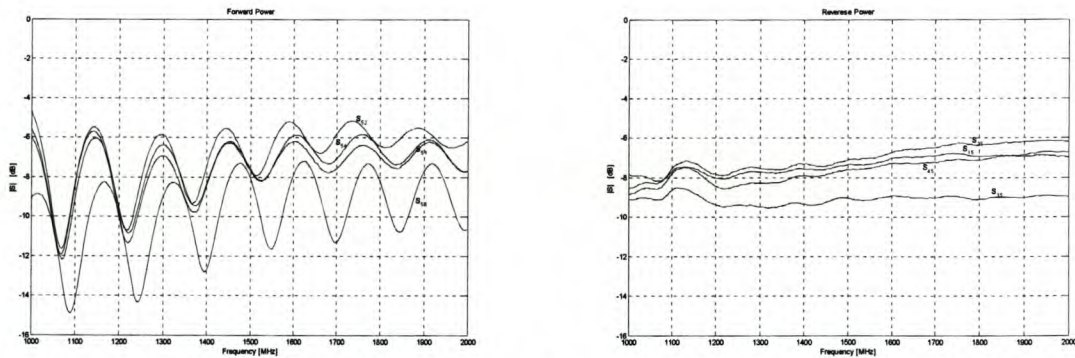


Figure 57 Forward S-Parameters

The power loss when a signal passes through the combiner is between 5 dB and 15 dB and between 6 dB and 10 dB when used as a splitter. The loss in port three is more than the other ports.

The reflection coefficients for each port are plotted in Figure 58.

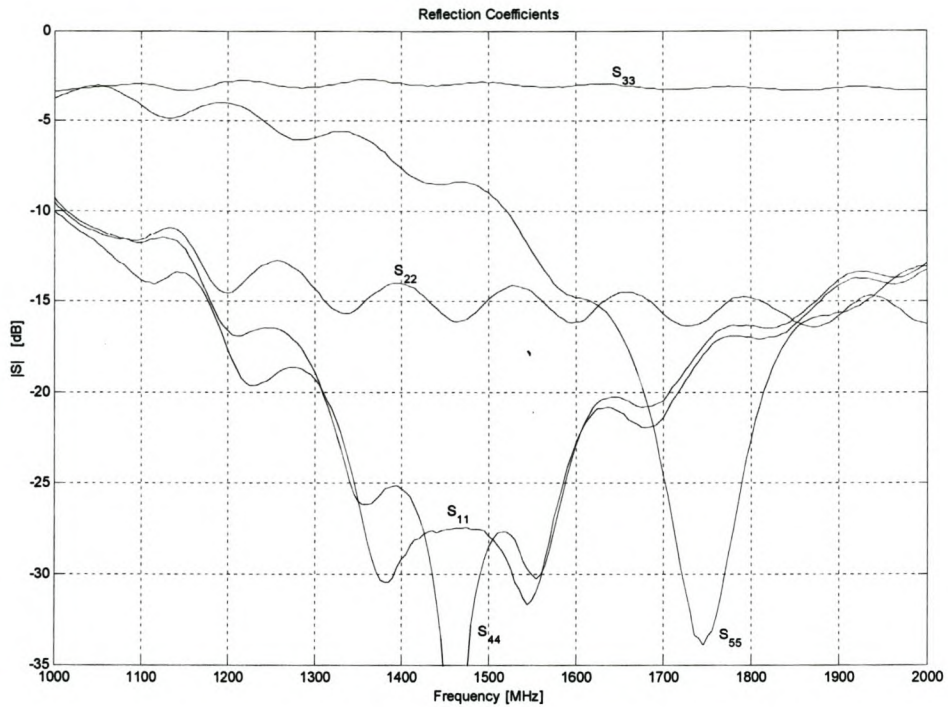


Figure 58 Reflection Coefficients

It is clear that all input ports are well matched between 1 GHz and 2 GHz. Port five is not well matches to a 50 Ω load.

The isolation between ports is plotted in Figure 59.

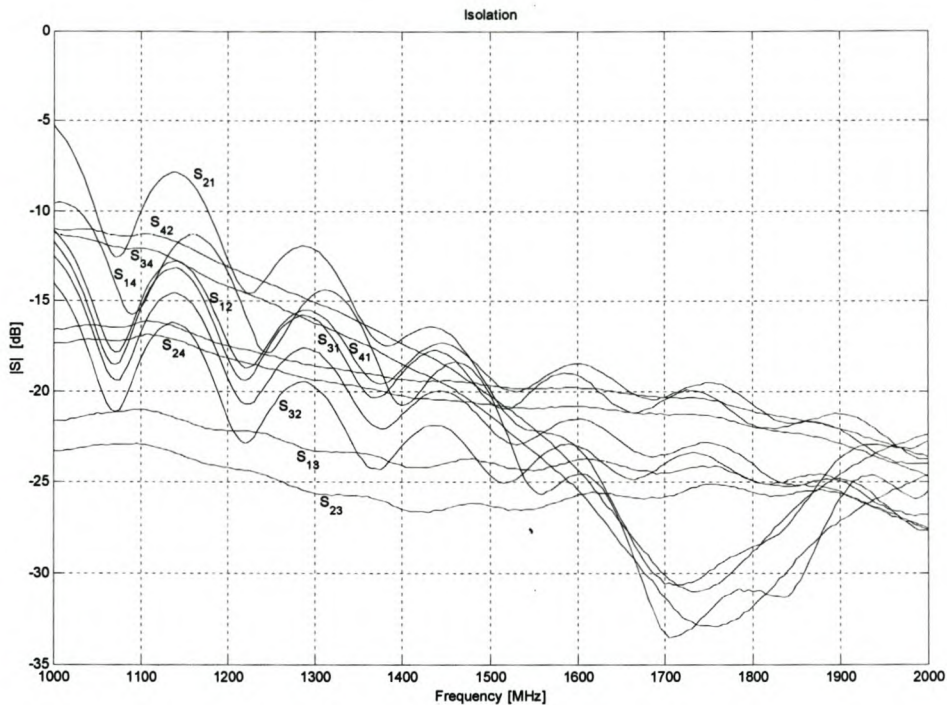


Figure 59 Isolation

The isolation between ports are generally below -15 dB. This value is acceptable.

The combiner is connected to the modulator output with an *LMR100* coaxial cable and *MCX* connectors.

4.12. Modulated Frequency Spectrum

The modulated frequency spectrum of modulator number 2 is shown in Figure 60.

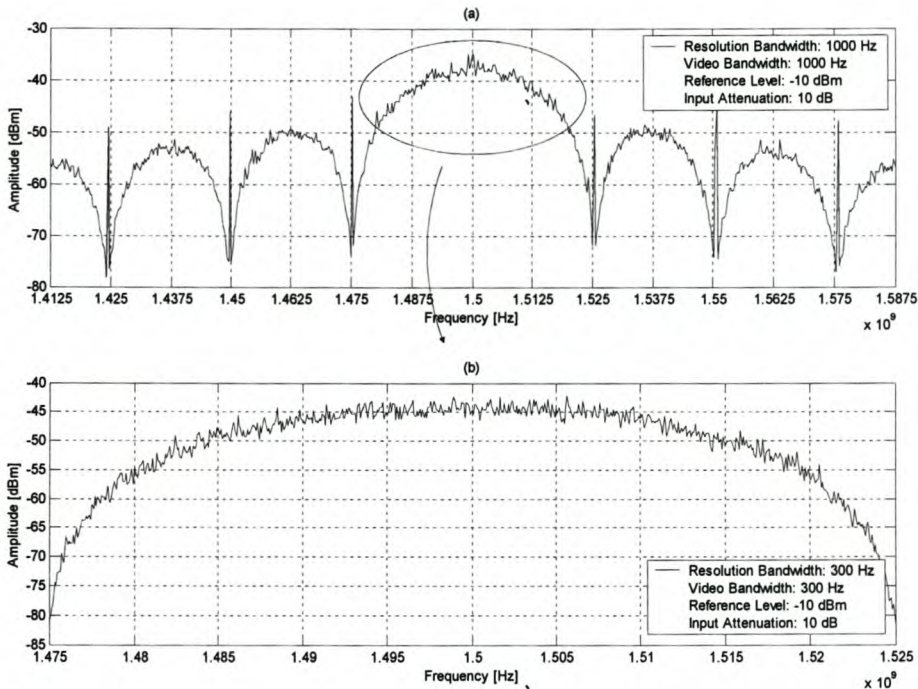


Figure 60 Modulated Frequency Spectrum

It is clear from Figure 60 that no carrier leakthrough is present. Also, note the digital clock leakthrough at multiples of 25 MHz. These spurious frequencies are outside the effective bandwidth and no interference is expected. When a double or triple channel transmitter is implemented, these frequency components might fall inside the main lobe of another modulated channel.

4.13. Transmitter Tuning and Testing

4.13.1. Compensation for Amplitude Mismatch, Oscillator Leakthrough and Phase Error

When a rectangular single sideband I/Q signal is modulated by a QPSK modulator, the abovementioned inaccuracies become apparent. These are identified as spurious signals in the frequency spectrum. The theoretical analysis of these as well as the compensation was discussed in chapter 3 and is summarized in Table 8. The carrier frequency is represented by f_c and the symbol rate by SR . As was

mentioned in section 4.4.1, when single sideband data is generated by the data generator, the symbol rate is divided by two.

Table 8 Modulator Inaccuracies and Compensation

Modulator Inaccuracy	Compensation	Spurious Frequency
Oscillator Leakthrough	DC-offset,	f_c
Amplitude Mismatch	Amplitude Compensation	$f_c - SR$ $f_c + 3SR$ $f_c - 5SR$...
Phase Error	no compensation	$f_c - SR$ $f_c + 3SR$ $f_c - 5SR$...

The modulated frequency spectrum is shown in Figure 61. Graph (a) is before compensation is applied and graph (b) after. The spurious frequencies are marked. The symbol rate, as indicated by the *QPSK System Controller* software as the DDS frequency is 25 MHz. Since the data generator divides this symbol rate by two, the new symbol rate is 12.5 Msps. One channel of a single sideband signal consists of a bit stream of 1 and 0's. Therefore the fundamental frequency component is at 6.25 MHz. Note the same distance between the fundamental frequency component and the carrier frequency. The carrier frequency is at 1.5 GHz.

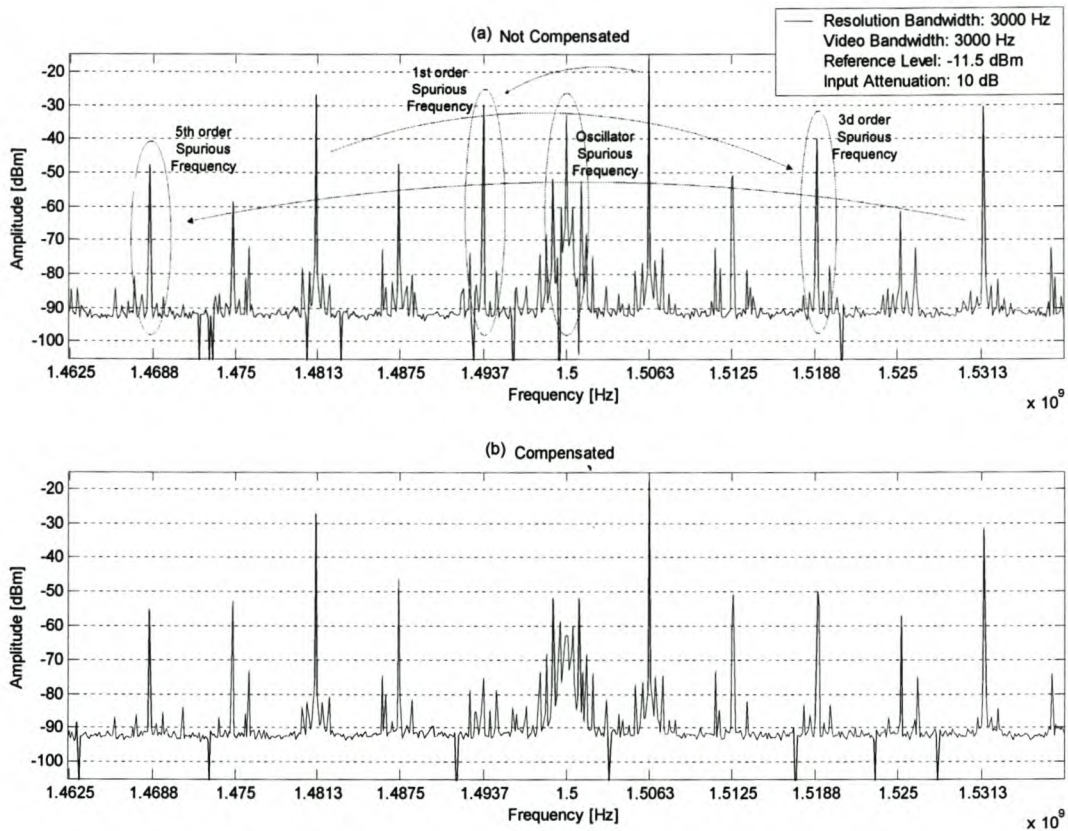


Figure 61 Compensation of Inaccuracies

The carrier and sideband rejection measured in Figure 61 are 35 dB and 60 dB respectively. This is better than specified in Table 7.

The spurious frequencies at multiples of 25 MHz are caused by leakthrough of the digital clock. Since the *I* and *Q* channels are routed in close proximity to each other, leakthrough and mixing products are present. The spurious signal at frequency 12.5 MHz above (and below) the carrier frequency is an example of such a mixing product. It is caused by the product of one channel's third order harmonic and the other channel's fundamental. These products can be minimized by the use of better PCB layout techniques.

The methods used to compensate for inaccuracies will be better explained:

Oscillator Leakthrough

The spurious frequency component at the carrier frequency is caused by oscillator leakthrough and/or DC-offset. As was described earlier, DC-offset can be varied in order to compensate for oscillator leakthrough. Offset, relative to the modulator's reference voltage, is added to each channel separately before modulation and is controlled with a variable resistor.

The technique is to vary one channel's offset until a minimum leakthrough is reached. Switch to the other channel and vary the offset until a minimum is reached. This is an iterative process and should continue until the leakthrough is as low as possible.

As shown in Figure 61(b), the leakthrough did not disappear completely. In order to improve this, a multi-turn variable resistor should be used to increase the tune resolution. It might be further improved if the modulator's reference voltage is adjustable. A simple voltage division circuit should work.

Amplitude Mismatch

The spurious frequency components at fundamental, third, fifth, etc. are partly caused by amplitude mismatch in each channel and in the mixing circuit of the modulator. As described earlier, the mismatch in the modulator can be compensated for with a purposely generated channel mismatch. The amplitude of each channel is controlled with a variable resistor, controlling the gain of the buffer.

The technique is to vary one channel's amplitude until the fundamental spurious frequency reaches a minimum. The same is done for the second channel. Again, this is an iterative process and should continue until the fundamental frequency component is as low as possible. It might be that the spurious signal does not disappear completely, since the modulator's phase error also causes a spurious signal at the same frequency.

Phase Error

When phase error inside the modulator is present, the spurious signals are the same as in the case of amplitude mismatch. As explained in section 4.3, it is not possible to compensate for this error.

4.14. Computer Interface

The computer's serial port is used for communication with the microcontroller on the transmitter. The graphical user's interface of the transmitter page is shown in Figure 62.

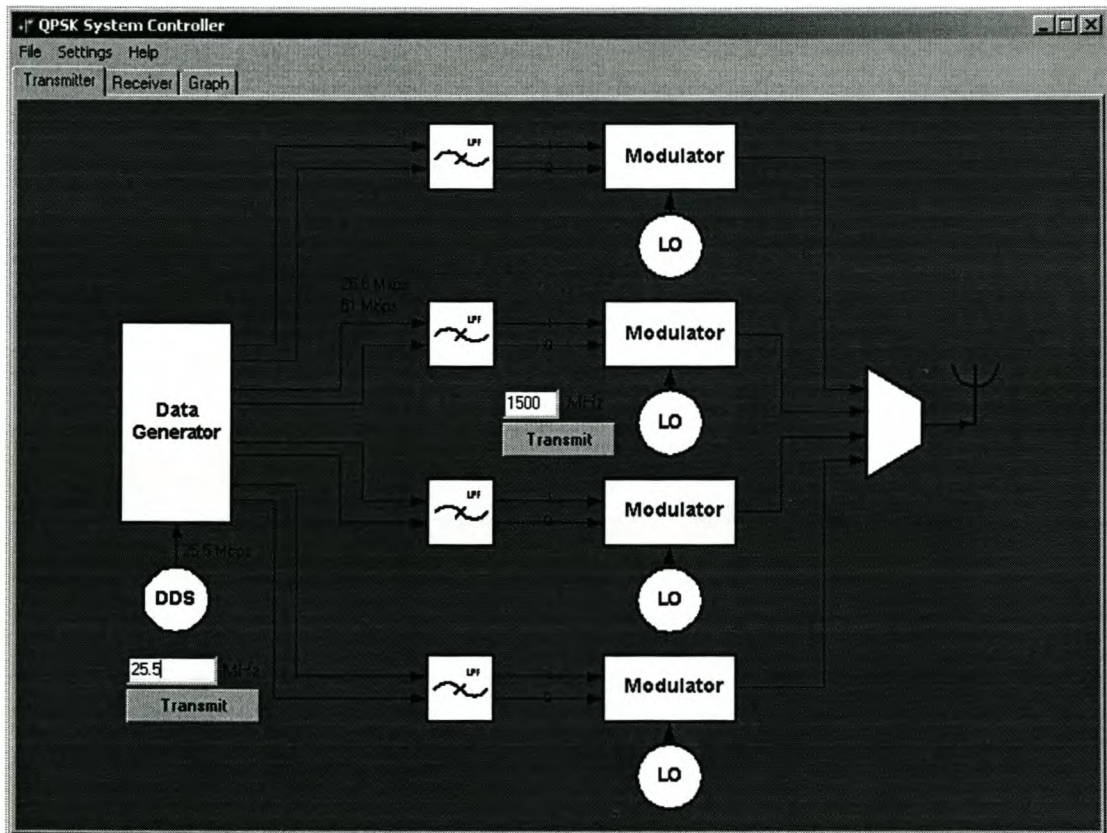


Figure 62 Graphical user's interface of Transmitter Section of QPSK System Controller Program

The user's guide is included in Appendix B.

4.15. Power Supply

In order to simplify the external power supply demand, it is required to use only one external power source and convert all voltage levels from there. An external voltage source of 20V to 30V was chosen. A photograph of the power supply section is shown in Figure 63.

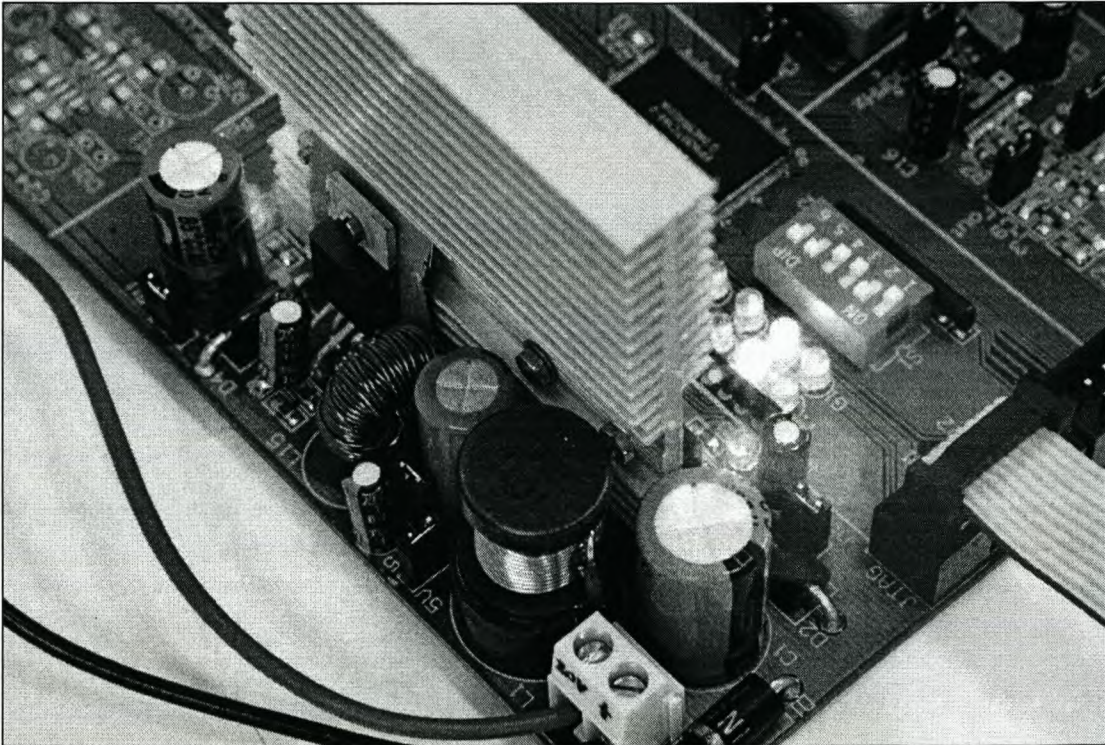


Figure 63 Photograph of Power Supply Section

A summary of the voltage levels required by the transmitter circuit is shown in Table 9.

Table 9 Voltage Levels of Transmitter Circuit

Supply Voltage	Components using Supply Voltage	Maximum Current	Current Used
3.3 V	FPGA Atmel Storage Device	210 mA	145 mA
2.5 V	FPGA	10 mA	10 mA
5 V	3.3 V Voltage Regulator 2.5 V Voltage Regulator Microcontroller Max 232 DDS Driver Modulator Oscillators Synthesizer	1.56 A	241 mA
-5 V	Driver	100 mA	74 mA
15 V	Synthesizer	140 mA	35 mA

Each voltage regulator can be disabled by a jumper. This is to simplify testing. Each rail is also equipped with a red LED to indicate the state of the rail.

The design and operation of each voltage regulator will be discussed in more detail.

4.15.1. 5 Volt Supply Rail

In order to generate a 5V level from an input of up to 30V, a regulator with the minimum amount of power loss is required. The loss in a linear voltage regulator will be too high. A solution to the problem is a switch mode regulator. A 3A, switching regulator from ON Semiconductor¹⁴ was implemented. The 5 V rail was designed for a load of up to 3A. The circuit schematic is shown in Appendix C. The output voltage for a load and no-load condition is shown in Figure 64.

¹⁴ Part number: LM2576

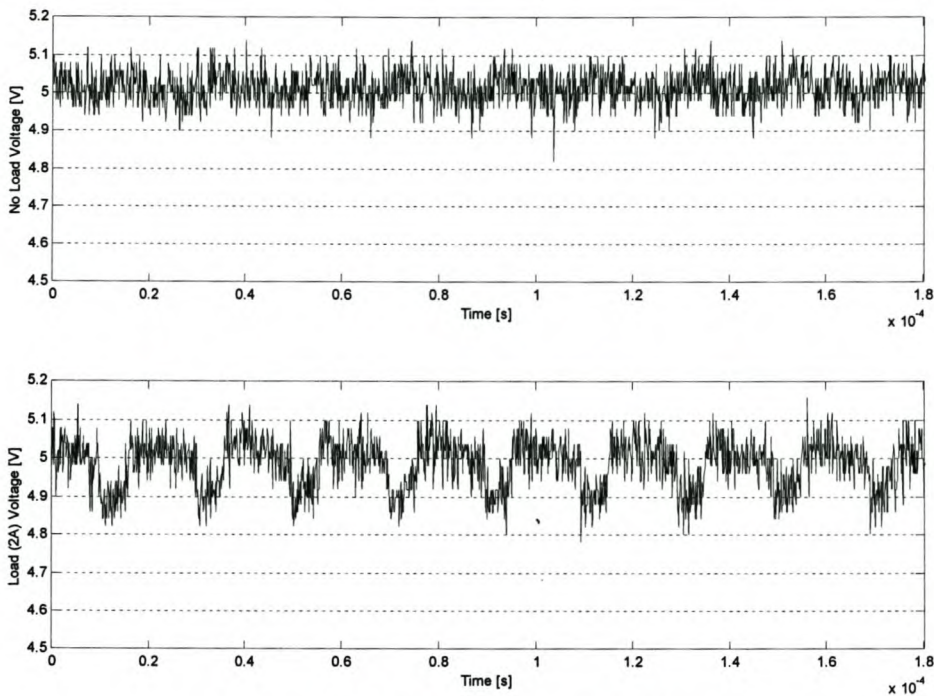


Figure 64 5 Volt Supply waveforms

According to Figure 64, the ripple for no load is 150 mV_{pp} , and for a load current of 2 A, 225 mV_{pp} . The switch mode frequency of 52 kHz is clearly visible. This ripple level is acceptable.

4.15.2. 3.3 Volt and 2.5 Volt Supply Rails

The 3.3V and 2.5V supplies are generated by linear regulators, with the 5V from the switch mode regulator as input voltage. The circuit schematic is shown in Appendix C. The 3.3V supply voltage is shown in Figure 65 for load and no-load condition. The 5V supply is loaded with an additional 1W load in order to increase output ripple of the 5V supply.

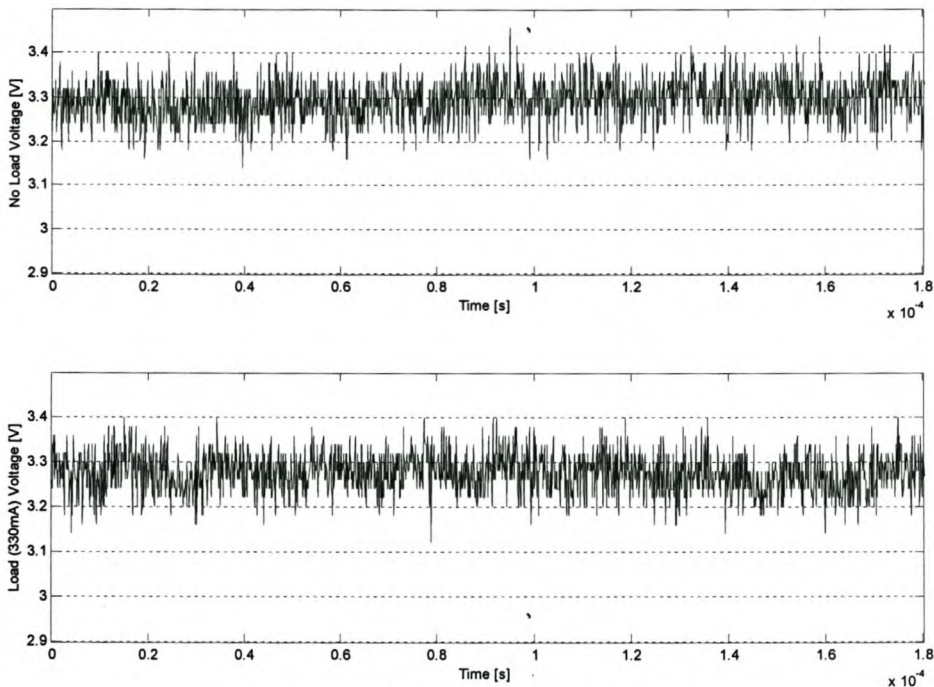


Figure 65 3.3 Volt Supply Waveforms

According to Figure 65, the ripple for no load and load current of 330 mA is 125 mV_{pp} . The switch mode ripple is reduced by more than 50%. According to the FPGA's data sheet [2], this voltage level is acceptable.

4.15.3. -5 Volt Supply Rail

The same switch mode regulator as for the 5V rail was used in a different configuration to generate a negative supply from a positive rail. The -5 V rail was designed for a load of up to 1A. The circuit schematic is shown in Appendix C. The output voltage for a load and no-load condition is shown in Figure 66.

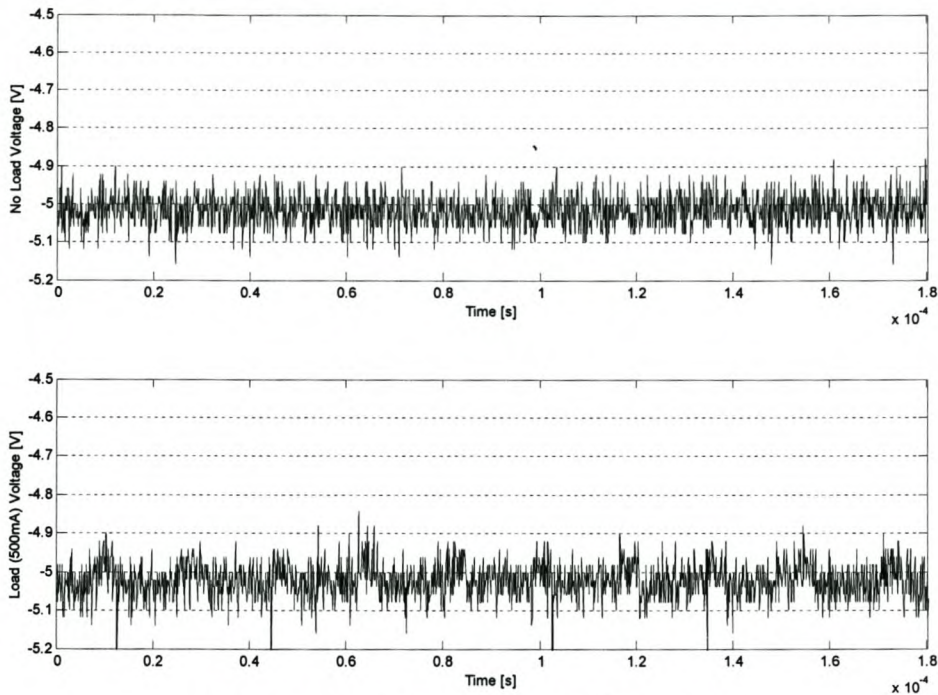


Figure 66 -5 Volt Supply Waveform

According to Figure 66, the ripple for no-load and load current of 500 mA is 150 mV_{pp}. This voltage level is acceptable for the driver [5].

4.15.4. 15 Volt Supply Rail

A linear voltage regulator was used for this rail¹⁵. The use of a linear regulator is justifiable due to the small current demand of this rail. The circuit schematic is shown in Appendix C.

¹⁵ Part number: LM7815

5. QPSK Receiver

The digital video broadcasting (DVB) standards cover all aspects of digital television from transmission through interfacing, conditional access and interactivity for digital video, audio and data. A consortium came together in 1993 committed to designing global standards for the delivery of digital television and data services. The DVB project is an industry-led consortium of over 300 broadcasters, manufacturers, network operators, software developers, regulatory bodies and others in over 35 countries [9].

To date, there are numerous broadcast services using DVB standards. There are hundreds of manufacturers offering DVB compliant equipment, which is already in use around the world. DVB dominates the digital broadcasting world. A wide spectrum of services in the satellite (DVB-S), terrestrial (DVB-T) and cable (DVB-C) are available [9].

This chapter will discuss the performance of a commercially available DVB-S receiver unit from Sancy. This unit was implemented in a QPSK receiver system. For the duration of this thesis, the term DVB will stand for the DVB-S standards.

5.1. DVB Receiver System

The Sancy DVB system is a very versatile digital receiver. A wide range of options can be controlled by programming registers through an I²C interface. The Sancy DVB block diagram is shown in Figure 67 [11].

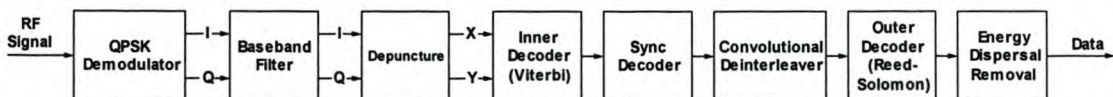


Figure 67 Sancy DVB Receiver's Block Diagram

The modulated signal is demodulated by the QPSK demodulator and an I and Q channel is obtained. After demodulation each channel is sampled and filtered by a digital filter. The puncture rate is removed before the inner Viterbi decoder removes the convolutional code. The receiver is able to recognise a number of puncture rates, including $\frac{1}{2}$ rate as used by the QPSK transmitter.

The synchronization byte decoder provides synchronization information for the de-interleaver. The convolutional de-interleaver allows an error bursts at the output of the inner decoder to be randomized on a byte basis in order to improve the burst error correction capability of the outer decoder. This block can be disabled through registers.

The Reed-Solomon outer decoder provides second level error protection. This decoder is developed to recover data when an error burst occurs. This decoder can be disabled.

The energy dispersal remover recovers the user data by removing the randomizing pattern used for energy dispersal purposes. This unit can be disabled.

In order to characterize the Sancy DVB receiver, a well-defined modulated signal is required. The signal generated by the custom-developed QPSK transmitter was used. The transmitter is tuned to give optimal performance. Increased performance was achieved when an external local oscillator was used¹⁶.

¹⁶ A SML03 (9kHz to 3.3GHz) Rhode&Schwarz Signal Generator was used.

5.2. Delphi Program

Delphi software has been custom-developed to program the Sancy DVB receiver's registers and monitor the state of the receiver. The user interface is shown in Figure 68.

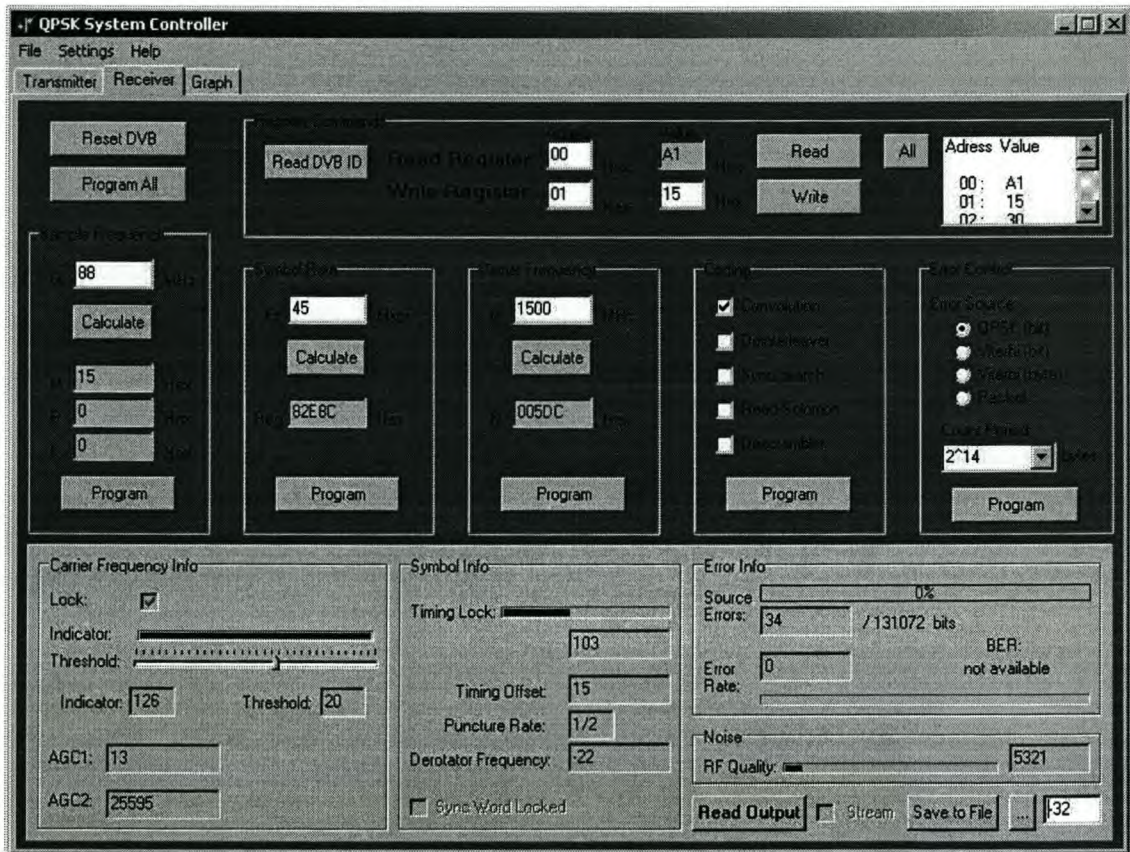


Figure 68 User Interface for Receiver Section of QPSK System Controller Program

A complete user's manual has been created and included in Appendix B.

5.3. Status Registers

When the Sancy DVB receiver is programmed, the status of the demodulator is monitored by reading different registers. Some of the registers are explained in Table 10 [29].

Table 10 Sancy DVB Receiver Status Registers

Register Name	Register	Address [Hex]	Register Size (Value Range)	Register Description
Carrier Locked Detector Register	CLDI	16	8 bit signed value (-128 to 127)	The CLDI register value is compared to a preset value, and yields CF=1 when CLDI is greater than the preset value. The value is also dependent upon channel noise. CLDI should be as high as possible.
Auto Gain Control Integrator Value	AGC1	16	8 bit signed value (-128 to 127)	Used as a measure of the signal amplitude, measured before the Nyquist filter
Auto Gain Control Integrator Value	AGC2	18,19	16 bit unsigned value (0 to 65535)	Used as a measure of the signal amplitude, measured after the Nyquist filter
Timing Lock Indicator Register	TLIR	17	8 bit unsigned value (0 to 255)	Value depends on upon signal-to-noise ratio and the signal lock state. TLIR should be as high as possible.
Timing Frequency Register	RTF	1A	8 bit signed value (-128 to 127)	Indication of the frequency offset when the receiver is locked. Value should be as close as possible to zero.
Carrier Frequency Register	CFR	22,23	16 bit signed value (-32768 to 32767)	An indication of the derotator frequency.
Error Count Register	ERRCNT	1D,1E	16 bit unsigned value (0 to 65535)	An error rate measurement (error mode 0), measuring the amount of errors within a certain number of bytes (eg. 2^{18} bytes) If the maximum count is exceeded, the count remains at the maximum value.
Viterbi Errors	VEERROR	26	8 bit unsigned value (0 to 255)	Indication of Viterbi errors
Noise Indicator Register	NIR	24,25	16 bit unsigned value (0 to 65535)	Used to measure RF signal Quality. Intended to be used with pre-recorded lookup tables. NIR should be as low as possible.

The registers can be divided into three categories, shown in Table 11.

Table 11 DVB Register Categorization

Register Category	Registers
Carrier Power	AGC ₁ , AGC ₂
Carrier Quality and Noise	CLDI, CFR TLIR, RTF, NIR
Errors	ERRCNT, VERROR

5.4. Carrier Frequency Varied

The carrier frequency of the modulator and demodulator was varied in order to determine the optimal carrier frequency for the Sancy DVB receiver.

For each frequency point data was captured for ten successive measurements and averaged. For error count and max error count, the counts were added and not averaged. To calculate the bit error rate, the total errors were divided by the total bits. If the bit error rate was zero (a value below 1×10^{-9}) for a specific frequency, the point was omitted from the logarithmic bit error rate plot. Data was captured for four different symbol rates.

The parameters that did not change during the measurement are summarized in Table 12.

Table 12 Measurement Parameters

Parameter	Value	Unit
Modulator Number	2	
Carrier Power	-32	dBm
Symbol Rate	5, 10, 25, 45	Msp
Bandwidth	full	
Noise	no	
DVB Sample Frequency	80	MHz

The signal power level in Table 12 was achieved by attenuating the output from modulator number two with 20 dB¹⁷.

When the carrier frequency is varied, the registers monitoring the carrier will be affected. These are carrier locked detector register (CLDI) and the carrier frequency register (CFR), indicating the derotation frequency. These are plotted in Figure 69 and Figure 70 respectively. Each register is limited by the size of the register. The grey areas in a graph are the out of range values of the specific register.

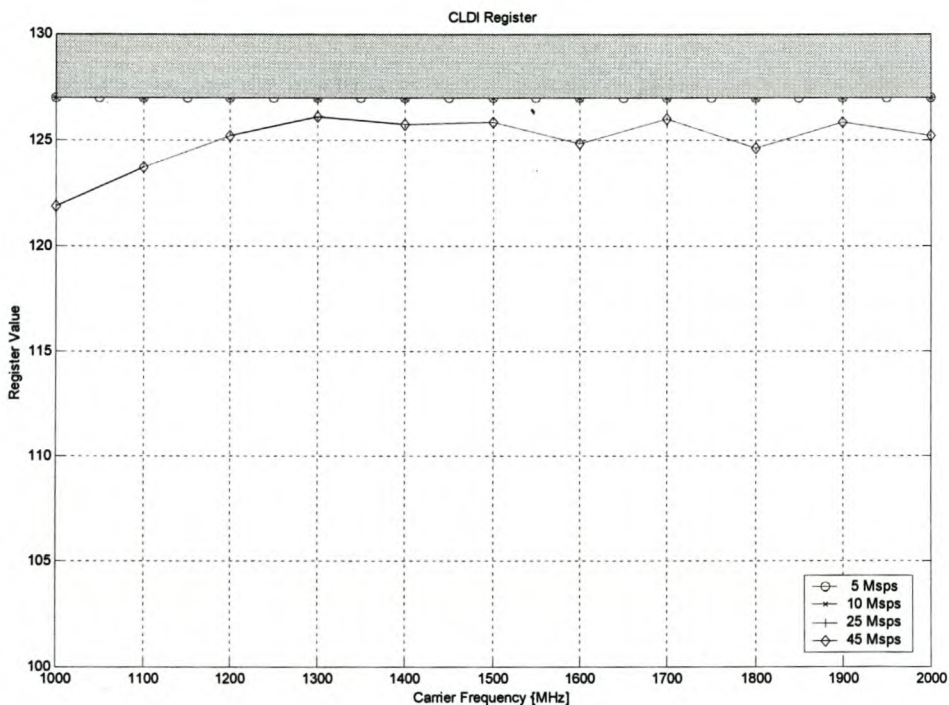


Figure 69 Carrier Locked Detector Register when the Carrier Frequency is Varied

The Sancy DVB receiver's carrier lock indicator value is the highest for lower data rates across the complete frequency range. At maximum data rate the lock indicator is lower, but still fairly good.

¹⁷ The HP 8496A Attenuator was used. This attenuator is characterized in Appendix F.

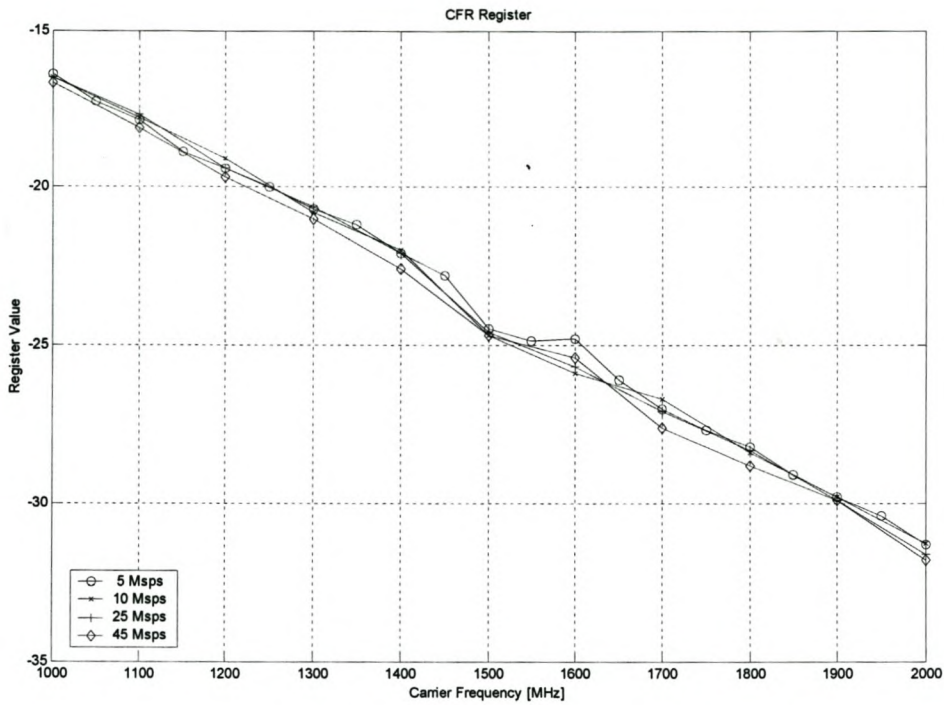


Figure 70 Carrier Frequency Register when the Carrier Frequency is Varied

The derotator frequency has a near linear response to frequency change for all data rates.

The carrier power register are AGC_1 and AGC_2 , where the former is plotted in Figure 71.

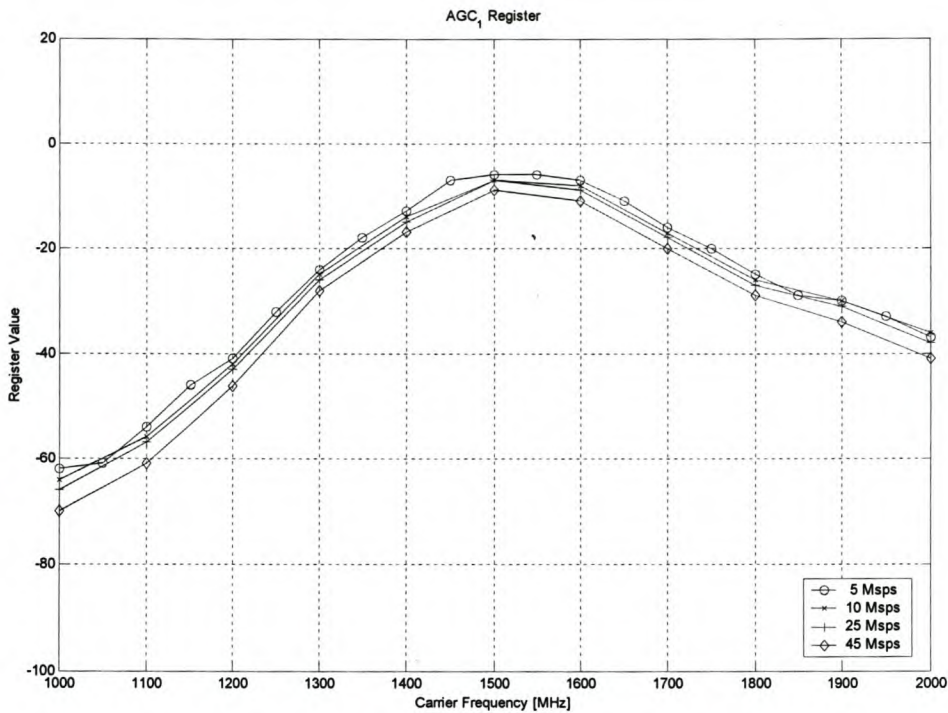


Figure 71 Carrier Power Register (before Filter) when the Carrier Frequency is Varied

When constant power is received, registers AGC_1 and AGC_2 remains constant. Figure 71 suggests that the transmitted power is varied with frequency, reaching a maximum at 1.5 GHz. Since the modulator's local oscillator power level remained constant across the frequency sweep, it might be possible that the modulator produced a power level that is not constant. After further inspection this was found not to be the case. This phenomenon will be dealt with in section 5.5.

The registers indicating carrier quality and noise, TLIR, RTF and NIR show that the quality and noise is constant across the frequency range.

The bit error rate is calculated from the error count register. This is plotted in Figure 72. The Viterbi error register is at zero across the frequency range.

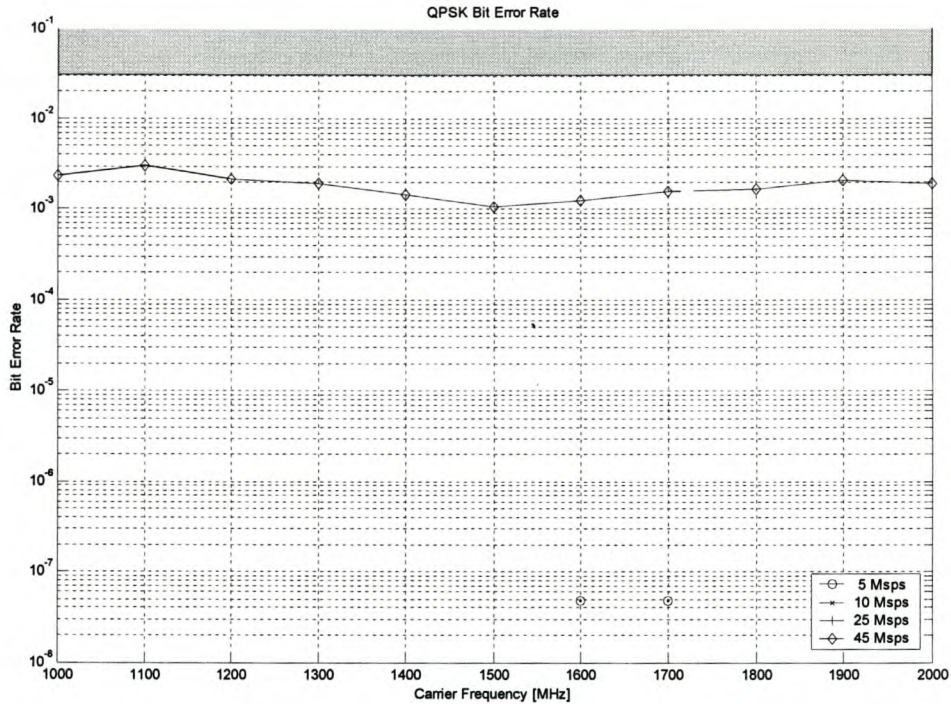


Figure 72 Bit Error Rate when the Carrier Frequency is Varied

The bit error rate is at zero for 10 Mps and 25 Mps across the frequency range. At the higher and lower symbol rates, a minimum value is reached at 1.5 GHz. Since the bit error rate variance at 45 Mps is relatively small, it is safe to assume that the receiver's optimal performance is not dependent upon the carrier frequency.

5.5. Carrier Power Varied

The input power to the Sancy DVB receiver was varied in order to determine the optimal power level for the receiver.

For each input power level the data of four different symbol rates was captured. The capturing method and averaging are the same as in section 5.4 when the carrier frequency was varied. The input power was measured with a power meter¹⁸.

The parameters that did not change during the measurement are summarized in Table 13.

Table 13 Measurement Parameters

Parameter	Value	Unit
Modulator Number	2	
Carrier Frequency	1.5	GHz
Symbol Rate	5, 10, 25, 45	Msps
Bandwidth	full	
DVB Sample Frequency	80	MHz

When the carrier power is varied, the registers monitoring the power levels will be affected. These are registers AGC₁ and AGC₂ and are plotted in Figure 73 and Figure 74 respectively.

¹⁸ WaveTek 8501A power meter

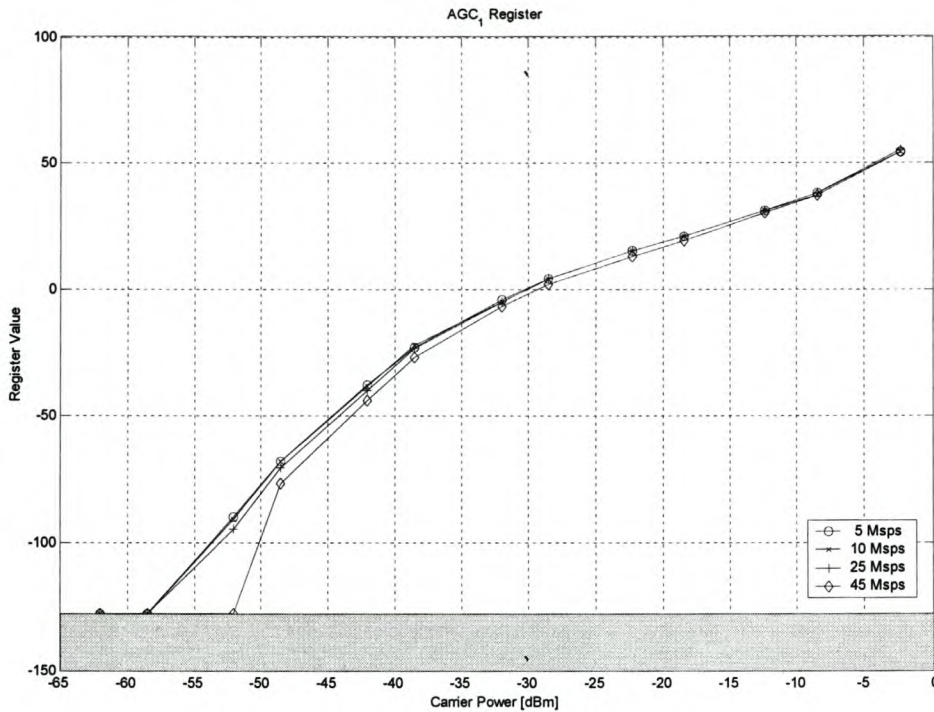


Figure 73 Carrier Power Register (before Filter) when the Carrier Power is Varied

Above -55 dBm register AGC_1 can be used to gauge the received power level. The relationship between carrier power and register AGC_1 's value is not linear, thus a lookup table should be used to indicate the power level of the carrier. The register value is dependent of the symbol rate used.

As was seen in Figure 71, for a fixed power level the value of AGC_1 register varied with the carrier frequency. Thus when a lookup table is implemented to gauge a power level above -55 dB, the carrier frequency should be taken into consideration.

Below -55 dBm register AGC_1 does not represent the power level. Register AGC_2 gives a better representation for low power levels.

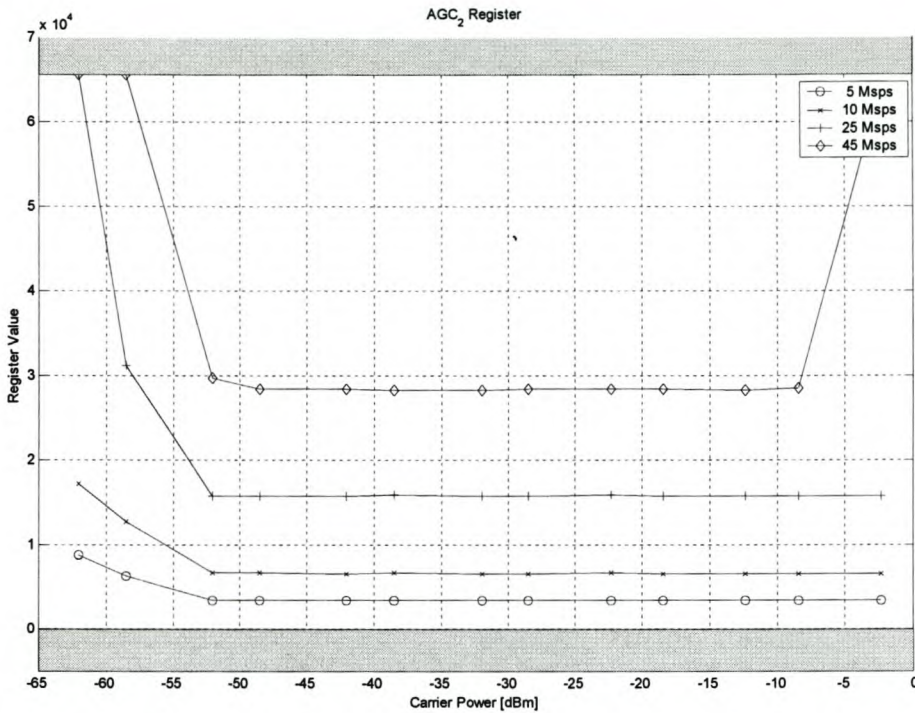


Figure 74 Carrier Power Register (after Filter) when the Carrier Power is Varied .

The Sancy DVB receiver is specified to operate from -65 dBm to -25 dBm. The upper power limit of -10 dBm should be noted at a bit rate of 45 Msps. Register AGC₂ is used to gauge the carrier power below -55 dBm. The register value is dependent on the symbol rate. When a lookup table is implemented to gauge the power level below -55 dBm, the symbol rate should be taken into consideration.

The registers that give an indication of the signal quality and noise are TLIR, RTF and NIR. The best indication of the signal quality and noise is the noise indicator register and is plotted in Figure 75. When the noise level is kept constant and signal level varied, the signal-to-noise level will vary and thus affect the noise indicator register.

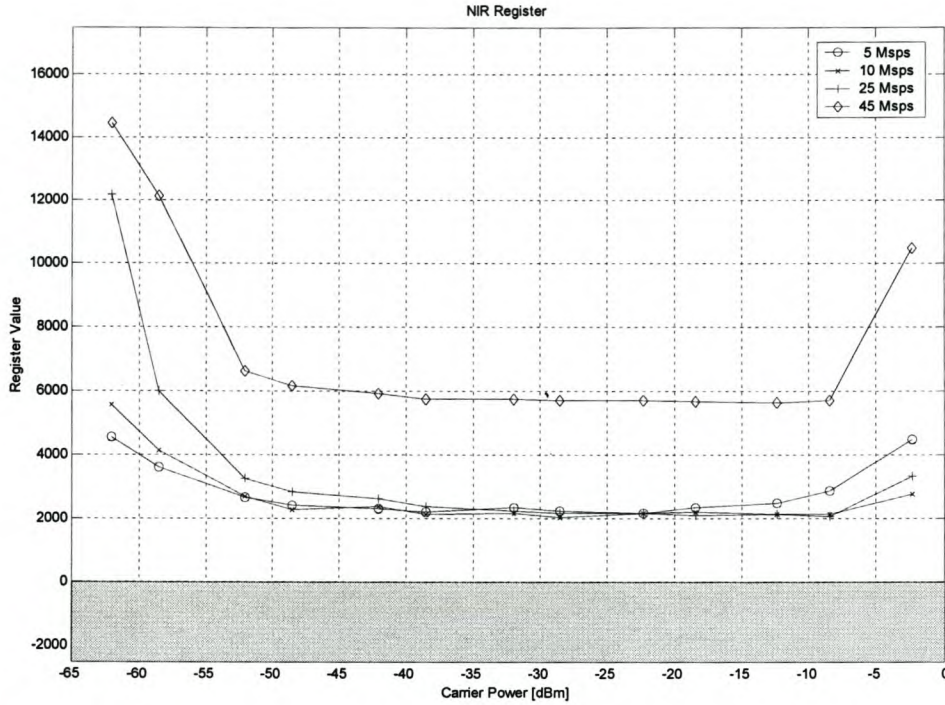


Figure 75 Noise Indicator Register when the Carrier Power is Varied

The noise indicator register shows that the quality of the RF signal is the best between -55 dBm and -10 dBm. The quality level for a specific symbol rate remains constant across this power range. Thus the optimal power range for the receiver can be defined from -55 dBm to -10 dBm. This optimal power range is verified by registers TLIR, CLDI, CFR and RTF.

The bit error rate is calculated from the error count register. This is plotted in Figure 76.

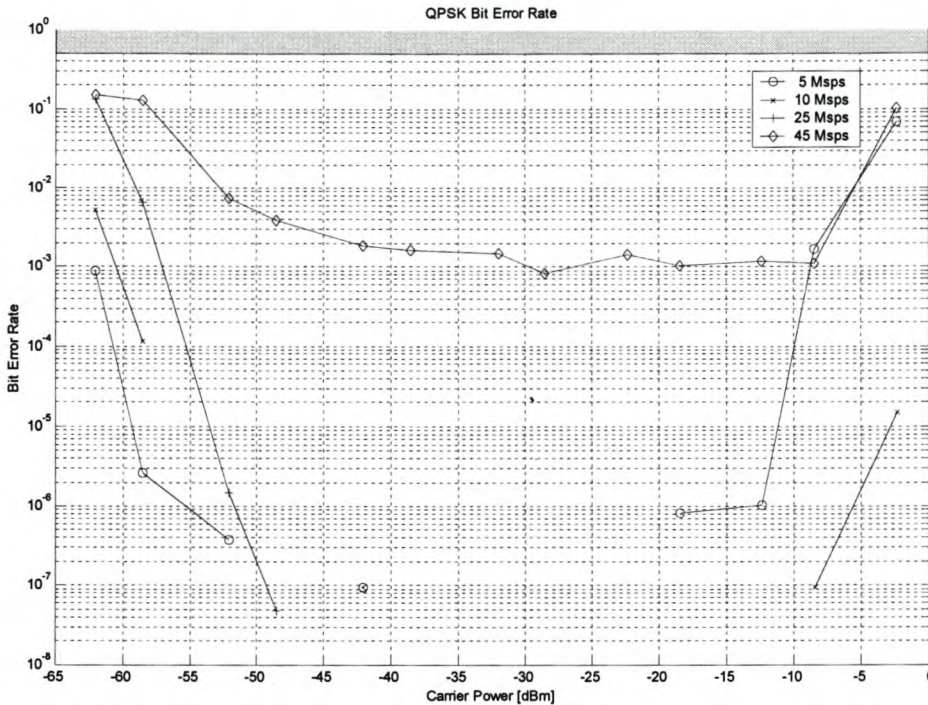


Figure 76 Bit Error Rate when the Carrier Power is Varied

The bit error rate for a specific symbol rate remains near constant across the optimal power range. Note the higher bit error rate at maximum symbol rate.

The Viterbi error register also indicates errors outside the optimal power range.

5.6. Symbol Rate Varied

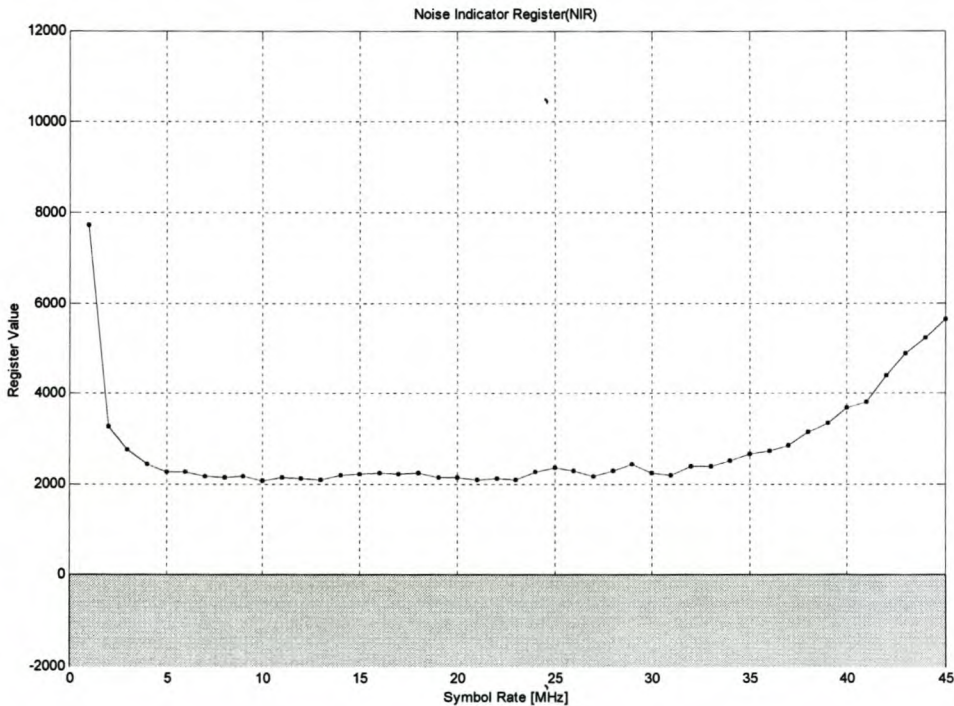
The symbol rate of the transmitter and Sancy DVB receiver was varied in order to determine the optimal symbol rate. The capturing method and averaging are the same as in section 5.4 when the carrier frequency was varied.

The parameters that did not change during the measurement are summarized in Table 14.

Table 14 Measurement Parameters

Parameter	Value	Unit
Modulator Number	2	
Carrier Power	-32	dBm
Carrier Frequency	1.5	GHz
Bandwidth	full	
DVB Sample Frequency	80	MHz

The noise indicator register gives a good indication of the RF signal quality and is plotted in Figure 77.

**Figure 77 Noise Indicator Register when the Symbol Rate is varied**

The receiver is not able to operate at a symbol rate below 2 Msps. A safe lower limit would be 5 Msps. When the symbol rate of 35 Msps is exceeded, the signal quality decreases. The timing lock indicator register also confirms a high timing lock within the abovementioned range. Although the receiver still locks at 45 Msps, these high symbol rates is not advisable.

The carrier power was kept constant for each symbol rate. Thus constant values for registers AGC₁ and AGC₂ were measured. Constant register values were also noted for registers CFR and RTF.

The QPSK bit error rate is calculated from the error count register. This is plotted in Figure 78.

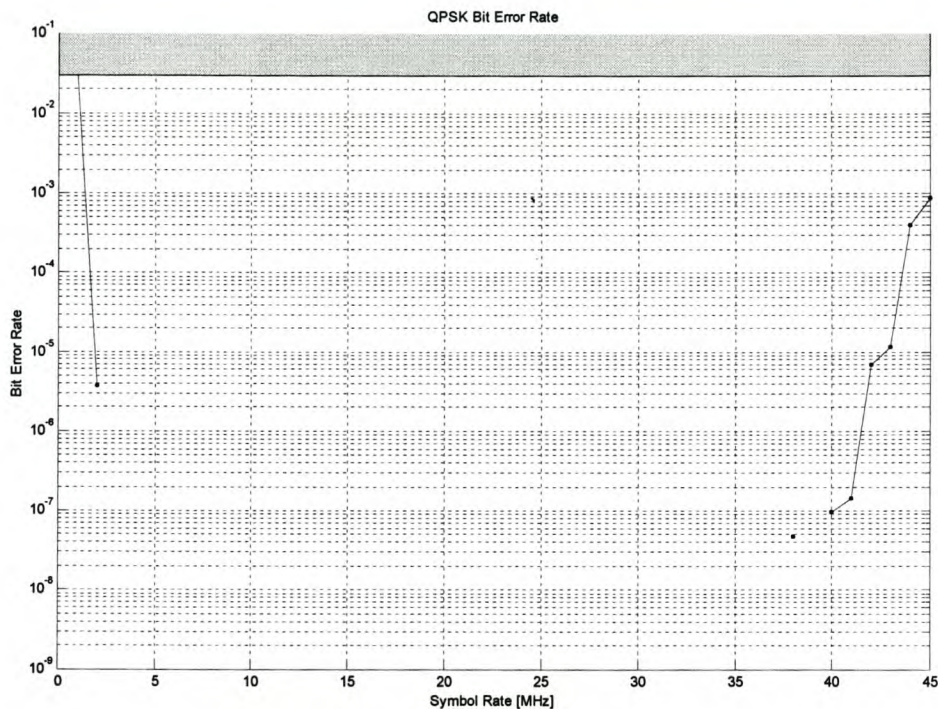


Figure 78 Bit Error Rate when the Symbol Rate is varied

As would be suspected, the bit error rate increased outside the optimal symbol rate range. The Viterbi errors remained zero across the symbol range.

5.7. Sample Frequency Varied

After demodulation each channel was sampled. The programmable sample rate relative to the symbol rate was varied in order to determine the influence on the performance of the receiver.

The uniform sampling theorem for low-pass signals is stated as follows: If a signal contains no frequency component above W hertz, then it is completely described by instantaneous sample values uniformly spaced in time with period T_s , as in equation (5.1). The frequency $2W$ is referred to as the Nyquist frequency [34].

$$\begin{aligned} T_s &\leq \frac{1}{2W} \\ f_s &\geq 2W \\ \frac{W}{f_s} &\leq \frac{1}{2} \end{aligned} \quad (5.1)$$

The sample frequency was kept constant at 24 MHz and the symbol rate varied. The capturing method and averaging is the same as in section 5.4 when the carrier frequency was varied.

The parameters that did not change during the measurement are summarized in Table 15.

Table 15 Measurement Parameters

Parameter	Value	Unit
Modulator Number	2	
Carrier Power	-32	dBm
Carrier Frequency	1.5	GHz
Bandwidth	full	
DVB Sample Frequency	24	MHz

The carrier lock indicator register is plotted in Figure 79.

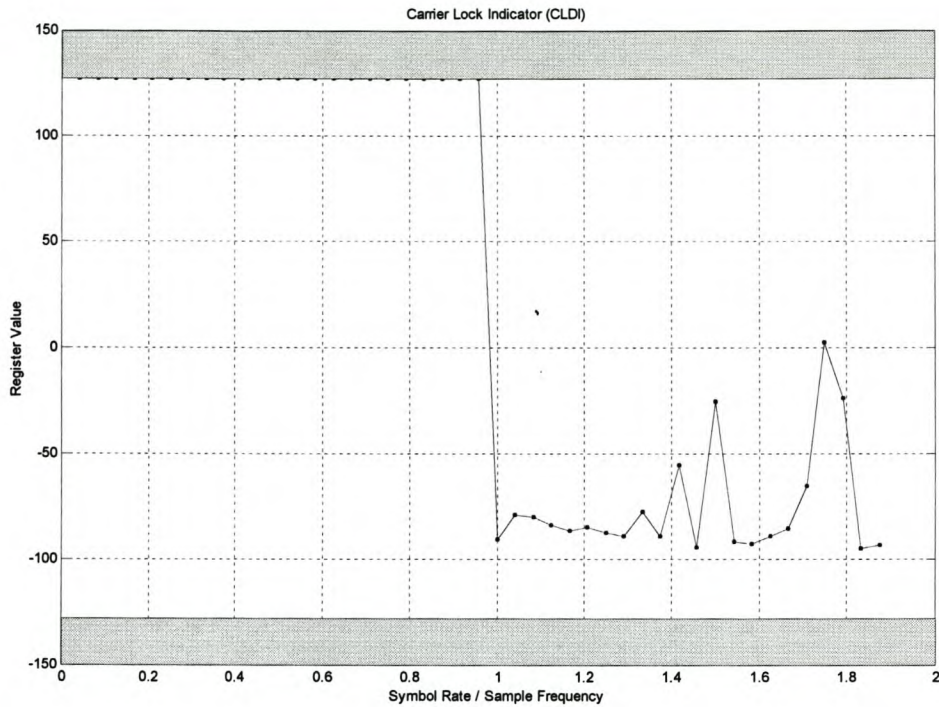


Figure 79 Carrier Lock Indicator when the Sample Frequency is varied

As was predicted, the receiver carrier lock was lost when the symbol rate was above half the sample frequency. Note that the receiver remains locked until the symbol rate is equal to the sample frequency.

The timing lock indicator register is plotted in Figure 80.

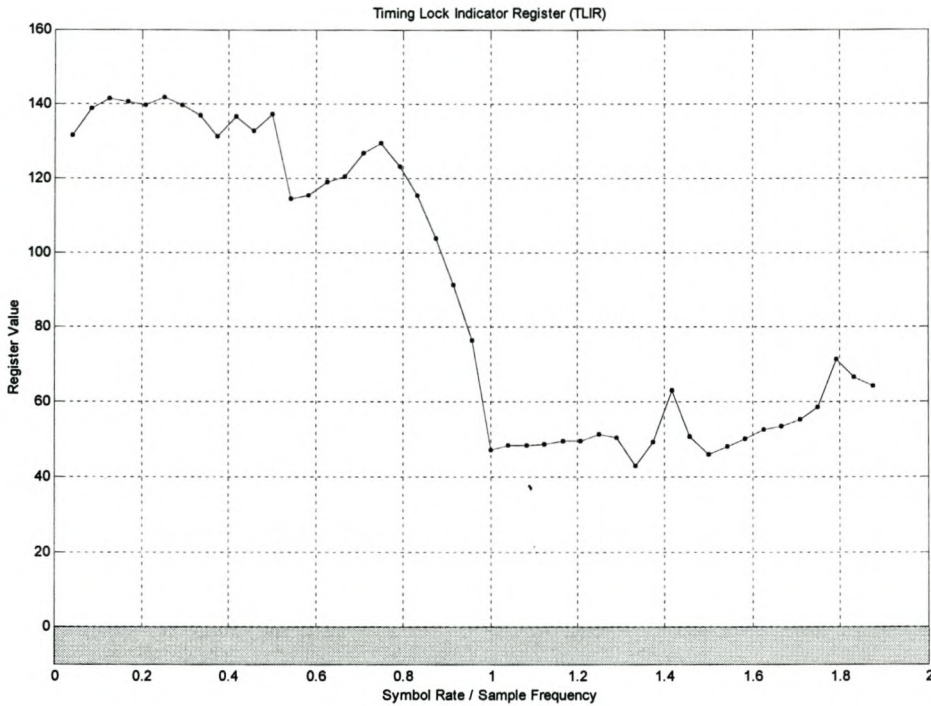


Figure 80 Timing Lock Indicator Register when the Sample Frequency is varied

The timing lock indicator register shows that timing lock starts to decay after the symbol rate is half the sample frequency. This corresponds to equation (5.1). The bit error rate plot in Figure 81 confirms this theory.

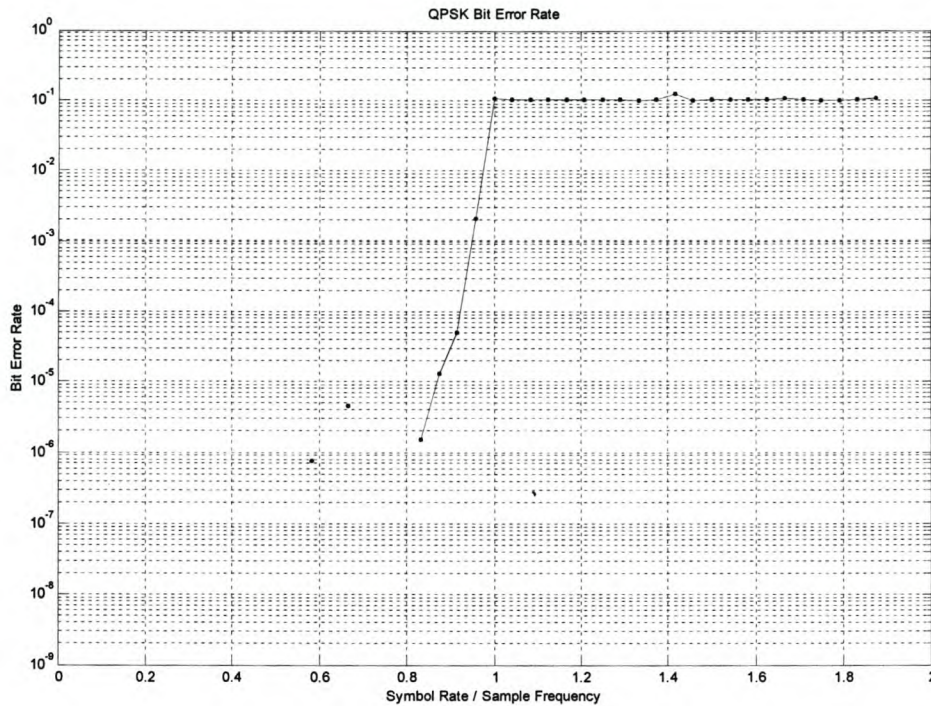


Figure 81 Bit Error Rate when the Sample Frequency is varied

The minimum sample frequency was now determined as twice the symbol rate. The influence of higher sample frequencies will now be investigated.

The symbol rate was varied and compared for three different sample frequencies. The frequencies were chosen at 60 MHz, well above the maximum symbol frequency, at 72 MHz and at the maximum sample frequency of 88 MHz. The capturing method and averaging are the same as in section 5.4 when the carrier frequency was varied.

The parameters that did not change during this measurement are summarized in Table 16.

Table 16 Measurement Parameters

Parameter	Value	Unit
Modulator Number	2	
Carrier Power	-32	dBm
Carrier Frequency	1.5	GHz
Bandwidth	full	
Noise	no	
DVB Sample Frequency	60, 72, 88	MHz

Registers TLIR and NIR, used to indicate signal quality and noise, are plotted in Figure 82 and Figure 83 respectively.

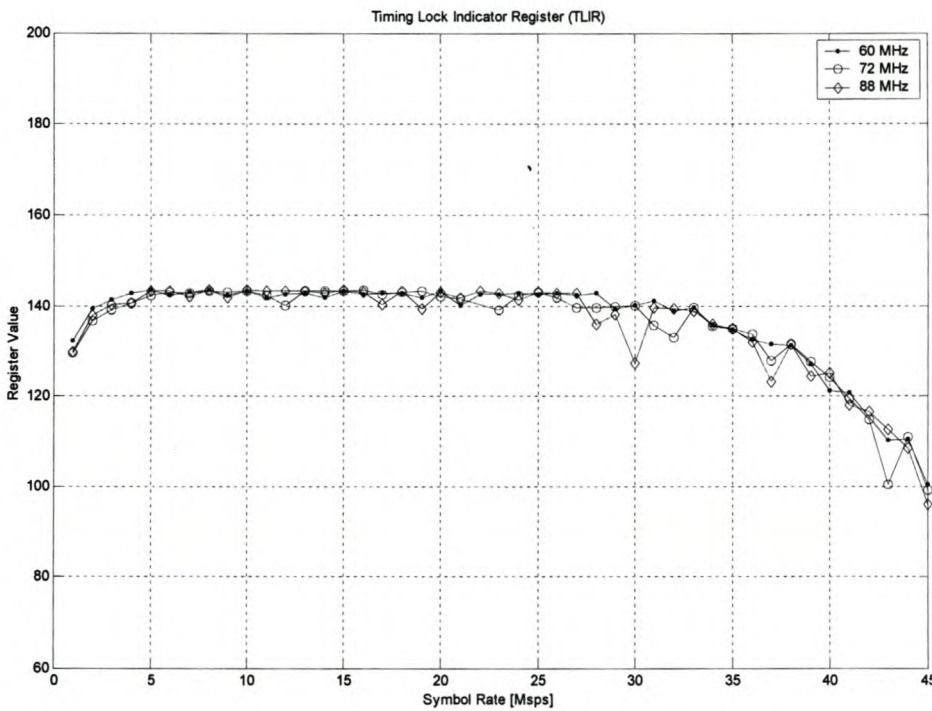


Figure 82 Timing Lock Indicator Register when the Symbol Rate is Varied for Three Sample Frequencies

The timing lock indicator register indicates that all three sample frequencies produce the same lock quality. The same is true for the noise indicator register.

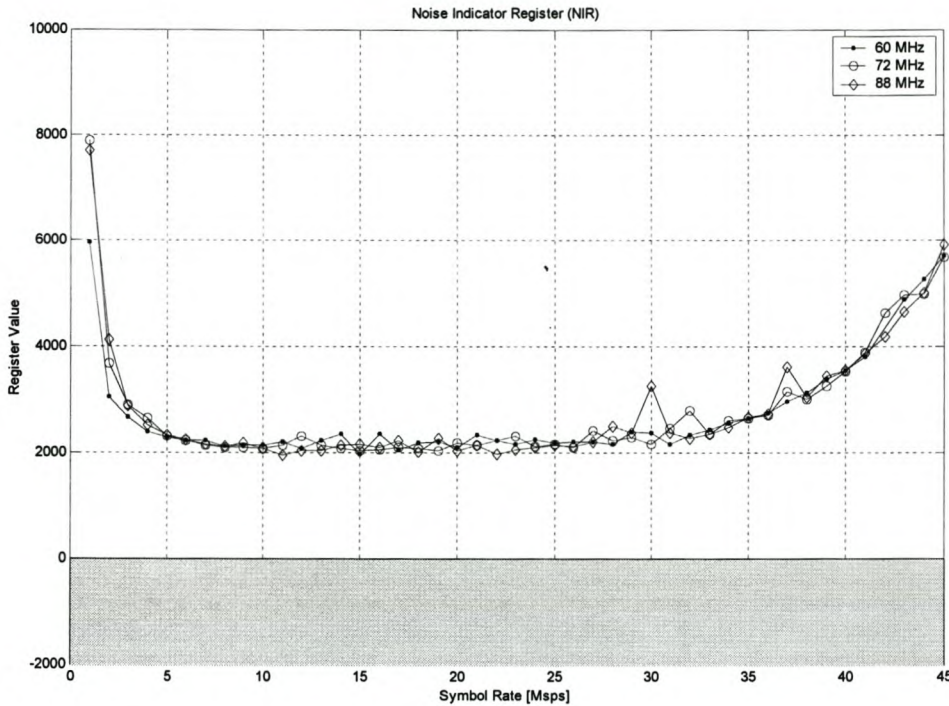


Figure 83 Noise Indicator Register when the Symbol Rate is Varied for Three Sample Frequencies

Since the signal quality and noise are exactly the same for all three sample frequencies, it is suspected that the receiver's performance does not depend on the sample frequency, as long as the sample frequency is well above the symbol rate. This is verified with the bit error rate plot in Figure 84.

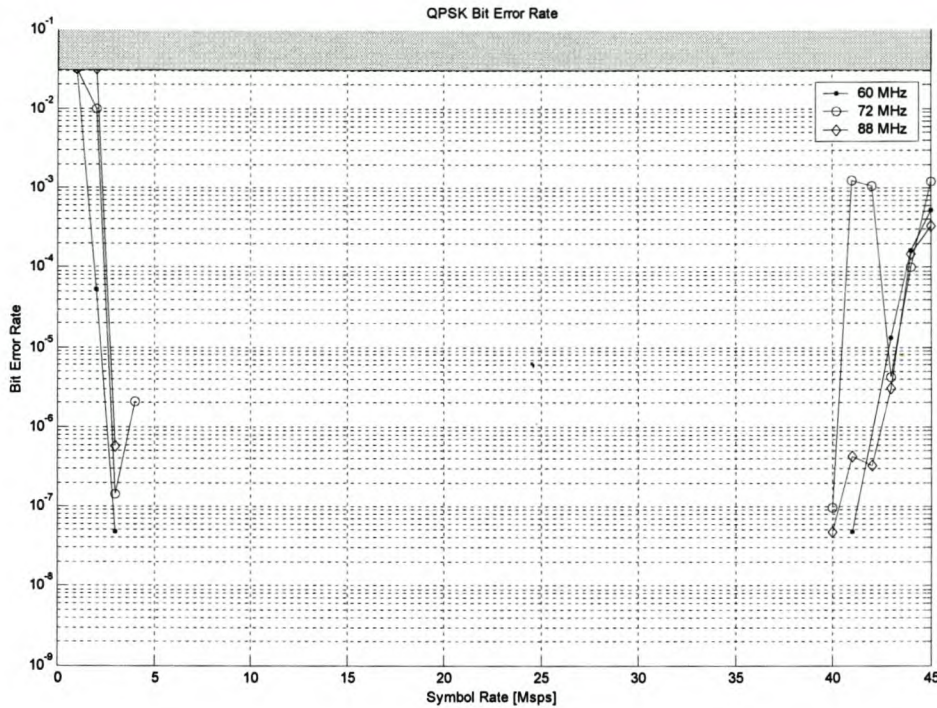


Figure 84 Bit Error Rate Register when the Symbol Rate is Varied for Three Sample Frequencies

The bit error rate is the same for all three sample frequencies. As was noted in section 5.6, the bit error rate increased at very low and high symbol rates.

5.8. Signal-to-Noise Ratio Varied

The signal-to-noise ratio (SNR) was varied in order to determine the influence on the Sancy DVB receiver. This ratio is defined as the signal power to the noise power in a given bandwidth [34].

The thermal noise of a resistor was amplified and combined with the output from modulator three. The modulated signal still remained clear from the noise floor. In order to vary the modulated signal power, the amplitude of the modulator's local oscillator was decreased.

For a modulated signal with unlimited bandwidth the signal and noise power are measured in the nil-to-nil bandwidth. The spectrum analyzer used to measure the power in the specified bandwidth has an internal noise floor of -52.3 dBm ¹⁹. When the power of the QPSK modulated signal is added and varied, the measured power varies from -21.4 dBm to -44.0 dBm . Thus the influence from the internal spectrum analyzer's noise varies from 0.08% to 14%. When the signal power is measured the influence of the internal spectrum analyzer's noise is ignored.

The noise power is measured in the same bandwidth as the signal power. The amplified thermal noise is measured (when the modulated signal is removed) as -45.8 dBm .

The varied signal-to-noise ratio is the signal power to the noise power. The capturing method and averaging are the same as in section 5.4 when the carrier frequency was varied. The parameters that did not change during the measurement are summarized in Table 17.

Table 17 Measurement Parameters

Parameter	Value	Unit
Modulator Number	3	
Amplified Thermal Noise Level	-45.8	dBm
Carrier Frequency	1.5	GHz
Symbol Rate	25	Msp/s
Baseband Shaping	None	
DVB Sample Frequency	80	MHz

The measured frequency spectrum of the modulated signal is plotted in Figure 85. The signal-to-noise ratio is 10.5 dB.

¹⁹ Agilent E4401B 9kHz-1.5GHz Esa-E Series Spectrum Analyser

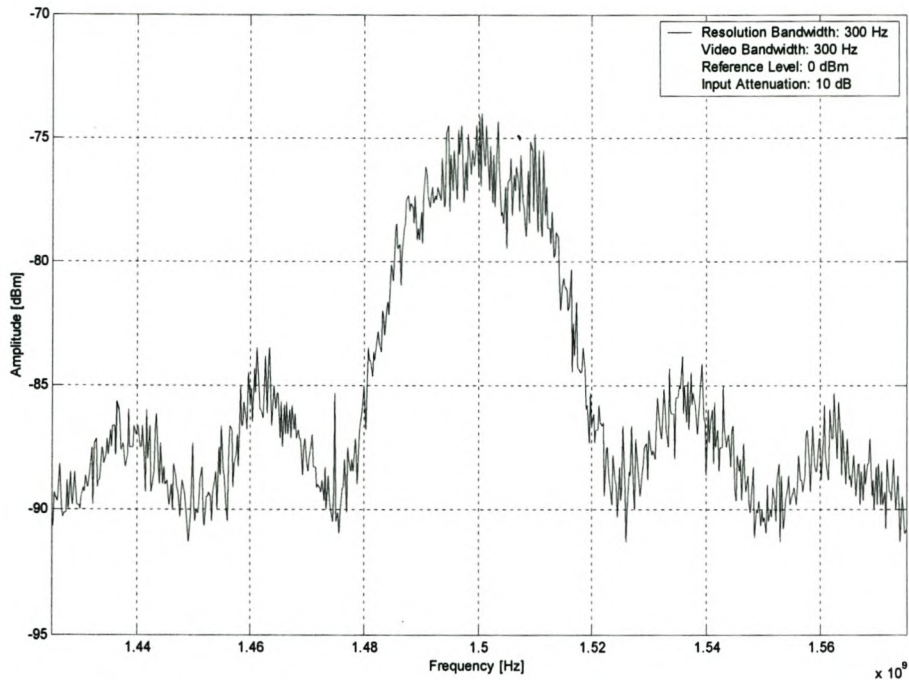


Figure 85 Frequency Spectrum of QPSK Signal in Noise

The noise indicator register gives an indication of the RF signal quality and the noise present in the signal. This register is plotted in Figure 86.

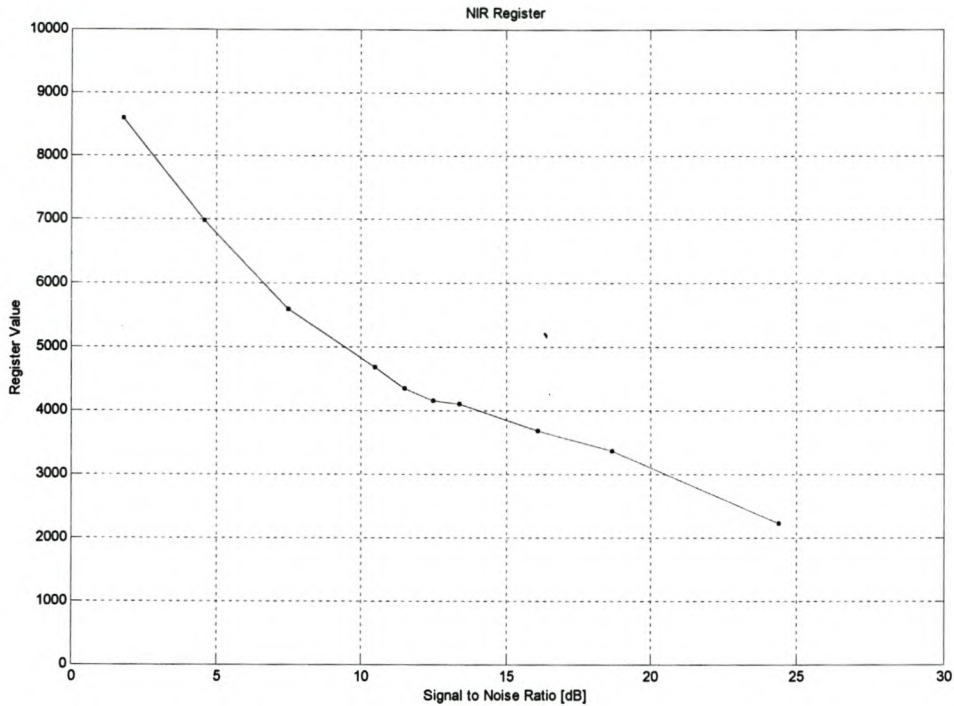


Figure 86 Noise Indicator Register when the Signal-to-Noise Ratio is Varied

The noise indicator register shows that when the signal-to-noise ratio is decreased, the noise indicator value increases. The relationship is not linear, thus in order to gauge the signal-to-noise ratio, a lookup table must be implemented.

Registers CFR and RTF produced a constant value when the signal-to-noise ratio was varied.

Carrier power register AGC_1 is used for high carrier power levels. This register is plotted in Figure 87.

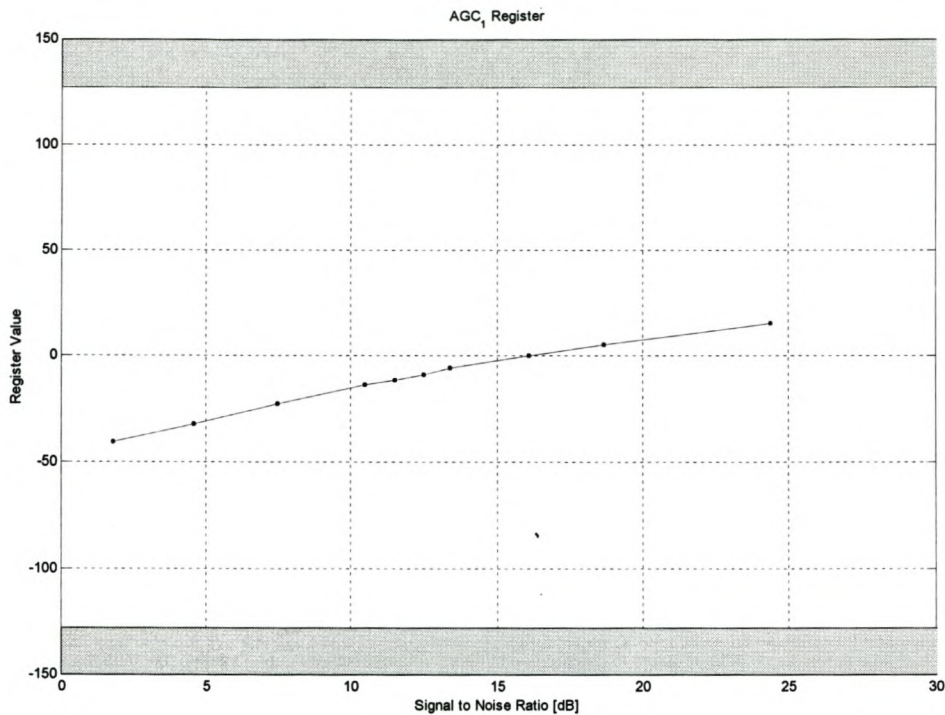


Figure 87 Carrier Power Register (before Filter) when the Signal-to-Noise Ratio is Varied

As would be expected the when the signal-to-noise ratio is varied, the signal power register shows a liner response.

The QPSK bit error rate is calculated from the error count register. This is plotted in Figure 88.

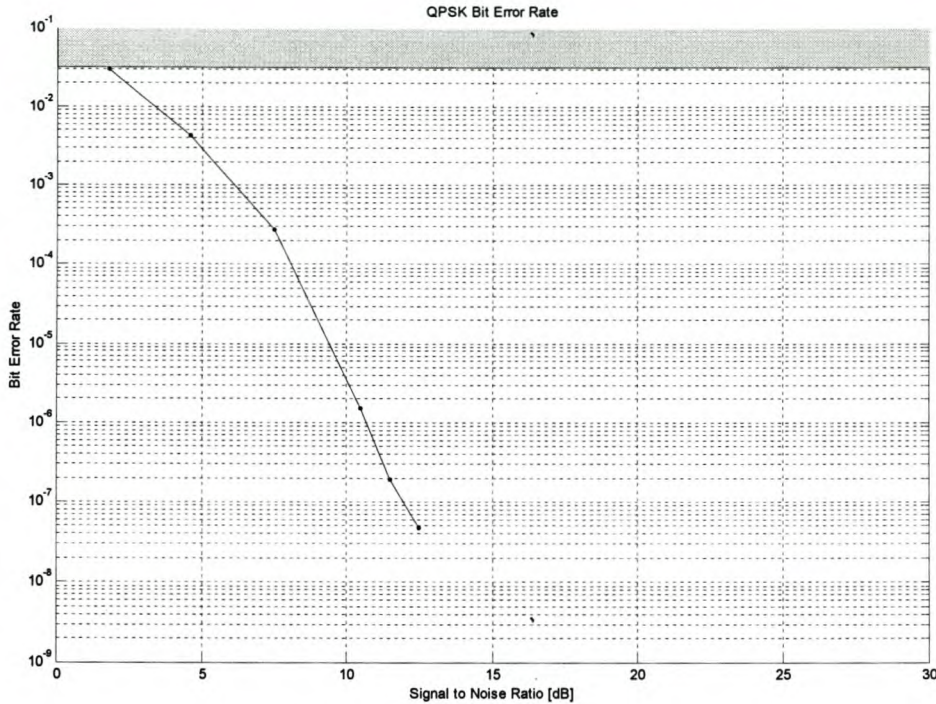


Figure 88 Bit Error Rate when the Signal-to-Noise Ratio is Varied

A signal-to-noise ratio of 13 dB produced error-free transmission. This is adopted as the safe lower signal-to-noise ratio limit. Figure 88 indicates the bit error rate for QPSK errors. When the bit error rate is measured for Viterbi errors, error free transmission was measured until carrier lock failed. Carrier lock failed below a signal-to-noise ratio of 2 dB.

5.9. Summary

The Sancy DVB receiver's optimal characteristics are summarized in Table 18.

Table 18 Optimal Operational Values of DVB Receiver

Parameter	Optimal Range		Unit
	Minimum	Maximum	
Carrier Frequency	1000	2000	MHz
Carrier Power Level	-55	-10	dBm
Symbol Rate	5	35	Msp/s
Signal-to-Noise Ratio	13		dB
Sample Frequency	2 x Symbol Rate	88	MHz

6. System Measurement

The complete communication system will be analyzed in this chapter. The system consists of the custom-developed transmitter and the Sancy DVB receiver. The transmitter is tuned to compensate for inaccuracies and the performance of the system is monitored through custom-developed software, interfacing with the Sancy DVB receiver.

Firstly, the characteristics of a single modulation channel will be investigated. This will be expanded to a double, and later a triple channel system. Four similar channels have been designed but only three was constructed. This allows for an additional channel to be tested on a later stage.

6.1. Single Channel System

Before a multichannel system can be investigated, it is important to determine the characteristics of a single channel system with limited bandwidth.

6.1.1. Limited Bandwidth

The influence of the baseband I and Q channel's bandwidth on the bit error rate (and thus the performance of the system) will be determined. The most logical method to determine this is to keep the data rate constant and vary the low-pass filter's cutoff frequency. Different filters must be constructed for each data rate in order to do this. An alternative method is to use a fixed low-pass filter and vary the data rate.

In section 5.6 the symbol rate of a system with unlimited bandwidth was varied and the bit error rate recorded. This was compared with a system with limited

bandwidth. Two similar Bessel-Thomson low-pass filters were used to filter the baseband I and Q channels²⁰. The frequency spectrum of a QPSK modulated signal for infinite bandwidth (a) and filtered by a Bessel-Thomson filter (b) is shown in Figure 89.

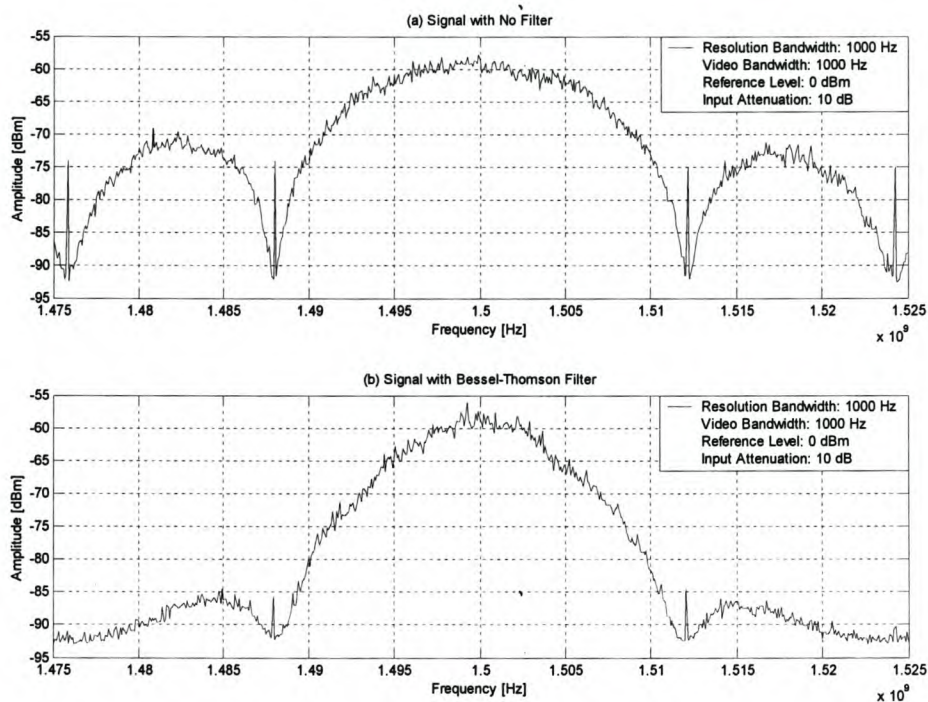


Figure 89 Frequency Spectrum of a QPSK Modulated Signal where Baseband is Filtered by Bessel-Thomson Filters (b) and for Unlimited Bandwidth (a).

When a QPSK modulated signal is filtered by a brickwall filter, the influence of limited bandwidth become apparent on the bit error rate of the system. The Monte Carlo simulation of such a system is shown in Figure 90. The carrier frequency is 2 GHz and the simulation was executed with a total symbol count of 10000 symbols. The Matlab source code is included on the accompanying CD.

²⁰ The filters were described in section 4.7

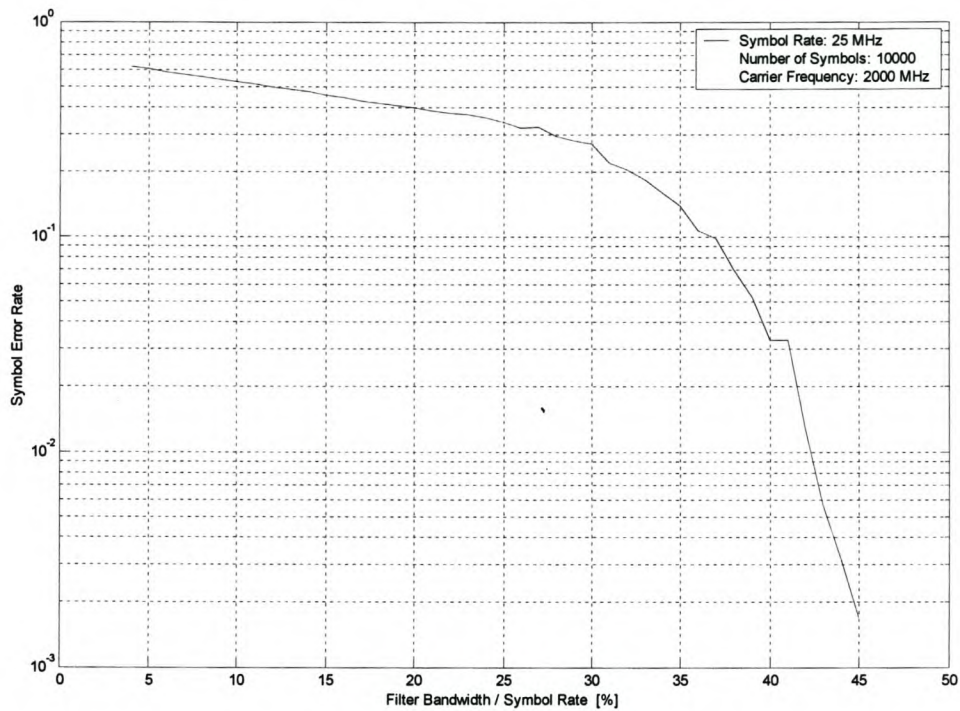


Figure 90 Monte Carlo Simulation to Indicate the Influence of Filter Bandwidth on SER

Figure 90 suggests that the bandwidth required for a QPSK system is 2 bps/Hz. In other words, the bandwidth required for the transmission of 25 Msps (or 50 Mbps) is 25 MHz. This confirms the theoretical effective bandwidth of 2 bps/Hz as given in Table 1. The effective bandwidth is depicted in Figure 91.

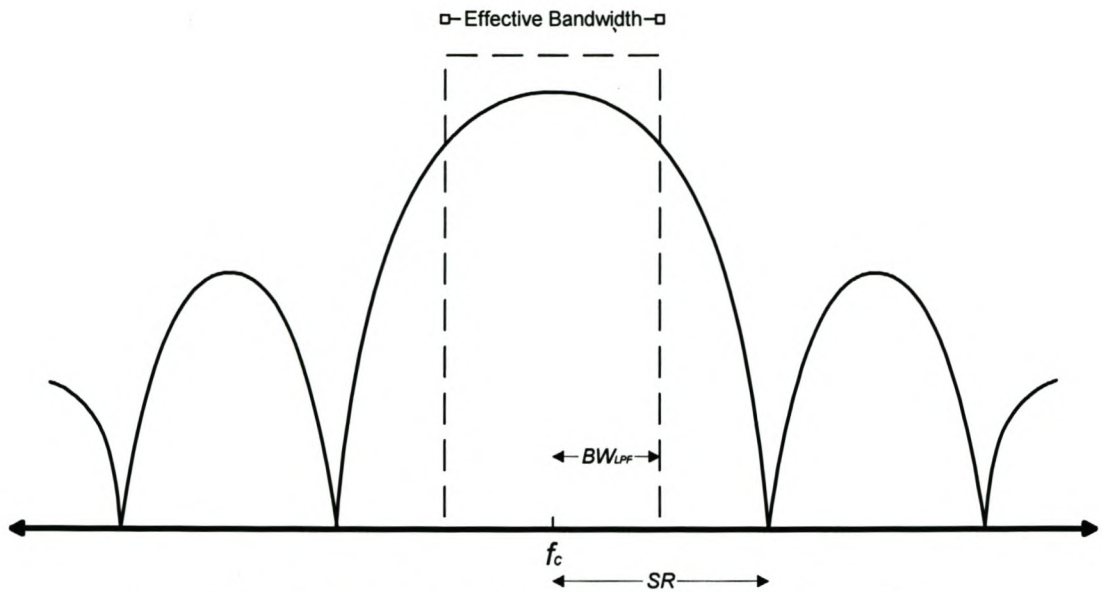


Figure 91 Effective bandwidth of QPSK Modulated Signal

Figure 92 contains the bit error rate plot when the baseband I/Q channels are shaped by the constructed Bessel-Thomson filter. The measurement parameters are summarized in Table 19. A bit error rate of zero was omitted from the logarithmic plot.

Table 19 Measurement Parameters

Parameter	Value	Unit
Modulator Number	2	
Carrier Power	-32	dBm
Baseband Shaping	6 MHz Bessel-Thomson Filter	
DVB Sample Frequency	80	MHz

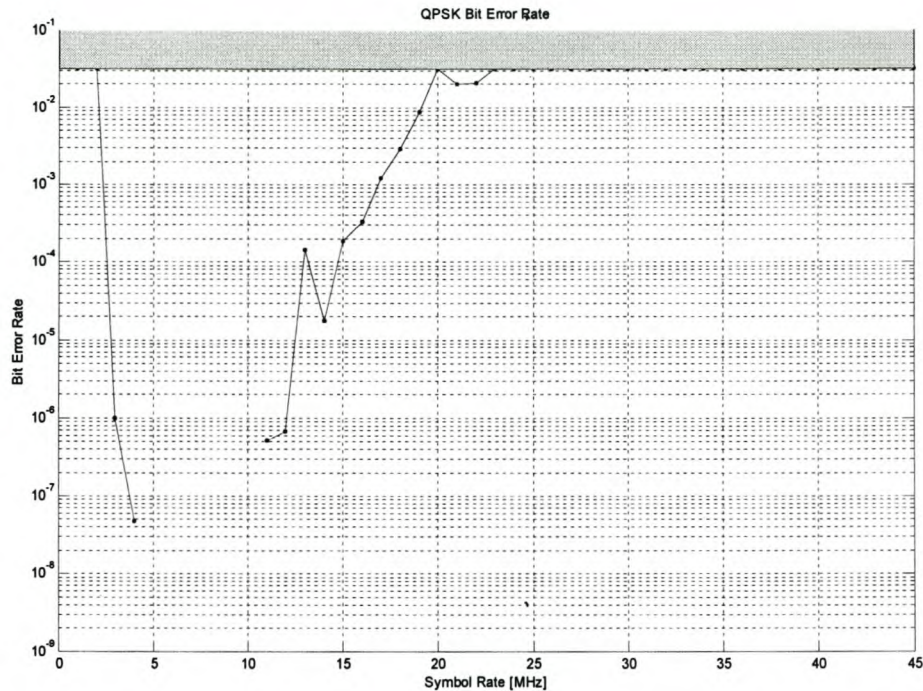


Figure 92 Influence of Symbol Rate on BER in system with Limited Bandwidth

The bandwidth of the Bessel-Thomson filter is 6 MHz. According to Figure 90 the bit error rate should start to increase at 12 Msps. This is confirmed by Figure 92. The high bit error rate at low symbol rates is caused by the Sancy DVB receiver's inability to operate at these low symbol rates.

When the constructed Chebyshev filter with a cutoff frequency of 25 MHz was used, no influence on the bit error rate was noticed. The bit error rate should start to increase at twice the filter's cutoff frequency. This symbol rate of 50 Msps is above the operating limit of the Sancy DVB receiver.

6.2. Double Channel System

When two QPSK modulated signals are placed alongside each other on the frequency spectrum they influence one another to some degree. To what extent will be determined and the optimal carrier spacing will be found. Firstly, the case of unlimited bandwidth will be examined. Secondly, a system with limited bandwidth will be studied.

6.2.1. Unlimited Bandwidth

The frequency spectrum of a double, QPSK-modulated, channel system is shown in Figure 93. The carrier spacing is equal to the symbol rate.

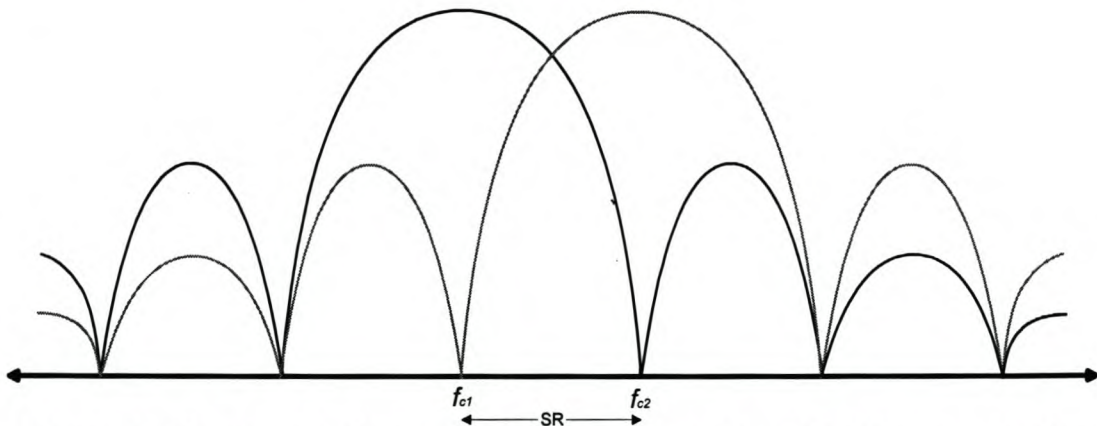


Figure 93 Frequency Spectrum of a Combined Double Channel System

Two QPSK-modulated signals were constructed for a Monte Carlo simulation in Matlab. The carrier spacing between the two signals was varied and the symbol error rate of one channel measured. The symbol rate remained at 25 Msps throughout the simulation. The symbol error rate is plotted in Figure 94.

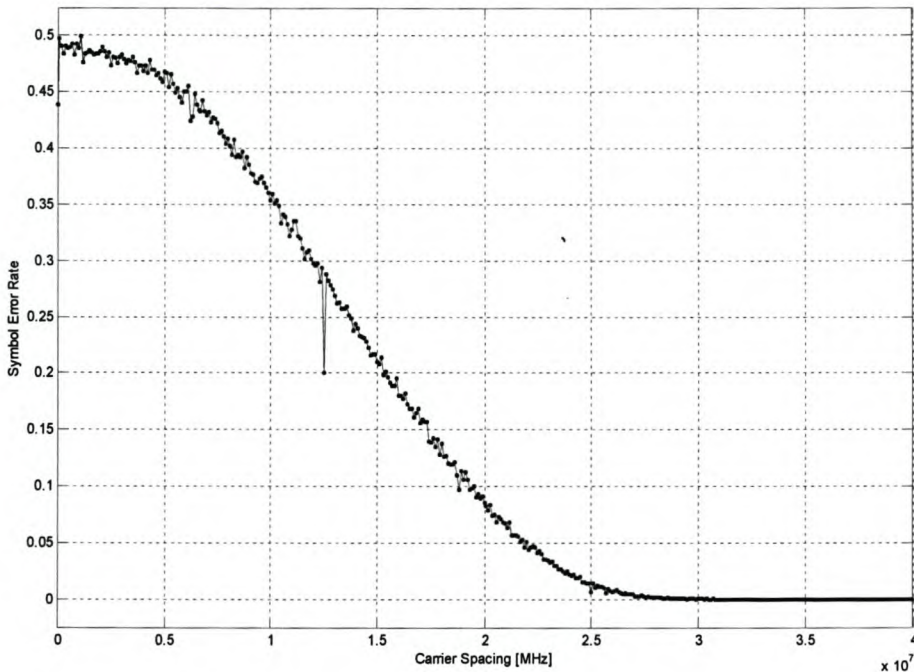


Figure 94 Monte Carlo simulation to indicate the Influence of Carrier Spacing on SER in a Double Channel System

Figure 94 suggest that a carrier spacing between 1 to 1.2 times the symbol rate produced low symbol error rates. This condition is graphically shown in Figure 93.

In the physical system modulators two and three were used to generate each channel signal. The lower carrier frequency remained fixed at 1 GHz and the higher carrier frequency was varied. The Sancy DVB receiver was programmed to receive the fixed lower carrier frequency. When the receiver is locked to a signal, the signal quality is allowed to degrade while carrier lock is maintained. It is thus not preferable to establish lock and vary the carrier spacing continuously. In order to determine if the Sancy DVB receiver is able to lock with a certain amount of interference from a nearby channel, the communication channel between transmitter and receiver was broken for each different spacing. The receiver was then reset and reprogrammed.

The measured frequency spectrum of the combined modulated signals is shown in Figure 95. The lower carrier frequency is 1 GHz and the difference between the carrier frequencies are 20 MHz. The symbol rate of each channel is 10 Msps.

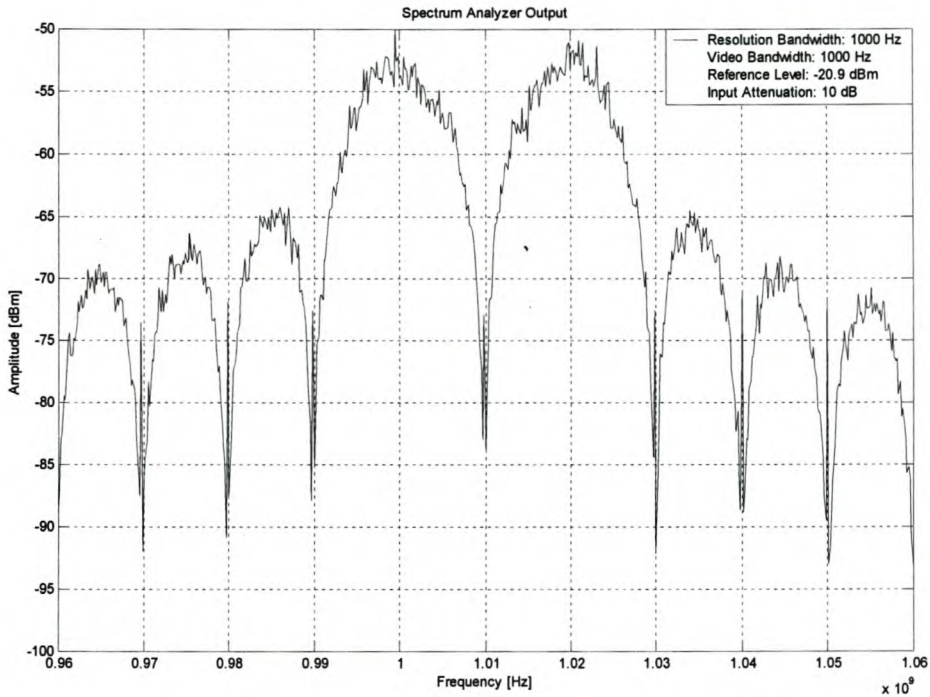


Figure 95 Frequency Spectrum of a Combined Double Channel System

The recorded bit error rate is plotted in Figure 96. The measurement parameters are summarized in Table 20. The choice of symbol rate will be discussed later in this section.

Table 20 Measurement Parameters of a Double Channel System with Unlimited Bandwidth

Parameter	Value	Unit
Symbol Rate	10	Mpsps
Modulator Number	2,3	
Carrier Power	-32	dBm
Fixed Carrier Frequency	1	GHz
DVB Sample Frequency	80	MHz

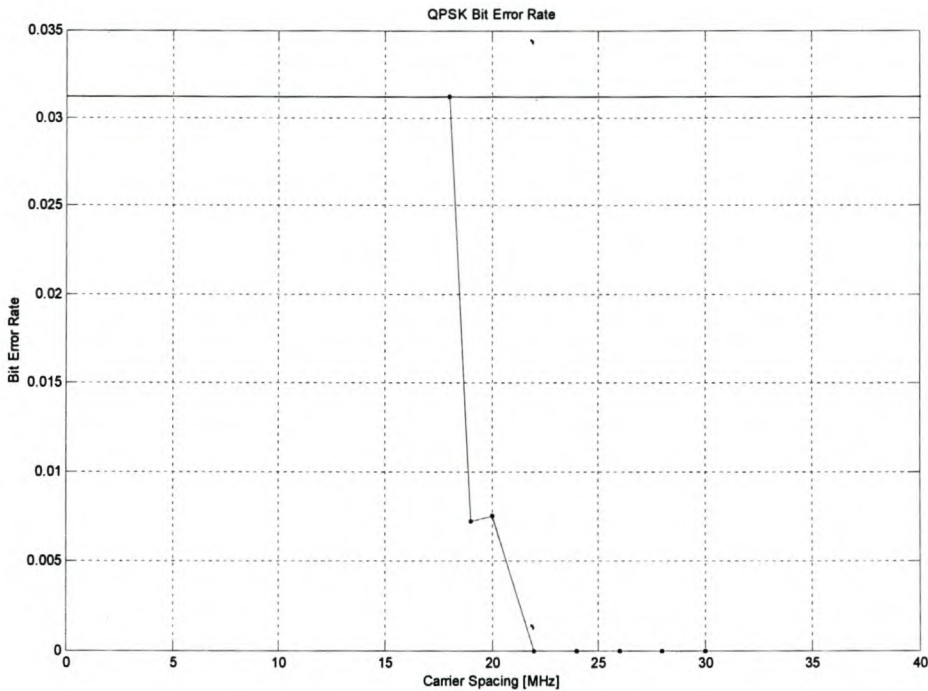


Figure 96 Influence of Carrier Spacing on BER in a Double Channel System with Unlimited Bandwidth

Figure 96 indicates that transmission with a carrier spacing greater than 2.2 times the symbol rate was error free. According to Figure 94 the minimum carrier spacing is equal to the symbol rate. In the practical system the Sancy DVB receiver is not able to obtain lock below 18 MHz (or 1.8 times the symbol rate).

6.2.2. Limited Bandwidth

A double channel system was simulated in Matlab by means of the Monte Carlo method. The carrier spacing between the two signals was varied and the symbol error rate of one channel measured. The baseband I/Q channels were fixed at 25 Msps and several brickwall filters were applied. The filter bandwidth ranged from 12.5 MHz to infinity. The symbol error rate is plotted in Figure 97.

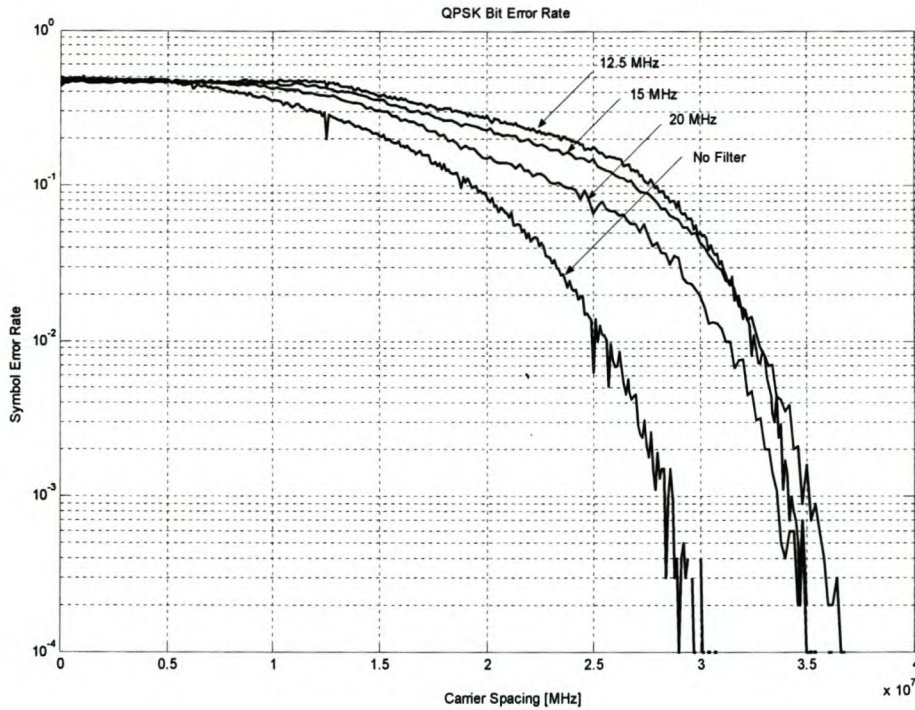


Figure 97 Monte Carlo Simulation to Indicate the Influence of Carrier Spacing on SER in a Double Channel System with Limited Bandwidth

The symbol error rate is related to the filter bandwidth. When the system with a 12.5 MHz filter is examined, it is clear that the maximum error rate occurs when the carrier spacing is below 12.5 MHz. This condition is shown in Figure 98.

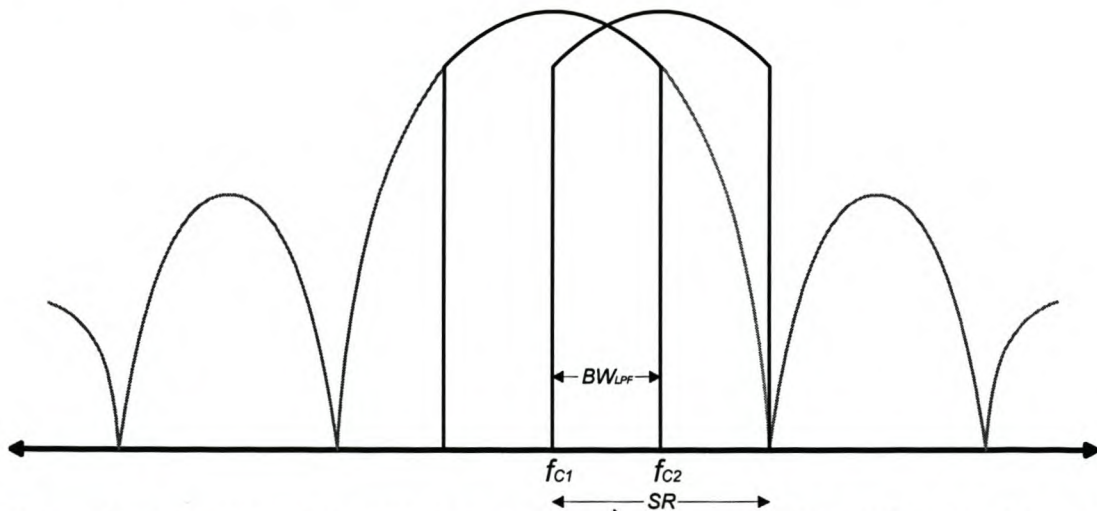


Figure 98 Combined Double Channel Spectrum with Small Carrier Spacing

When one carrier spacing is considered in Figure 97, it is clear that the symbol error rate increases as the filter bandwidth decreases. This is due to the fact that a brickwall filter was used. Unless special techniques are applied, an increase in the Q-factor of a baseband filter will cause an increase in the intersymbol interference. In Figure 97 the combination of intersymbol interference and a decrease in bandwidth caused the symbol error rate to increase.

When a perfect brickwall filter is applied, it is expected to receive no errors when the carrier spacing is above 25 MHz (since the two modulated signals are completely separated). Figure 97 shows that this was not the case. As shown by the block diagram in Figure 5, the demodulator has an internal filter with a bandwidth equal to the symbol rate. When the difference between the filter spacing and the I/Q channel bandwidth is smaller than the symbol frequency, interference from the nearby channel is present. This is graphically illustrated in Figure 99.

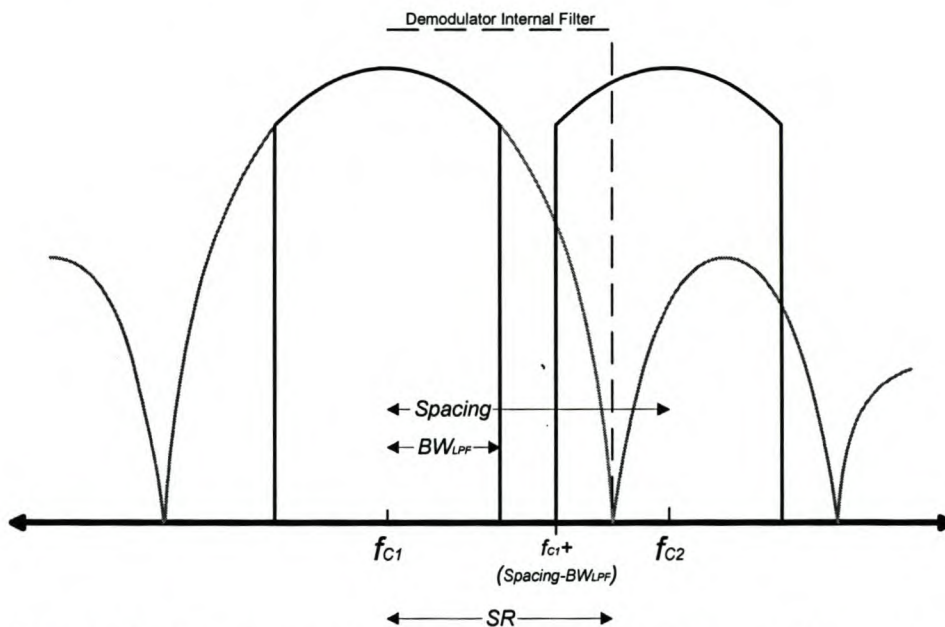


Figure 99 Frequency Spectrum of Double Channel System and Demodulator's Internal Filter Bandwidth

In the physical system, the same method that was explained in section 6.2.1 was followed. The four baseband I/Q channels were filtered by the constructed Bessel-Thomson filters, numbered $B1$ through $B4$. The measured frequency spectrum of the combined modulated signals is shown in Figure 100. The lower carrier frequency is 1 GHz and the carrier spacing is 20 MHz. The symbol rate was chosen as 10 Msps.

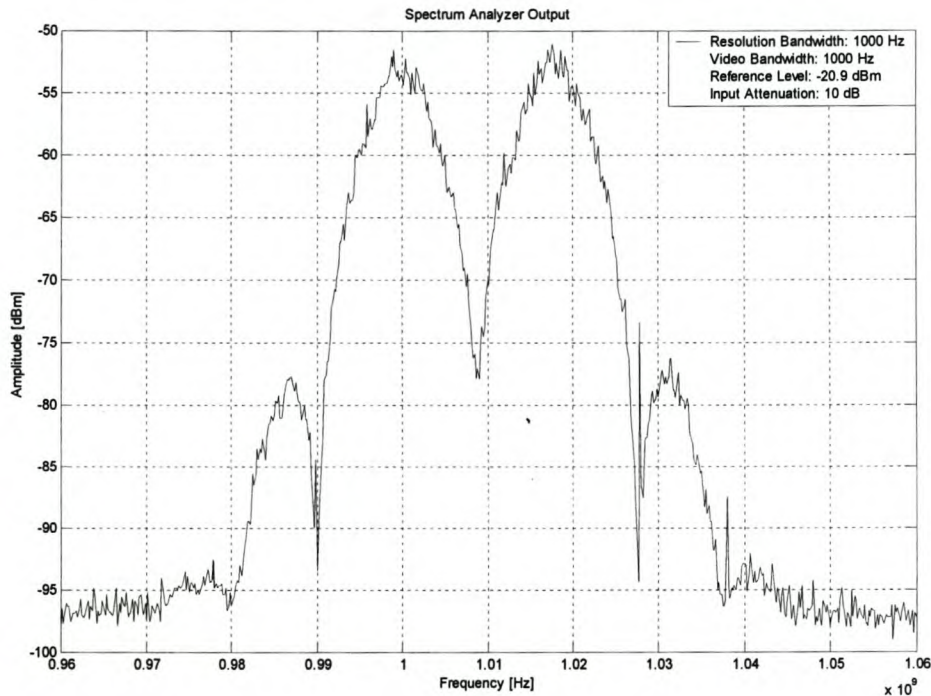


Figure 100 Frequency Spectrum of a Double Channel System with Limited Bandwidth

According to Figure 92 (with the filter present), a symbol rate between 5 Msps and 10 Msps produced the best bit error rate. The symbol rate was chosen as 10 Msps. The measured bit error rate when a filter is used is compared with a system with unlimited bandwidth in Figure 101. The measurement parameters are the same as in Table 20. A bit error rate of zero was omitted from the logarithmic plot.

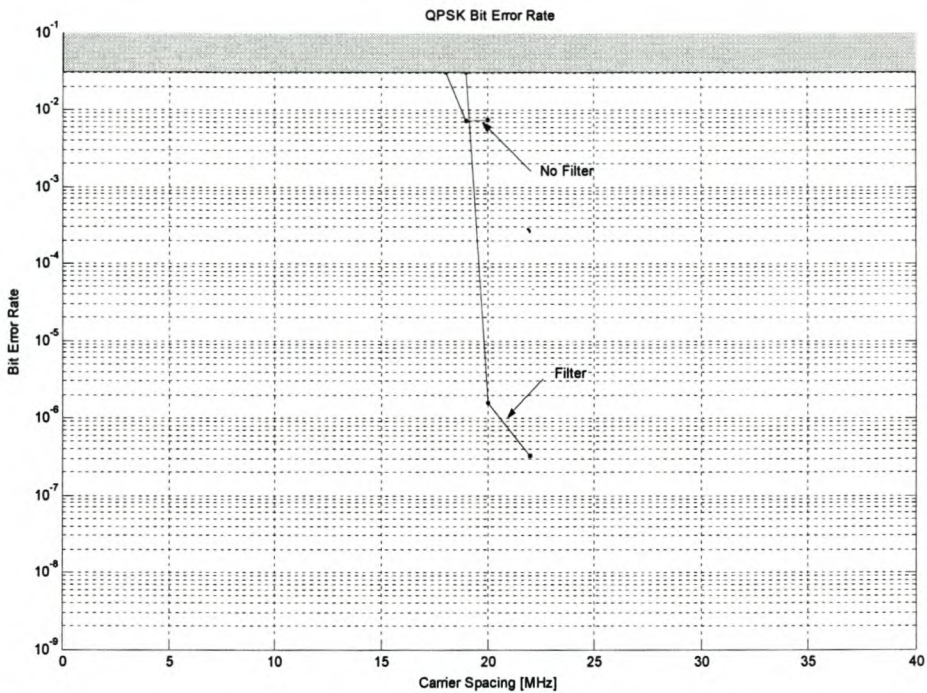


Figure 101 Influence of Carrier Spacing on BER in a Double Channel System with Limited Bandwidth

The Sancy DVB receiver was not able to obtain carrier lock at spacings below 20 MHz. When the frequency spectrum of Figure 100 is compared with Figure 95, it is clear that filtering causes the QPSK signal to deform. This deformation, in combination with the interference from a nearby channel, caused the minimum channel spacing to increase. The difference is so small that it would be acceptable to conclude that the influence of limited bandwidth does not significantly affect the minimum carrier spacing.

6.3. Triple Channel System

The system of two QPSK-modulated signals is now extended to a three channel system. The cases of unlimited and limited bandwidth will again be considered.

6.3.1. Unlimited Bandwidth

The frequency spectrum of a triple channel QPSK-modulated system with unlimited bandwidth is shown in Figure 102. The carrier spacing is equal to the symbol rate.

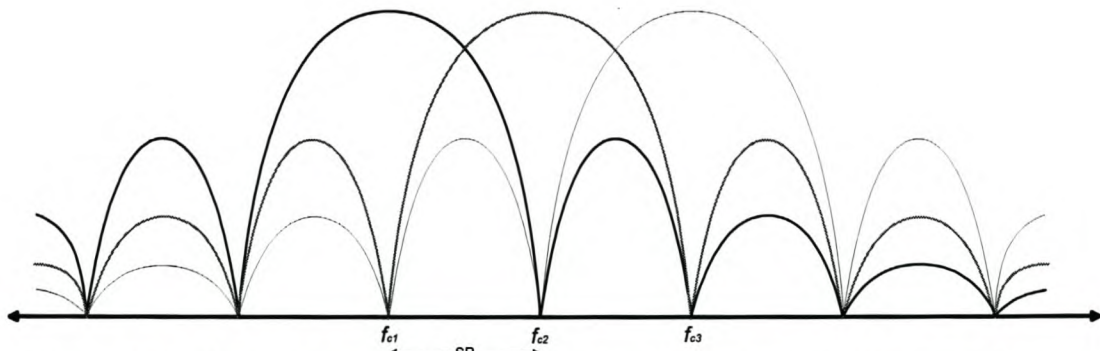


Figure 102 Frequency Spectrum of a Combined Triple Channel System

Three QPSK-modulated signals were constructed for a Monte Carlo simulation in Matlab. The carrier spacing between the three signals was varied and the centre channel's symbol error rate measured. The symbol rate for each of the three channels was 25 Mps. The symbol error rate is plotted in Figure 103.

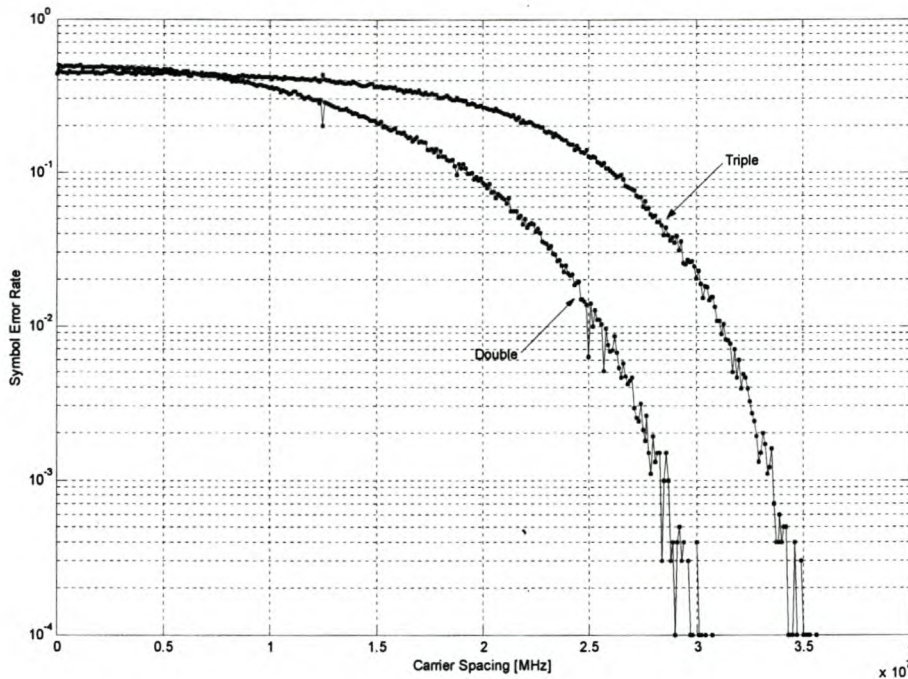


Figure 103 Monte Carlo Simulation to Indicate the Influence of Carrier Spacing on SER in a Double and Triple Channel System

Figure 103 indicates that the minimum channel spacing for a triple system is 37 MHz, or approximately 1.5 times the symbol rate. When the triple system is compared with the double system, it is clear that the influence from the nearby channels on both sides increased the minimum channel spacing.

When the bit error rate was measured for different carrier spacings in the physical system, modulators numbered two, three and four were used. The symbol rate remained fixed and the carrier frequency of modulator number two was kept constant at 1 GHz. The Sancy DVB receiver was programmed to receive this signal. The transmission path was again broken and the receiver was reset and reprogrammed for each data point. The carrier frequencies of modulators numbered three and four were varied. A photograph of the measurement setup is shown in Figure 104.

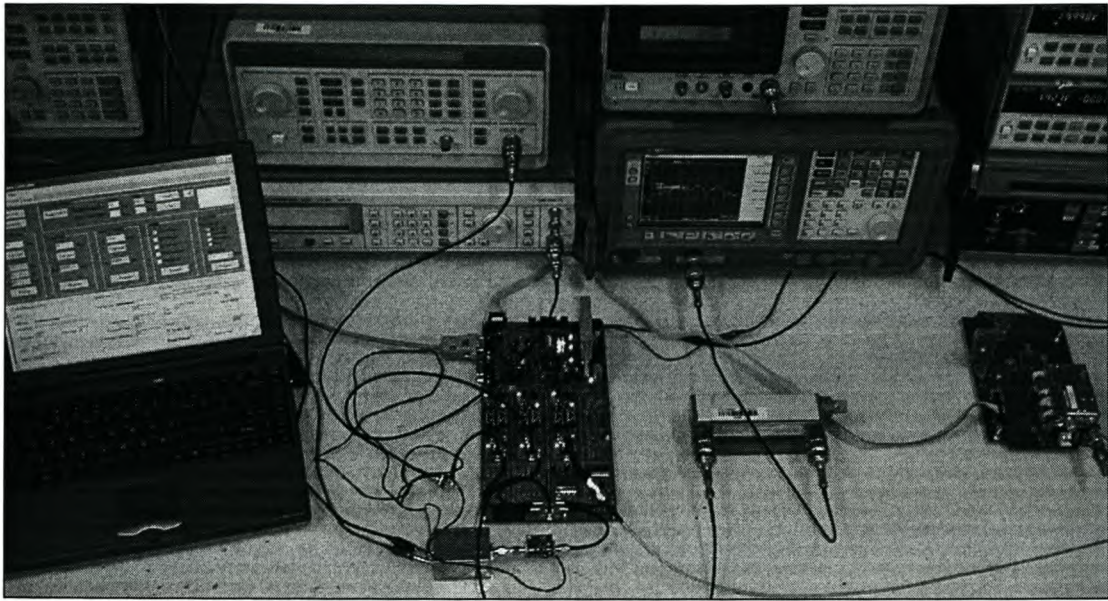


Figure 104 Photograph of Triple Channel Measurement Setup

The measured frequency spectrum of the triple channel system with unlimited bandwidth is shown in Figure 105. The centre carrier frequency is 1 GHz and the carrier spacing in both directions is 10 MHz. The symbol rate of each channel is 10 Msps.

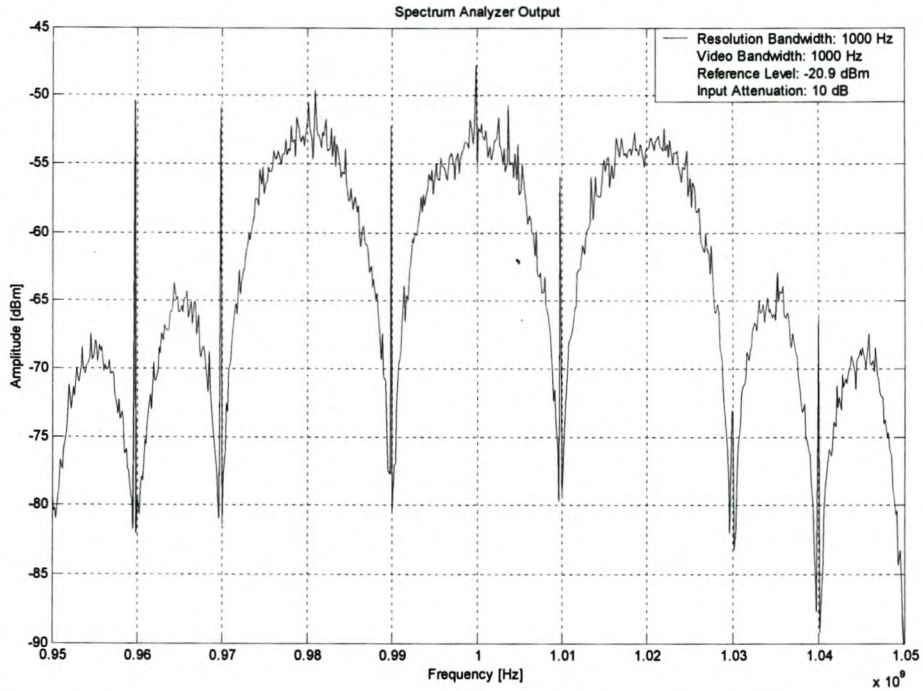


Figure 105 Frequency Spectrum of a Combined Triple Channel System

The measured bit error rate for a double and triple system is plotted in Figure 106. The measurement parameters are summarized in Table 21. A bit error rate of zero was omitted from the logarithmic plot.

Table 21 Measurement parameters of a Triple Channel System with Unlimited Bandwidth

Parameter	Value	Unit
Symbol Rate	10	Mbps
Modulators used	2,3,4	
Carrier Power	-32	dBm
Fixed Centre Carrier Frequency	1	GHz
DVB Sample Frequency	80	MHz
Baseband Shaping	none	

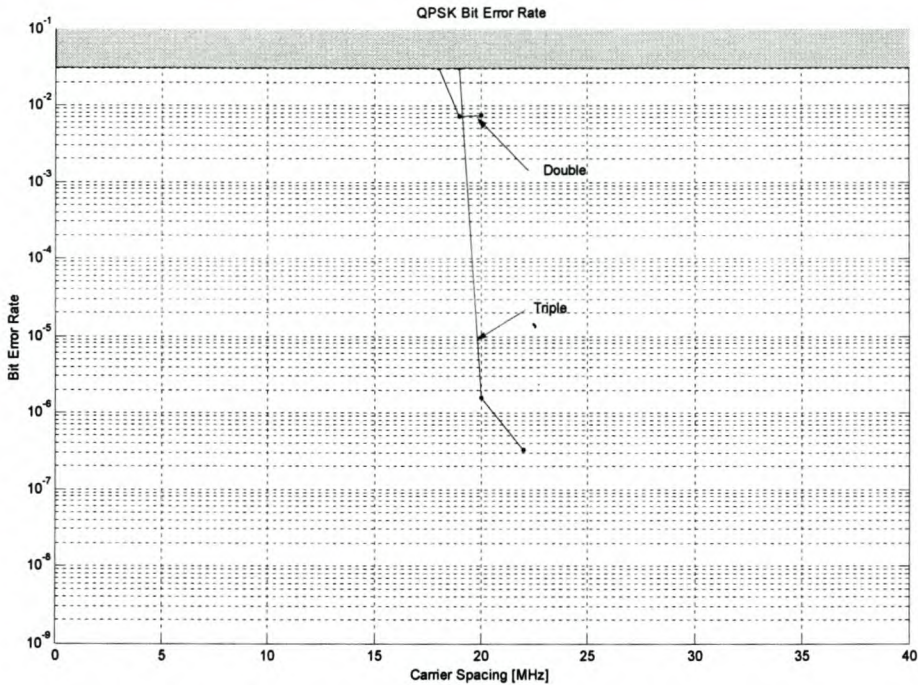


Figure 106 Influence of Carrier Spacing on BER in a Triple Channel System with Unlimited Bandwidth

Figure 106 indicates that the minimum carrier spacing increased for a triple system. This was predicted in Figure 103 since interference was present from both sides. Figure 103 indicates that a carrier spacing greater than 1.5 times the symbol rate produced no errors. According to Figure 106 a carrier spacing above 22 MHz (2.2 times the symbol rate) is error-free. In the practical system the Sancy DVB receiver did not obtain lock below 20 MHz.

In order to determine the influence of noise on such a system the carrier spacing was chosen as the minimum carrier spacing of 2.2 times the symbol rate and the signal to noise ratio varied.

The frequency spectrum of a triple channel system with noise present is shown in Figure 107. The signal-to-noise ratio is 13.5 dB.

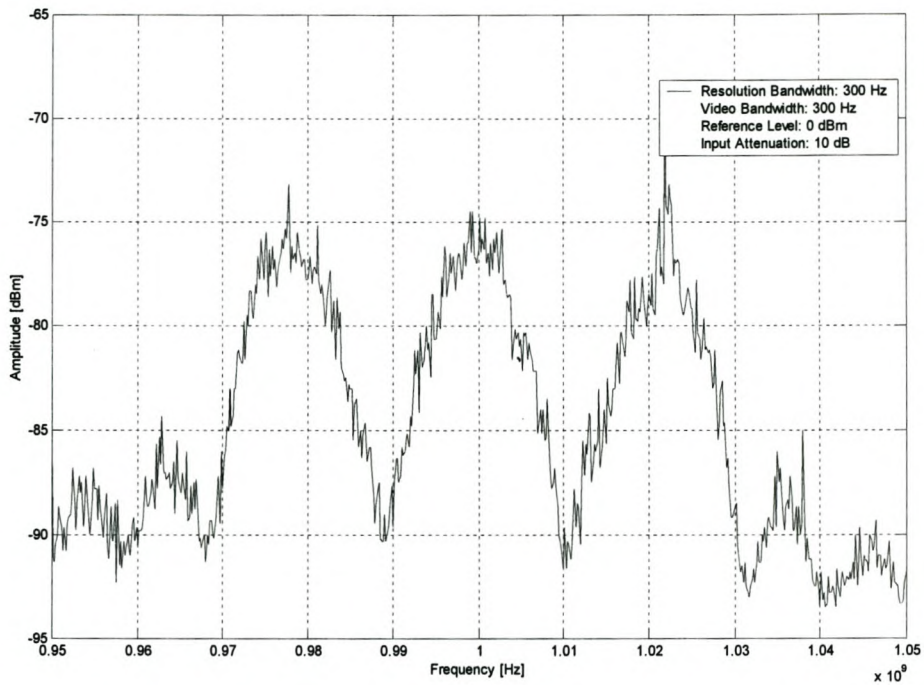


Figure 107 Frequency Spectrum of Triple Channel System with Noise

The measurement setup and procedure were similar to the signal-to-noise measurement in section 5.8. The NIR register is plotted in Figure 108.

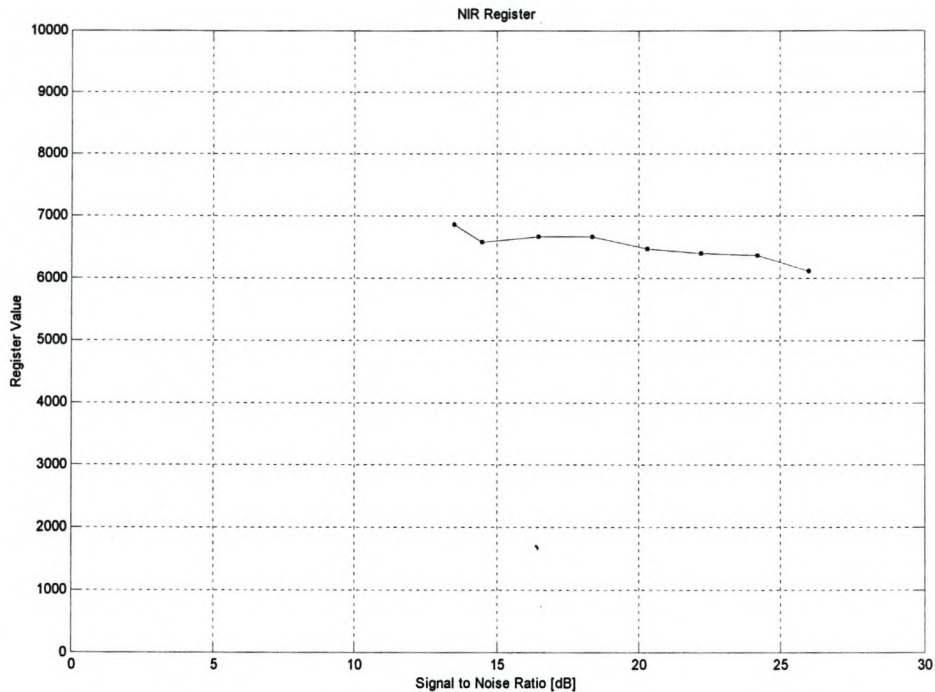


Figure 108 Influence of SNR on NIR Register in a Triple Channel System with Unlimited Bandwidth

When Figure 108 is compared to Figure 86 it is clear that more noise is present for a similar signal-to-noise ratio. This is caused by the interference from adjacent channels.

The measured QPSK bit error rate is plotted Figure 109.

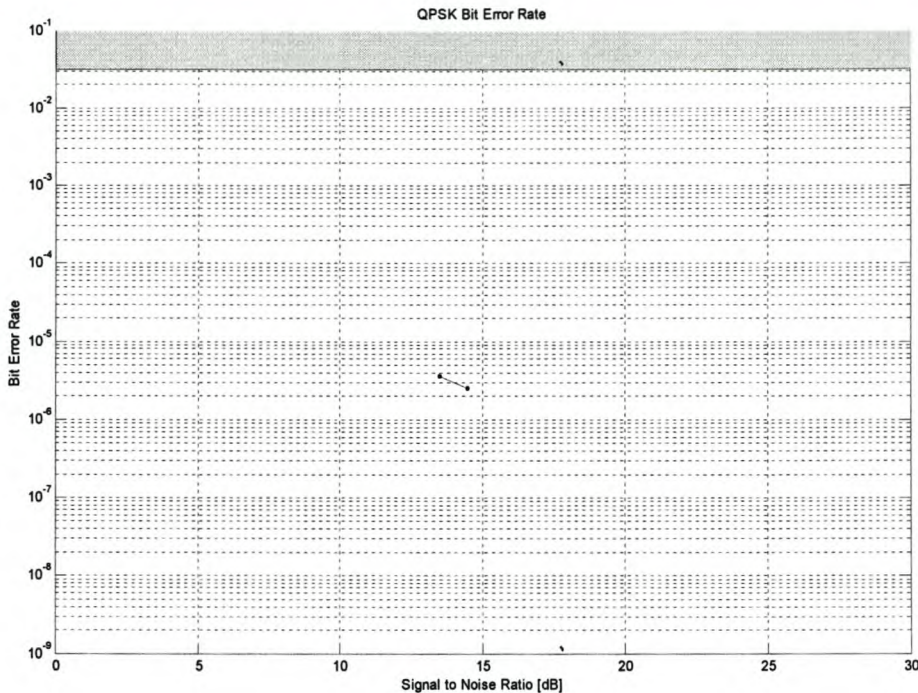


Figure 109 Influence of SNR on BER in a Triple Channel System with Unlimited Bandwidth

Error-free transmission occurs at a signal-to-noise ratio of 15 dB. This increase from the previously determined signal-to-noise ratio limit is caused by the interference from the adjacent channel. Again, the errors measured was QPSK bit errors. When Viterbi errors was measured, error-free transmission occurred until carrier lock was lost. Carrier lock was lost at a signal-to-noise ratio below 13.5 dB.

6.3.2. Limited Bandwidth

The triple channel system was simulated in Matlab by means of the Monte Carlo technique. The three modulators' baseband signals were filtered with a 12.5 MHz brickwall filter. The symbol rate was measured each time the carrier spacing between the two signals was varied. A symbol rate of 25 Msps was used. The frequency spectrum of such a system is shown in Figure 110.

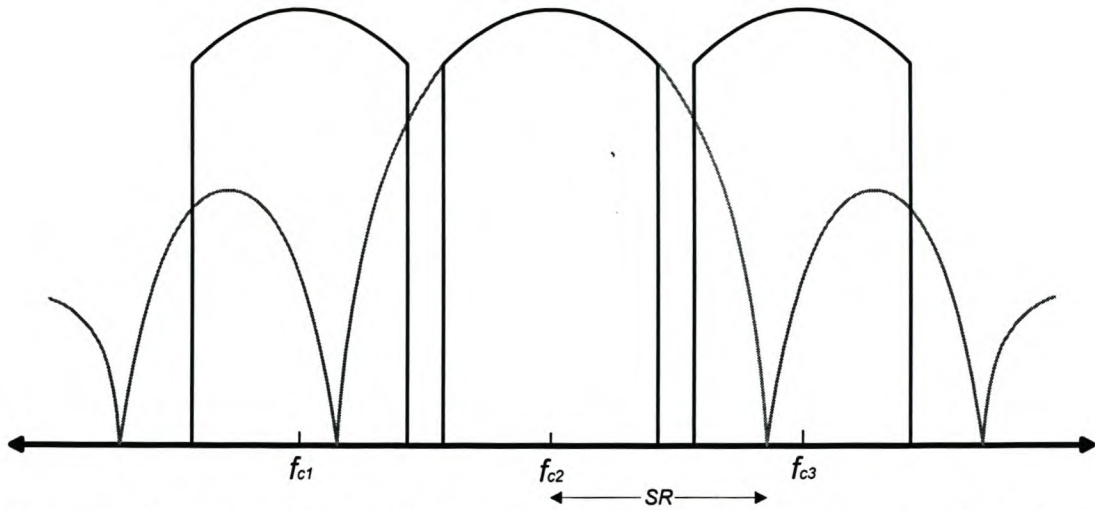


Figure 110 Frequency Spectrum of a Triple Channel System with Limited Bandwidth

The simulated bit error rates of the triple and double channel systems of section 6.2.2 are compared in Figure 111.

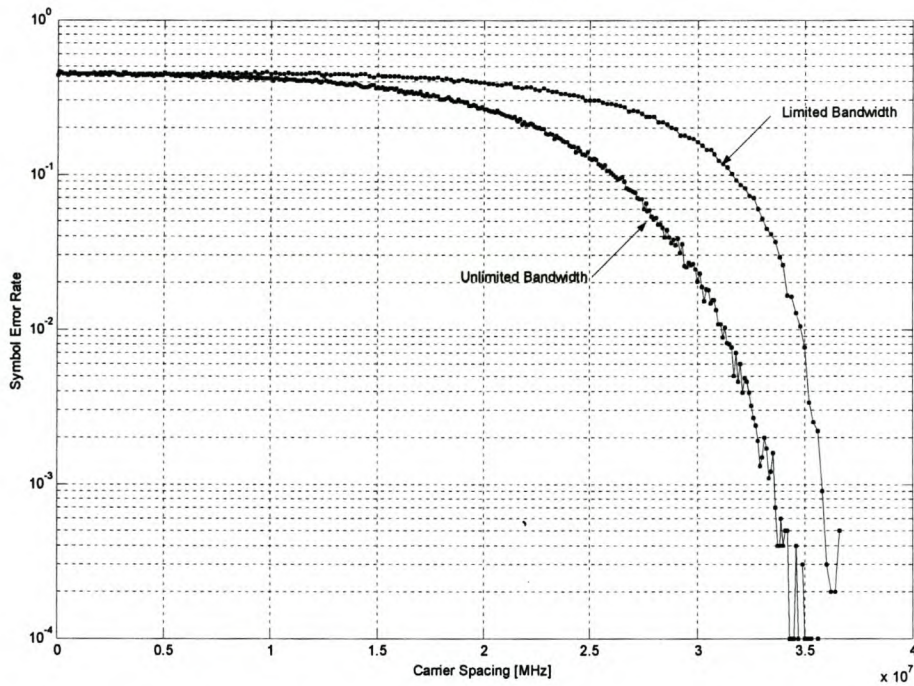


Figure 111 Monte Carlo simulations to indicate the Influence of Carrier Spacing on SER in a Triple Channel System with Limited Bandwidth

When the bandwidth of a double channel system is limited, the bit error rate increases. The same holds for a triple system.

In the physical system, the same method that was explained in section 6.3.1 was followed. The six baseband I/Q channels were filtered by the constructed Bessel-Thomson filters, numbered $B1$ through $B6$. The frequency spectrum of such a system is shown in Figure 110. The carrier frequencies, spacing and symbol rate were the same as in section 6.3.1.

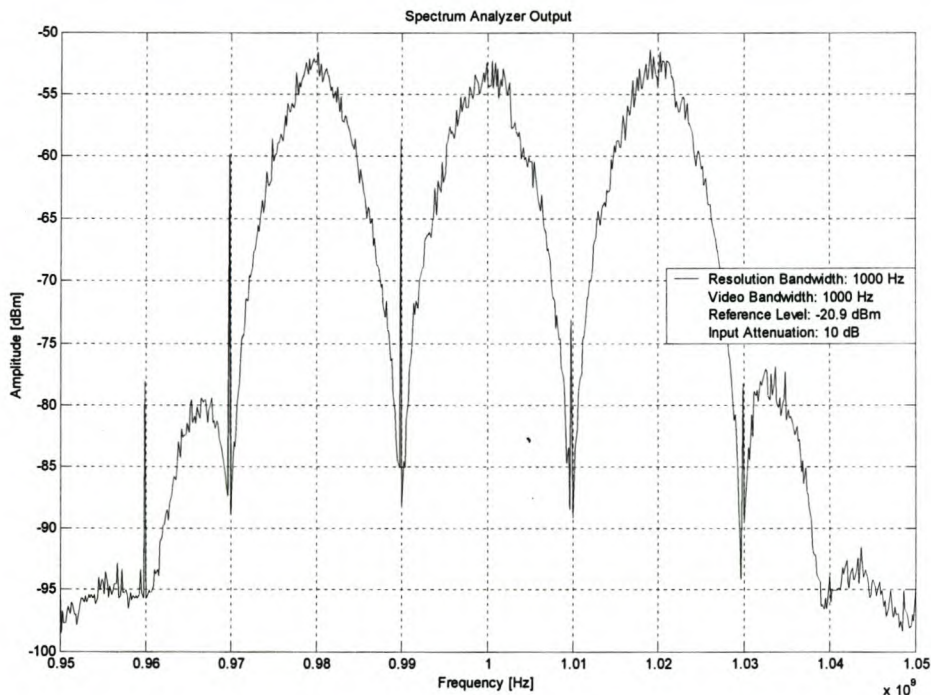


Figure 112 Frequency Spectrum of a Triple Channel System with Limited Bandwidth

The measured bit error rate is plotted in Figure 113 when a filter is used and for unlimited bandwidth. The measurement parameters are the same as in Table 21. A bit error rate of zero was omitted from the logarithmic plot.

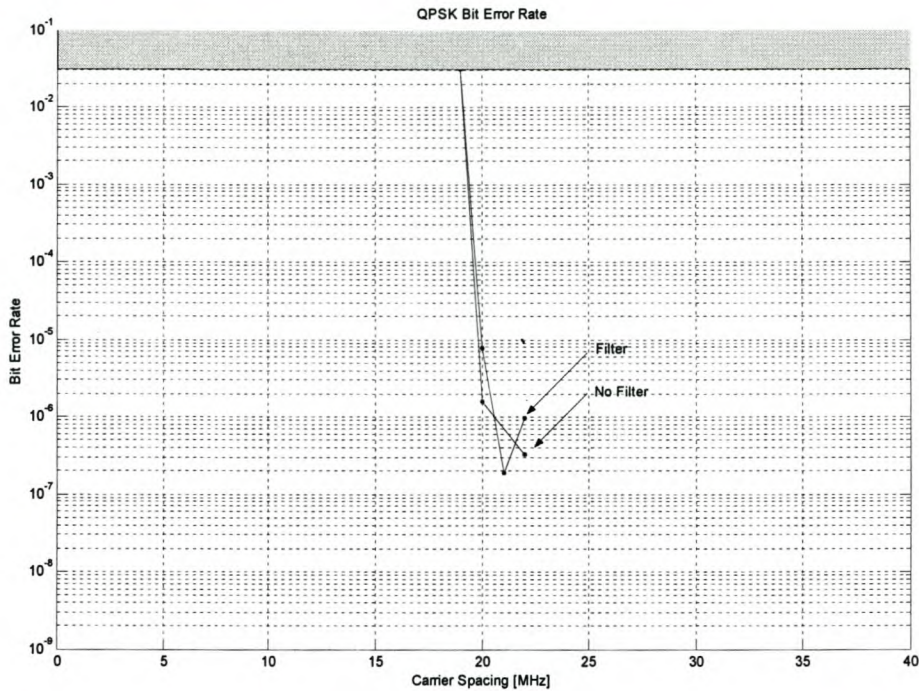


Figure 113 Influence of Carrier Spacing on BER in a Triple Channel System with Limited Bandwidth

The Sancy DVB receivers are not able to obtain carrier lock at spacings below 20 MHz. According to Figure 113, the minimum carrier spacing is above 2.2 times the symbol rate. The same is observed when the bit error rate of a system with filters is compared to a system without filters. The loss due to filter deformation is thus small enough to have no influence on the carrier spacing.

7. Conclusion & Recommendations

7.1. Research Results

Several inaccuracies exist in a QPSK transmitter. These influence the performance of the transmitter and the communication system. The possible inaccuracies identified are: amplitude mismatch, DC-offset, oscillator leakthrough, phase error and limited bandwidth. These inaccuracies were treated theoretically and a method of compensation was identified for each one. A simulation tool, that visually displays the combined influence of the inaccuracies on a communication system, was developed in Matlab.

A QPSK transmitter was custom-developed. The data rate and carrier frequency are variable and are controlled with custom-developed software from a personal computer. The transmitter was constructed with four similar modulation channels. The inaccuracies in each channel were compensated for. Each channel is equipped with a socket for different baseband filters. The output of all the channels is combined before transmission.

A Sancy DVB receiver unit was used in the custom-developed receiver. The receiver is programmed through the microcontroller on the transmitter circuit board with specially developed software on a personal computer. The demodulation status, signal quality and other status parameters are visually displayed by the software. The performance of the Sancy DVB receiver was characterized. This was done in order to determine the influence of varying transmitter parameters.

The performance of the communication system was determined for different transmitter configurations. Double and triple modulation channel systems were

analyzed. The bandwidth of each was varied and the minimum carrier spacing determined. The results are summarized in Table 22. The symbol rate is represented by SR .

Table 22 Summary of Communication System Results

		Minimum Carrier Spacing of Double Channel System	Minimum Carrier Spacing of Triple Channel System
Unlimited Bandwidth	Simulated	$1.2 \times SR$	$1.4 \times SR$
	Measured	$2.2 \times SR$	$2.2 \times SR$
Limited Bandwidth	Simulated	$1.5 \times SR$	$1.55 \times SR$
	Measured	$2.2 \times SR$	$2.2 \times SR$

The simulated performance of an unlimited double channel was compared with that of a triple channel system. The minimum carrier spacing increased when an additional channel was added. This result was predictable since more interference was present.

For the same systems with limited bandwidth, similar results were obtained. This was not predicted since the filtered signals were completely apart. The demodulator has an internal low-pass filter with bandwidth equal to the symbol rate. If the carrier spacing of an adjacent channel was below two times the symbol rate, the adjacent channel was within the demodulator's bandwidth. Thus the minimum carrier spacing increased when an additional channel was added, since extra interference was added.

The simulated minimum carrier spacings of a system with unlimited and of a system with limited bandwidth were compared. The spacing increased when the bandwidth was limited. This was due to the fact that a brickwall filter was used for baseband shaping. Usually an increase in the Q-factor factor of a baseband filter will cause an increase of the intersymbol interference. Special digital filters exist with a

high Q-factor and low intersymbol interference. The combination of intersymbol interference and limited bandwidth caused the minimum carrier spacing to increase.

The minimum carrier spacing in the physical system remained constant. The Sancy DVB receiver was not able to obtain carrier lock at a carrier spacing below two times the symbol rate. It might be possible to come closer to the simulated minimum carrier spacing if a different receiver unit is used and if carrier lock is attainable.

The use of a double and triple channel system was investigated in order to determine the feasibility of implementing such a system. The multichannel system was compared with a single channel system, operating at a high symbol rate. The frequency spectrum of both systems is shown in Figure 114.

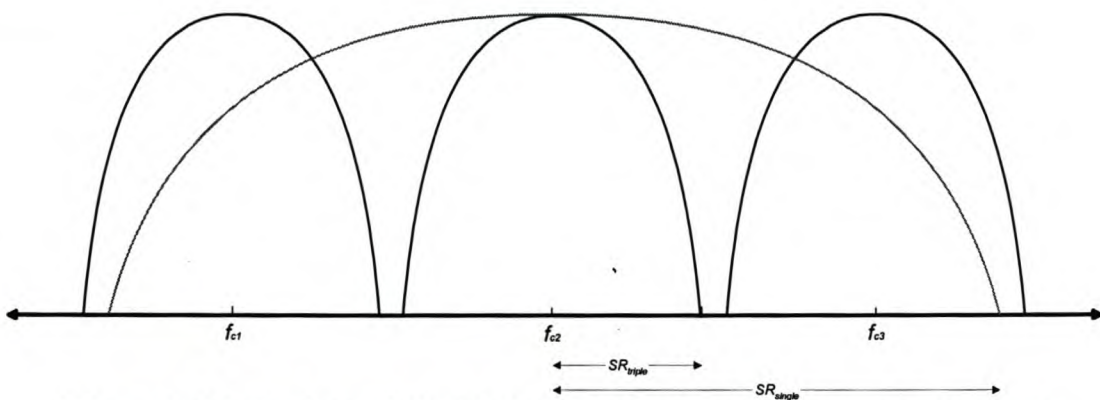


Figure 114 Single and Multichannel System Frequency Spectrum

As an example, a single channel system with a symbol rate of 150 Msps is compared with a triple channel system with a symbol rate of 50 Msps for each channel. It would be possible to space adjacent carriers 100 MHz apart, but it might be difficult to establish carrier lock. For this condition the nil-to-nil bandwidth of the single channel system is 300 MHz. The nil-to-nil bandwidth of a single channel in the triple channel system is 100 MHz. Thus the total occupied bandwidth is 300 MHz, the same as for the single channel system.

As mentioned before, it might be difficult to obtain carrier lock with channel spacing equalling symbol rate. A more conservative minimum carrier spacing would

be 2.2 times the symbol rate (as was suggested in Table 22). The total occupied bandwidth of the triple channel system would then be 320 MHz. This would result in a 7% increase in occupied bandwidth. The frequency spectrum of both systems is shown in Figure 114. This result is true when the occupied bandwidth for the single channel system is the nil-to-nil bandwidth.

7.2. Further Work

This thesis produced a solid foundation for further development. The hardware and software were custom-developed and can be used in further studies. Some recommendations are now made for this:

- At this stage the transmitter is capable of encoding the data with differential encoding. The Sancy DVB receiver is capable of dealing with a number of coding schemes and data scramblers.

The FPGA's source code could be modified to accommodate schemes such as Reed-Solomon encoding [27], convolutional interleaving and energy dispersal [11]. A synchronization word could also be added to the transmitted data [11] in order to confirm the correctness of received data.

- Disadvantages of the receiver circuit board are the following. The receiver circuit board was modified to make the Sancy DVB unit more accessible. This made the receiver less robust. Several voltage levels were required for the receiver. The receiver was also programmed with the microcontroller on the transmitter circuit board. Thus the receiver can not be used as an isolated unit.

In further studies the receiver circuit board can be redesigned to accommodate an accessible Sancy DVB unit, to provide all the voltage

levels from a single supply and to host a microcontroller to program the Sancy DVB unit and interface with a personal computer.

- In this thesis baseband shaping was performed with an analog filter. In order to minimize intersymbol interference a Bessel-Thomson filter was used. A low Q-factor was compulsory in order to obtain a flat phase response. Therefore, the measurement of the influence of limited bandwidth was not a complete success.

In further studies the use of a digital filter could be investigated. A digital filter would give more freedom when the influence of different filters is investigated. A raised-cosine filter will limit interference from an adjacent channel [1, 32].

- In order to determine the performance of a multichannel system, the receiver was custom-developed with one Sancy DVB unit to receive one channel. It was assumed that the other channels would respond similarly to the measured channel.

A receiver could be custom-developed with a Sancy DVB receiver for each channel. The output from the receivers should then be synchronized and combined. If this is possible, the true performance of a multichannel system could be determined.

7.3. Summary

The inaccuracies present in a QPSK system was theoretically examined in this study. The influence of these inaccuracies on the frequency spectrum was also determined. Methods of compensating for inaccuracies were developed and the frequency spectrum was used to measure these.

A multichannel QPSK transmitter was designed and constructed. Software was custom-developed to vary the data rate and the carrier frequencies of the transmitter. The methods developed for inaccuracy compensation was applied when the modulators were tuned.

The Sancy DVB unit was used as receiver. Software was custom-developed in Delphi to program the unit's registers and to visually display the demodulation status on a personal computer.

The Influence of carrier spacing of a double and a triple channel system was determined. The bandwidth was limited with a baseband filter and the performance measured.

It was found that it is preferable to use a multichannel system rather than a single channel system. The occupied bandwidth of a multichannel system is 7% more than the bandwidth occupied by a high speed single channel system. This increase in bandwidth is justified by the decrease in costs. The current cost of a custom-developed high speed demodulator, operating in a specific bandwidth, with fixed symbol rate and intermediate frequency, is R300 000. The cost of one Sancy DVB receiver unit is R60. Thus for a triple channel system, the receiver units would cost only R180. It is estimated that the total receiver costs would be less than 0.2% of the cost of a custom-developed high speed single channel receiver.

This thesis was an attempt to develop a multichannel system, operating at high data rate. It further proves that it is possible to implement such a system. The low

cost, reliability, high performance and flexibility of a multichannel system ensures that this is the ultimate choice for a high speed satellite communication system with general application possibilities.

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Appendix A - User's Guide for Matlab Simulation Tool

The QPSK Simulation Tool was developed in Matlab²¹ to visually display the influence of inaccuracies on the system. The program is included on the accompanying CD. The graphical user's interface for the simulation tool is shown in Figure 115.

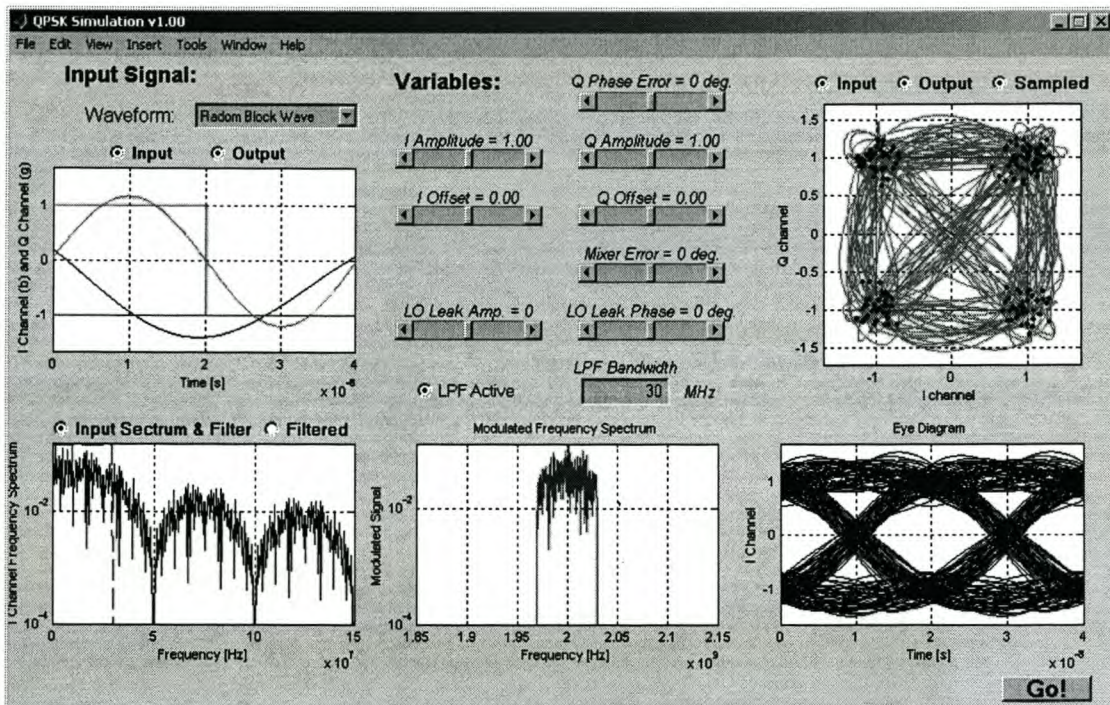


Figure 115 Graphical User's Interface of Simulation Tool

Each section will be discussed in more detail.

Input Signal

The software allows several possibilities for input data: single sideband sinusoidal signals, single sideband rectangular signal and random digital data. The input data type is selected with the **Waveform** combo box. When a waveform is selected a

²¹ Matlab 6.0.0.88 by MathWorks

series of 200 symbols is generated. Two symbol periods of the I and Q channel waveforms is displayed when the **Input** radio button is selected.

A single sideband (Q channels is delayed with 90°) sinusoidal signal is generated with a frequency of 25 MHz. The positive cycle represents a digital 1 and the negative cycle a digital 0. Thus the symbol rate is 50 Msps.

When **SSB Block Wave** is selected, the single sideband rectangular signal is generated with a symbol rate of 50 Msps.

A random bit stream of digital bits is generated when **Random Block Wave** is selected. Again the symbol rate is 50 Msps. A new random series is generated with every simulation.

The three input data types are shown in Figure 116.

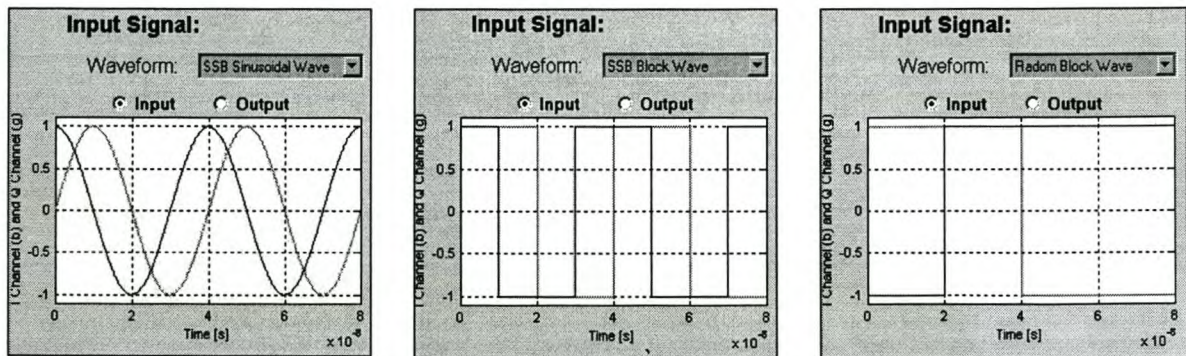


Figure 116 Three Different Input Data Types

Inaccuracies

The software allows for several inaccuracies to be selected and varied. This section of the software is shown in Figure 117.

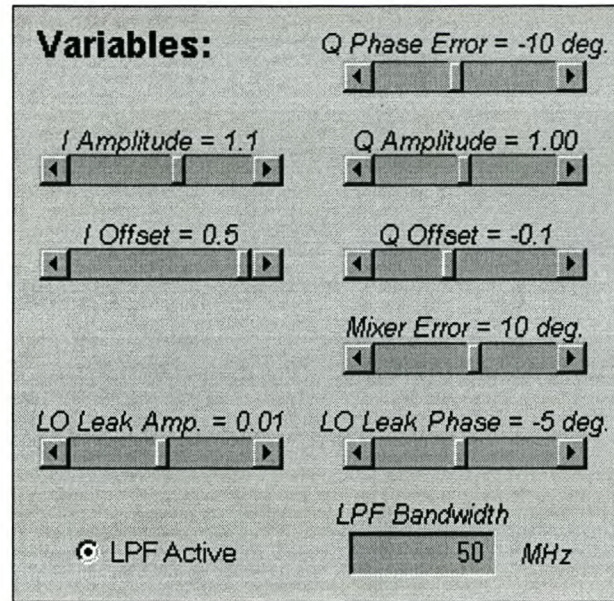


Figure 117 Inaccuracies Section

The inaccuracies can be divided into three categories were they are applied, as shown in Table 23.

Table 23 Inaccuracy Categories

Category	Inaccuracy Description
Input Data	I and Q Channel Amplitude I and Q Channel Offset Q Channel Phase Error
Baseband Shaping	Rectangular Filter Bandwidth
Modulator	Mixer Phase Error LO Leakthrough Amplitude and Phase

For the *Input Data* inaccuracies the inaccuracies is applied on the input signal and graphically displayed on the I and Q channel waveforms when the **Input** radio button is selected.

It is possible to enable baseband shaping with the **LPF Active** radio button. The baseband *I* and *Q* channels is filtered with a rectangular lowpass filter. The bandwidth is specified by **LPF Bandwidth** text box. The frequency spectrum of the unfiltered baseband *I* channel and filter response is showed when radio button **Input Spectrum & Filter** is selected. The spectrum of the filtered *I* channel is displayed when the radio button **Filtered** is selected. The spectrum of both these conditions is displayed in Figure 118.

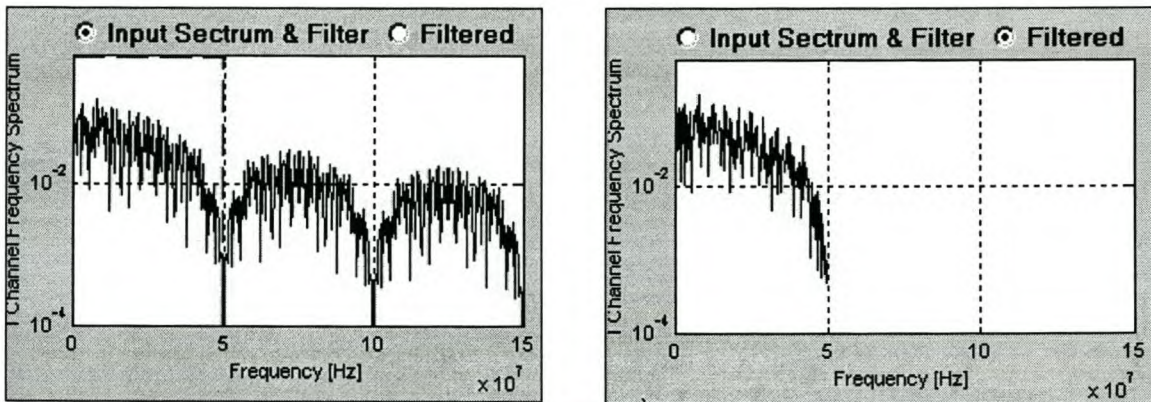


Figure 118 Baseband *I* Channel's Frequency Spectrum

Modulator

When the **Go!** button is pressed, the baseband shaping, modulation and demodulation process starts. The QPSK modulator modulates the baseband *I* and *Q* channels. The modulator inaccuracies are added in the modulation process. A carrier frequency of 2 GHz is used. An example of the frequency spectrum of a modulated signal is displayed in Figure 119.

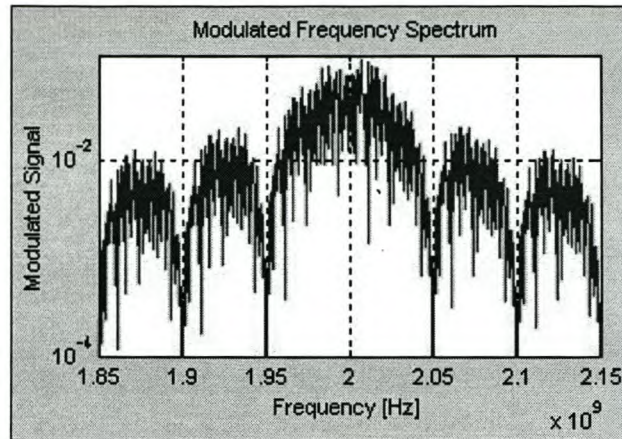


Figure 119 Modulated Frequency Spectrum Section

Demodulator and Output

After demodulation the I and Q channel are displayed in various ways: the channel's time response, the state space and the eye diagram is shown.

The I and Q channel's time response of two symbols after demodulation is displayed when the **Output** radio button is selected. This is shown in Figure 120.

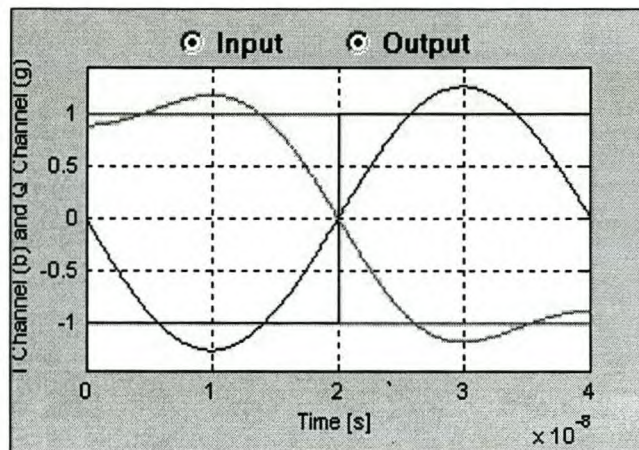
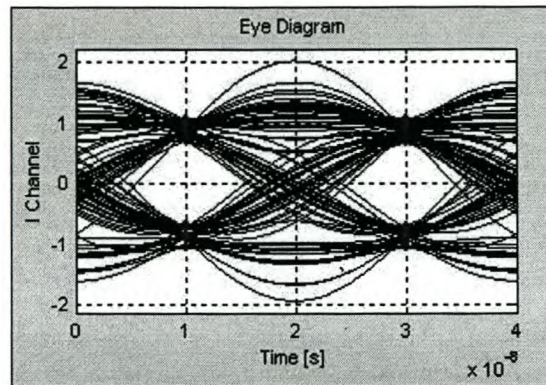
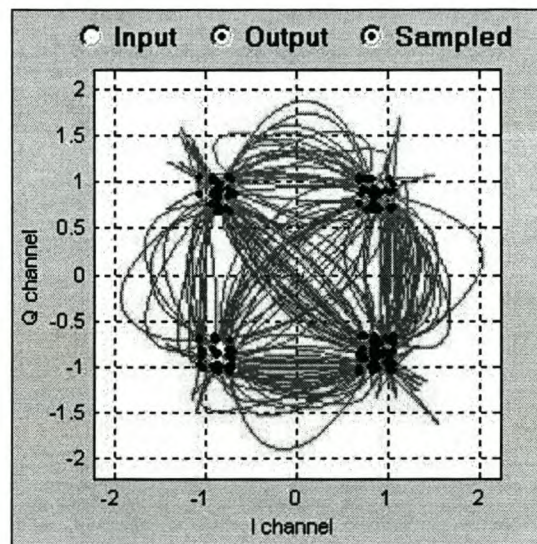


Figure 120 I and Q Channel after Demodulation

The eye diagram of the I channel after demodulation is plotted. The sample positions are indicated by a dot on the graph. An example of such a diagram is shown in Figure 121.

**Figure 121 Eye Diagram**

The state space after demodulation is displayed when the **Output** radio button is selected. The sample positions is indicated when the **Sampled** radio button is selected. An example of such a plot is displayed in Figure 122.

**Figure 122 State Space**

Code Structure

A flow diagram of the simulation's Matlab source code is shown in Figure 123. Each block represents a Matlab function. The complete source code is included on the accompanying CD.

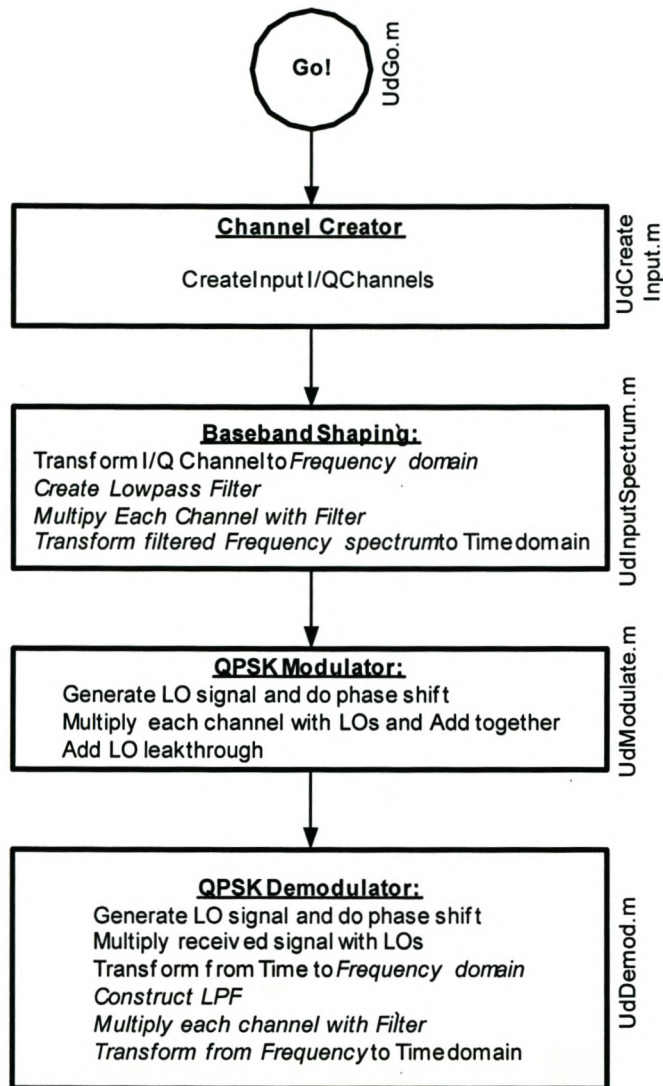


Figure 123 Flow Diagram of Code Structure

Appendix B - User's Guide for QPSK System Controller

The QPSK System Controller software was developed in Delphi²² to control the custom-developed QPSK transmitter and Sancy DVB receiver. The software was also responsible for displaying the status of the Sancy DVB receiver and graph these for various transmitter conditions.

The software is divided into three sections, or pages, each with a different function.

Transmitter Page

This section of the *QPSK System Controller* program is created to control the custom-developed multi-channel QPSK transmitter. A screenshot of this section is shown in Figure 124.

²² Borland Delphi Professional Version 6.0

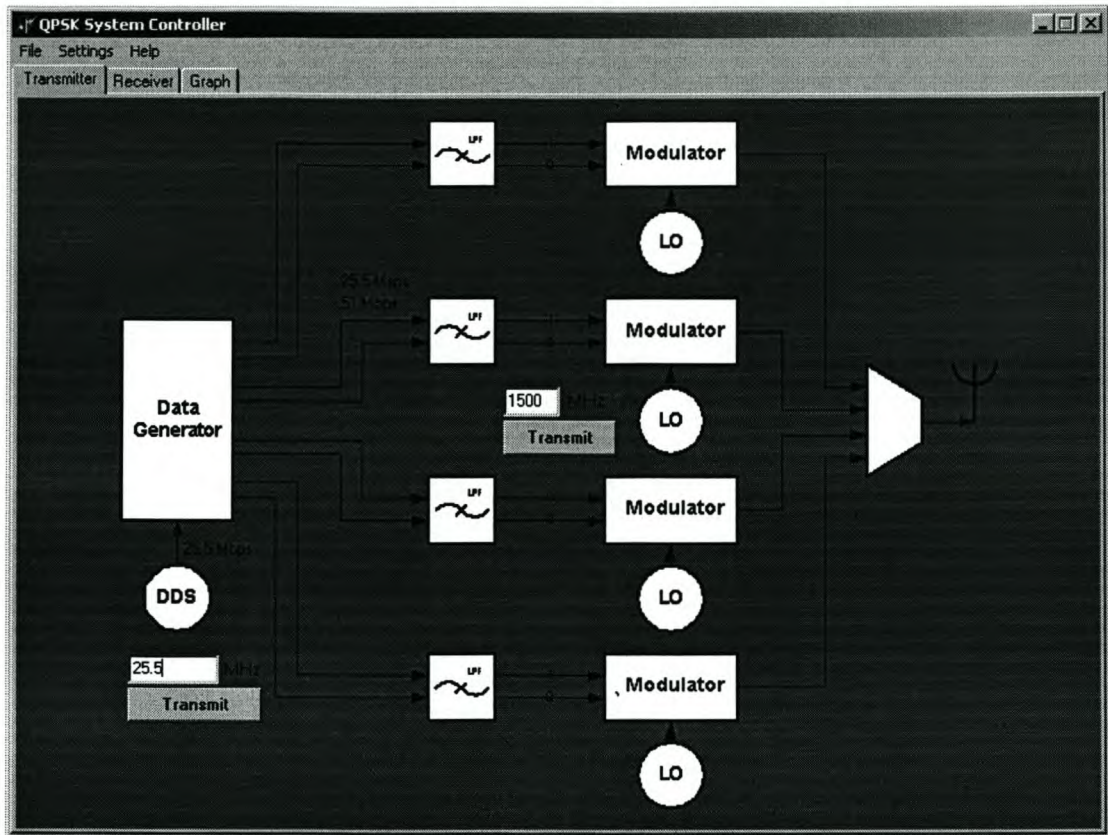


Figure 124 Transmitter Page

Two transmitter variables are controlled through this page: the DDS' clock frequency and the carrier frequency of synthesizer number two.

The frequency of the DDS can be varied between 0 Hz and 70 MHz in steps of 1 Hz. This signal is used as a clock for the FPGA's data generator and the data rate is therefore controlled. The data rate of the system is the same as the frequency of the DDS. When the data is differentially encoded with $\frac{1}{2}$ rate, the symbol rate is the same as the initial data rate and the transmitted data rate is double the symbol rate.

The frequency of the synthesizer number two can be varied between 1 GHz and 2 GHz in steps of 1 MHz. The other three channels are not yet equipped with synthesizers and are thus not implemented in the software. This can be expanded in a later stage.

Receiver Page

This section of the program is created to control the Sancy DVB receiver. A screenshot of this page is shown in Figure 125.

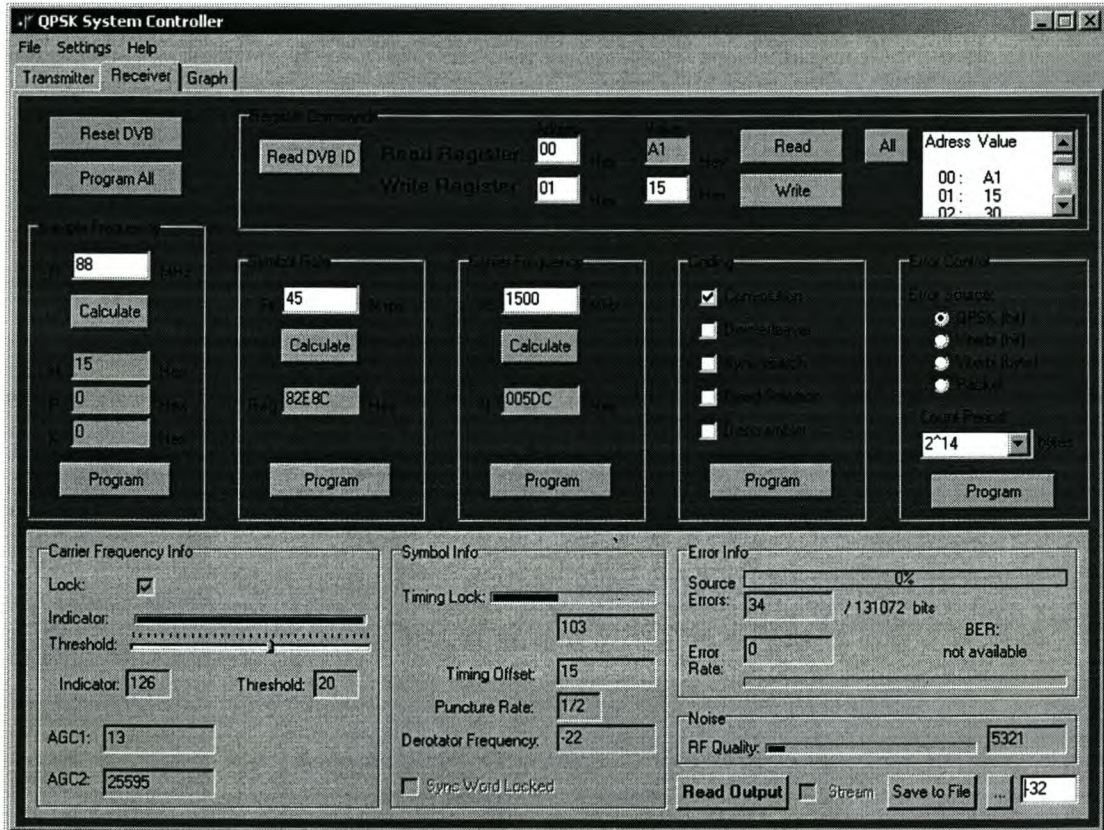


Figure 125 Receiver Page

The receiver page are divided into several sections

Register Commands

This section offers the ability to read the value of a specific register (or all at once) and to program a register with a value.

Each I²C unit has a specific ID by which it is identified. By definition the Sancy DVB's ID is located in register 00_{hex} with value A1_{hex}. When the **Read DVB ID** button is pressed, the value A1_{hex} should be displayed in the **Value** text box of the **Read Register** row.

When a different register is to be read, the hexadecimal address should be entered in the **Address** text box in the **Read Register** row. When the **Read** button is pressed, the corresponding register value is displayed in the **Value** text box.

When the values of all the registers are to be read at once the **All** button will display all register addresses and values in the memo box.

When a value is to be written to a register, the register's address and value is entered in the **Address** and **Value** text boxes in the **Write Register** row. The **Write** button will program the Sancy DVB receiver.

DVB Initialization Procedure

The sample frequency of the Sancy DVB receiver is programmed in the **Sample Frequency** section. The sample frequency can be varied up to 88 MHz, in steps of 1 MHz. The value is entered in the f_s text box. When the **Calculate** button is pressed the three registers regarding sample frequency is calculated. These are displayed in the **M**, **P** and **K** text boxes. The **Program** button programs these register with the calculated values.

The programming of the DVB receiver's sample frequency sometimes produces errors. Values not dividable by eight usually cause errors but exceptions exist. It was also noted that a sample frequency was acceptable for a certain symbol rate but not another. The source of this problem might be the software developed to program the Sancy DVB unit or the unit itself. This phenomenon still remains a mystery.

The symbol rate is programmed in the **Symbol Rate** section. The symbol rate can be varied between 1 Msps and 45 Msps in steps of 1 Msps. The rate is entered in the **Fs** text box. The **Calculate** button will calculate the 5 byte register value to program the symbol rate. This is done when the **Program** button is pressed.

The carrier frequency is programmed in the **Carrier Frequency** section. A carrier frequency between 950 MHz and 2150 MHz in steps of 1 MHz can be entered in the **fc** text box. The **Calculate** button will transform the frequency value into a register

value. The DVB receiver is programmed with this value when the **Program** button is pressed.

In the **Coding** section different demodulators can be enabled through check boxes. The Convolutional decoder can not be disabled. The **Program** button programs the state of each decoder.

In the **Error Control** section the method of error measurement is controlled. The **Error Source** is selected with radio buttons. The **QPSK (bit)** radio button indicates that bit errors are counted after QPSK demodulation. **Viterbi (bit)** and **Viterbi (byte)** indicates that bit and byte errors are counted after the Viterbi decoder. For the **Packet** radio button, packet errors are counted. The **Count Period** specifies the total number of bytes considered in an error count. The **Program** button programs the Sancy DVB receiver with these configurations.

The **Reset** button resets the Sancy DVB receiver and returns all registers to the reset state. The **Program All** button is an automatic process of pressing all the **Program** buttons in sequence of: sample frequency, symbol rate, carrier frequency, coding and finally error control.

Status

When the **Read Output** button is pressed all the status displays are updated with the latest information. The different displays are discussed:

The **Carrier Frequency Info** box displays the register information regarding the carrier frequency. The **Indicator** bar and text box displays the value of the CLDI register. This register indicates the carrier lock. A high value indicates a good lock. The **Threshold** slider and text box sets the CLDT register value. This value is compared with the CLDI register and if the CLDI register is bigger, the **Lock** flag indicates that carrier lock is obtained. The **AGC1** and **AGC2** text boxes displays these register values. These values give an indication of the carrier power.

The **Symbol Info** box displays information about the status of the symbol quality. The **Timing Lock** bar and text box indicates the value of the TLI register. This register's value depends upon signal to noise ratio and the signal lock state. The **Timing Offset** text box displays the value of the RTF register, indicating the amount of timing offset. Ideally this value should be zero. The **Puncture Rate** text box displays the detected puncture rate when lock is obtained. For the developed system this value should be $\frac{1}{2}$. The **Derotator Frequency** text box displayed the value of the CFR register. This value is used to calculate the derotation frequency. When a synchronization word is detected and the DVB receiver is set up to search for this word (enabled **Sync search** checkbox), the **Sync Word Locked** flag is displayed.

The **Error Info** box displays the status of the error count registers. The **Source Errors** bar and text box indicate the value of the ERRCNT register. This register counts the errors occurring at the position as was specified by **Error Source** radio button group. A text label displays the total number of units considered for the count. This value is determined by the **Count Period** drop down box. The **Error Rate** bar and text box display the value of register VERROR. This register indicates the amount of errors after the Viterbi decoder.

The **Noise** box display information about the amount of noise present in the system. The **RF Quality** bar and text box display the value of the NIR register.

Save to File

The file is selected by pressing the [...] button. A **Browse for File** window is opened to select a file. This window is shown in Figure 126. A new filename could be entered in the **File Name** text box. The extension should be included.

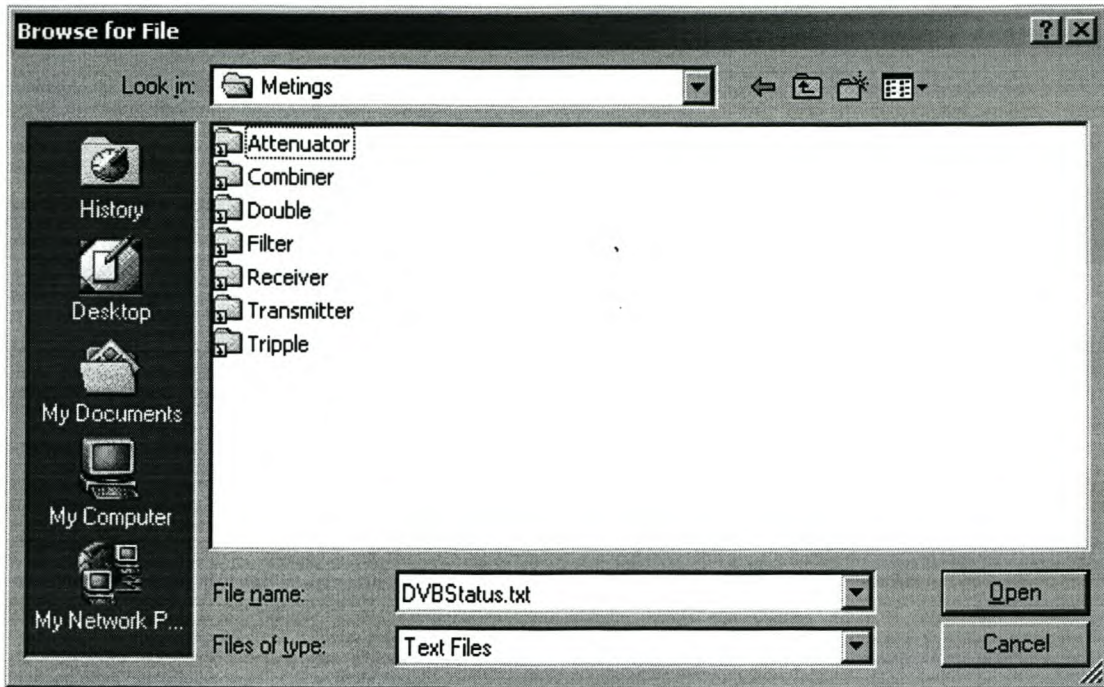


Figure 126 Browse for File Window

When the **Save to File** button is pressed all status registers are saved to the current text file. The sequence in which the registers are saved are as follow:

[User Input, Carrier Frequency, CLDI, AGC1, AGC2, Symbol Rate, Puncture Rate, TLIR, RTF, CFR, Sample Frequency, Error Source, ERRCNT, Total Error Cnt, VERROR, NIR]

The blank text box is used as user input field and is also saved in the selected file. If this button is pressed more than once, a new line with register values is inserted at the end of the current file.

Graph Page

This section of the program is created to vary a parameter on the transmitter board and record and plot the status of the Sancy DVB receiver. A screenshot of this page is shown in Figure 127.

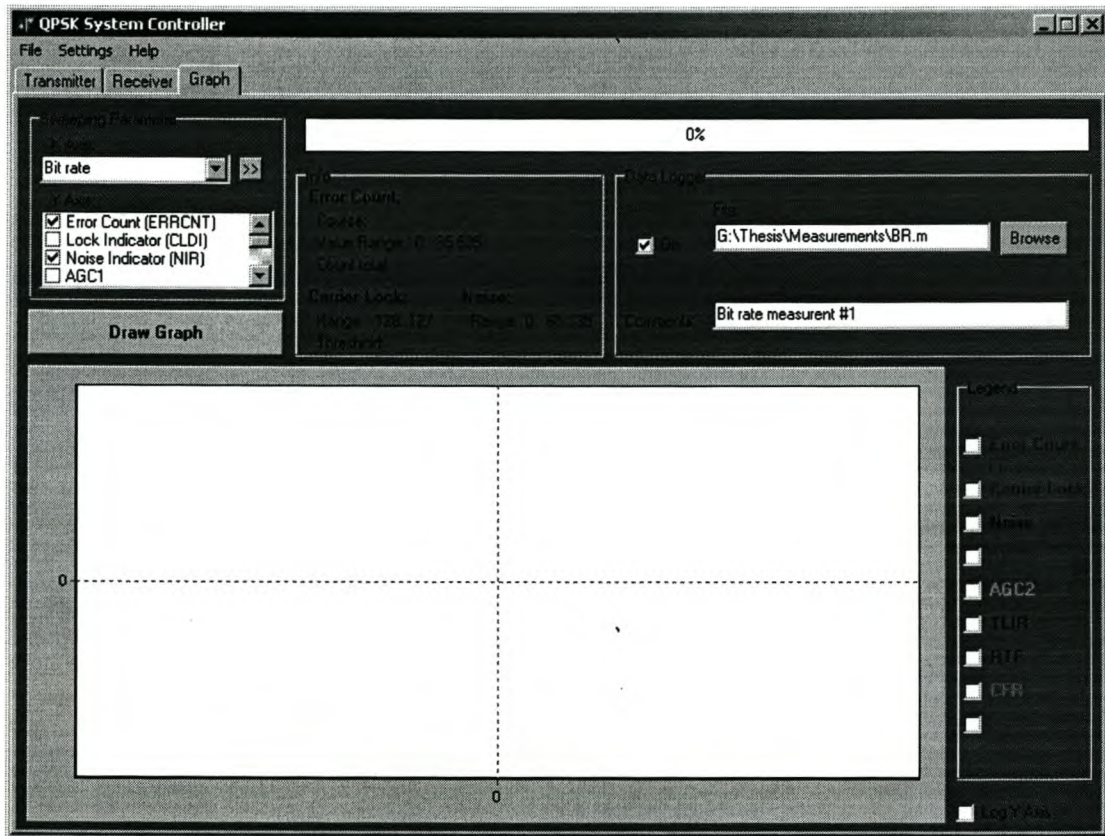


Figure 127 Graph Page

Sweeping Parameter

This section of the page determines the axes of the graph to be measured. The **X Axis** dropdown list specifies the transmitter parameter to be varied. The **bit rate** and **Carrier Frequency #2** are the two possibilities. Each of these could be defined by pressing the >> button to open the corresponding window. A screenshot of this is shown in Figure 128.

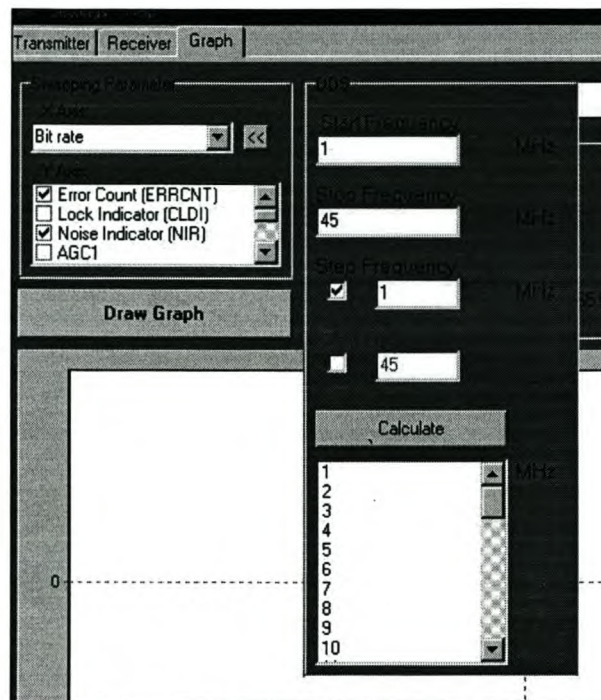


Figure 128 Variable Definition

Three possibilities of defining the data range exist: entering the start, stop and step frequency, entering the start and stop frequency and number of points and finally entering the start and step frequency and the number of points. When the **Calculate** button is pressed, the values are calculated and displayed in the list box. The variable definition box is closed when the << button is pressed.

The **Y Axis** check list specifies the register values to be recorded. All the selected registers will be plotted.

Graph

When the **Draw Graph** button is pressed the measurement begins. The variables not specified in this page will be adopted from the transmitter and the receiver pages. Thus if the data rate is varied for a measurement, the carrier frequency of the transmitter and receiver should be programmed before the measurement start. The status bar will display the progress of the measurement.

After the measurement is finished, the different plots can be disabled by selecting the check box in the legend. The graph can be converted to a logarithmic plot by

selecting the **Log Y Axis** checkbox. This is only possible when all registers that might have a negative or zero value is turned off.

Data logger

If the data is to be saved to a file, the **On** checkbox should be selected before the **Draw Graph** button is pressed. The filename is entered in the **File** text box. The **Browse** button opens a window similar to the one shown in Figure 126. This window allows for a file to be selected. The user's measurement comment can be entered in the **Comments** text box and is included in the file.

The selected register values are saved to the selected file, one line for each X axis data point. The sequence in which the registers are saved is as follow:

X Variable – Error Count, Carrier Lock, Noise, AGC1, AGC2, Timing Lock Indicator, Timing Offset, Derotator Frequency, Error Rate Indicator

For one single X axis data point ten measurements are captured. The register values are saved in abovementioned order repeated ten times.

Interface Protocol

When the menu option **Settings, Serial Settings** is selected, the **Serial Settings** window is opened. This window is shown in Figure 129.

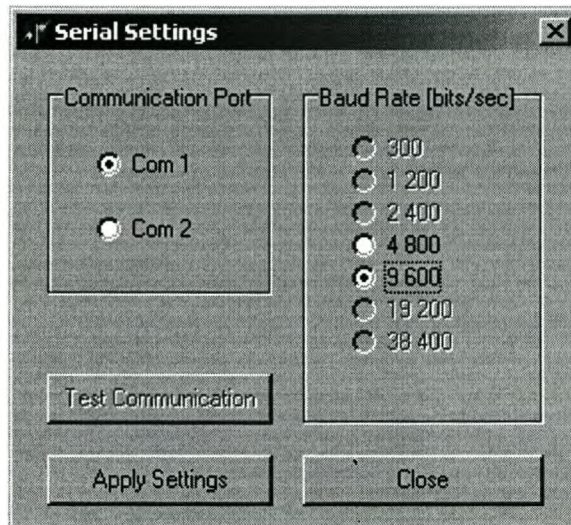


Figure 129 Serial Settings Window

Either *Com 1* or *Com 2* can be selected as communication path. The protocol is as follows: 9600baud, 8-bit UART, no parity, 1 stop bit. In order to ensure that no data is lost during communication, the microcontroller will retransmit each byte after reception. The computer will check if this byte is correct and continue if so.

The computer acts as a master device and the microcontroller as slave, thus all instructions are initiated by the computer. An eight bit code is allocated for each computer instruction, usually followed by a number of data bytes. A stop byte ($5F_{Hex}$) is used to terminate an instruction. When more than one byte is required to program a register, the most significant byte is transmitted first. The instructions are summarized in Table 24.

Table 24 Instruction Codes

Instruction Code	Instruction Description	Bytes transmitted after code	Number of bytes expected after write
01 _{Hex}	Program DDS with Frequency Code	<ul style="list-style-type: none"> • 4 bytes frequency code • stop byte 	
02 _{Hex}	Program Synthesizer 2 registers	<ul style="list-style-type: none"> • 2 byte R register • 1 byte P register • 2 bytes B register • 1 byte A register • stop byte 	
03 _{Hex}	Read DVB Registers	<ul style="list-style-type: none"> • 1 to 8 register address bytes • stop byte 	<ul style="list-style-type: none"> • Code 03_{Hex} • 1 to 8 register value bytes
04 _{Hex}	Write DVB Registers	<ul style="list-style-type: none"> • 1 to 4 register address, followed by register value bytes • stop byte 	<ul style="list-style-type: none"> • Code 0A_{Hex} • 1 confirmation byte
05 _{Hex}	Reset DVB	<ul style="list-style-type: none"> • stop byte 	
06 _{Hex}	Program DVB Synthesizer register	<ul style="list-style-type: none"> • 4 register bytes • stop byte 	<ul style="list-style-type: none"> • Code 0A_{Hex} • 1 confirmation byte

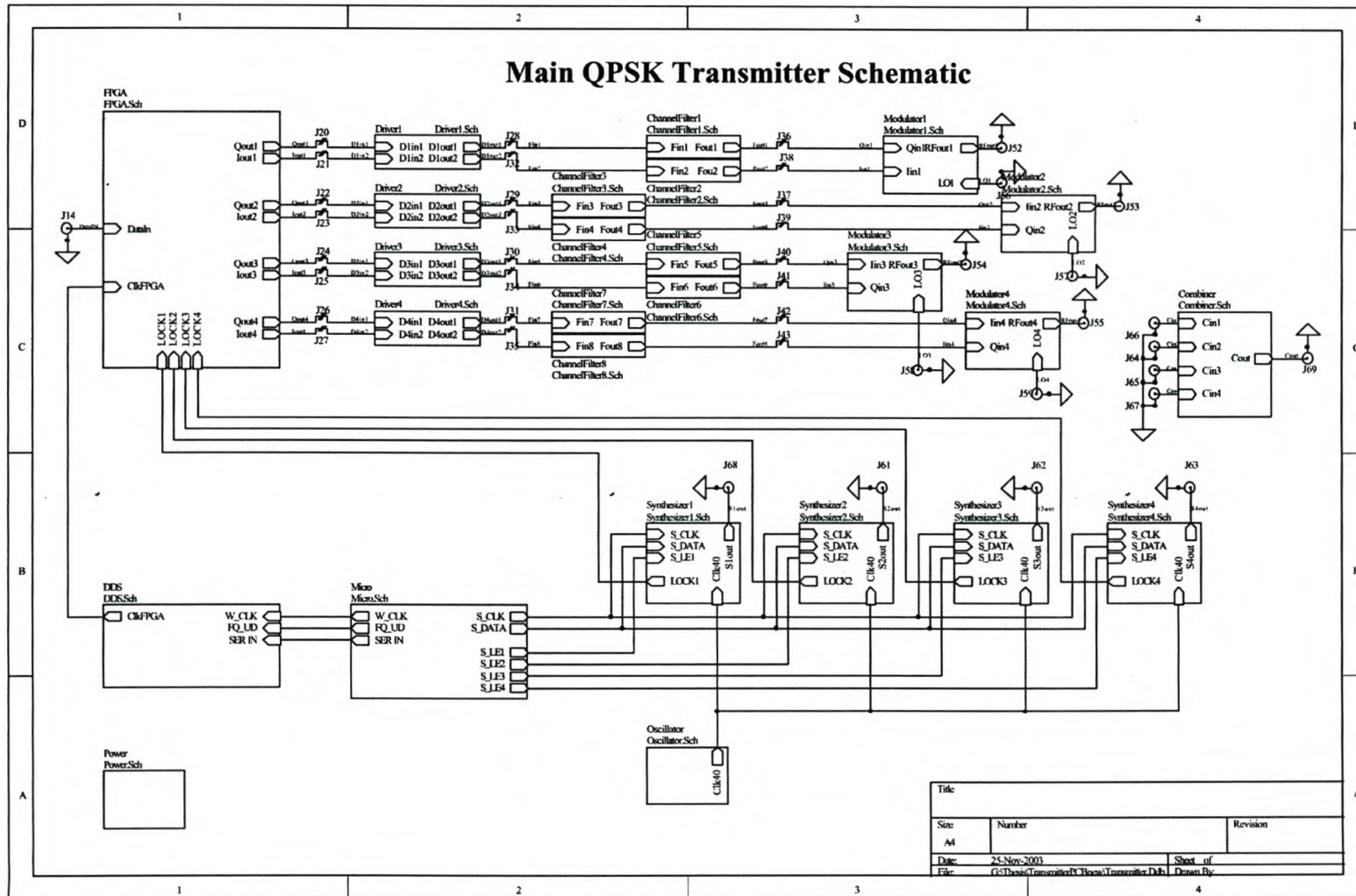
The *Read DVB Register* Instruction will be used as example to demonstrate the interface. DVB address 00_{Hex} and 04_{Hex} will be read:

Computer transmits to microcontroller:

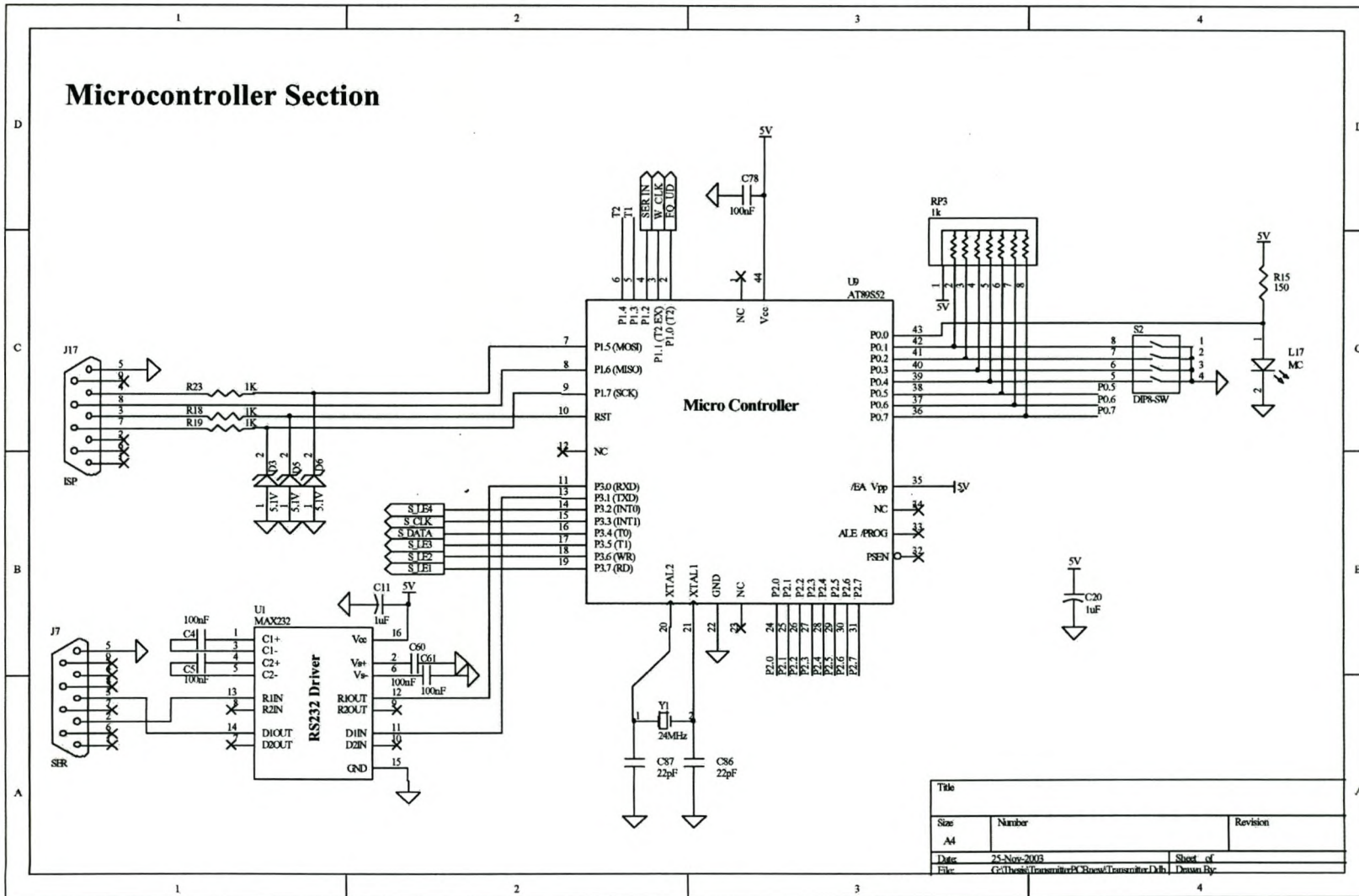
- 1) 03_{Hex} (instruction code)
- 2) 00_{Hex} (register address 1)
- 3) 04_{Hex} (register address 2)
- 4) 5F_{Hex} (stop byte)

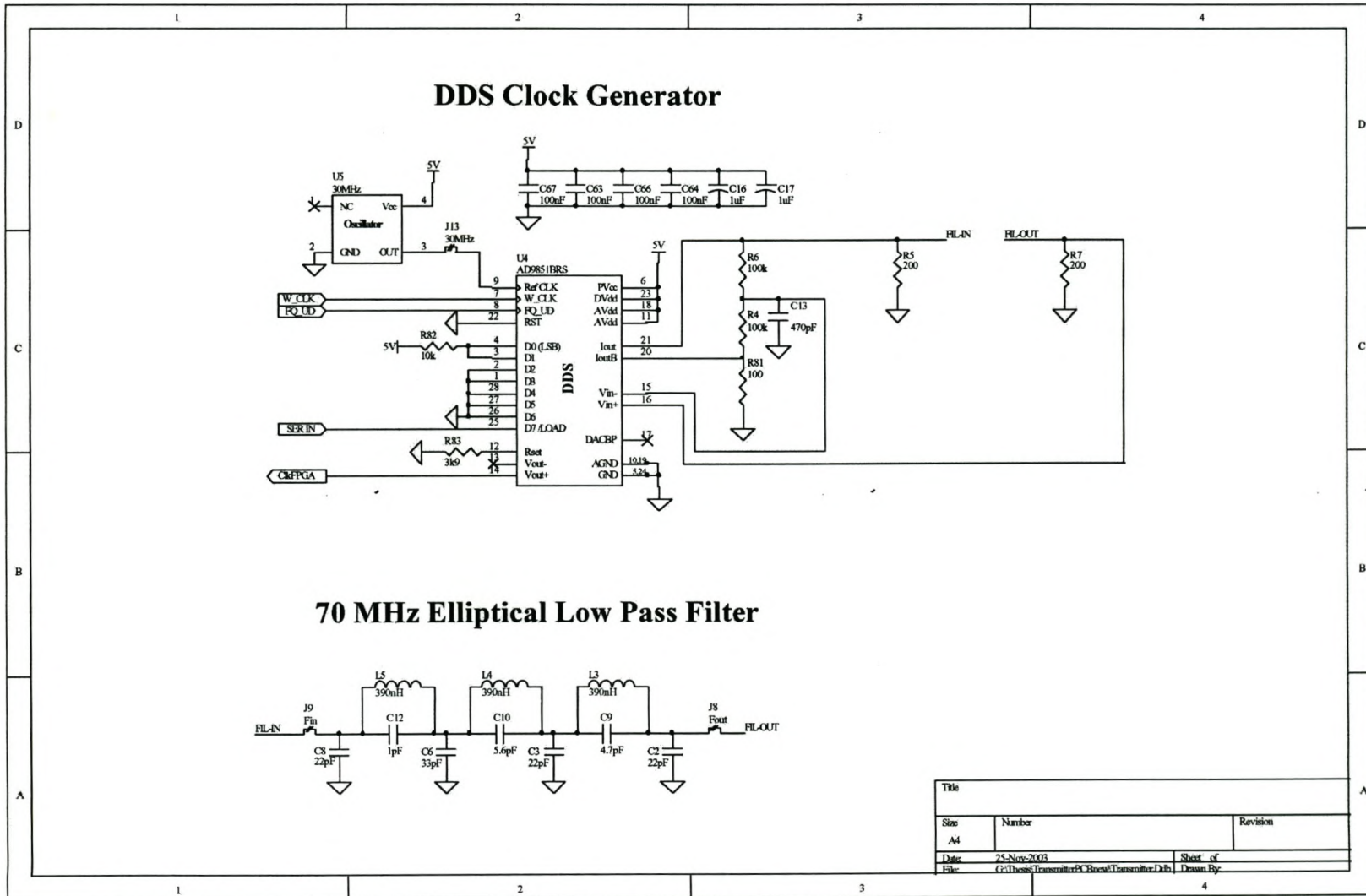
Computer receives for microcontroller:

- 5) 03_{Hex} (code)
- 6) 1A_{Hex} (register value 1)
- 7) 00_{Hex} (register value 2)

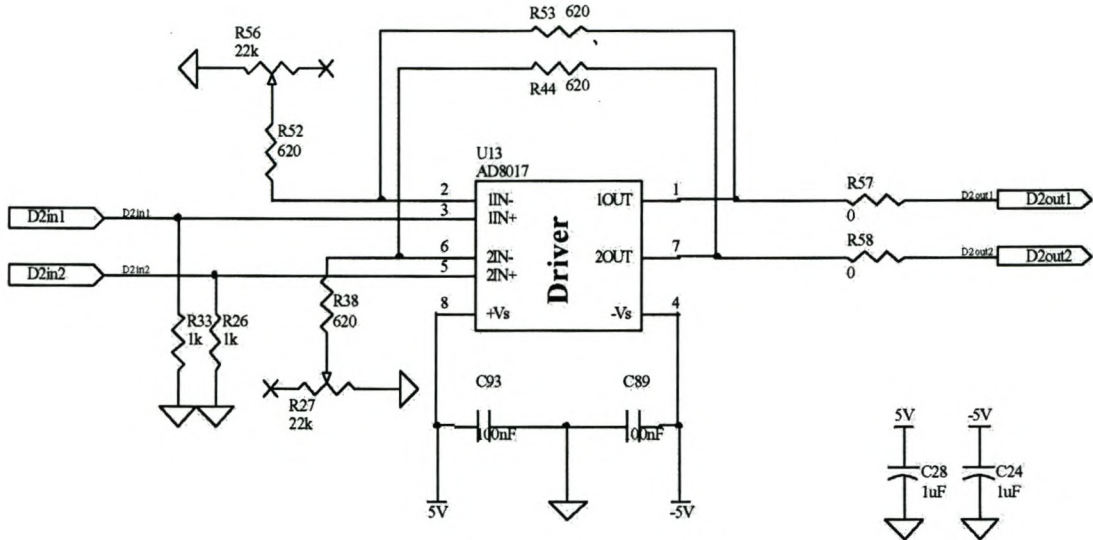


Appendix C - Schematic Diagrams of Transmitter

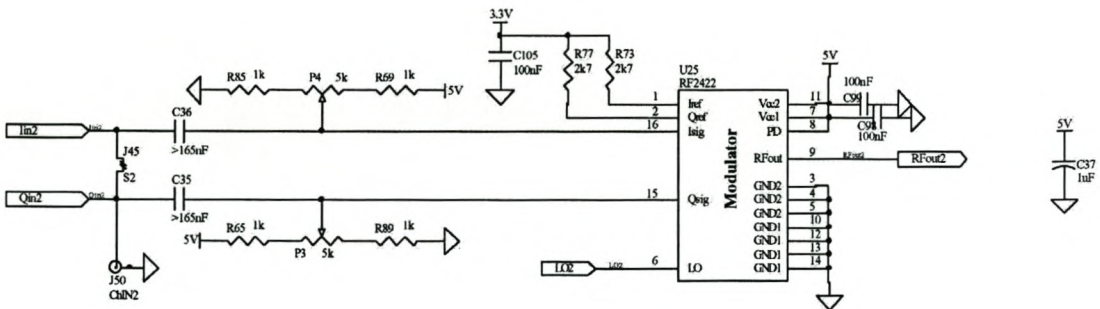




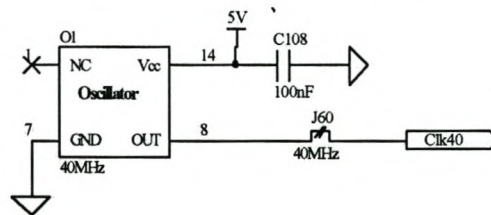
I&Q Line Driver 2



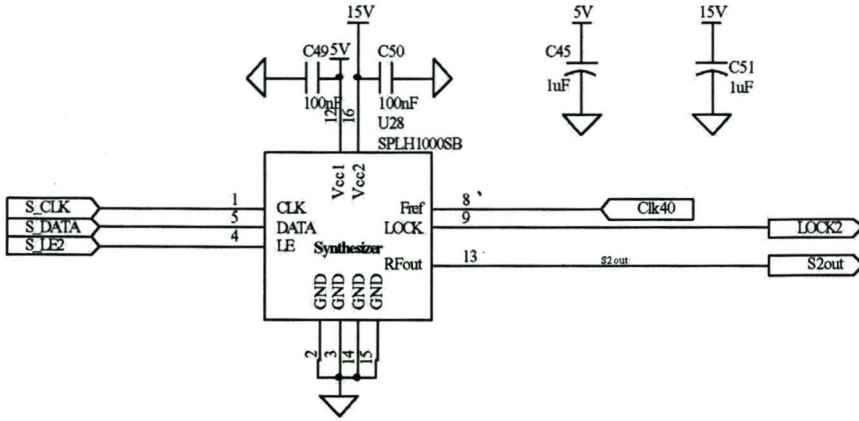
QPSK Modulator 2



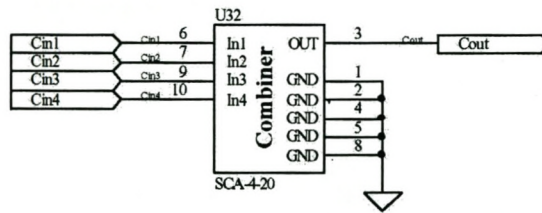
40 MHz Clock Reference

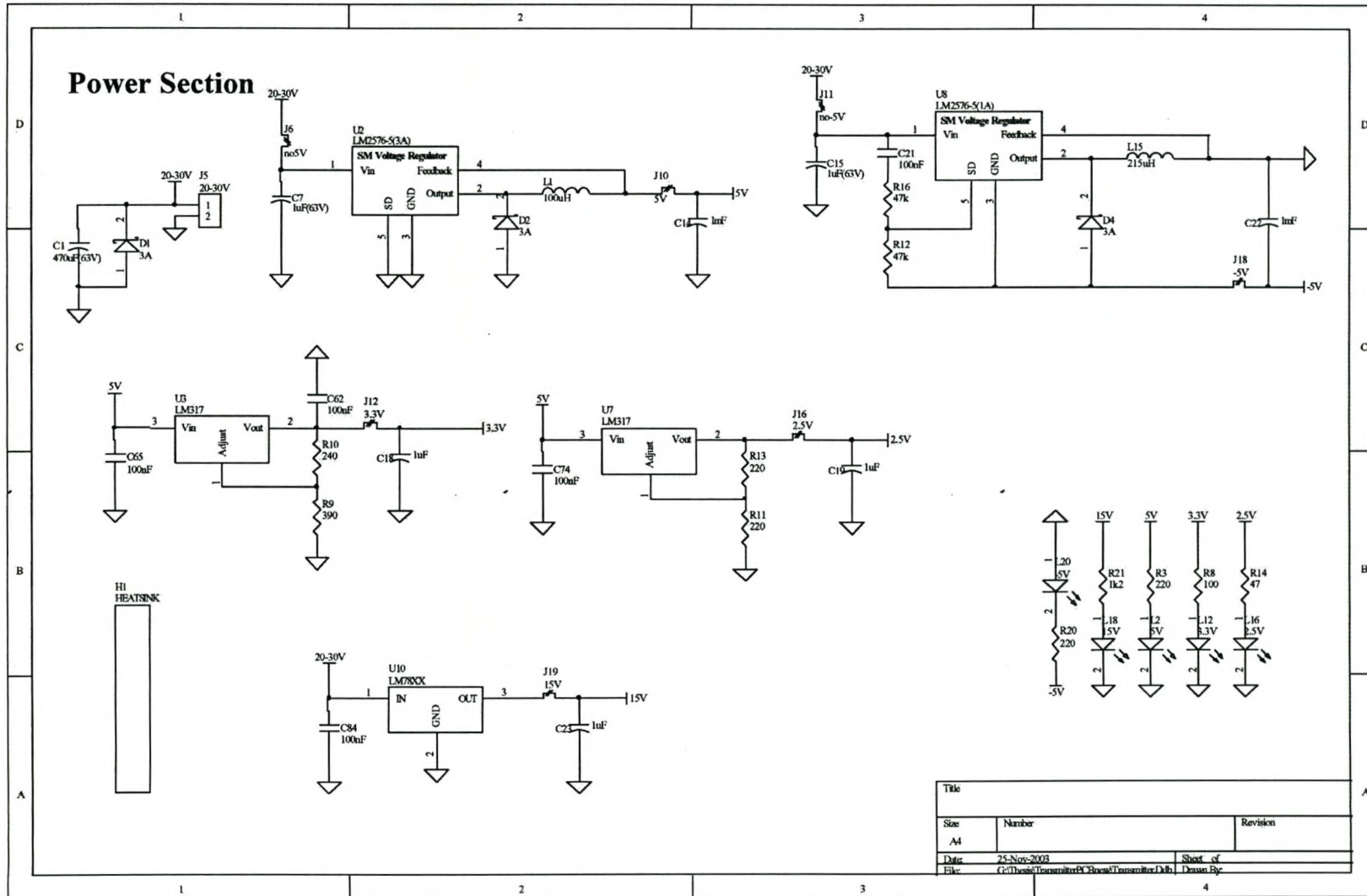


Synthesizer 2



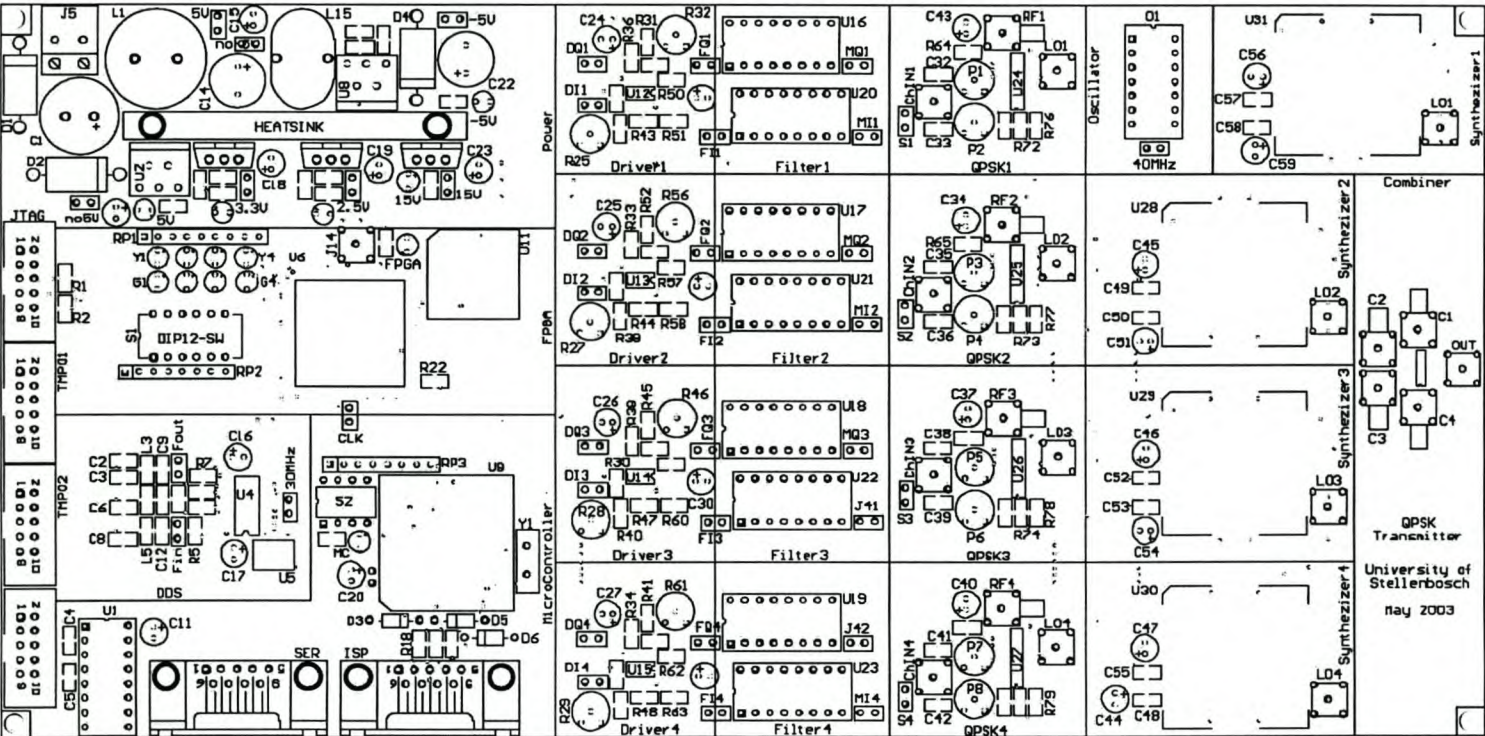
Combiner Section



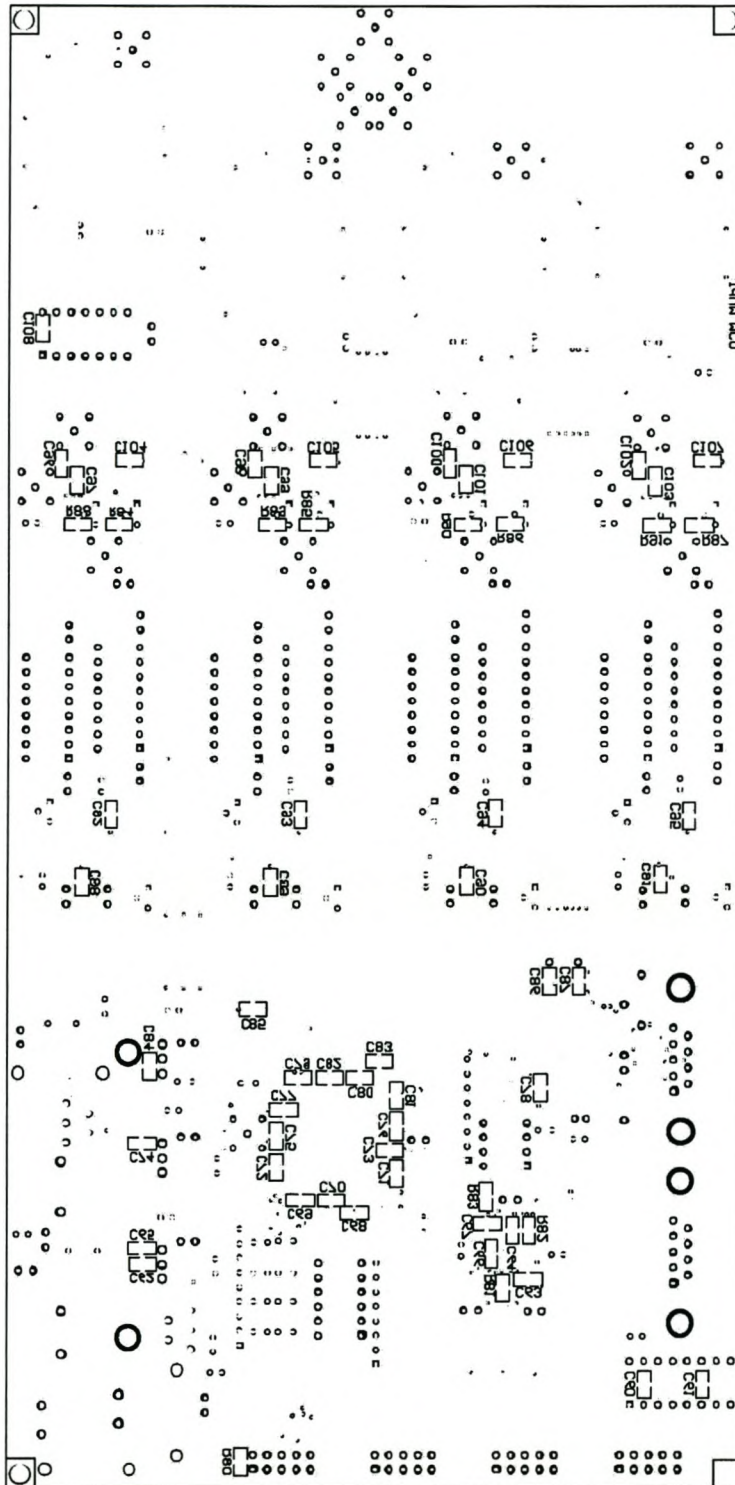


Appendix D - Transmitter PCB Drawings

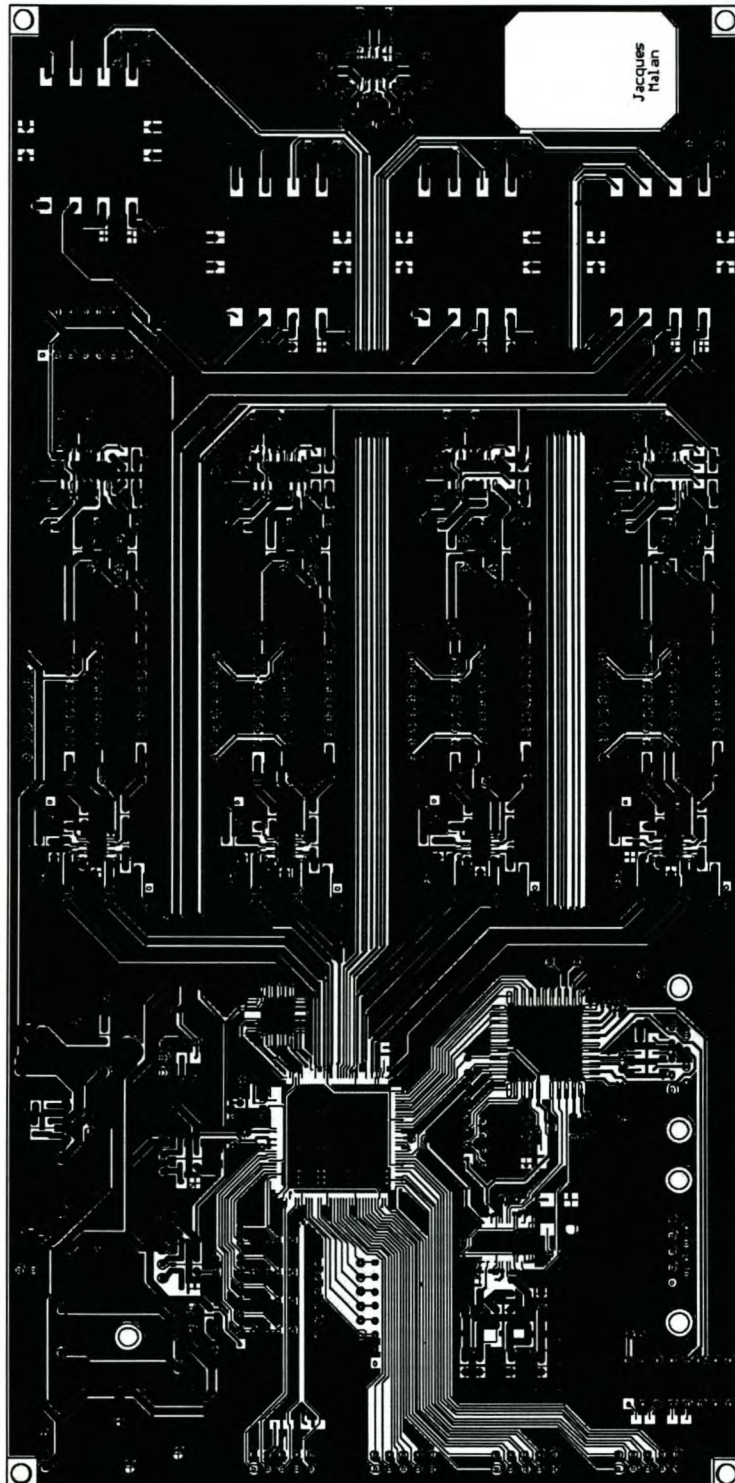
Top Overlay (1:1.333)



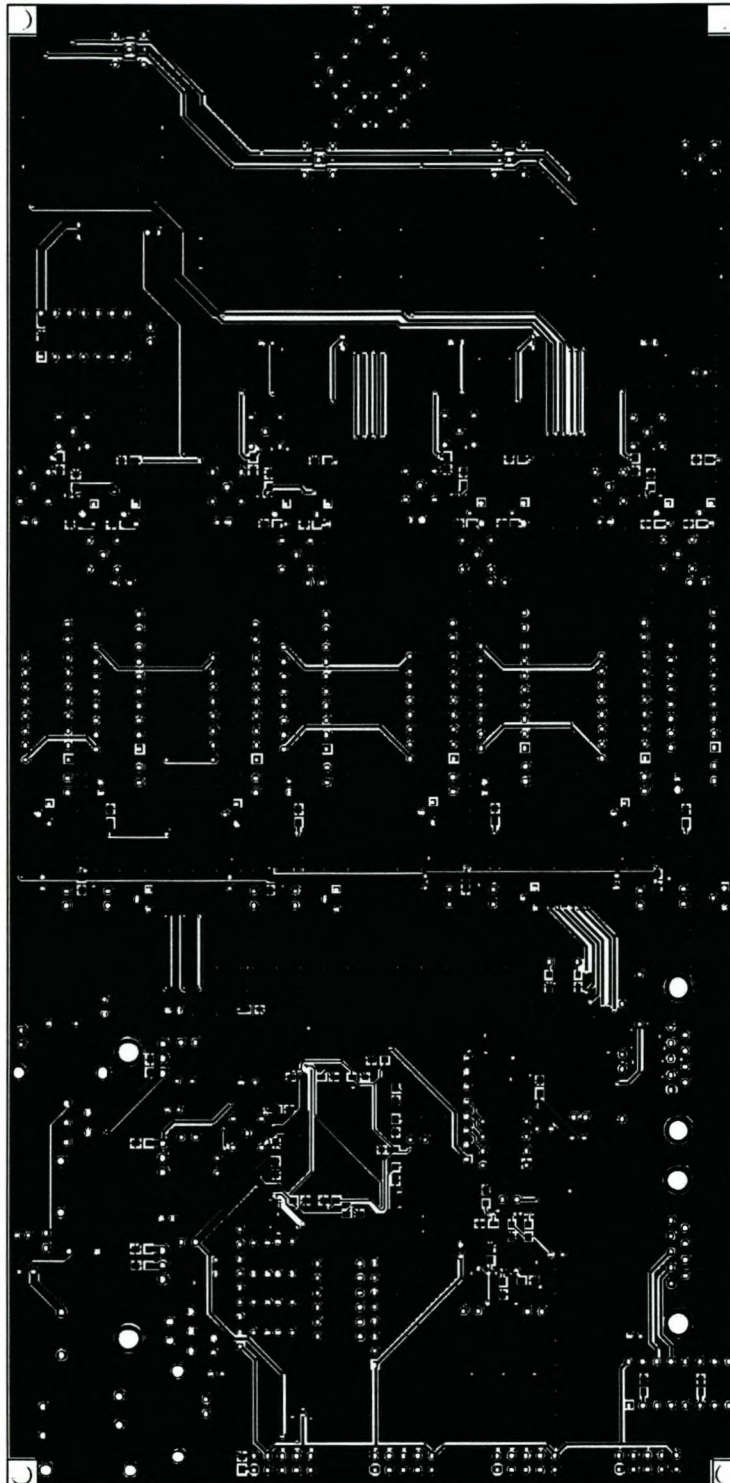
Bottom Overlay (1:1.333)



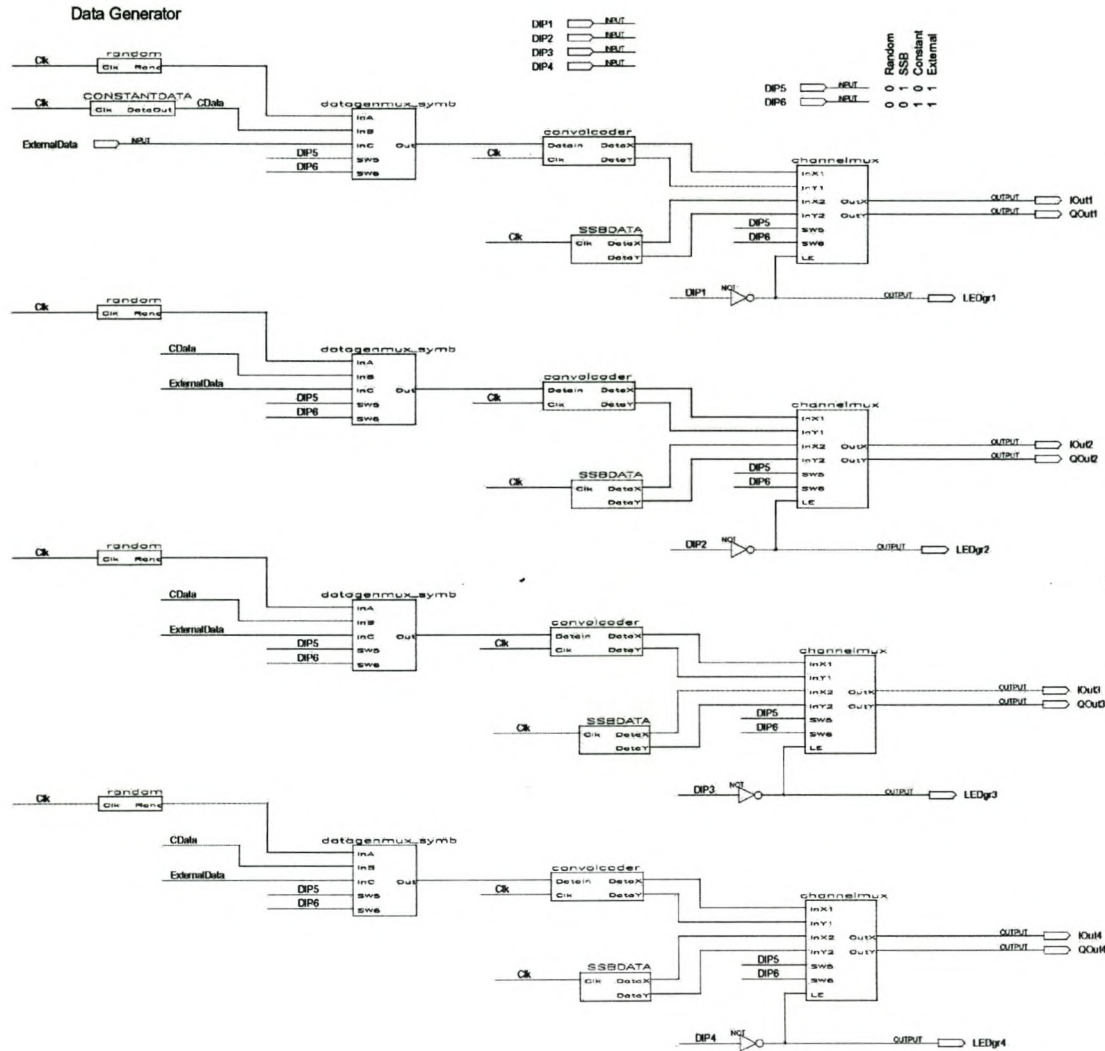
Top Layer (1:1.333)



Bottom Layer (1:1.333)



Appendix E - FPGA Schematics and Source Code



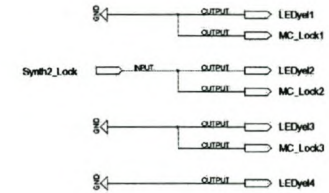
Blinking LED



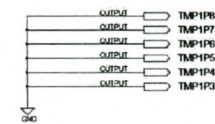
Receiver Interface



Synthesizer Lock Detect

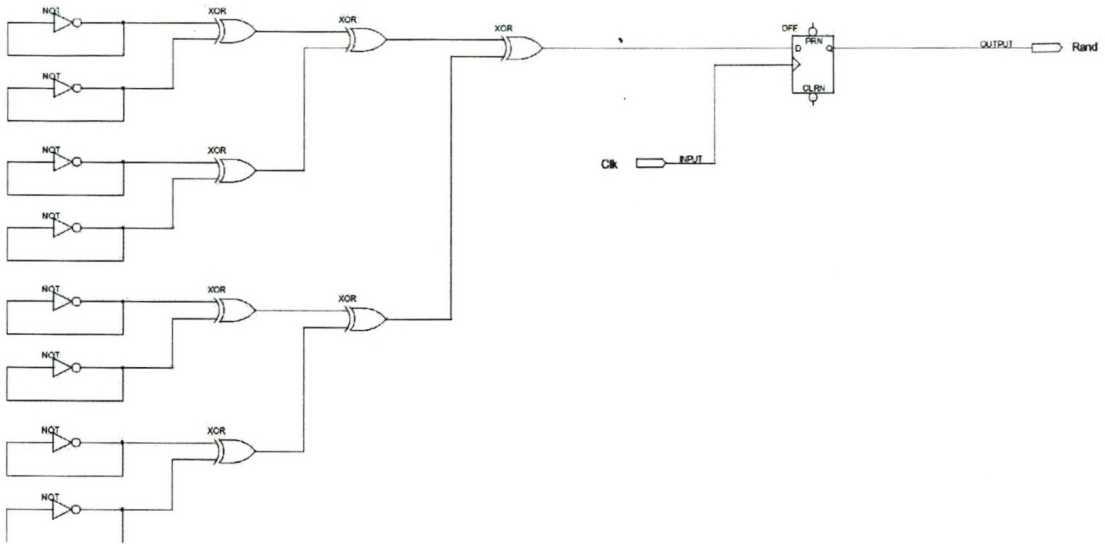


TMP1 Port

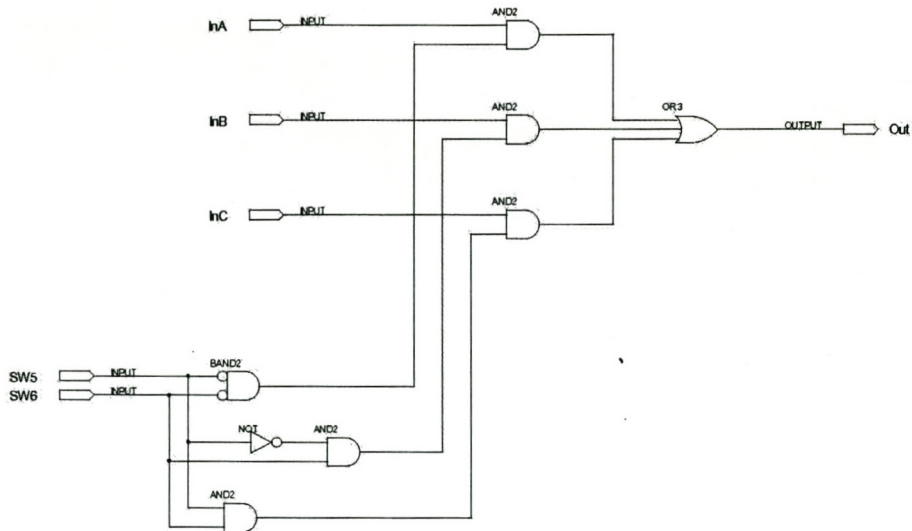


transmitter.gdf

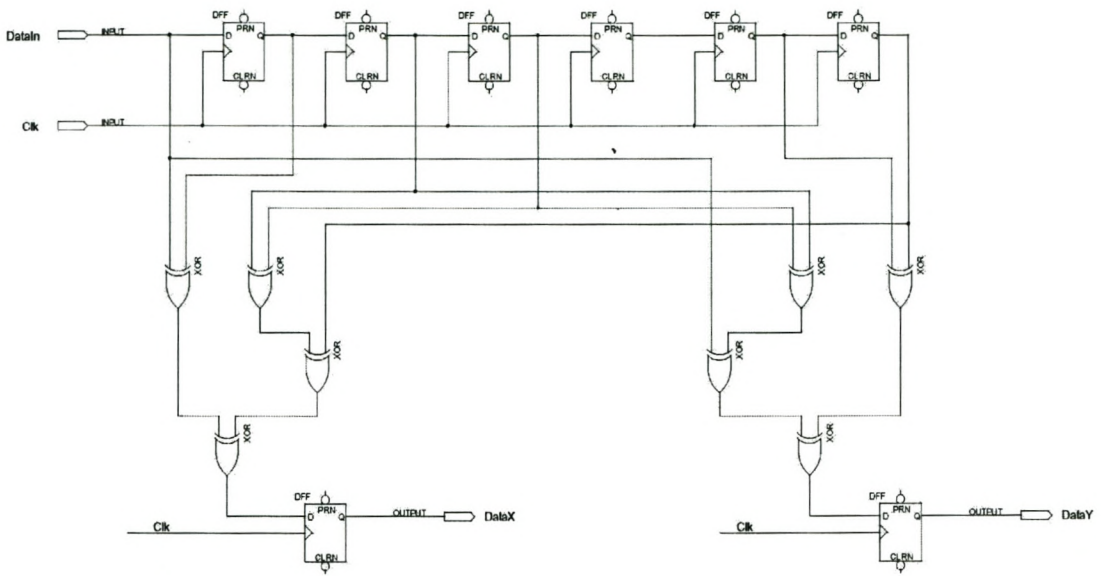
Random.gdf



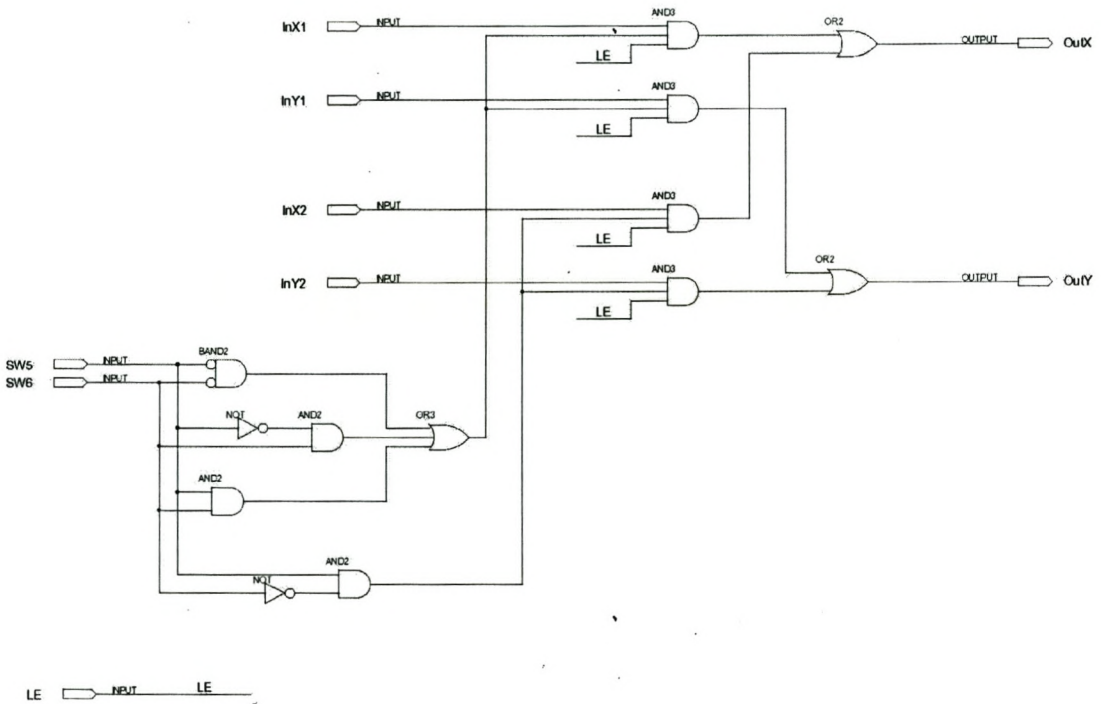
datagenmux_symb.gdf



convolcoder.gdf



channelmux.gdf



Constantdata.vhd

```
library IEEE;
use IEEE.std_logic_1164.all;

ENTITY ConstantData is

    port (      Clk      : in std_logic;
            DataOut    : out std_logic
            );

end ConstantData;

ARCHITECTURE a of ConstantData is

    signal      St      : integer range 0 to 15;

begin

    PROCESS (Clk)
    begin
        if (Clk'event and Clk = '1') then
            St <= St+1;
            case St is
                when 0 =>
                    DataOut <= '1';
                when 1 =>
                    DataOut <= '1';
                when 2 =>
                    DataOut <= '0';
                when 3 =>
                    DataOut <= '1';
                when 4 =>
                    DataOut <= '0';
                when 5 =>
                    DataOut <= '0';
                when 6 =>
                    DataOut <= '1';
                when 7 =>
                    DataOut <= '0';
                when 8 =>
                    DataOut <= '1';
                when 9 =>
                    DataOut <= '0';
                when 10 =>
                    DataOut <= '0';
                when 11 =>
                    DataOut <= '1';
                when 12 =>
                    DataOut <= '1';
                when 13 =>
                    DataOut <= '1';
                when 14 =>
                    DataOut <= '0';
                when 15 =>
                    DataOut <= '1';
            end case;
        end if;
    end PROCESS;

end a;
```

```

        end case;
    end if;

    end PROCESS;

end a;

```

ssbdata.vhd

```

library IEEE;
use IEEE.std_logic_1164.all;

ENTITY SSBData is

    port (
        Clk      : in std_logic;
        DataX    : out std_logic;
        DataY    : out std_logic
    );

end SSBData;

ARCHITECTURE a of SSBData is

    signal      St          : integer range 0 to 3;
    signal      ClkI        : std_logic;

begin

    ClkI <= not(Clk);

    PROCESS (Clk)
    begin
        if (Clk'event and Clk = '1') then
            St <= St+1;
            case St is
                when 0 =>
                    DataX <= '1';
                    DataY <= '0';
                when 1 =>
                    DataX <= '1';
                    DataY <= '1';
                when 2 =>
                    DataX <= '0';
                    DataY <= '1';
                when 3 =>
                    DataX <= '0';
                    DataY <= '0';
            end case;
        end if;

    end PROCESS;

end a;

```

Appendix F - HP8496A DC-4GHz Attenuator

The HP8496A attenuator has been measured. The attenuation is variable in steps of 10 dB between 0dB and -110 dB.

The attenuation is plotted in Figure 130. The frequency range is between 1 and 2 GHz and the attenuation dial is varied between 0 and -70 dB. Each line represents a different attenuation setting.

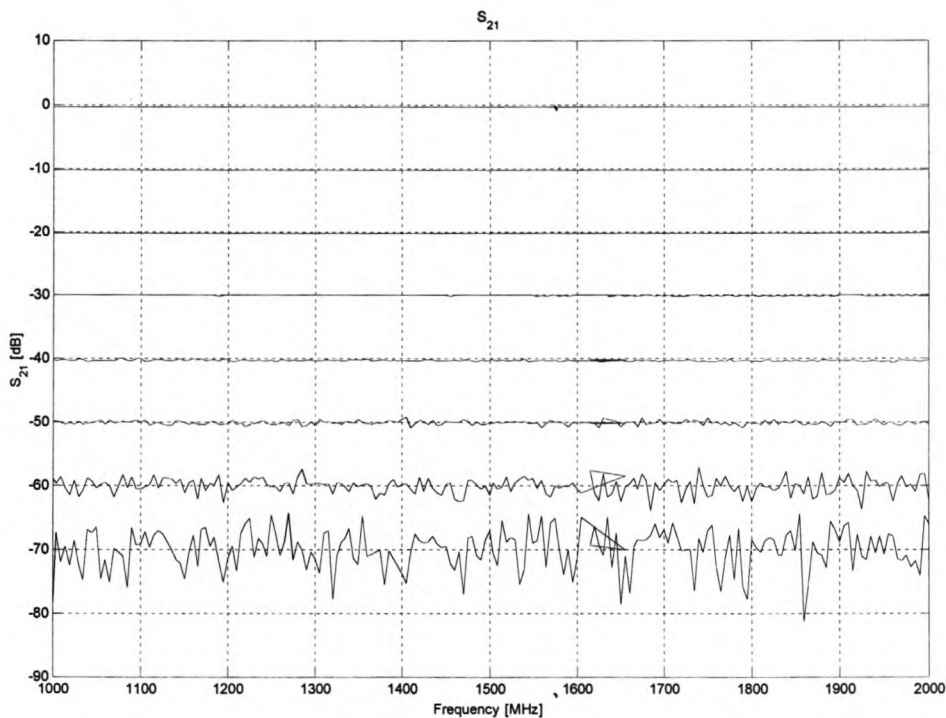


Figure 130 Attenuation of HP8496A attenuator

From Figure 130 it is clear that the attenuation is constant across the relevant frequency band.

The input and output reflection coefficients are plotted in Figure 131. Each line represents a different attenuation setting.

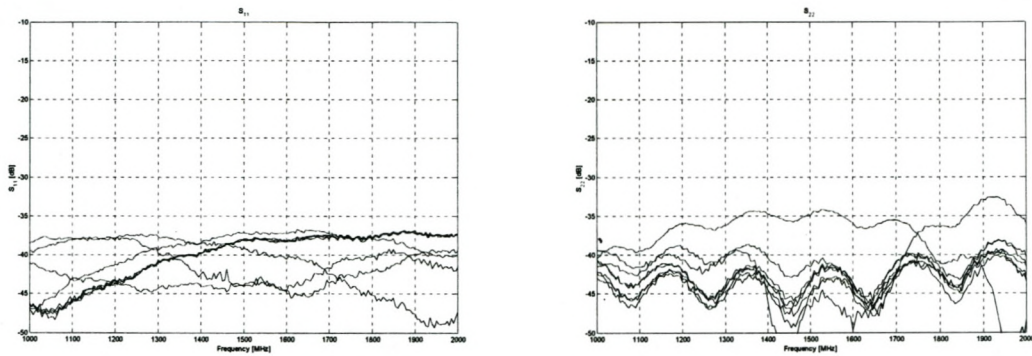


Figure 131 Reflection Coefficients

It is clear that the attenuator is well match across the relevant frequency range.