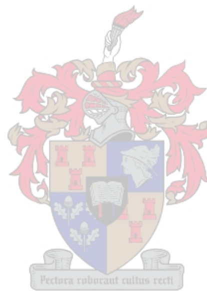
Design and Analysis of Broadband Microwave PIN Diode Switches

Quintin Engelbrecht



Thesis presented in partial fulfilment of the requirements for the degree of Master of Science in Engineering at the University of Stellenbosch.

Study leaders: Prof. Johann De Swardt and Dr. Cornell van Niekerk

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Declaration

I, the undersigned, hereby declare that the work contained in this thesis is my own original work and has not previously in its entirety or in part been submitted at any university for a degree.

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Synopsis

The aim of this thesis is the analysis and design of a broadband PIN diode switch.

Pin diode switches are gaining popularity in RF and microwave applications today. This is due to their excellent switching and power handling capabilities, reliability, low cost and small size. An analysis and design procedure for broadband PIN diode switch design, using the series, shunt and compound topologies respectively, is presented.

In order to do a proper switch design, accurate practical models for the components are required. Parameter extraction therefore formed an important consideration for this study. A parameter extraction procedure is presented, which enables the designer to very accurately extract the required models for the components in the environment they operate in. The designer can then do a proper design to ensure that the switch response when measured, closely corresponds to that simulated.

A compound configuration switch was designed, built and measured to confirm the validity of the design procedure. The results illustrate that if the extracted models of the components are integrated into the design, the measured and simulated response compare remarkably well.

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Opsomming

Die doel van die tesis is die analise en ontwerp van 'n wyeband PIN diode skakelaar.

PIN diode skakelaars is besig om meer populariteit te verwerf in hedendaagse RF en mikrogolf toepassings. Dit is as gevolg van die diode se goeie skakel- en drywing hantering vermoëns, betroubaarheid, lae koste en klein fisiese dimensies. 'n Analise en ontwerpsprosedure vir wye band PIN diode skakelaars in die serie, parallel en saamgestelde topologieë word getoon.

Om 'n deeglike skakelaar ontwerp te doen, word akkurate en praktiese modele van die komponente benodig. Parameter ekstraksie was daarom 'n groot oorweging vir hierdie studie. 'n Metode om parameters te onttrek word getoon wat die ontwerper in staat stel om akkurate modelle van komponente te onttrek, in die omgewing waarin hulle gebruik word. Die ontwerper kan dan 'n deeglike ontwerp doen wat as dit gemeet word, die gemete en gesimuleerde resultate goed sal ooreenstem.

'n Saamgestelde topologie skakelaar is ontwerp, gebou en gemeet om die ontwerpsprosedure te verifieer. Die resultate toon dat as die modelle wat onttrek is, gebruik word in die ontwerp, dan stem die gemete en gesimuleerde resultate baie goed ooreen.

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To my wife, Lize

Thank you for your loyal support and for always being by my side. You are a wonderful person and best friend ever.

I love you very much,

Quintin

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Table of Contents

Declaration i

Synopsis ii

Opsomming iii

Acknowledgements iv

LIST OF FIGURES xi

LIST OF TABLES xv

Glossary xvi

1 Introduction 1

2 PIN diode physics 2

2.1 PIN diode fundamentals 2

2.1.1 Forward biased PIN diode 3

2.1.1.1 Simplified linear high frequency model of forward biased PIN diode 6

2.1.2 Reverse biased PIN diode 7

2.1.2.1 Simplified linear high frequency model of reverse biased PIN diode 8

2.1.3 Equivalent low and high frequency model of the PIN diode 8

2.2 Packaging parasitic elements 10

2.3 PIN diode switching characteristics 11

3 Switch topologies 13

3.1 Switch terminology 13

3.1.1 "ON" and "OFF" states of switch 13

3.1.2 Absorptive and reflective switch 13

3.1.3 Insertion loss 14

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3.1.4 Isolation 14
3.1.5 Video leakage 14
3.1.6 Switching speed 15
3.1.6.1 Rise Time 15
3.1.6.2 Fall Time 15
3.1.6.3 ON Time 15
3.1.6.4 OFF Time 15
3.1.7 SPST switch 16
3.1.8 SPDT switch 16
3.1.9 SPMT switch 16

3.2 Switch configuration 16
3.2.1 Series configuration switch 17
3.2.1.1 Insertion loss 18
3.2.1.2 Isolation 20
3.2.1.3 Power Dissipation 21
3.2.1.4 Peak RF current 22
3.2.1.5 Peak RF voltage 22
3.2.1.6 Manufacturing 23
3.2.1.7 General design information 23
3.2.1.7.1 SPST switch 24
3.2.1.7.2 SPDT switch 28
3.2.2 Shunt configuration switch 32
3.2.2.1 Insertion Loss 33
3.2.2.2 Isolation 35
3.2.2.3 Power dissipation 36
3.2.2.4 Peak RF Current 37
3.2.2.5 Peak RF voltage 38
3.2.2.6 Manufacturing 38
3.2.2.7 General design information 38
3.2.2.7.1 SPST switch 39
3.2.2.7.2 SPDT switch 42

4 Device characterisation 46

4.1 Motive for device characterisation 46

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4.2 Parameter extraction methods **47**
4.2.1 Modelling 47
4.2.2 De-embedding 48
4.2.3 In-fixture calibration 48

4.3 TRL Calibration **49**
4.3.1 TRL test fixture design 50
4.3.1.1 Calibration standards 52
4.3.1.1.1 Thru standard 53
4.3.1.1.2 Reflect standard 54
4.3.1.1.3 Line standard 55

4.4 Measurements **60**
4.4.1 Soft substrate 60
4.4.2 Hard substrate 62

4.5 General problems and recommendations with TRL kits **64**
4.5.1 Soft substrate 64
4.5.2 Hard substrate 66
4.5.3 Conclusion 67

4.6 Parameter extraction **67**
4.6.1 Soft substrate 68
4.6.2 Hard substrate 76
4.6.2.1 Series configuration 77
4.6.2.2 Shunt configuration with diode placed next to the track 80
4.6.2.3 Shunt configuration with diode between the transmission lines 83

4.7 Results **85**

5 Practical switch **87**

5.1 Compound switch configuration **87**

5.2 Insertion loss **88**

5.3 Isolation **88**

5.4 General design information **89**

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5.4.1 Compound switch 89
5.4.1.1 Influence of junction T1: 90
5.4.1.2 Influence of Section 1 90
5.4.1.3 Influence of T2 91
5.4.1.4 Influence of Line 1 and T3 91
5.4.1.5 Simulation results 91
5.4.2 Compound switch with additional series diode 93
5.4.3 Compound switch with additional shunt diode 95

5.5 Hard and soft substrate technology overview 96
5.5.1 Difference in technology 97
5.5.1.1 Advantage of hard substrates 97
5.5.1.2 Disadvantage of hard substrates 97
5.5.1.3 Disadvantage of soft substrates 97
5.5.1.4 Advantage of soft substrates 98
5.5.2 Design differences 98
5.5.2.1 Series configuration diode 98
5.5.2.2 Shunt configuration diode 99

5.6 Practical switch design procedure 99
5.6.1 Soft substrate switch design 100
5.6.1.1 Design approach 101
5.6.1.1.1 Step 1: Substrate selection 103
5.6.1.1.2 Step 2, 4, 5: PIN diode selection 103
5.6.1.1.3 Step 3: Optimisation 106
5.6.1.1.4 Step 4: Insertion loss check 110
5.6.1.1.5 Step 5: Isolation check 110
5.6.1.1.6 Step 6: DC-decoupling capacitors and biasing circuit design 111
5.6.1.1.7 Step 7, 9: Final optimisation and layout 113
5.6.1.1.8 Manufacturing of the switch 116

6 Results 119

7 Conclusion 122

Derivation of the Insertion loss equation for a SPST series configuration switch 1

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Derivation of the Isolation for a SPST series configuration switch **3**

Derivation of the Insertion loss equation for the SPST shunt configuration switch **4**

Derivation of the Isolation equation for the SPST shunt configuration switch **6**

HPND-4005 Datasheet **7**

References **xi**

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LIST OF FIGURES

FIGURE 1: PIN DIODE CHIP GEOMETRY [1] 2

FIGURE 2: PIN DIODE CHARGE RESPONSE AS A FUNCTION OF FREQUENCY [3] 4

FIGURE 3: R_S VERSUS I_D TRACE FOR HPND-4005 PIN DIODE [12] 6

FIGURE 4: SIMPLE LINEAR MODEL OF A FORWARD BIASED PIN DIODE 7

FIGURE 5: SIMPLE LINEAR MODEL OF A REVERSE BIASED PIN DIODE 8

FIGURE 6: LOW FREQUENCY EQUIVALENT CIRCUIT OF A PIN DIODE 9

FIGURE 7: HIGH FREQUENCY EQUIVALENT CIRCUIT OF A PIN DIODE 9

FIGURE 8: TYPES OF PACKAGING [3] 10

FIGURE 9: PIN DIODE FORWARD TO REVERSE BIASED SWITCHING SPEED [1] 11

FIGURE 10: SWITCHING SPEED DEFINITIONS [7] 15

FIGURE 11: SERIES CONFIGURATION SPST PIN DIODE SWITCH 17

FIGURE 12: SPDT SERIES CONFIGURATION PIN DIODE SWITCH 18

FIGURE 13: INSERTION LOSS VERSUS SERIES RESISTANCE (R_S) FOR A SERIES CONFIGURATION SPST PIN DIODE SWITCH IN A 50 Ω SYSTEM 19

FIGURE 14: RF EQUIVALENT CIRCUIT OF A SERIES CONFIGURATION SPST PIN DIODE SWITCH WITH A PRACTICAL DIODEL MODEL 19

FIGURE 15: ISOLATION FOR A SERIES SPST PIN DIODE SWITCH IN A 50 Ω SYSTEM 20

FIGURE 16: SCHEMATIC USED FOR SIMULATING A SERIES CONFIGURATION SPST SWITCH 23

FIGURE 17: SPST SERIES CONFIGURATION SWITCH WITH TWO SERIES DIODES 25

FIGURE 18: INSERTION LOSS FOR SPST SERIES CONFIGURATION SWITCH WITH ONE, TWO AND THREE DIODES REPECTIVELY 26

FIGURE 19: ISOLATION FOR SPST SERIES CONFIGURATION SWITCH WITH ONE, TWO AND THREE DIODES REPECTIVELY 26

FIGURE 20: RETURN LOSS TRACES FOR SPST SERIES CONFIGURATION WITH ONE, TWO AND THREE DIODES REPECTIVELY 27

FIGURE 21: SERIES CONFIGURATION SPDT SWITCH 28

FIGURE 22: SERIES CONFIGURATION SPDT SWITCH WITH ADDITIONAL SERIES DIODE 29

FIGURE 23: SIMULATED RESULTS FOR SPDT SWITCH PRESENTED IN FIGURE 22 30

FIGURE 24: SIMULATED ISOLATION FOR SPDT SERIES CONFIGURATION SWITCH WITH ONE, TWO AND THREE DIODES REPECTIVELY 31

FIGURE 25: SHUNT CONFIGURATION SPST PIN DIODE SWITCH 32

FIGURE 26: SHUNT CONFIGURATION SPDT PIN DIODE SWITCH 32

FIGURE 27: INSERTION LOSS FOR A SHUNT CONFIGURATION SPST SWITCH IN A 50 Ω SYSTEM 34

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FIGURE 28: RF EQUIVALENT CIRCUIT OF A SHUNT CONFIGURATION SPST PIN DIODE SWITCH WITH PRACTICAL MODEL 34

FIGURE 29: ISOLATION VERSUS SERIES RESISTANCE (R_S) FOR A SHUNT CONFIGURATION SPST SWITCH IN A 50 Ω SYSTEM 36

FIGURE 30: SCHEMATIC USED FOR SIMULATING A SPST SHUNT CONFIGURATION SWITCH 39

FIGURE 31: SCHEMATIC FOR SIMULATING SHUNT CONFIGURATION SPST SWITCH WITH TWO DIODES 39

FIGURE 32: SIMULATION RESULTS OF SPST SWITCH WITH 2 SHUNT DIODES, DESIGNED TO OPERATE FROM 500 MHZ TO20 GHZ 40

FIGURE 33: SIMULATION RESULTS OF SPST SWITCH WITH 2 SHUNT DIODES, DESIGNED TO OPERATE FROM 500 MHZ TO30 GHZ 41

FIGURE 34: SHUNT CONFIGURATION SPDT SWITCH 42

FIGURE 35: SHUNT CONFIGURATION SPDT SWITCH WITH ADDITIONAL SHUNT DIODES 43

FIGURE 36: SIMULATED RESULTS FOR SPDT SWITCH PRESENTED IN FIGURE 34 44

FIGURE 37: SIMULATED RESULTS FOR SPDT SWITCH PRESENTED IN FIGURE 35 44

FIGURE 38: MODELLING PARAMETER EXTRACTION METHOD [10] 47

FIGURE 39: DE-EMBEDDED MODEL USED [10] 48

FIGURE 40: IN-FIXTURE CALIBRATION [10] 49

FIGURE 41: R&D TYPE TRL CALIBRATION KIT [10] 50

FIGURE 42: PHOTOGRAPH OF DESIGNED TRL CALIBRATION KIT 51

FIGURE 43: AUTOCAD DRAWING OF DESIGNED TRL CALIBRATION KIT 52

FIGURE 44: AUTOCAD DRAWING OF THRU STANDARD 54

FIGURE 45: AUTOCAD DRAWING OF REFLECT STANDARD 55

FIGURE 46: AUTOCAD DRAWING OF A LINE STANDARD 57

FIGURE 47: S_{11} OF THE THRU STANDARD ON SOFT SUBSTRATE 60

FIGURE 48: MEASURED PHASE OF S_{21} PARAMETER FOR THRU STANDARD ON SOFT SUBSTRATE ...61

FIGURE 49: PHOTOGRAPH OF THRU STANDARD ON SOFT SUBSTRATE 62

FIGURE 50: S_{11} OF THE THRU STANDARD ON HARD SUBSTRATE 62

FIGURE 51: MEASURED PHASE OF S_{21} PARAMETER OF THRU STANDARD ON HARD SUBSTRATE 63

FIGURE 52: PHOTOGRAPH OF THRU STANDARD ON HARD SUBSTRATE 64

FIGURE 53: MEASURED S_{11} OF THE THRU STANDARD ON HARD SUBSTRATE WITH AND WITHOUT 66

FIGURE 54: PIN DIODE MODEL USED FOR PARAMETER EXTRACTION 68

FIGURE 55: M-26 PACKAGING FROM MDT CORPORATION 69

FIGURE 56: INSERTION LOSS FOR MP61004 PIN DIODE IN M-26 PACKAGE 69

FIGURE 57: ISOLATION FOR MP61004 PIN DIODE IN A M-26 PACKAGE 70

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FIGURE 58: BEAM LEAD PACKAGE DIMENSIONS FOR HPND-4005 PIN DIODE[12] 72
FIGURE 59: INSERTION LOSS FOR HPND-4005 PIN DIODE 72
FIGURE 60: ISOLATION FOR HPND-4005 PIN DIODE 73
FIGURE 61: ELECTROMAGNETIC SIMULATION SCHEMATIC 74
FIGURE 62: ESTIMATED COUPLING ACROSS HPND-4005 PIN DIODE 74
FIGURE 63: TOP, SIDE AND FRONT VIEW OF THE P10 PACKAGE FOR MP61004 PIN DIODE (DIMENSIONS ARE IN MILS) 76
FIGURE 64: PHOTOGRAPH OF SERIES CONNECTED MP61004 PIN DIODE 77
FIGURE 65: INSERTION LOSS FOR SERIES CONNECTED MP61004 PIN DIODE WITH P10 PACKAGING 78
FIGURE 66: ISOLATION FOR SERIES CONNECTED MP61004 PIN DIODE WITH P10 PACKAGING 78
FIGURE 67: MODEL USED FOR DIODE CHARACTERISATION IN HARD SUBSTRATE 79
FIGURE 68: PHOTOGRAPH TAKEN UNDER MICROSCOPE OF A SHUNT CONFIGURATION WITH DIODE NEXT TO TRACK 80
FIGURE 69: INSERTION LOSS FOR MP61004 DIODE IN SHUNT CONFIGURATION WITH DIODE NEXT TO TRANSMISSION LINE 81
FIGURE 70: ISOLATION FOR MP61004 DIODE IN SHUNT CONFIGURATION WITH DIODE NEXT TO TRANSMISSION LINE 81
FIGURE 71: SCHEMATIC USED TO SIMULATE THE SHUNT CONFIGURATION. 82
FIGURE 72: PHOTOGRAPH TAKEN UNDER MICROSCOPE OF THE SHUNT CONNECTED DIODE WITH THE TRANSMISSION LINE SPLIT AND THE DIODE PLACED BETWEEN THE TRANSMISSION LINES 83
FIGURE 73: INSERTION LOSS FOR MP61004 DIODE IN SHUNT CONFIGURATION WITH DIODE PLACED BETWEEN THE TRANSMISSION LINES 83
FIGURE 74: ISOLATION FOR MP61004 DIODE IN SHUNT CONFIGURATION WITH DIODE PLACED BETWEEN THE TRANSMISSION LINES 84
FIGURE 75: MODEL USED FOR PARAMETER EXTRACTION 84
FIGURE 76: SCHEMATIC DIAGRAM OF SPST COMPOUND CONFIGURATION SWITCH 87
FIGURE 77: SCHEMATIC DIAGRAM OF SPDT COMPOUND CONFIGURATION SWITCH USED IN MWO90
FIGURE 78: SIMULATED RESPONSE FOR SPDT COMPOUND CONFIGURATION SWITCH SHOWN IN FIGURE 77 92
FIGURE 79: SCHEMATIC DIAGRAM OF SPDT COMPOUND CONFIGURATION SWITCH WITH ADDITIONAL SERIES DIODE 93
FIGURE 80: SIMULATED RESPONSE FOR SPDT COMPOUND CONFIGURATION SWITCH WITH ADDITIONAL SERIES DIODE 94

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FIGURE 81: SCHEMATIC DIAGRAM OF SPDT COMPOUND CONFIGURATION SWITCH WITH ADDITIONAL SHUNT DIODE 95
FIGURE 82: SIMULATED RESULTS FOR SPDT COMPOUND CONFIGURATION SWITCH WITH ADDITIONAL SHUNT DIODE 96
FIGURE 83: FLOW DIAGRAM OF PREFERRED COMPOUND SWITCH DESIGN APPROACH 102
FIGURE 84: SCHEMATIC DIAGRAM OF SPDT COMPOUND CONFIGURATION SWITCH WITH ADDITIONAL SERIES DIODE 103
FIGURE 85: LINEAR MODEL OF PIN DIODE USED IN SIMULATIONS 107
FIGURE 86: RESULTS OF THE SPDT SWITCH WITH JUNCTION T1 CHANGED TO 0.5 × 0.5MM 108
FIGURE 87: SWITCH RESPONSE AFTER CHANGES MADE IN SECTION 1 109
FIGURE 88: SWITCH RESULTS WITH ADDITIONAL DIODE ADDED 110
FIGURE 89: SIMULATION RESULTS FOR SWITCH WHERE IDEAL CAPACITORS AND INDUCTORS MODELS RE REPLACED WITH NON-IDEAL CAPACITORS AND INDUCTORS MODELS 113
FIGURE 90: SCHEMATIC OF FINAL OPTIMISED SWITCH 114
FIGURE 91: SIMULATED RESPONSE OF FINAL OPTIMISED SWITCH 115
FIGURE 92: FINAL LAYOUT OF SWITCH 116
FIGURE 93: PHOTOGRAPH TAKEN OF ETCHED SUBSTRATE 117
FIGURE 94: PHOTOGRAPHS OF FINAL CONSTRUCTED SWITCH 118
FIGURE 95: MEASURED RESPONSE OF THE SWITCH 119
FIGURE 96: MEASURED AND SIMULATED ISOLATION AND INSERTION LOSS OF THE SWITCH 120
FIGURE 97: MEASURED AND SIMULATED RETURN LOSS OF SWITCH 121

LIST OF TABLES

TABLE 1: PROPERTIES FOR SUBSTRATE USED IN SIMULATIONS 24

TABLE 2: PARAMETER VALUES FOR HPND-4005 PIN DIODE 24

TABLE 3: DESIGN PARAMETERS FOR SPST SERIES CONFIGURATION SWITCH 25

TABLE 4: DESIGN PARAMETERS FOR SPDT SWITCH SHOWN IN FIGURE 22 30

TABLE 5: PARAMETER VALUES FOR THE TWO SPST DESIGNS 41

TABLE 6: PARAMETER VALUES FOR SPSD DESIGN 44

TABLE 7: TRL SUBSTRATE PROPERTIES 53

TABLE 8: PROPERTIES OF MDT MP61004 PIN DIODE 69

TABLE 9: EXTRACTED PARAMETER VALUES FOR MP61004 IN M-26 PACKAGING 70

TABLE 10: PROPERTIES OF HPND-4005 PIN DIODE [12] 72

TABLE 11: EXTRACTED AND SPECIFIED PARAMETERS OF THE HPND-4005 PIN DIODE 73

TABLE 12: SPECIFIED PROPERTIES OF MP61004 PIN DIODE IN P10 PACKAGE 76

TABLE 13: SPECIFIED AND MEASURED PARAMETERS OF THE MP61004-P10 PIN DIODE 79

TABLE 14: SPECIFIED AND MEASURED PARAMETER VALUES FOR MP61004 DIODE IN P10 PACKAGE 82

TABLE 15: SPECIFIED AND MEASURED PARAMETER VALUES FOR MP61004 DIODE IN P10 PACKAGE 85

TABLE 16: EXTRACTED AND SPECIFIED PARAMETERS OF THE HPND-4005 PIN DIODE 106

TABLE 17: TRANSMISSION LINE LENGTHS TO PRODUCE RESULTS SHOWN IN FIGURE 87. ALL LINES NOT LISTED IN THE TABLE REMAIN UNCHANGED. 109

TABLE 18: TRANSMISSION LINE LENGTHS TO PRODUCE RESULTS SHOWN IN FIGURE 88. ALL LINES NOT IN THE TABLE REMAINS UNCHANGED. 111

TABLE 19: TRANSMISSION LINE LENGTHS AND WIDTHS FOR FINAL OPTIMISED SWITCH 115

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Glossary

AC	Alternating Current
dB	Decibel
DC	Direct Current
F_h	Highest operating frequency
F_L	Lowest operating frequency
F_m or F_0	Midband frequency
GHz	Gigahertz
HZ	Hertz
"I" region	Intrinsic region
kHz	Kilohertz
MHz	Megahertz
Microwave	Microwave frequency range
ms	Milliseconds
MWO	Microwave Office software package
ns	Nanoseconds
Ω	Ohm
RF	Radio Frequency
μs	Microseconds
VSWR (σ)	Voltage Standing Wave Ration
W	Watt

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1 Introduction

This document presents an analysis and design of a broadband PIN diode switch. The idea is to equip a designer with a set of "design tools" which will enable him/her to successfully design a switch that when built, the measured and simulated results should compare very well.

In order to achieve this, the fundamentals of the PIN diode device will first be discussed in Chapter 2. This will provide an adequate foundation to fully understand the switch operation.

Chapter 3 will provide an analysis and design procedure for the series and shunt configuration switches. The design procedures presented are not based on a theoretical study, but were developed by doing various simulations on these two configuration types, and in the process, gaining knowledge and experience on how to manipulate certain switch responses.

In the design of a practical switch, accurate models for components are required. The component information provided by the manufacturers is usually not sufficient. Chapter 4 will present a parameter extraction procedure that will enable a designer to extract very accurate component models.

In Chapter 5, a design procedure for the compound configuration switch will be presented. A practical switch will then be designed and built. The measured results will be discussed in Chapter 6.

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2 PIN diode physics

This chapter presents an overview on PIN diode fundamentals and operating characteristics to form an adequate basis for discussions in the subsequent chapters.

The most important property of a PIN diode is the fact that it can, under certain circumstances, behave as an almost pure resistance at RF and microwave frequencies. This resistance can be varied by varying the forward bias control current through the diode. A PIN diode is therefore a current controlled device.

When the forward bias current through the diode is varied continuously, it can be used for attenuating, levelling and amplitude control of an RF or microwave signal. When the control current is varied in discrete steps, the device can be used for phase shifting, pulse modulation or switching of an RF or microwave signal. The latter property of the diode, where it is used as a switching device, will be discussed in more detail in the following chapters.

The microwave PIN diode's small physical size compared to a wavelength, high switching speed and relatively low package parasitic elements, makes it an ideal component for use in broadband RF and microwave signal control circuits.

Another important feature of the PIN diode is its ability to control large RF and microwave signals by using much smaller level of dc excitation [1].

2.1 PIN diode fundamentals

A PIN diode is a semiconductor device consisting of a layer of intrinsic (high resistivity) material of finite area and thickness that is contained or sandwiched between two layers of highly doped P and N type materials. A model of a PIN diode is shown in Figure 1.

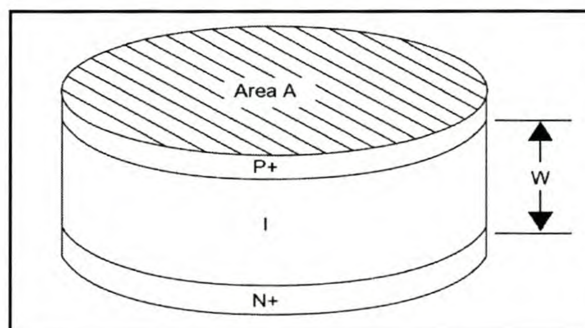

Figure 1: Pin diode chip geometry [1]

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The performance characteristics of the diode mainly depend on the chip geometry. Manufacturers manipulate the chip geometry to meet their specific requirements or needs in terms of:

1. Switching speed
2. Reverse biased junction capacitance
3. Forward biased resistance
4. Power handling capability
5. Carrier lifetime
6. Breakdown voltage
7. Distortion

Most of the above-mentioned requirements are in some way related to each other and manipulating some of them, usually means making a trade-off between them.

The following sections will discuss how the diode reacts in its different bias states and show how the diode operations are frequency related.

The contents of the following sections are a combination of information taken from references [1], [2], [3] and [4] and the references will therefore not always be explicitly indicated.

2.1.1 Forward biased PIN diode

When the diode is forward biased, charge (holes and electrons) is injected into the intrinsic, or "I" region, from the P and N layers. These charges do not recombine instantaneously but has a finite lifetime, τ, in the "I" region. This results in an average stored charge, Q, which lowers the resistivity of the "I" region.

The charge in the "I" region is related to the diode current by:

$$I_d = \frac{dQ_d}{dt} + \frac{Q_d}{\tau} \quad A \qquad 2.1$$

where I_d = Diode current.

Q_d = Charge stored in the diode.

τ = Carrier recombination lifetime.

If the diode is biased with only a constant current, the stored charge is constant, and from equation 2.1 is equal to:

$$Q_d = I_d \tau \quad [Coulombs] \qquad 2.2$$

Equation 2.2 shows that the charge is dependent on the bias current as well as the carrier life of the diode.

If the biasing consists of both a dc current and a time varying signal (ac) component, the dc component of the charge will be modulated by the presence of the ac component. The degree of modulation depends on the relative level of the two charge components as well as the frequency of the ac signal. The frequency dependence of the modulation can be seen by solving the Laplace transform of equation 2.1, which yields:

$$Q_d = \frac{i_d \tau (j\omega)}{1 + j\omega\tau} \quad [Coulombs] \qquad 2.3$$

where $\omega = 2\pi f$

The result of equation 2.3 is plotted in Figure 2. It can be seen that at frequencies below $f_c = 1/2\pi\tau$, the ac signal has the same effect as the dc bias component. Above f_c however, the modulation effect decreases with about 6 dB/octave. The frequency f_c therefore determines the lowest operating frequency of the diode.

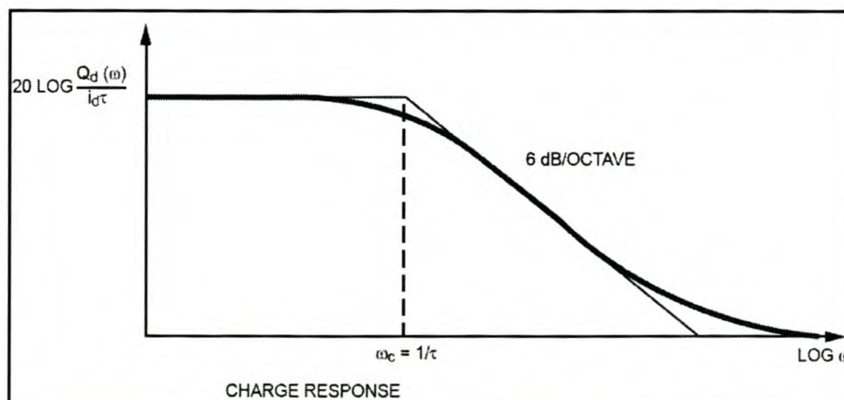

Figure 2: PIN diode charge response as a function of frequency [3]

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The carrier lifetime, τ, which affects f_c, is determined by the design of the diode and is the primary parameter that influences the switching speed. The typical lifetime of a PIN diode can vary between 5 ns to 80 μs depending on the desired use or function of the diode.

The carrier lifetime is not the only parameter that determines the lowest operating frequency of the diode. An equally important parameter, is the "I" region thickness which relates to the transit time frequency, f_T, of the diode. Equation 2.4 shows the formula for calculating f_T for a silicon diode. The highest of the frequencies f_c or f_T determines the actual lowest operating frequency of the diode. In this document it is assumed that f_c is higher that f_T.

$$f_T > \frac{1300}{W^2} \quad [MHz] \qquad \text{(where W in } \mu\text{m)} \qquad 2.4$$

If operated below f_c, the diode behaves as a normal PN junction diode. The RF signal incident on the diode will be rectified and the signal will be distorted considerably. In the vicinity of f_c the diode behaves as a linear resistor with a small non-linear component present. The RF signal still has some degree of distortion. In theory, at frequencies well above f_c, the diode behaves like a pure linear resistance. The value of the resistance is controlled by the dc (or low frequency) control bias signal. At high frequencies, the diode becomes to "slow" to respond to the signal and cannot switch between the forward and reverse bias states. To a high frequency RF signal, a forward biased diode therefore looks like a resistance, and the signal travels through the diode without any distortion. A practical diode, however, will never present a 100% linear resistance, and this small nonlinear resistance effect will lead to low intermodulation distortion of the signal.

The resistance, R_s, of the "I" region, at RF or microwave frequencies well above f_c can be expressed as:

$$R_s = \frac{W^2}{(\mu_n + \mu_p) Q_d} \quad [\Omega] \qquad 2.5$$

where W = "I" region width

μ_N = electron mobility

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μ_P = hole mobility

If the diode is biased with a constant current source, R_s can be written as an inverse function of the forward bias current through the diode by combining equations 2.2 and 2.5, then:

$$R_s = \frac{W^2}{(\mu_n + \mu_p) I_d \tau} \; [\Omega] \qquad 2.6$$

Equation 2.6 shows that R_s has a hyperbolic relation to I_d. Equation 2.6 also shows that in theory, R_s is independent of the area of the "I" region. In a practical diode, R_s is dependent on the area because the effective carrier lifetime is dependent on the area and thickness, due to edge recombination effects. The R_s versus I_d trace for a HPND-4005 beam lead PIN diode is shown in Figure 3. The graph is copied from the datasheets of this diode. It shows how a typical R_s versus I_d trace for a PIN diode looks like.

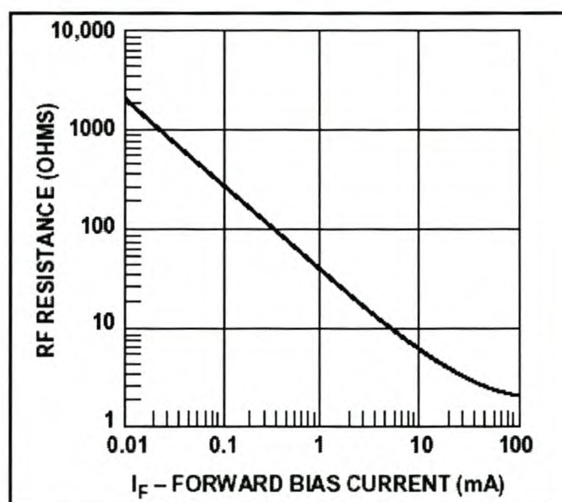

Figure 3: R_s versus I_d trace for HPND-4005 PIN diode [12]

2.1.1.1 Simplified linear high frequency model of forward biased PIN diode

A simplified linear high frequency model for a forward biased PIN diode is presented in Figure 4. L is the package inductance that will be discussed in more detail in section 2.1.3 and R_s is the RF resistance derived in equation 2.6.

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Figure 4: Simple linear model of a forward biased PIN diode

2.1.2 Reverse biased PIN diode

When the diode is reverse biased, ideally no charge is stored in the "I" region and the diode appears as a capacitor shunted by a parallel resistance. The formula for calculating the capacitance is shown in equation 2.7. The capacitance depends only on the geometry of the "I" region layer. Equation 2.7 is also the equation used for calculating the parallel plate capacitance where the effects of the fringing field are ignored.

$$C = \frac{\varepsilon A}{W} \quad [F] \qquad 2.7$$

where ε = Dielectric constant

A = Junction area

W = "I" region thickness

Equation 2.7 is only valid at frequencies above the dielectric relaxation frequency, f_r, of the "I" region. Equation 2.8 shows the formula for calculating the dielectric relaxation frequency.

$$f_r > \frac{1}{2\pi\rho\varepsilon} \quad [Hz] \qquad 2.8$$

where ε = Dielectric constant

ρ = "I" region resistivity

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If the diode is taken from a forward bias state to a zero bias state, there remains some finite charge stored in the "I" region. This is due to impurities in the "I" region. This charge however is not mobile. The shunt resistance mentioned in the previous paragraph presents this stored charge. If the diode is operated in the above-mentioned state, it behaves like a lossy capacitor. To sweep out the remaining fixed charge from the "I" region, some small reverse DC voltage must be applied. If all the carriers are depleted from die "I" region, the diode looks like a lossless capacitor.

2.1.2.1 Simplified linear high frequency model of reverse biased PIN diode

A simplified linear high frequency model of a reverse biased PIN diode is presented in Figure 5. In the model, L is the package inductance, C is the RF capacitance derived in equation 2.7, and R represents the conductivity of the "I" region if charge exists in this region when the diode is zero or reverse biased. R is associated with the loss factor of the diode's capacitance and is proportional to voltage across the diode and inversely proportional to frequency. In most RF or microwave applications the value of R is higher than the reactance of the capacitance, C, and is therefore less significant.

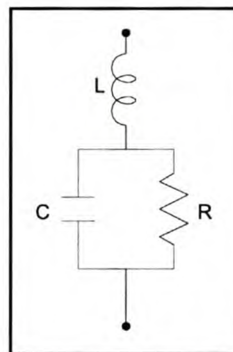

Figure 5: Simple linear model of a reverse biased PIN diode

2.1.3 Equivalent low and high frequency model of the PIN diode

From the diode behaviour shown in Figure 2, it can be seen that the equivalent circuit for the diode is frequency dependant. This section will discuss these frequency related models for the PIN diode. In the discussions to follow, the topology of the equivalent circuit model presented in Figure 6 and Figure 7 stays the same; it is just the meaning and values of some of the elements that change.

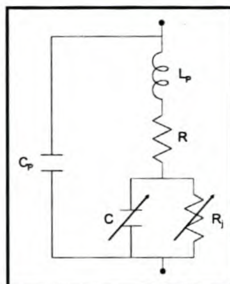

Figure 6: Low frequency equivalent circuit of a PIN diode

The low frequency (below fc) model for the diode is shown in Figure 6. This model is equivalent to that of a normal PN junction diode. The parasitic package inductance and capacitance, Lp, and Cp, depends only on the type of packaging used for the diode. The diode leads and/or the bonding wire within the package both contribute to Lp. R is the resistance of the diode leads and C is equal to the junction capacitance, which is a function of applied voltage. R_j is the junction resistance and is equal to:

$$R_j \cong \frac{nkT}{qI_{dc}} \quad [\Omega] \qquad 2.9$$

Where I_{dc} = Forward bias current

At frequencies in the region of f_c it is difficult to set up a standard equivalent circuit since the diode's behaviour may differ. Depending on the way the device was designed by the manufacturer, it can reflect a behaviour that is more inductive or more capacitive of nature.

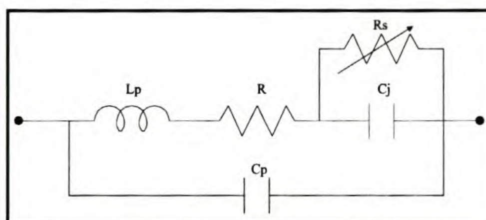

Figure 7: High frequency equivalent circuit of a PIN diode

The equivalent model for the diode at frequencies much higher than f_c is presented in Figure 7. The package elements L_p, C_p and R stays the same as in low frequency model since it's related to the diode packaging. The junction capacitance, C_j, represents the "I" region capacitance (equation 2.7). C_j should be zero in the forward biased state since the "I" region is

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then conducting. In a practical diode, however, it presents a small capacitance effect and is then referred to as C_d, the diffusion capacitance. R_s presents the effective "I" region resistance. Even though this value is shown as variable, the resistance is nearly constant with respect to an RF signal. The value of R_s depends on the biasing state (see sections 2.1.1 and 2.1.2 above).

2.2 Packaging parasitic elements

The parasitic elements discussed above depend on the type of packaging used for the diode. Figure 8 shows a few types of packaging used in the industry. Figure 8 also show some typical parasitic element values associated with some packages.

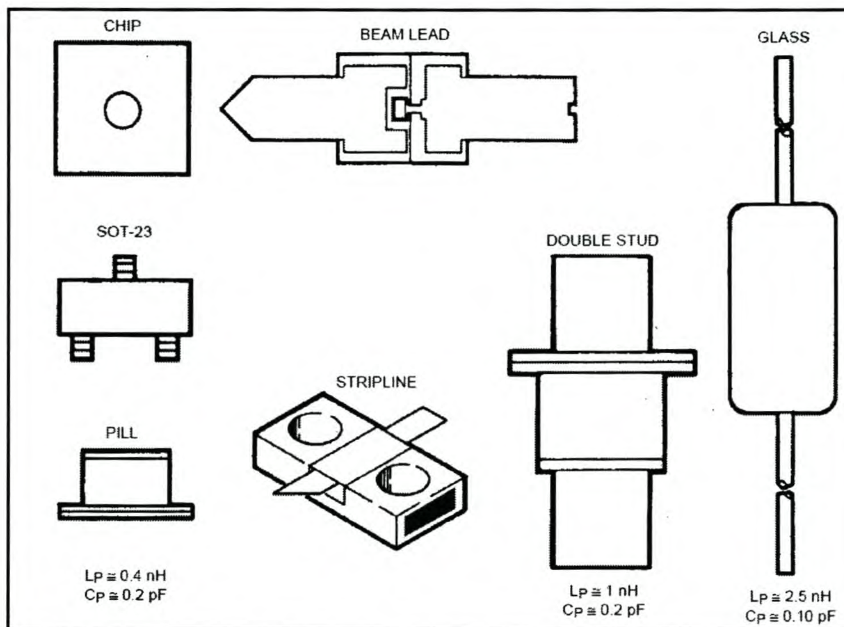

Figure 8: Types of packaging [3]

Each type of packaging has its own advantages and disadvantages. The trick is to find the right package for your application. Many factors play a role in choosing the right package for the diode. Typical factors are:

- Frequency range
- Type of substrate used
- Technology used for circuit assembly and manufacturing
- Diode configuration

2.3 PIN diode switching characteristics

Switching speed can be defined in many ways. It is more sensible to define switching speed in terms of the application the diode is being used in. In switching applications, it is the time required to fill or remove the charge from the "I" region or in other words, the transition time from the minimum insertion loss state to the high isolation state and vice versa [1].

Let's consider the case where the diode is switched from forward biased to reverse biased. When the diode is forward biased by the current, I_F, a charge equilibrium exists in the "I" region. This stored charge condition causes the diode to be in a low resistance state. If the diode is suddenly reverse biased, the positive and negative charge takes a time, τ , to recombine. During this recombination time, a reverse current, I_R, can flow through the diode. Only after all the charge is removed from the "I" region, will the diode stop conducting and go into the capacitive state. T_{FR}, the forward to reverse biased switching time, is dependant on I_F, I_R and the carrier lifetime, τ , and can be expressed as [1]

$$T_{FR} = \ln\left(1 + \frac{I_F}{I_R}\right)\tau \qquad \text{[sec]} \qquad 2.10$$

A typical shape of a I_F vs. time trace is shown in Figure 9.

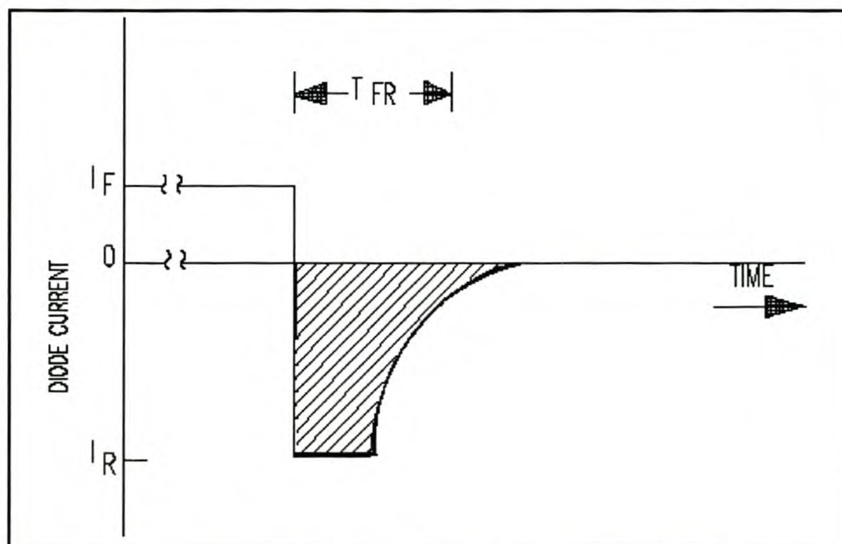

Figure 9: PIN diode forward to reverse biased switching speed [1]

This trace can be manipulated by the driver circuit to suite the application the diode is used for.

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Let's consider the case where the diode is switched from the reverse to the forward biased state. If the reverse bias voltage is sufficient, the "I" region will be fully depleted of mobile carriers. When the diode is forward biased, the depletion region will collapse almost instantaneously and the injection of carriers begins in a finite time to fill the "I" region. The time required to fill the "I" region primarily depends on the transit time (equation 2.4) of the "I" region. The reverse to forward biased switching time, T_{RF}, is usually faster than the forward to reverse biased switching time, T_{FR} [1].

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3 Switch topologies

The definitions of terminologies that are used to characterise a switch will be discussed in this chapter. Throughout this document, these stated definitions will then be used.

The series and shunt configuration switches, with their typical properties, will then be reviewed and discussed. Design guidelines for both configuration types will be presented and evaluated, with simulation results shown to confirm the validity of the guidelines. In the evaluation process, a few ideal switch designs will be performed. These will show the typical properties of the configuration types, and the advantages and disadvantages of using them.

In this document, it is assumed that microstrip circuits are used. All the presented equations are valid only for microstrip circuits.

3.1 Switch terminology

This section gives an insight on general switch terminology and definitions of parameters, some of which will be used in discussions in the succeeding sections and chapters. These parameters are generally used to characterise or specify a switch.

3.1.1 "ON" and "OFF" states of switch

The "on" state refers to the conducting (low resistance) state of the switch. In this state, ideally the RF signal travels from the input to the output port without any attenuation or distortion.

The "off" state refers to the isolation (high impedance) state of the switch where in theory, no RF signals travel from the input to the output ports.

3.1.2 Absorptive and reflective switch

An absorptive switch, also known as a non-reflective switch, is a switch that presents a low VSWR in both its "on" and "off" states. This simply means that in both switching states, the RF input and output ports are matched to its load.

A reflective switch presents a high VSWR in its "off" state and a low VSWR in its "on" state. It is therefore only matched at the RF input and output ports when in its "on" state.

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3.1.3 Insertion loss

Insertion loss is the attenuation of RF power measured between the input and output ports of the switch when in its "on" state.

When the switch is in its "on" state, depending on the switch topology, large values of bias as well as RF current may flow through the switch structure. This causes a significant amount of ohmic loss [5].

3.1.4 Isolation

The isolation is a measure of the RF power that is not transferred from one port to the other, both from attenuation loss and reflection loss, when the switch is in the "off" state. It is a measure of how effective the switch is turned off. It is determined by calculating the difference in the power measured at the output port when the switch is biased in the "on" state, and the power measured at the output port with the switch biased in the "off" state, while keeping the input port power constant [5]. Therefore:

$$\text{Isolation} = \left(P_{out}\right)_{on} - \left(P_{out}\right)_{off} \quad \text{[dB]} \qquad 3.1$$

3.1.5 Video leakage

Video leakage refers to the spurious signals present at the RF ports when it is switched between the "on" and "off" states, without any RF signal present. These signals arise from the waveforms generated by the switch driver and, in particular, from the leading edge voltage spike required for high speed switching of PIN diodes. When measured in a 50 Ω system, the magnitude of the video leakage can be as much as several volts.

The magnitude of the video leakage can be reduced significantly by the inclusion of high pass or "video filters" in the switch, but the high frequency signals that fall within the pass band of the switch can be eliminated by reducing the switching speed [6].

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3.1.6 Switching speed

No standard definition for switching speed exists. The most common definitions used are stated in sections 3.1.6.1 to 3.1.6.4. In the definitions stated, it is assumed that when the control signal goes "high", the switch goes into its "on" state and vice versa. Figure 10 is a graphical representation of the definitions.

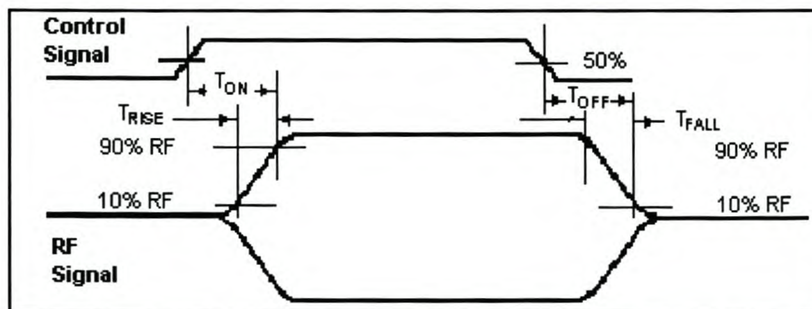

Figure 10: Switching speed definitions [7]

3.1.6.1 Rise Time

The rise time is the time it takes the RF signal to rise from 10% to 90% of the "on" level when the switch is switched to the "on" state (see Figure 10).

3.1.6.2 Fall Time

The fall time is the time it takes the RF signal to fall from 90% to 10% of the "on" level when the switch is switched to the "off" state (see Figure 10).

3.1.6.3 ON Time

The ON time is the time measured from 50% of the control signal to where the RF signal reaches 90% of its "on" level (see Figure 10).

3.1.6.4 OFF Time

The OFF time is the time measured from 50% of the control signal to where the RF signal reaches 10% of its "on" level (see Figure 10).

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3.1.7 SPST switch

A Single Pole Single Throw (SPST) switch has only two RF ports. In the "on" state, RF power is conducted from one port to the other while in the "off" state, RF power is isolated from one RF port to the other.

3.1.8 SPDT switch

The Single Pole Double Throw (SPDT) switch has three RF ports, one common port and two input/output ports. It is a combination of two SPST switches joined at a common port. It operates in a similar way to the SPST switch with the only difference being that RF power can be directed from the common RF port to either one of the other two input/output RF ports. It is important to note that RF power from the common port can only be directed to one of the output ports at a time. While power is directed to the one port, the other port is isolated from both the common port as well as the port to which the RF power is directed.

3.1.9 SPMT switch

When referred to a Single Pole Multi Throw (SPMT) switch, it implies the switch has M+1 RF input/output ports. A SPMT switch is a combination of M SPST switches joined at one common port. As with the SPDT switch, RF power can only be directed from the common port to one of the other M ports. While power is directed to one port, the other M-1 ports are isolated from both the common port as well as the port to which the power is directed.

3.2 Switch configuration

Ideally, one would want to design a switch with zero insertion loss, infinite isolation, no video leakage, be perfectly matched (when desired) and switch instantaneously. It is however not possible to manufacture such a perfect switch and usually a trade-off must made between these switch properties.

In designing a switch, the switch configuration is a very important choice to make. Every configuration has its own advantages and disadvantages. This section will discuss the series and shunt configuration switches with their advantages and disadvantages. It will then become apparent how the parameter trade-offs and the switch configuration choice are closely related

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to each other as well as which parameters influences which specific switch properties. Some preferred design guidelines for each topology will be presented and discussed.

The design of a compound configuration switch will be discussed in Chapter 5.

3.2.1 Series configuration switch

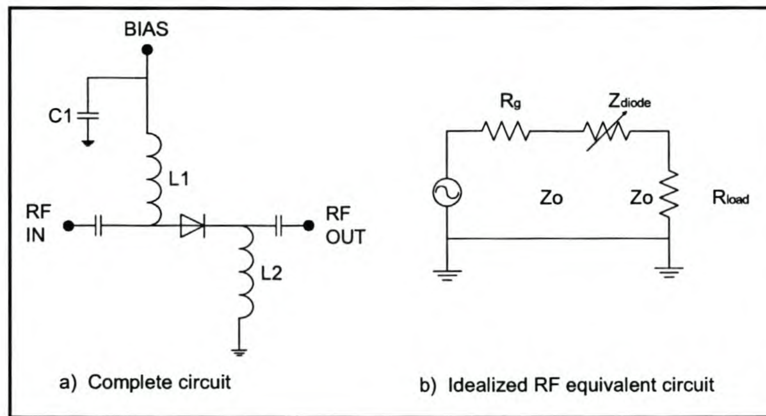

Figure 11: Series configuration SPST PIN diode switch

Figure 11 shows a schematic drawing and RF equivalent circuit of a series configuration SPST PIN diode switch. In this configuration, the PIN diode is connected in series with the transmission line.

The switch works as follows: It is turned "on" by forward biasing the diode and turned "off" by reverse biasing the diode. In the "on" state, RF power is conducted from the input to the output RF port through the diode. In the "off" state, RF power is reflected at the diode since it presents a high impedance.

The biasing network consists of the inductor L1 and capacitor C1. The inductor is used as an RF choke. From an RF point of view, the choke presents a high impedance in parallel with the RF path, and therefore minimal RF power is lost in the biasing network. From a dc point of view, the inductor provides a path for the dc biasing current. The capacitor forms part of a low pass filter that is implemented in the biasing network. The design of the biasing network will be discussed in Chapter 5.

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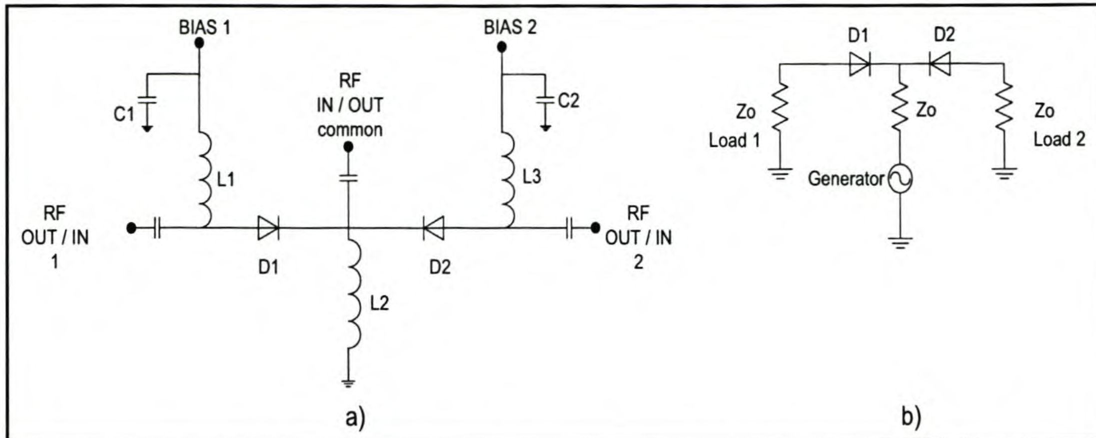

Figure 12: SPDT series configuration PIN diode switch

Figure 12 shows a schematic diagram and RF equivalent circuit of a SPDT series configuration switch. From the schematic, it is clear that it is a combination of two SPST switches joined at a common port. The biasing is similar to that of the SPST switch. By forward biasing D1, RF power is directed from the common port the RF port 1. By reverse biasing D1, the two ports are isolated from each other. The same applies for biasing D2. RF power can only be directed from the common port to one RF output port at a time.

The series configuration switch is often used for broadband applications where minimum insertion loss is required [2]. The insertion loss and power dissipation of the series switch primarily depends on the diode's series resistance, while the isolation is a function of the diode's junction and parasitic package capacitance.

3.2.1.1 Insertion loss

The insertion loss for a series configuration switch is primarily a function of the series resistance of the diode. A formula for calculating the insertion loss for a SPST series configuration switch is shown in equation 3.2. The derivation of equation 3.2 is shown in the appendices.

$$Insertion\,loss = 20\log_{10}\left[1 + R_s/2Z_0\right] \quad [dB] \qquad 3.2$$

where R_s is the forward biased RF resistance of the PIN diode.

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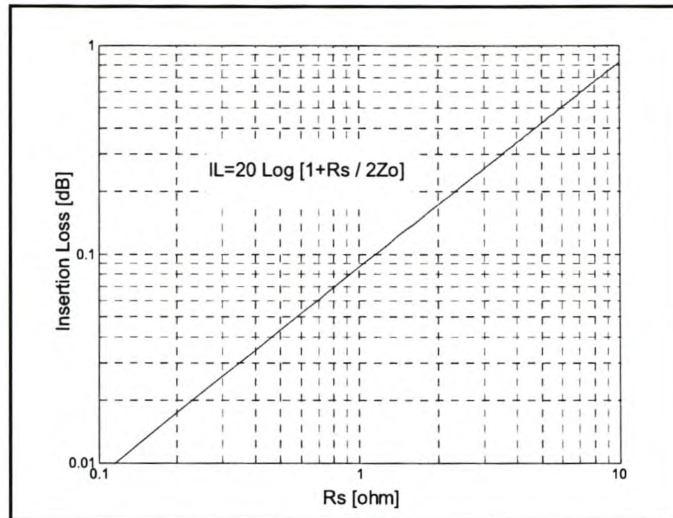

Figure 13: Insertion loss versus series resistance (R_S) for a series configuration SPST PIN diode switch in a 50 Ω system

Equation 3.2 is graphically presented in Figure 13 with Z_0 = 50 Ω. In the equation, it is assumed that the diode is ideal and presents a pure resistance with no parasitic elements (see Figure 11b).

In Chapter 5 it will be shown that in a practical diode, this is however not the case. Parasitic elements are always present and have to be taken into account. Figure 14 shows a circuit where a more realistic model of a practical diode is used as opposed to the model used in Figure 11 b.

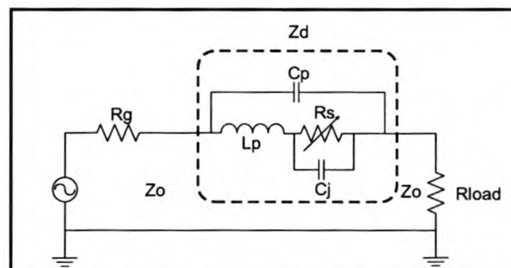

Figure 14: RF Equivalent circuit of a series configuration SPST PIN diode switch with practical diode model

A practical diode contains several reactance elements and consequently, the insertion loss becomes frequency dependant. If $R_S^{'}$ and $X_S^{'}$ are the series equivalent resistance and reactance of the diode, then $Z_d = R_S^{'} + jX_s^{'}$. If R_s in equation 3.2 is replaced with Z_d [3], then:

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$$Insertion\,loss = 10\log\left[\frac{\left(\frac{R_s^{'}}{Z_0}+2\right)^2+\left(\frac{X_s^{'}}{Z_0}\right)^2}{4}\right] \quad [dB] \qquad 3.3$$

The insertion loss equation for the SPST switch is also valid for the SPDT switch. The equation only gives the insertion loss for the diode itself. Other losses in the transmission lines, biasing network and reverse biased diode are not accounted for, but do influence the total measurable insertion loss. These additional losses have to be calculated and added together in order to calculate the total insertion loss for the switch.

3.2.1.2 Isolation

The isolation for the series configuration switch is primarily a function of the junction and package capacitance of the diode. For narrow bandwidth switches, this is not a problem because the total (package + junction) capacitance can be tuned out at a specific frequency. For broadband applications, the total capacitance however is a problem.

The formula for calculating the isolation for a SPST configuration switch is shown in equation 3.4. The derivation is done in the appendices.

$$Isolation = 10\log_{10}\left[1+1/\left(4\pi fCZ_0\right)^2\right] \quad [dB] \qquad 3.4$$

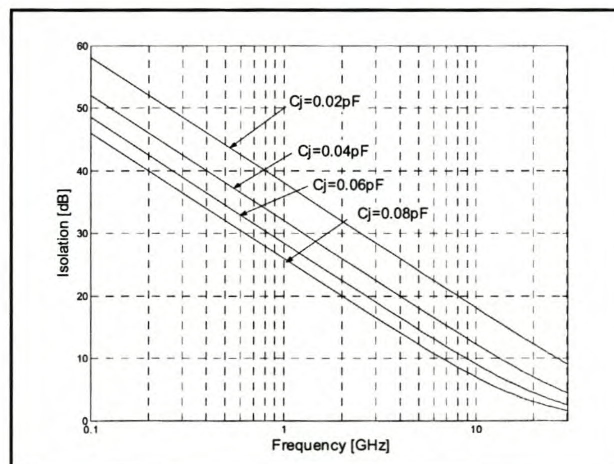

Figure 15: Isolation for a series SPST PIN diode switch in a 50 Ω system

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The isolation for the SPST series configuration switch is graphically presented in Figure 15 as a function of the junction capacitance. It gives an idea of the isolation that can be expected if the junction capacitance is known.

Equation 3.3 can also be used to find the isolation of a practical diode if the impedance of the practical reverse biased diode is known and can be written in the form $Z_d = R_S^{'} + jX_s^{'}$.

With a SPDT configuration switch, it is assumed that the common port is always "connected" to one RF output port while being isolated from the other. From Figure 12 b) it can be seen that, when one diode is forward biased and the other reverse biased, only half of the RF generator voltage applied in the SPST configuration, is applied to the reverse biased diode in the SPDT configuration. This happens because the generator is always being presented with a matched load on the "on" port. This decrease in voltage provides an additional 6 dB of isolation. An additional 6 dB must therefore be added to equation 3.4 in order to find the isolation for a SPDT or SPMT series configuration switch [8]. Equation 3.5 gives the isolation for a SPMT switch.

$$Isolation_{SPMT} = 10\log_{10}\left[1 + 1/\left(4\pi f C Z_0\right)^2\right] + 6 \quad [dB] \qquad 3.5$$

3.2.1.3 Power Dissipation

The power dissipation in the diode for a series configuration switch is [2]:

$$P_D = \frac{4R_s Z_0}{\left(2Z_0 + R_s\right)^2} \bullet P_{AV} \quad [\mathrm{W}] \qquad 3.6$$

and for $Z_0 >> R_s$ equation 3.6 can be simplified to:

$$P_D \approx \frac{R_s}{Z_0} \bullet P_{AV} \quad [\mathrm{W}] \qquad 3.7$$

where the maximum available power is given by:

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$$P_{AV} = \frac{V_G^2}{4Z_0} \quad \text{[W]} \qquad 3.8$$

It should be noted that equations 3.6 and 3.7 only apply for matched switches. For VSWR (σ) values other than unity, P_{AV} must be multiplied by the factor $[2\sigma/(\sigma+1)^2]$, designated "sigma", to obtain that maximum required power dissipation rate of the diode [2].

3.2.1.4 Peak RF current

The peak RF current that will flow through the series connected diode is given as:

$$I_p = \sqrt{\frac{2P_{AV}}{Z_0}} \quad \text{[A]} \qquad 3.9$$

Equation 3.9 applies only for a matched switch. If it is not matched, the value of P_{AV} must be adjusted as shown in section 3.2.1.4 above.

3.2.1.5 Peak RF voltage

The peak RF voltage that can exist across the diode in a SPST configuration is given in equation 3.10 :

$$V_p = \sqrt{8P_{AV}Z_0} \qquad 3.10$$

For a SPMT configuration, the RF voltage is [2]:

$$V_p = \sqrt{2P_{AV}Z_0}\left(\frac{2\sigma}{\sigma+1}\right) \qquad 3.11$$

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If the switch is not matched, P_{AV} in equation 3.10 must be adjusted as discussed in section 3.2.1.3.

3.2.1.6 Manufacturing

From a manufacturing point of view, the major advantage of the series connected switch is the fact that it is very easy to construct. It can be manufactured on both hard and soft substrate with no real advanced technology needed. All diodes are placed on top and in series with the microstrip lines, and consequently, no ground problems exist. Chip and beam lead diodes are favoured for this topology, depending on the manufacturing facilities.

3.2.1.7 General design information

This section will provide guidelines for designing of a series configuration switch. These design guidelines are based on simulations performed on the switch configuration. The simulation results will be shown and discussed. The Microwave Office (MWO) software package was used to perform the simulations in.

It is assumed that, unless stated otherwise, the components (diodes, inductors, capacitors) used in the simulations are ideal and that the switch is used in a 50 Ω system. The integration of the practical components into the design is discussed in Chapter 5.

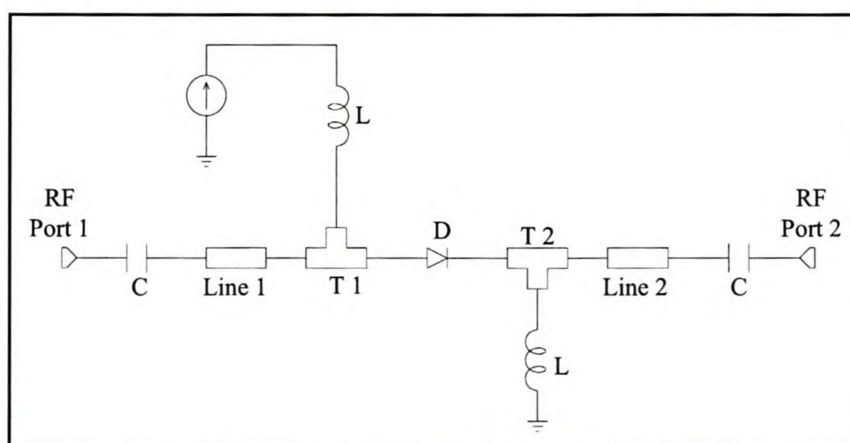

Figure 16: Schematic used for simulating a series configuration SPST switch

Figure 16 shows the schematic drawing used in MWO to simulate the properties of the series configuration SPST switch. The junctions T1 and T2 are configured to have rectangular

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shapes, and not T-shapes. If not stated otherwise, the width of the junctions are the same as that of the adjacent lines, and the length long enough to mount the inductor onto it.

By using this T-junction instead of a transmission line, the simulations are more accurate. The properties for the substrate and diode used in the simulations are shown in Table 1 and Table 2.

Designation	CER – 10 (Taconic)
Substrate thickness (h)	25 mil and 15mil
Dielectric constant (ε_r)	9.5
Copper thickness (t)	18 um
Dissipation factor ($\tan\delta$)	0.0035

Table 1: Properties for substrate used in simulations

Part number	HPND-4005
Series resistance (R_s) @ 20 mA	4.7 Ω
Capacitance (C_j) @ V_r = 10 V	0.017 pF
Minority carrier lifetime (τ)	50 ns

Table 2: Parameter values for HPND-4005 PIN diode

3.2.1.7.1 SPST switch

As previously mentioned, the SPST series configuration switch generally has a very good insertion loss property, but cannot provide very high isolation, even if two or more diodes are connected in series.

The design guidelines for the switch shown in Figure 16 are:

- **General information**
  For maximum isolation and return loss, and minimum insertion loss, Lines 1 and 2 should have a characteristic impedance of Z_0 at the midband frequency, f_0. These line lengths should also be kept as short as possible to minimize the insertion loss.

- **Improved isolation**
  To improve the isolation, additional series diodes can be added. Figure 17 shows a schematic drawing where an additional diode has been added to the switch shown in Figure 16. Any number of these sections can be added. For best overall performance in terms of return loss, isolation and insertion loss, the spacing between the diodes,

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provided by Line 3, should be λ/4 at the highest operation frequency, f_h. Lines 1 and 2 must have an impedance Z_0 at f_0 to ensure sufficient matching at the RF ports.

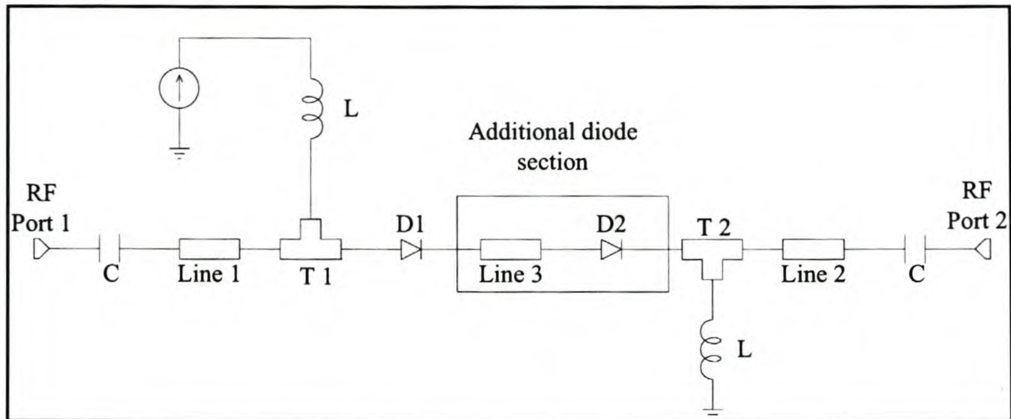

Figure 17: SPST series configuration switch with two series diodes

- **Simulation results**

Figure 18, Figure 19 and Figure 20 show the simulation results for the SPST series configuration switch which was designed to operate from 500MHz to 30GHz. The switch was designed with one, two and three series diodes respectively. The idea with the design was not to meet specific requirements, but only to show how the switch response is influenced with the additional diodes added.

The design parameters are shown in Table 3. The idea in this section is to characterise the properties of the switch, and therefore the dc decoupling capacitor and RF choke values, C and L, are set to 100 pF and 100 nH respectively. This is done in order to minimise their influence on the switch properties.

Diode	HPND-4005
Substrate thickness	25mil
Line 1; Line 2 (L × W)	5 x 0.69 mm (Z = 50 Ω @ 15 GHz)
Line 3 (L × W)	0.9 x 0.69 mm (L = λ/4@30 GHz; Z = 50 Ω @ 15GHz)

Table 3: Design parameters for SPST series configuration switch

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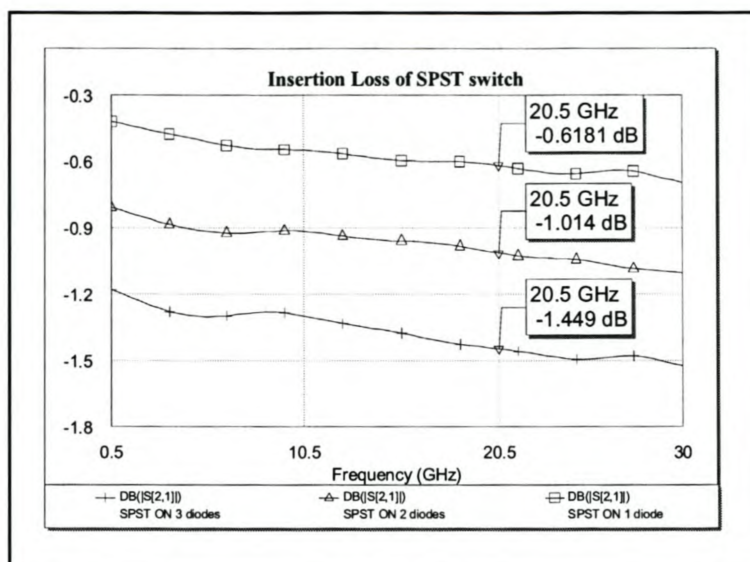

Figure 18: Insertion loss for SPST series configuration switch with one, two and three diodes respectively

Figure 18 shows the insertion loss for the switch. The switch with one diode has an insertion loss of 0.6181 dB. From Figure 13, the expected loss in a diode with a series resistance of 4.7 Ω is 0.4 dB. The simulated transmission line loss in this switch at 20.5 GHz, without the diode is about 0.22 dB. By adding the transmission line loss and the loss in the diode, the expected insertion loss compares well to the simulated 0.6181 dB. With the addition of a second and third diode, the insertion loss increased with the expected 0.4 dB per diode added.

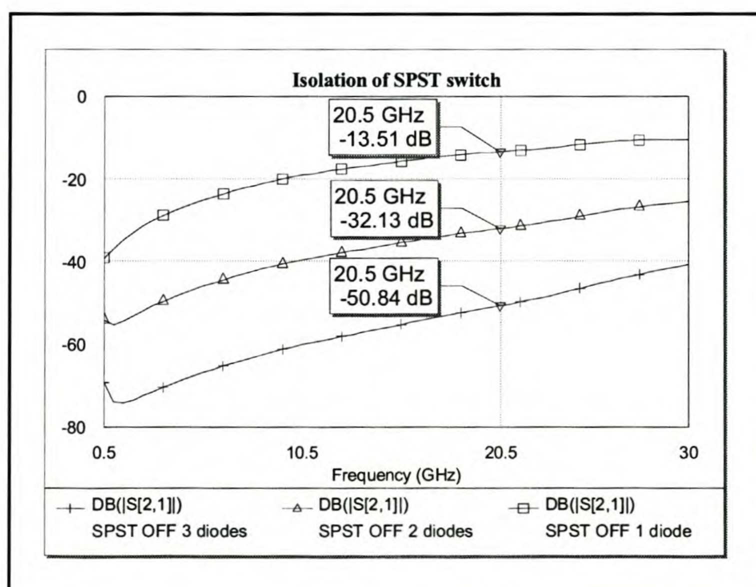

Figure 19: Isolation for SPST series configuration switch with one, two and three diodes respectively

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The simulated isolation is shown in Figure 19. From equation 3.4, the isolation for a diode with a junction capacitance of 0.017 pF equals 13.4 dB at 20.5 GHz . This very closely corresponds to the simulated value of 13.51 dB. If additional diodes were to be added, the isolation is expected to increase with the same amount that a single diode can contribute to. In this specific application, the isolation is expected to increase with 13.4 dB at 20.5 GHz. In Figure 19 it can be seen that the isolation improved with about 19 dB per diode added. This phenomenon arises from the optimal spacing between the diodes.

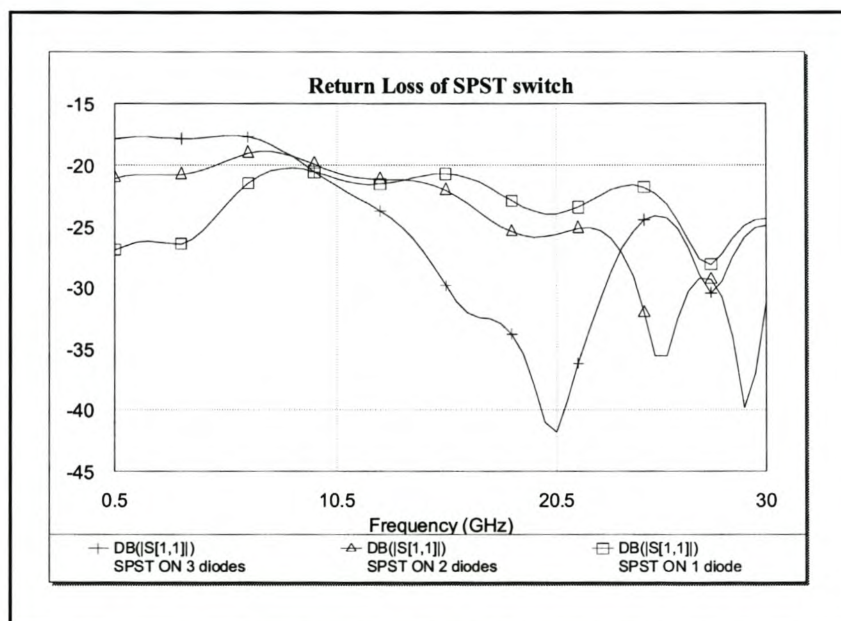

Figure 20: Return loss traces for SPST series configuration with one, two and three diodes respectively

From Figure 20 it can be seen that the switch is well matched across the operating band of the switch.

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3.2.1.7.2 SPDT switch

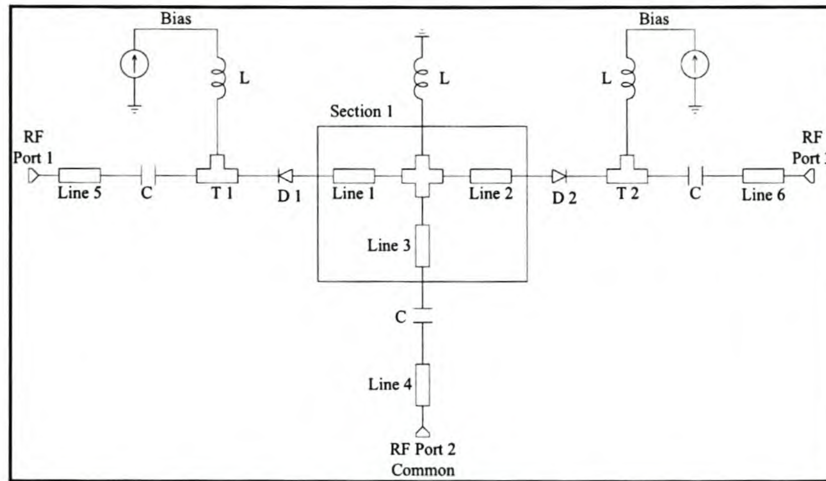

Figure 21: Series configuration SPDT switch

Figure 21 shows a schematic diagram of a series configuration SPDT switch. The switch is symmetrical around the common port, so Line 1 is equal to Line 2, and Line 5 equal to Line 6. Although the SPDT switch can also operate across a very broad band, it is not as broadband as the SPST switch. This is mainly due to the loading of the "off" arm of the switch. Generally, when designing a SPDT switch, a trade off has to be made between bandwidth and return loss at the RF ports.

The preferred design guidelines for a broadband SPDT series configuration switch are:

- **Section 1**

  In a broadband SPDT switch design, the most critical part in the design is the section marked "Section 1" in Figure 21. Section 1 mostly influences the bandwidth and insertion loss of the switch. Generally, for maximum bandwidth, the transmission line lengths and widths, and junction area in Section 1, has to be as short and small as possible, but keeping in mind that component sizes are the physical limitations of the minimum lengths and widths. For optimum bandwidth, Lines 1, 2 and 3 have to be identical in length and width, and the junction has to be configured as a square with the same widths as the transmission lines.

  The type of technology at hand, and orientation of components, would determine the minimum sizes of transmission lines in Section 1. In Chapter 5, the different types of technologies with their advantages and disadvantages will be discussed in more detail.

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In this section, only an example of how it could influence a switch design will be explained.

Typically, in this design, it would be preferable to have wire-bonding facilities. One would mount the diode cathodes on junctions T1 and T2, and bond to Lines 1 and 2. The capacitor, C, could be mounted on Line 4 and then bonded to Line 3. The area in Section 1 then just has to have enough space for the bonding wire and inductor, L.

If the polarity of the diodes had been reversed, the situation would be much different. The cathodes would then be placed on Lines 1 and 2, and therefore more area would be needed. The minimum lengths and widths of Lines 1 and 2 would then be limited by the size of the diode.

The return loss can be adjusted by varying the lengths and widths of junctions T1 and T2.

- **Improved isolation**

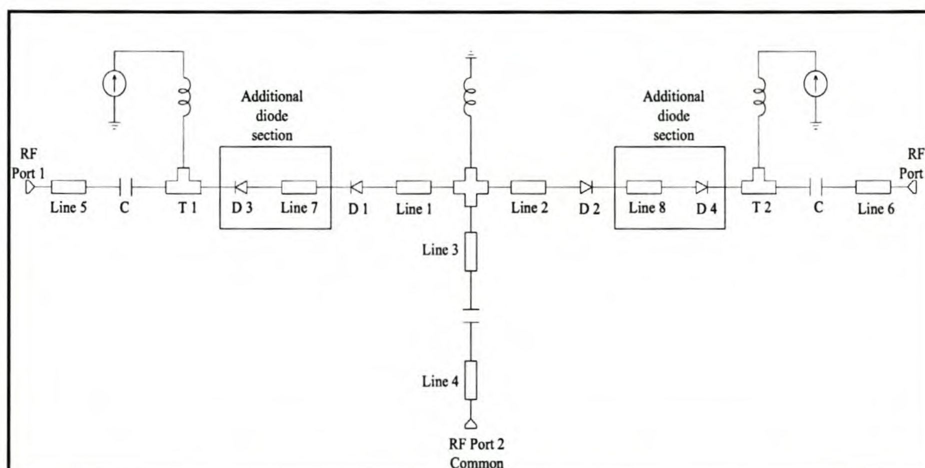

Figure 22: Series configuration SPDT switch with additional series diode

The isolation of the switch can be improved by adding additional diodes. There is an optimum spacing between the diodes, provided by Lines 7 and 8 in Figure 22, for which the isolation is a maximum. The optimum spacing is typically between 45 and 90 degrees at f_h. A 60 degree line would be a good starting point for a design.

- **Return loss**

The impedance of the Lines 7 and 8 is used to optimise the return loss, and should be lower than Z_0 at f_0. The width of junctions T1 and T2 also play a significant role in

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adjusting the return loss and must be used in conjunction with Lines 7 and 8 to optimise the return loss.

- **Designed switch**

A SPDT switch with an additional diode was designed by following the above-mentioned guidelines. The switch was not designed for a specific requirement. The idea was to apply the guidelines in order to verify them, and to optimise the switch for best response in terms of bandwidth, insertion loss and isolation. The switch operates in the band 500 MHz to 30 GHz. The switch illustrated in Figure 22 was used for the design. The substrate properties are shown in Table 1 on page 24 and the design parameters in Table 4.

Substrate	CER-10, 25 mil, $\varepsilon_r = 9.5$, $\tan\delta = 0.0035$
PIN diode	HPND-4005
Line1, Line 2, Line 3 (L × W)	0.3 x 0.2 mm
Line 4, Line 5, Line 6 (L × W)	5 x 0.65 mm
Width of T1 and T2	0.6 mm
Line 7, Line 8 (L × W)	0.6 x 0.8 mm (L = 60^0 @30 GHz; Z = 45 Ω @ 15GHz)

Table 4: Design parameters for SPDT switch shown in Figure 22

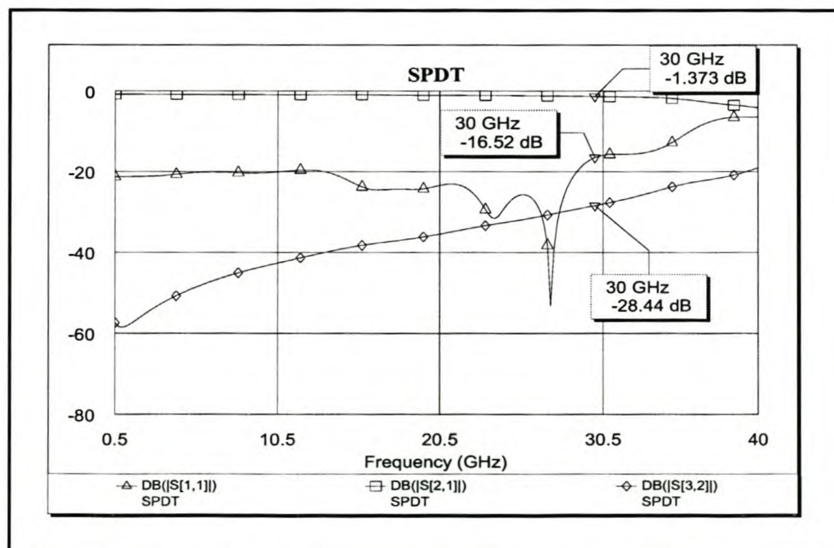

Figure 23: Simulated results for SPDT switch presented in Figure 22

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Figure 23 shows the simulated results of the SPDT switch. In the simulations, Port 1 was in the "on" state, and Port 3 was in the "off" state. From Figure 23 it can be seen that the switch is well matched across the required band, with the return loss better than 16.52 dB.

From equation 3.5, the expected isolation, at 30 GHz, for a switch with diodes having a junction capacitance of 0.017 pF each, is 22 dB. The simulated value is 28.44 dB. The increase in the simulated value of the isolation is due to the optimised spacing between the diodes.

The expected insertion loss, from equation 3.2, for a switch having diodes with a forward biased resistance of 4.7 Ω, is 0.78 dB. The simulated value is 1.373 dB. The transmission line losses, as well as the losses in the isolated arm of the switch contribute to the additional 0.593 dB.

From equation 3.5 the isolation for a SPDT switch with one, two and three diodes respectively at 30 GHz, would be 16.3, 22 and 25.47 dB. Figure 24 shows the simulated results for a switch with one, two and three diodes. The expected and simulated values differ very much. In the case of the switch with three diodes, the simulated value is almost double the expected value. This difference is due to the optimal spacing between the diodes.

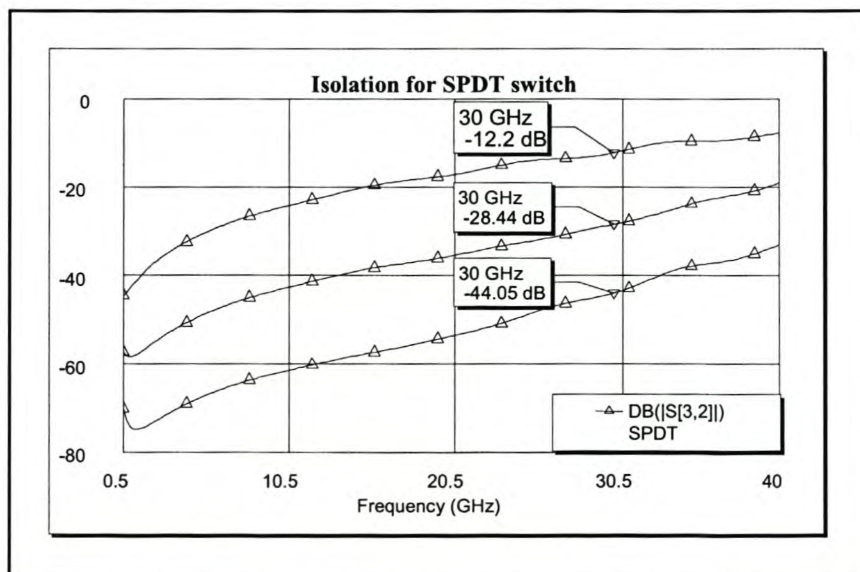

Figure 24: Simulated isolation for SPDT series configuration switch with one, two and three diodes

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3.2.2 Shunt configuration switch

The shunt configuration switch offers high isolation and is capable of handling more power than the series configuration switch. This is so because one of the diode electrodes can be "heat-sinked" to ground.

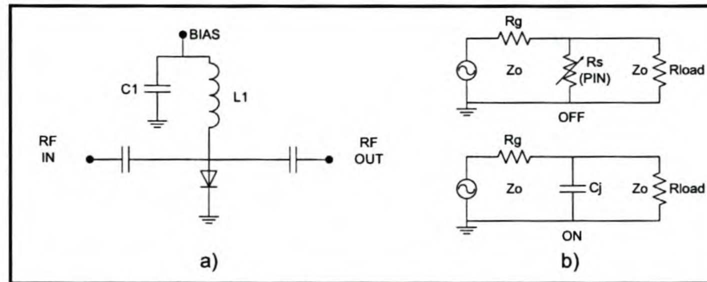

Figure 25: Shunt configuration SPST PIN diode switch

Figure 25 shows a schematic drawing and RF equivalent circuit of a typical shunt connected SPST PIN diode switch. As the name implies, the PIN diode is shunt connected with the transmission line.

The switch is turned "on" by reverse biasing the diode and turned "off" by forward biasing the diode. In the "on" state, the diode presents a short circuit to ground in the RF path, and as a result of this, all the incident energy is then reflected. In the "off" state, the diode presents a high impedance in parallel with the RF path and has a minimal affect on the RF power.

The biasing network is the same as in the case of the series configuration switch, and was discussed in section 3.2.1.

The SPST shunt configuration switch is capable of offering very high isolation over large bandwidths for a single diode.

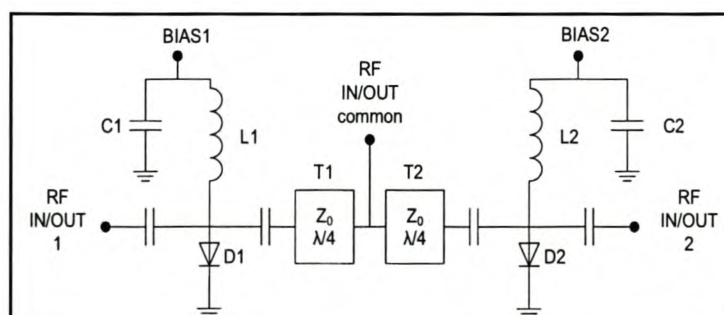

Figure 26: Shunt configuration SPDT PIN diode switch

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A schematic diagram for a SPDT shunt configuration PIN diode switch is shown in Figure 26. It can be seen that the SPDT switch is a combination of two SPST switches, joined together with λ/4 spacing at f_0 between the diodes and the common RF port. The λ/4 transmission line automatically places a restriction on the bandwidth of the switch.

At the midband frequency, f_0, where the transmission lines T1 and T2 are λ/4 in length, the SPDT switch operates as follows: When diode D1 is forward biased and diode D2 reverse biased, RF power will flow from the common port to port 2, and port 1 will be isolated. The λ/4 transmission line will transform the short circuit at D1 to a high impedance at the common junction, and thus eliminates any reactive loading that might exist from the isolated arm of the circuit at that point [5]. If the frequency is changed, the electrical length of the transmission lines also changes accordingly and this creates a mismatch at the common junction. Techniques to improve the bandwidth of the switch will be discussed in more detail later in section 3.2.2.7

In the shunt configuration, the isolation and power dissipation of the switch is primarily a function of the diode's forward bias resistance whereas the insertion loss is mainly dependant on the diode's capacitance.

3.2.2.1 Insertion Loss

The formula for calculating the insertion loss for a SPST shunt configuration switch is shown in equation 3.12. The derivation of the equation is shown in the appendices.

$$Insertion\,loss = 20\log_{10}\left[1+\frac{Z_0}{2Z}\right] \quad [dB] \qquad 3.12$$

where: Z = diode impedance

Z_0 = microstrip characteristic impedance

If an ideal PIN diode with a reverse bias impedance of $Z = 1/j2fC_j$ is used, then the insertion loss is [5]:

$$Insertion\,loss = 10\log_{10}\left[1+\left(\pi f C_j Z_0\right)^2\right] \quad [dB] \qquad 3.13$$

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where: C_j = reverse bias junction capacitance of the diode

f = frequency in Hz

The insertion loss is graphically presented in Figure 27 as a function of the junction capacitance. It gives an idea of the typical insertion loss that can be expected for an ideal diode.

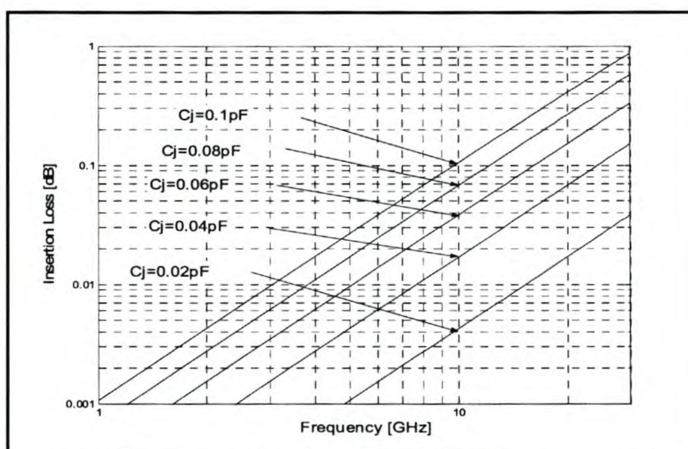

Figure 27: Insertion loss for a shunt configuration SPST switch in a 50Ω system

With a practical diode, the parasitic elements do influence the insertion loss and depending on the diode packaging, could play a more dominant role than the diode junction capacitance. In equation 3.13 it is assumed that the diode is perfect with no parasitic elements (see Figure 25 b). Figure 28 shows a circuit where a more realistic model of a practical diode is used as opposed to the model used in Figure 25 b.

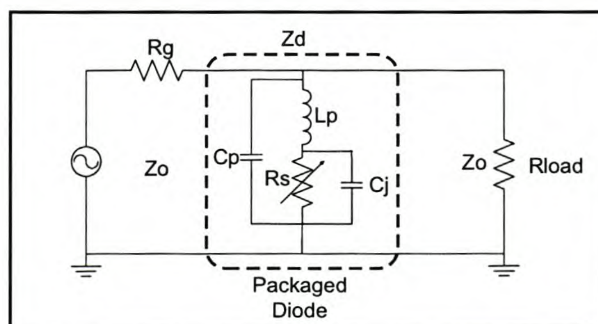

Figure 28: RF Equivalent circuit of a shunt configuration SPST PIN diode switch with practical diode model

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A practical diode contains several reactance elements. If $R_S^{'}$ and $X_S^{'}$ are the series equivalent resistance and reactance of the diode, then $Z_d = R_S^{'} + jX_s^{'}$. If Z in equation 3.12 is replaced with Z_d [3], then:

$$Insertion\,loss = 10\log\left[\frac{\left(\frac{R_s^{'}Z_0}{R_s^{'2}+X_s^{'2}}+2\right)^2+\left(\frac{X_s^{'}Z_0}{R_s^{'2}+X_s^{'2}}\right)^2}{4}\right] \quad [dB] \qquad 3.14$$

The insertion loss equations shown for the SPST switch are also valid for the SPDT switch. It is important to note that equations 3.13 and 3.14 only give the insertion loss of the diode itself. To calculate the total insertion loss, all other losses such as those in the biasing network and transmission lines must be accounted for.

3.2.2.2 Isolation

The isolation is primarily a function of the forward bias resistance of the diode. The formula for calculating the isolation for the SPST shunt configuration switch is shown in equation 3.15. The derivation is shown in the appendices.

$$Isolation = 20\log_{10}\left[1+\frac{Z_0}{2R_s}\right] \quad [dB] \qquad 3.15$$

where: R_s = diode series resistance

Figure 29 is a graphical presentation of equation 3.15 and shows the isolation as a function of the series forward biased resistance of the diode.

If the model of a practical forward biased diode is known and its impedance can be written in the form $Z_d = R_S^{'} + jX_s^{'}$, then equation 3.14 can also be used to find the isolation of a practical diode.

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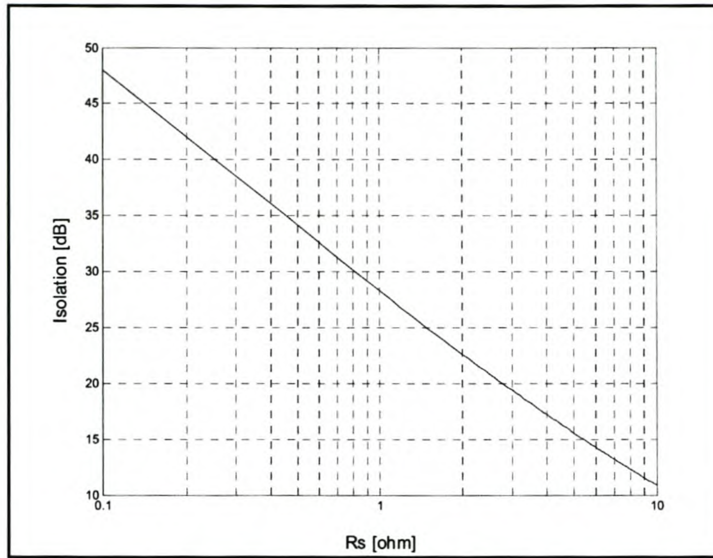

Figure 29: Isolation versus series resistance (R_S) for a shunt configuration SPST switch in a 50 Ω system

In a SPMT configuration, an additional isolation of 6 dB is obtained. The same argument discussed in section 3.2.1.2 on page 20 for the series connected SPDT switch, applies to the shunt connected SPMT configuration. Therefore the isolation for a SPMT switch is:

$$Isolation_{SPMT} = 20\log_{10}\left[1+\frac{Z_0}{2R_s}\right]+6 \qquad [dB] \qquad 3.16$$

The isolation of the SPDT switch is double that of the SPST switch (i.e. 3dB), plus the additional 6 dB due to the effect of the multi throw switch junction (as discussed in section 3.2.1.2 above) [5].

3.2.2.3 Power dissipation

The power dissipation in the diode in a shunt configuration switch is [2]:

$$P_D = \frac{4R_s Z_0}{(Z_0+2R_s)^2} \bullet P_{AV} \qquad [\mathrm{W}] \qquad 3.17$$

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For $Z_0 >> R_s$, equation 3.17 can be simplified to:

$$P_D \approx \frac{4R_s}{Z_0} \bullet P_{AV} \quad [\mathrm{W}] \qquad 3.18$$

where the maximum available power is given by:

$$P_{AV} = \frac{V_G^2}{4Z_0} \quad [\mathrm{W}] \qquad 3.19$$

Equations 3.17 and 3.19 are only valid for matched switches. If the switch is not matched, refer to the discussion in Section 3.2.1.3 on page 21.

3.2.2.4 Peak RF Current

The peak RF current that will flow through the diode in a SPST configuration is given as:

$$I_p = \sqrt{\frac{8P_{AV}}{Z_0}} \quad [\mathrm{A}] \qquad 3.20$$

In a SPMT configuration, the peak RF current is [2]:

$$I_p = \sqrt{\frac{2P_{AV}}{Z_0}} \left(\frac{2\sigma}{\sigma+1}\right) \quad [\mathrm{A}] \qquad 3.21$$

Equation 3.20 only applies for a matched the switch. If the switch is not matched, refer to Section 3.2.1.3.

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3.2.2.5 Peak RF voltage

The peak RF voltage that can exist across the diode in a shunt configuration switch is given in equation 3.10:

$$V_p = \sqrt{2P_{AV}Z_0} \qquad 3.22$$

Equation 3.22 is only valid of if the switch is matched. If the switch is not matched, refer to Section 3.2.1.3.

3.2.2.6 Manufacturing

On microstrip, the shunt configuration switch is more difficult to manufacture than the series configuration switch. The reason for this is that it is difficult to connect the diode to ground without adding parasitic inductance in series with the diode. At microwave frequencies, this extra inductance has a large influence on the switch properties. It mostly has an influence on the isolation of the switch.

3.2.2.7 General design information

The following section will provide information regarding the design of a shunt configuration switch. The design procedure to be discussed is more a "rule of thumb" procedure that gives guidelines on how to design the switch and how to improve the switch performance.

This design procedure was developed by doing various simulations to establish which elements influence the switch response, and in what way. As verification of the guidelines, simulation results will be shown. The simulations were done in the frequency band 500 MHz to 40 GHz.

The guidelines have the following limitations: On a substrate with a specified thickness, the rules only apply up to the frequency where the length of a $\lambda/4$ transmission line is twice the width of a 50 Ω line at that frequency. If the switch should operate at a higher frequency, a lower substrate thickness is required. The rules also only apply for diodes with C_j values smaller than 1 pF.

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In the schematic diagrams to follow, all the junctions are configured as rectangular transmission lines and are therefore referred to as "Lines". It is assumed that the diodes, capacitors and inductors are ideal and that the switch will be used in a 50 Ω system.

3.2.2.7.1 SPST switch

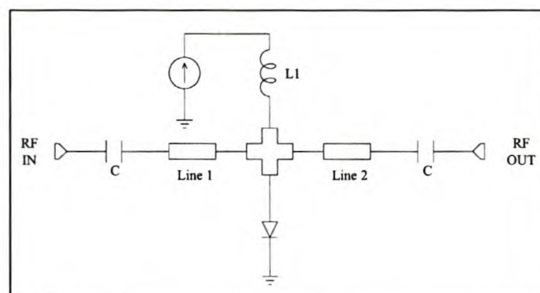

Figure 30: Schematic used for simulating a SPST shunt configuration switch

Figure 30 shows a schematic drawing of a shunt configuration switch that was used in Microwave Office to simulate the properties of the switch. The parameters of the substrate and diode used in the simulations, are shown in Table 1 and Table 2 on page 24.

- **General information**
  The SPST switch can operate across a very broad band with low insertion loss and high isolation properties. For best overall broadband performance, with maximum isolation and best matching across the band, the transmission lines, Line 1 and Line 2, should have a characteristic impedance of 50 Ω at the midband frequency, f_0. For minimum insertion loss, the transmission lines should be kept as short as possible.

- **Isolation**

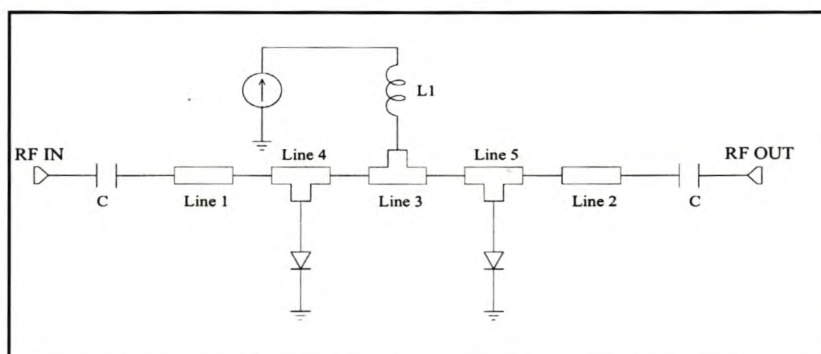

Figure 31: Schematic for simulating shunt configuration SPST switch with two diodes

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The isolation can be improved by adding additional shunt diodes with optimum spacing between them. Figure 31 shows a schematic drawing of a SPST switch with two shunt diodes. This optimum spacing, provided by Line3, is a quarter wavelength long of the highest operating frequency, f_h.

- **Return loss**

  To minimize the return loss at the RF ports, Line 1 and Line 2 should have a 50 Ω impedance at the midband frequency and Line 3 should have an impedance generally lower than 50 Ω at f_h. Because Line 1 and Line 2 have a 50 Ω impedance, their lengths are not that critical.

  Lines 4 and 5 are just long enough to mount the diode or bonding wire from the diode onto, and have the same width as Line 3. Line 3 therefore determines the distance between the two diodes.

- **Biasing network**

  The biasing network can be attached to the RF circuit at any point since it is designed to minimize the effect it has on the RF circuit. In Figure 31 it was attached at the indicated point to make the switch symmetrical.

- **Simulation results**

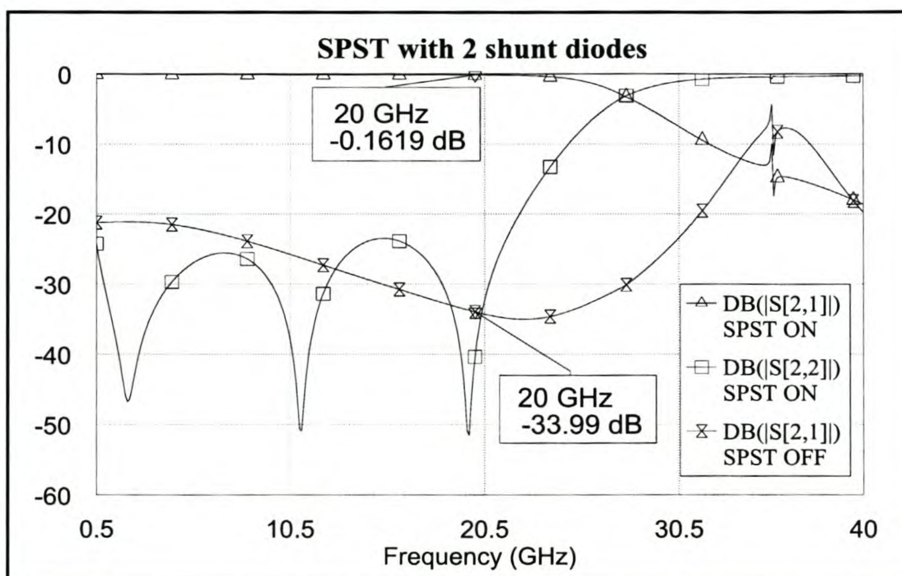

Figure 32: Simulation results of SPST switch with 2 shunt diodes, designed to operate from 500MHz to 20 GHz

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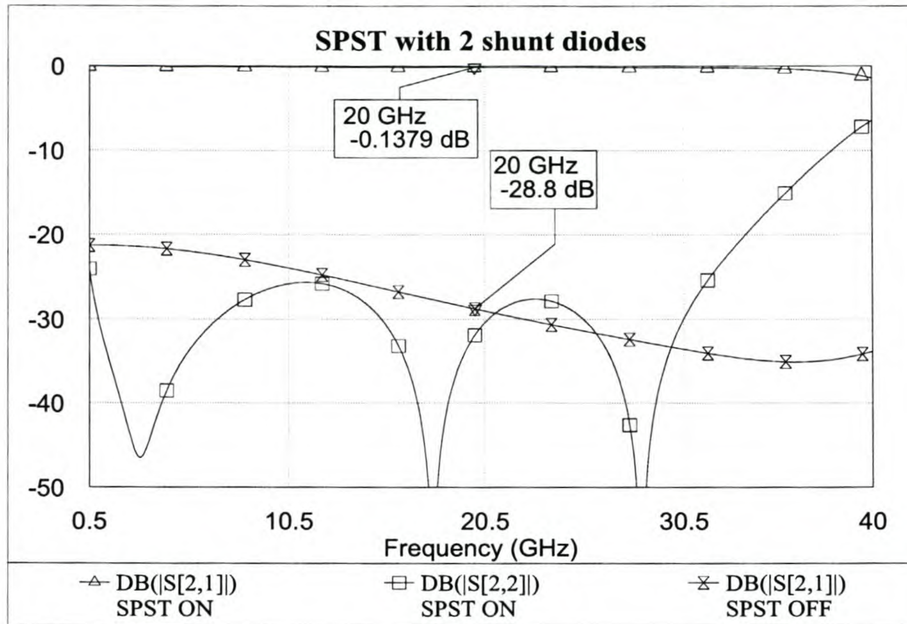

Figure 33: Simulation results of SPST switch with 2 shunt diodes, designed to operate from 500MHz to 30 GHz

Figure 32 and Figure 33 shows the simulation results of the switch presented in Figure 31. It was designed by using the above mentioned rules and operates from 500 MHz to 20 GHZ and 500 MHz to 30 GHz respectively. The 500 MHz to 20GHz design was done on 25 mil thick substrate and the 500 MHz to30 GHz design on a 15 mil thick substrate. The transmission line properties for the two designs are listed in Table 5.

As in the previous design, the switch was not designed for a specific requirement. It was designed to validate the design procedure and in the process, show what typical response can be achieved from the switch.

	500MHz – 20 GHz	500MHz – 30 GHz
Substrate thickness	25mil	15mil
Line 1 (L × W)	2.94 x 0.66 mm	1.95 x 0.39 mm
Line 2 (L × W)	2.94 x 0.66 mm	1.95 x 0.39 mm
Line 3 (L × W)	1.37 x 0.78 mm	0.92 x 0.45 mm
PIN diode	HPND-4005	HPND-4005

Table 5: Parameter values for the two SPST designs

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From the results shown above, it is clear that in both designs, the switches are well matched across the expected frequency bands with the return loss better than 20 dB.

From equation 3.15, the expected isolation for the switch should be 21.3 dB. The simulated results show than the isolation it better that the expected value. This is mainly because of the spacing between the diodes.

The losses in the transmission lines are the main contribution to the simulated insertion loss since the loss in the diodes are insignificantly small compared to those in the transmission lines.

3.2.2.7.2 SPDT switch

Figure 34 shows the schematic diagram used in MWO to simulate the switch properties of a shunt configuration SPDT switch. The switch is symmetrical around the common port, Port 2, so Line 1 is equal to Line 2 and Line 3 equal to Line 4.

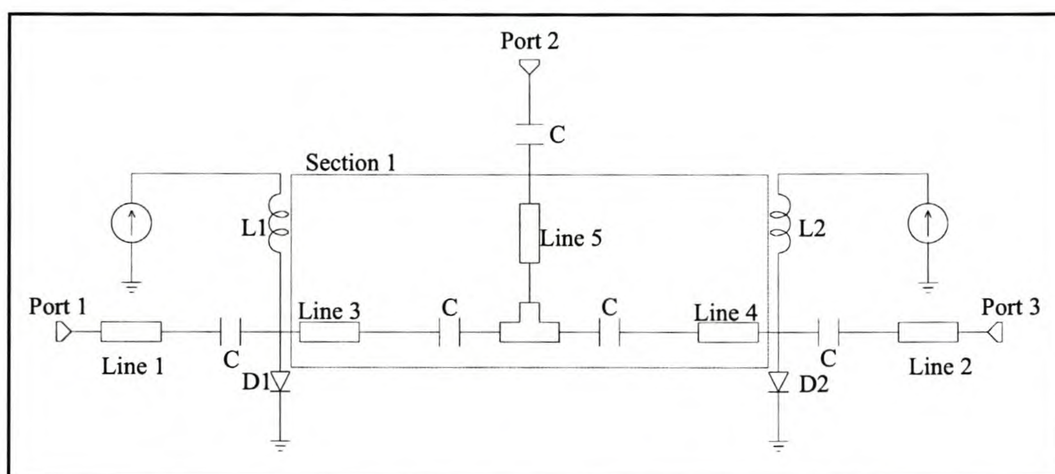

Figure 34: Shunt configuration SPDT switch

The SPDT switch has the limitation that it is not as broadband as the SPST switch. This limitation occurs because of the λ/4 spacing between the diode and the common junction (see Figure 26 on page 32). The design guidelines for the SPDT configuration are:

- **Section 1**
  The common junction area, marked "Section 1" in Figure 34, is the most critical part in the SPDT switch design. The bandwidth of the switch can be improved with a simple matching technique where the Lines 3, 4 and 5 identical in length and impedance. The

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lengths are set to λ/4 of the midband frequency, f_o, and the impedance chosen to a value, Z, below 50 Ω at f_0 [9]. The bandwidth is directly dependant on the value of Z, but has a certain maximum value that cannot be exceeded.

- **Improved isolation**

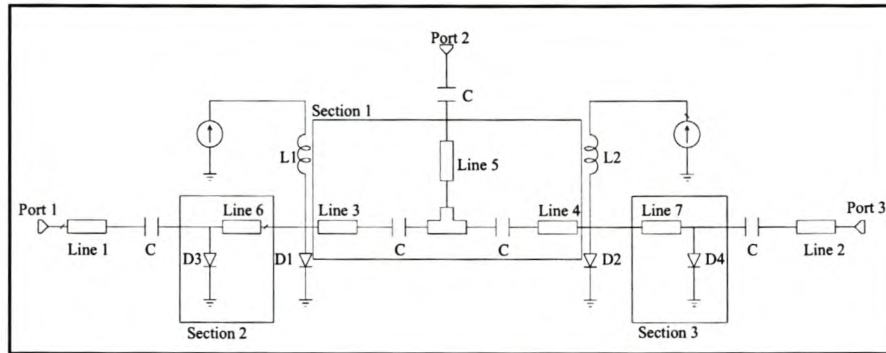

Figure 35: Shunt configuration SPDT switch with additional shunt diodes

To improve the isolation of the SPDT switch, additional shunt diodes can be added. Figure 35 shows a schematic drawing where the additional diodes have been added in Sections 3 and 4. The optimal spacing between the diodes, provided by Lines 6 and 7, is a quarter of a wavelength at f_0 long.

- **Return loss**

The impedance of the line 6 and Line 7 must be set equal to Z_0. If the above mentioned matching technique is applied, the bandwidth is not constrained by the additional diodes. These additional sections however increase the insertion loss of the switch. A trade off has to be made between the isolation, insertion loss and return loss of the switch.

- **Simulation results**

The simulated results of the switches presented in Figure 34 and Figure 35, are shown in Figure 36 and Figure 37 respectively. In the simulations, Port 3 is in the "off" state, and Port 1 in the "on" state.

The transmission line properties for the switches are listed in Table 6.

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Substrate thickness	25 mil
PIN diode	HPND-4005
Line 1, Line 2 (L × W)	10 x 0.66 mm
Line 3, Line 4, Line 5 (L × W)	2.86 x 1.5 mm
Line 6, Line 7 (L × W)	2.86 x 0.66 mm

Table 6: Parameter values for SPSD design

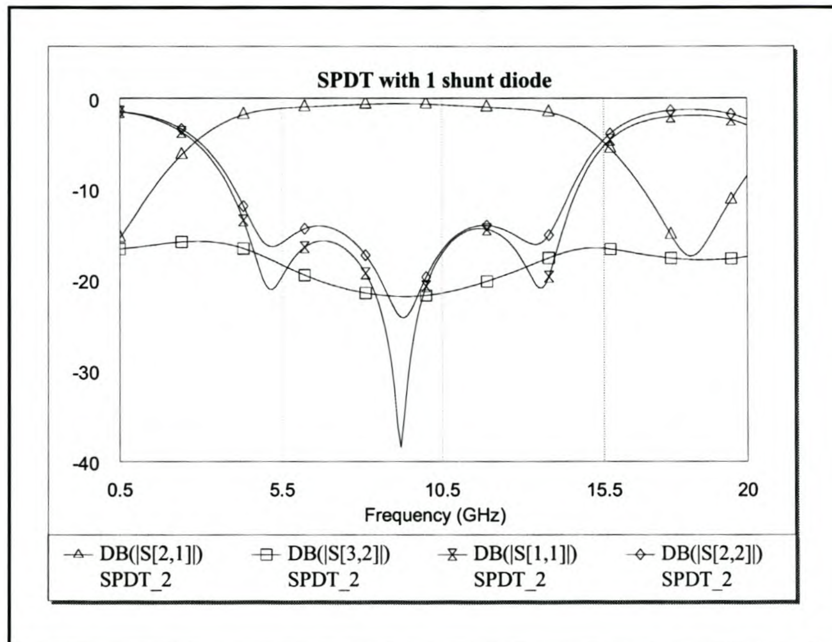

Figure 36: Simulated results for SPDT switch presented in Figure 34

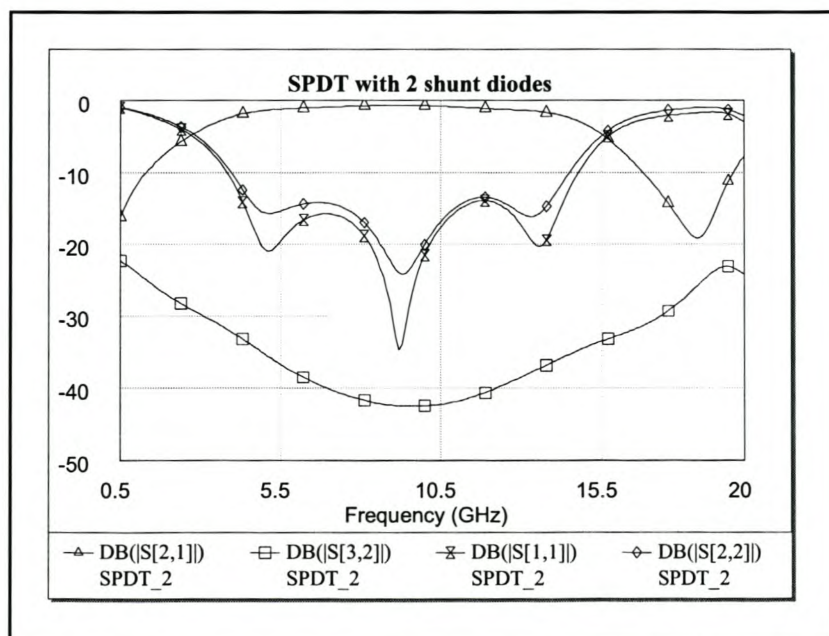

Figure 37: Simulated results for SPDT switch presented in Figure 35

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From the simulation results, it can be seen that the addition of Sections 2 and 3 have no significant influence on the bandwidth of the switch. Compared to the SPST switch, the SPDT switch is definitely not as broadband.

The isolation improved tremendously with the additional diode added, but not across the complete band.

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4 Device characterisation

This chapter will first discuss why there is a need for the device characterisation and then show possible ways on how to accomplish it.

The Thru-Reflect-Line (TRL) calibration and measurement test fixture was chosen as the preferred option for device characterisation. The design of the test fixture will be discussed in more detail.

The measurements made on the fixture, and parameter extraction results performed on two PIN diodes will be presented.

4.1 Motive for device characterisation

In the previous chapters, it was assumed that the components used in designs, are ideal. The designs were done with linear models and parameter values specified by the component manufacturers. Practical components are not ideal, and this factor has to be taken into account in order to do a proper design. The component information available from the manufacturers is usually very limited and not sufficient to build a complex or more detailed model. The conditions under which the device parameters are specified may also differ from the conditions under which it will operate in, in the design. Consequently, there is a need for a better device model for a proper design.

The need is to characterise and extract an exact model of the component under the specified conditions it is intended to operate under. These conditions would typically be

- The substrate it will be used on
- Biasing conditions
- Frequency range

With the simulation software packages available today it is possible to simulate transmission line circuits very accurately. When a design is done with these software packages, the only limitation is usually the lack of an accurate model of the components being used. If better component models could be used in the simulation packages, simulation results could be more accurate. This would reduce the number of design iterations until a final product is reached. It would save time and cost involved in the development of the product.

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4.2 Parameter extraction methods

Normally when measuring the properties of a device with a network analyser, it is mounted in a test fixture. When taking the measurement, the effects of the fixture are also included in the measurement and therefore it is not very accurate. To have an accurate measurement of the device properties, the effects of the fixture must be removed. The three fundamental techniques used to remove the errors introduced by fixtures are modelling, de-embedding and direct measurement [10]. The relative performance of the fixture compared to the accuracy specifications of the device being measured, will determine which extraction method should be used.

4.2.1 Modelling

The modelling extraction method uses mathematical corrections, derived from an accurate model of the fixture, to remove the influence of the fixture on the measurement. The modelling method requires some known data regarding the fixture characteristics. The fixture itself would typically be measured in the process of finding an accurate model of it [10].

The simplest way in which modelling is done is with the port extension feature of the network analyser. To use this feature, a full two-port calibration must be done up to the indicated points in Figure 38. This calibration sets the calibration reference plane at the junctions of the test cables. The fixture is then connected and this reference plane is mathematically shifted to the DUT by using the port extension feature on the network analyser [10].

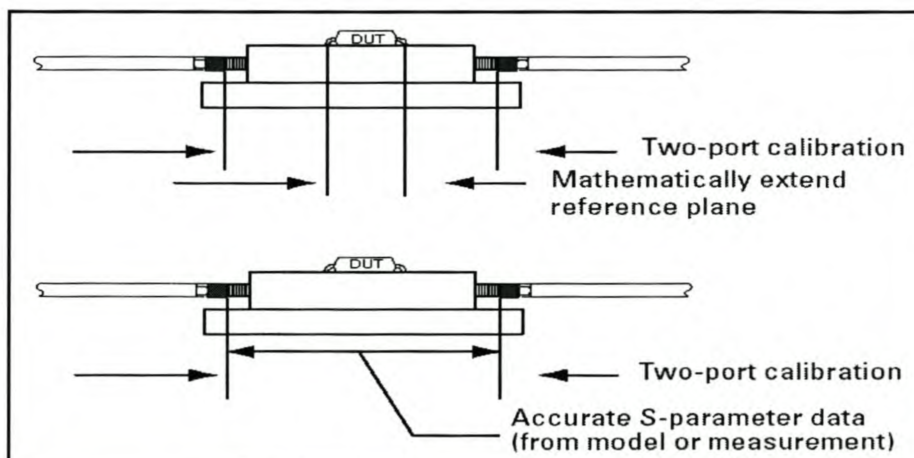

Figure 38: Modelling parameter extraction method [10]

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The port extensions function of the network analyser assumes the fixture is lossless and has a linear phase and constant impedance. These conditions are not always true in a practical situation. If the fixture performance is significantly better than that of the DUT, this method would be adequate [10].

4.2.2 De-embedding

The de-embedding method requires a very accurate linear model, or S parameter data of the fixture used to measure the DUT. The network analyser is calibrated with coaxial standards up to the indicated points in Figure 39. In order to find a model of the DUT, external software, like *MATLAB* for instance, is then used to combine the error data from the calibration with the modelled or measured error data of the fixture. The accuracy of this method therefore depends only on how well the actual performance of the fixture matches the modelled performance [10].

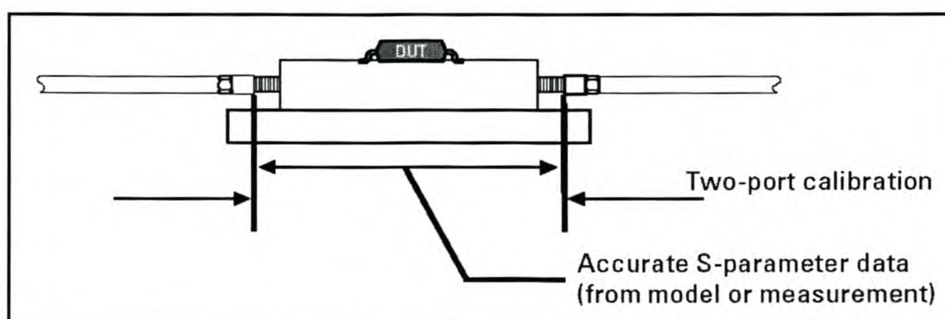

Figure 39: De-embedded model used [10]

The disadvantage of this method is the fact that external software is needed and that it is not always easy to find an accurate model of the fixture.

4.2.3 In-fixture calibration

The in-fixture calibration method usually involves measuring physical in-fixture calibration standards and then calculating the error terms. This method is based on how precisely the properties of the calibration standards are known. The number of error terms that can be corrected depends on the type of calibration done. Normalisation for instance can only remove one error term where as a full two port calibration can correct twelve error terms.

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The in-fixture calibration method has the advantage that the exact fixture properties need not be known because they are measured during the calibration procedure.

The two-port calibration provides very accurate measurements. Two commonly used types of two-port calibration are: Short-Open-Load-Thru (SOLT) and Thru-Reflect-Line (TRL). These are named after the types of standards used in the calibration.

A calibration at the coaxial ports of the network analyser removes all the effects of the network analyser and cables up to the connecters of the fixture. The effects of the fixture however are not accounted for. Ideally, an in-fixture calibration would be preferable, but high-quality SOLT in-fixture standards are not available to allow for a conventional two-port calibration of the system at the desired reference plain of the DUT. In microstrip, a short circuit is inductive, an open circuit radiates energy and a purely resistive broadband load is difficult to produce [10].

The Thru-Reflect-Line (TRL) calibration is an alternative to the SOLT two-port calibration method. The TRL calibration standards are more easily fabricated and their characterisation is less stringent than the SOLT standards. With TRL calibration the effects of the fixture is also accounted for during the calibration process. The reference (or measurement) plane of the calibration is set at the DUT itself and is therefore the most accurate calibration technique. The TRL calibration technique will be discussed in more detail in section 4.3.

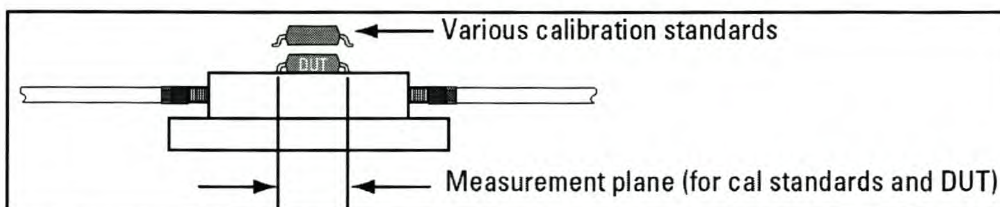

Figure 40: In-fixture calibration [10]

4.3 TRL Calibration

As mentioned previously, high quality broadband SOLT standards for in-fixture calibration at microwave frequencies are not readily available. With the TRL calibration however, it is possible to calibrate very accurately at microwave frequencies. The TRL calibration method was therefore chosen as the best option for device characterisation at microwave frequencies.

Notice that the letters TRL, LRL, LRM and TRM are often interchanged, depending on which calibration standards are used. The LRL for instance indicates that two **L**ine standards and a

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Reflect standard are used whereas the TRM shows that a **T**hru, **R**eflect and **M**atch standard are used. All these terms still refer to the same basic calibration procedure.

TRL calibration relies on the characteristic impedance of simple transmission lines rather than on a set of discrete impedance standards. Transmission lines are easy to fabricate and their impedances can be determined from their physical dimensions and the substrate properties [10].

In Chapter 5 a switch will be designed to operate from 2 to 18 GHz. For a proper design, the components have to be characterised across that band. A TRL calibration kit can be bought, but is very expensive. It was decided to design and build a complete TRL jig in-house. The design of the kit will be discussed in section 4.3.1 below.

4.3.1 TRL test fixture design

There are two types of calibration test fixtures, namely those used for R&D work and those used for manufacturing purposes. TRL calibration jigs intended for manufacturing use, look different from those used for R&D work, mainly because their design goals are different. A fixture designed for R&D work is usually very simple and not very rugged because only a few devices will be measured. It can be PC board based with each standard having its own connectors. Figure 41 shows a photograph of a typical calibration kit used for R&D purposes.

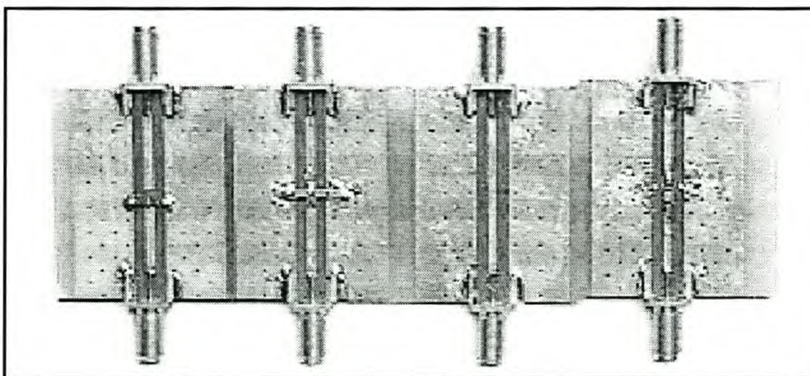

Figure 41: R&D type TRL calibration kit [10]

With a test fixture used for manufacturing or large quantity volumes, throughput is the main concern. A fixture that allows quick insertion, alignment and clamping of standards is needed. It must also be rugged since many components will be inserted and measured in the duration of

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its lifetime. Fixtures designed for manufacturing use tend to be mechanically more sophisticated [10].

It was decided to design and build a test fixture that is similar to one used for manufacturing purposes. The main frame and the design concept were done by the University of Stellenbosch. This report will show how the fixture operates and will then focus on the design of the calibration standards and discuss general problems that were experienced mechanically with the fixture. Figure 42 and Figure 43 shows a photograph and AutoCAD drawing of the test fixture that was designed.

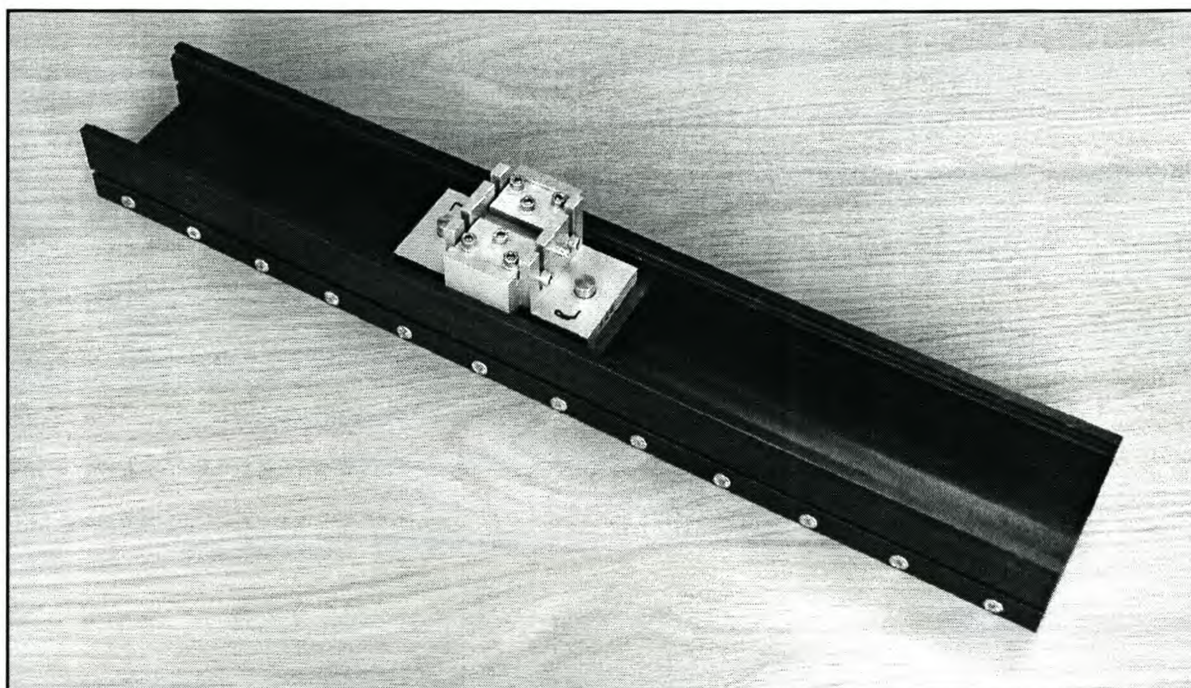

Figure 42: Photograph of designed TRL calibration kit

The test fixture operates as follows: The DUT is put on the main frame. It can slide horizontally in the main frame as seen from the top and side view in Figure 43. The connectors slide into the correct position from above and are then tightened by two screws from the side. To make alignment of the connectors with the DUT easy, the connectors can move horizontally and vertically as seen from the top view and vertically as seen from the side view in Figure 43. Experience has shown that a very good and repeatable connection can be made between the connector and the DUT by only applying vertical pressure. The pressure is applied by hand.

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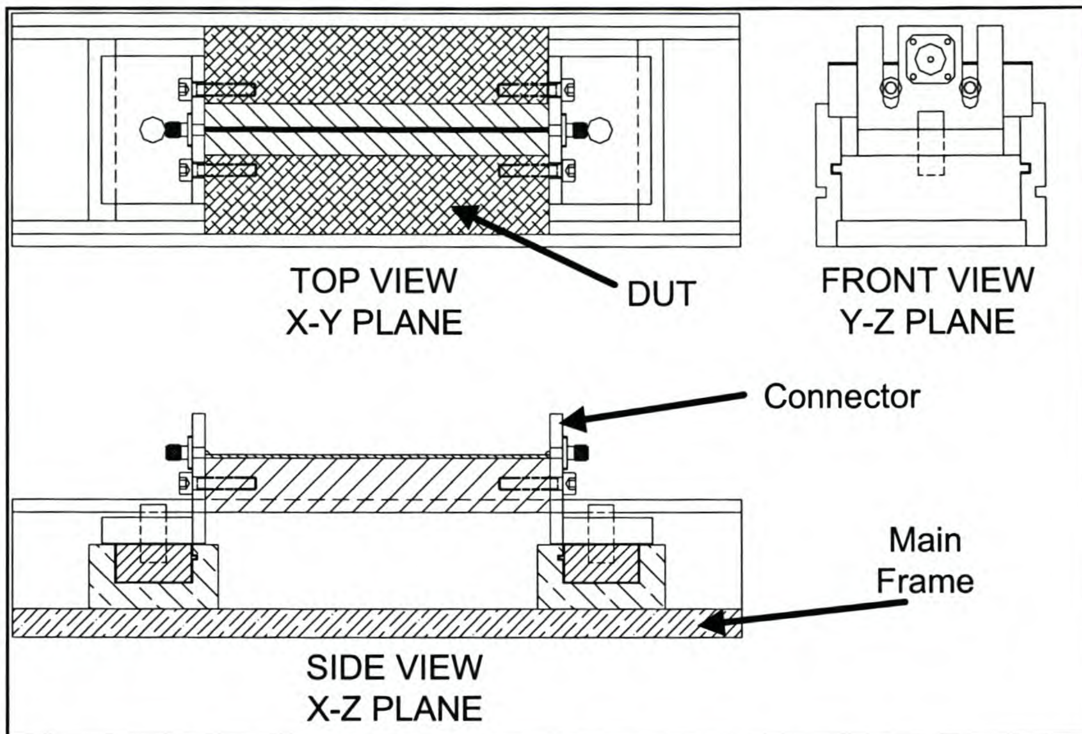

Figure 43: AutoCAD drawing of designed TRL calibration kit

4.3.1.1 Calibration standards

When building a set of TRL calibration standards for a microstrip or any other fixture environment, the specified requirements for each of these standards must be satisfied. The standards and their requirements will be discussed in sections 4.3.1.1.1 to 4.3.1.1.3 below.

A problem that could arise is higher order modes that can be generated at the connection between the connectors and the DUT. To partially solve the problem, launchers are employed. The launchers refer to the microstrip between the connectors and the calibration reference plane. The launchers are integrated into the DUT and calibration standards and are not added as additional inserts, or as part of the connectors. The idea with the launchers is that the higher order modes are attenuated along the microstrip. It should therefore be long enough so that the modes are completely attenuated at the calibration plane. Another possible solution to higher order modes that can be used in conjunction with the launchers, is to put the DUT and calibration standards in a "waveguide environment", where the waveguide is in cuttoff to the higher order modes. The waveguide environment is created by putting the microstrip in a channel with the width and height of the channel the same as that of the required waveguide to suppress the higher order modes.

Two sets of calibration standards will be designed, one on a soft substrate and the other on a hard substrate. The standards on the soft substrate will be designed to calibrate from 500 MHz

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to 18 GHz and the ones on the hard substrate from 2 to 18 GHz. The substrate properties are listed in Table 7. Microstrip lines will be used for the standards.

	Soft substrate	**Hard substrate**
Designation	CER-10 (Taconic)	Alumina
Dielectric constant (εr)	9.5	9.9
Substrate thickness (h)	25 mil	15 mil
Copper thickness (t)	18 um	2.54 um
Dissipation factor	0.0035	0.0004

Table 7: TRL substrate properties

4.3.1.1.1 Thru standard

With the thru standard, there is a choice of either a zero or a non-zero length standard. With a zero length standard, the impedance of the standard need not be known, but it must be lossless. The requirements for the thru is:

$$S_{21} = S_{12} = 1\angle 0^0$$
$$S_{11} = S_{22} = 0$$

If a non-zero length thru standard is used, the characteristic impedance must be the same as that of the line standard, Z_0.

The thru standard can be used to set the calibration reference plane during the calibration procedure. If it is used to set the reference plane, the electrical length and insertion phase must be well known. If a non-zero thru is used and specified to have a zero delay, the calibration reference plane will be in the middle of the line [10].

It was decided to use a zero-length thru standard for both the calibration kits. The thru standard was also used to set the calibration reference plane since it is better defined than the reflect standard.

Soft substrate design

The launchers were chosen to be 20 mm long, with the same width as that of the line standards. A length of 20 mm would be sufficient to ensure that no higher order modes exist at the

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calibration plane. The width of the line standard is calculated in section 4.3.1.1.3. The total length of the thru standard is therefore 40 (20 +20) mm. The width of the launchers is 0.66782 mm.

Figure 44 shows the AutoCAD drawing of the top view of the thru standard with its dimensions. The substrate is mounted on an aluminium base to fit onto the main frame.

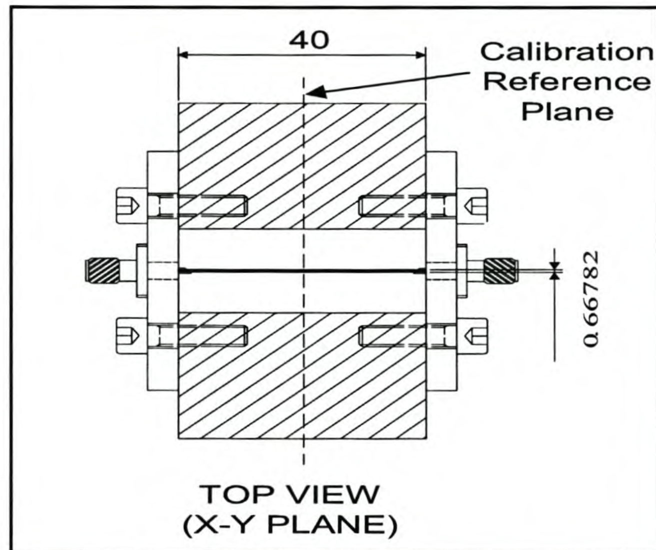

Figure 44: AutoCAD drawing of thru standard

Hard substrate design

Due to the sizes in which the substrates were available, the launchers needed to be shortened to 10 mm. The 10 mm launchers should be adequate to suppress higher order modes at the calibration plane. The length of the thru standard is 20 mm and the width 0.38183 mm.

4.3.1.1.2 Reflect standard

The reflection coefficient (Γ) magnitude should ideally be equal to 1, but need not be known. The phase of Γ must be known and specified to within ¼ of a wavelength. Γ must be identical on both the calibration ports. If the reflect option is used to set the calibration reference plane, the phase response must be well known and specified [10].

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Soft substrate design

Figure 45 shows the AutoCAD drawing of the designed reflect standard. The launchers are 20 mm long and 0.66782 mm wide. The gap of 16.916 mm was chosen for convenience sake of the manufacturing process of the bases, since one of the line standards are the same length. The 16.916 mm gap should be adequate for an open with no coupling between the launchers.

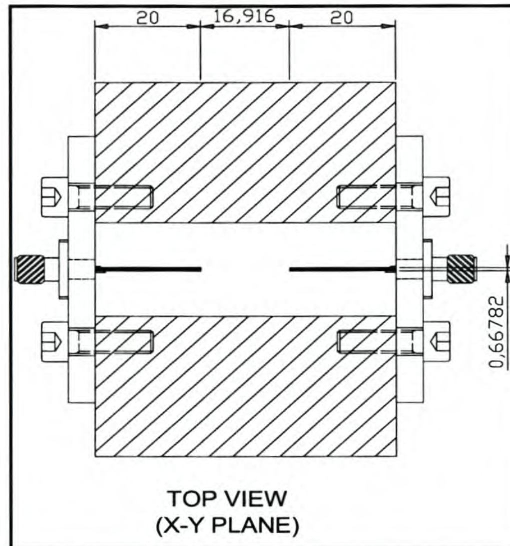

Figure 45: AutoCAD drawing of reflect standard

Hard substrate design

On the hard substrate, the launcher lengths are 10 mm with an opening of 4.9 mm. As in the case of the soft substrate, for manufacturing purposes, the opening length was chosen to be the same as that of one of the line standards. The width of the transmission lines are 0.38183 mm.

4.3.1.1.3 Line standard

The characteristic impedance of the line standard, Z_0, establishes the reference impedance of the measurement (i.e. $S_{11} = S_{22} = 0$). The calibration reference impedance is defined to be the same as the impedance of the line. The alternative to using the impedance of the line standard is to use the system impedance, which is equal to 50 Ω. This will result in an error if the transmission line standards do not have a perfect 50 Ω impedance over the complete calibration band. On microstrip, this error will be unavoidable as the lines are dispersive and the line impedance is frequency dependant.

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The insertion phase must be known and specified within $\pm 90^0$. It must not be the same as the thru standard. The difference between the line and the thru standards must be between (20^0 and 160^0) $\pm n \times 180^0$. The measurement uncertainty increases as the insertion phase nears 0^0 or any integer value of 180^0.

The optimal length is 90^0 ($\lambda/4$) of insertion phase relative to the thru standard. The useable bandwidth for a single line and thru pair is 8:1. Multiple lines can be used to increase the bandwidth of the calibration. If multiple lines are used, both the lines have to meet the insertion phase requirements and need to be the same width.

Soft substrate design

To cover the 500 MHz to18 GHz frequency band, two line standards are required. Equation 4.1 gives the optimal "split frequency" for the band if two line standards is required.

$$f_s = \sqrt{f_{start} \cdot f_{stop}} \quad 4.1$$

The split frequency for the 0.5-18 GHz band is:

$$f_s = 3 \quad GHz \quad 4.2$$

The first line standard, Line 1, will be used to calibrate from 500 MHz to 3 GHz and the second, Line 2, from 3 GHz to 18 GHz.

Both lines will have the same impedance of 50 Ω calculated at 9.25 GHz, the midband frequency of the total calibration bandwidth. The line widths for both line standards are 0.66782 mm.

The midband frequency for Line 1 is:

$$\begin{aligned} f_m &= \frac{0.5+3}{2} \\ &= 1.75 \quad GHz \end{aligned} \quad 4.3$$

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For optimum calibration bandwidth for a line standard, the length of the standard must be a quarter wavelength of f_m. The optimum length for Line 1, L_1, on the specified substrate is:

$$L_1 = 16.916 \text{ mm}$$

The Microwave Office package was used to check whether the phase is within the specified limits.

Phase check for Line 1:

At 500 MHz : $\phi = 25.675^0 > 20^0$

At 3 GHz : $\phi = 155.55^0 < 160^0$

The phase for Line 1 is within the specified limits.

Figure 46 shows an AutoCAD drawing of the Line 1 standard. It also indicates where the calibration planes are.

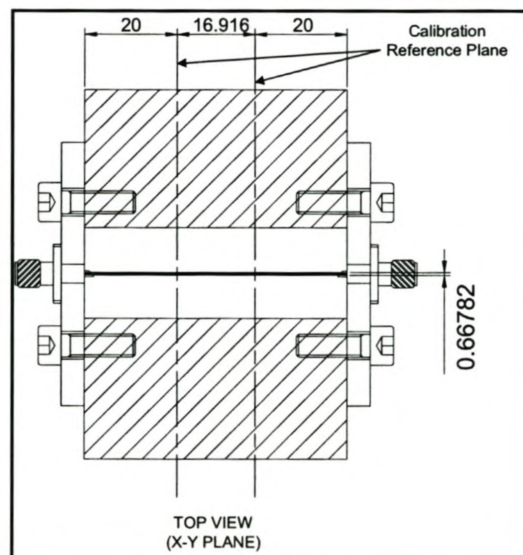

Figure 46: AutoCAD drawing of a line standard

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The midband frequency for Line 2 is:

$$f_m = 10.5 \quad GHz \tag{4.4}$$

The optimum line length for Line 2 is:

$$L_2 = 2.7183 \text{ mm}$$

Phase check for Line 2:

At 3 GHz : $\phi = 25^0 > 20^0$

At 18 GHz : $\phi = 158.21^0 < 160^0$

The phase for Line 2 is also within the required limitations.

Hard substrate design

Because the same equations are used for the soft and hard substrate design, they will not be repeated in this section.

Two line standards are required to cover the 2 to18GHz frequency band. The optimal "split frequency" for the two line standards is:

$$f_s = 6 \quad GHz$$

The first line standard, Line 1, is used to calibrate from 2 to 6 GHz and the second, Line 2, from 6 to 18 GHz.

Both lines will have an impedance of 50 Ω calculated at 9 GHz. The line widths for both line standards are 0.38183 mm.

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With the midband frequency for Line 1 being 4 GHz, for optimum calibration bandwidth, the line length should be 7.22 mm. The maximum length of the available substrates is 25 mm. With 10 mm launchers, a line of 7.22 mm is long. It was decided to use a 4.9 mm line instead. Therefore:

$$L_1 = 4.9 \text{ mm}$$

Phase check for Line 1:

At 2 GHz : $\phi = 30.44^0 > 20^0$

At 6 GHz : $\phi = 92.16^0 < 160^0$

Even though the optimal line length have not been chosen, the phase is still within the allowable limits.

The midband frequency for Line 2 is 12 GHz. The optimal line length for Line 2 is therefore:

$$L_2 = 2.3593 \approx 2.3 \text{ mm}$$

Phase check for Line 2:

At 6 GHz : $\phi = 43.26^0 > 20^0$

At 18 GHz : $\phi = 133.26^0 < 160^0$

The phase of Line 2 is within the required limitations.

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4.4 Measurements

This section will show the measurements done on the two TRL kits in order to evaluate their accuracy and performance. It will show what sort of results could be expected from measurements made on the kits.

To evaluate the kits, two calibration standards will be measured after a full two-port TRL calibration has been done on both kits respectively. S_{11} and S_{21} are typical measurements done on the calibration standards to evaluate the quality of calibration done. These measurements will be presented and discussed in the subsequent sections.

Possible ways on how to improve the performance or calibration quality of the kits will be discussed in section 4.5

4.4.1 Soft substrate

The return loss, S_{11}, is a measure of the repeatability of the connections made. The lower the value (in dB), the better the repeatability. Ideally, one would want every connection to be made identical to the previous one. This is however not the case, but one strives to meet that goal. As mentioned before, experience has shown that connections made by hand are very repeatable whereas soldered connections are surprisingly not.

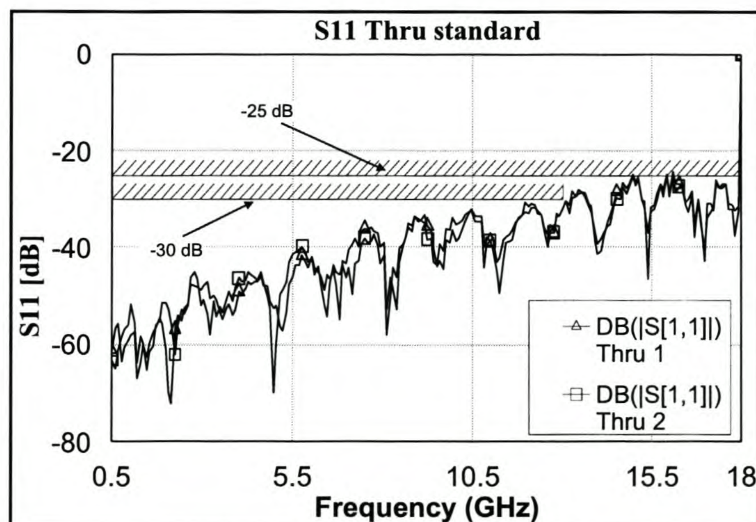

Figure 47: S_{11} of the thru standard on soft substrate

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Figure 47 shows two measured S_{11} parameters on the thru standard after calibration. The connections between the connectors and the standard have been connected, broken and reconnected between the displayed data. From Figure 47 it can be seen that both traces look very similar. This firstly indicates that from an RF point of view, the connections look very similar. Secondly, it shows that the connections are very repeatable. A return loss of -30 dB was expected for the calibration. This goal had been achieved from 500 MHz to 13 GHz. The measured S_{11} parameter is however better than -25 dB across the whole calibration band. It shows that the connections are in fact very repeatable, and very good.

Figure 48 shows the phase of the measured S_{21} parameter of the thru standard. It was expected to have a phase variation of 2^0 across the band. Again, this goal had been achieved up to 13 GHz. The phase variation across the band is 4^0. This is not as good as expected, but is still a good phase measurement. The phase response observed above 15 GHz is suspected to be due to the presence of higher order modes.

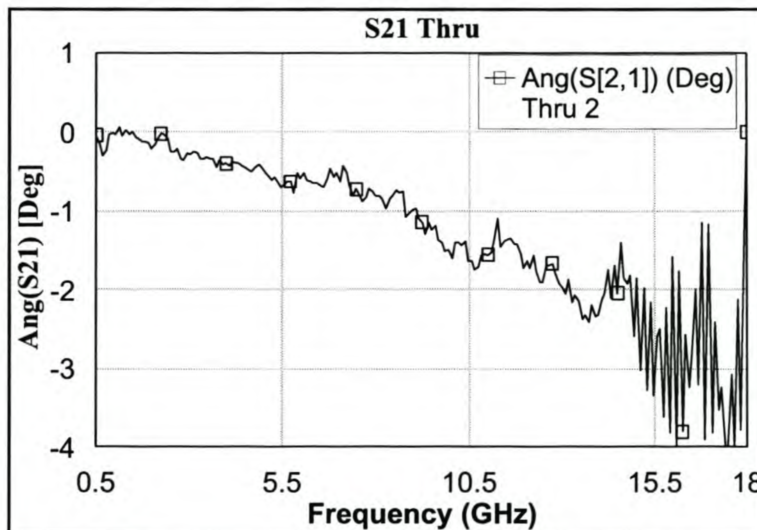

Figure 48: Measured phase of S_{21} parameter for thru standard on soft substrate

In the shown results, the microstrip transmission lines were put in a channel. The channel can be seen in the photograph shown in Figure 49. The idea with the channel is to simulate a rectangular waveguide with the "top" end removed. The waveguide dimensions are chosen as such that it would suppress unwanted higher order modes. The channel was chosen to be 10 mm wide and 7.3 mm high. The channel almost has the same dimensions as that of a rectangular waveguide with a cuttoff frequency of about 21 GHz [11]. This would imply that no higher order modes below 20 GHz could propagate in the channel/waveguide. Experiments have been done with and without the "top" as well as with different wall heights. Care has

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been taken so that the line impedances were not influenced with the addition of the top end and with the channel size adjustments done. No significant difference was noted. The phase response above 15 GHz was unaffected by these experiments.

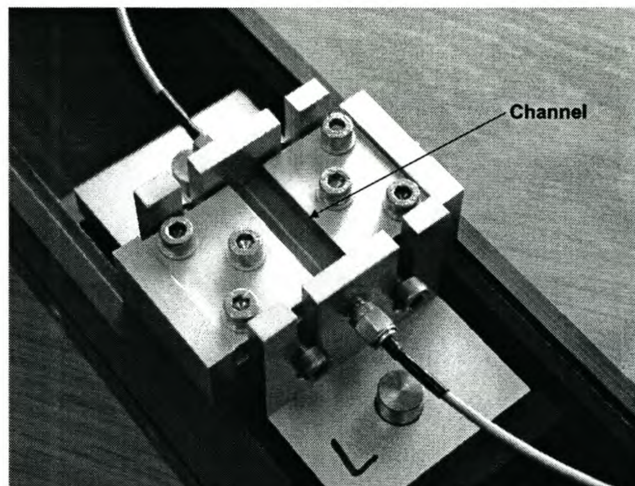

Figure 49: Photograph of thru standard on soft substrate

A connector with a pin diameter and length of 1.2 mm and 3 mm respectively was used for the shown results. Section 4.5 will give more insight into the specific connector types for the various substrates.

4.4.2 Hard substrate

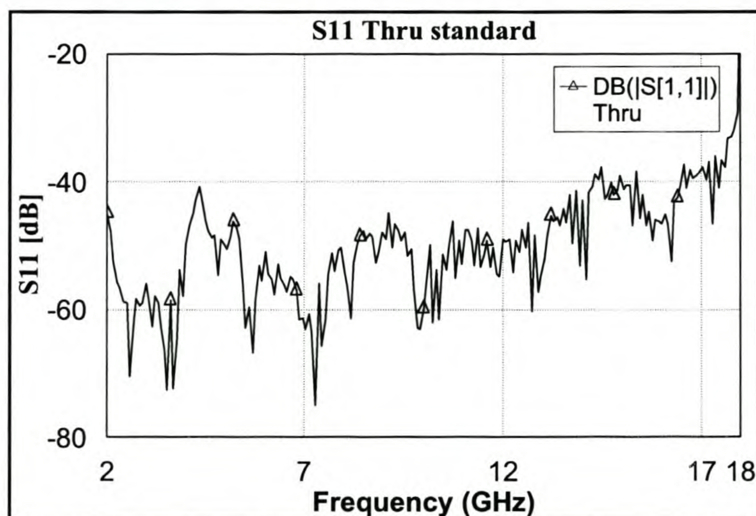

Figure 50: S_{11} of the thru standard on hard substrate

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Figure 50 shows the measured S_{11} parameter of the thru standard after calibration. The results look much better than those measured on the soft substrate do. S_{11} is generally lower than -40 dB across almost the complete frequency band. These results are better than the expected -30 dB. It shows that the connections are in fact very repeatable.

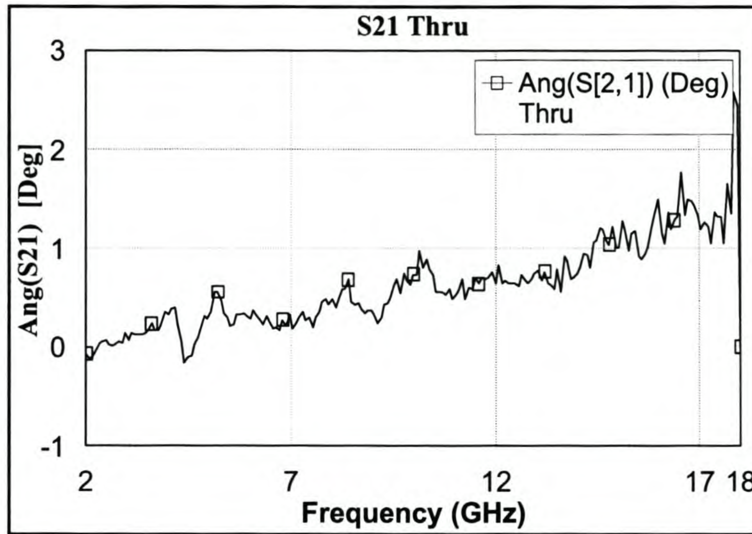

Figure 51: Measured phase of S_{21} parameter of thru standard on hard substrate

Figure 51 shows the measured phase of the S_{21} parameter of the thru standard. Again, the results look better than in the case of the soft substrate. The phase variation is better than the expected 2^0.

In contrary to the soft substrate experiments, the hard substrate microstrip transmission lines were mounted on the aluminium base with no channel environment. Figure 52 shows a photograph of a calibration standard on hard substrate. From the results shown, it can be seen that no high order modes are present. Experiments have also been performed with the transmission line in a channel, with and without a top. No difference was noted in the measurements.

A connector with a pin diameter and length of 0.48 mm and 0.9 mm respectively was used for the shown results.

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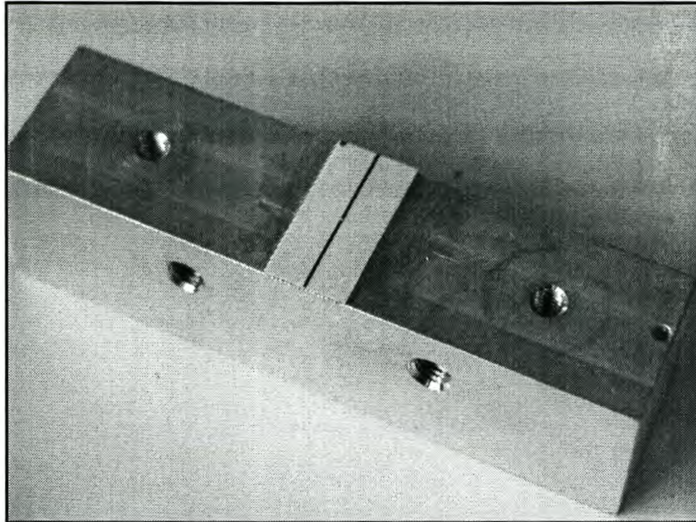

Figure 52: Photograph of thru standard on hard substrate

4.5 General problems and recommendations with TRL kits

Mechanically the kit had no problems and performed very well. In general, the connectors were both the problem, as well as the solution to most of the problems that were experienced with the test fixture. It was decided to use SMA type connectors since they operate from DC to 18 GHz and device characterisation was only needed up to 18 GHz.

Experiments have been performed with two different sets of connectors on both substrates. The first connector had a pin diameter of 1.2 mm and length of 3 mm, while the second had a diameter of 0.48 mm and a length of 0.9 mm. The advantage of the first connector is that it is a very rigid connector compared to the second. The disadvantage is that it is bigger and more bulky than the second option and it is more difficult to line up with the transmission line.

The main advantage of the smaller connector is that it can easily be aligned. Another advantage is the Teflon dielectric that is better matched to the substrate thickness. This indicates that the microstrip to coax transition has less discontinuity. A higher quality transition leads to better calibration results. The drawback of this connector is that it has to be handled with extra care because it bends very easily.

4.5.1 Soft substrate

On the soft substrate, the smaller connector was used at first. The reason for this choice being that a 50 Ω impedance line on the substrate roughly has the same width as the connector pin

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diameter. The idea was that if the pin diameter and transmission line width were more or less the same size, it would reduce the transition effects.

The first calibration attempt presented very good results with a return loss (S_{11}) on the thru standard of less than -35 dB from 500 MHz up to 16 GHz. The second calibration attempt only offered a return loss of -25 dB on the thru standard. With every successive calibration, the repeatability became worse. Even if a calibration had been done, the measured return loss on a selected standard reduced every time a connection was broken and reconnected.

When the substrate and connectors were examined under a microscope, it was found that the substrate compressed at the place where the connector presses down on the board/track. As a result of this, the track cracked and broke. Every time the connection had been broken and reconnected, the track cracked and broke even further, up to the point where it was completely broken.

When the connectors were examined, it was found that the connectors had bent. When connectors were connected, vertical pressure was applied by hand. With connection repeatability in mind, it was considered that if more vertical pressure is applied when making the connections, the connection would be better and more repeatable. This was clearly not the case. To solve the above-mentioned problem, it was thought that less pressure should be applied when making a connection. The substrate then would not compress and the track would not break.

The connectors were replaced and a new set of calibration standard microstrip boards were etched. After a few measurements the same results were found as with the previous set of standards and connectors, the connectors were bent and the substrates compressed again. The tracks however were not broken this time. This was clearly not the solution to the problem.

The next best solution was to try the bigger connectors. These connectors would provide a larger contact area, and hopefully the substrate would then compress less. With the new connectors, the same tests were performed as with the first set of connectors. The results were much better. The results of these measurements were already discussed in section 4.4.1. It was however found that the substrate still compressed if too much pressure were applied. The same results were measured if the vertical pressure is not applied by hand, but only by the weight of the connector itself.

The main problem with the soft substrate is therefore the fact that is can compress very easily at the place where the connectors are applied. For the best repeatability at the connections, the

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connectors with the larger pin must be used with the only vertical pressure applied being that of the weight of the connector itself.

The repeatability is also a function of the alignment of the connectors to the tracks. For better repeatability results, extra care has to be taken with the alignment of the connectors before it is tightened.

4.5.2 Hard substrate

In the case of the hard substrate, the bigger connector was used at first since it produced good results with the soft substrate. On the hard substrate, the line widths of the standards are 0.38183 mm. With the connector pin diameter of 1.2 mm, the alignment of the connector to the track was more difficult. This could also be seen from the S_{11} parameter of the thru standard after a calibration had been done. A definite shift or drop in the figure was observed at the split frequency. This indicates that there was a definite difference in the connection quality on the two line standards during the calibration procedure. After every successive calibration the results looked different. It was then decided to try the connector with the smaller pin, for this would make alignment easier.

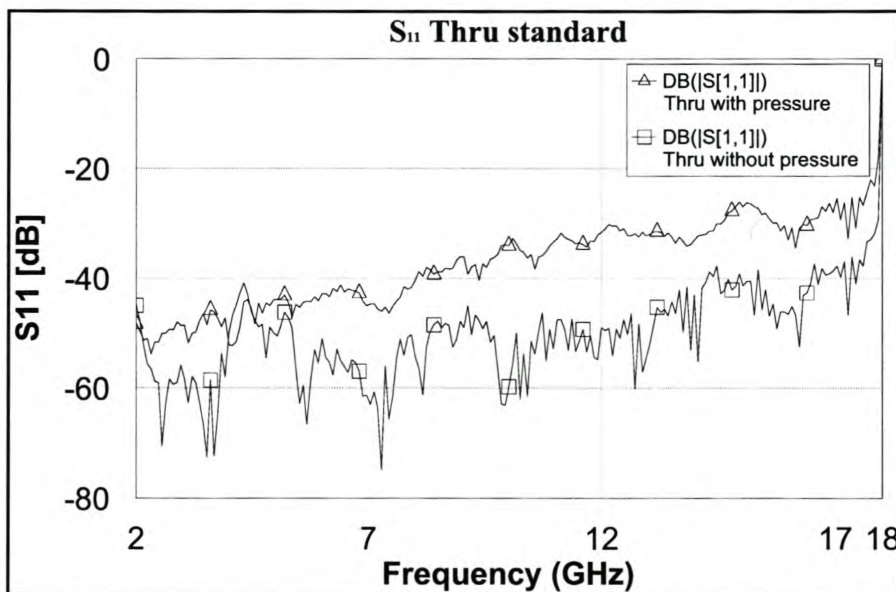

Figure 53: Measured S_{11} of the thru standard on hard substrate with and without applied pressure in the connectors

The results for the calibration done with the connectors with the smaller pins had already been presented in section 4.4.2. The results were very good and beyond expectation. In the

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presented results, the weight of the connector itself was the only contribution to vertical pressure applied. Experiments were done to see if the results could be improved by applying more vertical pressure in the connectors. The results in fact got worse when more pressure was applied.

Figure 53 shows a comparison between the measured return loss of the thru standard with and without the additional pressure applied to the connectors. From 7 GHz and above it can be seen that the trace where pressure was applied, has a degradation in the reflection of the thru standard of approximately 15 dB.

Under a microscope, it was found that no damage had been done to the standards itself, but the connectors had bent again. With the connector pins bent, there is less area under the connection. This would therefore explain the degradation in the return loss graphs.

4.5.3 Conclusion

In general, the problems with the soft substrate are that it compresses at the area where the connector is attached. The immediate solution to this problem is to use a connector with a larger pin. The larger pin would apply pressure across a larger area and this would reduce the compression of the substrate and cause less damage to the substrate and the tracks on the substrate. The connector with the larger pin is more robust and does not damage that easy.

The advantage of the hard substrate is that a connector with a smaller pin can be used. This would allow for easy alignment of the connectors with the tracks. Another advantage is that the substrate itself does not damage as easy as the soft substrate. The disadvantage of the connector is that much care must be taken not to damage it.

Despite the problems that were experienced with the jig, the design was very successful and very accurate measurements can be made.

4.6 Parameter extraction

In Section 4.1 the motives were given for device characterization. One of the motives was to try to find a linear model for a device to see how the actual device properties differ, or not, from the predicted properties based on the theoretical parameter values specified by the manufacturer.

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A TRL calibration kit was successfully designed and tested. In this section, PIN diodes in specific configurations that are relevant to switch design, will be measured on the TRL kit and then matched to theoretical models. The aim is not only to do parameter extraction, but also to use the data for design purposes in Chapter 5. The extracted parameters of the PIN diode itself will be based on the model presented in Figure 54.

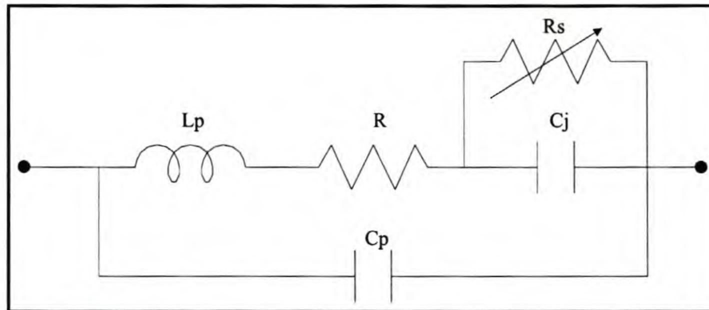

Figure 54: PIN diode model used for parameter extraction

The parameter extraction will be done on both hard and soft substrate. Different technologies can be applied to both substrate types. One can then see the advantage and disadvantage of using each substrate, and what properties can be expected from a diode mounted on these substrates.

In this and the following sections, when referring to an insertion loss or isolation graph, the S_{21} parameter will actually be plotted. In all the measurements performed, the diodes are forward biased with a 37.2 mA and reverse biased with 10 volts across the diode.

4.6.1 Soft substrate

On the soft substrate, two PIN diodes were measured for parameter extraction. The first was the MP61004 in a M-26 type packaging. The diode is product of *MDT Corporation*. The second is the HPND-4005 beam lead PIN diode from *Agilent Technologies*. Both diodes were used in a series connected configuration.

Since the calibration kit can calibrate from 500 MHz to 18 GHz, the parameters will be extracted in the same frequency range.

MP61004 PIN diode

The properties of the diode as given by the manufacturer, are shown in Table 8. The package interior is presented in Figure 55. The specific packaging was chosen because the pin widths

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are more of less the same width as that of a 50 Ω impedance line at 10 GHz on the chosen substrate. Since a switch will be designed to operate from 2-18 GHz, the diode is required to operate in that same band.

Part Number	Cj @ -10V Max. (pF)	Min Reverse breakdown voltage (V)	Max. Forward Resistance @20mA (Ω)	Typical Switching Speed (ns)	Typical Minority Carrier Lifetime (ns)
MP61004	0.06	100	2	9	15

Table 8: Properties of MDT MP61004 PIN diode

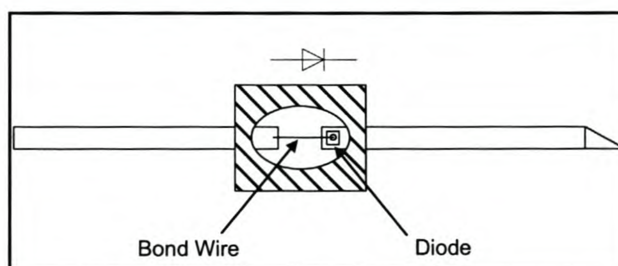

Figure 55: M-26 packaging from MDT Corporation

According to the manufacturer, this diode is designed to operate from 500 MHz to above 18 GHz. The manufacturer also gave their assurance that the chosen M-26 packing is suitable to operate in the same frequency range.

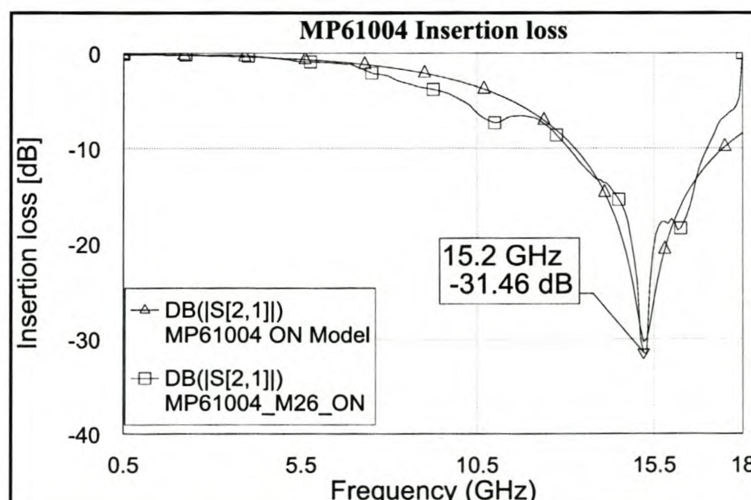

Figure 56: Insertion loss for MP61004 PIN diode in M-26 package

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Figure 56 shows the measured insertion loss of the diode. It is displayed as trace "MP61004_M26_ON". From the displayed data, it is clear that the diode is not fit to operate from 500 MHz to 18 GHz. It seems as if there is some resonant point at 15.2 GHz. The source of the resonance will be discussed later when parameter extraction on the diode is done.

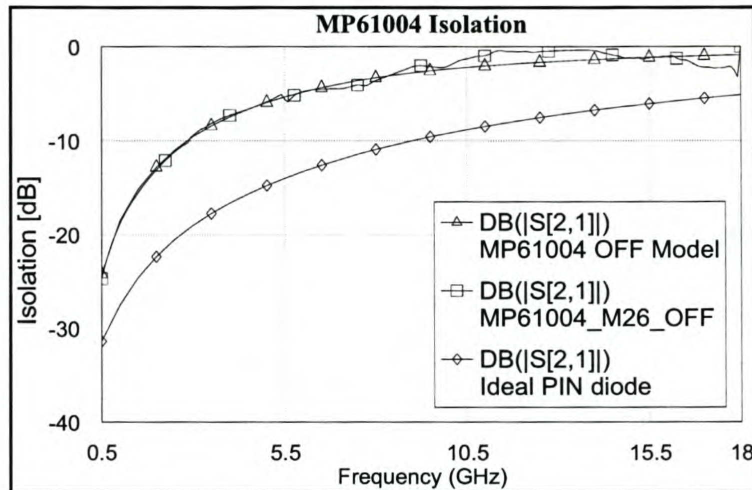

Figure 57: Isolation for MP61004 PIN diode in a M-26 package

Figure 57 shows the measured isolation of the diode. It is displayed as trace "MP61004_M26_OFF" on the graph. The figure also shows the isolation trace of an ideal PIN diode with a junction capacitance of 0.06 pF. One can see there is a difference of about 9 dB at 5 GHz and 5 dB difference at 15 GHz in the isolation.

The measured data was used to extract the necessary parameters to build a theoretical model to simulate the measured practical diode. The model presented in Figure 54 was used. The extracted parameter values as well as those specified by the manufacturer are shown in Table 9. Microwave Office was used to extract the parameters and display the required data.

Part number	Lp (nH)	Cp (pF)	R(Ω)	Rs (Ω)	Cj (pF)
MP61004-M26 (Measured)	0.84	0.13	0	2	0.06
MP61004-M26 (Specified)	0.4	0.1	0	2	0.06

Table 9: Extracted parameter values for MP61004 in M-26 packaging

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The insertion loss and isolation of the model are displayed together with the measured data in Figure 56 and Figure 57. The diode model closely resembles the measured diode data. The deviation in the insertion loss curve is probably due to extra and more complex parasitic elements in the packaging. It is very difficult to find a model for these elements.

From the extracted parameters, it can be seen that the parasitic capacitance plays a more significant role in the isolation than the junction capacitance. The measured isolation is less than a quarter of the simulated isolation of an ideal diode where no parasitic capacitance is present.

The insertion loss trace clearly has a resonant point. After the parameter extraction, it was found that the resonance was due to the parasitic inductance and capacitance. Equation 4.5 gives the formula for calculating the resonance frequency between these two elements. With $L_P = 0.84$ nH and $C_P = 0.13$ pF, the calculated value corresponds well to the measured value of 15.2GHz.

$$f_r = \frac{1}{2\pi\sqrt{L_P C_P}} \qquad 4.5$$

With the parasitic elements specified by the manufacturer, the resonant frequency would be 25.1GHz. The diode would then be able to operate from 500 MHz to 18 GHz. To verify that the supplied manufacturer data were incorrect, two diodes were tested. Both the diodes gave the same results.

The MP61004 PIN diode with the M-26 packaging can therefore not be used up to 18 GHz as specified by the manufacturers. The diode will later be tested in a different package on the hard substrate.

HPND-4005 PIN diode

The HPND-4005 PIN diode is a product of *Agilent Technologies*. It comes only in the standard beam lead packaging. The beam lead package and its dimensions are shown in Figure 58. The properties as specified on the datasheets are shown in Table 10. *Agilent Technologies* specify on their datasheets that this diode can operate from 1 to 18GHz. One thing to note is that the stated junction capacitance is calculated from isolation measurements done on the diode in a series configuration. It should therefore correspond well to the measured values on the TRL kit.

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Part number	Cj @-10V Typ. (pF)	VBR Min.	Forward Resistance @20mA Max. (Ω)	Minority Carrier Lifetime Typ. (ns)
HPND-4005	0.017	100	6.5	50

Table 10: Properties of HPND-4005 PIN diode [12]

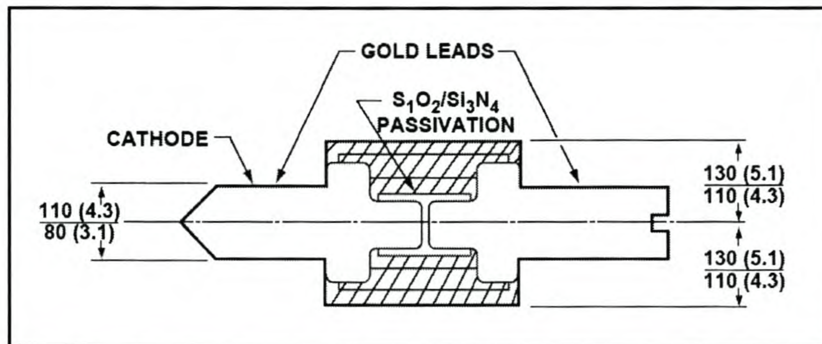

Figure 58: Beam lead package dimensions for HPND-4005 PIN diode[12]

(Dimensions are in um (1/1000 inch))

The diode was measured in an "open" environment with only the aluminium base as a ground i.e. it was not placed in a channel or waveguide environment. Silver leaded conductive epoxy was used to attach the diode to the transmission lines.

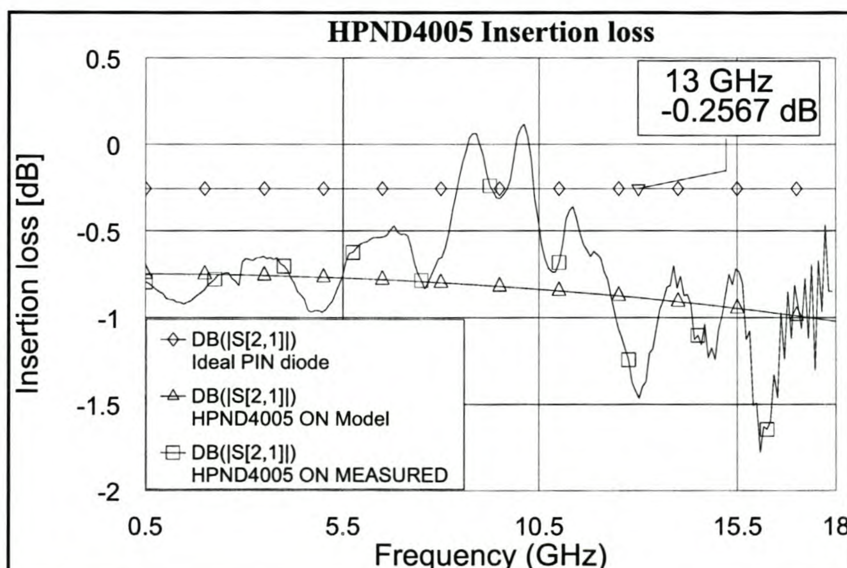

Figure 59: Insertion loss for HPND-4005 PIN diode

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Figure 59 shows the measured insertion loss of the HPND-4005 PIN diode. The data is marked as trace "HPND4005 ON MEASURED". From the displayed data, it can be seen that the diode can operate from 500 MHz to 18 GHz, as specified by the manufacturer. The insertion loss of an ideal PIN diode with a junction resistance of 6.5 Ω is also shown in Figure 59. The measured insertion loss is generally more than the expected 0.2567dB.

The reason why the insertion loss graph is not as "smooth" as expected, is not quite clear. The response between 16 and 18 GHz could be higher order modes that are present. The diode was placed in both a channel and waveguide environment to see whether it would make a difference in the results, but no dramatic differences were noticed. It could also be due to the epoxy that was used, but this could not be confirmed.

Figure 60 shows the measured isolation of the HPND-4005 PIN diode. It is displayed as trace "HPND4005 OFF MEASURED". Also shown on the graph is the simulated isolation of an ideal PIN diode with a junction capacitance of 0.017 pF. There is a difference of about 7 dB.

The extracted and specified parameters are listed in Table 11. The diode junction resistance and capacitance were found to be the same as the specified values, but the parasitic elements varied significantly.

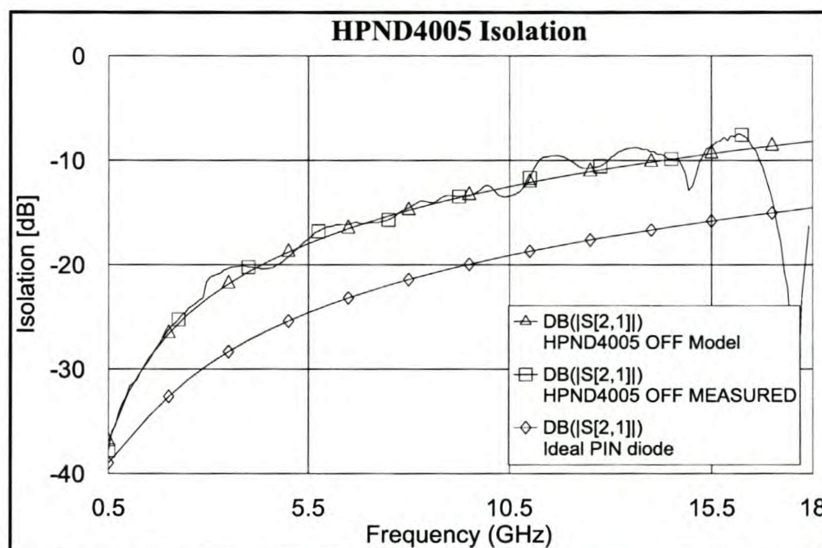

Figure 60: Isolation for HPND-4005 PIN diode

Part number	Lp (nH)	Cp (pF)	R(Ω)	Rs (Ω)	Cj (pF)
HPND-4005 (Measured)	0.2	0.021	2.5	6.5	0.017
HPND-4005 (Specified)	0	0	0	6.5	0.017

Table 11: Extracted and specified parameters of the HPND-4005 PIN diode

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The parasitic capacitance was found to be 0.021pF. Since the specified junction capacitance of the diode was calculated from an isolation measurement, it was expected that the measured capacitance would compare well to the specified value of 0.017 pF. Because the diode is so small, it was likely that there would be coupling across the diode. An electromagnetic (EM) simulation was done in Microwave Office to verify the coupling from line to line across the diode. Figure 61 shows the schematic that was used for the simulation. The diode gap is the same size as the diode.

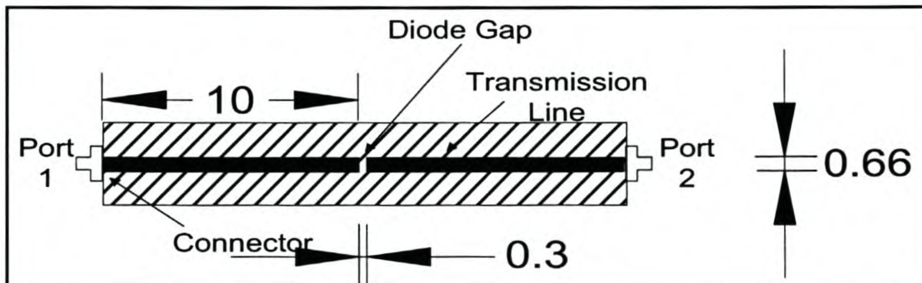

Figure 61: Electromagnetic simulation schematic

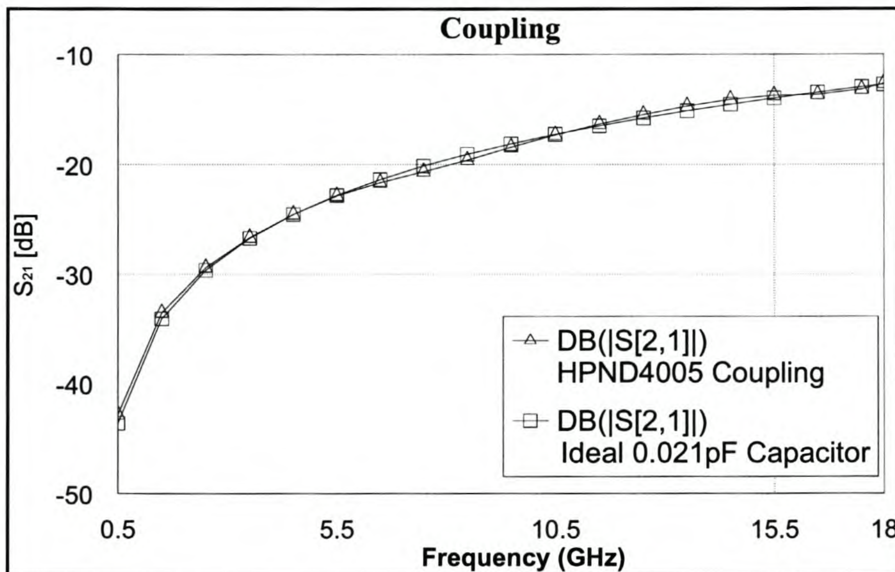

Figure 62: Estimated coupling across HPND-4005 PIN diode

The coupling was determined by simulating S_{21} of the schematic shown in Figure 61. Figure 62 shows the EM simulation results. The S_{21} parameter of an ideal 0.021 pF capacitor is also displayed on the graph. These two traces are almost identical. It would then be fair to say that the coupling could be simulated as a capacitance of 0.021 pF. This value corresponds well to

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the measured parasitic capacitance. The parasitic capacitance is therefore due to the coupling across the diode gap.

The measured series parasitic resistance of 2.5 Ω is much higher than the expected 0 Ω. The resistance of the epoxy on both sides of the diode were measured with a multimeter and found to be 1 Ω and 1.4 Ω respectively at DC. This could explain the measured parasitic series resistance. This series resistance alone would contribute to an offset of about 0.21 dB to the insertion loss graph.

A model, built from the extracted parameter values listed in Table 11, was simulated in MWO. The insertion loss and isolation are plotted in Figure 59 and Figure 60 as traces "HPND4005 ON MEASURED" and "HPND4005 OFF MEASURED". Generally, the model properties closely match those of the measured diode. The insertion loss variations are impossible to model.

To improve the isolation of the diode, it was placed in both a channel and a waveguide environment. No significant change in the isolation was noticed.

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4.6.2 Hard substrate

In this section, the MP61004 diode will be used in a "P10" package. The diode will be connected in three different configurations that are all relevant to PIN diode switch designs. The aim is to identify what type of properties can be expected from these configurations, as well as to see which configurations would be preferable above the others with regard to a specific switch property requirement. The configurations are:

- Series configuration
- Parallel configuration with diode next to track/transmission line
- Parallel configuration with track split and diode placed between the two tracks/transmission lines

The P10 package outline and its dimensions are shown in Figure 63. The base of the diode is the cathode and the pad on top is the anode.

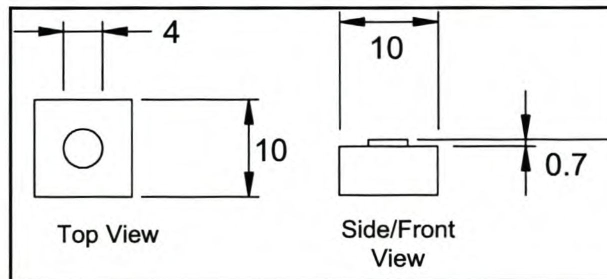

Figure 63: Top, side and front view of the P10 package for MP61004 PIN diode (Dimensions are in mils)

Part Number	Cj @-10V Max. (pF)	Min Reverse breakdown voltage (V)	Max. Forward Resistance @20mA (Ω)	Typical Switching Speed (ns)	Typical Minority Carrier Lifetime (ns)
MP61004-P10	0.058	100	2	9	15

Table 12: Specified properties of MP61004 Pin diode in P10 package

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The properties of the diode, as specified by *MDT Corporation*, are listed in Table 12. The junction capacitance is a bit lower than with the M-26 package.

The hard substrate TRL kit has been designed to calibrate from 2 GHz to 18 GHz. The diodes was characterised in the same frequency range. The bond wire that will be used in all the configurations has a diameter of 0.7 mils.

4.6.2.1 Series configuration

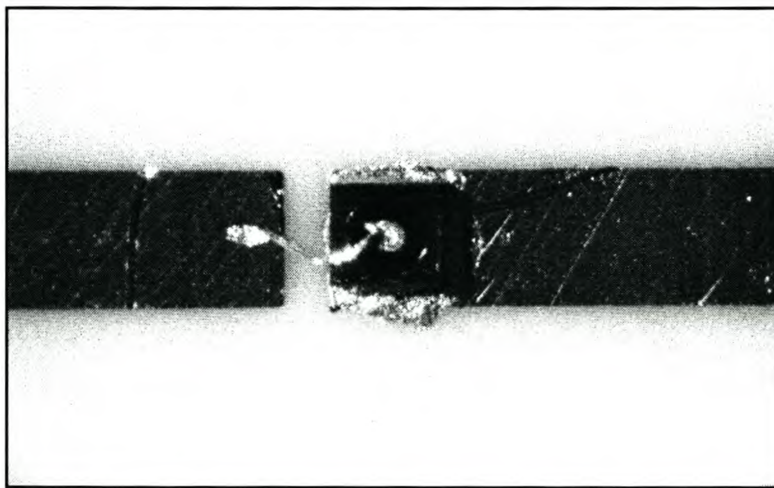

Figure 64: Photograph of series connected MP61004 PIN diode

Figure 64 shows a photograph of the series connected PIN diode. The cathode is on the right hand side track and the anode is connected to the left track with a gold bonding wire. The gap between the two tracks is 0.1 mm wide. The gap should provide adequate isolation between the tracks, while keeping it narrow enough in order to keep the inductance from the bonding wire small, so that no resonances appear in the 2 to 18 GHz band. Both the tracks are 0.381 mm wide.

Figure 65 shows the measured insertion loss of the diode. With the inductance of the bond wire in mind, the increase in the insertion loss is expected. The dramatic decrease in the insertion loss at about 16 GHz will be discussed later when the parameter extraction is done.

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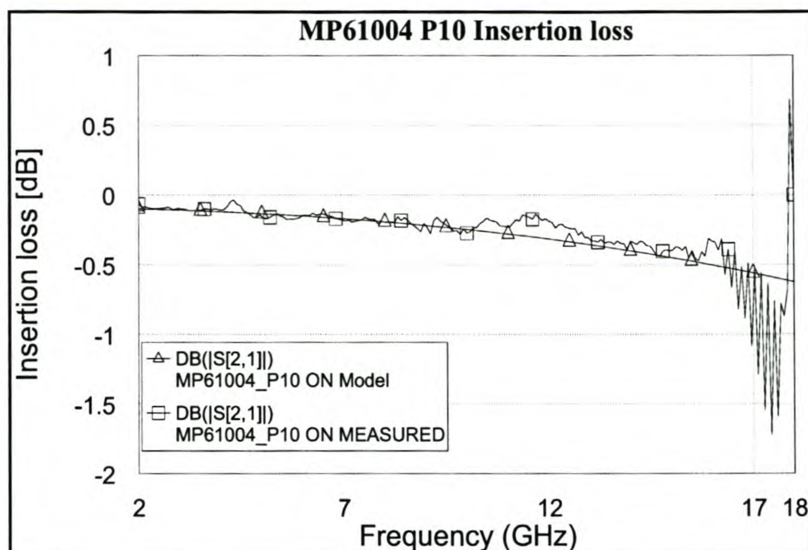

Figure 65: Insertion loss for series connected MP61004 PIN diode with P10 packaging

In Figure 66 the measured isolation of the diode is shown. The isolation of an ideal PIN diode with a junction capacitance of 0.059 pF is also plotted on the same graph. One can see that the shape of the measured isolation takes on the same form as that of the ideal diode, but has an offset of about 6 dB. This is probably due to parasitic capacitances that are present in the measured diode.

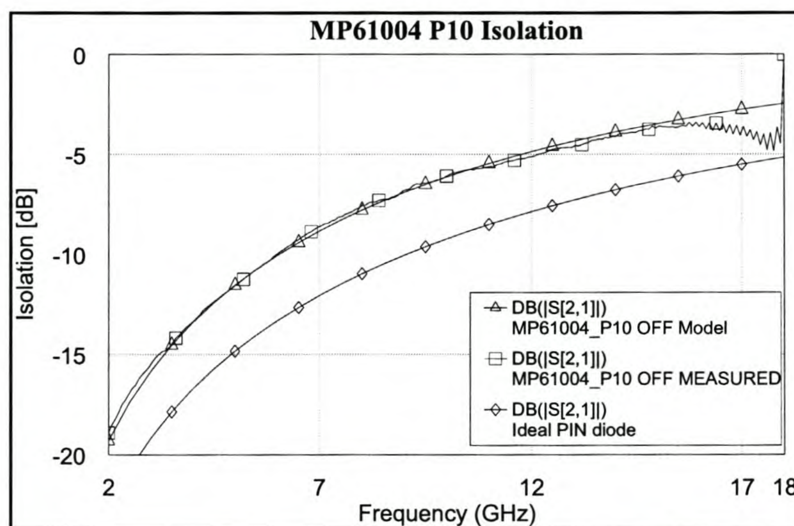

Figure 66: Isolation for series connected MP61004 PIN diode with P10 packaging

The model that will be used for parameter extraction for this configuration is shown in Figure 67. Instead of the normal ideal inductor that was implemented in the soft substrate model, the bond wire element, which is a standard element in Microwave Office, was integrated into the model.

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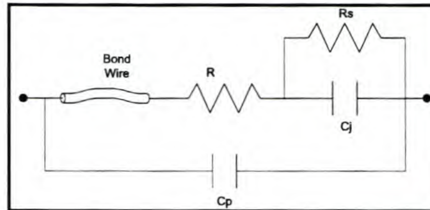

Figure 67: Model used for diode characterisation in hard substrate

The extracted and specified parameter values from the manufacturer are listed in Table 13. The specified parasitic inductance was obviously not specified by the manufacturer. The inductance value was expected from the specific bond wire length. The measured inductance just confirmed the calculated value.

Part Number	Lp (nH)	Cp (pF)	R (Ω)	Rs Ω	Cj (pF)
MP61004-P10 (Specified)	0.3	0	0	2	0.59
MP61004-P10 (Measured)	0.29	0.028	0	1	0.59

Table 13: Specified and measured parameters of the MP61004-P10 PIN diode

Overall, the extracted and specified parameter values compare very well. The only major difference is in the coupling capacitance that was measured. To confirm the coupling across the gap, the same EM simulation that had been performed for the HPND-4005 diode, was repeated for this diode. In the simulation, the gap and track width were adjusted to 0.1 and 0.381 mm respectively. The equivalent capacitance to present the coupling was found to be 0.018 pF. This value is still smaller than the expected 0.028 pF.

The diode properties of both the extracted diode model and the measured diode are plotted in Figure 65 and Figure 66. The properties of the model are marked as traces "MP61004_P10 ON MODEL" and "MP61004_P10 OFF MODEL" respectively. One can see that the extracted model is a good representation of the practical measured diode.

In both the insertion loss and isolation graphs, a definite deviation at about 16 GHz can be seen. This phenomenon could not be addressed while doing the parameter extraction. The

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only explanation for the deviation is that either the diode is not able to operate above 16 GHz, or because higher order modes are present. It is more likely that higher order modes are present, but this could not be confirmed.

4.6.2.2 Shunt configuration with diode placed next to the track

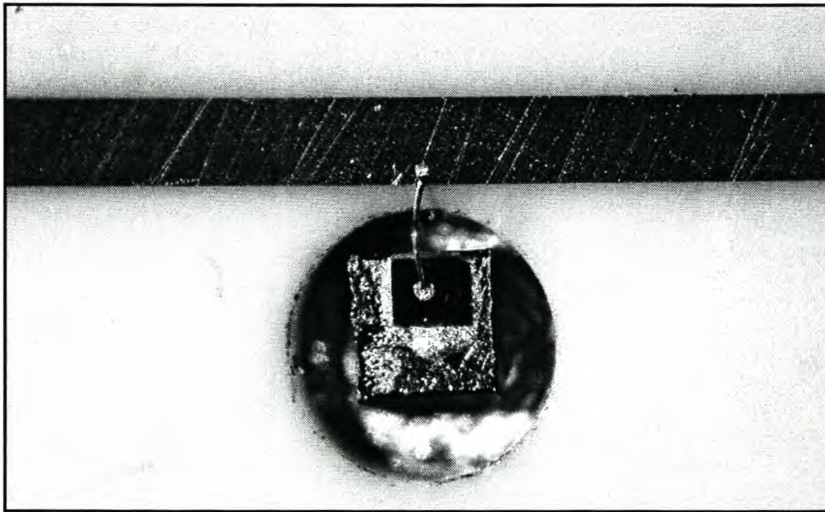

Figure 68: Photograph taken under microscope of a shunt configuration with diode next to track

Figure 68 shows a photograph of diode in a shunt configuration with the diode placed next to the track. With this diode, the cathode is placed on ground and the anode is connected to the track. With this type of connection, a good ground connection is required. To achieve the required ground connection, a hole is drilled through substrate onto the "ground". The diode is then mounted onto a covar standoff in the hole, directly onto "ground". The standoff is used to bring the diode to the same level as the track in order to minimise the bond wire length. As the bond wire contributes to the parasitic inductance of the diode, it is sensible to keep it as short as possible.

Figure 69 shows the measured insertion loss for the MP61004 diode in this configuration. The insertion loss is measured with the diode being reverse biased. The data is displayed as trace "MP61004 P10 OFF MEASURED" on the graph. The results looks similar to that of the series configuration diode. The gradual increase in the insertion loss is due to the junction capacitance of the diode which is frequency dependant. The same dramatic increase in insertion loss is noticed at 16 GHz.

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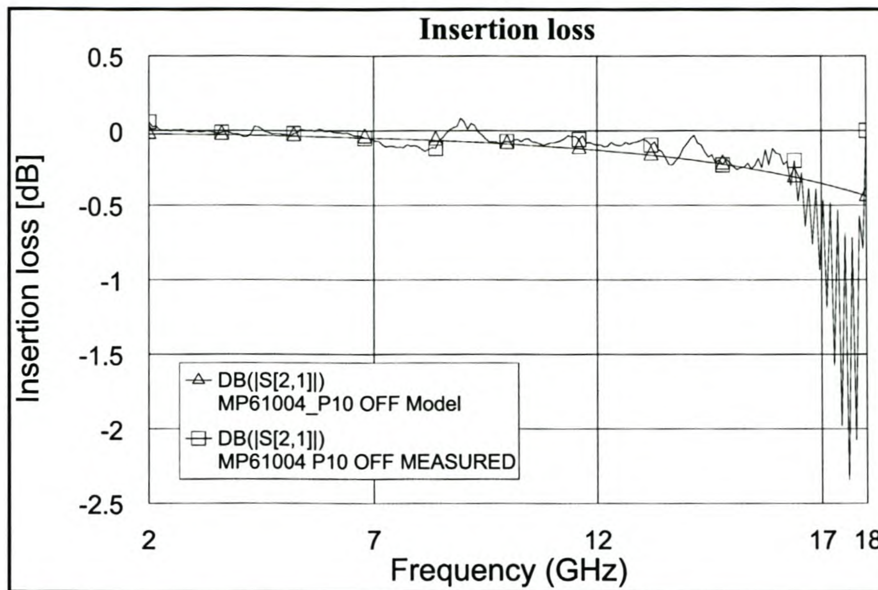

Figure 69: Insertion loss for MP61004 diode in shunt configuration with diode next to transmission line

Figure 70 shows the measured isolation of the diode. The diode is forward biased to provide the necessary isolation. The decrease in the isolation is due to the bond wire inductance and was therefore expected. It can clearly be seen that this configuration is not capable of providing high isolation at higher frequencies.

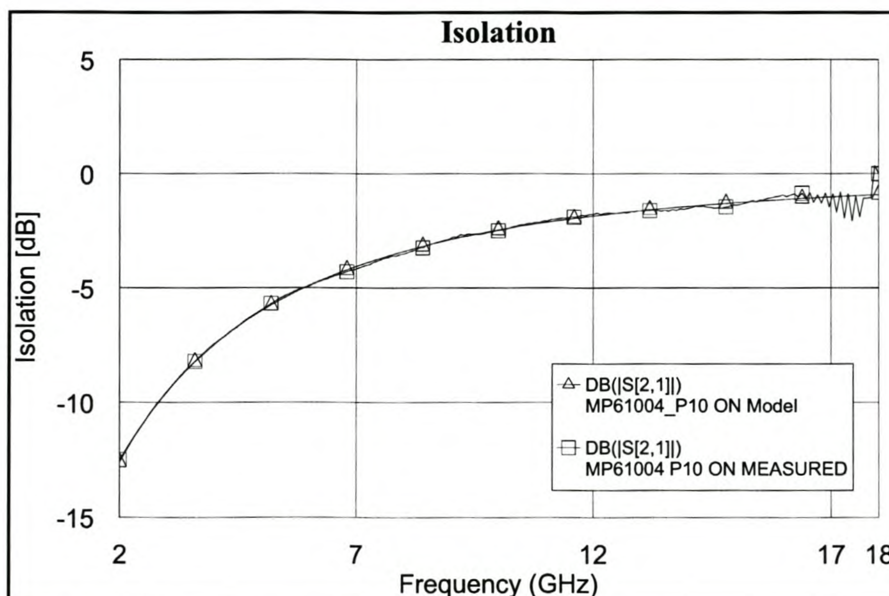

Figure 70: Isolation for MP61004 diode in shunt configuration with diode next to transmission line

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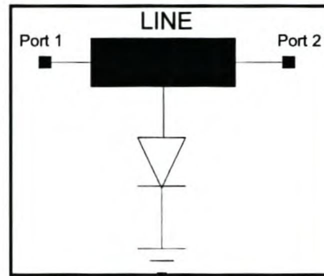

Figure 71: Schematic used to simulate the shunt configuration.

The simulation schematic that was used for parameter the extraction of this shunt configuration is shown in Figure 71. The transmission line had a width of 0.381 mm. The model for the diode itself is presented in Figure 67. The extracted parameters are listed in Table 14.

Part Number	Lp (nH)	Cp (pF)	R (Ω)	Rs Ω	Cj (pF)
MP61004-P10 (Specified)	0.45	0	0	2	0.59
MP61004-P10 (Measured)	0.49	0	0	1.55	0.59

Table 14: Specified and measured parameter values for MP61004 diode in P10 package

The specified and measured parameters correlate exceptionally well. The parasitic inductance was estimated to be 0.45 nH. This value was calculated from the bond wire length. It can be seen from the parameters that no parasitic capacitance is present in this configuration.

The insertion loss and isolation of the extracted model is displayed in Figure 69 and Figure 70. It is displayed as traces "MP61004_P10 OFF MODEL" and "MP61004_P10 ON MODEL".

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4.6.2.3 Shunt configuration with diode between the transmission lines

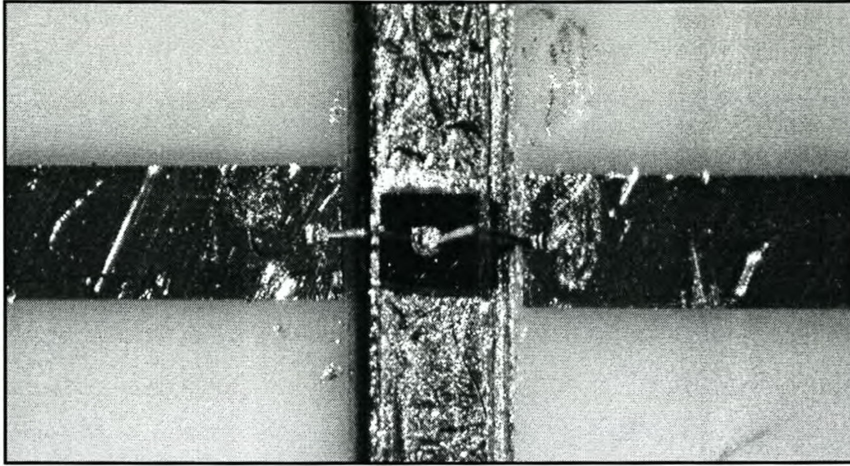

Figure 72: Photograph taken under microscope of the shunt connected diode with the transmission line split and the diode placed between the transmission lines

In this section a second shunt configuration will be discussed. In this configuration the transmission line is split in two. The diode cathode is mounted onto ground, between the two tracks and bond wires are then used to connect the tracks to each other as well as to the anode of the diode. Figure 72 shows a photograph of this. In the photo, the tracks lie in the horizontal plane. Though it not very clear in the photo, the diode is mounted on a covar base to lift the diode to be level with the tracks. This is done to reduce the bond wire length needed to connect the tracks to the diode.

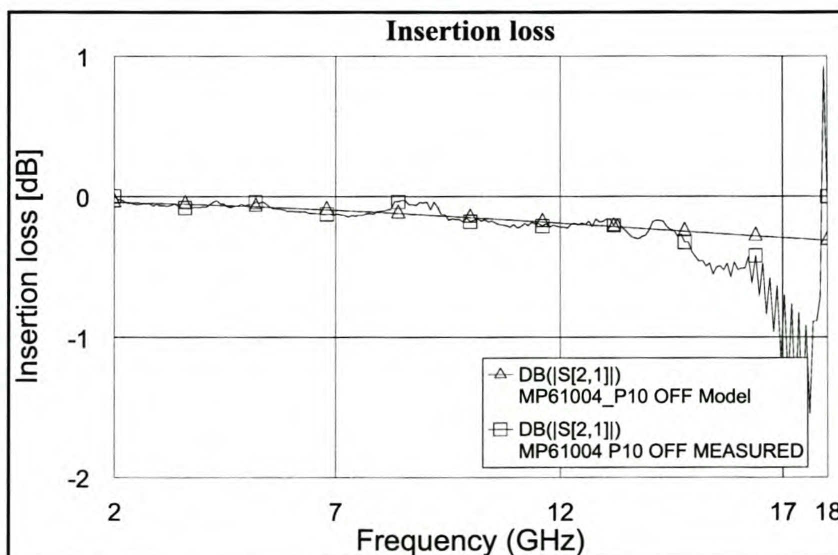

Figure 73: Insertion loss for MP61004 diode in shunt configuration with diode placed between the transmission lines

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Figure 73 shows the measured insertion loss for the diode in this shunt configuration. There is no significant improvement above the other diode configurations. It looks as if the diode is performing well up to 16 GHz after which the insertion loss decreases noticeably fast. Based on the previous measurements, this decrease above 16 GHz was expected.

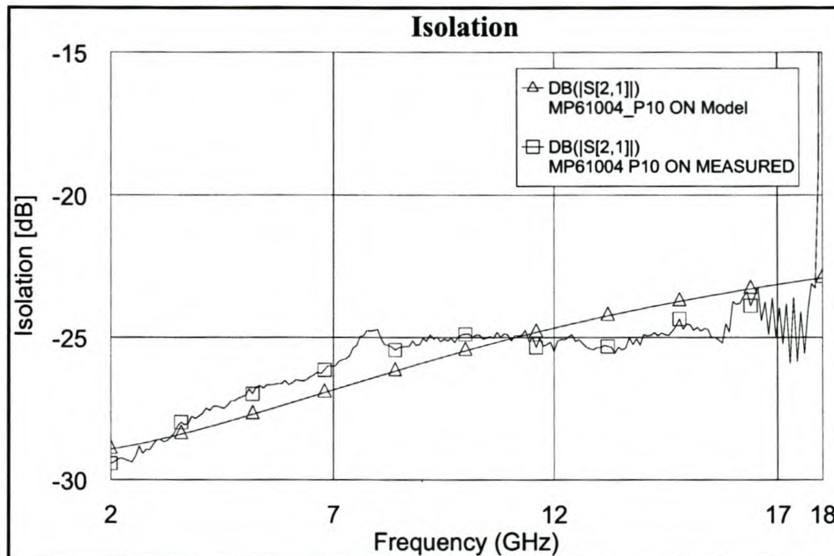

Figure 74: Isolation for MP61004 diode in shunt configuration with diode placed between the transmission lines

Figure 74 shows the measured isolation. One can see that there is a huge improvement in the isolation compared to the previous two configurations.

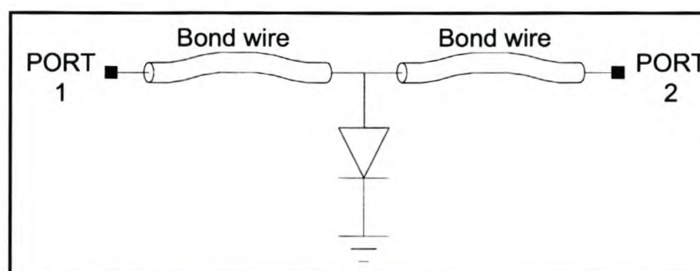

Figure 75: Model used for parameter extraction

Figure 75 shows the model that was used in MWO for parameter extraction for this diode configuration. The model for the diode itself is shown in Figure 54 on page 68.

The extracted and specified parameter values for this configuration are listed in Table 15. Except for the junction resistance and parasitic inductance, the extracted and specified parameters are identical.

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Part Number	Bond wire length (mm)	Lp (nH)	Cp (pF)	R (Ω)	Rs Ω	Cj (pF)
MP61004-P10 (Specified)	0.22	0	0	0	2	0.59
MP61004-P10 (Measured)	0.22	0.019	0	0	0.99	0.59

Table 15: Specified and measured parameter values for MP61004 diode in P10 package

The properties of the simulation model are shown in Figure 73 and Figure 74. From the results shown, it can be seen that the model is a good approximation of the measured diode.

4.7 Results

Overall, this chapter produced very good results. It has demonstrated a few techniques on how to do parameter extraction. TRL calibration was the preferred method for device characterisation. A TRL kit with two calibration sets were successfully designed and tested. This made it possible to do parameter extraction on both hard and soft substrates.

The results and recommendations of the TRL kit and calibrations standards were discussed in section 4.5 and will therefore not be repeated here.

The parameter extraction results on both the soft and hard substrates were very good and revealed relevant information. On the soft substrate, it was indeed found that the manufacturer data is not always correct and this fact has to be taken into account. It was proved that the packaging plays a significant role in the device operation. If for instance a design had been done with the M-26 packaging at 15 GHz, there would be no way that the designed switch would have worked within specifications. Now, before the design is performed, one of the possible problems could be eliminated.

On the hard substrate, the results were in general better than those on the soft substrate were. It was shown that the simulation software provides a good approximation for parasitic elements, such as bond wire, at high frequencies. The expected and measured values compared very well up to 16 GHz. It is expected that higher order modes exist above this frequency, but it could not be confirmed.

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It is now possible to characterise a device in the environment in which it will operate. This information can be implemented in designs, and will reduce the amount of design iterations until a final design is reached.

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5 Practical switch

In Chapter 3 different switch topologies and design guidelines for the given topologies were discussed. In all the designs it was assumed that the elements were ideal. This was done to determine the effect of the different PIN diode parameters and topologies on the switch operation.

In a practical switch, parasitic elements are always present and can not be ignored. In this chapter, it will be shown how to account for all these elements in the switch design. A few guidelines for designing a compound configuration switch will be discussed, after which a preferred design procedure will be presented. This design procedure will then be used for designing and building a practical switch.

The advantages and disadvantages of hard and soft substrate design will also be discussed in the subsequent sections.

5.1 Compound switch configuration

The series and the shunt connected PIN diode switch configurations were discussed in Chapter 3. The series configuration switch has low insertion loss across a large bandwidth while the shunt configuration switch on the other hand offers high isolation, but is not as broadband. The compound configuration switch is a cascade connection of the series and shunt configuration switches. It offers low insertion loss as well as good isolation over a large bandwidth, giving an overall improved performance [5]. A schematic diagram of a SPST compound switch is shown in Figure 76.

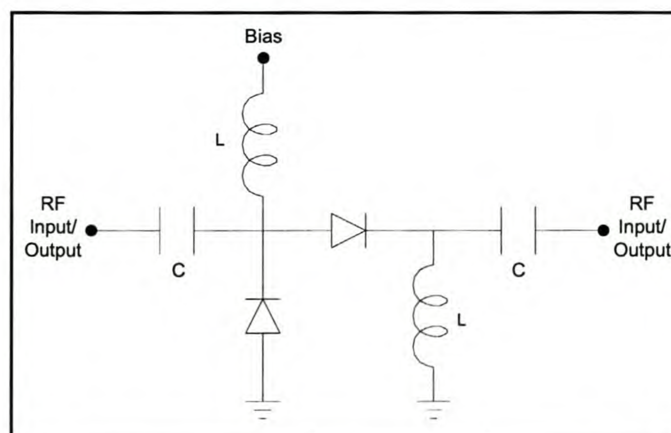

Figure 76: Schematic diagram of SPST compound configuration switch

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5.2 Insertion loss

In the "on" state, the series diode must be forward biased and the shunt diode reverse biased. Assuming that the transmission line connecting the diodes is ideal, then the insertion loss is equal to the sum of the individual series and shunt configuration switches. The formula used to calculate the insertion loss is shown in equation 5.1. It is easily derived from the ABCD parameters of the individual series and shunt connected diodes.

$$IL = 10Log\left[\left(1+\frac{R_s}{Z_0}\right)^2 + \left(\pi f C_T\right)^2 \left(Z_0 + R_s\right)^2\right] \qquad \text{[dB]} \qquad 5.1$$

where: R_s is the series resistance of the series diode

C_T the junction capacitance of the shunt diode

In equation 5.1 it is assumed that both the diodes are ideal. To include the parasitic elements, R_s and C_T can each be replaced with an impedance of the form $Z = R' + jX'$, where R' and X' represents the diode equivalent series resistance and reactance at the relevant biasing conditions.

If an additional series or shunt diode, or combination of both is added, the insertion loss of the additional diode/s must be included.

5.3 Isolation

In the "off" state, the series diode must be reverse biased and the shunt diode forward biased. As with the insertion loss, the isolation is equal to the sum of the isolation presented by the respective series and shunt diodes. Equation 5.2 shows the formula for calculating the isolation for a SPST compound switch. In the equation it is assumed that ideal diodes are used. To include the parasitic elements of the diodes, a similar procedure to that followed in Section 5.2 needs to be applied.

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$$Isolation = 10Log\left[\left(1+\frac{Z_0}{2R_s}\right)^2 + \frac{1}{4\pi fC_T Z_0}\left(1+\frac{Z_0}{R_s}\right)^2\right] \quad \text{[dB]} \qquad 5.2$$

If an additional series or shunt diode, or combination of both is added, the isolation of the individual diode must be added to that calculated using equation 5.2.

In a SPMT configuration, an additional 6 dB of isolation must be added to equation 5.2.

5.4 General design information

This section will give general information and guidelines on the design of a compound configuration switch. These guidelines will be used in the design of a practical switch which is to be built and tested. The information provided in this section will be based on simulations done in MWO only. These design guidelines were simulated and tested on 10 mil, 15 mil and 25 mil thick substrates with the dielectric constant varied between 9.5 and 10. The maximum frequency where these design guidelines are still valid on the different substrates, is the frequency where the length of a quarter wavelength line is equal to the width of a 50 Ω line at that frequency.

The properties of the substrate that will be used for demonstration and validation purposes, in this chapter, are listed in Table 7 on page 53. On this substrate the maximum operating frequency is 30 GHz.

The model derived from the extracted parameter values of the HPND-4005 PIN diode will be used in the simulations. These parameter values are listed in Table 11 on page 73. The bias circuitry and coupling capacitors are assumed ideal at this stage. The switch will be designed to operate in a 50 Ω system.

5.4.1 Compound switch

Figure 77 shows a schematic diagram of a SPDT compound PIN diode switch. The switch is symmetrical around port 2. As mentioned previously, the T-junctions are set up to have a horizontal rectangular shape as apposed to a "T" shape.

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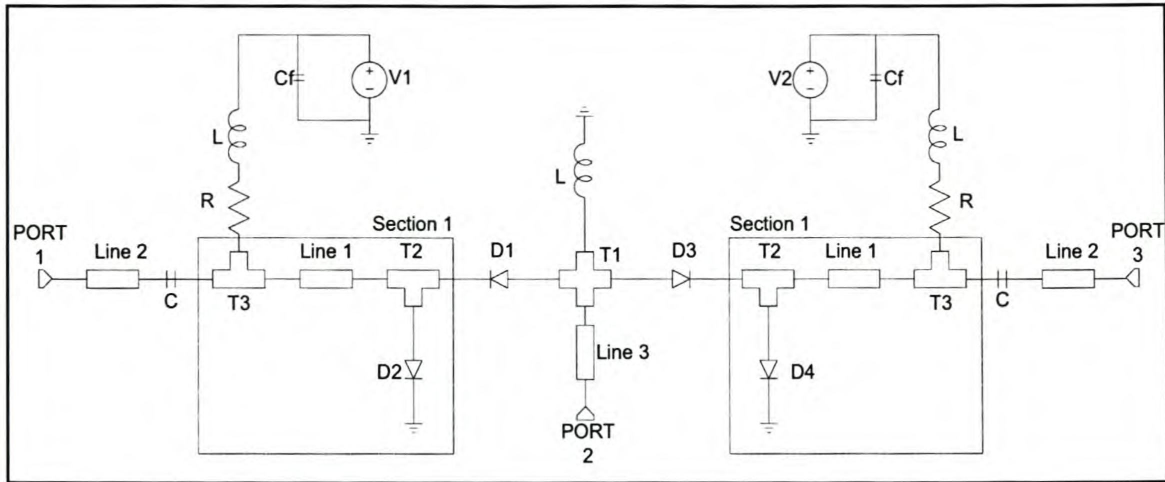

Figure 77: Schematic diagram of SPDT compound configuration switch used in MWO

The design guidelines will be discussed hereafter:

5.4.1.1 Influence of junction T1:

The width of T1 influences the return loss at the RF ports and has to be as small as possible. The length may be varied to adjust the bandwidth, but must be shorter than a $\lambda/4$ at f_h. If the rest of the circuit can be seen as a "load", and the load changes for any change in circuitry, then for every "load" there exists a certain ratio between the length and width of T1 for which the return loss is optimum. The length of T1 has minimal influence on the isolation. In view of the fact that the components must fit onto the junction when constructed, the minimum dimensions of the junction are limited by the orientation of components and type of substrate used. This statement will become clear when the difference between the hard and soft substrate are discussed.

5.4.1.2 Influence of Section 1

The area marked "Section 1" is the critical part of the switch design. It influences the isolation, return loss and bandwidth of the switch. Improved isolation, return loss and bandwidth is achieved if the series and shunt diodes are mounted as close as possible to each other.

In order to get the required bandwidth, a trade-off has to be made between the isolation and the return loss. This trade-off is made by adjusting the geometry of T2, T3 and Line 1. T2 has the greater influence on the isolation whereas the combination of Line 1 and T3 generally influence the return loss.

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5.4.1.3 Influence of T2

The width of T2 significantly influences the isolation and is used to set the maximum achievable isolation with a reasonable return loss at the RF ports. For every diode, with its associated parasitic elements, there exists an optimum impedance for T2 for which the isolation is a maximum. This impedance is dependant upon the diode and can therefore not be specified in any way. The length of T2 should be made as small as possible, but never shorter than the line width.

5.4.1.4 Influence of Line 1 and T3

The combination of Line 1 and T3 can be seen as a "step impedance transformer" and is used to adjust the bandwidth in terms of the return loss at the RF ports. Their influence on the isolation is minimal. In most cases, at frequencies below 18 GHz, Line 1 can be left out and the step impedance between T3 and T2 will be sufficient to do the necessary matching. If both T3 and Line 1 are used, the lengths of T2 and Line 1 do not play a major role and should be kept as short as possible with the minimum length being the line width. If only T3 is used, optimal results are found when the length of T3 is set to $\lambda/4$ at f_h. In both cases, the widths of the lines are more important for impedance matching than the lengths. The required impedance value for T3 and Line 1 for a specific bandwidth, depends upon the diode properties and can therefore not be specified.

If adjusting Line 1 and T3 is not sufficient to get an acceptable return loss at the RF ports, one can either adjust the length of T1 or the width of T2 to lower the overall return loss. This adjustment is done at the cost of isolation.

5.4.1.5 Simulation results

Figure 78 shows the simulated response of the switch shown in Figure 77. In this simulation, port 2 is the common port, port 1 is in the "on" state and port 3 in the "off " state. Also shown is the isolation and insertion loss traces of the switch with an ideal diode used instead of the practical model. These traces were added to compare the results of the compound switch with those presented for the series- and shunt connected switches discussed in Chapter 3. The return loss does not change drastically with the change from the practical to the ideal diode and was therefore not displayed.

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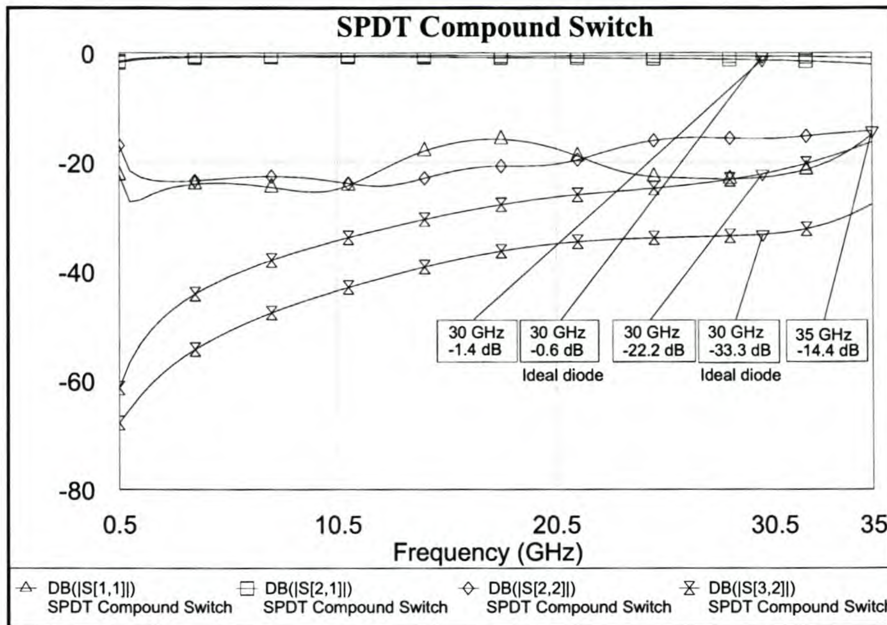

Figure 78: Simulated response for SPDT compound configuration switch shown in Figure 77

The switch is well matched across the band with the return loss better than -14.4 dB at both ports 1 and 2. From the results it is clear that this configuration combines the advantages of both the series- and shunt configuration switches. If one looks at the ideal case and compare the results shown in Figure 78 to those of the SPST series configuration switch presented in Figure 18 on page 26, the insertion loss of the compound switch, with two diodes, is almost the same as that of the SPST series configuration switch with one diode.

The simulated results of a SPDT series configuration switch with two diodes were shown in Figure 23 on page 30. At 30 GHz, this switch provides about the same isolation as the compound switch. The insertion loss of the compound switch however, is half that of the series switch. This indicates that in theory, for the same bandwidth, isolation and number of diodes used, the insertion loss can be halved if the compound configuration is used instead of the series configuration.

The isolation of a shunt configuration switch should in theory not be frequency dependant. If the average isolation of the shunt configuration switch with one diode (see Figure 36 on page 44) can be taken as 20 dB, then the total isolation for the compound switch with two diodes is the sum of the isolations of the individual series and shunt configuration switches with one diode each.

In Figure 78 it can also be seen how the results of a switch differ when a practical measured model of a diode is used instead of the ideal diode model, as specified by the manufacturers. The results look very different. The isolation with the practical diode included, is two thirds of

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the expected value and the insertion loss is more then double the expected value. Even though it is not an exact representation of a practical switch, for the capacitors, resistances, inductors and connector transitions are assumed ideal, it is still far more accurate than when the ideal diode is used. It gives an idea of the results that can be expected.

For additional isolation, three options are available. One can either add an additional series diode, or an additional shunt diode, or a combination of both.

5.4.2 Compound switch with additional series diode

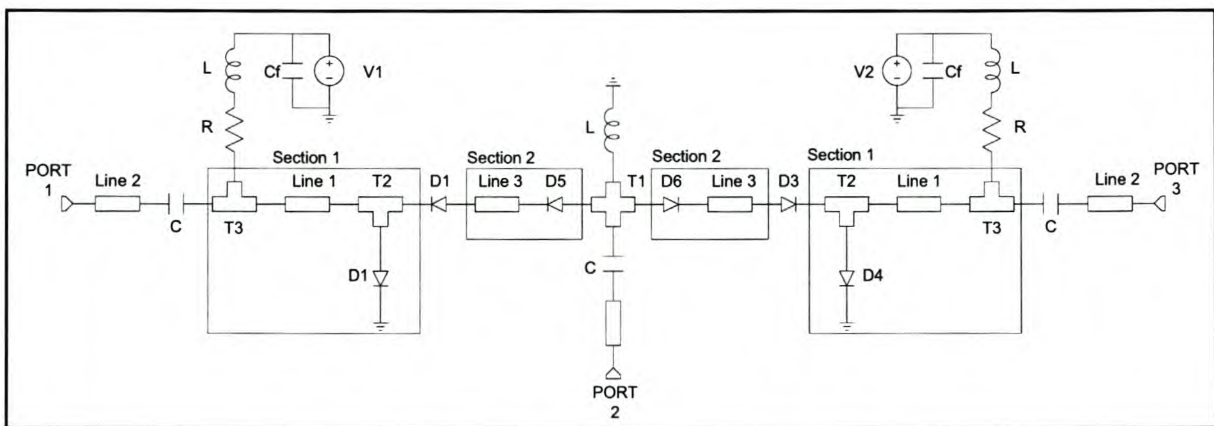

Figure 79: Schematic diagram of SPDT compound configuration switch with additional series diode

Figure 79 shows a SPDT switch where an additional series diode has been added. The additional diode is shown as Section 2 in the schematic.

If the diode D1 in Figure 77 can be seen as a "load", then the addition of Section 2 in Figure 79 can be seen only as a change in the load. This would then indicate that all the design guidelines discussed above still hold for this case where the additional diode has been added. Figure 80 shows the simulated response of the SPDT switch with the additional series diode.

With the addition of Section 2 the isolation is improved, but the insertion loss deteriorated. Below 18 GHz, the return loss is not influenced much by the addition of Section 2. Above this frequency, it becomes increasingly difficult to keep the return loss below 12 dB. The reason for this is, the circuit, from a practical and manufacturing point of view, becomes too small. The return loss becomes very sensitive to variation in line lengths and widths. This is not desirable for manufacturing or production purposes.

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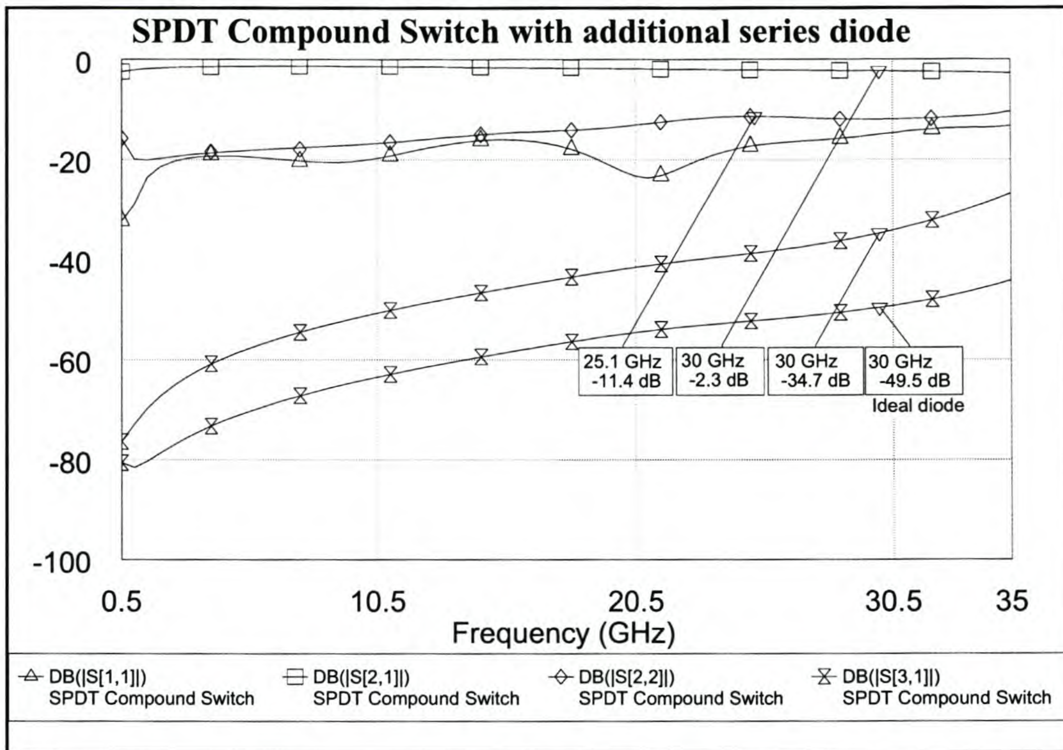

Figure 80: Simulated response for SPDT compound configuration switch with additional series diode

One would also notice that the additional isolation, provided by the extra diode, is different for the ideal and practical diode. This is because in the case of the ideal diode, one does not have to sacrifice as much isolation as with the practical diode to tune the return loss to obtain the required bandwidth. If the switch is designed to operate below 18 GHz, the return loss is not influenced much when exchanging the practical and ideal diodes in the circuit. Since no tuning is then needed for improving the return loss, the additional isolation in both cases are almost the same.

In general, the guidelines for the geometry of Line 3 are as follows:

If the switch operates below 18 GHz, for maximum isolation and return loss, the length of Line 3 should be a $\lambda/4$ of f_h, where f_h is lower than 18 GHz. The line should have an impedance equal to Z_0 at f_m. For operation between 18 and 30 GHz, the impedance of Line 3 should be lower than Z_0 and the length should be $\lambda/4$ of f_h. These guidelines are very general and may vary under certain circumstances, especially at the higher frequencies.

With the additional series diode, the insertion loss increased by 0.9 dB. If the model of the practical diode is extrapolated to 30 GHz, the diode, in the "on" state, has an insertion loss of 0.9 dB at this frequency. This confirms the expected increase in the insertion loss of the switch.

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In Figure 24 (on page 31) it was shown that the isolation, at 30 GHz, for the SPDT series configuration switch with two series diodes is about 28 dB. If this is added to the 20 dB isolation provided by the parallel-connected SPDT switch with one diode, it compares favourably to the simulated 49.5 dB for the compound switch with one parallel and two series diodes.

5.4.3 Compound switch with additional shunt diode

Figure 81 presents the case where an additional shunt diode has been added to improve the isolation. Line 1 in Section 1 was omitted in this figure since it had no significant influence. If diodes D1 and D3 are seen as loads, then the addition of Section 3 can be seen as a change in the load. This would mean that all the design rules discussed above for Section 1 still apply.

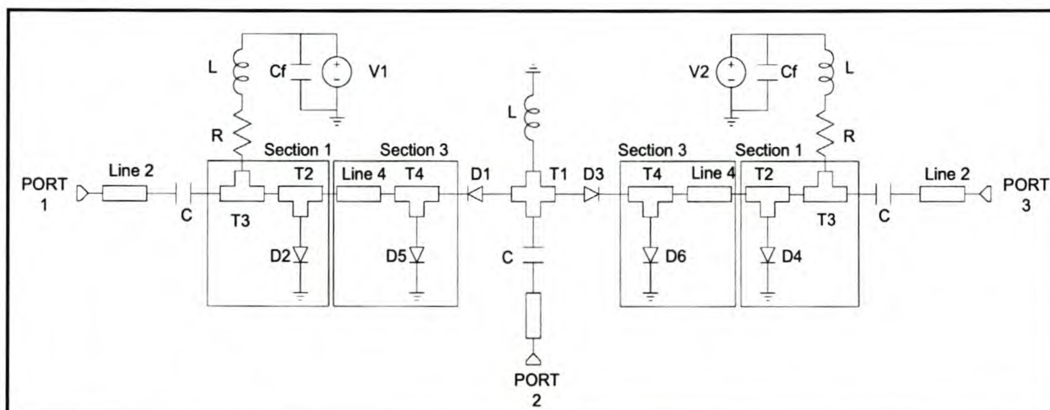

Figure 81: Schematic diagram of SPDT compound configuration switch with additional shunt diode

Junction T4 has the same influence on the switch performance as T2. It was mentioned before that junction T2 has an optimum impedance for which the isolation is a maximum. This impedance is dependant only on the shunt diode connected to the junction. Therefore, if both the shunt diodes are the same, and it can be assumed that their parasitic elements are identical, then junctions T2 and T4 should have the same geometry for optimum response. If the two shunt diodes are not the same, then junctions T2 and T4 should be tuned individually for maximum isolation.

With reference to Line 4, the same guidelines that were discussed for Line 3 applies to Line 4.

The simulated response for the switch represented in Figure 81 is shown in Figure 82. If these results are compared to those presented for the additional series diode, the following can be said: The isolation increase in both cases is similar for the ideal as well as the practical diode.

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If one looks at the insertion loss, the additional series diode provided an extra 0.9 dB of loss, whereas the shunt diode contributed to an additional 0.1 dB. The biggest advantage of the additional shunt diode above the additional series diode, is the fact that the overall return loss response is much lower for the same bandwidth and it is easier to tune the switch for a low return loss.

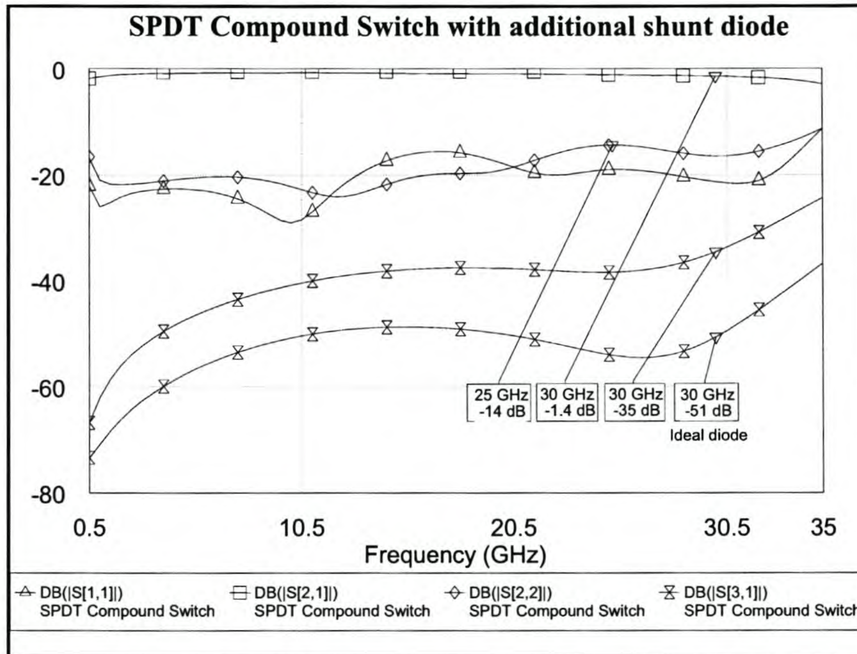

Figure 82: Simulated results for SPDT compound configuration switch with additional shunt diode

From a response point of view, if given the choice, the compound configuration with an additional shunt diode would always be the chosen configuration. It will become clear in the following sections that the type of substrate used also plays a significant role in this decision.

5.5 Hard and soft substrate technology overview

The switch design procedure on both hard and soft substrates is the same. The main difference in the design is the implementation options that are available or possible on the substrates. Different technologies are used on the two substrate types.

Hard substrate implementation is generally more advanced and sophisticated than that of soft substrates. Section 5.5.1 will point out the differences in the technologies that are available for the two substrate types.

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5.5.1 Difference in technology

The aim of this section is not to discuss all the differences in the technologies, but only those factors that are relevant to PIN diode switch design. A brief overview of the advantages and disadvantages between using the two substrate types will also be discussed.

5.5.1.1 Advantage of hard substrates

The main advantage of the hard substrate above the soft is the fact that it is physically hard. This allows for ultra-sonic bonding to be applied on the substrate, which in turn implies that components can be used in die form. Components in die form can generally be used at higher frequencies because their parasitic elements are less than conventional packaged components. Resistors, needed for biasing, are etched on the substrate and can operate at much higher frequencies than the surface mount resistors. In general, everything done on the hard substrate is physically done on a much smaller scale, and with everything being smaller, the parasitic elements are minimised. Everything is manufactured with more precision and accuracy on the hard substrate.

5.5.1.2 Disadvantage of hard substrates

A disadvantage of working with hard substrates is that more sophisticated and high technology equipment is required. The equipment is also more expensive than that needed to work with soft substrates. The hard substrate is also more brittle and fragile. This is typically a problem if the substrate is mounted on a material with a different thermal expansion coefficient. Under temperature variation, the substrate could either break of shear loose from the material it is mounted on.

5.5.1.3 Disadvantage of soft substrates

Ultra-sonic bonding can in most cases not be applied on soft substrates since the substrate compress and the track onto which the bonding is applied, could break or damage. Surface mount components are mostly used and must be soldered or epoxied onto the substrate. Because the device packaging is much larger, the parasitic elements play a more significant role and this reduces the maximum frequency at which the switch or components can operate.

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Although the PIN diodes can be bought in a smaller beam lead package, the capacitors, resistors and inductors needed for biasing and dc-decoupling, may still present a problem. Conventional packaged capacitors and inductors for instance are seldom specified to operate up to 18 GHz.

5.5.1.4 Advantage of soft substrates

The advantage of the soft substrate is that advanced technology is not required and most manufacturing can be done in-house in any facility. Surface mount components are also less expensive than those bought in die form.

5.5.2 Design differences

The previous section showed the differences in the technologies that can be implemented on the two substrate types. This section will show how these differences are relevant to the PIN diode switch design.

In PIN diode switch design, in essence only two types of diode configurations are required, a series and a shunt configuration. The heart of the design therefore lies in the quality of the connections that can be achieved on the substrate.

In the previous chapter, parameter extraction was done on the series configuration diode on soft substrate, and in both configuration types on hard substrate.

5.5.2.1 Series configuration diode

With the series configuration diode it was found that the diode performance, in terms of isolation and insertion loss, were the same on both substrate types. No substrate would in this regard be preferred over the other.

In terms of design differences, there are no real design differences between the two substrates. Both substrates would more or less offer the same results in terms of isolation and insertion loss. On the soft substrate, due to the type of packaging used, the upper frequency range of the diode and other components is likely to be the greatest limiting factor.

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5.5.2.2 Shunt configuration diode

With the shunt configuration diode on the other hand, a significant performance difference was noticed between the two substrates. The main reason for this is the different diode packaging types that can be used on the two substrates. On the hard substrate, with the die packaging, two types of shunt configurations can be constructed, whereas on the soft substrate, only one connection type is possible. With a shunt configuration diode, a good ground connection is essential to provide sufficient isolation. On the soft substrate, achieving a good ground is a problem. There is always some parasitic inductance present between the diode anode or cathode and ground. If a via, for instance, is used for a connection to ground, it still contributes to some inductive element present. The parasitic inductance and series resistance of the packaging are also present and play a significant role.

On the hard substrate, it was shown that a shunt configuration could be constructed in two ways. The first way is by splitting the track in two and placing the diode between the tracks. Bond wires are then used to connect to the tracks (see Figure 72 on page 83). The second way is by simply mounting the diode next to the track and bonding from the anode to the track (see Figure 68 on page 80). The first option is the preferred option. It is a high quality shunt connection that provides much better isolation than the second option. The response is also less frequency dependant. With the second option, you have exactly the same problem as on the soft substrate, namely the inductance going to ground.

In terms of design differences, in the case of a compound or shunt configuration switch, when designing on a hard substrate, one would definitely go for option one in the shunt diode construction. On the soft substrate, only one option is available.

5.6 Practical switch design procedure

In the previous chapters a few design guidelines for the series, shunt and compound configuration switches were discussed. In most cases, it was assumed that the components were ideal. This was done to show the design concepts of the three configuration types and give an overview on how to manipulate certain switch responses. It was also shown how to optimise the switch response for a specific requirement in terms of insertion loss, isolation and bandwidth.

When designing a practical switch, all the above-mentioned design guidelines still hold. The idea is to get the simulations to be as realistic and practical as possible. The simulation model

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should in theory be an exact representation of the switch to be built. This would reduce the number of iterations needed to achieve a final design. To do this, the known practical elements must be integrated into the design. These practical elements include the following:

1. Transmission line losses.
2. Resonances and other frequency dependant characteristics of components.
3. Practical models for diodes in their specific configurations and biasing conditions.
4. Connector and transmission line transients.
5. Parasitic elements.
6. Bond-wire inductance.
7. Cavity resonances in the housing.

All the above-mentioned elements play a role in the switch design, some more critical than others, but nevertheless, they all have to be accounted for in the design. Most manufacturers make the s-parameters for their components available to designers. These parameters can then be imported into a design package such as Microwave Office.

It was found that the s-parameters for a single component can vary when measured on different substrates with different heights and in the altered configurations. It is mostly the parasitic elements that differ. In Chapter 4 it was shown how to accurately do parameter extraction on components. Ideally, for the diodes, one would rather use extracted parameters instead of those supplied by the manufacturers. The parameter extraction has to be done on the substrate the component will be used on, as well as in the configuration and biasing conditions it will operate under. It will later be shown that this is the most accurate way to simulate the switch.

The following section will show how to design a practical switch and how to include these practical elements in the design. The switch will then be built and the measured results will be compared to those simulated.

5.6.1 Soft substrate switch design

A PIN diode switch with three diodes will be designed and built. The compound switch will be used as a "base" design and an additional series diode will be added. The idea is to achieve the optimum switch response, but more importantly, to make sure that the simulated results compare well with the measured results, and if not, to find a reason for this difference.

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The initial specifications for the switch:

1. Frequency : 2 – 18 GHz
2. Insertion loss : < 5 dB
3. Return loss : < 10 dB
4. Isolation : As best as possible

5.6.1.1 Design approach

In this section, a preferred "design approach" to design a compound configuration PIN diode switch will be considered and applied. An important fact to note is that this is only a suggested way to design a switch, and is certainly not the only way. If this suggested approach is followed systematically, the designer will be able to successfully design a switch that when built, the measured and simulated results will compare very well.

A flow diagram of the suggested design approach is shown in Figure 83. In the flow diagram, whenever it is stated to optimise the switch, the design guidelines in Section 5.4 will be applied.

The design of the switch will be done by following the steps shown in the flow diagram systematically. Each of the steps will be handled as an entity, and will be discussed in more detail in the subsequent sections.

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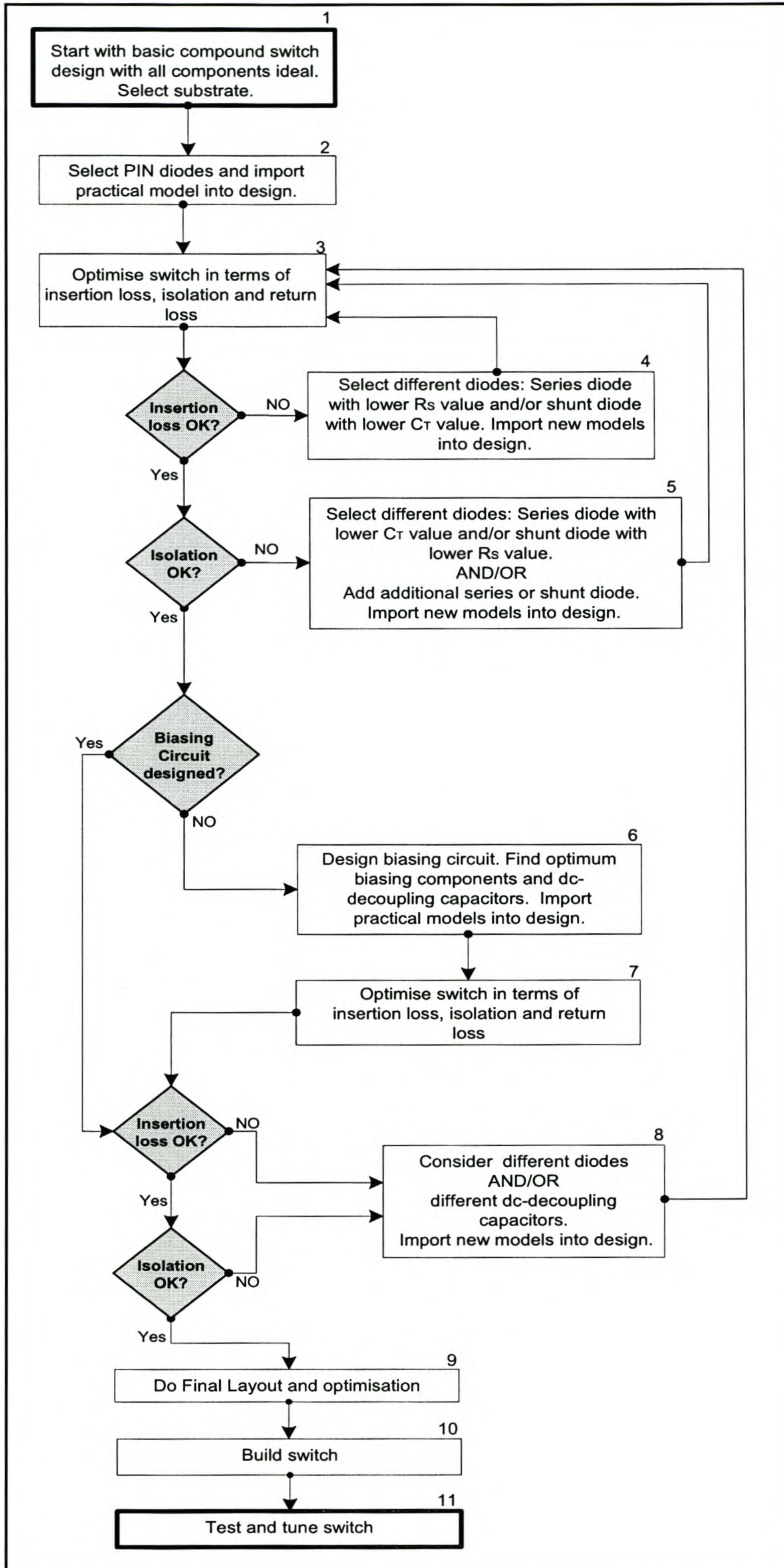

Figure 83: Flow diagram of preferred compound switch design approach

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5.6.1.1.1 Step 1: Substrate selection

When choosing a substrate, two main factors to keep in mind, are the sizes of the components that have to fit onto the transmission lines and the constraints to the guidelines in section 5.4. Another factor to consider is parasitic elements, and how they differ, due to the substrate properties.

The same substrate that was used in the previous chapters will be used for this switch. The substrate properties are listed in Table 1. The 25 mil thick substrate will be used. On this substrate, for the guidelines in section 5.4 to be valid, the maximum operating frequency of the switch must be below 30 GHz. The specified maximum operating frequency of the switch is well below 30 GHz, so the design guidelines are valid.

Figure 84 shows a schematic diagram of an ideal compound switch with an additional series diode. All elements are assumed ideal with the capacitors and inductors made infinitely large to minimise their influence on the switch response. Ideally, by design, the biasing and dc-decoupling components should not influence the switch response very much. One would therefore expect that later, when including the s-parameter models of these components into the simulations, minimal change would be needed to optimise the design again.

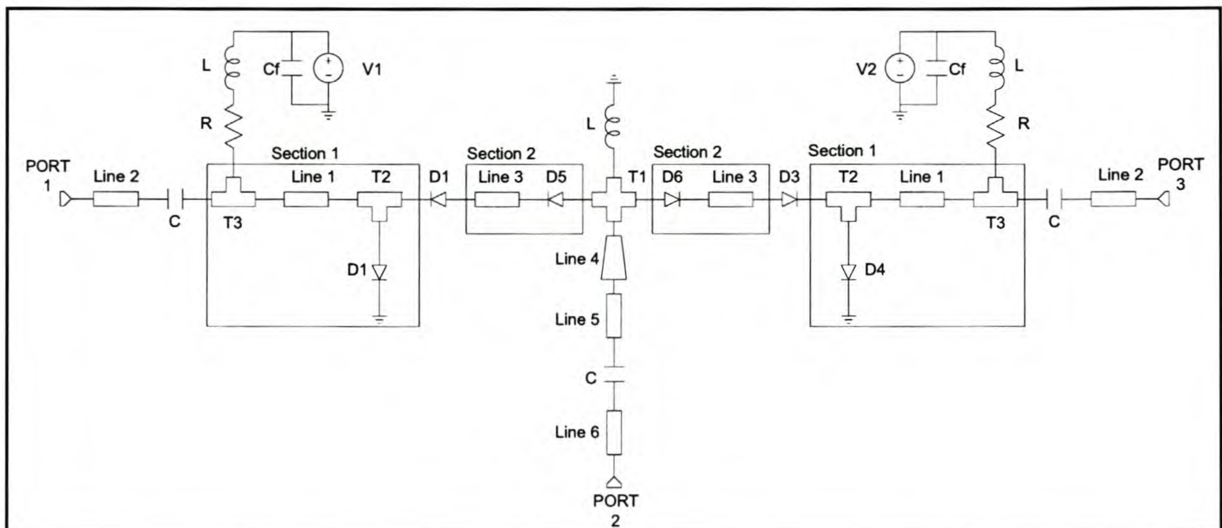

Figure 84: Schematic diagram of SPDT compound configuration switch with additional series diode

5.6.1.1.2 Step 2, 4, 5: PIN diode selection

Steps 2, 4 and 5 will be discussed together, because they all have to do with selecting the desired PIN diodes.

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The first step in choosing a diode would be to look at the packaging. One must make sure that the packaging is suitable to operate across the required bandwidth and can be mounted on the substrate. One manufacturer specified some of their packaging to operate up to 18 GHz, but when measured on the TRL kit, it was found that it could only operate up to 6 GHz. To confirm whether this poor performance was due to the diode or the packaging, that same diode was measured in a different package. It was then confirmed that it was in fact the packaging that presented the problems above 6 GHz, and not the diode.

On the soft substrate, only the beam-lead packaging was found suitable to operate up to 18 GHz and will be used in the design.

- **PIN diode selection:**

  Now that the packaging was decided on, the next step would be to look at the diode properties. PIN diodes are mostly specified in terms of junction capacitance (C_j), series resistance (R_S), switching time or "minority carrier lifetime" and breakdown voltage. When selecting a diode, one usually has to make some trade-off between these parameters since they are all in some way related to each other (see chapter 2).

  With a PIN diode one could roughly say that the junction capacitance and the series resistance are inverse proportional to each other, or in other words, a diode with a lower R_s would typically have a higher C_j and vice versa. This information becomes relevant when selecting the specific diodes for the shunt and series configurations.

  When selecting the diodes, the main factors to take into account are the switch isolation, insertion loss and switching time specifications. Equation 5.1 shows the formula for calculating the insertion loss of the compound switch with no additional series of shunt diode. Knowing that R_s (typical value 3 Ω) is the series resistance of the forward biased series diode and C_j (typical value 0.05 pF) is the reverse biased junction capacitance of the shunt diode, one can see that the series diode has the greater influence on the insertion loss. To minimise the insertion loss, the obvious choice would be to choose a series diode with R_s as low as possible.

  If at a later stage the isolation specification of the switch is not met, with reference to the series diode, the designer can improve the isolation by either selecting a series diode with a smaller C_j value, or add an additional diode. In both cases however, the insertion loss will also increase. Based on the application and other design constraints that might exist, it is up to the designer to decide which option would be the best. A design constraint might for

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instance be the size available in a housing or additional cost involved by adding another diode.

Equation 5.2 shows the formula for calculating the isolation. Here both the series and the shunt diode play a major role in providing sufficient isolation. With the series diodes chosen, for maximum isolation, the shunt diode has to be chosen with R_s as small as possible.

The minority carrier lifetime also has to be taken into account when selecting a diode, for this determines the lowest operating frequency of the switch. Refer to the discussion in section 2.1.1 on how the minority carrier lifetime influences the operating frequency and which diode to select in this regard.

The switching speed is also usually one of the switch specifications. When selecting the diodes, care has to be taken to make sure that the selected diodes can at least switch within this specification.

- **Selected PIN diode:**

The HPND-4028 and the HPND-4005 diodes both have very attractive properties and will be considered for the switch. The HPND-4028 has a very low series resistance (2.3 Ω) and a very fast switching speed. The HPND-4005 on the other hand has a very low junction capacitance (0.017 pF), which is favourable for the isolation. From the datasheets, the HPND-4005 has a flatter response from 2-18 GHz than the HPND-4028. The insertion loss specification of the HPND-4028 seems to deteriorate above 10 GHz whereas with the HPND-4005, this is not the case.

The HPND-4005 PIN diode will be used for both the series and shunt diodes. The diode properties are listed in Table 16. The main reasons for choosing this diode are:

- With the beam-lead packaging the diode can be mounted on the soft substrate.
- It has a flat response up to 18 GHz.
- Since two series diodes will be used, the lower junction capacitance will contribute significantly to the switch isolation.

In terms of switch performance, this diode is perhaps not the best option. As mentioned before, the establishment of a design procedure/approach is more important here than meeting specific switch specifications. The main idea is to make sure that the simulations

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and the measurements correlate well with each other. The HPND-4005 looks like a "safer" option in terms of broadband response than the HPND-4028.

Part number	Lp (nH)	Cp (pF)	R(Ω)	R_s (Ω)	C_j (pF)
HPND-4005 (Measured)	0.2	0.021	2.5	6.5	0.017
HPND-4005 (Specified by HP)	0	0	0	6.5(max)	0.017(typ)

Table 16: Extracted and specified parameters of the HPND-4005 PIN diode

At the time the switch was designed, it was not yet possible to measure the diode properties. The design of the TRL kit and the switch were done in parallel. Only after the switch was built, the practical diode properties could be measured. Therefore, at this point, the parameters specified by the manufacturer will be used and imported into the simulations.

When using parameters as specified by the manufacturers, an important fact to note is that some manufacturers specify the parameters as measured on a specific substrate, while others specify them as measured on the wafer. The first option would be most accurate since it already includes some parasitic elements.

5.6.1.1.3 Step 3: Optimisation

In this section the standard compound switch will be optimised in terms of insertion loss, isolation and return loss across the band 2-18 GHz. The guidelines in section 0 will be followed to optimise the switch. The schematic used for simulating the switch, is shown in Figure 84. Section 2 in the schematic is omitted at this time.

- **Initial simulation setup**

  As mentioned previously, the parameters specified by the manufacturers will be used in the simulations. No parasitic inductance is specified by the manufacturer, but knowing it is present, a 0.2 nH series inductance (L_P) will be added to the diode model. The linear diode model that will be used in the simulations is shown in Figure 85 below.

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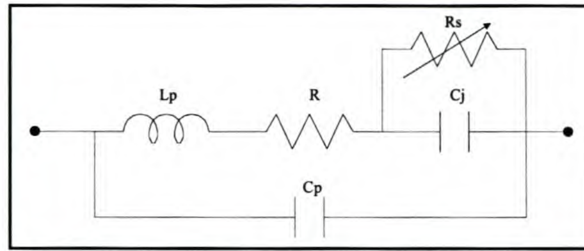

Figure 85: Linear model of PIN diode used in simulations

On the soft substrate, surface mount capacitors and wire wound inductors will be used. This automatically sets a few design constraints beforehand, and they have to be taken into account during the design process. The constraints are:

1. The capacitors have to be soldered onto the transmission lines so there has to be physically enough space for the capacitor and the solder flow. All the transmission lines that connect to the capacitors therefore have to be at least the same width as the capacitor.
2. The RF chokes/inductors have to be epoxied onto the transmission lines, so there must be enough space for the epoxy as well as for the inductor "end-wire".
3. The PIN diode leads are 0.22 mm long and 0.11 mm wide. Again, there must be enough space for the leads as well as the epoxy.

The above-mentioned constraints automatically set the minimum lengths and widths of certain transmission lines in the circuit shown in Figure 84.

The switch is required to operate from 2-18 GHz. To start with, all the transmission lines are set up to have 50 Ω impedance at the center frequency (10 GHz) of the band. The line lengths can initially be set to any value, but must be longer than the width of the lines. A 50 Ω impedance line at 10 GHz is 0.62 mm wide. It was decided to make all the lines 1.2 mm in length.

In the simulations, the frequency range will be set to 0.5-19 GHz, to evaluate the "out-of-band" performance. Usually during the manufacturing process, there are some tolerances and then the "out-of-band" response can become "in-band".

- **Setting up T1**

When simulated, the initial switch response looked reasonable. The grey traces in Figure 86 show the initial simulation results. The return loss is the only parameter that does not look good across the band.

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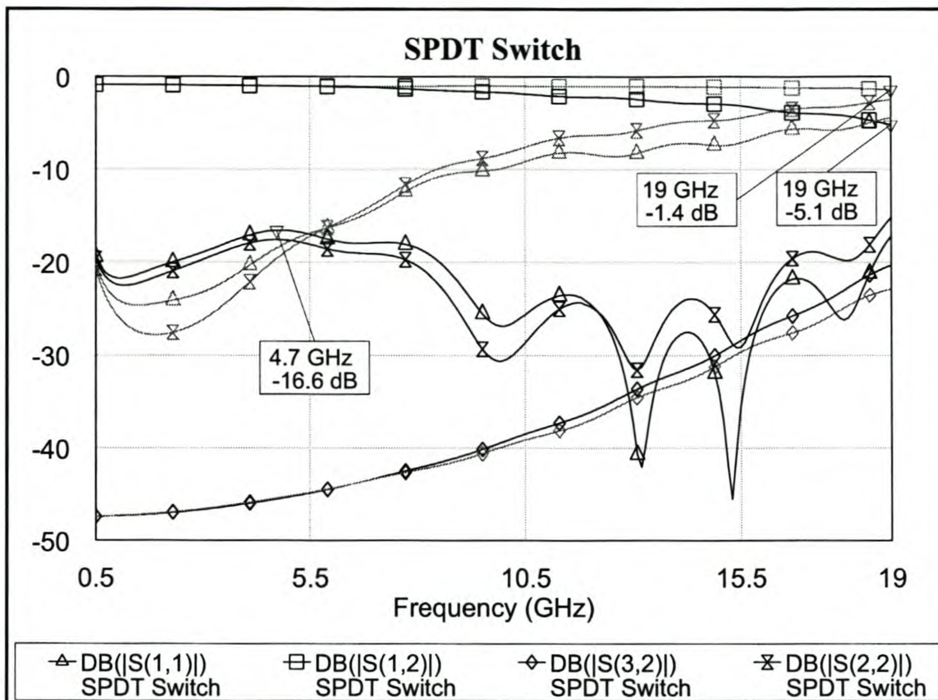

Figure 86: Results of the SPDT switch with junction T1 changed to 0.5 × 0.5mm

This response was expected since junction T1, setup as a rectangle, is much too long and too wide according to the guidelines in section 0. Knowing that at least three components (2 diodes, 1 RF choke) need to interconnect at this junction, and keeping the size of the components in mind, the junction was then changed to be 0.5 × 0.5 mm.

The results of the circuit with T1 changed is shown as the black traces in Figure 86. By only changing the dimensions of T1, the bandwidth increased tremendously and the insertion loss improved as well. The isolation was not affected much.

- **Setting up Section 1**

Even though the overall response looks very good, the geometry of the line and junctions in Section 1 were changed to try to flatten the return loss response on ports 1 and 2 and to improve the isolation. The switch response, after the changes had been made, is shown in Figure 87. The black traces show the response after mentioned circuit changes. The return loss on both ports 1 and 2 is below -20 dB and the isolation increased with 3 dB.

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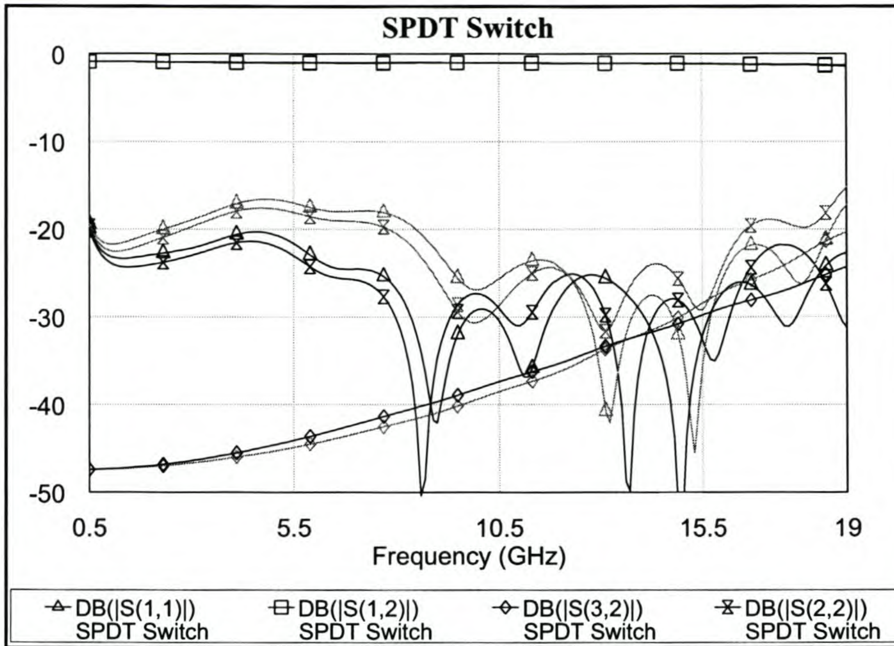

Figure 87: Switch response after changes made in Section 1

The transmission line lengths and widths in Section 1 that were changed, are listed in Table 17. All the lines not listed in the table were unchanged and is therefore still 1.2 × 0.62 mm. Line 4 is a tapered line with the end widths equal to the widths of the adjacent lines. From Table 17 it can be seen that junction T2 has a width of 0.7 mm. In theory the width should be 0.4 mm to produce more isolation (4 dB extra). It was chosen to be 0.7 mm because of the accuracy with which the transmission lines can be etched in-house. Because of this manufacturing constraint, the suggestion is to try to avoid big steps in the widths of successive transmission lines. The in-house manufacturing will later be discussed in more detail.

Description	Length (mm)	Width
T1	0.5	0.5
T2	0.4	0.6
Line 1	1	0.8
T3	1.8	0.75

Table 17: Transmission line lengths to produce results shown in Figure 87.
All lines not listed in the table remain unchanged.

At this stage, not too much time were spent in optimising the design. All lines will most probably have to be altered when adding the additional diode and the other component s-

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parameter models. The designer should develop a good idea on how the switch response reacts to certain changes in the circuit schematics. This knowledge should then make it easier and faster for the designer to manipulate the switch response later when needed.

5.6.1.1.4 Step 4: Insertion loss check

The insertion loss is well within the specifications, so the next step would be to look at the isolation.

5.6.1.1.5 Step 5: Isolation check

Even though the isolation was not a specific specification, an additional diode will be added to show how it influences the switch response and the optimisation process. In this section, the additional series diode is included in the circuit diagram and the switch is optimised for best overall performance. With the diode added, Step 3 is therefore implemented again to optimise the switch.

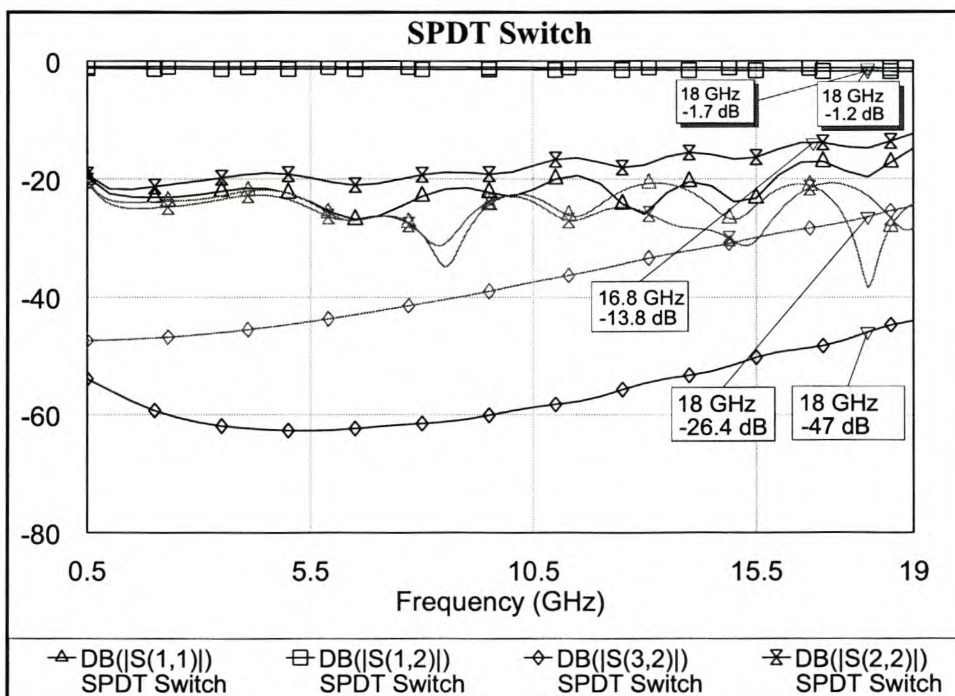

Figure 88: Switch results with additional diode added

Figure 88 shows the response of the switch with, and without the additional diode. The black traces show the response of the switch with the additional diode. One can see that the return loss has deteriorated considerably, but the isolation increased significantly with about 20 dB.

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During the optimisation process, a trade-off had to be made between return loss and the isolation. The isolation could be improved, but at the expense of return loss, and vice versa. Knowing that the return loss could possibly deteriorate even more when the connectors are added to the circuit, it was decided to leave some margin for error with the return loss.

The new line lengths and widths of the circuit are listed in Table 18. Only minor adjustments were made to the lines in Section 1. It was mostly the line widths that needed to be adjusted, not the lengths. This makes it easier for the designer because the variables used for optimisation are in fact halved. The length of Line 3 is λ/4 at 18 GHz and has an impedance of 44 Ω at 10 GHz. This agrees with the guidelines in section 5.4.2.

Description	Length (mm)	Width
T1	0.5	0.5
T2	0.4	0.6
Line 1	1	0.6
Line 3	1.5	0.8
T3	1.8	0.7

Table 18: Transmission line lengths to produce results shown in Figure 88. All lines not listed in the table remain unchanged.

With the insertion loss and isolation within the specifications, the optimum dc-decoupling capacitors must be included and the biasing circuit designed.

5.6.1.1.6 Step 6: DC-decoupling capacitors and biasing circuit design

The first step is to find suitable components that can be mounted on the soft substrate and operate up to 18 GHz.

- **Find components to be used**
  For the biasing circuit, no chip or surface mount inductors could be found that can operate up to 18 GHz without having some resonance in the operating frequency band. The wire-wound inductors, usually used on the hard substrates, were the only inductors that could be found that could operate up to 18 GHz without any problems. They will be mounted onto the tracks with conductive epoxy. No s-parameter model could be found for this inductor. This is however not too much of a problem because once mounted on the track, they can be tuned by tweaking them. If there are then any resonances, resulting from the inductor, they

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can be tuned to be out of band. For the inductor, the ideal inductor model with a value of 20 nH will be used in the simulations.

Only one capacitor could be found that is suitable to operate up to 18 GHz without any resonances in the band, the "broadband dc block" (*CO8BLBB1X5UX*) from *DI-Labs*. This capacitor will be used for dc-decoupling as well as the biasing circuit. The s-parameters for the capacitors were downloaded from the manufacturer's website and will be used in the simulations.

- **Design biasing circuit**

  Because the switch is broadband, few biasing options are available. When designing a biasing circuit, it has to be designed so that it presents a high input impedance into the biasing circuit at the interconnect between the RF path and the biasing circuit. This has to be achieved across the complete operating band in order to minimise the influence of the biasing circuit on the RF circuit. To accomplish this, the inductor has to be mounted as close as possible to the transmission line, junction T3 in this case. This will ensure that the inductor sets the input impedance to the biasing circuit.

  One would ideally want the inductor to present an impedance of 10 times Z_0 at the lowest operating frequency. The 20 nH inductor will present a 250 Ω impedance at 2 GHz. Even though this is lower than the wanted 500 Ω, the impedance is still acceptable for the design.

- **Influence of biasing circuit and non-ideal dc-decoupling capacitor**

  Figure 89 shows the switch response with the capacitor and inductor models replaced as discussed above. The grey traces show the switch response with the ideal components (same as in previous section) and the black traces show the response with the non-ideal components. The transmission lines were unchanged.

  The non-ideal components therefore influence the switch response significantly. It can now be seen why it is so important to include the practical models of the components that are used. With the dc-decoupling capacitors for instance, it was expected that they would have minimal contribution to the insertion loss, but in fact, they contribute to an additional 3 dB of insertion loss at 18 GHz, more than the 1.7 dB contribution of the diodes. The more realistic inductor value of 20 nH, instead of the previously assumed infinitely large inductance, also has a great influence on the lower frequencies.

  Since the predicted insertion loss and isolation are within the specifications, the optimisation and final layout of the switch will be done together in one step.

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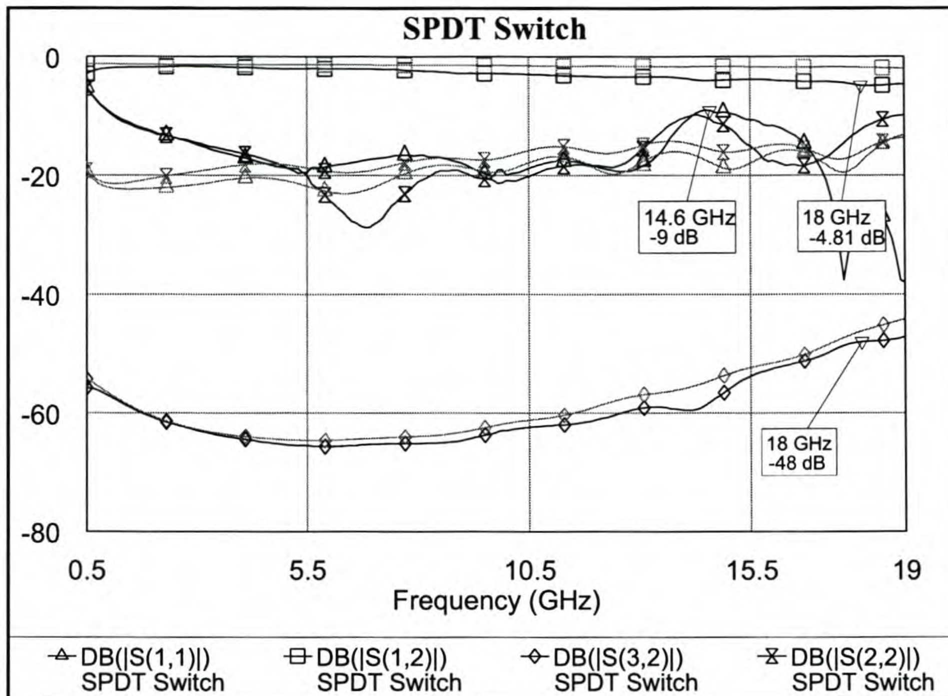

Figure 89: Simulation results for switch where ideal capacitors and inductors models are replaced with non-ideal capacitors and inductors models

5.6.1.1.7 Step 7, 9: Final optimisation and layout

With all the practical components and component values now included in the simulation, the switch was optimised and the layout finalized. Since the design is not for a specific application, the layout is fairly simple.

To make sure no high order modes could propagate on the lines, the feeding lines on the RF ports were made longer than required. Even though this increases the insertion loss, as previously mentioned, the idea from the start was not to design a perfect switch, but rather to have a simulation that represents a practical switch as close as possible.

While optimising the switch and doing the final layout, from a practical and manufacturing point of view, some concerns were raised and had to be addressed. The accuracy with which the transmission lines can be etched in-house was one of the major issues. The issue was not so much the accuracy of the line lengths, but more the transitions between connecting lines with different widths (see section 1 in Figure 84). During the etching process, some of the transitions are "automatically" tapered. This phenomenon is not desired, and can be a possible problem. For this reason, where possible, the widths of connecting lines were kept the same or the width changes were kept as small as possible.

To make sure that there were enough physical space to add the dc-decoupling capacitors connecting to junction T3, an extra line was added between junction T3 and the capacitor.

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From here on forward, that line will be referred to as "Line 7". This line also made the return loss less sensitive to variation of the parasitic series inductance in the diode model.

In the simulations, the parasitic series inductance in the diode model was varied between 0.1 nH and 0.2 nH to see what the influence on the switch response would be. Since this inductance is also included in the shunt diode model, as expected, the variation in the inductance mainly influenced the isolation. The return loss was also influenced, but it was still below -11 dB.

The schematic of the final optimised switch is shown in Figure 90. In the biasing circuit, all the bends have a radius of 2 mm and has the same width of the adjacent lines. The transmission line indicated "pad" is setup as a 2 × 2 mm rectangular pad where the actual biasing resistor and will be soldered on. The transmission line lengths and widths of the schematic are listed in Table 19. The length of line 3 was changed to compensate for the influence of the dc-decoupling capacitors on the return loss and is therefore now not setup for optimum isolation as specified in the design guidelines. Most of the other changes were made to the line impedances, and not the line lengths. This makes perfectly sense since the line impedances mostly influences the matching at the RF ports.

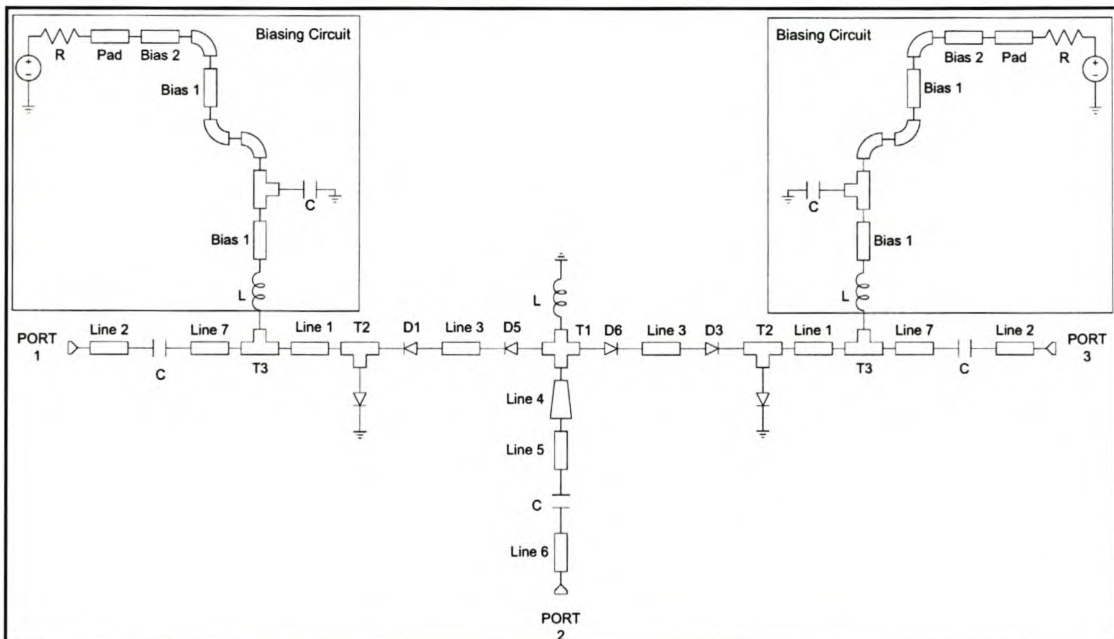

Figure 90: Schematic of final optimised switch

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Description	Length (mm)	Width
T1	0.5	0.50
T2	0.4	0.70
T3	1.3	0.80
Line 1	1.8	0.70
Line 2	15	0.72
Line 3	0.4	0.8
Line 4	1	0.5 & 0.76
Line 5 & 6	10	0.76
Line 7	1	0.72
Bias 1	4	0.6
Bias 2	12	0.6
Pad	2	2

Table 19: Transmission line lengths and widths for final optimised switch

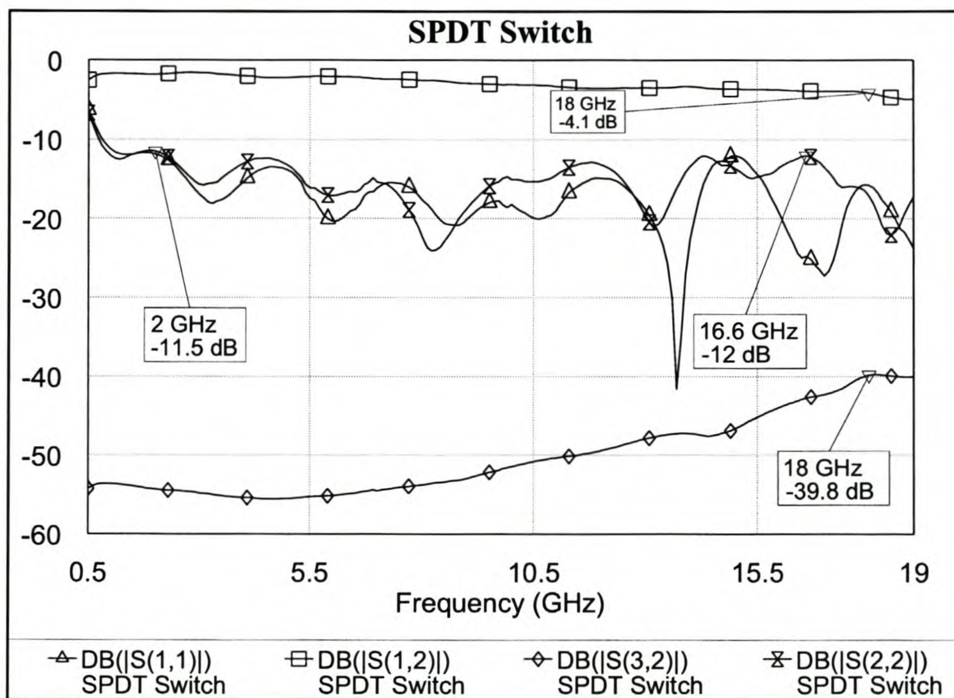

Figure 91: Simulated response of final optimised switch

Figure 91 shows the response of the optimised switch. If the diode model used in the simulations is correct, and no problems occur during the manufacturing process, then in theory, in MWO, the proposed simulation model for the switch is the best practical simulation of the switch to be built. Overall, the response looks very good. The return loss is better than -11.5

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dB across the whole band and the isolation better than 39 dB. The transitions from the connectors to the transmission lines are not simulated and it is expected that it could bring the return loss down to about -10 dB.

Figure 92 shows the final layout of the switch. In the circuit layout, all the lines connecting to junction T1 were laid out perpendicular to each other in order to reduce the coupling between the transmission lines. The ground planes for the biasing capacitors and the shunt diodes are also shown in the layout. The ground planes are manufactured by etching a patch on the substrate and then punching a "shaft" through the substrate into the housing underneath. The idea was to create a very good ground as well as keep the substrate tight on the housing floor. The funny shapes of the "ground planes" were to try and keep away from the transmission lines so that they do not lose their transmission line properties at the higher frequencies.

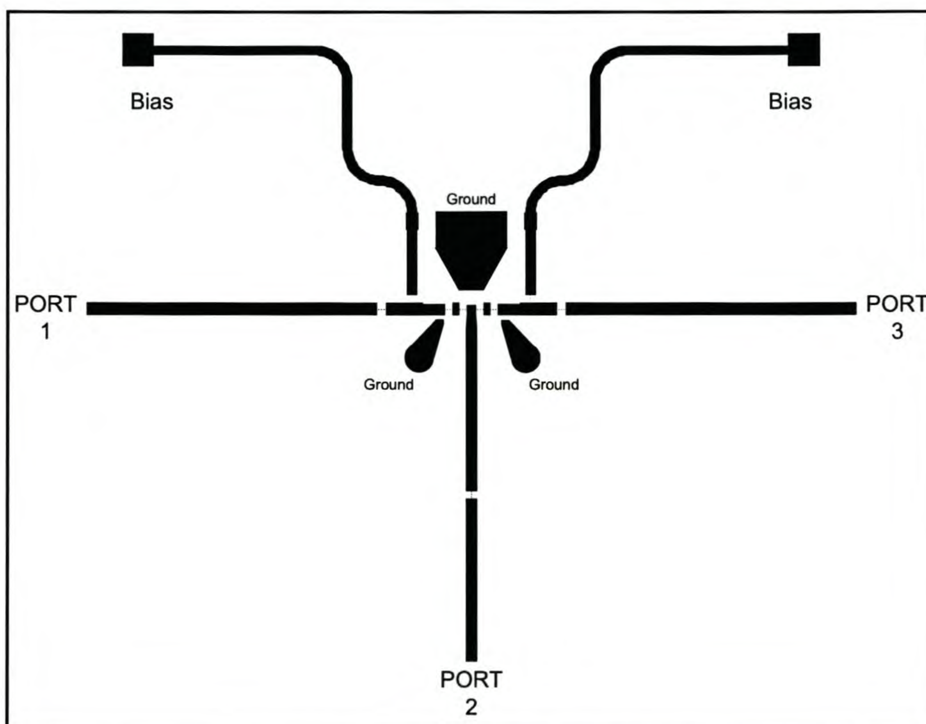

Figure 92: Final layout of switch

The next section will discuss the issues around the manufacturing of the switch.

5.6.1.1.8 Manufacturing of the switch

The layout of the switch was shown in the previous section. The substrate was etched in-house at the university facilities. Figure 93 shows a photograph taken of the etched substrate under

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the microscope. In the photograph junction T1, the PIN diodes and the bias RF choke can clearly be seen.

As indicated on the photograph, one can see that some of the corners were "rounded" during the etching process. This might produce problems, but hopefully the influence would be minimal.

After the substrate was etched, the housing was machined and the substrate epoxied onto the housing with conductive epoxy. The "ground shafts" were then inserted at the ground planes. After insertion them, their impedance from the ground plane to the housing were measured with a multi meter to get an idea of how good the connection to ground is. It had a value of 0.1 Ω. The components were then mounted onto the substrate with the inductive epoxy and put into the oven to harden.

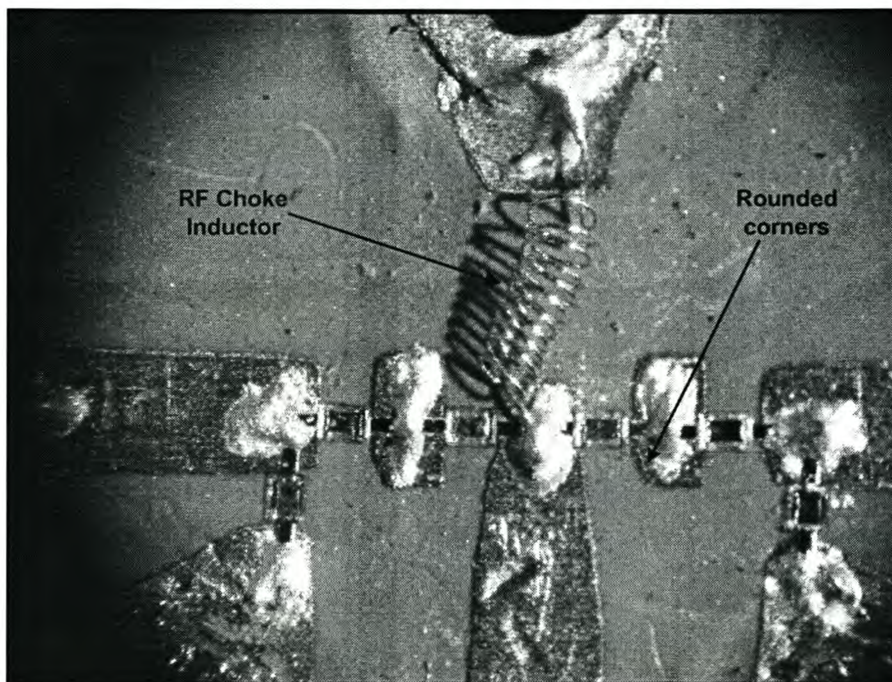

Figure 93: Photograph taken of etched substrate

After taking the switch from the oven, the impedance to ground were measured again. This time the impedance was measured to be 1.8 Ω. It was also noticed that the shafts were loose and lifted out above the substrate. They could physically be turned around. This probably resulted from a different heat expansion coefficient. Realising this is a problem, and trying to get a good ground, the shafts were punched into the housing a bit deeper. This partially solved the problem because in time, the shafts lifted again.

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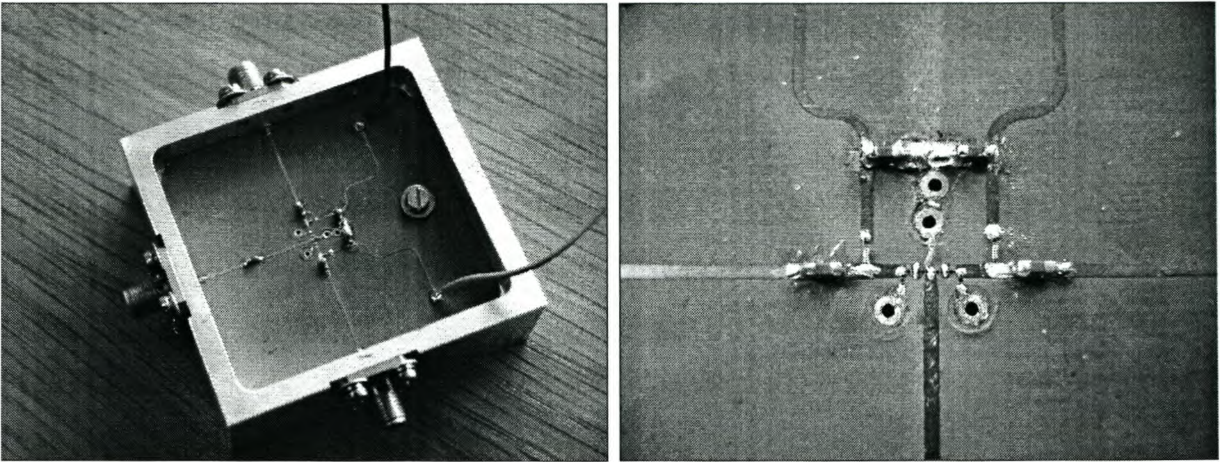

Figure 94: Photographs of final constructed switch

Figure 94 shows two photographs taken of the final switch that was built.

The measurement results will be discussed in the next chapter.

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6 Results

In this chapter, the measured results of the switch will be discussed and where possible, explanations will be given if the simulated and measured results differ.

The switch was built and measured on a HP8510 vector network analyser. For the measurements, the switch was forward biased with 37 mA and reverse biased with -15 V. The parameter extraction on the HPND-4005 was performed under these same biasing conditions. The measured results, after "tweaking" the RF choke, are shown in Figure 95. One can see that the results are quite different from what was expected. The next step now would be to try to find a valid reason for the difference.

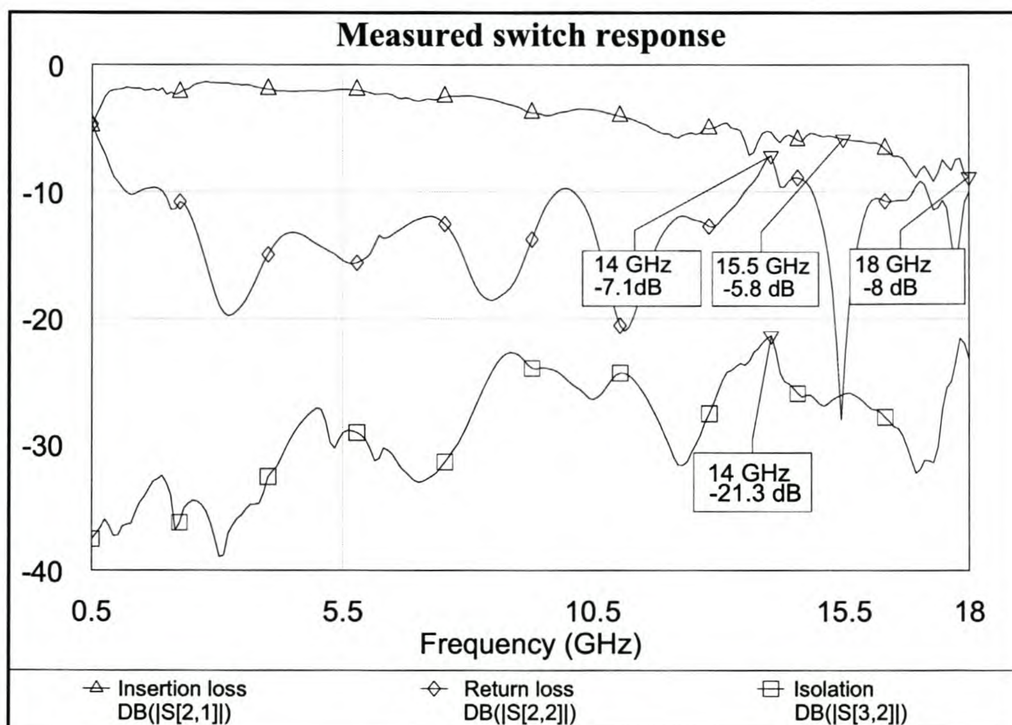

Figure 95: Measured response of the switch

In the previous chapter it was shown how significant influence the s-parameters of the dc-decoupling capacitors had on the switch response. It is expected that if the measured s-parameters of the diodes are included in the simulation, it would have the same influence in the switch parameters. The first step in "debugging" would therefore be to look at the diodes.

The whole of Chapter 4 was devoted to device characterization. In section 4.6.1, the exact parameters of the HPND-4005 diode in both the forward and reverse biased state was

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successfully extracted. The measured s-parameters are therefore available, and can be imported into the simulation.

With the practical diode s-parameters now included, the simulation compared amazingly well to the measured parameters. The measured and new simulated isolation and insertion loss are shown in Figure 96. On average, the two isolation traces compare very well. The reason for the fluctuations in the measured isolation is not clear and there is no way to account for it in the simulation. The insertion loss curves also compares very well.

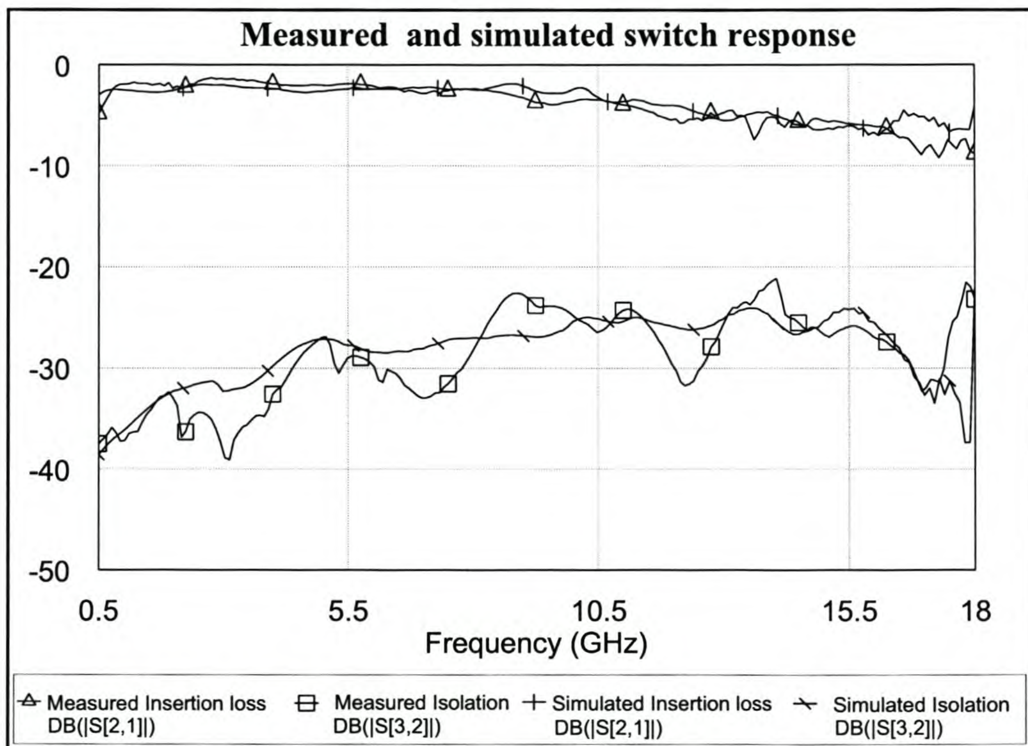

Figure 96: Measured and simulated isolation and insertion loss of the switch

The return loss on both the ports is the only parameter that does not compare to the measured values. An exact reason for this difference is not known, but a good estimation would be the connector transitions. These transitions could not be included into the simulations. Figure 97 shows the measured and simulated return loss. Although the curves differ very much, one can only see that they have the same trend and the same maximum value of -6.2 dB. It was later noticed that the substrate was shearing loose from the housing. By applying pressure on the substrate to attain a better ground, the return loss could be improved with 1 dB.

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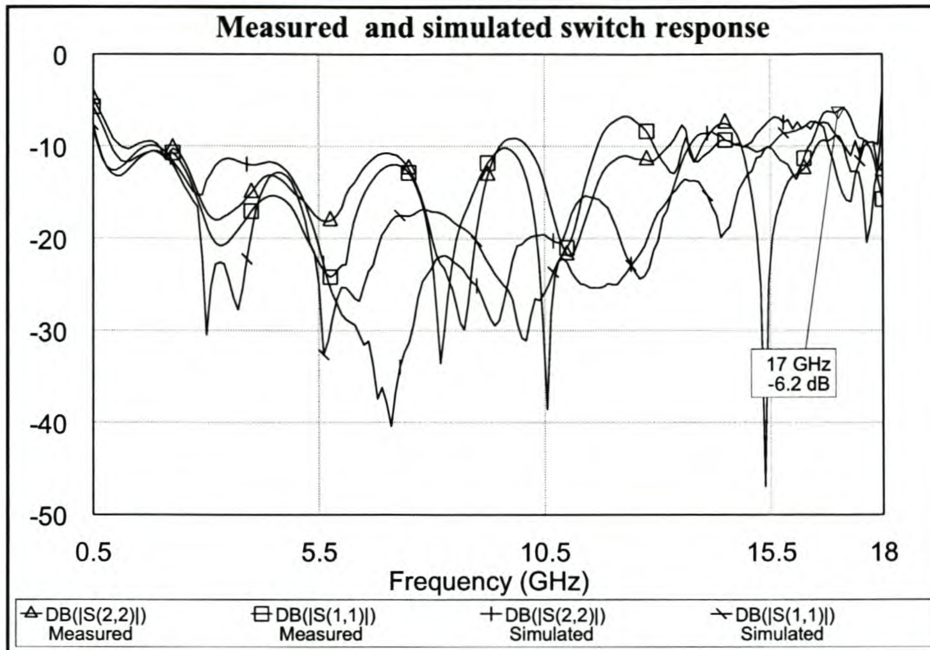

Figure 97: Measured and simulated return loss of switch

To conclude this chapter, it was seen that the actual diode properties played a significant role in the switch design. Once the proper or "complete" diode models were imported into the simulations, the simulated and measured results compared remarkably well. It is therefore proven that one cannot only rely on the data from the manufacturer's datasheet. It is to the designer's advantage to rather use measured parameters of the diodes and other components in order to have accurate simulations and save time.

The measured switch results were not as good as expected. The reason for this was the lack of a proper diode model at the time the design was done. It was shown that when the proper diode model were used, the simulations correlated very well to the measured results. In Chapter 4 it was shown how to do accurate parameter extraction on a diode. Based on the fact that an accurate diode model can now be extracted, it is believed with much confidence that if a second iteration switch is designed, it will meet the design specifications, and the simulated results will be comparable with the measured results.

The goal was to set up a simulation that would represent a practical switch as close a possible. This goal was definitely achieved and it was shown how to systematically accomplish it.

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7 Conclusion

The aim of this thesis was to present an analysis and design procedure for a broadband PIN diode switch, and equip a designer with a set of "design tools" to successfully design a switch that when built, the measured and simulated results should compare very well. This goal was definitely achieved.

A design procedure for the series, shunt and compound configuration switches were illustrated and it was shown how to include all the practical elements into the design. A TRL calibration kit was successfully designed to ensure that the designer could extract the exact models of the components to be used.

A compound configuration switch was designed and built. The switch was designed without a practical model known for the diodes. When the switch response were measured, it did not compare to the expected simulated values. After however extracting the model for the diode used, and importing the model into the design, the measured results compared remarkably well to that simulated.

The designer is therefore now equipped to successfully design a broadband PIN diode switch and produce measured results that resemble the simulated results.

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Derivation of the Insertion loss equation for a SPST series configuration switch

The equation for calculation the insertion loss for a SPST series configuration switch can be derived as follows:

$$\text{Insertion Loss} = \text{- Gain} = 20 \text{ Log } \left(1/S_{21}\right) \quad [dB] \qquad 1.1$$

The ABCD parameters for a series impedance are [11]:

$$A = 1$$
$$B = Z$$
$$C = 0$$
$$D = 1$$

S_{21} can be derived from the ABCD parameters [11]:

$$S_{21} = \frac{2}{A + B/Z_0 + CZ_0 + D} \qquad 1.2$$

$$\therefore \quad S_{21} = \frac{1}{1 + Z/2Z_0} \qquad 1.3$$

By combining equations 1.1 and 1.3, equation 1.4 gives the insertion loss for a SPST PIN diode switch.

$$\textit{Insertion loss} = 20\log_{10}\left[1 + Z/2Z_0\right] \quad [dB] \qquad 1.4$$

where Z = diode series impedance

Z_0 = microstrip characteristic impedance

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If an ideal PIN diode is used, Z is equal to R_s and then equation 1.4 becomes:

$$Insertion\,loss = 20\log_{10}\left[1 + R_s/2Z_0\right] \quad [dB] \qquad 1.5$$

where R_s is the forward biased RF resistance of the PIN diode.

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Derivation of the Isolation for a SPST series configuration switch

The equation for calculation the isolation for the SPST series configuration switch is shown in equation 1.6:

$$\text{Isolation} = -\text{ Gain} = 20 \text{ Log } \left(1/S_{21}\right) \quad [dB] \qquad 1.6$$

To solve equation 1.6, S_{21} for a series impedance is required. S_{21} for a series impedance was already derived in equation 1.3 and is shown again in equation 1.7:

$$\begin{aligned} S_{21} &= \frac{2}{2+Z/Z_0} \\ &= \frac{1}{1+Z/2Z_0} \end{aligned} \qquad 1.7$$

If Z in equation 1.7 is replaced with $Z = 1/j2\pi fC$, the impedance of the reverse biased diode, then:

$$Isolation = 10\log_{10}\left[1+1/\left(4\pi fCZ_0\right)^2\right] \quad [dB] \qquad 1.8$$

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Derivation of the Insertion loss equation for the SPST shunt configuration switch

The equation for calculation the insertion loss for a SPST shunt configuration switch can be derived as follows:

$$\text{Insertion Loss} = -\text{Gain} = 20\ \text{Log}\ \left(1/S_{21}\right) \quad [dB] \tag{1.9}$$

The ABCD parameters for a shunt impedance are [11]:

$$A = 1$$
$$B = 0$$
$$C = 1/Z$$
$$D = 1$$

S_{21} is then derived from the ABCD parameters [11]:

$$S_{21} = \frac{2}{A + B/Z_0 + CZ_0 + D} \tag{1.10}$$

$$\therefore \quad S_{21} = \frac{2}{2 + Z_0/Z} \tag{1.11}$$

By combining equations 1.9 and 1.11, equation 3.12 gives the insertion loss for a SPST shunt connected switch.

$$IL = 20\log_{10}\left[1 + \frac{Z_0}{2Z}\right] \quad [dB] \tag{1.12}$$

where Z = diode impedance

Z_0 = microstrip characteristic impedance

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If an ideal PIN diode with a reverse bias impedance of $Z = 1/j2fC_j$ is used, then:

$$IL = 10\log_{10}\left[1 + \left(\pi f C_j Z_0\right)^2\right] \quad [dB] \tag{1.13}$$

where C_j = reverse bias junction capacitance of the diode

f = frequency in Hz

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Derivation of the Isolation equation for the SPST shunt configuration switch

The equation for calculation the isolation for the SPST shunt configuration switch is shown in equation 1.14:

$$\text{Isolation} = -\text{Gain} = 20\ \text{Log}\left(1/S_{21}\right) \quad [dB] \qquad 1.14$$

S_{21} for a shunt impedance is:

$$S_{21} = \frac{2}{2 + Z_0/Z} \qquad 1.15$$

If an ideal diode is used, Z in equation 1.15 is replaced with $Z = R_s$ then

$$Isolation = 20\log_{10}\left[1 + \frac{Z_0}{2R_s}\right] \quad [dB] \qquad 1.16$$

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HPND-4005 Datasheet

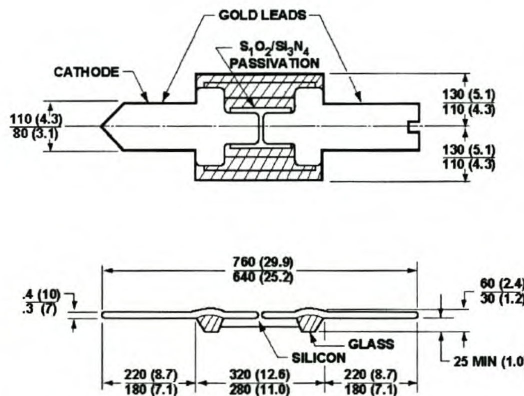
Beam Lead PIN Diode

Technical Data

HPND-4005

Features

- **High Breakdown Voltage 120 V Typical**
- **Low Capacitance 0.017 pF Typical**
- **Low Resistance 4.7 Ω Typical**
- **Rugged Construction 4 Grams Minimum Lead Pull**
- **Nitride Passivated**



Outline 21

Description

The HPND-4005 planar beam lead PIN diode is constructed to offer exceptional lead strength while achieving excellent electrical performance at high frequencies. High beam strength offers users superior assembly yield, while extremely low capacitance allows high isolation to be realized.

Nitride passivation and polyimide coating provide reliable device protection.

Applications

The HPND-4005 beam lead PIN diode is designed for use in stripline or microstrip circuits. Applications include switching, attenuating, phase shifting, limiting, and modulating at microwave frequencies. The extremely low capacitance of the HPND-4005 makes it ideal for circuits requiring high isolation in a series diode configuration.

Maximum Ratings

Operating Temperature .... -65°C to +175°C
Storage Temperature .... -65°C to +200°C
Power Dissipation at T_{CASE} = 25°C .... 250 mW
(Derate linearly to zero at 175°C.)
Minimum Lead Strength .... 4 grams pull on either lead
Diode Mounting Temperature .... 220°C for 10 sec. max.

2

Electrical Specifications at $T_A = 25°C$

Part Number HPND-	Breakdown Voltage V_{BR} (V)		Series Resistance R_S (Ω)[2]		Capacitance C_T (pF)[1,2]		Forward Voltage V_F (V)	Reverse Current I_R (nA)	Minority Carrier Lifetime τ (ns)[2]	
	Min.	**Typ.**	**Typ.**	**Max.**	**Typ.**	**Max.**	**Max.**	**Max.**	**Min.**	**Typ.**
4005	100	120	4.7	6.5	0.017	0.02	1.0	100	50	100
Test Conditions	$I_R = 10$ mA		$I_F = 20$ mA, $I_F = 100$ MHz		$V_R = 10$ V, f = 10 GHz		$I_F = 20$ mA	$V_R = 30$ V	$I_F = 10$ mA, $I_R = 6$ mA	

Notes:
1. Total capacitance calculated from measured isolation value in a series configuration.
2. Test performed on packaged samples.

Typical Parameters

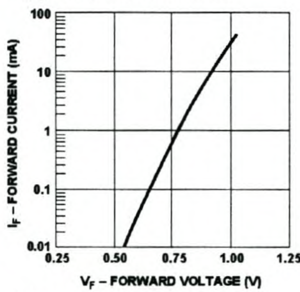


Figure 1. Typical Forward Conduction Characteristics.

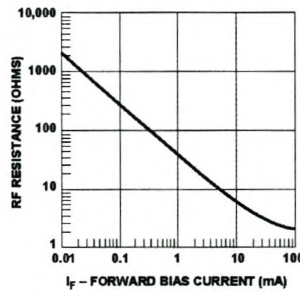


Figure 2. Typical RF Resistance vs. Forward Bias Current.

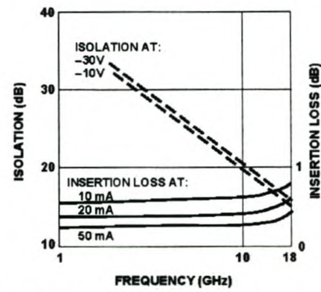


Figure 3. Typical Isolation and Insertion Loss in the Series Configuration ($Z_O = 50$ Ω).

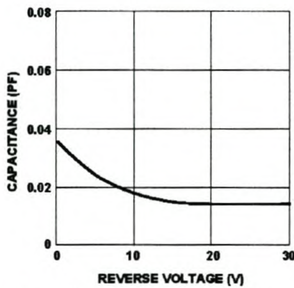


Figure 4. Typical Capacitance at 10 GHz vs. Reverse Bias.

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Bonding and Handling Procedures for Beam Lead Diodes

1. Storage
Under normal circumstances, storage of beam lead diodes in Agilent-supplied waffle/gel packs is sufficient. In particularly dusty or chemically hazardous environments, storage in an inert atmosphere desiccator is advised.

2. Handling
In order to avoid damage to beam lead devices, particular care must be exercised during inspection, testing, and assembly. Although the beam lead diode is designed to have exceptional lead strength, its small size and delicate nature requires that special handling techniques be observed so that the devices will not be mechanically or electrically damaged. A vacuum pickup is recommended for picking up beam lead devices, particularly larger ones, e.g., quads. Care must be exercised to assure that the vacuum opening of the needle is sufficiently small to avoid passage of the device through the opening. A #27 tip is recommended for picking up single beam lead devices. A 20X magnification is needed for precise positioning of the tip on the device. Where a vacuum pickup is not used, a sharpened wooden Q-tip dipped in isopropyl alcohol is very commonly used to handle beam lead devices.

3. Cleaning
For organic contamination use a warm rinse of trichloroethane, or its locally approved equivalent, followed by a cold rinse in acetone and methanol. Dry under infrared heat lamp for 5–10 minutes on clean filter paper. Freon degreaser, or its locally approved equivalent, may replace trichloroethane for light organic contamination.

- Ultrasonic cleaning is not recommended.
- Acid solvents should not be used.

4. Bonding
Thermocompression: See Application Note 979 "The Handling and Bonding of Beam Lead Devices Made Easy". This method is good for hard substrates only.

Wobble: This method picks up the device, places it on the substrate and forms a thermocompression bond all in one operation. This is described in the latest version of MIL-STD-883, Method 2017, and is intended for hard substrates only.

Resistance Welding or Parallel-GAP Welding: To make welding on soft substrates easier, a low pressure welding head is recommended. Suitable equipment is available from HUGHES, Industrial Products Division in Carlsbad, CA.

Epoxy: With solvent free, low resistivity epoxies (available from ABLESTIK and improvements in dispensing equipment, the quality of epoxy bonds is sufficient for many applications.

5. Lead Stress
In the process of bonding a beam lead diode, a certain amount of "bugging" occurs. The term *bugging* refers to the chip lifting away from the substrate during the bonding process due to the deformation of the beam by the bonding tool. This effect is beneficial as it provides stress relief for the diode during thermal cycling of the substrate. The coefficient of expansion of some substrate materials, specifically soft substrates, is such that some bugging is essential if the circuit is to be operated over wide temperature extremes.

Thick metal clad ground planes restrict the thermal expansion of the dielectric substrates in the X-Y axis. The expansion of the dielectric will then be mainly in the Z axis, which does not affect the beam lead device. An alternate solution to the problem of dielectric ground plane expansion is to heat the substrate to the maximum required operating temperature during the beam lead attachment. Thus, the substrate is at maximum expansion when the device is bonded. Subsequent cooling of the substrate will cause bugging, similar to bugging in thermocompression bonding or epoxy bonding. Other methods of bugging are preforming the leads during assembly or prestressing the substrate.

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