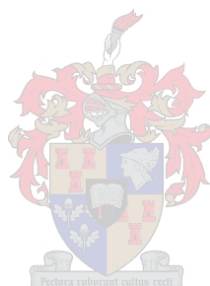


# SYNTHESIZER MODULATION FOR WIDEBAND FM GENERATION

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Thesis presented in partial fulfillment of the requirements  
for the degree of Master of Science in Engineering at the  
University of Stellenbosch.

Advisor

Prof. J. B. de Swardt

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– Declaration –

“I, the undersigned, hereby declare that the work contained in this thesis is my own original work and that I have not previously in its entirety or in part submitted it at any university for a degree.”

Signature

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Date



## Abstract

The high performance of present digital phase-locked loops makes it the preferred choice for the generation of stable, low noise, tunable local oscillators in wireless communications applications. Most transmitters use superheterodyn techniques for up-conversion of the modulated signal to the required transmission frequency. Another technique is to inject the modulation signal into a phase-locked loop and consequently generate a frequency modulated signal directly at the transmission frequency.

The aim of this study is to obtain a synthesizer configuration for the effective generation of wideband FM, considering both passive and active loop filters. The selection is based on synthesizer output signal quality, settling time and loop response to the modulation signal.

# Opsomming

Die hoë werksverrigting van fase-sluit lusse maak dit die verkiesde keuse vir die generasie van stabiele, lae ruis, verstelbare ossillators vir draadlose kommunikasie toepassings. Meeste senders gebruik "superheterodyn" tegnieke vir die op-menging van die gemoduleerde sein na die verlangde uitsaai frekwensie. 'n Ander tegniek is om die modulاسie sein in 'n fase-sluit lus te voer en so doende 'n gemoduleerde sein direk by die transmissie frekwensie te genereer.

Die doel van hierdie studie is om 'n sintetiseerder konfigurasie te verkry vir die effektiewe opwekking van 'n wyeband FM sein, deur beide passiewe en aktiewe lus filters in konsiderasie te neem. Die seleksie geskiet gebaseer op sintetiseerder uittree sein kwaliteit, sluit tyd en lus gedrag as gevolg van die modulاسie sein.

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- And lastly to all my friends for all their support and well wishes.

# Nomenclature

AC	- Alternating Current
CW	- Continues Wave
dB	- Decibel
dBc	- Decibel with respect to the Carrier
dBm	- Decibel with respect to a Milli-Watt
DC	- Direct Current
ECCM	- Electronic Counter Counter Measures
FM	- Frequency Modulated / Frequency Modulation
FSK	- Frequency Shift-Key
GaAs	- Galium Arsenide
GHz	- Giga-Hertz
HF	- High Frequency
Hz	- Hertz
IC	- Integrated Circuit
IF	- Intermediate Frequency
kHz	- Kilo-Hertz
$K_{\phi}$	- Phase/Frequency Detector Gain
$K_{sum}$	- Summation Network Gain
$K_{VCO}$	- Voltage-Controller Oscillator Gain
LO	- Local Oscillator
MHz	- Mega-Hertz
ms	- Milli-Seconds
N	- Feedback Division Ratio

$\Omega$	- Ohm
PFD	- Phase/Frequency Detector
PLL	- Phase-Locked Loop
rad	- Radians
RF	- Radio Frequency
RMS	- Root Mean Square
(S/N)	- Signal to Noise
UHF	- Ultra High Frequency
us	- Micro-Seconds
VCO	- Voltage-Controlled Oscillator
VHF	- Very High Frequency

## Acknowledgments

## Nomenclature

## Table of Contents

## Introduction

## Synthesizer Specifications

### 1 Synthesizer Architectures

### 2 General Synthesizer Loop Equations

#### 2.1 General Loop Equation

#### 2.2 System Noise Performance

##### 2.2.1 Phase Noise Characteristics of Amplifiers

##### 2.2.2 Phase Noise Characteristics of Dividers

##### 2.2.3 Reference Oscillator Phase Noise

### 3 Synthesizer Parameter Considerations

#### 3.1 Factors Influencing Loop Parameter Choice

##### 3.1.1 Phase Detector Type

##### 3.1.2 Loop Bandwidth

##### 3.1.3 Damping Ratio

# Table of Contents

<b>Opsomming</b>	<b>iii</b>
<b>Abstract</b>	<b>iv</b>
<b>Acknowledgements</b>	<b>v</b>
<b>Nomenclature</b>	<b>vi</b>
<b>Table of Contents</b>	<b>xii</b>
<b>Introduction</b>	<b>1</b>
<b>Synthesizer Specifications</b>	<b>3</b>
<b>1 Synthesizer Architectures</b>	<b>4</b>
<b>2 General Synthesizer Loop Equations</b>	<b>6</b>
2.1 General Loop Equations . . . . .	7
2.2 System Noise Performance . . . . .	12
2.2.1 Phase Noise Characteristics of Amplifiers . . . . .	12
2.2.2 Phase Noise Characteristics of Dividers . . . . .	12
2.2.3 Reference Oscillator Phase Noise . . . . .	12
<b>3 Synthesizer Parameter Considerations</b>	<b>14</b>
3.1 Factors Influencing Loop Parameters Choices . . . . .	14
3.1.1 Phase Detector Type . . . . .	14
3.1.2 Loop Bandwidth . . . . .	15
3.1.3 Damping Ratio . . . . .	15



3.1.4	Loop Gain . . . . .	15
3.1.5	Loop Division Ratio . . . . .	16
3.1.6	Noise in a Phase-Locked System . . . . .	16
3.1.7	Choice of Comparison Frequency . . . . .	18
3.1.8	Reference Sidebands . . . . .	19
3.1.9	Non-Reference Spurious Signals . . . . .	20
<b>4</b>	<b>Prescaler and Synthesizer IC Selection</b>	<b>22</b>
4.1	Selection of the Synthesizer IC and Prescaler . . . . .	22
<b>5</b>	<b>Reference Oscillator</b>	<b>26</b>
5.1	Design of Crystal Oscillators . . . . .	27
5.2	On-Board Oscillator . . . . .	28
5.3	Discrete Oscillator . . . . .	28
<b>6</b>	<b>Voltage-Controlled Oscillator</b>	<b>30</b>
<b>7</b>	<b>Hybrid Coupler</b>	<b>32</b>
<b>8</b>	<b>Charge Pump Design</b>	<b>35</b>
<b>9</b>	<b>Summing Network</b>	<b>37</b>
<b>10</b>	<b>The Loop Filter - Second-Order Synthesizer</b>	<b>40</b>
10.1	Loop Equations . . . . .	40
10.2	Loop Response to Change in Division Ratio . . . . .	42
10.3	Synthesizer Transient Response . . . . .	42
10.4	Phase Error due to Modulation . . . . .	44
10.5	VCO Modulation as a Function of Modulation Frequency . . . . .	46
<b>11</b>	<b>The Loop Filter - Third-Order Synthesizer</b>	<b>49</b>
11.1	Choice of Loop Amplifier . . . . .	49
11.2	Loop Equations . . . . .	50
11.3	Synthesizer Transient Response . . . . .	52
11.4	Phase Error due to Modulation . . . . .	53



11.5	VCO Modulation as a Function of Modulation Frequency . . . . .	54
<b>12</b>	<b>The Loop Filter - Fourth-Order Synthesizer</b>	<b>56</b>
12.1	Derivation of Component Values . . . . .	57
12.2	Designing the Loop Filter for Optimal Attenuation . . . . .	58
12.2.1	Determining the True Added Attenuation . . . . .	59
12.3	Synthesizer Transient Response . . . . .	60
12.3.1	VCO Non-Linearity . . . . .	61
12.3.2	VCO Input Capacitance . . . . .	62
12.3.3	Phase/Frequency Detector Discrete Sampling Effects . . . . .	62
12.4	Phase Error due to Modulation . . . . .	62
12.5	VCO Modulation as a Function of Modulation Frequency . . . . .	63
<b>13</b>	<b>Implementation</b>	<b>64</b>
13.1	Implementation Considerations . . . . .	64
13.1.1	Second-Order System . . . . .	64
13.1.2	Third-Order System . . . . .	65
13.1.3	Fourth-Order System . . . . .	67
13.2	Implemented Fourth-Order System . . . . .	68
<b>14</b>	<b>Synthesizer Measurements for Theoretical Verification</b>	<b>69</b>
14.1	Second-Order System . . . . .	70
14.1.1	Second-Order System Test 1 . . . . .	70
14.1.2	Second-Order System Test 2 . . . . .	73
14.1.3	Second-Order System Test 3 . . . . .	75
14.1.4	Second-Order System Test 4 . . . . .	77
14.2	Second-Order System Synopsis . . . . .	79
14.3	Third-Order System . . . . .	80
14.3.1	Third-Order System Test 1 . . . . .	80
14.3.2	Third-Order System Test 2 . . . . .	83
14.3.3	Third-Order System Test 3 . . . . .	85
14.4	Third-Order System Synopsis . . . . .	87
14.5	Fourth-Order System . . . . .	88

14.5.1	Fourth-Order System Test 1 . . . . .	88
14.5.2	Fourth-Order System Test 2 . . . . .	91
14.5.3	Fourth-Order System Test 3 . . . . .	93
14.5.4	Fourth-Order System Synopsis . . . . .	95
14.6	Measurement of High Frequency Summing Network . . . . .	96
14.7	Phase Noise Analysis . . . . .	98
14.7.1	Reference Oscillator Noise . . . . .	98
14.7.2	Amplifier Noise . . . . .	98
14.7.3	VCO Noise . . . . .	100
14.7.4	Phase/Frequency Detector Noise . . . . .	100
14.7.5	System Phase Noise . . . . .	102
<b>15</b>	<b>Synthesizer Configuration Comparison and Improvement</b>	<b>103</b>
15.1	Settling Time . . . . .	103
15.2	VCO Deviation due to Modulation Signal . . . . .	104
15.3	Reference Suppression . . . . .	104
15.4	Improvement to Fourth-Order System . . . . .	105
15.5	Comparison of Reference Oscillators . . . . .	108
	<b>Conclusions</b>	<b>109</b>
	<b>A Oscillator Analysis method</b>	<b>113</b>
	<b>B Design of the External Charge Pump</b>	<b>120</b>
	<b>C Oscillator Basics</b>	<b>122</b>
C.1	Basic Oscillator Theory . . . . .	122
C.2	Crystal Resonators . . . . .	122
C.3	Choice of Active Element . . . . .	123
	<b>D Summing Network Design</b>	<b>125</b>
D.1	Input Isolation Network . . . . .	125
D.2	Addition of Bias Voltage to Synthesizer Control Signal . . . . .	125
D.3	Output Isolation Network . . . . .	127

D.4 Nodal Summing Network . . . . .	130
<b>E Derivation of Component Values</b>	<b>132</b>
<b>F Derivation of Optimal Attenuation for Loop Filter</b>	<b>135</b>
F.1 Determining the True Added Attenuation . . . . .	135
F.2 Design for Optimal Attenuation . . . . .	136
<b>G Derivation of Equation for <math>C_1</math></b>	<b>138</b>
<b>H Derivation of Second-Order Transient Response</b>	<b>139</b>
H.1 Derivation of Transfer Function . . . . .	139
H.2 Second-Order Transient Analysis . . . . .	139
<b>I Calculation of Frequency Modulated Output Spectrum</b>	<b>141</b>
<b>J Motorola MC145170 PLL synthesizer IC Datasheet</b>	<b>143</b>
<b>Bibliography</b>	<b>144</b>



# Introduction

A frequency synthesizer is a variable-frequency generator with crystal-controlled stability. It is well known that crystal oscillators are superior to most other oscillators because of their stability and low phase noise. Due to this fact, it is desirable to use crystal resonators in almost all single frequency oscillators. Unfortunately, crystal resonators do not operate at very high frequencies and other methods have to be used for the generation of stable carrier signals at these frequencies. Several choices are available for the generation of high frequency carrier signals, such as dielectric resonator oscillators, cavity resonators, YIG Oscillators, magnetrons and phase-locked loop frequency synthesizers.

Synthesizers are generally subequipment designed to provide one or several Continuous Wave (CW) reference signals to the equipment or systems into which they are integrated. These signals are used as local oscillators in receivers and often to up-convert Intermediate Frequency (IF) signals before transmission (communication, radars, etc.). Modern equipment and systems operate at not only one single frequency, but rather over a frequency range, thus requiring sources with several output frequencies. These frequencies are generally equally spaced within the overall bandwidth of the equipment and frequency selection must be made easily and accurately [1].

Although most transmitters use a superheterodyn technique to up-convert the modulated signal to the wanted transmission frequency, this requires additional amplifiers to compensate for mixer insertion loss and filters to suppress mixer images. Another technique is to generate the modulated signal directly at the wanted transmission frequency. This can be done by using a synthesizer locked on the wanted transmission frequency and combining the modulation signal with the Voltage-Controlled Oscillator (VCO) control signal prior to applying it to the VCO.

The aim of this study is to investigate the use of different synthesizer configurations for the purpose of generating wideband Frequency Modulated (FM) signals at E+F band (2.45 GHz) while also examining the effect of the modulation signal on synthesizer performance. To incorporate most synthesizer configurations in the study, both passive and active loop filter configurations (Loop filters containing amplifiers as well as a charge pump circuit) will be considered. The key synthesizer features investigated include settling time, VCO modulation response, reference suppression, cost and ease of implementation.

The investigation starts with an overview of synthesizers with the purpose of deriving the general loop equation. This is followed by the global synthesizer design containing all loop parameters choices. Thereafter the various components composing the synthesizer are considered and designed. A theoretical analysis is performed on the synthesizer configurations considered, followed by validation in the form of practical measurements. The final chapter contains a theoretical comparison of the synthesizer types leading to the final conclusion.

With this study all the necessary groundwork for the design of synthesizers will be presented with numerous synthesizer characteristics theoretically analyzed and practically verified.

# Synthesizer Specifications

Although the focus of the study is to investigate the response of the synthesizer to a modulation signal, certain design requirements must be established. The following specifications will be used during the design:

Output Frequency:	- 2.45 GHz
Maximum Modulation Frequency:	- 50 MHz
Settling Time:	- 500 us
Phase Noise:	- -55 dBc @ 10kHz
Reference Signal Suppression:	- -35 dBc

As some of the synthesizer configurations considered in the study will not be able to achieve these specifications (due to component availability limitations), these design requirements will not be imposed during practical evaluation.



# Chapter 1

## Synthesizer Architectures

There are two basic approaches to frequency synthesis, namely direct and indirect synthesis.

*Direct Analogue Synthesis:* This is the oldest type of synthesis used to generate high frequency signals. The output signal is derived by combining multiple crystal-controlled oscillator outputs or a single stable frequency source with multiple divider/comb-generator sections [2].

The simplest way to design a synthesizer, i.e. a device that generates many frequencies from one or several reference sources, is to use a combination of sources with their outputs being selected by means of a switch. Various combinations are digitally switched in, and the unwanted subharmonics and other spurious frequencies are filtered out. The sources can be stable microwave oscillators using dielectric resonators, or HF, VHF or UHF oscillators using crystal resonators, etc. This type of device remains convenient only when a low number of frequencies are required, since size and cost increase linearly with required frequencies. The main advantage of direct incoherent synthesis is good flexibility due to the fact that the sources utilized in the synthesizer are independent so their number is chosen to define the number of frequencies required [1].

Unfortunately it is only possible to generate Frequency Shift-Key (FSK) modulation with this type of synthesizer unless a large number of frequency sources are used which is impractical. Another type of direct synthesizer is to use a digital-to-analog converter to digitally generate a sinusoidal waveform. This technique also proves to be very effective,



but the technology does not exist at the present moment to digitally produce signals directly at S-band.

*Indirect synthesis:* This approach relies on a spectrally pure VCO and programmable Phase-Locked Loop (PLL) circuitry. While slower and susceptible to noise on the VCO control line, the indirect frequency synthesis method is less expensive, requires much less filtering, and offers greater output power with lower spurious subharmonics [2].

Although susceptibility of FM noise on the VCO is seen in a negative light, this susceptibility can also be used for the generation of a FM signal. This can be done by intentionally superimposing the modulation signal onto the VCO control line of a synthesizer locked onto the wanted transmission frequency. This will generate a wideband modulated signal at the wanted transmission frequency only if the modulation frequency is higher than the loop bandwidth, otherwise the synthesizer will compensate for the disturbance to keep the output frequency stable.

The following section provides an overview of the basic synthesizer concepts necessary to thoroughly understand this study. This section is intended as background, but is necessary to comprehend advanced synthesizer concepts presented in subsequent chapters.

## Chapter 2

# General Synthesizer Loop Equations

### INTRODUCTION

For the effective design of synthesizers a thorough understanding of synthesizer functionality is required. Since feedback is used to acquire and maintain phase-lock, control system theory is required for synthesizer analysis. Figure 2.1 shows a conventional PLL used for directly generating a FM signal at the wanted transmission frequency.

The loop has the advantage of being adaptable to frequency agile systems in military equipment for the purpose of Electronic Counter Counter Measures (ECCM), by changing the loop division ratio in a pseudo-random mode. Such a system promotes the desirability of using a super-heterodyne receiver system since the Local Oscillator (LO) in the receiver can be a duplicate of the transmitter loop, with the receiver loop division ratio so chosen as to maintain a constant IF on any channel.

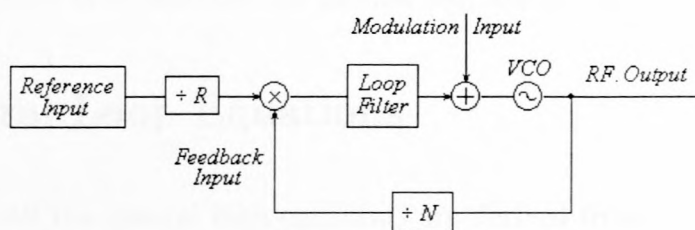


Figure 2.1: Synthesizer Block-Diagram

In the closed-loop system of figure 2.1, VCO deviation decrease substantially for modulation frequencies (or "disturbance" frequencies) below the loop bandwidth, thus constraining the modulation frequency range to frequencies above the loop bandwidth [3]. Using this characteristic, the loop's operation can be divided into two frequency domains depending on the frequency inside the loop. The synthesizer will compensate for disturbances of frequencies below the loop bandwidth, while disturbances of frequencies above the loop bandwidth will produce modulation of the VCO.

Another aspect to consider is the choice of phase/frequency detector (PFD); namely, a conventional voltage PFD or charge pump PFD. Unlike the voltage PFD, a charge pump produces current pulses with an average value proportional to the phase error. The charge pump PLL offers many advantages over the classical voltage PFD PLL including a zero steady state phase error. It also allows one to use a passive filter and still have many of the benefits of using an active filter with the voltage PFD [4].

The final synthesizer parameter to select is the type and order of loop filter. Rohde [4] states that although the third-order loop using a conventional PFD is initially more difficult to treat mathematically, it will give rise to better reference signal suppression, faster settling times and is better reproducible than second-order loops. This is due to the fact that there is always stray capacitance in the circuit that can be incorporated into the third-order loop where this is not always possible with a second-order loop. To complement this, Banerjee [5] suggests a fourth-order loop using a charge pump PFD.

To be able to find the best solution, second, third and fourth-order loops will be analyzed with the fourth-order loop using a charge pump PFD. The first step in the design of a frequency synthesizer is to establish the general loop equations.

## 2.1 General Loop Equations

In this section all the general loop equations are derived from first principles in order to provide the reader with a better understanding of the inner workings of a frequency synthesizer. Assuming the phase detector as a linear multiplier network and ignoring the summation product, the phase detector output signal is determined as:



$$V_d(t) = K_d \sin(\theta_i(t) - \theta_0(t)) \quad (2.1)$$

with

$$\begin{aligned} \theta_i(t) &= \omega_i(t) + \theta_i \\ \theta_0(t) &= \omega_0(t) + \theta_0 \\ K_d &= \text{Phase Detector Gain} \end{aligned}$$

where  $\omega_i(t)$  and  $\theta_i$  are the frequency and initial phase of the reference input respectively, while  $\omega_0(t)$  and  $\theta_0$  are the frequency and initial phase of the VCO output signal divided by the feedback division ratio  $N$ . For small phase errors, the phase detector operation can be approximated as linear, thus

$$V_d(t) \approx K_d(\theta_i(t) - \theta_0(t)) \quad (2.2)$$

The output frequency of the VCO is now given by

$$\omega_{vco}(t) = K_{vco}V_c(t) + \omega_{0f}(t) \quad (2.3)$$

where

$$\begin{aligned} K_{vco} &= \text{VCO Deviation Constant in Rad/s/Volt} \\ V_c(t) &= \text{VCO Control Voltage} \\ \omega_{0f} &= \text{Free Running VCO Frequency} \end{aligned}$$

Substituting for  $V_c(t)$ ,

$$\omega_{vco}(t) = \omega_{0f}(t) + K_{vco}(V_m(t) + K_{sum}K_dF(s)\theta(t)) \quad (2.4)$$

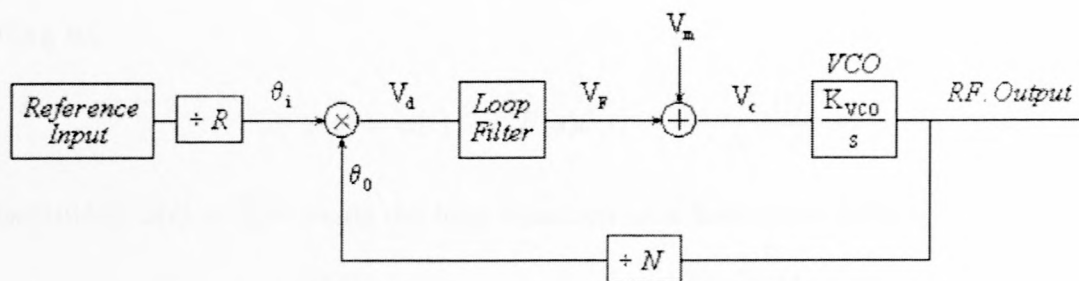


Figure 2.2: Synthesizer Block-Diagram

where

$$\begin{aligned}
 V_m(t) &= \text{Modulating signal} \\
 F(s) &= \text{LaPlace Representation of Filter} \\
 \theta(t) &= \theta_i(t) - \theta_0(t) = \text{Loop Phase Error} \\
 K_{sum} &= \text{Amplification Factor of Summation Network}
 \end{aligned}$$

The factor  $K_{sum}$  is the amplification factor of the summation network with which only the loop filter output signal is amplified. This factor is inserted to accommodate the situation when the VCO control voltage is higher than the maximum output voltage of the loop filter or when higher loop gain is required. Now, since

$$\theta(t) = \theta_i(t) - \theta_0(t)$$

differentiating gives,

$$\omega(t) = \omega_i(t) - \omega_0(t) = \omega_i(t) - \frac{\omega_{vco}(t)}{N}$$

Substituting for  $\omega_{vco}(t)$  into (2.4) yields,

$$\omega(t) = \omega_i(t) - \frac{\omega_{0f}(t)}{N} - KF(s)\theta(t) - \frac{K_{vco}V_m(t)}{N} \quad (2.5)$$

where,

$$K = \frac{K_{vco}K_dK_{sum}}{N} = \text{Loop Gain}$$

By now letting,

$$\omega_i(t) - \frac{\omega_{0f}(t)}{N} = \alpha(t)$$

leading to,

$$\omega(t) = \alpha(t) - KF(s)\theta(t) - \frac{K_{vco}V_m(t)}{N} \quad (2.6)$$

Substituting  $\omega(t) = \frac{d\theta(t)}{dt}$  yields the loop equation as a first-order differential equation:

$$\frac{d\theta(t)}{dt} + KF(s)\theta(t) = \alpha(t) - \frac{K_{vco}V_m(t)}{N} \quad (2.7)$$

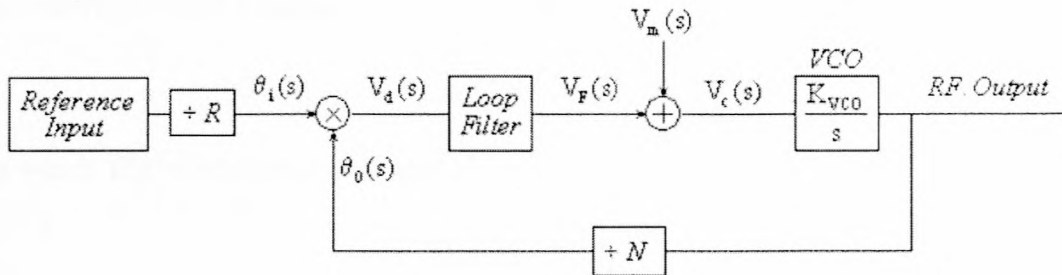


Figure 2.3: Equivalent Laplace Loop Configuration

This equation can be misleading due to the use of both time domain and frequency domain terms, and is simplified if the equation is transformed to the frequency domain using Laplace. Analysis of the block-diagram of figure 2.3 yields:

$$\omega_0(s) = s\theta_0(s) + \frac{\omega_{0f}(s)}{N} = \frac{s\theta_{vco}(s) + \omega_{0f}(s)}{N} = \frac{K_{vco}V_c(s) + \omega_{0f}(s)}{N} \quad (2.8)$$

By now following the same procedure, this equation simplifies to:

$$\omega(s) = \alpha(s) - KF(s)\theta(s) - \frac{K_{vco}V_m(s)}{N} \quad (2.9)$$

This is the Laplace transform of equation (2.7) and describes the loop phase error taking all loop parameters into account. Further general properties of the loop can be obtained from the block-diagram of figure 2.3 as follows:

$$\begin{aligned} V_c(s) &= K_{sum}V_F(s) + V_m(s) \\ &= K_{sum}K_dF(s)\theta(s) + V_m(s) \end{aligned} \quad (2.10)$$

This equation can be normalized by taking into account that,

$$\begin{aligned} \theta(s) &= \theta_i(s) - \theta_0(s) \\ &= \frac{\omega_i(s)}{s} - \frac{1}{N} \left( \frac{\omega_{0f}(s)}{s} + \frac{K_{vco}V_c(s)}{s} \right) \end{aligned}$$

Assuming the initial phase shifts to be zero ( $\theta_i = \theta_0 = 0$ ) and the VCO free running frequency  $\frac{\omega_{0f}(s)}{N}$  to equal the input reference frequency  $\omega_i(s)$ ,

$$\theta(s) = -\frac{K_{vco}V_c(s)}{Ns} \quad (2.11)$$

Equation (2.10) now simplifies to:

$$V_c(s) = K_d K_{sum} F(s) \left( -\frac{K_{vco} V_c(s)}{N s} \right) + V_m(s)$$

from which the relationship is obtained,

$$\frac{V_c(s)}{V_m(s)} = \frac{s}{s + K F(s)} \quad (2.12)$$

This equation describes the effect a modulation signal will have on the VCO control voltage and thus also the amount of modulation produced by the VCO. A similar calculation is performed to show the relationship between  $V_F$  and  $V_m$ . From the block-diagram of figure 2.3:

$$\begin{aligned} V_F(s) &= K_d F(s) \theta(s) \\ &= -K_d F(s) \left( \frac{K_{vco} V_c(s)}{N s} \right) \\ &= -\left( \frac{K_d K_{vco} F(s)}{N s} \right) (K_{sum} V_F(s) + V_m(s)) \end{aligned}$$

yielding,

$$\frac{V_F(s)}{V_m(s)} = -\frac{\left( \frac{K}{K_{sum}} \right) F(s)}{s + K F(s)} \quad (2.13)$$

The above equation describes the loop filter output signal as a function of the modulation signal. Using a similar technique to obtain an equation for the phase error due to the modulation (from (2.11)):

$$\begin{aligned} \theta(s) &= -\frac{K_{vco} V_c(s)}{N s} \\ &= -\left( \frac{K_{vco}}{N s} \right) (K_{sum} V_F(s) + V_m(s)) \\ &= -\left( \frac{K_{vco}}{N s} \right) (K_{sum} K_d F(s) \theta(s) + V_m(s)) \end{aligned}$$

leading to,

$$\frac{\theta(s)}{V_m(s)} = -\frac{1}{N} \left[ \frac{K_{vco}}{s + K F(s)} \right] \quad (2.14)$$

In all the above equations, the loop response both during normal operation and due to the modulation signal are modeled. As these are general equations, they apply for all loop filter orders and synthesizer configurations.



## 2.2 System Noise Performance

Apart from the general system performance as described by the loop equation, generated noise by all system components contributes significantly to the design and performance of the system. It is thus logical to use low noise components as far as possible and to isolated components to limit cross-interference. The following sections provide a slight overview of the leading causes of system noise.

### 2.2.1 Phase Noise Characteristics of Amplifiers

To minimize the effect of loading on the VCO, it is imperative to buffer the VCO output with an isolation amplifier. In doing so, the phase noise of the system is degraded due to the noise contribution of the amplifier. Most practical transistors have various internal noise sources to contend with. One of the more significant noise contributors is flicker noise, which depends on the active device used. The cause of flicker noise is low-frequency device noise modulating the phase of the passing signal through modulation of the transconductance, and thus the input and output impedances of the device [4]. Minimization of this noise contributing effect is performed by selection of the correct amplifier for the frequency range and application [3].

### 2.2.2 Phase Noise Characteristics of Dividers

Usually the phase noise contribution by a divider is to reduce the noise by a factor equal to the feedback division ratio  $N$ . This very desirable characteristic can be used to reduce the phase noise of the reference oscillator where a clean reference signal is required.

### 2.2.3 Reference Oscillator Phase Noise

Selection of a reference oscillator is fairly simple, the lower the phase noise the better. The reason being that the synthesizer has the effect whereby the reference signal is multiplied to produce the output signal, together with the reference phase noise. In other words, for a synthesizer with an output frequency 1000 times higher than the reference frequency, the phase noise of the output signal will be 60 dB higher than the reference

signal phase noise [4]. To thus produce as clean an output signal as possible, a reference signal with minimal phase noise is required.

Due to the complexity of a synthesizer, every parameter choice has both positive and negative effects on the system. The next chapter will highlight most of the considerations for choosing loop parameters as well as the effect the choice has on other loop variables.

## Synthesizer Parameter Selection

### INTRODUCTION

In the design of an application specific PLL, the designer must take into account the bandwidth, settling time, loop delay, phase noise, and lock time. There are a number of parameters that influence these parameters and these parameters are inter-related. The following sections will discuss the various parameters and their inter-relationships.

### 3.1 Factors Influencing Loop Parameters

#### 3.1.1 Phase Detector Type

There is a large variety of phase detectors available, each with its own characteristics. Amongst these are very simple phase detectors such as the edge-triggered JK flip-flop and the edge-triggered D flip-flop. The edge-triggered JK flip-flop is a simple phase detector that can be used as a current source with an external current source. The edge-triggered D flip-flop can be used as a current source with an external current source. The edge-triggered JK flip-flop is a simple phase detector that can be used as a current source with an external current source. The edge-triggered D flip-flop can be used as a current source with an external current source.

In order to compare the performance of the different phase detectors, the following table shows the lock time, lock voltage, PFD, and charge pump current for each type of phase detector. The PFD is implemented using a PLL with a loop delay of 10 ns.

## Chapter 3

# Synthesizer Parameter Considerations

### INTRODUCTION

In the design of an application specific synthesizer the choice of loop parameters (Loop Bandwidth, Damping Ratio, Loop Gain, Division Ratio's etc.) are essential for optimum performance. There are a variety of factors to be taken into account in the selection of these parameters as most have hidden adverse effects on loop performance. A few of these aspects are discussed below.

## 3.1 Factors Influencing Loop Parameters Choices

### 3.1.1 Phase Detector Type

There is a large variety of phase detectors available, each having its own advantages above the rest. Amongst these, two very distinct phase detectors are obtained, namely the edge-triggered JK master/slave flip-flop phase/frequency detector and an active integrator comparator commonly referred to as a charge pump phase/frequency detector. The output current of a charge pump circuit is of constant amplitude and variable duty cycle that can be modeled as a current source with an average output current proportional to the phase error.

To obtain a perspective of the effect phase detector types have on synthesizer performance, both voltage PFD and charge pump detectors will be investigated. The voltage PFD is implemented using a PLL synthesizer IC. To test the effects of the charge pump



detector, an external charge pump circuit is connected to the same PLL IC producing the required current pulses.

### 3.1.2 Loop Bandwidth

As with all synthesizer parameters, there are many factors to be considered during the choice of the loop bandwidth, with the primary determining factors being the comparison frequency as well as the synthesizer settling time. Banerjee [5] states that the discrete sampling effect of the phase detector will not effect settling time, provided the comparison frequency is large ( $\times 10$ ) compared to the loop bandwidth. On the other hand, too low a loop bandwidth will cause unrealistic settling times.

Usually the most important factors to consider when choosing the loop bandwidth is settling time and required reference suppression. With the loop bandwidth too narrow, increased reference suppression will be achieved but at the cost of longer settling times. For this application the most important considerations will be the synthesizer settling time and minimum modulation frequency. The loop bandwidth must be chosen, bearing in mind that the loop tracks phase changes at rates below the loop bandwidth, and ignores those occurring at rates above the loop bandwidth.

### 3.1.3 Damping Ratio

The damping in a phase locked loop can be independently chosen and set at any desired value provided the system is of third-order or higher. The damping determines the response of the loop to step changes of frequency, as well as the settling times after such a step. Most practical applications utilize critical or over-damping.

### 3.1.4 Loop Gain

It is important to keep the steady-state phase error small, therefore requiring a high DC loop gain [4]. Du Plooy [3] showed that a loop tracking improvement of 4% will be achieved for loop gains of more than ten times the loop bandwidth. In cases where the loop gain is too low, an amplifier can be used to increase the gain which can make the loop noisy and eventually even unstable [4]. Too high a loop gain must also be avoided

as this will lead to saturation of loop components. In most practical applications, it is possible to have a loop gain higher than the loop bandwidth by a factor of up to  $10^6$  [3].

During the selection of a VCO, it is desirable to keep the VCO gain as low as possible to reduce spurious responses. This is because of spurious signals coupling onto the high impedance VCO control line [4].

### 3.1.5 Loop Division Ratio

Although loop division ratio directly affects loop gain, these subjects can be treated as being independent since any change in  $N$  can be compensated for by varying the gain for other loop components. Du Plooy [3] stated that as the phase error is a function of  $\Delta$  (frequency deviation of the VCO at the phase detector input) when the loop division ratio is changed, it is desirable to keep  $\Delta$  small and thus to keep  $N$  at a relatively high value.

### 3.1.6 Noise in a Phase-Locked System

This section discusses the influence of the noise generated by the synthesizer components on the output noise. For simplicity, the block-diagram of figure 3.1 will be considered. From this diagram the following derivations are made:

$$G(s) = \frac{K_\phi K_{vco} Z(s)}{s}$$

$$H(s) = \frac{1}{N}$$

where  $Z(s)$  is the transfer function of the loop filter. From this, the transfer functions multiplying the various noise sources is derived and shown in Table 3.1. In other words, if a noise source is introduced at the source labeled in Table 3.1, the noise is multiplied to the system output by the corresponding transfer function. The reference noise has a factor of  $\frac{1}{R}$  multiplying it while the phase detector noise has a multiplication factor of  $\frac{1}{K_\phi}$ .

From the table it should be apparent that the phase detector noise,  $N$  divider noise,  $R$  divider noise, and the crystal noise all contain a common factor in their transfer functions:

$$\frac{G(s)}{1 + G(s)H(s)}$$



Table 3.1: PLL Noise Source Transfer Functions

Source ( $R_s$ )	Transfer Function
Reference	$\frac{1}{R} \frac{G(s)}{1+G(s)H(s)}$
R Divider	$\frac{G(s)}{1+G(s)H(s)}$
Phase Detector	$\frac{1}{K_\phi} \frac{G(s)}{1+G(s)H(s)}$
VCO	$\frac{1}{1+G(s)H(s)}$
N Divider	$\frac{G(s)}{1+G(s)H(s)}$

For this reason, all of these noise sources will be referred to as in band noise sources. It should be noted that the VCO noise is not included in this group which means that the VCO noise contributes the most noise outside the loop bandwidth.

Banerjee [5] stated that decreasing the loop bandwidth will reduce the RMS phase error. This is true, but only to a point. Within the loop bandwidth, the dominant noise source is the PLL (everything except for the VCO), while outside the loop bandwidth, the dominant noise source is the VCO. Decreasing the loop bandwidth beyond the point where the PLL noise equals the VCO noise, the phase error starts to increase. The loop bandwidth must thus be chosen in such a way that the PLL noise equals the VCO noise at the specific point of operation to achieve optimal RMS phase error [5].

For locking purposes, the effect of noise in this type of loop can be ignored if the VCO is designed to produce appreciable output power, and thus a high signal to noise ratio [3]. Noise in the loop is not troublesome if the VCO signal/noise ratio exceeds as little as 10 dB. Gardner [6] states that satisfactory loop operation can be obtained for phase detector input signals with a signal-to-noise ratio not less than 6 dB. The VCO signal to noise (S/N) ratio is required to be substantial, since spectral purity of the RF output signal is required for transmission purposes [3].

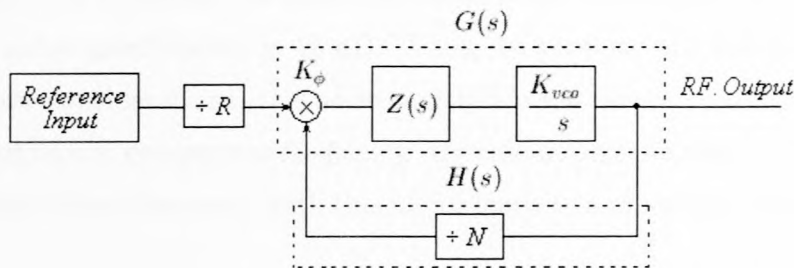


Figure 3.1: Simplified Block-Diagram of Synthesizer

### 3.1.7 Choice of Comparison Frequency

From the above considerations, it becomes apparent that the correct choice of comparison frequency is essential for obtaining the required loop performance. In order to achieve high frequency resolution, the comparison frequency must be small, corresponding to small frequency step sizes. To ensure loop stability the loop bandwidth must be smaller than the comparison frequency [4]. Therefore, a low comparison frequency will result in slow frequency jump capabilities.

Aside from loop dynamic variations, noise also depends on the selection of the comparison frequency. Since the synthesizer functions as a low-pass filter for reference oscillator and phase detector noise, but as a high-pass filter for VCO noise, the VCO noise contribution to the system can be minimized by using a wide bandwidth synthesizer. At the same time, the loop bandwidth should be less than the reference frequency to minimize reference and phase detector noise [4].

Therefore, the desire to have a low comparison frequency to obtain fine frequency resolution is offset by the need to have a high comparison frequency to reduce loop settling time and the noise contributed by the VCO.

During the design, settling time can be manipulated by varying the loop bandwidth, whereas the frequency resolution and system output phase noise is fixed once the comparison frequency is chosen. As there is no frequency resolution requirement, the phase noise specification is the determining factor on the choice of minimum comparison frequency.

Phase noise inside the bandwidth of the system is primarily dominated by either the reference oscillator or phase detector. On average, both components produce phase noise levels of  $-150$  dBc/Hz @ 10kHz. Assuming the dominating component to produce a noise level of  $-140$  dBc/Hz @ 10kHz, the allowable phase noise degradation with respect to the system phase noise specification is 85 dB. Thus, to produce the specified phase noise level with above considerations, the noise multiplication factor can be calculated, and thus also the minimum comparison frequency. By calculating the ratio of the degradation and dividing the output frequency with this factor leads to a minimum reference frequency of 138 kHz.



### 3.1.8 Reference Sidebands

In the design of PLL frequency synthesizers, a significant role is performed by spurious outputs and reference sidebands. These reference sidebands and spurious outputs can be caused in a myriad of ways, but the most common spurious responses encountered are the reference sidebands. The type of PFD, order of loop filter and loop bandwidth determines the amount of comparison frequency attenuation and thus the reference suppression.

For charge pump circuits these spurious signals are primarily caused by mismatches and leakage in the charge pump [5]. The leakage and mismatch in the charge pump leads to an AC modulated VCO control signal causing FM modulation of the output signal. Mismatch tends to dominate at high comparison frequencies while leakage tends to dominate at low comparison frequencies. The end result of mismatch and leakage is reference sidebands appearing on the output spectrum at multiples of the comparison frequency [5]. Much can be done to eliminate reference sideband problems, such as using the highest current mode, using a VCO with a lower gain and lower leakage, designing a higher order loop filter, and adding a notch filter to the loop filter [5].

#### Leakage Related Spurious Signals

As mentioned before, leakage effects are the dominant cause of reference sidebands at low comparison frequencies. In the locked condition of the PLL, the charge pump will generate short current pulses with long periods in between, during which the charge pump is in a high impedance state. During the high impedance state, the charge pump will ideally have an infinite impedance. This is in fact not the case with practical charge pumps and some leakage will occur.

Charge pumps are unfortunately not the only component with leakage. VCO, filter capacitors and sometimes even the board used contributes to leakage. To guard against leakage not due to the PLL loop filter, components must be placed far apart, capacitors used with low leakage properties and low leakage VCOs used.

To be able to predict spurious levels, the assumption is made that leakage is caused by the charge pump leakage alone, thus not taking charge pump mismatch into account. Through this assumption, the spurious levels can be predicted using the following equation [5]:

$$S_1 = 20 * \log \left[ \frac{K_{VCO} \times leakage}{F_{comp}^2 (C_1 + C_2) \sqrt{1 + (2\pi F_{Comp} R_3 C_3)^2}} \right] \quad (3.1)$$

### Mismatch Related Spurious Signals (Charge Pump Systems)

Reference sideband modeling with only leakage current is usually inadequate. The other contributor is charge pump mismatch that occurs when the current sunk by the charge pump does not equal the current delivered. This mismatch is defined as follows:

$$Mismatch(\%) = 200\% \left( \frac{I_{source} - I_{sink}}{I_{source} + I_{sink}} \right)$$

It is interesting to note that optimal performance is not achieved at 0% mismatch. The reason being that turn-on times are longer for PNP (source) device than for NPN (sink) devices. Due to turn-on times, PNP devices must source longer to keep a net zero current flow. Leakage current is also usually sinking current, meaning that the PNP device must source even longer. Through empirical measurements done by Banerjee [5], it was found that optimal performance is obtained with a +4% mismatch.

As mismatch is also dependent on VCO control voltage, there will be a certain frequency at which optimal spurious performance is achieved. Banerjee determined that over a VCO frequency range, mismatch can vary with 24.6%, yielding spurious level variations of 13.2 dB.

### 3.1.9 Non-Reference Spurious Signals

Besides reference sidebands, many other spurious responses can also occur. The following section describes a few measures to eliminate some spurious signals.

#### Electromagnetic Interference

Circuit layout is critical for obtaining optimum synthesizer performance. Care must be taken to avoid creating wire loops susceptible to magnetic coupling, as this will produce spurious signals on the synthesizer output. Should it not be possible to circumvent using



a loop, the area inside the loop must be minimized. Coupling can also lead to increased reference sidebands if care is not taken during the layout and power supply filtering. To minimize coupling, all connection wires must be as close to a ground plane as possible.

An aspect usually overlooked is common impedance coupling, mostly observed on power supplying lines. This is the effect where current drawn by one component causes a voltage drop on the power line that can influence other components connected further along the same supply line. To avoid this effect, the power to every component must be provided with its own separate power line.

Where possible, it is advisable to use coaxial cable to connect signals between components. Impedance matching between components is essential, as mismatches will result in reflected signals in coaxial lines that can cause standing waves and increased radiation.

### **Power Line Decoupling**

Power line decoupling is one of the most important principles when constructing any circuit. In most systems, the only "unscreened" connection between components are power lines by which signals can couple into other components in the system. Power line decoupling or filtering is performed by inserting a series inductor and parallel capacitors to ground. Most manufacturers suggest placing decoupling capacitors as close to all PLL components as possible. Ferrite beads can also be used and are effective over the frequency range 0.01 - 1000 MHz. For sensitive equipment with low bias current components, a small resistor can also be placed in series with the power line to obtain additional power line noise suppression.

Now that most loop considerations and physical layout have been discussed, the next step is to obtain the required synthesizer components. The first subject to be examined is the selection of the prescaler and synthesizer IC.

# Chapter 4

## Prescaler and Synthesizer IC Selection

### INTRODUCTION

This section explores the selection of the PLL IC and Prescaler to be used in all the system configurations. The requirement for design flexibility and experience, is to incorporate an external prescaler into the feedback path.

In the microwave field, halvers are generally used as prescalers [7, 8]. These dividers are based on flip-flop designs, thus producing an output frequency equal to the input frequency divided by  $2^N$  where N is the number of divider stages. Generally two types of materials are used to manufacture dividers, namely silicon and gallium arsenide (GaAs). Due to their higher electron mobility and higher maximum speed, GaAs dividers are being used more frequently [1].

### 4.1 Selection of the Synthesizer IC and Prescaler

The interdependence of the prescaler and PLL IC makes it desirable to select both at the same time. Due to specifications and limited product ranges of prescalers, obtaining the correct prescaler for an application can be difficult. Due to the nature of the synthesizer output frequency, quite a selection of prescalers are available. Factors considered with the selection process is prescaler input power range, input and output impedance, output power and required supply voltage.

Figure 4.1 shows the block-diagram representation of a typical PLL IC with the synthesizer components integrated into the IC shown in figure 4.2. As with the prescaler, quite



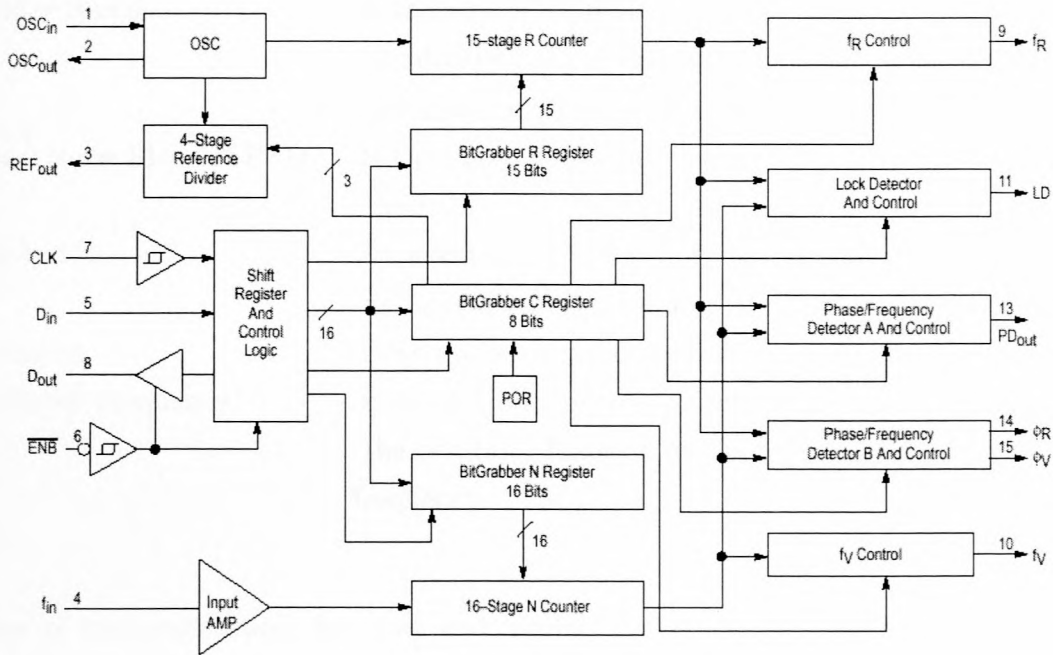


Figure 4.1: Block-Diagram of PLL IC

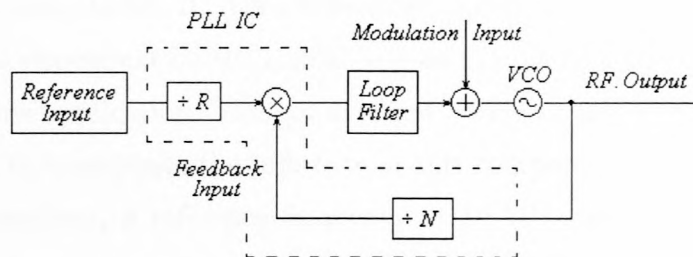


Figure 4.2: Synthesizer Block-Diagram

a variety of suitable PLL ICs are available. The general criteria used for selecting a PLL IC are as follows:

- |                               |  |
|-------------------------------|--|
| Input Frequency Range         | - The range of input frequencies must comply with the lowest and highest required VCO output frequencies divided by the prescaler. |
| Input sensitivity             | - Sensitivity must be compatible with the prescaler output level.  |
| Programming of IC             | - Serial or parallel programming interface.  |
| Supply Voltage                | - Preferably comply with existing system voltages.   |
| Phase/Frequency Detector Type | - Is the PFD type and specifications as desired.   |

Divider Ranges	- Is the wanted comparison frequency achievable with the divider ranges available. This is coupled with the maximum obtainable comparison frequency.
Phase Noise Floor of PFD	- Is the phase noise specifications achievable with the PFD noise floor.
Supply Current	- Excessive current consumption may result in non-conformance to power specifications.
Packaging	- Does the package comply with requirements.
Oscillator Frequency	- If an on-board reference oscillator is available, can the oscillator function at the required reference frequency.

Ease of implementation, low cost and availability led to the choice of the Motorola MC145170 PLL Synthesizer IC (refer to appendix J for the datasheet). This IC has the added advantage of having an internal reference oscillator that only requires the mounting of an external crystal. As the IC has a reference frequency divider, the choice of reference frequency is more dependent on the availability and implementation ease of the reference oscillator. For this application, both an external oscillator and the internal oscillator of the IC was used to investigate the influence of this component. As an output frequency of 2.45 GHz is required, a reference frequency of 10 MHz is chosen which could easily be divided into almost any comparison frequency. The IC also has a three-state output as well as double-ended PFD output. The former will be used for the realization of the voltage PFD circuit while the latter is ideal for interfacing to the external charge pump circuit.

Along with the PLL IC, the NEC UPB1506  $\div 64$  prescaler is selected to keep the value of N as large as possible to avoid large loop gain variations during frequency hopping. Verification of prescaler functionality is essential prior to integration with the system.

Although the device datasheets specify a minimum input power, the measurements performed do not necessarily apply to this specific application condition as physical layout can effect performance. Minimum input power measurements were performed, verifying operation for signal levels above -21 dBm.

For the same reasons mentioned above, the output power of the prescaler should be measured. The output power for an input signal strength of -10 dBm is obtained as -10.4 dBm. To show the interaction between the prescaler and the PLL synthesizer IC specifications, a summation block-diagram is shown in figure 4.3.

From figure 4.3 it is apparent that the prescaler was designed for driving sensitive high impedance ( $< 2 \text{ k}\Omega$ ) components such as high speed comparators. Instead of using costly high frequency comparators, a more elegant solution is obtained by using a transistor amplifier for both amplification and level translation. Although saturation of the amplifier effects the signal amplitude, it does not however influence the feedback signal frequency and the functionality of the system. The amplifier however introduces noise into the system as well as a phase delay in the feedback path, with the latter being compensated for by the synthesizer.

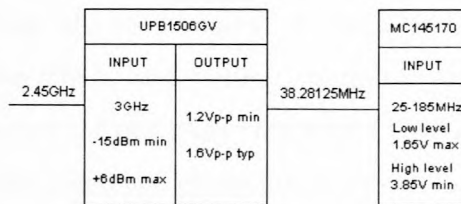


Figure 4.3: Interface diagram between Prescaler and Synthesizer IC

## Division Ratio

To accommodate the high input frequency from the VCO, the  $\div 64$  prescaler is used to lower the VCO frequency within the operational frequency range of the PLL IC. A Matlab program was used to determine the comparison frequency using the selected system frequencies. The optimum divider ratios were calculated as  $R=64$  and  $N=245$  leading to a comparison frequency of 156.25 kHz.

Now that all the system operating frequencies are known, the design and realization of the loop components can commence. The first component considered is the reference oscillator.



# Chapter 5

## Reference Oscillator

### INTRODUCTION

For this study, low phase noise design is not the focus and only some low noise reference oscillator considerations will be discussed. Crystal oscillators in general are easy to construct when temperature effect, load pulling, oscillator pushing and phase noise are of a lesser concern. If synthesizer output phase noise is a vital design parameter, great care must be taken to achieve low reference phase noise due to the multiplication effect of the reference oscillator phase noise.

Along with the reference oscillator designed in this section, an on-chip reference oscillator is also available. For interest sake, the effect of the on-chip reference oscillator on the output phase noise will be observed by interchanging the reference oscillators.

As in most systems, communication systems frequency stability coupled with low phase noise is of great importance. The following effects play an important role in the frequency stability of an oscillator:

- Temperature Variations
- Q of Resonator
- Transistor
- Loading of the Oscillator
- Biasing Network
- Biasing Voltage Variations

Due to the high cost of oven controlled oscillators compared to temperature compensated oscillators, frequently the latter are used as references for frequency synthesizers. In



Appendix C a brief discussion is presented about basic oscillator theory, crystal resonators and the choice of active component as it applies to crystal oscillators.

For increased oscillator frequency stability, the influence of the transistor should be minimized. This is performed by the addition of external capacitors to the input and output of the transistor, thereby virtually eliminating the effect of the transistor capacitances. In order to minimize oscillator components, it is desirable to use transistors with low input and output capacitances [9].

For this application the only specification placed on the reference oscillator is an oscillating frequency of 10MHz and noise levels lower than -140 dBc/Hz @ 10 kHz. The latter specification can not be measured by using a spectrum analyzer and special techniques such as the two- or three- oscillator measurement methods are required. These methods require specialized equipment which is not readily available.

Due to the lenient noise specification, a general purpose transistor is used as an active element. The transistor selected for the oscillator is the Motorola 2N3904 NPN transistor with a cut-off frequency ( $f_t$ ) of 200 MHz and input and output capacitance of 4 pF and 8 pF respectively.

## 5.1 Design of Crystal Oscillators

A Critical element for the design of a crystal oscillator is the choice of oscillator configuration. The three oscillator configurations considered are the Colpitts-, Clapp- and Pierce configurations. For the Colpitts configuration the biasing resistors are across the crystal and degrade performance at low frequencies. This configuration is also more susceptible to squegging (squegging is the term used when random oscillation occur with “dead zones” between the oscillations). If a choke is used to supply the DC voltage to the transistor of a Clapp oscillator, spurious oscillations can occur. The best solution is to only use a resistor for the biasing, or to use a large resistor in series with the inductor. This characteristic makes the Clapp oscillator undesirable for low supply voltages. The Pierce oscillator is generally the simplest to design, whilst the Colpitts is the most difficult. Frequency stability of the Pierce oscillator generally ranges from 0.0002 to 0.0005 percent worse than the stability of the crystal alone. The Clapp oscillator is slightly inferior to

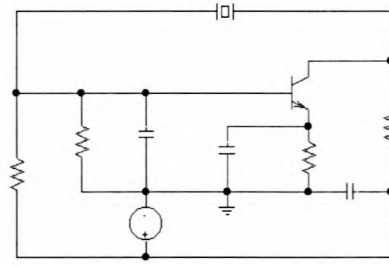


Figure 5.1: Pierce Oscillator Configuration

the Pierce oscillator and the Colpitts oscillator is slightly inferior to the Clapp oscillator in this respect [9]. The Pierce oscillator configuration (shown in figure 5.1) is used for the discrete oscillator design because of its superior frequency stability and ease of design.

## 5.2 On-Board Oscillator

For the on-board oscillator (oscillator contained in PLL synthesizer IC) only a crystal, shunt resistor and capacitors should be added to the IC circuitry. Unlike most receiver IC's using a Colpitts oscillator configuration, the on-board oscillator uses a Pierce configuration. Unfortunately the on-board oscillator is not discussed in detail in the datasheets and no information is available on its functionality or performance predictions. The only evaluation possible between the designed and on-board oscillators is a comparison of the output phase noise when switching between the oscillators.

## 5.3 Discrete Oscillator

The application notes of the synthesizer IC recommends that the input from the oscillator be terminated with a  $50\ \Omega$  parallel resistor, therefore it is required that the oscillator must be designed for a loading impedance of  $50\ \Omega$ .

For the oscillator to drive the IC, a signal level of  $1\ V_{p-p}$  is required. The signal level produced when connected to the IC does not meet this specification due to the low IC input impedance. This is easily rectified by inserting a buffer amplifier that also acts as an isolation amplifier, therefore countering oscillator pulling.

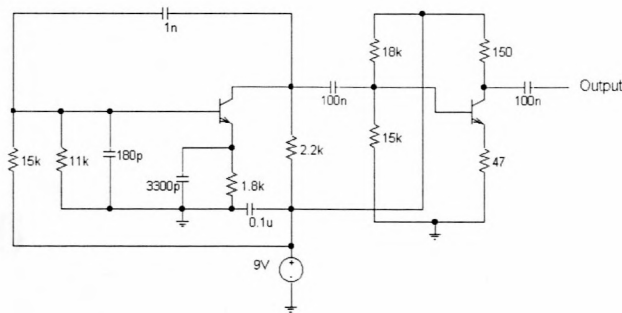


Figure 5.2: Pierce Oscillator Configuration

The final oscillator coupled with the buffer amplifier is shown in figure 5.2. The simulation program Pspice predicted the practical performance of the oscillator very accurately. With the reference oscillator, prescaler and PLL IC obtained, the next component to be considered is the VCO unit.



## Chapter 6

# Voltage-Controlled Oscillator

### INTRODUCTION

As with all electronic oscillators, frequency stability and waveform purity are critical design considerations in microwave oscillators for achieving the best performance. In order to achieve the best performance, the frequency-determining element, the “resonator”, must be of a form and material that isolate it as much as possible from the deleterious effects of its environment. Further it must have electrical characteristics of frequency selectivity, both in magnitude and phase that are the ultimate for its form [10].

Examination of the oscillator circuit reveals that the ideal design procedure is to divide the oscillator into two elements namely the active circuit and the resonator circuit. The active circuit includes the device and its embedment either in the transmission form or reflection form of oscillator. The resonator circuit includes any mechanical and electronic tuning, coupling to the output port and coupling to the active circuit. In other words, a division plane is created between the resonator circuit and active circuit.

Conditions for oscillation at this dividing plane or planes between the elements are then obtained followed by the design of the two elements. The active and resonator elements are designed to fit the oscillation conditions only at the division plane. This division between the two parts of the oscillator then becomes the physical coupling plane or planes in the practical realization of the actual oscillator. During design and testing any unwanted gain regions of the amplifier as well as spurious resonances in the resonator can be found and eliminated [11].



## Selection of Voltage-Controller Oscillator

Generally, selection of a VCO is primarily performed based on the following considerations:

- Frequency range required
- Output power required
- Frequency tuning linearity
- Low VCO gain to minimize spurious responses
- Low phase noise
- Low VCO pulling and pushing
- Power output linearity
- Load impedance
- Input capacitance as low as possible

The characteristics focused on for the selection of this VCO is the frequency range, VCO gain, phase noise and frequency tuning linearity. For this application, VCO gain is important because this will determine the amount of FM deviation for the applied modulation signal. Considerations to be kept in mind for the VCO gain selection is the modulation signal amplitude as well as the amount of modulation due to the control signal reference frequency component. A general rule of thumb is to keep the VCO gain as low as possible to minimize reference sidebands. Frequency tuning linearity causes variation of the loop gain and should also be minimized.

Due to the limited manufactures of VCOs, selection is limited to a few product lines adhering to the frequency range requirements. Of these most are designed for high VCO gain and are not suitable for this application. Availability and phase noise considerations were utilized during the final selection process.

The VCO selected is the V804ME03 from Z-Communications with a frequency range of 2230-2570 MHz and average power output of 5.5 dBm. It is also specified to produce phase noise of -91 dBc/Hz @ 10 kHz and exhibits low pulling and pushing characteristics. As two output ports are not provided by the VCO unit, a power splitter is required.

## Chapter 7

### Hybrid Coupler

Various methods exist to achieve division of output signal; using an amplifier buffer, resistive splitter or hybrid coupler. Constructing an amplifier buffer requires active devices and matching networks in the feedback path which can contribute to the system noise. The simplest method of achieving the divider action is to design a resistive splitting network or 3 dB hybrid coupler. To obtain design experience the hybrid coupler option was opted for. The basic layout of a microstrip hybrid coupler is shown in figure 7.1.

Analysis of this coupler is performed using symmetry planes that correspond to either electric or magnetic walls [12]. Using different excitations the following equations are obtained:

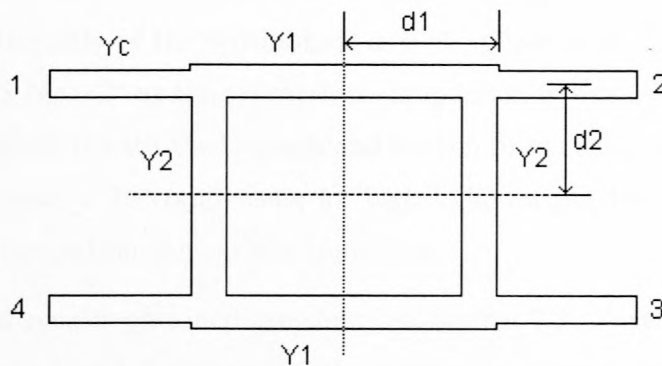


Figure 7.1: Hybrid Coupler Block-diagram

$$\begin{aligned}\Gamma_a &= \frac{Y_c - jY_1t_1 - jY_2t_2}{Y_c + jY_1t_1 + jY_2t_2} \\ \Gamma_b &= \frac{Y_ct_1 + jY_1 - jY_2t_2t_1}{Y_ct_1 - jY_1 + jY_2t_2t_1} \\ \Gamma_c &= \frac{Y_ct_2 - jY_1t_1t_2 + jY_2}{Y_ct_2 + jY_1t_1t_2 - jY_2} \\ \Gamma_d &= \frac{Y_ct_1t_2 + jY_1t_2 + jY_2t_1}{Y_ct_1t_2 - jY_1t_2 - jY_2t_1}\end{aligned}$$

where  $t_1 = \tan\theta_1 = \tan\beta_1d_1$  and  $t_2 = \tan\theta_2 = \tan\beta_2d_2$ , and  $Y_c, Y_1, Y_2$  are the characteristic admittance of the input line, the through line, and the branch line as shown in figure 7.1. Collin [12] states that the S-parameters of the coupler are given by:

$$\begin{aligned}S_{11} &= \frac{(\Gamma_a + \Gamma_b + \Gamma_c + \Gamma_d)}{4} \\ S_{12} &= S_{21} = \frac{(\Gamma_a - \Gamma_b + \Gamma_c - \Gamma_d)}{4} \\ S_{13} &= S_{31} = \frac{(\Gamma_a - \Gamma_b - \Gamma_c + \Gamma_d)}{4} \\ S_{14} &= S_{41} = \frac{(\Gamma_a + \Gamma_b - \Gamma_c - \Gamma_d)}{4}\end{aligned}$$

By now choosing  $t_1 = t_2 = 1$  so that the through lines and branch lines are one-quarter wavelength lines and also choosing  $Y_2 = Y_c$  and  $Y_1 = \sqrt{Y_c}$  a 3 dB coupler is obtained. The coupler has the characteristic that two output ports are  $90^\circ$  out of phase. This will not affect the functionality of the synthesizer, as a  $90^\circ$  phase shift at 2.45 GHz translates to a phase shift of  $5.74e - 3^\circ$  at the synthesizer comparison frequency. For a  $50 \Omega$  system,  $Z_1=50 \Omega$  and  $Z_2=35.35 \Omega$  with the through and branch lines one-quarter wavelength long at the relevant frequency. To compensate for high VCO output levels, provision is made for a 5 dB attenuator pad on the coupler input line.

The measurement results obtained are shown in figures 7.2. Port 1 is allocated as the input port with ports 3 and 4 assigned as the synthesizer output and prescaler feedback port respectively. It should be noted that S21 was not measured because port 2 will always be terminated with a  $50 \Omega$  load making this measurement irrelevant. The results show a low S11 over the measured frequency range as well as a relatively flat coupling to the synthesizer output port (S31). The prescaler feedback port coupling (S41) exhibits a 6 dB variation which will not affect system performance due to high prescaler sensitivity.



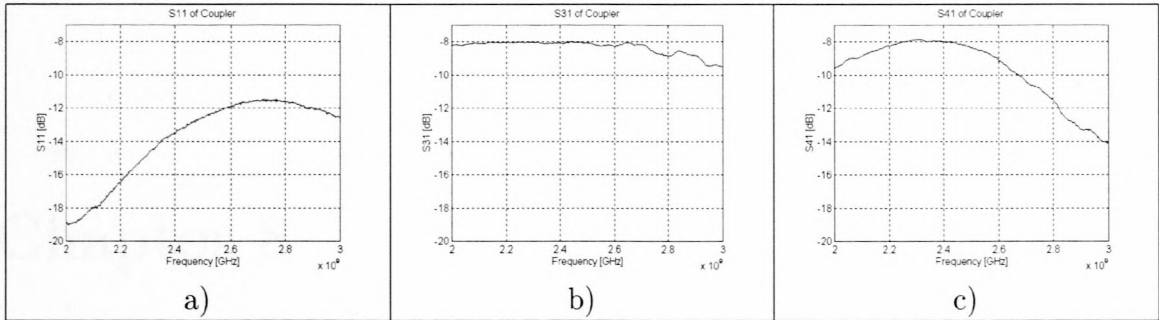


Figure 7.2: a) S11 of Hybrid Coupler b) S31 of Hybrid Coupler c) S41 of Hybrid Coupler

The design and implementation of all RF components are now completed and more attention can be given to the low frequency components. The only component still outstanding to complete the synthesizer configurations is the charge pump circuit used in the fourth-order system.



## Chapter 8

# Charge Pump Design

The primary concerns when selecting a charge pump circuit is the maximum current supplied by the pump and degree of charge pump mismatch as discussed in section 3.1.8. Unfortunately, PLL IC mismatch can be substantial, hence the design of an external charge pump circuit is required so that any mismatch can be corrected. Testing of charge pump mismatch is a simple procedure as long as the maximum charge pump output voltage is not exceeded during the measurements.

Reviewing the transfer functions of the various noise sources (section 3.1.6) reveals that the charge pump noise is divided by the charge pump gain. Banerjee [5] states that usually when the charge pump gain is increased, the charge pump noise increase as well. In some cases, no difference in phase noise is observed for different charge pump gain settings. The influence of the charge pump gain is therefore specific to the PLL IC used. Banerjee found that by decreasing the charge pump from 4 mA to 1 mA, a typical phase noise degradation of 4 dB is measured. The current application requires both low noise and fast settling times, thus yielding a choice of 5 mA for the charge pump current. This value is usually a selectable option for charge pump current in most PLL IC's.

The details pertaining to the charge pump circuit design is obtainable in Appendix B. Using current mirror techniques, the circuit of figure 8.1 is obtained for the chosen charge pump current [4].

Shown on the circuit is the double-ended outputs of the PLL IC ( $\phi V$  and  $\phi R$ ) used to drive the charge pump circuit. The general application transistors MMBT3904 and MMBT3906 from Motorola are used for the realization of the pump circuit. Measurements

show a mismatch of 1.4% which will degrade system performance minimally.

All the individual components for the various synthesizers are now completed. The summing network required for modulation signal injection is the only component not realized and is investigated in the following chapter.

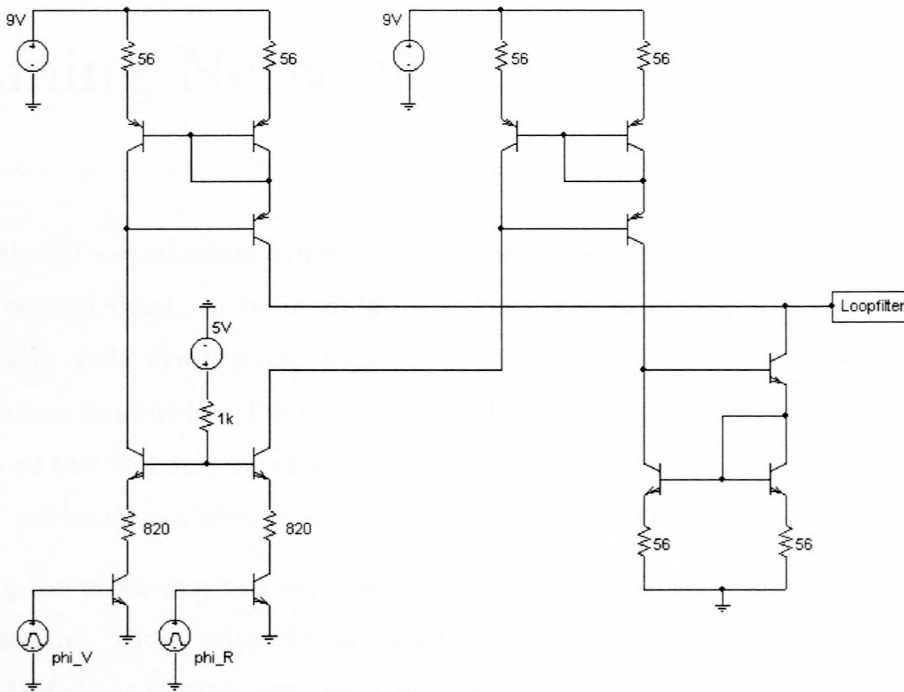


Figure 8.1: Charge Pump Circuit

## Chapter 9

# Summing Network

Modulation of a synthesizer can be accomplished by either adding a modulation signal to the VCO control signal, or by modulation of the synthesizer reference signal. Due to the low pass effect of the synthesizer, the latter will only be effective for modulation frequencies below the loop bandwidth. On the other hand, addition of the modulation signal to the VCO control line will only be effective for frequencies above the loop bandwidth. As high frequency modulation ability is required, the addition method is selected.

By using the block-diagram summation network depicted in figure 9.1, this ability can be implemented. Along with the modulation signal, a DC offset is added to the control signal for transistor biasing purposes discussed in Appendix D.

The maximum VCO control signal specified is 9 V, while the maximum PLL synthesizer IC output is only 5 V, requiring a gain factor of 1.8 to be incorporated into the summation

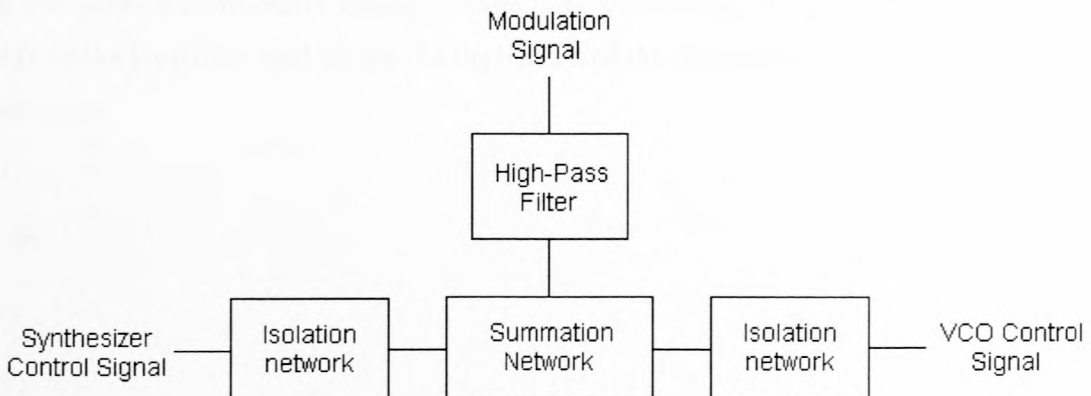


Figure 9.1: Summation Block-diagram



network. Instead of using a fixed gain value, the summation gain is designed to be variable in order to investigate the effects of varying loop gain on system characteristics. To isolate the control signal from the modulation signal, a high-pass filter is inserted between the control and modulation signals.

The summation network should not influence synthesizer functionality, while being able to sum high frequency signals to the DC VCO control signal. To this end any summing network pole contributed to the system must be at least 10 times higher than the synthesizer bandwidth [4]. Resulting in the high-pass filter pole being chosen at 100 kHz.

All mathematical models used for synthesizer analysis and synthesis assumes an infinite VCO input impedance. This requires an isolation amplifier to achieve the best correlation between the physical circuit and mathematical models. The isolation amplifier output impedance and the capacitive input impedance of the VCO forms a RC filter limiting the modulation frequency. Lowering of the amplifier output impedance thus has the effect of extending the modulation signal frequency range [4].

To achieve functionality at high output frequencies while also producing sufficient gain, a discrete transistor amplifier is used as active element in the output isolation network while a nodal summation network is constructed to perform the summing function. Refer to Appendix D for details concerning the design. The summation network realized (shown in figure 9.2) produces the simulated and measured results of figures 9.3 and 9.4. The figures verify that the synthesizer and modulation signal complies with the requirements.

All components required for the study are now complete and available for integration into the various synthesizer configurations. The following chapters discuss the detailed design of the loop filter and shows the derivation of the theoretical synthesizer performance predictions.

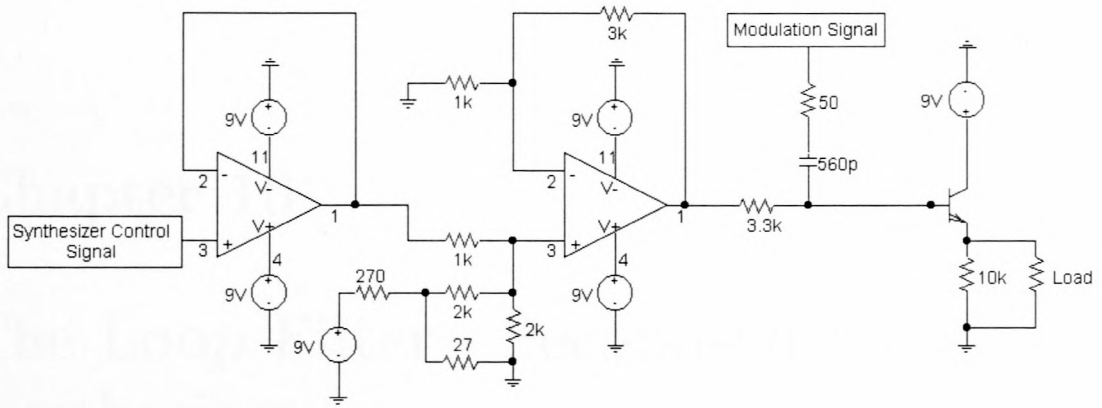


Figure 9.2: Final Summation Network

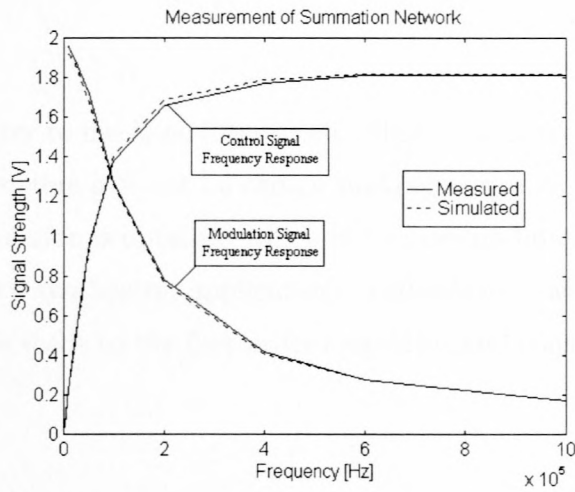


Figure 9.3: Frequency response of final summation network

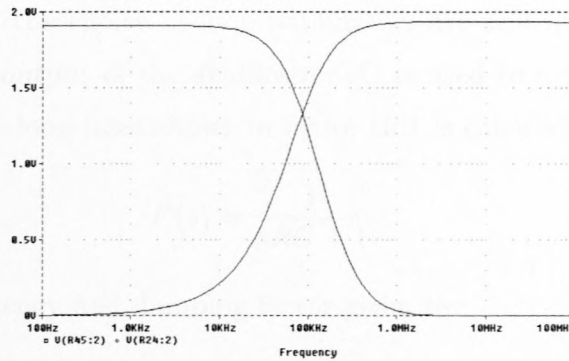


Figure 9.4: Simulated Frequency Response of Final Summation Network

## Chapter 10

# The Loop Filter - Second-Order Synthesizer

### INTRODUCTION

The simplest loop filter to use is no filter at all. This minimum configuration has several drawbacks; loop parameters can not be chosen making optimum performance impossible and no reference suppression is obtained which will cause modulation of the output signal. Therefore, for frequency synthesizer applications, a simple loop without any filter is rarely used [4]. Naturally this leads to the first-order loop filter and consequently a second-order system.

### 10.1 Loop Equations

Second-order loops using a first-order loop filter is a drastic improvement over the first-order system although the choice of loop parameters are still limited. For this system the single-ended PFD output of the synthesizer IC is used to drive the loop filter. The transfer function of the loop filter shown in figure 10.1 is calculated as:

$$F(s) = \frac{1}{sRC + 1}$$

with the natural frequency and damping factor given by:

$$\omega_n = \sqrt{\frac{K}{RC}}$$



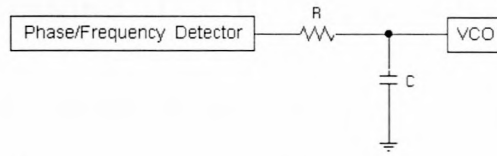


Figure 10.1: First-Order Loop Filter

where,

$$K = \frac{K_{VCO}K_{\phi}K_s}{N}$$

with,

$$K_{VCO} = \text{VCO Gain}$$

$$K_{\phi} = \text{Phase Detector Gain}$$

$$K_s = \text{Amplifier Gain}$$

$$N = \text{Feedback Division Ratio}$$

and,

$$2\xi = \frac{\omega_n}{K} = \sqrt{\frac{1}{RCK}} \quad (10.1)$$

Equation (10.1) shows how the natural frequency and damping factor is directly related through the loop gain and is not independently selectable. The 3-dB bandwidth ( $B$ ) is derived using the closed loop transfer function leading to [4]:

$$B = \omega_n \sqrt{1 - 2\xi^2 + \sqrt{2 - 4 \times \xi^2 + 4 \times \xi^4}} \quad (10.2)$$

Another parameter of interest is the system settling time. Rohde [4] states that the rise time of a second-order system is approximately related to the system bandwidth through the equation:

$$t_r = \frac{2.2}{B} \quad (10.3)$$

Although this loop filter may seem trivial, its significance must not be underestimated. Most modern day simple synthesizers utilizing classic voltage PFD can be implemented using this filter, yielding satisfactory results.

## 10.2 Loop Response to Change in Division Ratio

The loop's response to a change in division ratio is an important parameter in the successful application of the loop, and could perhaps even invalidate its use in channel changing applications. A change in loop division ratio is equivalent to the VCO of the basic phase-locked loop (shown in figure 2.1) being subjected to a voltage step modulating signal  $V_m$  of amplitude B volts. To prove this statement, the error function with a step change in the reference frequency is analyzed:

$$\frac{\theta(s)}{\theta_i(s)} = \frac{s}{s + KF(s)}$$

with  $\theta_i(s) = \frac{\Delta\omega}{s^2}$ ,

$$\theta(s) = \frac{\Delta\omega}{s(s + KF(s))}$$

Now looking at equation (2.14),

$$\frac{\theta(s)}{V_m(s)} = -\frac{1}{N} \left[ \frac{K_{VCO}}{s + KF(s)} \right]$$

with  $V_m(s) = \frac{B}{s}$ ,

$$\theta(s) = \frac{\frac{BK_{VCO}}{N}}{s(s + KF(s))}$$

where  $\frac{BK_{VCO}}{N}$  is the change in VCO frequency at the input to the PFD equivalent to a change of  $\Delta\omega$  in the reference frequency. This proves that a change in the division ratio can be regarded as a frequency step change of the reference frequency. The next section will focus on the application of this statement to determine the system transient response.

## 10.3 Synthesizer Transient Response

This section investigates the transient response of a PLL frequency synthesizer when the N divider is changed. This is accomplished by generating a third-order model where the only approximation is the continuous time approximation used for the PFD.

The aim of this analysis is to derive an expression for the transient response to be able to predict properties such as the settling time, rise time, overshoot, ringing, and damping

factor. To achieve an accurate prediction of the PLL response, all the poles and zeros of the transfer function must be included in the analysis. This is accomplished by multiplying the transfer function by  $\frac{f_2 - f_1}{Ns^2}$  to express the frequency step as a phase step in the Laplace domain. To now also represent the transfer function in the frequency domain, it must be multiplied by  $s$ . The transfer function thus reduces to:

$$\overline{F(s)} = CL(s) \left( \frac{f_2 - f_1}{Ns} \right) = \frac{n_1}{D_2 s^2 + D_1 s + D_0}$$

where,

$$\begin{aligned} n_1 &= \frac{K_\phi K_{VCO} K_s (f_2 - f_1)}{N} \\ D_2 &= RC \\ D_1 &= 1 \\ D_0 &= \frac{K_\phi K_{VCO} K_s}{N} \\ CL(s) &= \text{Closed-Loop Transfer Function} \end{aligned}$$

This equation is expanded into partial fractions by utilizing the following equation:

$$\overline{F(s)} = \sum_{i=0}^1 A_i \left[ \frac{1}{s(s - p_i)} \right]$$

where,

$$A_i = n_1 \prod_{k \neq i} \frac{1}{p_i - p_k}$$

Calculation of the transient response is performed by using the following inverse Laplace transform:

$$F(t) = f_2 + \sum_{i=0}^1 A_i e^{p_i t} \left( \frac{1}{p_i} \right)$$

Note that some of the coefficient  $A_i$  will be complex, however, they will combine in such a way that they all have negative real parts. The system will be unstable if the poles of the system do not have negative real parts. The transient response is calculated using Matlab for the following loop parameters with the results shown in figure 10.2:



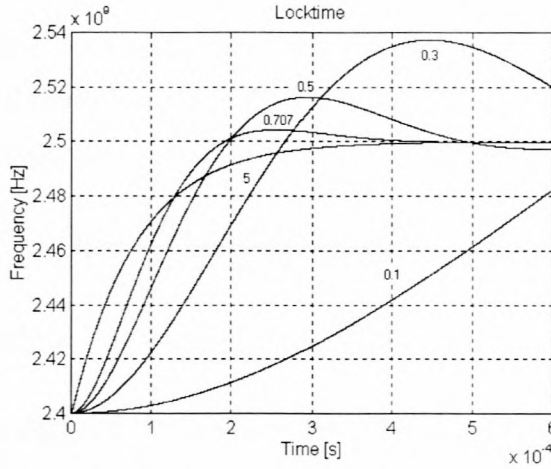


Figure 10.2: Transient Response of Second-Order Synthesizer

$$\begin{aligned}
 \text{Damping Factor} &= 0.1, 0.3, 0.5, 0.707, 5 \\
 N &= 15680 \\
 K_{VCO} &= 77e6 \\
 K_{\phi} &= 5/4/\pi \\
 K_{sum} &= 1
 \end{aligned}$$

(10.4)

Due to the dependent nature of the natural frequency and damping factor on loop gain, the higher the damping factor of the system, the faster the end frequency is reached. The figure clearly illustrates the overshooting characteristics for various damping factors.

## 10.4 Phase Error due to Modulation

The phase error introduced due to application of a sinusoidal modulation signal is of interest. The effect of modulation on the loop is obtained from equation (2.14):

$$\frac{\theta(s)}{V_m(s)} = -\frac{1}{N} \left[ \frac{K_{vco}}{s + KF(s)} \right] \quad (10.5)$$

Assuming a sinusoidal modulation signal,  $V_m(s)$  is given by:

$$V_m(s) = \frac{A\omega_m}{s^2 + \omega_m^2}$$

Thus leading to,

$$\theta(s) = -\frac{A\omega_m}{N} \left[ \frac{K_{vco}}{s + KF(s)} \right] \left[ \frac{1}{s^2 + \omega_m^2} \right] \quad (10.6)$$

To now obtain the time domain phase error, the inverse Laplace transform of equation (10.6) is to be calculated. All poles contributed by the loop filter transfer function  $F(s)$  will be complex leading to the partial fraction expansion for the poles of:

$$\theta(s) = \frac{K_1 + jK_2}{s + \alpha_1 + j\beta_1} + \frac{K_1 - jK_2}{s + \alpha_1 - j\beta_1}$$

Taking the inverse Laplace transform of these terms,

$$\theta(t) = e^{-\alpha_1 t} [2K_1 \cos(\beta t) - 2K_2 \sin(\beta t)]$$

From this equation it is clear that the filter poles will only contribute to the phase error transient response due to the exponential decaying multiplication factor, and will hence be ignored. Partial fraction expansion of the pole contributed by the modulation signal is given by:

$$\theta(s) = \frac{K_3 + jK_4}{s + j\omega_m} + \frac{K_3 - jK_4}{s - j\omega_m}$$

Using the inverse Laplace transform of these terms,

$$\theta(t) = 2K_3 \cos(\omega_m t) - 2K_4 \sin(\omega_m t)$$

The above equation shows these poles to produce a continuous variation of the phase error. Solving for  $K_3$  and  $K_4$ , the magnitude of phase error variation due to application of the modulation signal is determined. To demonstrate the effect of the damping factor on the phase error, the above equations are solved for the following values producing the graph of figure 10.3 (The equations show that the phase error will vary in accordance with the modulation signal amplitude and frequency. Hence the normalization of the x-axis with respect to modulation signal amplitude and frequency while the y axis is only normalized with respect to the modulation frequency.):

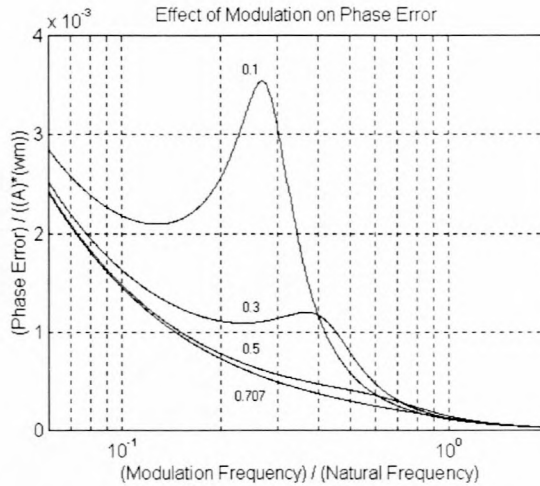


Figure 10.3: Magnitude of Phase Error due to Modulation Signal

$$\begin{aligned}
 \text{Damping Factor} &= 0.2, 0.3, 0.5, 0.707 \\
 N &= 15680 \\
 K_{VCO} &= 77e6 \\
 K_{\phi} &= 5/4/\pi \\
 K_{sum} &= 1 \\
 \text{Modulation Signal Amplitude} &= 1 \\
 \text{Modulation Frequency [rad]} &= 1000 - 100000
 \end{aligned}$$

From the figure it appears that the maximum phase error for the second-order system does not occur at a constant offset from the natural frequency. The curve also illustrates that at modulation frequencies above the natural loop frequency, the loop becomes increasingly insensitive to modulation and the maximum modulation frequency is only limited by the summation network and VCO. At frequencies well below the natural loop frequency, the phase error becomes progressively more as the loop attempts to counter the modulation signal.

## 10.5 VCO Modulation as a Function of Modulation Frequency

As modulation of the VCO output is the purpose of this study, this characteristic is the subject of this section. All system parameters are linked for a second-order system, thus only the effect of damping factor on VCO modulation will be discussed. Modulation of



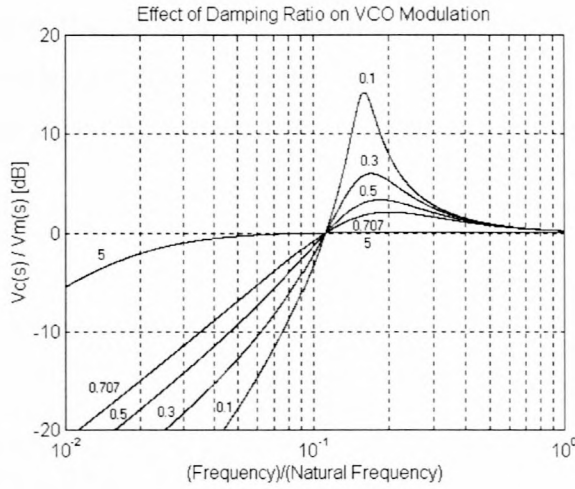


Figure 10.4: Effect of Damping Factor on VCO Modulation

the VCO control line due to the applied modulation signal has been determined earlier as (2.12):

$$\frac{V_c(s)}{V_m(s)} = \frac{s}{s + KF(s)}$$

where  $V_c(s)$  is the VCO control voltage and  $V_m(s)$  represents the modulation signal. To now demonstrate the effect of the damping factor on the VCO modulation, figure 10.4 shows a graph where the following synthesizer values are used (frequency axis normalized with respect to the modulation frequency):

$$\begin{aligned} \text{Damping Factor} &= 0.1, 0.3, 0.5, 0.707, 5 \\ N &= 15680 \\ K_{VCO} &= 77e6 \\ K_\phi &= 5/4/\pi \\ K_{sum} &= 1 \\ \text{Modulation Signal Amplitude} &= 1 \\ \text{Modulation Frequency [rad]} &= 1000 - 100000 \end{aligned}$$

Near and below the natural frequency of the loop, the frequency deviation displays a peaking phenomenon. This region can still be used in applications where low frequency modulation and fast settling times are required (thus a high natural frequency). Pre-emphasis or de-emphasis must then be employed to ensure that the bandwidth of the output signal does not exceed the input bandwidth of the receiver.

For frequencies below the peaking phenomenon the loop suppresses the modulation signal with 20 dB/decade as can be expected from a second-order system. As predicted, almost no modulation signal attenuation is obtained for frequencies above the natural frequency of loop.

## Chapter 11

# The Loop Filter - Sample and Hold Synthesizer

## INTRODUCTION

The third-order loop is really the most important loop that has not been used until now. It is the only loop that can be used to realize the very precise combination of low noise and high rejection and wide loop bandwidth. It is the only loop that can be used to realize the very precise combination of low noise and high rejection and wide loop bandwidth.

Although a third-order system is usually thought of as a system with three poles, a second-order system can be used to approximate the third-order system. The reason for this being that the third-order system in the system can be approximated with a second-order system. The reason for this being that the third-order system in the system can be approximated with a second-order system. The reason for this being that the third-order system in the system can be approximated with a second-order system.

## 11.1 - Choice of Loop Amplifier

In many applications the loop amplifier frequency must be high. This is because the loop amplifier frequency must be high. This is because the loop amplifier frequency must be high. This is because the loop amplifier frequency must be high. This is because the loop amplifier frequency must be high.

# Chapter 11

## The Loop Filter - Third-Order Synthesizer

### INTRODUCTION

The third-order loop is really the most important when voltage PFD is considered, but has not been used that often in the past [4]. This is contributed to a lack of understanding or not realizing that, by proper combination of the time constants, the unavoidable feed-through capacitors and some series capacitors can be incorporated to obtain this type of loop.

Although a third-order system is initially somewhat more difficult to treat mathematically than a second-order, better reference suppression, faster settling times and better reproducibility is achieved. The reason for this being that stray capacitance and other elements in the system can be incorporated into a third-order loop, whereas this is not possible in a second-order loop [4]. For this system, an active loop filter will be used which also has many considerations.

### 11.1 Choice of Loop Amplifier

In some applications the comparison frequency must be sufficiently high to accommodate fast locking, this means that the loop filter cut-off frequency must also be sufficiently high. The use of very wideband amplifiers is necessary in the realization of active loop filters due to the high cut-off frequency. An efficient method of realizing these loop amplifiers is



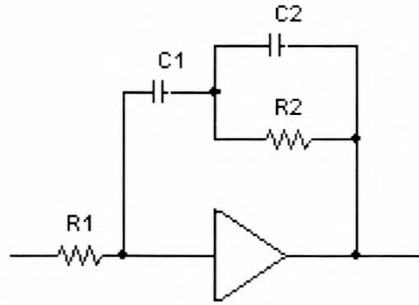


Figure 11.1: Second-Order loop filter

to use wideband operational amplifiers [4].

For this application the pole introduced by the operational amplifier must be at least ten times higher than the loop bandwidth which in turn must be ten times lower than the comparison frequency. As a comparison frequency of 156.25 kHz is used, an operational amplifier gain bandwidth product of higher than 800 kHz is required as a maximum gain of 5 will be used. The common LF351 operational amplifier easily meets this requirement with its high impedance J-FET input stage and high slew rate.

## 11.2 Loop Equations

The third-order loop can be developed from a second-order loop by adding one RC filter at the output. Figure 11.1 shows the second-order loop filter producing the third-order system. This loop has two integrators, one being the VCO and the other being the operational amplifier comprising of three time constants. The voltage transfer function of the filter is as follows:

$$F(s) = -\frac{1 + s\tau_2}{(s\tau_1)(1 + s\tau_3)} \quad (11.1)$$

with,

$$\begin{aligned} \tau_1 &= C_1 R_1 \\ \tau_2 &= R_2 (C_1 + C_2) \\ \tau_3 &= C_2 R_2 \end{aligned}$$

The open-loop gain is given by:

$$A(s) = K_\phi K_F F(s) \frac{K_{VCO}}{N_S} \quad (11.2)$$

Substituting the filter transfer function into (11.2) and setting  $s = j\omega$ , the phase of the open-loop gain is obtained as:

$$\tan\phi = \frac{\omega\tau_2}{1 + \omega^2\tau_2\tau_3} - \frac{\omega\tau_3}{1 + \omega^2\tau_2\tau_3} \quad (11.3)$$

Assuming now that,

$$\omega^2\tau_2\tau_3 \ll 1$$

the phase margin is given by:

$$\phi = \tan^{-1}(\omega\tau_2) - \tan^{-1}(\omega\tau_3) \quad (11.4)$$

To determine the natural frequency  $\omega_n$  of the system, the point of zero phase slope is found leading to,

$$\omega_n = \sqrt{\frac{1}{\tau_2\tau_3}} \quad (11.5)$$

Since all the system characteristics have been derived, attention can be given to the design of the time constants for specific loop parameters. By setting the open-loop gain equal to unity, the relationship between the first time constant and the loop bandwidth ( $\omega_c$ ) is obtained as:

$$\tau_1 = \frac{K_\phi K_0}{N\omega_c^2} \sqrt{\frac{1 + \omega_c^2\tau_2^2}{1 + \omega_c^2\tau_3^2}} \quad (11.6)$$

If we set,

$$\alpha = \tan^{-1}(\omega\tau_2) \quad \text{and} \quad \beta = \tan^{-1}(\omega\tau_3)$$

equation (11.4) can be written as,

$$\phi = \alpha - \beta + \pi$$

and,

$$\tan\phi = \tan(\alpha - \beta) = \frac{\tan\alpha - \tan\beta}{1 + (\tan\alpha)(\tan\beta)} = \frac{\omega\tau_2 - \omega\tau_3}{1 + \omega^2\tau_2\tau_3} \quad (11.7)$$

By now setting,

$$\begin{aligned} \omega_c = \omega_n &= \frac{1}{\sqrt{\tau_2\tau_3}} \\ \tau_2 &= \frac{1}{\omega_n^2\tau_3} \end{aligned} \quad (11.8)$$

Substituting (11.8) into (11.7), the time constant  $\tau_3$  is determined as follows:

$$\begin{aligned}
 \tau_3 &= \frac{-2\tan\phi_n\omega_n + \sqrt{4\tan^2\phi_n\omega_n^2 + 4\omega_n^2}}{2\omega_n^2} \\
 &= \frac{-\tan\phi_n + \sqrt{(\cos^2\phi_n + \sin^2\phi_n)/\cos^2\phi_n}}{\omega_n} \\
 &= \frac{-\tan\phi_n + 1/\cos\phi_n}{\omega_n}
 \end{aligned} \tag{11.9}$$

As can be seen from (11.9),  $\tau_3$  is determined by using all the specified loop characteristics. Once  $\tau_3$  is known,  $\tau_2$  can be calculated using (11.8) followed by  $\tau_1$  with equation (11.7). Once all the time constants are known, the filter components are calculated and a full analysis of the system is performed to ensure optimum performance. Analysis of the system is discussed in the following sections and is performed in general to generate a generic third-order loop design technique applicable to any classic voltage PFD third-order synthesizer.

### 11.3 Synthesizer Transient Response

To obtain the transient response of the system, a third-order model is derived where the continuous time approximation is used for the phase detector. The same procedure is used for the analysis as for the second-order system. The transfer function of this system is now given by:

$$\overline{F(s)} = CL(s) \left( \frac{f_2 - f_1}{Ns} \right) = \frac{n_1(1 + s\tau_2)}{D_3s^3 + D_2s^2 + D_1s + D_0}$$

where,

$$n_1 = K_\phi K_{VCO} K_s (f_2 - f_1)$$

$$D_3 = N\tau_1\tau_3$$

$$D_2 = N\tau_1$$

$$D_1 = K_\phi K_{VCO} K_s \tau_2$$

$$D_0 = K_\phi K_{VCO} K_s$$



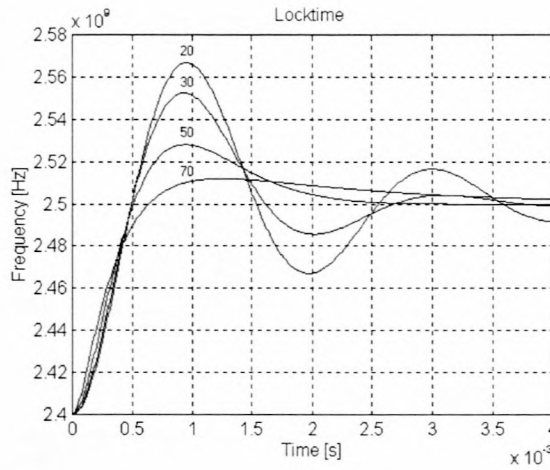


Figure 11.2: Transient Response of Third-Order Synthesizer

Employing the inverse Laplace transform, the transient response is calculated as:

$$F(t) = f_2 + \sum_{i=0}^3 A_i e^{p_i t} \left( \frac{1}{p_i} + R_2 C_2 \right)$$

with,

$$A_i = n_1 \prod_{k \neq i} \frac{1}{p_i - p_k}$$

The transient response is calculated using Matlab for the following loop parameters with the results shown in figure 11.2:

$$\begin{aligned} \text{Phase Margin} &= 20, 30, 50, 70 \\ N &= 15680 \\ K_{VCO} &= 77e6 \\ K_{\phi} &= 5mA \\ K_{sum} &= 1 \\ \text{Natural Frequency} &= 500 \text{ Hz} \end{aligned}$$

The figure illustrates that a low phase margin results in increased settling time and overshoot, while high phase margins again produces extended settling times but no overshoot.

## 11.4 Phase Error due to Modulation

Assuming a sinusoidal modulation signal and using the same equations as in section 10.4, the phase error is determined as:

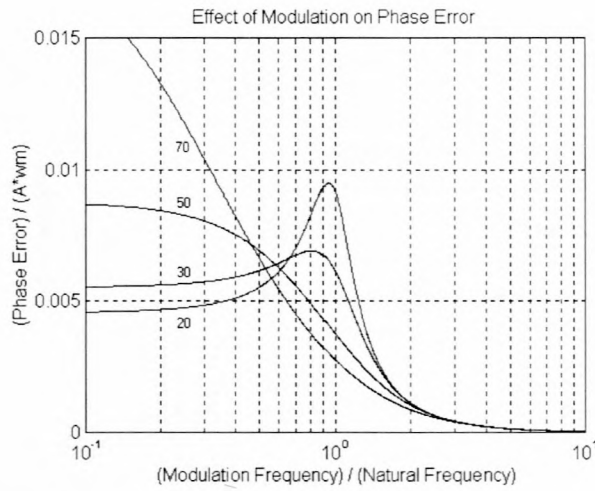


Figure 11.3: Magnitude of Phase Error due to Modulation Signal

$$\theta(s) = -\frac{A\omega_m}{N} \left[ \frac{K_{vco}}{s + KF(s)} \right] \left[ \frac{1}{s^2 + \omega_m^2} \right]$$

By performing the inverse Laplace transform and again ignoring all transient effects, the graph of figure 11.3 is obtained for the following values:

$$\begin{aligned} \text{Phase Margin} &= 20, 30, 50, 70 \\ \text{Natural Frequency} &= 500 \\ N &= 15680 \\ K_{VCO} &= 77e6 \\ K_\phi &= 5mA \\ K_{sum} &= 1 \\ \text{Modulation Signal Amplitude} &= 1 \\ \text{Modulation Frequency [rad]} &= 1000 - 100000 \end{aligned}$$

For low phase margins all modulation frequencies have little effect on the phase of the system. Systems with high phase margins have the disadvantage of producing high phase errors due to the applied modulation signal.

## 11.5 VCO Modulation as a Function of Modulation Frequency

Following the same procedure as section 10.5, the effect of phase margin variations on VCO modulation is shown in figure 11.4 for the following synthesizer parameters:

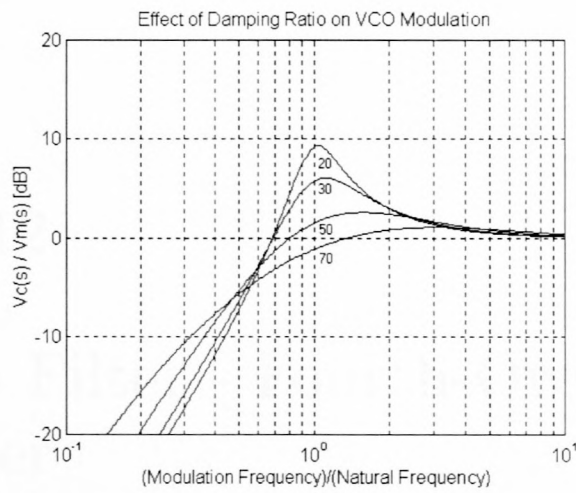


Figure 11.4: Effect of Phase Margin on VCO Modulation

$$\text{Phase Margin} = 20, 30, 50, 70$$

$$N = 15680$$

$$K_{VCO} = 77e6$$

$$K_{\phi} = 5mA$$

$$K_{sum} = 1$$

$$\text{Modulation Signal Amplitude} = 1$$

$$\text{Modulation Frequency [rad]} = 1000 - 100000$$

The graph shows that peaking occurs at frequencies just above the loop bandwidth. For frequencies below the peaking phenomenon, the loop suppresses the modulation signal with 40 dB/decade. For frequencies above the natural frequency of loop, almost no modulation signal attenuation is obtained.



## Chapter 12

# The Loop Filter - Fourth-Order Synthesizer

### INTRODUCTION

As the vast majority of PLLs incorporates PFDs combined with charge pump circuits, it seems relevant that such a circuit must also be investigated. The charge pump offers many advantages over the classical voltage PFD PLL including the use of passive filters and still having many of the benefits of using an active filter with the voltage PFD. Passive filters are the preferred choice of most synthesizer designers as almost no noise is generated with passive filters coupled with low implementation cost [5].

The passive third-order loop filter proposed for the synthesizer is shown in figure 12.1. Capacitor  $C_2$  is added for significant spurious level reduction. The components  $R_2$  and  $C_3$  are added to improve reference frequency suppression.

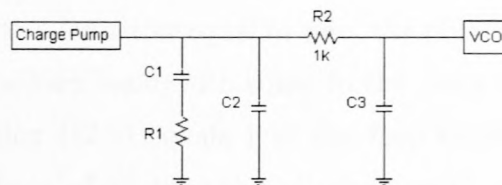


Figure 12.1: Passive Third-Order Loop Filter

## 12.1 Derivation of Component Values

It can be difficult to calculate component values as will be shown in this section. The component values are not only a factor of the loop parameters, but also of the added attenuation of the loop filter. This factor will be discussed in detail during development of the analysis equations.

The transfer function of the loop filter is given by:

$$Z(s) = \left( \frac{1 + sT_2}{s(1 + sT_1)(1 + sT_3)} \right) \left( \frac{T_1}{C_1T_2} \right) \quad (12.1)$$

with,

$$\begin{aligned} T_2 &= R_2C_2 \\ T_1 + T_3 &= \frac{C_2C_3R_2 + C_1C_2R_2 + C_1C_3R_3 + C_2C_3R_3}{C_1 + C_2 + C_3} \\ \frac{T_1 + T_3}{T_2} &= \frac{C_1C_3R_3}{C_1 + C_2 + C_3} \end{aligned}$$

with  $T_1$ ,  $T_2$  and  $T_3$  representing the time constants of the loop filter. Using this filter transfer function the open-loop gain of the system is given by:

$$\begin{aligned} Gain_{OL} &= \frac{K_{VCO}K_\phi}{s^2N} \left( \frac{1 + sT_2}{(1 + sT_1)(1 + sT_3)} \right) \left( \frac{T_1}{C_1T_2} \right) \\ &= \frac{K_{VCO}K_\phi}{s^2N} \left( \frac{1 + sT_2}{(1 + sT_1)(1 + sT_3)} \right) \left( \frac{1}{C_1 + C_2 + C_3} \right) \end{aligned} \quad (12.2)$$

From the open-loop gain it is now possible to obtain the phase margin equation as:

$$\phi = \tan^{-1}(\omega T_2) - \tan^{-1}(\omega T_1) - \tan^{-1}(\omega T_3) + 180 \quad (12.3)$$

Using (12.3) and setting the derivative equal to zero, the point of maximum phase margin is obtained. Choosing the loop bandwidth equal to the point of maximum phase margin and knowing that equation (12.2) equals 1 at the loop bandwidth, 4 equations and 4 unknowns are obtained from which the value of capacitor  $C_1$  is obtained. The quadratic equation of  $C_1$  is as follows (Refer to Appendix E for the detailed derivation of this equation):

$$T_2(k_4 + 1)C_1^2 + (k_3 - k_2 - k_3(k_4 + 1))C_1 + k_3k_1 = 0 \quad (12.4)$$

In order to minimize the effect of the input capacitance of the VCO on the loop filter, the value of  $k_4$  must be as large as possible which will in turn result in a large value for  $C_3$ . To find the largest value of  $k_4$ , the first step is to set the discriminator of (12.4) equal to zero. The discriminant for equation (12.4) is:

$$Ak_4^2 + Bk_4 + C$$

where,

$$A = k_3^2$$

$$B = 2k_2k_3 - 4T_2k_3k_1$$

$$C = k_2^2 - 4T_2k_3k_1$$

With the discriminant equated to zero and solved for  $k_4$ , one obtains the restriction:

$$k_4 < r_1 \text{ or } k_4 > r_2$$

with  $r_1$  and  $r_2$  being the roots, and  $r_1 < r_2$ . Banerjee [5] states that  $k_4 = r_1$  is usually the largest possible choice for  $k_4$  yielding component values that are both real and non-negative. Once  $k_4$  is selected, equation (12.4) can be solved for  $C_1$  followed by the solution of  $C_2$ ,  $C_3$ ,  $R_2$  and  $R_3$  in that order. If the component values obtained is complex or negative, it may be necessary to adjust  $k_4$  or ATTEN and recalculate the component values. The next section will investigate the choice of  $k_4$  for optimal loop performance.

## 12.2 Designing the Loop Filter for Optimal Attenuation

In synthesizer design, the designer specifies various variables such as  $w_p$  (second-order bandwidth),  $w_c$  (third-order bandwidth),  $\phi$  (second-order phase margin),  $N$  (Loop division ratio) and for this system the added attenuation ATTEN (added attenuation due to  $R_3$  and  $C_3$ ) as well. ATTEN is merely an index and is not the actual added reference attenuation added to the loop as will be shown. For ATTEN = 0,  $w_c = w_p$ , however as ATTEN increases,  $w_c$  decreases to levels well below  $w_p$ . Note that  $w_p$  is not the true bandwidth, but the second-order bandwidth while  $w_c$  is the third-order bandwidth and thus the correct bandwidth. The next section investigates the actual added attenuation for



a filter of fixed loop bandwidth  $w_c$ , and investigates the value of ATTEN that maximizes the true added attenuation over a fixed loop bandwidth.

### 12.2.1 Determining the True Added Attenuation

The addition of components  $R_3$  and  $C_3$  forms an additional pole in the loop filter to increase spurious attenuation and also reduce loop bandwidth. The first instinct when choosing ATTEN is to use the largest possible value. By doing this other filter properties can be changed such as the filter constant  $T_1$  which decreases. This could result in a net effect turning out to be different than once thought [5].

For a specified bandwidth, ATTEN can only be increased until  $w_p$  becomes infinite which corresponds to the maximum value for ATTEN. This point corresponds to  $T_1$  becoming zero meaning that the filter consists of only  $R_3$  and  $C_3$  and is clearly not the optimum solution. Choosing ATTEN as zero is also not the best choice as this would result in the pole not being inserted at all. An optimum value must exist for ATTEN that will lead to the maximum added attenuation of a specific bandwidth [5]. ATTEN is defined as [13]:

$$ATTEN = 20 \log \left| 1 + (2\pi f_{com} R_3 C_3)^2 \right|$$

Calculation of the optimum value is performed by firstly obtaining the frequency domain equivalent of the synthesizer forward loop gain. By then substituting the known equation for  $C_1$  and comparing the obtained attenuation to the attenuation obtained from a second-order loop filter, it is found that the optimum attenuation is achieved when (Refer to Appendix F for the detailed derivation):

$$T_1 = T_3 = \frac{K_{ATTEN}}{2} = \frac{\sec(\phi_c) - \tan(\phi_c)}{2\omega_c}$$

This is the optimum choice of  $T_3$ . Banerjee [5] found that it is better to design with a higher ATTEN when the comparison frequency is large relative to the loop bandwidth. As ATTEN is increased, the capacitor  $C_3$  tends to become smaller. Caution must be taken that  $C_3$  does not become too small as the VCO input capacitance will start to dominate the extra loop filter pole.

## 12.3 Synthesizer Transient Response

For this loop filter, a fourth-order model is derived where the continuous time approximation is once again used for the PFD. The same procedure is used for the analysis of the transient response of this synthesizer as for the second- and third- order synthesizers. The transfer function of this system is given by:

$$\overline{F(s)} = CL(s) \left( \frac{f_2 - f_1}{Ns} \right) = \frac{n_1(1 + sA_1)}{s^4 + D_3s^3 + D_2s^2 + D_1s + D_0}$$

where,

$$\begin{aligned} n_1 &= \frac{K_\phi K_{VCO}(f_2 - f_1)}{NC_1C_2C_3R_2R_3} \\ A &= \frac{K_\phi K_{VCO}(f_2 - f_1)}{NC_1C_3R_3} \\ D_3 &= \frac{B_2}{B_1} = \frac{C_2C_3R_2 + C_1C_2R_2 + C_1C_3R_3 + C_2C_3R_3}{R_2R_3C_1C_2C_3} \\ D_2 &= \frac{B_3}{B_1} = \frac{C_1 + C_2 + C_3}{R_2R_3C_1C_2C_3} \\ D_1 &= \frac{K_\phi K_{VCO}}{NR_3C_1C_3} \\ D_0 &= \frac{K_\phi K_{VCO}}{NR_2R_3C_1C_2C_3} \end{aligned}$$

The transient response is calculated by using the inverse Laplace transform:

$$F(t) = f_2 + \sum_{i=0}^3 A_i e^{p_i t} \left( \frac{1}{p_i} + R_2 C_2 \right)$$

with,

$$A_i = n_1 \prod_{k \neq i} \frac{1}{p_i - p_k}$$

The transient response is calculated using Matlab for the following loop parameters with the results shown in figure 12.2:

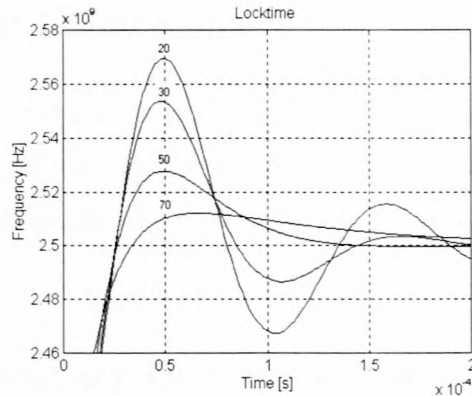


Figure 12.2: Transient Response of Fourth-Order Synthesizer

$$\text{Phase Margin} = 20, 30, 50, 70$$

$$N = 15680$$

$$K_{VCO} = 77e6$$

$$K_{\phi} = 5mA$$

$$K_{sum} = 1$$

$$\text{Modulation Signal Amplitude} = 1$$

$$\text{Modulation Frequency [rad]} = 1000 - 100000$$

The lower the phase margin, the more overshoot will occur and the final settling time also increases. The same effects are seen as with the third-order system. Factors that could cause theoretical settling time predictions to be inaccurate are:

- VCO Non-Linearity
- VCO Input Capacitance
- Phase/Frequency Detector Discrete Sampling Effects

### 12.3.1 VCO Non-Linearity

A significant problem with PLL analysis is VCO non-linearity. At high VCO control voltages the VCO gain tends to be less, leading to lower loop gain and thus also longer settling times. It is also possible that the VCO control voltage can go outside the tuning range due to overshoot and cause response predictions to be incorrect. The design must be performed with higher phase margin in order to minimize the overshoot.



### 12.3.2 VCO Input Capacitance

The input capacitance of the VCO adds in parallel with capacitor  $C_3$  and therefore the characteristics of the loop filter can be changed in such a way that the loop bandwidth can be altered and therefore also the settling time. To minimize this effect capacitor  $C_3$  must be as big as possible.

### 12.3.3 Phase/Frequency Detector Discrete Sampling Effects

The discrete sampling effects of the PFD tend to have little bearing on the settling time, provided that the comparison frequency is large (10X) compared to the loop bandwidth. Banerjee [5] stated that a fourth-order model was compared to another model that did take these effects into account. The comparison led to the conclusion that the difference in the settling time is negligible.

## 12.4 Phase Error due to Modulation

Assuming a sinusoidal modulation signal and using the same equations as in section 10.4 the phase error is determined as:

$$\theta(s) = -\frac{A\omega_m}{N} \left[ \frac{K_{vco}}{s + KF(s)} \right] \left[ \frac{1}{s^2 + \omega_m^2} \right]$$

By performing the inverse Laplace transform and again ignoring all transient effects, the graph of figure 12.3 was obtained for the following values:

$$\begin{aligned} \text{Phase Margin} &= 20, 30, 50, 70 \\ N &= 15680 \\ K_{VCO} &= 77e6 \\ K_\phi &= 5mA \\ K_{sum} &= 1 \\ \text{Modulation Signal Amplitude} &= 1 \\ \text{Modulation Frequency [rad]} &= 1000 - 100000 \end{aligned}$$

The results obtained are identical to that of the third-order system.

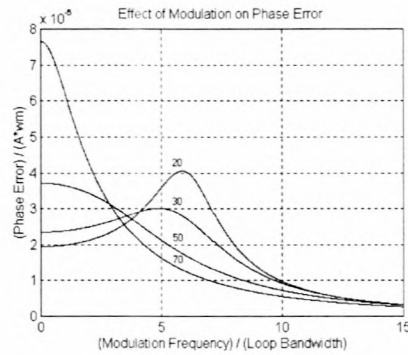


Figure 12.3: Magnitude of Phase Error due to Modulation Signal

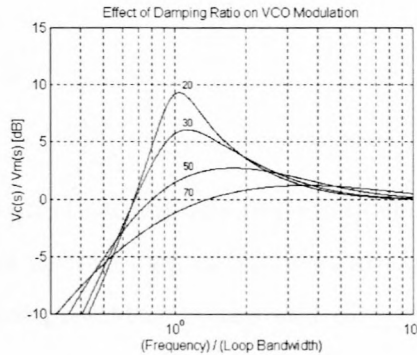


Figure 12.4: Effect of Phase Margin on VCO Modulation

## 12.5 VCO Modulation as a Function of Modulation Frequency

Following the same procedure as section 10.5, the effect of phase margin variation on VCO modulation is shown in figure 12.4 with the following synthesizer parameters:

$$\begin{aligned}
 \text{Phase Margin} &= 20, 30, 50, 70 \\
 N &= 15680 \\
 K_{VCO} &= 77e6 \\
 K_{\phi} &= 5mA \\
 K_{sum} &= 1 \\
 \text{Modulation Signal Amplitude} &= 1 \\
 \text{Modulation Frequency [rad]} &= 1000 - 100000
 \end{aligned}$$

Again, identical results are obtained when compared to the third-order system. All of the proposed synthesizer configurations have now been analyzed theoretically. In the next chapter the implementation of the various loop filter configurations are examined.

# Chapter 13

## Implementation

### INTRODUCTION

This section presents the practical implementation of the proposed synthesizer configurations. The selection of the various loop parameters are considered for each system with the designed circuit diagram presented at the end of each section. The only topic not investigated is the loop filter which is the subject of the following chapter.

### 13.1 Implementation Considerations

#### 13.1.1 Second-Order System

Due to the system's lack of design freedom, the only selectable parameter is the damping factor. Damping factor values of 0.3, 0.707 and 2 are used during the tests to facilitate adequate synthesizer parameter variations. For further theoretical prediction analysis, summation network gains of 2 and 5 are used to test system performance variation due to loop gain deviations. For this system a VCO gain of 77 MHz/V and PFD gain of  $\frac{5}{4\pi}$  is used [4].

Capacitor and resistor values are chosen, keeping availability of the desired value and package in mind. Care was taken to choose capacitor values not exceeding available ceramic values while using realistic surface mount resistor values. Surface mount components are used to reduce coupling and physical loop filter size.

Figure 13.1 shows the circuit used for the realization of the loop filter and low frequency



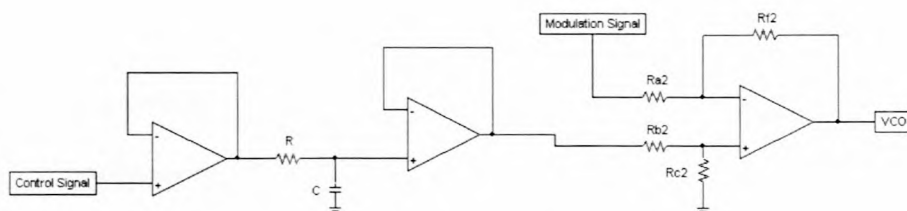


Figure 13.1: Implementation of Second-Order Loop Filter and Summation Network

summation network. The limited output current of the PLL IC necessitated the use of an isolation amplifier. The LF351 operational amplifier is used primarily because of availability, high gain-bandwidth product and current sourcing properties. Loading on the loop filter caused by the summation network is minimized by another isolation amplifier. The low frequency summation network resistor values will be selected to obtain the required summation gain while providing a unity gain path for the modulation signal.

### 13.1.2 Third-Order System

To obtain a realistic value for time constant  $T_1$ , a natural frequency of 500 Hz is used. To now obtain practical values for resistor  $R_1$ , capacitor  $C_1$  is chosen as 100 nF (largest ceramic capacitor available). For evaluation purposes, phase margin values of  $30^\circ$  and  $50^\circ$  and summation network gains of 1 and 2 are used.

It must be noted that a PFD gain of  $\frac{5}{2\pi}$  is used due to the active filter incorporated in the system. To better understand this statement, the PFD gain of both the second- and third-order systems are analyzed. The second-order system uses the output of the IC directly causing the detector gain to depend solely on the IC characteristics. The IC datasheet states that the tri-state comparator will output an average of 0 V for input signals shifted  $+360^\circ$  and 5 V for  $-360^\circ$  (or visa versa depending on the operational programming of the IC). This consequently produces a PFD gain of  $\frac{5V}{4\pi}$ .

The practical implementation of the active filter must be understood to relate the active filter functionality to the phase detector (see figure 13.2). Due to the integration action of the active filter, any DC (positive or negative) signal applied to the filter will result in the filter output saturating against the supply voltages. To avoid this the PFD signal (0 V-5 V) must be level shifted to obtain a voltage swing around 0V, hence the first

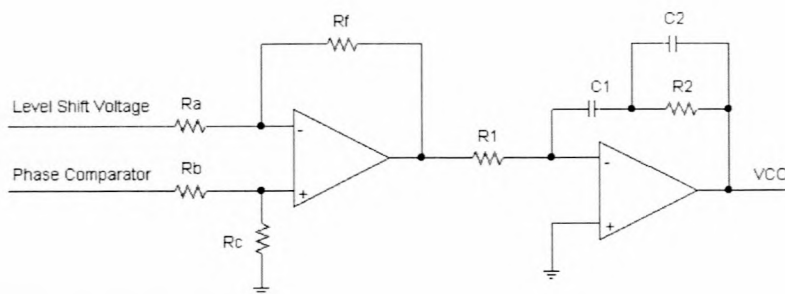


Figure 13.2: Implementation of Third-Order Loop Filter

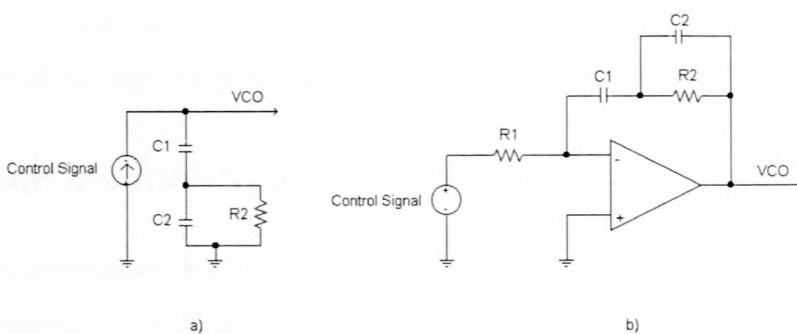


Figure 13.3: Transformation of Active Loop Filter

operational amplifier section of the loop filter.

It is now possible to transform the active loop filter to a passive loop filter driven by a charge pump circuit. It must be recognized that the operational amplifier output port is a low impedance point equivalent to a ground point. The transformation is done as shown in figure 13.3 where the voltage source and input resistor is replaced with a current source. Now an 5 V output pulse from the comparator will be equivalent to a positive current pulse from the charge pump and a 0 V pulse equivalent to a negative charge pump pulse. From the above, it is thus clear that the active filter effectively doubles the output range of the PFD leading to a gain of  $\frac{5V}{2\pi}$ .

Realization of the loop filter and low frequency summation function is shown in figure 13.4. Resistors  $R_{f1}$ ,  $R_{a1}$ ,  $R_{b1}$  and  $R_{c1}$  will be selected to obtain unity gain for both the control signal and offset correction signal. A high resistive value for  $R_{b1}$  and  $R_{c1}$  is used to avoid saturation of the IC output current. The second stage is the loop filter which component values will be determined for the required loop characteristics. The final stage is a low frequency summation network necessary to determine the loop response

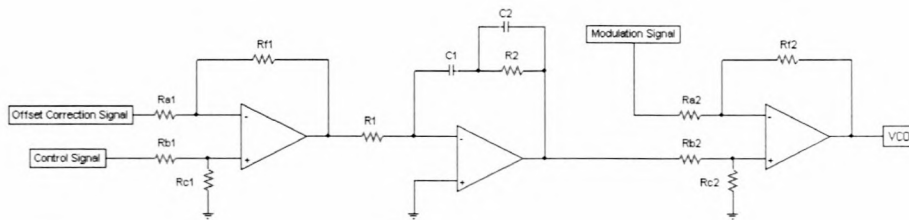


Figure 13.4: Implementation of Third-Order Loop Filter and Summation Network

to disturbance signals. Here the resistor values will be selected to obtain the required summation gain and maintain unity gain for the modulation signal. The combination of  $R_{b2}$  and  $R_{c2}$  must be kept large to minimize loop filter loading.

### 13.1.3 Fourth-Order System

As previously mentioned, a PFD gain of 5 mA was chosen due to settling time and phase noise considerations. A synthesizer loop bandwidth of 9.5 kHz is used to obtain realistic component values while phase margin values of  $20^\circ$  and  $50^\circ$  are used with summation network gains of 1 and 2. The circuit used for the loop filter and low frequency summation network is shown in figure 13.5.

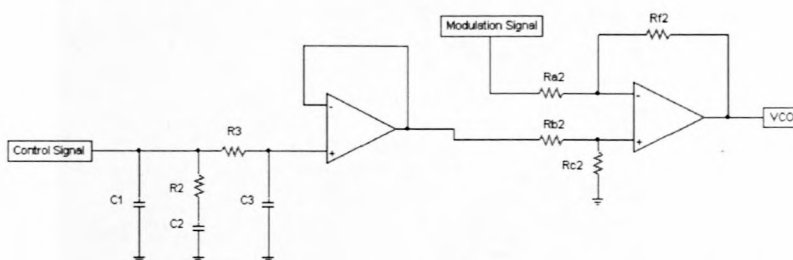


Figure 13.5: Implementation of Fourth-Order Loop Filter and Summation Network



## 13.2 Implemented Fourth-Order System

To provide a better understanding of the study, figure 13.6 shows the practically implemented system while figure 13.7 shows the physical component placement. From these figures the EMI shielding of the loop filter, VCO and prescaler are clearly visible.

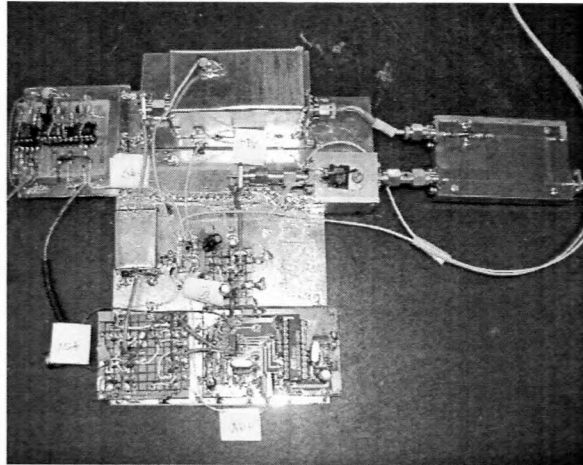


Figure 13.6: Photograph of Implemented System

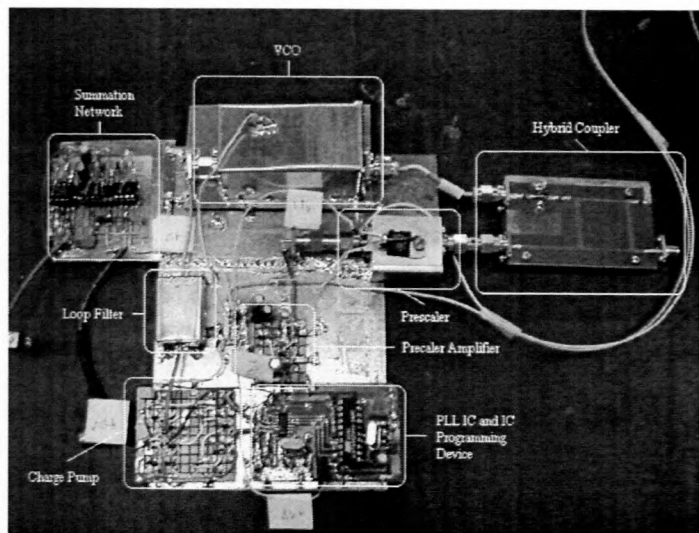


Figure 13.7: Photograph of Implemented System

## Chapter 14

# Synthesizer Measurements for Theoretical Verification

### INTRODUCTION

The aim of this section is to practically investigate the theoretical predictions of the various systems done in previous chapters. In each test section, either the loop gain or phase margin/damping factor will be varied for all the synthesizer types under investigation.

For the second-order system, three tests will be performed to observe the system's response to damping factor variations, while a fourth test will investigate the loop gain variation response. For the third- and fourth-order system, only three tests will be performed, where the first and second examines the effect of phase margins variations with the third exploring system response to loop gain variations.

For each system, only the results of the first conducted test will be discussed and the results of the succeeding tests shall be discussed at the end of the particular section.

## 14.1 Second-Order System

### 14.1.1 Second-Order System Test 1

The following synthesizer parameters are used:

$$\begin{aligned}
 \text{Damping Factor} &= 0.3 \\
 N &= 15680 \\
 K_{VCO} &= 77e6 \\
 K_{\phi} &= 5/4/\pi \\
 K_{sum} &= 2
 \end{aligned}$$

leading to the calculated values:

$$\begin{aligned}
 \text{Natural Frequency} &= 2.34 \text{ kHz} \\
 \text{Bandwidth} &= 21.4 \text{ kHz} \\
 \text{Rise Time} &= 102 \text{ us} \\
 C &= 10 \text{ nF} \\
 R &= 12 \text{ k}\Omega
 \end{aligned}$$

The filter frequency response shown in figure 14.1 a) predicts a reference suppression of 41 dB. Please note that this is not reference sideband suppression of the output spectrum (measured in dBc), but suppression of the reference frequency component of the control voltage by the loop filter (measured in dB). This prediction is possible due to the use of a voltage PFD where reference suppression is obtained only through the loop filter. Measurement of the filter input and output signal amplitudes revealed a physical reference suppression of 39 dB. This will produce a large reference frequency component on the control voltage applied to the VCO.

The system output spectrum with no externally applied modulation is shown in figure 14.1 b) from which it is evident that this system will not be applicable for narrow bandwidth systems. This is due to the wideband modulation produced by the combination of low loop filter reference suppression and high VCO gain. The output spectrum is easily justified by noting that a reference suppression of only 39 dB is measured. It must also be noted that the output signal from the PFD does not have a dynamic range of 5 V when the system is phase-locked, but in fact generates 3.8 V (measured) corrective pulses. Combining these elements with the summation network produces a VCO modulating signal of 85.2 mV which, when multiplied by the VCO gain, generates a VCO deviation of 6.56 MHz corresponding to the maximum deviation of the output spectrum.



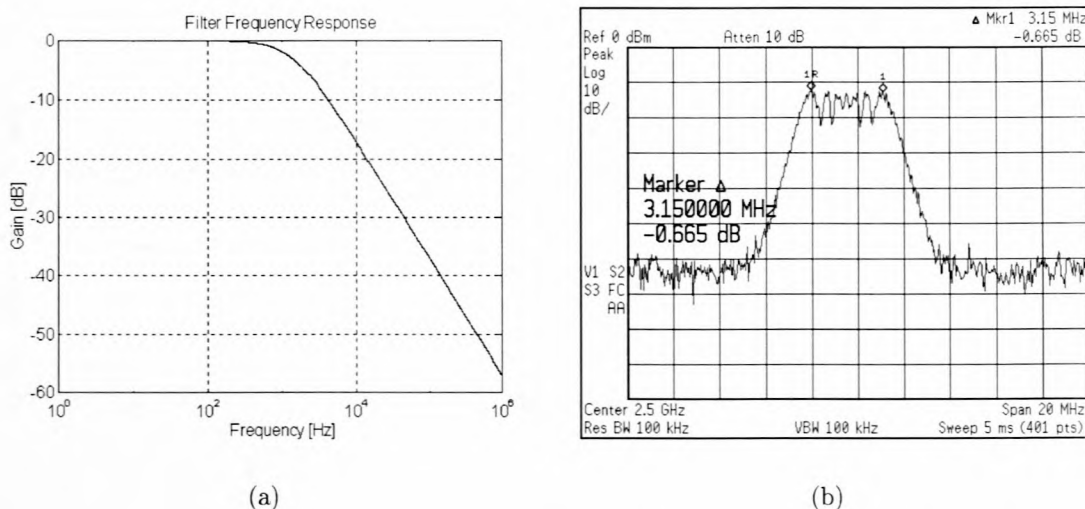


Figure 14.1: **a)** Frequency Response of Second-Order System Loop Filter **b)** Output Spectrum of Second-Order Synthesizer Without External Modulation

The measured and simulated settling time results are shown in figure 14.2, where graph b) is the VCO control voltage corresponding to the output frequency. Visual comparison verifies the correlation between the theoretical and practical results. Figure 14.2 b) also shows the characteristic ringing effect of an underdamped system on the VCO control signal.

The cursor appearing on figure 14.2 b), placed on the theoretical rise time prediction, confirms the prediction validity. The prediction, although seemingly accurate, is crude and does not produce an accurate prediction of the synthesizer settling time, which is crucial to any synthesizer design. Therefore it is only useful to determine the speed at which the final frequency will be reached, but conveys no accurate information regarding the settling time. Using graph 14.2 b), a 1 ms settling time for the system is measured. More accurate settling time results require instruments which are able to graph frequency against time.

As modulation of the VCO due to an externally applied signal is of interest, figure 14.3 shows this characteristic as well as the measured VCO deviation. For low modulation frequencies, the loop compensates and is able to attenuate the modulation signal (or disturbance) severely producing low VCO output frequency deviations. With increasing modulation frequency, the corrective ability of the loop deteriorates, thus increasing the

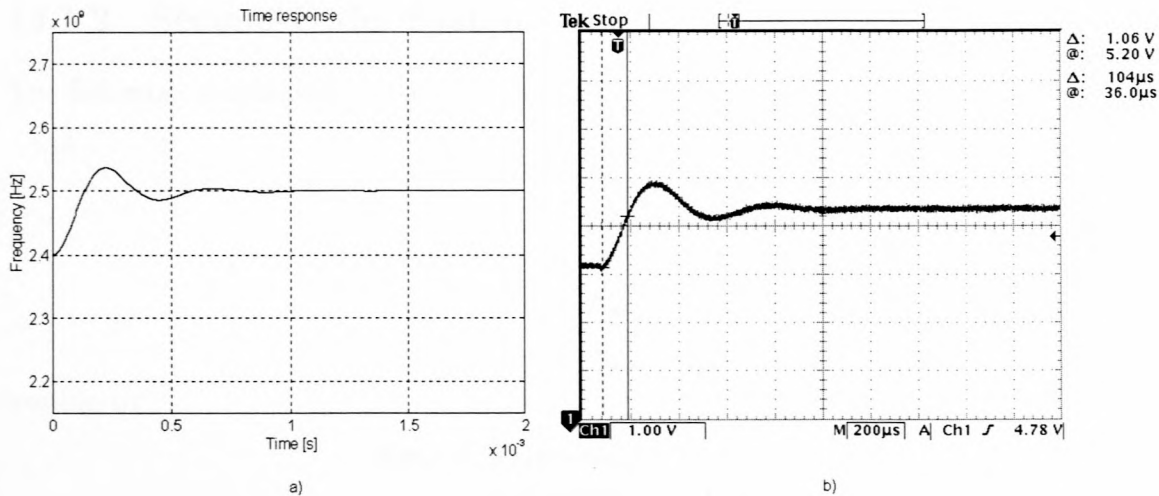


Figure 14.2: Settling Time of Second-Order System

deviation of the VCO output frequency until the modulation frequency reaches the loop bandwidth. No correction by the loop is possible above the loop bandwidth and the modulation signal is transferred to the VCO without any attenuation. If care is not taken during the selection of the loop bandwidth, the peaking phenomenon observed on the graph could lead to over modulation of the VCO and increase transmission bandwidth. The variation between measured and simulated data is almost negligible, thus confirming the accuracy of the theoretical predictions.

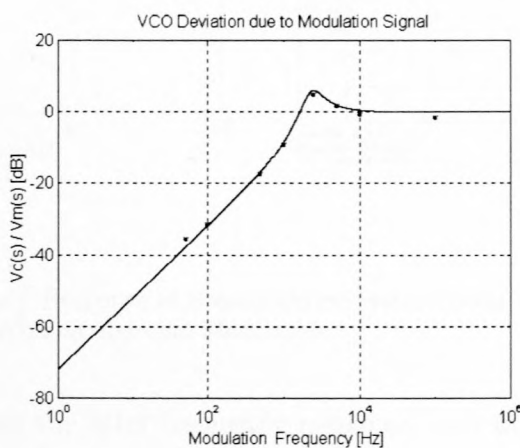


Figure 14.3: VCO Deviation Due to Modulation Signal

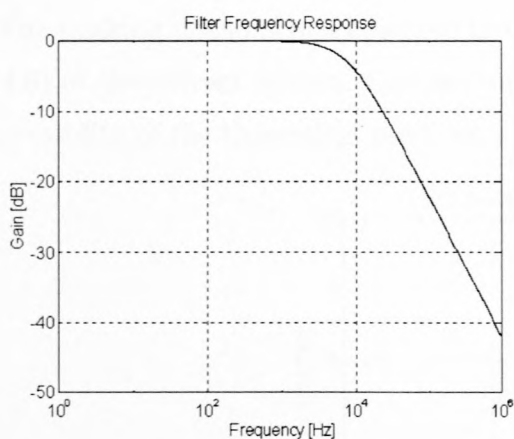
### 14.1.2 Second-Order System Test 2

The following synthesizer parameters are used:

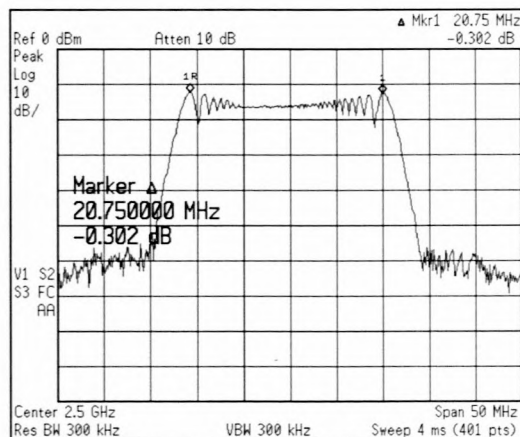
$$\begin{aligned} \text{Damping Factor} &= 0.707 \\ N &= 15680 \\ K_{VCO} &= 77e6 \\ K_{\phi} &= 5/4/\pi \\ K_{sum} &= 2 \end{aligned}$$

leading to:

$$\begin{aligned} \text{Natural Frequency} &= 5.53 \text{ kHz} \\ \text{Bandwidth} &= 34.7 \text{ kHz} \\ \text{Rise Time} &= 63.6 \text{ us} \\ C &= 10 \text{ nF} \\ R &= 2 \text{ k}\Omega \end{aligned}$$



(a)



(b)

Figure 14.4: **a)** Frequency Response of Second-Order System Loop Filter **b)** Output Spectrum of Second-Order Synthesizer Without External Modulation

Figure 14.4 a) displays the filter frequency response, indicating a theoretical reference suppression of 25 dB while b) shows the system output spectrum with no externally applied modulation. Using the same technique as Test 1, a reference suppression of 24.5 dB is measured.



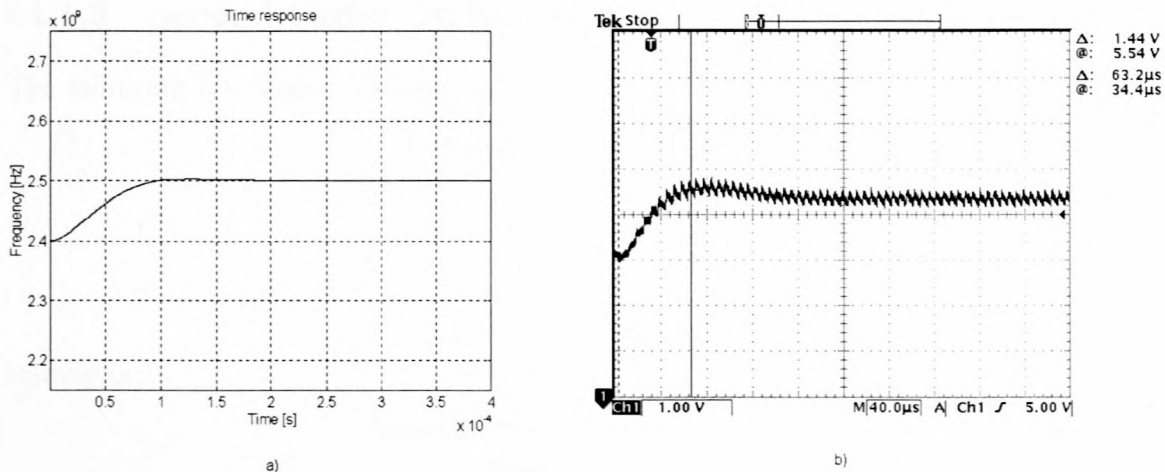


Figure 14.5: Settling Time of Second-Order System

The settling time prediction is verified with the measurement taken from the practical circuit. Using the measurement graph, a settling time of 250  $\mu$ s is obtained.

The peaking phenomenon observed in test 1 is also visible on the VCO deviation graph (14.6) of the current system. Comparison of the measured and simulated results confirm the validity of the theoretical prediction.

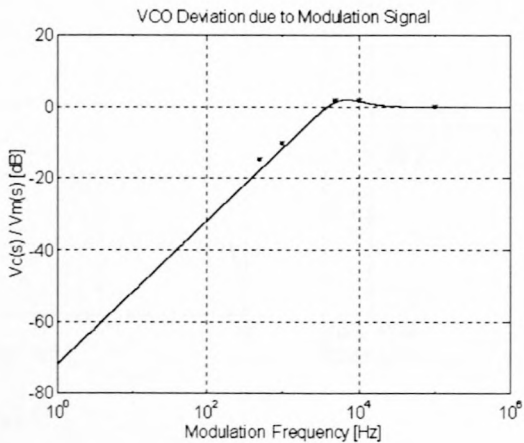


Figure 14.6: VCO Deviation Due to Modulation Signal

### 14.1.3 Second-Order System Test 3

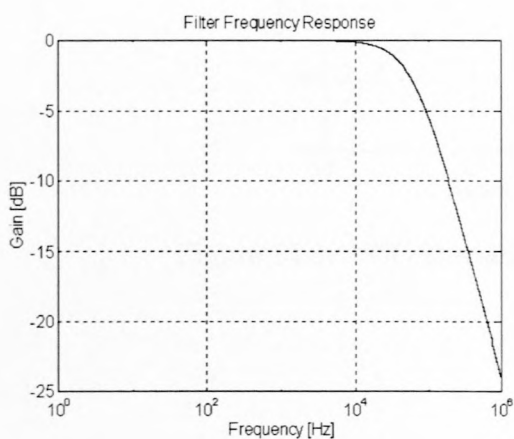
The following synthesizer parameters are used:

$$\begin{aligned}
 \text{Damping Factor} &= 2 \\
 N &= 15680 \\
 K_{VCO} &= 77e6 \\
 K_{\phi} &= 5/4/\pi \\
 K_{sum} &= 2
 \end{aligned}$$

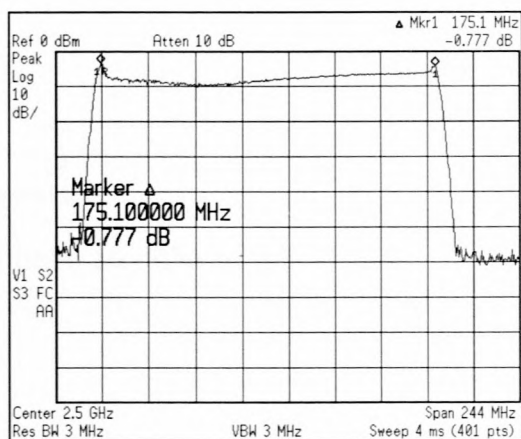
leading to:

$$\begin{aligned}
 \text{Natural Frequency} &= 15.6 \text{ kHz} \\
 \text{Bandwidth} &= 26.2 \text{ kHz} \\
 \text{Rise Time} &= 84 \text{ us} \\
 C &= 10 \text{ nF} \\
 R &= 255 \text{ } \Omega
 \end{aligned}$$

Reference suppression measurement indicate the achievement of 12 dB suppression for a prediction of 12.5 dB. This system also achieves a measured settling time of 200 us.



(a)



(b)

Figure 14.7: a) Frequency Response of Second-Order System Loop Filter b) Output Spectrum of Second-Order Synthesizer Without External Modulation

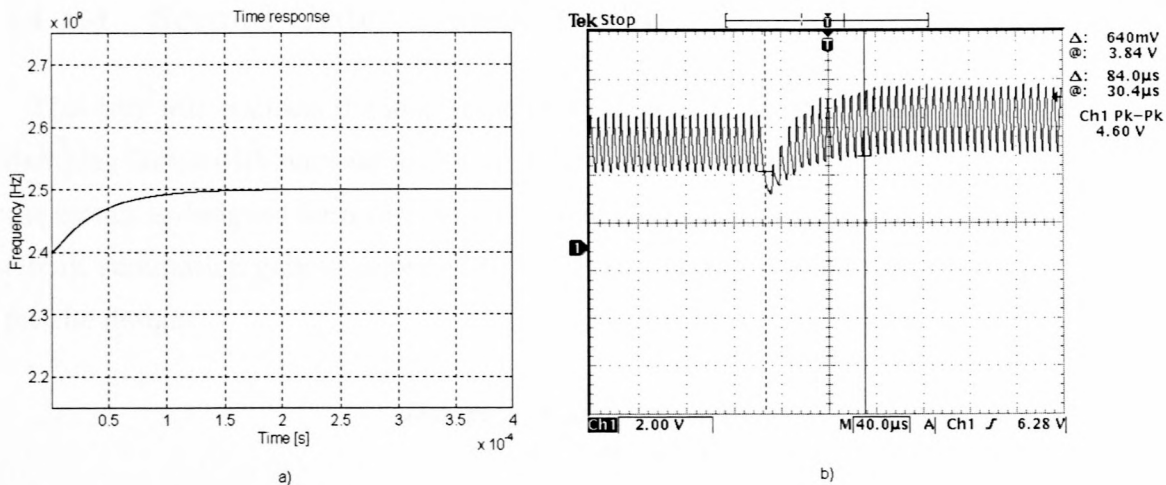


Figure 14.8: Settling Time of Second-Order System

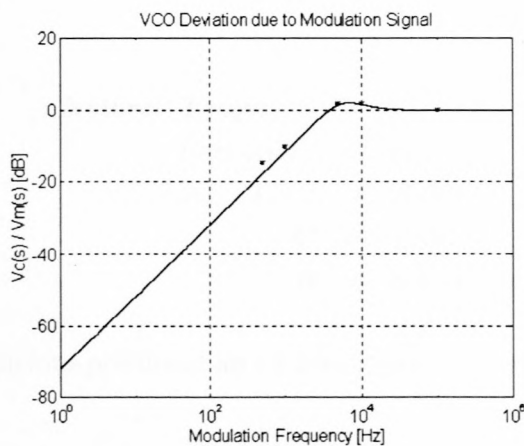


Figure 14.9: VCO Deviation Due to Modulation Signal



#### 14.1.4 Second-Order System Test 4

This test will evaluate the loop response to loop gain variations. For this test a critical damping factor with increase loop gain is used. To further test the theoretical predictions, the circuit is designed for a summation gain of 5 instead of the normal 2, but the practical circuit summation gain is increased to 10. The following synthesizer parameters are used for the design:

$$\begin{aligned}
 \text{Damping Factor} &= 0.707 \\
 N &= 15680 \\
 K_{VCO} &= 77e6 \\
 K_{\phi} &= 5/4/\pi \\
 K_{sum} &= 5
 \end{aligned}$$

leading to:

$$\begin{aligned}
 \text{Natural Frequency} &= 13.8 \text{ kHz} \\
 \text{Bandwidth} &= 86.8 \text{ kHz} \\
 \text{Rise Time} &= 25.3 \text{ us} \\
 C &= 1 \text{ nF} \\
 R &= 8.2 \text{ k}\Omega
 \end{aligned}$$

Theoretically the simulations predicted an 18 dB suppression while an 18.4 dB suppression is obtained.

This design is a reminder that all loop component limitations must be kept in mind at all times. To achieve the increased loop gain, the gain of an operation amplifier is increased. This has the effect of lowering the operational amplifier bandwidth to such an extent that loop functionality becomes compromised. Earlier in the study it was mentioned that any pole introduced into the loop must be ten times higher than the loop bandwidth to prevent loop performance degradation. For this design the loop bandwidth is 86.8 kHz, while the bandwidth of the operational amplifier with a gain of 10 is obtained (using datasheets) as 400 kHz which will definitely influence synthesizer performance.

By incorporating this pole into the theoretical prediction, the total loop filter frequency response is shown in figure 14.10 a). This figure shows an expected reference suppression of 18.7 dB while an 18.4 dB suppression is measured. A settling time of 150 us is also measured for the configuration under discussion.

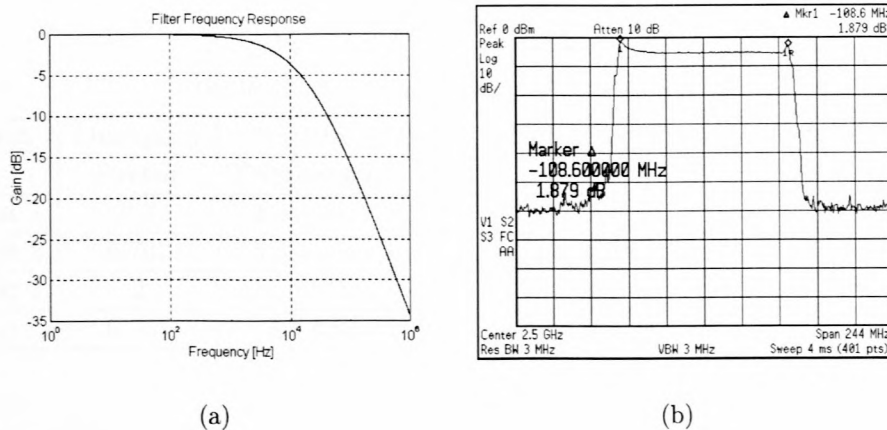


Figure 14.10: **a)** Frequency Response of Second-Order System Loop Filter **b)** Output Spectrum of Second-Order Synthesizer Without External Modulation

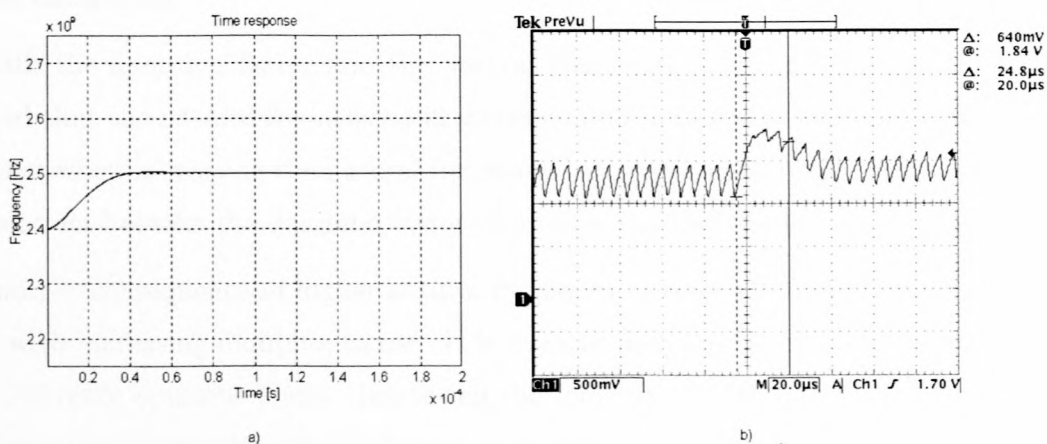


Figure 14.11: Settling time of Second-Order System

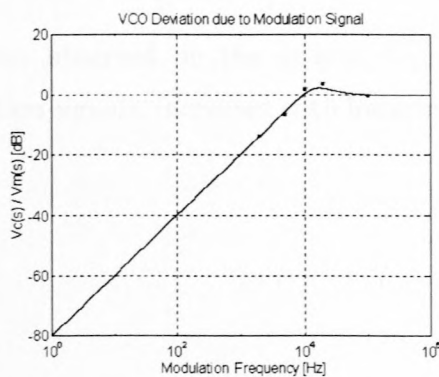


Figure 14.12: VCO Deviation Due to Modulation Signal

## 14.2 Second-Order System Synopsis

Table 14.1: Second-Order Test Results

Test	Damping Factor	Natural Frequency	$K_{sum}$	Settling Time	Reference Suppression
Test 1	0.3	2.34 kHz	2	1 ms	39 dB
Test 2	0.707	5.53 kHz	2	250 us	25 dB
Test 3	2	15.6 kHz	2	200 us	12 dB
Test 4	0.707	13.8 kHz	10	150 us	18 dB

The low loop filter reference suppression causes modulation of the VCO resulting in increased signal bandwidth. Application of an external modulation signal will further increase VCO output frequency deviation and thus increase the required transmission signal bandwidth.

With the damping factor and the natural frequency interdependence, it is to be expected that the natural frequency will increase with increasing damping factor. The first instinct when increasing the natural frequency is to assume decreased settling time. This is incorrect because the damping factor also has a significant effect on settling times.

Another consequence of higher natural frequency is the reduction of reference suppression with increasing damping factor. This leads to increased output spectrum bandwidth and reference spurious levels. Increasing the loop bandwidth also increases the natural frequency and thus decreasing reference suppression.

Settling time is effectively reduced by increasing damping factor as well as loop gain again due to the increased natural frequency.

The peaking phenomenon observed on the graphs depicting VCO deviation due to externally applied modulation signals, increases with lowering synthesizer damping factor.



## 14.3 Third-Order System

### 14.3.1 Third-Order System Test 1

The following synthesizer parameters are used:

$$\begin{aligned}
 \textit{Phase Margin} &= 30 \textit{ Degrees} \\
 \textit{Natural Frequency} &= 500\textit{Hz} \\
 N &= 15360 \\
 K_{VCO} &= 77e6 \\
 K_{\phi} &= 5/2/\pi \\
 K_{sum} &= 1
 \end{aligned}$$

This leads to the calculated values:

$$\begin{aligned}
 R1 &= 47 \textit{ k}\Omega \\
 C1 &= 100 \textit{ nF} \\
 R2 &= 3.9 \textit{ k}\Omega \\
 C2 &= 47 \textit{ nF}
 \end{aligned}$$

The filter frequency response is shown in figure 14.13 a) where reference suppression prediction difficulty is increased due to the integration action of the active loop filter. The integration action causes the IC to generate corrective pulses with the output only being active for a short period. This results in the generation of narrow corrective pulses leading to improved reference suppression. A reference suppression of 63.9 dB is measured for this system (This is still the attenuation of the reference frequency component on the control voltage to the VCO [Measured in dB]). The output spectrum without external modulation, shown in figure 14.13 b), indicates the increase reference suppression. The only means of utilizing this signal as a FM carrier is to incorporate a high-pass filter at the demodulator output to remove the reference frequency component.

During synthesizer locking, an interesting event is observed on the VCO control line shown in figure 14.14. The measured graph shows a constant charging slope not observed in the simulation results. Through closer inspection the average output voltage of the PFD is 2.5 V due to the long charging time of C1, thus producing a C1 charging current of 56  $\mu\text{A}$  through  $R_1$ . Calculations revealed that the capacitor voltage will increase with 3 V in 3 ms explaining the constant charging slope of the loop filter output. It should also be noted that a similar discharging slope is observed on the control signal. Taking

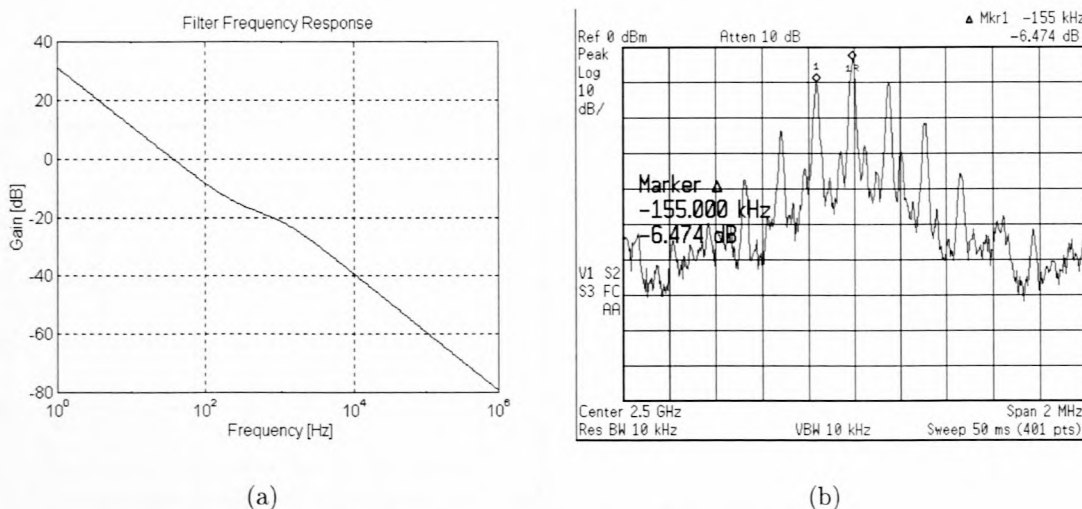


Figure 14.13: a) Frequency Response of Third-Order System Loop Filter b) Output Spectrum of Third-Order Synthesizer Without External Modulation

the above into consideration it seems that the settling time simulation is only valid if the capacitor charging characteristic can be incorporated into the simulation. This subject will not be addressed in this study as time domain simulations are required. A 6 ms settling time is measured for this configuration.

Deviation of the VCO, shown in figure 14.15 a), exhibits the same general characteristics as seen in the second-order systems. Apart from VCO modulation, phase deviation caused by application of the modulation signal is also investigated for this configuration. The simulated phase deviation along with the measured data is shown in figure 14.15 b). This graph shows the phase variation of the feedback signal at the input to the PFD. For low modulation frequencies an almost constant phase variation is obtained as the loop compensates for the modulation signal. For frequencies near the loop bandwidth, a peaking phenomenon is observed while no compensation is possible for modulation signal frequencies above the loop bandwidth and no phase variation observable.

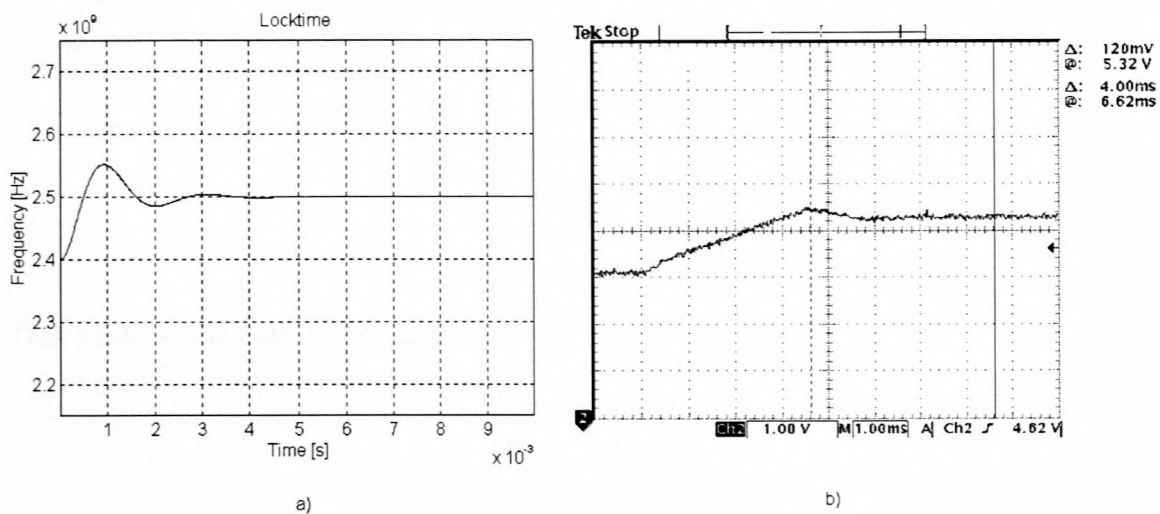


Figure 14.14: Settling Time of Third-Order System

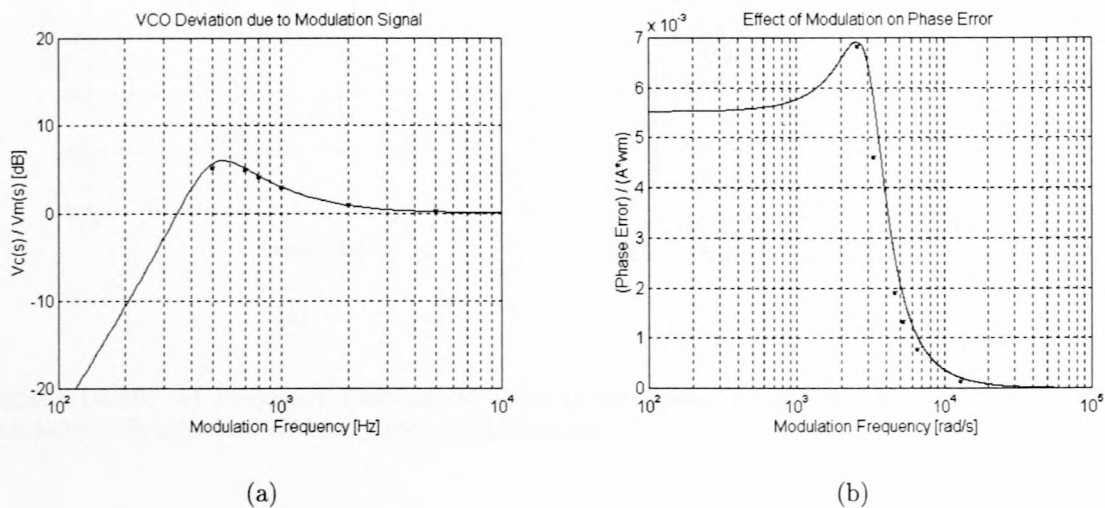


Figure 14.15: a) VCO Deviation Due to Modulation Signal b) Phase Deviation Due to Modulation Signal



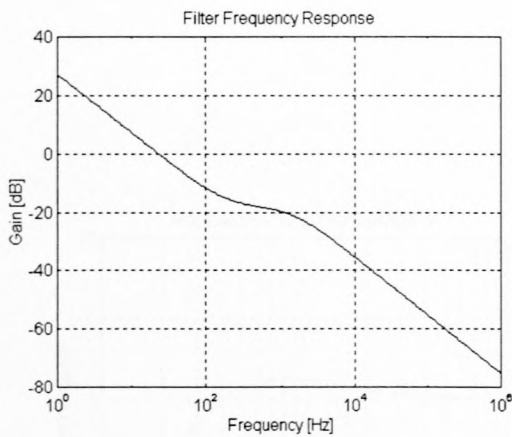
### 14.3.2 Third-Order System Test 2

The following synthesizer parameters are used:

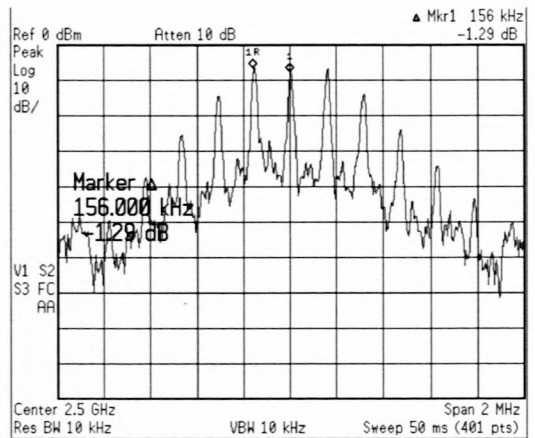
$$\begin{aligned}
 \text{Phase Margin} &= 50 \text{ Degrees} \\
 \text{Natural Frequency} &= 500\text{Hz} \\
 N &= 15360 \\
 K_{VCO} &= 77e6 \\
 K_{\phi} &= 5/2/\pi \\
 K_{sum} &= 1
 \end{aligned}$$

This leads to the calculated values:

$$\begin{aligned}
 R1 &= 70 \text{ k}\Omega \\
 C1 &= 100 \text{ nF} \\
 R2 &= 7.6 \text{ k}\Omega \\
 C2 &= 15 \text{ nF}
 \end{aligned}$$

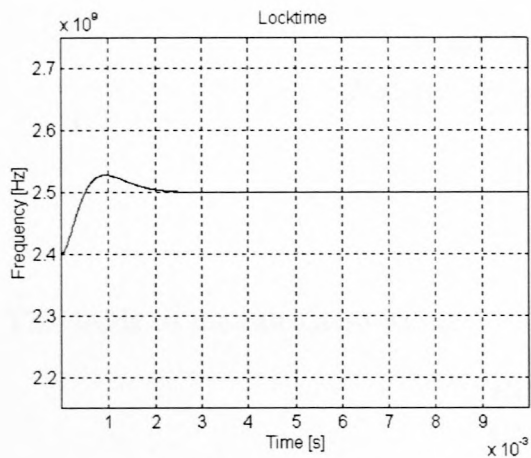


(a)

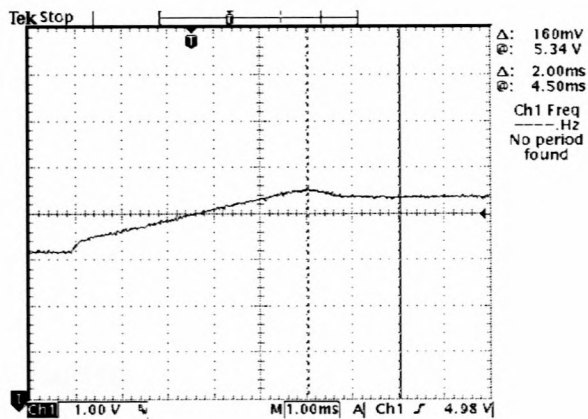


(b)

Figure 14.16: **a)** Frequency Response of Third-Order System Loop Filter **b)** Output Spectrum of Third-Order Synthesizer Without External Modulation

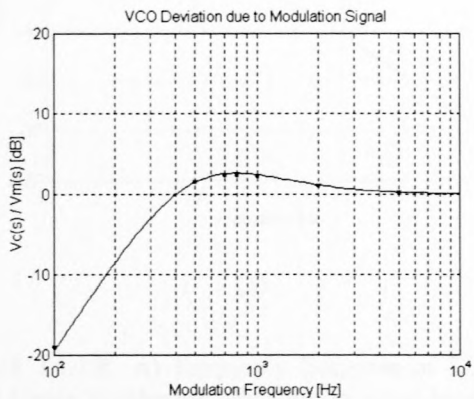


a)

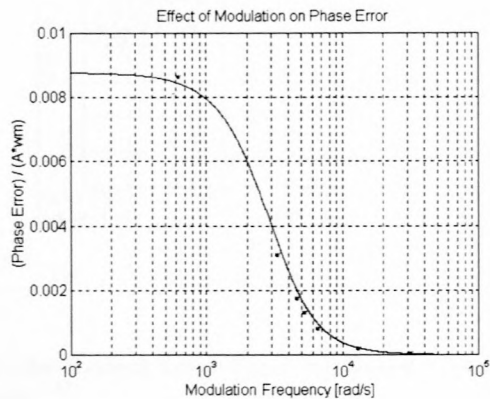


b)

Figure 14.17: Settling Time of Third-Order System



(a)



(b)

Figure 14.18: a) VCO Deviation Due to Modulation Signal b) Phase Deviation Due to Modulation Signal

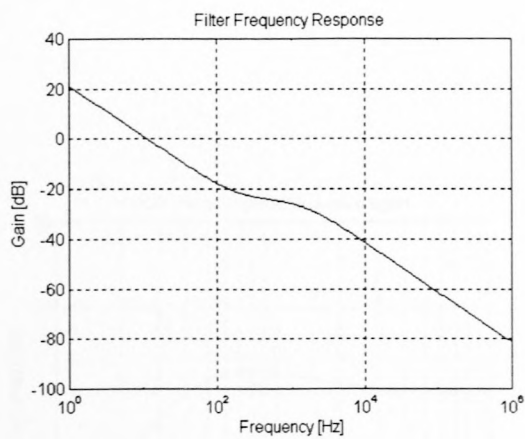
### 14.3.3 Third-Order System Test 3

The following synthesizer parameters are used:

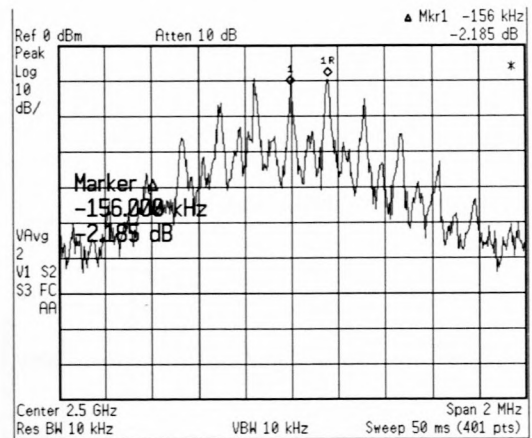
$$\begin{aligned} \text{Phase Margin} &= 50 \text{ Degrees} \\ \text{Natural Frequency} &= 500 \text{ Hz} \\ N &= 15360 \\ K_{VCO} &= 77e6 \\ K_{\phi} &= 5/2/\pi \\ K_{sum} &= 2 \end{aligned}$$

This leads to the calculated values:

$$\begin{aligned} R1 &= 150 \text{ k}\Omega \\ C1 &= 100 \text{ nF} \\ R2 &= 7.6 \text{ k}\Omega \\ C2 &= 15 \text{ nF} \end{aligned}$$



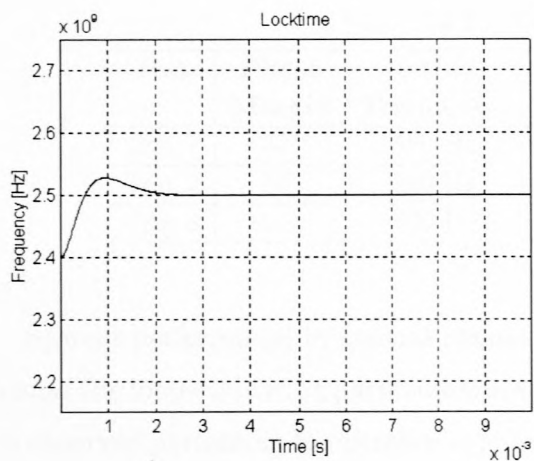
(a)



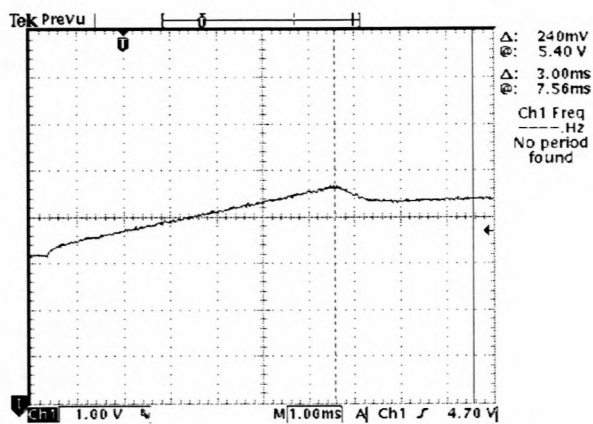
(b)

Figure 14.19: a) Frequency Response of Third-Order System Loop Filter b) Output Spectrum of Third-Order Synthesizer Without External Modulation



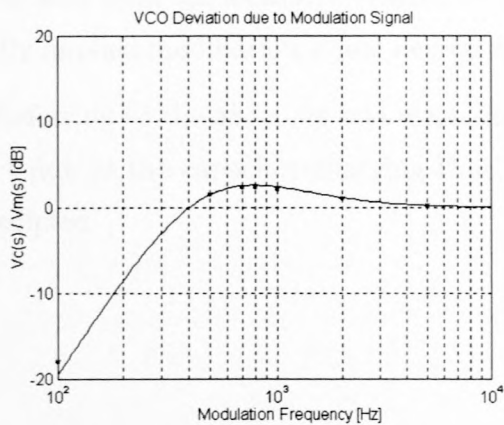


a)

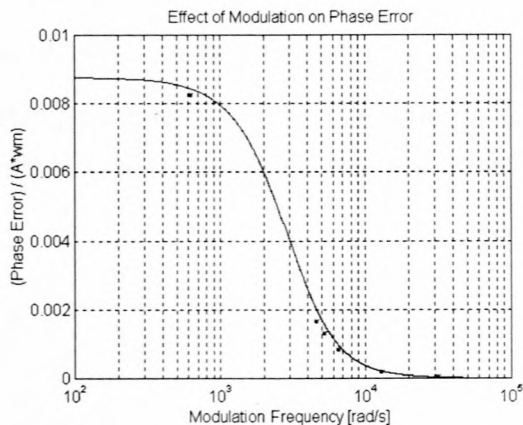


b)

Figure 14.20: Settling Time of Third-Order System



(a)



(b)

Figure 14.21: a) VCO Deviation Due to Modulation Signal b) Phase Deviation Due to Modulation Signal

## 14.4 Third-Order System Synopsis

Table 14.2: Third-Order Test Results

Test	Phase Margin	Natural Frequency	$K_{\text{sum}}$	Settling Time	Reference Suppression
Test 1	30°	500 Hz	1	6 ms	64 dB
Test 2	50°	500 Hz	1	7.5 ms	57 dB
Test 3	50°	500 Hz	2	8.5 ms	64 dB

System performance in general cannot be compared to second-order system results because the loop evaluation parameters are not identical. In spite of this, a vast improvement is observed pertaining to reference suppression leading to reduced transmission bandwidth. The integration action of the loop filter causes the loop to respond differently compared to the second-order system response. Phase Margin increase causes a decrease in reference suppression and increased transmission bandwidth. Loop gain increase now has the effect of increasing reference suppression.

Increasing the phase margin causes an increase in the settling times. Settling time is also negatively affected with increased synthesizer loop gain.

As seen from the measured results, VCO and phase deviation peaking due to the externally applied modulation signal decreases with increasing phase margin.

Referring to the above, it is evident that although the settling time prediction is incorrect due to the capacitor charging time, the other system characteristics are accurately predicted.

## 14.5 Fourth-Order System

### 14.5.1 Fourth-Order System Test 1

The following synthesizer parameters are used:

$$\begin{aligned}
 \text{Phase Margin} &= 20 \\
 \text{Loop Bandwidth} &= 9.5\text{kHz} \\
 N &= 15680 \\
 K_{VCO} &= 77\text{e6} \\
 K_{\phi} &= 5 * 2 * \pi \text{ mA} \\
 K_{sum} &= 1
 \end{aligned}$$

This leads to the calculated values:

$$\begin{aligned}
 \text{ATTEN} &= 24.5358 \\
 C_1 &= 12 \text{ nF} \\
 C_2 &= 47 \text{ nF} \\
 C_3 &= 120 \text{ pF} \\
 R_2 &= 390 \ \Omega \\
 R_3 &= 36 \text{ k}\Omega
 \end{aligned}$$

Figure 14.22 a) shows the simulated open-loop gain of the system, thus predicting the achievement of the required 9.5 kHz loop bandwidth.

The filter frequency response, shown in figure 14.22 b), shows a reference frequency gain of 33 dB. This is in fact a gain factor to obtain the VCO control voltage from the charge pump current, thus 5 mA will produce 230 mV on the VCO control line. This statement is only true if a sinusoidal charge pump current was used, but due to the fact that only corrective pulses are generated, increased reference suppression is achieved. The use of a charge pump complicates reference suppression prediction as current amplitude and pulse duration are the determining factors.

Figure 14.23 shows the measured reference sideband level as -44.4 dBc. Note that this measurement is performed using a spectrum analyzer (measured in dBc).

Measured and simulated settling times are shown in figure 14.24 where the capacitor charging slope is observed again. The system settling time is obtained as 550 us using the measured graph. Due to the low phase margin, the characteristic ringing effect of the system is clearly noticeable. To show the improved performance of this system over



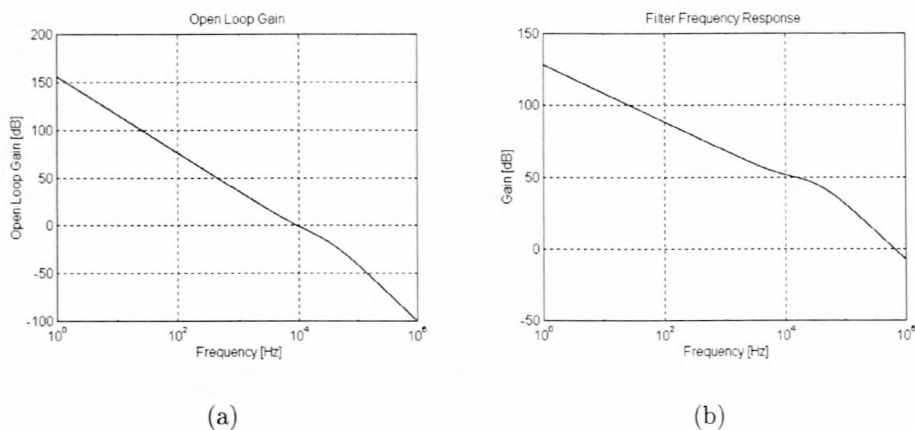


Figure 14.22: **a)** Open-Loop Gain of Fourth-Order System **b)** Frequency Response of Fourth-Order System Loop Filter

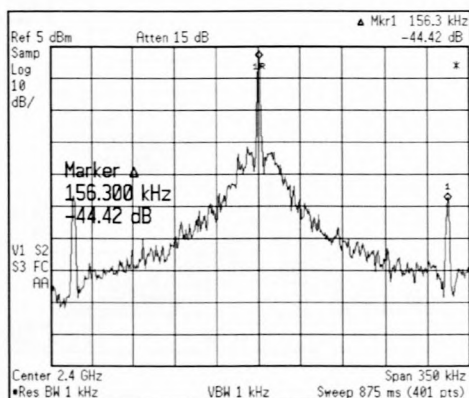


Figure 14.23: Output Spectrum of Fourth-Order Synthesizer Without External Modulation

previous systems, refer to the output signal spectrum measurements shown in figures 14.25 and 14.23. The first figure shows the clean spectrum obtained for a wide spectrum analyzer span and resolution bandwidth, while the second shows the obtained reference suppression level.

Figure 14.26 a) shows the modulation of the VCO along with the measured VCO deviation results. The variation between measured and simulated data is almost negligible, thus confirming the accuracy of the prediction.

As with the third-order system, the phase deviation caused by the modulation signal is investigated. Figure 14.26 b) shows the simulated and measured results of the phase deviation. The results again verify the prediction validity.

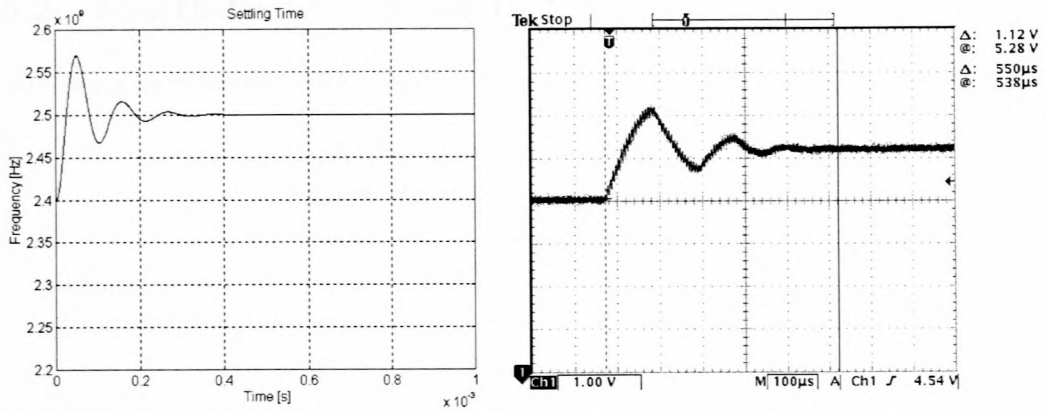


Figure 14.24: Settling Time of Fourth-Order System

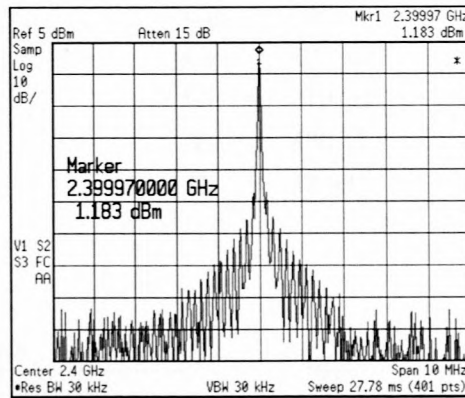


Figure 14.25: Output Spectrum of Fourth-Order Synthesizer Without External Modulation

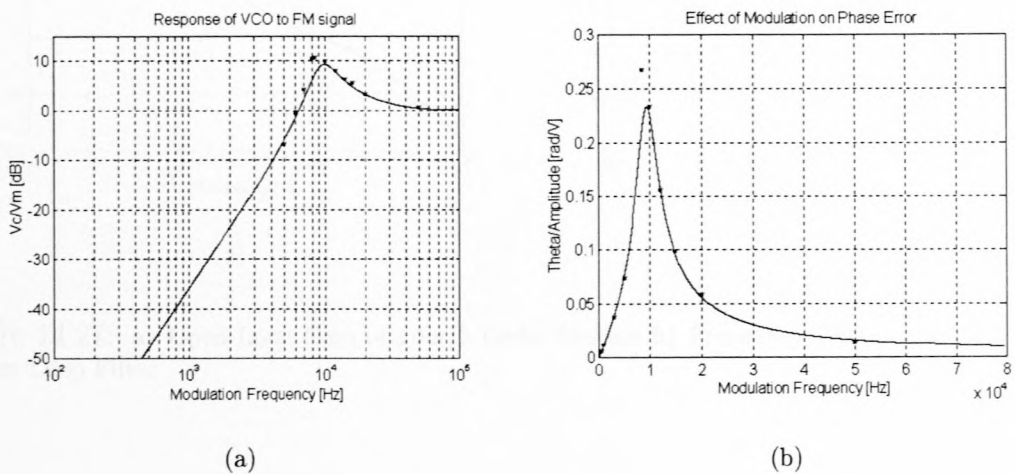


Figure 14.26: a) Modulation of VCO due to Modulating Signal b) Phase Deviation Due to Modulation Signal

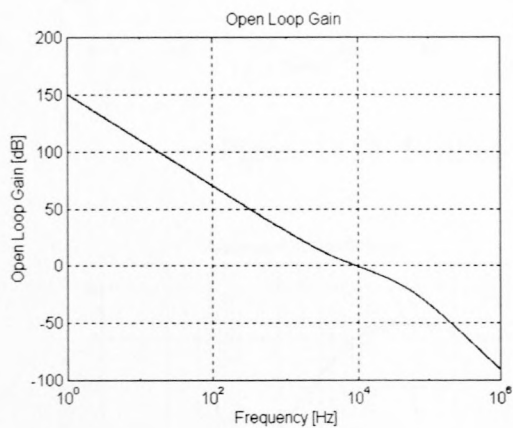
## 14.5.2 Fourth-Order System Test 2

The following synthesizer parameters are used:

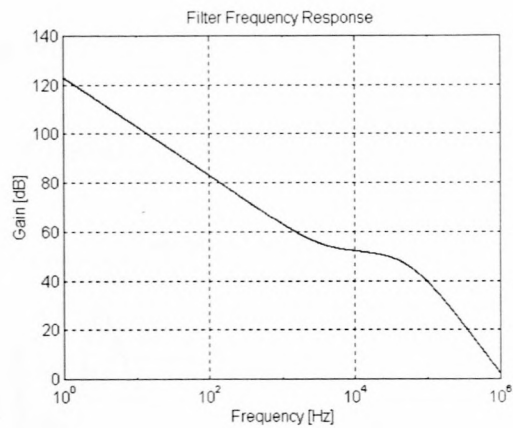
$$\begin{aligned} \text{Phase Margin} &= 50 \\ \text{Loop Bandwidth} &= 9.5\text{kHz} \\ N &= 15680 \\ K_{VCO} &= 77e6 \\ K_{\phi} &= 5 * 2 * \pi \text{ mA} \\ K_{sum} &= 1 \end{aligned}$$

This leads to the calculated values:

$$\begin{aligned} \text{ATTEN} &= 15.97 \\ C_1 &= 6.8 \text{ nF} \\ C_2 &= 100 \text{ nF} \\ C_3 &= 270 \text{ pF} \\ R_2 &= 430 \text{ } \Omega \\ R_3 &= 12 \text{ k}\Omega \end{aligned}$$



(a)



(b)

Figure 14.27: **a)** Open-Loop Gain of Fourth-Order System **b)** Frequency Response of Fourth-Order System Loop Filter



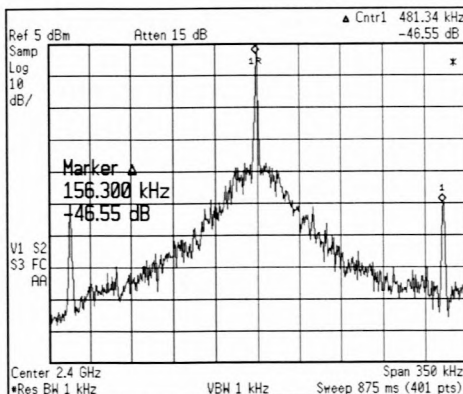


Figure 14.28: Output Spectrum of Fourth-Order Synthesizer Without External Modulation

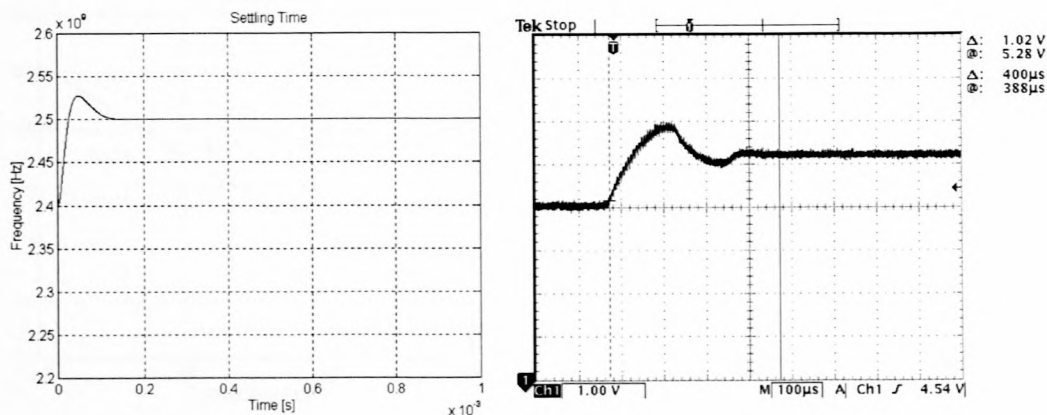


Figure 14.29: Settling Time of Fourth-Order System

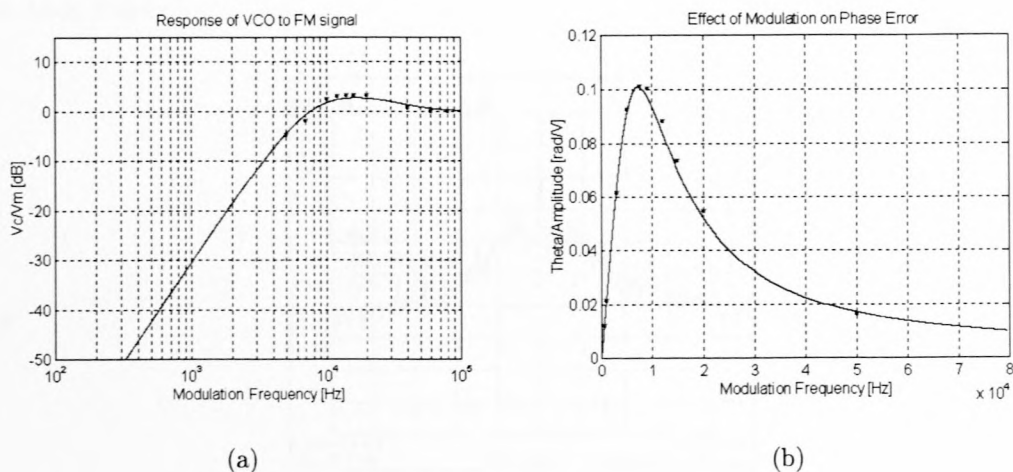


Figure 14.30: a) Modulation of VCO due to Modulating Signal b) Phase Deviation Due to Modulation Signal

### 14.5.3 Fourth-Order System Test 3

For this test, the same loop filter as Test 2 of this section is used. The synthesizer loop gain is varied by simply doubling the summation gain.

$$\begin{aligned}
 ATTEN &= 15.97 \\
 C_1 &= 6.8 \text{ nF} \\
 C_2 &= 100 \text{ nF} \\
 C_3 &= 270 \text{ pF} \\
 R_2 &= 430 \text{ } \Omega \\
 R_3 &= 12 \text{ k}\Omega
 \end{aligned}$$

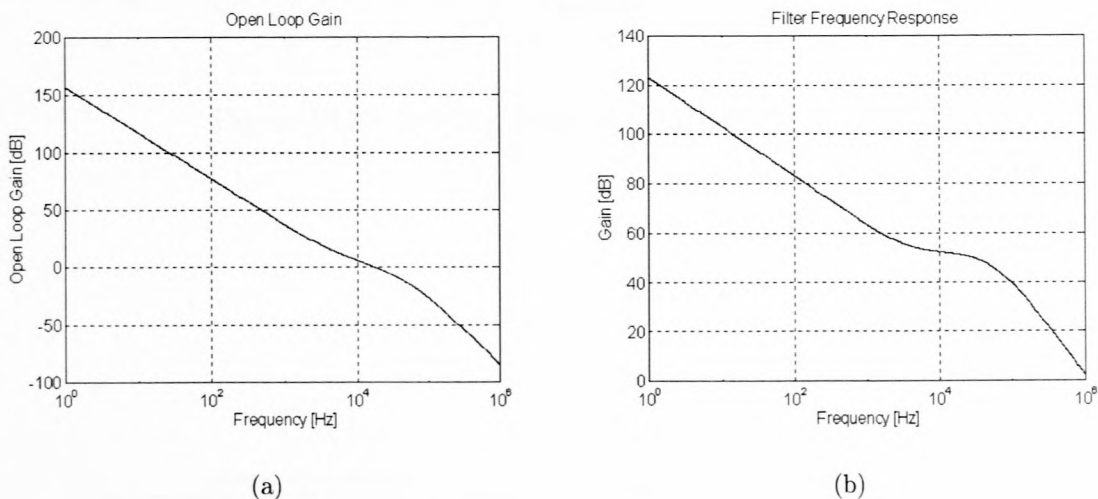


Figure 14.31: a) Open-Loop Gain of Fourth-Order System b) Frequency Response of Fourth-Order System Loop Filter

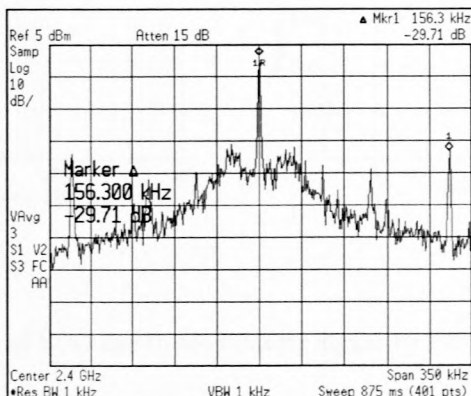


Figure 14.32: Output Spectrum of Fourth-Order Synthesizer Without External Modulation

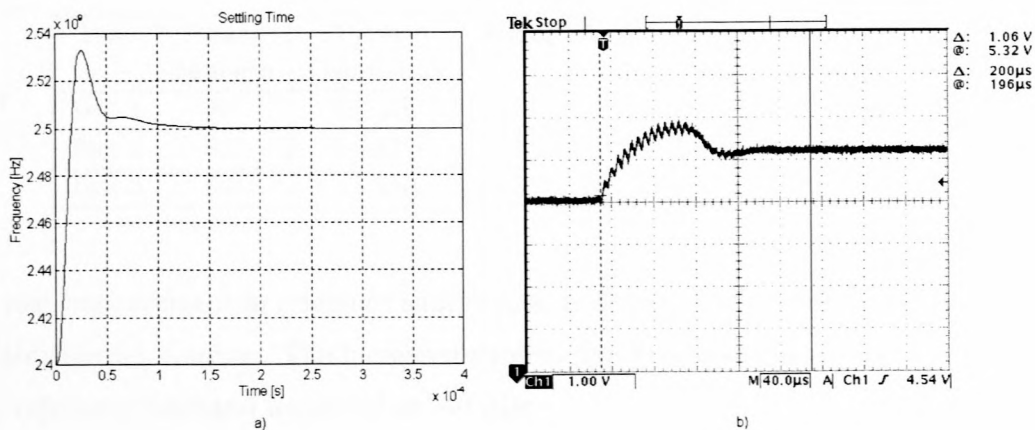


Figure 14.33: Settling Time of Fourth-Order System

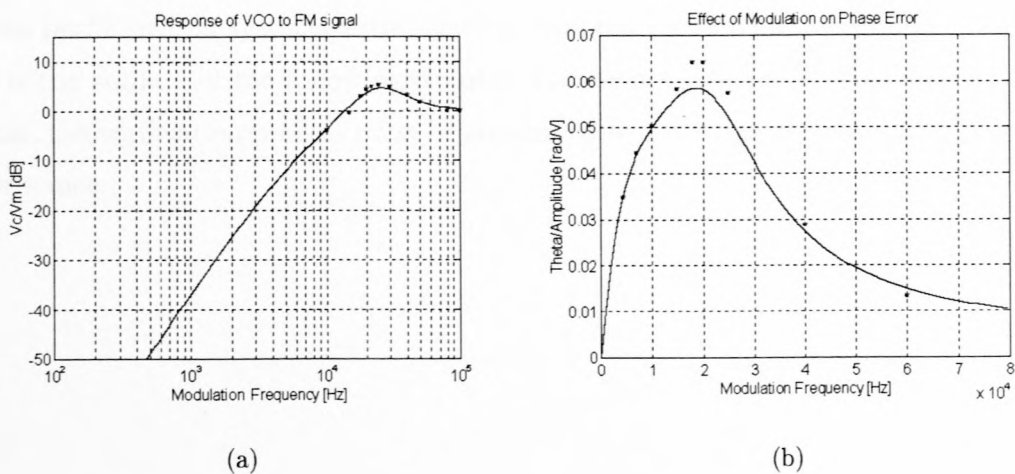


Figure 14.34: a) Modulation of VCO due to Modulating Signal b) Phase Deviation Due to Modulation Signal

#### 14.5.4 Fourth-Order System Synopsis

Table 14.3: Fourth-Order Test Results

Test	Phase Margin	Natural Frequency	$K_{\text{sum}}$	Settling Time	Reference Suppression
Test 1	20°	9.5 kHz	1	550 $\mu\text{s}$	-44.4 dBc
Test 2	50°	9.5 kHz	1	400 $\mu\text{s}$	-46.5 dBc
Test 3	50°	9.5 kHz	2	200 $\mu\text{s}$	-29.7 dBc

A vast improvement in reference suppression is observed when compared to the second- and third-order systems. The increased suppression produces clean carrier output signals with reference sideband levels below -40 dBc.

With increasing phase margin the measurements show a reduction of settling times and increased reference suppression. VCO deviation peaking due to the modulation signal decreases as with increasing phase margin. Increasing the loop gain causes reference suppression decrease along with a reduction of settling time.

The theoretical prediction for all the proposed systems is very accurate in all cases except for settling time, thus leading to the conclusion that further system analysis can be performed using these theoretical predictions only. The final system comparison will thus be performed on systems with identical loop parameters on a theoretical basis only. This is the subject of the following chapter, but before continuing with the comparison process, the verification process must be concluded by investigating the summing network performance.



## 14.6 Measurement of High Frequency Summing Network

Functional verification of the summing network is performed by applying a modulation signal using a high frequency signal generator with a  $50 \Omega$  output impedance to the summing network integrated into a fourth-order system. Since a high frequency demodulator is not available, comparison of the output spectrum with a calculated FM spectrum (using Bessel functions) is the only verification method. Refer to Appendix I for the detailed discussion on the FM spectrum calculation.

Figures 14.35, 14.36 and 14.37 show the measured and calculated output spectra for modulation frequencies of 10 MHz, 20 MHz and 40 MHz respectively. A modulation signal power level of -20 dBm is used for verification. Table 14.4 shows the calculated modulation signal power level required to produce the exact measured spectra. The table verifies that the simulated and measured performance is almost identical if measurement accuracy tolerance is taking in account. This test validates the summation network functionality as well as the wideband FM generation capability of the system.

Table 14.4: Comparison of Applied and Required Modulation Power Levels

Modulation Frequency	Applied Signal Power	Simulated Signal Power to Produce Measured Spectrum
10 MHz	-20 dBm	-18.6 dBm
20 MHz	-20 dBm	-20.5 dBm
40 MHz	-20 dBm	-19.9 dBm

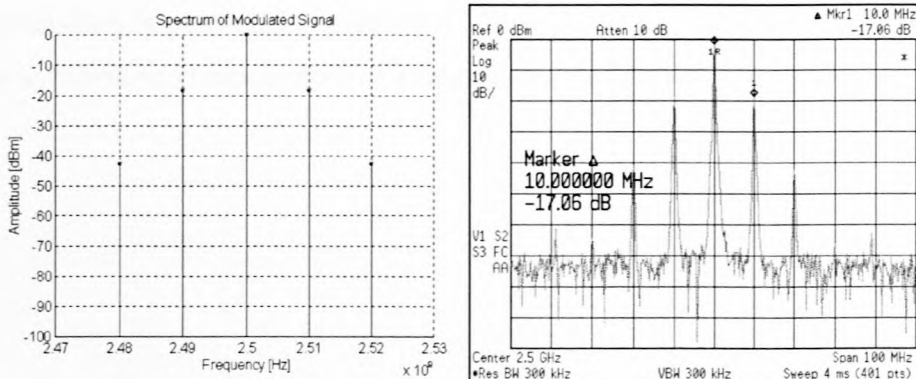


Figure 14.35: Output Spectrum of Fourth-Order Synthesizer with High Frequency FM Modulation

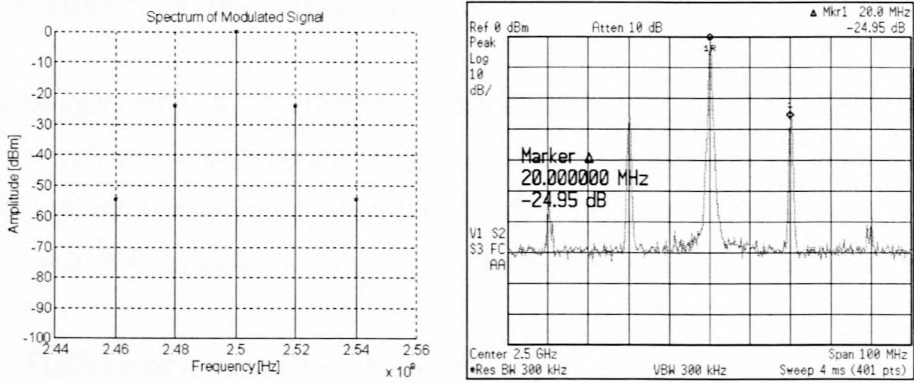


Figure 14.36: Output Spectrum of Fourth-Order Synthesizer with High Frequency FM Modulation

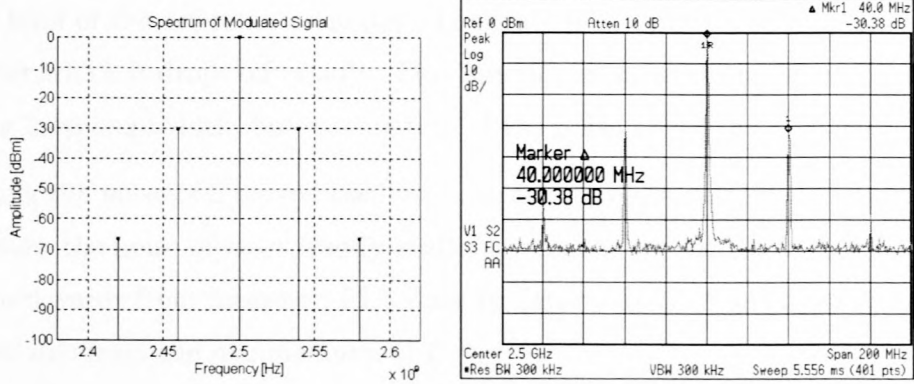


Figure 14.37: Output Spectrum of Fourth-Order Synthesizer with High Frequency FM Modulation

Functionality and performance of all synthesizer components are complete and the only subject untouched is phase noise prediction. This is investigated in the following section where the synthesizer components are analyzed on the basis of phase noise.

## 14.7 Phase Noise Analysis

For this analysis only the fourth-order synthesizer will be investigated, being the most complicated system. Noise generated by the various synthesizer components can be translated to the synthesizer output through the transfer functions derived in section 3.1.6. The translated noise is then summed to produce the total output phase noise of the system.

### 14.7.1 Reference Oscillator Noise

The crystal oscillator noise is amplified in the loop by the gain of the closed loop transfer function. Within the loop bandwidth, the closed loop gain is very large, hence increasing the noise level of the reference oscillator. This gain is flat until it reaches the loop bandwidth, after which it drops off rapidly. This function represents amplification of the noise within the loop bandwidth, but attenuation of the noise above this frequency [14].

Measuring the noise of a crystal oscillator can be quite difficult since the noise is significantly below the noise of most readily available test equipment. In fact, it may be easier to work backwards from measured PLL data to determine the oscillator noise if the data is not available from the manufacturer [14].

Due to lack of manufacturer data and instrumentation limitations, the phase noise of the reference oscillator is not known. To be able to continue with the investigation, the assumption is made that the reference oscillator is generating the noise spectrum of figure 14.38. This spectrum is obtained by utilizing a practical temperature compensated crystal oscillator (TCXO) example and degrading the noise by a safety margin of 15 dB. This assumption is made on the basis that the reference oscillator noise will not dominate the analysis and will only contribute to the in-band noise.

### 14.7.2 Amplifier Noise

The noise generated by an amplifier is specified in equivalent noise voltage ( $e_N$ ) and equivalent noise current ( $i_N$ ) with units of  $\frac{nV}{\sqrt{Hz}}$  and  $\frac{pA}{\sqrt{Hz}}$  respectively. To obtain the noise in a given bandwidth, one must integrate the noise over the bandwidth and multiply it with the amplifier gain as specified [15]. For this verification test a unit gain amplifier is

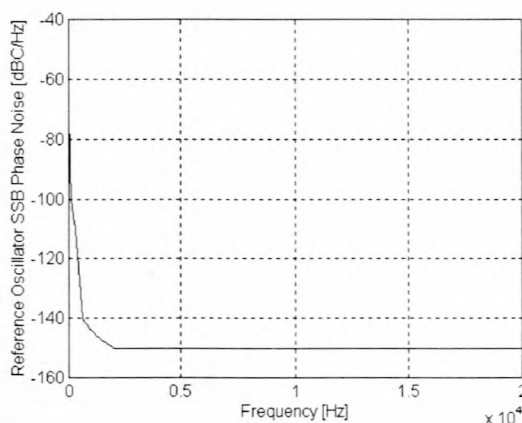


Figure 14.38: Single Sideband Reference Oscillator Noise

used.

If the noise in the band of interest is not flat, the band must be broken into sections, calculating average noise in each section and multiplying by the square root of the section bandwidth. Along with the equivalent noise voltage of the amplifier, the thermal noise generated by the input resistance must be taken into consideration. This thermal noise is white in nature and is calculated using the following equation:

$$\overline{e_r^2} = 4kTRB$$

where

$$T = \text{Temperature}[K]$$

$$R = \text{Resistance}[Ohm]$$

$$B = \text{Bandwidth}$$

$$k = \text{Boltzman's Constant}(1.38 \times 10^{-23})$$

Unfortunately the noise current of the LF351 operational amplifier is only specified at 1 kHz as 0.01 pA, therefore the variation thereof is not known over the frequency range. Calculation of the amplifier noise is performed as shown in table 14.5 with the input impedance  $R_{gen} = 35k\Omega$ .

The calculated noise is transferred to the system output and converted to noise in a 50  $\Omega$  system. The total amplifier noise contribution is shown in figure 14.39.



Table 14.5: Amplifier Noise Calculation

Frequency Range	Bandwidth (BW)	$e_n \times \sqrt{BW}$	$I_n \times R_{gen} \times \sqrt{BW}$	$e_r \times \sqrt{BW}$	$\sqrt{(e_n^2 + e_i^2 + e_r^2) \times BW}$
10-20 Hz	10	1.39e-7	1.11e-9	7.61e-8	1.59e-7
20-40 Hz	20	1.48e-7	1.57e-9	1.08e-7	1.83e-7
40-60 Hz	20	1.25e-7	1.57e-9	1.08e-7	1.65e-7
60-100 Hz	40	1.39e-7	2.21e-9	1.52e-7	2.06e-7
100-200 Hz	100	1.8e-7	3.5e-9	2.41e-7	3.01e-7
200-400 Hz	200	2.4e-7	4.95e-9	3.4e-7	4.17e-7
400-1000 Hz	600	3.67e-7	8.57e-9	5.9e-7	6.95e-7
1000-10000 Hz	9000	1.38e-6	3.32e-8	2.28e-6	2.67e-6
10000-20000 Hz	10000	1.5e-6	3.5e-8	2.41e-6	2.84e-6

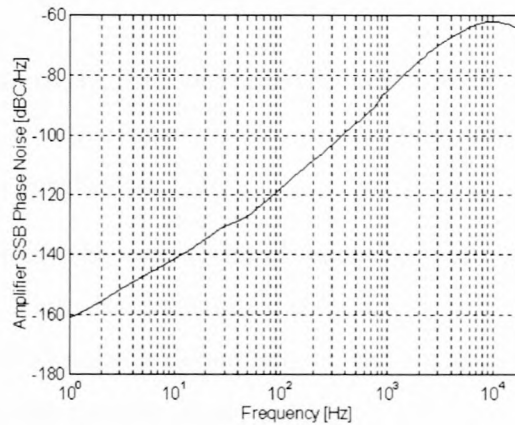


Figure 14.39: Single Sideband Amplifier Noise

### 14.7.3 VCO Noise

The noise from a VCO is inversely proportional to offset frequency from the carrier. The VCO noise is effectively high-pass filtered by the PLL, providing rejection of phase noise or phase error within the bandwidth, but leaving VCO noise well outside of the loop bandwidth [14]. To obtain the most accurate representation of the system noise, the VCO phase noise is measured and displayed in figure 14.40.

### 14.7.4 Phase/Frequency Detector Noise

The phase/frequency detector noise is a form of noise that represents the internal noise floor of the PFD and frequency dividers within the PLL. The noise is modeled as flat versus frequency and the specific value can be obtained from the manufacturer of the synthesizer

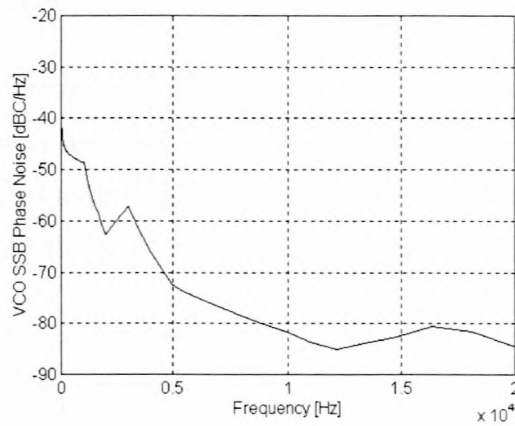


Figure 14.40: Single Sideband VCO Noise

IC. The actual noise floor of the PFD degrades proportionally to the comparison frequency. This noise source is flat with respect to frequency, but it is shaped by the closed loop transfer function of the synthesizer [14].

Banerjee [5] states that the out of band noise is typically dominated by the noise generated by the PFD. This also determines the noise floor for frequencies above the loop bandwidth. Since the PFD noise is dependent on the comparison frequency, Banerjee and Lascari [14] states that the close-in phase noise produced by the PFD is given by:

$$\text{Phase Noise} = (1 \text{ Hz Normalized Phase Noise Floor of Phase Detector}) + 10\log(\text{Comparison Frequency}) + 20\log(N)$$

The noise floor of the Motorola IC used is not known and not noted in the manufacturer's datasheet. For the national PLL IC though, typical values of the 1 Hz normalized phase noise floor range between -199 dBc/Hz for the National LMX 1600 IC and -211 dBc/Hz for the LMX233 series IC's [5]. Using a value of -208, the system phase noise due to the PFD is theoretically calculated as -72 dBc/Hz. Taking this value and transforming it to the output of the PFD leads to a PFD noise of -161 dBc/Hz for the comparison frequency used.

### 14.7.5 System Phase Noise

Summing all the above mentioned translated noise sources at the output of the system, the total output spectrum noise of figure 14.41 is obtained. Also shown in the figure is the measured values of system phase noise. The correlation achieved between the theoretical prediction and the measure results is remarkable, thus proving the validity of the prediction.

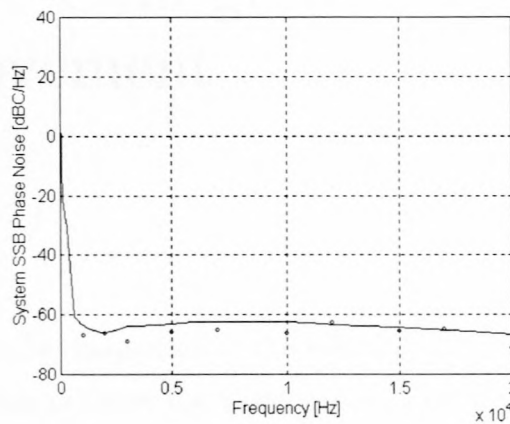


Figure 14.41: Comparison of Theoretical and Measured System Phase Noise

For offset frequencies lower than the system bandwidth from the center frequency, the reference oscillator noise is dominant for small frequency offsets while the PFD produces the noise floor for larger offsets. For frequency offsets larger than the system bandwidth from the center frequency, the VCO noise is dominant.

All theoretical predictions are now completed and verified. The final section in this study deals with the comparison of the analyzed synthesizer configurations to obtain the best performance.

# Chapter 15

## Synthesizer Configuration Comparison and Improvement

### INTRODUCTION

This section presents the comparison of the various synthesizer configurations to determine which configuration achieves the best performance. The comparison is performed based on theoretical system characteristic predictions for systems with identical loop parameters. The parameters remaining fixed throughout the comparison are the loop bandwidth and phase margin/damping factor. The comparison is based on settling time, VCO modulation and reference suppression characteristics.

A phase margin of  $50^\circ$  and damping factor of 0.5 is used for the predictions. Due to the limited parameter choices of the second-order synthesizer, the loop bandwidth is determined by this system. For a damping factor of 0.7 a loop bandwidth of 3168 Hz is achieved and will be used as a fixed value throughout this section.

### 15.1 Settling Time

The settling time of all three systems is shown in figure 15.1. The results show almost identical results for all three systems. Therefore, this test does not contribute to the conclusion of which system performs the best.



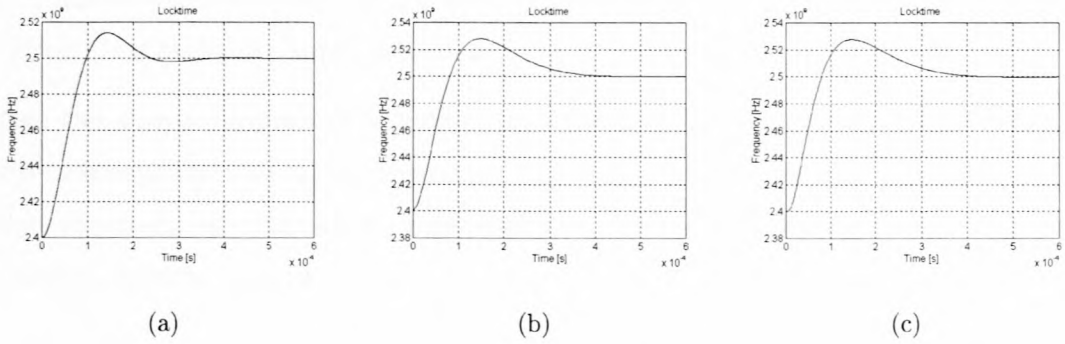


Figure 15.1: a) Settling Time of Second-Order System b) Settling Time of Third-Order System c) Settling Time of Fourth-Order System

## 15.2 VCO Deviation due to Modulation Signal

Deviation of the VCO for the various systems due to the application of the modulation signal is shown in figure 15.2. No significant differences is observed from the figures and therefore no system is clearly identified as superior in this respect.

## 15.3 Reference Suppression

A reference suppression of 20.6 dB is predicted for the second-order system while the third and fourth-order systems suppression is difficult to determine. The statement can be made that the third-order system reference suppression will be higher than the second-order system due to the integration action of the loop filter. The fourth-order system will

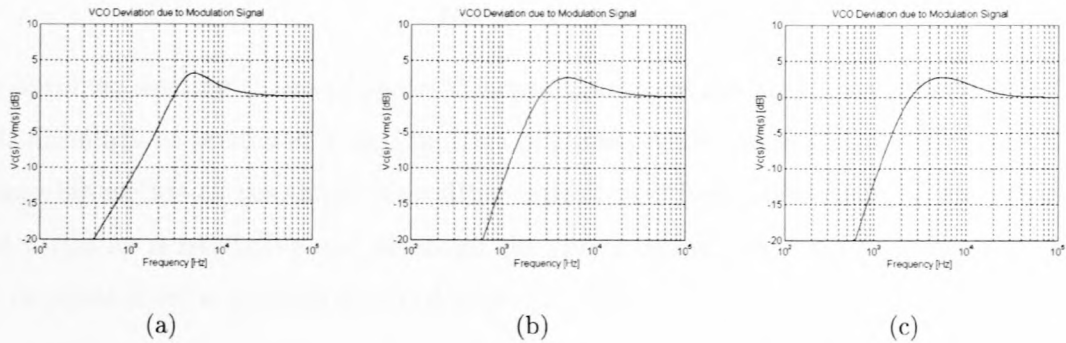


Figure 15.2: a) Deviation of VCO for Second-Order System b) Deviation of VCO for Third-Order System c) Deviation of VCO for Fourth-Order System

in turn achieve higher reference suppression than the third-order system due to the added RC filter, thus being the superior system in this regard.

From the above comparison it is clear that the best performance is obtained from the fourth-order system with a charge pump PFD. Although all specifications are met by the current fourth-order synthesizer, a more efficient system can be obtained by enhancing the output spectral quality.

## 15.4 Improvement to Fourth-Order System

The current system produces reference sidebands almost equal to the in-band noise floor and could jeopardize demodulation performance. The bandwidth of the following system is reduced producing improved reference suppression at the expense of a longer settling time:

$$\begin{aligned}
 \text{Phase Margin} &= 50 \\
 \text{Loop Bandwidth} &= 4.7\text{kHz} \\
 N &= 15680 \\
 K_{VCO} &= 77\text{e6} \\
 K_{\phi} &= 5 * 2 * \pi \text{ mA} \\
 K_{sum} &= 1
 \end{aligned}$$

with

$$\begin{aligned}
 C_1 &= 27 \text{ nF} \\
 C_2 &= 440 \text{ nF} \\
 C_3 &= 2.2 \text{ nF} \\
 R_2 &= 200 \ \Omega \\
 R_3 &= 2.4 \text{ k}\Omega
 \end{aligned}$$

The obtained settling time and spectral measurement results are shown in figures 15.3 and 15.4. Simulations predicted a settling time of 600us, while the practical circuit could only achieve 800us due to the larger loop filter capacitor. Phase noise and reference sideband level variation is negligible and although the specifications are exceeded, improvement is still required from a spectral point of view.

As a point of interest, the bandwidth of the system was reduced with the knowledge that the synthesizer will no long meet the settling time specifications. The following system resulted:

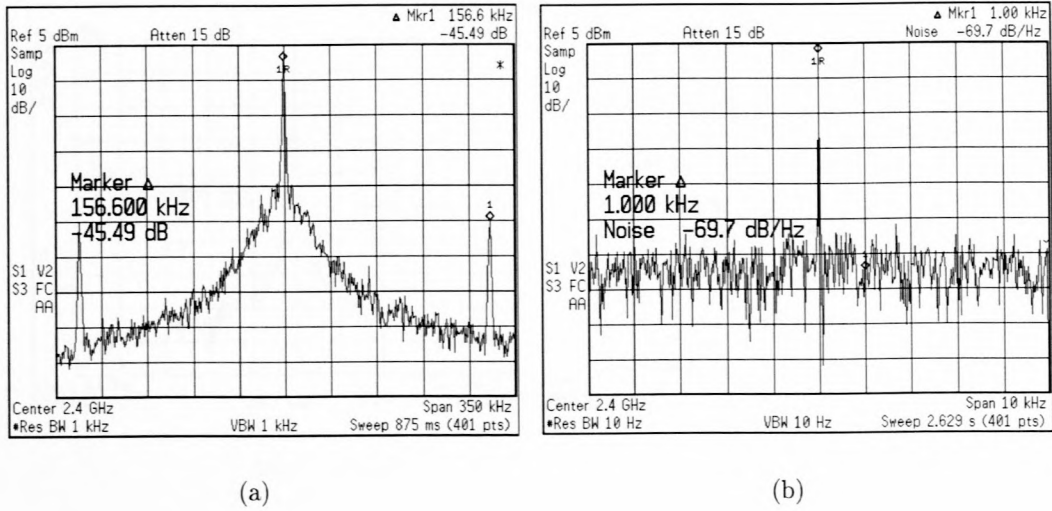


Figure 15.3: a) Spectrum of Improved System b) Spectrum of Improved System Showing Phase Noise

$$\begin{aligned}
 \text{Phase Margin} &= 50 \\
 \text{Loop Bandwidth} &= 1.45 \text{ kHz} \\
 N &= 15680 \\
 K_{VCO} &= 77e6 \\
 K_{\phi} &= 5 * 2 * \pi \text{ mA} \\
 K_{sum} &= 1
 \end{aligned}$$

with

$$\begin{aligned}
 C_1 &= 265 \text{ nF} \\
 C_2 &= 4.7 \text{ uF} \\
 C_3 &= 56 \text{ nF} \\
 R_2 &= 68 \text{ } \Omega \\
 R_3 &= 330 \text{ } \Omega
 \end{aligned}$$

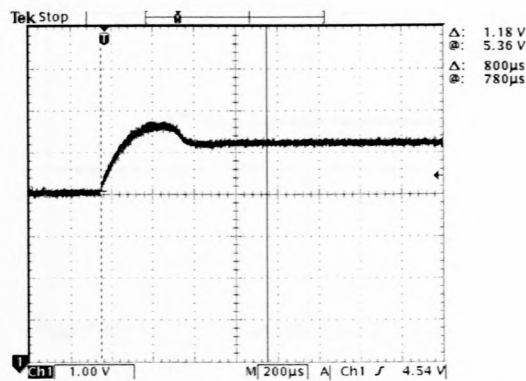


Figure 15.4: Settling Time of Improved System

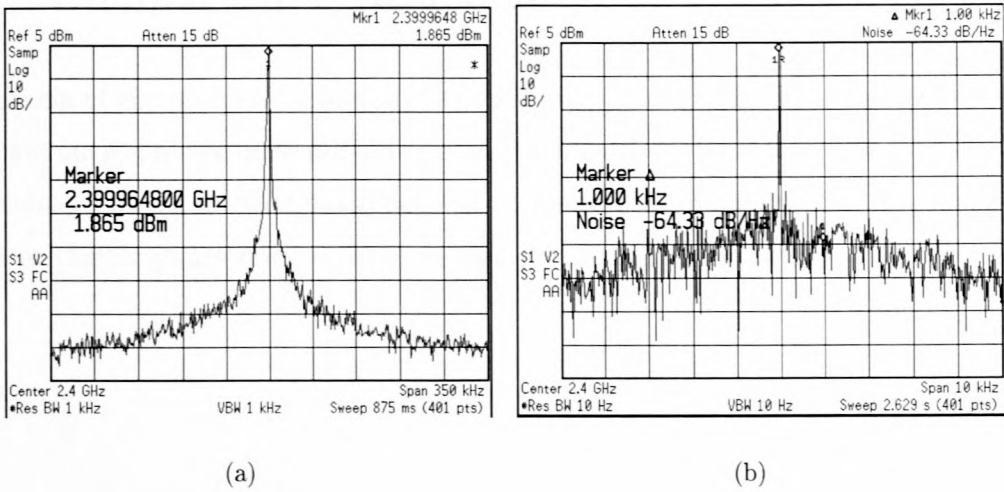


Figure 15.5: a) Spectrum of Further Improved System b) Spectrum of Further Improved System Showing Phase Noise

Figures 15.5 and 15.6 shows the obtained settling time and spectral measurements. A settling time of 3 ms was predicted, while a measured settling time of 5 ms was achieved. A slight degradation in phase noise is observed due to the reduced bandwidth. The produced reference sidebands are not even noticeable above the noise, providing a vast improvement of signal spectral purity.

The results above shows that improvement of the synthesizer output signal spectral purity can be obtained by reducing the loop bandwidth. Other options to investigate for output spectrum improvement is to increase the comparison frequency or to insert a notch filter after the loop filter to effectively suppress the reference frequency component of the control voltage.

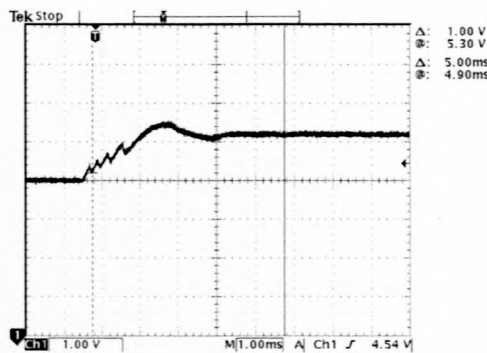


Figure 15.6: Settling Time of Improved System





# Conclusions

## Achievements

The aim of this study was to obtain a synthesizer configuration for the effective generation of wideband FM, considering both passive and active loop filters and to also practically verify theoretical system performance predictions. The selection is based on synthesizer output signal quality, settling time and loop response to the modulation signal. During development of the various synthesizers, the following achievements were obtained:

- Derivation of general loop equations. These equations are the basis for evaluation of all the synthesizer configurations.
- Phase noise characteristics of the various components were discussed pertaining to the effect on the system and choice of components.
- All synthesizer parameters were addressed along with the influence each exhibits on system performance. The importance of this section can't be emphasized enough as all adverse effects must be considered before choosing any system parameter.
- The realization of a hybrid splitter using microwave techniques. A simulation program was used during design with practical and simulated results comparing well.
- An external charge pump circuit was designed utilizing discrete transistors.
- During design and layout, utilization of EMC principles reduced cross-talk and increased component isolation. Care was taken to minimize the effects of environmental noise on the system.

- Successful theoretical predictions of all synthesizer configurations considered. This includes passive and active loop filter analysis as well as system performance predictions due to variation of damping factor/phase margin and loop gain. The following theoretical predictions were performed:
  - Settling time or transient response of system.
  - VCO response due to the application of a modulation signal.
  - Phase error variation due to the modulation signal.
- Successful practical implementation of the various synthesizer configurations.
- Practical verification of performance predictions of all synthesizer configurations. Measurements taken from the practical circuits verified the simulation accuracy with almost negligible deviation in most cases.
- Successful generation of a high frequency FM signal. Using Bessel functions, the output spectrum of the modulated signal was verified with the results corresponding well to the simulations performed.
- Successful prediction of system phase noise. Using some realistic assumptions, the system phase noise was predicted with remarkable accuracy.
- Implementation of a synthesizer with increased reference suppression. Modifying the system loop filter produced a system displaying minimal noise degradation and producing reference sidebands below the system noise level.

## Future Development Opportunities

- Investigate the use of a "notch" filter. Intuitively a notch filter centered on the reference frequency will reduce reference sidebands without altering settling times.
- A complete study of synthesizer noise and the effects of parameter variation on noise performance predictions.
- Establishing a man-machine interface (MMI) for synthesizer output frequency control.
- Investigation of minimum channel hopping speed limitations.
- Investigate the use of a sampling phase detector as feedback device.
- Design of a low noise voltage-controller oscillator.
- Generation of low noise local oscillator signals using high comparison frequencies.
- Time domain synthesizer settling simulations. Settling time simulations in the time domain will eliminate errors due to capacitor characteristics.



## Concluding Remarks

This thesis showed the development and verification of synthesizers for the purpose of FM generation. During this phase, special attention was given to parameter selection and the consequences thereof. A synthesizer was successfully developed generating a wideband FM output signal directly at the required frequency, resulting in the aim of this study being achieved.

During the course of this study knowledge associated with the use and implementation of various synthesizer aspects was obtained. Various theoretical analysis methods were used for simulations and system performance predictions providing improved insight into control systems. Valuable practical experience was obtained during implementation and measurement of the diverse components, leading to the mastering of numerous synthesizer principles.

# Appendix A

## Oscillator Analysis method

In the design of oscillators, the paths most commonly chosen is the reflection and open-loop gain design techniques. The former relies on the negative gate impedance presented by a destabilized transistor while the latter relies on gain supplied by a stable transistor. Although the reflection technique is easily understood and implemented, there remains an uncertainty about the level of negative resistance needed to sustain oscillation while minimizing phase noise. The most effective way of avoiding this problem is to use loop-gain analysis methods on reflection oscillator designs.

Rogers [11] stated that the open-loop gain of an amplifier plays a significant role in the phase noise performance of the oscillator. Too high an open-loop gain will produce excessive signal compression causing increased phase noise, while too low an open-loop gain will cause oscillator start-up problems. The question now remains, how low an open-loop gain can be used without compromising oscillator start-up ?

In order to control the output power of an oscillator, the load termination presented to the transistor should be controlled as well [16]. This represents the first substantial problem as the output of the transistor is fed back to the input which is dependent on the transistor load. To better understand the problem, the oscillator configuration is transformed as shown in figure A.1. The transformation is performed by floating the original ground and introducing a virtual ground at the source of the transistor.

The oscillator output power can be controlled by the generation of the transistor's power contours by either the power parameter approach or by non-linear simulations. In the design of an oscillator, the ideal approach is to select a load line for the transistor and then

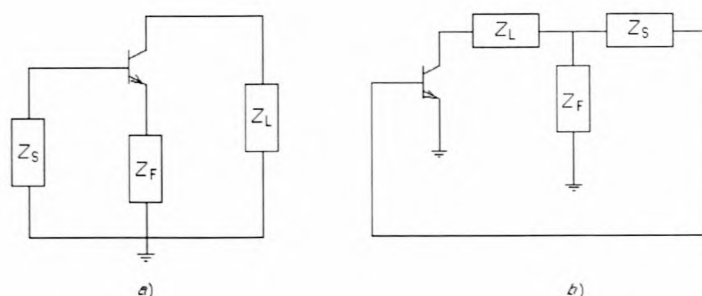


Figure A.1: Transformation of Oscillator Impedances : **a)** Original Block-Diagram Representation of a Reflection Oscillator **b)** Transformed Block-Diagram of the Reflection Oscillator

design a feedback network, giving the correct transistor loading and the required open-loop gain. Ideally, the load line at steady-state should be controlled, but excellent results can also be obtained with the small-signal parameters if the open-loop gain required is low [16].

Care should be taken to maximize the loaded  $Q$  (or phase slope of the open-loop gain) for low phase noise requirements. This will reflect on the choice of the resonator to be used and the load line chosen (higher parallel or lower series resistance will be associated with higher  $Q_s$ ). In simple cases the loaded  $Q$  at start-up can be estimated from the open-loop gain response by using the following equation [16]:

$$Q = \frac{\pi}{360}(\Delta\theta/\Delta f)f_0$$

where the phase slope  $\Delta\theta/\Delta f$  is specified in degrees per gigahertz and the resonant frequency in gigahertz. Instead of attempting to estimate the loaded  $Q$ , a better option is to directly control the phase loop slope [16]. Again a point is reached where the open-loop gain and loop phase must be obtained for an oscillator. The above arguments affirm the notion that a need exists for an analysis/design method for reflection oscillators in terms of loop gain. The following sections present an analysis method for this purpose.

For this analysis it is assumed that the oscillator design was performed using the negative resistance (reflection) approach and that the input impedances of the transistor ( $Z_{in}$ ), load ( $Z_L$ ), destabilization network ( $Z_f$ ) and resonator ( $Z_s$ ) are known. With these components known, along with the transistor parameters, equations can be derived to calculate the open-loop gain of the oscillator.

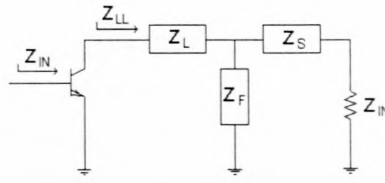


Figure A.2: Breaking of the Feedback Loop

The first step in the analysis is to obtain the Z-parameters of the transistor used. This is done by transformation of the transistor S-parameters using the following equation:

$$\begin{aligned} \mathbf{Z}_t &= \begin{pmatrix} z_{11t} & z_{12t} \\ z_{21t} & z_{22t} \end{pmatrix} \\ &= \mathbf{Z}_0(\mathbf{I} + \mathbf{S})(\mathbf{I} - \mathbf{S})^{-1} \end{aligned}$$

where  $\mathbf{I}$  is the unity matrix and  $\mathbf{S}$  is the transistor S-parameters. As the destabilization network is in series with the transistor, the equivalent transistor Z-matrix ( $\mathbf{Z}$ ) is equal to the sum of the transistor and destabilization network Z-matrices [17], or:

$$\mathbf{Z}_{eq} = \mathbf{Z}_t + \mathbf{Z}_f$$

which implies:

$$\begin{aligned} z_{11eq} &= z_{11t} + z_{11f} \\ z_{21eq} &= z_{21t} + z_{21f} \\ z_{12eq} &= z_{12t} + z_{12f} \\ z_{22eq} &= z_{22t} + z_{22f} \end{aligned}$$

Now that the Z-parameters of the transistor taking the destabilization network into account is known, the input impedance of the transistor with no feedback can now be calculated using [18]:

$$Z_{in(load)} = z_{11eq} - \frac{z_{12eq} \times z_{21eq}}{z_{22eq} + Z_l} \quad (\text{A.1})$$

By using feedback breaking techniques, the oscillator of figure A.1 can be represented as shown in figure A.2. where [2],

$$Z_{LL} = z_{11n} - \frac{z_{21n}z_{12n}}{z_{22n} + Z_{in}} \quad (\text{A.2})$$

and  $\mathbf{Z}_n$  is the Z-parameters of the oscillator feedback network given by (see figure A.3):



$$\begin{aligned}
z_{11n} &= \frac{V_1}{I_1} \Big|_{I_2=0} = Z_{Ltemp} + Z_F \\
z_{21n} &= \frac{V_2}{I_1} \Big|_{I_2=0} \text{ and } V_2 = V_1 \left( \frac{Z_F}{Z_F + Z_{Ltemp}} \right) = Z_F I_1 \implies \frac{V_2}{I_1} = Z_F \\
z_{22n} &= \frac{V_2}{I_2} \Big|_{I_1=0} = Z_{Stemp} + Z_F \\
z_{12n} &= \frac{V_1}{I_2} \Big|_{I_1=0} \text{ and } V_1 = Z_F (I_2) \implies \frac{V_1}{I_2} = Z_F
\end{aligned}$$

The input impedance of the transistor is now given by [17]:

$$Z_{in} = z_{11t} - \frac{z_{21t}z_{12t}}{z_{22t} + Z_{LL}} \quad (\text{A.3})$$

Combining (A.2) and (A.3) gives:

$$Z_{in}^2(A) + Z_{in}(B) - (C) = 0 \quad (\text{A.4})$$

where,

$$\begin{aligned}
A &= (z_{22t} + z_{11n}) \\
B &= (z_{22t}z_{22n} + z_{11n}z_{22n} - z_{21n}z_{12n} - z_{11t}z_{22t} - z_{11t}z_{11n} + z_{12t}z_{21t}) \\
C &= (z_{11t}z_{22t}z_{22n} - z_{11n}z_{11t}z_{22n} + z_{11t}z_{21n}z_{12t}z_{22n})
\end{aligned}$$

From the above, if the Z-parameters of the transistor and the feedback network are known, equation (A.4) can be solved yielding the transistor input impedance taking the feedback network into account. The next step is to calculate the open-loop gain, given the input impedance of the transistor and feedback network. Firstly an equation for the open-loop gain of the oscillator must be obtained.

To obtain these equations, two-port models must be used. Figure A.4 shows the circuit diagram for the oscillator with the transistor represented as a two-port device. Using Z-parameter equations, two equations are derived:

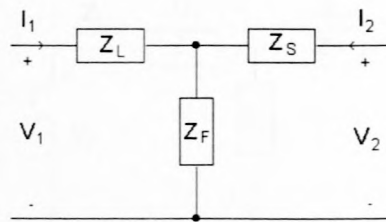


Figure A.3: Two-Port Representation of the Feedback Network

$$V_2 = z_{21}I_1 - z_{22}I_2 \quad (\text{A.5})$$

$$V_2 = I_2 Z_{LL} \quad (\text{A.6})$$

By substituting (A.6) into (A.5),

$$\frac{I_2}{I_1} = \frac{z_{21}}{z_{22} + Z_{LL}} = A_I \quad (\text{A.7})$$

The open-loop gain ( $G_{Loop}$ ) is defined as the current gain around the loop as follows:

$$\begin{aligned} G_{Loop} I_1 &= I_3 \\ &= \left( \frac{Z_f}{Z_f + Z_s + Z_{in}} \right) I_2 \end{aligned} \quad (\text{A.8})$$

From equations (A.7) and (A.8), once  $Z_{LL}$  is known, the open-loop gain can be calculated. As  $Z_{LL}$  can be calculated from equation (A.2) with the calculated input impedance of the transistor, it is thus now possible to calculate the open-loop gain of an oscillator. To verify the validity of these equations, an analysis of an oscillator designed using Touchstone is performed. The negative of the transistor input impedance as well as the resonator impedance are shown in figure A.5.

The figure shows that oscillations will occur at 10.5GHz with a negative input resistance of  $-29.6\Omega$ . Although the input impedance is known, it will be recalculated using equation (A.4). This equation provides two possible answers although only one is correct. A solution to this problem is discussed later in the analysis.

As open-loop gain magnitude is dependent on the transistor negative input resistance, the real part of the transistor input impedance and source impedance are used for the calculation. Likewise, the imaginary part of the impedances are used to calculate the

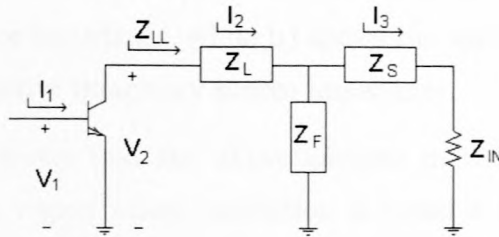


Figure A.4: Transistor as Two-Port Device

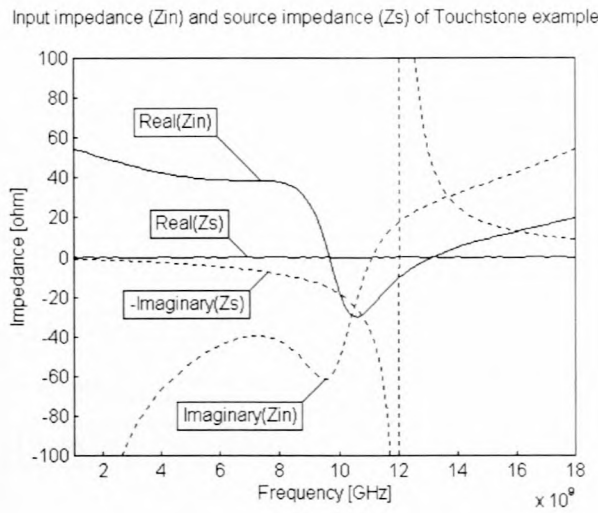


Figure A.5: Input Impedance ( $Z_{in}$ ) and Resonator Impedance ( $Z_S$ ) of Touchstone Example

open-loop gain angle. As the real and imaginary impedances are used separately in the calculations, the load impedance  $Z_L$  has to be recalculated in both cases to take this factor into account. This temporary load impedance is calculated using (employing (A.3)):

$$Z_{Ltemp} = \frac{z_{11} \times z_{22} - Z_{in} \times z_{22} - z_{12} \times z_{21}}{Z_{in} - z_{11}} \quad (\text{A.9})$$

By using (A.4) followed by (A.2) and (A.8), two solutions are obtained for the open-loop gain magnitude because of the roots obtained from (A.4). To find the correct solution, a known condition is entered into  $Z_S$  which will provide a known answer for the open-loop gain. The logical method is to insert a value equal to the negative of the transistor input impedance which will yield an open-loop gain magnitude of 1 and angle of  $0^\circ$ . Figure A.6 shows the open-loop gain obtained for the Touchstone example together with the transistor input impedance and resonator impedance of the oscillator. For clarification reasons, figure A.7 **a**) shows only the open-loop gain magnitude along with the real input impedance and real source impedance, while **b**) shows the open-loop gain phase with the imaginary input and negative imaginary source impedance.

This example clearly shows that the above analysis method predicts the oscillation frequency as well as the region where oscillation is possible (negative transistor input impedance). Although this method has not yet been tested against practical circuits, all tests indicate that favorable results will be achieved.

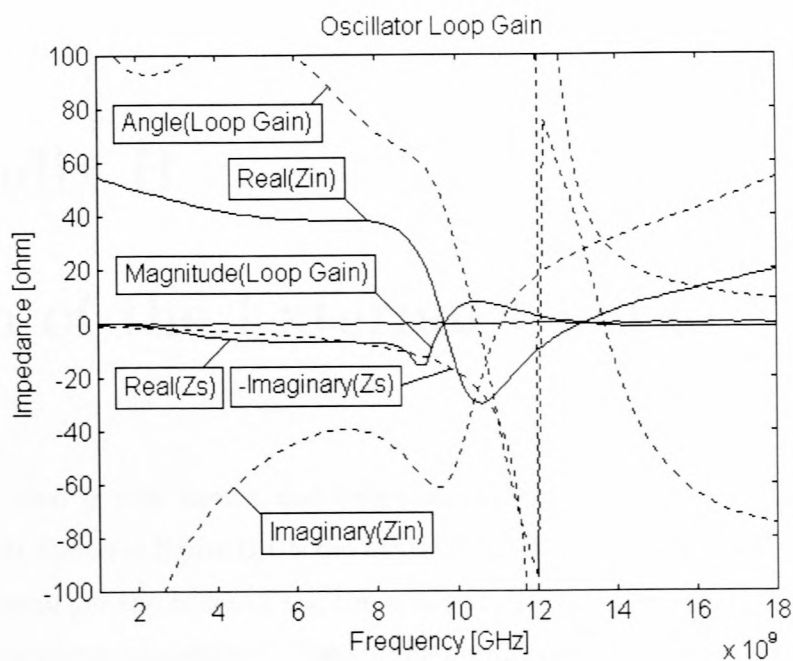


Figure A.6: Oscillator Impedances and Loop Gain

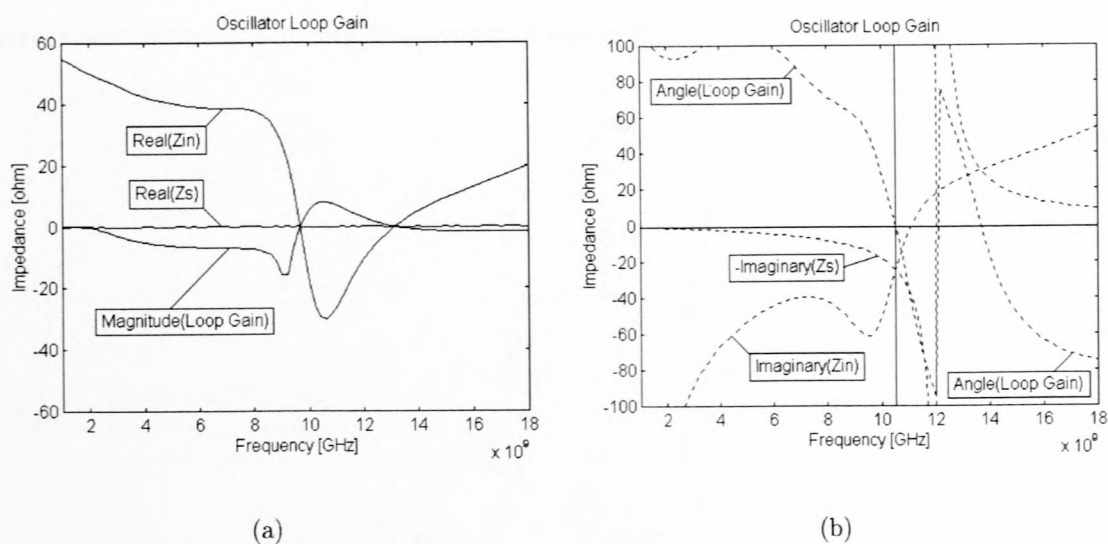


Figure A.7: Oscillator Impedances and Loop Gain



# Appendix B

## Design of the External Charge Pump

The circuit used is well known and based on current mirror techniques. The current selection circuit shown in figure B.1 is the heart of the charge pump circuit. A fixed voltage of 5 V will appear on the bases of the top transistors due to the negligible base currents (high transistor input impedance). The charge pump control voltages ( $\phi_R$  and  $\phi_V$ ) has a voltage swing of between 0.1 V and 4.9 V guaranteed by the datasheet. For all practical purposes, the collector of the bottom transistor  $V_b$  will be at ground potential while  $V_a$  will be at 4.3 V when the control signal is active. With this assumption, the required charge pump current is determined primarily by resistor R1. To obtain the required 5 mA resistor value of  $860 \Omega$  is used. The source and sink paths are created utilizing current mirrors techniques producing the circuit of figure B.2.

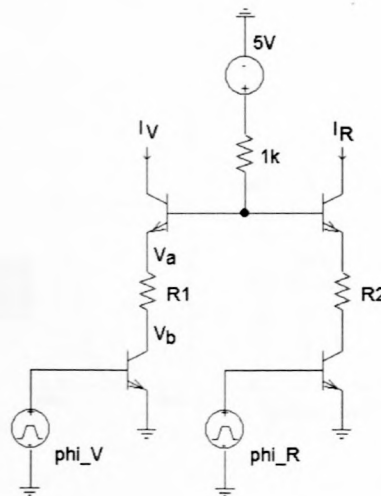


Figure B.1: Current Selection Circuit

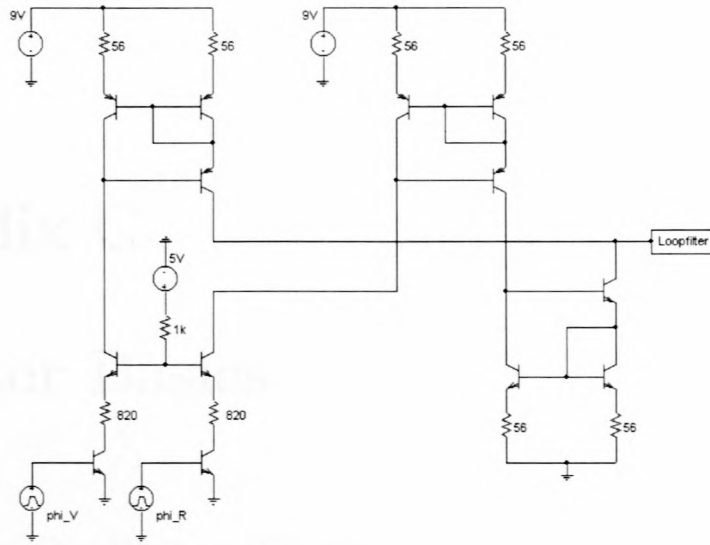


Figure B.2: Charge Pump Circuit

Frequency response and time domain output signal simulation results are shown in figure B.3. The frequency response graph shows a pole contributed to the system at 16 MHz, well above system influence range. To differentiate between the time domain signals, the output signal of figure B.3 b) have been elevated by 10 V.

The time domain simulation predicts a 2.181 V voltage drop across the loading resistor, thus predicting an output current of 5.07 mA. Source and sink currents of 5.14 mA and 5.05 mA were obtained through physical measurements. This results in a mismatch of 1.4%.

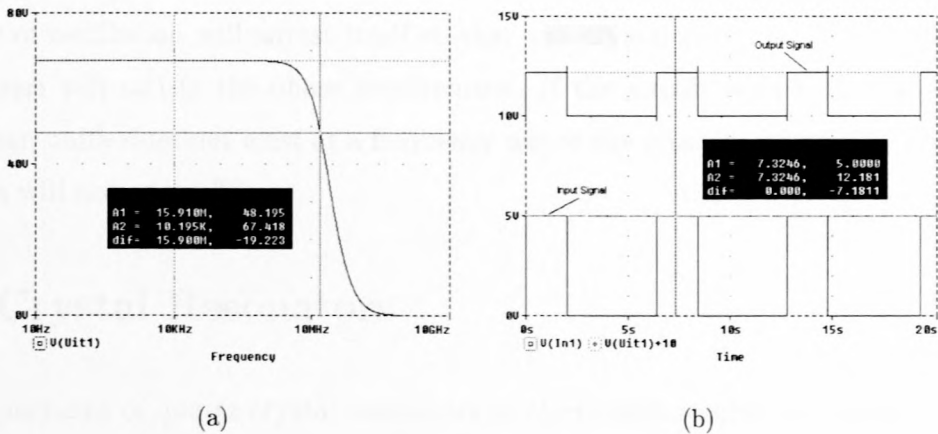


Figure B.3: a) Charge Pump Frequency Response b) Charge Pump Time Domain Output

# Appendix C

## Oscillator Basics

### C.1 Basic Oscillator Theory

In the design of a crystal oscillator, an understanding of basic oscillator theory is not only desirable but essential. Therefore, a brief explanation of crystal oscillator operation is presented here. A crystal oscillator can be thought of as a closed loop system composed of an amplifier and a feedback network containing a crystal. The amplitude of oscillation builds up to the point where loop non-linearities decrease the loop gain to unity. The frequency adjusts itself so that the total phase shift around the loop is  $0^\circ$  or  $360^\circ$ . The crystal, which has a large reactance-frequency slope, is located in the feedback network at a point where it has maximum influence on the frequency of oscillation. A crystal oscillator is unique in that the impedance of the crystal changes so rapidly with frequency that all other circuit components can be considered to be of constant reactance. The frequency of oscillation will adjust itself so that the crystal presents a reactance to the circuit which will satisfy the phase requirement. If the circuit is such that a loop gain greater than unity does not exist at a frequency where the phase requirement can be met, oscillation will not occur [9].

### C.2 Crystal Resonators

The importance of quartz crystal resonators in electronics results from their extremely high Q, relatively small size and excellent temperature stability. A quartz crystal resonator utilizes the piezoelectric properties of quartz. If stress is applied to a crystal in a certain

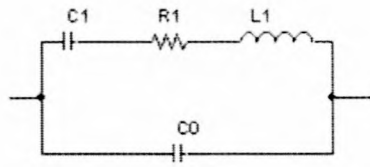


Figure C.1: Electrical Model of Crystal Resonator

direction, electric charge appears in a perpendicular direction. Conversely, if an electric field is applied, it will cause mechanical deflection of the crystal. In a quartz crystal resonator, a thin slab of quartz is placed between two electrodes. An alternating voltage applied to these electrodes causes the quartz to vibrate. If the frequency of this voltage is close to the mechanical resonance of the quartz slab, the amplitude of the vibration will increase. The strain of these vibrations causes the quartz to produce a sinusoidal electric field which controls the effective impedance between the two electrodes. This impedance is strongly dependent on the excitation frequency and possesses an extremely high  $Q$  [9].

Electrically, a quartz crystal can be represented by the equivalent circuit of figure C.1 where the series combination  $R_1$ ,  $L_1$ , and  $C_1$  represent the quartz, and  $C_0$  represents the shunt capacitance of the electrodes in parallel with the holder capacitance. The inductor  $L_1$  is a function of the mass of the quartz, while  $C_1$  is associated with its stiffness. The resistor  $R_1$  results from the loss in the quartz and mounting arrangement.

### C.3 Choice of Active Element

The choice of an active element is very important when certain oscillator specifications must be met. The transistor chosen must obviously be operative over the required temperature range and must be compatible with the oscillator circuit. At VHF, the influence of the low frequency parameters are minimized, and thus the transistor becomes less dependent on temperature.

The cut-off frequency ( $f_t$ ) of a transistor is an important characteristic, as it is some measure of the phase shift through it at the operating frequency. This phase shift is lagging and causes the oscillator frequency to decrease and to become more dependent on the transistor. Therefore, it is desirable to use a transistor with a cut-off frequency at least an order of magnitude higher than the operating frequency. To obtain high-stability



oscillators, it is desirable to minimize the effects of the transistor on the frequency. For this reason the input and output capacitances of the transistor are often swamped out by the addition of external input and output capacitors. If the input and output capacitances are small, they can be swamped out effectively without the external capacitors becoming large enough to prevent oscillation. Therefore, it is desirable to use transistors with low input and output capacitances [9].

## Summing Network Example

The circuit in Fig. 10.10 is a summing network which is used to combine the signals from several oscillators. The circuit is a voltage divider network which is used to combine the signals from several oscillators. The circuit is a voltage divider network which is used to combine the signals from several oscillators.

The circuit in Fig. 10.10 is a summing network which is used to combine the signals from several oscillators. The circuit is a voltage divider network which is used to combine the signals from several oscillators.

## D.18 Input Isolation Network

For good input isolation for the oscillator network is required. The circuit in Fig. 10.11 is a voltage divider network which is used to combine the signals from several oscillators. The circuit is a voltage divider network which is used to combine the signals from several oscillators.

## D.19 Addition of Bias Voltage to Synthetic Signal

Due to the low frequency of the oscillator signal, the addition of a bias voltage to the oscillator signal is required. The circuit in Fig. 10.12 is a voltage divider network which is used to combine the signals from several oscillators.

# Appendix D

## Summing Network Design

The aim of the summing network is to combine the synthesizer control signal and the modulation signal for application to the VCO. In order to comply with the requirements, a discrete transistor amplifier is used which necessitates adding a DC offset voltage (chosen as 0.8 V to ensure forward biasing) to the control signal.

The first section in this appendix addresses the input isolation network followed by the addition of the bias voltage to the synthesizer control signal. Thereafter the design of the isolation network will be discussed, followed by the nodal summing network design.

### D.1 Input Isolation Network

To provide a high input impedance for the synthesizer loop filter, an input isolation network is required. This network consists of a LF351 operation amplifier utilized in the follower configuration. The LF351 performance is satisfactory for the purpose because of its high input impedance and high gain-bandwidth product.

### D.2 Addition of Bias Voltage to Synthesizer Control Signal

Due to the low frequency of the summing signals, the summation is achieved using an operation amplifier. A LF351 again features, configured as shown in figure D.1. Along with the summation property, this circuit amplifies the synthesizer control signal by a

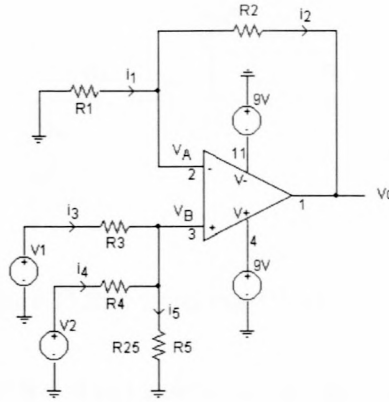


Figure D.1: Summing Block-Diagram

factor of 2 to obtain the full VCO control voltage range. The gain factor can be altered with minor changes to this circuit to vary synthesizer loop gain.

The transfer function of the circuit is calculated as:

$$V_0 = V_1 A_1 \left(1 + \frac{R_2}{R_1}\right) + V_2 A_2 \left(1 + \frac{R_2}{R_1}\right) \quad (\text{D.1})$$

where

$$\begin{aligned} A_1 &= \left( \frac{R_4 R_5}{R_4 R_5 + R_3 R_5 + R_3 R_4} \right) \\ A_2 &= \left( \frac{R_3 R_5}{R_4 R_5 + R_3 R_5 + R_3 R_4} \right) \end{aligned} \quad (\text{D.2})$$

By choosing the resistors  $R_1$  and  $R_2$  as  $1 \text{ k}\Omega$  and  $3 \text{ k}\Omega$  respectively along with a  $V_1$  gain of 2 leads to (Using (D.1) and (D.2)):

$$\begin{aligned} A_1 \left(1 + \frac{R_2}{R_1}\right) &= 2 \\ R_4 R_5 &= R_3 R_5 + R_3 R_4 \end{aligned} \quad (\text{D.3})$$

Using a  $V_2$  gain of 1, (D.1), (D.2) and (D.3):

$$R_5 = R_4 \quad (\text{D.4})$$

leading to (inserting (D.4) into (D.3)):

$$R_4 = 2R_3$$

By choosing  $R_3$  as  $1 \text{ k}\Omega$  results in  $R_4 = R_5 = 2 \text{ k}\Omega$ . The bias voltage  $V_2$  is generated using

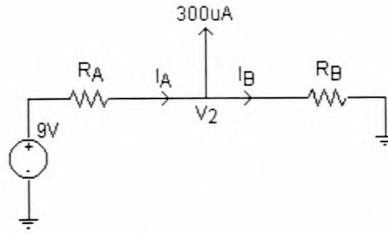


Figure D.2: Summing Block-Diagram

a voltage division network with a fixed reference voltage of 9 V. To calculate the resistor values required to perform the voltage division,  $V_B$  is calculated using Kirchoff's current law (using the resistor values calculated above):

$$V_B = V_1 \left( \frac{R_4 R_5}{R_4 R_5 + R_3 R_5 + R_3 R_4} \right) + \left( \frac{R_3 R_5}{R_4 R_5 + R_3 R_5 + R_3 R_4} \right) = V_1(0.5) + V_2(0.25) \quad (\text{D.5})$$

Transistor under-biasing can occur if current  $i_4$  becomes too small due to the control voltage  $V_1$  becoming too small. This is eliminated by calculating a minimum current value for  $i_4$ . Using (D.5) with  $V_1 = 0V$  and  $V_2 = 0.8V$ , the minimum current is obtained as 300  $\mu\text{A}$ , resulting in the voltage division network of figure D.2. The maximum current value for  $i_4$  is also calculated (using  $V_1=9\text{ V}$  and  $V_2=0.8\text{ V}$ ) as 2.35 mA.

For  $V_1$  to have a minimal effect on the bias voltage, the current through resistor  $R_B$  should be as high as possible. For this reason the current through  $R_B$  is chosen as 13 times higher than the maximum  $i_4$  current. With a voltage drop of 0.8 V over  $R_B$ , this leads to  $R_B = 26\Omega \approx 27\Omega$  and  $R_A = 265\Omega$ .

Now that the network summing the DC bias and synthesizer control signal have been designed, the next obstacle is to construct the output isolation network as the nodal summing network depends on its characteristics.

### D.3 Output Isolation Network

The reason for incorporating an output isolation network is to obtain a high input impedance for the nodal summing network. Due to the high modulation signal frequency and ease of design, a discrete transistor amplifier is used to produce the high input impedance required. An emitter-follower amplifier implementation is ideal for the



purpose because of its high input impedance, non-inverting and unit gain properties. Due to its high frequency properties and low cost, the 2N3904 transistor is used. (The 2N2222 transistor could also be used) with a minimum  $\beta$  specified as 30. Biasing for the amplifier is obtained from the DC bias voltage added to the synthesizer control signal. Shown in figure D.3 a) is the output isolation network.

For nodal summing network calculations, the input impedance of the output isolation network is required and is obtained using two methods; the first method utilizes the transistor small-signal model while a simulation package is used for the second.

Only the minimum input impedance of the output isolation network is of concern because a higher output isolation network input impedance will have lesser of an effect on the summing node. The small-signal model of the output isolation network is shown in figure D.3 b).

From the small-signal model the input impedance is obtained by:

$$R_{in} = \frac{V_{in}}{i_b}$$

where

$$V_{in} = i_b(R_{pi} + (\beta + 1)R_e)$$

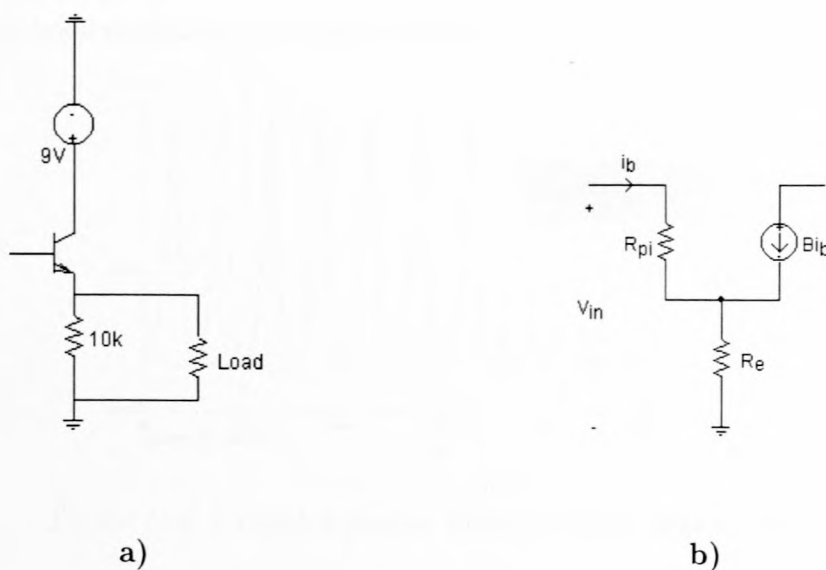


Figure D.3: a) Output Isolation Amplifier b) Small-Signal Model of Isolation Amplifier

Thus,

$$R_{in} = R_{pi} + (\beta + 1)R_e = R_{pi} + 310000$$

As the input impedance of the VCO is unknown, it will be assumed as  $100 \text{ k}\Omega$  which will not affect the output isolation network. This is a fair assumption as the control voltage is normally connected directly to a varactor diode with very low leakage currents. According to Neamen [19]:

$$R_{pi} = \frac{\beta}{g_m}$$

$$g_m = \frac{I_{CQ}}{V_T}$$

where  $V_T \approx 0.026$ . The maximum  $I_{CQ}$  will occur with  $9 \text{ V}$  across  $R_e$ , leading to:

$$I_{CQmax} \approx 1 \text{ mA}$$

This in turn leads to a maximum  $R_{pi}$  of  $780 \text{ }\Omega$ . From this calculation it is evident that  $R_{pi}$  can be ignored for this calculation. Following the calculations above, the isolation network input impedance is obtained as  $310 \text{ k}\Omega$ .

For the second method PSpice is used yielding the simulation results illustrated in figure D.3. The simulation clearly shows that the minimum attained input impedance amounts to  $216 \text{ k}\Omega$ , which is less than the calculated small-signal value. For safety, the lower value of the two methods is used for the nodal summation calculations.

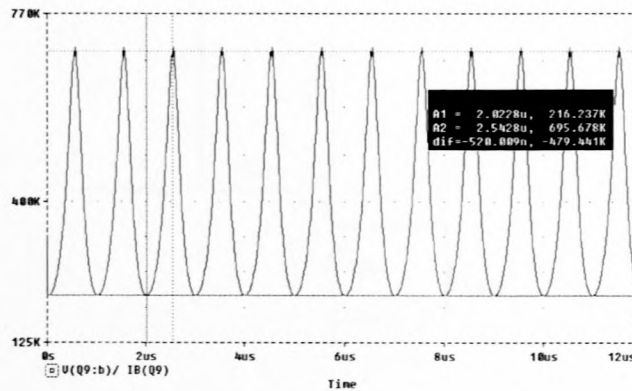


Figure D.3: Output Isolation Network Input Impedance

## D.4 Nodal Summing Network

To realize this section of the network, the circuit illustrated in figure D.4 is used. The value of the coupling capacitor (C) is calculated from the specification of the pole due to the series combination of this capacitor and the  $50\ \Omega$  source resistor. To ensure that synthesizer functionality is not compromised, the pole is chosen at a frequency of 100 kHz. Resistor R is calculated by setting the voltage division losses of the control signal equal to the voltage division losses of the modulation signal, or:

$$V_{out\_low\_freq} = V_{control} \left( \frac{R_i}{R + R_i} \right) \Rightarrow Loss_L = \frac{R_i}{R + R_i}$$

and

$$V_{out\_high\_freq} = V_{mod} \left( \frac{R \parallel R_i}{R \parallel R_i + 50} \right) \Rightarrow Loss_H = \frac{R \parallel R_i}{R \parallel R_i + 50}$$

where  $R_i$  is the input impedance of the output isolation network. The assumption is made that the capacitor is a perfect short at high frequencies and visa versa. Equating the loss factors of the two situations lead to a resistor value of 3.3 k $\Omega$ .

The final summing network is shown in figure D.5, with the simulated and measured frequency response of both control signal and modulation signal shown in figure D.6. From the figure it is clear that the requirements are fully achieved by this network.

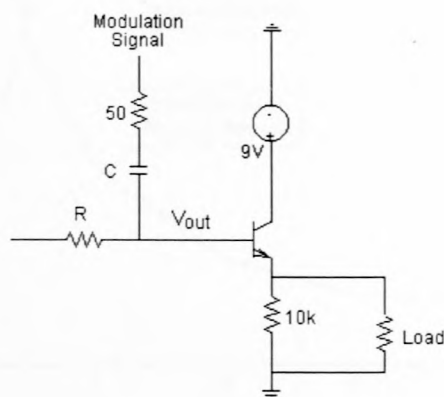


Figure D.4: Nodal Summing Network

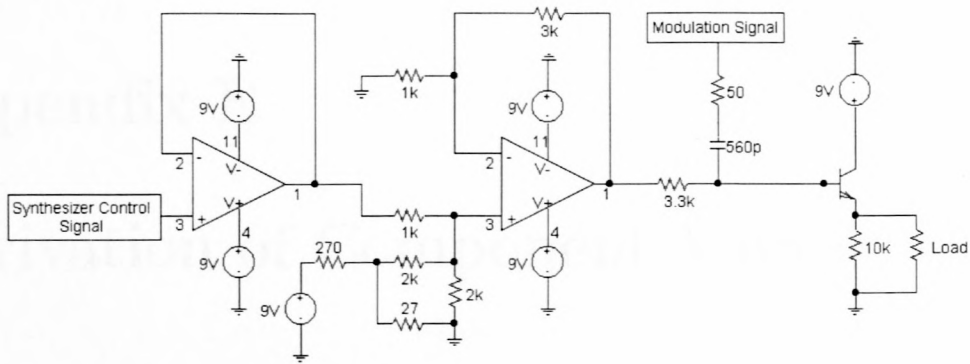


Figure D.5: Summing Network

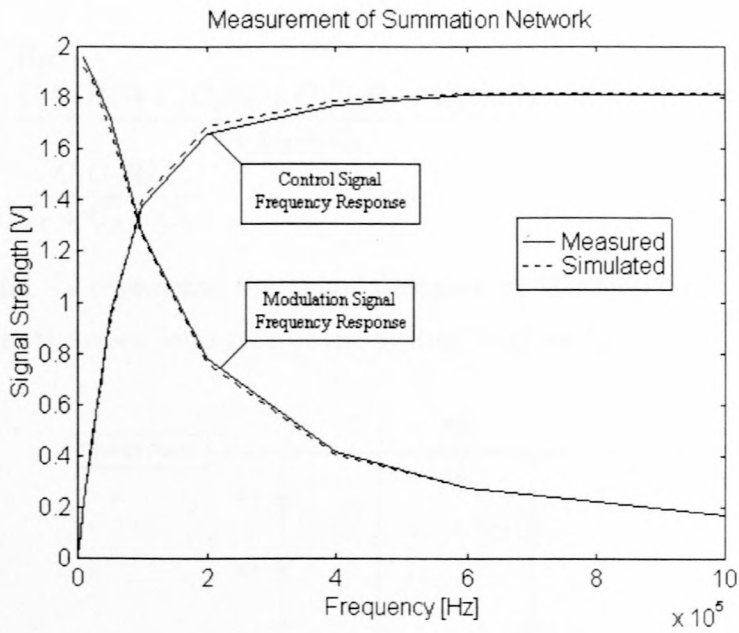


Figure D.6: Frequency Response of Summing Network



# Appendix E

## Derivation of Component Values

This section describes the derivation of the fourth-order system component values, taking charge pump circuitry into account. The transfer function of the fourth-order system is shown in figure E.1 is as follows:

$$Z(s) = \left( \frac{1 + sT_2}{s(1 + sT_1)(1 + sT_3)} \right) \left( \frac{T_1}{C_1T_2} \right) \quad (\text{E.1})$$

with

$$\begin{aligned} T_2 &= R_2C_2 \\ T_1 + T_3 &= \frac{C_2C_3R_2 + C_1C_2R_2 + C_1C_3R_3 + C_2C_3R_3}{C_1 + C_2 + C_3} \\ \frac{T_1 + T_3}{T_2} &= \frac{C_1C_3R_3}{C_1 + C_2 + C_3} \end{aligned}$$

where  $T_1$ ,  $T_2$  and  $T_3$  represents the time constants of the loop filter. Using the filter transfer function, the open-loop gain of the system is given by:

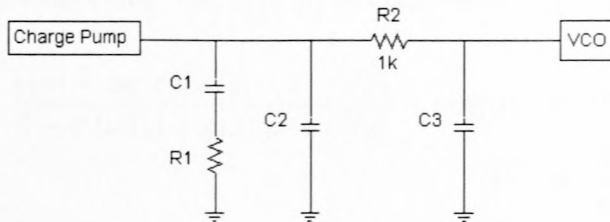


Figure E.1: Passive Third-Order Loop Filter

$$\begin{aligned}
 \text{Gain}_{(\text{Open-Loop})} &= \frac{K_{VCO}K_{\phi}}{s^2N} \left( \frac{1 + sT_2}{(1 + sT_1)(1 + sT_3)} \right) \left( \frac{T_1}{C_1T_2} \right) \\
 &= \frac{K_{VCO}K_{\phi}}{s^2N} \left( \frac{1 + sT_2}{(1 + sT_1)(1 + sT_3)} \right) \left( \frac{1}{C_1 + C_2 + C_3} \right)
 \end{aligned}$$

From the open-loop gain the phase margin equation is obtain as:

$$\phi = \tan^{-1}(\omega T_2) - \tan^{-1}(\omega T_1) - \tan^{-1}(\omega T_3) + 180 \quad (\text{E.2})$$

taking the tangent of both sides yields:

$$\tan(\phi) = \frac{\omega T_2 - \omega^3 T_1 T_2 T_3 - \omega T_1 - \omega T_3}{1 - \omega^2 T_1 T_3 - T_2 \omega^2 (T_1 + T_3)} \quad (\text{E.3})$$

The next step is to derive an exact method for the solving of the time constants  $T_1$  and  $T_2$ . By choosing the loop bandwidth to maximize the phase margin, (taking the derivative of equation (E.2) and setting it equal to zero):

$$\begin{aligned}
 \frac{\omega T_2}{1 + (\omega T_2)^2} &= \frac{\omega T_1}{1 + (\omega T_1)^2} + \frac{\omega T_3}{1 + (\omega T_3)^2} \\
 &= f(\omega T_1)
 \end{aligned} \quad (\text{E.4})$$

Yielding:

$$\begin{aligned}
 \omega T_2 &= \frac{1 \pm \sqrt{1 - 4f(\omega T_1)^2}}{2f(\omega T_1)} \\
 &= g(\omega T_1)
 \end{aligned} \quad (\text{E.5})$$

Banerjee [5] states that in (E.5), it has been found by trial and error that the positive root provides the correct answer. However, it is possible that using the negative root could yield better results in some cases. Using (E.5) to eliminated  $\omega T_2$  in equation (E.3) yields:

$$\begin{aligned}
 \frac{g(x) - xg(x)[\omega T_3] - x - \omega T_3}{1 - x(\omega T_3) + g(x)[x + \omega T_3]} - \tan(\phi) &= 0 \\
 T_1 &= \frac{x}{\omega}
 \end{aligned}$$

Once  $T_1$  is known,  $T_2$  is determined by

$$T_2 = \frac{g(\omega T_1)}{\omega}$$

By definition, the open loop transfer function gain is equal to one at the loop bandwidth.

Therefore,

$$C_1 + C_2 + C_3 = \frac{K_{VCO}K_\phi}{\omega^2 N} \sqrt{\frac{1 + (\omega T_2)^2}{[1 + (\omega T_1)^2][1 + (\omega T_3)^2]}}$$

All the above equations are now incorporated into a system of 4 equations and 4 unknowns that can be solved for one variable. The 4 equations are as follows:

*Constants*

$$k_1 = \frac{K_{VCO}K_\phi}{\omega^2 N} \sqrt{\frac{1 + (\omega T_2)^2}{[1 + (\omega T_1)^2][1 + (\omega T_3)^2]}}$$

$$k_2 = (T_1 + T_3)k_1$$

$$k_3 = \frac{T_1 T_3 k_1}{T_2}$$

$$k_4 = \frac{C_3}{C_1} = \text{To be calculated later}$$

*Equations*

$$k_1 = C_1 + C_2 + C_3$$

$$k_2 = T_2(C_1 + C_3) + R_3 C_3(C_1 + C_2)$$

$$k_3 = R_3 C_1 C_3$$

$$k_4 = \frac{C_3}{C_1}$$

$$k_1 = C_1(k_4 + 1) + C_2$$

$$k_2 = T_2 C_1(k_4 + 1) + k_3 + \frac{k_3 C_2}{C_1}$$

Combining these leads to a quadratic equation that is solved for  $C_1$ :

$$T_2(k_4 + 1)C_1^2 + (k_3 - k_2 - k_3(k_4 + 1))C_1 + k_3 k_1 = 0$$

# Appendix F

## Derivation of Optimal Attenuation for Loop Filter

### F.1 Determining the True Added Attenuation

The forward loop gain ( $G(s)$ ) is the product of the phase detector gain, loop filter transfer function and VCO gain (divided by  $s$ ). As the spurs that must be attenuated by the extra pole is far outside the loop bandwidth, the closed loop transfer function multiplying the spurs can be approximated as:

$$\left| \frac{sG(s)}{1 + \frac{G(s)}{N}} \right| \approx |sG(s)| = \left| \frac{K_\phi K_{VCO}}{C_1 N \omega} \left( \frac{T_1(1 + sT_2)}{T_2(1 + sT_1)(1 + sT_3)} \right) \right|$$

The transfer function is multiplied by  $s$  to transform the phase transfer function to the frequency domain. Taking the magnitude of this equation:

$$|sG(s)| = \frac{K_\phi K_{VCO} T_1}{C_1 N \omega T_2} \sqrt{\frac{1 + \omega^2 T_2^2}{(1 + \omega^2 T_1^2)(1 + \omega^2 T_3^2)}}$$

However,  $C_1$  is not constant and is given by (Refer to Appendix G for the derivation of this equation) :

$$C_1 = \frac{K_\phi K_{VCO} T_1}{N \omega_c^2 T_2} \sqrt{\frac{1 + \omega_c^2 T_2^2}{(1 + \omega_c^2 T_1^2)(1 + \omega_c^2 T_3^2)}}$$

Substitution yields the following expression for  $G(s)$ :

$$|sG(s)| = \frac{\omega_c^2}{\omega} \sqrt{\frac{(1 + \omega^2 T_2^2)(1 + \omega_c^2 T_1^2)(1 + \omega_c^2 T_3^2)}{(1 + \omega_c^2 T_2^2)(1 + \omega^2 T_1^2)(1 + \omega^2 T_3^2)}}$$



Of concern is the spurious attenuation added over a second-order loop filter. During this derivation, the apostrophe (') will denote the values for the second-order filter. The following equations are required for the derivation:

$$T_1 + T_3 = \frac{\sec(\phi_c) - \tan(\phi_c)}{\omega_c} = T'_1$$

$$T'_2 = T_2 = \frac{1}{\omega_c^2(T_1 + T_3)} = \frac{\omega_c}{\sec(\phi_c) - \tan(\phi_c)}$$

with the true added attenuation over the second-order filter given by:

$$A(T_1, T_3) = 10 \log \left| \frac{1 + \omega_c^2(T_1 + T_3)^2}{1 + f_c^2(T_1 + T_3)^2} \frac{1 + f_c^2 T_1^2}{1 + \omega_c^2 T_1^2} \frac{1 + f_c T_3^2}{1 + \omega_c^2 T_3^2} \right|$$

with  $f_c = 2\pi f_{comp}$ .

## F.2 Design for Optimal Attenuation

Designing for optimal attenuation can be stated as follows; with all loop filters with the following values constant:

- $\omega_c$  (Third-Order Closed Loop Bandwidth)
- $\phi_p$  (Second-Order Phase Margin)
- $N$  (High Frequency Divider Ratio)
- $K_{VCO}$  (VCO Gain)
- $K_\phi$  (Charge Pump Gain)
- $f_{comp}$  (Comparison Frequency)

maximize  $A(T_1, T_3)$  subject to the constraint:

$$T_1 + T_3 = constant = \frac{\sec(\phi_c) - \tan(\phi_c)}{\omega_c} = K_{ATTEN} \quad (F.1)$$

Note that this makes  $A(T_1, T_3)$  symmetric in  $T_1$  and  $T_3$ . In other words:

$$A(x, y) = A(y, x) \quad (F.2)$$

This is solved using LaGrange multipliers and the problem is restated as:  
Minimize:

$$Y(T_1, T_3, \lambda) = A(T_1, T_3) + \lambda |K - T_1 - T_3|$$

This is performed by setting:

$$\frac{dY}{dT_1} = \frac{dY}{dT_3} = \frac{dY}{d\lambda} = 0 \quad (\text{F.3})$$

and finding the corresponding values for  $T_1$ ,  $T_3$  and  $\lambda$  satisfying the equation. Proceeding from (F.3) yields:

$$\frac{dY}{dT_1} = \frac{dY}{dT_3} = \lambda \quad (\text{F.4})$$

and

$$K_{ATTEN} = T_1 - T_3 \quad (\text{F.5})$$

where equation (F.5) is satisfied because it is the constraint. Recalling from (F.2) the symmetry properties of  $A(T_1, T_3)$  which also apply to its derivatives, then it follows that (F.4) will be satisfied if:

$$T_1 = T_3$$

Substituting this into (F.1) yields:

$$T_1 = T_3 = \frac{K_{ATTEN}}{2} = \frac{\sec(\phi_c) - \tan(\phi_c)}{2\omega_c}$$

which is the optimal choice of  $T_3$ .

# Appendix G

## Derivation of Equation for $C_1$

### Response

The transfer impedance of the loop filter is:

$$Z = \frac{sR_2C_2 + 1}{s[s^2C_1C_2C_3R_2R_3 + s(C_2C_3R_2 + C_1C_2R_2 + C_1C_3R_3 + C_2C_3R_3) + C_1 + C_2 + C_3]}$$

Assuming now that:

$$C_1 \geq 10C_3$$

equation (12.2) changes to:

$$\begin{aligned} T_2 &= R_2C_2 \\ T_1 + T_3 &= \frac{C_1C_2R_2 + C_1C_3R_3 + C_2C_3R_3}{C_1 + C_2} \\ \frac{T_1 + T_3}{T_2} &= \frac{C_1C_3R_3}{C_1 + C_2} \end{aligned}$$

leading to an open-loop gain equation of:

$$Gain_{OL}|_{s=j\omega} = \frac{-K_\phi K_{VCO}(1 + j\omega T_2) T_1}{\omega^2 C_1 N (1 + j\omega T_1)} \frac{1}{T_2 (1 + j\omega T_3)}$$

At a frequency equal to the loop bandwidth ( $\omega_c$ ), the magnitude of the open-loop gain is per definition 1. Using this condition leads to:

$$C_1 = \frac{K_\phi K_{VCO} T_1}{\omega_c^2 N T_2} \sqrt{\frac{(1 + \omega_c^2 T_2^2)}{(1 + \omega_c^2 T_1^2)(1 + \omega_c^2 T_3^2)}}$$

# Appendix H

## Derivation of Second-Order Transient Response

### H.1 Derivation of Transfer Function

The transfer function of the loop filter is given by:

$$F(s) = \frac{1}{sRC + 1}$$

This leads to the closed-loop transfer function:

$$CL(s) = \frac{N}{\frac{s^2}{\omega_n^2} + \frac{2\xi s}{\omega_n} + 1}$$

where

$$\begin{aligned}\omega_n &= \sqrt{\frac{K}{\tau}} \\ 2\xi &= \frac{\omega_n}{K} = \sqrt{\frac{1}{\tau K}}\end{aligned}$$

### H.2 Second-Order Transient Analysis

The aim of this section is to derive an expression for the transient analysis that can be plotted and properties such as the settling time, rise time, overshoot, ringing and damping factor seen from the graphs. In order to obtain an accurate prediction of the PLL, all the poles and zeros of the transfer function must be included in the analysis. To



achieve this, the transfer function is multiplied by  $\frac{f_2 - f_1}{Ns^2}$  to express the frequency step as a phase step in the Laplace domain. The transfer function is multiplied by  $s$  to represent the transfer function in the frequency domain. The transfer function thus reduces to:

$$\overline{F(s)} = CL(s) \left( \frac{f_2 - f_1}{Ns} \right) = \frac{n_1}{D_2 s^2 + D_1 s + D_0}$$

where

$$\begin{aligned} n_1 &= \frac{K_\phi K_{VCO} K_s (f_2 - f_1)}{N} \\ D_2 &= \tau \\ D_1 &= 1 \\ D_0 &= \frac{K_\phi K_{VCO} K_s}{N} \end{aligned}$$

Since the poles of the transfer function is the zeroes of the denominator, the poles of the system can be calculated numerically. With the poles of the system known, the transfer function can be written as:

$$CL(s) \left( \frac{f_2 - f_1}{Ns} \right) = \sum_{i=0}^3 A_i \left[ \frac{1}{s(s - p_i)} + \frac{R_2 C_2}{s - p_i} \right]$$

$$A_i = n_1 \prod_{k \neq i} \frac{1}{p_i - p_k}$$

From the above equation the transient response is calculated by using the inverse Laplace transform:

$$F(t) = f_2 + \sum_{i=0}^3 A_i e^{p_i t} \left( \frac{1}{p_i} + R_2 C_2 \right)$$

## Appendix I

# Calculation of Frequency Modulated Output Spectrum

This Appendix presents the calculation of the frequency modulated synthesizer output spectrum. This section will almost exclusively be presented from Ziemer and Tranter [20]. With the carrier and modulation signals represented by:

$$\begin{aligned}C(t) &= A_c \cos W_c t \\M(t) &= A_m \cos W_m t\end{aligned}$$

the instantaneous frequency of the output signal is given by:

$$\frac{d\theta(t)}{dt} = 2\pi f_c + kM(t)$$

where  $k$  is the modulation sensitivity in radian frequency per volt. This leads to the angle of the output signal being given by:

$$\theta(t) = \omega_c t + \frac{kA_m}{\omega_m} \sin \omega_m t$$

Manipulation of this equation leads to:

$$Y(t) = A_c \cos \left[ \omega_c t + \frac{kA_m}{\omega_m} \sin \omega_m t \right]$$

The modulation index is defined as:

$$\beta = \frac{kA_m}{\omega_m} = \frac{\frac{kA_m}{2\pi}}{f_m} = \frac{\Delta f}{f_m}$$

where  $\Delta f$  is the maximum carrier frequency deviation by the modulation signal.

An FM signal with a carrier frequency  $\omega_c$  and a message frequency  $\omega_m$  contains an infinite number of spectral components at  $\omega_c \pm n\omega_m$ . The amplitude of each sideband is determined by the Bessel function as obtained from:

$$\begin{aligned}
 \frac{Y(t)}{A_c} &= \cos \left[ \omega_c t + \frac{kA_m}{\omega_m} \sin \omega_m t \right] \\
 &= \sum_{v=-\infty}^{\infty} J_v(\beta) \cos(\omega_c t + v\omega_m t) \\
 &= J_0(\beta) \cos \omega_c t \\
 &+ J_1(\beta) \cos(\omega_c t + \omega_m t) + J_{-1}(\beta) \cos(\omega_c - \omega_m t) \\
 &= J_2(\beta) \cos(\omega_c t + 2\omega_m t) + J_{-2}(\beta) \cos(\omega_c - 2\omega_m t) \\
 &+ \dots
 \end{aligned}$$

where the Bessel function is given by:

$$J_v(\beta) = \sum_{n=0}^{\infty} \frac{(-1)^n}{n! \Gamma(1+v+n)} \left( \frac{\beta}{2} \right)^{2n+v}$$

with  $v$  the order of the Bessel function. Bessel function amplitudes decrease with increasing order. As the modulation index  $\beta$  increases, the spectral energy shifts from the carrier frequency to an increasing number of significant sidebands. This necessitates the use of wider bandwidths for demodulation.



MOTOROLA

MC145170

# PLL Frequency Synthesizer with Serial Interface

## Appendix J

# Motorola MC145170 PLL synthesizer IC Datasheet

The MC145170 is a PLL frequency synthesizer with a serial interface. It is designed for use in portable equipment where space and power consumption are critical. The device is capable of generating frequencies from 100 kHz to 100 MHz with a resolution of 100 kHz. It features a low-power CMOS design and a serial interface for easy integration into microprocessor-based systems.

The MC145170 is available in two versions: MC145170-1 (CMOS) and MC145170-2 (NMOS). The CMOS version is recommended for use in portable equipment due to its low power consumption. The device is available in a 16-pin DIP package.

- Operating Voltage: 2.7V to 5.5V
- Maximum Operating Frequency: 100 MHz
- Operating Current: 100  $\mu$ A to 1 mA
- Operating Temperature Range: -40°C to 85°C
- N Counter Division Range: 1 to 65535
- M Counter Division Range: 1 to 15
- Input Interface: 3-wire Serial Interface
- Output Frequency: 100 kHz to 100 MHz
- Low-Power CMOS Design



COMPARISON OF THE PLL FREQUENCY SYNTHESIZERS

Parameter	MC145170-1	MC145170-2
Maximum Supply Voltage	5.5V	5.5V
Maximum Operating Frequency	100 MHz	100 MHz
Operating Current (I <sub>CC</sub> )	100 $\mu$ A	100 $\mu$ A
Power-On Reset Time	100 $\mu$ s	100 $\mu$ s

FUNCTIONAL BLOCK DIAGRAM

Block	Function
Serial Interface	3-wire Serial Interface
N Counter	1 to 65535
M Counter	1 to 15
PLL Core	100 kHz to 100 MHz




**MOTOROLA**

## PLL Frequency Synthesizer with Serial Interface

The new MC145170-2 is pin-for-pin compatible with the MC145170-1. A comparison of the two parts is shown in the table below. The MC145170-2 is recommended for new designs and has a more robust power-on reset (POR) circuit that is more responsive to momentary power supply interruptions. The two devices are actually the same chip with mask options for the POR circuit. The more robust POR circuit draws approximately 20  $\mu$ A additional supply current. Note that the maximum specification of 100  $\mu$ A quiescent supply current has not changed.

The MC145170-2 is a single-chip synthesizer capable of direct usage in the MF, HF, and VHF bands. A special architecture makes this PLL easy to program. Either a bit- or byte-oriented format may be used. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 2-byte serial transfer to the 16-bit N register.

The device features fully programmable R and N counters, an amplifier at the  $f_{in}$  pin, on-chip support of an external crystal, a programmable reference output, and both single- and double-ended phase detectors with linear transfer functions (no dead zones). A configuration (C) register allows the part to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing noise and interference.

In order to reduce lock times and prevent erroneous data from being loaded into the counters, a patented jam-load feature is included. Whenever a new divide ratio is loaded into the N register, both the N and R counters are jam-loaded with their respective values and begin counting down together. The phase detectors are also initialized during the jam load.

- Operating Voltage Range: 2.7 to 5.5 V
- Maximum Operating Frequency:
  - 185 MHz @  $V_{in} = 500$  mVpp, 4.5 V Minimum Supply
  - 100 MHz @  $V_{in} = 500$  mVpp, 3.0 V Minimum Supply
- Operating Supply Current:
  - 0.6 mA @ 3.0 V, 30 MHz
  - 1.5 mA @ 3.0 V, 100 MHz
  - 3.0 mA @ 5.0 V, 50 MHz
  - 5.8 mA @ 5.0 V, 185 MHz
- Operating Temperature Range: -40 to 85°C
- R Counter Division Range: 1 and 5 to 32,767
- N Counter Division Range: 40 to 65,535
- Direct Interface to Motorola SPI Serial Data Port
- See Application Notes AN1207/D and AN1671/D
- See web site *mot-sps.com* for MC145170 control software. Select in order, Products, Wireless Semiconductor, Download, then PLL Demo Software. Choose PLLGEN.EXE.

BitGrabber is a trademark of Motorola Inc.

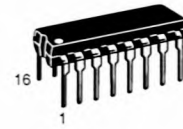
### COMPARISON OF THE PLL FREQUENCY SYNTHESIZERS

Parameter	MC145170-2	MC145170-1
Minimum Supply Voltage	2.7 V	2.5 V
Maximum Input Current, $f_{in}$	150 $\mu$ A	120 $\mu$ A
Dynamic Characteristics, $f_{in}$ (Figure 23)	Unchanged	-
Power-On Reset Circuit	Improved	-

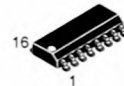
## MC145170-2

### CMOS PLL FREQUENCY SYNTHESIZER WITH SERIAL INTERFACE

SEMICONDUCTOR  
TECHNICAL DATA



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 648

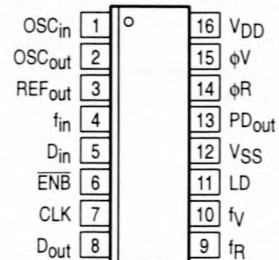


**D SUFFIX**  
PLASTIC PACKAGE  
CASE 751B  
(SOG-16)



**DT SUFFIX**  
PLASTIC PACKAGE  
CASE 948C  
(TSSOP-16)

### PIN CONNECTIONS

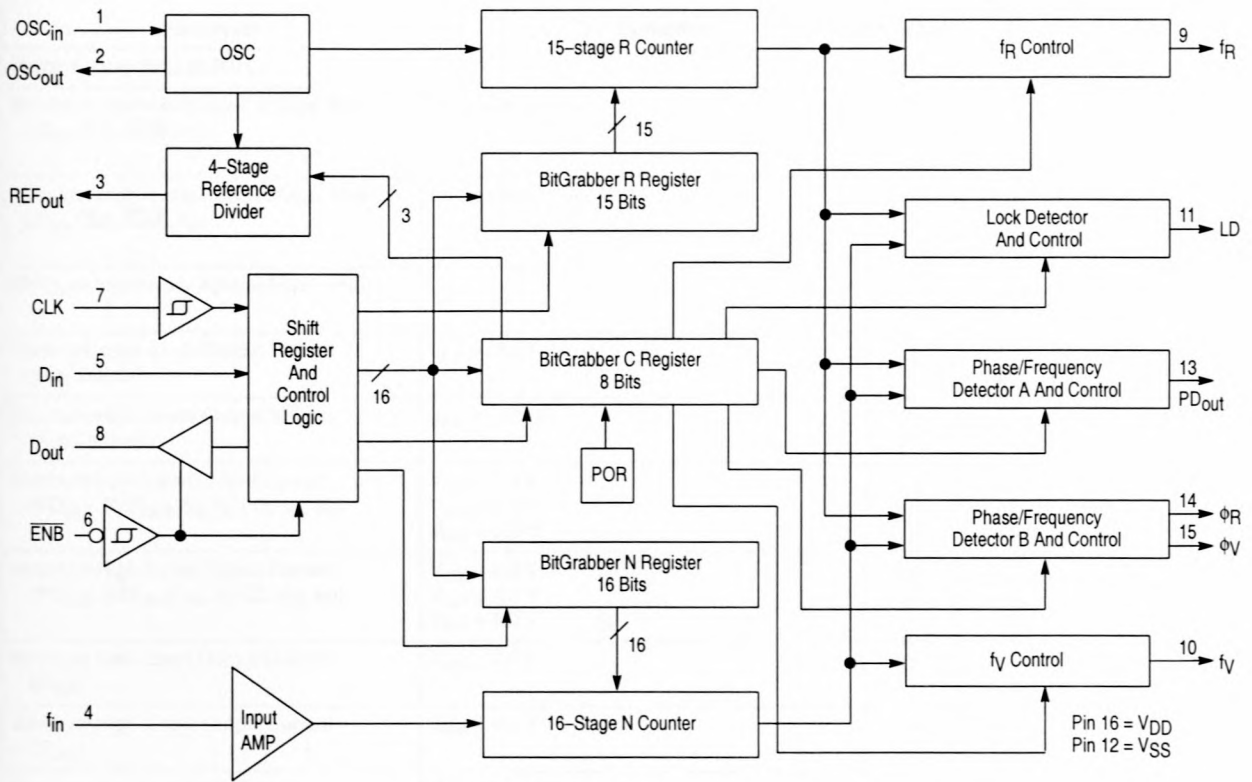


(Top View)

### ORDERING INFORMATION

Device	Operating Temp Range	Package
MC145170P2	$T_A = -40$ to $85^\circ\text{C}$	Plastic DIP
MC145170D2		SOG-16
MC145170DT2		TSSOP-16

## MC145170-2 BLOCK DIAGRAM



This device contains 4,800 active transistors.

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

Parameter	Symbol	Value	Unit
DC Supply Voltage	$V_{DD}$	-0.5 to 5.5	V
DC Input Voltage	$V_{in}$	-0.5 to $V_{DD} + 0.5$	V
DC Output Voltage	$V_{out}$	-0.5 to $V_{DD} + 0.5$	V
DC Input Current, per Pin	$I_{in}$	$\pm 10$	mA
DC Output Current, per Pin	$I_{out}$	$\pm 20$	mA
DC Supply Current, $V_{DD}$ and $V_{SS}$ Pins	$I_{DD}$	$\pm 30$	mA
Power Dissipation, per Package	$P_D$	300	mW
Storage Temperature	$T_{stg}$	-65 to 150	$^{\circ}C$
Lead Temperature, 1 mm from Case for 10 seconds	$T_L$	260	$^{\circ}C$

**NOTES:** 1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.  
2. ESD data available upon request.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

## MC145170-2

### ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$ , $T_A = -40$ to $85^\circ\text{C}$ )

Parameter	Test Condition	Symbol	$V_{DD}$ V	Guaranteed Limit	Unit
Power Supply Voltage Range		$V_{DD}$	–	2.7 to 5.5	V
Maximum Low-Level Input Voltage [Note 1] ( $D_{in}$ , CLK, $\overline{ENB}$ , $f_{in}$ )	dc Coupling to $f_{in}$	$V_{IL}$	2.7 4.5 5.5	0.54 1.35 1.65	V
Minimum High-Level Input Voltage [Note 1] ( $D_{in}$ , CLK, $\overline{ENB}$ , $f_{in}$ )	dc Coupling to $f_{in}$	$V_{IH}$	2.7 4.5 5.5	2.16 3.15 3.85	V
Minimum Hysteresis Voltage (CLK, $\overline{ENB}$ )		$V_{Hys}$	2.7 5.5	0.15 0.20	V
Maximum Low-Level Output Voltage (Any Output)	$I_{out} = 20 \mu\text{A}$	$V_{OL}$	2.7 5.5	0.1 0.1	V
Minimum High-Level Output Voltage (Any Output)	$I_{out} = -20 \mu\text{A}$	$V_{OH}$	2.7 5.5	2.6 5.4	V
Minimum Low-Level Output Current ( $PD_{out}$ , $REF_{out}$ , $f_R$ , $f_V$ , LD, $\phi_R$ , $\phi_V$ )	$V_{out} = 0.3 \text{ V}$ $V_{out} = 0.4 \text{ V}$ $V_{out} = 0.5 \text{ V}$	$I_{OL}$	2.7 4.5 5.5	0.12 0.36 0.36	mA
Minimum High-Level Output Current ( $PD_{out}$ , $REF_{out}$ , $f_R$ , $f_V$ , LD, $\phi_R$ , $\phi_V$ )	$V_{out} = 2.4 \text{ V}$ $V_{out} = 4.1 \text{ V}$ $V_{out} = 5.0 \text{ V}$	$I_{OH}$	2.7 4.5 5.5	-0.12 -0.36 -0.36	mA
Minimum Low-Level Output Current ( $D_{out}$ )	$V_{out} = 0.4 \text{ V}$	$I_{OL}$	4.5	1.6	mA
Minimum High-Level Output Current ( $D_{out}$ )	$V_{out} = 4.1 \text{ V}$	$I_{OH}$	4.5	-1.6	mA
Maximum Input Leakage Current ( $D_{in}$ , CLK, $\overline{ENB}$ , $OSC_{in}$ )	$V_{in} = V_{DD}$ or $V_{SS}$	$I_{in}$	5.5	$\pm 1.0$	$\mu\text{A}$
Maximum Input Current ( $f_{in}$ )	$V_{in} = V_{DD}$ or $V_{SS}$	$I_{in}$	5.5	$\pm 150$	$\mu\text{A}$
Maximum Output Leakage Current ( $PD_{out}$ )  ( $D_{out}$ )	$V_{in} = V_{DD}$ or $V_{SS}$ , Output in High-Impedance State	$I_{OZ}$	5.5  5.5	$\pm 100$  $\pm 5.0$	nA  $\mu\text{A}$
Maximum Quiescent Supply Current	$V_{in} = V_{DD}$ or $V_{SS}$ ; Outputs Open; Excluding $f_{in}$ Amp Input Current Component	$I_{DD}$	5.5	100	$\mu\text{A}$
Maximum Operating Supply Current	$f_{in} = 500 \text{ mVpp}$ ; $OSC_{in} = 1.0 \text{ MHz @ } 1.0 \text{ Vpp}$ ; LD, $f_R$ , $f_V$ , $REF_{out}$ = Inactive and No Connect; $OSC_{out}$ , $\phi_V$ , $\phi_R$ , $PD_{out}$ = No Connect; $D_{in}$ , $\overline{ENB}$ , CLK = $V_{DD}$ or $V_{SS}$	$I_{dd}$	–	[Note 2]	mA

NOTES: 1. When dc coupling to the  $OSC_{in}$  pin is used, the pin must be driven rail-to-rail. In this case,  $OSC_{out}$  should be floated.

2. The nominal values at 3.0 V are 0.6 mA @ 30 MHz, and 1.5 mA @ 100 MHz. The nominal values at 5.0 V are 3.0 mA @ 50 MHz, and 5.8 mA @ 185 MHz. These are not guaranteed limits.

## MC145170-2

**AC INTERFACE CHARACTERISTICS** (  $T_A = -40$  to  $85^\circ\text{C}$ ,  $C_L = 50$  pF, Input  $t_r = t_f = 10$  ns, unless otherwise noted.)

Parameter	Symbol	Figure No.	V <sub>DD</sub> V	Guaranteed Limit	Unit
Serial Data Clock Frequency (Note: Refer to Clock $t_w$ Below)	$f_{clk}$	1	2.7 4.5 5.5	dc to 3.0 dc to 4.0 dc to 4.0	MHz
Maximum Propagation Delay, CLK to D <sub>out</sub>	$t_{PLH}$ , $t_{PHL}$	1, 5	2.7 4.5 5.5	150 85 85	ns
Maximum Disable Time, D <sub>out</sub> Active to High Impedance	$t_{PLZ}$ , $t_{PHZ}$	2, 6	2.7 4.5 5.5	300 200 200	ns
Access Time, D <sub>out</sub> High Impedance to Active	$t_{PZL}$ , $t_{PZH}$	2, 6	2.7 4.5 5.5	0 to 200 0 to 100 0 to 100	ns
Maximum Output Transition Time, D <sub>out</sub>	$t_{TLH}$ , $t_{THL}$	1, 5	2.7	150	ns
			4.5	50	
			5.5	50	
		1, 5	2.7	900	ns
			4.5	150	
			5.5	150	
Maximum Input Capacitance – D <sub>in</sub> , $\overline{\text{ENB}}$ , CLK	$C_{in}$		–	10	pF
Maximum Output Capacitance – D <sub>out</sub>	$C_{out}$		–	10	pF

**TIMING REQUIREMENTS** (  $T_A = -40$  to  $85^\circ\text{C}$ , Input  $t_r = t_f = 10$  ns, unless otherwise noted.)

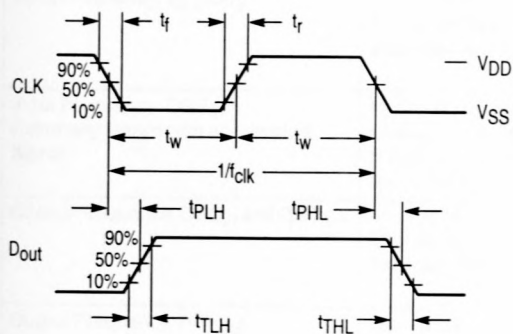
Parameter	Symbol	Figure No.	V <sub>DD</sub> V	Guaranteed Limit	Unit
Minimum Setup and Hold Times, D <sub>in</sub> vs CLK	$t_{su}$ , $t_h$	3	2.7 4.5 5.5	55 40 40	ns
Minimum Setup, Hold, and Recovery Times, $\overline{\text{ENB}}$ vs CLK	$t_{su}$ , $t_h$ , $t_{rec}$	4	2.7 4.5 5.5	135 100 100	ns
Minimum Inactive-High Pulse Width, $\overline{\text{ENB}}$	$t_{w(H)}$	4	2.7 4.5 5.5	400 300 300	ns
Minimum Pulse Width, CLK	$t_w$	1	2.7 4.5 5.5	166 125 125	ns
Maximum Input Rise and Fall Times, CLK	$t_r$ , $t_f$	1	2.7 4.5 5.5	100 100 100	$\mu\text{s}$



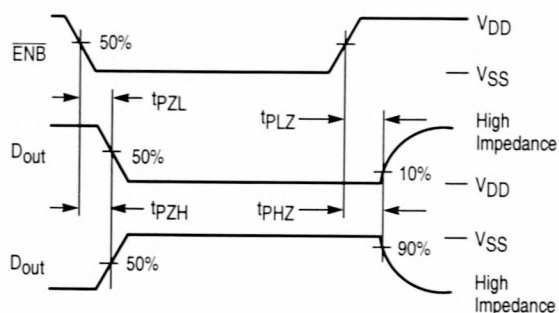
# MC145170-2

## SWITCHING WAVEFORMS

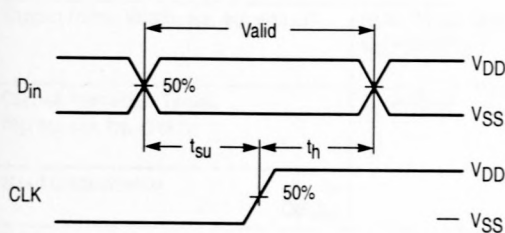
**Figure 1.**



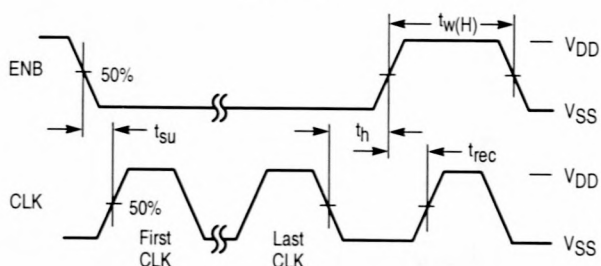
**Figure 2.**



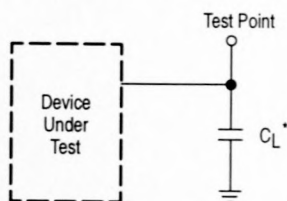
**Figure 3.**



**Figure 4.**

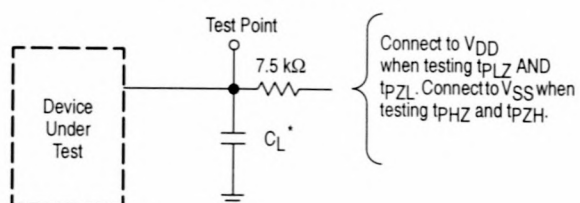


**Figure 5. Test Circuit**



\* Includes all probe and fixture capacitance.

**Figure 6. Test Circuit**



\* Includes all probe and fixture capacitance.

## MC145170-2

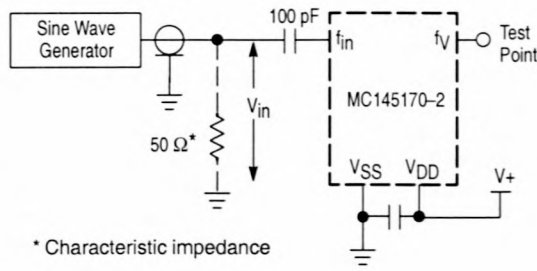
### LOOP SPECIFICATIONS ( $T_A = -40$ to $85^\circ\text{C}$ )

Parameter	Test Condition	Symbol	Figure No.	V <sub>DD</sub> V	Guaranteed Range		Unit
					Min	Max	
Input Frequency, $f_{in}$ [Note]	$V_{in} \geq 500$ mVpp Sine Wave, N Counter Set to Divide Ratio Such that $f_y \leq 2.0$ MHz	f	7	2.7 3.0 4.5 5.5	5.0 5.0 25 45	80 100 185 185	MHz
Input Frequency, OSC <sub>in</sub> Externally Driven with ac-coupled Signal	$V_{in} \geq 1.0$ V <sub>pp</sub> Sine Wave, OSC <sub>out</sub> = No Connect, R Counter Set to Divide Ratio Such that $f_R \leq 2$ MHz	f	8a	2.7 3.0 4.5 5.5	1.0* 1.0* 1.0* 1.0*	22 25 30 35	MHz
Crystal Frequency, OSC <sub>in</sub> and OSC <sub>out</sub>	$C1 \leq 30$ pF $C2 \leq 30$ pF Includes Stray Capacitance	f <sub>XTAL</sub>	9	2.7 3.0 4.5 5.5	2.0 2.0 2.0 2.0	12 12 15 15	MHz
Output Frequency, REF <sub>out</sub>	$C_L = 30$ pF	f <sub>out</sub>	10, 12	2.7 4.5 5.5	dc dc dc	– 10 10	MHz
Operating Frequency of the Phase Detectors		f		2.7 4.5 5.5	dc dc dc	– 2.0 2.0	MHz
Output Pulse Width, $\phi_R$ , $\phi_V$ , and LD	$f_R$ in Phase with $f_y$ $C_L = 50$ pF	t <sub>w</sub>	11, 12	2.7 4.5 5.5	– 20 16	– 100 90	ns
Output Transition Times, $\phi_R$ , $\phi_V$ , LD, $f_R$ , and $f_y$	$C_L = 50$ pF	t <sub>TLH</sub> , t <sub>THL</sub>	11, 12	2.7 4.5 5.5	– – –	– 65 60	ns
Input Capacitance $f_{in}$ OSC <sub>in</sub>		C <sub>in</sub>	– –	– –	– –	7.0 7.0	pF

\* IF lower frequency is desired, use wave shaping or higher amplitude sinusoidal signal in ac-coupled case. Also, see Figure 22 for dc coupling.

# MC145170-2

Figure 7. Test Circuit,  $f_{in}$



\* Characteristic impedance

Figure 8.

Figure 8a. Test Circuit, OSC Circuit Externally Driven [Note]

Figure 8b. Circuit to Eliminate Self-Oscillation, OSC Circuit Externally Driven [Note]

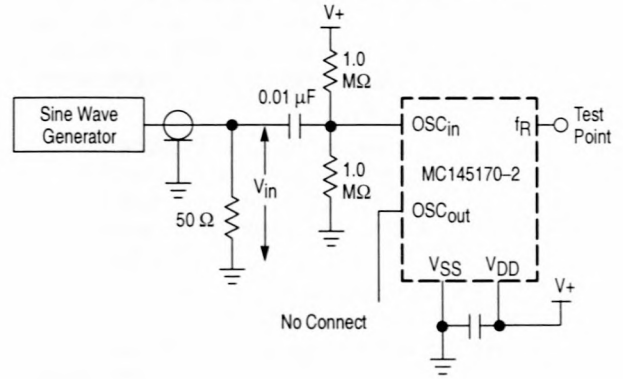
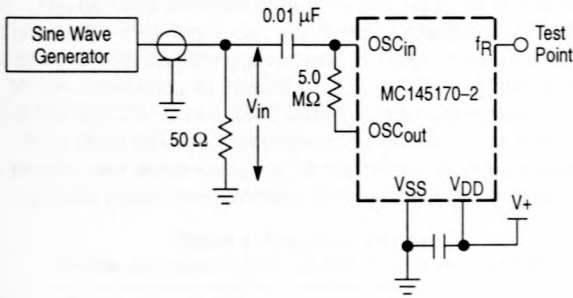


Figure 9. Test Circuit, OSC Circuit with Crystal

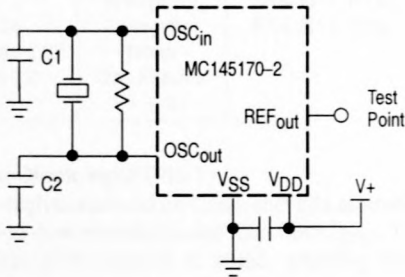


Figure 10. Switching Waveform

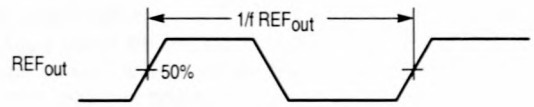


Figure 11. Switching Waveform

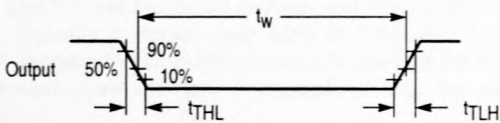
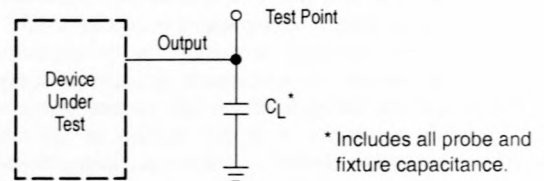


Figure 12. Test Load Circuit



**NOTE:** Use the circuit of Figure 8b to eliminate self-oscillation of the OSC<sub>in</sub> pin when the MC145170-2 has power applied with no external signal applied at V<sub>in</sub>. (Self-oscillation is not harmful to the MC145170-2 and does not damage the IC.)

## MC145170-2

### PIN DESCRIPTIONS

#### DIGITAL INTERFACE PINS

##### **D<sub>in</sub>**

##### **Serial Data Input (Pin 5)**

The bit stream begins with the most significant bit (MSB) and is shifted in on the low-to-high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the N register, or 3 bytes (24 bits) to access the R register. Additionally, the R register can be accessed with a 15-bit transfer (see Table 1). An optional pattern which resets the device is shown in Figure 13. The values in the C, N, and R registers do not change during shifting because the transfer of data to the registers is controlled by  $\overline{\text{ENB}}$ .

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided (i.e., the registers may be accessed in any sequence). Data is retained in the registers over a supply range of 2.7 to 5.5 V. The formats are shown in Figures 13, 14, 15, and 16.

$D_{in}$  typically switches near 50% of  $V_{DD}$  to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail-to-rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull-up resistor of 1 to 10 k $\Omega$  must be used. Parameters to consider when sizing the resistor are worst-case  $I_{OL}$  of the driving device, maximum tolerable power consumption, and maximum data rate.

**Table 1. Register Access**

(MSBs are shifted in first, C0, N0, and R0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
9 to 13	See Figure 13	(Reset)
8	C Register	C7, C6, C5, . . . , C0
16	N Register	N15, N14, N13, . . . , N0
15 or 24	R Register	R14, R13, R12, . . . , R0
Other Values $\leq$ 32	None	
Values > 32	See Figures 24 — 31	

##### **CLK**

##### **Serial Data Clock Input (Pin 7)**

Low-to-high transitions on Clock shift bits available at  $D_{in}$ , while high-to-low transitions shift bits from  $D_{out}$ . The chip's 16-1/2-stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Four to eight clock cycles followed by five clock cycles are needed to reset the device; this is optional. Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the N register. Either 15 or 24 cycles can be used to access the R register (see Table 1 and Figures 13, 14, 15, and 16). For cascaded devices, see Figures 24 to 31.

CLK typically switches near 50% of  $V_{DD}$  and has a Schmitt-triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D<sub>in</sub>** for more information.

##### **NOTE**

To guarantee proper operation of the power-on reset (POR) circuit, the CLK pin must be held at the potential of either the  $V_{SS}$  or  $V_{DD}$  pin during power up. That is, the CLK input should not be floated or toggled while the  $V_{DD}$  pin is ramping from 0 to at least 2.7 V. If control of the CLK pin is not practical during power up, the initialization sequence shown in Figure 13 must be used.

##### $\overline{\text{ENB}}$

##### **Active-Low Enable Input (Pin 6)**

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When  $\overline{\text{ENB}}$  is in an inactive high state, shifting is inhibited,  $D_{out}$  is forced to the high-impedance state, and the port is held in the initialized state. To transfer data to the device,  $\overline{\text{ENB}}$  (which must start inactive high) is taken low, a serial transfer is made via  $D_{in}$  and CLK, and  $\overline{\text{ENB}}$  is taken back high. The low-to-high transition on  $\overline{\text{ENB}}$  transfers data to the C, N, or R register depending on the data stream length per Table 1.

##### **NOTE**

Transitions on  $\overline{\text{ENB}}$  must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when  $\overline{\text{ENB}}$  is high and CLK is low.

This input is also Schmitt-triggered and switches near 50% of  $V_{DD}$ , thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D<sub>in</sub>** for more information.

##### **D<sub>out</sub>**

##### **Three-State Serial Data Output (Pin 8)**

Data is transferred out of the 16-1/2-stage shift register through  $D_{out}$  on the high-to-low transition of CLK. This output is a No Connect, unless used in one of the manners discussed below.

$D_{out}$  could be fed back to an MCU/MPU to perform a wrap-around test of serial data. This could be part of a system check conducted at power up to test the integrity of the system's processor, PC board traces, solder joints, etc.

The pin could be monitored at an in-line QA test during board manufacturing.

Finally,  $D_{out}$  facilitates troubleshooting a system and permits cascading devices.

##### **REFERENCE PINS**

##### **OSC<sub>in</sub>/OSC<sub>out</sub>**

##### **Reference Oscillator Input/Output (Pins 1, 2)**

These pins form a reference oscillator when connected to terminals of an external parallel-resonant crystal. Frequency-setting capacitors of appropriate values as recommended by the crystal supplier are connected from each pin to ground (up to a maximum of 30 pF each, including stray capacitance). An external feedback resistor of 1.0 to 5.0 M $\Omega$  is connected directly across the pins to ensure linear operation of the amplifier. The required connections for the components are shown in Figure 9.

If desired, an external clock source can be ac coupled to OSC<sub>in</sub>. A 0.01  $\mu$ F coupling capacitor is used for measurement purposes and is the minimum size



## MC145170-2

recommended for applications. An external feedback resistor of approximately  $5\text{ M}\Omega$  is required across the  $\text{OSC}_{\text{IN}}$  and  $\text{OSC}_{\text{OUT}}$  pins in the ac-coupled case (see Figure 8a or alternate circuit 8b).  $\text{OSC}_{\text{OUT}}$  is an internal node on the device and should not be used to drive any loads (i.e.,  $\text{OSC}_{\text{OUT}}$  is unbuffered). However, the buffered  $\text{REF}_{\text{OUT}}$  is available to drive external loads.

The external signal level must be at least  $1\text{ V}_{\text{p-p}}$ ; the maximum frequencies are given in the **Loop Specifications** table. These maximum frequencies apply for R Counter divide ratios as indicated in the table. For very small ratios, the maximum frequency is limited to the divide ratio times  $2\text{ MHz}$ . (Reason: the phase/frequency detectors are limited to a maximum input frequency of  $2\text{ MHz}$ .)

If an external source is available which swings virtually rail-to-rail ( $\text{V}_{\text{DD}}$  to  $\text{V}_{\text{SS}}$ ), then dc coupling can be used. In the dc-coupled case, no external feedback resistor is needed.  $\text{OSC}_{\text{OUT}}$  must be a No Connect to avoid loading an internal node on the device, as noted above. For frequencies below  $1\text{ MHz}$ , dc coupling must be used. The R counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the  $\text{OSC}_{\text{IN}}$  pin. See Figure 22.

Each rising edge on the  $\text{OSC}_{\text{IN}}$  pin causes the R counter to decrement by one.

### $\text{REF}_{\text{OUT}}$

#### Reference Frequency Output (Pin 3)

This output is the buffered output of the crystal-generated reference frequency or externally provided reference source. This output may be enabled, disabled, or scaled via bits in the C register (see Figure 14).

$\text{REF}_{\text{OUT}}$  can be used to drive a microprocessor clock input, thereby saving a crystal. Upon power up, the on-chip power-on-initialize circuit forces  $\text{REF}_{\text{OUT}}$  to the  $\text{OSC}_{\text{IN}}$  divided-by-8 mode.

$\text{REF}_{\text{OUT}}$  is capable of operation to  $10\text{ MHz}$ ; see the **Loop Specifications** table. Therefore, divide values for the reference divider are restricted to two or higher for  $\text{OSC}_{\text{IN}}$  frequencies above  $10\text{ MHz}$ .

If unused, the pin should be floated and should be disabled via the C register to minimize dynamic power consumption and electromagnetic interference (EMI).

## COUNTER OUTPUT PINS

### $f_{\text{R}}$

#### R Counter Output (Pin 9)

This signal is the buffered output of the 15-stage R counter.  $f_{\text{R}}$  can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The  $f_{\text{R}}$  signal can be used to verify the R counter's divide ratio. This ratio extends from 5 to  $32,767$  and is determined by the binary value loaded into the R register. Also, direct access to the phase detector via the  $\text{OSC}_{\text{IN}}$  pin is allowed by choosing a divide value of 1 (see Figure 15). The maximum frequency which the phase detectors operate is  $2\text{ MHz}$ . Therefore, the frequency of  $f_{\text{R}}$  must not exceed  $2\text{ MHz}$ .

When activated, the  $f_{\text{R}}$  signal appears as normally low and pulses high. The pulse width is 4.5 cycles of the  $\text{OSC}_{\text{IN}}$  pin signal, except when a divide ratio of 1 is selected. When 1 is

selected, the  $\text{OSC}_{\text{IN}}$  signal is buffered and appears at the  $f_{\text{R}}$  pin.

### $f_{\text{V}}$

#### N Counter Output (Pin 10)

This signal is the buffered output of the 16-stage N counter.  $f_{\text{V}}$  can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The  $f_{\text{V}}$  signal can be used to verify the N counter's divide ratio. This ratio extends from 40 to  $65,535$  and is determined by the binary value loaded into the N register. The maximum frequency which the phase detectors operate is  $2\text{ MHz}$ . Therefore, the frequency of  $f_{\text{V}}$  must not exceed  $2\text{ MHz}$ .

When activated, the  $f_{\text{V}}$  signal appears as normally low and pulses high.

## LOOP PINS

### $f_{\text{IN}}$

#### Frequency Input (Pin 4)

This pin is a frequency input from the VCO. This pin feeds the on-chip amplifier which drives the N counter. This signal is normally sourced from an external voltage-controlled oscillator (VCO), and is ac-coupled into  $f_{\text{IN}}$ . A  $100\text{ pF}$  coupling capacitor is used for measurement purposes and is the minimum size recommended for applications (see Figure 7). The frequency capability of this input is dependent on the supply voltage as listed in the **Loop Specifications** table. For small divide ratios, the maximum frequency is limited to the divide ratio times  $2\text{ MHz}$ . (Reason: the phase/frequency detectors are limited to a maximum frequency of  $2\text{ MHz}$ .)

For signals which swing from at least the  $\text{V}_{\text{IL}}$  to  $\text{V}_{\text{IH}}$  levels listed in the **Electrical Characteristics** table, dc coupling may be used. Also, for low frequency signals (less than the minimum frequencies shown in the **Loop Specifications** table), dc coupling is a requirement. The N counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the  $f_{\text{IN}}$  pin. See Figure 22.

Each rising edge on the  $f_{\text{IN}}$  pin causes the N counter to decrement by 1.

### $\text{PD}_{\text{OUT}}$

#### Single-Ended Phase/Frequency Detector Output (Pin 13)

This is a three-state output for use as a loop error signal when combined with an external low-pass filter. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 14)

Frequency of  $f_{\text{V}} > f_{\text{R}}$  or Phase of  $f_{\text{V}}$  Leading  $f_{\text{R}}$ : negative pulses from high impedance

Frequency of  $f_{\text{V}} < f_{\text{R}}$  or Phase of  $f_{\text{V}}$  Lagging  $f_{\text{R}}$ : positive pulses from high impedance

Frequency and Phase of  $f_{\text{V}} = f_{\text{R}}$ : essentially high-impedance state; voltage at pin determined by loop filter

POL bit (C7) = high

## MC145170-2

Frequency of  $f_V > f_R$  or Phase of  $f_V$  Leading  $f_R$ : positive pulses from high impedance

Frequency of  $f_V < f_R$  or Phase of  $f_V$  Lagging  $f_R$ : negative pulses from high impedance

Frequency and Phase of  $f_V = f_R$ : essentially high-impedance state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired,  $PD_{out}$  can be forced to the high-impedance state by utilization of the disable feature in the C register (patented).

### $\phi_R$ and $\phi_V$

#### Double-Ended Phase/Frequency Detector Outputs (Pins 14, 15)

These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 14)

Frequency of  $f_V > f_R$  or Phase of  $f_V$  Leading  $f_R$ :  $\phi_V =$  negative pulses,  $\phi_R =$  essentially high

Frequency of  $f_V < f_R$  or Phase of  $f_V$  Lagging  $f_R$ :  $\phi_V =$  essentially high,  $\phi_R =$  negative pulses

Frequency and Phase of  $f_V = f_R$ :  $\phi_V$  and  $\phi_R$  remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high

Frequency of  $f_V > f_R$  or Phase of  $f_V$  Leading  $f_R$ :  $\phi_R =$  negative pulses,  $\phi_V =$  essentially high

Frequency of  $f_V < f_R$  or Phase of  $f_V$  Lagging  $f_R$ :  $\phi_R =$  essentially high,  $\phi_V =$  negative pulses

Frequency and Phase of  $f_V = f_R$ :  $\phi_V$  and  $\phi_R$  remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via the C register (patented).

### LD

#### Lock Detector Output (Pin 11)

This output is essentially at a high level with narrow low-going pulses when the loop is locked ( $f_R$  and  $f_V$  of the same phase and frequency). The output pulses low when  $f_V$  and  $f_R$  are out of phase or different frequencies (see Figure 17).

This output can be enabled and disabled via the C register (patented). Upon power up, on-chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

### POWER SUPPLY

#### V<sub>DD</sub>

##### Most Positive Supply Potential (Pin 16)

This pin may range from 2.7 to 5.5 V with respect to  $V_{SS}$ .

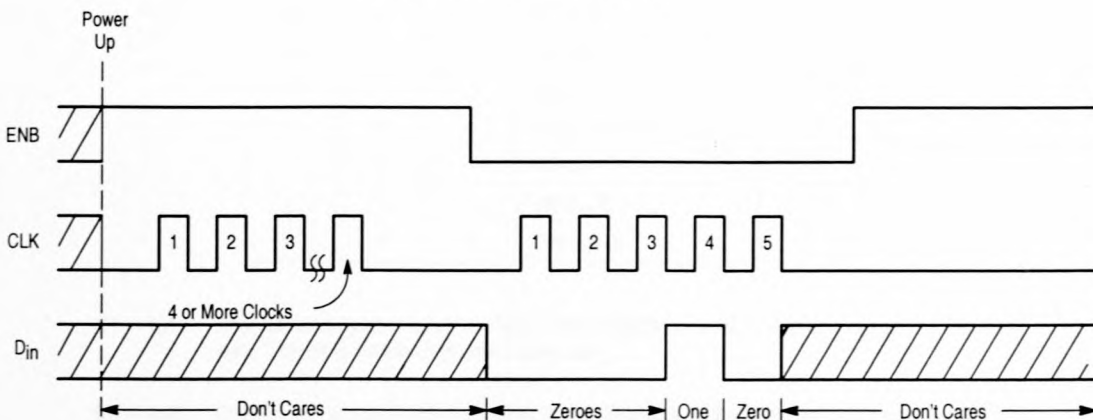
For optimum performance,  $V_{DD}$  should be bypassed to  $V_{SS}$  using low-inductance capacitor(s) mounted very close to the device. Lead lengths on the capacitor(s) should be minimized. (The very fast switching speed of the device causes current spikes on the power leads.)

#### V<sub>SS</sub>

##### Most Negative Supply Potential (Pin 12)

This pin is usually ground. For measurement purposes, the  $V_{SS}$  pin is tied to a ground plane.

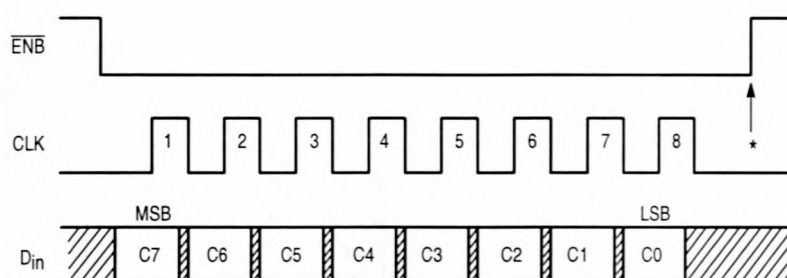
Figure 13. Reset Sequence



**NOTE:** This initialization sequence is usually not necessary because the on-chip power-on reset circuit performs the initialization function. However, this initialization sequence must be used immediately after power up if control of the CLK pin is not possible. That is, if CLK (Pin 7) toggles or floats upon power up, use the above sequence to reset the device. Also, use this sequence if power is momentarily interrupted such that the supply voltage to the device is reduced to below 2.7 V, but not down to at least 1 V (for example, the supply drops down to 2 V). This is necessary because the on-chip power-on reset is only activated when the supply ramps up from a voltage below approximately 1.0 V.

## MC145170-2

Figure 14. C Register Access and Format (8 Clock Cycles are Used)



\* At this point, the new byte is transferred to the C register and stored. No other registers are affected.

- C7 — POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts  $PD_{out}$  and interchanges the  $\phi_R$  function with  $\phi_V$  as depicted in Figure 17. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.
- C6 — PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A ( $PD_{out}$ ) and disables phase/frequency detector B by forcing  $\phi_R$  and  $\phi_V$  to the static high state. When cleared low, phase/frequency detector B is enabled ( $\phi_R$  and  $\phi_V$ ) and phase/frequency detector A is disabled with  $PD_{out}$  forced to the high-impedance state. This bit is cleared low at power up.
- C5 — LDE: Enables the lock detector output when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.
- C4 — C2, OSC2 — OSC0: Reference output controls which determine the  $REF_{out}$  characteristics as shown below. Upon power up, the bits are initialized such that  $OSC_{in}/8$  is selected.

C4	C3	C2	$REF_{out}$ Frequency
0	0	0	dc (Static Low)
0	0	1	$OSC_{in}$
0	1	0	$OSC_{in}/2$
0	1	1	$OSC_{in}/4$
1	0	0	$OSC_{in}/8$ (POR Default)
1	0	1	$OSC_{in}/16$
1	1	0	$OSC_{in}/8$
1	1	1	$OSC_{in}/16$

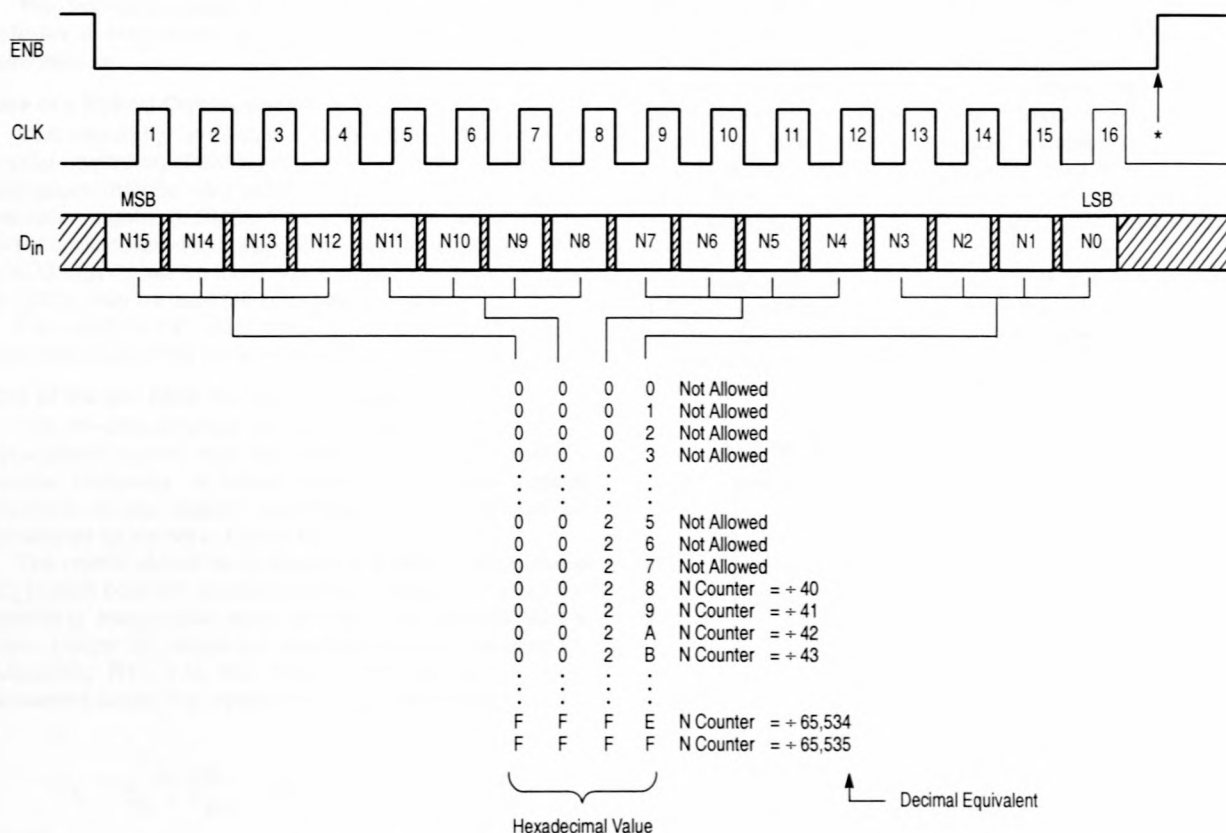
- C1 —  $f_V$ E: Enables the  $f_V$  output when set high. When cleared low, the  $f_V$  output is forced to a static low level. The bit is cleared low upon power up.
- C0 —  $f_R$ E: Enables the  $f_R$  output when set high. When cleared low, the  $f_R$  output is forced to a static low level. The bit is cleared low upon power up.





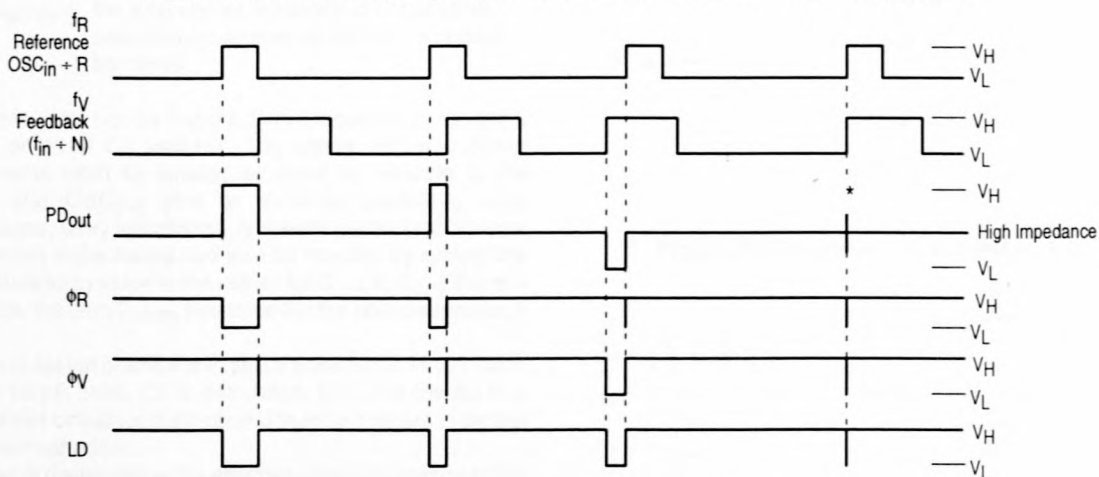
# MC145170-2

Figure 16. N Register Access and Format (16 Clock Cycles Are Used)



\* At this point, the two new bytes are transferred to the N register and stored. No other registers are affected. In addition, the N and R counters are jam-loaded and begin counting down together.

Figure 17. Phase/Frequency Detectors and Lock Detector Output Waveforms



$V_H$  = High voltage level

$V_L$  = Low voltage level

\* At this point, when both  $f_R$  and  $f_V$  are in phase, both the sinking and sourcing output FETs are turned on for a very short interval.

**NOTE:** The  $PD_{out}$  generates error pulses during out-of-lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low-pass filter capacitor.  $PD_{out}$ ,  $\phi_R$ , and  $\phi_V$  are shown with the polarity bit (POL) = low; see Figure 14 for POL.

## MC145170-2 DESIGN CONSIDERATIONS

### CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

#### Use of a Hybrid Crystal Oscillator

Commercially available temperature-compensated crystal oscillators (TCXOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to OSC<sub>in</sub>. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC<sub>in</sub> may be used (see Figures 8a and 8b).

For additional information about TCXOs, visit [motorola.com](http://motorola.com) on the world wide web.

#### Use of the On-Chip Oscillator Circuitry

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 18.

The crystal should be specified for a loading capacitance ( $C_L$ ) which does not exceed 20 pF when used at the highest operating frequencies listed in the **Loop Specifications** table. Larger  $C_L$  values are possible for lower frequencies. Assuming  $R_1 = 0 \Omega$ , the shunt load capacitance ( $C_L$ ) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C_1 \times C_2}{C_1 + C_2}$$

where

$C_{in} = 5.0 \text{ pF}$  (see Figure 19)

$C_{out} = 6.0 \text{ pF}$  (see Figure 19)

$C_a = 1.0 \text{ pF}$  (see Figure 19)

$C_1$  and  $C_2 =$  external capacitors (see Figure 18)

$C_{stray} =$  the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on-frequency by making a portion or all of  $C_1$  variable. The crystal and associated components must be located as close as possible to the OSC<sub>in</sub> and OSC<sub>out</sub> pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for  $C_{in}$  and  $C_{out}$ . For this approach, the term  $C_{stray}$  becomes 0 in the above expression for  $C_L$ .

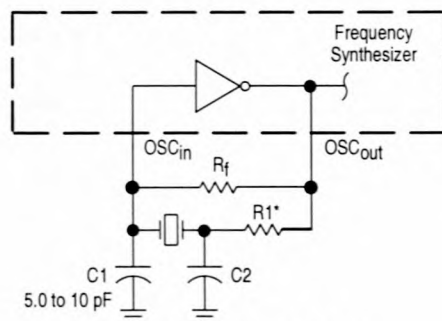
A good design practice is to pick a small value for  $C_1$ , such as 5 to 10 pF. Next,  $C_2$  is calculated.  $C_1 < C_2$  results in a more robust circuit for start-up and is more tolerant of crystal parameter variations.

Power is dissipated in the effective series resistance of the crystal,  $R_e$ , in Figure 20. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency.  $R_1$  in Figure 18 limits the drive level. The use of  $R_1$  is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency at the REF<sub>out</sub> pin (OSC<sub>out</sub> is not used because loading impacts the oscillator). The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or  $R_1$  must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of  $R_1$ .

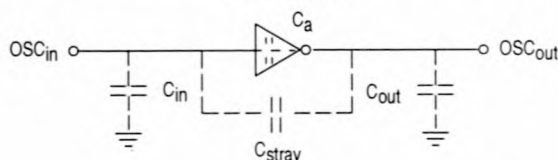
Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 2).

**Figure 18. Pierce Crystal Oscillator Circuit**

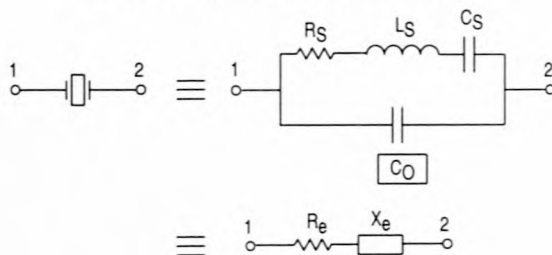


\* May be needed in certain cases. See text.

**Figure 19. Parasitic Capacitances of the Amplifier and  $C_{stray}$**



**Figure 20. Equivalent Crystal Networks**



**NOTE:** Values are supplied by crystal manufacturer (parallel resonant crystal).

## MC145170-2 RECOMMENDED READING

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit—Definitions and Method of Measurement", *Proc. IEEE*, Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology*, June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.

See web site [mot-sps.com](http://mot-sps.com) for MC145170-2 control software. Select in order, Products, Wireless Semiconductor, Download, then PLL Demo Software. Choose PLLGEN.EXE.

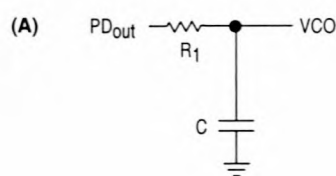
**Table 2. Partial List of Crystal Manufacturers**

CTS Corp.
United States Crystal Corp.
Crystek Crystal
Statek Corp.
Fox Electronics

**NOTE:** Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

## MC145170-2

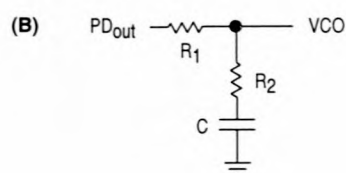
### PHASE-LOCKED LOOP — LOW PASS FILTER DESIGN



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1 C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

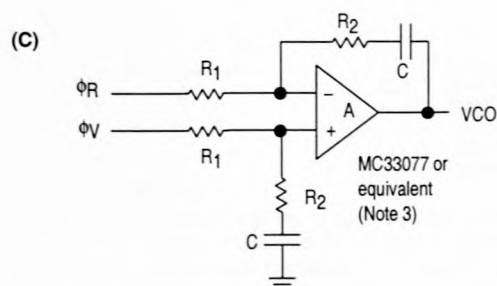
$$F(s) = \frac{1}{R_1 s C + 1}$$



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5 \omega_n \left( R_2 C + \frac{N}{K_\phi K_{VCO}} \right)$$

$$F(s) = \frac{R_2 s C + 1}{(R_1 + R_2) s C + 1}$$



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

Assuming Gain A Is Very Large, Then:

$$F(s) = \frac{R_2 s C + 1}{R_1 s C}$$

#### NOTES:

- For (C),  $R_1$  is frequently split into two series resistors; each resistor is equal to  $R_1$  divided by 2. A capacitor  $C_C$  is then placed from the midpoint to ground to further filter the error pulses. The value of  $C_C$  should be such that the corner frequency of this network does not significantly affect  $\omega_n$ .
- The  $\phi_R$  and  $\phi_V$  outputs swing rail-to-rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp.
- For the latest information on MC33077 or equivalent, see the Motorola Analog IC web site at <http://www.mot-sps.com/analog>.

#### DEFINITIONS:

$N$  = Total Division Ratio in Feedback Loop

$K_\phi$  (Phase Detector Gain) =  $V_{DD} / 4\pi$  volts per radian for  $PD_{out}$

$K_\phi$  (Phase Detector Gain) =  $V_{DD} / 2\pi$  volts per radian for  $\phi_V$  and  $\phi_R$

$$K_{VCO} \text{ (VCO Gain)} = \frac{2\pi \Delta f_{VCO}}{\Delta V_{VCO}}$$

For a nominal design starting point, the user might consider a damping factor  $\zeta \approx 0.7$  and a natural loop frequency  $\omega_n = (2\pi f_R / 50)$  where  $f_R$  is the frequency at the phase detector input. Larger  $\omega_n$  values result in faster loop lock times and, for similar sideband filtering, higher  $f_R$ -related VCO sidebands.

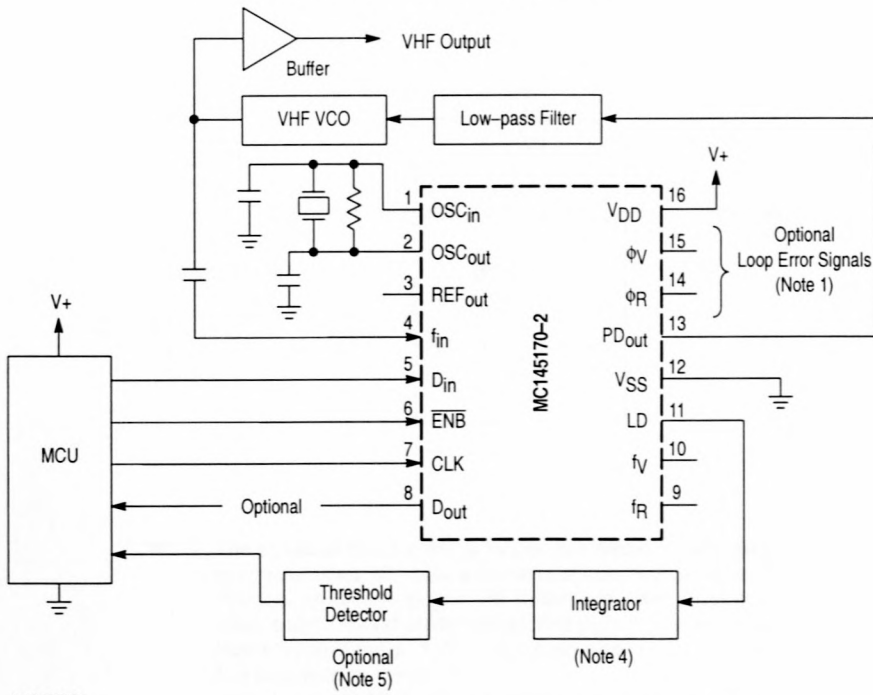
#### RECOMMENDED READING:

- Gardner, Floyd M., *Phaselock Techniques (second edition)*. New York, Wiley-Interscience, 1979.
- Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition)*. New York, Wiley-Interscience, 1980.
- Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design*. New York, Wiley-Interscience, 1976.
- Egan, William F., *Frequency Synthesis by Phase Lock*. New York, Wiley-Interscience, 1981.
- Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design*. Englewood Cliffs, NJ, Prentice-Hall, 1983.
- Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments*. Indianapolis, Howard W. Sams and Co., 1978.
- Kinley, Harold, *The PLL Synthesizer Cookbook*. Blue Ridge Summit, PA, Tab Books, 1980.
- Seidman, Arthur H., *Integrated Circuits Applications Handbook*, Chapter 17, pp. 538-586. New York, John Wiley & Sons.
- Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN*, March 5, 1980.
- AN535, Phase-Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
- AR254, Phase-Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design*, 1987.
- AN1207, The MC145170 in Basic HF and VHF Oscillators, Motorola Semiconductor Products, Inc., 1992.
- AN1671, MC145170 PSpice Modeling Kit, Motorola Semiconductor Products, Inc., 1998.



## MC145170-2

Figure 21. Example Application

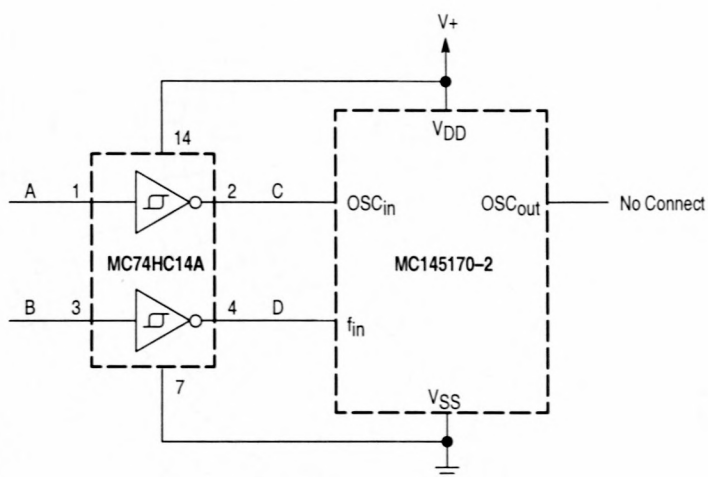


**NOTES:**

1. The  $\phi_R$  and  $\phi_V$  outputs are fed to an external combiner/loop filter. See the Phase-Locked Loop — Low-Pass Filter Design page for additional information. The  $\phi_R$  and  $\phi_V$  outputs swing rail-to-rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.
2. For optimum performance, bypass the  $V_{DD}$  pin to  $V_{SS}$  (GND) with one or more low-inductance capacitors.
3. The R counter is programmed for a divide value =  $OSC_{in}/f_R$ . Typically,  $f_R$  is the tuning resolution required for the VCO. Also, the VCO frequency divided by  $f_R = N$ , where N is the divide value of the N counter.
4. May be an R-C low-pass filter.
5. May be a bipolar transistor.

## MC145170-2

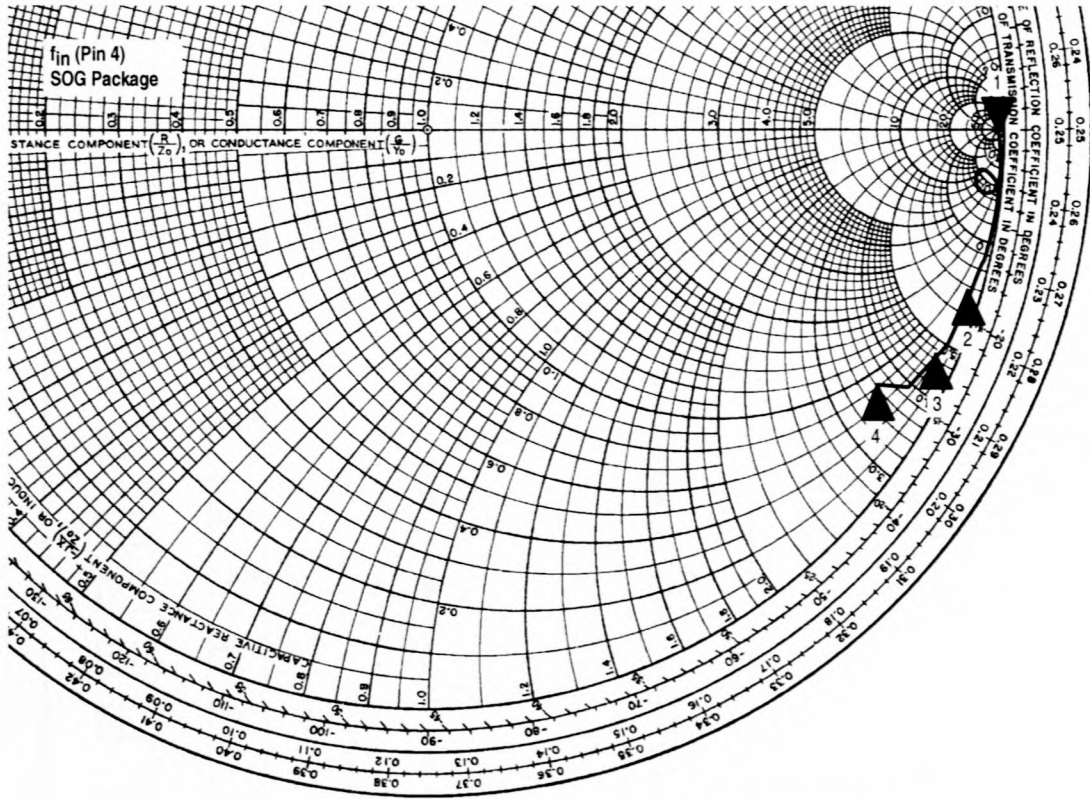
Figure 22. Low Frequency Operation Using dc Coupling



NOTE: The signals at Points A and B may be low-frequency sinusoidal or square waves with slow edge rates or noisy signal edges. At Points C and D, the signals are cleaned up, have sharp edge rates, and rail-to-rail signal swings. With signals as described at Points C and D, the MC145170-2 is guaranteed to operate down to a frequency as low as dc. Refer to the MC74HC14A data sheet for input switching levels and hysteresis voltage range.

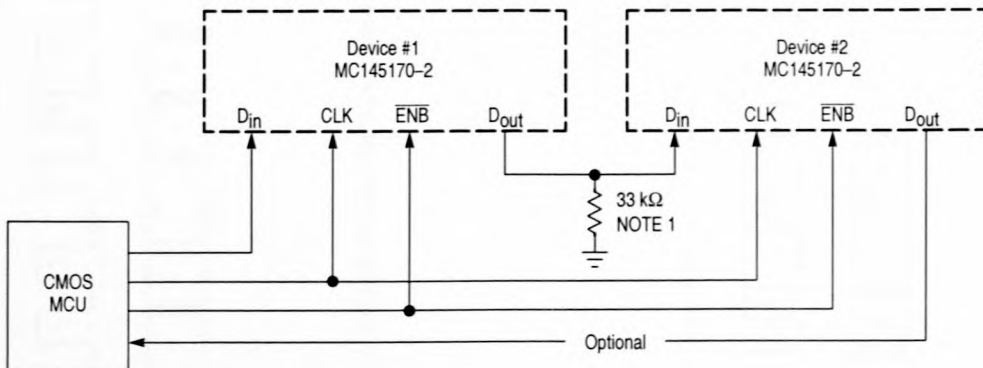
## MC145170-2

Figure 23. Input Impedance at  $f_{in}$  — Series Format ( $R + jX$ )  
(5.0 MHz to 185 MHz)



Marker	Frequency (MHz)	Resistance ( $\Omega$ )	Reactance ( $\Omega$ )	Capacitance (pF)
1	5	2390	-5900	5.39
2	100	39.2	-347	4.58
3	150	25.8	-237	4.48
4	185	42.6	-180	4.79

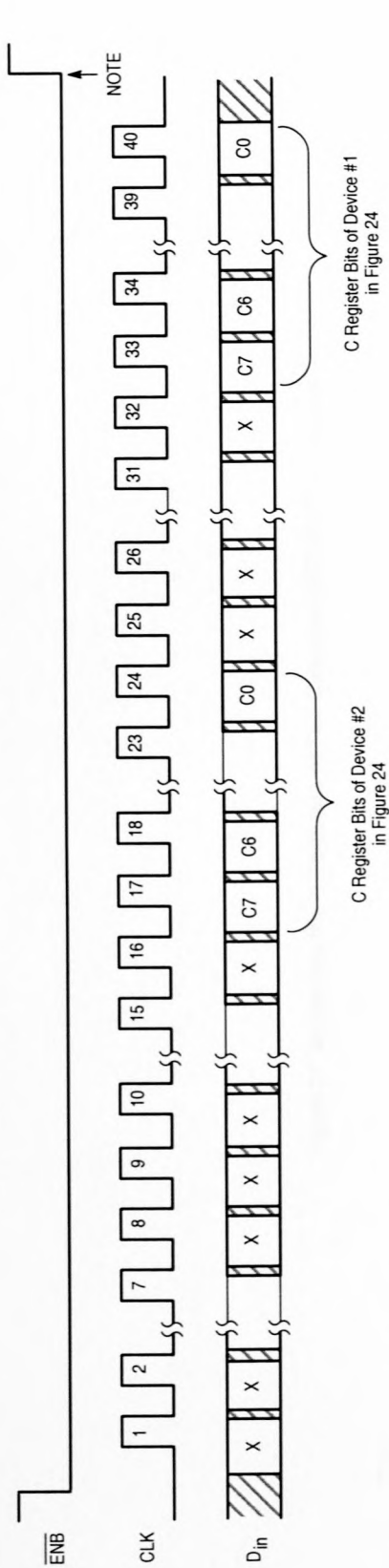
Figure 24. Cascading Two MC145170-2 Devices



NOTES:

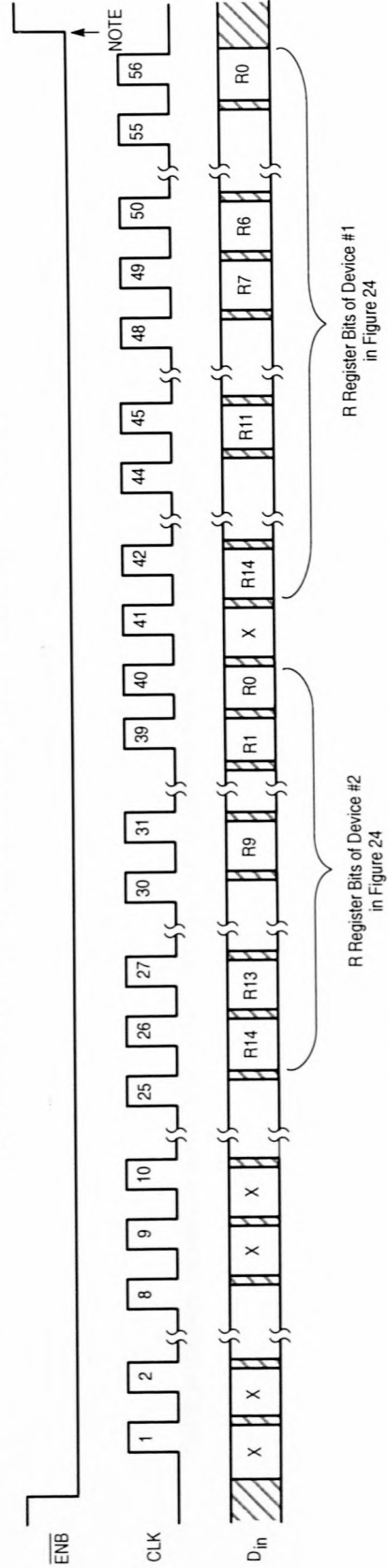
1. The 33 k $\Omega$  resistor is needed to prevent the D<sub>in</sub> pin from floating. (The D<sub>out</sub> pin is a three-state output.)
2. See related Figures 25, 26, and 27.

Figure 25. Accessing the C Registers of Two Cascaded MC145170-2 Devices



NOTE: At this point, the new data is transferred to the C registers of both devices and stored. No other registers are affected.

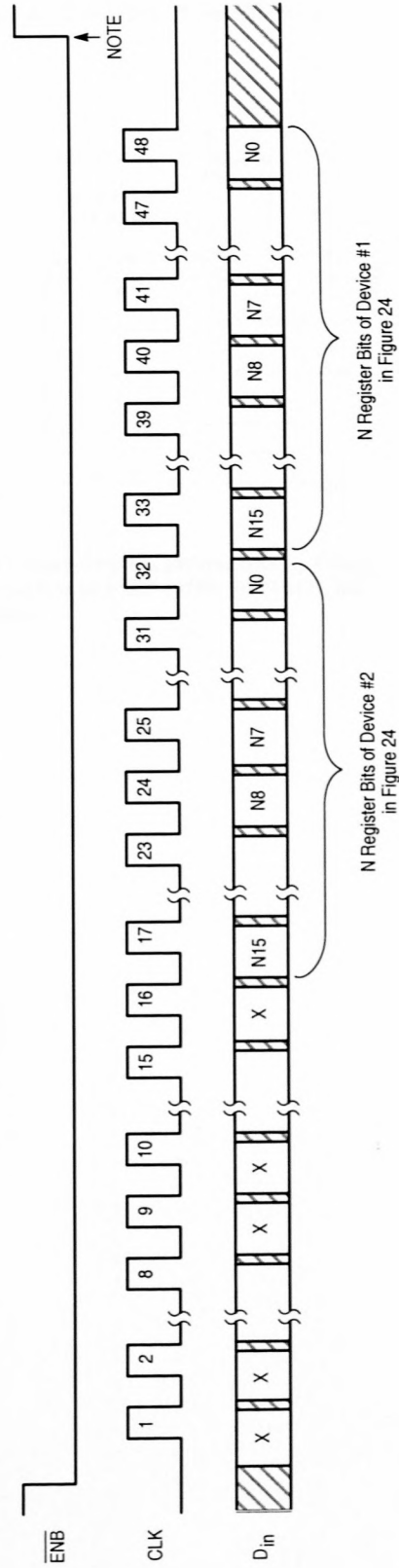
Figure 26. Accessing the R Registers of Two Cascaded MC145170-2 Devices



NOTE: At this point, the new data is transferred to the R registers of both devices and stored. No other registers are affected.



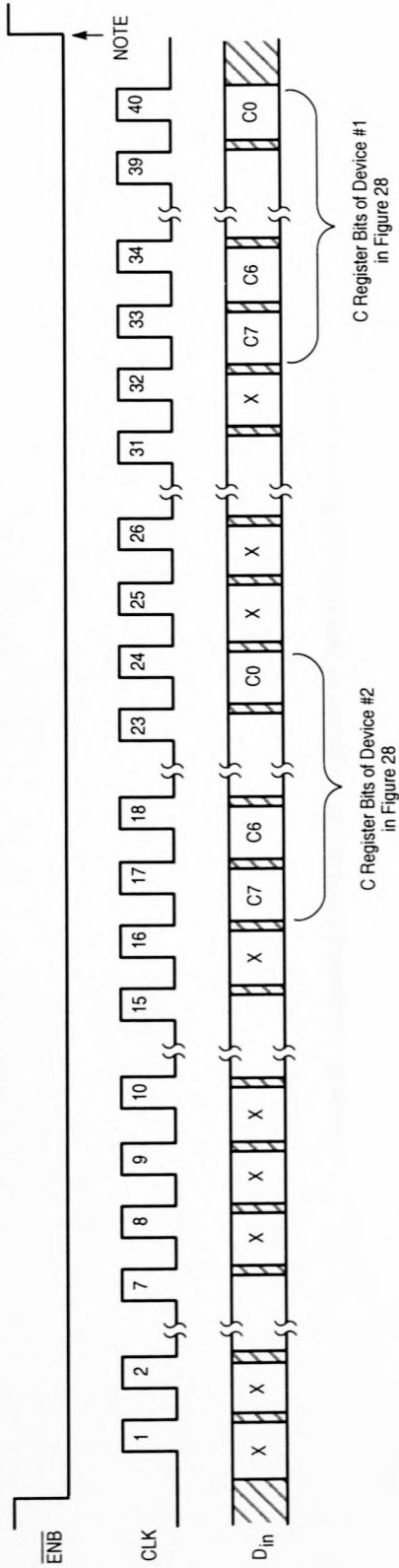
Figure 27. Accessing the N Registers of Two Cascaded MC145170-2 Devices



NOTE: At this point, the new data is transferred to the N registers of both devices and stored. No other registers are affected.

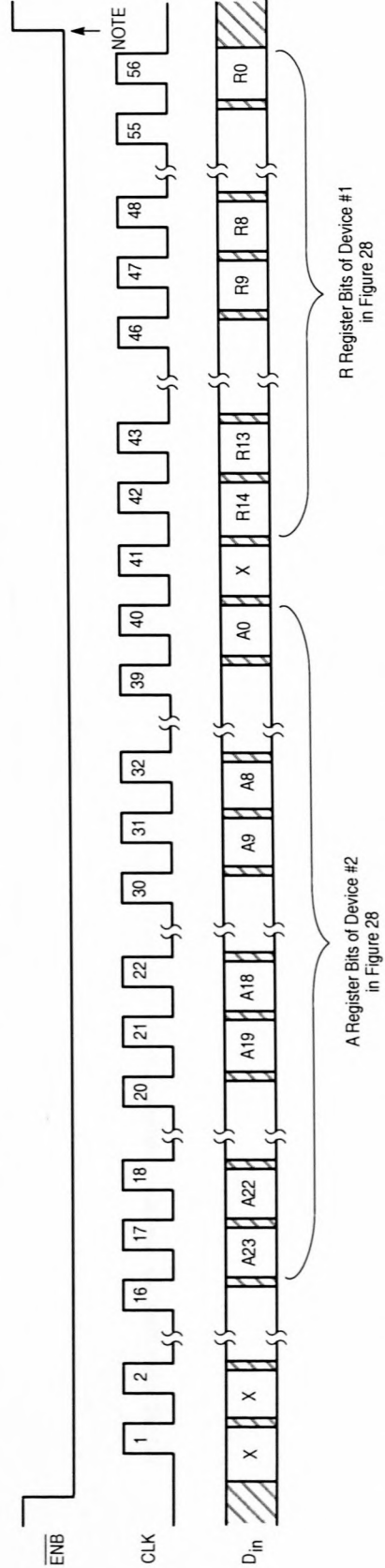


Figure 29. Accessing the C Registers of Two Different Device Types



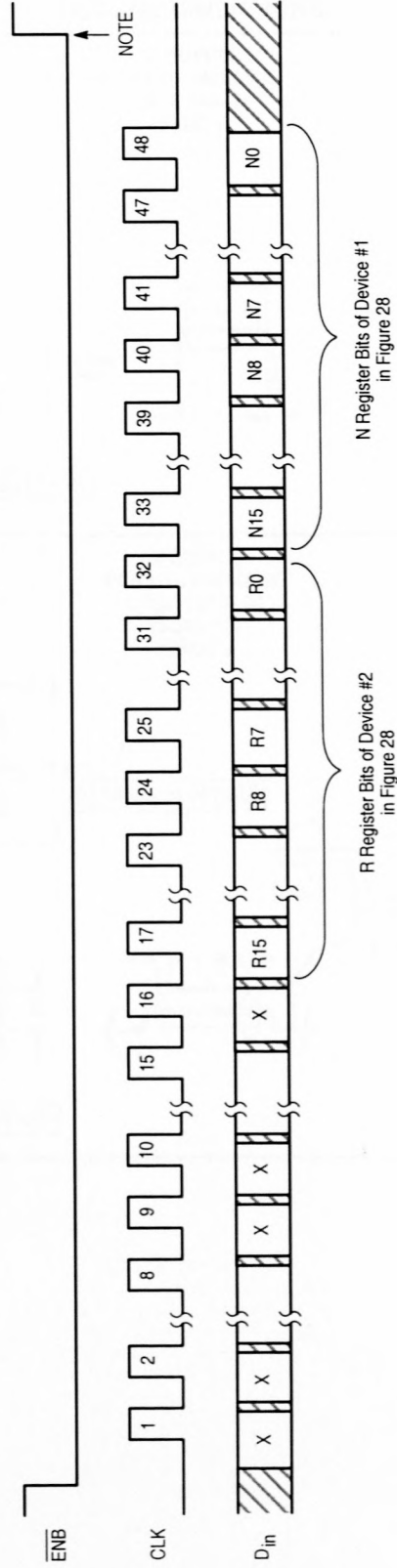
NOTE: At this point, the new data is transferred to the C registers of both devices and stored. No other registers are affected.

Figure 30. Accessing the A and R Registers of Two Different Device Types



NOTE: At this point, the new data is transferred to the A register of Device #2 and R register of Device #1 and stored. No other registers are affected.

Figure 31. Accessing the R and N Registers of Two Different Device Types



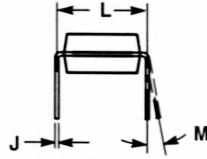
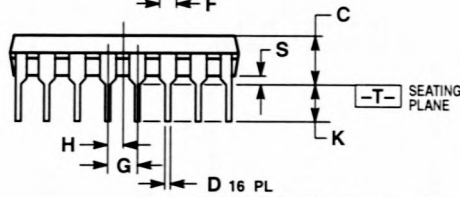
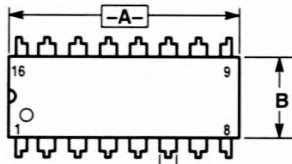
NOTE: At this point, the new data is transferred to the R register of Device #2 and N register of Device #1 and stored. No other registers are affected.



# MC145170-2

## OUTLINE DIMENSIONS

### P SUFFIX PLASTIC PACKAGE CASE 648-08 ISSUE R



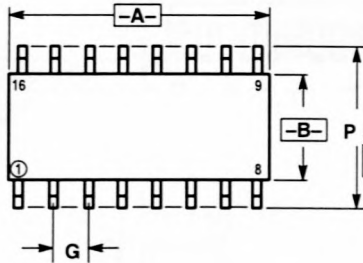
$\oplus 0.25 (0.010) \text{ (M) T A (M)}$

#### NOTES:

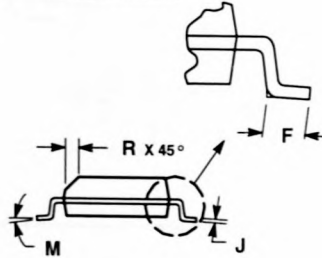
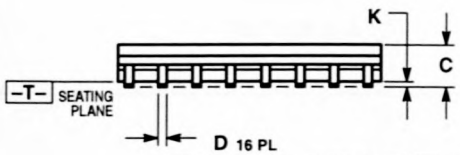
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

### D SUFFIX PLASTIC PACKAGE CASE 751B-05 (SOG-16) ISSUE J



$\oplus 0.25 (0.010) \text{ (M) B (S)}$



$\oplus 0.25 (0.010) \text{ (M) T B (S) A (S)}$

#### NOTES:

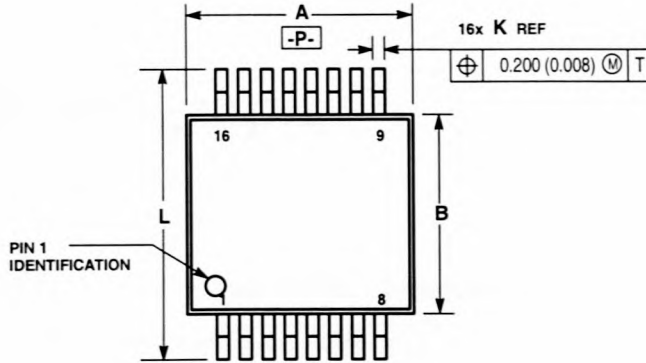
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

# MC145170-2

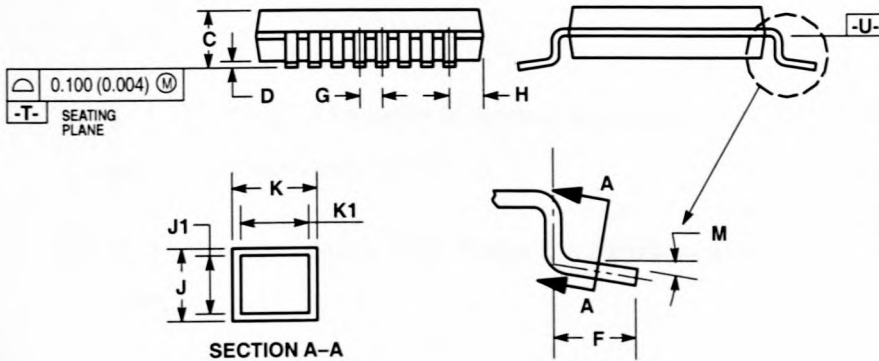
## OUTLINE DIMENSIONS

DT SUFFIX  
PLASTIC PACKAGE  
CASE 948C-03  
(TSSOP-16)  
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -U-.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	5.10	—	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.25	0.002	0.010
F	0.45	0.55	0.018	0.022
G	0.65 BSC 0.026 BSC			
H	0.22	0.23	0.009	0.010
J	0.09	0.24	0.004	0.009
J1	0.09	0.18	0.004	0.007
K	0.16	0.32	0.006	0.013
K1	0.16	0.26	0.006	0.010
L	6.30	6.50	0.248	0.256
M	0°	10°	0°	10°

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