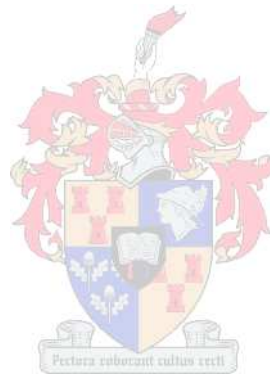


GaN Microwave Power FET Nonlinear Modelling Techniques

by

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requirements for the degree of Master of Science in
Engineering at Stellenbosch University*

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Declaration

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Abstract

The main focus of this thesis is to document the formulation, extraction and validation of nonlinear models for the on-wafer gallium nitride (GaN) high-electron mobility (HEMT) devices manufactured at the Interuniversity Microelectronics Centre (IMEC) in Leuven, Belgium. GaN semiconductor technology is fast emerging and it is expected that these devices will play an important role in RF and microwave power amplifier applications. One of the main advantages of the new GaN semiconductor technology is that it combines a very wide band-gap with high electron mobility, which amounts to higher levels of gain at very high frequencies. HEMT devices based on GaN, is a fairly new technology and not many nonlinear models have been proposed in literature. This thesis details the design of hardware and software used in the development of the nonlinear models. An intermodulation distortion (IMD) measurement setup was developed to measure the second and higher-order derivative of the nonlinear drain current. The derivatives are extracted directly from measurements and are required to improve the nonlinear model IMD predictions. Nonlinear model extraction software was developed to automate the modelling process, which was fundamental in the nonlinear model investigation. The models are implemented in Agilent's Advanced Design System (ADS) and it is shown that the models are capable of accurately predicting the measured S-parameters, large-signal single-tone and two-tone behaviour of the GaN devices.

Opsomming

Die hoofdoel van hierdie tesis is om die formulering, onttrekking en validasie van nie-lineêre modelle vir onverpakte gallium nitraat (GaN) hoë-elektronmobilisering transistors (HEMTs) te dokumenteer. Die transistors is vervaardig by die *Interuniversity Microelectronics Centre* (IMEC) in Leuven, België. GaN-halfgeleier tegnologie is besig om vinnig veld te wen en daar word voorspel dat hierdie transistors 'n belangrike rol gaan speel in RF en mikrogolf krag-versterker toepassings. Een van die hoof voordele van die nuwe GaN-halfgeleier tegnologie is dat dit 'n baie wyd band-gaping het met hoë-elektronmobilisering, wat lei tot hoë aanwinst by mikrogolf frekwensies. GaN HEMTs is 'n redelik nuwe tegnologie en nie baie nie-lineêre modelle is al voorgestel in literatuur nie. Hierdie tesis ondersoek die ontwerp van die hardeware en sagteware soos gebruik in die ontwikkeling van nie-lineêre modelle. 'n Intermodulasie distorsie-opstelling (IMD-opstelling) is ontwikkel vir die meting van die tweede en hoër orde afgeleides van die nie-lineêre stroom. Die afgeleides is direk uit die metings onttrek en moet die nie-lineêre IMD-voorspellings te verbeter. Nie-lineêre onttrekking sagteware is ontwikkel om die modellerings proses te outomatiseer. Die modelle word geïmplementeer in *Agilent se Advanced Design System* (ADS) en bewys dat die modelle in staat is om akkurate afgemete S-parameters, grootsein enkeltoon en tweetoon gedrag van die GaN-transistors te kan voorspel.

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CHAPTER 1

Introduction

1.1 Introduction

The main objective of this thesis is to investigate, characterise and model a new advanced microwave transistor. The technology referred to is gallium nitride (GaN) high-electron mobility transistors (HEMTs). The HEMTs measured and modelled are manufactured at the Interuniversity Microelectronics Centre (IMEC) in Leuven, Belgium. GaN semiconductor technology offers higher levels of gain at very high frequencies compared to similar devices in the market today. As this technology is relatively new, not many models have been proposed in literature and the goal of this work is to develop nonlinear models that accurately predict the linear and nonlinear behaviour of the GaN HEMTs measured.

The goal of this chapter is to give a brief introduction to the basic principles of nonlinear modelling. These principles are fundamental to fully understand how nonlinear models are derived in practice. The final section of this chapter will present the scope and layout of this thesis.

1.2 Overview of Nonlinear Modelling Techniques

Physically-based modelling, black box modelling and equivalent circuit modelling are the three main modelling approaches to describe the nonlinear behaviour of a device [12]. Each of these techniques will be discussed briefly in this section.

Physically-based modelling describes the active device in terms of the motion of charge carriers and geometrical characteristics, allowing both a physical and an electrical description of the device. The advantage of this approach is that it provides valuable insight into the operation of the semiconductor device. The disadvantage, however, is that this type of model is rather

complex and requires time-consuming numerical methods to obtain solutions, thus it will not be considered in this work.

The next modelling technique is known as “Black Box Modelling”. In this approach, the device is represented by a behavioural input-output model. It arises from system theory, where basic building blocks of any complexity are represented by a transfer function. The parameters of the mathematical model are fitted to a set of measured results. The newest work in this field provides very powerful models by extracting nonlinear state space equations directly from measured data. This technique requires a large amount of nonlinear vector measurements taken with the large-signal vector network analyser (LSNA). However, the accessibility of a LSNA measurement system is in most cases problematic and is a major disadvantage of this technique. The method also requires extensive fitting procedures that can be very time consuming. A trade-off between model accuracy and model simplicity has to be made, which does not make this approach suitable for this work.

The most widely used type of device model in practice is the equivalent circuit model. This model offers several key advantages over the physically-based and “Black Box” models. The first is that the small-signal equivalent model provides a link between the measured DC and S-parameters and the electronic processes occurring within the device. The elements in the equivalent circuit provide a lumped element approximation to some aspect of the physical device. A properly chosen topology, in addition to being physically meaningful, provides an excellent match to measurements over a very wide frequency range and allows for extrapolation of behaviour at frequencies beyond the capability of the available measurement setup. The main advantage of this method is that it is relatively fast and straightforward, which makes it ideal to implement in nonlinear simulation packages. The equivalent circuit parameters (ECPs) are extracted using measurements taken from the vector network analyser (VNA). Once the ECPs have been extracted, the equivalent quasi-static nonlinear model can be derived. The model can be extended to a non quasi-static model to improve the accuracy of the model predictions.

All factors considered, it is concluded that the equivalent circuit model approach will be used to model the devices in this work. In chapter four, a detailed description of the equivalent circuit model topology is presented, as well as the deduction of the nonlinear models.

1.3 Introduction to Nonlinear Equivalent Circuit Models

The main objective of an equivalent circuit is to model all the electrical characteristics of the original circuit on which it is based. When dealing with complex circuits such as transistor models, the equivalent circuit is made up of linear and nonlinear elements and must be able to

accurately predict both the linear and nonlinear behaviour of the device. In practice, the nonlinear equivalent circuit model is the most widely used nonlinear model and is fairly simple to implement in commercial computer aided design (CAD) programs.

The most common method to construct these models is from measured multi-bias DC and high-frequency S-parameter data. Pulsed I-V measurements can also be used, but these measurement setups are not always accessible and will not be used in this work. The measured S-parameter data from the VNA is used to extract the linear equivalent circuit model. This model represents the small-signal response of the device. A typical small-signal model of a field effect transistor (FET) model consists of an intrinsic and an extrinsic section as shown in Figure 1.1. All the elements outside the dashed box represent the extrinsic elements. These elements are related to the packaging of the device and are bias-independent. The elements inside the box represent the intrinsic elements and are bias-dependent.

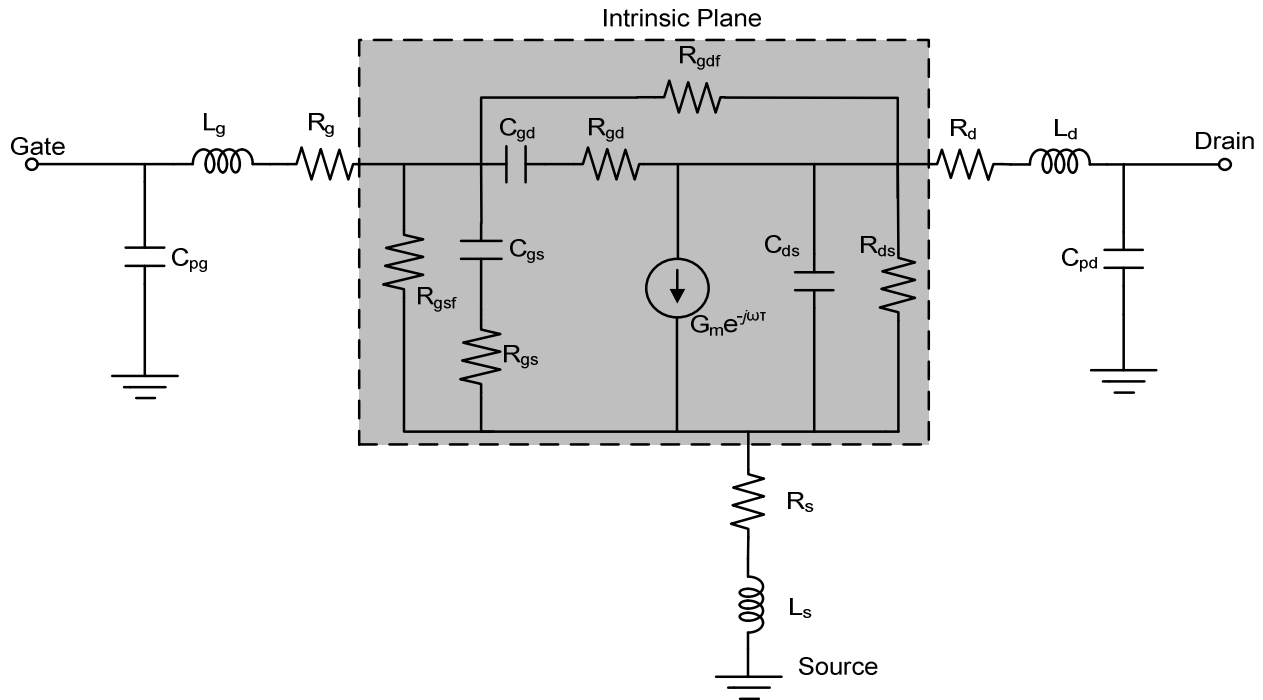


Figure 1.1 The typical small-signal equivalent circuit for an FET.

Once the equivalent circuit parameters have been extracted the next step is to construct the nonlinear current and charge functions seen in Figure 1.2. The nonlinear model is consistent with the small-signal equivalent scheme, provided that the corresponding non-linear characteristics at both ports are obtained by the path independent contour integrals. The nonlinear models transform the large amount of extracted small-signal parameters into a single set of parameters. The result is a nonlinear circuit model representation of the device that should be able to predict

the linear and nonlinear behaviour of the device. The model seen in Figure 1.2 is known as the nonlinear state-space representation and will be discussed in more detail in chapter four.

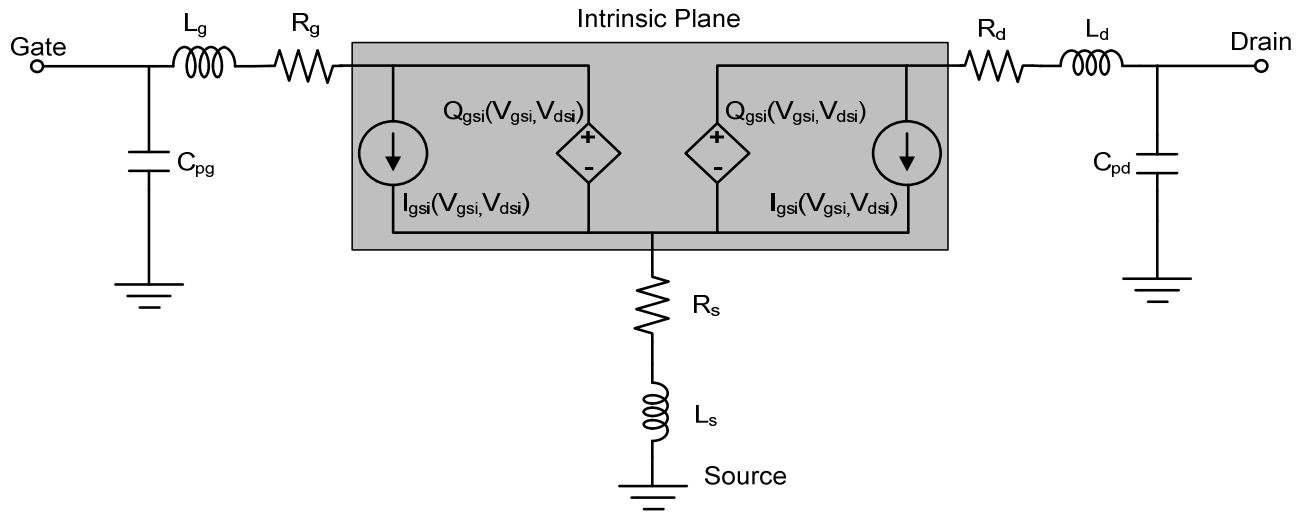


Figure 1.2 The transformed state-space nonlinear model representation.

1.4 Scope and Layout of this Study

The main goal of this thesis is to develop equivalent circuit nonlinear models for an emergent active device technology, GaN HEMTs. The models should be capable of accurately predicting the linear and nonlinear behaviour of the devices. The linear characteristics include the small-signal S-parameters predictions, while the nonlinear characteristics include the harmonic and intermodulation distortion predictions. A key focus of the nonlinear models is to ensure that the model can still predict the linear small-signal S-parameters. GaN is expected to play an important role in future power amplifier applications of microwave and wireless digital telecommunications systems. GaN technology is relatively new and not many models have been presented in literature. The aim of this thesis is to develop a model that can accurately predict the linear and nonlinear behaviour of the measured devices. The following paragraphs give a brief overview of the content of this thesis.

In chapter two, an overview of GaN HEMT technology is presented, as well as the procedure followed in the device characterisation process. This chapter also discusses the various measurement instruments that were used in the characterisation and validation process of the on-wafer devices. Chapter three presents a low-frequency intermodulation distortion measurement setup used to measure the second and higher order intermodulation performance of the nonlinear drain current source, I_{ds} . The current source I_{ds} represents one of the main nonlinearities in an

equivalent circuit nonlinear model and should thus be modelled as accurately as possible. The main objective of the measurement setup is to extract a Taylor series, describing the higher order derivatives of I_{ds} directly from measurements. The Taylor series coefficients are essential for the construction of models that can accurately predict nonlinear intermodulation distortion (IMD) behaviour.

The goal of chapter four is to present a formulation and investigate the nonlinear models proposed for the GaN HEMTs. The starting point of the process is to determine the small-signal equivalent circuit model topology, followed by the detailed ECP extraction procedure. Once the ECPs are determined, the corresponding nonlinear model is constructed. The complete nonlinear model construction is discussed with a description of the nonlinear modelling procedure and formulation. The current derivative data extracted in chapter three is incorporated in the final nonlinear model. The addition of the derivative information leads to a nonlinear model that improves the S-parameter, large-signal single-tone and large-signal two-tone IMD predictions.

In chapter five, the proposed nonlinear models are verified by comparing the CAD model predictions to measurements from the VNA and LSNA. This chapter gives an overview of the error functions used to represent the difference between the measured and modelled parameters. The software tools used to implement the nonlinear models in Agilent's Advanced Design System (ADS) is described in this chapter. Finally, the nonlinear model predictions are compared to the measured S-parameters, large-signal single-tone and large-signal two-tone results. Chapter six provides an overview of the results and provides recommendations for future research.

CHAPTER 2

Device Characterisation and Measurement Setups

2.1 Introduction

It is very important to fully understand the device technology that is to be modelled and the measurement instruments needed in the modelling process. This chapter is dedicated to provide insight into the on-wafer gallium nitride (GaN) high-electron mobility transistors (HEMT) devices modelled, as well as the measurement setups used to characterise and verify the devices. It is vital to understand the operation and data obtained from each instrument. The measurement equipment is not only used to extract the equivalent circuit models, but also to verify the accuracy of the models. Once the parameters have been extracted, the models are implemented in a simulation package and the measured results are compared with the model predictions.

In section 2.2, an overview of the GaN HEMT technology is presented, with the explanation of the basic operation of a HEMT to provide insight into the modelling process. Before a device is measured, a selection process must be followed to ensure that the optimal devices are measured, which is discussed in section 2.3. Section 2.4 provides an overview of the various linear and nonlinear measurement instruments necessary in the nonlinear modelling process. In section 2.4.1, the vector network analyser (VNA) is discussed, from which the values of the equivalent circuit parameters (ECPs) are extracted. Section 2.4.2 discusses the large-signal network analyser (LSNA), which is used as an independent measurement to perform the nonlinear large-signal validations.

2.2 GaN HEMT Technology

Over the last few years, many different technologies have been investigated in the field of power amplifiers. The latest breakthrough has come in the development of wide band-gap materials, for example, GaN. Devices based on wide band-gap materials are capable of handling higher power densities in a more efficient way than devices fabricated from other semiconductor materials. It is a result of the combination of high energy band-gap, high critical electric field, low dielectric

constant and high thermal conductivity. The main property advantages of GaN over competing semiconductor materials are demonstrated in Table 2.1 [5]. There is a wide range of applications for GaN devices, ranging from commercial applications to the medical field. GaN has been grown on many different substrates, including sapphire, Si and SiC. The most widely reported substrate is sapphire, as it has the advantage of being relatively cheap and is offered in large diameter wafers. Most importantly, it provides an excellent low-loss microwave substrate. The disadvantage of sapphire is that the thermal conductivity is very poor and will severely limit the power density and total power performance of devices fabricated on it. The devices measured in this work are based on a SiC substrate, which has promising characteristics in terms of lattice matching and thermal conductivity, and it is also an excellent microwave substrate. The disadvantages of devices on SiC are the costs related to the growth process, limited wafer size and material defects. The material defects play a critical role in the device characterisation and will be discussed in section 2.3.

Property	Si	GaAs	GaN
Suitable for high power applications	Medium	Low	High
Suitable for high frequencies	Low	High	High
HEMT structures	No	Yes	Yes
Low cost substrates	Yes	No	Yes

Table 2.1 The key advantages of GaN over competing semiconductor technologies.

A key advantage of the HEMT devices is that it overcomes the performance limits of the conventional metal semiconductor field effect transistor (MESFET), as it exhibits more gain, a higher operating frequency and a lower noise figure. Figure 2.1 shows the basic structure of an HEMT device. It consists of a hetero-junction, composed of a narrow band-gap (GaN) material and a wide band-gap (AlGaN) material. The wide band-gap semiconductor is doped, resulting in states of lower energy [13], which leads to the electrons diffusing from the wide to the narrow band-gap semiconductor. These electrons form a thin layer which is known as a two-dimensional electron gas (2DEG). Within this region, the electrons are able to move freely because there are no other donor atoms or other items with which electrons will collide, making the mobility of the electrons in the gas very high. The output current flowing between source and drain is controlled by the modulation of the carrier density in the channel through the gate. When the gate voltage is equal to zero, a 2DEG is accumulated at the hetero-interface and the channel is open. When a positive gate voltage is applied, the output current increases. This is a result of the increase in 2DEG density and consequently the current density in the channel. However, when the gate voltage is lower than the pinch-off voltage (typically a negative voltage), the drain current approaches zero regardless of the drain bias, since the 2DEG in the channel is depleted [13].

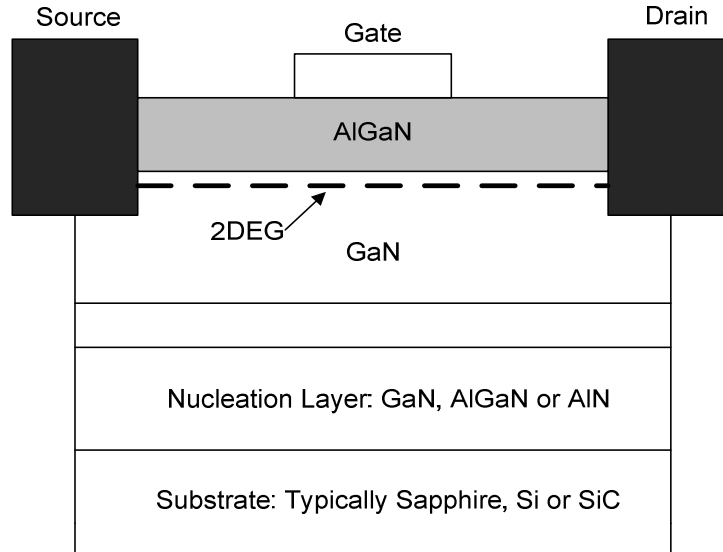


Figure 2.1 The basic structure of an HEMT device.

2.3 Device Characterisation

In this section, the selection method for the characterisation of on-wafer GaN HEMT devices is detailed. As mentioned in the previous section the devices measured were fabricated on a SiC substrate, which in practice has led to difficulties regarding the growth process, wafer size and material defects. The result is that the device characteristics can differ depending on the position on the wafer. A number of different device topologies are fabricated on each wafer. The subscript in the name indicates the number of fingers and gate widths of the device. Table 2.2 gives a summary of the devices measured at IMEC. It is important to select the appropriate device on the wafer, in order to accurately characterise the desired topology.

Two-Finger Devices	Four-Finger Devices
T ₀₂ Devices (2×50µm)	T ₁₀ Devices (4×100µm)
T ₀₃ Devices (2×100µm)	T ₁₂ Devices (4×150µm)
T ₀₆ Devices (2×150µm)	
T ₀₇ Devices (2×200µm)	

Table 2.2 The different GaN HEMT topologies measured at IMEC.

The first step in the characterisation process is to measure the drain current curves of a least five devices of the same topology. This measurement is done with a constant gate voltage and the drain voltage swept over the desired range. From these I_{DS} curves, a mean current plot is

constructed, as seen in Figure 2.2. In this figure, the T02 devices are selected to demonstrate this approach. It can be seen that the curves have a relatively wide spread. With such a spread, it becomes vital to determine the optimal device to measure. The devices with the I_{DS} curve nearest to the mean plot are selected to characterise. Selecting the devices this way ensures that an average device is selected, which resembles the best average performance of that device topology. Once the appropriate device is selected, the characterisation process can begin, which is an automated Matlab procedure used at IMEC. The automated program measures the S-parameters over a user-defined bias range and step size. Care must be taken when entering the bias range, as the device can be damaged during the process if it is put under too much strain. The gate bias range is swept from -8V to 0V in steps of 0.2V, and drain biasing from 0V to 10V in steps of 0.5V. This leads to 861 bias points in total and is enough to fully characterise the devices, with the measurement time only taking a few hours. The S-parameters are measured from 45MHz to 40GHz with 201 frequency points. Any more points could lead to extra unwanted strain on the device which can cause damage, preventing the device from being used for the modelling process. The following section will describe the different measurement setups used to characterise the nonlinear behaviour of the on-wafer GaN HEMT devices in this work.

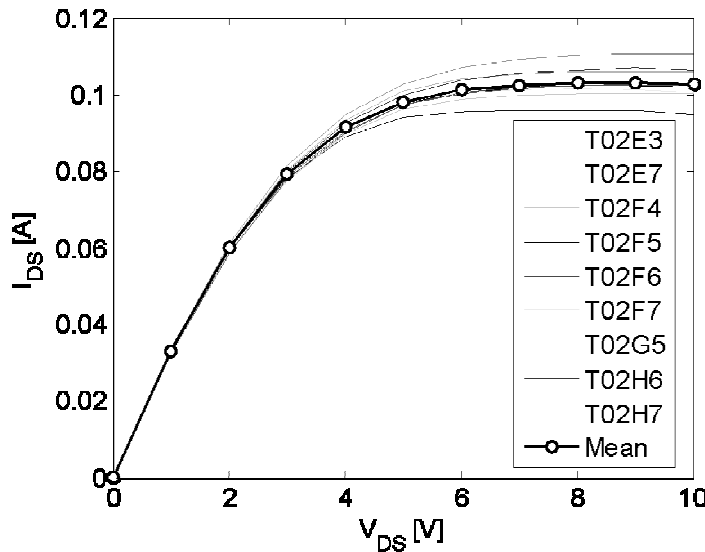


Figure 2.2 The different DC drain current curves for devices of the same topology.

2.4 Linear and Nonlinear Measurement Setups

In this section, a brief description of the measurement setups used to characterise and verify the on-wafer GaN HEMT devices is given. It is very important to understand the instruments to ensure accurate and reliable measurements. The nonlinear models that will be simulated in a

nonlinear simulation package are derived from measurements and thus it is vital that the experimental data is as accurate as possible. The first measurement setup of importance is the HP8510C VNA, which was used at IMEC to measure the S-parameters of the devices. The small-signal equivalent circuit parameters are extracted from the S-parameters. The second system is the LSNA, which was used at the Department of Electrical Engineering (ESAT) at the Catholic University Leuven, Belgium, for large-signal single-tone and two-tone verification measurements.

2.4.1 Vector Network Analyser

Nonlinear models are derived from linear equivalent circuit models which are extracted from linear S-parameters and DC measurements. These linear measurements are performed using a VNA which measures both the magnitude and phase of all the complex S-parameters of a device. The VNA measures the ratio of the scattered and incident travelling voltage waves at the fundamental frequency, as demonstrated in Figure 2.3, which implies that the VNA is a linear measurement system. However, before the S-parameter can be measured a calibration process must be followed [13], [17]. The calibration ensures that the plane of the measurement is shifted to the ports of the device under test (DUT).

By measuring known precision standards, the systematic errors can be removed mathematically from the experimental setup. These systematic errors are a result of imperfections of the VNA and the test setup. If it is assumed that the errors are time invariant, then it is possible to characterise the error with a calibration process and remove the effect from the measured data [17]. The main calibration techniques which have been developed for connector and on-wafer technologies are short-open-load-through (SOLT), thru-reflect-load (TRL), load-reflect-match (LRM) and the line-reflect-reflect-match (LRRM). The SOLT and LRM are mostly used, where the SOLT calibration has been successfully used for RF characterisation up to a few GHz. However, the accuracy of the calibration decreases for frequencies higher than 20GHz, which is not sufficient for the frequency ranges required in this work. The reason is that it is very difficult to produce a high quality purely resistive load and it is difficult to have an accurate definition of the planar open circuit and the planar short circuit at such high frequencies, as the short circuit is inductive and an open circuit radiates energy [12]. Thus, the calibration technique used in this work is the LRM. This technique requires a single reflective impedance of which the model's preciseness is less stringent than for the SOLT technique and the calibration is valid up to 50GHz [13]. The advantage of using the LRM technique is that only three impedance standards are necessary. The standards are a 50Ω load at each port, a short or open at both ports and a line standard between the two ports.

Figure 2.4 shows the HP8510C VNA used to measure the on-wafer GaN HEMT devices at IMEC. A close-up of the probe station is shown in Figure 2.5, where the probes are placed at the gate and drain terminal of the device. A microscope is used to place the probes at exact locations at ports of the device. This displays the enlarged image on a monitor as shown in Figure 2.6. Using this measurement setup, the complete small-signal RF characterisation of the devices was performed.

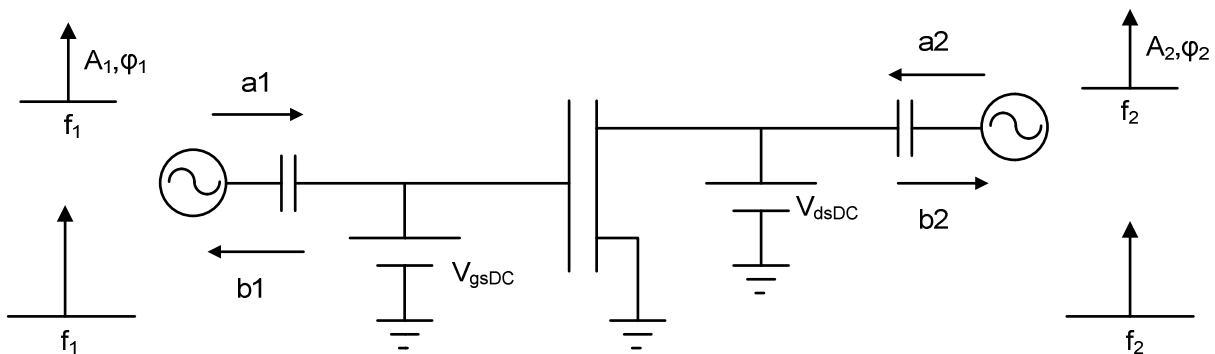


Figure 2.3 The VNA measures both the magnitude and phase of all the complex S-parameters at the fundamental frequency of a device under test.



Figure 2.4 The HP8510C VNA was used to measure the linear S-parameters of the on-wafer GaN HEMT devices at IMEC.

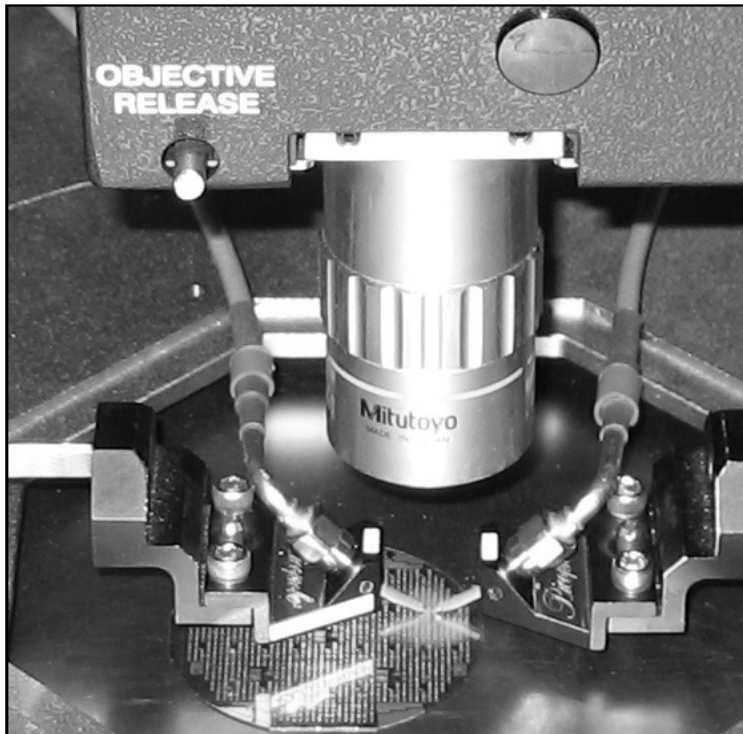


Figure 2.5 The measurement probes are placed at the gate and drain terminal of the device. A microscope is used to display the image on a monitor in order to help with the placement of the probes.

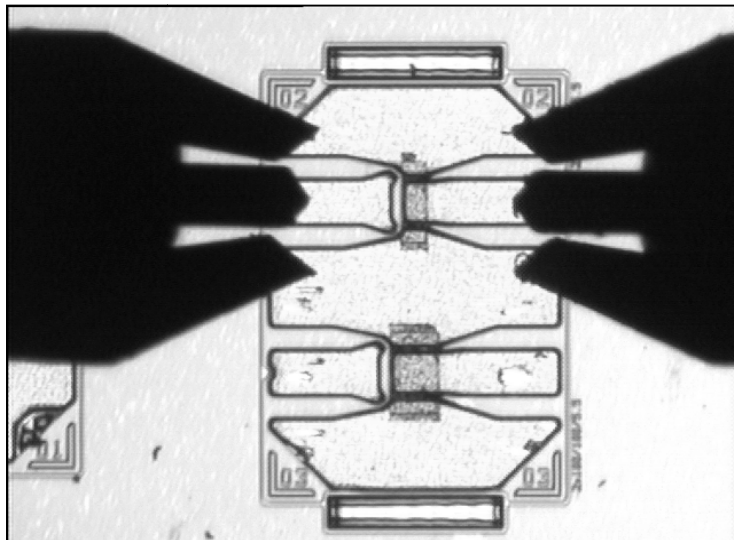


Figure 2.6 The image of the magnified T₀₂ device topology is displayed on the monitor, which is used to accurately place the probes at the precise locations at the gate and drain terminals.

2.4.2 Large-Signal Network Analyser

In order to verify nonlinear models and to use nonlinear measurements in the model generation process, amplitude and phase information of all the spectral components are necessary. The LSNA measures both the magnitude and phase of all harmonics of the incident and scattered travelling voltage waves at the device ports. The LSNA has two sources that can simultaneously excite both ports of the device as shown in Figure 2.7. Signals a_1 , a_2 represent the incident travelling power waves at port one and b_1 , b_2 the reflected travelling power waves at port two of the device. The LSNA sweeps the excitation power levels, but the excitation frequencies a_1 and a_2 are constant. The system also measures harmonics and intermodulation distortion (IMD) products of b_1 and b_2 waves at port one and port two respectively. Once the travelling power waves have been measured, the current and voltage wave forms can be calculated using Fourier theory. The LSNA seen in Figure 2.8 was used to measure the on-wafer GaN devices in this work and is located at the ESAT, K.U. Leuven, Belgium. It was used under the supervision of Prof. Dominique Schreurs. The LSNA setup has an RF bandwidth of 600MHz to 20GHz and the nonlinear measurements consist of single-tone and two-tone measurements over various bias conditions. The calibration process for the LSNA consists of three steps. The first is a linear calibration, which is followed by an absolute power calibration and finally a phase calibration [48].

The LSNA is a nonlinear measurement instrument and thus it is possible to generate a two-tone excitation signal, which can be used to perform intermodulation distortion measurements. In earlier measurements, it was observed that memory effects appear in the lower MHz frequency range when using the LSNA. The effect can be attributed to the Agilent biasing network, which is modelled as a simple series capacitor, a parallel inductor and a series resistor. Table 2.3 summarises the model values according to datasheets for the inductor L, capacitor C and the resistance R.

	Agilent 11612B	Pulse Labs Picosecond 5580
C	800pF	0.22 μ F
L	2 μ H	1.1mH
R	1.5 Ω	0.8 Ω

Table 2.3 Comparison between model parameters for the Agilent 11612B and Pulse Labs Picosecond 5580 bias tees.

The problem originates from the time constant relating to the model values. The effect can be overcome by using the Pulse Labs Picosecond 5580 bias-tees described in chapter three. The setup is demonstrated in Figure 2.9, where the Agilent bias-tees are bypassed with the Picosecond 5580 bias-tees. The equivalent inductor, capacitor and resistor values for the

Picosecond 5580 bias-tees are also shown in Table 2.3. S_{21} for the Agilent bias tee becomes 1 only around 45MHz, while S_{21} of the Picosecond Pulse Labs bias-tees becomes 1 around 10KHz. The tone-spacing used in this work is 200KHz and by evaluating the S_{21} values of both the Agilent and Picosecond bias-tees, it is concluded that the Agilent bias-tees would be unacceptable for the two-tone experiments.

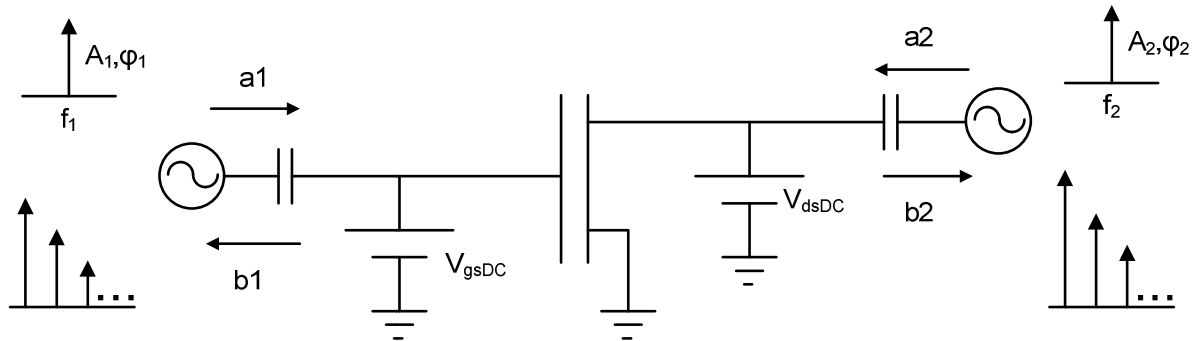


Figure 2.7 The LSNA measures both the magnitude and phase of all the complex S-parameters at all the harmonics of a device under test.

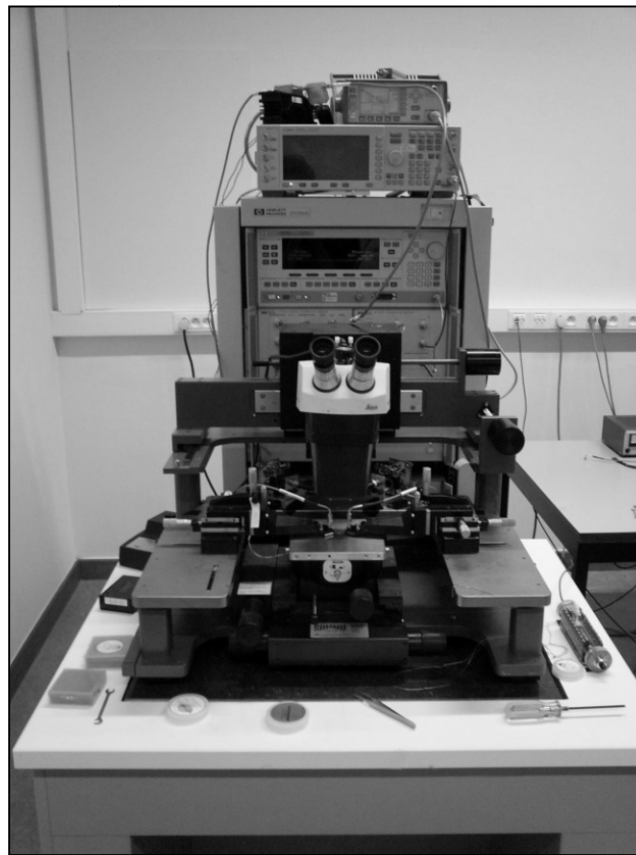


Figure 2.8 A photograph of the LSNA setup used at the ESAT-TELEMIC lab. The system has an RF bandwidth of 600MHz to 20GHz.

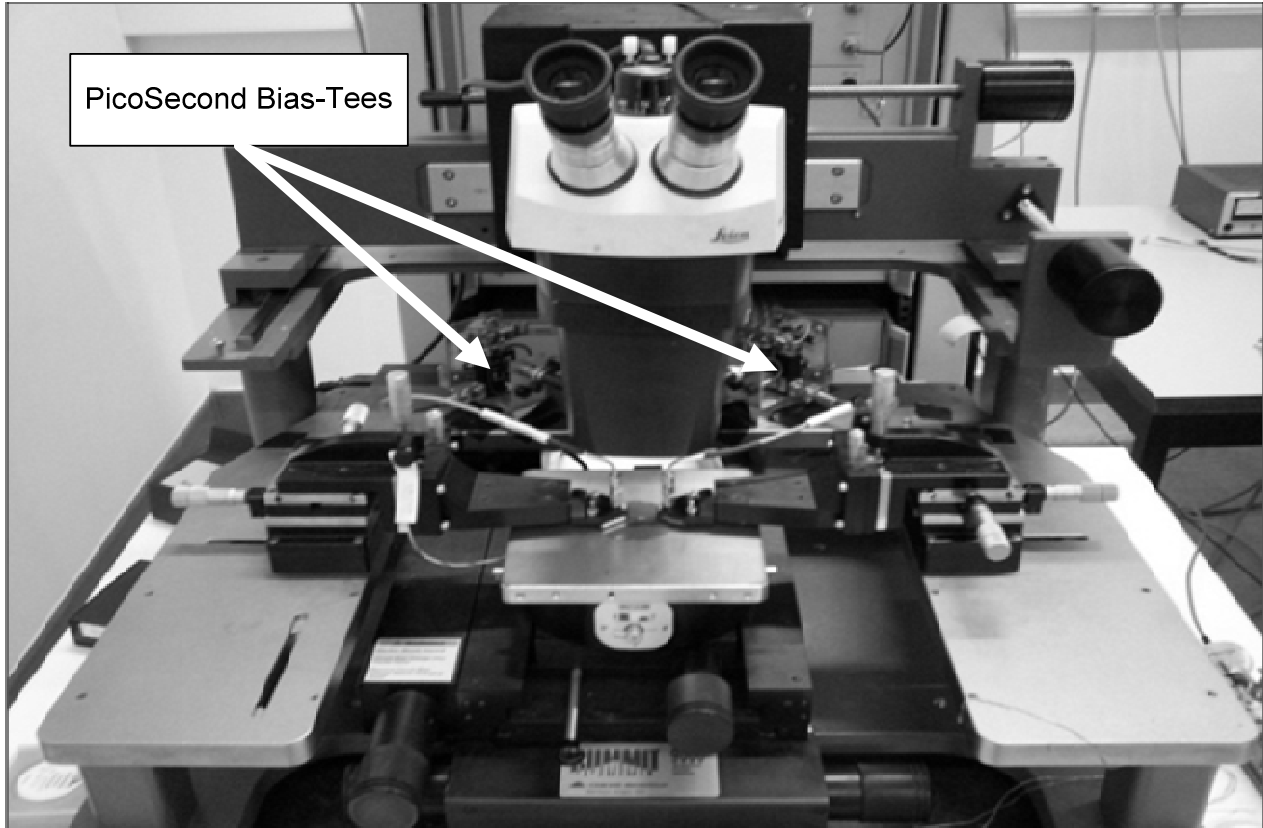


Figure 2.9 The modified LSNA with the external Picosecond bias-tee used to perform the large-signal two tone measurements.

2.5 Conclusion

In this chapter, an overview of GaN HEMT technology is given, along with the basic principles of the measurement instruments required in the modelling process. Before the characterisation can begin, a device selection process is followed to ensure that the optimal device of the desired topology is selected. It is very important to have a thorough understanding of the basic principles of the measurement instruments, which will ensure the correct interpretation of measured data. This chapter gives an overview of the VNA and LSNA. The linear S-parameters of the devices are measured using the VNA, which is used to extract the small-signal equivalent circuit parameters (ECP). From the small-signal ECP, the nonlinear models are constructed and verified using an LSNA.

CHAPTER 3

Intermodulation Distortion Characterisation

3.1 Introduction

Intermodulation distortion (IMD) predictions have become a critical part of microwave and RF amplifier design. Greater performance is required from amplifier and receiver circuits due to the development of new and more sophisticated modulation techniques. Intermodulation is unwanted in any system, as it creates spurious signals and generates minor to severe interference with operations. Thus, the ability to predict IMD allows for optimal system design and simulation. In the equivalent circuit model, the drain current source I_{ds} is the main contributor to the nonlinear behaviour of the device [1], [7]. The I_{ds} current derivatives are thus essential for the construction of models that can accurately predict nonlinear IMD. In this chapter, a measurement setup is investigated that is used to extract the higher order derivatives of the nonlinear drain current source $I_{ds}(V_{gs}, V_{ds})$. The derivatives and cross-derivatives of I_{ds} with respect to V_{gs} and V_{ds} are extracted directly from measurements. The technique was first applied in [6] to extract the coefficients of GaAs field effect transistor (FET) devices, where the cross-terms of the $I_{ds}(V_{gs}, V_{ds})$ Taylor series expansion were successfully extracted. This technique is an extension of [9], where previously the cross-terms were neglected, also noted in [8], [10]. The goal of this chapter is to investigate if this extraction procedure can be applied to high-power gallium nitride (GaN) high-electron mobility transistors (HEMT) devices. The investigation starts by implementing the technique on a GaAs FET device measured at the University of Stellenbosch, then extending the measurement setup to measure on-wafer GaN HEMT devices at the Interuniversity Microelectronics Centre (IMEC) in Leuven, Belgium.

The question can be asked why a special measurement setup must be used to extract the higher order derivatives of the drain and why it cannot be obtained directly from DC measurements. One of the most important questions when evaluating $I_{ds}(V_{gs}, V_{ds})$ is if data derived from DC is still valid for AC analysis. It is generally considered that $I_{ds}(V_{gs}, V_{ds})$ can be represented as a memory-less function, which implies the quasistatic assumption. The quasistatic approximation implies that the response of each of the nonlinearities at a certain time does not depend on past time AC behaviour can be viewed as a succession of static DC excitations. Under this assumption, DC behaviour can indeed be used to predict AC performance. However, this is a theoretical assumption and is not adequate in practice [1], [2]. Derivatives cannot be extracted

from DC as a result of errors associated with successive differential operations. It is almost impossible to determine small-signal nonlinearities for Volterra analysis by differentiating the measured I/V characteristic. The repeated differentiation of the measured I/V curve introduces numerical noise, which in most cases becomes significantly large relative to the nonlinearity, as shown in Figure 3.1. The most accurate and widely used method is to extract the Taylor series coefficients from RF measurements. Thus any empirical model intended to predict very high signal-to-distortion ratios must be extracted from, or at least adjusted to, measured higher order AC data. In the same way that G_m and G_{ds} is extracted from measured linear S-parameter data, so too the higher order current derivatives must be extracted from higher order AC behaviour. The goal of this chapter is to describe the measurement techniques used to extract the nonlinear Taylor coefficients directly from measurements.

It is vital to understand the origins of distortion behaviour before undertaking the task of IMD characterisation. These principles are discussed in section 3.2. Section 3.3 gives an overview of the principles of Volterra series analysis, which is used as a basis to predict the intermodulation performance of the devices. In section 3.4, the nonlinear Taylor series model of the drain current source $I_{ds}(V_{gs}, V_{ds})$ is presented. The full IMD characterisation procedure is discussed in section 3.5, which includes the measurement setups and extraction software used in this work. Section 3.6 documents the detailed methodology involved in the extraction process. The results and experiences gained during the study are documented in section 3.7, while section 3.8 gives the final comments of the work presented in this chapter.

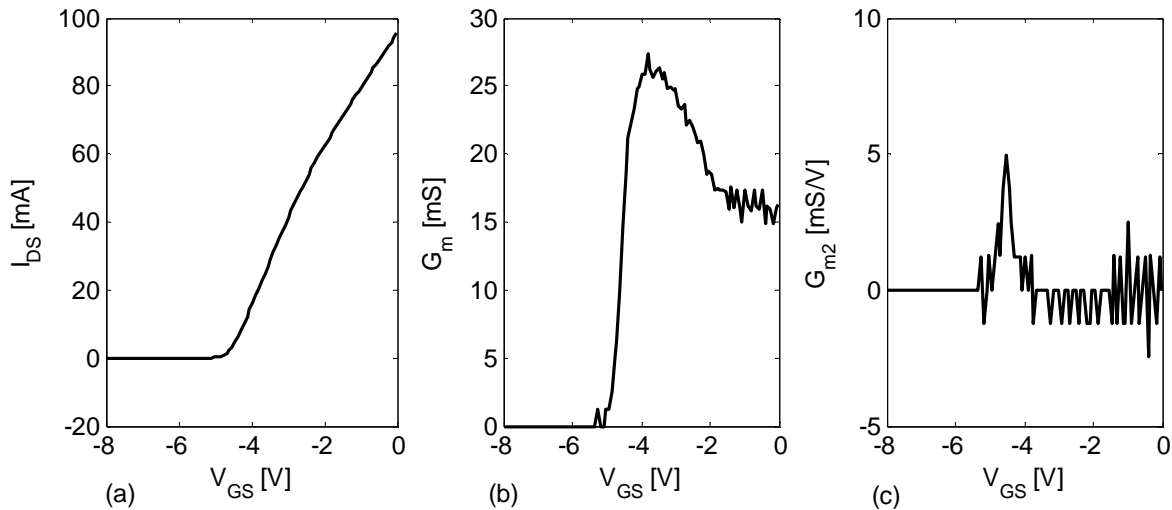


Figure 3.1 (a) The plot of measured DC drain current I_{DS} is shown, while (b) a noisy G_m is shown, which was obtained by directly differentiating I_{DS} . In (c) an extremely noise G_{m2} is plotted, which was determined by differentiating G_m .

3.2 Origin of Nonlinear Distortion Behaviour

Before a nonlinear model is developed and the task of IMD predictions undertaken, the fundamental principle and origin of nonlinear distortion behaviour should be fully understood. In this section, a mathematical analysis of an arbitrary nonlinearity will be used to demonstrate the origin of important nonlinear parameters. Only the basic principles are discussed in this section, but for the full mathematical analysis of the nonlinear phenomenon refer to [1], [3].

Figure 3.2 shows a general third order nonlinearity with an excitation V_s and a resulting current I . The source impedance is set to zero to simplify the mathematical analysis and thus V equals V_s . The current I can be found by substituting the source voltage V_s into a third order power series function that describes the nonlinear current expressed in equation (3.1) where a , b and c are constant, real coefficients. For the purpose of this example to simplify the mathematics, V_s is restricted to a two-tone excitation given by equation (3.2).

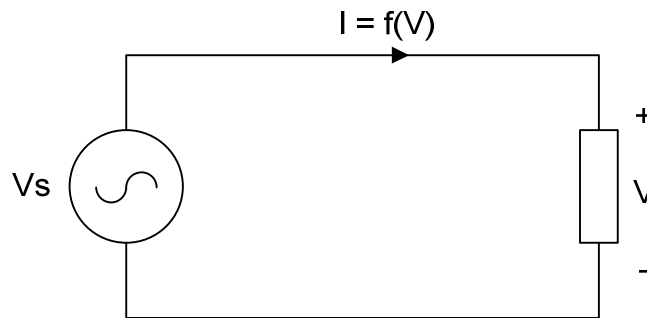


Figure 3.2 A nonlinearity excited by voltage source V_s with the current a nonlinear function of the voltage V across the nonlinear device is used to demonstrate the mathematical origin of intermodulation distortion.

$$I = aV + bV^2 + cV^3 \quad (3.1)$$

$$V_s = V = V_1 \cos(\omega_1 t) + V_2 \cos(\omega_2 t) \quad (3.2)$$

Substituting equation (3.2) into equation (3.1) results in three terms that can be grouped together to describe the order of the nonlinear current components. The total current in the nonlinear element is the sum of the currents components given by equations (3.3), (3.4) and (3.5).

$$i_a = aV_s(t) = aV_1\cos(\omega_1 t) + aV_2\cos(\omega_2 t) \quad (3.3)$$

$$i_b(t) = bV_s^2 = \frac{b}{2} \left\{ \begin{aligned} &V_1^2 + V_2^2 + V_1^2\cos(2\omega_1 t) + V_2^2\cos(2\omega_2 t) \\ &+ 2V_1V_2[\cos((\omega_1 + \omega_2)t) + \cos((\omega_1 - \omega_2)t)] \end{aligned} \right\} \quad (3.4)$$

$$i_c(t) = cV_s^3 = \frac{c}{4} \left\{ \begin{aligned} &V_1^3\cos(3\omega_1 t) + V_2^3\cos(3\omega_2 t) \\ &+ 3V_1^2V_2[\cos((2\omega_1 + \omega_2)t) + \cos((2\omega_1 - \omega_2)t)] \\ &+ 3V_1V_2^2[\cos((\omega_1 + 2\omega_2)t) + \cos((\omega_1 - 2\omega_2)t)] \\ &+ 3(V_1^3 + 2V_1V_2^2)\cos(\omega_1 t) \\ &+ 3(V_2^3 + 2V_1^2V_2)\cos(\omega_2 t) \end{aligned} \right\} \quad (3.5)$$

The current component given by equation (3.3) is the result of the first term in equation (3.1) and is the linear or first order component. Equation (3.4) is quadratic term in equation (3.1) and is the second order component, while equation (3.5) is due to the cubic term and is the third order response. Trigonometric identities shown in equations (3.6) to (3.8) for squares and products of cosines were used to simplify equations (3.3) to (3.5).

$$\cos(\alpha) \cdot \cos(\alpha) = \frac{1}{2}\cos(\alpha - \beta) + \frac{1}{2}\cos(\alpha + \beta) \quad (3.6)$$

$$\cos(\alpha)^2 = \frac{1}{2} + \frac{1}{2}\cos(2\alpha) \quad (3.7)$$

$$\cos(\alpha)^3 = \frac{3}{4}\cos(\alpha) + \frac{1}{4}\cos(3\alpha) \quad (3.8)$$

In equations (3.3) to (3.5) it can be seen that several new frequency products are generated by a fairly simple nonlinearity. These equations can be used to explain a number of nonlinear effects that are common in RF devices and systems, such as harmonic generation, saturation, cross-modulation, AM-to-PM conversion and intermodulation. All these characteristics can serve as a figure of merit when defining different aspects of a system or circuits nonlinear behaviour. All these phenomena have been describe in literature [1], [3], but the most relevant to this thesis is harmonic and IMD.

IMD is the result of two or more signals of different frequencies that are present at the input of a nonlinear device. These signals are mixed together and form additional signals at frequencies that are not at harmonic frequencies of the original input signals. The mixing frequencies are linear combinations of the terms in equations (3.3) to (3.5) and are expressed as $\pm m\omega_1 \pm n\omega_2$, except where m or n is equal to zero. The order of the distortion product is given by the sum of $|m| + |n|$. Even-order products usually occur at much higher or lower frequencies than the original signals and thus do not cause any interference problems. The products that warrant concern are the third order products that occur at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ as they fall within the pass-band and are the strongest of all the odd-order products. This statement implies that these components are significantly close to the original signals. These are extremely difficult to reject with filters and are the main source of distortion in any system. Thus, it is extremely important that any nonlinear model should accurately predict third order IMD products.

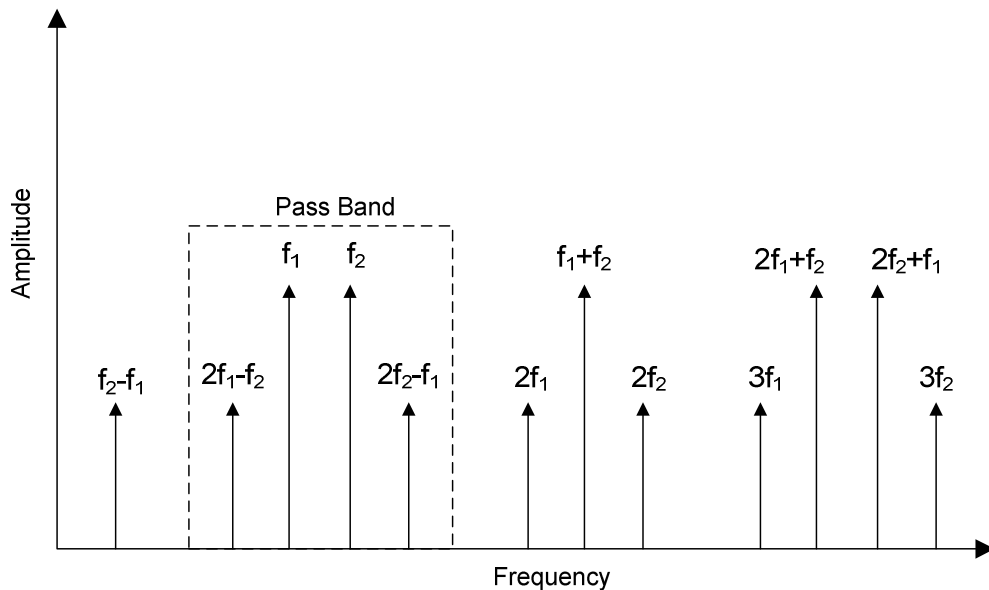


Figure 3.3 The distribution of harmonics and intermodulation products are plotted versus frequency for a two-tone excitation ω_1 and ω_2 . It can be seen that intermodulation products fall within the pass band.

3.3 Principles of Volterra Series Analysis

The standard analysis technique for distortion prediction in medium power systems has been Volterra series analysis, which can be divided into two approaches. The first is a transfer function approach where general n^{th} order Volterra kernels are derived from first principles [1], [11]. However the method is fairly complex when applied to circuits with multiple nodes and

thus will not be considered. The second and most common technique is known as the method of nonlinear currents, which has the advantage that only the frequency components of interest need to be calculated. The following section is a summary of this approach, as demonstrated in [1], [2].

3.3.1 Nonlinear Currents Method

The nonlinear currents method is an extension of the Volterra series and in this technique the current components are calculated using lower order voltage components. These current components are used to determine the voltage components of the same order, which in turn are used to calculate the next higher order current components. As mentioned, the advantage of this approach is that it is only necessary to calculate the frequency components of interest, thus it is rarely necessary to calculate the entire nonlinear transfer function.

The circuit shown in Figure 3.4 is used to demonstrate the analysis procedure. The circuit consists of a voltage source, a linear resistor and a nonlinear conductance. The conductance has a voltage of $v(t)$ across it and a current response $i(t)$. The current/voltage relation is expressed in equation (3.9).

$$i = g_1 v + g_2 v^2 + g_3 v^3 + \dots \quad (3.9)$$

The Taylor series coefficients are given by g_n , while $i(t)$ and $v(t)$ represent the incremental current and voltage associated with the nonlinear conductance around the bias point. The voltage $v(t)$ consists of all the mixing products. The sum of all n^{th} order mixing products is represented by $v_n(t)$, as shown in equation (3.10). The order of mixing products is defined by checking the subscript of the term, for example, v_1 represents the first order product, while v_2 the second order product and v_3 the third order product. When two terms are multiplied, the order of the product is determined by adding the subscript values, for example, $v_1 v_2$ results in a third order product and $v_2 v_3$ in a fifth order product.

$$v = v_1 + v_2 + v_3 + v_n + \dots \quad (3.10)$$

$$v = v_1 + v_2 + v_3 \quad (3.11)$$

The circuit in Figure 3.4 is now transformed using the substitution theorem, which is discussed in the next section, and redrawn as shown in Figure 3.5(a). The nonlinearity is transformed to a linear conductance and several nonlinear current sources. The linear conductance represents the

linear part of equation (3.9) and the current sources represent the nonlinear terms in equation (3.9). The goal is to only predict up to the third order products (IM3) and thus the Taylor series and the mixing products are limited to the third degree. Equation (3.10) can be rewritten only to include the third degree and lower terms, as shown in equation (3.11).

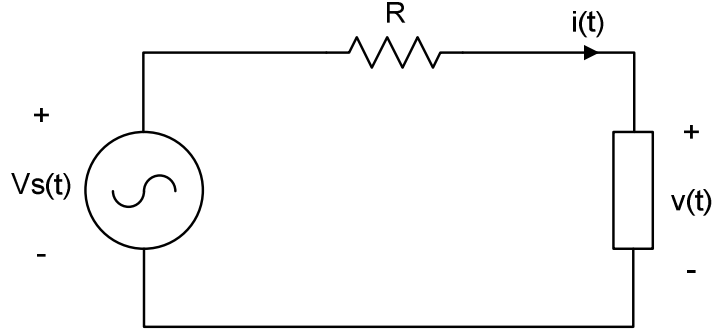


Figure 3.4 The circuit used to demonstrate the nonlinear currents method consists of a voltage source $v_s(t)$, a linear resistor R and a weakly defined nonlinearity with a voltage drop of $v(t)$.

The next step is to determine the second v^2 and third v^3 order voltage terms in equation (3.9). The determination of the v^2 term will be demonstrated as an example. Equation (3.12) shows the product of the terms in equation (3.11), while equation (3.13) expresses all the terms after the multiplication procedure. The result is a number of terms ranging in orders from second degree v_1^2 to sixth degree v_2^3 . The only terms of interest are the third degree and lower terms. The first two terms in equation (3.14) are third degree and lower, while the terms in the square bracket are higher than third degree and can be neglected. The result is that equation (3.14) can be simplified to equation (3.15). The same technique is used to determine the third order term v^3 , which leads to equation (3.16).

$$v^2 = (v_1 + v_2 + v_3)(v_1 + v_2 + v_3) \quad (3.12)$$

$$v^2 = v_1^2 + v_1v_2 + v_1v_3 + v_2v_1 + v_2^2 + v_2v_3 + v_3v_1 + v_3v_2 + v_3^2 \quad (3.13)$$

$$v^2 = v_1^2 + 2v_1v_2 + [2v_1v_3 + 2v_2v_3 + v_2^2 + v_3^2] \quad (3.14)$$

$$v^2 = v_1^2 + 2v_1v_2 \quad (3.15)$$

$$v^3 = v_1^3 \quad (3.16)$$

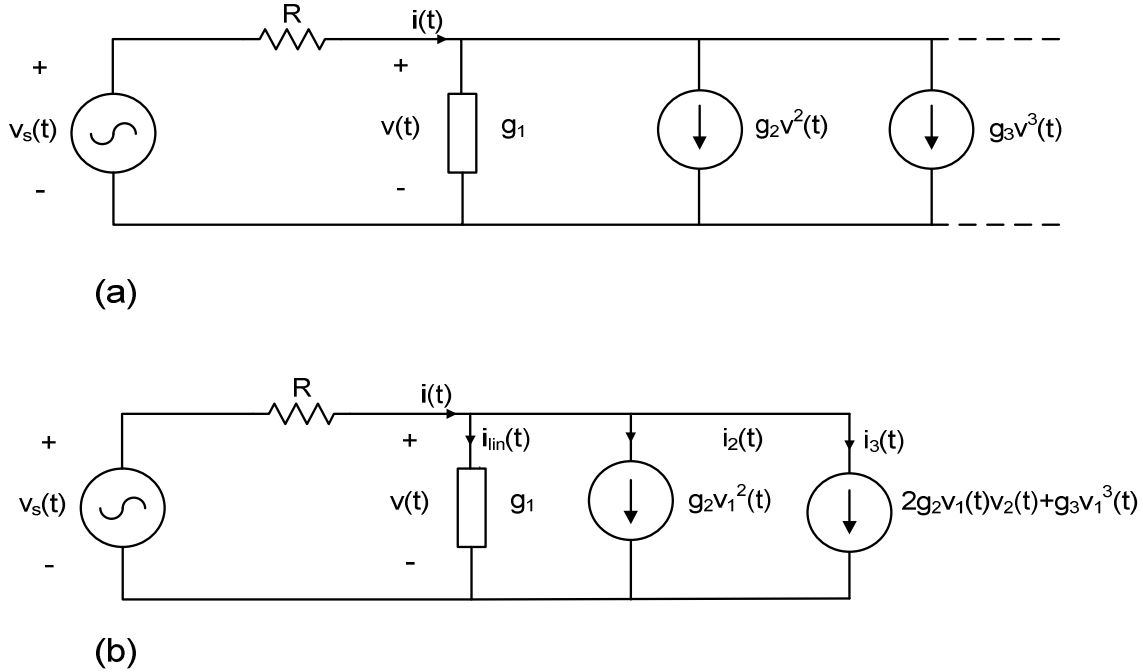


Figure 3.5 In (a) the nonlinear resistor has been converted to a linear resistor and a set of nonlinear current sources. In (b) the current sources have been rearranged so that each represents a single order of mixing products.

Now the circuit in Figure 3.5(a) is rearranged as shown in Figure 3.5(b) so that each current source represents the same order of mixing frequencies. The total current $i(t)$ is a combination of all the current sources as expressed in equation (3.17). The linear part of the current is expressed by equation (3.18) and the current sources $i_2(t)$ and $i_3(t)$ in equation (3.19) and equation (3.20), represent all the second and third order current components in the nonlinear elements that arise from the terms in equation (3.9).

$$i = i_{lin} + i_2 + i_3 \quad (3.17)$$

$$i_{lin} = g_1 v = g_1 [v_1 + v_2 + v_3] \quad (3.18)$$

$$i_2 = g_2 v_1^2 \quad (3.19)$$

$$i_3 = 2g_2 v_1 v_2 + g_3 v_1^3 \quad (3.20)$$

The voltage $v(t)$ over the linear resistor $g_1(t)$ can be easily expressed in terms of the excitation voltage $v_s(t)$ by using the standard voltage divider rule. In equations (3.18) to (3.20) it can be

seen that the first order voltage components $v_1(t)$ are generated by the first order source $v_s(t)$, the second order current $i_2(t)$ is a function of the first order voltages, and the third order current $i_3(t)$ is a function of the first and second order voltages. This implies that the currents of each order greater than one are always functions of lower order voltages. From these observations, an analysis procedure can be formulated:

The first step is to find the first order components by open circuiting the current sources, thereby setting them equal to zero and finding $v_1(t)$ under $v_s(t)$ excitation, which is an ordinary linear analysis. The second step is to determine the second order current, $i_2(t)$, from the voltages $v_1(t)$ found in the previous step. The voltage source $v_s(t)$ is short-circuited, making $i_2(t)$ the only excitation. Now the second-order voltages $v_2(t)$ can be determined, by performing a linear analysis of the circuit. In the third step, the third-order current $i_3(t)$ can be derived from $v_1(t)$, $v_2(t)$, $g_2(t)$ and $g_3(t)$. The voltage source $v_s(t)$ is short-circuited and the current source $i_2(t)$ open-circuited for the calculation of the third order voltages components. The procedure can be continued up to the desired higher order response. From these voltage and current components, the output powers can be calculated at the desired frequencies.

The procedure explained above forms the basis of the nonlinear currents method and will be implemented to extract the Taylor series coefficients. The aim of the nonlinear currents method is to predict a set of voltages and currents and then to compare the result to a set of measured values. The result is a matrix of equations where the only the coefficients are unknown and by applying simple calculations, the coefficients can be solved.

3.3.2 The Substitution Theorem

In section 3.3.1, the substitution theorem is referred to. In this section, the method will be described as detailed in [1]. Figure 3.6(a) shows a linear voltage-controlled current source I with a current GV , where V is defined as the control voltage over the source. The current is unchanged if the controlled source is substituted with a transconductance G . The principle stays the same for a source with a more complicated nonlinear transfer function. If a conductance having the same I/V characteristic can be substituted, then the presentations will be equivalent. Thus, the formal definition of the substitution theorem is:

“A linear or nonlinear resistive circuit element having the characteristic $I=f(V)$ is equivalent to a controlled current source having the same characteristic, wherein V is the terminal voltage.” [1].

An illustration of the substitution theorem is shown in Figure 3.6(b). The I/V characteristic of the nonlinear conductance is described by the power series in equation (3.21). The nonlinear element

can be described by an equivalent circuit that includes a linear conductance G_1 and controlled current sources representing the higher-degree terms in the series as seen with the circuit on right in Figure 3.6(b).

$$i = g_1 v + g_2 v^2 + g_3 v^3 + \dots \quad (3.21)$$

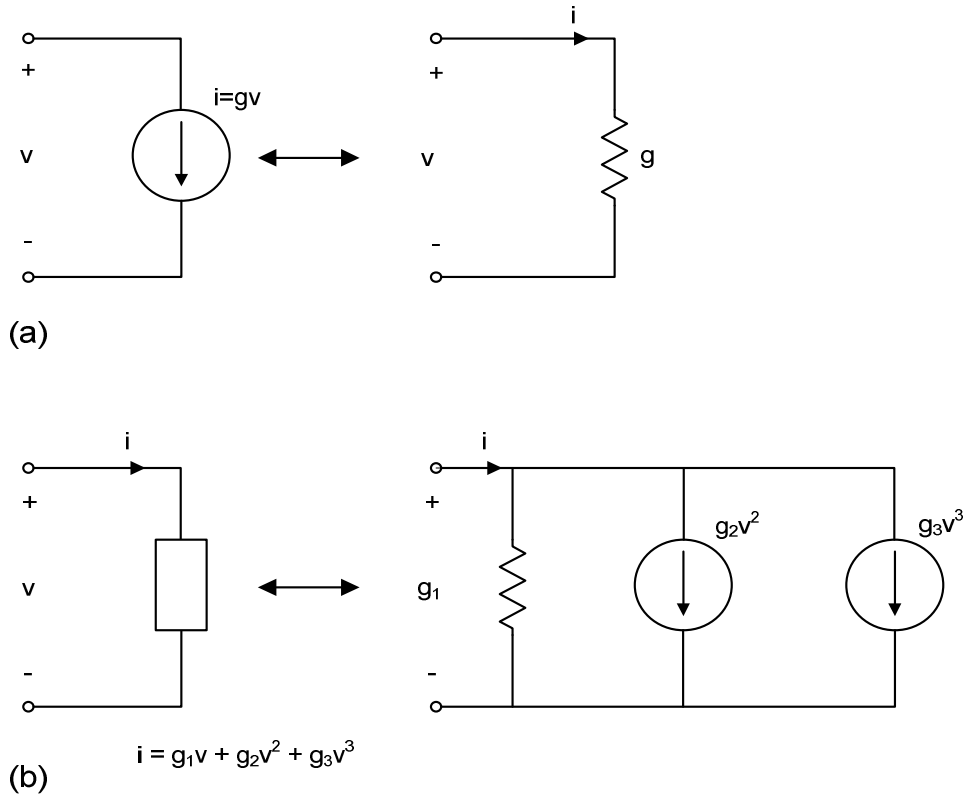


Figure 3.6 (a) A linear-voltage controlled source $i = gv$ can be substituted by a current source with a conductance g and the current will be unchanged. In (b) a nonlinear conductance described by the power series $i = g_1.v + g_2.v^2 + g_3.v^3$ is replaced by a linear conductance g_1 and controlled current sources representing the higher-degree terms in the series.

3.4 Nonlinear Taylor Series IMD Model

The main goal of this chapter is to demonstrate the IMD modelling and characterisation techniques implemented for the GaN HEMT power transistors. However, before the power devices were measured a system was investigated and developed at the University of Stellenbosch where firstly a CFY-30 GaAs FET was characterised. The purpose of this system was to serve as a test scenario, where the hardware, software and Volterra series analysis

techniques were evaluated. This system was successfully developed with positive results, which will be demonstrated in section 3.7, and used as basis for the on-wafer systems used at IMEC. The measurement setup is used to directly extract the Taylor series coefficients of the nonlinear drain current $I_{ds}(V_{gs}, V_{ds})$, but before this can be done, a model for $I_{ds}(V_{gs}, V_{ds})$ must be defined. Firstly, the drain current source in the case of a GaAs FET device is modelled by a two-dimensional Taylor series [2], [6], and secondly for a GaN HEMT by a one-dimensional Taylor series [14] in the vicinity of the DC bias voltages. This section will describe each of the models and provide the reasoning behind the different models.

The origins of intermodulation in the FET will be investigated by examining the nonlinear current source $I_{ds}(V_{gs}, V_{ds})$. The FET model is dependent on two control voltages (V_{gs}, V_{ds}) and thus requires a two-dimensional Taylor series expansion [1], [2], [6] given by equation (3.22).

$$\begin{aligned}
I_{ds}(V_{gs}, V_{ds}) = & I_{DS} + \frac{\delta I_{ds}}{\delta V_{gs}} v_{gs} + \frac{\delta I_{ds}}{\delta V_{ds}} v_{ds} + \\
& + \frac{1}{2} \frac{\delta^2 I_{ds}}{\delta V_{gs}^2} v_{gs}^2 + \frac{\delta^2 I_{ds}}{\delta V_{gs} \delta V_{ds}} v_{gs} v_{ds} + \frac{1}{2} \frac{\delta^2 I_{ds}}{\delta V_{ds}^2} v_{ds}^2 \\
& + \frac{1}{6} \frac{\delta^3 I_{ds}}{\delta V_{gs}^3} v_{gs}^3 + \frac{1}{2} \frac{\delta^3 I_{ds}}{\delta V_{gs}^2 \delta V_{ds}} v_{gs}^2 v_{ds} + \frac{1}{2} \frac{\delta^3 I_{ds}}{\delta V_{gs} \delta V_{ds}^2} v_{gs} v_{ds}^2 + \frac{1}{6} \frac{\delta^3 I_{ds}}{\delta V_{ds}^3} v_{ds}^3
\end{aligned} \tag{3.22}$$

In this expression, I_{DS} represents the DC bias current of $I_{ds}(V_{GS}, V_{DS})$, while v_{gs}, v_{ds} are the small-signal AC deviations of V_{gs} and V_{ds} from the bias point. The derivatives are evaluated at V_{gs} equal to V_{GS} and V_{ds} equal to V_{DS} [6]. The AC component of equation (3.22) can be expressed in terms of incremental voltages and currents and rewritten in equation (3.23).

$$\begin{aligned}
i_{ds}(v_{gs}, v_{ds}) = & G_m v_{gs} + G_{ds} v_{ds} + \\
& + G_{m2} v_{gs}^2 + G_{md} v_{gs} v_{ds} + G_{d2} v_{ds}^2 + \\
& + G_{m3} v_{gs}^3 + G_{m2d} v_{gs}^2 v_{ds} + G_{md2} v_{gs} v_{ds}^2 + G_{d3} v_{ds}^3
\end{aligned} \tag{3.23}$$

The coefficients in equation (3.23) correspond to the derivatives of equation (3.22) and Table 3.1 identifies the significance of each coefficient [6]. G_m and G_{ds} can be extracted from conventional small-signal measurements, while the cross-products G_{md} , G_{m2d} and G_{md2} are the coefficients that physically arise from the interaction observed between the input and the output of the device, which is responsible for the nonlinear mixing of the v_{gs} and v_{ds} signals.

G_m	linear transconductance
G_{ds}	output conductance
G_{m2}, G_{m3}	second and third order transconductance variations with V_{gs}
G_{d2}, G_{d3}	second and third order output conductance variations with V_{ds}
G_{md}, G_{m2d}	first and second order nonlinear dependence of G_{ds} on V_{gs}
G_{md}, G_{md2}	first and second order nonlinear dependence of G_m on V_{ds}

Table 3.1 It is important to understand the physical meaning of each coefficient as it will give insight into the parameter extraction process. The significance of each coefficient is summarised in this table.

GaAs FET's are relatively low-power devices and generating cross-products to measure and evaluate by exciting the gate and the drain ports with external sources is fairly standard. However, as the device power increases, so too does the excitation levels required to generate distortion, especially at the drain of the device. The GaN devices measured at IMEC are high-power devices and thus require much larger excitation levels at the drain port. Thus, to be able to generate the required cross-products, the measurement system should have a high-power source at the drain side and very high-performance diplexer to reject the leakage of harmonics generated from the large signal source. Even if such a measurement system can be developed, the main problem is still that a large drive signal at the output of the device will make it act in an unnatural way, which implies that the validity of the data for such a measurement is questioned. This is not a unique problem to the GaN HEMTs measured at IMEC. In more recent work [14], it has been demonstrated that the nonlinear drain current source of high-power GaN transistors can successfully be modelled with a one-dimensional Taylor series expansion. The result is that the expression in equation (3.22) is now replaced with equation (3.24). In terms of incremental voltages and currents equation (3.23) can now be expressed as equation (3.25).

$$I_{ds}(V_{gs}) = I_{DS} + \frac{\delta I_{ds}}{\delta V_{gs}} v_{gs} + \frac{1}{2} \frac{\delta^2 I_{ds}}{\delta V_{gs}^2} v_{gs}^2 + \frac{1}{6} \frac{\delta^3 I_{ds}}{\delta V_{gs}^3} v_{gs}^3 \quad (3.24)$$

$$i_{ds}(v_{gs}) = G_m v_{gs} + G_{m2} v_{gs}^2 + G_{m3} v_{gs}^3 \quad (3.25)$$

Studies have shown that modelling high-power GaN devices with this model produces good results [14] and thus extracting G_m , G_{m2} and G_{m3} is sufficient for accurate intermodulation distortion analysis. The expression given in equation (3.25) is used to model the nonlinear current source for the GaN HEMTs in this work and results shown in chapter four and five validate the model as being accurate and reliable. The next section details the characterisation procedure used to extract the Taylor series coefficients described in this section.

3.5 IMD Characterisation Procedure

The characterisation procedure used to extract the nonlinear coefficients was based on the setup presented in [2], [6]. An equivalent measurement setup was used. However, additional Matlab software was developed to automate the extraction procedure. The hardware setup in this work was extended for test fixture and on-wafer measurements as demonstrated at the University of Stellenbosch and at IMEC in Belgium. The proposed measurement setup is a low-frequency intermodulation test system to measure the second and higher order intermodulation performance of a device's drain current source, $I_{ds}(V_{gs}, V_{ds})$. The advantage of the system is that the higher order derivatives and cross-derivatives of I_{ds} with respect to V_{gs} and V_{ds} are directly extracted through measurements. The following sections give a detailed description of the measurement setups and the software procedure used to extract the nonlinear current coefficients.

3.5.1 IMD Measurement Setups

The IMD measurement setup is designed for low frequency measurements, which implies that the device should behave as a memory-less nonlinearity. The frequencies selected must be low enough so that the effects of the device capacitances can be neglected, but as high as possible so that low-frequency dispersion can be avoided. Following this reasoning, frequencies between 9MHz and 30MHz were selected and the measurement system was designed accordingly. Taking into account the availability of components and the chosen frequency range, excitation frequencies of 9MHz and 10MHz were selected for excitation sources V_S and V_L respectively. The block diagram of the measurement setup is shown in Figure 3.7. The figure shows two excitation sources V_S and V_L that are injected at the gate and the drain ports respectively, which must have very good spectral purity and are used to induce distortion in the device. The distortion components are measured as output powers on a spectrum analyser. The disadvantage of using the spectrum analyser is that only the magnitude of the output powers can be measured and thus another method must be used to determine the phase of these components. The possibility of using an oscilloscope to determine the phase of the output signals was investigated.

The investigation revealed that the oscilloscope's dynamic range is not sufficient and thus phase of signals that are less than -40dBm in power cannot be determined. Because the second and third order powers are low-level signals, a phase change cannot be determined in this way. The general method is to determine the phase change manually by evaluating the location of the power nulls. A power null is where a nonlinear coefficient has a change in sign, which will be discussed in section 3.5.2.

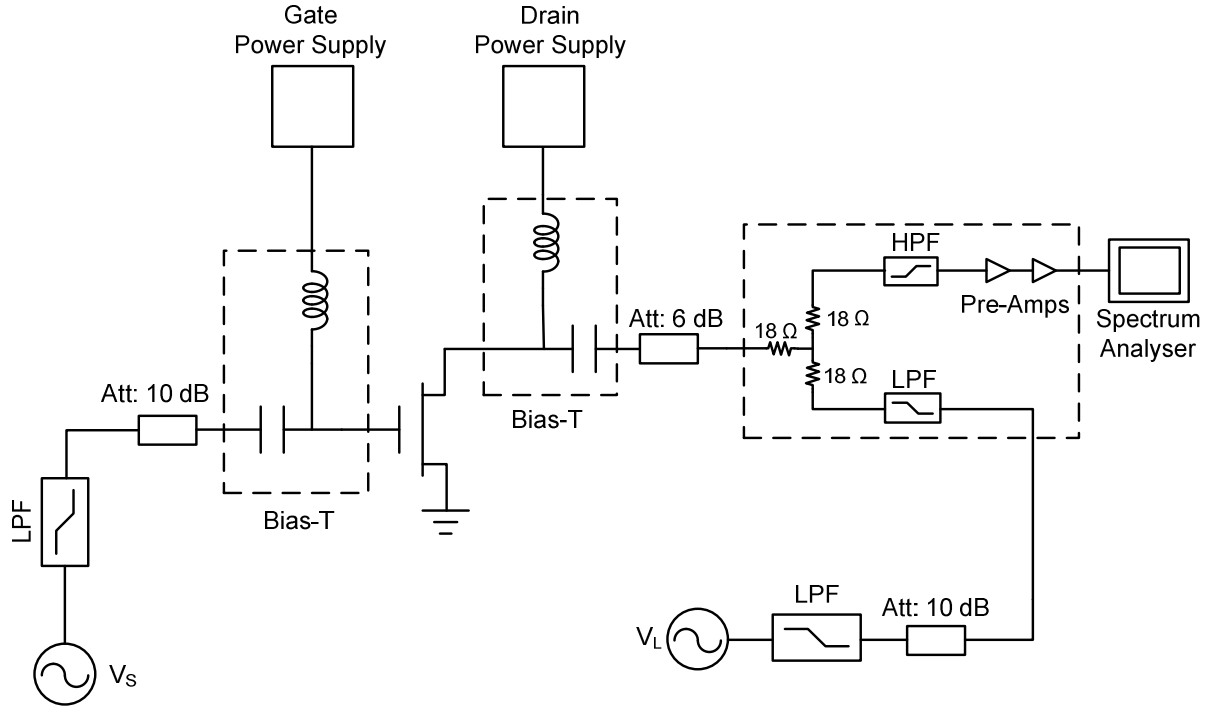


Figure 3.7 The block diagram of the low-frequency IMD measurement setup used to extract the nonlinear coefficients of the drain current $I_{ds}(V_{gs}, V_{ds})$.

As stated above, signals with very good spectral purity have to be injected into the gate and drain terminals of the device. The second and third harmonics generated from the signal source need to be rejected as much as possible as these components could create unwanted spurious signals that could result in mixing products that are not generated by the device. The additional mixing products could lead to inaccurate coefficient extractions. Coaxial Mini-Circuits 10.7MHz low-pass filters are connected to each signal generator to filter out any spurious harmonic distortion, while attenuators guarantee the necessary broadband matching at all ports. Figure 3.8 shows the S_{21} response of the 10.7MHz coaxial filter as measured on a network analyser. The filter has an insertion loss of about 0.3dB in the pass band and a rejection of about 27.65dB at 18MHz and 35.5dB at 20MHz in the stop-band as demonstrated in Figure 3.8.

An important consideration in the system is the design of the diplexer. The diplexer consists of a 18MHz high-pass and 10MHz low-pass filter connected in parallel. The filters are connected via a 6dB resistive divider, consisting of three 18Ω resistors. The circuit diagram of the diplexer is shown in Figure 3.9. The main objective is to reject the fundamental frequencies and ensure that the signal levels from the amplifiers do not generate unwanted spurious signals. Thus, only the higher order components are passed through the diplexer, while the fundamental tones from V_s and V_L are rejected. The response of the diplexer is given in Figure 3.10 as measured on a network analyser. S_{21} is the response of the low-pass filter and S_{32} the response of the high-pass filter. S_{13} is a measure of the isolation that port 3 has from port 1.

The diplexer is followed by an amplifier stage. Mini-Circuits Era-51 broad-band monolithic amplifiers were used for the gain blocks in this stage. These are wideband amplifiers that offer high dynamic range and are relatively simple to implement. Figure 3.9 shows the block diagram of the diplexer and amplifier with the port allocations as measured on the VNA. In Figure 3.10, the S_{21} , S_{31} and S_{32} responses of diplexer and amplifier stages is shown. This figure shows that the response over the required frequency range is relatively flat over the frequency band. Figure 3.11 shows a photograph of all the components necessary to extract the nonlinear coefficients of any device. Figure 3.12 shows a photograph of the IMD system used for test fixture measurements at the University of Stellenbosch. The IMD system was adapted to measure the on-wafer devices at IMEC, shown in Figure 3.13. The next section describes the technique used to determine the phase change of the nonlinear current derivatives, which corresponds to a power null in the measured output power curves.

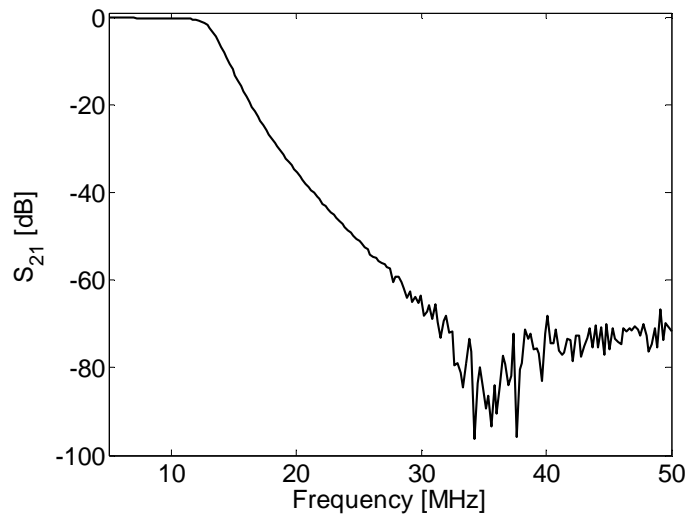


Figure 3.8 The S_{21} response of the 10.7 MHz coaxial low-pass filter.

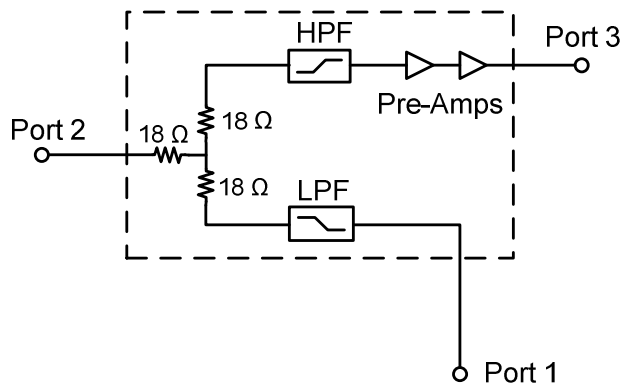


Figure 3.9 The circuit diagram of the diplexer and amplifier stages with the port allocations measured on the VNA.

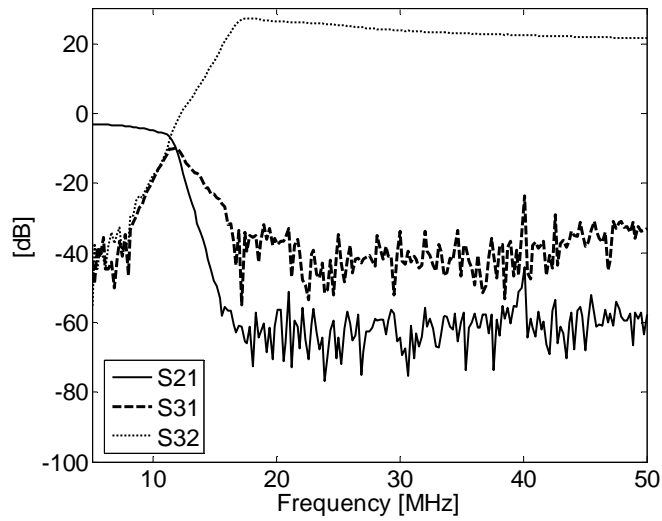


Figure 3.10 The transmission coefficients S_{21} , S_{31} and S_{32} measurements of the diplexer and the amplifier stage combined.

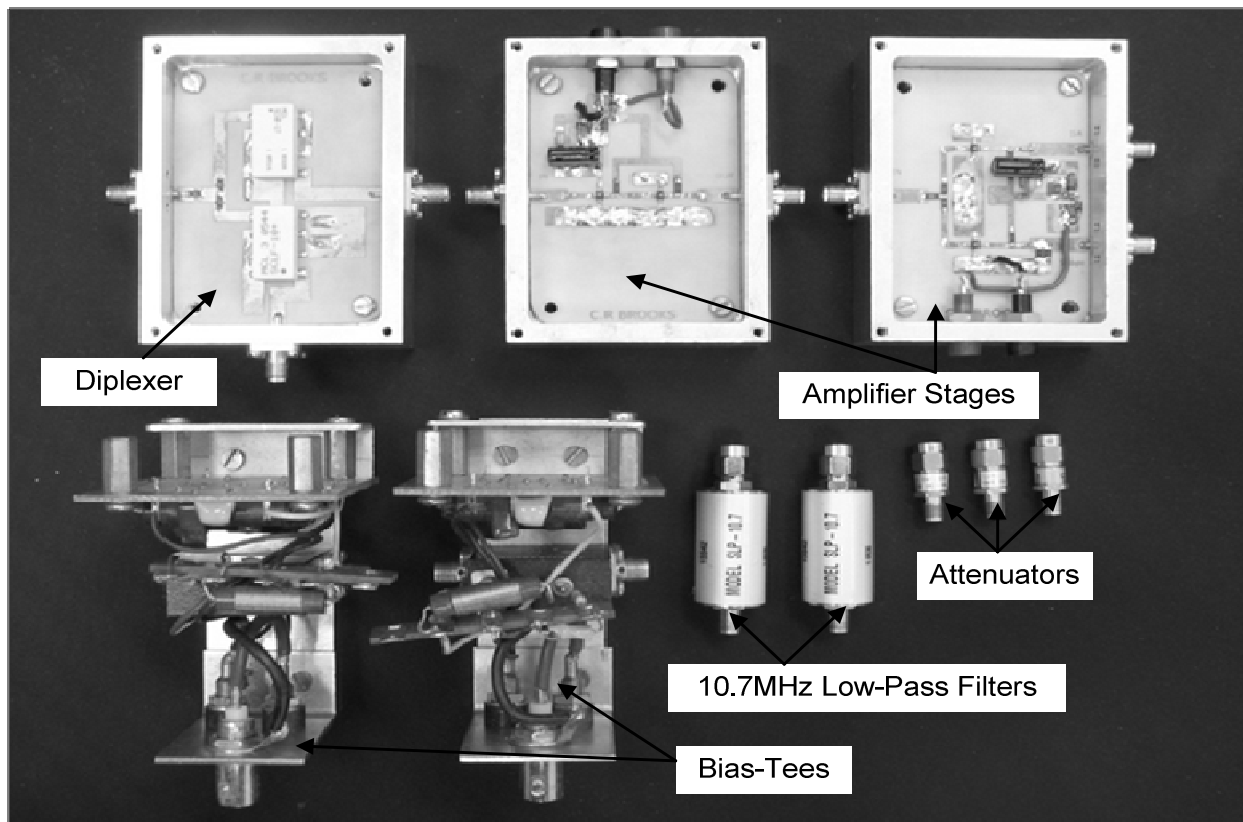


Figure 3.11 The complete set of components needed to perform the extraction procedure consists of two bias-tees, two 10.7MHz low-pass filters, three attenuators, a diplexer and amplifier stages.



Figure 3.12 A photograph of the IMD system used for test fixture measurements at the University of Stellenbosch to extract the higher order current derivatives of the CFY-30 GaAs FET.

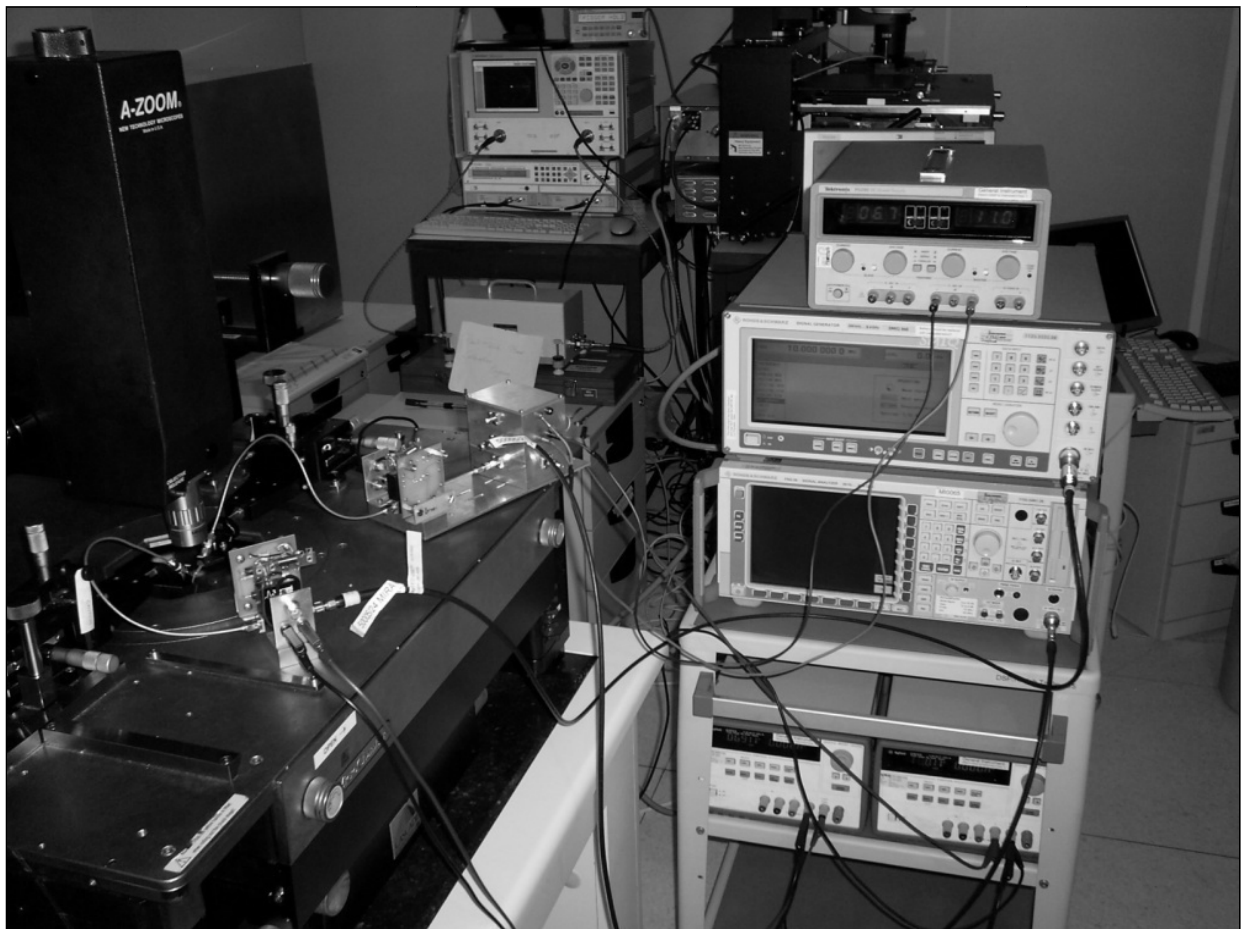


Figure 3.13 The IMD system was adapted to extract the current derivatives of the on-wafer GaN HEMT devices measurement at IMEC.

3.5.2 Phase Information

Phase information is very important as it represents the sign of the Taylor series coefficients that are extracted during the characterisation process. As mentioned, phase formation cannot be determined using only the spectrum analyser and thus the goal of this section is to describe an alternative method to determine the phase definitions. The advantage of using a low-frequency measurement setup is that all the Taylor series coefficients become purely real. This ensures that the infinite possible range of unknown phases, are restricted to a value of 0 or 180 degrees. A phase change can be determined by evaluating where the power nulls are located. The easiest way to identify a power null is to find a sharp downward spike in the output power curves as indicated in Figure 3.14. The $P_o(2\omega_1)$ curve represents the second harmonic and has a sharp downward spike at around -3.644V, which indicates a power null and a phase change. The same argument is valid for $P_o(3\omega_1)$, which is the third order harmonic. Where $P_o(2\omega_1)$ has a gradient of zero, the phase of $P_o(3\omega_1)$ will change as seen at about -4.615V.

By using simple reasoning, the phases of the coefficients can be determined [2]. Firstly, below cut-off, the device has zero current, which results in zero n^{th} degree coefficients as seen in Figure 3.15. As the device starts to conduct, the threshold is passed and every n^{th} degree coefficient must start with a positive value. The n^{th} degree coefficient will keep its sign until the $(n-1)^{\text{th}}$ degree coefficient passes through a maximum and begins to decrease. As the n^{th} degree coefficient is simply the derivative of the $(n-1)^{\text{th}}$ degree coefficient at this point, the n^{th} degree coefficient must pass through zero and change its sign as seen in Figure 3.15. Following this simple reasoning, the phase information of all the Taylor series coefficients can be determined up to the desired order.

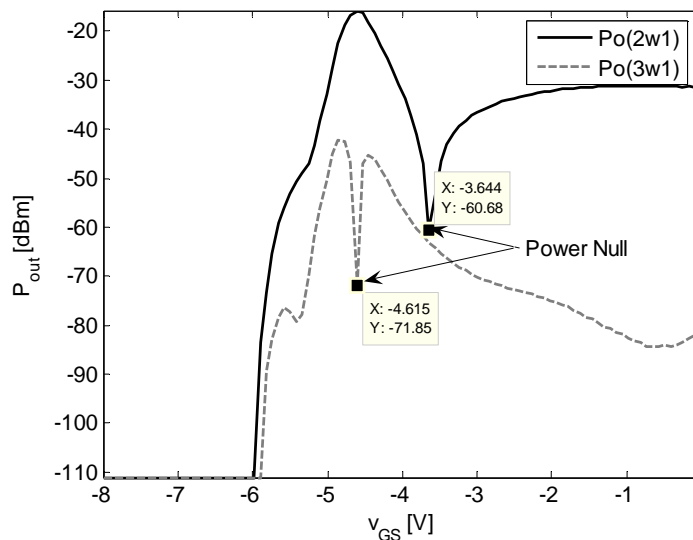


Figure 3.14 The measured second $P_o(2\omega_1)$ and third $P_o(3\omega_1)$ harmonic output power levels with each experiencing a power null, from which the phase information can be extracted.

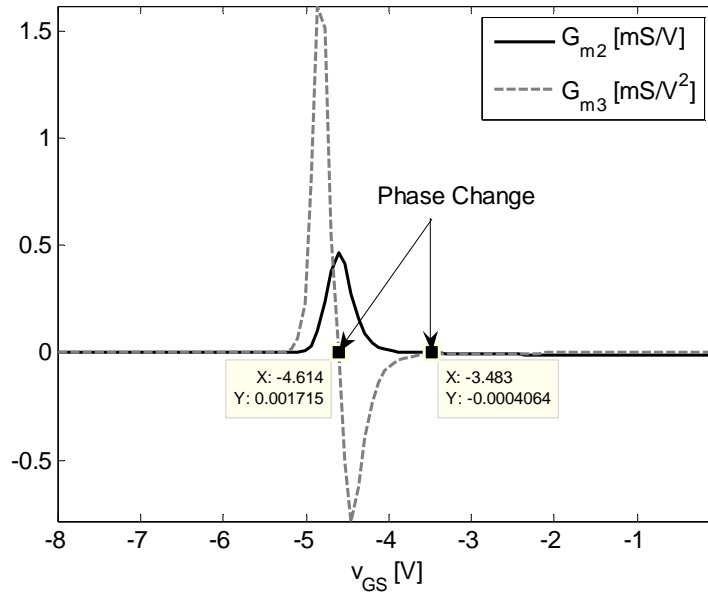


Figure 3.15 The extracted second G_{m2} and third G_{m3} order Taylor series coefficients which both change phase over the gate voltage V_{GS} bias range.

3.5.3 De-Embedding Procedure

The first objective of the de-embedding procedure is to determine the source impedance Z_S , Z_L , the excitation voltages $V_S(\omega_1)$, $V_L(\omega_2)$ and the port voltages $V_1(\omega)$, $V_2(\omega)$ as seen in Figure 3.16. Secondly, the response of the diplexer and amplifier stages must be defined to de-embed the measured output power levels from the spectrum analyser and determine the exact levels at the ports of the device. Once the exact output powers are measured at the ports, the voltages can be calculated. It is important to accurately determine the voltages, impedances and currents injected into the terminals of the device as these values are used in the nonlinear currents method calculations, which will be demonstrated in section 3.6. Thus, the cables, filters, attenuators, bias-tees, diplexer and amplifiers have to be characterised and de-embedded.

The de-embedding structures for the gate and drain ports are presented in Figure 3.17(a) and Figure 3.17(b) respectively. The setups are reconstructed to exactly match the setups used during the IMD measurements, which will ensure accurate results. Firstly, the gate port is evaluated by performing a two-port S-parameter measurement on the setup shown in Figure 3.17(a) and a three-port measurement on the setup in Figure 3.17(b). All the S-parameters are measured using a calibrated VNA. By measuring $S_{21}(\omega_1)$ in Figure 3.17(a) and $S_{21}(\omega_2)$ in Figure 3.17(b), the response of the signal through the gate and drain biasing network can be determined. Subtracting the transmission parameter $S_{21}(\omega)$ from the level on the signal generator $P_{SIG}(\omega)$, the exact signal

level at the gate terminal $P_S(\omega_1)$ and $P_L(\omega_2)$ can be calculated. This power level in dBm can be converted to a voltage value using the standard log conversion to obtain the equivalent power in Watts. To determine excitation voltages $V_S(\omega_1)$, $V_L(\omega_2)$, the source impedance $Z_S(\omega_1)$, $Z_L(\omega_2)$ must first be determined. $Z_S(\omega_1)$ is calculated by converting S_{22} in Figure 3.17(a) into the equivalent input impedance as seen from the gate of the device under test. $Z_L(\omega_2)$ is determined in an equivalent way by converting S_{22} , seen in Figure 3.17(b), into an impedance value. Once the excitation voltages $P_S(\omega_1)$, $P_L(\omega_2)$ and source impedances $Z_S(\omega_1)$, $Z_L(\omega_2)$ are determined, then equations (3.26) to (3.27) can be used to calculate the equivalent source voltages $V_S(\omega_1)$, $V_L(\omega_2)$. The next step is to determine the port voltage $V_1(\omega)$, $V_2(\omega)$ at the terminals of the device. The measured low-frequency S-parameters taken from the VNA at the external terminals of the device are converted to Y-parameters. Using the Y-parameters, the input and output impedances $Z_{in}(\omega)$ and $Z_{out}(\omega)$ of the device are determined. With the source voltages $V_S(\omega_1)$, $V_L(\omega_2)$, source impedance $Z_S(\omega_1)$, $Z_L(\omega_2)$ and terminal impedances $Z_{in}(\omega)$, $Z_{out}(\omega)$ shown by the transistor, it is possible to determine the voltages at the device terminal $V_1(\omega_1)$ and $V_2(\omega_2)$.

$$V_S(\omega_1)[V] = \sqrt{1000 \times P_S(\omega_1)[mW] \times Z_S(\omega_1)[\Omega]} \quad (3.26)$$

$$V_L(\omega_2)[V] = \sqrt{1000 \times P_L(\omega_2)[mW] \times Z_L(\omega_2)[\Omega]} \quad (3.27)$$

It should be noted that the drain setup is dependent on the device measured. In the case of the Stellenbosch measurement setup, where the FET device was characterised, the device was excited with signals at the gate and drain of the device. However, in the setup at IMEC, only a signal at the gate of the device was injected and the third port of the diplexer in Figure 3.17(b) is terminated with a 50Ω load. Thus the drain excitation V_L is set to zero, as there is no drain excitation and the only parameter that needs to be determined is Z_L .

The final stage in the process is to de-embed the response of the diplexer and amplifier stages seen in Figure 3.17(b). By subtracting the $S_{32}(\omega)$ transmission coefficient from the measured output power levels on the spectrum analyser $P_{SA}(\omega)$, the exact levels at the ports of the device can be determined $P_2(\omega_{mix})$. The spectrum analyser $P_{SA}(\omega)$ measurements are performed at all the second and third order mixing products. Once again, the measured value is in dBm and by following the procedure above, the voltage at the terminals of the device can be determined using equation (3.28).

$$V_2(\omega_{mix1})[V] = \sqrt{1000 \times P_L(\omega_{mix})[mW] \times Z_L(\omega_{mix})[\Omega]} \quad (3.28)$$

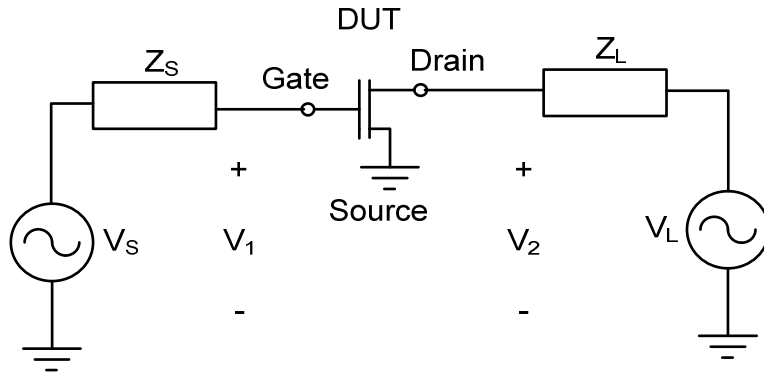


Figure 3.16 The goal of the de-embedding procedure is to determine the impedance Z_S , Z_L and injected voltages V_S , V_L as these parameters are used in nonlinear currents method calculations.

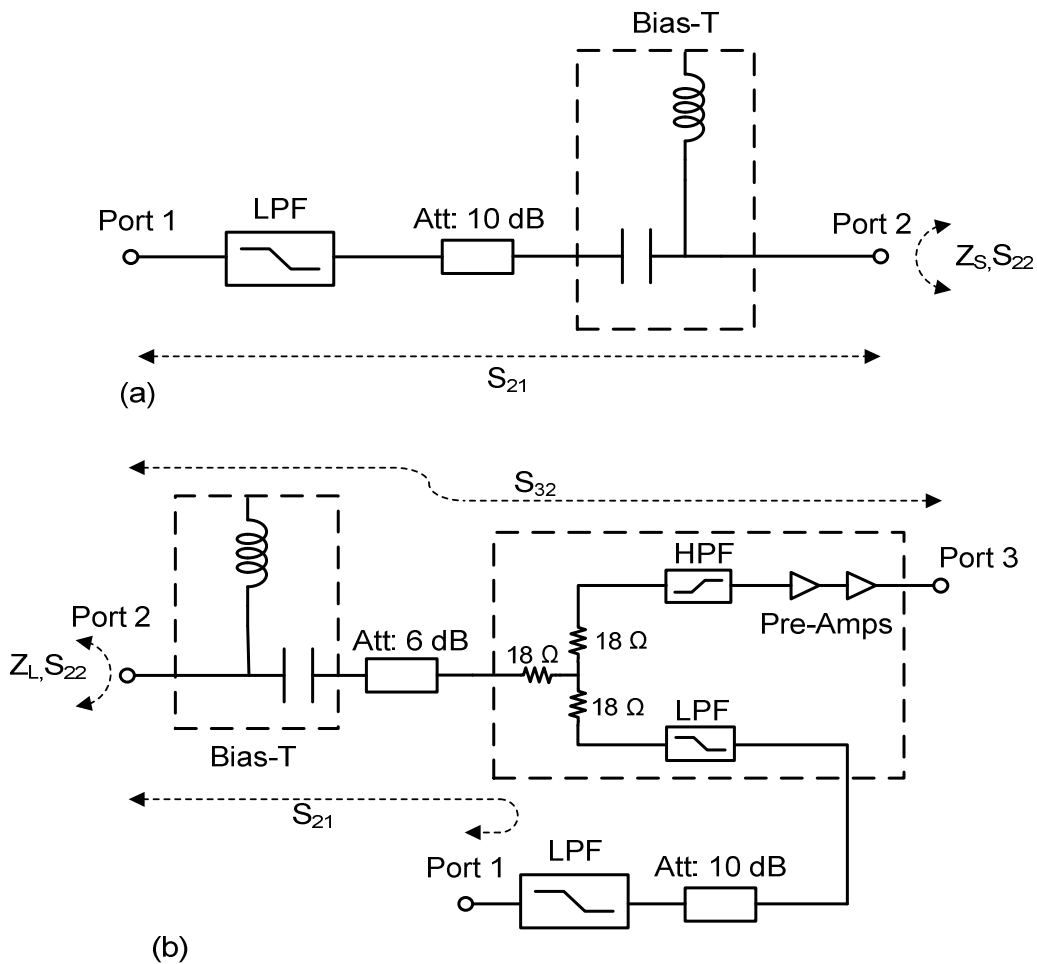


Figure 3.17 The de-embedding setup taking into account the low-pass filter, attenuator, bias-tee, cables and transition as connected to the (a) gate and (b) drain port of the device under test.

3.5.4 Measurement Extraction Procedure

The main goal of the measurement setup is to measure various mixing IMD products of the devices under test (DUT). The output powers measured are converted to voltage and current values and by applying the nonlinear currents method, the IMD behaviour of the devices is predicted. The measured and predicted parameters are presented in a matrix, which is a function of the nonlinear coefficients. The advantage of using this technique is that by applying simple matrix algebra the coefficients can be determined. The basic idea of the extraction procedure is to measure the output powers of the device as a function of the gate voltage V_{GS} . The gate voltage is swept from a point where the device is in pinch-off to another point at which the device is fully conducting. Each gate voltage sweep is performed at a predefined drain bias V_{DS} point. From the measurements and using the nonlinear currents method, the higher order current derivatives of the drain current $I_{ds}(V_{gs}, V_{ds})$ are determined as a function of the gate bias, V_{GS} . However, before this bias sweep is done, the appropriate excitation power levels have to be determined. The power levels should not be too high, otherwise spurious signals are generated which cause inaccurate coefficient calculations, but should be high enough to cause distortion that can be measured accurately.

A Matlab procedure has been developed to fully automate the extraction process. Before the extraction can begin, a number of parameters need to be specified, for example, voltages, excitation frequencies, maximum power levels, delay between measurement points and the spectrum analyser settings. Most of these settings will be different for various devices, thus the characteristics of each device should be taken into account. For example the biasing voltage range for the different technologies will not be the same. The spectrum analyser settings include the resolution bandwidth, video bandwidth and the frequency span. The centre frequency setting is automatically determined when the user specifies the excitation frequencies f_1 and f_2 . A trade-off between measurement time and spectrum analyser settings has to be considered. The narrower the resolution and video settings are, the longer the extraction time, but measurements are done with greater accuracy. The complete extraction procedure can vary between one and one-and-a-half hours, depending on the parameter settings. When working with these devices, one must take care not to overstrain the devices, especially when dealing with new technologies. In some cases, as seen at IMEC, there are only a few working devices on a new wafer and device degradation needs to be considered. The following section describes the three stage extraction procedure that was implemented in this work to extract the nonlinear Taylor series coefficients of the drain current source $I_{ds}(V_{gs}, V_{ds})$.

The first step is to determine the gate voltage V_{GS} at which the device switches on, known as the threshold voltage V_T . At this point, the device behaves in its most nonlinear way and will be used in the second step to determine the optimum input powers. For each measurement, the drain voltage V_{DS} is set to a predefined value, while the gate voltage V_{GS} is swept from a state where

the device is in the pinch-off region to a fully conducting state. The drain current I_{DS} is measured on the programmable Agilent power supplies as a function of the gate voltage and plotted on a graph. A typical plot of the drain current versus gate voltage is shown in Figure 3.18, with the black dot indicating where the device is starting to conduct. The upper gate voltage boundary could not be swept higher than 0V as the DC sources used in these experiments could not reverse polarity. Once the threshold voltage V_T is determined, the next step is to determine the optimal excitation amplitudes injected into the gate and the drain ports of the transistor.

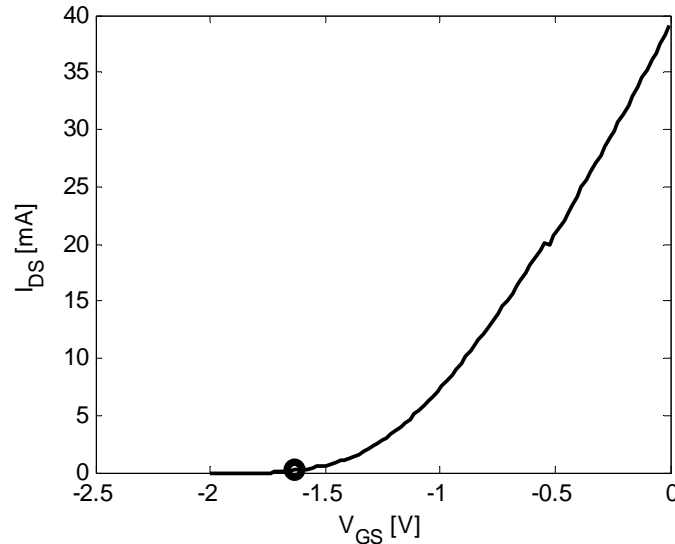


Figure 3.18 A typical plot of drain current I_{DS} versus gate voltages. The black dot around -1.6V is the estimated threshold voltage as determined by the extraction software.

Using the threshold voltage V_T , determined in the previous step, the optimal excitation amplitude levels are determined by performing a power sweep over the specified range of input powers and measuring the output harmonics. Care must be taken in determining the excitation levels, because if the levels are driven too high, the devices could start demonstrating compression or expansion as a result of the higher order products. The goal is to determine the maximum excitation level where the device is still a dominantly third order system. It is important that the device does not exhibit higher than third order responses, as the model used to represent the device's behaviour is based on a third order system. The best value would be the largest input signal where the fundamental curve still has a gradient of 1/1, the second harmonic has a gradient of 2/1 and third harmonic a gradient of 3/1. However, the third harmonic is generally below the noise floor and too small to measure and thus will not be considered. The procedure is to sweep the excitation source $V_S(\omega_1)$ from low to high power value, while $V_L(\omega_2)$ is set to zero as seen in Figure 3.19(a). The next step is to set $V_S(\omega_1)$ to zero and sweep $V_L(\omega_2)$ from a low to a high power value as demonstrated in Figure 3.19(b). In Figure 3.19(a), $P_{out}(\omega_1)$ represents the fundamental output power and $P_{out}(2\omega_1)$ the second harmonic for an excitation signal $P_S(\omega_1)$ at

the gate port. The Matlab software determines the point where the fundamental and the harmonic curves start to deviate from their expected 1/1 and 2/1 gradients. The software also compares the point at which the fundamental and the harmonic exhibit higher than third order behaviour and selects the component with the lowest level as the optimum point. The result is the optimum excitation signal amplitudes to be injected into the gate and the drain of the device.

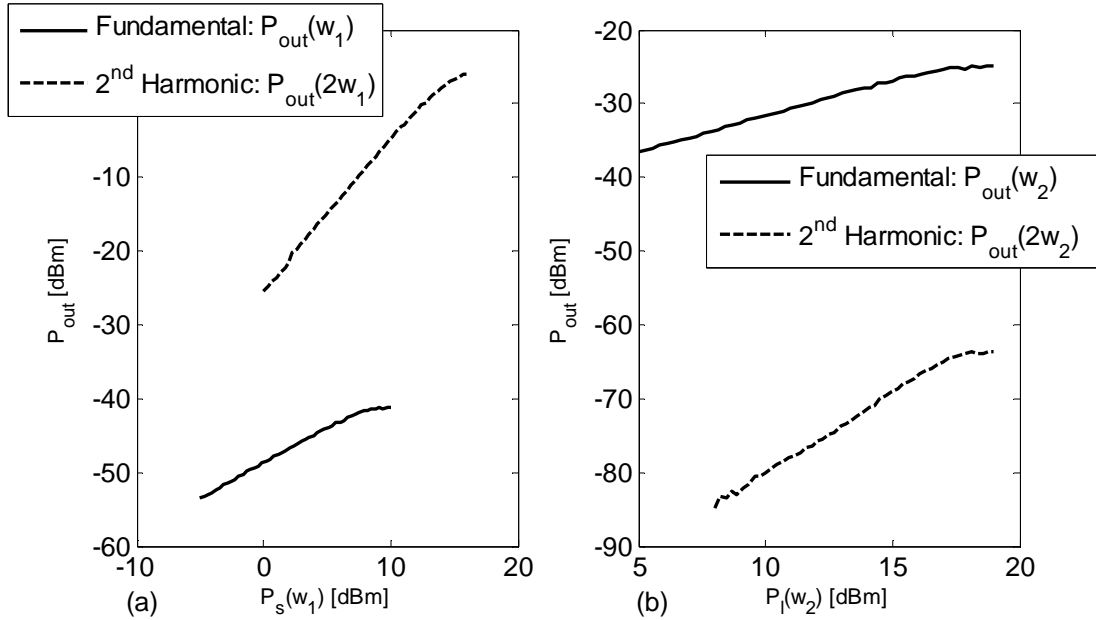


Figure 3.19 (a) The output power of the fundamental and second harmonic versus the input power sweep of $P_s(\omega_1)$, while $P_L(\omega_2)$ is set to zero. (b) The output curves of the fundamental and second harmonic versus the input power $P_L(\omega_2)$, while $P_s(\omega_1)$ is set to zero.

In the final step, the excitation input power levels determined in the previous step are applied to the gate $V_S(\omega_1)$ and drain $V_L(\omega_2)$ ports of the device. The gate voltage V_{GS} is swept with the desired bias range with a set drain voltage V_{DS} . The extraction procedure measures the amplitude levels at the following second and third order products, $P_o(2\omega_1)$, $P_o(\omega_1+\omega_2)$, $P_o(2\omega_2)$, $P_o(3\omega_1)$, $P_o(2\omega_1+\omega_2)$, $P_o(\omega_1+2\omega_2)$ and $P_o(3\omega_2)$. Typical second and third order output power levels measured for the CFY30 are shown in Figure 3.20 and Figure 3.21. Some of the measured output powers have very small levels and are almost in the noise floor and a judgement has to be made regarding the measurement uncertainty in each measurement. Before the output products are measured the input excitation levels are set to zero and five noise floor points are evaluated to determine an average value, which is used as the noise floor parameter. The measured output power levels have to be at least 15dB above the noise floor for an accurate measurement. If the measurement uncertainty is less than 15dB, the measured point is set to the noise floor value seen in Figure 3.21(d).

Figure 3.23 shows the block diagram of the measurement procedure and describes the basic operation of each step. The figure provides an overview of the complete procedure in a simple flow diagram format. As mentioned before, the system was first developed to characterise GaAs FETs at the University of Stellenbosch and later GaN HEMTs at IMEC. In section 3.4, the Taylor series representation of each device is discussed, where firstly the FET is modelled as a two-dimensional series and the HEMT with a one-dimensional series. The procedure described above is used in the case for the GaAs FET with two excitation sources. To characterise the GaN HEMTs, the procedure described above is used, except that only a single excitation signal is injected into the gate of the device $V_S(\omega_1)$, with the source at the drain port $V_L(\omega_2)$ set to zero. The result is that only one second order product at $P_O(2\omega_1)$ and one third order product at $P_O(3\omega_1)$ needs to be measured, as shown in Figure 3.22. From these output products, the G_{m2} and G_{m3} can be directly extracted, which will be discussed in section 3.6. G_m is extracted from conventional small-signal S-parameter measurements. The following section discusses the extraction methodology, which details the determination of the Taylor series coefficients from the output powers measured in this section.

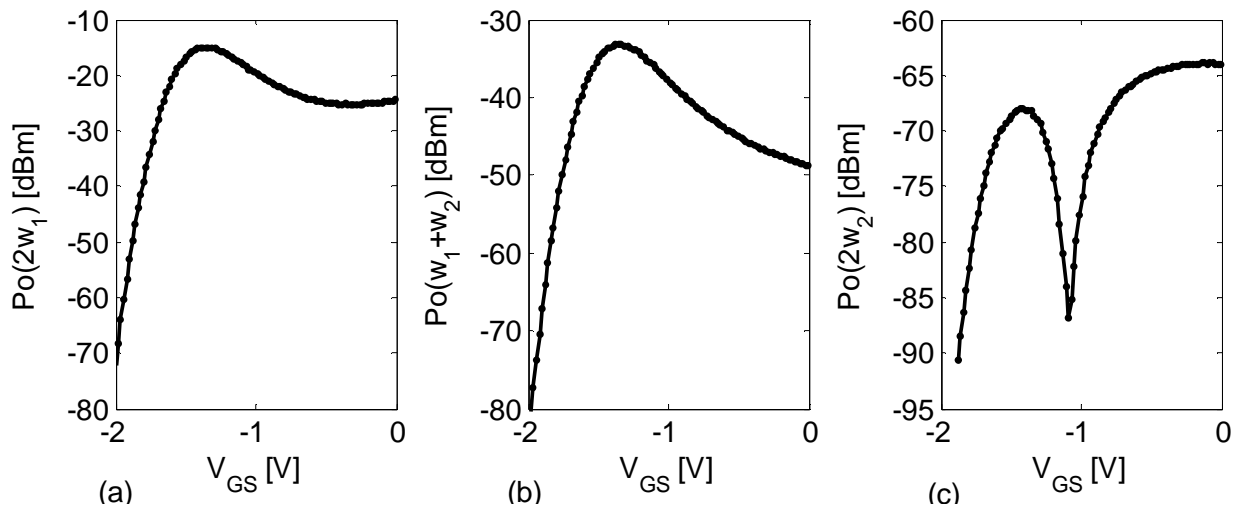


Figure 3.20 The typical second order output powers measured for the CFY-30 GaAs FET, where (a) is output power product at $P_O(2\omega_1)$, (b) at $P_O(\omega_1+\omega_2)$ and (c) $P_O(2\omega_2)$. The output power products are measured as a function of the gate voltage V_{GS} .

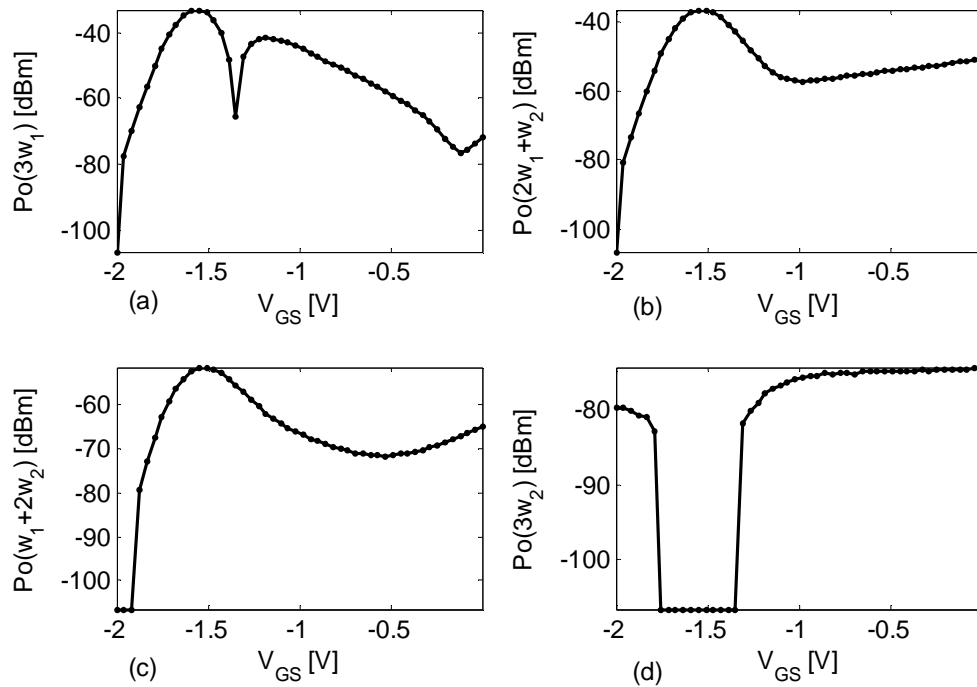


Figure 3.21 The typical third order output powers measured for the CFY-30 GaAs FET, where (a) is output power product at $P_O(3\omega_1)$, (b) at $P_O(2\omega_1+\omega_2)$, (c) $P_O(\omega_1+2\omega_2)$ and (d) $P_O(3\omega_2)$. The output power products are measured as a function of the gate voltage V_{GS} .

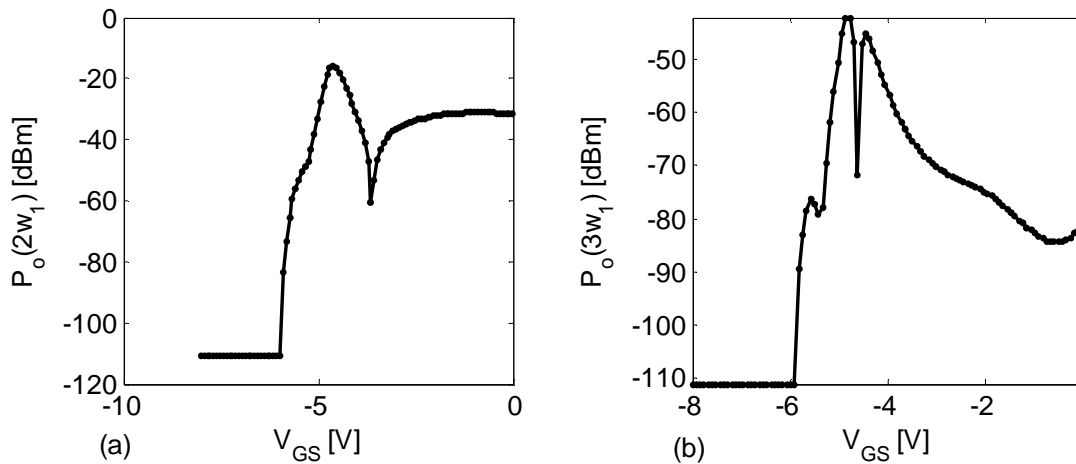


Figure 3.22 The typical second and third order output powers measured for the GaN HEMT, where (a) is output power second order product at $P_O(2\omega_1)$ and (b) the third order product at $P_O(3\omega_1)$. The output power products are measured as a function of the gate voltage V_{GS} .

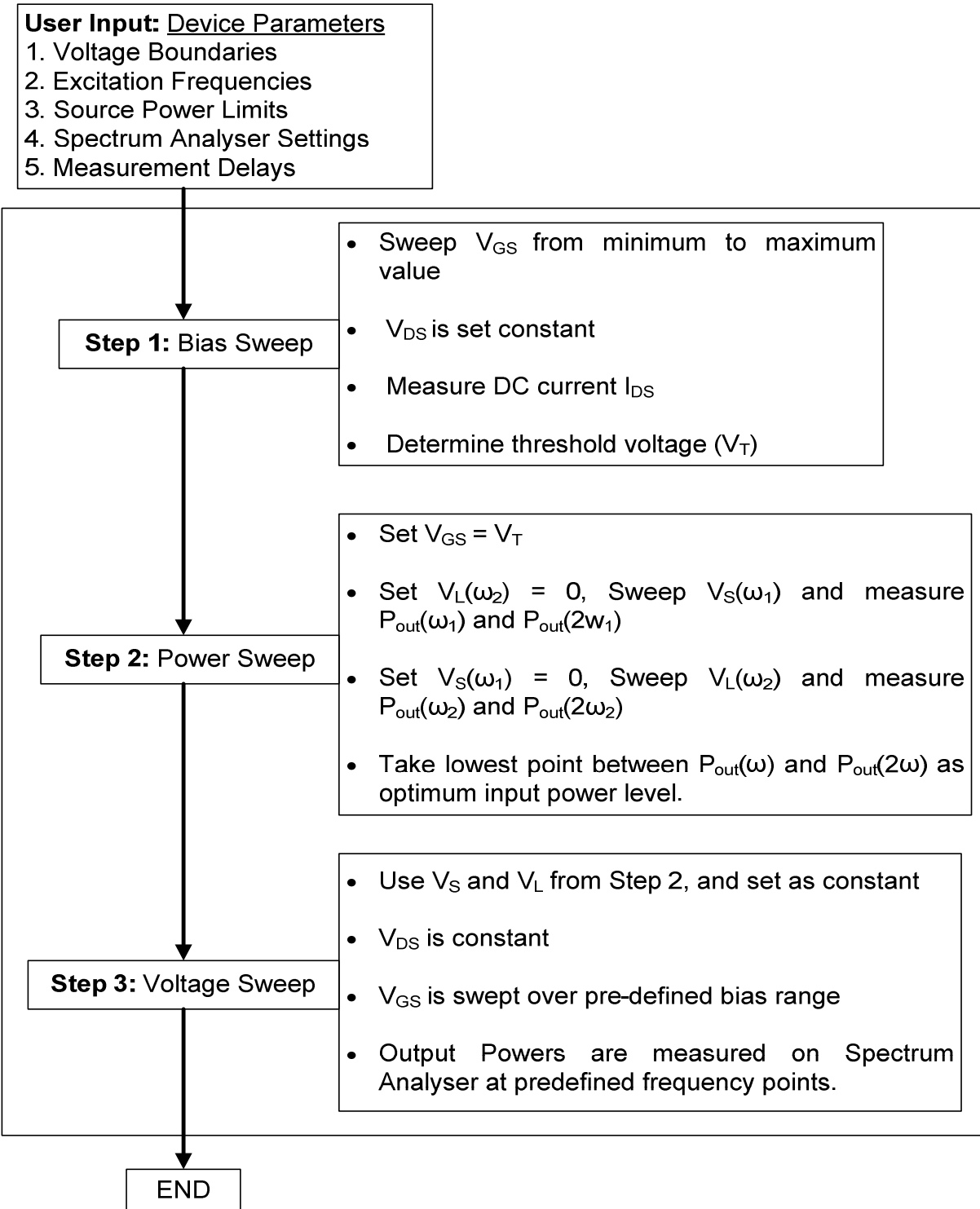


Figure 3.23 The block diagram of the complete measurement procedure is divided into three steps. The first step is a bias sweep, the second is a power sweep and the third is a voltage sweep.

3.6 Extraction Methodology

The main goal of this section is to demonstrate that the extraction methodology is based on the requirement that the system can be described by a set of well conditioned equations. Using the equations described in this section, it is possible to predict a set of the port voltages, for example, $V_1(\omega)$ and $V_2(\omega)$, at the mixing frequencies of interest. Comparing these predicted voltages to the correspondent measured voltages, the desired direct extraction of the seven coefficients can be obtained. The following analytical analysis is a summary of the work presented in [1], [2], [6].

The equivalent circuit used for the nonlinear currents method of Volterra series is shown in Figure 3.24, with the port voltages and currents defined as used in the analysis procedure. As the test system is primarily designed as a low frequency characterisation system, a few assumptions can be made to simplify the analysis. The first is that at very low frequencies, C_{gs} is basically an open circuit and its overall nonlinear contribution can be neglected. Therefore, the only major nonlinear component is the drain current source $NI_{ds}(V_{gs}, V_{ds})$. Thus, the main objective of the extraction procedure is to extract the nonlinear coefficients of the small-signal behavioural model of the drain current source $NI_{ds}(V_{gs}, V_{ds})$. The drain source $NI_{ds}(V_{gs}, V_{ds})$ is assumed to be memory-less and is represented by a bi-dimensional Taylor series approximation in the vicinity of a bias point as described in section 3.4. The capacitances C_{gs} , C_{ds} and C_{dg} of the equivalent circuit in Figure 3.24 can be treated as open circuits at these low frequencies and the inductances L_g , L_d and L_s as short circuits. The simplified equivalent circuit, which is now used in the circuit analysis, is shown in Figure 3.25. The equivalent circuit is divided into four-port system as seen in Figure 3.24 and Figure 3.25, with the Y-parameter matrix relating the port currents, and voltages I_1 , I_2 , V_1 , V_2 to the control voltages V_{gs} , V_{ds} and nonlinear components of the drain currents NI_{ds} . The matrix of Y-parameters is expressed in equation (3.29), with equations (3.30) and (3.31) representing the boundary conditions imposed by the sources (V_L, Z_L) and (V_L, Z_L) . Equations (3.34) and (3.35) express the control voltages (V_{gs}, V_{ds}) in terms of the excitation sources in the equivalent circuit namely $V_S(\omega_1)$, $V_L(\omega_2)$ and NI_{ds} . The constants K_{GS} , K_{GL} , K_{RG} , K_{DS} , K_{DL} and K_{RD} can be determined by applying the superposition principle and de-embedding the parasitics of the external Y-parameters. In the first order or linear response calculations, the current source NI_{ds} in Figure 3.25 is set equal to zero according to the nonlinear currents method of Volterra series analysis. As the first order analysis is assumed to be linear, the principle of superposition holds for the driving voltages $V_S(\omega_1)$ and $V_L(\omega_2)$. The result is that control voltage V_{gs} can be determined in terms of both the excitation sources $V_S(\omega_1)$ and $V_L(\omega_2)$ with the a constant scalar values K_{GS} and K_{GL} respectively. The same principle holds for the determination of the control voltage V_{ds} in terms of $V_S(\omega_1)$ and $V_L(\omega_2)$ with the a constant scalar value K_{DS} and K_{DL} respectively.

In the determination of the second and higher order response the sources V_S and V_L are set equal to zero and the nonlinear current source NI_{ds} is assumed to be the only excitation source.

Applying the nonlinear currents method to the circuit in Figure 3.25 results in a system of coupled equations, expressed in (3.36) and (3.37)[2]. Equation (3.36) represents the second order nonlinear components and (3.37) the third order nonlinear components. $NI_{ds23}(\omega)$ represents the third-order $NI_{ds}(\omega)$ current component generated in the second-degree coefficients.

From an extraction point of view, the first step is to measure the second and third output power ratios between the carriers $Po(\omega_1)$, $Po(\omega_2)$ and the second order mixing products at $2\omega_1$, $\omega_1 + \omega_2$, $2\omega_2$, $3\omega_1$, $2\omega_1 + \omega_2$, $\omega_1 + 2\omega_2$ and $3\omega_2$ on the spectrum analyser. The phase of these products cannot be measured on the spectrum analyser and should be found by evaluating the power nulls that correspond to a phase change, as discussed in section 3.5.2. By using equations (3.29) to (3.35) the desired terminal voltages $V_1(\omega)$ and $V_2(\omega)$ at the seven mixing products of interest can be predicted. The output voltages $V_2(\omega)$ at the mixing frequencies are solved by using equations (3.29) to (3.35), with the excitation sources $V_S(\omega_1)$ and $V_L(\omega_2)$ set to zero. Using the predicted output voltages and the output impedances at each of these frequencies, determined in section 3.5.3, the output powers at $Po(2\omega_1)$, $Po(\omega_1 + \omega_1)$ and $Po(2\omega_2)$ are calculated. By evaluating excitation power levels at $Po(\omega_1)$ and $Po(\omega_2)$, the predicted output carrier-to-harmonic distortion ratios can be constructed and determined. The predicted carrier-to-harmonic distortion ratios are now compared to the corresponding measured values. The result is a system of three linear equations, seen in equation (3.36) that can be solved for the three second order coefficients G_{m2} , G_{md} and G_{d2} . The next step is to use these second order coefficients to predict in a similar way the third order output power ratios that are compared once again to the corresponding measured ratios. The result is a set of four linear equations demonstrated in equation (3.37) from which the four coefficients G_{m3} , G_{m2d} , G_{md2} , G_{d3} can be solved for. The nonlinear coefficients can be extracted with relative ease by the definition of the set of well conditioned equations, making the process fairly robust.

As stated in section 3.4, two Taylor series models are extracted in this work. The first is a model for the low-power GaAs FET two-dimensional data set where G_{m2} , G_{md} , G_{d2} , G_{m3} , G_{m2d} , G_{md2} and G_{d3} are extracted. The second is the extraction of the parameter set for the high-power GaN HEMTs, in which only G_m , G_{m2} and G_{m3} are extracted. In principle, the extraction procedure is exactly the same for both models, except that for the high-power device the simplified model is obtained by setting V_L equal to zero in equations (3.36) to (3.37). By setting V_L equal to zero, equations (3.36) to (3.37) can easily be evaluated for G_{m2} and G_{m3} , where G_m is once again extracted from conventional small-signal S-parameter measurements.

This section has demonstrated the direct extraction methodology of the nonlinear Taylor series coefficients for both the GaAs FET and GaN HEMTs device modelled in this work. The next section presents the extraction results.

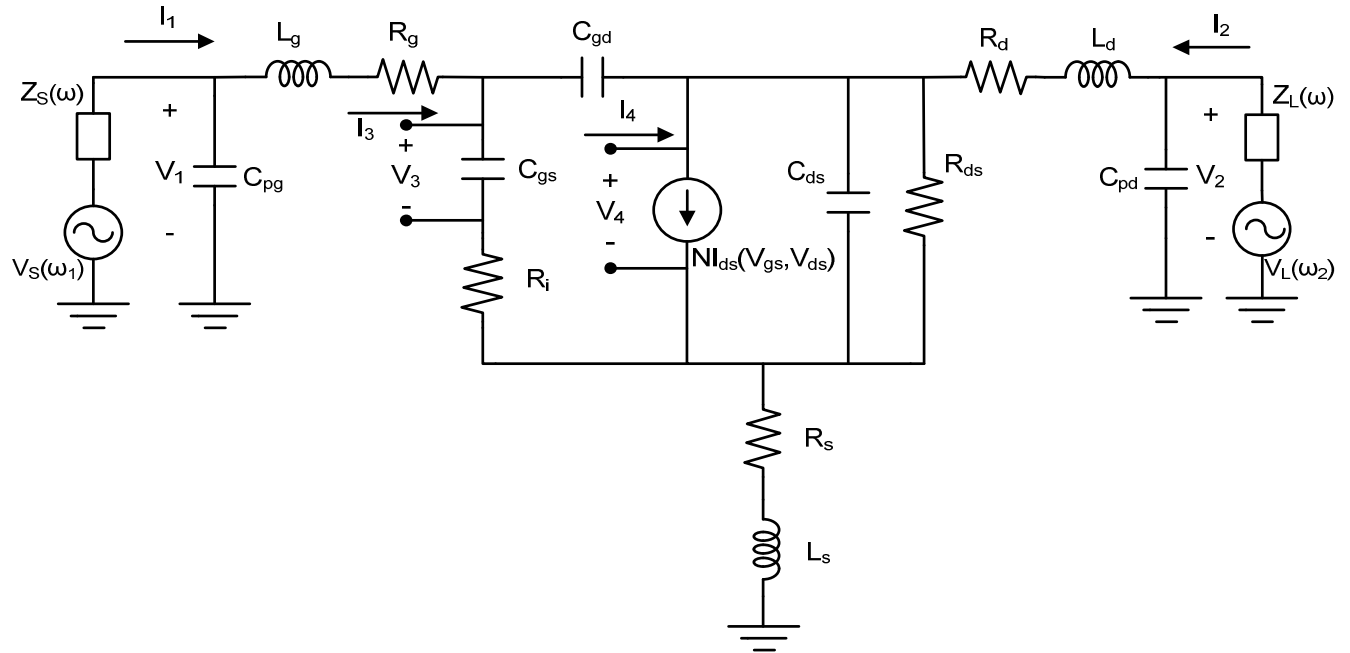


Figure 3.24 The equivalent circuit used for calculating the second and higher order distortion voltages and currents by applying the nonlinear currents method.

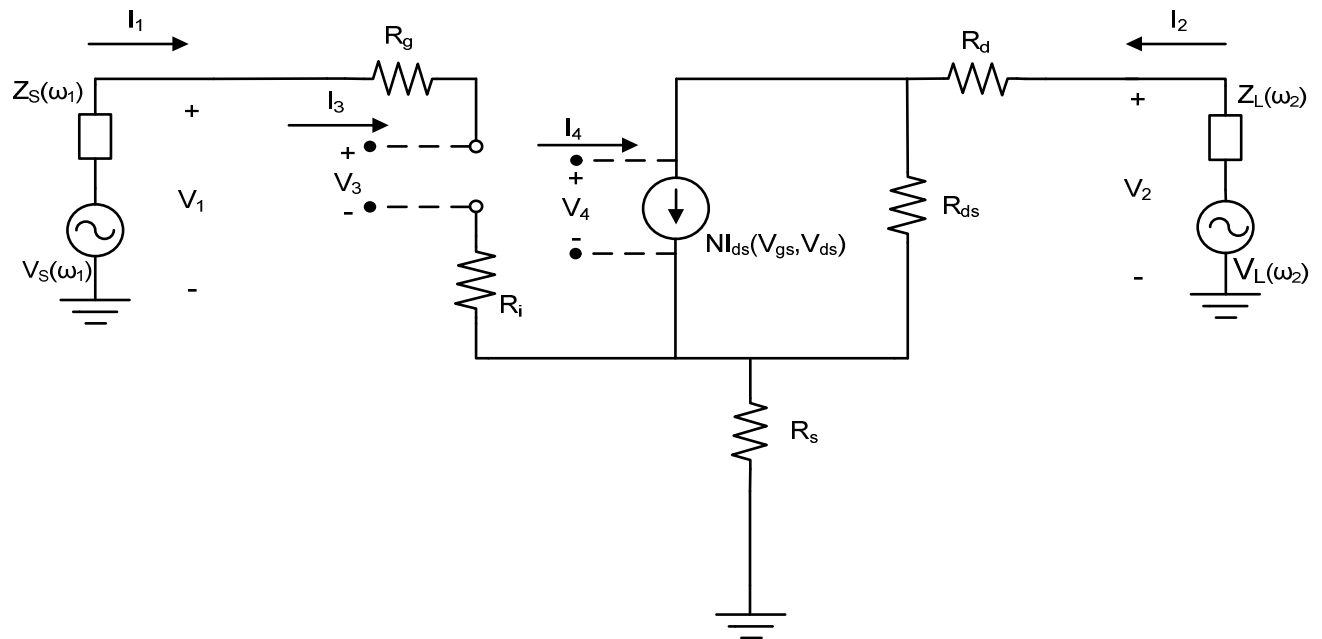


Figure 3.25 The simplified equivalent circuit valid for low frequency analysis.

$$\begin{bmatrix} \mathbf{I}_1 \\ \mathbf{I}_2 \\ \mathbf{I}_3 \\ \mathbf{I}_4 \end{bmatrix} = \begin{bmatrix} \mathbf{Y}_{11} & \mathbf{Y}_{12} & \mathbf{Y}_{13} & \mathbf{Y}_{14} \\ \mathbf{Y}_{21} & \mathbf{Y}_{22} & \mathbf{Y}_{23} & \mathbf{Y}_{24} \\ \mathbf{Y}_{31} & \mathbf{Y}_{32} & \mathbf{Y}_{33} & \mathbf{Y}_{34} \\ \mathbf{Y}_{41} & \mathbf{Y}_{42} & \mathbf{Y}_{43} & \mathbf{Y}_{44} \end{bmatrix} \times \begin{bmatrix} \mathbf{V}_1 \\ \mathbf{V}_2 \\ \mathbf{V}_3 \\ \mathbf{V}_4 \end{bmatrix} \quad (3.29)$$

$$\mathbf{V}_1 = \mathbf{V}_S - \mathbf{Z}_S \mathbf{I}_1 \quad (3.30)$$

$$\mathbf{V}_2 = \mathbf{V}_L - \mathbf{Z}_L \mathbf{I}_2 \quad (3.31)$$

$$\mathbf{I}_3 = 0 \quad (3.32)$$

$$\mathbf{I}_4 = -\mathbf{N} \mathbf{I}_{ds} \quad (3.33)$$

$$\mathbf{V}_3 = \mathbf{V}_{gs} = \mathbf{K}_{GS} \mathbf{V}_S + \mathbf{K}_{GL} \mathbf{V}_L + \mathbf{K}_{RG} \mathbf{N} \mathbf{I}_{ds} \quad (3.34)$$

$$\mathbf{V}_4 = \mathbf{V}_{ds} = \mathbf{K}_{DS} \mathbf{V}_S + \mathbf{K}_{DL} \mathbf{V}_L + \mathbf{K}_{RD} \mathbf{N} \mathbf{I}_{ds} \quad (3.35)$$

$$\begin{bmatrix} \mathbf{K}_{GS}^2 & & & \\ 2\mathbf{K}_{GS} \mathbf{K}_{GL} & \mathbf{K}_{GS} \cdot \mathbf{K}_{DS} & & \\ \mathbf{K}_{GL}^2 & (\mathbf{K}_{GS} \mathbf{K}_{DL} + \mathbf{K}_{GL} \mathbf{K}_{DS}) & \mathbf{K}_{DS}^2 & \\ & \mathbf{K}_{GL} \mathbf{K}_{DL} & 2\mathbf{K}_{DS} \mathbf{K}_{DL} & \mathbf{K}_{DL}^2 \end{bmatrix} \times \begin{bmatrix} \mathbf{G}_{m2} \\ \mathbf{G}_{md} \\ \mathbf{G}_{d2} \end{bmatrix} = \begin{bmatrix} \frac{2\mathbf{N} \mathbf{I}_{ds} (2\omega_1)}{|\mathbf{V}_S|^2} \\ \frac{2\mathbf{N} \mathbf{I}_{ds} (\omega_1 + \omega_2)}{|\mathbf{V}_S| |\mathbf{V}_L|} \\ \frac{2\mathbf{N} \mathbf{I}_{ds} (2\omega_2)}{|\mathbf{V}_L|^2} \end{bmatrix} \quad (3.36)$$

$$\begin{bmatrix}
K_{GS}^3 & K_{GS}^2 K_{DS} & K_{GS} K_{DS}^2 & K_{DS}^3 \\
3K_{GS}^2 K_{GL} & (K_{GS}^2 K_{DL} + 2K_{GS} K_{GL} K_{DS}) & (K_{GL} K_{DS}^2 + 2K_{GS} K_{DL} K_{DS}) & 3K_{DS}^2 K_{DL} \\
3K_{GL}^2 K_{GS} & (K_{GL}^2 K_{DS} + 2K_{GL} K_{GS} K_{DL}) & (K_{GS} K_{DL}^2 + 2K_{GL} K_{DL} K_{DS}) & 3K_{DL}^2 K_{DS} \\
K_{GL}^3 & K_{GL}^2 K_{DL} & K_{GL} K_{DL}^2 & K_{DL}^3
\end{bmatrix} \times
\begin{bmatrix}
4 \cdot \frac{NI_{ds}(3\omega_1) - NI_{ds23}(3\omega_1)}{|V_S|^3} \\
4 \cdot \frac{NI_{ds}(2\omega_1 + \omega_2) - NI_{ds23}(2\omega_1 + \omega_2)}{|V_S|^2 |V_L|} \\
4 \cdot \frac{NI_{ds}(\omega_1 + 2\omega_2) - NI_{ds23}(\omega_1 + 2\omega_2)}{|V_S| |V_L|^2} \\
4 \cdot \frac{NI_{ds}(3\omega_2) - NI_{ds23}(3\omega_2)}{|V_L|^3}
\end{bmatrix} \quad (3.37)$$

3.7 Extraction Results

During this author's exchange period in Belgium, some time was spent at the University of Aveiro in Portugal with Prof. J.C. Pedro, who has published many books and articles in the field of intermodulation distortion. The purpose of the visit was to gain measurement experience and spend time with an expert in this field of research. The main goal of the visit was to verify that the measurement setup designed in this thesis extracted the correct information. The verification was done by measuring a device, provided by the University of Aveiro, using the original system as presented in [6]. The same measurement was then repeated with the setup developed in this thesis. The result was that the two measurements were similar and the setup designed in this thesis was indeed fully functional. Thus the extracted coefficients presented in this thesis are accurate and can be used to construct the necessary models.

The IMD setup and extraction procedure was first tested on a CFY-30 GaAs FET measured at Stellenbosch University. The FET was measured using a test fixture system as shown in the previous section. These devices are low-power devices and as explained in section 3.3, are modelled with a two-dimensional Taylor series expanded around a DC bias voltage. Figure 3.26(a) to (c) shows the extracted second order coefficients, while Figure 3.27(a) to (c) shows the extracted third order coefficients. The output power measured for $P_{out}(3\omega_2)$ was of the order of -80dBm and thus the extracted G_{m3} was so small and noisy that no useful information can be gathered from this product. Hence it is not plotted in the graphs below. Figure 3.28(a) to (c) shows the result of typical values that can be expected for the GaN devices. The device measured was a two-finger T_{03} device with a gate width of 300 μ m. In chapter four the extracted Taylor

series coefficients are used to construct a nonlinear model, which predicts the linear and nonlinear behaviour of the device with excellent results.

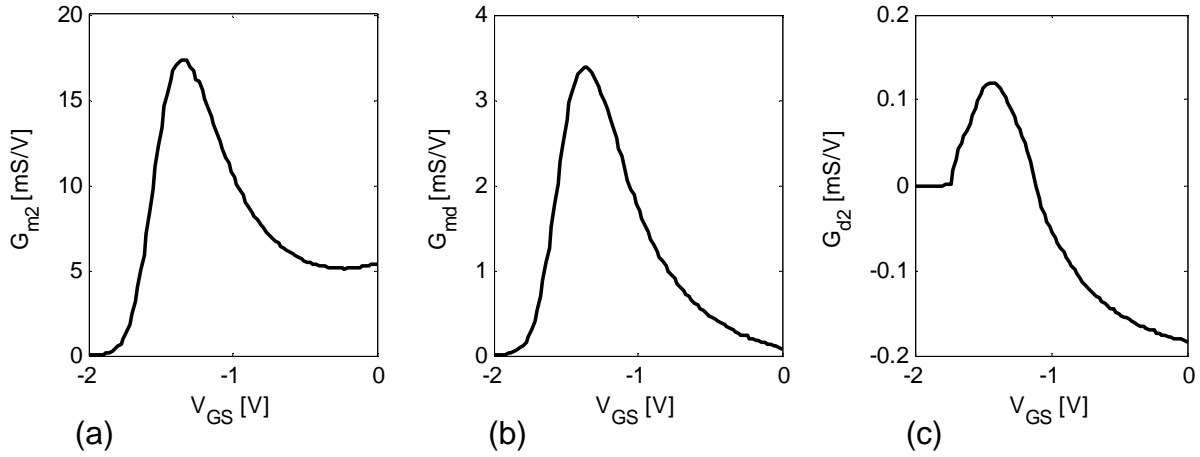


Figure 3.26 The typical second order extracted Taylor series coefficients for the CFY-30 GaAs FET, where (a) is G_{m2} , (b) G_{md} and (c) G_{d2} . The coefficients are extracted as a function of the gate voltage V_{GS} .

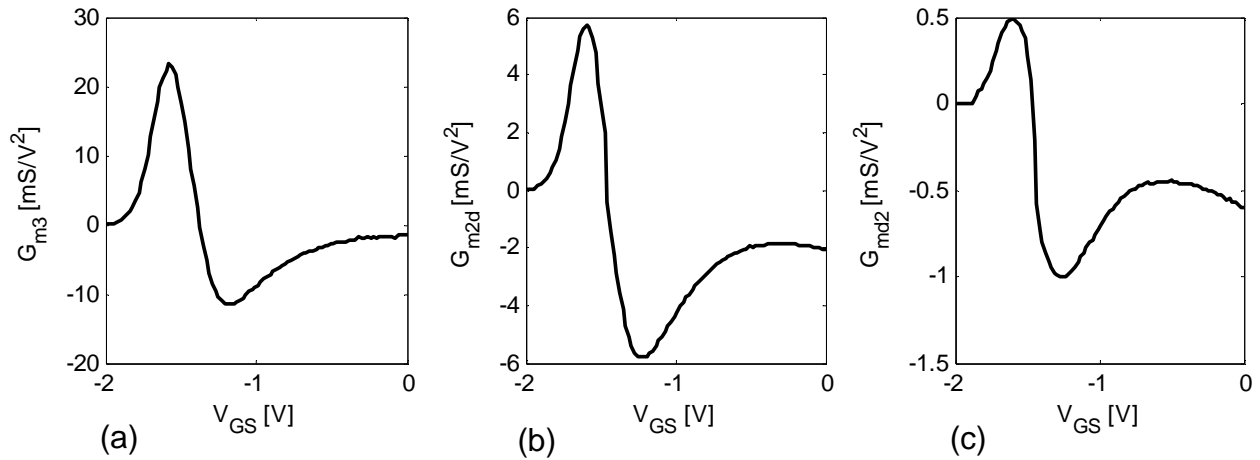


Figure 3.27 The typical third order extracted Taylor series coefficients for the CFY-30 GaAs FET, where (a) is G_{m3} , (b) G_{m2d} and (c) G_{md2} . The coefficients are extracted as a function of the gate voltage V_{GS} .

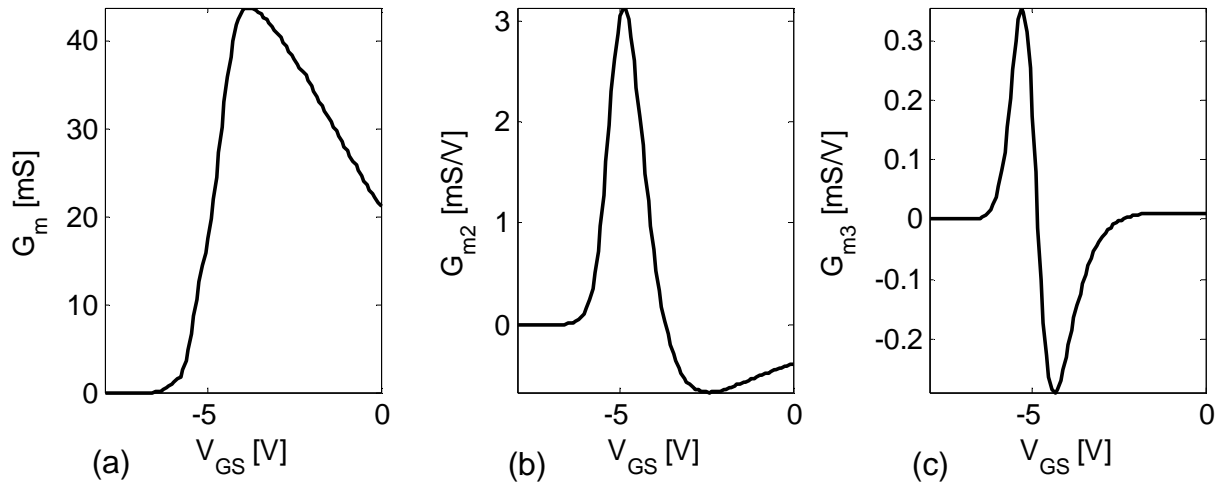


Figure 3.28 The typical first, second and third order extracted Taylor series coefficients for the GaN HEMT, where (a) is G_m extracted from S-parameter measurements, (b) the second order product G_{m2} and (c) the third order G_{m3} product. The output power products are measured as a function of the gate voltage V_{GS} .

3.8 Conclusion

The main goal of this chapter is to present the measurement setup used to extract the Taylor series coefficients of the nonlinear drain current source $I_{ds}(V_{gs}, V_{ds})$ directly from measurements. From the measurements, the higher order derivatives and cross-derivatives of I_{ds} with respect to V_{gs} and V_{ds} can be determined and are essential in the construction of nonlinear models that can accurately predict nonlinear IMD. The low-frequency IMD test system was successfully designed and implemented to extract nonlinear coefficients for two technologies, namely GaAs FETs and GaN HEMTs. The setup was firstly tested at the University of Stellenbosch on a GaAs FET device, which served as a basis to expand the measurement setup to measure on-wafer GaN HEMT devices at IMEC in Leuven, Belgium. In both cases, the nonlinear Taylor series coefficients were successfully extracted.

The extracted nonlinear coefficients of the drain current source $I_{ds}(V_{gs}, V_{ds})$ from this chapter are incorporated into the nonlinear model in chapter four and can be implemented in commercial CAD programs such as Microwave Office and Agilent's Advanced Design System (ADS).

CHAPTER 4

Nonlinear Model Formulation

4.1 Introduction

The goal of this chapter is to outline the basic structure of the equivalent circuit nonlinear model. The complete formulation and extraction procedure used for the on-wafer gallium nitride (GaN) high-electron mobility transistor (HEMT) devices is presented. The nonlinear model components and their functions will be discussed, as well as the problems associated with different model formulations. A few factors must be considered in the model formulation process.

Firstly, it is not guaranteed that nonlinear models linearise correctly, in other words, the small-signal data from which they were constructed is not accurately represented. The result would be clearly noticeable in the inability of the nonlinear models to accurately predict the linear S-parameters of the device. Another factor to consider is that table-based models may become inaccurate due to interpolation of “noisy” data. It is especially problematic for small signals that fall far between measured data points. The solution is to represent the data with an analytical function. With a function, the data is represented with a smooth curve, eliminating any noisy data points. A big advantage is that no interpolation is required. Finally, what is required to represent soft nonlinearities that give rise to intermodulation distortion (IMD) products? As mentioned in chapter three, derivatives cannot be extracted from DC as a result of errors associated with successive differential operations. It was demonstrated that it is almost impossible to determine small-signal nonlinearities for IMD predictions by differentiating the measured I/V characteristic. The conclusion is that any empirical model intended to predict very high signal-to-distortion ratios must be extracted from, or at least adjusted to, measured higher order AC data.

Before the nonlinear models are constructed, the modelling process should be fully understood. In section 4.2, an overview of the nonlinear modelling procedure is given. The section outlines the step-by-step modelling procedure from the first S-parameter measurements to the final nonlinear model implementation in Agilent’s Advanced Design System (ADS). The starting point of the modelling process is the determination of the linear small-signal equivalent circuit topology in section 4.3. The equivalent circuit parameters (ECPs) provide a lumped element approximation to various aspects of the physical device. Section 4.3.1 discusses the topology

used to model the GaN HEMT devices in this work. It is very important that the small-signal parameters are determined as accurately as possible, as these parameter values are used in the large-signal nonlinear model formulation. The extraction of the ECPs is performed with an optimisation-based extraction tool, programmed by Van Niekerk [18]. The extraction tool is discussed in section 4.3.2.

Once the small-signal equivalent circuit parameters have been extracted, the next step is to construct the nonlinear model. The nonlinear model transforms the large amount of extracted ECPs into a single set of parameters that can predict the linear and nonlinear behaviour of the device. The formulation of the nonlinear models from the ECP is discussed in section 4.4.1. In order to investigate the functions derived in section 4.4.1 a Matlab program is developed in section 4.5.1 that determines the table-based integration functions. With this program, any random integration starting point and integration path can be selected. The program is used in section 4.5.2 to investigate the result of selecting different integration starting points. By comparing the results of the model predictions, the optimal starting point is selected. In section 4.5.3 the two models deduced in section 4.4.1, namely the Root and modified Root are investigated. The next step in the process is representing the drain current source I_{dsi} with an analytical function, detailed in section 4.5.4. The function used is known as the Fager model and a Matlab program is used to optimise the model parameters. The Fager model is expanded in section 4.5.5 to include the extracted derivative information from chapter three. With the results of the investigation and the addition of the analytical drain current function, a nonlinear model is proposed that improves the accuracy of the S-parameter, large-signal single-tone and large-signal two-tone IMD predictions.

4.2 Nonlinear Modelling Procedure

This section gives an overview of the nonlinear model construction procedure, from the first measurements to the final model. The procedure can be summarised in a flow diagram, as shown in Figure 4.1 [12].

The first step is to measure the S-parameters on the vector network analyser (VNA) over the required voltage bias range. From these measurements, the small-signal equivalent circuit parameters are extracted for each bias point, described in section 4.3. Then, by integration, the constitutive relations are constructed using the method that will be explained in section 4.4. The constitutive relations are then implemented into Agilent's Advanced Design System (ADS), either in table-based format or as analytical functions. The final step is to verify the models by comparing the model predictions to the measurements from the VNA and LSNA. The proposed nonlinear model's small-signal predictions are verified against measured S-parameters from the

VNA. The nonlinear large-signal predictions are verified by comparing the model predictions to the measured large-signal single-tone and two-tone measurements performed on the LSNA. Comparing the results of the measured and predicted values, it is possible to determine the accuracy of the models. The following section describes the small-signal equivalent circuit topology and the optimisation-based tool for the extraction of the ECP.

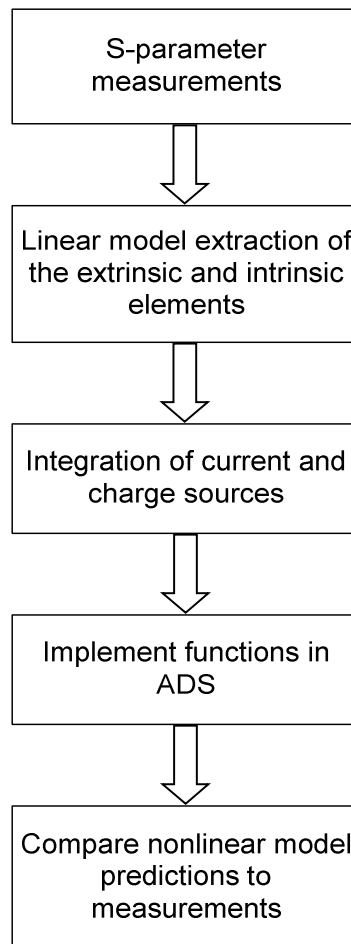


Figure 4.1 Flow diagram of the nonlinear modelling procedure.

4.3 Linear Modelling

Linear models describe the linear behaviour of a device and in some cases can also be applied to evaluate nonlinear networks if the operating signals are sufficiently small. The model used to characterise the device's behaviour under the small-signal approximation is the equivalent circuit model. In practice, this is the most widely used linear model [12], [13], [14], [16], as it produces

highly accurate model predictions and thus will be used as basis for the linear modelling process in this thesis.

4.3.1 Small-Signal Equivalent Circuit Model

The elements in the equivalent circuit provide a lumped element approximation to some aspect of the physical device. The model provides a link between the measured DC, S-parameters and the electronic process occurring within the device. An advantage of this approach is that once the circuit parameters have been determined, then the model can be used to extrapolate the small-signal behaviour beyond the available capabilities of the measurement setups. It is very important that the small-signal parameters are determined as accurately as possible, as these parameter values are used in the large-signal nonlinear model formulation. The first step in the linear modelling process is to choose the correct model topology that would be able to describe the response of the device over a wide range of bias and frequency points. To obtain insight into the construction of the model and a physical meaning of the circuit parameters, it is necessary to evaluate a cross section of a HEMT, as shown in Figure 4.2. The standard two-dimensional representation format used in circuit analysis is shown in Figure 4.3. The small-signal equivalent circuit model can be divided into an extrinsic and intrinsic part as seen in Figure 4.3. The bias-dependant intrinsic elements are located inside the dashed box in Figure 4.2 and Figure 4.3, while the bias-independent extrinsic elements are all the elements outside the dashed box.

The extrinsic part consists of parasitic elements that are related to the geometry of the device. The parasitic capacitance C_{pg} represents the capacitance between the gate and the source, while C_{pd} is the parasitic capacitance between the drain and the source. C_{pgd} represents the parasitic capacitance between the gate and the drain. In modelling terms, it is difficult to independently determine C_{gd} and C_{pgd} of on-wafer devices, and thus C_{pgd} is incorporated into C_{gd} . The parasitic inductance L_g , L_s and L_d are associated to the metal contact pads. The extrinsic gate resistance is due to the gate Schottky contact, while the drain and source resistances are due to their ohmic contacts. The resistances R_{gsf} and R_{gdf} represent the leakage current through the gate-source and gate-drain Schottky diodes, and for the purpose of this work are neglected, as the values do not have a significant influence on this topology.

The intrinsic part can be divided into four sections, an input section consisting of a series RC network (C_{gs} , R_{gs}), a feedback series RC network (C_{gd} , R_{gd}), a voltage-controlled current source ($G_m e^{-j\omega\tau}$) and a parallel RC network (C_{ds} , R_{ds}) at the output of the intrinsic plane. The capacitances C_{gs} and C_{gd} model the change in the depletion region under the gate with respect to V_{gs} and V_{gd} respectively. R_{gs} and R_{gd} model the charging resistances in the channel and are tied to the time that it takes for charge in the channel to redistribute. C_{ds} models the geometric capacitance effects between the source and drain electrodes. The intrinsic gain mechanism is

provided by transconductance g_m , which represents the measure of incremental change in output current I_{ds} for a change in input voltage V_{gs} . The output conductance g_{ds} is a measure of incremental change in output current I_{ds} with change in output voltage V_{ds} . The two terms can be mathematically defined as $G_m = \partial I_{ds} / \partial V_{gs}$ and $G_{ds} = \partial I_{ds} / \partial V_{ds}$ respectively. The transconductance cannot change instantaneously with a change with input voltage V_{gs} and thus the parameter τ represents the transconductance delay. The delay τ represents the time associated with the redistribution of charge after a fluctuation of the gate voltage V_{gs} . The next section describes the extraction tool programmed by Van Niekerk [18] which was used to perform the extraction of the ECP in this work.

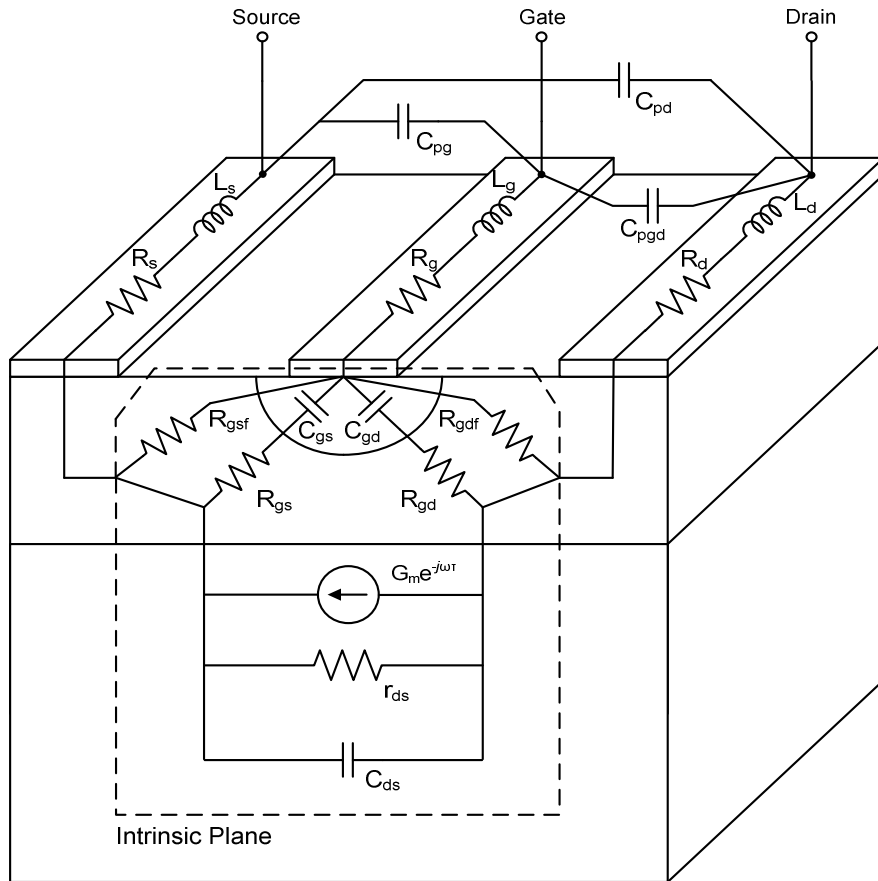


Figure 4.2 The physical origin of the small-signal equivalent circuit parameters of a HEMT device.

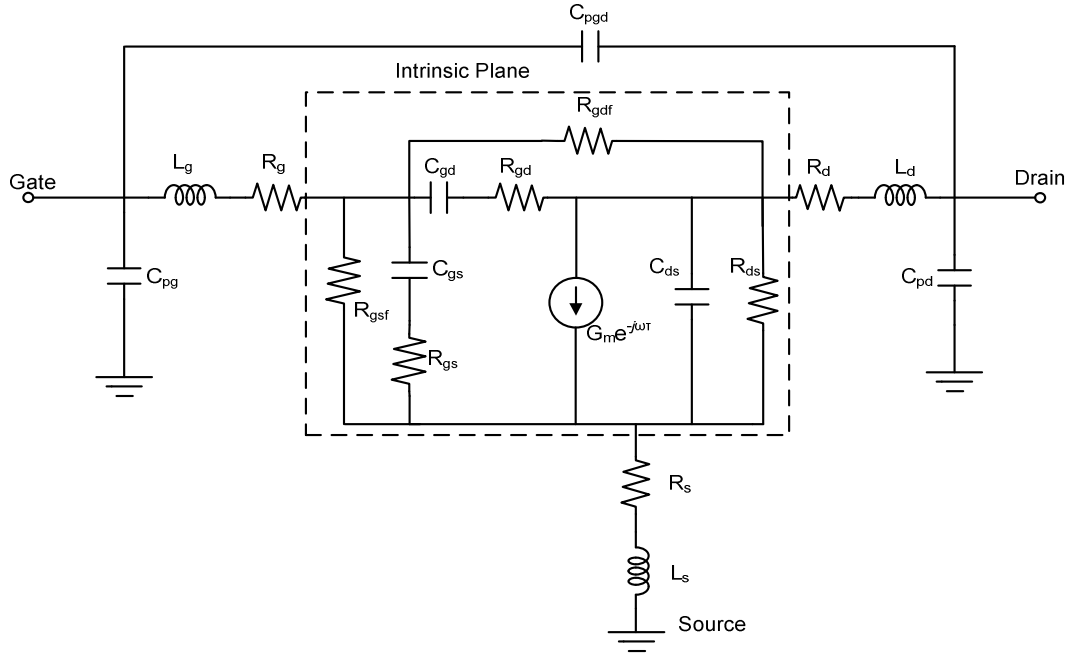


Figure 4.3 The small-signal equivalent circuit topology used to model an on-wafer GaN HEMT.

4.3.2 Extrinsic and Intrinsic Parameter Extraction

Extraction methods of the bias-independent extrinsic and bias-dependant intrinsic elements are well documented in literature and will not be discussed in great detail, as it is not the main focus of this thesis, so for further detail refer to [33] to [46]. The extraction of the ECP in this work is performed using an extraction software tool called PCFETGUI programmed by Van Niekerk [18]. The purpose of PCFETGUI is to create a user-friendly extraction tool, which can be used to accurately and efficiently extract the ECP for a number of circuit topologies.

Before the extraction procedure can begin, the selection of a number of S-parameter bias points must be considered at which the extraction process will take place. Only a few points are required to perform the optimisation-based extraction. If a large number of S-parameters are used the extraction time increases significantly without improving the accuracy. A good selection of bias points strongly improves the ability of the optimisation extraction algorithms to converge. There are two types of points that must be selected, cold and hot bias points. Cold bias points are defined as points where V_{ds} is kept at 0V and V_{gs} is below the pinch-off voltage, while hot bias points are defined as the points where the device is switched on. In the cold condition, the intrinsic part of the small-signal equivalent circuit in Figure 4.3 is reduced to only the three intrinsic capacitors C_{gs} , C_{gd} and C_{ds} [12], [22].

With the selection of the hot bias points, PCFETGUI implements four filter parameters that allow the user to specify a region in which S-parameter selection can take place, as seen in Figure 4.4(a). However, there are still too many points selected to perform an optimisation-based parameter extraction. The optimal extraction set should only consist of about five cold bias points and ten hot bias points. The advantage of using PCFETGUI is that the selection algorithm automatically scans through the list of bias points available and selects the optimal S-parameters measured under cold and hot bias conditions, referred to as intelligent bias point selection [22]. In this method, bias points are selected by evaluating the S-parameters of each point. The points for which the S-parameters indicate the widest spread are selected. This ensures that the maximum amount of information can be extracted from the small set of selected S-parameters and also improves the ability of the extraction algorithm to converge. The result of the intelligent bias point selection is shown in Figure 4.4(b). Once the cold and hot bias points have been selected, the extraction of the extrinsic and intrinsic parameters can begin.

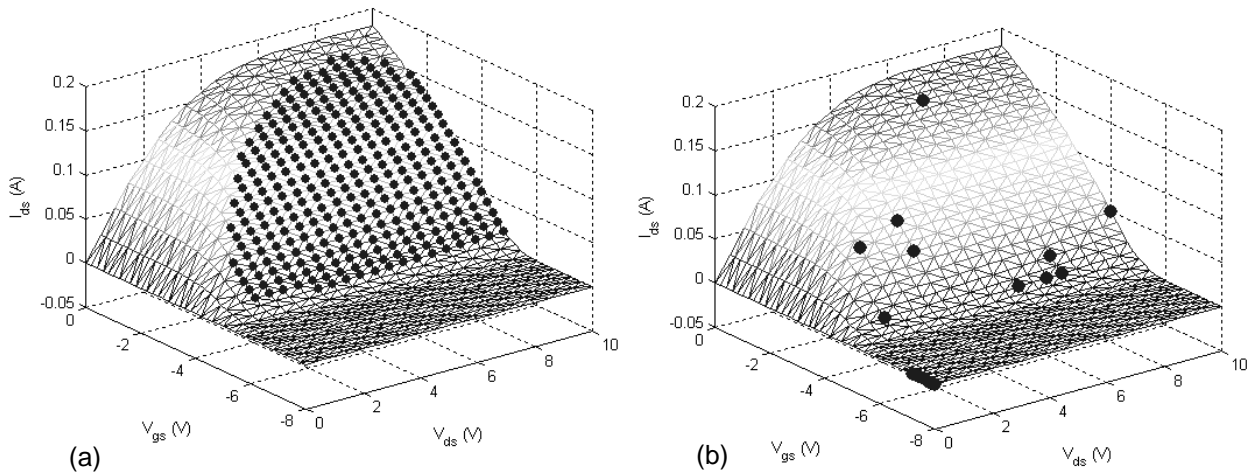


Figure 4.4 (a) The result of applying the user-defined filters to a complete set of extracted bias points, while in (b) the intelligent bias point selection reduces the data set to an optimal of five cold and ten hot bias points.

The first step in the PCFETGUI optimisation procedure is to determine the starting values of the ECP, using direct extraction techniques. From the starting values, a minimum and maximum limit is assigned to the element parameters. This limit is the range in which the optimiser searches for a final value. It is possible to manually change the minimum and maximum limit of the search function, depending on the individual element. After the limits have been determined, PCFETGUI implements a robust multi-bias optimisation-based parameter extraction [22], [23], [24], [25] technique to compute the values of the ECP. The advantage of the extraction algorithm is that it is robust in the sense that it is independent of parameter starting values. However, as mentioned above, starting values have been determined that are already close to the final values,

which increases the chance of the optimiser converging. The result of the extracted extrinsic parameters using PCFETGUI for the T_{03} device topology is presented in Table 4.1.

After the optimised extrinsic parameters have been determined, all the measured S-parameters can be used to extract the intrinsic small-signal model parameters. The intrinsic elements are determined through direct extraction techniques [25] and calculated using the equations proposed in [32]. The modelled intrinsic parameter values are fitted to the measured values by implementing a Gauss-Newton optimiser. The calculated values are already close to the optimal values and thus the optimisation is not too time-consuming. PCFETGUI has a feature where the optimised parameters can be compared to the directly extracted parameters. By comparing the two results, it is possible to determine the accuracy of the directly extracted parameters. PCFETGUI does not determine the value of R_{gd} . R_{gd} was calculated using equation (4.1). The result of the intrinsic parameter extraction for a T_{03} device is shown in Figure 4.5(a) to (h). The next section details the nonlinear model formulation using the equivalent circuit parameters extracted in this section.

$$R_{gd} = -\text{Re}\left(\frac{1}{Y_{12}}\right) \quad (4.1)$$

Extrinsic Parameter	Value
R_g	7.63 Ω
L_g	65.6nH
R_s	1.64 Ω
L_s	4.46nH
R_d	2.47 Ω
L_d	47.94nH
C_{pg}	46fF
C_{pd}	32fF

Table 4.1 Extracted extrinsic parameters of the on-wafer GaN HEMT T_{03} device.

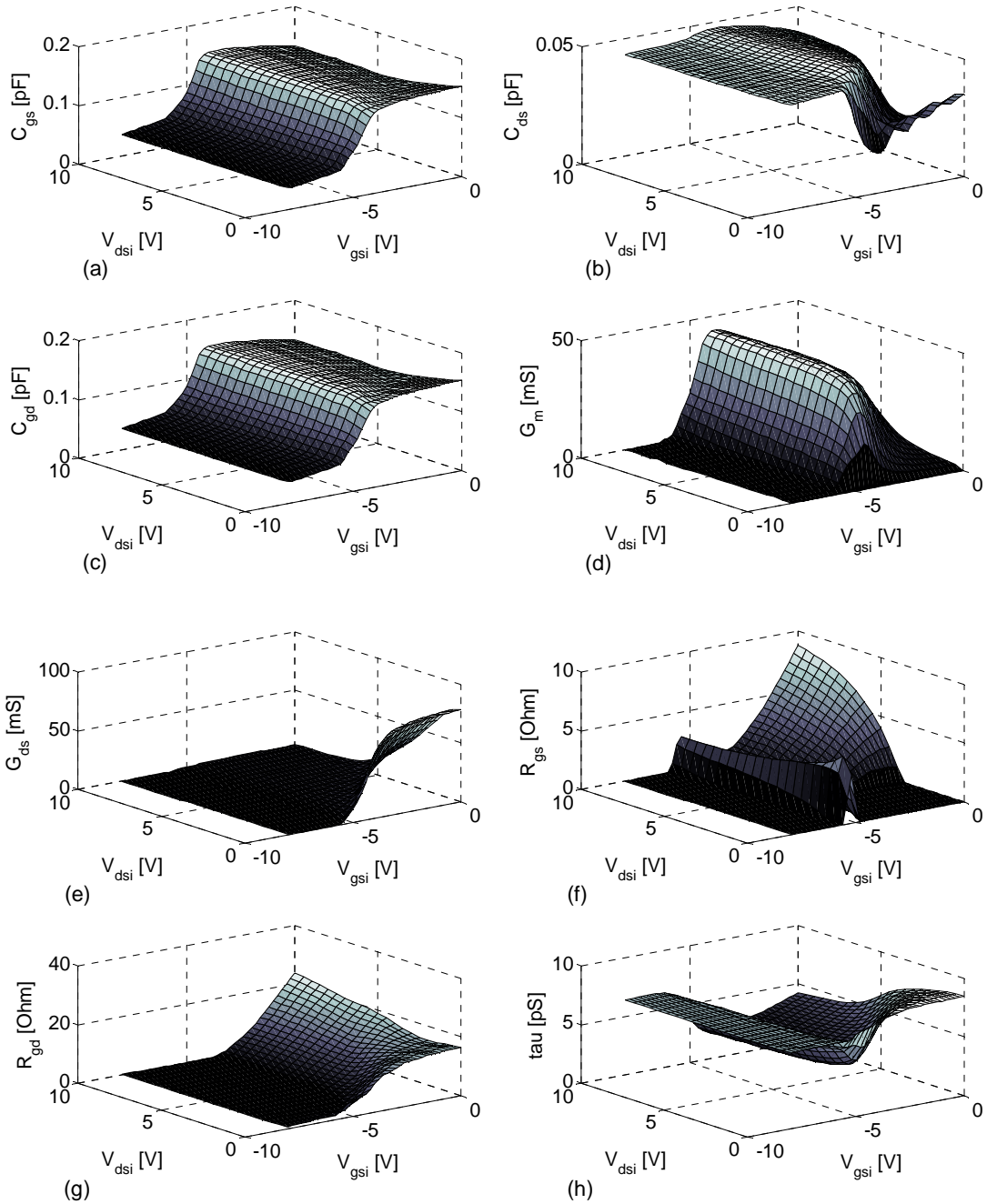


Figure 4.5 The plots of the extracted bias-dependant intrinsic elements of the T₀₃ device, where (a) is C_{gs} , (b) C_{ds} , (c) C_{gd} , (d) G_m , (e) G_{ds} , (f) R_i , (g) R_{gd} and (h) tau versus the intrinsic gate V_{gsi} and drain V_{dsi} voltages.

4.4 Nonlinear Modelling

Nonlinear models predict the behaviour of a device under large-signal excitation levels, which make them ideal for modelling GaN HEMT power devices. In the previous section, the small-signal equivalent parameter set was extracted over a predefined bias range. Nonlinear models transform the large amount of extracted small-signal parameters into a single set of parameters and not only predict the DC behaviour of the device, but also the behaviour under various input power levels.

4.4.1 Nonlinear Model Formulation

The nonlinear model is deduced from the linear small-signal equivalent circuit model, which is extracted at the desired gate and drain bias points. As mentioned, the equivalent circuit can be divided into the bias-independent extrinsic elements and the bias-dependent intrinsic elements. The nonlinear model is formulated with respect to the intrinsic device plane as defined by the dashed box in Figure 4.3. After the parameter extraction of the ECP is performed, the first step is to de-embed extrinsic elements from the measured S-parameters, so that the constitutive relations can be determined at the intrinsic device plane. The de-embedding procedure is summarised in the following steps [21].

Firstly, the external S-parameters of the device are measured and converted to Y-parameters. The parasitic capacitances C_{pg} and C_{pd} are de-embedded from the Y-parameters, which are then converted to Z-parameters. The series elements L_g , R_g at the gate terminal, L_s , R_s at the source terminal and L_d , R_d at the drain terminal are subtracted from the Z-parameters in the previous step. The de-embedded Z-parameters are then converted back to Y-parameters, which are now referenced at the intrinsic device plane as seen in Figure 4.3. These intrinsic Y-parameters will be used in the deduction of the nonlinear model.

The procedure above described the translation of the S-parameters at the extrinsic device plane to Y-parameters, at the intrinsic device plane. The next step is to shift the extrinsic bias voltages (V_{gs} , V_{ds}) to the intrinsic device plane (V_{gsi} , V_{dsi}). This is done to accurately determine the intrinsic charge and current functions, as the functions are dependent on the intrinsic bias voltages (V_{gsi} , V_{dsi}). To shift the bias plane, a correction has to be made that takes into account the voltage drop over the DC cables used to bias the device and the extrinsic series resistances. The effects of the voltage drops are that the intrinsic voltages V_{gsi} and V_{dsi} do not form an equidistant grid. A uniform voltage grid is generally required for the implementation of table-based models in commercial nonlinear circuit simulators. The extrinsic voltage grid (V_{gs}, V_{ds}) is

shifted to the intrinsic bias plane (V_{gsi} , V_{dsi}) by means of Kirchoff's voltage and current laws. The intrinsic gate V_{gsi} and drain voltages V_{dsi} are given in equations (4.2) and (4.3) [12].

$$V_{dsi} = V_{ds} - (R_{dc2} + R_d + R_s)I_{ds} - R_s I_{gs} \quad (4.2)$$

$$V_{gsi} = V_{gs} - (R_{dc1} + R_g + R_s)I_{gs} - R_s I_{ds} \quad (4.3)$$

R_{dc1} and R_{dc2} represent the resistances of the gate and drain bias lines respectively and each has a resistance of about 1.5Ω . Once the bias plane is shifted to the intrinsic plane (V_{gsi} , V_{dsi}) and the intrinsic Y-parameters have been determined, the deduction of the nonlinear current and charge sources can begin. Assuming that the resistance R_{gs} and R_{gd} in Figure 4.3 can be neglected and there is no frequency dispersion, the two-port intrinsic small-signal equivalent circuit can be presented in a Y-matrix, as expressed in equation (4.4) [12]. The conductances G_{gsf} and G_{gdf} are the inverse of the resistances R_{gsf} and R_{gdf} . As mentioned in section 4.3.1, these resistances are neglected, which means that G_{gsf} and G_{gdf} can be set to zero in the calculations that follow.

$$Y = \begin{bmatrix} G_{gsf} + G_{gdf} + j\omega(C_{gs} + C_{gd}) & G_{gdf} + j\omega C_{gd} \\ G_m - G_{gdf} - j\omega C_{gd} & g_{ds} + G_{gdf} + j\omega(C_{ds} + C_{gd}) \end{bmatrix} \quad (4.4)$$

The real parts of the Y-parameters are frequency independent, while the imaginary parts are frequency dependent. By definition, the small-signal equivalent scheme is consistent with the nonlinear model, provided that the corresponding nonlinear characteristics at gate and drain port can be obtained by the path-independent contour integrals [12]. The port current and charge functions are given by equations (4.5) and (4.6), where port i equal to 1 represents the gate and port i equal to 2 represents the drain. V_1 , V_2 are the instantaneous voltages at the gate and drain ports and V_{10} , V_{20} the starting point of the integration functions.

$$I_i(V_1, V_2) = I_i(V_{10}, V_{20}) + \int_{V_{10}}^{V_1} \text{Re}\{Y_{i1}(V, V_{20})\}dV + \int_{V_{20}}^{V_2} \text{Re}\{Y_{i2}(V_1, V)\}dV \quad (4.5)$$

$$Q_i(V_1, V_2) = \int_{V_{10}}^{V_1} \frac{\text{Im}\{Y_{i1}(V, V_{20})\}}{2\pi f} dV + \int_{V_{20}}^{V_2} \frac{\text{Im}\{Y_{i2}(V_1, V)\}}{2\pi f} dV \quad (4.6)$$

The requirement of path-independent integrals is equivalent to the special conditions that are imposed on Y_{ij} with i, j equal to 1 or 2 called the integrability conditions [29], [30], [31]. Root has shown that the integrability conditions are approximately satisfied for MESFETs and

HEMTs [29]. Port charges must therefore be constructed via path-independent integration so that only one value for charge exists for each combination of V_{gsi} and V_{dsi} , [16]. Charge conservation therefore requires that a charge source behaves periodically over a period of simulation, and if it is not satisfied, the model will show a non-physical gain in energy for each period of simulation. This can cause the simulation to crash or produce incorrect results [13]. The following section presents the formulation of the current and charge functions.

The four constitutive relations that describe the nonlinear model can be determined from the integration of the bias-dependent intrinsic circuit parameters with respect to the intrinsic gate and drain voltages and are given in the following four equations (4.7) to (4.10) [12].

$$I_{gsi}(V_{gsi}, V_{dsi}) = I_{gs}(V_{gsi0}, V_{dsi0}) + \int_{V_{gs0}}^{V_{gsi}} [G_{gsf}(V, V_{dsi0}) + G_{gdf}(V, V_{dsi0})]dV - \int_{V_{ds0}}^{V_{dsi}} G_{gdf}(V_{gsi}, V)dV \quad (4.7)$$

$$Q_{gsi}(V_{gsi}, V_{dsi}) = \int_{V_{gs0}}^{V_{gsi}} [C_{gs}(V, V_{dsi0}) + C_{gd}(V, V_{dsi0})]dV - \int_{V_{ds0}}^{V_{dsi}} C_{gd}(V_{gsi}, V)dV \quad (4.8)$$

$$I_{dsi}(V_{gsi}, V_{dsi}) = I_{ds}(V_{gsi0}, V_{dsi0}) + \int_{V_{gs0}}^{V_{gsi}} [g_m(V, V_{dsi0}) - G_{gdf}(V, V_{dsi0})]dV + \int_{V_{ds0}}^{V_{dsi}} [g_{ds}(V_{gsi}, V)dV + G_{gdf}(V_{gsi}, V)]dV \quad (4.9)$$

$$Q_{dsi}(V_{gsi}, V_{dsi}) = \int_{V_{ds0}}^{V_{dsi}} [C_{gd}(V_{gsi}, V) + C_{ds}(V_{gsi}, V)]dV - \int_{V_{gs0}}^{V_{gsi}} C_{gd}(V, V_{dsi0})dV \quad (4.10)$$

From equations (4.7) to (4.10) it can be shown that the nonlinear model of an HEMT device consists of a parallel connection of a charge and current source at the gate and at the drain, as seen in Figure 4.6, which is referred to as the Root model. This nonlinear model is quasi-static because the constitutive relations change instantaneously with varying terminal voltages. The constitutive relations are generally presented in an analytical functions [49] to [51] or in a table-based format [47], [48], [52] to [54]. The final model presented in section 4.5.3 is a combination of the two representations.

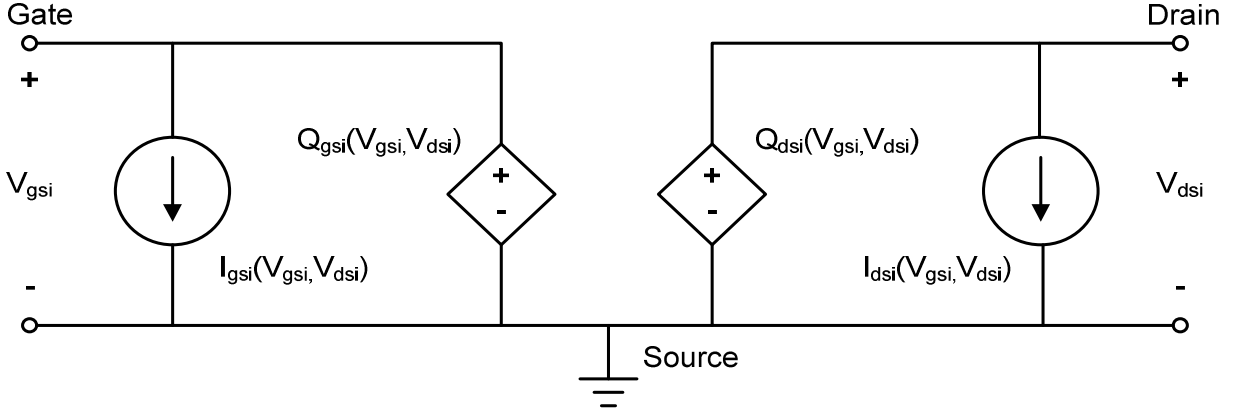


Figure 4.6 The intrinsic quasi-static nonlinear HEMT model, referred to as the Root model.

The Root model can be extended to include the resistances R_{gs} and R_{gd} in the nonlinear model. The addition of the resistances leads to a modified intrinsic small-signal equivalent circuit shown in Figure 4.7 and is known as the modified Root model [12].

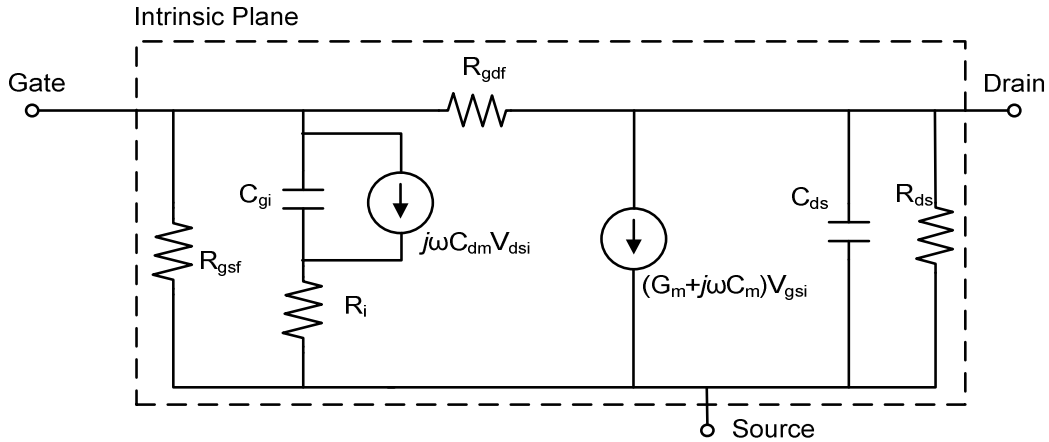


Figure 4.7 The intrinsic small-signal equivalent circuit of the modified Root model is shown.

The calculations of the intrinsic elements corresponding to the modified small-signal equivalent scheme, is presented in [12], [55]. Employing the new component names of the modified small-signal equivalent scheme results in equations (4.8) and (4.10) changing to equations (4.11) and (4.12) respectively.

$$Q_{gs}(V_{gsi}, V_{dsi}) = \int_{V_{gsi0}}^{V_{gsi}} C_{gi}(V, V_{dsi0}) + \int_{V_{dsi0}}^{V_{dsi}} G_{dm}(V_{gsi}, V)dV \quad (4.11)$$

$$Q_{ds}(V_{gsi}, V_{dsi}) = \int_{V_{gsi0}}^{V_{gsi}} C_m(V, V_{dsi0}) + \int_{V_{dsi0}}^{V_{dsi}} C_{ds}(V_{gsi}, V) dV \quad (4.12)$$

The corresponding nonlinear intrinsic model is shown in Figure 4.8, with the addition of a nonlinear charging resistor R_i at the gate port of the model. R_i is dependent on the bias voltages (V_{gsi}, V_{dsi}) and is calculated using equations (4.13). This charging resistor leads to the model now becoming non quasi-static.

$$R_i = \text{Re} \left(\frac{1}{Y_{11}} \right) \quad (4.13)$$

As mentioned, the constitutive relations of the Root or modified Root models are implemented in a nonlinear design package, either as table-based or analytical models. In table-based models, the relations are tabulated as a function of the terminal voltages, and during simulation the tables are accessed and the interpolated values are returned. The advantage of table-based models is that the models can be straightforwardly implemented without an optimisation process. Analytical models offer the advantage of being represented by a limited number of parameters. These models need some form of optimisation to fit the parameter set of the specified function. The main advantage of these models is the fact that the functions can be extrapolated, as the function is not limited to the extracted grid and the analytical models also have a shorter simulation time.

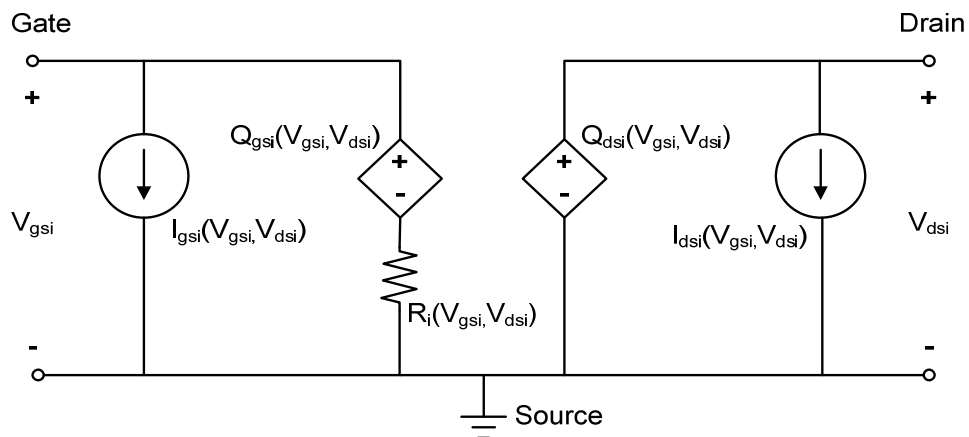


Figure 4.8 The modified Root nonlinear model with a charging resistance R_i .

The following section describes a Matlab program that was developed to determine the constitutive relations in table-based format, while in section 4.4.3, another Matlab program is presented that performs the optimisation process for the analytical drain current source I_{dsi} function.

4.5 Nonlinear Model Investigation and Construction

This section details the methodology behind the construction of the proposed GaN HEMT nonlinear model. Investigations into some key aspects of the nonlinear model will be presented, which will provide the basis of reasoning behind the final model construction. To illustrate the model construction, only a single bias point is selected, at which the devices would typically operate. The bias point selected is for class-A operation, where V_{GS} is equal to -4V and V_{DS} is equal to 8V. At this point, the device has a maximum gain. The T₀₃ device is selected to demonstrate the nonlinear model construction, as it is the intermediate device with respect to gate size, which is directly proportional to the output current I_{ds} . Only a single bias point is selected, as the goal of this section is only to demonstrate the methodology behind the model construction. In chapter five the performance of the models are evaluated over a wide range of bias points.

4.5.1 Construction of Table-Based Integration Function

In order to fully investigate the nonlinear charge and current functions derived in section 4.4.1, a Matlab program was developed that can integrate the functions from any randomly selected starting point (V_{gs0} , V_{ds0}). With the Matlab program, it is also possible to select the integration paths, thus either starting the integration with respect to the x-direction (V_{gsi}) and then the y-direction (V_{dsi}), or first with respect to the y-direction (V_{dsi}) and then the x-direction (V_{gsi}). The program calculates the integration functions for both the Root and modified Root models and saves the data in a CITI file format, which can be directly imported into ADS.

Before the functions can be calculated, it should be noted that the integration functions cannot be directly determined from the extracted equivalent circuit parameters because of the voltage drop over the DC cables and parasitic elements. The extrinsic elements must first be de-embedded so that the voltage plane is shifted to the intrinsic plane. After the de-embedding, the intrinsic voltage plane is non-uniform, as shown in Figure 4.9, which cannot be implemented in a nonlinear simulator package. Thus, an extrapolation technique must be used that ensures that after the de-embedding process, the intrinsic planes are still uniform. The de-embedding procedure is automatically executed in the Matlab program using the following procedure.

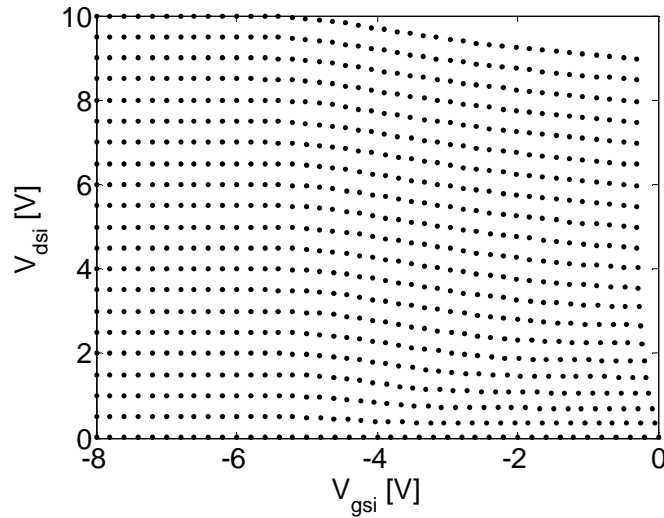


Figure 4.9 The plots of the intrinsic gate V_{gsi} versus drain V_{dsi} voltages are non-uniform as a result of the de-embedding process.

Firstly, the original extrinsic voltage planes boundaries (V_{gs} , V_{ds}) are shifted by linear extrapolation. If the extrinsic boundaries (V_{gs} , V_{ds}) are not extrapolated before the de-embedding process, the result is that after the de-embedding, the intrinsic plane (V_{gsi} , V_{dsi}) is mapped onto a smaller and non-uniform grid, as seen in Figure 4.9. The amount the planes are shifted is directly related to the values of the parasitic resistors. Equations (4.2) and (4.3) are used to determine the new intrinsic voltage plane. The result is that the original plane is widened so that when the intrinsic planes are shifted, the nonlinear functions will fall within the original voltage grid. Once the extrinsic elements are de-embedded and the intrinsic voltage plane (V_{gsi} , V_{dsi}) mapped, the nonlinear integration functions can be determined. The nonlinear Root model equations (4.7) to (4.10) and modified Root model equations (4.11) to (4.13) are implemented in Matlab. The T_{03} device topology is selected to demonstrate a typical set of extracted function using the Matlab procedure, shown in Figure 4.10(a) to (d). These functions can now be imported into ADS for nonlinear model simulation. As mentioned, the devices measured have no significant gate leakage and thus I_{gsi} is equal to zero as seen in Figure 4.10(b).

The functions shown in Figure 4.10(a) to (d) are implemented in a table-based format and in section 4.5.4 an analytical function is implemented to fit the drain current source model I_{dsi} . Only the drain current source is implemented as an analytical function as it is the most dominant nonlinearity in the nonlinear model. In the next section, the result of selecting different integration starting is investigated.

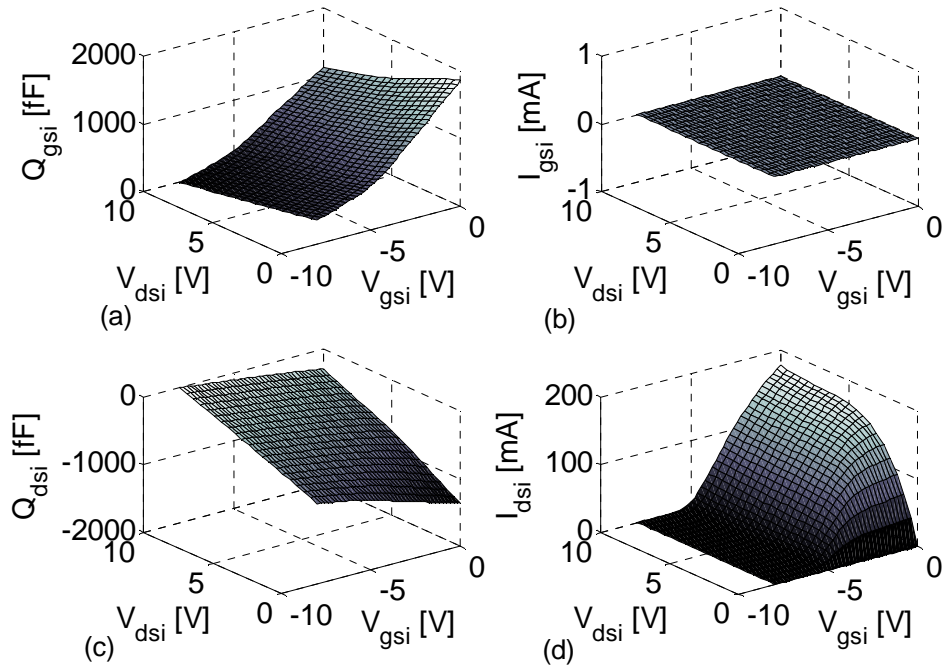


Figure 4.10 The table-based nonlinear functions extracted for the T_{03} device, where (a) is the gate charge Q_{gsi} , (b) the gate current I_{gsi} , (c) the drain charge Q_{dsi} and (d) the drain current I_{dsi} function.

4.5.2 Investigation of the Integration Starting Points

The most important consideration with regard to the integration functions is the choice of the starting point (V_{gs0}, V_{ds0}) for the integrals. To investigate the integration functions, a Matlab program was developed in section 4.5.1, which allows any random starting point and integration path to be chosen. Using this Matlab program, the constitutive relations can be constructed from any desired starting point (V_{gs0}, V_{ds0}) and directly imported into ADS for simulation. The Matlab program can also be used to verify whether the integrability conditions are fulfilled. The way the integrability conditions are verified is by comparing the difference between the plots taken at the same integration starting point, but integrated in different directions. By evaluating the error associated with the integration process, it is possible to determine the best starting point for the integration. The biasing values in Table 4.1 were selected as starting points to construct the current and charge functions.

	V_{gs0}	V_{ds0}
1.	0V	0V
2.	-8V	0V
3.	-8V	10V
4.	0V	10V

Table 4.1 Table of integration starting points

In Figure 4.11 to Figure 4.14 the absolute difference in error between the different integration paths for the starting points in Table 4.1 are presented. These are the corner bias points over which the device is characterised. More points were evaluated in the investigation, but will not be shown in order to avoid unnecessary plots that do not add extra information. When analysing Figure 4.11 to Figure 4.14 it can be seen that the difference near the integration starting point (V_{gs0} , V_{ds0}) is small. However, the difference increases as the integration is taken further from the starting point. This is a result of numerical problems relating to the extracted ECP in certain regions and leads to the integrability conditions not being perfectly satisfied. Ideally, the best integration starting point is where the integrability conditions are satisfied best at the point of operation. For a Class-A operating point (V_{GS} equal to -4V, V_{DS} equal to 8V), the best integration starting point would be where V_{gs0} is equal to -8V and V_{ds0} is equal to 0V or 10V, as seen in Figure 4.12 and Figure 4.13 respectively. Using these starting parameters, the error at the operating point is much smaller compared to the same biasing points seen in Figure 4.11 and Figure 4.14.

The next step is to use the same integration starting points shown in Table 4.1 to construct the nonlinear models and compare the predictions of the models to the measured results. This should verify if the suggested integration starting points of V_{gs0} equal to -8V and V_{ds0} equal to 0V or 10V will give the best result. For each of the starting points, the nonlinear functions were constructed and modelled in ADS. A series of comparisons between measured and modelled results were analysed to determine which starting point gives the best result. The models were first compared to the large-signal single-tone measurements as seen in Figure 4.15 to Figure 4.17 and then to the measured S-parameters of the device, as shown in Figure 4.18 to Figure 4.21.

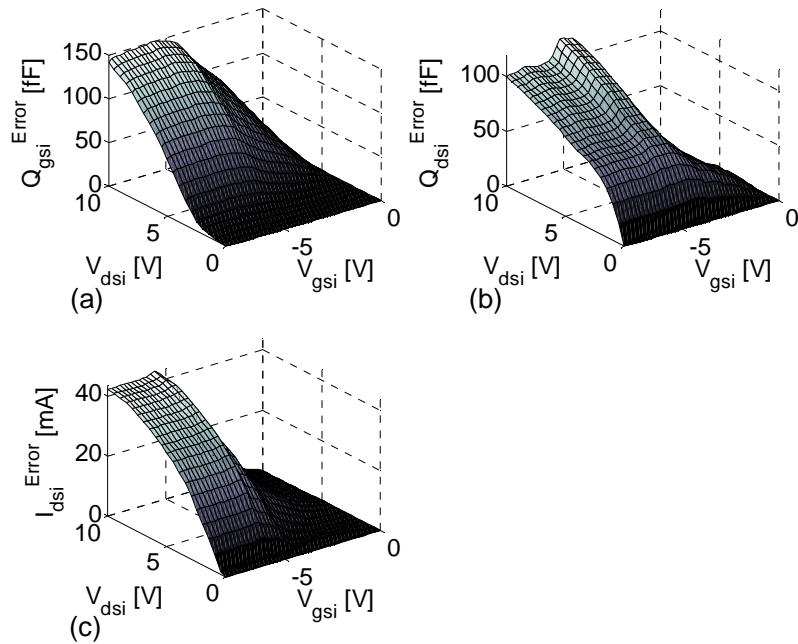


Figure 4.11 The absolute difference of (a) Q_{gsi} , (b) Q_{dsi} and (c) I_{dsi} associated with the integration process when an integration starting point of $V_{gs0} = 0V$, $V_{ds0} = 0V$ is selected.

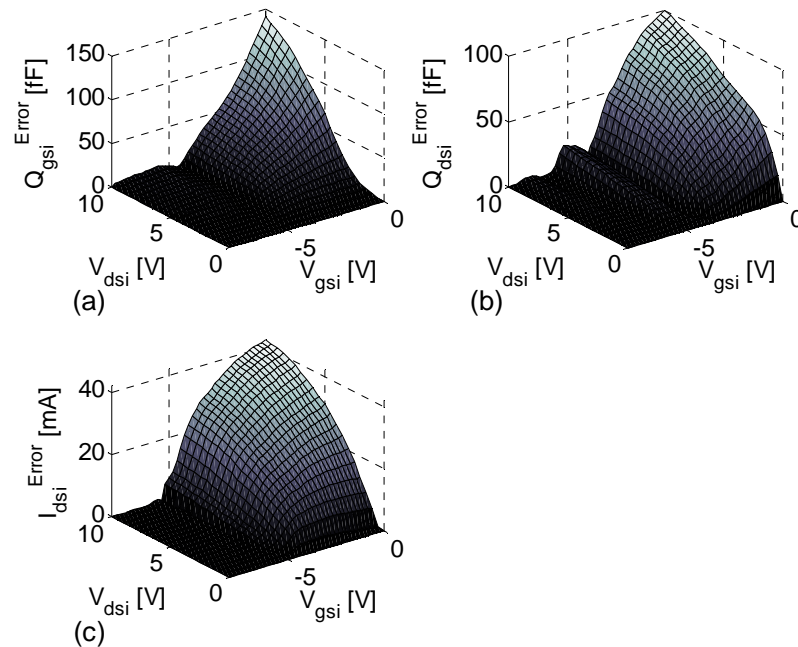


Figure 4.12 The absolute difference of (a) Q_{gsi} , (b) Q_{dsi} and (c) I_{dsi} associated with the integration process when an integration starting point of $V_{gs0} = -8V$, $V_{ds0} = 0V$ is selected.

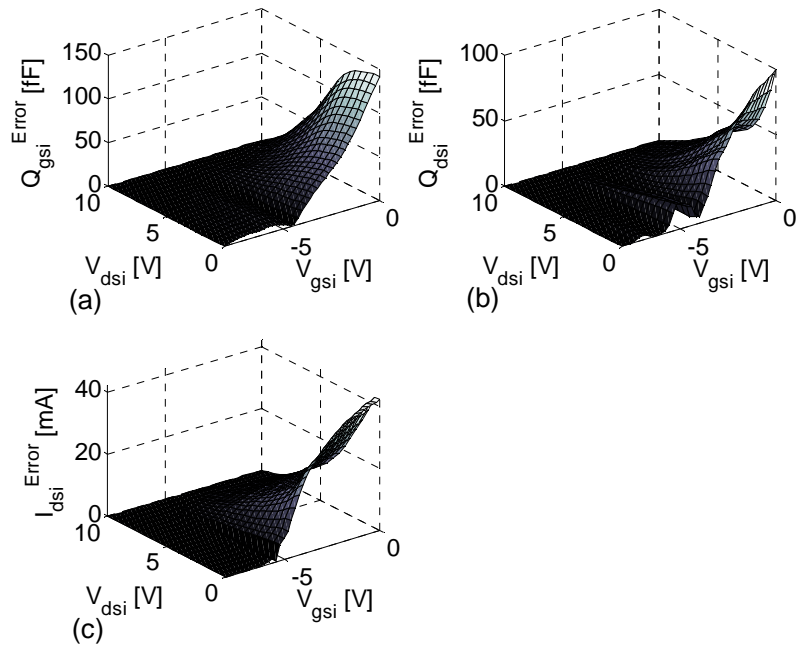


Figure 4.13 The absolute difference of (a) Q_{gsi} , (b) Q_{dsi} and (c) I_{dsi} associated with the integration process when an integration starting point of $V_{gs0} = -8V$, $V_{ds0} = 10V$ is selected.

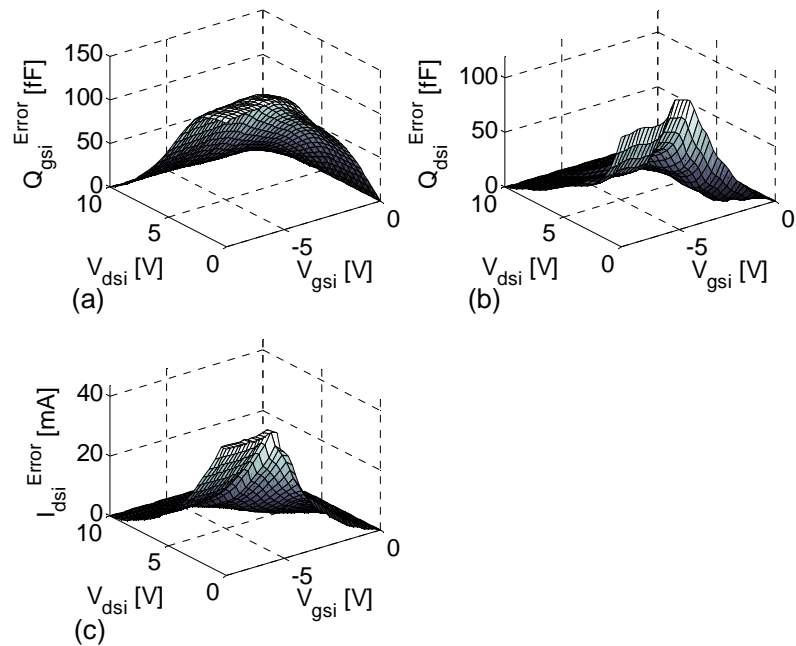


Figure 4.14 The absolute difference of (a) Q_{gsi} , (b) Q_{dsi} and (c) I_{dsi} associated with the integration process when an integration starting point of $V_{gs0} = 0V$, $V_{ds0} = 10V$ is selected.

Figure 4.15(a) to (c) shows the plot of input power P_{in} versus output power P_{out} of the fundamental, second harmonic and third harmonic. Figure 4.16 shows the instantaneous voltage and current wave forms with an input power P_{in} equal to 2.45 dBm. As mentioned, the device is biased for typical Class-A operation (V_{GS} equal to -4V, V_{DS} equal to 8V) with the fundamental tone f_o equal to 2GHz. Firstly, it should be noted that the model prediction of the large-signal single-tone measurements at low power levels is fairly inaccurate, which can be attributed to the poor dynamic range of the measurement setup. However, the LSNA also measures the time domain wave forms for a fixed input power, which can give a more accurate comparison between the measured and simulated models at a fixed point, as seen in Figure 4.16(a) to (d). The legend bar in Figure 4.15 is the same for Figure 4.16 to Figure 4.17. A factor that must be considered is that these are experimental on-wafer devices and the manufacturing process is not always perfect. Devices that are exactly the same can differ dramatically, depending on the position on the wafer, which can make the modelling process even more difficult. An example of this can be observed in Figure 4.15(b), where the measured curve has a dip around an input power of +2dBm. All the models predict a slope of 2/1, which could be correct as it is the second harmonic. In this case, it is better to evaluate the time wave form to compare the measured and simulated results.

Evaluating Figure 4.15 to Figure 4.21 it can be seen that an integration starting point of V_{gs0} equal to -8V and V_{ds0} equal to 0V or 10V gives the best modelling result as predicted earlier in this section. This result can be attributed to the fact that the integration starting point was taken at a low drain current condition. If the starting point was taken at a high drain current condition, then negative and unphysical values of the drain current may be obtained. Also, if the starting point is not taken from a low current condition, then output conductance can also reach unphysical high values in the linear region, which are due to both numerical problems and dispersion. The other advantage of selecting the integration starting point at V_{gs0} equal to -8V is that if the integration is firstly carried out with respect to the intrinsic drain voltage V_{dsi} and secondly, with respect to the intrinsic gate voltage V_{gsi} the output conductance is only used under pinch-off condition, where the effect of this parameter can be almost neglected. However, if the integration starting point was first carried out with respect to the intrinsic gate voltage V_{gsi} instead of the intrinsic drain voltage, then the drain current is very sensitive to the value of g_{ds} in the linear region, as most of the area under the g_{ds} curve occurs at low drain voltage. By evaluating Figure 4.15 to Figure 4.21 and following the reasoning above, it is deduced that an integration starting point of V_{gs0} equal to -8V and V_{ds0} equal to 0V or 10V gives the best result. However, V_{ds0} equal to 10V is closer to the operating point and thus will be used to determine the integration functions in this thesis.

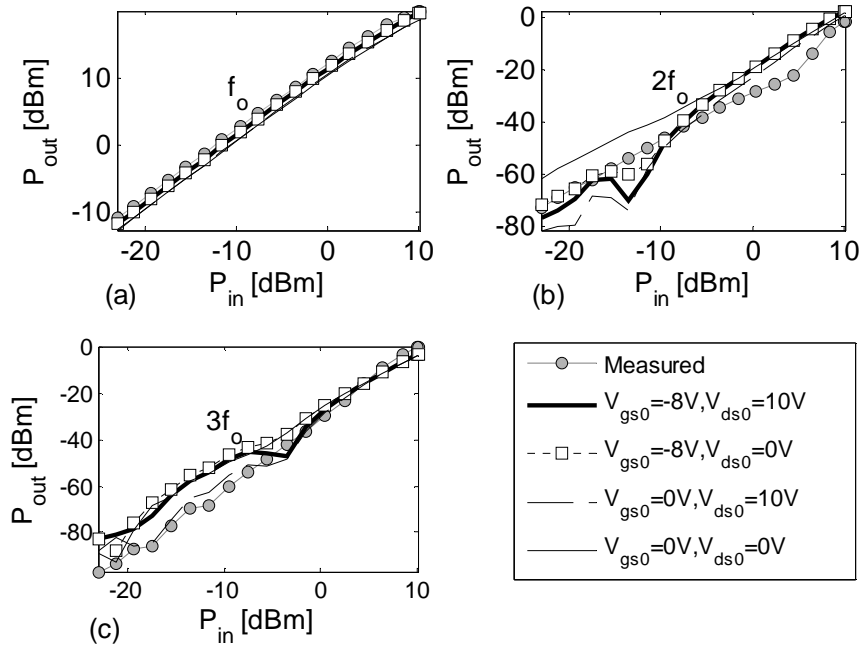


Figure 4.15 The large-signal single-tone measurements of the (a) fundamental, (b) second harmonic and (c) third harmonic for different integration starting points.

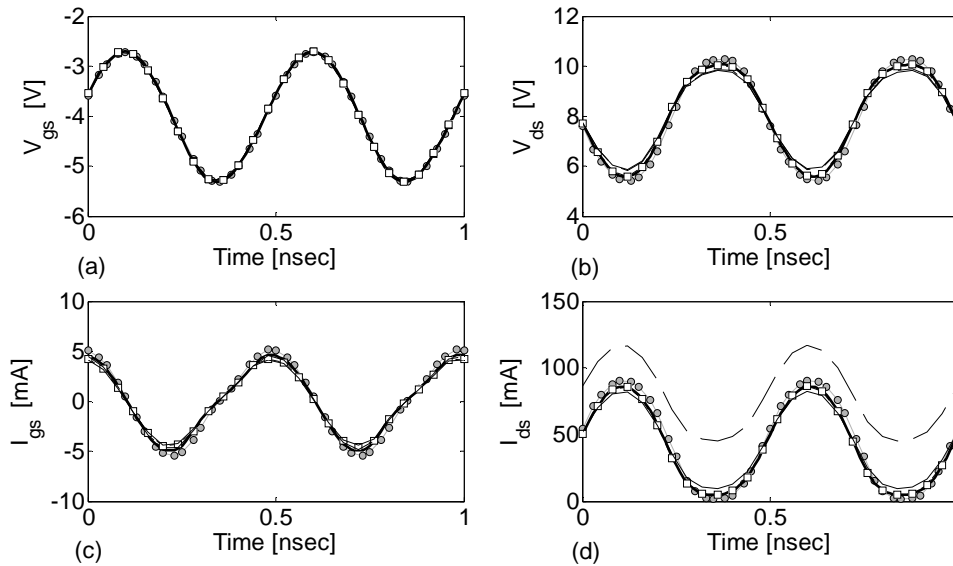


Figure 4.16 The time wave forms of the gate (a) and drain (b) voltages, as well as the gate (c) and drain (d) current wave forms. An excitation with an input power level of $P_{in} = 2.45\text{dBm}$ and fundamental frequency $f_0 = 2\text{GHz}$ is applied.

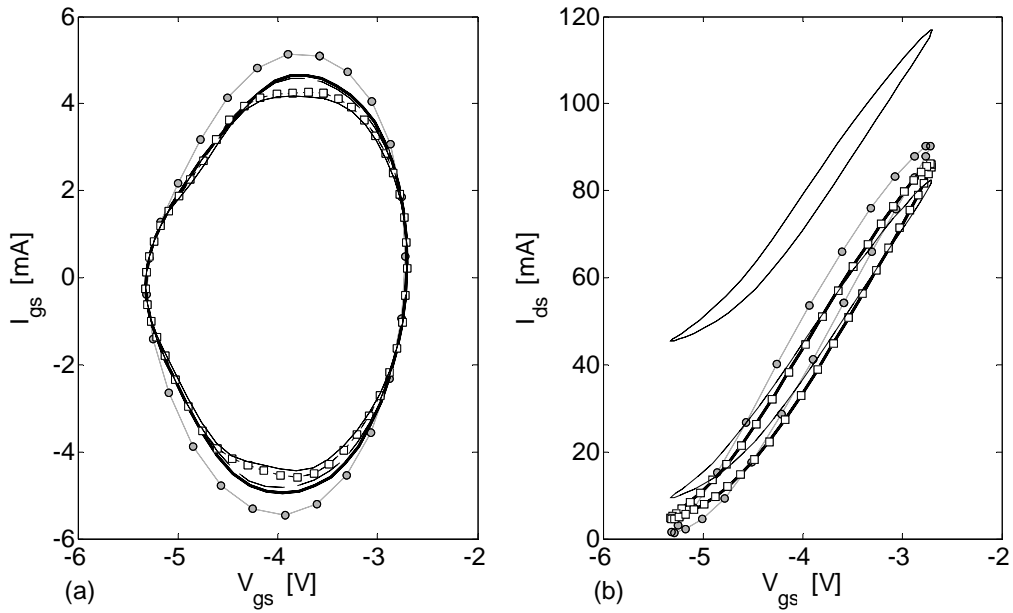


Figure 4.17 The voltage versus current plots at the gate (a) and drain (b) ports for an input power level of $P_{in} = 2.45\text{dBm}$ and a fundamental frequency of $f_0 = 2\text{GHz}$.

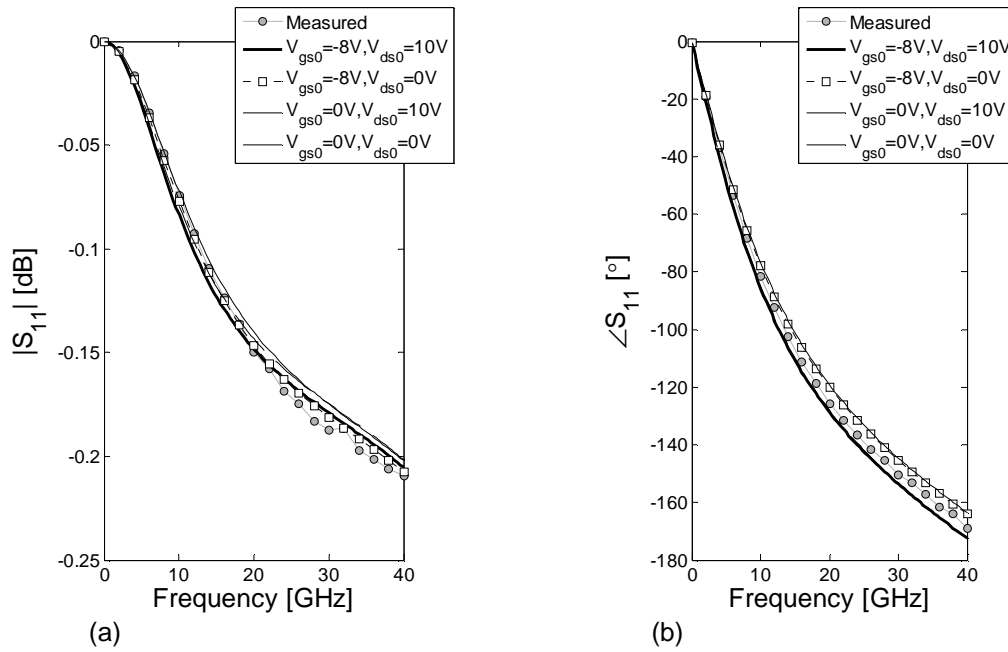


Figure 4.18 The plots of the magnitude (a) and phase (b) of S_{11} versus frequency with different integration starting points.

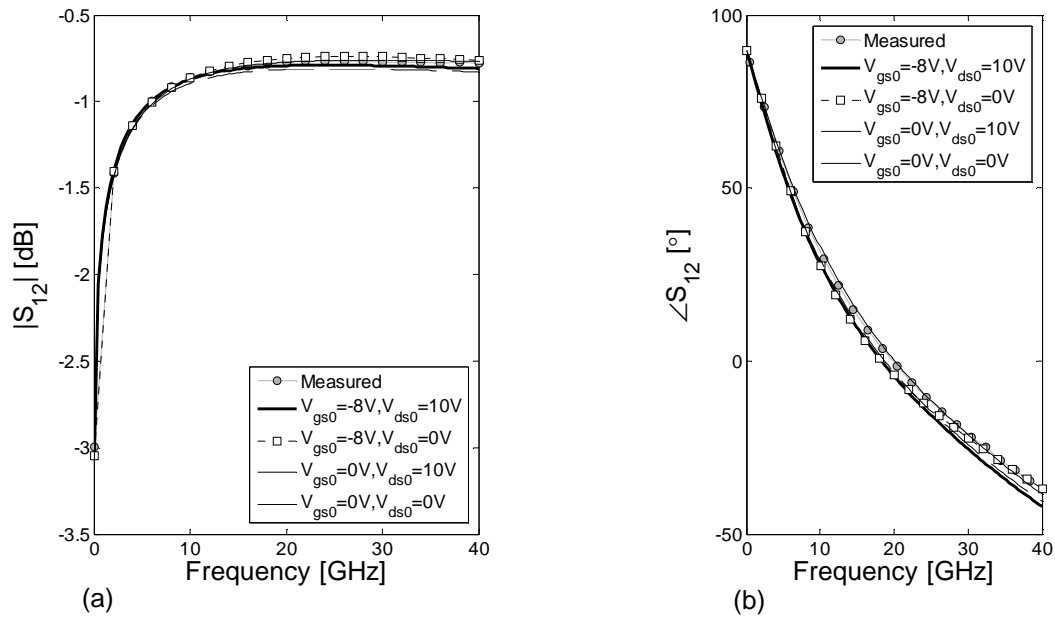


Figure 4.19 The plots of the magnitude (a) and phase (b) of S_{12} versus frequency with different integration starting points.

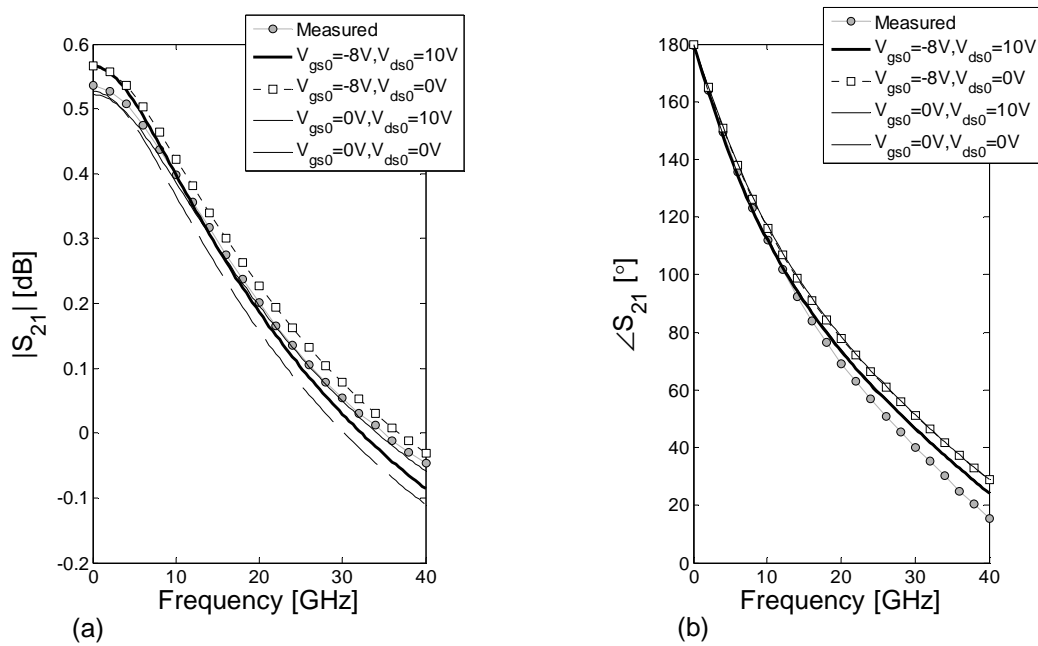


Figure 4.20 The plots of the magnitude (a) and phase (b) of S_{21} versus frequency with different integration starting points.

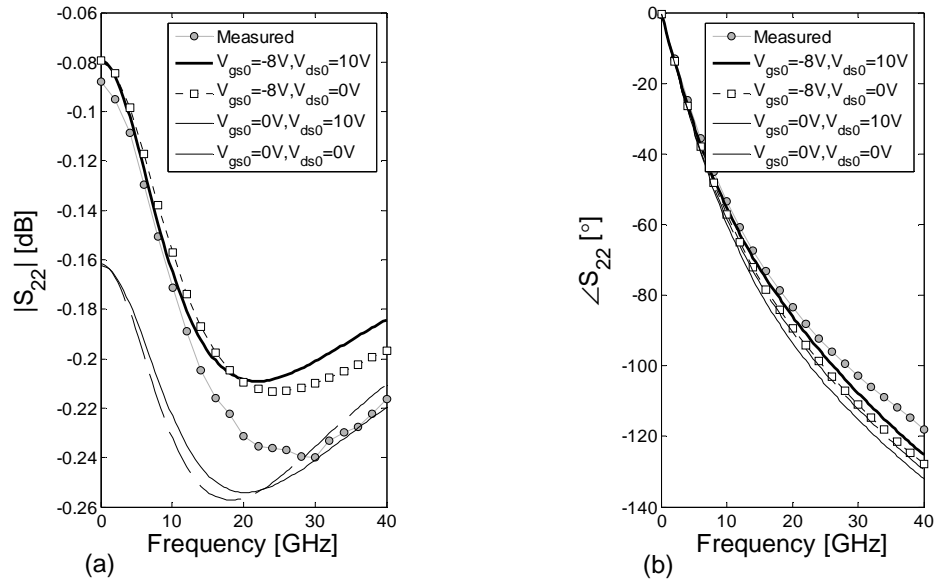


Figure 4.21 The plots of the magnitude (a) and phase (b) of S_{22} versus frequency with different integration starting points.

4.5.3 Root Model versus Modified Root Model

The model presented in Figure 4.6 is the standard nonlinear model used for a wide range of devices. The model consists of four sources, I_{gsi} , Q_{gsi} at the gate port and I_{dsi} , Q_{dsi} at the drain port. I_{gsi} represents the gate leakage of the device and can be attributed to device degradation. The device measured for this analysis had little to no degradation and thus the I_{gsi} sources will have no significant contribution to the model and can be neglected. The sources can be presented in either look-up tables or as analytical functions. As a starting point, the table-based models are implemented using ADS. However, later in the section, analytical models will be implemented. Once again, the model predictions were compared to the measured large-signal one-tone results in Figure 4.22 to Figure 4.24 and S-parameter measurements in Figure 4.25 to Figure 4.28. The first observation from the large-signal single-tone measurements is that there is no difference between the Root and modified Root model. This result is expected as the only difference between the two models is the charging resistance R_i . The resistance only improves the S-parameter predictions, which can be clearly observed in Figure 4.25 to Figure 4.28. In conclusion, the modified Root model gives the same result as the Root model with the single-tone predictions, but better results with the S-parameter predictions. Thus, the modified Root model will be used as a base model in the next sections.

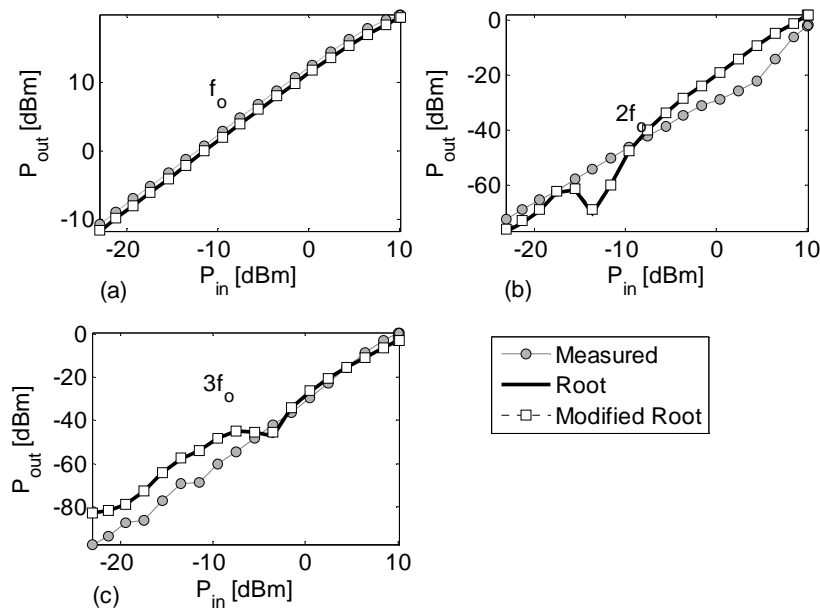


Figure 4.22 The large-signal single-tone measurements of the (a) fundamental, (b) second harmonic and (c) third harmonic. The grey circled line represents the measured data, while the solid line presents the Root model and the dashed line the modified Root model.

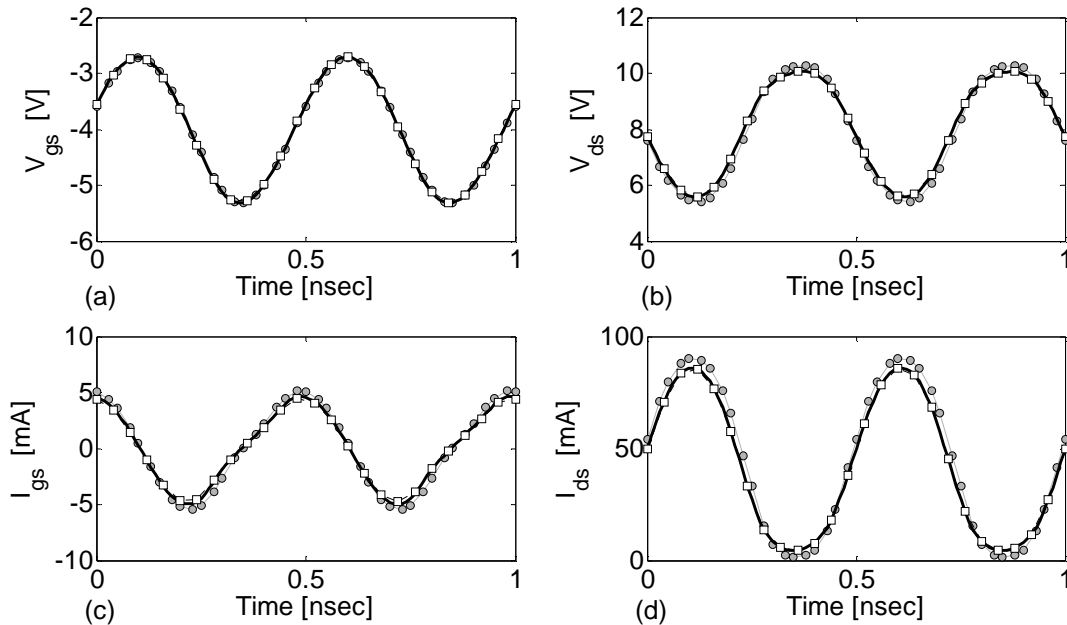


Figure 4.23 The time wave forms of the gate (a) and drain (b) voltages, as well as the gate (c) and drain (d) current wave forms. The grey circled line represents the measured data, while the solid line the Root model and the dashed line the modified Root model.

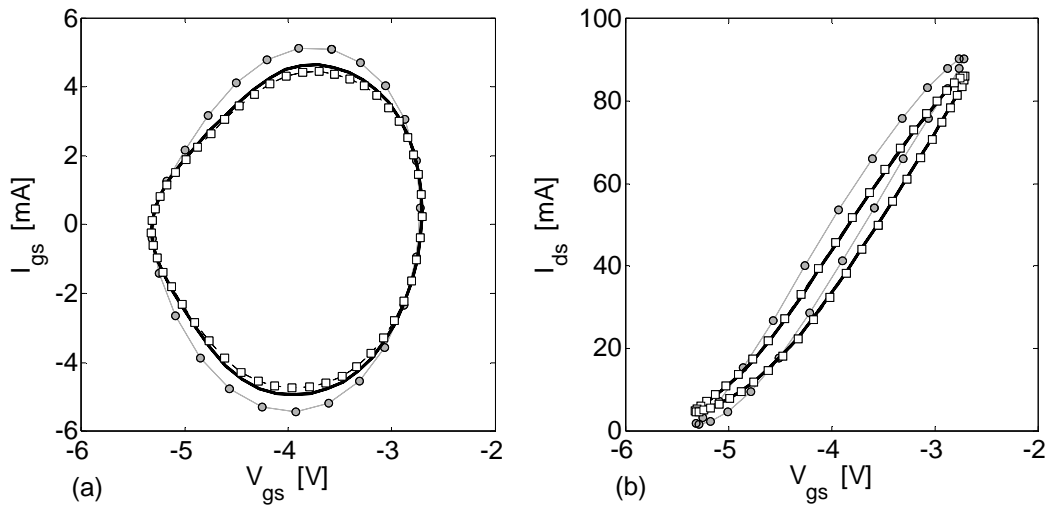


Figure 4.24 The voltage versus current plots at the gate (a) and drain (b) ports. The circled line represents the measured data, while the solid line the Root model and the dashed line the modified Root model.

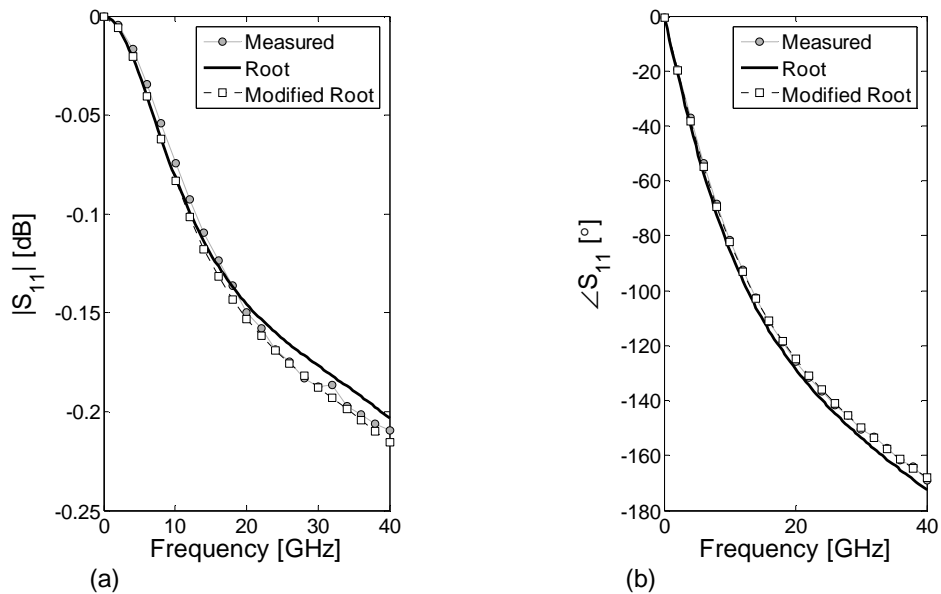


Figure 4.25 The plots of the magnitude (a) and phase (b) of S_{11} versus frequency. The grey circled line represents the measured data, while the solid line the Root model and the dashed line the modified Root model.

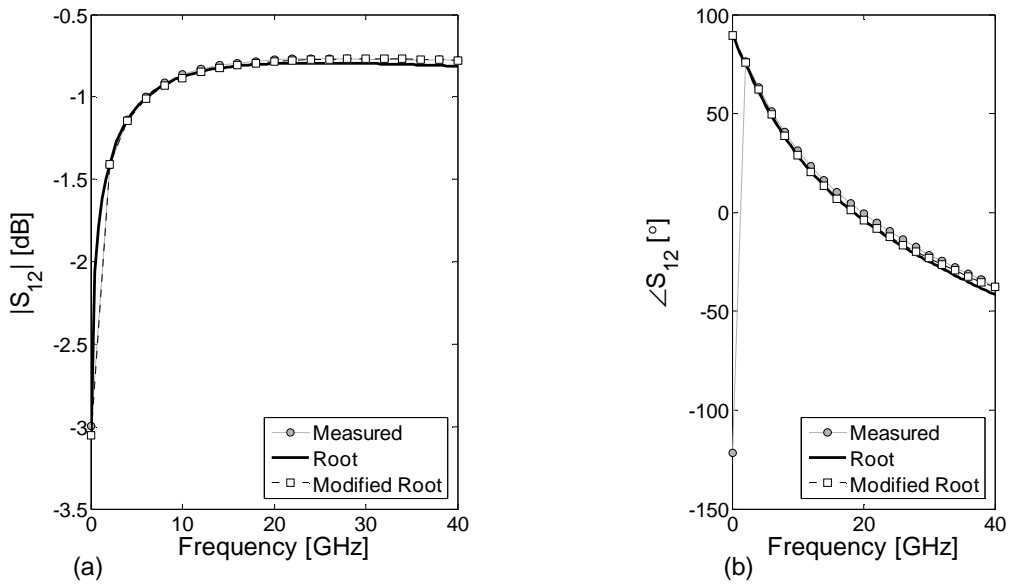


Figure 4.26 The plots of the magnitude (a) and phase (b) of S_{12} versus frequency. The grey circled line represents the measured data, while the solid line the Root model and the black dashed line the modified Root model.

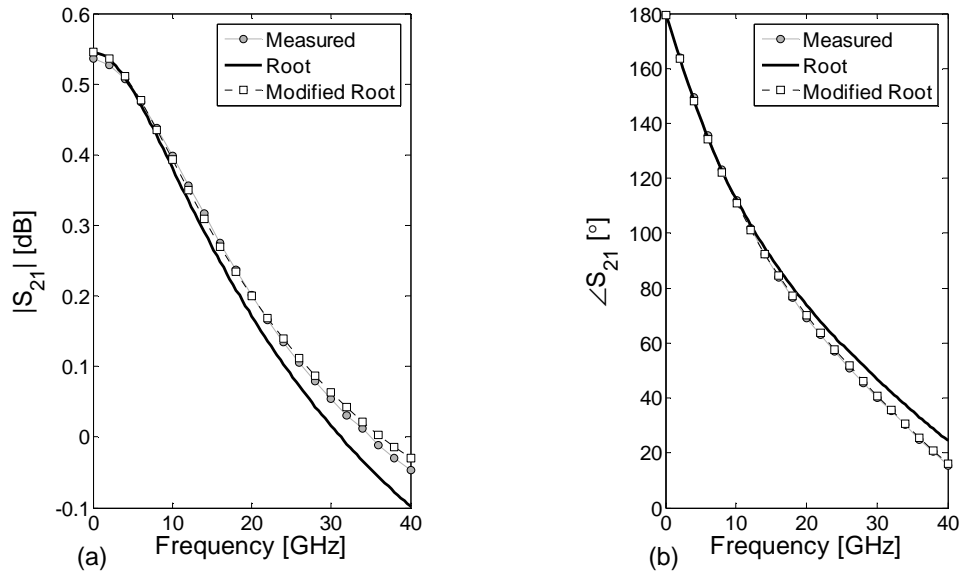


Figure 4.27 The plots of the magnitude (a) and phase (b) of S_{21} versus frequency. The grey circled line represents the measured data, while the solid line the Root model and the dashed line the modified Root model.

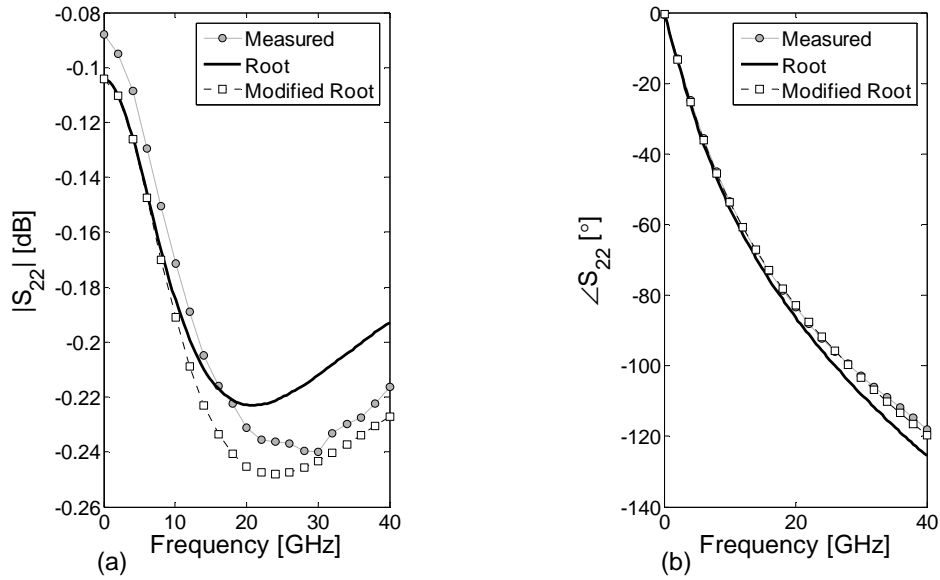


Figure 4.28 The plots of the magnitude (a) and phase (b) of S_{22} versus frequency. The grey circled line represents the measured data, while the solid line the Root model and the black dashed line the modified Root model.

4.5.4 Analytical Modelling of the Drain Current Source

As mentioned, the models used thus far have been table-based models. The disadvantage of table-based models is that the data sets include noise. It is almost impossible to obtain the higher order derivatives by differentiating the drain current I_{dsi} directly. These models also struggle when dealing with small excitation signals. The tables are forced to interpolate and if data points are too far apart, the interpolation becomes noisy and inaccurate. In this section, the table-based drain current source is replaced with an analytical function.

It is well documented that the drain current source is the main origin of nonlinear behaviour in an HEMT device and thus should be modelled as accurately as possible. The I_{dsi} model must be able to predict the higher order derivatives of the current in order to accurately represent soft nonlinear behaviour such as IMD. In chapter three, a measurement setup is presented that extracts these derivatives directly from measurements. The analytical function used to model the drain current source is known as the Fager model [28]. This model has been successfully used to predict IMD behaviour of a GaN HEMT device [14]. The model is defined by a set of equations, each representing four specific operating regions, shown in Figure 4.29. The advantage of observing separate regions is that the modelling can be broken into smaller sections, which

together form the nonlinear current equation. This allows accurate IMD prediction, as well as the accurate prediction of output power and efficiency.

The different regions seen in Figure 4.29 are defined as follows. Firstly, in region A, the device is biased in the sub-threshold region, then as V_{GS} is increased and region B is entered the drain current starts to rise quadratically and G_m has a linear slope. In region C, the current increases linearly and the transconductance becomes constant. This region is known to provide good linearity, but at the cost of efficiency. As the bias is further increased, region D is entered and the device becomes saturated, which leads to a drop in transconductance. The final set of equations is given in equations (4.16) to (4.20), which are implemented in ADS. For the full detailed deduction of these equations refer to [14], [16], [28]. Table 4.2 gives a short description of each of the parameters in equations (4.16) to (4.20).

A Matlab program was developed that implements a Gauss-Newton optimiser to fit the analytical function given in equation (4.20) to the table-based integration function derived in equation (4.9). The function optimises the Fager parameters in Table 4.2 by comparing the table-based values I_{dsi}^{table} , shown in equation (4.14), to the results from analytical function $I_{dsi}^{modelled}$. Equation (4.15) is used to model the error between the table-based I_{dsi}^{table} and modelled $I_{dsi}^{modelled}$ parameters. Error functions must be dimensionless and thus the difference between I_{dsi}^{table} and $I_{dsi}^{modelled}$ is divided again by I_{dsi}^{table} in order to normalise the function. The result of the optimiser is used as a figure of merit to determine if the optimiser has reached the minimum target error. Once the optimiser reaches a value under the user-defined target, the optimisation is complete.

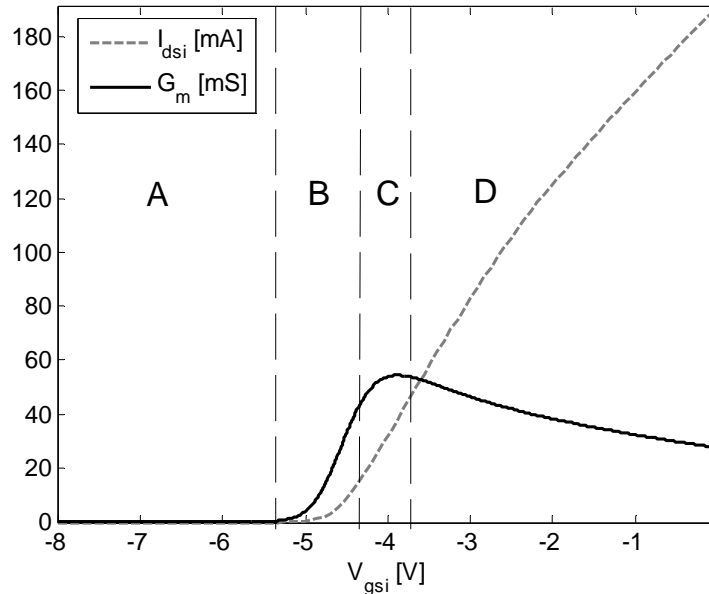


Figure 4.29 The plots of the drain current I_{dsi} and transconductance G_m versus gate voltage V_{GS} . The graph is divided into four regions that represent the condition of the device.

Parameter	Description
V_T	Determines the turn-on voltage
γ	Determines the dependence of V_T with V_{DS}
V_{ST}	Controls the turn-on abruptness
β	Controls the slope in the quadratic region
V_L, β	Determines the slope of the quadratic region and the transition to the linear region
p_{lin}	Used to tune the transconductance slope in the linear region
V_K	Represents the constant gate voltage at which the device becomes saturated
Δ	Determines the slope of the saturation
λ, α, p_{sat}	Controls the dependence on the drain source voltage V_{DS}

Table 4.2 Summary of the Fager model parameters.

$$\text{Data} = [V_{gs}^{\text{table}} \quad V_{ds}^{\text{table}} \quad I_{dsi}^{\text{table}}] \quad (4.14)$$

$$\text{Error}_{I_{ds}} = \sqrt{\sum_{i=1}^N \frac{|I_{dsi}^{\text{table}}|^2 - |I_{dsi}^{\text{modelled}}|^2}{|I_{dsi}^{\text{table}}|^2}} \quad (4.15)$$

The starting values for the optimiser must be manually entered and may require some tuning. It should be noted that these values are only the starting values for the optimiser and thus are not expected to be a perfect fit. The values can be derived by evaluating equations (4.16) to (4.20). Firstly, the threshold voltage V_T is determined from the peak of $G_{m2}(V_{gs})$ or the first null in $G_{m3}(V_{gs})$. By tuning γ in equation (4.16) it is possible to get a first stage fit from equation (4.17), as shown in Figure 4.30(a). The next step in the process is to tune V_K and Δ in equation (4.18) to obtain the second stage fit seen in Figure 4.30(b). In the third stage, V_{ST} must be tuned in order to obtain the relative turn-on abruptness, demonstrated in Figure 4.30(c). Finally, in the last stage V_L , p_{lin} , λ , α and p_{sat} are tuned to get the first order drain current $I_{dsi}^{\text{modelled}}$ fit as seen in Figure 4.30(d). Once the starting values have been determined, the next step is to run the optimiser function to optimise each parameter for the best possible fit.

The function optimises the Fager parameters for a number of drain voltage V_{dsi} points, shown in Figure 4.31(a) to (d). The idea is to divide the drain current function I_{dsi} into smaller sections and fit the parameters of the Fager model to each section simultaneously. The final model is the combination of the individual optimised sections, as shown in Figure 4.32. From this figure, it can be seen that the final optimised function demonstrates an excellent fit to the table-based drain current data set. The set of parameter values for the T_{03} device is presented in Table 4.3. The following section describes how the optimiser is expanded to include the extracted higher order drain current derivatives (G_m , G_{m2} , G_{m3}) from chapter three.

$$V_{T0}(V_{dsi}) = V_T + \gamma \cdot V_{dsi} \quad (4.16)$$

$$V_{GS1}(V_{gsi}) = V_{gsi} - V_{T0}(V_{dsi}) \quad (4.17)$$

$$V_{GS2}(V_{gsi}) = V_{GS1} - \frac{1}{2} \left(V_{GS1} + \sqrt{(V_{GS1} - V_K)^2 + \Delta^2} - \sqrt{V_K^2 + \Delta^2} \right) \quad (4.18)$$

$$V_{GS3}(V_{gsi}) = V_{ST} \cdot \ln \left(1 + e^{\frac{V_{GS2}}{V_{ST}}} \right) \quad (4.19)$$

$$I_{dsi}^{\text{modelled}}(V_{gsi}) = \beta \cdot \frac{V_{GS3}^2}{1 + \frac{V_{GS3}}{V_L}} (1 + \lambda V_{ds}) \tanh \left(\frac{\alpha V_{dsi}}{V_{GS3}^{P_{sat}}} \right) \quad (4.20)$$

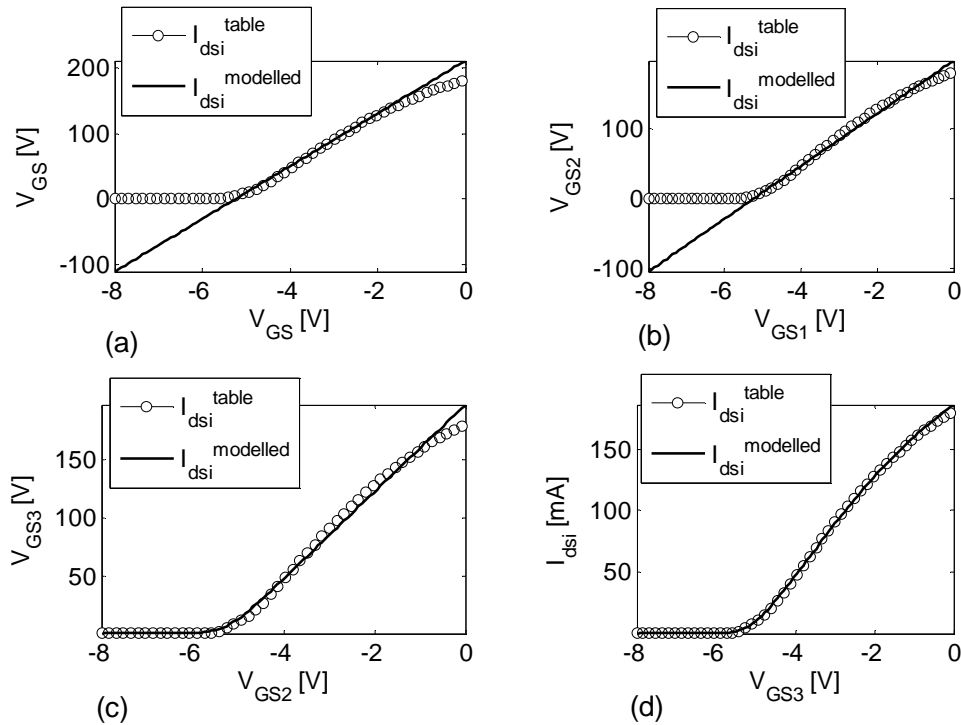


Figure 4.30 The different stages of the Fager model $I_{dsi}^{\text{modelled}}$ fitted to the table-based drain current I_{dsi}^{table} data set. (a) Represents the first stage fit of equation (4.17). (b) The second stage fit of equation (4.18). (c) The third stage fit of equation (4.19) and (d) is the fourth stage fit of equation (4.20).

Parameter	I_{dsi}
V_{ST}	1.3395e-001
V_T	-5.0547e+000
β	2.2426e-001
V_L	8.1402e-001
p_{lin}	1.0090e+000
V_K	-5.9153e-001
Δ	6.7430e+000
λ	-1.1725e-003
p_{sat}	1.2374e+000
α	5.0382e-001
γ	-5.9567e-002

Table 4.3 The values of the optimised Fager model parameters for the T_{03} device topology.

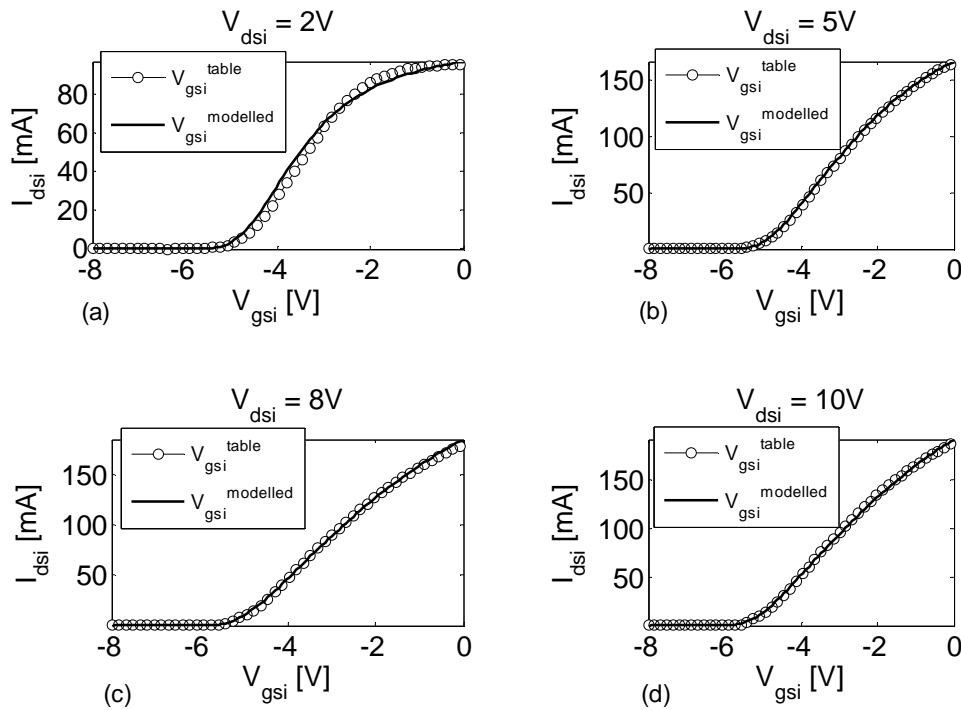


Figure 4.31 The measured drain current I_{dsi} is compared to the optimised modelled function for the T_{03} device. Points at a fixed drain voltage bias (a) $V_{dsi} = 2V$, (b) $V_{dsi} = 5V$, (c) $V_{dsi} = 8V$ and (d) $V_{dsi} = 10V$ are shown versus gate voltage V_{gsi} .

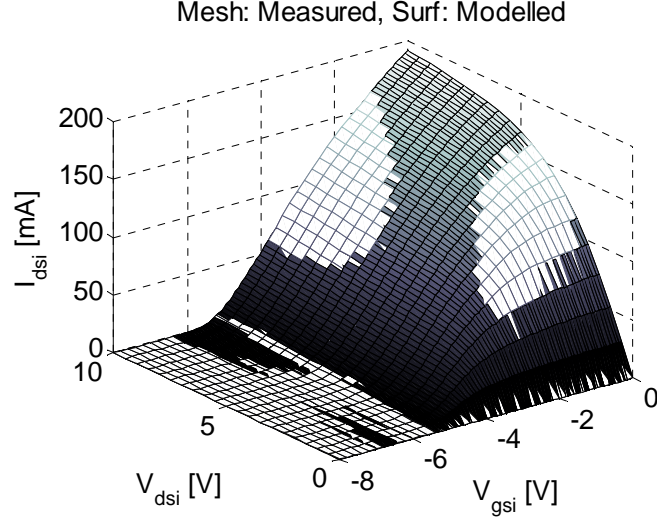


Figure 4.32 The measured drain current I_{dsi} shown as the mesh grid is compared to the optimised modelled function plotted as the surf plot for the T_{03} device.

4.5.5 Incorporating Measured Gradient into the Fager Drain Current Model

The optimiser function presented in section 4.5.4 is modified to include the drain current derivatives ($G_m^{\text{extracted}}$, $G_{m2}^{\text{extracted}}$, $G_{m3}^{\text{extracted}}$) extracted in chapter three. The gradient data is added as an extra parameter set, shown in equation (4.21). The function optimises the Fager parameters to fit the model simultaneously to the I_{dsi}^{table} data and the current derivatives $G_m^{\text{extracted}}$, $G_{m2}^{\text{extracted}}$ and $G_{m3}^{\text{extracted}}$. The main goal of including the gradient data in the nonlinear drain current model I_{dsi} is to improve the accuracy of the IMD predictions. The current gradients are extracted over a swept gate voltage V_{gsi} , while the drain voltage V_{dsi} is set to a constant value. The biasing voltages would be the typical points of interest to model the IMD performance of the device. The white strip in Figure 4.33 shows the typical range over which the gradients are extracted for the T_{03} device.

$$\text{Data} = [V_{gs} \quad V_{ds} \quad I_{dsi}^{\text{table}} \quad G_m^{\text{extracted}} \quad G_{m2}^{\text{extracted}} \quad G_{m3}^{\text{extracted}}] \quad (4.21)$$

As mentioned in the previous section, an error function is used to compare the modelling error between the table-based data and the Fager model. The error function is now expanded to include the errors between the measured ($G_m^{\text{extracted}}$, $G_{m2}^{\text{extracted}}$, $G_{m3}^{\text{extracted}}$) and modelled (G_m^{modelled} , G_{m2}^{modelled} , G_{m3}^{modelled}) derivatives. The final error function in equation (4.25) is thus the combination of the drain current modelling error in equation (4.15) and the higher order derivatives G_m , G_{m2} and G_{m3} shown in equations (4.22) to (4.24).

Figure 4.34 shows a comparison between the optimised drain current function derivatives and the extracted derivatives. The result of adding the measured gradient data is an optimised analytical function that not only accurately predicts the small-signal S-parameters, but also large-signal single-tone and two-tone IMD predictions. The result of the table-based models compared to the combined analytical model is shown in Figure 4.35 to Figure 4.42.

From these figures, it can be seen that the model is similar to the table-based model when comparing the large-signal single-tone and S-parameter predictions. This is to be expected as the analytical function is directly fitted to the drain current sources I_{dsi} . However, a dramatic improvement can be seen in the two-tone IMD predictions demonstrated in Figure 4.42, where the model with the additional extracted derivative data is far more accurate than the standard table-based model. This is the proposed model that is used in chapter five to demonstrate the accuracy of the model over a wide range of bias points.

$$\text{Error_G}_m = \sqrt{\sum_{i=1}^N \frac{|G_m^{\text{meas}}|^2 - |G_m^{\text{modelled}}|^2}{|G_m^{\text{meas}}|^2}} \quad (4.22)$$

$$\text{Error_G}_{m2} = \sqrt{\sum_{i=1}^N \frac{|G_{m2}^{\text{meas}}|^2 - |G_{m2}^{\text{modelled}}|^2}{|G_{m2}^{\text{meas}}|^2}} \quad (4.23)$$

$$\text{Error_G}_{m3} = \sqrt{\sum_{i=1}^N \frac{|G_{m3}^{\text{meas}}|^2 - |G_{m3}^{\text{modelled}}|^2}{|G_{m3}^{\text{meas}}|^2}} \quad (4.24)$$

$$\text{ErrorFuncion} = \text{Error_I}_{ds} + \text{Error_G}_m + \text{Error_G}_{m2} + \text{Error_G}_{m3} \quad (4.25)$$

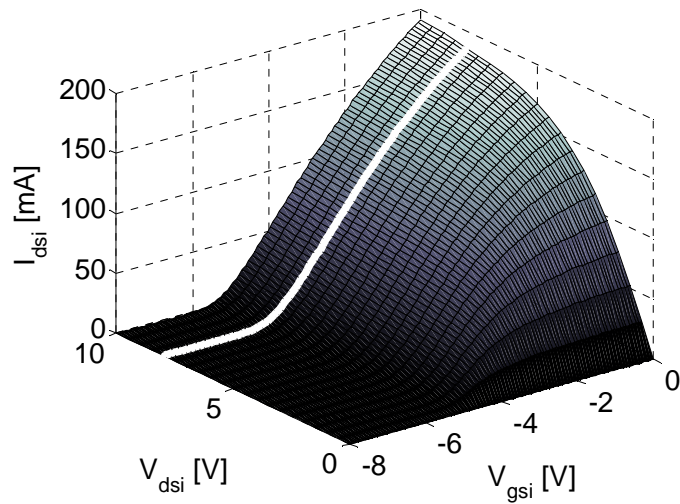


Figure 4.33 The bias points at which the nonlinear coefficients are extracted for the T_{03} device. The drain voltage V_{dsi} is set to a constant value and the coefficients are extracted at a gate bias V_{gsi} from $-8V$ to $0V$.

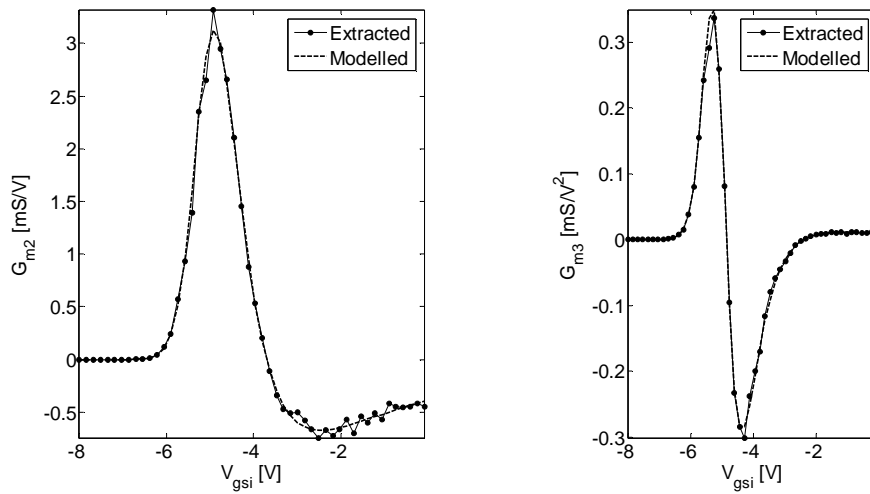


Figure 4.34 The comparison between the optimised model function and extracted IMD coefficients is determined as a function of the gate voltage V_{gsi} . The drain voltage is set to a constant value of $V_{dsi} = 8V$.

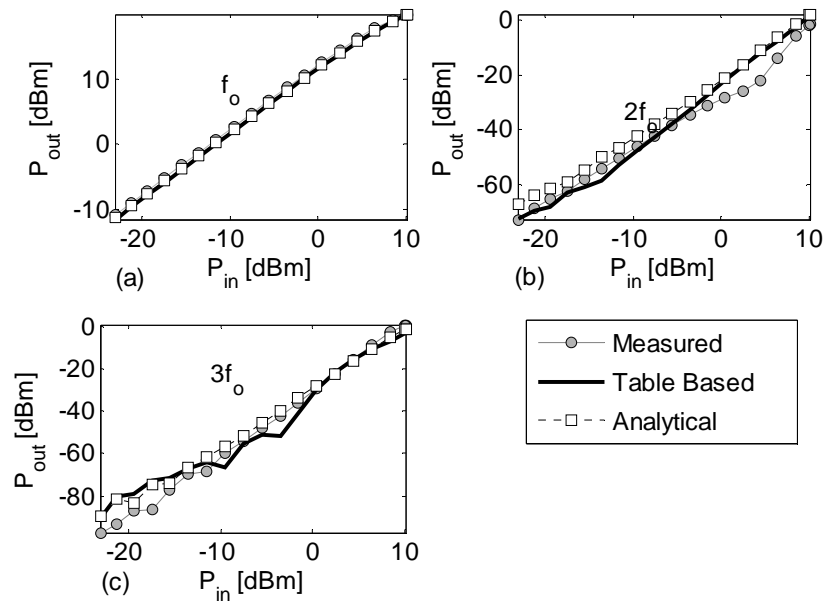


Figure 4.35 The large-signal single-tone measurements of the (a) fundamental, (b) second harmonic and (c) third harmonic. The grey circled line represents the measured data, while the solid line represents the table-based model predictions and the dashed line the analytical-based model.

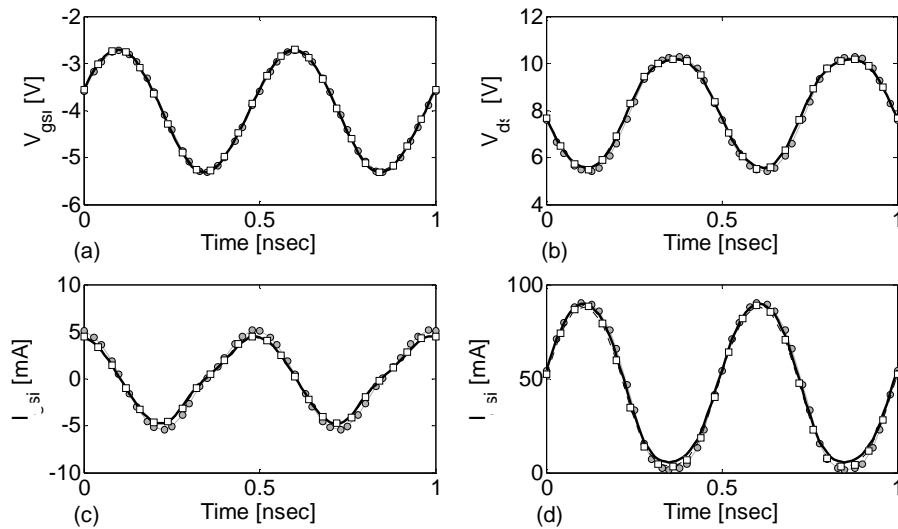


Figure 4.36 The time wave forms of the gate (a) and drain (b) voltages, as well as the gate (c) and drain (d) current wave forms. The grey circled line represents the measured data, while the solid line represents the table-based model predictions and the dashed line the analytical-based model.

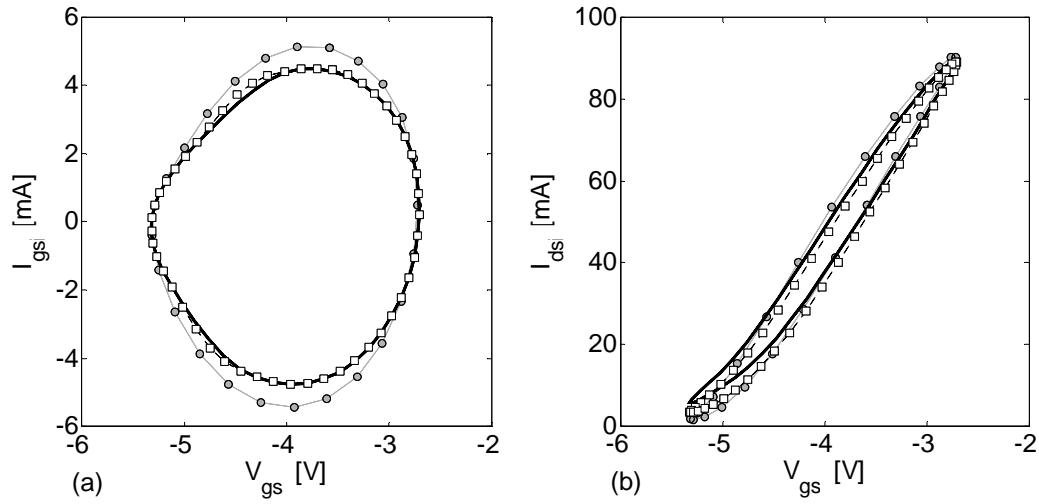


Figure 4.37 The voltage versus current plots at the gate (a) and drain (b) ports. The grey circled line represents the measured data, while the solid line represents the table-based model predictions and the dashed line the analytical-based model.

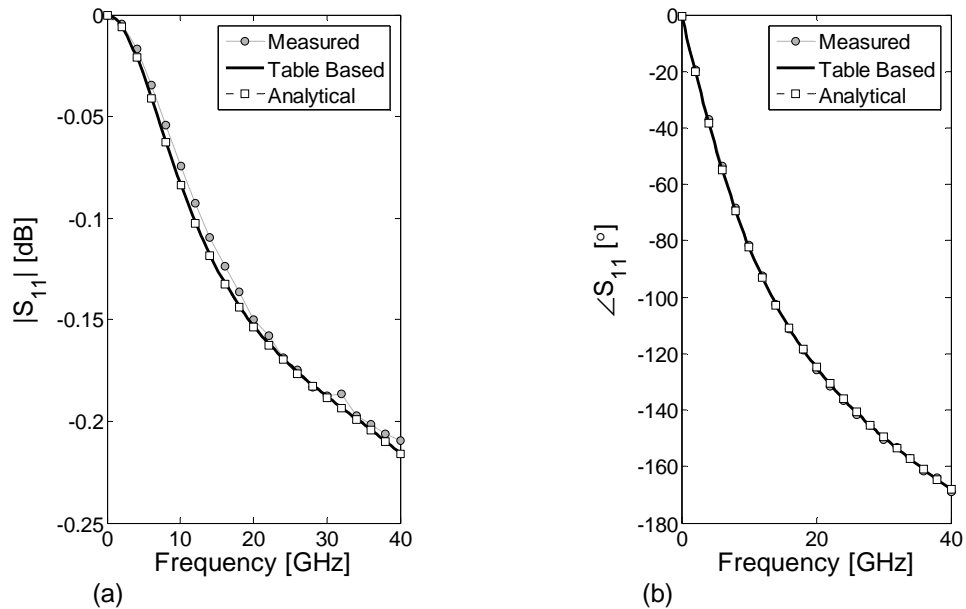


Figure 4.38 The plots of the magnitude (a) and phase (b) of S_{11} versus frequency. The grey circled line represents the measured data, while the solid line represents the table-based model predictions and the dashed line the analytical-based model.

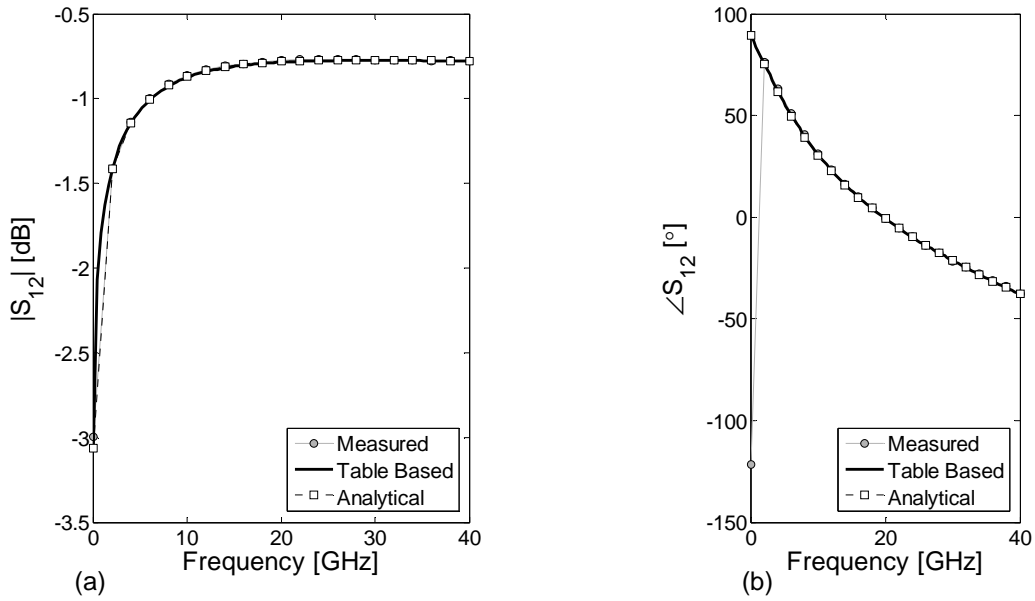


Figure 4.39 The plots of the magnitude (a) and phase, (b) of S_{12} versus frequency. The grey circled line represents the measured data, while the solid line represents the table-based model predictions and the dashed line the analytical-based model.

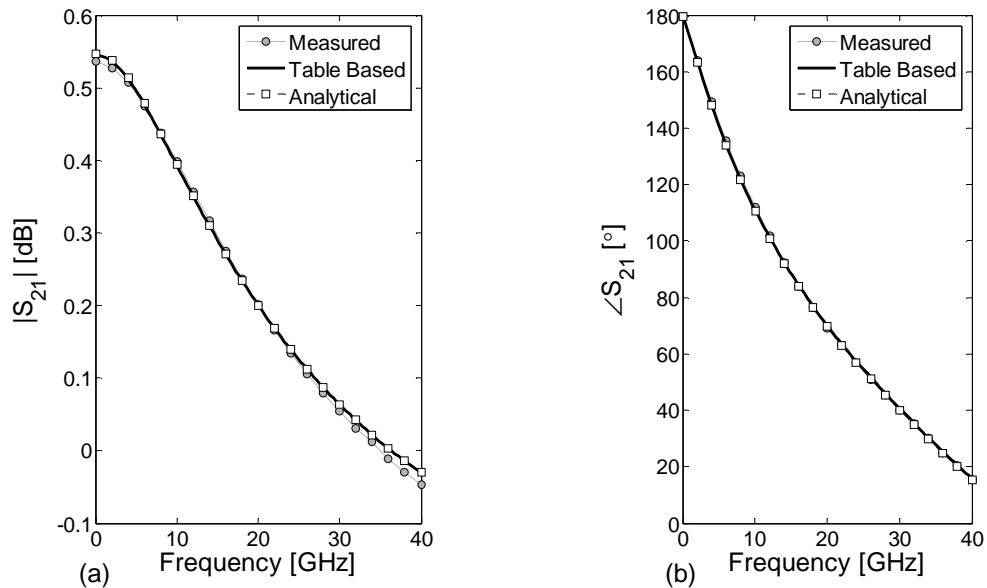


Figure 4.40 The plots of the magnitude (a) and phase (b) of S_{21} versus frequency. The grey circled line represents the measured data, while the solid line represents the table-based model predictions and the dashed line the analytical-based model.

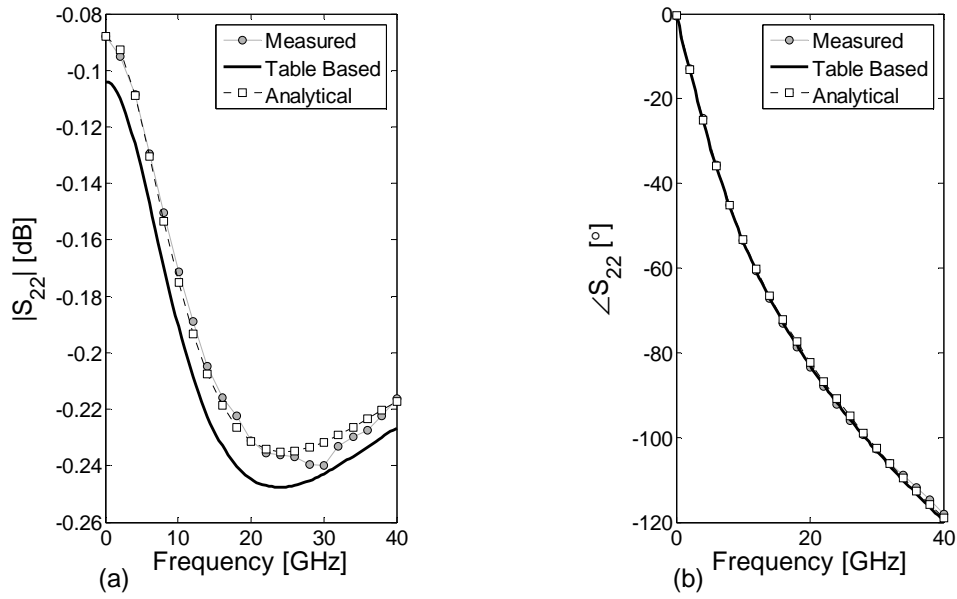


Figure 4.41 The plots of the magnitude (a) and phase (b) of S_{22} versus frequency. The grey circled line represents the measured data, while the solid line represents the table-based model predictions and the dashed line the analytical-based model.

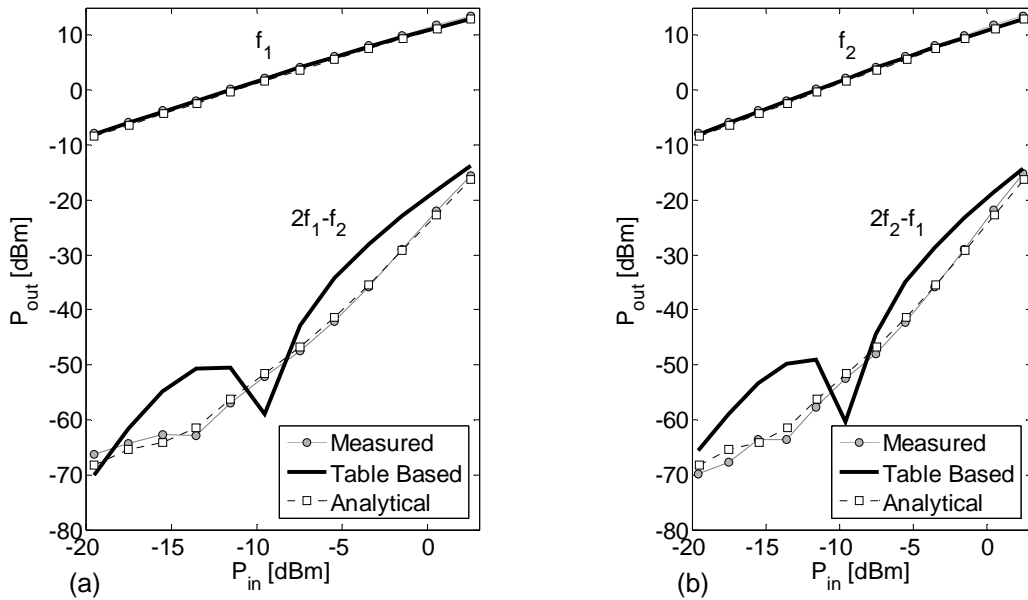


Figure 4.42 The (a) lower and (b) upper IMD products. The grey circled line represents the measured data, while the solid line represents the table-based model predictions and the dashed line the analytical-based model.

4.6 Conclusion

In this chapter, the linear and nonlinear modelling methodology of on-wafer GaN HEMT devices is documented. Firstly, the linear small-signal equivalent circuit topology was presented, followed by a description of the PCFETGUI extraction procedure. Then, the nonlinear model was deduced so that it was consistent with the small-signal equivalent scheme. A Matlab program was developed that can determine the table-based nonlinear integration functions from any desired integration starting point. The drain current source function was then replaced with the Fager model, which is an analytical representation. Another Matlab program was developed that implements a Gauss-Newton optimiser to fit the parameters of the function to the measured values. To improve the prediction capabilities of the function, the current derivative data extracted in chapter three is incorporated into the model. A few key aspects of the nonlinear model were investigated, starting with the evaluation of different integration starting points. The next step was to compare the results of the Root model to the modified Root model. Finally, the drain current source was implemented as an analytical function with the IMD coefficient data extracted from chapter three. In the nonlinear model investigation process, only a single bias point was used to demonstrate the results. The performance of the nonlinear models over a wide range of bias points is validated in the next chapter. In conclusion, the nonlinear model presented in this chapter is designed to accurately predict the linear and nonlinear behaviour of an on-wafer GaN HEMT device.

CHAPTER 5

Nonlinear Model Validation

5.1 Introduction

The goal of this chapter is to verify the nonlinear models proposed for the on-wafer gallium nitride (GaN) high-electron mobility transistor (HEMT) devices measured at the Interuniversity Microelectronics Centre (IMEC) in Leuven, Belgium. The nonlinear models are implemented in Agilent's Advanced Design System (ADS), where the simulation predictions are compared to the measured data from the vector network analyser (VNA) and large-signal network analyser (LSNA). The models are evaluated by their ability to accurately predict the linear and nonlinear behaviour of the devices. Error functions are used to evaluate the predictions over a wide range of bias points and in section 5.2 an overview of the basic principles of error functions is given. Section 5.3 outlines the implementation of the nonlinear models in ADS.

Section 5.4 presents the performance of the nonlinear models, which include the verification of the small-signal S-parameter prediction, large-signal single-tone and two-tone intermodulation distortion prediction. Two devices, T_{02} and T_{12} , are evaluated, as these are the smallest and largest devices measured. The devices are typically expected to operate in a Class-AB mode and thus a point in this region will be demonstrated for both the devices, while error functions are used to evaluate the performance of the T_{02} device over a wide range of bias points. For the largest T_{12} device, only a single point in a class-AB operating region is verified. A limited number of operational T_{12} devices were found on the wafer and for the sake of preserving the device, only a single biasing region is selected to verify the accuracy of the nonlinear model. Finally, the results are discussed in the last section in this chapter.

5.2 Error Functions

Error functions are used to evaluate a modelling error over a wide range of points by representing the difference between the measured and simulated values in an analytical expression. The expressions are dimensionless and not unique, as there are many different

equations that can be used to express modelling errors. The advantage of using error functions is that a large amount of data at a single bias point can be presented as a single representative value. The value of the error function is thus a ratio between the measured and simulated result. By evaluating the values over the desired range of points, it is possible to determine the performance of the model predictions. The points with the largest values are the worst cases and the points with the smallest value the best predictions. The functions used to model the errors in this work are given in equations (5.1) to (5.3).

$$E_{rr} = \frac{1}{N} \cdot \sum_{i=1}^N |S_{xy}^{\text{meas}} - S_{xy}^{\text{sim}}| \quad (5.1)$$

$$E_{rr} = \sqrt{\frac{1}{N} \cdot \sum_{k=1}^M \sum_{i=1}^N \frac{|P_{\text{out}}^{\text{meas}} - P_{\text{out}}^{\text{sim}}|^2}{|P_{\text{out}}^{\text{meas}}|^2}} \quad (5.2)$$

$$E_{rr} = \sqrt{\frac{1}{N} \cdot \sum_{k=1}^M \sum_{i=1}^N \frac{|\text{IMD3}_{\text{out}}^{\text{meas}} - \text{IMD3}_{\text{out}}^{\text{sim}}|^2}{|\text{IMD3}_{\text{out}}^{\text{meas}}|^2}} \quad (5.3)$$

Equation (5.1) is used to model the error of the S-parameter predictions at a single bias point. The simulated prediction S_{xy}^{sim} is subtracted from the measured parameter S_{xy}^{meas} at each frequency point N. The result is then divided by N to obtain the average error over the frequency range. S_{xy} represents the port parameter, where x, y is equal to 1 or 2. Equation (5.2) represents the large-signal single-tone modelling error and equation (5.3) the large-signal two-tone intermodulation modelling error. As both equations (5.2) and (5.3) evaluate output power levels, the error functions are defined in similar ways. Once again, the simulated predictions ($P_{\text{out}}^{\text{sim}}$, $\text{IM3}_{\text{out}}^{\text{sim}}$) are subtracted from the measured parameters ($P_{\text{out}}^{\text{meas}}$, $\text{IM3}_{\text{out}}^{\text{meas}}$) in equation (5.2) and (5.3). All the parameter quantities are expressed in Watts. However, the error functions are required to be dimensionless and thus the quantities must be normalised. The subtracted result between the simulated and measured parameter is divided by the measured value, leading to a normalised value. The parameter N represents the number of points evaluated, while M represents the number of output harmonics. The result is divided by N again to obtain the average value over the N number of power points. Equation (5.2) is only evaluated for the fundamental frequency f_0 , second $2f_0$ and third harmonic $3f_0$ (M is equal to 3).

In equation (5.3) N and M have similar figures of merit, however M now represents the fundamental tones (f_1, f_2) and the intermodulation products ($2f_1-f_2, 2f_2-f_1$). Once again, the error value is determined at each bias point in the verification process. The values are tabulated according to the corresponding bias point and plotted on a graph. These graphs can be presented in various types of plots. In the next section, three types of graphs are used. The first is a three-dimensional plot of the S-parameter error function versus the bias voltages (V_{gs}, V_{ds}). The second is a bubble plot of the large-signal single-tone error functions versus the bias voltages. Finally, the last plot is a two-dimensional graph of the large-signal two-tone IMD error functions versus the bias voltages. The section gives a brief overview of how the nonlinear models were implemented in ADS.

5.3 Simulation Models

The implementation of nonlinear models in a simulation package is very important, as it is the final step in which the model predictions are compared to measured results. This section gives an overview of the implementation of the nonlinear models in Agilent's Advanced Design System (ADS). Three types of modelling predictions were evaluated: linear S-parameters, nonlinear large-signal single-tone and nonlinear large-signal two-tone intermodulation. Figure 5.1 shows the complete nonlinear model with the important sections outlined in boxes. It should be noted that the figure is not very clear, as the purpose of the figure is to capture a complete overview of the building blocks, with the explanation of each block to follow in the next paragraphs.

The basic intrinsic and extrinsic model setup is unchanged in all the simulations. However, the biasing networks are different, depending on the type of simulation required. The gate terminal S-parameter biasing network is shown in Figure 5.2. Both the gate and drain ports are terminated in 50Ω loads, as seen from the ports of the VNA, while the biasing voltages are supplied by the voltage source V_{DC} . A series resistance accounts for the voltage drop over the DC cables. Figure 5.2 also shows the method used to import the values of the extrinsic gate resistance R_g , inductance L_g and capacitance C_{pg} using data access components (DACs). The values of the extrinsic elements are saved in a text file and directly imported into ADS. The drain and source extrinsic elements R_s, R_d, L_s, L_d and C_{pd} are also imported using a similar method, while the drain terminal is biased similar to the gate terminal. For the large-signal single-tone and large-signal two-tone predictions the extrinsic elements are imported using the same technique.

Figure 5.3 shows the symbolic defined device (SDD) used to implement the nonlinear intrinsic model topology required in this work. The SDD specifies port currents, which can be seen in the notation $I[X,Y] = \text{value}$. The X represents the specific port, while Y determines if the values are

given as a current or charge parameter. If Y is equal to zero, the current parameter must be given. However, if Y is equal to one, a charge parameter must be given. The charge parameter is differentiated to give the equivalent current contribution. The charge sources Q_{gsi} and Q_{dsi} are determined using the Matlab program described in section 4.3.3, where the parameters are saved in a table-based text file. Figure 5.4 shows the implementation of the drain current analytical Fager model I_{dsi} described in section 4.3.5. The final drain current source model includes the extracted derivative data from chapter three in order to improve the IMD prediction capability of the nonlinear model. Once the parameters for the intrinsic and extrinsic parameters are determined and imported into the model, the final step is to run the desired simulation. For each simulation, a separate project has to be created where the S-parameters, single-tone and two-tone predictions are simulated. Each model simulates the number of bias points measured during the device characterisation process. At each point, the error function calculates the corresponding value and saves the result in a text file, which is opened in Matlab and presented in a graphical chart. From the graphical information, the performance of the model predictions can be evaluated. The next section gives the results of the predictions from the ADS models compared to measured values from the VNA and LSNA.

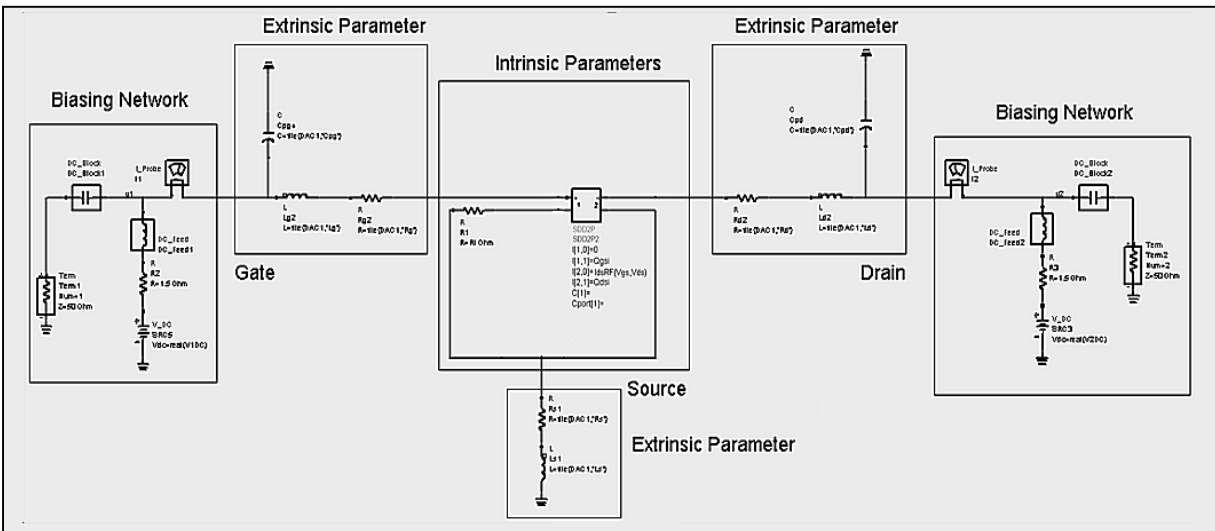


Figure 5.1 The basic simulation diagram consists of the intrinsic elements, extrinsic elements at the gate, source and drain ports and biasing networks at the gate and drain ports.

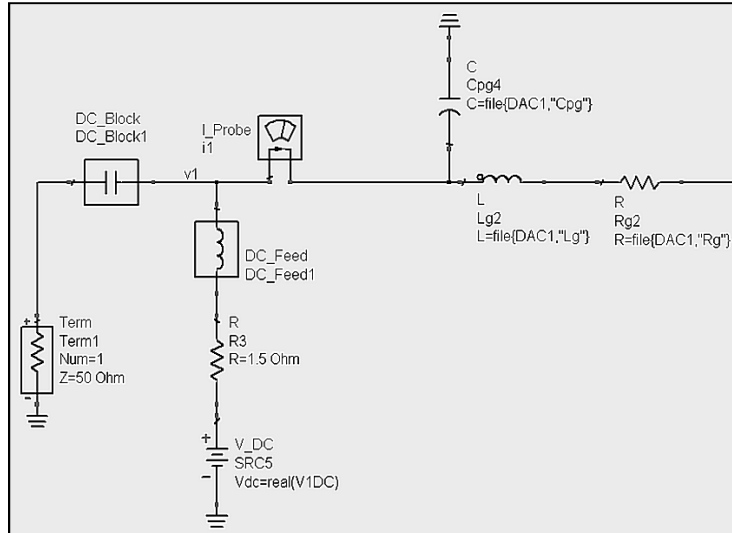


Figure 5.2 The biasing network used for the S-parameter is terminated in a 50Ω load to represent the terminals of the VNA. The extrinsic parameters are saved in a text file, which is imported using a DAC.

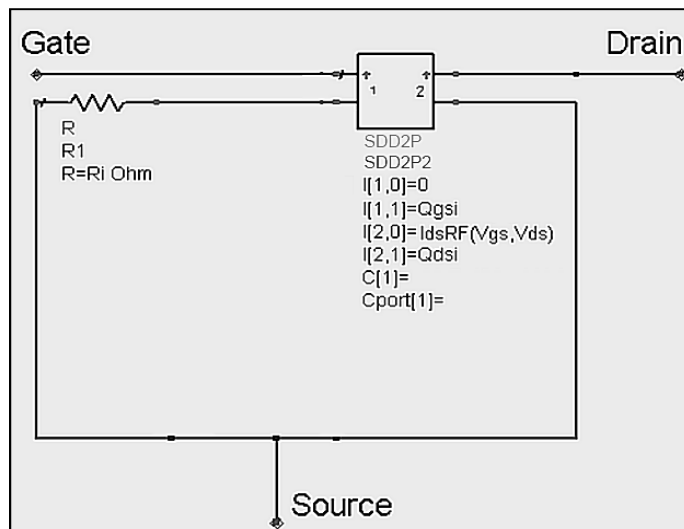


Figure 5.3 The SDD used to implement the intrinsic parameters of the nonlinear model. The charge sources are imported using a DAC, while the drain current source is implemented using analytical functions.

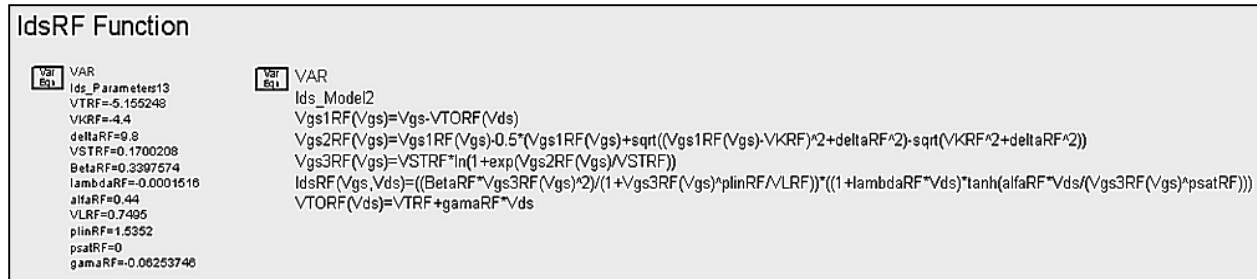


Figure 5.4 The technique used to implement the nonlinear current source I_{dsi} as an analytical function in ADS.

5.4 Nonlinear Model Verification

In this section, the verification and performance of the proposed nonlinear models are evaluated. The verifications include small-signal S-parameter, large-signal single-tone and two-tone IMD predictions. A wide range of devices was measured. However, it is not meaningful to show all the results, so for a fair evaluation, only the smallest and largest device will be demonstrated. The smallest device is a two-finger T_{02} device with a gate width of $2 \times 50 \mu\text{m}$ and the largest device is a four-finger T_{12} device with a gate width of $4 \times 150 \mu\text{m}$.

Error functions were used to evaluate the performance of the T_{02} device over a wide range of bias points, while a typical Class-AB operating point was selected to demonstrate the model accuracy. The T_{12} device is not evaluated over a wide range of bias points, as the yield of the device on the wafer is relatively poor and degradation must be considered. Thus, only a typical Class-AB operation point is evaluated for the T_{12} device. With the S-parameter predictions, a bias point below pinch-off is used to verify the model under a pinch-off condition for both the T_{02} and T_{12} devices.

5.4.1 Linear S-Parameters

The S-parameter modelling error for the T_{02} device is shown in Figure 5.5, where (a) S_{11} , (b) S_{12} , (c) S_{21} and (d) S_{22} represent the modelling error as a function of the gate V_{gs} and drain V_{ds} voltages. From the figures, it can be seen that the error is the smallest in the region where V_{gs} is smaller than -5.4V . In this region, the device is in the pinch-off condition and the drain current is equal to zero. The nonlinear model now only consists of the charge gate Q_{gsi} and drain Q_{gsi} charge sources and thus the ability to predict the behaviour simplifies. However, as the biasing is increased, the device turns on and the drain current starts to increase, so the modelling error also

increases. The increase in error can be attributed to the error relating to the integration starting point discussed in section 4.5.1. The integration starting point for the nonlinear current and charge functions was taken at a low drain voltage, where V_{gs0} is equal to -8V and large drain voltage V_{ds0} equal to 10V. The result is that the integration error increases as the gate voltage increases, with drain voltage decreasing, corresponding to the trends seen in Figure 5.5(a) to (d). In order to relate the relative values of the error functions, the performance of the T_{02} device is evaluated under a pinch-off and Class-AB operating region, which will be demonstrated in Figure 5.6 to Figure 5.13. Figure 5.6 to Figure 5.9 shows the predicted versus measured magnitude and phase S-parameters values of the T_{02} device in a pinch-off condition. From the plots, it can be seen that the predicted values for S_{11} , S_{12} , S_{21} and S_{22} are very accurate, compared to the measured values. However, above 30GHz, there is a slight deviation, but comparing the relative values, the error is still small.

For the T_{12} device, only two points are evaluated, the first is pinch-off, which is shown in Figure 5.14 to Figure 5.17 and a Class-AB operating point shown in Figure 5.18 to Figure 5.21. Evaluating both of these bias points, it can be seen that the modelled values of S_{12} , S_{21} and S_{22} are very accurate, compared to the measured values. However, S_{11} is not as accurate, but the errors are still relative small. An observation is that the S-parameter prediction of the T_{12} device also deviates slightly over 30 GHz, but once again the error is relatively small and does not have a degrading effect on the overall performance of the model.

The overall performance of the nonlinear S-parameter predictions for both the T_{02} and T_{12} device proves to be very accurate up to 30GHz with a relatively small deviation up to 40GHz. In conclusion, the S-parameter predictions for both the T_{02} and T_{12} device are very accurate and in the next section the large-signal single-tone performance of the devices is evaluated.

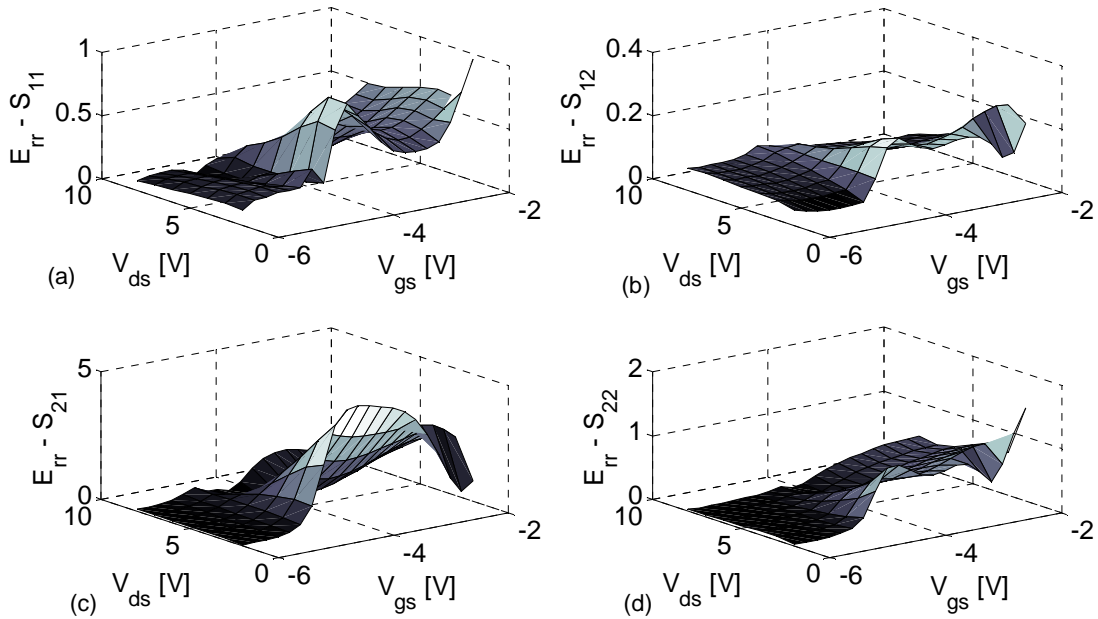


Figure 5.5 The S-parameter error made in modelling (a) S_{11} (b) S_{12} (c) S_{21} (d) S_{22} as a function of the gate voltage V_{gs} , and drain voltages V_{ds} .

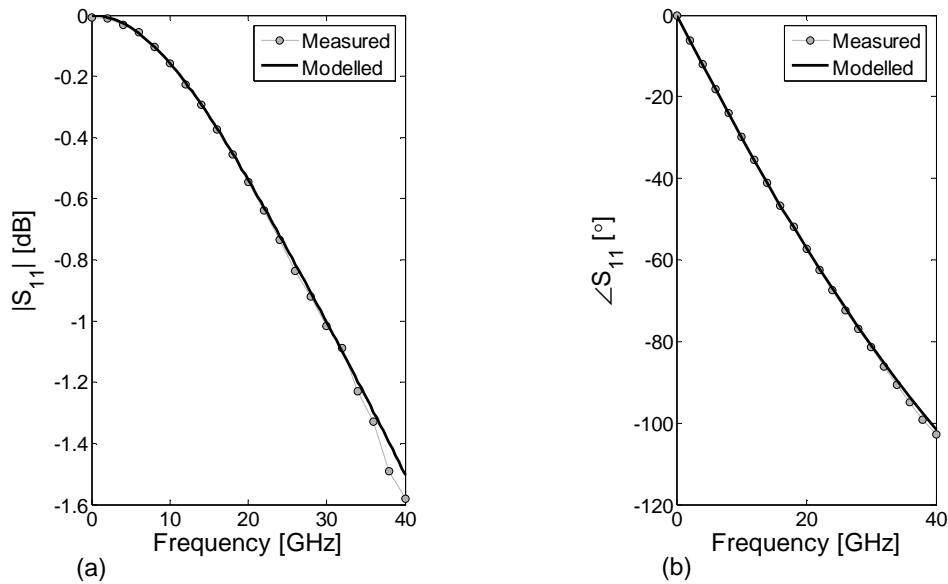


Figure 5.6 The measured and modelled plots of the magnitude (a) and phase (b) of S_{11} versus frequency of the T_{02} device biased in a pinch-off condition ($V_{gs} = -6V$, $V_{ds} = 8V$). The grey circled line represents the measured data, while the solid line represents the modelled prediction.

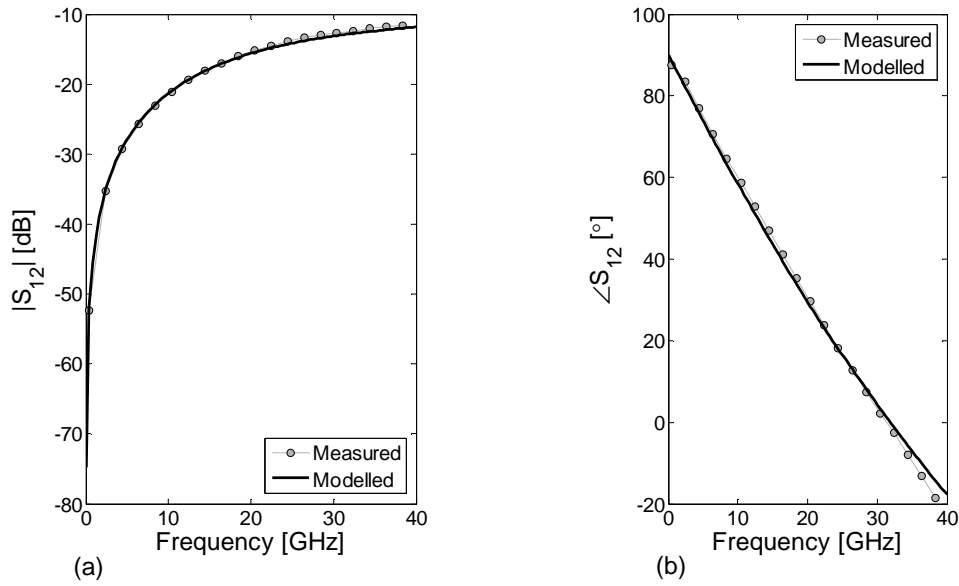


Figure 5.7 The measured and modelled plots of the magnitude (a) and phase (b) of S_{12} versus frequency of the T_{02} device biased in a pinch-off condition ($V_{gs} = -6V$, $V_{ds} = 8V$). The grey circled line represents the measured data, while the solid line represents the modelled prediction.

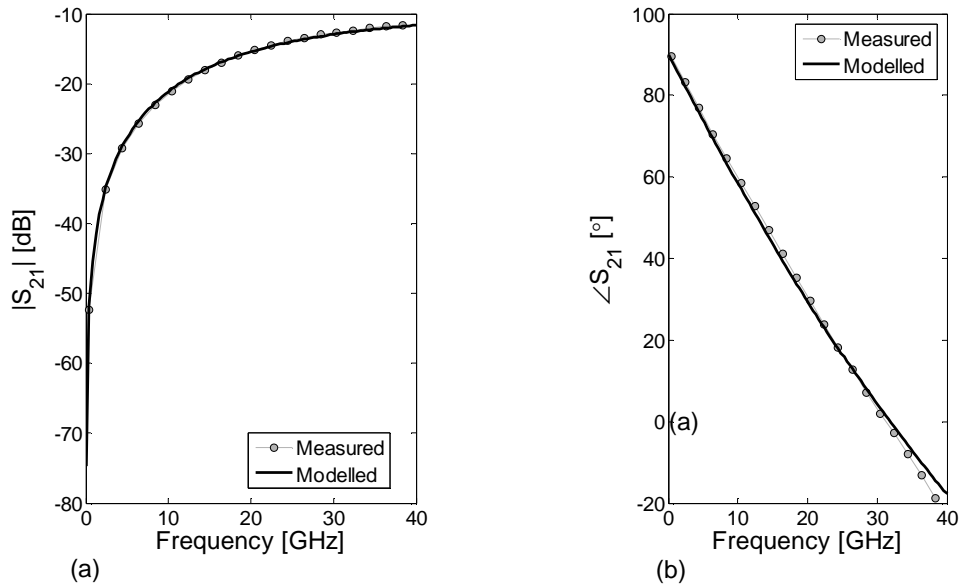


Figure 5.8 The figures show the plots of the magnitude (a) and phase (b) of S_{21} versus frequency of the T_{02} device biased in a pinch-off condition ($V_{gs} = -6V$, $V_{ds} = 8V$). The grey circled line represents the measured data, while the solid line represents the modelled prediction.

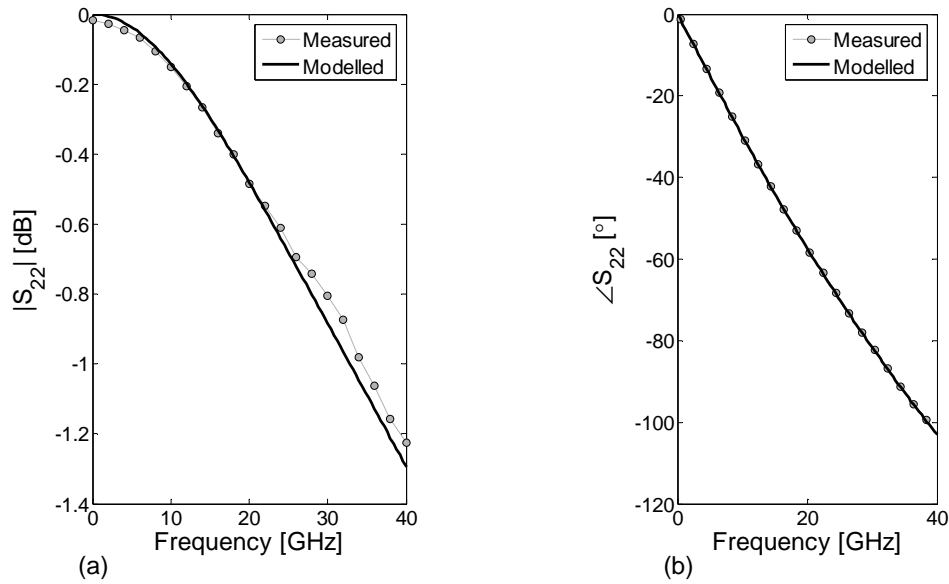


Figure 5.9 The measured and modelled plots of the magnitude (a) and phase (b) of S_{22} versus frequency of the T_{02} device biased in a pinch-off condition ($V_{gs} = -6V$, $V_{ds} = 8V$). The grey circled line represents the measured data, while the solid line represents the modelled prediction.

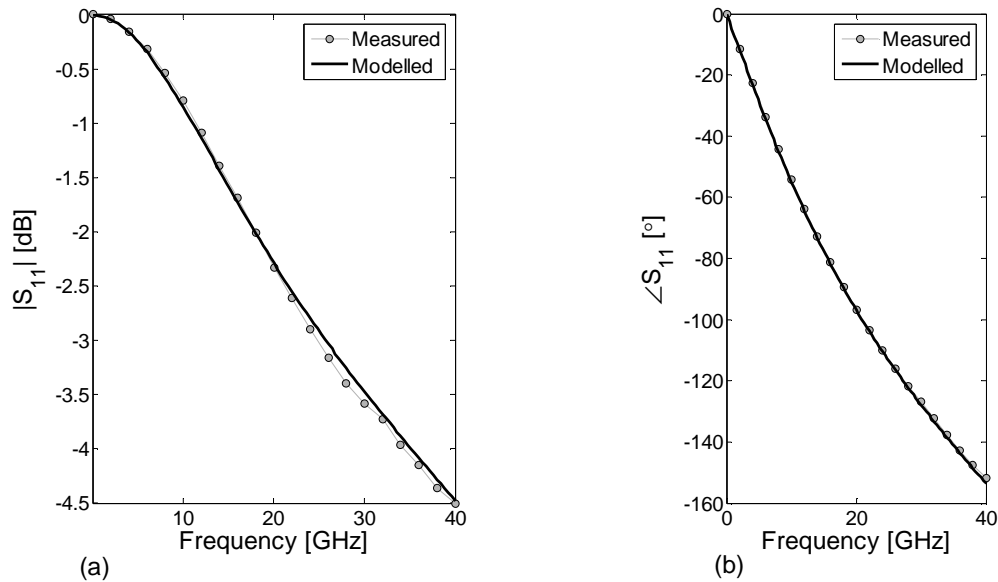


Figure 5.10 The measured and modelled plots of the magnitude (a) and phase (b) of S_{11} versus frequency of the T_{02} device biased for Class-AB operation ($V_{gs} = -4V$, $V_{ds} = 8V$). The grey circled line represents the measured data, while the solid line represents the modelled prediction.

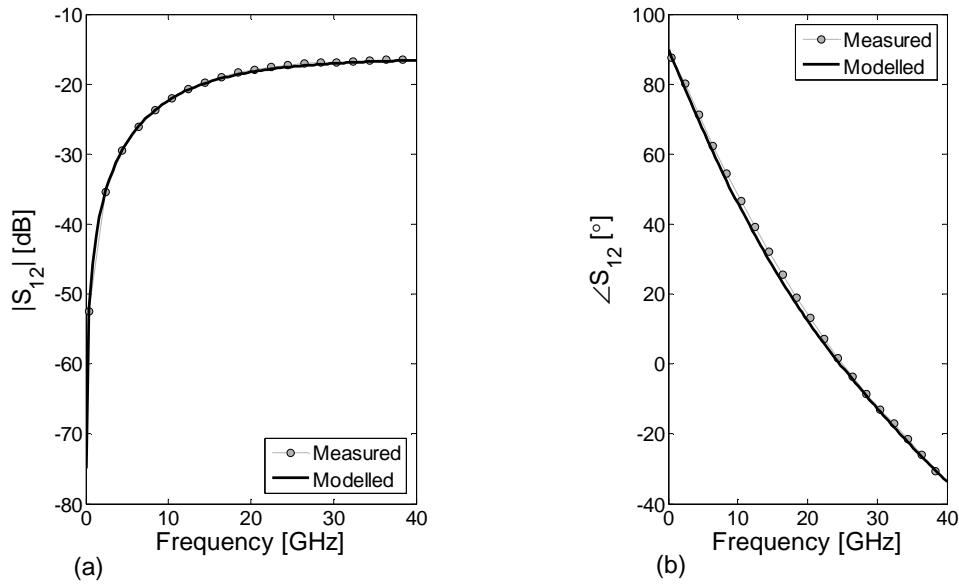


Figure 5.11 The measured and modelled plots of the magnitude (a) and phase (b) of S_{12} versus frequency of the T_{02} device biased for Class-AB operation ($V_{gs} = -4V$, $V_{ds} = 8V$). The grey circled line represents the measured data, while the solid line represents the modelled prediction.

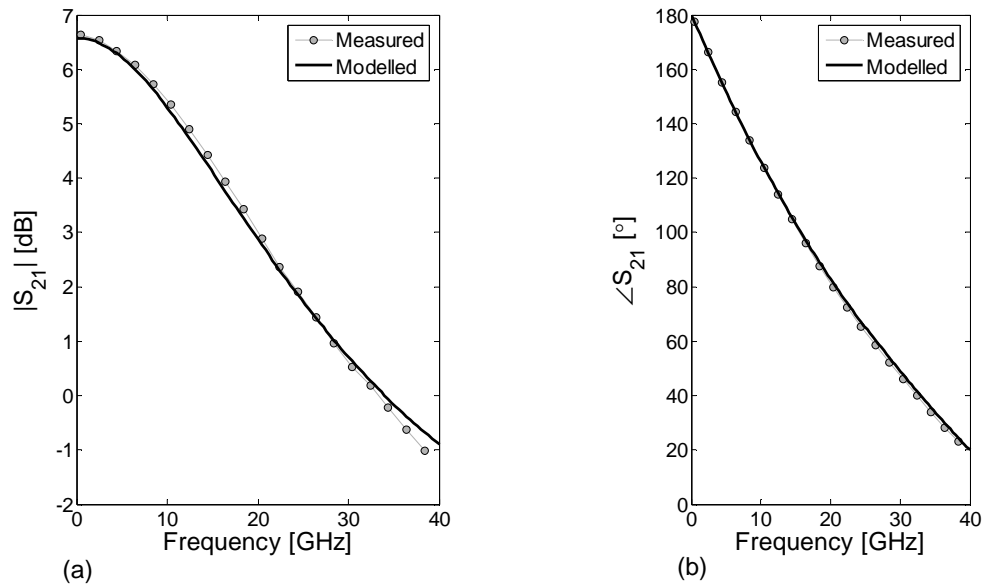


Figure 5.12 The measured and modelled plots of the magnitude (a) and phase (b) of S_{21} versus frequency of the T_{02} device biased for Class-AB operation ($V_{gs} = -4V$, $V_{ds} = 8V$). The grey circled line represents the measured data, while the solid line represents the modelled prediction.

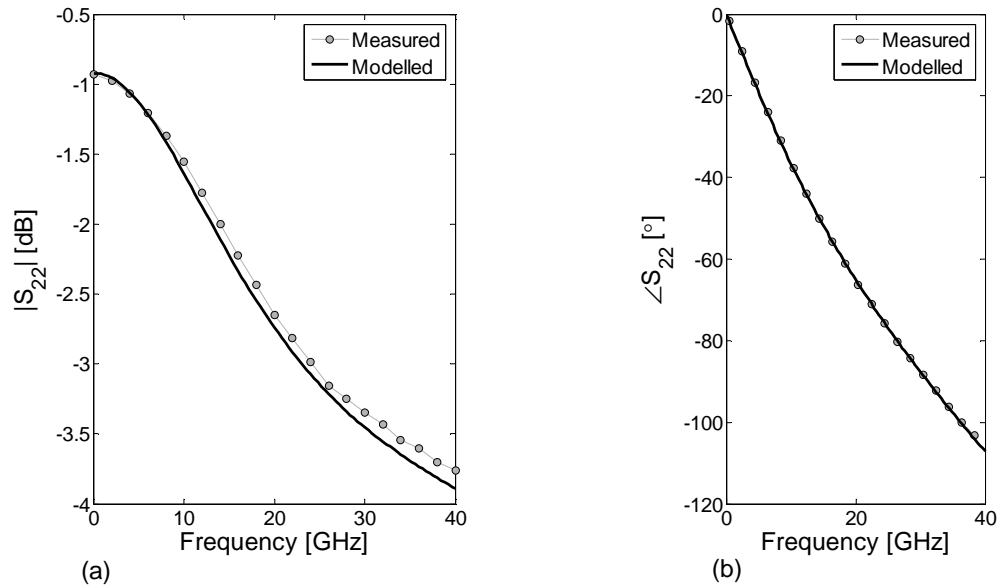


Figure 5.13 The measured and modelled plots of the magnitude (a) and phase (b) of S_{22} versus frequency of the T_{02} device biased for Class-AB operation ($V_{gs} = -4V$, $V_{ds} = 8V$). The grey circled line represents the measured data, while the solid line represents the modelled prediction.

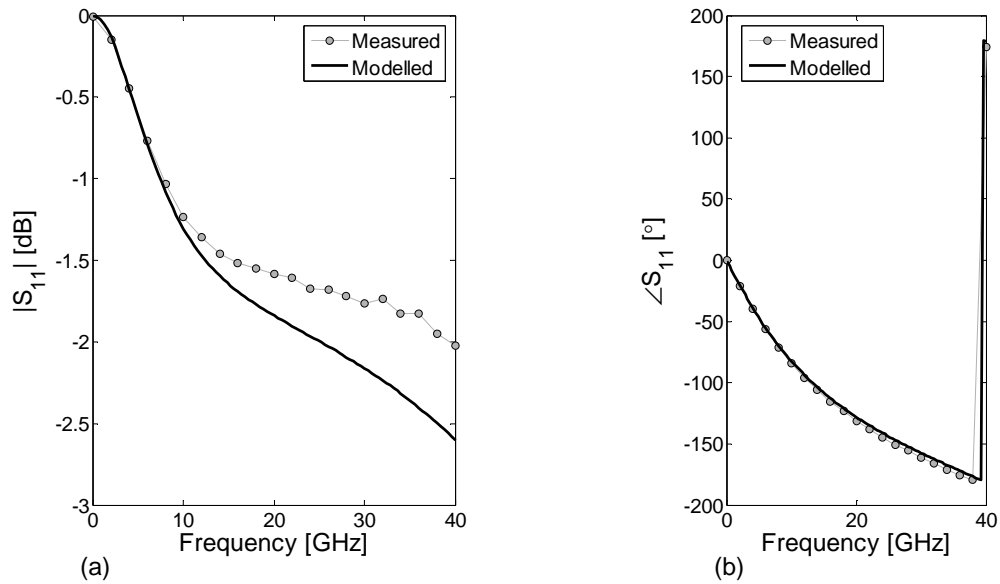


Figure 5.14 The measured and modelled plots of the magnitude (a) and phase (b) of S_{11} versus frequency of the T_{12} device biased in a pinch-off condition ($V_{gs} = -8V$, $V_{ds} = 8V$). The grey circled line represents the measured data, while the solid line represents the modelled prediction.

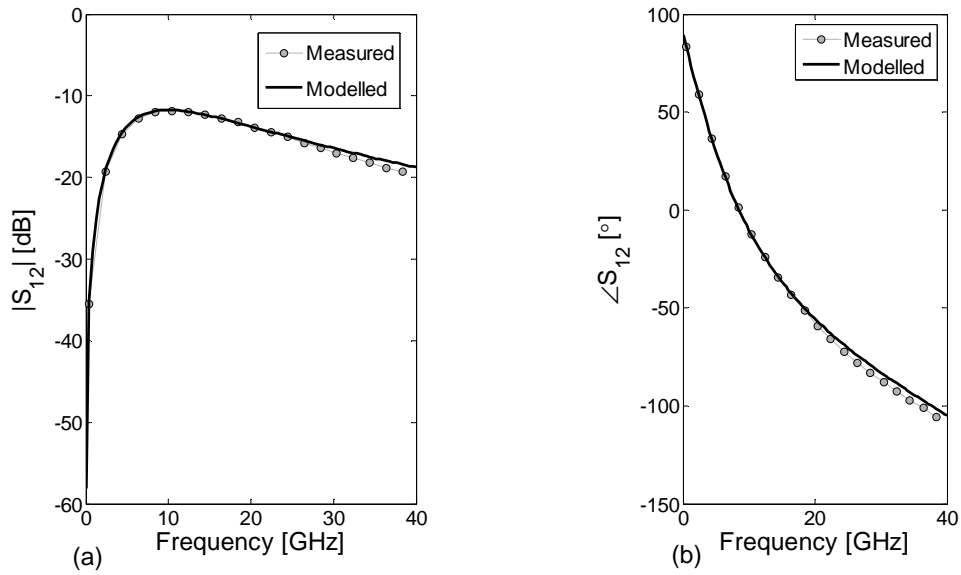


Figure 5.15 The measured and modelled plots of the magnitude (a) and phase (b) of S_{12} versus frequency of the T_{12} device biased in a pinch-off condition ($V_{gs} = -8V$, $V_{ds} = 8V$). The grey circled line represents the measured data, while the solid line represents the modelled prediction.

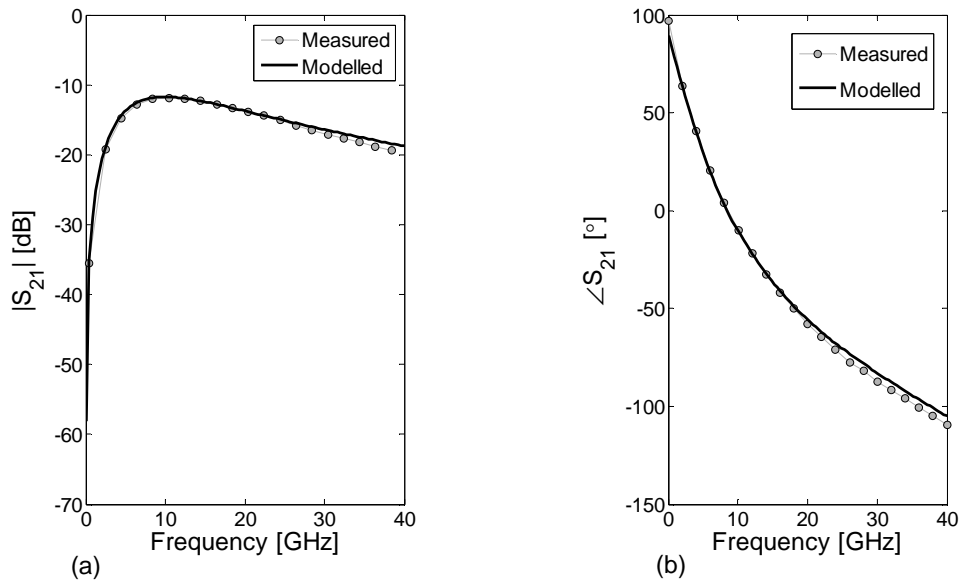


Figure 5.16 The measured and modelled plots of the magnitude (a) and phase (b) of S_{21} versus frequency of the T_{12} device biased in a pinch-off condition ($V_{gs} = -8V$, $V_{ds} = 8V$). The grey circled line represents the measured data, while the solid line represents the modelled prediction.

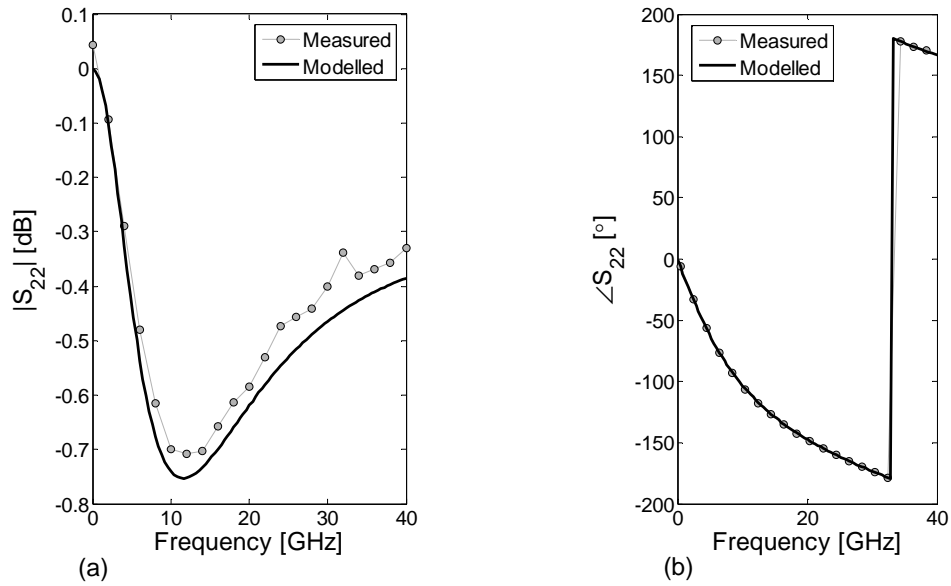


Figure 5.17 The measured and modelled plots of the magnitude (a) and phase (b) of S_{22} versus frequency of the T_{12} device biased in a pinch-off condition ($V_{gs} = -8V$, $V_{ds} = 8V$). The grey circled line represents the measured data, while the solid line represents the modelled prediction.

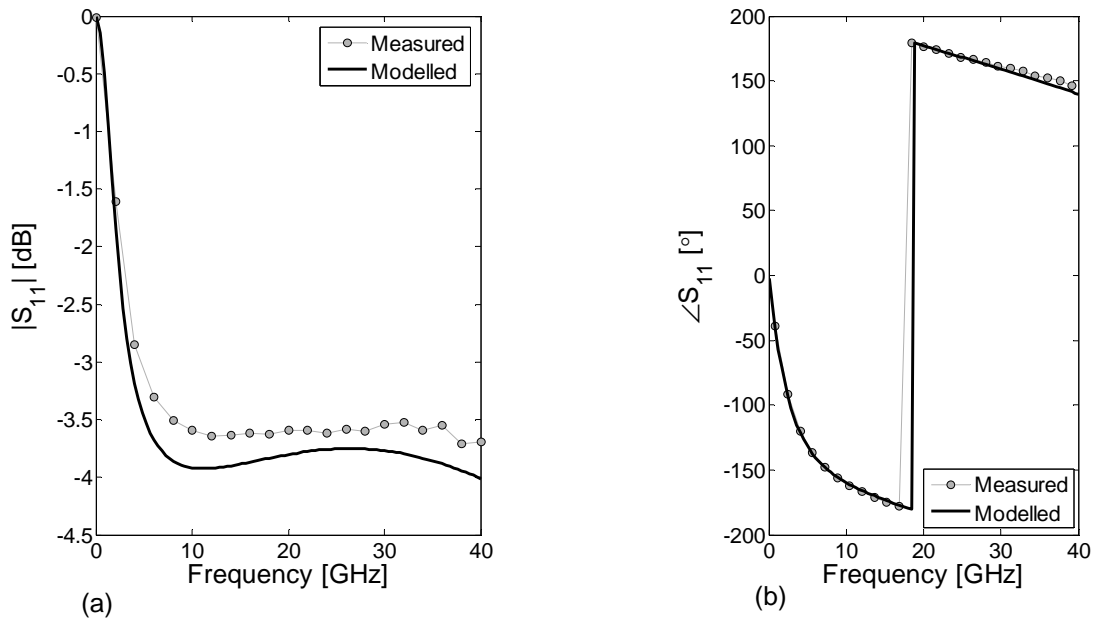


Figure 5.18 The measured and modelled plots of the magnitude (a) and phase (b) of S_{11} versus frequency of the T_{12} device biased for Class-AB operation ($V_{gs} = -4V$, $V_{ds} = 8V$). The grey circled line represents the measured data, while the solid line represents the modelled prediction.

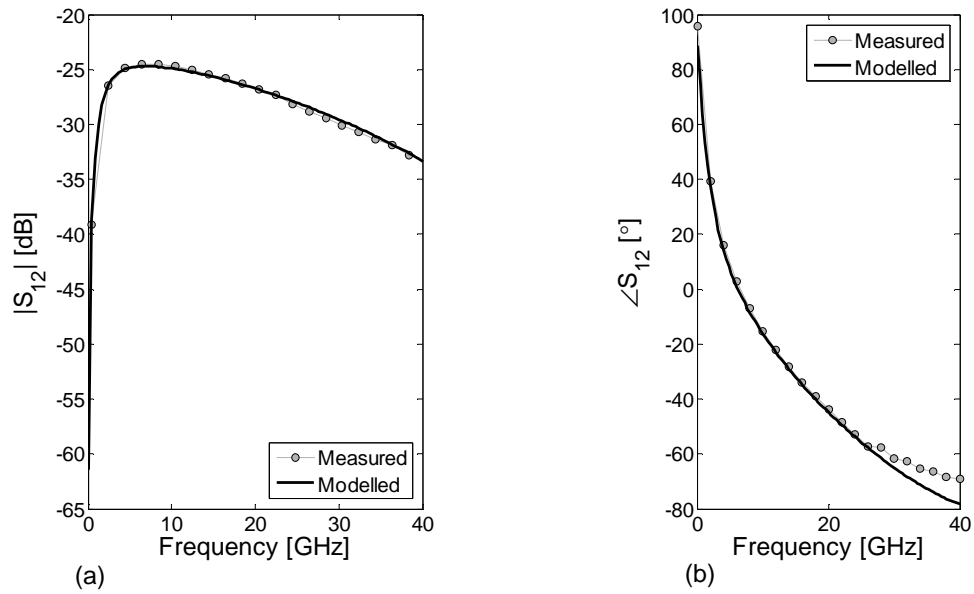


Figure 5.19 The measured and modelled plots of the magnitude (a) and phase (b) of S_{12} versus frequency of the T_{12} device biased for Class-AB operation ($V_{gs} = -4V$, $V_{ds} = 8V$). The grey circled line represents the measured data, while the solid line represents the modelled prediction.

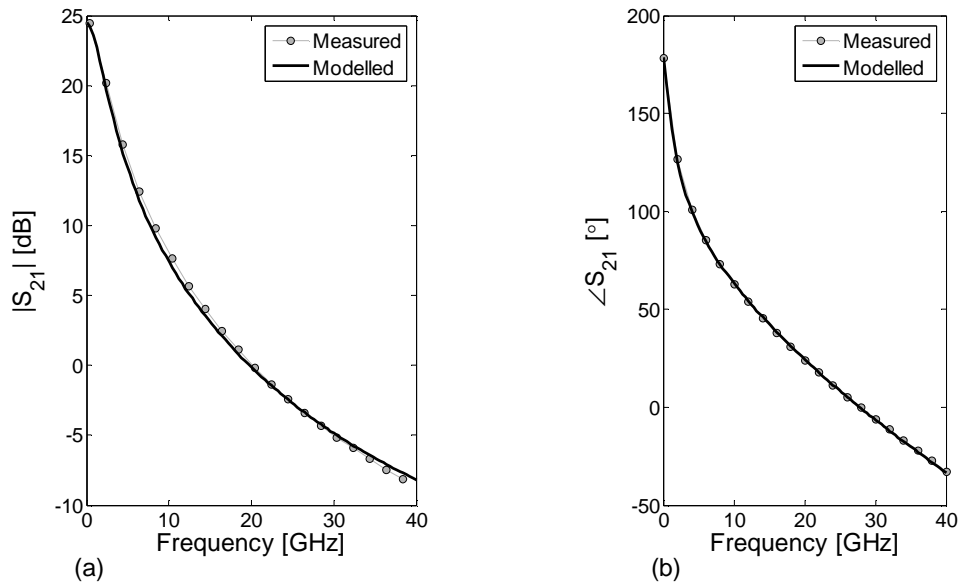


Figure 5.20 The measured and modelled plots of the magnitude (a) and phase (b) of S_{21} versus frequency of the T_{12} device biased for Class-AB operation ($V_{gs} = -4V$, $V_{ds} = 8V$). The grey circled line represents the measured data, while the solid line represents the modelled prediction.

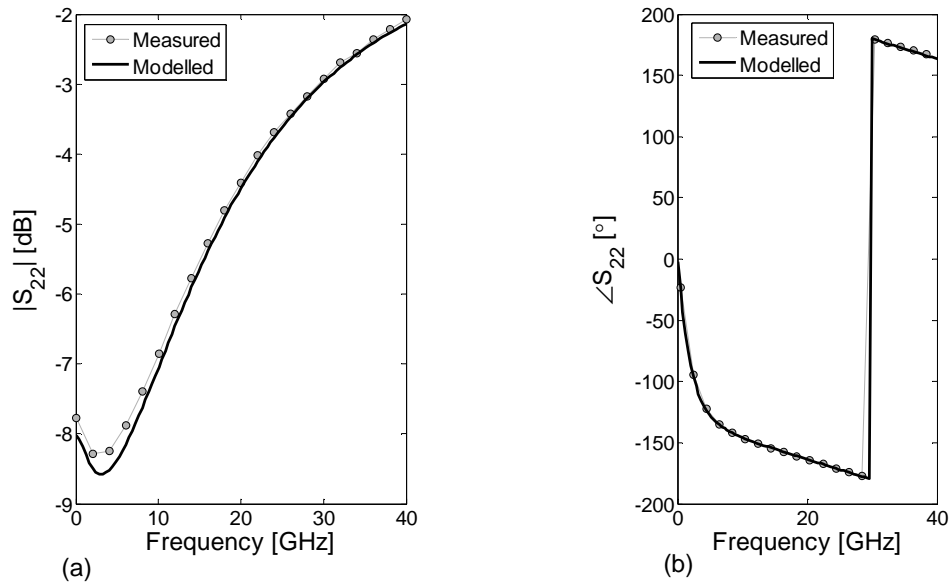


Figure 5.21 The measured and modelled plots of the magnitude (a) and phase (b) of S_{22} versus frequency of the T_{12} device biased for Class-AB operation ($V_{gs} = -4V$, $V_{ds} = 8V$). The grey circled line represents the measured data, while the solid line represents the modelled prediction.

5.4.2 Large-Signal Single-Tone

The validation of the large-signal response is obtained by comparing measurements taken from the LSNA to the model predictions simulated in ADS. The highest measurable frequency of the LSNA measurement setup is 20GHz, thus a fundamental frequency of 2GHz is chosen to be able to measure a sufficient number of harmonics. The first, second and third output harmonics of the models are determined as a function of input power and are verified against measured data. The T_{02} device is evaluated using error functions and a typical Class-AB operating point is selected to demonstrate the model accuracy. With the T_{12} device, only a Class-AB operating bias point is demonstrated, as the procedure to construct error functions requires multiple points, which could lead to device degradation or even failure.

Figure 5.22 shows the bubble plot of the error function for the T_{02} device with the gate biased from -5V to -2V, and a drain voltage from 2V to 10V. A lower gate voltage limit of -5V is selected, as in this region the device is operating in a Class-B mode. An upper gate voltage limit of -2V is used to evaluate the device in a Class-A operating mode. When evaluating Figure 5.22 it can be seen that that the error decreases from V_{gs} is equal to -5V, which is the Class-B mode, to -2V in the Class-A mode. The modelling error in the Class-B mode is expected to be fairly inaccurate, as the device is starting to conduct and the device's nonlinear behaviour is at its

highest. As the biasing increases to a Class-AB mode, where V_{gs} is equal to $-4V$, so the nonlinear behaviour decreases and the model has a more accurate prediction. When the biasing is further increased in a Class-A operating region, the nonlinear behaviour is small, as the device is in a linear operating region, which can be clearly seen with the decrease in circle diameter where V_{gs} is equal to $2V$. In order to obtain a fair result, a Class-AB operating point is selected to demonstrate the accuracy of nonlinear model predictions. Figure 5.23(a) magnitude, (b) phase shows the plot of simulated input power, P_{in} , versus output power, P_{out} of the fundamental, second harmonic and third harmonic compared to the measured values for the T_{02} device biased for Class-AB operation. Figure 5.24 shows the instantaneous voltage and current wave forms with an input power P_{in} equal to $2.45dBm$ (fundamental tone f_o equal to $2GHz$). In Figure 5.23 it can be observed that the magnitude for all the harmonics is very accurate. The output phases are also fairly accurate, except for the third order harmonic, which has a deviation at the higher input power levels. It should be noted that the decrease in prediction at the lower power level is due to the resolution of the measurement setup. However, from these figures the T_{02} device model can be seen to predict the nonlinear single-tone behaviour with a high degree of accuracy.

Figure 5.25 demonstrates the comparison between simulated and measured large-signal single-tone results for the T_{12} device, while Figure 5.26 demonstrates the voltage and current wave form comparisons with an input power P_{in} equal to $12dBm$ (fundamental tone f_o equal to $2GHz$) for Class-AB operation. The model shows good results for first and second output harmonics, however there is deviation in the magnitude and phase of the third order output harmonic. This is a small deviation relative to the relative magnitudes of the second and third harmonics and, as an overall performance, is still very accurate. Comparing all the results, it can be concluded that the nonlinear models for both the T_{02} and T_{12} devices show a good ability to predict the large-signal single-tone response of the devices.

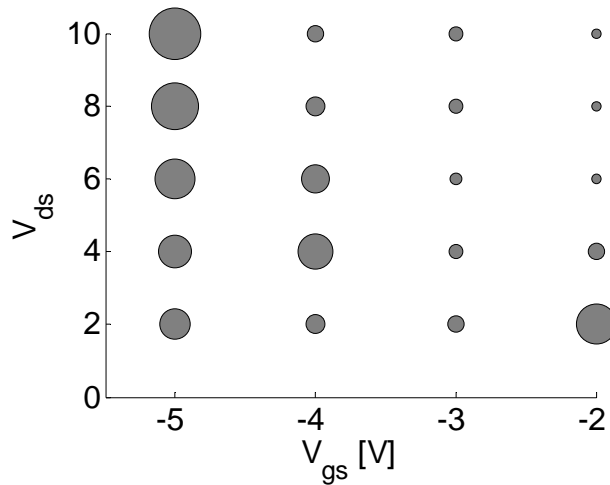


Figure 5.22 The error function of the large-signal single-tone for the T_{02} device as a function of gate V_{gs} and drain V_{ds} bias voltages.

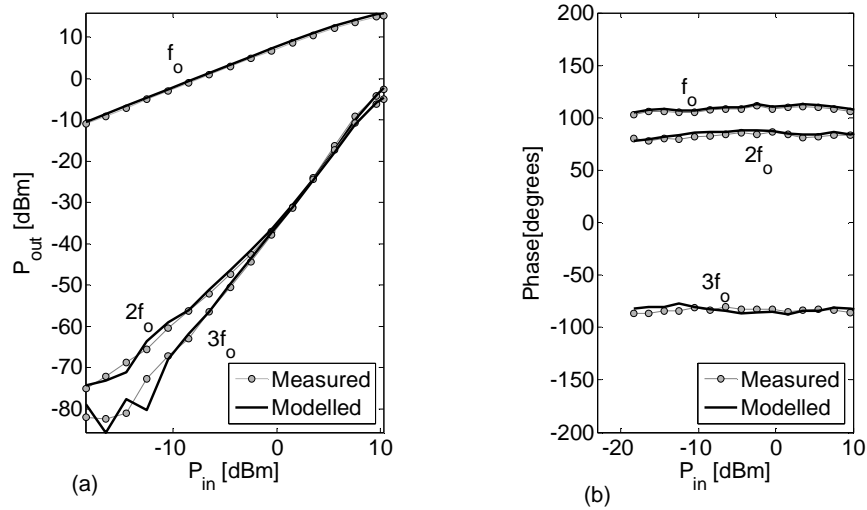


Figure 5.23 The large-signal single-tone measurements of the (a) magnitude and (b) phase for the fundamental, second and third harmonic of the T_{02} device in a Class-AB ($V_{gs} = -4V$, $V_{ds} = 8V$) operating region. The grey circled line represents the measured data, while the solid line represents the model.

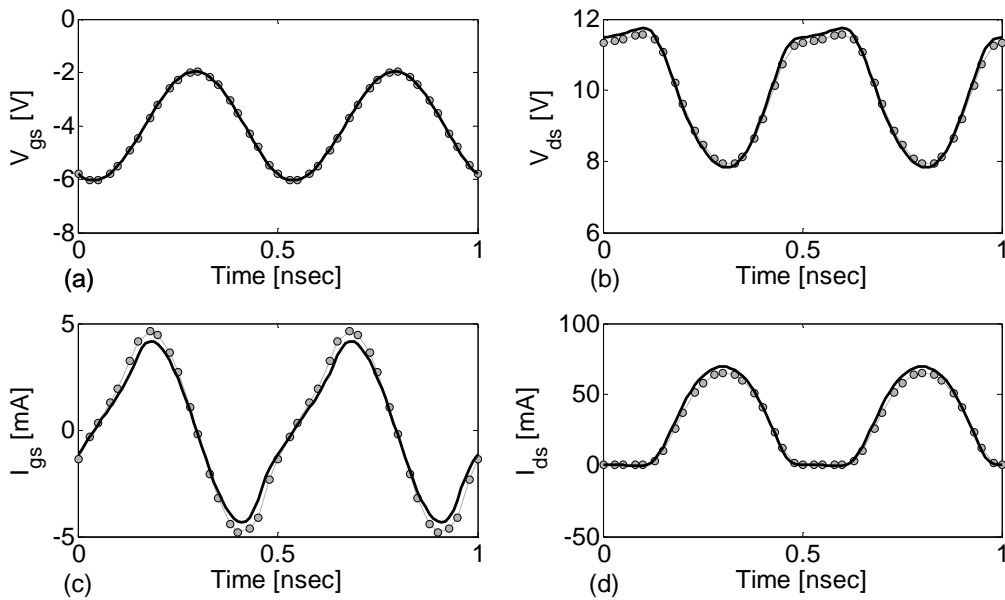


Figure 5.24 The time wave forms of the gate (a) and drain (b) voltages, as well as the gate (c) and drain (d) current wave forms of the T_{02} device in a Class-AB ($V_{gs} = -4V$, $V_{ds} = 8V$) operating region. The grey circled line represents the measured data, while the solid line represents the model predictions.

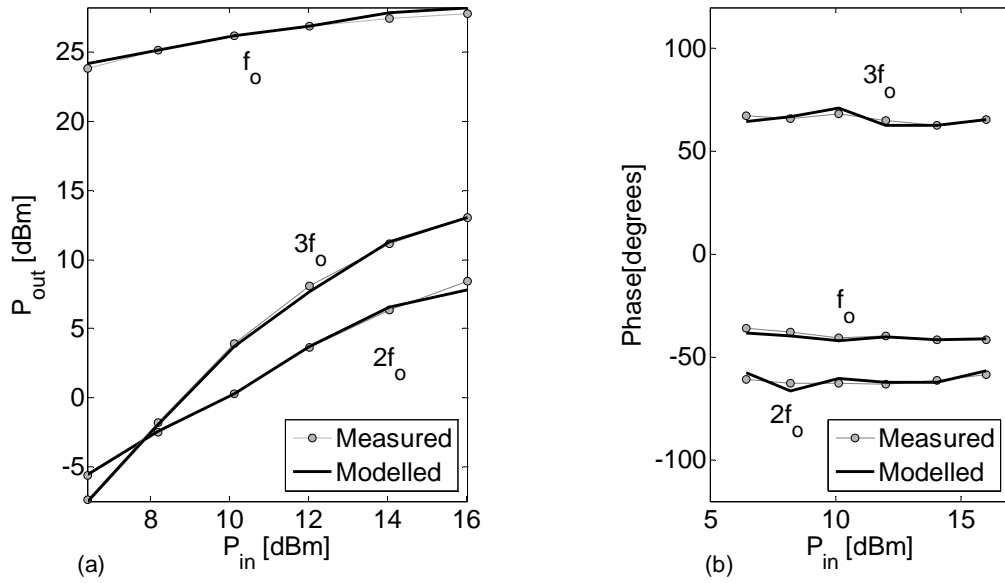


Figure 5.25 The large-signal single-tone measurements of the (a) magnitude and (b) phase for the fundamental, second and third harmonic of the T_{12} device in a Class-AB ($V_{gs} = -4V$, $V_{ds} = 8V$) operating region. The grey circled line represents the measured data, while the solid line represents the model predictions.

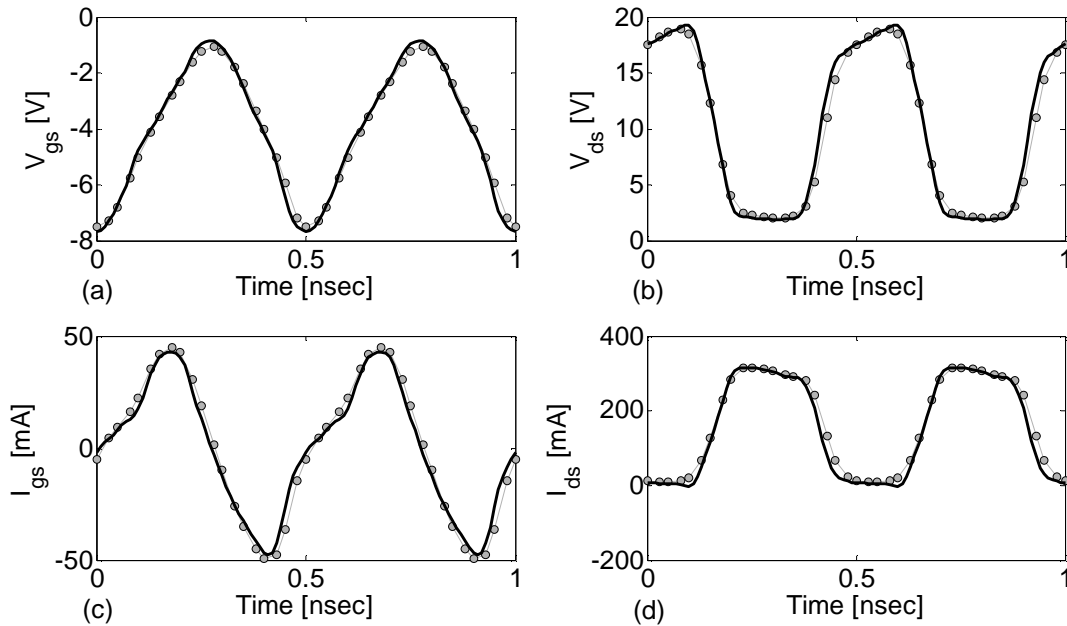


Figure 5.26 The time wave forms of the gate (a) and drain (b) voltages, as well as the gate (c) and drain (d) current wave forms of the T_{12} device in a Class-AB ($V_{gs} = -4V$, $V_{ds} = 8V$) operating region. The grey circled line represents the measured data, while the solid line represents the model predictions.

5.4.3 Large-Signal Two-Tone IMD

The LSNA measurement setup was also used to verify the IMD predictions. The measurement is done by generating two input tones at a centre frequency of 1GHz and tone separation of 200KHz. The T_{02} device was evaluated at a single drain voltage point where V_{ds} is equal to 8V, while the gate voltage V_{gs} is swept from -5V to -3V. The T_{12} device, however, is only evaluated at a single gate and drain voltage point. The devices were only measured at these specific points, as at this stage, S-parameter and large-signal single-tone measurements have been performed on the devices. Performing the two-tone measurements at too many points could lead to device degradation or complete failure.

Equation (5.3) is used to evaluate the IMD modelling error between the measured and simulated predictions of the T_{02} device. The gate voltage V_{gs} is swept steps from -5V to -3V, at a constant drain voltage V_{ds} equal to 8V as shown in Figure 5.27. It can be observed that error decreases from -5V to -3V. This observation corresponds with the results seen in the single-tone case, where the least accurate prediction is in the Class-B mode and the most accurate is in the Class-A mode. As stated before, the device is at its most nonlinear in the class-B operating mode, which is at -5V. As the voltage increases, so the nonlinear behaviour of the device also decreases. In the class-A mode at V_{gs} equal to -3V, the prediction is the most accurate. As with the previous predictions, a class-AB (V_{gs} equal to -4V, V_{ds} equal to 8V) operating point is selected to demonstrate the accuracy of the nonlinear models, which is presented in Figure 5.28. The input power P_{in} , is swept from -15dBm to 5dBm with ten evenly spaced points in between. Figure 5.28 compares the nonlinear model predictions generated in ADS to the measured values taken from the LSNA, which demonstrates an accurate level of IMD predictions. The accuracy of the IMD predictions can be attributed to the extraction of the nonlinear coefficients, which are implemented in the drain current formulation as demonstrated in chapter three.

Figure 5.29 shows the IMD prediction for the T_{12} device for a Class-AB operating mode (V_{gs} equal to -4V, V_{ds} equal to 8V). The input power levels of the T_{12} device are evaluated at higher input levels, but with only five points in between, where P_{in} is swept from 3dBm to 12dBm. The predictions are not as accurate as that of the T_{02} model, but are still highly accurate compared to the measured values, proving that the implementation of the extracted nonlinear coefficients lead to improved intermodulation predictions.

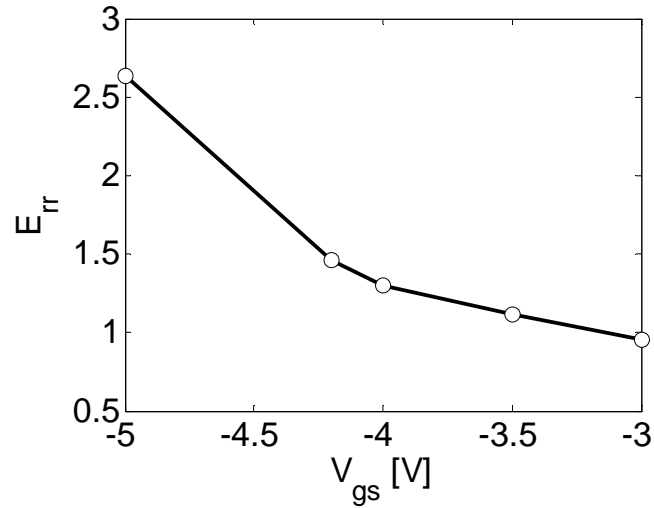


Figure 5.27 The error function of the large-signal two-tone prediction for the T_{02} device, where the gate voltage V_{gs} is increased from -5V to -3V with a constant drain voltage $V_{ds} = 8V$.

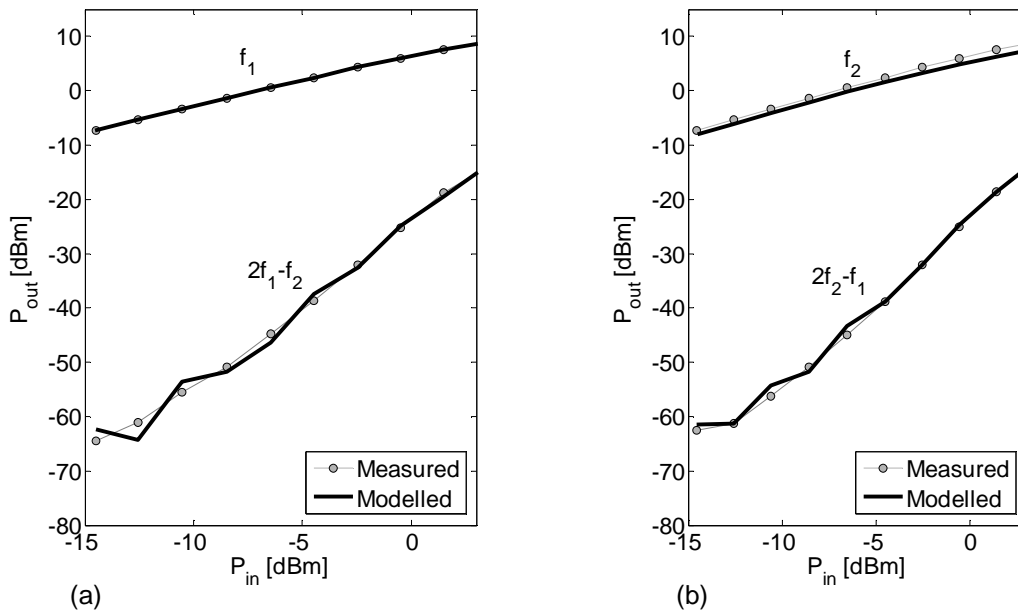


Figure 5.28 The figure shows the (a) lower and (b) upper IMD products of the T_{02} device in a Class-AB ($V_{gs} = -4V$, $V_{ds} = 8V$) operating region. The grey circled line represents the measured data, while the solid line represents the model predictions.

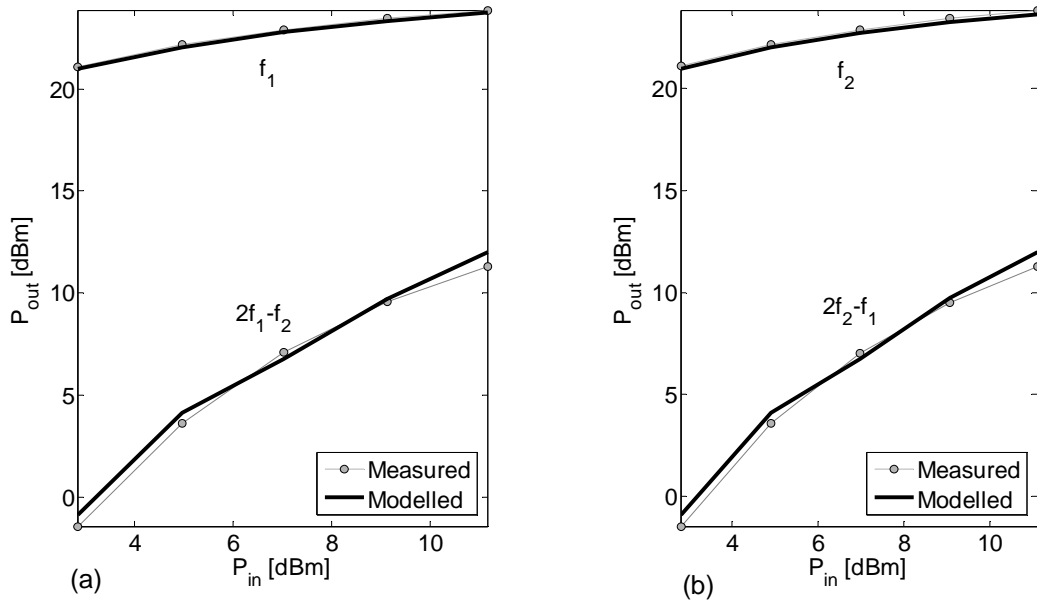


Figure 5.29 The figure shows the (a) lower and (b) upper IMD products of the T_{12} device in a Class-AB ($V_{gs} = -4V$, $V_{ds} = 8V$) operating region. The grey circled line represents the measured data, while the solid line represents the model predictions.

5.5 Conclusion

In this chapter, the nonlinear models proposed for the on-wafer GaN HEMT devices were verified by evaluating the ability of the models to predict the linear and nonlinear behaviour. The T_{02} and T_{12} devices were evaluated as these are the smallest and largest devices measured. Error functions were used to determine the modelling error over a wide range of bias points for the T_{02} device, while the T_{12} device was only evaluated at a single point due to poor yield on the wafer.

Error functions were used to model prediction error of the T_{02} device over a wide range of points. Only two points were used to evaluate the device's small-signal behaviour, which were in pinch-off and Class-AB. Both the models predicted the small-signal behaviour in each of the regions with good a level of agreement up to 30GHz, but showed a slight deviation above 30GHz. The models produced extremely accurate magnitude and phase predictions for S_{21} for the Class-AB condition, which is the typical region in which these devices operate. The T_{12} device had a slight problem predicting S_{11} , but still showed good accuracy for the rest of the S-parameter predictions.

The accuracy of the nonlinear model prediction of the single-tone harmonic power and phase as a function of input power was evaluated for Class-AB operation for the T_{02} and T_{12} devices. The simulation prediction for the Class-AB mode for both the devices was able to predict the output power with good accuracy. The magnitude prediction up to the third harmonic showed good agreement to the measured values and the phase prediction also showed good agreement up to the second harmonic, but could not predict the third order phase with reasonable accuracy.

The IMD predictions for both the T_{02} and T_{12} devices were evaluated for a Class-AB operating bias point. Both models produced extremely accurate predictions for the Class-AB operation modes. In conclusion, the models were found to predict the overall linear and nonlinear behaviour of the on-wafer GaN device with good accuracy.

CHAPTER 6

Conclusion

6.1 Introduction

The focus of this thesis is to develop nonlinear models for on-wafer gallium nitride (GaN) high-electron mobility transistor (HEMT) devices, with the main goal of implementing the models in Agilent's Advanced Design System (ADS). The development included the investigation of different model topologies and the characterising of the transistor devices. The nonlinear models were implemented in ADS, where the measured results were compared to the model predictions. An intermodulation distortion (IMD) measurement setup was developed, which is used to directly extract the higher order derivatives of the drain current nonlinearity and improves the IMD predictions. The proposed nonlinear model is able to predict the linear and nonlinear behaviour of the devices with a high degree of accuracy. The goal of this chapter is to give an overview of the individual achievements of the work presented. The content and outcome of each chapter is listed and possible future developments are discussed.

6.2 Overview and Conclusions

In chapter one, an overview of the various nonlinear modelling techniques is given to ensure a basic understanding of the different methods, as well as the reason behind selecting the technique used in this work. Chapter two is dedicated to providing insight into the GaN HEMT devices modelled, with a description of the characterisation and device selection process. The chapter also details the various measurement instruments used to characterise the devices and verify proposed nonlinear models in this work. Knowledge of the basic operation of each instrument is needed to ensure that reliable and accurate measurements are obtained, as the nonlinear models are derived from the measurements.

Chapter three describes a low frequency IMD measurement setup that measures the second and higher order intermodulation performance of the nonlinear current source $I_{ds}(V_{gs}, V_{ds})$. From these measurements, the higher order derivatives and cross-derivatives of I_{ds} with respect to V_{gs}

and V_{ds} can be extracted directly. The current derivatives are vital in the construction of models that can accurately predict nonlinear IMD. The extracted coefficients are used later in chapter four to create an analytical drain current function that improves IMD predictions. Chapter three also gives an overview of the Volterra series analysis techniques used to extract the Taylor series coefficients.

The purpose of chapter four is to detail the nonlinear model formulation of the on-wafer GaN HEMT devices. Firstly, the determination of the linear small-signal equivalent circuit model topology is detailed, as well as the extraction procedure. The determination of the equivalent circuit parameters is extremely important as these parameters are used as a basis in the formulation of the nonlinear models and thus an optimisation-based extraction tool is utilised. However, the main focus of chapter four is to present the nonlinear modelling methodology process, which starts off with the derivation of the quasi-static nonlinear model. A Matlab program is developed that determines the table-based integration functions. The next step in the process is representing the drain current source I_{dsi} with an analytical function. The function used is known as the Fager model and another Matlab program is used to optimise the model parameters. The IMD coefficient data extracted in chapter three is then incorporated into the function. Different aspects of the nonlinear model are investigated to better understand what would work best for an on-wafer GaN HEMT device. Finally, a nonlinear model is presented that incorporates the drain current derivatives into the analytical drain current function. The addition of the derivative information leads to a nonlinear model that improves the S-parameter, large-signal single-tone and large-signal two IMD predictions.

In chapter five the nonlinear models derived in chapter four are implemented in ADS, where the device measurements are compared to model predictions. The chapter also gives an overview of the techniques used to implement the nonlinear models in ADS. The main focus of the chapter is to evaluate the ability of the models to predict the linear and nonlinear behaviour of the devices. The performance of the models is evaluated over a wide range of bias points by implementing error functions in the simulations. The model performance is validated by comparing the measured results of the small-signal S-parameter prediction, large-signal single-tone and two-tone IMD to the model prediction. The T_{02} and T_{12} device topologies are evaluated, as these are the smallest and largest devices measured, while a typical Class-AB operating point is selected to demonstrate the performance of the models. A very large portion of the work was aimed at developing the necessary infrastructure required to perform experiments. Measurement automation software was also developed to ensure fast and accurate implementation of models. Error functions are used to evaluate the performance of the T_{02} device over a wide range of bias points, while only a single point in a Class-AB operating region is demonstrated for the T_{12} device. With the T_{12} device, only a limited number of operational devices were found on the wafer and, for the sake of preserving the device, only a single point is selected to perform the measurements. When comparing the measured values of the linear S-parameter, nonlinear large-

signal single-tone and two-tone IMD to the model predictions, it can be concluded that the proposed models are highly accurate and definitely suited for the GaN HEMT technology.

6.3 Future Work and Recommendations

The GaN HEMT technology is relatively new on the market and the subject of nonlinear models has yet to be fully explored. The purpose of this thesis is to create a basis for future developments, ideas of possible future work will be presented in the following section.

The first possible area of improvement is the study of thermal effects relating to the modelling process, which was neglected in this work due to the necessary equipment not being available. The study would include extensive temperature testing, which would have to be conducted in a controlled system. The modelling function would now add an extra parameter, which is a function of temperature. The next area of study would be to implement the adaptive multi-bias S-parameter measurement algorithm to perform the device characterisation. The advantage of using the algorithm is that areas where the device characteristics change rapidly are identified and a number of new user-specified bias points can be added in the required regions. The nonlinear drain current I_{ds} was modelled using an analytical model first implemented by Fager and the charge sources as table-based models. The next step would be to implement the charge sources with analytical functions. The final step is to use a vector-fitting technique to model the nonlinear charge and current functions. The advantage of vector fitting is that the functions will generate a smooth curve, eliminating noisy data.

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