High Power LDMOS L-Band Radar Amplifiers

by

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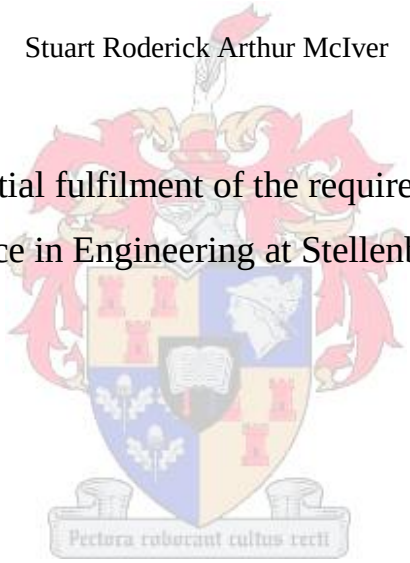

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Declaration

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Abstract

The thesis details the design, construction and experimental evaluation of 30W, 35W and 250W L-Band LDMOS Radar amplifiers. Each amplifier module contains an integrated high speed power supply in order to optimize RF pulse repeatability and to improve radar MTI factor (Moving Target Indication.) As part of the work, a pulsed RF measurement system for measuring the dynamic I-V curves of a power FET was developed. Work was also done on low impedance S-parameter measurement test fixtures for the characterisation of power FETs. These measurement systems generated design information which was used in the development of the L-Band power amplifiers.

Opsomming

Hierdie tesis beskryf die ontwerp, bou en experimentele evaluering van ‘n 30W, 35W en 250W L-band LDMOS radarversterker. Elke versterker bevat ook ‘n geintegreerde hoë-spoed kragbron om optimum RF pulsherhaalbaarheid te verseker en die radar se ‘MTI (Moving Target Indication)’ te verbeter. ‘n RF-pulsmetingstelsel is ook ontwikkel om die dinamiese I-V kurwes van ‘n hoë-krag FET te meet. Verder is daar ook gewerk aan ‘n toetsopstelling vir lae-impedansie S-parameters om hoë-krag FETs te karakteriseer. Hierdie toetsopstelling is gebruik om ontwerpsdata te genereer wat gebruik is in die ontwerp van die L-band kragversterkers.

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Chapter 1 – Introduction

1.1 History of Amplifiers

RF and microwave power amplifiers are widely used in applications such as wireless communications, jamming, imaging, radar and RF heating. Their development began between the late 19th century and the mid 1920s. This was with spark, arc and alternator technologies. These technologies were capable of generating up to 5kW at frequencies from LF to MF. With the advent of vacuum tube technology in 1907, a means of electronically generating and controlling RF signals was available. This technology became dominant in the late 1920s and lasted until the mid 1970s. They remain in use even today in some applications as they provide an inexpensive and rugged means of generating over 10kW of power at RF frequencies. Discrete solid state RF power devices began to appear in the 1960's with the introduction of Silicon bipolar transistors (BJT). Following this, in the 1970's, was the introduction of Gallium Arsenide Metal Semiconductor Field Effect Transistors (GaAs MESFET). These allowed solid state to be used in power applications at lower microwave frequencies.

The introduction of solid-state-RF-Power devices facilitated the use of lower voltages, higher currents, and relatively low load resistances. From the late 1980's and 1990's this technology has led to the proliferation of a large variety of new solid state devices such as high electron mobility transistors (HEMT's), pseudomorphic HEMT's, hetero-junction FET's and hetero-junction bipolar transistors (HBT's) from a variety of new materials including Silicon Carbide (SiC), Gallium Nitride (GaN) and others such as InP (Indium Phosphide). With these it was possible to offer amplification at frequencies up to 100GHz or more. [1] [2] [3] [4] [5] [6] [7].

Amplifiers are made up of five basic sections. These are the input and output matching networks, the input and output biasing networks and the transistor itself. In an amplifier design, the actual amplification is performed within the device. But it is the design of the matching and biasing networks that pose the greatest challenge for the designer. The biasing networks, both input and output, ensure that the transistor device has the correct DC bias point. They also supply the device with the energy required to provide the necessary amplification. The input matching network ensures that the power supplied to the amplifier is actually transferred to the device and not reflected back to the source. The output matching network ensures that the device "sees" the correct load at its terminals as well as ensuring that the power delivered by the amplifier is absorbed by the load [8].

1.2 Background to Power Amplifier Design

In general power amplifier design theory, the method of using a conjugate match of the external networks connected to the input and output of the transistor devices, would seem to suffice. In practical situations this does not take into account the limitations of the devices. To utilize the maximum current and voltage swing of

the transistors, a lower value of load resistance is required. This is commonly known as the "load-line match". It is commonly stated that using a load-line match instead of a conjugate match will result in large reflection (VSWR) issues. Practical experience has shown that this is not as large a problem as is sometimes perceived. In a simple load-line matched PA connected to an antenna matched to 50 Ω, VSWR measurements have shown that reflected power is entirely a function of the degree of match between the antenna and the 50 Ω system. The PA, although, does present a reverse mismatch, which could cause a problem in some situations. This can however be solved using an isolator, circulator or balanced configurations of the system. [8]

In order to optimally place a load line, measurements of the current-voltage (I-V) curves are required. These I-V curves provide information on the maximum drain-source voltage (V_{ds}) and current (I_{ds}). Using Cripps's method of load-line matching, along with the measurements of V_{ds} and I_{ds}, an optimal load resistance R_{opt} can be calculated [8].

This method poses a few problems. The main problem it the measurement of I-V curves. Traditional I-V curve measurements make use of DC stimulation of the device under test (DUT) in order to generate the curves. In PA design this poses a serious problem as at higher power the DUT heats up beyond its thermal safe operating area (SOA), and thus attempting to place a load line using this data relies greatly on estimation. A secondary problem is that DC measurements do not show the performance of the DUT under practical RF situations. Using a pulsed RF I-V measurement overcomes this problem by using high frequency DUT stimulation to generate the I-V curves, thus a more accurate optimal load-line placement is possible.

A further issue that requires attention is that of the effect that the DUT package has on the final product's performance. In order to correctly take into account this effect, an accurate package characterization in required. This allows for the incorporation of firstly, the effect of the gate and drain leads, secondly, the effect the bond wires that connect the leads to the transistor die, and finally, the extraction of the intrinsic FET model [9].

A further general PA issue is that of thermal effects. In PA systems where the efficiency is relatively low, the ability of a system to remain thermally stable becomes important. Fluctuations in the temperature of the transistor and surrounding elements can cause large unwanted, unpredictable effects and can even lead to system failure.

Further problems arise when designing a power amplifier (PA). The largest of these is the question of how to accurately characterise a device, such as power transistors, in order to predict behaviour. This would allow for the optimal design of the amplifier. Since measuring total current and total voltage at higher frequencies is difficult, S-parameters are generally used. These allow the behaviour of the power transistor to be characterised in familiar terms such as gain, loss and reflection coefficient. Another advantage of using S-parameters as a design tool is that they can be cascaded in order to get a prediction of the overall performance of a system. They can also be de-embedded from a system measurement in order to gain an understanding of the behaviour of separate sections of the system that are otherwise not available for measurement. With respect to power

amplifier measurement, this allows for the de-embedding of the behaviour of the transistor package, which results in the understanding of the characteristic of the device itself [10].

The S-parameter measurements are not entirely straightforward. These measurements require a test fixture to connect the device to the coaxial-based test equipment. This fixture must facilitate the smooth transition from coaxial to microstrip transmission lines. It must also convert the 50 Ω based impedances of the network analysers and other measurement systems, to the much lower impedances associated with high power transistors. These two features of the test fixture, along with ensuring that the track widths of the test fixture transmission lines do not differ from the widths of the transistor package tabs, greatly help in reducing the large unwanted discontinuities that may occur during the high frequency S-parameter measurements.

1.3 Power Amplifier Design in RADAR Applications

This thesis has, so far in this section, explained some of the general problems that a designer encounters when designing a PA. These problems apply for PA's in the kHz range to PA's that operate in the high GHz range. When designing a PA specifically for the radar bands, further issues become evident.

The first of these issues is cost. Manufacture's of transistors charge very high prices for radar specific transistors. A second issue is the availability of radar transistors. Due to the fact that radar band transistors have obvious military applications, manufacturers might not sell radar band transistors to smaller companies and to companies outside the country of origin. This is both due to loyalty to bigger local companies and to the desire to maintain a military technological advantage.

1.4 Problem Statement

One possible solution, to the issue of cost and availability of devices for RADAR applications, is to use transistors that are designed for other frequencies. These transistors are easily available and in most cases much cheaper. This idea comes with its own problems, mainly that these transistors are pre-matched to other frequency bands. This increases the complexity of the input and output matching circuits that are required for optimal performance.

Designing a PA for a radar band, places greater constraints on the specifications of the system. Firstly, consecutive pulses must be highly repeatable. This allows the system to remove stationary clutter from a radar image. This is especially important when viewing slow moving targets. Secondly, the pulse shape must be stable over a wide variety of pulse lengths, without 'drooping' or fading. The final main constraint is that the PA must be able to operate at wide enough frequencies. This would allow a radar system to be adaptable to different situations, such as different types of scans, improve resolution, as well as facilitating immunity to 'jamming.'

The focus of this work is to approach the problem of RADAR power amplifier design under these constraints.

1.5 Investigation Aims

This thesis aims to investigate the development of three separate L-Band RADAR amplifiers using commonly available transistor devices as well as pre-matched military devices. These amplifiers would be combined in a cascade design in order to provide a high gain, high output power RADAR amplifier, as shown in Figure 1. In the investigation of these developments, certain aims need to be considered. Firstly, and most importantly for RADAR amplifier design, is the available output power. It was decided that the designs should, at least, meet the specified output power of the device being used. Secondly, the amplifiers should provide this output power over the specified bandwidth. In this case all three amplifiers need to operate in the L-band, which stretches from 1.2 to 1.4 GHz. Thirdly, the input match of the amplifiers should be below -15dB across the specified band. Finally the gain of the amplifiers should be as flat as possible. A gain variation of less than 3dB was deemed to be acceptable.

A further investigation criterion of the amplifiers is the pulse repeatability as well as the pulse droop.

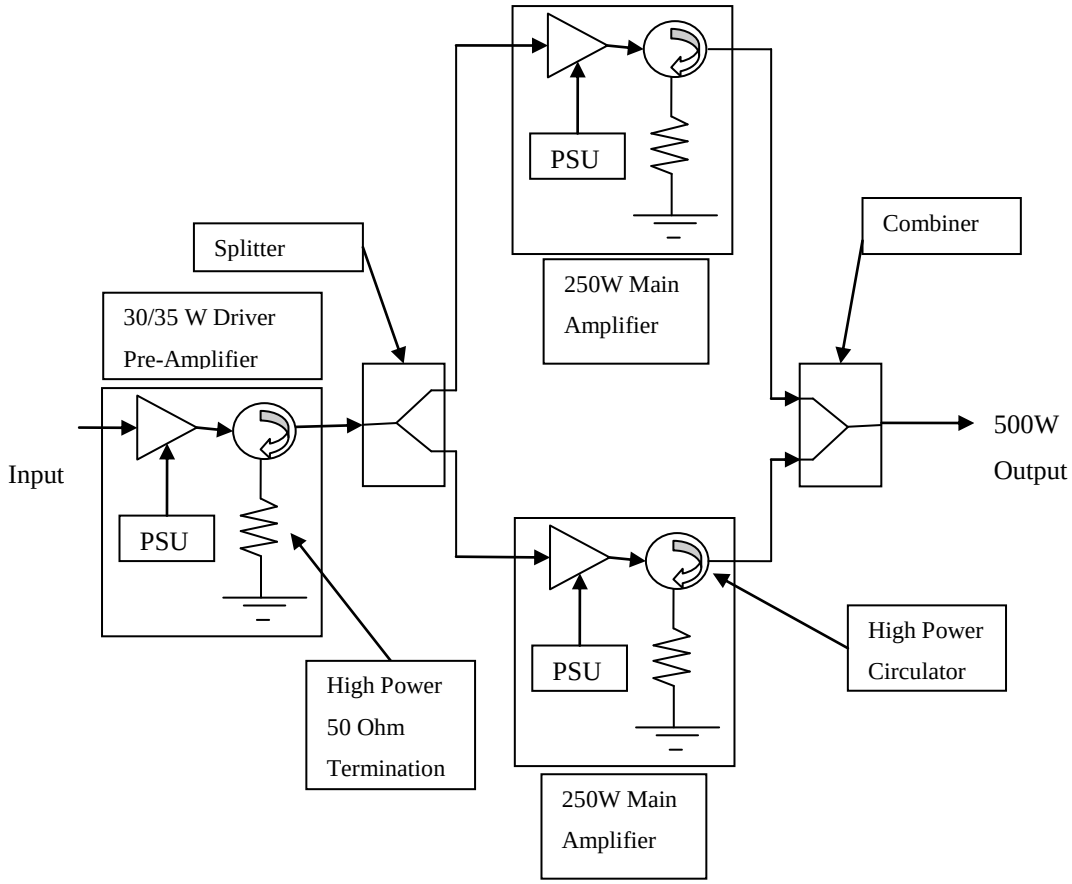

Figure 1 - Layout of a typical cascaded power amplifier system which includes driver amplifiers, main power amplifiers as well as splitters, combiners, circulators and high power 50 Ohm terminations used to dissipate any reflected power.

1.6 Thesis Approach

The problem is divided into three sub-problems. The first is the design of the measurement systems used to characterise devices. The second involves the use of these systems to characterise the three devices used. The pulsed RF measurement system for the generation of the pulsed RF I-V curves of the BLF2045, and the low impedance TRL fixture for the measurement of low impedance S-parameters of all three devices. Finally, the information obtained is used to design the three power amplifiers. A peripheral problem that was also addressed was that of a high speed power supply capable of rapid rise time current pulses to the amplifiers while maintaining a very stable voltage at the drain of the device.

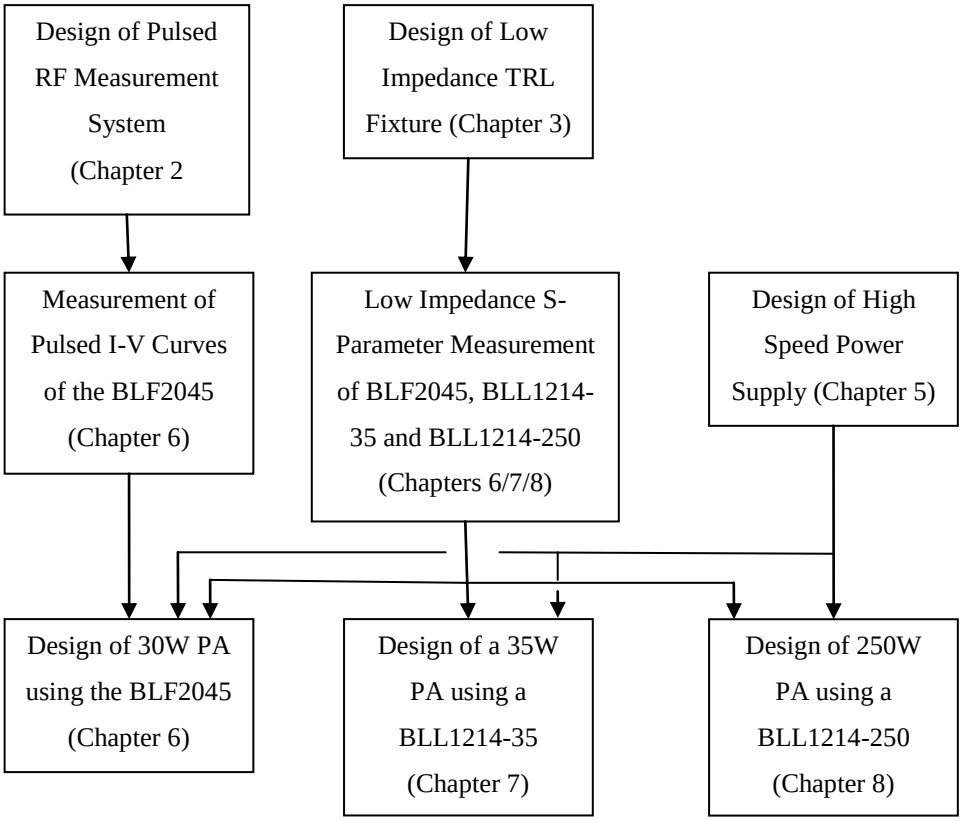

Figure 2 - Diagram showing the approach to the thesis. The diagram shows the steps required to design the three amplifiers as well as the flow of information generated by the stages.

This document is divided into eight chapters.

Chapter 2 describes the design of the pulsed I-V measurement system. It will also describe the control of the system, calibration, and results obtained from the various devices.

Chapter 3 describes the design of a low impedance TRL fixture. This chapter also describes the testing procedures as well as the system validation.

Chapter 4 describes the small-signal parameter extraction procedure performed on the BLF2045 device.

Chapter 5 describes the design of a high speed power supply.

Chapter 6 outlines the design of a 30W PA using an unmatched commercial BLF2045 device using results obtained in chapters 2 and 4.

Chapter 7 outlines the design of a 35W PA using a pre-matched BLL1214-35 device. This is an L-band radar specific device, and the design of the PA is mainly used as a comparative tool in the evaluation of the design procedure of the unmatched BLF2045 device.

Chapter 8 outlines the design of a 250W PA using a pre-matched BLL1214-250 device. The design procedure of this PA follows the same lines as the 35W PA described in the previous chapter.

Chapter 9 provides a conclusion to the work. It brings the various ideas together and critically discusses the successes and shortcomings of the design processes and procedures.

Chapter 2 - Pulsed I-V Measurement System Design

2.1 Introduction

When designing any power amplifier, with the exception of those using pre-matched devices, an intricate knowledge of the functioning of the device is required. The approach here uses a pulsed I-V measurement system in order to generate some of the information that can be used in the load line placement that will be described in Chapter 6. It would be appropriate, at this stage, to discuss why a pulsed I-V measurement system is chosen when DC measurements have been sufficient until now.

In order to answer this question, one must examine the shortcomings of the traditional DC measurement scheme as well as the ways in which a pulsed system overcomes these problems.

The main issue with the traditional DC measurement scheme is that it has a very limited safe area of operation (SOA). This is due to the fact that the high voltages and currents result in large self heating of the device, which, if large enough, can result in permanent damage to the device. The pulsed measurement system overcomes this problem by applying a short pulse with a relatively long time between pulses in order to maintain a constant quiescent condition, effectively showing the RF behaviour of the device at an unchanging bias. This allows the testing of the device well beyond the SOA thus providing much needed information of the device at high power operating points.

The second problem with a DC measurement scheme is that that of dispersion. These dispersion effects contribute to large differences between the measured DC curves and the practical HF operation. Various dispersion mechanisms include thermal, rate-dependant and electron trapping phenomena [2]. These mechanisms are usually slow acting, so that a DC stimulus of the device affects them greatly, whereas an HF stimulus does not. These effects are also dependant on the substrate used in manufacturing the devices. Silicone LDMOS transistors are less prone to dispersion effect where as transistors build on other substrates, such as Gallium Arsenide are more so. A pulsed measurement scheme is thus used to acquire characteristic I-V curves that are free of dispersion. The strategy is to maintain a constant quiescent point while measuring the I-V curves. The period between pulses is normally long enough to allow the quiescent condition to recover from any perturbation that may occur during each pulse. Pulsed measurements yield characteristic curves that show a greater correspondence to the RF behaviour of the device than DC I-V curves.

It bears mentioning at this stage, that the pulsed measurement system was utilized to test two different substrates. Initially the system was tested at IMEC in Belgium. There it was used to test Gallium Arsenide and Silicone Carbide ‘on-wafer’ transistors. This was used as both an initial system verification test as well as an opportunity to obtain data on pulsed RF measurements of non-Silicone transistors. The main test was performed in Stellenbosch, on the Si LDMOS FET mentioned in Chapter 1.

2.2 System Overview

Before going into the specific details of the pulsed measurement system, it would be advisable for one to view the operating principals of the system as a whole, as well as an example of the signals that the system will generate in order to measure the pulsed I-V curves. In the simplest form of the system, a sinusoidal pulse, with a DC offset of 0V, would be applied to the gate of the device under test (DUT). The pulse width as well as the delay between pulses can be arbitrarily chosen. In most cases the pulse width would be in the order of a 10% duty cycle to ensure that self heating does not occur. This gate voltage would cause a current to flow from the drain to the source, with a magnitude dependant on the instantaneous gate voltage. Thus by applying varying gate voltage amplitudes, I-V curves can be established. A further form of the system allows the system to apply a sinusoidal pulse which can be provided with a DC offset within the pulse. Thus the offset can sweep from 0V at the minimum to some arbitrary voltage at the maximum.

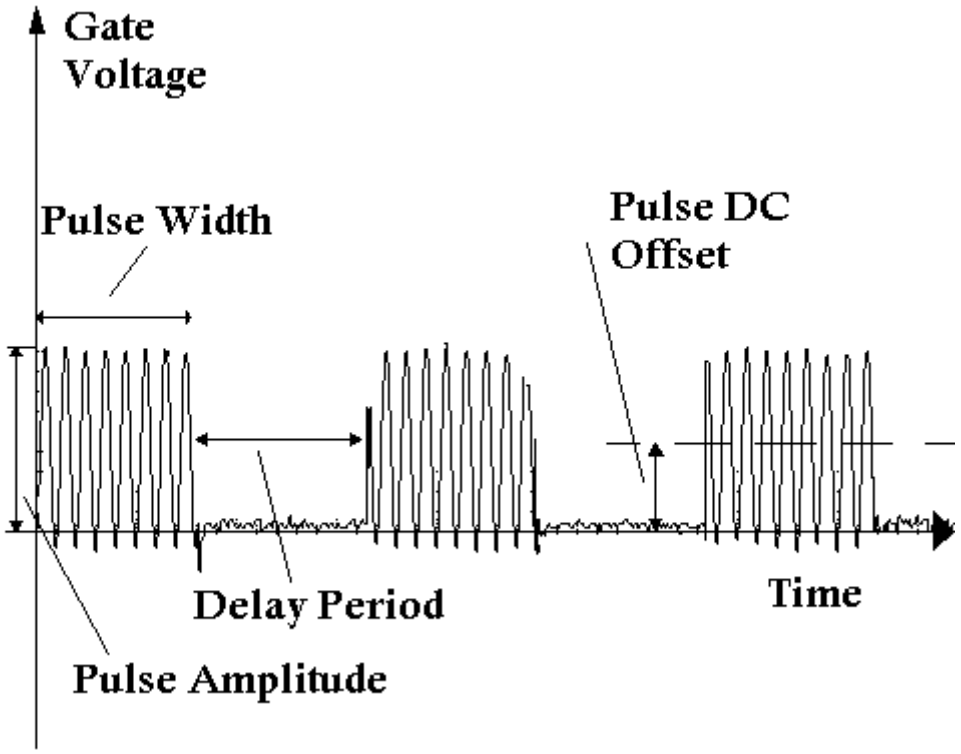

Figure 3 - A figure showing an example of a pulsed sinusoidal signal applied to the gate of the DUT in order to generate the required I-V curves. The signal shows gate voltage against time.

The system is comprised of 4 main sections, namely:

1. Gate Pulser hardware.
2. Custom Test Fixture for Packaged Devices.
3. A Programmable DC power supply at the drain.
4. Control System.

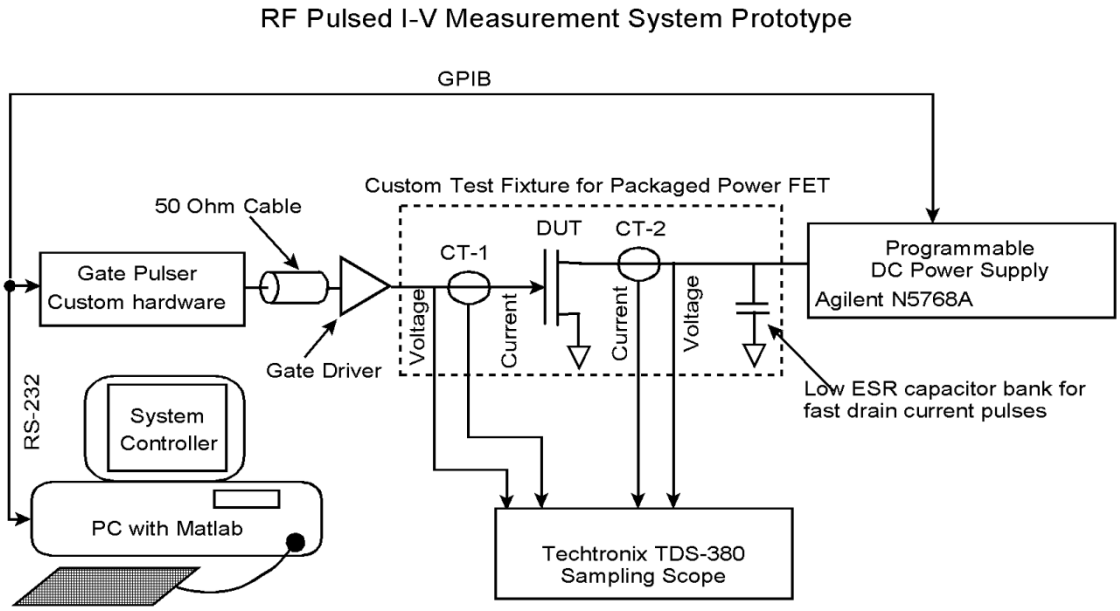

Figure 4 - A figure showing pulsed measurement system overview including the control equipment needed to automate the measurement.

The first section is the gate pulser hardware. This hardware generates the sinusoidal signal, applies the amplitude variation as well as the required DC offset, and modulates the signal.

The second section is the custom test fixture. This allows for the mounting of the specific DUT package, as well as mounting for current and voltage sensors at both the gate and the drain of the DUT. These sensors are measured using a Tektronix TDS-380 oscilloscope. This fixture also allows the DUT to be driven directly at the gate by having a built-in driver in the fixture.

The next section is the programmable drain DC power supply. This section is implemented with an industry standard Agilent N5768A programmable power supply which can be controlled via MATLAB. The final section is the control system. This section involves the use of Microchip demo board which controls various Digital-to-Analogue Converters (DACs) and digital control signals which in turn control the gate pulser hardware. This section also uses MATLAB to control the Microchip demo board as well as the power supplies directly.

2.3 Gate Pulser

The gate pulser is the main hardware section of the entire measurement system. In the design of this section the following specifications were kept in mind:

The frequency within the pulse needs to be controllable. Ideally the frequency range must be between 1MHz and 20MHz

There needs to be 40dB range of variable gain in the voltage amplitude of the applied signal. This gain must be from -10dB to +30dB.

The voltage amplitude must have up to 10V of swing. This is required in order to fully test the range of the DUTs.

The pulse width as well as the delay period needs to be variable, as can be seen in Figure 3.

The pulse DC offset must be selectable between three positions:

1. Zero Offset – The signal swings around 0V without any DC offset
2. Positive Offset – The signal must swing from a minimum of 0V to the maximum voltage.
3. Negative Offset – The signal must swing from a maximum of 0V to the minimum voltage.

Provision is made for an external signal for signal generation if necessary.

Keeping these specifications in mind, the pulsar hardware was split into the following sections:

1. Sinusoidal Signal Generation
2. External Signal Relay
3. Amplitude Variation
4. Level Detection
5. DC and Level Addition
6. Signal Modulation

The full system schematic can be seen in Figure 5

2.3.1 Sinusoidal Signal Generation

In order to generate the sinusoidal signal, a Maxim MAX038 high-frequency waveform generator was used. This chip was chosen due to its following properties:

1. 0.1Hz – 20MHz operating frequency range
2. Various waveform types can be created including: triangle, sawtooth, sine, square and pulse. Only the sinusoidal was implemented in this design
3. Independent frequency and duty cycle adjustments.

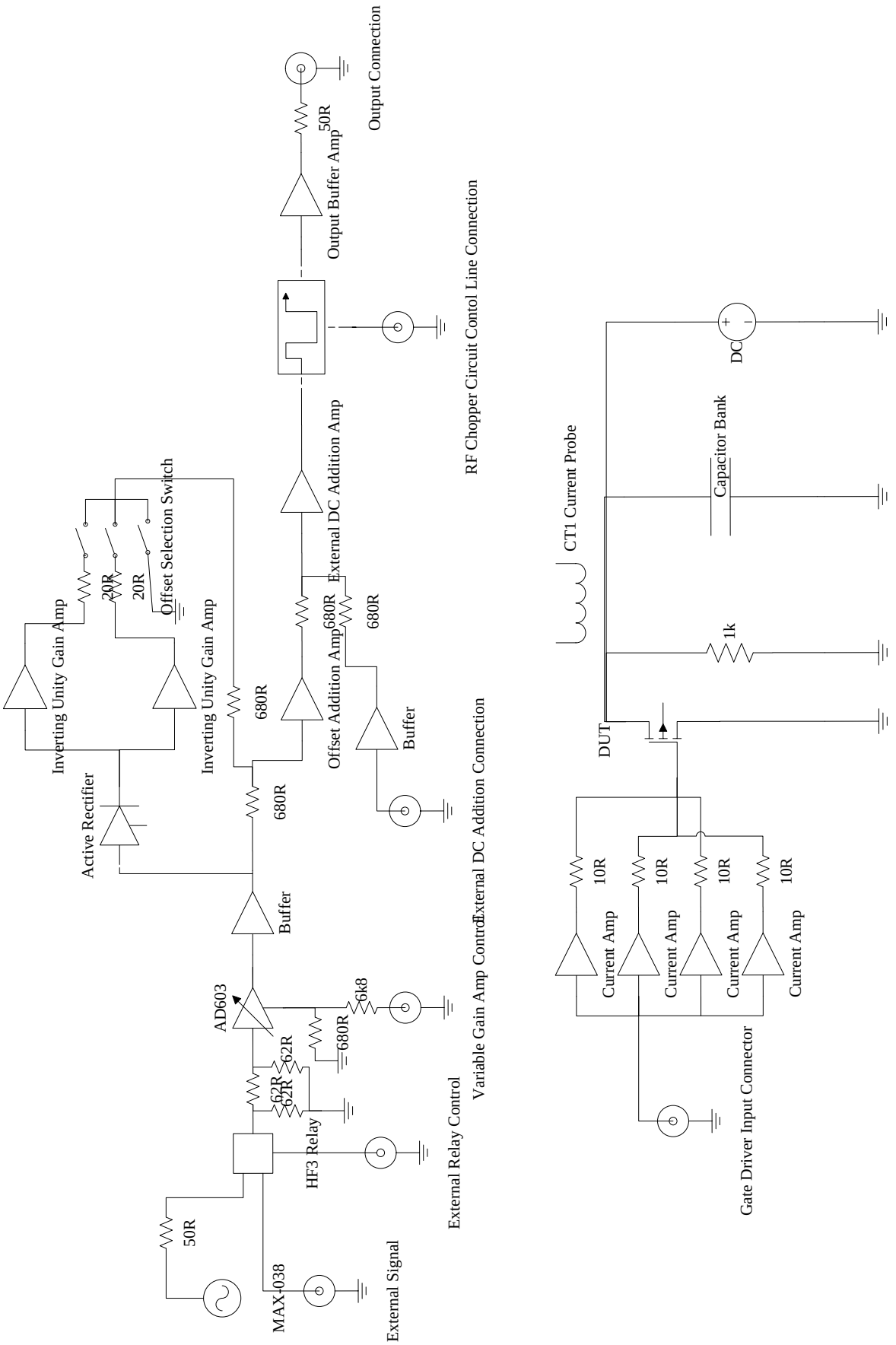

Figure 5 – Figure full schematic of gate pulser system

The first task with the MAX038 is to select the type of wave form. This is done by setting the TTL/CMOS-logic address pins (A0 and A1). Since this hardware will not be switching between different waveforms, it was decided to connect A1 directly to the 5V, and although A0 can be view as 'Don't care' it was decided to connect it to ground for the sake of thoroughness.

The second task is to select the operating frequency of the MAX038. This frequency is determined by the current into I_{in}, the capacitance C_{osc} and the voltage on the F_{adj} pin. Although the original specification of the hardware was to have a variable frequency, it was found that the maximum frequency possible was 6MHz. This was not due to the limitations of the MAX038 but rather due to limitations in the rise times of other components. This issue will be discussed in later in the chapter.

In order to set the centre frequency the following equation is used [11]:

$$Fo(MHz) = Iin(\mu A) \div Cf \quad (1)$$

Where:
F_o = Centre Frequency
I_{in} = Current into the I_{in} pin
C_f = Capacitance between the C_{osc} pin and ground

By examining the data page it was decided that the value of C_f = 33 pF should be used. This would allow the current into the I_{in} pin when operating at F_o = 6MHz to be approximately 200uA. The reason for this is that, for optimal performance, I_{in} should be kept between 10uA and 400uA.
Thus for a centre frequency, $F_{o,}$ of 6MHz

$$Iin = Fo \times Cf = 198\mu A \quad (2)$$

The value of R3 was chosen to be 6.8KΩ. This allowed the value of V_{in} to be in the region between 1 and 2V depending on the frequency required.

It can also be seen, from the data page, that the I_{in} pin is internally forced to a virtual ground, and thus:

$$V_{in} = I_{in} \times R_3 = 1.334V \quad (3)$$

The final task in setting the operating frequency F_o is to set the voltage on the F_{ADJ} pin. This pin has a constant 250µA constant current sink that must be furnished by the voltage source. The MAX038 also provides a reference pin (REF) that has a constant, internally supplied voltage of 2.5V.
Thus:

$$R_f = \frac{(V_{ref} - V_{fadj})}{250\mu A} \quad 4$$

This resistance R_f was implemented using a surface-mount multi-turn variable 20KΩ resistor. Thus the centre frequency F_o can be fine tuned by tuning the resistor R3.
The duty cycle adjustment pin, D_{ADJ}, was connected to ground. This is the suggested connection, shown in the data page, when using the MAX038 as a sinusoidal waveform generator. All other pins are connected as suggested in the data page [11]. This includes various DC de-coupling capacitors.
The output impedance is low, thus in order to ensure a 50 Ω output impedance from the MAX038, two 100 Ω resistors were placed in parallel at the OUT pin.

2.3.2 External Signal Relay

In order to implement signal selection between the MAX038 and an external signal, an AXICOM HF3 surface-mount relay was used [12].
A voltage control voltage applied across pins 1 and 11 selects the external input. The default state connects the internal input from the MAX38, at pin 20, to output pin 6.

This relay was chosen for two reasons. Firstly the fact that it is surface-mount, and secondly because it has an internal impedance of 50 Ω.

In order to select the external signal, a TTL/CMOS 5V voltage is applied to pin 1, and to switch back to the MAX038 signal a 0V voltage is applied to the same pin. This signal is supplied by the Microchip control board, and will be discussed later in the chapter.

2.3.3 Amplitude Variation

In order to implement the variable gain amplification, an Analogue Devices AD603 [13] variable gain amplifier was chosen. The reasons for this were firstly that it provides a wide (40dB) gain range, and secondly because of its simplicity. It is controlled with a simple voltage difference between two pins.

In order to control the variable gain, a voltage range of -0.5V and +0.5V varies the gain between the minimum and maximum respectively. In order to achieve this, a voltage divider network, from a 5V supply to the GNEG control pin, was implemented. The ratio of R1:R2 was chosen to be 10:1. Thus ensuring that the voltage at the GNEG control pin is a constant 0.5V.

A voltage applied to the GPOS pin that varied between 0V and 1 V would therefore result in the voltage Vg to swing between the desired -0.5V and +0.5V.

It was also found that output from the MAX038 causes the AD603 to saturate too quickly. Thus a 50 Ω 18 dB resistive attenuation Pi-network was placed at the VIN pin to ensure the maximum voltage gain control.
The final stage of the amplitude variation is to amplify the output voltage of the AD603, which is ±3V, to the required ±10V.
In order to implement this gain, a National Semiconductor LM6181 current feedback op amp [14] was chosen. This operational amplifier can provide a high output drive of up to ±10V, and has a high slew rate of 2000V/µs.

The LM6181 is a current feed-back op-amp used in a non-inverting set-up. The value of the feedback resistor was chosen to be 820 Ω. This was at the suggestion of the data page in order to ensure the best performance over all possible applications [14].

Since, the output of the AD603 is ±3V and the required voltage is ±10V, a gain 3.33 is required.

2.3.4 Level Detection

In order to measure the amplitude of the signal, an active full-wave rectification circuit, Figure 6, is used [15]. This circuit is implemented using a Texas Instruments THS4031 voltage feed-back op-amp [16]. This operational amplifier has an output voltage swing of up to ±13V and can drive up to 90mA. Secondly, it has a high slew rate of 100V/µs. The principle of this circuit is that the operational amplifier maintains the bias on the diodes so that they remain on the verge of being on. This increases the accuracy of the circuit over traditional rectification circuits, which do not take the voltage required to switch the diodes ‘on’ into account.

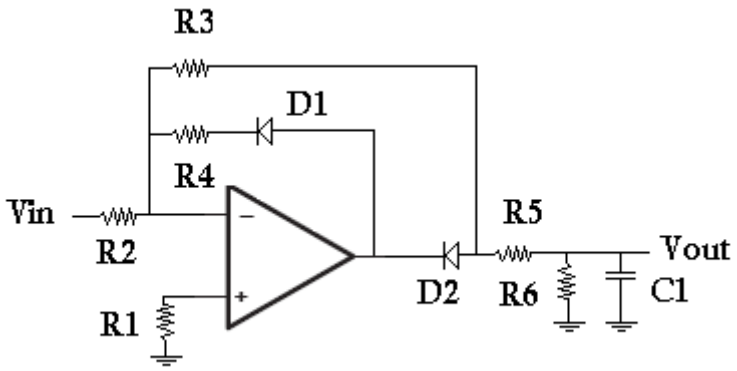

Figure 6 - Figure showing the schematic of active diode full-wave rectifier

The gain of the active rectifier is set at unity by selecting R3 equal to R2. These two resistors were set at 820 Ω. R1 is set at R2//R3 thus R1 equals 410 Ω. R5 is placed in series with the operational amplifier as the output drives a capacitor directly. It is set as 20 Ω as per suggestion in the data page. The R6 and C1 combination is chosen to set the time constant τ.

$$\tau = RC \quad (5)$$

With R6 equal to 2KΩ, and C1 equal to 100nF, τ has a value of 0.2ms
This ensures that the ripple voltage on the level detector is small enough to not affect the DC offset of the pulse.

2.3.5 DC and Level Addition

This section involves four parts. Firstly, the output of the level detector is buffered with both an inverting and a non-inverting unity amplifier. This provides a both a positive and negative DC voltage that is proportional to the amplitude of the pulse. Next the voltage to be added to the signal in order to provide the desired offset is selected. It can be a positive, negative or zero offset. The next step is to use an addition circuit to add the DC offset. The final stage is to add a precision external DC voltage to the signal in order to compensate for the amplitude and frequency dependant errors in the level detection and amplitude control.

A 20 Ω resistor is placed at the output of both unity amplifiers. This is in order to ensure that in the possible event that the outputs of the amplifiers are shorted, the circuits are protected.

A LM6181 [14] is selected as the operational amplifiers for the addition amplifiers due to their high speed capabilities.
The feedback resistor in both the additions circuits is again chosen to be 820 Ω. Gain is provided by both amplifiers to compensate for the voltage division that occurs as a result of the addition circuit.

2.3.6 Pulse Modulation

The modulation circuit was implemented using a Maxim DG413F fault protected, analogue switch. When first implemented, it was found that a single switch did not provide enough isolation between the input and output. Thus it was decided to use a cascade design in order to increase the isolation.
A single control line is used to operate all the switches simultaneously. A problem could occur if the series switches switch on before the parallel switches switch off, thus effectively shorting the circuit down to ground. This is prevented by the break before make feature of the DG413F. The output of the switch circuit is then buffered using a LM6181 operational amplifier.

The 50 Ω series resistor is used to ensure a match to the 50 Ω cable used to connect the pulse generation hardware to the test fixture.

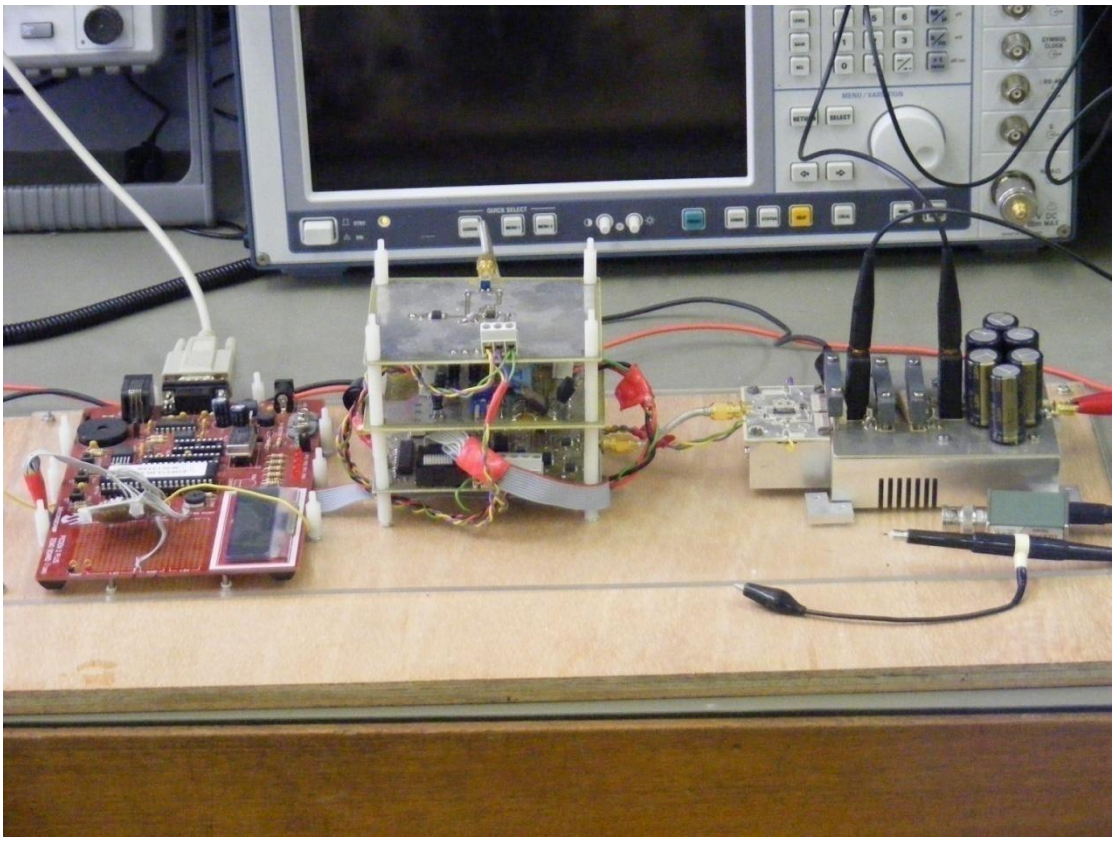

Figure 7 - Figure showing final Pulsed I-V measurement setup

2.4 Test Fixture for Power FETS

When designing the test fixture, various ideas had to be kept in mind. Firstly the gate driver must provide a gate stimulus voltage, irrespective of the required gate current, directly to the gate of the DUT. Secondly the fixture must provide for a voltage and current probe at both the gate and drain of the DUT. Finally the fixture must provide a large, low effective series resistance (ESR) capacitor bank at the drain. This is to ensure that the measurements are not influenced by a voltage drop at the drain.

The gate driver was implemented using an Analog Devices AD8392 quad pack current feed-back op-amp [17]. The AD8392 has a high current output (400mA), large output voltage swing (±12V) and high slew rate (900V/µs). The quad pack allows for a compact design. The design put the four op-amps in parallel with each other and places a series resistor at the output of each op-amp in order to isolate them from each other.

The choice of feedback and gain resistors was according to the suggestions in the data page [17].
The gate driver circuit board is mounted on an aluminium block. This block is then attached to the main DUT fixture block. This allows for a strong mechanical attachment, as well as allowing a modular implementation of the gate driver which would allow for future improvements. This would be useful if there is a need to change the driver amplifier.
The voltage sensing is implemented by mounting high impedance probe attachments directly on to the PCB. A thin high impedance transmission line connects the mounting point to the gate and drain.
Current sensing is achieved by the use of two Tektronix current probes, a CT-1 and CT-2 probe. These probes are mounted directly to the fixture block.

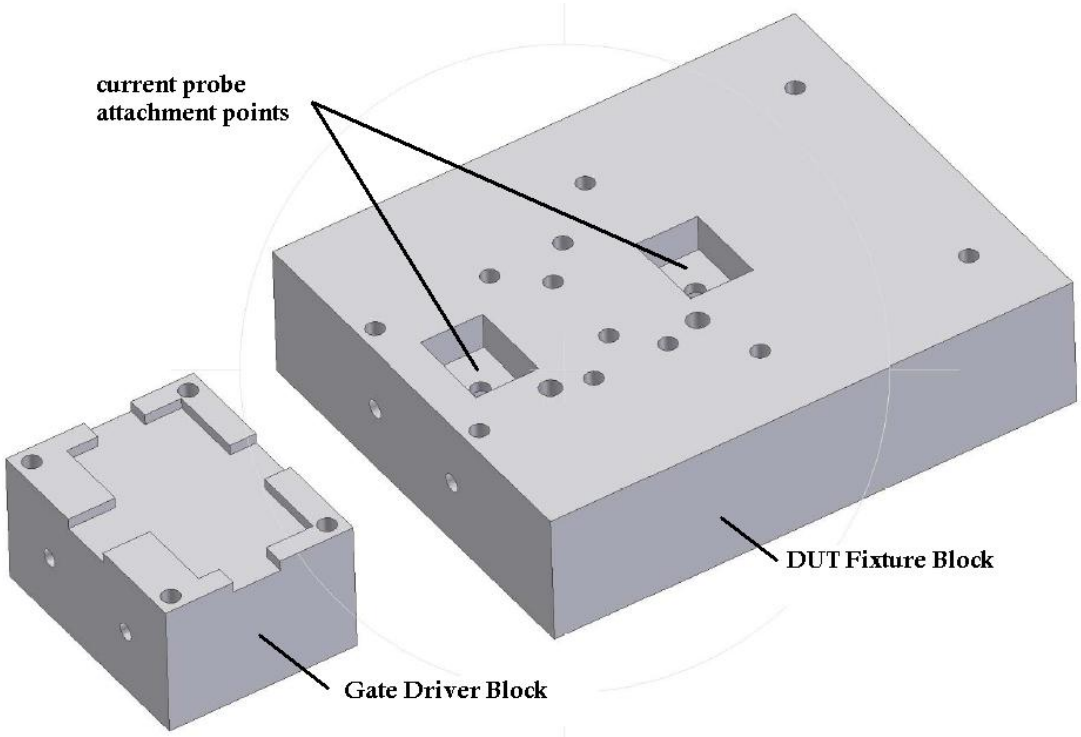

Figure 8 - Figure of gate driver block and DUT fixture block

When performing initial tests on various devices, an unwanted resonance was observed in the measurements. This was found to be due to the series inductance of the current probe. In the practical implementation, shown in Figure 7, Figure 8 and Figure 9, the current probe requires a short length of copper wire to pass through the probe, which has an inductance. A common estimate for the inductance of a thin wire is 1nH per millimetre. The length of wire used is roughly 10mm, thus a series inductance of 10nH is added. This inductance, along with the

small capacitance formed at the drain caused a resonant effect. In order to solve the problem, a shunt resistor was placed directly at the drain. The value of this resistor was chosen to be 1kΩ. This allowed for the stabilization of the drain while not drawing more than 26mA of DC current from the power supply.

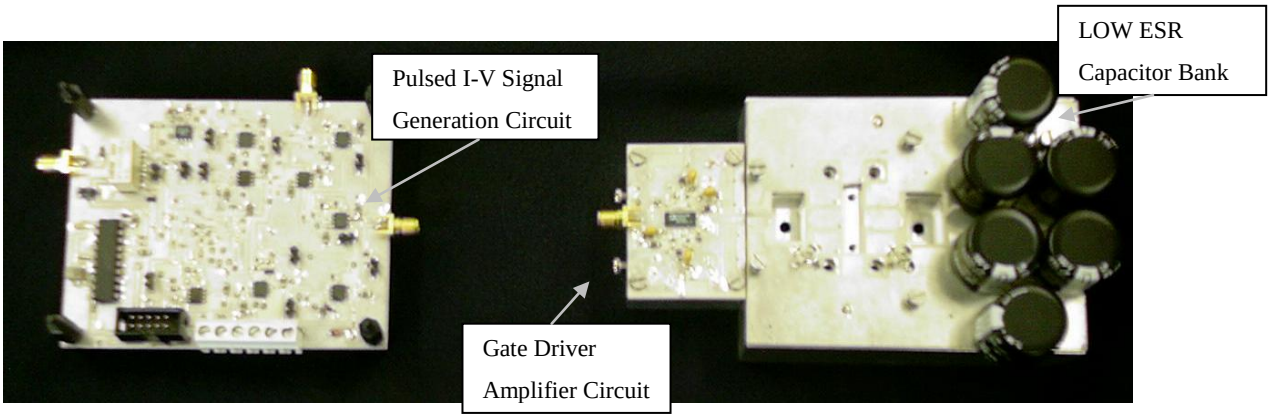

Figure 9 - Photo of fixture assembly shown in two separate sections. The section on the left shows the pulsed I-V signal generation circuit. The section on the right shows the gate driver amplifiers attached to the power FET test fixture

2.5 Control System

The control of the entire system, as shown in Figure 10, is done by means of MATLAB executable code. This code allows the user to send instructions via a serial cable to the Microchip demonstration board. The demonstration board controls an 8-bit Maxim MAX5102 dual digital to analogue converter (DAC) [18], as well as seven TTL/CMOS logic control lines. The DACs are used to control the amplitude variation and the frequency variation as described earlier in the chapter. The logic control lines are used to control the relay position, the various offset and addition switches and the modulation cascade switch.

The DC voltage output of each of the DACs is controlled by the following:

$$Vout = (Nb \times Vref) \div 256 \quad (6)$$

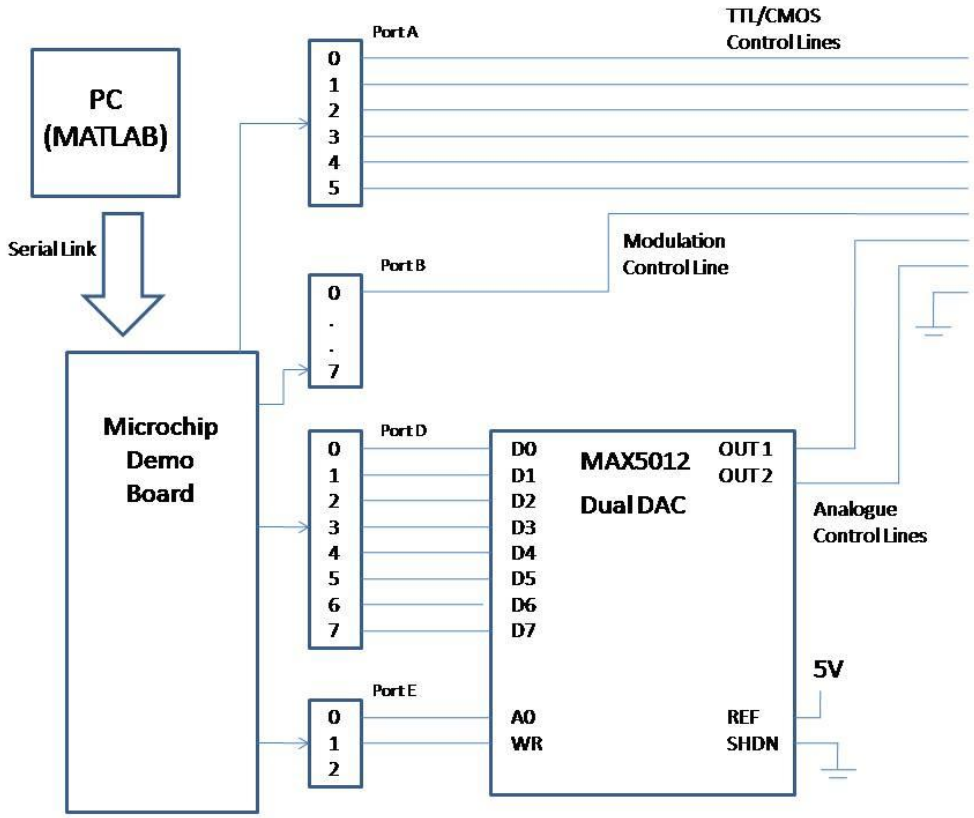

Figure 10 - Figure showing schematic of the control system.

The MAX5102 DAC is controlled by firstly setting the 8-bit parallel control line (D0...D7). The PIC then selects the DAC to be set by setting the address line (A0) on the MAX5102 to either high (sets DAC 1) or low (sets DAC 2). The write line is then toggled on and off to latch the 8-bit level of the selected DAC.

2.6 Measurement System

Data retrieval was performed by firstly setting the gate voltage and then sweeping the drain voltage. The resulting currents were measured on a Tectonics TDS-380 oscilloscope. These measurements were performed by hand as the computer interface of the oscilloscope was not implemented at the time. This allowed for possibility of inaccuracies, although this was minimised by measuring each point several times and averaging the results.

2.7 Calibration

In order to ensure that the measurements taken were accurate enough to correctly characterize the device, two calibration techniques were used. Firstly, a known power was applied to a known 50 Ω load. This was implemented using a Rohde & Schwartz SMIQ signal generator. The frequency was set at 6MHz to ensure that

there could be no distortion of the results due to a frequency dependent response. By measuring the resulting currents flowing through the 50 Ω load and the voltage over the load, an exact calibration of the voltage and current sensors could be made. Through this technique, it was found that both resulted in negligible measurement errors.

2.8 Results

As discussed previously, a pulsed RF test of transistors allows for various advantages over traditional DC measurements. The main advantage is that in RF testing, the SOA (safe operating area) is much greater. This allows for a better understanding of the devices high power response. A second advantage is that it allows the effect of dispersion and temperature to be taken into account. This would allow for better design parameters, such as load-line placement, and would thus lead to a more efficient and effective design.

Testing of the system was performed in two ways. Firstly the system was transported to IMEC in Belgium. These tests involved DC as well as RF pulse testing. Slight modifications were made to allow for on-wafer testing but functionally the system remained identical.

The second set of tests was perfumed at the University of Stellenbosch on LDMOS devices. This involved only pulsed RF testing.

The first set of results shown are those from the tests performed on on-wafer silicon carbide transistors at IMEC in Belgium. These test highlighted the first main difference between DC and RF pulse testing.

IMEC uses a hybrid between DC testing and RF pulse testing whereby the gate of the transistor is stimulated with a DC (square wave) pulse. By comparing the results of these tests to those of a similar RF pulse test, the direct effect of RF pulse testing can be seen.

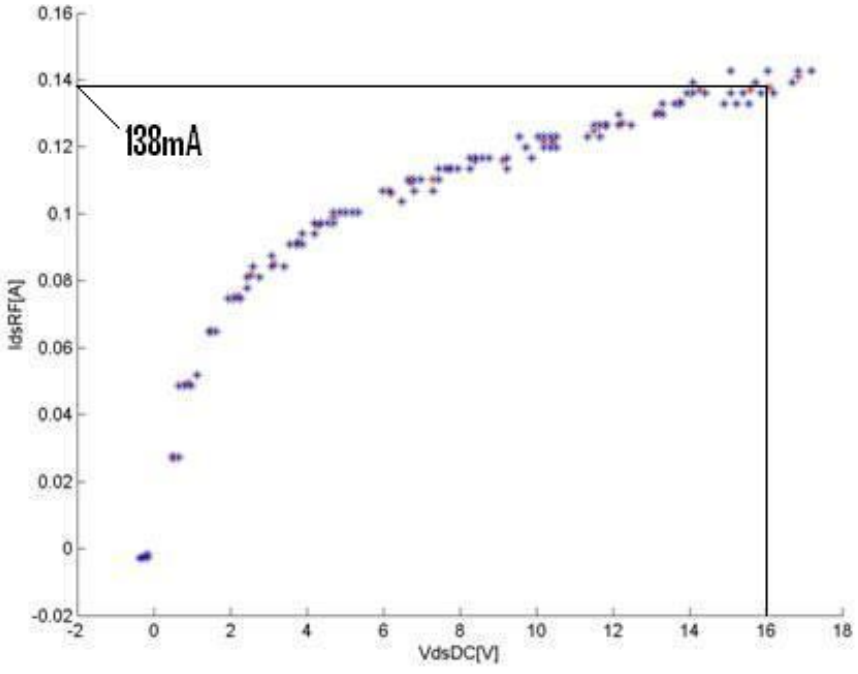

Figure 11 - Figure showing pulsed RF I-V curve of Silicon Carbide transistor P259_4_T03F3

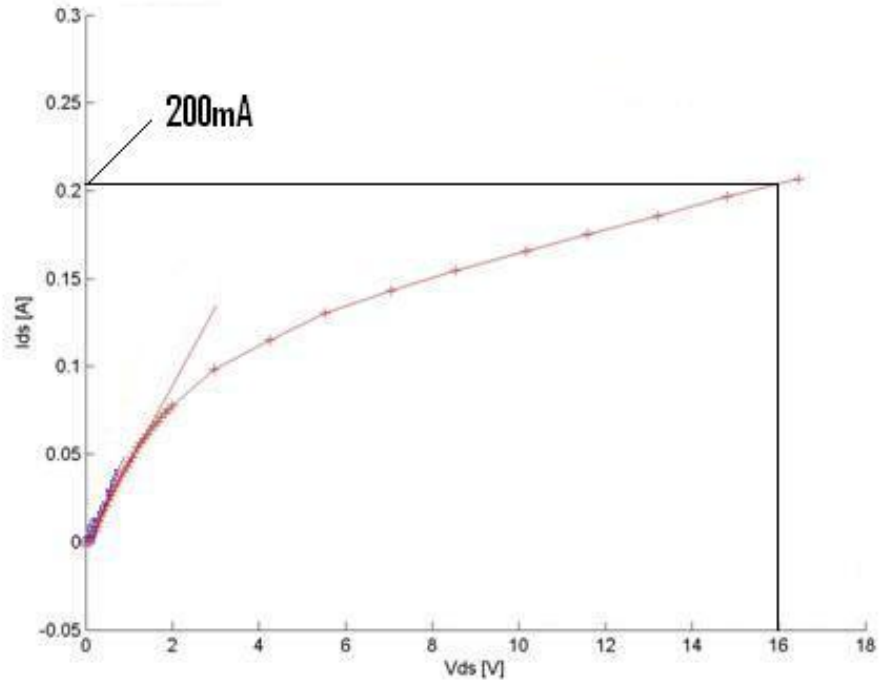

Figure 12 - Figure showing pulsed DC I-V curve of Silicon Carbide transistor P259_4_T03F3

The graph showing the pulsed RF I-V curve, Figure 11, when compared to the pulsed DC I-V curve, Figure 12, shows a ± 30% drop in drain current Ids. This can be directly correlated to the fact that the gate is receiving a RF pulse instead of a DC pulse. Thus the effect of dispersion can be observed. In order to show a repeatable result and thus rule out the possibility of single transistor malfunctioning, the test was repeated on several transistors. The results shown in Figure 13 indicate a constant drop in drain current of approximately 20 – 30 %.

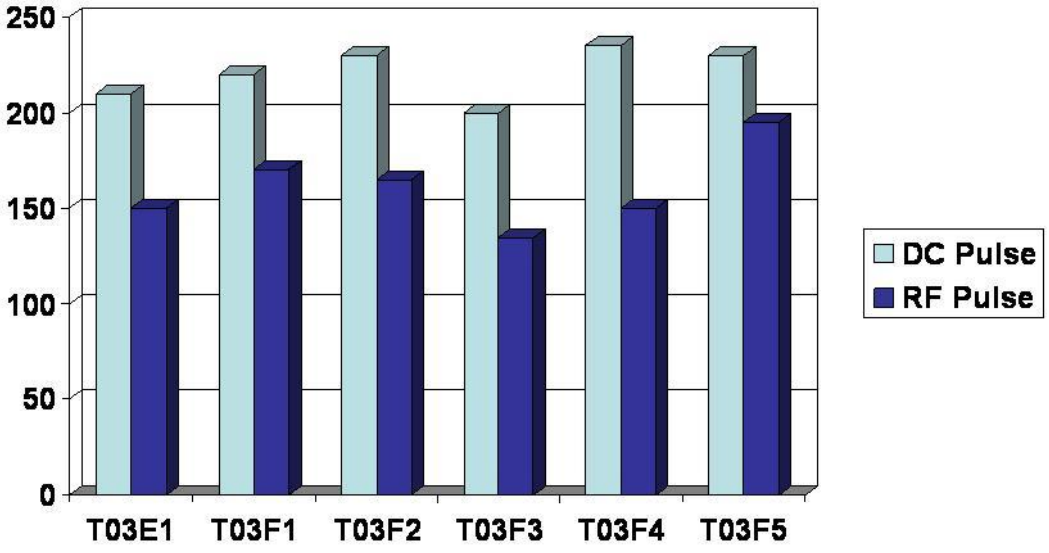

Figure 13 - Diagram comparing the measured Ids of RF vs. DC pulsed measurements

The second set of results are those of the RF pulse tests that were performed on the silicon based BLF2045 LDMOS transistor. The following graphs show the trend of the I-V curves to varying gate and drain voltages. This allows a direct comparison between pulsed RF measurements, shown in Figure 14, to a pure DC measurement, shown in Figure 15. The measurement was limited to operation within the safe operating area.

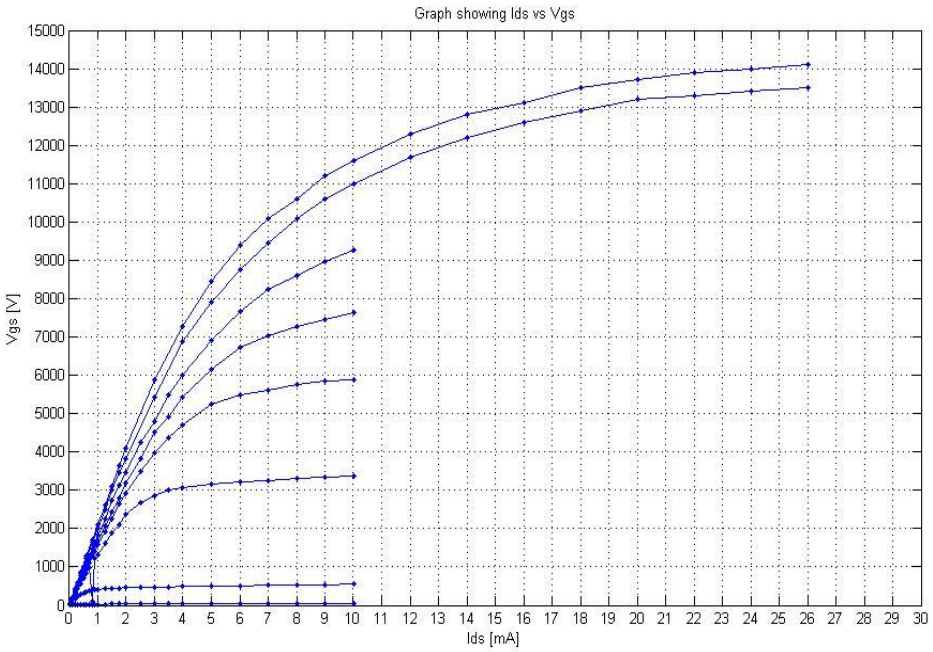

Figure 14 - Graph showing pulsed RF I-V curves for BLF2045 LDMOS device

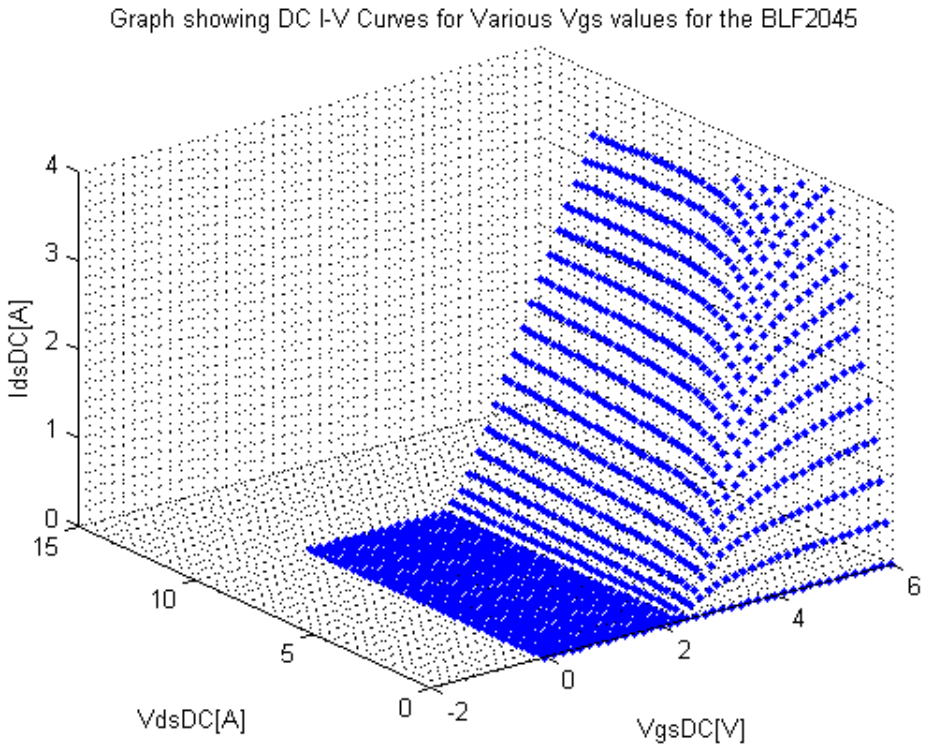

Figure 15 - Graph showing DC I-V curves for various V_{GS} of the BLF2045 LDMOS device.

This test highlighted a much greater range of Ids swing in the pulsed RF I-V curves of Figure 14, and secondly, a more subtle difference in the shape of the pulsed RF and DC I-V curves. In the testing of the DC I-V curve, the knee area, which is the area in which the device begins to saturate, is distinct. This is very different when performing the pulsed RF testing which shows a more gradual transition into saturation. The significance of this fact is that load-line placement, for which I-V curves are the most important measurement, becomes a more difficult task. This will be discussed more detail in chapter 6.
A final result observed is that the device was not full driven into saturation. This would be due to a lack of voltage range of the gate driver.

2.9 Recommended System Improvements

Although the system showed very promising results, various flaws are apparent in the design. These hamper the effectiveness of the system. In order to improve the design, the following issues should be addressed:
The signal generator should be replaced with a high speed (>100MHz) digitally controlled IC.
The amplitude control should be replaced with a set pre-amplifier which amplifies the signal to a set maximum level and this should then be followed by a variable attenuator. This is suggested because of the fact that a major limiting factor in the design was that of the limited slew rate of the AD603 variable gain op-amp. The faster LM6181 op-amps compensated for this to some degree but do not counteract the limitations completely.
The level detection should be replaced with a digitally controlled power meter. This would allow a much greater accuracy as it would not be frequency or amplitude dependant as is the case with the active peak detector.
The DC level addition should be replaced with a DAC which would be set depending on the feedback from the power meter. This would also then facilitate a calibration procedure.
Finally, the gate driver amplifier should be replaced with a high speed, high voltage transistor amplifier. This would allow for a much greater range of gate voltages, thus enabling a view of the entire range of the devices operation.

2.10 Conclusions

By using a pulsed RF measurement system instead of a DC measurement system it was found that new modes of system operation can be observed, although the accuracy and usefulness of this is still unproven. It showed that a device can be tested well beyond the DC SOA without fear of damage, which facilitates the creation of more accurate designs and estimations. It showed differences between the nature of DC and RF responses, as well as variations in the curve shapes.
It should be mentioned, though, that this system is not without its shortcomings. These faults are mainly due to the fact that the system is in a prototype stage of development.
These changes aside, the design of the pulsed RF measurement system was a success and proved the concept. This system can only lead to a greater understanding, and improved design of power amplifiers. The results obtained in this section will form the basis of design process of the 30W BLF2045 amplifier in chapter 6.

Chapter 3 - Advanced Low Impedance TRL Fixture

3.1 Introduction

The goal of this chapter is to document the design and implementation of a high-accuracy RF test fixture that allows for very accurate low impedance measurements of high power devices [19] [20]. This test fixture is implemented using a THRU-REFLECT-LINE (TRL) calibration method and pre-matching networks in order to create a smooth, frequency independent, and low reflection transition from a 50 Ohm coaxial environment to a low impedance microstrip measurement environment [21] [22].
The first section of this chapter will discuss the design and implementation of the Klopfenstein pre-matching networks [23]. The second section of the chapter will discuss the design of the mechanical fixture, and the third section will discuss the testing and validation procedure.

3.2 Low Impedance TRL design

3.2.1 Klopfenstein Taper Design

As mentioned before, one of the challenges of a low impedance measurement test fixture is to create a smooth transition between the 50 Ohm coaxial environment and the low impedance device environment. This was implemented by using a Klopfenstein taper [23]. The reason for this choice is twofold. Firstly, a Klopfenstein taper allows for a very low reflection transition, and secondly, the taper provides a frequency independent response over a very wide band [24]. A further advantage of the Klopfenstein taper over other taper designs (such as triangular and exponential tapers) is that, for a given reflection coefficient within the pass band, the Klopfenstein taper gives the shortest taper length [24].

In all the taper designs, MATLAB code written by Pieter Jacob De Villiers Malan was used to generate the actual taper models. This code was written as part of his MSc.Eng thesis [24].

In order to design the tapers the following information was necessary: the input impedance, the output impedance, the maximum ripple within the pass band as well as the minimum operating frequency. The substrate dielectric constant must also be known. This is a value that is dependent on the substrate chosen. In this project Rodgers 6010 was used. This substrate has a typical ε_r of 10.2 ± 0.25. This allows low impedances to be realised with moderate track widths. Specifically it allows the design of the 50 Ω input track width to be 0.58mm which is roughly the same width as the inner pin of the SMA connectors used in the fixture design.

The input impedance is naturally 50 Ω as this is the impedance of the coaxial measurement environment of the network analyser. The output tab widths were chosen to be the same as the transistor tab widths. The tab widths were between 5mm and 13mm. These widths along with the chosen substrates high ε_r results in a low characteristic impedance which is closer to the transistor port impedance, thus resulting in less of a mismatch between the DUT and the measurement system.

In terms of this project, two different tapers were required. The first taper, shown in Figure 16, was used to measure the low power BLF2045 and BLL1214-35 transistors. The second taper was used to measure the high power BLL1214-20 transistor, this taper has the same profile as the taper shown in Figure 16 but has a wider tab width.

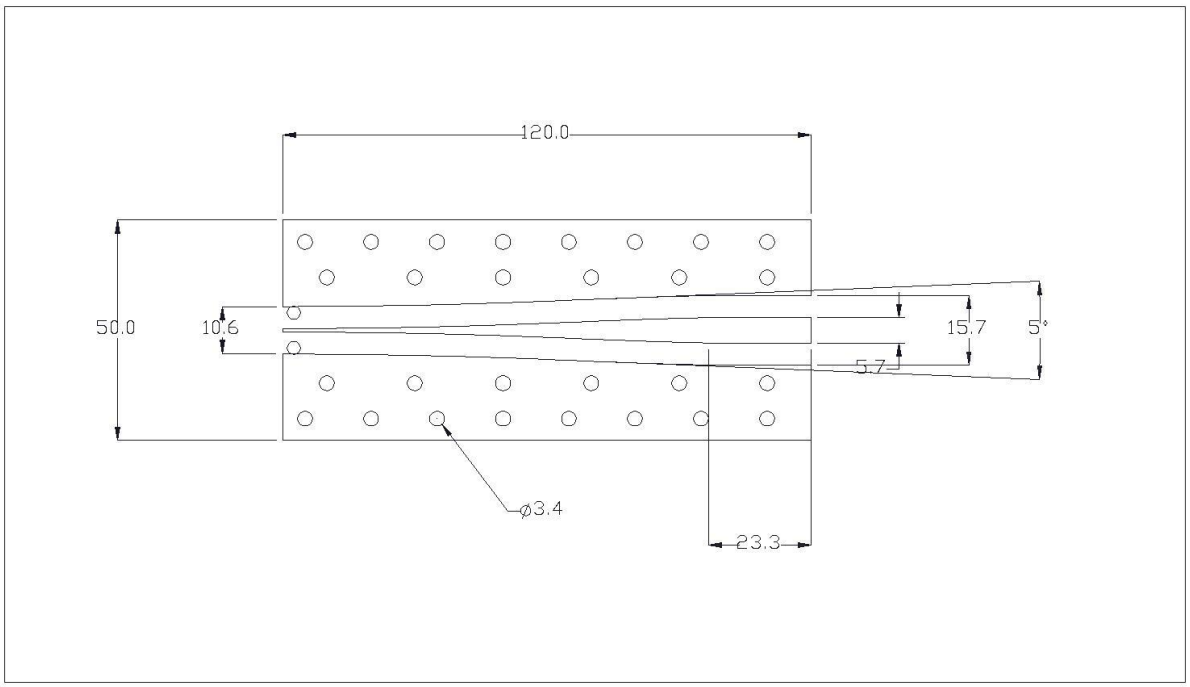

Figure 16 - Figure Showing Klopfenstein Taper Profile of BLF2045 and BLL1214-35 measurement fixtures including mounting holes for screws.

As both the BLF2045 and BLL1214-35 transistors use the same package, the same taper design could be used. The port tab widths on the two transistors are between 5.53mm and 5.7 mm.Thus, the final output impedance of the low power taper is 10.7551Ω

The BLL1214-250 is packaged in a larger die. This accommodates a higher power capability. The tab widths on this package are between 12.57mm and 12.83mm. Thus, the final output impedance for the high power taper is 5.33811Ω

The MATAB Klopfenstein design program [24] calculated the tapers to be 96.7283mm long. As this is an awkward number, a short transmission line was added to the output port in order to lengthen the taper to a more

useable length of 110mm. This line had the same width as the low impedance output (DUT) port, as to not affect the output impedance.

3.2.2 Mechanical Fixture Design

There are two considerations when designing a mechanically sound test fixture. The first and most important is to ensure that the in-fixture measurements are accurate. The second is to maintain an easily repeatable measurement. One should keep in mind that although measurement and fixture errors can be compensated for in the calibration process, this proves to be detrimental to the overall measurement accuracy of the system. It should also be noted that as the measurement fixture requires manufacturing, the design must be of reasonably low complexity so that designs can be created without the large cost of outsourced machining.

As mentioned previously in the chapter, two fixtures were designed. A complete fixture for the low power devices and a second fixture for the high power device. Fortunately the size of each fixture allowed for the reuse of the design, with only the actual DUT (Device Under Test) fixture block being different.

Each fixture set comprised of six sections: the tapered launch sections with their coaxial to microstrip conversions, the DUT fixture blocks and the three TRL (Through-Line-Reflect) calibration standards, these being a zero length through standard, two non-zero line standards, and a short standard [24] [22] [25] [26] [27]. The DUT fixture block could also double as an open standard.

The first step in the mechanical design is the coaxial to microstrip conversion. A flange mount female SMA connector was used to provide the coaxial launch due to their relatively low cost and availability. The SMA connector chosen provided an inner pin diameter that was near to the 0.58mm of the 50 Ω initial taper width.

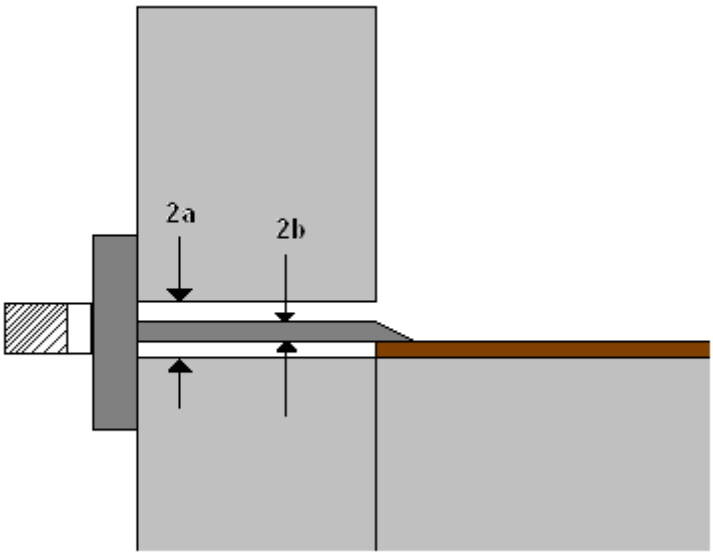

Figure 17 - Figure showing the coaxial to microstrip conversion including the dimensioning of the coaxial to microstrip transition implemented in order to maintain a 50 Ω impedance.

The dimensions of the inner pin and the hole diameter were designed firstly so that the 50 Ω impedance was maintained but also to ensure that the ground discontinuity at the transition is minimised by placing the edge of the hole at the same point as the underside of the 0.635mm substrate.
Next, the inner pin diameter and hole diameter, as shown in Figure 17, needed to be chosen. Two equations dictate these values. Firstly, the equation for the characteristic impedance of a coaxial line (Z_0) [28] [29].

$$Z_0 = \sqrt{\frac{\mu}{\epsilon}} \times \frac{\ln\left(\frac{a}{b}\right)}{2\pi} \quad (7)$$

where
$\mu = 4 \times \Pi \times 10^{-7}$
$\varepsilon = 8.854 \times 10^{-12}$

Secondly the physical restrictions of the fixture result in the equation

$$2a = 2 \times 0.635 + 2b \quad (8)$$

Solving these equations for a Z_0 of 50Ω results unusable values as the accuracies required would not be possible with available machining techniques. Thus an approximation was made:

$$Inner\ Pin\ \emptyset = 0.6mm$$
$$Outer\ Hole\ \emptyset = 1.4mm$$

This resulted in characteristic impedance Z_0 of 50.799Ω.

The next step was a precautionary step. It was decided that, as a coaxial-microstrip transition can cause higher-order modes to propagate, a short channel would be placed at the transition. This would help to suppress any possible higher-order modes.

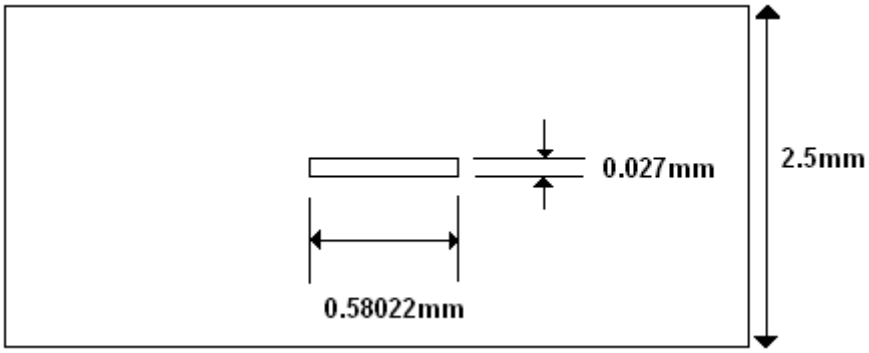

Figure 18 - Figure showing approximation of the cross section of a waveguide channel at coaxial-microstrip transition

Several approximations were made when choosing the dimensions of the channel shown in cross section in Figure 18. Firstly, the effect of the substrate was ignored, and secondly the width was chosen wide enough to not effect design significantly.

The width of the track as well as the thickness of the track was also fixed at 0.58022mm and 0.027mm respectively. The centre frequency (f_c) was chosen to be 1.3GHz.

The next step was to design the calibration standards.

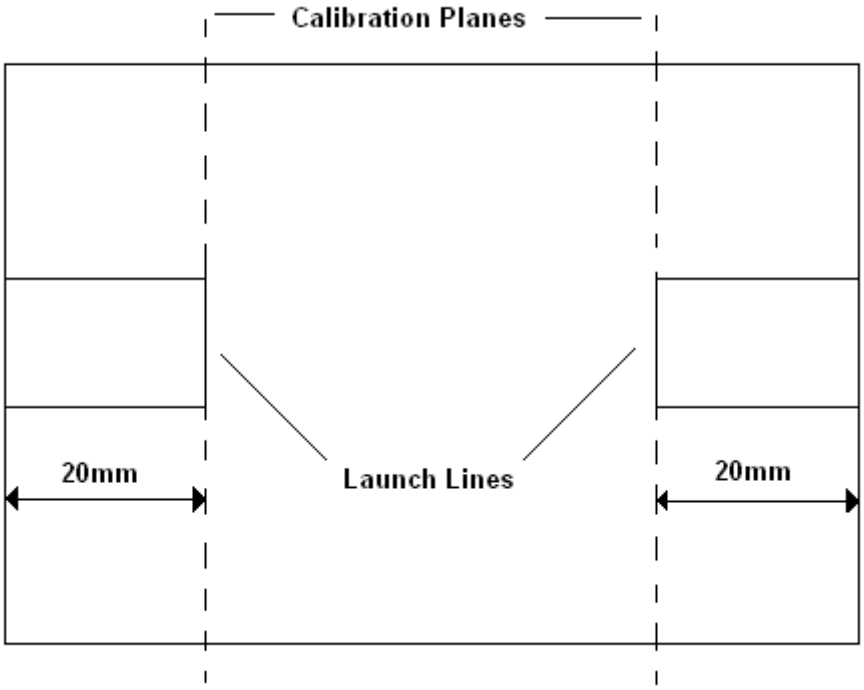

Figure 19 - Figure showing the design plan of the calibration standards as well as their launch lines and calibration planes.

The use of launching lines, shown in Figure 19, allowed a repeatable transition between the taper blocks and each of the calibration and DUT blocks. In a TRL standard calibration, a non-zero length line is required. The choice of line length determines the frequency band over which the calibration remains valid.
For any given length, the minimum and maximum operating frequencies are those at which the line is 20^o and 160^o respectively [27] [26].

It was decided that two calibration lines would be used, the first to cover the 500MHz– 4 GHz band, and the second to cover the 1 GHz – 8 GHz band.
The calculations resulted in the two lines being ±12mm and ±6mm for the low and high band respectively.

Table 1 - Table showing the relative electrical lengths of LINE 1 calibration Standard (12mm)

	Frequency	Angle (degrees)
Centre Frequency	2.25 GHz	96.1674
Upper Frequency Limit	4 GHz	172.433
Lower Frequency Limit	0.5 GHz	21.2149

Table 2 - Table showing the relative electrical lengths of LINE 2 calibration standard (6mm)

	Frequency	Angle
Centre Frequency	4.5 GHz	97.2185
Upper Frequency Limit	8 GHz	175.247
Lower Frequency Limit	1 GHz	21.2485

These values show that the calibration would begin to lose validity at the higher frequencies. This is acceptable in the scope of the project as the measurements would be most important below 2 GHz. These values are independent of the different line impedances.

The next stage in the mechanical design is the transistor fixture blocks. These blocks must provide both an electrical and mechanical attachment of the DUT to the block. A recess was milled out of the aluminium block to provide the depth needed to mount the source flange of the DUT. This was screwed down to provide a strong mechanical connection for heat transfer as well as a continuous electrical connection.

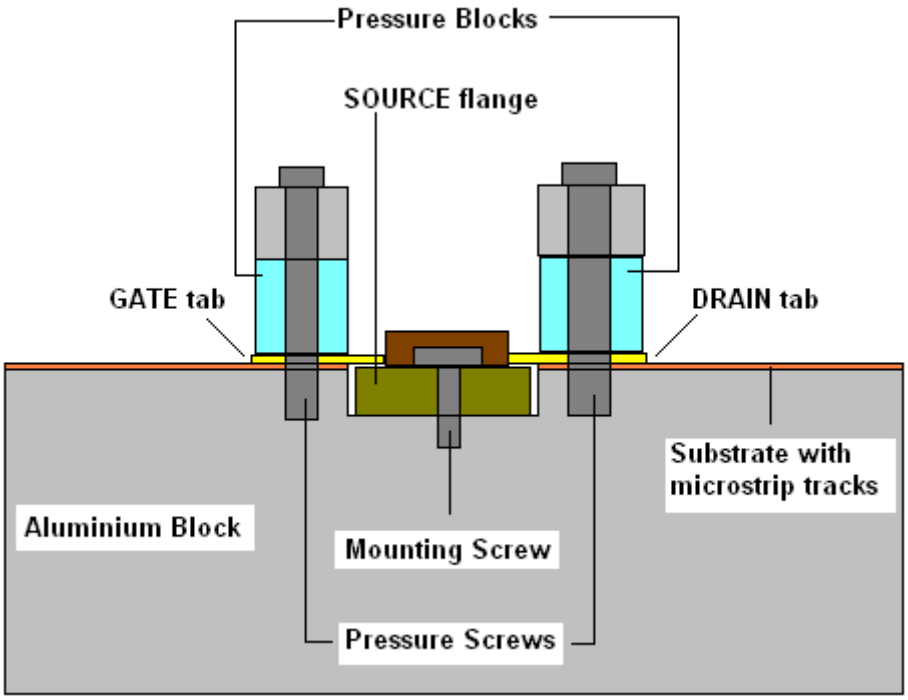

Figure 20 - Figure showing the cross section of the DUT fixture block

In order to provide a good electrical connection between the gate and drain tabs and the microstrip tracks, Teflon pressure pads were placed over the tabs. These were screwed down in order to apply the needed pressure. A specific DUT fixture block was designed for each specific transistor to be tested.

The final stage in design was to provide a method of providing an electrical connection between the two tapers and whichever bock was placed in the fixture, be it the calibration standards or the DUT fixture itself. It is very important that the connection is repeatable in every case; otherwise the calibration would not be able to remove the effect of the connection from the results.

It is also important, from an accuracy point of view to ensure that there is no step discontinuity, as seen in Figure 21, between the blocks as this could add unwanted errors.

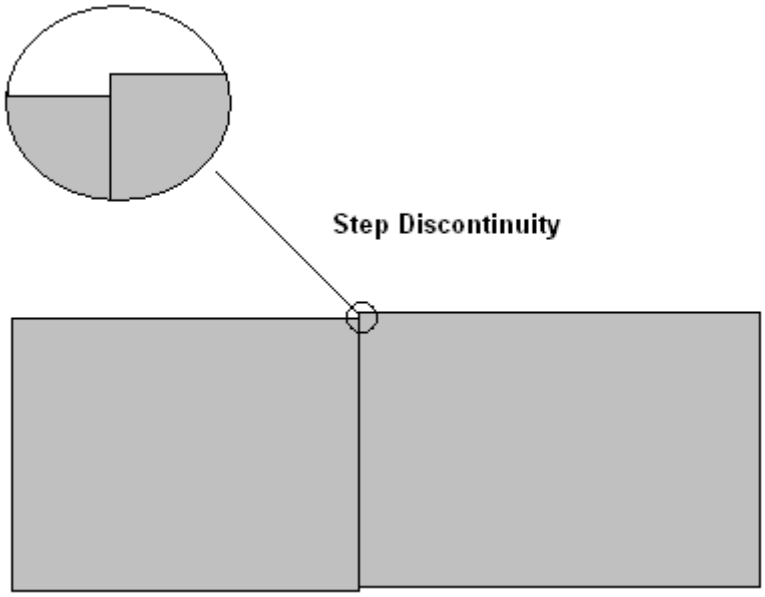

Figure 21 - Figure showing the possible step discontinuity in the ground surface of two fixture blocks

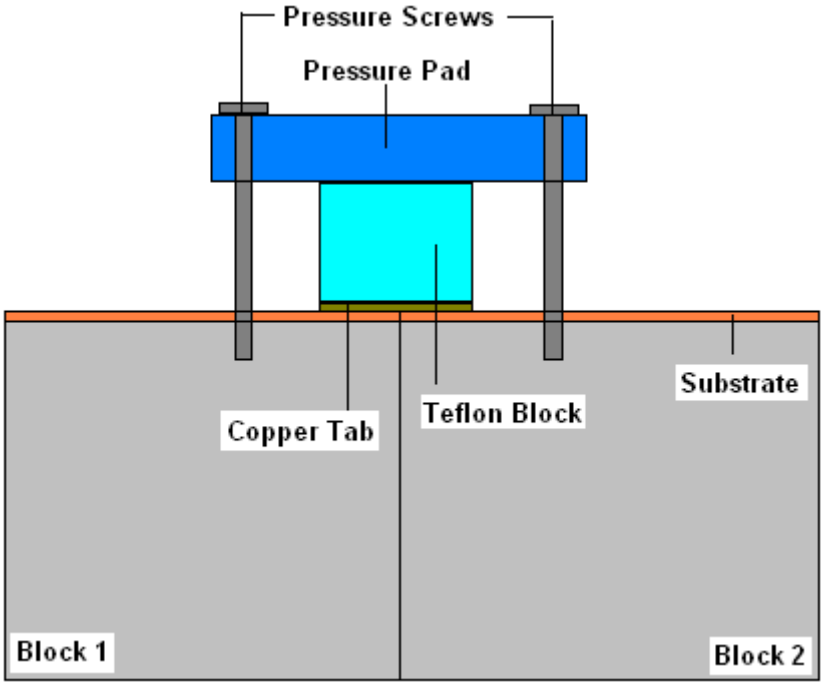

Figure 22 - Figure showing the connection between two blocks

In order to provide this repeatable electrical connection a copper tab was placed so that it overlapped with both sides of the block connection. This copper tab was exactly the same width as the two microstrip transmission lines that it joins. Pressure was applied using a Teflon block, which is pressed down by a pressure block which is screwed in to the aluminium block. This pressure ensures a good electrical connection. A cross sectional view of the transitions can be seen in Figure 22. When forming the connection, the blocks must be lined up by eye to

ensure that there is no discontinuity between the blocks. This has the potential for human error, although careful alignment kept this to a minimum. The test fixture can be seen in Figure 23.

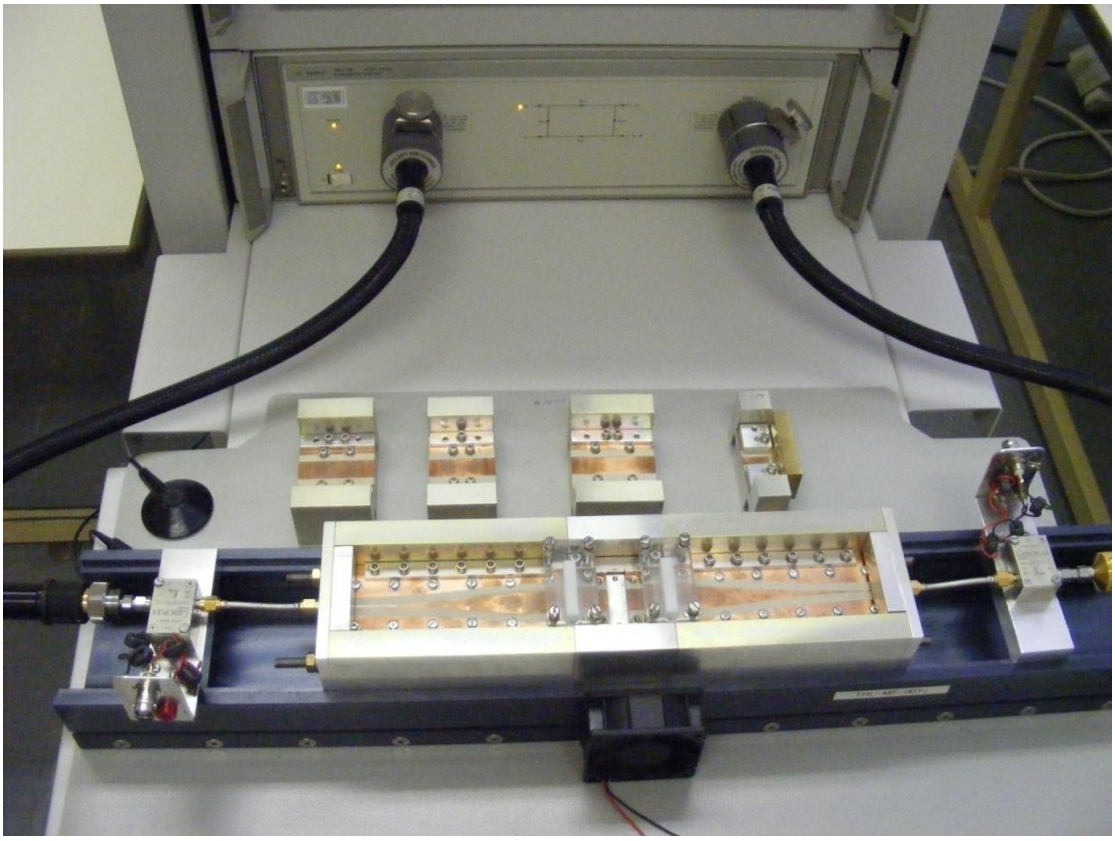

Figure 23 - Figure showing the final Low-Impedance Test Fixture including calibration standards

3.3 Testing and Validation

In order to use the results gathered from the low impedance test fixture, the test fixture needs to be validated. It was decided to use a method of complex permittivity determination [24] [30] [31] [32]. The advantage of this method is that it does not require network calibration. This method [30] calculates the complex permittivity from un-calibrated vector network analyser (VNA) measurements, and as the dielectric constant (and consequently the complex permittivity) of the substrate are known (10.2 ±0.2), the measurement system can be verified. It uses the measurement of the propagation constants of two different length transmission lines i and j. The transmission lines must be identical in every other way.

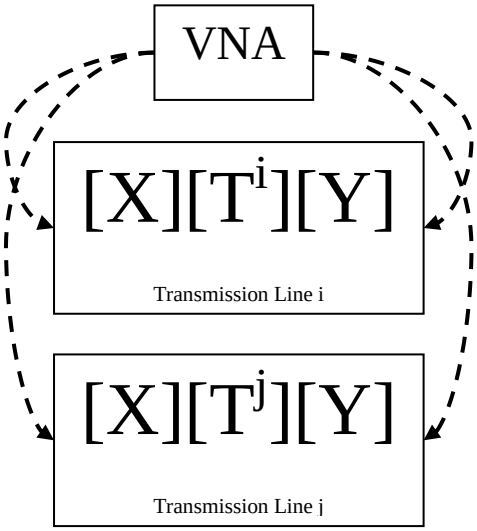

Figure 24 – Figure showing the representation of the low impedance TRL validation system. Two transmission lines are represented. The un-calibrated VNA, cable and fixture errors are represented by the matrixes X and Y. The transmission lines are represented by matrixes T^i and T^j.

Let the measured scattering parameter matrix M^i be,

$$M^i = XT^iY = \frac{1}{S_{21i}}\begin{bmatrix}(S_{12i}S_{21i} - S_{11i}S_{22i}) & S_{11i}\\ -S_{22i} & 1\end{bmatrix} \quad (9)$$

T^i and T^j are the cascade matrixes for the ideal transmission lines *i* and *j*, and the matrices X and Y represent the inherent errors in the VNA and test fixture.

Similarly,

$$M^j = XT^jY = \frac{1}{S_{21j}}\begin{bmatrix}(S_{12j}S_{21j} - S_{11j}S_{22j}) & S_{11j}\\ -S_{22j} & 1\end{bmatrix} \quad (10)$$

where

$$T^i = \begin{bmatrix}e^{-\gamma li} & 0\\ 0 & e^{\gamma li}\end{bmatrix} \quad (11)$$

$$T^j = \begin{bmatrix} e^{-\gamma lj} & 0 \\ 0 & e^{\gamma lj} \end{bmatrix}$$

12

l = length of the transmission line

γ = propagation constant

Transmission lines *i* and *j* must identical in all respects apart from length.

The cascade matrices *i* and *j* can be re-arranged into

$$M^{ij}X = XT^{ij}$$

13

Where

$$M^{ij} = M^j[M^i]^{-1}$$

14

And

$$T = T^j[T^i]^{-1}$$

15

Since T^{ij} is diagonal, its diagonal elements are the eigenvalues of T^{ij} and M^{ij}. These values, $\lambda_{1M}{}^{ij}$ and $\lambda_{2M}{}^{ij}$ of M^{ij} are

$$\lambda_{1M}^{ij}, \lambda_{2M}^{ij} = \frac{\left(M_{11}^{ij} + M_{22}^{ij}\right) \pm \sqrt{\left(M_{11}^{ij} - M_{22}^{ij}\right)^2 + 4M_{12}^{ij}M_{21}^{ij}}}{2}$$

16

And the two eigenvalues $\lambda_{1T}{}^{ij}$ and $\lambda_{2T}{}^{ij}$ of T^{ij} are

$$\lambda_{1M}^{ij}, \lambda_{2M}^{ij} = e^{\pm\gamma(l_j - l_j)}$$

17

Combining these two eigenvalue equations provides the propagation constant γ.

$$\gamma = \frac{\ln(\lambda^{ij})}{l_i - l_j}$$

18

Where the average of the two eigenvalues is,

$$\lambda^{ij} = \frac{1}{2}\left[\lambda_{1M}^{ij} + \frac{1}{\lambda_{2M}^{ij}}\right]$$

19

The complex propagation constant can be divided into its real and imaginary parts

$$\gamma(\omega) = \alpha(\omega) + j\beta(\omega)$$

20

Where α is the attenuation factor and β is the phase factor.

The effective dielectric constant ε_{rEff} for a microstrip transmission line is given by [2]

$$\varepsilon_{rEff} = \left(\frac{c(\beta - \alpha)}{\omega}\right)^2$$

21

One should note that the γ is inversely proportional to the difference between the lengths of the two transmission lines. This is the weakness in this validation method. It relies of the exact physical measurement of the transmission lines which could result in errors.

It was found that when two transmission lines, where the difference between the line lengths was not great enough were used, large variations in the resulting effective ε_r were evident. This was due to the fact that the errors in length measurement would be much greater (percentage wise) than if transmission lines with larger length differences were used.

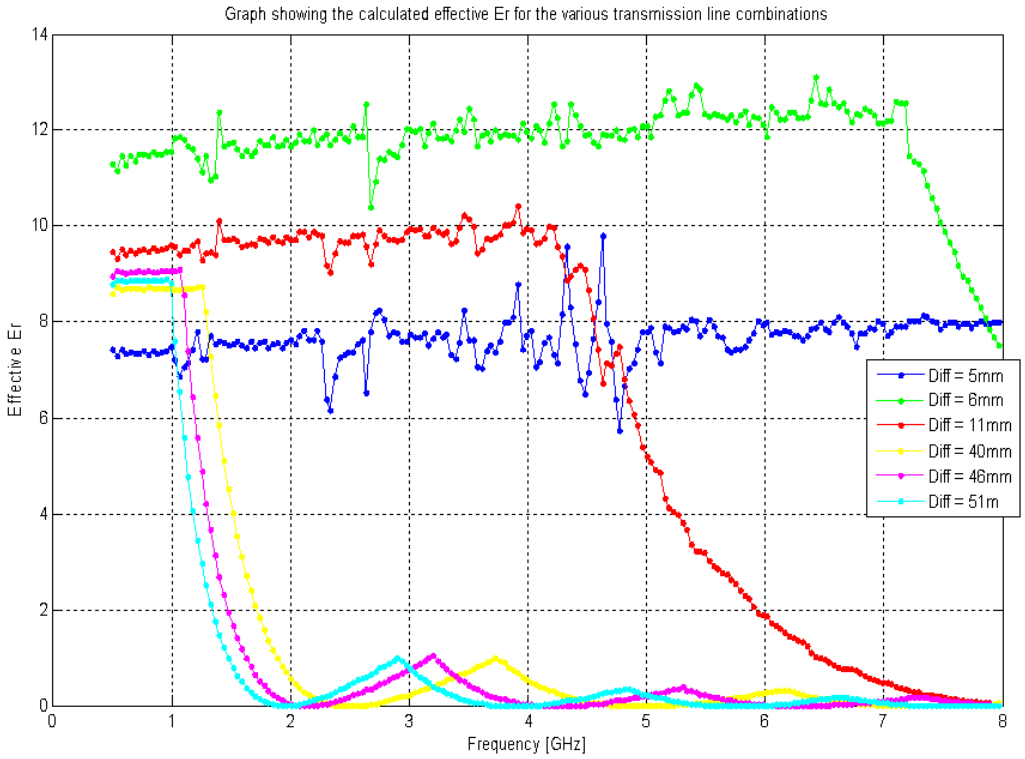

Figure 25 - Graph showing effective ε_r as well as areas of validity and variation due to length differences for the various transmission line combinations

Figure 25 shows the calculated effective dielectric obtained gained from the measurement of the different line lengths. In order to get consistent results the difference between transmission line lengths need to be as large as possible.

One should also note the areas of validity, below the steep drop off, for the various transmission line combinations, as well as the large variation in the results when using transmission lines with smaller differences in lengths.
Using these results it was decided that the data from the three combinations with the largest differences in length (40mm, 46mm, and 51mm) would be used.

A Gauss-Newton optimization routine was used to adjust the dielectric constant to obtain the best fit between the modeled and measured effective dielectric constant across the frequency band of interest.

Table 3 - Table showing Calculated ε_r (real) for the various line length differences

Line Combination Length Difference	ε_r (Real)
40mm	10.2664
46mm	10.6359
51mm	10.4808

An average of these values was taken and used later in the project. This value was

$$\varepsilon_r = 10.4610$$

22

This value is slightly higher than the specification on the Rodgers board of 10.2±0.2.

3.4 Conclusion

The aim of this chapter was to design and implement a low impedance TRL fixture in order to provide high accuracy measurements of devices with very low impedances thus reducing the measurement error due to the large impedance mismatch between the 50 Ω VNA measurement environment and the low impedance device environment.

Testing and validation of the fixture was done by using an effective ε_r extraction method and using this to calculate the dielectric constant of the Rodgers substrate. Discrepancies between the calculated results and the Rodgers specification were attributed to the errors in measured transmission lengths and were taken into account when choosing valid data areas.

A final ε_r was calculated and used throughout the project and although it was slightly higher that the specification, 10.2 ± 0.25, of the Rodgers board, it corresponded sufficiently to validate the low impedance TRL measurement fixture.

Chapter 4 - LDMOS Equivalent Circuit Parameter Extraction

4.1 Introduction

When designing RF circuits, an intricate knowledge of the devices used in the system is required in order to correctly predict the RF behaviour and subsequently make the correct design decisions. The LDMOS amplifier circuits developed in this project are no exception. The method used in this chapter models the LDMOS devices using compact, equivalent circuit models to predict the RF behaviour of these devices [33] [24] [34] [35] [36]. The parameters of these equivalent models are then optimised in order to get the best possible fit between the S-parameter response of the model and the measured S-parameters of the device under various conditions.

There are four areas of design in which the equivalent circuit is used.

1. Load line impedance calculations
2. Low frequency stability analysis
3. Linear gain and frequency response predictions
4. Input match calculations

In LDMOS device, the equivalent circuit can be divided into three main sections. The first section contains the extracted package parameters. These represent the package elements such as inductance, capacitance and resistance associated with the gate and drain leads [9]. The second section contains the extrinsic parameters. They represent the reactances associated with the bond wire elements used to connect the device and the package. These extrinsic parameters are independent of bias conditions. The third section in the equivalent model contains the intrinsic parameters. These parameters are bias dependent, and represent the small signal FET parameters of the device.

This chapter will firstly present an equivalent circuit model for the package, extrinsic and intrinsic parameters. It will then extract preliminary values for all the elements within the model. The measured data will finally be used to optimise the element values so that the model predicted S-parameter data of the model fits the measured S-parameters.

4.2 LDMOS Package Parameter Extraction

In order to extract the package parameters, two empty BLL1214-35 L-Band radar transistor packages were obtained. These packages were measured using the low impedance test fixture. One of the packages was left empty to act as an open standard measurement while the other was filled with solder to act as a short standard measurement. These packages are shown in Figure 26, and illustrate the identical mechanical nature of the two packages. This figure is obtained from [24].

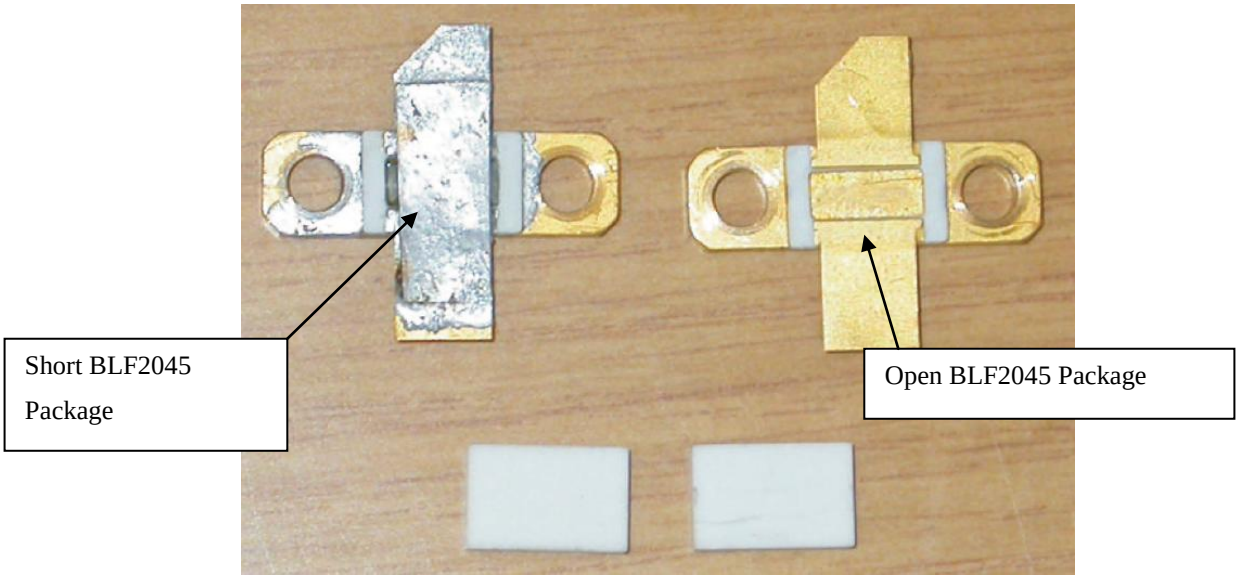

Figure 26 - Figure showing the open and "short-all" packages of the BLF2045

An advantage to using this method to extract the package parameters is that both the open and “short-all” standards have a common mechanical design and thus the tab models (shown in Figure 27 and Figure 28) are equivalent, allowing a simple parameter extraction process. This process is based on the methods described in [33].

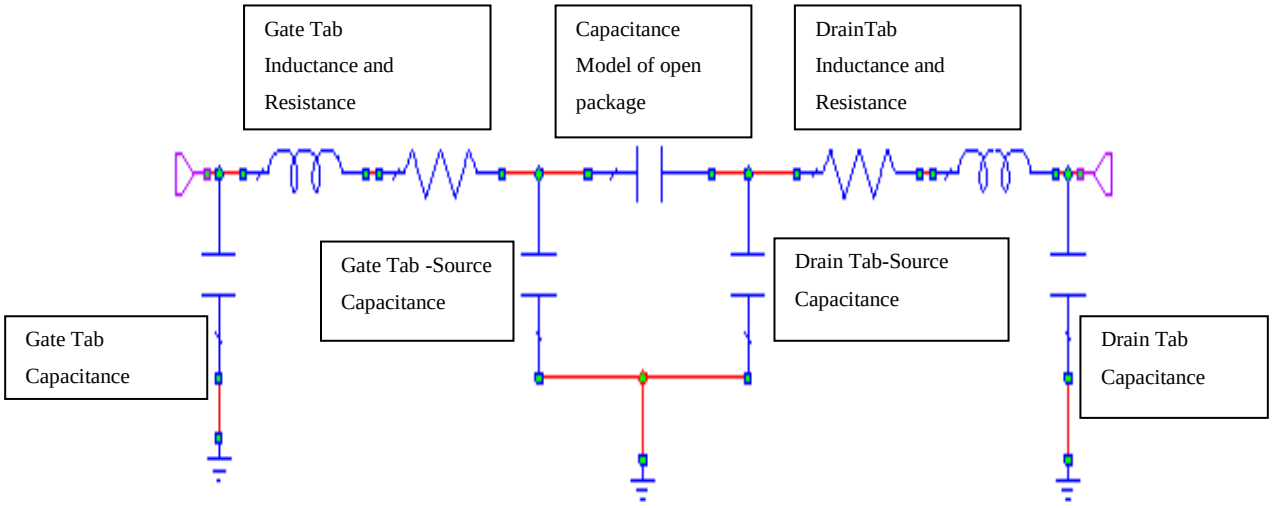

Figure 27 - Figure showing the open standard BLF205 model

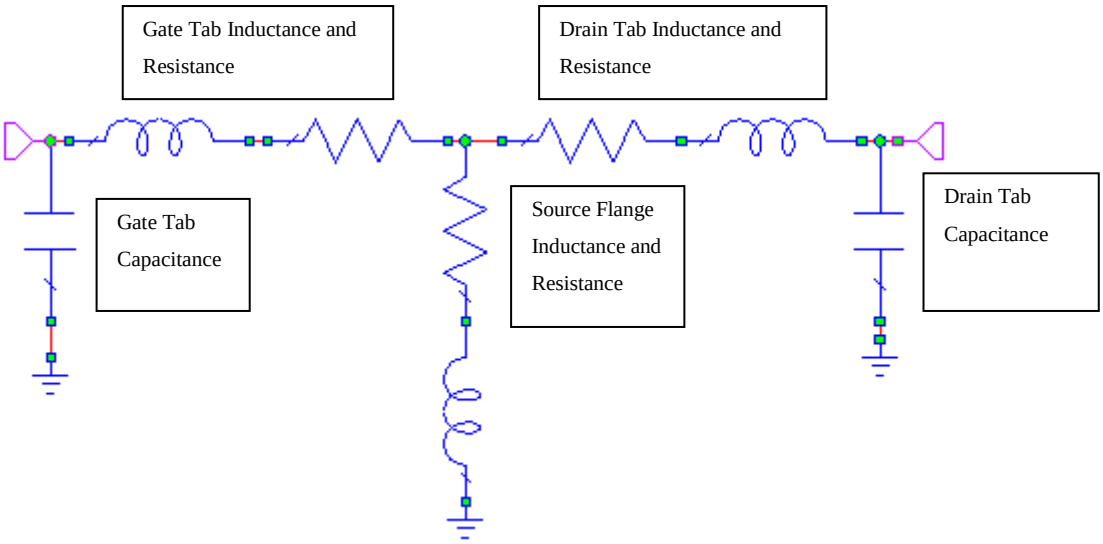

Figure 28 - Figure showing the 'short-all' standard BLL2045 model

The models are placed in AWR Microwave Office® and compared with the data obtained from the measured open and short packages. The values of the various model elements are then optimised until an accurate fit between the models and the data is obtained.

This optimisation is performed on the S_{11} and S_{22} data of both the open and short packages simultaneously in order to get the most accurate model of the package parameters. The comparison between the model and measured responses can be seen in Figure 29 and Figure 30, and illustrate the level of accuracy that these package parameter models provide. It can also be seen how important a high accuracy measurement setup is as the data resides in highly error sensitive areas on the edge of the Smith chart. The optimised package parameters are shown in

Table 4.

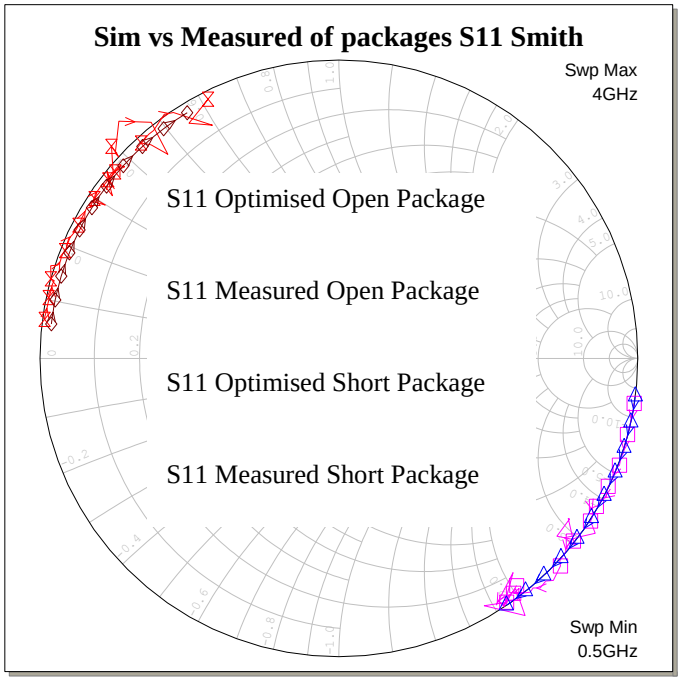

Figure 29 - Figure showing the Smith chart of the measured vs. the simulated S11 data of the open and “short-all” standards

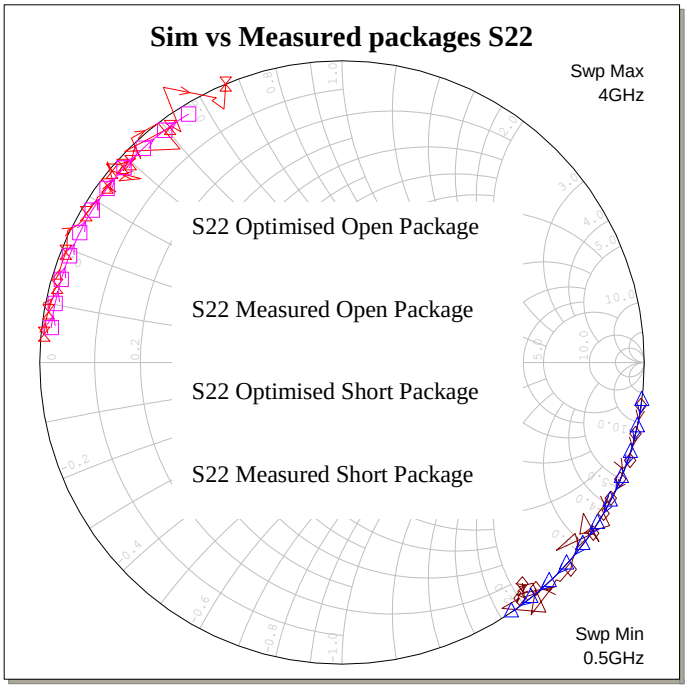

Figure 30 - Figure showing the Smith chart of the measured vs. the simulated S_{22} data of the open and 'short-all' standards

Table 4 - Table showing the extracted package parameters vs. the optimised package parameters

Element	Extracted Value	Optimised Value
C-Tab [pF]	2.2896	1.139
R-Tab [Ω]	0.0669	0.1197
L-Tab [nH]	0.17985	0.1946
R-Flange [Ω]	0.0094	0.04804
L-Flange [nH]	0.0070155	0.006869
C-Package [pF]	15.611	0.7718
C-Package-Coupled [pF]	-4.3257e-16	0

One should note that at the higher frequencies where the TRL calibration models begin to fail, the errors in the measurements become more apparent. It should also be noted that this does not pose a large threat to the design process as the RADAR devices will only be operated at the lower frequencies.

4.3 Extrinsic Parameter Extraction

Now that the package parameters have been established, the effect of the extrinsic parameters must be established and de-embedded. These parameters represent the series resistance, inductance and capacitance of the bond wires that exist between the package tabs and the device die itself. These parameters are extracted directly from the small signal measurements performed on a device in the zero bias (V_{GS} = 0 and V_{DS} = 0) cold condition. Before the extrinsic elements are calculated, the package elements are first de-embedded from the measured cold S-parameters.

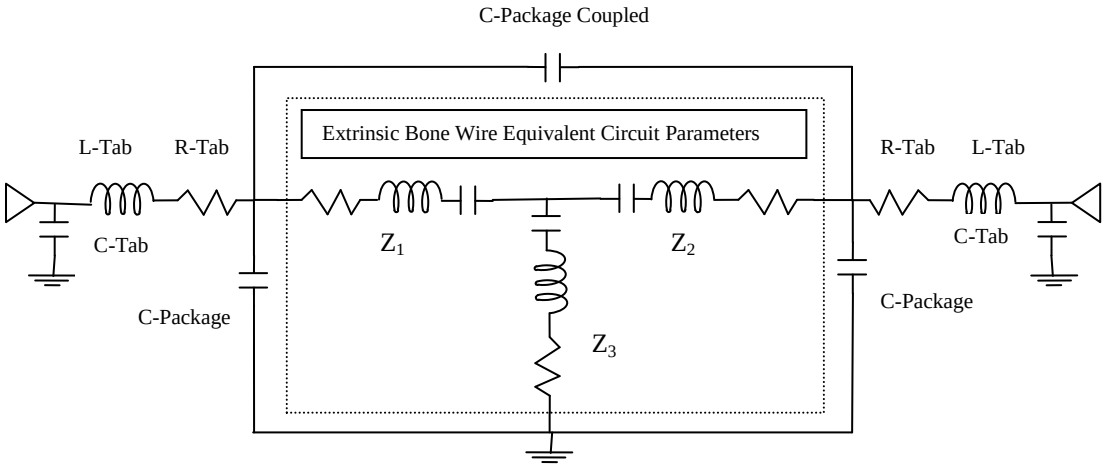

Figure 31 - Figure showing the model of both the package parameters and the extrinsic bond wire parameters of a BLF2045 transistor. This model is used for calculations but not to represent the device.

Figure 31 shows the model of the extrinsic parameters. The model depicts a star topology. In order to extract the complex reactance's of each branch of the model, the method described in [24] [33] was used. This firstly uses the measured z-parameters to extract the complex reactances

$$Z_1 = z_{11} - z_{12} \tag{23}$$

$$Z_2 = z_{22} - z_{12} \tag{24}$$

$$Z_3 = z_{12} \tag{25}$$

The branches, shown in Figure 31, are represented as follows:

$$Z_1 = R_g + j\omega L_g + \frac{1}{j\omega C_g} \tag{26}$$

$$Z_2 = R_d + j\omega L_d + \frac{1}{j\omega C_d} \tag{27}$$

$$Z_3 = R_s + j\omega L_s + \frac{1}{j\omega C_s} \tag{28}$$

At this stage a least-squares fit algorithm is used to determine the best possible values of the resistances, inductances and capacitances in each of the three branches. A star-delta transformation can then be used to convert the series capacitances into a Π network, shown in Figure 32, that is commonly used to model the intrinsic section of a FET.

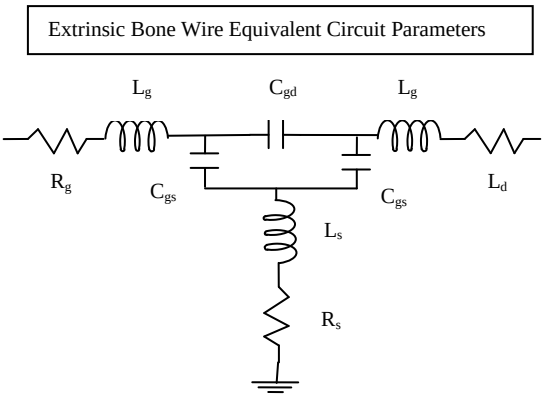

Figure 32 - Figure showing the model of the extrinsic bond wire parameters of a BLF2045 transistor.

As seen before in the chapter, the data measured resides in the very error sensitive area on the edge of the smith chart. The model was then optimised against the measured data in order to create an optimal fit between the simulated model response and the measured data.

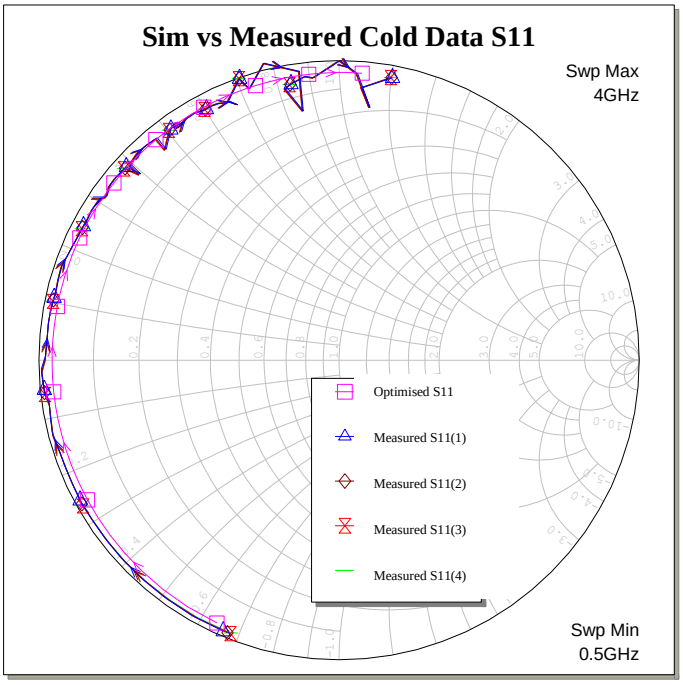

Figure 33 - Figure showing the S11 of the cold data measurement vs. the model simulations for the BLF2045 device

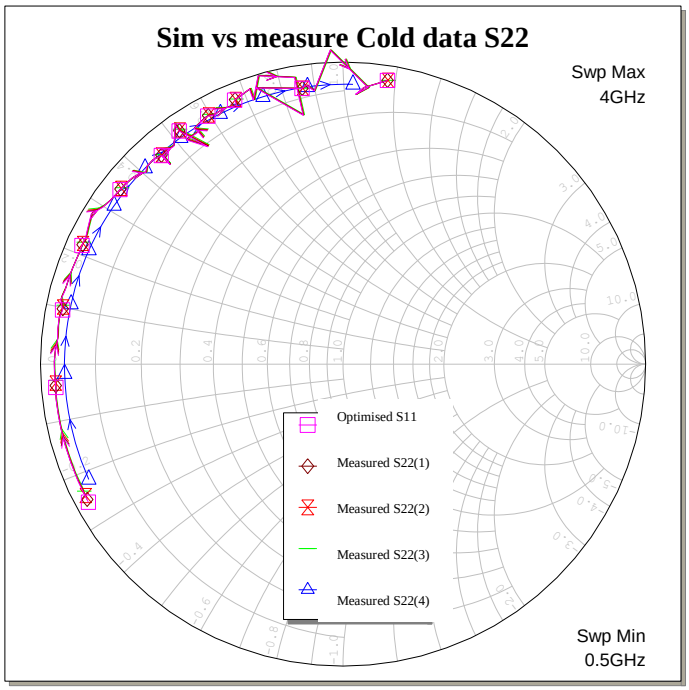

Figure 34 - Figure showing the S22 of the cold data measurement vs. the model measurements for the BLF2045 device

Table 5 - Table showing the initial calculated element values of the cold measurements vs. the optimised values of the corresponding elements

Element	Extracted Value	Optimised Value
C-Tab [pF]	2.2896	1.139
R-Tab [Ω]	0.0669	0.1197
L-Tab [nH]	0.17985	0.1946
R-Flange [Ω]	0.0094	0.04804
L-Flange [nH]	0.0070155	0.006869
C-Package [pF]	15.611	0.7718
C-Package-Coupled [pF]	-4.3257e-16	0
R-gate [Ω]	0.0596	0.1022
R-drain [Ω]	0.219	0.2977
R-source [Ω]	0.03867	0.01687
L-gate [nH]	0.1674	0.1683
L-drain [nH]	0.1324	0.1339
L-Source [nH]	0.01242	0.01206
Cgs [pF]	31.39	31.61
Cgd [pF]	8.367	7.504
Cds [pF]	86.6	87.08

Once again a very good fit was established, although there is a deviation from the measured data in the higher frequency range. This is due to the fact that the measurement uncertainty is higher at the upper frequency ranges. As before this can be ignored as the device will only operated at the lower frequencies.

4.4 Intrinsic Parameter Extraction

The final step in the process is to extract the intrinsic circuit parameters for the BLF2045 LDMOS device. These parameters model the small signal behaviour of the device while active specific bias point. As the extrinsic and package parameters are known, they can be de-embedded from the active S-parameter measurements of the device, thus yielding the S-parameters of the active device. In order to simplify simulations within Microwave Office, an existing small-signal device was used within the model.

In order to gain a better understanding of the device, measurements at several bias points were taken. The device is being used in a high power design so the bias point with the largest drain bias current was chosen. This is due to the large signal behaviour of the final power amplifier which effectively biases the device at a higher bias point than the class-B quincent bias point at which the FET is initially biased.

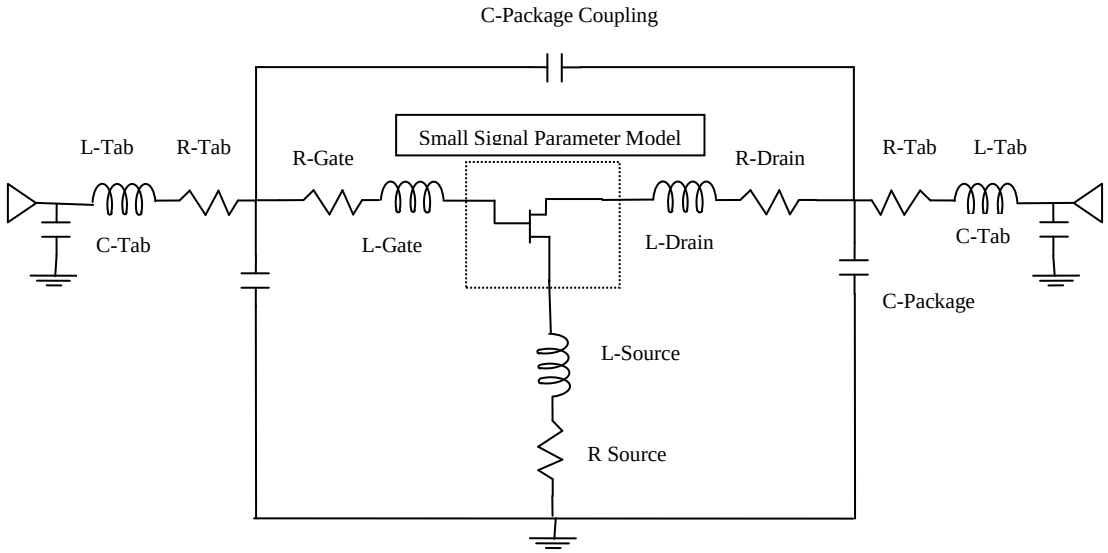

Figure 35 - Figure showing the intrinsic small signal device model within the extrinsic and package elements. The bond wire capacitances are included in the small signal device model.

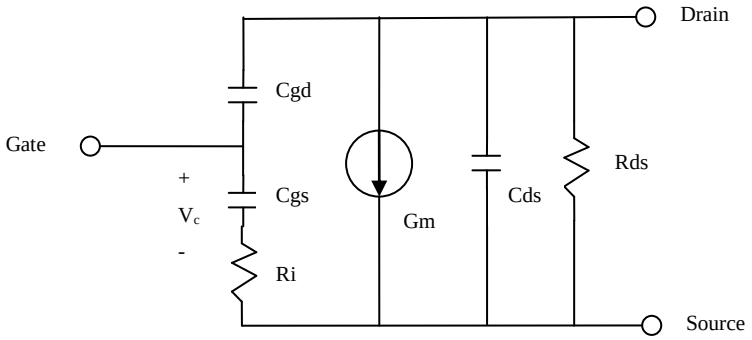

Figure 36 - Figure showing the intrinsic small signal parameter model

After de-embedding the package and extrinsic parameters from the active measurements, the S-parameters of the device are transformed into their Y-parameter format for ease of use. The Y-parameters can then be written as a combination of the intrinsic parameters [24].

$$y_{11} = \frac{{C_{gs}}^2\omega^2}{D1} + \frac{\omega^2 R_{gd}{C_{gd}}^2}{D2} + j\omega\left(\frac{C_{gs}}{D1} + \frac{C_{gd}}{D2}\right) \quad 29$$

$$y_{12} = -\frac{\omega^2 R_{gd}{C_{gd}}^2}{D2} - j\omega\frac{C_{gd}}{D2} \quad 30$$

$$y_{21} = \frac{gm\, e^{-j\omega\tau}}{1 + j\omega C_{gs}} - j\frac{\omega C_{gd}}{1 + j\omega R_{gd} C_{gd}}$$

31

$$y_{22} = \frac{\omega^2 R_{gd} {C_{gd}}^2}{D2} + j\omega\left(C_{ds} + \frac{C_{gd}}{D2}\right)$$

32

where,

$$D1 = 1 + \omega^2 {C_{gs}}^2$$

33

$$D1 = 1 + \omega^2 {C_{gd}}^2 {R_{gd}}^2$$

34

At this stage the separation of the real and imaginary parts of the Y-parameters allows the intrinsic model parameters to be extracted [24].

$$C_{gd} = \frac{Im(Y_{12})}{\omega}\left(1 + \left(\frac{Re(Y_{12})}{Im(Y_{12})}\right)^2\right)$$

35

$$C_{gs} = \frac{Im(Y_{11}) + Im(Y_{12})}{\omega}\left(1 + \frac{(Re(Y_{11}) + Re(Y_{12}))^2}{(Im(Y_{11}) + Im(Y_{12}))^2}\right)$$

36

$$C_{ds} = \frac{Im(Y_{22}) + Im(Y_{12})}{\omega}$$

37

$$R_{ds} = \frac{Re(Y_{22}) + Re(Y_{12})}{\omega}$$

38

$$R_{gd} = \frac{Re(Y_{12})}{\omega C_{gd} Im(Y_{12})}$$

39

$$g_m = \sqrt{((Re(Y_{21}) - Re(Y_{12}))^2 + (Im(Y_{21}) + Im(Y_{12}))^2 D1}$$

40

$$\tau = \frac{1}{\omega}\arcsin\left(\frac{Im(Y_{12}) - Im(Y_{21}) - \omega C_{gs}(Re(Y_{21}) - (Y_{12}))}{g_m}\right)$$

41

The intrinsic parameters are valid for all frequencies within the measurement range. As mentioned earlier in this chapter, they are bias dependent, and the bias point chosen was the highest possible bias current allowable within the SOA (Safe Operating Area).

In order to ensure an accurate match between the extracted parameter sets and the measured data, models were implemented in MWO and an optimisation was performed.

Figure 37 to 41 show the measured results of the BLF2045 device as well as the corresponding optimised model response.

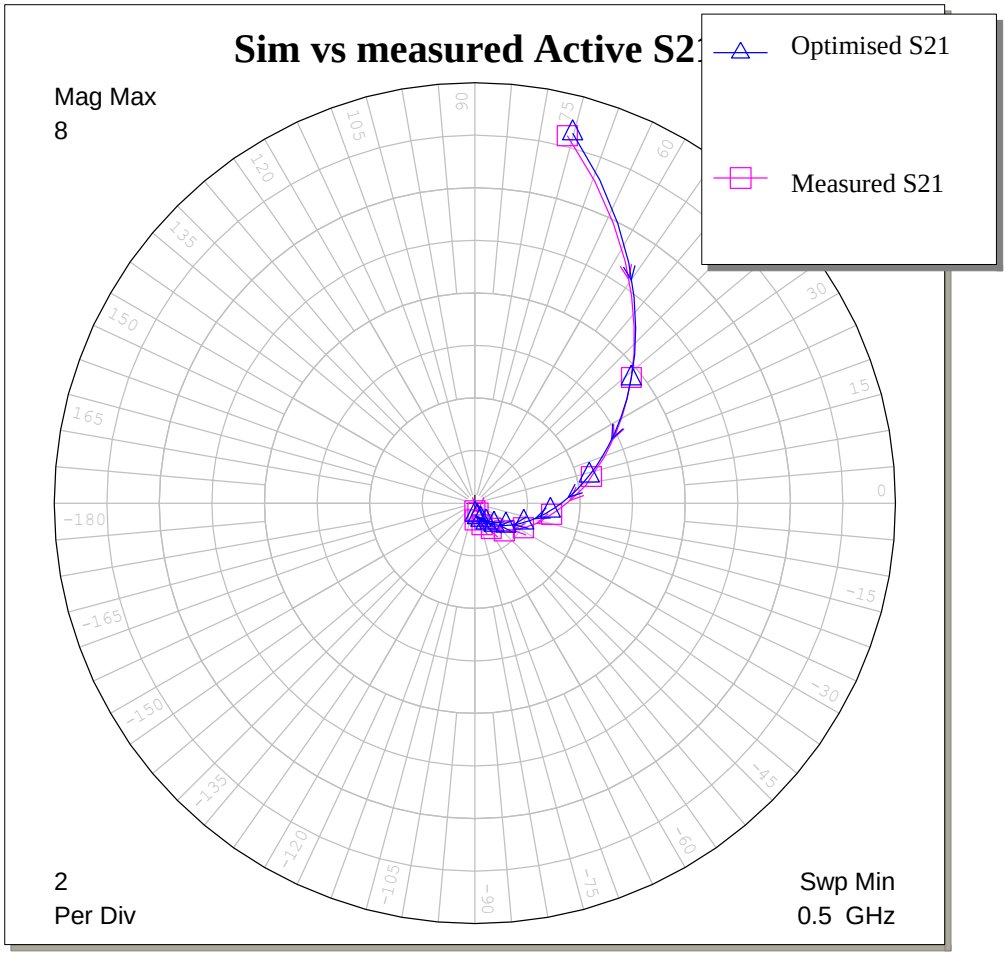

Figure 37 - Figure showing the measured S21 of the BLF2045 vs. the optimised model response

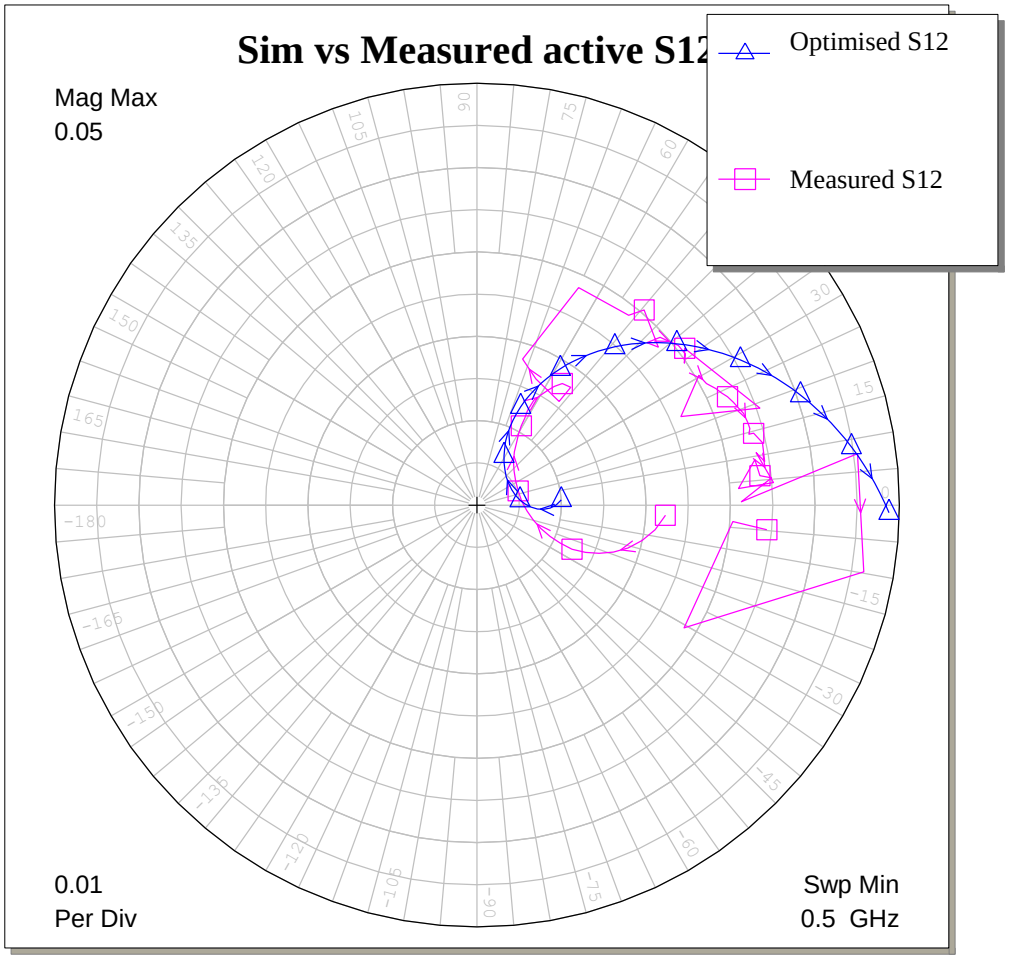

Figure 38 - showing the measured S12 of the BLF2045 vs. the optimised model response

One should note that the measured S_{12} results shown in Figure 38 do not correspond to the optimised model values as accurately as the S_{21} response of the model shown in Figure 39. This is due to the fact that measurements of S_{12} are near the noise floor of the measurement environment and thus less accurate. This is not a problem as the device response is dominated by S_{21}.

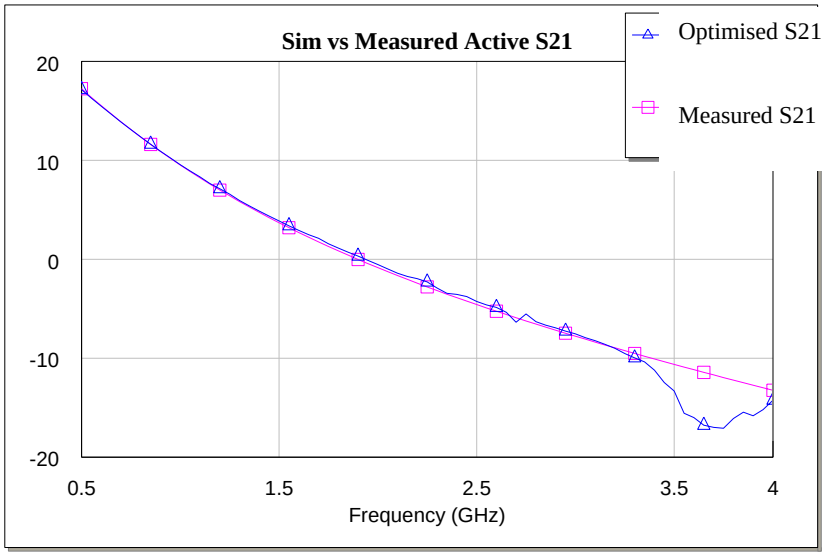

Figure 39 - showing the measured magnitude of the S21 of the BLF2045 vs. the optimised model response

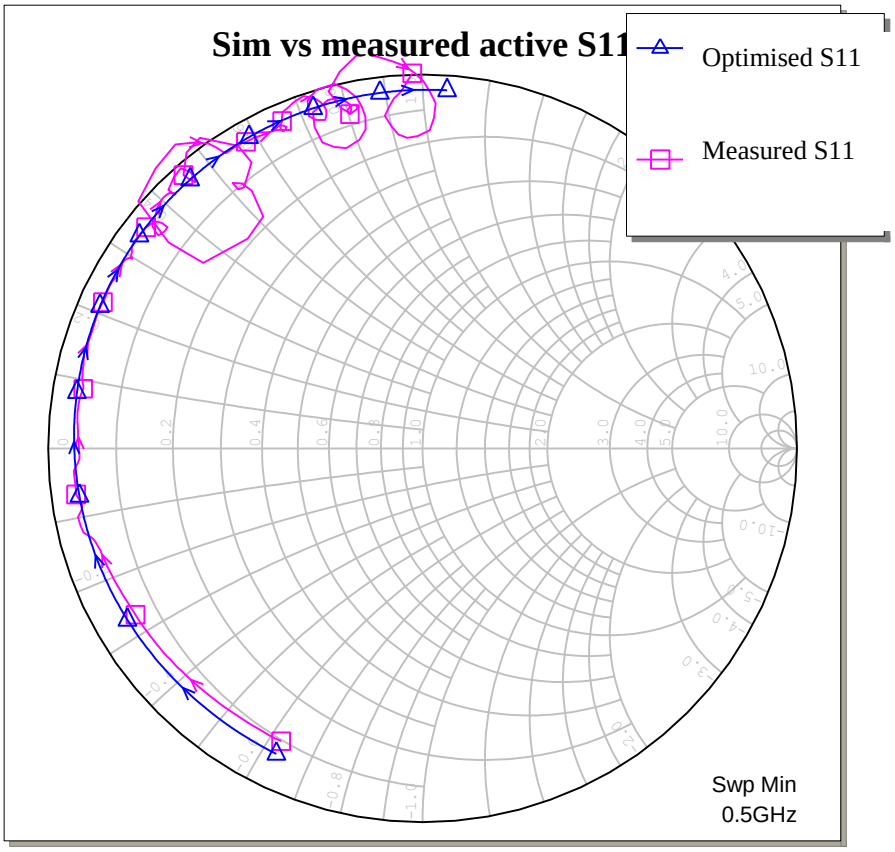

Figure 40 - showing the measured input reflection S11 of the BLF2045 vs. the optimised model response

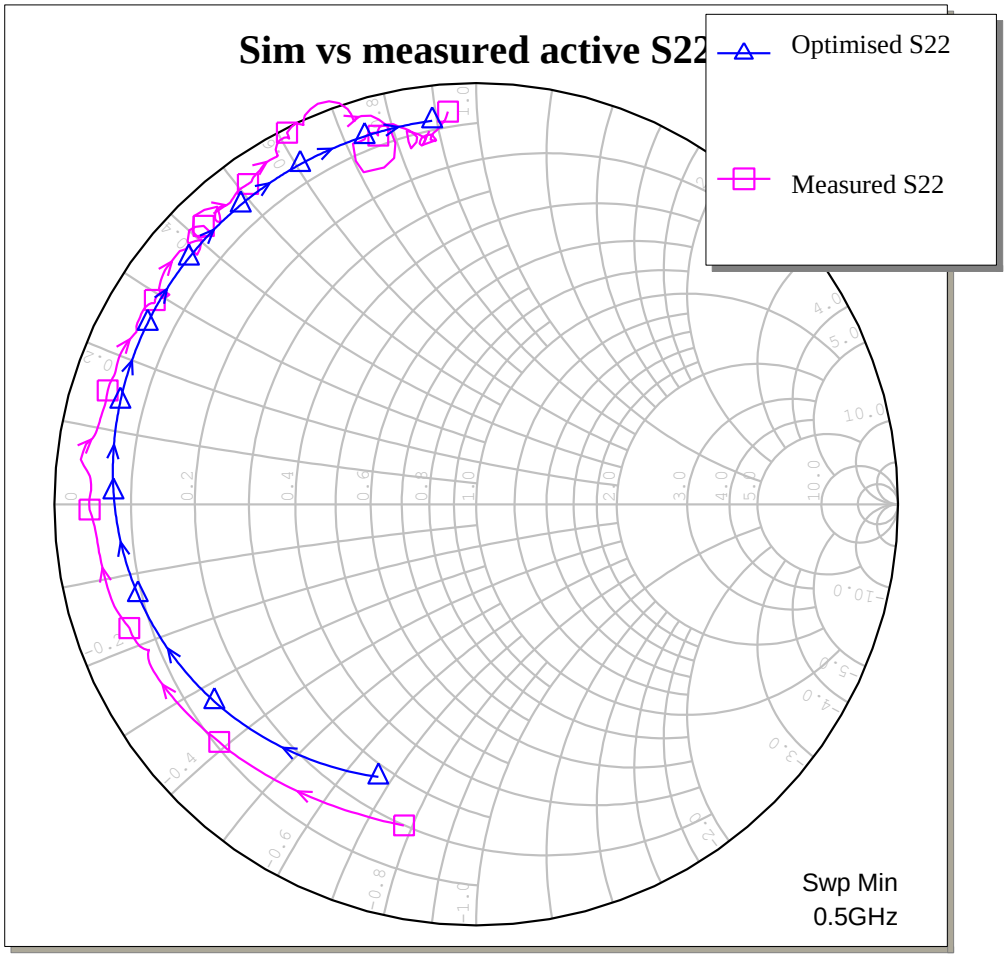

Figure 41 - showing the measured output reflection S22 of the BLF2045 vs. the optimised model response

Table 6 - Table showing the extracted values of the intrinsic parameters of the BLF2045 vs. the optimised intrinsic parameter values for the BLF2045

Element	Calculated Value	Optimised Value
Cgd [pF]	1.0989	0.5381
Cgs [pF]	32.76	36.27
Cds [pF]	32.364	32.55
Ri [Ω]	-0.1353	0.11775
Rds [Ω]	-50.5458	38.79
Gm	0.9276	0.9954
Tau [pS]	9.8459	11.81

Table 6 shows a numerical comparison between the extracted intrinsic parameter values and the final optimised parameter values. One notices a close tie-up between the extracted model parameter values and the optimised model parameter values. This is with the exception of the extracted Ri and Rds parameters. These model elements are highly sensitive to noise and measurement induced errors. These errors are removed from the model by optimisation.

4.5 Conclusion

This chapter firstly used an empty and fully shorted device package to determine the effect the package has on the RF response of a BLF2045 device. This response was then modelled and the model was compared and optimised to actual measured values in order to ensure a great accuracy.

The next step used a functioning BLF2045 device in the zero bias condition (V_{gs} = 0, V_{ds} = 0) to measure and model the effect that the extrinsic parameters of the device have on the RF response of the BLF2045. These results were again optimised to ensure accuracy.

The final step was to measure the active response of the BLF2045 at a high bias point in order to measure and model the effect of the intrinsic parameters of the BLF2045 device. Once again an optimisation was used to ensure an accurate model to measurement fit.

All final models tie up very closely to the measured results in each step, which allows for a better design process in the latter stages of the project. A further encouraging result of this chapter is that the preliminary extracted value of the parameters and the final optimised values only differ slightly which in part verifies the validity of the extraction process.

Chapter 5 – Power Supply Design

5.1 Introduction

In RADAR amplifier power supply design, as in all power supply design, the ability of the supply to provide constant and reliable power to the load under all types of operating conditions is the largest factor to consider when going through the design process. This issue is however exacerbated by the fact that the power output of the RADAR device is delivered in pulses of varying duration and repetition rate.

The power supply designed is based on an initial design by Prof PW van der Walt of Reutech Radar Systems.

5.2 Operating Principals

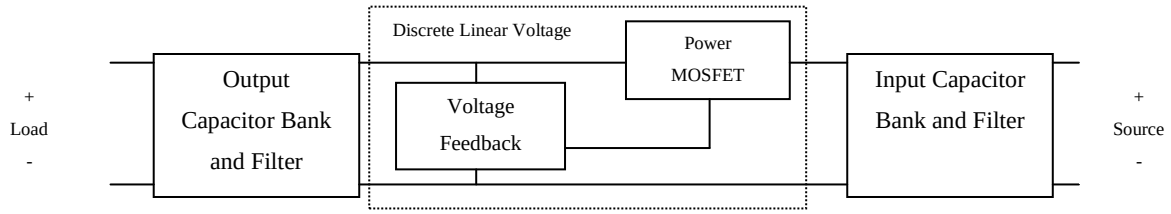

Figure 42 - Block Diagram of pulsed power supply

The power supply consists of four sections as seen in Figure 43. First, is the input capacitor bank and filter stage. This stage provides charge storage for the power supply and minimises the voltage ripple.

The second stage is the four parallel power MOSFETs. These are switched on when a signal is received from the voltage feedback section. This allows a rapid flow or charge from the input capacitor bank in order to recharge the output capacitor bank. The four MOSFETS are placed in parallel to reduce the series resistance.

The third stage, the voltage feedback section, senses the drop in voltage of the output capacitor bank, and in turn signals the power FET switch to close and thus raises the output voltage. This sensing is achieved by implementing a high impedance voltage division network from the output voltage to ground which allows the output voltage to be proportionally reduced to a 5V level. This is compared with a precision 5V voltage regulator using a negative feedback THS4031 [16] op-amp level detector. A drop in output voltage results in a positive gate voltage (V_{GS}) on the n-channel IRFRU110 MOSFET [37]. This allows current to flow through the pull up 220Ω resistor. This results in a negative gate voltage (V_{GS}) on the p-channel IRF4905 MOSFET [38]. This allows current to flow through from the input capacitor bank into the output capacitor bank. This results in

an increase in the voltage of the output capacitor bank which results in a proportional increase in voltage to the reference 5V level. This gradually reduces V_{GS} of the IRFRU110 and reduces the current through the MOSFET.

The final stage is the output capacitor bank and filter. This section provides the primary charge storage for the amplifier load. As the amplifier pulses, the capacitor bank accommodates rapidly changing current draw. It also has a high frequency filter to suppress the voltage transients caused by the parasitic inductances of the circuit wires as the current rapidly changes. A 100uH air core inductor is used to prevent RF from reaching the power supply unit.

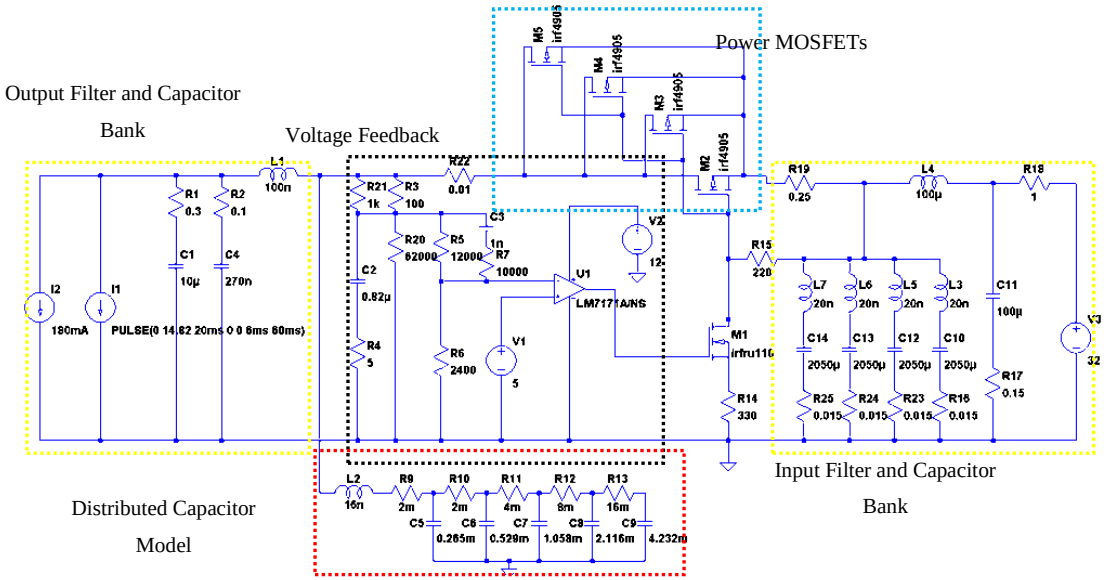

Figure 43 - Figure showing model schematic used in the simulation of the pulsed power supply including the distributed capacitor model used to predict the pulsed response of the power supply

5.3 Practical Implementation

There are 4 major issues to consider when designing a power amplifier (PA) power supply. The foremost issue is the choice of capacitors. The capacitors must be able to handle relatively large voltage (up to 50V) while still having the largest possible capacitance for a compact size. The capacitor must also have very low parasitic inductances and ESR. This factor ruled out the use of axial capacitors as the long leads are far too inductive. It was finally decided that large surface mount (SMD) capacitors were the only option. Eight 1000µF SMD capacitors were used in each of the capacitor banks. In order to reduce the inductance of the capacitor layout, 4 capacitors were placed in a square configuration on both the top and bottom of the substrate board. The top and bottom tracks were joined at multiple points with vias.

The second issue was the choice of MOSFET switches. The switches must obviously be able handle the high voltages and current of a PA power supply, as well as having the lowest possible ‘on’ resistance, as the power

dissipation of each MOSFET switch is directly proportional to the series resistance the switch. With these factors in mind, International Rectifier – IRF4905 HEXFET ® Power MOSFETs were chosen. These provide a very fast switching time (± 100ns) as well very low $R_{DS(ON)}$ resistance of 0.02Ω per MOSFET switch. In order to further decrease the resistance of the switch stage of the power supply, it was decided to place four of the switches in parallel; thus decreasing the series resistance to ±0.005Ω.

The issue of power dissipation is tightly linked to the MOSFET switches, as they are one of the areas of series resistance between the power supply and the PA. It was found that the parallel configuration was sufficient in lowering the power dissipation to relatively low levels. It should be noted that there is also a series resistor (1Ω) present at the input to the circuit, and that this does dissipate large amounts of power. Unfortunately this is unavoidable although its self heating effect was reduced by large wattage resistors in parallel to achieve the effective resistance.

The final issue to keep in mind when designing a PA power supply is the layout. When deciding on the layout, the most important part of the design principal is to keep the parasitic inductances, as well as the series resistances as low as possible. This in turn would keep the losses within the power supply, as well as the power dissipation, low and allow the response time of the power supply to be as fast as possible.

The layout was designed in a series approach using both sides of the substrate board. This allowed a better utilisation of space, and thus all transmission lines can be kept as short as possible. These transmission lines were also designed to be as wide as possible, within the space provided, in order to minimise their series resistances.

5.4 Test and Evaluation

The initial tests were performed using a test jig which simulated the effective resistance of a device under maximum current. This test was performed at a maximum of 10% duty cycle and 100µs pulse width. This is the maximum requirement for most modern RADAR systems. It was found that the test setup was not sufficient to test the power supply under more rigorous conditions, as the power dissipation proved to great and sections of the testing jig, mainly soldering, began to melt.

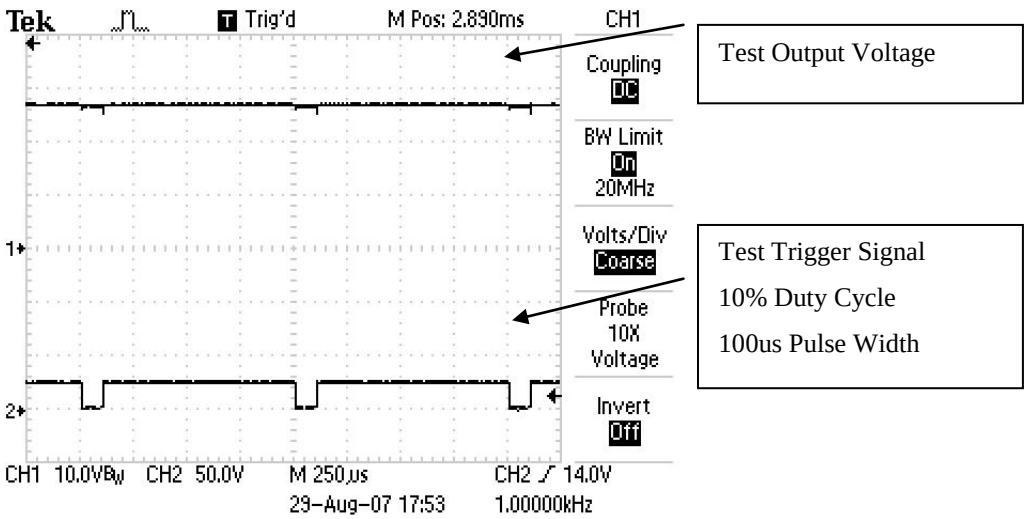

Figure 44 - Figure showing output voltage of power supply during initial tests at the maximum specifications of 10% duty cycle and 100us pulse length

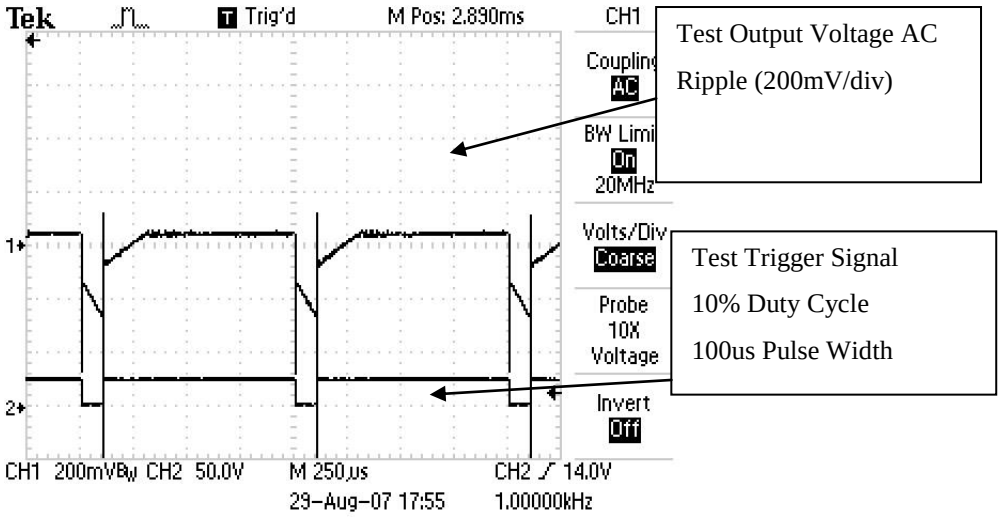

Figure 45 - Figure showing power supply AC ripple during initial tests at the maximum specifications of 10% duty cycle and 100us pulse length.

These initial results, shown in Figure 45, indicated that at the maximum duty cycle of 10%, and pulse width of 100us the resulting voltage ripple is less than 300mV. This would not degrade the performance of even the high power 250W amplifier.

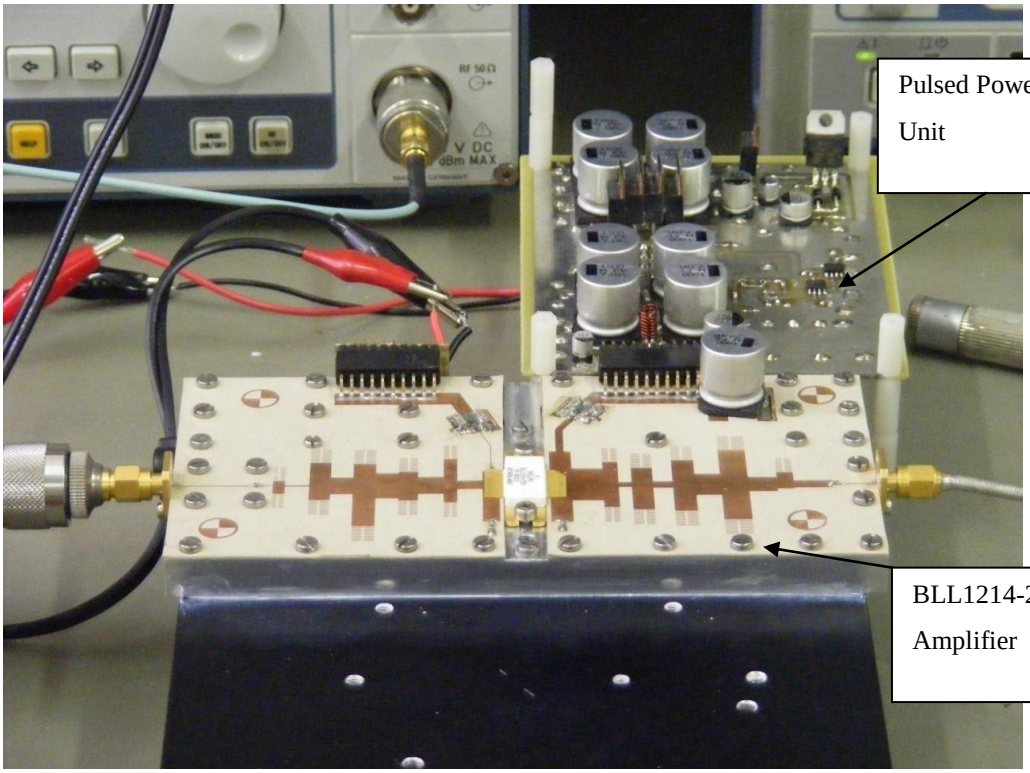

Figure 46 - Figure showing the power supply connected to the BLL1214-250 250W amplifier used in the final power supply evaluation.

The final test was performed during the operation of the BLL1214-250 amplifier operating at a maximum output power of ±54dBm.

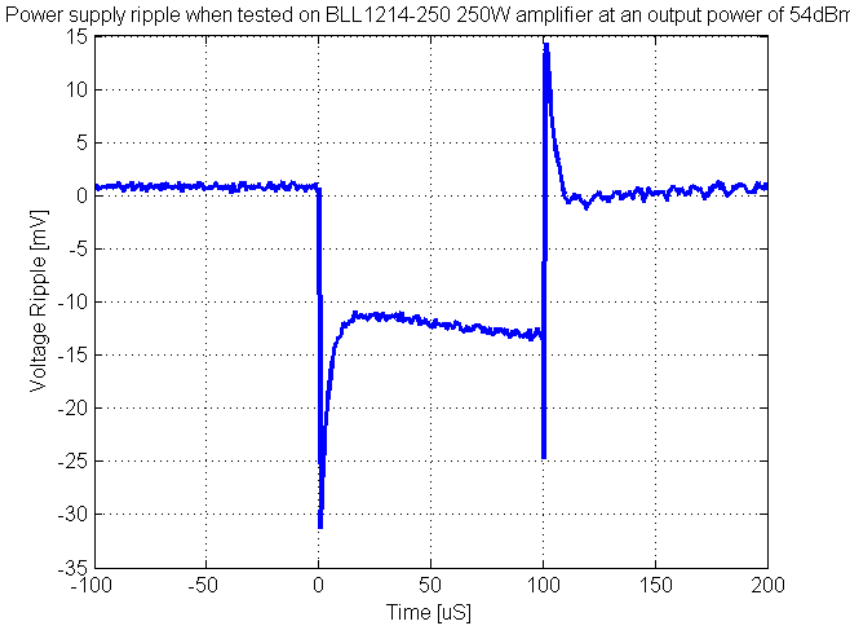

Figure 47 - Figure showing measured power supply ripple during final BLL1214-250 250W amplifier operation at output power of +-54dBm at a 10% duty cycle.

The measured results, shown above, show a more than acceptable voltage ripple on the output voltage of the power supply at the highest possibly load.

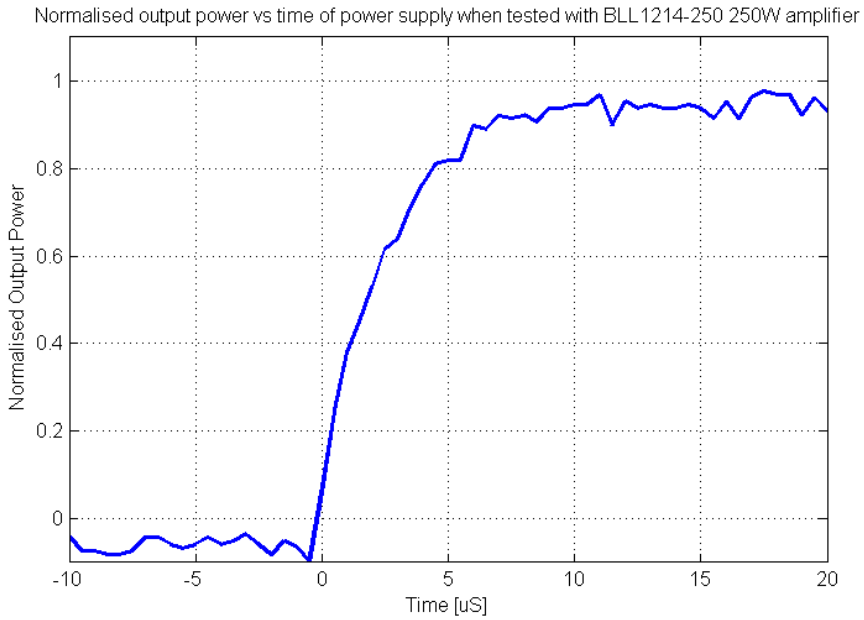

Figure 48 - Figure showing the normalised power output of the BLL1214-250 250W amplifier, indicating the power supply's ability to rapidly supply current to the amplifier.

The ability of the power supply to provide a rapid rise time current supply to the amplifiers is indicated in Figure 48. A 10% to 90% rise time of 5µs was achieved.

5.5 Conclusion

The aim was to design and test a power supply that would be able to provide a constant and reliable voltage under typical RADAR operating conditions.

The results show that the power supply was more than adequate in providing a high power amplifier with sufficient power quality with a rapid rise time. This helps greatly in the pulse repeatability of the final amplifier, as well as helping to minimise the pulse droop.

Chapter 6 – BLF2045 Amplifier Design

6.1 Introduction

The aim of this chapter is to investigate the feasibility of using an unmatched BLF2045 [39] commercial device in order to design and manufacture a high power 1.2GHz-1.4GHz L-band RADAR amplifier [40] [41].
There are various advantages to using a commercial device as opposed to a pre-matched military device. Firstly, commercial devices are much more easily obtainable as there are little or no restrictions on their purchase. Secondly, as they are unmatched, they can be used in a variety of frequency bands. Thirdly, as they are commercially made, they are much cheaper. One should also note that there are also disadvantages to using a commercial device as opposed to a military device. The fact that the device is unmatched, while providing versatility, also means that the design of the amplifier is that much more difficult. Thus the design risk is greater. A further disadvantage is that, as commercial devices are not used in military situations, they do not have to conform to military specifications of robustness and reliability, and thus are more likely to fail. This can also mean that the lifetime of the commercial device can be limited when compared to a military device.

The design of an amplifier using an unmatched device is performed in several stages.

1. DC and pulsed I-V measurements.
2. Multi bias S-Parameter characterisation using equivalent circuit parameter extraction.
3. DC bias circuit design.
4. Output matching network design in order to achieve optimal output load for maximum power transfer.
5. Input matching network design.

This chapter will begin by implementing a load line placement amplifier design using the data gathered, and models developed in chapters 2, 3 and 4.
This chapter will then focus on the design and implementation of the DC bias networks and the design of the input and output matching networks used in the amplifier implementation.
This chapter will then describe and discuss the measurements of the final design and draw conclusions as to its feasibility as an alternative to equivalent amplifiers based on military devices.

6.2 Amplifier Design

6.2.1 Optimum Load Line placement

In order to establish the optimal load, the I-V characteristics of the device must be analysed. One needs to establish the quiescent drain bias point of the device, the knee point of the amplifier, where the device begins to enter saturation and the drain-source current which corresponds to the knee voltage. A factor of two is included in the calculation of the optimal output load as the RF voltage at the drain swing equally both sides of the quiescent drain bias point.

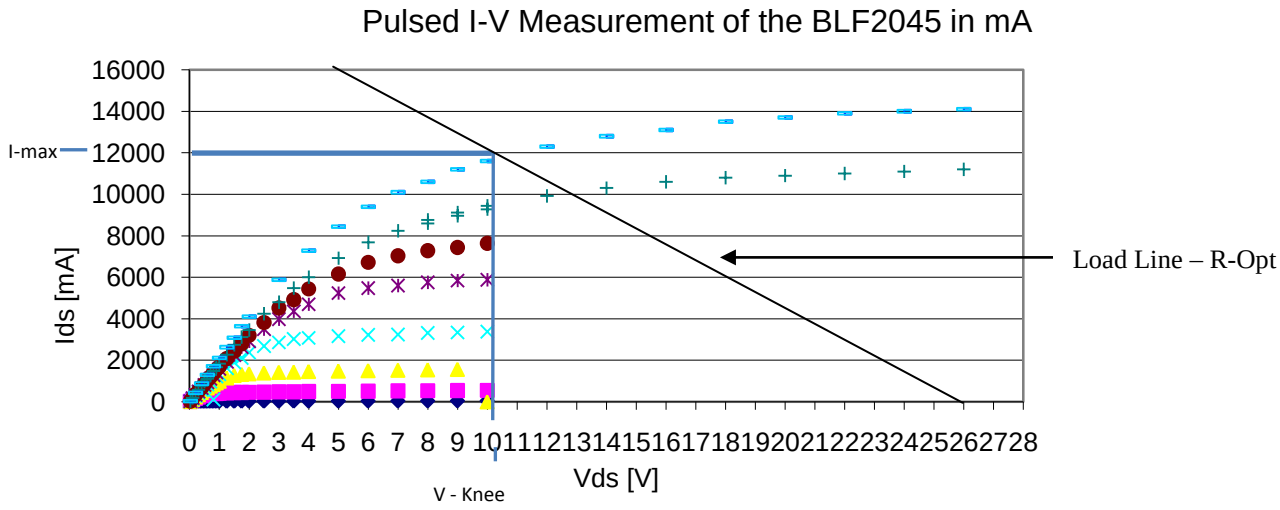

Figure 49 - Figure showing the pulsed I-V curve for various Vgs and load line placement

$$Ropt = \frac{(Vdsq - Vknee)}{\frac{Imax}{2}} \quad (42)$$

Vdsq = 26V

Vknee = 10V

Imax = 12A

R_{opt} = 2.67 Ohm

Thus in order for maximum power output, if a perfect 50Ω load is attached to the output of the amplifier then a constant, a purely real load of 2.67Ω should be seen from the current source.

6.2.2 Output Network Design to Achieve Power Match

The aim of this section is to design and implement an external matching network that would ensure that the load seen from the current source within the equivalent circuit of the BLF2045 device is a constant optimal load throughout the operating bandwidth of 1.2-1.4GHz. This ensures maximum possible current and voltage swing of the output and thus maximum output power. This method differs from a more traditional conjugate match method which ensures maximum power transfer but not necessarily maximum power.
The matching network must include the DC bias network which would supply the amplifier with power.

6.2.2.1 Output Bias Network Design

The purpose of the DC bias network is to provide the output section of the amplifier with the power required to generate the RF output signal. A short transmission line connects the drain of the BLF2045 to the external DC power source.
The length of the transmission line was chosen to be λ/4 at 1.6 GHz, shown in Figure 50. A large storage capacitor was placed close to the amplifier to provide energy directly to the amplifier with the minimum possible series inductance. Due to the RF short, the bias network acts as an open circuit at 1.6GHz. The open circuit point was chosen slightly higher than the operating frequency of 1.2-1.4 GHz in order to ensure that the DC bias network remains inductive, and presents high impedance to RF, throughout the operating band. This can be seen in the Figure 51. This provides high impedance for the RF output power, ensuring that the system does not leak any RF power to the bias network. Several ceramic capacitors were placed at λ/4 from the drain in order to suppress any possible RF components from leaking back to the DC power supply. A snubber circuit, consisting of a capacitor and resistor in series, was also placed λ/4 away from the drain to assist in the suppression of RF signals.

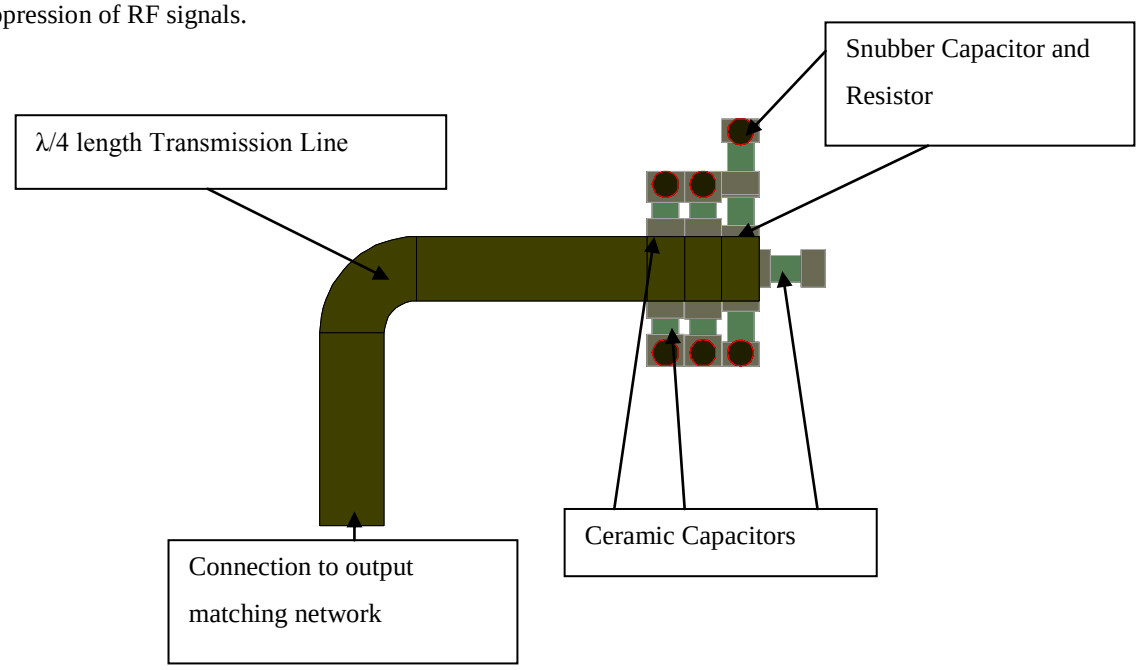

Figure 50 - Figure showing the model layout of the output DC bias network

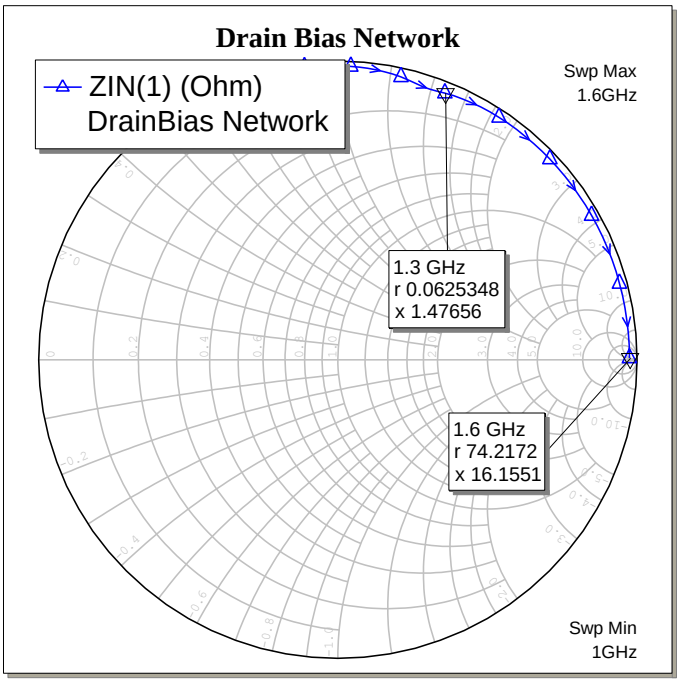

Figure 51 - Figure showing the smith chart of the output DC bias network

This matching network must include the DC bias network as well as the impedance transformation network. It must also take the intrinsic, extrinsic and package parameters into account within its design.

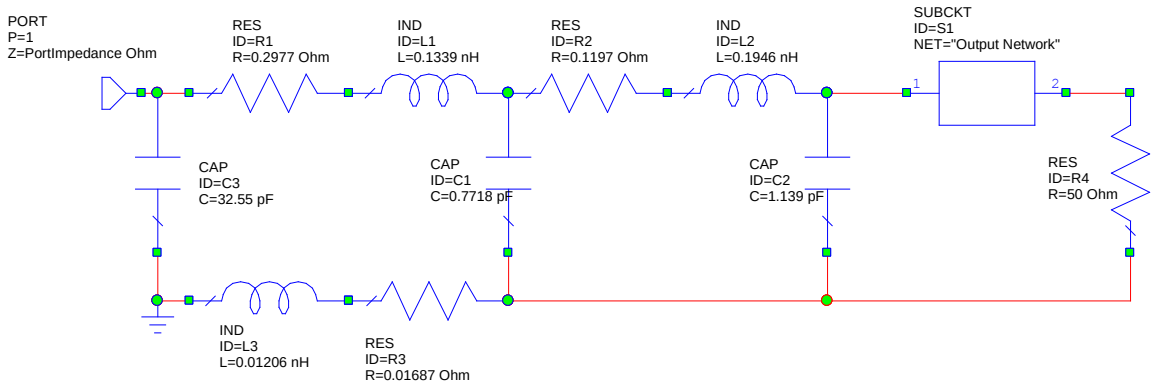

Figure 52 - Figure showing the schematic of the load as seen from the current source within the BLF2045 including the output matching network which takes the DC bias network into account

As in all high power amplifier implementations, the output impedance is very low, in the range of 0.5-5Ω. In order to transform such a low impedance to a 50Ω load a Chebyshev Short Step Impedance Transformer [42] was used. This method requires three items of information. These being the fractional operating band width-ω,

the Impedance mismatch ratio-r and the number of sections-n. Using these, the impedance of each matching network section can be obtained from tables included in [42].
The fractional operating bandwidth ω is given by:

$$\omega = \frac{\theta_2 - \theta_1}{\theta_m} \quad (43)$$

where:
Θ_1 is the start frequency
Θ_2 is the end frequency
Θ_m is the centre frequency
ω is the bandwidth

and

$$\theta_m = \frac{\theta_2 - \theta_1}{2} \quad (44)$$

The impedance mismatch ration r is given by:

$$r = \frac{Z_0}{Z_{n+1}} \quad (45)$$

where:

Z_0 is the initial impedance
Z_{n+1} is the final impedance
n is the section number
r is the impedance mismatch ratio

The number of sections (n) is chosen by evaluating the space available and the mismatch ratio. The more sections, the better the match will be over the band, but the more space it will take. It was decided that 12 sections would be required. Unfortunately the tables used only caters for up to 10 sections. Thus it was decided to create a two stage transform network where Z_{n+1} for the first transformation network becomes the Z_0 for the second transformation network.

A series DC de-coupling capacitor was also implemented to prevent any DC current from flowing to the load. In addition, a shunt capacitor was placed within the matching network. This allowed the optimisation algorithm

to add a large capacitance if needed. This network was then optimised in Microwave Office, by implementing alternating short sections of wide and narrow transmission lines, to obtain the desired load. Figure 53 shows the resulting desired load across the 1.2GHz to 1.4GHz bandwidth. There is a slight variation from 2.67Ω. The imaginary component of the load is kept lower than an absolute value of 0.75. Over such a bandwidth this was shown to be the best optimised solution. Figure 54 shows the implemented BLF2045 amplifier.

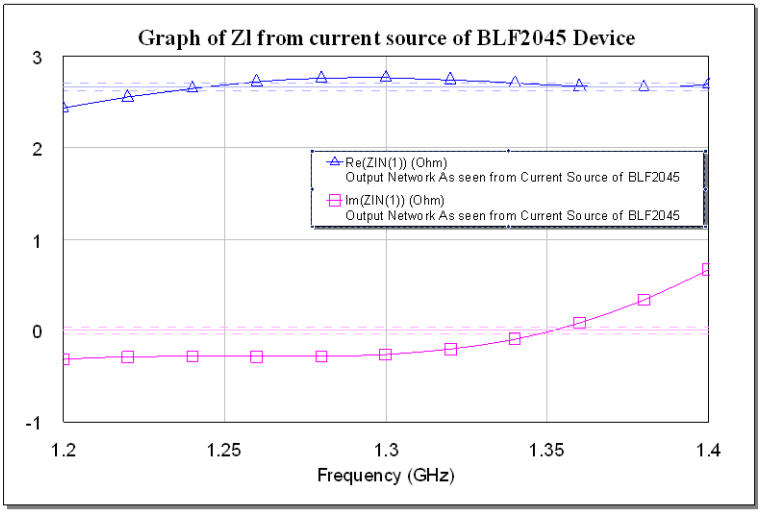

Figure 53 - Figure showing the simulation of the final load as seen from the current source after optimisation

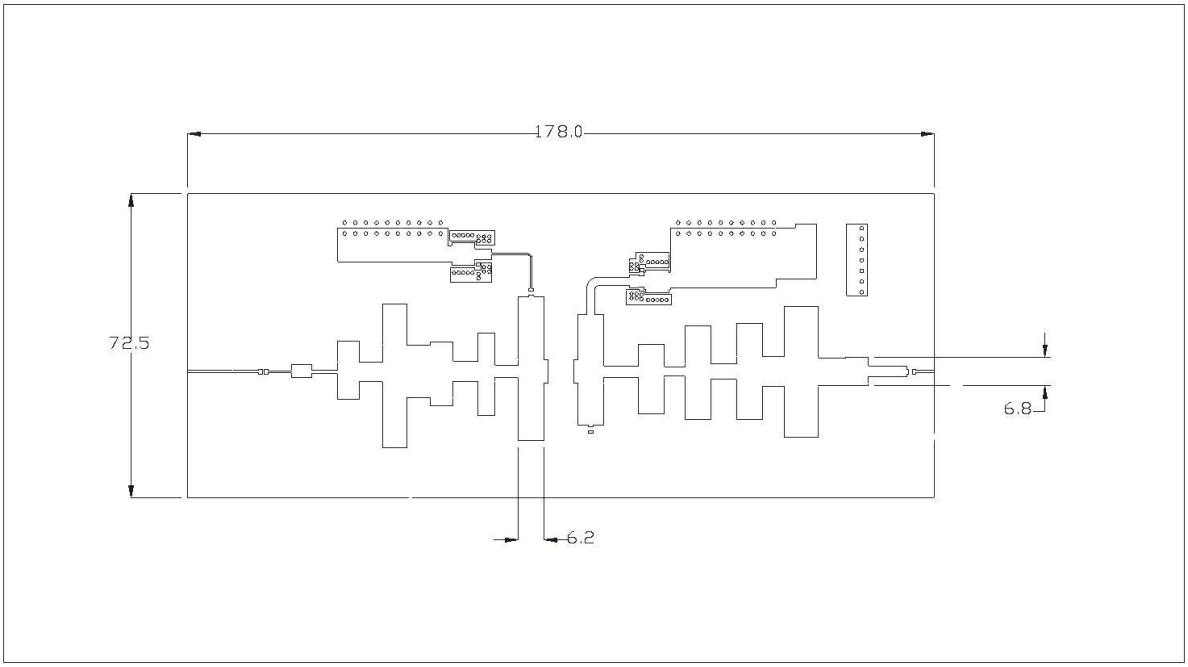

Figure 54 - Figure showing the final input and output matching network of the BLF2045 amplifier including the DC bias network, the impedance transformation network and the DC de-coupling capacitor

6.2.3 Input DC Bias Network Design

The purpose of the input DC bias network is similar to that of the output bias network, although whereas the output bias network provides the high power needed to generate the RF signal, the input bias network biases the BLF2045 in a class AB condition. Thus the device can be seen as being just on. A short transmission line connects the gate of the BLF2045 to the external DC power source.

The length of the transmission line was again chosen to be λ/4 at 1.6 GHz. Several ceramic capacitors were placed at λ/4 from the drain in order to suppress any possible RF components from leaking back to the DC power supply, and to ensure a RF short. Due to this RF short, the bias network acts as an open circuit at 1.6 GHz. It was again chosen slightly higher than the operating frequency of 1.2-1.4 GHz in order to ensure that the DC bias network remains inductive throughout the operating band. A snubber circuit was also place λ/4 away from the drain to assist in the suppression of RF signals. The width of the transmission line in the input bias network was chosen to be 2mm as the series impedance was not an issue as the current through the bias network was very low. A resistor was placed in series with the bias network in order to help stabilise the amplifier. This resistor provides an increase in the shunt resistance to ground thus loading the device. This helps to dissipate any out of band energy which could help sustain an oscillation.

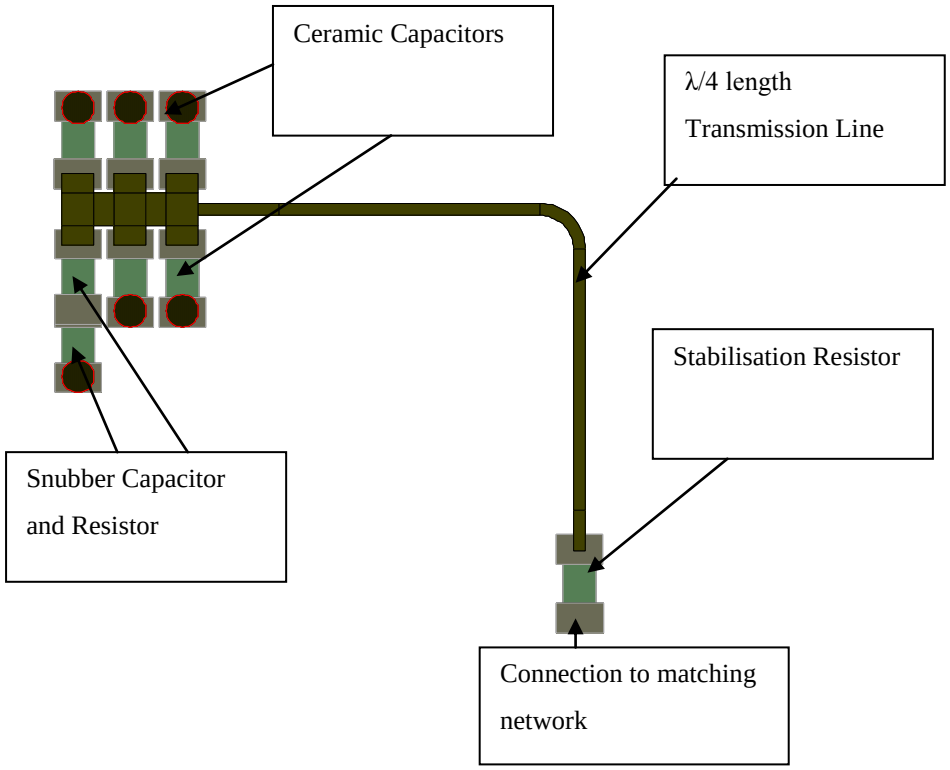

Figure 55 - Figure showing the design of the output DC bias network

6.2.4 Input Matching Network Design

The aim of this section is to design and implement a conjugate match input network for the BLF2045 amplifier. This is to ensure that the maximum power is transferred into the amplifier.

The first step is to use the S-parameters, simulated from the equivalent circuit determined in chapter 4, to find the S_{11} as seen from the input of the device. The next step is to design a conjugate match network.

A Chebyshev Short Step Impedance Transformer [42] was again used to create the impedance transformer. A series DC de-coupling capacitor was again implemented. The full network was then optimised for both input match, S_{11}, as well as the S_{21} gain.

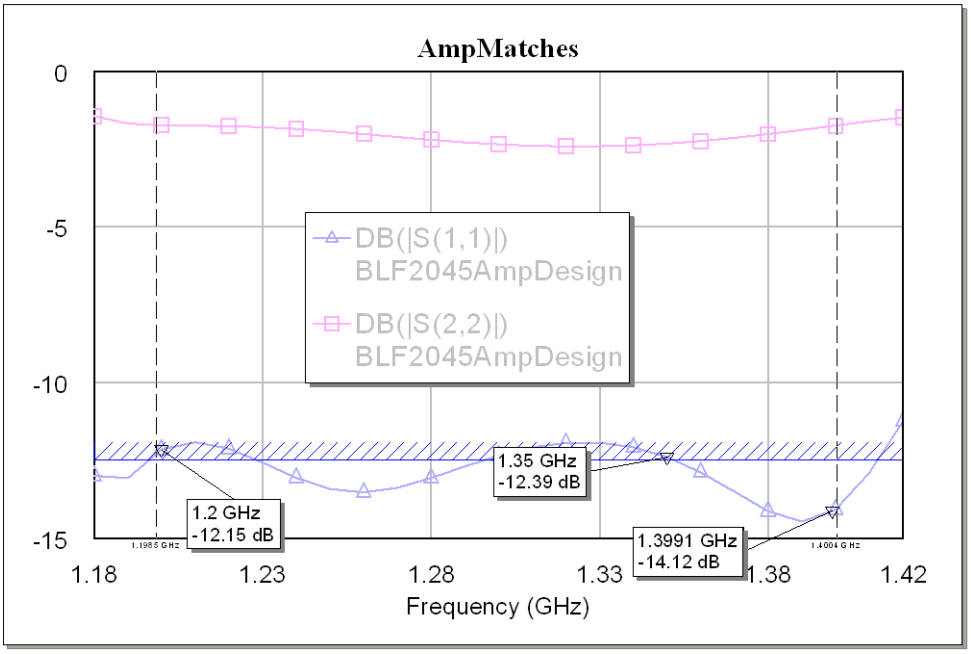

Figure 56 - Figure showing the final simulated S_{11} and S_{22} of the amplifier within the operating L-Band

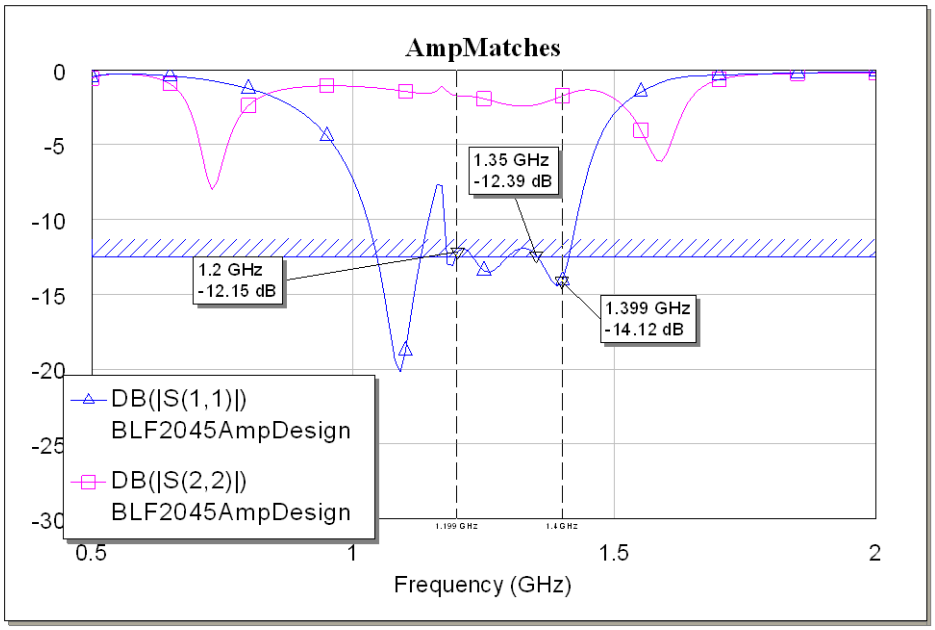

Figure 57 - Figure showing the simulated S_{11} and S_{22} of the final amplifier over from 0.5-2Ghz

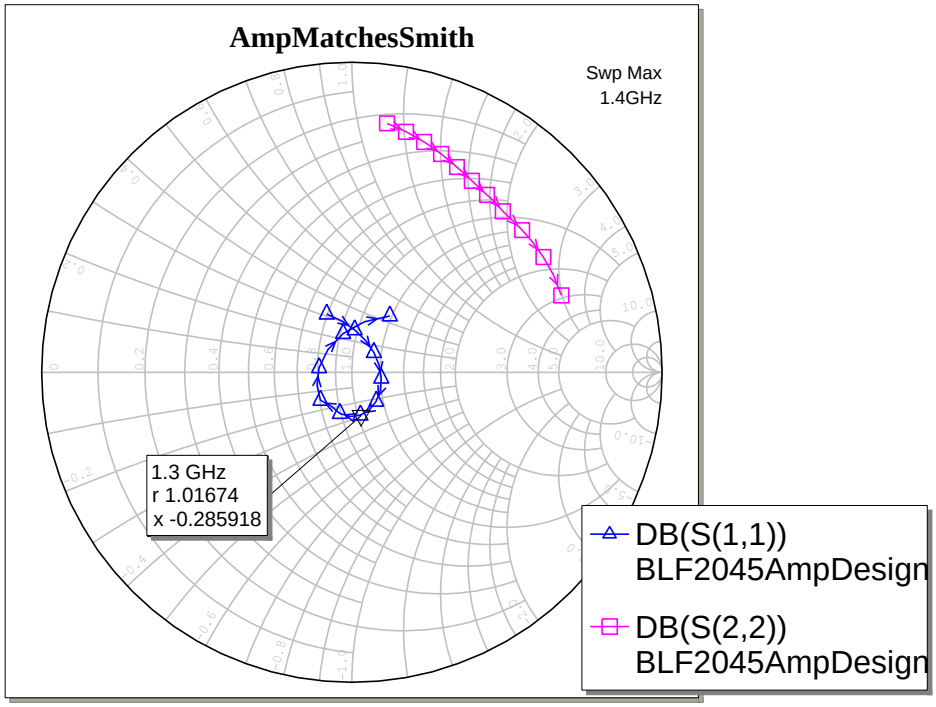

Figure 58 - Figure showing the smith chart of S_{11} and S_{22} of the final BLF2045 amplifier design

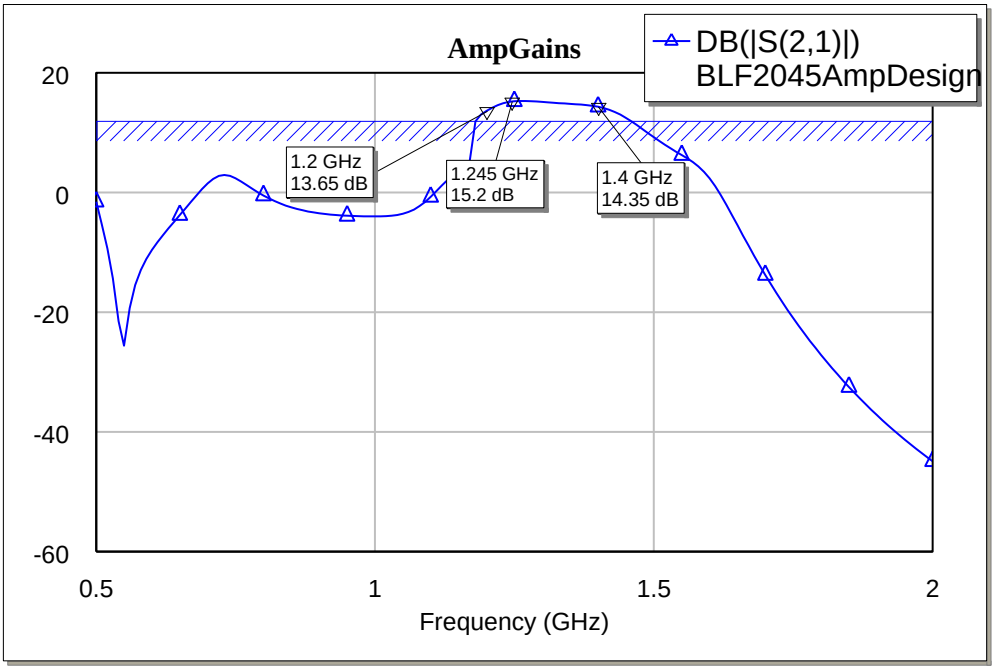

Figure 59 - Figure showing the simulated S_{21} of the final BLF2045 amplifier design from 0.5-2GHz

It should be noticed that, in Figure 58, the final s_{22} is not as good as the s_{11}. This is due to the fact that the output was designed for maximum power output whereas the input was designed with a conjugate match in mind. An overall gain of over 12 dB was achieved in the final simulation.

The overall circuit stability was simulated as a final test to ensure that the amplifier remained stable at all frequencies. This simulation was performed over a wide frequency range to ensure unconditional stability.
The stability analysis was performed within Microwave office using the built-in algorithms. These algorithms include μ1 and μ2 stability criteria, B and K stability criteria as well as stability circles.

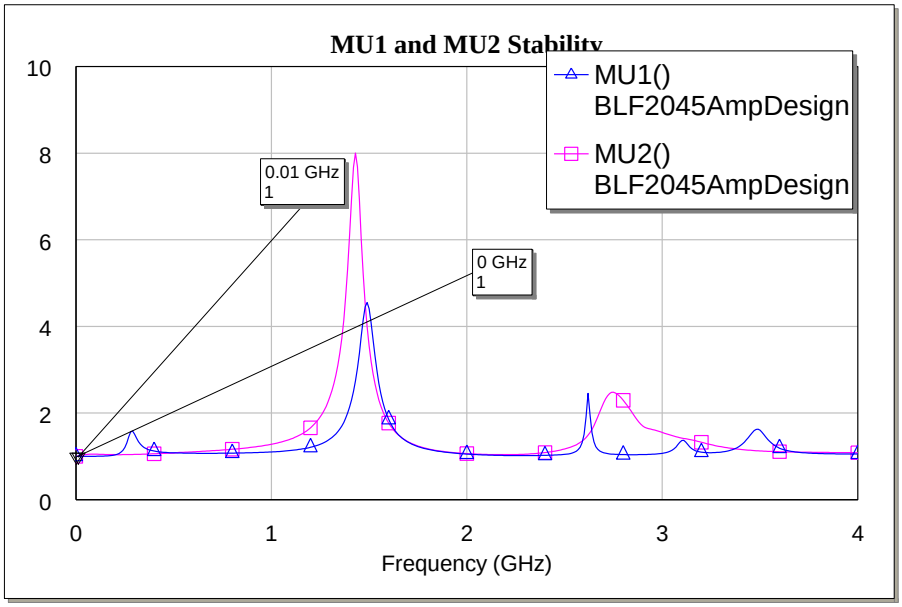

Figure 60 - Figure showing graphs of μ1 and μ2 stability criteria

In the μ1 and μ2 stability analysis, shown in Figure 60, the values of μ1 and μ2 must be greater than 1 to ensure un-conditional stability.
The simulations showed that the BLF2045 should remain stable at all frequencies up to 4 GHz.

6.3 Results

6.3.1 Measurement setup

The first step in testing of any amplifier is to ensure that the device does not oscillate under any conditions. If oscillations were to occur it could permanently damage the amplifier as well as any other device connected to it.

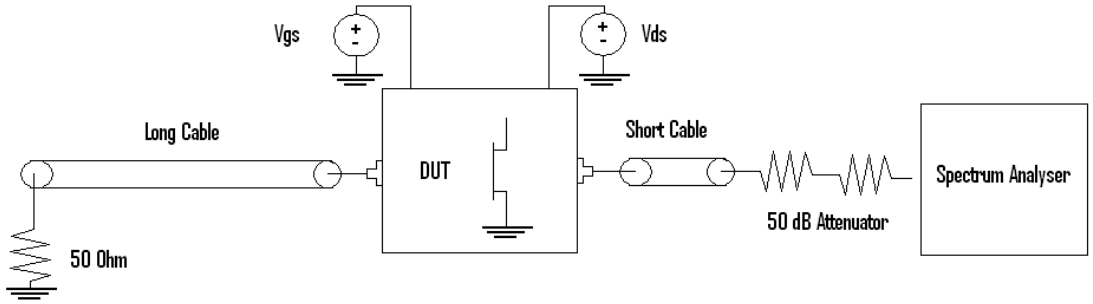

Figure 61 - Figure showing the setup to test the stability of a DUT

The setup shown in Figure 61 was used to test the stability. The gate voltage, V_{gs}, is tested at 0V as well as at the quiescent bias condition of 2.47V. The drain voltage V_{ds} is kept at the device specified 26V. Any oscillation would result in a visible spike on the spectrum analyser. A long section of cable is connected to the input of the DUT, as this would increase the chance of instability.
The DUT showd no signs of oscillations and thus was safe to connect directly to a VNA without the chance of damage.

The next step is evaluating the small signal S-parameter performance of the amplifier. This is done by connecting the device directly to the VNA. One must ensure that the power output at each of the ports is sufficiently low as to protect the VNA from a possible RF overload. In this test the V_{gs} is kept at quiescent bias condition of 2.47V and V_{ds} is kept at 26V.

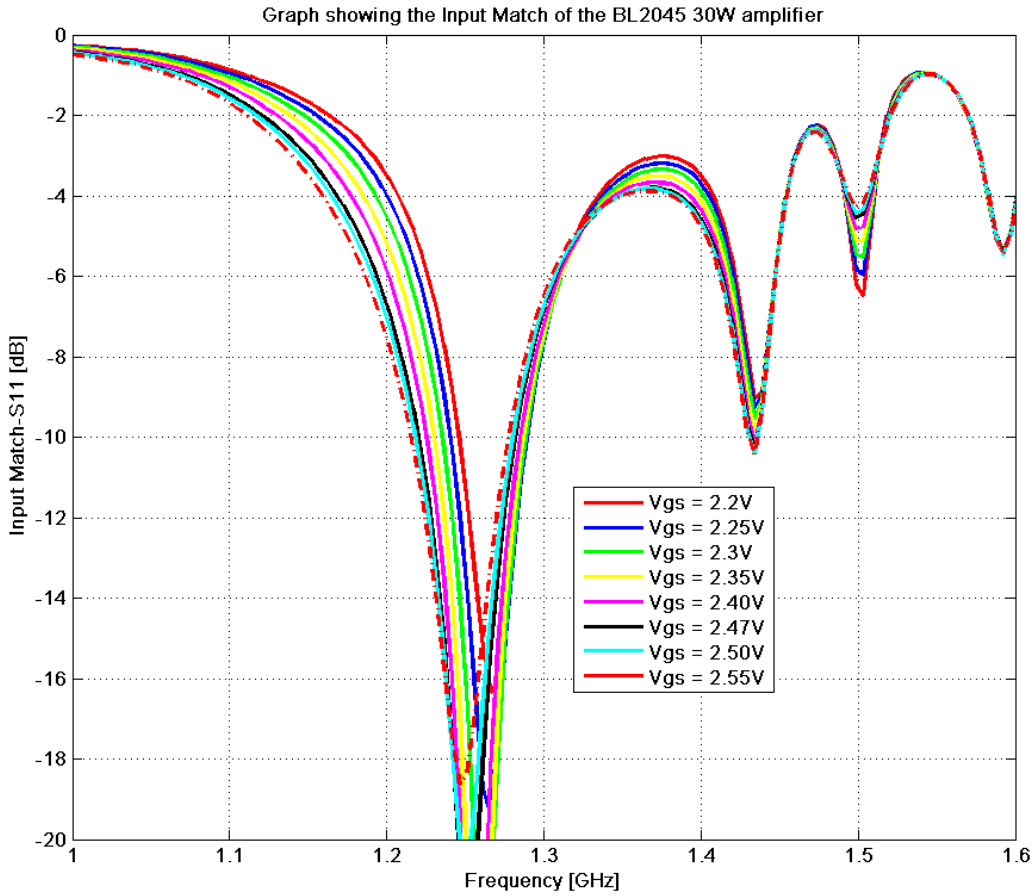

Figure 62 - Figure showing the measured small signal s-parameter S_{11} measurement of the BLF2045 30W amplifier

The measured S_{11}, shown in Figure 62, shows a relatively good input match, although is not as good as the simulated match shown in Figure 56. The centre frequency is 1.25GHz and not 1.3GHz. The bandwidth is lower than predicted.

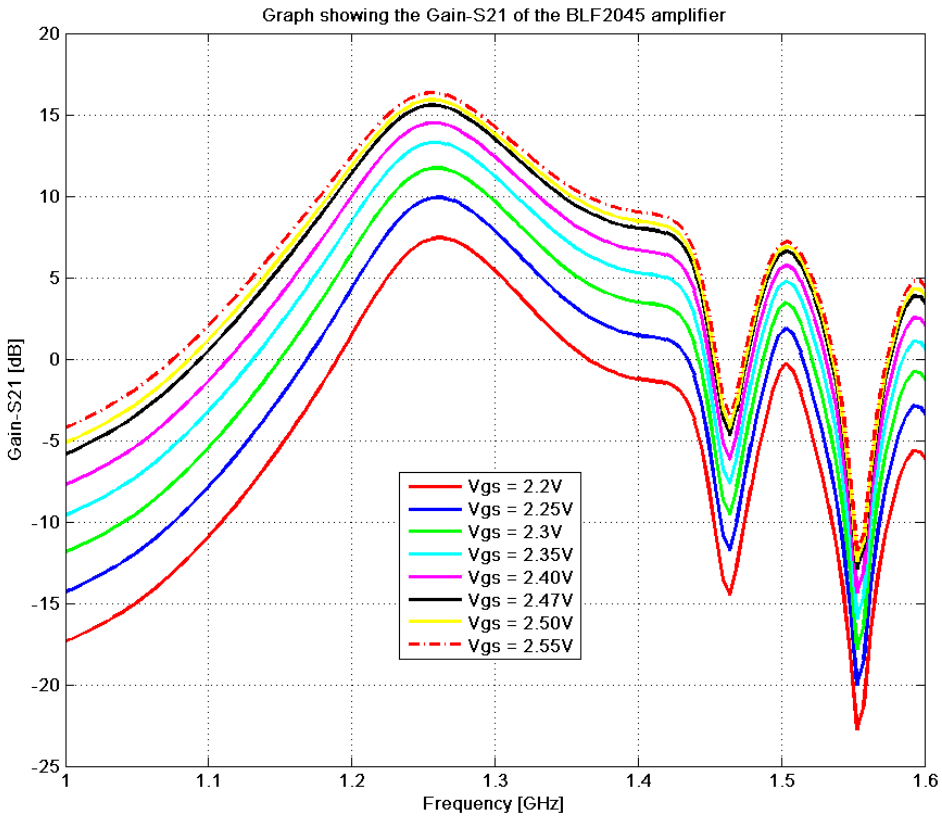

Figure 63 - Figure showing the measured small signal S_{21} gain measurement of the BLF2045 30W amplifier

The measured S_{21}, shown in Figure 63, shows good gain above 10dB, although the gain variation is greater than simulated gain shown in Figure 59. The centre frequency is 1.25GHz and not 1.3GHz. This frequency also corresponds to the point at which the effective load seen by the current source is exactly 2.67Ω as shown in Figure 53. It is possible that this is a result of the optimum load being seen by the current source, but it is likely that this is a coincidence and that the input match at this frequency is the dominant factor in the gain performance. The bandwidth is lower than predicted.

The next step is the final high power measurements of the device. In order to ensure that the results are highly accurate, a system self calibration procedure was created using MATLAB. In the first step, the 50Ω attenuators are accurately measured over the full range of measurement frequencies. This data is stored in a reference look-up table. Next the input to the Hittite driver amplifier is swept in input power and frequency. This ensures that for every required output power from the Hittite driver amplifier, the exact input power required to achieve that required driver output power is known. This allows the frequency dependent effects of the Hittite driver amplifier to be removed from the full high power system tests. A circulator is inserted between the Hittite pre-amplifier and the BLF2045 30W amplifier. This protects the Hittite amplifier from any power that could be reflected from a possible mismatch at the input of the BLF2045 30W amplifier.

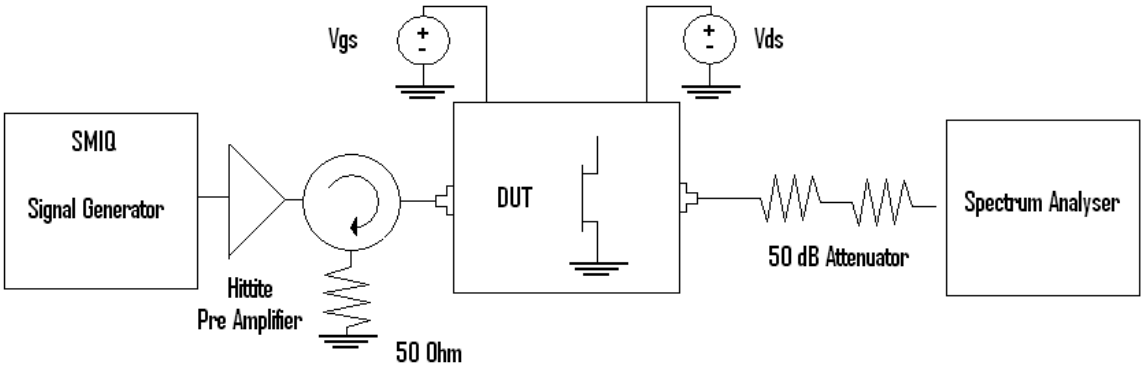

Figure 64 - Figure showing the equipment setup used to measure the high power response of the BLF2045

The entire system is controlled via automated MATLAB code written specifically for the task.

Both the small signal S-parameter and the high power results show a properly working amplifier. Within the design bandwidth the amplifier shows a gain of in excess of 15db. This is significantly higher than the simulated gain.

The results shown in Figure 62 and Figure 63 also indicate the variation in response of the amplifier due to a changing gate bias point. This variation due to effective bias point is also reflected in Figure 65.

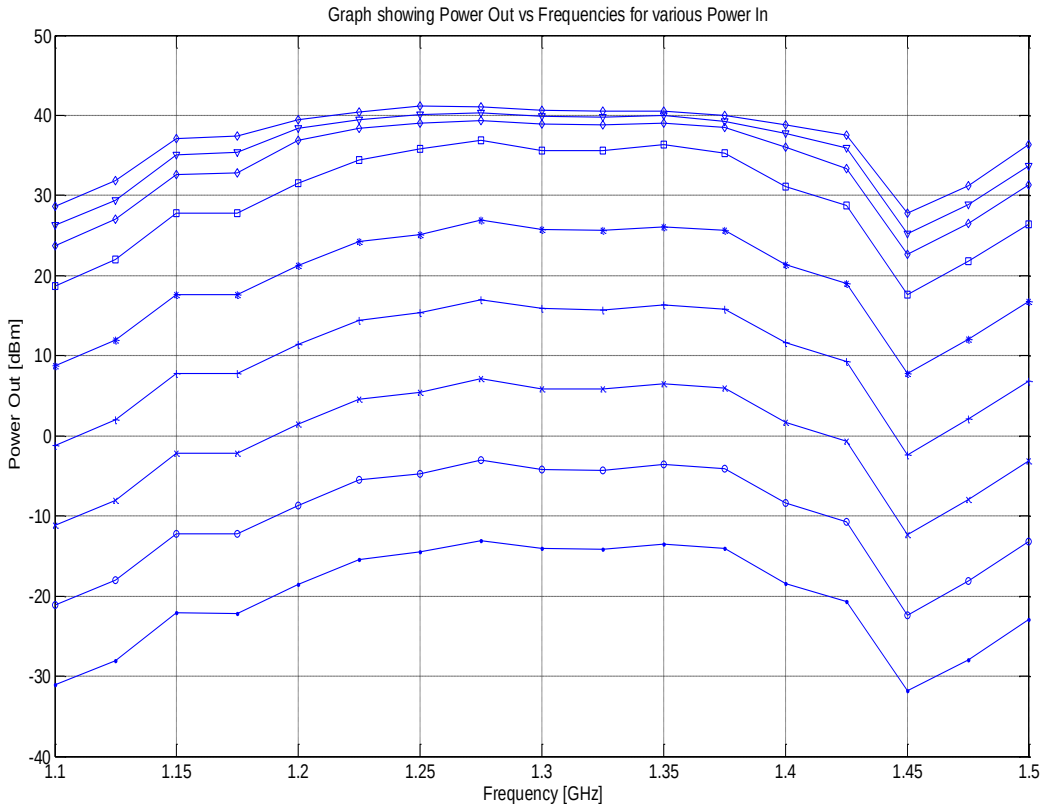

Figure 65 - Figure showing the measured BLF2045 amplifiers Output Power vs. Frequencies for various Input Powers

The results plotted in Figure 66 show the linear behaviour of the amplifier for input powers of up to 20dBm. At input powers higher than 20dBm the BLF2045 amplifier begins to go into compression. The 3dB compression occurs at approximately 40.5dBm. This result equates to a 3dB difference from the desired 30W performance of the device.

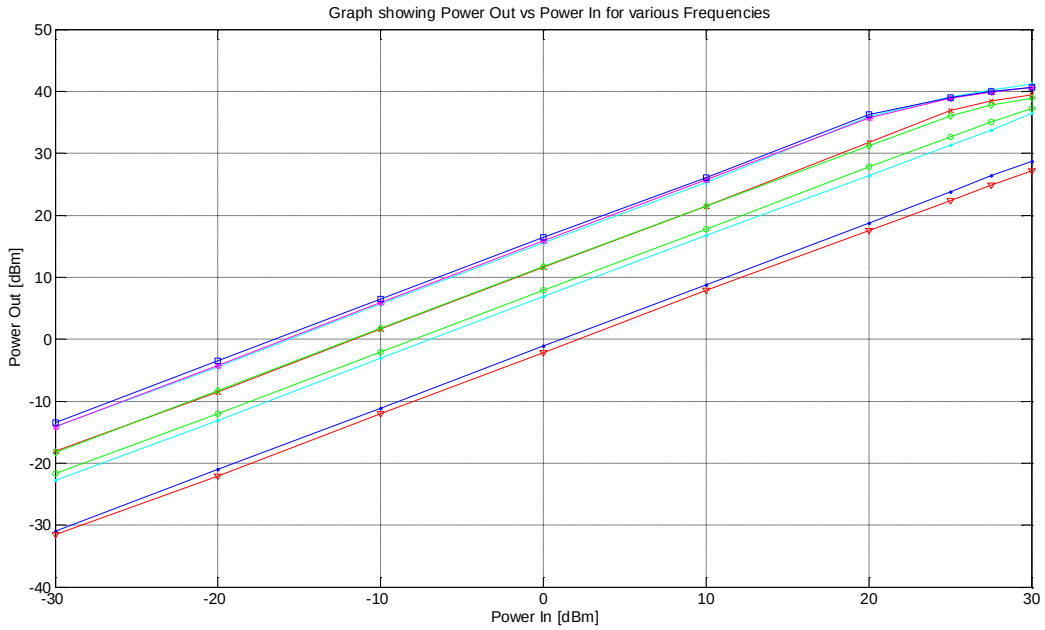

Figure 66 - Figure showing the measured results from the BLF2045 amplifier showing the Output power vs. the Input power for various frequencies

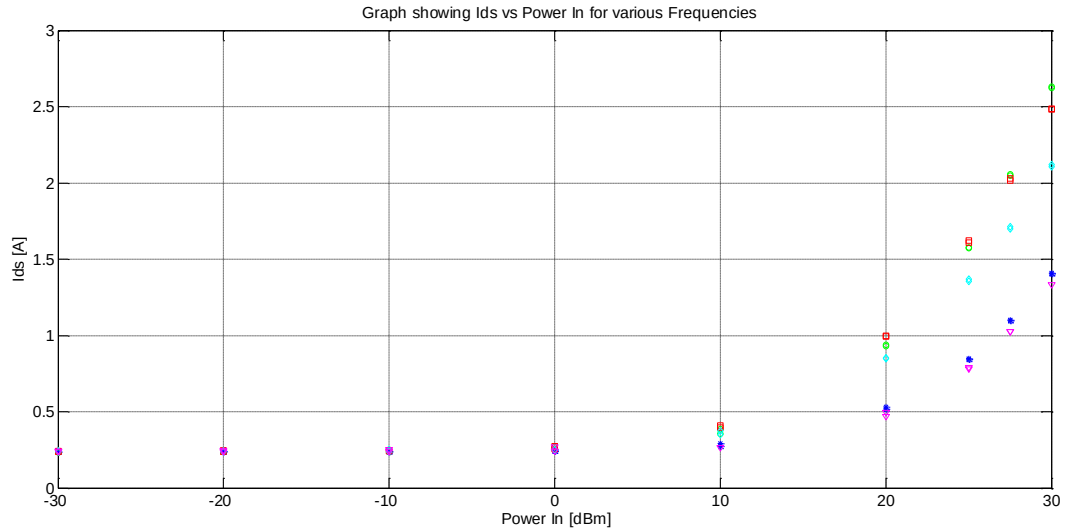

Figure 67 - Figure showing the measured upward and downward ramp results from the BLF2045 amplifier showing the Drain Current (Ids) vs Input Power for various frequencies

The results plotted in
Figure 67 are used to show that the amplifier does not exhibit any memory effects, due to self heating, during operation. During testing, the amplifier is driven at various power levels from very low to full compression and then back to very low levels. At each point the DC I_{DS} is measured. Any memory effects would result in differences between the current, I_{DS}, of the upward and downward ramps.

6.4 Conclusion

As an initial design, the BLF2045 30W amplifier was a success, even though the full 30W output power was not achieved. It serves to highlight the main areas of design sensitivity.
The initial RF I-V curves show that any misplacement of the load line, even if it is very small, can result in lower output power.
Small signal s-parameter measurement proved to also be an issue. This is due to the fact that as an amplifier begins to operate at higher power levels the effective DC bias point is raised. This is due to the effective DC addition of the half wave recification of the input of the class AB amplifier design. This point is beyond the DC safe area of operation of the amplifier and network analyser. It was also noted that the s-parameter measurements were, in fact, taken at the specified DC bias point and thus were not valid at the higher power levels.
The main area that required a redesign is the input and output matching networks. The initial design uses only transmission lines, which vary from narrow to wide, to simulate the short-step-stub transformers of the input and output stages. The issue this design highlights is that the due to the low impedances inherent to the high power amplifiers, the transmission line models are at the edge of their validity.
A redesign would substitute the single wide transmission lines with two narrower transmission line that run perpendicular (open ended shunt transmission lines) in order to create the same physical dimensions while still maintaining the model integrity.
A redesign of the bias network using an EM simulation of the vias would also improve the accuracy of the simulations.

Chapter 7 – BLL1214-35 RADAR Amplifier Design

7.1 Introduction

The aim of this chapter is to investigate the performance of a BLL1214 35W [43] device when used in a power matched RADAR amplifier. The main purpose of this design is to create a baseline for comparison with the BLF2045 commercial amplifier.
As mentioned before, the BLL1214-35 is a pre-matched military specification device and thus there are certain advantages, over the BLF2045 device, when designing power amplifiers. The most relevant advantage is that the internal matching network of the device allows for a simpler, lower risk, design process. However, this simple design has a down side. In the case of the BLL1214-35 the fact that it is pre-matched makes it less flexible for other applications. The BLL1214-35s military design also ensures that its availability is restricted and, in addition, the cost is increased.

The design of an amplifier using a matched device occurs in several stages.

1. Device Characterisation from S-Parameter measurements using the low impedance TRL measurement fixture.
2. Output DC bias circuit design.
3. Output impedance matching network design using the specified load-pull data from the BLL1214-35 data page.
4. Input DC bias circuit design.
5. Input impedance matching using a conjugate match from the measured s-parameters.
6. Final amplifier optimisation for maximum input as well as output power and gain flatness.

This chapter will focus thus on the design and implementation of the DC bias networks, and the design of the input and output matching networks. It was decided, after completion of the BLF2045 30W amplifier, to move away from the short-wide transmission line model to implement the matching networks, and use a construction of narrow long open circuit shunt transmission lines. This ensures the same physical dimensions as required by the Chebyshev Matching Network [42], while still maintaining the AWR Microwave Office® model integrity.
The final section of this chapter will discuss the measurements of the final design as well as its possible use as a pre-amplifier in a high power RADAR system.

7.2 Design

7.2.1 S-Parameter Measurement

The S-Parameter measurements are taken to order to design conjugate match input matching network. These measurements are used instead of the manufactures' specified network parameters, due to the fact that these specified values are for only the Q-point of the device. By performing s-parameter measurements at various bias points gives insight into the response of the device at higher power levels.

In the design of the amplifier the s-parameters of the highest Q-point were chosen, as this would most accurately estimate the response of the device at the higher power levels.

The final s-parameter measurements are used to create accurate high power simulation, as well as allowing for effective optimisations.

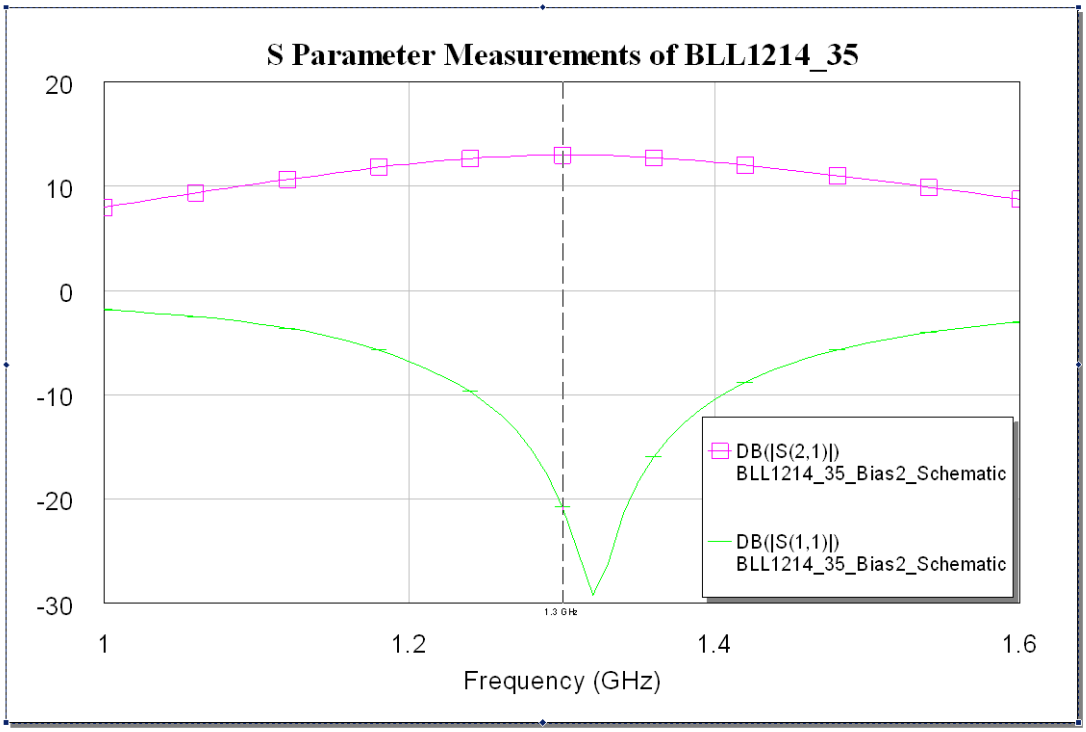

Figure 68 - Graph Showing S-Parameter Measurement of BLL1214-35 gained from Low Impedance TRL Test Fixture

7.2.2 Output DC Bias Network Design

As described in Chapter 6, the purpose of the DC bias network is to provide the output section of the amplifier with the power required to generate the RF output signal. It was decided that, as the functionality of the bias network in the BLL1214-35 amplifier is in essentially the same as the bias network of the BLF2045 amplifier, the same design can be implemented.

The following features were again, as in the BLF2045 design, implemented:

1. A quarter wavelength (λ/4), at 1.6 GHz, length of transmission line connects the drain of the BLL1214-35 to the external DC power source.
2. Several ceramic capacitors were placed at λ/4 from the drain in order to suppress any possible RF components from leaking back to the DC power supply.
3. A snubber circuit was also place λ/4 away from the drain to assist in the suppression of RF signals.
4. The width of the transmission line was made wide as to reduce the series impedance of the bias network so that losses within the network can be minimised.

7.2.3 Output Impedance Matching Network Design

The output impedance matching network was designed using the load-pull data specified in the manufacturer's data page. As the BLL1214-35 is pre-matched, one cannot use measured s-parameters for parameter extraction. The pre-matching network prevents any analytical method of circuit parameter extraction.

Table 7 - Table of Manufacturers Specified Input and Output Impedances of BLL1214-35

Frequency [GHz]	Zs (Ω)	Zl (Ω)
1.2	6.48 – j3.9	1.95 + j3.27
1.25	3.88 – j3.2	1.90 + j2.57
1.3	3.28 – j2.4	2.01 + j2.27
1.35	2.55 – j1.48	2.20 + j2.26
1.4	1.69 – j0.51	1.72 + j2.35

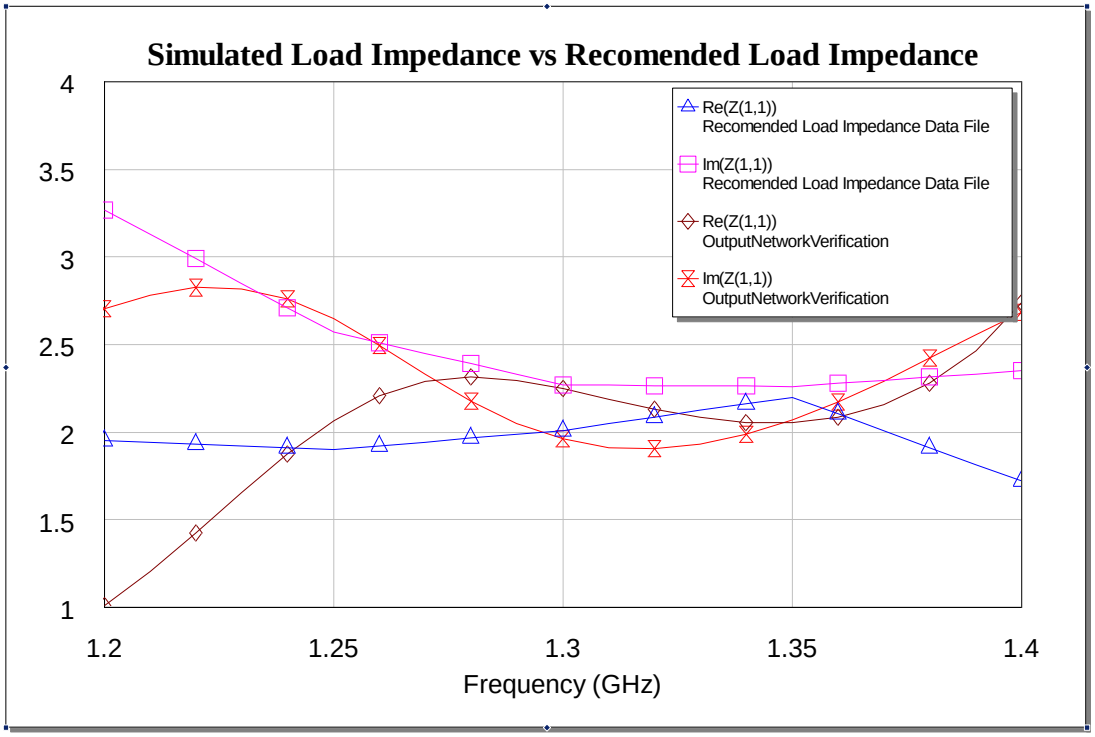

Figure 69 - Figure Showing Simulated Load Impedance vs. Recommended Load Impedance

7.2.4 Input DC Bias Network Design

As, similar to chapter 6, the input DC bias network follows the same design procedure as the output DC bias network. The input bias network biases the BLL1214-35 in a class AB condition. As in the design of the BLF2045 amplifier the following design criteria were considered:

1. A quarter wavelength (λ/4), at 1.6 GHz, length of transmission line connects the drain of the BLL1214-35 to the external DC power source.
2. Several ceramic capacitors were placed at λ/4 from the drain in order to suppress any possible RF components from leaking back to the DC power supply.
3. A snubber circuit was also place λ/4 away from the drain to assist in the suppression of RF signals.
4. The width of the transmission line in the input bias network was chosen to be 2mm as the series impedance was not an issue as the current through the bias network was very low.
5. A resistor was placed in series with the bias network in order to help stabilise the amplifier.

7.2.5 Input Impedance Matching Network Design

The aim of this section is to design and implement a conjugate match input network for the BLL1214-35 amplifier. This is to ensure that the maximum power is transferred into the amplifier.

In Chapter 6 the design makes use of the simulated s-parameters extracted from the equivalent circuit. This method provides insight into the structure of the device and thus allows the designer to tailor the performance of the device to specific tasks, which is not possible in pre-matched devices which have specific working parameters. In the design of the BLL1214-35 35W amplifier design, that method is not possible as the pre-matching network prevents the insight into the inner workings of the device. In this case, one could use the manufacturer's specified input impedances. It was in decided instead, though, to use the measured s-parameters to design the conjugate matching network. This approach was chosen as the low impedance TRL test fixture allowed for more accurate measurements at various bias points. It was decided the s-parameter measurements from the highest measured bias point should be used, as this would give the most accurate prediction of the high power behaviour of the device.

A Chebyshev Short Step Impedance Transformer [42] was again used to create the impedance transformer. A series DC de-coupling capacitor was again implemented. In order to help with the stability of the circuit, a shunt circuit, comprising of a capacitor and resistor in series, was implemented directly at the gate of the device. The full network was then optimised for input match as well as overall gain and stability.

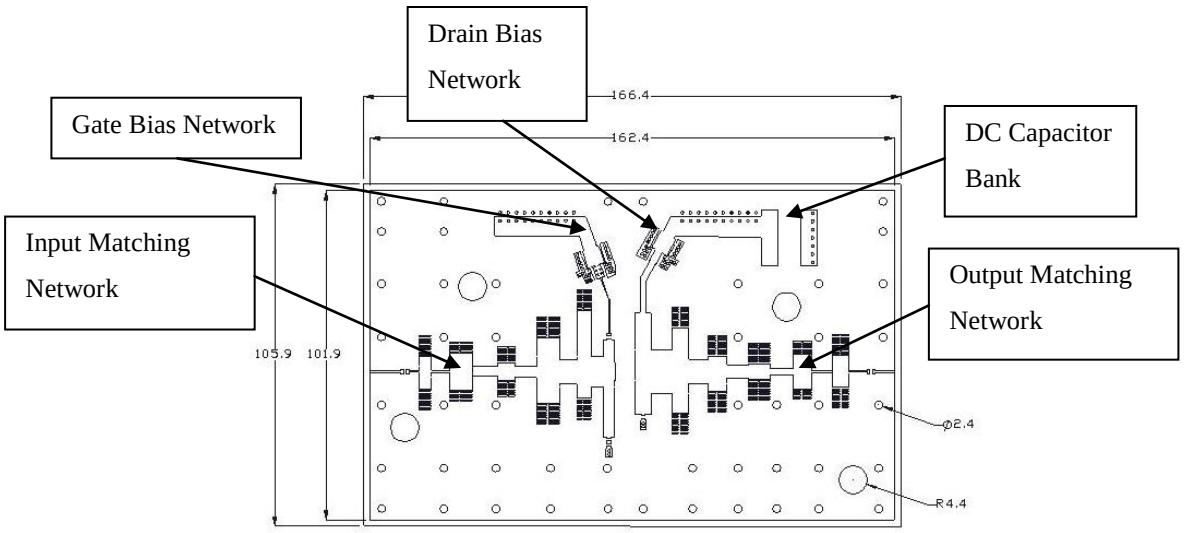

Figure 70 - Figure showing the final layout of the BLL1214-35 amplifier including both the input and output matching networks

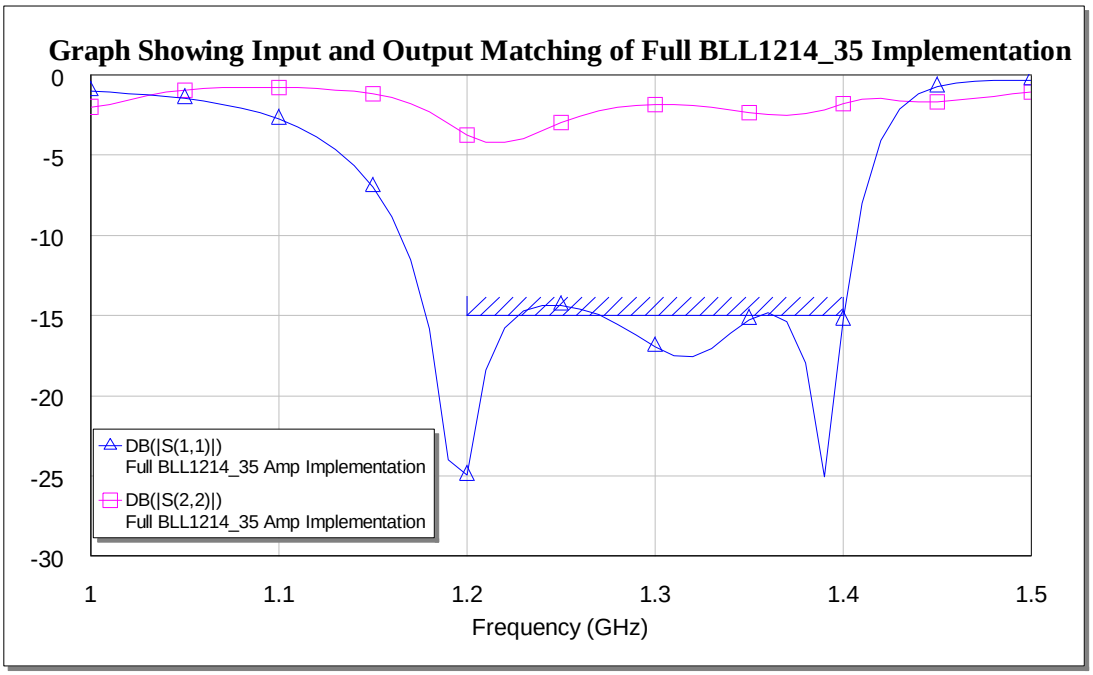

Figure 71 - Figure Showing Simulated Input and Output Matching of BLL1214-35 35W Amplifier

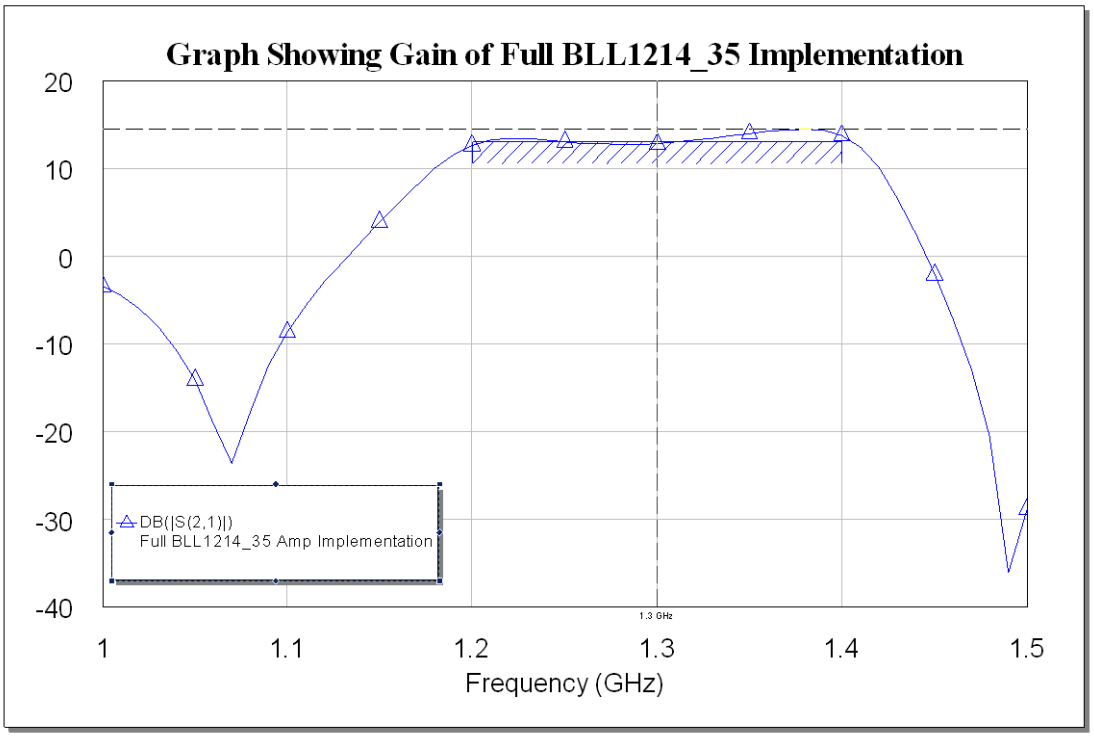

Figure 72 – Figure showing Simulated Gain (S21) of BLL1214-35 35W Amplifier

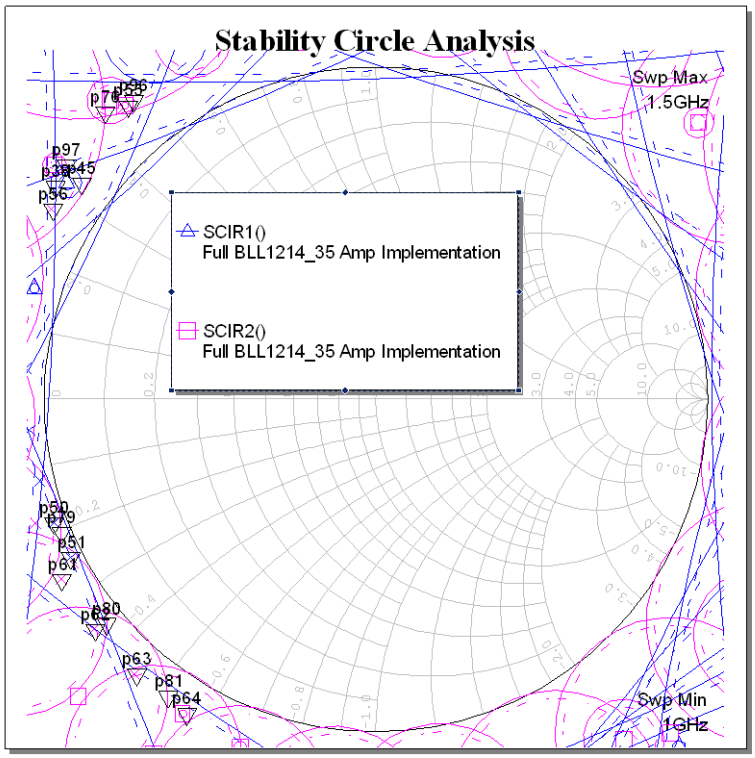

Figure 73 – Figure showing Simulated Stability Circle Analysis of BLL1214-35 35W Amplifier

7.3 Measurement Setup

The measurement setups described in Chapter 6.3.1 was repeated in this section. Several steps were taken to ensure that the measurement of the BLL1214-35 35W amplifier is accurate. The first of these steps is to ensure that the amplifier remains unconditionally stable over all frequencies. This setup can be seen in Figure 61. This is done by first terminating the input of the amplifier with a long section of cable, which in turn is terminated with a 50Ω load. This provides the device with conditions that are most likely to cause oscillations. Next, the output of the amplifier is connected to a spectrum analyser (SA) via a short section of cable and two high power attenuators, together achieving 50 dB of attenuation. The DC gate and drain voltage are swept from 0 V to the maximum voltages within the SOA (Safe Operating Area). At each gate and drain point, the peak RF signal is measured with the SA. The SA is set so that the noise level is below -50dB. Thus if a peak is measured higher than the noise level, one can deduce that the amplifier is oscillating. The attenuators are used to ensure protection of the costly SA.

The next step is to measure the active S-parameters of the amplifier. This provides insight into the performance of the amplifier under low power, small signal conditions. This indicates whether the amplifier is functioning, although in the case of high power amplifiers this does indicate the high power performance. This is due to the fact that as the power levels increase, the effective bias point is raised beyond the DC safe operating area.

The next step is the final high power measurements of the device. In order to ensure that the results are highly accurate, a system self calibration procedure was created using MATLAB. The method used in Chapter 6 is again employed. This setup can be seen in Figure 64. In the first step, the 50Ω attenuators are accurately measured over the full range of measurement frequencies. This data is stored in a reference look-up table. Next the input to the Hittite driver amplifier is swept in respect to both to input power and frequency. This ensures that for every required output power from the Hittite driver amplifier, the exact input power required to achieve that required driver output power is known. This allows the frequency dependent effects of the Hittite driver amplifier to be removed from the full high power system tests. A circulator is inserted between the Hittite pre-amplifier and the BLL1214-35 amplifier. This protects the Hittite amplifier from any power that could be reflected from a possible mismatch at the input of the BLL1214-35 amplifier. The output power is measured using a digital power meter. The RF input signal from the SMIQ signal generator to the Hittite pre-amplifier is pulsed using a 10% duty cycle square wave at 1 kHz. This signal, to control the pulse frequency and duration, is supplied by a wave form generator. This signal is also used as an input into the power meter in order to synchronise the pulse received from the output of the BLL1214-35 amplifier, with the trigger of the power meter. The entire system is then controlled via MATLAB code written for the task.

7.4 Results

The measured small signal s-parameters show a reasonable input match. A centre frequency match of between -12dB and -16dB was obtained. The match over the entire bandwidth, although, was not as effective. An overall match of between -6dB and -8dB was obtained. The input match was tested at 4.6V, 4.64V, 4.7V, 4.75V, 4.8V and 4.85V. Figure 74 shows how the input match varies as function of DC bias point.

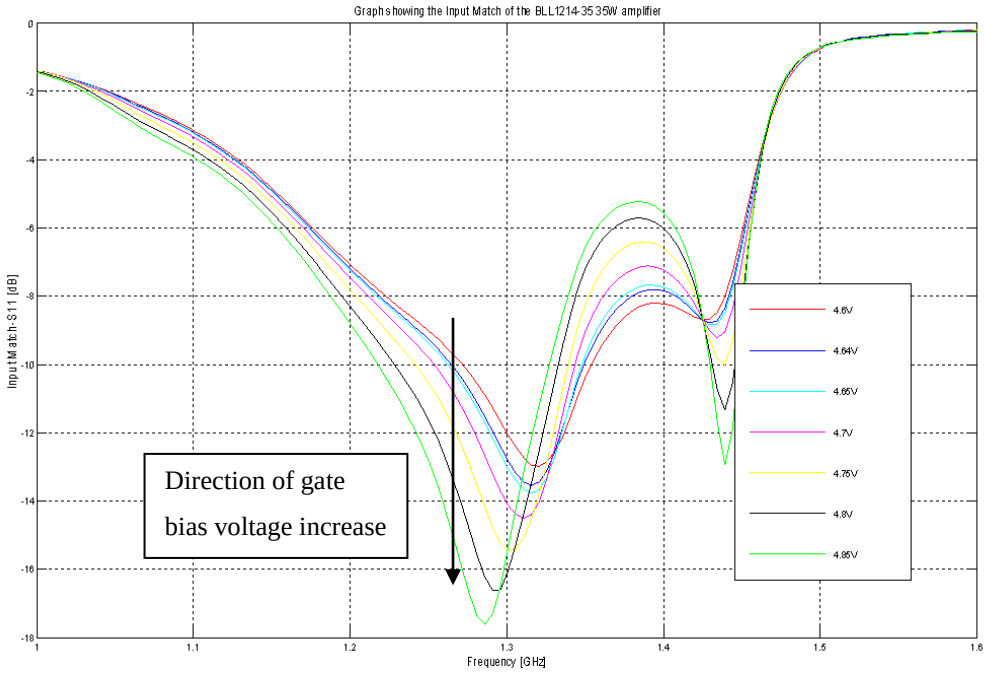

Figure 74 - Figure showing the Input Match-S11 of the BLL1214-35 35W amplifier for various DC bias points

The small signal gain, Figure 75, also showed an acceptable centre band performance of over 13dB but the gain over the entire bandwidth was again degraded. The effect that the different DC gate bias voltage has on the overall S-parameters can be again seen in the gain of the BLL1214-35 amplifier.

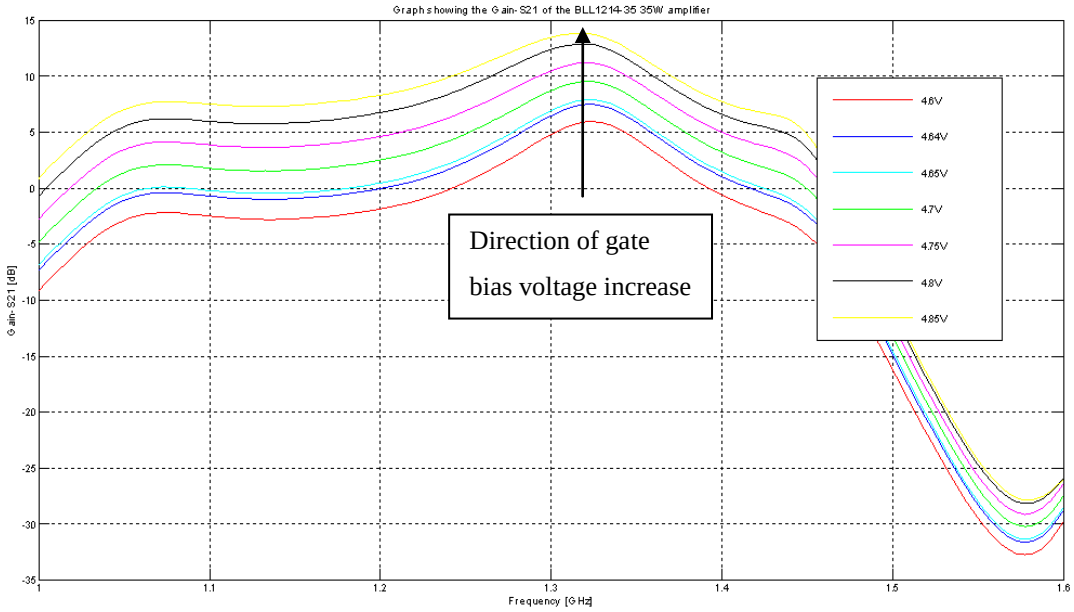

Figure 75 - Figure showing the Gain-S21 of the BLL1214-35 35W amplifier for various DC bias points

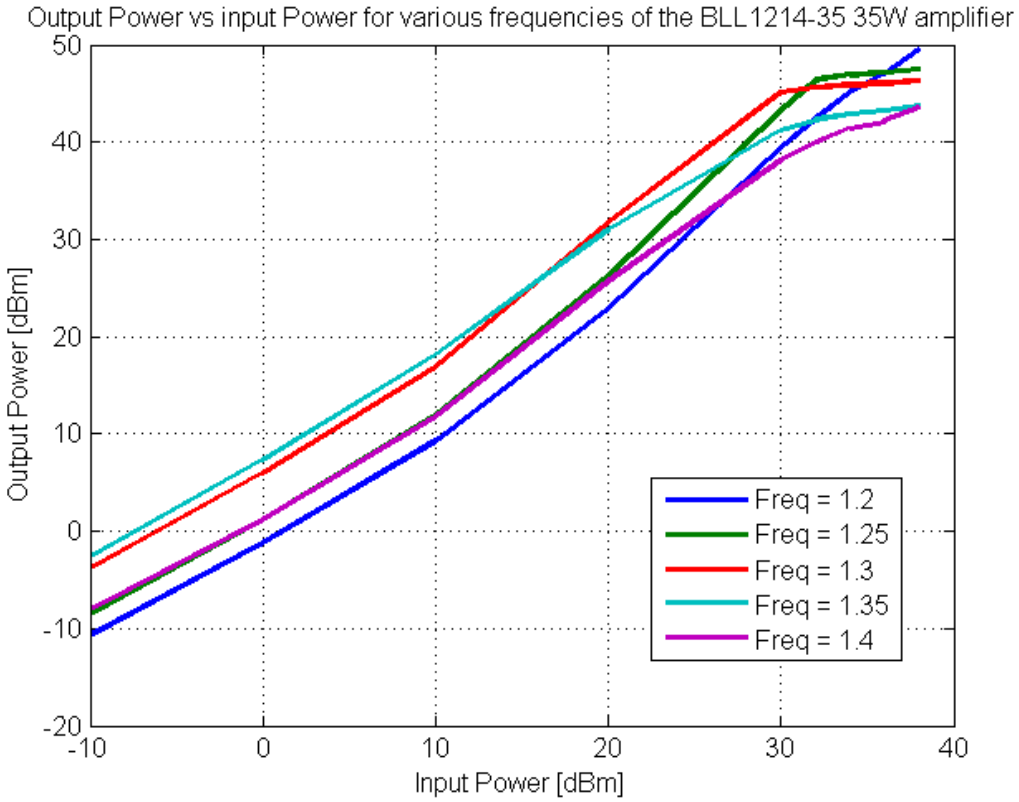

Figure 76 - Figure showing the output power of the BLL1214-35 35W amplifier with respect to the input power

The next stage of the amplifiers evaluation is the high power measurements.

Figure 76 shows good linearity of the BLL1214-35 amplifier over the entire frequency band. Compression can be seen when an input power above 30dbm is applied.

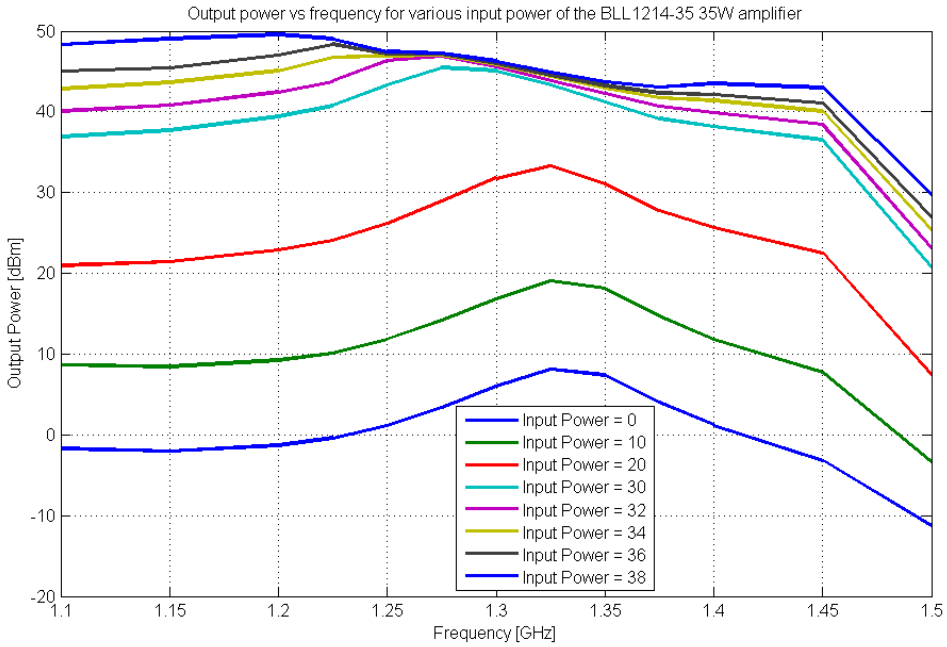

Figure 77 - Figure showing the Output power of the BLL1214-35 35W amplifier with respect to the frequency

Figure 77 shows the gain flatness of the amplifier over the band. At the higher input powers, the amplifier begins to show a flatter gain profile as a result of compression.

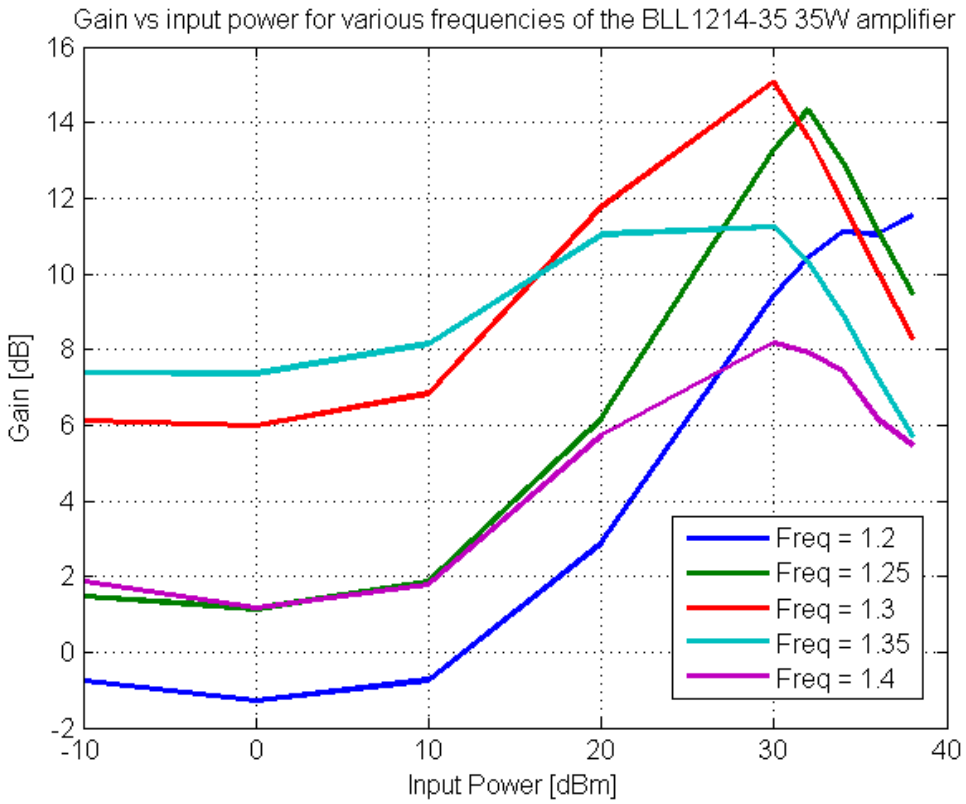

Figure 78 - Figure showing the gain of the BLL1214-35 35W amplifier with respect to the input power

Figure 78 shows an important result. It shows how the amplifier begins to operate in line with the simulated results shown in Figure 72. This is due to the effective bias point increase caused by the high input power below compression.

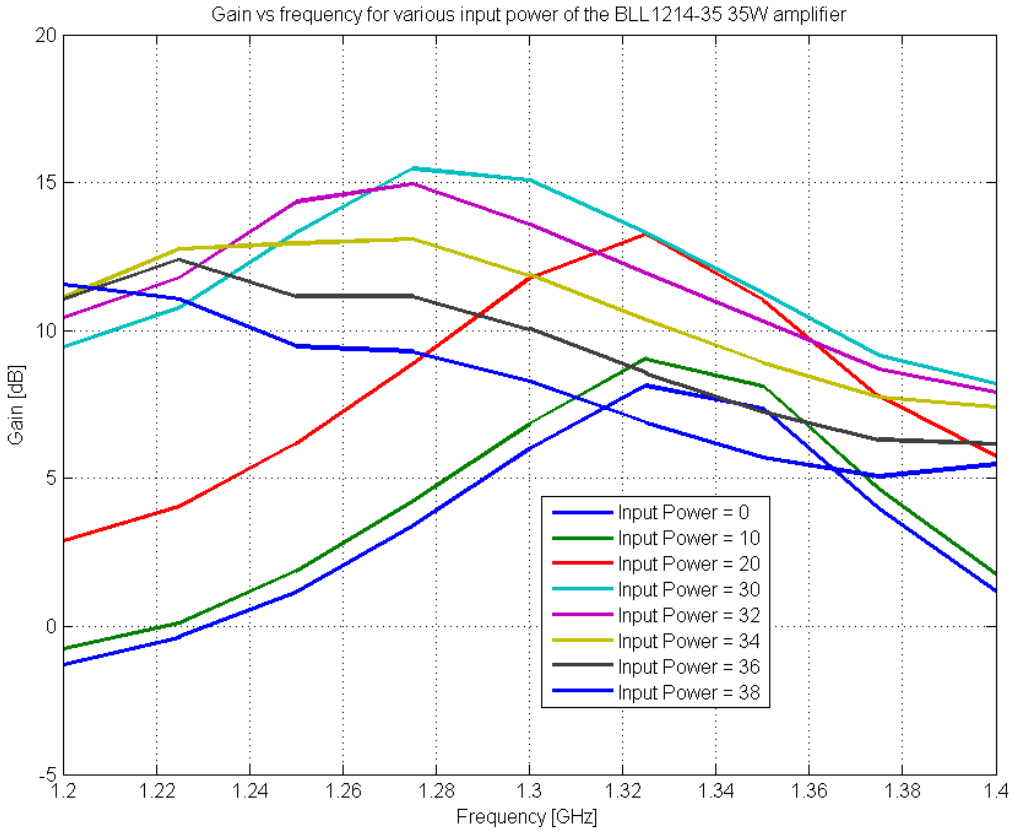

Figure 79 - Figure showing the gain of the BLL1214-35 35W amplifier with respect to frequency

Figure 79 shows the gain performance of the amplifier with respect to frequency. The gain is shown to improve as the input power increases up until the amplifier begins to enter compression.

7.4.1 Recommendations

The shift from using short, wide transmission used in the BLF2045 30W amplifier simulation models to the use of narrow shunt open circuit terminated transmission lines used in the BLL1214-35 35W amplifier resulted in a much improved final performance of the amplifier. This applies to the small signal s-parameters as well as the maximum output power and linearity. The trend should be continued to all the sections impedance matching networks, as only the very wide transmission lines, in the BLL1214-35 amplifier, were replaced. This should again improve the performance of the amplifier.

7.5 Conclusion

The design of the BLL1214-35 35W amplifier, as a comparative amplifier design, was a success. The main improvement was the used of shunt open circuit terminated transmission lines in the simulation of the matching networks. A pulsed peak output power of 49.55 dBm was achieved, which is higher than the specified power of the device. This was not achieved throughout the required band and the peak output power and gain fluctuated greatly with respect to both frequency and input power. The variation in the performance of the amplifier as a function of input power again indicates that the correct choice of the bias point when measuring the s-parameters of the device is vital. The frequency dependant variations indicate that the models used in the simulations, although improved from the design in chapter 6, still have room for improvement.

The use of the pulsed power supply also proved to be successful as there was no discernable droop in the output power.

Chapter 8 – BLL1214-250 RADAR Amplifier Design

8.1 Introduction

The aim of this chapter is to investigate the performance of a BLL1214-250 250W device [44] when used in a power matched RADAR amplifier. The main purpose of this design is to create a high power, output stage L-Band RADAR power amplifier. The BLL1214-250 device is a pre-matched, military specification LDMOS device. The design principle in this process follows the same lines as the design process as in Chapter 7. The design process makes use of lessons learned in the design of the BLL1214-35 35W amplifier. The most important of these is the insight into the accurate modelling of the input and output impedance matching networks.

In Chapter 6, the simulation models make use of short, wide transmission lines within the model to design the matching networks. This was not as successful as hoped, as the dimensions of the transmission lines, required to implement the low impedances, resulted in the breakdown of the simulation models. Chapter 7 improved on this by replacing the widest of the required transmission lines with pairs of shunt, open circuit, narrow transmission lines. This resulted in a substantial improvement in the operation of the amplifier. This chapter will use this insight by implementing all of the matching network segments with this method.

The BLL1214-250, like the BLL1214-35, is a pre-matched device, and like the BLL1214-35, it has the advantage of having a less risky design process, and similarly has the disadvantage of being restricted in its uses and availability. The military applications of the device also ensure that the cost of the device is increased.

The design of an amplifier using a matched device occurs in several stages.

1. Device Characterisation from S-Parameter measurements using the low impedance TRL measurement fixture.
2. Output DC bias circuit design.
3. Output impedance matching network design using the specified load-pull data from the BLL1214-250 data page.
4. Input DC bias circuit design.
5. Input impedance matching using a conjugate match from the measured s-parameters.
6. Final amplifier optimisation for maximum input as well as output power and gain flatness.

This chapter will focus thus on the design and implementation of the DC bias networks, and the design of the input and output matching networks.
The final section of this chapter will discuss the measurements of the final design as well as its possible use as a final output stage amplifier in a high power RADAR system.

8.2 Design

8.2.1 S-Parameter Measurement

The S-Parameter measurements of the BLL1214-250 device followed the same method as was used in Chapter 6 and Chapter 7.
The S-Parameter measurements are taken to order to design conjugate match input matching network. These measurements are used instead of the manufactures specified network parameters due to the fact that these specified values are for only the Q-point of the device. By performing s-parameter measurements at various bias points gives insight into the response of the device at higher power levels.
In the design of the amplifier the s-parameters of the highest Q-point were chosen, as this would most accurately estimate the response of the device at the higher power levels.

8.2.2 Output DC Bias Network Design

As described in Chapter 6 and Chapter 7, the purpose of the DC bias network is to provide the output section of the amplifier with the power required to generate the RF output signal. It was decided that, as the functionality of the bias network in the BLL1214-250 amplifier is essentially the same as the bias network of the BLF2045 amplifier and the BLL1214-35 amplifier, the same design can be implemented.

The following features were again, as in the BLF2045 and BLL1214-35 designs, implemented:

1. A quarter wavelength (λ/4), at 1.6 GHz, length of transmission line connects the drain of the BLL1214-250 to the external DC power source.
2. Several ceramic capacitors were placed λ/4 from the drain in order to suppress any possible RF components from leaking back to the DC power supply.
3. A snubber circuit was also place λ/4 away from the drain to assist in the suppression of RF signals.
4. The width of the transmission line was made wide as to reduce the series impedance of the bias network so that losses within the network can be minimised.

8.2.3 Output Impedance Matching Network Design

The output impedance matching network was designed using the load-pull data specified in the manufacturer's data page. As the BLL1214-250 is pre-matched, one cannot use measured s-parameters for circuit parameter extraction. The pre-matching network prevents any analytical method of circuit parameter extraction.

Table 8 -Table of Manufacturers Specified Input and Output Impedances of BLL1214-250

Frequency [GHz]	Zs (Ω)	Zl (Ω)
1.2	1.3 – j2.8	1.1 - j0.9
1.25	1.9 – j2.9	1 - j0.5
1.3	4.6 – j2.9	0.8 – j0.2
1.35	5.7 – j0.3	0.7 – j0.3
1.4	2.7 – j1.8	0.6 + j0.4

One should notice the differences in output impedances of the BLL1214-35 device shown in Table 7, and the impedances of the BLL1214-250 device shown in Table 8. This illustrates how that, even with internal pre-matching networks within the devices, the impedances presented to the external circuits are extremely low.

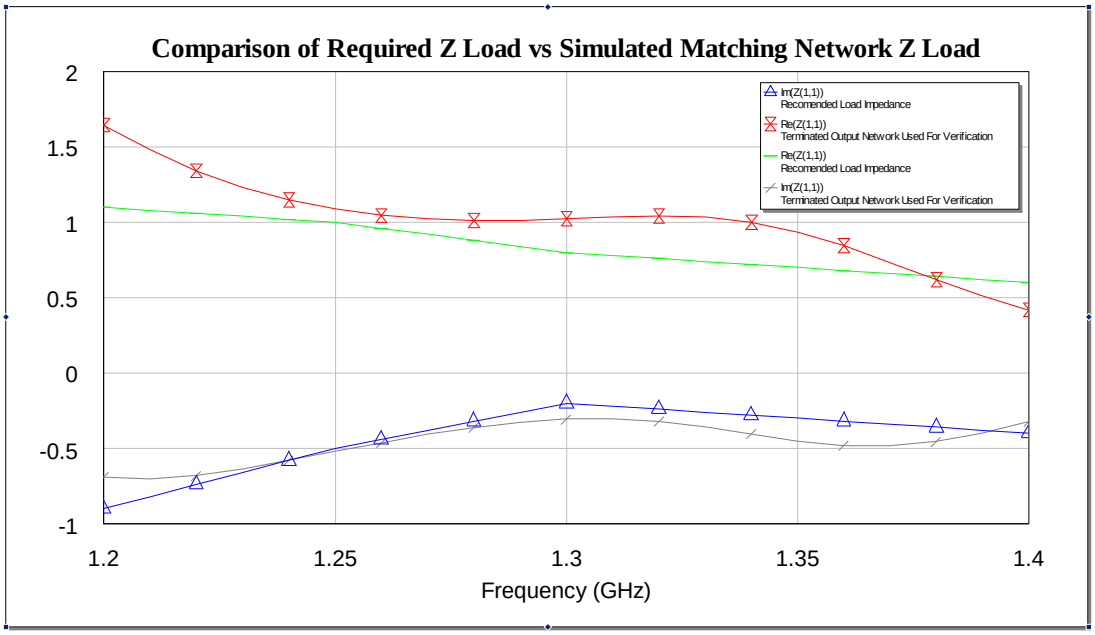

Figure 80 - Graph Showing Comparison between Required Drain Impedance and Simulated Matching Network Impedance

Figure 80 shows a greatly improved match between the data page specified required load, and the simulated load presented by the output matching network. This is a result of the improved AWR Microwave modelling methods gained from the implementation experience gained in chapters 6 and 7.

8.2.4 Input DC Bias Network Design

As in, Chapter 6 and Chapter 7, the input DC bias network follows the same design procedure as the output DC bias network.

The aim of the input bias network of the BLL1214-250 is to bias the device in a class AB condition. As in the design of the BLF2045 and BLL1214-35 amplifiers the following design criteria were considered:

1. A λ/4, at 1.6 GHz, length of transmission line connects the drain of the BLL1214-250 to the external DC power source.
2. Several ceramic capacitors were placed at λ/4 from the drain in order to suppress any possible RF components from leaking back to the DC power supply.
3. A snubber circuit was also place λ/4 away from the drain to assist in the suppression of RF signals.
4. The width of the transmission line in the input bias network was chosen to be 2mm as the series impedance was not an issue as the current through the bias network was very low.
5. A resistor was placed in series with the bias network in order to help stabilise the amplifier.

8.2.5 Input Impedance Matching Network Design

The aim of this section is to design and implement a conjugate match input network for the BLL1214-250 250W amplifier. This is to ensure that the maximum power is transferred into the amplifier.

In Chapter 6, the design makes use of the simulated s-parameter extracted from the equivalent circuit. In this design, as in Chapter 7, that method is not possible as the pre-matching network prevents the insight into the inner workings of the device. In this case, one could use the manufacturer's specified input impedances. It was decided instead, though, to use the measured s-parameters to design the conjugate matching network.

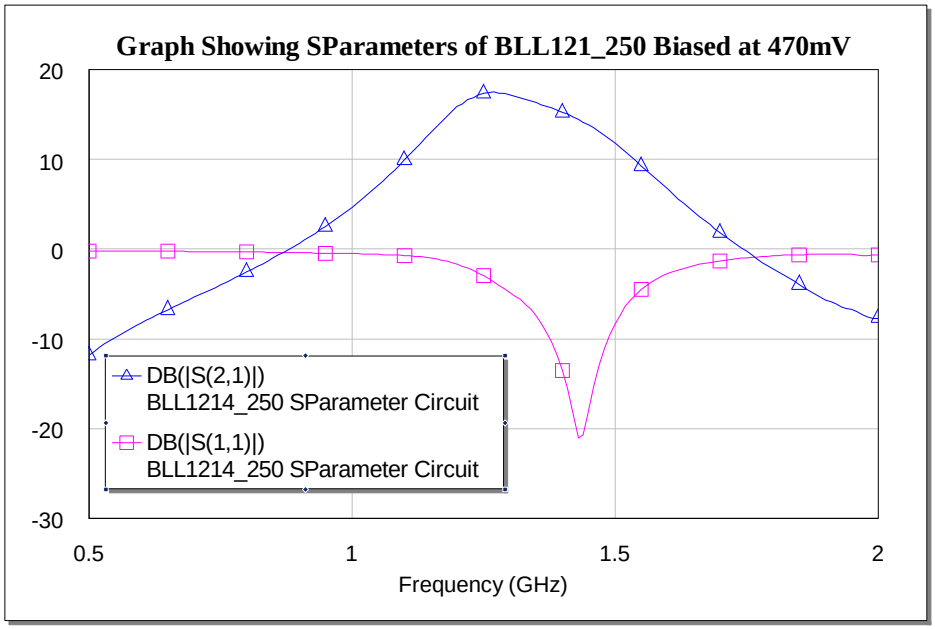

Figure 81 - Graph Showing S-Parameter Measurement of BLL1214-250 gained from Low Impedance TRL Test Fixture

This approach was chosen as the low impedance TRL test fixture allowed for more accurate measurements at various bias points. It was decided the s-parameter measurements from the highest measured bias point should be used, as this would give the most accurate prediction of the high power behaviour of the device.

A Chebyshev Short Step Impedance Transformer [42] was again used to create the impedance transformer. A series DC de-coupling capacitor was again implemented. In order to help with the stability of the circuit, a shunt circuit, comprising of a capacitor and resistor in series, was implemented directly at the gate of the device. The full network was then optimised for input match as well as overall gain and stability.

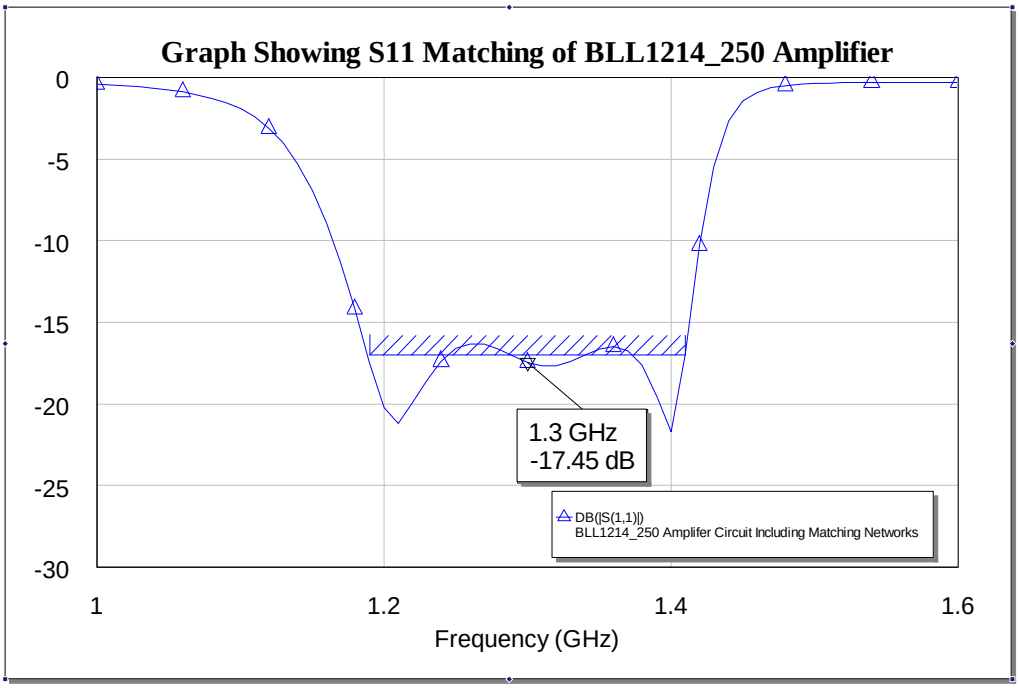

Figure 82 - Graph showing Simulated Impedance Match of BLL1214-250 Amplifier

Figure 82 shows a good simulated input match, S_{11}, of the BLL1214-250 amplifier.
Figure 83 shows also show good simulated results. The gain, S_{21}, is above 14dB across the 1.2GHz to 1.4GHz band.

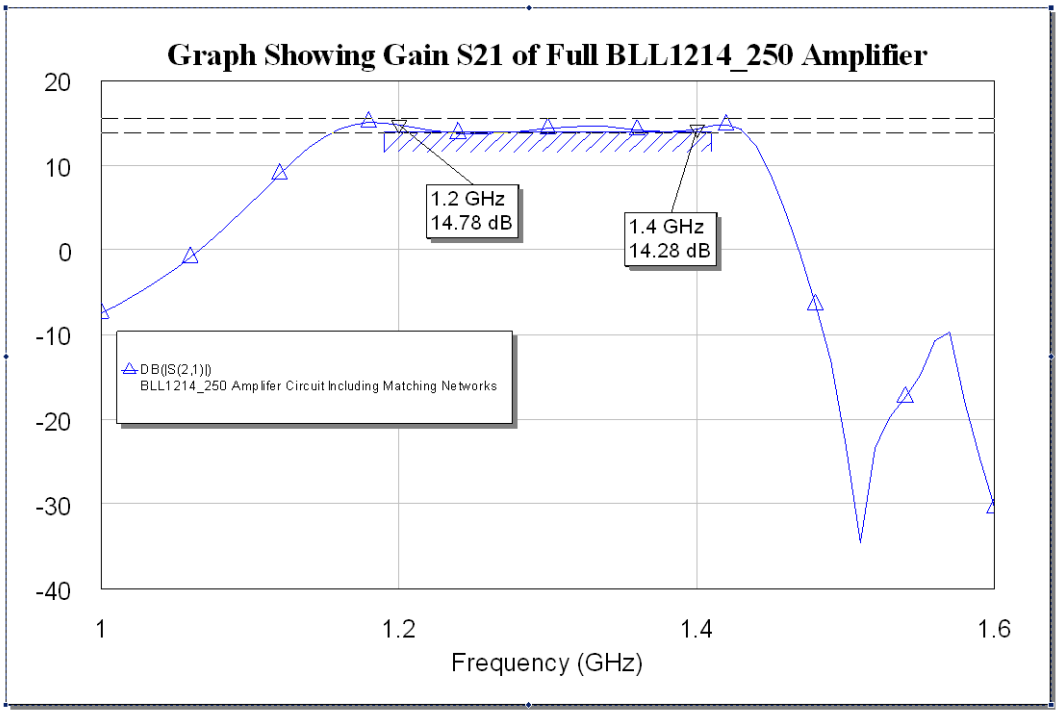

Figure 83 - Graph showing Simulated S_{21} Gain of BLL1214-250 Amplifier

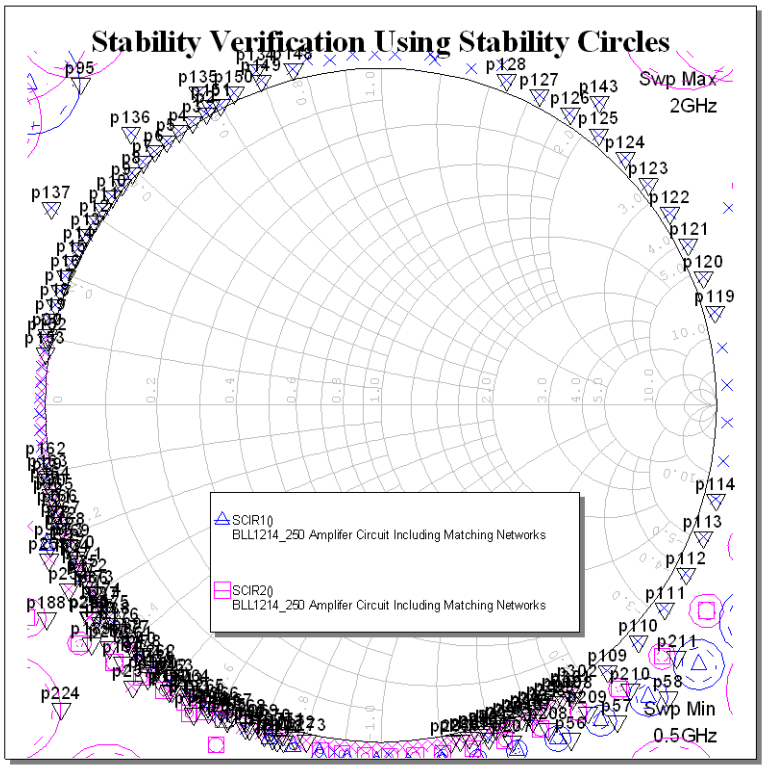

Figure 84 - Simulated Input and Output Stability Circles Simulated from 0.5GHz to 3GHz

Figure 84 shows the results of a stability circle analysis and that the BLL1214-250 amplifier exhibits unconditional stability.

Drain Capacitor Bank

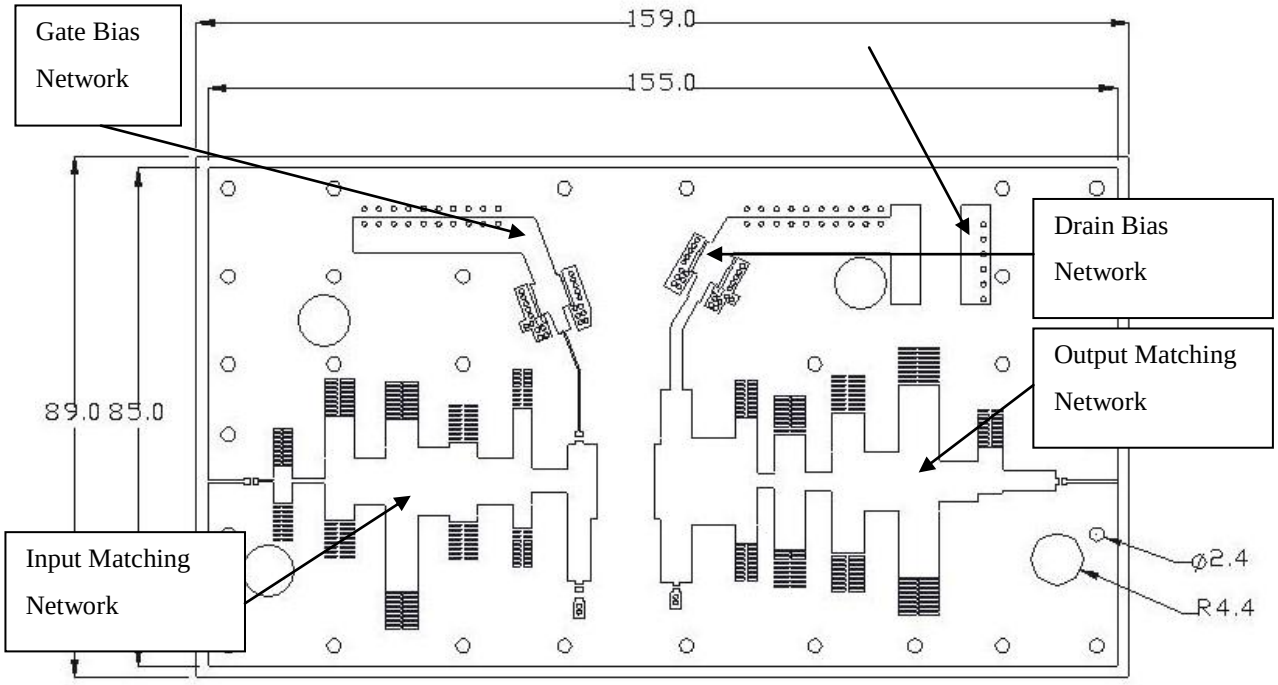

Figure 85 - Figure showing the layout of the BLL1214-250 250W amplifier including the input and output DC bias networks

8.3 Measurement Setup

The measurement setup described in Chapters 6.3.1 and in 7.3 was repeated in this section. Several steps were taken to ensure that the measurement of the BLL1214-250 250W amplifier is measured accurately. The setup can be seen in Figure 61. The first of these steps is to ensure that the amplifier remains unconditionally stable over all frequencies. This is done by terminating the input of the amplifier with a long section of cable, which in turn is terminated with a 50Ω load. The output of the amplifier is connected to a spectrum analyser (SA) via a short section of cable and two high power attenuators, together achieving 50 dB of attenuation. The DC gate and drain voltage are swept from 0 V to the maximum voltages within the SOA (Safe Operating Area). At each gate and drain point, the peak RF signal is measured with the SA. The SA is set so that the noise level is below -50dB. Thus if a peak is measured higher than the noise level, one can deduce that the amplifier is oscillating. The attenuators are used to ensure that protection of the costly SA.

The next step is to measure the active s-parameters of the amplifier. This gives one insight in to the performance of the amplifier under low power small signal conditions. This indicates whether the amplifier is functioning, although as in the case of all high power amplifiers - this does indicate the high power performance, as the power levels increase, the effective bias point is raised beyond the DC safe operating area.

The next step is the final high power measurements of the device. In order to ensure that the results are highly accurate, a system self calibration procedure was created using MATLAB. The method used in Chapter 6 and Chapter 7 is again employed, and can be seen in Figure 64.

The final measurement is to establish the high power input match of the amplifier. This measurement allows a scalar measurement of the S11 of the BLL1214-250 250W amplifier. This measurement setup is shown in Figure 86 and Figure 87. In order to do this a directional coupler is inserted between the circulator at the output of the Hittite Pre-Amplifier, and the input of the BLL1214-250 250W amplifier. This setup couples -10dB of the signal reflected back by the amplifier down towards the power meter.

For example, an amplifier with an input match of -15dB and an input power of 40dBm, the directional coupler would couple 15dBm down towards the power meter. In order to protect the power meter, an additional 20 dB attenuator was place in front of the power meter. This would result in -5 dBm being measured by the power meter.

Thus:

$$\square 11 = \square\square\square\square\square\square\square\square\square\square\square\square\square\square + 20\square\square + 10\square\square - \square\square\square\square\square\square\square\square\square\square\square$$

46

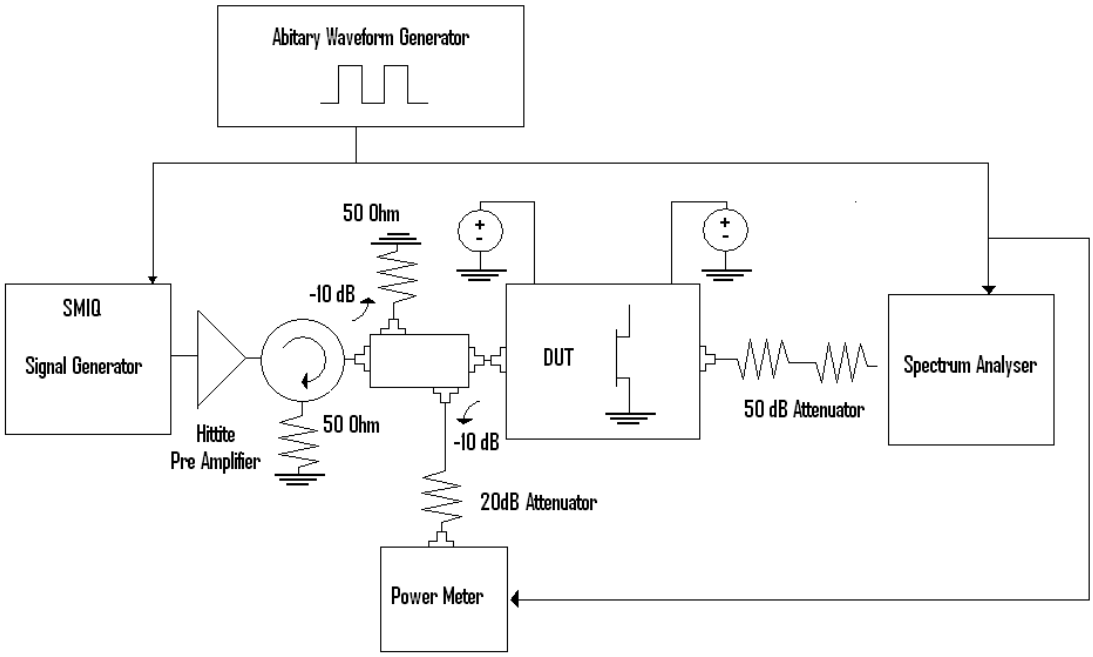

Figure 86 - Figure showing the high power input match measurement setup

In order to ensure that the amplifier's input power is calibrated, the method used for the initial power measurement calibration is repeated. The only difference being that the directional coupler is inserted. Once again MATLAB code is used to control each stage of the calibration and measurement sections. As a further check of the accuracy of the measured output power, the spectrum analyser was again attached to the output of the amplifier and the readings were compared to the original measurements.

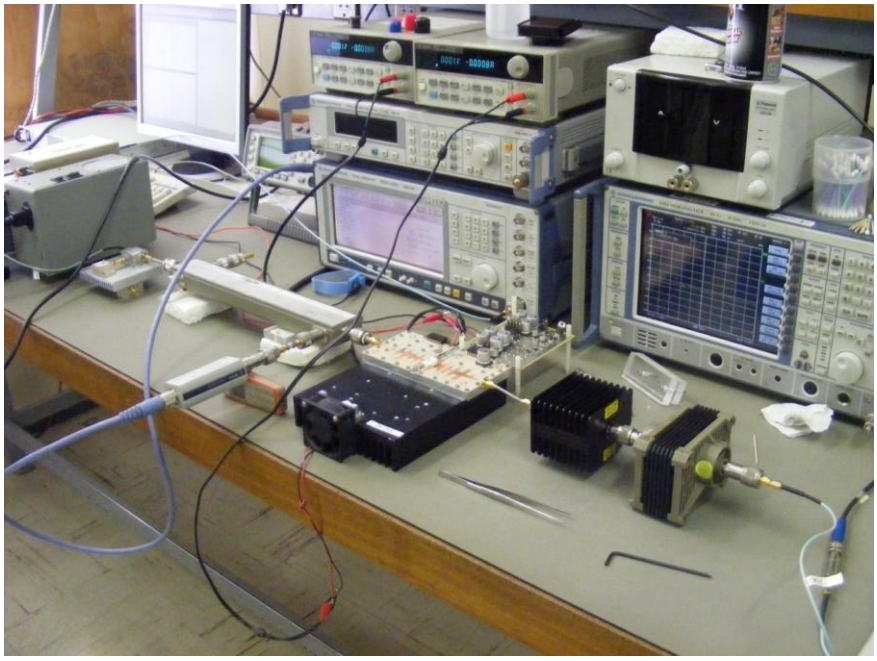

Figure 87 - Figure showing implementation of high power input match and output power measurement setup

8.4 Results

The initial S-Parameter measurements, Figure 88, showed an improvement in the designs implemented in Chapter 6, and Chapter 7. Although the desired -12dB match across the band was not achieved, a match of less than -5dB was obtained, with a match of less that -10dB was obtained for more than 65% of the band depending on the bias point.

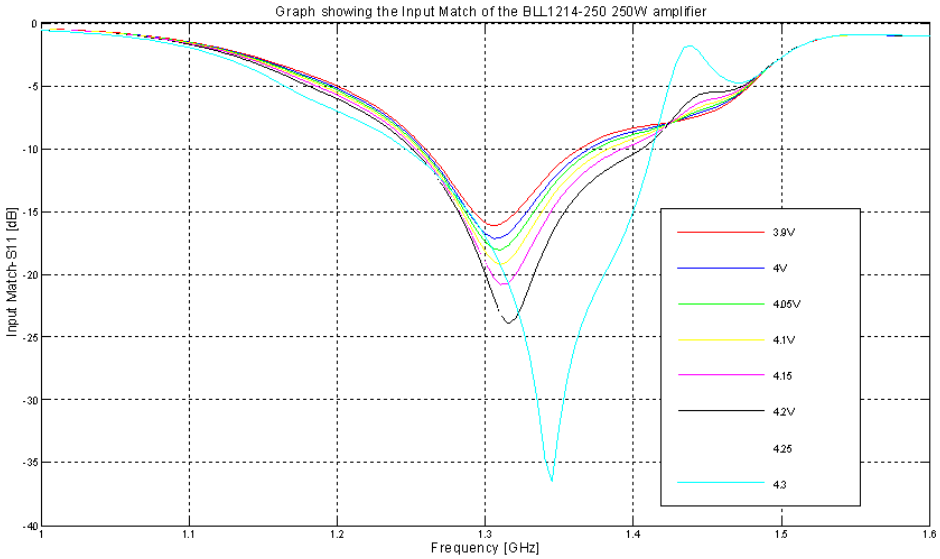

Figure 88 - Figure showing the initial small signal S_{11} measurement of the BLL1214-250 250W amplifier

The initial gain (S_{21}) measurements, Figure 89, showed a less encouraging result. A small signal gain of above 5dB was obtained across the band, with a maximum gain of 17dB. The initial measurements also indicated the bias dependence.

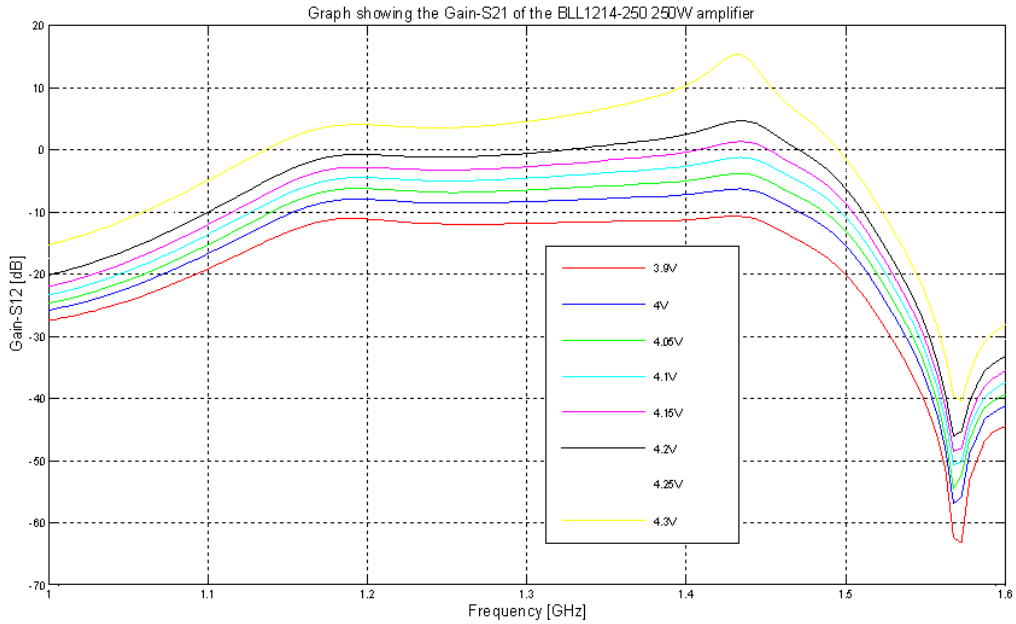

Figure 89 - Figure showing the initial small signal gain (S_{21}) measurements

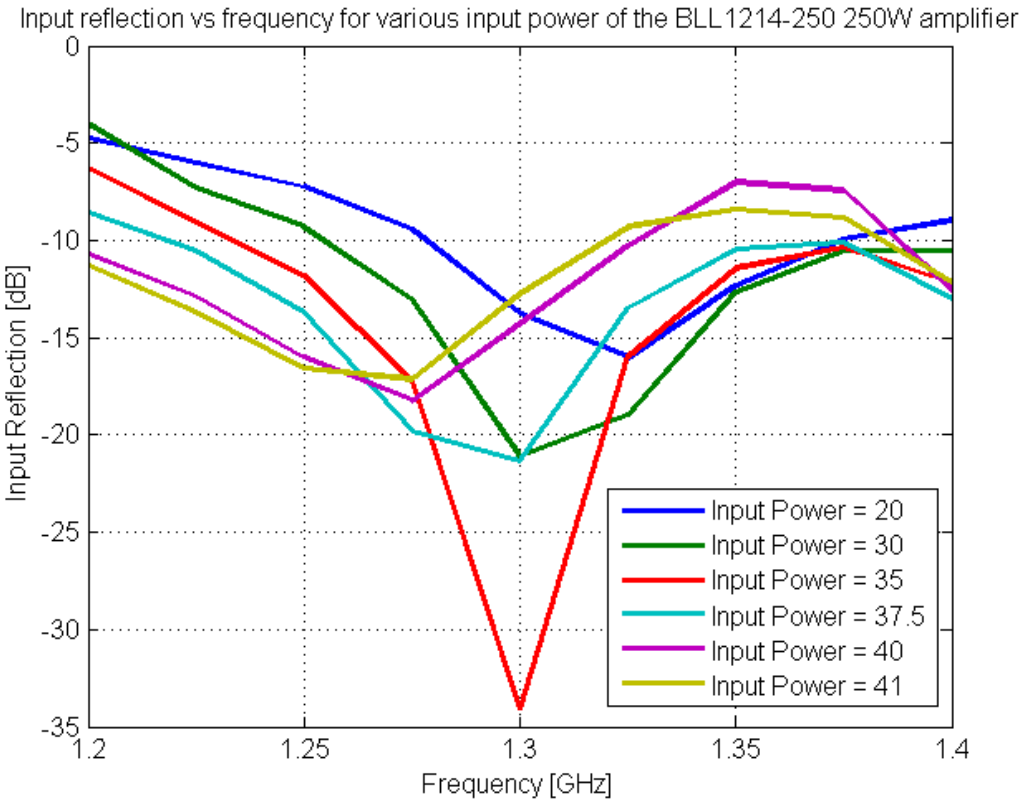

Figure 90 - Figure showing the measured pulsed high power input match of the BLL1214-250 250W amplifier

The pulsed high power input match measurements, Figure 90, show an improved result from the small signal measurements. A match of less than -10dB was obtained for ±80% of the band, although this result varies according to the input power. The best result was obtained at an input power of 37.5dBm.

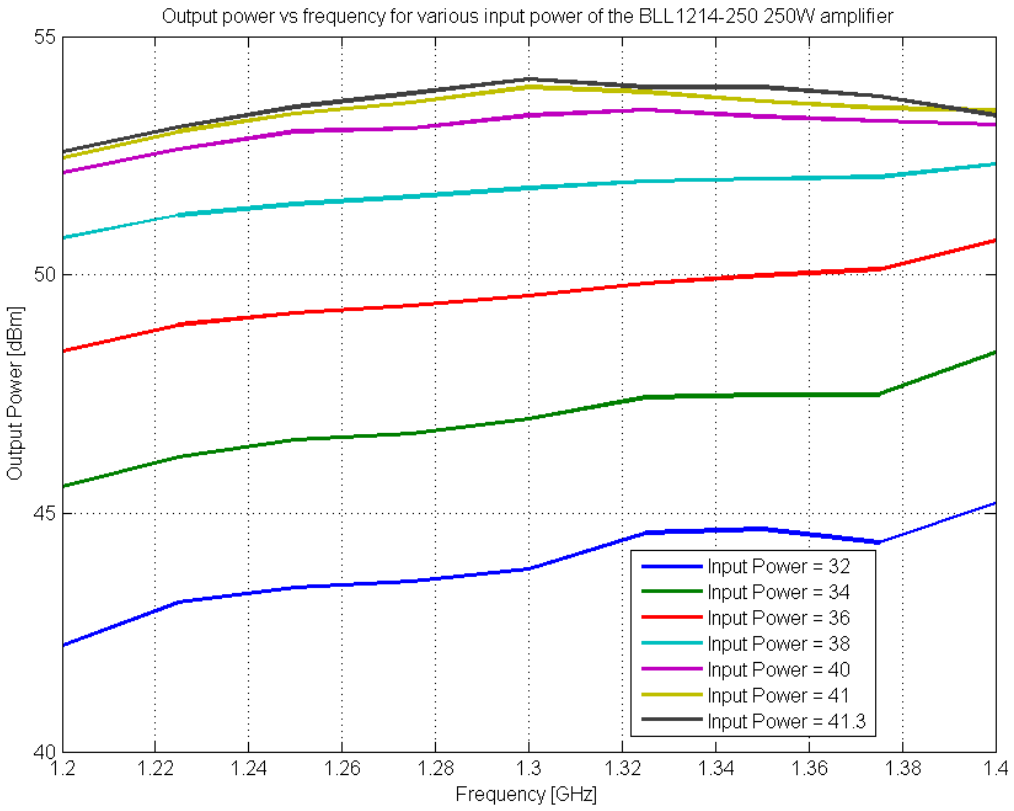

Figure 91 - Figure showing the Output Power of the BLL1214-250 250W amplifier

Figure 91 shows the output power with respect to frequency. This indicates that the amplifiers output power curve remains flat over the frequency band. The maximum gain ripple measured was less than 2dB. This shows a great improvement on the previous designs of the BLL1214-35 and the BLF2045 amplifiers.

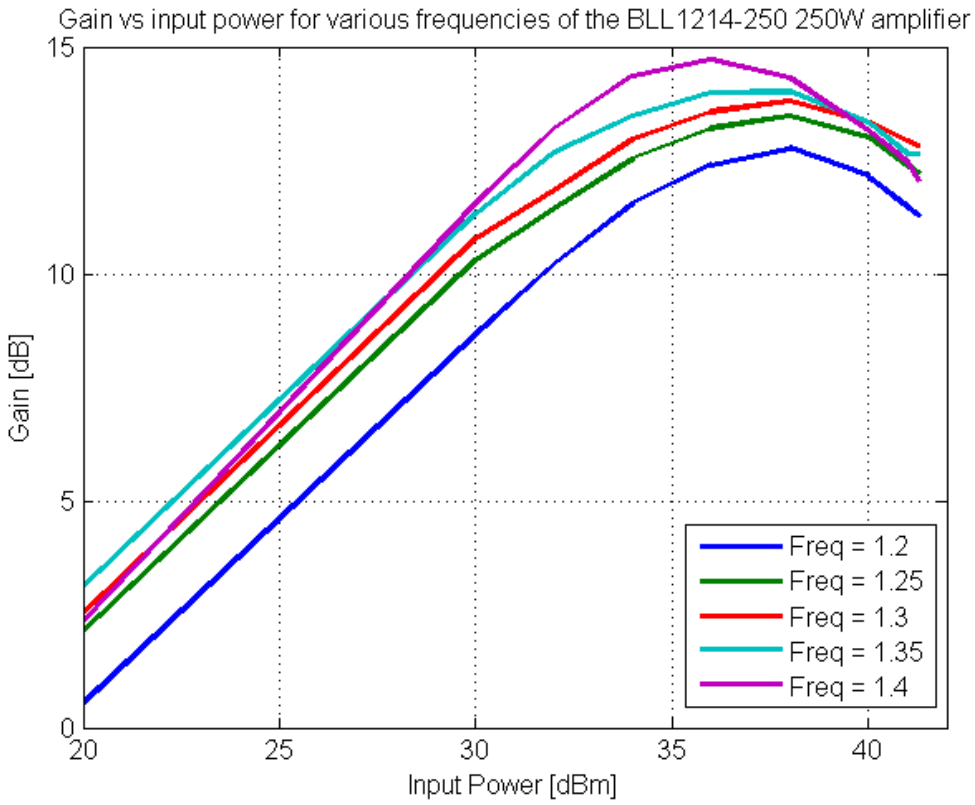

Figure 92 - Figure showing the gain of the BLL1214-250 250W amplifier with respect to the input power

Figure 92 shows how the gain of the BLL1214-250 amplifier varied as a direct result of the input power to the amplifier, which is linked to the effective gate bias point. This variation highlights one of the difficulties in designing of high power amplifiers, that being that input impedances change as a function of bias point and that the matching networks do not. Thus an amplifier can only be designed for a specific set of input powers. In the case of this design, the maximum gain was obtained at an input power of ±36dBm. This value corresponds to when the amplifier begins to enter compression as can be seen in Figure 94.

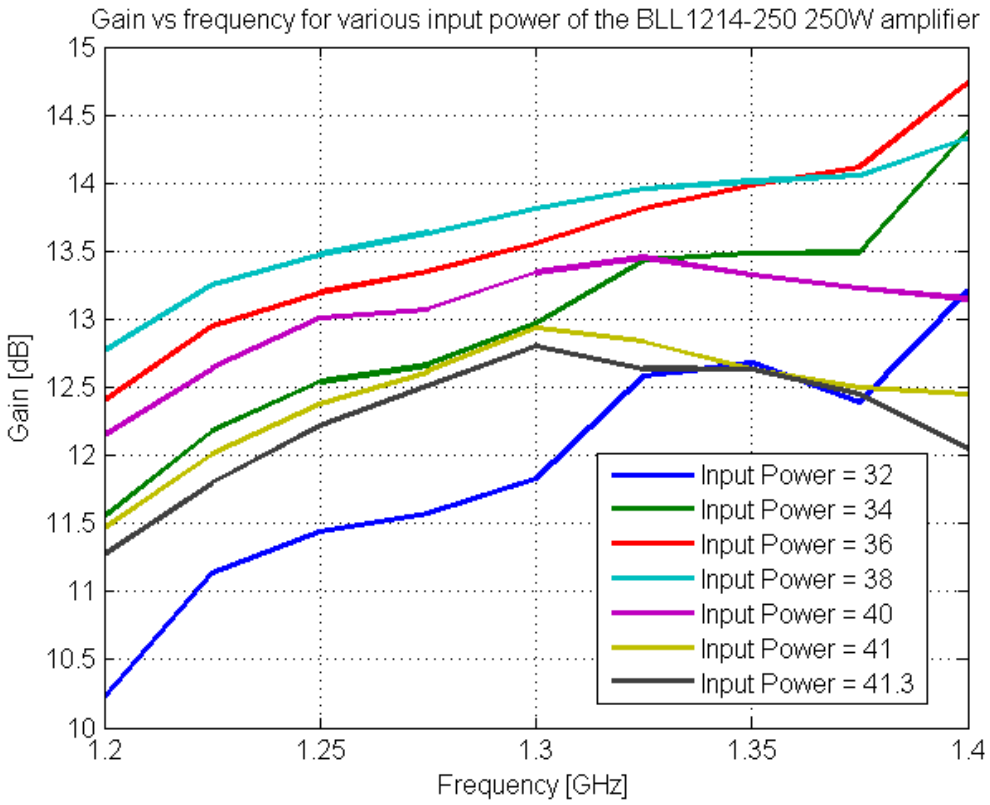

Figure 93 – Figure showing the gain curve of the BLL1214-250 250W amplifier with respect to frequency

This result shown in Figure 93 indicates the flatness of the gain curve with respect to frequency. This again shows an improvement from the previous designs. A gain flatness of less than 2 dB was achieved when operating at the desired power levels.

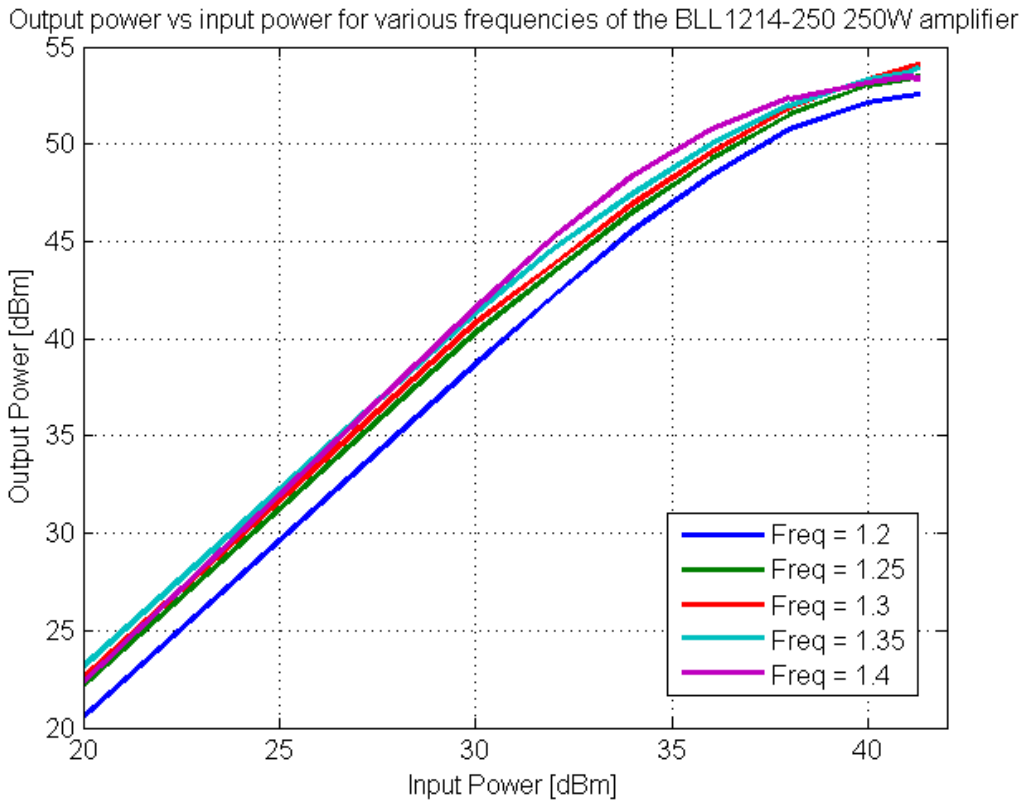

Figure 94 – Figure showing the Output power of the BLL1214-250 250W amplifier

Figure 94 shows the linearity of the output power of the BLL1214-250 amplifier with respect to input power. The amplifier remains linear up until an output power of approximately 50dBm. This again shows an improvement in the performance of the previous designs. A final output power of 54.1 dBm was obtained. This equates to over 250W of output power.

8.4.1 Recommendations

The design of the BLL1214-250, as mentioned before, showed a significant improvement from the design of the BLL1214-35 35W amplifier and the BLF2045 30W amplifier. The greatest area of improvement was the design of the impedance matching networks. This is attributed to the further use of the open circuited shunt transmission lines in order to improve the Chebyshev matching network model performance. This area could be further improved by creating the matching networks by using an electromagnetic simulation program such as CST or Zeland IE3D. The main areas which could still be improved on would be the S-parameter bias point measurement. This should be revisited to ensure that the matching networks are designed with the maximum input power in mind. This would degrade the performance of the amplifier at the lower input powers but improve the performance at the high end of the amplifiers performance.

8.5 Conclusion

The design of the BLL1214-250 250W amplifier was a great success. A final output power of over 250W was obtained. The gain of the amplifier showed an acceptable ripple of less than 2 dB across the required band as well as input power. The small signal, as well as the high power input match measurements were shown to be acceptable although there is room for improvement as the amplifier showed a slightly narrow band response. Overall, despite the fact that the amplifier meets all desired specifications; a single redesign would result in an overall improvement in the performance. The output power of the amplifier is unlikely to improve, but the iteration would allow for a better understanding of the bias point and input power dependence of the amplifier.

Chapter 9 – General Conclusion

9.1 Conclusion

A pulsed RF I-V curve measurement system has been presented. It is based on a modular design using off-the-shelf components. The system has been tested using both on-wafer measurements as well as full device measurements. The system has allowed I-V measurement to be performed well beyond the DC safe operating area (SOA). A noticeable difference in the magnitude of the I-V measurements between the DC I-V curves and the pulsed RF I-V curve was established. This is attributed to the various dispersion effects that present differently in the DC I-V measurements as opposed to the pulsed RF I-V measurements. There is also a subtle difference in the shape of the I-V curves when using a pulsed RF stimulus. The transition slope, from linear behaviour to saturation, of the I-V curves presents itself more gradually thus making a selection of the knee point more difficult.

A low impedance TRL test fixture has been presented and validated by using dielectric constant extraction. It has allowed repeatable and accurate s-parameter measurement of three high power LDMOS devices. The exact value of the dielectric constant allows an accurate circuit design process. The measurement of high power devices in a low impedance environment increases the measurement accuracy.

An equivalent circuit parameter extraction and modelling method is presented and it has yielded a circuit model that tracks the measured response of the high power BLF2045 30W device accurately. The method has yielded parameters for the modelling of the package, intrinsic and extrinsic device properties and thus allows a better amplifier design process.

A high power pulsed power supply has been designed and implemented. It has the ability to provide rapid response, high current pulses to an amplifier with little or no voltage ripple or pulse droop. It has the ability to recharge rapidly. Initial measurements showed that the power supply was able to function under high loads but the measurements were not able to define the limits of the design as the test fixture was not able to handle self heating. Under final amplifier measurement the power supply was able to provide the BLL1214-250 250W device with a stable voltage which had maximum 300mV ripple. It also had a 10% to 90% rise time of 5μs.

The BLF2045 30W amplifier design has been presented using pulsed I-V curve measurement, load-line placement and equivalent circuit model extraction. The performance was not as successful as hoped for and did not fully establish that pulse RF I-V measurements are an improvement on the DC measurements. This is attributed to a possible incorrect load line placement and to an inaccurate matching network design.

The BLL1214-35 35W amplifier design has been presented using load pull data as specified by the manufacturer. It has an improved design, as the matching network design used information gathered from the

BLF2045 design. It has an improved performance compared to the BLF2045 amplifier. The amplifier has a peak output power of over 35W although the gain and power flatness did not perform as hoped. This is attributed to the matching network design that, while improved, does not provide a sufficiently wideband performance. It also highlights the design dependence on the effective gate bias point due to the amplifiers' high input power signals.

A BLL1214-250 250W amplifier is presented using the load-pull data as provided by the manufacturer. The information gathered in the design process of the BLF2045 30W, and BLL1214-35 35W amplifiers allowed an improvement in the design. The amplifier performed well under high power testing. A high gain of between 12 dB and 15 dB was achieved across the band. The gain flatness is less than ±1dB when operating at high power. Input match shows an effective gate bias dependence. The amplifier provides a maximum output power of 54.1 dBm. The output power ripple is less than 2 dB across the band.

9.2 Recommendations

The pulsed RF I-V measurement system should be redesigned using commercial components. This should include wideband signal generation and amplification in order to test the devices at the correct operating frequencies. It will also allow the device to be tested into saturation.

The load line placement technique should be performed iteratively when using the pulsed RF I-V curves as the gradual knee area transition does not present an obvious load line position.

The low impedance test fixture should be modified to include active cooling. This will allow measurement of the device at high bias points beyond the SOA. The s-parameters obtained from these higher bias points should be used in the design of the amplifier.

An iterative process should be employed in the design of the input matching network to establish the bias point that should be used to provide the best overall performance.

An EM simulation package should be used for all matching network designs.

The ultimate goal of a 250W single stage L-Band amplifier was achieved. In the process a great deal was learned about low impedance measurements of active devices, large mismatch impedance transformation networks and high power amplifier design.

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