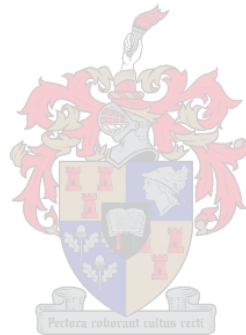


Low Impedance Characterisation and Modeling Of High Power LDMOS Devices

Pieter Jacob De Villiers Malan



Thesis presented in partial fulfillment of the requirements for the degree
of Master of Engineering at the University of Stellenbosch.

Supervisors: Dr. C. van Niekerk, Prof. P. W. van der Walt

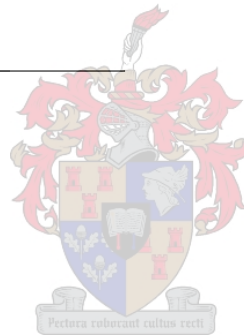
December 2005

Declaration

I, the undersigned, hereby declare that the work contained in this thesis is my own original work and that I have not previously in its entirety or in part submitted it at any university for a degree.

P. J. De V. Malan _____

Date _____



Abstract

Keywords - Low Impedance, TRL (Thru-Reflect-Line) Calibration, Substrate Parameter Extraction, LDMOS Small-Signal Parameter Extraction, Load Line Method, Power Amplifier.

In RF power transistor characterisation, the designer is confronted with low impedance measurements (typically from 1 Ohm to 12 Ohm). These transistors are contained in metal-ceramic packages of which the lead widths vary with power capability. This thesis presents a high-quality fixture design with low impedance TRL calibration standards for characterisation of an LDMOS transistor. Pre-matching networks are used to transform to the low impedance environment. Since these pre-matching networks are independent of the termination impedance, the low impedance port can always be designed to comply with the same dimension as the device which is being measured.

The low impedance TRL fixture together with modeling procedures was used to develop an equivalent circuit representation of an LDMOS transistor. The equivalent circuit representation was divided into two extraction steps of which the first step extracts the electrical package behavior for the metal-ceramic LDMOS package. This model accounts for package effects, like package lead capacitance and the parasitic resistance and inductance of the bond-wires. The second step extracts the small-signal intrinsic parameters of the LDMOS transistor. Realistic results are obtained for the LDMOS transistor despite the small values of the parasitics in the power devices. Measured S-parameters were used to verify the overall modeling methodology.

A class-AB pulsed power amplifier was designed with the equivalent circuit extracted to verify the circuit model. This circuit design was compared with a standard test circuit supplied by Motorola.

Opsomming

Sleutelwoorde - Lae Impedansie, TRL (Thru-Reflect-Line) Kalibrasie, Substraat Parameter Ekstraksie, LDMOS Kleinsein Parameter Ekstraksie, Laslyn Metode, Drywings Versterker.

Tydens RF drywingstransistor-karakterisering word die ontwerper met lae impedansie metings (tipies van 1 Ohm tot 12 Ohm) gekonfronteer. Hierdie transistors word in metaal-keramiek pakkies verpak en die transistor voerterminale varieer gewoonlik met drywingsvermoë. Hierdie tesis stel 'n hoë kwaliteit toestelontwerp met lae impedansie TRL kalibrasiestandaarde voor waarmee LDMOS transistor karakterisering gedoen kan word. Voorafaangepaste netwerke word gebruik om na die lae impedansie omgewing te transformeer. Aangesien hierdie vooraf aangepaste netwerke onafhanklik van die terminasie poortimpedansie is, kan die lae impedansie poort altyd ontwerp word om dieselfde dimensies as die gemete ontwerp aan te neem.

Die lae impedansie TRL toetsbasis, tesame met modelleringsprosesse, is gebruik om 'n ekwivalente stroombaanvoorstelling vir die LDMOS transistor te onttrek. Die ekwivalente stroombaan onttrekkingsprosedure is opgedeel in twee stappe waarvan die eerste stap 'n elektriese voorstelling vir die metaal-keramiek pakkie van die LDMOS transistor onttrek. Hierdie model maak voorsiening vir die pakkie se voerterminaal kapasitansies en die parasitiese weerstand en induktansie van die mikrohegtings drade. Die tweede stap is om die kleinsein interne model van die LDMOS transistor te onttrek. Realistiese resultate is verkry ten spyte van die klein parasitiese waardes van die LDMOS drywingstransistor. Gemete S-parameters is gebruik om hierdie ekwivalente stroombaanvoorstelling te verifieer.

'n Klas-AB gepulste drywingsversterker is ontwerp om die ekwivalente stroombaan onttrekking te verifieer. Hierdie versterkerontwerp is met 'n standaard toetsversterkerontwerp wat deur Motorola verskaf word, vergelyk.

*To my parents Cobus and Leone,
my fiancée, Annette
and my sister, Estie.*



Acknowledgements

I would like to express my sincere gratitude to my promoters, Dr Cornell van Niekerk and Prof. P.W. van der Walt, for their advice, guidance, patience and moral support, and for Reutech Radar Systems for the financial support without which this work would not have been possible. I would also like to thank Applied Wave Research for providing Microwave Office with which a lot of work was done.

I would like to thank Mr. W. Croukamp for many painstaking hours of meticulous machining over a period of two years. Mr. A. Cupido should also be mentioned for the etching of most of the microstrip circuits.

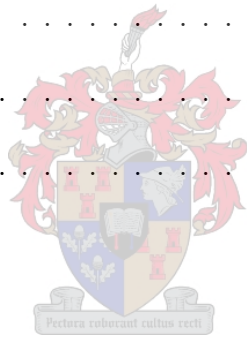
To my parents a special word of thanks for your understanding, unconditional support, encouragement and prayers.

Finally, I want to thank my heavenly Father who has given me the ability and perseverance to fulfill this task.

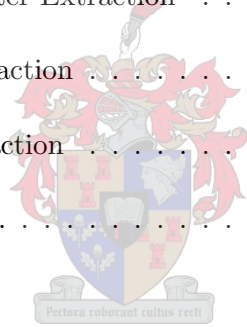
"A theory is something nobody believes, except the person who made it. An experiment is something everybody believes, except the person who made it." - Albert Einstein (1879-1955)

Contents

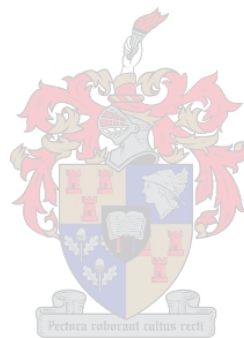
List of Tables	ix
List of Figures	x
1 Introduction	1
1.1 The History of Amplifiers	1
1.2 Problem Statement	1
1.3 Layout of Thesis	4
2 Klopfenstein Taper Design	5
2.1 Introduction	5
2.2 The Optimal Design of Transmission-Line Tapers	5
2.2.1 10 Ohm Klopfenstein Taper Design Example	9
2.2.2 5 Ohm Klopfenstein Taper Design Example	13
2.3 Conclusion	16
3 Advanced Low Impedance TRL Fixture Design	17
3.1 Introduction	17
3.2 A High-Quality Low Impedance TRL Test Fixture Design	18
3.2.1 50 Ohm Split Connector TRL Fixture	19
3.2.2 Low impedance Split Connector TRL Fixture	24



3.2.3	Split Connector Low Impedance TRL Calibration Standards Design	28
3.2.4	Split Block TRL Fixture	32
3.2.5	Split Block Low Impedance TRL Calibration Standards Design	36
3.3	Microstrip Transmission Line Parameter Extraction	42
3.3.1	The Direct TRL Calibration Technique	44
3.3.2	Parameter Extraction with the Multiline Method	46
3.4	Conclusion	53
4	LDMOS Transistor Equivalent Circuit Parameter Extraction	54
4.1	Introduction	54
4.2	LDMOS Package Parameter Extraction	54
4.3	Extrinsic Parameter Extraction	61
4.4	Intrinsic Parameter Extraction	68
4.5	Conclusion	75
5	Class-AB Amplifier Design	76
5.1	Introduction	76
5.2	Class-AB Load Line Amplifier Designed with Line-Stub Matching	76
5.3	Class-AB Load Line Amplifier Designed with Quarter-Wave Transformer Matching	82
5.4	Power Amplifier Measurements	84
5.5	Conclusion	93
6	General Conclusion	94
6.1	Conclusion	94
6.2	Recommendations	95

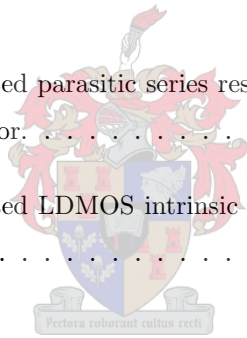


<i>Contents</i>	viii
A Klopfenstein Taper Matlab Code	96
B Microstrip Parameter Extraction Matlab Code	100
C LDMOS Power Amplifier Circuit Layout	112
C.1 Class-AB Power Amplifier Designed with Line-Stub Matching Networks	112
C.2 Motorola Test Circuit Layout	113
C.3 Class-AB Power Amplifier Designed with Quarter-Wave Transformer Matching Networks	114
C.4 Motorola Transistor Intrinsic Layout	115
Bibliography	120



List of Tables

3.1	Standard definitions table for the TRL standards used on a HP8510C vector network analyser used to perform a full two-port calibration.	31
3.2	Requirements for microstrip TRL standards used on the HP8510C vector network analyser.	31
3.3	Standard definitions table for the in-fixture TRL standards used on a HP8510C vector network analyser used to perform a full two-port calibration.	36
4.1	A comparison of the extracted parasitic series resistances and inductances of a 30-Watt Motorola RF power transistor.	69
4.2	A comparison of the extracted LDMOS intrinsic parameters of a 30-Watt Motorola RF power transistor.	73
5.1	A comparison of the amplifier design with the quarter-wave transformer matching and the Motorola test circuit design.	93



List of Figures

1.1	A graphical representation of the source and load match system and measurement uncertainty.	3
2.1	A tapered transmission line matching section and the model for an incremental length of tapered line.	7
2.2	The back-to-back 10 Ohm taper structure that was simulated in Microwave Office. This figure is not set to scale.	10
2.3	A comparison of the simulated and measured input reflection coefficient of a 50 Ohm to 10 Ohm Klopfenstein transformer placed back-to-back. The input reflection is shown on a linear scale.	11
2.4	A comparison of the simulated and measured input reflection coefficient of a 50 Ohm to 10 Ohm Klopfenstein transformer placed back-to-back. The input reflection is shown on a logarithmic scale.	11
2.5	A comparison of the simulated input reflection coefficient of a 50 Ohm to 10 Ohm single Klopfenstein transformer and a back-to-back transformer. The input reflection is shown on a linear scale.	12
2.6	A comparison of the simulated input reflection coefficient of a 50 Ohm to 10 Ohm single Klopfenstein transformer and a back-to-back transformer. The input reflection is shown on a logarithmic scale.	12
2.7	The back-to-back 5 Ohm taper structure that was simulated in Microwave Office. This figure is not set to scale.	14
2.8	A comparison of the simulated and measured input reflection coefficient of a 50 Ohm to 5 Ohm Klopfenstein transformer. The input reflection is shown on a linear scale.	15

2.9	A comparison of the simulated and measured input reflection coefficient of a 50 Ohm to 5 Ohm Klopfenstein transformer. The input reflection is shown on a logarithmic scale.	15
2.10	A comparison between the single simulated transformer and the Matlab calculated transformer, the input reflection is shown on a linear scale.	16
3.1	The layout of the split connector 50 Ohm TRL calibrations standards implemented in microstrip transmission lines (this figure is not set to scale).	19
3.2	The through standards reflection response measured after a TRL calibration was performed. An reflection of -40 dB over the frequency band are measured.	21
3.3	The through standards phase response measured after a TRL calibration was performed. A phase error of less than 0.6° is measured over the calibrated band.	21
3.4	The open standards input and output reflections measured on a 50 Ohm Smith chart.	22
3.5	A comparison between the measured phase response, the trace marked Line1 (△ marker), and the MWO (ideal) simulated phase response, the trace marked Microstrip Line1 (□ marker), of the line 1 standard.	22
3.6	A comparison between the measured phase response, the trace marked Line2 (△ marker), and the MWO (ideal) simulated phase response, the trace marked Microstrip Line2 (□ marker), of the line 2 standard.	23
3.7	A comparison between the measured input and output reflection responses, the traces marked Amp (◇ and ∇ marker), and the MWO (ideal) simulated input and output reflection responses, the traces marked GaAs Transistor (△ and □ marker), of the conjugate test amplifier circuit.	24
3.8	A comparison between the measured gain response, the trace marked Amp (□ marker), and the MWO (ideal) simulated gain response, the trace marked GaAs Transistor (△ marker), of the conjugate test amplifier circuit.	25
3.9	A comparison between the measured input and output reflection responses, the traces marked Amp (◇ and ∇ marker), and the MWO (fine-tuned) simulated input and output reflection responses, the traces marked GaAs Transistor (△ and □ marker), of the conjugate test amplifier circuit.	25

3.10 The SMA connector holder providing a 3-dimensional alignment. This connector can be aligned up or down (via Alignment A), right to left (via Alignment B), forwards and backwards (via Alignment C). 26

3.11 The cable straightener providing cable stability. The cable hole A is large enough for the use of a wide range of cable sizes. 27

3.12 The DUT clamp providing enough pressure to the DUT for repeatable measurements. The pressure point A is replaceable for measuring various devices with the same clamp. 28

3.13 The layout of the split connector low impedance TRL calibration standards implemented in microstrip transmission-lines (this figure is not set to scale). 30

3.14 A photo representation of the split connector TRL standards. From left to right are the open, line 2, line 1 and the through standards. 30

3.15 The through standards reflection response measured after TRL calibration was performed. A reflection better than -20 dB at 10.5 GHz are measured for both S_{11} and S_{22} . The reflection is illustrated on a logarithmic scale. 33

3.16 The through standards phase response measured after TRL calibration was performed. An phase error of less than 2° at 10.5 GHz are measured for the through standard. 33

3.17 A comparison between the measured phase response, the trace marked Measured Line1 (Δ marker), and MWO (ideal) simulated phase response, the trace marked Microstrip Line1 (\square marker), of the line 1 standard. 34

3.18 A comparison between the measured phase response, the trace marked Measured Line2 (Δ marker), and MWO (ideal) simulated phase response, the trace marked Microstrip Line2 (\square marker), of the line 2 standard. 34

3.19 The layout of the split block low impedance TRL calibration standards implemented in microstrip transmission-lines (this figure is not set to scale). 37

3.20 A photo representation of the split block and the TRL standards. From left to right are the open, line 1, line 2 and through standards. 37

3.21 The through standards reflection response measured after TRL calibration was performed. A reflection better than -35 dB up to 8 GHz are measured for both S_{11} and S_{22} . The reflection is illustrated on a logarithmic scale. 39

3.22 The through standards phase response measured after TRL calibration was performed. A phase error of 0.5° at 8 GHz is measured for the through standard. 39

3.23 A comparison between the measured phase response, the trace marked Microstrip Line1 (Δ marker), and the MWO (ideal) simulated phase response, the trace marked Measured Line1 (\square marker), of the line 1 standard. 40

3.24 A comparison between the measured phase response, the trace marked Microstrip Line2 (Δ marker), and the MWO (ideal) simulated phase response, the trace marked Measured Line2 (\square marker), of the line 2 standard. 40

3.25 The measured input and output reflection phase responses of the open standard. The open reflections are displayed on a low impedance (12 Ohm) Smith chart. 41

3.26 The through standards reflection response measured after a TRL calibration was performed. An reflection of -30 dB over the frequency band are measured. 41

3.27 The through standards phase response measured after TRL calibration was performed. The worst phase error, an error of 0.9° , was measured at 4.5 GHz for the through standard. 42

3.28 The measured input and output reflection phase responses of the short standard. The short standards reflections are displayed on a low impedance (12-ohm) Smith chart. 43

3.29 A comparison between the measured phase response, the trace marked Line1 (Δ marker), and MWO (ideal) simulated phase response, the trace marked Microstrip Line1 (\square marker), of the line 1 standard. 43

3.30 A comparison between the measured phase response, the trace marked Line2 (Δ marker), and MWO (ideal) simulated phase response, the trace marked Microstrip Line2 (\square marker), of the line 2 standard. 44

3.31 The extracted Rogers 6010.2 substrate parameters with the two-tier method. The line impedance is illustrated on the left hand side while the effective dielectric constant is illustrated on the right hand side. 46

3.32 The impedance and effective dielectric constant extracted with the multilayer method from uncalibration data. 50

3.33 The impedance and effective dielectric constant extracted with the multilayer method after a SOLT calibration. 50

3.34 A comparison between the MWO (modified) simulated phase response, the trace marked Microstrip Line1 (\square marker), and the measured phase response, the trace marked Line1 (\triangle marker), of the line 1 standard. 52

3.35 A comparison between the MWO (modified) simulated phase response, the trace marked Microstrip Line2 (\square marker), and the measured phase response, the trace marked Line2 (\triangle marker), of the line 2 standard. 52

4.1 An illustration of the LDMOS transistors small-signal equivalent circuit representation and the LDMOS metal-ceramic package terminology. 55

4.2 A photo representation of the Philips transistor package used as the open and short-all structures in the package extraction measurements. The packaged area that is hatched at 45° is the gate flange, the area that is dashed is the drain flange and the solid area is the grounded source. 56

4.3 An equivalent circuit representation of the open standard used. 56

4.4 An equivalent circuit representation of the short-all standard used. 57

4.5 A comparison between the measured open standards input and output reflections, traces marked Measured Open Standard (\square marker), and the open equivalent circuit model input and output reflections, traces marked LDMOS Open Model (\triangle marker). These S-parameters are illustrated on a 12-ohm Smith chart. 57

4.6 A comparison between the measured open standards transmission magnitude, the trace marked Measured Open Standard (\square marker), and the open equivalent circuit model transmission magnitude, the trace marked LDMOS Open Model (\triangle marker). 58

4.7 A comparison between the measured open standards transmission phase, the trace marked Measured Open Standard (\square marker), and the open equivalent circuit model transmission phase, the trace marked LDMOS Open Model (\triangle marker). 58

4.8 A comparison between the measured short-all standards input and output reflections, traces marked Measured Shortall Standard (\square marker), and the short-all equivalent circuit model input and output reflections, traces marked LDMOS Shortall Model (\triangle marker). These S-parameters are illustrated on a 12-ohm Smith chart. 59

4.9	A comparison between the measured short-all standards transmission magnitude, the trace marked Measured Shortall Standard (\square marker), and the short-all equivalent circuit model transmission magnitude, the trace marked LDMOS Shortall Model (\triangle marker).	59
4.10	A comparison between the measured short-all standards transmission phase, the trace marked Measured Shortall Standard (\square marker), and the short-all equivalent circuit model transmission phase, the trace marked LDMOS Shortall Model (\triangle marker).	60
4.11	Delta-star transformation of the small-signal circuit of an off-state biased LDMOS transistor.	61
4.12	A comparison between the measured Z_1 series branch impedance, the trace marked Measured Model (\triangle marker), and the extrinsic final equivalent circuit model, the trace marked Final Model (\square marker), and the extrinsic initial model, the trace marked Initial Model (\diamond marker).	63
4.13	A comparison between the measured Z_1 series branch impedance, the trace marked Measured Model (\triangle marker), and the extrinsic final equivalent circuit model, the trace marked Final Model (\square marker), and the extrinsic equivalent initial model, the trace marked Initial Model (\diamond marker).	64
4.14	A comparison between the measured Z_2 series branch impedance, the trace marked Measured Model (\triangle marker), and the extrinsic final equivalent circuit model, the trace marked Final Model (\square marker), and the extrinsic initial model, the trace marked Initial Model (\diamond marker).	65
4.15	A comparison between the measured Z_2 series branch impedance, the trace marked Measured Model (\triangle marker), and the extrinsic final equivalent circuit model, the trace marked Final Model (\square marker), and the extrinsic initial model, the trace marked Initial Model (\diamond marker).	65
4.16	A comparison between the measured Z_3 series branch impedance, the trace marked Measured Model (\triangle marker), and the extrinsic final equivalent circuit model, the trace marked Final Model (\square marker), and the extrinsic initial model, the trace marked Initial Model (\diamond marker).	66

4.17 A comparison between the measured Z_3 series branch impedance, the trace marked Measured Model (Δ marker), and the extrinsic final equivalent circuit model, the trace marked Final Model (\square marker), and the extrinsic initial model, the trace marked Initial Model (\diamond marker). 66

4.18 A comparison between the measured extrinsic cold models input and output reflections, traces marked Measured Model (Δ marker), and the extrinsic final equivalent circuit models input and output reflections, traces marked Final Model (\diamond marker), and the extrinsic initial models input and output reflections, traces marked Initial Model (\square marker). These S-parameters are illustrated on a 12-ohm Smith chart. 67

4.19 A comparison between the measured extrinsic cold de-embedded transmission magnitude, the trace marked Measured Model (Δ marker), and the extrinsic final circuit model transmission magnitude, the trace marked Final Model (\diamond marker), and the extrinsic initial model transmission magnitude, the trace marked Initial Model (\square marker). 67

4.20 A comparison between the measured extrinsic cold de-embedded transmission phase, the trace marked Measured Model (Δ marker), and the extrinsic final circuit model transmission phase, the trace marked Final Model (\diamond marker), and the extrinsic initial model transmission phase, the trace marked Initial Model (\square marker). 68

4.21 A representation of a LDMOS small-signal intrinsic equivalent circuit model. . . 69

4.22 The extracted C_{gs} and C_{ds} capacitances at multiple biasing conditions. 71

4.23 The extracted G_m and C_m parameters for the voltage dependent current generator at multiple biasing conditions. 72

4.24 The extracted R_{gd} and R_{ds} resistances at multiple biasing conditions. 72

4.25 The extracted C_{gd} capacitance at multiple biasing conditions. 72

4.26 A comparison between the measured intrinsic input and output reflections, traces marked LDMOS Transistor Measured (\square marker), and the Microwave Office complete circuit model input and output reflections, traces marked LDMOS MWO Model (Δ marker), and the Matlab starting model input and output reflections, traces marked LDMOS Matlab Model (\diamond marker). 73

4.27	A comparison between the measured intrinsic transmission magnitude, traces marked LDMOS Transistor Measured (\square marker), and the Microwave Office complete circuit model transmission magnitude, traces marked LDMOS MWO Model (\triangle marker), and the Matlab starting model transmission magnitude, traces marked LDMOS Matlab Model (\diamond marker).	74
4.28	A comparison between the measured intrinsic transmission phase, traces marked LDMOS Transistor Measured (\square marker), and the Microwave Office complete circuit model transmission phase, traces marked LDMOS MWO Model (\triangle marker), and the Matlab starting model transmission phase, traces marked LDMOS Matlab Model (\diamond marker).	74
5.1	Measured current-voltage ($I_{DS} - V_{DS}$) characteristic curves for different V_{GS} voltages for a Motorola LDMOS transistor.	78
5.2	A schematic representation for determining Z_{opt} from R_{opt}	79
5.3	A schematic of the drain bias and matching circuit for the class-AB amplifier. . .	80
5.4	The real and imaginary parts of R_{opt} for the drain matching circuit.	80
5.5	A schematic of the gate bias and matching circuit for the class-AB amplifier. . .	81
5.6	The simulated class-AB amplifier input reflection (\triangle marker), output reflection (\diamond marker) and gain (\square marker).	82
5.7	A schematic of the drain bias and matching circuit for the class-AB amplifier. . .	83
5.8	The real and imaginary parts of R_{opt} for the drain matching circuit.	84
5.9	A schematic of the gate bias and matching circuit for the class-AB amplifier. . .	85
5.10	A comparison between the measured amplifiers gain and input reflection, traces marked Measured ClassAB Amp, and the simulated amplifiers gain and input reflection, traces marked Class AB Amplifier.	86
5.11	A comparison between the measured fine-tuned amplifiers gain and input reflection, traces marked Measured ClassAB Amp, and the simulated amplifiers gain and input reflection, traces marked Class AB Amplifier.	86

5.12	The class-AB amplifiers simulated input and output reflections (traces marked \diamond and ∇) and the input and output stability circles (traces marked \triangle and \square). The data is shown on a 50 Ohm Smith chart.	87
5.13	The output reflection of the mini-circuits driver amplifier.	88
5.14	A comparison between the amplifier's simulated gain and input reflection (traces marked Class AB Amplifier) and the amplifier's measured gain and input reflection (traces marked ClassABamp Measurements).	89
5.15	A comparison between the amplifier's fine-tuned gain and input reflection (traces marked Class AB Amplifier) and the amplifier's measured gain and input reflection (traces marked ClassABamp Measurements).	89
5.16	The Motorola class-AB amplifier's measured gain (trace marked \diamond), input and output reflections (traces marked \triangle and \square respectively).	90
5.17	A schematic and photo representation of the measurement setup used to perform swept power amplifier (DUT) measurements with a HP8562 spectrum analyser.	90
5.18	The input versus output power levels for both the designed amplifier and Motorola test amplifier. Power levels at different frequencies for each amplifier are shown.	92
5.19	The drain current as a function of input power for both the designed amplifier and Motorola test amplifier. Currents at different frequencies for each amplifier are shown.	92
C.1	The class-AB load line pulsed amplifier schematic. This figure is not set to scale.	112
C.2	The class-AB load line pulsed amplifier photo representation. This figure is not set to scale.	113
C.3	The Motorola 945 MHz broadband test circuit schematic. This figure is not set to scale.	113
C.4	The Motorola 945 MHz broadband test circuit photo representation. This figure is not set to scale.	114
C.5	The class-AB load line pulsed amplifier schematic. This figure is not set to scale.	114
C.6	The class-AB load line pulsed amplifier photo representation. This figure is not set to scale.	115

- C.7 The Motorola MRF9030 intrinsic photo layout. Notice the gate and drain bond-wire pads as well as the cascaded MOSFETs to obtain a single 30 Watt transistor. 115
- C.8 The Motorola MRF9030 intrinsic photo layout (zoomed in). Again, notice the gate and drain bond-wire pads as well as the cascaded MOSFETs to obtain a single 30 Watt transistor. 116



Chapter 1

Introduction

1.1 The History of Amplifiers

The development of RF power sources started in 1895 through to the mid 1920s. In those days RF power was generated by spark, arc, and alternator techniques. Vacuum tube transmitters were dominant from the late 1920s through the mid 1970s. Discrete solid state RF power devices began to appear at the end of the 1960s with the introduction of silicon bipolar transistors. These transistors had several disadvantages namely, restricted amplification, limited bandwidth, high noise figure, low efficiency, and physically large structures. GaAs MESFETs were introduced in the late 1970s and offered usable gain for amplification at lower microwave frequencies. In the 1980s and 1990s a variety of new solid state devices were introduced by using a variety of new materials such as InP, SiC, and GaN. Today, GaAs FETs and LDMOS transistors are used in most applications, because they have accomplished similar power amplification with lower noise, higher efficiency and smaller structures. Some of these devices can amplify up to 100 GHz or more [1].

Today's RF power transistors, as opposed to older transistors, have greatly improved performance, because they have higher efficiencies and broader bandwidths for multimedia services. Because these devices consume less power, they promise to remain cooler, which leads to simplifications in product design and improved product reliability.

1.2 Problem Statement

RF and microwave power amplifiers are used in a wide variety of applications including wireless communications. A power amplifier is a circuit that converts DC power into a significant

amount of RF or microwave output power. RF power can be generated by a wide variety of techniques using a wide variety of devices. In modern applications frequencies from VLF (very low frequency) through millimeter wave are used for communication, navigation, and broadcasting. Output powers vary from 10 mW in short-range unlicensed wireless systems to 1 MW in long-range broadcast transmitters.

Laterally diffused metal-oxide-silicon (LDMOS) transistor offers a good alternative to GaAs MESFET and silicon bipolar junction (BJT) transistors for L- or S-Band power amplifiers [2]. LDMOS technology offer higher RF gain, linearity, better intermodulation distortion and is more cost effective compared to competing technologies [3, 4]. LDMOS devices typically operate from 26-36 V_{dc} supplies and are currently available with power outputs up to 250 Watt at frequencies up to 2 GHz [1, 5]. LDMOS amplifiers are contained in leaded packages. The lead widths of the package devices usually vary with power capability, the higher the output power the wider the lead width and the lower the impedance. A thick substrate with a low dielectric constant could be used to manufacture wide 50 Ohm lines that match the width of the transistor leads, but this causes a large dimensional discontinuity between the line and the transistor. The large impedance mismatch between the measured system and the transistor results in poor measurement accuracy and also holds the risk that the transistor may oscillate. Another problem, because of this excessive mismatch, is that the device measured source and load match would be situated on the edge of the Smith chart (basically short circuited), as illustrated in Figure 1.1, causing measurement accuracy problems. The system source and load match have a certain impedance uncertainty area, although this area has the same radius at the measurement impedance, the source and load errors are greatly magnified and directly result in significant measurement inaccuracy, as illustrated in Figure 1.1.

Measuring these devices requires a test fixture to connect to coaxial-based test equipment. The main goal is to design a high-quality RF fixture with low impedance TRL (Thru-Reflect-Line) calibration standards that will provide repeatable and accurate in-fixture low impedance measurements [6]. The thick substrate could be used to manufacture wide 50 Ohm lines that matches the transistor leads, but many systems are forced to use a particular substrate with a specific thickness and dielectric constant and the fixture has to accommodate these substrate variations. A wide 50 Ohm line also causes large discontinuities at the coaxial to microstrip transition because in most cases the connector pin diameter and line width differs a great deal. Large reflections between the intended measurement plane and the network analyser ports has a negative impact on calibration accuracy. Finally, the fixture has to be able to transform the 50 Ohm measurement environment to the low impedance environment to ensure that the reflections seen by the vector network analyser from the low impedance calibration standards are as small as possible, this resulting in improved input and output reflection measurements. An

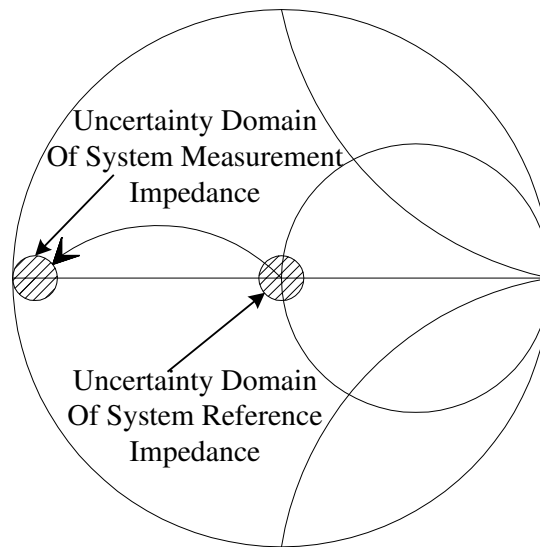


Figure 1.1: A graphical representation of the source and load match system and measurement uncertainty [5].

advantage of transforming to the low impedance environment is that the mismatch between the 50 Ohm measurement environment and the low impedance environment is smaller, and device measurements can be performed more accurately.

Present low impedance TRL technology is based on quarter-wave pre-matching [5, 6]. An alternative to pre-matching is to use wide microstrip 50 Ohm lines [7]. The disadvantage of the wide 50 Ohm line design is that custom thickness substrate has to be manufactured, which is very expensive and not commercially used. This technique is not capable of measuring a wide variety of devices because for different devices with different lead dimensions, different custom substrates has to be manufactured. The disadvantage with the quarter-wave pre-matching networks is that these networks only provide narrowband matches and these structures will have a large mismatch which will degrade the vector network analyser calibration performance. The risk for the transistor to become unstable is minimised by terminating the transistor ports with wideband low impedance terminations.

This thesis presents a high-quality fixture with low impedance TRL microstrip calibration standards for characterisation of an LDMOS transistor. The pre-matching networks used are cascaded transformer arrangements that were extended into microstrip transmission line tapers to allow the characterisation of networks in a low impedance environment. With this approach it is possible to accommodate any particular substrate, connector and device. The advantage of the taper pre-matching networks is that these networks operate as highpass filters to ensure a wideband match.

1.3 Layout of Thesis

The aim of this thesis is to develop a low impedance TRL test fixture with a systematic procedure with which the small-signal equivalent circuit parameter extraction of an LDMOS transistor can be performed.

Chapter 2 describes the design of the Klopfenstein taper which is used to act as transitions between the 50 Ohm measurement environment and the low impedance environment. Two taper examples were implemented to verify the Klopfenstein taper design.

Chapter 3 describes the development of two low impedance test fixtures, namely the split connector and the split block test fixture. Both these fixtures use TRL calibration standards to perform a full two-port calibration. The chapter ends with substrate parameter extraction performed with the split block low impedance test fixture. The substrate parameter extraction performed here will be used in the final chapter to design a power amplifier.

Chapter 4 outlines the small-signal parameter extraction procedure performed on an LDMOS transistor. The LDMOS transistor parameter extraction can be divided into three parts, firstly, the transistor package model extraction, then the extrinsic model extraction and lastly the intrinsic model extraction. The package model represents the transistor's gate and drain leads, the extrinsic model represents the bond-wires that connect the gate and drain lead to the transistor-die, while the intrinsic model represents the transistor-die.

Finally, Chapter 5 concludes with the design of a class-AB power amplifier. This amplifier is designed with the small-signal equivalent circuit extracted in Chapter 4 and Cripp's [8] load line method. This design is compared with Motorola's test circuit example to verify the design technique.

Chapter 2

Klopfenstein Taper Design

2.1 Introduction

The Klopfenstein taper was designed to transform the 50 Ohm measurement environment to a low impedance environment with a broadband match. In order to achieve broadband matching a multi-section transformer can be designed with a large number of matching stages. These structures are designed to act as pre-matching networks for device measurements in the low impedance environment. With this approach it is possible to accommodate any particular device and substrate. This chapter merely describe the design of the Klopfenstein taper together with two taper examples. Chapter 3 makes use of these structures for performing a low impedance TRL calibration.

2.2 The Optimal Design of Transmission-Line Tapers

To resolve the low impedance issues in RF power transistor characterisation, multi-section quarter-wave transformers were used to match the 50 Ohm measurement environment to the low impedance transistor leads. The change in the impedance level is obtained in a number of discrete steps. By allowing the number of discrete steps to increase indefinitely for a fixed length, a continuous transmission line taper can be formed. These impedance levels are transformed by a tapered transition which has a characteristic impedance that varies continuously in a smooth fashion from the 50 Ohm vector network analyser environment to the low impedance of the transistor.

The wideband impedance transformers can typically be realised in three different taper structures, namely the exponential taper, triangular taper and the Klopfenstein taper [9]. By chang-

ing the type of taper different passband characteristics can be obtained. The Klopfenstein taper gives a more acceptable reflection response than either the triangular or exponential taper response [10, 11]. The performance of this taper is optimal in the sense that for a given reflection coefficient magnitude in the passband, the taper has the shortest matching section. The characteristic impedance of this taper is a real number and is independent of the frequency. The wave propagating in the line is essentially TEM, and the propagation constant is purely imaginary and proportional to frequency.

The theory of small reflections is used to predict the reflection coefficient response as a function of the taper impedance, $Z(z)$. Consider the continuously tapered line shown in Figure 2.1 as being made up of a number of incremental sections of length Δz , with an impedance change $\Delta Z(z)$ from one section to the next. The incremental reflection coefficient from the step at z is given by

$$\Delta\Gamma = \frac{(Z + \Delta Z) - Z}{(Z + \Delta Z) + Z} \approx \frac{\Delta Z}{2Z}. \quad (2.1)$$

In the limit as $\Delta z \rightarrow 0$, we have an exact differential

$$d\Gamma = \frac{dZ}{2Z} = \frac{1}{2} \frac{d \ln Z / Z_o}{dz} dz \quad (2.2)$$

since

$$\frac{d \ln Z / Z_o}{dz} dz = \frac{1}{f} \frac{df(z)}{dz} dz \quad (2.3)$$

By using the theory of small reflections, the total reflection coefficient at $z = 0$ can be found by summing all the partial reflections with their appropriate phase shifts.

$$\Gamma(\Theta) = \frac{1}{2} \int_{z=0}^L \exp^{-2j\beta z} \ln \frac{Z}{Z_o} dz \quad (2.4)$$

where $\Theta = 2\beta l$. β is defined as

$$\beta = \frac{2\pi}{\lambda} \quad (2.5)$$

where λ is the wave length.

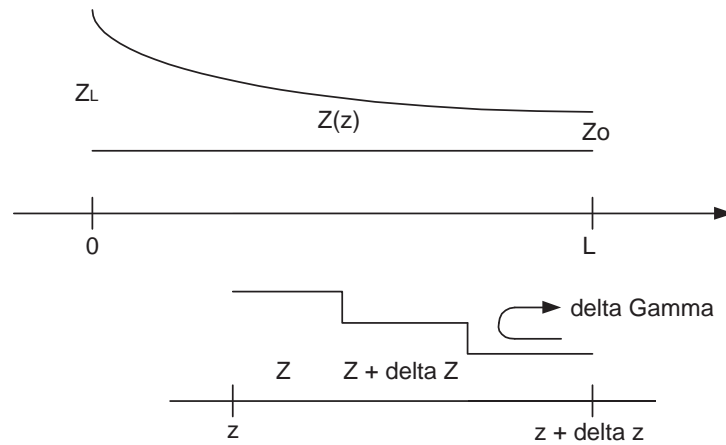


Figure 2.1: A tapered transmission line matching section and the model for an incremental length of tapered line.

Thus, if $Z(z)$ is known, $\Gamma(\Theta)$ can be found as a function of frequency. Alternatively, if $\Gamma(\Theta)$ is specified, then $Z(z)$ can be calculated.

The detailed derivation will not be presented here, only the necessary results for the design of the Klopfenstein taper are given below [9]. The logarithm of the characteristic impedance variation for the Klopfenstein taper is given by

$$\ln Z(z) = \frac{1}{2} \ln Z_O Z_L + \frac{\Gamma_O}{\cosh A} A^2 \phi\left(\frac{2z}{L} - 1, A\right), \quad \text{for } 0 \leq z \leq L, \quad (2.6)$$

where Z_O and Z_L are the two impedances to be matched, Γ_O the initial reflection coefficient, L the length of the taper and A the maximum allowed reflection magnitude in the passband. The function $\phi(x, A)$ is defined as

$$\phi(x, A) = -\phi(-x, A) = \int_0^x \frac{I_1(A\sqrt{1-y^2})}{A\sqrt{1-y^2}} dy, \quad \text{for } |x| \leq 1, \quad (2.7)$$

where $I_1(x)$ is the modified Bessel function and x is the length of the taper. The reflection coefficient at zero frequency is given as

$$\Gamma_O = \frac{Z_L - Z_O}{Z_L + Z_O} \approx \frac{1}{2} \ln\left(\frac{Z_L}{Z_O}\right). \quad (2.8)$$

The passband is defined as $\beta L \geq A$, and so the maximum ripple in the passband is

$$\Gamma_m = \frac{\Gamma_O}{\cosh A}, \quad (2.9)$$

because $\Gamma(\Theta)$ oscillates between $\pm \frac{\Gamma}{\cosh A}$ for $\beta L \geq A$. β is the propagation constant of the line and is purely imaginary and proportional to the frequency.

These equations were implemented in the Matlab environment (see Appendix A) to calculate the impedance and reflection variation of the taper over the length of the taper. Equation 2.6 represent the impedance profile of the taper. This profile has to be converted into physical microstrip transmission line widths. The impedances obtained from Equation 2.6 together with the substrate parameters (ε_r and h) were used to calculate the physical width variation of the taper over the length of the taper. Equation 2.10 was used in the Matlab environment to extract the width of the taper as a function of impedance variation [12]. By varying the width, W , and keeping the height, h , constant in Equation 2.10, can the impedance be matched to the impedance profile calculated with Equation 2.6. The physical width of the transmission line varies with impedance.

$$Z_o = \frac{120\pi}{\sqrt{\varepsilon_{r,eff}} \left[\frac{W}{h} + 1.393 + 0.667 \ln\left(\frac{W}{h} + 1.444\right) \right]} \quad (2.10)$$

$$\begin{aligned} \varepsilon_{r,eff0} &= \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \frac{1}{\sqrt{1 + \frac{12h}{W}}} \\ \varepsilon_{r,eff}(n) &= \varepsilon_r - \frac{\varepsilon_r - \varepsilon_{r,eff0}}{1 + P_f} \\ P_f &= P_1 P_2 (0.1844 + P_3 P_4) (10f(n)h) \\ P_1 &= 0.27488 + (0.6315 + \frac{0.525}{(1 + 0.157f(n)h)^{20}}) \frac{W}{h} - 0.065683 \exp(-8.7513 \frac{W}{h}) \\ P_2 &= 0.33622(1 - \exp^{-0.03442\varepsilon_r}) \\ P_3 &= (0.0363 \exp(-4.6 \frac{W}{h})) (1 - \exp^{(f(n)h/3.87)^{4.97}}) \\ P_4 &= 1 + 2.751(1 - \exp^{(\frac{-\varepsilon_r}{15.916})^8}) \end{aligned} \quad (2.11)$$

where Z_o is the characteristic impedance, $\varepsilon_{r,eff}(n)$ is the effective dielectric constant, accounting for dispersion, of the substrate, ε_r is the dielectric constant of the substrate, W is the width of the microstrip line and h is the height of the substrate. The physical widths calculated above were drawn via Matlab into an AutoCad file, (*.dxf). The figure created in AutoCad was then imported as an EM structure into Microwave Office [13] to perform EM simulations.

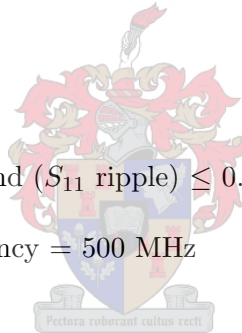
The effect of the $\varepsilon_{r,eff}$ on the length of the taper design was not accounted for. A fixed scaling factor was used rather than to scale each section to account for $\varepsilon_{r,eff}$ changes. This could be the explanation for small differences observed between the measured and modelled taper structures.

Two transformer examples were designed, namely a taper realizing a 50 Ohm to 10 Ohm transformation and a taper realizing a 50 Ohm to 5 Ohm transformation. Both these tapers are implemented on GIL MC3D medium frequency laminated substrate with a height of 0.762 mm and an ε_r of 3.86. These two example tapers were implemented on the GIL substrate to verify the technique discussed above and differ from the substrate used in the final product.

2.2.1 10 Ohm Klopfenstein Taper Design Example

A 10 Ohm Klopfenstein taper with the following specifications was simulated in Microwave Office [13] and compared with the results measured on a vector network analyser [14].

- Input Impedance = 50 Ω
- Output Impedance = 10 Ω
- Maximum Ripple in Passband (S_{11} ripple) ≤ 0.1
- Minimum Operating Frequency = 500 MHz



In order to accommodate the experimental evaluation of the taper design in a 50 Ohm measurement environment, two back-to-back 10 Ohm tapers were simulated and measured. The Microwave Office EM simulator [13] was used to calculate the S-parameters of the back-to-back taper structure shown in Figure 2.2. For the 10 Ohm Klopfenstein taper, illustrated in Figure 2.2, the taper impedance at $x = 0$ is 10 Ohm while the taper impedance at $x = \pm L$ is 50 Ohm. Both port-impedances of the taper are therefore 50 Ohm. The EM simulation of the 10 Ohm taper, displayed in Figure 2.2, was configured as follows:

- Frequency Range
 - 0.3 GHz to 3 GHz in steps of 0.01 GHz
- Enclosure
 - Size: 318 mm by 50 mm
 - Grid: 318 by 200 divisions
 - Cell Size: X = 1 mm, Y = 0.25 mm

- Dielectric Layers
 - Layer 1: Air, Thickness = 10 mm, $\epsilon_r = 1$, Loss Tangent = 0
 - Layer 2: Substrate, Thickness = 0.762 mm, $\epsilon_r = 3.86$, Loss Tangent = 0
- Boundaries
 - Enclosure Top: Approximately Open
 - Enclosure Bottom: Perfect Conductor

The choice of the cell size used in the EM simulation was a compromise between acceptable simulation accuracy and simulation time. For acceptable simulation accuracy and time, the cell size at the highest simulation frequency for a half-wavelength was chosen to have a minimum of 10 mesh cells occurring in the x-direction of the structure, and a minimum of 3 mesh cells in the y-direction of the structure across the narrowest section, as illustrated in Figure 2.2. The wavelength is calculated with Equation 2.12 where c is the speed of light, f is the maximum simulation frequency of 3 GHz and the effective ϵ_r is 3.5 for the GIL substrate used. From these calculations it is clear that the chosen grid satisfies the mentioned grid density criteria.

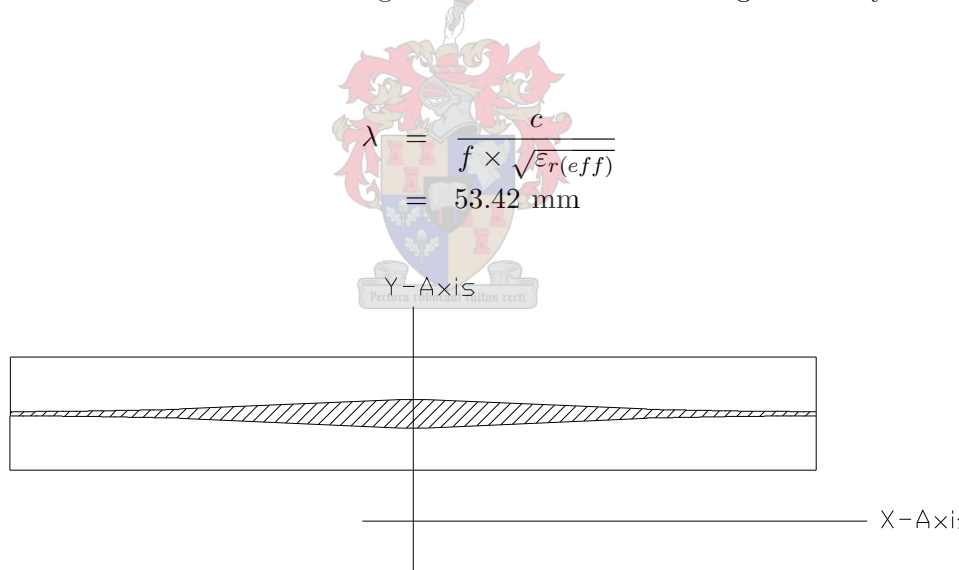
$$\lambda = \frac{c}{f \times \sqrt{\epsilon_r(\text{eff})}} = 53.42 \text{ mm} \quad (2.12)$$


Figure 2.2: The back-to-back 10 Ohm taper structure that was simulated in Microwave Office. This figure is not set to scale.

Figures 2.3 and 2.4 show the modeled and measured input reflection of the taper structure. The trace marked AWR Simulated Taper (Δ marker) is the result of the Microwave Office EM simulation, while the trace marked HP8753C Measured Taper (\diamond marker) is the data of the network analyser measurement. As illustrated in Figure 2.4, the maximum reflection in the simulated and measured data for the back-to-back taper is below -10 dB in the frequency band of interest. The measured and simulated results in Figures 2.3 and 2.4 show tolerable correlation.

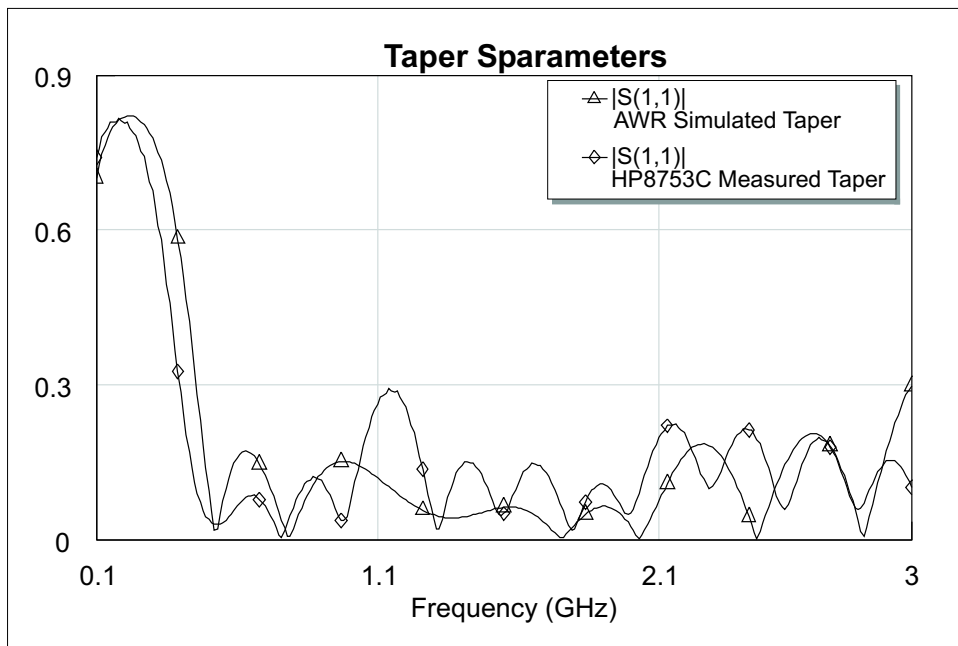


Figure 2.3: A comparison of the simulated and measured input reflection coefficient of a 50 Ohm to 10 Ohm Klopfenstein transformer placed back-to-back. The input reflection is shown on a linear scale.

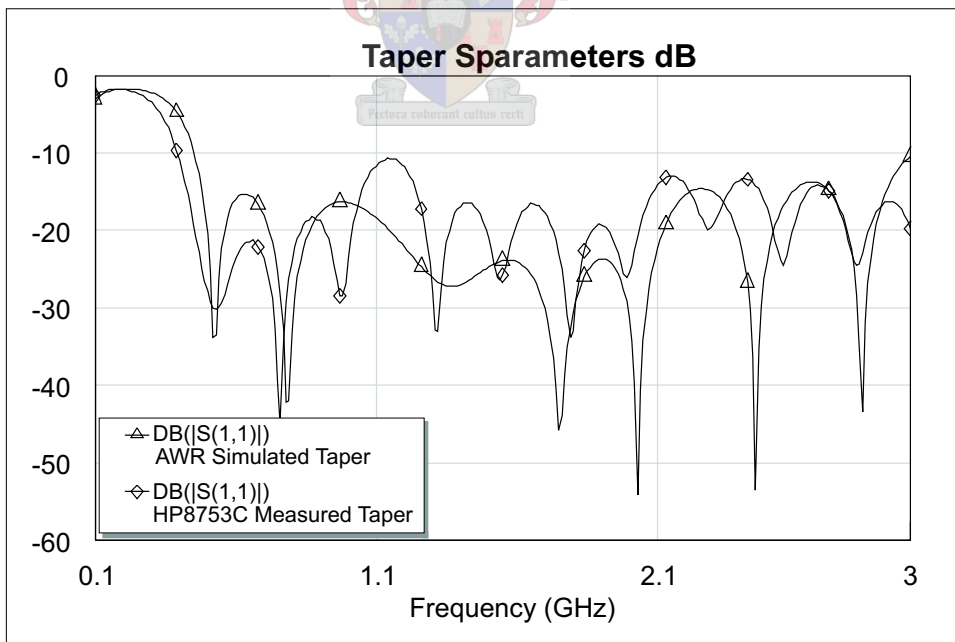


Figure 2.4: A comparison of the simulated and measured input reflection coefficient of a 50 Ohm to 10 Ohm Klopfenstein transformer placed back-to-back. The input reflection is shown on a logarithmic scale.

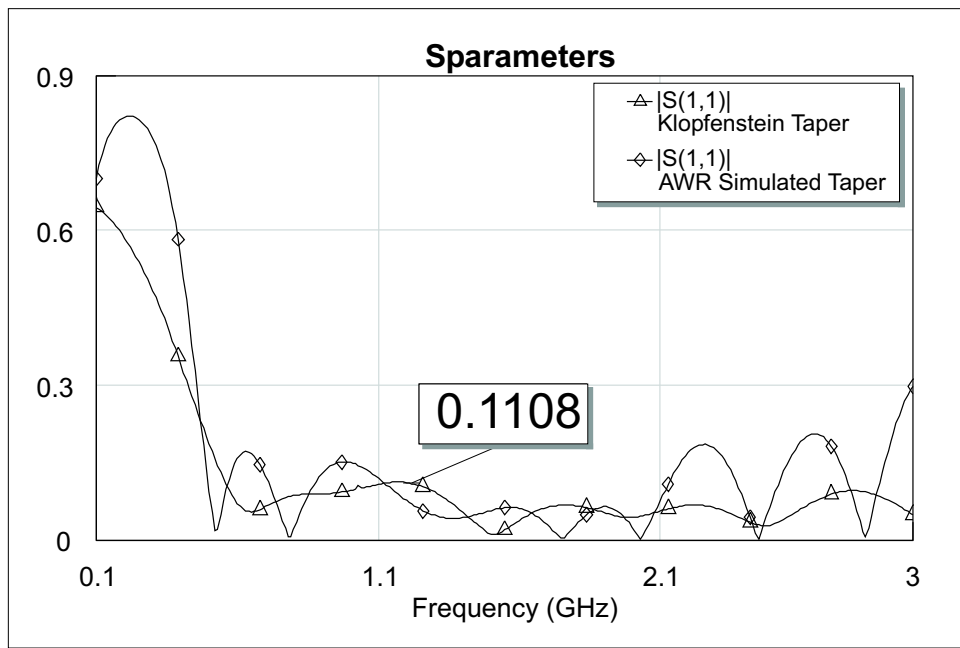


Figure 2.5: A comparison of the simulated input reflection coefficient of a 50 Ohm to 10 Ohm single Klopfenstein transformer and a back-to-back transformer. The input reflection is shown on a linear scale.

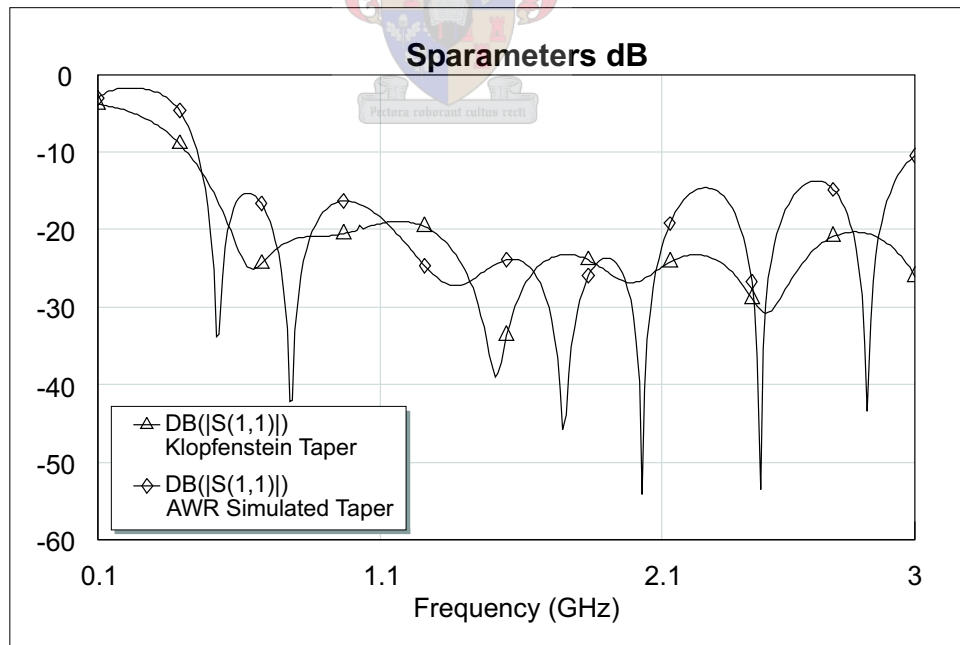


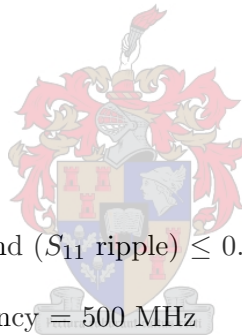
Figure 2.6: A comparison of the simulated input reflection coefficient of a 50 Ohm to 10 Ohm single Klopfenstein transformer and a back-to-back transformer. The input reflection is shown on a logarithmic scale.

The reflection of two tapers placed back-to-back can be as much as double that of a single taper terminated in a 10 Ohm load, as illustrated in Figure 2.5. In Figures 2.5 and 2.6, the trace marked Klopfenstein Taper (Δ marker) is the simulated result of the single taper, while the trace marked AWR Simulated Taper (\diamond marker) is the result of the two tapers back-to-back. The simulated result of the single taper illustrated in Figure 2.5 (trace marked Klopfenstein Taper, Δ marker), compares exceptionally well with the design specifications, with a maximum passband ripple of 0.1108.

2.2.2 5 Ohm Klopfenstein Taper Design Example

A second taper with lower impedance (5 Ohm) was designed. This taper was implemented on the same GIL substrate as before, which means this structure is even larger than in the 10 Ohm case, as illustrated in Figure 2.7. A 5 Ohm Klopfenstein taper with the following specifications was simulated in Microwave Office [13] and compared with the results measured on a vector network analyser [14].

- Input Impedance = 50 Ω
- Output Impedance = 5 Ω
- Maximum Ripple in Passband (S_{11} ripple) ≤ 0.1
- Minimum Operating Frequency = 500 MHz



This taper structure is physically very large, as illustrated in Figure 2.7. This is due to the fact that the output impedance is very low and it was implemented on low ϵ_r substrate. Due to this structure being physically very large, it was divided into 3 smaller sections (Enclosure 1 - 3) to ensure accurate EM simulation results in Microwave Office. The main reason for dividing the structure was computer memory limitations. To overcome this problem the three sections were cascaded in order to obtain the response of the complete structure. The grid of the 5 Ohm taper is calculated using Equation 2.12, as for the 10 Ohm taper. The 5 Ohm taper EM structure simulated in Microwave Office [13] was configured as follows.

- Frequency Range
 - 0.3 GHz to 2.5 GHz in steps of 0.02 GHz
- Enclosure 1
 - Size: 60 mm by 6 mm

- Grid: 120 by 30 divisions
- Cell Size: X = 0.5 mm, Y = 0.2 mm
- Enclosure 2
 - Size: 60 mm by 20 mm
 - Grid: 100 by 50 divisions
 - Cell Size: X = 0.6 mm, Y = 0.4 mm
- Enclosure 3
 - Size: 60 mm by 30 mm
 - Grid: 40 by 40 divisions
 - Cell Size: X = 1 mm, Y = 0.75 mm
- Dielectric Layers (For all the above Enclosures)
 - Layer 1: Air, Thickness = 10 mm, $\epsilon_r = 1$, Loss Tangent = 0
 - Layer 2: Substrate, Thickness = 0.762 mm, $\epsilon_r = 3.86$, Loss Tangent = 0
- Boundaries (For all the above Enclosures)
 - Enclosure Top: Approximately Open
 - Enclosure Bottom: Perfect Conductor

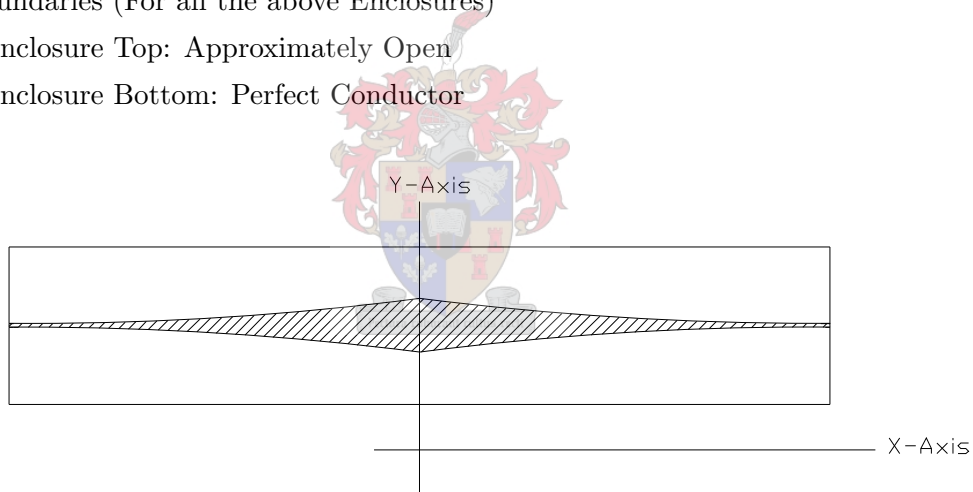


Figure 2.7: The back-to-back 5 Ohm taper structure that was simulated in Microwave Office. This figure is not set to scale.

The result of the EM simulated back-to-back taper is illustrated in Figures 2.8 and 2.9, marked with the trace AWR Simulated Taper (Δ marker). The trace marked Measured Taper (\diamond marker) is the measured result of the back-to-back taper, measured on the network analyser. The measured and simulated results in Figures 2.8 and 2.9 show tolerable correlation. The maximum error between the measured and simulated data for the back-to-back 5 Ohm taper is 3.32 dB, as shown in Figure 2.9. The single taper EM simulated result compared to the Matlab calculated taper is illustrated in Figure 2.10. The trace marked Taper Segments (\diamond marker) is the EM simulated result, comparing exceptionally well with the design specifications, the

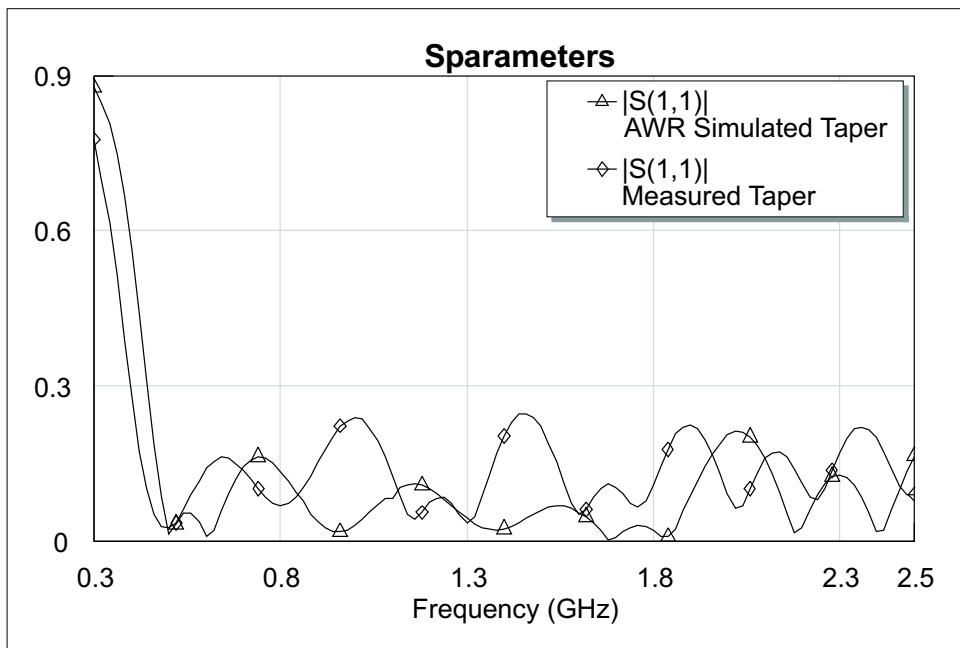


Figure 2.8: A comparison of the simulated and measured input reflection coefficient of a 50 Ohm to 5 Ohm Klopfenstein transformer. The input reflection is shown on a linear scale.

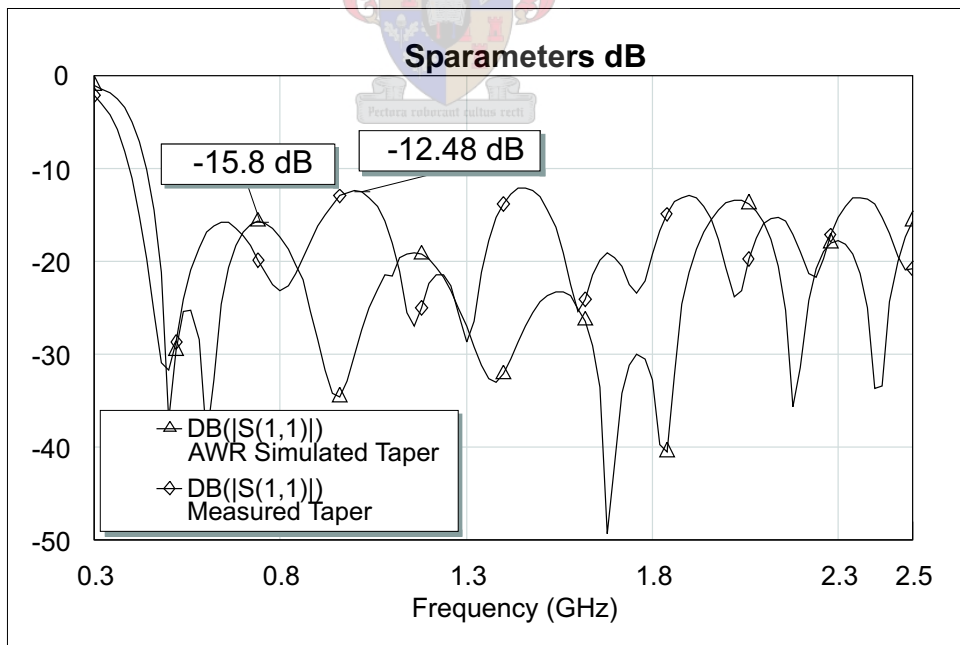


Figure 2.9: A comparison of the simulated and measured input reflection coefficient of a 50 Ohm to 5 Ohm Klopfenstein transformer. The input reflection is shown on a logarithmic scale.

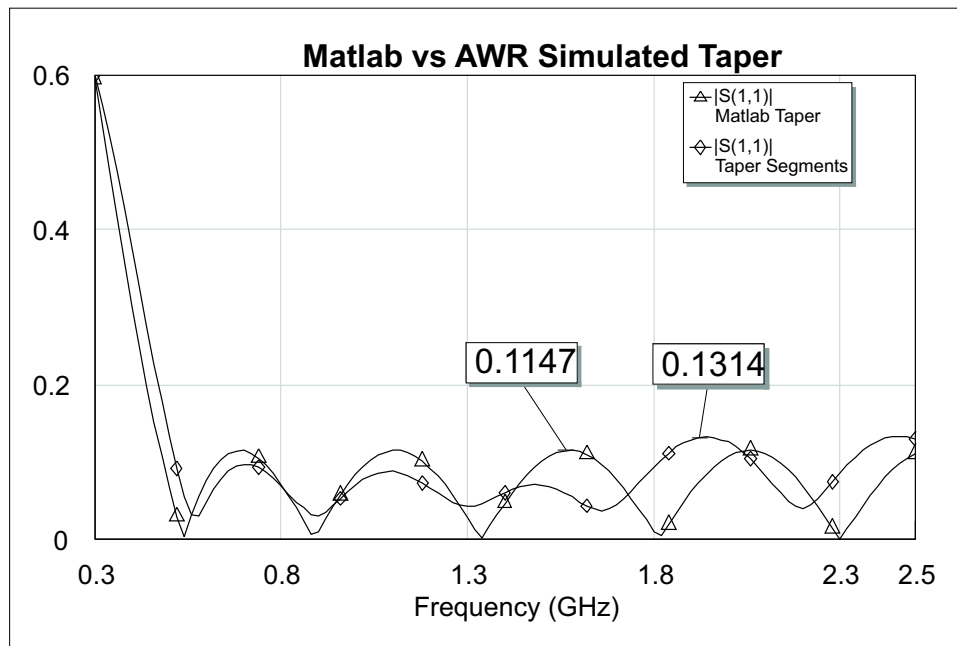


Figure 2.10: A comparison between the single simulated transformer and the Matlab calculated transformer, the input reflection is shown on a linear scale.

trace marked Matlab Taper (Δ marker). The Matlab taper passband ripple is 0.1147, while the simulated passband ripple for the single taper is 0.1314.

2.3 Conclusion

This chapter presented the theory of the design of optimal cascaded transformer arrangements that was extended to the design of continuous transmission line tapers. Also, the characteristic impedance contour for an optimal transmission line taper can be found. This impedance contour can be thought of as the envelope of the pointwise specified characteristic impedance of the cascaded transformer arrangement.

Two taper examples were implemented and measured and acceptable results were obtained. With these taper structures better reflection measurements can be performed in the low impedance environment. The small differences between the Matlab prediction and the Microwave Office simulation obtained might be due to the use of fixed scaling in the calculation of the taper length, as shown in Figure 2.10.

Chapter 3

Advanced Low Impedance TRL Fixture Design

3.1 Introduction

Many devices in today's communications systems are contained in leaded packages without coaxial connectors. Measuring these devices requires a test fixture to connect to coaxial-based test equipment. The lead widths of the package transistors vary with power capability, leading to varying input impedances (typically 1 Ohm to 12 Ohm). The biggest problem is to maintain the accuracy of the low impedance S-parameter measurement and to ensure that the mismatch between the low impedance device and the 50 Ohm measurement environment is as small as possible. A large mismatch leads to the risk that the transistor may start to oscillate and that measurement accuracy is destroyed.

Thick, low ϵ_r substrates are available with which wide 50 Ohm lines could be manufactured to accommodate for the device tabs, but in many applications the system is forced to use a particular substrate with certain substrate parameters, including ϵ_r and height. An HP8510C vector network analyser is used to perform two port S-parameter measurements. The low impedance test fixture's main goal is to compensate for the vector network analyser and the particular substrate, to ensure that the electrical environment in which the transistor is characterised, is as close as possible to the final product's environment.

The main goal of this chapter is the design of a high-quality RF fixture with Thru-Reflect-Line (TRL) calibration standards, providing repeatable and accurate low impedance in-fixture measurements. An advanced low impedance TRL calibration test fixture has been designed to resolve the difficulty of non-50 Ohm calibration used by the vector network analyser. To compensate for the low impedance environment, cascaded transformer arrangements that were

extended into microstrip transmission line tapers were used as pre-matching networks. The pre-matching networks allow the network analyser to measure devices with a low impedance termination.

3.2 A High-Quality Low Impedance TRL Test Fixture Design

It is important to produce a test fixture of high-quality, as this will ensure accurate and repeatable in-fixture measurements. Building a poor fixture and expecting the calibration to compensate for fixture and measurement errors is not a good idea, as measurement repeatability and accuracy will suffer.

The electrical and mechanical challenges of a TRL test fixture should not be under-estimated, as they play a large roll in the repeatability and accuracy of test fixtures. The following electrical and mechanical requirements should be considered when TRL test fixtures are designed. The fixture has to be mechanically stable and the mechanical complexity has to be of a level that will make it easy to use and manufacture. The fixture must be able to provide a high level of calibration accuracy and measurement repeatability. The design must be such that the different measurement configurations required for a TRL calibration and device measurements are to be performed as rapidly as possible. The test fixture design must be flexible in a way that different users, different substrates and different package components can be accommodated. The test fixture must be large enough to accommodate additional components such as bias-T networks, adjustable tuners and pre-matching networks as part of a measurement set up, if they are needed.

The most important electrical problem is that the fixture must be able to deliver the RF signal to the device under test (DUT), in this case converting the signal from a coaxial to a non-coaxial environment [15]. Also, the system reference impedance Z_o (usually 50 Ohms) must be maintained as well as good RF grounding to ensure a good match. Fixtures designed to test non-50-Ohm devices, may need matching elements, in this case a taper to act as a wideband impedance transformer. The Klopfenstein taper concept described in Section 2.2 was utilized to design the pre-matching networks to compensate for the low impedance environment.

Two different low impedance TRL test fixtures were investigated, namely, the split connector test fixture and the split block test fixture. In each of these test fixtures the tapers used are not part of the calibration standards, but merely act as transitions between the 50 Ohm vector network analyser measurement system and the low impedance transmission line standards.

The difference between the two test fixtures are that the split block uses the same two taper structures, with the SMA connectors soldered onto the microstrip lines to improve the coaxial to microstrip transition, while the split connector uses different taper structures in each calibration measurement. Another difference is that the split block fixture's discontinuity is situated at the low impedance calibration standards, while the discontinuity in the split connector fixture is positioned at the SMA connectors. The split block fixture presents manufacturing challenges, such as the same height of all parts (calibration standard blocks and the split blocks) used and the alignment of microstrip lines. The split connector fixture challenges the users measurement ability, with the placement of the SMA connector that has to be the same in each measurement to keep the discontinuity as small as possible. These two different sets of calibration standards are illustrated in Figures 3.13 and 3.19.

3.2.1 50 Ohm Split Connector TRL Fixture

The split connector TRL test fixtures idea was imitated from Inter-Continental Microwave [16]. This concept has not been implemented before and it was decided to test this technique with 50 Ohm TRL calibration standards before implementing it in the low impedance environment.

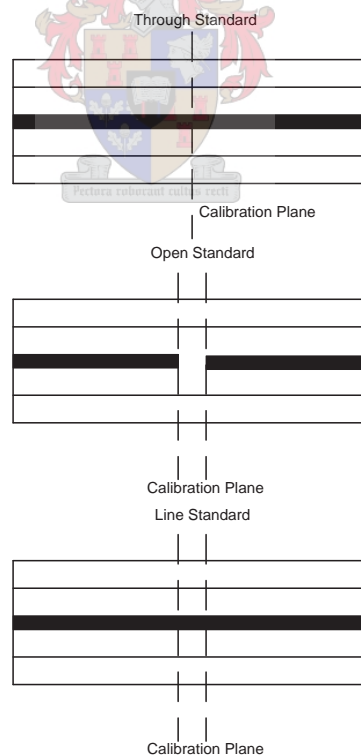


Figure 3.1: The layout of the split connector 50 Ohm TRL calibrations standards implemented in microstrip transmission lines (this figure is not set to scale).

This test fixture was designed to have a highly flexible and re-usable base structure to provide a test platform to perform multiple microwave S-parameter measurements and to accommodate different users. RF-Launchers, adjustable in 3-dimensions, were used to accommodate different midsections and different substrate thicknesses. The concept of having a mainframe with plug-in type midsections makes it a very adaptable and cost effective solution. This test fixtures flexible design concept can handle custom requirements and future expansions. The split connector test fixture was firstly designed in the 50 Ohm environment before it was implemented into the low impedance environment. The 50 Ohm TRL calibration standards were implemented on the following substrate:

- Taconic TLY-5A High Frequency Laminate
- $\epsilon_r = 2.54$
- Height = 0.508 mm
- Tan $\delta = 0.0009$

This calibration kit consists of a zero-length through, open reflection and two line standards with which a calibration from 500 MHz up to 18 GHz could be performed. After the full two-port calibration was performed each of the calibration standards was re-measured to obtain the self-consistency measurements. These measurements are illustrated in Figures 3.2 to 3.6.

The through reflection is measured to be better than -40 dB over the calibrated frequency band, while the measured through phase variation is 0.6° over the calibrated frequency band. The trace marked ThruC (Δ marker) are the through measurements measured directly after the calibration was performed, and do not account for test fixture's mechanical variations. The trace marked ThruM (\square marker) are the through measurements accounting for mechanical variations. Mechanical variations are obtained when the standard being measured is removed from the fixture and placed back and re-measured. The through reflection and phase measurements are illustrated in Figures 3.2 and 3.3 respectively.

The open standards input and output reflections are as expected, on the open side of the Smith chart (50 Ohm chart), as illustrated in Figure 3.4. The line standards phase measurements correlate very well with their ideal simulated results. The Microwave Office simulated microstrip phase, the trace marked Microstrip Line1 (\square marker), compares very well with the measured phase, the trace marked Line1 (Δ marker) as illustrated in Figure 3.5. This correlation is also noticed for line 2 in Figure 3.6. The maximum deviation of the phase response between measured and simulated data is 2° . This deviation can be related to variations in the substrates dielectric constant.

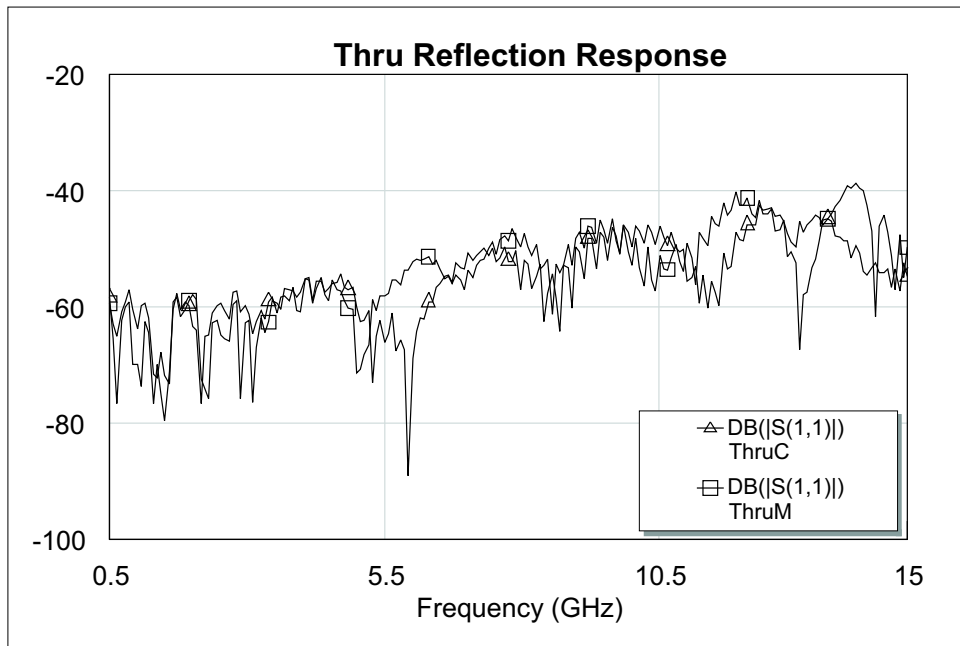


Figure 3.2: The through standards reflection response measured after a TRL calibration was performed. A reflection of -40 dB over the frequency band are measured.

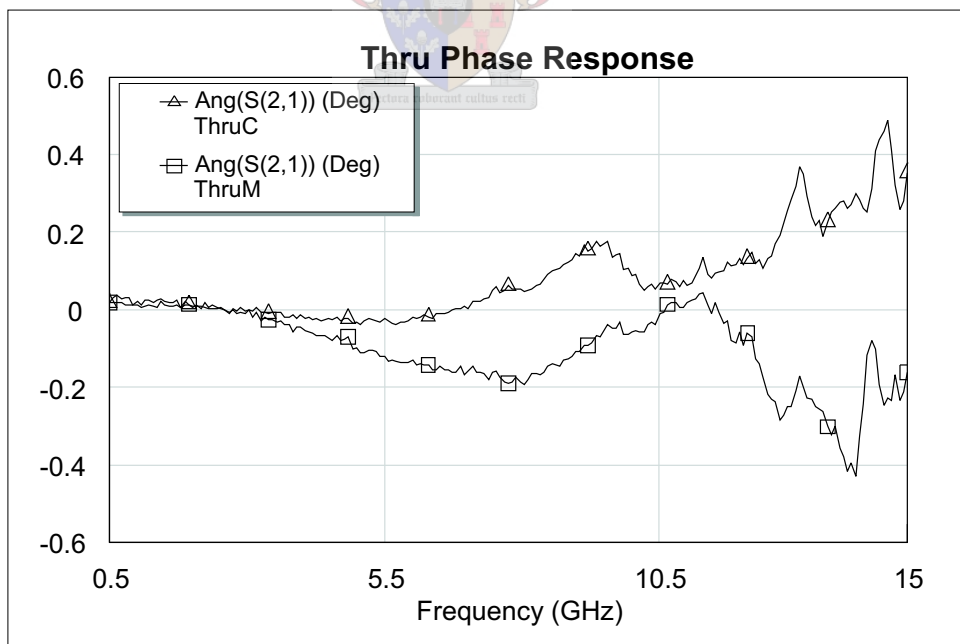


Figure 3.3: The through standards phase response measured after a TRL calibration was performed. A phase error of less than 0.6° is measured over the calibrated band.

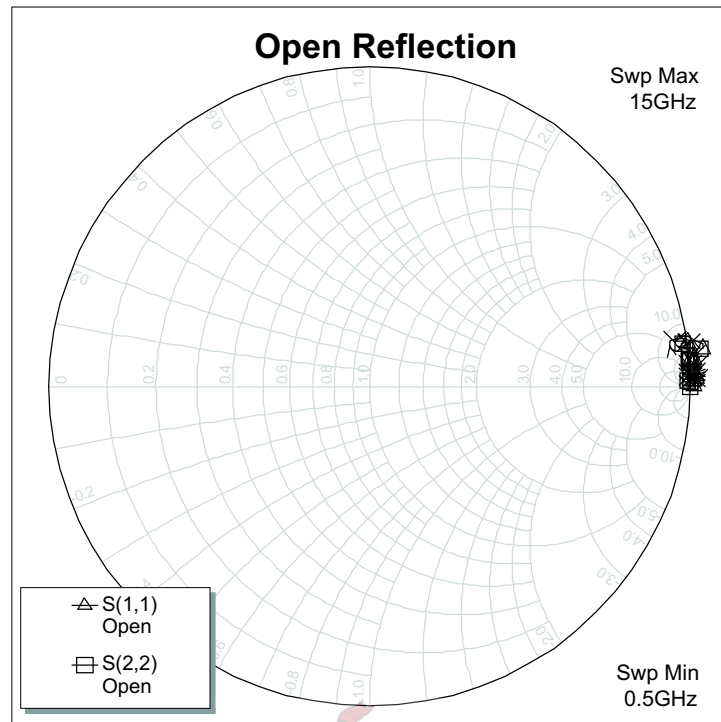


Figure 3.4: The open standards input and output reflections measured on a 50 Ohm Smith chart.

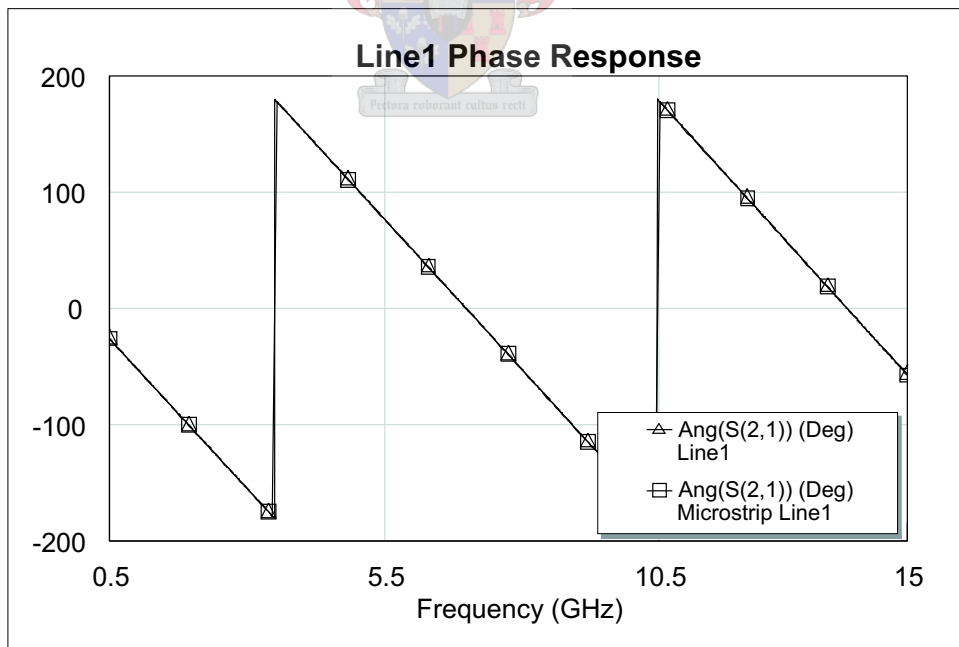


Figure 3.5: A comparison between the measured phase response, the trace marked Line1 (△ marker), and the MWO (ideal) simulated phase response, the trace marked Microstrip Line1 (□ marker), of the line 1 standard.

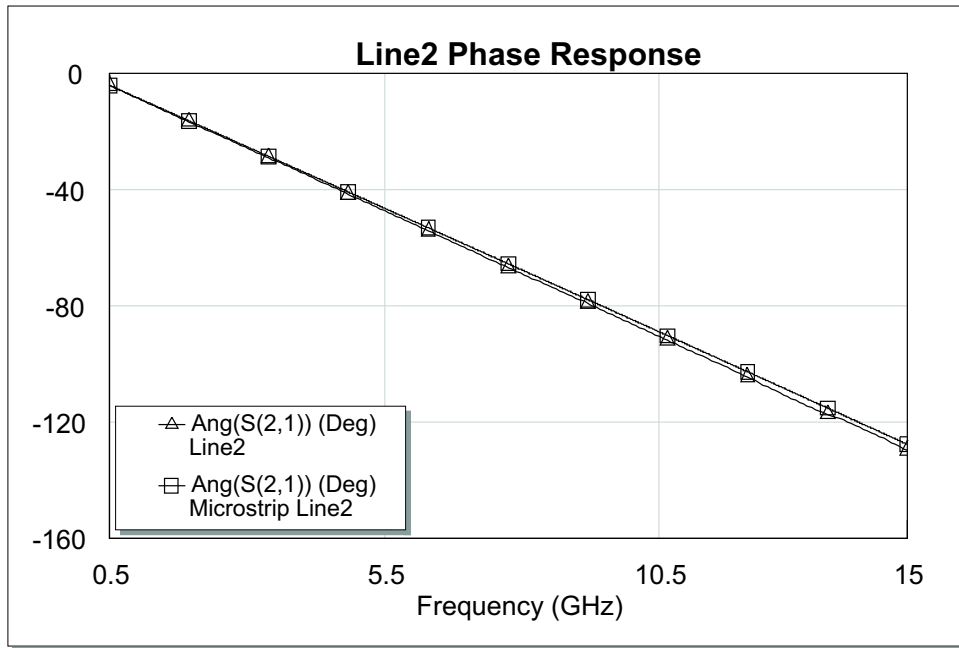


Figure 3.6: A comparison between the measured phase response, the trace marked Line2 (\triangle marker), and the MWO (ideal) simulated phase response, the trace marked Microstrip Line2 (\square marker), of the line 2 standard.

This split connector TRL test fixture and calibration kit was used to measure the S-parameters of a 1-Watt Fujitsu FLL101ME power GaAs FET transistor. These S-parameters were used to design a maximum gain (conjugate match) amplifier. This amplifier also had to be unconditionally stable. For a conjugate matched amplifier, maximum power transfer from the input and output matching networks to the transistor will occur when the following two equations are satisfied,

$$\begin{aligned}\Gamma_{\text{in}} &= \Gamma_S^* \\ \Gamma_{\text{out}} &= \Gamma_L^*\end{aligned}\quad (3.1)$$

where Γ_{in} and Γ_{out} are the reflection coefficients looking into the gate and drain of the transistor and Γ_S and Γ_L are the reflection coefficients looking toward the source and load [9]. The conjugate matched amplifier was implemented on the following substrate:

- Rogers High Frequency Laminates 6010.2
- $\epsilon_r = 10.2$
- Height = 0.635 mm

- $\text{Tan } \delta = 0.0023$

The amplifier was designed to be located at a center frequency of 1.3 GHz with a 10% bandwidth. The amplifiers simulated and measured input, and output reflections and gain are illustrated in Figures 3.7 and 3.8. The measured results are shifted compared to the simulated results. The simulated models for the dc-blocking capacitors and stabilising resistor, that was used in the RF path, was not very accurate. More complex and accurate high frequency models contain parasitic inductance. The inductance for each component in the RF path was fine-tuned to obtain a better match, as shown in Figure 3.9. These models should have contained a series inductance of 0.8 nH each.

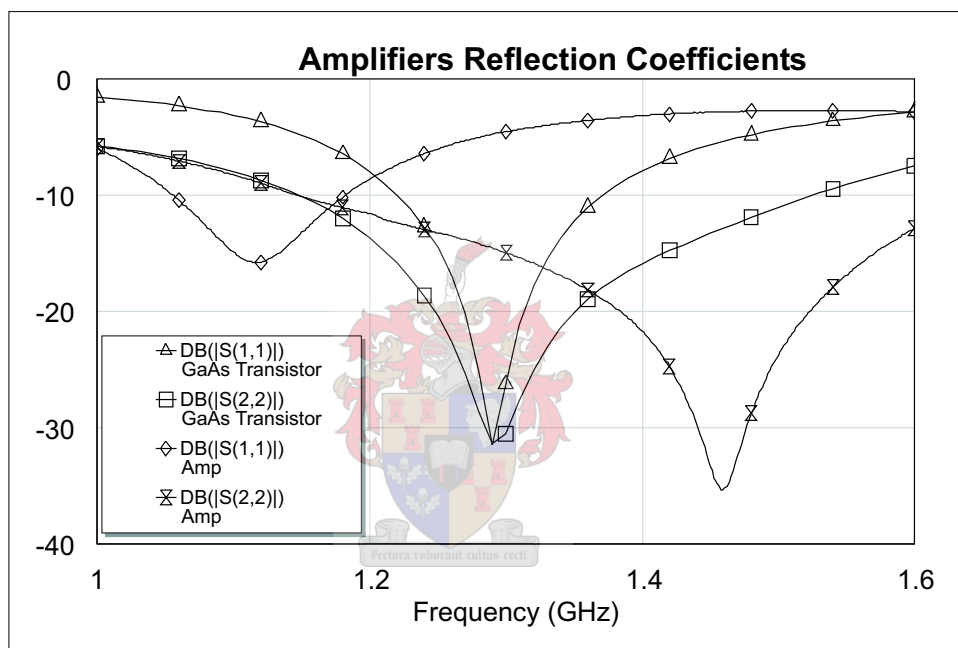


Figure 3.7: A comparison between the measured input and output reflection responses, the traces marked Amp (\diamond and ∇ marker), and the MWO (ideal) simulated input and output reflection responses, the traces marked GaAs Transistor (\triangle and \square marker), of the conjugate test amplifier circuit.

The maximum gain amplifier designed with the S-parameters measured with the 50 Ohm split connector TRL test fixture, illustrates that the operation of the fixture is acceptable. This TRL technique can be used to design different TRL test fixtures.

3.2.2 Low impedance Split Connector TRL Fixture

The measurements obtained from the 50 Ohm split connector TRL test fixture was acceptable. The overall mechanical operation and flexibility of the test fixture was found to be user

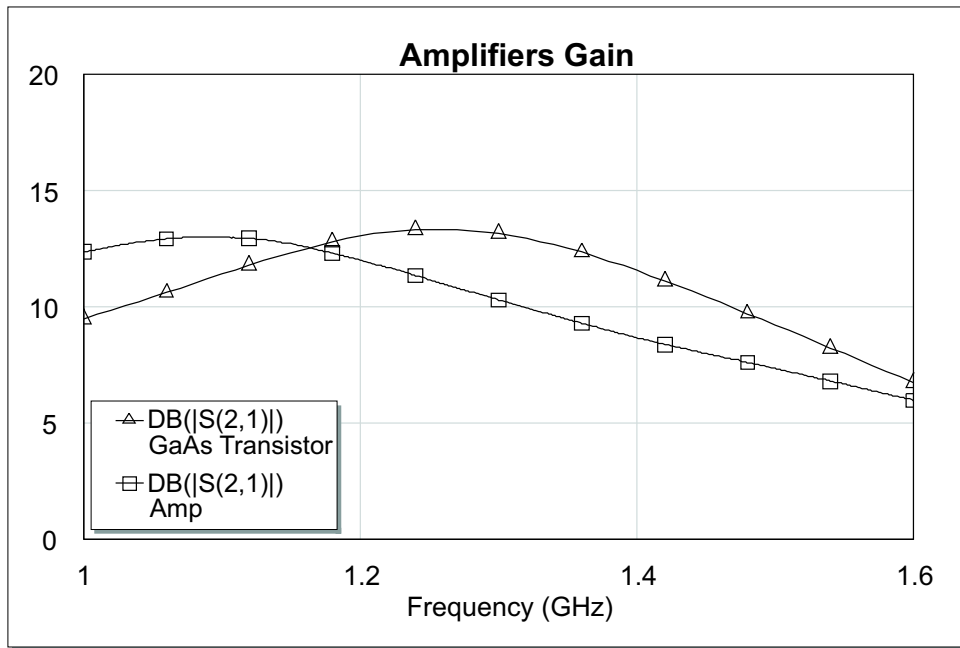


Figure 3.8: A comparison between the measured gain response, the trace marked Amp (\square marker), and the MWO (ideal) simulated gain response, the trace marked GaAs Transistor (\triangle marker), of the conjugate test amplifier circuit.

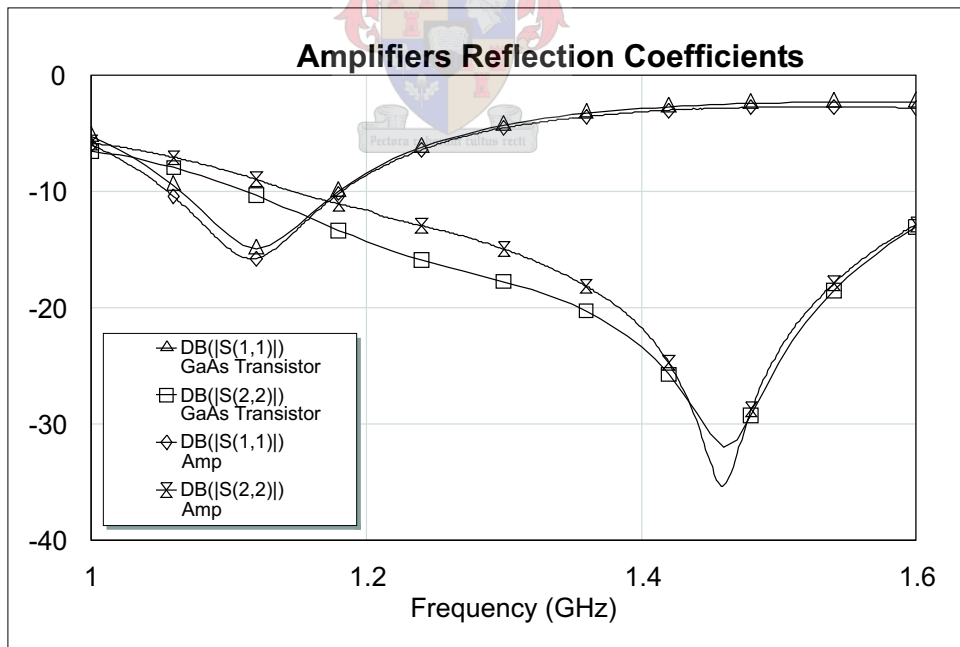


Figure 3.9: A comparison between the measured input and output reflection responses, the traces marked Amp (\diamond and ∇ marker), and the MWO (fine-tuned) simulated input and output reflection responses, the traces marked GaAs Transistor (\triangle and \square marker), of the conjugate test amplifier circuit.

friendly. Thus, it was decided to implement the low impedance TRL calibration standards in the split connector TRL test fixtures environment. These low impedance calibration standards are illustrated in Figure 3.13, and the following points outline some of the test fixtures design obstacles.

- **The RF-Launchers/SMA Connector Holders**

One of the most challenging aspects of test fixture design is the transition occurring at the RF-Launcher or SMA connector holder. This is where the first discontinuity in the RF path occurs because of the coaxial to microstrip line transition. This discontinuity occurs typically because the RF signal is converted from a radial E-field to a planar E-field and the diameter of the center pin is not exactly the same as the width of the microstrip line, causing fringing capacitance [15]. The constraint that has to be taken into account is the particular substrate used, because this determines the width of the microstrip line being connected to. In this test fixture setup the center pin diameter of the SMA connector used is 1.25 mm while the microstrip line width is 0.58 mm. SMA connectors with smaller pins are available, but each time the pin is placed on the microstrip line, it cuts through the line and damages it. The SMA connector holder, illustrated in Figure 3.10, provides a 3-dimensional way of alignment to ensure that a suitable RF contact is established to the microstrip lines. Spirt-levels are mounted on the connectors to assist with the alignment and to ensure consistent repeatability.

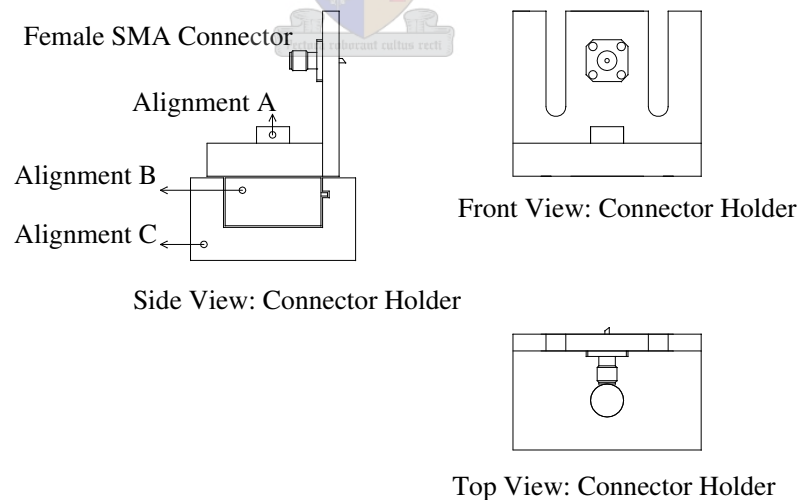


Figure 3.10: The SMA connector holder providing a 3-dimensional alignment. This connector can be aligned up or down (via Alignment A), right to left (via Alignment B), forwards and backwards (via Alignment C).

- **The Measurement Cables**

The test cables used between the network analyser and the fixture are very important. They should exhibit low loss over the required frequency range and the amplitude, phase and thermal stability of the cables should be good to ensure repeatable measurements [15]. Cable straighteners, illustrated in Figure 3.11, were used to assist with cable stability. Loops in the cable can be added to allow for some variation in the test fixture setup if multiple fixtures with different lengths are measured. This minimizes mechanical movement in test cables during the different calibration and device measurements.

A 1 m cable made by Times Microwave with the following properties has been used with this fixture:

- TFlex-405
- Impedance = 50 ± 1 -ohm
- Operating Frequency 0.05 to 18 GHz
- Dielectric (PTFE) = 1.63
- Capacitance = 96.1 pF/m
- Loss of Cable = 3.48 dB/m @ 18 GHz

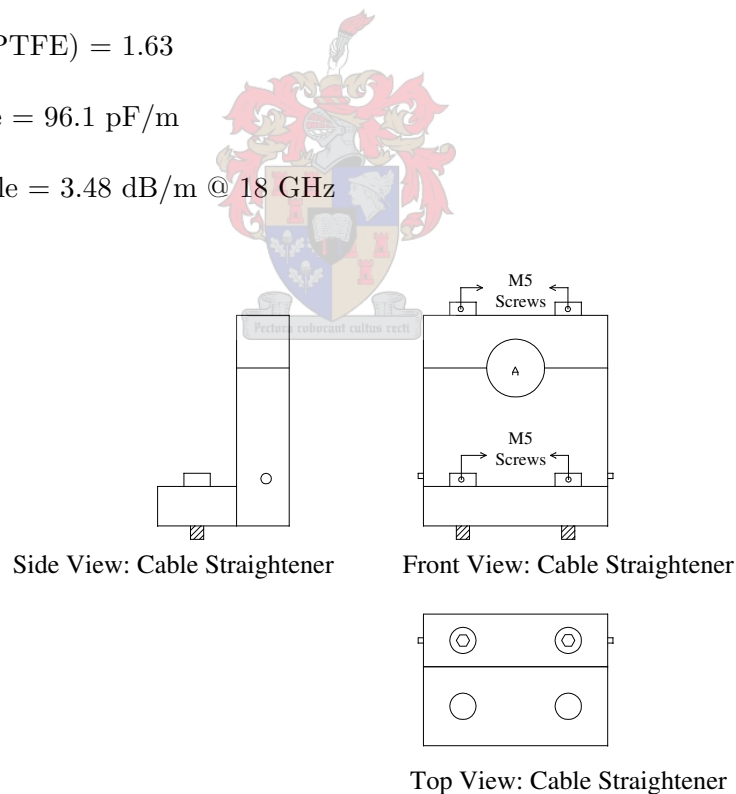


Figure 3.11: The cable straightener providing cable stability. The cable hole A is large enough for the use of a wide range of cable sizes.

- **The DUT Fixture**

Providing a good electrical contact to the DUT is another important aspect of fixture design [15]. The main idea is to manufacture a non-destructive fixture with a pressure mechanism so that many different parts can be measured with ease. Soldering parts into the fixture is not a viable option because it would prevent the DUT (such as a transistor) that is being characterised, from being re-used in an application circuit. For measuring these devices a DUT fixture is manufactured with a clamp, illustrated in Figure 3.12. The clamp operates as a release mechanism that pops the DUT out of the fixture, making for easy retrieval after the part is tested. With this clamp controlled, consistent pressure can be applied to the device that is being characterised. Consistent pressure is important since contact resistance between the DUT and the fixture can vary with pressure.

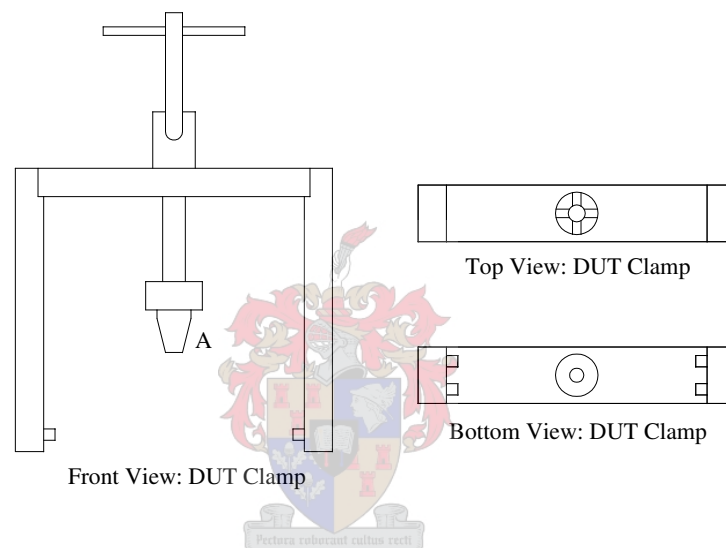


Figure 3.12: The DUT clamp providing enough pressure to the DUT for repeatable measurements. The pressure point A is replaceable for measuring various devices with the same clamp.

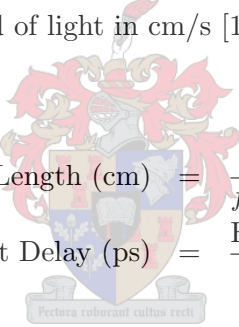
3.2.3 Split Connector Low Impedance TRL Calibration Standards Design

For many microstrip device measurements, TRL is a viable calibration technique that utilizes simple and available in-fixture calibration standards. The main advantage of TRL is that the calibration standards are relatively easy to make and define. The following substrate from Rogers was used to implement the TRL taper standards. This is the same substrate that is to be used in the final application, and is used to ensure that the test fixtures electrical environment is as close as possible to the final products environment.

- Rogers RT/duroid 6010.2 High Frequency Laminate

- $\epsilon_r = 10.2$
- Height = 0.635 mm
- Tan $\delta = 0.0023$

An open standard was used as the reflect standard. The open standard was purely chosen on the basis that this standard could be fabricated more accurately than a short standard. To reduce the measurement uncertainty, the insertion phase between the through and delay line are 20° for the lower frequency and 160° for the upper frequency. The only drawback is that the transmission-lines can only be used over an 8:1 bandwidth, thus two transmission line standards are used to calibrate up to 18 GHz (the maximum frequency of the HP8510C vector network analyser) [17]. The calibration kit was designed up to 18 GHz to measure the maximum operating frequency of the low impedance calibration standards. The delay of each standard can be computed with Equation 3.2, where the electrical length is in cm, the offset delay is in pico seconds, f_1 is the start frequency of the line standard, f_2 is the stop frequency of the line standard in GHz and c is the speed of light in cm/s [14].



$$\begin{aligned} \text{Electrical Length (cm)} &= \frac{15}{f_1 + f_2} \\ \text{Offset Delay (ps)} &= \frac{\text{Electrical Length}}{c} \end{aligned} \quad (3.2)$$

The line standards length specifications for a TRL calibration is not a critical parameter as the length is never explicitly used during the calibration calculations. A zero length through was used in this case, thus the transmission line standard delays calculated using Equation 3.2 are:

- through Delay = 0 ps
- Line1 Delay = 151.62 ps (Physical length = 16 mm at $f = 1.15$ GHz)
- Line2 Delay = 27.05 ps (Physical length = 2.6 mm at $f = 6.75$ GHz)

A standard definition table, as shown in Table 3.1, list all the parameters that are used by the HP8510C vector network analyser to specify the mathematical model for the TRL line standards calculated above [18].

Figure 3.13 illustrates the layout of the cascaded transformer tapers used to implement the TRL taper standards. This fixture design can incorporate a traditional two lead RF power transistor.

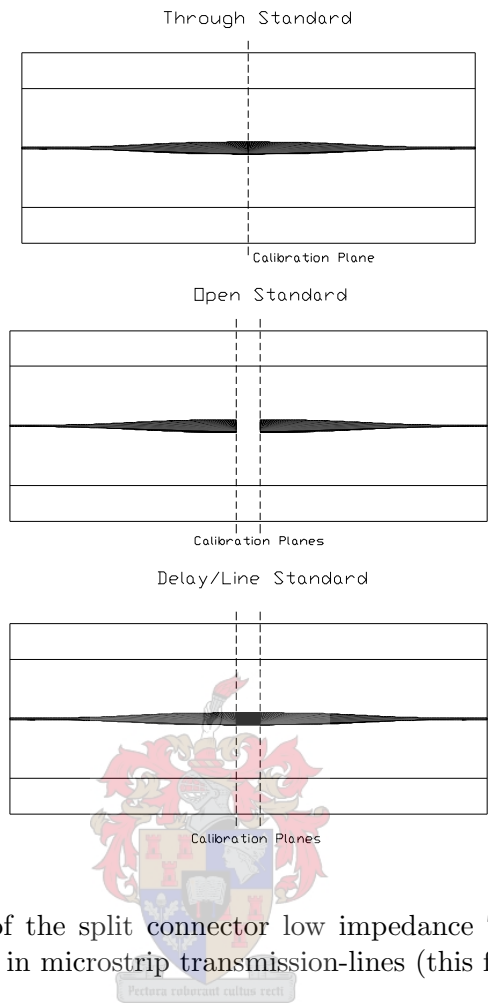


Figure 3.13: The layout of the split connector low impedance TRL calibration standards implemented in microstrip transmission-lines (this figure is not set to scale).

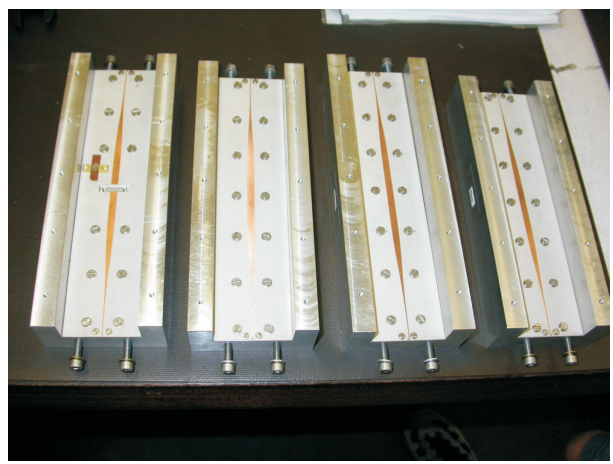


Figure 3.14: A photo representation of the split connector TRL standards. From left to right are the open, line 2, line 1 and the through standards.

No.	Type	L_o	L_1	L_2	L_3	Delay (ps)	Z_o Ω	Loss $G\Omega/s$	Min. Freq. (GHz)	Max. Freq. (GHz)	STD Label
14	Delay					0	12	0	0	999	through
15	Delay					151.62	12	0	0.5	2.8	Line1
16	Delay					27.05	12	0	2.5	16	Line2
18	Open	0	0	0	0	0	12	0	0	999	Open

Table 3.1: Standard definitions table for the TRL standards used on a HP8510C vector network analyser used to perform a full two-port calibration.

After performing a full two-port TRL calibration, the calibration plane is in the center of the through standard and at the end of the open standard as illustrated in Figure 3.13. After the calibration, each of these calibration standards are remeasured to obtain the self-consistency test measurements. The self-consistency test is not a formal calibration verification, it merely provides confidence in the calibration setup. A formal calibration is when a microstrip standard, for which the response is known, is measured after the calibration to verify the particular calibration setup [19, 20]. By using verification standards it is possible to quantify the accuracy and uncertainty of the calibration. The self-consistency test measurements should satisfy the requirements of TRL standards implemented in the microstrip environment, as listed in Table 3.2.

Standard Type	Requirement
through (Zero Length)	$S_{21} = S_{12} = 1 \angle 0^\circ, S_{11} = S_{22} = 0$
Reflect	Open Standards Phase $0^\circ \pm 90^\circ$
Lines	Phase difference between through and Line = 20° to 160°

Table 3.2: Requirements for microstrip TRL standards used on the HP8510C vector network analyser.

From all the phase responses of the standards measured is it noticeable that the data above 10 GHz are inadequate. The maximum operating frequency for microstrip lines can be calculated with the following equation [21, 22].

$$f_c = \frac{300}{\sqrt{\epsilon_{r,eff}}(2W + 0.8h)} \quad (3.3)$$

In this case $\epsilon_{r,eff} = 8.6$, $W = 5.05$ mm, $h = 0.635$ mm, thus using Equation 3.3, the maximum operating frequency is calculated to be 8.855 GHz. The calibration verification results up to the maximum operating frequency are as expected, except for the phase of line 2, as shown in Figure 3.18. At 10.5 GHz the simulated microstrip phase, the trace marked Microstrip Line2

(□ marker), is -100° while the measured phase, the trace marked Measured Line2 (\triangle marker), is -158° . This difference means that line 2 is electrically longer (physical length of 4.1 mm, 1.5 mm longer) than expected. If the substrate ϵ_r is varied in the Microwave Office environment, an ϵ_r of 20 is required before the measured and simulated phase response for line 2 correlates.

It is also presumed that the transmission lines used as calibration standards have identical dispersion characteristics, i.e. identical height, width and relative dielectric constant. However, when measurement results are compared to Microwave Office simulated results, illustrated in Figures 3.17 and 3.18, dispersion is noticeable. Dispersion occurs when a transmission medium exhibits a variable propagation or phase velocity as a function of frequency [17]. The result of dispersion is a non-linear phase shift versus frequency, as seen in Figure 3.18 for the line 2 standard. One of the possible explanations for the phenomenon seen in Figure 3.18, is that each of the four calibration standards used (through, line 1, line 2 and reflect) in the calibration has its own set of tapers. These tapers widths may differ from each other because of the fact that it is very large structures which complicates the production accuracy. Thus, the assumption of identical taper structures used in the calibration falls away. It is clearly seen from the measured phase results of the line 2 standard that the reference plane of the calibration is shifted.

It was noticed that the reflection standards self-consistency test measurement did not satisfy the reflection standards requirement as described in Table 3.2. This is because the open-ended lines are very wide and radiate at these high frequencies.

The phase measurement of line 2, as shown in Figure 3.18, indicates that the line standard has a different length. This deviation in line length means that the calibration plane is shifted. When the calibration plane is not positioned as expected, an unfit calibration is presumed. Possible explanations for this unfit calibration kit can be the result of bad repeatability in the SMA connector's mechanical or electrical contact. Another possible explanation could be the manufactured repeatability of the tapers. These errors provides the motivation for designing a second TRL fixture as describe in paragraph 3.2.4.

3.2.4 Split Block TRL Fixture

The implementation of the split block is more traditional than the split connector and has proved to provide good results in the past. The main difference between this test fixture and the split connector is that the fixture uses the same taper structures in each calibration measurement. The calibration standards are placed between the low impedance taper structures and are not fixed in the taper structure as in the split connector case. The difference between these two test fixtures are illustrated in Figures 3.13 and 3.19. The following outline the design steps of the

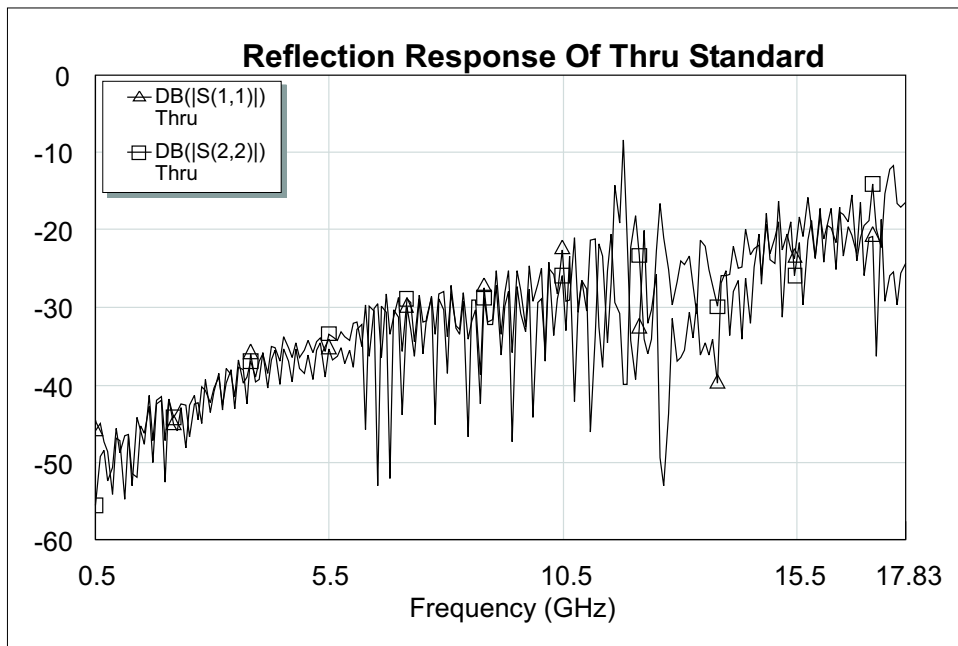


Figure 3.15: The through standards reflection response measured after TRL calibration was performed. A reflection better than -20 dB at 10.5 GHz are measured for both S_{11} and S_{22} . The reflection is illustrated on a logarithmic scale.

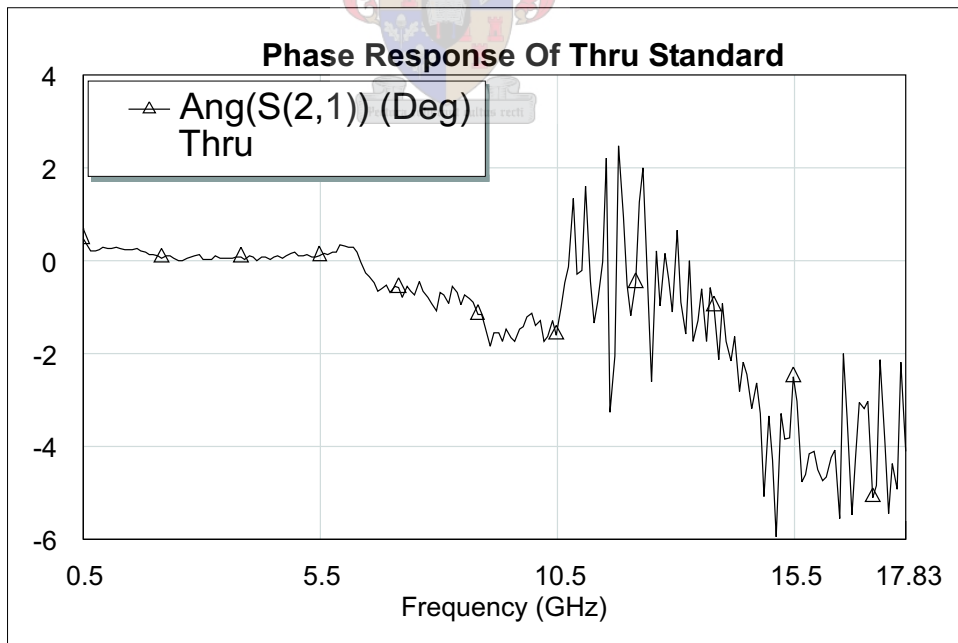


Figure 3.16: The through standards phase response measured after TRL calibration was performed. An phase error of less than 2° at 10.5 GHz are measured for the through standard.

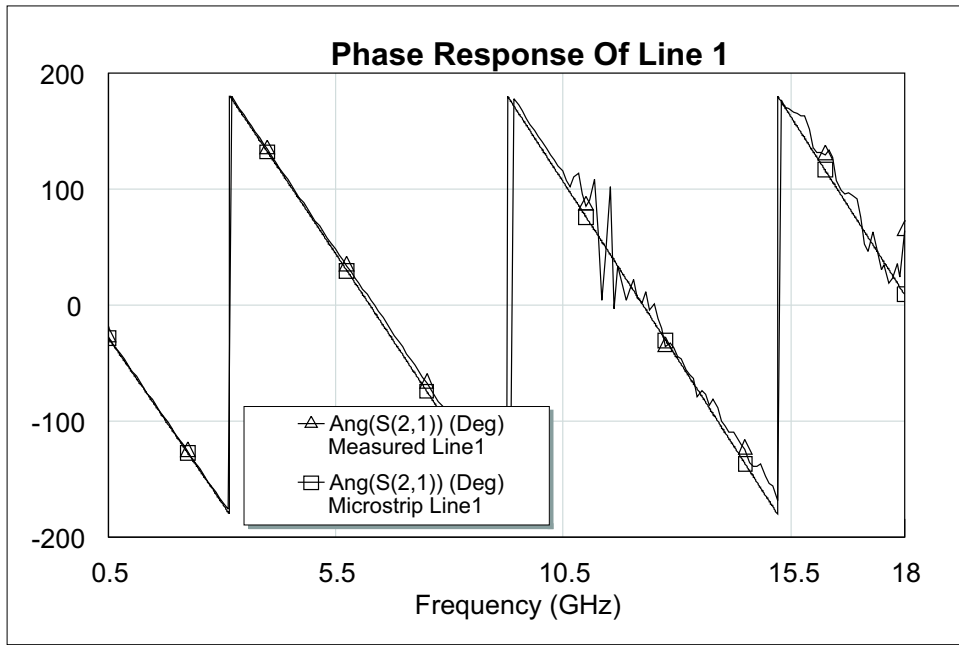


Figure 3.17: A comparison between the measured phase response, the trace marked Measured Line1 (Δ marker), and MWO (ideal) simulated phase response, the trace marked Microstrip Line1 (\square marker), of the line 1 standard.

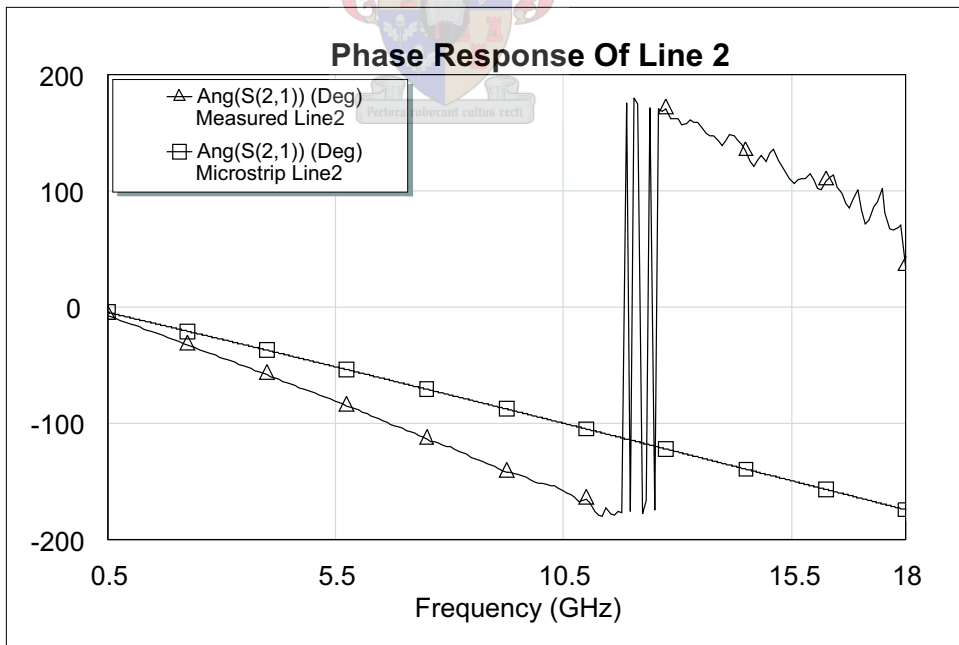


Figure 3.18: A comparison between the measured phase response, the trace marked Measured Line2 (Δ marker), and MWO (ideal) simulated phase response, the trace marked Microstrip Line2 (\square marker), of the line 2 standard.

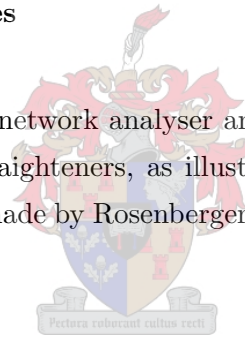
split block TRL test fixture.

- **The SMA Connectors**

In this calibration kit one set of SMA connectors and taper structures was used in all the calibration steps. One of the main differences between the split connector and split block test fixture is that for the split block the SMA connectors were soldered onto the substrate. The second difference is that in this test fixture set up, the center pin diameter of the SMA connector used is 0.47 mm while the microstrip line width is 0.58 mm. The transition from the co-axial to the microstrip environment should be improved with this because the connector pin is smaller than the transmission-line, which will decrease the fringing capacitance. The soldering of the connector pin onto the transmission-line would further improve the fixtures accuracy because this transition is now exactly the same in all calibration measurements.

- **The Measurement Cables**

The test cables used between the network analyser and this calibration fixture differs from the cables previously used. Cable straighteners, as illustrated in Figure 3.11, were used to assist with cable stability. A 1 m cable made by Rosenberger Micro-Coax with the following properties was used:



- UFA 210B
- Impedance = 50 ± 1 -ohm
- Operating Frequency 0.05 to 26.5 GHz
- Capacitance = 86 pF/m
- Loss of Cable = 2 dB/m @ 26.5 GHz
- Phase stability = 2° @ 26.5 GHz
- Velocity of propagation = 77 %

This cable's specifications are better than the Times Microwave cable and was used to further improve measurement accuracy and repeatability.

- **The DUT Fixture**

The split block fixture works on the principle that each standard (through, reflect and line) is placed between two microstrip taper pre-matching blocks. A discontinuity occurs at the junction between the pre-matching networks and the calibration standards. The position of the calibration plane and this junction is not identical. To improve the calibration, the microstrip junction's discontinuity is absorbed in the calibration. To ensure good repeatability and electrical contact between the taper pre-matching networks and the DUT, which can be the through, reflect or line standard, the DUT clamp (illustrated in Figure 3.12) is used. The pressure point A together with a small piece of copper is each time replaced with the appropriate mechanism to ensure good electrical contact between the microstrip taper pre-matching network and the DUT.

3.2.5 Split Block Low Impedance TRL Calibration Standards Design

The microstrip TRL calibration standards were implemented on the same substrate (Rogers 6010.2) as the split connector test fixture. An open standard was again used as the reflection standard but the line standard lengths differ from the previous kit. With these line standards, a calibration up to 8 GHz can be performed. The calibration standard offset delays are calculated with Equation 3.2 and are:

- Through Delay = 0 ps
- Line1 Delay = 125.08 ps (Physical length = 12.7 mm at $f = 1.5$ GHz)
- Line2 Delay = 45.5 ps (Physical length = 4.3 mm at $f = 2.5$ GHz)

A standard definition table, see Table 3.3, list all the parameters that are used by the HP8510C vector network analyser to specify the mathematical model for the in-fixture TRL taper standards calculated above [18].

No.	Type	L_o	L_1	L_2	L_3	Delay (ps)	Z_o Ω	Loss $G\Omega/s$	Min. Freq. (GHz)	Max. Freq. (GHz)	STD Label
14	Delay					0	12	0	0	999	through
15	Delay					125	12	0	0.5	3.5	Line1
16	Delay					45.5	12	0	3	8	Line2
18	Open	0	0	0	0	0	12	0	0	999	Open

Table 3.3: Standard definitions table for the in-fixture TRL standards used on a HP8510C vector network analyser used to perform a full two-port calibration.

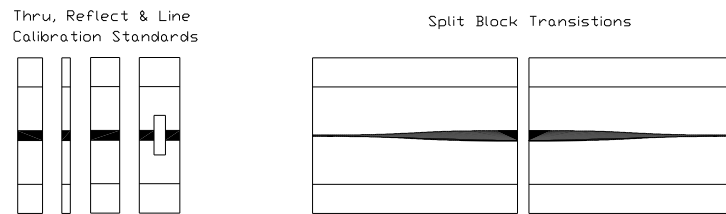


Figure 3.19: The layout of the split block low impedance TRL calibration standards implemented in microstrip transmission-lines (this figure is not set to scale).

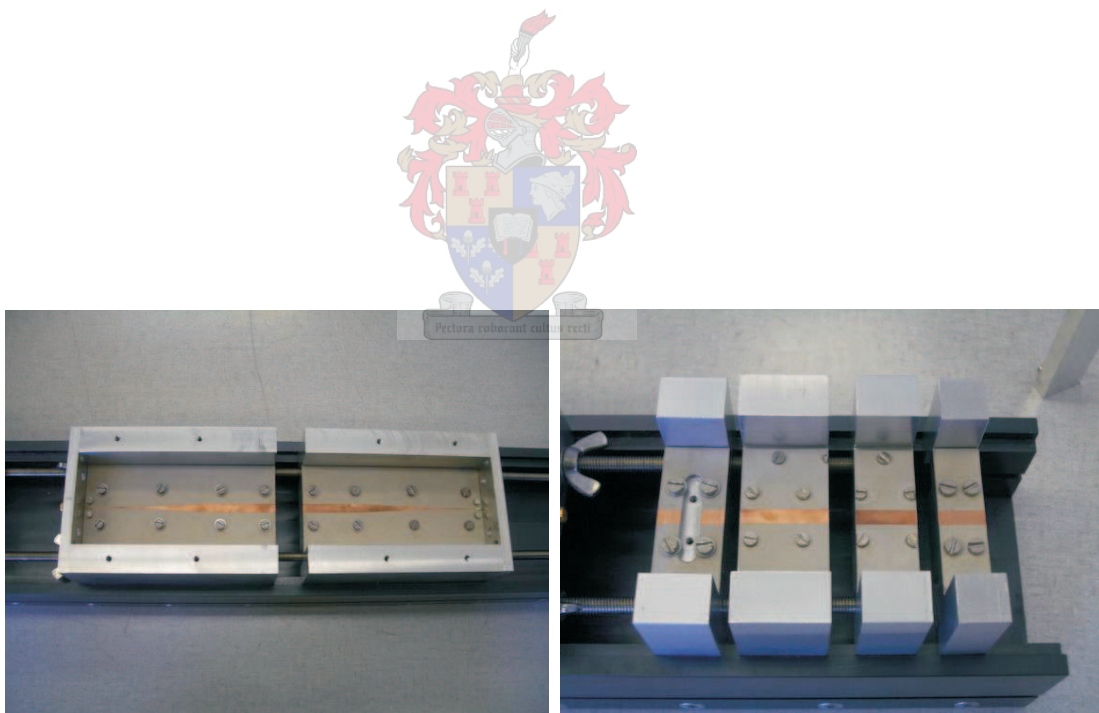


Figure 3.20: A photo representation of the split block and the TRL standards. From left to right are the open, line 1, line 2 and through standards.

After performing a full two-port calibration, the calibration standards were re-measured to obtain the self-consistency test measurements of the split block test fixture. The requirements for verifying microstrip TRL standards are summarized in Table 3.2. The self-consistency test measurements are illustrated in Figures 3.21 to 3.25. The through reflection is measured to be better than -35 dB over the calibrated frequency band, while the measured through phase variation is 0.5° over the calibrated frequency band. The trace marked Measured ThruC (Δ marker) are the through measurements measured directly after the calibration was performed, excluding test fixture mechanical variations. The trace marked Measured ThruM (\square marker) are the through measurements accounting for test fixture mechanical variations. The through measurements are shown in Figures 3.21 and 3.22.

Compared to the split connector test fixtures measurement results, the simulated and measured phase of the line standards correlate much better. For the line 2 standard, at 6.5 GHz the simulated microstrip phase, the trace marked Microstrip Line2 (Δ marker), is -101° while the measured phase, the trace marked Measured Line2 (\square marker), is -90.5° . This is illustrated in Figure 3.24. This difference is much more tolerable than the split connector test fixture measurements. There are still small phase differences between the measured and simulated line standards, but these phase differences are the results of line length and ϵ_r variations. This calibration's measured results are an improvement on the split connector calibration measurements. However, as illustrated in Figure 3.25, the reflection standard phase measurement has resonance peaks. This means that to the vector network analyser the open standard does not act as an open. This is because of the width of the open-ended lines, which will lead to more radiation from the open at high frequencies.

Replacing the open reflection standard with a short reflection standard quickly solved this problem. The short was implemented by shorting a microstrip transmission-line directly to ground. The path to ground was only 0.635 mm long, the height of the substrate. Only one short standard was manufactured and used at both port 1 and port 2 during the calibration procedure. The full two-port calibration was repeated (with the short standard as reflection) and a self-consistency test was performed to verify the behavior of the microstrip TRL standards. The measured results are shown in Figures 3.26 to 3.30.

The measured through reflection, the trace marked ThruM (\square marker and Δ marker), is compared with a ideal microstrip transmission line simulated in Microwave Office (MWO), the trace marked Microstrip Line (\diamond marker). A reflection of -30 dB was measured over the calibrated frequency band, while a reflection of -40 dB was simulated in MWO. The MWO model assumes a Quasi-TEM mode of propagation and incorporates the effects of dielectric and conductive losses, and is an acceptable indication of a realistic measurement. The measured results of the through standard, illustrated in Figure 3.26, differs only 10 dB with the simulated data. The

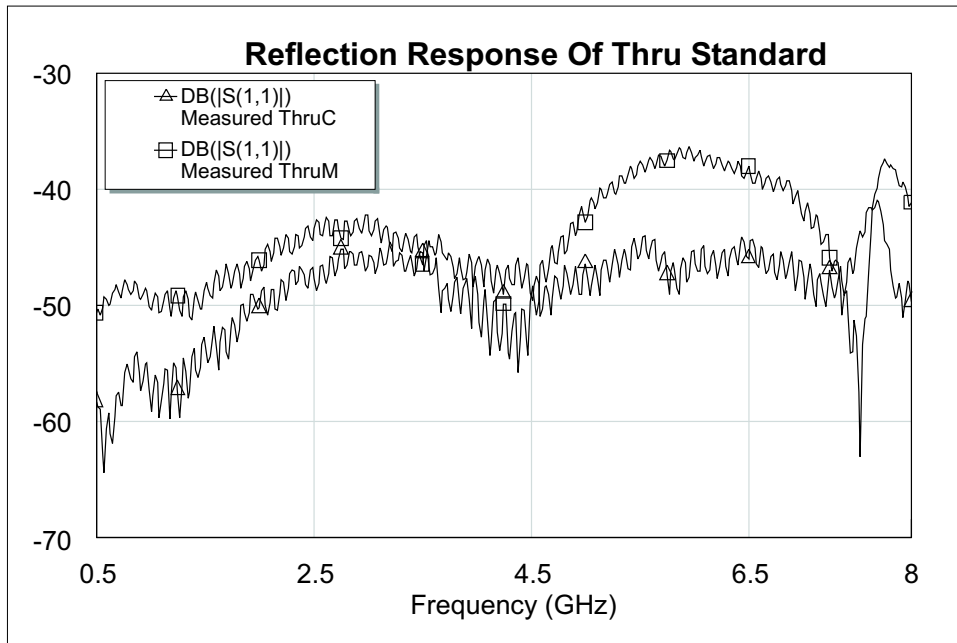


Figure 3.21: The through standards reflection response measured after TRL calibration was performed. A reflection better than -35 dB up to 8 GHz are measured for both S_{11} and S_{22} . The reflection is illustrated on a logarithmic scale.

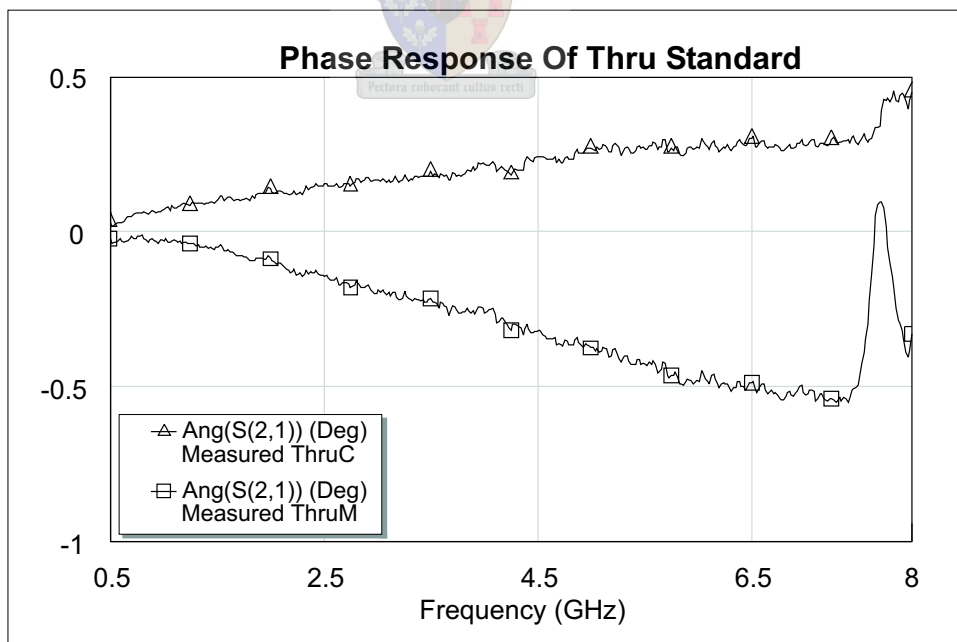


Figure 3.22: The through standards phase response measured after TRL calibration was performed. A phase error of 0.5° at 8 GHz is measured for the through standard.

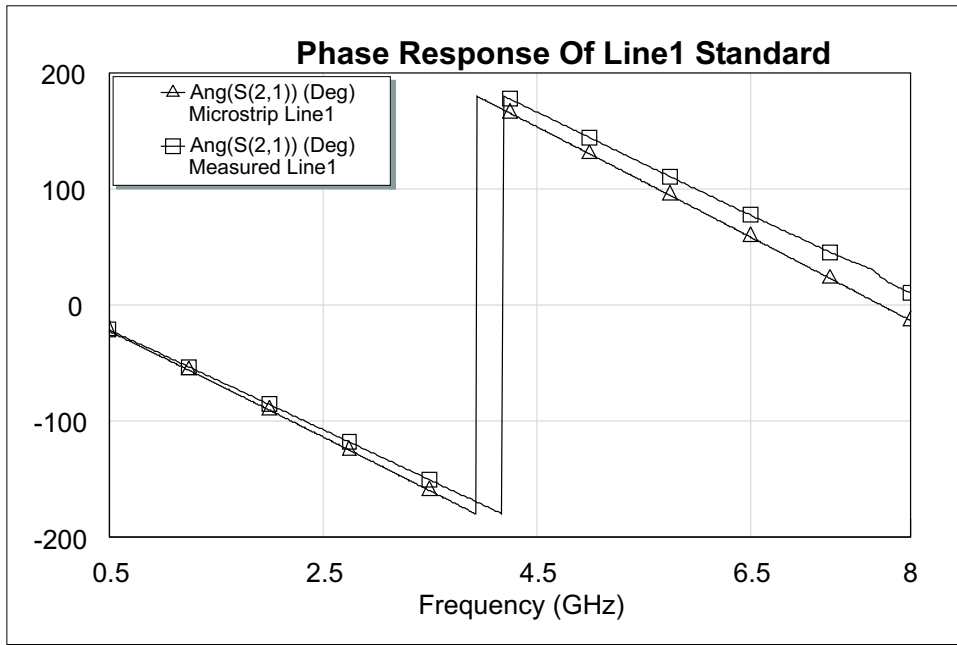


Figure 3.23: A comparison between the measured phase response, the trace marked Microstrip Line1 (Δ marker), and the MWO (ideal) simulated phase response, the trace marked Measured Line1 (\square marker), of the line 1 standard.

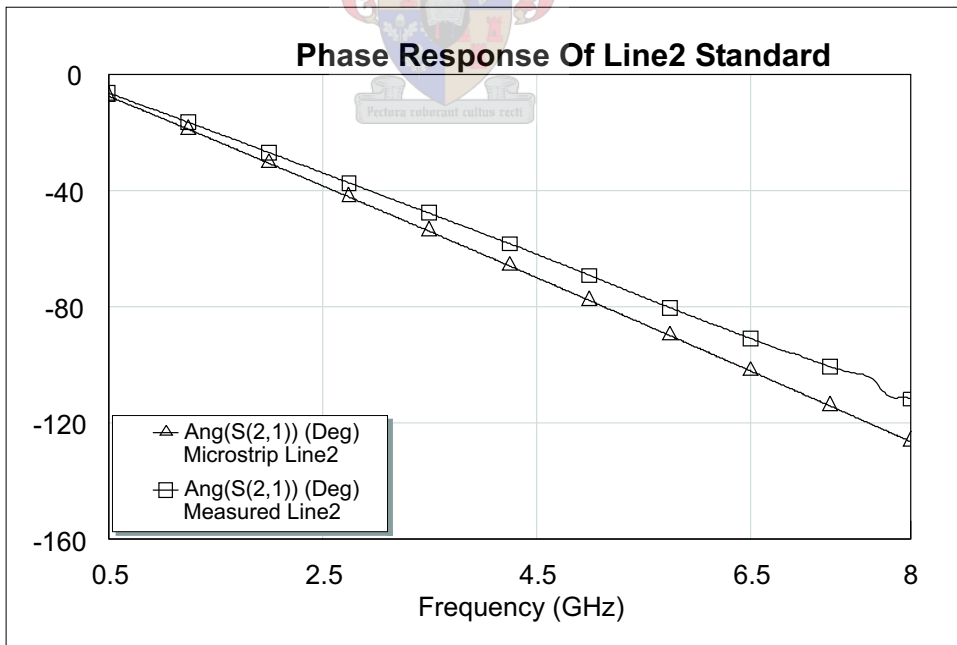


Figure 3.24: A comparison between the measured phase response, the trace marked Microstrip Line2 (Δ marker), and the MWO (ideal) simulated phase response, the trace marked Measured Line2 (\square marker), of the line 2 standard.

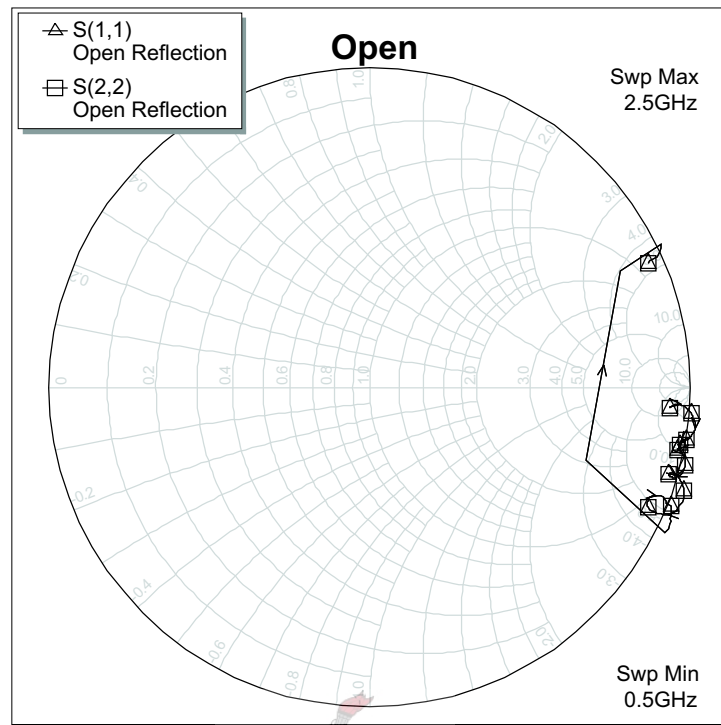


Figure 3.25: The measured input and output reflection phase responses of the open standard. The open reflections are displayed on a low impedance (12 Ohm) Smith chart.

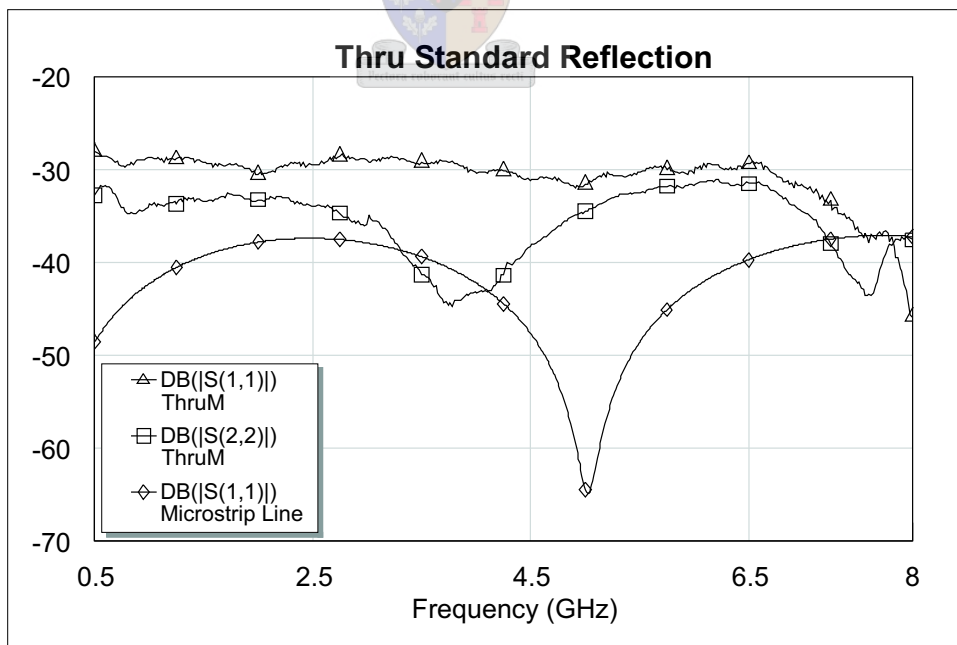


Figure 3.26: The through standards reflection response measured after a TRL calibration was performed. A reflection of -30 dB over the frequency band are measured.

measured phase response has an error of 0.9° at 4.5 GHz, illustrated in Figure 3.27. The trace marked ThruC (\square marker) is the measured phase directly after calibration, not incorporating mechanical variations from test fixture. The trace marked ThruM (\triangle marker) is the measured phase results that incorporate test fixture mechanical variations. The short standards measured meets the requirements stated in Table 3.2. The measured results are illustrated in Figure 3.28. The line standards phase responses, illustrated in Figures 3.29 and 3.30, compare well with the simulated phase of the microstrip lines used. The maximum phase deviation between the measured and simulated data is 6° . This phase difference is the result of substrate dielectric constant variations, as will be discussed in Section 3.3. This test fixture together with these calibration standards fulfills all requirements of a good, reliable and repeatable microstrip TRL test fixture.

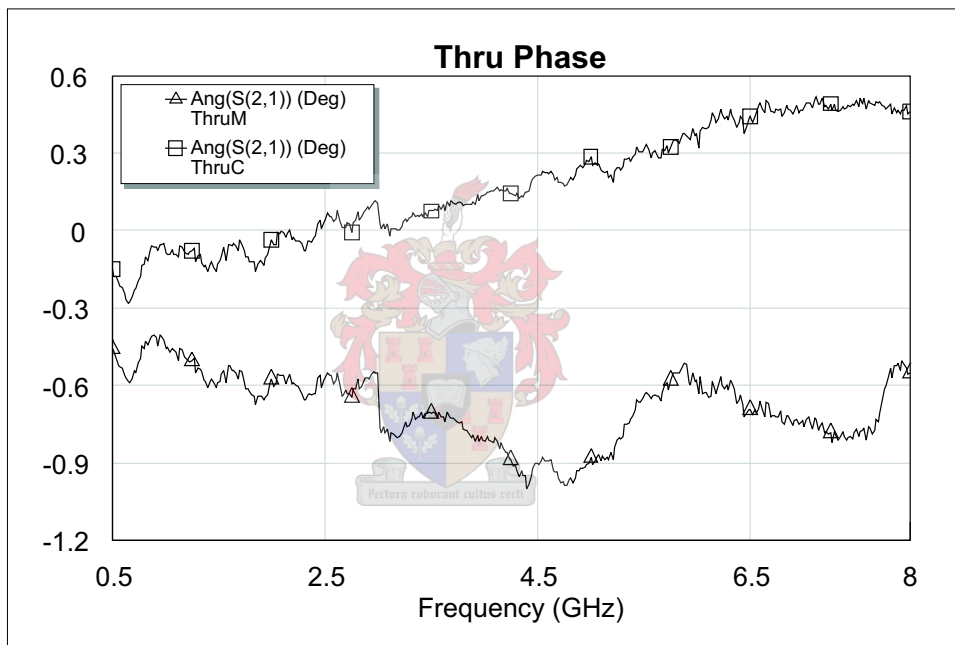


Figure 3.27: The through standards phase response measured after TRL calibration was performed. The worst phase error, an error of 0.9° , was measured at 4.5 GHz for the through standard.

3.3 Microstrip Transmission Line Parameter Extraction

The characteristic impedance of a dispersive microstrip transmission line may be determined by using the propagation constant, which is extracted from measured S-parameters obtained from a vector network analyser. The resulting impedance-transformed S-parameters better

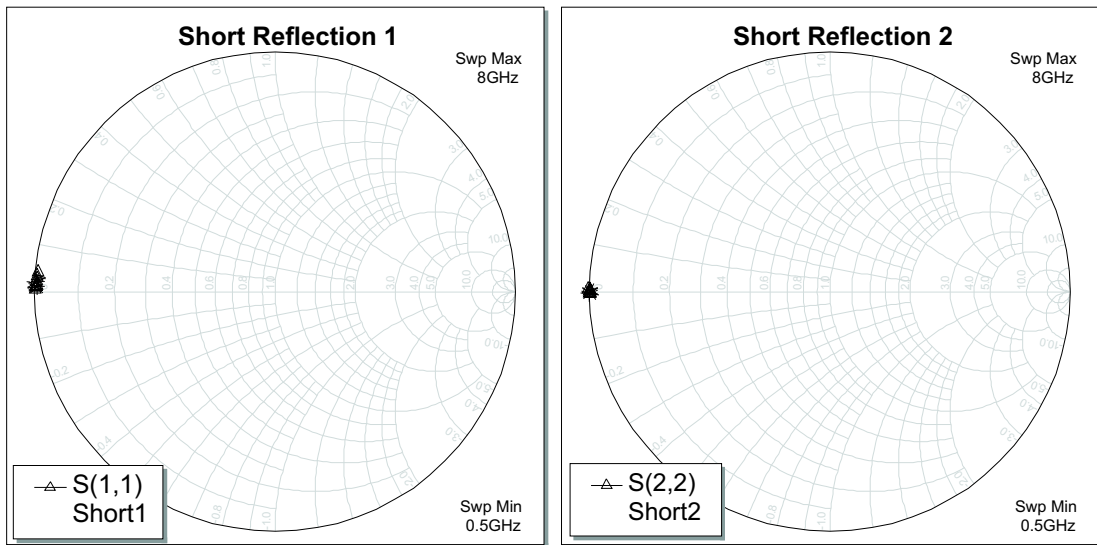


Figure 3.28: The measured input and output reflection phase responses of the short standard. The short standards reflections are displayed on a low impedance (12-ohm) Smith chart.

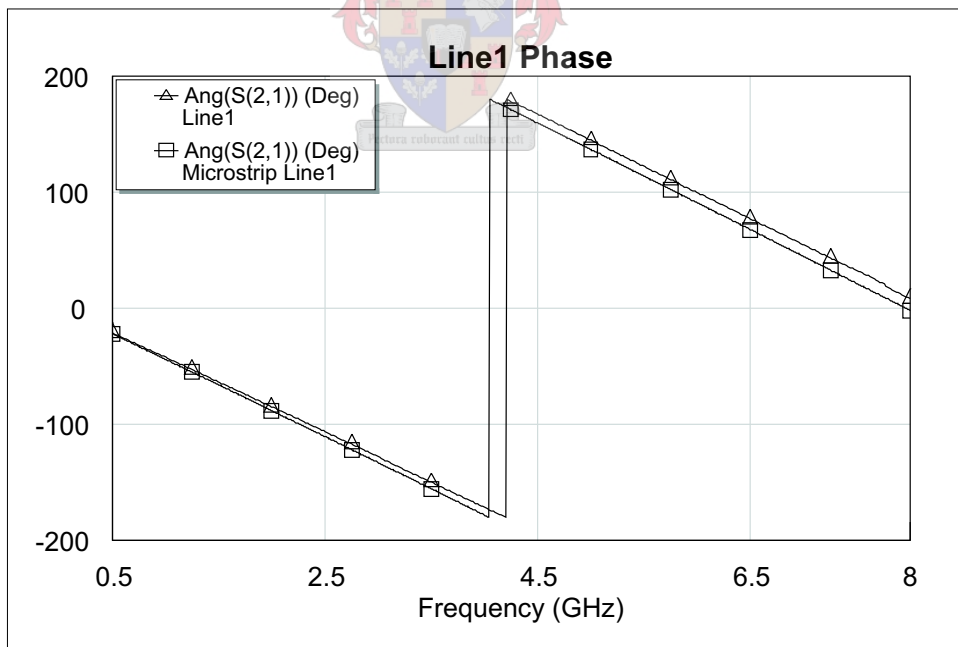


Figure 3.29: A comparison between the measured phase response, the trace marked Line1 (△ marker), and MWO (ideal) simulated phase response, the trace marked Microstrip Line1 (□ marker), of the line 1 standard.

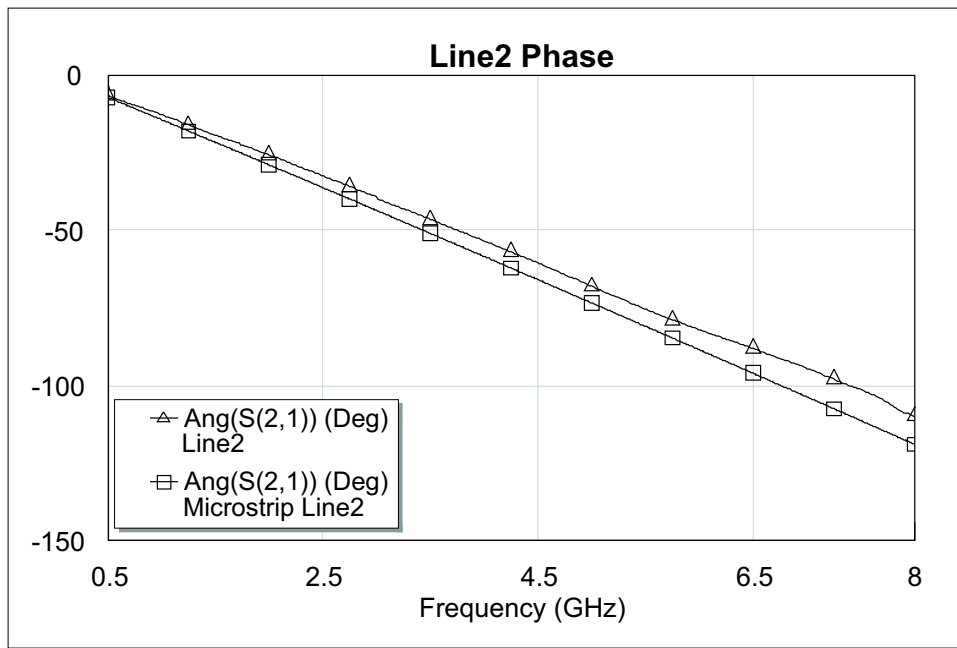


Figure 3.30: A comparison between the measured phase response, the trace marked Line2 (\triangle marker), and MWO (ideal) simulated phase response, the trace marked Microstrip Line2 (\square marker), of the line 2 standard.

reflect the nature of the device under test (DUT). The ϵ_r parameter was extracted because the manufacturing tolerance of the substrate used (Rogers 6010.2), is 9.5-10.45 and a more exact number is needed. The microstrip propagation-constant was measured with two different techniques. The first approach used is the direct TRL calibration technique described by Engen and Hoer [23] to extract the propagation constant after performing a two-tier calibration. The second method used is the multilayer approach proposed by Marks [24, 25]. This technique can be used with either uncalibrated measurements or a two-tier calibration. These two techniques provide three sets of data for extracting the substrate parameters.

3.3.1 The Direct TRL Calibration Technique

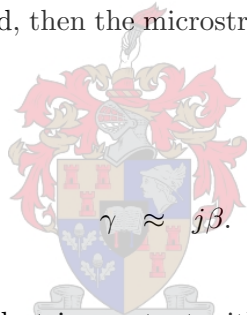
To implement the first technique, a first-tier SOLT (short-open-load-thru) calibration must be performed. The first-tier calibration was performed with a commercially available 85052D 3.5 mm Economy calibration kit provided by Hewlett-Packard. The aim of the first-tier SOLT calibration procedure is to compensate for the effect of the vector network analyser hardware and the measurement set up (like the cables). This calibration process establishes a primary measurement reference plane, at the ends of the cables used. Once the calibration is completed, the vector network analyser can measure the response of the system contained between the

primary calibration planes [26].

The pre-matching networks together with the TRL calibration standards (thru-reflect-line standards), described in Section 3.2.5, was placed between the primary calibration planes and measured. Code, based on Engen and Hoer [23], was implemented in the Matlab environment (see Appendix B). This code then performed the second-tier calibration by de-embedding the effect of the TRL test fixture from the DUT measurements using the measurements performed on the TRL calibration standards. The output consists of the de-embedded device S-parameters, and the complex propagation constant (γ) of the line standard used in the TRL calibration. The complex propagation constant is,

$$\gamma = \alpha + j\beta \quad (3.4)$$

where α is the attenuation constant and β is the propagation constant. Assume that the propagation constant (γ) loss is neglected, then the microstrip transmission line propagation constant becomes [9],



$$\gamma \approx j\beta. \quad (3.5)$$

Use β to calculate the effective dielectric constant with the following equation,

$$\varepsilon_{r(eff)} = \left(\frac{c\beta}{2\pi f} \right)^2. \quad (3.6)$$

The effective dielectric constant can be used to calculate the characteristic impedance of the microstrip calibration line. Since microstrip is a dispersive transmission line, the characteristic impedance will vary as a function of frequency. The characteristic impedance is calculated as follows [9],

$$Z_o = \frac{120\pi}{\sqrt{\varepsilon_{r,e\text{ff}}} \left[\frac{W}{h} + 1.393 + 0.667 \ln \left(\frac{W}{h} + 1.44 \right) \right]} \quad (3.7)$$

where W is the width and h is the height of the transmission line. The measured S-parameters can be renormalised with respect to the characteristic impedance.

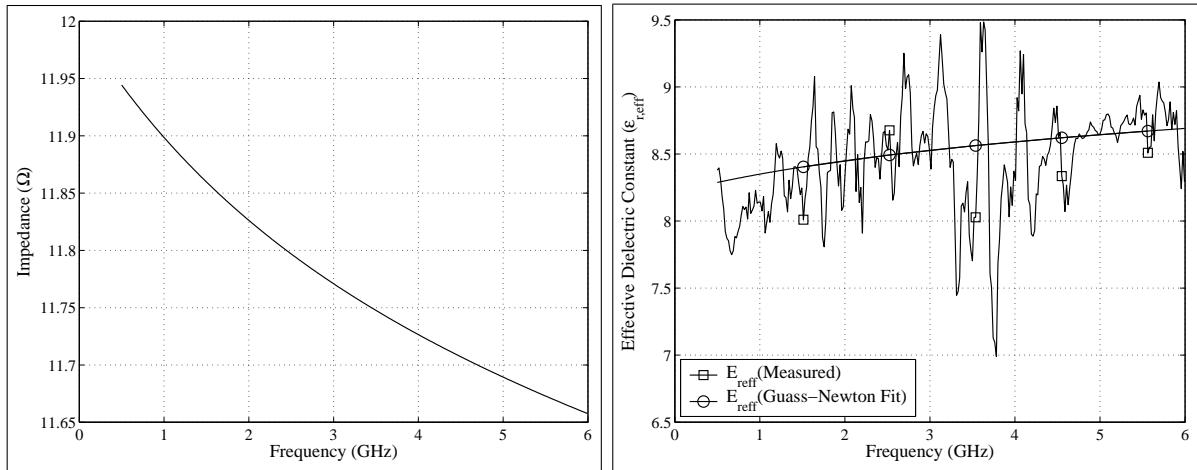


Figure 3.31: The extracted Rogers 6010.2 substrate parameters with the two-tier method. The line impedance is illustrated on the left hand side while the effective dielectric constant is illustrated on the right hand side.

The measured effective dielectric constant extracted with the two-tier calibration method is illustrated in Figure 3.31. The trace marked $E_{r,eff}(\text{Measured})$ (\square marker), is the measured effective dielectric constant, while the trace marked $E_{r,eff}(\text{Gauss-Newton Fit})$ (\circ marker) represents the Gauss-Newton least-squares fit onto the measured effective dielectric constant. A Gauss-Newton optimiser is used to fit the effective dielectric constant model calculated in Equation 2.11 onto the measured effective dielectric constant. The Gauss-Newton optimiser is used to adjust the dielectric constant of the substrate until a "least-squares" fit between the measured and modelled effective dielectric constant is minimised. The model fit is not a polynomial fit onto the measured data, but the substrate parameters are varied to fit the measured data the best. The ϵ_r extracted from this technique was calculated to be 9.8132. The impedance extracted is also illustrated in Figure 3.31. A change of 0.3Ω in the characteristic impedance of the microstrip line is observed [27].

3.3.2 Parameter Extraction with the Multiline Method

The second method used was the multiline method, as described by Marks [24, 28, 29]. This method is used for determining the propagation-constant from S-parameter measurements of two or more transmission line standards. The advantage of the multiline method is that no network analyser calibration is needed. The S-parameter measurements of the line standards are conveniently represented in wave cascade matrix (M) form. For a two-port device, the relationship is as follows,

$$M = \frac{1}{S_{21}} \begin{bmatrix} (S_{12}S_{21} - S_{11}S_{22}) & S_{11} \\ -S_{22} & 1 \end{bmatrix} \quad (3.8)$$

The multiline method uses switch-term-corrected measurements from pairs of transmission lines in order to find γ . For any given transmission line measurement, the wave cascade matrix is determined as follows,

$$M^i = XT^iY \quad (3.9)$$

$$T^i = \begin{bmatrix} \exp^{-\gamma l_i} & 0 \\ 0 & \exp^{\gamma l_i} \end{bmatrix} \quad (3.10)$$

where cascade matrices X and Y represent imperfections of the network analyser, the effects of the cables connected to the transmission lines and the pre-matching transmission line tapers. The matrix T^i represents the cascade matrix for an ideal transmission line standard i . The measured cascade matrices of two transmission line standards i and j of differing lengths can be combined into an eigenvalue equation [28],

$$M^{ij}X = XT^{ij} \quad (3.11)$$

where

$$M^{ij} = M^j[M^i]^{-1} \quad (3.12)$$

and

$$T^{ij} = T^j[T^i]^{-1} \quad (3.13)$$

$$T^{ij} = \begin{bmatrix} \exp^{-\gamma(l_j-l_i)} & 0 \\ 0 & \exp^{\gamma(l_j-l_i)} \end{bmatrix} \quad (3.14)$$

where l_i and l_j are the physical lengths of the transmission line standards.

$$T^{ij} = \begin{bmatrix} E^{ij} & 0 \\ 0 & E^{ij} \end{bmatrix} \quad (3.15)$$

Since T^{ij} is diagonal, its diagonal elements are the eigenvalues of T^{ij} and M^{ij} . The two eigenvalues λ_{1M}^{ij} and λ_{2M}^{ij} of M_{ij} are

$$\lambda_{1M}^{ij}, \lambda_{2M}^{ij} = \frac{1}{2} \left[(M_{11}^{ij} + M_{22}^{ij}) \pm \sqrt{(M_{11}^{ij} - M_{22}^{ij})^2 + 4M_{12}^{ij}M_{21}^{ij}} \right] \quad (3.16)$$

and the two eigenvalues λ_{1T}^{ij} and λ_{2T}^{ij} of T_{ij} are

$$\lambda_{1T}^{ij}, \lambda_{2T}^{ij} = e^{\pm\gamma(l_j - l_i)} \quad (3.17)$$

The next step is to calculate which of these two eigenvalues is the correct one. To carry out the assignment, an initial guess is made, $E_1^{ij} = \lambda_{1M}^{ij}$ and $E_2^{ij} = \lambda_{2M}^{ij}$. A propagation-constant is computed from the E 's and compare to the estimated γ_{est} defined in Equation 3.18. A second guess, $E_1^{ij} = \lambda_{2M}^{ij}$ and $E_2^{ij} = \lambda_{1M}^{ij}$ provides another difference between the computed propagation-constant and γ_{est} .

The following procedure were used to obtain the correct eigenvalue. An estimate of the propagation-constant γ_{est} was computed, based on user-supplied transmission line parameters. An accurate estimate for $\epsilon_{r,eff}$, the effective dielectric constant of the transmission line standards are needed. Only one value may be entered for the real part, $\epsilon'_{r,eff}$, without specifying a frequency. For lossy transmission lines, an estimate of the imaginary part of the effective dielectric constant, $\epsilon''_{r,eff}$, at 1 GHz may be entered. The estimated value for the effective dielectric constant can be calculated as follows,

$$\gamma_{est} = j \frac{2\pi f}{100c} \sqrt{\epsilon'_{r,est} + j \frac{\epsilon''_{r,est}}{f/10^9}} \quad (3.18)$$

where c is the speed of light in vacuum in cm/s and f is the frequency in Hz. Calculate the two different eigenvalues possibilities,

$$\lambda_a = \frac{\lambda_{1M}^{ij} + \frac{1}{\lambda_{2M}^{ij}}}{2} \quad (3.19)$$

$$\lambda_b = \frac{\lambda_{2M}^{ij} + \frac{1}{\lambda_{1M}^{ij}}}{2} \quad (3.20)$$

Next, compute $\gamma\Delta l$ from the average eigenvalues,

$$\gamma_a \Delta l = -\ln(\lambda_a) + j2\pi P \quad (3.21)$$

$$\gamma_b \Delta l = -\ln(\lambda_b) + j2\pi P \quad (3.22)$$

where the number of periods P is needed to estimate the total delay,

$$P = \frac{\text{Im}\{\gamma_{est}\Delta l\} - \text{Im}\{-\ln(\lambda_{a,b})\}}{2\pi} \quad (3.23)$$

Lastly, compute the relative difference (D) between the two eigenvalues used,

$$\begin{aligned} D_a &= \frac{|\gamma_a \Delta l - \gamma_{est} \Delta l|}{|-\gamma_{est} \Delta l|} \\ D_b &= \frac{|\gamma_b \Delta l - \gamma_{est} \Delta l|}{|-\gamma_{est} \Delta l|} \end{aligned} \quad (3.24)$$

The smaller difference case is generally taken as the correct eigenvalue. Finally, combine Equation 3.16 and Equation 3.17, with the correct eigenvalue, to solve for the propagation constant. The propagation constant can be calculated as follow,

$$\gamma = \frac{\ln(\lambda^{ij})}{l_i - l_j} \quad (3.25)$$

Once the correct γ is established, the transmission line effective dielectric constant and the impedance can be calculated as follows [9],

$$\epsilon_{r,eff} = - \left[\frac{\gamma}{(\omega/100c)} \right]^2 \quad (3.26)$$

where $\omega = 2\pi f$ and c is the speed of light in cm/s.

$$Z_o = \frac{120\pi}{\sqrt{\epsilon_{r,eff} \left[\frac{W}{h} + 1.393 + 0.667 \ln \left(\frac{W}{h} + 1.44 \right) \right]}} \quad (3.27)$$

where W is the width and h is the height of the transmission line. The multiline method was implemented in the Matlab environment (see Appendix B) to perform the extraction.

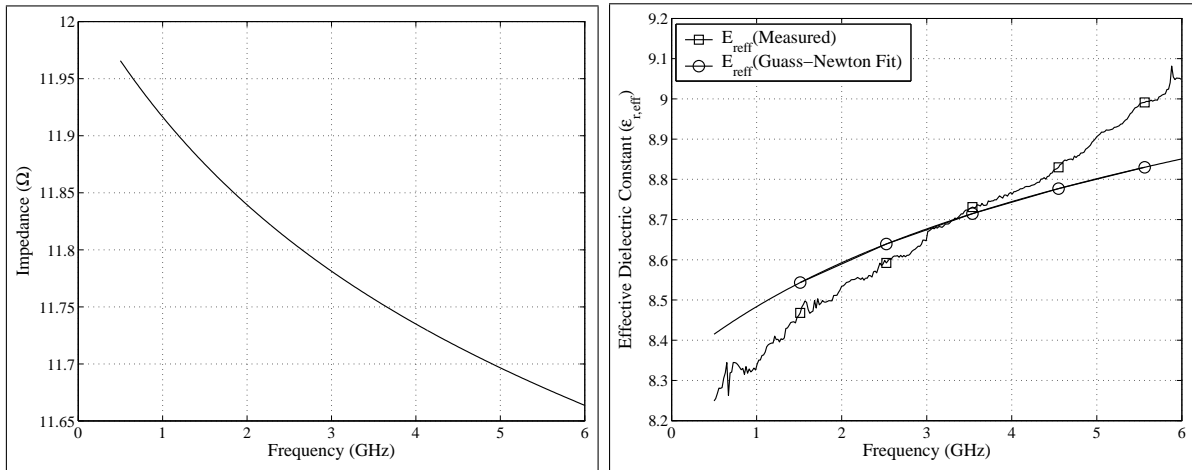


Figure 3.32: The impedance and effective dielectric constant extracted with the multiline method from uncalibration data.

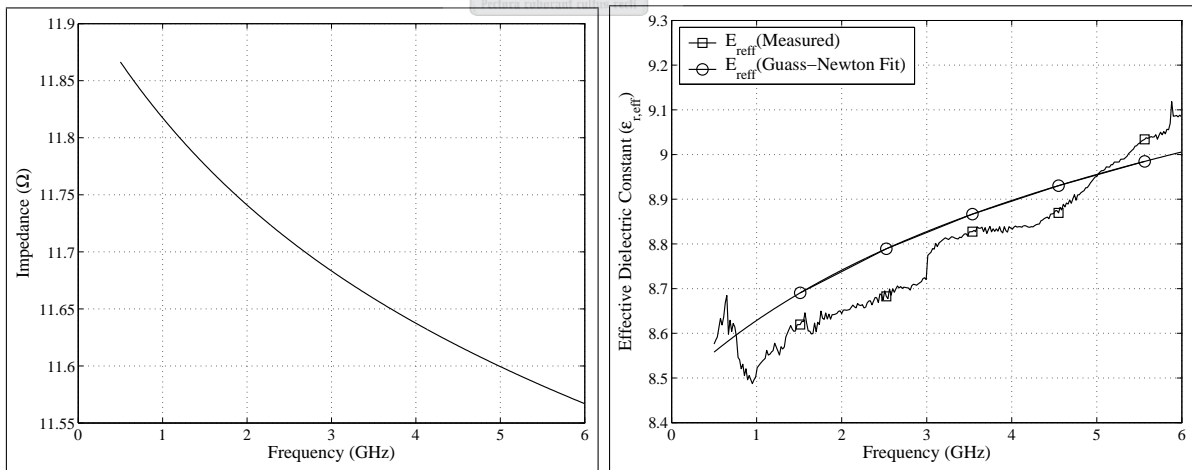
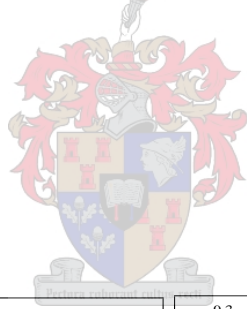


Figure 3.33: The impedance and effective dielectric constant extracted with the multiline method after a SOLT calibration.

In Figures 3.32 and 3.33, the trace marked $E_{r,eff}$ (Measured), (\square marker), is the measured effective dielectric constant extracted with Marks [24, 29] method. The trace marked $E_{r,eff}$ (Guass-Newton Fit), (\circ marker), is the Guass-Newton least-squares fit of the $E_{r,eff}$ (model) onto the measured effective dielectric constant. The impedance and effective dielectric constant shown in Figure 3.32 was extracted with uncalibrated data, while the impedance and effective dielectric constant shown in Figure 3.33 was extracted with data obtained after performing a SOLT calibration to account for imperfections of the network analyser and the effects of the cables connected to the transmission lines. The extracted ε_r from the first measurement was 9.9412 and from the second measurement 9.9636.

Equation 3.27 was used to calculate the extracted characteristic impedance of the microstrip line. The impedance extracted by the two different measurements are illustrated in Figures 3.32 and 3.33, on the left hand side. A change less than 0.3Ω in the characteristic impedance of the microstrip line is observed. The change in the characteristic impedance of the transmission line may make devices seem more mismatched than what they really are. To compensate for this mismatch the measured S-parameters should be normalised by this extracted impedance [30, 31].

The different extracted dielectric constants obtained from these various measurement techniques were implemented in the MWO environment to see if the simulated and measured data correlate better than before. The measured and simulated data is exactly the same with a ε_r of 9.9636, as illustrated in Figures 3.34 and 3.35.

Compared to the technique described in Section 3.3.1, the multiline method is considerably smoother. The sharp peaks obtained with the direct method, as shown in Figure 3.31, are eliminated. Both techniques used provide accurate dielectric constant parameters with which precision designs can be implemented.

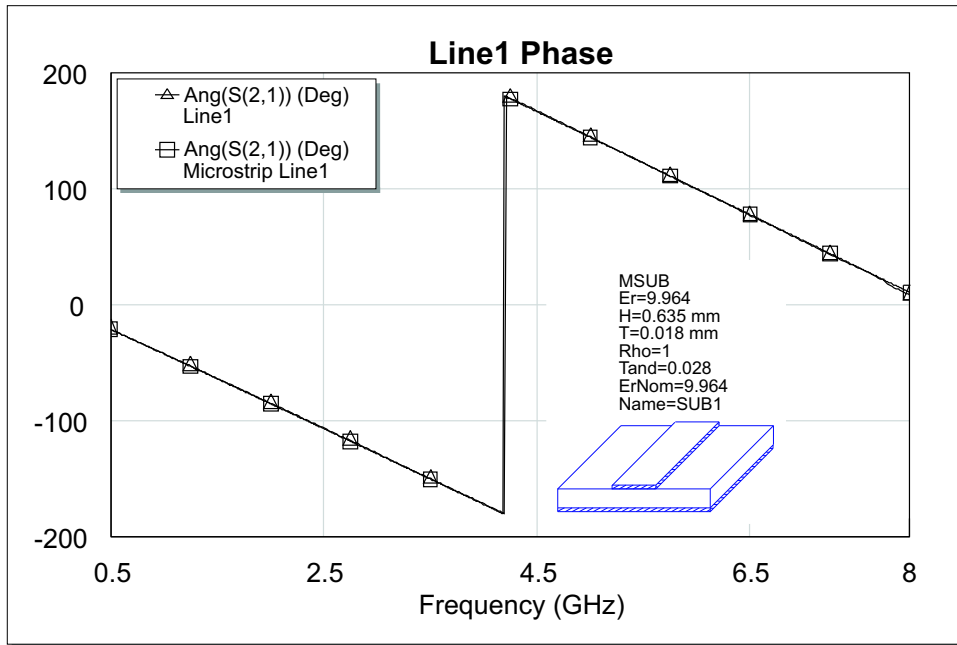


Figure 3.34: A comparison between the MWO (modified) simulated phase response, the trace marked Microstrip Line1 (□ marker), and the measured phase response, the trace marked Line1 (△ marker), of the line 1 standard.

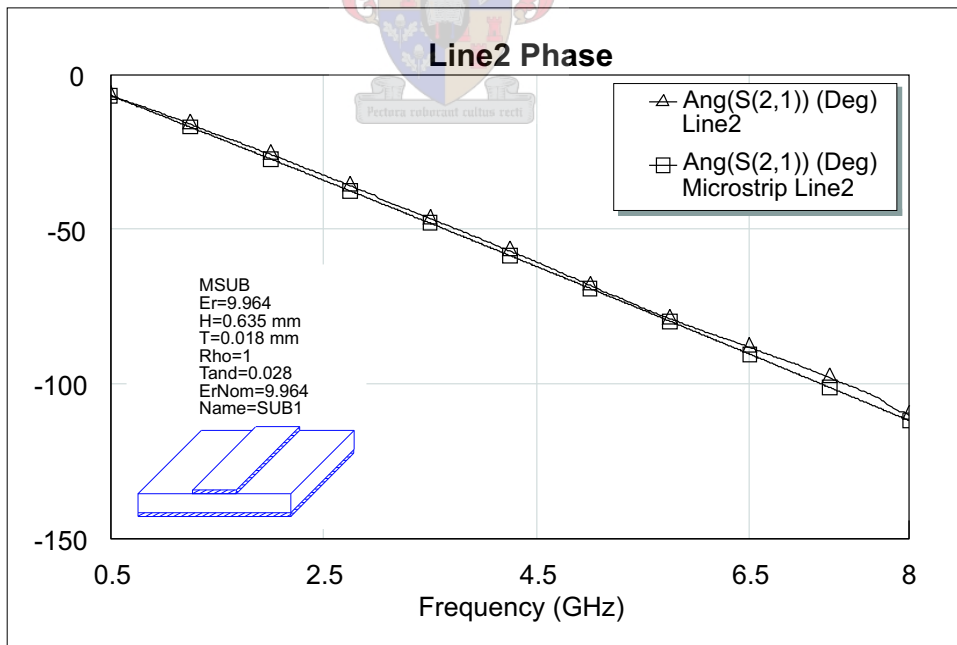


Figure 3.35: A comparison between the MWO (modified) simulated phase response, the trace marked Microstrip Line2 (□ marker), and the measured phase response, the trace marked Line2 (△ marker), of the line 2 standard.

3.4 Conclusion

This chapter presented the development of high-quality low impedance TRL test fixtures. The development started with the design of microstrip transmission line tapers which transforms the 50 Ohm measurement environment to a low impedance environment. This method was extended into the design of a multi purpose TRL test fixture. Two different methods were used to design two low impedance TRL calibration kits. The first method was the split connector test fixture, and the second method was the more traditional split block test fixture. The split connector test fixtures measured results were not as expected but with a number of changes and attention this technique can achieve all expectations to a high level of accuracy. The split block test fixture presented good repeatable measurements. This calibration was used to perform the substrate parameter extraction of the substrate used.

Moreover, the cost of implementing these low impedance test fixtures is small. For a wide calibration band over which more than one line is needed in any case, the proposed methods simply provide a more efficient utilization of available information at very little additional cost.



Chapter 4

LDMOS Transistor Equivalent Circuit Parameter Extraction

4.1 Introduction

Designing RF circuits requires RF behavioral models of all the devices used in the circuit describing their function in the system. To model the behavior of LDMOS transistors, compact models or equivalent circuit-based models as proposed in [32, 33] can be used. The small-signal equivalent circuit model is obtained by optimising the circuit component values to attain a close fit between the small-signal S-parameters measurements of the device and the equivalent circuit model. The small-signal equivalent circuit representation of the LDMOS transistor can be divided into two parts, namely the intrinsic elements, which are functions of the biasing conditions, and the extrinsic elements, which are independent of the biasing conditions.

The LDMOS equivalent circuit modeling is performed in three steps. The first step is to extract the transistor package components (gate and drain leads). The next step is to extract the bondwires that connect the transistor gate and drain leads with the transistor-die. The last step in the equivalent circuit modeling is the extraction of the intrinsic FET model. Representations of an LDMOS equivalent circuit model and a LDMOS transistor package are illustrated in Figure 4.1.

4.2 LDMOS Package Parameter Extraction

The main goal of the parameter extraction, is to develop an accurate equivalent circuit model for the LDMOS packaged transistor. This model can be used in conjunction with active tran-

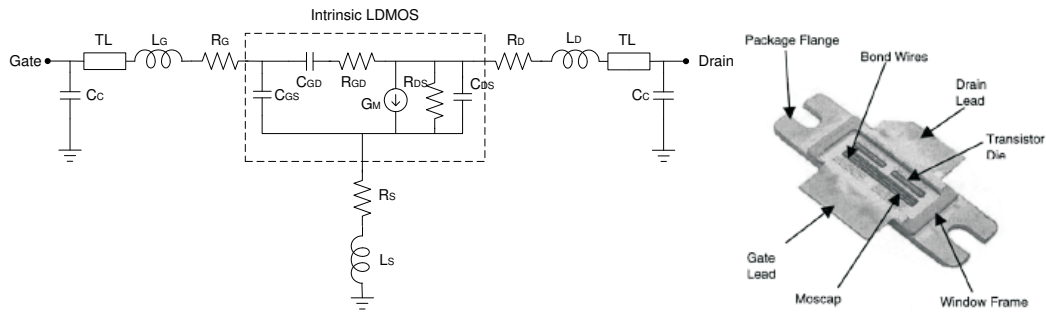


Figure 4.1: An illustration of the LDMOS transistors small-signal equivalent circuit representation and the LDMOS metal-ceramic package terminology [34, 35, 7].

sistor models to predict the performance of packaged transistors more accurately. High-power RF devices are generally contained in metal-ceramic packages, used due to their power dissipation ability, mechanical strength and ruggedness. Knowledge of the equivalent circuit model of a LDMOS transistor package is very useful in designing microwave power circuits. It has previously been demonstrated that at high frequencies, the package parasitic effects play an important role in the accurate prediction of transistor performance [7, 36]. Thus, the first step in extracting an equivalent circuit is to generate an electrical package model for the extrinsic package elements. These package elements are independent of the biasing conditions, and form the parasitic components that largely influence the electrical behavior of the RF device. The parasitic components mainly originate from the package lead-to-substrate capacitance (C_c) and the short length of transmission line across the ceramic window frame of the gate and drain terminals of the package (TL), as illustrated in Figures 4.3 and 4.4.

Empty BLL1214-35 L-band radar LDMOS driver transistor packages (obtained from Philips Semiconductor) were used to obtain the package parameters. One was used as an open circuit and the other was modified to a short-all circuit. A short standard is normally a two-port structure of which one port is shorted and the other port is open-ended, but the short-all is a two-port structure of which both ports are shorted simultaneously. The open and short-all standards used are illustrated in Figure 4.2. The advantage of using these standards is that both the gate and drain leads of the two are equivalent, enabling their effects to be extracted easily.

Equivalent circuit representations for the open and short-all standards are illustrated in Figures 4.3 and 4.4 respectively. The open standard equivalent circuit model consists of capacitive coupling between the gate and drain leads, C_{Cgd} , as well as capacitive coupling between the gate-source and drain-source terminals, C_{Cgs} and C_{Cds} . The short-all equivalent circuit model consists of electromagnetic coupling between the transistor package ports. This coupling is represented with a star inductor network, L_{Cgs} , L_{Cds} and L_{Cs} . These capacitors and inductors

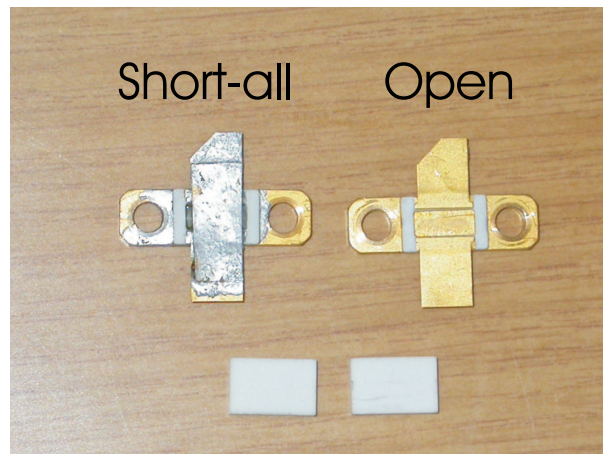


Figure 4.2: A photo representation of the Philips transistor package used as the open and short-all structures in the package extraction measurements. The packaged area that is hatched at 45° is the gate flange, the area that is dashed is the drain flange and the solid area is the grounded source.

are only used to model the open and short-all standards to obtain the lead parameters, and are not part of the final transistor model.

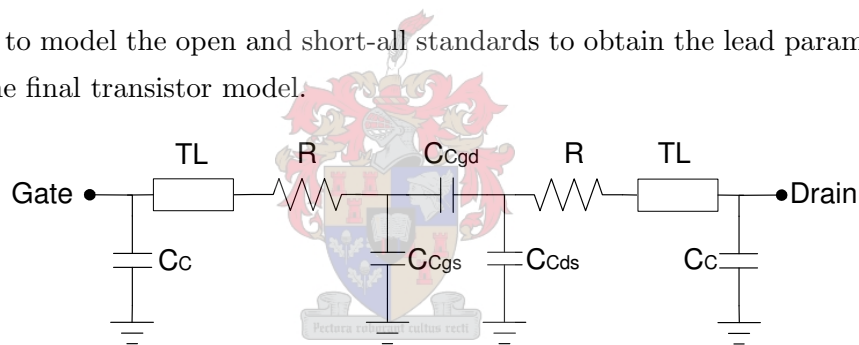


Figure 4.3: An equivalent circuit representation of the open standard used.

All of the circuit parameters, as illustrated in Figures 4.3 and 4.4, are extracted from S-parameter measurements performed on the standards, except for the short lengths of transmission line at the gate and drain terminals. These parameters were obtained from physical dimension measurements on the package.

To examine the role of the packaged transistor, the equivalent circuits illustrated in Figures 4.3 and 4.4, were compared with the measured S-parameter data of the empty Philips packages. The electrical performance of these empty packages was measured up to 8 GHz through the use of the split block TRL test fixture. Figures 4.5 to 4.10 illustrate the measured and equivalent circuit model measurements for both standards.

The package gate and drain transmission lines were simulated as an ideal lossless transmission line. This model implies that the line length is specified as an electrical length at a certain

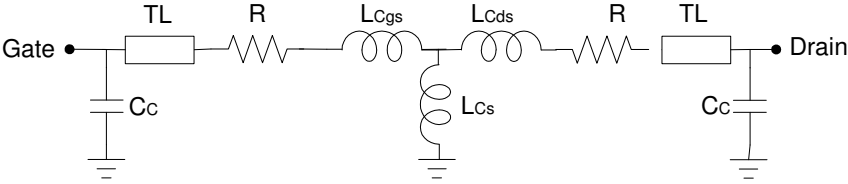


Figure 4.4: An equivalent circuit representation of the short-all standard used.

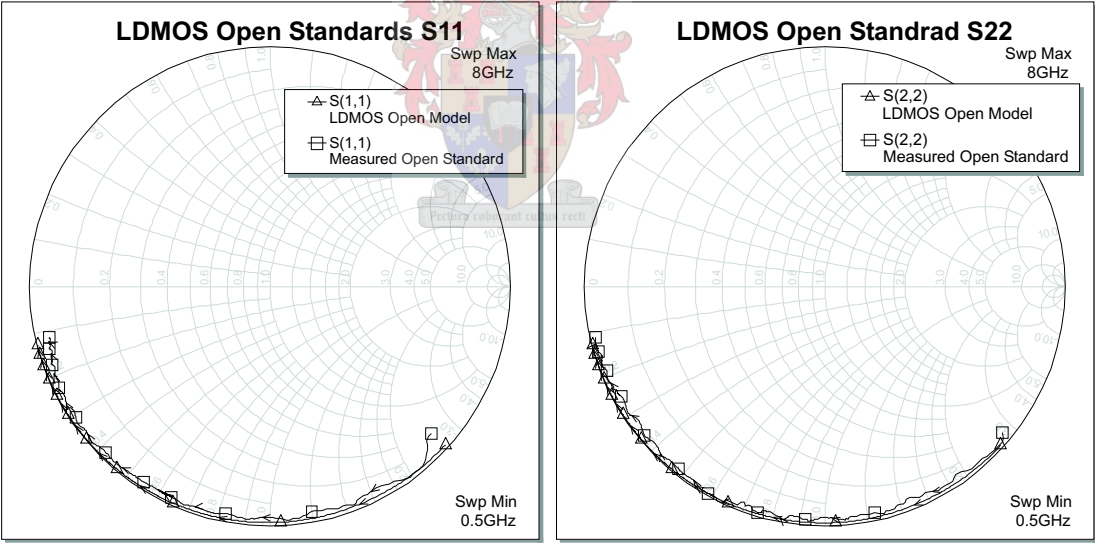


Figure 4.5: A comparison between the measured open standards input and output reflections, traces marked Measured Open Standard (\square marker), and the open equivalent circuit model input and output reflections, traces marked LDMOS Open Model (\triangle marker). These S-parameters are illustrated on a 12-ohm Smith chart.

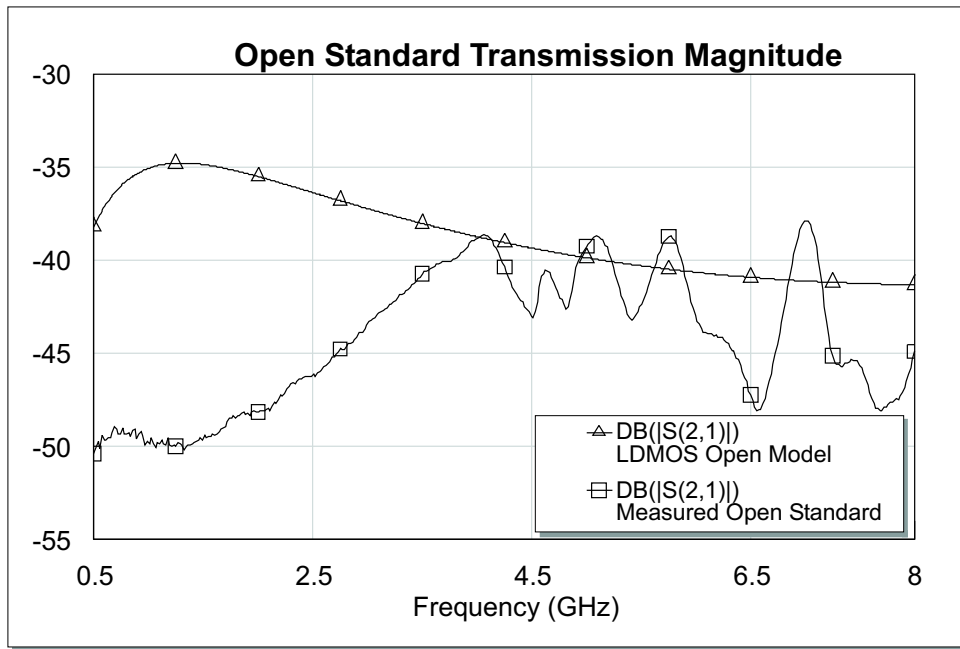


Figure 4.6: A comparison between the measured open standards transmission magnitude, the trace marked Measured Open Standard (\square marker), and the open equivalent circuit model transmission magnitude, the trace marked LDMOS Open Model (Δ marker).

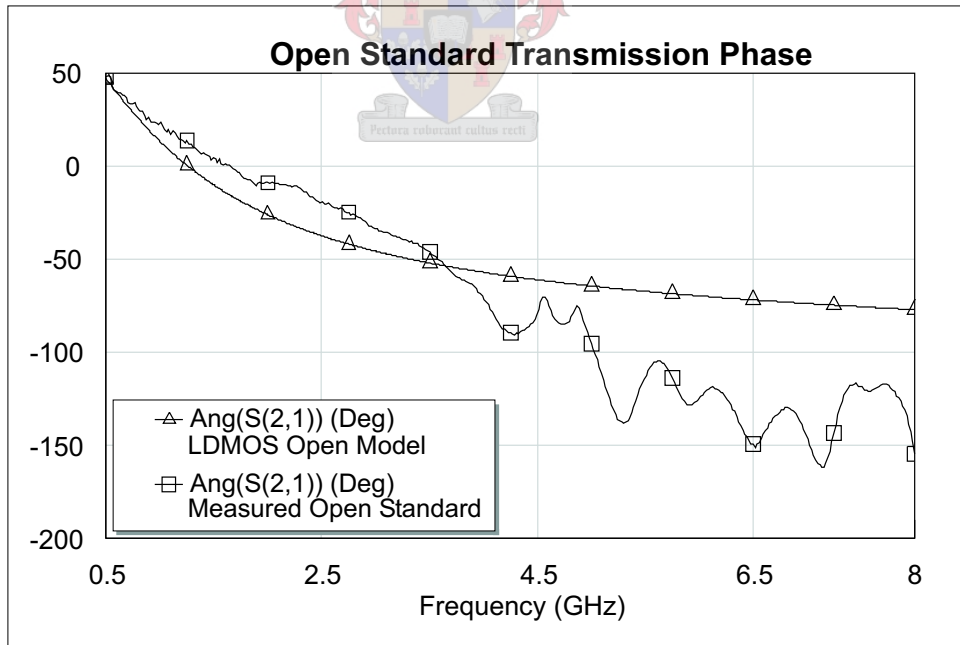


Figure 4.7: A comparison between the measured open standards transmission phase, the trace marked Measured Open Standard (\square marker), and the open equivalent circuit model transmission phase, the trace marked LDMOS Open Model (Δ marker).

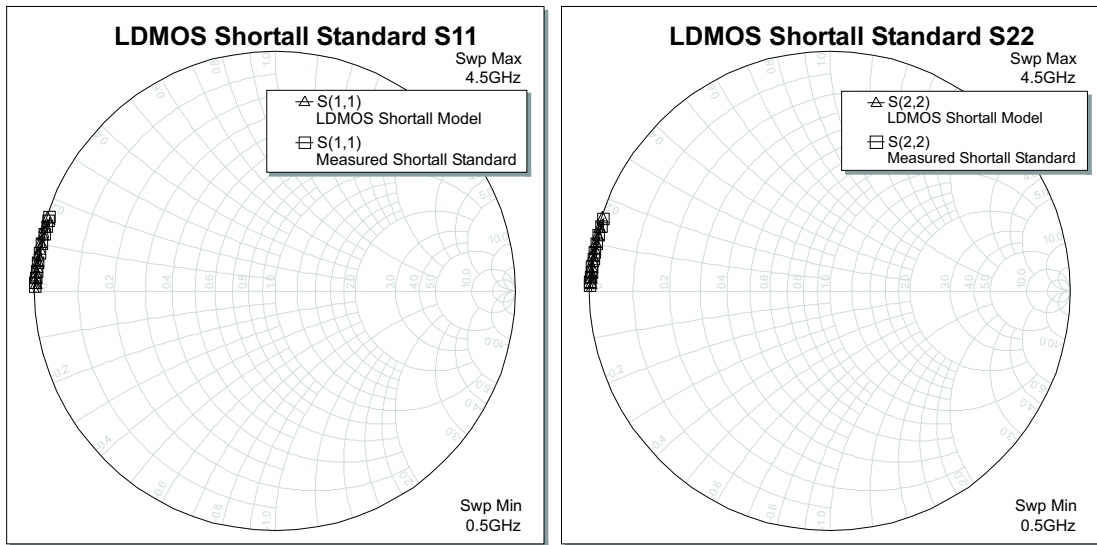


Figure 4.8: A comparison between the measured short-all standards input and output reflections, traces marked Measured Shortall Standard (\square marker), and the short-all equivalent circuit model input and output reflections, traces marked LDMOS Shortall Model (\triangle marker). These S-parameters are illustrated on a 12-ohm Smith chart.

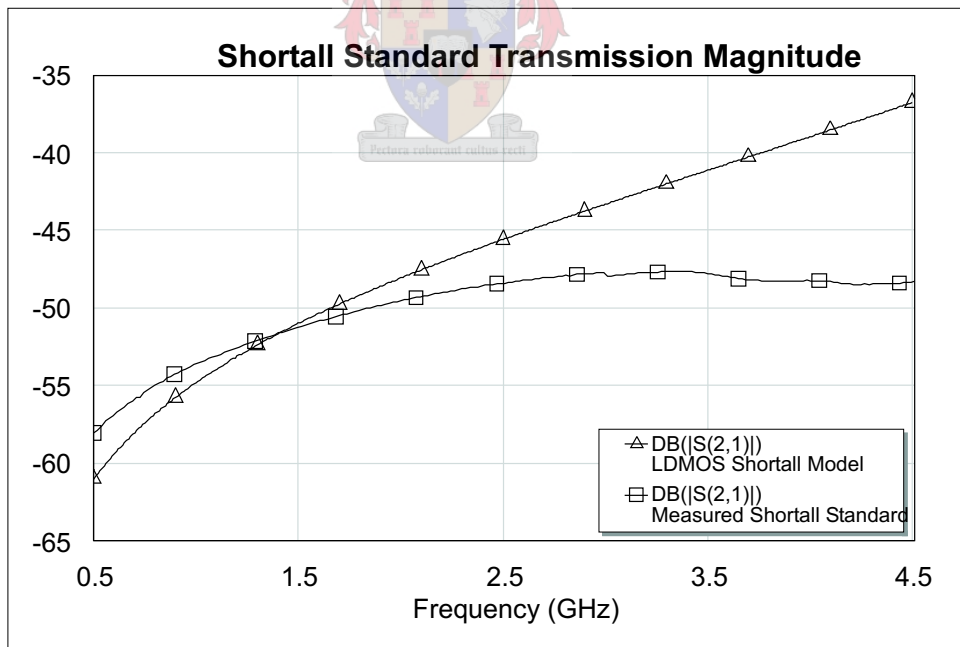


Figure 4.9: A comparison between the measured short-all standards transmission magnitude, the trace marked Measured Shortall Standard (\square marker), and the short-all equivalent circuit model transmission magnitude, the trace marked LDMOS Shortall Model (\triangle marker).

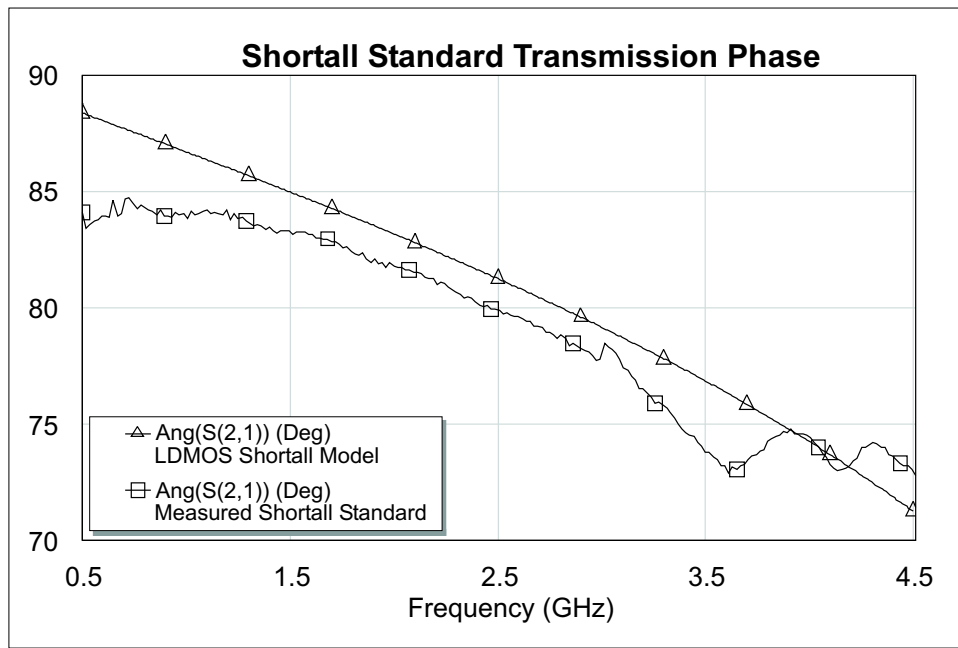


Figure 4.10: A comparison between the measured short-all standards transmission phase, the trace marked Measured Shortall Standard (\square marker), and the short-all equivalent circuit model transmission phase, the trace marked LDMOS Shortall Model (\triangle marker).

specified frequency with a certain characteristic impedance value. The transmission lines were calculated to have a characteristic impedance (Z_o) of 2.204Ω , and an electrical length of 6.464° at 1 GHz. The lead-to-substrate capacitance C_C starting value was obtained from [7] and fine-tuned in Microwave Office. The fine-tuned lead-to-substrate capacitance C_C was extracted to be 1.876 pF and compares well with Motorola's LDMOS RF transistor package (case 360B-01) that was extracted to be 2.1 pF [7].

The input and output reflections of the open standard were measured and modeled up to 8 GHz, while the input and output reflections of the short-all standard were only modeled up to 4.5 GHz. Both these standards appeared to be symmetrical, as forward and reverse measurements did not seem to have an effect on the results. However, improved measurement results were obtained when the ceramic caps, as shown in Figure 4.2, were pressed onto the standards during measurement. The measured data of the short-all standard showed unexplained resonances that could not be modeled above 5 GHz. Measurement imperfections and construction problems leading to standard imperfections, might be the cause of these resonances. It was decided to fit the short-all model only up to 4.5 GHz, as shown in Figures 4.8 to 4.10. The comparison between the measured and modeled input and output reflections of the two standards shows exceptional correlation, as shown in Figures 4.5 and 4.8. The transmission parameter (S_{21}) of

the open and short-all standards were only modeled up to 4.5 GHz, being difficult to model due to the simplistic models and the dynamic range and noise floor of the calibration. The maximum magnitude and phase difference between the measurement and model of the short-all up to 2.5 GHz is 3 dB and 5° respectively, as shown in Figures 4.9 and 4.10. Overall, the transmission parameters of the two standards showed acceptable comparison.

4.3 Extrinsic Parameter Extraction

The next step is the extraction of the devices small-signal extrinsic parameters, representing the bond-wires connecting the gate and drain leads to the intrinsic transistors-die. The extraction is based on the direct analysis of small signal Z-parameters measured on the device biased in off-state, i.e. at no conduction ($V_{GS} = 0$ V and $V_{DS} = 0$ V) [37]. The LDMOS intrinsic non-linear capacitances, one of the key challenges when modeling LDMOS devices, were analysed by performing the extraction using small-signal measurements at different applied voltages ($V_{GS} < V_p$) [38]. The off-state bias condition causes the contribution of the voltage dependent current generator (G_m), used in the model illustrated in Figure 4.1, to become zero. The output drain-source resistance maximises to become an open circuit. Thus, the zero bias intrinsic small-signal equivalent circuit reduces to a delta capacitive network [4].

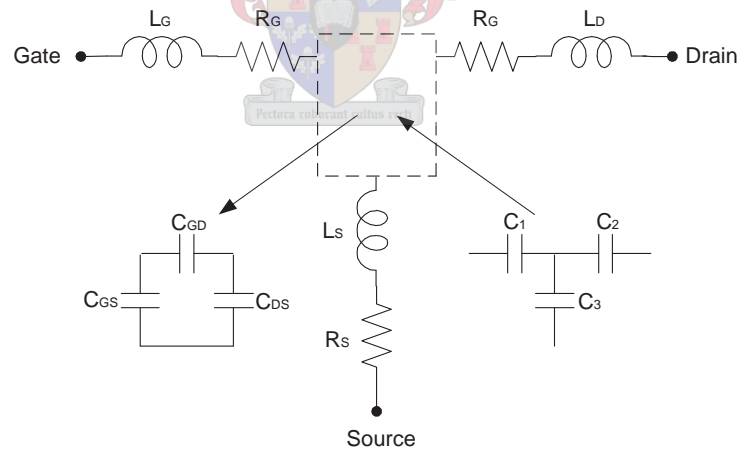


Figure 4.11: Delta-star transformation of the small-signal circuit of an off-state biased LDMOS transistor [37].

The nature of this equivalent delta capacitive network does not appear to allow direct extraction of its parameters in one single analysis step from small-signal Y- or Z-parameter measurements [37]. To overcome this obstacle the simple delta-star transformation configuration is used, as illustrated in Figure 4.11. This transformation is performed with the following set of equations,

$$\begin{aligned}
C_{GS} &= \frac{1}{C_2 \Delta_C} \\
C_{DS} &= \frac{1}{C_1 \Delta_C} \\
C_{GD} &= \frac{1}{C_3 \Delta_C} \\
\Delta_C &= \frac{1}{C_1 C_2} + \frac{1}{C_1 C_3} + \frac{1}{C_2 C_3}.
\end{aligned} \tag{4.1}$$

This new equivalent star network allows direct extraction of its parameters from Z-parameter measurements. The following equations can be used to compute the three different branch impedance elements,

$$\begin{aligned}
Z_1 &= R_G + j\omega L_G - \frac{j}{\omega C_1} \\
Z_2 &= R_D + j\omega L_D - \frac{j}{\omega C_2} \\
Z_3 &= R_S + j\omega L_S - \frac{j}{\omega C_3}.
\end{aligned} \tag{4.2}$$

These branch impedances can be computed directly from the measured Z-parameters with the following set of equations [37],



$$\begin{aligned}
Z_1 &= z_{11} - z_{12} \\
Z_2 &= z_{22} - z_{12} \\
Z_3 &= z_{12}.
\end{aligned} \tag{4.3}$$

The parasitic series resistances will simply be the real parts of the calculated branch impedances. The series inductance and capacitance values must be extracted by analyzing the frequency dependence of the imaginary parts. For example, from Z_1 multiplied by ω the following equation is obtained,

$$\omega \text{Im}(Z_1) = \omega^2 L - \frac{1}{C} \tag{4.4}$$

A simple least-squares fit can be used to fit the measured Z-parameter data, enabling the calculation of the capacitance and inductance with Equation 4.4. The same applies to the other

two extracted impedances Z_2 and Z_3 , therefore obtaining all six reactive elements directly from measured data. The final device capacitances are transformed back to a delta network with Equation 4.1.

The procedure described above was implemented in the Matlab environment to obtain initial values for the model shown in Figure 4.11. The initial model is compared with the transistor measured data after the packages parameters are de-embedded. This comparison was performed in Microwave Office. The initial models fit could be improved with Microwave Office tuners or optimisers.

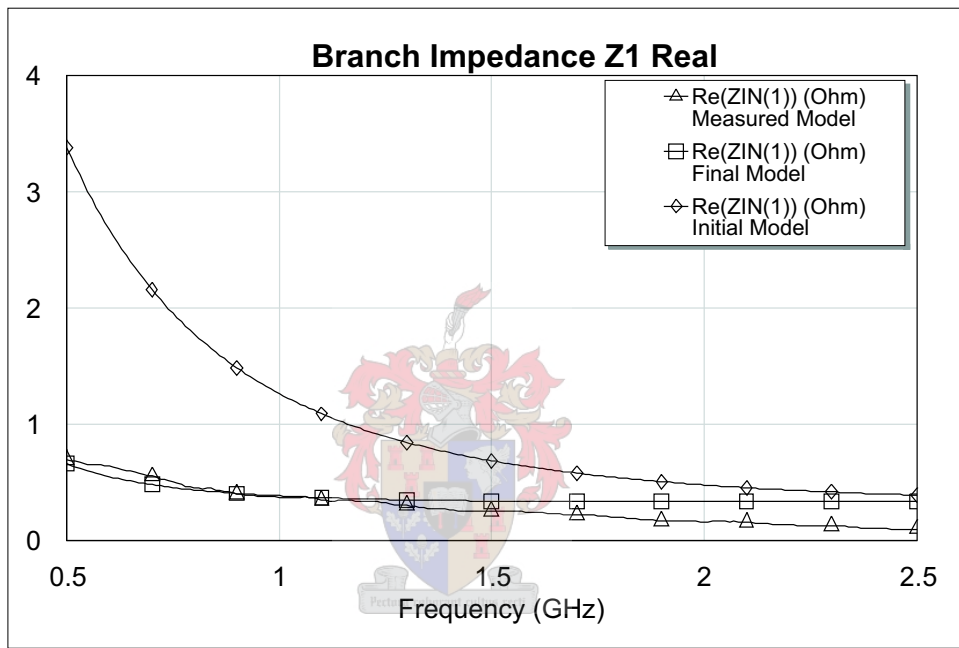


Figure 4.12: A comparison between the measured Z_1 series branch impedance, the trace marked Measured Model (\triangle marker), and the extrinsic final equivalent circuit model, the trace marked Final Model (\square marker), and the extrinsic initial model, the trace marked Initial Model (\diamond marker).

Figures 4.12 to 4.17 illustrate the comparison between the branch impedances obtained with the calculations above and the measured impedances. The traces marked Measured Model (\triangle marker), are the different measured branch impedances after the package model obtained in Section 4.2, was de-embedded. The traces marked Initial Model (\diamond marker), are the different branch impedances calculated in Matlab to obtain initial values for the series RLC circuits [38]. The traces marked Final Model (\square marker) represents the final fine-tuned branch impedances. The simple model representation for the cold FET, as shown in Figure 4.11, could only be fitted up to 2.5 GHz, a more complex model should be used to fit higher frequencies. A close fit for both the real and imaginary parts between the modeled and measured data is obtained up to a

frequency of 2.5 GHz.

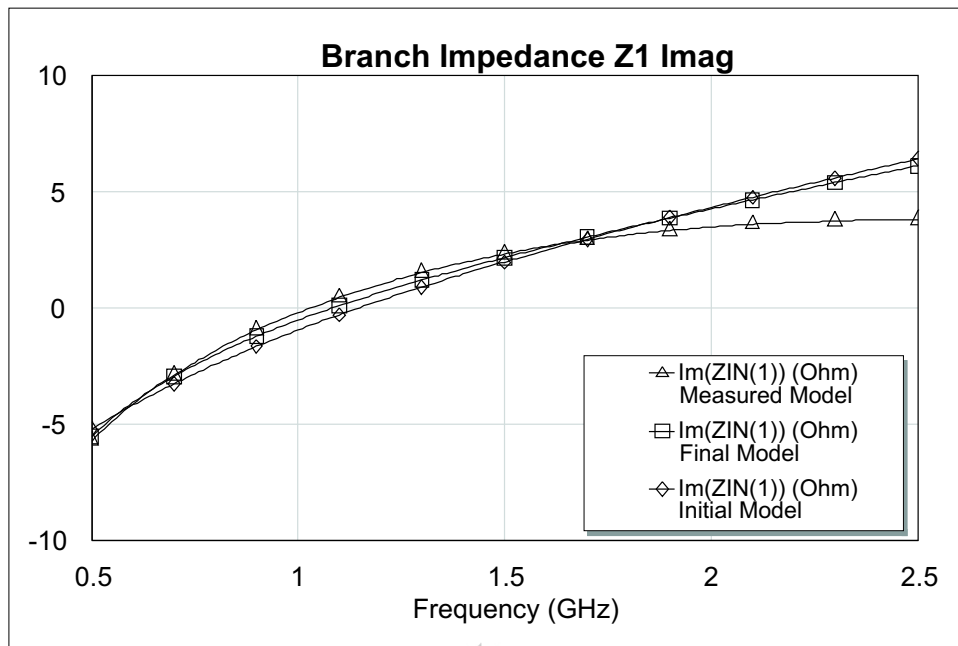


Figure 4.13: A comparison between the measured Z_1 series branch impedance, the trace marked Measured Model (\triangle marker), and the extrinsic final equivalent circuit model, the trace marked Final Model (\square marker), and the extrinsic equivalent initial model, the trace marked Initial Model (\diamond marker).

Figures 4.18 to 4.20 illustrate the measured and modeled S-parameter comparison for the cold FET model. Notice that in each of these figures the Matlab model, calculated with Equations 4.1 to 4.4, is an acceptable starting point. Figure 4.19 show that there is a 20 dB difference between the initial models transmission amplitude and the measurement. Figure 4.20 shows that the transmission phase difference between these two models are 20° . The final fine-tuned model in Microwave Office provides an excellent match between modeled and measured data. The magnitude and phase difference between measured and final model data are less than 1 dB and 5° , respectively.

The extrinsic model for one of Motorola's LDMOS RF power transistors has been extracted. The transistor was packaged in a metal-ceramic package (case 360B-05) and compared with a Motorola LDMOS RF power transistor packaged in a metal-ceramic package (case 360B-01) [7]. The transistor contains 24 active cells and the package contains 12 gate bond-wires and 13 drain bond-wires. The gate and drain bond-wires are non-symmetrical, explaining the difference between gate and drain impedances. The different values obtained for the model illustrated in Figure 4.11 are listed in Table 4.1.

The comparison between the initial calculated and the fine-tuned values are very good. The

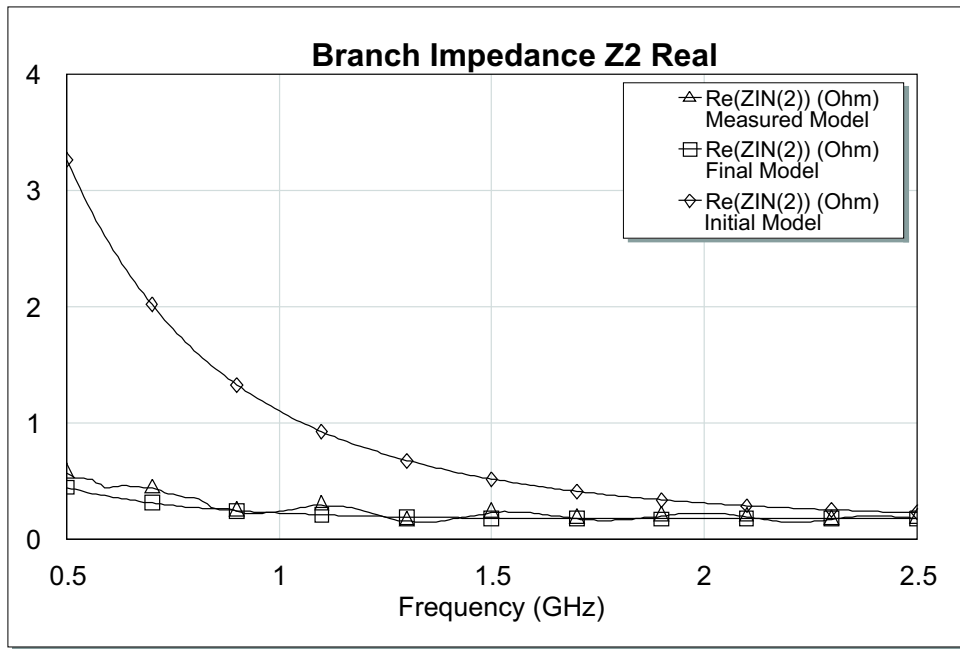


Figure 4.14: A comparison between the measured Z_2 series branch impedance, the trace marked Measured Model (\triangle marker), and the extrinsic final equivalent circuit model, the trace marked Final Model (\square marker), and the extrinsic initial model, the trace marked Initial Model (\diamond marker).

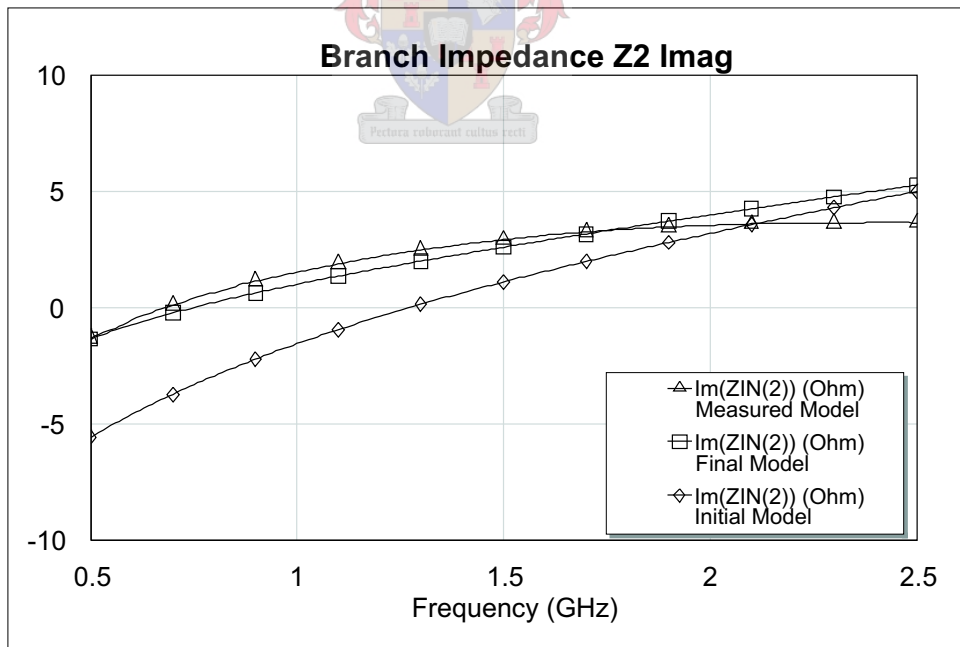


Figure 4.15: A comparison between the measured Z_2 series branch impedance, the trace marked Measured Model (\triangle marker), and the extrinsic final equivalent circuit model, the trace marked Final Model (\square marker), and the extrinsic initial model, the trace marked Initial Model (\diamond marker).

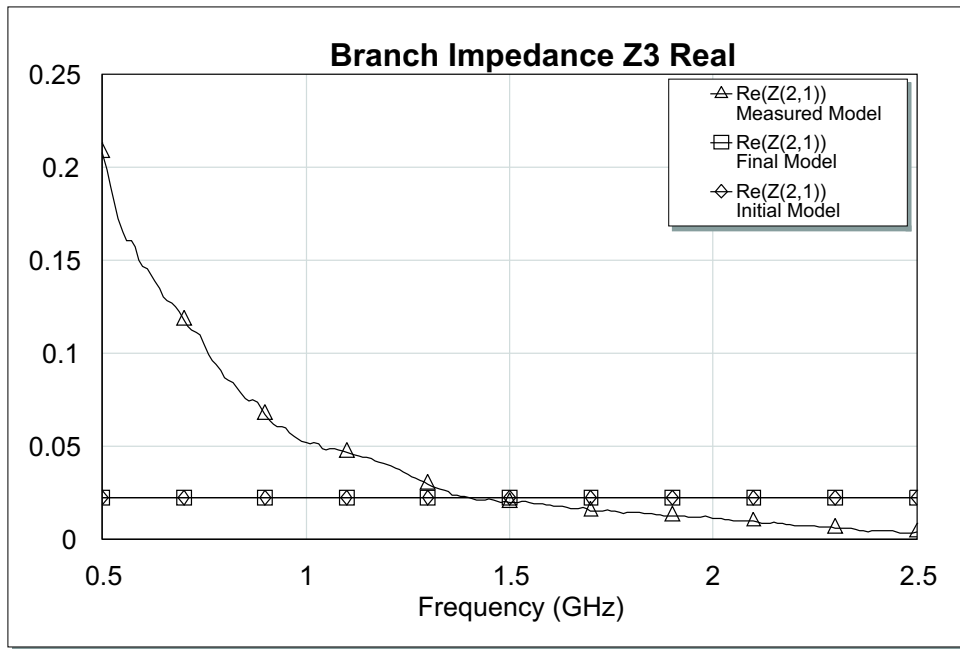


Figure 4.16: A comparison between the measured Z_3 series branch impedance, the trace marked Measured Model (\triangle marker), and the extrinsic final equivalent circuit model, the trace marked Final Model (\square marker), and the extrinsic initial model, the trace marked Initial Model (\diamond marker).

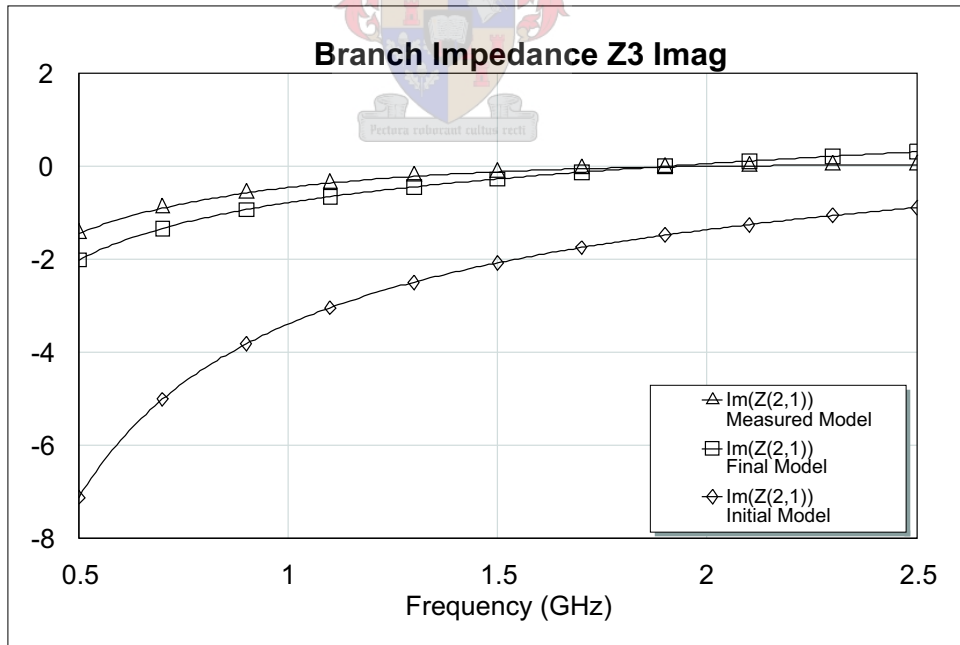


Figure 4.17: A comparison between the measured Z_3 series branch impedance, the trace marked Measured Model (\triangle marker), and the extrinsic final equivalent circuit model, the trace marked Final Model (\square marker), and the extrinsic initial model, the trace marked Initial Model (\diamond marker).

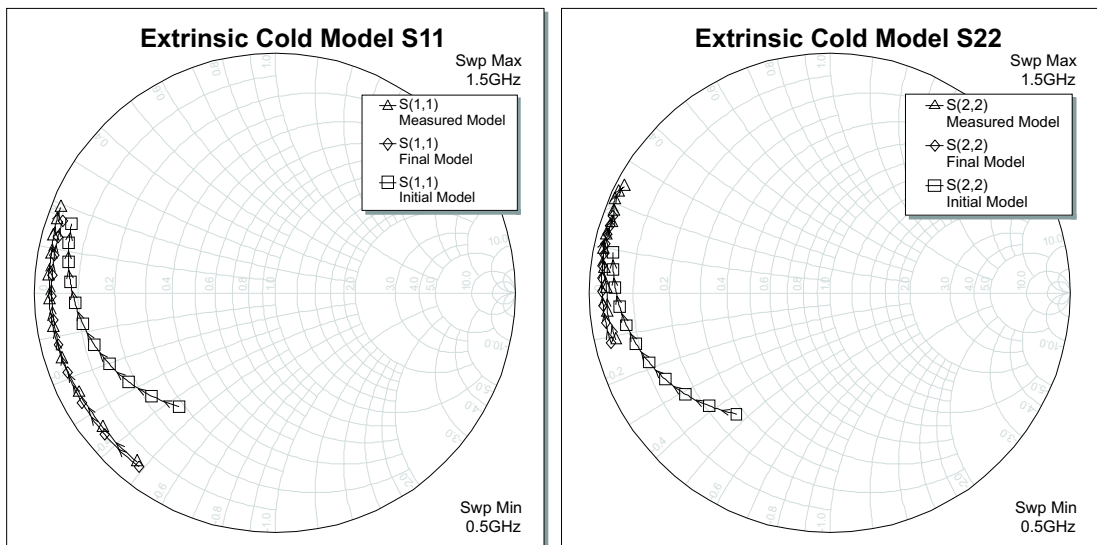


Figure 4.18: A comparison between the measured extrinsic cold models input and output reflections, traces marked Measured Model (Δ marker), and the extrinsic final equivalent circuit models input and output reflections, traces marked Final Model (\diamond marker), and the extrinsic initial models input and output reflections, traces marked Initial Model (\square marker). These S-parameters are illustrated on a 12-ohm Smith chart.

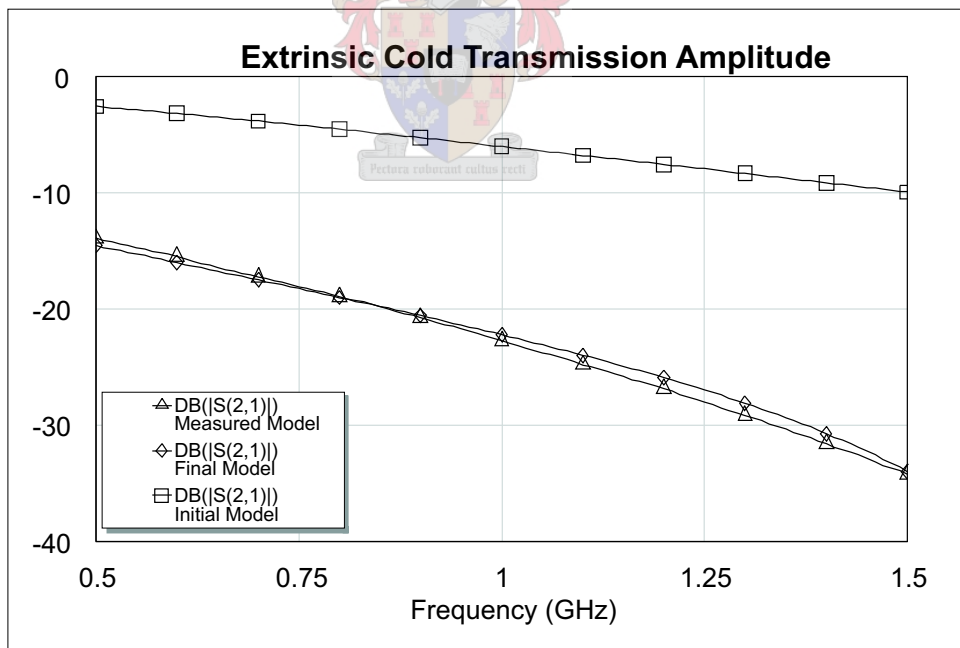


Figure 4.19: A comparison between the measured extrinsic cold de-embedded transmission magnitude, the trace marked Measured Model (Δ marker), and the extrinsic final circuit model transmission magnitude, the trace marked Final Model (\diamond marker), and the extrinsic initial model transmission magnitude, the trace marked Initial Model (\square marker).

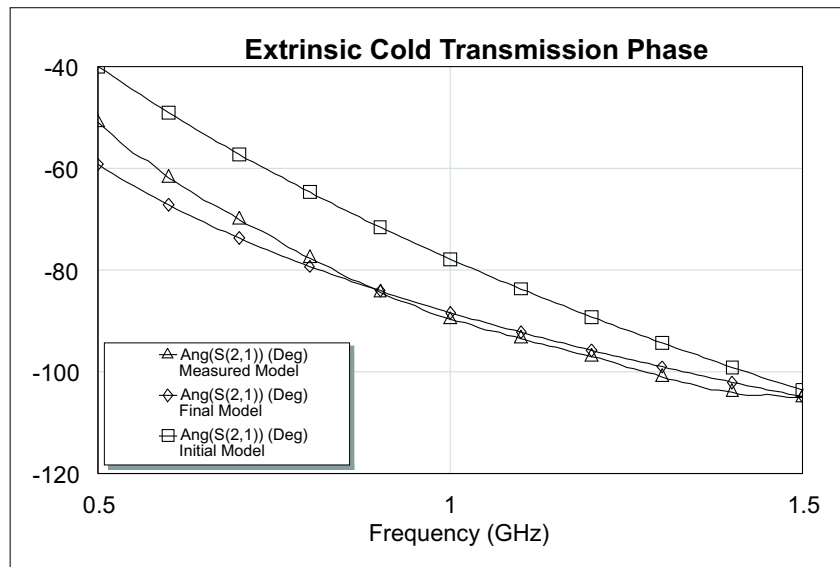
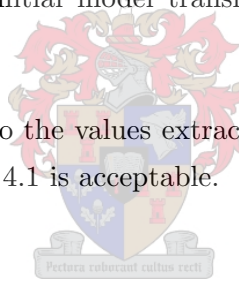


Figure 4.20: A comparison between the measured extrinsic cold de-embedded transmission phase, the trace marked Measured Model (\triangle marker), and the extrinsic final circuit model transmission phase, the trace marked Final Model (\diamond marker), and the extrinsic initial model transmission phase, the trace marked Initial Model (\square marker).

fine-tuned values were compared to the values extracted for a similar Motorola transistor, and the comparison as shown in Table 4.1 is acceptable.



4.4 Intrinsic Parameter Extraction

The final step to complete the equivalent circuit model for the LDMOS transistor, illustrated in Figure 4.1, is to extract the intrinsic element circuit. These small-signal equivalent circuit parameters are all functions of the biasing conditions [39]. The intrinsic model, illustrated in Figure 4.21 presents a PI topology. It is convenient to use the admittance (Y) parameters to characterise the intrinsic model's electrical properties. All the extrinsic elements, extracted in Sections 4.2 and 4.3, are known. The S-parameter measurements of the transistor, measured with active bias conditions, can be transformed into Z- and Y-parameters to subtract the series and parallel extrinsic elements. After all the extrinsic elements are de-embedded the intrinsic Y-parameters are obtained.

The intrinsic model, illustrated in Figure 4.21, can be described by the following equations [41, 42],

	Initial Values	Fine-Tuned Values	Motorola's Extracted Values (case 360-01)
$R_g(\Omega)$	0.3130	0.3130	-
$R_d(\Omega)$	0.1550	0.1550	-
$R_s(\Omega)$	0.0226	0.0226	-
$L_g(\text{pH})$	484	432	490
$L_d(\text{pH})$	395	322	380
$L_s(\text{pH})$	35	47	64

Table 4.1: A comparison of the extracted parasitic series resistances and inductances of a 30-Watt Motorola RF power transistor.

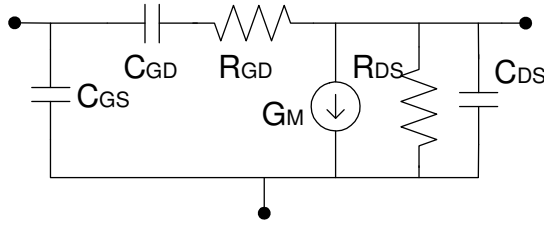


Figure 4.21: A representation of a LDMOS small-signal intrinsic equivalent circuit model [34, 4, 40, 35].

$$Y_{11} = \frac{C_{gs}^2 \omega^2}{D1} + \frac{\omega^2 R_{gd} C_{gd}^2}{D2} + j\omega \left(\frac{C_{gs}}{D1} + \frac{C_{gd}}{D2} \right) \quad (4.5)$$

$$Y_{12} = -\frac{\omega^2 R_{gd} C_{gd}^2}{D2} - j\omega \frac{C_{gd}}{D2} \quad (4.6)$$

$$Y_{21} = \frac{g_m e^{-j\omega\tau}}{1 + j\omega C_{gs}} - j \frac{\omega C_{gd}}{1 + j\omega R_{gd} C_{gd}} \quad (4.7)$$

$$Y_{22} = \frac{\omega^2 R_{gd} C_{gd}^2}{D2} + j\omega \left(C_{ds} + \frac{C_{gd}}{D2} \right) \quad (4.8)$$

where

$$D1 = 1 + \omega^2 C_{gs}^2 \quad (4.9)$$

$$D2 = 1 + \omega^2 C_{gd}^2 R_{gd}^2. \quad (4.10)$$

By separating these equations into their real and imaginary parts, the circuit elements of the small-signal equivalent circuit can be determined [41].

$$C_{gd} = -\frac{Im(Y_{12})}{\omega} \left(1 + \left(\frac{Re(Y_{12})}{Im(Y_{12})} \right)^2 \right) \quad (4.11)$$

$$C_{gs} = \frac{Im(Y_{11}) + Im(Y_{12})}{\omega} \left(1 + \frac{(Re(Y_{11}) + Re(Y_{12}))^2}{(Im(Y_{11}) + Im(Y_{12}))^2} \right) \quad (4.12)$$

$$C_{ds} = \frac{Im(Y_{22}) + Im(Y_{12})}{\omega} \quad (4.13)$$

$$R_{ds} = \frac{Im(Y_{22}) + Im(Y_{12})}{\omega} \quad (4.14)$$

$$R_{gd} = \frac{Re(Y_{12})}{\omega C_{gd} Im(Y_{12})} \quad (4.15)$$

$$g_m = \sqrt{((Re(Y_{21}) - Re(Y_{12}))^2 + (Im(Y_{21}) + Im(Y_{12}))^2) D1} \quad (4.16)$$

$$\tau = \frac{1}{\omega} \arcsin \left(\frac{Im(Y_{12}) - Im(Y_{21}) - \omega C_{gs} (Re(Y_{21}) - Re(Y_{12}))}{g_m} \right) \quad (4.17)$$

The voltage dependent current generator in the transistor model can be represented by the following equations [35, 43, 42],

$$i_{ds} = V_i g_m e^{-j\omega\tau} \quad (4.18)$$

$$\begin{aligned} &= V_i (g_m \cos(\omega\tau) - j g_m \sin(\omega\tau)) \\ &= V_i \left(g_m \cos(\omega\tau) - j \omega g_m \tau \frac{\sin(\omega\tau)}{\omega\tau} \right) \\ &\approx V_i (g_m - j \omega g_m \tau) \text{ when } \tau \ll 1 \end{aligned}$$

$$i_{ds} = V_i (g_m + j\omega C_m) \text{ where } C_m \equiv -g_m \tau, \quad (4.19)$$

where C_m represents the transc capacitance. The transc capacitance is calculated because Equation 4.19 is used to describe the final active non-linear intrinsic model. Equations 4.11 through 4.19 are valid for all LDMOS bias conditions, and for all frequencies for which the equivalent circuit, illustrated in Figure 4.21, is valid.

The intrinsic model elements are bias dependent. Figures 4.22 to 4.25 present these extracted values under different gate and drain bias conditions. With Equations 4.5 to 4.19 initial values can be obtained for these elements, which are very close to the final solutions. The Microwave Office optimisation procedure is used to fine-tune the initial values, which is very fast and rapidly converges to the final values. Figures 4.22 and 4.25 illustrates the measured $C_{gs}(V_{GS}, V_{DS})$, $C_{ds}(V_{GS}, V_{DS})$ and $C_{gd}(V_{GS}, V_{DS})$ curves for the LDMOS transistor. These figures indicate that C_{gd} and C_{ds} has a low dependence on V_{GS} . The extracted C_{ds} capacitance is very useful for designing amplifiers operating in either class-AB, class-B or class-C mode.

Figure 4.22 shows the extracted drain and gate bias dependencies of C_{gs} and C_{ds} . The extracted C_{gs} data shows a very smooth and continuous trend, varying with only 9 pF. Figure 4.23 shows the extracted parameters representing the voltage dependent current generator, as described by Equation 4.19. Below pinch-off the transistor has no gain and both g_m and C_m are zero, while in the active operating region the transistor produces gain and both g_m and C_m are non-zero. The transcapacitance (C_m) represents the phase response of the voltage dependent current generator and can take on negative values as illustrated in Figure 4.23. This capacitance has the largest influence on the transmission phase response of the intrinsic small-signal model response. Figure 4.24 shows the extracted intrinsic resistances, R_{gd} and R_{ds} . The gate-drain resistance (R_{gd}) represents the gate-drain time-delay in the non-quasi-static model. This parameter is very unstable and very sensitive to extract. A value for this parameter was extracted, but appears not to have any influence on the final intrinsic model. The drain-source resistance (R_{ds}) represents the slope of the $I_{ds} - V_{ds}$ curve. Below pinch-off this resistance is taken to be an open circuit, while in the active region the resistance decreases.

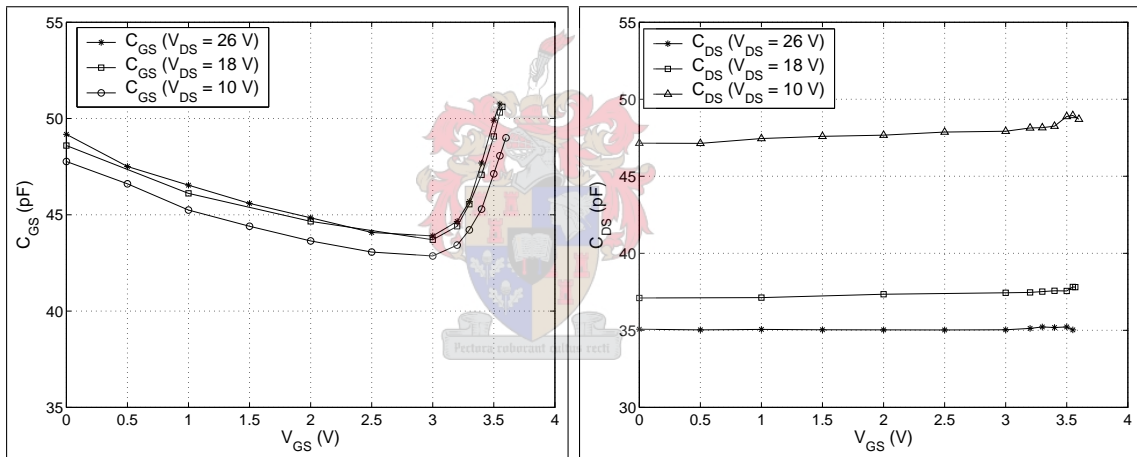


Figure 4.22: The extracted C_{gs} and C_{ds} capacitances at multiple biasing conditions.

The intrinsic equivalent model together with extrinsic and package model parameters were implemented in Microwave Office to obtain the complete equivalent circuit model for the LDMOS transistor. Figures 4.26 and 4.28 illustrate the S-parameter comparison between the initial model, traces marked LDMOS Initial Model (\diamond marker), the final fine-tuned model, traces marked LDMOS Final Model (\triangle marker), and the transistors measured S-parameters, traces marked LDMOS Measurement (\square marker). The input and output reflections between the modeled and measured data correlate very well up to 1.5 GHz. The initial model's transmission magnitude and phase data compares tolerably with the measured data. The final fine-tuned model compares exceptionally well with the measured data. The worst magnitude difference between fine-tuned modeled and measured transistor is less than 1.5 dB, and the worst phase

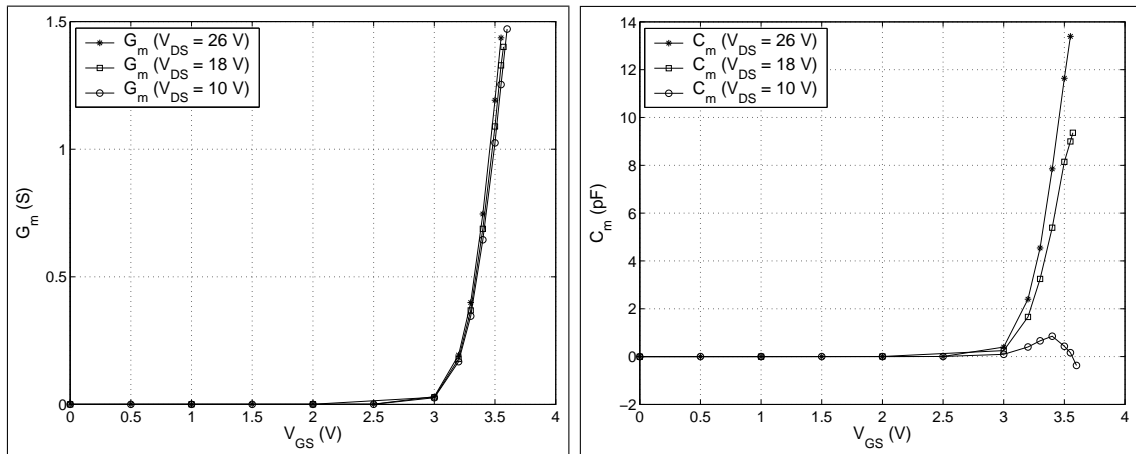


Figure 4.23: The extracted G_m and C_m parameters for the voltage dependent current generator at multiple biasing conditions.

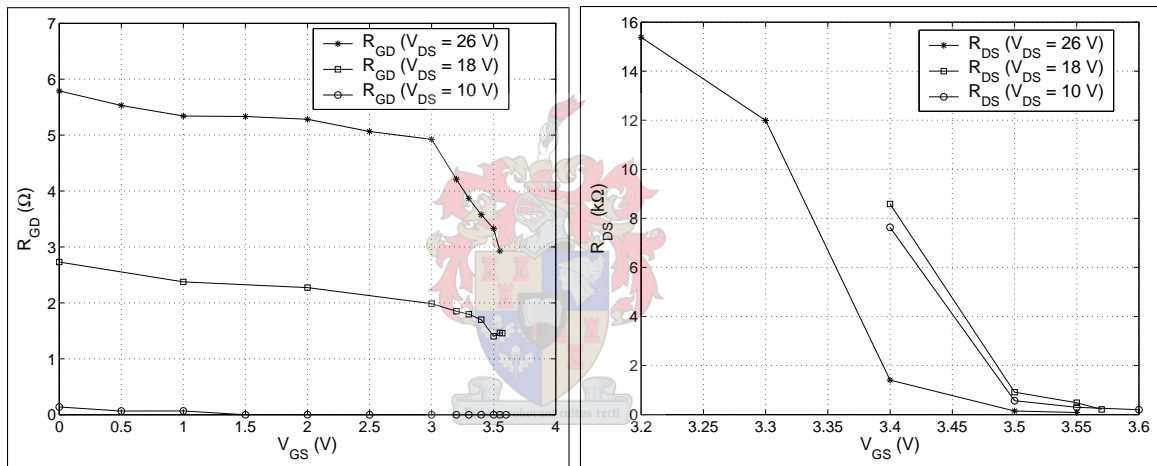


Figure 4.24: The extracted R_{gd} and R_{ds} resistances at multiple biasing conditions.

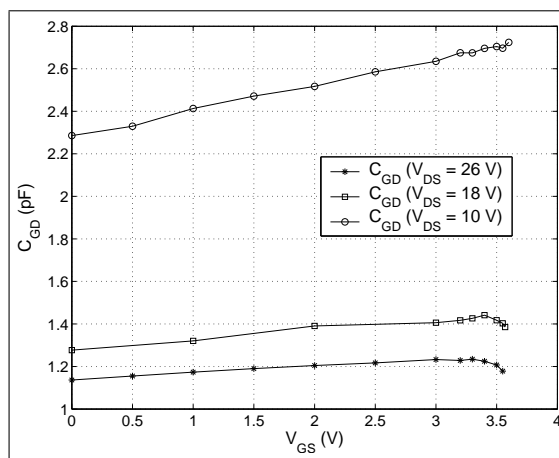


Figure 4.25: The extracted C_{gd} capacitance at multiple biasing conditions.

difference is less than 10° .

	Initial Values	Fine-Tuned Values	Motorola Datasheet Values (MRF9030)
C_{gs} (pF)	50.8	48	49.5
C_{ds} (pF)	35	36.3	26.5
C_{gd} (pF)	1.18	0.84	1.0
R_{gd} (Ω)	2.93	-	-
R_{ds} (Ω)	87.1	90	-
G_M (S)	1.55	1.9	-
C_M (pF)	13.4	-	-

Table 4.2: A comparison of the extracted LDMOS intrinsic parameters of a 30-Watt Motorola RF power transistor.

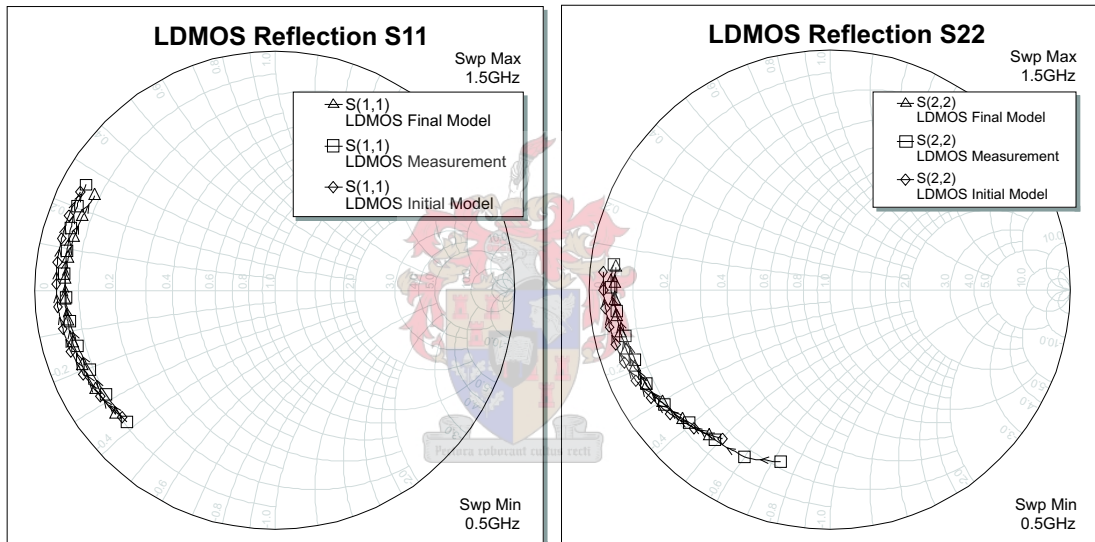


Figure 4.26: A comparison between the measured intrinsic input and output reflections, traces marked LDMOS Transistor Measured (\square marker), and the Microwave Office complete circuit model input and output reflections, traces marked LDMOS MWO Model (\triangle marker), and the Matlab starting model input and output reflections, traces marked LDMOS Matlab Model (\diamond marker).

The initial and fine-tuned values extracted for the intrinsic model are given in Table 4.2. These values were extracted at $V_{gs} = 3.5$ V and $V_{ds} = 26$ V, which is the quiescent bias point of a class-AB amplifier. The initial values and the fine-tuned values compares very well. The fine-tuned intrinsic capacitors are compared to the transistor's data sheet capacitor values. The data sheet values were obtained with capacitance-voltage measurements performed on a LCR meter at 1 MHz, and compares very well with the extracted fine-tuned values.

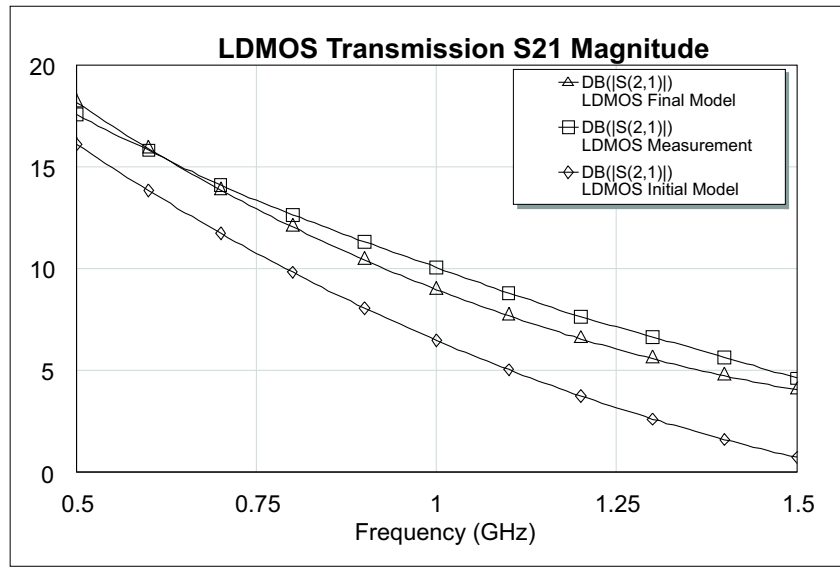


Figure 4.27: A comparison between the measured intrinsic transmission magnitude, traces marked LDMOS Transistor Measured (\square marker), and the Microwave Office complete circuit model transmission magnitude, traces marked LDMOS MWO Model (Δ marker), and the Matlab starting model transmission magnitude, traces marked LDMOS Matlab Model (\diamond marker).

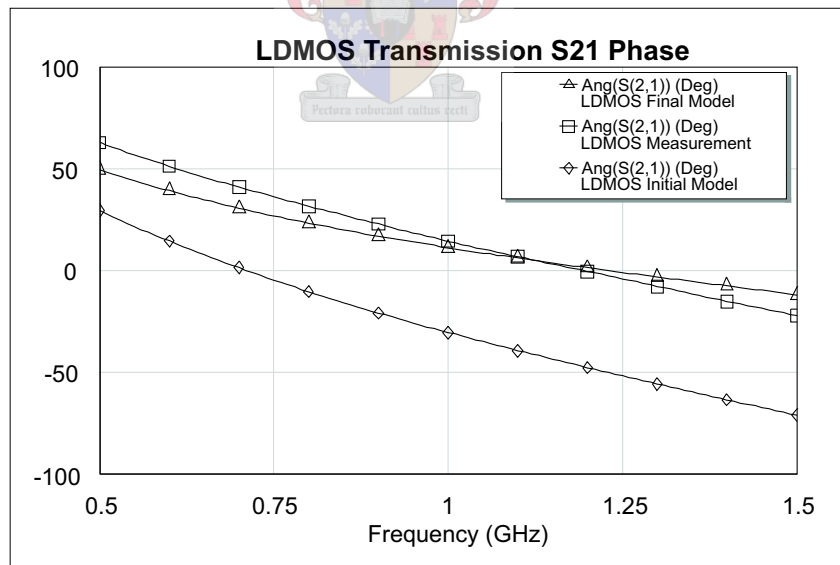


Figure 4.28: A comparison between the measured intrinsic transmission phase, traces marked LDMOS Transistor Measured (\square marker), and the Microwave Office complete circuit model transmission phase, traces marked LDMOS MWO Model (Δ marker), and the Matlab starting model transmission phase, traces marked LDMOS Matlab Model (\diamond marker).

4.5 Conclusion

This chapter presents an extended small-signal equivalent circuit for LDMOS transistor parameter extraction. It includes both the extrinsic and intrinsic elements of the transistor. The extrinsic elements represent the metal-ceramic transistor package and the bond-wires of the device, while the intrinsic element model the transistor-die. These parameters were extracted with various parameter extraction techniques to obtain starting values for equivalent circuit models. These models were fine-tuned in a commercialized software package (Microwave Office) to obtain the final model parameters.

The small-signal operation of a 30-Watt Motorola (MRF9030) LDMOS transistor was presented and compared with its measurements. The modeled S-parameters have a good correspondence with the measured S-parameters. With the presented small-signal equivalent circuit various techniques can be used to design class-AB or class-B amplifier circuits.



Chapter 5

Class-AB Amplifier Design

5.1 Introduction

Power amplifiers are the main power consumption blocks in any advanced wireless communication system. Power amplifiers are often biased in class-AB operation to compromise between linearity and power-added efficiency (PAE) [44]. This operation will increase the lifetime of the battery, and reduce the size and weight of the heat sink. In addition, class-AB operation is often used in push-pull configurations, to eliminate the crossover distortion that may be introduced when biased in class-B operation [45].

To verify the LDMOS small-signal equivalent circuit extracted in the previous chapter, a 945 MHz class-AB power amplifier was designed, implemented and measured.

5.2 Class-AB Load Line Amplifier Designed with Line-Stub Matching

The small-signal equivalent circuit extracted in Chapter 4 together with Cripp's load line method, can be used to design a class-AB power amplifier [8, 46]. The main advantage of the load line method, is that it ensures maximum voltage and current swing. The next set of design steps was followed in the class-AB amplifier design procedure.

Step 1: Amplifier Specifications

A 19 dB, 30 Watt LDMOS Motorola transistor (MRF9030) was used to design a class-AB amplifier. The amplifier is designed to operate from 930 MHz to 960 MHz, with a center

frequency of 945 MHz. The amplifier was designed to operate over the same frequency band as the example amplifier in the Motorola data sheet, to be able to compare this designs operation to that of the Motorola data sheet test circuit. The design was implemented on the same substrate used in Section 3.3, Rogers 6010.2, ϵ_r of 9.95 (as extracted in Section 3.3) and height of 0.635 mm. The amplifiers quiescent DC bias point of class-AB operation is at $V_{DSQ} = 26$ V and $I_{DSQ} = 250$ mA ($V_{GSQ} = 3.5$ V).

Step 2: Establish R_{opt}

Cripp's method assumes that $V_{DSmax} = 2V_{DSQ}$ and that the designer has complete freedom in choosing the quiescent bias point for his amplifier design. The optimum load for class-AB operation can be approximated by,

$$R_{opt} = \frac{V_{DSQ} - V_{knee}}{\frac{I_{MAX}}{2}} \quad (5.1)$$

where V_{DSQ} is the drain supply voltage, V_{knee} is the transistor knee voltage and I_{MAX} is the maximum drain current. These values are obtained from the I_{DS} versus V_{DS} plot, illustrated in Figure 5.1. The values required for Equation 5.1 are obtained from Figure 5.1, resulting in:

- $V_{DSmax} = 26$ V
- $V_{knee} = 6$ V
- $I_{MAX} = 5.75$ A
- $R_{opt} = 6.956 \approx 7 \Omega$.

This load line is optimally placed, to provide the best voltage and current swing from the chosen quiescent bias point, thus maximising the output power.

Step 3: Design of the Output Matching Network

The next step is to calculate Z_{opt} . Z_{opt} is defined as the optimum impedance that the external output matching network must present to the intrinsic current source, so that the intrinsic current source will see a load resistance of R_{opt} , as illustrated in Figure 5.2. A simplified model, illustrated in Figure 5.2, is used to represent the internal reactances of the transistor. The only intrinsic capacitance that is taken into account in the calculation of Z_{opt} is C_{ds} . Intrinsic

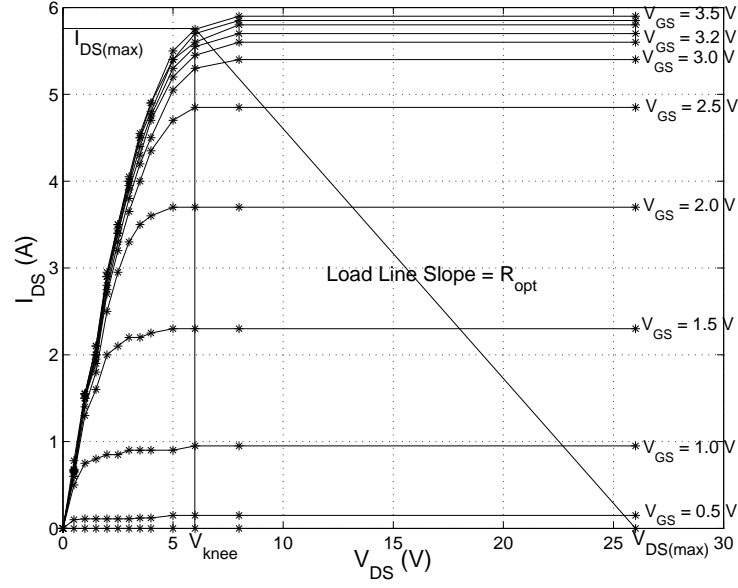


Figure 5.1: Measured current-voltage ($I_{DS} - V_{DS}$) characteristic curves for different V_{GS} voltages for a Motorola LDMOS transistor.

capacitor C_{gs} does not influence the value of Z_{opt} due to its position in the equivalent circuit model, and C_{gd} is small, making its effect on the device output impedance negligible [47]. The remaining elements in the drain extrinsic network represent the drain bond-wires and drain lead parameters, also shown in Figure 5.2.

One approach to determine Z_{opt} is to terminate the extrinsic network with a complex impedance, the value of which is optimised till a load of R_{opt} (7Ω) is seen at the intrinsic ideal current source I_{ds} . A gradient optimiser from a commercialised software package (Microwave Office) was used to obtain this solution. The value of Z_{opt} , determined at the center frequency (945 MHz), in this way is,

$$Z_{opt} = 1.17 + j1.15 \quad (5.2)$$

Once Z_{opt} is known, various matching techniques can be used to design a matching network that will transform 50 Ohm to Z_{opt} and vice versa. With this technique it is advised to start with the design of the drain biasing network, since this network will have a noticeable influence on the output matching network.

The input impedance of the bias network must be as high as possible at the center frequency, this being the reason for the narrow quarter-wave transmission line (TL1), as illustrated in Figure 5.3. This high impedance is to prevent the RF signal from making its way up to the supply and

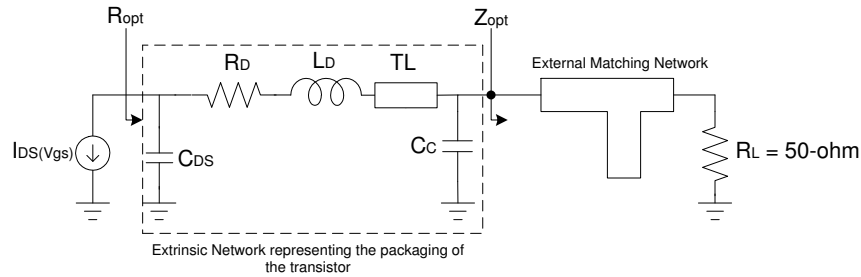


Figure 5.2: A schematic representation for determining Z_{opt} from R_{opt} .

form a potentially disastrous feedback path. A series resistor-capacitor combination is placed in parallel with two capacitors in the biasing network. This circuit brings a dissipating element in parallel to the decoupling capacitors and improves the stability of the amplifier [48, 46]. A large 2200 μF capacitor is placed directly next to the V_{DS} supply, to produce enough current should the amplifier be tested in pulsed mode.

For the drain matching circuit (illustrated in Figure 5.3), the series transmission line (TL2) and shunt transmission line stub (TL2) were used to transform Z_{opt} to 12 Ohm. The second series transmission line (TL3) was implemented as a transformer to transform from a low impedance to a higher impedance closer to 50 Ohm. Transmission line TL4 runs to the edge of the circuit board, at which point an impedance of 50 Ohm is established. Normal practice would be to run a 50 Ohm transmission line to the edge of the physical circuit board, but a 50 Ohm line on the chosen substrate has a width of only 0.591 mm. Given that the SMA connector used has a center pin with a 1.2 mm cross section, this would create an unacceptably large discontinuity at the co-axial to microstrip transition. The width of transmission line TL4 was fixed at 1.2 mm.

The drain bias and matching circuit was implemented in Microwave Office and fine-tuned. The final matching circuit transmission line widths and lengths are shown in Figure 5.3. R_{opt} calculated with this circuit is shown in Figure 5.4. The real value of R_{opt} at the center frequency is 6.919 Ohm, varying with 2.7 Ohm over the design frequency band, while the imaginary value is at worst 0.377 Ohm.

Step 4: Design of the Input Matching Network

Once the load network is known, the last step is to design the input matching network. The input matching circuit is designed by determining Z_{in} , the input impedance of the device S-parameters terminated with the load network designed in the previous section, as illustrated in Figure 5.5. The design of the gate bias and matching network follows the same procedure as a conjugate match design. For a conjugate match, maximum power transfer from the input

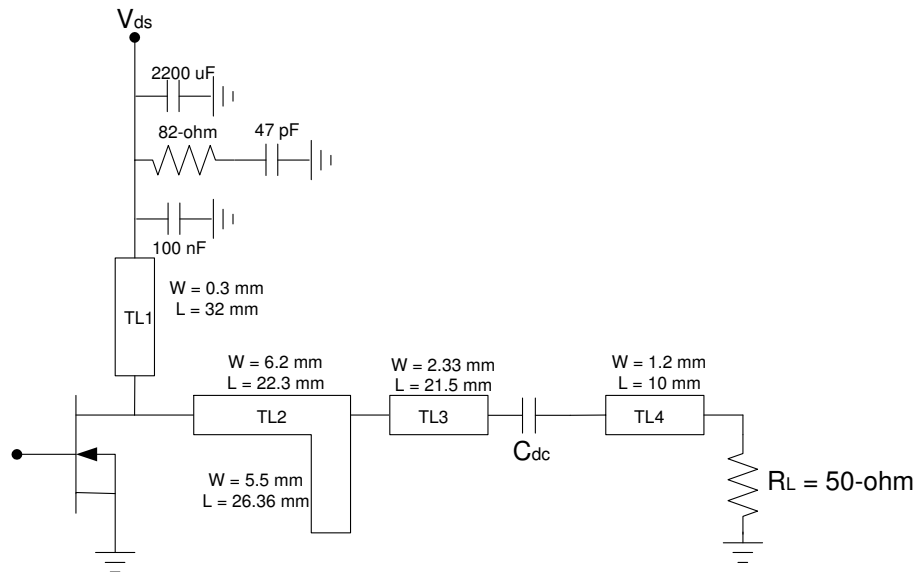


Figure 5.3: A schematic of the drain bias and matching circuit for the class-AB amplifier.

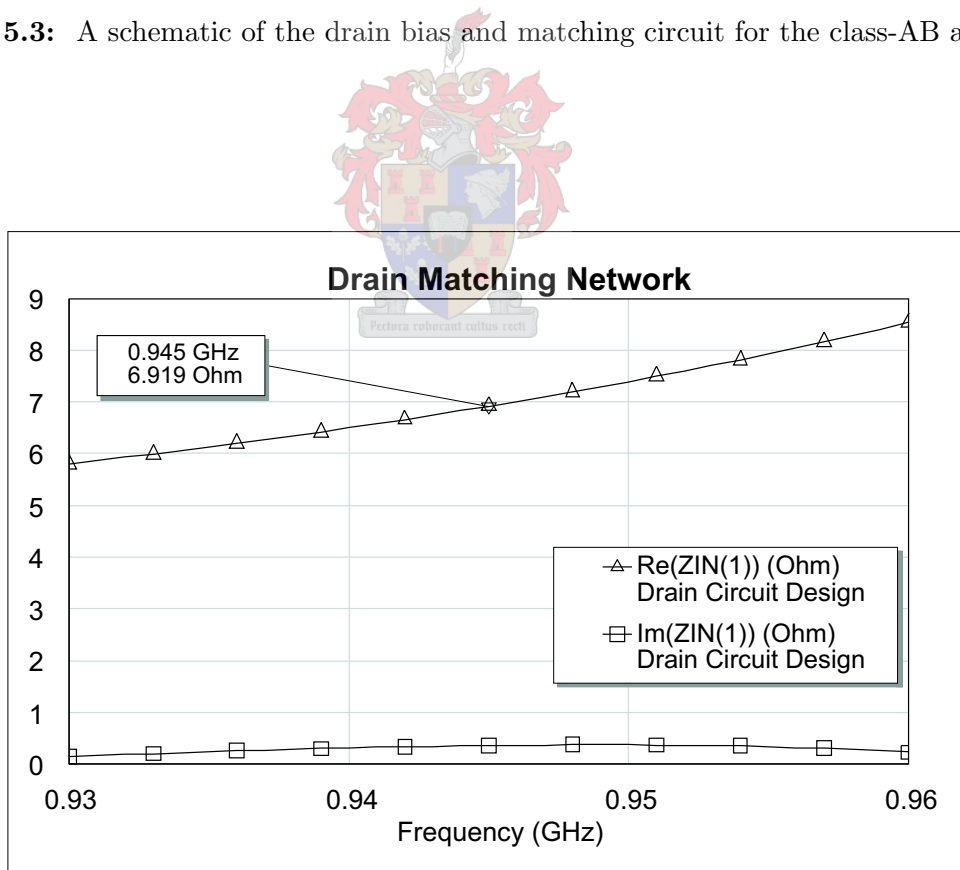


Figure 5.4: The real and imaginary parts of R_{opt} for the drain matching circuit.

matching network to the transistor at the center frequency will occur when [9],

$$Z_{in} = Z_S^* \quad (5.3)$$

$$= 0.78442 - j1.1931. \quad (5.4)$$

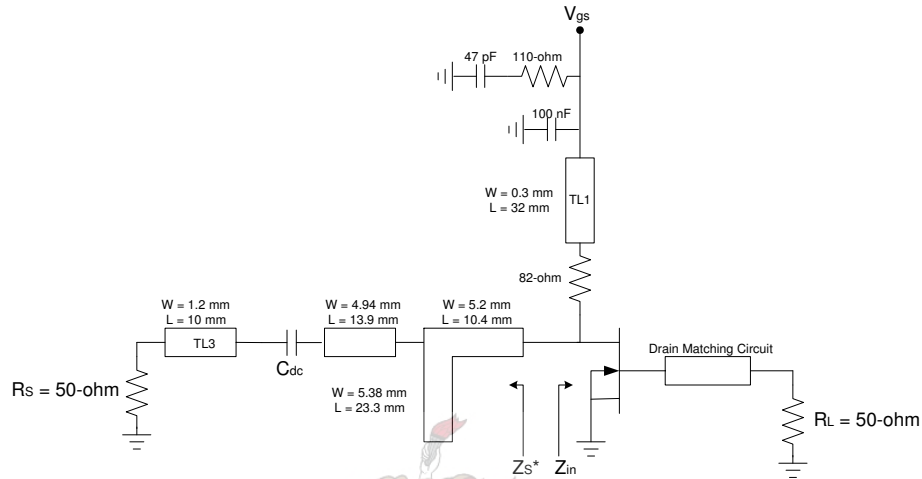


Figure 5.5: A schematic of the gate bias and matching circuit for the class-AB amplifier.

As in the drain bias network case, the input impedance of the gate bias network must be as high as possible at the center frequency, this being the reason for the 82 Ohm resistance and the narrow quarter-wave transmission line (TL1). This high impedance is to prevent the RF signal from making its way up to the supply and form a potentially disastrous feedback path. A resistor in series with a capacitor is placed in the biasing network. This circuit brings a dissipating element in parallel to the decoupling capacitors and improves the stability of the amplifier [48, 46].

The gate matching circuit consists of a series transmission line (TL2) and a shunt transmission line stub (TL2) to transform Z_{in}^* to 12 Ohm. The second series transmission line (TL3) is used as a transformer to transform the low impedance to a higher impedance closer to 50 Ohm. As in the drain matching circuit, the last series transmission line (TL4) was fixed at a width of 1.2 mm to match the SMA connector pin width.

Figure 5.6 shows the simulated S-parameters of the class-AB amplifier. The input reflection (Δ marker) is -47.3 dB at the center frequency and -20 dB across the design frequency band. The output reflection (\diamond marker) is only -1 dB, as expected, since the output matching circuit is designed for a specific load line. The small-signal gain (\square marker) across the design frequency band vary with less than a 1 dB and is simulated as 20.8 dB.

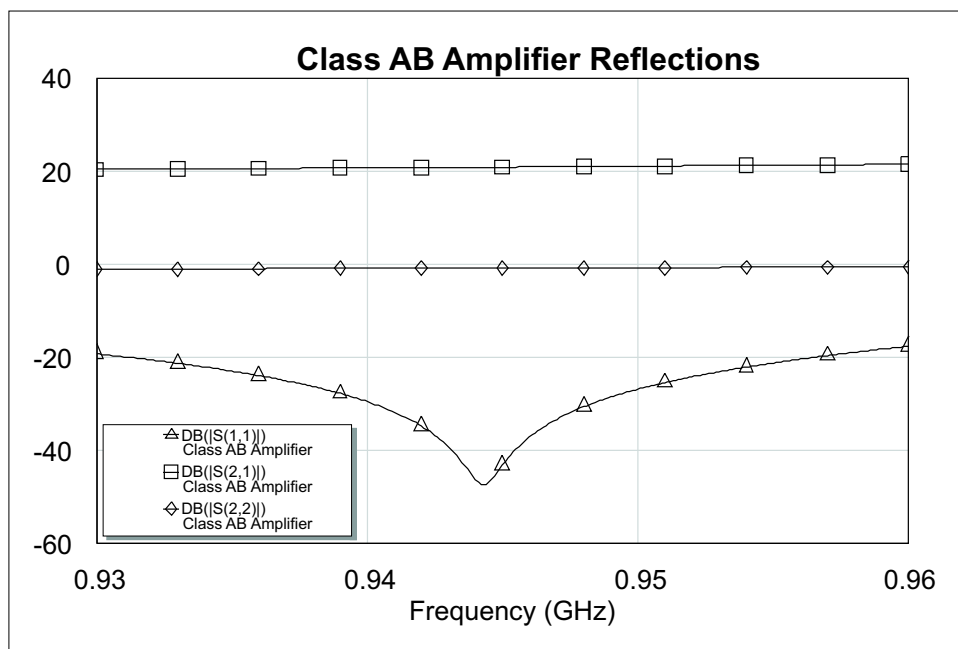


Figure 5.6: The simulated class-AB amplifier input reflection (Δ marker), output reflection (\diamond marker) and gain (\square marker).

Step 5: Generation of the Physical Layout

The final step is to generate a layout and build the circuit. Both the class-AB power amplifier and Motorola test circuit layouts are shown in Appendix C. The layout of the class-AB power amplifier was directly generated from the simulation environment of Microwave Office, while the Motorola test circuit schematic is available in the data sheet. The physical layout of the Motorola test circuit was also available in electronic format from Motorola's web-site [49].

5.3 Class-AB Load Line Amplifier Designed with Quarter-Wave Transformer Matching

A second class-AB amplifier was designed. This amplifier's specifications and quiescent bias point is the same as previously described in Section 5.2, step 1 and 2. The aim with the second design is to use a different method of matching and to ensure that the amplifier circuit is unconditionally stable. Quarter-wave transformers were used to match the input and output of the second design amplifier. The next set of design steps was followed in the second class-AB amplifier design procedure.

Step 1: Design of the Output Matching Network

Since the amplifier specifications and quiescent bias point remains the same the optimum impedance, Z_{opt} as given in Equation 5.2, also remains unchanged. The same drain bias network as in the previous design with unchanged component values was used for this amplifier. For the drain matching circuit (illustrated in Figure 5.7), quarter-wave transformers (TL2) were used to first transform Z_{opt} to 12 Ohm and then to 50 Ohm. The width of the last series transmission line (TL3) was fixed at 1.2 mm, again to match the SMA connector pin width.

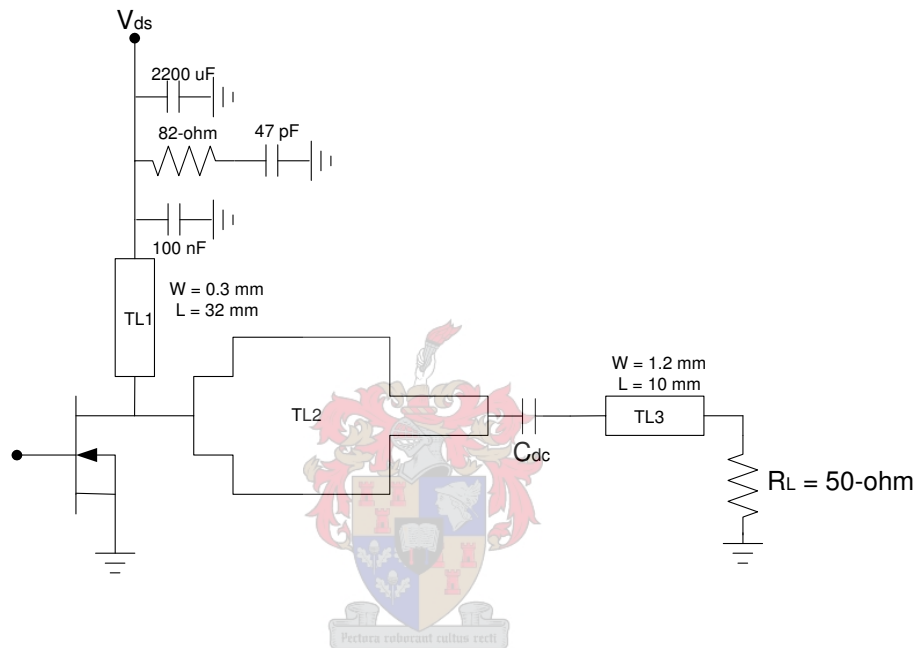


Figure 5.7: A schematic of the drain bias and matching circuit for the class-AB amplifier.

The drain bias and matching circuit was implemented in Microwave Office and fine-tuned. R_{opt} calculated with this circuit is shown in Figure 5.8. The real value of R_{opt} at the center frequency is 7.03 Ohm, varying with 0.9 Ohm over the design frequency band, while the imaginary value is 0.346 Ohm at the center frequency. Compared to the previous matching circuit design, this design presents better simulated results.

Step 2: Design of the Input Matching Network

The input matching network is designed by determining Z_{in} , the input impedance resulting from the device S-parameters terminated by the drain matching network, as shown in Figure 5.9. Again the same gate bias network as in the previous design was used in this design, as shown in Figure 5.9. The gate matching circuit consists of quarter-wave transformers (TL2) to first convert Z_{in} to 12 Ohm and then to 50 Ohm. As in the drain matching circuit, the last series transmission line (TL3) was fixed at a width of 1.2 mm to match the SMA connector pin width,

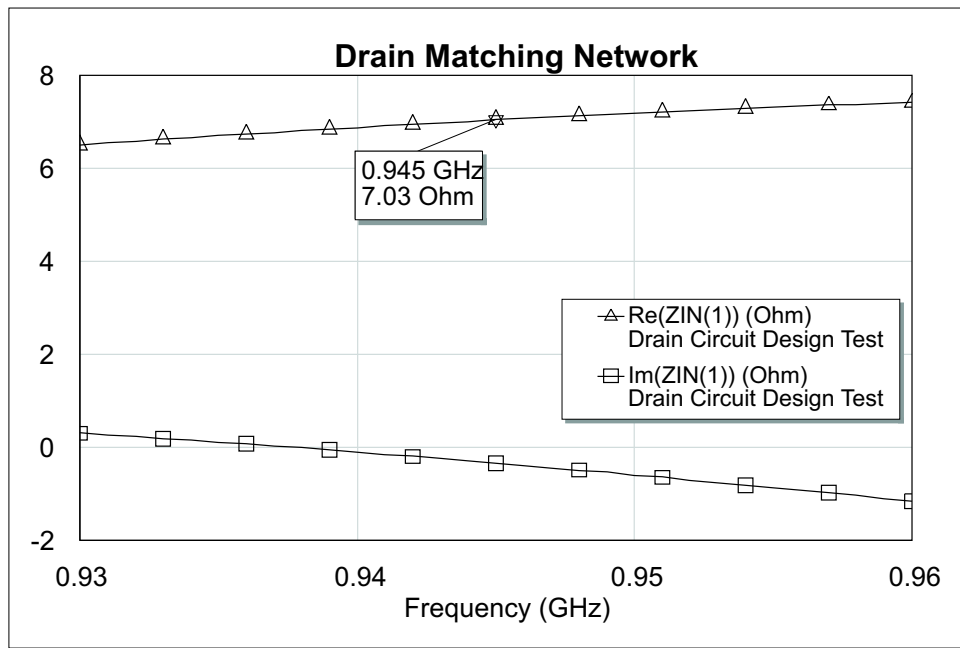
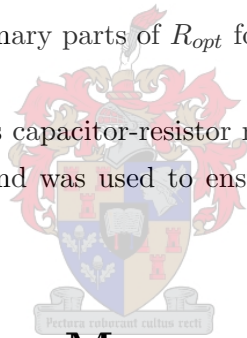


Figure 5.8: The real and imaginary parts of R_{opt} for the drain matching circuit.

as shown in Figure 5.9. The series capacitor-resistor network connected between the matching transmission line (TL2) and ground was used to ensure that the amplifier is unconditionally stable.



5.4 Power Amplifier Measurements

The input reflection, gain and 1 dB compression point of the two designed amplifiers and the Motorola test amplifier were measured and compared. The measured results follows in the two sections below.

Line-Stub Matching Amplifier Measurements

The designed class-AB amplifier's small-signal S-parameters were measured on a HP8753 vector network analyser. Figure 5.10 shows the comparison between the simulated and measured S-parameters of the class-AB amplifier. The measured input reflection (the trace marked ClassAB Amp Measured, \diamond marker) at a shifted center frequency (890 MHz) is -19.6 dB. The measured small-signal gain (the trace marked ClassAB Amp Measured, ∇ marker) across the design frequency band vary with less than a 1 dB and is measured as 18.3 dB.

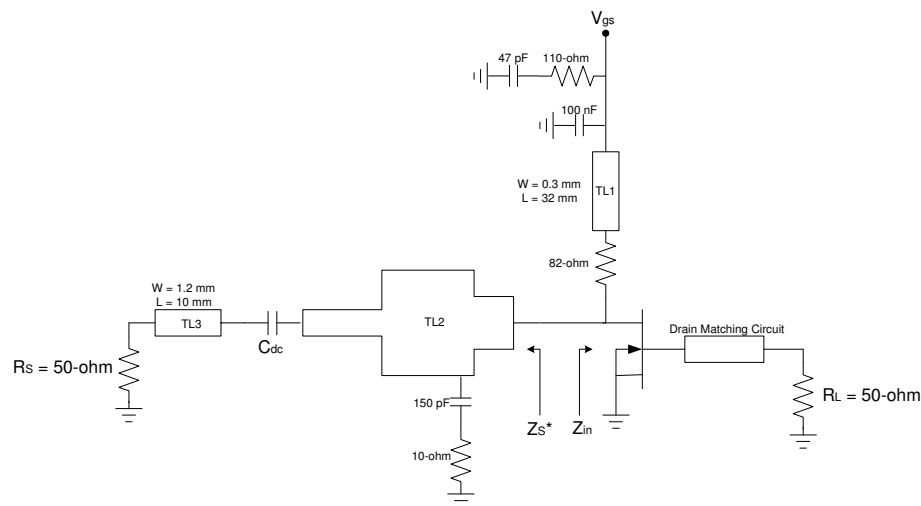


Figure 5.9: A schematic of the gate bias and matching circuit for the class-AB amplifier.

The amplifier circuit's input matching open-circuit stub was tuned in the Microwave Office environment. The transmission line's electrical length depends on the dielectric constant of the substrate and the fringing capacitance at the open-ended side. To compensate for these effects the transmission line should be shorter. The line was trimmed by 4 mm, almost double the distance calculated in Microwave Office. This is an indication that the fringing capacitance have a larger influence than predicted by the Microwave Office simulations. Figure 5.11 shows the comparison between the simulated and fine-tuned measured S-parameters of the class-AB amplifier. The measured input reflection (the trace marked Measured ClassAB Amp, \diamond marker) at the center frequency (945 MHz) is -17.6 dB and is -16.3 dB and -14.9 dB at the minimum (930 MHz) and maximum (960 MHz) frequencies respectively. The small-signal gain (the trace marked ClassAB Amp, ∇ marker) across the design frequency band vary with less than a 1 dB and is measured as 19.1 dB. The measured data correlates very well with the simulated data.

The amplifier was only designed to be conditionally stable and is only stable for a certain range of passive source and load impedances. Conditional stability is when stability circles cross certain areas of the Smith chart (certain impedances can satisfy oscillation conditions), however, the input and output impedances may never fall inside the unstable areas. The amplifier has regions where the device output impedance falls within the unstable area, as shown in Figure 5.12. The amplifier's source impedances are well outside the input stability circles while the load impedances falls within the output instability area, as shown in Figure 5.12. While power measurements were performed on the amplifier the device failed at an output power of approximately 3 Watt. After failure, a gate current of several milliamperes was measured. This is an indication that the transistor's gate-source diode has failed. The output impedance of the driver (shown in Figure 5.17) amplifier was questionable, but Figure 5.13 illustrates that the

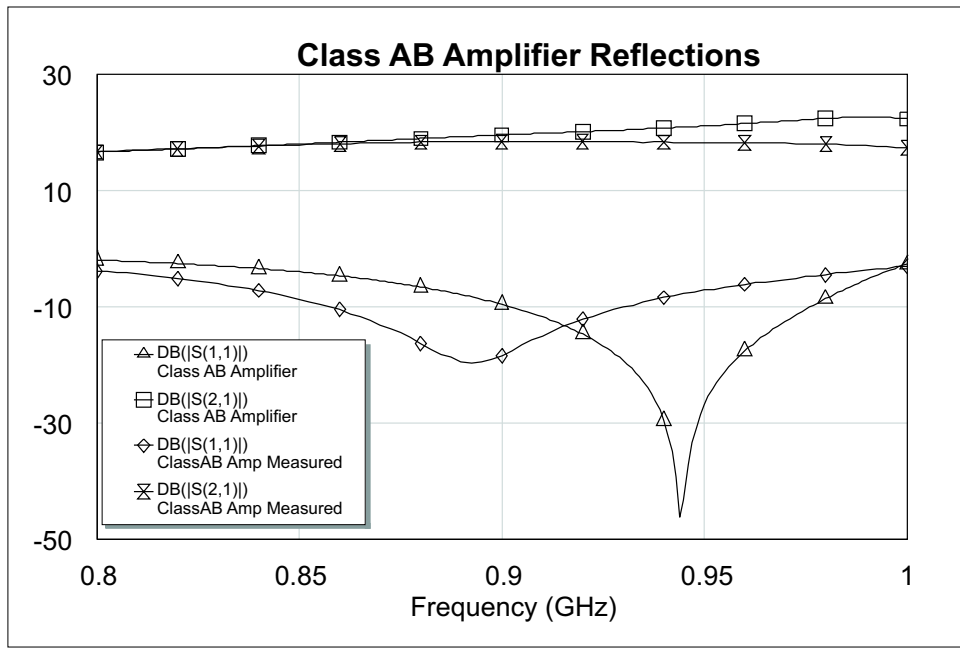


Figure 5.10: A comparison between the measured amplifiers gain and input reflection, traces marked Measured ClassAB Amp, and the simulated amplifiers gain and input reflection, traces marked Class AB Amplifier.

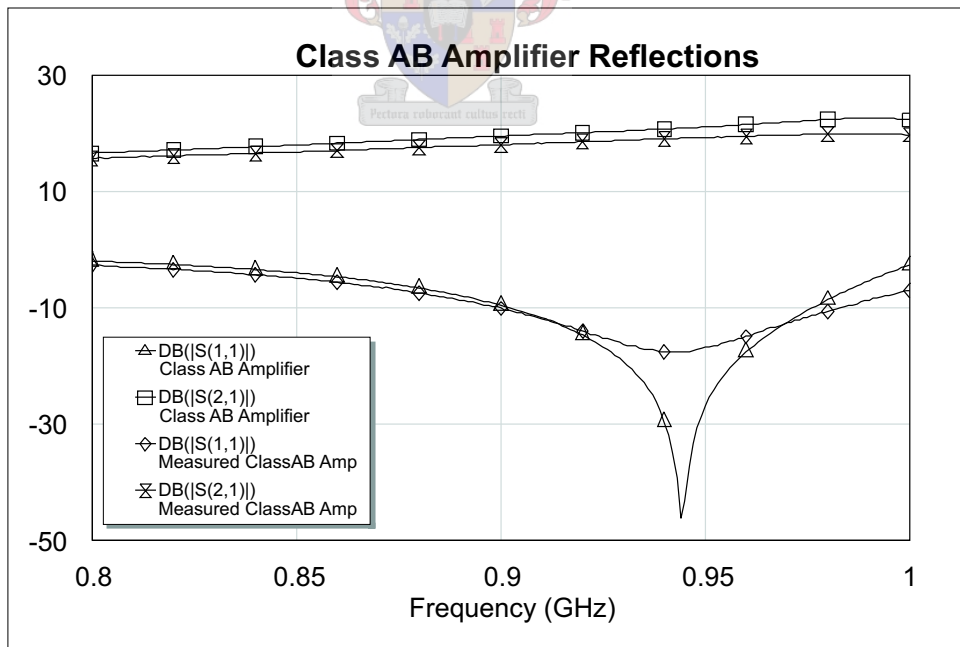


Figure 5.11: A comparison between the measured fine-tuned amplifiers gain and input reflection, traces marked Measured ClassAB Amp, and the simulated amplifiers gain and input reflection, traces marked Class AB Amplifier.

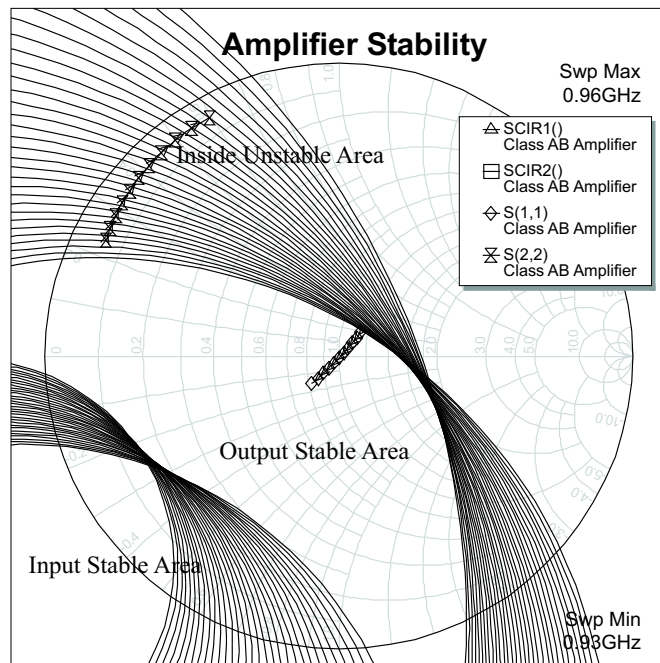


Figure 5.12: The class-AB amplifiers simulated input and output reflections (traces marked \diamond and ∇) and the input and output stability circles (traces marked \triangle and \square). The data is shown on a 50 Ohm Smith chart.

driver amplifier is reasonably matched.

Quarter-Wave Transformer Matching Amplifier and Motorola Test Amplifier Measurements

The designed class-AB amplifier's small-signal S-parameters were measured on a HP8510C vector network analyser. Figure 5.14 shows the comparison between the simulated and measured S-parameters of the class-AB amplifier. Both the gain and input reflection measurements are shifted with 70 MHz from the design center frequency. The gain measured at 870 MHz (the trace marked ClassABamp Measurements, \square marker), is 16.33 dB while the simulated gain at 945 MHz (the trace marked Class AB Amplifier, \diamond marker), is 17.87 dB, as shown in Figure 5.14. The amplifier's measured input reflection at 870 MHz (the trace marked ClassABamp Measurements, \triangle marker), is -27.61 dB with a 70 MHz band (from 840-910 MHz) below -10 dB. The small-signal gain measured in this frequency band vary with 0.6 dB. The amplifier's simulated input reflection at 945 MHz (the trace marked Class AB Amplifier, ∇ marker), is -24.29 dB with a 60 MHz band below -10 dB, as shown in Figure 5.14.

The measured data correlates well with the simulated data except for the shift in center frequency. However, when an inductance of 2.2 nH is added between the series capacitor-resistor

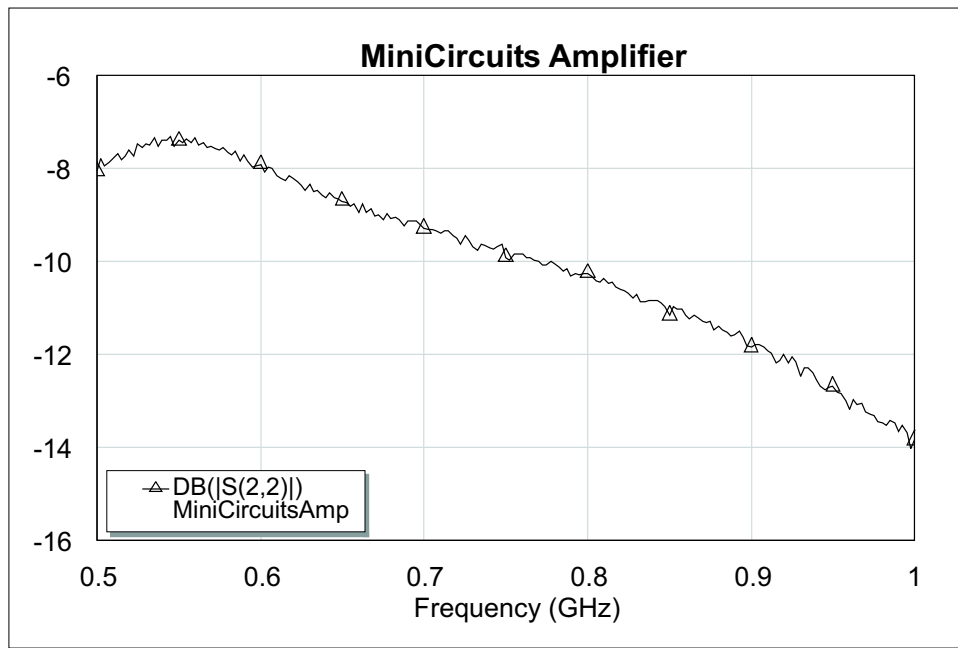


Figure 5.13: The output reflection of the mini-circuits driver amplifier.

network and ground (see stabilisation network in Figure 5.9), and the dielectric constant of the substrate used is changed to 10.01 (from 9.96), the design amplifier's gain and input reflection data is the same as the measured data, as shown in Figure 5.15. This inductance originates from the parasitic inductance of the SMD stabilising resistor and the inductance of the via pad used to connect the resistor to ground. This inductance was not taken into account during initial simulations because accurate models for the resistor and via pad were not available. A second transistor was used to build this amplifier and the small-signal equivalent circuit could differ for this transistor and can also be responsible for the shift in frequency.

The test amplifier circuit obtained from the Motorola data sheet, as illustrated in Appendix C, was implemented on Taconic RF-35-0300, 30 mil, $\epsilon_r = 3.55$ substrate. This is the exact substrate specified by Motorola. The amplifier's small-signal S-parameters were measured on an HP8510C vector network analyser and is shown in Figure 5.16. The amplifier was designed to operate at 945 MHz. Measured data shows that the amplifier only operates at 800 MHz, a 145 MHz difference. The amplifier's measured gain (the trace marked MotorolaAmp, \diamond marker), is 7.7 dB. The amplifier's input and output reflections (the traces marked MotorolaAmp, \triangle and \square markers respectively), is -0.33 dB and -2.5 dB respectively. The input matching network is poorly designed and nearly all input power is reflected. However, the Motorola design makes provision for three tunable capacitors which can be used to adjust the input matching network.

The HP8562 spectrum analyser was used to perform swept power gain measurements on both the

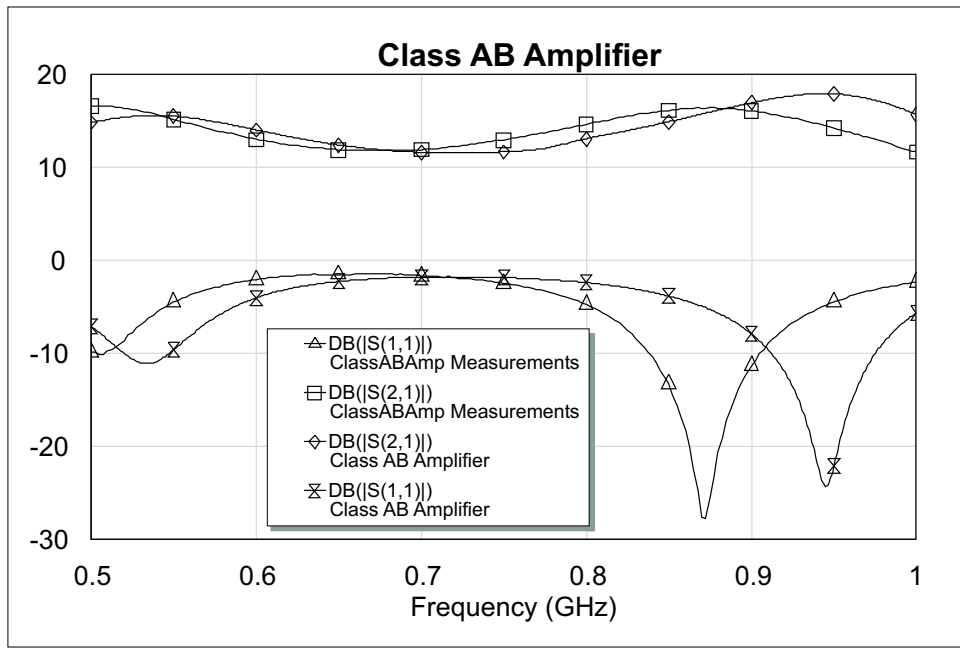


Figure 5.14: A comparison between the amplifier’s simulated gain and input reflection (traces marked Class AB Amplifier) and the amplifier’s measured gain and input reflection (traces marked ClassABamp Measurements).

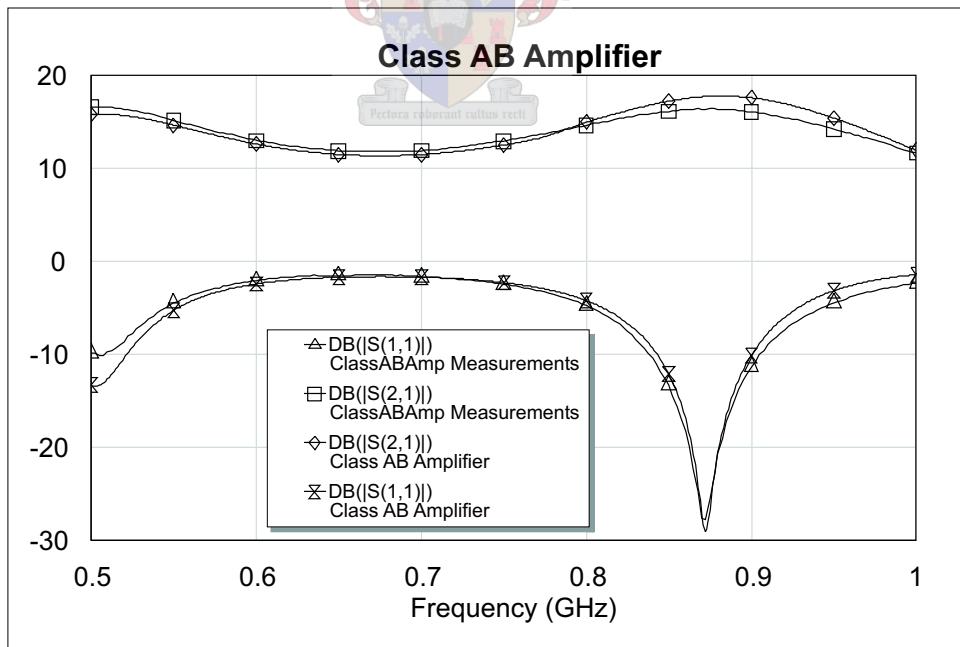


Figure 5.15: A comparison between the amplifier’s fine-tuned gain and input reflection (traces marked Class AB Amplifier) and the amplifier’s measured gain and input reflection (traces marked ClassABamp Measurements).

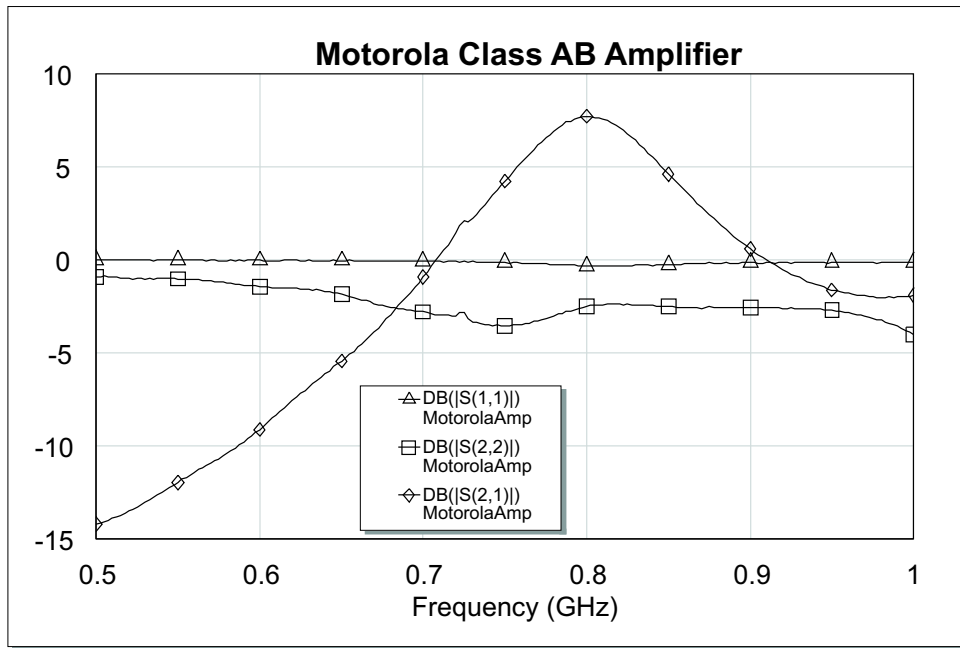


Figure 5.16: The Motorola class-AB amplifier’s measured gain (trace marked ◇), input and output reflections (traces marked △ and □ respectively).

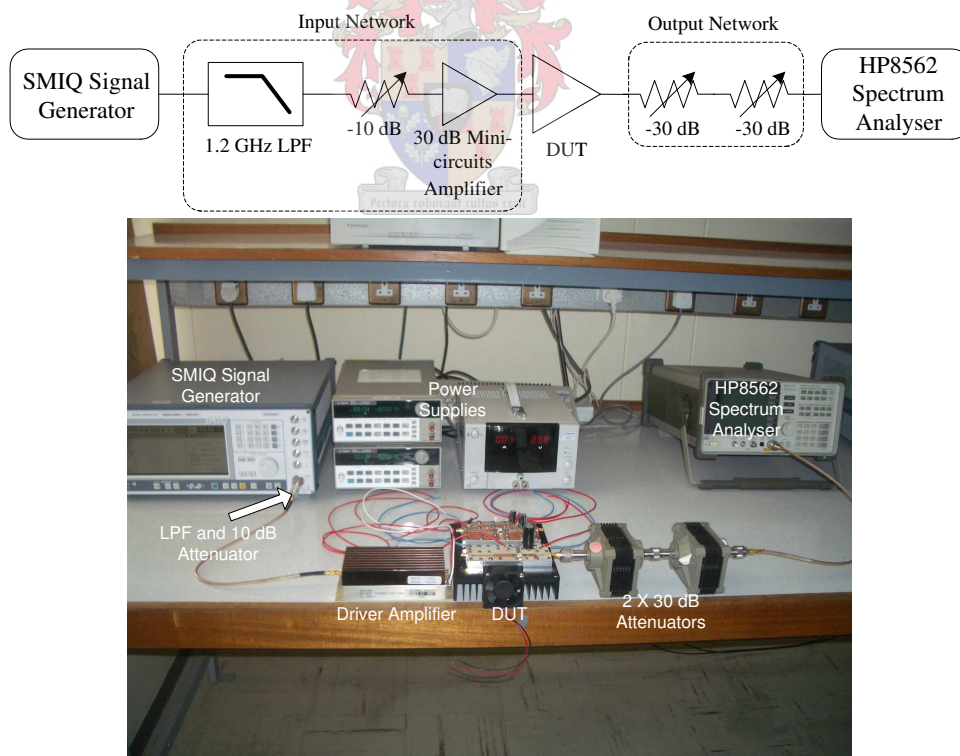


Figure 5.17: A schematic and photo representation of the measurement setup used to perform swept power amplifier (DUT) measurements with a HP8562 spectrum analyser.

Motorola test amplifier and the designed amplifier. The basic setup for power gain measurements with the spectrum analyser and a signal generator is shown in Figure 5.17. The 1.2 GHz low pass filter ensures that the levels of the signal generator harmonics are low enough while the 10 dB attenuator ensure that the signal generator's power levels do not drive the mini-circuits amplifier into compression. The attenuator also improves the match between the signal source and the mini-circuits driver amplifier. The mini-circuits amplifier is used to provide enough power to drive the DUT amplifier into compression to ensure that its characteristics is measured over most of its output power range. Two 30 dB attenuators are placed in front of the spectrum analyser because the input power levels to the HP8562 spectrum analyser should be kept below 30 dBm to prevent damage to the machine and the spectrum analyser mixer input power levels should be below -30 dBm to prevent distortion in the measurement. Both the input and output networks S-parameters, as shown in Figure 5.17, were measured and used to transference the measured power levels to the input and output of the amplifier being measured.

Figure 5.18 shows the input versus output power levels for both the design amplifier and the Motorola test amplifier. Power levels at different frequencies were measured. The design amplifier's gain measured with the spectrum analyser is 14.77 dBm, an output signal of 31.6 Watt is measured for an input signal of 1 Watt. To quantify the linear operating range of the amplifier, the 1 dB compression point is defined as the power level for which the output power has decreased by 1 dB from the ideal characteristic. The designed amplifier's 1 dB compression point is 45 dBm (31.6 W, referred to the output), as shown in Figure 5.18. The measured 1 dB compression for the designed amplifier input power is 28 dBm, which is also the compression point of the mini-circuit driver amplifier. A driver amplifier with a higher compression point is required because the mini-circuits driver is suspected to enter compression before the designed (DUT) amplifier. The measured gain for the Motorola test amplifier is 20 dB and the 1 dB compression point is 45 dBm (referred to the output). The amplifier's gain measured on the network analyser was 7.7 dB, and differs with 12.3 dB. The explanation for this phenomenon is difficult because the same measurement setup was used for both amplifier power measurements. It is suspected that the driver amplifier could present the correct input impedance to the Motorola amplifier and therefore the increase in gain.

Figure 5.19 shows the drain current as a function of input power for both the design amplifier and the Motorola test amplifier. When the input signal is small these amplifiers operate in class-A mode, however, when the input signal increase the drain current increase and the amplifiers operate in class-AB mode.

Table 5.1 compares the measured results of the designed amplifier and the Motorola test amplifier. From this comparison it is clearly noticeable that the amplifier designed with the small-signal equivalent circuit performs better than the Motorola test amplifier.

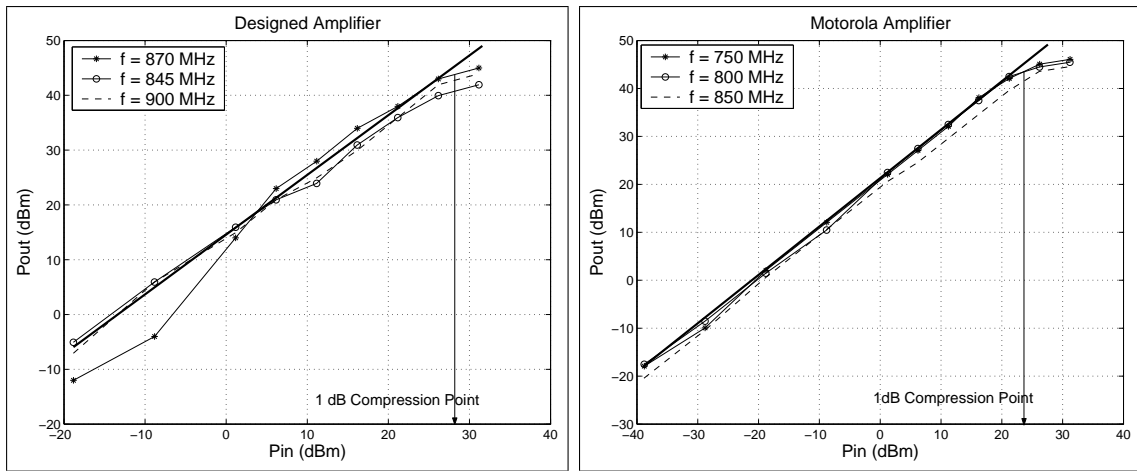


Figure 5.18: The input versus output power levels for both the designed amplifier and Motorola test amplifier. Power levels at different frequencies for each amplifier are shown.

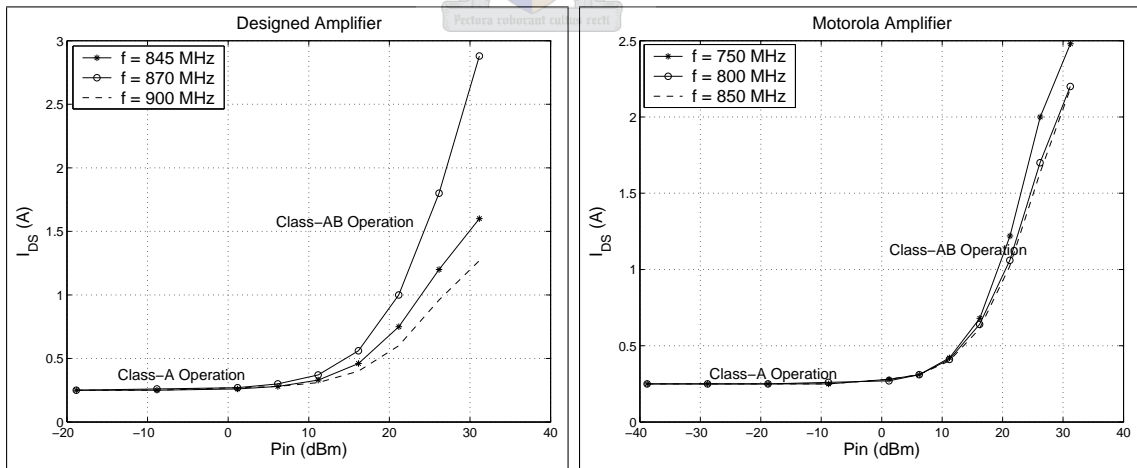


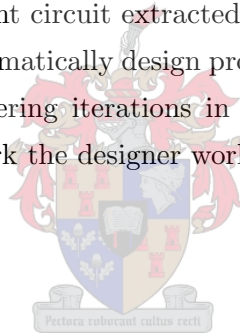
Figure 5.19: The drain current as a function of input power for both the designed amplifier and Motorola test amplifier. Currents at different frequencies for each amplifier are shown.

	Design Amplifier	Motorola Amplifier
P_{1dB} (dBm)	45	45
Gain (dB)	16.33	7.7
S_{11} (dB)	-27.61	-0.33
Bandwidth (MHz)	70	60

Table 5.1: A comparison of the amplifier design with the quarter-wave transformer matching and the Motorola test circuit design.

5.5 Conclusion

A class-AB power amplifier was designed with the small-signal equivalent circuit extracted in the previous chapter. Compared to the amplifier designed by Motorola, better gain, input reflection and power measurement results are obtained with the designed amplifier. The designed amplifier confirm that the small-signal equivalent circuit extracted is accurate for power amplifier design applications. The Motorola amplifier design is very complicated and uses a great deal of tunable passive components. The equivalent circuit extracted provide more detailed information about the device that allows a more systematically design procedure for power amplifiers. The detailed information allows reverse engineering iterations in a more sensible manner, while with the Motorola tunable capacitor network the designer works in the dark.



Chapter 6

General Conclusion

6.1 Conclusion

Two different fixtures has been presented based on 3.5 mm coaxial connectors and microstrip TRL calibrations standards. The mechanical advantage of the generalised TRL fixture makes it possible to design the fixtures electrical environment to be the same as the final products. The first TRL fixture, the split connector fixture, did not present results as expected. The second fixture, the split block fixture, delivered acceptable results and was used to perform further measurements.

The split block TRL fixture was used to perform the substrate parameter extraction. Two different methods were used to extract both the dielectric constant and the characteristic impedance of the microstrip transmission lines. The values of the characteristic impedance determined could be used to set the reference impedance of the TRL calibrations to improve the accuracy with which network parameters are measured. The exact value extracted for the dielectric constant could be used in designing more accurate circuits on this particular substrate.

The split block TRL fixture enable the designer to perform measurements in an arbitrary low impedance environment. This allows S-parameter measurements on transistors with low port impedances which can not be accurately measured in a 50 Ohm system. Without these accurate S-parameters the equivalent circuit model extraction is not possible. The split block low impedance TRL test fixture was used to extract the small signal equivalent circuit model for a Motorola LDMOS power transistor. The modeling procedure was divided into three steps. The first step was to generate an equivalent model for the metal-ceramic package. This was obtained with the help of LDMOS empty metal-ceramic packages. The second step was to extract the device small-signal extrinsic parameters, these parameters represent the bond-wires connecting

the gate and drain leads to the intrinsic transistors-die. The third and final step was to extract the transistors intrinsic elements which represents the intrinsic transistor-die.

A class-AB power amplifier was designed with the small-signal equivalent circuit extracted. Compared to the amplifier designed by Motorola, better measured results are obtained with the designed amplifier. The designed amplifier prove that small-signal equivalent circuit extracted was helpful. The equivalent circuit extracted for the LDMOS transistor provide a reliable tool with which the designer could design more accurate and viable power amplifiers.

6.2 Recommendations

The split connector TRL test fixture has been implemented as a low impedance device measurement tool. This test fixture's measurement results were unsatisfying. The split connector fixture is attractive from both a mechanical and measurement point of view, and it is recommended that this structure be investigated further. For a first recommendation this fixture can be further developed to a working instrument.

The small-signal equivalent circuit model can be expanded with pulsed bias measurements. This current-voltage characterisation approximate the behavior of the transistor under large signal RF conditions more closely. There are three issues that are addressed by pulsed I-V measurements namely, surface state occupancy, thermally induced changes in the output current due to self-heating of the device and the inability to perform measurements at DC power levels higher than those that can tolerated continuously without destroying the device [50]. With this data accurate nonlinear device models can be created.


For a final recommendation, the procedure used on the 30 Watt LDMOS transistor can be extended to develop a model for the 250 Watt LDMOS transistor. The 250 Watt amplifiers can be cascaded with 4-way power dividers and combiners to obtain a 1 kW amplifier. Continuing in this way the 1 kW amplifier can be combined to obtain amplifiers of higher (e.g. 12 kW) peak output powers. These amplifiers are typically used in modern radar systems.

Appendix A

Klopfenstein Taper Matlab Code

KlopTaper.m

```
function KlopTaper(Zload,Zzero,Ripple,freq,er,h,w,fname);  
  
[Imp,Len] = KlopfensteinTaperFunction(Zload,Zzero,Ripple,freq,er);  
  
Zin = flipplr(Imp');  
  
[Wd] = LineWidthTaper(Zin,er,h,w,freq);  
  
Lengths = Len*1e3;  
Widths = Wd;  
  
TaperFirstOrderLine(fname,1,Widths,Lengths);  
  
display('Your Klopfenstein Taper Design Is Finished !!!!');
```



KlopfensteinTaperFunction.m

```
% The calculation of a Klopfenstein Taper, calculating the reflection  
% coefficient and the impedance. This function return the impedance  
% of the line and line length for a certain substrate and terminated  
% impedances.  
%  
% Author: P. J. de V. Malan  
% 29 July 2003  
%  
% Ripple The ripple in dB in the passband.  
% freq The minimum frequency for taper.  
% Er The Er of the substrate used.  
%  
% [Impedance,Length]=KlopfensteinTaperFunction(Zload,Zzero,Ripple,freq,Er);  
%  
  
function [Impedance,Length]=KlopfensteinTaperFunction(Zload,Zzero,Ripple,freq,Er);  
  
close all;  
  
Impedance = [];  
Length = [];  
  
%Rho is the reflection coefficient at zero frequency.
```

```

ZL = Zload;
Zo = Zzero;
Rho = 0.5*log(ZL/Zo);

%The maximum ripple in the passband, Rhom.
RippledB = Ripple;
A = acosh(10^(RippledB/20));

%Reflection coefficient
BetaL = 0:0.01:6*pi;
Gamma = Rho.*exp(-i.*BetaL).*((cos(sqrt(BetaL.^2-A^2)))./cosh(A));

% figure;
% plot(BetaL,abs(Gamma));grid;
% title('Klopfenstein Taper Reflection Coefficient. ');
% xlabel('\betaL = 2\pi(L/\lambda)');
% ylabel('\Gamma');

%The characteristic impedance for the Klopfenstein taper.
c = 0;
p = 0;
s = 0;
L = 1;
Npts = 1001;
dz = 0.01;
for z = 0.1:dz:L
    x = (2*z/L)-1;
    if (x == 1)
        x = 0.9999;
    end
    dy = (x-0)/(Npts-1);
    y = 0:dy:x;

    F = A.*sqrt(1-y.^2);
    G = besseli(1,F);
    krnl = G./F;
    size(krnl,2);
    if (size(y,2)==0)
        integral = 0;
    else
        integral = (dy/3)*(krnl(1) + 4*sum(krnl(2:2:Npts-1),2) + 2*sum(krnl(3:2:Npts-2),2) + krnl(Npts));
    end
    c = c + 1;
    p(c) = x;
    s(c) = integral;

    Z = exp(0.5*log(Zo*ZL) + (Rho/cosh(A))*A^2.*integral);
    Impedance(c) = Z;
end;
% figure;
% plot(p,s);grid;
% axis([0 1 0 4]);
% title('Plot of \Phi(z,A). ');
% %Parameter A determines the maximum magnitude of reflection coefficient in pass band.
% xlabel('z');
% ylabel('\Phi(z,A)');
%
figure;
plot(p,Impedance);grid;
title('Klopfenstein Taper Impedance Graph');
xlabel('x/l');
ylabel('Impedance (\Omega)');

%Calculate the length of line
f = freq;
c = 299.792458e6;
er = Er;

```



```

ref = 3.27; %Reflection of 0.1

c_new = c/sqrt(er);
lambda = c_new/f;

Length = (ref/(2*pi))*lambda;
Impedance = Impedance';

```

LineWidthTaper.m

```

% Following program obtained from Finney and Thomas,"Calculus"
% second edition p.187-p.194 and Peter V. O'Neil, "Advanced
% Engineering Mathematics" second edition p.1063.
%
% Zline          calculated line impedance from taper.
% Zsol           impedance calculated from width equation.
%
% Computes the line width of a microstrip line. All
% physical dimensions are in mm, while the frequency is in Hz.
% Er and H is the substrate parameters. The first value of
% the line width is based on a guess.
%
% [Width]=LineWidthTaper(Zline,er,h,W,f);

function [Width]=LineWidthTaper(Zin,er,h,w,freq);

Width = [];

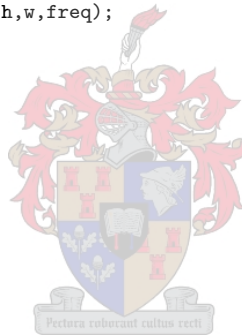
q = waitbar(0,'Please wait...');

for a = 1:length(Zin)
    waitbar(a/100,q)
    for n = 1:1:1000
        Fun = fun(Zin(a),er,h,w,freq);
        Der = der(Zin(a),er,h,w,freq);

        w = w + Fun./Der;

        n = n + 1;
    end;
    Width = [Width w];
end;
close(q)

```



TaperFirstOrderLine.m

```

function TaperFirstOrderLine(fname,scale,Widths,Lengths);

% fname = Name of taper design 'Taper.dxf'
% scale = AutoCad scale 1 means 1:1
% Widths = matrix of widths starting with the smallest
% Lengths = length of taper
%
% TaperLine(fname,scale,Widths,Lengths);

[fid,err]=DXF_start(fname,scale);

% First Order Approx. Lines -----

width = Widths./2;
x = 0;

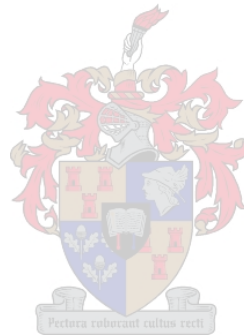
```

```
y = 0;
L = Lengths/(length(width));

for n = 1:length(width)-1
    DXF_line(fid,x,width(n),x+L,y+width(n+1),1,1);
    DXF_line(fid,x,-width(n),x+L,-y-width(n+1),1,1);
    x = x + L;
end;

% for n = 1:length(width)-1
%     DXF_line(fid,x,-width(n),x+L,-y-width(n+1),1,1);
%     x = x + L;
% end;

% -----
DXF_end(fid);
```



Appendix B

Microstrip Parameter Extraction Matlab Code

comp2method.m

% This routine compares Hoer and Marks methods

```
clear all;  
close all;
```

```
% Load data  
load TThru.txt;  
load TThruM.txt;  
load TLine1.txt;  
load TLine2.txt;  
load TShort.txt;  
load TLLine.txt;  
load Line1.txt;  
load ThruM.txt;
```



% Setup the measured frequency range

```
fsrt = 500e6;  
fstp = 8e9;  
Np = 400;  
fvalid = 8e9;  
inc = (fstp-fsrt)/Np;  
f = fsrt:inc:fstp;  
freq = f';
```

% Load data in useable matrix form

```
TThru_S11 = TThru(:,1) + i.*TThru(:,2);  
TThru_S21 = TThru(:,3) + i.*TThru(:,4);  
TThru_S12 = TThru(:,5) + i.*TThru(:,6);  
TThru_S22 = TThru(:,7) + i.*TThru(:,8);  
Stthru = [TThru_S11 TThru_S21 TThru_S12 TThru_S22];
```

```
TThruM_S11 = TThruM(:,1) + i.*TThruM(:,2);  
TThruM_S21 = TThruM(:,3) + i.*TThruM(:,4);  
TThruM_S12 = TThruM(:,5) + i.*TThruM(:,6);  
TThruM_S22 = TThruM(:,7) + i.*TThruM(:,8);  
StthruM = [TThruM_S11 TThruM_S21 TThruM_S12 TThruM_S22];
```

```
TLine1_S11 = TLine1(:,1) + i.*TLine1(:,2);  
TLine1_S21 = TLine1(:,3) + i.*TLine1(:,4);
```



```

TLine1_S12 = TLine1(:,5) + i.*TLine1(:,6);
TLine1_S22 = TLine1(:,7) + i.*TLine1(:,8);
Stline1 = [TLine1_S11 TLine1_S21 TLine1_S12 TLine1_S22];

TLine2_S11 = TLine2(:,1) + i.*TLine2(:,2);
TLine2_S21 = TLine2(:,3) + i.*TLine2(:,4);
TLine2_S12 = TLine2(:,5) + i.*TLine2(:,6);
TLine2_S22 = TLine2(:,7) + i.*TLine2(:,8);
Stline2 = [TLine2_S11 TLine2_S21 TLine2_S12 TLine2_S22];

TShort_S11 = TShort(:,1) + i.*TShort(:,2);
TShort_S21 = TShort(:,3) + i.*TShort(:,4);
TShort_S12 = TShort(:,5) + i.*TShort(:,6);
TShort_S22 = TShort(:,7) + i.*TShort(:,8);
Stshort = [TShort_S11 TShort_S21 TShort_S12 TShort_S22];

TLLine_S11 = TLLine(:,1) + i.*TLLine(:,2);
TLLine_S21 = TLLine(:,3) + i.*TLLine(:,4);
TLLine_S12 = TLLine(:,5) + i.*TLLine(:,6);
TLLine_S22 = TLLine(:,7) + i.*TLLine(:,8);
Stlline = [TLLine_S11 TLLine_S21 TLLine_S12 TLLine_S22];

SlineM{1} = Stline1;
SlineM{2} = Stline2;

% Perform a two-tier calibration with a short refelection standard
[Sx,GL1] = trl2_short(Stthru,Stshort,SlineM,StthruM,freq,3.5e9);

% Line parameter extraction Method 1

beta = imag(GL1);
c = 299.792458e6;
lgth1 = 11.9/1000;
lgth2 = 3.8/1000;
fr = 3.5e9;
f1 = find(f < fr);
f2 = find(f >= fr);

Eeff1 = ((c.*beta(f1))./(2.*pi.*f(f1).*(lgth1)))^2;
Eeff2 = ((c.*beta(f2))./(2.*pi.*f(f2).*(lgth2)))^2;

Ereff = [Eeff1';Eeff2'];

findex = find(f > 0.7e9);

[Zo1,Er1,ErEffMeas1,Ereff1_1,Z1] = extract_mlz_02(10.2,0.635,5.0,Ereff(findex)...
,freq(findex)');
Er1

% Line parameter extraction Method 2

length1 = 12/1000;
length2 = 0/1000;

EreffEst = 8.613;

[G,Er2,ErEffMeas2,Ereff1_2,Z2] = cpc_mm(Line1,ThruM,length1,length2,EreffEst,f);
Er2

% Line parameter extraction Method 3

S21 = Line1(:,3) + i.*Line1(:,4);
AngS21 = unwrap(angle(S21));

Eeff = ((c.*abs(AngS21))./(2.*pi.*f'.*length1))^2;
[Zo,Er3,ErEffMeas3,Ereff1_3,Z3] = extract_mlz_02(10.2,0.635,5.05,Eeff,f');
Er3

```

```

% Plots
findex2 = find(f < 6e9);

plot4(f(findex2)/1E9,ErEffMeas1(findex2),ErEffMeas2(findex2),ErEffMeas3(findex2)...
,ErEff1_1(findex2),'Eeff(Engen & Hoer Two-Tier Cal)', 'Eeff(Marks Full 2-port Cal)')...
,'Eeff(Marks Two-Tier Cal)', 'Eeff(Guass-Newton Fit)',3,'Frequency (GHz)')...
,'Effective Dielectric Constant')

plot33(f(findex2)/1E9,Z1(findex2),Z2(findex2),Z3(findex2),...
'Impedance(Engen & Hoer Two-Tier Cal)', 'Impedance(Marks Full 2-port Cal)')...
,'Impedance(Marks Full 2-port Cal)',3,'Frequency (GHz)', 'Zo (\Omega)')

trl2short.m

function [Sx,GL,R1]=trl2_short(Sthru,Sshort,SlineM,Sdut,freq,fr);

% TRL2 performs a multi-line two-tier TRL calibration for a vector network
% analyser. The calibration differs from the TRL function in that
% provision is made for the use of multiple line standards in order to
% increase the calibration bandwidth and/or increase accuracy. There is
% no limit on the number of line standards that can be used.
%
% The first calibration consist of a normal co-axial SOLT two-port calibration
% followed by measurements on the TRL calibration standards and the DUT. The
% function then performs the second tier of the calibration by de-embedding the
% effect of the TRL test fixture from the DUT measurements using the measurements
% performed on the TRL calibration standards.
%
% The function uses the following input parameters:
%
% Sthru Four colom matrix containing S-Parameters of the thru measurement on
% TRL test fixture.
% Sshort Four colom matrix containing S-Parameters of the open measurement on
% TRL test fixture. Only S11 and S22 is of interest here and the S21 and
% S12 data which will be in the noise floor of the VNA will be discarded.
% SlineM A cell array consisting of four colom matrixes containing S-Parameters
% of the different line measurements on the TRL test fixture.
% The cell matrix is build up by specifying:
%
% SlineM{1}=Sline1, SlineM{2}=Sline2,...,SlineM{k}=Slinek
%
% Sdut Four colom matrix containing S-Parameters of the DUT inserted into the
% TRL test fixture.
% f Frequencies at which S-Parameters were measured in Hz.
% fr Vector containing the frequencies in Hz where one line
% standard takes over from another
%
% The coloms of the S-Parameter matrix represent [S11 S21 S12 S22].
%
% format: [Sx,GL]=trl2(Sthru,Sopen,SlineM,Sdut,freq,fr)
%
% The output consists of the de-embedded device S-Parameters (Sx), and the propagation
% constant (GL) of the line standard used in the TRL calibration. The propagation constant
% can be used to calculate the characteristic impedance of the microstrip calibration
% line. Since microstrip is a dispersive transmission line, the characteristic impedance
% will vary as a function of frequency. The measured S-Parameters will be normalised with
% respect to the actual characteristic impedance of the transmission line calibration
% standard. By extracting this impedance, the S-Parameter data can be renormalised to
% 50 Ohm.
%
% See TRLPOST.M for some post processing functions that can be performed.
%
% Writer : C. van Niekerk
% Version : 3.50
% Date : 07/06/1995

% This program is based on the work in the presented in the following paper:

```

```

%
% [1] G.F. Engen, C.A. Hoer, "Thru-Reflect-Line: An Improved Technique for
%      Calibrating the Dual Six-Port Automatic Network Analyser,"
%      IEEE Trans. MTT, Vol. 27, No. 12, December 1979, pp. 987-998

% Define the imaginary constant
i=sqrt(-1);

% Convert the measured s-parameters of the DEVICE to one variable

S11d = Sdut(:,1);
S21d = Sdut(:,2);
S12d = Sdut(:,3);
S22d = Sdut(:,4);

% Convert the measured s-parameters of the REFLECT standard to one variable

S11r = Sshort(:,1);
S22r = Sshort(:,4);

% Convert the measured s-parameters of the THRU standard to one variable

S11t = Sthru(:,1);
S21t = Sthru(:,2);
S12t = Sthru(:,3);
S22t = Sthru(:,4);

% Convert the measured s-parameters of the LINE standard to one variable
%
% The different line standards used in the calibration is combined here by
% using the frequency range for which they are assigned.

fr=[min(freq) fr max(freq)];

for n=2:length(fr)

    k=find( freq(find(freq <= fr(n))) >= fr(n-1));

    S11l(k) = SlineM{n-1}(k,1);
    S21l(k) = SlineM{n-1}(k,2);
    S12l(k) = SlineM{n-1}(k,3);
    S22l(k) = SlineM{n-1}(k,4);

end;

% Compute the wave cascading matrix for the thru standard

R11t = -(S11t.*S22t - S12t.*S21t)./S21t;
R12t = S11t./S21t;
R21t = -S22t./S21t;
R22t = 1 ./ S21t;

% Compute the wave cascading matrix for the line standard

R11l = -(S11l.*S22l - S12l.*S21l)./S21l;
R12l = S11l./S21l;
R21l = -S22l./S21l;
R22l = 1 ./ S21l;

% Compute the wave cascading matrix for the device standard

R11m = -(S11d.*S22d - S12d.*S21d)./S21d;
R12m = S11d./S21d;
R21m = -S22d./S21d;
R22m = 1 ./ S21d;

% Calculate the two possible virtual error networks for port A

```

```

% and port B using the s-parameters of the thru and line standards

% Determine the number of frequency points

nfreq=length(freq);

for n = 1:nfreq

    Rt = [ R11t(n) R12t(n) ; R21t(n) R22t(n) ];
    Rl = [ R11l(n) R12l(n) ; R21l(n) R22l(n) ];
    T = Rl*inv(Rt);

% Solve a set of quadratic equations to get the values of r11a/r21a
% and r12a/r22a

    A = T(2,1);
    B = T(2,2) - T(1,1);
    C = -T(1,2);

    K1 = (-B + sqrt((B^2)-4*A*C))/(2*A);
    K2 = (-B - sqrt((B^2)-4*A*C))/(2*A);

% Choose between the two possible roots to get the right values for
% b and c/a

    if abs(K1)<abs(K2)
        b = K1;
        ca = 1/K2;
    end;

    if abs(K2)<abs(K1)
        b = K2;
        ca = 1/K1;
    end;

% Calculates the propagation constant of the LINE standard.

    GL(n) = -log(T(1,1)+T(1,2)*ca);

% Calculates "a"

    w1 = S11r(n);
    w2 = S22r(n);

    g = 1/S21t(n);
    d = -(S11t(n)*S22t(n) - S12t(n)*S21t(n));
    e = S11t(n);
    f = -S22t(n);

    gamma = (f-d*ca)/(1-e*ca);
    beta_alfa = (e-b)/(d-b*f);

    a = sqrt(((w1-b)*(1+w2*beta_alfa)*(d-b*f))/((w2+gamma)*(1-w1*ca)*(1-e*ca)));

% Calculates the reflection coefficients at each port to determine the correct
% sign that should be assigned to a

    R1a = (w1-b)/(a-w1*a*ca);
    R1b = (w1-b)/(w1*a*ca-a);

% A short is used for the reflection measurement. Use this information to
% chose the sign of a

    if abs(angle(R1a)*180/pi)<90
        a = -a;
        as(n) = a;
        c = ca*a;
    end;

```



```

if abs(angle(R1b)*180/pi)<90
    a = a;
    as(n) = a;
    c = ca*a;
end;

R1(n) = (w1-b)/(a-c*w1);

alfa = (d-b*f)/(a*(1-e*ca));
beta = beta_alfa*alfa;

r22p22 = R11t(n)/(a*alfa + b*gamma);

IRa = [ 1 -b ; -c a ];
IRb = [ 1 -beta ; -gamma alfa ];

Rm = [ R11m(n) R12m(n) ; R21m(n) R22m(n) ];

Rx = 1/(r22p22*(alfa-gamma*beta)*(a-b*c))*IRa*Rm*IRb;

S11x(n) = Rx(1,2)/Rx(2,2);
S12x(n) = Rx(1,1) - Rx(1,2)*Rx(2,1)/Rx(2,2);
S21x(n) = 1/Rx(2,2);
S22x(n) = -Rx(2,1)/Rx(2,2);

end;

Sx=[S11x.' S21x.' S12x.' S22x.'];

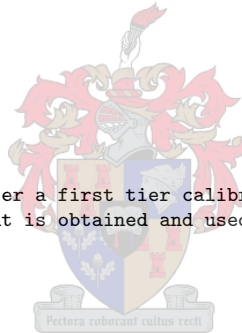
```

ttcalerext.m

```

% This routine do a TRL calibration after a first tier calibration was performed. From the
% TRL calibration a propogation constant is obtained and used to calculate Er_eff and the
% line impedance.
%
% Author : P.J.De V. Malan
% Date   : Augustus 2004
%

```



```

clear all;
close all;

```

```

% Load measured data

```

```

load TThru.txt;
load TThruM.txt;
load TLine1.txt;
load TLine2.txt;
load TShort.txt;
load TLLine.txt;

```

```

% Setup the measured frequency range

```

```

fsrt = 500e6;
fstp = 8e9;
Np = 400;
fvalid = 8e9;
inc = (fstp-fsrt)/Np;
f = fsrt:inc:fstp;
freq = f';

```

```

% Load data in useable matrix form

```

```

TThru_S11 = TThru(:,1) + i.*TThru(:,2);
TThru_S21 = TThru(:,3) + i.*TThru(:,4);
TThru_S12 = TThru(:,5) + i.*TThru(:,6);

```

```

TThru_S22 = TThru(:,7) + i.*TThru(:,8);
Stthru = [TThru_S11 TThru_S21 TThru_S12 TThru_S22];

TThruM_S11 = TThruM(:,1) + i.*TThruM(:,2);
TThruM_S21 = TThruM(:,3) + i.*TThruM(:,4);
TThruM_S12 = TThruM(:,5) + i.*TThruM(:,6);
TThruM_S22 = TThruM(:,7) + i.*TThruM(:,8);
StthruM = [TThruM_S11 TThruM_S21 TThruM_S12 TThruM_S22];

TLine1_S11 = TLine1(:,1) + i.*TLine1(:,2);
TLine1_S21 = TLine1(:,3) + i.*TLine1(:,4);
TLine1_S12 = TLine1(:,5) + i.*TLine1(:,6);
TLine1_S22 = TLine1(:,7) + i.*TLine1(:,8);
Stline1 = [TLine1_S11 TLine1_S21 TLine1_S12 TLine1_S22];

TLine2_S11 = TLine2(:,1) + i.*TLine2(:,2);
TLine2_S21 = TLine2(:,3) + i.*TLine2(:,4);
TLine2_S12 = TLine2(:,5) + i.*TLine2(:,6);
TLine2_S22 = TLine2(:,7) + i.*TLine2(:,8);
Stline2 = [TLine2_S11 TLine2_S21 TLine2_S12 TLine2_S22];

TShort_S11 = TShort(:,1) + i.*TShort(:,2);
TShort_S21 = TShort(:,3) + i.*TShort(:,4);
TShort_S12 = TShort(:,5) + i.*TShort(:,6);
TShort_S22 = TShort(:,7) + i.*TShort(:,8);
Stshort = [TShort_S11 TShort_S21 TShort_S12 TShort_S22];

TLLine_S11 = TLLine(:,1) + i.*TLLine(:,2);
TLLine_S21 = TLLine(:,3) + i.*TLLine(:,4);
TLLine_S12 = TLLine(:,5) + i.*TLLine(:,6);
TLLine_S22 = TLLine(:,7) + i.*TLLine(:,8);
Stlline = [TLLine_S11 TLLine_S21 TLLine_S12 TLLine_S22];

SlineM{1} = Stline1;
SlineM{2} = Stline2;

% Perform a two-tier calibration with a short refelection standard

[Sxshort, GLs] = trl2_short(Stthru, Stshort, SlineM, Stshort, freq, 3.5e9);
[Sxline1, GLl1] = trl2_short(Stthru, Stshort, SlineM, Stline1, freq, 3.5e9);
[Sxline2, GLl2] = trl2_short(Stthru, Stshort, SlineM, Stline2, freq, 3.5e9);
[Sxthru, GLt] = trl2_short(Stthru, Stshort, SlineM, Stthru, freq, 3.5e9);
[SxthruM, GLtM] = trl2_short(Stthru, Stshort, SlineM, StthruM, freq, 3.5e9);
[Sxlline, GLl1] = trl2_short(Stthru, Stshort, SlineM, Stlline, freq, 3.5e9);

wrtstone(Sxshort, freq./1e6, 'TTCalShort.s2p', 'Short');
wrtstone(Sxline1, freq./1e6, 'TTCalLine1.s2p', 'Line1');
wrtstone(Sxline2, freq./1e6, 'TTCalLine2.s2p', 'Line2');
wrtstone(Sxthru, freq./1e6, 'TTCalThru.s2p', 'Thru');
wrtstone(SxthruM, freq./1e6, 'TTCalThruM.s2p', 'ThruM');
wrtstone(Sxlline, freq./1e6, 'TTCalLLine.s2p', 'LLine');

% Line parameter extraction

beta = imag(GLtM);
c = 299.792458e6;
lgth1 = 11.9/1000;
lgth2 = 3.8/1000;
fr = 3.5e9;
f1 = find(f < fr);
f2 = find(f >= fr);

Eeff1 = ((c.*beta(f1))./(2.*pi.*f(f1).*(lgth1))).^2;
Eeff2 = ((c.*beta(f2))./(2.*pi.*f(f2).*(lgth2))).^2;

Ereff = [Eeff1'; Eeff2'];

findex = find(f > 0.7e9);

```

```
[Zo,Er] = extract_mlz_02(10.2,0.635,5.0,Ereff(findex),freq(findex)');
```

```
Er
GLtM
```

cpcmm.m

```
function [G,Er,ErEffMeas,Ereff1,Z0] = cpc_mm(Sline1,Sline2,length1,length2,EreffEst,f);
```

```
% Determine the complex propagation constant of two transmission lines,
% line1 and line2 of different lengths. All equations from "A Multiline
% Method of Network Analyzer Calibration" and "Multiline TRL Revealed".
```

```
%
% Sline1 - Line 1 S-parameters
% Sline2 - Line 2 S-parameters
% length1 - Length of Line 1 (mm)
% length2 - Length of Line 2 (mm)
% EreffEst - An estimate of the complex effective dielectric constant
% f - Frequency range of operation (Hz)
```

```
%
% Author: P.J.De V. Malan
% Date : Augustus 2004
```

```
%
```

```
% Define the imaginary constant
```

```
i = sqrt(-1);
```

```
% Convert the measured s-parameters of line 1
```

```
S11Line1 = Sline1(:,1) + i.*Sline1(:,2);
S21Line1 = Sline1(:,3) + i.*Sline1(:,4);
S12Line1 = Sline1(:,5) + i.*Sline1(:,6);
S22Line1 = Sline1(:,7) + i.*Sline1(:,8);
```

```
% Convert the measured s-parameters of line 2
```

```
S11Line2 = Sline2(:,1) + i.*Sline2(:,2);
S21Line2 = Sline2(:,3) + i.*Sline2(:,4);
S12Line2 = Sline2(:,5) + i.*Sline2(:,6);
S22Line2 = Sline2(:,7) + i.*Sline2(:,8);
```

```
for k = 1:length(f),
```

```
    % Calculate the wave cascading matrix of line 1
```

```
    M11Line1 = (S12Line1(k).*S21Line1(k) - S11Line1(k).*S22Line1(k))./S21Line1(k);
    M12Line1 = S11Line1(k)./S21Line1(k);
    M21Line1 = -S22Line1(k)./S21Line1(k);
    M22Line1 = 1./S21Line1(k);
```

```
    MLine1 = [M11Line1 M12Line1;M21Line1 M22Line1];
```

```
    % Calculate the wave cascading matrix of line 2
```

```
    M11Line2 = (S12Line2(k).*S21Line2(k) - S11Line2(k).*S22Line2(k))./S21Line2(k);
    M12Line2 = S11Line2(k)./S21Line2(k);
    M21Line2 = -S22Line2(k)./S21Line2(k);
    M22Line2 = 1./S21Line2(k);
```

```
    MLine2 = [M11Line2 M12Line2;M21Line2 M22Line2];
```

```
    % The measured cascade matrices of the two transmission lines
```

```
    Mnew = MLine2.*inv(MLine1);
```

```
    M11 = Mnew(1,1);
```

```
    M12 = Mnew(1,2);
```

```

M21 = Mnew(2,1);
M22 = Mnew(2,2);

% Calculate the two eigenvalues

Lamda1M = ((M11 + M22) + sqrt((M11 - M22)^2 + (4*M12*M21)))/2;
Lamda2M = ((M11 + M22) - sqrt((M11 - M22)^2 + (4*M12*M21)))/2;

% Calculate the propagation constant

EigenValue_A = 0.5.*(Lamda1M + (1./Lamda2M));
EigenValue_B = 0.5.*(Lamda2M + (1./Lamda1M));

gamma_est = MarksGammaEst(EreffEst,f(k));

deltalength = length1 - length2;
P1 = round((imag(gamma_est*deltalength) - imag(-log(EigenValue_A')))/(2*pi));
P2 = round((imag(gamma_est*deltalength) - imag(-log(EigenValue_B')))/(2*pi));

gamma_A = (-log(EigenValue_A') + i*2*pi*P1)/deltalength;
gamma_B = (-log(EigenValue_B') + i*2*pi*P2)/deltalength;

% Compute difference in eigenvalues

Differ1 = abs(gamma_A.*deltalength - gamma_est.*deltalength)./abs(gamma_est.*deltalength);
Differ2 = abs(gamma_B.*deltalength + gamma_est.*deltalength)./abs(-gamma_est.*deltalength);

if Differ1 <= Differ2,
    G = gamma_A;
else
    G = gamma_B;
end;
Gamma(k) = G;
end;

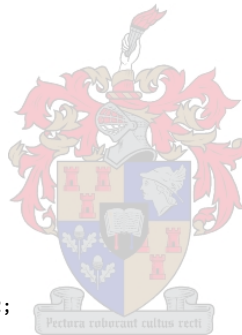
% Plots
c = 299.792458e6;

Eeff = ((c.*abs(Gamma))./(2.*pi.*f)).^2;

findex = find(f < 6e9);

[Zo,Er,ErEffMeas,Ereff1,Z0] = extract_mlz_02(10.2,0.635,5.0,Eeff(findex)',f(findex)');

```



extractmlz02.m

```

function [Z1,Er,ErEffMeas,Ereff1,Z0]=extract_mlz_02(er_init,h,W,Eeff_init,f);

% EXTRACT_MLZ extracts impedance and dielectric constant of the microstrip
% line and the substrate on which it is made. The impedance is determined
% as a function of frequency and therefore includes the dispersive
% behaviour of the substrate. The measured data used to extract the
% transmission line characteristics is obtained from the complex
% propagation constant of the line determined from a TRL calibration. The
% extracted impedance can be used to re-normalise S-parameters measured
% with a TRL test fixture. The curve fitting is done using a least squares
% damped Gauss-Newton procedure.
%
% All physical units are specified in mm and the frequency is in Hz.
%
% format: [Z,er]=extract_mlz(er_init,L,h,W,GL,freq);
%
NumIt = 2;

% Calculates the effective wavelength Beta of the microstrip LINE standard

```



```

ErEffMeas = Eeff_init';

% Calculate the effective dielectric constant for the microstrip line using
% the design parameters of the microstrip line

for k=1:length(f),
    Ereff0(k) = Eeff(er_init,h,W,f(k)/1E9);
end;

% Use a Guass-Newton optimization routine to adjust the dielectric constant
% to obtain the best fit between the modelled and measured effective
% dielectric constant across the frequency band of interest.

Er = OptGsNwt1(NumIt,er_init,h,W,ErEffMeas,f);
for k=1:length(f),
    Ereff1(k) = Eeff(Er,h,W,f(k)/1E9);
    ZO(k)=imp(er_init,h,W,f(k));
    Z1(k)=imp(Er,h,W,f(k));
end;

% Plot the comparative results
%
% Compare the measured, initial and extracted effective dielectric constant
% of the TRL microstrip line

% figure;
% plot(f/1E9,ErEffMeas,'blue')
% hold on
% grid on
% xlabel('Frequency (GHz)')
% ylabel('Effective Dielectric Constant')
% title('Effective Dielectric Constant of the TRL Microstrip Line Standard')
%
% plot(f/1E9,Ereff0,'green')
% plot(f/1E9,Ereff1,'red')
% legend('Eeff','Eeff(Design)','Eeff(Guass-Newton)');

% Plot the characteristic impedance of the TRL microstrip line standard as
% a function of frequency.

% figure;
% plot(f/1E9,ZO);
% hold on
% grid on
% xlabel('Frequency (GHz)')
% ylabel('Zo')
% title('Characteristic Impedance of the TRL Microstrip Line Standard')

% -----

% Additional functions to be used in the automated extraction Er extraction
% algorithm

function [Er]=OptGsNwt1(NumIt,er_init,h,W,ErEffMeas,f);

%

Er = er_init;
ErNew = Er;

for k=1:length(f)
    ErMod(k)=Eeff(Er,h,W,f(k)/1E9);
end;
OldFnc = sum(abs(ErEffMeas-ErMod).^2);
q=0;
pp=1;

```

```

while (pp > 0.01)

    q=q+1;
    alpha = 1;
    DoRefine = 1;
    NumRefine=0;
    ErOld=Er;

    while (DoRefine == 1);

        [dx,e] = StepGsNwt1(Er,h,W,ErEffMeas,f);
        ErNew = Er + alpha*dx;
        [e]=errvect(ErNew,h,W,ErEffMeas,f);
        EFnc = sum(e.^2);

        if (EFnc < OldFnc),
            Er = ErNew;
            OldFnc=EFnc;
            DoRefine = 0;
        end; % { if EFnc }

        alpha=alpha/2;
        NumRefine=NumRefine+1;
        if (NumRefine > 10), DoRefine = 0; end;

    end; % { while DoRefine }

    pp=abs(ErOld-Er)/ErOld*100;

    if (q > 6), pp=0; end;

end; % { while pp }

function [dx,e0]=StepGsNwt1(Er0,h,W,ErEffMeas,f);

% StepGsNwt1(Xp,ParNum,mn,S,freq) calculates the optimisation
% step for a one dimensional small-signal extraction problem
% using the Gauss-Newton algorithm. Central point differensiation
% is used in determining the Jacobian and Hessian functions.
%
% format: [dx]=StepGsNwt1(Er,h,W,Beta,f)
%
dif=Er0/100;
Er1=Er0+dif;
Er2=Er0-dif;

[e0]=errvect(Er0,h,W,ErEffMeas,f);
[e1]=errvect(Er1,h,W,ErEffMeas,f);
[e2]=errvect(Er2,h,W,ErEffMeas,f);

J=(e1-e2)./(2*dif);
A=sum(J.^2);
C=sum(J.*e0);
dx=-C/A;

function [e]=errvect(Er,h,W,ErEffMeas,f);

for k=1:length(f)
    Ereff(k) = Eeff(Er,h,W,f(k)/1E9);
end;
e=abs(Ereff-ErEffMeas);

```

MarksGammaEst.m

```

function [gamma_est] = MarksGammaEst(Er_est,f);

% Determines the estimated gamma of a transmission line. The "Multiline TRL Revealed"
% paper's equations were implemented here.
%
% Er_est - An estimate of the complex effective dielectric constant
% f      - Frequency range of operation (Hz)
%
% P.J.De V. Malan

% Constants

j = sqrt(-1);
pi = 3.1416;

w = 2.*pi.*f;
Er = Er_est;
c = 299.792458e6;

% Propagation Equations

G = j.*(w./(c)).*sqrt(real(Er) - j.*(imag(Er)./(f./10^9)));

alpha = real(G);
beta = imag(G);

Ereff = ((c.*imag(G))./(2.*pi.*f)).^2;

gamma_est = G;

% Plots

% figure;
% plot(f./1e9,(20/log(10)).*alpha);grid;
% title('Attenuation');
% xlabel('Frequency (GHz)');
% ylabel('dB');
%
% figure;
% plot(f./1e9,(beta.*pi)./180);grid;
% title('Phase');
% xlabel('Frequency (GHz)');
% ylabel('Degrees');
%
% figure;
% plot(f./1e9,real(Ereff));grid;
% title('E_r,_e_f_f');
% xlabel('Frequency (GHz)');
% ylabel('E_r');

```



Appendix C

LDMOS Power Amplifier Circuit Layout

C.1 Class-AB Power Amplifier Designed with Line-Stub Matching Networks

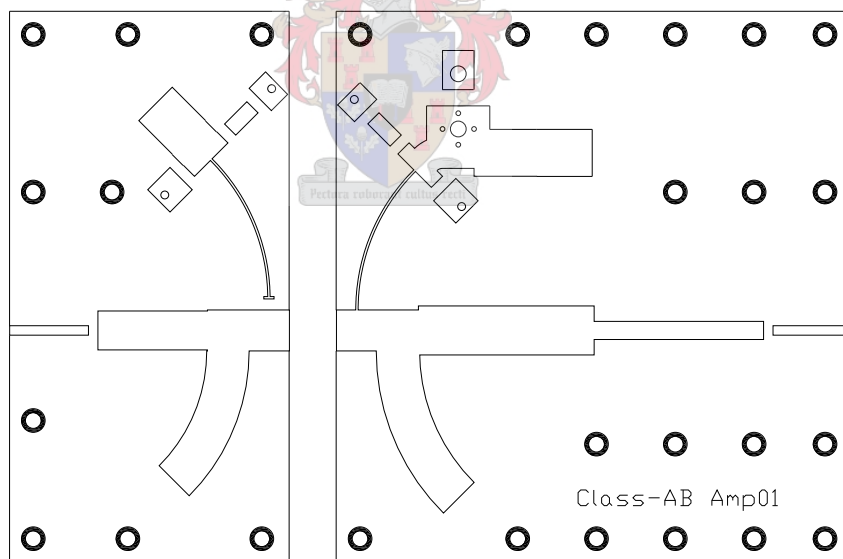


Figure C.1: The class-AB load line pulsed amplifier schematic. This figure is not set to scale.

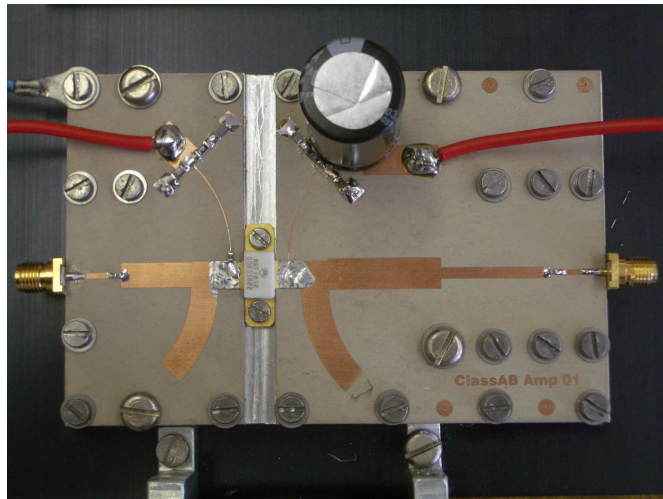


Figure C.2: The class-AB load line pulsed amplifier photo representation. This figure is not set to scale.

C.2 Motorola Test Circuit Layout

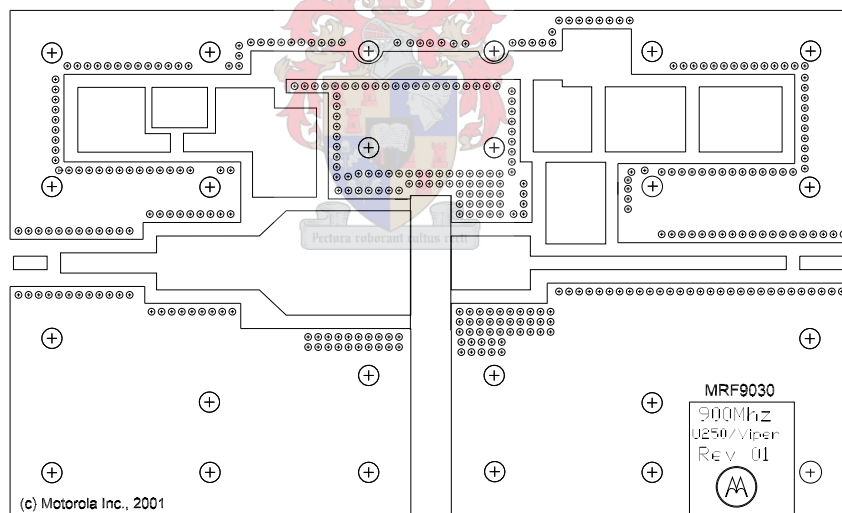


Figure C.3: The Motorola 945 MHz broadband test circuit schematic. This figure is not set to scale.

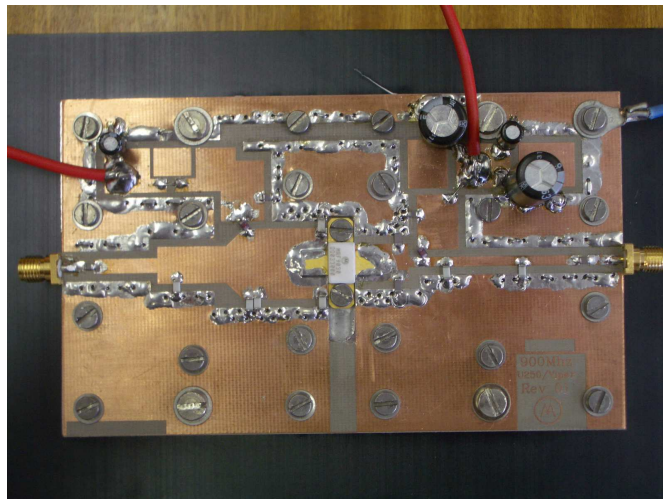


Figure C.4: The Motorola 945 MHz broadband test circuit photo representation. This figure is not set to scale.

C.3 Class-AB Power Amplifier Designed with Quarter-Wave Transformer Matching Networks

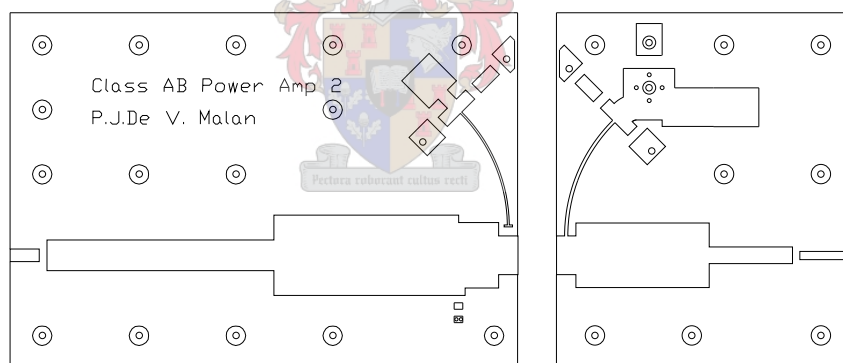


Figure C.5: The class-AB load line pulsed amplifier schematic. This figure is not set to scale.

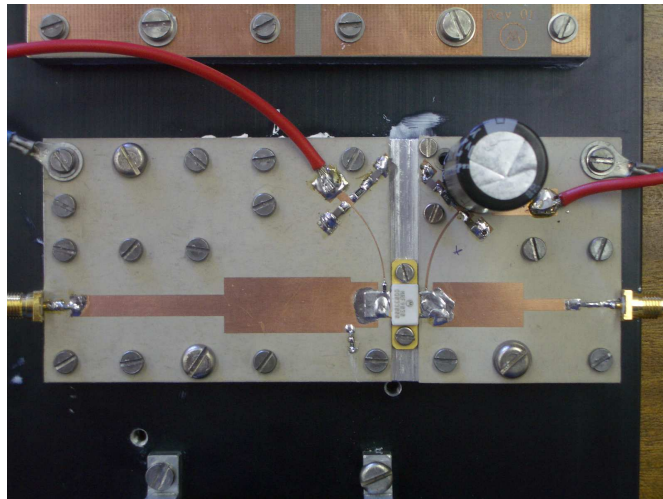


Figure C.6: The class-AB load line pulsed amplifier photo representation. This figure is not set to scale.

C.4 Motorola Transistor Intrinsic Layout



Figure C.7: The Motorola MRF9030 intrinsic photo layout. Notice the gate and drain bond-wire pads as well as the cascaded MOSFETs to obtain a single 30 Watt transistor.

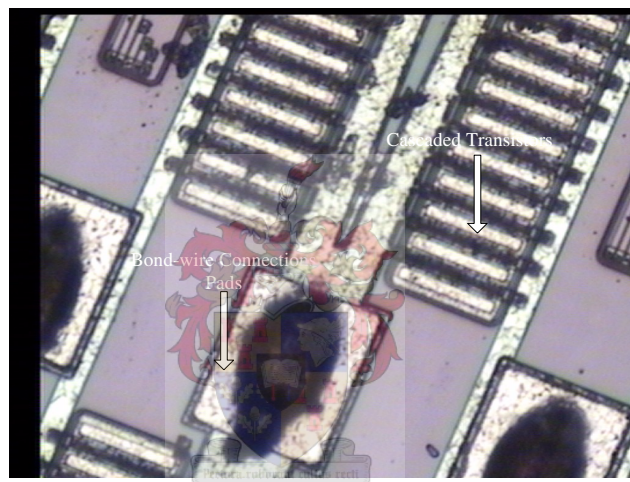


Figure C.8: The Motorola MRF9030 intrinsic photo layout (zoomed in). Again, notice the gate and drain bond-wire pads as well as the cascaded MOSFETs to obtain a single 30 Watt transistor.

Bibliography

- [1] F.H. Raab, P. Asbeck, S. Cripps, P.B. Kenington, Z.B. Popovic, N. Pothecary, J.F. Sevic, and N.O. Sokal, "RF and microwave power amplifier and transmitter technologies - Part 1," *High Frequency Electronics*, pp. 22–36, May 2003.
- [2] Y. Yang, J Yi, and B. Kim, "Accurate RF large-signal model of LDMOSFETs including self-heating effect," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 2, February 2001.
- [3] C. Fager, J.C. Pedro, N. Borges de Carvalho, and H. Zirath, "Prediction of IMD in LDMOS transistor amplifiers using a new large-signal model," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 12, December 2002.
- [4] J. Jang, O. Tornblad, T. Arnborg, Q. Chen, K. Banerjee, Z. Yu, and R.W. Dutton, "RF LDMOS characterization and its compact modeling," *IEEE*, 2001.
- [5] J.F. Sevic, "A sub 1 ohm load-pull quarter-wave pre-matching network based on a two-tier trl calibration," *Maury Microwave Corporation*, pp. 73–81, dec 2002.
- [6] C. Shih, "Advanced TRL (Through-Reflect-Line) fixture design and error analyses for RF high power transistor characterization and automatic load pull measurement," pp. 72–76.
- [7] T. Liang, J.A. Pla, P.H. Aaen, and M. Mahalingam, "Equivalent-circuit modeling and verification of metal-ceramic packages for RF and microwave power transistors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 6, pp. 709–714, June 1999.
- [8] S.C. Cripps, *RF Power amplifiers for Wireless Communications*, Artech House, 1999.
- [9] D.M. Pozar, *Microwave Engineering*, John Wiley and Sons, Inc, 2nd edition, 1998.
- [10] R.W. Klopfenstein, "A transmission line taper of improved design," *Proceedings of the IRE*, pp. 31–35, Jan. 1955.
- [11] R.E. Collin, *Foundations For Microwave Engineering*, McGraw-Hill International, 2nd edition.
- [12] B.C. Wadell, *Transmission Line Design Handbook*.

- [13] Inc Applied Wave Research, *Microwave Office 2002*, v5.00 edition, 2002.
- [14] Hewlett Packard, *Network Analyser*, Agilent PN 8753-1.
- [15] D. Ballo, “Designing and calibrating RF fixtures for surface-mount devices,” 1996.
- [16] *Inter-continental Microwave*, <http://www.icmicrowave.com>.
- [17] Agilent PN 8720-2, *In-fixture Microstrip Device Measurements Using TRL Calibration*, Agilent Technologies, 2nd edition, 2000.
- [18] Agilent PN 8510-5B, *Specifying Calibration Standards for the Agilent 8510 Network Analyzer*, Agilent Technologies, 2nd edition, 2000.
- [19] D.F. Williams and R.B. Marks, “Comparison of on-wafer calibrations,” *National Institute of Standards and Technology*, pp. 68–81.
- [20] W. Oldfield, “Development of calibration and verification standards in microstrip to 60 GHz,” pp. 26–32.
- [21] Golio, *The RF and Microwave Handbook*, pp.9-40.
- [22] Hoffman, *Handbook of Microwave Integrated Circuits*, pp.180-190.
- [23] G.F. Engen and C.A. Hoer, ““Thru-Reflect-Line”: An improved technique for calibrating the dual six-port automatic network analyzer,” *IEEE Transactions Microwave Theory and Techniques*, vol. MTT-27, no. 12, pp. 987–993, December 1979.
- [24] D.C. DeGroot, J.A. Jargon, and R.B. Marks, “Multiline TRL revealed,” .
- [25] D.C. DeGroot, D.K. Walker, and R.B. Marks, “Impedance mismatch effects on propagation constant measurements,” *7th IEEE EPEP Conf. Dig.*, pp. 141–143, October 1996.
- [26] J.A. Jargon and R.B. Marks, “Two-tier multiline TRL for calibration of low-cost network analyzers,” pp. 1–8, December 1995.
- [27] R.B Marks and D.F. Williams, “Characteristic impedance determination using propagation constant measurements,” *IEEE Microwave and Guided Wave Letters*, vol. 1, no. 6, pp. 141–143, June 1991.
- [28] M.D. Janezic and J.A. Jargon, “Complex permittivity determination from propagation constant measurements,” *IEEE Microwave and Guided Wave Letters*, vol. 9, no. 2, pp. 76–78, February 1999.
- [29] R.B. Marks, “A multiline method of network analyzer calibration,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 39, no. 7, pp. 1205–1215, July 1991.
- [30] D.F. Williams, “Accurate characteristic impedance measurements on silicon,” *Publication of the National Institute of Standards and Technology*, pp. 1–5.

- [31] D.F. Williams, “Characteristic-impedance measurements error on lossy substrates,” *Publication of the National Institute of Standards and Technology*, pp. 1–5.
- [32] H. Cho and D.E. Burk, “A three-step method for the de-embedding of high-frequency s-parameter measurements,” June 1991.
- [33] E.P. Vandamme, D.M.M.-P. Schreurs, and C. van Dinther, “Improved three-step de-embedding method to accurately account for the influence of pad parasitics in silican on-wafer RF test-structures,” April 2001.
- [34] Y. Yang, Y.Y. Woo, J. Yi, and B. Kim, “A new empirical large-signal model of Si LDMOSFETs for high-power amplifier design,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 9, pp. 1626–1633, September 2001.
- [35] A.V. Grebennikov and F. Lin, “An efficient CAD-oriented large-signal MOSFET model,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 10, pp. 1732–1742, October 2000.
- [36] T. Johansson and T. Arnborg, “A novel approach to 3-D modeling of packaged RF power transistors,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 6, pp. 760–768, June 1999.
- [37] R. Gaddi, P.J. Tasker, and J.A. Pla, “Direct extraction of LDMOS small signal parameters from off-state measurements,” *Electronics Letters*, vol. 36, no. 23, pp. 1964–1966, November 2000.
- [38] F. Lin and G. Kompa, “FET model parameter extraction based on optimization with data-fitting and bidirectional search - a new concept,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 42, no. 7, pp. 1114–1121, July 1994.
- [39] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, “A new method for determining the FET small-signal equivalent circuit,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, no. 7, pp. 1151–1159, July 1988.
- [40] P. Roblin, S. Akhtar, and J. Strahler, “New non-quasi-static theory for extracting small-signal parameters applied to LDMOSFETs,” *IEEE Microwave and Guided Wave Letters*, vol. 10, no. 8, pp. 322–324, Augustus 2000.
- [41] M. Berroth and R. Bosch, “High-frequency equivalent circuit of GaAs FET’s for large-signal applications,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 39, no. 2, pp. 224–229, February 1991.
- [42] M. Berroth and R. Bosch, “Broad-band determination of the FET small-signal equivalent circuit,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 38, no. 7, pp. 891–895, July 1990.
- [43] D.E. Root and B. Hughes, “Principles of non-linear active device modeling for circuit simulation,” .

- [44] C.Y. Hang, Y. Qian, and T. Itoh, “High efficiency S-band class AB push-pull power amplifier with wide band harmonic suppression,” *IEEE*, 2001.
- [45] F.H. Raab, P. Asbeck, S. Cripps, P.B. Kenington, Z.B. Popovic, N. Potheary, J.F. Sevic, and N.O. Sokal, “RF and microwave power amplifier and transmitter technologies - Part 2,” *High Frequency Electronics*, pp. 22–36, May 2003.
- [46] J.L.B. Walker, *High-Power GaAs FET Amplifiers*, Artech House, 1993.
- [47] F. Giannini, G. Leuzzi, E. Limiti, and L. Scucchia, “Design-oriented non-linear analysis of class-AB power amplifiers,” *IEEE MTT-S Digest*, pp. 297–300, 1993.
- [48] R. Basset, “High-Power GaAs FET device bias considerations,” *Fujitsu Application 010*, pp. 1–7.
- [49] *Motorola*, <http://www.motorola.com>.
- [50] W. Clausen L. Dunleavy and T. Weller, *Pulsed I-V for Nonlinear Modeling*, Mod-elithics Inc. Technical Feature.

